Temperature Sensitive Behavioral Modeling of Analog to Digital Converters

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To my parents, my sine qua non.

Acknowledgments

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Abstract

Using commercial analog to digital converters (ADCs) outside their designed operating temperature range is inherently risky and device performance remains uncertain. Current methods of performance verification rely on expensive, time-consuming characterization procedures. A behavioral model capturing expected device performance, especially one which can be applied *a priori* and without testing, could enable system engineers to quickly downselect components for use within a system. To this end, a behavioral ADC model is described, tested and validated against measured performance.

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Chapter 1

Introduction

Digital electronics, the "brain" of modern spacecraft, perform storage, analysis, and transmission of valuable information obtained during a mission. Electronics on the periphery, at or near the interface between sensors and any central processing, are often analog or mixed-signal and subject to demanding environments including extreme temperature ranges and harsh radiation. To mitigate such effects, devices can be insulated from their environment using a special enclosure that offers temperature stability and some radiation shielding while incurring not insignificant power and weight costs. Ideally, one would like to be able to operate such electronics outside of the costly insulating environment but the main obstacle is the lack of guaranteed functionality when parts are operated outside their stated design ranges.

For mixed signal parts like ADCs, disruption of the digital circuitry and failure of internal reference voltage generators can result in total lack of output. Barring extensive testing and with little to no access to extreme temperature-sensitive transistor models and schematics, it is difficult to estimate *a priori* performance; nevertheless, it may be possible to identify performance trends correlated with particular technology nodes, architectures, or processes. This work seeks to characterize two commercial ADCs over a wide temperature range, observing changes in performance and functionality, and incorporating such changes into a behavioral model. Additionally, the ability to estimate performance from datasheet parameters and transfer curve trends is investigated. The ability to estimate a converter's

performance limitations purely from datasheet information would be an invaluable tool in a system engineer's arsenal.

1.1 Motivation

Testing for flight qualification imposes significant time and cost burdens on organizations while limiting the pool of potential parts which can feasibly be incorporated into an approved list upon which system designers can rely. Reducing test time allows more parts to be considered for qualification while screening potentially unreliable parts from consideration. When testing commercial off the shelf (COTS) parts, there is the additional question of functionality since in many cases parts will be operating outside their design ranges with respect to either temperature or radiation. Because these commercial parts will be operating outside of a region guaranteed by the manufacturer, it is very difficult if not impossible to state definitively whether a given part will continue to function and achieve acceptable performance. Nevertheless, the project aims to uncover underlying parametric trends in parts which can be used to estimate the degree of degradation experienced by a part. Such a technique would allow engineers to down-rate a part by designating it as having less than ideal but still acceptable performance.

1.2 Goals

The main goals of this work include the following: (a) demonstration of a generic ADC modeling approach which is able to incorporate temperature-dependent effects; (b) prediction from datasheet of ADC performance; and (c) development of architecture-specific models to capture archetypal behavior. Because several ADCs of different architectures were investigated, the modeling methodology needed to be generic and broadly applicable. Furthermore, the model would be built from input-output data, limiting the information available to characterize the model. However, there may be architecture-specific effects which are more readily captured by a model addressing such factors. In these cases, additional behavioral models targeting the specific architectures investigated were built.

Chapter 2

Background and Literature Review

2.1 Overview of ADC Theory & Architectures

ADCs are complex mixed signal chips that discretize a signal with respect to both time and value. This is done in order to interface with digital computer systems which recognize only a finite number of values and operate in discrete timesteps. For so-called Nyquist rate ADCs, the sampling procedure must be done quickly enough to maintain all information within a particular frequency band (the Nyquist zone). Ideally, this is done through impulse sampling whereby an amplifier instantaneously obtains the value of the input at regular intervals but practical circuit implementations, using a track and hold amplifier (THA), actually do so in two steps: first, the THA maintains a lock on the changing input signal during its tracking phase and second, it stores the value during the holding phase, usually as charge on a capacitor. An overview of THA behavior as well as architecture designs is presented below.

2.1.1 Track and Hold Amplifier

Switched capacitor networks used to implement THA functionality form the bulk of on-chip implementations. Figure 2.1 shows a typical example while Figure 2.2 shows the accompanying clock timing diagram, both from [1]. The opening and closing of switches

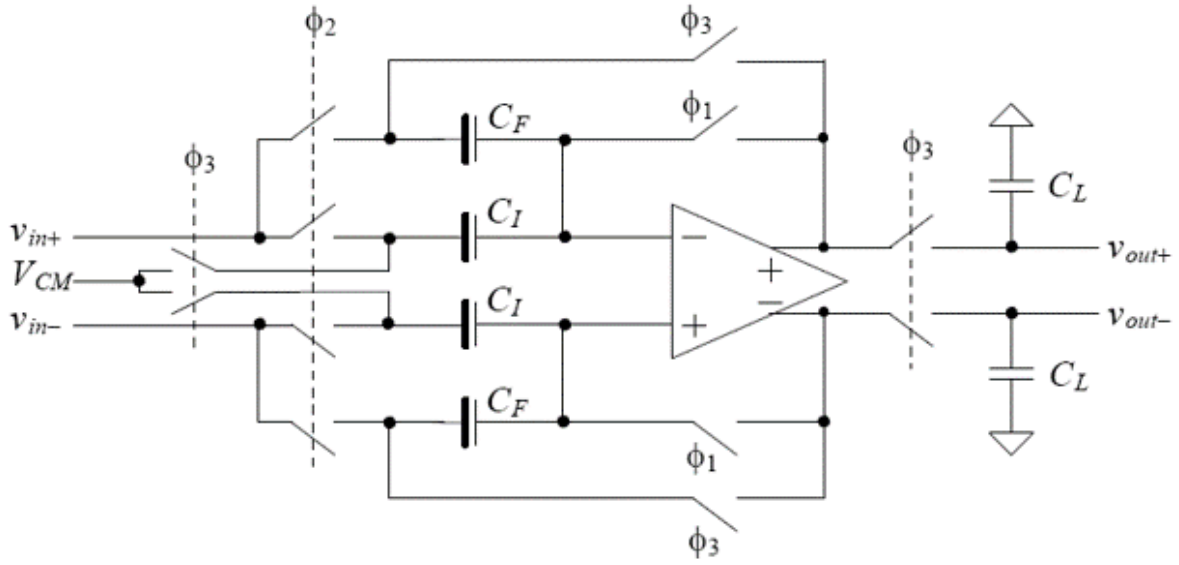


Figure 2.1: Typical THA Implementation from Baker

allows the amplifier to alternate between track and hold modes using charge sharing among capacitors to implement tracking, subtraction, gain, and hold functionality.

Tracking performance depends critically on amplifier performance. Large open-loop gain is required to obtain an output that is within 1 least significant bit (LSB) of the input in order to meet design requirements regarding accuracy. Sampling capacitors along with switch on-resistance must be sized to balance thermal noise contributions of resistors, which are better with larger capacitors, and speed requirements, which are more easily met with smaller capacitors. The time needed to acquire a step input, termed an amplifier's settling time, depends on bandwidth as well as the sizing of switches and sampling capacitors. When the amplifier's tracking of the input becomes slew rate (SR) limited, there is additional distortion added to the output so internal capacitor sizing of the amplifier is also a factor to consider during design to meet overall specifications.

During converter operation, the basic operation consists of two phases: first tracking the input and then maintaining the result for further processing. Referring to the timing diagram in Figure 2.2, switches ϕ_1 and ϕ_2 close in quick succession while switches ϕ_3 remains open, setting the amplifier in tracking mode. During this period, negative feedback action on the part of the amplifier maintains a representation of the input signal in the form of

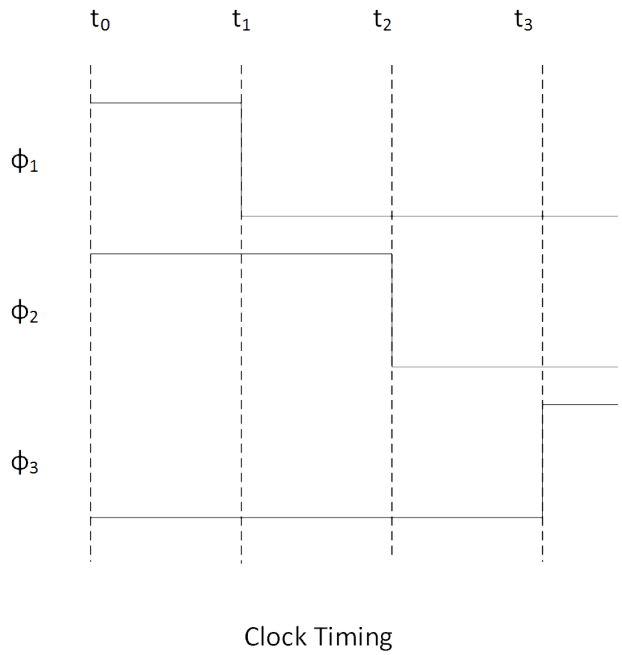


Figure 2.2: Clock Timing for THA from Baker

charge at the input node. The charge stored on sampling and feedback capacitors is shown in Equations 2.1 – 2.2 which simply apply $Q = CV$ to all relevant capacitors in the circuit and assumes ideal amplifier operation. After a half clock cycle, switches ϕ_1 and ϕ_2 open in quick succession readying the amplifier for its holding phase. During the next half clock cycle, ϕ_3 switches close, connecting the stored charge to the output while simultaneously effecting both gain and subtraction via connecting the common mode voltage V_{CM} as indicated in Figure 2.4 and Equations 2.3 – 2.5. At this point, the charge stored on the capacitor starts to decrease due to a leakage path present in all real capacitors. Capturing faster signals requires using smaller capacitors which are more sensitive to discharging, engendering shorter conversion times.

$$Q_{\mathrm{I,F}}{}^{\phi_1} = C_{\mathrm{I}}(v_{\mathrm{in}} - V_{\mathrm{CM}} \pm V_{\mathrm{os}}) + C_{\mathrm{F}}(v_{\mathrm{in}} - V_{\mathrm{CM}} \pm V_{\mathrm{os}}) \tag{2.1}$$

$$Q_{\mathrm{F}}{}^{\phi_3} = C_{\mathrm{F}}(v_{\mathrm{out}} - V_{\mathrm{CM}} \pm V_{\mathrm{os}}) = Q_{\mathrm{F}}{}^{\phi_1} + Q_{\mathrm{I}}{}^{\phi_1} - Q_{\mathrm{I}}{}^{\phi_3} \tag{2.2}$$

$$Q_{\mathrm{I}}{}^{\phi_3} = C_I(v_{\mathrm{CM}} - V_{\mathrm{CM}} \pm V_{\mathrm{os}}) \tag{2.3}$$

$$Q_{\mathrm{F}}{}^{\phi_3} = C_F(v_{\mathrm{out}} - V_{\mathrm{CM}} \pm V_{\mathrm{os}}) \tag{2.4}$$

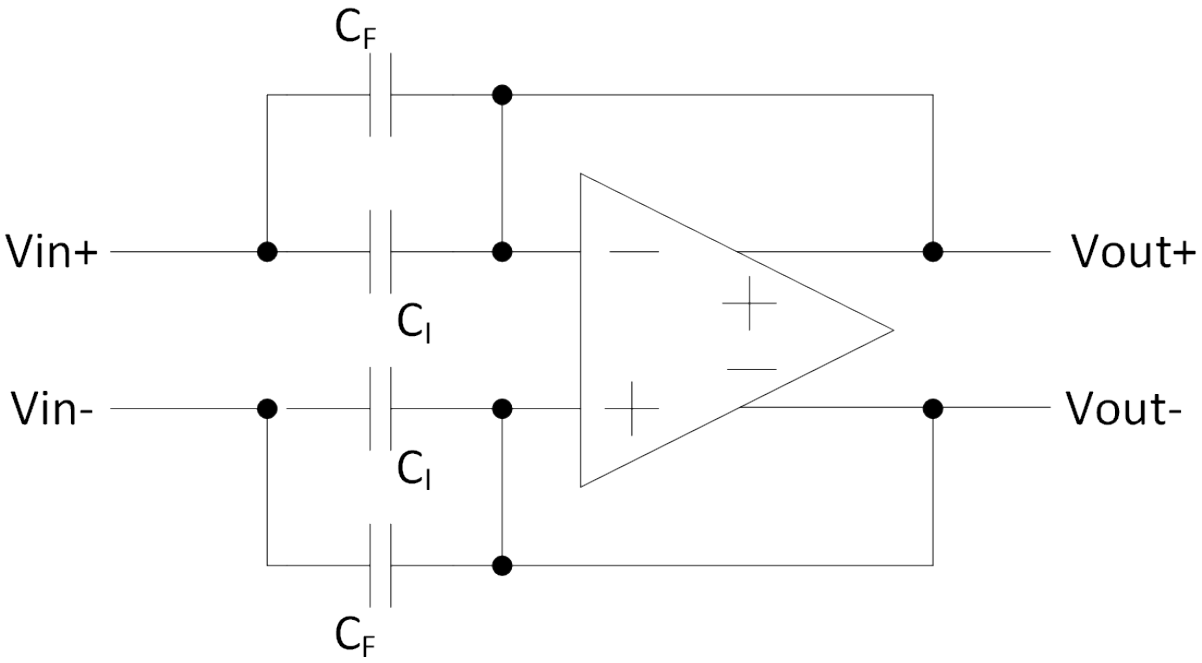


Figure 2.3: THA in Tracking Configuration

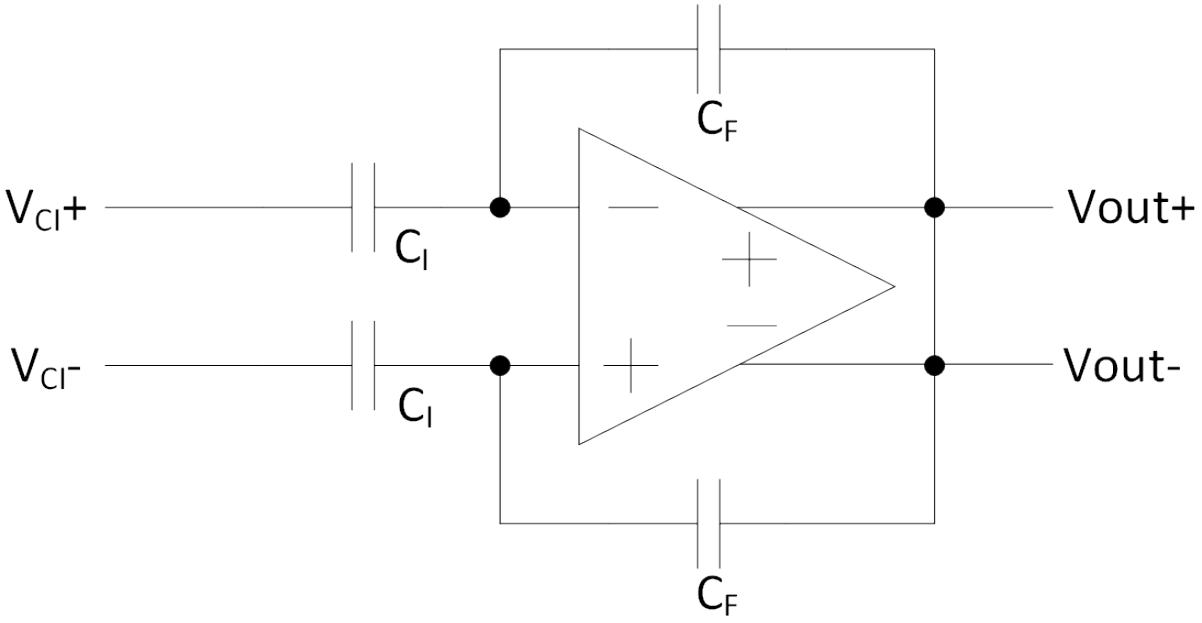


Figure 2.4: THA in Holding Configuration

$$v_{\text{out}} = \left(1 + \frac{C_I}{C_F}\right) v_{\text{in}} - \frac{C_I}{C_F} V_{\text{CM}} \tag{2.5}$$

2.1.2 Quantization

Due to the complexity of mixed signal parts, engineers have devised a number of metrics allowing comparison between different parts. While noting that there are many different digital output representations, the principal operations of most ADCs can be decomposed into two fundamental operations: sampling in time followed by quantizing in value. Before exploring several common architectures in depth, it is worth making some general remarks concerning quantization. The first is that quantization, when done properly, introduces no additional distortion into the signal [2]. Additionally, for a sinusoidal input spanning the full scale range (FSR) of the converter, the ideal signal to noise ratio (SNR) is given by

$$\text{SNR} = 10 \log_{10} \frac{3r^2}{2} \text{ dB} = 1.76 + 6.02N \text{ dB} \tag{2.6}$$

where $r = \frac{2E}{E_0}$, E is the root-mean-square (RMS) input voltage, E_0 is the RMS error voltage, and N is the number of bits of the converter.

As noted in [2], "When there are many steps there is virtually no correlation between errors in successive samples except when there is complete correlation of successive signal values." An intuitive way to see this is to consider a 4-bit system with a reference of 1 V. With 16 discrete output levels starting at 31.25 mV spaced equally apart by 62.5 mV, any value between 343.75 mV and 406.25 mV will be recognized only as its particular code, $6_{10} = 0110_2$. The binary code 0110_2 corresponds to a fraction of the reference voltage: $0110_2 = 6_{10} = \frac{6}{2^4} \cdot V_{REF} = 375$ mV. The difference between the actual analog input value and the equivalent binary code value is termed the *quantization error*. The range of values taken on by the

Table 2.1: Resolution for Ideal Converters

Resolution	SNR [dB]
10	61.96
12	74.00
14	86.04
16	98.08

quantization error is determined by the resolution or number of distinct levels recognized by the converter. Higher resolution outputs then have lower error and less *quantization noise* associated with them. For a ramp signal, the difference between the input and converted output, termed the residue, is a sawtooth wave with uniform amplitude density distributed across a range equal to the step size of the converter. The PDF and variance, respectively, of a uniformly distributed random variable are given by

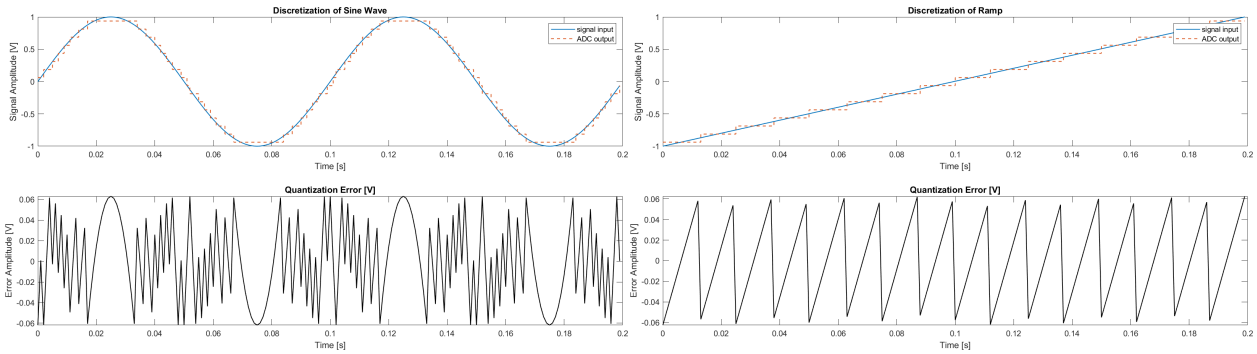
$$\text{PDF} = \begin{cases} \frac{1}{b-a}, & e \in [a, b] \\ 0, & \text{otherwise} \end{cases} \tag{2.7}$$

$$\sigma^2 = \frac{1}{12}(b-a) \tag{2.8}$$

Recognizing that the width $q = b - a$ is equal to the step size for an ideal converter, one arrives at $\sigma^2 = \frac{q}{12}$ where q represents the voltage range of a single decision level. Figures 2.5a and 2.5b show typical error signals for a ramp and sinusoid with a 4-bit, $2^4 = 16$ level converter.

2.2 Architecture Overview

A general-purpose model of an ADC is helpful but certain architecture-specific effects may arise which are not easily captured by generic models. This work focuses on two converters representing some of the most popular general purpose architectures, namely SAR and



(a) Sinusoid (b) Ramp

Figure 2.5: Error Signal for Ideal Quantization

pipeline. Restricting this investigation to these architectures is justified by the fact that a large percentage of converters currently available fall into one of these two categories. According to [3], roughly 30% and 25% of all proposed ADCs from 1997–2019 are pipeline or SAR architecture, respectively, accounting for just over half of all proposed ADCs. An introduction to the theory and implementation of several popular architectures will help inform the subsequent model discussion. Figure 2.6 illustrates the application space of several architectures.

2.2.1 Flash ADC

Flash converters appear as some of the earliest designs [4] but due to their high power consumption, their use is mainly in RF applications where dynamic performance is prized over and above resolution and precision. Flash converters operating in the GHz range often have resolution anywhere from 6 to 8 bits and are inherently parallel, performing all comparisons at once using $2^N - 1$ comparators to produce N bits for 2^N distinct output codes as shown in Figure 2.7. The raw digital output format is thermometer code where the number of 1s is an indication of the code value (e.g. $3 = 0000111$ for a 3 bit converter). To obtain a conventional binary representation (signed magnitude, 1s complement, 2s complement,

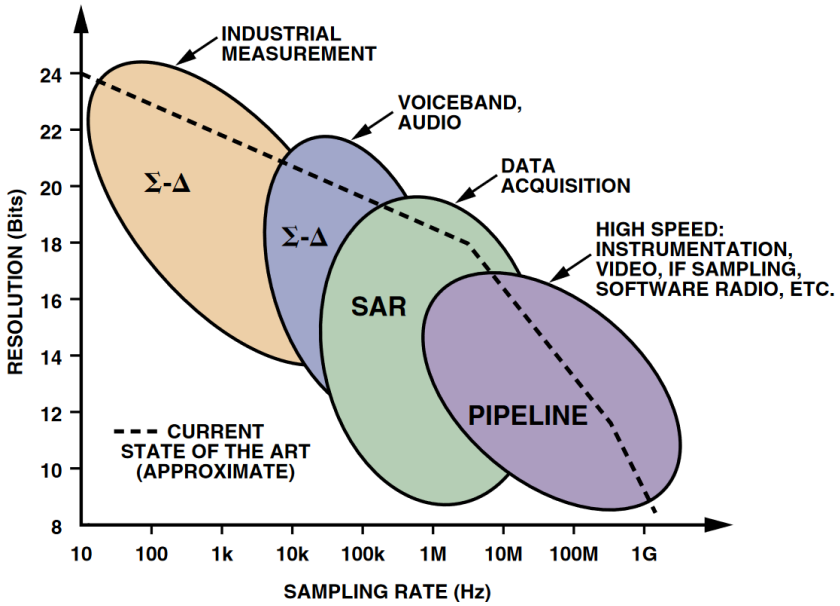


Figure 2.6: Comparison of Typical Architecture Performance Spaces from Kester

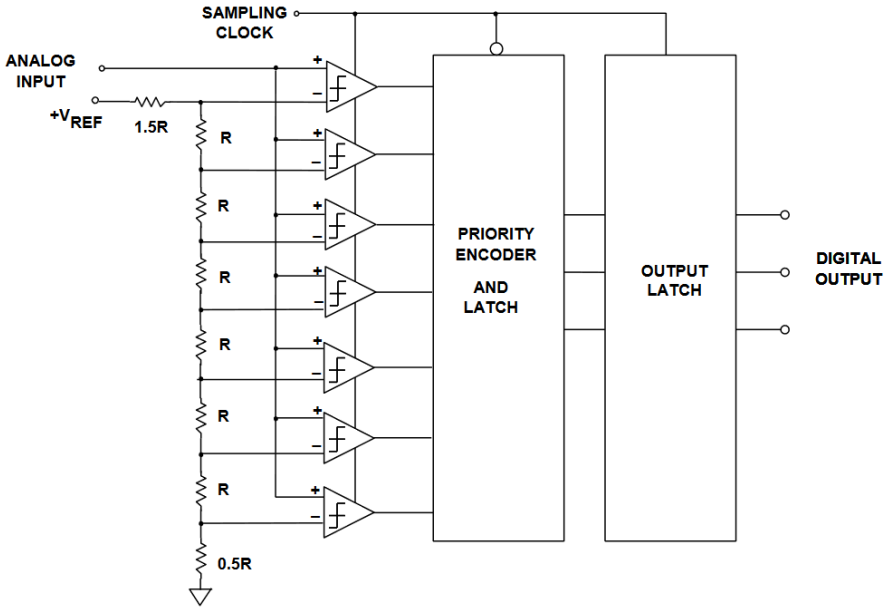


Figure 2.7: Standard Resistor String Flash ADC from Kester

Gray code, etc.), all designs feature an internal decoder which converts thermometer to binary representation. The most popular realizations are capacitive charge redistribution and resistor string voltage division.

2.2.2 Successive Approximation Register ADC

The successive approximation register (SAR) architecture is conceptually very simple and able to be implemented with relatively few analog blocks, mainly a THA, comparator, and digital to analog converter (DAC), with digital support in the form of control logic, registers, and output latches. DAC approaches vary but two popular architectures include resistive string voltage division and capacitive charge redistribution. The latter offers the advantage of being a switched-capacitor network which integrates seamlessly into a mixed-signal paradigm.

The first step to convert an input is to track the input for half a clock period before holding the last value, all done using the THA block. In some instances, the THA is not a separate block but may in fact use the capacitive DAC with switched-capacitor techniques to perform the sampling. Following acquisition of a voltage signal, a higher-frequency clock is used to control the internal decision logic. This faster clock may be internally generated

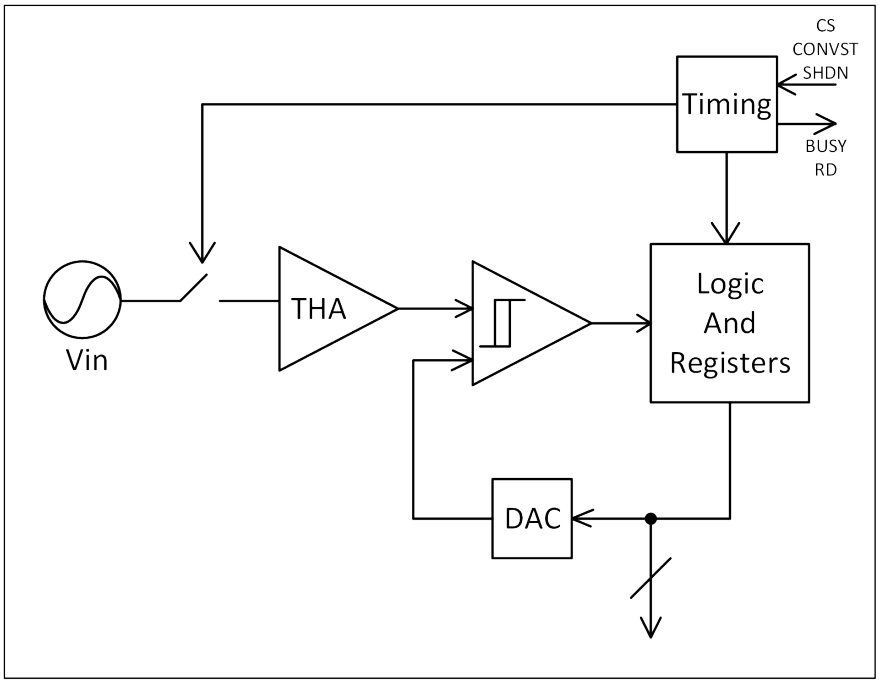


Figure 2.8: Typical SAR Block Diagram

Data: ±VREF, VINp, VINn
Result: Binary Representation of Input
while not finished **do**
  foreach n_i in N **do**
    Apply '1' to bit n_i
    if Comparator == 0 (Input > DAC) **then**
      Set n_i to '1'
      Latch '1' to output
    else
      Set n_i to '0'
      Latch '0' to output
    end
  end
end

Algorithm 1: SAR ADC Algorithm

or formed from the externally supplied sampling clock. Algorithm 1 shows the basic steps of SAR conversion: for each bit decision, the comparator output is checked. If high, then the current DAC output as decided by the control logic is insufficient to balance the input so the current bit is left high and the next lowest bit is tried. If low, then the current DAC output as decided by the control logic is larger than necessary to balance the input so the current bit is set low and the next lowest bit is tried. This process continues until all N bits have been tried.

2.2.3 Pipeline ADC

The pipeline architecture is characterized by high throughput, latency due to the use of internal substages, and generally favorable trade-offs between speed and number of bits. The pipeline is an extension of the two-step flash converter whereby successive stages convert the error between the input signal and a low-resolution approximation. Gain is applied to this error term or residue and then another approximation is formed. The key points concerning the pipeline, whose block diagram is shown in Figure 2.9, are the following: (1) once all pipeline stages are operating, throughput is very high; (2) the most sensitive stages are the early ones as any error in these stages compounds over subsequent stages; and (3) due to the sensitivity of the front end, successive stages usually incorporate some form of redundancy to tolerate errors. In practice, digital redundancy is necessary to tolerate unavoidable errors in component matching, interstage amplifier gains, offset errors in substage flash converters, and distortion in substage multiplying digital to analog converter (MDAC). This means that digital recombination of each stage's output must be performed before forming the final binary representation. For the models presented later, this bit recombination process is assumed ideal.

Each pipeline stage except for the last operates according to a similar design. Firstly, the input is sampled and held by a THA. For the first stage, the THA is a separate block whereas for later stages, this functionality is performed by the previous stage's MDAC. The ith coarse flash stage-ADC (sADC) forms an n_i-bit representation of the input which is used to actuate switches connecting binary weighted capacitors onto the other side of a differential amplifier, performing subtraction on the input. Next, charge redistribution

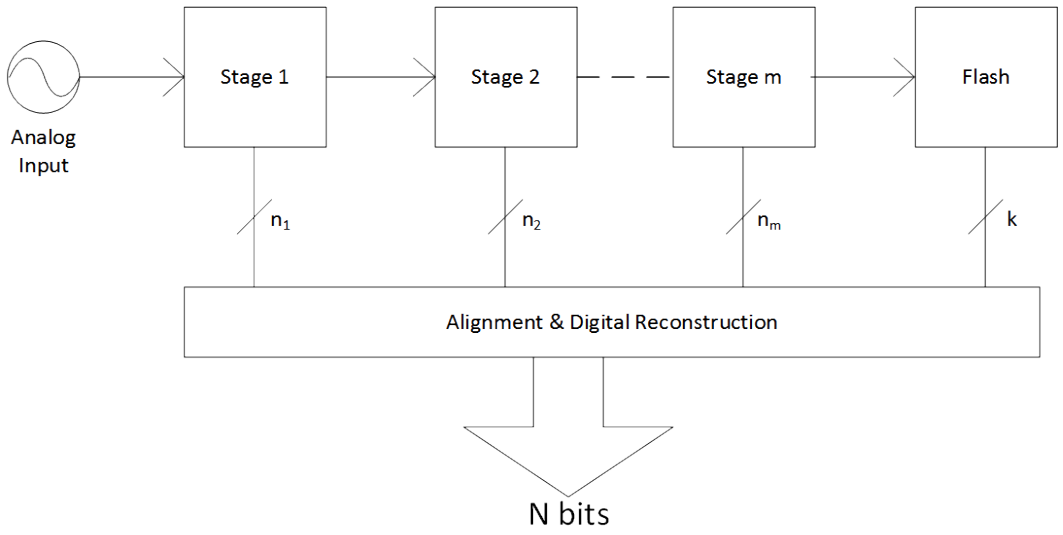


Figure 2.9: Block Diagram of Pipeline ADC

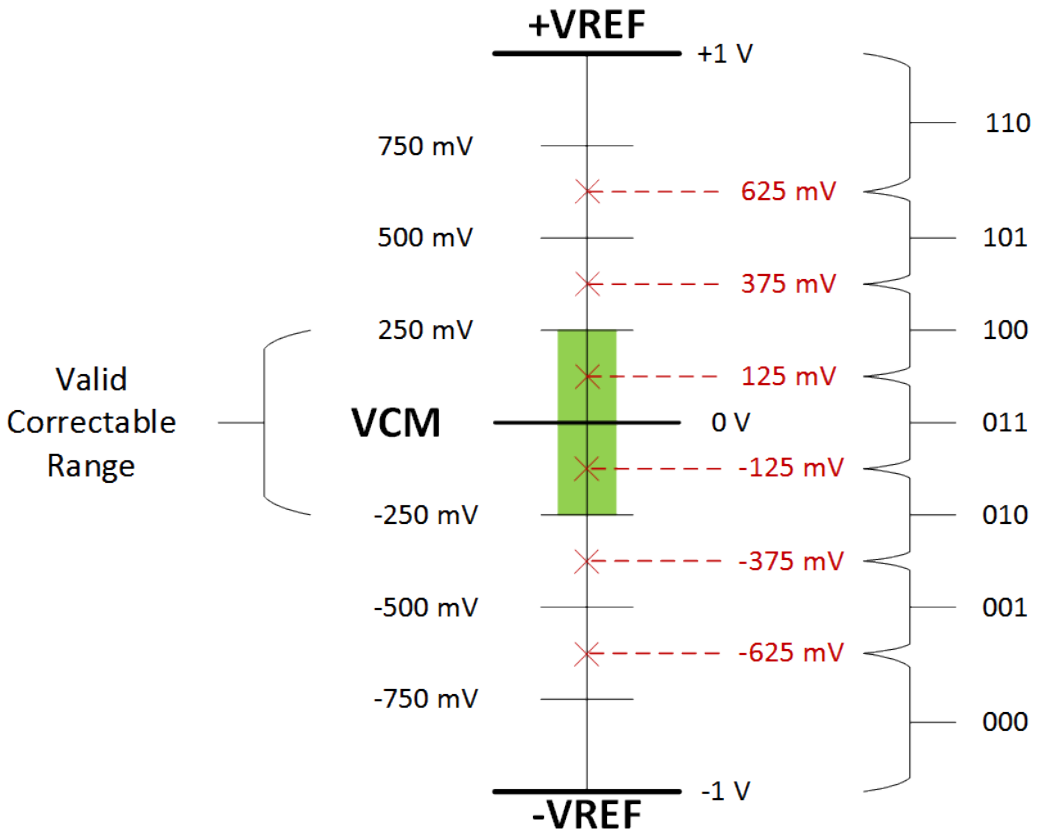


Figure 2.10: Decision Levels for Stage ADC (sADC)

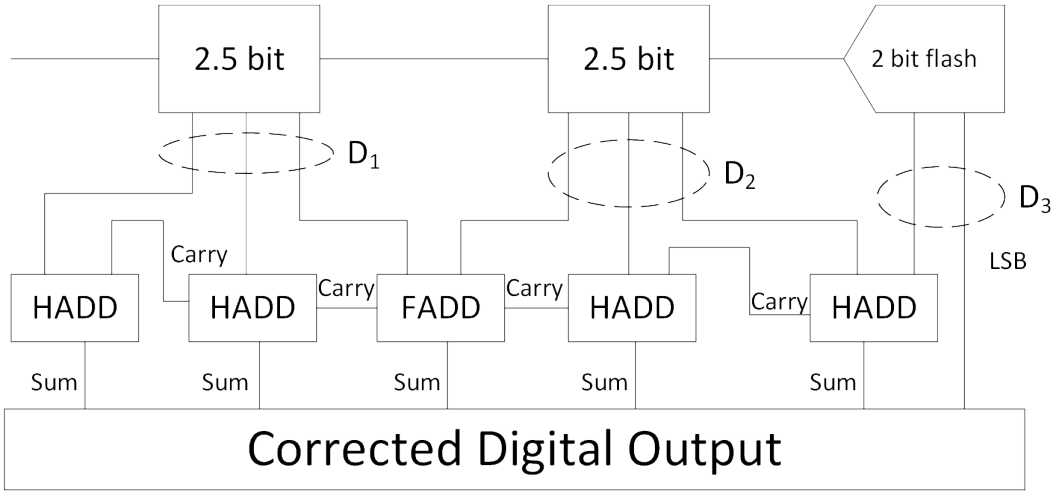


Figure 2.11: Digital Implementation of Redundant Signed Digit

action of a capacitor network around the amplifier adds gain to the resulting stage residue before being passed onto the next stage where this basic procedure is repeated. Because of extra voltage headroom due to the so-called digital redundancy, there is an extra bit from the flash stage at the MSB position. This extra bit is not used when determining the actual code value but must be recombined in order to account for overrange and underrange in the code values internal to the converter.

As shown in Figure 2.10, there is a valid range within which any error can be corrected as well as a set of decision levels used to ensure the residue with gain falls within $\pm V_{REF}$ V. Because each substage (excepting the last flash stage) is afforded one extra bit of redundancy, only half the entire range is normally used. The sADC outputs a binary code which must be decoded in order to select the proper switches to produce the correct residue. This is done as part of the MDAC structure which also performs subtraction, gain, and THA functionality for the subsequent stage. Once the sADC digital output is known, the set of bit outputs from each stage must be recombined to form a single code corresponding to the pipeline ADC's measured output. It is worth explaining the redundant signed bit algorithm used in many pipeline architectures, an algorithm whose basic idea is shown in Algorithm 2 and block-based implementation in Figure 2.11. It is first assumed that the final flash stage incorporates no error correction and its raw digital output is used. The result of this final

stage is shifted such that its MSB overlaps with the LSB of the previous stage and a half-adder (HADD) used to perform the bit-wise add and carry. A half adder again combines the incoming carry bit with the stage bit. This sequence continues until all bits are recombined starting from the ADC's overall LSB and propagating backwards to its overall MSB. Logic circuits necessary for implementing digital recombination include bit storage units (flip-flops or latches), half adders, and full adders. Due to the design of the substages, the all-ones code $11\ldots1_2$ from a substage is never reached, instead the maximum binary output from a substage is $11\ldots10_2$.

2.2.4 Noise Shaping ADC

Noise shaping converters occupy an application space where resolution is of paramount importance and sampling rate is a secondary concern. This architecture generally performs some type of low-resolution conversion while oversampling followed by digital filtering to produce a high-resolution representation of the input signal. The basic process is shown in Figure 2.13 where a comparator is used to produce a 1-bit representation of the input. A feedback loop with an integrator as the loop filter implements noise shaping. Noise shaping in this context means that the feedback action acts mainly on the low-frequency portion of the input, i.e. high-frequency content tends to be noisier. This is what is meant by "pushing up" the noise into a higher frequency range. The increased noise PSD at higher frequencies is removed by digital filtering which produces a high-resolution digital output at moderate speeds. This architecture is especially popular for audio recording which operates at 24 bits and 96 kHz. There are two important characteristics, the STF (signal transfer function) and NTF (noise transfer function) which can be derived from Figure 2.13, resulting in Equation 2.10 – 2.11. $\mathcal{Z}$-transform equations are given as follows:

$$(X_i - Y_i)H(z) + E_i = Y_i \tag{2.9}$$

$$\text{STF} = \frac{Y_i}{X_i} = \frac{H(z)}{1 + H(z)} = 1 \tag{2.10}$$

$$\text{NTF} = \frac{Y_i}{E_i} = \frac{1}{1 + H(z)} = 1 - z^{-1} \tag{2.11}$$

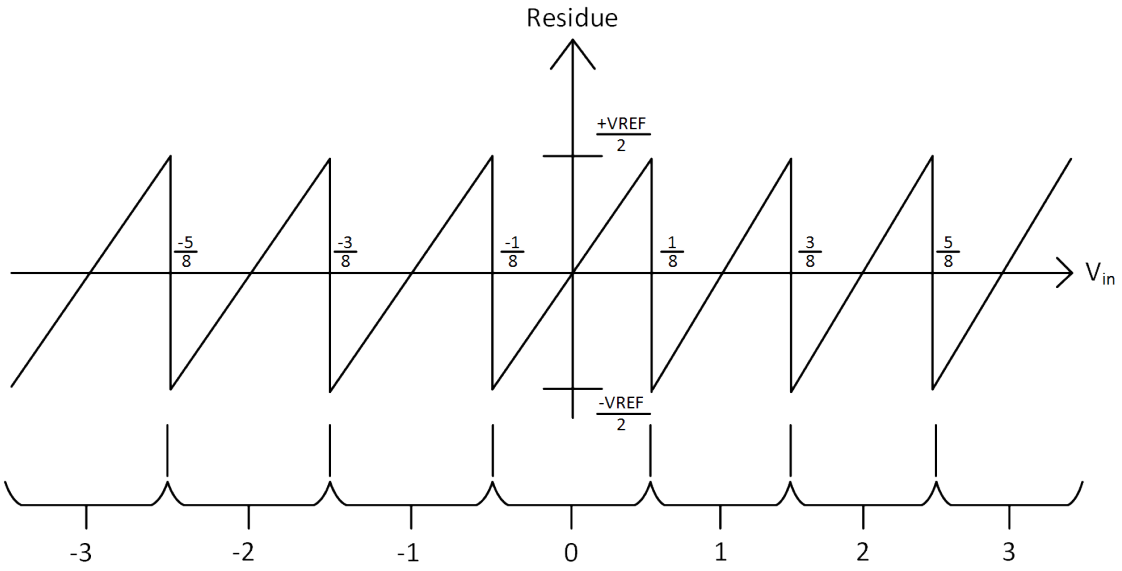


Figure 2.12: 2.5 Bit Residue Transfer Curve

Data: ±VREF, VINp, VINn
Result: Residue Voltage
while not finished **do**
  foreach Stage in ADC **do**
    Diff_{in} = VINp - VINn
    subADC = FLASH(Diff_{in})
    subDAC = DAC(subADC)
    residue = Diff_{in} - subDAC
  end
end

Algorithm 2: Pipeline Stage Algorithm

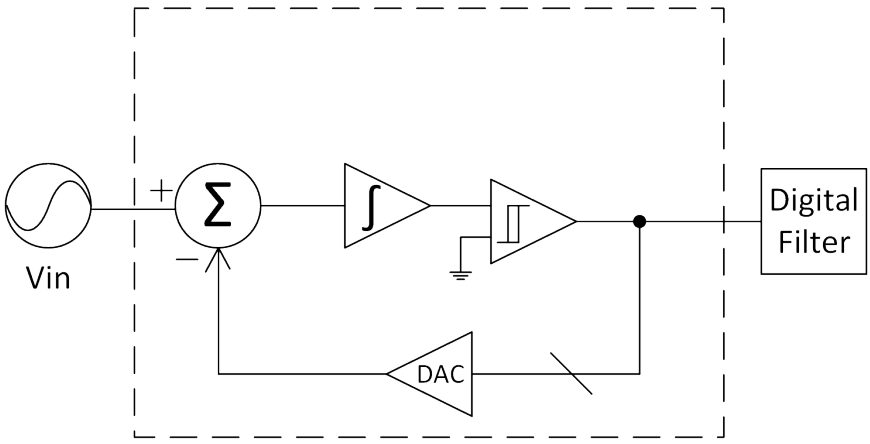


Figure 2.13: Σ-Δ Converter Block Diagram

Table 2.2: Modeling Approach Comparison

Approach	**Speed**	**Accuracy**	**Effort needed**
Transistor	Low	High	High
Macromodel	Medium	Medium	Medium
Behavioral	High	Low	Medium

2.2.5 Model Approach Survey

There is a popular phrase from renown statistician George Box stating "Essentially, all models are wrong, but some are useful" [5]. Correspondingly, there are tradeoffs as shown in Table 2.2 regarding how accurately one wants to model a phenomenon and how many resources one is willing to spend on obtaining results. Following a good overview of ADC modeling approaches found in [6], I decided the most appropriate approach is that of the generic behavioral model. The merits and drawbacks of each approach are briefly detailed below.

Transistor Based Models

Transistor based models use a nonlinear solver to iteratively simulate node voltages and currents via KVL and KCL for electrical devices defined by specifications like SPICE models. This process requires schematic information which is usually hidden behind vendor intellectual property (IP) and process information relating to specific transistor parameters like threshold voltages, geometry information, and other physical parameters. Such transistor

models are typically calibrated for process variation and across a range of *standard* operating temperatures. Because the project investigates testing complex COTS parts, no schematic information is available, and the devices operate well outside of established design margins, requiring cold-specific models to handle effects such as carrier freeze-out and changes in device performance. Such cold-specific transistor models are, apart from [7, 8], not available. The time investment needed to develop a calibrated model for a complex mixed-signal device is quite extensive, and does not provide a methodology which saves testing time.

Indeed, the time investment in developing compact cryogenic transistor models as delineated in the above references is non-trivial. The overall approach is to first compute the electrostatics of charge carriers obeying Boltzmann statistics. This can be done by starting with Poisson's equation

$$\nabla^2\phi = -\frac{q}{\epsilon}(p - n + D) \tag{2.12}$$

along with time-varying charge carrier dynamics

$$\frac{\partial n}{\partial t} = \nabla \cdot (-n\mu_n \nabla\phi + \mu_n V_{th} \nabla n) + GR_n \tag{2.13}$$

$$\frac{\partial p}{\partial t} = \nabla \cdot (p\mu_p \nabla\phi + \mu_p V_{th} \nabla p) + GR_p \tag{2.14}$$

Additionally, the changes in activation energy and bandgap energy must be taken into account as these affect the number of free carriers available for transport. As a final note, though not pursued here, it is possible to incorporate a range of reliability concerns as demonstrated for radiation in [9] using a hierarchical VHDL-AMS simulation.

Macromodels

In contrast to transistor-level models, macromodels utilize functional subcircuit blocks consisting of electrical elements to incorporate realistic effects of devices. This approach has worked well for all-analog devices like op-amps and comparators [10, 11, 12] but must be modified to include mixed-signal systems. A common approach shown in Figure 2.14 is the so-called Boyle macromodel which uses transistors to model the input pair along with cascaded blocks implementing the frequency response and output stages. Such an approach

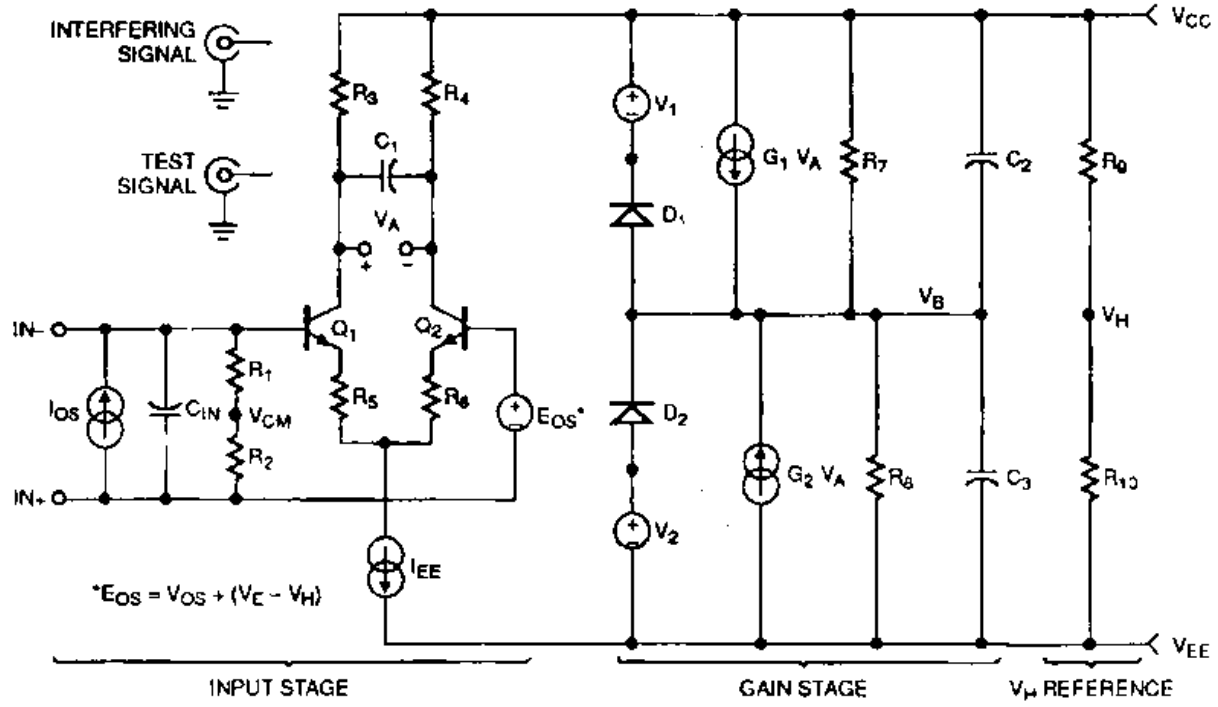


Figure 2.14: Boyle Macromodel

works well for amplifiers and can be configured using existing SPICE-like simulators. The approach may have difficulty modeling mixed-signal systems where actions are often performed in discrete time steps. In particular, to model a mixed-signal system using the macromodel approach, one must take into account the input-output behavior of digital pins through the use of IBIS models. While most IBIS simulators are closed source, the approach as a whole is architecture-specific. Different models must be developed for each type of ADC, each with a particular circuit topology, and it is difficult to populate or reverse-engineer salient parameters using only input-output information from COTS testing. Therefore, the macromodel approach was deemed insufficient in terms of capturing universal performance trends across different ADC architectures. A circuit based macro-model for pipeline ADCs is demonstrated in [13] where library blocks of amplifiers, comparators, and others are used to synthesize individual pipeline stages, but again, such an approach is specific to one architecture.

Behavioral Models

While the above approaches incorporate some topology or structural information into the resulting model, sometimes such information is unavailable. When only input-output data is available for consideration, the result is a situation for which behavioral models are ideally suited. There are a few approaches here as well, including system identification [14], Volterra series [15], polynomial transfer function [16], and integral nonlinearity (INL) curve characterization [6]. Some of these approaches are specific to ADCs while others are borrowed from control systems theory and may be applied to any process which produces an output for a given input. In the end, I chose the INL curve characterization approach because its construction relies upon well-documented test methods [17], it is widely applicable to any converter, and it is applicable to conceptually breaking up the analog front-end and digital back-end processing.

2.3 ADC Testing

ADC testing involves obtaining specifications related to supply current, the impact of the converter on inputs, and the accuracy of the converter itself. A good overview of ADC testing can be found in [18] but there are broadly three categories of testing: (1) measuring the effect of a converter on an input; (2) characterizing the converter's decision process; and (3) testing the functionality of the converter via DC operating point. As I was limited by the setup to standard input-output tests, I decided to adopt something measurable to quantify performance as well as something descriptive that could be used to build the model. Towards this end, I utilized both the standard sine-wave testing for parameters such as SNR, total harmonic distortion (THD), signal to noise and distortion (SINAD), spurious-free dynamic range (SFDR), etc. while also building the transfer curve via histogram tests using both sine and ramp signals. The two sets of tests provided information for the model blocks which could be applied regardless of converter topology. A brief discussion of test methodology follows.

2.3.1 Dynamic Sine Testing

Sine wave testing exercises the converter by applying a standard sine test signal. Such signals are useful not only for their theoretical importance but also because test equipment typically has very good performance regarding such signals. To improve performance, one can always insert a low-pass filter (LPF) at the front of the circuit under test.

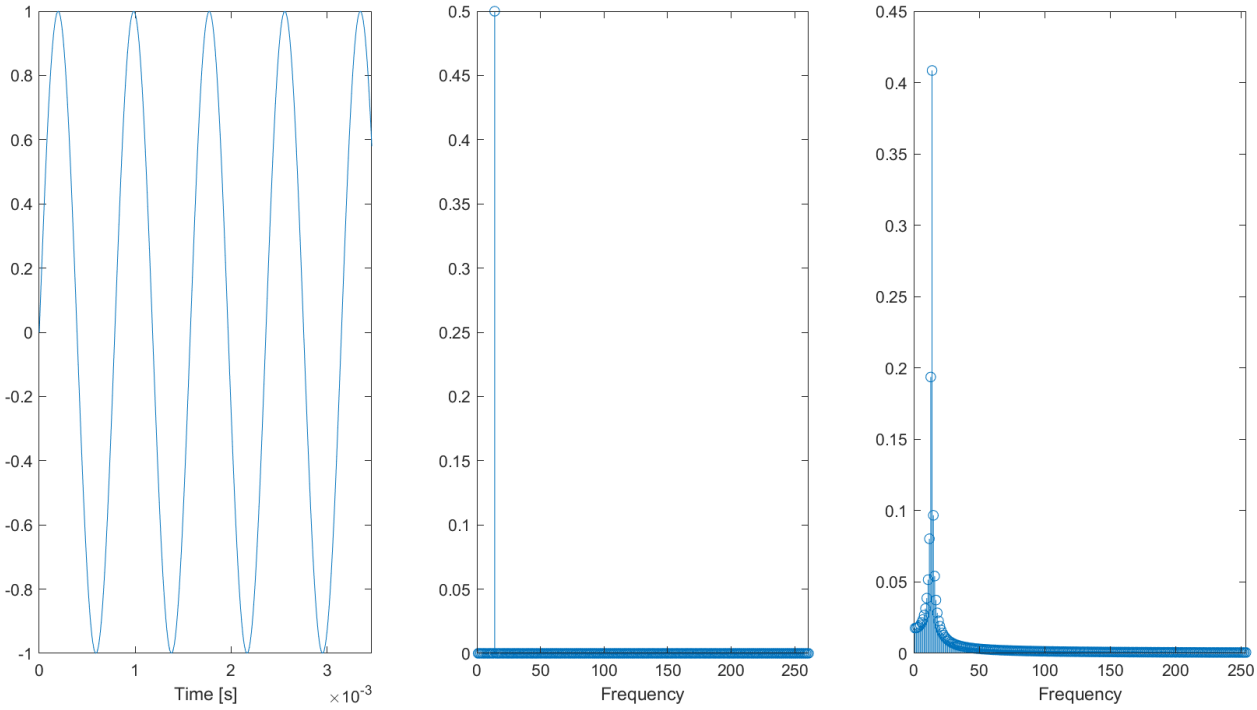


Figure 2.15: Sampling with and without Leakage

Frequency Domain Testing

Many of the parameters of interest can be found in the frequency domain by taking a fast Fourier transform (FFT) of the output data. However, care must be taken with respect to coherence, the relationship between input and sample frequencies. When a periodic waveform is sampled at an integer multiple of its fundamental period, there is redundancy in the data collected which produces a misleading picture of the device under test (DUT). To avoid this, one must ensure that the input and sample frequencies are relative primes, that is that they contain no common divisors.

Table 2.3: Table of Various Fourier Transforms

	Continuous Time	Discrete Time
Periodic	Continuous Time Fourier Series	Discrete Time Fourier Series
Aperiodic	Fourier Transform	Discrete Time Fourier Transform

The other point is more subtle and relates to Fourier sampling theory. Periodic continuous-time (CT) signals can be expressed via an infinite series of complex exponential terms, the Fourier Series. An aperiodic CT signal can be expressed via a continuum of complex exponential terms, the Fourier Transform. For discrete-time (DT) signals, their frequency domain representations are periodic and either a continuum (DFT) or a finite, discrete set (DTFT). The types of transform according to periodic/aperiodic and discrete/continuous are shown in Table 2.3. The underlying assumption behind the DTFT is that the data it operates on is one period of a larger periodic signal [19]. This assumption is often violated in practice whenever signal endpoints display a discontinuity upon successive "cycles". From a frequency domain standpoint, there are additional terms present and what should be a single tone is smeared across multiple frequencies resulting in an imprecise measurement as seen in Figure 2.15. The standard prescription for such cases is to use a window function to smoothly taper the endpoints of the signal ensuring localization in frequency coefficients, a procedure that is equivalent to convolving the original input's frequency response with the frequency response of the window. To ensure coherence, a useful relation between sample period, input period, and total number of points is shown in Equation 2.15 where N_{cyc} and N_{pts} are relative primes, i.e. neither has a common divisor. This ensures that the input is not repetitively sampled and most if not all output codes are obtained.

$$\frac{F_{in}}{F_s} = \frac{N_{cyc}}{N_{pts}} \tag{2.15}$$

Using a window has ancillary effects including lowering signal power, changing the amplitude, and possibly generating interference between nearby frequency peaks [20].

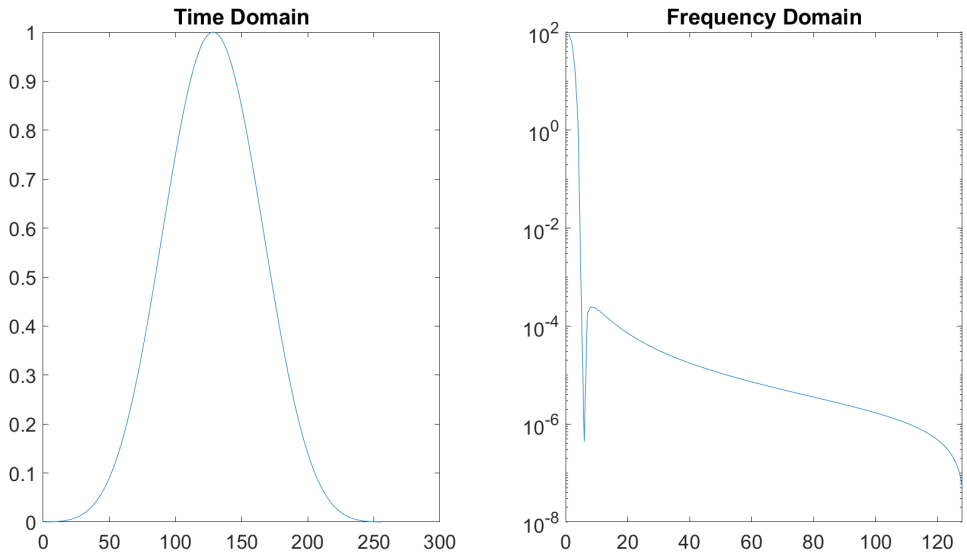


Figure 2.16: Blackman-Harris Window in Time and Frequency Domains

Time Domain Testing

Time domain testing serves mainly as a complement to frequency domain testing, a sanity check of results. Frequency domain data can be misleading so having a safeguard against unwarranted conclusions is helpful. Signal to noise and distortion (SINAD) is most naturally found in the time domain by first finding the best-fit sinusoid, then comparing the power in the residue (NAD) with that of the best-fit sinusoid. The log ratio of these quantities yields SINAD and in practice, agrees quite well with frequency data:

$$\text{SINAD [dB]} = 10 \log_{10} \left(\frac{P_{sig}}{\text{NAD}} \right) \tag{2.16}$$

2.4 Histogram Testing

Another area where time domain testing has a role is in computing the ADC's transfer curve by obtaining the INL/DNL curves. These curves can be obtained in numerous ways but I used the histogram test. The basic idea is that under non-ideal circumstances, all code bins will have unequal width with wider bins having more counts than narrower bins. Comparing the experimental histogram to the ideal histogram gives a statistical estimate of the width

of each bin or the converter's DNL. By integrating or summing the result, one arrives at the INL curve.

2.4.1 Sine Histogram

For a sinusoidal input, the ideal probability density function (PDF) is given by Equation 2.17. It is also necessary to overdrive the converter slightly to obtain an estimate of all transition locations. The basic idea is to assume a Gaussian distribution of errors about the true decision level and to maintain a $\pm 3\sigma$ band below $\pm 1/2$ LSB for each decision level. This is especially true for measurements taken near the peaks of the input where the converter error is largest. Another aspect to consider is generating enough samples to be statistically confident in the results. Assuming errors in estimating the true converter decision level are Gaussian distributed, it can be shown [21] that the number of points to obtain a given precision is given by Equation 2.18 where $Z_{\alpha/2} = 2.575$ for 99% confidence and $\beta = 0.1$ for DNL accuracy. Unfortunately, the number of points needed to obtain a given precision increases exponentially with the converter resolution so a 12-bit device needs $1,070,678$ points while a 14-bit device needs $4,282,712$ points.

$$\text{PDF} = \frac{1}{\pi\sqrt{1-(\frac{x}{A})^2}} \tag{2.17}$$

$$N_{pts} = \pi 2^{N-1}\frac{(Z_{\alpha/2})^2}{\beta^2} \tag{2.18}$$

2.4.2 Ramp Histogram

Compared to sinusoids, ramp signals are much simpler from a probability perspective as they possesses a uniform PDF. For ADC testing, this range is distributed evenly across each permissible output code and makes computing the DNL and INL much easier. In reality, some bins are wider than others and this fact allows one to estimate the DNL of the converter. To compute DNL using a ramp input, one excludes bins containing overranges (first and last codes) and normalizes each bin count by the mean bin count, then subtracts 1 from the normalized counts, directly giving the DNL.

2.4.3 Summary of Literature Reviewed

Regarding cryogenic testing of COTS for reliability, there are not many references since such an effort is rarely attempted. However, authors in [22] performed lifetime testing of a COTS ADC in cryogenic temperatures while looking for signs of degradation. Specifically, the AD7274, a 350 nm COTS ADC, was driven with a DC voltage under slight voltage stress of 5.5 V while INL and DNL were periodically taken under nominal voltage conditions all while the device operated at cryogenic temperatures. The authors found that after 800 hrs, no significant change in INL or DNL was observed. Monitoring the supply current revealed a 1.5% degradation, however. Of the two likely effects, voltage stress and hot carrier effects (HCE), only voltage stress contributed to any observed change. Another HCE study for 180 nm complementary metal oxide semiconductor (CMOS) devices with access to I_{sub} and other device parameters was performed for an ASIC in [23]. There, the main concern was impact ionization leading to interface traps which lower device performance due to a combination of lower transconductance, lower output resistance, and higher threshold voltage. Because this test had so many differences in measurement capability, its methodologies and results were of little use to the investigation presented in this thesis.

2.5 Summary

This chapter presents an overview of quantization and sampling theory, two aspects of ADC design and testing one must be familiar with. Additionally, a model survey was presented briefly detailing the design behind the most common architectures. In particular, the flash, SAR, pipeline, and sigma-delta ($\Sigma\Delta$) were described. Although several ADC architectures were reviewed, testing and modeling focused on pipeline and SAR devices due to their prevalence among silicon CMOS ADCs.

Next, a description of common ADC tests and their implementation was given. Such tests were used to characterize the performance and functionality of devices tested in order to extract temperature-dependent trends. Finally, a literature review concerning approaches and similar work was given.

Chapter 3

Architecture Agnostic Behavioral ADC Model

3.1 Overview

The simplest way to understand a converter is to recognize that it simply bins values according to transition locations. The location of code decision points, termed the transfer curve of an ADC, reflects an abstract understanding of data converters. In theory, if one could characterize a converter's transition locations subject to various parameters like input value, past values, temperature, etc. it would be possible to substitute this binning function for the converter itself. This approach is explored in Chapter 4. However, other effects impacting converter performance can be considered separately and their effects added together as part of a single model, an approach which is discussed below under the heading of a 'generic block description'.

3.2 Generic Block Description

Initially, I considered developing a block-based description of the converter which could be built from either a datasheet or measured input-output data as shown in Figure 3.1. As part of this approach, I recognized that several non-ideal effects would need to be incorporated to produce something approximating the observed performance of the ADC

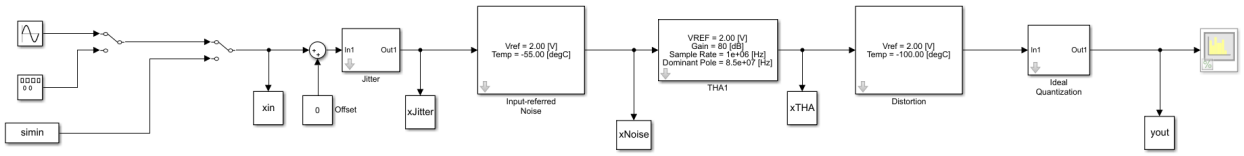


Figure 3.1: Generic Block Diagram of Converter

in question [24]. Ideally, one would be able to draw direct connections between the converter architecture and overall error sources but this was not possible for COTS components whose internals were unknown. Thus, mathematical modifications to the input in accordance with observed performance were used. The main considerations are explored below along with their implementations in Simulink.

3.2.1 Reference Voltage

ADCs compute a binary fractional representation of the input voltage with respect to a (hopefully) fixed reference. Initially, the impact of the reference voltage on part performance was unknown and assumed to be significant since the reference voltage is the benchmark against which all input voltages are compared. As simulation revealed, a noisy reference in fact directly injects noise onto the conversion process resulting in highly degraded SNR as shown in Figure 3.2. This can be seen by looking at ideal quantization shown in Equation 3.1 where x is the input voltage, q is the LSB voltage, k is the output code, and n is the RMS noise voltage.

$$k = \left\lfloor \frac{x}{(1+n)q} \right\rfloor \tag{3.1}$$

Initial testing of the AD9225 pipeline converter bore this out as initial results indicated worse noise performance than expected; it was later discovered that the common-mode level pin on the DUT had not been bypassed properly and once the appropriate filtering had been applied, the device achieved performance comparable to datasheet specified performance. This indicates the degree to which noise can affect the performance of a converter. There are two main types of variation which can affect the reference voltage, namely deviation of its value with respect to temperature, sometimes termed drift, and the coupling of unwanted noise onto the reference node. Impacts of reference drift on converter resolution are less

significant than noise as shown in Figure 3.3. Such SNR variation with voltage level can be explained by noting that for a larger reference voltage relative to the same input signal level, the signal power relative to quantization noise is correspondingly decreased. Put another way, if the reference voltage were to drop while the noise level remained constant, the number of codes affected by noise would increase. Concerning the effects of a noisy reference while again assuming ideal quantization, direct coupling of noise onto the reference voltage produces noise directly in series with the output. This effect is shown in Figure 3.2 where an RMS noise voltage level of 0.1 LSB causes a converter to lose 0.5 bits of resolution.

For precisely such reasons related to noise and voltage level, most commercial ADCs are equipped with a temperature-compensated CMOS-based bandgap voltage reference followed by an amplifier to buffer, filter, and possibly perform single-ended (SE) to double-ended (DE) conversion [25]. Figures 3.4a and 3.4b show block-diagram representations of amplifiers used in the parts that were tested. For functionality to be maintained, both the bandgap generator circuit and buffering amplifier must be operational. Unfortunately, there is no *a priori* way to ensure functionality of these critical blocks and even for parts which permit external references to be supplied, there is no guarantee that internal amplifiers will present the externally supplied voltage to the converter. Indeed, prior investigations of the LTC1419 in [26, 27] revealed that while the converter was tolerant of single-event upsets (SEU), the converter's ability to "see" its reference voltage, even when supplied externally, appeared to fail past -60 °C, falling from $+2.5$ V to $+1.25$ V. This unexpected behavior at low temperatures was confirmed experimentally during testing at UT as shown in Figure 3.5.

Based on the provided block diagram in Figure 3.4b, it was speculated that it might be possible to drive the output of the reference buffer directly using the REFCOMP pin. Doing so would restore the reference voltage level to a nominal $+2.5$ V and improve SNR by mitigating degradation due to collapse of the reference voltage, an effect which can be estimated according to Equation 3.2 with a resulting SNR degradation estimated in Equation 3.3. The approximations proved accurate as evidenced by Figure 3.6 where about 12 dB of SNR degradation was observed, leading to an effective resolution of 8.35 bits. After routing an external reference directly to the buffer amplifier's output of the LTC1419, performance

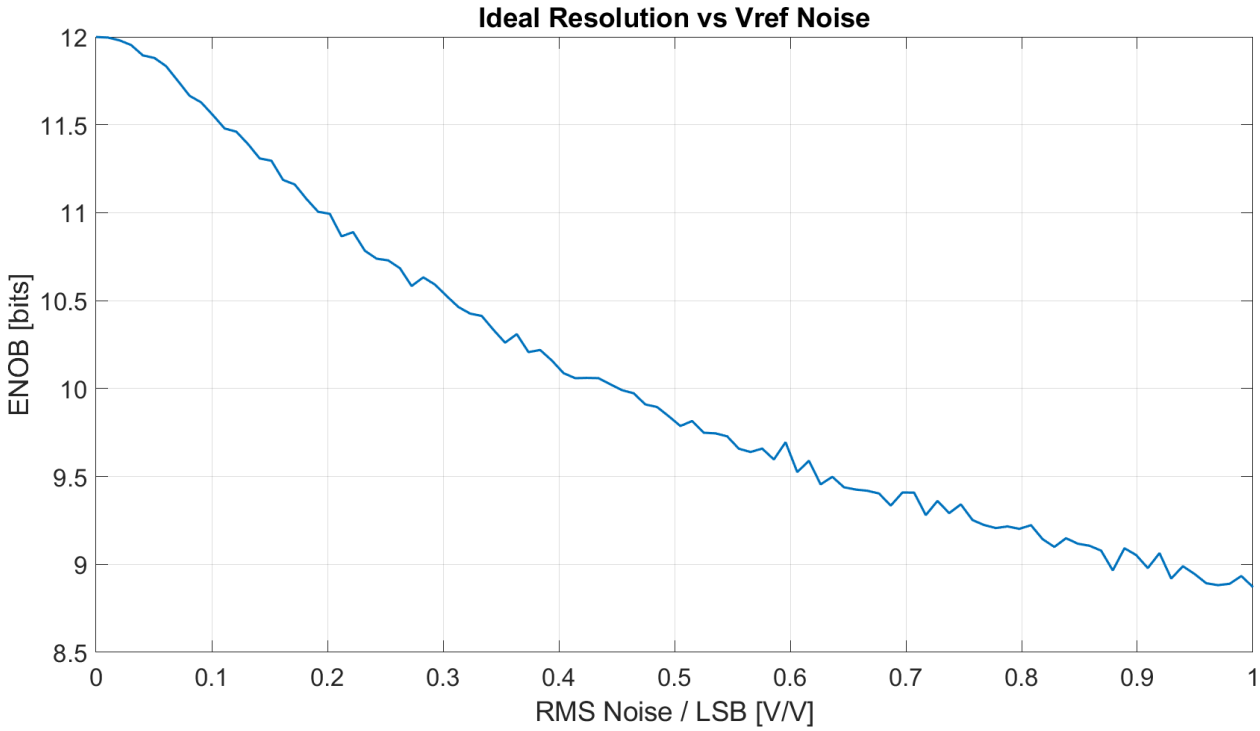


Figure 3.2: Ideal ADC Resolution vs Reference Noise

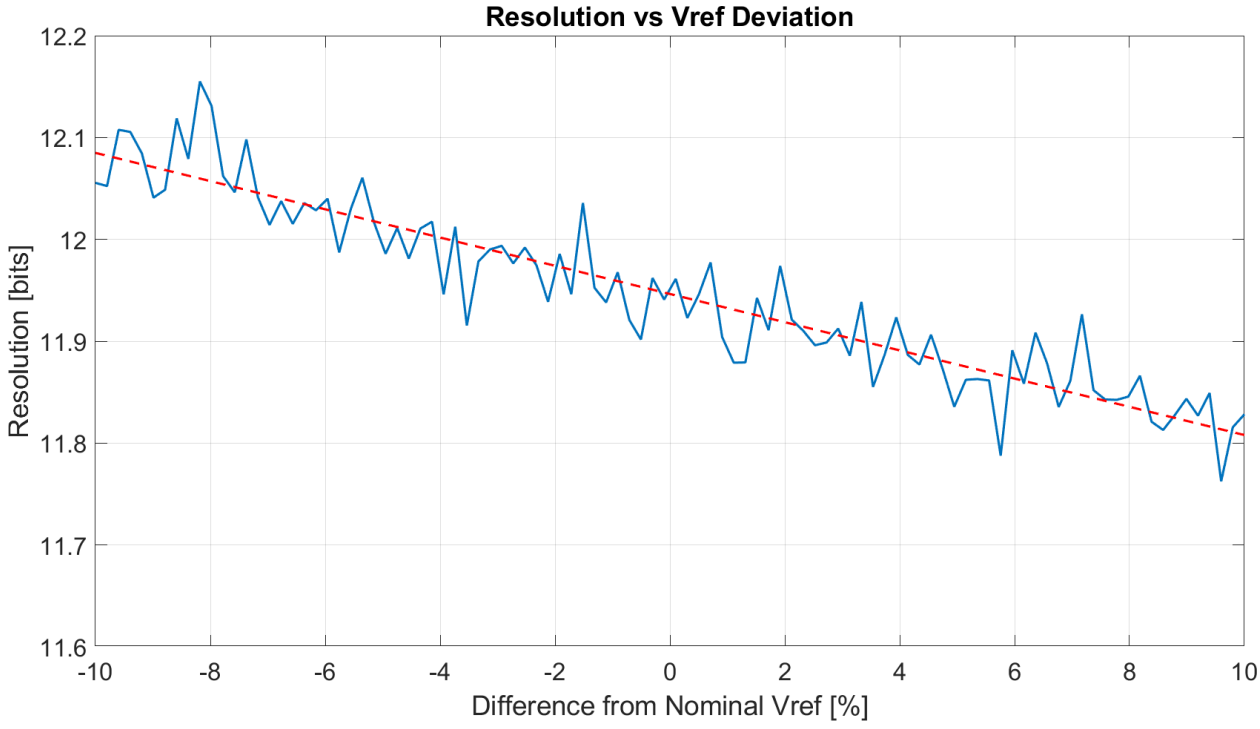
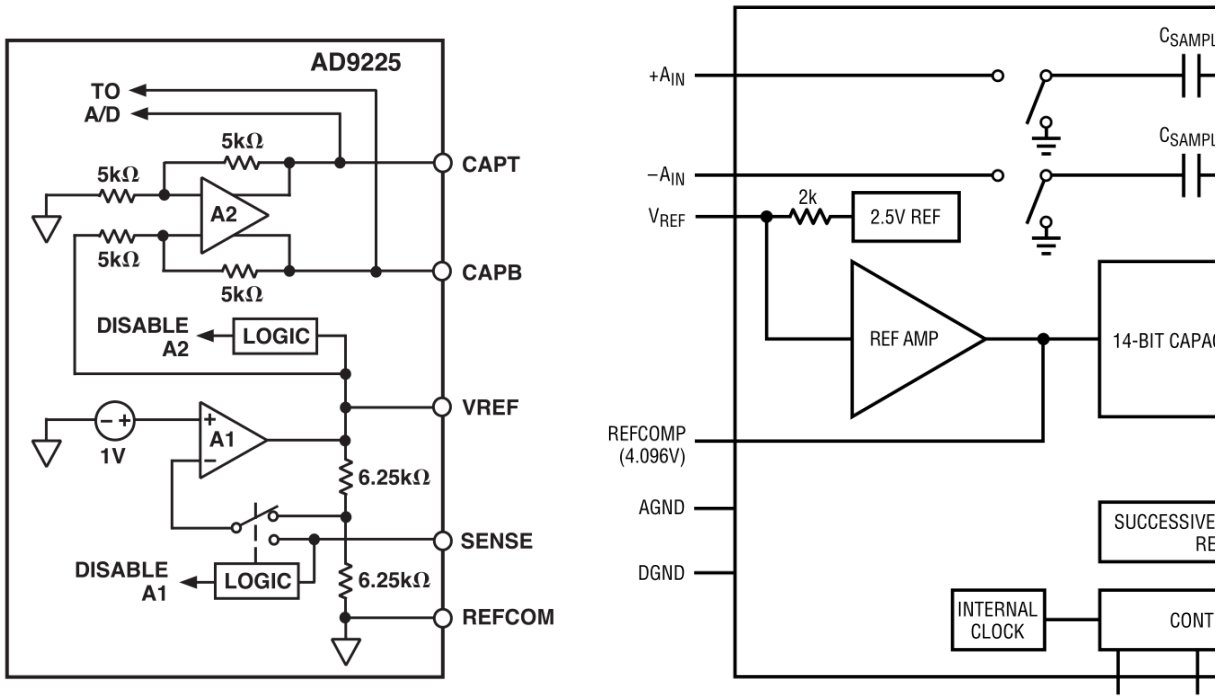


Figure 3.3: Resolution vs Deviation from Nominal Vref



(a) AD9225 Reference Circuit

(b) LTC1419 Reference Circuit

Figure 3.4: ADC Reference Circuits

and reference level returned.

$$\begin{aligned} N_{\text{effective}} &= N_{\text{ideal}} - \log_2\left(\frac{V_{\text{REF,meas}}}{V_{\text{REF,nominal}}}\right) \\ &= 14 + \log_2\left(\frac{0.98\text{V}}{2.5\text{ V}}\right) \\ &= 12.65 \text{ bits} \end{aligned} \tag{3.2}$$

$$\begin{aligned} \text{SNR}_{\text{original}} - \text{SNR}_{\text{degraded}} &= 6.02(N_{\text{original}} - N_{\text{degraded}}) \\ &= 64 + 6.02 \cdot \log_2\left(\frac{0.98\text{ V}}{2.5\text{ V}}\right) \\ &= 55.87 \text{ [dB]} \end{aligned} \tag{3.3}$$

There are several key takeaways from the above observations, namely that a converter's internal reference amplifier must maintain functionality or its output must be able to be driven externally, and some testing is necessary to determine the functionality of converter references and amplifiers. To include the effects of non-ideal reference voltage

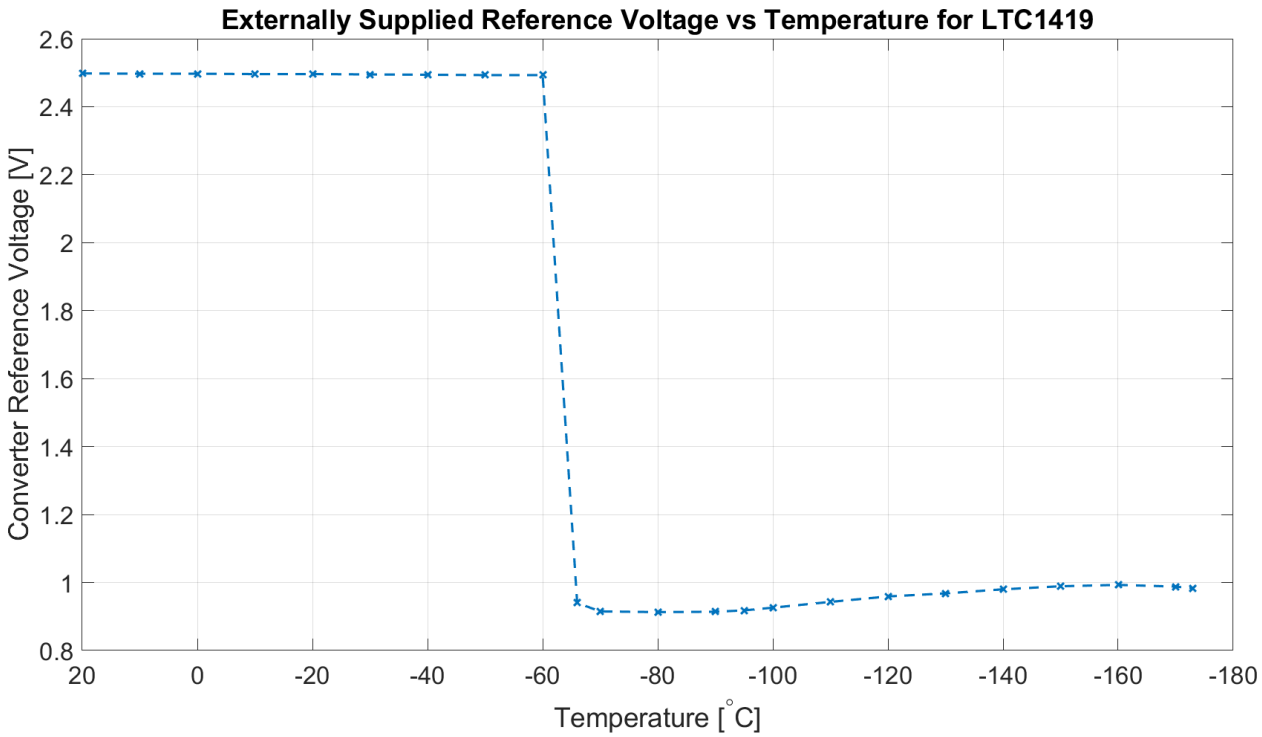


Figure 3.5: LTC1419 Reference Voltage Collapse

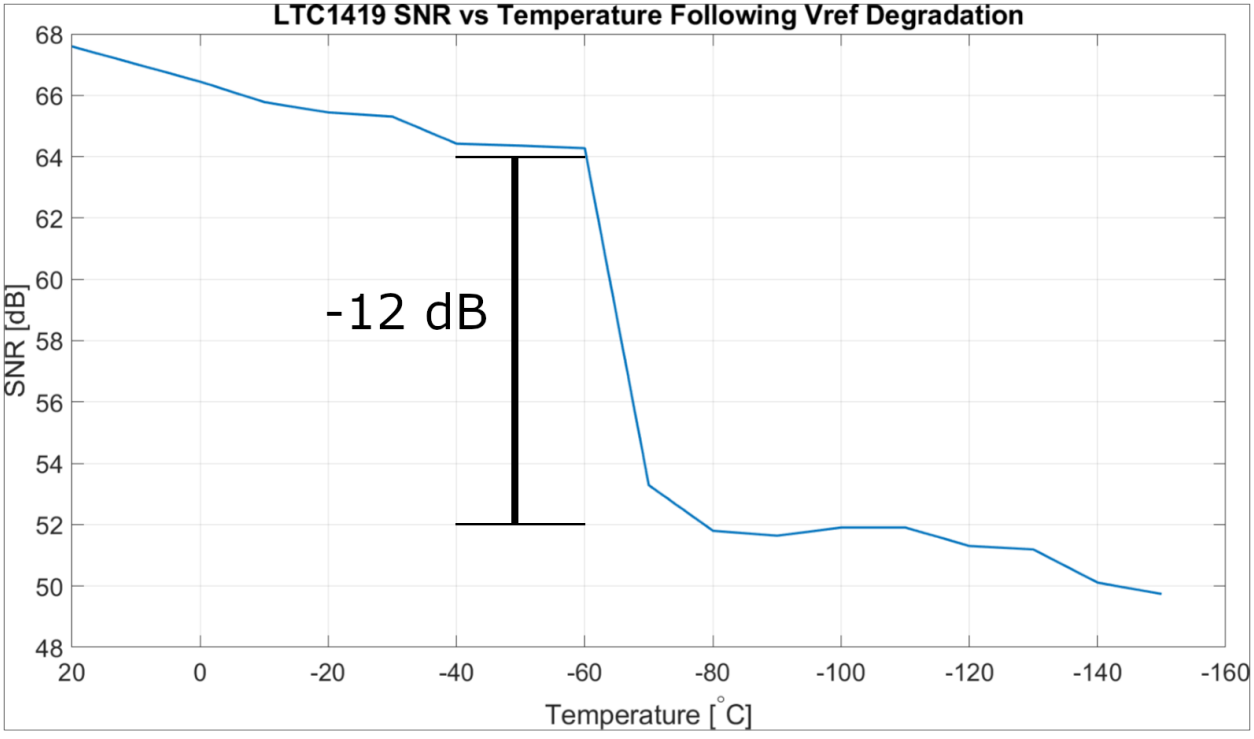


Figure 3.6: LTC1419 SNR Degradation with Vref Collapse

with temperature, one can measure its variation across temperature and either perform a polynomial fit whose coefficients are stored and reconstructed or use a piecewise linear approximation in the form of a look-up table (LUT) with interpolation.

3.2.2 THA Block Model

An important block accounting for many aspects of overall ADC performance is the front-end tracking amplifier used in most Nyquist-rate applications. When using a tracking amplifier, it is necessary to meet requirements concerning gain, bandwidth, slew rate, and settling time. Figure 3.7 shows a single-pole tracking system with finite gain and zero-order hold at the end. Block diagram analysis results in the following equations where X and Y refer to the input and output respectively:

$$Y = \omega_{pole}\left(\frac{GX - Y}{s}\right) \tag{3.4}$$

$$\frac{Y}{X} = \frac{G}{1 + \frac{s}{\omega_{pole}}} \tag{3.5}$$

Although a single-pole response may seem unnecessarily simplistic, our test frequencies were nowhere near the stated limits of the actual amplifier so the approximation was not unwarranted. The block representation includes the ability to change DC gain, the dominant pole frequency, as well as the slew-rate of the amplifier.

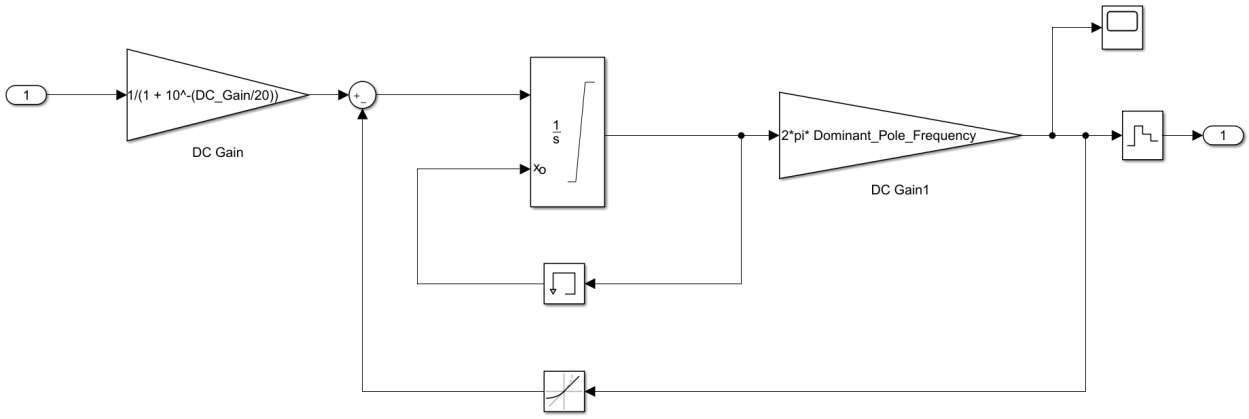


Figure 3.7: Generic Block Representation of THA

3.2.3 Polynomial Predistortion

In addition to quantization noise, ADCs introduce distortion into the input signal due to internal amplification, hysteretic effects, and non-ideal behavior of components like capacitors which may have a non-linear relationship with an input signal. The degree of distortion depends on various factors including tracking amplifier performance and architecture-specific internal circuitry operating during conversion. When evaluating COTS ADCs without access to internal nodes, it is very difficult to isolate specific contributors to overall performance but it is possible to behaviorally incorporate predistortion while assuming ideal quantization. This is because modern converters are subject to Bennett's analysis which states that quantization introduces distortion that is not significantly correlated with the input and may be regarded as noise [2]. Multiplying the processed input prior to quantization by a polynomial introduces the proper amount of distortion proportional to what can be measured. In practice, testing the converter revealed harmonic content in the form of THD coefficients which, when measured across temperature, made possible parameterization of the polynomial coefficients as well.

The task that remains is to compute power series coefficients from measured THD harmonics. Doing so requires that the relationship between sinusoidal amplitudes and power series representation be established [28, 29]. The degree of nonlinearity in the distortion polynomial determines the highest harmonic included in the simulated output; since testing revealed that the harmonic at $5 \times f_{\text{in}}$ was usually sufficient to characterize the "important" distortion, only 6 components total were used. To aid in computing power series terms from sinusoidal coefficients, Table 3.1, showing common power expressions of trigonometric identities for both sine and cosine terms, was used. In equations 3.6 and 3.7, the output

Table 3.1: Sine and Cosine Power Formulae

Sine	Cosine
$\sin^2 x = \frac{1-\cos(2x)}{2}$	$\cos^2 x = \frac{1+\cos(2x)}{2}$
$\sin^3 x = \frac{3\sin x-\sin(3x)}{4}$	$\cos^3 x = \frac{3\cos x+\cos(3x)}{4}$
$\sin^4 x = \frac{3-4\cos(2x)+\cos(4x)}{8}$	$\cos^4 x = \frac{3+4\cos(2x)+\cos(4x)}{8}$
$\sin^5 x = \frac{10\sin x-5\sin(3x)+\sin(5x)}{16}$	$\cos^5 x = \frac{10\cos x+5\cos(3x)+\cos(5x)}{16}$

is y and input is x. To avoid numerical errors and ill-conditioned matrices, the input was normalized on the range $[-1, \ldots, 1]$ by dividing the input voltage by the reference voltage before computing the signal power of the fundamental and its harmonics and the sinusoidal coefficients could then be matched term by term to the power series coefficients.

$$x = A\cos\theta \tag{3.6}$$

$$\begin{aligned} y =& a_0 + a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4 + a_5 x^5 \\ =& \big(a_0 + \frac{1}{2}a_2 A^2 + \frac{3}{8}a_4 A^4\big) + \\ & \big(a_1 A + \frac{3}{4}a_3 A^3 + \frac{5}{8}a_5 A^5\big)\cos\theta + \\ & \big(\frac{1}{2}a_2 A^2 + \frac{1}{2}a_4 A^4\big)\cos(2\theta) + \\ & \big(\frac{1}{4}a_3 A^3 + \frac{5}{16}a_5 A^5\big)\cos(3\theta) + \\ & \big(\frac{1}{8}a_4 A^4\big)\cos(4\theta) + \\ & \big(\frac{1}{16}a_5 A^5\big)\cos(5\theta) \end{aligned} \tag{3.7}$$

Returning to the calibration of power series based on standard sinusoidal THD test data, it is necessary to match each harmonic coefficient against the six power series coefficients. Since the amplitude is assumed known and the input stationary, the necessary harmonic components can be obtained by performing a standard FFT on the sinusoidal output data. Denoting the Fourier magnitude transform as $X(f) = |\mathrm{FFT}(x)|$ yields a set of linear equations shown in Equation 3.8 and in matrix form in Equation 3.9.

$$\begin{aligned} X(0) &= a_0 + \frac{1}{2}a_2 A^2 + \frac{3}{8}a_4 A^4 \\ X(f_{in}) &= a_1 A + \frac{3}{4}a_3 A^3 + \frac{5}{8}a_5 A^5 \\ X(2f_{in}) &= \frac{1}{2}a_2 A^2 + \frac{1}{2}a_4 A^4 \\ X(3f_{in}) &= \frac{1}{4}a_3 A^3 + \frac{5}{16}a_5 A^5 \\ X(4f_{in}) &= \frac{1}{8}a_4 A^4 \\ X(5f_{in}) &= \frac{1}{16}a_5 A^5 \end{aligned} \tag{3.8}$$

$$\begin{bmatrix} X(0) \\ X(f_{in}) \\ X(2f_{in}) \\ X(3f_{in}) \\ X(4f_{in}) \\ X(5f_{in}) \end{bmatrix}_{6\times1} = \begin{bmatrix} 1 & 0 & \frac{1}{2}A^2 & 0 & \frac{3}{8}A^4 & 0 \\ 0 & A & 0 & \frac{3}{4}A^3 & 0 & \frac{5}{8}A^5 \\ 0 & 0 & \frac{1}{2}A^2 & 0 & \frac{1}{2}A^4 & 0 \\ 0 & 0 & 0 & \frac{1}{4}A^3 & 0 & \frac{5}{16}A^5 \\ 0 & 0 & 0 & 0 & \frac{1}{8}A^4 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{16}A^5 \end{bmatrix}_{6\times6} \begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \end{bmatrix}_{6\times1} \tag{3.9}$$

The solution to this set of linear equations gives the coefficients of a polynomial which predistorts the input before quantization, giving rise to the proper amount of distortion. This procedure was done for two sets of AD9225 data as shown in Figures 3.9 and 3.10, and for the LTC1419 as shown in Figure 3.8. The similarity of both simulated and measured THD figures indicates that the polynomial predistortion approach is valid. Implementing the predistortion in terms of the generic block model shown on Figure 3.7 is done by storing the calibrated power series coefficients in a look-up table (LUT) and allowing the user to select between different temperatures. Since the polynomial calibration was done for only a finite number of temperatures, linear interpolation of polynomial coefficient values between temperature points is required. Figures 3.11, 3.12 and 3.13 show 3D waterfall plots of the distortion portions of the polynomials and their increased curvature near the edges of converter range indicates that input range compression may be an influencing factor.

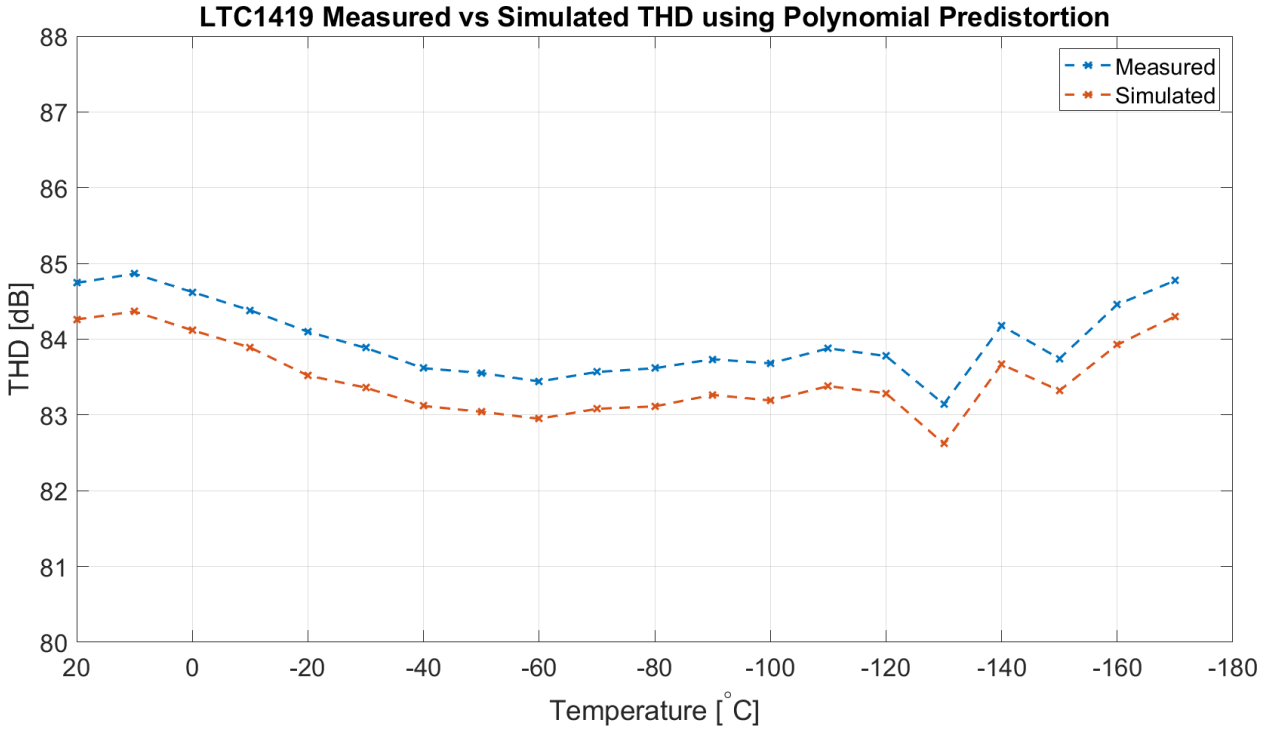


Figure 3.8: LTC1419 THD Using Polynomial Predistortion

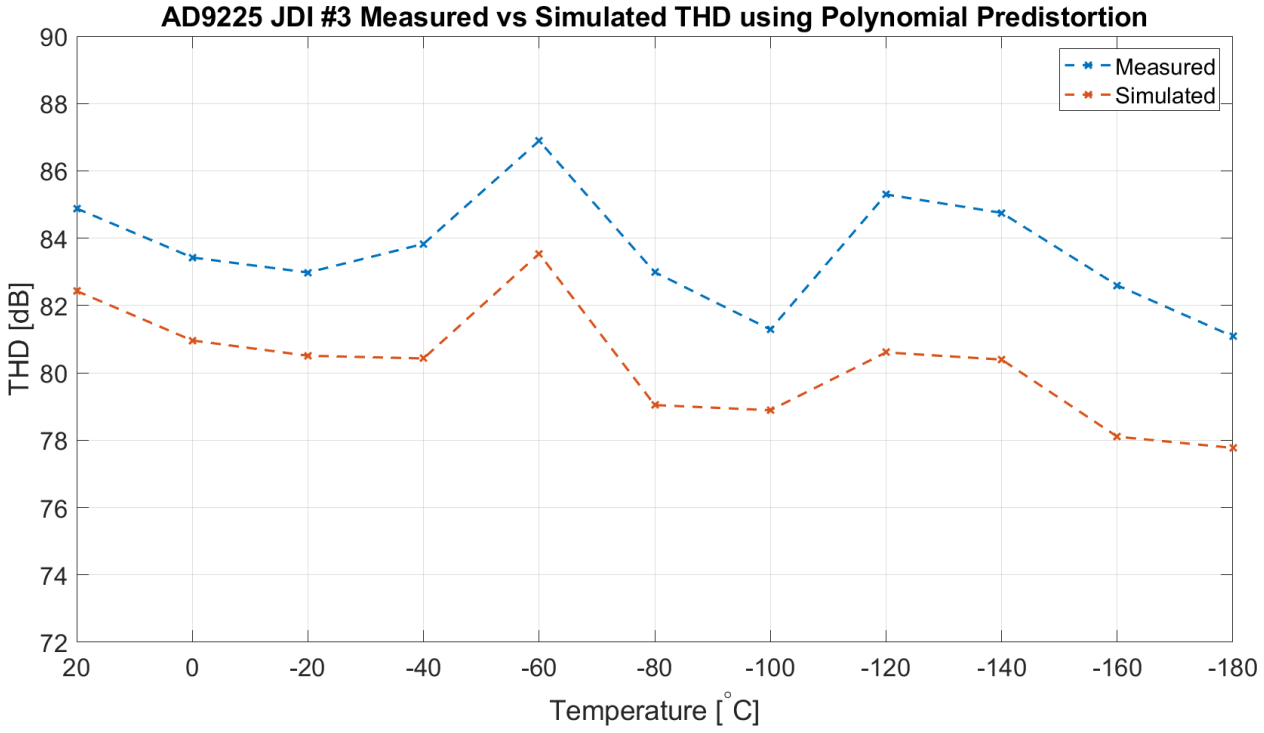


Figure 3.9: AD9225 THD Using Polynomial Predistortion

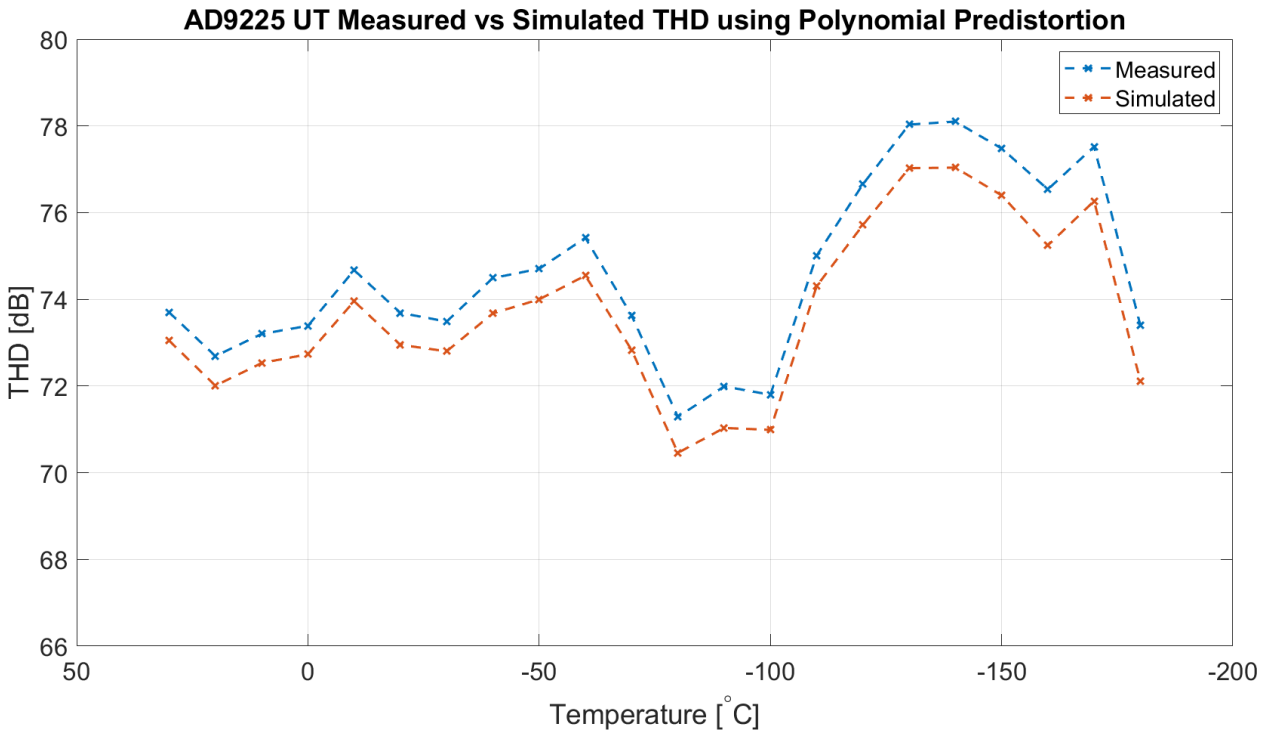


Figure 3.10: AD9225 THD Using Polynomial Predistortion

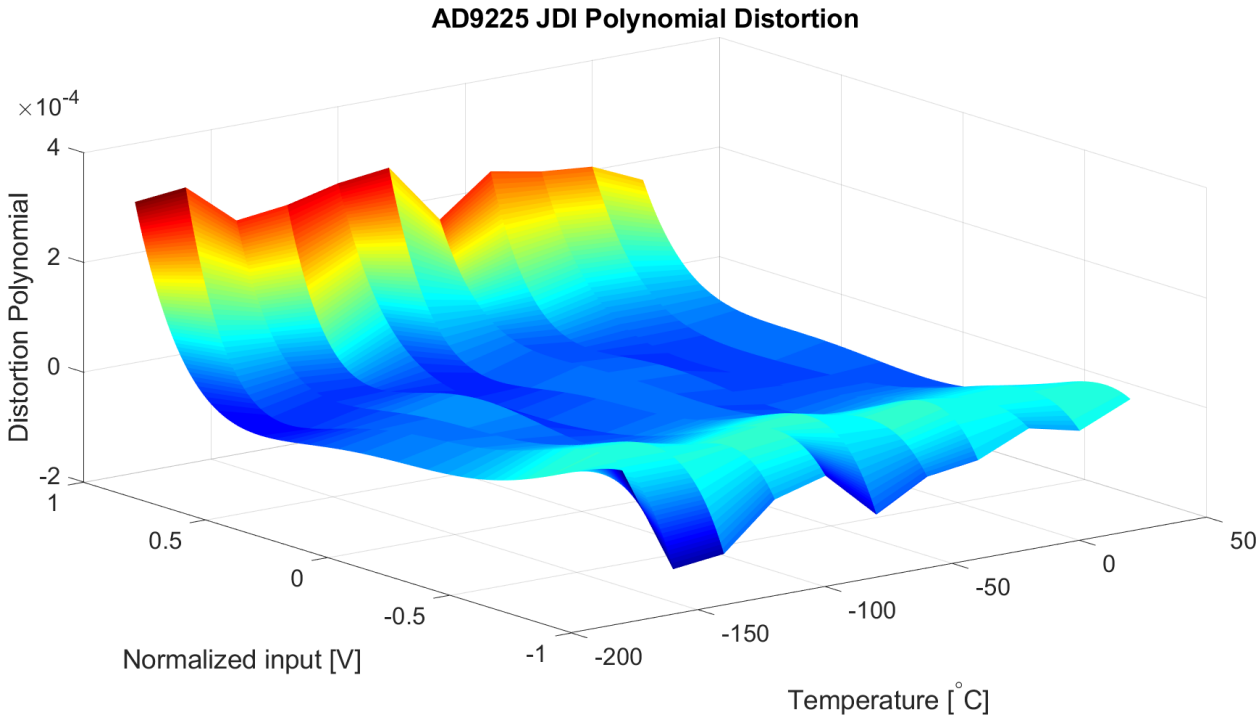


Figure 3.11: JDI AD9225 Distortion Polynomial

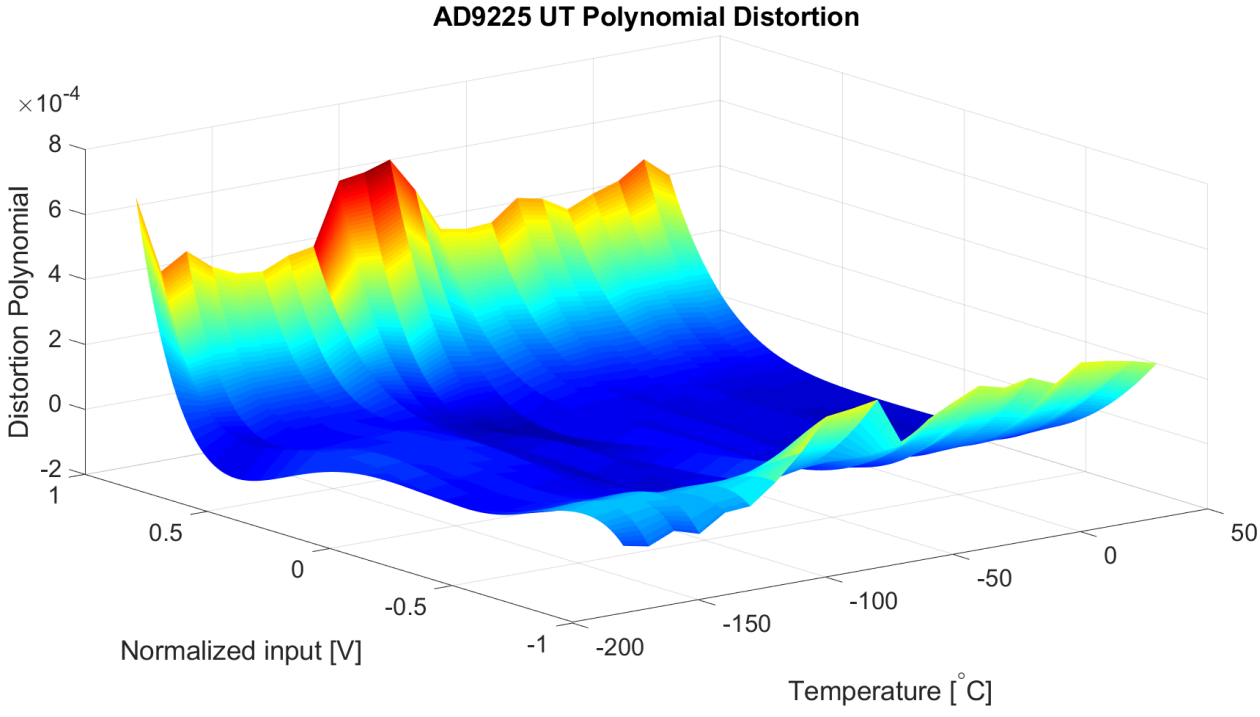


Figure 3.12: UT AD9225 Distortion Polynomial

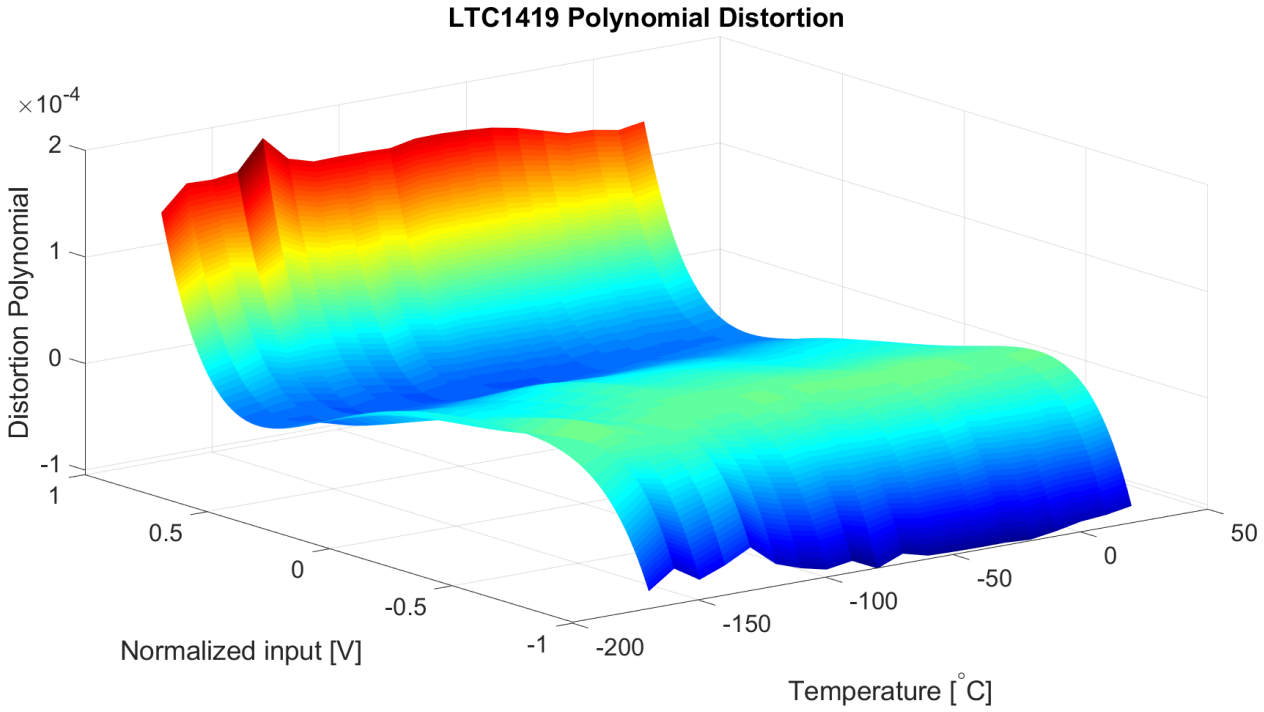


Figure 3.13: LTC1419 Distortion Polynomial

3.2.4 Input-Referred Noise

In addition to modeling THD via a polynomial distortion function, the additive noise level on top of quantization of the converter must also be accounted for. As discussed in Chapter 2, the quantization process itself generates distortion, usually modeled as additive noise, which degrades the input's SNR and limits the meaningful signal level a converter can respond to. Additional noise in the system, arising from a range of sources, further impacts converter performance. For most purposes, this can be considered additive Gaussian noise whose variance can be obtained from standard sinusoidal tests measuring SNR. After computing the appropriate noise level, measurements again revealed a very close match between the calibrated and measured level as shown in Figures 3.14 and 3.15.

3.2.5 Jitter

Jitter refers to uncertainty in the sampling instant which, depending on the input signal slope, introduces a corresponding uncertainty or error in the observed and quantized output. This can be incorporated into the converter model in one of two ways, either by directly introducing a random phase onto the sample clock or by noting the approximately linear relationship between time and signal uncertainty. The limits of a converter's SNR imposed by jitter can be a concern. Considering the simplest case of a sinusoidal input yields Equation 3.10 for a jittery input, Equation 3.11 for the error due to jitter, and Equation 3.12 for the RMS error due to jitter [1]. Equation 3.13 [1] gives the theoretical maximum SNR due to jitter with variance σ_t^2.

$$\begin{aligned} V_i &= A\sin(\omega(t+t_j)) \\ &= A\sin(\omega t)\cos(\omega t_j) + A\cos(\omega t)\sin(\omega t_j) \\ &= A\sin(\omega t)\left[1 - 2\sin^2(\frac{\omega t_j}{2})\right] \\ &+ A\cos(\omega t)\left[2\sin(\frac{\omega t_j}{2})\cos(\frac{\omega t_j}{2})\right] \\ &\approx A\sin(\omega t) + A\omega t_j\cos(\omega t_j) \end{aligned} \tag{3.10}$$

[1] Using identities from [30]: $\sin(z_1+z_2) = \sin(z_1)\cos(z_2) + \cos(z_1)\sin(z_2)$, $\cos(2z) = 2\cos^2(z) - 1 = 1 - 2\sin^2(z)$

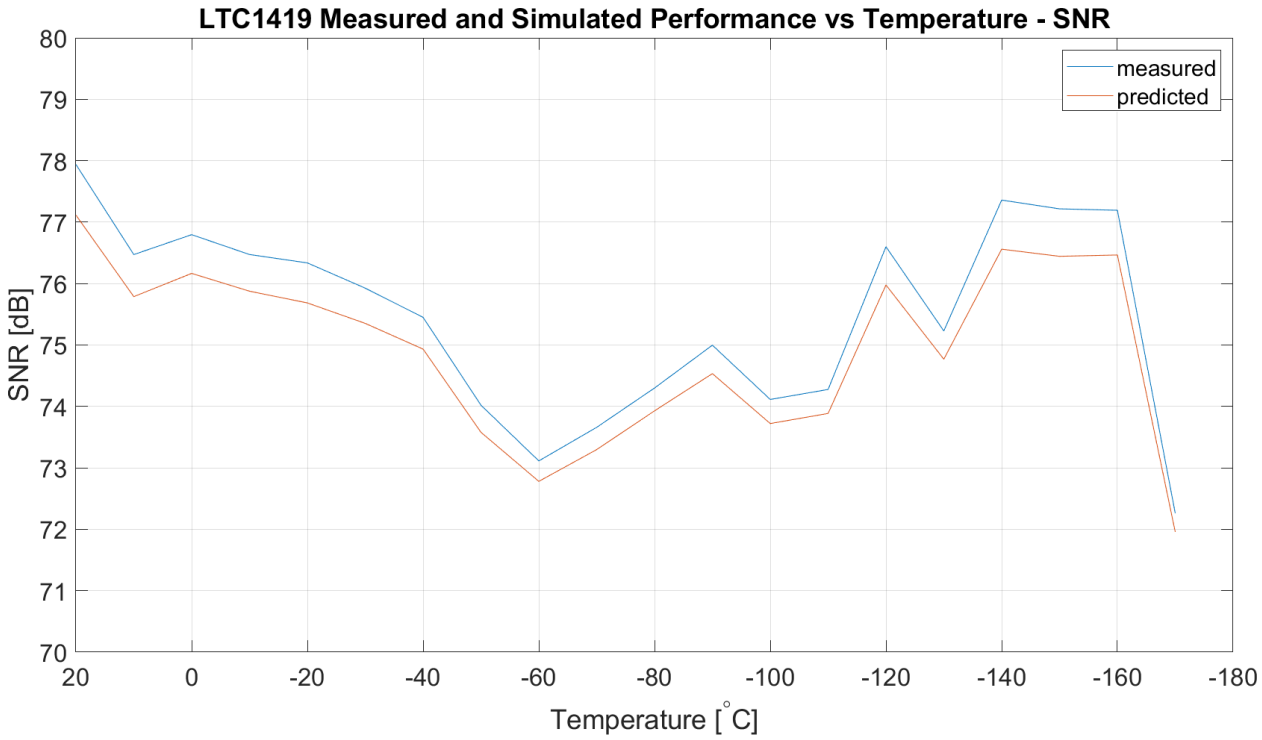


Figure 3.14: LTC1419 SNR - Model vs Measured

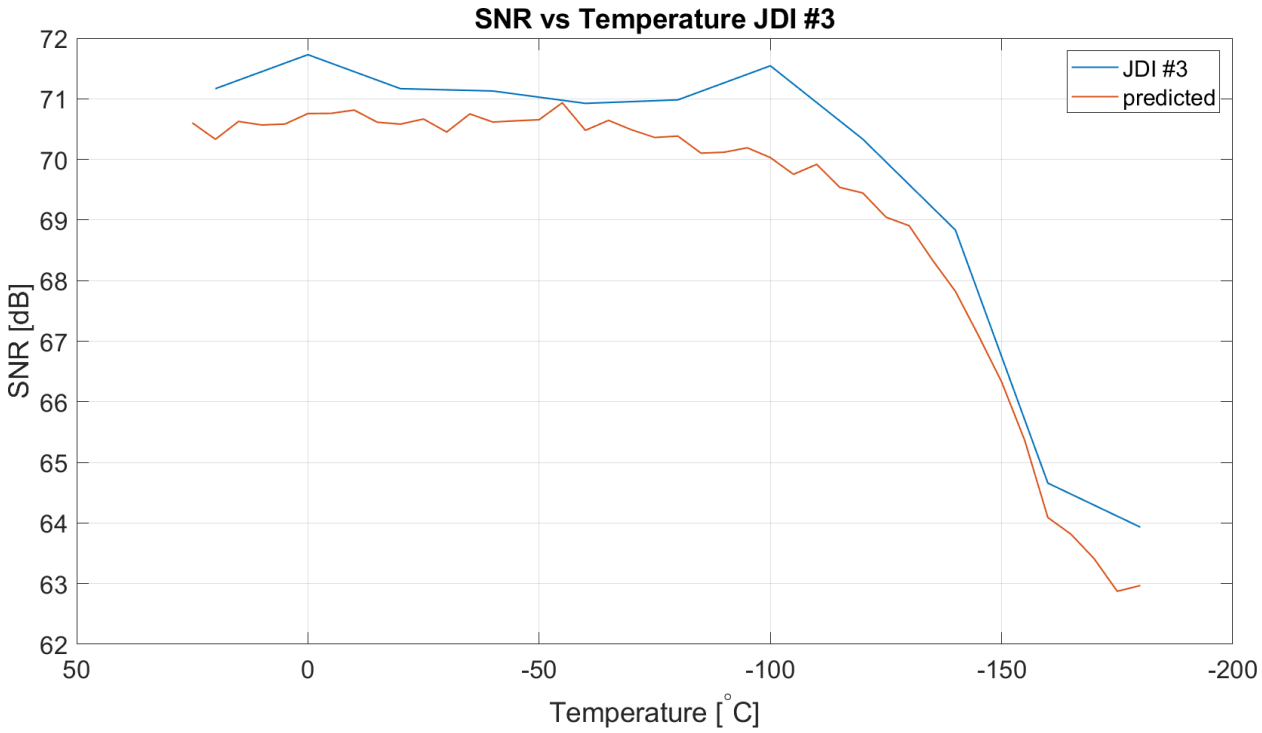


Figure 3.15: AD9225 SNR - Model vs Measured

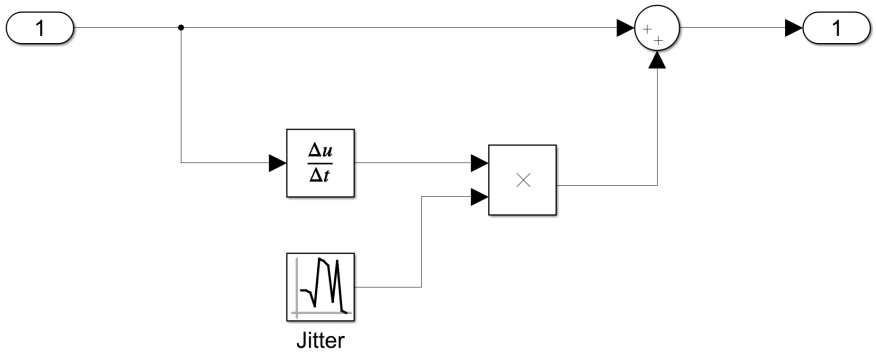


Figure 3.16: Behavioral Block Implementing Jitter

$$\begin{aligned} \epsilon(t) &= V_i - A\sin(\omega t) \\ &\approx A\omega t_j \cos(\omega t_j) \end{aligned} \tag{3.11}$$

$$\begin{aligned} \overline{\epsilon^2(t)} &= \overline{t_j^2} \cdot \frac{1}{T}\int_0^T \left[A\omega\cos(\omega t)\right]^2 dt \\ &= \frac{A^2\omega^2\sigma_t^2}{2} \end{aligned} \tag{3.12}$$

$$\text{SNR} = -20\log_{10}(\omega\sigma_t) = -20\log_{10}(2\pi f\sigma_t) \tag{3.13}$$

For the AD9225, $\sigma_t = 1$ ps and $\omega_{\text{Max}} = 2\pi \times 25$ MHz yielding a maximum SNR of $-20\log_{10}(\omega\sigma_t) = 98.06$ dB, well above the 74 dB noise floor due to quantization noise. This theoretical prediction corresponded with testing, namely that jitter was never a concern.

Returning to the inclusion of jitter in the generic ADC model, one may assume a linear uncertainty relationship between time and amplitude, with the timing uncertainty represented as a Gaussian distributed noise, leading to Equation 3.14 where t_j is the RMS jitter. A block incorporating this effect is shown in Figure 3.16.

$$V_{jitter} = \left|\frac{dV_{in}}{dt}\right| \times t_j \tag{3.14}$$

One common way of testing for jitter is so-called beat testing [31, 32]. During such tests, a set of data is taken for a particular periodic waveform, usually a sinusoid. Next, another set of data is taken for the same waveform but with a period that is augmented by the sampling period. Any differences in observed performance between the two sets of data are due to

jitter. In testing, this phenomenon was never observed most likely due to the relatively low sample rate of our device (< 25 MHz).

3.3 Datasheet Cryogenic Predictive Performance Model

A major goal of the project is to predict or extrapolate part performance from limited data enabling engineers to better downselect parts with fewer time and cost burdens associated with thorough characterization. Towards this end, a methodology is proposed which takes advantage of standard datasheet information to generate a behavioral converter model and extend its performance across temperature, hopefully enabling some measure of predictive performance. Such a model would be useful in scenarios where expensive, time-consuming testing is to be avoided. The basic idea is to consider only the components necessary to simulate any converter regardless of architecture; for most applications, this includes a front-end THA and the internal quantization process. The next step is to generate a behavioral ADC model purely from existing *a priori* information without testing and to then to apply measured performance trends and compare predicted with measured output. The model methodology can be broken down into several steps, namely the following: (1) choosing a part to test and model; (2) reverse-engineering the parameters required of the front-end THA, if applicable; (3) obtaining the device's transfer curve; and (4) building a model from existing information and (5) applying parametric performance trends obtained from other parts. The individual steps in this process will be explained in more detail below.

3.3.1 Reverse-Engineering of THA Parameters

A good overview of salient specifications for realistic behavioral amplifier modeling is found in [33] and [34]. More specifically, the basic operation of the amplifier is one of tracking combined with feedback. As transistors are used as the switch elements, non-ideal effects like switch on-resistance, input-dependent charge injection, clock feedthrough, jitter, thermal noise, and flicker noise are present. The 1st order response of the amplifier may be included as well. This approach takes the existing amplifier model and includes the effects of the sampling network around it.

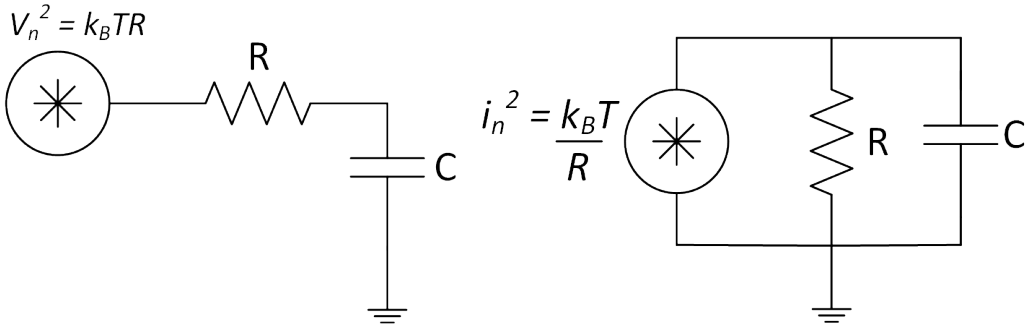


Figure 3.17: kTC Noise

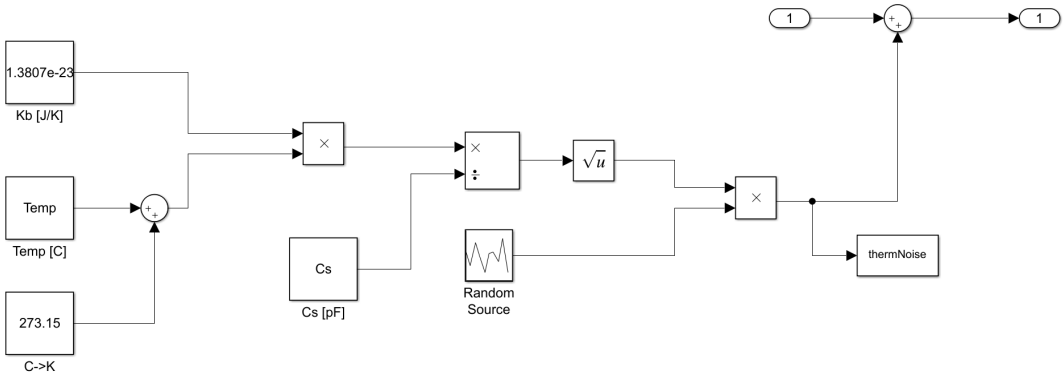


Figure 3.18: Thermal Noise

Jitter

As explained above in a previous section, jitter is modeled behaviorally according to a linear relationship between the input derivative and the expected jitter value so further modification is unnecessary.

Switch Thermal Noise

On account of a resistive element's thermal noise, very sensitive systems are sometimes run under cryogenic conditions to improve their fidelity. It is therefore somewhat surprising that the measured noise performance of both converters tested noticeably decreased beyond a certain temperature. Though I suspect this was due to increased switching noise, it remains a fact that thermal noise is a concern in most applications. For THAs, the noise contribution of the sampling network around the amplifier can be a limiting factor.

J. B. Johnson first observed and described thermal noise in [35] and correctly speculated that it refers to random charge fluctuations caused by thermal energy. In the original paper, an expression is developed in terms of the real part of a terminating element's impedance, $R(\omega)$, along with the power transfer admittance characteristic, $Y(\omega)$ as shown in Equation 3.15 where k_B is Boltzmann's constant and T is the temperature in Kelvin. Only a short time later, H. Nyquist in [36] gave a theoretical justification for the popular form of thermal noise power by appealing to statistical mechanics and the equipartition theorem as shown in Equation 3.16.

$$\bar{I}^2 = \frac{2k_BT}{\pi}\int_0^\infty R(\omega)|Y(\omega)|^2 d\omega \tag{3.15}$$

$$\overline{v_n^2} = 4k_BTR \tag{3.16}$$

Although more exact expressions for thermal noise in switched-capacitor networks have been developed [37], it is sufficient for most purposes to consider the 1st order LPF cases illustrated in Figure 3.17. The series sampling capacitor $C_s = 5$ pF for the AD9225; in this case, the equivalent RMS noise voltage due to the sampling switch and capacitor is given by Equation 3.17. A behavioral implementation of thermal noise is shown in Figure 3.18 where the effect is to add noise in series with the input.

$$\begin{aligned}
\text{NTF} &= \overline{v_n^2}\int_0^\infty |H(\omega)|^2 d\omega \\
&= 4k_BTR\int_0^\infty \frac{d\omega}{1+\frac{\omega}{\omega_p}} \\
&= 4k_BTR\cdot\frac{\omega_{\text{enbw}}}{2\pi} \\
&= 4k_BTR\cdot\frac{1}{4RC} \\
&= \frac{k_BT}{C_s}
\end{aligned} \tag{3.17}$$

Switch Charge Injection

During the 'on' period of a CMOS switch, charge is stored under the gate permitting charge flow across the device. When the device is turned off, however, some fraction of this stored charge is injected onto the sampling node, decreasing the held voltage. This

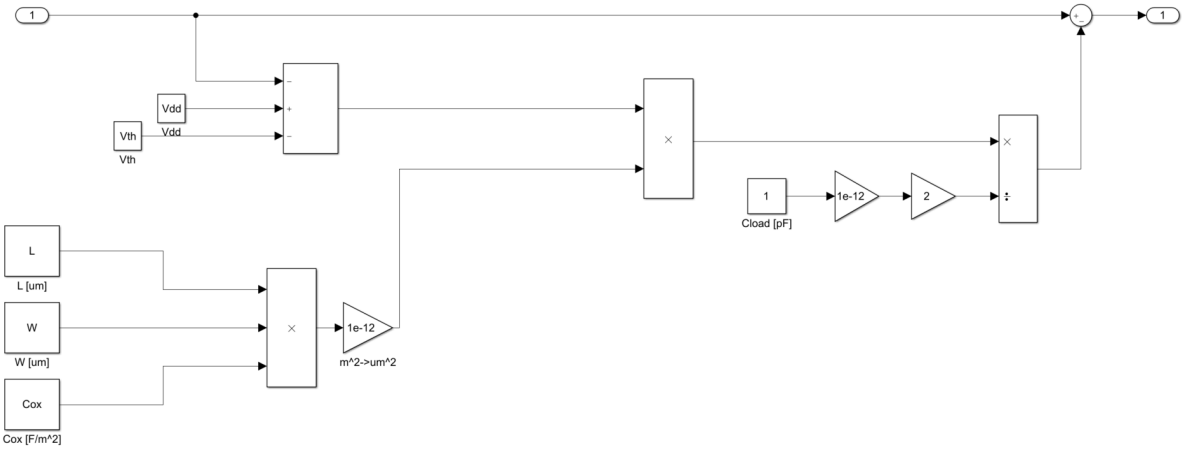


Figure 3.19: Switch Charge Injection

effect, with careful design techniques like correlated double sampling (CDS), is independent of the input signal and results in a constant offset that can be calibrated out or greatly reduced by the addition of a dummy transistor or through using a fully differential input stage. According to standard heuristics [38], the stored gate charge can be expressed in the following equations permitting an expression incorporating such an effect during turn off. The behavioral implementation is shown in Figure 3.19.

$$Q_{CH} = W \times L \times C_{ox}(V_{GS} - V_{TH}) \tag{3.18}$$

$$V_{GS} = V_{DD} - V_{in} \tag{3.19}$$

$$\begin{aligned} V_{inj} &= -\frac{Q_{CH}}{C_s} \\ &= -\frac{W \times L \times C_{ox}(V_{DD} - V_{in} - V_{TH})}{C_s} \end{aligned} \tag{3.20}$$

Gain

Negative feedback action is used in both tracking and hold configurations. To maintain an output within 1 LSB of the input, the amplifier's gain in the bandwidth of interest must be above a certain nominal value. This value can be approximated by considering a 1st order

system responding to a step input which must settle within the sampling period. One can show that during the holding period, $\frac{V_{\mathrm{FS}}}{1\mathrm{LSB}} < A_{\mathrm{OL,DC}}$ [1].

For the AD9225, $V_{\mathrm{FS}} = 4$ V, 1 LSB $= \frac{4}{2^{12}} = 976.5625$ µV and $\mathrm{A_{OL,DC}} > 4,096$ [V/V]. In most amplifiers, however, gain is a nonlinear function of the output voltage. As the amplifier's output approaches the supply rails, there is usually a degradation in the amount of DC gain which can force the error to zero using negative feedback. Since this gain varies with input and thus output signal level, it introduces distortion into the signal path. In equation form, this can be expressed by making the gain itself a function of the output voltage level:

$$A = A_o(1 + \alpha_1|V_o| + \alpha_2|V_o|^2 + \dots) \tag{3.21}$$

Parameterizing the constants in Equation 3.21 allows one to take into consideration the nonlinear output characteristic sometimes found in amplifiers.

Bandwidth

Closely related to the notion of an amplifier's overall gain is its gain-bandwidth product (GBW). The main idea is that the amplifier must settle to within 1 LSB within half the sampling period. By considering the gain error a function of the DC open-loop gain, the steady-state step response error is given by [39]

$$e^{-\frac{T_s}{2\tau}} = e^{-\frac{\pi f_p}{F_s}} < 1 \text{ LSB} \tag{3.22}$$

$$f_p > \frac{F_s \ln(1 \text{ LSB})}{\pi} = 55 \text{ MHz} \tag{3.23}$$

Slew Rate

Slew rate is closely related to the notion of full-power bandwidth (FPBW), the frequency at which a full-scale sinusoidal input has a maximum rate of change equal to the amplifier's slew rate. According to [40] and the definition above, full-power bandwidth can be expressed as in Equation 3.24 and related to slew rate in Equation 3.25 where V_p refers to the peak input amplitude of a sine wave. The necessary parameters can be incorporated into the THA

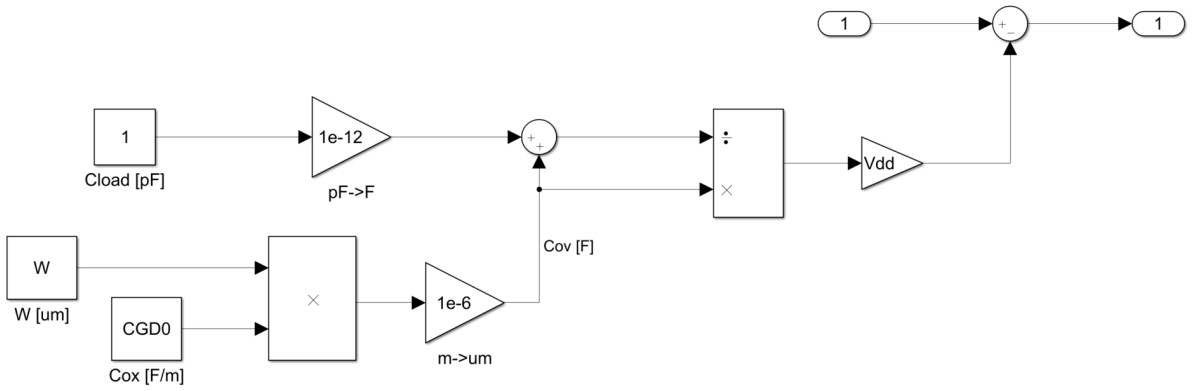


Figure 3.20: Clock Feedthrough

model according to datasheet estimates of either SR or FPBW.

$$\begin{aligned} \text{FPBW} &= \frac{\text{SR}}{2\pi V_p} \\ &= \frac{\text{SR}}{\pi \cdot V_{\text{FS}}} \end{aligned} \tag{3.24}$$

$$\begin{aligned} \text{SR} &= \pi \cdot \text{FPBW} \cdot V_{\text{FS}} \\ &= \pi \cdot 125 \text{ MHz} \cdot 4 \text{ V} \\ &= 1570 \text{ V/µs} \end{aligned} \tag{3.25}$$

Clock Feedthrough

As shown in Figure 3.20, clock feedthrough refers to the capacitive coupling of clock edges onto the signal path via the series sampling switch. This parameter is thus technology and size dependent due to parasitic gate-source capacitance C_{GD} as shown by Equation 3.26. Practically, the sampling transistor size needs to be estimated either by rule of thumb or from prior literature.

$$V_{clk} = -\frac{WC_{GD0}}{WC_{GD0} + C_L} \times V_{DD} \tag{3.26}$$

$1/f$ Noise

Different generating mechanisms are thought to exist but a simplified view from [38] is given by Equation 3.27. This noise can be generated by passing Gaussian noise with unit variance through a LPF to achieve the spectral density before then multiplying the result by the flicker noise constant K_f to achieve the proper variance. For 0.5 µm technology, $K_f = 1 \times 10^{-27}$ C^2/m^2. Figure 3.22 shows a typical input/output set of curves for the described THA model.

$$V^2{}_{\text{flicker}} = \frac{K_f}{C_{ox}WL}\frac{1}{f}\ [\text{V}^2/\text{Hz}] \tag{3.27}$$

3.3.2 Datasheet Transfer Curve Reconstruction

An ADC's transfer curve is a monotonically increasing set of converter decision levels that can be used to incorporate non-ideal effects of quantization. With two major blocks then, the THA and quantizer, one can model most salient characteristics of an ADC behaviorally from input-output data only. Constructing the transfer curve requires several items, namely the following: (1) offset error, a parameter indicating the difference between the ideal first transition level and the actual measured one; (2) gain error, a parameter indicating the degree to which the converter decision levels depart from their ideal levels, basically a slope error; and (3) non-linearity error, a set of values that describe the differences between the measured and ideal decision levels once a linear trend has been removed. Fortunately, all three items can be obtained from a datasheet without testing. Furthermore, standard ADC tests can be used to determine a converter's transfer curve [17]. The main idea is to characterize an ADC's transfer curve across different temperatures, identifying parametric trends which can then be applied *a priori* to obtain an estimate of converter performance without the need for timely, costly testing. Of course, this methodology is useful only to the extant that it predicts and/or explains measured behavior.

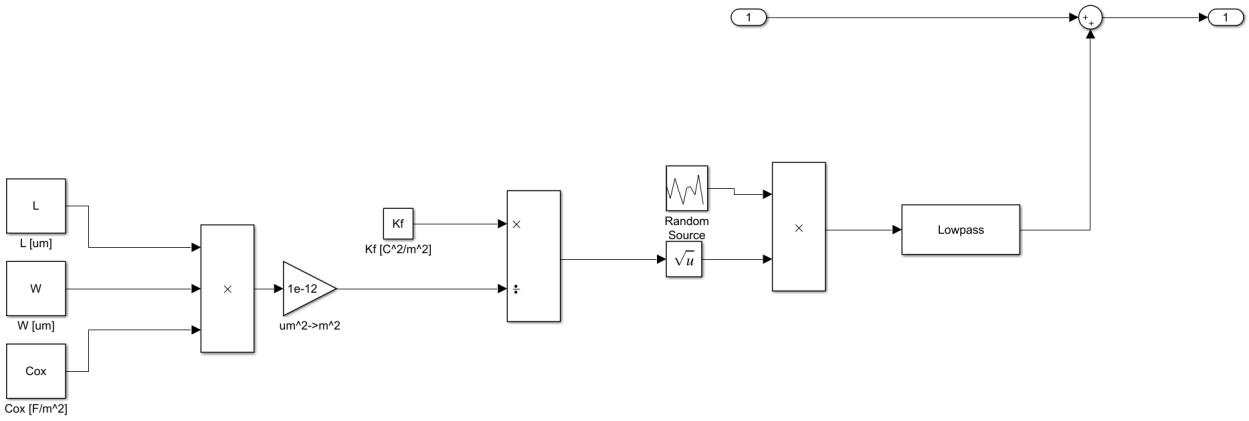


Figure 3.21: Flicker Noise

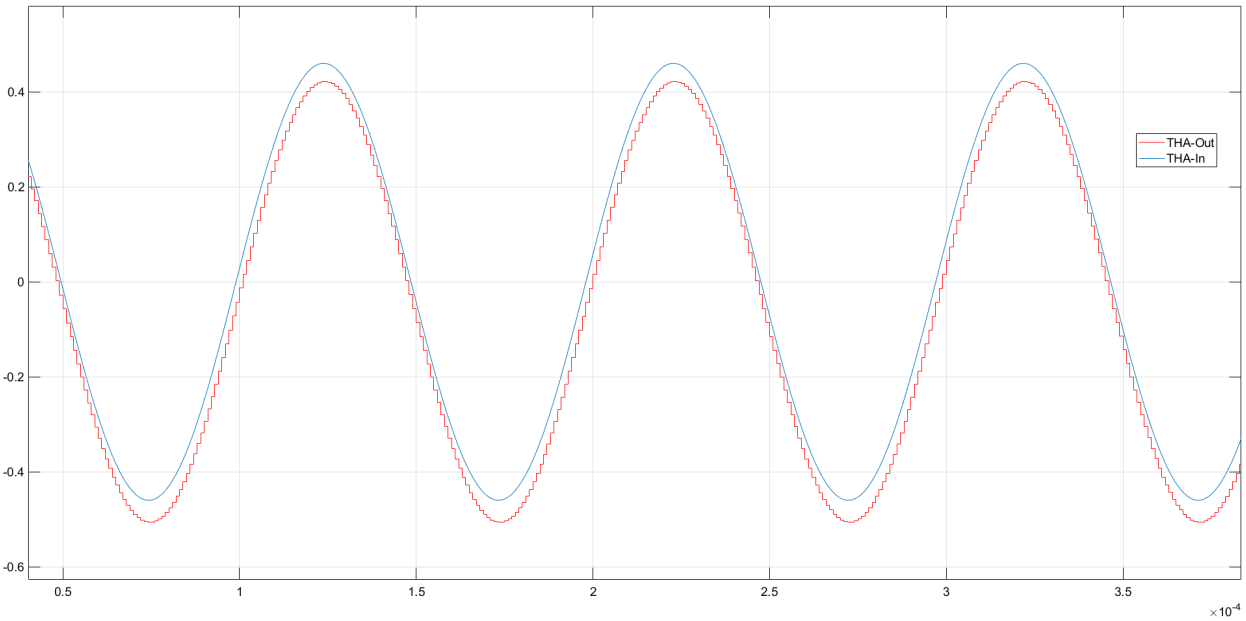


Figure 3.22: Behavioral THA Input and Output

Table 3.2: Transfer Curve Parameters for ADCs Tested

	Offset Voltage [%FSR]	Gain Error [%FSR]	Number of Bits
AD9225	±0.3	±0.5	12
LTC1419	±0.15	±0.30	14

Offset, Gain Error

Datasheets typically give a range of values for offset and gain error, usually measured in percent full-scale. Equations converting offset error to LSBs are given below where T_k refers to the transfer curve.

$$V_{\mathrm{OS}}[\mathrm{LSB}] = T_k(1) - 0.5 \tag{3.28}$$

$$GE[\%FSR] = 100 \times \frac{T_k(2^N - 1) - T_k(1) - (2^N - 2)}{2^N - 2} \tag{3.29}$$

Because datasheets give typical ranges, when constructing likely transfer curves, it is possible to assume either a uniform or normal distribution of offsets and gain errors. This enables statistical calculation of expected performance using the transfer characteristics of a device.

INL

The INL curve represents non-linearity inherent in the device contributing towards distortion in the output. For the transfer curve to be used as a predictor of performance, it must be possible to describe and forecast it. From looking at a standard INL curve from a datasheet, it can be seen that there are two main components, namely the low-code-frequency (LCF) portion and the high-code-frequency (HCF) portion [41] as shown in Equation 3.30. It has been suggested that it is possible to characterize both the LCF and HCF with respect to output code. However, since this work is interested in temperature-sensitive modeling, I decided to characterize the LCF across temperature in addition to output code.

$$INL = LCF[k, T] + HCF[k] \tag{3.30}$$

As shown in Equation 3.31, this can be done using polynomial regression where the output code, k, is used as the regressor variable and each set of polynomial coefficients is indexed

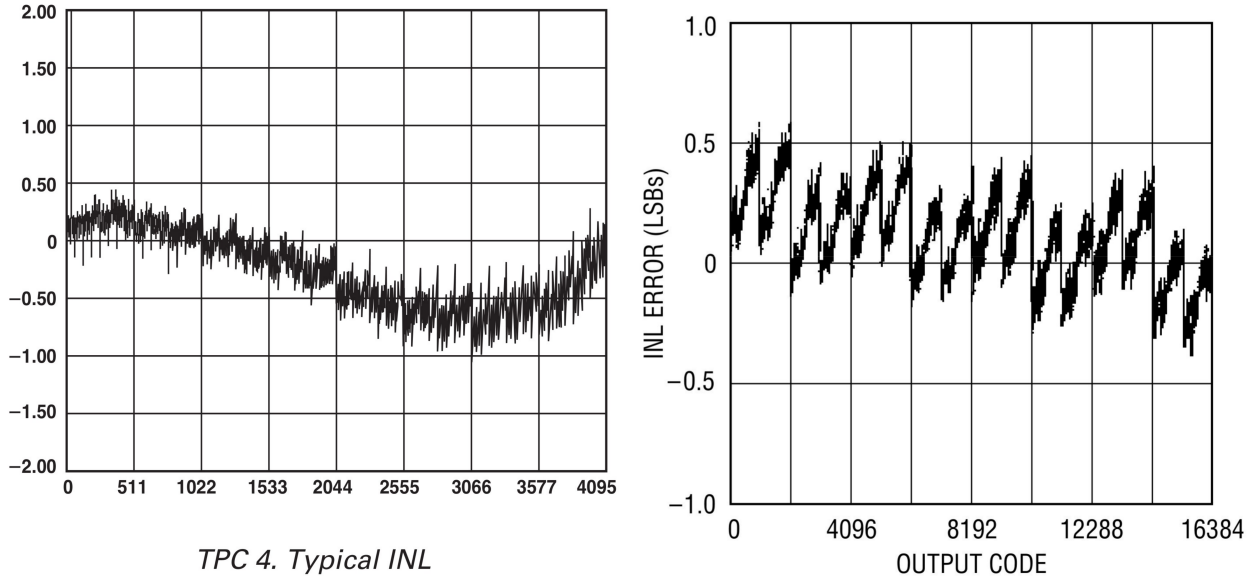


Figure 3.23: INL Curves for AD9225 and LTC1419

according to temperature to form the LCF.

$$LCF[k, T_i] = \alpha_{i,1} + \alpha_{i,2} \cdot k + \cdots + \alpha_{i,m} \cdot k^m \tag{3.31}$$

The first step is to reconstruct the INL curve from pictures typically given on datasheets as shown in Figure 3.23. Because the input image is binary (i.e. black and white), morphological operations will be necessary. The first step in processing is to obtain a mask to remove grid lines. Since these are only a few pixel wide at most, it is possible to identify them using structuring elements that are very long and thin. The next steps target removal of remaining spurious pixels like "islands" of one or more isolated pixels as well as broken "bridges" or pixels where one or two in series have been removed due to the gridline mask. Once grid mask artifacts have been removed, the resulting INL image is still "noisy" in that it is difficult to distinguish where exactly a particular INL value might lie on the vertical/voltage axis. This can be solved by considering each image column to be a sample from a Gaussian distribution where on pixels are projected onto the vertical axis. In this way, each column of pixels is expressed as a distribution of likely pixels and the most likely Gaussian describing the pixel positions can be used to estimate the curve. This process generates several curves, all of which maintain the overall shape and providing variation in the end result. The image

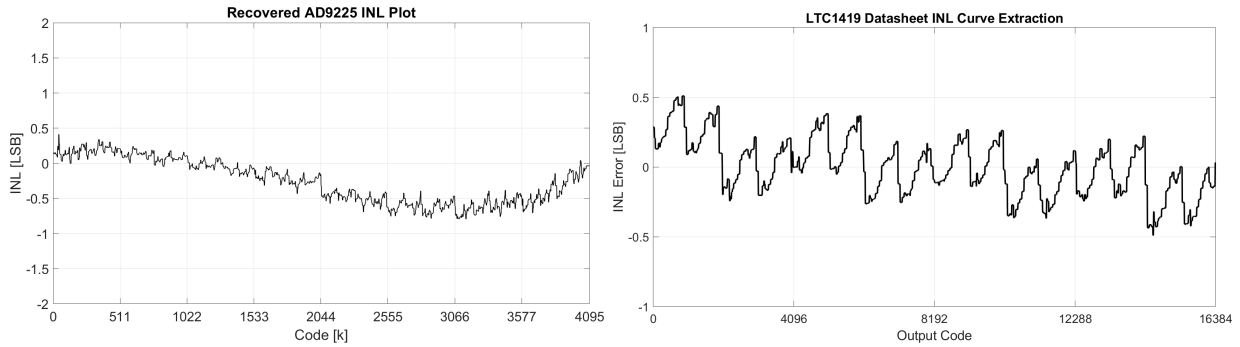


Figure 3.24: Reconstructed INL Curve from AD9225 and LTC1419 Datasheets

must then be resized in order to provide the proper number of values to reconstruct the INL curve. Recall that the x-axis refers indices of the decision levels while the y-axis refers to the voltage value of the INL for a particular decision level. After dealing with the problem of missing values using a median interpolation scheme, the image was resized using bicubic image warping.

3.3.3 Extraction of LCF

At this point, the INL curve describing nonlinearity in the ADC transfer function has been obtained either experimentally or from processing the datasheet and is shown in Figure 3.25. To provide a temperature predictive model, it is necessary to parameterize the transfer curve such that its evolution across temperature can be tracked, characterized, and hopefully predicted. Referring to literature [42], there are several ways to do this but I decided to use a polynomial regression combined with line segment fitting to characterize the overall shape and residue respectively. The low-code frequency portion refers to the overall shape of the INL curve, a smoothly varying polynomial with respect to the output codes that accounts for measured distortion. The highest power used to characterize this polynomial is reflected in the THD measurements and the highest harmonic obtained. For example, if a 4th order polynomial is used, the highest harmonic the model produces is $4f_{in}$. Polynomial regression is an example of linear regression since the coefficients can be placed into a vector where the polynomial described by the vector of coefficients forms a basis onto which the input data is projected. Equation 3.32-3.34 show the solution of this linear system to obtain the LCF

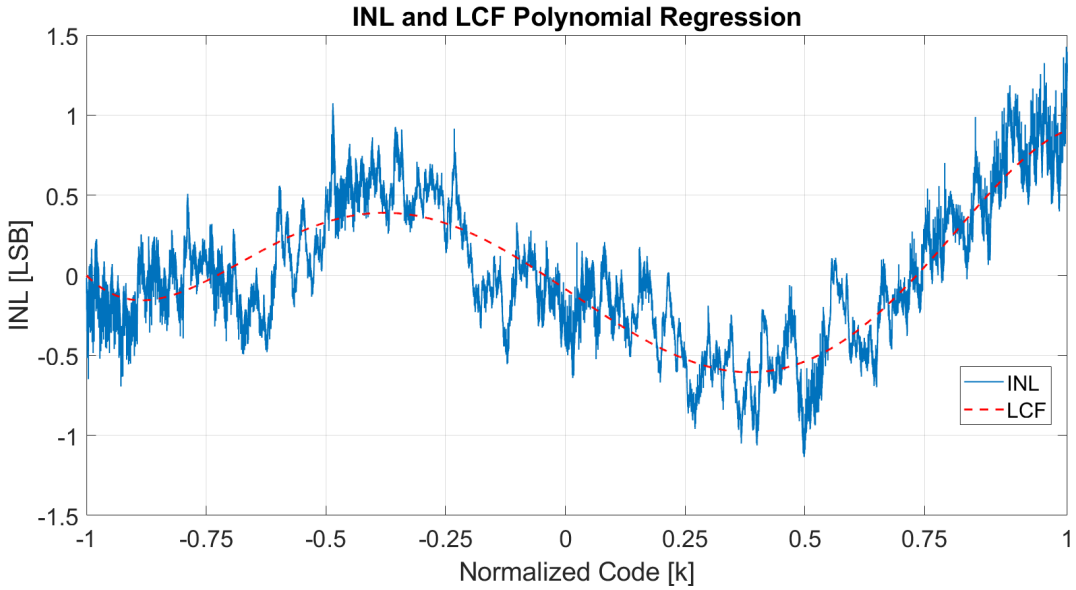


Figure 3.25: INL and LCF Polynomial Regression

coefficients.

$$\begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_n \end{bmatrix}_{n\times 1} = \begin{bmatrix} 1 & X_{11} & X_{12} & \dots & X_{1k} \\ 1 & X_{21} & X_{22} & \dots & X_{2k} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & X_{n1} & X_{n2} & \dots & X_{nk} \end{bmatrix}_{n\times k} \begin{bmatrix} \beta_0 \\ \beta_1 \\ \vdots \\ \beta_{k-1} \end{bmatrix}_{k\times 1} \tag{3.32}$$

$$\boldsymbol{Y}_{n\times 1} = \boldsymbol{X}_{n\times k}\boldsymbol{\beta}_{k\times 1} + \epsilon \tag{3.33}$$

$$\boldsymbol{\beta} = (X^T X)^{-1} XY \tag{3.34}$$

3.3.4 LCF Coefficient Trend Analysis

Once a polynomial regression has been performed over the INL data to extract the LCF portion, it is necessary to observe the trends present in each polynomial coefficient in order to identify any trends which could be used predictively to estimate another part's transfer curve across temperature. The aim is to capture the trend of the polynomial coefficients with respect to temperature and to then apply the same trend to another part or to a curve extracted from the datasheet. This would permit investigation of part to part variation as well as possibly capture universal trends in the ADC's performance. When doing so, there are several main questions that must be answered in order for the approach to be valid,

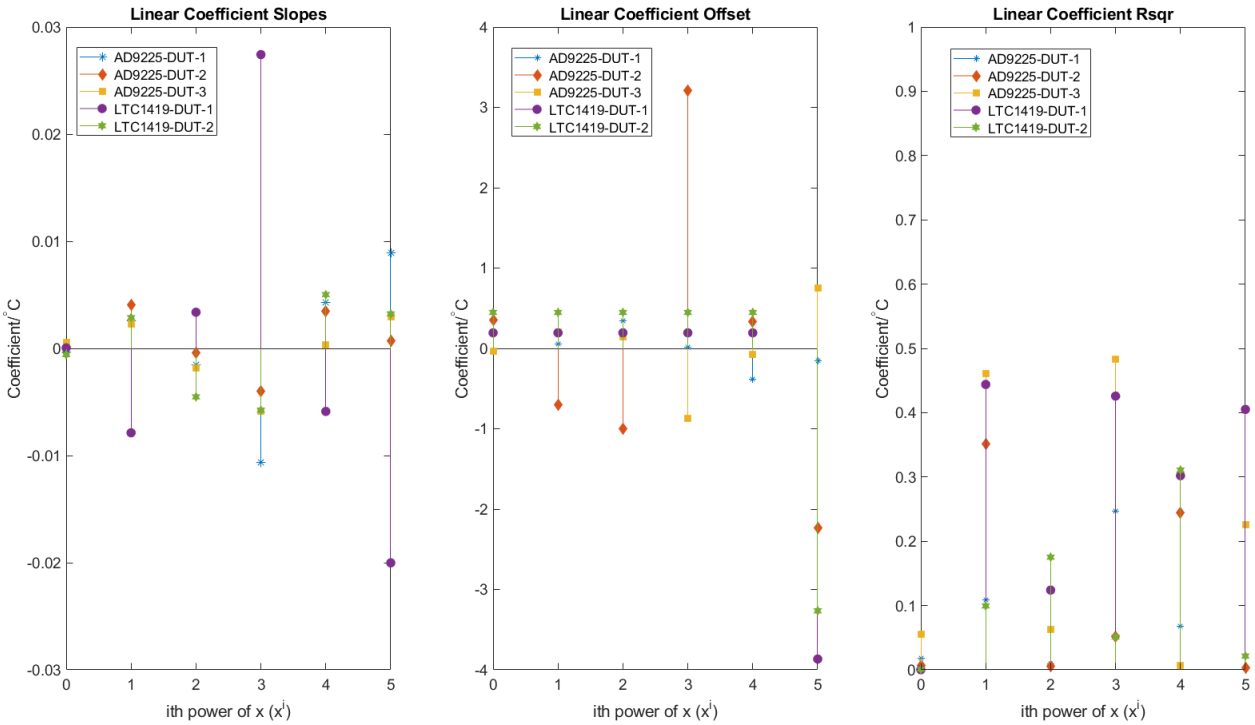


Figure 3.26: Slope, Offset and R^2 for LCF Coefficient Linear Fits

namely whether the reconstructed INL curves taken using the linear trends of individual coefficients show similarity with measured INL curves and if it is the case that observed variation in the INL curve is a prominent factor in overall ADC performance. To address these concerns, the polynomial coefficients were plotted with respect to temperature and a linear fit performed, regressing the LCF coefficients against temperature. Figure 3.26 shows the slopes, offsets, and R^2 values for both AD9225 and LTC1419 using several sets of INL data for each part. The most important parameters to observe are the slopes and R^2 values: as can be seen from the figure, the slopes of most coefficients from all DUTs are similar, except for LTC1419-DUT1. While it is unknown why this is the case, the model would be valid if there is universality in the temperature behavior of the constituent coefficients of the polynomial regression of the transfer curve. For most of the devices tested, this appears to be the case. However, by looking at the R^2 value, one can get an indication of whether the obtained fits are describing a meaningful trend with respect to temperature or whether the effect of temperature on the linear fit is small. Unfortunately, all the values in this regard are rather low, peaking around 0.5 indicating a weak linear trend. From observing

the coefficient vs temperature plots, this was caused by normal performance and weak trends across a large temperature range followed by sharp deviations near the minimum temperature tested, -180 °C.

3.3.5 HCF

Referring again to Equation 3.30, HCF represents the high-frequency portion of the INL curve that is the residue leftover from polynomial regression. When plotted, its waveform displays a periodicity in the code domain due to the recurrence of certain bit combinations internal to the converter. There are several approaches to characterizing a quasi-periodic waveform but perhaps the simplest approach is to iteratively fit linear segments across an interval as shown in Figure 3.27. Using Algorithm 3, an initial set of points are selected as vertices; next, a search space is established around the initial vertex location and the best-fit location identified by the choice which minimizes the norm of the square error of the HCF curve and fitted linear segment. The resulting segmented linear approximation is then added back to the LCF curve to generate an INL curve at each temperature. Because this waveform is very noisy, it is difficult for the algorithm to always find the best vertex points at which to start/stop line segments so a smoothing operation is first performed using a moving mean filter.

3.3.6 HCFn

Further accuracy describing the total INL curve is possible by considering the leftover from LCF and HCF portions to be composed of random noise termed $HCFn$. This remainder, as shown on Figure 3.28, is the mostly uncorrelated portion of the transfer curve described by a sampling from a Gaussian-distributed noise source.

3.3.7 INL Curve Testing

Sine testing was performed according to [21] which shows it is possible to obtain the transfer curve using either a static input, like a slow moving ramp signal, or a dynamic one like a sinusoidal input. After analyzing the output histogram to find the INL curve, the most likely

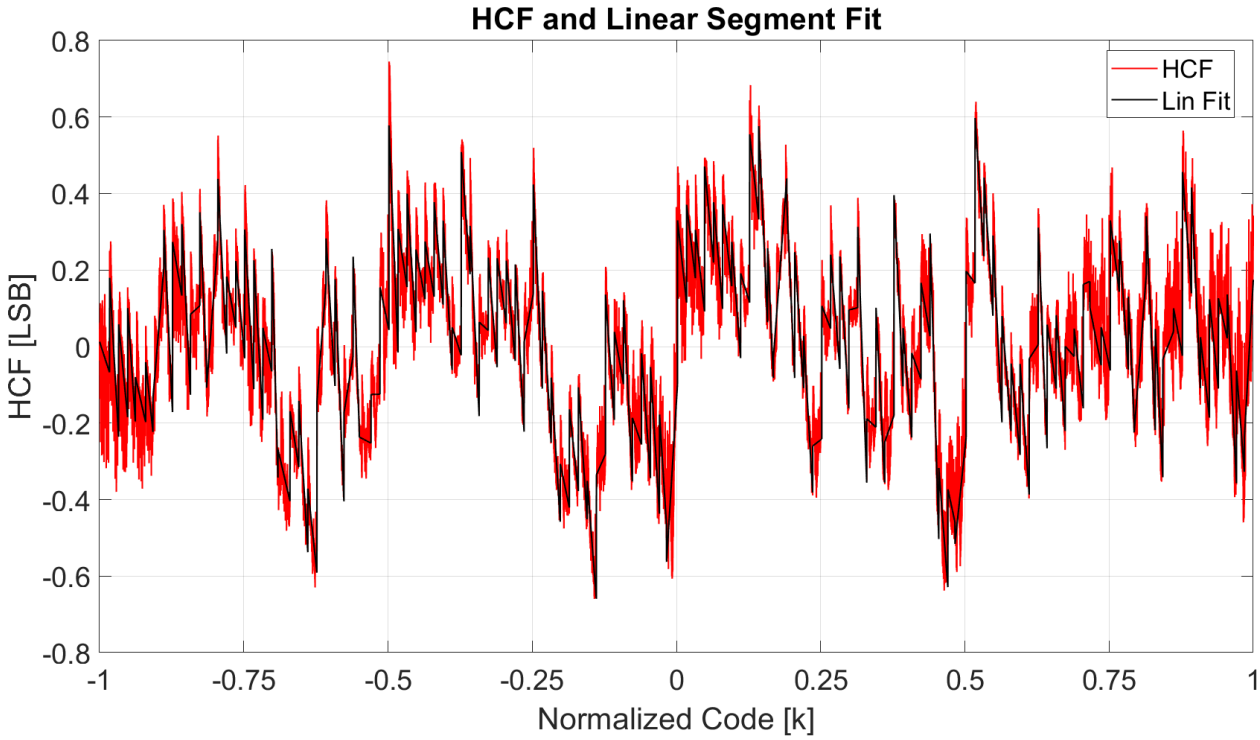


Figure 3.27: HCF and Best-fit Linear Segmentation

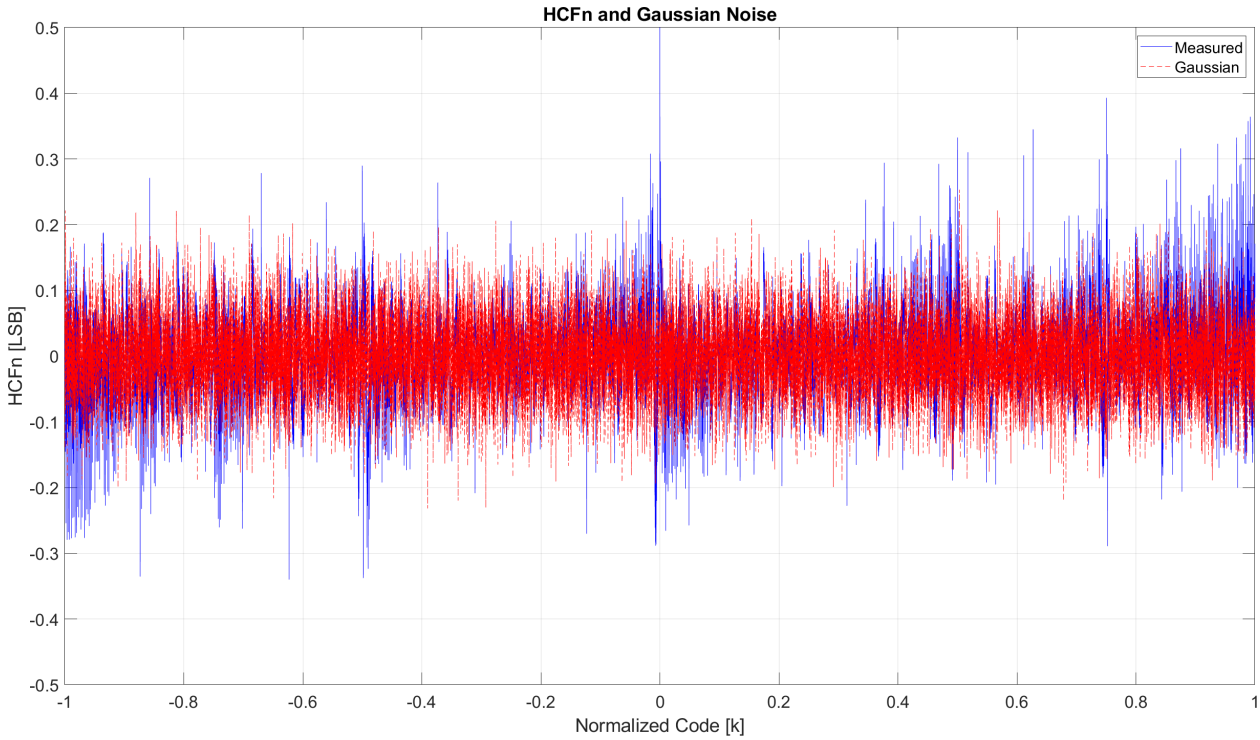


Figure 3.28: Residue from LCF and HCF (HCFn)

Result: Linear Coeffs for HCF
Load HCF INL data;
Initialize line segment length;
Initialize anchor point locations (left,right);
foreach *line segment* **do**
    Establish start,end points;
    Initialize error to zero;
    foreach *Point in search space* **do**
        Establish temporary start,end points;
        Establish linear range for fitting;
        Compute best-fit line segment over range;
        Compute and store error;
    end
    Find anchor point giving minimum error;
    Update actual anchor points;
end

Algorithm 3: Vertex Finding

transition locations are computed and then plotted to give the overall transfer characteristic. A best-fit line is removed, leaving the INL curve which describes the nonlinearities associated with the converter. Since polynomial regression is used to determine the smooth LCF portion of the INL, it is necessary to find the appropriate regression order that simultaneously minimizes the residue while keeping the number of parameters to a minimum. As in k-means clustering, it is helpful to plot the error metric, in this case the 2-norm of the residue, against the regression order or number of model coefficients. The best option is found at the "elbow", the point at which more coefficients do not improve model accuracy and fewer coefficients degrade performance. Referring to Figure 3.29 showing the residue error, it was decided that datasheet INL curve can be adequately approximated using 6 coefficients or a 5th order polynomial.

3D plots of the evolution of the LCF portion for AD9225 subject to ramp input in Figure 3.30 reveal a progressive change in the overall INL shape as the temperature decreases. The main question however is this: does this change in the nonlinearity portion of the ADC account for changes in observed performance? Later examination of converter performance indicates that there is a degree of distortion accounted for by the nonlinearity of the converter's transfer curve.

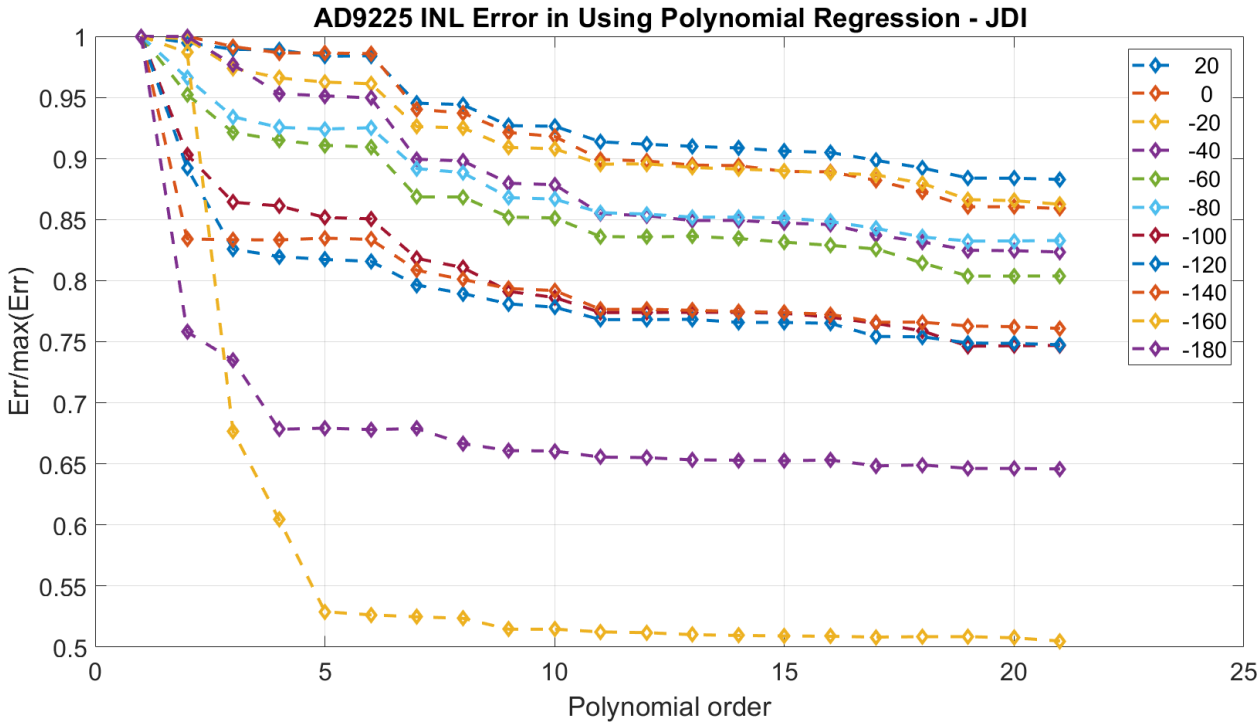


Figure 3.29: Error in Regression Residue vs Model Order

Figure 3.30: AD9225 INL Regression Using JDI Ramp Data

3.4 Summary

This chapter discussed the development of an initial generic ADC model using input-output measurements. Behavioral blocks modeling the nonideal factors in conversion were assembled to reproduce the measured characteristics of the converter while assuming an ideal quantization process. Specific aspects were discussed including jitter, reference voltage, and the track and hold amplifier block. Simulated data closely agreed with measured data regarding SNR and THD. Next, the development of a datasheet-based model was covered. Composed of two main components, this model used a THA section to model the analog capture of the input while incorporating relevant nonidealities. The transfer curve model section used extracted datasheet measurements to form the non-ideal quantization function of the device. Together, the two sections allow a user to obtain an ADC model extracted from datasheet information. When measured temperature trends are applied to the transfer function, it is possible to forecast the performance of a converter across temperature provided the reference voltage remains operational.

Chapter 4

Architecture Specific Behavioral ADC Models

In addition to generic models capturing ADC device behavior, it is also helpful to investigate architecture-specific models explicitly. Such models should replicate internal converter structure, hopefully providing a way to investigate non-idealities at the architecture level and their corresponding signatures at the input-output level.

4.1 MATLAB/SIMULINK Pipeline ADC Model

A classic treatment of the basic elements of converter design in given in [43] while an exhaustive treatment is covered in [44]. There exists a pipeline model including several non-ideal effects in [45], a brief overview in [46], in addition to an in-depth treatment in [47]. Pipeline bit decomposition with INL functions for bit groupings and stage transfer/residue functions are given in [48] but this approach was infeasible since our methodology precludes obtaining each individual stage's residue/transfer curve. For our purposes, each pipeline stage consists of a sub-ADC (sADC), DAC, multiplier, and subtraction function as shown in Figure 4.1. In practice, the functionality of the DAC, multiplier, and subtraction are incorporated into a single block, namely the multiplying DAC (MDAC). Behaviorally, however, it is possible to separate these functions. Errors and non-idealities associated with each block of the pipeline substage contributes towards the overall error but in

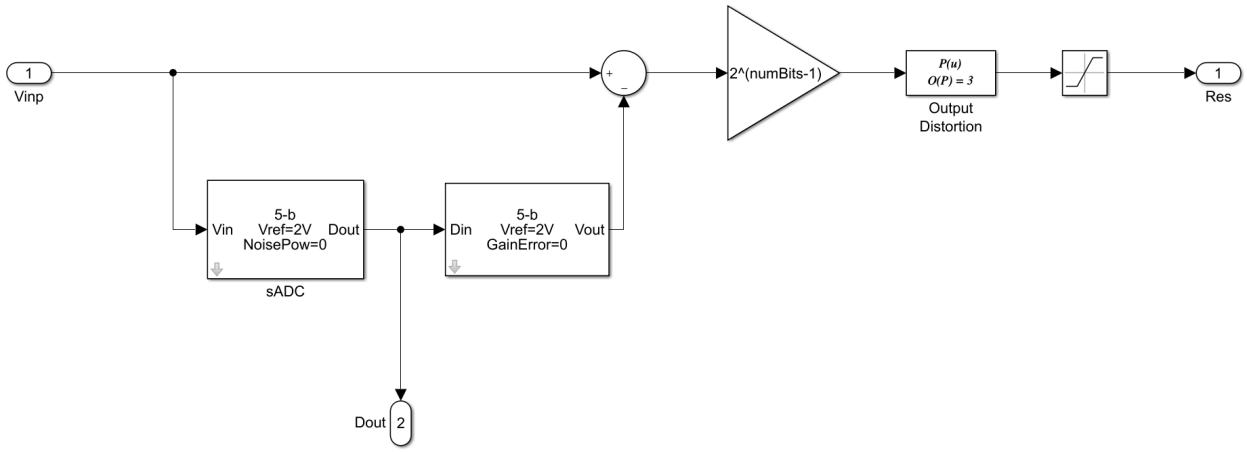


Figure 4.1: Block Diagram of Typical Pipeline Substage

varying amounts. A model incorporating such effects has the ability to reproduce observed errors, possibly allowing a user to pinpoint a specific block or error which may be limiting performance because there are design criteria which must be met in order to ensure a successful converter [49]. There are several sections of interest regarding the pipeline ADC, each of which must be behaviorally modeled to reproduce overall results but the INL remains a reliable indicator of where in the ADC errors occur.

4.1.1 Sub-ADC

The sub-ADC or sADC shown in Figure 4.2 performs quantization just like any other ADC but the main difference is that the pipeline architecture uses an additional redundant bit. This extra bit allows the converter to tolerate errors in fabrication that could potentially lead to a overranging or underranging. To provide redundancy, the input signal must be kept within half the full input range as one extra bit is used per stage in order to provide headroom for inevitable errors in fabrication and conversion and to prevent errors from cascading throughout the rest of the conversion. The main sources of error affecting the sADC stage are offset error, input-referred noise, and decision level error, all of which lead to deviations in the ideal decision levels. These effects can be lumped together into two random noise sources which are added to both the ideal decision levels and the input signal itself. The additional redundant bits normally provide coverage for slight deviations in decision levels as well as noise tolerance.

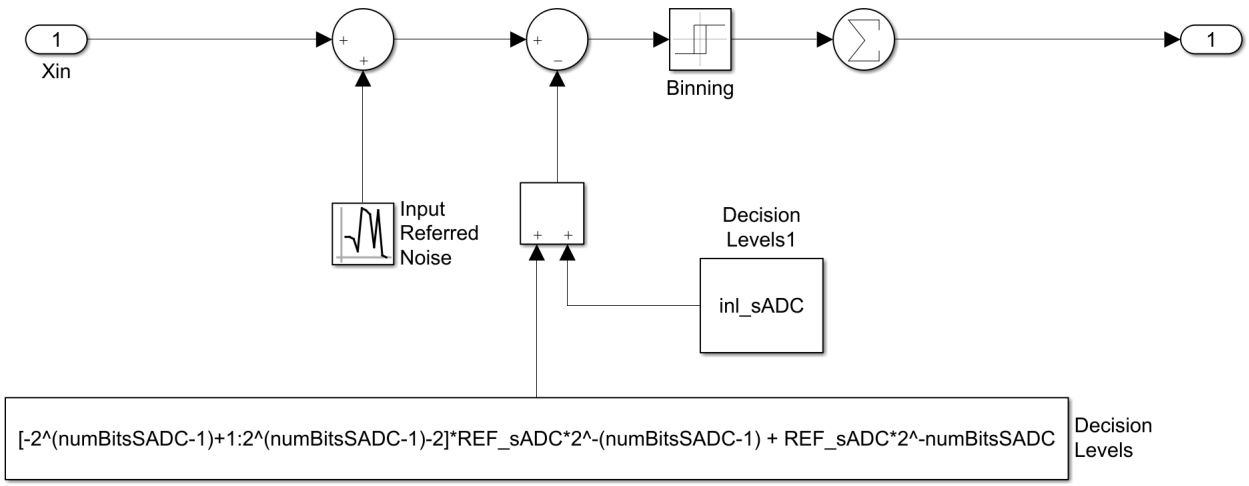


Figure 4.2: Implementation of sADC Stage

4.1.2 MDAC

The heart of each pipeline stage is the multiplying DAC (MDAC) which is typically a switched-capacitor network placed around a differential amplifier. There are several errors which can affect the result as shown in [50]. The first stage MDAC must be accurate to within the entire range of the overall converter since any error at this point would propagate throughout, fundamentally limiting resolution. The effects of errors can be broken up, however, as shown in Figure 4.3, into behavioral blocks, each of which is paramaterizable according to user-specified options. Doing so allows for parameter sweeps and even optimization according to experimental data. The sub-DAC (sDAC) block takes the output of the sub-ADC block and produces an analog voltage which is then subtracted from the held input to produce a residue error voltage. In the circuit topology, the overall closed-loop gain is ideally set by infinite open-loop gain but in practice, the DC gain of the MDAC is finite and furthermore varies with input signal level. This finite, signal-dependent DC gain introduces distortion into the sDAC output along with any internal noise that may be present. These factors are all incorporated into the behavioral model shown in Figure 4.3.

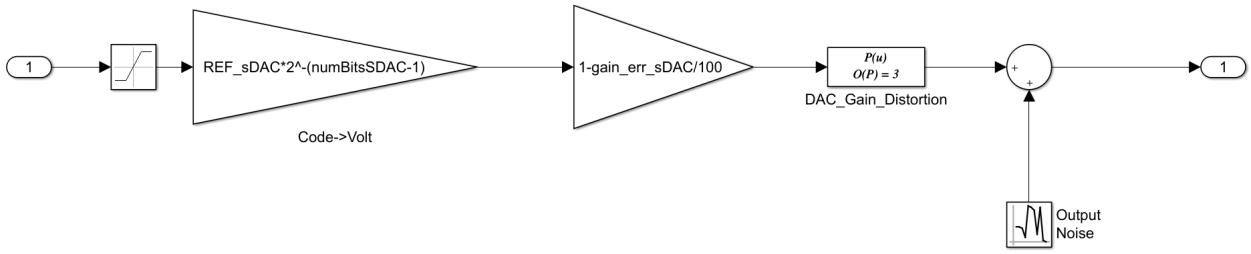


Figure 4.3: Stage DAC

4.2 MATLAB/SIMULINK SAR ADC Model

The SAR ADC is popular due to its low-power operation and balance of accuracy against speed while remaining conceptually simple. Because of its structural simplicity, the SAR can be built with relatively few blocks. For the model presented here, the main components include the track-and-hold amplifier, comparator, DAC, and digital logic [51, 52, 53].

4.2.1 Model Blocks

I used Simulink to model the mixed-signal environment as well as to execute the logic flow of the SAR algorithm. This decision dovetailed nicely with using MATLAB to implement a generic, black-box version focused on the INL since a predistortion function can be applied to model the effects of INL for a generic input.

Logic

SAR logic can be implemented in hardware using a linear feedback shift register (LFSR) [54] or in Simulink using a Stateflow diagram as shown in Figure 4.4. The basic flow is as follows: (1) sample and hold incoming input signal; (2) start conversion upon an internal clock's rising/falling edge; (3) reset the ADC output and zero the DAC; (4) for each bit, assert it high and observe the comparator output; (5) update the current bit and move onto the next bit. This process was assumed ideal as testing revealed no obvious errors in this process.

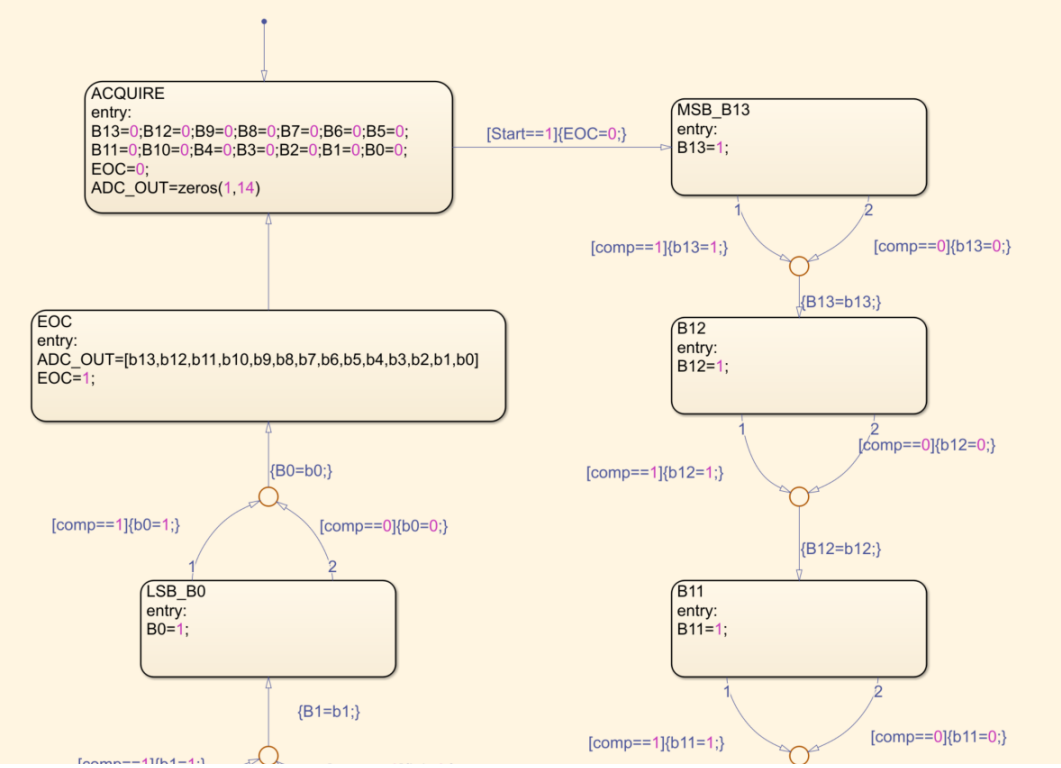


Figure 4.4: Simulink Stateflow Environment

4.2.2 THA

The THA model was built following a survey of existing approaches to amplifier performance in [55, 56, 57] and includes a first-order response, finite gain and bandwidth, and slew rate limiting. It is possible to adjust gain and cutoff frequency which introduce accuracy errors in the output but are generally not associated with distortion, assuming single-pole response.

4.2.3 Comparator

An important element of any standard SAR ADC is its comparator. The circuit-based implementation often consists of three stages: (1) pre-amplification to avoid metastability; (2) decision circuits with some amount of positive feedback to add robustness and avoid oscillation; and (3) output buffers to decouple loading effects from the decision circuit and improve transition time. The preamp is typically realized with a differential pair and active loads. Doing so reduces input-referred offset and helps mitigate kickback effects due to switching of elements inside the decision circuit. The decision circuit determines the

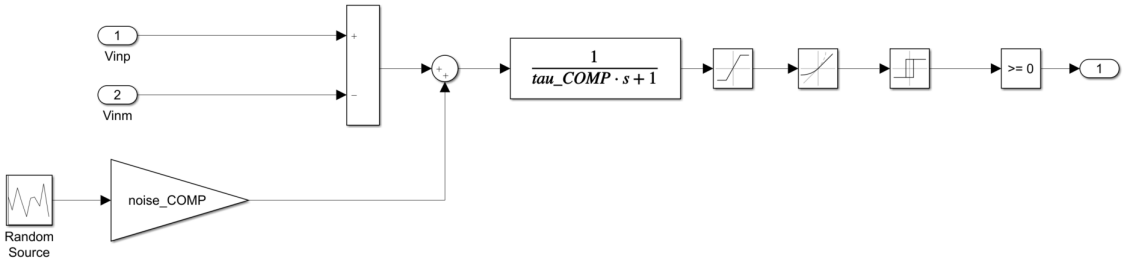


Figure 4.5: Simulink Comparator Model

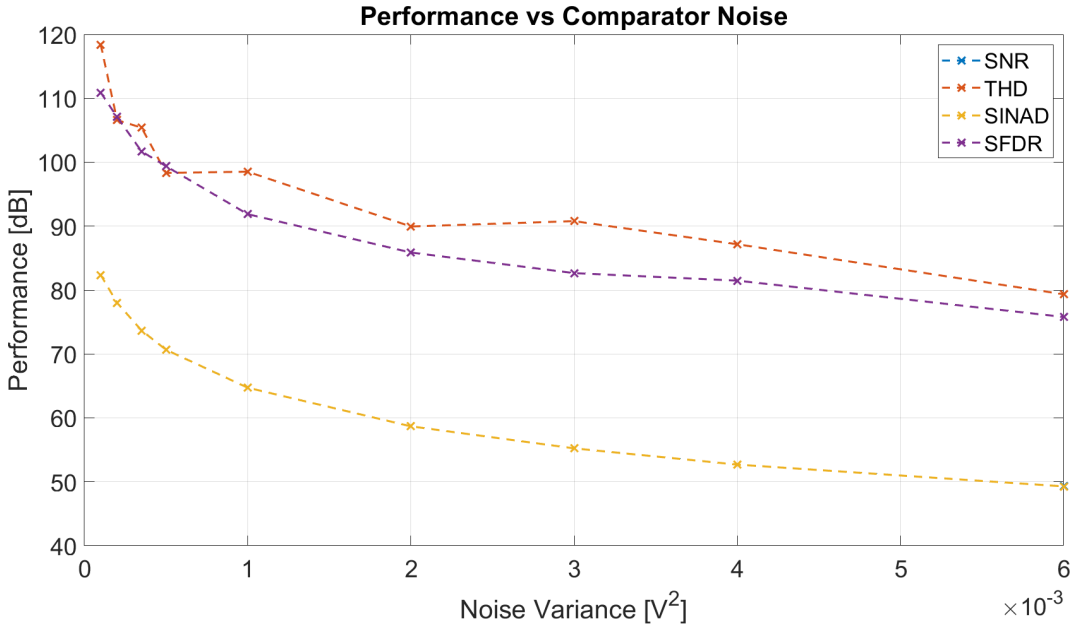


Figure 4.6: Effect of Comparator Noise on SAR Performance

resolution of the overall device as a comparator with less than one LSB of resolution does not have full precision. The output buffer takes the result of the decision circuit and drives the load to the required logic levels (e.g. 5, 3.3, 1.8 V) without incurring much slewing. The Simulink model of a comparator is shown in Figure 4.5 which includes noise coupled onto the input, a 1st order response, slew-rate limiting, saturation, and a relay to implement hysteresis. Hysteresis, usually implemented by a small amount of positive feedback, adds robustness to the comparator and prevents oscillations in the presence of noise around the decision point. Figure 4.6 demonstrates how the performance of a typical SAR ADC can be degraded due to input-referred noise coupling onto the comparator.

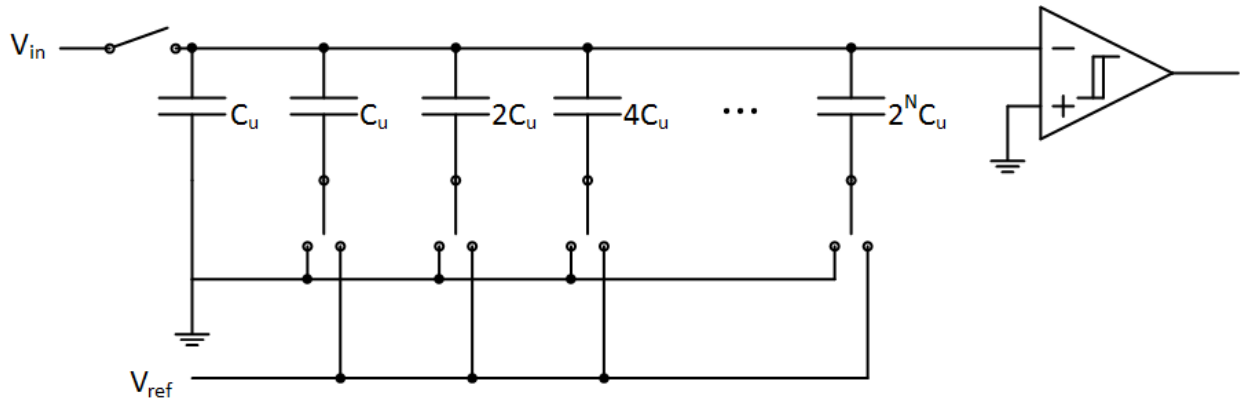


Figure 4.7: Binary Weighted CDAC Schematic

4.2.4 Capacitive DAC

The capacitive DAC (CDAC) principal of operation is to use capacitive voltage division between the held input voltage and a bank of capacitors to record and store bit decisions made by the comparator. There are two popular architectures of the CDAC, namely the binary weighted array and the split-capacitive array.

Binary Weighted Capacitive Array

The operation of the binary weighted array is relatively straightforward: referring to Figure 4.7, during the sampling period, the input is connected to the bank of capacitors which presents a parallel capacitance $C_{eq} = 2^N \cdot C_u$ where C_u is the unit capacitance. At the end of the sampling period, a charge corresponding to the input voltage is stored on the top plate of the capacitor array equal to $Q_{top-plate} = V_{in} \cdot 2^N \cdot C_u$. During the hold phase, the SAR logic activates the N bits in serial order starting at the MSB. Following each comparator decision, the bit in question is either kept high or set low, then the next bit tried. This process continues until all N bits have been tried and the output is latched to the output. A behavioral CDAC model using a binary weighted capacitor array is shown in Figure 4.8 and incorporates several non-ideal effects including capacitor mismatch, parasitic capacitance at the common node of the capacitor bank, and noise coupled onto the capacitors. The mismatch can be randomly generated using a Gaussian/normal distribution or specified as a particular percentage value of the unit capacitance C_u allowing one to determine the

acceptable mismatch for a given resolution. The parasitic capacitance can be modeled either as a constant, which adds a signal-independent offset, or as a polynomial function of the previous output voltage which adds nonlinearity. According to capacitive voltage division, the CDAC output due to a particular bit combination and reference voltage is given by Equation 4.1 where D_i is 0 or 1 depending on the SAR logic and $C_i = 2^{N-i} \cdot C_u$.

$$\begin{aligned} C_{DAC} &= \Big(\frac{C_{on}}{C_{tot} + C_p}\Big) V_{ref} \\ &= \Big(\frac{\sum_i^N D_i \cdot C_i}{C_{tot} + C_p}\Big) V_{ref} \end{aligned} \tag{4.1}$$

Split Capacitor Array

The binary-weighted capacitor array suffers from several problems as overall resolution increases; in particular, the total capacitance and switching power required in a binary weighted array can become unmanageable. To illustrate, a 12-bit ADC with unit capacitance $C_u = 0.5$ pF would have a total capacitance of $2^{12} \cdot C_u = 2048$ pF with the largest single capacitor being 1024 pF. In other words, a linear increase in resolution leads to an exponential increases in capacitor area and dynamic power consumption. A split-DAC arrangement, however, breaks apart the binary wighted array into two or more sections, saving critical area and lowering the overall capacitance which reduces power consumption during charging and discharging. Figure 4.9 shows a typical arrangement of an LSB array for the bottom L bits, and an MSB array for the top M bits where $N = M + L$. In the case of a two-segment split array, the attenuation capacitor is

$$C_a = \frac{C_{LSB}}{C_{MSB}} = \frac{2^L}{2^M} = \frac{2^L}{2^L - 1} = \frac{128}{127} \tag{4.2}$$

for a 14-bit device. Referring to the simplified schematic of a split capacitor array on Figure 4.10, the equations describing the DAC output for a given bit combination requires solving, in the case of a two-section array, a set of two linear equations. Denoting the relevant nodes as V_A and V_B, one arrives at two equations from charge conservation

$$Q_A = -Q_B \tag{4.3}$$

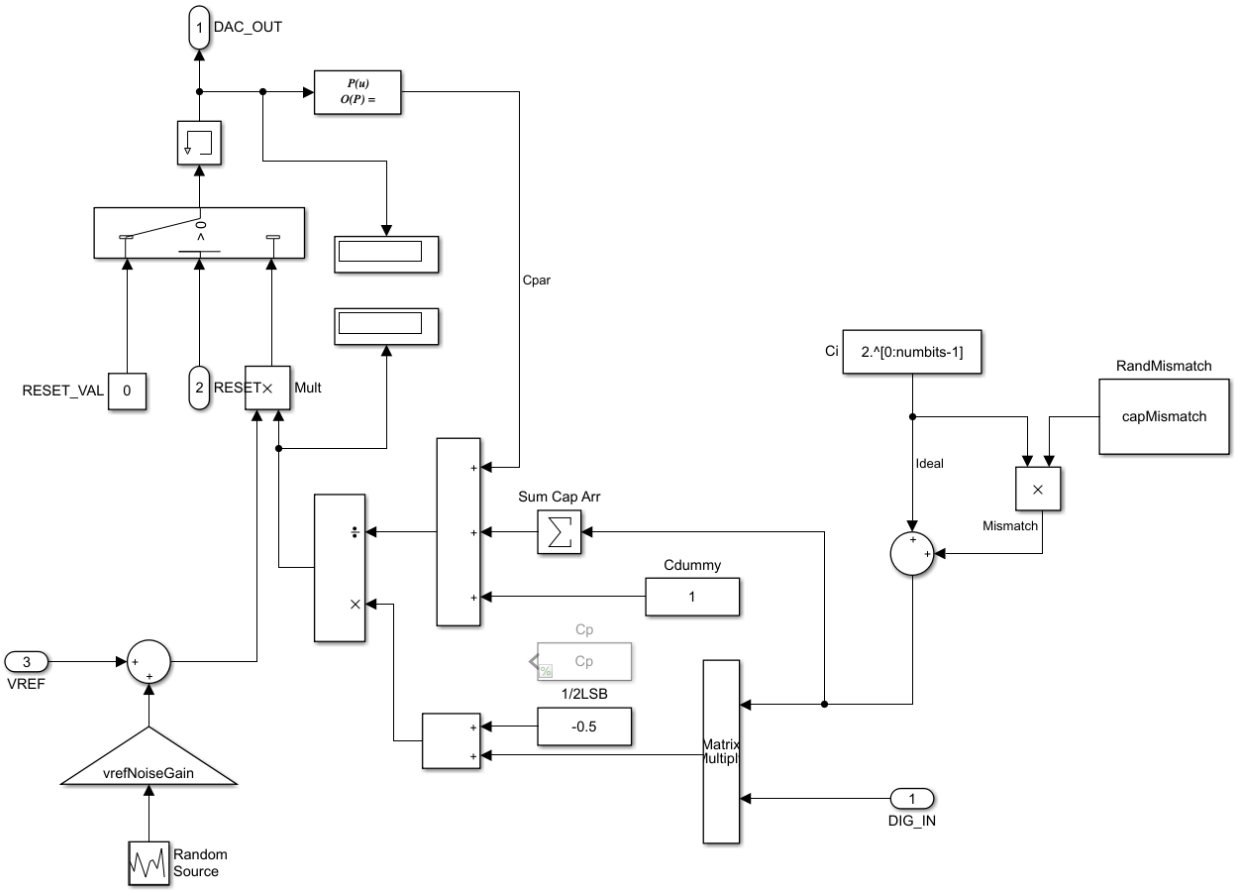


Figure 4.8: Binary Weighted Behavioral CDAC

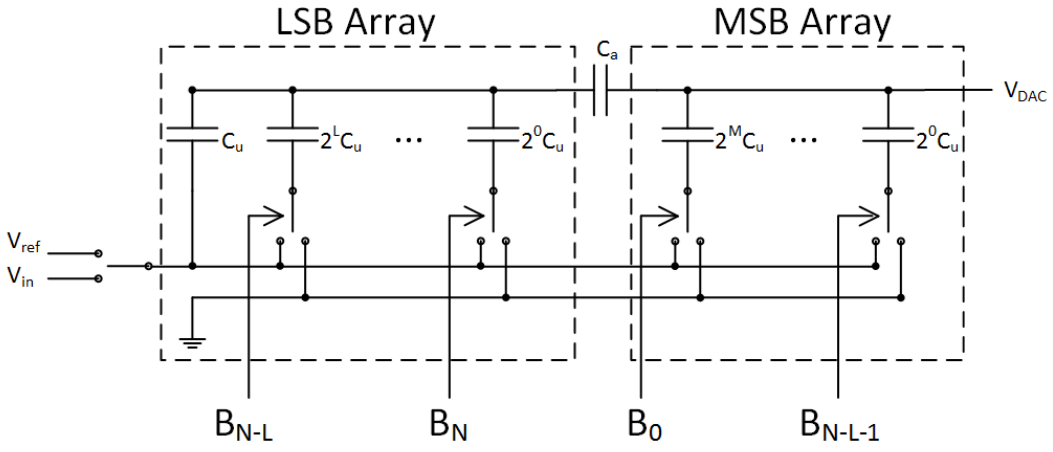


Figure 4.9: Typical Split Capacitor Array

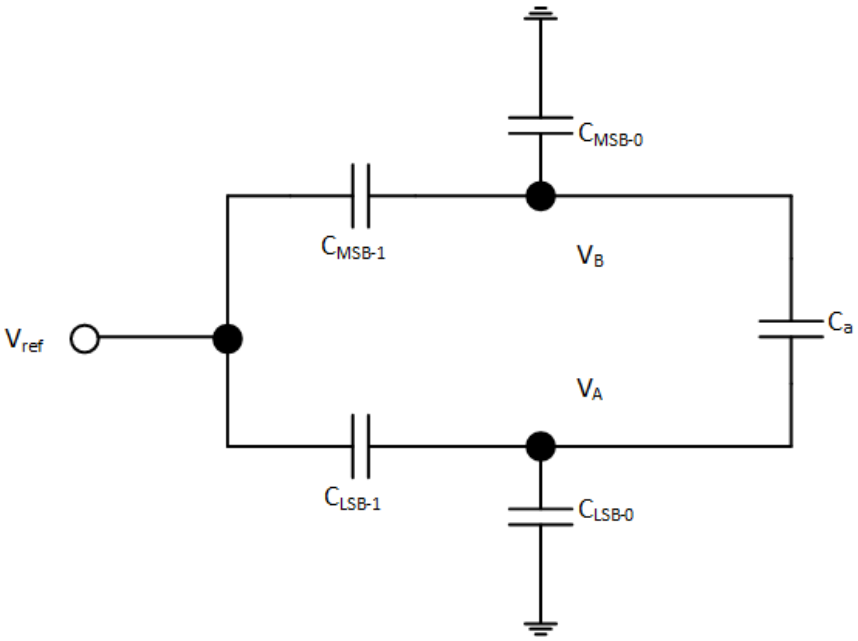


Figure 4.10: Split Capacitor DAC Equivalent Circuit

$$Q_{Vref} = -Q_A = -Q_B = 0 \tag{4.4}$$

$$Q_A = C_{LSB-0}V_A + C_{LSB-1}(V_A - V_{ref}) + C_a(V_A - V_B) = 0 \tag{4.5}$$

$$Q_B = C_{MSB-0}V_B + C_{MSB-1}(V_B - V_{ref}) + C_a(V_B - V_A) = 0 \tag{4.6}$$

where C_{LSB-1} and C_{MSB-1} refer to the equivalent capacitance of the 'on' capacitors, and C_{LSB-0} and C_{MSB-0} to the 'off' capacitor, respectively. Rewriting in matrix form and solving yields

$$\begin{bmatrix} V_{ref}C_{LSB-1} \\ V_{ref}C_{MSB-1} \end{bmatrix} = \begin{bmatrix} C_{LSB} + C_a & -C_a \\ -C_a & C_{MSB} + C_a \end{bmatrix} \begin{bmatrix} V_A \\ V_B \end{bmatrix} \tag{4.7}$$

$$V_A = V_{ref} \times \frac{C_aC_{MSB-1} + C_{LSB-1}(C_{MSB} + C_a)}{C_{LSB}(C_{MSB} + C_a) + C_aC_{MSB}} \tag{4.8}$$

$$V_B = V_{ref} \times \frac{C_{LSB}C_{MSB-1} + C_a(C_{MSB-1} + C_{LSB-1})}{C_{LSB}(C_{MSB} + C_a) + C_aC_{MSB}} \tag{4.9}$$

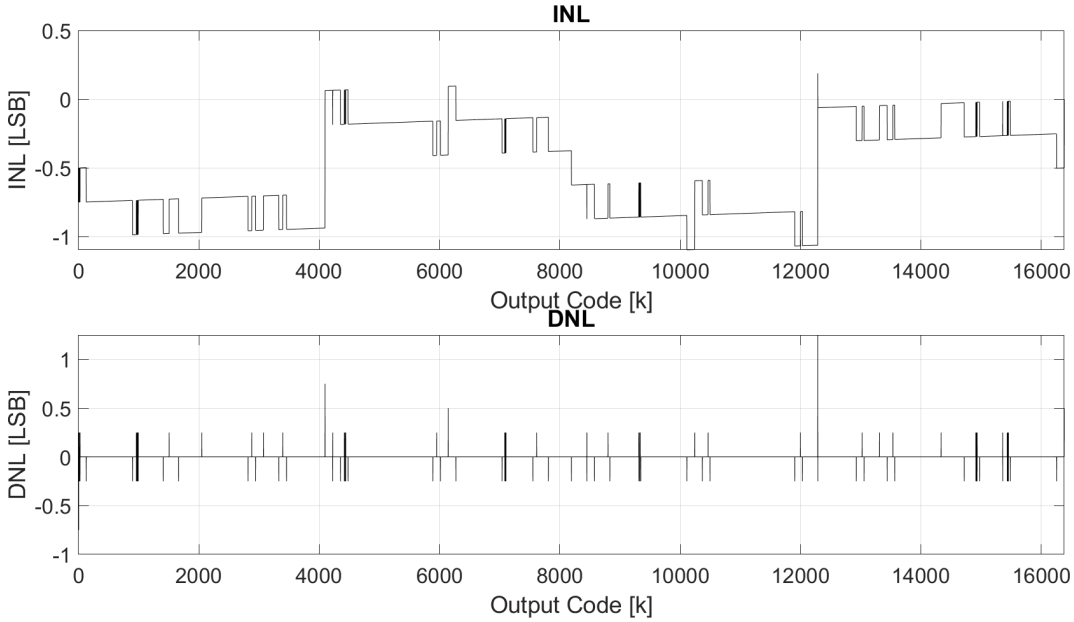


Figure 4.11: INL and DNL Due to Capacitor Mismatch

where the DAC output voltage is given by V_B. For a 12-bit ADC with $L = M = 6$, the total capacitance is given by $2^6 + 2^6 - 1 + \frac{2^6}{2^6-1} = 128\frac{1}{63} \cdot C_u$ which is only 3.125 % of the total capacitance for a binary array and represents serious area and power savings. The importance of capacitor mismatch on overall converter linearity is shown in Figure 4.11

DAC Settling Time

The main timing limitation which determines the shortest conversion time of a SAR ADC is the settling time of the DAC, especially around major transitions which involve charging/discharging large capacitances. The worst case condition is a step input from 0 to V_{FS} or code 0 to 2^N. Assuming a 1st order response for an RC network created by a transistor switch on-resistance in series with a DAC capacitor, the error in the output due to a step input is $e(t) = e^{-t/\tau}$. By taking the output only when the DAC has settled to within 1/2 LSB, it is possible to estimate the number of time constants required to achieve a given resolution. The LTC1419 has $N = 14$ with $F_s = 800$ kSPS and $T_s = 1.25$ µs. There are 14 conversions which need to be performed within T_s and additional clock cycles are necessary for initialization and latching the output. Assuming 16 cycles gives the settling period $T_{settle} = \frac{1.25}{16}$ µs = 78.125 ns for a single conversion to settle. Per Table 4.1, this is equal

Table 4.1: Table of DAC Settling Time

Resolution (N)	# of time constants (t/τ)
10	7.62
12	9.01
14	10.40
16	11.78

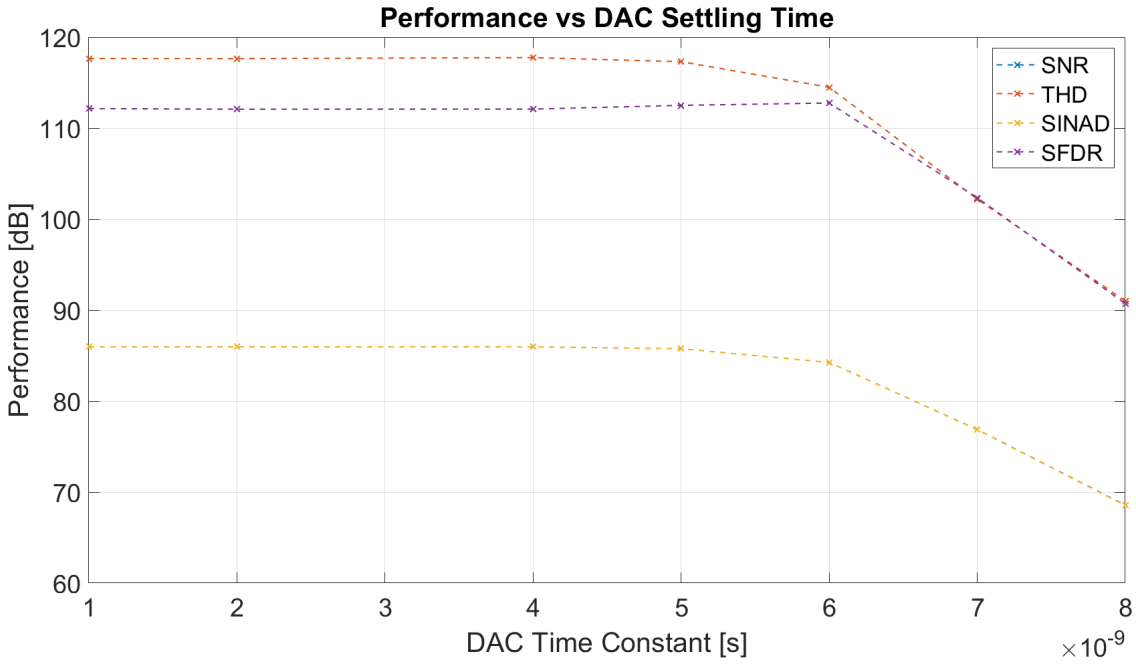


Figure 4.12: SAR Sine Parameters vs DAC Settling Time

to approximately 10.4 time constants giving the overall time constant $\tau_{LTC1419} = 7.512$ ns. As is often the case, a designer must overdesign by aiming for a much lower settling time than is theoretically allowed in order to ensure the proper device resolution. Figure 4.12 shows the impact of settling time on the converter's overall performance. It can be seen that using the maximum allowable settling time results in about 14 dB degradation of SNR with an equivalent resolution drop equal to about 2 bits.

4.3 Summary

This section reviewed the design of architectural specific models for a pipeline and SAR ADC. While attention was given to the two particular devices tested, the models are flexible

enough to be applied to different instances of each architecture while still incorporating relevant blocks where performance impact of nonidealities is accounted for. The pipeline model includes blocks implementing the behavior of substages containing a stage-ADC and stage-DAC, as well as ideal digital recombination of the redundant stage output bits. Next, a SAR ADC model was presented including a THA front end, execution of digital logic, comparator, and behavioral DAC for binary weighted or split capacitor array. The DAC can take into account capacitor mismatch, non-ideal references, and the finite settling time. Although each model was developed for a particular ADC, it is possible to modify them in the appropriate ways so as to model any particular pipeline or SAR ADC.

Chapter 5

Experimental Results

This section will focus on how well the datasheet-based predictive model performance relates to measured part to part variation, as well as how well such applied temperature trends can be applied to another part. Such a comparison will test the universality of the model and trends developed.

5.1 Test Board

Experimental measurements of various converters was a crucial step not only in building the models but also in verifying the models' accuracy. Meeting design requirements for accurately testing 12 and 14-bit ADCs was challenging but became more achievable through various board iterations. The details of each test board will be briefly discussed below before presenting the results of testing.

5.1.1 AD9225 UT Test Board

By the end of the project, the in-house board had undergone significant revision reflecting our increased understanding of what is necessary to achieve good performance at cryogenic temperatures using commercial components. Figure 5.1 demonstrates the final board design for testing the AD9225. Two inputs are routed to the device which is soldered to an adapter board, situated atop a socket for easy insertion and removal, allowing for either

fully differential if both inputs are 180° out of phase or single-ended testing if one input is set to a DC level. The DUT's internally generated reference voltage is buffered by an op-amp, the OPA2356, to a test pin for easy measurement. The clock signal is routed to an inverter for buffering, producing a clean clock edge for conversion timing. The 12 digital output channels of the AD9225 are routed to a digital buffer, then onto pin headers for measurement by a logic analyzer. The board's performance characteristics are demonstrated in Figures 5.2, 5.3 and 5.4. Sinusoidal testing reveals THD comparable to datasheet values but with a slightly degraded SNR which may be due to the lack of an input filter. The INL and DNL of the converter are well within nominal ranges, indicating all codes present. Finally, the board noise, measured with both inputs grounded, yields an average code value of 2043 ($0111-1111-1011_2$), only 5 away from the ideal value of 2048 ($1000-0000-0000_2$). Furthermore, the input-referred to the board has a standard deviation of only 0.33 LSBs, indicating that there is minor fluctuation affecting only the lowest bit. Such results give confidence in the data collected to form the model.

5.1.2 LTC1419 Modified Evaluation Board

The LTC1419 was unproven in cold, having been documented to have issues with the reference voltage past -60 °C [26]. Because of this, our initial investigations consisted mainly of using the manufacturer-provided evaluation board and modifying it where appropriate and necessary. Modifications included stripping off the on-board voltage regulators and supplying power directly from an external power supply, as well as bypassing the on-chap reference voltage through the REFCOM pin.

5.2 Predictive Datasheet ADC Model Comparison

The universal ADC model developed in this work consists of a front-end THA and transfer curve. The THA parameters, where applicable, include temperature sensitivity as in the case of thermal noise. The overall shape of the transfer curve, as determined by polynomial regression, has temperature dependencies as well. The temperature trends of the constituent polynomial coefficients can be used to estimate the transfer curve given a measurement

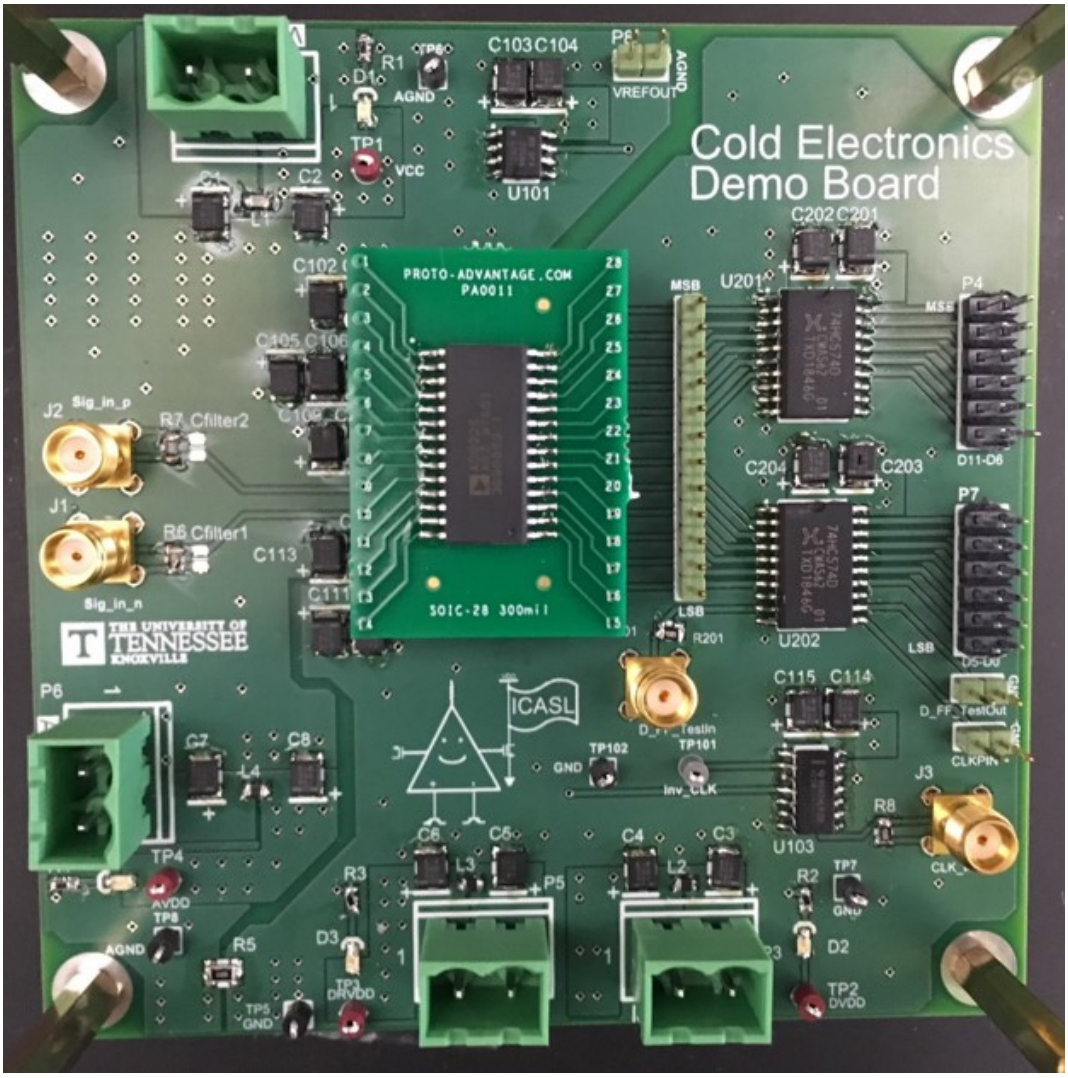


Figure 5.1: Final Board Top View

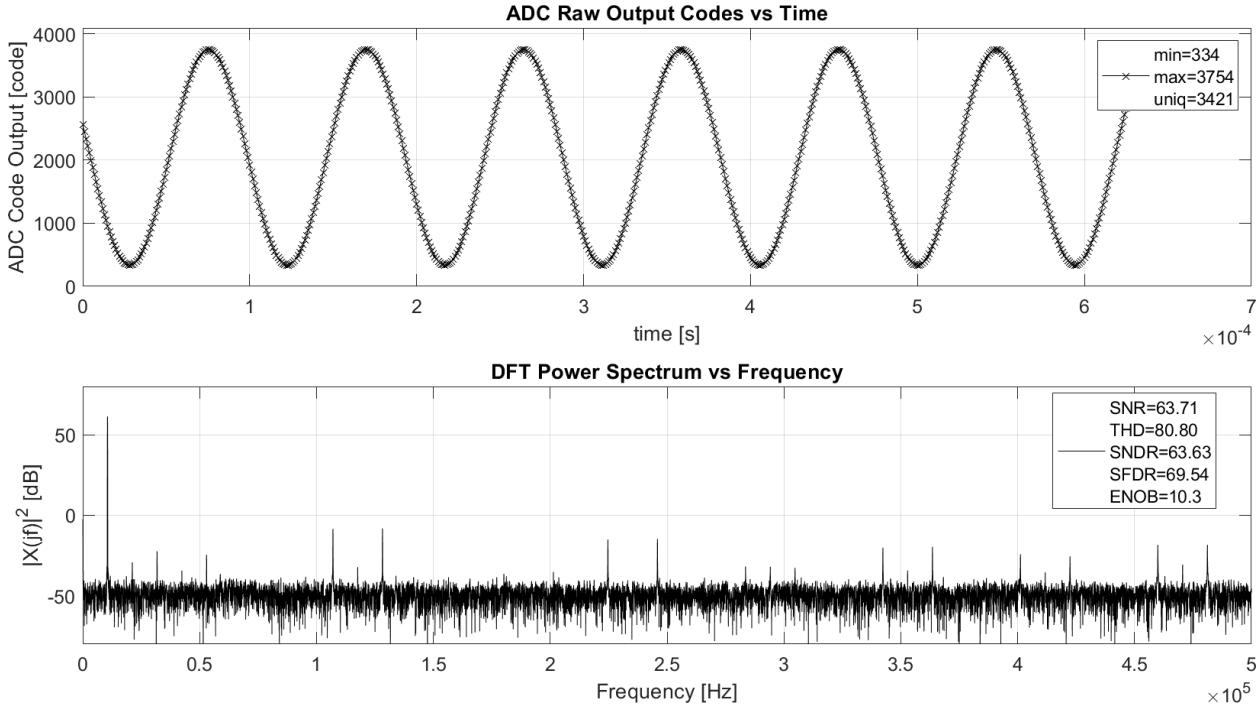


Figure 5.2: Final AD9225 Sine Results

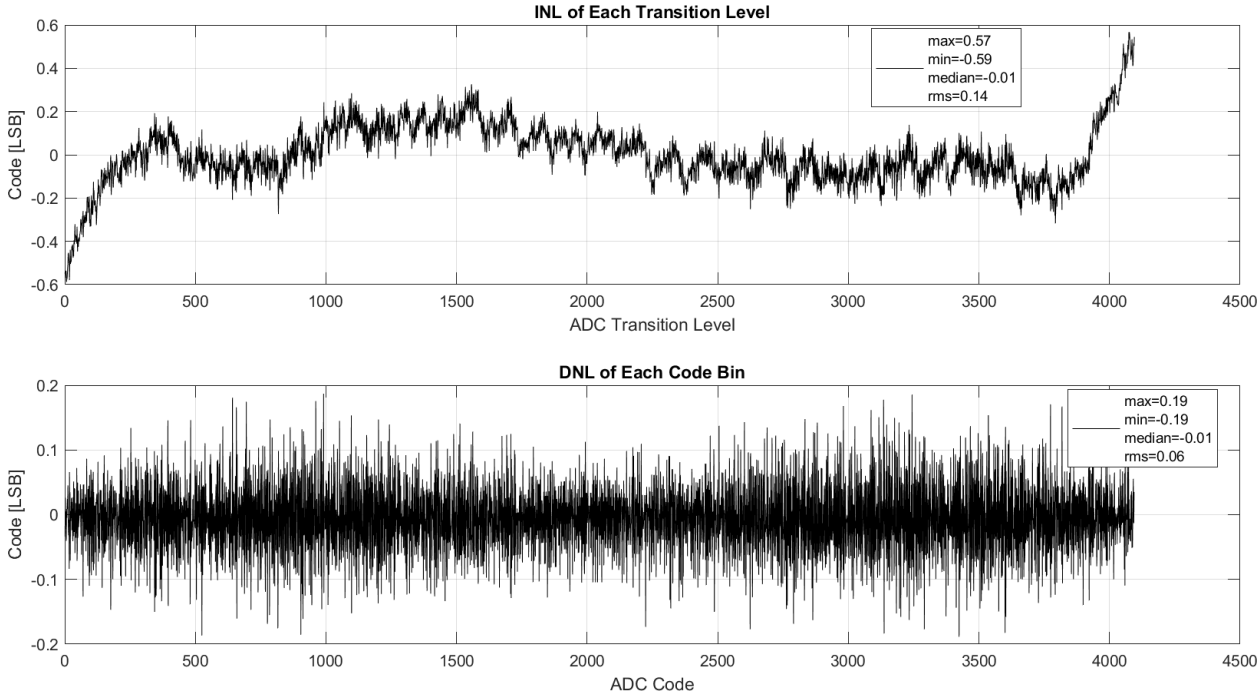


Figure 5.3: Final AD9225 INL/DNL Results

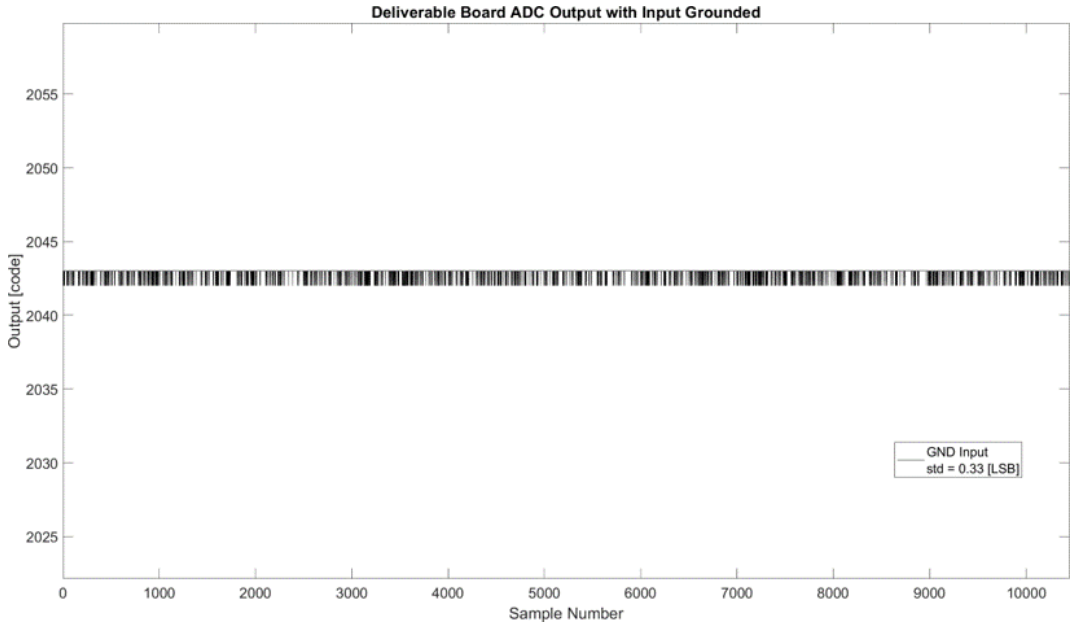


Figure 5.4: Final AD9225 Board Noise Results

at a particular temperature. The input-referred noise, normalized by the converter's ideal quantization noise level, also has been observed to have a trend which can be used to estimate the input-referred noise at a particular temperature. Taken together, these components use aggregate trends in each of the aforementioned components to construct a universal ADC model that can be applied regardless of architecture. The correspondence of the models developed to measured performance are discussed below.

5.2.1 Universal ADC Model Part to Part Variation

In order to estimate part to part variation of a particular converter, it is necessary to average the temperature characteristics of several DUTs of the same part and incorporate their aggregate trend into the model. The trends regarding INL shape coefficients and normalized input-referred noise will be used in reconstructing converter performance. The results of this process are shown in Figures 5.5, 5.7, 5.9, and 5.11. Shown in Figures 5.6, 5.8, 5.10, and 5.12 are the percent differences between the model simulation and measured part performance for each DUT.

The three AD9225 devices are shown in red, green, and blue while the universal model results are shown in black. Firstly, all parts display performance within a particular band,

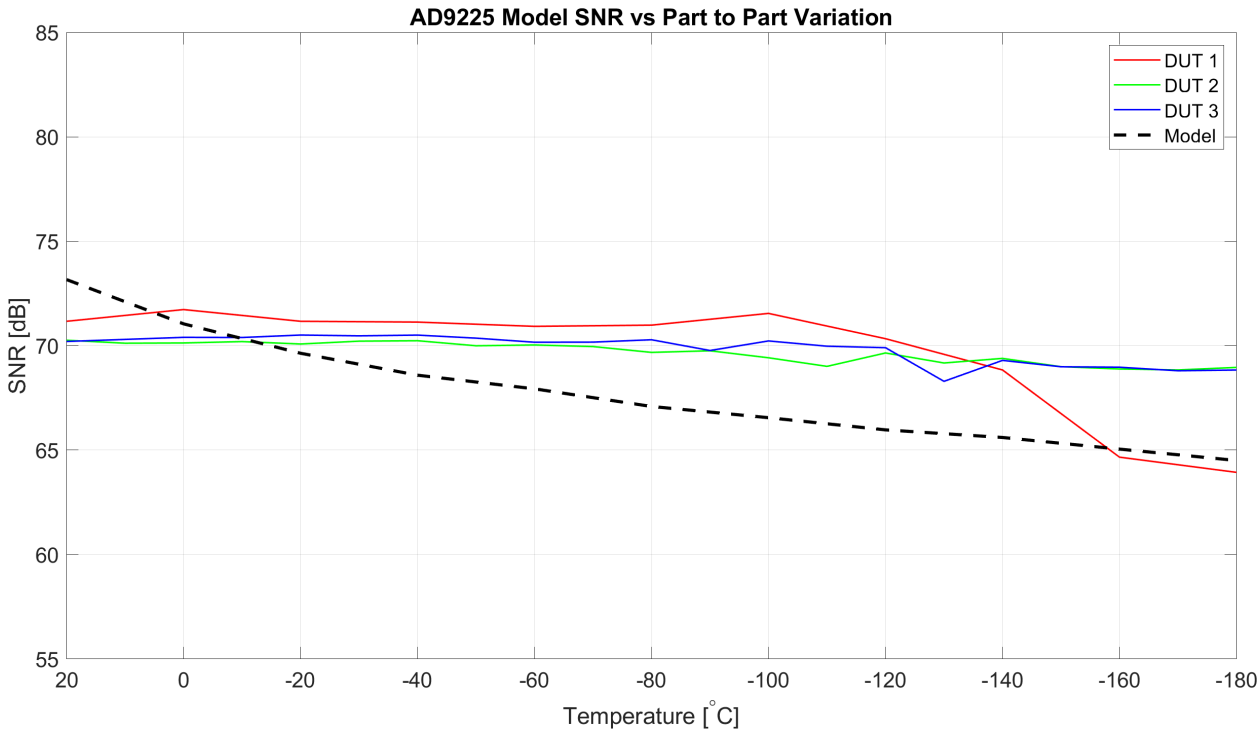


Figure 5.5: SNR Part to Part Variation

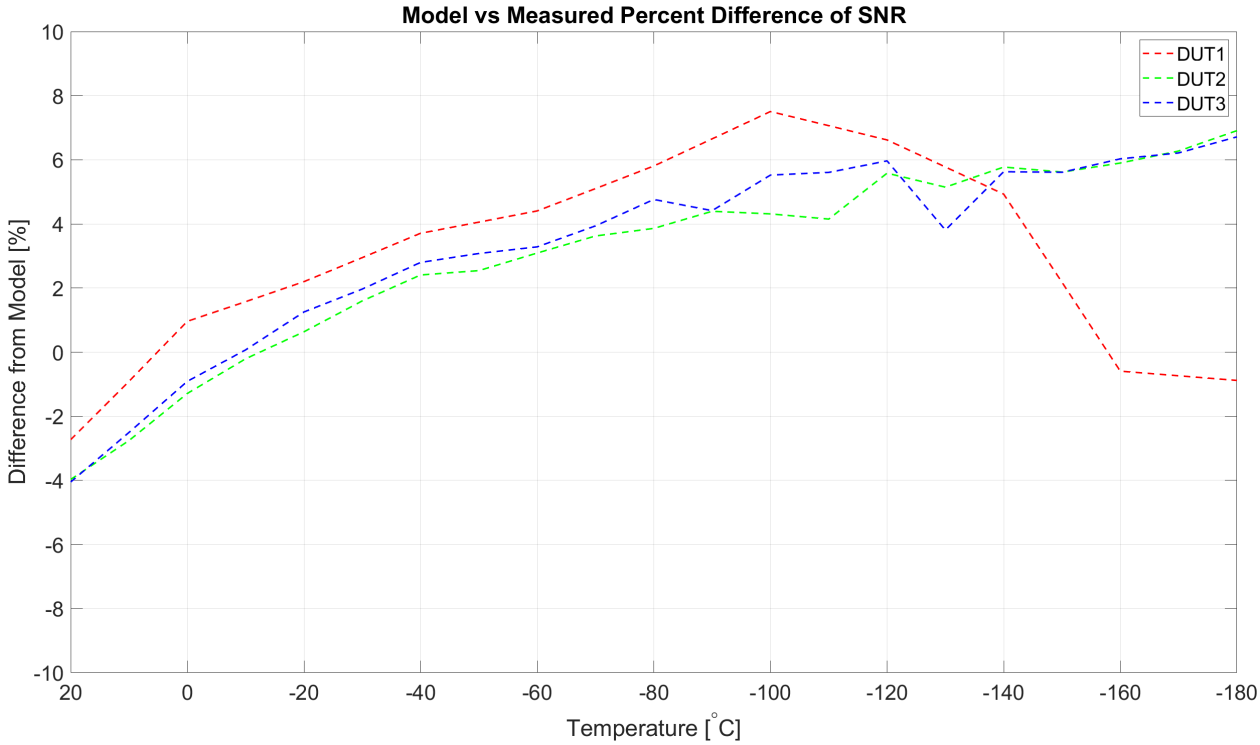


Figure 5.6: SNR Model Percent Difference

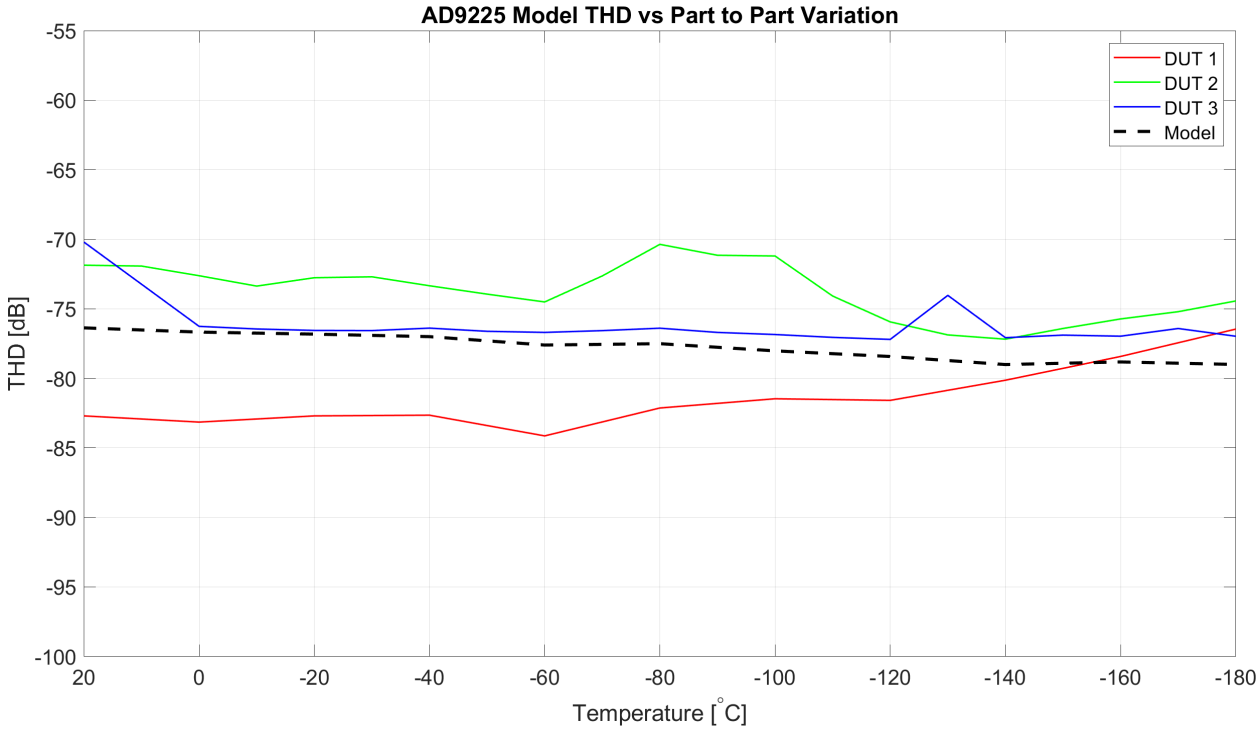


Figure 5.7: THD Part to Part Variation

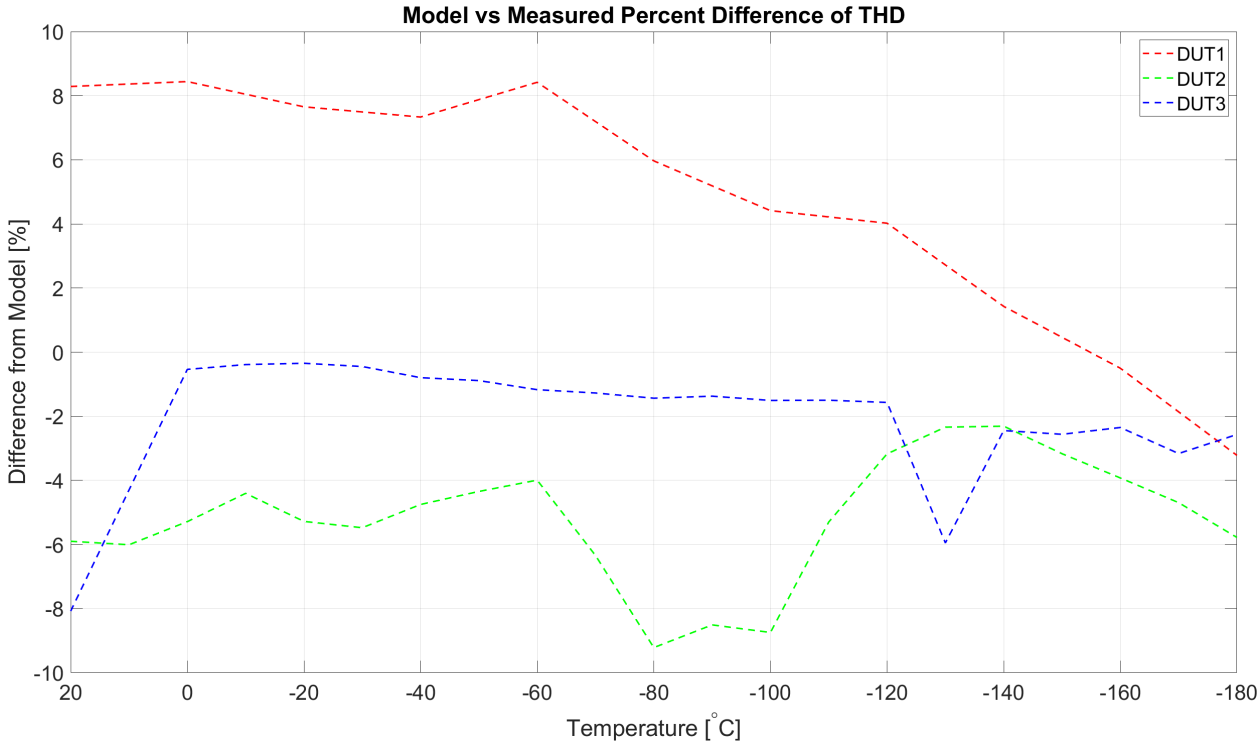


Figure 5.8: THD Model Percent Difference

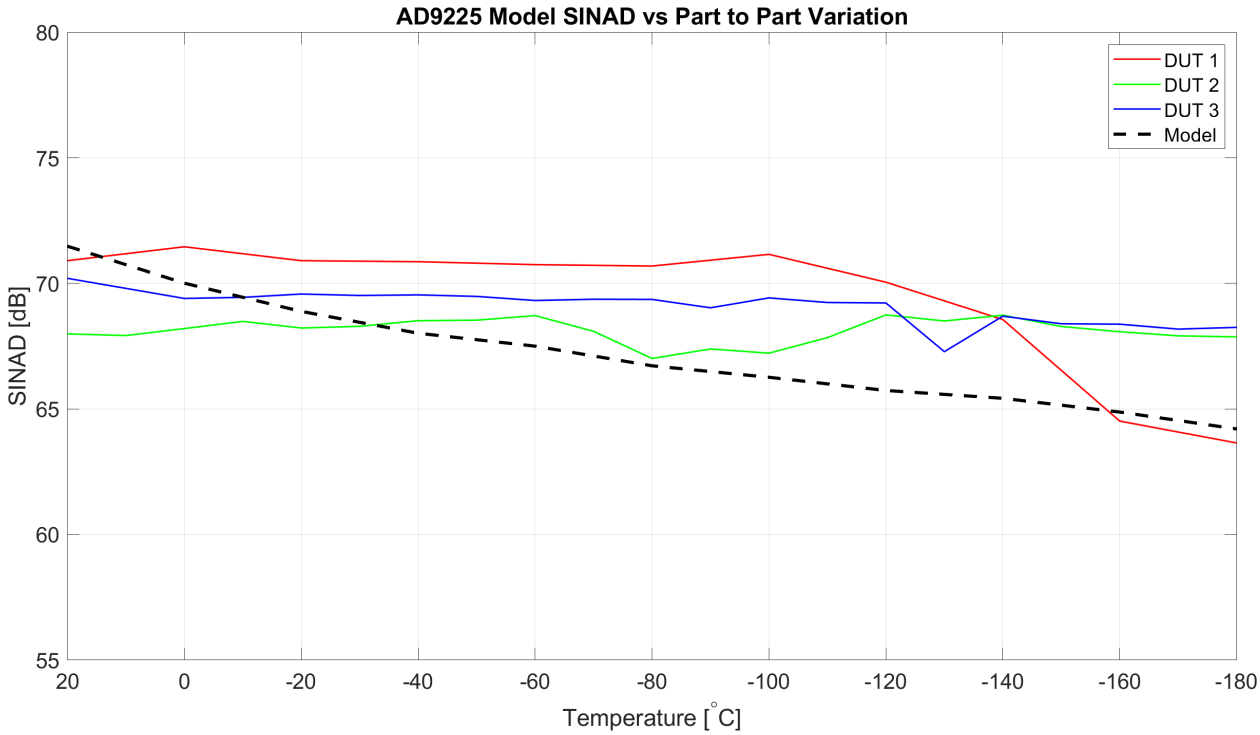


Figure 5.9: SINAD Part to Part Variation

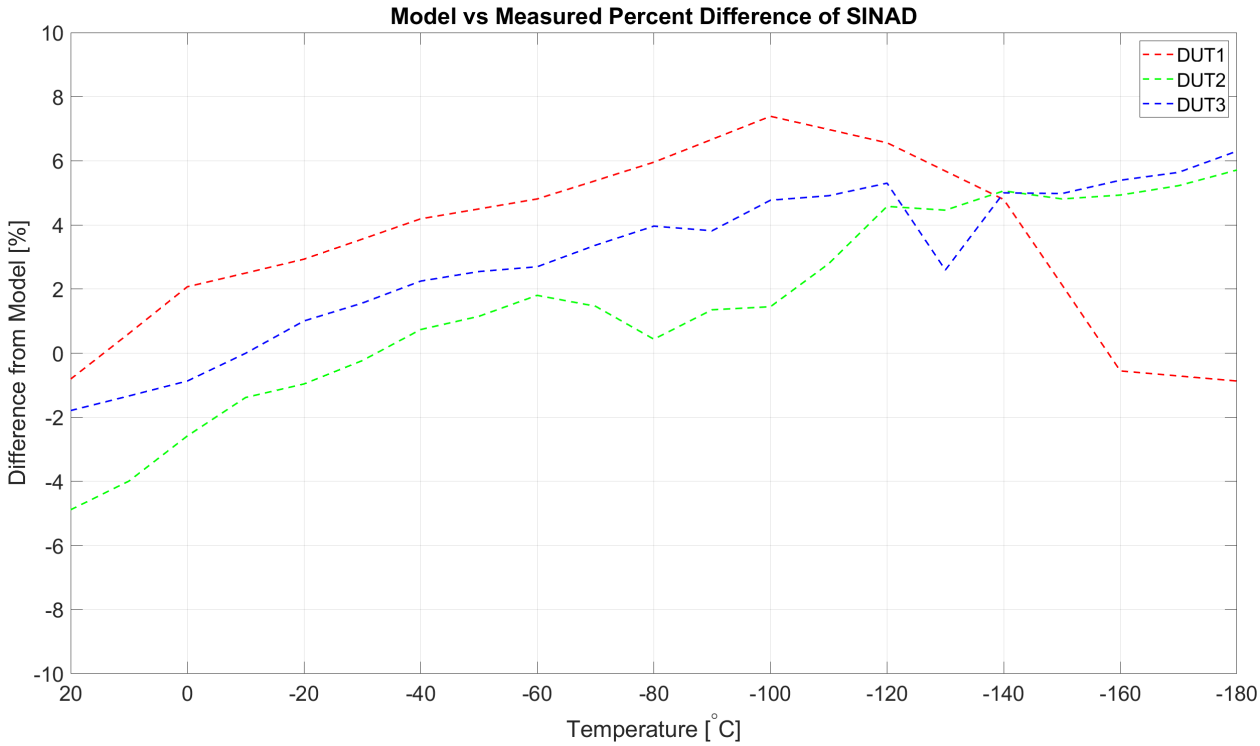


Figure 5.10: SINAD Model Percent Difference

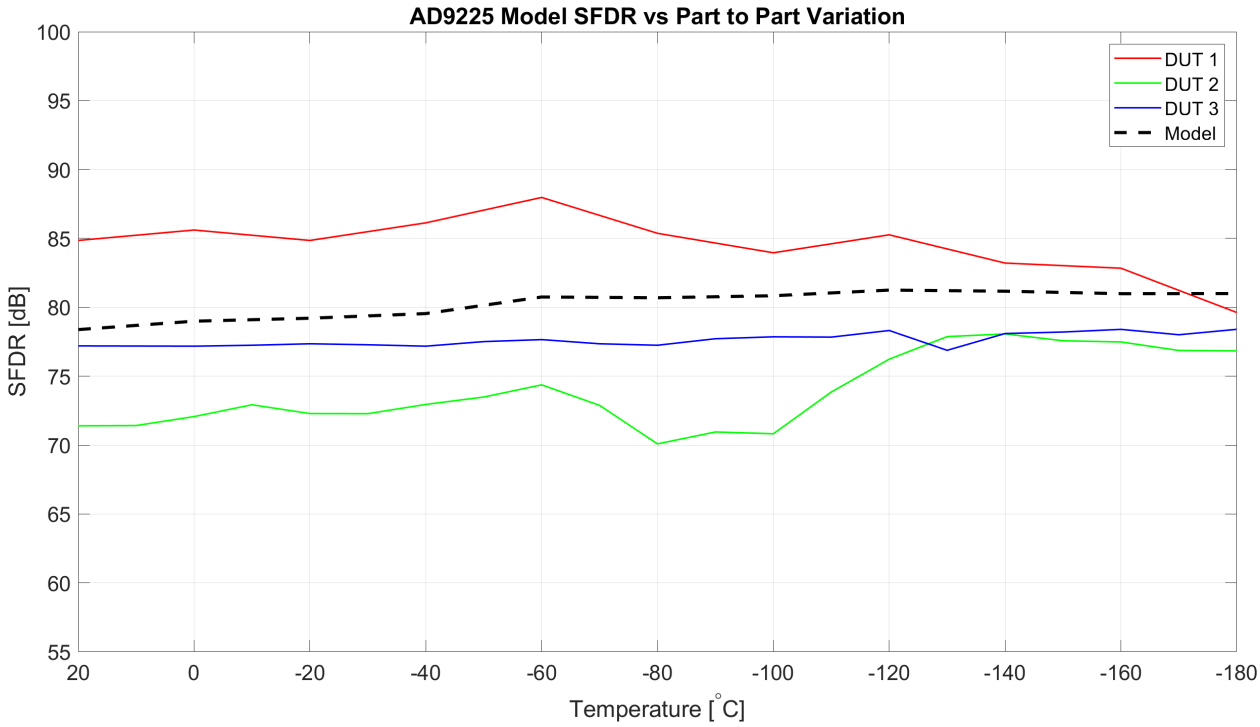


Figure 5.11: SFDR Part to Part Variation

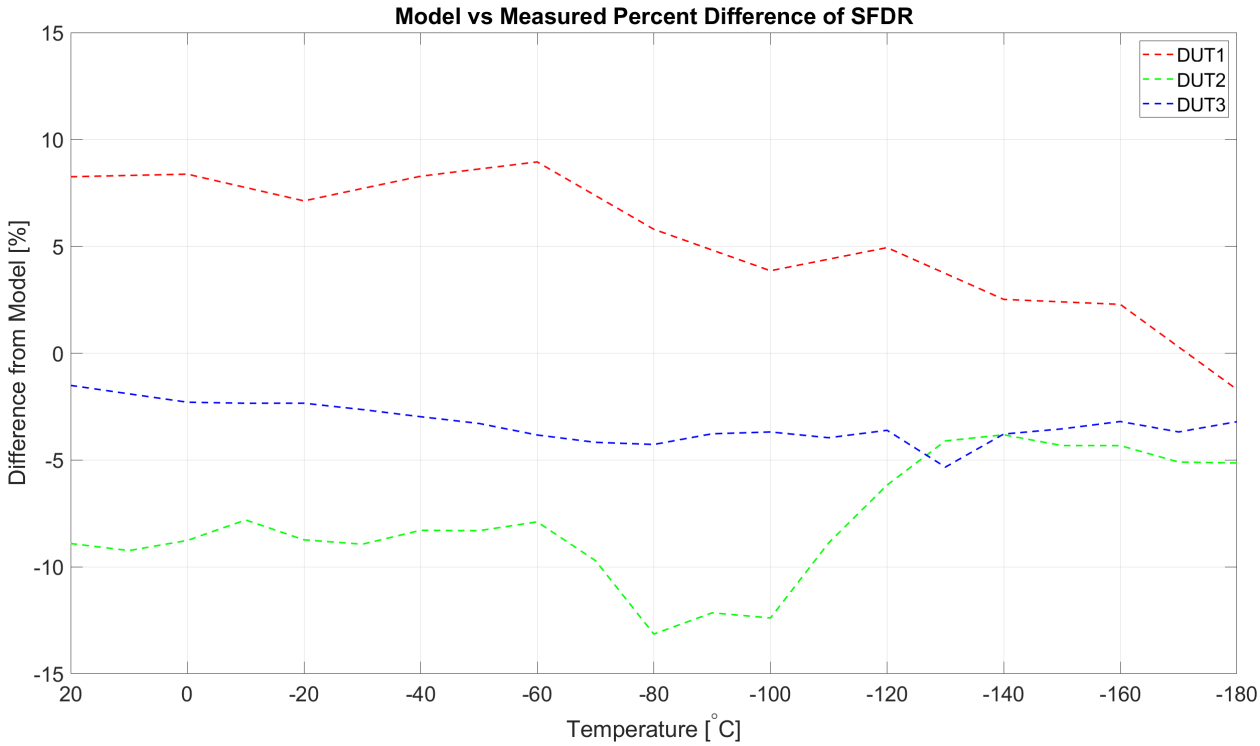


Figure 5.12: SFDR Model Percent Difference

Table 5.1: Additional ADCs

Device	Resolution	Speed	Architecture
LTC1420	12	10 MSPS	Pipeline
LTC2225	12	10 MSPS	Pipeline
AD7693	16	500 kSPS	SAR

i.e. there are no outliers. Also, some of the parameters seem independent of temperature. The fact that the universal model is able to capture both performance that varies with temperature and performance that is independent is a good sign. In most cases, the percent differences, with original values in dB, do not exceed ±10% except for SFDR.

5.2.2 Cross-part Prediction

Beyond capturing performance of a particular part, the universal trends developed can also be applied to another part using technology information and the INL curve. Again applying universal noise and INL shape coefficient trends, one arrives at Figures 5.13, 5.15, 5.17, and 5.19. Also shown in Figures 5.14, 5.16, 5.18, and 5.20 are the percent differences between the simulation and measured performance. In most cases, the difference does not exceed 15% except for THD. The universal model, then, is capable of estimating performance of another part to within 15% of the true performance.

5.2.3 Application to Different ADCs

It is also worth exploring how much total variation can be expected from applying the developed methodology, i.e. how much variation the model can produce. To answer this, it is necessary to look at several other CMOS ADCs and evaluate the variance of predicted performance parameters. The devices in question are shown in Table 5.1. The basic strategy is to populate the THA parameters and use the datasheet INL curve along with coefficient trends to estimate the performance of the part across temperature. The results of this procedure are shown in Figures 5.21, 5.22, and 5.23.

Finally, Table 5.2 shows a comparison between model predicted performance at room temperature and datasheet performance at room temperature. The difference between the

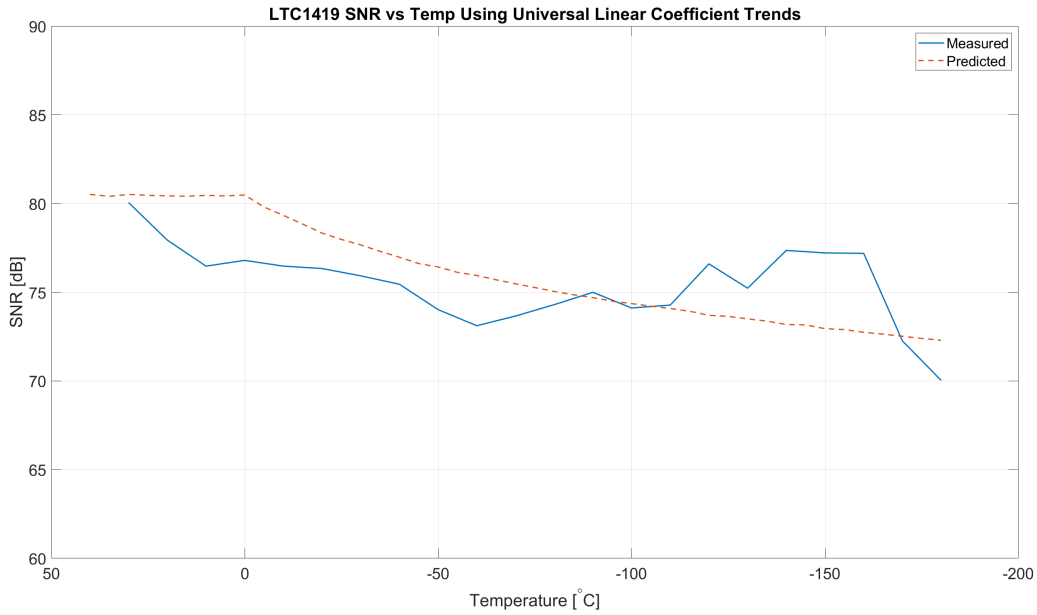


Figure 5.13: Cross-part SNR Prediction of LTC1419

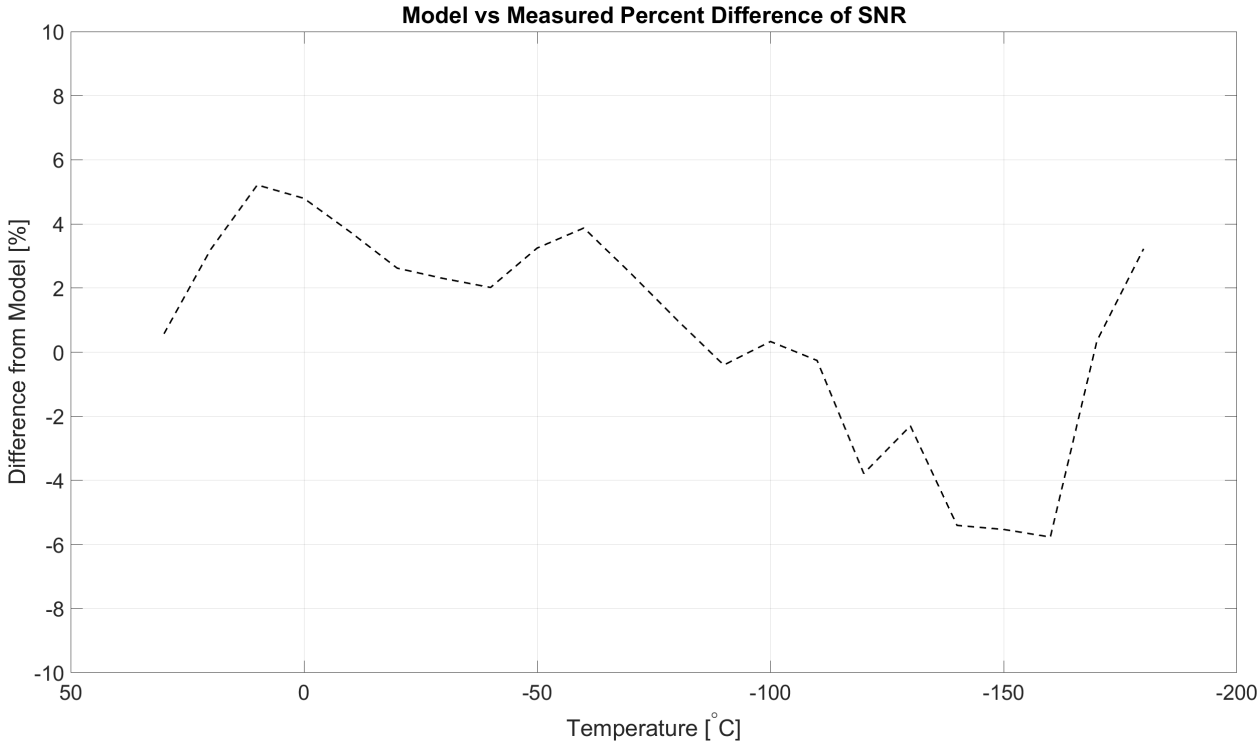


Figure 5.14: AD9225 Percent Model Difference - SNR

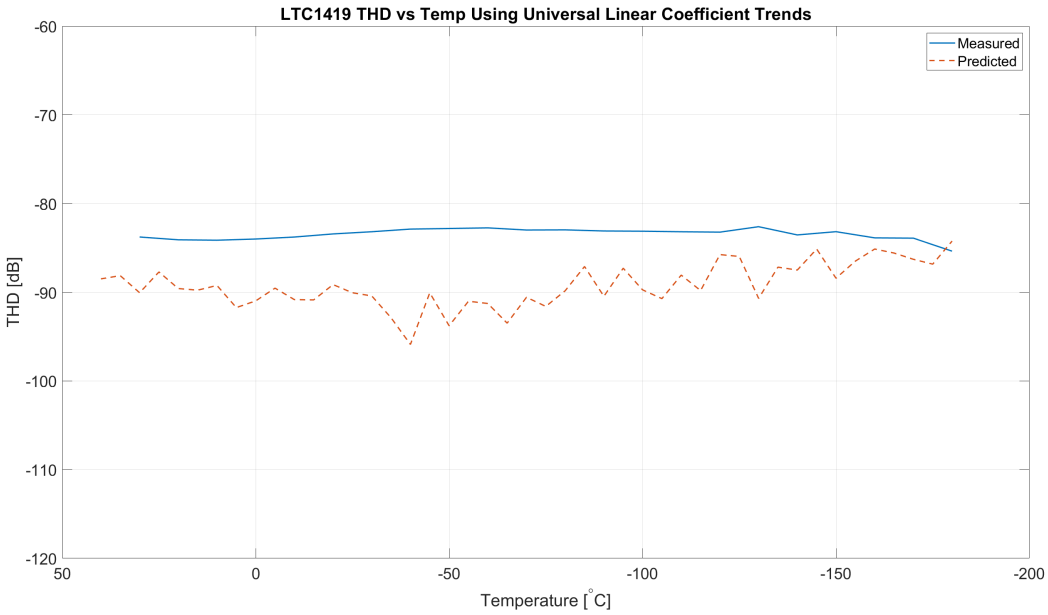


Figure 5.15: Cross-part THD Prediction of LTC1419

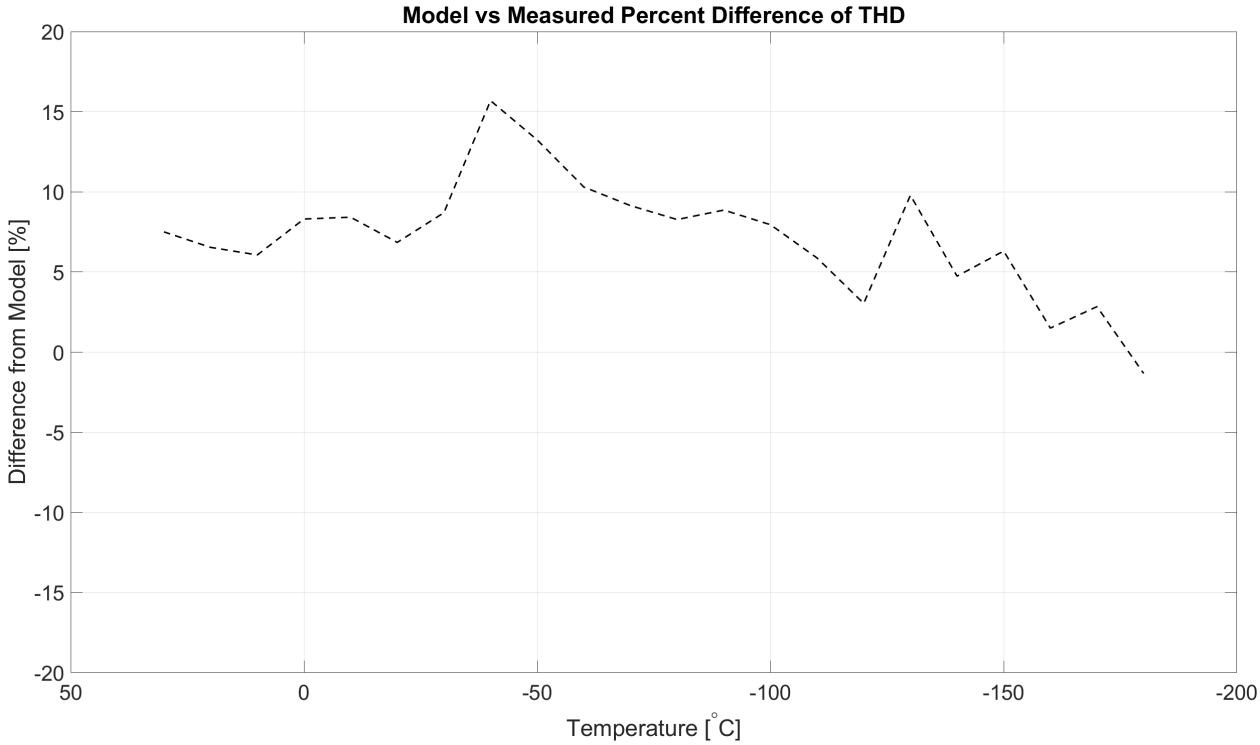


Figure 5.16: AD9225 Percent Model Difference - THD

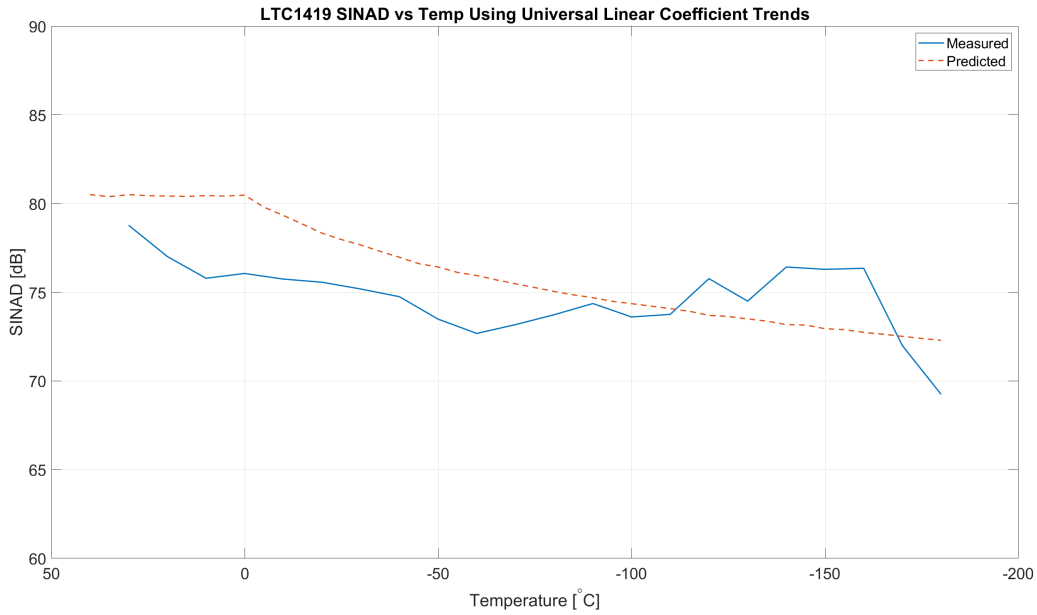


Figure 5.17: Cross-part SNDR Prediction of LTC1419

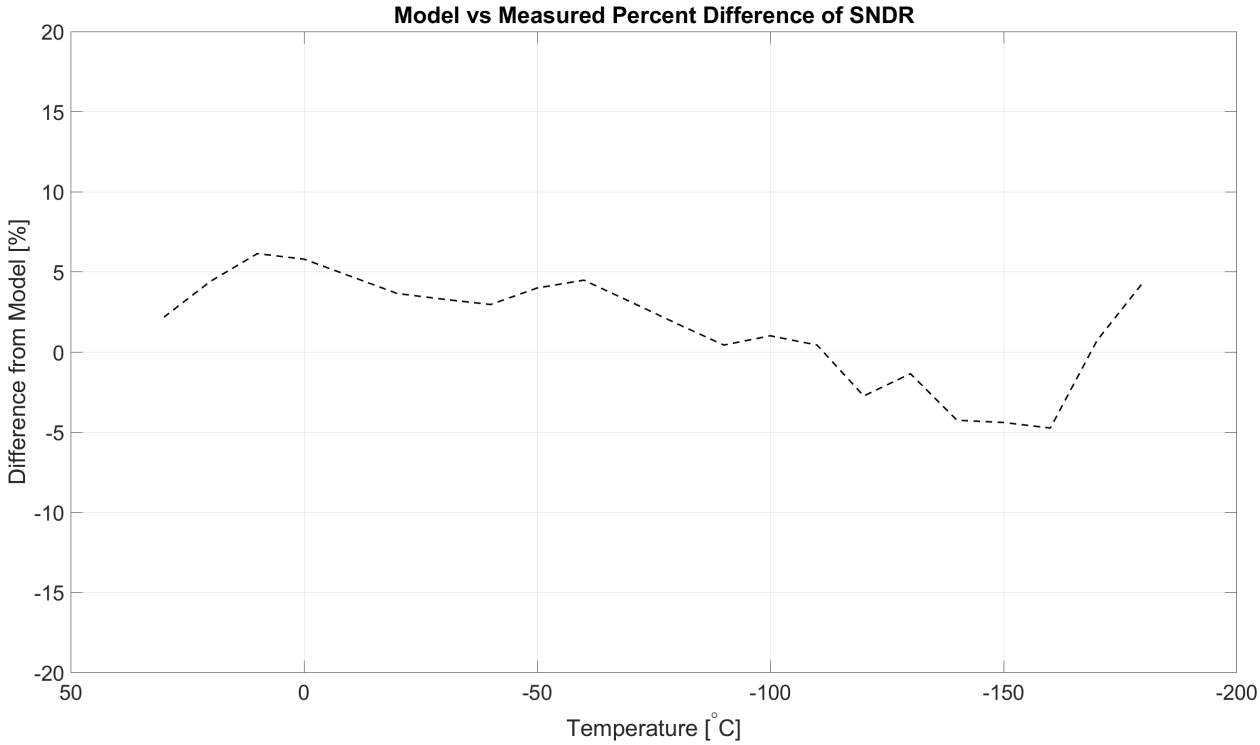


Figure 5.18: AD9225 Percent Model Difference - SNDR

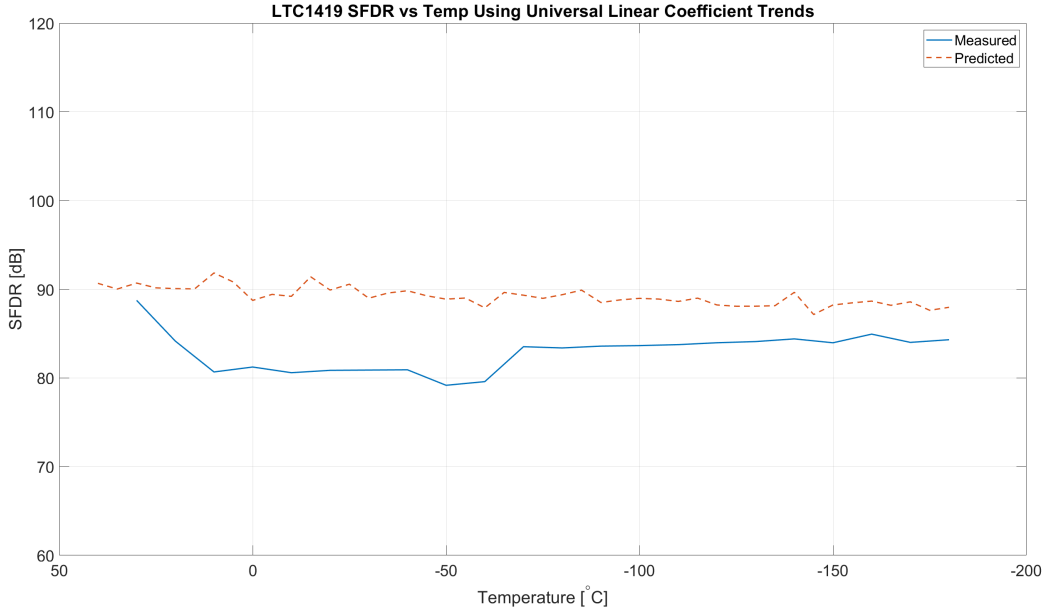


Figure 5.19: Cross-part SFDR Prediction of LTC1419

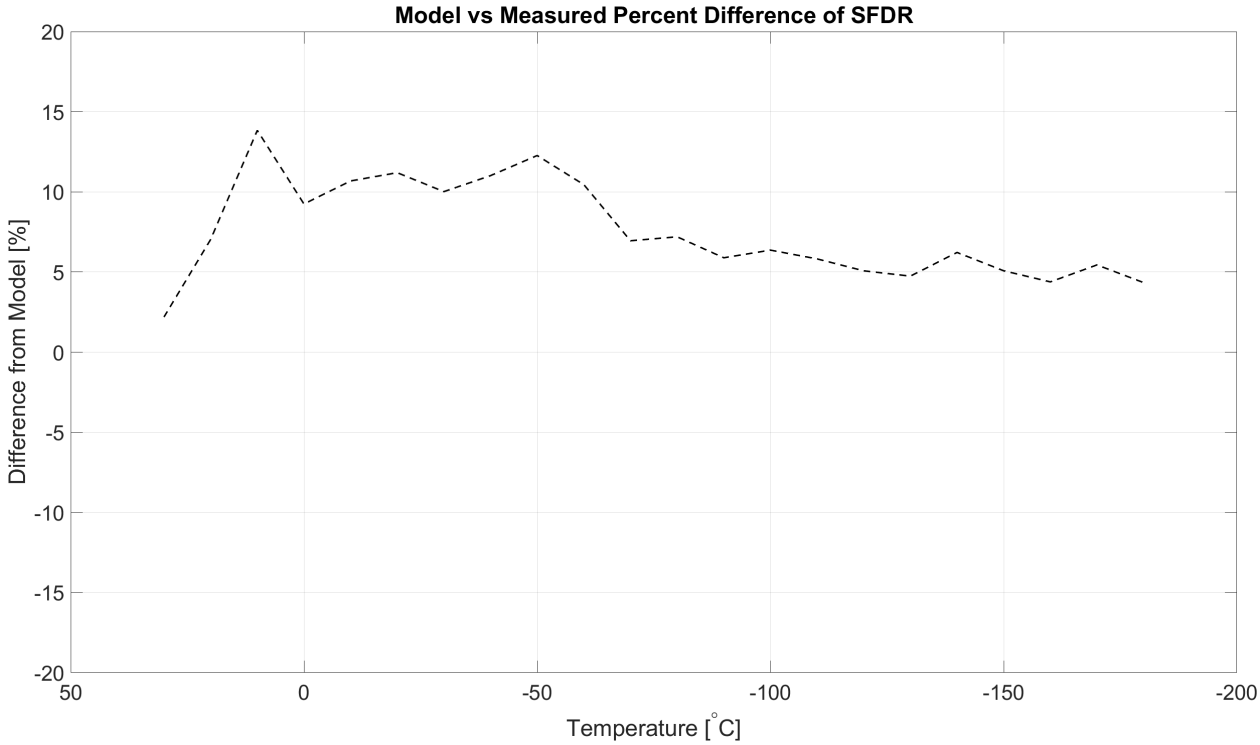


Figure 5.20: AD9225 Percent Model Difference - SFDR

Table 5.2: Baseline Model Comparison

	SNR	THD	SFDR
Model - LTC1420	72.09	-86.61	85.38
Datasheet - LTC1420	71.00	-81.00	85.00
Model - LTC2225	71.43	-85.14	82.95
Datasheet - LTC2225	71.30	-82.16	90.00
Model - AD7693	94.16	-126.03	126.83
Datasheet - AD7693	96.40	-120.00	124.00

two is a baseline for how well the model can approximate realistic converter behavior. For most parameters, the initial model and datasheet values are quite close, indicating a promising start for accurately capturing converter performance.

5.2.4 1st Order Extrapolation

While the model is capable of utilizing a datasheet curve and universal coefficient trends to form a 0th-order estimate of ADC performance, the actual coefficient trends can be measured across the part's nominal temperature range and used to create a more accurate 1st order model. The result of applying this technique is shown in Figures 5.24-5.31 for both the AD9225 and LTC1419.

5.2.5 Model Coefficient Statistical Analysis

Beyond comparing measured and simulated performance, it is useful to consider a statistical analysis of the relevant coefficient parameters to shed light on how much, if any, importance and significance the model coefficients hold.

Model Coefficient Covariance Matrix

The covariance matrix of model coefficients is obtained by populating a matrix whose columns are observations of INL coefficients across temperature and whose rows are a particular power of x. The covariance of each term is then computed and stored in a symmetric 6×6 matrix and can also be normalized, as shown in the heatmap in Figure

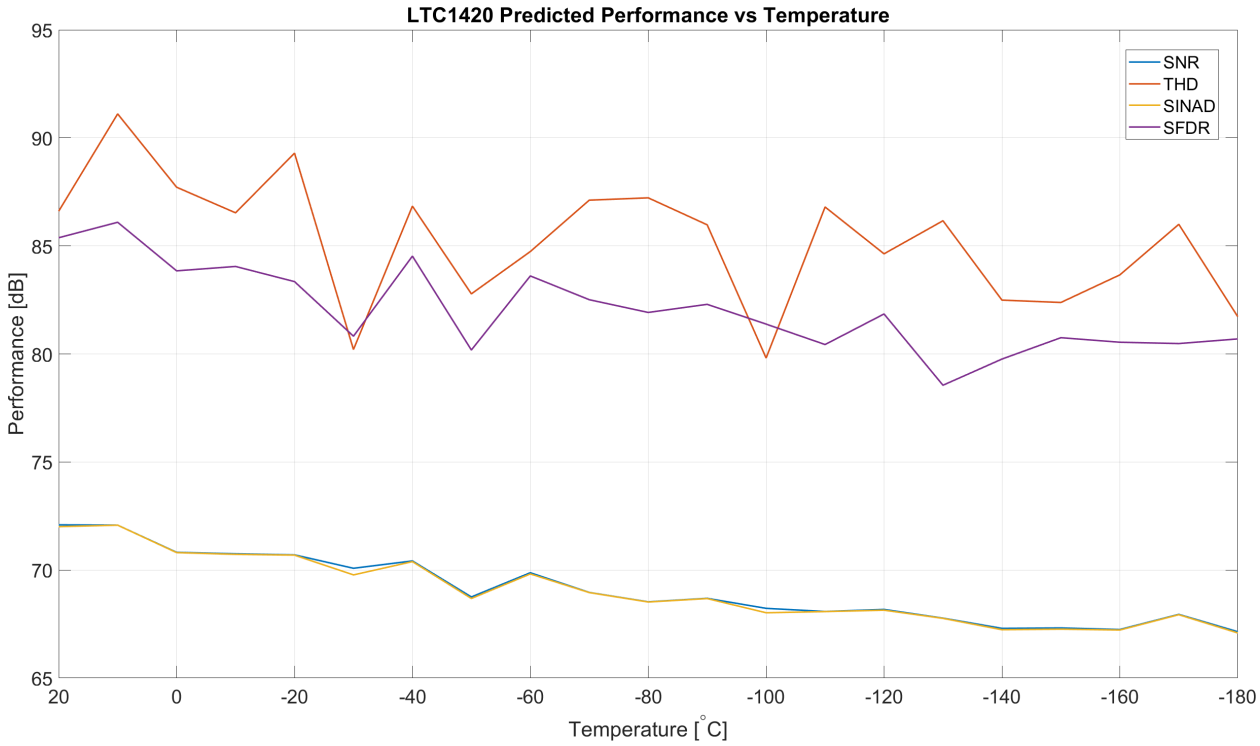


Figure 5.21: LTC1420 Predicted Performance

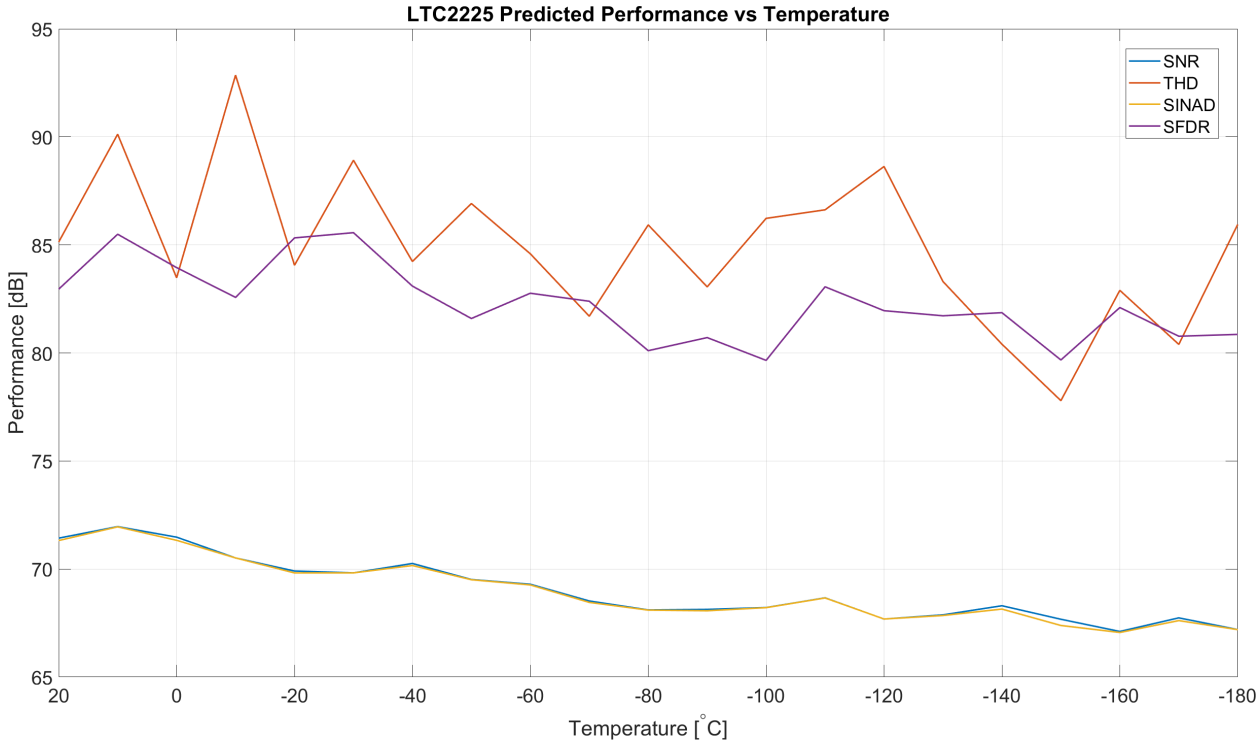


Figure 5.22: LTC2225 Predicted Performance

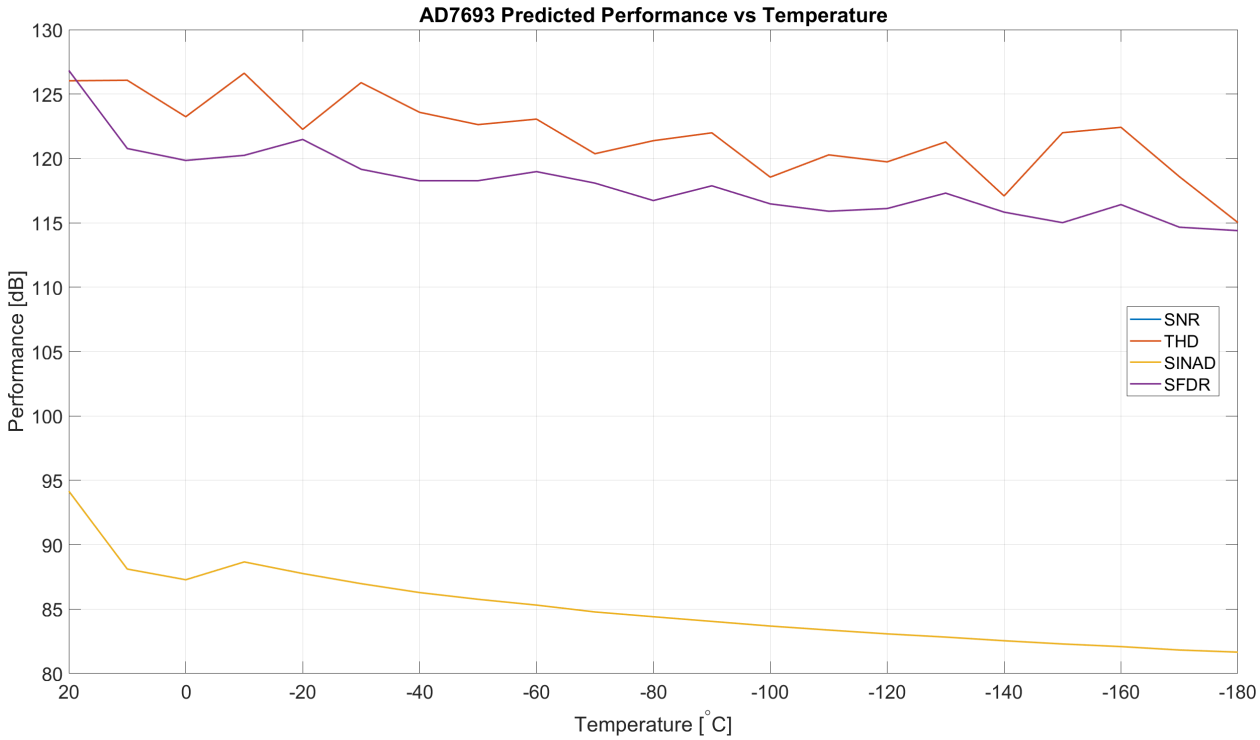


Figure 5.23: AD7693 Predicted Performance

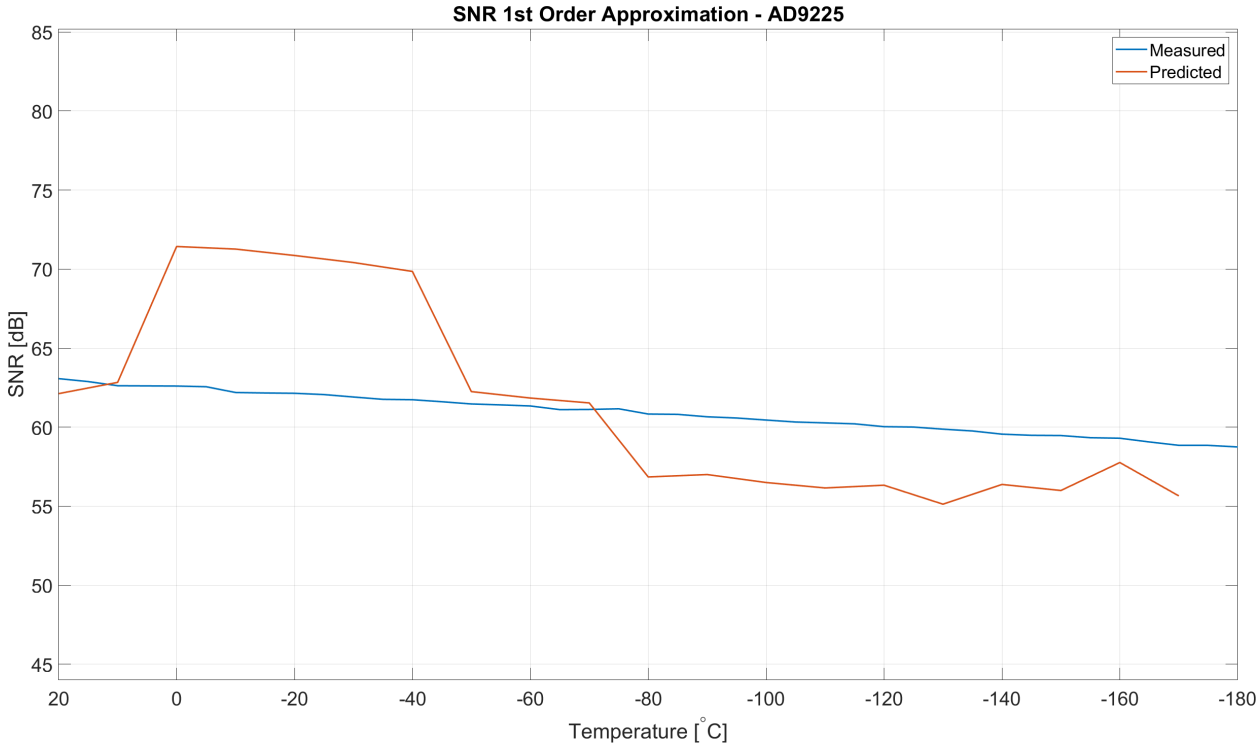


Figure 5.24: 1st Order Model - AD9225 SNR

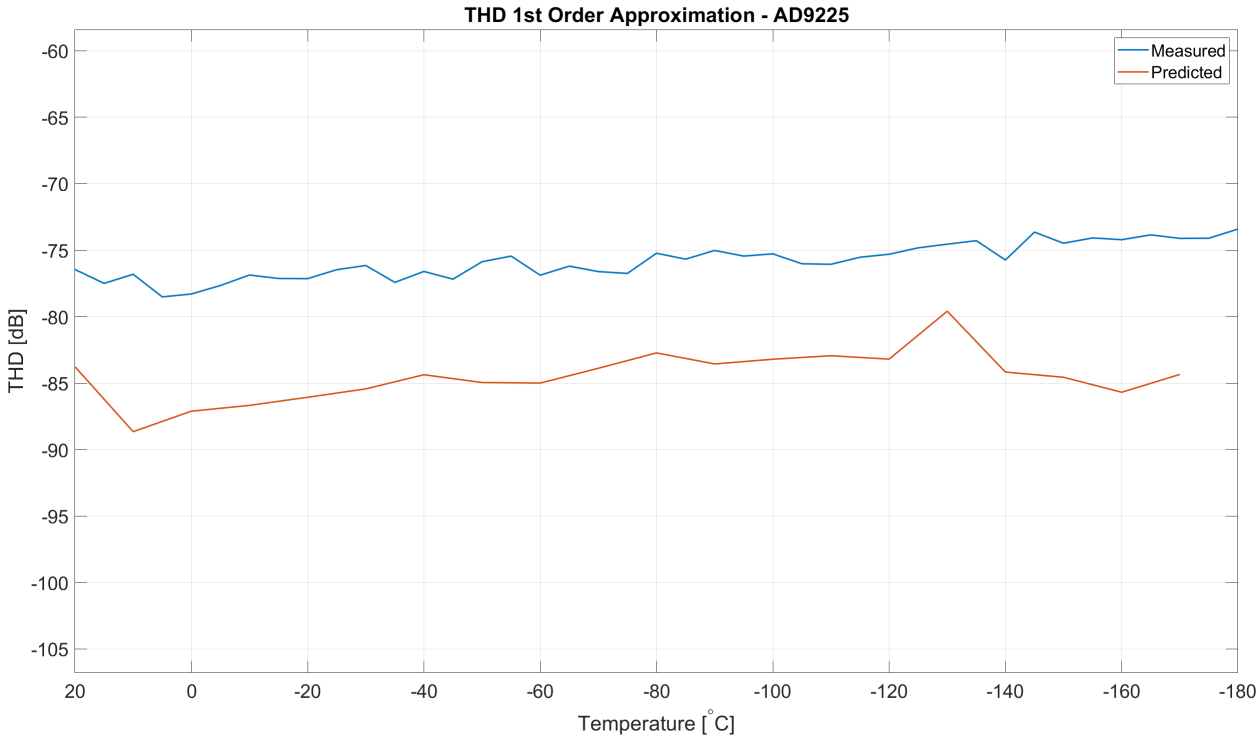


Figure 5.25: 1st Order Model - AD9225 THD

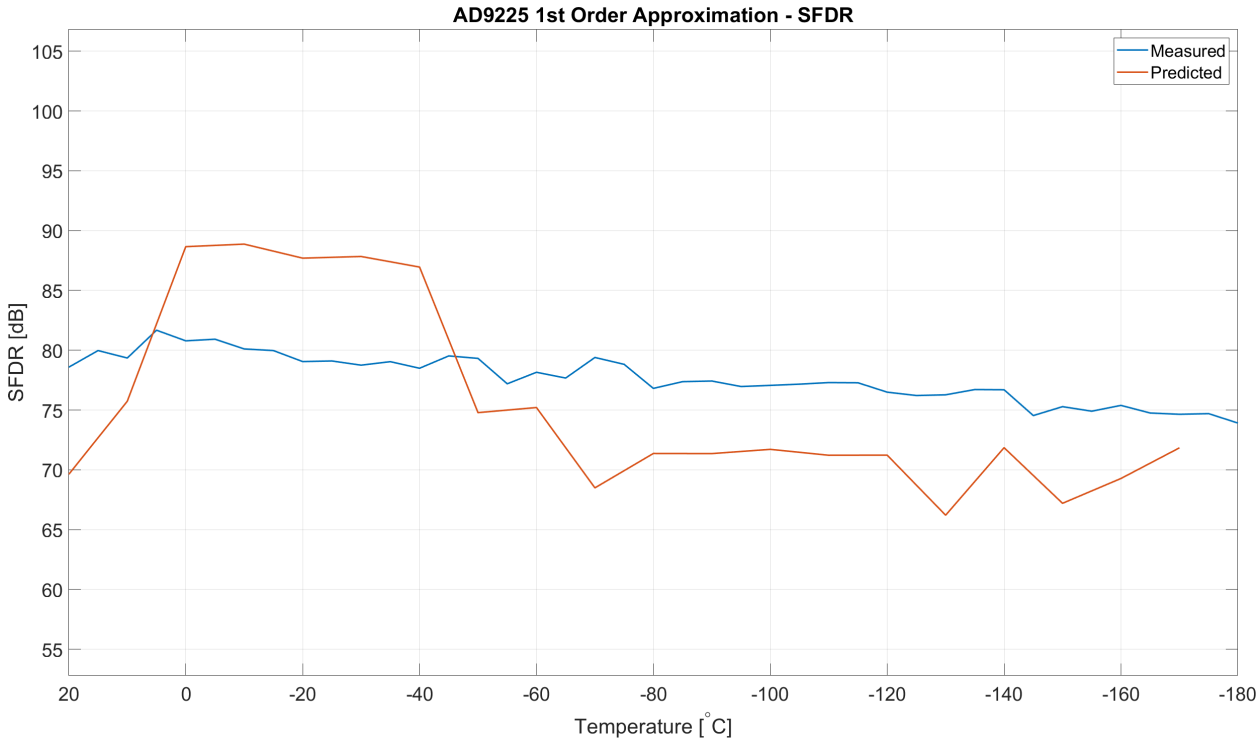


Figure 5.26: 1st Order Model - AD9225 SFDR

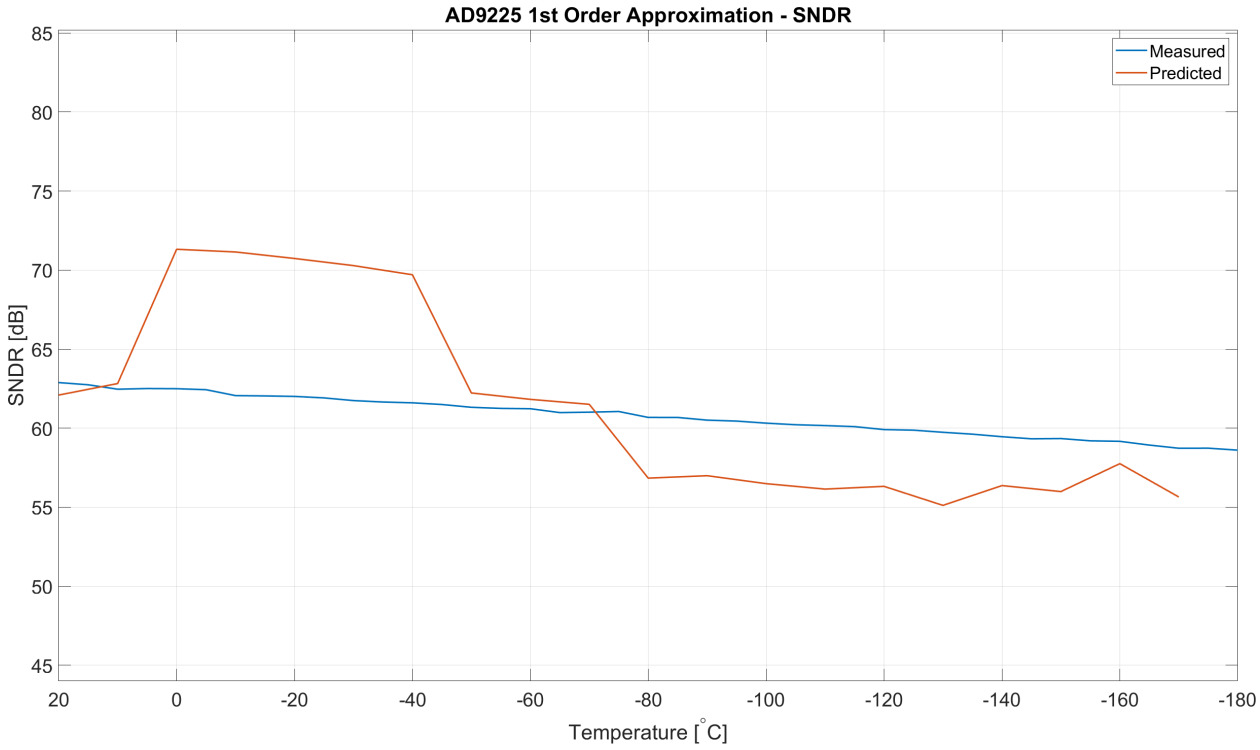


Figure 5.27: 1st Order Model - AD9225 SNDR

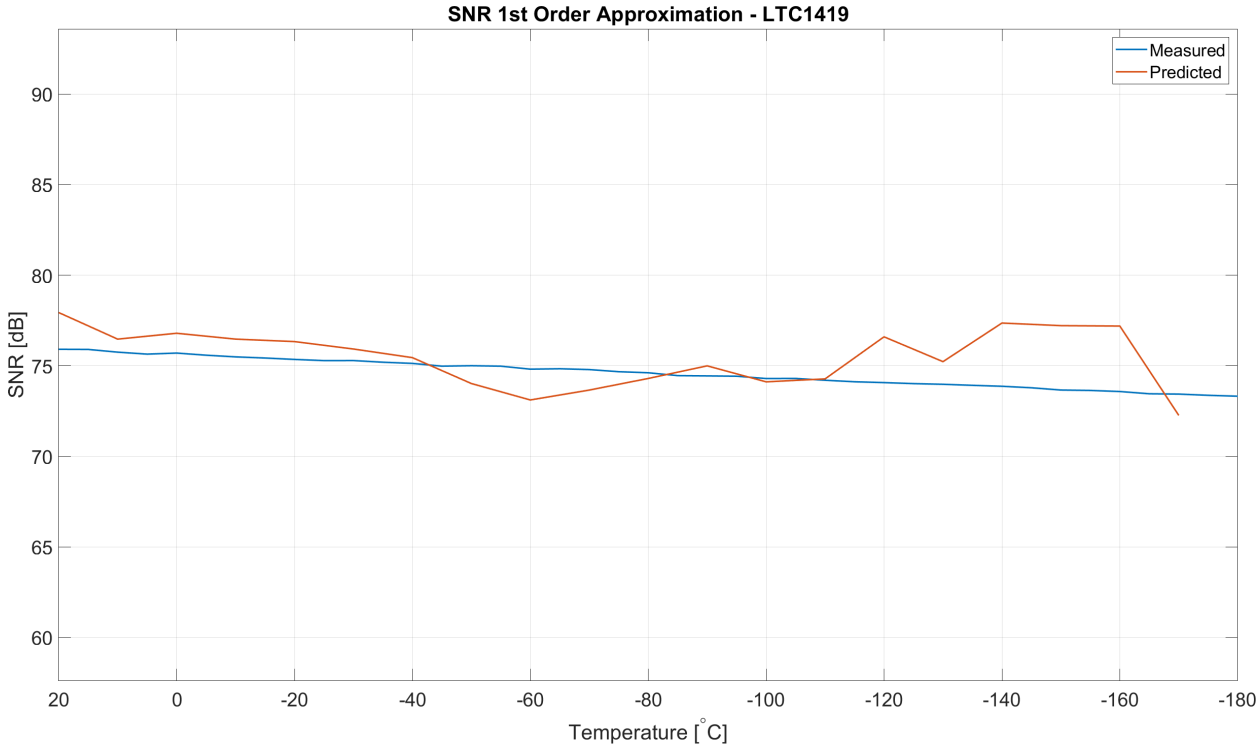


Figure 5.28: 1st Order Model - LTC1419 SNR

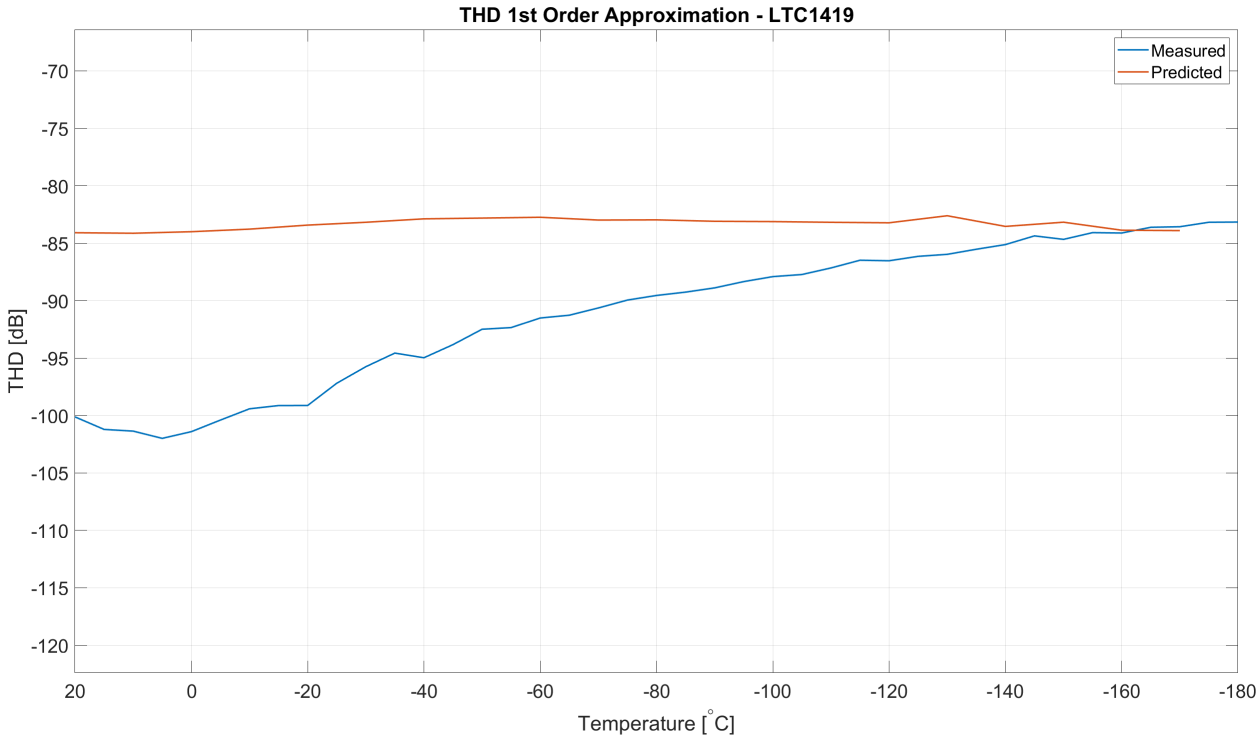


Figure 5.29: 1st Order Model - LTC1419 THD

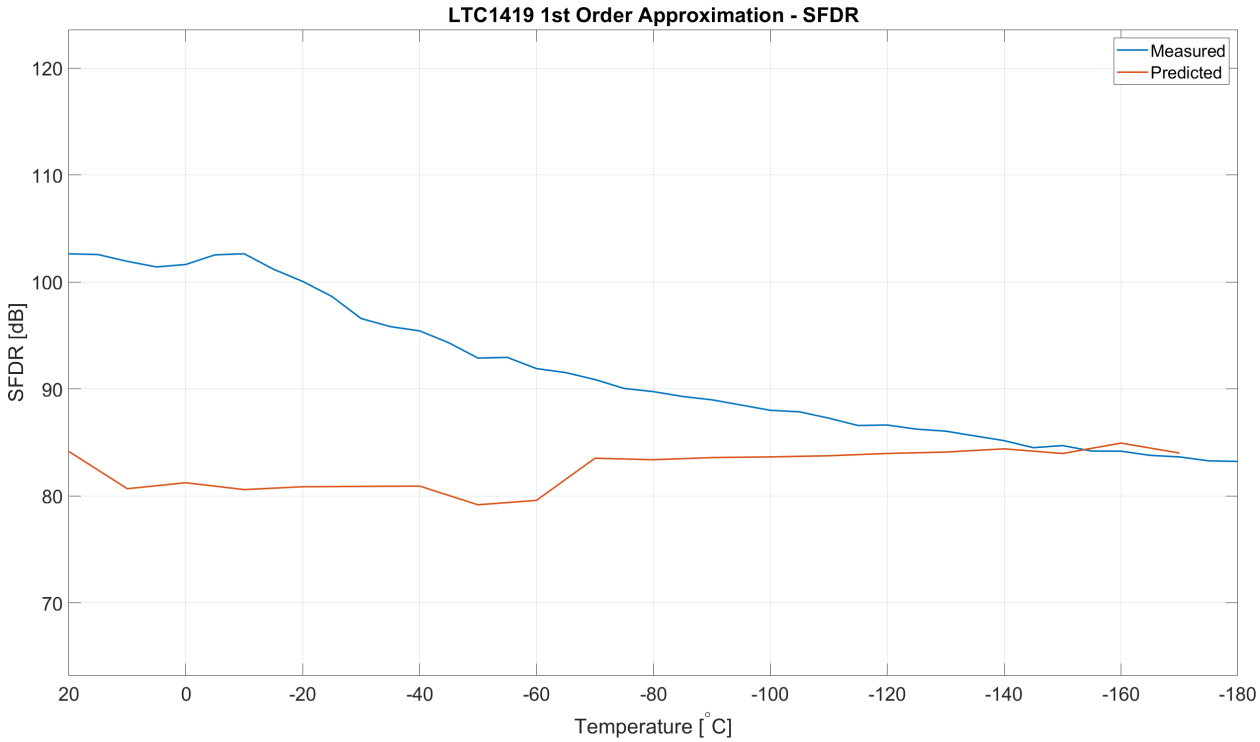


Figure 5.30: 1st Order Model - LTC1419 SFDR

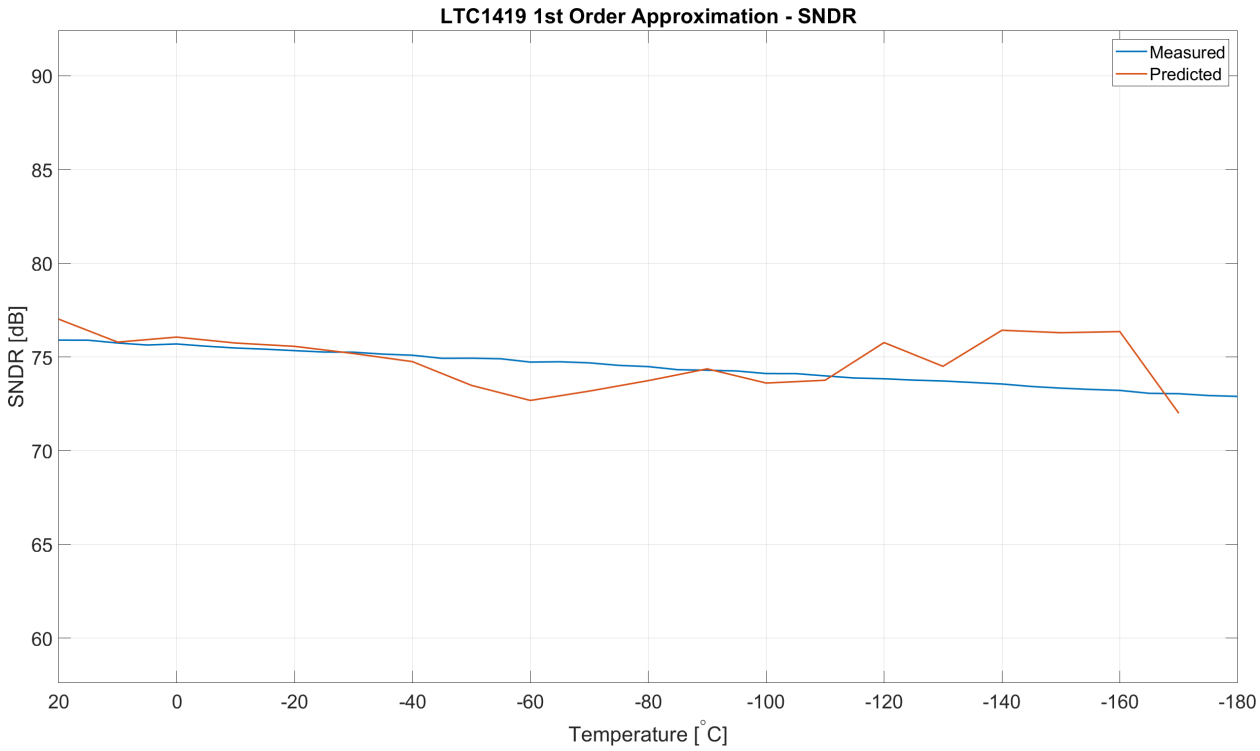


Figure 5.31: 1st Order Model - LTC1419 SNDR

5.32. There appears to be a strong relationship between the odd-order coefficients with little interaction among the even-order coefficients, perhaps due to the fully-differential design of both the AD9225 and LTC1419.

In addition to the correlation coefficient matrix, it is also useful to look at the p-values associated with the correlation matrix. In this case, a p-value of near zero indicates strong evidence to reject the null hypothesis, i.e. the assertion that any observed variation in a parameter is due to random noise and is not statistically significant. In this case, from looking at the heatmap shown in Figure 5.33, one immediately observes that odd-order coefficients have very low p-values indicating strong confidence that their correlations are statistically significant. Beyond that, x^4 and x^2 appear to be weakly correlated.

p-Value for Slope of Model Coefficients

In addition to the correlation matrix, it is also useful to consider the linear models used to derive the temperature trends of the INL polynomial coefficients, especially the slope with respect to temperature. The important parameter in this case is the p-value associated with

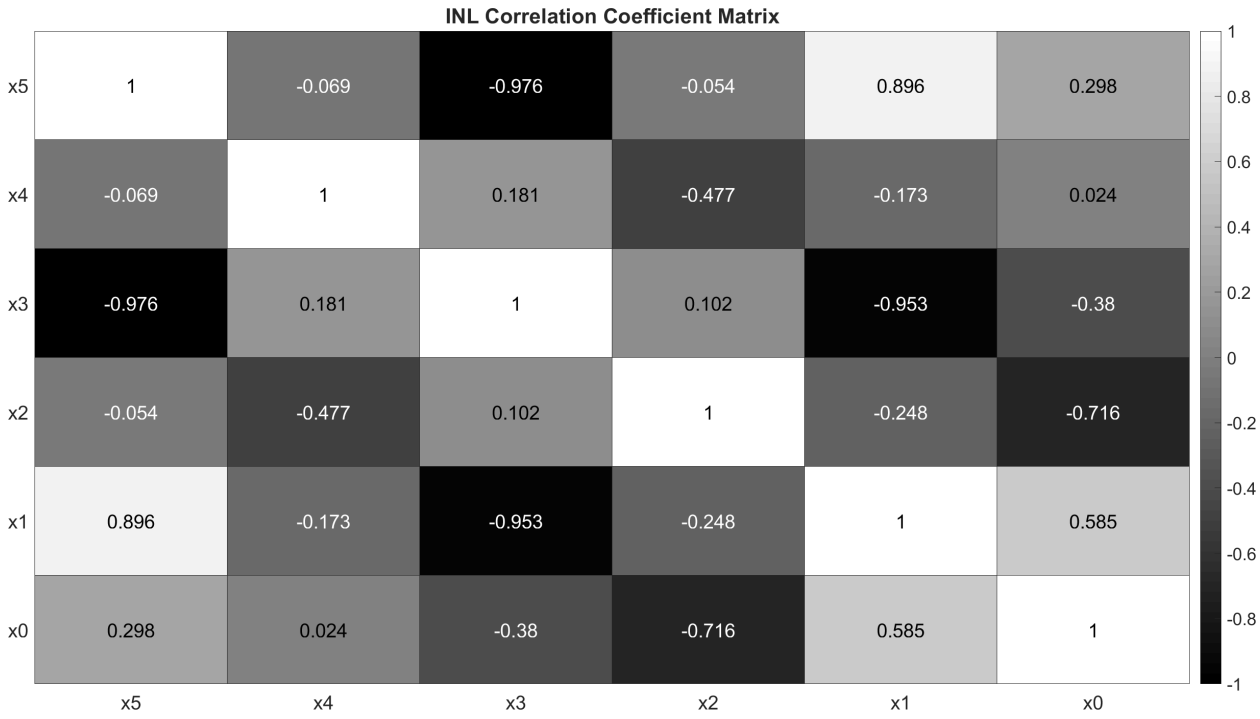


Figure 5.32: Correlation Coefficients of INL Model Terms

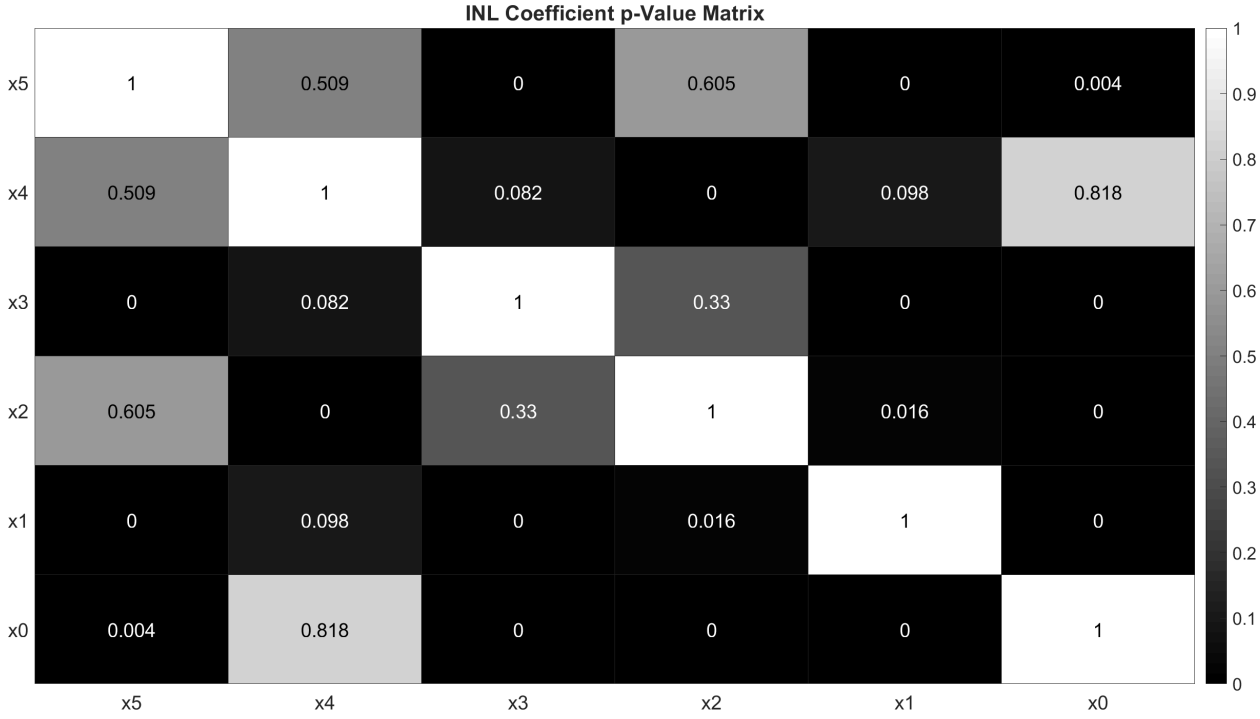


Figure 5.33: INL p-Value Coefficient

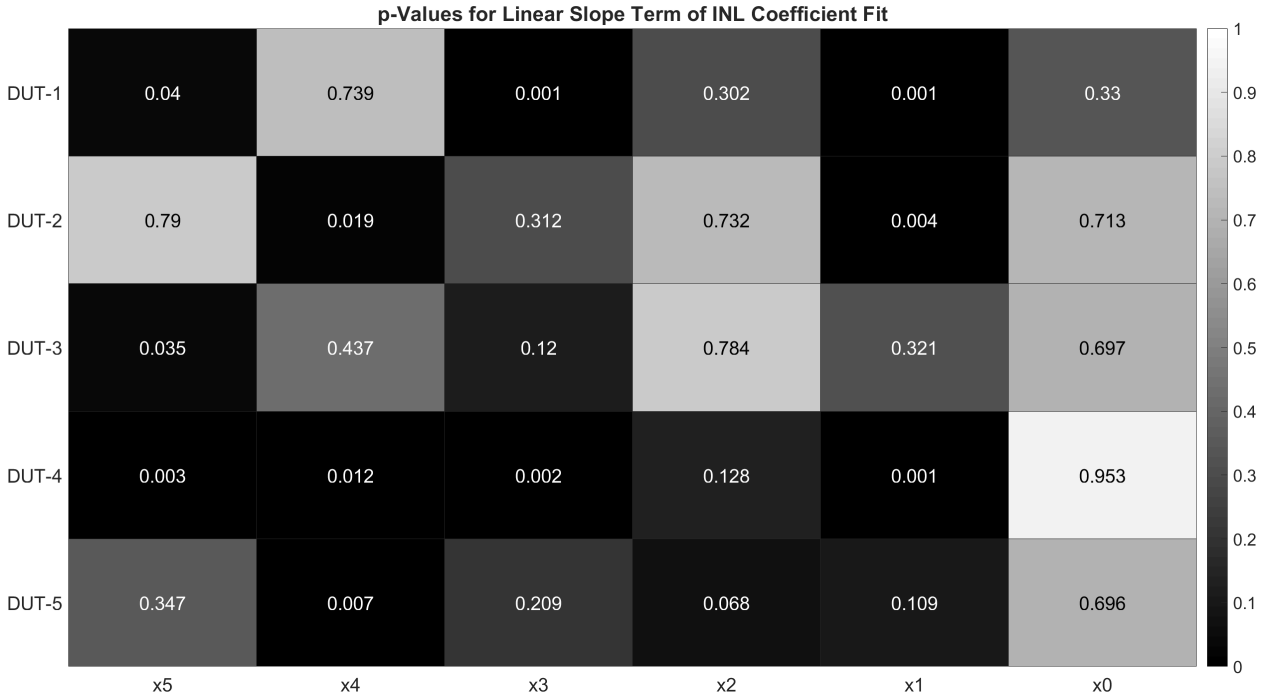


Figure 5.34: Linear Slope p-Value

the temperature slope coefficient for the two ADCs tested as shown in Figure 5.34. Statistical significance of results is typically confirmed when $p < 0.05$. From the figure above, the odd-order coefficients in general appear to be more statistically significant. DUT-1 has slopes that are the most significant, followed by DUT-4. The other devices tested contain only weakly significant trends and the universal model was built by considering an aggregate of all trends. This may have been an unwise choice as some devices display more meaningful variation with respect to temperature in their INL coefficients than others and should be weighted accordingly.

Principal Component Analysis Cluster Analysis of Model Coefficients

To round out a deeper look at the model parameters, it can be worthwhile to apply clustering techniques to further analyze the model coefficients. Such an analysis would reveal hidden patterns in the data indicating whether the trends are universal or are meaningfully separated according to the actual device tested. To accomplish this, one can apply principal component analysis (PCA) to find eigenvectors of the covariance matrix given earlier which, along with their associated eigenvalues, give the directions and strength of maximal variance. In this

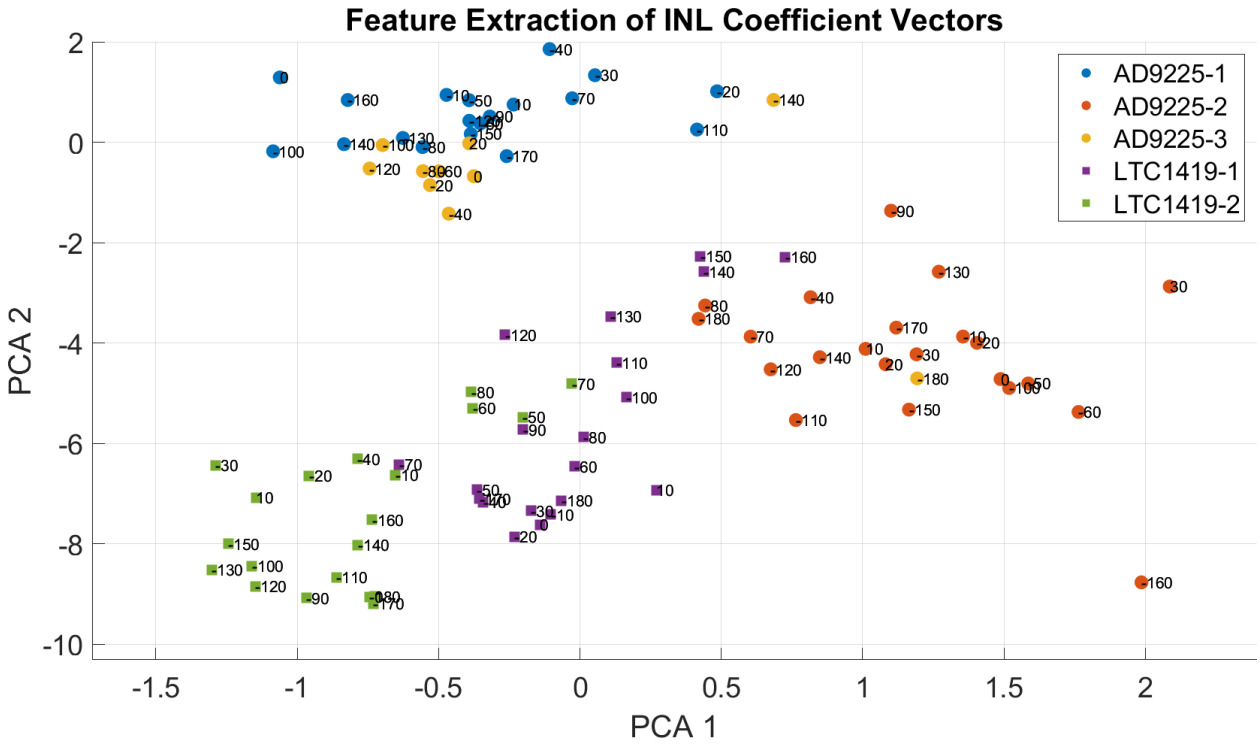


Figure 5.35: PCA Clustering of INL Coefficients

case, the data is the 6 dimensional LCF polynomial coefficients, one for each temperature, for all devices tested.

By projecting the data onto a lower dimension along the vectors of maximal variance, the relevant features and relationships can be maintained while suppressing noise. The results of dimensionality reduction from 6D to 2D are shown in Figure 5.35. The 2D coefficient vectors have been color-coded according to specific ADCs tested and labeled with their respective temperatures. As can be clearly seen from the data, there are natural clusters corresponding to each of the devices indicating the coefficients vary around a common point, one for each device. A question then is whether there is a meaningful way to collate these coefficient trends when, clearly, they cluster according to the specific device tested. The disparate clustering brings to question the validity and existence of a universal model.

5.3 Summary and Commentary on Results

The overall goal was to build a generic ADC model which could be built from minimal test data and had the ability to forecast the performance of a device across various temperatures. A major question is this: how do the assumptions used to build the model impact its ability to achieve the stated goal? The extrapolation of observed trends in the model parameters of the transfer curve and normalized input noise power, termed the 0th order model, seem capable of estimating to some degree the cross part performance of multiple converters. This seems to indicate that the methodology is sound and that some meaningful trend is being observed. Such hopeful signs belie the remaining difficulty of reverse-engineering the exact source of temperature instability, as seen in the testing of the LTC1419 where the on-chip reference amplifier failed to operate past -60 °C.

Chapter 6

Conclusions

6.1 This Work

Attempting to predict part performance through limited testing, especially when using parts outside of their intended design range, remains a difficult goal. Architecture agnostic behavioral models, while broadly applicable and fast to simulate, can have trouble capturing specific device performance especially when devices operate outside of their intended temperature ranges. While some device behavior can be captured by applying architecture-specific models, there remains a degree of uncertainty regarding overall functionality and performance.

Internal biasing of parts is often affected by large swings in temperature, upsetting carefully tuned voltages and currents. In one instance, the internal voltage reference buffer amplifier died at -60 °C necessitating rerouting of external voltage to another pin. Such occurrences cannot be easily captured or predicted *a priori* from models without incorporating specific cryogenic effects on individual transistors. Doing so would then require access to copyright-protected schematics and process information. To adequately predict and guarantee cold-temperature performance, it may be necessary to investigate potential circuits at the transistor level using tuned cold-sensitive transistor models. At the very least, component testing and characterization must allow access to internal nodes for monitoring of bias points. Regardless of these challenges, several converters were tested and their transfer curves and noise responses characterized across temperature. The trends in these parameters

were then applied to initial values from datasheets and the overall trend matched the observed data. While there was an offset for many of the measured parameters, the overall trend was clear.

6.2 Future Work

Given existing model efforts, several areas of improvement exist depending on the particular model approach in question. For the architecture specific models, it may be recommended to port them to Verilog-AMS for easier integration with common circuit simulators. This could permit transistor-based realistic models of say internal amplifiers, comparators, or DACs, to interact with functional blocks, greatly speeding up simulation of a mixed-signal chip or system. Regarding the generic INL-based ADC model, a major improvement would be to include input slope dependence into INL model to accurately capture the dynamic nature of converter transition locations. Such a modification could go a long way towards improving the model's ability to capture distortion.

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Vita

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