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I am submitting herewith a thesis written by Chris G. Moscone entitled "A CMOS Integrating Amplifier For The PHENIX Ring Imaging Cherenkov Detector." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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A CMOS Integrating Amplifier For The PHENIX Ring Imaging Cherenkov Detector

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Chris G. Moscone
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Dedication

This thesis is dedicated to my fiancee, Tina, whose continual support and understanding has provided me the strength and motivation to pursue my dreams,

and

to my mother Jean Brady, whose love and guidance has built the foundation on which I now stand.

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Finally, I would like to thank God for giving me the ability, motivation, and strength to pursue this work.

Abstract

A CMOS integrating amplifier has been developed for use in the PHENIX Ring Imaging Cherenkov (RICH) detector. The amplifier, consisting of a charge-integrating amplifier followed by a variable gain amplifier (VGA), is an element of a photon measurement system comprising a photomultiplier tube, a wideband, gain-of-10 amplifier, the integrating amplifier, and an analog memory followed by an ADC and double correlated sampling implemented in software. The integrating amplifier is designed for a nominal full scale input of 160 pC with a gain of 20 mV/pC and a dynamic range of 1000:1. The VGA is used for equalizing gains prior to forming analog sums for trigger purposes. The gain of the VGA is variable over a 3:1 range using a 5-bit digital control, and the risetime is held to approximately 20 ns using switched compensation in the VGA. Details of the design and results from several prototype devices fabricated in 1.2 μm Orbit CMOS are presented. A complete noise analysis of the integrating amplifier and the correlated sampling process is included as well as a comparison of calculated, simulated and measured results.

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List of Abbreviations

ADC	Analog To Digital Converter
AMU	Analog Memory Unit
BRAHMS	Broad Range Hadron Magnetic Spectrometers Experiment
DAC	Digital To Analog Converter
DIP	Dual Inline Package
EMCal	Electromagnetic Calorimeter
FET	Field Effect Transistor
IC	Integrated Circuit
INL	Integral Nonlinearity
LHC	Large Hadron Collider
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MVD	Multiplicity Vertex Detector
NMOS	N-Channel Metal Oxide Semiconductor
PHENIX	Pioneering High Energy Nuclear Instrumentation Experiment
PMOS	P-Channel Metal Oxide Semiconductor
PMT	Photomultiplier Tube
PSD	Power Spectral Density
QGP	Quark-Gluon Plasma
RF	Radio Frequency
RHIC	Relativistic Heavy Ion Collider
RICH	Ring Imaging Cherenkov Detector

SPICE	Simulation Program with Integrated Circuit Emphasis
STAR	Solenoidal Tracker at RHIC
TEC	Time Expansion Chamber
TOF	Time Of Flight
VGA	Variable Gain Amplifier
W/L	Width to Length ratio

Chapter 1

Colliders and Detector Systems

1.1 Introduction to Colliders

Understanding the world in which we live is a fundamental goal of science. Particle physics is a branch of science which seeks to explore the nature, composition, and behavior of the matter which forms our universe. Modern science has taken tremendous strides forward in the area of particle physics during the Twentieth Century. In the search for the building blocks of matter, particle physics experiments have revealed a world previously unknown, and have provided insight into the world of elementary particles, which includes quarks and leptons, and the forces between them.

An investigation of matter on this sub-atomic scale cannot be carried out with conventional measurement devices. Instead, physicists use devices known as colliders to provide crucial data about elementary particles. A collider is a high-energy accelerator which can supply particles with sufficient energy to simulate their behavior as they did in the very early moments of the universe. Experiments can therefore be performed in which accelerated particles gain sufficient energy so that, upon collision with other high-energy particles, new particles are formed. The formation of new particles occurs as energy is converted into mass in accordance with Einstein's equation, $E = mc^2$.

The information gained from collider experiments is used to verify or discount present physics theories, as well as to provide steering and guidance for future theoretical work. Past accomplishments of particle physics include the first observations of quarks, discovery of the breakdown of symmetry of the laws governing matter and anti-matter, and the recognition that the electromagnetic force and the force governing radioactivity are different forms of a single underlying force. Today's research involves trying to understand why particles have the masses that they do, why there is more matter than anti-matter in the universe, and what makes up the 90 percent of matter in the universe that we know exists but is presently invisible to us [1].

1.2 Collider Detectors

Several collider facilities exist around the world. In Switzerland, CERN is home to numerous accelerator experiments. CERN's Large Hadron Collider (LHC), under construction, is an accelerator which will collide protons head-on at energies of approximately 14TeV. This energy is sufficient to allow scientists to recreate the conditions prevailing in the universe just 10^{-12} seconds after the "Big Bang". It will also collide beams of heavy ions such as lead with a total collision energy in excess of 1,250TeV, about thirty times higher than at the Relativistic Heavy Ion Collider (RHIC) under construction at the Brookhaven Laboratory in the US [2].

In the United States, Brookhaven National Laboratory is home to the Relativistic Heavy Ion Collider (RHIC) [3]. Scheduled for completion in 1999, RHIC will collide heavy ions at energies of 100GeV in each beam. These collision energies are expected to be high enough to create a hot, dense plasma of quarks and gluons. This quark - gluon plasma (QGP) is thought to have existed in the early moments of the universe immediately after the Big Bang. Four main experiments and their associated detectors at RHIC include: Solenoidal Tracker At RHIC (STAR), PHOBOS Detector, Broad Range Hadron Magnetic Spectrometers Experiment (BRAHMS), and the Pioneering High Energy Nuclear Ion Experiment (PHENIX) detector.

STAR is primarily a large hadron detector. STAR will search for signatures of quark-gluon plasma (QGP) formation and investigate the behavior of strongly interacting matter at high energy density [3]. PHOBOS is a smaller detector designed to examine and analyze a very large number of unselected gold-gold collisions [3]. For each collision the detector gives a global picture of the consequences of the collision and detailed information about a small subset of the nuclear fragments ejected from the high energy density region. BRAHMS is a small detector, with emphasis on hadron detection. BRAHMS is designed to measure charged hadrons over a wide range of rapidity and transverse momentum to study the reaction mechanisms of the relativistic heavy ion reactions and the properties of the nuclear matter formed therein [3]. The PHENIX experiment and detector's primary goal is to detect a new phase of matter, the quark-gluon plasma (QGP), and to measure its properties. PHENIX emphasizes detection primarily of electrons, photons, and muons.

The scope of this thesis deals with the energy-channel electron energy measurement electronics associated with the PHENIX experiment's Ring Imaging Cherenkov (RICH) Detector. The RICH detector subsystem serves as one of the primary devices for the detection of electrons. The following sections seek to provide additional detail into the operation and requirements of the PHENIX detector and the PHENIX RICH subsystem, as well as to outline the objective of this thesis with respect to the RICH energy-channel front-end electronics requirements.

1.2.1 The PHENIX Detector

The "Big Bang" theory postulates that the universe began as a singularity, minute in size but containing enormous pressure and temperature. Within this singularity, the four fundamental forces of nature, including gravity, the strong and weak nuclear forces, and the electromagnetic force, are theorized to have been united into one force. During the expansion of the singularity, the universe transitioned through several stages in which the pressure and temperature dropped and the four forces separated.

Physicists believe that the universe existed as a Quark-Gluon Plasma (QGP) several microseconds after the Big Bang. During the QGP phase, separation of the weak nuclear force and the electromagnetic force may have occurred. A confirmation of this theory requires a direct study of the QGP. As a means to this end, the PHENIX experiment and detector is designed to re-create and measure the various types of particles and phases of matter associated with the QGP.

Figure 1.1 illustrates a cutaway view of the PHENIX detector, showing the location of the various detector subsystems. The PHENIX detector contains three instrumented spectrometers, or "arms", along with a set of inner detectors, which are

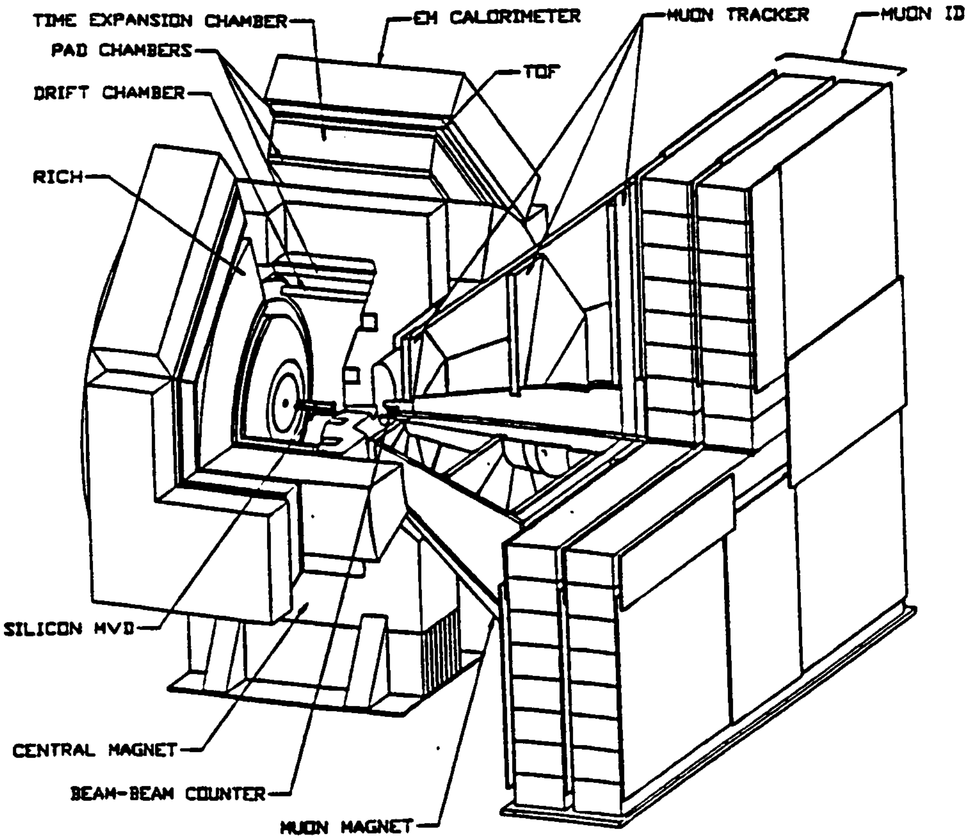


Figure 1.1 A Cutaway View Of The PHENIX Detector Indicating Various Subsystems And Their Locations [4]

centered around the particle beam collision point. A brief overview of the PHENIX detector subsystems is provided in the following sections.

1.2.1.1 PHENIX Muon Arm

The Muon Arm contains detectors which perform the functions of charged particle tracking and momentum analysis, along with muon identification. The Muon Arm contains a central magnet which establishes a radial magnetic field. Charged particles which emerge from the particle collision point in the polar angle range $10° \leq \theta \leq 35°$ pass through the pole tip of the central magnet. Those particles which emerge from the pole tip enter the Muon Arm. Particle momentum may be measured by observing the trajectories of the charged particles in a magnetic field using devices called drift chambers (muon tracking subsystem). The drift chambers are arranged in three stations, located at the entrance to, in the middle of, and at the end of the muon magnet field. Muon identification is handled by means of a muon identifier. The muon identifier consists of concrete absorber walls interleaved with tubes using cathode pad readouts, and is able to distinguish muons from pions and other particle collision shower products.

1.2.1.2 PHENIX Inner Detectors

The inner detector subsystems are able to measure the start time and vertex location of an event, as well as the event multiplicity and multiplicity distribution. The inner detectors are comprised of two main subsystems: the Beam-Beam Cherenkov counters and the Multiplicity Vertex Detector.

The two Beam-Beam Cherenkov counters are located upstream and downstream of the particle collision point, and are used in coincidence to provide a rough vertex location ($\sigma_z < 2$cm) and a precise event start time ($\sigma_t < 100$ps).

The Multiplicity Vertex Detector (MVD) directly surrounds the particle collision point, and consists of a two-layer barrel with two one-layer endcaps. The MVD measures the total event multiplicity (number of detectors which register a "hit" during a single beam clock), while also providing a precise ($\sigma_z < 500$um) vertex location.

1.2.1.3 PHENIX Central Arms

The PHENIX detector central arms are composed of four systems which perform the functions of charged particle tracking and momentum measurement, electron and photon energy measurement, and particle identification [4]. These systems include an electromagnetic calorimeter (EMCal), Time-of-Flight detector, Time Expansion Chamber (TEC), and a Ring-Imaging Cherenkov Counter.

The PHENIX electromagnetic calorimeter has been designed primarily to make precision measurements of promptly produced photons and electron pairs from nucleus-nucleus collisions at RHIC, with the objective of observing the QGP expected to form as a result of these collisions [3]. EMCal will use both Lead-Glass and Lead-Scintillator calorimeter units to discriminate between photons and electrons, and to measure both particle energy and position.

The PHENIX time-of-flight (TOF) counter serves as a particle identification device for hadrons. Charged hadrons are measured over a large momentum range with an array of high-resolution scintillators, which provide a means of separating pions and kaons.

The PHENIX Central Arms also contain two Ring-Imaging Cherenkov (RICH) detectors, positioned on the central arms between the inner and outer groups of tracking detectors as shown in Figure 1.2. The RICH detector subsystem serves as one of the primary devices for the identification of electrons. As the scope of this thesis involves the electron energy-measurement electronics for RICH, the following section will provide additional depth into the operation of the RICH detector.

1.3 PHENIX RICH Subsystem Overview

The Ring Imaging Cherenkov Detector subsystem serves as one of the primary detectors of electrons. The RICH detector is located outside of the PHENIX central magnet, and is positioned in radius between the inner and outer groups of tracking detectors. The RICH detector is filled with a Cherenkov radiator gas, either ethane or methane. The principle of operation is based on the detection of Cherenkov light emitted by a charged particle traveling through the Cherenkov radiator gas. In the RICH detector, these particles are typically the result of a collision.

When a charged particle travels faster than the speed of light in a dielectric medium, the polarized molecules of the medium emit electromagnetic radiation (Cherenkov photons) on a cone whose axis is the particle trajectory direction. The medium for the RICH detector is the Cherenkov radiator gas. The opening angle of the cone is related to the particle velocity and the refractive index of the traversed medium.

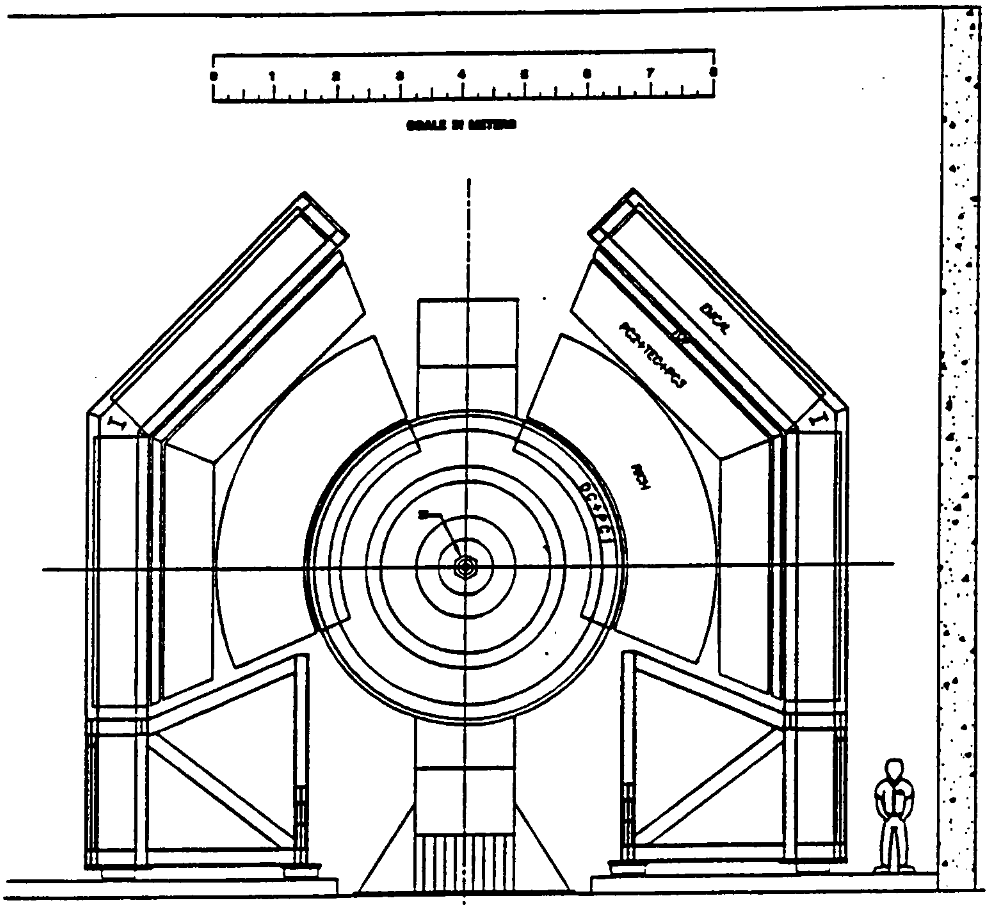


Figure 1.2 A Cross Section View Of PHENIX Through The Nominal Collision Point With Subsystems Labeled On The Right Central Arm [4]

Cherenkov radiation is emitted only if the particle's velocity upon entering the medium is greater than the speed of light in the medium. For each particle's mass (electron, positron, high-momentum hadron), this radiation threshold corresponds to a different threshold in momentum. By utilizing momentum information from the tracking detectors, particle identification is possible.

Cherenkov photons generated by charged particles proceed outwards on their cone trajectory, until finally striking one of the electron arm mirrors. Figures 1.3 and 1.4 indicate the geometry of the RICH optics and a typical Cherenkov photon trajectory.Each mirror is a section of a sphere of radius 4.0 meters, and is designed so as to focus the cone of Cherenkov photons onto a photomultiplier tube detector array.

Cherenkov photons from a good event, or collision, form a circular image at the focal plane on the photomultiplier tubes. The circular image is a result of the cone of photons intersecting the plane of the photomultiplier tubes. The center of this circular image allows determination of the direction vector of the photon's path. This direction vector is used to distinguish the few electron tracks from among the hundreds of charged pion tracks [4]. In order to ensure a unique matching of the light to the track, high segmentation of the photomultiplier tube arrays is necessary. The RICH detector utilizes 5120 channels of photomultiplier tubes (PMTs) in order to provide the required resolution for matching.

The PMTs produce a charge output in proportion to the number of photons striking the input. The RICH front end electronics act on this charge output to

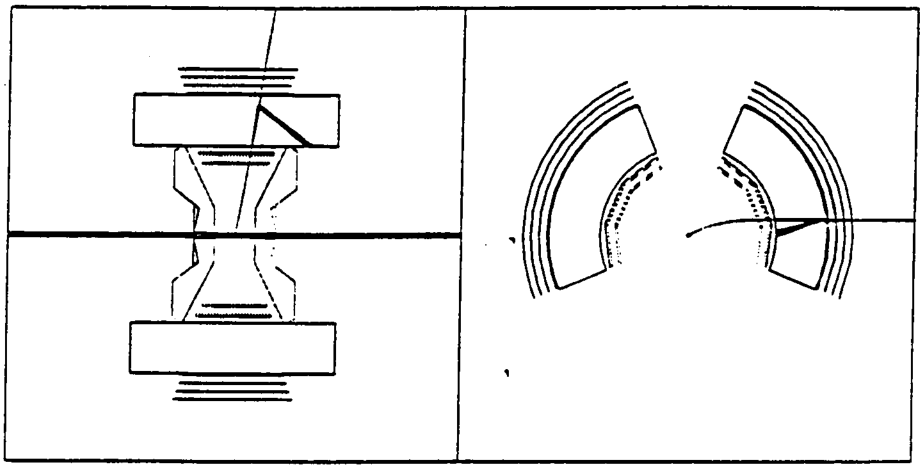


Figure 1.3 Cherenkov Photons Emitted By A 400 MeV/c Electron Are Reflected And Focused By The Mirror

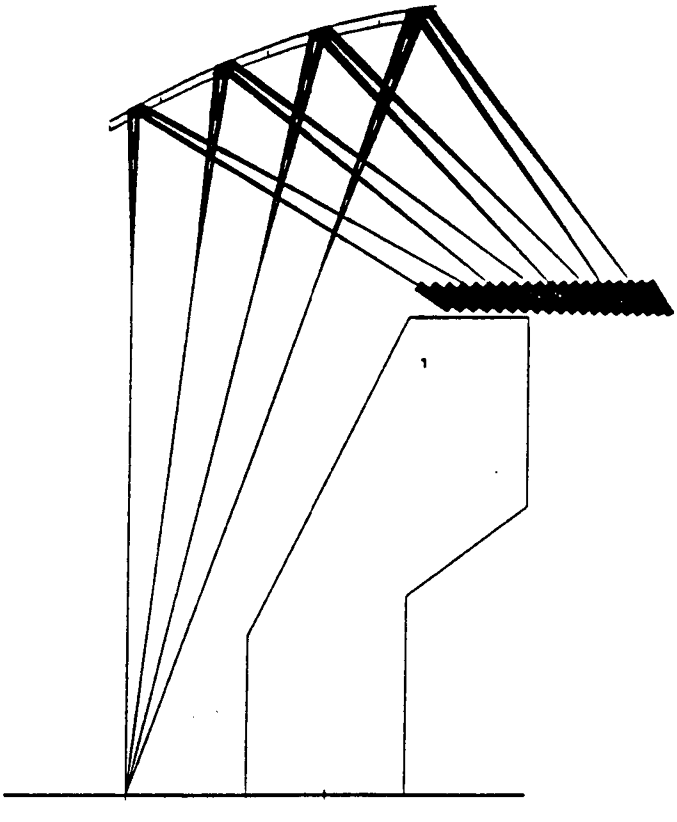


Figure 1.4 Schematic r-z View Of RICH And Its Optics. Components Shown Are: Mirrors, PMT Array, Central Magnet, Electron Tracks, And Cherenkov Rays

form both a timing measurement and an energy measurement for each PMT. A block diagram of the RICH front end electronics is shown in Figure 1.5.

The purpose of the timing electronics is to measure the time of occurrence of a collision, or event, with respect to a known reference. In this case, the known reference is the 9.4MHz RF clock used to accelerate the particle beam. This clock is more commonly known as the beam clock. The beam clock represents the rate at which "packets" of pre-accelerated particles are introduced into the main collider. These packets travel in opposite directions, and a collision between packets is referred to as a "beam crossing".

The PHENIX RICH timing electronics are active for each beam crossing. The beam crossing rate is 9.4 MHz, which requires the timing discriminator to trigger and return to its baseline in approximately 106ns. The timing electronics are able to trigger on an event with a timing resolution of $\sigma_t \approx 300$ps.

Similarly, the PHENIX RICH charge measurement, or "energy channel", electronics are required to be active for each beam crossing. The energy channel electronics consist of a charge-integrating amplifier followed by a variable gain amplifier (VGA). Since the integrator and VGA are required to be active for each beam crossing, the combined response of the integrator, VGA, and the following analog sum electronics must settle within one beam crossing, or approximately 106ns. The integrating amplifier integrates the output pulse from the PMT's amplifier. This integration provides a measurement of the number of Cherenkov photons striking the particular PMT, which in

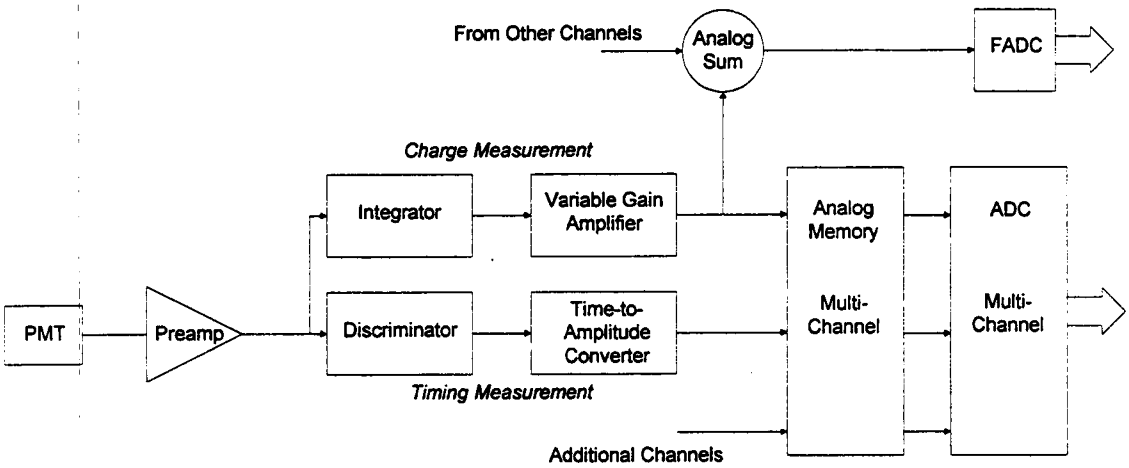


Figure 1.5 RICH Front End Electronics Block Diagram

turn is combined with the number of photons from adjacent PMTs to find Cherenkov rings for electron identification .

The VGA is used to equalize the gains of the photomultiplier tubes prior to forming analog sums for trigger purposes, using a 5-bit digital control over a 3:1 range. The VGA also allows compensation of the PMT gains as the PMTs age. In many detectors of this kind, the photomultiplier tube gains are matched by using an individual high-voltage programmable power supply for each PMT. These programmable high-voltage supplies are considerably more expensive than ordinary high-voltage supplies with a distribution network. By equalizing the gains of the 5120 different PMT channels in the electronics rather than in the supplies, a considerable cost savings is realized.

1.4 Thesis Objective

A CMOS integrating amplifier has been developed for use in the PHENIX Ring Imaging Cherenkov (RICH) detector. The amplifier, consisting of a charge-integrating amplifier followed by a variable gain amplifier (VGA), is an element of a photon measurement system comprising a photomultiplier tube, a wideband, gain-of-10 amplifier, the integrating amplifier, and an analog memory followed by an ADC and double correlated sampling implemented in software. The main focus of this thesis involves the RICH detector's energy channel integrating amplifier, which includes the active integrator amplifier and VGA.

In this work, a short overview of colliders, the PHENIX detector, the RICH subsystem, and the associated RICH front-end electronics are provided. The RICH subsystem energy channel front-end electronics requirements are discussed in detail, and the choice of the particular designs selected for the active integrator and VGA amplifiers are explored.

A detailed design methodology and analysis are presented for both the active integrator and VGA op-amps. The design requirements for both the integrator and VGA with respect to bandwidth, stability, power consumption, and noise are analyzed individually, and these results are compared with both a SPICE simulation, and with the actual performance of the IC op-amps themselves.

Since the integrator and VGA function together as a system, the overall system performance of both devices together is also characterized. The system transient response, risetime versus bandwidth, gain linearity, and output linearity with respect to input charge are characterized using both simulations and experimental results. The system noise response, including the effects of the double-correlated sampling on the system noise performance, is modeled both analytically and with SPICE. These results are compared to the noise performance of the actual system.

Chapter 2

RICH Energy Channel Electronics Requirements

2.1 Introduction

The PHENIX Ring Imaging Cherenkov (RICH) detector subsystem is used for electron identification using the Cherenkov photon ring. ωThis ring is generated in a gaseous Cherenkov radiator medium and is imaged onto a photomultiplier tube array via a spherical mirror. The RICH PMT array contains 5120 PMTs, which provide the required resolution necessary to match a given Cherenkov ring to its particular track. The highest level function of the charge measurement electronics and the associated software algorithms involves observing the array of 5120 PMTs to determine the location of the Cherenkov rings, which typically may overlap several sets of PMTs. The lowest level function of the electronics is to determine the number of photo-electrons generated in each photomultiplier tube during a given interaction. Each PMT connects to an individual integrating amplifier used for the purpose of measuring the charge output of that specific PMT.

Hamamatsu H3171S photomultiplier tubes are used for the RICH detector, operating at an approximate gain of 10^7. At this gain level, one incoming photoelectron generates a PMT charge output of 1.6pC. Because this is a relatively small charge, the charge integrating electronics need to be mounted on or near the detector to minimize any ill effects such as pickup, loss, or distortion due to a long cable. However, since the RICH detector uses a flammable gas for the Cherenkov radiator, remotely located electronics are desirable from a safety standpoint. The gas vessel is also somewhat inaccessible, and remotely located electronics facilitate access and repair convenience. For these reasons, a reasonable compromise would be to put a fast amplifier, capable of providing a gain of 10 into a 50Ω load, just outside the gas vessel. The remainder of the electronics, including the charge integrating amplifiers, will be located separately. The charge integrating amplifiers, one per PMT for a total of 5120, are grouped in multi-channel chips utilizing eight channels per chip.

2.2 RICH Electronics Requirements

The basic architecture of one individual PMT channel of the PHENIX RICH front end electronics is shown in Figure 2.1. Figure 2.2 illuistrates a block diagram of the RICH chip, which incorporates 8 channels per chip, and Figure 2.3 shows the RICH chip layout. Referring to Figure 2.1, the output of the PMT gain-of-10 preamp drives both a charge measurement channel and a timing channel. The outputs of the charge-measurement and timing channels are recorded in an analog memory clocked at the beam clock rate (9.4MHz). The output of the variable gain amplifier is also summed with the charge outputs from adjacent channel VGAs. This charge summation is performed so that the RICH detector trigger logic will be sensitive to Cherenkov rings which typically overlap no more than 20 sets of PMTs. The analog sum outputs are flash converted for

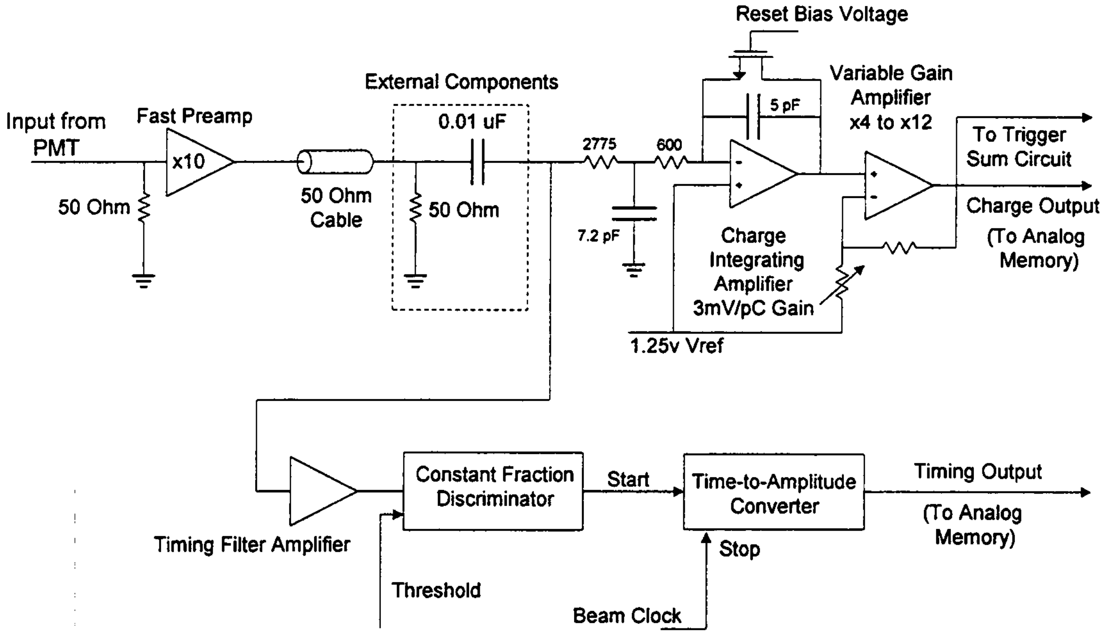


Figure 2.1 RICH Front End Electronics Energy Channel Diagram

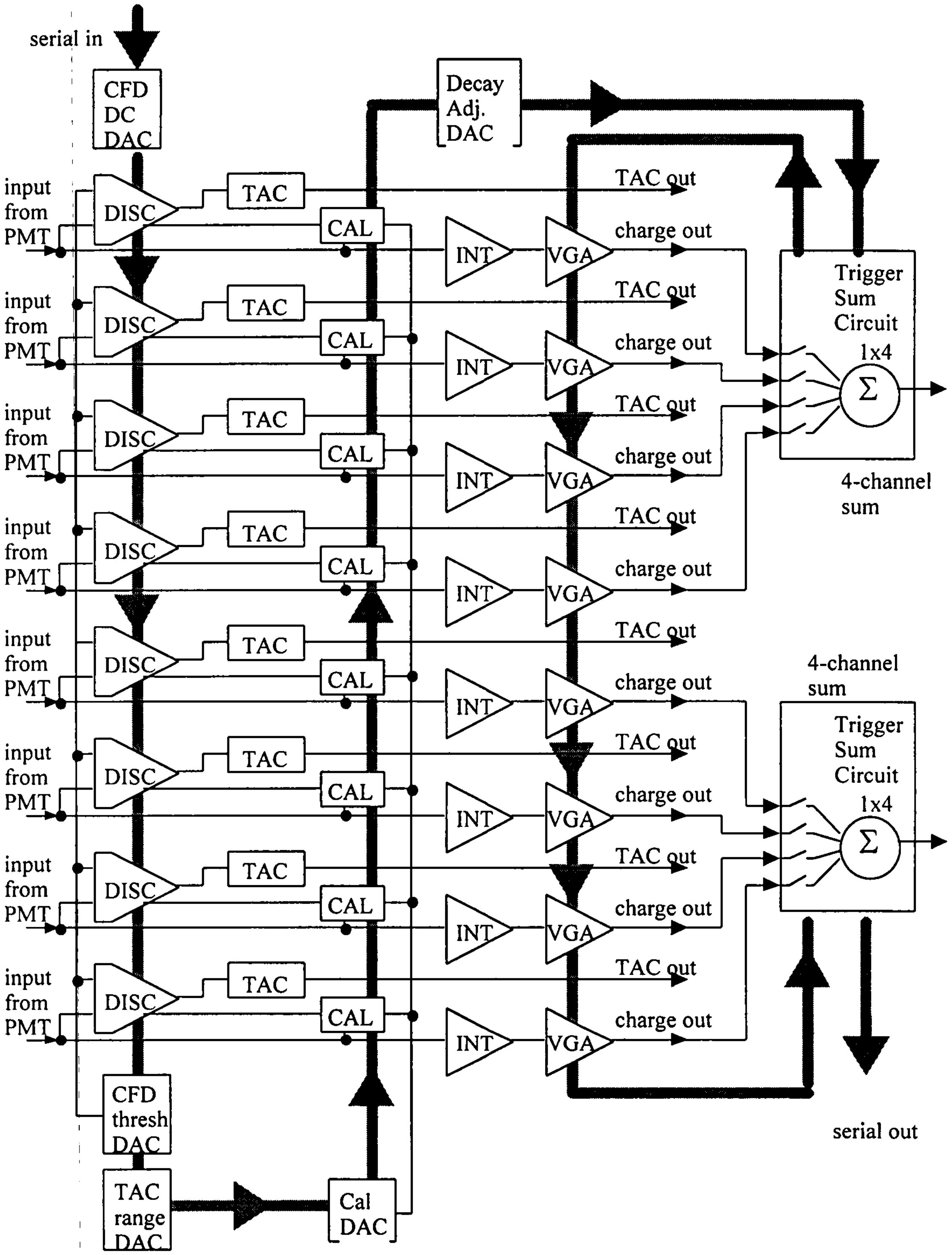


Figure 2.2 RICH Chip Block Diagram

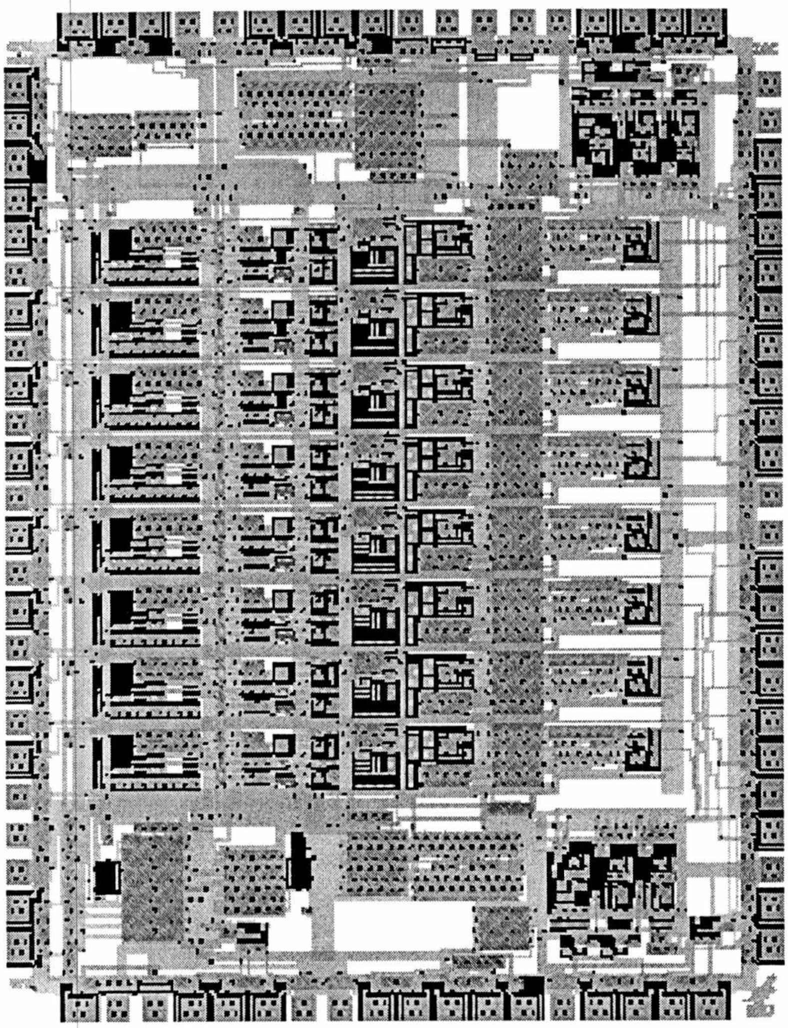


Figure 2.3 RICH Chip Layout

use in the experiment trigger logic. Information from the energy and timing channels stored in the analog memory is digitized on-demand by a multi-channel ADC. The PMT outputs, channel architecture, and the overall RICH operating modes place a number of constraints on the integrating amplifier.

The output of the analog summing circuit is digitized on every bunch crossing, or once every beam clock. The integrating amplifier, analog sum circuit, and flash ADC must therefore respond and settle in considerably less than one bunch crossing time, which is approximately 106ns. Since these devices operate in series, the integrating amplifier itself must respond in considerably less than 106ns. This requirement establishes the risetime specification for the overall integrating amplifier. In order for the analog summing circuits that follow the integrating amplifier to complete processing within one bunch crossing, the overall integrating amplifier risetime must be 20ns or less.

The noise contribution of the integrating amplifier is an important design consideration as well. The noise of the integrating amplifier should be sufficiently low so that the uncertainty in the number of photoelectrons measured is due to the statistics of the PMT, rather than the noise level of the amplifier, analog sum, or the digitization process. The RICH specifications call for a 1000:1 dynamic range at full scale. In other words, when the integrating amplifier is at maximum output voltage, the rms noise level of the amplifier should be 1000 times less than the full-scale amplifier voltage. The integrating amplifier is designed to be able to swing 3.25V at full scale. The rms noise of the integrating amplifier must be less than 3.25mV at the output based on this specification. Equivalently, the full-scale input charge is 160pC, yielding an input-referred rms noise level of 160fC.

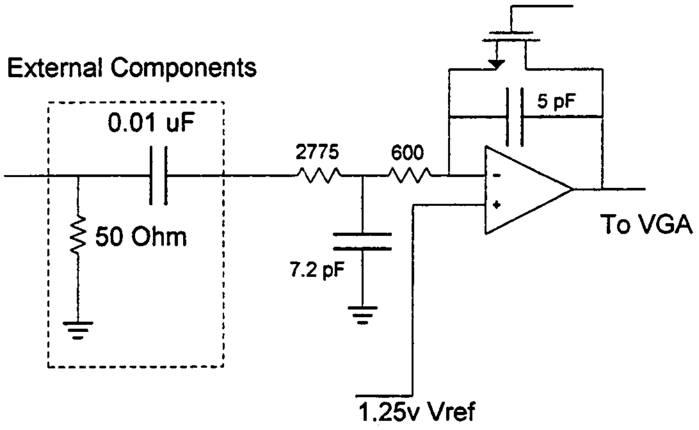
Several other design specifications shape the final integrating amplifier design. Both the integrator and VGA are specified for 5-volt operation. The VGA must compensate for the variable PMT gains over a 3:1 range, using a 5-bit digital control, while maintaining a constant risetime. The maximum output dynamic range of the VGA is 3.25V, corresponding to a nominal full-scale charge input of 160pC. The integrating amplifier, which includes the integrator op-amp and VGA, must provide a linear output over the full range of charge input. In addition, the integrating amplifier must provide a good 50-ohm termination for the PMT times-10 cable-driver amplifier, and the integrator reset time must be adjustable over a range of 5us to 100us. Table 2.1 summarizes the RICH integrating amplifier specifications.

2.3 Integrator and VGA Design Considerations

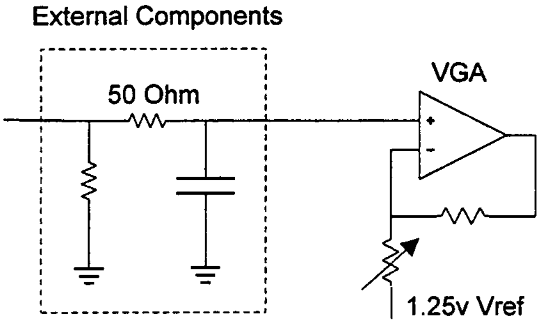
Two approaches to the integrator design have been investigated, as shown in Figure 2.4. The first approach involves the use of a passive integrator, which utilizes external components to achieve integration off-chip. The second approach involves on-chip integration using an active integrator. Both methods of integration have certain inherent advantages, and thus the selection of the active integration method as the method of choice achieves a balance of advantages with some compromise.

Table 2.1 RICH Integrating Amplifier Specifications

Item	Value	Comment
PMT Gain	~ 1x10e7	approximate
PMT Pulse	5ns risetime	
Maximum PMT Charge	16pC	~ 10 photoelectrons
PMT Amplifier Charge Gain	10	Charge delivered to 50 ohms divided by PMT charge
Maximum Charge Input to Energy Channel Electronics	160pC	16pC x 10
Integrator Reset Time	5us to 100us	Adjustable
Least Count (Volts)	3.5mV	At ADC input
Least Count (Charge)	0.16pC	At integrator input
Noise	< 1 Least Count rms	At integrating amplifier output
Integral Nonlinearity (Charge)	< 1%	Integrating amplifier voltage output vs charge input
Charge Sampling Interval	100ns - 200ns	
PMT Gain Variation	< 3:1	At nominal high-voltage setting
Integrating Amplifier Gain Programmability Range	3:1	Implemented via VGA
VGA Gain Control	5-bit	
VGA Gains	x4 to x12	x6.5 nominal
VGA Compensation Control	3-bit	Maintains ~15ns risetime for VGA
Full Scale Input Charge		
VGA = x4	260pC	
VGA = x6.5	160pC	
VGA = x12	87pC	



Active Integrating Amplifier System



Passive Integrating Amplifier System

Figure 2.4 Integrating Amplifier Architectures

The passive integration method locates the large integration capacitor off-chip. This method saves valuable chip area, and also maximizes the signal level by using the full PMT output pulse current for integration. The passive integrator also allows the integrator decay time to be easily adjusted by changing external passive components. The main advantage of the passive integrator, however, appears to be in the area of noise performance. The active integrator in general has a relatively large gain at low frequencies, making the active integrator susceptible to large low-frequency noise levels. Prior simulations done for the PHENIX lead-glass and lead-scintillator calorimeters using nearly-ideal amplifiers indicate that a factor-of-two better output signal-to-noise ratio may be possible when using the passive integrator circuit [5].

The active integrator implementation has been selected over the passive integrator for use in the PHENIX RICH energy channel integrating amplifier, primarily due to the 50-ohm termination provided by the active integrator, but also in light of efforts to reduce the integrator op-amp noise to meet the RICH noise specs. Since the RICH electronics are remotely located, the PMT array must rely on the individual cable-driver x10 amplifiers to deliver the PMT pulse to the integrating amplifier. In this configuration, the input impedance to the active integrator is very close to 50 ohms for all frequencies of interest. This provides a much better termination for the cable driver than that provided by the passive integrator circuit. This termination is necessary, since any ringing would likely distort the charge linearity of the integrator, as well as making timing (discrimination) measurements difficult.

The nature of the active integrator's 50 ohm termination leads to a disadvantage with respect to the amount of signal charge available to be integrated. A tradeoff occurs with respect to the integrator input resistance and the integrating capacitor size. As the input resistance drops, the integrating capacitor must be made larger to preserve the output dynamic range of the integrator. In the RICH integrator, approximately 98.4% of the available signal charge is lost in the terminating resistor. A larger integrating capacitor is not a practical solution on a reasonably-sized die. The maximum integrating capacitor size is also limited by the output drive current of the integrator op-amp. The minimum integrator input resistance is therefore fixed by the integrating capacitor size and the op-amp output drive current, the required output dynamic range of the integrator, and the maximum input pulse from the PMT amplifier.

The RICH electronics specifications also call for an adjustable integrator reset time, varying from 5us to 100us. The integrator reset time is the time required for the integrator to return to its baseline (DC bias) output setting. The integrator reset time is typically much longer than the integrator risetime, which is desirable for the purpose of sampling the integrator output before the reset causes an appreciable error, although this error might be compensated for in the sampling software. However, a long integrator reset time, which causes little sampling error, is detrimental to the low-frequency noise performance of the integrating amplifier. Hence the desire for an adjustable reset time, which achieves a balance between sampling error, time-to-reset, and noise performance.

The design of the active integrator lends itself readily to the implementation of an adjustable integrator reset control. Instead of using a fixed resistor in the feedback path, an N-channel MOSFET biased in the linear region is used to control the integrator reset time. The FET presents several advantages over a comparable fixed resistor. The FET provides a nominal resistance of approximately 500K ohms, which would be impractical to achieve using a fixed resistor due to chip area constraints. The FET also provides a convenient means of adjusting the integrator reset time. By modulating the FET's gate voltage, the effective resistance of the FET in the linear region may be varied so as to provide the required reset time control. In addition, this gate voltage modulation may be achieved by utilizing an on-chip DAC, which automates the reset-time adjustment and negates any external component swaps required in a passive integrator, providing both speed and ease of adjustability.

The VGA utilizes a standard voltage-feedback topology. The feedback resistor is fixed, and the 5-bit gain control is achieved through the use of 5 parallel CMOS switches which provide 31 different levels of resistance between a 1.25V reference and the amplifier's inverting input. Due to the voltage feedback topology, the amplifier's bandwidth and hence risetime vary as the gain is varied. This risetime variation is minimized by using variable compensation, allowing the bandwidth to remain fairly constant as the gain changes over the 3:1 range.

A VGA utilizing a current feedback topology might achieve the constant-bandwidth result without the need for the additional variable compensation. In a current feedback topology, the amplifier's inverting input pin impedance is typically low compared to the external fixed resistors which determine the gain. This low inverting input impedance allows for gain changes to be made via the external resistors, without significantly affecting the poles in the loop transmission, which allows for a relatively constant bandwidth as gain changes. The current feedback amplifier also typically has a much higher slew rate than a voltage feedback amplifier, due to the ability of the feedback current to directly drive the amplifier's internal dominant capacitance.

With respect to the RICH electronics specifications, the necessary slew rate for the VGA is well within the performance boundaries attainable for a typical voltage feedback amplifier. The voltage feedback topology does require variable compensation to allow constant bandwidth vs. gain. The RICH VGA is required to operate in a non-inverting configuration, which implies that the inverting input voltage will move as the input voltage moves. This can complicate the biasing in a current-feedback design. The voltage feedback configuration is therefore somewhat simpler to implement in a non-inverting application. The RICH VGA uses a 3-bit adjustable right-half-plane-zero compensation method to maintain the amplifier bandwidth. In addition to maintaining the bandwidth, the compensation has been tuned to provide a non-ringing transient pulse response for the range of gains, since the amplifier's settling time must not limit the desired sampling interval. The voltage feedback topology utilized for the RICH VGA is similar to the VGA used for the PHENIX Electromagnetic Calorimeter [6]. The RICH VGA is designed with PMOS inputs for handling input signals closer to ground, and has been recompensated and re-biased for lower power dissipation. Since the time required to tailor the voltage feedback design to the RICH specifications was relatively short, the choice of this voltage feedback, variable compensation topology provides the advantage of a shortened design cycle and a simplified design, along with a tuned amplifier response suitable for all necessary RICH gain ranges.

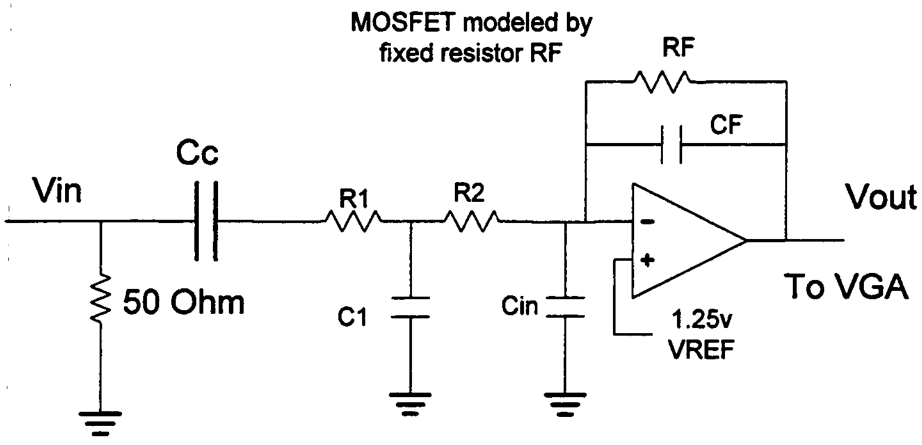
Chapter 3

RICH Integrator Design

3.1 Integrator Requirements and Design Considerations

The charge integrator design used for the PHENIX RICH detector energy channel is similar to prototypes made for the PHENIX lead scintillator and lead glass calorimeters [5]. A diagram of the RICH integrator is presented in Figure 3.1. The PHENIX RICH integrator offers some improvements over the earlier PHENIX integrators with respect to noise, in an effort to narrow the signal-to-noise ratio performance gap between the active integration method and the passive integration method. Relative to earlier PHENIX active integrator designs, the input resistance of the RICH integrator has been decreased, allowing a larger percentage of the input charge to be integrated, which improves the input signal-to-noise ratio by increasing the signal. Also, the equivalent input noise for the RICH integrator op-amp has been lowered in an effort to meet the RICH noise specification of 3.5mV rms at the VGA output. The target input e_n for the RICH integrator op-amp is $\leq$ 10nV/Hz$^{1/2}$ in order to meet this specification, based on early simulation results. The integrator op-amp's equivalent input noise voltage has been lowered by increasing the g_m of the input differential pair, achieved through device size scaling and through increased differential pair bias currents.

The nominal charge gain for the integrating amplifier is determined by the nominal full-scale charge input of 160pC, the nominal gain of the VGA, and the



Cc = 0.01u
R1 = 2775
R2 = 600
RF = 559k nominal

C1 = 7.2pF
Cin (op-amp input capacitance) = 1pF
CF = 5pF

RICH Active Integrator Amplifier

Figure 3.1 RICH Active Integrator

maximum output dynamic range of the VGA of 3.25V. The VGA gain spans the range from 4 to 12, with a gain of 6.5 considered nominal with respect to the expected PMT output level. The integrator must therefore be able to produce a nominal dynamic voltage swing of 0.5 volts, which corresponds to the VGA dynamic range of 3.25V divided by the VGA nominal gain of 6.5. The peak required dynamic output voltage swing of the integrator is approximately 0.81V, which corresponds to the VGA dynamic range of 3.25V divided by the VGA minimum gain of 4. The integrator must remain linear over this region.

The overall integrating amplifier, which includes the integrator and VGA, has a target risetime of approximately 20ns. The specification for the integrator alone calls for a 10ns or less risetime. Since the integrator must remain linear over a 0.81V output dynamic range, and must swing this voltage range in 10ns, the minimum required positive slew rate for the integrator op-amp is 81 volts per microsecond. The current requirements necessary to achieve this slew rate must also be balanced with the power dissipation requirement of roughly 10 milliwatts. The negative slew rate is not important, since the integrator must only respond to negative-going input pulses which create a positive-going output pulse.

The integrator feedback capacitor has been chosen to be 5pF, which allows a reasonable compromise between chip area and the amount of signal to be integrated. As the feedback capacitor becomes larger, the integrator input resistance can be made smaller, given the fixed dynamic output range of the integrator. This allows a greater percentage of the PMT charge to be integrated, although at the cost of increased chip area. Given the 5pF integrator feedback capacitor, the input resistance to the integrator is then specified such that the proportion of the nominal full-scale PMT charge which is integrated yields a dynamic range of 0.5 volts at the integrator output. This required integrator input resistance is approximately 3150 ohms. (The integrator input resistance, extracted by SPICE, is approximately 3375 ohms). The nominal maximum charge of 160pC from the PMT thus splits between the 50 ohm terminating resistor and the 3k integrator input impedance, yielding approximately 2.6pC of full-scale charge available for integration.

Capacitor C_c is a coupling capacitor which serves as a DC blocking capacitor between ground and the 1.25V integrator reference. From a noise standpoint, the value of C_c should be minimized, since the pole/zero in the non-inverting gain created by C_c and R_{in} limits the low-frequency amplitude of the non-inverting gain, which in turn limits any low-frequency noise created by the op-amp and the 1.25V reference. This low-frequency noise source is significant, and is covered in more detail in Chapter 5. Minimizing C_c in order to limit the integrator's low-frequency bandwidth has a detrimental effect on the integrator's reset time, however. As C_c drops in value below approximately 0.01uF, the $R_{IN}C_C$ time constant approaches the R_FC_F time constant, resulting in a loss of reset time adjustability via the reset MOSFET gate bias voltage and an increasing dependence of the reset time on the coupling capacitor. Since an adjustable integrator reset time is a requirement, a balance must be achieved between low-frequency noise rejection and reset time adjustability. From SPICE simulations of the integrating amplifier, and from chip testing using a noisy LM385 1.25V reference for the integrator, a 0.01uF coupling capacitor allows for an adjustable integrator reset time which just meets the RICH specs, achieving a good balance between the reset time adjustability specification and low-frequency reference noise rejection.

The capacitor C_1 serves as a pre-integration capacitor, slowing the incoming falling edge from the PMT so as not to overdrive the op-amp input. Early simulations revealed that the 2.5ns falltime from the PMT amplifier was fast enough to overdrive the differential input of the integrator op-amp, causing the integrator output to slew. The unwanted slewing results in a loss of charge and a corresponding non-linear integrator output vs. charge input. Capacitor C_1 also serves to improve the phase margin of the overall integrator circuit, providing lead compensation with resistor R_2 which delays the loop phase shift relative to the loop gain crossover point. This compensation becomes beneficial especially as the load capacitance increases. Without the 7.2pF capacitor C_1, the integrator circuit of Figure 3.1 has a phase margin of approximately 24 degrees. With capacitor C_1, the integrator phase margin is increased to approximately 55 degrees.

The charge gain from input to output for the integrator is shown in Equations 3.1 and 3.2. This derivation is based on the circuit given in Figure 3.1, neglecting C_{IN} and assuming an ideal op-amp. The input current I_{IN} is assumed to flow out of the circuit node defined by V_{IN} in Figure 3.1. The 50-ohm termination resistor is defined in Equation 3.1 as R_T. The low-frequency corner at 4647Hz is set by the sum of R_1 and R_2, and the coupling capacitor C_C. The high-frequency corner at 56943Hz is set by R_F and C_F.

$$\frac{V_{OUT}}{I_{IN}} = \frac{(R_F)(sR_T C_C)}{(1+sR_F C_F)\left[1+s(R_2C_1+R_1C_C+R_2C_C+R_TC_C)+s^2(R_1R_2C_1C_C+R_TR_2C_1C_C)\right]} \tag{3.1}$$

$$\frac{V_{OUT}}{I_{IN}} = \frac{\left(j\frac{f}{318300Hz}\right)(R_F)}{\left(1+j\frac{f}{56943}\right)\left(1+j\frac{f}{4647}\right)\left(1+j\frac{f}{44.67MHz}\right)} \tag{3.2}$$

The pole at 56943Hz, set by R_FC_F, sets the risetime for the charge transfer function shown by Equation 3.2. Equation 3.2 is useful from a noise bandwidth perspective, since the zero at DC and the two dominant poles appear also in the transfer function from the integrator op-amps non-inverting input to the output. This zero and two poles establish the low-frequency bandwidth for the integrator. Adjustment of the coupling capacitor C_C up or down in value moves the pole at 4647Hz down or up, respectively. For example, reducing C_C shifts the pole at 4647Hz towards the pole at 56943Hz. As this occurs, the integrator reset time, which is designed to be dependent on R_FC_F, becomes increasingly dependent on the value of the coupling capacitor C_C. However, the integrator's low frequency noise bandwidth decreases as C_C decreases also. Figure 3.2 illustrates a plot of Equation 3.1 vs. frequency.

3.2 Integrator Op-Amp Design Topology and Compensation

The op-amp used for the RICH integrator is a standard differential-pair, single-ended output amplifier fabricated in a 1.2μ CMOS Orbit process. Figure 3.3 shows the RICH integrator op-amp in detail. This op-amp is based on the PHENIX Lead-Scintillator integrator op-amp [5], but has revised bias currents, device sizes, and compensation to meet the RICH specifications. PMOS input devices are used in the differential pair in order to allow biasing the inputs closer to the negative (ground) supply rail. Nominal supply voltages are 5V and ground, with the inputs biased at 1.25V.

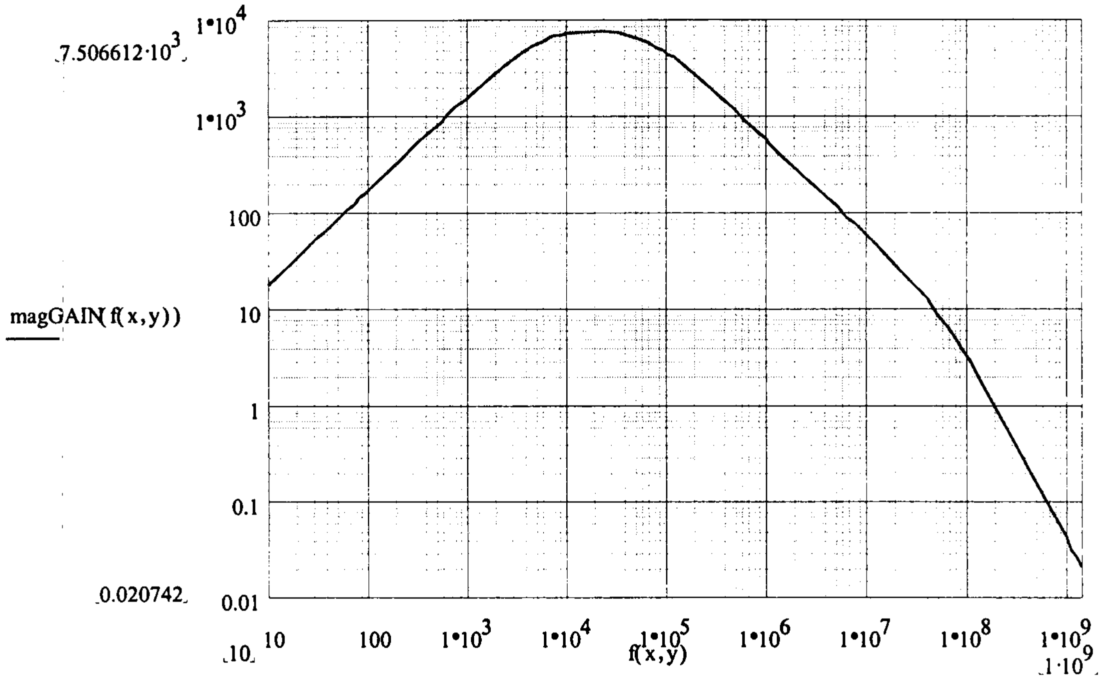


Figure 3.2 Plot of Equation 3.1, Active Integrator Charge Gain Transfer Function

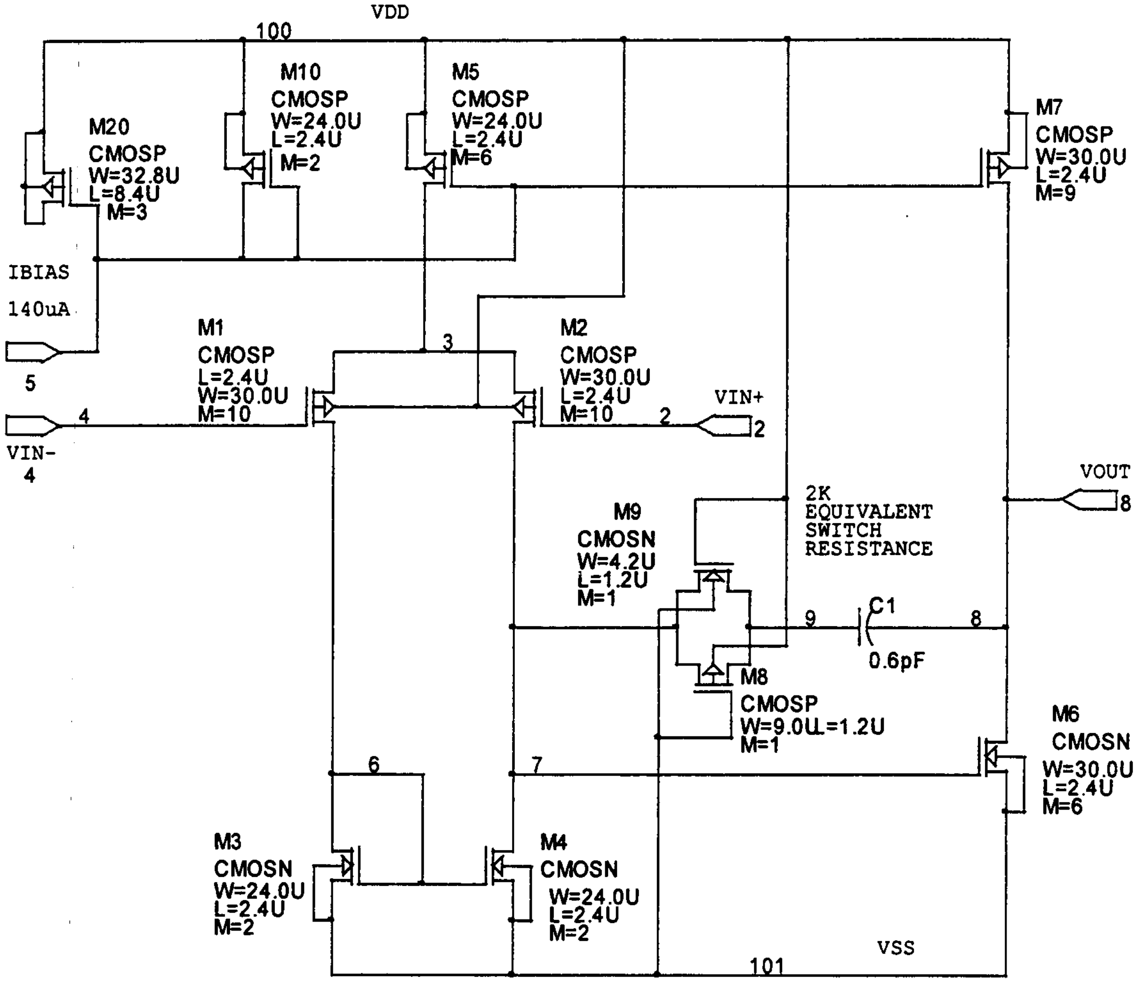


Figure 3.3 RICH Integrator Operational Amplifier

The nominal bias current is 140μA, resulting in 6.8mW of power dissipation. The power dissipation may be reduced somewhat by reducing the differential pair bias currents, however this results in a higher equivalent input thermal noise. Raising the differential pair bias current reduces the input equivalent thermal noise, however this design is somewhat constrained by power dissipation limitations dictated by the thermal limitations of the final package. In this respect, the integrator power dissipation is desired to be minimized. Section 3.4 deals with the op-amp's differential pair design for low-noise performance in more detail.

The op-amp's positive slew rate is dictated primarily by the bias current in output device M7 and the load capacitance. The load capacitance is large enough that the differential pair bias current and the compensation capacitor C_1 do not determine the slew rate. As the op-amp output swings positive, device M6 turns off and M7 supplies its full bias current to the load. Biasing M7 at approximately 800μA, with a load capacitance of 8pF yields a slew rate of 100 volts per microsecond, exceeding the minimum slew rate spec of 81 volts per microsecond.

MOSFETs M8 and M9, along with capacitor C_1 form the compensation for the integrator op-amp. Without internal compensation, the integrator op-amp in Figure 3.3 is unstable in a unity-gain configuration, with a negative phase margin at unity gain. Without internal op-amp compensation, and when used in the integrator circuit of Figure 3.1 with a load capacitance of 8pF, the overall integrator circuit has a phase margin of approximately 25 degrees. Clearly, internal op-amp compensation is required to improve the overall integrator circuit phase margin.

The reason for the integrator op-amp's poor uncompensated phase margin is related to the amplifier's dominant poles, which occur at the drain of M2 and at the output. Uncompensated, the poles are relatively close together, causing excessive phase shift relative to the open-loop gain 0-dB point. One compensation technique, the Miller compensation method, may be used to split these poles apart, delaying the phase shift for an improved phase margin.

The Miller compensation method involves placing a capacitor from the output to the input of the second transconductance stage, or from the drain to the gate of device M6. This "Miller" capacitor affects both dominant amplifier poles. The gain of the second stage amplifies the second stage gate-to-drain capacitance via the Miller effect, significantly increasing the capacitance at the drain of M2. This moves the pole at the drain of M2 lower in frequency by a significant amount. The Miller capacitor also moves the output pole to a higher frequency, with the desired result of delaying the open-loop phase shift relative to the open-loop zero-dB gain crossover point.

In addition to separating the amplifier's dominant poles, the Miller capacitor also adds a zero to the open-loop amplifier response. This zero occurs in the right-half plane, and is located at $Z_1 = g_{m6}/C_{Miller}$. The right-half plane zero can be detrimental to the amplifier's stability, since it causes the amplifier's open-loop gain Bode response to increase, while simultaneously causing additional open-loop phase shift . These two negative effects work in conjunction to potentially decrease the amplifier's phase margin.

To compensate for right-half plane zero, a nulling resistor is placed in series with the Miller capacitor. Referring to Figure 3.3, M8 and M9 together form a CMOS switch which serves as a nulling resistor to compensate for the right-half plane zero formed by compensation capacitor C_1. The combination of the nulling resistor, compensation capacitor, and output gain stage form three main poles and one zero. These pole/zero locations may be approximated by [7]

$$p_1 = \frac{-1}{2\pi(1+g_{m6}R_2)R_1C_{1comp}} \tag{3.3}$$

$$p_2 = \frac{-g_{m6}C_{1comp}}{2\pi(C_1C_2 + C_{1comp}C_1 + C_{1comp}C_2)} \tag{3.4}$$

$$p_3 = \frac{-1}{2\pi(R_zC_1)} \tag{3.5}$$

$$z_1 = \frac{1}{2\pi\left(\dfrac{1}{g_{m6}} - R_z\right)} \tag{3.6}$$

where R_1 = Total equivalent resistance at drain of device M2 ≅ 48.1k

R_2 = Total equivalent resistance at output ≅ 29.5k

R_z = Nulling resistor value ≅ 2k

C_1 = Total capacitance at drain node of device M2 ≅ 5.5pF

C_{1comp} = Compensation capacitor value ≅ 0.65pF

C_2 = Total equivalent capacitance at output ≅ 8.4pF

This analysis does not completely consider the effects of the gate-to-drain capacitance of output device M6. C_{GD6} provides a small amount of Miller compensation, but is not connected in series with the nulling resistor as is the compensation capacitor. C_{GD6} is very small (~50fF) compared to compensating capacitor C_{1comp}, but sees a Miller gain of approximately 85 around the second stage. This Miller capacitance is grouped in with the C_1 capacitance as an approximation, as in Equation 3.8. Also, a fourth amplifier pole exists at the source of devices M1 and M2, located at approximately 150MHz.

The total equivalent resistance R1 is equal to the parallel output impedance of devices M2 and M4. The output resistance of device M4 is found to be approximately 286k from SPICE. The overall output resistance of device M2 is approximately 57.8k, and the node resistance at the drain of device M2 is represented by the parallel combination of the output resistance of M2 and M4, or 48.1k. The transconductance of device M2, g_{m2}, is 0.00128 A/V.

The overall output impedance is given by the parallel combination of the output impedances of devices M6 and M7. With r_{o6} equal to 85k and r_{o7} equal to 45.3k, the total output resistance is 29.5k. The CMOS switch resistance, as modeled by SPICE, is approximately 2k.

C_1, the total capacitance at the drain node of M2, consists of the sum of the capacitances looking in the drains of devices M2 and M4, and the capacitance looking in the gate of device M6. The capacitance looking in the drain of device M2, and M4 also, may be represented by

$$C_{DTotal} = C_{DG} + C_{DB} \tag{3.7}$$

where C_{DG} primarily consists of overlap capacitance. The capacitance looking into the gate of device M6 may be represented by

$$C_{GTotal} = C_{GS} + C_{GB} + C_{GD}^{*} \tag{3.8}$$

In this analysis, $C_{GD6}(1-A_2)$ is grouped in with C_1 as an approximation, and the total contribution to C_1 by device M6 is given by $C_{GS6} + C_{GB6} + C_{GD6}(1-A_2)$, where A_2 is the gate to drain gain of device M6. A_2, given by $g_{M6}R_2$, is equal to approximately 85. Capacitance C_1 is therefore given by

$$C_1 = C_{DG2} + C_{DB2} + C_{DG4} + C_{DB4} + C_{GS6} + C_{GB6} + C_{GD6}(1 - A_2) \cong 5.5pF \qquad \textbf{(3.9)}$$

Similarly, assuming a load capacitance of 8pF, the output capacitance C_2 is given by

$$C_2 = C_{DG7} + C_{DB7} + C_{DG6} + C_{DB6} + C_{LOAD} \cong 8.3975pF \qquad \textbf{(3.10)}$$

The transconductance of device M2 is approximately 0.00128 A/V, and the transconductance of the second stage device M6 is approximately 0.00287 A/V. Using these parameters, along with the output impedances previously calculated, yields an open-loop gain of 5212, given by the product ($g_{M2}g_{M6}R_1R_2$). The gain bandwidth product, assuming no load capacitance, is approximately 200MHz as modeled by SPICE.

The approximate amplifier poles, as given by Equations 3.3 through 3.5, occur at 59400Hz, 5.38MHz, and 14.4 MHz respectively. A fourth amplifier pole, associated with the source node of the differential pair input devices, occurs at approximately 150MHz. Equation 3.6 shows the compensated location of the zero, which is originally in the right-half plane. Equation 3.6 presents two options to deal with the negative effects of the right-half plane zero. One possible compensation method would be to make R_z equal to $1/g_{m6}$, removing the right-half plane zero altogether. Another option is to make R_z greater than $1/g_{m6}$, which has the effect of moving the right-half plane zero into the left-half plane. Relocating the zero to the left-half plane has the advantage of allowing the designer to place the zero on top of an existing amplifier pole, cancelling the effect of that pole. R_z is selected in this design through simulations so as to provide the best transient response. R_z is equal to approximately 2k and with $1/g_{m6}$ equal to 348, the zero is located at 148MHz in the left-half plane, close to the 150MHz pole. This compensation method produces a very good transient pulse response for the overall integrator circuit.

Equation 3.11 shows the integrator op-amp loop transmission with approximate pole and zero locations, based on the above hand-calculated values and including the 8pF load capacitance. Figures 3.4 and 3.5 show the HSPICE loop transmission with and without the load capacitance, respectively. All HSPICE simulations utilize the BSIM model. With no load capacitance, the integrator op-amp, at unity gain, has a phase margin of approximately 32 degrees. Section 3.3 provides a detailed stability analysis of the overall integrator circuit of Figure 3.1, using the results obtained in this section for the integrator op-amp.

$$T_{OP-AMP} = \frac{-5212\left(1+j\dfrac{f}{148MHz}\right)}{\left(1+j\dfrac{f}{59400}\right)\left(1+j\dfrac{f}{5.58MHz}\right)\left(1+j\dfrac{f}{14.4MHz}\right)\left(1+j\dfrac{f}{150MHz}\right)} \tag{3.11}$$

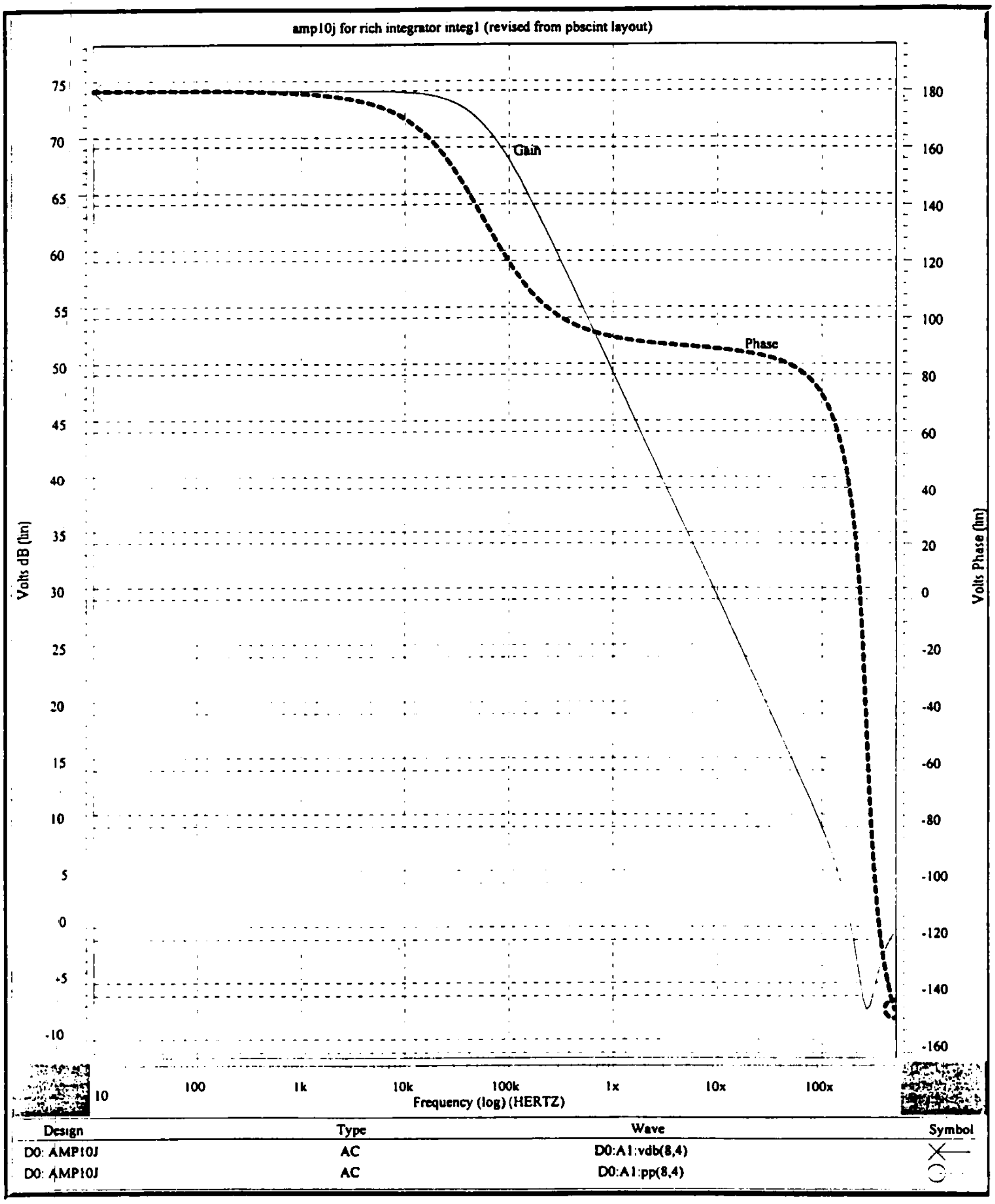
3.3 Overall Integrator Circuit Stability Analysis

The stability analysis presented in this section refers to the overall integrator circuit of Figure 3.1. The feedback MOSFET is modeled as a fixed resistor for simplicity, and the input capacitance of the op-amp is included for completeness.

Breaking the feedback loop and applying circuit analysis techniques, the loop transmission for the integrator circuit is given by

$$T_{INTEGRATOR} = \frac{\left[1+as+bs^2\right]\left(1+sR_FC_F\right)\left(T_{OP-AMP}\right)}{1+cs+ds^2+es^3} \tag{3.12}$$

where



Design	Type	Wave	Symbol
D0: AMP10J	AC	D0:A1:vdb(8,4)	✕
D0: AMP10J	AC	D0:A1:pp(8,4)	○

Figure 3.4 RICH Integrator Op-Amp Loop Transmission, No Load Capacitance

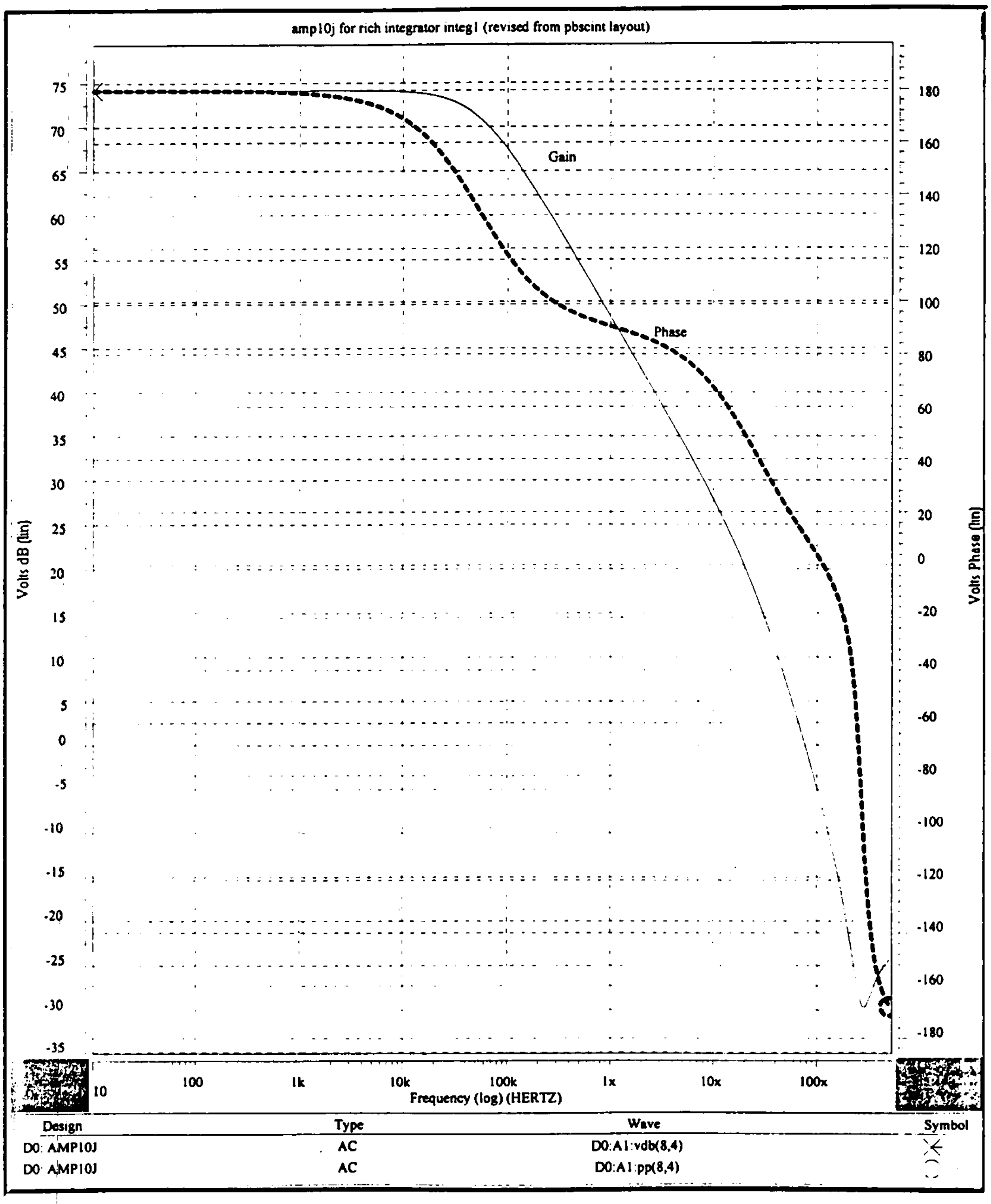


Figure 3.5 RICH Integrator Op-Amp Loop Transmission, 8pF Load Capacitance

$$a = R_{IN}C_C + R_2C_1 + R_2C_C \tag{3.13}$$

$$b = R_{IN}R_2C_1C_C \tag{3.14}$$

$$c = R_F(C_F + C_1 + C_C + C_{IN}) + R_{IN}C_C + R_2C_1 + R_2C_C \tag{3.15}$$

$$d = R_FC_F(R_{IN}C_C + R_2C_1 + R_2C_C) + R_{IN}R_2C_1C_C + R_F(R_{IN}C_1C_C + R_{IN}C_{IN}C_C + R_2C_{IN}C_1 + R_2C_{IN}C_C) \tag{3.16}$$

$$e = R_FR_{IN}R_2C_1C_C(C_F + C_{IN}) \tag{3.17}$$

and

$$R_{IN} = R_1 + 50\Omega \text{ termination resistor} \tag{3.18}$$

Using nominal values for R_{IN} of 2825, $R_2 = 600$, $R_F = 559K$ (assuming a gate bias voltage of 4V), $C_C = 0.01uF$, $C_1 = 7.2pF$, $C_F = 5pF$, and $C_{IN} = 1pF$, and including the expression for $T_{OP\text{-}AMP}$, the overall integrator loop transmission represented by Equation 3.12 may be expressed as

$$T = \left[\frac{\left(1+j\frac{f}{4647}\right)\left(1+j\frac{f}{44.7MHz}\right)\left(1+j\frac{f}{56900}\right)}{\left(1+j\frac{f}{28}\right)\left(1+j\frac{f}{4.1MHz}\right)\left(1+j\frac{f}{84.8MHz}\right)}\right]\left[\frac{-5212\left(1+j\frac{f}{148MHz}\right)}{\left(1+j\frac{f}{150MHz}\right)\left(1+j\frac{f}{59400}\right)\left(1+j\frac{f}{5.58MHz}\right)\left(1+j\frac{f}{14.4MHz}\right)}\right] \tag{3.19}$$

The lefthand brackets in Equation 3.19 contain the 3 poles and 3 zeroes contributed by the feedback network, while the righthand brackets contain the 4 poles and 1 zero contributed by the op-amp. Figures 3.6, 3.7, 3.8, and 3.9 graphically present the frequency response of the active integrator. Figure 3.6 shows a Bode plot of Equation 3.19, with a gate bias voltage of 4 volts corresponding to an equivalent R_F of 559k. Figure 3.7 also refers to Equation 3.19, except with a gate bias voltage of 3 volts corresponding to an equivalent R_F of 2.9 Meg ohms. From Figures 3.6 and 3.7, it is evident that Equation 3.19 models the frequency response adequately below about

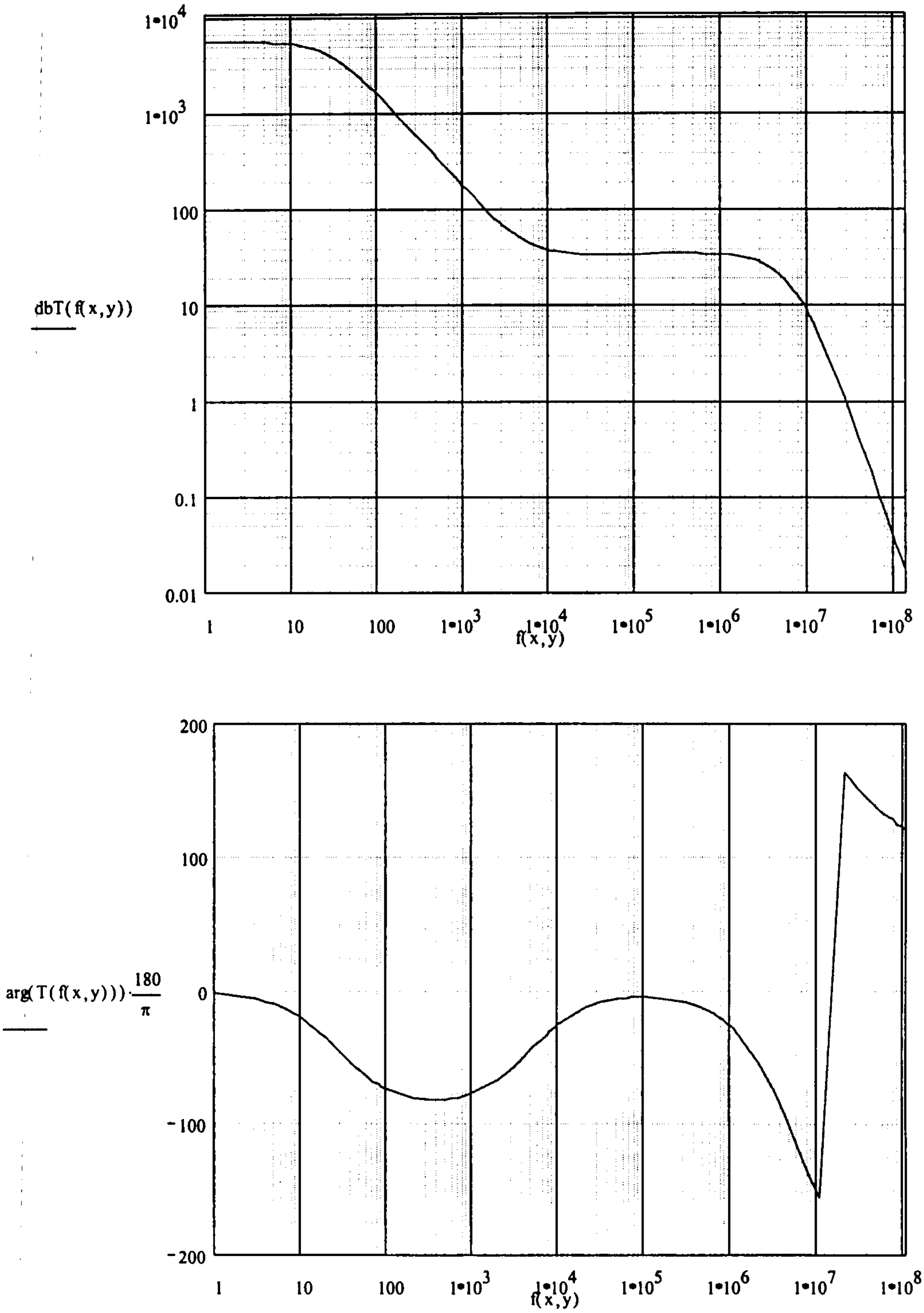


Figure 3.6 Equation 3.19, $R_F = 559K$

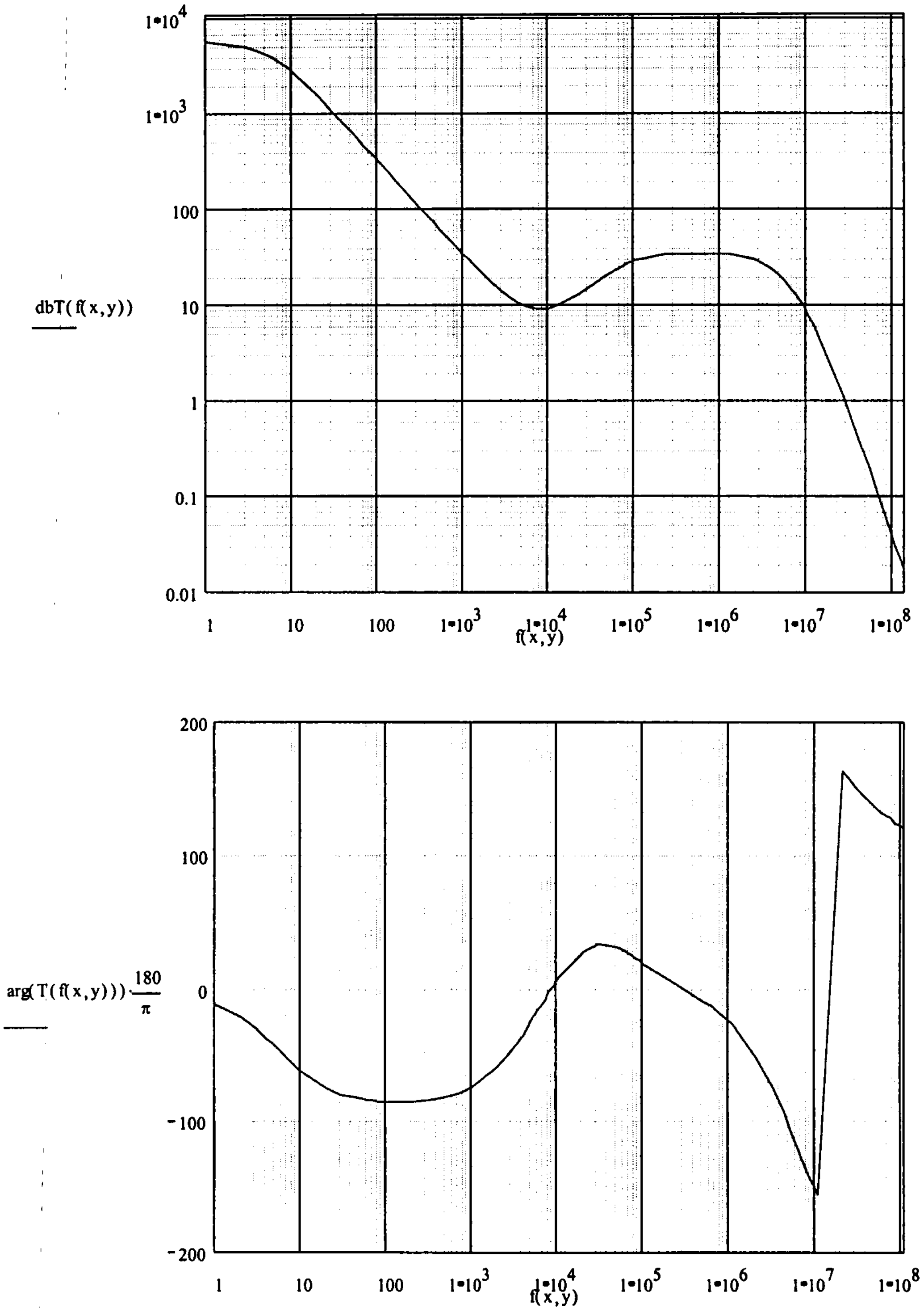
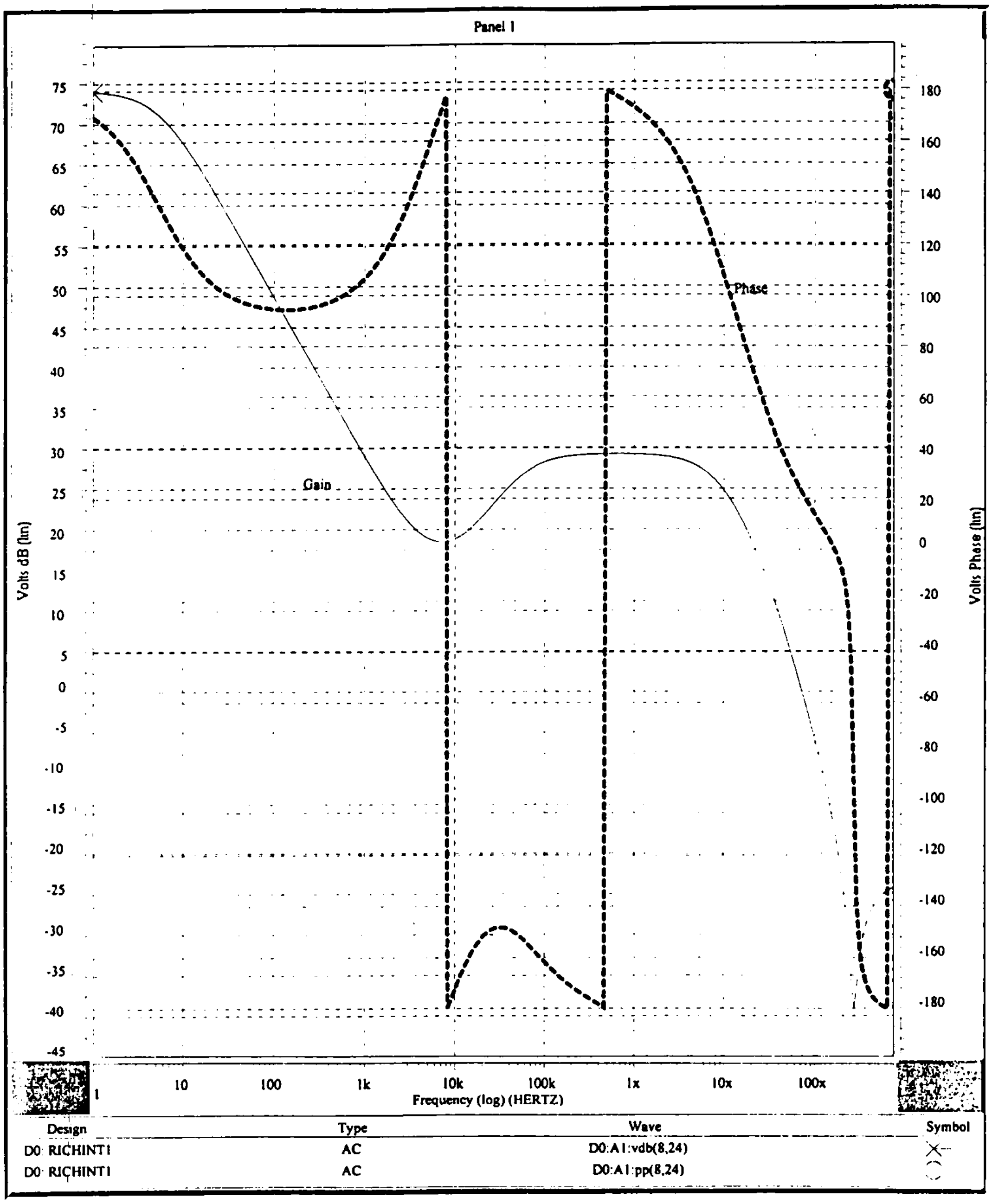


Figure 3.7 Equation 3.19, $R_F = 2.9M$ Ohms

Figure 3.8 RICH Integrator Loop Transmission, HSPICE, R_F = 559K



Design	Type	Wave	Symbol
D0: RICHINT1	AC	D0:A1:vdb(8,24)	×
D0: RICHINT1	AC	D0:A1:pp(8,24)	○

Figure 3.9 RICH Integrator Loop Transmission, HSPICE, R_F = 2.9M Ohms

10MHz, but does underestimate the integrator circuit's phase margin at higher frequencies. Figures 3.8 and 3.9 show an HSPICE generated Bode plot of the actual integrator circuit, for the R_F values of 559k and 2.9 Meg, respectively. In Fig. 3.8 and 3.9, the overall integrator circuit maintains a phase margin of approximately 55 degrees. Equation 3.19 agrees reasonably well with the simulated HSPICE results up to about 50MHz.

3.4 Op-Amp Design Considerations For Low-Noise Performance

Based on early HSPICE simulation results of the integrating amplifier and of the integrator op-amp itself, the target thermal equivalent input noise voltage for the integrator op-amp is to be maintained at $\leq 10\text{nV/Hz}^{1/2}$. This e_n level helps to assure that the noise contribution from the integrator op-amp does not cause the overall integrating amplifier's output rms noise to exceed 3.5mV after correlation, at the nominal VGA gain of 6.5 and the nominal integrator charge gain of 20mV/pC. The actual noise performance of this circuit is covered in more detail in Chapter 5.

The op-amp design rules which dictate the equivalent input thermal noise for the op-amp are fairly straightforward. The op-amp itself consists of two gain stages, which include the differential pair and the output device M6. The gain across the differential pair is approximately 53, while the gain of output device M6 is approximately 85. The differential pair gain is large enough such that the noise contribution from the differential input is much larger than the contribution from the output stage device M6. Therefore, the noise contribution of device M6 may be ignored, and the primary noise contributors are assumed to include the input devices M1 and M2, and the differential pair loads M3 and M4.

Figure 3.10 shows a noise model for the differential pair input used in the RICH integrator op-amp. The thermal noise generators for each source are shown in the top illustration. These independent noise sources may be combined and referred to the input as shown in the bottom illustration of Figure 3.10. The input devices M1 and M2 contribute directly to the input-referred amplifier thermal noise. The noise sources for load devices M3 and M4 reflect back to the input by the ratio of the common-source gain of device M4 to the common-source gain of device M2. This ratio effectively becomes the ratio of the transconductance of device M4 to the transconductance of device M2. By making the transconductance of device M2 large with respect to the transconductance of device M4 (and similarly for devices M1 and M3), the input-referred noise contributions of devices M3 and M4 may be significantly reduced.

Considering the thermal noise contributions of devices M1, M2, M3, and M4, the input-referred equivalent thermal noise for the op-amp may be expressed by [8]

$$\overline{v_{th}^2} = \frac{16kT}{3\sqrt{2\mu_P C_{OX}\left(W/L\right)_1 I_D}}\left(1+\sqrt{\frac{\mu_N\left(W/L\right)_3}{\mu_P\left(W/L\right)_1}}\right)\Delta f \qquad \textbf{(3.20)}$$

The term in parenthesis in Equation 3.20 represents the contribution of the load devices M3 and M4. The transconductance of M3 and M4 has been reduced with respect to devices M1 and M2 by making the W/L ratio for devices M3 and M4 approximately 6.25 times smaller than that for M1 and M2, thus reducing the noise contribution of the load devices. The differential pair is operated at as high a bias current as possible without exceeding the power dissipation specification for the op-amp, in order to

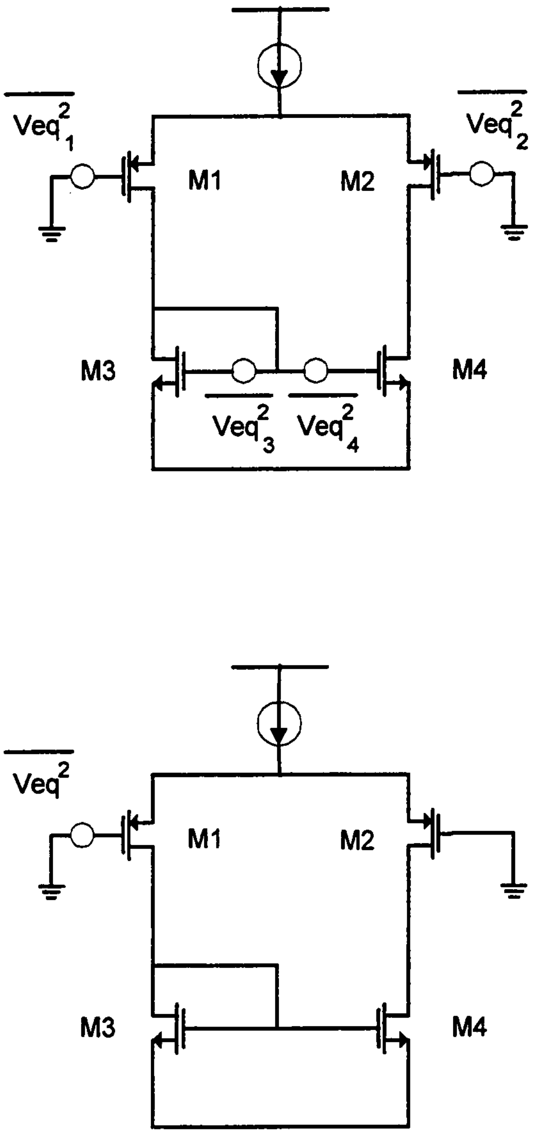


Figure 3.10 Differential Pair Noise Model

maximize the denominator of Equation 3.20 and further reduce the thermal noise. Using typical process parameters for Orbit's 1.2µ process, with a drain current in devices M1 and M2 of approximately 210uA, yields an input-referred thermal noise voltage of 6.2nV/Hz$^{1/2}$ for the RICH integrator op-amp.

The flicker noise generated by a MOS transistor is typically inversely proportional to the WL product. For the differential pair of Figure 3.10, the input-referred flicker noise generator is given by [8]

$$\overline{V_{1/f}{}^2} = \frac{2K_P}{fW_1L_1C_{OX}}\left(1+\frac{K_N\mu_N L_1{}^2}{K_P\mu_P L_3{}^2}\right)\Delta f \qquad \textbf{(3.21)}$$

For the 1.2µ Orbit process, the N-channel flicker noise coefficient K_N is typically 10 to 20 times higher than the P-channel flicker noise coefficient. The term in parenthesis in Equation 3.21 represents the flicker noise contribution due to the N-channel active load devices M3 and M4. Since the active load devices M3 and M4 have the same channel lengths as input devices M1 and M2, the flicker noise contribution due to the loads is not reduced any by the denominator of Equation 3.21. In fact, Equation 3.21 indicates that the N-channel loads may be a significant flicker noise contributor to the active integrator circuit. In Chapter 5, the flicker noise of the integrator op-amp is shown to be the primary noise contributor to the integrating amplifier.

Chapter 4

RICH Variable Gain Amplifier Design

4.1 Variable Gain Amplifier Requirements

The RICH detector relies on Hamamatsu H3171S photomultiplier tubes (PMTs) to convert detected electrons to a charge pulse. This charge pulse is integrated using an integrating amplifier, and the resulting pulse height is proportional to the number of electrons striking the PMT. The RICH detector uses this information to locate the presence and location of Cherenkov rings, which yield information about particle trajectories. The typical Cherenkov ring will overlap several set of PMTs.

The RICH detector will utilize 6400 PMTs, for a total of 6400 channels, providing the needed resolution to accurately locate Cherenkov ring centers. Each channel will have its own independent integrating amplifier. Each channel should ideally exhibit little or no gain variability with respect to the other channels. However, the PMTs unavoidably vary in gain. This PMT gain variation, left unchecked, will cause channel-to-channel gain variability and a corresponding loss in ring location accuracy.

The PMT gains may be equalized by relying on an independent adjustable high-voltage supply for each PMT. In addition to taking up space, this solution is also very expensive, requiring a separate adjustably power supply for each of the 6400 PMTs. A more cost-effective solution is to calibrate the PMT gain in the electronics. A variable gain amplifier, or VGA, has been implemented immediately following the integrator, providing the necessary gain compensation to calibrate each PMT and minimize any channel-to-channel gain variations.

The primary requirement for the VGA is that of equalizing the PMT gains, immediately following the integrator and prior to forming analog sums for trigger purposes. For the analog sum circuitry, the gains must be matched to about 6%. This means that the minimum gain stepsize must be no greater than approximately 6% of the actual gain.

The VGA has several other requirements in addition to providing a gain adjustment over a non-inverting 3:1 range. The VGA risetime specification calls for a 10% to 90% risetime in the range of 10ns to 20ns, for any value of gain. A risetime faster than 10ns implies excessive circuit bandwidth, which is detrimental to noise performance. The VGA must have a risetime of at least 20ns in order to allow the trigger sum circuits and analog memory following the VGA to perform their functions within the 100ns window allotted by the beam clock. To achieve a relatively constant bandwidth as the gain is varied, a variable compensation method must be used in conjunction with the variable gain.

The VGA must have an output dynamic range greater than 3V to fully utilize the resolution of the analog memory and ADC, and must have an output offset voltage less than 100mV to preserve the AMU/ADC dynamic range.

4.2 Overall VGA Design

With respect to the amplifier configuration, two possible feedback topologies exist for the design of a variable gain amplifier; either a current feedback configuration or a voltage feedback configuration. The current feedback topology is inherently a constant bandwidth vs. gain device, which presents an advantage with respect to the RICH risetime specification range. A current feedback amplifier would be able to maintain a relatively constant bandwidth vs. gain, without the need for switched variable compensation.

However, the RICH VGA must operate as a non-inverting amplifier. In this configuration, the low-impedance inverting input of a current feedback amplifier will see a varying voltage (approximately 0.8 volts max for the RICH VGA) as the output voltage swings over its dynamic range. This varying voltage across the inverting input, which typically is a low-impedance FET source, can upset the amplifier bias points if not properly accounted for in the design. In addition, the current feedback topology typically has a higher current noise referred to the inverting input than does a typical voltage feedback amplifier, since the full source bias current appears at the input of the current feedback device.

For these reasons, a voltage feedback topology has been selected for the RICH VGA. Figure 4.1 illustrates the basic layout of the RICH VGA, including a block diagram of the amplifier with internal compensation as well as the gain switches. The voltage feedback configuration does necessitate having a switched variable compensation to maintain amplifier bandwidth as the gain changes. This bandwidth compensation is shown in Figure 4.2 as the 3-bit frequency control which is internal to the op-amp itself. The VGA gain varies linearly over a 3:1 range, from times 4 to times 12, with 32 separate gains available. The gain stepsize is approximately 0.259, allowing 6.5% gain matching at a gain of 4 and 2.2% gain matching at a gain of 12.

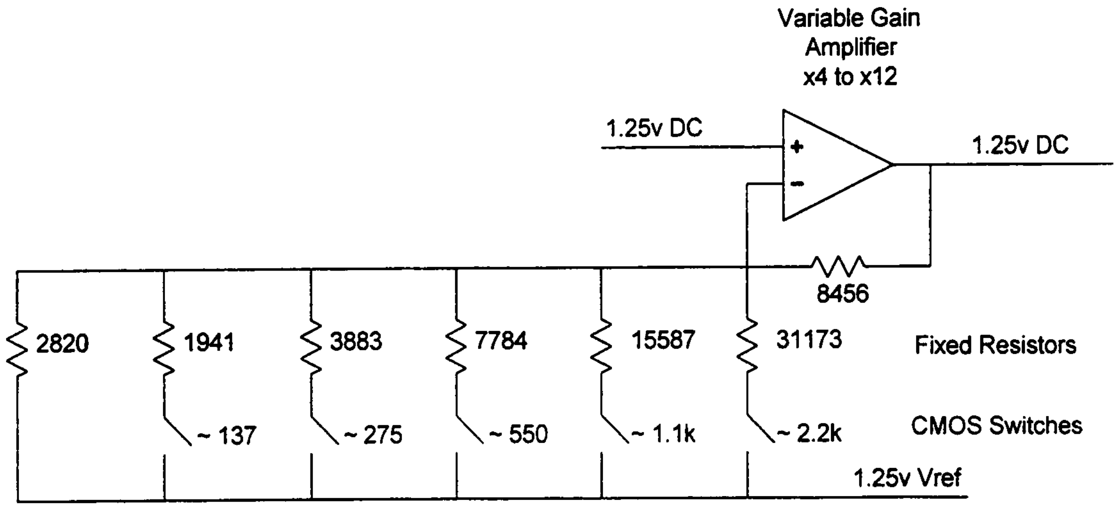


Figure 4.1 RICH VGA Block Diagram

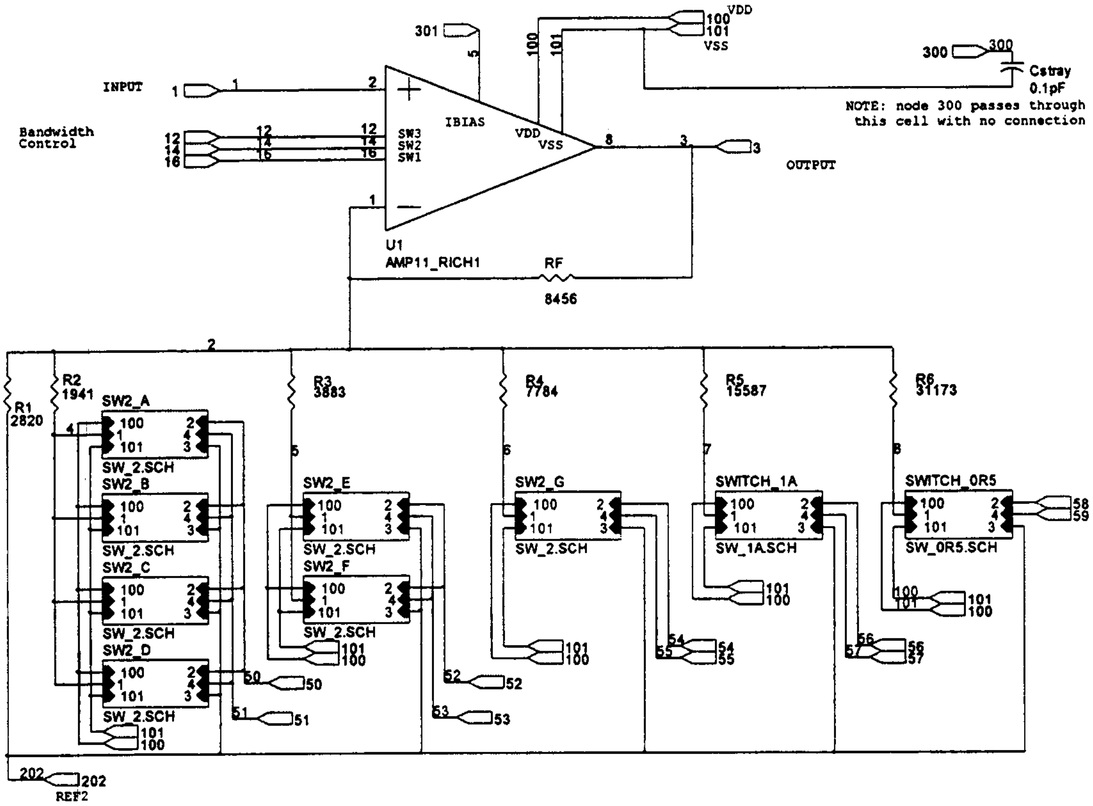


Figure 4.2 RICH Variable Gain Amplifier

Several options exist for the placement of the gain switches. From the RICH specifications, a 5-bit gain resolution is required in order to meet the 6% gain matching specification, necessitating 5 gain control switches. To switch the amplifier gain, these switches may be placed so as to vary the feedback resistance or to vary the resistance from the inverting terminal to ground.

Varying the feedback resistance has several disadvantages. First, the feedback resistance is typically larger than the resistance from the inverting terminal to ground. This implies that locating at least 5 different switched parallel resistances in the feedback loop will consume more chip area due to the large resistance. Second, the drain-to-body and drain-to-gate capacitance of the CMOS switches will appear at the output of the op-amp, the inverting terminal, or both, depending on the placement of the switches relative to the feedback resistors. For these reasons, placement of the CMOS switches in the path from the inverting terminal to ground is preferred.

One potential problem with using CMOS switches to vary the amplifier gain is that the switch resistance varies as the voltage across the switch varies. As the amplifier output swings across its dynamic range, the voltage across the CMOS switches will unavoidably vary, causing the amplifier gain to vary with the output voltage. The design and layout of the RICH VGA gain control switches seeks to minimize these effects.

In Figure 4.1, the 5 CMOS switches are placed in series with fixed resistors, in the path from the inverting terminal to ground. Each of the 5 CMOS switches has an equivalent resistance of approximately 7% of its adjacent fixed series resistor. This switch sizing and placement has two beneficial effects which help to minimize the amplifier gain variation as output voltage varies.

First, there is a considerable amount of voltage division which occurs from the amplifier output to the switch. For a 3.25 volt full-scale output voltage swing, the inverting input swings 0.8125 volts worst-case, at a gain of 4. Since the CMOS switches have a resistance of approximately 7% of each fixed resistor, the voltage swing across each CMOS switch is at worst slightly over 0.05 volts. For a nominal VGA gain of 6.5, and an output dynamic range of 3.25 volts, the CMOS switch voltage variation drops to just over 0.03 volts. This voltage division greatly reduces the total switch resistance variation. Simulations have shown that the total CMOS switch resistance variation, as a percentage of the total switch resistance, is less than 10% worst case.

Second, the fact that each CMOS switch has a total resistance of less than 10% of its corresponding fixed resistor means that the switch resistance variation contributes only a small percentage variation to the total resistance from the inverting input to ground. In effect, if the CMOS switch resistance varies by 10%, but the switch represents only 7% of the fixed resistance, then the total resistance from the inverting input to ground only varies by 0.7%, for a gain variation of about 0.64% worst case over the full dynamic output range.

With all switches off, the amplifier has a gain of approximately 4. With all switches on, the amplifier gain is approximately 12. The CMOS switch resistances, and their corresponding series fixed resistors, are binary-weighted. The binary weighting allows a digital 5-bit binary input to linearly vary the gain.

The external gain resistors are sized with respect to several considerations. The ratio of the feedback resistor to the other resistors must be sufficient to provide a gain range of times 4 to times 12. If the fixed resistors are made small in order to conserve chip area, this implies that the CMOS switch resistances will be small, resulting in a large W/L value for the switch. Also, having a small resistance in the feedback loop can be detrimental to the slew rate performance of the op-amp, since the feedback resistor consumes part of the amplifier's drive current.

The RICH VGA's CMOS switches have been minimized in size in order to conserve chip area, since these particular CMOS switches occupy a relatively large amount of chip area compared to their corresponding fixed resistors. The on resistance of a CMOS switch is proportional to the ratio of length to width, or L/W. Both L and W have been roughly minimized for the largest switch, switch_0r5 in Figure 4.1. This switch has an on resistance of approximately 2.2k, a W/L of 4.2/1.2 for the N-channel device and 12/1.2 for the P-channel device, and represents the least-significant bit (LSB) in the gain control.

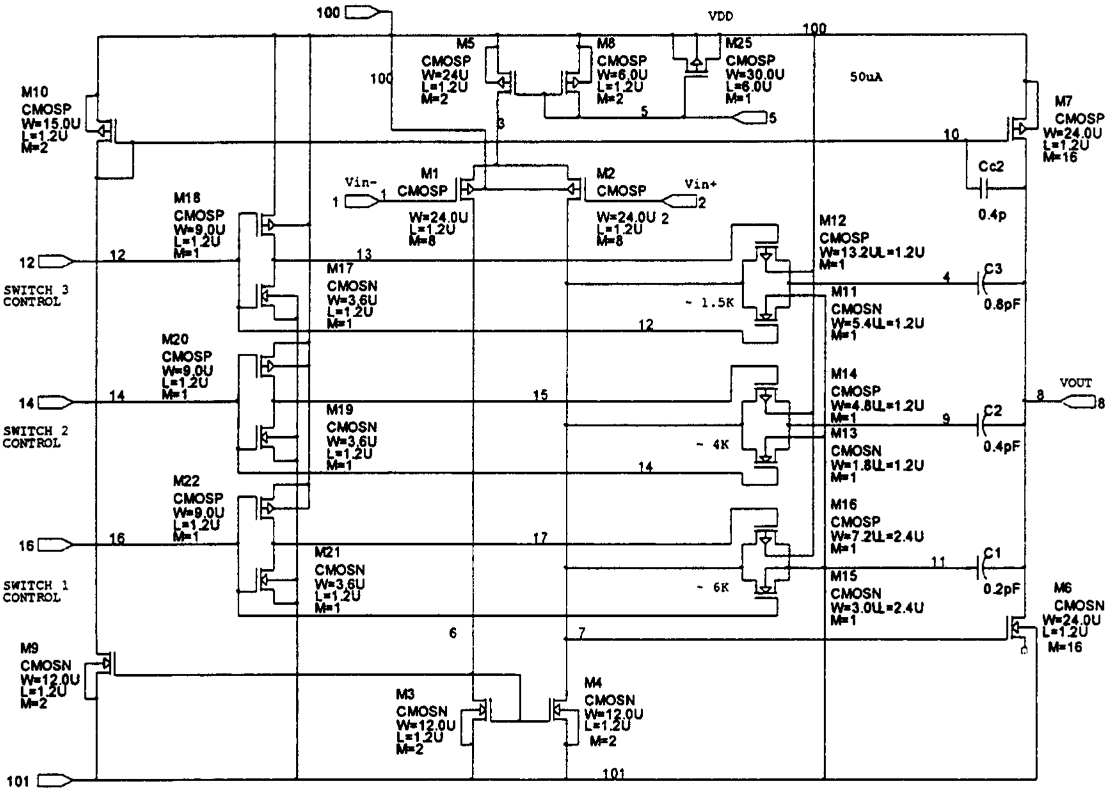
To preserve the binary weighting, switch_1a of Figure 4.1 has roughly one-half the on resistance of switch_0r5, achieved by doubling the device widths with respect to switch_0r5. Similarly, switch_2 has one-half the resistance of switch_1a, and double the width. In this manner, the CMOS switch resistances are binary-weighted.

With the CMOS switch resistances set, the fixed resistors are scaled such that each corresponding CMOS switch resistance is approximately 7% of the fixed resistor. The final fixed resistor R_1, and the feedback resistor R_F, are scaled such that the gain is equal to 4 with all switches off, and so that the LSB switch creates a gain change of approximately 0.25 volts/volt. The fixed resistor and feedback resistor have final values of 2820 and 8456 ohms, respectively, to meet these two criteria. The feedback resistance does not hinder the output drive current capability of the amplifier, drawing about 290uA worst-case. The amplifier itself is capable of providing an output drive current of approximately 2.2mA, under a positive large-signal input condition.

4.3 VGA Operational Amplifier Design

The RICH Variable Gain Amplifier op-amp is shown in Figure 4.3. The op-amp is a basic two-stage design, utilizing PMOS input devices. The PMOS input devices provide sufficient V_{GS} headroom for the amplifier input to be DC biased at 1.25 volts, and the negative rail at ground. This input biasing is beneficial since the input to the VGA is essentially a positive-going step, for which biasing the input, and consequently the output near the negative supply allows for a higher output dynamic range. The positive voltage rail is 5V.

The VGA op-amp is internally compensated with 3 bits of variable compensation. Devices M17 through M22 are inverters, which activate the CMOS switches comprised of devices M11 through M16. These CMOS switches, along with capacitors C1 through C3, provide enough series resistance and capacitance from the gate-to-drain of device M6 to provide stability through pole-splitting and right-half-plane zero compensation as discussed in Chapter 3. By applying a digital input to the inverter switch controls, 8 different capacitance combinations may be switched in and out to provide the variable compensation. In this manner, the compensation can be matched to the particular gain of the amplifier, maintaining a substantially constant bandwidth. The compensation capacitors are binary-weighted, so that a linearly increasing amount of compensation capacitance is switched in via the digital switch controls. The CMOS switch resistance



NOTE: DESIGNED FOR 5V OPERATION, SWITCHED COMPENSATION FOR BW CONTROL

Figure 4.3 RICH VGA Operational Amplifier values have been selected based on simulations so as to provide the best transient pulse response for all gain ranges.

The primary 2-stage gain path through the op-amp consists of the differential pair as the first gain stage, followed by device M6 as the final gain path. In general, the device lengths have been kept to a minimum, in an effort to trade open loop gain for bandwidth. Consequently, the Early voltages of the MOS devices are relatively low. Devices M9 and M10 mirror additional drive current to device M7, for positive output voltage swings only, serving to increase the positive slew rate performance of the amplifier. Since the VGA must respond only to positive-going input signals, the negative slew rate is not critical to the amplifier performance. The amplifier's positive slew rate is limited by the ~12pF load capacitance and the output current drive capability, and not so much by the differential pair bias current and the compensation capacitors.

Assuming a worst-case 3.25-volt output positive dynamic voltage swing, with a risetime of ~20ns, the VGA slew rate should exceed 162 volts/microsecond, with a 12pF load capacitance. To meet this slew rate specification, output device M7 must provide 1.95mA of drive current to the load. The nominal bias current through device M8 is 50uA, resulting in a nominal bias current in device M7 of 1.28mA, neglecting channel-length modulation effects. Including channel-length modulation effects in devices M5, M9, and M7, simulations indicate the device M7 actually draws 2.36mA of bias current. In the event of a large-signal positive-going input, device M2 turns off and M1 turns on hard, doubling the bias current in device M3. This bias current is in turn mirrored to device M9, doubling M9's bias current as well, if channel-length modulation effects are not considered. The current available to drive the load, provided by device M7, is theoretically doubled over the nominal bias value due to the doubled current through device M10. In this manner, for a positive-going large signal, the current available from device M7 is roughly doubled over the 2.36mA nominal bias current, allowing a theoretical 391 volt/microsecond positive slew rate into a 12pF load.

However, the actual op-amp in simulations exhibits a slew rate of approximately 170 volts/microsecond, well below that of the theoretical maximum slew rate of 391 volts/microsecond. The reason for the less-than-theoretical slew rate has to do with the amount of current that is actually mirrored into load device M7. Instead of the load current in M7 doubling due to a large signal response, M7's drive current only increases from 2.36mA at idle to 2.75mA at full positive slew. The reasons for this loss of available drive current are twofold. First, at high frequencies two additional poles exist at the gate of device M9 and at the drain of M9, which tend to reduce the gain around this secondary loop, causing the effective current gain to roll off as well. Consequently, at high frequencies the current in M9 is not doubled as a result of a doubling of current in M3. In fact, the current in M9 only increases by about 30% for a large positive input signal. Second, about 500uA of the available drive current from device M7 is lost through the compensation capacitors C1-C3, and Cc2, during the transition to large-signal response. The total amount of current available to drive the load capacitance is about 2.14mA from device M7, resulting in a simulated positive slew rate of about 178 volts/microsecond.

The low Early voltage of the devices also necessitates additional design considerations with respect to the amplifier's offset voltage. Ideally, to achieve a low systematic offset, the drain voltages of devices M1 and M2 should be matched, and the drain currents sourced by devices M6 and M7 should be matched. If the drain voltages of devices M1 and M2 match, then device M6 carries 16 times the drain current of device M4. The drain current through M9 mirrors that through M3 on a 1:1 basis neglecting Early voltage. Consequently, M10 should be sized so as to mirror the same amount of current as device M6 carries. If this sizing is done, then device M10 is required to have a W/L ratio of 12, neglecting Early voltage effects. Thus, if the current in device M4 is I, the current through devices M7 and M6 is mirrored at exactly 16I, and the circuit is balanced.

In the actual chip, however, scaling device M10 with a W/L of 12 results in an imbalance of drain currents in M6 and M7, with a resulting large positive systematic offset voltage. This is a result of the Early voltage, which is low enough to cause channel-length modulation related biasing offsets which propagate through the circuit. For example, the nominal bias current through device M8 is 50uA. The differential pair bias currents through M1 and M2 are 127uA each. Device M4 mirrors this current to output device M6 by the ratio of 16:1, resulting in M6 trying to source 2mA. Device M3 mirrors the 127uA differential pair bias current to device M9. M9, however, experiences channel-length modulation which increases its total bias current to 144.5uA. This is mirrored through device M10 to output device M7. If M10 is scaled with a W/L of 12, then device M7 sources 2.3mA ideally, but actually attempts to source slightly more current due to channel length modulation effects on M7. Thus, M7 attempts to drive more current than M6, resulting in a positive systematic offset.

This offset has been partially compensated for by increasing the W/L ratio of device M10. Since M10 carries a higher-than-normal current due to its low output resistance, the current mirroring W/L ratio between M10 and M7 should be reduced to cause the higher-than-normal current in M10 to produce the correct current in M7, more closely matching the current in M6. The width of device M10 has been increased to 15um from 12um, which more closely balances the current drive through the output pair.

The 50uA bias current in device M8 results in a total power dissipation of 14 milliwatts with a 5V supply. Most of the power is consumed by the 2.36mA bias in output devices M7 and M6.

The input-referred equivalent noise voltage for the VGA op-amp may be derived using Equation 3.20, referring to the differential pair noise model of Figure 3.9. As with the integrator op-amp of Chapter 3, the transconductance of M3 and M4 has been reduced with respect to devices M1 and M2 by making the W/L ratio for devices M3 and M4 approximately 8 times smaller than that for M1 and M2, thus reducing the noise contribution of the load devices. The differential pair is operated at as high a bias current as possible without exceeding the power dissipation specification for the op-amp, in order to maximize the denominator of Equation 3.20 and further reduce the thermal noise.

The VGA op-amp's differential pair input noise voltage is approximately $6.5\text{nV/Hz}^{1/2}$, considering only the amplifier and using Equation 3.20. Considering the amplifier operating with a gain of 12, the total equivalent input noise voltage becomes $7.3\text{nV/Hz}^{1/2}$, which takes into account the noise generated by the feedback resistors as well as the white amplifier noise.

4.4 VGA Operational Amplifier Stability and Open Loop Response

A primary requirement for the RICH VGA is that of maintaining a fixed risetime range for a gain range of times 4 to times 12. The VGA risetime requirements specify a 10ns risetime minimum, along with a 20ns risetime maximum. The worst case for risetime occurs when the amplifier is operated at a maximum gain of 12, since as amplifier gain increases, closed loop bandwidth decreases. Using the approximate relationship between bandwidth and risetime for a single-pole rolloff,

$$Risetime \approx {}^{0.35}\!/_{f_{HI}} \tag{4.1}$$

and using the maximum risetime bound of 20ns, the closed loop amplifier bandwidth must be no less than 17.5MHz. Assuming a worst-case non-inverting gain of 12, the open loop amplifier gain-bandwidth product must be roughly 12 times the closed loop bandwidth, or 210MHz.

In general, small gate length devices are utilized to trade open-loop gain for additional amplifier bandwidth, by reducing the device output resistances and to an extent, capacitances. The amplifier open loop gain is determined primarily by the gain across the differential pair, followed by the gain across output device M6. Differential pair devices M1 and M2 have a g_m of approximately 0.001 A/V, including the body effect, which reduces the differential pair transconductance by about 75 uA/V. The equivalent load resistance of device M2 is equal to the parallel combination of the output resistance of devices M2 and M4. Device M4 has an output resistance of approximately 115875Ω. The output resistance of device M2 is increased somewhat by the presence of source resistance in the form of $1/g_m$ of device M1. The nominal output resistance of device M2 is approximately 21645Ω. The total node resistance at the output of device M2 is 21645 in parallel with 115875. Using these values, the first stage gain $g_{m1}R_{L1}$ is approximately 18.24.

The second stage gain is given by $g_{m6}R_{L6}$. R_{L6} is given by the parallel combination of the output resistance of devices 6 and 7, and is approximately 3115Ω. Using g_{m6} of approximately 9.61mA/V yields a second stage gain of 29.95, for a total primary path gain of 546.

The op-amp also has a secondary gain path, through device M1, M9, and M7. This path generally has very low impedances, and exists for the purpose of providing additional positive slew rate capability. As such, the small-signal gain around this loop is small, approximately 20 V/V. Adding this gain to the primary path gain yields a total small-signal amplifier gain of 566. This estimate is slightly below the open-loop gain of 589 predicted by HSPICE. The amplifier's dominant pole occurs at approximately 390kHz, with the 0.8pF compensation capacitor switched in, yielding a gain bandwidth product of approximately 230 MHz.

In general, the analysis of Section 3.2 regarding the integrator op-amp Miller compensation may be used to approximate the dominant pole location for the VGA op-amp. The main difference is that the VGA has an additional gain path, through devices M9 and M10 to output device M7. This additional gain path causes the high-frequency response of the VGA to deviate slightly from the integrator op-amp response presented in Chapter 3. A model for this additional gain path is presented later in this chapter.

The VGA utilizes three different Miller capacitors, binary-weighted for seven different variable compensation settings. The CMOS switches serve two purposes. First, they allow different compensation paths to be switched in or out in order to compensate the VGA for different gain ranges. Second, they provide a resistance in series with the Miller capacitor which compensates the right-half plane zero generated by the Miller capacitor. Clearly, the right-half plane zero location is different for each different possible compensation path. However, in general the switch resistances are large enough with respect to the second-stage transimpedance that the right-half plane zero is always moved into the left half plane, for any given compensation combination. This compensation method provides the best amplifier transient response and settling time.

The primary amplifier nodes which dominate the open-loop frequency response include the internal node at the drain of M2, and the output node. The capacitance at the drain of M2 may be approximated by

$$C_1 = C_{DG2} + C_{DB2} + C_{DG4} + C_{DB4} + C_{GS6} + C_{GB6} + C_{GD6}(1 - A_6) + C_{STRAY} + C_{SWITCH} \quad \textbf{(4.2)}$$

The switch capacitance includes the drain-to-ground capacitance of the CMOS switches, and is typically on the order of several femtofarads, small enough to be negligible.

The capacitance at the output node consists primarily of the output capacitances of load devices M6 and M7, plus any load capacitance which may exist. The output capacitance may be approximated by

$$C_2 = C_{DG7} + C_{DB7} + C_{DG6} + C_{DB6} + C_{LOAD} \quad \textbf{(4.3)}$$

As indicated earlier, the open-loop right-half-plane zero compensation analysis presented for the integrator op-amp in Chapter 3 yields a fair approximation for the dominant pole of the VGA, but does not properly account for the additional gain path through devices M9 and M10 in the VGA. This additional gain path primarily affects the location of the right-half plane zero in the open loop frequency response. A more detailed model of the VGA open-loop frequency response is shown in Figure 4.4.

In the gain model of Figure 4.4, the gate-to-drain Miller capacitance of device M6 is assumed to be grouped in with the capacitance C_2, while the compensation capacitor itself is modeled by C_C. The compensation Miller capacitance consists primarily of the compensation capacitor. The main difference between the VGA 2-stage gain model of Figure 4.4 and the model for the integrator is the inclusion of a second transconductance generator in the VGA model of Figure 4.4.

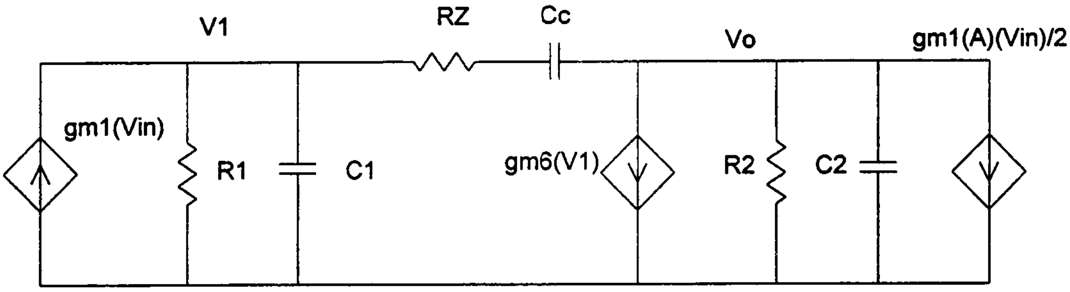
The added transconductance generator, $(g_{M1}/2)(A)V_{in}$, models the effect of the current gain path from the differential pair through device M9, M10, and M7. The current gain, A, is the ratio of the change in current in device M7 to the change in current of device M1. The change in current in device M1 due to a single-sided input voltage V_{in} is equal to $g_{M1}/2$.

The small-signal current gain A reduces ideally to the ratio of $(W/L)_7$ to $(W/L)_{10}$, or 12.8. In actuality, the current gain is less than this due to Early voltage effects in the transistors. HSPICE simulations indicate that A is closer to ~7 for small-signals.

Nodal analysis is employed to establish the relationship between the input voltage V_{in} and the output voltage V_o for Figure 4.4. In Figure 4.4, voltage V_1 represents the node at the drain of device M2, and V_O represents the node at the output. Referring to the node at V_1, current summation produces the relationship

$$g_{M1}V_{IN} - V_1\left({}^{1}\!/_{R_1} + SC_1 \right) - (V_1 - V_O)\left(\frac{SC_C}{1 + SR_Z C_C} \right) = 0 \tag{4.4}$$

RICH VGA Open-Loop Gain Model, Cap Code = 100



gm1 = 0.001

R1 = 18238

C1 = 4.414 pF

gm6 = 0.00961

R2 = 3115

C2 = 1.1pF No Load
13.1pF Load

A ~ 12.8

RZ = 1500, Cc = 0.8pF

Figure 4.4 RICH VGA Open Loop Gain Model

Current summation at the output node establishes the second nodal equation

$$\left(V_1 - V_O\right)\left(\frac{SC_C}{1+SR_ZC_C}\right) - g_{M6}V_1 - V_O\left(\frac{1}{R_2} + SC_2\right) - \frac{g_{M1}A}{2}\left(V_{IN}\right) = 0 \qquad \textbf{(4.5)}$$

By combining these two equations and eliminating the variable V_1, the relationship between V_{IN} and V_O becomes

$$\frac{V_O}{V_{IN}} = \frac{\left(-g_{M1}g_{M6}R_1R_2 - \frac{g_{M1}}{2}\left(AR_2\right)\right)\left(aS^2 + bS + 1\right)}{cS^3 + dS^2 + eS + 1} \qquad \textbf{(4.6)}$$

where

$$a = \frac{AC_1R_1R_ZC_C}{2R_1g_{M6} + A} \qquad \textbf{(4.7)}$$

$$b = \frac{-2C_CR_1 + 2R_1g_{M6}R_ZC_C + AR_ZC_C + AR_1C_1 + AR_1C_C}{2R_1g_{M6} + A} \qquad \textbf{(4.8)}$$

$$c = R_1C_1R_2C_2R_ZC_C \qquad \textbf{(4.9)}$$

$$d = R_1C_1R_ZC_C + R_1C_1R_2C_2 + R_1C_CR_2C_2 + R_ZC_CR_2C_2 + R_1C_1R_2C_C \qquad \textbf{(4.10)}$$

$$e = R_ZC_C + R_1C_1 + R_1C_C + R_2C_2 + R_2C_C + R_1C_CR_2g_{M6} \qquad \textbf{(4.11)}$$

With respect to Equation 4.6, the current gain term, A, appears only in the numerator. This observation leads to an interesting aspect of the amplifier topology of Figure 4.3. The current gain of the secondary loop may be used, to an extent, to adjust the location of the loop zero(s) and thus affect the stability of the amplifier, independently of the compensation capacitors and resistors, and independently of the amplifier loop poles.

MATHCAD simulations of Equation 4.6 reveal that, with R_Z equal to approximately zero, the two zeroes occur in the left-half plane. Thus, the secondary gain loop is able to shift the right-half plane zero that occurs in the amplifier of Figure 3.3 into the left half plane. A second left-half plane zero is also created, and is typically an order of magnitude higher in frequency than the dominant zero.

Allen and Holberg [9] derived an input/output expression for Figure 4.4 for the case in which R_Z is not present. For this case, the dominant zero occurs at approximately

$$z \approx \frac{-g_{M6}}{(0.5A-1)C_C} \tag{4.12}$$

When A is equal to 2, the zero occurs at infinity. For values of A greater than 2, the zero is shifted into the left-half plane, and moves towards the origin as A increases.

The effect of increasing A in the model of Figure 4.4 is to shift both zeroes toward the origin, in the left half plane, without affecting the amplifier poles. Similarly, increasing the value of the compensation resistor R_Z in Figure 4.4 shifts the zeroes towards the origin, but also moves the poles somewhat. Solving Equation 4.6, using the values given in Figure 4.4 with no load capacitance, yields the following transfer function.

$$V_O/V_{IN} = \frac{-566\left(1+j\frac{f}{112MHz}\right)\left(1+j\frac{f}{2088MHz}\right)}{\left(1+j\frac{f}{296kHz}\right)\left(1+j\frac{f}{150MHz+j136MHz}\right)\left(1+j\frac{f}{150MHz-j136MHz}\right)} \tag{4.13}$$

The transfer function given by Equation 4.13 does an adequate job of predicting the amplifier poles, but does not agree with SPICE regarding the location of the amplifier's dominant zero. SPICE does not indicate the presence of a zero anywhere below 500MHz in the open-loop response. A large source of this discrepancy in the model of Figure 4.4, and consequently in Equation 4.13, has to do with the frequency response of the current gain term, A. In Figure 4.4, the current gain A is modeled as a constant, in order to simplify the output/input relationship so as to provide better intuitive insights into the general behavior of the amplifier model. In practice, the current gain A is frequency dependent, due to poles that occur at the gate of M9, the drain of M9, and to a secondary right-half plane zero that occurs as a result of the secondary loop compensation capacitor C_{C2}. These poles will cause the current gain A to fall off with increasing frequency. SPICE simulations of the actual circuit reveal this frequency dependency of the current gain, showing the value of A falling to approximately 4 for a typical small-signal fast rising-edge input pulse. The effect of this rolloff in A with frequency is to shift the dominant left-half plane zero higher in frequency. Therefore, Equation 4.6, which does not consider the frequency dependency of current gain A, estimates the zero locations at too low of a frequency.

The secondary loop compensation capacitor C_{C2} provides gate-to-drain Miller compensation around device M7. This compensation capacitor does not significantly affect the phase margin of the overall amplifier. However, it does improve the amplifier's positive-going pulse response for certain gain ranges and compensation settings. Typically, the VGA demonstrates the positive-going pulse response of Figure 4.5 without the secondary loop compensation capacitor, C_{C2}, for low gains and low values of load capacitance. The output pulse response shows a "notch", which appears to occur at the transition from one dominant time constant to another, slower time constant. Again, this "notch" is most noticeable at low gains and low values of load capacitance.

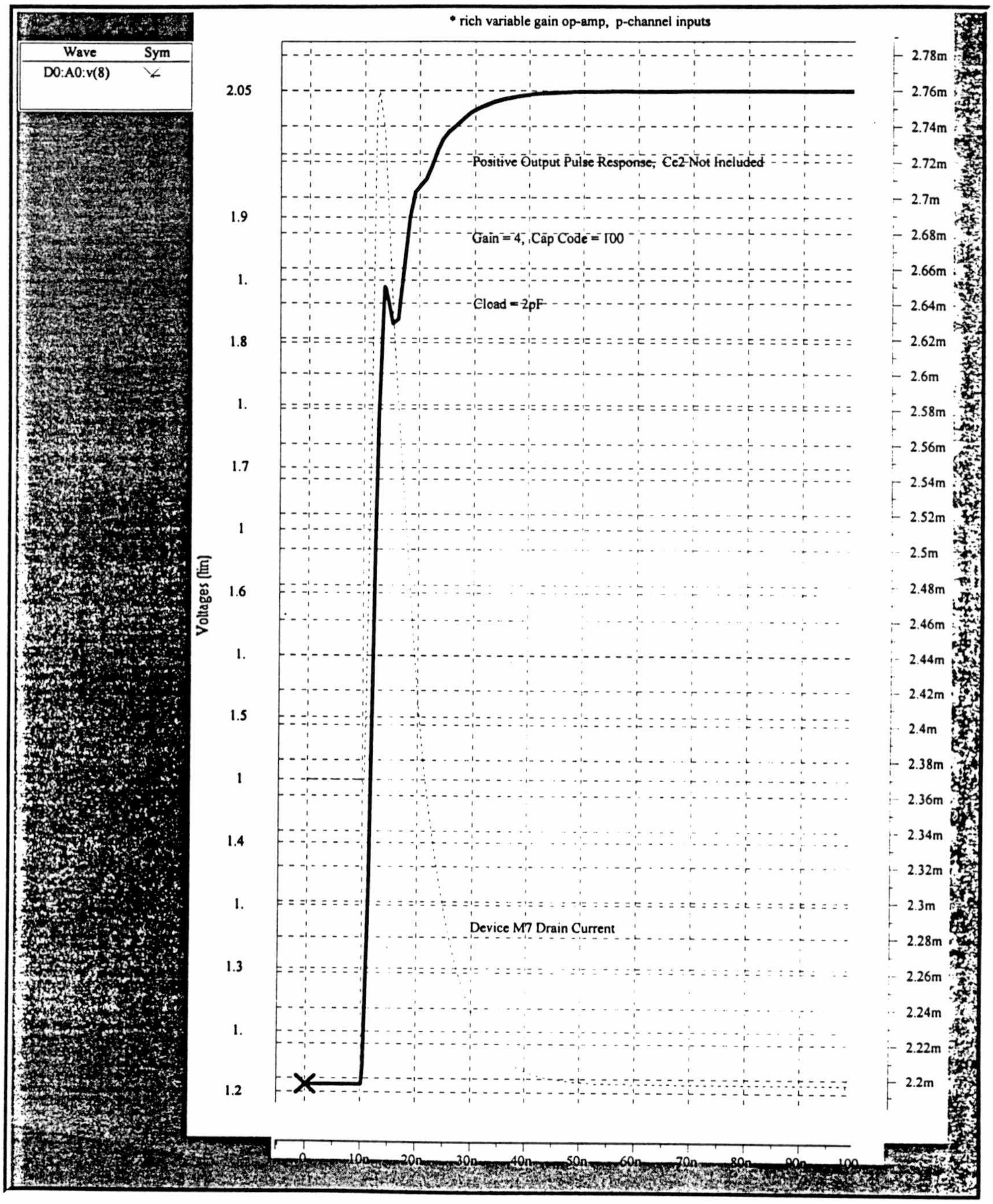


Figure 4.5 VGA Positive Pulse Response, C_{C2} Not Included

Figure 4.5 also shows the drain current response of device M7, indicating the correlation in device M7's drain current response with the notch in the output pulse response.

Simulations reveal that compensation capacitor C_{C2} slows somewhat the response of the secondary loop, introducing a secondary dominant node at the gate of M7 and slightly reducing the peak drain current sourced by device M7 for a positive-going output pulse. Thus, the secondary loop response does not tend to fight the primary loop, and the two loops are able to smoothly transition from a large-signal response to a small-signal response. Figure 4.6 shows the VGA pulse response under the same conditions as Figure 4.5, except for the inclusion of compensation capacitor C_{C2}.

A disadvantage of including compensation capacitor C_{C2} is a degradation of the VGA's positive slew rate. Simulations reveal that C_{C2} affects the amplifier's positive slew rate in two ways. First, C_{C2} slightly limits the peak drain current sourced by M7 at high frequencies, by further reducing the loop current gain with frequency. Second, a portion of M7's drain current that would otherwise be available to drive the load is lost through C_{C2} during the large-signal response. As a result, the inclusion of C_{C2} reduces the simulated positive slew rate from approximately 210 volts/microsecond to approximately 170 volts/microsecond.

Figure 4.7 shows an HSPICE simulation of the VGA operational amplifier's open-loop response. HSPICE predicts an open-loop gain of 589, with a gain bandwidth product of 230 MHz, yielding the amplifier bandwidth required to meet the risetime specifications. The relatively low open loop gain is not a problem for the intended application, since absolute gain accuracy is not a primary concern. Figure 4.8 shows an HSPICE simulation of the output and input-referred noise voltage, in $V/Hz^{1/2}$ for the

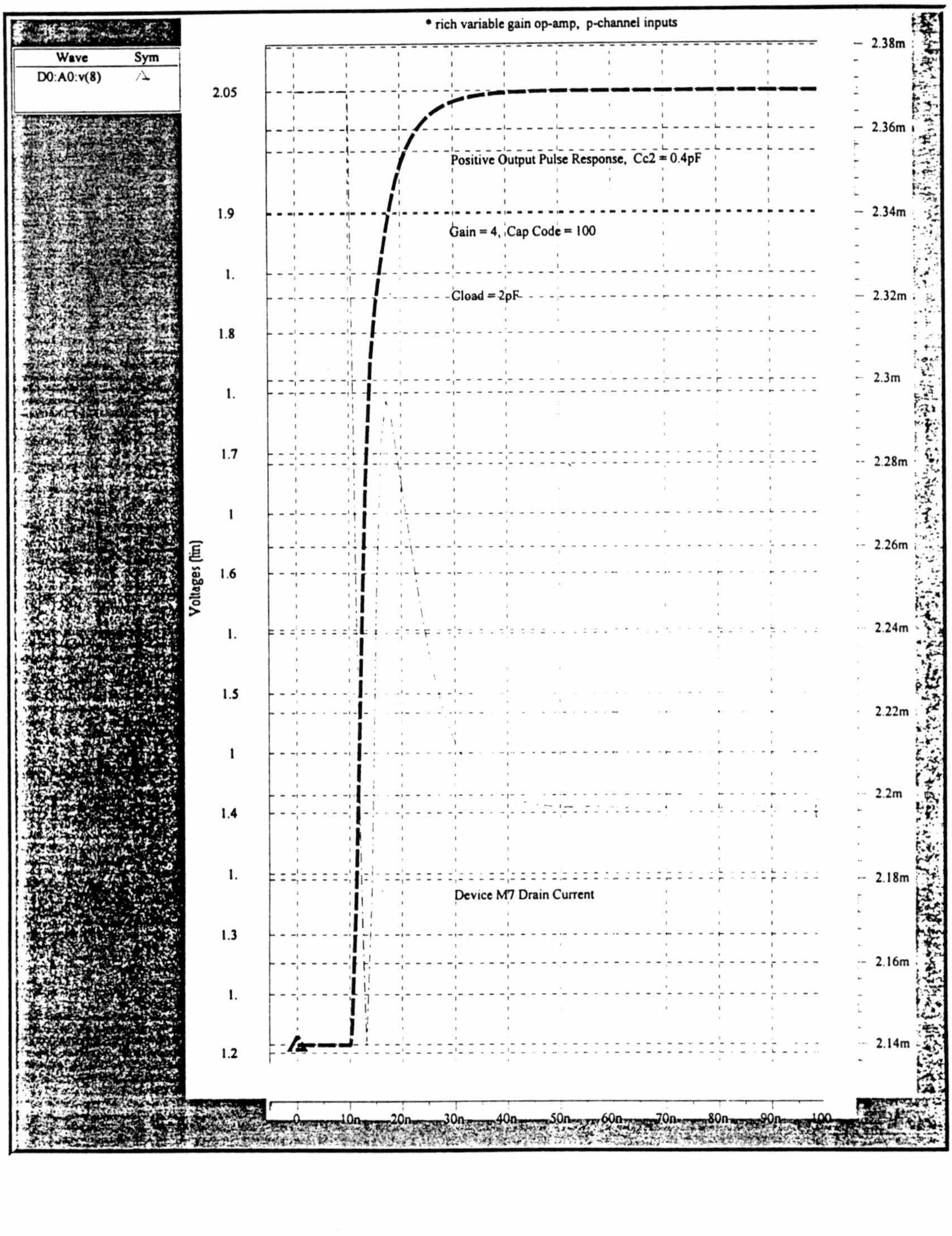


Figure 4.6 VGA Positive Pulse Response, $C_{C2} = 0.4$pF

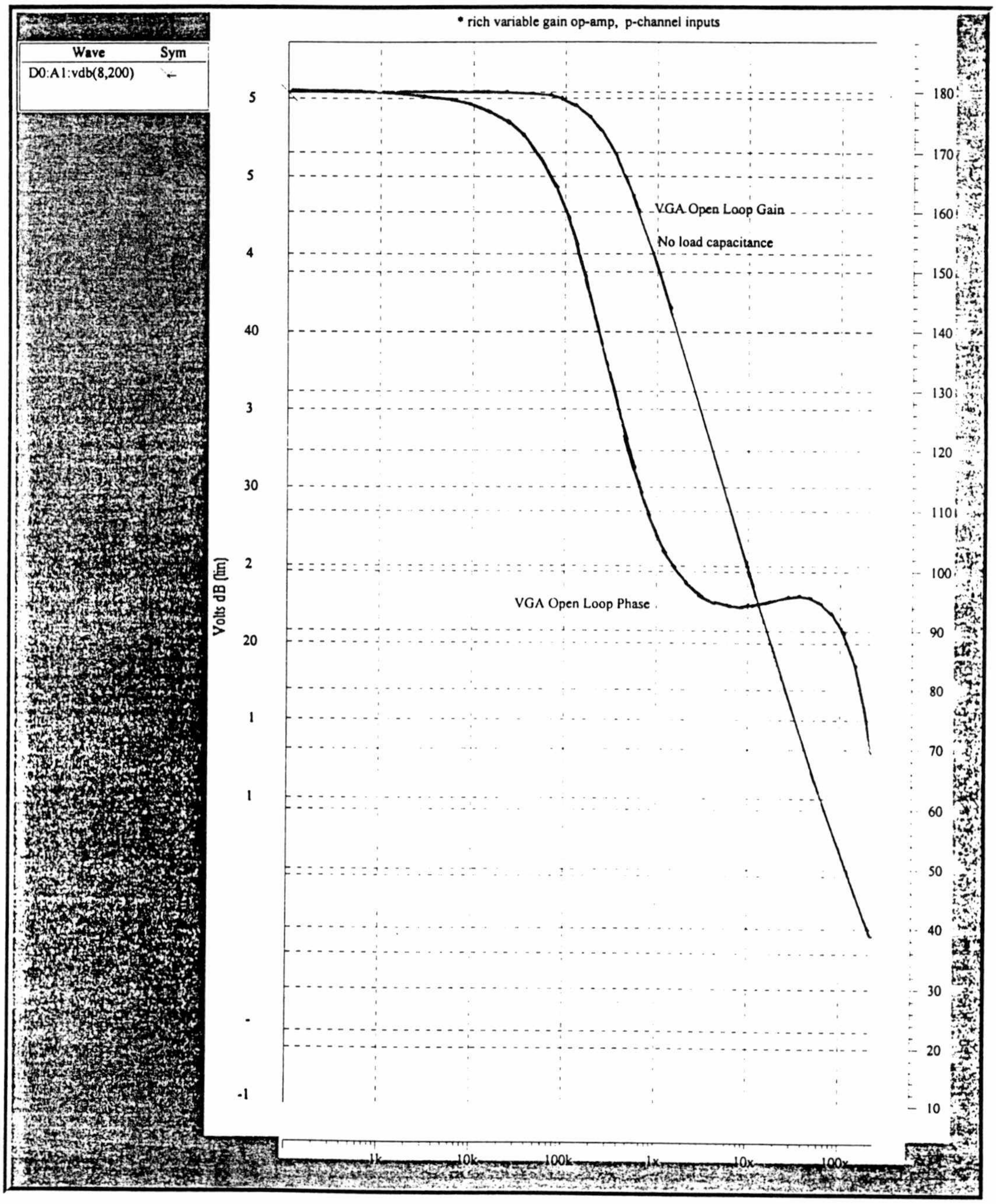


Figure 4.7 VGA Open Loop Gain and Phase, Cap Code = 100, No Load Cap.

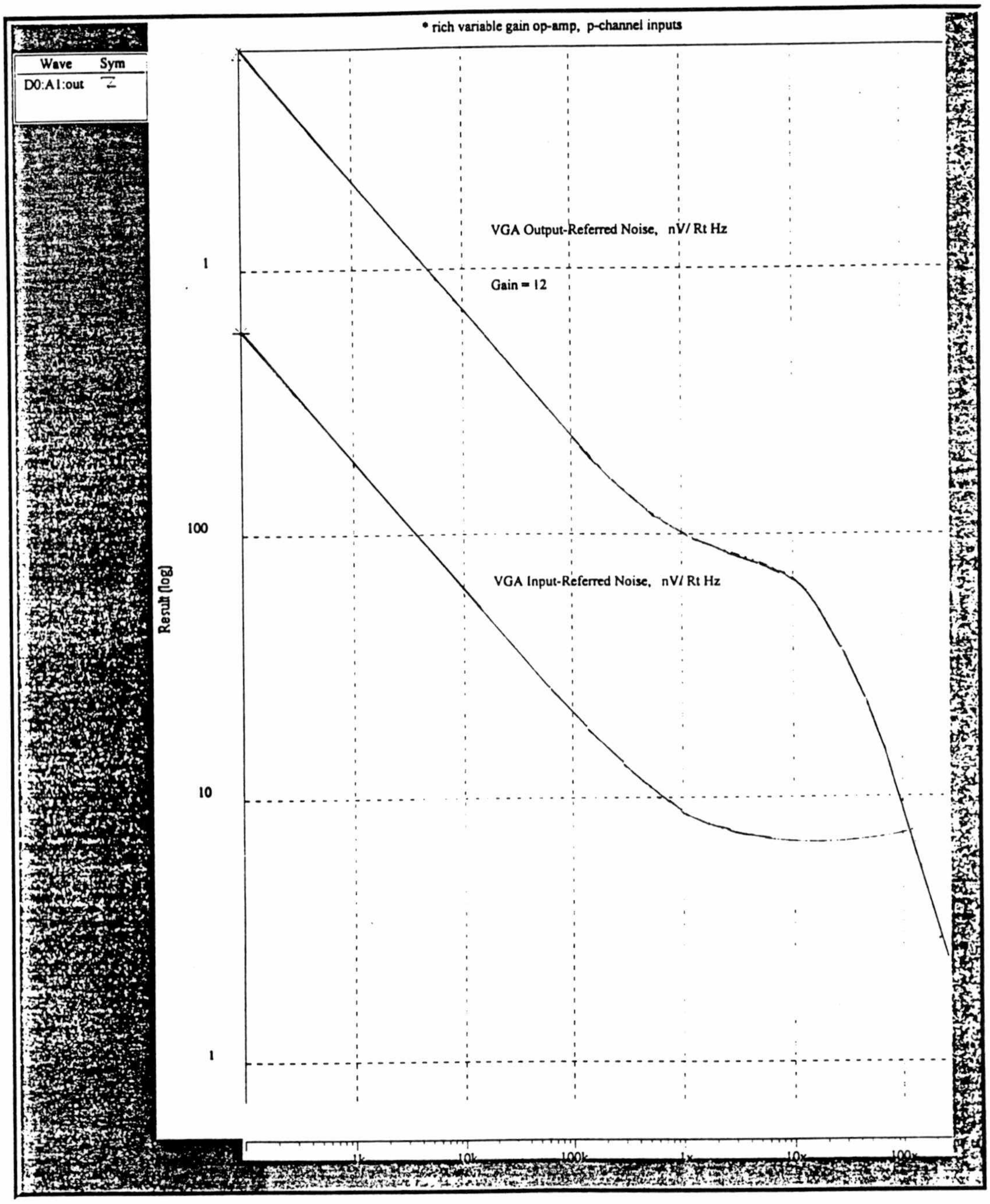


Figure 4.8 VGA Input and Output-Referred Noise, Gain=12, nV/Rt Hz

VGA operating at a gain of 12. The simulation reveals a 1/f noise corner at approximately 1 MHz, which is fairly consistent with measured data.

Chapter 5

Energy Channel Performance

5.1 Introduction

For the purpose of testing the RICH integrator and VGA, a testboard has been designed and assembled. The RICH prototype testboard contains independent voltage regulators and references for powering the amplifiers, along with a chip socket for the prototype RICH energy-channel test chip. The testboard also utilizes Elantec 2073 operational amplifiers as output buffers for the energy channel, along with an 8-bit DIP switch used for adjusting the gain and compensation of the VGA. The prototype RICH energy channel test chip, containing the integrator op-amp and the VGA, is fabricated in Orbit's 1.2u process. Twelve chips have been examined in all. Each test chip contains three integrators, and four VGAs. Three of the integrators and three of the VGAs are connected together to form three prototype "energy channels", and the remaining fourth VGA is a stand-alone device. In addition, a single integrator op-amp and a single VGA op-amp are present on the chip, fabricated without their associated feedback networks.

The integrator op-amp of Figure 3.1, along with the feedback capacitor, feedback reset MOSFET, input resistors R_1 and R_2, and capacitor C_1 are fabricated "on-chip". The external coupling capacitor C_C and the 50 ohm terminating resistor are external to the chip, mounted on the testboard. A means for adjusting the integrator's reset MOSFET gate bias voltage is provided via a potentiometer. The experimental results for the integrator are presented in Section 5.2.

The experimental results for the VGA are presented in Section 5.3. The VGA has been tested independently of the integrator, to establish baseline results for the VGA's risetime vs. gain, gain linearity vs. gain code, offset voltage, and noise performance.

5.2 Integrator Performance and Results

The RICH integrator must meet several important design criteria relevant to the RICH electronics specifications. Of primary importance to the RICH specifications are the integrator's risetime, charge gain and charge gain linearity, power consumption, decay time adjustability range, and noise performance. The charge gain linearity is measured for the system as a whole, including the integrator and VGA together, and is presented in the system results of Section 5.4. The noise performance of the integrator is discussed in Section 5.5. Other parameters which affect the ability of the integrator to function properly include the op-amp's slew rate, input offset voltage, and output dynamic range.

Figure 5.1 shows the measured pulse response for the integrator. The integrator must only respond with a positive-going output pulse, since the polarity of the PMT tends to pull charge out of the integrator, resulting in a positive output pulse. The risetime for the pulse response is approximately 9ns, which meets the 10ns risetime specification for the integrator. This measurement was taken with an oscilloscope probe attached to the output of the integrator op-amp. The probe capacitance is large enough to affect both the stability of the amplifier, as well as the slew rate. The actual risetime of the integrator is faster than that shown in Figure 5.1, since the probe capacitance tends to slow the integrator's output response somewhat.

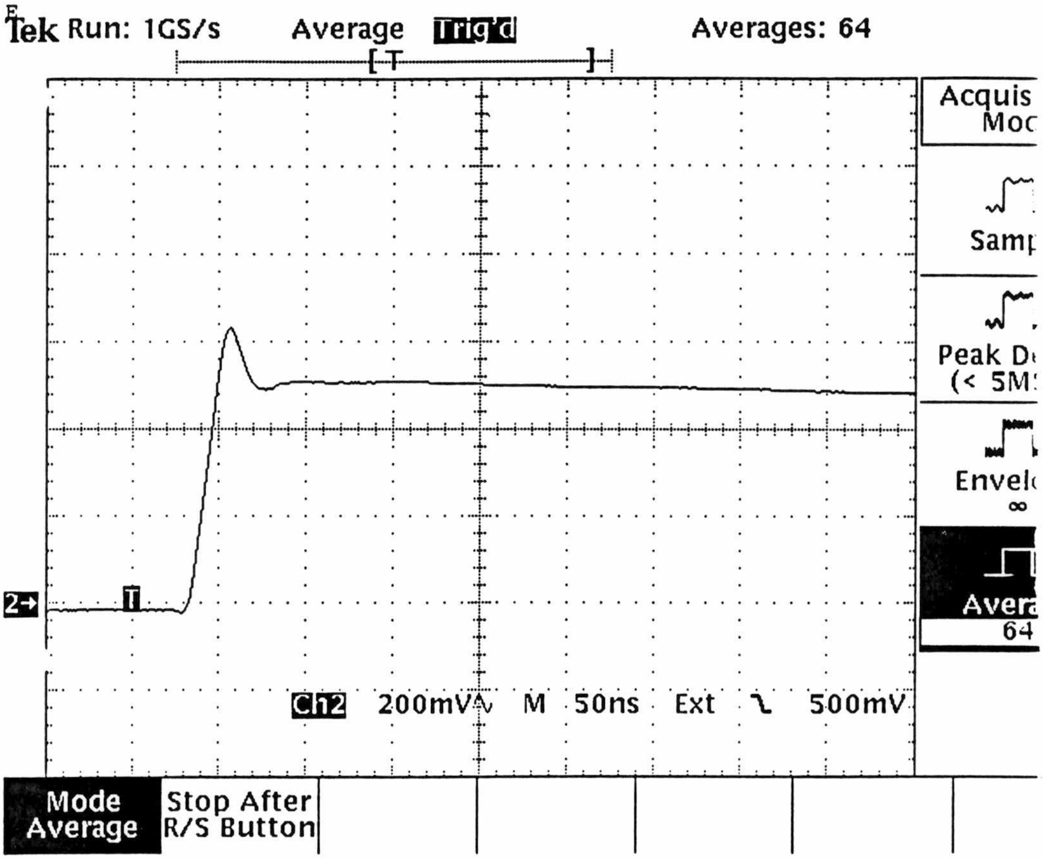


Figure 5.1 Integrator Pulse Response

Figure 5.2 shows the integrator's positive slew rate, again measured with a probe attached to the output of the integrator. The measured slew rate is 32.4 volts/microsecond, but this measurement is also affected by the probe capacitance. Since the integrator can provide approximately 800uA of drive current to the load, the 32.4 volt/microsecond slew rate indicates the presence of approximately 25pF of load capacitance, much of which is due to the probe. Again, the integrator slew rate is determined primarily by the large load capacitance and available drive current, and not as much by the compensation capacitance and differential pair bias current. The specification calls for an 80 volt/microsecond slew rate into a ~10pF load, 5pF of which includes the feedback capacitor. The measured slew with a 25pF load indicates that, for a 10pF load, the slew rate would improve to ~80 volts/microsecond, with the load capacitance still dominating the slew rate.

Figure 5.3 shows the measured range of adjustability for the integrator reset time, vs. the reset MOSFET gate bias voltage. The range for the reset gate bias voltage spans from about 2.7 volts to 4.75 volts, with the reset MOSFET source biased at 1.25V. Figure 5.4 shows a typical reset cycle, with a reset gate bias voltage of 3V. The integrator demonstrates some overshoot during reset, contributing to the extended settling times shown in Figure 5.4.

The power consumption for the integrator op-amp is approximately 6.74 milliwatts, operating from a 5V supply. The measured input-referred offset voltage for the integrator op-amp is 2.14mV, averaged over 12 different chips. The standard deviation in the offset voltage is 7.06mV, and the offset voltage range spans from -12.2mV to 14.9mV. The offset voltage measurements reveal a systematic positive offset

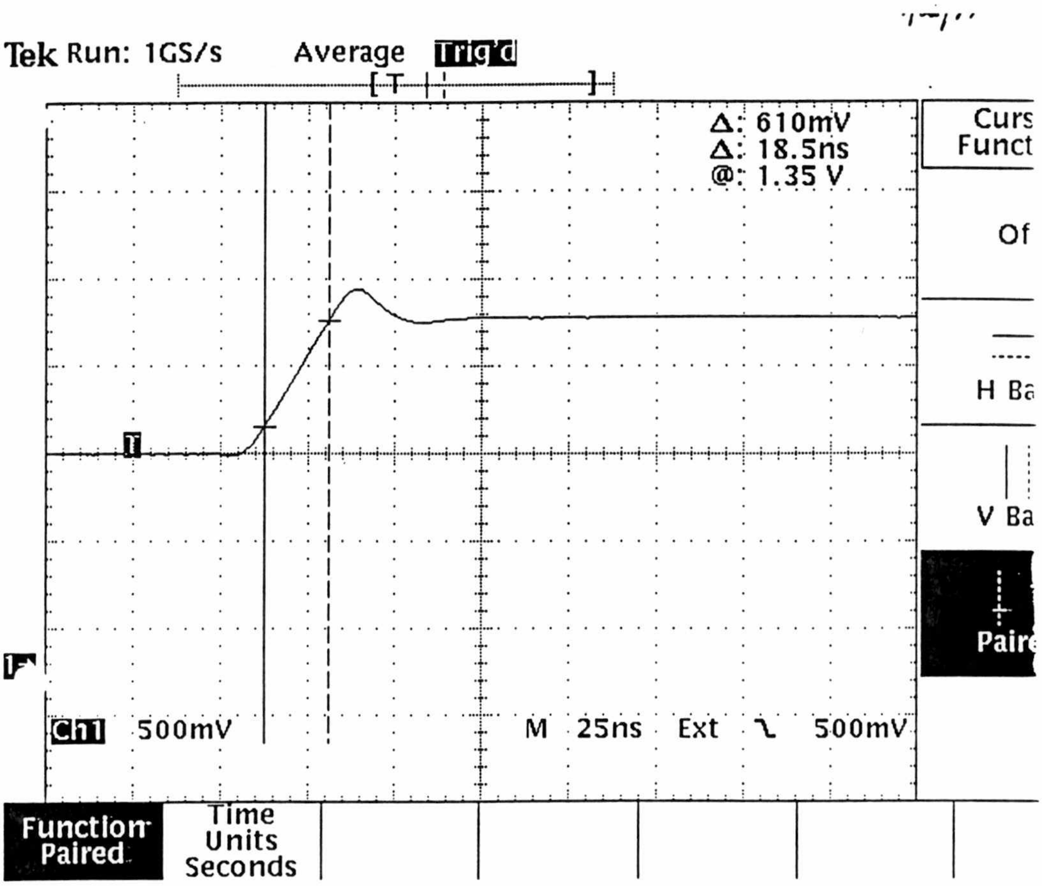


Figure 5.2 Integrator Positive Slew Rate, Measured

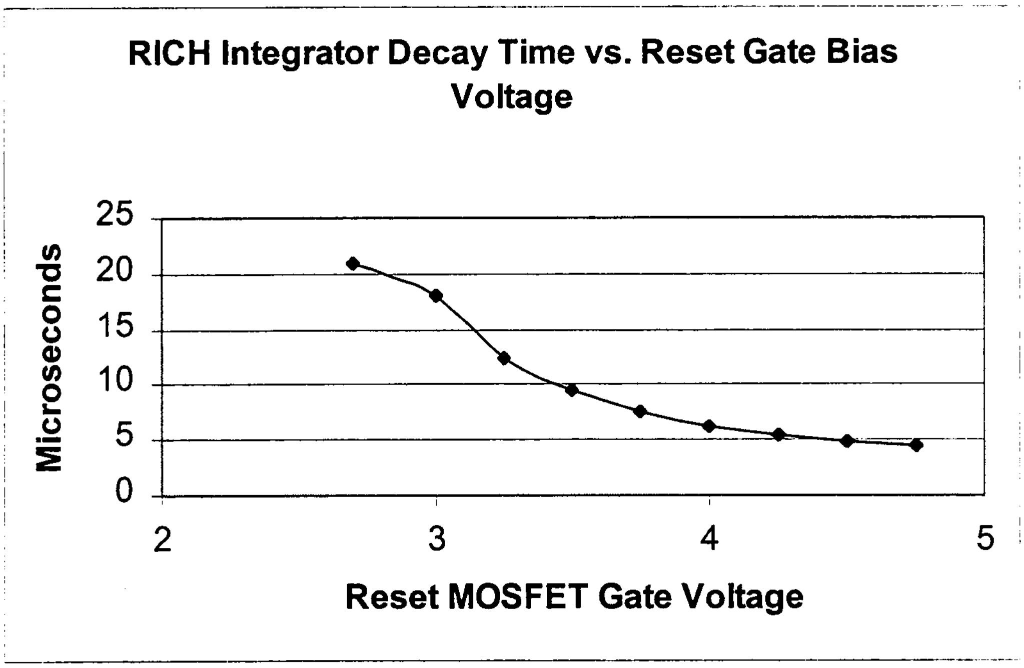


Figure 5.3 Integrator Decay Time vs. Reset MOSFET Gate Bias Voltage

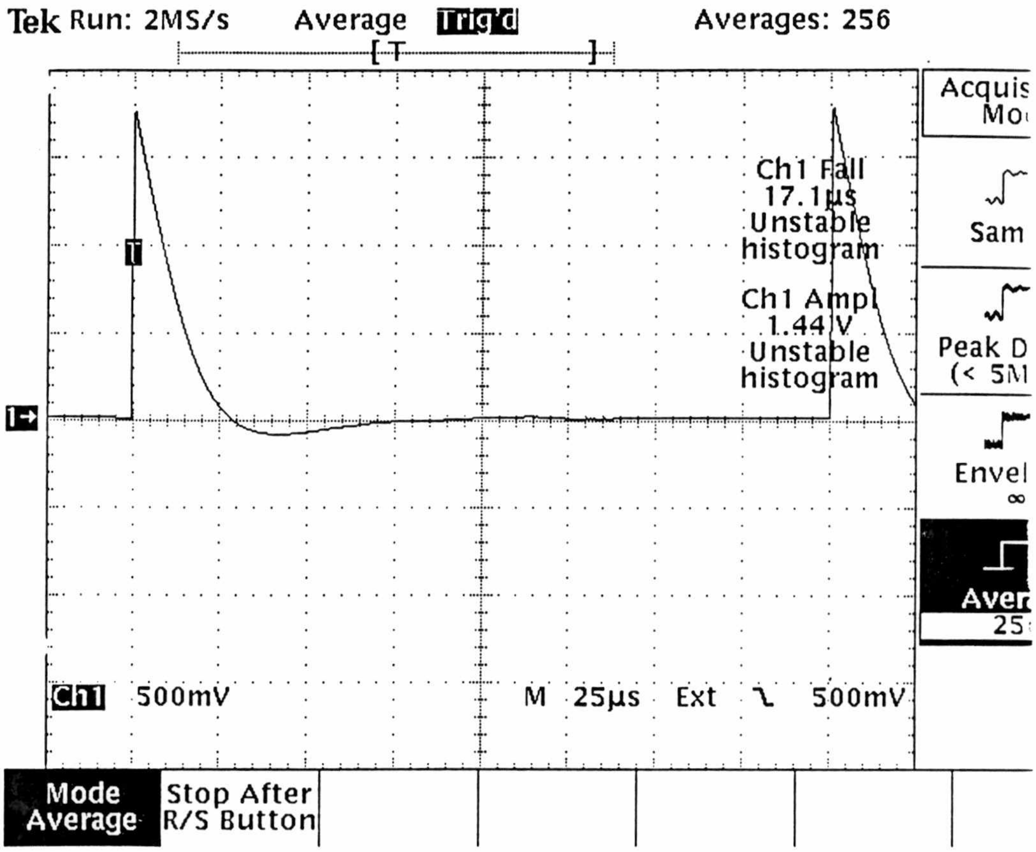


Figure 5.4 Typical Integrator Reset Cycle

voltage, which is predicted by SPICE and is a result of channel-length modulation effects which cause a slight imbalance in the gate-to-source voltages of output devices M6 and M7.

5.3 Variable Gain Amplifier Performance

The RICH variable gain amplifier (VGA) is used primarily to match the PMT gains to within 6% over a 3:1 range, while maintaining a risetime range of 10 to 20 ns. Thus, the primary performance criteria used to establish baseline results for the VGA include risetime vs. gain, gain linearity, and stability vs. gain. In addition, the VGA must meet a minimum positive slew rate requirement of approximately 162 volts/microsecond, have less than 100mV output offset, and have an output dynamic range of 3.25 volts. The output white noise PSD for the VGA is desired to be less than 10nV/Rt Hz, to minimize the white noise contribution due to the VGA for the integrating amplifier.

Figure 5.5 shows the measured VGA risetime vs. gain. The seven lines on the graph represent the different compensation capacitor combinations. For example, capacitor code "111" indicates all three compensation capacitors are switched in. Capacitor code "100" indicates that only the 0.8pF capacitor is switched in, and so forth. On the horizontal axis, a gain code of 0 corresponds to a gain of 4, while a gain code of 31 corresponds to a gain of 12. As expected, the VGA risetime increases both with increasing gain, and with increasing compensation capacitance. Figure 5.5 illustrates that, for any gain setting, a compensation capacitance combination is available which maintains the VGA risetime between 10 and 15ns.

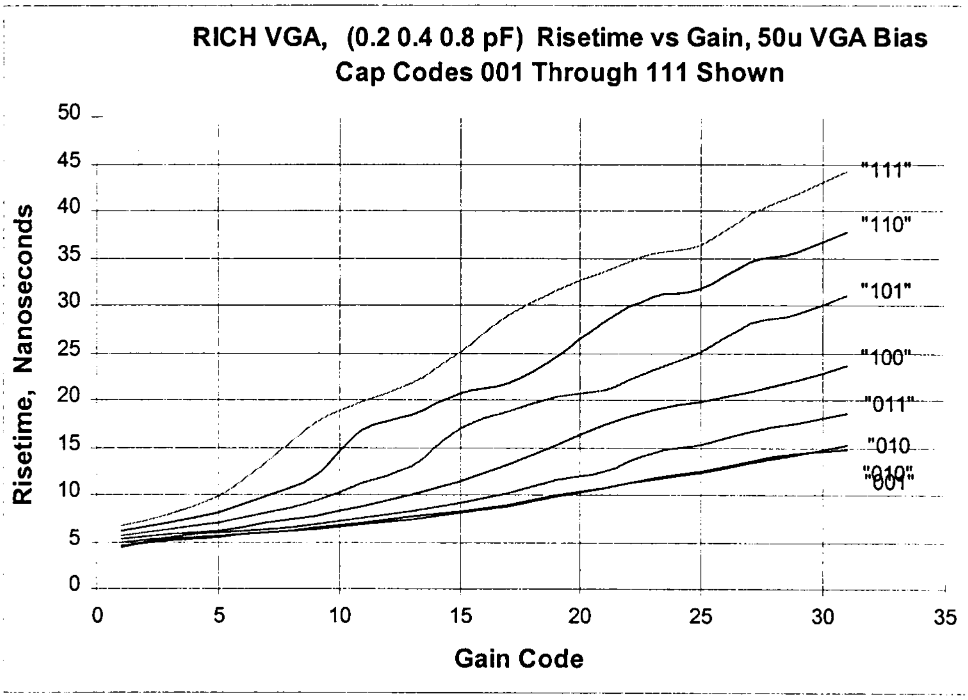


Figure 5.5 VGA Risetime vs. Gain

Figure 5.6 shows the results of an HSPICE simulation for the VGA, illustrating how the amplifier phase margin changes with changes in gain and compensation. The horizontal axis spans the gain range of times 4 to times 12, while the vertical axis shows the amplifier phase margin vs. the capacitor code. Only 5 capacitor codes, out of a possible 7, are shown on this plot for clarity. Capacitor code "001" corresponds to the minimum capacitance of 0.2pF, and as expected, yields the lowest phase margin vs. gain curve. Combining the results of Figure 5.6 with those of Figure 5.5 indicates that the VGA maintains both the desired bandwidth range along with exceptional stability over the operating gain range.

Figure 5.7 shows the measured VGA gain linearity, along with the percent INL. The percent INL is calculated from the deviation of the measured data with a least-squares fit of the measured data. The importance of Figure 5.7 relates to the ability of the VGA to match the PMT gains to within 6%. The worst case gain matching occurs at a gain of 4, where the fixed VGA gain stepsize is a relatively large percentage of the total gain. At a gain of 4, the VGA gain stepsize is approximately 5.5% to 6% of the total gain, while at a gain of 12, the VGA gain stepsize is approximately 2% of the total gain. The VGA's measured gain curve is monotonic, and demonstrates acceptable INL while meeting the gain matching requirement.

Figure 5.8 shows the measured 140 volt/microsecond positive slew rate for the VGA, using a cap code of "100". Figure 5.9 shows a typical pulse response for the VGA. The output pulse of Figure 5.9 was measured with a VGA gain of 8 and a capacitor code of "100". The low- overshoot, fast settling pulse response is typical of the total VGA gain range assuming utilization of the optimum capacitor code for any given gain.

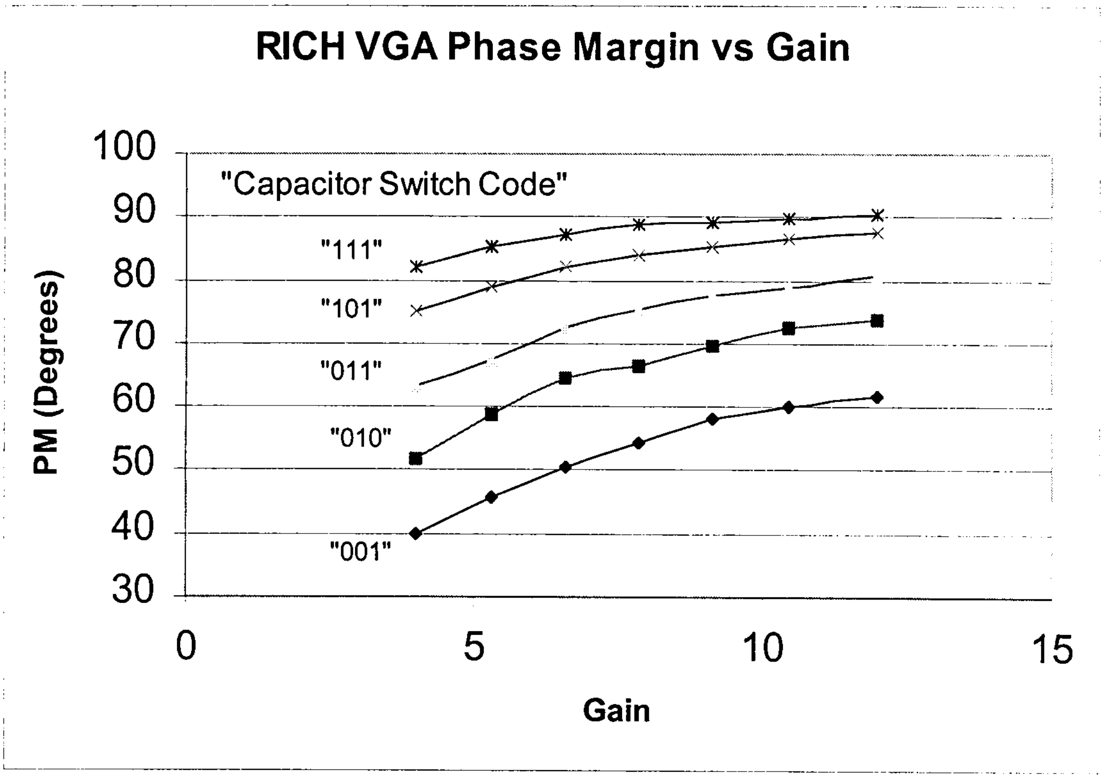


Figure 5.6 VGA Phase Margin vs. Gain

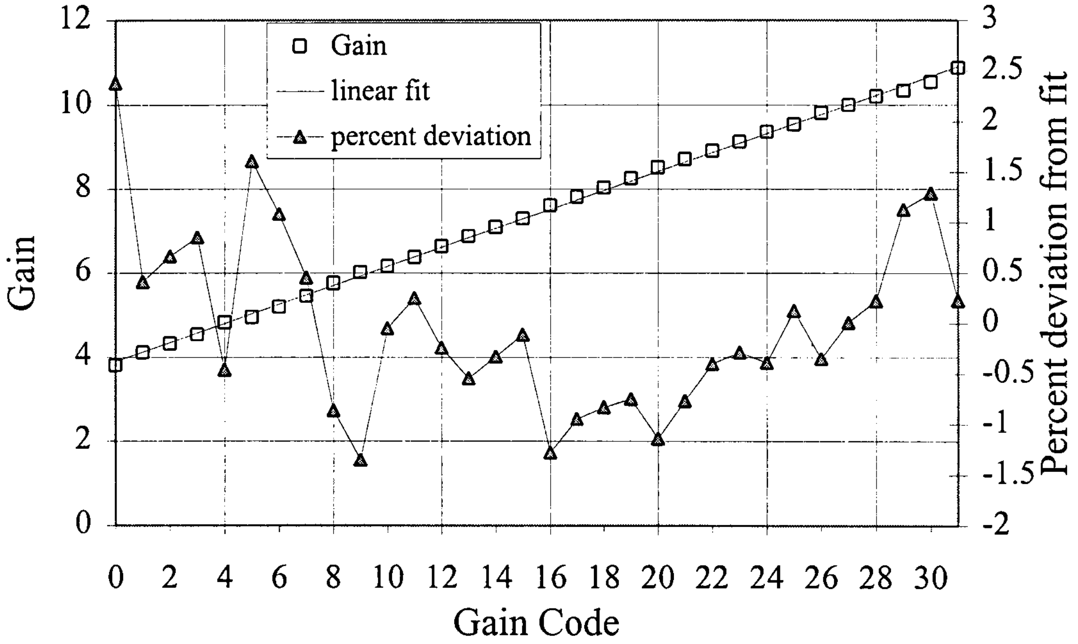


Figure 5.7 VGA Gain Linearity

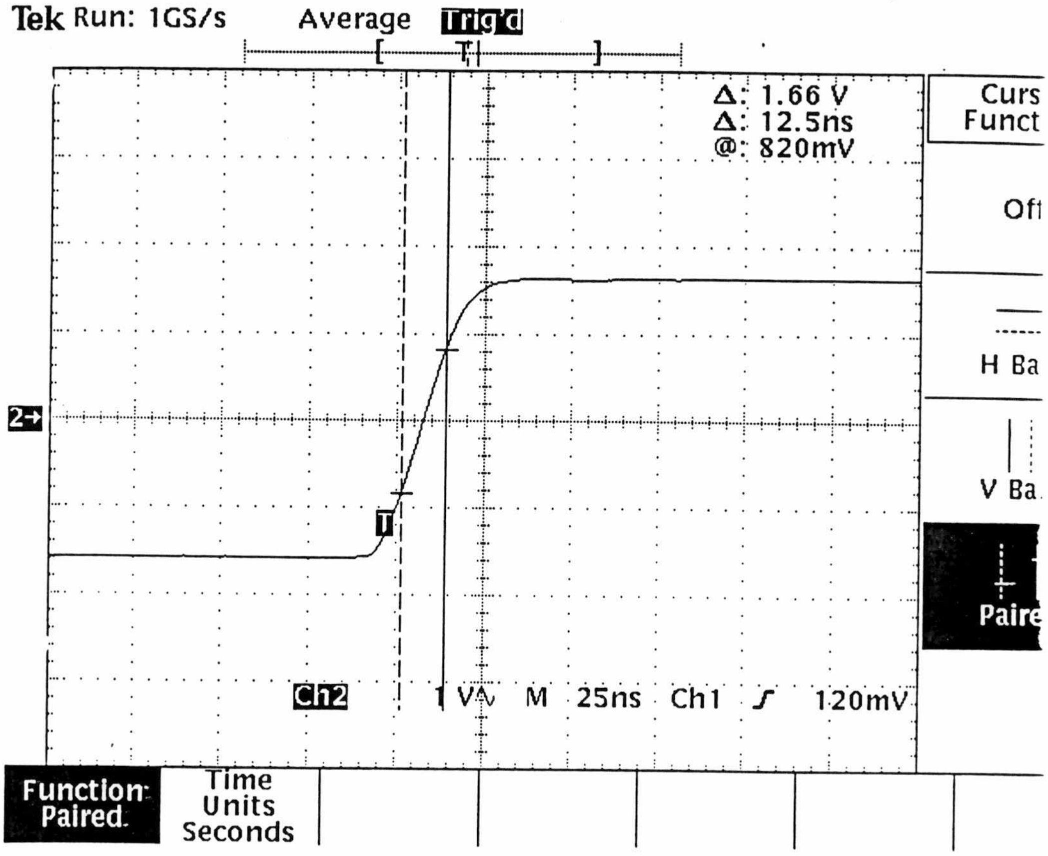


Figure 5.8 VGA Positive Slew Rate

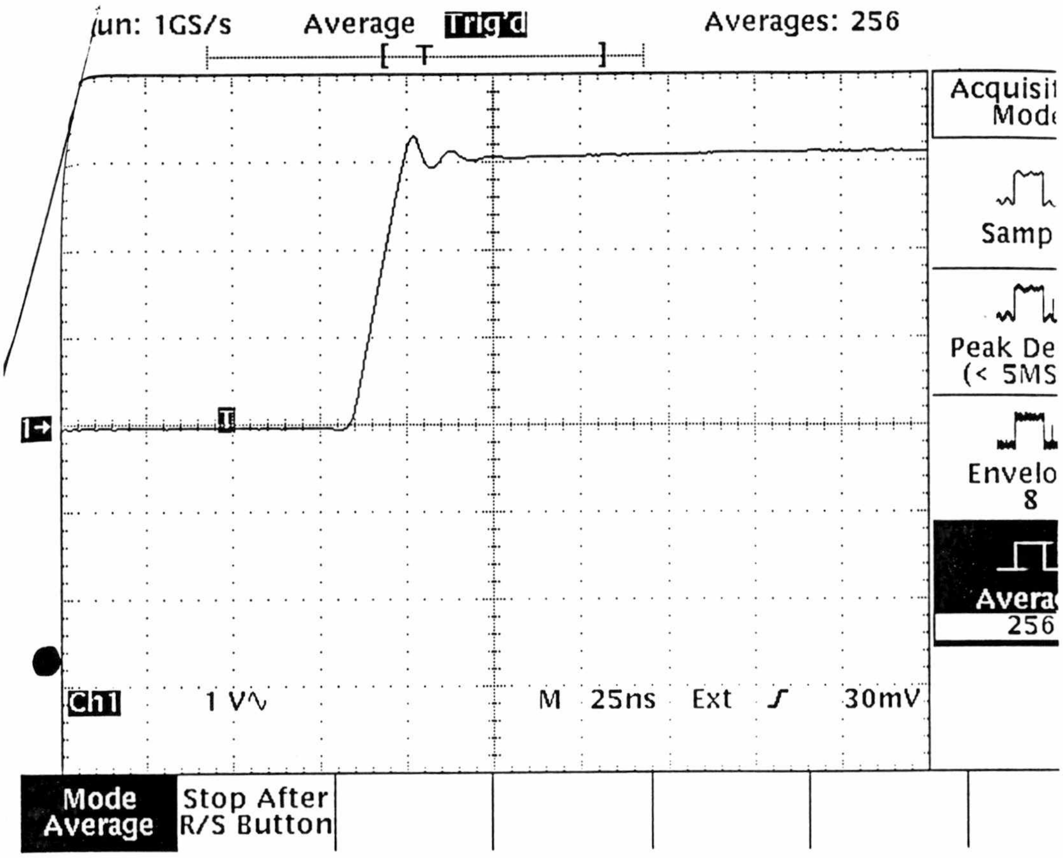


Figure 5.9 VGA Typical Pulse Response, Gain = 8, Cap Code = 100

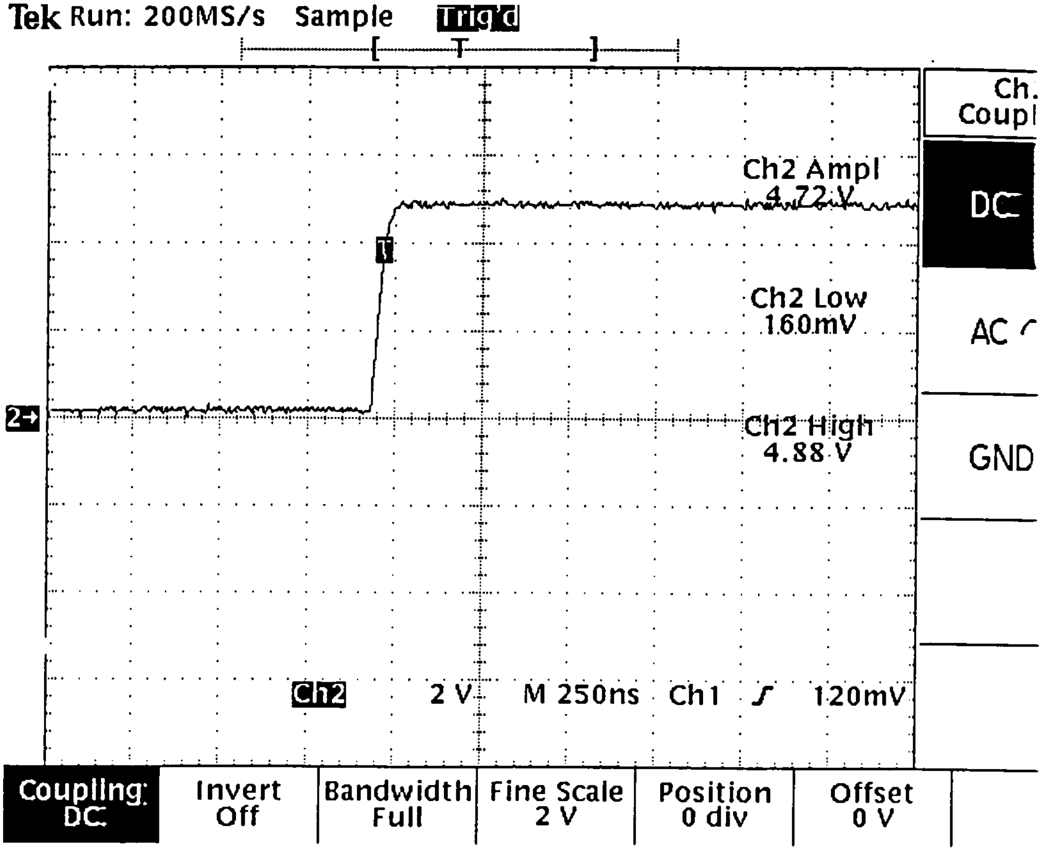
The input-referred offset voltage has been measured for twelve different VGA chips, and the average taken. The average input-referred offset voltage for the twelve chips is 4.97mV, revealing a positive systematic offset. The standard deviation in the input-referred offset is 6.84mV, with a range spanning –4.3mV to 17.9mV. In future chips, this systematic offset may be compensated out by further increasing the W/L ratio for device M10, as discussed in Chapter 4.

Power consumption for the VGA is 13.8mW, from a 5-volt supply. Figure 5.10 shows the measured output dynamic range of the VGA. With the output DC biased at 1.25V, and a desired output dynamic range of 3.25 volts, the VGA should be able to swing 4.5 volts peak at the output, from a 5 volt supply. The measured peak output voltage for the VGA is approximately 4.7 volts, with a 5 volt supply voltage. This peak output voltage measurement roughly agrees with the theoretical Vds_{SAT} for device M7, which is approximately $(V_{GS7}\text{-}V_{T7}) = 0.5$ volts, yielding a theoretical max output voltage of 4.5 volts.

5.4 Energy Channel System Transient Performance

The overall energy channel integrating amplifier consists of the integrator and VGA together. The primary performance criteria for the energy channel as a whole includes the system charge gain linearity, system risetime vs. VGA gain, and the system noise performance. The system noise performance is discussed in more detail in Section 5.4.

Figure 5.11 shows the charge gain linearity for the integrating amplifier system. The charge gain linearity is a measure of the linearity of the integrating amplifier output,



Ch2 Ampl 4.72 V

Ch2 Low 160mV

Ch2 High 4.88 V

Ch2 2 V M 250ns Ch1 ƒ 120mV

Coupling: DC

Invert Off

Bandwidth Full

Fine Scale 2 V

Position 0 div

Offset 0 V

Figure 5.10 VGA Output Dynamic Range

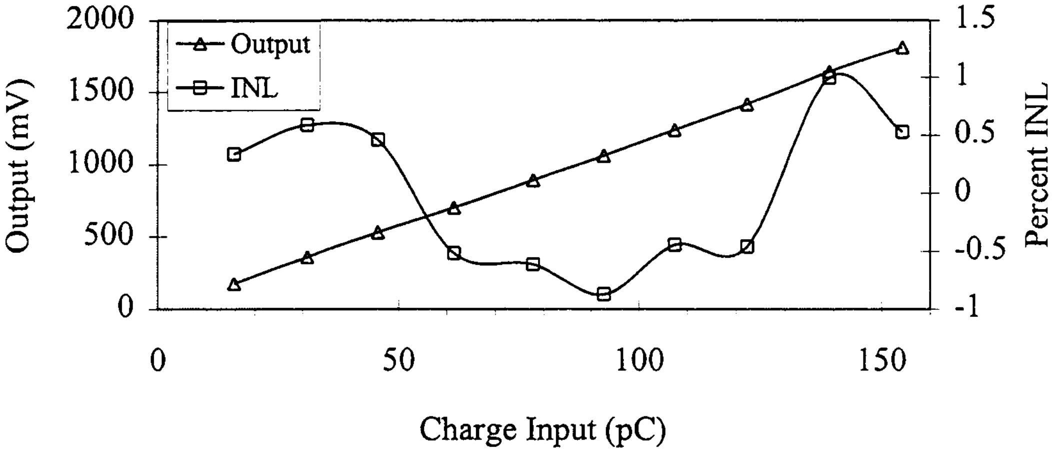


Figure 5.11 System Charge Gain Linearity

as the input charge is varied from the minimum of 16pC to the maximum of 160pC. Charge gain linearity is important since the integrating amplifier is used basically as an electron counter. The integrating amplifier output is proportional to the number of photoelectrons striking the detector. If the charge gain for the integrating amplifier is linear, the electron count becomes linearly proportional to the integrating amplifier output, which simplifies the software and calibrations downstream from the energy channel electronics.

In Figure 5.11, the charge input is actually a current pulse input to the integrator, generated by a Lecroy 9210 signal generator. The current pulse is integrated over time manually to determine the amount of charge going into the integrating amplifier. The input charge is varied from approximately 16pC to 160pC, and the integrating amplifier base-to-peak output is measured with an oscilloscope. For this figure, the VGA is set with a gain of 4. The integrating amplifier exhibits good charge gain linearity over the range of charge inputs, with an INL range of –0.87% to +0.99%. This INL range is sufficient for the RICH detector.

Figure 5.12 shows the system risetime vs. VGA gain code, for the seven possible VGA compensation capacitor codes. The data in Figure 5.12 was generated by applying a typical current pulse input to the integrator, and measuring the small-signal output response from the VGA while varying the gain and compensation. The overall system risetime can be maintained at or below approximately 23ns, by selecting the appropriate compensation capacitor setting which best optimizes the VGA's pulse response. The relatively quick risetime and settling times for the integrator and VGA allow time for the

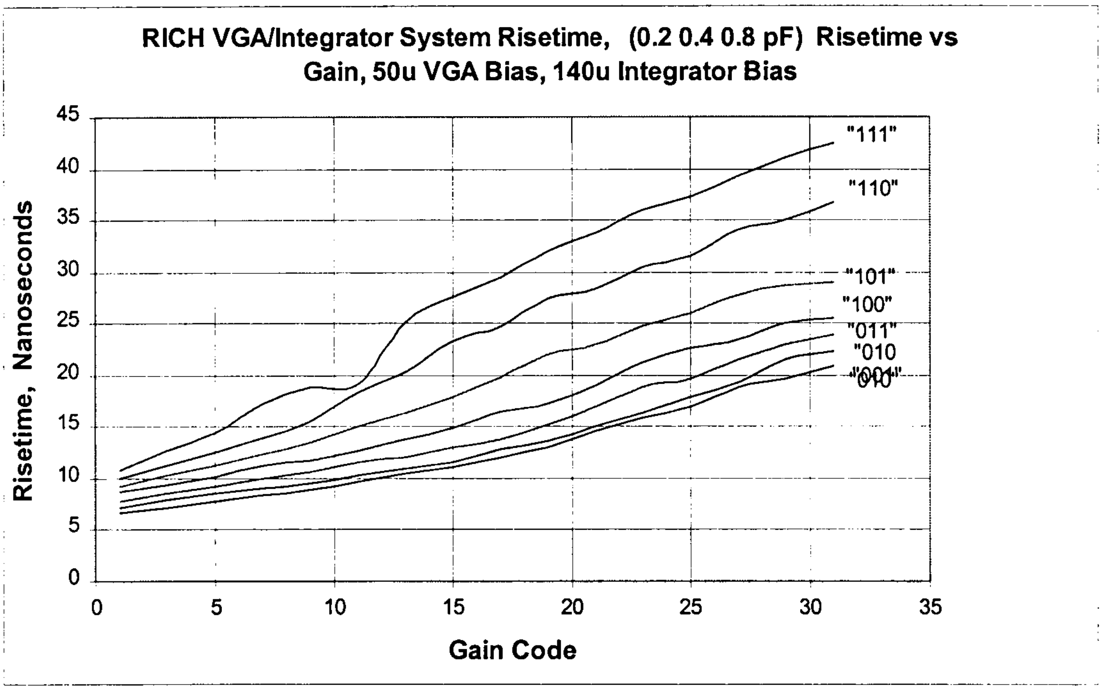


Figure 5.12 System Risetime vs. Gain

downstream trigger sum electronics to sum and settle well before the 100ns sampling deadline.

5.5 Energy Channel System Noise Performance

To evaluate the noise performance of the RICH energy channel integrating amplifier, consisting of the integrator and VGA, three different methods are employed. First, a noise model for the overall integrating amplifier is developed mathematically. This mathematical noise model establishes the noise power transfer function from the input of the integrating amplifier to the output, and provides much intuitive insight into the major noise contributors. Second, a SPICE noise model of the integrating amplifier is used to reinforce the validity of the mathematical model and to establish baseline noise results and design parameters for the chip. Third, noise measurements on the chip are performed to verify the actual noise performance of the integrating amplifier.

A simplified model of the integrating amplifier is shown in Figure 5.13. Several simplifying assumptions have been made which facilitate the derivation of an approximate, yet useable mathematical noise model. The dominant poles due to the integrator consist of the input pole defined by R_{IN} and C_C, and the feedback pole defined by R_F and C_F. The feedback reset MOSFET is modeled as a fixed resistor initially. The VGA is modeled as a single pole amplifier $A_{2(\omega)}$, and it is assumed initially that the noise of the variable gain amplifier is negligible compared to that of the integrator. This assumption is examined later. The software correlator is assumed to be noiseless, and the noise power spectral density of the amplifier is assumed to be white, that is, the 1/f term

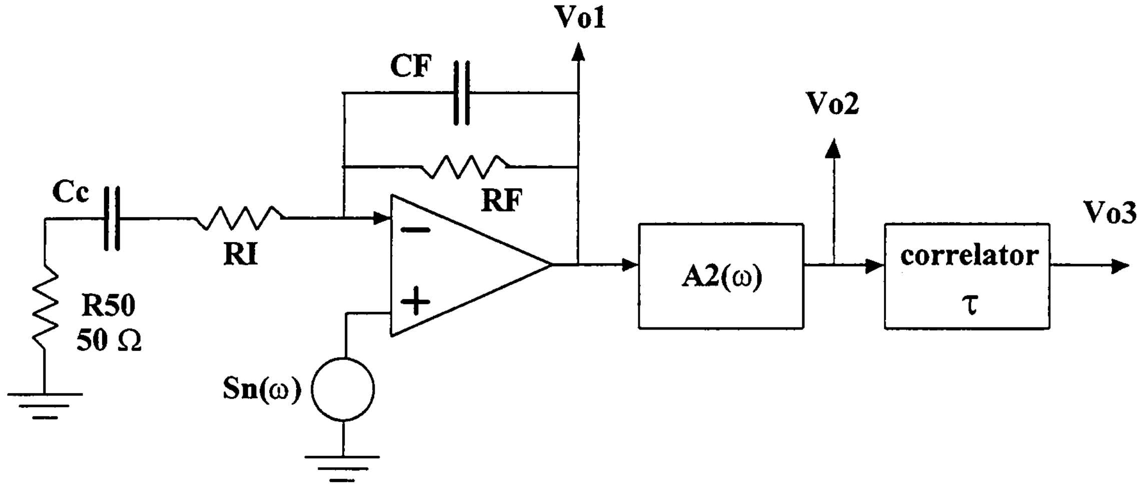


Figure 5.13 Noise Model For Integrating Amplifier

is not included. Neglecting the 1/f term is not a realistic assumption, but has little effect on the end result at the output of the correlator, due to the significant reduction in low-frequency noise through the correlator.

Figure 5.14 shows a block diagram for the double-correlated sampling process. The double-correlated sampling is used primarily as a high-pass filter, in order to reject any low-frequency noise which may have been amplified via the active integrator. Intuitively, the high-pass operation of the correlator is easy to understand. From Figure 5.14, the correlator subtracts a delayed version of the signal of interest from itself. In this case, the signal of interest is the output pulse from the VGA. Low frequency signals, which exhibit a high degree of correlation across the duration of the correlator delay time τ, are effectively canceled during the subtraction. High frequency signals, which are relatively uncorrelated across the correlator delay time τ, are passed.

The power transfer function for the correlator may be established as follows. Referring to Figure 5.14, the time domain input/output relation for the correlator is

$$X(t) = F(t) - F(t-\tau) \tag{5.1}$$

The Fourier transform of Equation 5.1 reveals the frequency-domain relationship to be

$$X(\omega) = F(\omega) - F(\omega)e^{-j\omega\tau} \tag{5.2}$$

$$H(\omega) = {X(\omega)}\big/{F(\omega)} = 1 - e^{-j\omega\tau} \tag{5.3}$$

The power transfer function for the correlator from input to output is expressed as HH^*, according to Equation 5.4.

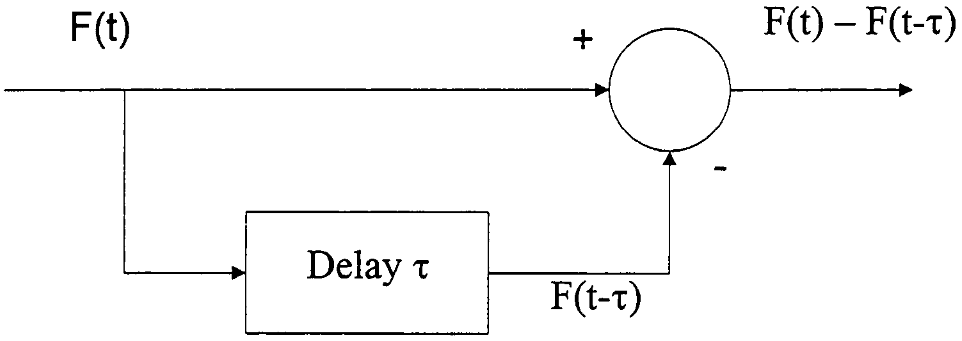


Figure 5.14 Double-Correlated Sampling Process

$$H(\omega)H^{*}(\omega) = (1 - e^{-j\omega\tau})(1 - e^{+j\omega\tau}) = 2(1 - \cos(\omega\tau)) = 4\sin^{2}\left(\frac{\omega\tau}{2}\right) \tag{5.4}$$

The variable gain amplifier is represented in Figure 5.13 by the block $A_{2(\omega)}$. The VGA is assumed to have a transfer function represented by a single pole of the form

$$A_{2(\omega)} = \frac{A_2}{1 + j\left(\omega/\omega_2\right)} \tag{5.5}$$

where A_2 is the VGA closed loop gain and ω_2 is the VGA's closed loop high frequency dominant pole.

The major noise contributors in the noise model of Figure 5.13 include the integrator input resistance, the equivalent input noise voltage of the integrator op-amp, and the feedback reset device. The noise contribution of the VGA will be examined separately.

At this point, some observations about modeling the feedback reset MOSFET as a fixed resistor should be mentioned. The reset MOSFET is biased in the linear region, and has a calculable resistance, essentially looking like a fixed resistor from a circuit bandwidth perspective. The primary noise sources include the gate leakage shot noise, given by i_G^2, and the drain-to-source current generator i_D^2. The gate leakage shot noise current may be neglected in this analysis, since the reset MOSFET gate driving impedance is small. The drain-to-source current generator i_D^2 consists of thermal noise due to the channel resistance, as well as flicker noise. For simplicity, the 1/f flicker noise component of the MOSFET is assumed not to be present in this analysis. This may not be a realistic assumption, but since the correlator attenuates low frequencies, the result at the correlator output will not change significantly. The i_D^2 term in the deep ohmic region is given by [10]

$$i_D^2 = 4kT(g_{DS}) \tag{5.6}$$

which represents the thermal noise due to the channel. The MOSFET channel conductance is represented by g_{DS} in Equation 5.6. With a gate bias voltage of 4 volts, implying a V_{GS} of 2.75 volts, the channel resistance is approximately 559k ohms as modeled from SPICE. From a bandwidth and noise perspective, the MOSFET therefore looks like a 559k resistor.

For the noise model derivation, it is helpful to define several variables which relate to the model. Referring to Figure 5.13, let

$$R_{IN} = R_I + R_{50} \tag{5.7}$$

$$\omega_I = \frac{1}{R_{IN}C_C} \tag{5.8}$$

$$\omega_F = \frac{1}{R_F C_F} \tag{5.9}$$

$$\omega_O = \frac{1}{R_F C_C} \tag{5.10}$$

$$Z_F = R_F \left\| \left(\frac{1}{sC_F} \right) \right. \tag{5.11}$$

$$Z_I = R_{IN} + \left(\frac{1}{sC_C} \right) \tag{5.12}$$

and

$$S_n(\omega) = e_n^2 + \frac{K_F}{\omega} \tag{5.13}$$

Equation 5.13 represents the equivalent input noise PSD for the integrator op-amp as consisting of a white noise component and a flicker noise component. Again referring to Figure 5.13, let $S_{no2}(\omega)$ be the single-sided noise power spectral density at the output of the VGA (V_{o2}), and let $S_{no3}(\omega)$ be the single-sided noise power spectral density at the output of the correlator (V_{o3}). The noise power spectral density at the VGA output may be expressed as

$$S_{no2}(\omega) = \left[4kTR_I \left| \frac{Z_F}{Z_I} \right|^2 + (e_n^{\ 2} + \frac{K_F}{\omega}) \left| 1 + \frac{Z_F}{Z_I} \right|^2 + 4kTR_F \left(\frac{1}{1 + \frac{\omega^2}{\omega_F^{\ 2}}} \right) \right] \left(\frac{A_2^{\ 2}}{1 + \frac{\omega^2}{\omega_2^{\ 2}}} \right) \qquad \textbf{(5.14)}$$

Integrating Equation 5.14 yields the mean-square noise voltage at the output of the VGA. In order to establish a closed-form solution for this integral, the approximation $1+Z_F/Z_I \approx Z_F/Z_I$ is made. This approximation is reasonable for calculating the total circuit noise since Z_F/Z_I is much greater than 1 over the area of interest. Equation 5.14 may be further simplified by noting that the decay time of the integrator is very long compared to the risetime of the VGA, or in other words, $\omega_F << \omega_2$ and ω_F determines the high frequency bandwidth. With these simplifications, Equation 5.14 reduces to

$$S_{no2}(\omega) = \left[\frac{\left(4kTR_I + e_n^{\ 2}\right)\left(\frac{\omega^2}{\omega_O^{\ 2}}\right) + K_F\left(\frac{\omega}{\omega_O^{\ 2}}\right)}{1 + \frac{\omega^2}{\omega_I^{\ 2}}} + 4kTR_F \right] \left(\frac{A_2^{\ 2}}{1 + \frac{\omega^2}{\omega_F^{\ 2}}} \right) \qquad \textbf{(5.15)}$$

The total noise power at the output of the VGA may be expressed as

$$\overline{e_{no2}^{\ 2}} = \int_0^\infty S_{no2}(\omega)d\omega \qquad \textbf{(5.16)}$$

A closed-form solution for the integral of Equation 5.15, represented by Equation 5.16, has been obtained. Evaluating the integral yields the solution for the noise power at the VGA output, expressed by

$$\overline{e_{no2}^{2}} = \frac{\pi K_1 \omega_I^2 \omega_F^2}{2\omega_O^2(\omega_I + \omega_F)} + \frac{\pi K_2 \omega_F}{2} + \frac{K_F A_2^2 \omega_I^2 \omega_F^2}{2\omega_O^2}\left(\frac{\ln(\omega_I^2) - \ln(\omega_F^2)}{\omega_I^2 - \omega_F^2}\right) \quad \textbf{(5.17)}$$

where

$$K_1 = A_2^2\left(\frac{4kTR_I}{2\pi} + e_n^2\right) \quad \textbf{(5.18)}$$

and

$$K_2 = A_2^2\left(\frac{4kTR_F}{2\pi}\right) \quad \textbf{(5.19)}$$

Referring again to Figure 5.13, $S_{no3}(\omega)$ represents the noise power spectral density at the output of the correlator. Combining Equations 5.4 and 5.15 yields the simplified expression for the noise power spectral density at the correlator output, given by Equation 5.20.

$$S_{no3}(\omega) = \left[\frac{\left(4kTR_I + e_n^2\right)\left(\frac{\omega^2}{\omega_O^2}\right) + K_F\left(\frac{\omega}{\omega_O^2}\right)}{1 + \frac{\omega^2}{\omega_I^2}} + 4kTR_F\right]\left(\frac{A_2^2}{1 + \frac{\omega^2}{\omega_F^2}}\right)\left(2(1 - \cos(\omega\tau))\right) \quad \textbf{(5.20)}$$

The noise voltage power at the output of the correlator may be expressed as

$$\overline{e_{no3}^{2}} = \int_0^\infty S_{no3}(\omega)\,d\omega \quad \textbf{(5.21)}$$

A closed form solution for the integral of Equation 5.20, represented by Equation 5.21 has been obtained, neglecting the $K_F\omega/\omega_O^2$ term. This term may be neglected with very little loss of accuracy in the closed form solution for Equation 5.21, since the correlator significantly reduces the contribution from the 1/f noise component. The closed form solution of Equation 5.21 yields the noise voltage power at the output of the correlator, given by

$$\overline{e_{no3}^{\,2}} = K_3\left[1-\frac{\omega_I e^{-\omega_I\tau}-\omega_F e^{-\omega_F\tau}}{\omega_I-\omega_F}\right]+K_2\pi\omega_F\left(1-e^{-\omega_F\tau}\right) \tag{5.22}$$

where

$$K_3 = \frac{\pi A_2^{\,2}\left(\frac{4kTR_I}{2\pi}+e_n^{\,2}\right)\omega_I^{\,2}\omega_F^{\,2}}{\omega_O^{\,2}\left(\omega_I+\omega_F\right)} \tag{5.23}$$

Equations 5.17 and 5.22 thus yield the total noise power before and after correlation, respectively. Equation 5.14, which is the exact (unsimplified) equation for the output noise PSD and includes the 1/f integrator noise model, is integrated numerically for both pre and post correlation cases, allowing a comparison between the simplified and unsimplified models. The noise of the VGA op-amp is not included in the analytical model at this point, since the first-stage integrator is considered to be the dominant noise source in this analysis.

Table 5.1, Table 5.2, and Table 5.3 present the results of Equations 5.14, 5.17 and 5.22 in tabular form for comparison purposes. Table 5.1 also presents measured results from the integrating amplifier, taken from data gathered by an HP3589 spectrum analyzer. In evaluating Equations 5.14, 5.17, and 5.22, the following parameters are used: R_{IN} = 3150 ohms, C_C=0.01uF, C_F=5pF, R_F=559K, VGA Gain = 8, τ=300ns, e_n=4.775*10^{-18} V^2/Rad/s (normalized to radians/second) for the integrator op-amp, and KF =6*10^{-12} for the integrator op-amp flicker noise, yielding a 1/f noise corner at

Table 5.1 Integrating Amplifier Output Noise

Method	Noise at VGA Output (mV rms)	Noise After Correlation (mV rms)
Spectrum Analyzer	11.2	3.56
HSPICE	8.8	2
Equation 5.14 Unsimplified Numerical Solution	8.0	Does Not Apply
Equation 5.17 Closed-form Integration Solution of simplified Equation 5.14 ($1+Z_F/Z_1 \approx Z_F/Z_1$)	6.6	Does Not Apply
Equation 5.20 Unsimplified Numerical Solution	Does Not Apply	1.90
Equation 5.22 Closed Form Integration Solution of Simplified Equation 5.20 (neglects 1/f, $1+Z_F/Z_1 \approx Z_F/Z_1$)	Does Not Apply	1.74

Table 5.2 % Noise Power Contribution From Each Source At The VGA Output, Based on Eq. 5.14

Noise Source	Percent Contribution at VGA Output
R_{IN}	12.70
e_n of Integrator Op-Amp	7.25
Flicker Noise of Integrator Op-Amp	79.90
R_F	< 1

Table 5.3 % Noise Power Contribution From Each Source At The Correlator Output, Based on Eq. 5.14 Multiplied By Correlator Transfer Function

Noise Source	Percent Contribution at Correlator Output
R_{IN}	49.4
e_n of Integrator Op-Amp	31.7
Flicker Noise of Integrator Op-Amp	18.8
R_F	< 1

200KHz. This 1/f noise corner is based on SPICE simulations of the integrator op-amp, and agrees relatively well with measured data. The value used for R_F is approximate with respect to the actual noise generated by the MOSFET; however, the percent noise contribution due to R_F is very small, so that this approximation does not significantly affect the results. Table 5.2 presents a breakdown of the major circuit noise contributors, along with the percent noise contribution at the VGA output due to each source based on the results of Equation 5.14. Similarly, Table 5.3 presents a breakdown of the major circuit noise contributors along wit the percent noise power contribution at the output of the correlator. In Table 5.1, the noise PSD generated from the spectrum analyzer is numerically integrated to generate the rms noise results. To obtain the noise after correlation, the noise PSD generated from the spectrum analyzer is applied to a software correlator, and the output of this software correlator is numerically integrated to determine the rms noise after correlation. In this case, Microsoft Excel is used to execute a correlation routine on the original spectrum analyzer PSD data. Excel is also used to numerically integrate the pre and post correlation PSD to obtain the rms values.

Figure 5.15 illustrates a plot of Equations 5.14, 5.15 and 5.20, representing the calculated exact and approximate theoretical noise PSD at the output of the VGA and at the output of the correlator, respectively. For comparison purposes, Figure 5.16 shows the measured PSD from the output of the VGA, with the VGA set for a non-inverting gain of 8. Figure 5.16 also shows the effect of the double-correlated sampling process on the measured PSD. To generate the post-correlation data in Figure 5.16, the measured PSD data is imported into Microsoft Excel, multiplied by the correlator transfer function, and graphed alongside the measured data.

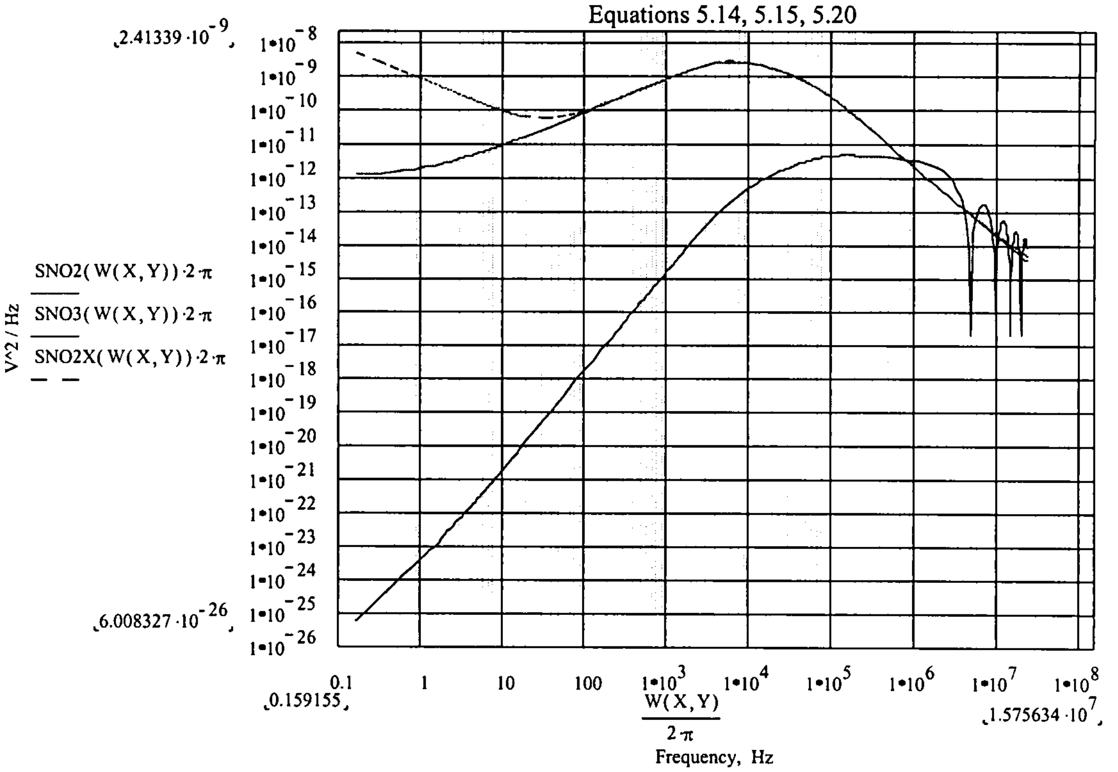


Figure 5.15 **Equations 5.14 5.15 and 5.20, Pre and Post Correlation, Theoretical. Top Trace Represents Eq. 5.14, Middle Trace Represents Eq. 5.15, Bottom Trace Represents Eq. 5.20**

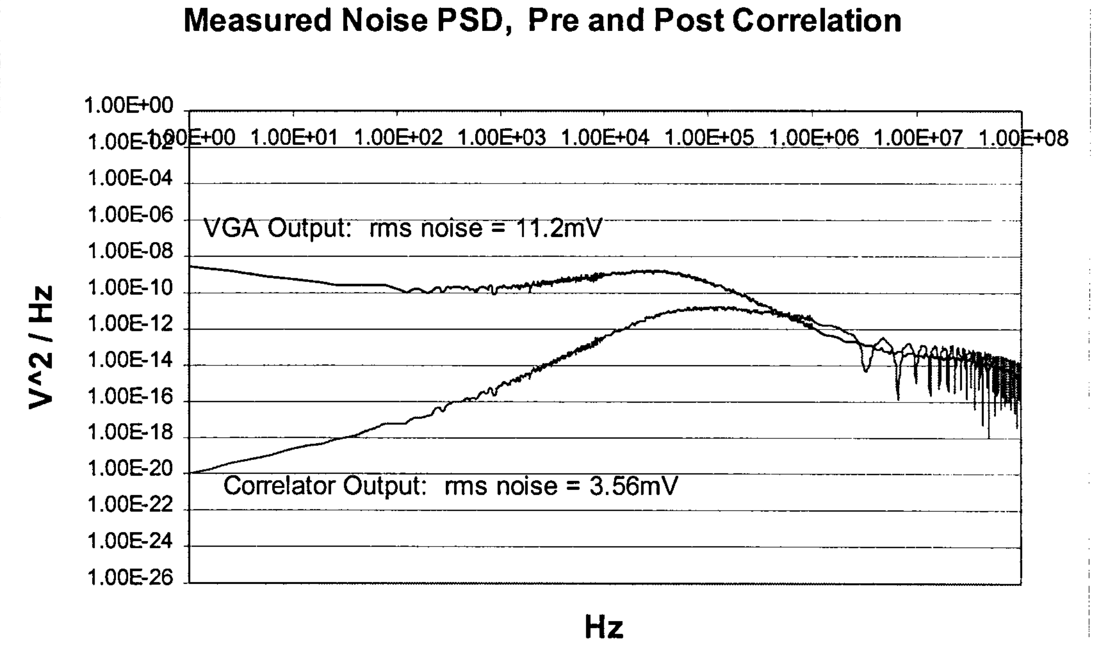


Figure 5.16 Measured Pre and Post Correlation PSD

Figure 5.15 provides some insight into the usefulness of the approximation $1+Z_F/Z_1 \approx Z_F/Z_1$. The top trace in Figure 5.15 represents the exact Equation 5.14, while the middle trace represents Equation 5.15 which applies the approximation $1+Z_F/Z_1 \approx Z_F/Z_1$. From Figure 5.15, it is evident that this approximation is very good for frequencies above about 100 Hz. Below 100 Hz, the approximation underestimates the noise contribution.

A comparison of Figures 5.15 and 5.16 reveals that Equation 5.14 provides a fairly good model for the noise PSD at the output of the VGA. The PSD predicted by Equation 5.14 peaks at a slightly lower frequency than the measured data. This difference is most likely due to error in the calculated value of the feedback resistance used for the reset MOSFET. Small variations in the reset MOSFET gate bias voltage cause relatively large changes in the MOSFET "on" resistance, which significantly affect the noise bandwidth of the integrating amplifier.

Similarly, small variations in parameters such as KF, e_n, and R_F can cause large variations in the output noise predicted by Equations 5.14 through 5.22. In general, Equations 5.14 through 5.22, as well as HSPICE, tend to underestimate the output noise power, typically at frequencies below 10KHz. Part of this error is likely due to additional noise sources on the chip testboard, such as the 1.25-volt reference for the integrator op-amp. The 1.25-volt reference in particular is known to generate additional 1/f noise in the 0-10KHz bandwidth. This noise source feeds directly into the non-inverting input of the integrator. Also, the 1/f noise corners used in Equations 5.14 through 5.22 are based on HSPICE simulation results, which may not accurately model the noise of the actual circuit. From the results presented in Table 5.2, the active integrator is shown to be very sensitive to low-frequency noise. Small changes in the 1/f noise corner in the integrator op-amp can produce large changes in the resulting output noise.

The double-correlated sampling process is a natural complement for the active integrator, since the correlator acts as a high-pass filter. Figures 5.15 and 5.16 indicate that the correlator significantly reduces the noise PSD contribution at relatively low frequencies. The correlator delay time τ is chosen to be short enough so that the low frequencies to be rejected have a high degree of correlation across the delay time, but long enough so that the high frequencies of interest are uncorrelated across τ. However, the correlator also adds to the noise PSD at high frequencies. An analysis of the data in Figures 5.14 and 5.15 reveals that the correlator adds approximately 50% more rms noise from roughly 1MHz to 100MHz. The subtraction of low frequency noise greatly offsets this high frequency noise addition for the RICH integrating amplifier application, though.

As a result of the active integrator's sensitivity to low-frequency noise, careful attention must be paid to minimizing the low-frequency bandwidth of the active integrator. Relying on the correlator to reduce low-frequency noise is not an entirely acceptable solution, since the correlator reduces 1/f noise at the output only, and not at any intermediate nodes. Since the VGA output is required to swing close to the rail, any low-frequency noise which appears at the VGA output may conceivably drive the VGA into the voltage rail, obscuring the desired signal. Hence, it is necessary to minimize the noise bandwidth of the integrating amplifier prior to the correlation process.

Referring again to Figure 5.13, coupling capacitor C_C is primarily used as a DC blocking capacitor. However, the proper choice for C_C is not arbitrary; rather, C_C is chosen so as to limit the low-frequency bandwidth of the active integrator. In the transfer function for the integrator, there exists a zero at DC, and the first pole occurs at approximately $1/R_{IN}C_C$. By making C_C small, this low-frequency pole is shifted upwards in frequency, thereby limiting the low-frequency bandwidth of the active integrator. If C_C is made too small, however, then the time constant C_CR_{IN} begins to dominate over the R_FC_F time constant, and the integrator reset time becomes overly dependent on C_C. As mentioned in Chapter 3, the 0.01uF coupling capacitor achieves a good balance between the adjustable reset time specification and low-frequency noise rejection.

The above analysis neglects any noise at the output due to the VGA. To establish the noise contribution from the VGA, the noise model of Figure 5.17 is used. The VGA operates at a closed-loop gain of 8 for this analysis, with an 8456 ohm feedback resistor and a 1208 ohm R_I resistor. The primary noise sources include the white noise and flicker noise components from the VGA's differential pair, represented by e_n and KF/ω in Figure 5.17. Additionally, resistors R_F and R_I provide a thermal noise contribution at the output. The expression for the output noise power spectral density of the VGA may be expressed as

$$e_{OUT}{}^2 = \left(e_n{}^2 + \frac{KF2}{\omega}\right) * \left(\frac{8^2}{1+\frac{\omega^2}{\omega_2{}^2}}\right) + \frac{4kTR_I}{2\pi}\left(\frac{7^2}{1+\frac{\omega^2}{\omega_2{}^2}}\right) + \frac{4kTR_F}{2\pi} \qquad \textbf{(5.24)}$$

Equation 5.24 assumes a single-pole closed-loop response from the VGA. Typical values for Equation 5.24 are e_n=6.5nV/Rt Hz, KF2=$4.225*10^{-11}$ (normalized to V^2 / radian/s) for a 1 MHz 1/f noise corner, and ω_2 = 28.75MHz*2*π at a non-inverting gain of 8. A numerical integration of Equation 5.24 (with values normalized for V^2/Radian/s) yield the total noise power at the output of the VGA due to the VGA, and the square root yields the

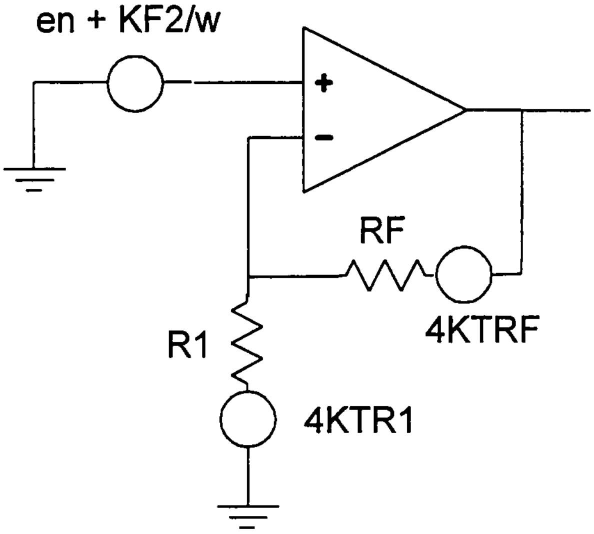


Figure 5.17 Noise Model for VGA

theoretical rms output noise voltage of 300uV rms over the operating bandwidth of the VGA.

For comparison, HSPICE predicts an output rms noise voltage of 360uV for the VGA, operating at a non-inverting gain of 8. Measurements taken using a HP 3589 spectrum analyzer indicate an output rms noise voltage of 750uV rms for the VGA, also at a gain of 8. The rms noise is calculated by numerically integrating the spectrum analyzer's PSD over the measurement bandwidth. The measured VGA noise is higher than the calculated VGA noise, however these measurements likely represent the noise floor of the testboard and measuring system rather than the VGA noise by itself.

The earlier assumption that the VGA is not a major noise contributor to the integrating amplifier is valid. Although the VGA is a wide-bandwidth device, it does not possess the large low-frequency gain of the integrator, and thus is relatively insensitive to flicker noise when used in this application. Also, since the VGA provides a second-stage of amplification, its noise contribution is significantly overshadowed by the first-stage integrator noise.

Chapter 6

Conclusions

An integrating amplifier for use in the PHENIX Ring Imaging Cherenkov Detector has been designed and fabricated in the 1.2μ CMOS Orbit process. The integrating amplifier consists of an active integrator, followed by a variable gain amplifier (VGA). The purpose of the integrating amplifier(s) and associated electronics for the RICH energy channel application consists primarily of observing the array of 5120 PMTs to determine the location of Cherenkov rings. The PMT input is typically part of a Cherenkov photon ring, which may span several sets of PMTs. The highest level function of the charge measurement electronics involves observing the array of 5120 PMTs to determine the location of the Cherenkov rings, while the lowest level function of the electronics consists of determining the number of photo-electrons generated in each photomultiplier tube during a given interaction.

Each PMT has an associated integrating amplifier. The PMTs output a current pulse proportional to a photoelectron input, which is in turn integrated by the integrating amplifier(s) to form a charge energy measurement. In addition to providing a voltage output proportional to the charge input, the integrating amplifier is also used to equalize the gains of the PMTs prior to forming analog sums for adjacent PMTs. These design objectives place a number of boundaries on the integrating amplifier specifications. The primary design boundaries which establish a design envelope for the integrating amplifier include the integrating amplifier risetime and settling time, VGA risetime vs. gain, overall charge gain linearity, power dissipation, and noise performance.

Twelve integrating amplifier chips have been fabricated and tested on a prototype testboard. The system risetime specification is dictated by the PHENIX beam clock rate, which essentially cycles the particle collision rate. The integrating amplifier, analog sum circuit, and flash ADC must respond and settle in considerably less than one bunch crossing time, which is approximately 106ns. In order for the analog summing circuits that follow the integrating amplifier to complete processing within one bunch crossing, the overall integrating amplifier risetime must be 20ns or less.

Measurements indicate that the integrating amplifier risetime can be maintained within an 11ns to 21ns range, for all VGA gain ranges. In addition, the system settling time for the integrating amplifier is within the required range for the downstream electronics to function properly. The VGA risetime is maintained within an 8ns to 15ns range for any gain setting, with a non-ringing transient pulse response. The variable compensation, variable gain voltage feedback amplifier design has proven to be an effective solution to the RICH electronics requirements.

The integrating amplifier demonstrates good charge gain linearity, maintaining +-1% INL over the full input charge range. Although nonlinearities in the charge gain transfer function could be normalized out with software, a much more desirable and simpler alternative is to maintain linearity in the integrating amplifier itself.

Both the integrator and VGA op-amps demonstrate a systematic positive offset voltage. The magnitude of the offset is within the specifications required for the RICH electronics, but further offset reductions are possible through simple device scaling to negate channel-length modulation effects, as described in Chapter 4.

Power dissipation levels in the integrator and VGA op-amps are slightly high, with 6.8mW for the integrator and 14.1mW for the VGA. These power dissipation levels represent efforts to maintain high differential pair biasing for noise performance, but primarily result from high output stage current biasing for slew rate performance. The power dissipation does not adversely affect circuit performance, but does require a proper choice of packaging for thermal constraints.

The integrating amplifier measured system noise performance is on target with the required 3.5mV rms output noise after correlation, for a nominal VGA gain. The integrating amplifier has been optimized with respect to low frequency bandwidth through a proper choice of the coupling capacitor. Further gains in noise performance are likely achievable through optimization of the integrator op-amp design, and also through elimination of testboard noise sources.

Efforts to optimize the integrator op-amp should target the differential pair, and particularly the N-channel load devices M3 and M4. For the 1.2μ Orbit process, the flicker noise parameter KF is typically 15 to 20 times higher for N channel devices vs. P channel devices. In this light, the flicker noise contribution due to load devices M3 and M4 can be reduced by increasing the ratio of channel length in the loads to channel length in the input devices. HSPICE simulations reveal that tripling this ratio can lead to a factor-of-five reduction in the 1/f noise corner for the integrator op-amp.

A significant testboard noise source is the 1.25V reference used to bias the integrator's positive input. Any noise injected by this reference will be multiplied by the integrator's non-inverting power transfer function, which has considerable gain at low frequencies. Early tests revealed that the LM385 reference exhibited 1/f noise in the zero to 10KHz bandwidth, which coincides with the integrator's low frequency bandwidth. Filtering of the 1.25V reference node is highly desirable, along with the use of a low-noise reference if possible.

Based on successful results with the prototype energy channel integrating amplifier and timing channel electronics, ongoing work is proceeding with the design of an 8-channel RICH chip. The 8-channel chip will contain 8 separate energy and timing channels. Each channel will contain an integrating amplifier, a discriminator and a time-to-amplitude converter. The integrating amplifier forms the energy channel, while the discriminator and time-to-amplitude converter form the timing channel. The VGA gain control and compensation control will be implemented via a shift register, and the integrator reset time will be controlled by the shift register and an on-chip DAC. In addition, the 8-channel chip will also contain the analog summing hardware, for summing the energy channel outputs from sets of four adjacent PMTs. The 8-channel chip is expected to begin testing in late 1998.

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Appendix

HSPICE Files

```
*******************************************************************************
*amp10j for RICH integrator integ1 (revised from PbScint layout)
* SPICE file created Thu Jan 26 15:02:29 1995


C1 9 8 CAP1r2  SCALE=1220.4
C2 8 1 CAP1r2P  SCALE=1471.0
Vcapb 1  0 DC 0V
*M1 6 4 3 100 CMOSP W=288.0U L=7.2U AD=633.6P PD=410.4U AS=1296.0P
PS=784.8U
*M2 7 2 3 100 CMOSP W=288.0U L=7.2U AD=633.6P PD=410.4U AS=0.0P PS=0.0U
M1 6 4 3 100 CMOSP W=288.0U L=2.4U AD=633.6P PD=410.4U AS=1296.0P
PS=784.8U
M2 7 2 3 100 CMOSP W=288.0U L=2.4U AD=633.6P PD=410.4U AS=0.0P PS=0.0U
M3 6 6 101 101 CMOSN W=48.0U L=2.4U AD=86.4P PD=55.2U AS=576.0P
PS=415.2U
M4 7 6 101 101 CMOSN W=48.0U L=2.4U AD=86.4P PD=55.2U AS=0.0P PS=0.0U
M5 3 5 100 100 CMOSP W=144.0U L=2.4U AD=0.0P PD=0.0U AS=1206.7P
PS=852.0U
*M6 8 7 101 101 CMOSN W=120.0U L=2.4U AD=216.0P PD=134.4U AS=0.0P
PS=0.0U
*M7 8 5 100 100 CMOSP W=180.0U L=2.4U AD=324.0P PD=201.6U AS=0.0P
PS=0.0U
M6 8 7 101 101 CMOSN W=180.0U L=2.4U AD=216.0P PD=134.4U AS=0.0P
PS=0.0U
M7 8 5 100 100 CMOSP W=270.0U L=2.4U AD=324.0P PD=201.6U AS=0.0P
PS=0.0U
M10 5 5 100 100 CMOSP W=48.0U L=2.4U AD=86.4P PD=55.2U AS=0.0P PS=0.0U
M19 100 5 100 100 CMOSP W=63.6U L=8.4U AD=0.0P PD=0.0U AS=0.0P PS=0.0U
*M1 6 4 3 100 CMOSP W=288.0U L=2.4U
*M2 7 2 3 100 CMOSP W=288.0U L=2.4U
*M3 6 6 101 101 CMOSN W=48.0U L=2.4U
*M4 7 6 101 101 CMOSN W=48.0U L=2.4U
*M5 3 5 100 100 CMOSP W=144.0U L=2.4U
*M6 8 7 101 101 CMOSN W=120.0U L=2.4U
*M7 8 5 100 100 CMOSP W=180.0U L=2.4U
*M10 5 5 100 100 CMOSP W=48.0U L=2.4U
*M19 100 5 100 100 CMOSP W=63.6U L=8.4U

*R1 7 9 RPOLY1r2 SCALE=154.5
*R1 7 9 RPOLY1r2 SCALE=80
R1 7 9 rcomp
* width=1.2U
C3 101 0 73.0F
C4 2 0 103.0F
C5 3 0 71.0F
C6 4 0 104.0F
C7 5 0 101.0F
C8 6 0 34.0F
C9 7 0 71.0F
C10 8 0 62.0F
C11 100 0 72.0F
*** Node Listing for subckt:  amp10cz
** N0                   ==  IdealGND
** N1      [U=2]        ==  CAPbody!
```

```
** N2       [U=2]      ==  N2
** N3       [U=3]      ==  N3
** N4       [U=2]      ==  N4
** N5       [U=6]      ==  N5
** N6       [U=4]      ==  N6
** N7       [U=4]      ==  N7
** N8       [U=4]      ==  N8
** N9       [U=2]      ==  N9
** N10      [U=6]      ==  PWerror!
** N100     [U=12]     ==  N100
** N101     [U=4]      ==  N101


*************************************************************
*
* Model Definitions for HSPICE
*
*************************************************************
.MODEL CAP1r2 C CAP=0.500FF
.MODEL CAP1r2P C CAP=0.057FF
.MODEL RPOLY1r2 R RES=22.4

*

*Input source

Vin 2 0 dc 0 ac 1 pulse(30e-6 0.005 10n 11n 11ns 8ns 100000ns)
Vin+ 4 0 dc 0

* Loads

rload1 8 0 1000k
*cload1 8 0 12pf
cload 1 8 0 8pF


r222 5 0 19k
c222 5 0 0.01u

* supply voltages

vdda 100 0 dc 3.75
vssa 101 0 dc -1.25

.data datnm
rcomp
1k
*1.5k
2k
*2.5k
3k
.enddata

.options post
.option converge=1
```

```
*
.op
*
*.include '\meta\lib\orbit\nwell1r2\bsim1.mod'
.include '\meta\lib\orbit\nwell1r2\nw1r213.nom'
*
.dc vin -0.001 0.001 .00001
.ac dec 30 10 1e9 sweep data=datnm
*.ac dec 10 10 1e8 sweep temp poi 3 25 50 75
*.noise v(99) vin 10
*
*.tran 0.1n 100ns sweep data=datnm
*.tran 0.1n 300ns
*
.END
```

```
* amp11_v5,   Op Amp for RICH VGA
*

** Subcircuit definition for amp11_v5
** Extraction file is /msd5/frank/ic/phenix/tacsm/amp11_v5.ext

* Sources and bias    ------------------------------------
VDD   100 0 5
VSS   101 0 0
Vin+  2 0 dc 2.5
*Vin-   1 0 dc 2.5
*Vlevel 20 0 dc 5
*Vtest  8 1 dc 0 ac 1
vdiff  2 1 dc 0
vcm    1 0 dc 0

Ibias  0 5 90u

*Rf    8 1 6889
*Rf1   1 20 8611
* ----------------------------------------------------------

C1 9 8 CAP1r2 SCALE=1020.2
C1P 8 0 CAP1r2P SCALE=1415.5
* C1=510.1FF C1P=80.7FF
M1 6 1 3 101 CMOSN M=8 W=12.0U L=1.2U GEO=3
M2 7 2 3 101 CMOSN M=8 W=12.0U L=1.2U GEO=3
M3 6 6 100 100 CMOSP M=2 W=12.0U L=1.2U GEO=1
M4 7 6 100 100 CMOSP M=2 W=12.0U L=1.2U GEO=1
M5 3 5 101 101 CMOSN M=2 W=24.0U L=1.2U GEO=1
M6 8 7 100 100 CMOSP M=8 W=24.0U L=1.2U GEO=3
M7 8 10 101 101 CMOSN M=8 W=24.0U L=1.2U GEO=3
M8 5 5 101 101 CMOSN M=2 W=6.0U L=1.2U GEO=1
M9 10 6 100 100 CMOSP M=2 W=12.0U L=1.2U GEO=1
M10 10 10 101 101 CMOSN M=2 W=15.0U L=1.2U GEO=1
```

```
R1 9 7 RPOLY SCALE=97.2
* R1=2177.8 (width=1.8U)
C2 101 0 33.0F
C3 10 0 54.0F
* C4 1 0 52.0F
C5 2 0 51.0F
C6 3 0 50.0F
C7 5 0 11.0F
C8 6 0 39.0F
C9 7 0 67.0F
C10 8 0 62.0F
C11 9 0 20.0F
C12 100 0 35.0F
*** Node Listing for subckt:  amp11_v5
** N0                           ==  IdealGND
** N1                [U=2]      ==  N1
** N2                [U=2]      ==  N2
** N3                [U=3]      ==  N3
** N5                [U=3]      ==  N5
** N6                [U=5]      ==  N6
** N7                [U=4]      ==  N7
** N8                [U=4]      ==  N8
** N9                [U=2]      ==  N9
** N10               [U=4]      ==  N10
** N11               [U=1]      ==  6_1384_1214#
** N100              [U=9]      ==  N100
** N101              [U=11]     ==  N101
** WARNING #1. Less than 2 connections found at N11
* Model Definitions for HSPICE
*
.MODEL RPOLY R RES=22.4
.MODEL CAP1r2P C CAP=0.057FF
.MODEL CAP1r2 C CAP=0.500FF
.include '\meta\lib\orbit\nwell1r2\bsim1.mod'

.OP
*.dc  Vin+ 0 5 0.05
.ac  dec 30 10000 1000MEG
.plot ac vdb(8,1) vp(8,1)
.end
```

```
*RICH integrator integ1 (revised from PbScint layout)
*This file includes amp10j plus the integrating cap, reset bias trans,
and pre-integration network.
* Chris Moscone,    9-15-97

*-----------------Pre-integration network-----------------------
RT    20 0 50
Ccoup 20 21 0.01u
R1    21 22 2775
R2    22 4  600
Cint  22 2 7.2p
```

```
* ------------------Amp 10j--------------------------------------

CCOMP 9 8 CAP1r2 SCALE=1207.8
C1P   8 0 CAP1r2P SCALE=1472.8
* C1=603.9FF C1P=83.9FF
M1 6 4 3 100 CMOSP M=10 W=30.0U L=2.4U GEO=3
M2 7 2 3 100 CMOSP M=10 W=30.0U L=2.4U GEO=3
M3 6 6 0 0   CMOSN M=2 W=24.0U L=2.4U GEO=3
M4 7 6 0 0   CMOSN M=2 W=24.0U L=2.4U GEO=3
M5 3 5 100 100 CMOSP M=6 W=24.0U L=2.4U GEO=3
M6 8 7 0   0   CMOSN M=6 W=30.0U L=2.4U GEO=3
M7 8 5 100 100 CMOSP M=9 W=30.0U L=2.4U GEO=3
M8 9 0 7 100 CMOSP W=9.0U L=1.2U GEO=0
M9 9 100 7 0 CMOSN W=4.2U L=1.2U GEO=0
M10 5 5 100 100 CMOSP M=2 W=24.0U L=2.4U GEO=3
M20 100 5 100 100 CMOSP M=2 W=37.2U L=8.4U GEO=0
C3 2 0 78.0F
C4 3 0 66.0F
C5 4 0 78.0F
C6 5 0 115.0F
C7 6 0 35.0F
C8 7 0 81.0F
C9 8 0 49.0F
C10 9 0 13.0F
C11 100 0 86.0F
*--------------------------Integrating cap and reset bias transistor---
----
CF 4 24 5p
M21 24 23 4 0 CMOSN W=1.8U L=100U
*-------------------------Loads --------------------------------------
Rload 8 0 1000k
Cload 8 0 2p
* -------------------------Bias voltages and currents------------------
----
VDD 100 0 5
VGATE 23 0 4.5
VREF1 2 0 DC 1.25
IBIAS 5 0 140U
VTEST1 24 8 DC 0
Vin 20 0 dc 0 ac 1 pulse(0 -0.8 10n 2n 11ns 10ns 100000ns)


* Model Definitions for HSPICE
*
.MODEL CAP1r2 C CAP=0.500FF
.MODEL CAP1r2P C CAP=0.057FF
.MODEL RPOLY1r2 R RES=22.4

*

* -----------------------------Input source----------------------------
-------
```

```
*.data datnm
*cvalue
*0.0001u
*0.001u
*0.01u
*0.1u
*1u
*.enddata

.options post
.option converge=1
*
.op
*
.include '\avanti\models\bsim1.mod'
*.include '\meta\lib\orbit\nwell1r2\orb1r2v1.18'
*
*.dc vin -0.001 0.001 .00001
*.ac dec 30 1 1e6 sweep data=datnm
.ac dec 30 1 700e6
*.ac dec 10 10 1e8 sweep temp poi 3 25 50 75
*.noise v(8) VREF1 20
*
*.tran 0.1n 100ns
*.tran 1n 10u sweep data=datnm
.PLOT  AC VDB(8,24)  VDB(8,7)  VDB(7,3)  VP(8,24) PAR('VM(8)/VM(7)')
PAR('VM(7)/VM(3)') PAR('VM(8)/I(VIN)')
.END




■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■■
* RICH Variable Gain Amplifier,  P-channel inputs
* (Same as amp1lrch, same as op-amp design in richc)
* C. Moscone    10-1-96



** Subcircuit definition for amp11_v4
** Extraction file is /msd1/wintenbe/iclayout/emcal/amp11_v4.ext
*.SUBCKT amp11_v4 1 2 5 6 8 12 14 16 100 101
* SUBCKT not used here

* ---------------------------------------------
VDD  100 0 5
VSS  101 0 0
VREF 102 0 1.25
VTEST 200 8 DC 0
*
* Cap switch controls
* "Low" means off
* V12 is the MSB
```

```
V12 12 0 DC 5
V14 14 0 DC 0
V16 16 0 DC 0

IBIAS 5 0 50u
Vin 2 0 dc 1.25 ac 1 pulse(1.25 1.45 10n 0.1n 0.1ns 100ns 1000ns)
* -------------------------------------------------
* op-amp
M1 105 1 3 100 CMOSP M=8 W=24.0U L=1.2U GEO=3
vtest1 105 6 dc 0
M2 7 2 3 100 CMOSP M=8 W=24.0U L=1.2U GEO=3
M3 6 6 101 101 CMOSN M=2 W=12.0U L=1.2U GEO=1
M4 7 6 101 101 CMOSN M=2 W=12.0U L=1.2U GEO=1
M5 3 5 100 100 CMOSP M=2 W=24.0U L=1.2U GEO=1
M6 8 7 101 101 CMOSN M=8 W=48.0U L=1.2U GEO=3
M7 106 10 100 100 CMOSP M=8 W=48.0U L=1.2U GEO=3
vtest2 106 8 dc 0
M8 5 5 100 100 CMOSP M=2 W=6.0U L=1.2U GEO=1
M9 10 6 101 101 CMOSN M=2 W=12.0U L=1.2U GEO=1
M10 10 10 100 100 CMOSP M=2 W=15U L=1.2U GEO=1
M11 4 12 7 101 CMOSN W=4.8U L=1.2U GEO=0
* --------------------
* Inverters and compensation cap. analog switches
M12 4 13 7 100 CMOSP W=12.0U L=1.2U GEO=0
M13 9 14 7 101 CMOSN W=2.4U L=1.2U GEO=0
M14 9 15 7 100 CMOSP W=6.0U L=1.2U GEO=0
* M15, 16, 11,12,13,14 are OFF and replaced by a fixed resistor Rc
M15 11 16 7 101 CMOSN W=2.4U L=2.4U GEO=0
M16 11 17 7 100 CMOSP W=6.0U L=2.4U GEO=0
M17 13 12 101 101 CMOSN W=3.6U L=1.2U GEO=0
M18 13 12 100 100 CMOSP W=9.0U L=1.2U GEO=0
M19 15 14 101 101 CMOSN W=3.6U L=1.2U GEO=0
M20 15 14 100 100 CMOSP W=9.0U L=1.2U GEO=0
M21 17 16 101 101 CMOSN W=3.6U L=1.2U GEO=0
M22 17 16 100 100 CMOSP W=9.0U L=1.2U GEO=0
RF   1 200 8456
*R1   1 102 1208
*RPLUS 2 0 1
RLOAD 8 0 1MEG
CLOAD 8 0 12p

* -----------------------------------------
* Compensation capacitors & resistors
ccom2 10 8 0.4p

C1 11 8 0.2p
*RC1 7 11 6k

C2  9 8 0.4p
*RC2 7 9 4k

C3  4 8 0.8p
*RC3 7 4 1.5k
```

```
* Some more parasitics
*C1 11 8 cap1r2 SCALE=785.9
C1P 8 0 CAP1r2P SCALE=953.9
* C1=392.9FF C1P=54.4FF
*C2 9 8 CAP1r2 SCALE=1571.8
C2P 8 0 CAP1r2P SCALE=953.9
* C2=785.9FF C2P=54.4FF
*C3 4 8 CAP1r2 SCALE=3141.4
C3P 8 0 CAP1r2P SCALE=953.9
* C3=1570.7FF C3P=54.4FF
* ------------------------------------------
* Parasitics
C4 7 100 10.0F
C5 101 0 60.0F
C6 10 0 54.0F
C7 11 0 20.0F
C8 12 0 30.0F
C9 13 0 11.0F
C10 14 0 26.0F
C11 15 0 11.0F
C12 16 0 20.0F
C13 17 0 12.0F
C14 1 0 52.0F
C15 2 0 51.0F
C16 3 0 50.0F
C17 4 0 46.0F
C18 5 0 10.0F
C19 6 0 39.0F
C20 7 0 98.0F
C21 8 0 63.0F
C22 9 0 27.0F
C23 100 0 36.0F

************************************************************
*
* Model Definitions for HSPICE
*
.MODEL RPOLY R RES=22.4
.MODEL CAP1r2P C CAP=0.057FF
.MODEL CAP1r2 C CAP=0.500FF
************************************************************

*.data datanm rcomp C1 r1
*1.1k 1.2p 2666.67
*2.2k .8p 1142.86
*4.4k .4p 727.27
*.enddata

* measure vga gain at 100hz (more or less)
*.measure ac 'gain' max vm(2) from=100hz to=200hz
* measure frequency where gain drops -3db of low frequency gain
*.measure ac 'f_3db' trig at=100
*+                   targ vm(2) val='(0.707*gain)' fall=1
```

```
.include '\avanti\models\bsim1.mod'
*.include '\meta\lib\orbit\nwell1r2\nw1r2l3.nom'
*.include '\meta\lib\orbit\nwell1r2\orb1r2v1.18'

.OP
*.TRAN .5N 100N 0 .5N sweep data=datanm
*.tran 1n 100n 0 1n
*.ac  dec 30 10000 1000MEG sweep data=datanm
.ac dec 30 100 500MEG
.noise v(8) Vin 20
*.plot ac vdb(8,200) vp(8,200)

.END
```

Vita

Chris Moscone was born in Boston, Massachusetts on June 8, 1965. He moved to Knoxville in 1969 and attended South-Young high school. After graduating from high school in 1983 he entered the University of Tennessee to pursue a degree in Mechanical Engineering. In June, 1988 he graduated Magma Cum Laude with a Bachelor of Science degree in Mechanical Engineering, and was accepted into graduate school in Mechanical Engineering at the University of Tennessee. In 1990, Chris accepted a job with the Aluminum Company of America's Tennessee Operations, where he worked as a Mechanical Project Engineer specializing in mechanical design and heat-transfer applications. Chris completed his Master of Science in Mechanical Engineering in 1991 while working for ALCOA. Chris left ALCOA in 1993, and re-enrolled at the University of Tennessee in Spring 1994 to pursue a Bachelor Degree in Electrical Engineering, graduating Magna Cum Laude in Spring 1996 with an analog electronics focus. With the encouragement of his professors, Chris enrolled in graduate school at the University of Tennessee and entered the joint UT-ORNL program in Mixed-Signal VLSI design, working primarily in the area of analog integrated circuit design. In addition to analog circuit design, Chris enjoys electronics as a hobby and is also interested in most forms of athletics including weightlifting and mountain-biking. Chris also enjoys modifying and assembling custom engines for automotive racing.