Online Switching Time Monitoring of SiC Devices Using Intelligent Gate Driver for Converter Performance Improvement

A Thesis Presented for the

Master of Science

Degree

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This Master's Thesis is dedicated to all of my loving family: Abigail, Mom, Dad, Davis, Nathan, Chelsea, Johnny, Paula, Adam, Anna Beth, Logan. Your love and support mean more to me than words could ever say. Abigail, I will love you forever and always.

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Abstract

Most intelligent gate drivers designed for new state of the art WBG devices typically only focus on protection and driving capabilities of the devices. This paper introduces an intelligent gate driver that incorporates online switching time monitoring of silicon carbide (SiC) devices. For this specific case study, three timing conditions (turn-off delay time, turn-off time, and voltage commutation time) of a SiC phase-leg are online monitored. This online monitoring system is achieved through transient detection circuits and a micro-controller. These timing conditions are then utilized to develop converter-level benefits for a voltage-source inverter application using SiC devices. Junction temperature monitoring is realized through turn-off delay time monitoring. Dead-time optimization is achieved with turn-off time monitoring. Dead-time compensation is obtained with turn-off time and voltage commutation time monitoring. The case study converter assembled for testing purposes is a half-bridge inverter using two SiC devices in a phase-leg configuration. All timing conditions are correctly monitored within reasonable difference of the actual condition time. The half-bridge inverter can operate at 600 V DC input and successfully obtain a junction temperature measurement through monitored turn-off delay time and the calibration curve. In addition, dead-time control is realized to reduce device power loss and improve AC output power quality. Furthermore, the proposed online time monitoring system is board-level integrated with the gate driver and suitable for the chip level integration, enabling this practical approach to be cost-effective for end users.

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Chapter 1

Introduction

1.1 Introduction and Background

1.1.1 Silicon Carbide in Voltage Source Inverters

The emerging technology of the silicon carbide (SiC) semiconductor is continuing to be a major research topic in the power electronics community. In recent years, there has been a shift of silicon carbide (SiC) power semiconductors replacing traditional silicon (Si) power semiconductors in voltage-source converters (VSC) [1]. Because there is a vast number of topologies classified as a VSC, the VSC of interest for this work is the 2-level voltage-source inverter (VSI). The classic topology for a three-phase two-level voltage-source inverter, using MOSFETs, can be seen in Figure 1.1. The VSI is a popular converter used in electric vehicle, uninterruptable power supply, and solar inverter applications [2, 3, 4]. In addition, the traction drive 3-phase PWM inverter is a major system under research because of the growth in the EV market [5]. Today's traction inverters can't penetrate the mass consumer automotive market as they typically have too high of cost and weight [4]. However, this application is seeing the shift from traditional Si IGBT to SiC MOSFET because the switching frequency can be higher in SiC, which allows SiC to have less power loss and the system can have smaller passives [4, 5, 6, 7].

Furthermore, SiC is being used more as an inverter's switching device in certain applications because it offers increased blocking voltages, lower on-resistance, increased

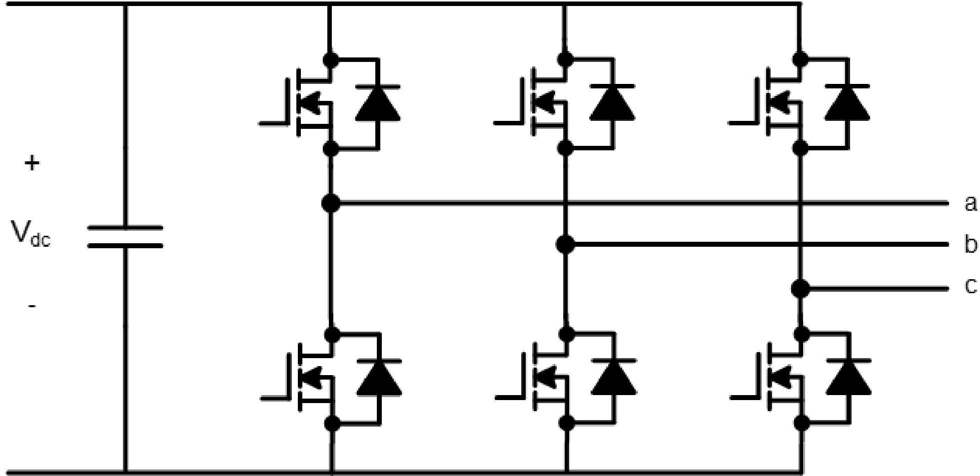


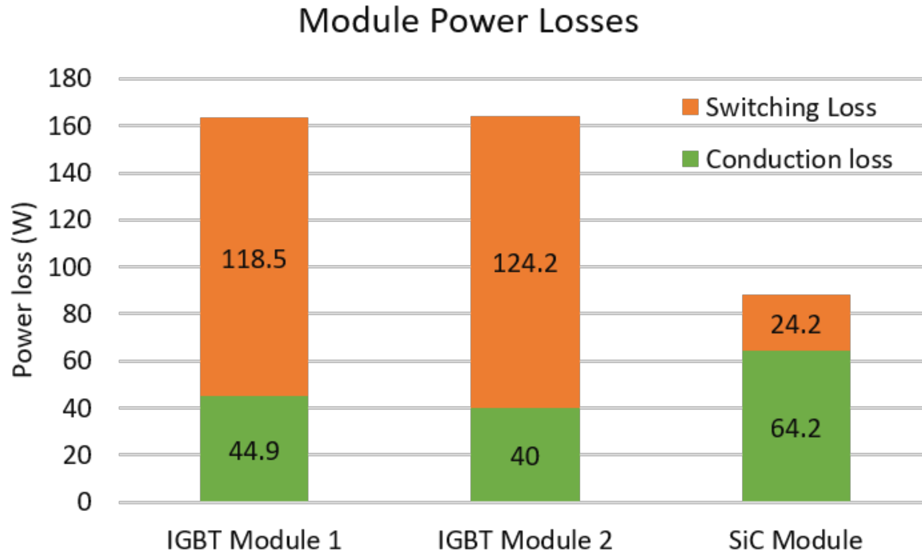
Figure 1.1: 3-phase 2-level voltage-source inverter

junction operating temperature, and faster switching capabilities [4, 8, 9, 10, 11]. An example of this is in analysis that looked at a general 3-phase voltage-source inverter that operated at 30 kW, 690 V_{DC}, 60 Hz fundamental, 15 kHz switching, and air cooled [8]. In their simulations, 150 A and 200 A 6th Generation Trench Field Stop Si IGBT half-bridge modules are compared against the 100 A SiC MOSFET half-bridge module. The results in Figure 1.2 show the benefit in power loss and operating temperature reduction from using SiC.

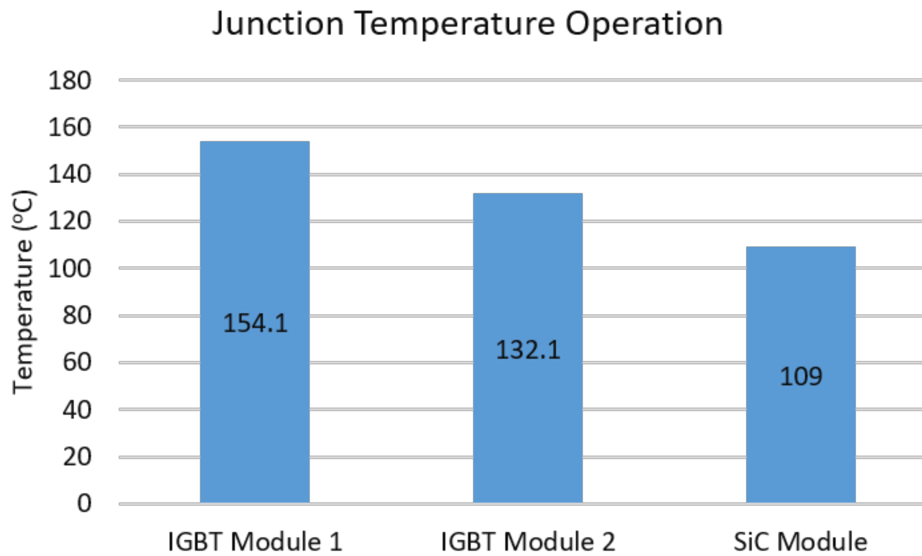
1.1.2 Intelligent Power Module Application

One area of increased research in regards to SiC is the design and development of intelligent power modules (IPM). An IPM is a group of advanced semiconductor dies (Si IGBT or SiC MOSFET) typically connected in a way to make a single *phase-leg* in a packaged module with potential for added intelligent features. A basic SiC power module from Wolfspeed can be seen in Figure 1.3. Power electronic applications using IPMs include: industrial motor drives, power supplies, electric vehicles, and renewable energy converters. One area of research in IPMs is the advanced packaging and cooling of the module [12]. This subject, however, is out of the scope of this thesis.

The other area of research for IPMs, which is in scope for this thesis as an application, is advanced driving, sensing, and control for the power module. An example of this type of IPM can be seen in the AgileSwitch commercial product (EDEM3) shown in Figure 1.4. The



(a) Power Module Losses in a VSI



(b) Power Module Temperature in a VSI

Figure 1.2: Simulation results for a 30 kW VSI at 15 kHz switching frequency with 150A and 200A Si IGBT modules and 100A SiC MOSFET module [8]

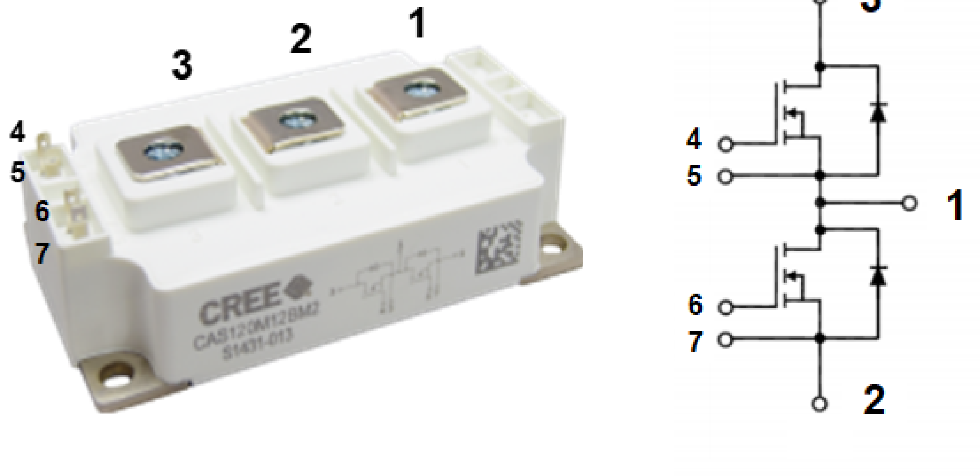


Figure 1.3: Wolfspeed SiC power module with associated phase-leg connection

EDEM3 product itself is an intelligent gate driver, which will be discussed in more detail in section 1.2.2, and it is connected to a compatible power module to form the IPM. The EDEM3 is designed to have advanced gate driving (i.e. augmented turn-off), high voltage isolation, and temperature monitoring. This is becoming more popular in industry: either module designers creating the advanced gate driver themselves to sell with the power module (e.g. Wolfspeed) or separate companies that design intelligent boards to accompany certain power modules (e.g. AgileSwitch). This is also being seen more for SiC power modules because it helps users take full advantage of SiC capabilities in converters, while mitigating any adverse effects. This will be further discussed in the scope of gate driver possibilities in section 1.2.2.

1.2 Motivation

With the great potential shown for SiC in power electronic applications, there are still challenges associated with using SiC in a converter. The motivation for this thesis work looks at two challenges (high temperature and high switching frequency operation) associated with

Figure 1.4: AgileSwitch intelligent gate driver on top of SiC power module [13]

using SiC, where pushing the bounds of operation to achieve the benefits of SiC has its trade-offs that must be accounted for. Also, the potential for new technologies in the gate driver component of a power electronics system is shown to be a motivating factor for this work.

1.2.1 SiC Challenges

Reliability and High Temperature Operation

Power electronic applications are continuing to demand converters with operation in higher temperature and power as well as higher power density. This is why wide bandgap (WBG) semiconductors have grown in popularity over the past several years as they possess increased blocking voltage, higher thermal conductivity, lower on-resistance, and faster switching capabilities when compared to silicon (Si) semiconductors [1, 14].

On the other hand, power electronic applications are also demanding highly reliable converters. For example, converters placed under the hood in electric vehicles are thermally stressed by ambient temperatures that can reach 150 °C, while still needing low failure rate and long lifetimes [15]. Also, safety requirements are very strict for converters in aerospace,

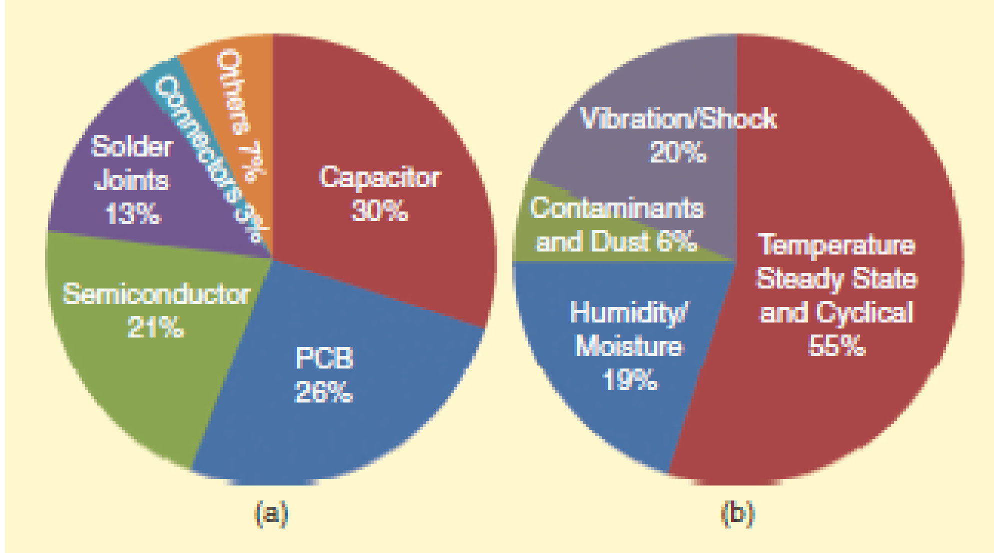


Figure 1.5: Surveys on failures in power electronic systems (a) Failure distribution among major components (b) Source of stress distribution for failures [17]

medical, and automotive applications. This creates an issue with the semiconductor switching devices, especially WBG devices, employed in the power electronic converters as they often rank as the most fragile components in power electronic systems [16]. In fact, Wang *et al.* [17] showed through their analysis, seen in Figure 1.5(a), that the semiconductor (IGBT in this case) accounts for one-fifth of the failures in a power electronic converter. Also note the high percentage of failure from high temperature operation and temperature cycling effect shown in Figure 1.5(b). This is why junction temperature has become the key indicator of the health condition of any power semiconductor device [18].

When looking specifically at SiC reliability variation from the temperature effect, there are a few characteristics that limit high reliability. The first one is gate oxide degradation causing threshold voltage shifting [19, 20]. The second degradation is bond wire lift-off that causes R_{ds-on} shifting [21, 22]. The third reliability issue is reduced short circuit withstand time from smaller SiC die size to absorb short circuit energy [23, 24]. The details of these SiC reliability issues are out of this works scope; however, it is important to mention them because of the importance that high junction temperature operation plays in reducing the reliability (i.e. increasing the chances of observing these issues). The conclusion can be drawn that to safely operate semiconductors in converters with high reliability, the temperature information of the device needs to be known and controlled.

High Frequency Operation with SiC

Because of noise, parasitics, and real converter setups, the observed switching performance of SiC devices in actual power converters is almost always worse than the ideal switching performance in manufacturer datasheets [2]. In fact, in an example SiC-based voltage source inverter, due to the increased overshoot current and slower turn-off time, the total switching energies were increased by a factor of 1.5 to 1.8 [25].

One example of a trade-off by using SiC is the device body diode characteristics and its effect on reverse conduction loss, especially at higher switching frequency. SiC devices have higher body diode forward voltage compared to other anti-parallel diodes connected to the switching devices, which produces more reverse conduction energy losses according to equation 1.1,

$$P_{dt} = 2V_f I_d t_{dt} f_s \tag{1.1}$$

where V_f is the forward voltage, I_d is the drain current, f_s is the switching frequency and t_{dt} is the dead-time. The SiC intrinsic V_f value cannot be changed and SiC applications require higher power ratings and switching rating (i.e. higher I_d and f_s); therefore, the dead-time parameter set in the control stage needs to be actively adjusted for ideal performance.

Also, a trade-off from higher switching frequency is PWM voltage distortion because of non-ideal switching commutation in the converter, which is also distorted from longer dead-time settings. This non-ideal switching commutation time is highly sensitive to operating conditions and converter load characteristics [26]. Figure 1.6 shows the difference in an inverter PWM output voltage switching at the turn-off transition for a motor load and inductor load [27]. The motor load introduces more parasitics that affect the switching performance of the semiconductor device shown with a longer turn-off time compared to the inductor load case.

Figure 1.7 demonstrates the non-linear variance effect of parasitic capacitance on the switching time with respect to load current. Ideally, the output mid-point voltage is just an amplified PWM input signal but dead-time and this non-ideal switching time cause distortion from that ideal case. After obtaining the Figure 1.7 switching data, the resulting output

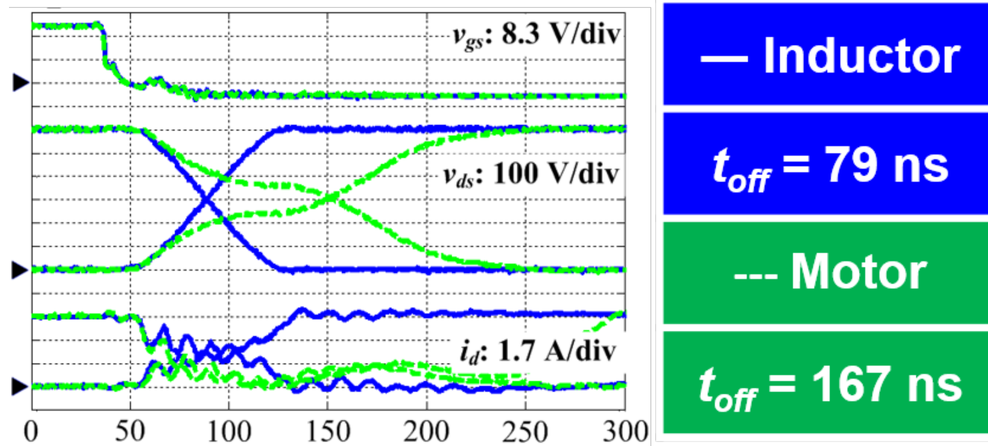


Figure 1.6: Effect load conditions have on output voltage distortion from different associated parasitic capacitance

voltage distortion was further examined for cases around the current zero-crossing in Figure 1.8. The snapshot is taken around the zero-current crossing to show the different variations on the midpoint PWM voltage distortion based on the current magnitude and polarity.

This output voltage distortion reduces the power quality at the output of the inverter, which some applications need low harmonics at the output [28]. Therefore these side-effects from higher switching frequency operation must be designed for to fully achieve the benefits of using SiC in high switching frequency applications.

1.2.2 Gate Driver Possibilities

Another motivation for this work is the untapped potential of a power electronic gate driver. There is new research work conducted in the area of power electronic gate drivers for SiC focusing on advanced gate driving due to the faster switching of SiC, the high voltage isolation issue with SiC-specific high voltage operation, and fast protection schemes needed [29, 30, 31, 32, 33]. These features help engineers take full advantage of SiC capabilities in converters, while mitigating any adverse effects.

One example of this is the intelligent gate driver designed for SiC devices by the FREEDM ERC group [33]. Their work looks at the two challenges associated with using SiC devices in medium voltage applications. One challenge is sufficient isolation between the power signals and control signals due to the high dv/dt and di/dt at the switching instants. The other

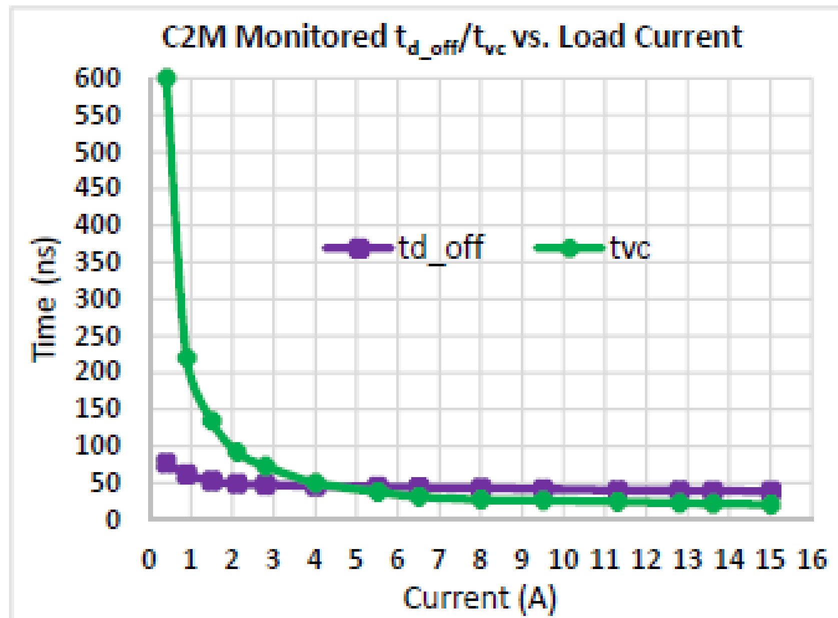


Figure 1.7: Monitored switching time test results with respect to load current

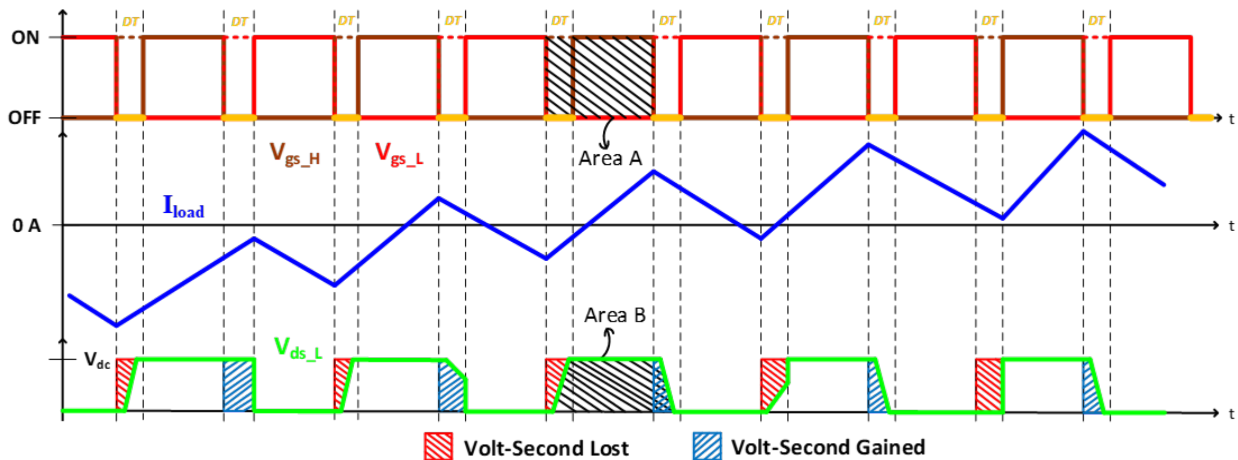


Figure 1.8: Inverter operation around the current zero-crossing with associated volt-second lost/gained each switching cycle

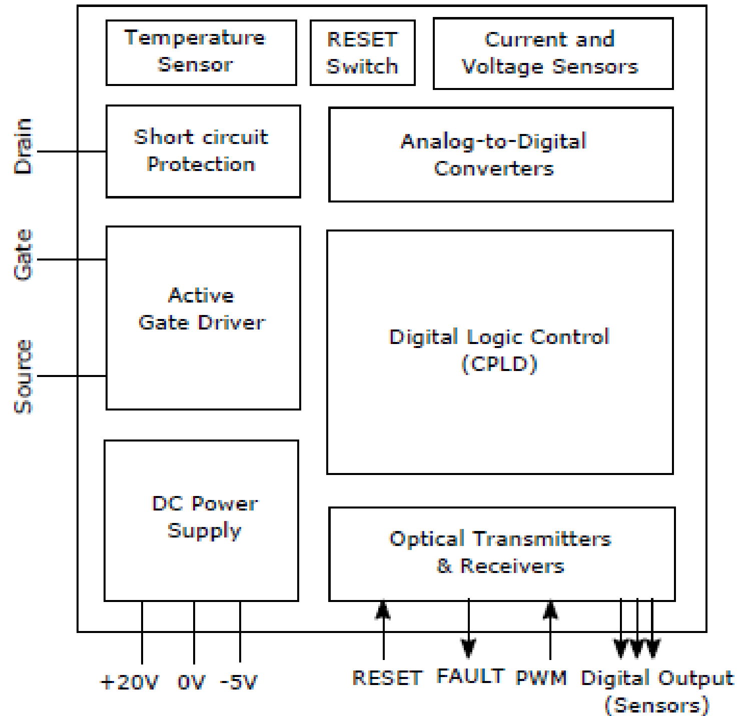


Figure 1.9: Block diagram of intelligent gate driver for medium voltage SiC application [33]

challenge is the need for faster protection because of the reduced short-circuit withstand time for the smaller die size of SiC as well as higher current and associated di/dt during a short-circuit fault condition. The components of the designed intelligent gate driver are shown in Figure 1.9. This work has great impact in the field of advanced gate drivers for SiC.

However, there is a lack of work looking at utilizing the gate driver as an advanced data sensor for the SiC devices. There is sensing in existing advanced gate driver but those approaches use the sensing for protection applications. Examples include: current sensing for overcurrent and short circuit protection, overtemperature protection using the thermistor in power modules, and undervoltage lock-out (UVLO) protection. Data sensing can be used for other applications outside of protection, and because the gate driver is the bridge between the power stage and control stage, incorporating data acquisition schemes in a gate driver can be advantageous.

1.3 Thesis Organization

This thesis is laid out in a logical manner with the goal to provide a brief overview of the topics with each succeeding chapter providing more explicit and detailed support for the main argument. The main argument is given directly below in a manner to be extremely concise and direct:

> **Main Argument:**
> The purpose of this thesis is showing the benefit of data sensing through the gate driver for SiC devices and showing an online, integrated switching time sensing design and development for converter-level benefits.

Chapter 2, the literature review, focuses on the studies that look at the two converter-level applications. The first is the method to sense devices' junction temperature through electrical parameters, which is introduced and surveyed. Then, literature discussing adaptive dead-time converter systems is presented and analyzed. Finally, the literature review is concluded with statements on issues still present on these topics and looks towards the design of this presented thesis.

Chapter 3 walks through the design of the switching time monitoring system. The dynamic switching performance of SiC is shown. Also, details of the monitoring system are discussed and designed to have accurate and online time sensing.

Chapter 4 shows the experimental results for the sensing scheme and resulting converter-level applications.

Chapter 5 evaluates the results from Chapter 4. The argument of the thesis is formed from the evidence so that a conclusion can be made. Once the argument is fully supported, further work is proposed for both future enhancements to the system and further applications to pursue.

Chapter 2

Literature Review

In this literature review, this thesis reviews the two applications applied in this work: junction temperature monitoring and dead-time control.

2.1 TSEP-based Temperature Sensing

In this section, the junction temperature sensing approach using TSEPs is reviewed. First, the background behind the approach is presented. Then the criteria that is used to access a given TSEP-based T_j sensing approach is summarized. Finally, the different implementations used in literature are analyzed and summarized.

2.1.1 Background of TSEP-Based Temperature Sensing

SiC performs well in high temperature applications because of an increase in thermal conductivity (λ) from 1.5 W/cm-K to 5.0 W/cm-K when compared to Si semiconductor devices [34]. Because SiC is *famous* for its high temperature operation, research focusing on the junction temperature (T_j) of SiC is an important topic. This temperature is important because it will determine the behaviors of the device in operation (e.g. output characteristics, transfer characteristics, etc.). The T_j of SiC is defined as the highest operating temperature of the surface of the internal SiC die [35]. The internal SiC die of a power semiconductor packaged device is shown in Figure 2.1. Having a packaged device is essential for easier

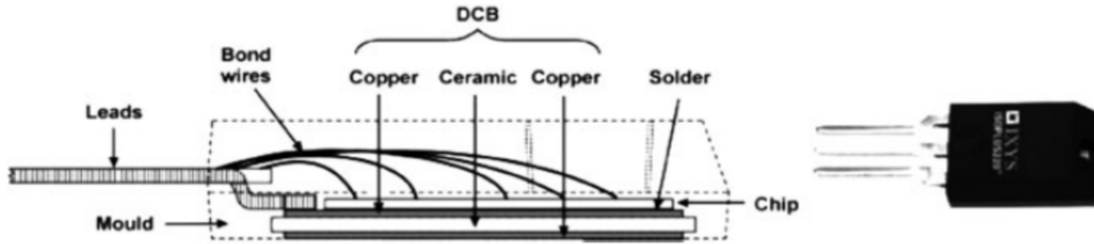


Figure 2.1: Diagram of sub-components of a classic TO package for a power MOSFET [36]

electrical connections to converter, mechanical support for the die, and thermal conduction to a heatsink. However, this package makes sensing the internal SiC die junction temperature difficult.

Traditional Forms of Temperature Sensing

A traditional approach to temperature sensing is using a physical contacting temperature sensor. Common sensors include thermocouples, fiber optic sensors, and thermistors [19, 37, 38, 39, 40, 41, 42]. As an example, Ibrahim *et al.* [19] uses fiber optic sensors attached to the exposed SiC dies to measure junction temperature in an application to run power cycling tests (PCTs) at high temperatures for SiC gate oxide trapping analysis. The fiber optic sensors give accurate junction temperature readings along with electrical isolation. However, to achieve the physical sensor based temperature sensing in this application, they had to expose the SiC dies shown in Figure 2.2, which is unrealistic in most applications where users just want to keep the SiC package intact.

Thermistors are another traditional physical contacting temperature sensor that can be leveraged to indicate junction temperature. In semiconductor temperature sensing applications, the small thermistor is inserted close to the die in a power module package. Most major SiC power module manufacturers are incorporating a NTC thermistor in the module to monitor temperature. In an application note from their silicon power module design, Infineon shows the placement of a NTC thermistor to indicate junction temperature, which is shown in Figure 2.3 [40]. This is an easy way to obtain a temperature reading that can be correlated to the junction temperature; however, the temperature reading is only a local measurement (similarly to other physical-contacting temperature sensors). Also,

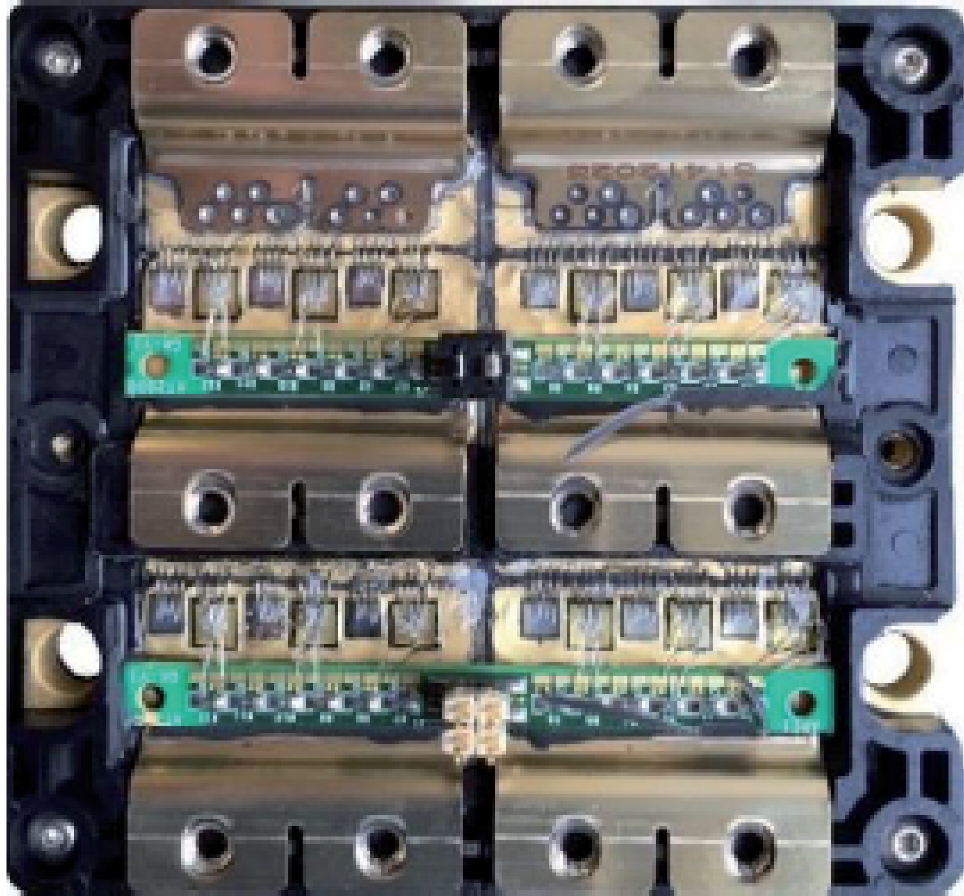


Figure 2.2: APEI SiC power module exposed [19]

isolation must be included in the external NTC interface circuit, and this approach is only available in applications using the power modules that include a NTC thermistor.

Another type of temperature sensing technique is with infrared radiation (IR) [38, 39, 43]. This concept is enabled by the temperature (T) dependence of spectral radiance (B_v) shown in Plancks law of radiation.

$$B_v = \frac{2hc^2}{\lambda^5} \times \frac{1}{\exp(\frac{hc}{\lambda kT}) - 1} \tag{2.1}$$

Spectral radiance is dependent upon temperature and wavelength so integrating equation 2.1 over all wavelengths yields the Stefan-Boltzmann equation for total emitted energy.

$$P = A \cdot \epsilon \cdot \sigma \cdot T^4 \tag{2.2}$$

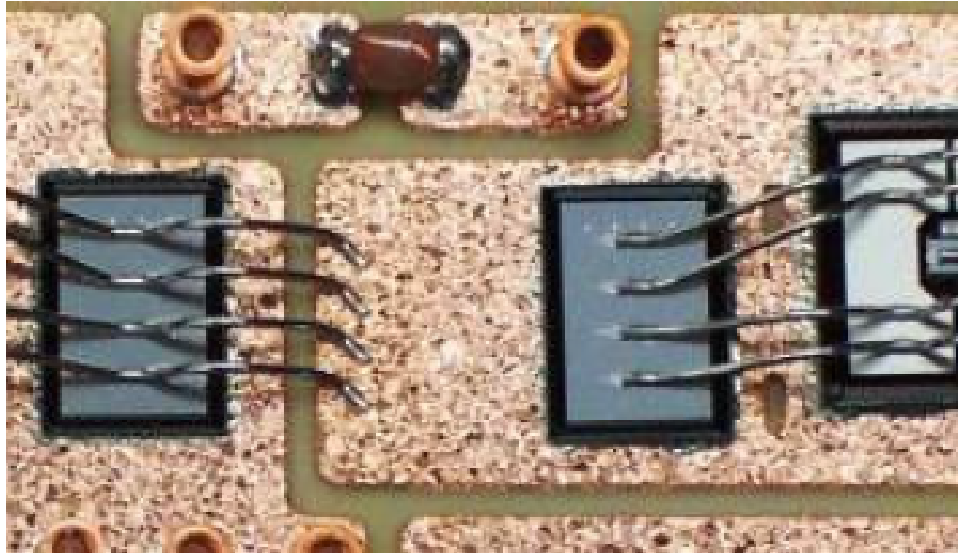


Figure 2.3: NTC thermistor (in red) mounted close to Si dies (in blue) in a power module [40]

Therefore, the IR camera can sense the objects radiation for a given area (A) and indicate the temperature. The key parameter in IR temperature sensing applications is the emissivity (ϵ). The values for ϵ of the materials on a chip can range from 0.1 (aluminum) to 0.6 (polysilicon) [38]. This can cause error in the temperature reading or create the need to black coat the semiconductor power module as shown in Figure 2.4 from the example in [39].

While physically-contacting temperature sensors and IR-based sensors are potentially the most accurate and/or simplest ways of monitoring temperature, the invasive nature of direct die measurement methods make them only suitable in laboratory testing conditions and therefore inapt for general applications [44]. There are other physical-contacting schemes (i.e. liquid crystals, thermographic phosphors) and optic based approaches (i.e. Raman effect, luminescence), but the goal of introducing these approaches is to show the need for a temperature sensing approach that does not need to have the SiC device package altered. Therefore, a full review of non-TSEP temperature sensing schemes is out of this works scope.

Another way to obtain temperature information is through thermal modeling. This is a traditional step taken in a power electronic system design because of the importance of thermal performance and it assists in the selection of the needed heatsink for the converter. The typical thermal model used for power semiconductor devices is shown in Figure 2.5

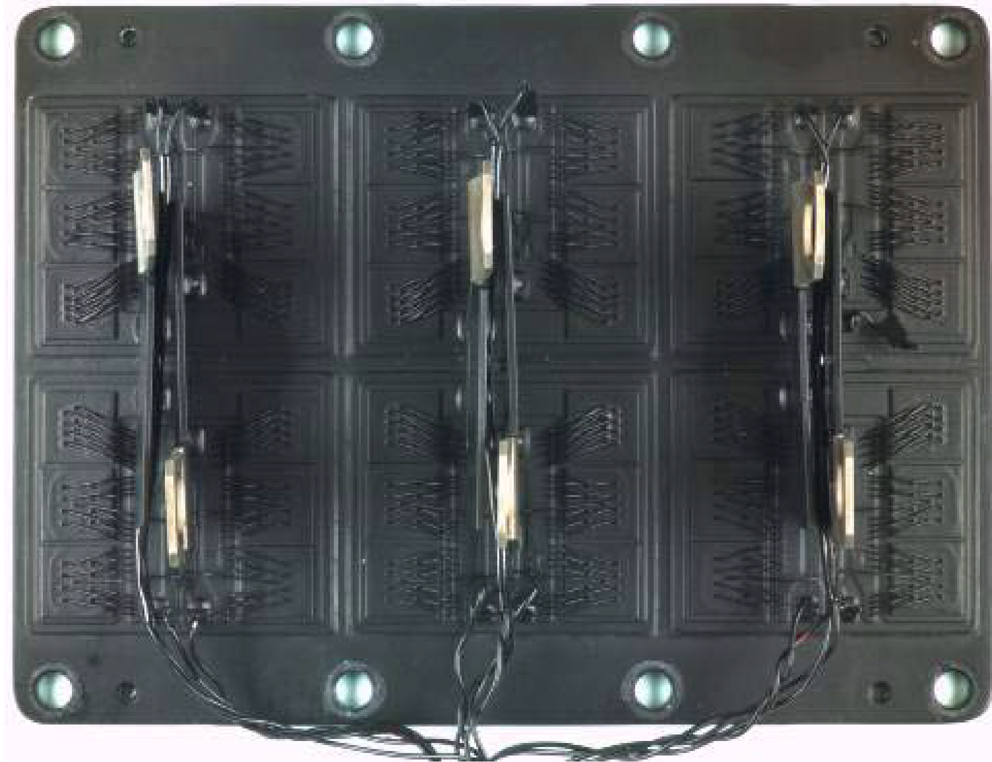


Figure 2.4: Black coated IGBT 6.5 kV module for IR camera temperature sensing [39]

[45]. The T_j estimation is a straightforward process where power loss calculations using simulations and datasheet values for device/heatsink thermal resistances are multiplied to obtain the estimated junction temperature. Even some semiconductor suppliers provide software tools for thermal modeling [46]. However, just like with any type of modeling, questions can be raised regarding the accuracy of the values used and the assumptions made that limit the thermal design. Bruckner *et al.* [47] showed in their analysis the error between an IR monitored temperature reading and a modeled temperature calculation. The modeled value was over-estimated based on worst-case datasheet values. Using the thermal model case led to an over-design in the heatsink of the system, which adds volume, weight, and cost to the system. Another aspect thermal models usually do not consider is the degradation of thermal impedances over the lifetime of a semiconductor [48, 49]. Therefore, there is value in obtaining a real-time operation junction temperature recording to add to the integrity of the thermal model.

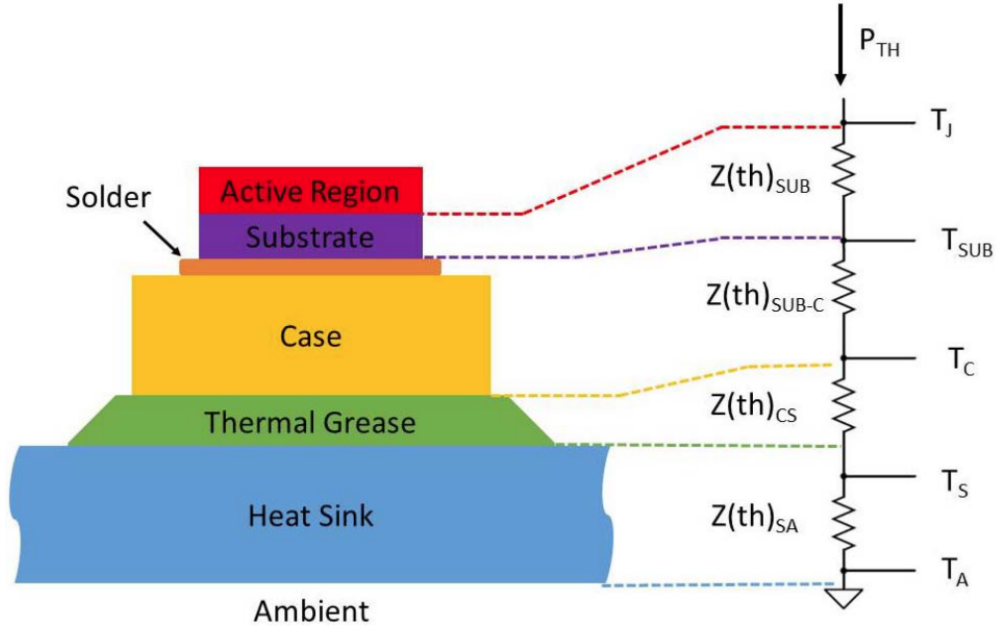


Figure 2.5: Thermal model of a power MOSFET [45]

TSEP-based Temperature Sensing Methodology

Another type of semiconductor temperature sensing, that is growing in research work, is leveraging a thermo-sensitive electrical parameter (TSEP) to indicate the device junction temperature, which is one of the main topics of discussion in this thesis and will be presented in the coming chapters.

The process to obtain the relationship between the electrical parameter of the semiconductor and the junction temperature is accomplished with a calibration curve. To obtain the data for the calibration curve, the temperature of the device is fixed by an external system (e.g. hot plate, oven, dielectric bath) [50]. Then, voltage and/or current is injected into the device to simulate real converter operation, and they are used as the variations of calibration curves. This step is important as all TSEPs are not solely dependent on temperature; therefore, other parameter variations must be accounted for. Finally, the selected TSEP is captured/monitored under an externally set temperature and the corresponding point on the calibration curve is obtained. Also note that this electrical operation must be fast (e.g. double-pulse test, curve tracing) to prevent device self-heating, which would cause error in the junction temperature value.

Considerations for TSEP-based T_j Sensing

The first consideration is the time resolution of the monitored data (i.e. the ability to track temperature swings). TSEP based approaches are only limited by the MCU processing speed of the received monitored data (i.e. time resolution on the order of tens to hundreds of microseconds); whereas, physical sensors and IR-based sensing have time resolution in the milli-second range [39].

The second consideration is the temperature distribution of the device under test and the corresponding location of temperature measurement. A combination of rare access to the device die and potential placing of physical temperature probe not on peak temperature spot cause it to be limited in comparison to the TSEP approach that uses the entire device die as the sensor [15].

The third consideration is the effect the temperature sensing has on the converter operation, and this is the one where the TSEP approach can potentially cause issues. However, this is why research is needed in the online monitoring schemes of TSEPs so that the converter operation is not negatively affected, and the TSEP temperature sensing approach can become more competitive as a semiconductor junction temperature monitoring approach.

2.1.2 TSEP Comparison Criteria

There needs to be a way to determine the effectiveness of a certain TSEP temperature sensing approach. This is done by evaluating the TSEP approach against five criteria, where the goal is to achieve good marks for all criteria or design a way to compensate for bad marks against a certain criteria.

One of the most important criteria a TSEP candidate must meet is the sensitivity it possesses with respect to junction temperature. Simplified, this is the slope parameter of the calibration curve; therefore, this value needs to be high enough to give a clear indication of a junction temperature value for a given TSEP value. Avenas *et al.* [50] proposed a ratio equation 2.3, which attempts to compare the sensitivity of various TSEPs.

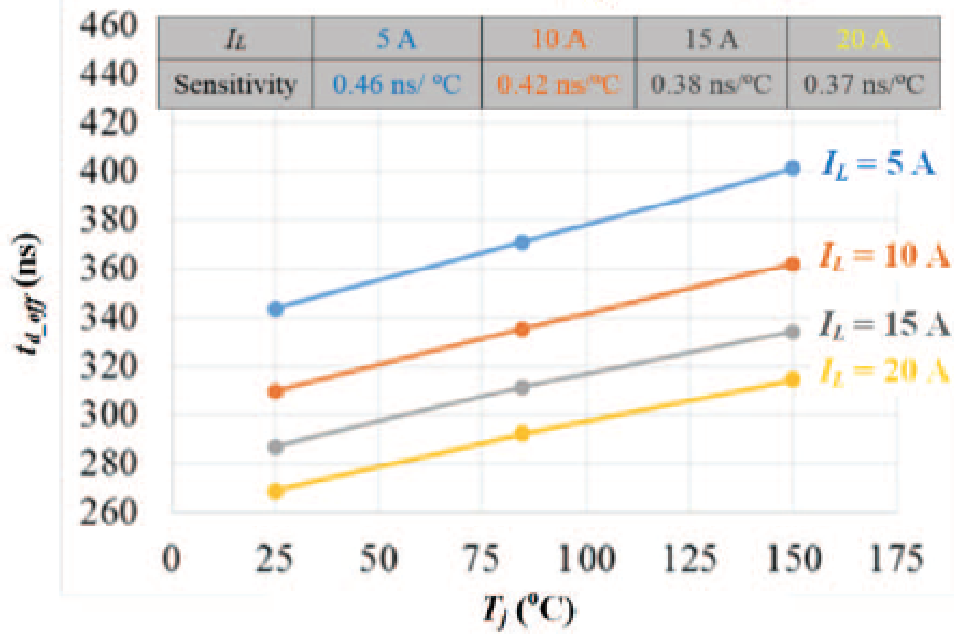


Figure 2.6: Good TSEP calibration curve of $t_{d,off}$ in terms of linearity and sensitivity [51]

$$S = \frac{\mid s \mid}{\mid val_{max} \mid} \tag{2.3}$$

where s is the sensitivity of the TSEP per °C and val_{max} is the maximum calibrated value of the TSEP. Though this is a good initial quantified comparison metric, the acceptable sensitivity is mainly dependent upon the degree of accuracy of the monitoring technique.

For example, Figure 2.6 shows a calibration curve for turn-off delay time as a TSEP implemented by Zhang *et al.* [51]. This research focusing on the sensitivity is the precursor to the junction temperature monitoring part of this thesis. All the curves have a sensitivity around 0.4 ns/°C, which at first glance could be interpreted as a bad sensitivity for how short of a time period that is 0.4 ns. However, their work designed a monitoring system with the accuracy of obtaining $t_{d,off}$ with a resolution of 0.1 ns. Therefore, this approach can easily correlate a sensed $t_{d,off}$ value with a single junction temperature value of 1 °C resolution.

Another criteria that would benefit a TSEP applicant is whether it is linearly dependent with temperature. This presents two major benefits in the monitoring temperature system. First, it simplifies the control-side processing to translate the input of the sensed electrical parameter into the output of junction temperature. Second, it simplifies the process of

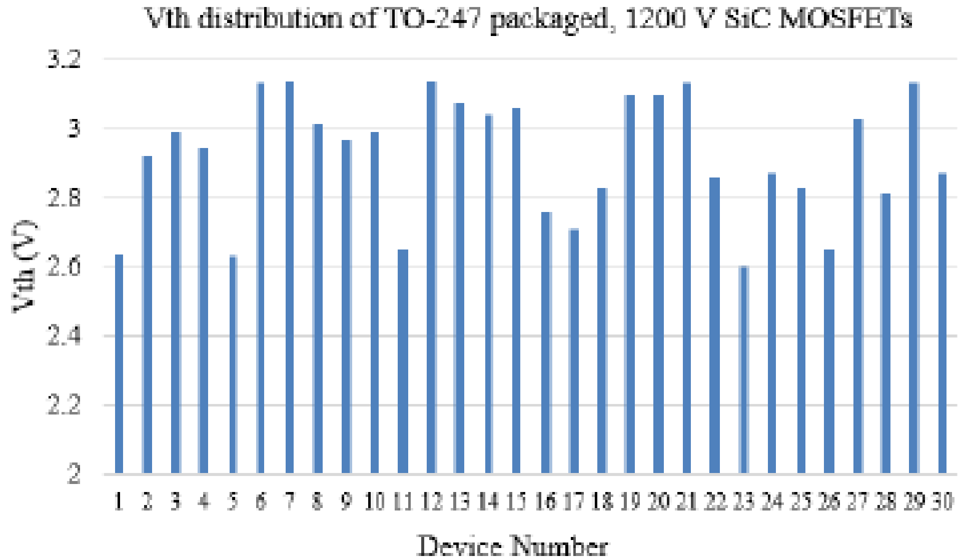


Figure 2.7: Gate threshold voltage distribution of 30 SiC discrete devices from the same supplier [53]

acquiring the calibration curve, which also means less calibration points are needed. This can again be seen in Figure 2.6, where Zhang *et al.* only had to obtain three points on the calibration curve for satisfactory results.

Another criteria that contributes to ease of use is the transferability of the calibration curve between devices. This is generally poor for any SiC TSEP scheme because of relatively immature manufacturing processes. The variation is easily expected for different SiC suppliers as shown in [52]. Also, there is variation in characteristics among SiC devices of the same supplier. An example of this is shown in the V_{th} fluctuation in Figure 2.7 detailed in [53]. Relating back to TSEP-based junction temperature monitoring, this lack of transferability means two things. One, calibration must be done for every SiC device installed in a converter. Two, issues could arise in SiC power module cases where multiple SiC dies are used with slight variations in TSEPs.

A more obvious criteria that must be met as a competitive TSEP is the accuracy of the processed temperature data. This has to be obtained in a couple of ways. First, the TSEP needs to be accurately monitored. This means that parasitics, switching speed, etc. cannot affect the accuracy of the captured electrical data. Second, the TSEP needs to avoid degradation, which introduces inaccuracy in the calibration curve.

In terms of true accuracy of acquiring the junction temperature, it is difficult to confirm the accuracy as works usually do not compare the temperature obtained from the TSEP with a more direct measurement method [50]. *One* way to verify the accuracy is verify the accuracy of the sensing and use the tolerance to compare against the sensitivity from calibration, which will then give an accuracy tolerance for the temperature sensing.

This is an area of future research to implement a system where two different temperature sensing approaches that can be easily implemented together are able to obtain a more precise and real-time temperature parameter. This also will account for any degradation that the electrical parameter might see.

Last but certainty not least is the criteria of the TSEP to be online sensed during converter operation. This is the criteria where the addition of the TSEP sensing circuitry should not negatively affect the converter operation. Newer TSEP approaches are more conscientious about using an approach that does not cause converter performance issues. An example of the lack of online sensing capability is found in Figure 2.8 from [48] that was using V_{th} as a TSEP. The V_{th} monitoring circuitry has to disconnect the DUT at C_1 to better sense the threshold voltage. Most general power converter engineers would not want to employ a temperature sensing option that requires them to have to disconnect a device from a potential safety critical application.

2.1.3 TSEP Sensing Approaches

As mentioned previously, TSEP based junction temperature monitoring is growing as a viable temperature sensing candidate. This is because there is a need for internal junction temperature sensing without exposing the die from its package. This section will outline the existing literature on research work that incorporated a TSEP sensing scheme in their power semiconductor operation. A note needs to be made that some work outlined will be for Si IGBTs. This is because of two things: both SiC devices and TSEP based sensing are new technologies that have not had much time to be research/implemented together. For the approaches on IGBTs, any special notes in relation to SiC devices will be made.

These TSEP schemes are the ones that have been around longer and well-characterized. The main drawback, however, is that they typically have to be performed in specific electrical

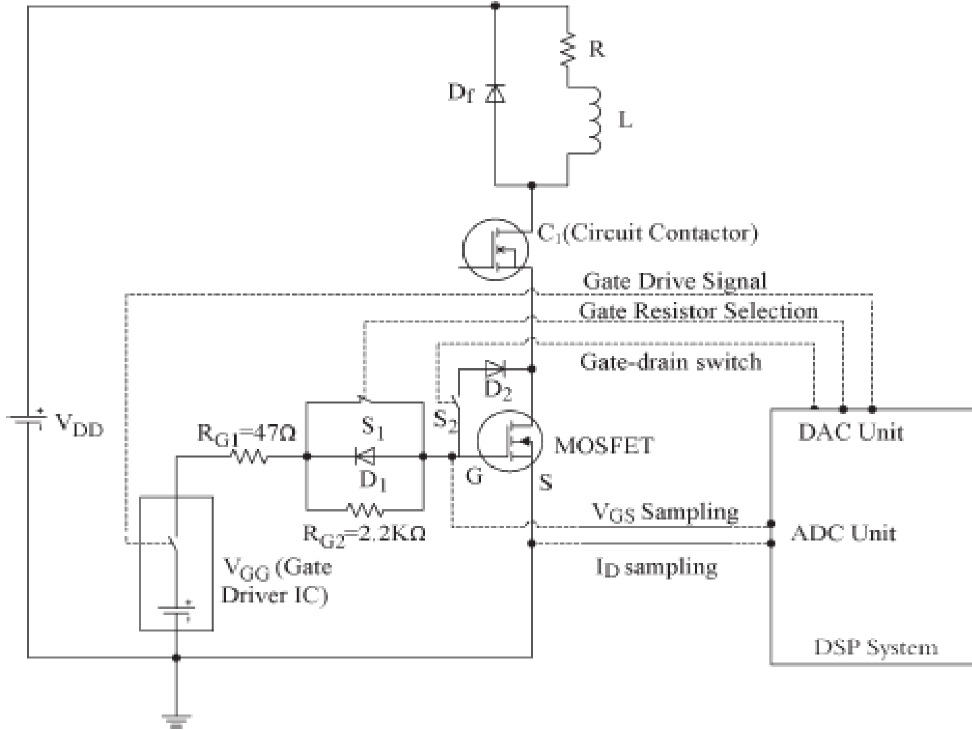


Figure 2.8: V_{th} sensing circuitry requiring disconnection from main circuit by C_1 to better acquire V_{th} value [48]

conditions; therefore, many attempts to incorporate the measurements in converter setups have required significant modification to the converter or control strategy. This can include the addition of supplementary components, momentary disconnection of power devices from the power circuit, and interruption to normal load current control [54].

Threshold Voltage

One of the most popular TSEPs is threshold voltage (V_{th}) [48, 55]. However, when graded against the criteria, it has been tested to have low sensitivity, inability to online sense, and potential to lose calibration from gate oxide trapping. Zhang *et al.* [55] analyze the relationship of $R_{g,int}$, R_{on}, and V_{th} with T_j for Si, SiC, and GaN devices. They conclude R_{on} and V_{th} are the best TSEPs, but they did not consider other impressive TSEPs in this study or account for difficult online sensing ability for these TSEPs. Also, this parameter as a TSEP is worse for SiC devices according to Table 2.1. Chen *et al.* [48] also realized the difficult to online monitor V_{th}, as mentioned earlier, in their application to estimate junction

Table 2.1: Junction temperature sensitivity of V_{th} for Si devices and SiC devices [55]

Power Device	T_j coefficient of V_{th}	Comments
Si MOSFET	-4.0 mV/°C	Linear
CoolMOS	-6.4 mV/°C	Linear
Si IGBT	-5.4 mV/°C	Linear
SiC MOSFET	-2.3 mV/°C	Linear

temperature for thermal path models incorporating thermal aging effect and comparing the results to a TSEP based junction temperature monitoring with V_{th}. They had issues during the switching transients from measurement noise but disconnected the device from the DC link during steady state to inject 5 mA into the device and record the V_{GS} considered as V_{th}. This was still very difficult, thus showing V_{th} is not the best TSEP and further analysis must be done to find a better approach.

Drain-Source On-voltage

Another traditional and popular TSEP is the device drain-source on-voltage. This condition as a TSEP has been highly researched for IGBTs. It is separated into two categories: under low current and under high current. The reason for on-voltage under low currents (i.e. close to 0 A) is the single dependence on temperature, good linearity, and good sensitivity. However, since most power electronic applications drive devices at high currents, applications implementing V_{on} sensing at low current must disrupt the converter operation to sense the V_{on} parameter. Therefore, V_{on} under high currents was researched to counteract this drawback. It still has relatively good linearity and sensitivity; however, now the drawbacks are dependence on current and gate voltage as well as needing accurate current sensors during operation.

When it comes to relating this TSEP to SiC based applications, V_{ds-on}, as a TSEP, is intrinsically worse in SiC than IGBTs as shown in [56] and in Figure 2.9. This figure uses on-resistance, which can be directly related to on-voltage using Ohms law, and shows that on-voltage as a TSEP for SiC is less sensitive and non-linear. Now it can still be used as a viable approach as shown in [57], but special design considerations must be taken into

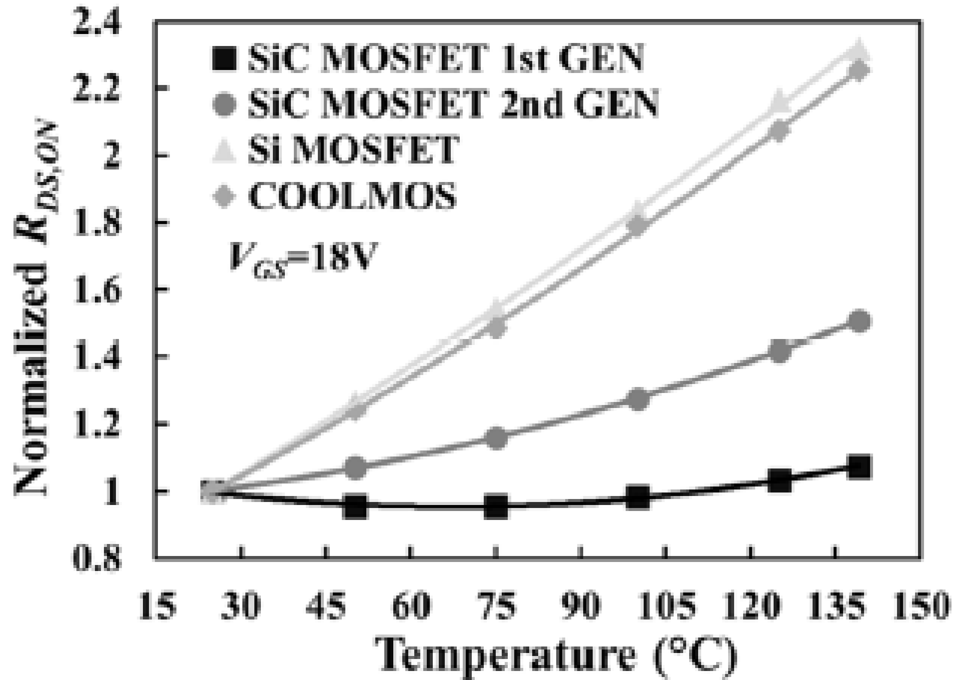


Figure 2.9: On-resistance as a function of junction temperature for SiC and Si devices [56]

account. A special and precise on-voltage circuitry was added to the gate driver to obtain the needed on-voltage reading. The DC-DC converter was operated in closed-loop so the current through the tested SiC device was easily accounted for. The implementation results can be seen in Figure 2.10, and one thing to note that was not considered was the aging effect of on-resistance from bond wire lift-off, which can reduce the accuracy of the approach over time.

The second type of TSEP approach is a static parameter (voltage/current) that can be statically characterized (i.e. with a curve tracer) against temperature.

Body Diode Forward Voltage

Another power semiconductor parameter leveraged as a TSEP of T_j is the diode forward voltage (V_f) [58, 59, 36]. Bergogne *et al.* [59] needed a way to know the junction temperature for SiC JFETs under lightning induced over-voltages. The issue associated with this method is the calibration must be done at low current to obtain an effective calibration curve with good sensitivity and linearity. However, the test during which to monitor forward voltage is

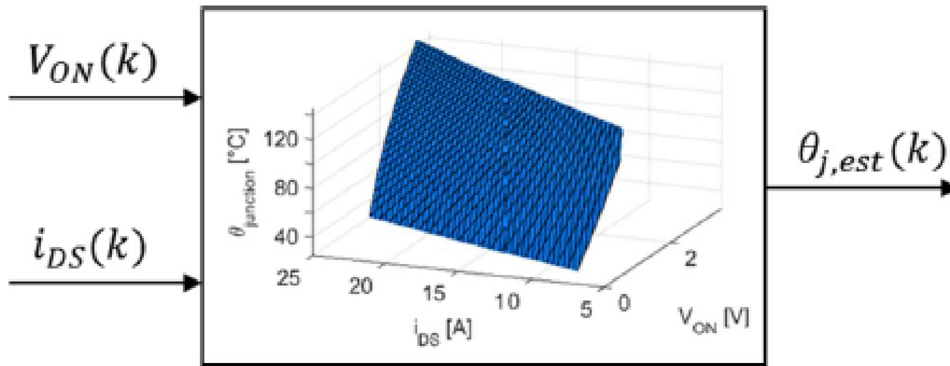


Figure 2.10: Capturing of V_{ON} and I_{DS} lead to estimated junction temperature through temperature calibration [57]

under a high current so a special test circuit is designed to relieve the DUT from the high current injection for a short duration to obtain the forward voltage value under low current. This causes the junction temperature to decrease in the hundreds of microseconds it takes to decrease the current thus creating an error in measuring the junction temperature that is difficult, they found, to compensate for as their error due to the electrical measurement is estimated to be 10 °C.

Another important topic is further expanded upon in this V_f based TSEP temperature sensing approach [58]. Using V_f for SiC Schottky diodes, the calibration curve is dependent on the current injected. In power modules, multiple SiC dies are used, where those dies can have slight variations in performance. This can cause the current sharing to be unequal; and thus, the junction temperatures will be different. This also means that the TSEP-based sensing will not account for this and cause error in the temperature sensing (i.e. obtain an average temperature over the entire module instead of the max temperature). Figure 2.11 and 2.12 shows the testing [58] conducted on this issue where the measured TSEP-based temperature recording tracks the average temperature of the two SiC devices. Therefore, this is a potential issue with the TSEP temperature sensing for implementation in a SiC power module.

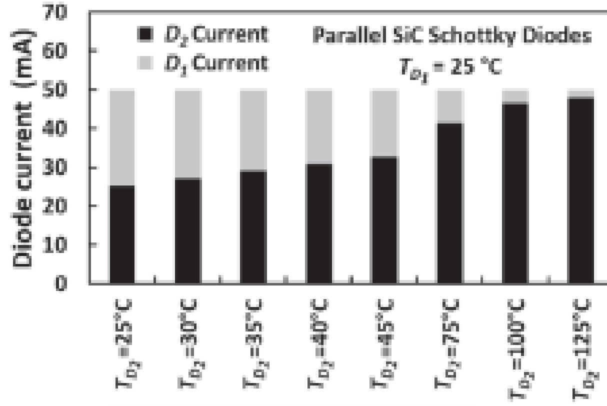


Figure 2.11: Current distribution mismatch for parallel-connected SiC devices D_1 and D_2 set to different temperatures [58]

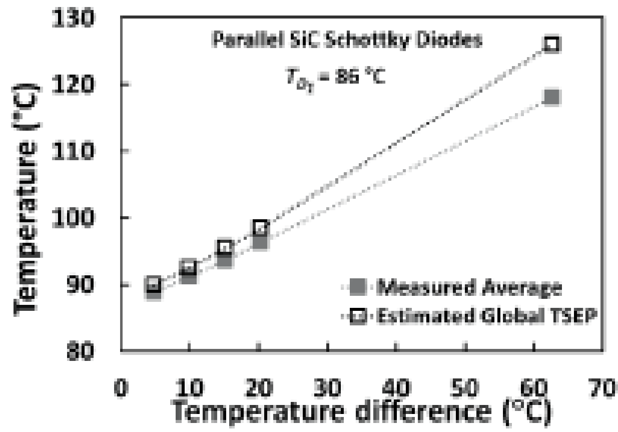


Figure 2.12: Measured TSEP temperature value vs. true averaged temperature value for D_1 and D_2 as temperature difference increases [58]

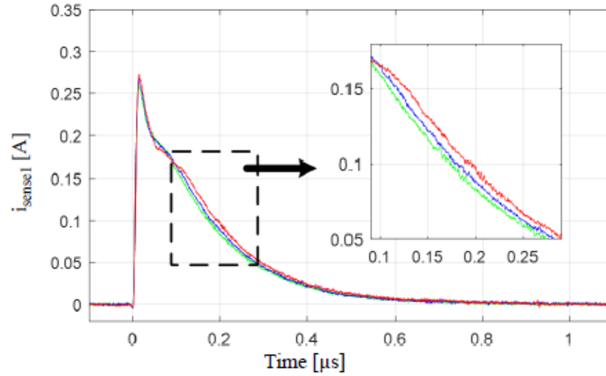


Figure 2.13: Sensed gate current for the push-pull topology at T_j = 45 °C (in green), 78 °C (in blue), and 105 °C (in red) [60]

Gate Current/Internal Resistance

A static parameter growing in popularity is the MOSFET gate current that varies with temperature because of the internal gate resistance dependence on temperature [44]. Niu *et al.* [60] uses gate current as their TSEP approach for SiC devices. They start by characterizing and evaluating (through simulation) different gate drive topologies: push-pull gate drive, current mirror gate drive, and inductor-based gate drive. This is done because of the different gate current sensing schemes that is needed for the different. Figure 2.13, 2.14, and 2.15 show the variations of gate current for the three gate drive topologies, which is why two different gate current sensing strategies are employed: $\int I_G$ sensing and I_{G-peak} sensing. The $\int I_G$ sensing technique is used for the push-pull and inductor based approaches where different gate current areas indicate the operating junction temperature. The I_{G-peak} sensing technique is used for the current mirror approach where the peak gate current value indicates the junction temperature. Now there are a few issues with this TSEP and sensing approach. First, gate current also depends on DC voltage and load current so those conditions must be considered, which adds complexity. Second, the gate current and sensing circuits are sensitive to noise and parasitics so careful board design and layout must be considered. Third, as the gate current is a fast transient signal, the sensing tolerance is a high 12 °C. However, a benefit of this approach is the fact that converter operation does not have to be disturbed as everything is kept on the control side of the power electronic system.

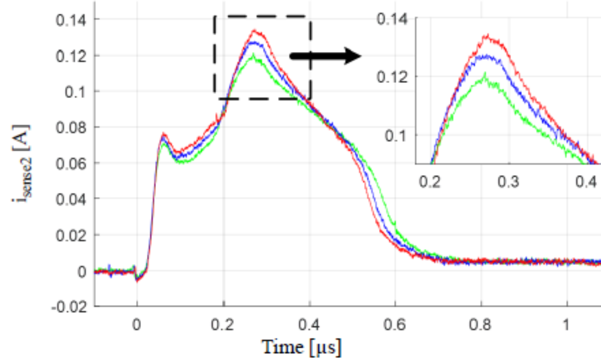


Figure 2.14: Sensed gate current for the current mirror topology at T_j = 45 °C (in green), 78 °C (in blue), and 105 °C (in red) [60]

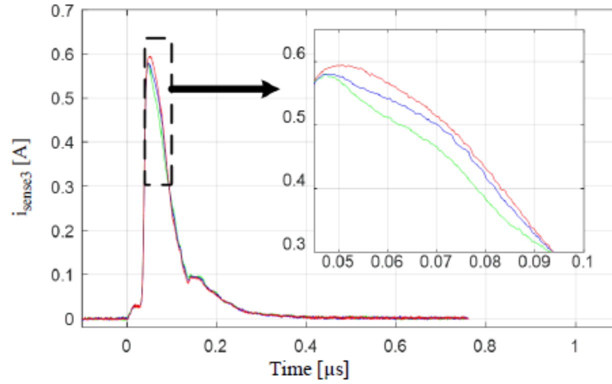


Figure 2.15: Sensed gate current for the inductor based topology at T_j = 45 °C (in green), 78 °C (in blue), and 105 °C (in red) [60]

The third type of TSEP scheme is a dynamic parameter (time-based) that is dynamically characterized (i.e. with a DPT) against temperature.

Turn-off Delay Time

A minor variation of V_{th} as a TSEP is the turn-off delay time ($t_{d,off}$). As the prequel literature to part of this work, Zhang *et al.* [51] investigates $t_{d,off}$ as a viable TSEP of junction temperature for SiC devices, focusing on the sensitivity analysis of this given TSEP in SiC. The biggest issue with $t_{d,off}$ as a TSEP is the poor sensitivity; however, a gate resistance regulation circuit was designed to accompany the online $t_{d,off}$ monitoring system to improve the sensitivity. This makes $t_{d,off}$ a competitive TSEP with passing grades in linearity, sensitivity, accuracy, and online capability. Also, the calibration curve can be seen, from earlier analysis, in Figure 2.6. One minor issue with $t_{d,off}$ as a TSEP is the

need to calibrate each device used in temperature sensing because of the intrinsic properties variation among SiC devices. Turn-off delay time can still experience shifts from gate oxide degradation; however, newer generation SiC devices have shown more gate oxide reliability [61]. This thesis will take this previous work a step further by applying the TSEP T_j sensing scheme into a intelligent gate driver with additional sensing features and obtaining more simulation and experimental results.

Turn-on Delay Time

A slight variation of $t_{d,off}$ that can be used as a TSEP is the turn-on delay time ($t_{d,on}$), which is the time from the start of the rise in gate voltage to the start of the rise in drain current. The equation, discussed in [62], for $t_{d,on}$ is given in 2.4.

$$t_{d,on} = R_G C_{iss} \ln(\frac{1}{1 - \frac{V_{th}}{V_{GS}}}) \tag{2.4}$$

It is similar to turn-off delay time in that it uses the temperature dependence of threshold voltage to be dependent on junction temperature itself. However, it is different from $t_{d,off}$ in that it is independent of current shown in Figure 2.16, which can be better leveraged in some applications like paralleling devices in a converter [63].

Shi *et al.* [64] use $t_{d,on}$ as their TSEP for junction temperature monitoring and implement it for Si and SiC devices. Seen in Table 2.2, SiC devices exhibit less sensitivity than Si, which is a trend in most TSEP cases. Their monitoring system is unique in that they impose a short impulse signal ($V_{impulse}$) on the gate voltage while the device is on. This gives better sensitivity for the $t_{d,on}$ capturing during the turn-on of the impulse signal. This scheme, combined with the reduced sensitivity, means two things: one, using this $t_{d,on}$ sensing approach needs a higher impulse signal which could result in current runaway or damage from high gate voltage, and two, the device current sensing must have high accuracy and bandwidth. The last point creates a tough design constraint as the sufficient current sensors (i.e. resistor shunts) must operate at lower currents due to power loss constraints.

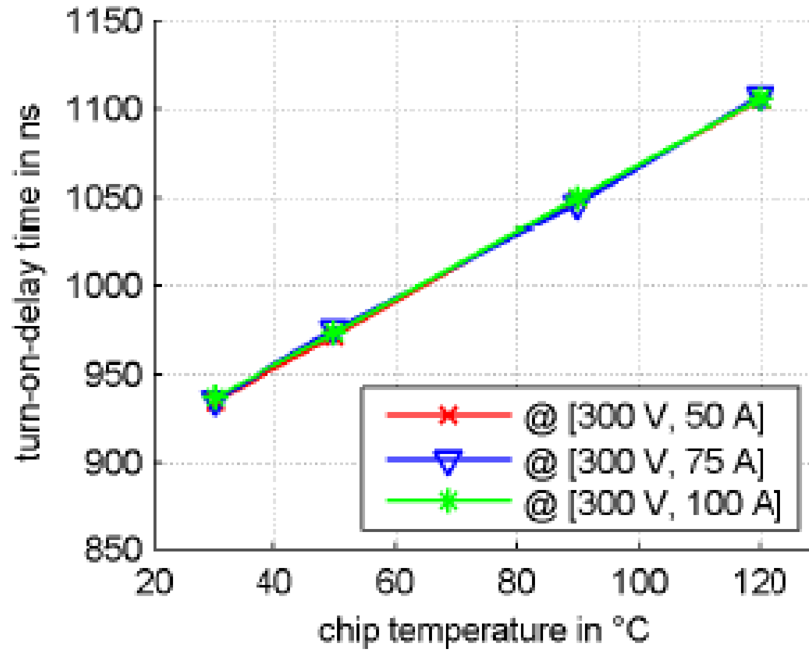


Figure 2.16: Turn-on delay time vs. junction temperature with independence from device current [63]

Table 2.2: Sensitivity of $t_{d,on}$ approach using gate voltage impulse signal for Si and SiC devices [40].

I_{DS} / $V_{impulse}$	0.2 V	0.4 V	0.6 V	0.8 V	1.0 V	Sensitivity
HRM7433D	1.150 A	2.425 A	3.688 A	4.938 A	6.250 A	6.651 A/V
IRFP260N	1.175 A	2.375 A	3.675 A	5.063 A	6.313 A	6.553 A/V
C2M0080120D	0.625 A	1.125 A	1.785 A	2.413 A	3.075 A	3.184 A/V

Drain-source Current Switching Rate

Gonzalez *et al.* [56] proposes output current switching rate coupled with the gate current plateau (I_{GP}) during turn-on as a TSEP for SiC devices. This TSEP is similar to $t_{d,off}$ where the gate resistance needs to be abnormally large (i.e. hundreds of ohms) to give good enough sensitivity between dI_{DS}/dt and T_j. The work was not able to create a monitoring system because of the complexity to have precise and fast dI_{DS}/dt monitoring as well as implementing gate resistance regulation to prevent high gate resistance during the entire operation. The potential for this TSEP is there with good linearity and temperature accuracy but intelligent gate driver ability is needed to balance the need for fast switching capability to improve converter size and performance but also high gate resistance (i.e. reduced switching speed) to measure dI_{DS}/dt.

2.2 Adaptive Dead-time Systems

For a phase-leg configuration of switching devices used in any VSC, the dead-time between the two devices is a critical parameter. The dead-time is necessary to prevent both devices from turning on and causing shoot-through failures; however, it causes issues in converter performance. Dead-time adds power loss in the form of body diode conduction loss and adds voltage distortion at the output of the converter. Therefore, adaptive dead-time regulation schemes can become beneficial by enhancing reliability (i.e. reduce heat from losses), improving converter efficiency, and enhance inverter output power quality.

2.2.1 Dead-time Elimination

One traditional approach is trying to eliminate the dead-time needed in a phase-leg of a inverter [65, 66, 67]. This is done by only switching one of the power semiconductors transistors for a half fundamental cycle and only switching the other transistor in the phase-leg for the other half fundamental cycle. This concept is shown in Figure 2.17. There are two keys to having successful dead-time elimination: free-wheeling diode conduction and precise current polarity detection. For utilizing the internal free-wheeling diode conduction, this

can work for an IGBT-based approach; however, in SiC applications, the MOSFET's body diode has a higher forward voltage, which would cause more overall device losses (mentioned in section 1.2.1) and make this type of approach insufficient.

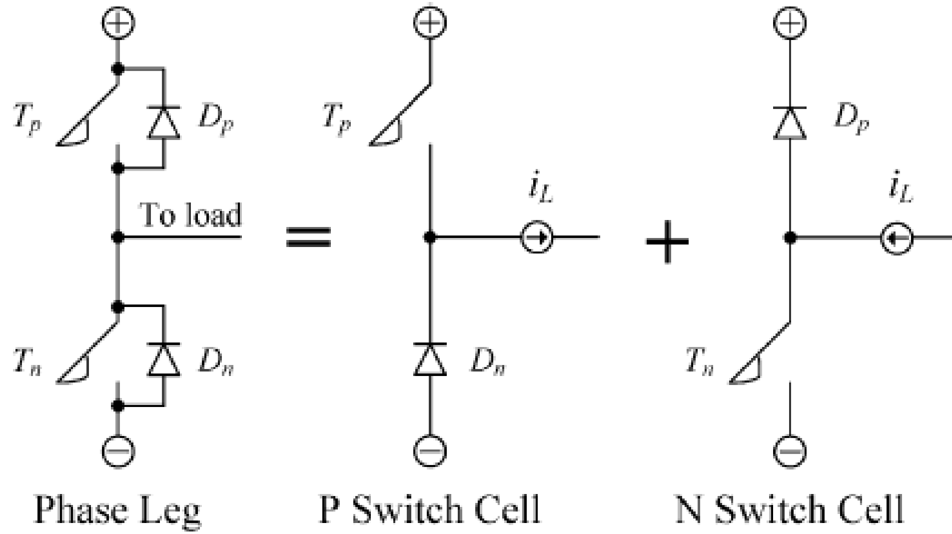
Also, in terms of current sensing, all three works state that precise current detection around the zero-crossing of a VSI is inaccurate. Chen et al. [65] adds complexity to their dead-time elimination system to avoid this issue. Wang et al. [66] and Yuan et al. [67] change their dead-time correction schemes around the zero crossing, which again avoids the issue of zero-current crossing. There is a need for SiC applications to design a dead-time correction scheme that can avoid body diode conduction and successfully accounts for the switching cases around the zero-current crossing without added complexity.

2.2.2 DC-DC Dead-time Regulation Schemes

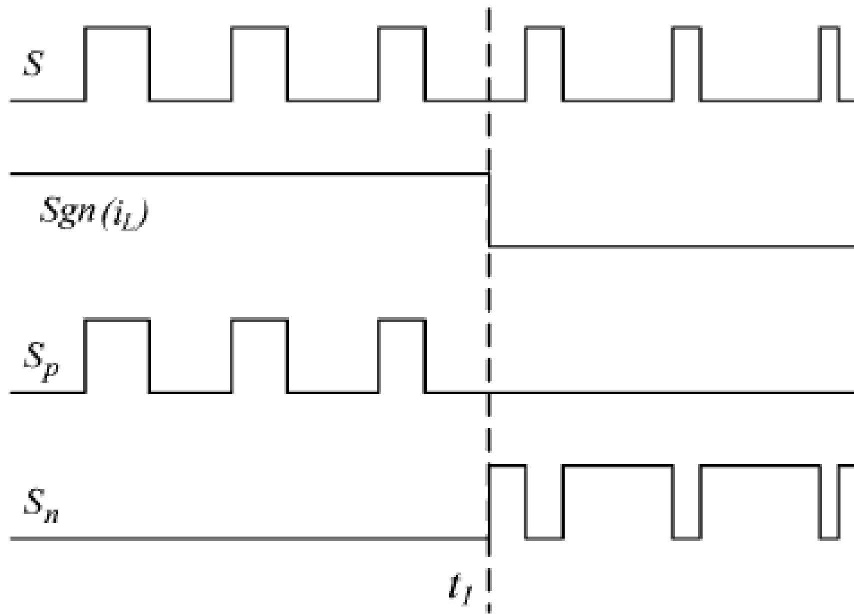
Other works have the same goal in mind as this proposed work, which is still implementing dead-time but optimizing the amount of dead-time in a switching cycle [68, 69, 70] to minimize device power loss. Yousefzadeh et al. [68] designed a control algorithm for DC-DC converters using traditional output voltage regulation feedback along with incremental change in dead-time each switching cycle to obtain the optimal dead-time and duty cycle. Lee et al. [69] also optimizes the dead-time in DC-DC converters but uses dead-time error voltage sensing circuits. A limitation with these works is they are limited to only DC-DC converters, where the current does not change from switching cycle to switching cycle. Therefore, these strategies cannot be applied to all 2-level VSCs, which is something this work will design to achieve.

2.2.3 Dead-time Compensation Including Non-ideal Switching

Dead-time compensation is a term used for strategies that look to fix the negative output voltage distortion from dead-time in VSIs. One major method of dead-time compensation is using the voltage-second balance theory [71, 72, 66, 28]. All of these papers analyze what causes the midpoint PWM output voltage to distort from the ideal pulse square waveform and how to best compensate for the distortion this causes on the converter. This is the ideal



(a) Phase-leg conduction for output current direction



(b) Dead-time elimination control scheme

Figure 2.17: Dead-time elimination concept [65]

approach for high frequency VSI applications since it breaks down the volt-second error on a switching cycle level. Limitations with traditional voltage-second balancing schemes, however, start with the need for a high bandwidth current transducer with inaccurate dynamic current sensing like the dead-time elimination schemes before. Also, most volt-second balancing schemes are an offline model-based implementation, which potentially does not account for variables involved in creating the voltage distortion like the load conditions effect on the voltage distortion.

Another common dead-time compensation scheme is using a feedback controller that sends the output characteristics back to the controller and compares to a reference to compensate for this distortion [73, 67]. This method is limited, especially in high frequency applications, because of the slow response time aspect of feedback controllers. Also, these methods require high control bandwidth and a complex controller that limit the flexibility of this type of compensation scheme.

2.3 Summary

Junction temperature monitoring is important for both controlling the temperature during converter operation and assessing the health of the device as junction temperature is a key indicator of health. In recent years, there has been more research work for TSEP-based temperature sensing in SiC applications. Apart from more research on SiC in general, there is more research is in this specific area because there is a need for a real-time, non-invasive SiC converter application temperature sensing scheme. After analyzing the different TSEPs for SiC and their sensing schemes, the conclusion is the TSEP scheme is a viable temperature sensing approach. Even though SiC is less sensitive to temperature due to the wider bandgap, there has still been successful work in developing innovative methods to use TSEPs to achieve junction temperature monitoring. From a general approach point of view, there are a few detailed areas of future work for the TSEP approach. First, little work has been done on the proper temperature verification method for a given TSEP. Second, there has yet to be a research work that implements a TSEP temperature sensing approach in a SiC intelligent power module.

Dead-time control is an important design condition for voltage-source inverters so negative effects of power loss and output voltage distortion can be compensated for. The literature shows there are different types of dead-time control schemes: compensate the volt-second error, optimize the dead-time setting, and eliminating dead-time altogether. With the application being a SiC-based high frequency VSI, it was concluded that a dead-time optimization method was better than dead-time elimination to avoid long free-wheeling diode conduction. Also based on the application, voltage-second balancing is a great approach to implement for compensation of the voltage distortion, but the issue of current polarity sensing must be considered.

Chapter 3

Switching Time Monitoring Design

3.1 Overview

The objective of this design is to construct an online, gate driver integrated switching time monitoring scheme for SiC devices. This objective is derived from the motivation to both incorporate indirect T_j sensing in a converter for reliability improvement and dead-time control for high frequency SiC VSCs.

3.2 Behavior of Switching Times for SiC Devices

The turn-off transition of the switching devices will be the focus of this monitoring system. The turn-off delay time was introduced in Section 2.1.3, but will be further discussed here. The turn-off delay time is defined as the time from the start of the fall in V_{GS} to the start of the rise in V_{DS}, shown in Figure 3.1. The equations of $t_{d,off}$ is shown in equation 3.1.

$$t_{d,off} = R_G C_{iss} \ln(\frac{V_{GS}}{V_{gp}}) \tag{3.1}$$

V_{gp} is the miller voltage, which is defined in equation 3.2.

$$V_{gp} = V_{th} - \frac{I_d}{g_m} \tag{3.2}$$

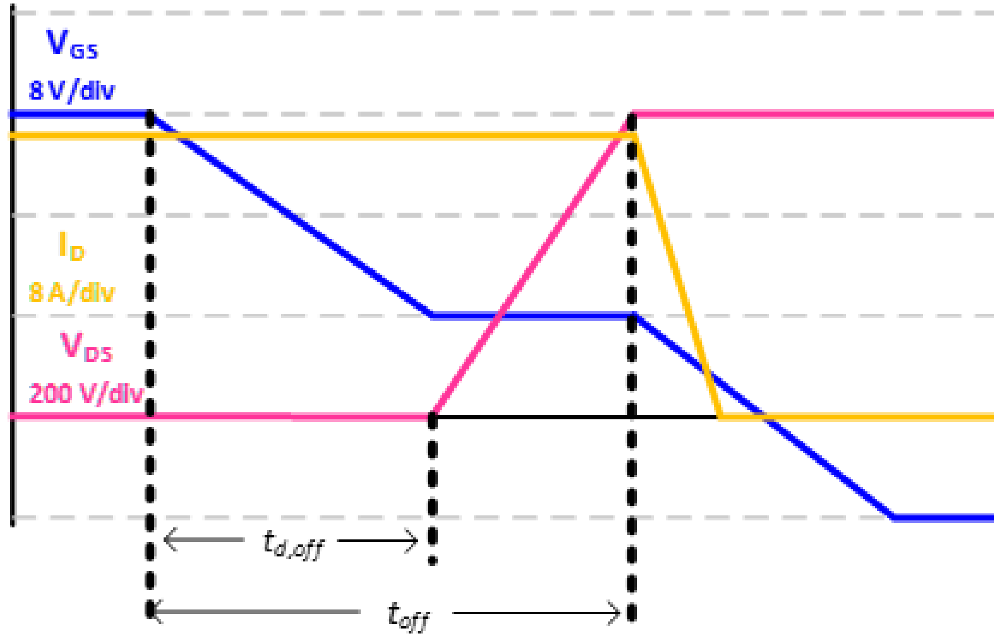


Figure 3.1: MOSFET turn-off transition showing turn-off delay time and defined turn-off time

The turn-off time of interest in this work is defined as the time from the start of the fall in V_{GS} to the end of the rise in V_{DS}. The equation of t_{off} is shown in equation 3.3, which is just $t_{d,off}$ plus the time it takes to charge the miller capacitance (i.e. the drain-source voltage commutation time).

$$t_{off} = R_G C_{iss} \ln(\frac{V_{GS}}{V_{gp}}) + R_G C_{gd} \frac{V_{DS}}{V_{gp}} \tag{3.3}$$

3.2.1 Sensitivity to Junction Temperature

One behavior of the switching time of any MOSFET is its variance with operating device temperature (i.e. junction temperature). This behavior can be traced back electrically to the transfer characteristic curve of the device, shown in Figure 3.2 for the test case device: Wolfspeed 2nd generation 1200 V SiC (C2M0080120D). With the change in V_{th} and g_m on the transfer curves for different junction temperatures, it can be seen using equations 3.1 - 3.3

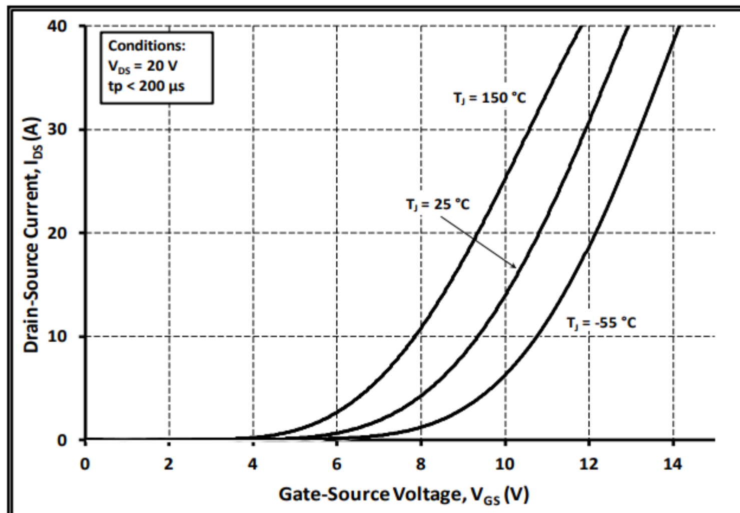


Figure 3.2: Wolfspeed SiC device datasheet — transfer characteristic curve

that this would cause $t_{d,off}$ and t_{off} to vary as well. This is important for the TSEP-based T_j monitoring scheme that will be implemented in Chapter 4.

To give an introduction on the sensitivity of $t_{d,off}$ with respect to T_j, a LTspice simulation was set up using the available Wolfspeed Spice model of their C2M0080120D SiC MOSFET. The spice schematic is shown in Figure 3.3, where the test is a DPT and the device can be thermally controlled with a voltage source.

Then, the $t_{d,off}$ is recorded for different operating temperature and currents with a R_g = 10 Ω. The corresponding calibration curves are shown in Figure 3.4, where it can be deduced that the device's $t_{d,off}$ sensitivity to T_j is inherently low. This is expected as mentioned in section 2.1.2 where SiC devices have less variability with temperature and for $t_{d,off}$ specifically, the input capacitance is less than Si MOSFETs so according to equation 3.1, that would cause less sensitivity.

Therefore, to achieve the online junction temperature monitoring using the turn off delay time with sufficient accuracy, either the sensitivity of turn-off delay time with respect to junction temperature should be enhanced or the resolution of turn-off delay time measurement should be high enough, or both should be improved simultaneously.

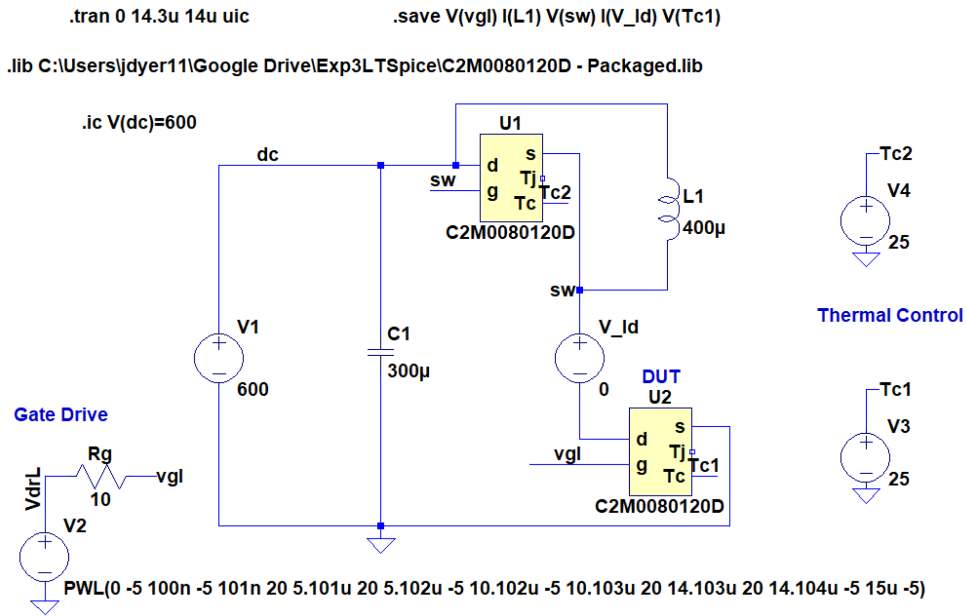
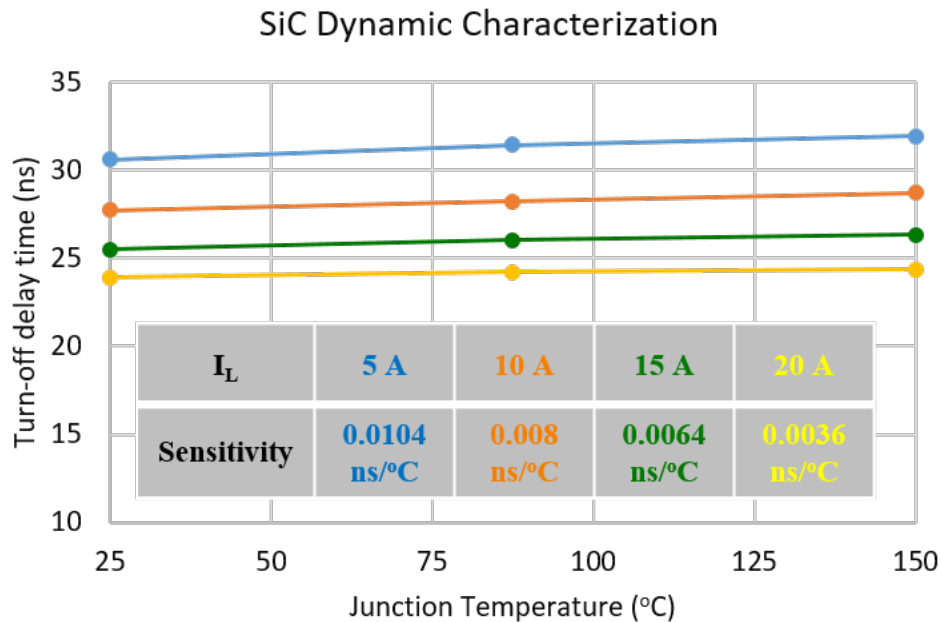


Figure 3.3: LTspice simulation to dynamically characterize Wolfspeed C2M0080120D SiC MOSFET



I_L	5 A	10 A	15 A	20 A
Sensitivity	0.0104 ns/°C	0.008 ns/°C	0.0064 ns/°C	0.0036 ns/°C

Figure 3.4: C2M0080120D natural $t_{d,off}$ vs. T_j sensitivity

3.2.2 Dependence on Voltage/Current

Ideally the selected TSEP only depends on temperature; however, turn-off delay time has other conditions that it depends on. In regards to current, turn-off delay time is dependent on that because of miller voltage (V_{gp}) having current in its equation 3.2. Also in regards to voltage, turn off delay time is not dependent on voltage because it is in the ON state and at a low voltage during turn-off delay time.

This is important in regards to the device application and hardware setup. First, in terms of the connections needed for sensing, turn-off delay time needs a drain connection along with the typical gate and source connection, which means the design must take the high voltage of the converter into the sensing circuit design. Second, for a power module application, the dies in parallel all have the same V_{DS} waveform but can have different I_D values; therefore, using $t_{d,off}$ will only give you the overall power module T_j and not indicate any current sharing mismatch. In a power module system where it is preferred to know the individual SiC die temperature, it is better to use $t_{d,on}$ as the TSEP because it does not depend on current and the calibration cannot be affected by current mismatch during converter operation. With this work's application being a single MOSFET in the TO-247 package, using $t_{d,off}$ as the TSEP is sufficient.

3.2.3 Different Types of Switching

For SiC phase-legs, the turn-off time (t_{off}) is sensitive to operating conditions and converter load characteristics [26, 27]. An example of this is looking at the hard turn-off transition of the low side SiC device, where the current is flowing into the phase-leg. This is simulated in LTspice with the Wolfspeed C2M0080120D SiC MOSFET model used before in section 3.2.1 but now it is placed in a half-bridge inverter with switching transition results shown in Figure 3.5. When load current is smaller, dv/dt of the drain-source voltage is limited by the power loop. All of the low I_L current is used to charge the output capacitance of the device, which causes the channel current to fall to zero faster than it takes to raise V_{ds} to the DC bus voltage. This means voltage rise time (t_{vr}) is longer than current fall time (t_{cf}), as shown in Figure 3.5a, and this case is called the power loop dominated turn-off. For the

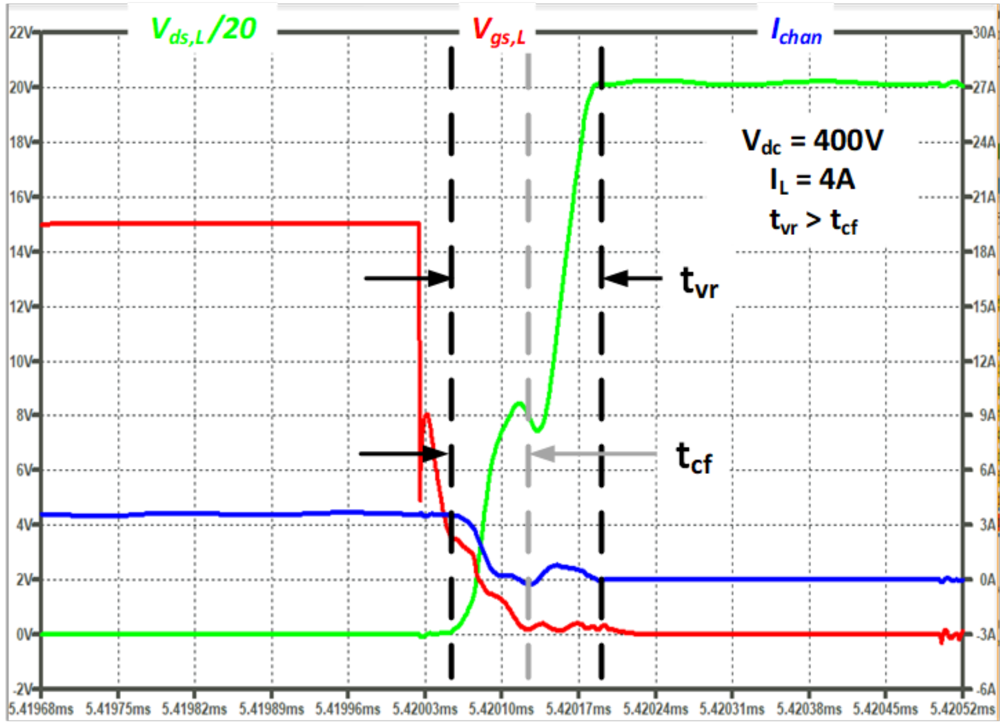
case of higher load current, only a portion of the load current is needed in the power loop to charge the output capacitance, whereas the rest of the load current travels via the gate loop. This means current fall time (t_{cf}) is longer than voltage rise time (t_{vr}), as shown in Figure 3.5b, and this case is called the gate loop dominated turn-off.

Therefore, the optimized dead-time (which is a application for this sensing design) for the case of a hard-turn off is dependent upon t_{vr} and t_{cf}, which are dependent upon load current. Now the online monitoring system, which will be discussed in more detail in section 3.3, can obtain the t_{vr} value for any switching cycle. However, it is difficult to monitor channel current and therefore know t_{cf}. So, Figure 3.6 shows the model used for optimized dead-time ($t_{dt(opt)}$) for the hard turn-off case, where monitored t_{vr} is used as $t_{dt(opt)}$ until the max t_{cf} value is reached and used as $t_{dt(opt)}$.

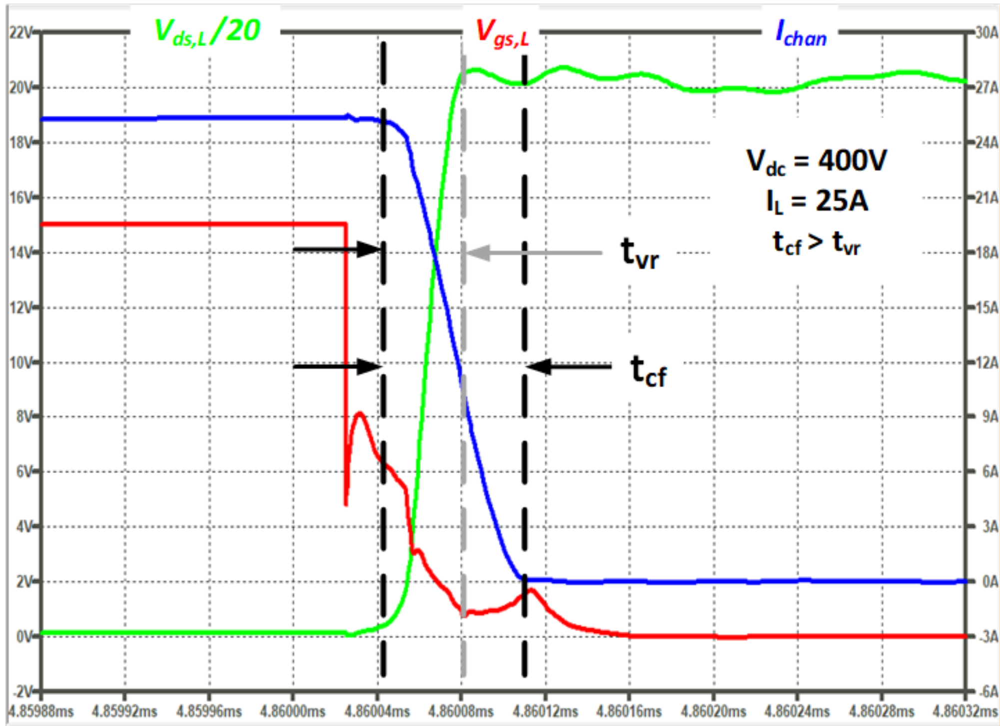
The analysis for dead-time optimization is not complete yet because the previous section only looked at a hard turn-off case for the low side device in a phase-leg configuration. This was because, in previous works, the converter topology chosen was a buck converter configured to have the DC load current flowing into the phase-leg, which makes the low side device the operating device and makes the upper SiC device be the synchronous device. However in a VSI application, the load current is AC and thus both devices can be the operating device and synchronous device depending on the current polarity, which means there are special considerations needed to be analyzed for full dead-time optimization.

Soft Turn-off Case

A power switching device experiences a soft turn-off when the load current is flowing in the direction of source to drain (i.e. the device is acting as the synchronous device). The turn off transition for this case can be seen in Figure 3.7d. For a VSI application, both switches can be the synchronous device so it would seem there is a need for current sensing to indicate the current polarity for each switching cycle. However, the monitoring system can be leveraged to indicate current polarity and this detail will be shared in section 3.4.3. The optimal dead-time in this case is just the time it takes for the gate-source voltage to drop to 0 V to prevent both channels turning on and causing a shoot-through current spike.



(a) at low currents, voltage rise takes longer ($t_{vr} > t_{cf}$)



(b) at high currents, current fall takes longer ($t_{cf} > t_{vr}$)

Figure 3.5: SiC LTSpice switching waveforms during the turn-off transient

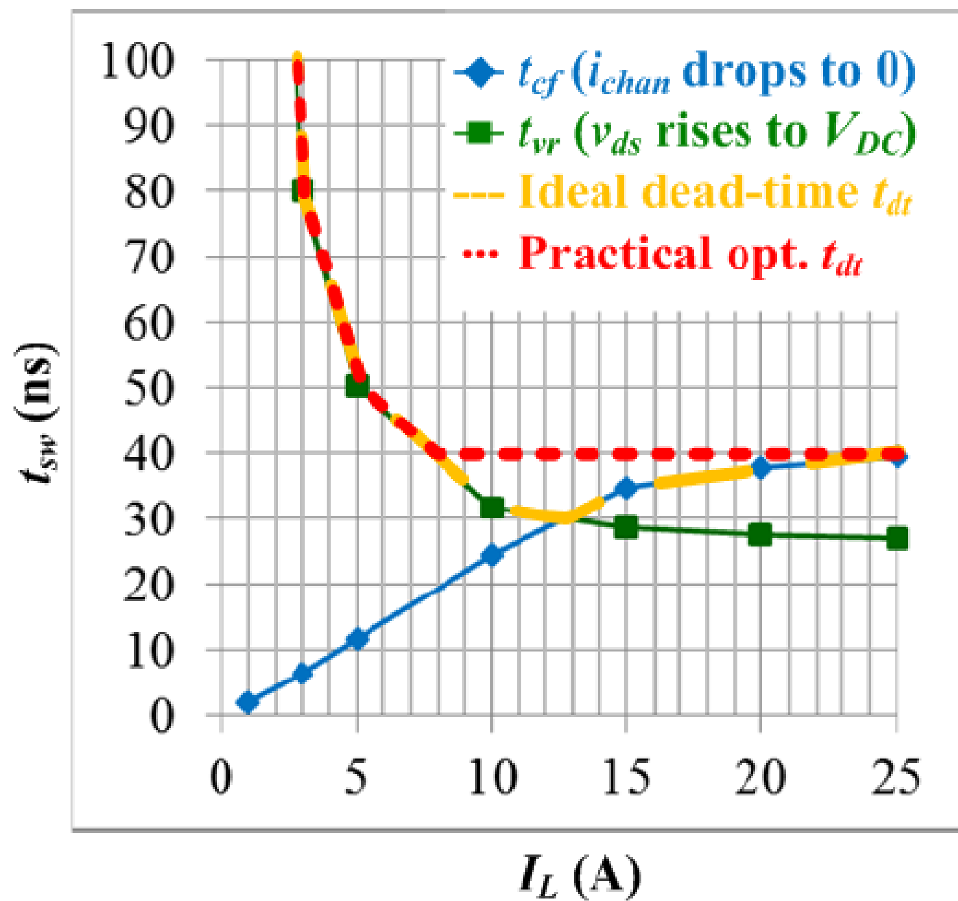


Figure 3.6: t_{cf} vs. t_{vr} determining optimal dead-time for hard turn-off case

Partial Hard Turn-on from Synchronous Device

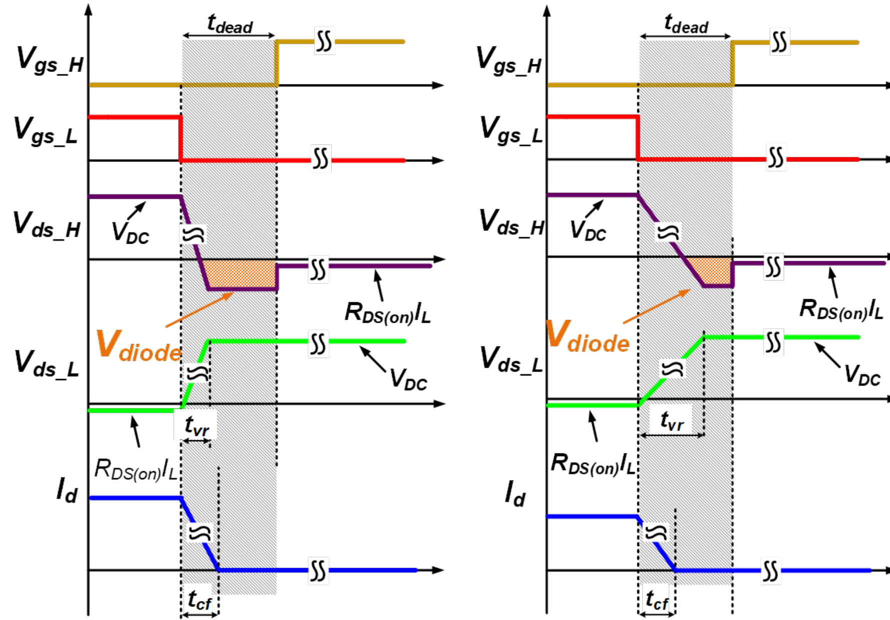
Another type of turn-off transition that can be seen in VSI operation is the partial hard turn-on for the synchronous device. This type arises when dead-time is set too aggressively and becomes shorter than the drain-source voltage rise time as shown in Figure 3.7c. This eliminates the reverse conduction losses but causes switching power loss in the synchronous device when it experiences a partial hard turn-on, which does not solve the problem of optimizing dead-time to reduce power loss. There is not an easy way to mitigate this through monitoring though as it would take knowing the voltage value the V_{ds} rose to before the partial hard turn-on to know how long the dead-time should be in this switching cycle case. The best way to avoid this case is conservatively set the dead-time in initial VSI operation.

In summary, the switching transition experienced in a VSI application during dead-time can be seen in Figure 3.7. This figure also shows where the reverse conduction power loss (i.e. case (a), (b), (d)) or switching losses (i.e. case (c)) occur. This phase-leg switching time monitoring system will log the turn-off times in a micro-controller and indicate the type of switching (discussed in more detail in section 3.4). This data can then be used to set optimal dead-time lengths to reduce power loss (shown in the results in chapter 4).

3.3 Time Detection Scheme

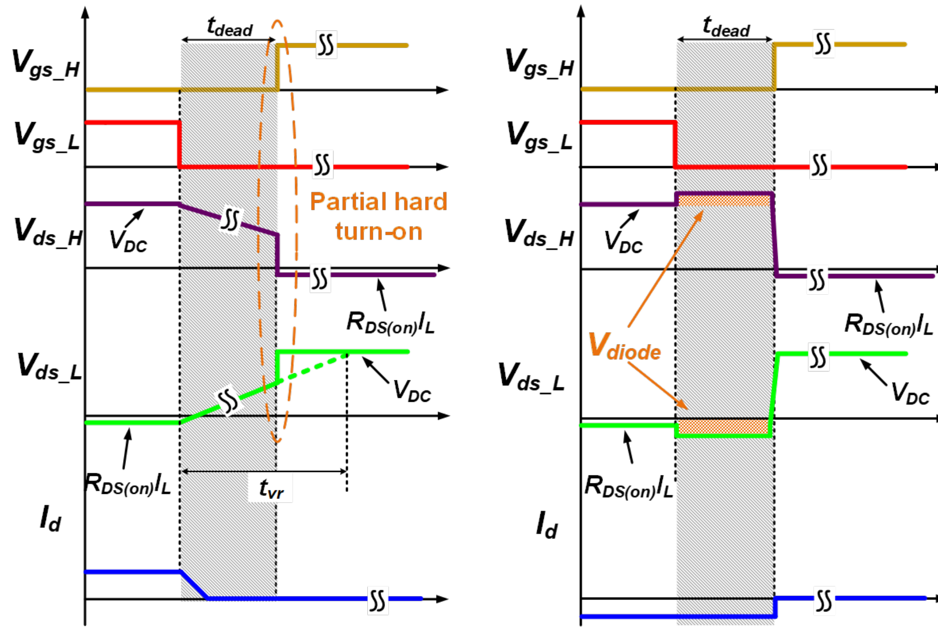
Two detection systems (one for each device) are implemented along with the gate driver circuits that capture the moments needed to monitor these timing conditions. Figure 3.8 shows a block diagram of the developed online switching time monitoring system. The intelligent gate driver assist circuits obtain the signals, gate-source voltage transient detector (GVTD), drain-source voltage transient detector (DVTD), and drain-source voltage fall-time detector (DVFD), from the gate-source voltage and drain-source voltage of the SiC device. These edge-detection signals produced are sent back to the micro-controller to be used to calculate the turn-off delay time, turn-off time, and voltage commutation time as shown on the left side of Figure 3.8.

The detection circuit schematics are shown on the right side of Figure 3.9a. GVTD occurs when the gate-source voltage begins to drop from the 20 V on-state. Each component in



(a) current fall dominated hard turn-off ($t_{dt} > t_{cf} > t_{vr}$)

(b) voltage rise dominated hard turn-off ($t_{dt} > t_{vr} > t_{cf}$)



(c) voltage rise dominated hard turn-off with partial hard turn-on ($t_{vr} > t_{dt} > t_{cf}$)

(d) soft turn-off

Figure 3.7: Diagram of all possible turn-off switching waveforms in a VSI application, showing diode losses in the dead-time

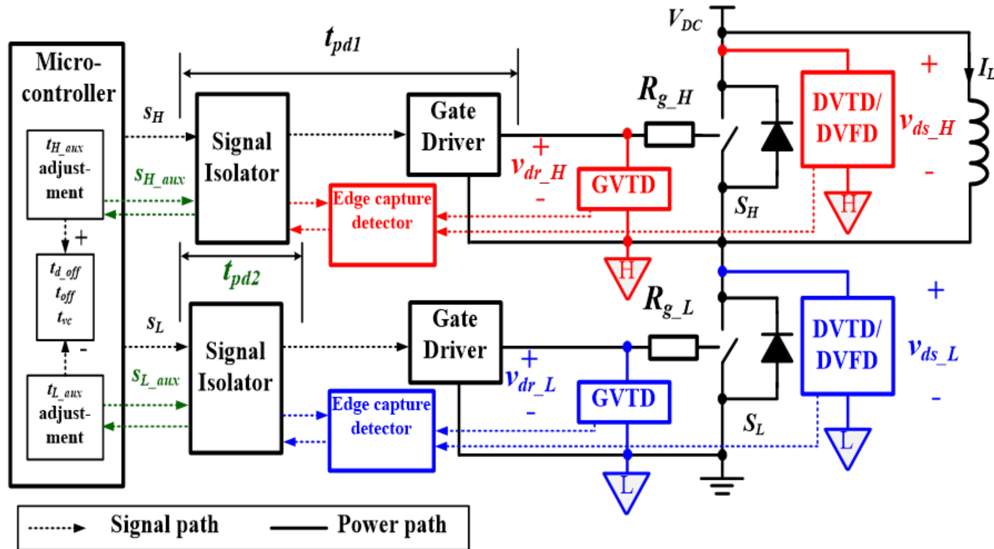


Figure 3.8: Block diagram of online monitoring system

this circuit plays a role in achieving the fast transient step. The diode bridge helps keep the output signals between the control-level voltage rails of 5 V and GND since the input signals (i.e. V_{gs} and V_{ds}) are apart of the power circuitry. The series-parallel RC circuit acts to both filter high frequency noise and capacitor charge pump to quickly move the voltage from 5 V to 0 V. DVTD occurs when the drain-source voltage begins to fall. This circuit looks similar to the GVTD because this circuit is detecting a similar point as the GVTD circuit, just on the complementary device's drain-source voltage. However, there are a couple of key differences that are designed for. One difference is the *C9* capacitor, from Figure 3.9a, has to block the V_{DC} voltage, which those ceramic capacitors are commercially available. The second difference is the *R16* pull-up resistor, from Figure 3.9a, that is needed to keep the DVTD signal, after the turn-off transition, back at 5 V instead of sitting at a voltage in the middle of 0 V and 5 V. DVFD occurs when the drain-source voltage of the complementary device approaches zero volts. This transient detection circuit is different in that it does not need to transition from 5 V to 0 V until after the complementary V_{ds} signal reaches 0 V, which means the sensing circuit needs to continue blocking the high voltage until it no longer needs blocking. The best way to implement this circuit is through high voltage blocking diodes (similar to the desaturation protection) that can keep the DVFD output at 5 V until the DUT fully turns off.

The simulations conducted to verify these circuits, seen in Figure 3.9, is an expansion of the DPT simulation in Figure 3.3 by adding the detection circuits. The schematic of 3.9a shows a traditional DPT with spice models for the Wolfspeed C2M0080120D. Because the low side SiC device is the active device, Figure 3.9b shows the low-side device turn-off transition. This also means that the detection circuits used and shown in Figure 3.9a are: low-side GVTD, high-side DVTD, and high-side DVFD. It is also worth noting that the GVTD, DVTD, and DVFD signals are sent to a 3-channel inverter IC to become rising-edge *digital* signals used in the edge-detection HRPWM capture in the following section.

3.4 Online Monitoring System

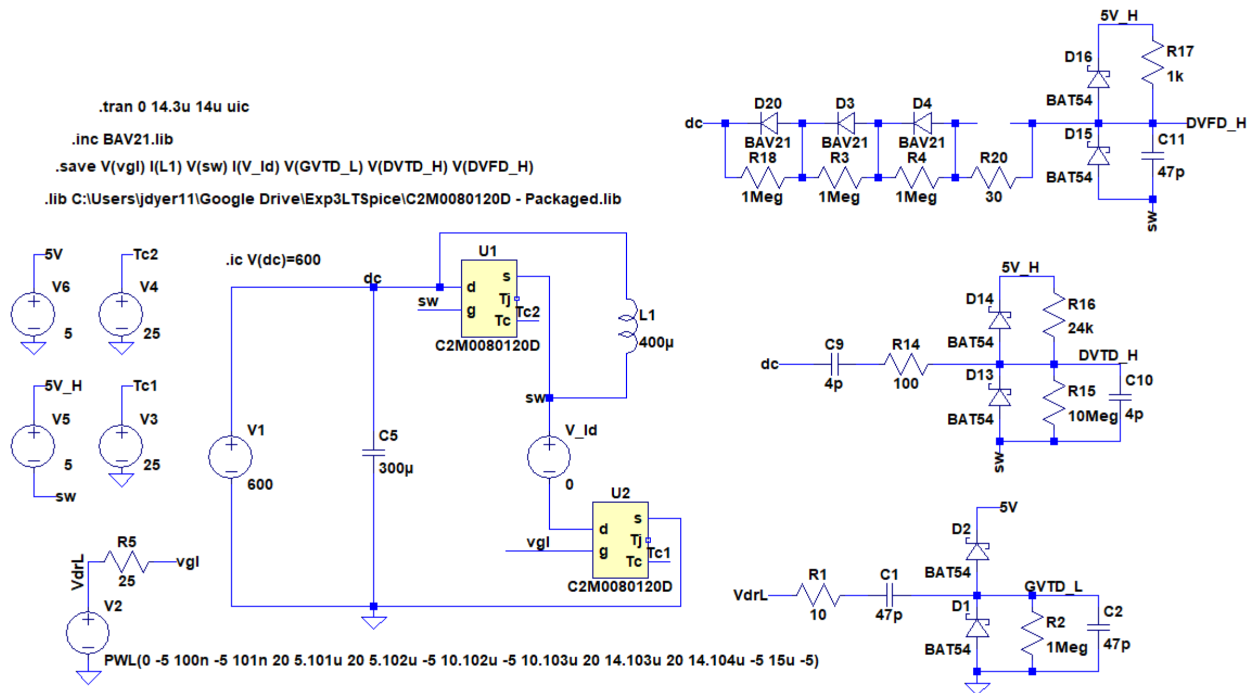
After the detection signals have been generated, those signals, that are now on control-level voltage, need to be captured to record the time between them (i.e. the SiC device turn-off time). This step will involve both the communication between the monitoring boards and the micro-controller (MCU) as well as the data processing on the software side.

3.4.1 PCB Design Overview

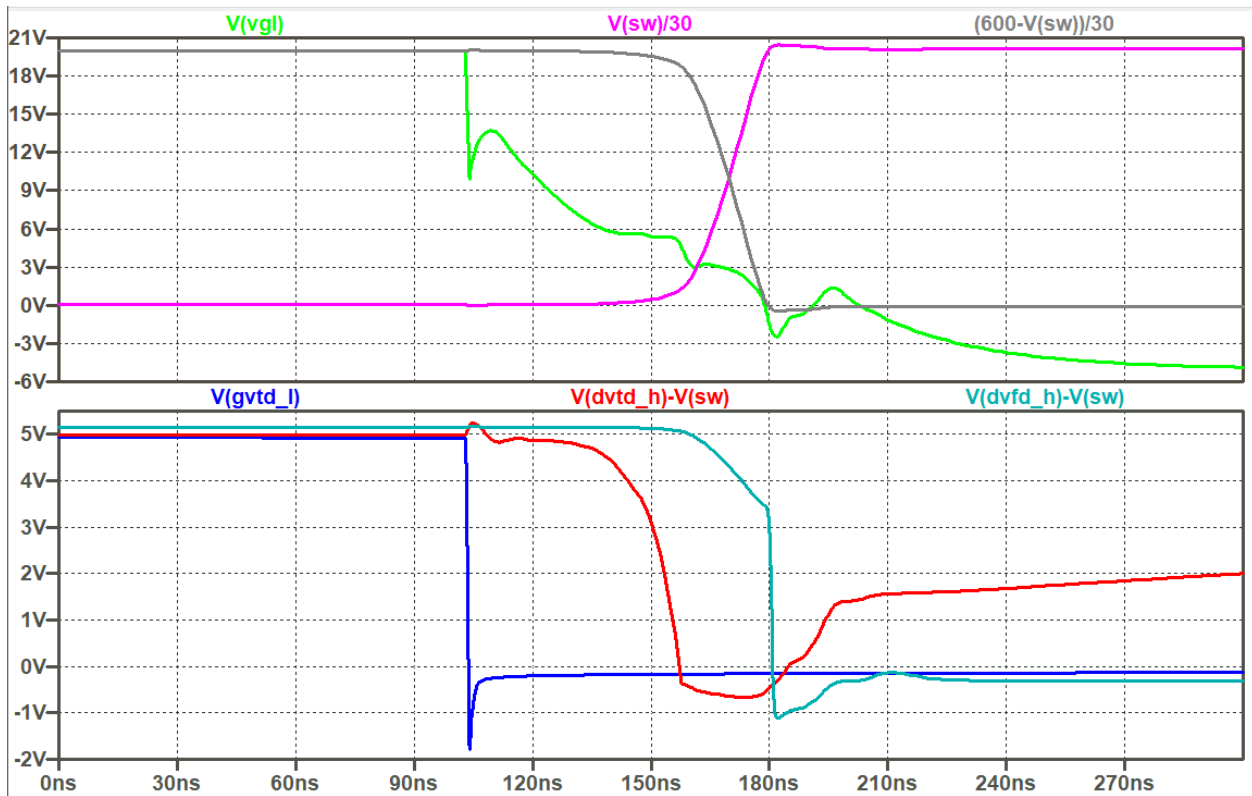
To give context on the circuits designed, the printed circuit board developed for the detection circuits that accompany the gate driver is shown in Figure 3.10. It was designed to have low parasitic connections to both the gate driver and switching device, which helps keep away noise in the signals. It also has a relatively small amount of component addition to the system in terms of size and cost. It is worth noting that the design could have implemented the gate driver board and the time monitoring board together on one board. However, the benefit of implementing the boards separately was isolating the initial debugging of this new circuit.

3.4.2 HRPWM Usage and MCU Connection

Because this design is an online monitoring approach, a processor is needed to continuous collect the data and process the results. The Texas Instruments Delfino TMS320F28335



(a) LTspice Detection Circuit Schematic



(b) LTspice Detection Circuit Waveforms

Figure 3.9: LTspice circuit analysis of the proposed turn-off time transient detectors

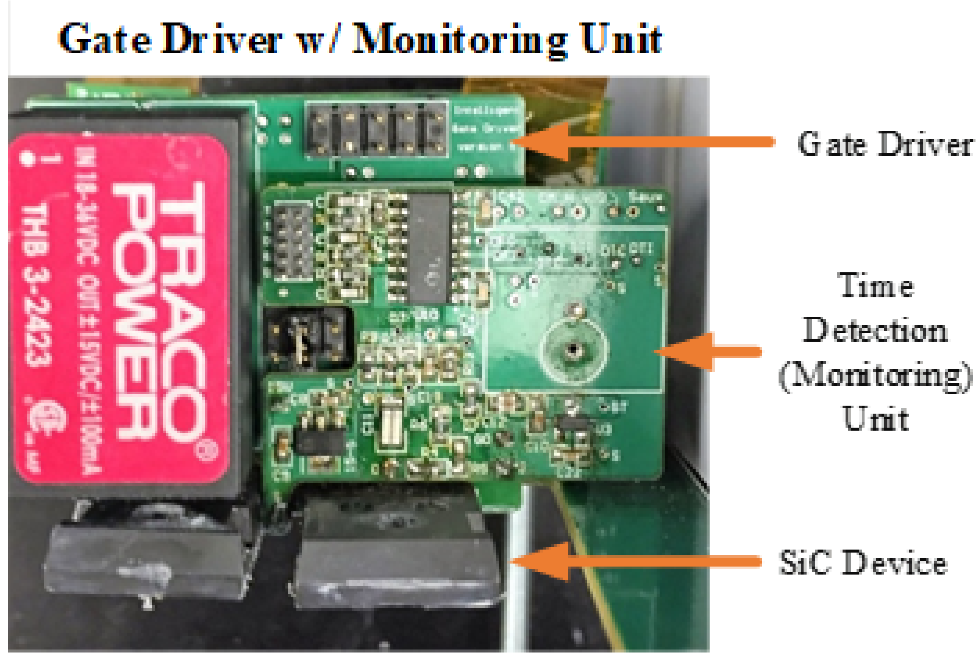


Figure 3.10: Constructed PCB of intelligent gate driver

was selected as the controller to the circuit design. The primary reason for this selection is the High Resolution PWM (HRPWM) feature on this MCU. The HRPWM feature is able to extend the time resolution capability of any of the PWM signal outputs of the MCU. The mechanism behind this ability in based on micro edge positioner (MEP) technology [74], shown in Figure 3.11. MEP logic is capable of positioning an edge very finely by sub-dividing one coarse system clock of a conventional PWM generator. This calculation for the time resolution capability of the HRPWM signal is shown in equation 3.4.

$$t_{HR,step} = \frac{1}{f_{CLK}} \div MEP_{scalefactor} \tag{3.4}$$

Therefore with a max system clock frequency of 150 MHz and a max MEP scale factor of 64, the time step accuracy of the HRPWM signal is on the order of 100 ps and can be set in the software code by the user. This is important because it increases the resolution of the edge-detection scheme used to acquire the nano-second fast turn-off time of SiC. Also, the increased sensing resolution enables less $t_{d,off}$ vs. T_j sensitivity improvement to achieve accurate temperature sensing, which will be discussed more in the implementation in chapter 4.

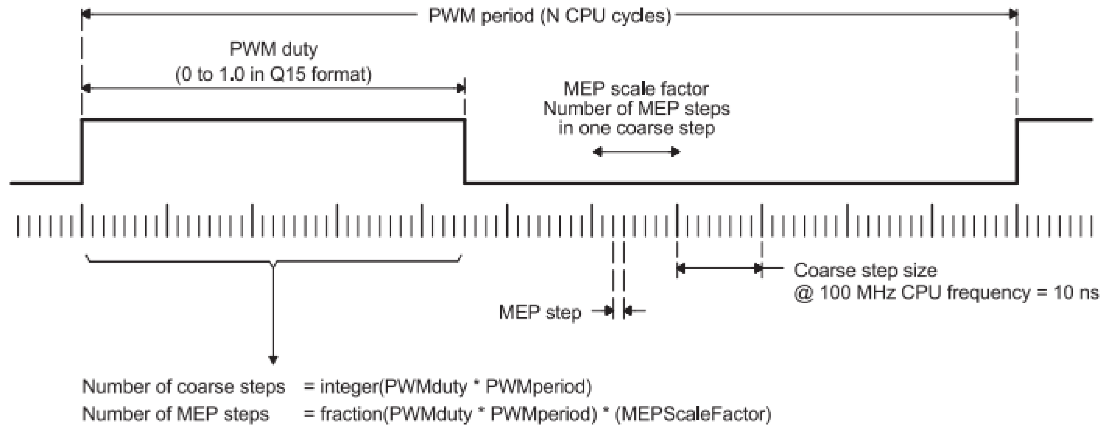


Figure 3.11: Operation logic using the MEP mechanism of HRPWM [74]

Figure 3.12 gives a visual representation of the three timing conditions and the HRPWM signal that captures the times of interest and sends the data back to the micro-controller. This HRPWM signal is labeled s_{aux} because this is the signal fed through isolation into the time detection PCB. It is important to note that propagation delay, shown in Figure 3.12, doesn't affect the sensed switching times. This is because the time of interest is the difference in the shifting time of the HRPWM signal; therefore, this shift from propagation delay will still produce the same monitored data.

The software mechanisms for enabling and processing the sensed switching time are shown in Figure 3.13 as the flowchart overview of the micro-controller code. The input data consists of the variables set initially in the code, GPIO input from the time detection PCB (i.e. gate driver system), and the user-defined LabVIEW data input coming through the serial communications interface (SCI). Assuming the PWMs are enabled from the LabVIEW GUI, the switching cycles are indexed to keep the different switching times within a fundamental cycle logged separately. Then the PWM 1 output, which is used for the gate signals, is set with duty cycle and dead-time specifications. These specifications come from the monitored turn-off time data to both optimize dead-time and compensate output volt-second error, which will be described in detail in section 4.2.

Next, if the monitoring is enabled from the LabVIEW GUI, the GPIO data is called to determine the current positioning of the s_{aux} signal. If a logic 0 is called, then the s_{aux} signal is preceding the edge-detection signal. Therefore, s_{aux} is stepped forward by moving the

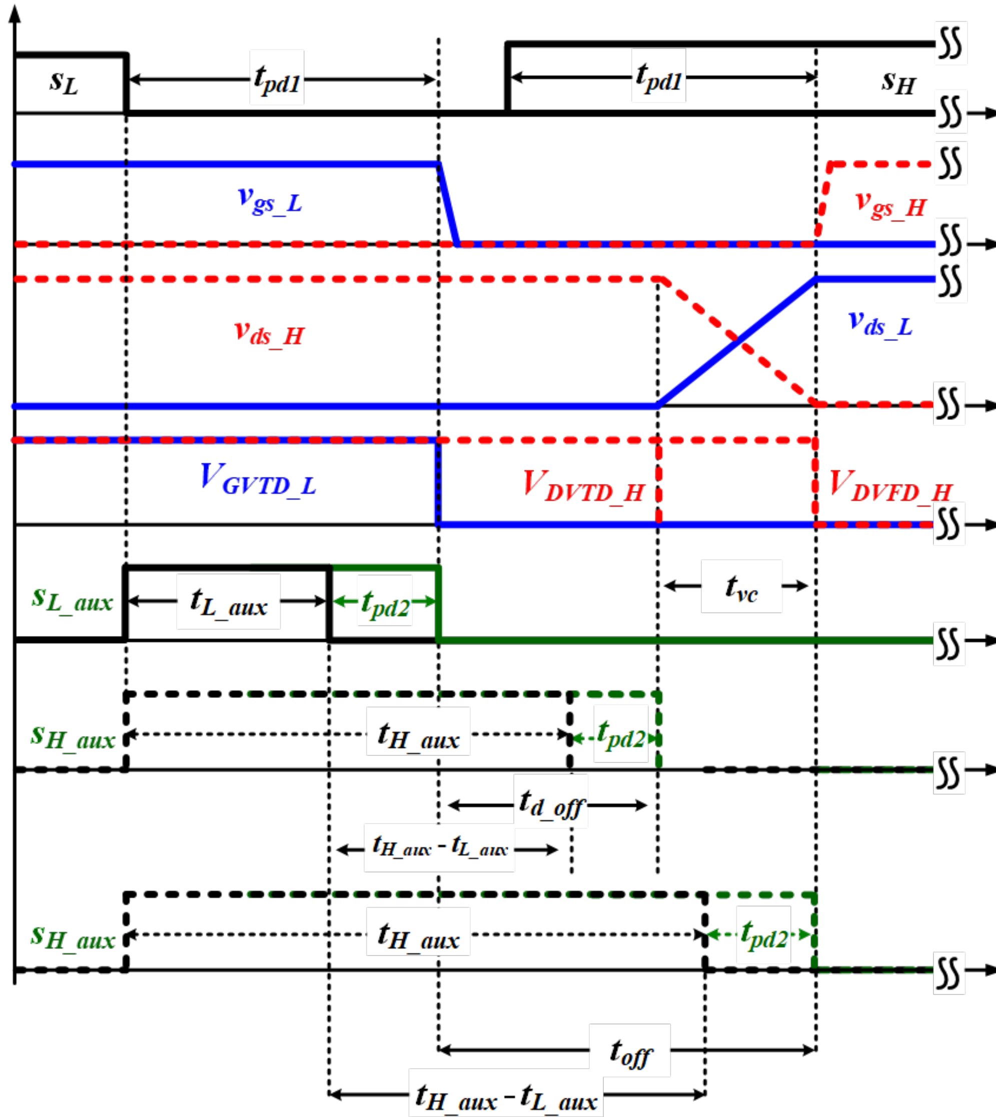


Figure 3.12: Turn-off time edge-detection analysis

comparator of the HRPWM signal in the software. This forward time-movement continues to happen until the HRPWM signal reaches the desired edge-detection signal (i.e. GVTD, DVTD, or DVFD). At this point, the GPIO flag is changed to logic 1 and sent to the controller to indicate moving past the edge-detection signal. This will tell the micro-controller to bring down the comparator of the HRPWM, which will allow for the s_{aux} signal to sense the exact moment of the edge-detection signal with a tolerance of 104 ps.

The time values are obtained inside the micro-controller by taking the change in the PWM comparator value and converting it to real-time in units of nano-seconds. Also, input comes from the LabVIEW GUI on whether to enable gate resistance regulation, which is used for the junction temperature monitoring. Details on this part of the system are given in section 4.4.1.

Another reason for using the Delfino TMS320F28335 was the ability to use the available MCU evaulation board: *eZdsp*, which is shown in Figure 3.14. This helped in making the focus on the ability and accuracy of the data acquisition system. Having to design a controller board would have added extra work and complexity that at this time was not in the scope of the project.

3.4.3 Eliminate Need for Current Sensing

The monitoring system can also be leveraged to indicate load current polarity as shown in Figure 3.15. The concept behind this ability is the different drain-source voltage waveforms for a hard turn-off and soft turn-off. The parameter that can clearly be used to indicate current polarity is turn-off delay time (i.e. the time from the start of the fall of the gate-source voltage to the start of the drain-source voltage rise). This ability to online know the current polarity without a dedicated current sensor turns out to be advantageous for a number of reasons. First, in a VSI application, some form of current sensor is necessary to know the type of switching transition (i.e. hard vs. soft switching) during monitoring. Second, traditional dedicated current sensors struggle to precisely know the load current value during a switching transition (i.e. limited bandwidth). This distinguishes this research work from other dead-time compensation/elimination schemes that deal with the issue of precise current sensing, especially around the zero current crossing. Therefore, this online

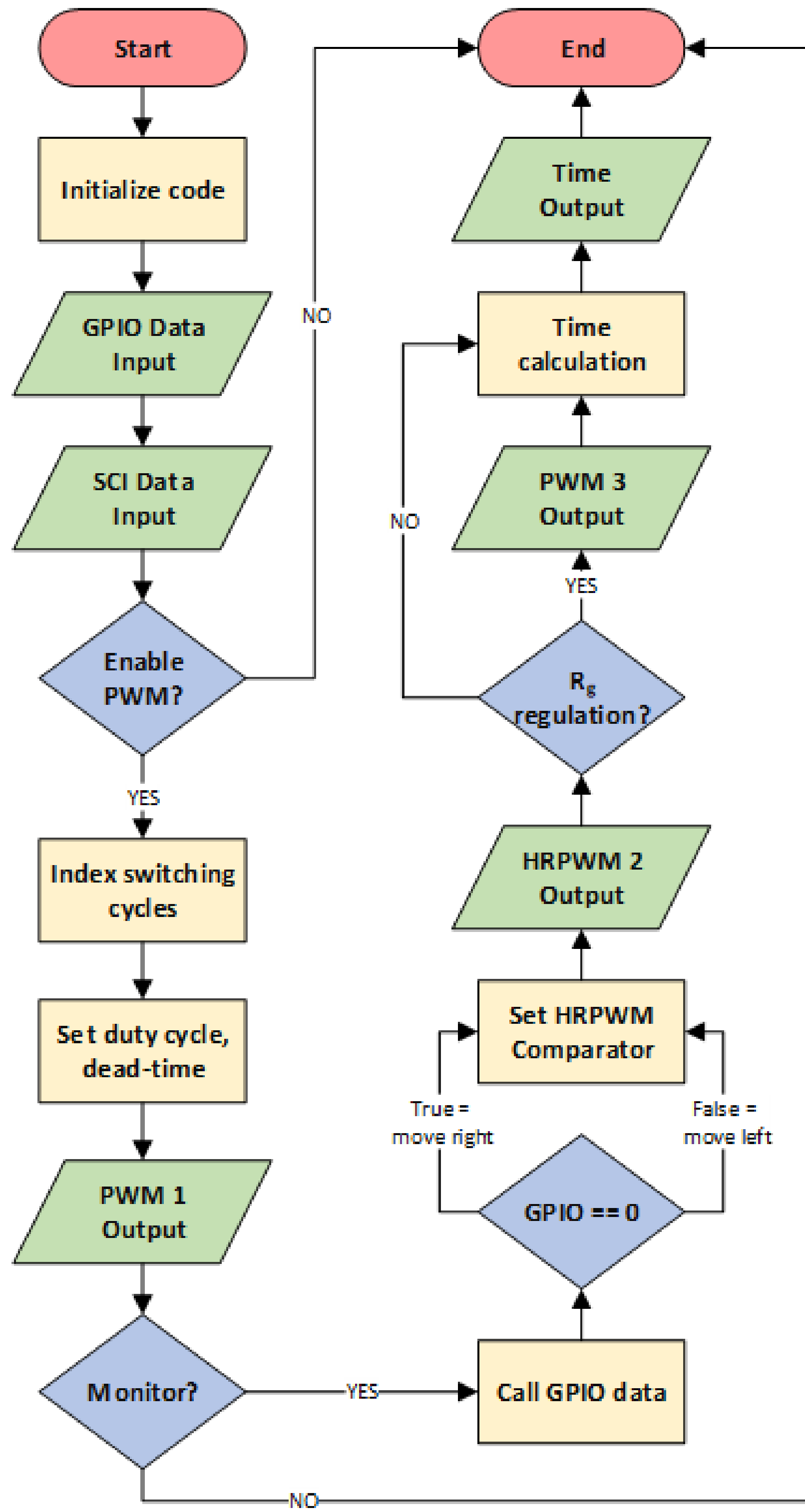


Figure 3.13: Flowchart of the micro-controller code to show inputs and outputs, enable and set PWMs, and the monitoring aspect of moving the HRPWM signal according to capturing the edge signals

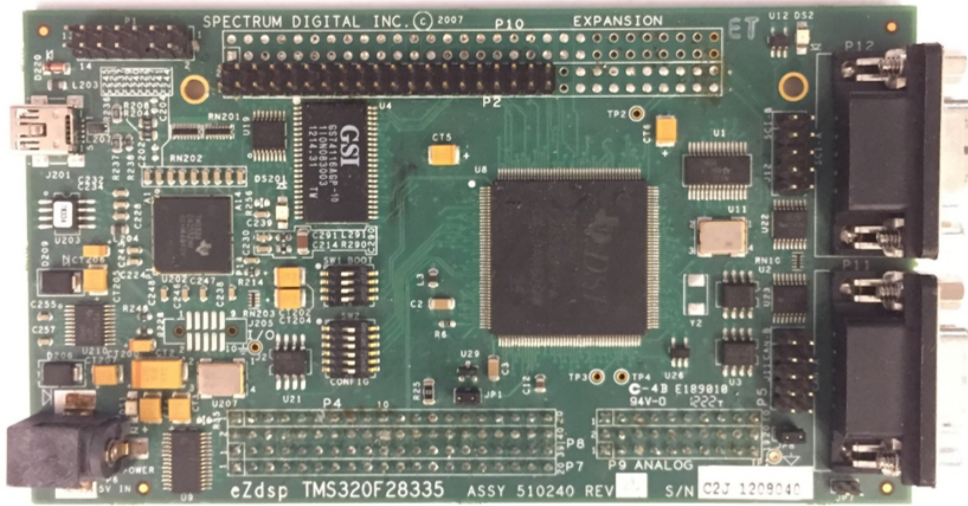


Figure 3.14: $eZdsp^{TM}$ F28335 evaluation board used as project processor

system is able to accomplish multiple tasks, in current polarity sensing and accurate t_{off} monitoring, towards the objective of dead-time control in any VSC.

3.5 Summary

This chapter presented the design of a turn-off switching time monitoring system for SiC devices used in a phase-leg. The monitoring system is set up to online record turn-off delay time, voltage commutation time, and total turn-off time. The conditions (voltage, current, temperature) that affect the switching time are analyzed and the various types of turn-off switching are shown through simulations using the Spice model of the used SiC device: C2M0080120D. For the monitoring system, simple detection circuits are deployed with the gate driver that generate the fast transient edge-detection signals needed to detect the start and end of the times of interest. These circuits work with a micro-controller to process and log the fast switching times in the controller in real-time. The intelligent gate driver system is set up to be used as a junction temperature monitoring and dead-time control system for a voltage-source inverter with results in the next chapter.

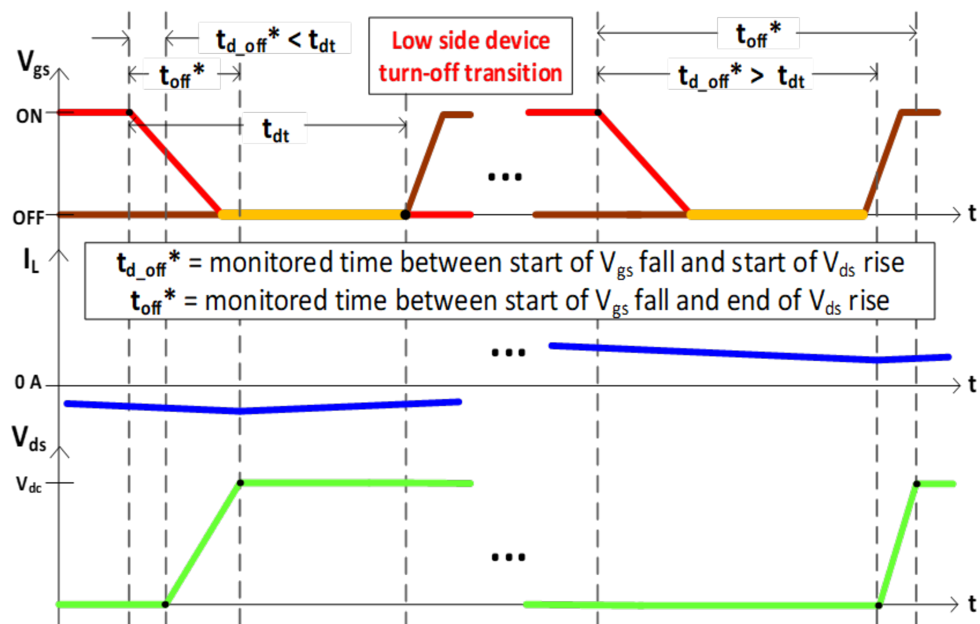


Figure 3.15: Difference in monitored turn-off delay time ($t_{d,off}$) for positive and negative load current which can indicate the two categories for optimized dead-time

Chapter 4

Experimental Verification

4.1 Accuracy of Time Detection

The three timing conditions of turn-off delay time, voltage-commutation time, and turn-off time were successfully monitored for both the low side device and high side device of a phase-leg configuration in both DPT operation and continuous operation. The capability of the high resolution PWM function of TMS320F28335 is fully utilized, which enables the very accurate 0.104 ns capture step. Figure 4.1 shows the process of capturing the three timing conditions in real-time with high sensing resolution. The processed micro-controller results are then compared with the oscilloscope captured waveform results. In comparing the two sets of data, the difference stayed well within a reasonable difference, proving a highly effective monitoring system. Figures 4.2 - 4.4 show the comparison curves for the three timing conditions for the low side device. The orange curve is the data taken from the oscilloscope capture and the blue curve is the data taken from the micro-controller. They are plotted for different load current values and the graphs show the accuracy of the monitoring process. To summarize the three sets of data, all monitored data stayed within $\pm$ 1 % change of the oscilloscope measured switching times. Next, this successful monitoring will be applied to the two converter-level applications: dead-time control and junction temperature monitoring.

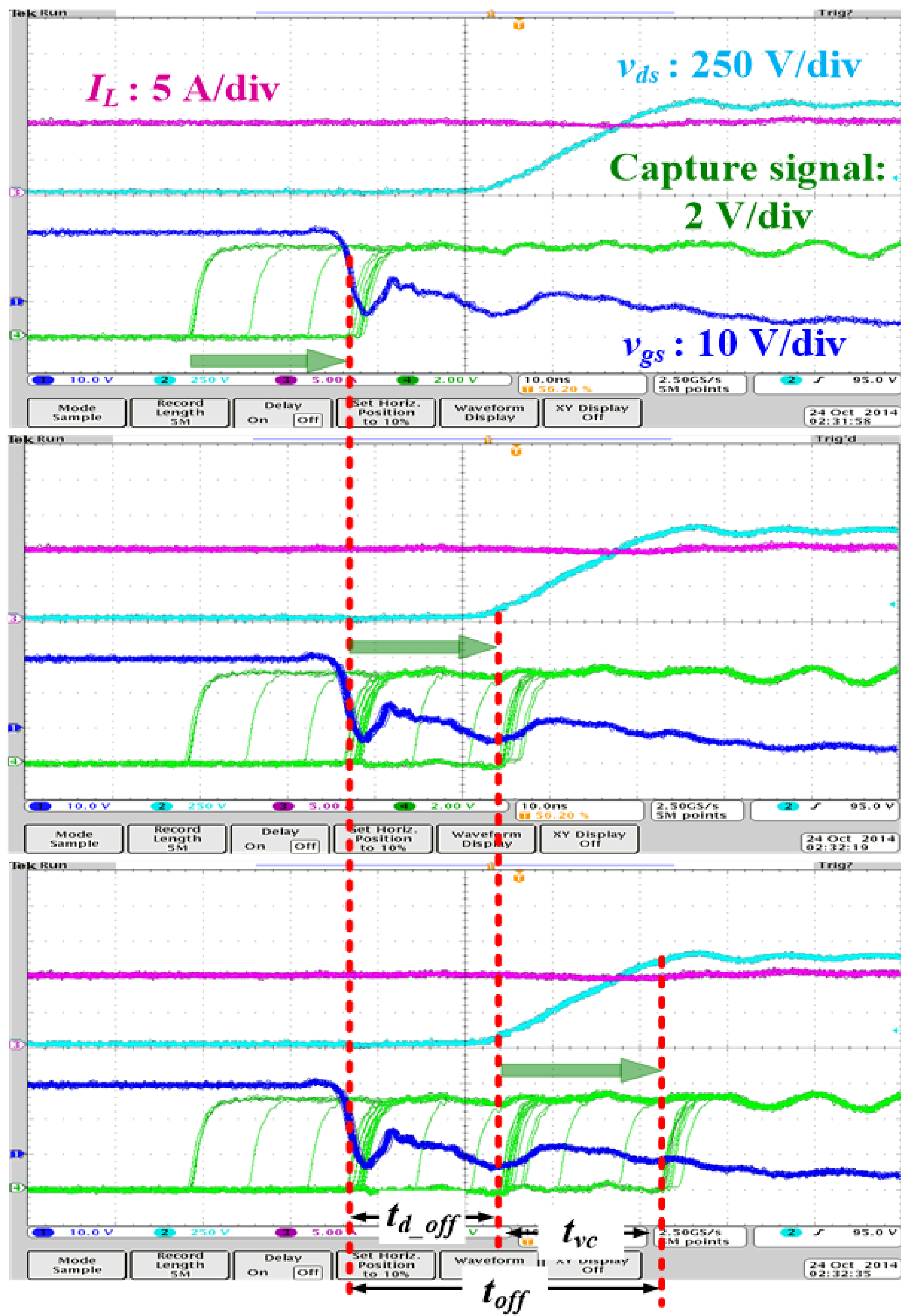


Figure 4.1: Dynamic process of auxiliary logic signals capturing the desired edge of switching voltage

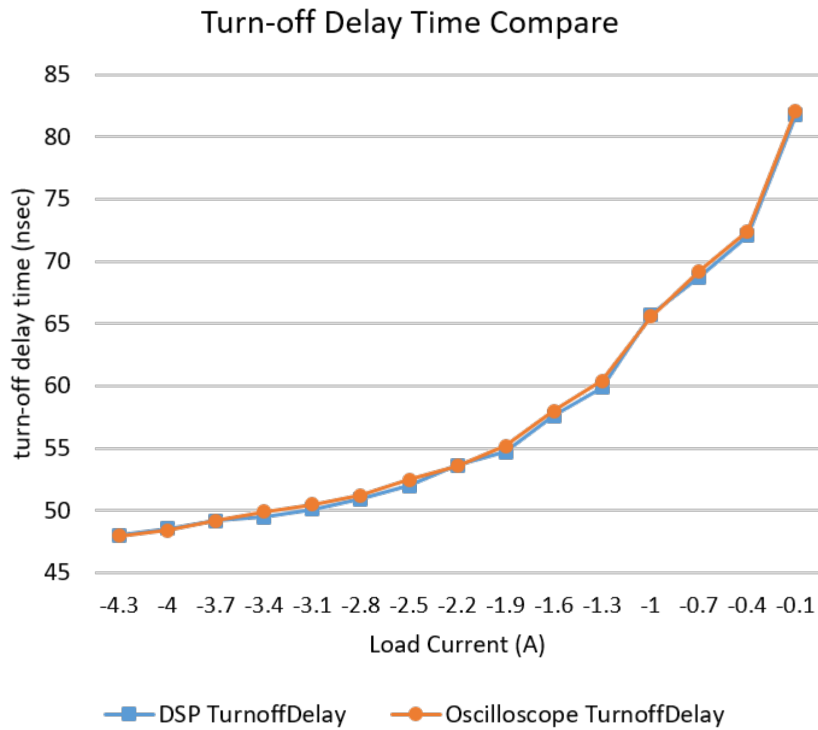


Figure 4.2: Monitored and oscilloscope $t_{d,off}$ data for different inverter load currents

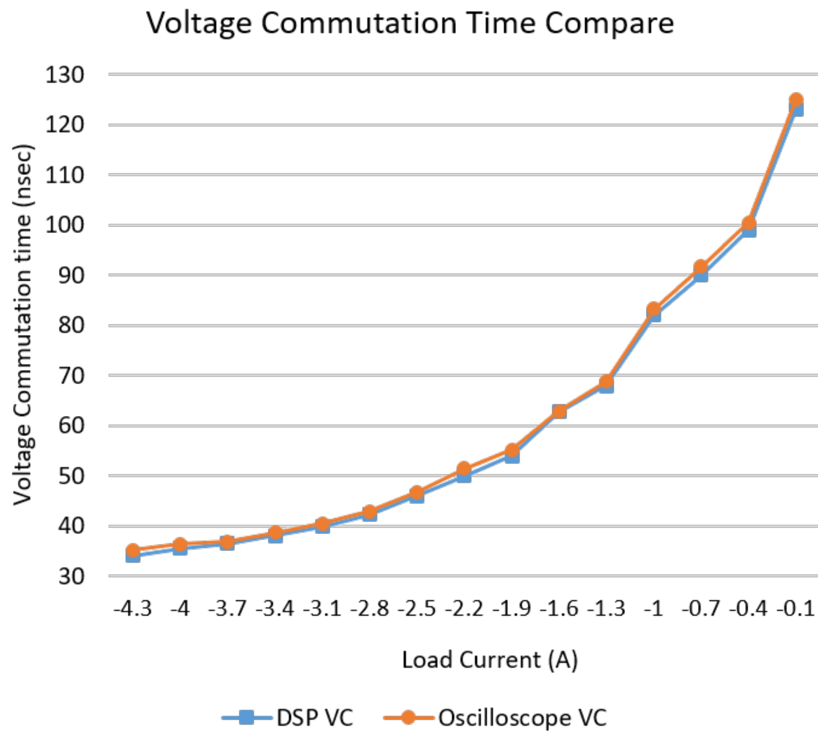


Figure 4.3: Monitored and oscilloscope t_{vc} data for different inverter load currents

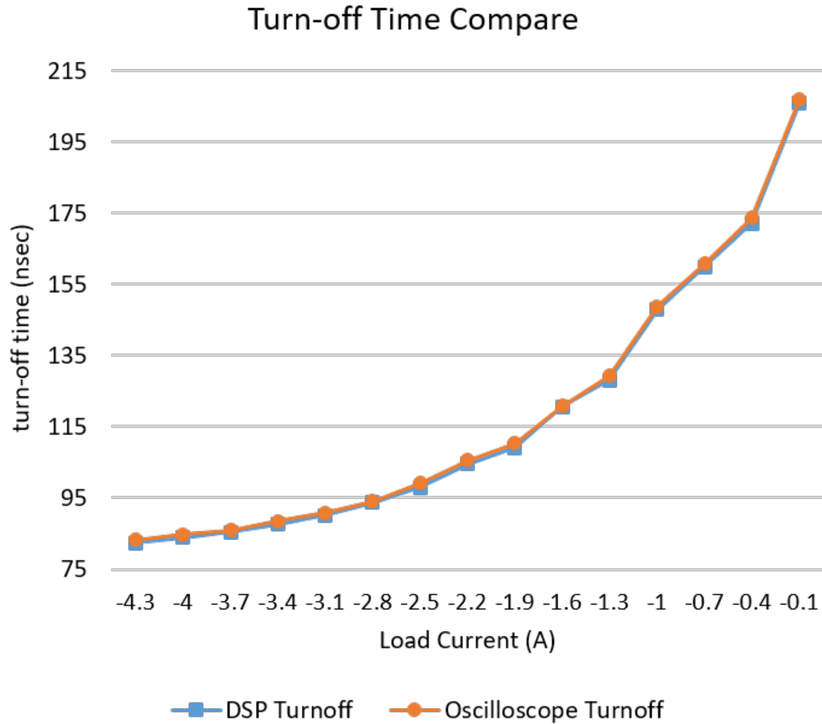


Figure 4.4: Monitored and oscilloscope t_{off} data for different inverter load currents

4.2 Dead-time Optimization

4.2.1 Hardware Setup and Continuous Sensing

To verify the dead-time control, a voltage-source inverter, which needs dead-time implemented to ensure shoot-through safety, is constructed as the converter of interest in this thesis. In deciding the topology of the inverter, it was desired to only have one semiconductor phase-leg, which would simplify the sensing and control to only looking at two devices and only constructing two intelligent gate drivers. Therefore, the half-bridge inverter topology was used with its associated schematic shown in Figure 4.5.

Based on the schematic in Figure 4.5, a 1 kW half-bridge inverter, shown in Figure 4.6, was constructed using two Wolfspeed C2M0080120D SiC devices in a phase-leg configuration. The parameters used in the inverter operation are shown in Table 4.1. The AC load included a 400 H inductor connected to the middle point of the phase-leg as well as a 4.8 μF capacitor and 10 Ω resistor in parallel on the output.

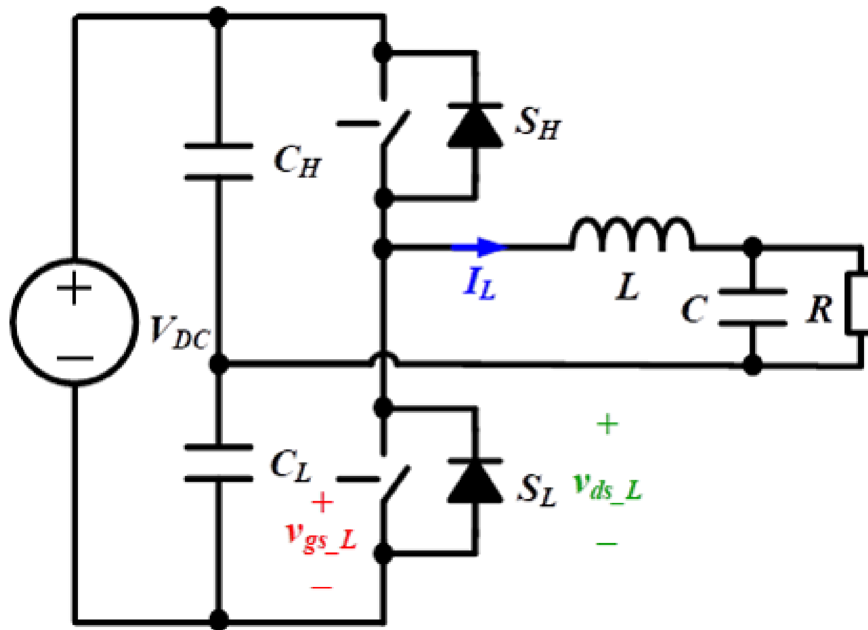


Figure 4.5: Schematic of inductor load based half-bridge inverter with L = 400 μH, C = 4.8 μF, and R = 10 Ω

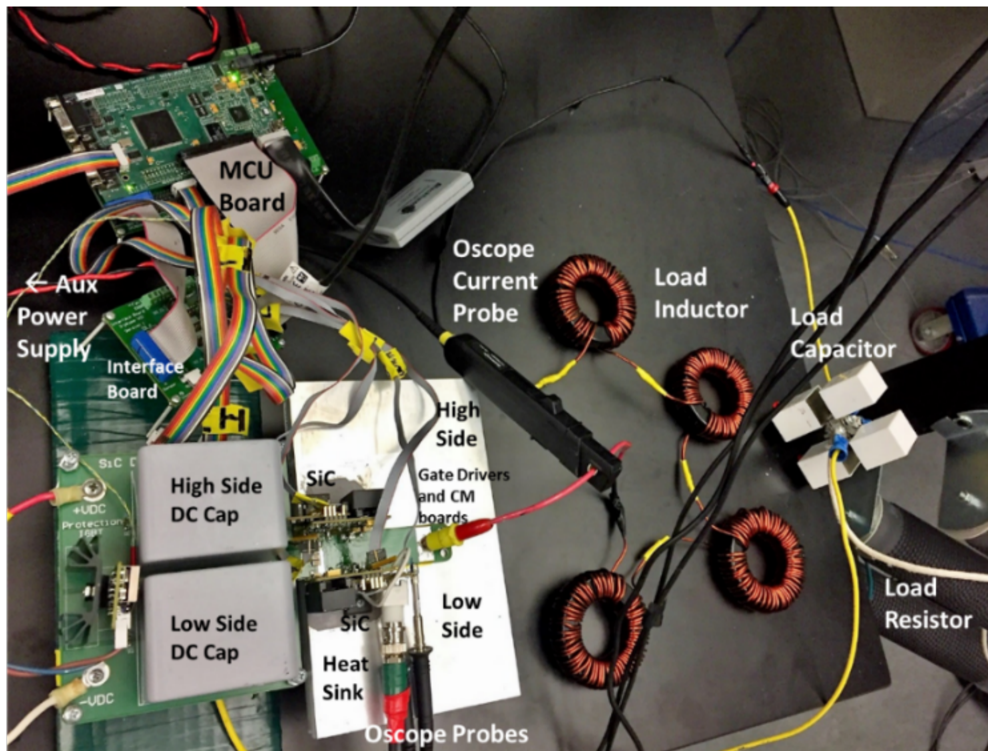


Figure 4.6: 1 kW half-bridge inverter test setup with labeled components

Table 4.1: Half-bridge inverter continuous operation conditions

Operation Parameter	Value
Input Voltage	400 V
RMS Output Current	15 A
Fundamental Frequency	360 Hz
Switching Frequency	50 kHz
Dead-time	500 ns

The inverter successfully operated and the monitoring system accurately captured the turn-off time for the critical switching cycles during inverter operation as shown through an oscilloscope capture in Figure 4.7. This figure used the persistence feature on the oscilloscope to portray the auxiliary signal capturing the end of the turn-off time for multiple switching cycles. The monitored data, processed in the micro-controller, updates the dead-time to the optimized value to increase converter efficiency and reduce power loss in the SiC devices shown in the next section.

4.2.2 Power Loss Results

A summary of the power loss analysis is shown in Table 4.2, where four dead-time situations are tested in the inverter. The related body diode reverse conduction loss is calculated using equation 4.1,

$$P_{diode} = 2V_f I_{rms}(t_{dt} - t_{off}) f_s \tag{4.1}$$

where V_f is the diode forward voltage from the datasheet, I_{rms} is the RMS load current, and f_s is the switching frequency. The partial hard turn-on loss (P_{ps}) is calculated using equation 4.2,

$$P_{ps} = (\frac{-V_1 I_d}{3} t_{sw} + \frac{V_1 I_d}{2} t_{sw}) f_s \tag{4.2}$$

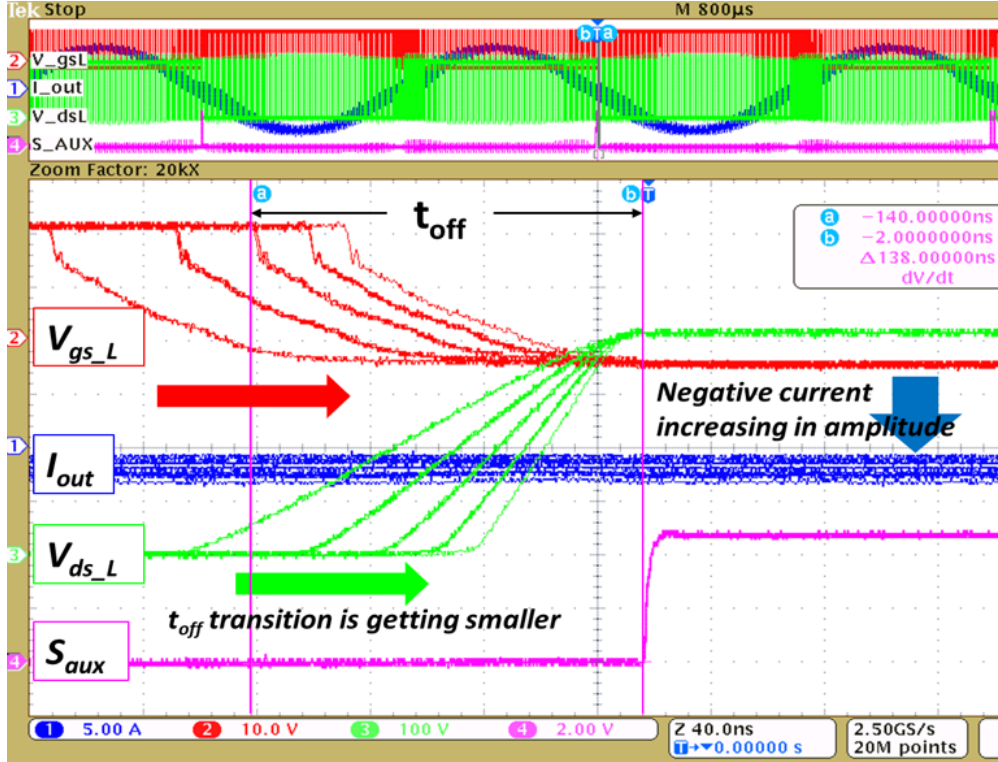


Figure 4.7: Turn-off time monitoring for multiple switching cycles during half-bridge inverter operation

where V_1 is the voltage level of V_{ds} at the time of the partial hard turn-on, I_d is the drain current, and t_{sw} is the switching time. The last column does an energy comparison inside of 1 μs, where the first case is just the reverse conduction energy loss during dead-time and the other cases feature other forms of energy loss less than the reverse conduction loss. E_{ps} is the energy lost from a partial hard turn-on and E_{chan} is the energy lost during the SiC channel conduction. Clearly the dead-time optimization approach presents the best performance and reduces the body diode power conduction loss on the devices by 91% when compared to the 500 ns case.

Table 4.2: Power loss analysis for dead-time implementations on the 1 kW HB inverter

Operation	Body diode reverse conduction loss	Partial hard turn-on loss	Energy loss in 1 μs (E_{dt} + E_{ps} + E_{chan})
Dead-time = 1 μs	2.852 W	0 W	57.04 + 0 + 0 = 57.04 μJ
Dead-time = 500 ns	1.417 W	0.133 W	28.34 + 2.66 + 8.36 = 39.36 μJ
Dead-time = 100 ns	0.08 W	1.06 W	1.6 + 21.2 + 17.14 = 39.94 μJ
Dead-time Optimization	0.1267 W	0 W	2.53 + 0 + 16.57 = 19.1 μJ

4.3 Dead-time Compensation

4.3.1 DTC Algorithm Description

Volt-Second Characterization

Dead-time (t_{dt}) adds voltage distortion at the midpoint of the phase-leg. The ideal midpoint voltage of a phase-leg is meant to mirror the input PWM signal; however, the device parasitic capacitance and non-ideal characteristics of the inductive load along with the previously mentioned deadtime cause the midpoint voltage to become distorted from the input PWM signal. The model for the distorted voltage is shown in detail in Figure 4.8 showing the process from PWM control signals to power semiconductor device switching signals, which includes the effect of dead-time (t_{dt}), propagation delay (t_{pd}), turn on/off delay time ($t_{d,off}$, $t_{d,on}$), voltage rise/fall time or otherwise called voltage commutation time (t_{vc}), and the body diode voltage effect (V_{diode}). Although the voltage distortion process has been evaluated in some previous research, few have considered the non-ideal characteristics of the inductive load and the parasitic capacitance of the switching device, especially a SiC switching device.

Since this work is implementing compensation based on the voltage-second balancing theory, the expressions derived are based upon the voltage-second area lost/gained in each dead-time interval. One assumption made in this work is the cancelling effect that the control-level propagation delays have on the voltage-second area analysis. It can be reasonably assumed the t_{pd} time is the same for each case in the gate driving process. The

derived equations 4.3 - 4.5 will be for the case of current flowing into the midpoint of the phase-leg as shown in Figure 4.8(a). The voltage-second lost/gained for the low side device turn-off transition and corresponding dead-time interval is given in 4.3 and 4.4:

$$VS_{lost,L(-)} = t_{d,offL}V_{DC} + 0.5t_{vc,off}V_{DC} \tag{4.3}$$

$$VS_{gain,L(-)} = V_{diode}(t_{dt} - t_{d,offL} - t_{vc,off}) \tag{4.4}$$

The voltage-second area gained for the high side device turnoff transition and corresponding dead-time interval is given in 4.5:

$$VS_{gain,H(-)} = t_{dt}(V_{DC} + V_{diode}) + t_{d,onL}(V_{DC} + V_{diode}) + 0.5t_{vc,on}V_{DC} \tag{4.5}$$

The derived equations 4.6 - 4.8 will be for the case of current flowing out of the midpoint of the phase-leg as shown in Figure 4.8(b). The voltage-second lost for the low side device turn-off transition and corresponding dead-time interval is given in 4.6:

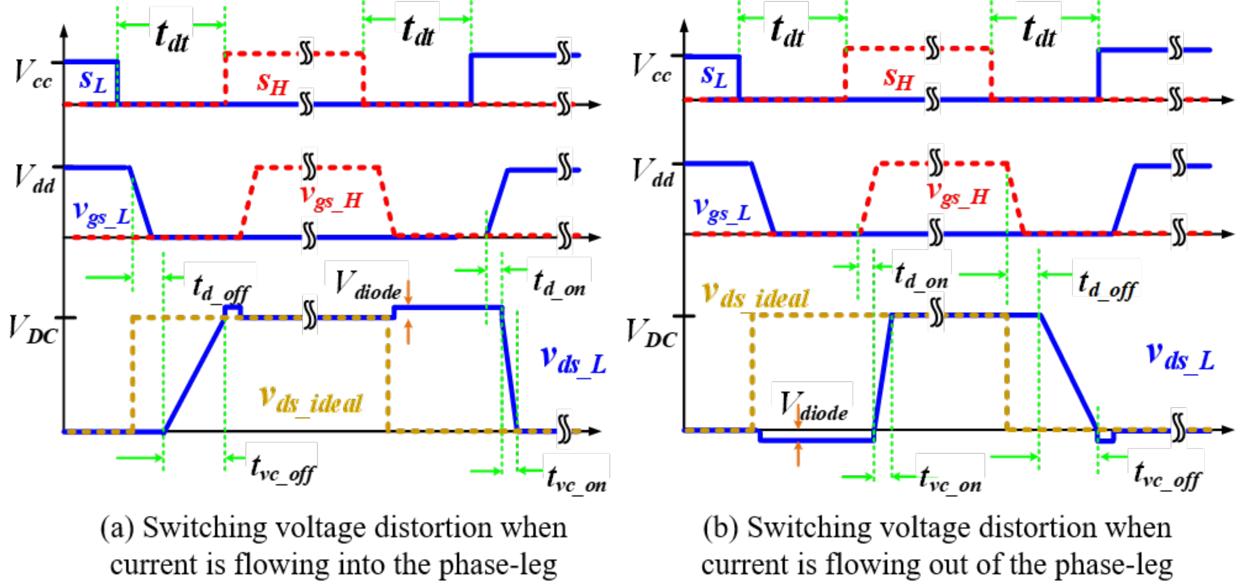
$$VS_{lost,L(+)} = t_{dt}(V_{DC} + V_{diode}) + t_{d,onH}(V_{DC} + V_{diode}) + 0.5t_{vc,on}V_{DC} \tag{4.6}$$

The voltage-second area lost/gained for the high side device turn-off transition and corresponding dead-time interval is given in 4.7 - 4.8:

$$VS_{gain,H(+)} = t_{d,offH}V_{DC} + 0.5t_{vc,off}V_{DC} \tag{4.7}$$

$$VS_{lost,H(+)} = V_{diode}(t_{dt} - t_{d,offH} - t_{vc,off}) \tag{4.8}$$

These equations will serve as the basis for the voltage-second balancing equations detailed and implemented in the following section. Another assumption made in this work because of its small influence is ignoring the effect of a partial hard turn-on at very low currents (i.e. zero-current clamping phenomenon). This work is also able to minimize this phenomenon by setting an initial conservative dead-time in the experimental section.



(a) Switching voltage distortion when current is flowing into the phase-leg

(b) Switching voltage distortion when current is flowing out of the phase-leg

Figure 4.8: Model of phase-leg output voltage distortion and resulting voltage-second error

Processing Data in MCU

Using equations 4.3 - 4.8 and the monitoring system described in section 3.4, this work then creates the micro-controller code to enable this dead-time compensation scheme. The TI TMS320F28335 Delfino MCU is used as the micro-controller, and the SPWM control scheme is used to drive the VSI. The goal of the voltage-second balancing scheme is to adjust the duty cycle for a given switching cycle to better match the control side voltage-second with the abnormal power switching side voltage-second that has been analyzed through equations 4.3 - 4.8. The duty cycle adjustment is done with equation 4.9, which converts the net volt-second gained/lost into a portion of duty cycle that can be added/subtracted to the initial duty cycle for a given switching cycle,

$$d_{comp} = \frac{\Delta VS}{V_{DC}T_s} \tag{4.9}$$

where the net volt-second area is given in 4.10.

$$\Delta VS = VS_{gain} - VS_{lost} \tag{4.10}$$

Then, three switching cycle scenarios are used in the implementation. The first scenario is when the current is flowing into the midpoint of the phase-leg for both dead-time intervals in a switching period. This scenario looks like Figure 4.8(a) and produces the voltage-second area lost/gained of equations 4.3 - 4.5. However, for the implementation, the parameters $t_{d,on}$ and $t_{vc,on}$ are ignored since they are not monitored in the system and are very short time periods. Therefore, when you combine the three equations using 4.10 and then convert the net voltage-second area into a compensated duty cycle value with 4.9, the result is 4.11 that is used in the micro-controller

$$Case1 : d_{comp} = -(\frac{t_{d,offL}}{T_s} + \frac{t_{vc,off}}{2T_s}) + \frac{V_{diode}}{V_{DC}}(\frac{t_{dt}}{T_s} + \frac{t_{d,offL}}{T_s} + \frac{t_{vc,off}}{2T_s}) + (1 + \frac{V_{diode}}{V_{DC}})\frac{t_{dt}}{T_s} \quad (4.11)$$

The second scenario is when current is flowing into the midpoint of the phase-leg for the low side device turn-off but flowing out of the midpoint of the phase-leg during the high side device turn-off (i.e. both cases are hard turn off switching). This scenario is a combination of the hard turn-off parts of Figure 4.8(a) and (b) and uses the voltage-second area calculations of 4.3, 4.4, 4.7, and 4.8. In this scenario, no parameters are ignored as this work captures all the time conditions in this case. Therefore, as before the resulting compensated duty cycle is shown in 4.12.

$$\begin{aligned} Case2 : d_{comp} = (\frac{t_{d,offH}}{T_s} + \frac{t_{vc,offH}}{2T_s}) - \frac{V_{diode}}{V_{DC}}(\frac{t_{dt}}{T_s} + \frac{t_{d,offH}}{T_s} + \frac{t_{vc,offH}}{2T_s}) \\ -(\frac{t_{d,offL}}{T_s} + \frac{t_{vc,offL}}{2T_s}) + \frac{V_{diode}}{V_{DC}}(\frac{t_{dt}}{T_s} + \frac{t_{d,offL}}{T_s} + \frac{t_{vc,offL}}{2T_s}) \end{aligned} \quad (4.12)$$

The third scenario is when current is flowing out of the midpoint of the phase-leg for both dead-time intervals in a switching period. This scenario resembles the switching waveforms shown in Figure 4.8(b). Similar to the first scenario, the $t_{d,on}$ and $t_{vc,on}$ parameters are ignored. Therefore, the compensated duty cycle value calculated based on 4.6 - 4.10 yield the expression shown in 4.13.

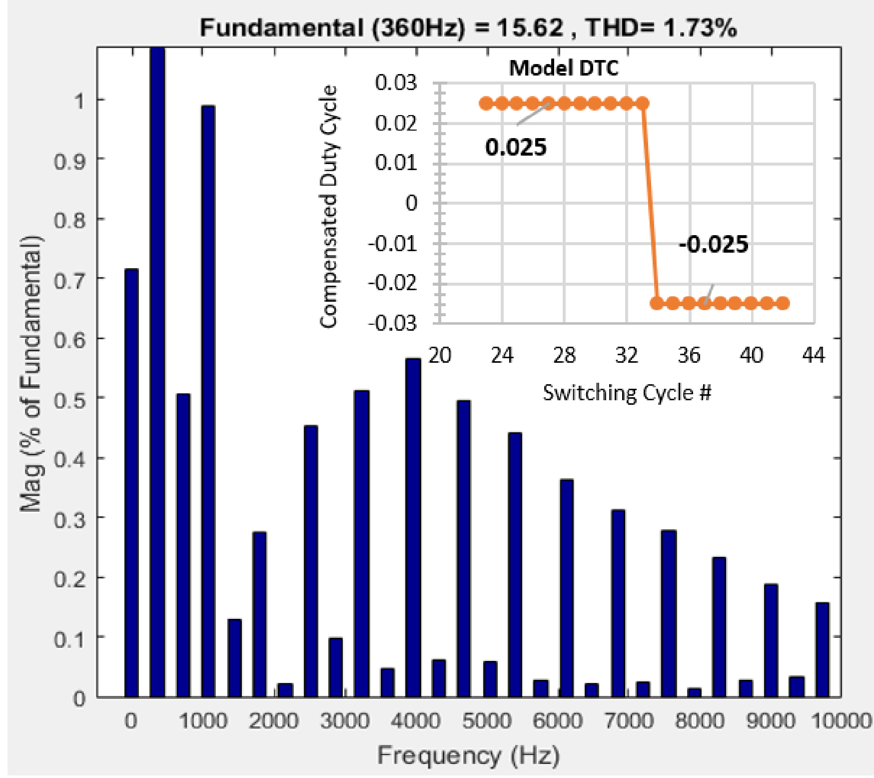


Figure 4.9: Model-based compensation approach considering t_{dt}

$$Case3: d_{comp} = (\frac{t_{d,offH}}{T_s} + \frac{t_{vc,off}}{2T_s}) - \frac{V_{diode}}{V_{DC}}(\frac{t_{dt}}{T_s} + \frac{t_{d,offH}}{T_s} + \frac{t_{vc,off}}{2T_s}) - (1 + \frac{V_{diode}}{V_{DC}})\frac{t_{dt}}{T_s} \quad (4.13)$$

4.3.2 Output Current FFT Results

To analyze the power quality improvements from this voltage-second matching, the 1 kW half-bridge inverter output current was obtained under four different conditions: no compensation, classic dead-time model-based compensation, improved model-based compensation, and full monitor-based compensation. The current fundamental value and THD improvement results for the three compensation schemes are shown in Figure 4.9 - 4.11.

Table 4.3 shows the incremental improvement towards the ideal VSI case with each dead-time compensation scheme with the proposed scheme giving the best results. The reason for including the fundamental current value is voltage-second balancing mainly corrects

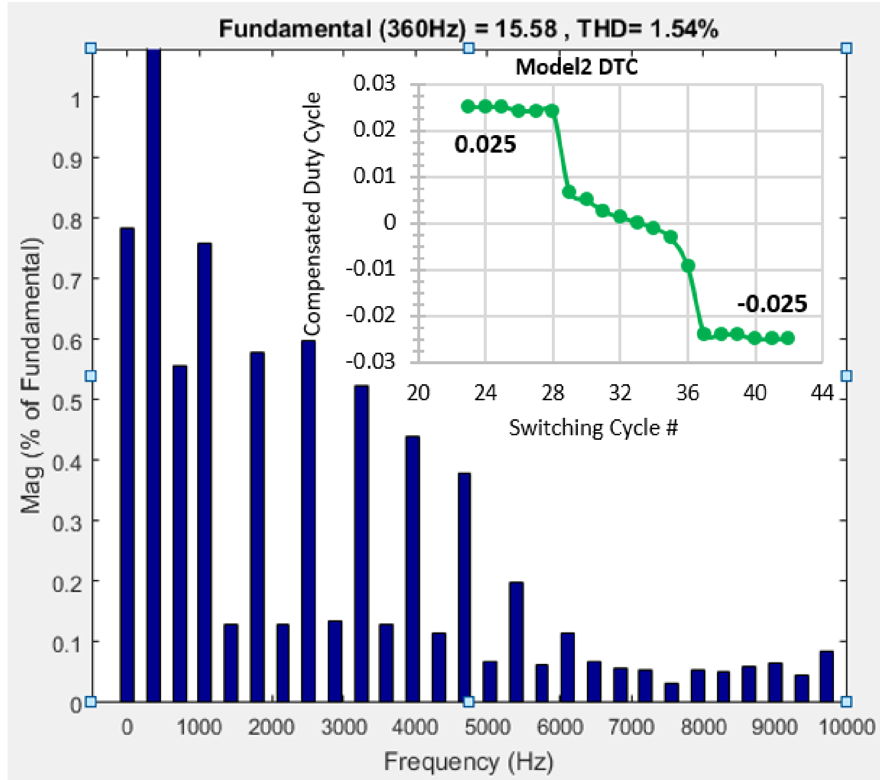


Figure 4.10: Model-based compensation approach considering t_{dt} and t_{vc}

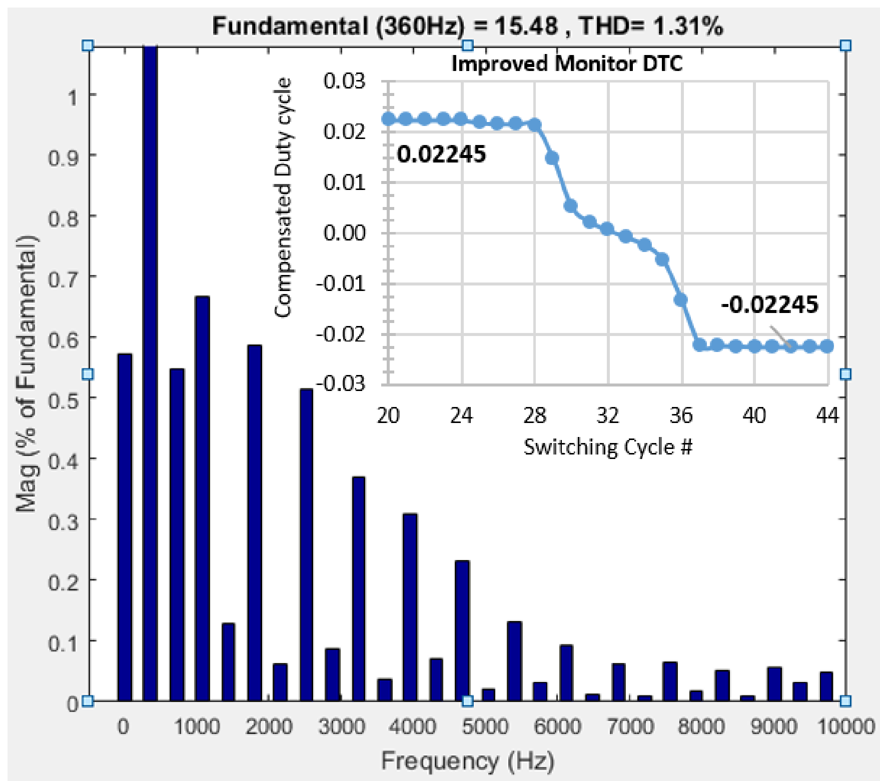


Figure 4.11: Monitor-based compensation approach considering t_{dt}, t_{vc}, and $t_{d,off}$

Table 4.3: Experimental results for output current characteristics of half-bridge inverter under different DTC conditions

	Ideal VSI	No DTC	Model 1 DTC	Model 2 DTC	Monitor DTC
Fundamental Value	15.24 A	14.42 A	15.62 A	15.58 A	15.48 A
THD	0%	3.3%	1.73%	1.54%	1.31%

average voltage/current error, which in turn would improve the fundamental voltage and current values closer to the ideal case. The classic model-based approach only considers the dead-time effect on the volt-second error and needs a precise current sensing to know the current polarity. The newer model technique only considers the t_{vc} effect around the current zero-crossing along with the dead-time effect. The full monitoring technique considers the $t_{d,off}$, t_{vc}, and t_{dt} effect for the full fundamental cycle. The graph inside each chart is the compensated duty cycle values used around the current zero-crossing. Also, the charts are zoomed in to show the reduction in the low frequency harmonics around the fundamental frequency.

4.4 TSEP Application

As mentioned in Section 3.2.1, the monitored turn-off delay time is used to indicate the SiC device's T_j. This is done by increasing the time's sensitivity to T_j, calibrating its relationship to temperature, and then operating the device continuously to verify the data. The following sections will show the results obtained for this approach.

4.4.1 Regulation of Gate Resistance

The sensitivity of turn-off delay time with respect to junction temperature can be improved by increasing the value of the gate resistance (R_g) or input gate-source capacitance (C_{gs}). Increasing R_g or C_{gs} causes the slew rate of the gate voltage to decrease (i.e. the transfer curves of Figure 3.2 become more separated from each other), which causes the change in turn-off delay time to be greater as junction temperature rises. This sensitivity enhancement is shown in Figure 4.12, where the simulated DPT from Figure 3.3 was run for the SiC device

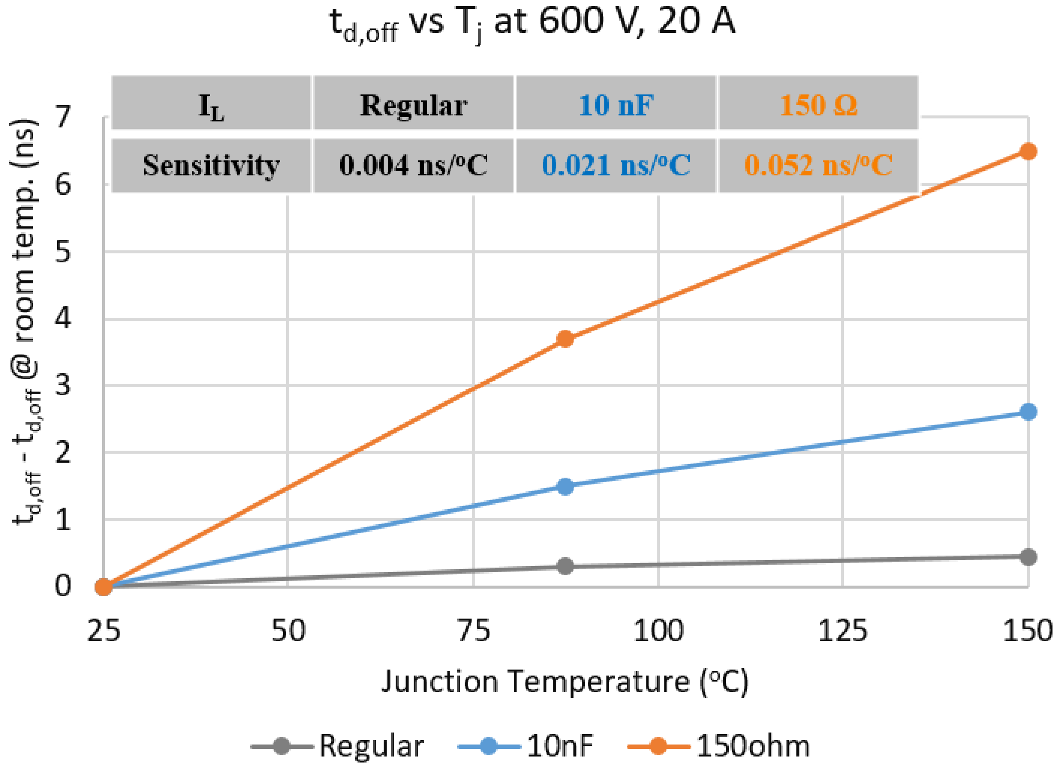


Figure 4.12: C2M0080120D SiC T_j sensitivity enhancement from $R_g = 150\ \Omega$ and $C_{gs} = 10$ nF

at 600 V and 20 A at varying temperature and varying R_g or C_{gs}. Also, note that the turn-off delay time has a positive coefficient with temperature so the $t_{d,off}$ values increased as temperature increased.

Needing to alter a gate driver parameter that slows down the switching is not ideal, causing higher switching losses. However, complementary circuitry can be added to the overall monitoring system to change the chosen parameter only during the turn-off transition where the monitoring takes place. In typical converter operation, temperature data isn't needed on a switching frequency sampling rate; therefore, only altering the gate driver parameter for one turn-off transition throughout the fundamental cycle is an adequate temperature sensor. This, in turn, keeps the switching losses added to the devices to be negligible. The details of the designed regulation system are shown in the following section.

Also, the decision needs to be made whether to use a R_g or C_{gs} regulation system. Implementing a R_g regulation system proved to be a better option for multiple reasons.

One, the sensitivity increases more for the R_g regulation option. Two, though both implementations would add minimal switching losses, implementing the C_{gs} regulation system would also add gate driver losses shown in equation 4.14, where gate charge (Q_g) of the power device depends on input capacitance.

$$P_{drv} = Q_g V_{DD} f_s \tag{4.14}$$

Grounding Issue

The circuit designed for the R_g regulation system is shown in Figure 4.13. It was desired to have the option to choose between a normal gate resistor (i.e. 10 Ω in this case) and the resistor for enhanced temperature sensitivity. The best way to implement this ability of two different gate resistors is by having a *switch* (using a MOSFET). One issue with trying to add a switch in the gate drive loop is the source of the MOSFET. To be able to drive the gate-source voltage of the MOSFET above the threshold voltage, the gate driver (i.e. using T.I. LM5114) must be sourced to the main SiC gate driver output voltage. This scheme is similar to the gate driver for the phase-leg high-side SiC device, where the source of that device in the mid-point that switches from a low potential to a high potential. The simulation results of Figure 4.14 show the correct functionality to regulate the gate resistance for a turn-off transition.

4.4.2 Temperature Calibration

A DPT environment is constructed to obtain accurate $t_{d,off}$ vs. T_j curves. The hardware assembled is shown in Figure 4.15. This setup enables the ability to tune the junction temperature of the device by setting the hot plate temperature. This is achieved because there is minimal power loss in a DPT so the hot plate temperature can be assumed to also be the junction temperature, especially by screwing the SiC devices to a copper block that sits on the hot plate, which removes any gaps in the thermal path.

Then the relationship between turn-off delay time and junction temperature is obtained under different load currents. The MCU sends the input PWM with according pulse width

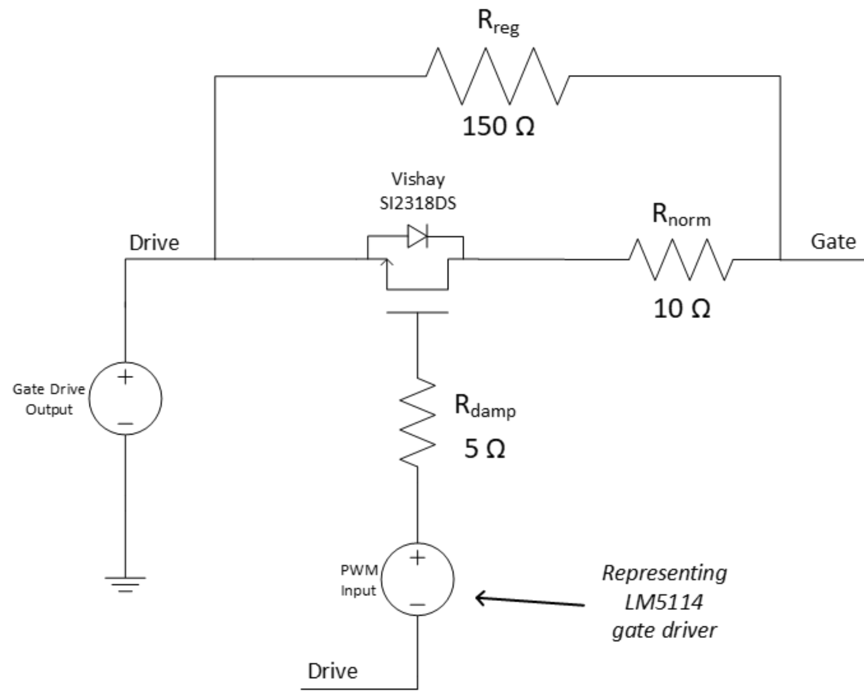


Figure 4.13: R_g regulation schematic incorporated in monitoring system design

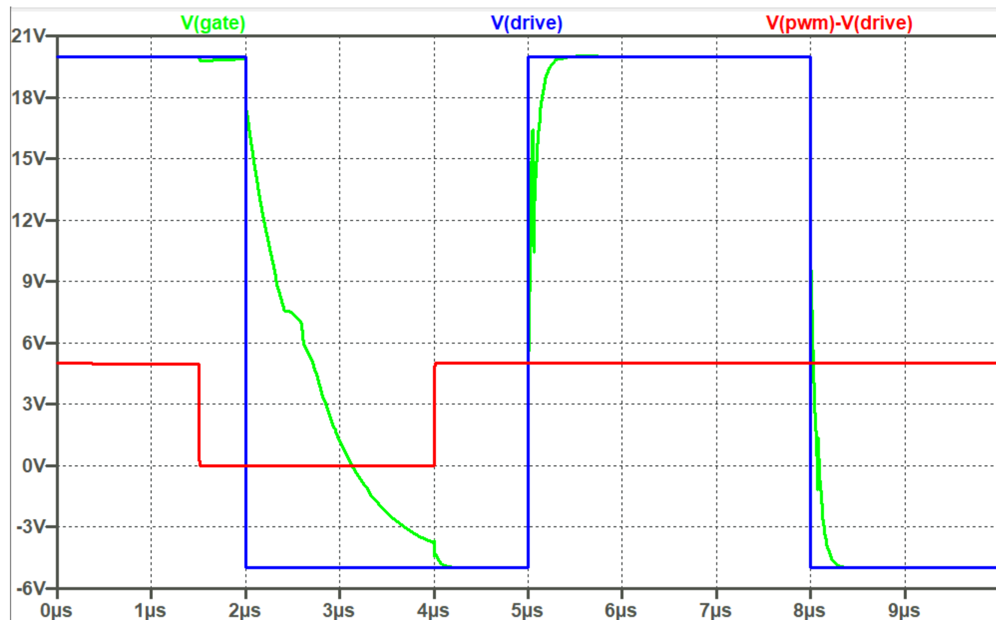


Figure 4.14: R_g regulation verification through LTspice for turn-on and turn-off

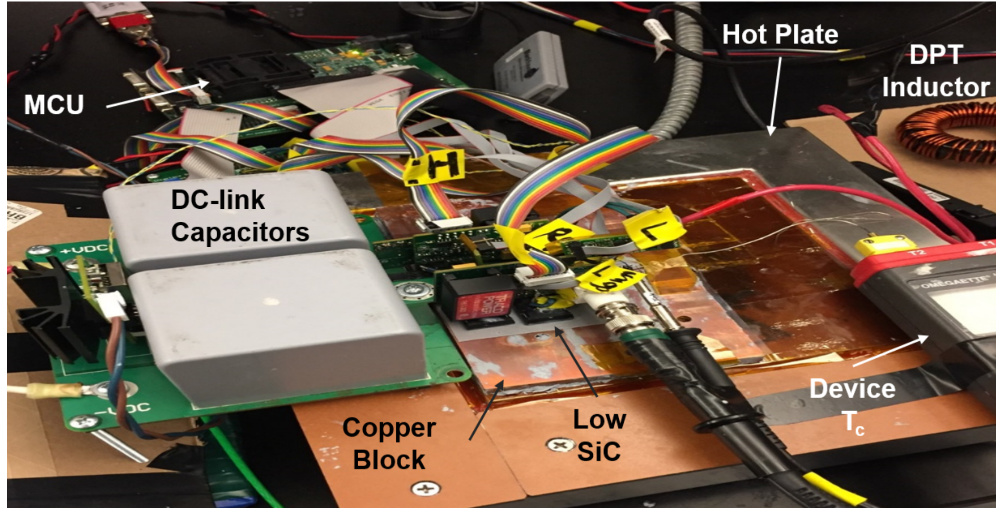


Figure 4.15: Hardware setup for DPT calibration

for setting the current level and receives back the monitored $t_{d,off}$. Figure 4.16 illustrates the calibration curve of the lower switch in the phase-leg. In this case study, the gate resistance regulation (GRR) assist circuit is employed. Due to the large gate resistance during the online junction temperature measurement, the sensitivity improves from tens of ps/°C to hundreds of ps/°C (see Figure 3.4 versus Figure 4.16).

Additionally, two sets of data are illustrated in Figure 4.16: one comes from the micro-controller (i.e., DSP in this case study) based on the online turn-off delay time monitoring (solid line); the other is based on the oscilloscope capture (dashed line), which should be the accurate results and is considered the benchmark. It shows in Figure 4.16 that the results obtained by the proposed turn-off delay time measurement are almost identical to the results directly read from the oscilloscope.

Figure 4.17 illustrates the calibration curve of the upper switch in the phase-leg. It can be observed that the coefficients of the calibration curve for the upper switch in Figure 4.17 are different than that of the lower switch in Figure 4.16, which indicate the mismatch between lower and upper SiC devices. Also, it shows the necessity of the separated calibration per device.

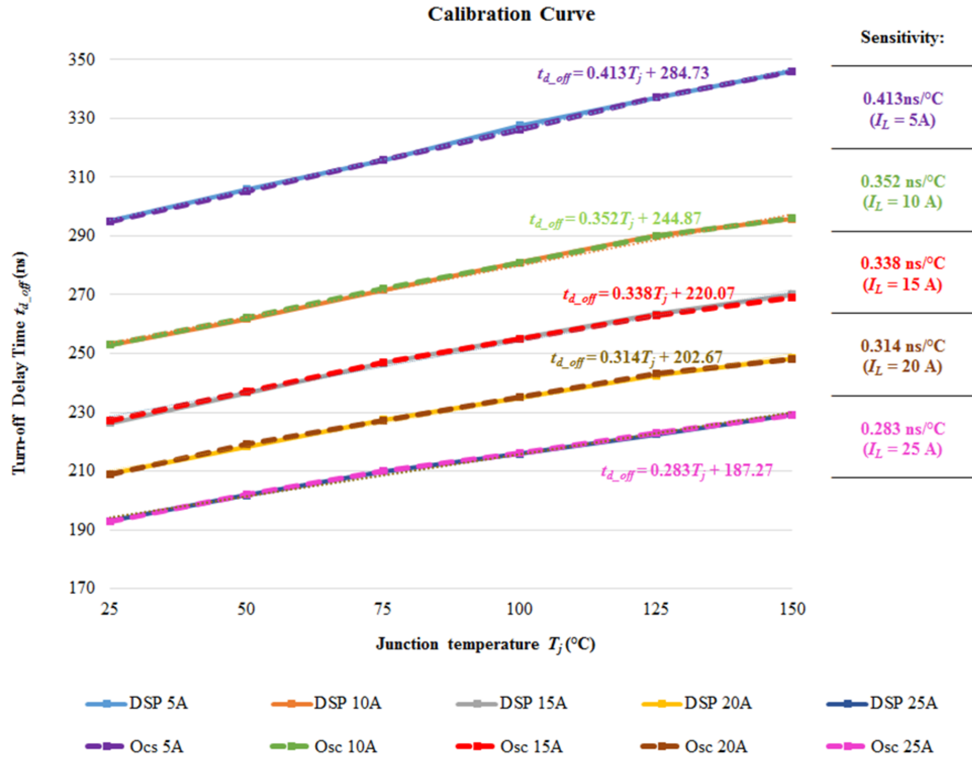


Figure 4.16: Calibration curve of the lower switch under V_{DC} of 600 V with R_g of 150 Ω with verification from oscilloscope

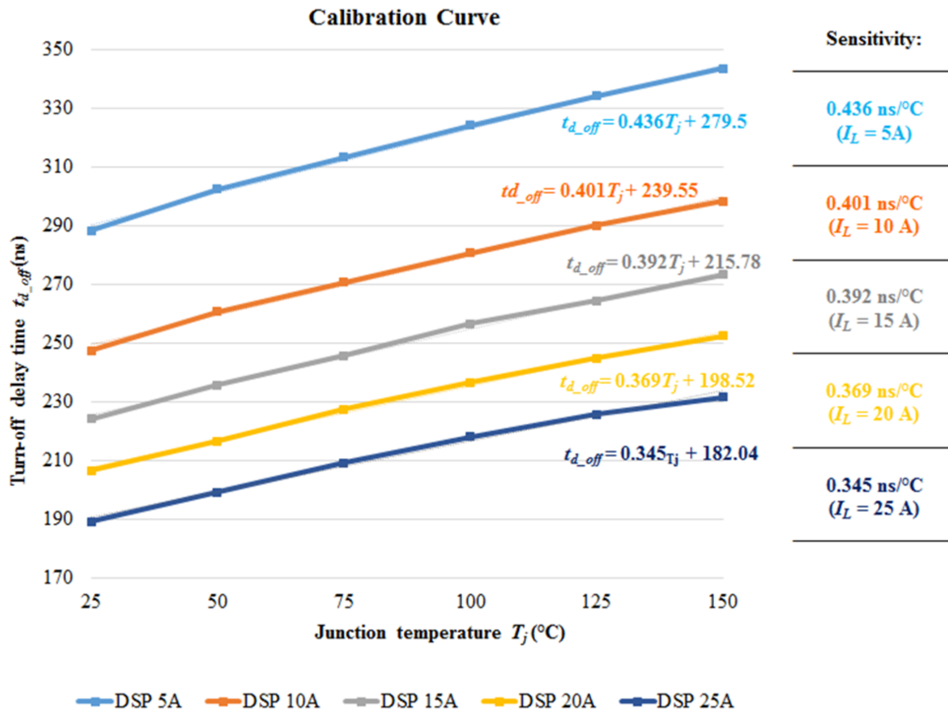


Figure 4.17: Calibration curve of the upper switch under V_{DC} of 600 V with R_g of 150 Ω

4.4.3 Continuous Operation T_j Sensing

The same half-bridge inverter hardware from Figure 4.6 is used for the experimental verification of the proposed online junction temperature monitoring system in a continuous operation environment. The only difference in operation is the DC input voltage is increased from 400 V to 600 V. This allowed the SiC devices to be more thermally stressed to see the monitoring capabilities at higher junction temperature.

Figure 4.18 and Figure 4.19 show the oscilloscope capture of the half bridge inverter, including gate-source voltage of the lower switch $v_{gs,L}$, drain-source voltage of the lower switch $v_{ds,L}$, load current I_L, and auxiliary capture signals s_{aux}. In this case study, during each fundamental cycle, the online junction temperature monitoring is activated, enabling the GRR assist circuit and generating the auxiliary capture signal for turn-off delay time monitoring of both lower and upper switches in the phase-leg configuration. Note that in practice, it is not necessary to update junction temperature for each fundamental cycle. Thus, the adverse effect of the GRR assist circuit on the converter performance is negligible.

The monitored $t_{d,off}$ data is processed in the micro-controller and internally compared to the calibration curve to produce the junction temperature of each device. Referring to the calibration curves of Figure 4.16 and Figure 4.17 based on $I_L = 22.5$ A at the time of the acquisition, the corresponding low side and high side device junction temperatures are 121 °C and 115 °C, respectively. Based on converter operation and thermal layout with heatsink, this temperature data is sufficient in indicating the internal device temperature.

4.5 Discussion

4.5.1 T_j Measurement Accuracy

As shown in Figure 4.16, if a GRR assist circuit with gate resistance of 150 Ω is employed, the sensitivity of the turn-off delay time on the junction temperature is improved to be $>$ 0.28 ns/°C. Meanwhile, considering achievable 0.104 ns capture resolution using the high resolution PWM function of TMS320F28335, the measurement error of the proposed system is less than 0.5 °C. Practically, due to the propagation delay distortion/mismatch and jitter

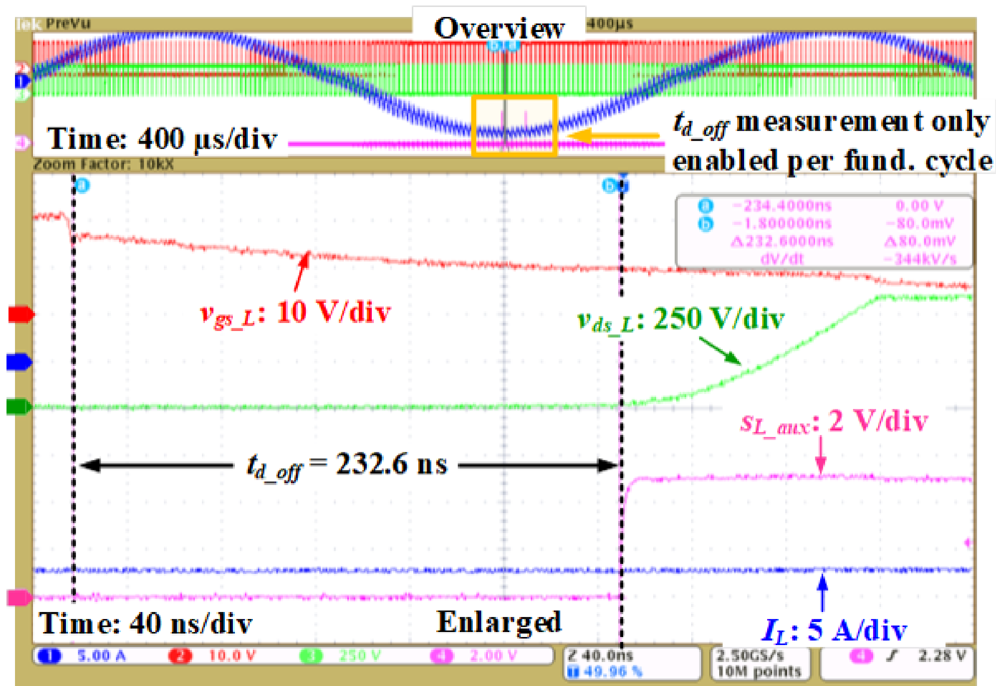


Figure 4.18: Online turn-off delay time monitoring for T_j recording when the lower switch is the operating switch

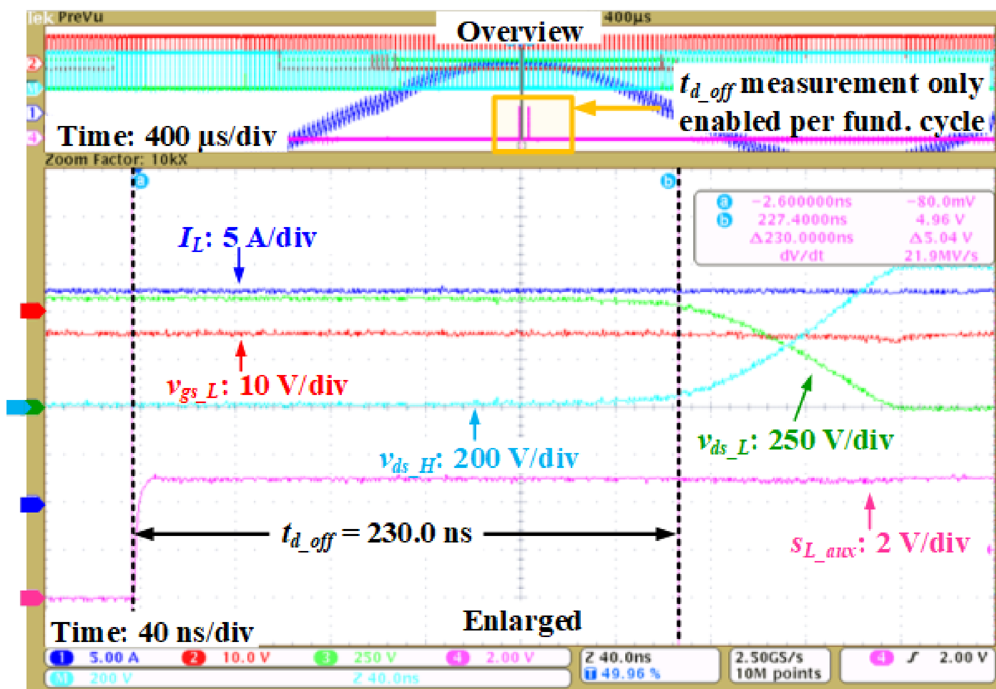


Figure 4.19: Online turn-off delay time monitoring for T_j recording when the upper switch is the operating switch

of the electronic integrated circuits (e.g., signal isolator and gate drive IC), their resultant uncertainty would adversely affect the minimum achievable capture resolution of the online turn-off delay monitoring. According to the test results, 0.5 ns uncertainty with respect to the turn-off delay sensing could be introduced, leading to increased junction temperature measurement error in the range of 2 °C to 3 °C. Note that this error can be further reduced with the sensitivity improvement via introducing larger gate resistance of the GRR assist circuit. For example, a GRR assist circuit with 300 Ω gate resistance is able to double the sensitivity as compared to that with 150 Ω gate resistance, as a result, the measurement error reduces by a factor of two (i.e., 1 °C to 1.5 °C).

To further prove the accuracy of the temperature sensing approach, a FLIR T600 was used to take thermal imaging of the SiC device under test during converter operation. The resulting thermal image of the low side SiC device is shown in Figure 4.20. This approach is not used as the primary validation of the accuracy for two reasons associated with content from chapter 2. One, the camera is recording the top-side case temperature (T_c) of the SiC device and that data is difficult to compare to the T_j data without knowledge of thermal resistances (R_{th}) and device power loss. Second, the FLIR camera's purpose is to give the user a general temperature map of the environment in frame, and as shown in section 2.1.1, IR-based temperature sensing approaches can be inaccurate at times. Nevertheless, this secondary temperature data can be compared with the TSEP-based T_j recording shown in Figure 4.21, which is a GUI set up to show the real-time monitored T_j during converter operation.

4.5.2 Aging Effect

Throughout this testing, the same two SiC devices were used. These devices operated under high temperatures both naturally in continuous operation and intentionally with a hot plate. After many hours of accumulated stress on the devices, it was discovered that $t_{d,off}$ decreased from degradation in the calibration curve, which can be seen in Figure 4.22.

To further analyze this behavior, the three SiC devices used throughout the testing were compared with a brand new device. Figure 4.23 shows a picture of the four devices analyzed:

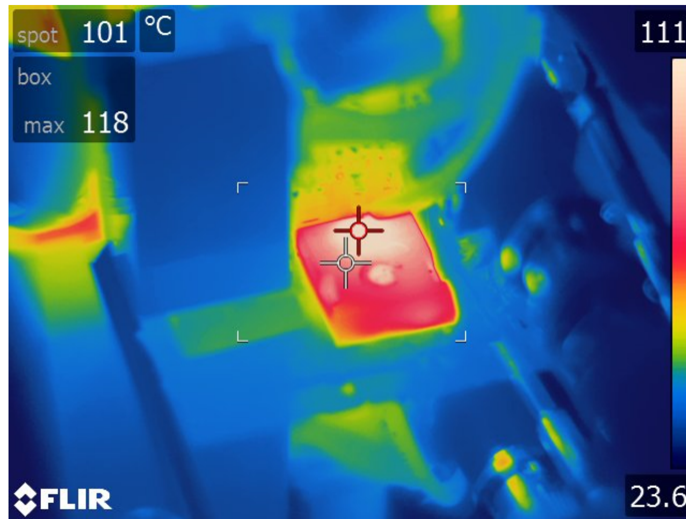


Figure 4.20: SiC device secondary temperature sensing with FLIR camera

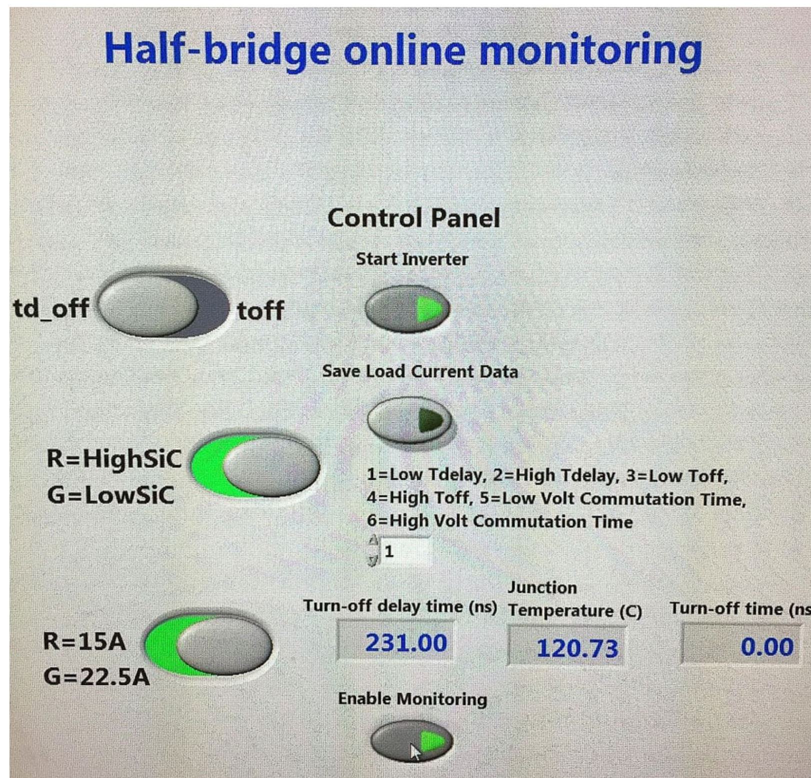


Figure 4.21: LabVIEW GUI of junction temperature monitoring

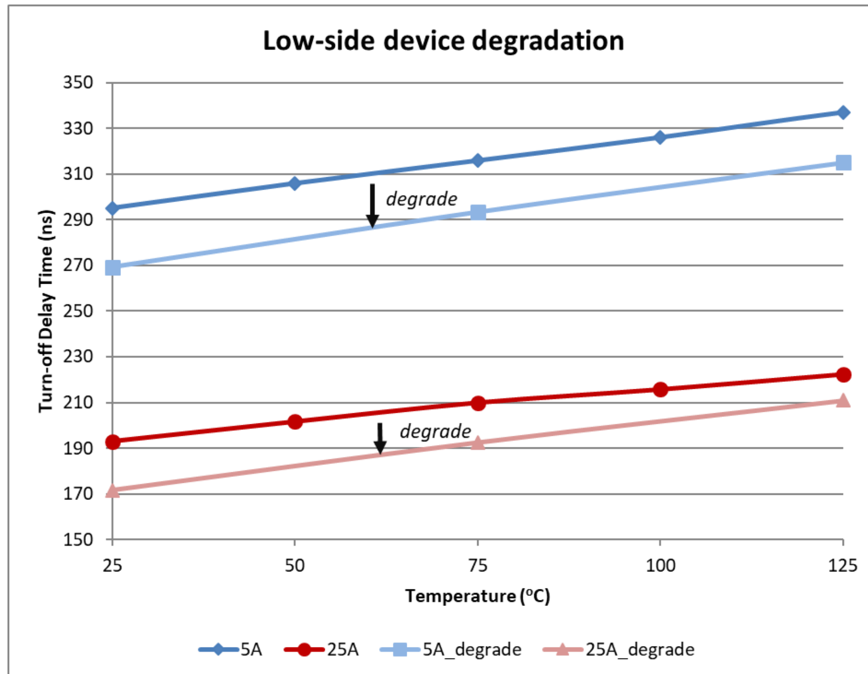


Figure 4.22: Low-side SiC degradation seen on calibration curve shift

- New - the brand new device
- Low - the degraded SiC device that was on the low side of the phase-leg
- High - the current high-side SiC device that had only recently been used
- Old - the degraded SiC device that was on the high side of the phase-leg and replaced

These devices were placed in a curve tracer and a transfer characteristic curve was plotted for all four devices. In looking at the results in Figure 4.24, the transfer curves of the degraded devices have shifted to the right. This is because the threshold voltage of the devices has increased due to gate oxide degradation. This gate oxide deterioration can be common for SiC from high gate biasing and high temperature operation.

Coming back to the shift in the calibration curve, this creates an interesting application for the TSEP-based T_j sensing scheme. If a secondary temperature measurement is applied (e.g. NTC thermistor in a power module), then this particular TSEP-based sensing scheme can be used as a device health monitoring approach. The way it would work is if the two temperature measurements started to diverge, this would indicate a start of a device

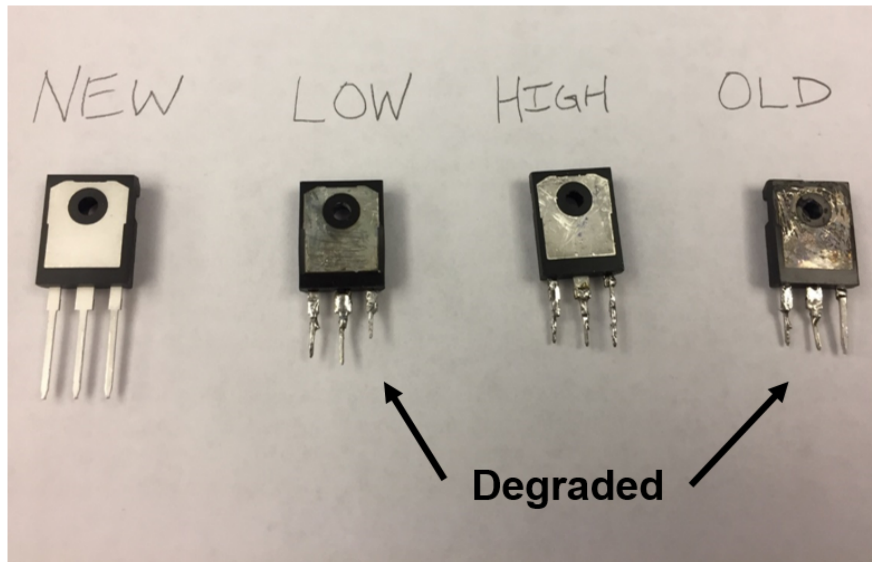


Figure 4.23: Picture of new and degraded SiC devices

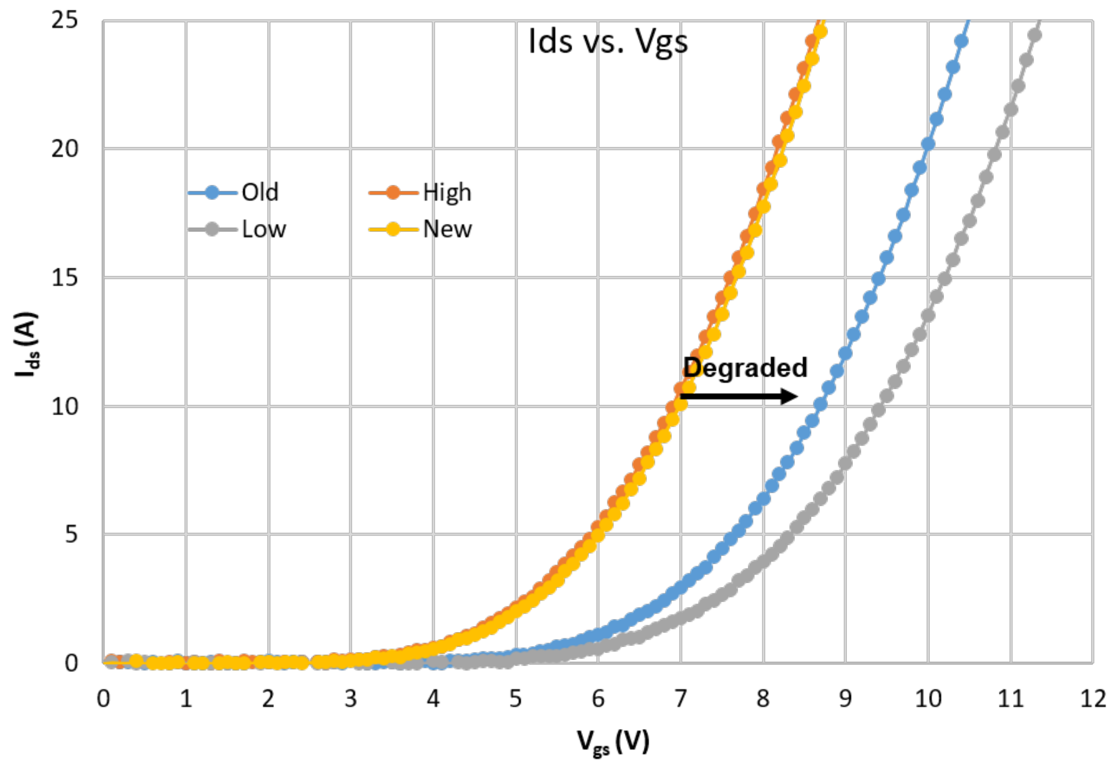


Figure 4.24: Transfer curves for new and degraded SiC devices

degradation. After a certain amount of deterioration time, maintenance could be called for on the device/converter.

4.5.3 Multi-Purpose Implementation

An important aspect of implementing a gate resistor regulation system as a part of this intelligent gate driver is its ability to be used in multiple applications. An argument can be made against this particular TSEP approach for needing to alter the converter behavior during operation, and even though the implementation has been shown to have minimal negative effect on the overall performance, adding this circuitry is increased complexity. However, this gate resistance regulation system can be leveraged for more than just the enhanced temperature sensitivity for junction temperature monitoring. An example of this is slowing down the switching time of a particular device that is overheating. If the SiC devices were used in an application where their switching loss was causing the devices to reach a overtemperature threshold, the GRR system could be used to not only monitor that overtemperature but also help cool the device down with slower switching.

Another example of multi-purpose implementation are the desaturation diodes that are used for short-circuit protection of power semiconductor transistors. Desat protection uses diodes with high reverse voltage to block the high voltage across the main SiC device in the OFF state, and then turns on to sense the main SiC's drain-source on-voltage to detect overcurrent. This monitoring system implementation also needed blocking diodes on the drain of the devices for blocking the high voltage during the main SiC turn-off shown in Figure 3.9a. In this work, desat protection was not implemented to be able to focus on the design of the monitoring system. In a future intelligent gate driver implementation, both desat protection and turn-off time monitoring can be implemented together using the same desat diodes.

According to the block diagram of online switching time monitoring illustrated in Figure 3.8, the extra implementation hardware primarily consists of four gate assist circuits, specifically including GRR assist circuit for sensitivity improvement, and GVTD, DVTD, and DVFD detection circuits. All of the auxiliary circuits depend on low voltage and consists of resistors, capacitors, diodes, and small transistors. As shown in Figure 3.10, the extra

circuits have been integrated with the conventional gate drive at the board level with small footprint. To take it a step further, these components can be embedded into a gate drive IC, enabling this approach to be less-complex and cost-effective for end users.

Although the experimental verification is carried out in a DC/AC converter as the focus voltage-source converter, the proposed approach can be extended to AC/DC and DC/DC converters where the power devices are operated in hard-switching PWM mode. Also, this approach is not limited to SiC devices, but can be leveraged to traditional Si IGBTs and even GaN HEMTs if the Miller voltage (i.e. turn-off delay time) of these devices is sufficiently sensitive to the junction temperature.

Chapter 5

Conclusions and Recommendations

5.1 Conclusions

This thesis shows the ability to apply a data acquisition system in a gate driver of SiC devices used in a VSI. This monitoring system not only added behavioral data of the devices but the data was used from converter-level benefits: dead-time control and junction temperature monitoring.

Test results show that with the proposed gate impedance regulation assist circuit, the sensitivity of the turn-off delay time with respect to junction temperature increases from tens of ps/°C to hundreds of ps/°C with little penalty of the power conversion performance. Also, the online monitoring system consisting of three gate assist units for capturing and recording critical moments during the turn-off transient allows the micro-controller to determine the turn-off delay time with a resolution within hundreds of pico-seconds. In the end, the proposed approach is capable of online monitoring junction temperature with satisfactory accuracy. Furthermore, the proposed gate assist circuits for sensitivity improvement and high precision turn-off delay time measurement are all transistor based, offering a suitable option for chip level integration and enabling this approach to be less-complex and cost-effective for end users.

A dead-time optimization scheme is proposed for any VSC using online turn-off monitoring for the two SiC devices in a phase-leg configuration. Dead-time optimization is preferred for SiC based converters because of higher reverse conduction loss, faster

switching frequency, and the turn-off times increased sensitivity to operating conditions and load characteristics. A dead-time compensation scheme is also added as an application of the monitoring system to improve power quality for VSIs. Dead-time compensation can help mitigate the negative effects of dead-time, parasitic capacitance and switching time sensitivity in high frequency SiC VSIs. The online monitoring system distinguishes itself by also detecting current polarity based on the V_{ds} switching waveform, which eliminates the need for a current sensor that can be unreliable around the zero current crossing.

A 1 kW half-bridge inverter experimental test, switching at 50 kHz, was conducted to obtain the results of the dead-time control. The test results show a 70% enhancement on the error against the ideal fundamental current value of the output current and a 2% THD improvement on the output current low frequency harmonics. In addition, the monitoring feature enables the scheme to be load application independent, eliminate the need for precise current sensing, especially during zero-crossing, and improve over offline modeling for accurate and dynamic implementation. The test results also show clear reverse conduction power loss reduction compared to conservative dead-time settings of 500 ns (91% reduction) and 1 μs (95.6% reduction). The optimization results also show 100% reduction in the partial hard turn-on loss when compared to the aggressive dead-time setting of 100 ns.

5.2 Future Work

Dead-time Compensation

This work leveraged the non-ideal switching time monitoring to compensate for the output voltage distortion caused by volt-second error from dead-time and non-ideal switching, which was a major contribution for this work. However, because the focus of the work was more on the monitoring scheme itself, detailed dead-time compensation was not performed. Only a single voltage-source inverter test case was performed and analyzed. Future work would be to evaluate multiple test cases comparing this dead-time compensation scheme to traditional implementations. This is especially true for varying ratios of fundamental frequency to switching frequency as this changes the amount of cycles where volt-second error can occur.

SiC Device Reliability Diagnostics and Prediction

As mentioned in the introduction, systems incorporating SiC still need to be improved in terms of reliability. In terms of how data sensing can help a semiconductor's reliability, condition monitoring can be applied. Condition monitoring is the technique or process for monitoring the operating characteristics of a component or an equipment, in such a way as to predict the need for maintenance before serious deterioration or breakdown [75, 76]. Condition monitoring has already proven its worth in a number of fields like: power systems [77], industrial equipment [78], and health monitoring [79].

Though this can be a great application for the work of data acquisition incorporated in a gate driver for SiC devices, it is difficult to realistically implement. The junction temperature monitoring system is a great first step since it is a device health parameter [18]. However, to be considered a condition monitoring implementation, there needs to be some diagnostics and lifetime prediction based on the sensed data. This would require accelerated aging testing to try and characteristic the behavior of the sensed parameter is relation to full lifetime performance. This type of work was not implemented as part of this thesis and if this application was decided to be researched, then accelerated aging testing setups would be needed.

Parallel-connected Device Application

As part of a previous UTK gate driver project, phase 1 designed a gate driver for new fabricated and packaged SiC discrete devices. This phase 1 gate driver had the features: high common mode transient immunity (CMTI) capability, fast switching and cross-talk suppression, and fast response short-circuit protection using desaturation method.

Phase 1 also designed a low parasitic power stage for adequate passive current sharing between four SiC devices connected in parallel. The reason for the power stage setup with discrete devices in parallel, as opposed to using a module, is for multiple reasons. First, GE wanted to see the performance of their own packaged devices. Second, this helped in research as the power stage could be treated as an *open-module*, where better characterization of individual device performance can be evaluated and studied [53].

This opened up a unique application for the on-going phase 2 of this project, which focuses on adding data acquisition in this IGD. With using discrete devices, sensing schemes could be applied to devices in parallel to understand in real-time how they are preforming in parallel. The approach being developed is using $t_{d,on}$ as a TSEP for T_j monitoring. This parameter is better to use in this application because the devices in parallel all have the same V_{DS} waveform but can have different I_D values. In a system where it is preferred for the TSEP to only be dependent on T_j, it is better to use $t_{d,on}$ as it does not depend on current and the calibration cannot be affected by current mismatch during converter operation. This work is on-going and will add research to the breadth of understanding on both TSEP-based junction temperature monitoring for SiC devices and incorporating data acquisition to a power electronics gate driver.

Bibliography

[1] J. Millan, P. Godignon, X. Perpi, A. Prez-Toms, and J. Rebollo, “A survey of wide bandgap power semiconductor devices,” *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2014. 1, 5

[2] Z. Zhang, “Characterization and realization of high switching-speed capability of sic power devices in voltage source converter,” Ph.D. dissertation, University of Tennessee, 2015. 1, 7

[3] K. Sung-Hun, S. R. Lee, H. Dehbonei, and C. V. Nayar, “Application of voltage- and current-controlled voltage source inverters for distributed generation systems,” *IEEE Transactions on Energy Conversion*, vol. 21, no. 3, pp. 782–792, 2006. 1

[4] K. Olejniczak, T. Flint, D. Simco, S. Storkov, B. McGee, R. Shaw, B. Passmore, K. George, A. Curbow, and T. McNutt, “A compact 110 kva, 140 °c ambient, 105 °c liquid cooled, all-sic inverter for electric vehicle traction drives,” in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 735–742. 1, 2

[5] Y. Haizhong, Y. Yang, and A. Emadi, “Traction inverters in hybrid electric vehicles,” in *2012 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2012, pp. 1–6. 1

[6] F. Shang, A. P. Arribas, and M. Krishnamurthy, “A comprehensive evaluation of sic devices in traction applications,” in *2014 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2014, pp. 1–5. 1

[7] B. Ozpineci, “System impact of silicon carbide power electronics on hybrid electric vehicle applications,” Ph.D. dissertation, University of Tennessee, 2002. 1

[8] M. Das, “Sic mosfet module replaces up to 3x higher current si igbt modules in voltage source inverter application,” 2013. 2, 3

[9] S. Hazra, A. De, L. Cheng, J. Palmour, M. Schupbach, B. A. Hull, S. Allen, and S. Bhattacharya, “High switching performance of 1700-v, 50-a sic power mosfet over si igbt/bimosfet for advanced power conversion applications,” *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4742–4754, 2016. 2

[10] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "Sic versus sievaluation of potentials for performance improvement of inverter and dcdc converter systems by sic power semiconductors," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2872–2882, 2011. 2

[11] S. Mao, T. Wu, X. Lu, J. Popovic, and J. A. Ferreira, "Three-phase active front-end rectifier efficiency improvement with silicon carbide power semiconductor devices," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–8. 2

[12] Z. Liang, F. Wang, and L. Tolbert, "Development of packaging technologies for advanced sic power modules," in *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2014, pp. 42–47. 2

[13] AgileSwitch, "Edem-econodual electrical series," in *datasheet*, 2015. 5

[14] C. M. DiMarino, "High temperature characterization and analysis of silicon carbide (sic) power pemiconductor transistors," Ph.D. dissertation, Virginia Polytechnic Inst. and State Univ, 2014. 5

[15] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Improved reliability of power modules: A review of online junction temperature measurement methods," *IEEE Industrial Electronics Magazine*, vol. 8, no. 3, pp. 17–27, 2014. 5, 18

[16] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Transactions on Industry Applications*, vol. 47, no. 3, pp. 1441–1451, 2011. 6

[17] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Industrial Electronics Magazine*, vol. 7, no. 2, pp. 17–26, 2013. 6

[18] H. Huang and P. A. Mawby, "A lifetime estimation technique for voltage source inverters," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 4113–4119, 2013. 6, 85

[19] A. Ibrahim, J. P. Ousten, R. Lallemand, and Z. Khatir, "Power cycling tests in high temperature conditions of sic-mosfet power modules and ageing assessment," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1–6. 6, 13, 14

[20] L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, "Reliability issues of sic mosfets: A technology for high-temperature environments," *IEEE Transactions on Device and Materials Reliability*, vol. 10, no. 4, pp. 418–426, 2010. 6

[21] D. P. Hamilton, M. R. Jennings, A. Prez-Toms, S. A. O. Russell, S. A. Hindmarsh, C. A. Fisher, and P. A. Mawby, "High-temperature electrical and thermal aging performance and application considerations for sic power dmosfets," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7967–7979, 2017. 6

[22] N. Baker, S. Munk-Nielsen, and S. Bczkowski, "Test setup for long term reliability investigation of silicon carbide mosfets," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–9. 6

[23] S. Mbarek, P. Dherbcourt, O. Latry, F. Fouquet, D. Othman, M. Berkani, and S. Lefebvre, "Robustness study of sic mosfet under harsh electrical and thermal constraints," in *International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS)*, 2014. 6

[24] A. J. Lelis, R. Green, and D. B. Habersat, "Sic mosfet reliability and implications for qualification testing," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2017, pp. 2A–4.1–2A–4.4. 6

[25] Z. Chen, "Characterization and modeling of high-switching-speed behavior of sic active devices," Ph.D. dissertation, Virginia Polytechnic Institute and State University, 2009. 7

[26] Z. Zhang, B. Guo, F. Wang, L. M. Tolbert, B. J. Blalock, Z. Liang, and P. Ning, "Impact of ringing on switching losses of wide band-gap devices in a phase-leg configuration," in

2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, 2014, pp. 2542–2549. 7, 40

[27] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Decoupling of interaction between wbg converter and motor load for switching performance improvement," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1569–1576. 7, 40

[28] B. Liu, R. Ren, E. Jones, F. Wang, D. Costinett, and Z. Zhang, "A modulation compensation scheme to reduce input current distortion in gan based high switching frequency three-phase three-level vienna type rectifiers," *IEEE Transactions on Power Electronics*, vol. 33, no. 99, pp. 283–298, 2017. 8, 32

[29] E. R. Motto, J. F. Donlon, M. Honsberg, and F. Tametani, "A new intelligent power module with enhanced diagnostics and protection," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 2398–2401. 8

[30] B. Whitaker, Z. Cole, B. Passmore, D. Martin, T. McNutt, A. Lostetter, M. N. Ericson, S. S. Frank, C. L. Britton, L. D. Marlino, A. Mantooth, M. Francis, R. Lamichhane, P. Shepherd, and M. Glover, "High-temperature sic power module with integrated sic gate drivers for future high-density power electronics applications," in *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2014, pp. 36–40. 8

[31] M. Otsuki, M. Watanabe, and A. Nishiura, "Trends and opportunities in intelligent power modules (ipm)," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2015, pp. 317–320. 8

[32] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent gate drive for fast switching and crosstalk suppression of sic devices," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9319–9332, 2017. 8

[33] A. Kumar, A. Ravichandran, S. Singh, S. Shah, and S. Bhattacharya, "An intelligent medium voltage gate driver with enhanced short circuit protection scheme for 10kv 4h-sic mosfets," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 2560–2566. 8, 10

[34] T. P. Chow, "Wide bandgap semiconductor power devices for energy efficient systems," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 402–405. 12

[35] STMicroelectonics, "Thermal effects and junction temperature evaluation of power mosfets," 2015. 12

[36] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Springer, 2011. 13, 24

[37] S. Carubelli and Z. Khatir, "Experimental validation of a thermal modelling method dedicated to multichip power modules in operating conditions," *Microelectronics Journal*, vol. 34, no. 12, pp. 1143–1151, 2003. 13

[38] D. L. Blackburn, "Temperature measurements of semiconductor devices - a review," in *Twentieth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (IEEE Cat. No.04CH37545)*, 2004, pp. 70–80. 13, 14, 15

[39] W. Brekel, T. Duetemeyer, G. Puk, and O. Schilling, "Time resolved in situ tvj measurements of 6.5kv igbts during inverter operation," in *PCIM Europe*, Nuremberg, Germany, 2009, pp. 806–813. 13, 14, 15, 16, 18

[40] Infineon, "Using the ntc inside a power electronic module," 2015. 13, 15

[41] TDK, "Ntc thermistors for power semiconductors," 2015. 13

[42] P.-L. Doumergue, "Using ntc temperature sensor integrated into power module," 2016. 13

[43] A. Hefner, D. Berning, D. Blackburn, C. Chapuy, and S. Bouche, "A high-speed thermal imaging system for semiconductor device analysis," in *Seventeenth*

Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.01CH37189), 2001, pp. 43–49. 14

[44] A. Griffo, J. Wang, K. Colombage, and T. Kamel, "Real-time measurement of temperature sensitive electrical parameters in sic power mosfets," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1–1, 2017. 15, 27

[45] K. Shenai, "Future prospects of widebandgap (wbg) semiconductor power switching devices," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 248–257, 2015. 16, 17

[46] Infineon, "Iposim," 2014). 16

[47] T. Bruckner and S. Bernet, "Estimation and measurement of junction temperatures in a three-level voltage source converter," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 3–12, 2007. 16

[48] H. Chen, B. Ji, V. Pickert, and W. Cao, "Real-time temperature estimation for power mosfets considering thermal aging effects," *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 1, pp. 220–228, 2014. 16, 21, 22

[49] D. C. Katsis and J. D. v. Wyk, "Void-induced thermal impedance in power semiconductor modules: some transient temperature effects," *IEEE Transactions on Industry Applications*, vol. 39, no. 5, pp. 1239–1246, 2003. 16

[50] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters-a review," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 3081–3092, 2012. 17, 18, 21

[51] Z. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, B. J. Blalock, and X. Wu, "Online junction temperature monitoring using turn-off delay time for silicon carbide power devices," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–7. 19, 28

[52] A. Marzoughi, R. Burgos, and D. Boroyevich, "Characterization and comparison of latest generation 900-v and 1.2-kv sic mosfets," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–8. 20

[53] A. Kadavelugu, E. Aeloiza, and C. Belcastro, "Short-circuit performance of multi-chip sic mosfet modules," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 285–290. 20, 85

[54] N. Baker, "An electrical method for junction temperature measurement of power semiconductor switches," Ph.D. dissertation, Aalborg University, 2016. 22

[55] L. Zhang, P. Liu, S. Guo, and A. Q. Huang, "Comparative study of temperature sensitive electrical parameters (tsep) of si, sic and gan power devices," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, pp. 302–307. 22, 23

[56] J. O. Gonzalez, O. Alatise, J. Hu, L. Ran, and P. A. Mawby, "An investigation of temperature-sensitive electrical parameters for sic power mosfets," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7954–7966, 2017. 23, 24, 31

[57] F. Stella, G. Pellegrino, E. Armando, and D. Dapr, "On-line temperature estimation of sic power mosfet modules through on-state resistance mapping," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 5907–5914. 23, 25

[58] J. O. Gonzalez, O. Alatise, L. Ran, and P. Mawby, "Impact of temperature imbalance on junction temperature identification for multiple chip modules using tseps," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2017, pp. 1–8. 24, 25, 26

[59] D. Bergogne, A. Hammoud, D. Tournier, C. Buttay, Y. Amieh, P. Bevilacqua, A. Zaoui, H. Morel, and B. Allard, "Electro-thermal behaviour of a sic jfet stressed by lightning-induced overvoltages," in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–8. 24

[60] H. Niu and R. Lorenz, "Real-time junction temperature sensing for silicon carbide mosfet with different gate drive topologies and different operating conditions," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017. 27, 28

[61] B. Hull, S. Allen, Q. Zhang, D. Gajewski, V. Pala, J. Richmond, S. Ryu, M. O. Loughlin, E. V. Brunt, L. Cheng, A. Burk, J. Casady, D. Grider, and J. Palmour, "Reliability and stability of sic power mosfets and next-generation sic mosfets," in *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2014, pp. 139–142. 29

[62] Vishay, "Power mosfet basics: Understanding gate charge and using it to assess switching performance," 2014. 29

[63] H. Kuhn and A. Mertens, "On-line junction temperature measurement of igbts based on temperature sensitive electrical parameters," in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–10. 29, 30

[64] B. Shi, S. Feng, L. Shi, D. Shi, Y. Zhang, and H. Zhu, "Junction temperature measurement method for power mosfets using turn-on delay of impulse signal," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017. 29

[65] L. Chen and F. Z. Peng, "Dead-time elimination for voltage source inverters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 574–580, 2008. 31, 32, 33

[66] Y. Wang, Q. Gao, and X. Cai, "Mixed pwm for dead-time elimination and compensation in a grid-tied inverter," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 10, pp. 4797–4803, 2011. 31, 32

[67] J. Yuan, Z. Zhao, B. Chen, C. Li, J. Wang, C. Tian, and Y. Chen, "An immune-algorithm-based dead-time elimination pwm control strategy in a single-phase inverter," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3964–3975, 2015. 31, 32, 34

[68] V. Yousefzadeh and D. Maksimovic, "Sensorless optimization of dead times in dc-dc converters with synchronous rectifiers," *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 994–1002, 2006. 32

[69] S. Lee, S. Jung, C. Park, C. T. Rim, and G. H. Cho, "Accurate dead-time control for synchronous buck converter with fast error sensing circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 11, pp. 3080–3089, 2013. 32

[70] Z. Zhang, H. Lu, D. Costinett, F. Wang, L. M. Tolbert, and B. J. Blalock, "Model based dead-time optimization for voltage source converters utilizing silicon carbide semiconductors," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016. 32

[71] C. Li, Y. Gu, W. Li, X. He, Z. Dong, G. Chen, C. Ma, and L. Zhang, "Analysis and compensation of dead-time effect considering parasitic capacitance and ripple current," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1501–1506. 32

[72] Z. Zhang and L. Xu, "Dead-time compensation of inverters considering snubber and parasitic capacitance," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 3179–3187, 2014. 32

[73] Y. Yang, K. Zhou, H. Wang, and F. Blaabjerg, "Harmonics mitigation of dead time effects in pwm converters using a repetitive controller," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1479–1486. 34

[74] "Tms320x2833x, 2823x high resolution pulse width modulator (hrpwm)," 2009. 49, 50

[75] T. Joseph, C. E. Ugalde-Loo, J. Liang, and P. F. Coventry, "Asset management strategies for power electronic converters in transmission networks: Application to hvdc and facts devices," *IEEE Access*, vol. 6, pp. 21 084–21 102, 2018. 85

[76] C. S. Kulkarni, J. R. Celaya, G. Biswas, and K. Goebel, "Prognostics of power electronics, methods and validation experiments," in *2012 IEEE AUTOTESTCON Proceedings*, 2012, pp. 194–199. 85

[77] J. Chai, Y. Liu, J. Guo, L. Wu, D. Zhou, W. Yao, Y. Liu, T. King, J. R. Gracia, and M. Patel, "Wide-area measurement data analytics using fnet/grideye: A review," in *2016 Power Systems Computation Conference (PSCC)*, 2016, pp. 1–6. 85

[78] K. Wang, *Intelligent Condition Monitoring and Diagnosis Systems.* Amsterdam, Netherlands: IOS Press, 2003. 85

[79] A. Pantelopoulos and N. G. Bourbakis, "A survey on wearable sensor-based systems for health monitoring and prognosis," *IEEE Transactions on Systems, Man, and Cybernetics, Part C (Applications and Reviews)*, vol. 40, no. 1, pp. 1–12, 2010. 85

Vita

Jacob Hamilton Dyer was born in Nashville, Tennessee. He attended Tennessee Technological University as an undergraduate and graduated magna cum laude in 2016 with a bachelors of science degree in electrical engineering. During his undergraduate studies, he earned two awards related to his senior capstone project: Best Capstone Project and Best Capstone Team Leader. He also was selected to be in the Eta Kappa Nu and Tau Beta Pi engineering honor societies. He also participated in undergraduate research in the area of power electronics, which led to a graduate-level research position at the University of Tennessee, Knoxville.

As a graduate student, Jacob was awarded the DOE Wide Bandgap Fellowship during the course of his master's studies. At UTK, Jacob's research has focused on intelligent gate drivers for SiC devices and their converter applications. While a student, Jacob has also served as the President of the CURENT Student Leadership Council as well as other officer positions in the SLC.