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A 2.4 GHz LC-VCO Using On-Chip Inductors and Accumulation-Mode Varactors in a CMOS 0.18 µm Process

Bryant Derand Williamson
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Bryant Derand Williamson entitled "A 2.4 GHz LC-VCO Using On-Chip Inductors and Accumulation-Mode Varactors in a CMOS 0.18 µm Process." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed K. Islam, Major Professor

We have read this thesis and recommend its acceptance:

Benjamin J. Blalock, M. Nance Ericson

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Vice Chancellor and
Dean of Graduate Studies

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A 2.4 GHz LC-VCO Using On-Chip Inductors and Accumulation-Mode Varactors in a CMOS 0.18 μm Process

A Thesis

Presented for the

Master of Science Degree

The University of Tennessee, Knoxville

Bryant Derand Williamson

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Abstract

The demand for low power, low cost, and low noise RF sub-systems has lead to the development of completely integrated transceivers. Frequency synthesizers containing a PLL and a crystal oscillator are perhaps the most challenging part of a transceiver's design. One of its nosiest, most power consuming components, the VCO, often makes the PLL a challenging design. For an LC-VCO, the best type of VCO for quality noise performance, the struggle lies in the fully integrated inductor. Despite the vast improvement in additional facets of the LC-VCO, the integrated inductor lags in its accomplishments; and the focus of designers is to work around the inductor's low quality factor. This research analyzes the LC-VCO and different means of compensating for design parameters hindered by a low-quality integrated inductor. It tests an LC-VCO developed in a 0.35 μm CMOS, 3.3V process and also designs an LC-VCO in a 0.18 μm CMOS, 1.8V process. The VCO design has a center frequency of 2.4 GHz. Also, its components and topology are scrutinized, while its performance is analyzed and verified through simulation results.

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Chapter 1 Introduction

1.1 Overview

With the growing demand for electronic devices to become smaller, cheaper, faster, and more reliable, wireless applications have, for the most part, kept up with personal and commercial expectations. Tasks as simple as opening a car door with a key have in recent years become somewhat rare. These advancements have not gone without notice because inventors now ponder the question, "What is the next device that would be convenient for wireless application?" Unaware to most consumers are the challenging tradeoffs presented to the designer when designing wireless communications circuits. These challenges are the result of a number of factors including ever increasing performance demands and integrated circuit design issues associated with continued process scaling and mass production. In addition, single chip systems require the use of fully integrated components, many of which are less desirable than their discrete counterparts. These factors make the design of fully integrated communications chips a continually evolving process.

One of the main parts of a wireless communication system, the transceiver, requires common circuits such as the phase locked loop (PLL). The voltage-controlled oscillator (VCO) is a key building block of the PLL and must be very accurate for most wireless applications. However, achieving the desired VCO characteristics for a particular application requires the designer to make design decisions based on a number of opposing parameters.

This thesis provides an overview of the design of a fully integrated VCO and discusses several of the tradeoffs common to VCO design. Architectural options and integrated component selections are discussed and simulation results for a newly designed, fully integrated LC-VCO (inductor-capacitor) are summarized. In addition, test results from a recently fabricated single chip VCO are provided.

1.2 Research Goals

The main objective of this research is to gain experimental and theoretical experience with voltage controlled oscillators. However, while doing so, a more comprehensible understanding of wireless technology will be attained. Through this research, the major problems associated with implementing an integrated RF LC-VCO will be investigated and considered in a new VCO design presented. Issues associated with the design, simulation, modeling, layout and testing of an integrated LC VCO will be discussed.

1.3 Contribution of Current Work

This thesis focuses on two primary tasks. First, a completely integrated 1.8 GHz LC-VCO fabricated in standard CMOS 0.35μm technology is examined and tested. From the results of these tests, a 2.4 GHz fully integrated LC-VCO in standard CMOS 0.18μm technology is developed in the course of examining different on-chip inductors and varactors, VCO device parameters, and the tradeoffs each parameter presents. Significant performance requirements are addressed in this design including a wide

tuning range (at least 400 MHz), low power dissipation (fewer than 15mW), low phase noise (less than -100dBc/Hz), and linear tuning. These two tasks together provide the reader with an overview of both the design and testing of modern fully integrated LC-VCOs.

1.4 Organization of Thesis

This thesis provides an overview of the design and testing of integrated LC VCOs. Chapter 2 begins with the history of the VCO including its origins and progression to its present day application in the phase locked loop. Performance parameters important in LC-VCO design are reviewed including the quality factor, a ratio of the energy stored versus energy lost. In Chapter 3 the role of the integrated inductor in the implementation of a VCO is discussed. A general discussion of the different physical types of integrated inductors and capacitors and how each affects VCO performance is presented. The primary circuit topologies for implementing an integrated LC-VCO are summarized in Chapter 4. The advantages, disadvantages, and examples of opportune conditions for the use of a given topology are provided. In Chapter 5 the test procedure of a completely integrated 1.8 GHz LC-VCO fabricated in a 0.35μm 3.3V CMOS process are reported. The parameters capable of being measured include tuning range, power consumption, and phase noise. The design of a fully integrated 2.4 GHz LC-VCO for fabrication in a 0.18μm 1.8V CMOS are presented in Chapter 6. Performance requirements are summarized and verified by simulation using proper models. A conclusion of this research and areas identified for future work are provided in Chapter 7.

Chapter 2 The Voltage Controlled Oscillator

The general function of an oscillator is to provide a periodic waveform. The frequency of these oscillations can be controlled by an input signal, typically a voltage or a current. The voltage controlled oscillator, often called a VCO, uses an input voltage to vary its output frequency. These devices are important parts of larger functions, such as phase locked loops, that are used in wireless communication systems. In this chapter, different oscillator topologies, as well as their characteristics, advantages, and disadvantages will be discussed.

2.1 The History of the VCO

Well before the modern day VCO, there was a need to generate oscillations for various electrical applications. Before 1910, the spark-gap oscillator was used for these functions. The spark-gap oscillator, as a part of the spark transmitter, worked on the same principle as a nearby radio picking up the RF radiation that is emitted by turning a light switch on or off. Despite its simplicity, the maturity of the spark transmitter (figure 2.1) suffered because of the disintegration of the insulation in the primary transformer. This breakdown was due to the large electro-magnetic fields produced by the sparks [24].

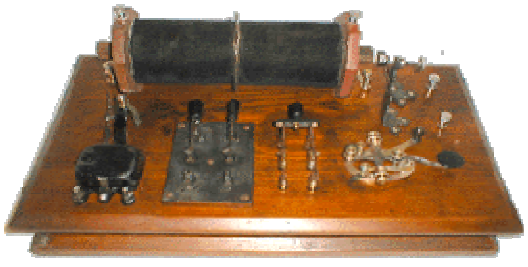


Figure 2.1 Picture of Homebrew Spark Transmitter [23]

The significant improvement of the VCO was realized when Edwin Armstrong created the heterodyne principle. Heterodyning is the mixing of multiple signals using a nonlinear device to create new frequencies. From this principle, Armstrong used an Audion, an early form of the vacuum tube, to produce a stable sinusoidal signal. Armstrong's work initiated a modernization of oscillator technology.

Edwin Armstrong's research was noticed and improved upon by Rober V.L. Hartley, who took advantage of then recent improvements in vacuum tube technology. In Hartley's design, the vacuum-tube behaved as an amplifier and used inductive feedback along with circuit capacitance to set the oscillation frequency [24]. This design advanced the quality of oscillators for transmitter and receiver applications because of the expanded range of frequencies. The frequency of Hartley's circuit could easily be adjusted by varying the feedback inductance or capacitance. In addition, Hartley's invention was extremely opportune because of its quick adaptation for use in World War I. Although these advances were significant, this was just the beginning of the advance of the voltage controlled oscillator.

The next notable advance in the voltage controlled oscillator came in the late 1940s with the invention of semiconductor amplifiers as opposed to the vacuum tube [24]. This transition lowered the size, power consumption, and cost of the VCO. Along with the invention of the varactor capacitor, the VCO had become an extremely precise electronic device. The progress of the varactor capacitor made the oscillator extremely important in phase locked loop implementation and gave way to the progress of then- thriving electronics such as the television. Although this technology was prominent well until the

1980s, oscillator design began to move toward the implementation of monolithic IC design [5].

2.2 The VCO as a Function of the Phase Locked Loop

The phase locked loop (PLL), shown in figure 2.2, is a key component of wireless communication systems. RF transceiver circuits call for tunable and precise local oscillator (LO) signals. The accuracy of the LO signal is an influential factor in the overall performance of a wireless system. The precision of the LO determines the closeness of channels in a system which is very important for narrow-band applications. A classic PLL architecture consists of a VCO, a low-pass loop filter, a phase/frequency detector (PFD), a charge pump (CP), and a frequency divider.

Oscillators are important parts in executing phase locked loop frequency synthesizers. A PLL contains a crystal oscillator and a voltage controlled oscillator, both of which are necessary for an accurate LO signal. A common crystal oscillator possesses

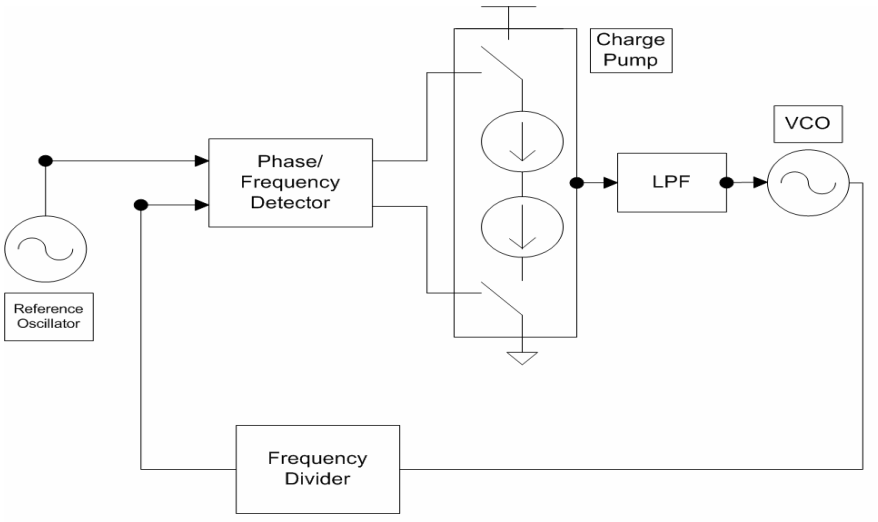


Figure 2.2 Basic Block Diagram of a PLL

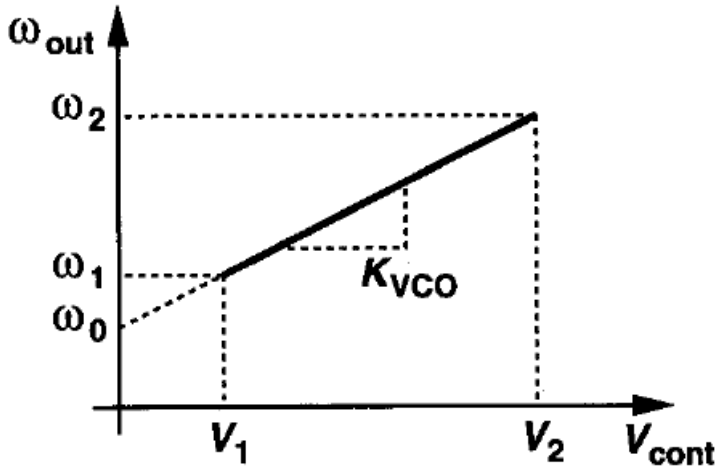
tremendous accuracy because of its high quality resonator. However, a crystal oscillator is unable to stand alone as a local oscillator signal because it cannot be built at sufficiently high RF frequencies. The other type of oscillator used in a PLL design is a voltage controlled oscillator. The VCO can be executed at RF frequencies while being made tunable, but has a low quality resonator, making it too unstable to sustain LO precision. On the other hand, by utilizing a crystal oscillator as a reference and a VCO as an output, an accurate, as well as synthesize-able LO signal can be maintained [1].

2.3 VCO Performance Parameters

Almost all wireless tasks require a tunable reference frequency. As mentioned in the preceding section, a voltage, as opposed to a current, is used as an input signal due to the current's complication of tuning the resonator. An ideal VCO will produce an output frequency that is linearly related to its input voltage. However, the linearity of its output is only one of the many essential parameters of a high-quality VCO. Other significant parameters include tuning range, power dissipation, phase noise, and output amplitude. However, many of these parameters oppose each other, requiring the designer to juggle the trade-offs given the application.

A. Tuning Linearity

Tuning linearity is a vital parameter of a VCO. Although linear tuning is desired, it is never the case because of the nonlinear behavior of VCO components. Linearity is preferred to keep K_{VCO}, the VCO gain, constant. A steady VCO gain, as seen in figure 2.3, assures that the PLL will perform efficiently [1].



$$\omega_{out} = \omega_0 + K_{VCO} V_{control}$$

Figure 2.3 Ideal VCO Tuning Linearity [9]

B. Tuning Range

Another essential parameter in the function of a quality VCO is its tuning range. A VCO's tuning range has two specifications. The first and most obvious is that the center frequency of the tuning range must be consistent with the frequency of the application. The second criterion deals with the deviation of the frequency stability to variations in temperature and process. This factor is one of the most challenging parts of designing a VCO given strict preliminary parameters. Often, a wide tuning range is selected to accommodate this issue. Nevertheless, the selection of a wide range causes a problem because of the variation in the VCO gain. The gain variation, due to tuning nonlinearities, causes the circuit output frequency and phase to fluctuate. The nonlinearities can be minimized by lowering the tuning range, but this is a direct contradiction of raising it to accommodate process and temperature limitations [1].

C. Power Consumption

The amount of power that a voltage controlled oscillator dissipates is one more important factor in the success of a design. The VCO block in a PLL usually consumes more power than any other part of the system [1]. With the increasing demand for low power devices, trade-offs have to be made between power consumption and other specifications. Since power affects almost all other aspects, the tuning range and phase noise are typically taken into account first. Usually, a budget is assigned for power, phase noise, or tuning range and the other two are tweaked to a satisfactory value accordingly.

D. Phase Noise

The next significant parameter in the design of a VCO is its phase noise. In the frequency domain, sidebands that appear around the frequency of oscillation are called phase noise (in the time domain this is called jitter) [1]. Phase noise can be minimized in several ways, all of which hinder the performance of the VCO in other areas. Therefore, as stated previously, many tradeoffs must be made to satisfy a particular application's requirements. In equation (1) below is the derivation of a linear time-invariant model of phase noise realized by Leeson [1].

$$L(f_m) = 10\log\left[\frac{2FkT}{Ps}\left(\frac{f_o}{2Q_L f_m}\right)^2\left(1+\frac{f_k}{f_m}\right)+\frac{|K_{VCO}|^2}{2f_m^2}S_{VCNT}+\frac{|K_{VDD}|^2}{2f_m^2}S_{VDD}+\frac{|K_{IB}|^2}{2f_m^2}S_{IB}\right] \quad (1)$$

Q_L = the loaded quality factor (quality factor of an oscillator is discussed later)

f_o = oscillation frequency

P_s = signal power of oscillation

f_m = offset frequency

F = noise factor of active devices

k = Boltzman's constant

T = temperature (Kelvin)

f_k = flicker noise corner frequency in the phase noise (not necessarily flicker noise corner of the active device)

$\frac{|K_{VCO}|^2}{2f_m^2} S_{VCNT}$, $\frac{|K_{VDD}|^2}{2f_m^2} S_{VDD}$, *and* $\frac{|K_{IB}|^2}{2f_m^2} S_{IB}$ are effectively the sensitivity of the VCO to the control voltage, supply, and bias current respectively

From inspection of equation (1), it seems as if there are several factors that can lower a VCO's phase noise. In reality, there are only about three that the designer can control. Q_L, F and P_s are each related to components of the voltage controlled oscillator. The loaded quality factor of the device, Q_L, is in the denominator of the phase noise equation, and is determined by the amount of series resistance in the oscillator tank [7]. This makes sense because high quality factor resonators inherently have lower phase noise. However, a high quality factor resonator is only achieved through high quality varactors and integrated inductors. The difficulty of achieving these high quality parts, especially in integrated implementation, will be discussed in the next chapter. The output power, P_s, is also in the denominator of Leeson's phase noise equation, which implies that a higher output power leads to lower phase noise. Nevertheless, what a designer must not forget is that output power is a major aspect in the design of a VCO and must be minimized. This is particularly important to the overall PLL since, as stated before, the VCO block consumes more power than any other block. The noise factor, F is in the

numerator of the equation and needs to be reduced in order to see a lower phase noise. Lowering the noise factor is directly related to the active devices chosen for the VCO. Lower flicker noise devices are better for this application. However, lowering the flicker noise in a transistor is especially compromising. PMOS devices inherently have lower flicker noise than NMOS devices, but bigger transistors (increasing gate area) are the key to lowering the overall flicker noise of any device. Still, bigger devices compromise the tuning range of the VCO because of extra gate capacitance.

Phase noise, fluctuations in the output amplitude and phase, are created when flicker noise of the active devices is up converted into the output spectrum of the VCO. Phase noise can also result from other sources such as the power supply. Phase noise is unwanted, especially in narrow band systems, because it can affect how closely channels can be placed within the system. For example, systems such as cellular applications are strictly governed with detailed specifications on phase noise for the efficient use of RF bands. Different components and causes of this noise are discussed throughout the text. Also discussed are methods and topologies to alleviate the affect of phase noise. Figures 2.4-2.6 demonstrate a typical phase noise spectrum and its calculation.

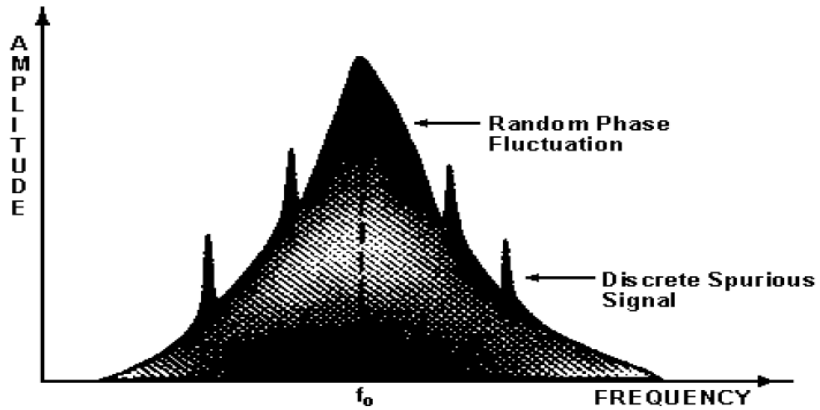


Figure 2.4 Example Spectrum Analyzer Display of Phase Noise [22]

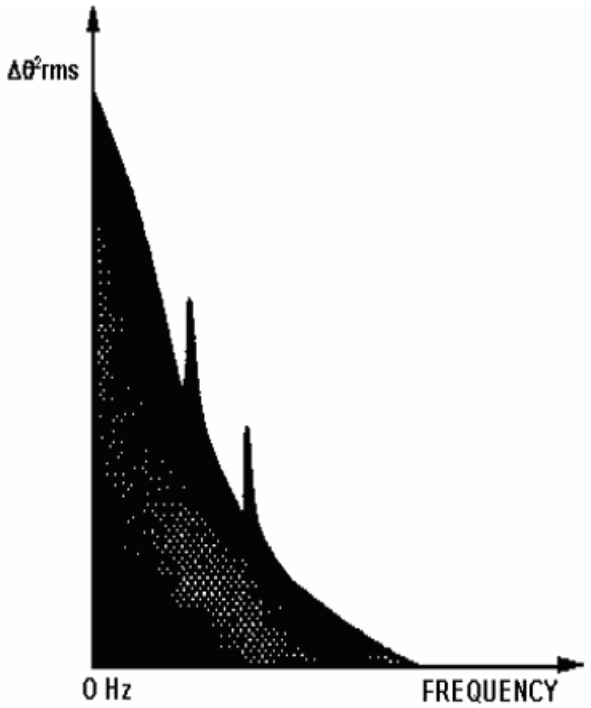


Figure 2.5 Single Sideband Representation of Spectrum [22]

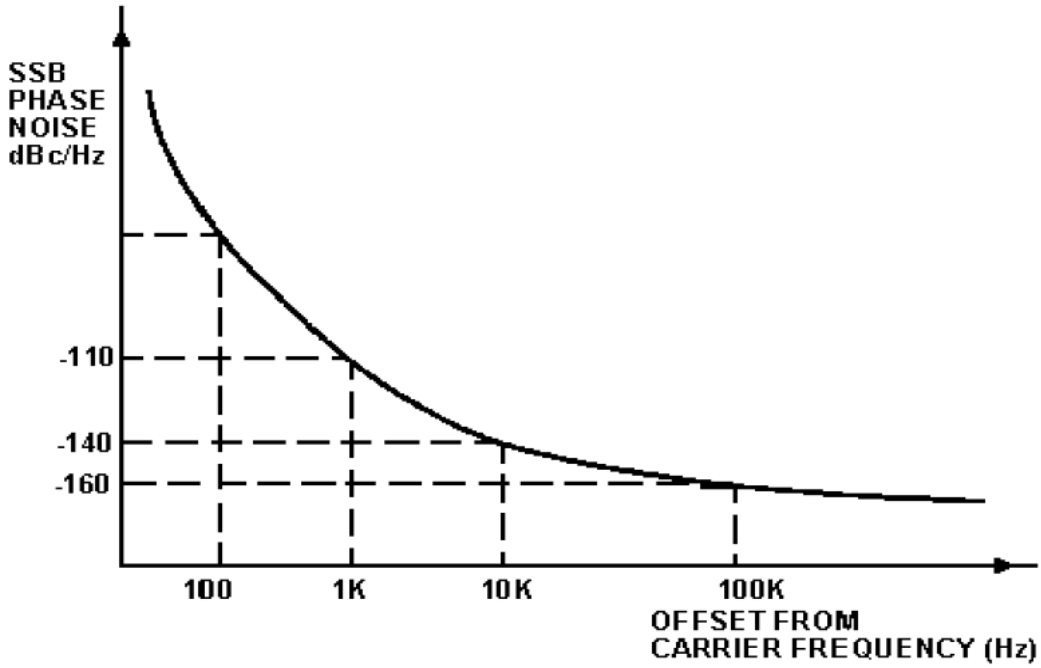


Figure 2.6 Single Sideband Phase Noise as a Function of Offset Frequency [22]

E. Output Amplitude

Output amplitude must be considered among other VCO design parameters . Increased amplitude implies less sensitivity to noise because of higher power consumption [1]. However, more power is a sacrifice because of possible power constraints. Also, elevated power may force a supply voltage higher than desired. Clearly, each of the VCO parameters imposes limitations on other parameters, and requires careful considerations.

2.4 The Quality Factor of a VCO

Perhaps the most essential part of an exceptional voltage controlled oscillator is its high quality resonator. The quality of a resonator, often called the quality factor (Q), is a vital factor in determining the phase noise of an oscillator. There are several working definitions for the quality factor, but all of them arrive at the same conclusion. A physicist would say [7]:

$$Q = 2\pi \times \frac{peak\ energy\ stored}{energy\ loss\ per\ cycle} \quad (2)$$

For an LC resonator, the Q is the ratio of energy stored to energy lost as it is passed back and forth from the inductor to the capacitor. Another definition treats the oscillator as a feedback network where the quality factor is defined as equation (3) [6]:

$$Q = \frac{\omega_o}{2}\left|\frac{d\phi}{d\omega}\right| \quad (3)$$

Representing the phase as a function of frequency and remembering that in order to maintain oscillation the phase shift around the loop must be zero, a variation from the

center frequency forces the phase slope positive and violates the oscillation condition. This violation drives the frequency back towards the center frequency. This Q is often called the "open loop Q" because it evaluates how far the closed loop system deviates from the center frequency [6].

The quality factor of a VCO can be calculated using the first definition, equation (2), and representing the tank as an LC with a parallel resistance R_p [7]. The sinusoidal voltage $V(t) = V_A \sin(\omega t)$ is applied to a test circuit seen in figure 2.7 at the bottom of the page. When V(t) reaches its maximum value, the voltage across the capacitor equals V_O and the current through the inductor is zero. Now, the energy in the capacitor is at its maximum and the energy in the inductor is zero. So peak energy stored can be represented as equation (4) [7]:

$$E_{peak} = \frac{CV_A^2}{2} \quad (4)$$

The energy lost through R_P can be represented as equation (5) [7]:

$$E_{loss} = \int_0^{2\pi/\omega} \frac{[V_A \sin(\omega t)]^2}{R_P} \cdot dt = \frac{\pi V_A^2}{\omega R_P} \quad (5)$$

The peak energy stored divided by the energy lost gives equation (6) [7]:

$$Q = 2\pi \times \frac{E_{peak}}{E_{loss}} = R_P \cdot \omega C = \frac{\omega L}{R_P} \quad (6)$$

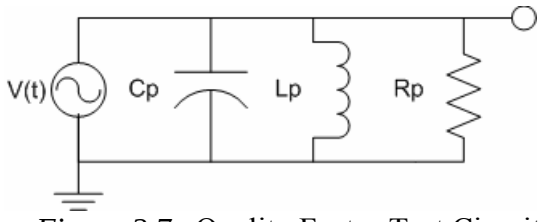


Figure 2.7 Quality Factor Test Circuit

The quality factor also plays a role in the calculation of the transconductance (g_m) for the cross coupled transistors of the VCO. The minimum oscillation requirement calls for $g_m \bullet R_P = 1$, but this is not assumed sufficient. Usually, a safety factor α, of 1.5-3 is used to assure oscillation. Through substitution $g_m = \frac{\alpha}{\omega QL}$, which is a basic design equation for an LC VCO, and is used to guarantee oscillation [7].

2.5 The LC VCO

Up until this point, most of this literature has discussed voltage controlled oscillators in general. However, it is important to analyze properties of the LC VCO since it is the architecture tested and designed in chapters 5 and 6, respectively. The LC-VCO uses an inductor and a capacitor as its resonator, with $1/(2\pi\sqrt{(LC)})$ setting the frequency of resonance [8]. In the ideal case, the impedance of the inductor and the capacitor are equal and opposite forming an infinite impedance at the resonant frequency. However, in practice, there is a series resistance associated with the inductor and the capacitor seen in figure 2.8 (a).

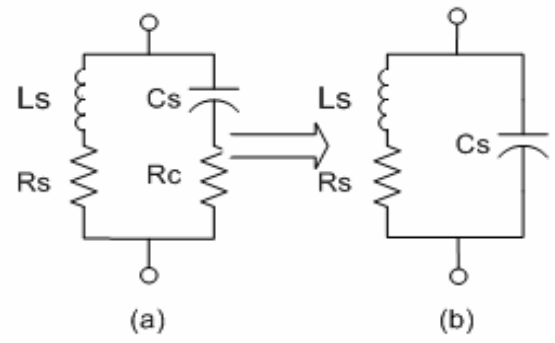


Figure 2.8 (a) Representation of the Oscillator Resonator Including Series Resistance of the Inductor and Capacitor (b) Simplified to Include Just the Resistance of the Inductor

Because the Q of the capacitor is much larger than the Q of the inductor, the losses due to R_c are minimal and often ignored. Therefore, the series model is represented in the form of figure 2.8 (b) on the previous page. Given this series model, a parallel model, which is more convenient for analysis, is usually constructed. In order for the series model to be equivalent to a parallel model [8],

$$L_s s + R_s = \frac{R_p L_p s}{R_p + L_p s} \quad (7)$$

Taking into account only steady state with s=jω this is rewritten as [8]:

$$(L_s R_p + L_p R_s)\, j\omega + R_s R_p - L_s L_p \omega^2 = R_p L_p\, j\omega$$

So if

$(L_s R_p + L_p R_s) = R_p L_p$ and $R_s R_p - L_s L_p \omega^2 = 0$ then

$R_p \approx \frac{L_s^2 \omega^2}{R_s}$ since $L_p \approx L_s$, and $L_p = L_s(1 + \frac{R_s^2}{L_s^2 \omega^2})$ [8]

With a current source in parallel with the RLC tank, initial oscillations can be induced, but will quickly disappear because of the losses through R_p. This is illustrated in figure 2.9.

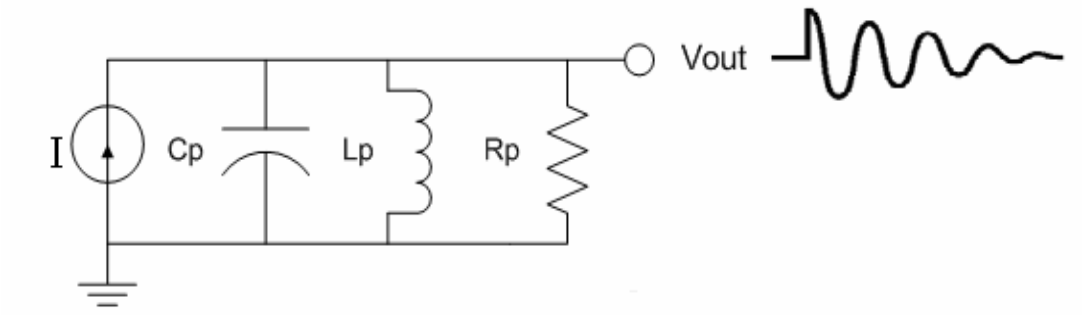


Figure 2.9 Oscillation Performance of the Voltage Controlled Oscillator With No Negative Resistance

Maintaining oscillations can be accomplished by the addition of a negative resistance, -R_p, placed in parallel with the circuit to yield $R_p // - R_p = \infty$. A negative resistance is implemented in practice by a positive feedback configured cross-coupled pair of transistors. From feedback theory,

$$R_{out} = R_{out}^{A}(1 + A\beta) \quad (8)$$

where R_{out}^{A} is the output resistance of the active pair [9]. If the feedback is positive then the loop gain, $A\beta$, will be negative, and a negative resistance will result. The negative resistance provided by the positive feedback loop appears in the form of equation (9)

which is derived from figure 2.10: $$R_{eq} = \frac{V_T}{I} = -(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}) = -\frac{2}{g_m} \quad (9)$$

With the addition of a negative resistance of at least R_p, then the oscillations will continue properly as seen in figure 2.11.

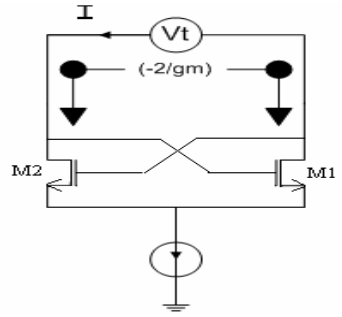


Figure 2.10 Reference Circuit for Derivation of Negative Resistance

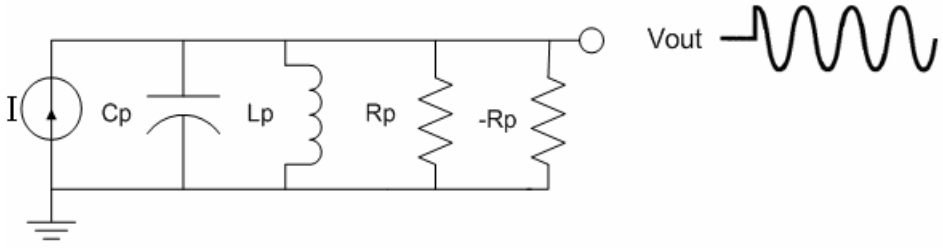


Figure 2.11 Adding Negative Resistance Which Cancels R_p Assures Proper Oscillation

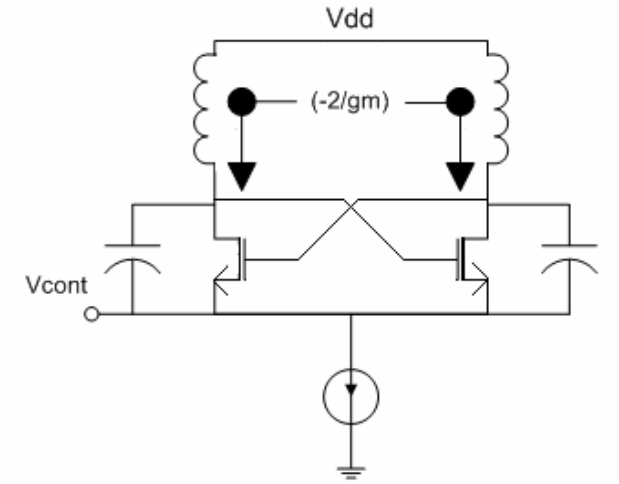


Figure 2.12 The Typical Active Circuit of an LC-VCO

Figure 2.12 is an example of the typical VCO with the control voltage represented as V_{cont}. Variations in LC-VCO designs lie in the use of different inductors and/or varactors. Also, there are many different topologies which vary the types of transistors used to achieve the negative resistance. The use of a specific topology or device is dependent on the specifications of the oscillator's application. The diverse types of inductors, varactors, and topologies will be explored in the following chapters.

Chapter 3 The Integrated Inductor and Varactor

Despite many improvements in the VCO, it still remains a challenging part of a fully integrated RF transceiver. This is due to the many design parameters associated with designing a VCO. For example, parameters such as power and phase noise have a direct relation to the quality factor of the tank and the linearity of the varactors. Also, the tuning range depends heavily on the varactor and VCO parasitics. For this reason, high quality inductors and varactors are necessary for good VCO performance. This chapter summarizes common options for integrated inductors and MOS-based varactors, and discusses associated non-ideal device parameters.

3.1 The Integrated Inductor

In voltage controlled oscillators, the most commonly used inductors are called hollow spiral inductors. In this case, hollow means that no winding stretches towards the center of the device. Figure 3.1 shows three types of frequently used spiral inductors which are the quadratical, octagonal, and symmetrical, octagonal inductors. For differential applications, the symmetry of the symmetrical inductor is advantageous. This is because the inductor looks the same from each port. However, the magnetic field

quadratical octagonal symmetrical octagonal

Figure 3.1 Example Spiral Inductors[4]

is changed through increasing the circularity, which is often limited. With all deep-sub-micron processes that contain several metal layers, there are two options in implementing an integrated inductor. One method produces a one layer inductor by connecting two metal layers in a pattern that imitates a solenoid [4]. For a one layer inductor, only the two outermost metal layers are used with the outermost metal as the core and the next as an outlet to prevent shorting. This method yields a more symmetrical magnetic field, but the series resistance of the inductor is increased due to the creation of a long metal strip. As well, nearby metal layers are at different potentials and generate a capacitance. The high series resistance of the inductor can be minimized by the second method, which forms a similar pattern, but stacks more of the available metals to increase the thickness. However, while doing so, this method also increases the coupling of the metal to the substrate. This happens when the effective thickness of the oxide insulation is decreased, which yields a greater capacitance between the metal and substrate. Therefore, the more metal layers used in the second method, the closer the metal is to the substrate, and the more coupling capacitance to the substrate [4]. Stacking also affects the self-resonance frequency (f_{sr}) of the inductor. This limits the application frequency because the inductor itself can resonate with its parasitic capacitances [2]. In subsequent paragraphs these losses will be discussed in detail, but it is first necessary to present inductance itself.

3.2 Total Inductance

The total inductance of an inductor has two parts, which are its self inductance and mutual inductance. Self inductance is created when an AC (alternating current)

current flows through a conductor and induces a magnetic field. The equation for self inductance in a rectangle shaped conductor derived by Grover is as follows [2]:

$$L_{self} = 2 \cdot l \left\{ \ln\left(\frac{2 \cdot l}{w + t} \right) + 0.5 + \frac{w + t}{3 \cdot l} \right\} \quad (10)$$

In this equation $l = length\ of\ the\ conductor\,(cm)$,

$w = width\ of\ the\ conductor\,(cm)$,

$t = thickness\ of\ the\ conductor\,(cm)$

$L_{self}\,(the\ self\ ind)\ is\ in\ nm$

However, when the width or thickness is increased to a value that doubles the length, this expression is no longer valid. Yet, this can not happen in integrated inductors. Using this equation, it can be proven that the self inductance increases with length and decreases with width if the thickness is held constant. The width's influence on the self inductance is due to the fact that inductance is established by the outer magnetic flux of the conductor [2].

The mutual inductance is a ratio of the flux between conductors 1 and 2 (two windings of the inductor), and the current in conductor 1 [2].

$$M_{12} = \frac{d\psi_{12}}{dI_1}(nm) \quad (11)$$

For two parallel conductors, $M = 2 \cdot l \cdot Q$ (12)

where $l = the\ length\ of\ the\ conductor\,(cm)$

$Q = geometic\ coefficient\ of\ the\ conductor\,(not\ quality\ factor)$

Mutual inductance, unlike self inductance, varies slightly with width, but significantly

varies with spacing. Nevertheless, mutual inductance is much more complicated than self inductance and makes up two of the three parts of the total inductance equation (13) [2].

$$L_{total} = \sum L_{self} + \sum M_{+} - \sum M_{-} \quad (13)$$

The separate parts denote partitions of mutual inductance that contribute to the self magnetic flux and those that degrade the self magnetic flux. Because of this complexity, simplifications have been made to the total inductance equation [2]. For example,

$$L \approx \frac{\mu_o n^2 a^2}{22r - 14a} \quad (14)$$

where $\mu_o =$ permeability of a vacuum

$n =$ number of turns

$r =$ outer radius of the inductor

$a =$ mean radius of the inductor

This approximation is for a square inductor, but it can be applied to other shapes by multiplying this equation by the ratio of the area of the square to the desired shape. Estimates using this approach usually produce errors less than 5% [2].

3.3 Inductor Series Resistance

The series resistance of a conductor is the resistance presented when a current travels through it. The series resistance can be represented as equation (15) [2] :

$$R = \rho' \cdot \frac{L}{A} \quad (15)$$

where $\rho' =$ resistivity/thickness

L = length

A = area

The stacking of metal layers, as suggested in section 3.1, increases the thickness of the conductor, which effectively decreases the resistance. However, this equation is only valid at low frequencies. As frequency increases, the current distribution in the conductor becomes non-uniform because of magnetic field effects, and an increase in series resistance results. These effects are not only a product of the conductor's properties, but are also a product of the persuasion of surrounding conductors.

The magnetic field effect with increase in frequency, due to only the conductor's properties, is called the skin effect [2]. This happens when the increase in frequency causes a magnetic field to cross its cross-section creating a perpendicular force over the current itself. The effect, called Lorenz's force, pushes the current distribution towards the edge of the conductor; and resistance is amplified since the current is now restricted to a smaller part of the total conductor [2]. The skin effect mainly depends on the skin depth, δ, of a conductor. For a typical cylindrical wire, the resistivity with frequency dependence can be written as equation (16) [2]:

$$\rho = \frac{1}{\sigma \cdot \delta} = \sqrt{\frac{\pi \cdot f \cdot \mu}{\sigma}} \quad (16)$$

where σ = conductivity of the conductor$(\Omega \bullet cm)^{-1}$

f = frequency of the AC current(Hz)

μ = magnetic permeability of the conductor (Ω/cm)

The field effects due to external magnetic fields are called proximity effects [2]. The proximity effect and the skin effect act together, but if there is no current flow in a

conductor, one will be produced. As a result, proximity effects happen regardless of an AC current or not. Also, inner coils have an even more heightened resistance due to the fact that the magnetic field gets stronger as it reaches the center of the inductor. Hollow inductors remedy this effect without appreciably decreasing the inductance per area efficiency since the inner windings create the least inductance anyway [2].

3.4 Inductor Substrate Losses

Since only a layer of silicon oxide separates the semiconductor from the substrate in an integrated inductor, two types of substrate effects result. The first type, a magnetically stimulated parasitic, is produced when the magnetic field penetrates the substrate and creates a voltage difference. This voltage difference induces a current that degrades the quality of the inductor. Also, since the induced substrate current is in the opposite direction of the coil current, it reduces the total magnetic field and inductance.

Electrically produced effects are also caused by the voltage difference created. The voltage difference creates a capacitance between the inductor and substrate. This capacitance can lower the self-resonance frequency of the inductor, which takes energy from the coil; and can eventually have it act as a capacitor. Ohmic losses are also created since currents appear in the substrate. Exclusive use of the outermost metal layer can help reduce this capacitance by increasing the distance from the metal to the substrate [2].

3.5 Capacitance Between Metal Windings

Another imperfection associated with the integrated inductor is the parasitic capacitance created between adjacent metal windings. Again, the silicon oxide between the windings acts as an insulator for a metal/silicon oxide/metal, parasitic capacitor. Also, because of the voltage difference between the windings, energy is collected by this parasitic. In the case of a stacked capacitor, this capacitance not only includes the bordering capacitance between metal windings, but the vertical capacitance between stacked metals [2].

3.6 Integrated Inductor Model

The most widely used inductor model is the π model of figure 3.2 [4]. Each of the π model's components is essential to accurate inductor modeling. C_f models the capacitance between adjacent metal strips. R_s represents the series resistance, while L is the coil inductance. C_{sub} is the parasitic capacitance between the metal and substrate, and R_{sub} accounts for the ohmic losses in the substrate created by induced currents. The flaw in the π model exists in the fact that it is a narrowband model [2]. However, the typical model for an inductor only includes the self inductance and the effective series resistance.

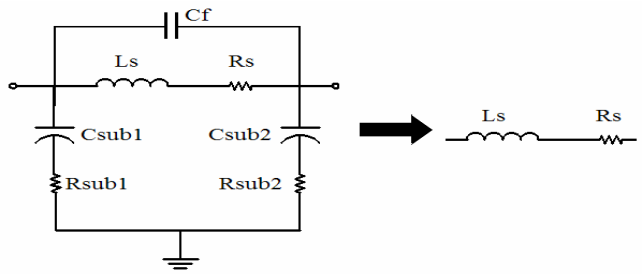


Figure 3.2 π Model of an Inductor

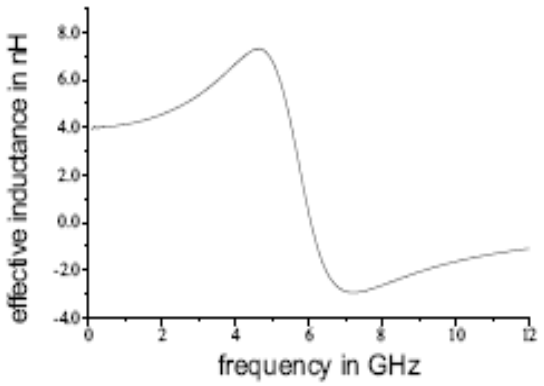


Figure 3.3 Effective Inductance vs. Frequency [4]

Figure 3.3 shows a typical effective inductance versus frequency plot. It is important to mention that the effective inductance reaches zero and becomes negative at some point. The frequency where the effective inductance crosses zero denotes the frequency in which the inductor resonates with its parasitic capacitances (f_{sr}) and no longer behaves as an inductor [4]. This effect was mentioned in previous sections.

3.7 Bondwire Inductors

Since high quality integrated inductors are difficult to implement, bondwire inductors are sometimes used because of their relatively high quality factor. Bondwires have greater surface area per unit length than do spiral inductors, so they have less resistive loss and a quality factor (Q) as much as a magnitude higher than that of a spiral inductor. Also, if placed far above a conducting surface, a bond wire has a significantly smaller parasitic capacitance to ground. Nevertheless, bond wire inductance is hard to control because of its large spread (typically ±20%) and irregular lengths [17]. Usually the varactor must compensate for the large spread of a bond wire inductor, but the large

capacitance tuning range required to handle this spread can cause unwanted fluctuations n the VCO gain. The DC inductance for a bond wire is given as equation (17) [10]:

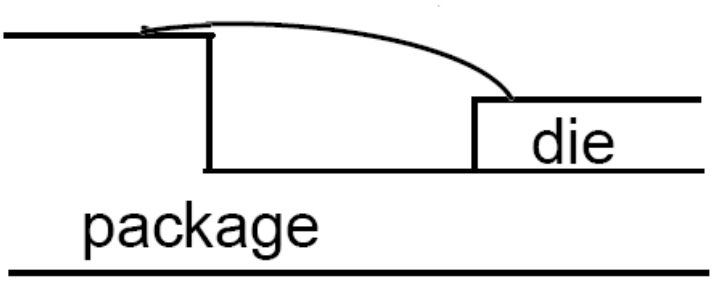
$$L = \frac{\mu_o l}{2\pi}\left(\ln(\frac{2l}{r}) - 0.75\right) (17)$$

where μ_o = permeability in free space

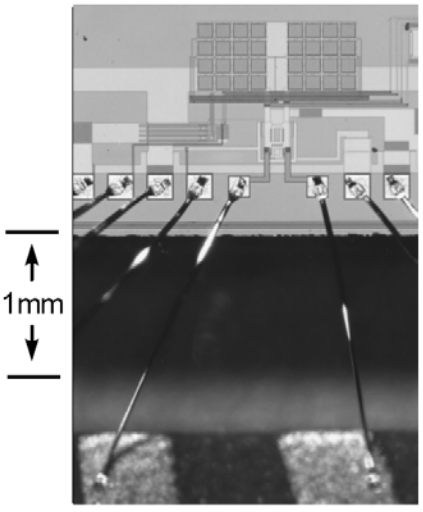
l = length of bondwire

r = radius of bondwire

This gives an inductance of about 2nH for a bond wire of length 2mm. Figures 3.4(a) and (b) help develop a visual image of a bond wire inductor [2].



(a)



(b)

Figure 3.4(a) Bondwire Structure *(b)*Illustration of Bondwire Inductors [22]

3.8 The MOS Varactor

MOS varactors are voltage-controlled capacitors established by the MOS structure and used in LC voltage controlled oscillators. The inductor, L, together with the varactor, C, generates an approximate oscillation frequency of [8]:

$$f_o = \frac{1}{2\pi \cdot \sqrt{LC}} \quad (18)$$

A MOS transistor with the drain, source, and body tied together accomplish a MOS capacitor with a variable capacitance between the gate and source [3]. The variable capacitance is dependent on the voltage between the body and gate, V_{BG}. For a PMOS structured MOS capacitor, when $V_{BG} > |V_T|$ (the threshold voltage of the device), an inversion layer of holes begins to form below the gate-semiconductor interface. Furthermore, when V_{BG} is much greater than $|V_T|$, the device works in strong inversion and behaves like a transistor. Conversely, as V_{BG} becomes increasingly negative, the device enters a mode called accumulation in which electrons flow freely at the gate-semiconductor interface. In both the strong inversion and accumulation regions of the MOS capacitor, the capacitance is measured as equation (19) [3]

$$C_{ox} = \frac{\varepsilon_{ox} S}{t_{ox}} \quad (19)$$

where ε_{ox} = dielectric constant of the oxide

S = transistor channel area

t_{ox} = oxide thickness

Though the strong inversion and accumulation regions boast the same overall effective capacitance, there is a big difference in the overall impedance of each region.

The strong inversion region of a MOS capacitor has a lower parasitic resistance than the accumulation mode region [18]. This is why the accumulation region of a MOS capacitor is often called bad capacitor area. Further explanation of this condition is shown in subsequent sections.

On the other hand, regions between strong inversion and accumulation exist for a MOS capacitor. When the device is in moderate inversion, weak inversion, or depletion, a small amount of mobile charge carriers of the appropriate polarity exist at the gate-semiconductor interface. This occurs when V_{BG} is neither positive nor negative enough to attract an abundance of either type of carriers. In these regions the capacitance is at its minimum. The effective capacitance decreases in these regions because it is then in series with a parallel combination of capacitors C_b and C_i. C_b is realized by the depletion region made of ionized donor atoms and C_i is due to the variation of the number of holes at the gate-semiconductor interface. Both C_b and C_i dominate in their perspective region and are successful in diminishing the effective capacitance [3]. Figure 3.5 illustrates the effects of C_b and C_i in the depletion, weak inversion, and moderate inversion regions.

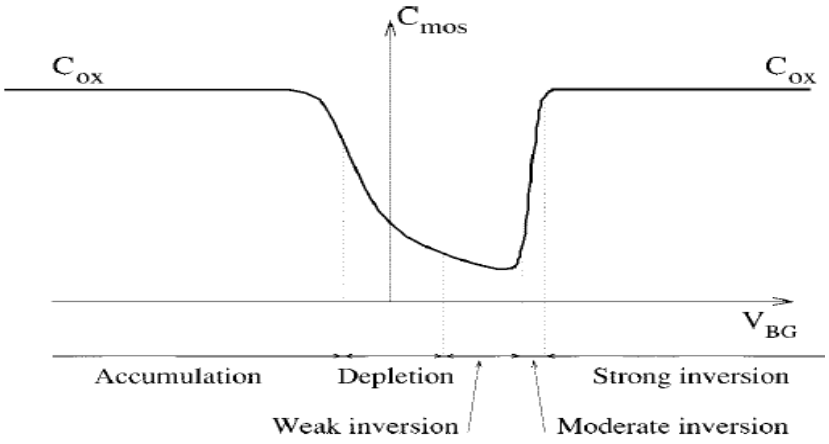


Figure 3.5 Capacitance vs. MOS Operation Region [3]

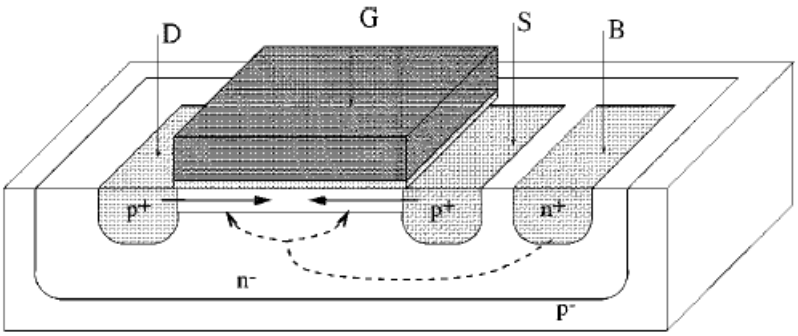


Figure 3.6 Charge Carrier Patterns [3]

Figure 3.6 shows the pattern of the charge carrier paths. The charge carrier path of the device in strong inversion is represented with the solid arrows, and the dashed lines represent the paths in depletion and accumulation. C_b dominates in the depletion region while C_i dominates the moderate inversion region, but neither of the parallel capacitances dominates in weak inversion [3]. These are unwanted effects of the MOS capacitor.

3.9 Inversion-Mode MOS Varactor

When the MOS capacitor is used in a VCO the effective capacitance is non-uniform throughout the signal period. This is because there is often a large signal at the gate of the capacitor (the output), and the device is subjected to the accumulation region of the MOS capacitor. Since this is the case, tuning becomes extremely complicated. A more uniform capacitance is obtained when the body is disconnected from the source-drain connection and attached to the supply rail [3]. Given that the capacitance is still a function of V_{BG}, this ensures that the device cannot enter accumulation and is always working in weak, moderate, or strong inversion.

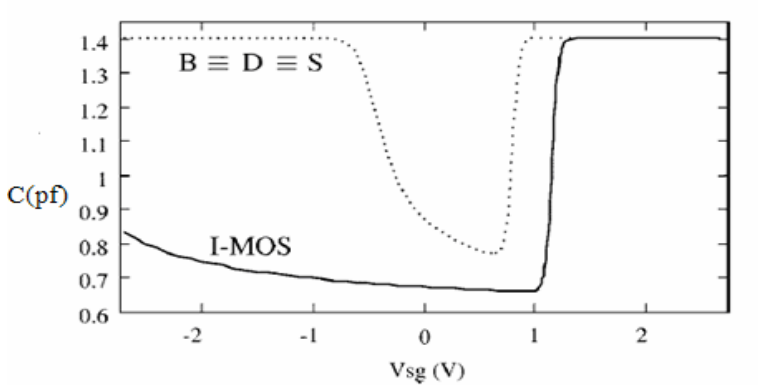


Figure 3.7 C-V Curve for an I-MOS Varactor [3]

Figure 3.7 compares the effective capacitance of a regular PMOS capacitor and an inversion-mode PMOS capacitor (I-MOS). Again, since the body is connected to the supply voltage and V_G cannot exceed this value, the I-MOS device is not able to enter its accumulation mode. Also, an NMOS device with the body tied to ground can be used as an inversion-mode capacitor [3]. The NMOS configuration offers less parasitic resistance, but is more susceptible to substrate noise.

3.10 Accumulation-Mode MOS Varactor

The accumulation-mode MOS varactor is perhaps more appealing than the inversion mode MOS varactor because of its wider tuning range. A PMOS accumulation mode varactor (A-MOS) can be attained if the strong, moderate, and weak inversion regions are never reached. This is accomplished by the restraint of holes in the channel by removing the p^+ doped drain and source. They are replaced with n^+ doped body contacts as shown in figure 3.8(a) on the next page, which disallow these regions. The n^+ contacts also prohibit extra parasitic capacitance between the drain and substrate, which increases the tuning range, and still exhibits a fairly low parasitic resistance [3].

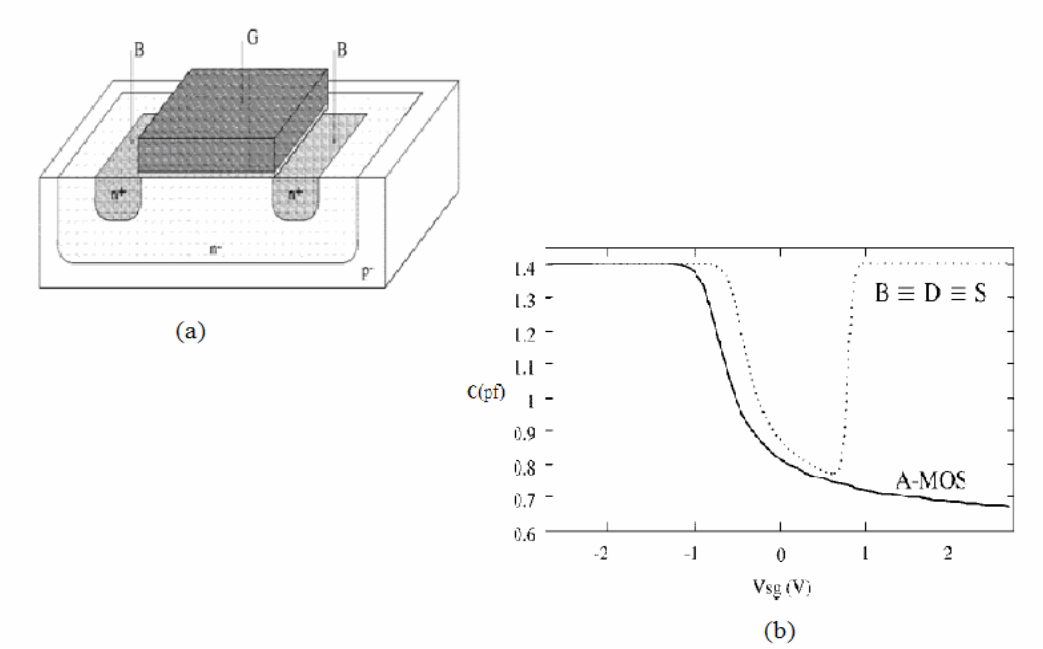


Figure 3.8 A-MOS Varactor Characteristics [3]

In the next illustration, figure 3.8(b), the A-MOS capacitor is compared to the conventional MOS varactor with body, drain, and source tied together. As seen, at V_G = 0 the device is already depleted and on the verge of accumulation with just a slightly positive voltage applied at the gate. Also, thermally generated holes are ineffective because radio frequencies are well above hole generation frequencies [3].

3.11 Varactor Parasitic Resistance

Since the model for a MOS varactor is often reduced to just a variable capacitor in series with a variable resistor, seen in Figure 3.9, it is important to understand some characteristics of this parasitic resistance. The approximation for this resistance when the device is in strong inversion is rather straightforward and is as equation (20) [3]:

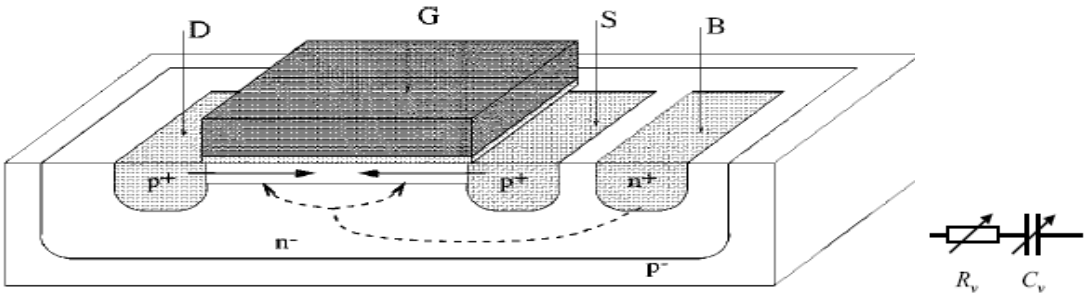


Figure 3.9 MOS Varactor Equivalent Circuit [3]

$$R = \frac{L}{12K_p W(V_{BG} - |V_T|)} \quad (20)$$

where L = length of the device

W= width of the device

K_p= the gain factor of the device

As V_{BG} decreases and the device starts to transition from strong to moderate inversion, the parasitic resistance increases. However, it never becomes infinite as the equation implies when V_{BG} equals $|V_T|$. Throughout moderate inversion the parasitic resistance becomes larger. Even though the holes present at the interface gradually decreases, C_i (the capacitance related to the amount of holes) is still much larger than C_b. However, as the device enters weak inversion, the modulation of the depletion region becomes as significant as the injection of holes; and C_b grows to be equal and larger than C_i. Parasitic resistance is now decreasing because it depends on the resistive losses of electrons traveling from the body to the interface; and electron mobility is thought to be about two and a half times higher than hole mobility. Because of this, an accumulation mode varactor's parasitic resistance is competitive with that of an inversion mode varactor. Yet, the resistance might never become as low as that in the strong inversion region [3].

In addition, there is also a resistance associated with the gate of a transistor. In order to develop the necessary capacitance for use in a VCO, the gate area has to be large. Since this resistance is proportional to the square resistance of the gate and the number of squares, a large gate area is a problem in lowering this resistance. To resolve this problem, the varactors are laid out in the same form as transistors. The gate is broken up into smaller gate fingers and put in parallel. Figure 3.10 is an example of such a layout[4].

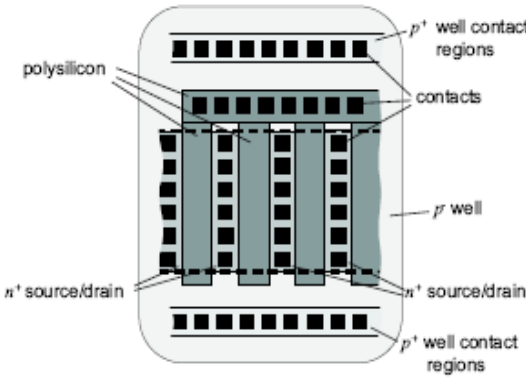


Figure 3.10 Example Varactor Layout [4]

Chapter 4 LC-VCO Topologies

There are several topologies aimed at realizing the active pair that generates a negative resistance which is required to sustain oscillations in a VCO. The selection of an active pair topology usually depends on the specifications of a particular VCO design, and may also depend on process technology. In other words, the designer must evaluate given restrictions on phase noise, power consumption, and other VCO parameters, and choose the topology that best accommodates the most vital specifications. In the following sections, the three main topologies (NMOS only, PMOS only, and complimentary NMOS and PMOS) and why each might be helpful or harmful in a particular design are presented.

4.1 NMOS Only Topology

As the name suggests, the NMOS only VCO topology uses only NMOS transistors to accomplish its active pair. Figure 4.1 is an illustration of a conventional NMOS only voltage controlled oscillator.

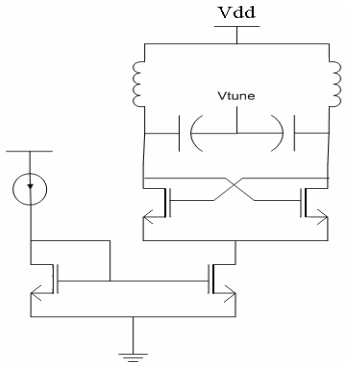


Figure 4.1 NMOS Only VCO

The NMOS only voltage controlled oscillator is perhaps the easiest topology to implement and is used when the specifications such as phase noise are moderate. The NMOS only topology has the advantage of a high transconductance, (g_m), per unit area due to the fact that electron mobility is larger than hole mobility. Hence for a given negative resistance, an NMOS transistor can be smaller than a PMOS transistor. This suggests that an NMOS only topology is slightly better for power consumption than its PMOS counterpart because it requires less current. Also due to the smaller area of the NMOS transistor, a higher tuning range is achieved for transistors with the same transconductance [1]. This concept is discussed in detail in a later section. Despite the preceding accomplishments, it is well documented that PMOS transistors have lower flicker noise density than NMOS transistors [12]. This is important because flicker noise is one of the main components of phase noise in a voltage controlled oscillator [1]. In addition, the PMOS only topology can help filter voltage supply noise, which is FM modulated to become another component of phase noise [12]. The PMOS only topology is able to isolate the noise caused by the supply through the impedance of its tail current source [12]. Nevertheless, NMOS only topologies are still implemented because of their ease and cost efficiency.

4.2 PMOS Only Topology

The PMOS only topology of figure 4.2 is used when the need for lower phase noise is present and parameters such as power consumption and tuning range are relaxed. For a consistent g_m, PMOS transistors are required to be larger than NMOS transistors.

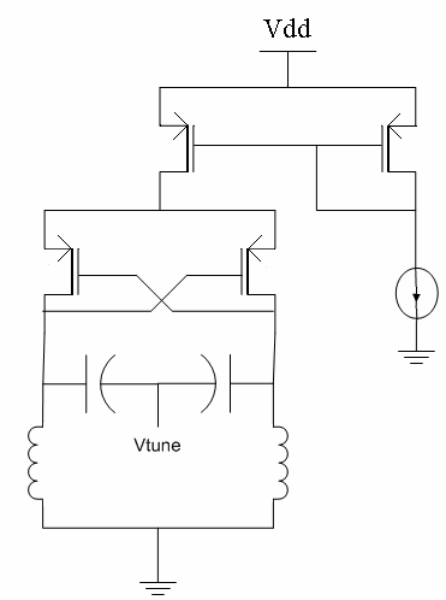


Figure 4.2 PMOS Only VCO

This can inhibit tuning range and require more power dissipation for the PMOS only VCO. However, when phase noise is a crucial issue, the PMOS only topology is extremely useful. Although the most straightforward observation is that PMOS transistors have lower flicker noise than do NMOS transistors, there are other advantages to a PMOS only topology. The PMOS only topology generates less drain current thermal noise for the same g_m as the NMOS only topology [12]. The drain current thermal noise for NMOS transistors is higher because velocity saturation is more dominant in NMOS transistors. Still, drain current thermal noise is a main component of phase noise in voltage controlled oscillators, and is diminished by the use of PMOS transistors.

Another reason the PMOS only topology is used is illustrated in figure 4.3. The PMOS only topology is able to reject voltage supply noise which is otherwise FM modulated into the oscillator feedback loop [12]. The illustration shows the importance of this rejection and how it affects the DC level at the output of VCO.

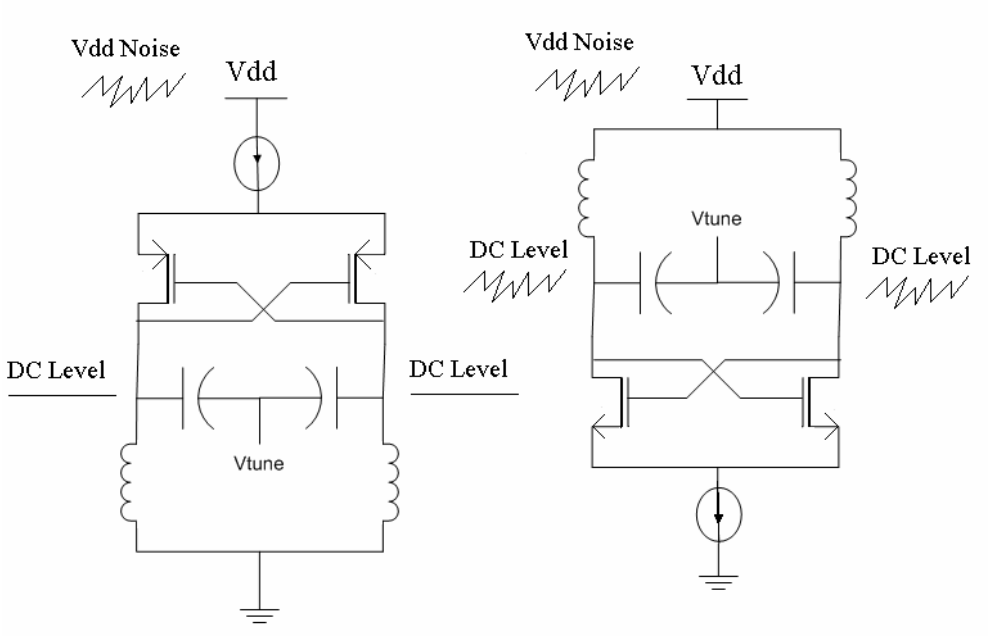


Figure 4.3 Voltage Supply Rejection Illustration

In addition, the PMOS topology is able to decrease noise associated with the bias of the transistors [12]. All these properties make the PMOS only topology excellent for phase noise minimization.

4.3 Complementary (NMOS/PMOS) Topology

Perhaps a more attractive alternative than either the NMOS only or PMOS only topology is the complimentary topology which uses both NMOS and PMOS transistors. The NMOS/PMOS complementary topology, as shown in figure 4.4, is used when there is enough voltage headroom available to stack transistors. However, with threshold voltages lowering more gradually than minimum channel lengths, implementing this topology is becoming difficult. Furthermore, increasing the sizes of the transistors to lower the saturation voltage provides further design problems, which will be discussed

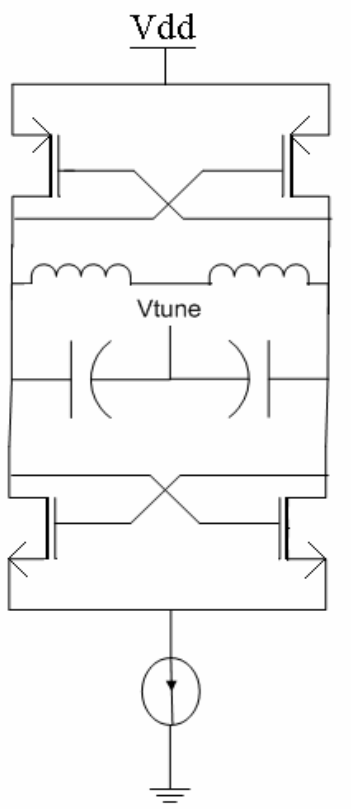


Figure 4.4 Complementary NMOS/PMOS Topology

later in the section. Yet, when executed successfully, the complementary topology can display several advantages.

The first and most obvious advantage of using a complementary pair is lower power consumption. This is because current is reused in the circuit and a tail current source is used at the discretion of the designer. The complementary pair only requires about half the start-up current of the other topologies [1]. Yet, when no tail current source is used, the designer must make sure the cross-coupled transistors are of sufficient sizes for proper oscillation. In this case, the designer must be careful in modeling the parasitics of the voltage controlled oscillator. The neglect of a parasitic on any level (simulation, design, or package) can overpower oscillations, and because of the lack of a

current source, the designer can not raise the power. Some designers slightly increase the size of the pair to make sure there is a sufficient amount of current for startup. However, enhancing the sizes of the cross-coupled pair diminishes the tuning range. For example, the oscillation frequency is calculated by equation (18):

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (18)$$

$$C_{ox} = \frac{\varepsilon_{ox} A}{d} \quad (21)$$

where ε_{ox} = dielectric constant of gate oxide

A = area

d = distance between conductors

As seen in equation (21) for oxide capacitance (C_{ox}) [18], increasing the size (area) of the transistors raises the effective oxide capacitance of the structure. This can be compared to adding a fixed capacitance to each end of the tuning range. The added capacitance works to reduce the oscillation frequency as observed from equation (18). Still, when well planned, the complementary topology can be very effective in reducing power consumption.

Another advantage of the complementary design is lower phase noise. From a simplified version of the phase noise equation (1) in chapter 2 [1],

$$L(f_m) = 10\log\left[\frac{2FkT}{P_s}\left(\frac{f_o}{2Q_L f_m}\right)^2\left(1+\frac{f_k}{f_m}\right)\right] \quad (1)$$

it can be observed that phase noise and power consumption are inversely proportional. In other words, the more power used, the lower the phase noise. Since the complementary pair only requires half the current of other topologies, the tail current can be raised with

less of a concern for power consumption. Furthermore, it can also be argued that the phase noise is lowered through the symmetry of the complementary topology. Since the complementary topology can offer a more uniform swing due to the use of both NMOS and PMOS transistors, the phase shift introduced during the rising edge is more similar to the phase shift seen in the falling edge (compared to the other topologies)[20]. So by using the NMOS/PMOS complementary pair, the designer must trade simplicity for precision.

Chapter 5 LC-VCO Testing and Results

In this chapter the test procedure of a fully integrated 1.8 GHz LC-VCO developed in a 0.35 µm process is presented. The steps taken in the VCO testing include the packaging of the die, the development of a test-board, and the actual testing of the chip. Parameters such as power consumption, phase noise, and tuning range are capable of being tested with the available equipment, and can be compared with simulation results. Also, valuable test experience is gained when encountering, contemplating, and solving problems that arise during the testing process. A diagram of the tested LC-VCO is shown below in figure 5.1. The black boxes denote the padded inputs and outputs of the VCO chip. The square at the bottom represents the 20 pin die and its pad orientation (pads vg1, vg2, and vcnt are not used).

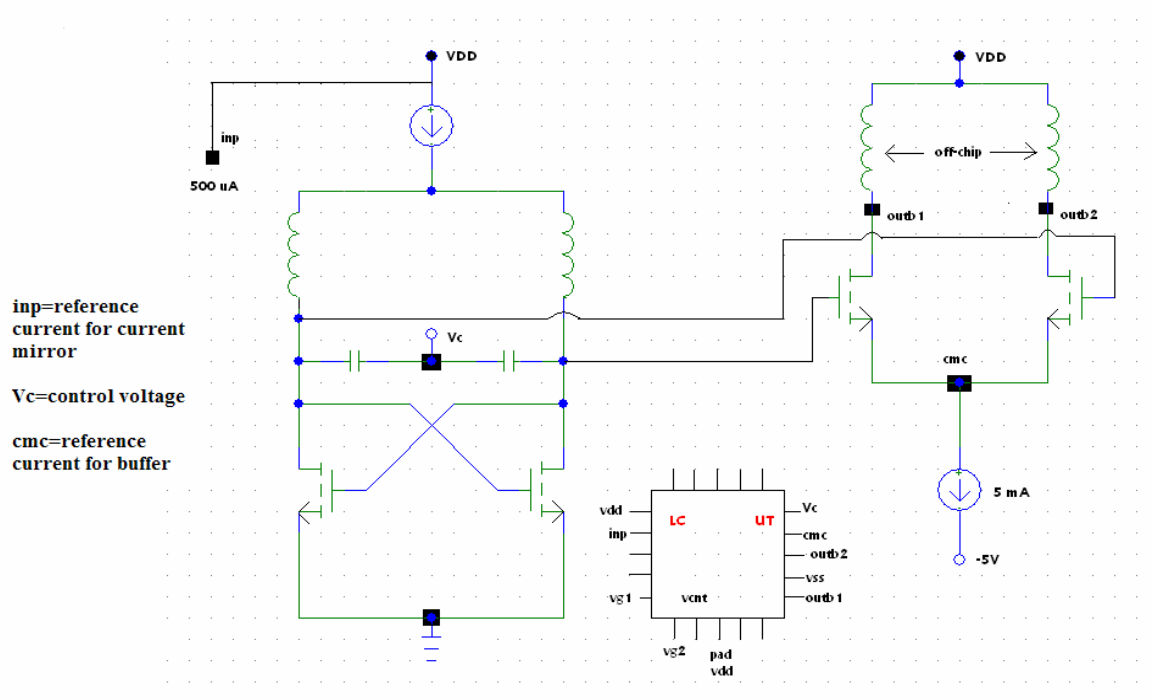


Figure 5.1 Schematic of a Fully Integrated 1.8 GHz LC-VCO Fabricated in a 0.35 µm Process with Pads Shown

5.1 VCO Characteristics

First, it is important to analyze the VCO being tested. The voltage controlled oscillator, shown in figure 5.1, has a voltage rail of 3.3 V, and uses an NMOS only topology. The tail current source that supplies the tank and active pair is a wide swing cascode current mirror, which requires a 500 μA reference. The VCO tank consists of a symmetrical, octagonal inductor with a value of 5.1 nH. The inductor, taken from ASITIC (Analysis and Simulation of Spiral Inductors and Transformers for Integrated Circuits), has an outer radius of 200 μm and contains four turns. The tank also employs body driven varactors to complete the NMOS only pair. Also, to isolate the circuit from external effects, a differential buffer is used as opposed to a source follower.

5.2 The Test Board and VCO Packaging

The test board, shown in figure 5.2, is comprised of an FR4 substrate with the ground plane on the extreme right side of the board. It includes JFET current sources for the current bias of nodes *inp* and *cmc*, arrangements to test the currents, and resistor sockets for interchanging JFET bias resistors. It also provides package-on-board capability and on-board supply filtering. The package, which is optimized for frequencies in the 2 GHz range, is a 24-pin quad flat package (QFP). The die was placed in the package using apoxy and bonded to the package with the K&S 4523A Digital Series wire bonder. The test set-up, also shown below in figure 5.3, features a dual power supply for the voltage rail and control voltage, and a spectrum analyzer with an aptitude of 3 GHz.

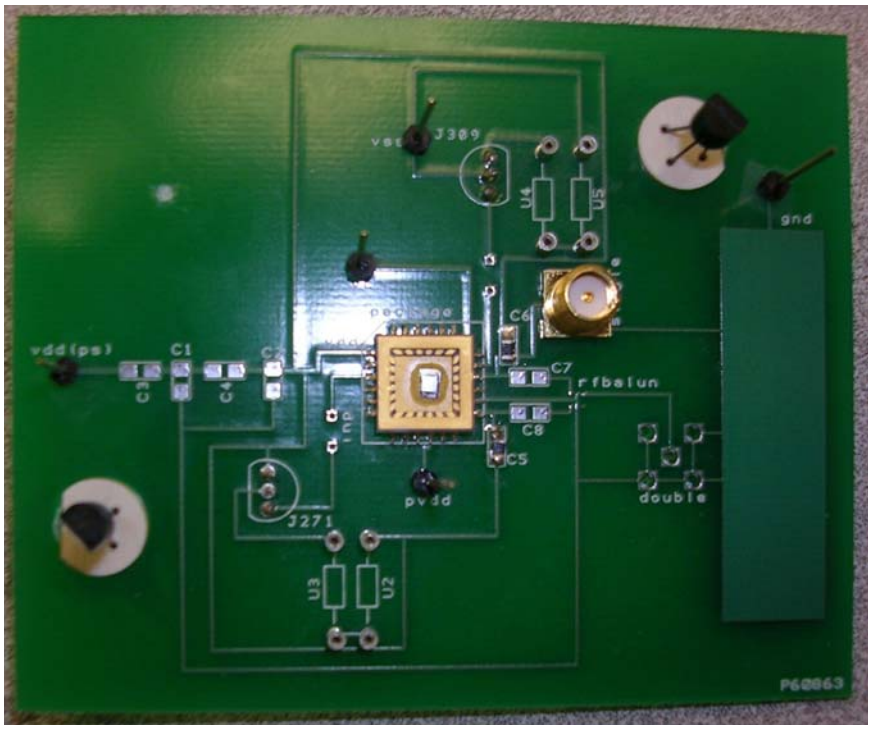


Figure 5.2 LC-VCO Testboard

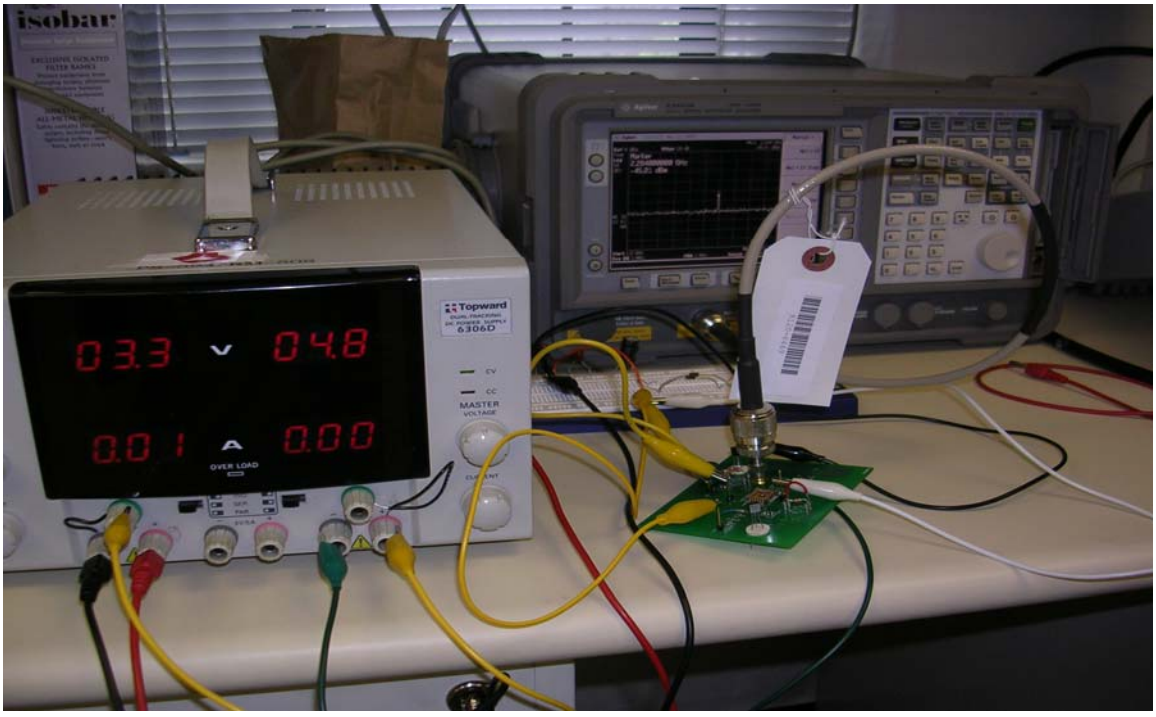


Figure 5.3 Test Setup for LC-VCO

5.3 Test Procedure and Results

Despite initial discouragement due to the extreme attenuation of what appeared to be an output signal, recent findings in the test procedure appear promising. After observing a frequency spike at 2.23 GHz, but -48 dB down, all of the bias voltages and currents were checked. This search found a non-existent bias current for the buffer pad, *cmc*. The next step was changing JFETs and checking connections, but these procedures did not help. However, while taking a closer look at the package under the microscope, it appears that there is a bad bond at that pad. Still, the output was unexplained. What is believed to be occurring is the coupling of the un-buffered output signal through a C_{gd} or some capacitance to the buffer output. This would explain a signal at the buffer output that is somewhat tunable. Figures 5.4 and 5.5 show the output signals at a control voltage of midsupply and vdd. Despite this, the testing is still in process.

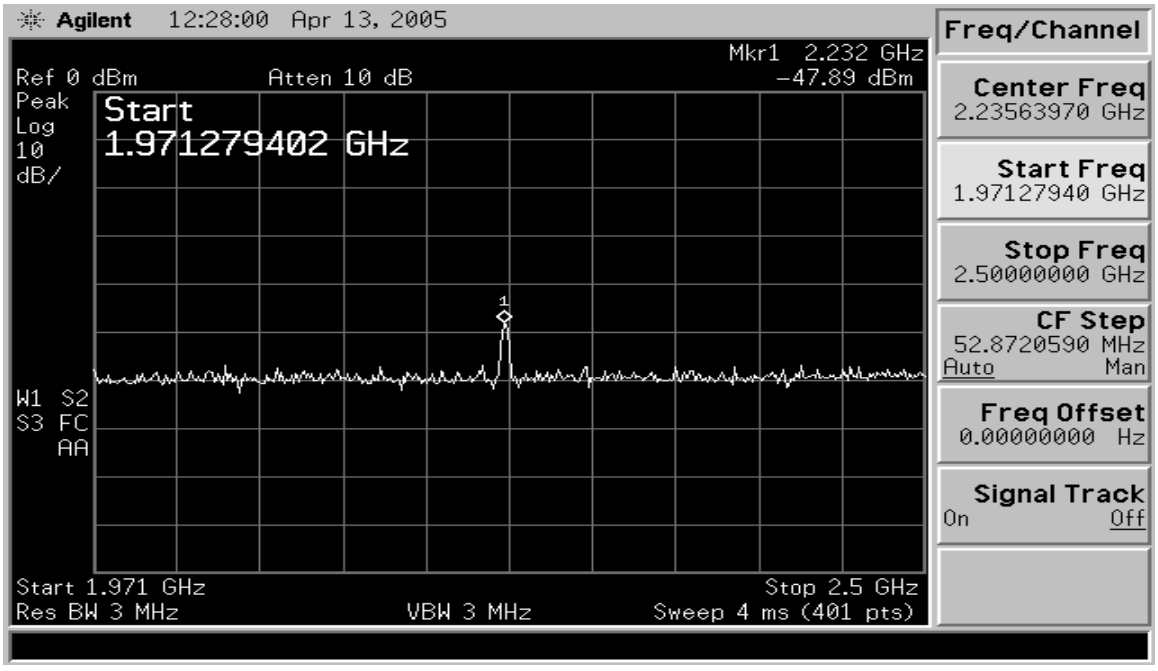


Figure 5.4 Output at Minimum Control Voltage

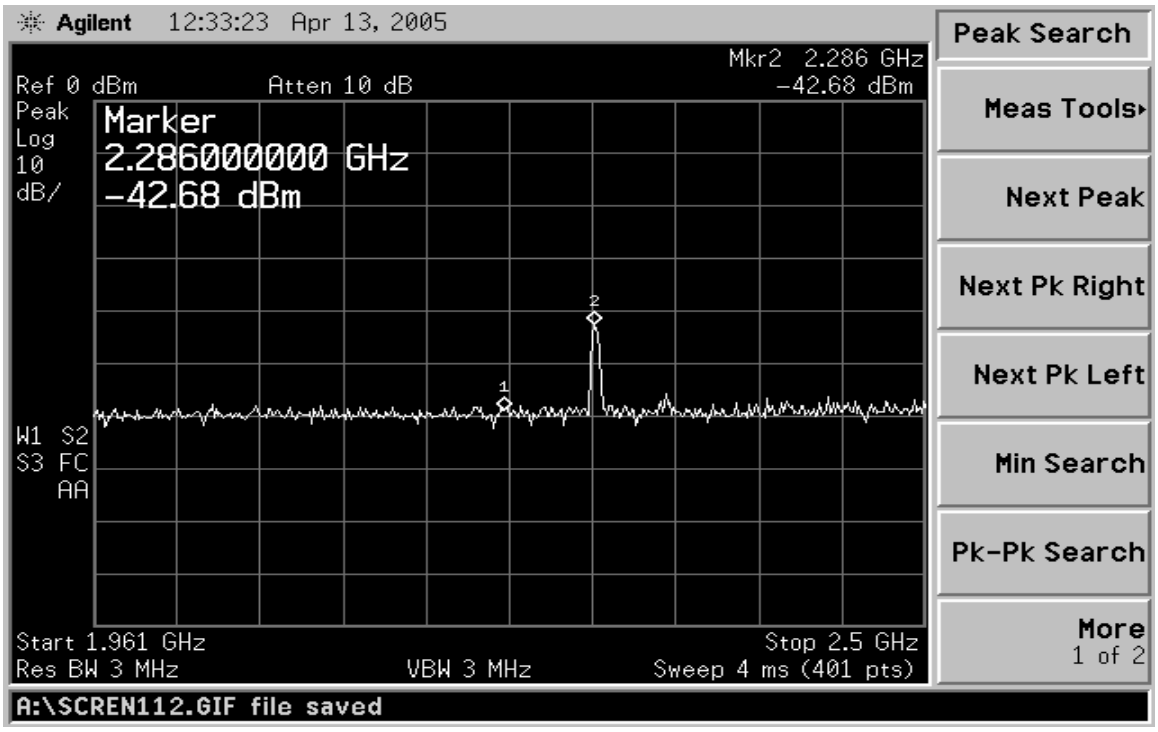


Figure 5.5 Output at Maximum Control Voltage

Chapter 6 Design of a 2.4 GHZ LC-VCO

Another critical element in comprehending the characteristics of an LC-VCO is the design of one. In the previous chapters, a fundamental understanding of the components and structures of a VCO are studied. Here, the complete design process of a 2.4 GHz LC-VCO for fabrication in a 0.18 μm, 1.8 V CMOS process is presented and analyzed. Also, the simulation results of the VCO are provided where they are appropriate. In order to efficiently describe the design process, the VCO is divided into three parts, which are the current source, LC tank, and the active pair topology. Figure 6.1 illustrates the different sections of the VCO for the reader's clarity. Section 1 is the wide-swing current source, section 2 is the LC-VCO tank, and section 3 is the VCO active pair topology.

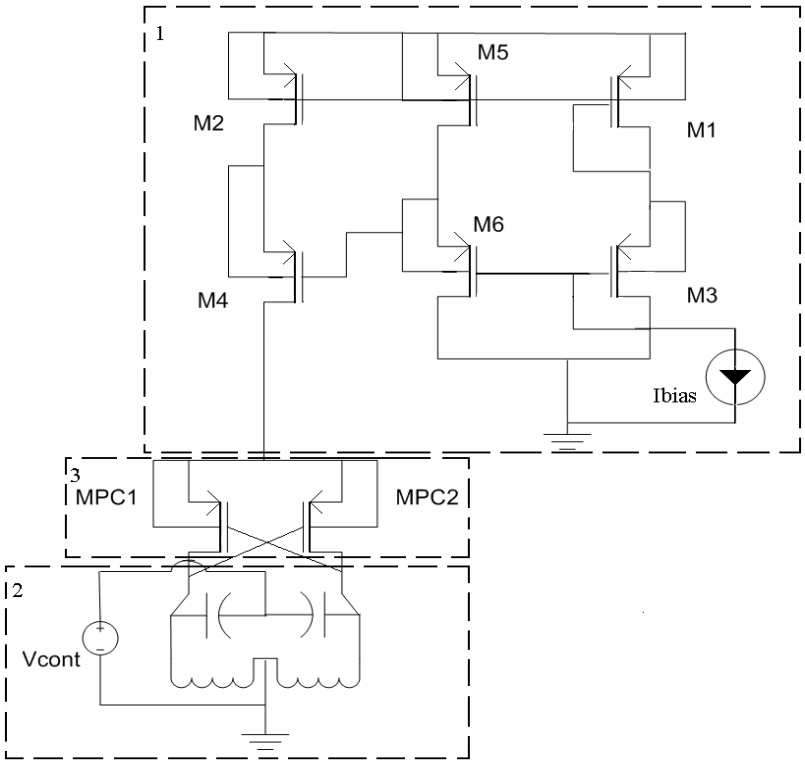


Figure 6.1 Schematic of Design Blocks of the LC-VCO

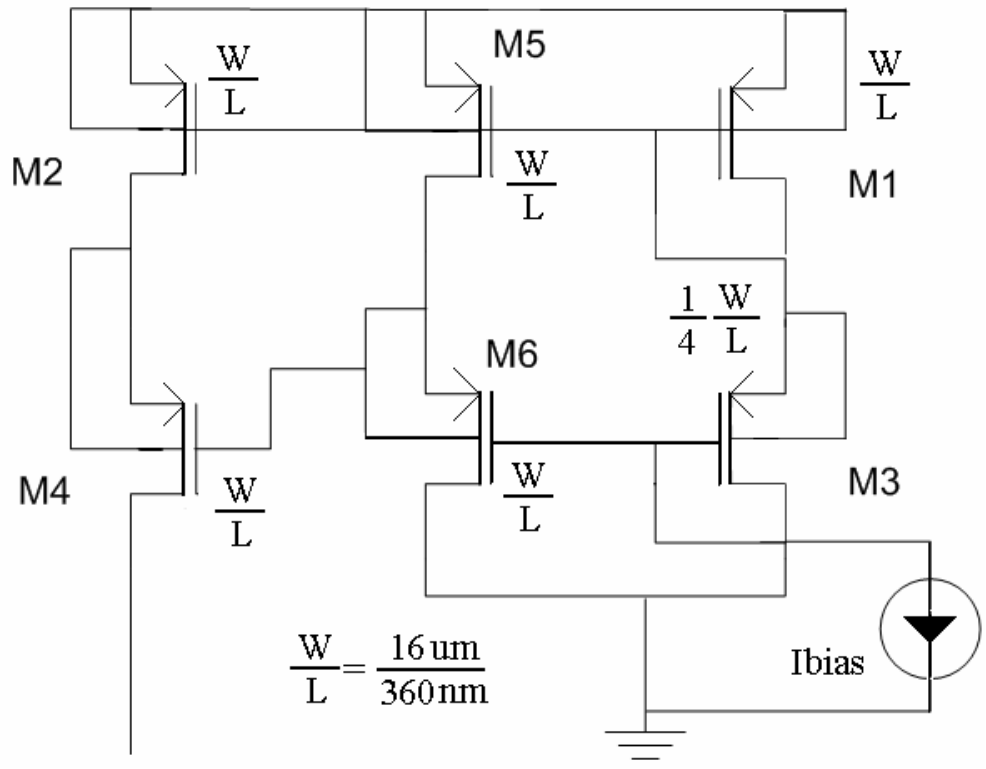


Figure 6.2 Wide-Swing Cascode Tail Current Source

6.1 The Tail Current Source

For this design, a wide-swing current mirror was used as the tail current source. The wide-swing cascade, in figure 6.2, sources 3-4 mA with a reference current of 400-540 µA. The output impedance of the wide-swing cascode is much higher than that of a simple current mirror because of the stacking of transistors. It boasts an output resistance of $R_{out} \approx g_{m4} r_o^2$ [18]. This is important for the generation of a constant bias current, which insures that the VCO opposes changes in activity due to voltage fluctuation. Figure 6.3 shows the current source's output current variation with a 10k Hz, 180mV peak-to-peak sin wave tied to the supply simulating vdd fluctuations. As seen, the tail current variation is less than 0.02 mV peak-to-peak.

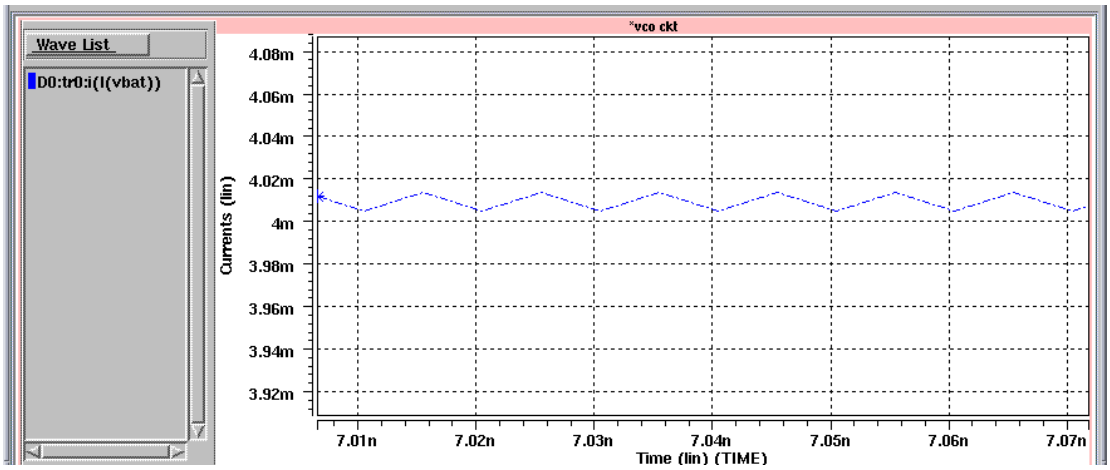


Figure 6.3 Tail Current Variation with 10kHz 180mV pk-pk Sin Wave Disturbace

Another advantage of the current source is its decreased output voltage. Since the gate of transistor M_4 is reduced to $2V_{DSsat} + V_T$, M_2's drain voltage becomes a V_{DSsat} [18]. This is done by sizing transistor M_3 such that its source-gate voltage is $2V_{DSsat}+V_T$. M_6 then acts as a level shift to bias the gate of M_4 at $2V_{DSsat} + V_T$ for a total output voltage of $2V_{DSsat}$ [21]. More voltage headroom gives the designer more flexibility with transistor sizing and topology capability. Disadvantages to this configuration include the use of more transistors.

6.2 The LC Tank Design

The next section of the design consists of the LC resonator. The resonator's quality has a direct effect on most of the characteristics of a VCO. More specifically, the quality of the inductor is extremely imperative because it dominates the quality factor of the varactor, since it is usually at least ten times (a magnitude) smaller. The inductor chosen for this design is a single-ended inductor taken from the 0.18 μm design kit, and is approximately 2.4 nH. The inductance is changed by varying the number of turns, n, in

the metal structure. Choosing this inductor allows the designer to perform a pad-to-pad LVS (layout versus simulation) check of the design. Also, selecting this inductor employs an excellent model which has been tested and developed by the vendor and is provided through MOSIS. In other words, an actual inductor was placed on a wafer and characterized for preciseness. This provides an advantage over an inductor imported from ASITIC because a pad-to pad LVS check is unattainable. Also, when an inductor is transferred from ASITIC to a Cadence environment, it first has to be formatted; and only the metal layers themselves are transferred. The designer must then depend on the ASITIC inductor model which is based on equations rather than experimental results. However, ASITIC provides symmetric inductor designs which are thought to be advantageous for differential applications such as these.

The varactor used for this design, whose characteristics are shown in figure 6.4, is an accumulation-mode varactor also taken from the 0.18 μm design kit. Its model is as well formulated from experimental results. Since varactor quality is often ignored, productive varactors have a linear output with a low parasitic resistance. The parasitic resistance presented by a large gate area is combated by stacking structures in parallel, as suggested in figure 3.10. The varcator arrangement for this design is a fifty branch, three group varactor. This means that each varactor is split into three groups of fifty gate fingers all tied in parallel. Since the varactor is a variable capacitance, the actual value is evaluated based on several variables. The HSpice model on the next page, figure 6.5, provides equations and means of obtaining each variable needed for the varactor capacitance and each of its parasitics. The varactor capacitance is specified as C_{gate} given that it is located between the gate and source of the structure.

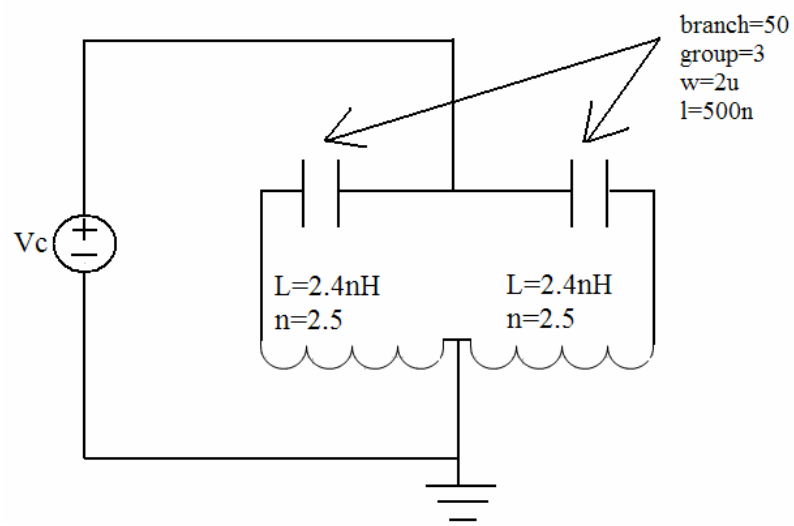


Figure 6.4 LC Tank Schematic

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```
.LIB RF_MVAR
*************************************************************************
* MOS VARACTOR MODEL :
*
*
*  HSPICE LEVEL 49:
*
*     ## library files:
*
*
*      Model name      L(um)     Group(g)   Branch(b)   Unit Cell
*      ------------------------------------------------
*       moscap_rf       0.5      1   8      10  50         24
*       moscap_rf33     0.5      1   8      10  50         24
*      ------------------------------------------------
*************************************************************************
.subckt moscap_rf gate bulk gnode b=50 g=3
.param dt='temper - 25'
.param Cgmin='((0.3055*b+0.0226)*g+0.04)*1.0e-14*(1+1.449e-4*dt+2.589e-7*(pow(dt,2)))'
.param dCg='((0.388*b-0.14)*g+0.08)*1.0e-14*(1-1.453e-4*dt+1.762e-8*(pow(dt,2)))'
.param dVgs='-0.08697*(1+3.484e-4*dt)'
.param Vgnorm='0.38*(1+1.053e-3*dt)'
.param Area='(1.04*b+2.54)*(3.12*g+1.38)*1.0e-12'
.param Peri='(2*(1.04*b+2.54)+2*(3.12*g+1.38))*1.0e-6'
Lgate gate 3 '(((6.8102/b)-0.9093)*g+46.312)*1.0e-12*l_mvfac'
Rgate 3 4 '((((0.9667/b)+0.0189)*g)+(2.6294/b)+0.2826)*rnpolys_mvfac' 4.963e-3 -5.684e-6
Cpar 4 5 '1.507427*b*g*1.0e-15*cmv_fac' 1.449e-4 2.589e-7
Cgate 4 5 '(Cgmin+dCg*(1.0+tanh((v(4,5)-dVgs)/Vgnorm)))*cmv_fac'
Rsd 5 9 '((((-16.648/b)-0.3366)/(g*g))+(((49.102/b)+0.9459)/g)-(4.8613/b)+0.3796)*rm1_mvfac' 4.963e-3 -5.684e-6
Lsd 9 bulk '(((6.8102/b)-0.9093)*g+46.312)*1.0e-12*l_mvfac'
Dnwpsub 6 5 MVNWDIO AREA=Area PJ=Peri
Csub 6 gnode '(1.91455*((1.04*b+2.54)+(3.12*g+1.38)))*csub_mvfac*1.0e-15'
Rsub 6 gnode '(5500/((1.04*b+2.54)+(3.12*g+1.38)))*rsub_mvfac'  9.277e-3 1.014e-4
.ends moscap_rf

.subckt moscap_rf33 gate bulk gnode b=25 g=4
.param dt='temper - 25'
.param Cgmin='((0.2668*b+0.0336)*g+(0.015091*b-0.12469))*1.0e-14*(1+9.459e-5*dt+3.469e-7*(pow(dt,2)))'
.param dCg='((0.201*b-0.049)*g+0.14)*1.0e-14*(1-1.076e-4*dt-1.962e-7*(pow(dt,2)))'
.param dVgs='-0.1758*(1+1.38e-3*dt)'
.param Vgnorm='0.55*(1+1.45e-3*dt)'
.param Area='(1.04*b+2.54)*(3.12*g+1.38)*1.0e-12'
.param Peri='(2*(1.04*b+2.54)+2*(3.12*g+1.38))*1.0e-6'
Lgate gate 3 '(((6.8102/b)-0.9093)*g+46.312)*1.0e-12*l_mvfac'
Rgate 3 4 '((((0.9667/b)+0.0189)*g)+(2.6294/b)+0.2826)*rnpolys_mvfac' 4.963e-3 -5.684e-6
Cpar 4 5 '1.160281*b*g*1.0e-15*cmv_fac' 9.459e-5 3.469e-7
Cgate 4 5 '(Cgmin+dCg*(1.0+tanh((v(4,5)-dVgs)/Vgnorm)))*cmv_fac'
Rsd 5 9 '((((-16.648/b)-0.3366)/(g*g))+(((49.102/b)+0.9459)/g)-(4.8613/b)+0.3796)*rm1_mvfac' 4.963e-3 -5.684e-6
Lsd 9 bulk '(((6.8102/b)-0.9093)*g+46.312)*1.0e-12*l_mvfac'
Dnwpsub 6 5 MVNWDIO AREA=Area PJ=Peri
Csub 6 gnode '(1.91455*((1.04*b+2.54)+(3.12*g+1.38)))*csub_mvfac*1.0e-15'
Rsub 6 gnode '(5500/((1.04*b+2.54)+(3.12*g+1.38)))*rsub_mvfac' 9.277e-3 1.014e-4
.ends moscap_rf33
.lib 'rf018.l' DIO_MVNWDIO
.ENDL RF_MVAR

.LIB DIO_MVNWDIO
.MODEL MVNWDIO D (                                LEVEL  = 3
+ IS     = 6.50E-7         RS     = 1.0E-10        N      = 1.03
+ BV     = 14.75           IBV    = 1E-3           IK     = 1E20
+ IKR    = 1E10            JSW    = 9.75E-13
+ CJ     = '1.337566E-4*cj_mvfac'                  PB     = 0.5846489
```

Figure 6.5 HSpice Model of the Varactor

6.3 The Active Pair

The active pair that cancels the effective parallel resistance created by the LC tank is the last block of the VCO. There are several topologies that achieve the negative resistance required to achieve oscillations, but for this design the PMOS only topology was chosen. Because of the extra voltage headroom contributed by the wide-swing cascode, the first thought was to implement the complementary topology. However, through many comparisons in simulation, the PMOS only topology's simplicity outweighed the complementary topology's slightly better performance in power dissipation. Also, since the wide-swing cascode provides excellent isolation from supply noise through its high output impedance, the PMOS only topology's superior phase noise performance complements this attribute. The PMOS pair is kept as small as possible to improve the tuning capabilities of the VCO. This is a trade-off because for a fixed current, increasing the size lowers V_{Dsat}, which makes it easier to keep every transistor saturated. This is seen in equation (22) where β is proportional to transistor size [21].

$$I_D = \frac{\beta}{2}(V_{Dsat})^2 \quad \text{where the size is proportional to} \quad (22)$$

The cross-coupled pair is shown in detail in figure 6.6.

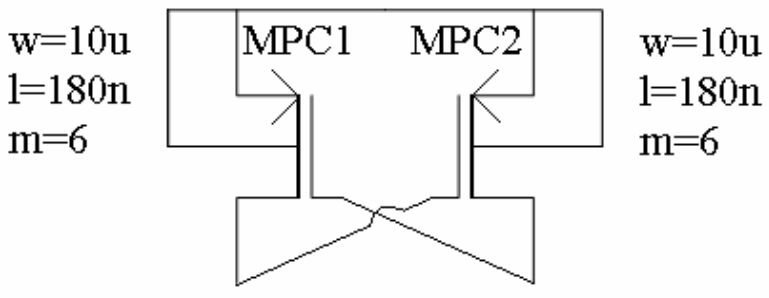


Figure 6.6 The Active Pair Schematic

6.4 Integrated Circuit Layout

Again, the design was executed in a 0.18 µm technology, with the inductors and varactors gathered from the 0.18 µm design kit. This enables a pad-to-pad LVS and provides accurate inductor and varactor models, which are important for a designer with little experience. In another existing design, the transistors used for the cross-coupled pair as well as the transistors used for the tail current source were laid out using the common centroid technique to improve transistor matching. The varactor layout, shown in figure 6.7, is consistent with the varactor schematic. Each varactor is made up of 3 groups of 50 gate fingers tied in parallel. The inductor layout, shown in figure 6.8, utilizes exclusively metal 6 (the outermost metal layer). As discussed in chapter 3, this procedure is effective in lowering substrate capacitance, but possesses a higher series resistance than that of a stacked capacitor. Each of these components is successfully implemented in the improved design described in this chapter.

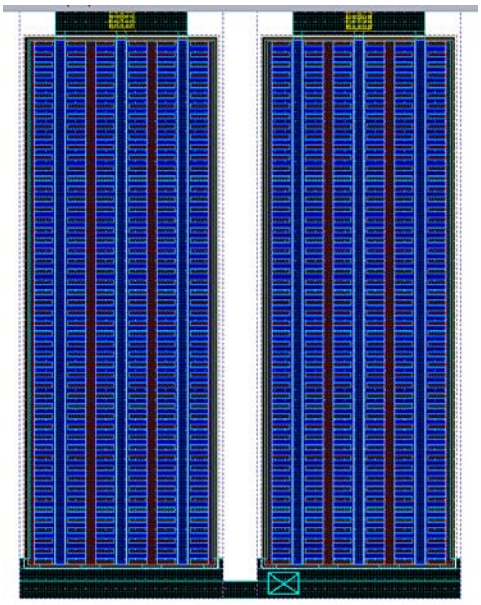


Figure 6.7 Varactor Layout

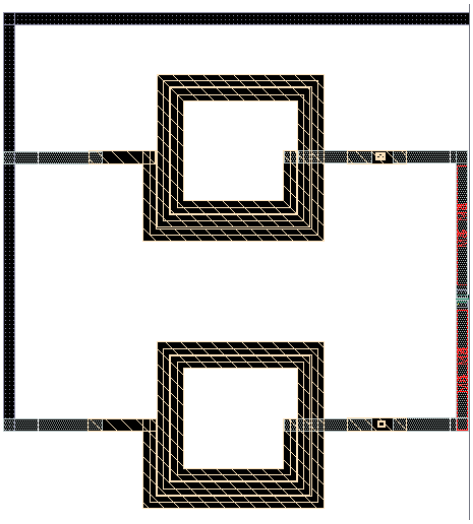


Figure 6.8 Layout of Inductors

6.5 Simulation Results

The simulation results for this design are taken from HSpice's schematic file of the voltage controlled oscillator. The schematic file is used as opposed to the post layout simulation file because of the difficulty in distinguishing nodes. However, the phase noise analysis is done using Spectre, since it is adapted for such tasks. In this section the reader is given a summary of the desired characteristics of the VCO, an explanation as to why each parameter is significant, and figures that display the VCO's actual performance. Also, some additional constraints set by the designer are explained and documented. Table 6.1 at the bottom of the page gives a summary of the requested attributes of the LC-VCO. As seen, the design calls for a wide tuning range, fairly low power consumption, a phase noise of less than -100dBc/Hz, and an output amplitude of at least 1V for its maximum and minimum current bias.

Table 6.1 Design Summary of Desired Characteristics

VCO Parameter	**Desired Result**
Power Supply	1.8V
Technology	0.18 μm CMOS
Center Frequency	2.4 GHz
Estimated Tuning Range	> 400 MHz
Power Consumption	<15mW
Phase Noise	<100 dBc/Hz @ 1MHz offset
Output Amplitude	>1V

A. Tuning Linearity

The first design parameter discussed is the tuning linearity. This parameter is important because it affects the consistency of the VCO. The more nonlinear the tuning range, the more K_{VCO} fluctuates. This becomes a problem when a PLL can not handle such variations, and may have trouble properly locking to a phase. Also, a high K_{VCO} due to a large tuning range, can allow unwanted harmonics to enter the VCO's spectrum. These harmonics change the behavior of the VCO by adding noise fluctuations to its output frequency and phase. This is seen in the phase noise equation below [1].

$$L(f_m) = 10\log\left[\frac{2FkT}{Ps}\left(\frac{f_o}{2Q_L f_m}\right)^2\left(1+\frac{f_k}{f_m}\right)+\frac{|K_{VCO}|^2}{2f_m^2}S_{VCNT}+\frac{|K_{VDD}|^2}{2f_m^2}S_{VDD}+\frac{|K_{IB}|^2}{2f_m^2}S_{IB}\right] \quad (1)$$

The term $\frac{|K_{VCO}|^2}{2f_m^2}$ represents the sensitivity of the output frequency to variations in the control voltage. As observed, if the magnitude of K_{VCO} is high, then the voltage controlled oscillator is more sensitive to variations in the control voltage. It also makes sense that this heightened sensitivity increases the noise in the circuit as well.

Table 6.2 lists the frequency of each process corner with the control voltage varied from 0 to 1.8 V in increments of 0.2 V. Figure 6.9 is a graph of these results. It gives a visual interpretation of the tuning linearity of the circuit through each process corner. It is most important for the VCO to exhibit a linear characteristic at and around its center frequency. Again, this reduces the probability of problems with PLL loop dynamics. Also, table 6.3 gives the reader an idea of how much K_{vco} fluctuates. Usually, K_{vco} is allowed to fluctuate within a certain range without affecting these same PLL loop dynamics PLL.

Table 6.2 Control Voltage vs. Frequency Through Process Corners

		frequency	
Control Voltage(Vc)	slow-slow(ss)	typical(tt)	fast-fast(ff)
0.00	2.04	2.12	2.20
0.20	2.20	2.26	2.32
0.40	2.34	2.38	2.42
0.60	2.46	2.50	2.52
0.80	2.56	2.58	2.60
1.00	2.62	2.66	2.68
1.20	2.68	2.72	2.74
1.40	2.72	2.76	2.80
1.60	2.74	2.80	2.84
1.80	2.76	2.82	2.86

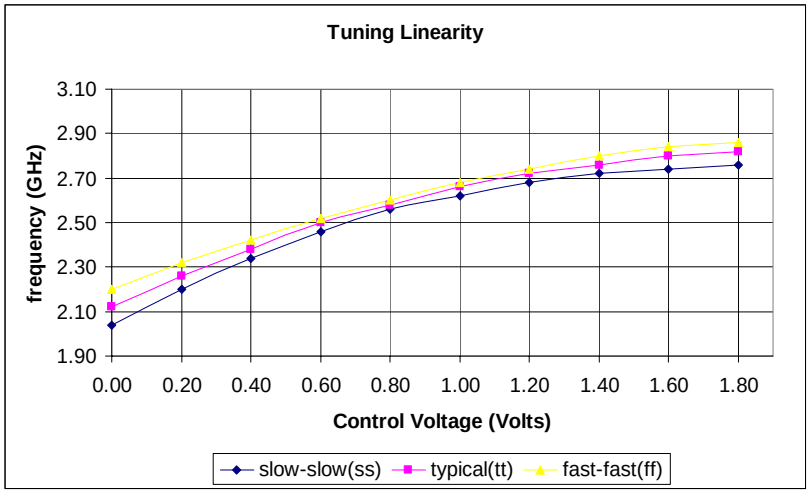


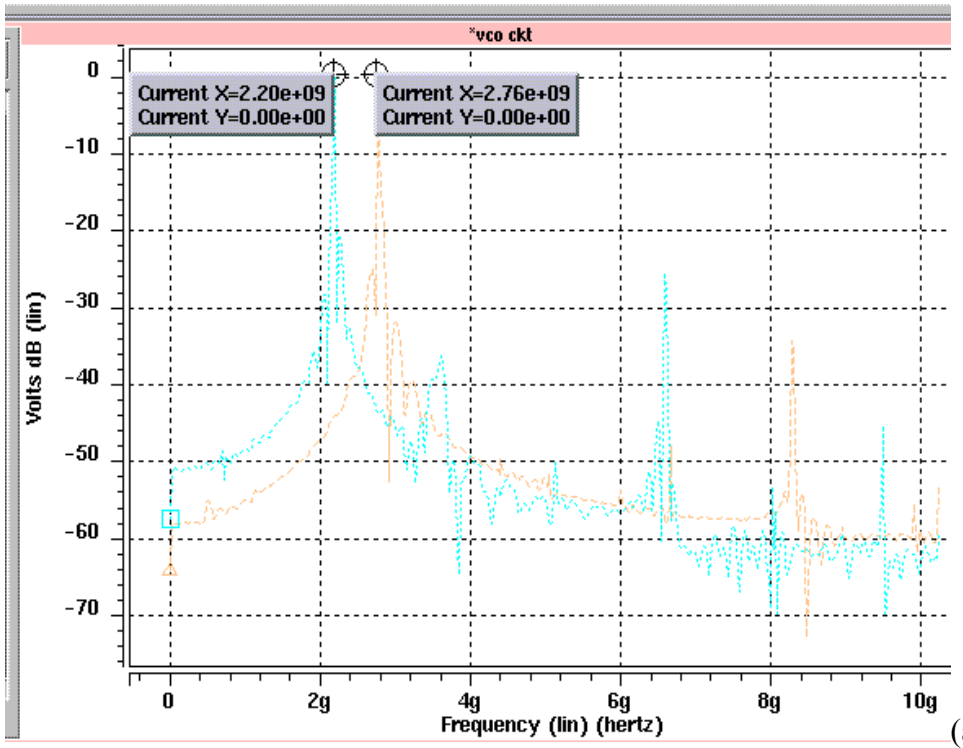
Figure 6.9 Graph of the Tuning Linearity Characteristics of the LC-VCO

Table 6.3 LC-VCO Gain Fluctuation

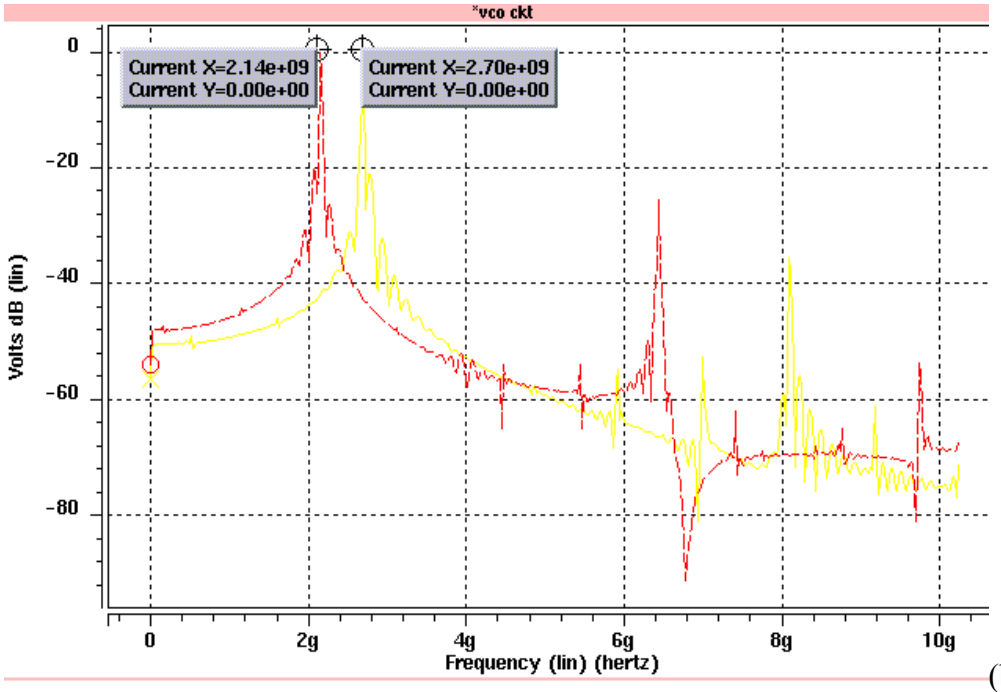
	Kvco	
slow-slow(ss)	typical(tt)	fast-fast(ff)
-	-	-
800MHz/V	700MHz/V	600MHz/V
700MHz/V	600MHz/V	500MHz/V
600MHz/V	600MHZ/V	500MHz/V
500MHz/V	400MHz/V	400MHz/V
300MHz/V	400MHz/V	400MHz/V
300MHz/V	300MHz/V	300MHz/V
200MHz/V	200MHz/V	300MHz/V
100MHz/V	200MHz/V	200MHz/V
100MHz/V	100MHz/V	100MHz/V

B. Tuning Range

The next design parameter discussed in this chapter is the tuning range. The tuning range and the tuning linearity coincide with each other because the effective tuning range depends on characteristics of the tuning linearity. Although a wide tuning range is desired, it presents trade-offs that must be addressed in order to implement a successful VCO. For this design, it appears that the estimated tuning range is about 720 MHz. However, a wide tuning range is only desired to withstand variations in linearity, process, and temperature. For example, depending on the dynamics of the PLL in which this design is allocated, only a certain portion of the VCO tuning range is chosen as its effective tuning range. Usually the range that presents the most linear quality (K_{VCO} constant within a certain tolerance) is selected. This range is again condensed by process corners and temperature variation analysis. However, the bandwidth must only be enough to cover the frequency range of the desired application after all limitations. Figures 6.10(a) and 6.10(b) give an example of such a transition. In 6.10(a), the effective tuning range is given by the highest frequency at a control voltage of 0 V and the lowest frequency at a control voltage of 1.8 V evaluated at the three process corners. More than often this is the fast-fast corner frequency at 0 V and the slow-slow corner frequency at the highest potential, which agrees with this design. This process, done at room temperature, lowers the tuning range from 720 MHz to 540 MHz. Furthermore a 75º C increase in temperature, which is seen in figure 6.10(b), shifts the tuning range 60 MHz backwards (backwards meaning lower in frequency). Effects such as these can make a VCO ineffective if not properly taken into account.



(a)



(b)

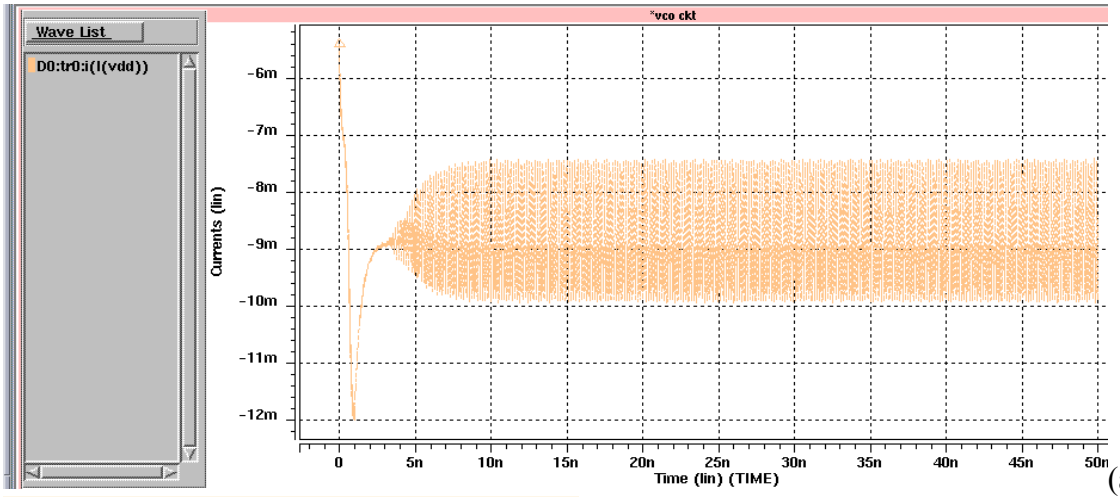
Figure 6.10(a) Effective Tuning Range with a Temperature of 25º C
(b) Effective Tuning Range with a Temperature of 100º C

C. Power Consumption

The power is another vital parameter of an LC-VCO. Since the VCO is one of the most power consuming blocks of a PLL, power is usually one of the first constraints set. The power affects most other aspects of the VCO and is strongly dependent on the sizes of the transistors and the amount of bias current used. Since this VCO design works for a bias current from 400-540 μA, it obviously consumes the most power when the bias current is 540 μA and the least when it is 400 μA. Given that a low amount of power is always preferred, the trade-off exists in the output amplitude and phase noise. The required peak-to-peak voltage of the output amplitude again depends on the application, but is heightened with bias current. As explained in chapter 2, an increase in power lowers phase noise also, but the designer must accommodate the circuit specifications. The minimum and maximum power is illustrated in figures 6.11(a) and (b).

D. Output Amplitude

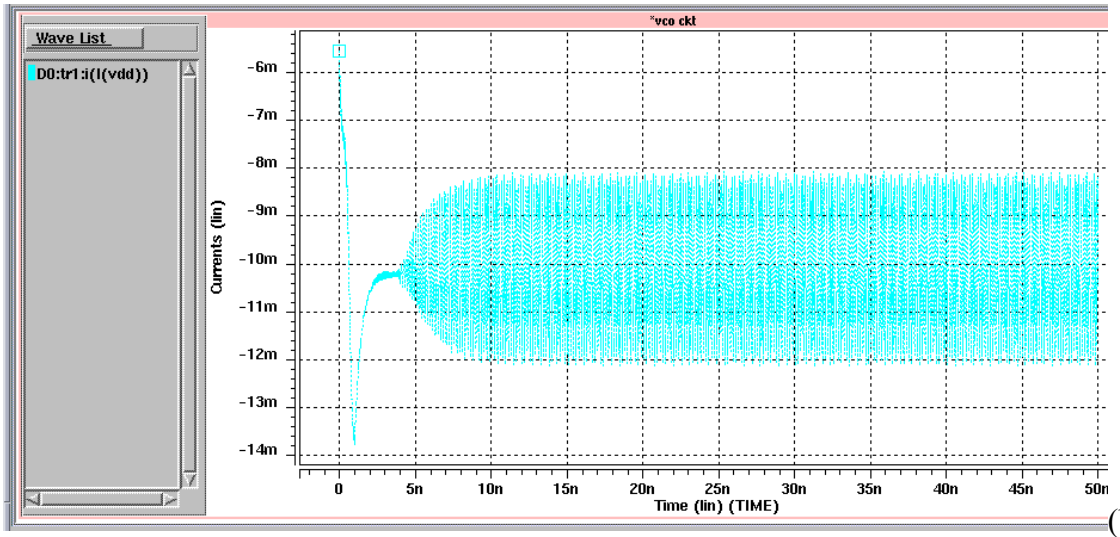
The output amplitude, often considered a secondary design parameter, is the peak-to-peak voltage of the VCO output. As previously stated, usually a specification is given for noise, tuning, or power and other parameters are tweaked accordingly. For a given tank, the output amplitude can only be increased by raising the bias current. As explained in the previous section, this affect lowers the phase noise while increasing power consumption. The output amplitude range, illustrated in figures 6.12(a) and (b), is about 1.48 V for the lowest bias current and about 1.66 V for the highest bias current. Depending on the amplitude desired by the next PLL stage (the frequency divider) and the power and phase noise constraints, the designer must decide which amplitude is best for the design.



(a)

```
****  voltage sources

subckt
element  0:v1        0:vdd       0:vss
 volts    900.0000m    1.8000      0.
 current -429.1563u   -8.8962m    9.5762m
 power    386.2406u   16.0132m    0.
```

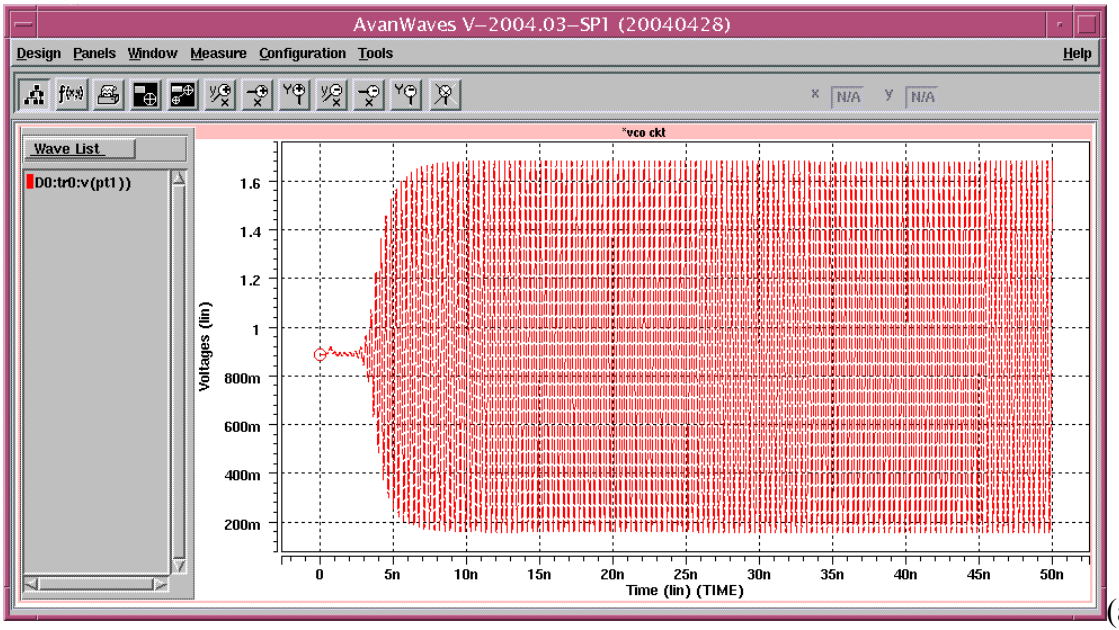


(b)

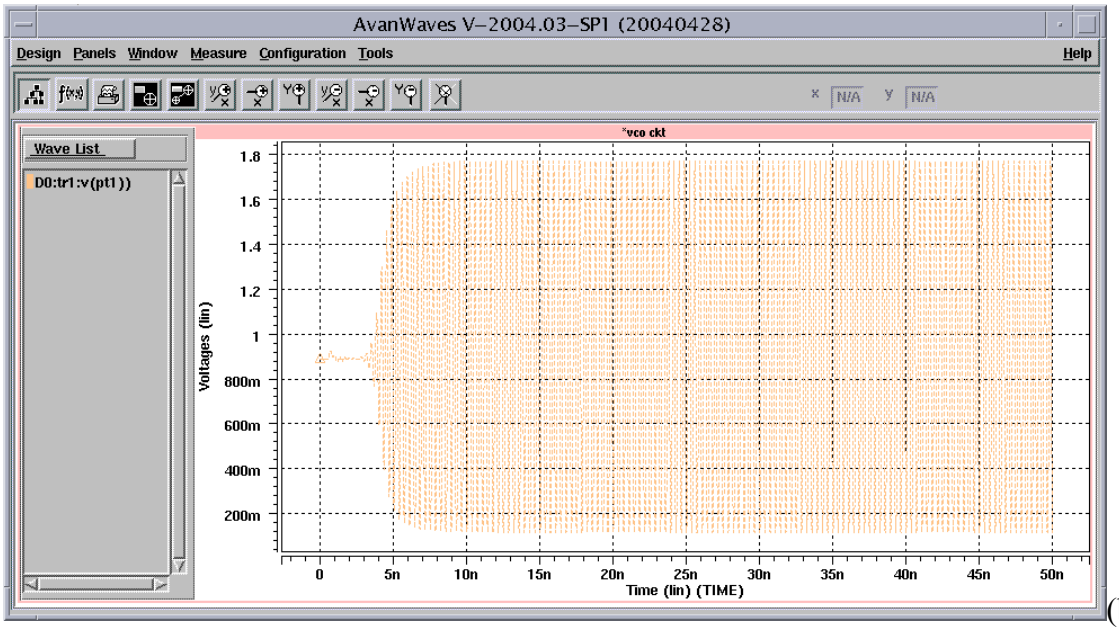
```
****  voltage sources

subckt
element  0:v1        0:vdd       0:vss
 volts    900.0000m    1.8000      0.
 current -721.9510u   -10.5861m   12.4649m
 power    649.7559u   19.0550m    0.
```

Figure 6.11(a) Minimum Output Power of the LC-VCO
(b) Maximum Output Power of the LC-VCO



(a)



(b)

Figure 6.12 (a) LC-VCO Output Amplitude Minimum
(b) LC-VCO Output Amplitude Maximim

E. Phase Noise

The phase noise performance of a VCO is important because it represents the stability of the output signal. As mentioned in previous chapters, some of the main sources of phase noise in LC-VCOs include flicker noise and the upconversion of supply rail and control voltage noise. Phase noise can also come from sources such a drain current thermal noise. The PMOS only topology can alleviate some of the affects of these sources, and the phase noise for this design is shown below in figure 6.13. The plot shows the single side band phase noise versus offset frequencies between 1 kHz and 3 MHz. At an offset frequency of 1MHz, the phase noise for this design is -127.1 dBc/Hz, which is competitive with similar VCOs, and meets the preset design specifications. The satisfactory phase noise performance may be a function of the PMOS only topology and the high output impedance of the wide-swing cascade.

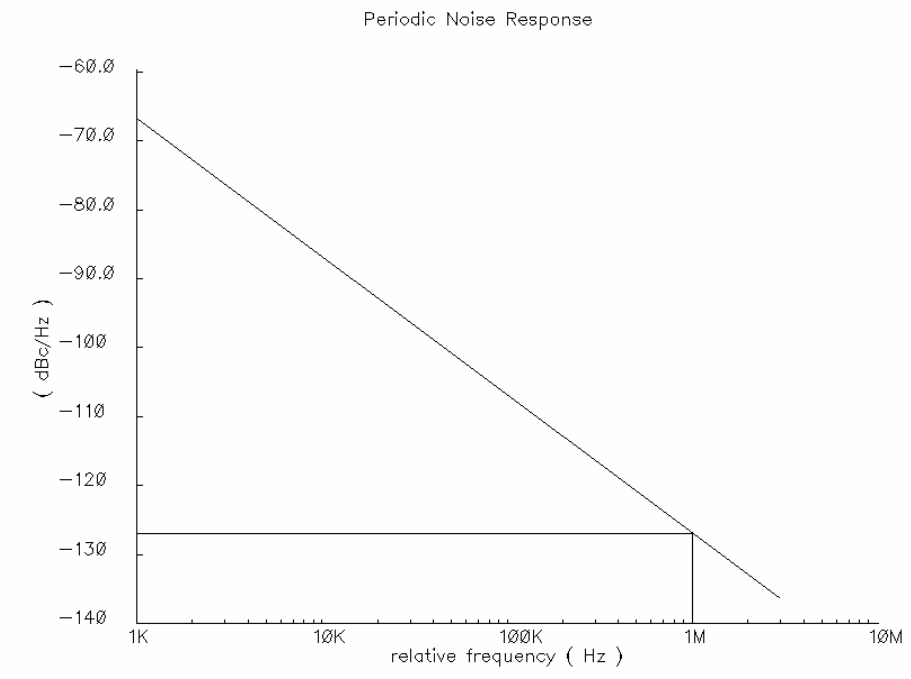
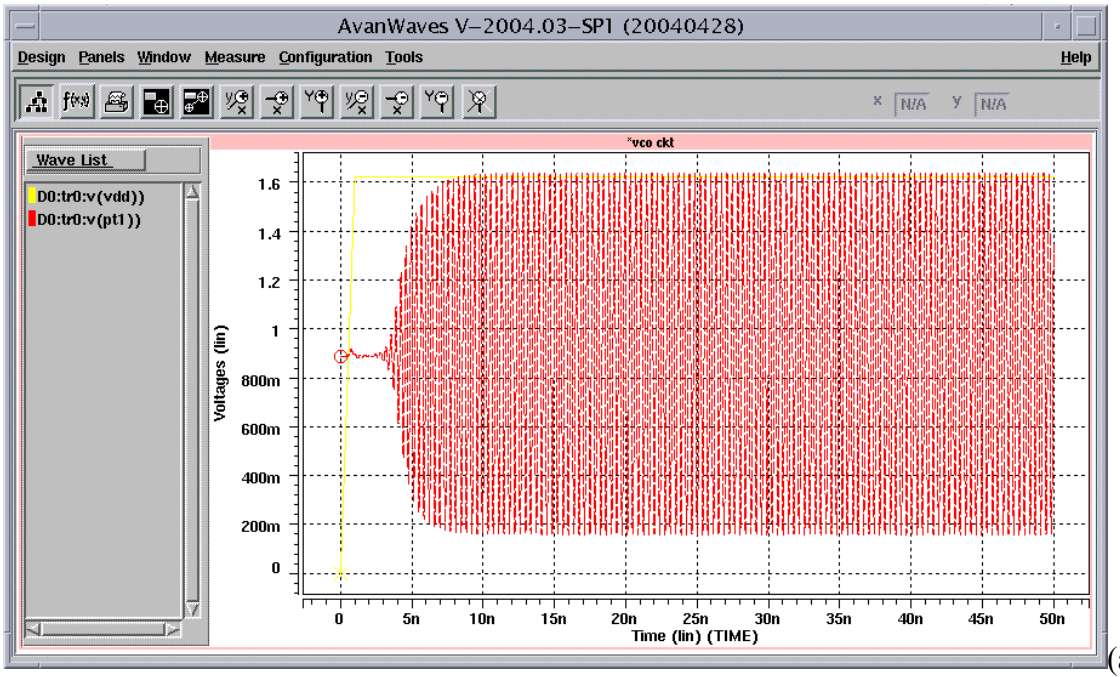


Figure 6.13 Spectre Phase Noise Plot of VCO

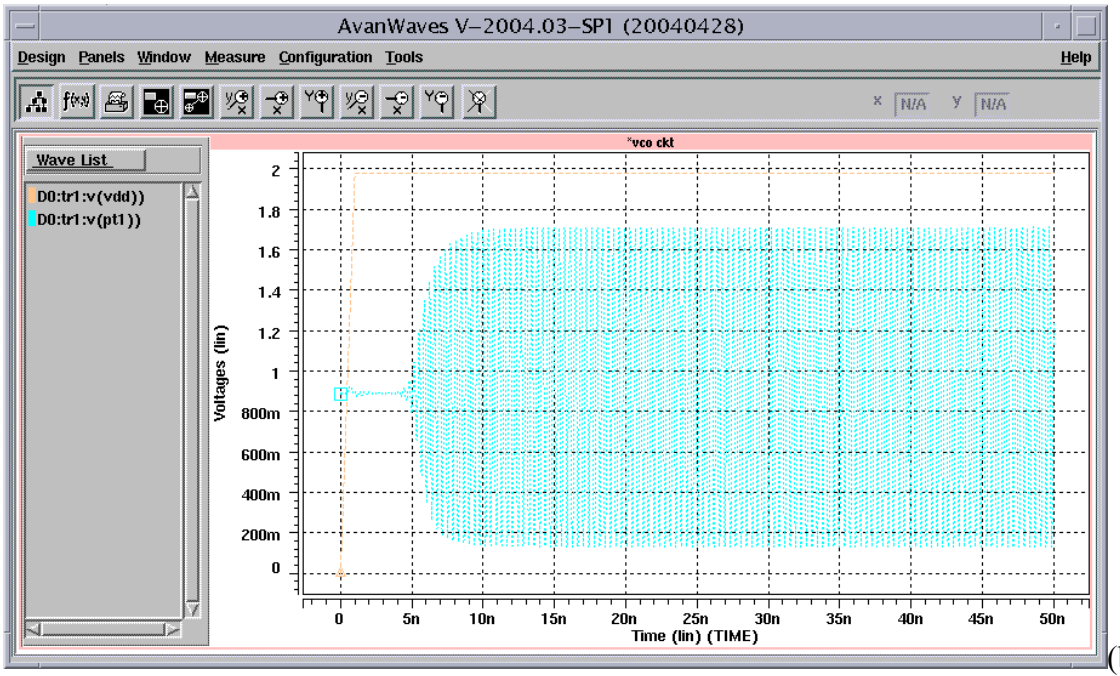
F. Other VCO Accomplishments

Another accomplishment in the design of the VCO includes consistent performance with ±10% variations in the supply rail. This achievement consists of a reliable output waveform and tuning characteristics for a range of 1.62 - 1.98 V. First, for the specified voltage range, the output sustains oscillations and remains at an output amplitude of greater than 1 V. This is shown in figures 6.14(a) and (b), which illustrate the output at 1.62 V and 1.98 V, respectively. Next, it is also important that the VCO exhibit steady tuning characteristics through changes in the supply rail. Figures 6.15(a) and (b) show the effective tuning range (at room temperature) at 1.62 V and 1.98 V. The control voltage for these plots is also adjusted to the new supply rail. These figures show an effective tuning range that is extremely consistent with the normal (1.8 V rail) effective tuning range.

The developed VCO uses source followers (W=8µm, L=180nm, m=8) as buffers for its output signals. This design is an improvement of an existing LC-VCO, also fabricated by the writer, and will be used for future LC-VCO architectures. At this time, packaging and test board preparations are being deliberated in great detail. The steps taken in the test procedure of the design in chapter 5 provide a learning experience for this design's test procedure. Improvements for the testing of this chip include more precise packaging, provisions for more accurate and straightforward monitoring of currents, and possible impedance matching.

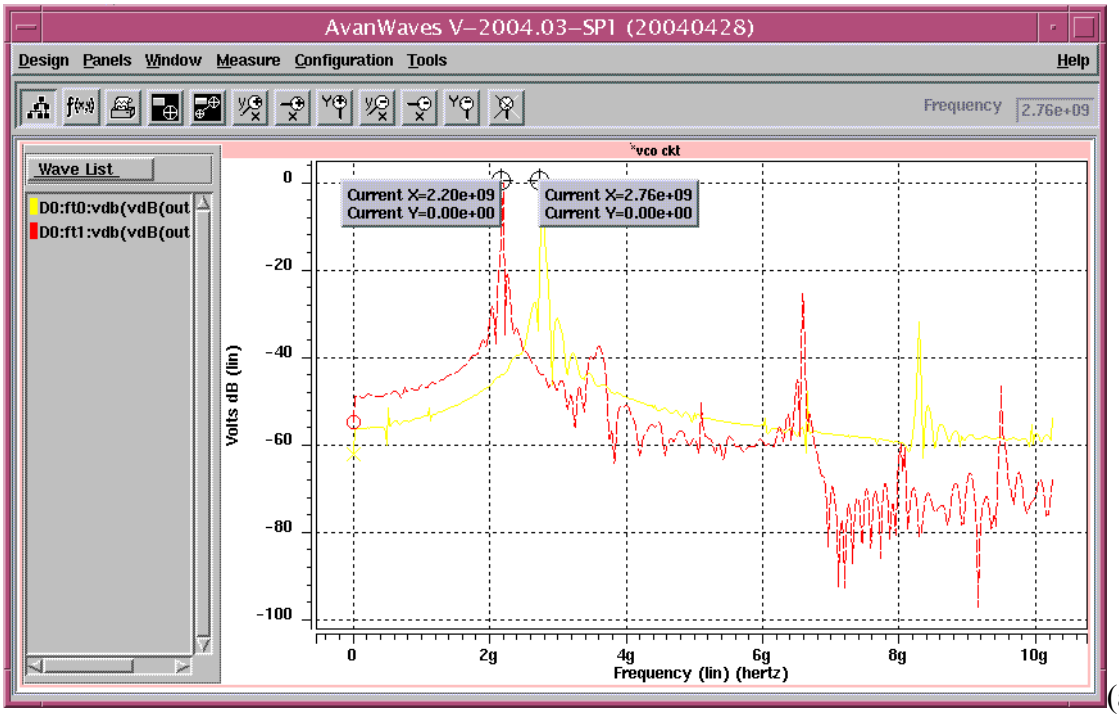


(a)

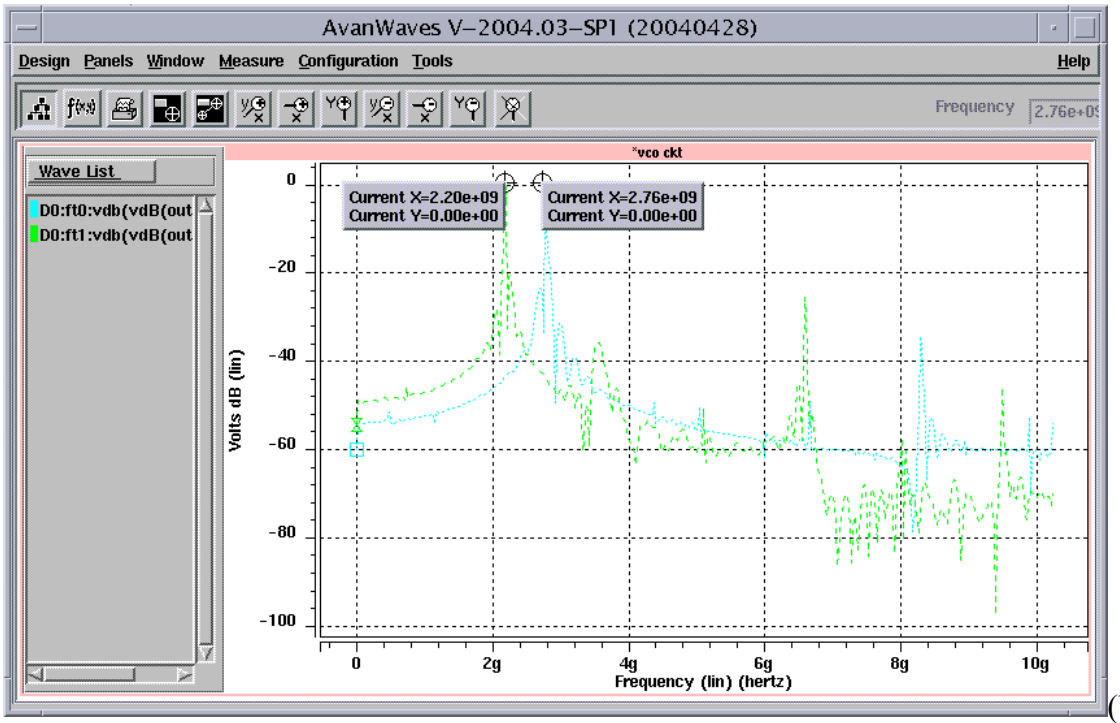


(b)

Figure 6.14 (a) Output Amplitude at 1.62 V Supply Rail
(b) Output Amplitude at 1.98 V Supply Rail



(a)



(b)

Figure 6.15 (a) Tuning Range at 1.62 V (at room temperature)
(b) Tuning Range at 1.98 V (at room temperature)

Chapter 7 Conclusion and Future Work

7.1 Conclusion

A completely integrated LC-VCO compatible with the ISM band was successfully implemented in a 0.18 μm CMOS technology. It has an effective tuning range of 460 MHz at room temperature and consumes approximately 14.24mW with a tail current of 260 μA. The VCO has a phase noise of -125.8 dBc/Hz at mid-supply and 1MHz offset which is more than satisfactory for this design. Despite moderately high power consumption, the VCO met all of the pre-determined design goals. However, the high power consumption is compensated by a relatively low phase noise. Also, valuable experience was gained with the testing of a 1.8 GHz LC-VCO in a 0.35 μm CMOS technology.

7.2 Future Work

Future work in the area of LC-VCOs lies in the improvement of the on-chip inductor. Raising the quality of the integrated inductor means improved phase noise performance, which can result in lower power devices. Since these are two of the main design parameters, other parameters will benefit from these improvements also. Furthermore, effort can also be put into lowering the area of the integrated inductor. They dominate the size of LC-VCO designs, while transistor sizes get smaller. Also, with the improvement of the integrated inductor could come other implementations with

its use. Though varactor quality is superior to inductor quality, improvement in the area of varactor linearity would widen tuning ranges. This could lower the bandwidth of current devices, but yield the same, if not better, results. Together, these improvements would present a tremendous step forward for wireless applications.

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Vita

Bryant Williamson was born on January 31, 1980, the son of Mary and Landers Williamson in Memphis, Tennessee. He graduated from White Station High School in 1998 where he excelled in the classroom and on the basketball court. He then pursued a basketball future at Kansas Wesleyan University before transferring to the University of Tennessee, Knoxville. After receiving an undergraduate Electrical Engineering degree from the University of Tennessee, he pursued his Masters also at the University of Tennessee. He would like to be noted for his hard work and determination during tranquil and intense periods. He would also like to say that no matter where a person is from or what their situation is, they can do anything (despite being told they can not).