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A 1.8 GHz LC-Voltage Controlled Oscillator Using On-Chip Inductors and Body Driven Varactors in CMOS 0.35 μm process

Lakshmipriya Seshan
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Lakshmipriya Seshan entitled "A 1.8 GHz LC-Voltage Controlled Oscillator Using On-Chip Inductors and Body Driven Varactors in CMOS 0.35 μm process." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed K. Islam, Major Professor

We have read this thesis and recommend its acceptance:

Benjamin J. Blalock, Donald W. Bouldin

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A Thesis

Presented for the

Master of Science Degree

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Lakshmipriya Seshan

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ABSTRACT

In an era dominated by the highly demanding wireless communication system, there is a great need for developing small, cheap, and low power RF sub-systems. This demand has lead to significant research on completely integrated transceiver systems. One of the great challenges in an integrated transceiver system is the frequency synthesizer. Frequency synthesizers are usually implemented using a phase locked loop (PLL) and low frequency highly stable crystal oscillator. The spectral purity of a synthesized carrier signal depends on the kind of Voltage Controlled Oscillator (VCO) used. Hence successful implementation of a low phase noise, completely integrated VCO in standard CMOS process is a major step towards implementing a completely integrated transceiver.

The best VCO architecture in terms of noise performance is LC-VCO. The aim of the current research is to design a completely integrated 1.8 GHz LC-VCO for a GSM or DCS-1800 receiver in standard CMOS 0.35 μm technology. The major challenge in a completely integrated LC-VCO is to develop an fully integrated inductor. In this research various means of implementing an integrated inductor have been scrutinized and the best feasible among them the on-chip spiral inductor has been analyzed elaborately. The complete design cycle from describing the specification of an inductor to the final layout in Cadence has been described. Also a new symmetrical, highly balanced on-chip inductor has been used in the current design. Another important and the most critical challenge is to implement a very high tuning range, high Q-factor on-chip varactor in standard CMOS process. In this research a new body driven varactor, which is forced to operate in accumulation mode has been developed and analyzed elaborately. The tuning range specification for the design was chosen to be 200 MHz accounting for component tolerance. Various means of measuring phase noise has been elaborately analyzed. Also detailed study on improving the noise performance of the LC-VCO has been studied.

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1 INTRODUCTION

1.1 Overview

If each decade has its name dedicated to a scientific advancement, then the nineties will certainly be known for making everyday life wireless. This has been accomplished by the technological revolution from the large, bulky, noisy, and costly mobile phone of eighties to the GSM (Global System for Mobile Communication) phones that fit into the pocket while offering high quality connection, several hours of talk time and at significantly lower cost. The demand for high bandwidth communication channels have further exploded with the advent of the Internet. The rapid advancement from professional wireless users to a real mass market was achieved mainly due to the high-density integrated circuit and efficient digital modulation schemes. Transceiver which forms the main unit in a wireless system is migrating from a multi-chip system to a single-chip with minimum external components. A major challenge in integrated transceiver is to accomplish low noise, low power, and high frequency optimized sub-blocks in a single unified technology. This has been the driving force behind the scaled CMOS technology. All these developments will lead to the long time goal to produce an omniscient wireless terminal that can handle voice, data and video along with amazing computational speed.

1.2 Motivation

A transceiver (transmitter-receiver) is the basic building block that interfaces between the user and the transmission medium in wireless communication. It consists of three blocks. The user block interfaces between the raw data and its digital data representation. The back-end module modulates or demodulates the digital data to and from the user interface by a suitable transmission technique such as GMSK, QPSK. The front end is the building block that does conversion between the high frequency wireless signals and the low frequency baseband signal. Figure 1.1 shows a simplified GSM1800 receiver architecture [1]. For the receiver system the front-end amplifies the wireless signal using a low noise

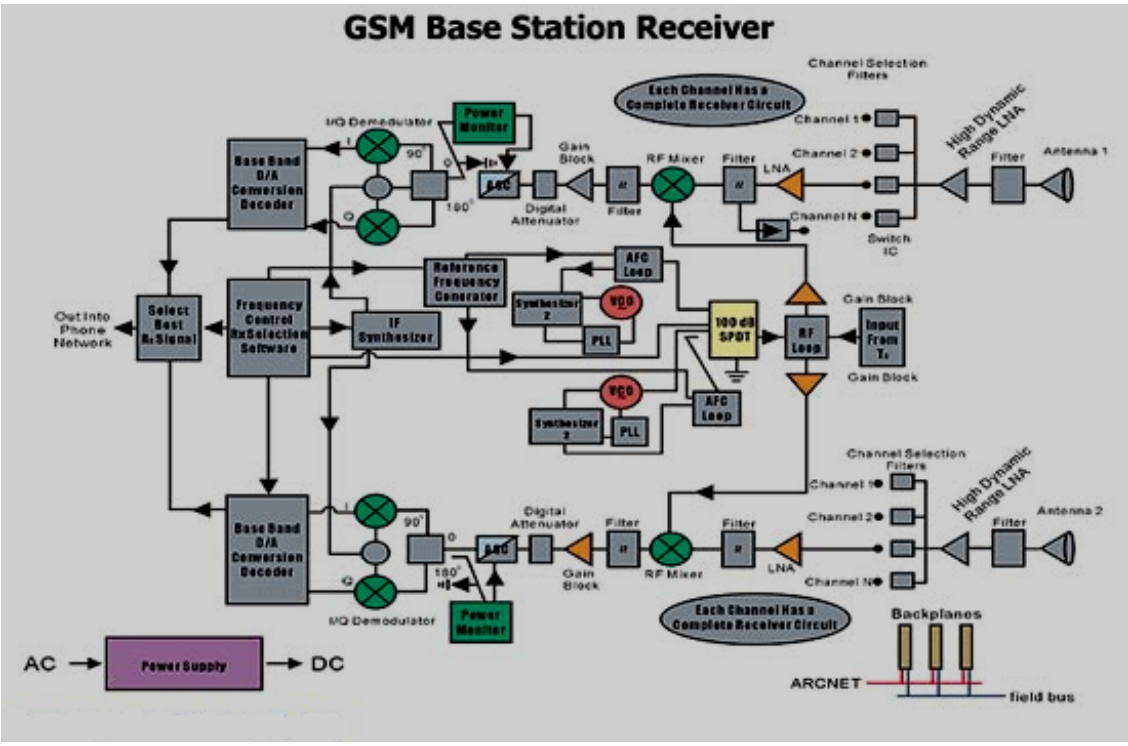


Figure 1.1 : GSM base station receiver [1]

amplifier (LNA), after removing unwanted signals through a band-pass filter (BPF). Then the received signals are mixed down with the local oscillator signal to the intermediate frequency (IF). The major problem with this architecture is the integration of high quality passive BPF, and the local oscillator in a single integrated circuit

One of the major blocks that determine the performance in the front end is the local oscillator or more commonly called the frequency synthesizer. The spectral purity of the synthesized sine wave from the monolithic frequency synthesizer using external discrete components is much higher than the fully integrated system. This is one of the key requirements for any transceiver system. But as the transceiver system evolves towards a single chip concept, the frequency synthesizer will move towards a integrated system. Hence new techniques are currently being investigated to realize high performance frequency synthesizers with comparative performance as the discrete counterpart.

For the lower end of the spectrum a very stable crystal oscillator can be used to generate a very accurate reference carrier signal. For higher frequencies (> few hundred MHz) the quality of the crystal resonator degrades due to the physical limitations and material properties. Many wireless applications require programmable carrier frequencies. The cost and board space of a multitude of crystals would be strenuous. Hence indirect frequency synthesizers based on a phase locked loop (PLL) are widely employed. In a PLL a high frequency RF signal is locked to a precise low frequency clock by means of a RF oscillator whose frequency is varied using a control signal embedded in a feedback loop. The critical block in the PLL architecture is the RF oscillator or more commonly known as the voltage controlled oscillator (VCO). The current research will focus on the silicon implementation of VCO for wireless application.

There are different ways of implementing a tuned VCO. Traditionally they were implemented easy to use hybrid models, but were bulky and expensive. High volume markets are governed by the price, package, performance and power. Integration reduces production cost due to large volume production. Integration also reduces the interface cost and allows cheaper packaging solutions. The performance depends on the choice of the IC technology. Table 1.1 provides a comparison of the performance of different VCO implementation reported in the literature during the time period 1995 – 2003.

1.3 Contribution of current work

Currently a lot of research is being pursued in developing RF circuits for the most widely used communication standards namely Digital Cellular System (DCS-1800) and GSM 1800 communication standard. The aim of the current research is to design a completely integrated 1.8 GHz LC-VCO for a GSM or DCS-1800 receiver in standard CMOS 0.35 μm technology. The major challenge in a completely integrated LC-VCO is to implement an integrated inductor. In this research various means of implementing an inductor has been scrutinized and best feasible among them the spiral inductor has been analyzed. Complete design cycle from describing the specification of an inductor to the final layout in Cadence has been described. Also a new symmetrical, highly balanced on-chip

Table 1.1: Comparison of previous VCO implementation

Paper	Type	f_o (GHz)	Power (mW)	Technology	Tuning Range	Vdd
Kwasniewski[13]	Ring	0.85	18	CMOS 1.2 µm	100 MHz	5.0
Soyeur[2]	LC	4	12	BiCMOS 0.5 µm	360 MHz	3.0
Rofourgaran[3]	LC/etch	0.82	25	CMOS 1 µm		3V
Razavi[4]	Ring	2	1.6	BiCMOS 0.6 µm		3V
Dauphinee[5]	LC	1.5	28	BiCMOS 0.8 µm	150 MHz	3.6
Plouchart[6]	LC	17.38	22	SiGE, BiCMOS	625 MHz	3.1
Razavi[7]	LC	1.8	7.5	CMOS 0.6 µm	120 MHz	3.3
Wang[8]	LC	9.8	12	CMOS 0.35 µm	270 MHz	2.7
Liu[9]	LC	6.29	18	CMOS 0.35 µm	300 MHz	1.5
Razavi[10]	LC	2.6/5.2	13	CMOS 0.35 µm	320 MHz	2.5
Jain[44]	Ring	5.3	4.7	CMOS 0.18 µm	1.25 GHz	1.8
Andreani[12]	LC	1.8	3.3	CMOS 0.6 µm	198 MHz	2.7
Levantino[14]	LC	5.1	7.25	CMOS 0.25 µm	1.1 GHz	2.5

inductor has been used in the current design. Another critical challenge in a LC-VCO is to implement a wide tuning range, high Q-factor on-chip varactor in standard CMOS process. Usually on-chip spiral inductors provide a very low Q-factor not more than 10. Thus in order to prevent further deterioration of the effective Q-factor, the Q-factor of the varactor should at least be 4-5 higher than the Q-factor of the inductor. Another goal of the current research is to explore the performance of different types of varactors realizable in standard CMOS process. Finally for the designed LC-VCO, a new body driven varactor, which is forced to operate in accumulation mode has been developed and analyzed. The tuning range specification for the design is chosen to be 200 MHz accounting for component tolerance. Various means of measuring phase noise has been explored. The influence of the various components non-ideality on the overall systems jitter has been studied.

1.4 Organization of this thesis

In Chapter 2, fundamentals of voltage-controlled oscillators are discussed. Voltage controlled oscillators are essential blocks in frequency synthesizers. The discussion is based on the harmonic LC-VCO most commonly used in wireless application. The relationship between the Q-factor and circuit parameters has been derived. LC-VCO

working principle along with different regions of operation has been described. Other types of VCO architecture have also been explained and their shortcoming for wireless application has been studied.

Chapter 3 discusses the different techniques for realizing an integrated inductor and high Q-factor varactor. Four different types of integrated inductors have been analyzed and the best feasible among them the spiral inductor in terms of practical large-scale implementation has been analyzed deeply. A general overview of ASITIC, the modeling tool used for analyzing the spiral inductors has been presented. Different types of conventional varactors in standard CMOS process have been compared. Elaborate analysis on the new body driven varactor operating in accumulation mode is also presented.

Chapter 4 begins with a discussion on the design of 1.8 GHz LC-VCO. Complete design steps from the specification of physical dimension to the final layout in Cadence have been presented. A general overview on the phase noise performance of the LC-VCO is also described. Finally, a better means of analyzing jitter based on the non-ideality of the individual tank elements has been developed.

Chapter 5 summarizes the design and provides suggestions for future work.

2 VOLTAGE CONTROLLED OSCILLATORS

Controlled Oscillators are autonomous circuits that produce a stable periodically time varying waveforms whose frequency of oscillation varies with the change in the control signal. The control signal can be the voltage or the current thus leading to two different types of controlled oscillators called the voltage-controlled oscillators (VCO) and the current controlled oscillators. In this chapter, oscillator design equations and other performance parameters will be derived based on the VCO. The same theory and the performance constraints are also valid for the current controlled oscillators.

2.1 History

The current stand of VCO owes its heritage to Edwing Armstrong who discovered that there needs to be a method to the change the frequency of an oscillator to maintain a constant IF frequency for varying input frequencies (Superhetrodyne principle). He designed a vacuum tube called Audion which used a spark-gap oscillator for varying the frequency. The basic oscillator topology was later improved by Rober. V. J. Hartley, who designed the first tuned oscillator using an amplifying device and inductive feedback, to recreate the damped tuned oscillations. This sparkling network lead way to many widely used topologies like Colpitts, Clapps, Armstrong, and Pierce all using some tuned network in the feedback loop, where either a capacitor or an inductor value would be varied mechanically for achieving variable frequency. Like many other inventions in electronics all these earlier topologies were very bulky, expensive and consumed huge amount of power making them viable for military applications only. The commercial utilization of these concepts became viable after the invention of bipolar transistors (1950) and the discovery of reverse biased pn junction for variable capacitors (1960's). Figure 2.1[14] shows the chronological changes in VCO technology from tube based VCO to monolithic VCO. The monolithic IC which promises amazing reduction in size and cost effective technology, advanced mainly due to the tough space constraint and large volume market offered by the new mobile wireless market.

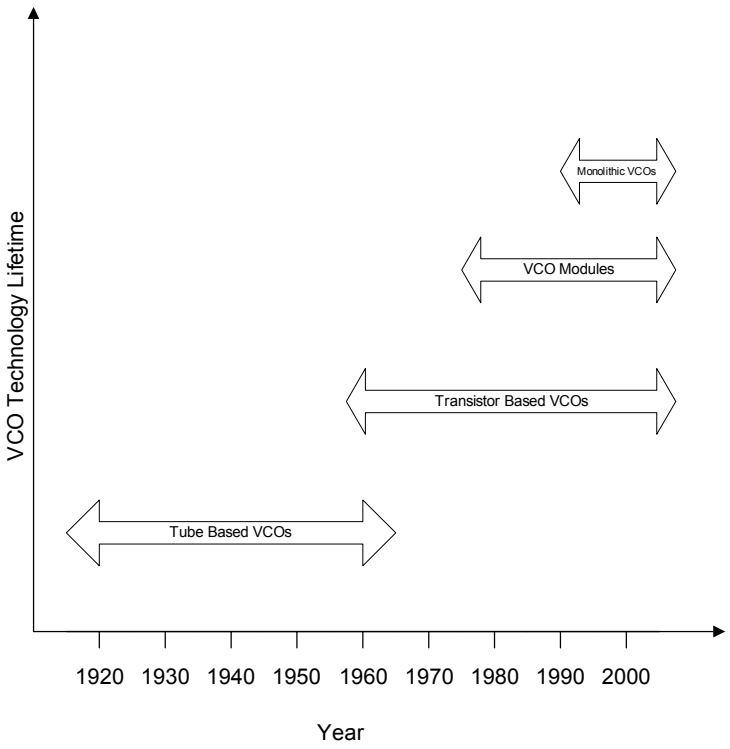


Figure 2.1 : Chronological changes in VCO

The VCO IC sizes have shrunken from 1300mm^2 in 1980's to the current figure of 40mm^2 that cost less than a dollar [14]. The first VCO using Si IC technology was developed at the University of California at Berkeley (1992). The high transition frequency of Si (f_T) was improved to suite the RF frequencies and monolithic components were developed for high frequencies. However the initial VCO IC's performances were mediocre, due to the discrete implementations in terms of phase noise and tuning characteristics. Integrated VCO offers many advantages such as the high level of integration with other transmitter blocks and cost effective solutions. Hence a lot of research is currently being pursued to improve the phase noise, tuning characteristics and other performance parameters of the integrated VCO in comparison with the discrete implementation. The quest for an optimum performance VCO has put researchers in a perpetual cycle.

2.2 Phase Locked Loop

As discussed in the previous sections one of the most critical blocks in a transceiver systems is the frequency synthesizer realized using phase locked loop (PLL). PLL are used in wide variety of applications such as frequency synthesizer in transceivers, clock recovery circuits in communication systems, synchronizing clocks in digital systems, FM demodulators etc. Depending on the applications one or more performance variables are optimized, but the basic architecture remains the same.

Figure 2.2 shows a simplified PLL architecture. It consists of four basic blocks namely phase and frequency detector (PFD), charge pump, voltage controlled oscillator (VCO) and frequency divider. A PLL is a feedback system whose output frequency is locked on to a multiple of the input frequency. In a PLL the PFD compares the phase and frequency of the input reference clock CLK_{in} with the scaled down frequency of the output signal CLK_{out}. The phase and frequency difference is converted into an equivalent complementary digital voltage P_{up} and P_{dn}. These control the switches of the charge pump, which charges or discharges C_1. The stored charge in C_1 is filtered through a low-

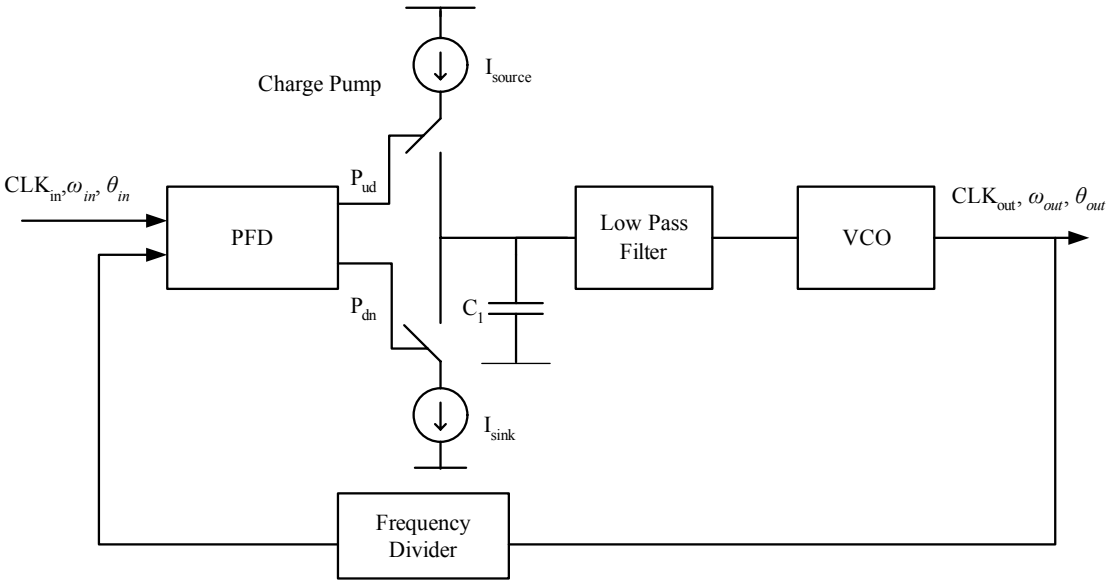


Figure 2.2 : PLL block diagram

pass filter and fed as control signal to the VCO. The output frequency of the VCO varies in proportion to the control voltage. Within a few iteration the output signal locks to a input reference clock signal. The novelty about this scheme is that the reference input clock can be a low frequency stable crystal clock signal and output can be RF carrier signal depending on the dividing ratio. The most critical block in terms of noise performance is the VCO.

2.3 Types of VCO

VCO can be broadly classified into two categories; the relaxation or the non-linear oscillators and the harmonic or the sinusoidal oscillators. Each category has its own advantages and disadvantages. Table 2.1 summarizes the difference between the two types.

The main applications of VCO are in communication transceivers and data communication, as a critical component in frequency synthesizers as discussed in the earlier section. Most of the sub-blocks except the frequency synthesizer in modern implementations are digital blocks. In a complete integrated environment the VCO share the same substrate with the rest of the noisy digital blocks. Hence the type of VCO chosen for such applications should be highly immune to noise for rest of the sub-blocks to function properly. Also the current wireless spectrum in the frequency range of 800MHz – 2.5GHz has very narrow channel spacing. Hence the reference carrier signal from the frequency synthesizer should be a pure sinusoidal signal. With all these strict noise requirements LC VCO becomes the best choice for wireless applications.

Non-linear oscillators which offer their own advantages such as wide tuning range and small area find wide application in data communication, clock recovery and some low frequency synthesizers which do not require strict noise requirements. In the current discussion the general working of VCO and its design equation would be derived based on general model of LC-VCO. Later a brief description of non-linear oscillators will be presented.

Table 2.1: VCO comparison

Harmonic Oscillators	Non- Linear Oscillators
Requires special considerations for stabilizing the tank	Simple design
Constrained by the area of passive implementation	Minimum area required
Built-in filter circuit	No built-in filter circuit
Limited tuning range	Wide tunabilty
Superior phase noise performance	Susceptible to noise
Output frequency is susceptible to passive device tolerance	Stable output frequency
Example : LC VCO	Example: Ring Oscillator

2.4 Analysis

An electronic oscillator generates a periodic output by a self-sustaining mechanism that allows its own noise to grow and eventually produce a stable periodic output [15]. In other words an electronic oscillator can also be described as a system that converts dc-power to a periodic output. There are two different topologies that describe how the noise signal builds up to a sustained periodic output. One is a simple feedback model as shown in Figure 2.3. The model has an amplifier whose frequency and amplitude dependent gain is given by $G(A,\omega)$ and a feedback tuned circuit whose transfer function is given by $H(\omega)$. The closed loop gain using control systems block simplification is given by

$$\frac{v_o}{v_i} = \frac{G(A,\omega)}{1 - G(A,\omega) * H(\omega)} \tag{2.1}$$

where v_o is the output signal. In case of oscillators, there is no input signal

$$v_i = 0 \tag{2.2}$$

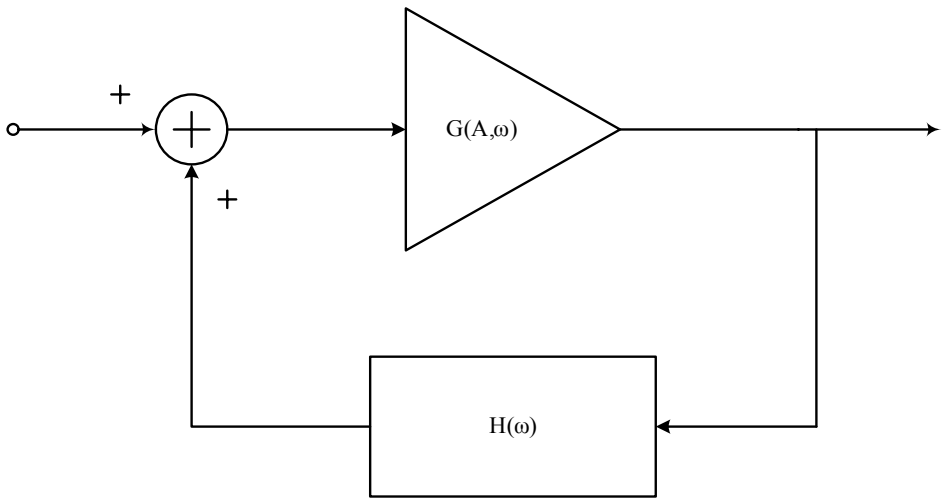


Figure 2.3 : Basic positive feedback network

Hence for a finite output the denominator of the closed loop transfer function must be zero.

$$G(A,\omega) * H(\omega) = 1 \tag{2.3}$$

The above equation is the mathematical implication of Barkhausen's theorem. The system oscillates if the magnitude of the loop gain (G(A,ω)*H(ω)) is unity and phase shift around the loop is zero or 360°. In RF oscillators, the frequency selective feedback network is designed such that the loop gain is unity and phase shift is zero exactly at the desired frequency. This concept can be mathematically modeled as a two-port network using the microwave theory. A simpler approach is to model it using two one-port networks as shown in Figure 2.4[15]. In this model the amplifier which is shown as the active element is designed such that it has enough gain to compensate for the loss in the feedback block which is the resonator circuit. The frequency of oscillation is determined by the resonant frequency of the feedback circuit, self-sustaining effect which allows the whole circuit's noise to be amplified and another mechanism which limits the amplitude of oscillation. Of course the simple model described above does not account for the amplitude limiting mechanism. This can be modeled by introducing a comparator network which measures the peak amplitude and compares it with the maximum and minimum limits and outputs a gain factor which controls the amplifier gain. The modified

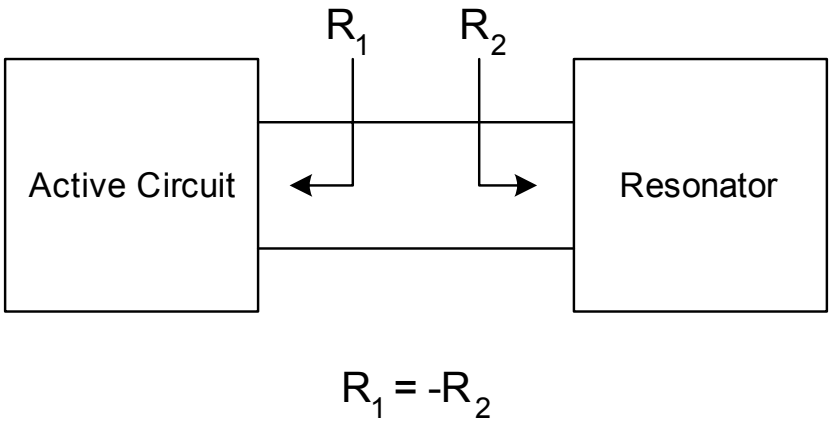


Figure 2.4 : One port network feedback model

mathematical model is shown in Figure 2.5. Initially during start up the amplitude of the output is small. Hence the gain control tends to increase the loop gain beyond unity. When the peak amplitude reaches the required steady state value of V_{REF}, the gain control restores the loop gain to unity. The value of V_{REF} must be chosen such that the output is a pure sinusoidal with minimum distortion.

VCO is a general oscillator except that its output frequency is determined by a control voltage. Hence the general mathematical model derived above also holds good for VCO. The output frequency is varied by varying the value of one of the passive elements of the resonator. The variation in the output frequency for an ideal VCO is a linear function of control voltage expressed mathematically by Eq (2.4).

$$\omega_{out} = \omega_{FR} + K_{VCO} * V_{cntl} \tag{2.4}$$

where ω_{out} is the output frequency, ω_{FR} is the fundamental or central frequency defined in the next section, K_{VCO} is the gain of the VCO(Hz/V) and V_{cntl} is the control voltage. The output signal *y(t)* for a sinusoidal output can be expressed as

$$y(t) = A\cos(\omega_{FR} * t + K_{VCO}\int_{-\infty}^{t} V_{cntl} * dt \tag{2.5}$$

In the above equation, if V_{cntl} is a sinusoidal input then the output is a frequency-modulated signal.

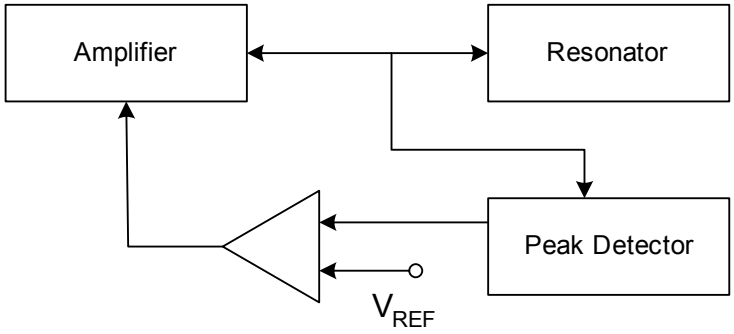


Figure 2.5 : Modified VCO mathematical model

2.4.1 Quality factor of an oscillator

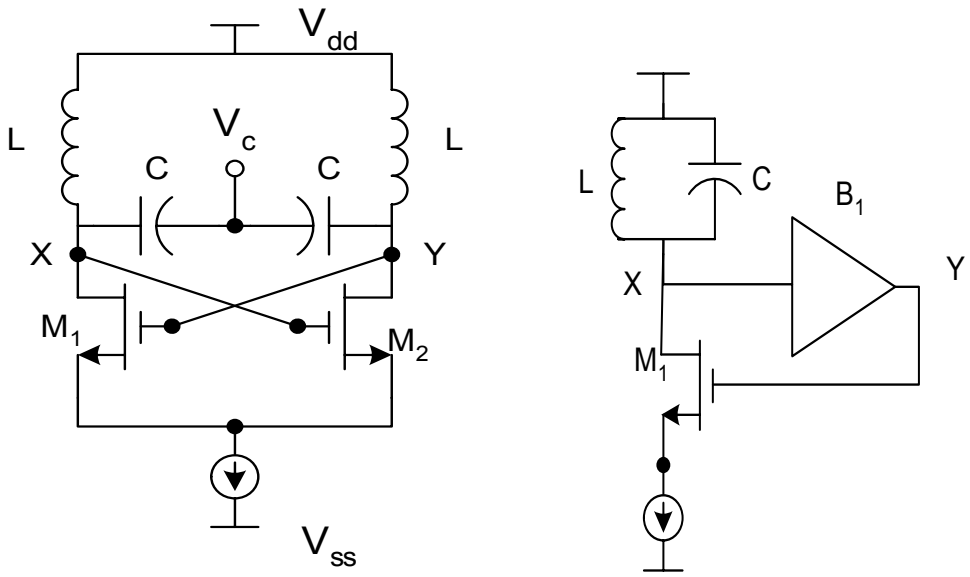
The quality factor (Q-factor) is one of the major important performance-determining characteristic of any resonant circuit. It is the measure of the ideality of the reactive components of the resonant circuit. There are different means to define Q-factor of a system. In basic physics it is defined as

$$2\pi * \frac{Energystored}{Energydissipated} \text{ per cycle} \tag{2.6}$$

Another definition is the measure of the sharpness of the frequency response as the resonance frequency to the -3 dB bandwidth. For high spectral purity, the Q-factor should ideally be infinity and practically a high value. Another definition for Q factor that is widely used in the analysis of oscillators is the defined using Eq (2.7) [15]

$$Q = \frac{\omega_o}{2}\left|\frac{d\phi}{d\omega}\right| \tag{2.7}$$

where ω_o is the output frequency, ϕ is the phase of the open loop transfer function. According to Barkhausen Theory described earlier, oscillation occurs when the open loop phase shift around the loop is zero. Hence for large deviations of the output frequency from ω_o, the phase shift would be more and would reinforce output frequency closer to ω_o. Figure 2.6a shows a complete differential LC oscillator. In any harmonic oscillator



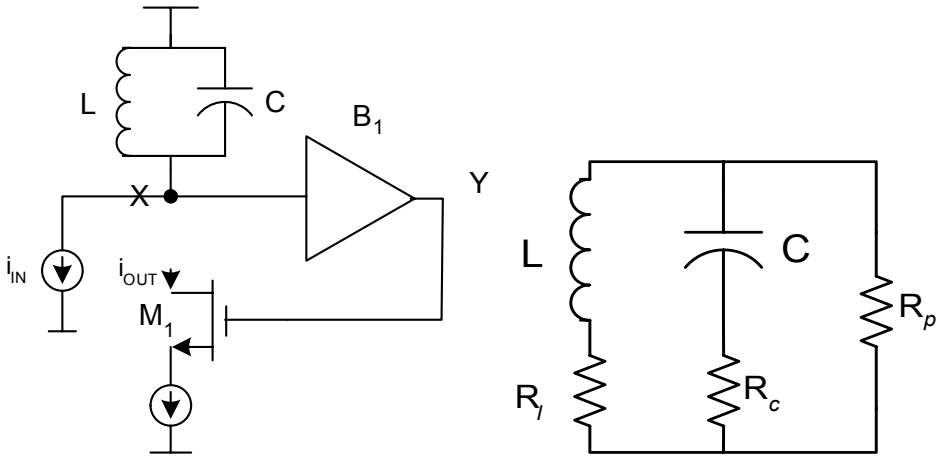
a. Differential LC oscillator schematic b. Equivalent single ended circuit

Figure 2.6: Differential LC-VCO topology

such as the LC-VCO the signal from the resonant circuit or the LC tank is fed back to the amplifier such that the impedance of the tank is not affected and required phase shift is also maintained. In the differential configuration a buffer using M_2 is used to feedback the signal from the first tank circuit as shown in Figure 2.6b. To estimate the open loop function the loop is broken at one end of tank circuit at X as shown in Figure 2.7a and an AC current source i_{IN} is inserted. The Equivalent Impedance of the tank circuit is shown in Figure 2.7b is given by

$$Z_{\tan k} = (sL + R_l) \| (sC + R_c) \| R_p \tag{2.8}$$

where R_l is the equivalent inductor resistance, Rc is the equivalent capacitor resistance, R_p is the resistance across the tank. The series resistances can be transferred to an equivalent parallel resistance. If R_{pl} represents the equivalent parallel resistance of the inductor, R_{pc} the equivalent parallel resistance of the capacitor. Then the equivalent parallel resistance ig given by $R_{peq} = R_p \,||\, R_{pl} \,||\, R_{pc}$. The voltage V_X at node X is given by



a: Equivalent Open Loop Circuit b: LC tank circuit

Figure 2.7: Open loop tank circuit

$$V_X = (sL \,||\, 1/sC \,||\, R_{peq}) * i_{IN} \tag{2.9}$$

The other cross-coupled transistor in this case M_2 acts a unity gain-inverting buffer. Hence the voltage V_Y at the node Y is given by

$$V_Y = V_X = (sL \,||\, 1/sC \,||\, R_{peq}) * i_{IN} \tag{2.10}$$

The drain current can be expressed as

$$i_{OUT} = gm * v_{gs} = gm * V_T = gm * (sL \left\| (1/sC) \right\| R_{peq}) * i_{IN} \tag{2.11}$$

Hence the open loop gain

$$\frac{i_{OUT}}{i_{IN}}(s) = \frac{sLR_{peq}gm}{s^2 LCR_{peq} + sL + R_{peq}} \tag{2.12}$$

$$\frac{i_{OUT}}{i_{IN}}(\omega) = \frac{j\omega R_{peq}L}{-\omega^2 LCR_{peq} + j\omega L + R_{peq}} \tag{2.13}$$

Open Loop phase shift

$$\phi = \frac{\pi}{2} - \tan^{-1}\frac{\omega L}{R_{peq} - \omega^2 LCR_{peq}} \tag{2.14}$$

$$\frac{d\phi}{d\omega} = \frac{R_{peq}L(1+\omega^2 LC)}{(1-\omega^2 LC)^2 + \omega^2 L^2} \tag{2.15}$$

$\left|\frac{d\phi}{d\omega}\right|_{\omega=\omega o} = 2CR_{peq}$, where the output frequency $\omega o = \frac{1}{\sqrt{LC}}$, Hence Q-factor can be expressed as

$$Q = \frac{\omega_0}{2} * \frac{d\phi}{d\omega} = \omega_o CR_{peq} = \frac{R_{peq}}{\omega_o L} \tag{2.16}$$

$$R_{peq} = \omega_o QL \tag{2.17}$$

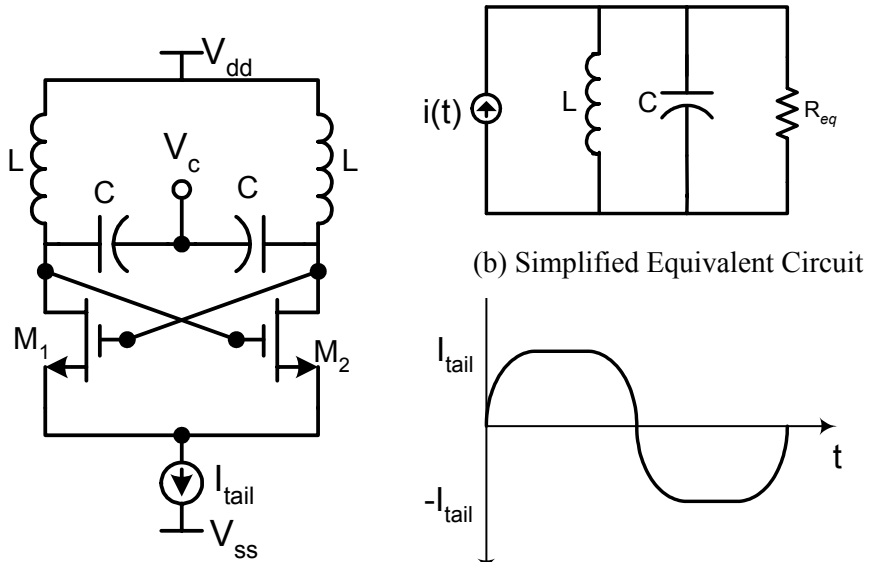
For an ideal oscillator $R_{peq} * gm = 1$, but in real design a safety factor α ranging from 1.5-3 is used. Hence the transconductance of the cross coupled transistors gm is given by

$$gm = \frac{\alpha}{\omega_o QL} \tag{2.18}$$

This is one of the key design equations for LC-VCO design.

2.5 Principle of LC oscillator

Deep insight into the design of optimized LC-VCO is possible only with the firm understanding of the trade-offs among the design parameters. This is essential to enhance circuit innovations and increase design productivity. Figure 2.8a shows a differential LC oscillator with NMOS differential pair, Figure 2.8b shows a simplified perspective of an LC oscillator. Here the equivalent current source *i(t)* is parallel with the resistance-inductance-capacitance (R_{eq}LC) tank. For a fully differential network the tail current is steered from one NMOS transistor to another. Hence i(t) can be considered as a pulse input which switches between I_{tail} and $-I_{tail}$ as shown in Figure 2.8c [17] . The LC tank functions as a bandpass filter whose center frequency is the resonant frequency of the tank and thus the tank filters all the harmonics of the fundamental frequency. At resonance the inductive and capacitive impedance cancel one another and thus the tank impedance is the equivalent parallel resistance R_{eq}. The resultant peak amplitude of the differential output is given by



(a) Differential LC Oscillator

(b) Simplified Equivalent Circuit

(c) Current Waveform

Figure 2.8: Functional block diagram of a LC oscillator

$$V_{amp} = \frac{4}{\pi} I_{tail} \times R_{eq} \tag{2.19}$$

At high frequencies the switching current can be closely approximated by a sinusoidal signal due to finite switching time and limited gain and the peak amplitude can be approximated to

$$V_{amp} = I_{tail} \times R_{eq} \tag{2.20}$$

Since the output depends only on the tail current this region of operation is referred as the *current limited* regime of operation. Figure 2.9 shows the simulated drain currents of the differential pair, the tank is designed to oscillate at 1.8 GHz. The tank energy E_{tank} is given by

$$E_{\tan k} = \frac{C \times V_{\tan k}^2}{2} = \frac{V_{\tan k}^2}{2\omega_o^2 L} \tag{2.21}$$

So in other words the tank amplitude V_{tank} can be expressed as a function of inductance

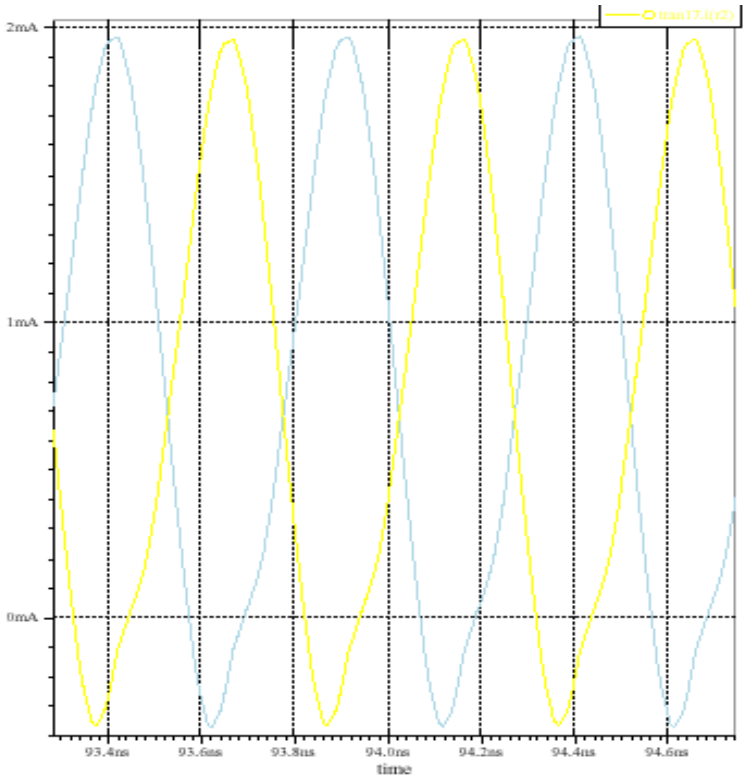


Figure 2.9 : Simulated drain currents in current mode

$$V_{\tan k} = \omega_0 \sqrt{2E_{\tan k}} L \tag{2.22}$$

The tank amplitude grows with the independent variable inductance L when all other variables are kept constant and hence this mode of operation is also referred as *inductance – limited mode*. Any equation valid in the current limited mode is also valid in inductance limited mode. V_{tank} grows with the bias current built-up or inductance until it reaches a saturated limiting voltage V_{limit} close to the supply voltage, this region is referred as *voltage limited mode* of operation. In this mode the PMOS transistor (current source) enters the triode region and the drain current does not stay constant and hence there is a huge drop in the V_{DS} in the differential pair.

Figure 2.10 shows the plot of drain current and output swing in this region of operation for different supply voltages. The tank amplitude is proportional to the tail current in the

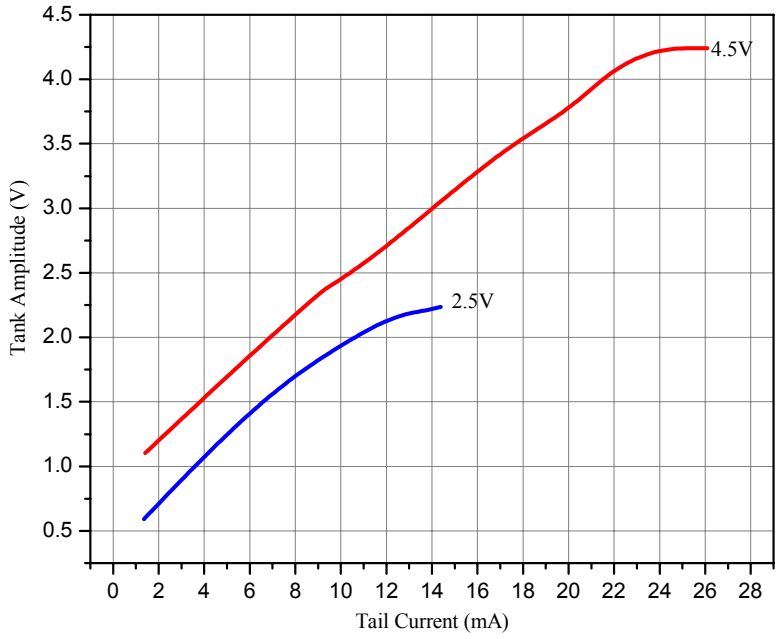


Figure 2.10 : Simulated tank voltage vs tail current

current limited region, while it is limited by the supply voltage in the voltage limited region.

2.6 Other VCO architectures

Earlier discussions were based on the widely used harmonic LC-VCO for wireless application. Other non-linear VCO architectures are also used in less noise critical applications. Some of the widely used architectures are discussed here

2.6.1 Ring oscillator

This is one of the most commonly used VCO configurations for realizing digital output. In simple terms, a ring oscillator architecture is a simple chain of odd number of inverters in a feedback loop as shown in Figure 2.11.

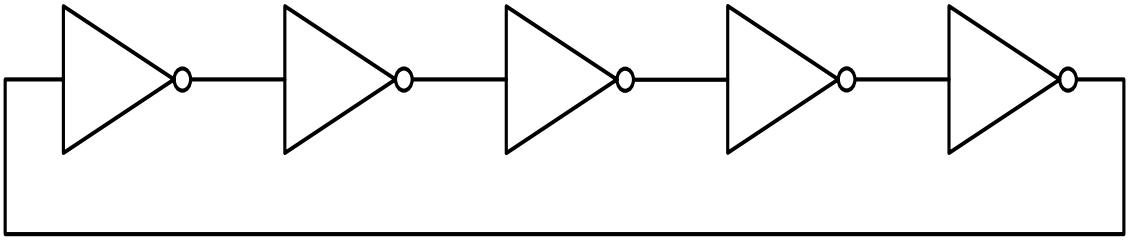


Figure 2.11 : A ring oscillator realized using five digital inverters

Each inverter provides approximately 90° phase shift at its unity gain frequency and hence the total phase shift in the forward path will always be greater than 180°. Thus the system is guaranteed to have a loop gain greater than unity and hence is unstable and oscillations occur. Assuming each inverter provides a delay τ_{inv}, the delay through n inverters is equal to half the time period of oscillation

$$\frac{T}{2} = n\tau_{inv} \tag{2.23}$$

Thus the frequency of oscillation:

$$f_{osc} = \frac{1}{2n\tau_{inv}} \tag{2.24}$$

By varying the delay of each inverter cell through an external control voltage, a VCO can be implemented. A simple ordinary CMOS inverter cannot be used for the unit cell inverter in ring VCO because of its poor power supply rejection.

A better scheme would be to use an even number of fully differential inverters. A simplified fully differential inverter cell is shown in Figure 2.12 [16]. The current source can be externally controlled by V_{cntl}. This configuration also provides high output impedance because of the cascode transistors Q_3 and Q_4 thus providing good power supply rejection. The delay of each inverter is proportional to the unity gain frequency. Thus

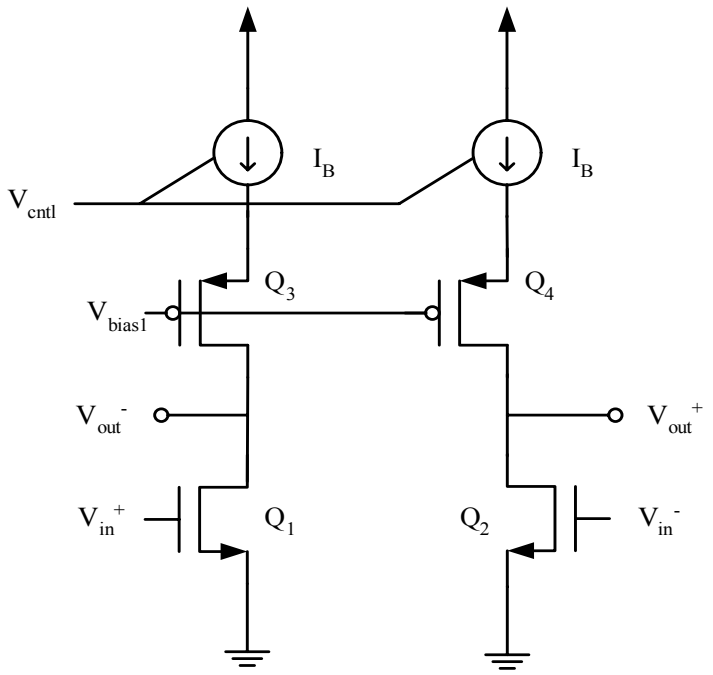


Figure 2.12 : A fully differential inverter with a programmable delay

$$\tau_{inv} \propto \frac{C_L}{g_m} \tag{2.25}$$

where C_L is the load capacitance, *gm*, the transconductance of the drive transistors

$$gm \propto \sqrt{I_B}\ , \text{thus } \tau_{inv} \propto \frac{1}{\sqrt{I_B}} \propto \frac{1}{\sqrt{V_{cntl}}}$$

Thus the relationship between the oscillation frequency and the control voltage is not linear, but in many VCO applications this non-linearity is not a constraint. Recently a number of ring VCO architectures are being developed with better linearity. The main disadvantage of a ring VCO compared to LC VCO is the poor noise performance thus limiting its application in wireless communication.

2.6.2 Relaxation oscillator

Another popular method of realizing a digital output is the relaxation oscillator. A typical circuit configuration using is shown in Figure 2.13. In this oscillator topology C_1 and C_2 are charged and discharged alternatively by the wide swing current mirror. The current through the cascode tail current transistors Q_5, Q_7 is equal to $\frac{V_{cntl}}{R}$ due to negative feedback. The voltage across the capacitor C_1, C_2 is fed as the input to the SR latch to set or reset the output Q and Q'. These outputs control the states of Q_1-Q_4. For example if Q is high and Q' is low. This causes Q_1 and Q_4 to turn on and Q_2 and Q_3 to turn off. This discharges C_1 and charges C_2. Once the capacitors have reached the threshold voltage, the SR latch is reset. This completes half a period of oscillation. The comparator provides better power supply rejection than directly connecting the capacitor outputs to the SR latch input. By varying the control voltage, the tail current can be varied. This will vary the charging and discharging time of the capacitors and thus the frequency of oscillation.

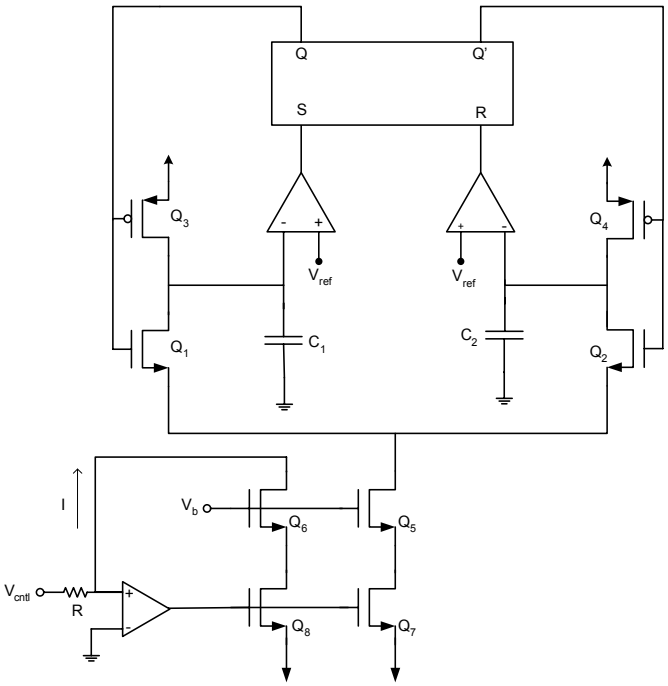


Figure 2.13 : A CMOS relaxation oscillator

2.6.3 Interpolative oscillator

All the previously discussed VCO configuration employed just one mode of varying the frequency such as a variable capacitor or resistor only. In Interpolative Oscillators the output signal is the sum of 'n' resonator outputs. Hence frequency can be varied not only by varying the resonant frequency of each tank sub system but also by varying the gain of each sub-block as shown in Figure 2.14 [15]. Here the open loop response H(s) is given

$$H(s) = \alpha_1 * H_1(s) + \alpha_2 * H_2(s) + \cdots\cdots\cdots\cdots \alpha_n * H_n(s) \qquad (2.26)$$

where α_1, α_2, …., α_n are the variable gains of each sub stage. For any system to oscillate according to Barkhausen theory total loop gain should be unity $H(s) - 1 = 0$

$$\alpha_1 * H_1(s) + \alpha_2 * H_2(s) + \cdots\cdots\cdots\cdots \alpha_n * H_n(s) - 1 = 0 \qquad (2.27)$$

By varying the control voltage such that the loop gain is unity, the system will oscillate for different combinations of α_n, thus providing a very large tuning range. Each sub-system has its own self resonant frequency; hence the output can have multiple frequency components. From a performance perspective the systems has very low spectral purity, hence limited in wireless application. Moreover it is very difficult to find a continuous range of control voltage such that the system oscillates.

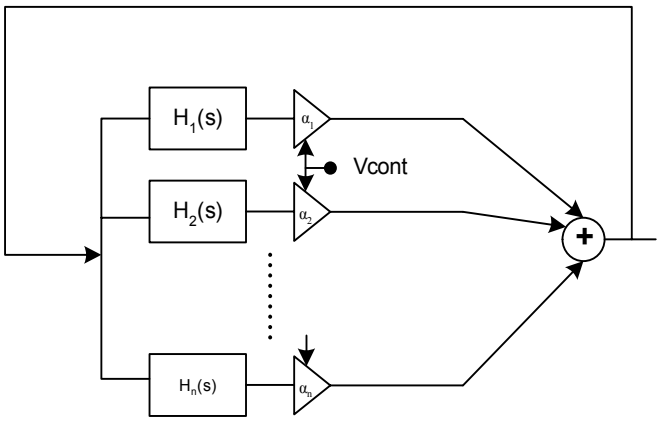


Figure 2.14 : Interpolative oscillator

3 INTEGRATED INDUCTORS AND VARACTORS

Phase Locked Loops (PLL) are widely used as frequency synthesizers, clock and data recovery circuits and carrier synchronization circuits in wireless application. Effective performance of PLL for these applications depends extensively on the implementation of the most critical component voltage controlled oscillator (VCO). Of the various implementations of VCO discussed in the earlier sections LC-VCO is the best choice in terms of noise performance. The major constraint in the implementation of integrated wireless communication device in silicon is the development of an integrated inductor as well as the high Q-factor varactor.

In this chapter, various means of realizing integrated inductors have been explored and finally, the most viable implementation of the spiral inductors in terms cost, high frequency of operation and repeatability has been elaborately analyzed. Different means of developing varactors in standard CMOS technology have been studied and a new novel scheme of using MOS transistors in accumulation mode body driven varactor has been presented. A simplified equivalent circuit for the body driven varactor has also been developed.

3.1 Importance of integrated inductor

As discussed in Chapter 1, there is a great need to develop a completely integrated transceiver system. The frequency limit used for commercial application is increasing everyday. As the desired frequency of operation increases the values of the inductance and the varactor capacitance decreases. Table 3.1 gives a general overview of the frequency of operation and the required inductance. Figure 3.1 [18] shows the different parasitic inductance associated with the bondpad and the package. The total effective inductance is the sum of the off-chip inductance and the parasitic inductance given by Eq (3.1)

Table 3.1: Inductance variation with frequency

Frequency	Inductance	Capacitance
10 MHz	253.3 μH	1 pF
100 MHz	2.53 μH	1 pF
1000 MHz	25.3 nH	1 pF
10000 MHz	0.253 nH	1 pF

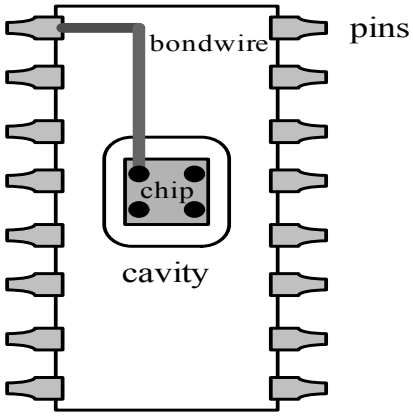


Figure 3.1 : Typical bonding diagram

$$L_{eff} = L_{offchip} + L_{pin} + L_{bondwire} \tag{3.1}$$

The bondwire inductance usually varies between 4.5 nH – 2.95 nH [19] depending on the package. The package inductance is usually around 0.5 nH. These parasitic effects are negligible at low RF frequencies. But at high frequencies around of 1 GHz the parasitic inductance becomes a substantial percentage of the total effective inductance. This reduces the performance of the effective inductor since substantial part of the effective inductance is contributed by the low Q-factor parasitic inductance. Thus although off-chip inductors can be used at around 1 GHz, the performance of these inductors are deteriorated. The problem is worse at higher frequencies of around 10 GHz, where the effective inductance required is only 0.253 nH for 1pF capacitance. Such a low value of inductance cannot be realized externally even with the best tiny package. Thus there arises a need for pondering new means of realizing integrated for wireless applications.

3.2 Integrated inductor design

The successful implementation of the LC VCO oscillator depends extensively on the performance of high Q integrated inductors. In the past the electronic circuits using inductors were rarely used due to their bulky and noisy nature. But in the current revolution for wireless communication products which require high spectral quality carrier signals which as per discussions in the earlier chapter points to the use LC VCO. Hence a lot of work is currently being pursued to build area efficient high performance inductors integrated with other transceiver circuits in a single die. The main constraint in this approach is the unavailability of standard modeled inductors in standard CMOS process. Currently there exist the following methods to implement integrated inductors:

3.2.1 Active inductors

In this method, the function of an inductor is emulated by using other passive elements and active elements. Figure 3.2 [20] shows a simplified implementation of an active inductor. The two transconductance amplifiers are connected back to back and a passive capacitor emulates the function of an inductor. Here g_{m1} and g_{m2} represent the effective transconductance gain of the two amplifiers respectively and C is the passive capacitor.

To derive an expression for the effective inductance the two amplifiers are considered ideal and an input V_{in} applied at the input of the active inductor, then the output current of the first op-amp I_{out} is given by Eq (3.2)

$$I_{out} = g_{m1} * V_{in} \tag{3.2}$$

The output voltage at the capacitive load V_{out} can be expressed as

$$V_o = I_{out} * (1/sC) = g_{m1} * (1/sC) * V_{in} \tag{3.3}$$

The input referred feedback current I_{in} is given by

$$I_{in} = -V_o * (-g_{m2}) = g_{m1} * g_{m2} * (1/sC) * V_{in} \tag{3.4}$$

The effective input impedance Z_{in} is given by

$$Z_{in} = \frac{sC}{g_{m1} * g_{m2}} \tag{3.5}$$

The equivalent inductance L_{eq} is given by

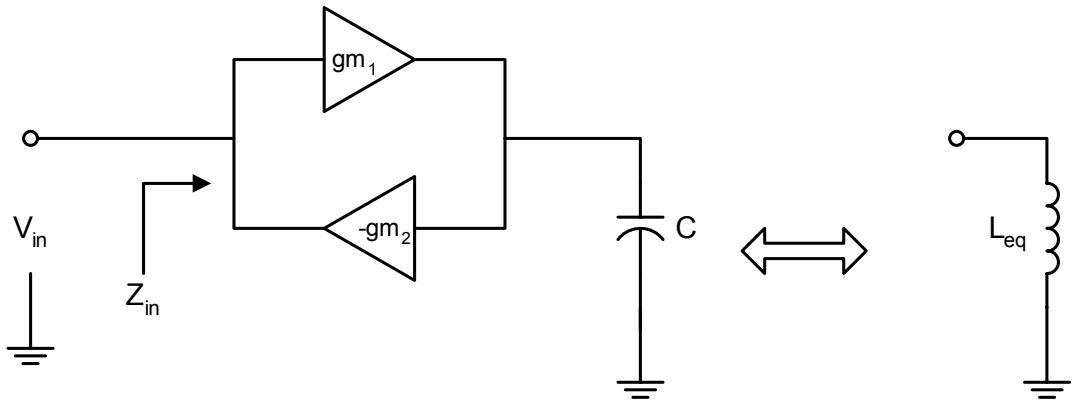


Figure 3.2: A gyrator based active inductor

$$L_{eq} = \frac{C}{g_{m1} * g_{m2}} \tag{3.6}$$

The resonant frequency of the tank circuit can be varied by controlling the transconductance gain g_{m1} and g_{m2}. This provides very large tuning range, which is the main advantage of this implementation. Moreover this type of inductor implementation offers other advantages like small area and simple implementation.

But the major disadvantage of this implementation is the noise performance. Noise generated by both the amplifiers would add to the total tuned circuit noise. Figure 3.3[21] shows the equivalent noise sources assuming each op-amp have an equivalent input referred noise voltage E_{gm} given by

$$E_{gm} = 4kT\frac{F}{g_m}\Delta f \tag{3.7}$$

where Δf is the noise bandwidth in Hz and F is the noise factor that is dependent on the particular op-amp design. The equivalent noise sources of the inductor can be calculated from Eq (3.8)

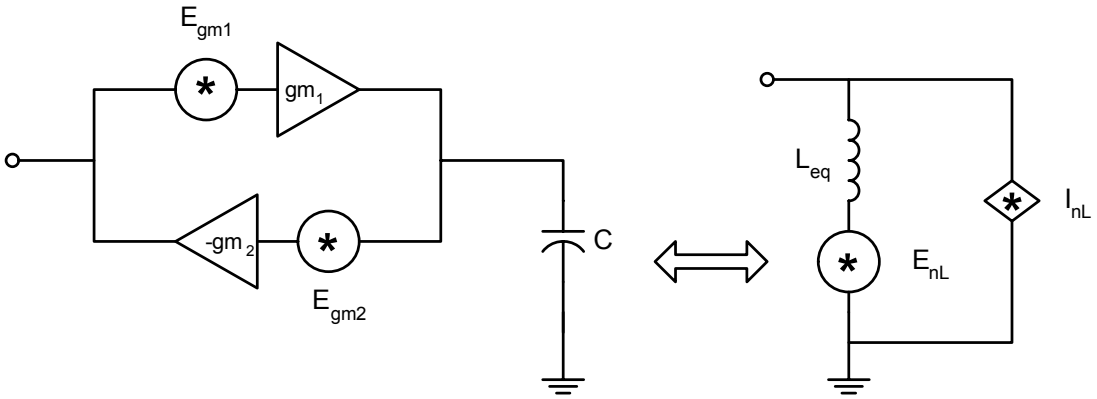


Figure 3.3: Equivalent noise circuit

$$E_{nL}^{\ 2} = E_{gm1}^{\ 2} = 4kT\frac{F_{gm1}}{g_{m1}}\Delta f \tag{3.8}$$

$$I_{nL}^{\ 2} = g_{m2}^{\ 2}E_{gm2}^{\ 2} = 4kTF_{gm2}g_{m2}\Delta f \tag{3.9}$$

Eq (3.8) and Eq (3.9) shows that the both the transconductance amplifier equivalent noise source contribute to the total inductor noise. The main purpose of using a LC-VCO in GHz range is to obtain carrier signals of high spectral purity. Even though active inductors offer wide tunabilty, this is inadequate for wireless applications.

3.2.2 Bondwire inductors

Another method of implementing an integrated inductor is to use the parasitic inductance of the bonding wire in an IC package. Figure 3.4 [20] shows a typical cross-section of the differential bondwire inductor. The inductance can be roughly calculated as 1nH per mm. Usually gold or aluminum are used as bondwire in standard IC package. The series resistance per unit length is given by

$$R_{series} = \frac{\rho}{A} \tag{3.10}$$

where ρ ,the resistivity of the wire is related to skin depth δ and permeability μ is given

$$\rho = \frac{\delta^2 \omega\mu}{2} \tag{3.11}$$

For a 1mm Al or Au at 1GHz, the skin depth is approximately 2.5μm which is relatively small compared to the typical radius of the bondwire (25 μm). Hence the area of the cross section A can be approximated as $2\pi r$. Substituting the values of permeability of Au for 1 GHz frequency the series resistance can be approximated as 125 mΩ per mm length [20]. Since the bondwire inductors have very low series resistance, or stated differently from a designers perspective, they have very high Q-factor of around 200, a very desirable characteristic of any resonant circuit.

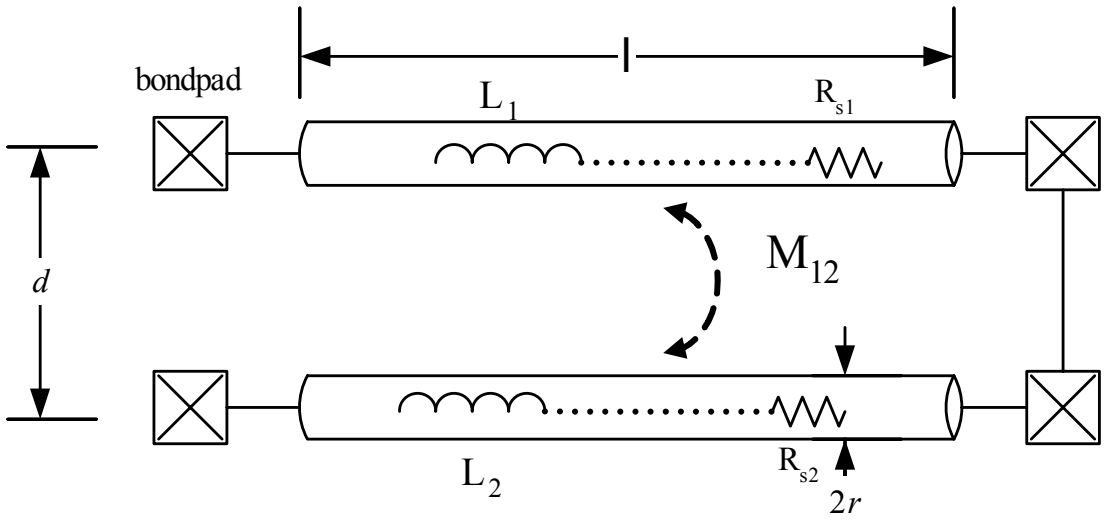


Figure 3.4 : Differential bondwire inductors

The parasitic capacitance of the bondwire to ground is very small if they are placed sufficiently far above any conducting planes. Hence the major contributor to the effective parasitic capacitance of these inductors is the bondpad capacitance. If the inductor is used differentially then the common end bondpad capacitance can be ignored. Hence the parasitic capacitance is the one from the two bondpads at the beginning and end of the bondwires.

Differential bondwire self inductance *L* and mutual inductance *M* can be approximated by Eq (3.12) and Eq (3.13) respectively, including only the first order effects[20]

$$L = \frac{l}{5}\left[\ln\left(\frac{2l}{r}\right) - 0.75 + \frac{r}{l}\right] \tag{3.12}$$

$$M = \frac{l}{5}\left[\ln\left(\frac{l}{d} + \sqrt{1+\left(\frac{l}{d}\right)^2}\right) - \sqrt{1+\left(\frac{d}{l}\right)^2} + \frac{d}{l}\right] \tag{3.13}$$

where l is the conductor length, r is the radius of the cross-section, d is the distance between the two bondwires. Any value of inductance can be achieved by varying the length of the bondwire. Higher values of inductance can be obtained using chip –to-chip

bondwire. All the equations have been described for an ideal straight bondwire with no variations in radius or length, but the radius and length of a practical bondwire varies, which leads to the major shortcomings of this method. Figure 3.5 shows a typical cross-sectional view of a bondwire inductor. The bondwire is extended vertically and then bend horizontally. For the above inductance equations to be true the bondwire should be extended vertically atleast for a length of 150μm, for a 50μm change in vertical length the inductance changes by 2% for a 4mm long bondwire. Similarly the horizontal wire may not be completely straight as shown in Figure 3.5. A bend in the wire will cause unpredictable variation in the inductance especially the vertical bend. The change in the mutual inductance due to a horizontal bend will be more severe than the vertical bend. Finite element simulations can model most of this effect.

The other parameter that influences the inductance is the wire radius *r*. Inductance varies with the logarithm of the *r*, the effect is somewhat less compared to other variation. All of these variation effects account for around 3-4%[20] variation in inductance. Apart from these there is an additional 2-3% safety margin due to imperfect modeling effects. Combing all these effects, bondwire inductance can vary by around 8 %. This large spread of bondwire inductance manifests the use of varactor with large tuning range to tune out the inductor variation. Good high tuning range varactors are difficult to realize in standard CMOS technology. Hence for commercial implementation of integrated LC-VCO bondwire inductance is usually avoided.

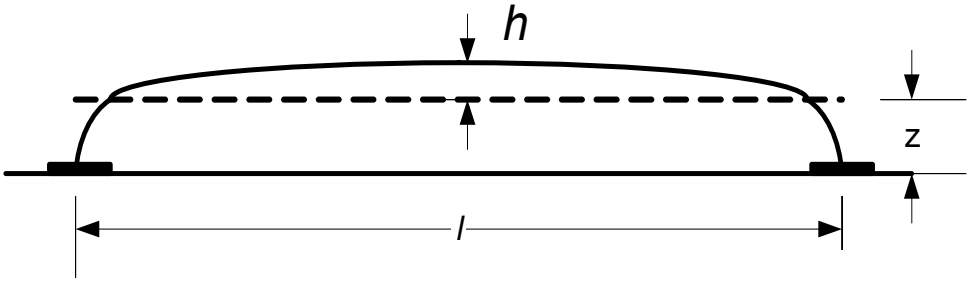


Figure 3.5: Bondwire inductor cross-section

3.2.3 Inductor on a package

Another method of integrating inductors is through thin film multi chip module technology (MCM) to connect multiple chips. The individual sub-RF blocks can now be implemented in the most suitable IC technology and can be eventually assembled in a relatively simple and economical way. An optimal partitioning of the system into the sub-blocks will lead to lower cost, increase of manufacturing yield and superior performance. Figure 3.6 shows the typical cross-section of a MCM technology [22] . It consists of alternating layers of a dielectric with ε_r = 2.7 and copper conductors stacked on high resistivity silicon, a borosilicate based glass or a low loss ceramic carrier substrate. An important advantage of this technique is there is no substrate coupling through the common substrate. Using this technology high performance and relatively cheap passive elements can be implemented directly in the MCM substrate. Inductors with values between 1-40 nH and Q-factors up to 50 can be achieved depending on the inductance, can be realized using highly conductive Cu as well as capacitors up to 1 nF/mm^2 (Ta_2O_5). Figure 3.7 [22] shows a photograph of a spiral inductor in MCM. The center of the spiral is connected to the outside through an underpass on a lower metal layer. The flip chip technology has much smaller parasitics than bonding wires. Using these high quality passive devices a number of passive circuits such as RF bandpass filter, matching networks, baluns, power splitters, combiners, antennas etc. can now be implemented in a

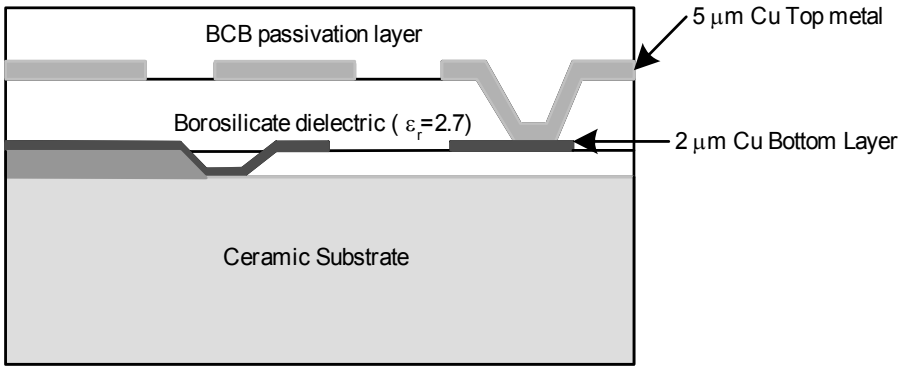


Figure 3.6: MCM-D layer architecture

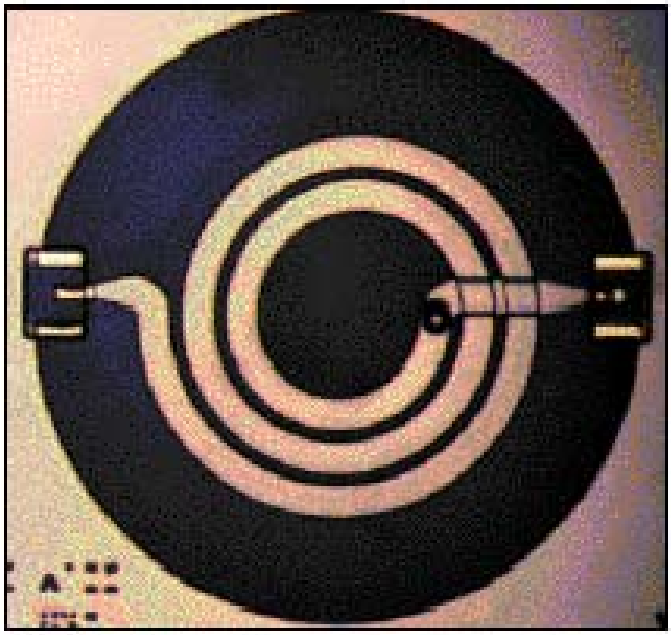


Figure 3.7: Photograph of a high Q spiral inductor in MCM-D

single package. In addition this technology provides an opportunity to integrate micro electro-mechanical systems (MEMS) which are utilized in numerous sensor circuits. The design of single package RF systems requires a good understanding of the features and limitations of different IC technologies and of the interconnection technologies.

3.2.4 Spiral inductors

A very practical and most widely accepted integrated inductor implementation is by utilizing one or more metal layers in the standard IC process. Figure 3.8 shows a cross section of metal layers of a standard IC process. Passive devices such as resistors, inductors and capacitors can be constructed from the metal and the polysilicon layers.

The conductivity of these metal layers plays an integral part in determining the Q-factor of such inductors, a very important performance determining parameter of inductors. Al has a conductivity $\sigma = 3.65 \times 10^7$ S/m, usually the metal layer thickness ranges from 0.5 μm to 4 μm resulting in sheet resistance values from 55 mΩ/□ to 7 mΩ/□ [23]. Other

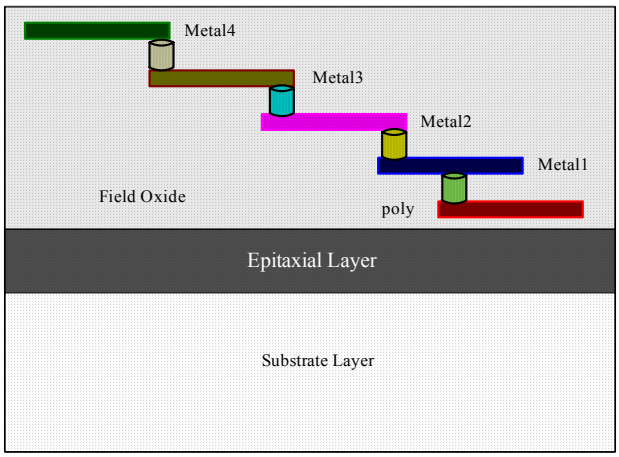


Figure 3.8: Cross-section of typical CMOS substrate layer

metals like Au, Ag, Cu have a lower sheet resistance than aluminum, but currently only aluminum is compatible with the standard IC process. A lot of research is currently being pursued to utilize the lower sheet resistance of Cu for better metal interconnect, the success of this research would further improve the performance of Si planar on-chip inductors. Each metal layer of different conductivity is fabricated by various processes such as diffusion, chemical vapor deposition and growth, epitaxy and ion implantation. The metal composition is slightly varied by mixing Al with other metals such as platinum, palladium, titanium and tungsten to overcome some of the limitations of Al like spiking, junction penetration etc. Electromigration in Al is another limitation, setting an upper bound on the maximum current density. This limits the application of Si integrated IC using on-chip inductors for high power applications like power amplifiers. For such applications the necessary metal width requires large areas resulting in lower self resonant frequencies limiting the application frequency. In some modern CMOS technology a thick top metal layer is used for high-speed digital blocks for reducing clock line delays. This top layer can be utilized for fabricating high quality spiral inductors with very low resistive losses and thus achieve high Q-factor. This top thick metal in many IC process resides on the top of an extra thick insulator for minimum substrate capacitance. The option of so many metal layers along with the interconnections results in wide varieties of inductors with no special IC processing steps in modern CMOS process.

3.3 Loss mechanism of on-chip inductor

In order to design the optimum inductor for a particular application, an insight into the various losses of the planar spiral inductor is necessary. For any inductor structure the change in the current distribution causes many undesirable effects such as skin effect, current constriction and current crowding. The alternating electric current always takes the path of the lowest impedance. The current tends to accumulate in the outer layer since magnetic field of the inductor produces opposing electric field. This opposing field follows a $\sqrt{f}$ dependence. The AC resistance increases with opposing field and this effect is known as *skin effect*. At high frequencies the effective cross-sectional area of the conductors decreases, thus increasing the current density. This causes more electric energy being lost as heat. At high frequencies the skin effect is expressed as depth of penetration δ given by Eq (3.14).

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{3.14}$$

where μ is the permeability and σ is the conductivity. The depth of penetration varies inversely with square root of frequency.

The above discussion considered the effect of a single metal layer. In a multi conductor system such as fully differential LC VCO, proximity effects due to mutual magnetic field affects the self inductance. If the coupling magnetic field adds to the self induced magnetic field, then the AC resistance increases.

Figure 3.9 [43] shows the loss current distribution for a spiral inductor. All the effects discussed above are independent of the substrate effects. In a standard CMOS process another source of loss and frequency limitation is the conductive Si substrate. The conductivity of Si varies with the doping concentration between 0.1 mS/cm for lightly doped Si (10^{13} atoms/cm^3) to 10^3 S/cm for heavily doped Si (10^{20} atoms/cm^3) [23]. The conductivity of the substrate causes some electromagnetic energy to be lost as heat. The

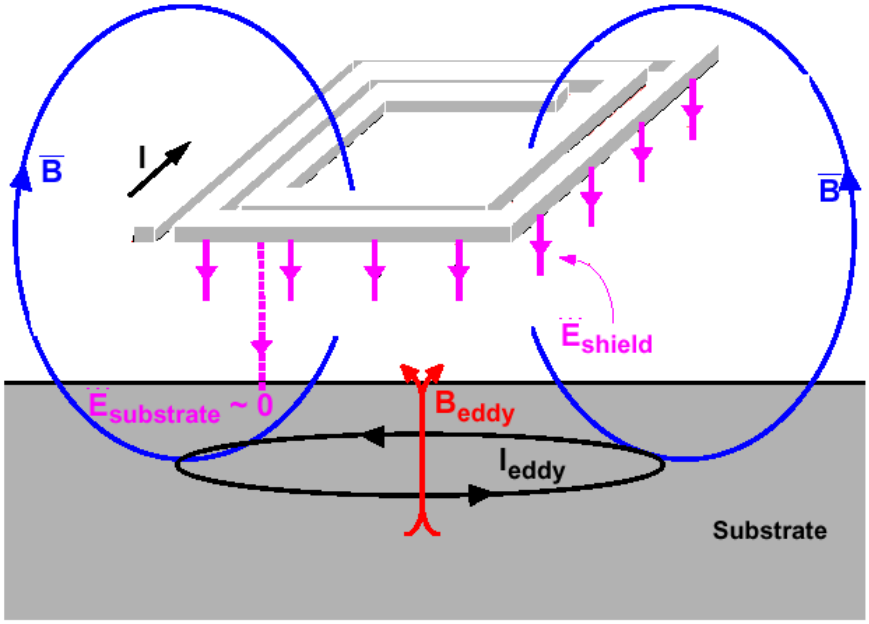


Figure 3.9: Loss current distribution of a spiral inductor

electric energy loss appears as a displacement current that flows through the substrate to nearby grounds. Another form of substrate loss is due to the time varying solenoidal electric field produced by the magnetic field. This electric field induces substrate currents perpendicular to the spiral segments. At high frequencies electromagnetically induced losses result when the physical dimensions of the devices approach the wavelength of propagation. This loss is very negligible even at 100 GHz frequency since the wavelength (3mm) becomes larger than the device dimension (submicron). Electromagnetic propagation into the substrate occurs at lower frequencies due to the lower propagation nature of Si and the wave propagation behaves like a "quasi- TEM" mode. The propagation speed is proportional to $\sqrt{\varepsilon_{Si}}$, slightly lower than the propagation in free space

.

3.4 On-chip spiral inductor modeling

The behavior of spiral inductors have been modeled in several ways [24][25] [26] . Figure 3.10 shows one of the most tangible model widely employed. It is composed of an ideal inductor L in series with the series resistance of the spiral R_s, which is a frequency dependent parameter. The substrate loss is modeled as a lumped coupling capacitor C_{ox1} and C_{ox2} at the two ends in series with the substrate resistance R_{SUB1} and R_{SUB2} which are also frequency dependent resistances. The structure of most spiral inductors configuration is not symmetric, and hence their geometric center and the electric center are slightly different. Hence the parasitic coupling substrate capacitances at the two end terminals vary slightly. The difference however is very small and the two capacitors are assumed to be the same for most geometrically symmetrical structures. C_p represents the coupling capacitance between the two terminals due to fringing fields in both the dielectric region and the air region. A capacitive split between C_{sub1} and C_{sub2} models the capacitance across the substrate. To simplify the equivalent model the coupling capacitor C_p and the substrate capacitance are neglected. This is valid since the related capacitance is very small and the inductor is operated at frequencies well below

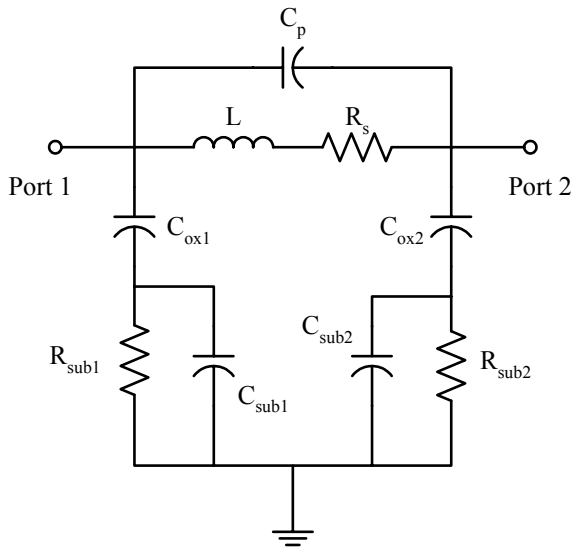


Figure 3.10 : Equivalent model of a spiral inductor

its self-resonant frequency. Hence the model shown in Figure 3.11 is a valid simplified model for the spiral inductor.

A lot of work has been done to derive an accurate formula for the inductance of a spiral inductor. Greenhouse [24] provides an empirical formula, which differs, from the experimental results by less than 10%. This was further proved by Nguyen et al.[28] . Further Remak and Burdick have derived formulas for calculating the inductance of a circular spiral, which differs from the actual measurements by less than 8%. Figure 3.12 shows the inductance variation with number of turns and outer dimension for a square spiral with width W=18 μm, and spacing between the metal lines S=3 μm. Eq (3.15) [29] provides a general empirical formula for inductance.

$$L = l(1.05 + 0.19n) \tag{3.15}$$

$$l = 1.027 \frac{\pi}{S + W}\left(R_o^2 - R_1^2\right) \tag{3.16}$$

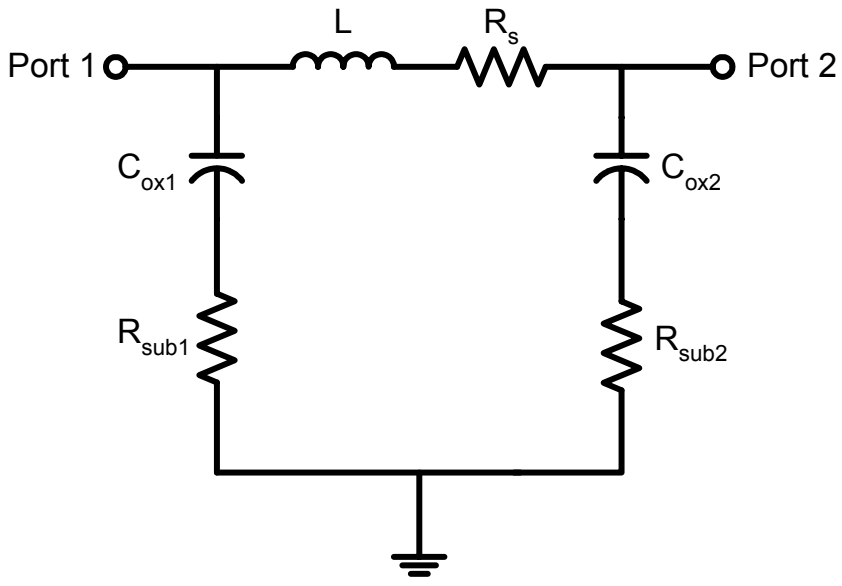


Figure 3.11 : Simplified model of a spiral inductor

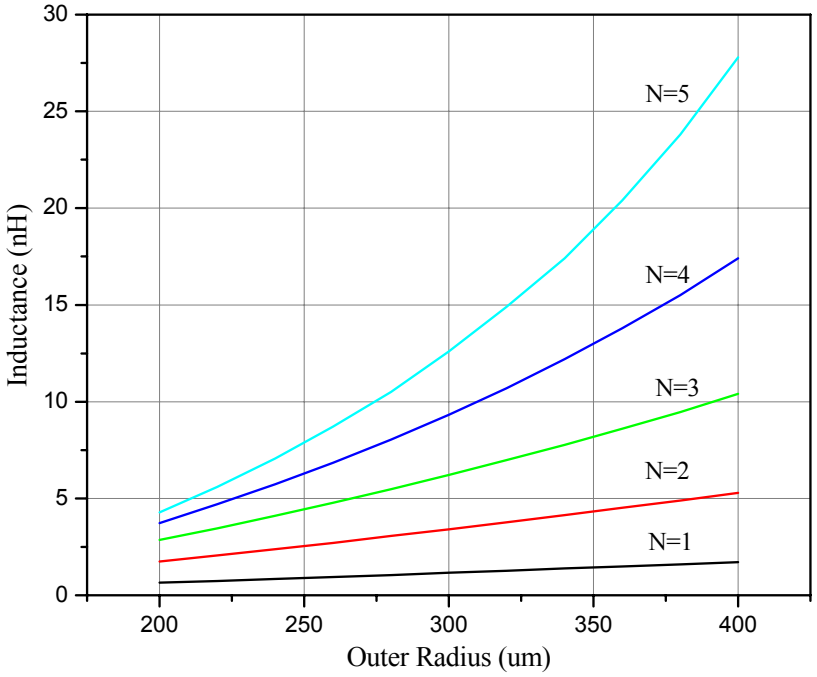


Figure 3.12: Inductance variation with physical dimensions

where l represents the spiral inductor length, n is number of turns, S is metal spacing, W is the wire length, R_o, R_I are the distance from the center of the inductor to the middle of the outermost and innermost segment respectively. However the simple empirical formulas described in Eq 3.15 is valid only for planar spiral inductors. For other inductor types using one or more metal layers or tapered inductors the simple empirical formula fails to hold true. A better means of modeling inductance is to utilize commercial simulators like ASITIC, EESOF, Momentum, APLAC, and Fast Henry which incorporate complex matrix capability for calculation. In the current research inductor models were developed using ASITIC (developed by Ali. M. Niknejad, UC Berkeley). Brief discussion on ASITIC has been provided in the latter section.

As described earlier the series resistance of the spiral R_s, parasitic parallel substrate resistance R_{SUB1}, R_{SUB2} are all frequency dependent elements. Eq (3.17) express the series resistance variations with frequency empirically [30]

$$R(f) = R_o\left(1 + k_1 f^{k_2}\right) \tag{3.17}$$

where R_o is the DC resistance, which can be calculated as the sheet resistance multiplied by the number of squares. The empirical constants k_1 and k_2 can be calculated by curve fitting measured data. For 0.35 μm technology Figure 3.13 shows variation of R_s with frequency and the extracted k_1 and k_2 values using curve fitting has been found to be -1.844×10^{-3} and 1.7×10^{-3}, respectively.

The capacitance can also be expressed empirically by Eq (3.18) [31]

$$C_{AV} = C_A(A_{IND} + A_{FR} - A_{BR}) \tag{3.18}$$

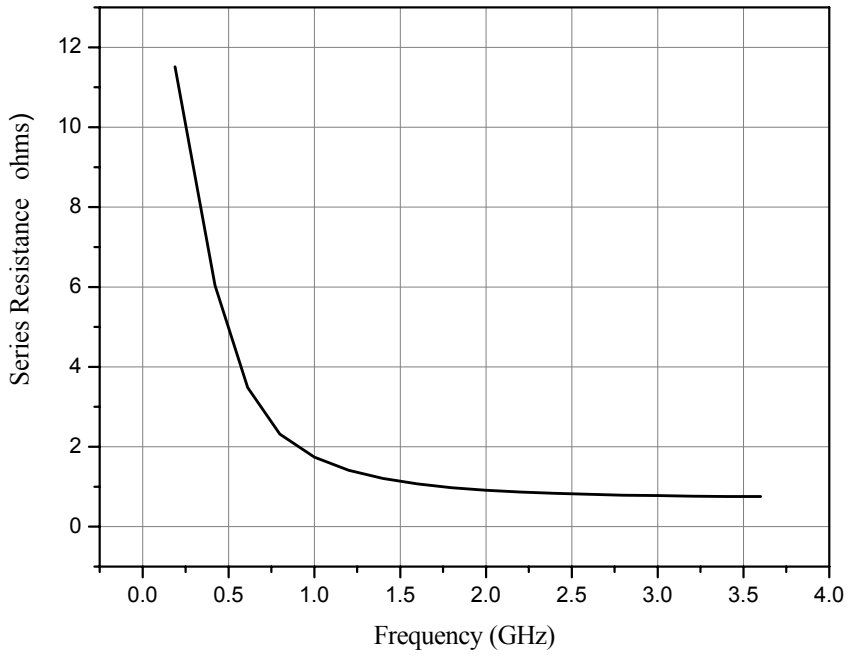


Figure 3.13 : Series Resistance variation with frequency

$$C_{ox1} \cong C_{ox2} \cong C_{AV} / 2 \tag{3.19}$$

where C_{AV} represents the capacitance of a vertical inductor area seen from the substrate, C_A is parallel plate capacitance per unit area between the inductor layer and the substrate, A_{IND} is the area of the spiral inductor cover, A_{FRI} is the area corresponding to the additive fringing contributions (approx. 3.5 μm x total perimeter) of the spiral inductor Similarly the substrate resistance can also be expressed empirically.

All these parasitic effects can be represented by a single design parameter, the Q-factor. The Q-factor is directly proportional to parallel resistance and inversely proportional to series resistance. In a multi-layer spiral inductor structure the interconnect resistance also adds on to the series resistance. The series resistance decreases with increase in metal width and multi-layer routing [32][33] . However these concepts are not the solution to achieve optimum Q-factor in the frequency range of interest because of high frequency magnetic field effects such as the skin effect [30] . As discussed earlier the skin effect causes the resistance of a metal line of wider metal width to increase with frequency faster than a narrower metal line. Figure 3.14 shows the variation in the Q factor with metal width. Another important design requirement is to achieve maximum inductance for a given area. In this perspective rectangular spiral provide the minimum inductance. and circular spiral provides the maximum inductance for the same area. In some process technology non-Manhattan shapes are not allowed. In such situations octagonal spiral would be the optimum inductor shape.

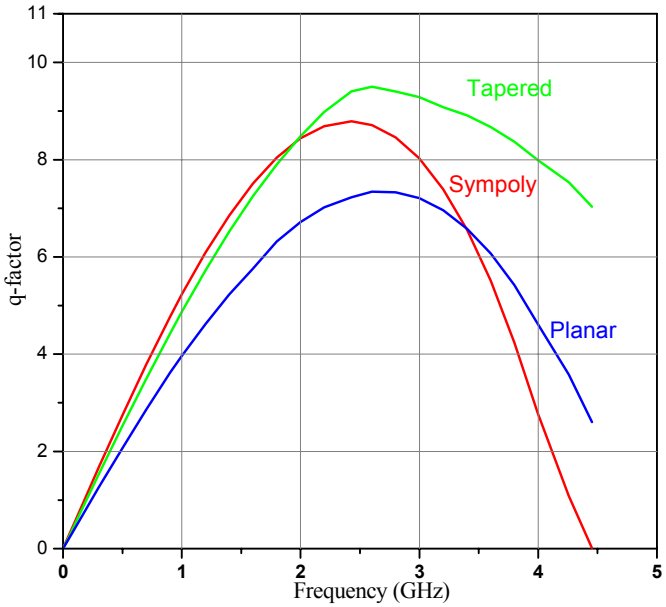


Figure 3.14: q-factor variation with frequency

3.5 *Planar inductor structures*

For the same inductance different inductor structures are possible. This section discusses some of the most widely used inductor structures.

3.5.1 Planar circular spiral

Planar spiral inductors are realized using single metal layer. Hence the planar inductor structures are the most widely used spiral inductor structures. The circular spiral is the most efficient inductor structure in terms of maximum inductance for a given area. Figure 3.15 shows a simple circular spiral structure. Inductance is determined by the physical dimensions such as inner or outer radius, the metal width, the metal layer, spacing between the spirals, and the number of turns.

Figure 3.15: Circular spiral

3.5.2 Tapered inductor

The simple planar inductor structure has very low Q-factor and hence alternate inductor structure have to be explored to realize an optimum inductor. The square tapered spiral has a constant spacing, but the metal width is tapered continuously in a linear fashion. The inner turns does not add to the overall inductance and thus the inner turns the wide metal width are used to minimize the series resistance. Figure 3.16 shows a simple tapered spiral structure. This structure gives the best Q-factor among the different the spiral inductor configurations. For differential inductor application such as LC-VCO this structure is not preferred since the electrical center is different from the geometrical center.

3.5.3 Symmetrical inductor

For differential applications such as the LC-VCO the most preferred inductor structure is the symmetrical polygon using two or more metal layers as shown in Figure 3.17. This

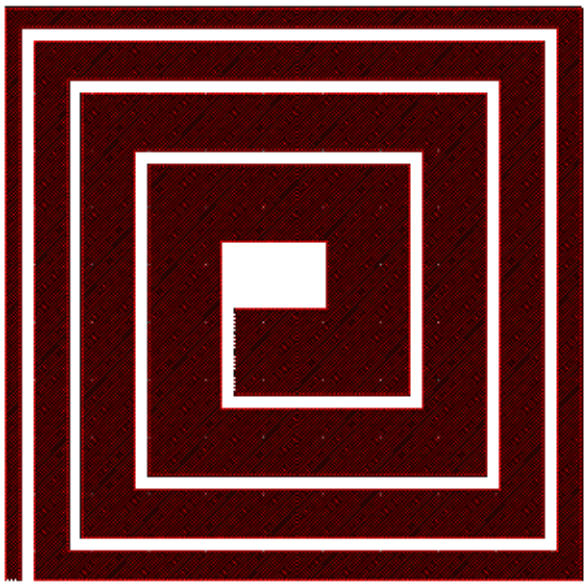


Figure 3.16: Tapered spiral

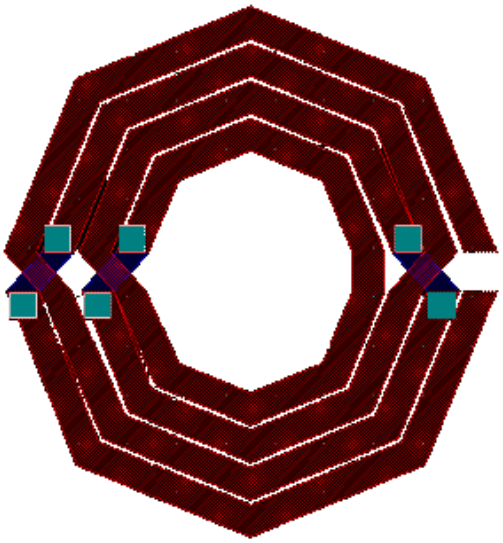


Figure 3.17: Poly-symmetrical spiral

structure provides Q-factor slightly less than the tapered inductor for identical physical dimensions. The spiral has both ports on the outer fringe and the spiral impedance is also symmetrical. The center of the spiral represents the true center tap for the inductance and the resistance. The space for transition should be greater than the sum of the metal width and spacing.

3.5.4 Transformer

On chip transformers can be realized very similar to inductors. In order to obtain high coupling factor, k, the two inductors are interwound as shown in Figure 3.18. The turns ration n is given by Eq (3.20)

$$n = k\sqrt{\frac{L_2}{L_1}} \tag{3.20}$$

In order to realize n ≠ 1 number of turns and metal pitch in the secondary are altered.

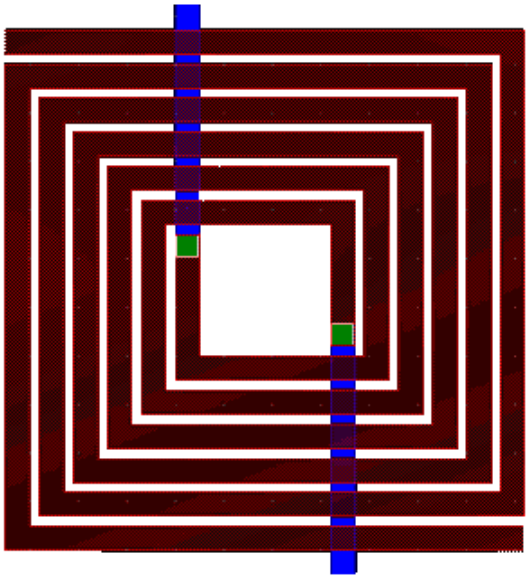


Figure 3.18 : Square spiral transformer

3.6 Design guide to on-chip CMOS inductors

This section addresses the major issues involved in the design of an optimum on-chip inductor in terms of different performance parameters

3.6.1 Process

High performance inductors depends to a great extent on the technology employed. The metal layers chosen should have very high conductivity thus reducing the parasitic series resistance. The performance of the inductor improves with the number of metal layers. The inductor should be realized in a metal layer which is at a maximum distance from the substrate. High substrate resistivity reduces the substrate coupling loss.

3.6.2 Q-factor

For most applications, it is advantageous that the inductor has a peak Q-factor at the frequency of operation. But for an LC-oscillator the peak Q frequency is usually chosen to be much smaller than the desired frequency of operation as the parasitic capacitance at the oscillator nodes and other parasitic effects of the varactor will further reduce the frequency of operation. Based on the discussion about the distribution of magnetic field it can be concluded that the inner metal turns do not substantially contribute to the total inductance and adds to the overall parasitic series resistance. Hence, to achieve minimum series resistance inductor structures with wide inner turns are designed.

3.6.3 Layer topology

In any multi-metal layer process metal 1 should never be used as it is too close to the substrate as this metal layer has the maximum substrate coupling effect. For example in a 3 metal process usually metal 3 is used for the spiral inductor. If metal 2 has a higher

conductivity than metal 3, then if the relative improvement in conductivity is more than the increase in capacitive effect then metal 2 would be preferred over metal 3.

3.6.4 Inductor area

The optimum inductor shape in terms of area is the circular spiral. But some of the technology process allow only non-Manhattan shapes. In such cases an octagonal shape that takes 2.7 % more area than a circular spiral is the best choice. A square spiral occupies 12.8 % larger area than a circular spiral. Inductor turns close to the center produce opposing magnetic field and tends to degrade the overall Q-factor. Hence high performance inductors are usually designed with wide inner radius. Also to reduce the series resistance wide metal wires are used.

3.7 ASITIC

ASITIC (Analysis and Simulation of Inductor and Transformers for Integrated Circuits) is a user-friendly tool designed to aid the RF circuit designer in designing, optimizing, layout of spiral inductor. ASITIC is the amalgamation of the key concepts and techniques described by Ali Niknejad[23]. ASITIC allows one to move easily between the electrical, physical, geometrical, and network domains as shown in Figure 3.19 [23]. In the electric domain, the device is described by the relevant electrical parameters, such as the inductance, the capacitance, the quality factor Q, the self-resonant frequency etc. In the physical domain, the device is described by the constituent material properties, such as the thickness, conductivity of the metal layer, its permittivity, and the permeability.

In the geometric domain, the physical dimensions and relative position in the volume of the integrated circuit describe the device. In the network domain, the device is described by the two port network parameters.

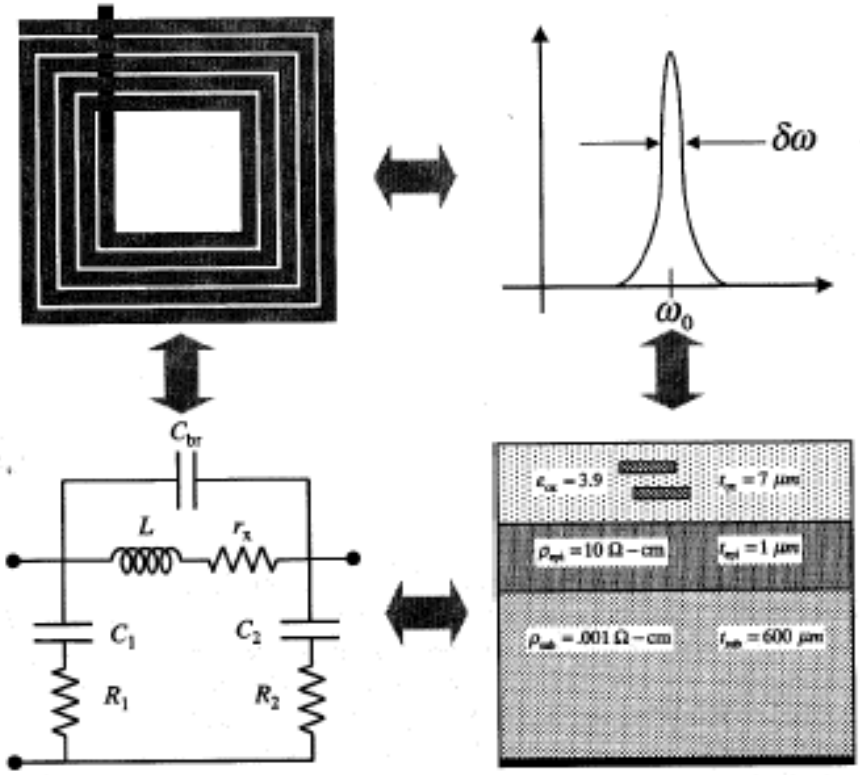


Figure 3.19 : Different domains in ASITIC

The ability to move easily from one domain to the other is an important advantage of ASITIC. This allows circuit designers and process engineers to optimize the device structure and maximize the quality of passive devices. Other highly sophisticated numerical tools such as Em solvers are comparatively slower than ASITIC by at least one or two orders of magnitude slower since they employ complex mathematical operation.

ASITIC has also been designed to be a fairly flexible tool. As mentioned before, the modern IC process allows highly complicated geometrical structures to be designed over the Si substrate. The MEMS revolution is continuously expanding the possibilities as more and more complex electromechanical structures are fabricated on Si. Thus one of the major goals of ASITIC from the outset is to allow the analysis of an arbitrary interconnection of metal structures over the Si substrates.

In summary, the goal of ASITIC has been to create an easy to use numerical software package for the analysis and design of passive devices over the Si substrate. The key criteria for the design of spiral inductors have been accuracy, flexibility, and efficiency.

Since 1995, ASITIC has been a freely available software package widely used in the IC and EM community. To date over 1500 universities, organizations and commercial entities have used ASITIC to solve practical and experimental problems. This has resulted in great interaction between the users and creators of ASITIC, which has fueled continuous evolution of ASITIC.

3.7.1 ASITIC organization

Figure 3.20 [23] illustrates the block diagram of ASITIC modules. ASITIC is composed of several software modules that interact over clearly defined interfaces. The user interacts with ASITIC at the top level through the graphical and text interfaces The technology file describes the pertinent process parameters such as the substrate layer thickness, the conductivity, and the permittivity data, as well as the metal thickness. By

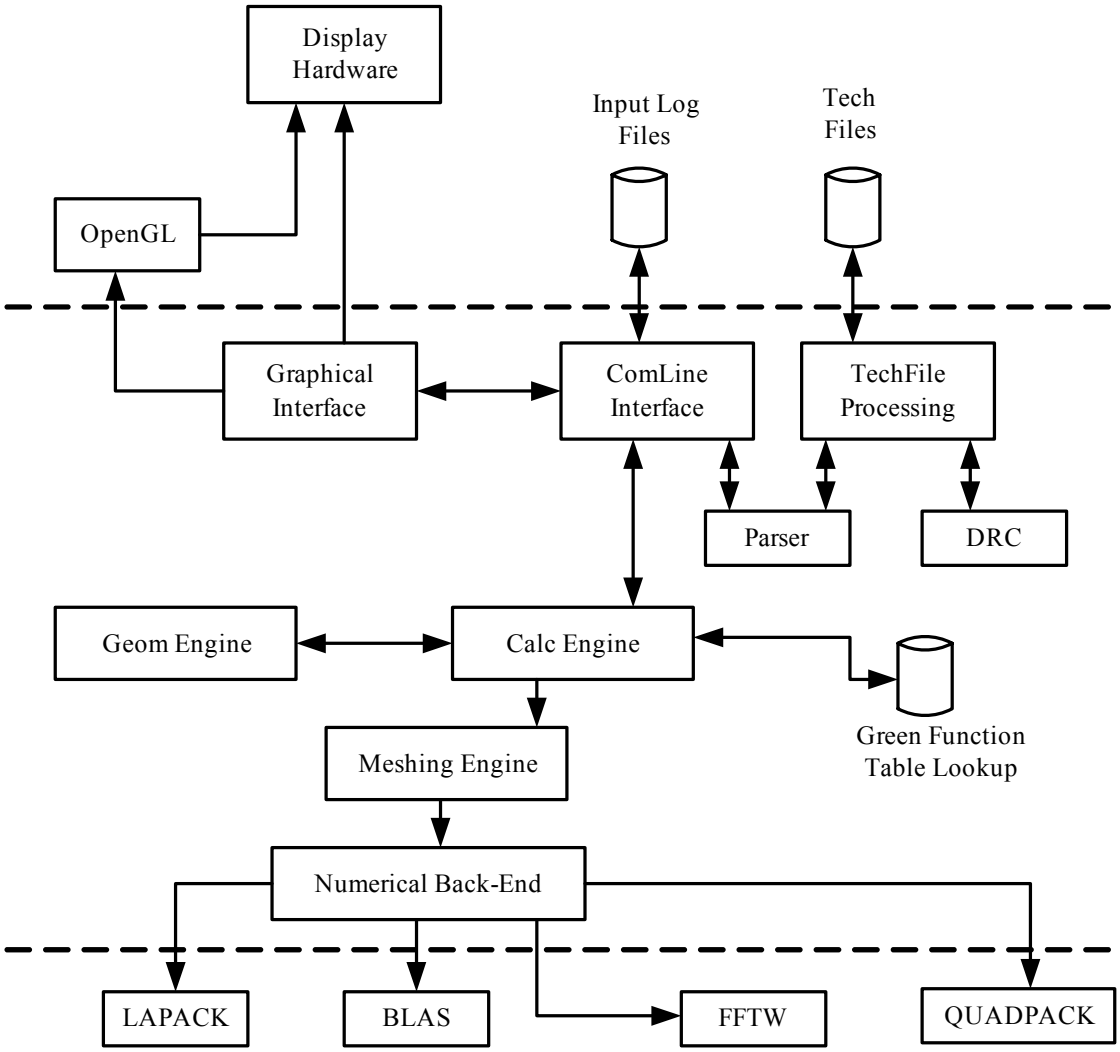


Figure 3.20 : Block diagram of the ASITIC modules

means of ASITIC commands, users are able to create, modify, optimize, and analyze passive devices.

The top ASITIC layers rely on the geometry and calculation engines to create and analyze structures. The geometry engine is able to synthesize structures such as square, circular structures. The calculation engine in turn depends on the meshing engine to convert geometric representation of devices into electrically small geometric sub-element used for the analysis. The numerical back-end modules convert the electrical sub-elements into algebraic equations through numerical integration. Several software libraries such as Basic Linear Algebra Subroutines (BLAS), Linear Algebra Package (LAPACK), an extension of LINPACK, Fastest FFT in the west (FFTW), and the numerical integration package QUADPACK accelerate the numerical computations.

Another important element in ASITIC has been the graphical interface. ASITIC is capable of displaying devices in two and three dimensions. The three-dimensional representations produced with openGL are highly useful in understanding and verifying complex multi-metal structures. Physical dimensions can be distorted to more easily visualizable structure. For instance, the z-direction can be scaled to clearly delineate closely spaced metal layers. ASITIC can also display the current and charge density in a spiral. This is an especially important visualization capability as it allows the device designer to understand the current flow and distribution, and hence the losses in the device.

3.8 Varactor realization

Another very important element in an LC VCO is the varactor. The power consumption of the VCO is proportional to the total capacitance of the tank and inversely proportional to the effective Q-factor of the tank. If Q_L represents the Q-factor of the spiral inductor, Q_V represents the Q-factor of the varactor and parasitic capacitance, then the overall quality factor of the tank Q_T is given by Eq (3.21) [34]

$$Q_T = \frac{Q_L * Q_V}{Q_L + Q_V} = \frac{Q_L}{1 + \frac{Q_V}{Q_L}} \tag{3.21}$$

Usually Q_L varies from 6-10 depending on the process and the type of inductor structure. Hence in order to obtain optimum Q_T one of the design challenges in a LC VCO is achieving high Q-factor varactors in standard CMOS process. Another important design parameter is the high tuning range represented by the maximum to minimum capacitance ratio, $\xi = C_{V,\max} / C_{V,\min}$. The control voltage must be compatible with the supply voltage and also provide linear capacitive variation. Hence one of the objectives of this research work was to evaluate the different types of varactors in CMOS process in terms of tuning range, Q-factor, optimum sizing, layout etc.

Two classes of device have been identified in CMOS process as varactors namely, junction diodes and MOS capacitors. In each case the device should be placed in separate wells in order to utilize the well potential as the control voltage. Hence there are losses associated with the lightly doped well.

3.8.1 Varicap diodes

Reverse biased diodes have been traditionally employed to realize a variable capacitor. In an n-well process, diodes are implemented as p+/n-well. In differential VCO design these diodes can be implemented in separate n-wells or for better symmetry a novel differential structure in a common n-well can also be utilized. An simple electrical model for a reverse biased diode consists of a variable capacitor, C_V which can be expressed in terms of control voltage V_{cntl} by Eq 3.22 [35]

$$C_V = \frac{CJ * A_{eq}}{\left(1 - \frac{V_{cntl}}{PB}\right)^{MJ}} + \frac{CJSW * P_{eq}}{\left(1 - \frac{V_{cntl}}{PBSW}\right)^{MJSW}} \tag{3.22}$$

where A_{eq} , P_{eq} are the diode area and perimeter respectively. The series equivalent resistance r_D is given by Eq (3.23)[35]

$$r_D = \frac{N * U_T}{JS * A_{eq} + JSW * P_{eq}} e^{\frac{V_{cntl}}{N * U_T}} \tag{3.23}$$

In standard CMOS process the conductive substrate provides another parasitic resistance R_{sub} through the lateral path from the junction to the small signal ground. The well substrate capacitor C_W trends to degrade the Q-factor of the tank for small unbalance in the differential outputs. However this capacitance is negligible compared to C_V as the doping levels in the well and the substrate, are low and hence the depletion region is wide. In order to avoid any further loss the control voltage node should be kept as a high impedance node. C_{ext} represents the additional capacitance due to the interconnections.

3.8.2 Conventional MOS varactor

A conventional MOS varactor is formed by connecting the source, the drain and the body to the control voltage while the gate connected to the tank. Here the capacitance value depends on the voltage V_{BG} between the body and the gate. For a PMOS capacitor, an inversion channel with mobile holes builds up for $V_{BG} > |V_T|$, where $|V_T|$ is the threshold voltage of the transistor. For $V_{BG} >> |V_T|$, the transistor operates in strong inversion and for $V_{BG} << |V_T|$, the device enters accumulation region. The interface is high enough to allow electrons to move freely. Thus in both strong inversion and accumulation regions, the interface capacitance C_{mos} is equal to $\varepsilon_{ox} * S / t_{ox}$, where S and t_{ox} are the channel area and the oxide thickness, respectively. In between the extreme regions of operation there exist intermediate region of operation where there are a few or very few mobile charge carriers at the gate oxide interface. The effective capacitance can be expressed as C_{ox} in series with the parallel capacitance C_b and C_i, where C_b accounts for the hole modulation in the weak and moderate depletion region and C_i accounts for the electron modulation in the accumulation region. The region of operation is determined by whether C_b or C_i dominates, if $C_b >> C_i$ then the device is in moderate inversion and if $C_i >> C_b$ the device is in accumulation and if neither of them dominates the device is in weak inversion. Figure 3.21 shows the capacitance variation with V_{BG}.

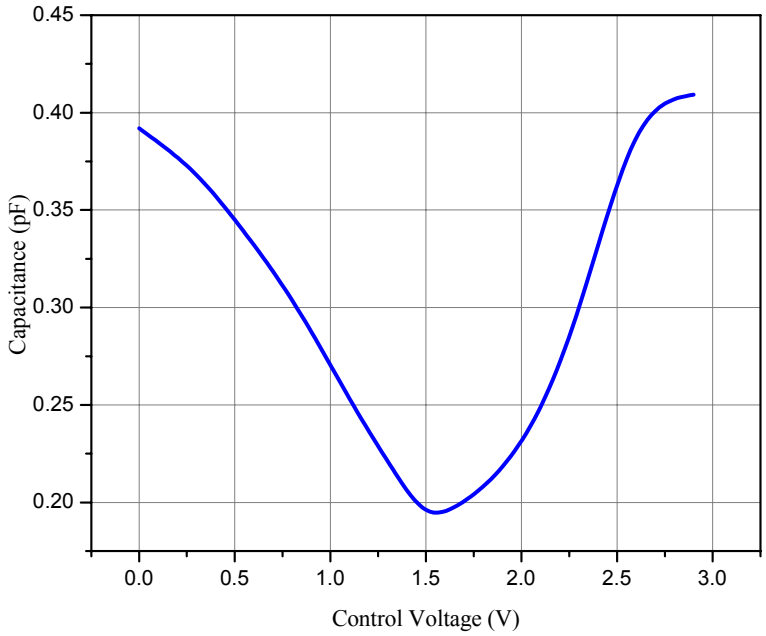


Figure 3.21 : Capacitive variation of a MOS varactor

As described earlier the varactor performance depends on C_{max}/ C_{min} ratio and the Q-factor. The quality factor depends on the channel resistance. For a PMOS device working in strong inversion the channel resistance is given by Eq. (3.24) [35]

$$R_{mos} = \frac{L}{12k_p W(V_{BG} - |V_T|)} \tag{3.24}$$

where W,L, and kp are the width, length and gain factor of the pmos transistor respectively. R_{mos} increases as V_{BG} approaches $|V_T|$ and hence theoretically becomes infinite when V_{BG} is equal to $|V_T|$. For moderate inversion the concentration of holes at the oxide interface decreases. In weak inversion, the modulation of the depletion region is as important as the hole injection and the channel resistance associated with the resistive losses of the electrons moves from the bulk contact to the interface between bulk and depletion region. Since electrons have approximately three times the mobility of holes, the parasitic resistance decreases in the depletion region compared to the strong inversion

region. The Q-factor is inversely proportional to the channel resistance. The channel resistance is directly proportional to L_{eff}^2 in the accumulation region and directly proportional to L_{eff} in the depletion region. For maximum Q-factor the length is kept at the minimum. The typical behavior of a MOS varactor in terms Q–factor variation with tuning voltage variation is shown in Figure 3.22. The Q-factor increases slightly in the accumulation region. As the device enters weak inversion region, the Q-factor drops due to decrease in the minority and the majority mobile charge carrier. The Q-factor increases as the device enters moderate depletion. The Q-factor reduces as the device enters the strong inversion region due to increase in conductivity of the channel.

The tuning characteristics of a MOS varactor shown in Figure 3.23 holds goods only for small signal voltage superimposed on the bias voltage V_{BG}. If the signal on the transistor gate is large as in a LC tank, then the instantaneous value of C_{mos} changes throughout the signal period. Although the average voltage across the varactor over a signal period is

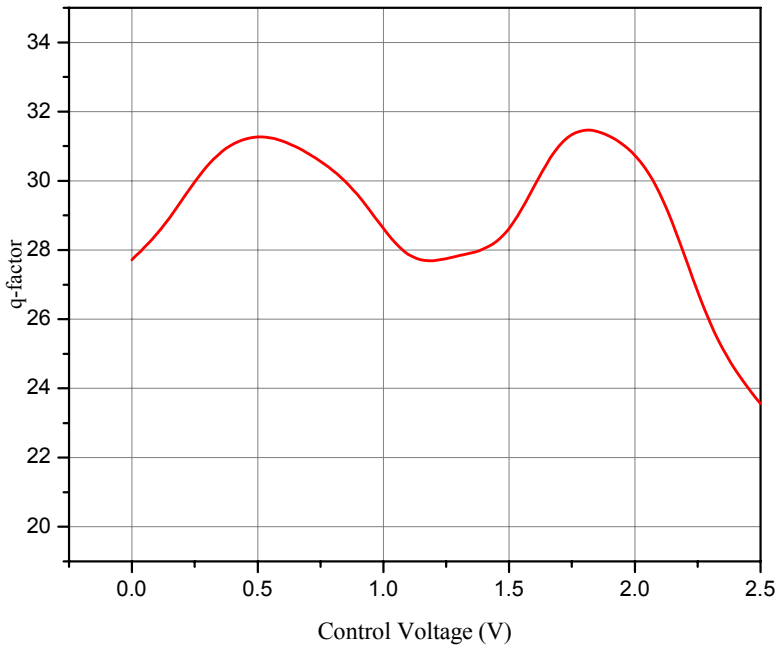


Figure 3.22 : Q-factor variation of MOS varactor

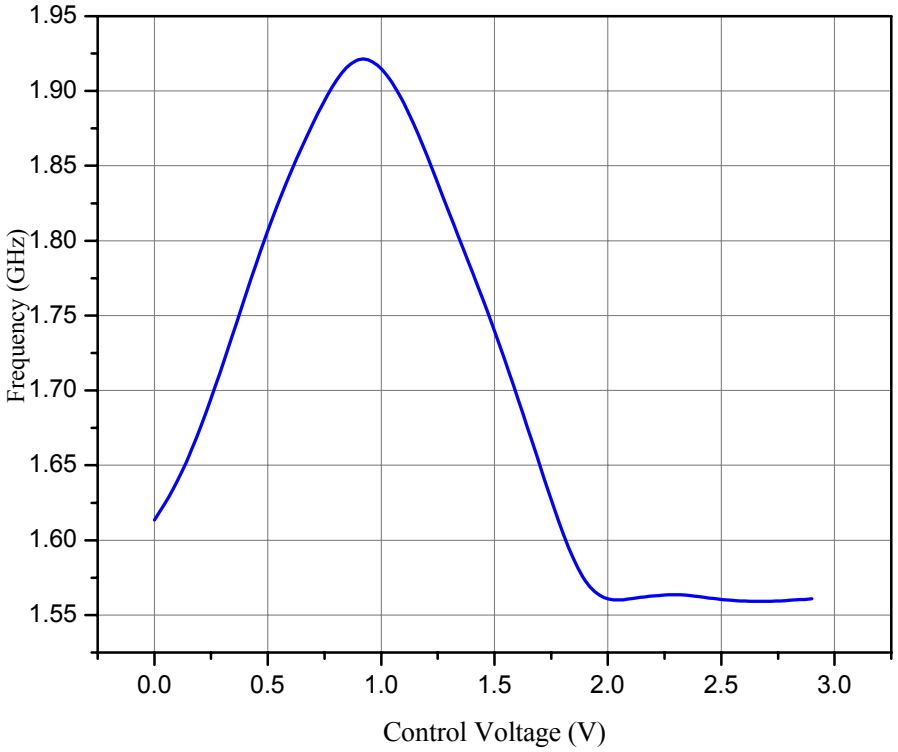


Figure 3.23 : Tuning characteristics of a MOS varactor

still constant V_{BG} but the instantaneous change in the gate voltage causes the output signal to be slightly frequency modulated and add to the total phase noise. The tunabilty of the varactor is impaired by the non-monotonicity of C_{mos}. One way to overcome these problems is to operate the MOS varactor either in depletion or accumulation over the entire tuning range. This concept has lead to the development of the body driven varactors.

3.8.3 Body driven MOS varactor

Conventional MOS varactors are not the optimum varactors for LC VCO application because of the non-monotonous variation in the capacitance within a signal cycle. Hence as described in the earlier section, another alternative is to operate the MOSFET in either depletion or accumulation region. Also the PMOS device gives a lower channel

resistance in the accumulation region thus higher Q. Thus one of the best alternatives without altering the device structure is the use of MOSFET configuration as shown in Figure 3.24. Here the source and the drain are grounded, the gate is connected to the tank node and the body is being driven by the control voltage $V_{cntl.}$ By grounding the source and drain the device is ensured to operate in accumulation throughout the entire signal cycle. This provides a large tuning range compared to the conventional varactor. Figure 3.25 shows the capacitance variation with tuning voltage for the same size MOSFET. The C_{max} / C_{min} ratio is around 3.8 for a W=2 µm, L= 3 µm and M= 48 in 0.35 µm process. The intrinsic C_{max}/ C_{min} ratio can be increased by increasing the lengths of the varactors but this will cause reduction in the Q-factor. Figure 3.26 shows the quality factor variation with control voltage for the body driven varactor. Compared to conventional MOS varactor Q-factor is higher for the same tuning range.

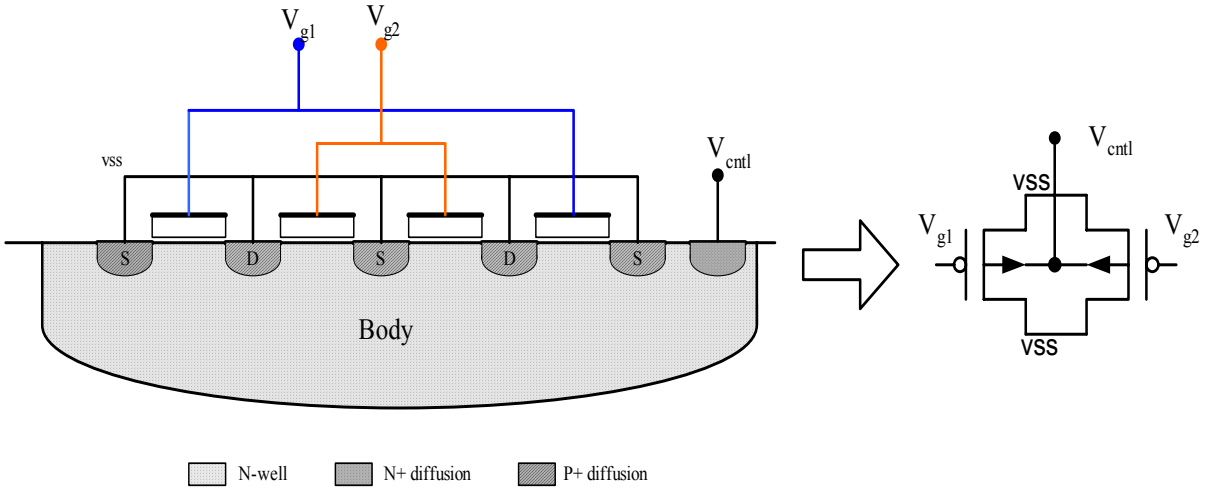


Figure 3.24 : Differential body driven varactor and its equivalent circuit

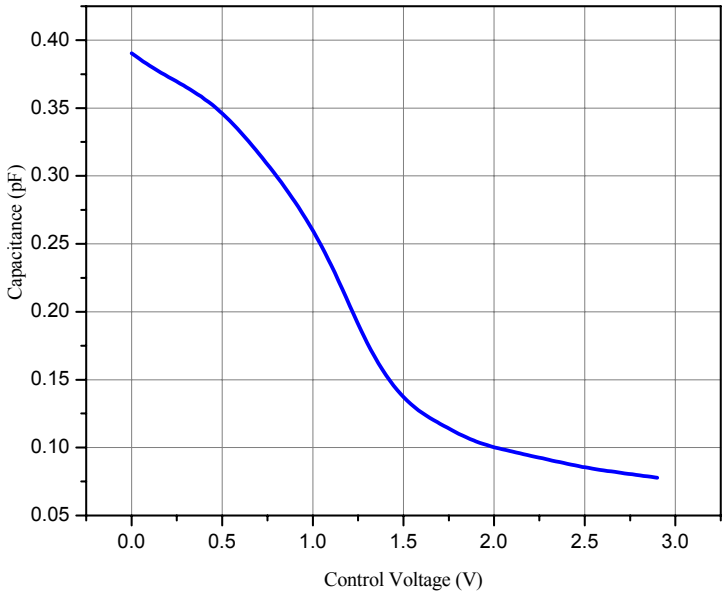


Figure 3.25: Capacitive variation with control voltage

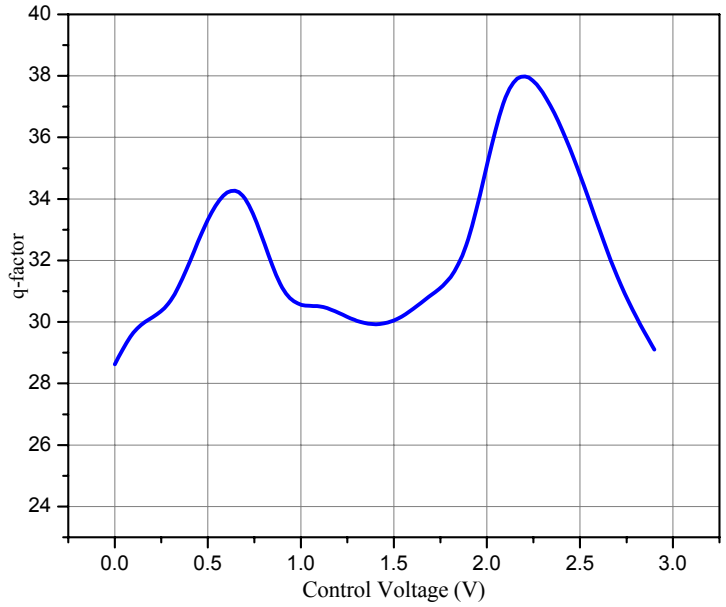


Figure 3.26 : Q-factor variation with control voltage

3.9 Body driven MOS varactor modeling

This section describes the general behavior model for body driven varactors. The main capacitor of concern is the gate to body capacitance, but there exist additional parasitic capacitance associated with the source and drain. Further, the MOS varactor as discussed in the previous is not an ideal capacitor and thus has its associated parasitic substrate and channel resistance. For a better understanding the MOS transistor can be viewed as consisting of two parts. The part between the source and the drain containing the inversion layer and the depletion region as well as the region between the oxide and the gate above them will be described as the intrinsic part. The part surrounded by the source and the drain resistance, the junction capacitance from the source, the drain and the gate to the body, the resistance of the body constitutes the extrinsic part. The effective capacitance between any terminals can thus be expressed as the parallel combination of the intrinsic and the extrinsic effects.

The parasitic extrinsic overlap capacitance between the gate and the source and the gate and the drain expressed as C_{gse} and C_{gde} respectively can be roughly estimated as

$$C_{gse} = C_{gde} = C_{ox}^{'} * LD * W \tag{3.25}$$

where $C_{ox}^{'}$ is the oxide capacitance per unit area which is inversely proportional to the oxide thickness, L_D is the overlap length and W is the width of the device. In addition to this another prominent extrinsic capacitance is the gate-body capacitance expressed as

$$C_{gbe} = C_{ox}^{'} * W_{eff} * L_{eff} \tag{3.26}$$

where $C_{ox}^{'}$ is the oxide capacitance per unit area, W_{eff} and L_{eff} are the effective width and length of the device respectively. In addition to the overlap capacitance there exist two junction capacitances C_{bse} between the body and the source and C_{bde} between the body and the drain. Each of these consists of a bottom wall part and a sidewall part. These capacitance can be expressed by Eq. (3.24) [36]

$$C_{bse} = \frac{AsC_{jo}^{'}}{\left[1 + \left(V_{SB} / \phi_1\right)\right]^{\eta_1}} + \frac{P_S C_{jo}^{*}}{\left[1 + \left(V_{SB} / \phi_2\right)\right]^{\eta_2}} \tag{3.27}$$

$$C_{bde} = \frac{A_D C_{jo}^{'}}{\left[1 + \left(V_{DB} / \phi_1\right)\right]^{\eta_1}} + \frac{P_D C_{jo}^{*}}{\left[1 + \left(V_{DB} / \phi_2\right)\right]^{\eta_2}} \tag{3.28}$$

where C_{jo}' is the bottom wall junction zero-bias capacitance per unit area, C_{jo}^{*} is the sidewall junction zero-bias capacitance per unit area, A_S and A_D represents the source and the drain bottom wall junction area, P_S and P_D represents the source and drain sidewall perimeter, ϕ_1 is the bottom wall junction built in potential, η_1 is the bottom wall junction characteristic exponent, ϕ_2 is the sidewall junction built in potential, η_2 is the sidewall junction characteristic exponent. The characteristic constants in the above equations can be calculated from the shapes and doping profiles of the junction.

Intrinsic capacitances are due to the charges inside the intrinsic part. These charges and the resulting capacitance depends on the region of operation. In the current design the body driven varactor is forced to operate in the accumulation region. In the accumulation mode the gate to body capacitance C_{gbi}, given by Eq (3.29) [37] is the only prominent capacitance for a PMOS transistor. All other capacitance can be neglected.

$$C_{gbi} = 1.785 \times 10^{-15} \sqrt{N_d^{+}} \left| \frac{\left[\exp(q\psi_s / kT) - 1\right]}{\left[\frac{-q\psi_s}{kT} + \exp(q\psi_s / kT) - 1\right]^{1/2}} \right| \tag{3.29}$$

where N_d^{+} represents the doping concentration of the n-well, ψ_s is the potential obtained from the Poisson's equation considering the contribution of electrons and holes at the Si/SiO_2 interface expressed in terms of gate voltage V_{GB} by Eq. (3.30)

$$V_{GB} = V_{FB} + 9.282 \times 10^{-17} \sqrt{N_d^{+}} \times \frac{t_{ox}}{\varepsilon_{ox}} \left[\frac{q\psi_s}{kT} + \exp(-q\psi_s / kT) - 1 \right]^{1/2} + \psi_s \tag{3.30}$$

The final simplified body driven varactor's behavioral model is shown in Figure 3.27. R_G represents the gate resistance, R_{SB} or R_{DB} represents the reverse biased diode resistance between the body and the drain which is usually very high, R_{GB} is the vertical resistance

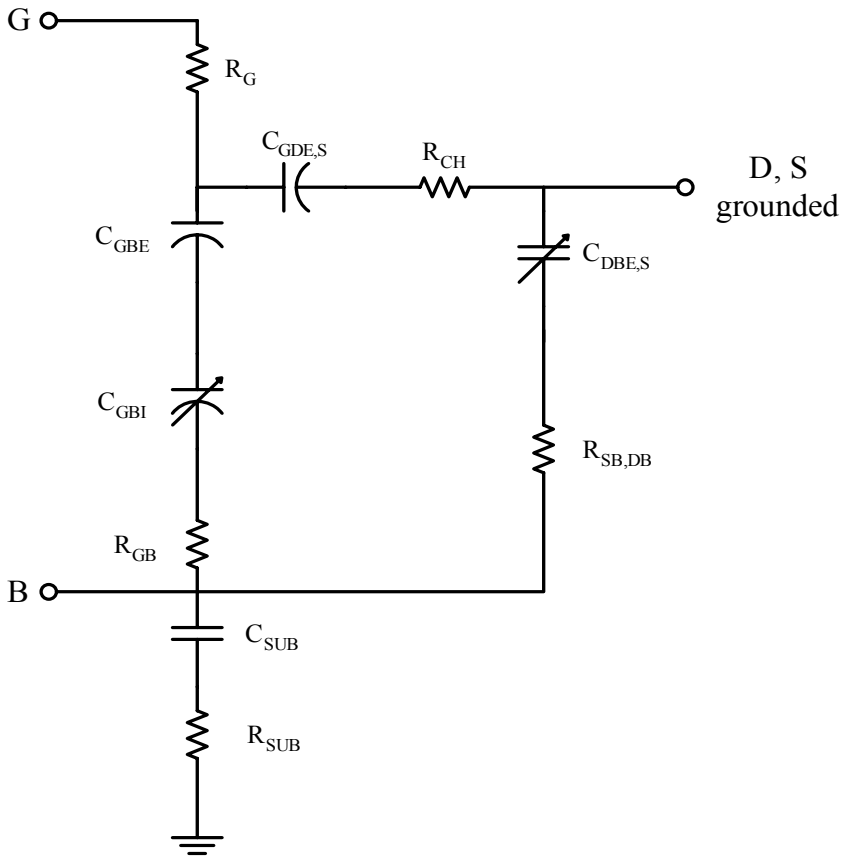


Figure 3.27 : Simplified model of the body driven varactor

of the body, C_{SUB} is the capacitance between the n-well and the substrate which is usually neglected since the depletion width of the p-n junction is very high, and R_{SUB} is the substrate resistance. The model is optimized for the accumulation mode. Table 3.2 shows the effective values of the capacitances between any two terminals including both the extrinsic and intrinsic effects.

Table 3.2 : Summary of capacitance

	Extrinsic Capacitance	Intrinsic Capacitance	Total Capacitance
C_{GB}'	$\frac{\varepsilon_{ox}}{t_{ox}} * W_{eff} * L_{eff}$	$C_{gbi} = 1.785 \times 10^{-15} \sqrt{N_d^+} \left\| \frac{[\exp(q\psi_s / kT) - 1]}{\left[\frac{-q\psi_s}{kT} + \exp(q\psi_s / kT) - 1\right]^{1/2}} \right| * W_e$	$\frac{1}{\frac{1}{C_{GBE}} + \frac{1}{C_{GBI}}}$
C_{GD}', C_{GS}'	$C_{ox}' * LD * W$	Negligible in accumulation region	C_{GDE}, C_{GSI}
C_{BS}', C_{BD}'	$C_{bse} = \frac{AsC_{jo}'}{\left[1 + (V_{SB} / \phi_1)\right]\eta_1} + \frac{P_S C_{jo}^*}{\left[1 + (V_{SB} / \phi_2)\right]\eta_2}$	Negligible in accumulation region	C_{BSE}, C_{BDE}

4 1.8 GHz LC VCO Design and Results

The aim of this research was to successfully implement a completely integrated 1.8 GHz LC-VCO compatible with GSM, DCS1800 standards. Chapter 2 gives a brief description on the different means of implementing integrated inductor and varactors. In this chapter a complete design approach to the design of LC-VCO is presented. Various precautions to be considered during layout are clearly explained. The simulation results of the 1.8 GHz LC-VCO are also provided. Finally a better means of analyzing jitter based on the non-ideality of the individual tank elements has been developed.

4.1 Design

In order to facilitate the complete description of the design , the system was divided into three conceptual blocks as shown in Figure 4.1.

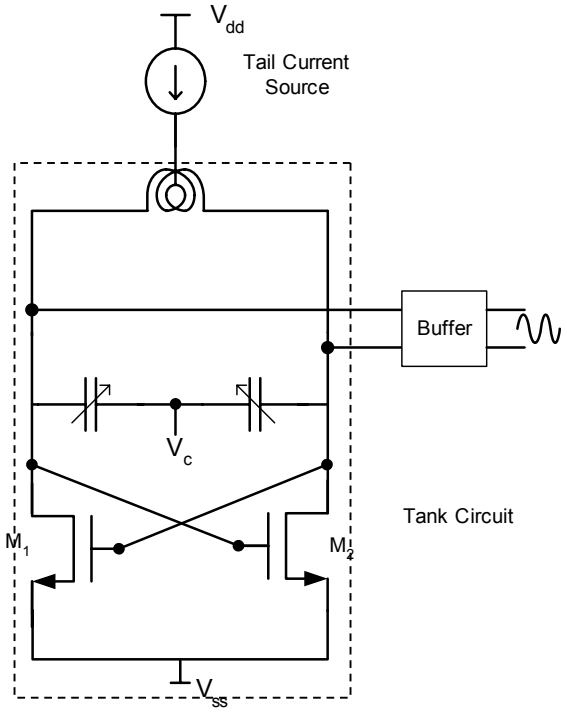


Figure 4.1: Conceptual block diagram

4.1.1 Tail current source

In this design a PMOS sourcing tail current source was used due to its low flicker noise contribution [38] . The schematic of the wide swing cascode current mirror is shown in Figure 4.2.

The reference current source was a 500μA sourcing current. NMOS devices M_{N2}-M_{N7} form the first pair of the wide swing cascode current mirrors. The diode connected transistor M_{N1} provides the gate bias for the cascode transistors M_{N2}, M_{N4}, M_{N6}. Ideally M_{N1} would be sized ¼ W/L of other cascode devices. The gate of M_{N2}, M_{N4}, M_{N6} is at $2\Delta V+V_{THN}$, and thus the source of M_{N3}, M_{N5}, M_{N7} would be at ΔV, ignoring body effect. The total minimum voltage across the NMOS cascode device is $2\Delta V$. The same analysis hold good for the PMOS device as well. In practical design usually the size of M_{N1}, M_{P1}, M_{P2} is made 1/5 W/L of other devices for proper biasing. The tail current is mirrored of from M_{P4} by M_{P5} and is sized to supply 6 mA of current.

4.1.2 Tank design

The next conceptual block is the tank circuit. This is the most critical block of the VCO. The reference current source provides 6 mA of current through the PMOS current source M_{P5}. The frequency range of interest is 1.6 GHz- 2.0 GHz. Since the on-chip inductor is the critical component of the tank circuit, the design approach was initially targeted towards finding an optimum inductor structure with high Q-factor in the desired frequency range. Different inductor structures were analyzed for this. From a differential structure perspective view a symmetrical octagonal spiral was found to be the optimum structure. Although the overall Q-factor is less than the tapered spiral of similar physical dimensions, its symmetric structure provides a number of advantages. One of the major constraints in implementing fully differential LC VCO configuration is to obtain completely symmetric inductors which match one another. Even if the two differential inductors have similar physical dimensions and similar structures, they will not provide perfect matching because of process variations across the chip. Perfectly matched

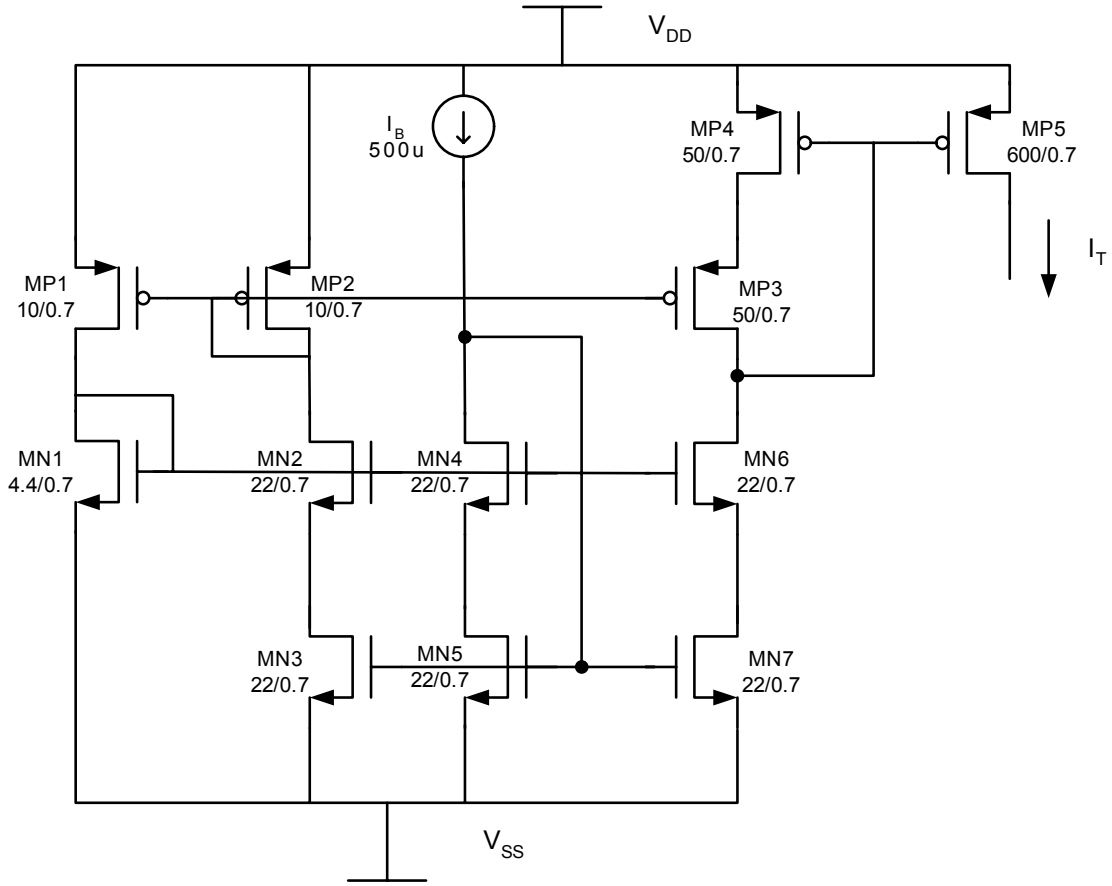


Figure 4.2: Current source schematic

inductor structures are a prime requirement for any differential structure. The structure described above provides the best possible symmetrical structure available with on-chip inductors. The parasitic effects at the common end of the differential inductors cancel one another or at least provide a balancing effect and hence better performance. The two differential inductors are wound in such a way that the mutual inductance adds constructively to the differential inductance. Thus this structure provides extra inductance without consuming any extra metal area. For the current design a 5.1nH octagonal symmetrical polygon with the outer radius 200 μm , metal width 16 μm, number of turns 4 using metal 4 as the top layer and metal 3 as the interconnect layer was employed.

The major disadvantage of a LC-VCO implementation using on-chip inductors is that the Q of the tank is dominated by the Q-factor of the on-chip inductor since it is less than the varactor Q-factor by atleast a factor of 10. Thus the Q-factor of the tank can be approximated to the Q-factor of the inductor. The cross coupled pair provides the required negative resistance to compensate for the loss in the tank circuit. The small signal transconductance of the cross-coupled pair can be estimated from Eq (2.18).

For simulation purpose the differential inductors were represented by its pi-equivalent circuit. The complete schematic of the tank circuit is shown in Figure 4.3. The next important tank component is the body driven varactor. The desired tuning range for GSM applications including component tolerance is around 1.6 GHz- 2.0 GHz. Initial simulations were run without any varactors to estimate the parasitic capacitance of at the oscillating node due to the cross-coupled pairs and the inductor parasitics. If C_p represents the parasitic capacitance at the oscillating node and C_{max} is the required capacitance for the minimum frequency limit, maximum capacitance needed from the body driven varactors (C_{VMAX}) can be calculated from the difference of the two capacitances.

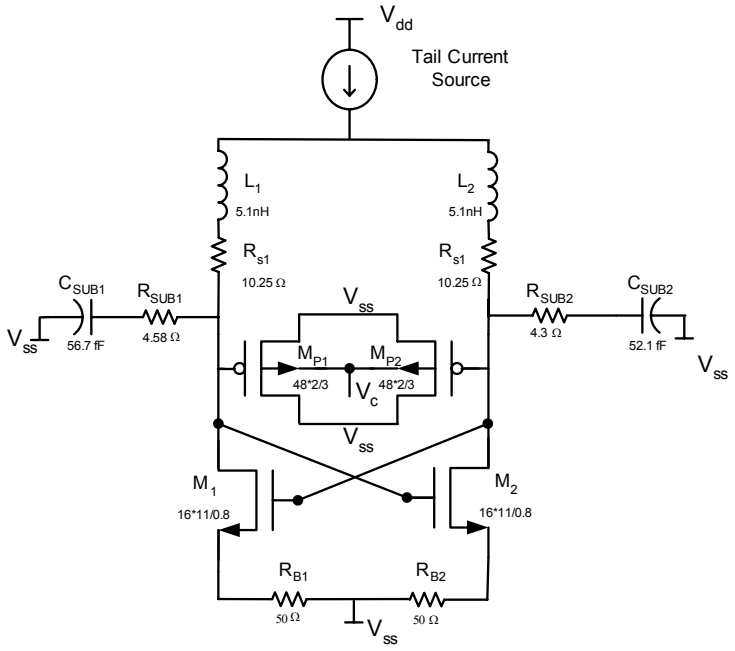


Figure 4.3: Tank circuit schematic

C_{VMAX} will be mainly be dominated by the gate to body oxide capacitance. From this W and L of the body driven varactors can be calculated using Eq 4. 1

$$W * L = C_{VMAX} * \frac{t_{ox}}{\varepsilon_{ox}} \tag{4.1}$$

The smaller width and length of the MOS varactors results in high Q but lower C_{vmax}/C_{vmin} ratio. Thus a compromise between the two is a design constraint. The differential on-chip inductors used in this design provides a Q-factor 8 @ 1.8 GHz. Thus the minimum desired Q of the varactor should be around 32 for the q-factor of the inductor to dominate. For the desired tuning range of 1.6 GHz- 2.0 GHz, the C_{max}/C_{min} ratio comes close to 1.12. Hence the optimum value of MOS varactors was found to be 48*2/3.

4.1.3 Buffer design

To isolate the tank core circuit from loading effect of the external load a simple differential buffer shown in Figure 4.4 was designed. The fully differential VCO tank

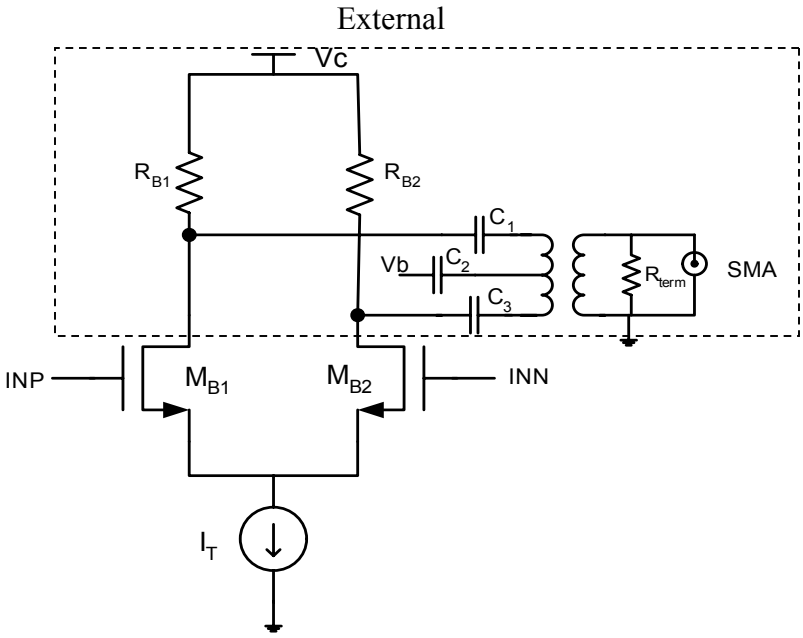


Figure 4.4: Buffer schematic

output is fed to the input of the differential pair. The buffer output is padded out as an open drain structure to drive an impedance matching network consists of coupling capacitors and transformer. R_{B1} and R_{B2} provide DC bias for the differential pair NMOS transistor. The transformer provides differential to single ended conversion. R_{term} provides proper termination for the SMA connector. The tail current I_T is also external.

4.2 Integrated circuit layout

The whole design was successfully implemented in 0.35 μm technology. Initially the inductor structure generated by ASITIC was saved in CIF format for importing into Cadence environment as described in Appendix B. As shown in Figure 4.5, the imported inductor layout is usually improperly placed and hence the layout has to be manually modified to the desired symmetrical structure. The final modified inductor structure is shown in Figure 4.6. In order to avoid LVS errors a metal res id was added for proper extraction of inductors.

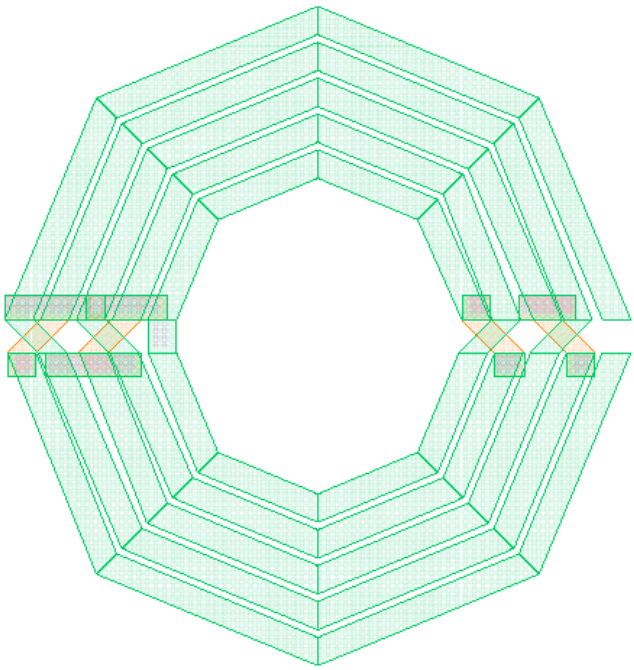


Figure 4.5: Layout imported from ASITIC

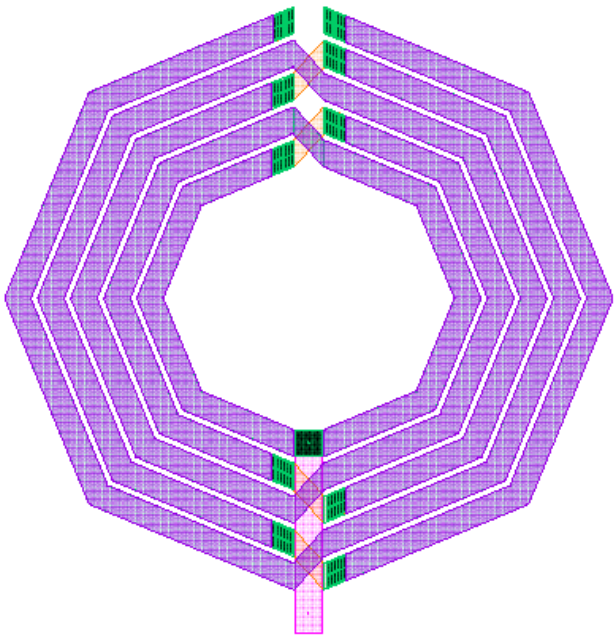


Figure 4.6 : Modified symmetrical inductor layout

Any extra parasitic resistance can dampen the oscillation of the tank. Hence a lot of care was taken during layout to reduce the parasitics wherever possible. The parasitic series resistances of the metal wires at the oscillation nodes were added to the overall series resistance of the on-chip inductors for simulation. The source and the drain areas of the cross-coupled pair and the tail current transistors were made wide enough to conduct mA of current. The varactors are placed at the center and the cross coupled NMOS transistors are placed in a common centroid fashion on either side of the varactors. A separate simpler padframe as shown in Figure 4.7 was designed and the final complete layout with the padframe is shown in Figure 4.8.

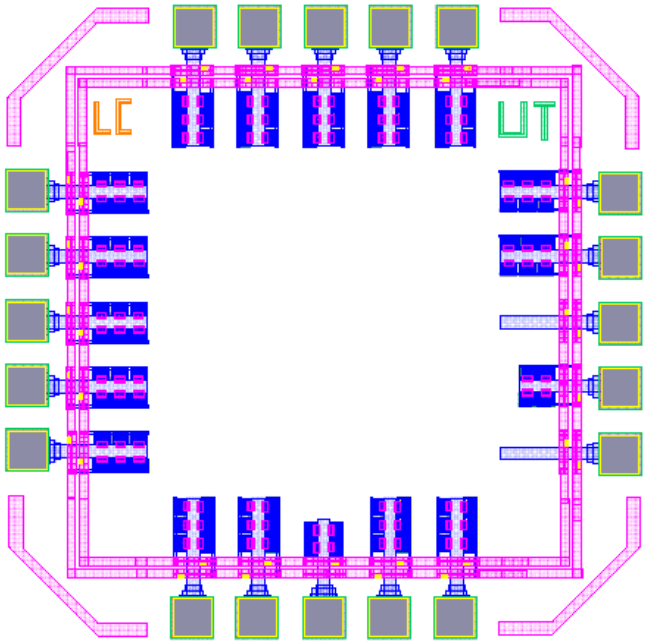


Figure 4.7: Padframe layout

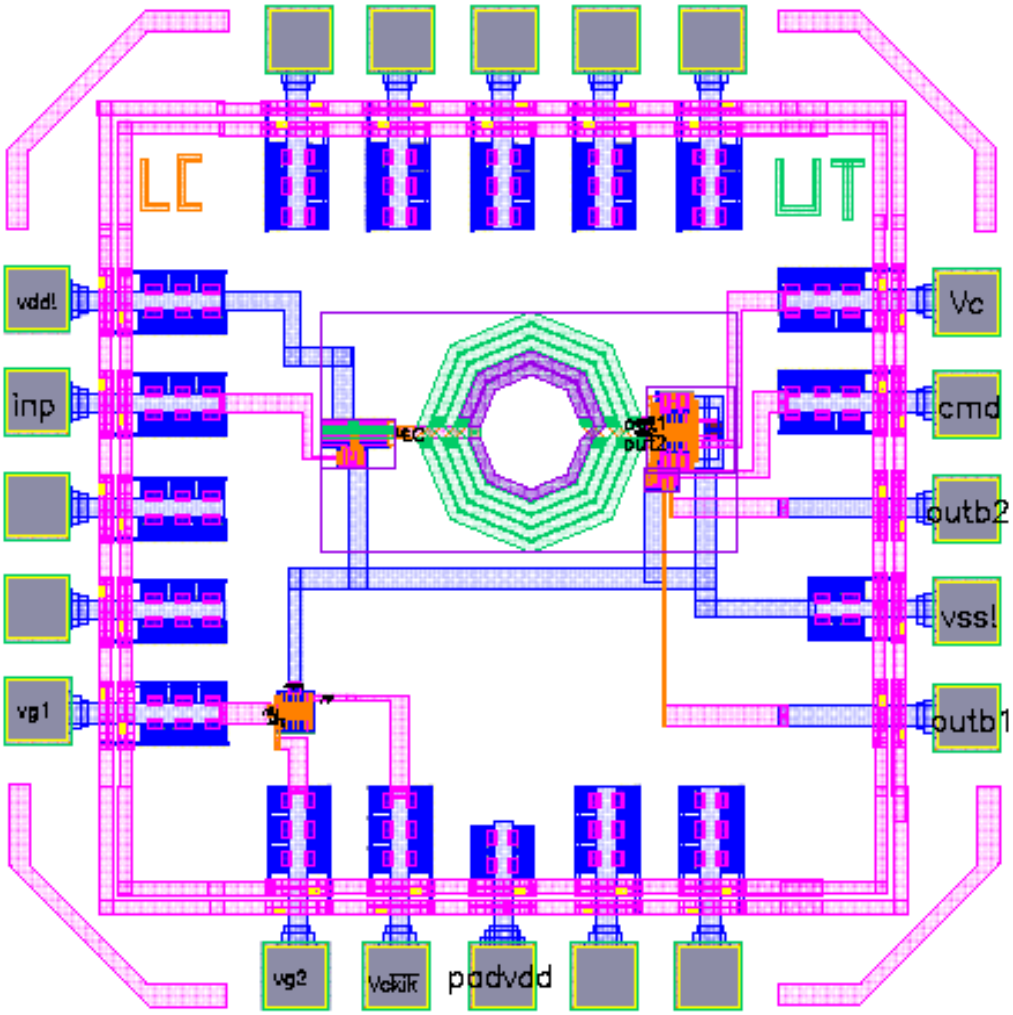


Figure 4.8: Complete layout

4.3 Simulation results

It is difficult to simulate the whole performance of VCO with SPICE like simulator directly. It is complicated to simulate the non-linear frequency domain behavior using linearized AC analysis. Hence large signal transient analysis was used to estimate the oscillator start-up and the amplitude of a steady state oscillation. As shown in Figure 4.9 the large signal oscillator build-up and the amplitude limits after about 10ns. By taking the FFT of the transient response we can estimate the harmonic content of the oscillator signal. Figure 4.10 shows the tuning characteristics of the oscillator. The oscillator has a linear tuning range of more than 400 MHz. Table 4.1 summarizes the AC and DC specifications of the LC VCO.

Table 4.1: Design summary

Parameter	**Simulated Result**
Power Supply	3.3V
Technology	0.35 μm CMOS process
Power Consumption	25 mW
Tuning Range	446 MHz
Center Frequency	1.8 GHz
Phase Noise @ 1kHz	-46.23 dBc/ Hz
Phase Noise @ 1MHz	-115.85 dBc/Hz
Output swing	1.5-1.94 V
K_{VCO}	410 MHz/ V
Tuning Voltage Range	1.5 V

Figure 4.9: Large signal transient response

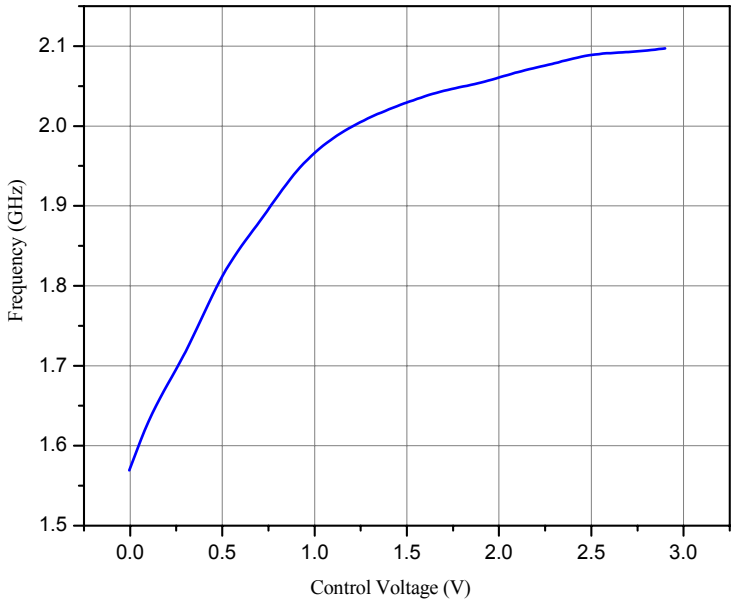


Figure 4.10 : Tuning characteristics of LC-VCO

4.4 Phase noise

In the previous chapters a lot of discussion on the design and different performance parameters of the LC-VCO has been discussed elaborately. In RF systems the LC-VCO are mostly a part of the frequency synthesizer. The frequency synthesizer provides functionality for frequency translation and filtering, synchronizing digital systems clocks for performing capturing data, reading memory. The relative stability of these signals is of particular interest when designing such systems. Frequency instability can cause inter-modulation distortion and logic timing errors in digital systems and RF. The performance parameter employed to quantify the frequency instability are system's phase noise and jitter.

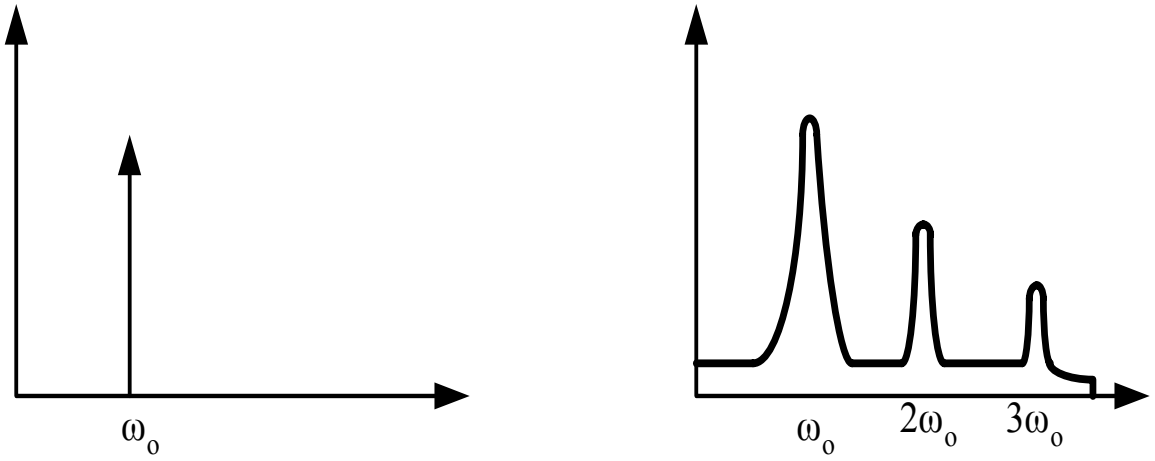
Phase noise is a frequency domain view of the noise spectrum around the oscillator frequency. The output of an ideal oscillator can be expressed as

$$V_{out}(t) = V_o \cos(\omega_o t + \phi_o) \tag{4.2}$$

where V_o represents the amplitude, ω_o the frequency and ϕ_o the phase reference. The one sided spectrum of this ideal oscillator as shown in Figure 4.11a consists of an impulse at ω_o. In practical oscillators however there exist random fluctuations in amplitude and phase and hence the output can be expressed in a general form as

$$V_{out}(t) = V_o(1 + \varepsilon(t)).\cos(\omega_o t + \phi(t)) \tag{4.3}$$

where $\phi(t)$ and $\varepsilon(t)$ represents the fluctuations in phase and amplitude respectively as a function of time. As a consequence of these fluctuations the output spectrum as shown in Figure 4.11b has sidebands close to the frequency of oscillation and its harmonics. Almost all practical oscillators inherently posses an amplitude limiting mechanism, hence amplitude fluctuations are greatly attenuated. Thus the main concern in the design of low noise oscillators is to achieve good phase noise performance.



(a) ideal oscillator (b) practical oscillator

Figure 4.11: Spectral content

In the time domain viewpoint, the spacing between the transitions is ideally a constant for an ideal oscillator. In practical oscillators the transition spacing will vary with time measured as timing jitter. In synchronous digital systems the clock signal controls the operation of several logic blocks. If the clock signal has non-zero timing jitter as shown in Figure 4.12 the data signal needs additional time to stabilize. This decreases the timing margins and hence reduces the maximum achievable frequency of operations for digital systems.

4.4.1 Phase noise behavior of LC-VCO

Phase noise appears in oscillators due to nonlinear and periodic variation in the circuit parameters. Here the effect is quite different from a normal amplifier due to the positive feedback network.

Noise can be injected either in the signal path as shown in Fig 4.11. The frequency response at frequencies close to the resonant frequency ω_o [41] can be approximated as

$$\frac{Y}{X}(\omega o + \Delta\omega) \approx \frac{-1}{\Delta\omega \dfrac{dH}{d\omega}} \tag{4.4}$$

H(ω) represents the forward transfer function, can be represented in polar form with a magnitude of |H| and a phase exp(jϕ)term.

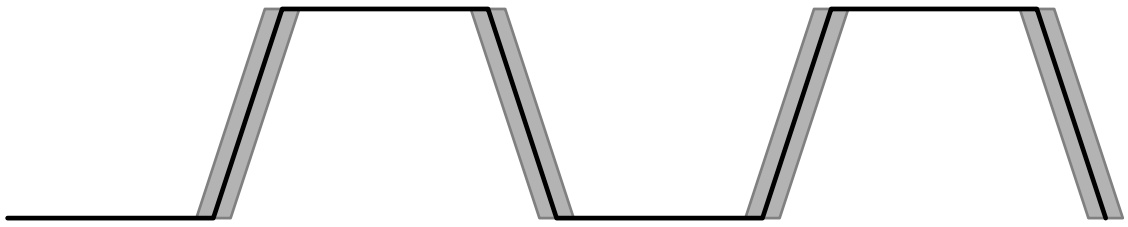


Figure 4.12 : Practical carrier signal in time domain

$$\left|\frac{dH}{d\omega}\right|^2 = \left|\frac{d|H|}{d\omega}\right|^2 + \left|\frac{d\phi}{d\omega}\right|^2 |H|^2 \tag{4.5}$$

For a LC-VCO the H(ω) magnitude does not vary a lot with frequency for small offsets from the resonant frequency and hence the magnitude term in Eq (4.5) can be ignored. Also |H| is close to unity for steady state oscillations. Eq (4.5) can now be rewritten as

$$\left|\frac{Y}{X}(j\omega)\right|^2 = \frac{1}{(\Delta\omega)^2\left|\frac{d\phi}{d\omega}\right|^2} \tag{4.6}$$

From the definition of the Q-factor, Eq (2.18) in Chapter 2 can be expressed in terms of Q-factor as

$$\left|\frac{Y}{X}(j\omega)\right|^2 = \frac{1}{4Q^2}\left(\frac{\omega o}{\Delta\omega}\right)^2 \tag{4.7}$$

Eq (4.7) is commonly known as "Lessons's equation [42] represents both the amplitude and phase noise effects. The noise performance of an LC oscillator depends extensively on the Q-factor of the tank, hence a lot of effort is expended on the design of high Q-factor on-chip inductors. Non-linear behavior of the oscillator system introduces noise folding and thus need additional terms in Eq (4.7) to represent the non-linear behavior.

Similar analysis can be performed for noise source injected through the control path. Any noise signal in the control voltage also affects the frequency of the oscillation and thus the phase noise as a frequency modulated signal.

The above discussion was based on the general influence of noise on the phase noise of the system. From the designer's perspective, a better means of analyzing phase noise is to study the influence of various circuit components on the total phase noise. In this current research the influence of individual components noise on the total oscillator phase noise has been analyzed elaborately.

A variation in the tail current source I_T introduces noise in the signal path as well as in the control path. The output common mode level (V_{CM}) of the cross-coupled pair can be approximated as

$$V_{CM} = V_{THN} + \frac{I_T}{gm_c} \tag{4.8}$$

To examine the variation of tail current source on the phase noise assume a small sinusoidal current source $\Delta I_T \cos(\omega_m t)$ superimposed on the tail current IT produces an additional variation ΔV_{BG} across the varactor and hence the output frequency varies from its ideal value. Eq (4.9) [40] quantifies the frequency fluctuation induced by the tail current variation

$$\left(\frac{\partial \omega_o}{\partial I_T}\right) = \left(\frac{\partial \omega_o}{\partial V_{BG}}\right)\left(\frac{\partial V_{BG}}{\partial I_T}\right) \tag{4.9}$$

The first term in Eq (4.9) is the VCO gain KVCO and the second term can be approximated from Eq (4.8) as $1/(2gm_{nmos})$. Hence high transconductance of the cross-coupled pair gives better phase noise performance. The effect of varactor voltage fluctuation on phase noise is similar to the frequency modulation effect produced by the tail current source. Variation in the tail current source also affects the amplitude of the output, thus indirectly induces a frequency fluctuations adding to the total phase noise. Sensitivity of frequency fluctuation with amplitude variation K_{Ao} is more complex due to the non-linear behavior of the tank and also sensitivity changes its sign. Usually the relation is derived numerically for given values of varactor bias voltage and amplitude.

Another source of upconverted phase noise is the power supply noise. In this design PMOS transistors have been employed as tail current source due to their low flicker noise contribution compared to NMOS transistors. A cascode tail current can provide a better power supply noise rejection; however this reduces the effective swing of the tank and hence is not an effective solution for low voltage designs. The phase noise is also affected

by power supply noise in a similar way. In order to simulate the power supply noise effect 100mV amplitude noise voltage was superimposed on the pure power supply at both near frequencies and far frequencies. The resulting jitter in the output tank voltage was measured.

The influence of the on-chip inductors and body driven varactors non-ideal behavior on phase noise depends on the Q-factor on these passive components as described in chapter 3. Table 4.2 summarizes the jitter due to each component of the tank. In each of these simulations, influence of each components non-ideal behavior on jitter was studied separately. Appendix 3 summarizes the calculation of phase noise.

Figure 4.13 shows the phase noise plot of the designed LC-VCO for mid tuning range using Spectre RF. The phase noise is expressed in dBc/Hz and is plotted for various offsets from the carrier signal. For mid tuning range the phase noise @ 1kHz offset is around -52 dBc/Hz and @ 1MHz offset is around -112 dBc/Hz.

Figure 4.14 shows the phase noise variation for 1kHz across the tuning range. The phase noise at near frequencies from the carrier first decreases, till the mid tuning range and then increases. Figure 4.15 shows the phase noise variation with tuning range at far offset from the carries. The same trend can be seen in this case.

Table 4.2 : Jitter summary

Parameter	Jitter	% percentage
Cross –coupled pair	6ps	35.2
Spiral Inductor	8ps	47
Body Driven Varactor	8ps	47
Current source no noise	4p	23.5
Current source noise 1MHz offset	6p	35.2

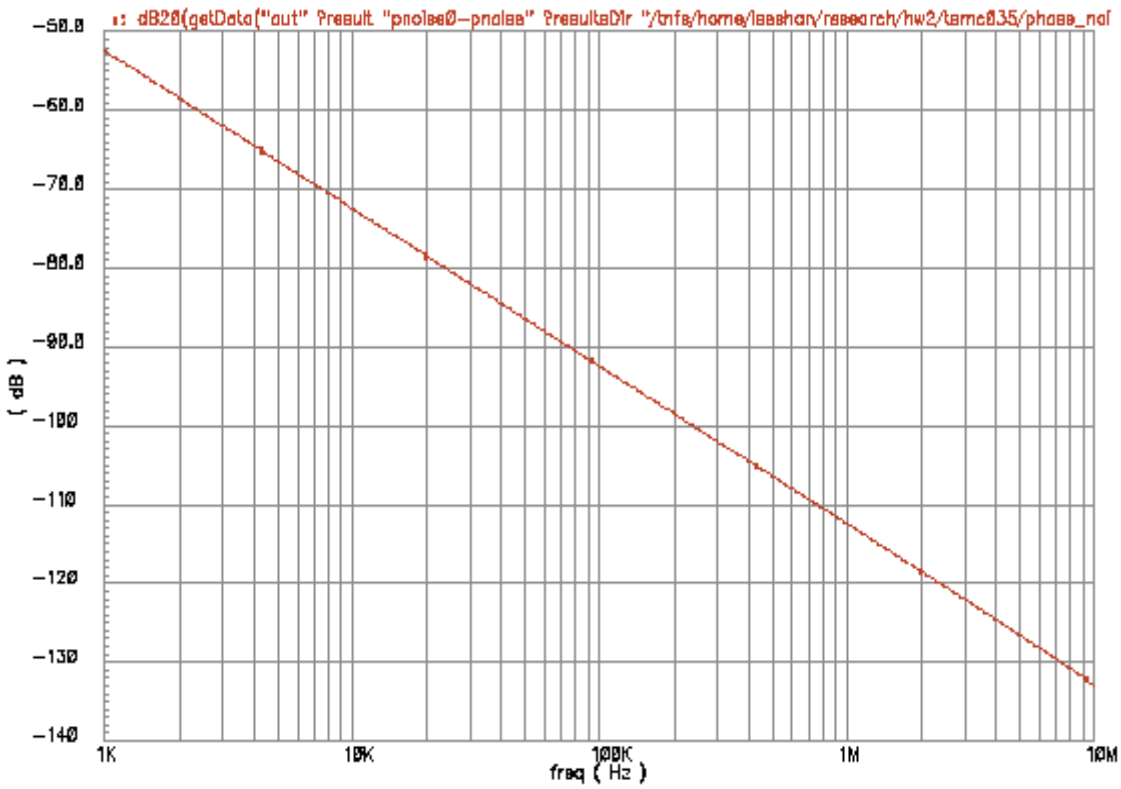


Figure 4.13 : Phase noise spectre plot

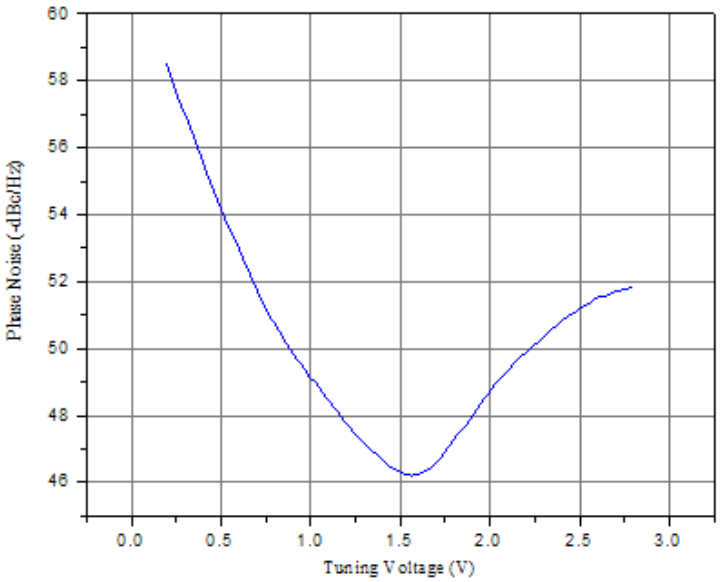


Figure 4.14: Phase noise variation @ 1 kHz offset

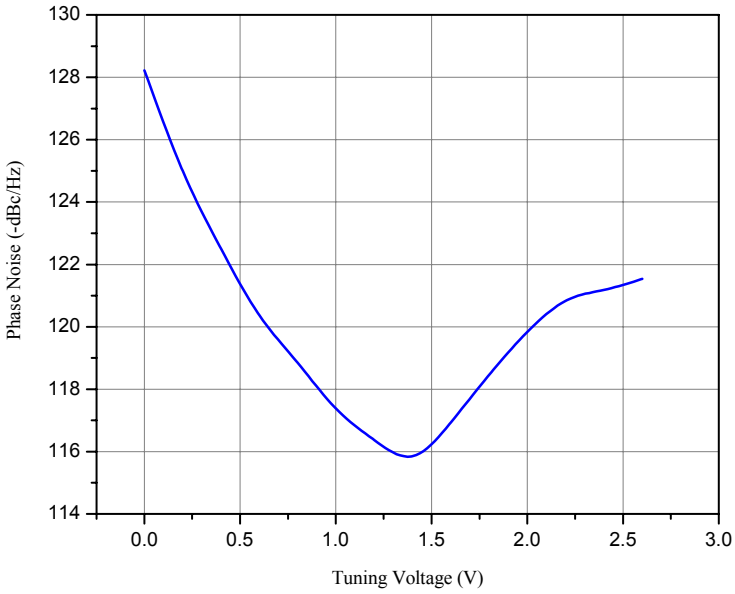


Figure 4.15: Phase noise variation @ 1 MHz offset

5 CONCLUSION AND FUTURE WORK

5.1 Conclusion

A complete integrated LC-VCO compatible with the GSM 1800, DCS receiver has been designed in standard CMOS 0.35 μm technology. The design specifications were all met with sufficient margin. The designed integrated LC-VCO has a linear tuning range from 1.595 GHz – 2.05 GHz. The designed VCO has a gain of 410 MHz/V. The worst case phase noise in dBc/Hz at 1 kHz offset across the tuning range is -46.23 dBc/Hz and @ 1 MHz offset from the carrier is -115.85 dBc/Hz. The power consumption of the block, excluding the output buffer power consumption is approximately 8.78 mW. Currently the design has been sent for fabrication and test board is being designed.

5.2 Future work

The major shortcoming of the spiral inductor is the poor Q-factor compared with inductor implementation. Hence one of the future goals is to explore different means of improving the q-factor of the most practically feasible integrated inductor implementation. The system will be redesigned in 0.18 μm standard CMOS process. The advantage of the 0.18 μm process is the availability of a thick top-metal layer, which can potentially improve the performance of the on-chip inductors.

The new varactor structure certainly provides a better performance than the conventional varactor. One of the future goals is to improve the simple equivalent circuit of the varactor by validating with the real measurement results. Also the fully symmetrical inductor structure will be also compared with the measurement results to validate the technology file.

The current research focused only on the application of on-chip inductors for VCO applications. One of the future goal is to investigate alternate applications of on-chip inductors. A more demanding application of on-chip inductors is in bio-implantable

electronics. Spiral inductor can been used as secondary of a transformer to deliver remote power to tiny bio-sensors. This technique will highly reduce the physical sizes of the bio-sensors.

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APPENDICES

APPENDIX A : Spice netlist

```
*LC only schematic netlist
.INC "/home/lseshan/smart/models/tsmc035.txt"
.global vdd! vss! 0

.subckt ind1 LC LC1 LC2

    C2 LC2 net016 52.1f
    C0 LC1 net8 56.7f
    R3 LC1 net13 10.25
    R4 LC2 net024 10.25
    R5 0 net016 4.3
    R2 0 net8 4.58
    L1 LC net024 5.1n ic=2.99m
    L0 LC net13 5.1n ic=3.01m

.ends

.subckt current_source_schematic Output
MP5 Output a4 vdd! vdd!  CMOSP  L=0.7u W=5u AD=800e-15 AS=800e-15
+ PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25 M=110
MP4 net33 a4 vdd! vdd!  CMOSP  L=0.7u W=5u AD=800e-15 AS=800e-15
+ PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25 M=10
MP3 a4 a3 net33 vdd!  CMOSP  L=0.7u W=5u AD=800e-15 AS=800e-15
+PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25 M=10
MP1 a1 a3 vdd! vdd!  CMOSP  L=0.7u W=5u AD=800e-15 AS=800e-15
+PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25  M=2
MP2 a3 a3 vdd! vdd!  CMOSP  L=0.7u W=5u AD=800e-15 AS=800e-15
+PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25 M=2
I0 vdd! a2 500u
MN7 net52 a2 vss! vss!  CMOSN  L=0.7u W=2.2u AD=800e-15 AS=800e-15
+ PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25  M=10
MN6 a4 a1 net52 vss!  CMOSN  L=0.7u W=2.2u AD=800e-15 AS=800e-15
+PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25 M=10
MN2 a3 a1 net64 vss!  CMOSN  L=0.7u W=2.2u AD=800e-15 AS=800e-15
+PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25 M=10
MN3 net64 a2 vss! vss!  CMOSN  L=0.7u W=2.2u AD=800e-15 AS=800e-15
+ PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25 M=10
MN1 a1 a1 vss! vss!  CMOSN  L=0.7u W=2.2u AD=800e-15 AS=800e-15
+PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25 M=2
MN5 net72 a2 vss! vss!  CMOSN  L=0.7u W=2.2u AD=800e-15 AS=800e-15
+ PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25  M=2
MN4 a2 a1 net72 vss!  CMOSN  L=0.7u W=4.4u AD=800e-15 AS=800e-15
+PD=3.6e-6 PS=3.6e-6 NRD=1.25 NRS=1.25  M=5

.ends


X33 net042 out1 out2 ind1
X32 net042 current_source_schematic
MP9 vss! out1 vss! Vc CMOSP w=2u l=3u m=48
MP8 vss! out2 vss! Vc CMOSP w=2u l=3u m=48
MN3 out1 out2 cmd1 vss! CMOSN w=11u l=800n m=16
```

```
MN0 out2 out1 cmd2 vss! CMOSN w=11u l=800n m=16
R1 cmd1 vss! 50
R2 cmd2 vss! 50

*Buffer Design
MNB1 outd1 out1 cd vss! CMOSN W=2u L=0.7u m=20
MNB2 outd2 out2 cd vss! CMOSN W=2u L=0.7u m=20
Ibuf cd vss! 5m
Rbuf1 outd1 vbuf 900
Rbuf2 outd2 vbuf 900

V42 vbuf 0 DC 4
C1 outd1 vss! 1p
C2 outd2 vss! 1p
.print v(out1,out2)

V1 vdd! 0 DC 3.3
V2 Vc 0 1.0
V3 vss! 0 0

.op
.tran 0.01n 60n
.probe id1 = i(R1)
.probe id2= i(R2)
.probe it = i(vdum)
.fft v(out1) start=20n stop=50n np=16384 window=kaiser

.end
```

APPENDIX B: Inductor layout using ASITIC

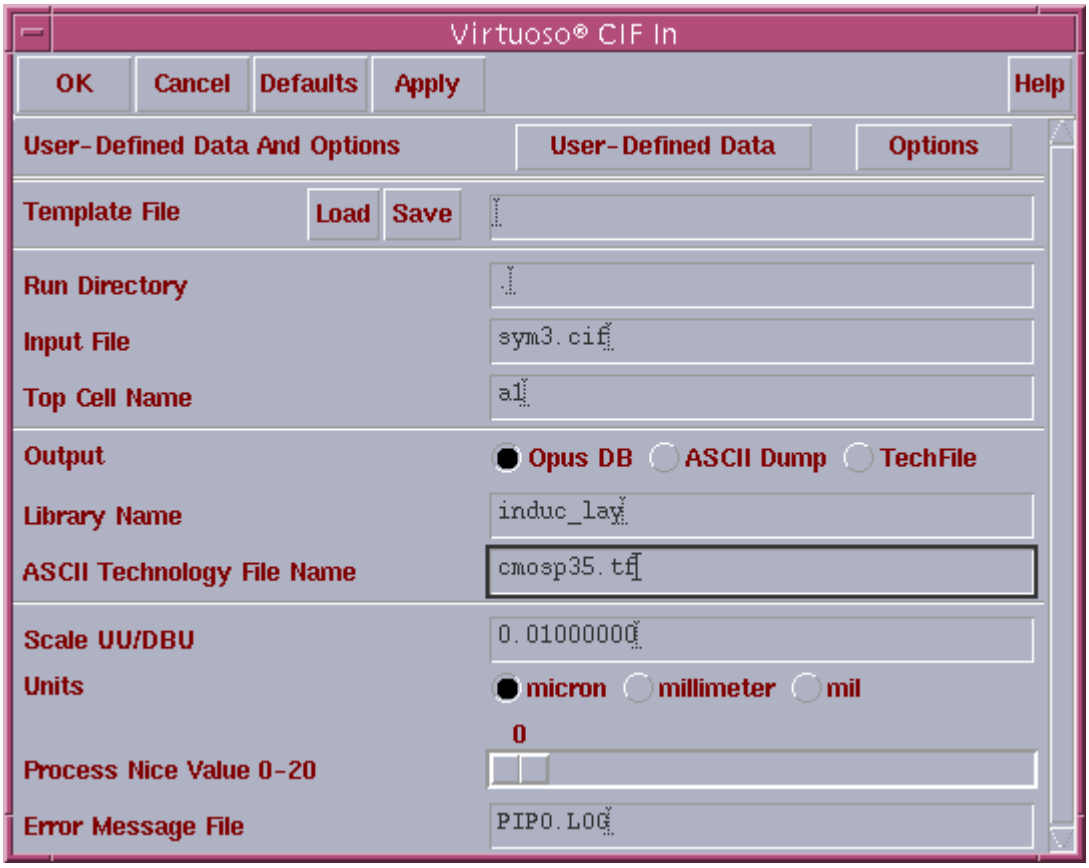
ASITIC Commands to generate the inductor structure

```
################################################
# ASITIC ver 03.19.00.01.29.01 INPUT/OUTPUT LOG File
# Generated on Tue Oct 21 23:03:54 2003
################################################

Technology File Name? tsmc.tek

ASITIC>  sympoly

Name? a5

Radius (center to edge)? 170

Metal width? 15

Metal layer? m4

Transition metal layer? m3

Spacing (metal edge to metal edge)? 4.5

Space for Transitions: 22

How many sides (>2)? 8

Turns? 5

Origin of spiral center (x y)? 20 20

ASITIC>  pi a5 2


Pi Model at f=2.00 GHz:  Q = 8.0, 8.5, 8.6
L  =  10.2 nH     R  =  10.25
Cs1=  56.1 fF     Rs1=  4.59
Cs2=  56.7 fF     Rs2= 4.58   f_res =  8.24GHz
```

Saving ASITIC layout in CIF

```
CIFSave a5 sym3.cif (1 10 poly)
```

Importing CIF in Cadence



APPENDIX C: Phase noise calculation

MATLAB code

```
load tran_normal.txt
t1 = tran_normal(:,2);
out=tran_normal(:,3);
%out2=f12(:,4);
%out=out1-out2;
if(out(2) > out(1))
    first=1;
    a_high_old=out(1);
else
    first=0;
    a_low_old=out(1);
end;
stop=1;
high_stop=1;
low_stop=1;
n_low=2;
n_high=2;

while(stop)
 if(first)
        while(high_stop)
             if(out(n_high) >= a_high_old)
                a_high_old = out(n_high);
                n_high= n_high+1;
            else
                high_stop=0;
                n_low=n_high;
                t_high_old=t1(n_high-1);
                a_low_old=a_high_old;
                first=0;

            end
        end

    else
        while(low_stop)
            if(out(n_low) <= a_low_old)
                 a_low_old = out(n_low);
                 n_low = n_low+1;
             else
               low_stop=0;
               n_high=n_low;
               t_low_old = t1(n_low-1);
               a_high_old=a_low_old;
               first=1;
           end
       end
      end
```

```
    if(high_stop==0 & low_stop==0)
       stop=0;
   end
end
gold_time=abs(t_low_old-t_high_old).*2;

if(t_low_old > t_high_old)
    k=n_low+1;
    nxt=1;
    a_high_nxt=a_low_old;
else
    k=n_high+1;
    nxt=0;
    a_low_nxt=a_high_old;
end

stop=1;
k1=1;
k2=1;
count=k;
high_stop=1;
low_stop=1;
    while(stop)
         if(nxt)
             while(high_stop & (count < size(out)))
                  if(out(count) >= a_high_nxt)
                 a_high_nxt = out(count);
                     count=count+1;
                 else
                    high_stop=0;
                    low_stop=1;
                    nxt=0;
                    delt_high(k1)=t1(count-1)-t_high_old;
                    k1=k1+1;
                    t_high_old=t1(count-1);
                    a_low_nxt = a_high_nxt;
                    count=count+1;
                end
            end
        else
            while(low_stop & (count < size(out)))
                  if(out(count) <= a_low_nxt)
                     a_low_nxt = out(count);
                     count=count+1;
                 else
                    low_stop=0;
                    high_stop=1;
                    nxt=1;
                    delt_low(k2)=t1(count-1)-t_low_old;
                    k2=k2+1;
                    t_low_old=t1(count-1);
                    a_high_nxt=a_low_nxt;
                    count=count+1;
                end
            end
```

```
    end
    if(count > (size(out)-1))
        stop=0;
    end
end

jitter_high=max(abs(delt_high-gold_time));
jitter_low=max(abs(delt_low-gold_time));
```

VITA

Lakshmipriya Seshan was born on the 30th of April 1979 in Trivandrum, India. She received her high school diploma from All Saints College, Trivandrum in 1996. Interested in an engineering career, she enrolled at College of Engineering, Trivandrum, majoring in Electronics and Communication Engineering. In June' 2000, she graduated with a Bachelor of Technology degree in Electronics and Communication. She then began her career in the industry and was employed at Wipro Technologies, Bangalore, as a VLSI/System Design Engineer, where she worked for a year. In Fall 2001, she enrolled at the University of Tennessee, Knoxville to earn a Master's in Electrical Engineering. She is currently working under the supervision of Dr.Syed K. Islam at the Analog VLSI and Devices Laboratory. She plans to complete her Master's with a specialization in Analog IC design in May 2004.