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A Lock-In Amplifier for Fluorescent Light Detection

Osman Oguz
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Osman Oguz entitled "A Lock-In Amplifier for Fluorescent Light Detection." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

S. K. Islam, Major Professor

We have read this thesis and recommend its acceptance:

A. L. Wintenberg, M. O. Pace

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A Lock-In Amplifier
For
Fluorescent Light Detection

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Osman Oguz

August 2002

Dedication

This thesis is dedicated to
my loving wife Merve and
my beautiful daughter Zeynep
for their daily support and sincere love.

Acknowledgments

First, I would like to express my sincere thankfulness to Dr. A. L. Wintenberg and Dr. S. K. Islam for their guidance, support and friendship throughout my master study.

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Most importantly, I thank my dearest loving friend and wife, Merve and her gift: my beautiful daughter Zeynep.

Abstract

An integrated on-chip lock-in amplifier has been developed for fluorescent light detection for biological applications. The system includes 2.1 μm x 2.1 μm tiny chip using a photodiode transimpedance amplifier topology for the pre-amp, followed by gain amplifier, demodulator and filtering stages. Synchronous demodulator or phase sensitive detector stage has two different architectures to demonstrate the difference between the results. The recommended transmitting light frequency is between 0.5 kHz to 5 kHz. We used 1 kHz frequency for the test.

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Abbreviations

BW	Bandwidth
CMOS	Complementary Metal-Oxide Semiconductor
DR	Dynamic Reserve
GBW	Gain Bandwidth
IC	Integrated Circuit
LED	Light Emitting Diode
LPF	Low Pass Filter
MDS	Minimum Detectable Signal
NBW	Noise Bandwidth
NF	Noise Figure
PLL	Phase Locked Loop
PM	Phase Margin
R4BS	Operational Amplifier
SNR	Signal to Noise Ratio
SR	Slew Rate

Chapter 1

General Considerations

1.1 Fluorescent Light Detection

When the light travels through an object several things can happen to the light. If the light strikes an object and bounces back, reflection has occurred. Transmission takes a place when the light cannot be affected by an object and can pass throughout it. In refraction, the light passes from one medium to another of different density. Absorption has occurred when the object takes up these light photons (figure 1.1.1). If these absorbed light photons are changed into longer wavelengths and reemitted, luminescence takes place. If it happens only during the time when light photons are striking an object, fluorescence occurred [31], [32], [47]. In other words, when a molecule absorbs a photon, one of its electrons is energized or excited. The electron may return to its lowest possible energy level. If this happens, its energy is dissipated as heat or as light of a longer wavelength than the wavelength of the absorbed light. This emission of light is called fluorescence. As an analytical technique (expose material to light and look at fluorescence with a detector), fluorescence light detection is applied to identify molecules [46].

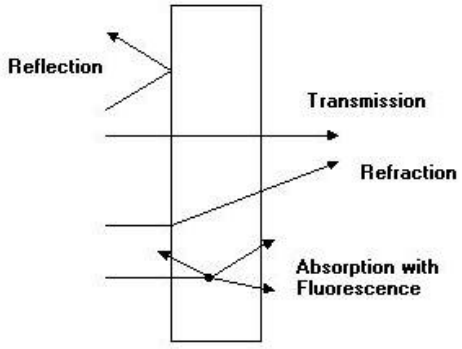

Figure 1.1.1 Several interactions of light photons when it strikes an object

Identifying molecules is very important in biotechnology. Radioactive labels are sometimes used along with radiation detectors. Fluorescence light detection has been used as an alternative to radioactive detection methods. A variety of sensing schemes have been developed for detection, such as electrochemical, optical absorption, and interferomic sensing. However, fluorescence sensing remains the most widely used methodology in biotechnology. Fluorescence detection offers exquisite sensitivity, compatibility, easy quantization, stability and low costs [35].

Traditional bio-fluorescence readers use bulky and discrete elements, which are expensive and require large equipment and precise alignment. The advantages of integrated biological analysis systems are compromised when these systems rely upon large and fragile optical sensing equipment. Integrated on-chip sensing architectures make these systems portable, robust, and practical. The integrated circuit contains the devices and circuits for detection of the optical signal and for recovery of this signal from the noise.

1.2. Lock-in Detection

Signal recovery instruments will always be in demand as long as experiments attempt to measure weak signals. For increasing the signal to noise ratio of a noisy signal, the most useful experimental technique is lock-in amplifier detection or phase sensitive detection. The lock-in amplifier detection's main basis is compressing all the signal information into a very narrow bandwidth (Δf) and amplify only frequencies in this bandwidth, and rejecting all noise outside Δf [1]. It really depends on knowing signal frequency and phase or having narrow-band signal information. Very small signals can be detected in the presence of large amounts of uncorrelated noise when the frequency and phase of desired signal are known. Lock-in detector is basically a synchronous demodulator followed by a low-pass filter. It amplifies only the component of the input signal at the reference signal frequency, and filters out all other frequencies. Commercial lock-in amplifiers are very costly, large in dimension, heavy and absolutely not suitable for portable instrumentation. Thus, integrated lock-in amplifiers can provide several benefits compared to commercial lock-in amplifiers [3].

1.3 Noise

Any unwanted disturbance that comes with a signal of interest is generally referred to as noise [9]. Random noise finds its way into experiments in a variety of ways. Good experimental design can reduce these noise sources and improve the measurement stability and accuracy. There are a variety of noise sources, which are present in all electronic signals.

Interference noise is picked up from the outside world. Interference noise is caused by unwanted interaction between the circuit and outside, or even between different parts of the circuit itself. This interaction can be electric, magnetic, electromagnetic etc. Interference noise can be periodic or completely random.

Transmitted noise is inherent in the received signal. Inherent noise is random in nature and is due to random phenomena, such as the thermal agitation of electrons in resistors and the random generation and recombination of electron-hole pairs in semiconductors. Device noise is generated within the devices, which are used in the systems (pre-amps, resistors, etc). Resistors and semiconductor junctions generate random noise.

Several noise types such as thermal noise, shot noise, flicker noise etc. may be observed in a semiconductor circuit. As shown in figure 1.3.1, at low frequencies flicker noise is dominant while at higher frequencies thermal and shot noises are dominant factors [10].

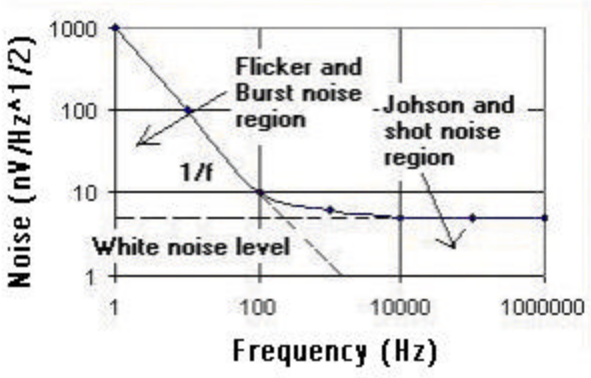

Figure 1.3.1 Noise spectral density plot

1.3.1 Johnson noise (Thermal noise)

Every resistor generates a noise voltage across its terminals due to thermal interaction between the free electrons. Resistors and the resistance within all electronic devices are constantly producing noise voltages, whose average power in a given bandwidth depends on temperature [13], [14]. This noise voltage is expressed as,

$$V_{noise}(rms) = (4kTRDf)^{1/2}\ , \qquad (1.1)$$

where k = *Boltzmann's constant* (1.38×10^{-23} *J / °K*), T is the temperature in Kelvin, R is the resistance generating the noise in ohms and Δf is the bandwidth of the measurement in Hz [7]. At room temperature $4kT = 1.66 \times 10^{-20}$ *V-C*.

1.3.2 Shot noise

Shot noise is introduced by carriers in the p-n junction of semiconductors. An electric current has noise due to the non-uniformity of the charge carriers in semiconductors. The distances traveled by the charge carriers vary because of random paths of motion. The rms current variation in a given bandwidth is a function of the dc current through the junction [13], [14]. The shot noise is given by

$$I_{noise}(rms) = (2qIDf)^{1/2}\ , \qquad (1.2)$$

where q is the electron charge, 1.6×10^{-19} coulomb, I is the rms ac current or dc current depending upon the circuit, and Δf is the bandwidth [7].

1.3.3 1 / f noise (Flicker noise)

Flicker noise effect occurs at low frequencies. It is inversely proportional to frequency and directly proportional to temperature. This is a type of noise found in all active devices. The origins of flicker noise are varied, but the noise occurs mainly due to random fluctuations in the amount of surface recombination [13], [14]. Flicker noise is always associated with a flow of direct current and displays a spectral density of the form,

$$I_{noise}(rms) = (K\frac{I^a}{f^b}\Delta f)^{1/2} \qquad (1.3)$$

where K is a constant for a particular device, a is a constant in the range 0.5 to 2, b is a constant of about unity, and Δf is a small bandwidth at frequency f [7].

Since flicker noise is insignificant compared to white noise in high frequencies, we can eliminate this noise effect by using the lock-in amplifier at high frequencies.

1.3.4 White noise

A uniform spectral density characterizes white noise [7]. Since white light consists of all visible frequencies in equal amounts, white noise is called by analogy with white light. It is independent of frequency [13]. White noise is present in all resistors and in semiconductor junctions. White noise, which appears in a resistor, is called thermal noise, and is called shot noise when it appears in semiconductor [14].

1.3.5 Total noise

All of these noise sources are incoherent. The total random noise is the square root of the sum of the squares of all the incoherent noise sources. Noise exists in all parts of the frequency spectrum; the noise contribution of a resistor or amplifier varies.

1.3.6 Signal to Noise ratio (SNR) and Noise Figure (NF)

Successfully detected and measured signal's quality is limited by the presence of noise and it is specified by means of the signal-to-noise ratio (SNR). In other way, SNR is the ratio of signal power to noise power in the output of the circuit. SNR can be expressed mathematically as

$$SNR = (Signal\ Power) / (Noise\ Power) = P_s / P_n. \qquad (1.4)$$

It is often expressed in dB form as

$$SNR = 10 \log (P_s / P_n), \qquad (1.5)$$

where P_s is the rms value of the signal, and P_n is that of its noise component, of course,

$$P = V^2 / R \quad or \quad P = I^2 R. \qquad (1.6)$$

The poorer the SNR, the more difficult it is to rescue the useful signal from noise. To exactly specify how noisy the device is in decibels, n*oise figure (NF)* is usually used.

$$NF = 10 \log [(Si / Ni) / (So / No)] = 10 \log (NR), \qquad (1.7)$$

where (S_i / N_i) is the signal to noise power ratio at the device's input and (S_o / N_o) is the signal to noise power ratio at its output. The term $[(S_i / N_i) / (S_o / N_o)]$ is called the noise ratio (NR) [7].

Signal-to-noise ratio becomes better by using larger time constants in lock-in amplifier applications. If the noise is only white noise, the lock-in amplifier does not perform better than a low pass filter.

1.3.7 Minimum Detectable Signal (MDS)

Minimum detectable signal can be defined as the signal for which *SNR = 1 [7]*.

So, for a circuit such as an amplifier with known V_{on} (rms output noise), the minimum detectable signal would be

$$S_{min} = V_{on} / Gain. \qquad (1.8)$$

The minimum detectable signal can be written as a function of the quantum efficiency, the leakage current, the noise of the photo detector and the noise and filtering characteristics of the signal recovery circuit. When the dark current of the photodiode is zero, MDS is given by,

$$MDS = \frac{1}{qh}\sqrt{\frac{4qA_{PD}I_S}{T_{INT}}}, \qquad (1.9)$$

where q is the electron charge *(1.6 x 10^{-19} coulomb)*, A_{PD} is the area of the photodiode, T_{INT} is the period of the signal, and I_S is the photodiode reverse bias current. For minimizing the MDS, η and T_{INT} must be maximized while for maximizing the MDS, I_S

and A_{PD} must be minimized. Small photodiode area provides a poor light collection efficiency, so signal process may be optimized by minimizing the I_S [29].

1.4 Lock-in Architecture

In the lock-in architecture, an input signal (embedded in noise) is amplified and rectified by a reference signal (it has same frequency with the input signal). A low-pass filter with a low cut-off frequency reduces the last noise harmonics. In this manner, the output of the filter is a voltage proportional to the amplitude of the input signal, while the noise is reduced by the synchronous demodulation operation (figure 1.4.1).

The input stage consists of a pre-amplifier and a gain stage. They pre-process the input signal buried in noise by amplifying it to a suitable level for the demodulator. They also increase the signal at the desired level.

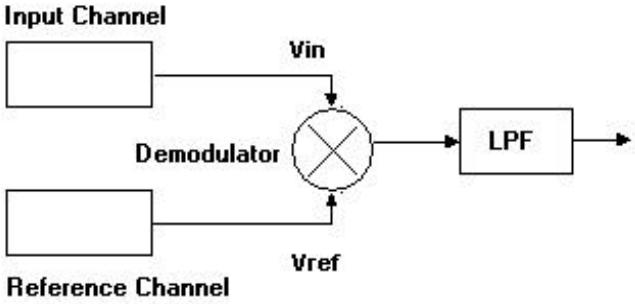

Figure 1.4.1 Block diagram of the lock-in amplifier

The reference channel provides the reference signal to be multiplied or phase shifted with the signal. A signal generator or a phase locked loop (PLL) can be used as a reference channel.

The demodulator is a full wave rectifier, which rectifies the input signal by using the reference signal. When the input signal and the reference signal have the same frequency, the demodulator output has a DC component proportional to the input signal amplitude and the cosine of the phase difference between the signals. The phase difference between the input signal and the reference can be brought to zero. The adjustment of the phase of the reference signal is done using a reference channel.

Noise will still be present at the output of the demodulator because of the presence of harmonics. For this reason, a low-pass filter has to be added to the output of the demodulator. A low-pass filter characterized by a low cut-off frequency is necessary to reduce the noise superimposed on the DC signal. Thus the lock-in amplifier can improve the SNR.

1.5 Scope of Thesis

This thesis presents both theoretical study and experimental verification of lock-in amplifiers for fluorescent light detection for biological applications. Amplifiers were implemented on the same substrate with the photo detector by using AMI 1.5 μm CMOS technology.

This thesis is divided five chapters. The first chapter introduces the lock-in amplifier. Chapter 2 is an overview of the mathematical theory of lock-in systems. The

third chapter describes the design of each building block, which is used in this work. Some critical issues are also addressed. Chapter 4 presents the test procedure and experimental results obtained for the prototype. Chapter 5 provides a summary and recommendations for future work.

Chapter 2

Lock-In Amplifier Theory

A lock-in amplifier is responsive to the amplitude of a signal but is also sensitive to the phase difference between an input signal and a reference signal. Phase sensitive detector or lock-in amplifier based systems can therefore be devised to measure variations in both the amplitude and phase of periodic signals in the presence of noise and interference. The treatment of lock-in amplifier response is unavoidably mathematical and one needs to know some basic transform methods.

We will focus on the use of lock-in amplifiers for the signal recovery problem and our objective will be to examine the general characteristics of signals and noise. Although the first step in signal recovery is the elimination of unwanted noise by filtering, signals and noise cannot be separated adequately by only filtering. A lock-in amplifier adds an additional step of demodulation.

Demodulators for signal recovery are supplied with a reference signal, which is precisely synchronized with the signal of interest. In general terms, operation depends on the high degree of correlation, which is known to exist between a periodic signal of interest and a reference signal.

In our experiment, measuring instrument has several noise sources, including flicker noise at low frequencies, dark current associated noise, and variations in light leaking into the instrument and reaching the photodiode from other sources.

If we show distribution of noise and signal power as shown in figure 2.1, we can say that the signal of interest is very small compare to the noise. The instrument becomes unusable with this result. Y-axis is in units of power per unit bandwidth in this figure, hence, the area under the corresponding curves represents the signal powers and the total noise.

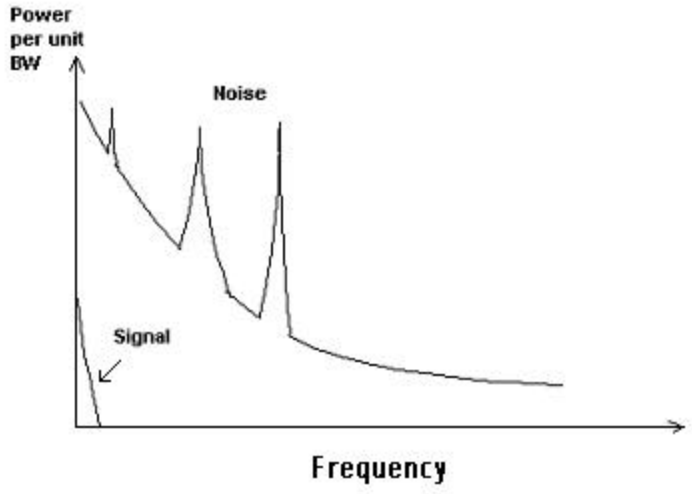

Fig 2.1 Representation of the signal buried in noise

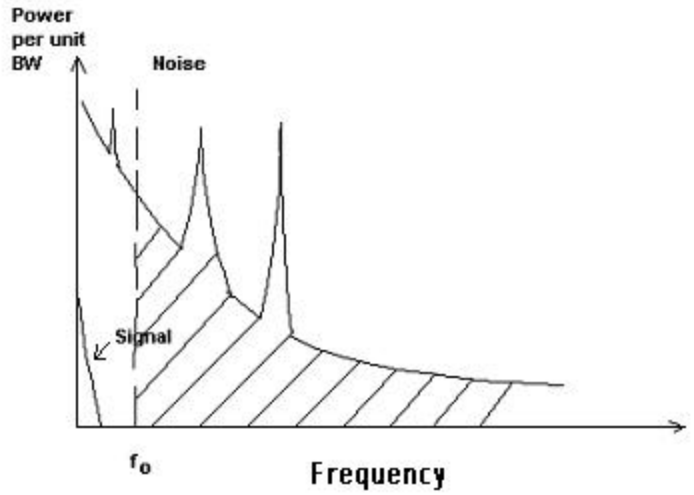

Figure 2.2 Representation of the LPF effect to the noisy signal

As shown in figure 2.2, a low pass filter can eliminate all noise signals beyond cut-off frequency, but still the noise is quite larger than the signal. It cannot give us any satisfactory signal to noise ratio. What we really need to do is to measure this signal far from the flicker noise effects, where white noise is dominant. We can move the signal away from a region where the background noise is high to a region where it is low using the synchronous demodulator at high frequencies (figure 2.3). In this case lower bandwidth gives better signal-to-noise ratio. The last stage of the lock-in amplifiers is the low pass filter, which eliminates the last harmonics of the signal beyond its cut-off frequency.

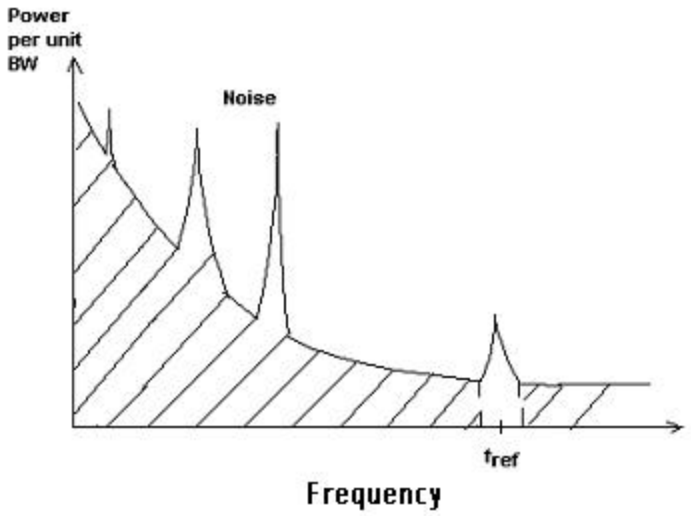

Figure 2.3 Representation of the synchronous demodulator effect to the noisy signal

2.1 Lock-in Experiment

The principal building blocks of the lock-in amplifier for fluorescent light detection are the excitation and the detection states. In the excitation state, light excites the fluorescence of biological materials. The detection state is built by several amplifier blocks and is followed demodulator and low pass filter.

The main approach to excite and detect the fluorescence is to send the input signal to the excitation state at the same frequency and phase with the reference signal into the demodulator. Using the same signal generator for both signals will be our main design implementation. In this case, excitation and detection states together are called signal channel. The signal channel of the lock-in amplifier contains an n-well/p-substrate photodiode, a wide band preamplifier, x100 voltage gain amplifier, demodulator and low pass filter. Reference channel is totally independent and it sends its signal to both LED

and demodulator at the same time. Therefore, both the reference and the input signal frequencies are the same while the phase difference is zero.

We will use the photo-detector circuit to test the noise rejection of our lock-in amplifier. The signal of interest will be a train of light pulses from an LED. We want the lock-in amplifier to detect the rms voltage from the photo-detector that is due to the LED and to reject everything else. A test circuit for noise rejection of lock-in amplifier is shown in figure 2.1.1.

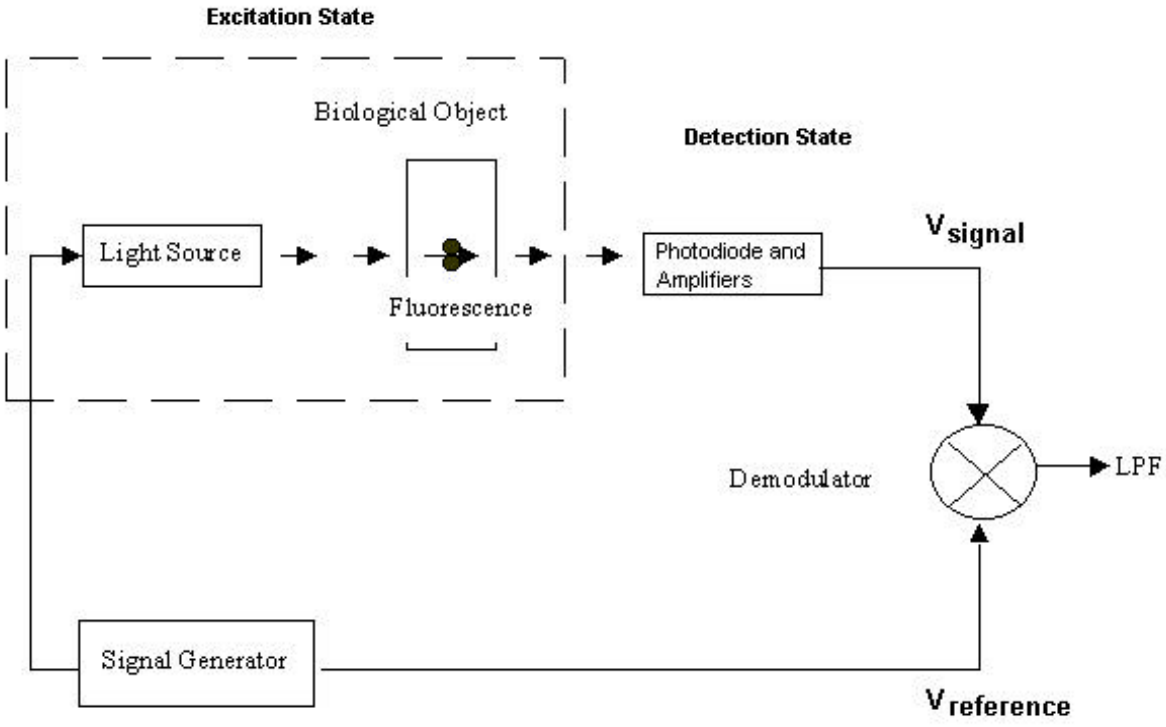

Figure 2.1.1. Test implementation of the lock-in amplifier

If we show both V_{signal} and $V_{reference}$ as sinusoidal signals for simplicity, the input signals of the demodulator can be represented as follows,

$$V_{sig}(t) = V_s \, Cos\,(\nu_s t + j_s) \qquad (2.1)$$

$$V_{ref}(t) = V_{ref} \, Cos\,(\nu_{ref} t + j_{ref}). \qquad (2.2)$$

Output of the demodulator is equal to

$$V_{demod\_out} = V_{ref}(t) * [\, V_{sig}(t) + V_{noise}(t) \,] \qquad (2.3)$$

$$V_{demod\_out} = V_{ref}(t)\, V_{sig}(t) + V_{ref}(t)\, V_{noise}(t). \qquad (2.4)$$

Since there is no correlation between the V_{ref} and V_{noise} [1], the average product of

$$V_{ref}(t) * V_{noise}(t) = 0, \quad then, \qquad (2.5)$$

$$V_{demod\_out} = V_{ref}(t)\, V_{sig}(t) \qquad (2.6)$$

$$V_{demod\_out} = V_s \, V_{ref} \, Cos\,(\nu_s t + j_s) \, Cos\,(\nu_{ref} t + j_{ref}). \qquad (2.7)$$

Trigonometric equivalent of the expression (2.7) is

$$V_{demod\_out} = V_s \, V_{ref} \, (1/2\, [Cos\,(\nu_s t - \nu_{ref} t + j_s - j_{ref}) + Cos(\nu_s t + \nu_{ref} t + j_s + j_{ref})]. \qquad (2.8)$$

If $\nu_s = \nu_{ref}$ (same frequency due to same source), then the demodulator output is equal to

$$V_{demod\_out} = (1/2)\, V_s \, V_{ref} \, [\, Cos\,(j_s - j_{ref}) + Cos\,(2\nu_s t + j_s + j_{ref}) \,]. \qquad (2.9)$$

The low pass filter eliminates the cut-off frequency components:

$$Cos\ (\ 2\nu_s\ t + \ j_s + j_{ref}\ ) = 0, \qquad (2.10)$$

Hence, the low pass filter output is

$$V_{lpf\_out} = (1/2)\ V_s\ V_{ref}\ [\ Cos\ (j_s - j_{ref}\ )\ ]. \qquad (2.11)$$

$j_s = j_{ref}$ (same phase due to same source), hence,

$$Cos\ (j_s - j_{ref}\ ) = Cos\ 0 = 1. \qquad (2.12)$$

The low pass filter output is equal to half of multiplied amplitudes of the input signal ($V_{sig}(t)$) and the reference signal ($V_{ref}(t)$) putting (2.12) in (2.11):

$$V_{lpf\_out} = (\ 1/2\ )\ V_s\ V_{ref}\ . \qquad (2.13)$$

To find exact input signal to the demodulator, we need to include the gain stage specifications,

$$V_{lpf\_out} = \ (\ 1/2\ )\ V_s\ V_{ref}\ *\ Av \qquad (2.14)$$

or

$$V_s = [2\ *\ (V_{lpf\_out})]\ /\ [V_{ref}\ *\ Av]. \qquad (2.15)$$

The pre amplifier characteristics are also important since we are interested in finding the photodetector input current, therefore,

$$I_s = V_s\ /\ R_{pre} \quad and \qquad (2.16)$$

$$I_s = [2 * (V_{lpf\_out})] / [V_{ref} * Av * R_{pre}] \quad (2.17)$$

where, I_S is the input current of the photodiode in amps, V_S is the amplitude of the input signal after the pre-amplifier stage in volts, and R_{pre} is the feedback resistor of the pre-amplifier stage in ohms. They are represented in figures 2.1.1 and 2.1.2.

Lock-in amplifiers as a general rule display the input signal in volts (rms) [22].

$$V(rms) = \left[\frac{1}{T}\int_0^T V_S{}^2 Sin^2 wtdt\right]^{1/2} = \frac{V_S}{\sqrt{2}} = 0.707V_S \quad (2.18)$$

$$V_S = V(rms) * \sqrt{2} \quad (2.19)$$

where V_S is the amplitude of the input signal. When the lock-in amplifier displays a magnitude of 1 V (rms), the component of the input signal at the reference frequency is 1.41 V amplitude or 2.82 V peak to peak.

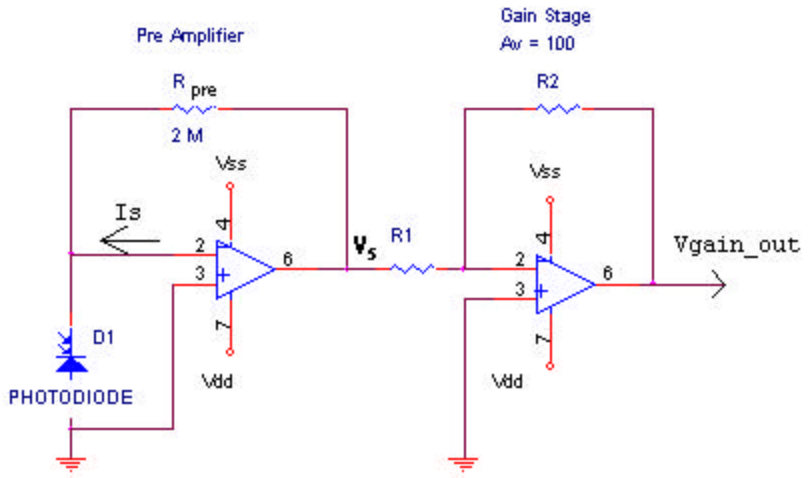

Figure 2.1.2 Representation of the preamplifier and the gain circuit

2.2 Mathematical Expressions

For more detailed explanation, we need to find Fourier expression of a square wave signal in this section. Fourier analysis basically says that any function can be written as a sum of sine and cosine functions of different frequencies and amplitudes.

Since we are interested in square wave signals for lock-in amplifier detection, Fourier series of a square wave signal (figure 2.2.1) can be shown by these expressions:

$$V_{ref}(t) = V_{ref} \quad 0 < t < T / 2 \qquad (2.20)$$

$$V_{ref}(t) = -V_{ref} \quad T / 2 < t < T \qquad (2.21)$$

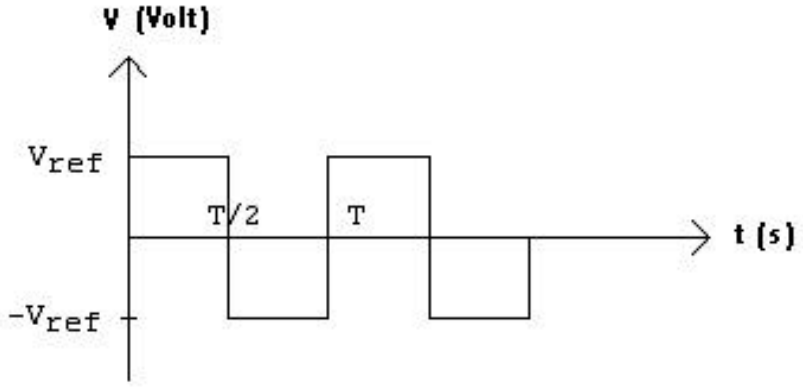

Figure 2.2.1 Square wave reference signal

Fourier series expression of that square wave signal is

$$F(t) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty}(a_n Cosn\nu t + b_n Sinnwt) \tag{2.22}$$

$$a_0 = \frac{1}{T}\int_0^T V_{ref}(t)dt \tag{2.23}$$

$$a_n = \frac{1}{T/2}\int_0^T V_{ref}(t)Cosnwtdt \tag{2.24}$$

$$b_n = \frac{1}{T/2}\int_0^T V_{ref}(t)Sinnwtdt \tag{2.25}$$

Average value of the reference signal is

$$a_o / 2 = 0. \tag{2.26}$$

To find the expression (2.24), we need to follow below process:

$$a_n = \frac{2}{T}\left[\int_0^{T/2} V_{ref}Cosnwtdt + \int_{T/2}^{T} -V_{ref}\cos nwtdt\right]$$

$$a_n = \frac{2V_{ref}}{Tnw}\left[Sinnwt\right]_0^{T/2} - \left[Sinnwt\right]_{T/2}^{T}$$

$$w = \frac{2p}{T} \Rightarrow$$

$$a_n = \frac{V_{ref}}{np}(2Sinnp - Sinn2p)$$

$$a_n = 0 \tag{2.27}$$

for all n.

Using same process for (2.25),

$$b_n = \frac{2}{T}\left[\int_0^{T/2} V_{ref} Sinnwtdt + \int_{T/2}^{T} -V_{ref} Sinnwtdt\right]$$

$$b_n = \frac{2V_{ref}}{Tnw}\left[-Cosnwt\right]_0^{T/2} + \left[Cosnwt\right]_{T/2}^{T}$$

$$w = \frac{2p}{T} \Rightarrow$$

$$b_n = \frac{V_{ref}}{pn}\left(-Cosnp + \cos 0 + Cosn2p - Cosnp\right)$$

$$b_n = \frac{2V_{ref}}{pn}(1 - Cosnp)$$

$$b_n = \frac{4V_{ref}}{pn} \qquad (2.28)$$

for n = 1,3,5,…

Obtaining the (2.26), (2.27) and (2.28) the result of the expression (2.22) is

$$F(t) = \frac{4V_{ref}}{p} Sinwt + \frac{4V_{ref}}{3p} Sin3wt + \frac{4V_{ref}}{5p} Sin5wt + ... \qquad (2.29)$$

$$F(t) = \frac{4V_{ref}}{p}\left(Sinwt + \frac{1}{3} Sin3wt + \frac{1}{5} Sin5wt + ...\right) \qquad (2.30)$$

The line spectrum (figure 2.2.2) for this series contains only odd harmonic sine terms. Its series contain only sine terms because the wave is odd function; and since it also has half-wave symmetry, only odd harmonics are present [37].

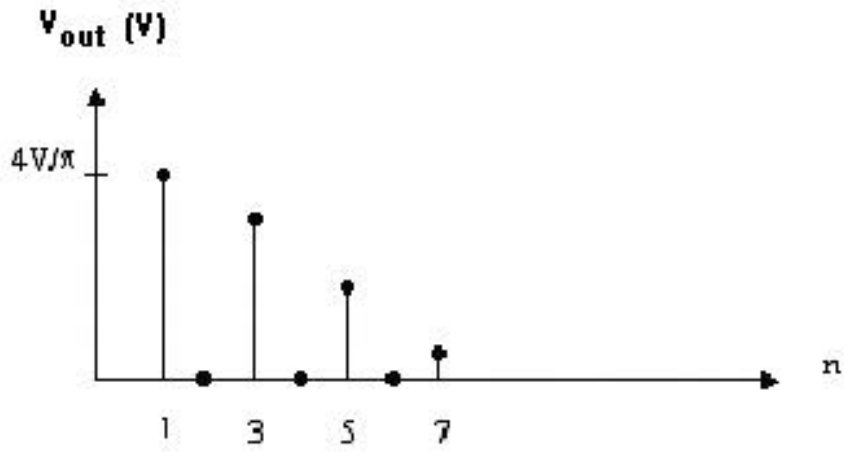

Figure 2.2.2 Line spectrum of the square wave signal

The expressions of the lock-in amplification are shown below. $V_{sig}(t)$ is a sinusoidal input signal and $V_{ref}(t)$ is a square wave signal where amplitude of the $V_{ref}(t)$ *is 1 V*.

For figure 2.2.3,

$$V_{sig}(t) = V_S \, Sin(wt) \qquad (2.31)$$

$$V_{ref}(t) = \frac{4*1}{p}\left[Sin(wt) + \frac{1}{3} Sin(3wt) + \ldots \right] \qquad (2.32)$$

$V_{demod\_out} = V_{sig}(t) * V_{ref}(t)$ Þ *(2.33)*

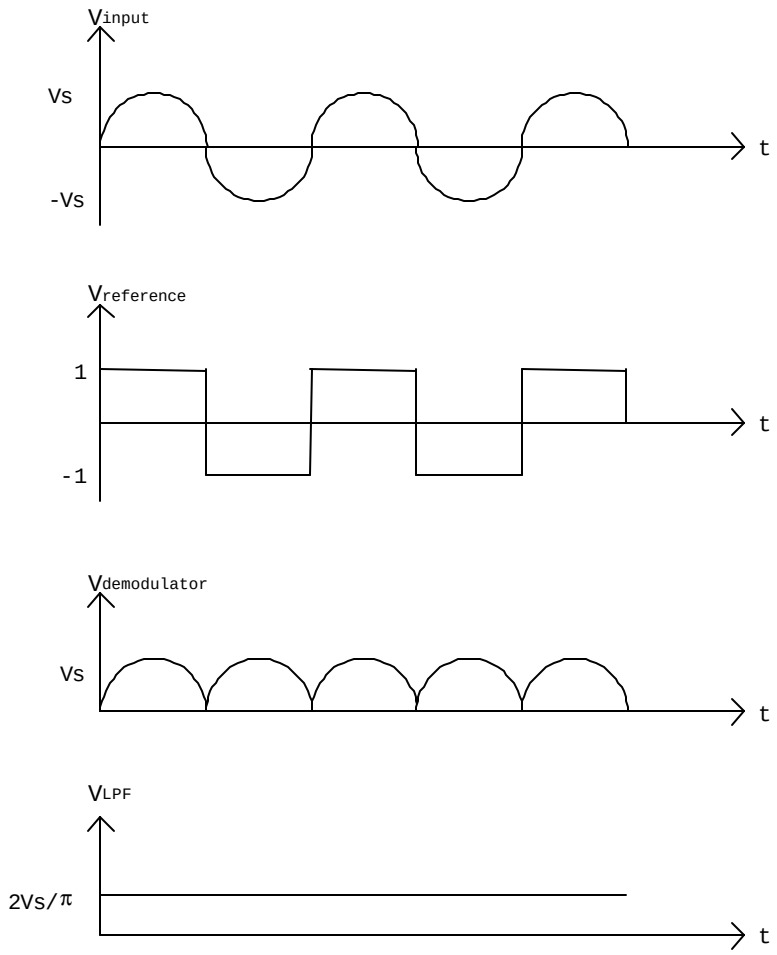

Figure 2.2.3 Outputs of the demodulator and LPF for sine wave input and square wave reference signals

The process of (2.33) can be shown as follows:

$$V_{demodulator\_out} = \frac{4V_S}{p}[Sin(wt)][Sin(wt) + \frac{1}{3}Sin(3wt) + ...]$$
$$V_{demodulator\_out} = \frac{4V_S}{p}[Sin^2(wt) + \frac{1}{3}Sin(wt)Sin(3wt) + \frac{1}{5}Sin(wt)Sin(5wt) + ...]$$
$$V_{demodulator\_out} = \frac{4V_S}{p}[\frac{1-Cos(2wt)}{2} + \frac{1}{3}\frac{1}{2}[Cos(2wt) - Cos(4w] + \frac{1}{5}\frac{1}{2}[Cos(4wt) - Cos(6wt)] + ...]$$
$$V_{demodulator\_out} = \frac{4V_S}{p}[\frac{1}{2} - \frac{2}{6}Cos(2wt) - \frac{2}{30}Cos(4wt) - \frac{2}{70}Cos(6wt) - ....]$$
$$V_{demodulator\_out} = \frac{2V_S}{p}[1 - \frac{2}{3}Cos(2wt) - \frac{2}{15}Cos(4wt) - \frac{2}{35}Cos(6wt) - ....] \qquad (2.34)$$

As a result, the low pass filter output will be equal to amplitude of equation (2.34),

$$V_{lpf\_out} = \frac{2V_S}{p} \qquad (2.35)$$

If both input and reference signal are square wave signal (figure 2.2.4), the demodulator output becomes:

$$V_{demodulator\_out} = \frac{16V_S}{p^2}[Sin(wt) + \frac{1}{3}Sin(3wt) + \frac{1}{5}Sin(5wt) + ...]^2 \qquad (2.36)$$

where amplitude of the V_{ref} is 1 V, hence, the low pass filter output is

$$V_{lpf\_out} = \frac{16V_S}{2p^2} + \frac{16V_S}{18p^2} + \frac{16V_S}{50p^2} + ... \qquad (2.37)$$

or

$$V_{lpf\_out} \gg V_s . \qquad (2.38)$$

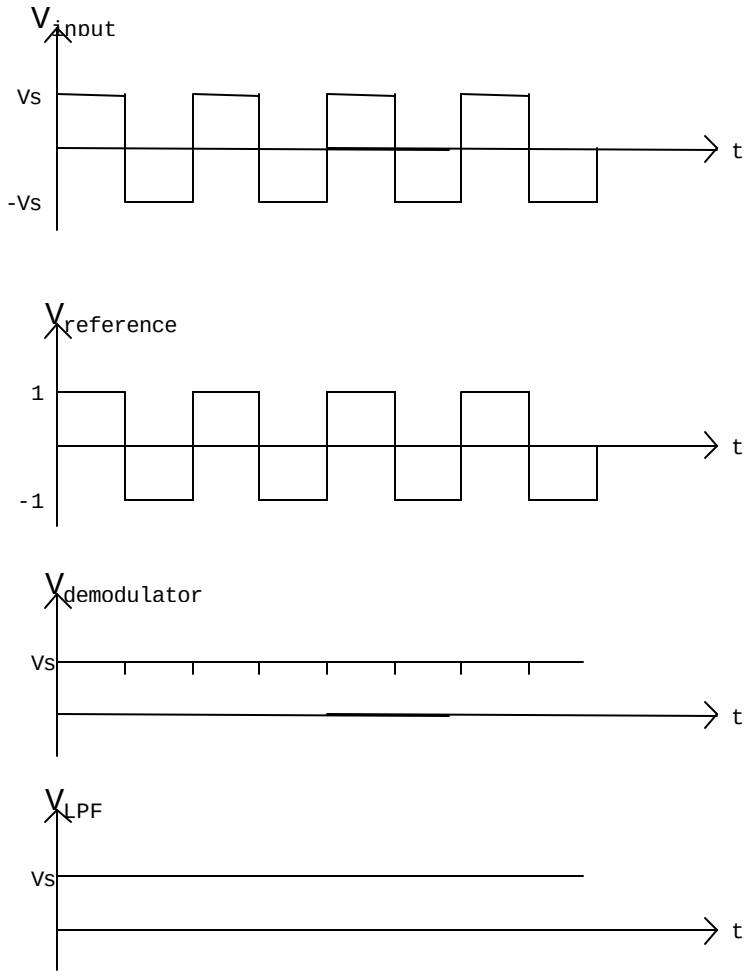

Figure 2.2.4 Outputs of the demodulator and LPF for square wave input and reference signals

Again, strictly speaking, we are using the synchronous demodulator as a full wave rectifier in this test. In this manner, demodulator output is nothing but full wave rectified signal of the input signal. If the input signal and the reference signal are still at the same frequency but out of phase, then

$V_{sig}(t) = V_s \, Sin(\nu t + j)$ *(2.39)*

The first dc term of the Fourier expression of demodulator output is now

$$V_{de\,\mathrm{mod}\,ulator\_out} = \frac{2V_S}{p} Cos\, j \quad . \qquad (2.40)$$

Therefore, the dc level of the low-pass filter output will be proportional to the cosine of the phase difference between the input signal and the reference signal. Generally speaking, as shown in figures 2.2.5 and 2.2.6, the dc component of the low pass filter output varies with the phase difference.

$j = 0 \;\; Þ \;\; V_{lpf\_out} = 2V_s / p$

$0 < j < 90° \;\; Þ \;\; 0 < V_{lpf\text{-}out} < 2Vs / p$

$j = 90° \;\; Þ \;\; V_{lpf\_out}$ *t = 0, and so on.*

Any odd multiplies of the reference frequency in the input signal will contribute to the dc output while even multiplies of the reference frequency will all average to zero [25]. The switch is in the (+1) gain 'on' position from (0 to T / 2) and in the (–1) gain 'off' position from (T / 2 to T) where $f_{ref} = 1 / T$ (figure 2.2.3) and f_{ref} = *the switch frequency*. If the input signal frequency differs from the switch frequency by Δf, actually in most applications the input signal and reference signal will not arrive at the demodulator exactly in the same phase. We can write these relationships between the input signal and the reference signal:

$$f_{sig} = f_{ref} + Df \quad (2.41)$$

$$w_{sig} = w_{ref} + Dw \quad (2.42)$$

$$w_{ref} = 2\,p\,f_{ref} \quad (2.43)$$

$$Dw = 2\,p\,Df \quad (2.44)$$

$$V_{sig} = V_s\,Sin\,(w_{ref} + Dw)\,t \quad (2.45)$$

$$V_{sig} = V_s\,Sin\,(w_{ref}\,t + j) \quad (2.46)$$

$$where\ j = Dwt \quad [25] \quad (2.47)$$

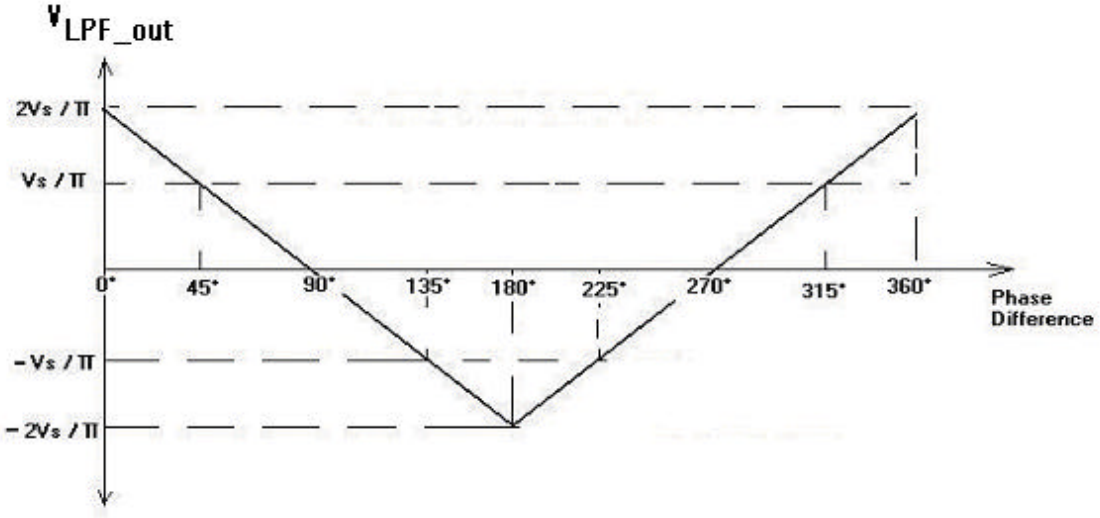

Figure 2.2.5 Representation of the LPF output by phase difference between the input and reference signals

The low pass filter output, V_{lpf_out}, will then be

$$V_{lpf\_out} = \frac{2}{T}\int_0^{T/2} V_S Sin(w_{ref}t + j)dt \qquad (2.48)$$

$$V_{lpf\_out} = \frac{2V_S}{p} Cos\, j \qquad (2.49)$$

$$V_{lpf\_out} = \frac{2V_S}{p} Cos(\Delta wt) \qquad (2.50)$$

The demodulator will respond to any odd multiplies of the reference frequency, but with a lower gain [1], such as the third multiple is equal to 1/3 value of the first multiple or the fifth multiple is equal to 1/5 value of the first multiple and so on. As shown in figure 2.2.7, the low pass filter output will approach zero, if the cut off frequency point, w_o, of the low pass filter is much less than Dw. The low pass filter output will vary with Dw, if w_o is bigger than Dw. For example, the output of the low pass filter is equal to $(2V_s/p)$ for a sinusoidal input signal and a square wave reference signal, and it falls rapidly to zero, depending on bandwidth of the low pass filter. This process repeats itself every odd multiplies of the reference frequency. The low pass filter output is sharply peaked at $w_{in} = w_{ref}$, and any odd multiplies of the reference frequency, such as, $w_{in} = 3w_{ref}$, $5w_{ref}$, $7w_{ref}$, *etc*. By using large time constants, we can get narrower bandwidth for the low pass filter. This process provides more noise rejection in the system.

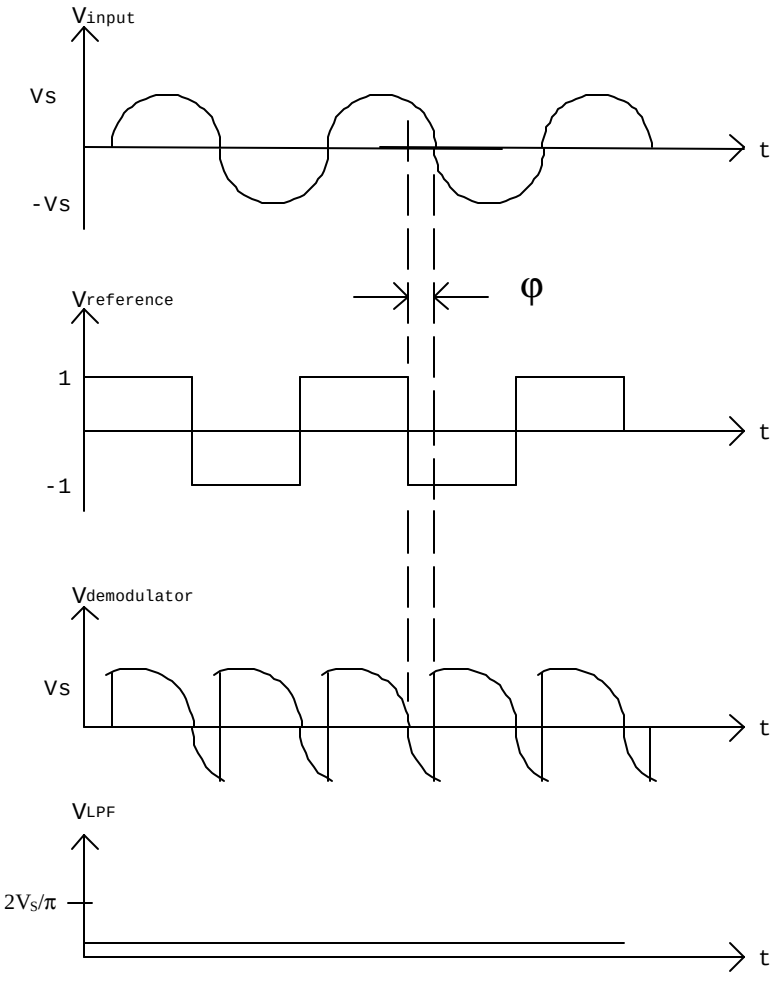

Figure 2.2.6 Demodulator and LPF outputs when they are out of phase

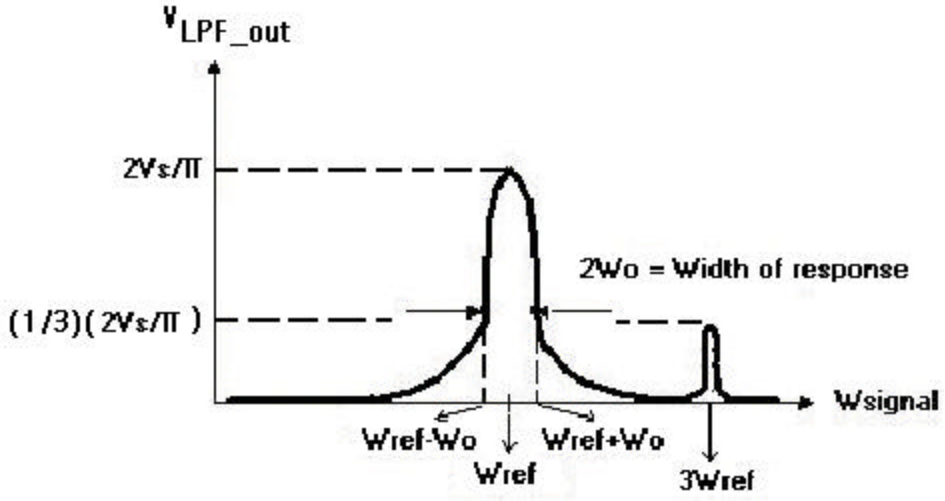

Figure 2.2.7 Odd multiplies of the reference frequency

2.3 Dynamic Reserve

The ability of detection and measurement of very small signals, which are obscured by large noise sources, of the lock-in amplifier is called dynamic reserve [1]. It is a useful performance benchmark for lock-in amplifiers. Dynamic reserve is a measure of the range of input signal amplitudes for which useful output can be obtained from a system. The more traditional definition of dynamic reserve is the maximum ratio between the amplitude of the noise into the bandwidth and amplitude of the signal to be amplified, expressed in dB. For example, if the full scale is 1 μV, then a dynamic reserve of 60 dB means that noise as large as 1 mV can be tolerated at the input without overload [15]. Thus, this implies that, at the dynamic reserve limit, the noise should not cause an overload anywhere in the lock-in amplifier system. By adjusting the distribution of the

input signal to very low amplitude, lock-in amplifiers can achieve high dynamic reserve. In this case, the signal at the demodulator is also very small. To remove the large noise components from the demodulator output, a low pass filter must be used.

2.4 Dynamic Range

If we show maximum allowed input voltage signal by ΔV, and minimum detectable signal (MDS) by S_{min}, input dynamic range will be

$$D_I = DV / S_{min} \; . \qquad (2.51)$$

Chapter 3

Lock-In Amplifier System Blocks

The main idea of this project is to build the detection system. We used a signal generator to produce both the input signal and the reference signal. The detection system of the proposed lock-in amplifier consists of five different stages. Each stage works with "low-voltage strategy". These stages are photodiode, preamplifier, gain, demodulator, and low pass filter stages (figure 3.1). We used two different approaches to build the demodulator. The main idea of doing this is to compare a new approach with the traditional approach.

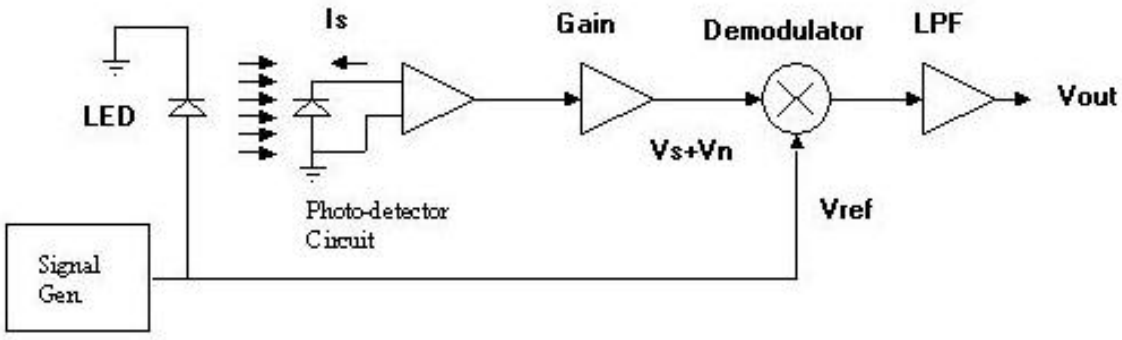

Figure 3.1 System blocks of the lock-in amplifier

3.1 R4BS Operational Amplifier

A fundamental block of the entire low-voltage, low-noise analog lock-in amplifier is the operational amplifier, which is called R4BS operational amplifier. All the amplifier blocks used in the lock-in use this op-amp. Design of an amplifier with desired frequency response is complicated by several factors. First, the frequency response of an operational amplifier corresponds to the frequency response of the open-loop gain and does not include the effects of the feedback network (figure 3.1.1). Second, high frequency compensation is generally required to obtain closed-loop stability for the overall feedback amplifier. Third, the output voltage of the amplifier is limited to some maximum rate of change, called slew-rate, which imposes both frequency and transient response limitations on the overall amplifier [9], [28].

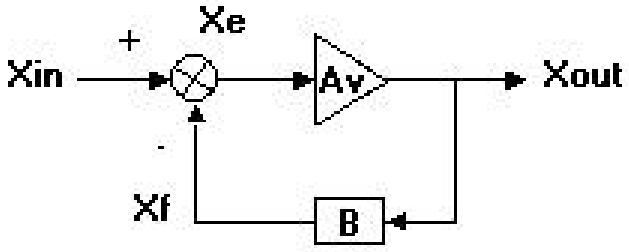

Figure 3.1.1. Block diagram of the negative feedback amplifier

To calculate the open loop gain of negative feedback amplifier, as shown in figure 3.1.1, we need to follow these expressions:

$$Open\_Loop\_Gain = A_{OL} = \frac{X_{out}}{X_e} \tag{3.1}$$

$$Gain\_of\_b\_network = b = \frac{X_f}{X_{out}} \tag{3.2}$$

$$Closed\_Loop\_Gain = Av = \frac{X_{out}}{X_{in}} \tag{3.3}$$

and $X_{in} = X_e + X_f$ (3.4)

$$Av = \frac{A_{OL}X_e}{X_e + X_f} = \frac{A_{OL}X_e}{X_e + (bX_{out})} = \frac{A_{OL}\frac{X_{out}}{A_{OL}}}{\frac{X_{out}}{A_{OL}} + (bX_{out})}$$

$$Av = \frac{A_{OL}X_{out}}{X_{out} + (bX_{out}A_{OL})} = \frac{A_{OL}X_{out}}{X_{out}(1 + bA_{OL})}$$

$$Av = \frac{A_{OL}}{1 + A_{OL}b}$$

$$Av = \frac{A_{OL}}{1 + T} \tag{3.5}$$

where, $(A_{OL} \times b)$ *is called loop gain,T.*

If $1/b = A_{ideal}$, (3.6)

$$Av = \frac{A_{OL}}{(1+T)}\frac{b}{b} = \frac{A_{OL}b}{(1+T)}\frac{1}{b}$$

$$Av = A_{ideal}\frac{T}{1+T}$$

$$Av = A_{ideal}\frac{1}{1+\frac{1}{T}} \tag{3.7}$$

The sign of T is always negative in a negative feedback amplifier. The loop gain T has no units. The operational amplifier can reach large 108 dB open loop gain (figure 3.1.2) with 11 MHz gain bandwidth. The fundamental reason for designing an amplifier with a very large open loop gain is the flexibility. It provides for the design of amplifiers with an arbitrary gain. Slew rate of the op-amp is 15 V/µs, which means that to complete a 15 V output swing, the R4BS op-amp needs approximately 1 µs (figure 3.1.3). Total noise output highly dependent on flicker noise effects up to 1 kHz (figure 3.1.4). Equivalent input noise starts to increase after 100 MHz frequency point (figure 3.1.5). Table 3.1 summarizes the general characteristics of the R4BS op-amp. We applied ± 2.5 V supply voltage to the op-amp during the experiment. One of the main advantages of this op-amp is its small size.

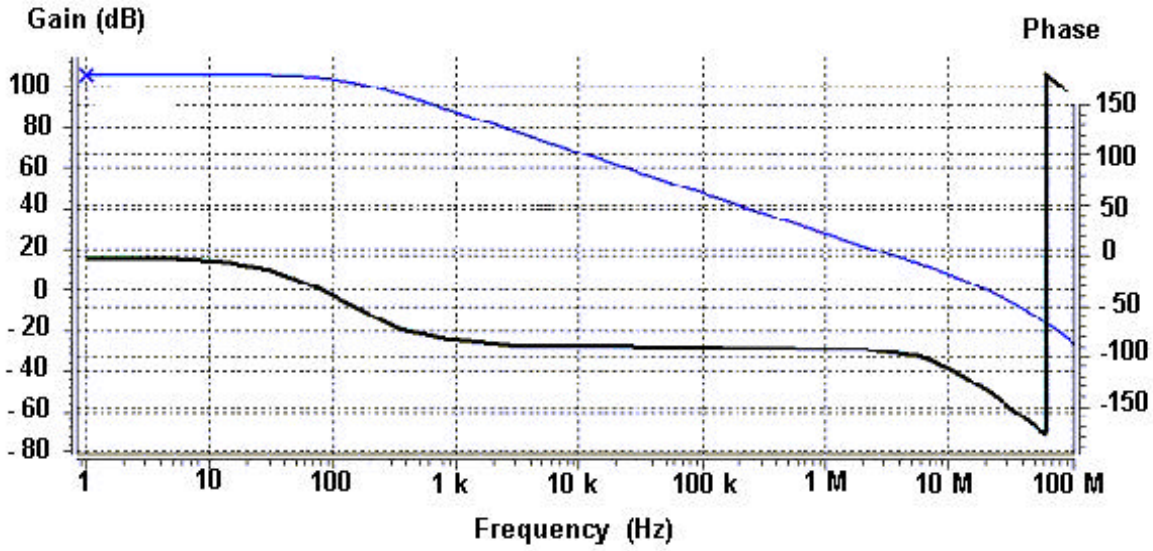

Figure 3.1.2 Open-loop gain and phase response of the op-amp

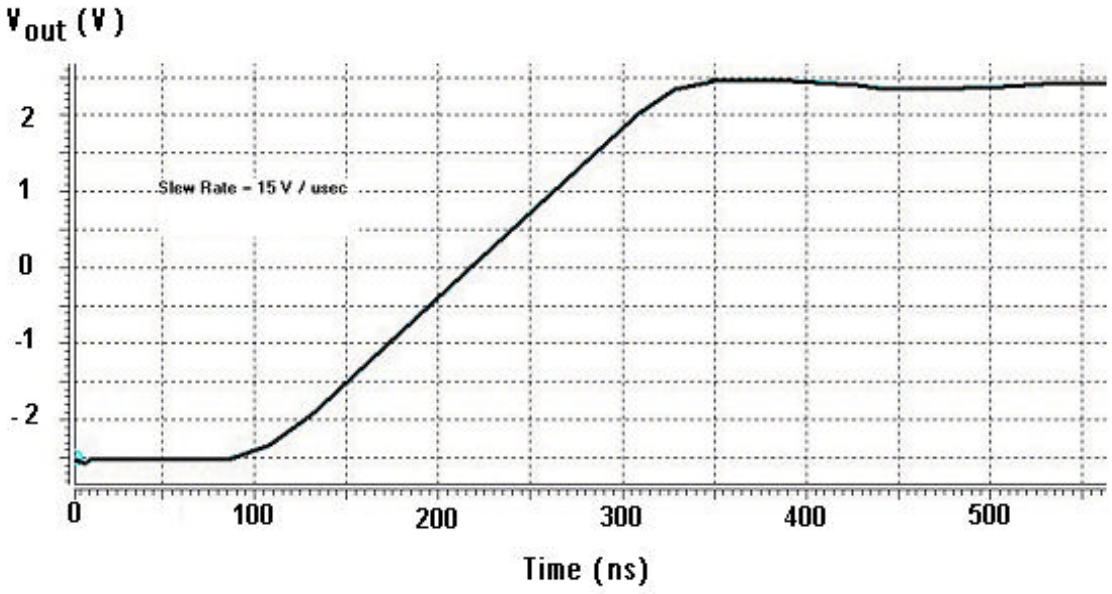

Figure 3.1.3. Slew rate of the op-amp

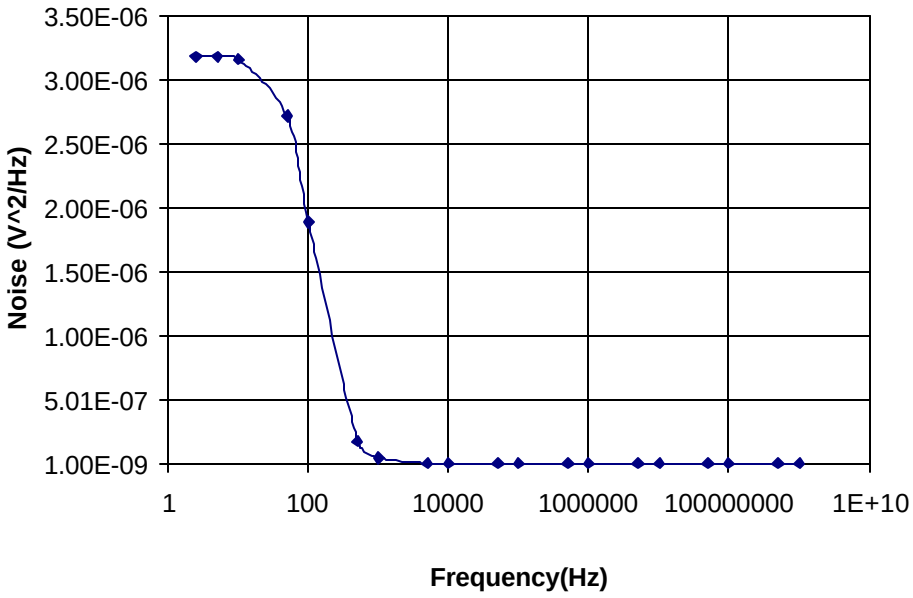

Figure 3.1.4 Total noise output voltage for the op-amp

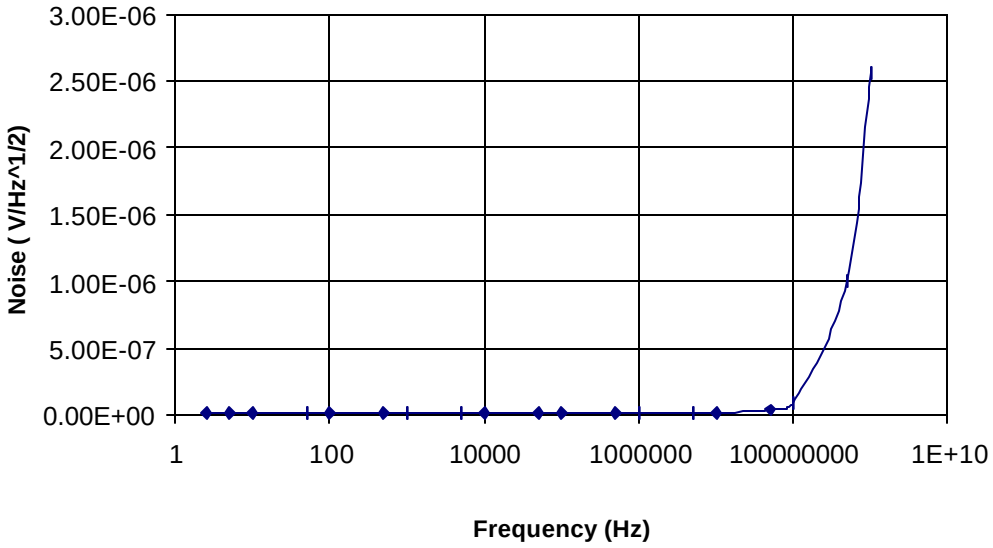

Figure 3.1.5 Equivalent input noise of the op-amp

Table 3.1 General characteristics of the R4BS Op-Amp

Gain	108 dB
Gain Bandwidth (GBW)	11 MHz
Phase Margin (PM)	50°
Slew Rate (SR)	15 V/μs
Supply Voltage	± 2.5 V
Input Offset Voltage	~ 1mV
Total Area Inside of the Chip	208.8 μm x 630.4 μm = 0.1316 mm^2

3.2 Photodiode

Photodiodes are used in a variety of applications where one needs to detect light or measure its intensity. While there are many ways to implement a photodiode, a p-n junction is one of the simplest structures (figure 3.2.1). Photodiodes made of Silicon (Si) are mainly used in consumer electronics. When a photodiode is reversed-biased and under dark conditions, very little current flows through it. This is termed the dark current. However, when a semiconductor is illuminated by light having energy greater than its band-gap energy, the light is absorbed in the semiconductor and electron-hole pairs are generated. The electrons migrate towards the "n" type silicon layer, while holes migrate toward the "p" type layer. It results in a small electrical current, which is proportional to the number of photons absorbed [11].

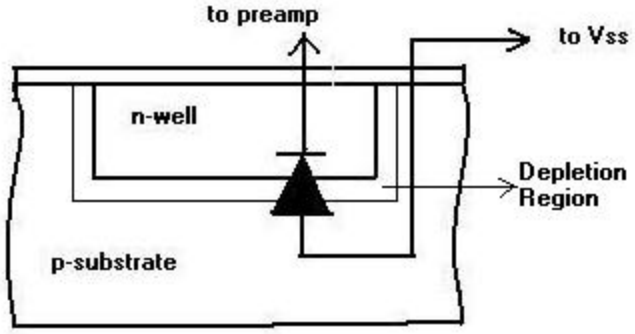

Figure 3.2.1 n-well / p-substrate photodiode

The top layer of the photodiode is very thin. Silicon becomes depleted of electrical charges near the p-n junction. This is known as the depletion region. Applying a reverse bias voltage across the junction will vary the depth of the depletion region. Some optical detection applications the photodiode's speed of response is critical. For example, if the photodiode is to respond to a series of light pulses *1ns (f = 1GHz)* apart, the photo generated minority carriers must diffuse to the junction and be swept across to the other side in a time much less than *1 ns (f = 1 GHz)*. In this application, the lock-in amplifier system needs to work up to *100 ms (f = 10 kHz)* apart, therefore most any photodiode has enough time to respond for our experiment at this speed.

An n-well / p-substrate 640 µm x 640 µm photodiode is used to detect fluorescent photons. The technology is AMI 1.5 µm CMOS process. Since the n-well / p-substrate diode collects the charge created deeper in silicon and has a spectral response that peaks at ~750 nm versus the p-diffusion / n-well that peaks at ~500 nm, an n-well / p-substrate photodiode would respond better to signals toward the red end of the visible spectrum [5], [30].

Responsivity is a measure of output current for a given light power launched into the diode. Spectral responsivity is the response that is achieved as a function of the wavelength. The measure of sensitivity is the ratio of radiant energy (in watts) incident on the photodiode to the photocurrent output in amperes. It is expressed as the absolute responsivity in amps per watt. Radiant energy is usually expressed as *watts/cm*^{2} and the photodiode current as *amps/cm*^{2}. The *cm*^{2} terms cancel each others and we are left with *amps/watt (A/W)*. A typical responsivity curve, which shows *A/W* as a function of wavelength, is given in figure 3.2.2 for n-well / p-substrate photodiode [40].

The noise in photodiodes is shot noise and Johnson noise and often limits the performance of the systems. The shot noise is the essential noise in photodiodes and is induced by the behavior of the photo-induced carriers and incident photons as particles. The Johnson noise is generated in the resistance connected to the photodiode and is caused by the random motion of carriers in the resistance.

The output current of photodiodes is typically a very low. As a result, the signal can be lost at the receiver connection between photodiode and the other stages. Using low-noise pre-amplification into the same circuit provide better signal-to-noise ratio.

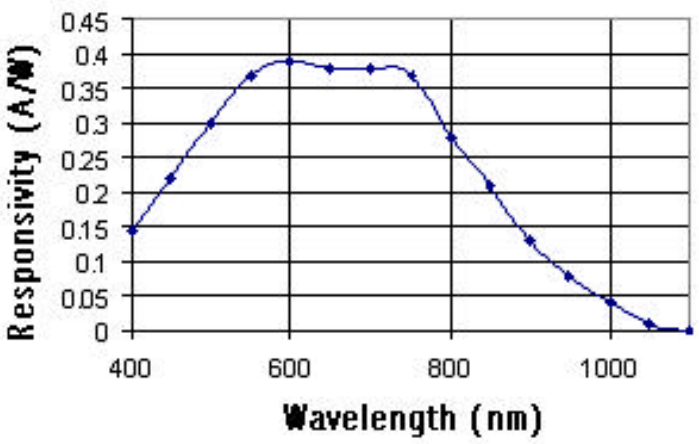

Figure 3.2.2 Typical responsivity curve for n-well / p-substrate photodiode [4]

3.3 Preamplifier stage

To pre-process the input signal, the photodiode is connected to the pre-amplifier before going to the demodulator. The pre-amplifier has a transimpedance configuration, which means our light source comes to photodiode output as a current source, while output of the pre-amplifier is voltage source. We can find the dc gain of the pre-amplifier circuit by dividing its input current to its output voltage

$$A_{dc} = V_o / I_S = R_f . \qquad (3.8)$$

To provide a 350 kV/A transimpedance dc gain across the pre-amplifier, the 350 kΩ feedback resistor should be connected to the pre-amplifier as shown in figure 3.3.1.

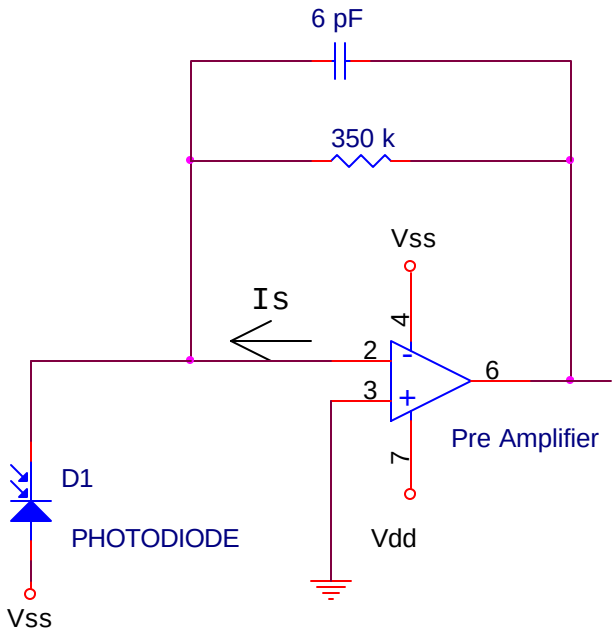

Figure 3.3.1 Photodiode and the pre-amplifier stage

The loop transmission for the pre-amplifier is

$$T = -A_{OL}\frac{1+ j\frac{f}{f_1}}{1+ j\frac{f}{f_2}} \qquad (3.9)$$

where

$$f_1 = \frac{1}{2pR_1C_1} \qquad (3.10)$$

and

$$f_2 = \frac{1}{2pR_1(C_D + C_1)} \qquad (3.11)$$

C_1 represent the feedback capacitance in parallel to R_1 (figure 3.3.1). The reason for adding 6 pF feedback capacitance for frequency compensation is to prevent oscillation or gain peaking in the circuit both as a result of an HSPICE transient analysis and the laboratory experiment. C_D represents the n-well / p-substrate junction capacitance in farads. It depends on the thickness of variable depletion region. Increasing the bias voltage increases the depth of depletion region and lowers the C_D value [4]. The ideal transfer function, V_o / I_S, for the detection circuit is

$$T = R_1\frac{1}{1+ j\frac{f}{f_1}} \qquad (3.12)$$

where

$$f_1 = \frac{1}{2pR_1C_1} \qquad (3.13)$$

-3 dB bandwidth of the pre-amplifier is 75.8 kHz by using 350 kΩ resistors and 6-pF capacitance. Although using smaller capacitance can increase this bandwidth, it leads to oscillation in the lock-in amplifier.

Noise is an area of concern for low-level signal detection [9]. The photodiode in figure 3.3.1 responds to incident light with a current I_S that the op-amp subsequently converts to a voltage V_o. To reduce noise, another capacitor can be added in parallel with R; however, this also reduces the signal-gain bandwidth. The optimum situation requires reduction of the bandwidth as much as possible without degrading the signal response.

3.4 Gain stage

Amplification or gain occurs in a device when the output is greater than the input. Gain is defined as the output divided by the input. A gain amplifier stage is often an essential step for best system sensitivity. Without a gain stage, the result can be distorted. These seriously degrade system performance. For this reason, a simple x100 inverting gain stage is used (figure 3.4.1) whose transfer function is expressed as,

$$Av = R_2 / R_1 = 100 \ . \qquad (3.14)$$

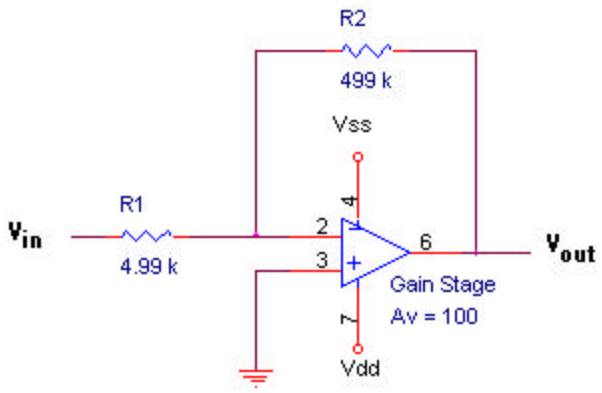

Figure 3.4.1 x100 voltage gain stage

A practical op-amp has non-ideal characteristics. For example, transistors, making up the op-amp, never have exactly similar characteristics. This situation is same for the input transistors of the op-amp. Because of this reason, op-amp acts like it has an extra small voltage source, and thus it may have a non-zero small output voltage. This input voltage is called the input offset voltage. If the gain of the circuit is large, the output voltage due to the input offset voltage will be large. R4BS op-amp has around 1 mV input offset voltage. This input offset voltage will be very large after the gain stage. So, it is necessary to make an input offset adjustment in the gain stage (figure 3.4.2). To explain this input offset voltage, we can write below expressions according to figure 3.4.2. Here, Maxim OP-27 operational amplifier was used.

According to figure 3.4.2 we can write

$$I = (V_{in}-V_{inn}) / R_1 \qquad (3.15)$$

$$V_{out} = V_{inn} - IR_2 \, . \qquad (3.16)$$

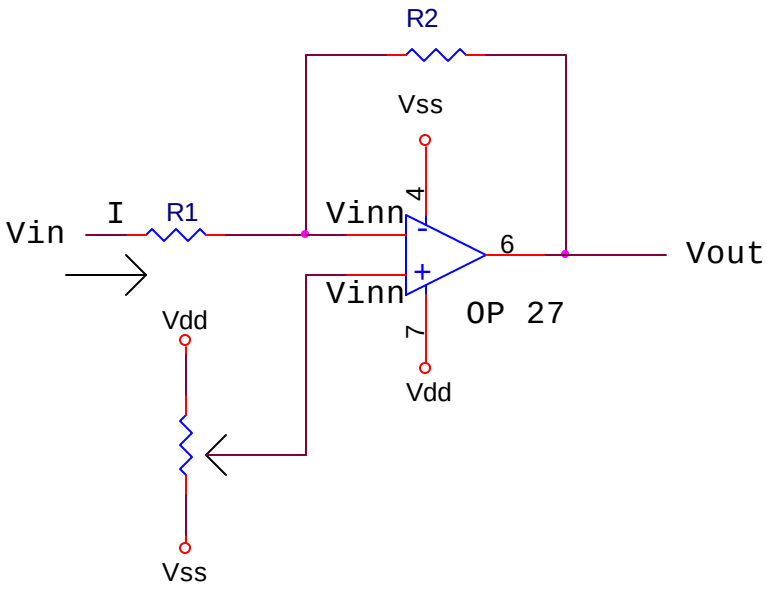

Figure 3.4.2 Input offset adjustment

Substituting (3.15) and (3.16)

$$V_{out} = V_{inn} - (R_2 / R_1)(V_{in} - V_{inn}) \qquad (3.17)$$

$$= 2V_{inn} - V_{in} \qquad (3.18)$$

where $R_1 = R_2$.

Since desired output signal, V_{out}, must be equal to $-V_{in}$, $(V_{out} = -V_{in})$ the value of $2V_{inn}$ is equal the offset voltage of op-amp. $2V_{inn}$ can be easily adjusted to zero by using variable resistor. Figure 3.4.3 shows the gain and phase response of the x100 voltage gain amplifier stage. The results were summarized in table 3.4.

Table 3.4 Gain stage general characteristics

Gain	100
Gain Bandwidth (GBW)	30 MHz
Phase Margin (PM)	140°

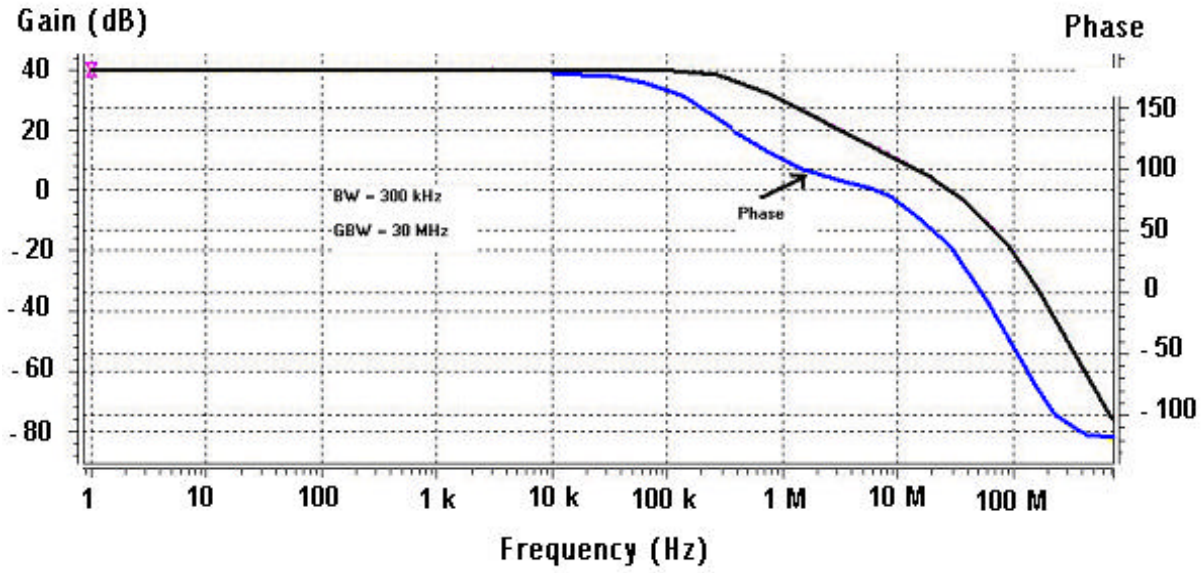

Figure 3.4.3 Gain amplifier phase and gain response

3.5 Low pass filter stage

The low pass filter (figure 3.5.1) provided with the majority of lock-in amplifiers is based on low cut-off frequency. A low pass filter is effective in suppressing noise at frequencies beyond cut-off. A filter is a circuit that processes signals on a frequency dependent basis. The manner in which its behavior varies with frequency is called the frequency response and is expressed in terms of the transfer function $H(jw)$, where $w = 2pf$ is the angular frequency in radians per second (rad / s).

The low-pass filter response is characterized by a frequency ω_0, called the cut-off frequency such that $|H(jw)| = 1$ for $(w < w_0)$ and $|H(jw)| = 0$ for $(w >> w_0)$ (except for ideal low pass filter), indicating that input signals with frequency less than ω_0 go through the filter with unchanged amplitude while signals $\omega > \omega_0$ undergo complete attenuation. A common example of the low pass filter application is the removal of high frequency noise from a signal.

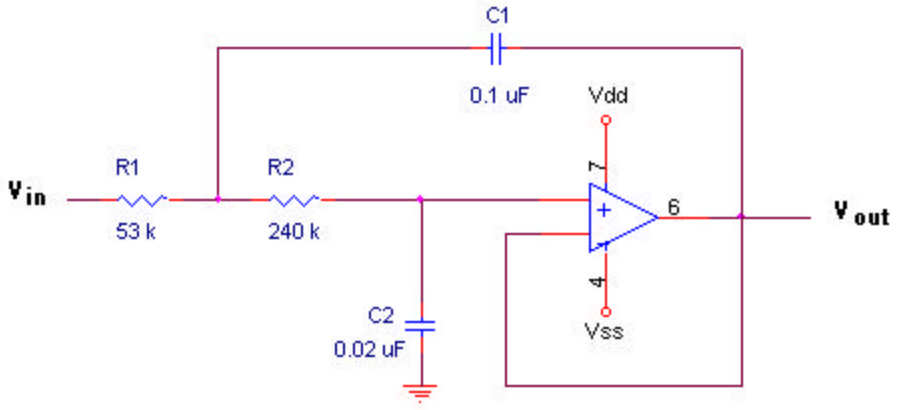

Figure 3.5.1 The Sallen and Key low pass filter stage

A Sallen and Key basic two-pole low pass filter (figure 3.5.1) was used in this lock-in amplifier project. Cut-off frequency of a Sallen and Key low pass filter is

$$w_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} = \frac{1}{\sqrt{53k\,240k\,0.02m\,0.1m}} = 198.6 rad/s \Rightarrow \quad (3.19)$$

$$f_0 = \frac{w_0}{2p} = 31.6 Hz \quad (3.20)$$

This is also shown in an HSPICE frequency analysis plot (figure 3.5.2).

The quality factor, Q, is

$$Q = \sqrt{\frac{C_1}{C_2}}\frac{\sqrt{R_1 R_2}}{R_1 + R_2} = \sqrt{\frac{0.1m}{0.02m}}\frac{\sqrt{53k\,240k}}{293k} = 0.86 \quad (3.21)$$

The Q of a filter is related to the overshoot and ringing in the transient response of the filter, and to the peaking of the frequency response: a high-Q circuit will display more peaking, or overshoot, than a low-Q circuit. In this experiment we have $f_0 = 31.6$ *Hz and* $Q = 0.86$

Although Q must be equal to 0.71 for best result [9], [28] we obtained Q equal to 0.86, due to necessity of using off-chip capacitors and resistors. If we inspect the figure 3.5.2, there is a little overshoot around at 20 Hz. This is the effect of quality factor, Q. When Q is 0.71 or ($1/\sqrt{2}$), the bandwidth response is smooth curve. Smooth curve will give us much more phase margin, less ringing and more stable circuit without oscillation. Its cut-off frequency and quality factor (Q) can be easily adjusted by varying the RC components. Table 3.5 summarizes the results of the low pass filter.

Table 3.5 General characteristics of the low-pass filter

Gain Bandwidth (GBW)	31.6 Hz
Phase Margin (PM)	100°

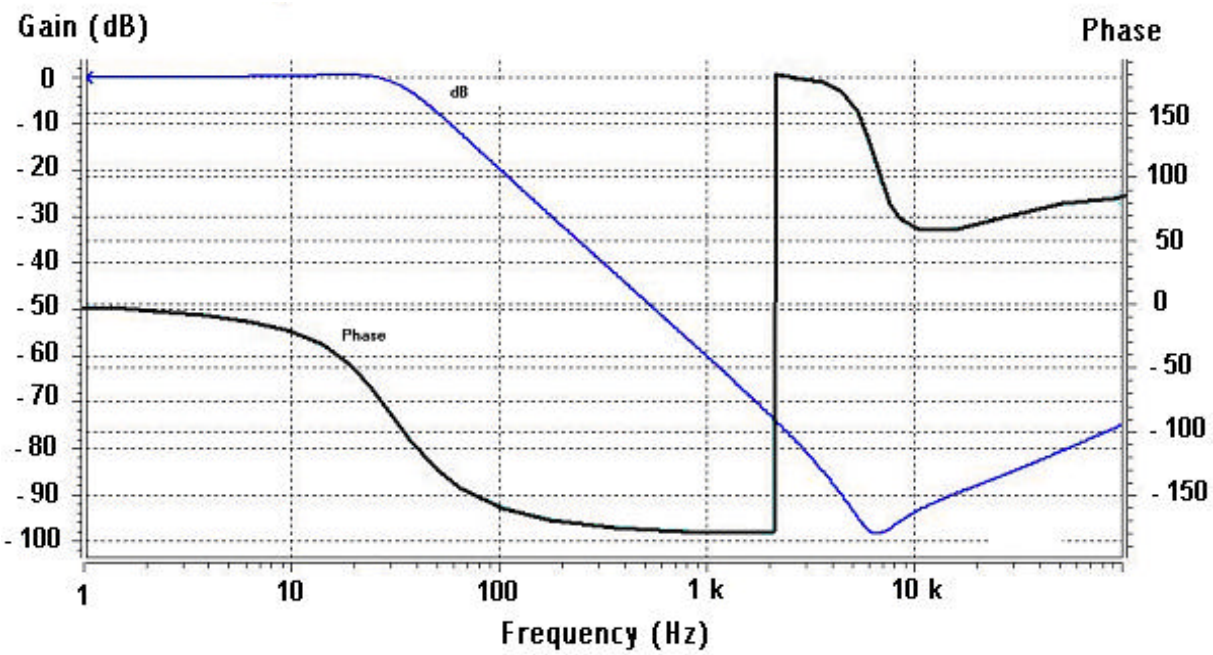

Figure 3.5.2 Low Pass Filter Gain and Phase response

3.6 Demodulator 1

Switched gain amplifier is the most important block of this demodulator. The switching operation occurs by complementary transmission gates (CMOS switch). In order to switch the control between the two transmission gates, a CMOS inverter has been utilized (Figure 3.6.1). Implementations of the CMOS switches for this demodulator shown in figure 3.6.2. Switching multipliers as a synchronous demodulator have wide dynamic range, high degree of precision, in addition to operational simplicity [2].

In this application, when first switch is 'on' and second switch is 'off', op-amp acts as non-inverting x1 gain amplifier. When second switch is on and first switch is off, it acts as inverting x1 gain amplifier. If we inspect the figure 3.6.3, the demodulator output is equal to full wave rectifying signal of the input signal. When V_{ref} is logic 1, first switch is 'off' and second switch is 'on'. V_{out} is equal to x1 gain of V_{in}. When V_{ref} is logic 0, first switch is 'on' and second switch is 'off'. V_{out} is equal to x1 inverting gain of V_{in}. Figure 3.6.3 shows the input and output voltage HSPICE simulation results by controlling the reference voltage. Figure 3.6.4 shows the zoomed in output response of these signals.

The important point of this demodulator is to get equal smooth bandwidth response during 'on' positions for both first and second switches. Figure 3.6.5 shows the frequency responses of amplifier during both positions.

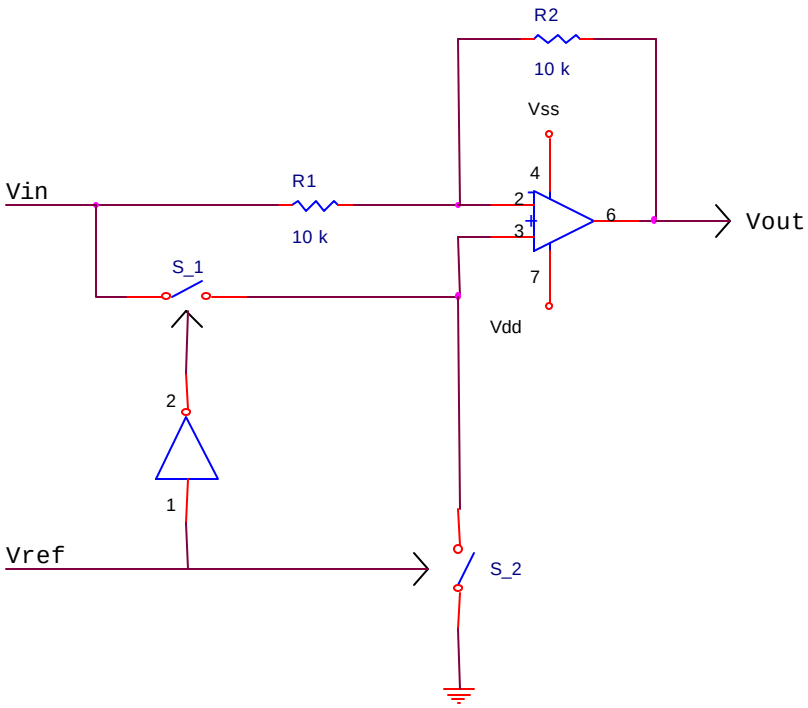

Figure 3.6.1 Representation of the demodulator_ 1

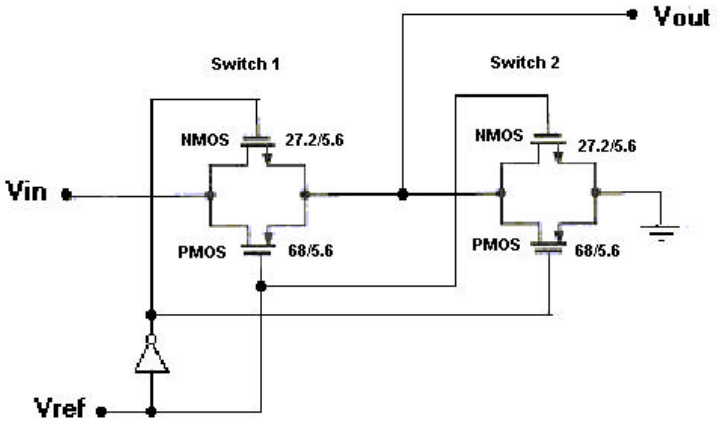

Figure 3.6.2 Implementations of the CMOS switches for demodulator_ 1

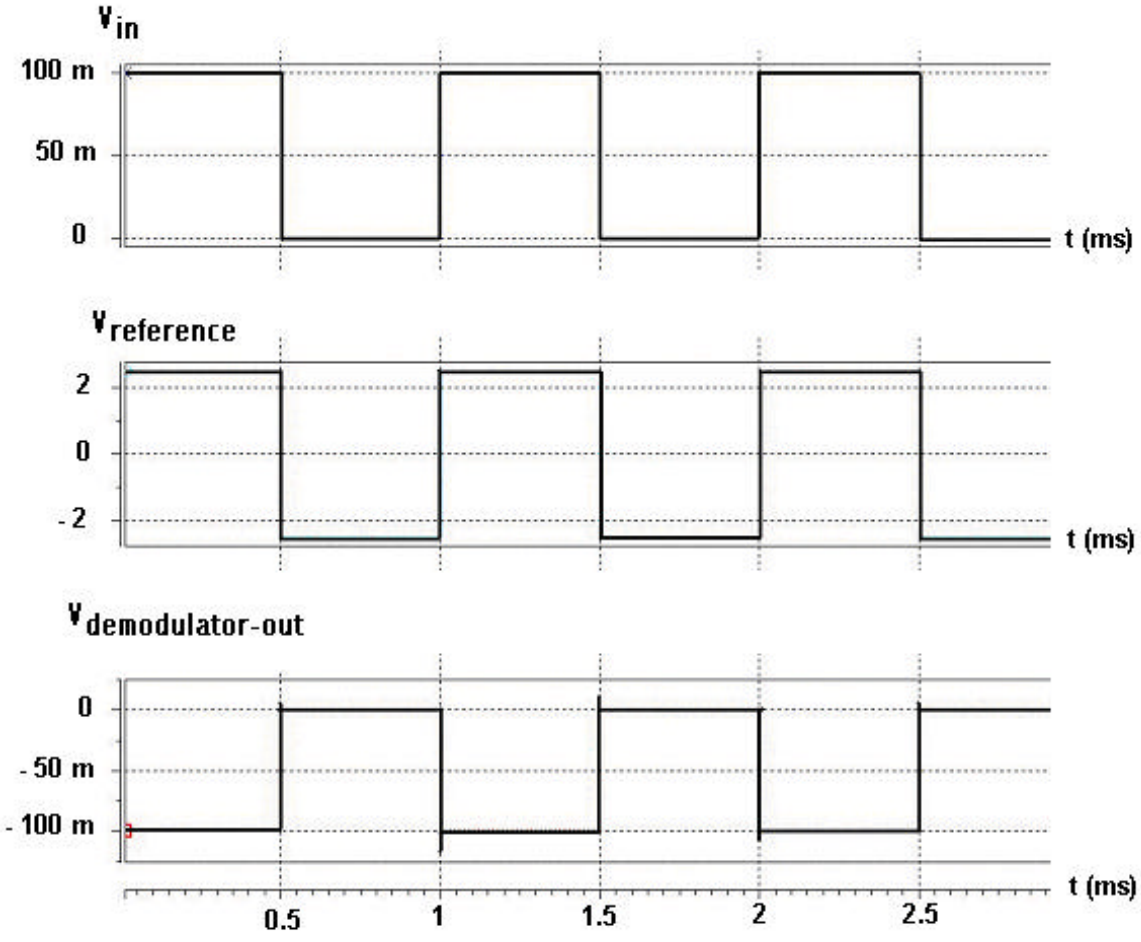

Figure 3.6.3 Input and output signals of the demodulator_1 by switching operation

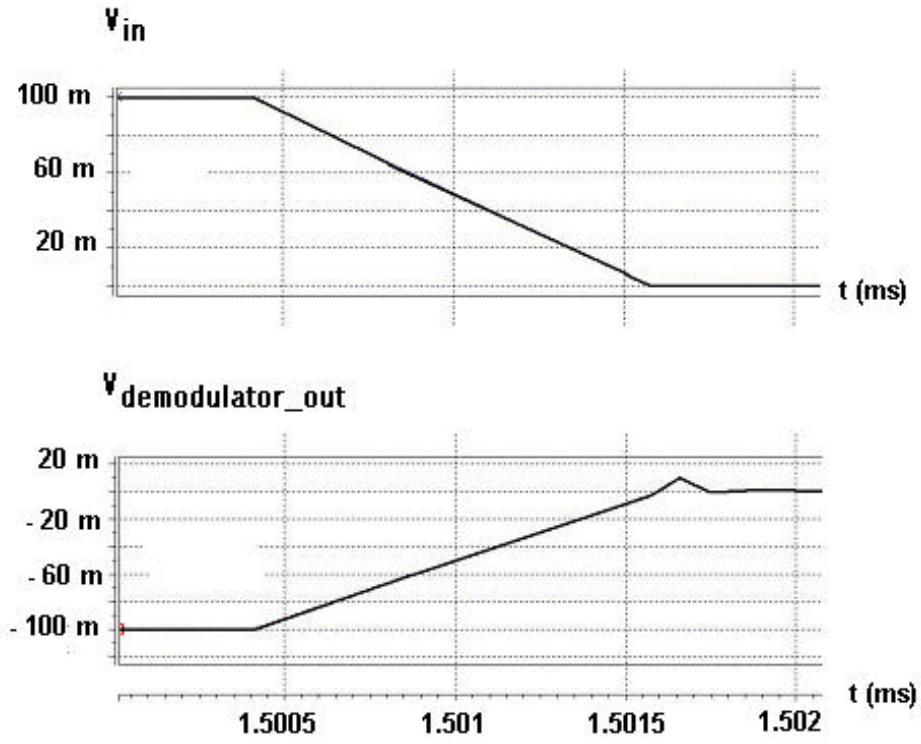

Figure 3.6.4 Zoomed in input and output signals of the demodulator_1

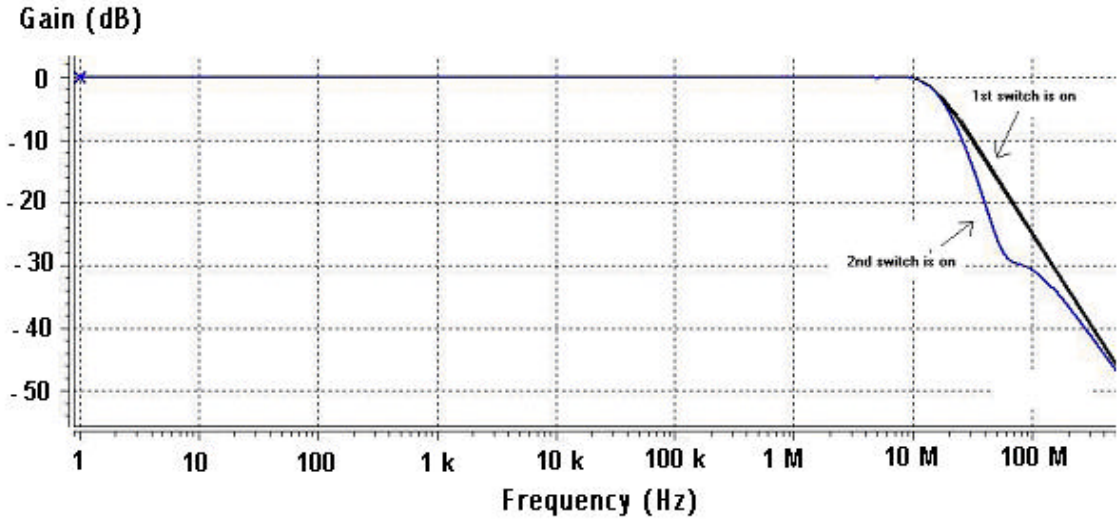

Figure 3.6.5 Gain responses of the amplifier during switching

3.7 Demodulator 2

This demodulator has a unity gain amplifier, an inverting x1 gain amplifier, a CMOS transmission gate, and another unity gain amplifier to buffer output of first and second amplifiers (Figure 3.7.1). This kind of demodulator can be considered the traditional way of full wave signal rectification [1]. In this demodulator, the signal spends equal times in its two states. While the first op-amp multiplies the input signal by (+1) gain, the second op-amp multiplies it by (–1) gain. So, the first op-amp is proportional to V_{in} while the second one is proportional to $-V_{in}$, or V_{in_inv}. Since V_{ref} and V_{in} are on same phase and frequency, switching times exactly the same when V_{in} goes from positive side to negative side and vice versa. For a good explanation, we need to look at figures 3.7.2, 3.7.3 and 3.7.4. When V_{in} and V_{ref} are positive, the first switch is 'off' and the second switch is 'on', V_{out} is equal to V_{in_inv}. When V_{in} is zero or negative value (in this experiment photodiode output is always between zero and any positive value) and also V_{ref} is negative, the second switch turns off while the first switch is 'on'. Hence, V_{out} is equal to the second op-amp output, V_{in}. As a result, the demodulator output is a full wave rectified version of the input signal. The reference voltage controls the two states of the switches. This is the key point for the demodulator. The switch changes position as the reference voltage changes polarity. This action gives a systematic change of gain between (+1) and (–1) in the signal path, and therefore causes full-wave rectification of the signal at the switch output. The output of the switch is then applied to the low pass filter, which smoother out the ripple component and delivers a dc voltage which is proportional to the amplitude of the input signal.

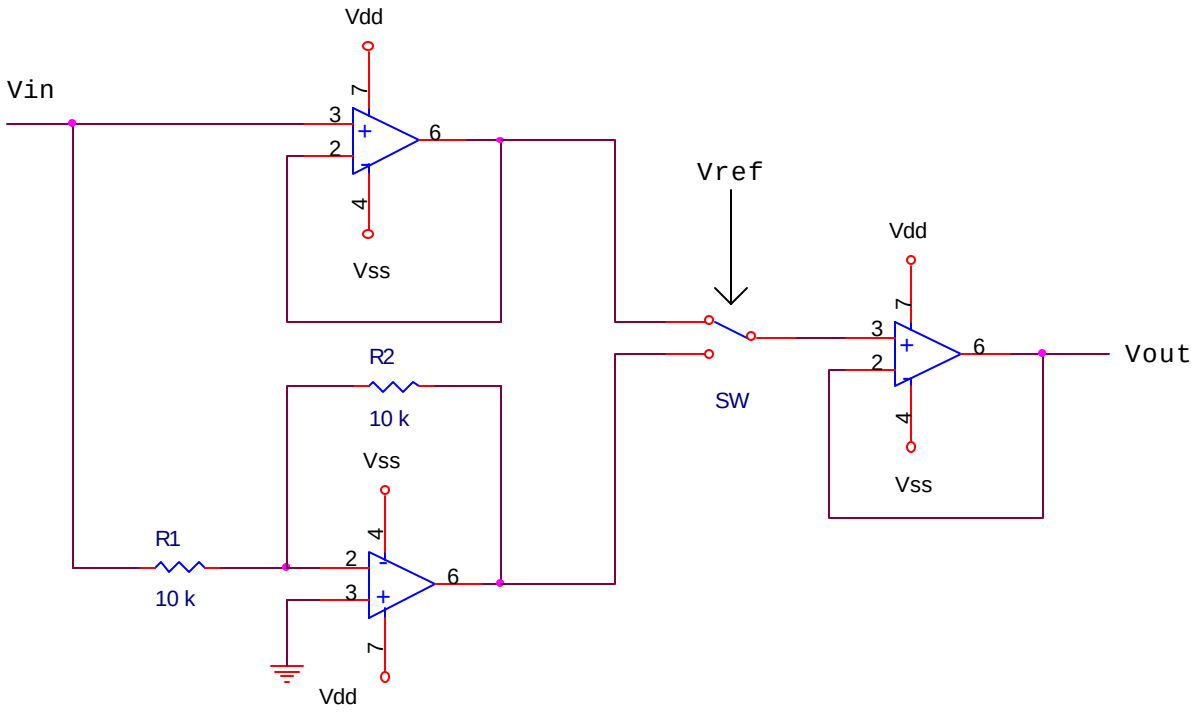

Figure 3.7.1 Representation of the demodulator_ 2

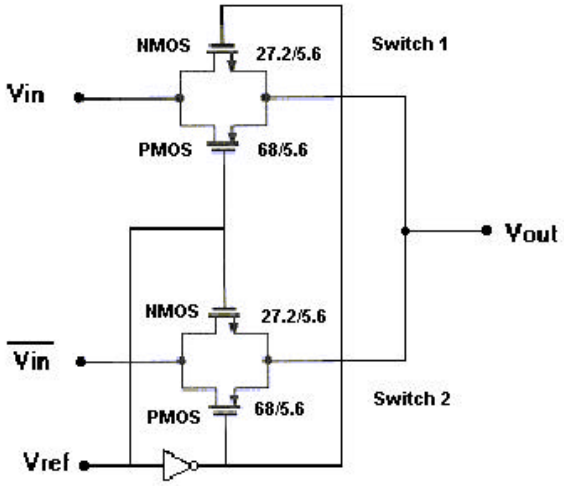

Figure 3.7.2 Implementations of the CMOS switches for demodulator_2

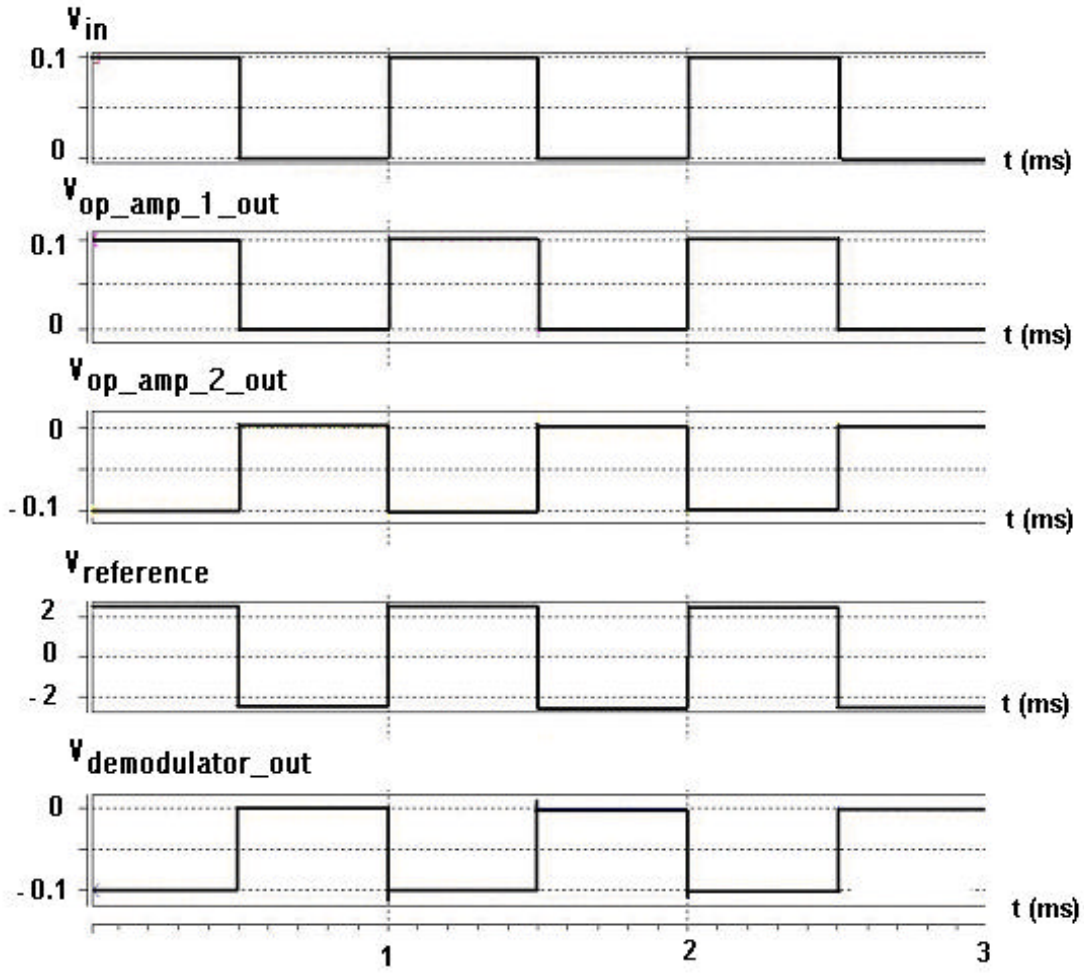

Figure 3.7.3 Input and output signals of the demodulator_2 by switching operation

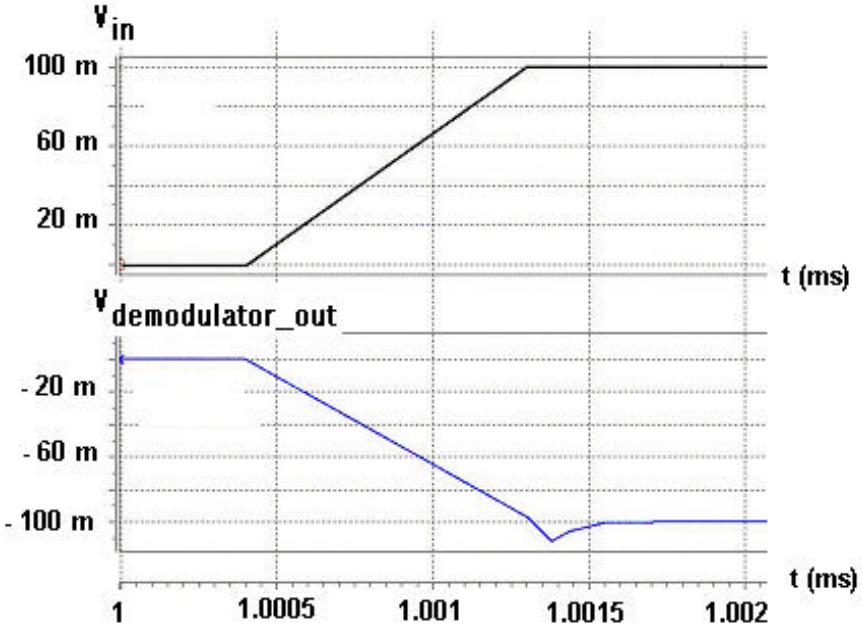

Figure 3.7.4 Zoomed in input and output signals of the demodulator_ 2

When the first amplifier is active and the second one is non-active or vice versa situation leads the non-equality frequency response between the amplifiers. The first amplifier gain bandwidth response has some overshoot around 12 MHz before the compensation (figure 3.7.5). Since both amplifiers have different closed loop response by depending on switch positions, compensation is necessary for preventing overshoot and ringing as a reason of less phase margin. To reduce this overshoot, we need to use larger compensation capacitor inside of the op-amp. Figure 3.7.6 shows both amplifier gain responses after compensation.

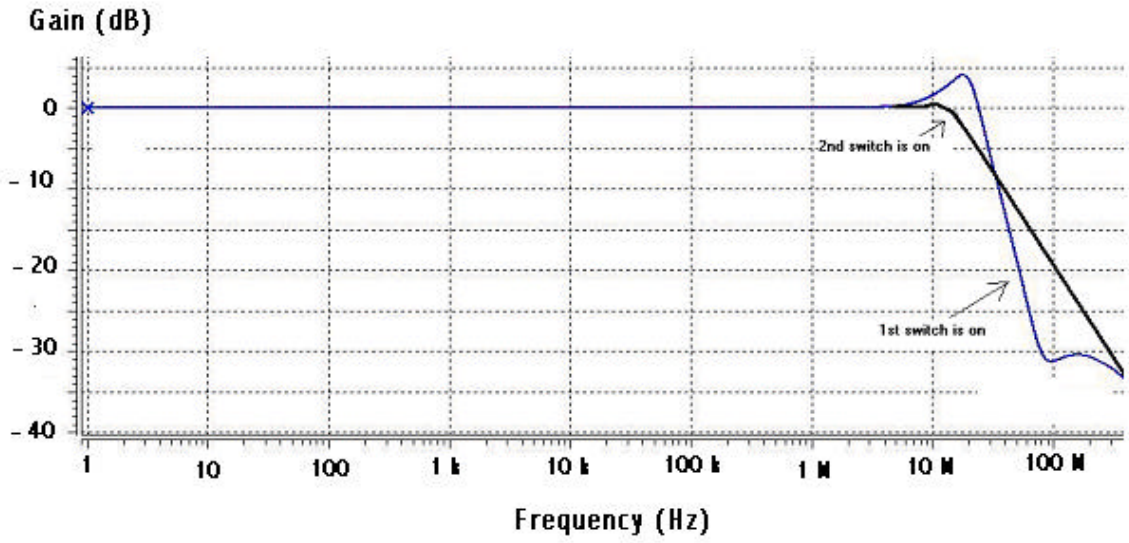

Figure 3.7.5 Gain responses of amplifiers during switching before compensation

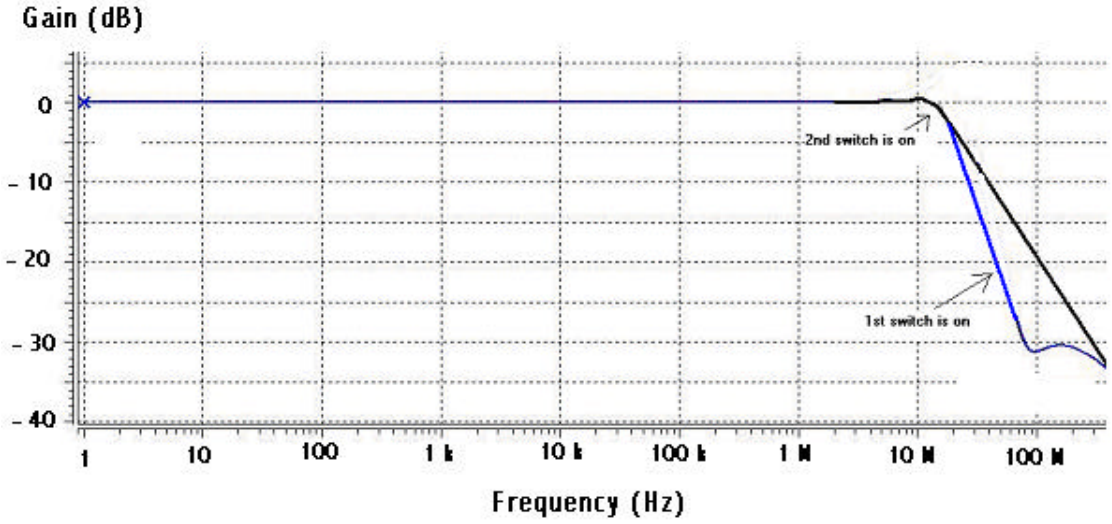

Figure 3.7.6 Gain Bandwidth responses of amplifier during switching after compensation

3.8 CMOS inverter

CMOS technology uses n-channel and p-channel MOSFETs in complementary pairs. In the CMOS inverter, the source of the PMOS is connected to V_{dd}, the source of the NMOS is connected to V_{ss}, and the drain terminals of two MOSFETs are connected together to form the output node (figure 3.8.1). Also, the substrates of both the NMOS and PMOS transistors are connected to their respective sources, thus eliminating body effect in both devices [8]. The circuit is designed so that there will never be a conducting path between in positive and negative power supplies under steady state conditions. When the NMOS is on, the PMOS is off or the PMOS is on, the NMOS is off. (table 3.8 and figure 3.8.2)

Let us consider an input of

$V_{in} = V_{ss} = -2.5\ V.$ *(3.22)*

For the NMOS, $V_{in} + V_{gs} = V_{ss} = -2.5$

$V_{gs} = 0$ *and* $V_{gs} < V_{tn}$ and NMOS is operating in cut-off region.

The PMOS has $V_{dd} = V_{in} + V_{sg} = 2.5\ V$ *(3.23)*

$V_{sd} < V_{sg} + V_{tp}$ and PMOS is operating in linear region (point A in figure 3.8.3).

If $V_{in} = V_{dd} = +2.5$ V,

for the NMOS, $V_{in} + V_{sg} = V_{ss} = -2.5\ V$ therefore, $V_{ds} < V_{gs} - V_{tn}$ and NMOS is operating in the linear region. For the PMOS, $V_{dd} = V_{in} + V_{sg}$ and $V_{sg} = 0$, it means that $V_{sg} < -V_{tp}$ and PMOS is operating in cut-off region (point E in figure 3.8.3).

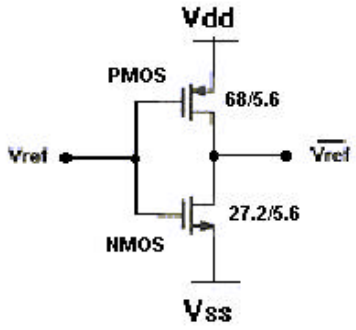

Figure 3.8.1Schematic of the CMOS inverter

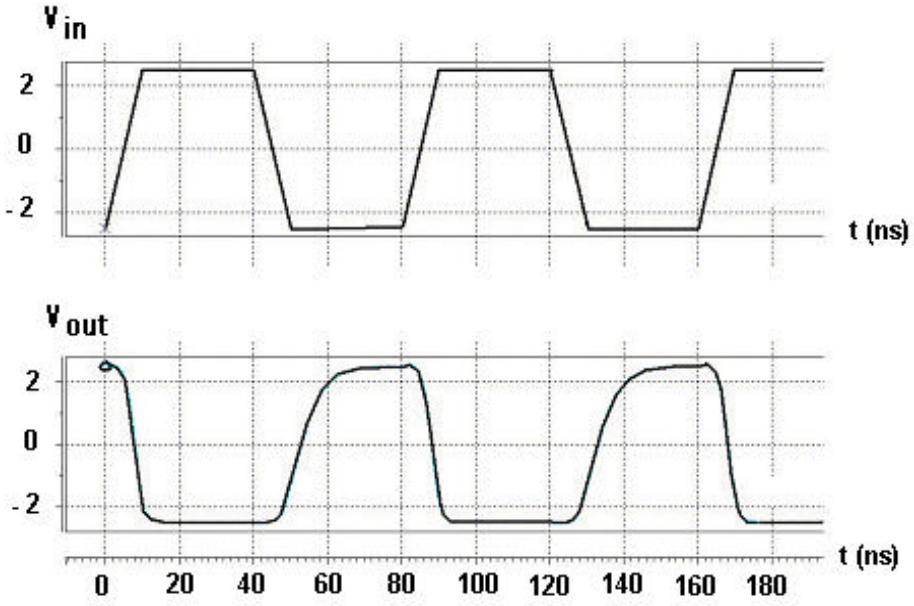

Figure 3.8.2 HSPICE characteristics of the CMOS inverter

Table 3.8 States of the inverter

Input	Output
-1	1
1	-1

For intermediate voltage inputs when the input reaches $V_{in} = V_{tn}$ NMOS turns on and operates in saturation region while PMOS is operating in the linear region (point B in figure 3.8.3).

As V_{in} increases above V_{tn}, the output voltage begins to reduce. When V_{ds} drops below $V_{gs} - V_{tn}$, NMOS enters the linear region of operation. When the output drops to $-V_{tp}$ below the input ($V_{sd} \geq V_{sg} + V_{tp}$ and V_{tp} is negative), PMOS operates in the saturation mode (point D in figure 3.8.3).

For $V_{in} = V_{out} = V_c$, both PMOS and NMOS are in the saturation region of operation (Point C in figure 3.8.3) [36].

3.9 CMOS switch

Figure 3.9.1 displays CMOS bi-directional transmission gate or CMOS switch. This is accomplished by controlling the gates of an NMOS and a PMOS device with complimentary clocks so that the two devices turn on and off simultaneously. Source and drain terminals of MOSFETs are connected in parallel and gate terminals driven by opposite signals indicated by V_{ref} and V_{ref_inv}.

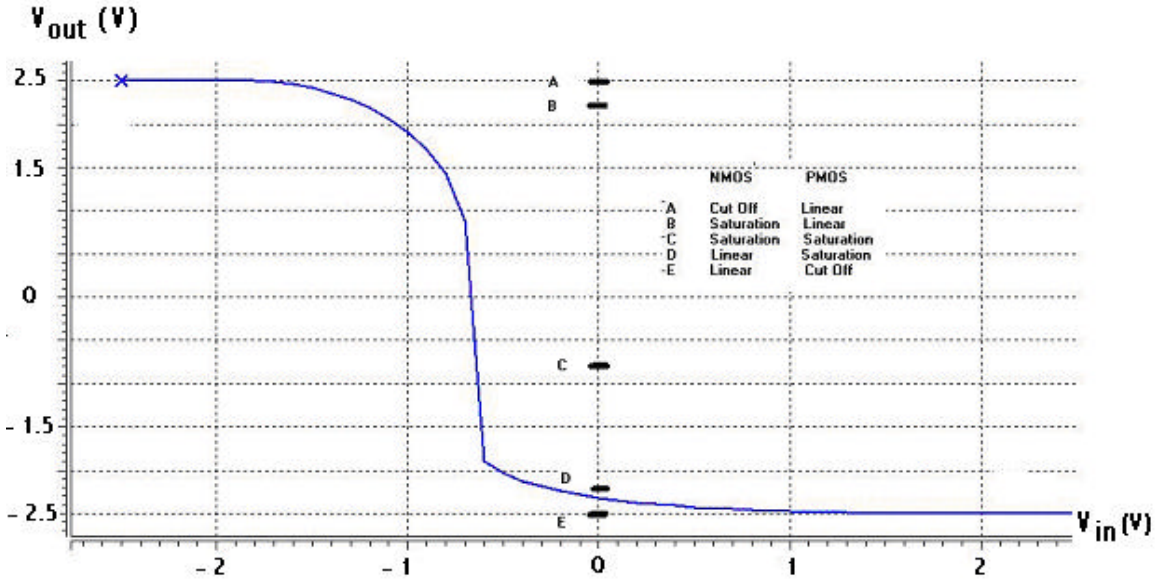

Figure 3.8.3 Voltage transfer characteristics of the CMOS inverter

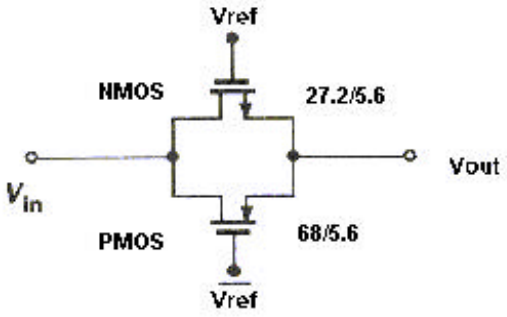

Figure 3.9.1 Schematic of the CMOS switch

In order to enable CMOS switch through the NMOS, V_{ref} must be high so that the NMOS gate voltage is positive with respect the source. Conversely, V_{ref_inv} must be low so that the gate terminal of PMOS is negative with respect its source and the PMOS is enabled.

When the transmission gate is in the conducting state V_{ref} is logic 1. The input and output terminals are connected together through the parallel combination of the on-resistances of the two transistors. The transmission gate represents a bi-directional resistive connection between the input and output terminals. The individual on-resistances R_{on_p} and R_{on_n}, as well as the equivalent on-resistance R_{on_cmos}, all vary as a function of the input voltage V_{in} (figure 3.9.2). The PMOS is cut-off $R_{on\_p} = \infty$ for $V_{in} \leq V_{tp}$, and the NMOS is cut-off for $V_{in} \geq V_{dd} - V_{tn}$. The equivalent on-resistance of a CMOS switch, compared with that of a single NMOS or PMOS device, varies much less as a function of the input voltage. The acquisition time of the switches can be decreased only by lowering R_{on}. Thus, in high speed applications, switches must be built by large W / L ratio, but this leads more charge injection errors according to below expression

$$Q_{ch} \approx WLC_{ox}(V_{GS}-V_{TH}). \qquad (3.24)$$

In this project, R_{on} is less than 1.7 kΩ for the switches (figure 3.9.3). The relatively constant on-resistance minimizes the harmonic distortion [41]. The equation of the on-resistance is

$$Ron = \frac{1}{\mu_n Cox \frac{W}{L}(V_{GS} - V_{TH})} = \frac{1}{g_m} \qquad (3.25)$$

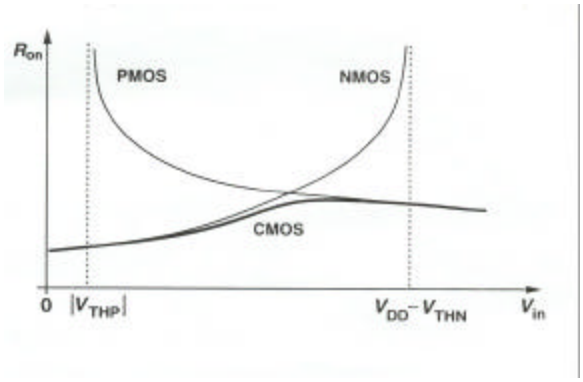

Figure 3.9.2 Representation of R_{on} resistances for NMOS, PMOS and CMOS transistors

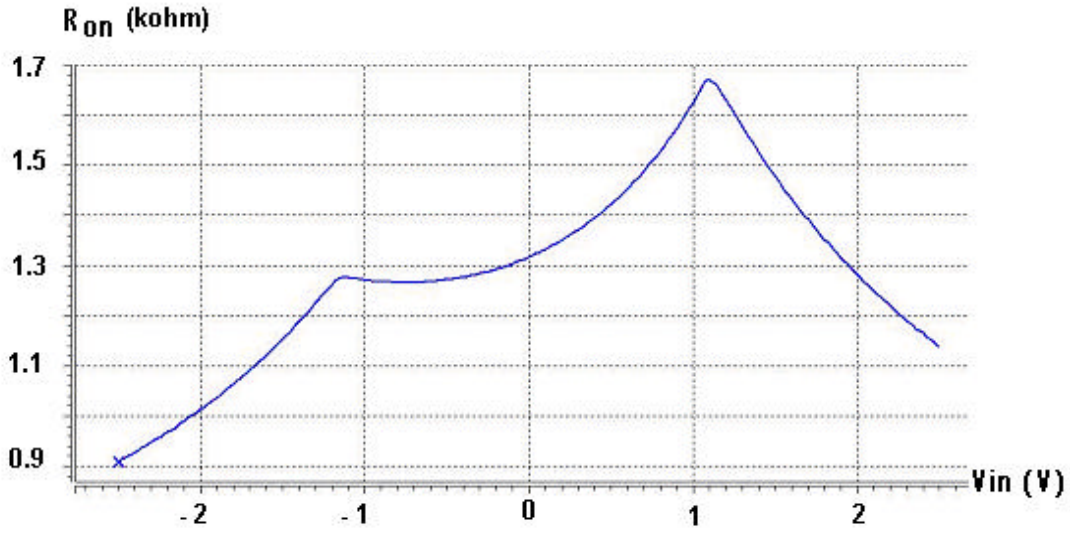

Figure 3.9.3 R_{on} characteristics of the CMOS switch

To design the CMOS switch, two aspects must be considered. First, the threshold voltages are made equal in magnitude. Second, the transconductance parameters, *kn and kp*, must be considered. Equating these parameters, we have

$$k_n' \frac{W_n}{L_n} = k_p' \frac{W_p}{L_p} \qquad (3.26)$$

where $K_n' = m_n C_{ox}$ *and* $K_p' = m_p C_{ox}$. *(3.27)*

Substituting (3.26) and (3.27) gives

$$m_n C_{OX} \frac{W_n}{L_n} = m_p C_{OX} \frac{W_p}{L_p} \qquad (3.28)$$

The oxide capacitance per unit area is

$c_{ox} = e_{ox} / t_{ox}$ *(F/cm^2)* *(3.29)*

where e_{ox} is oxide permittivity (F/cm). For SiO_2 $e_{ox} = 3.9\ e_o$, where $e_o = 8.854 \times 10^{-14}$ *F/cm* and t_{OX} is oxide thickness (cm). C_{OX} is same for both devices, thus, the equation (3.28) reduces to

$$m_n \frac{W_n}{L_n} = m_p \frac{W_p}{L_p} \qquad (3.30)$$

Typically, for the surface of silicon the electron and hole mobility are approximately

m_n *(Si) = 580 cm / V . s and* $m_p = 230$ *cm / V . s* *(3.31)*

where total impurity concentration, Ni, is *1 x 10^{17} cm^{-3}* at room temperature.

Substituting (3.30) and (3.31) yield

$$580 \frac{W_n}{L_n} = 230 \frac{W_p}{L_p} \qquad (3.32)$$

and reduces approximately to

$$\frac{W_p}{L_p} \approx 2.5 \frac{W_n}{L_n} \qquad (3.33)$$

Therefore, the CMOS switch devices must be related by the charge carrier mobility ratio of approximately 2.5 for silicon [36].

V_{in} and V_{out} HSPICE transient analysis characteristics response to V_{ref} and V_{ref_inv} for CMOS switch are shown in figure 3.9.4. When switch is on (approximately between 5 ns – 55 ns and 115 ns – 165 ns), V_{out} is equal to V_{in}. When switch is off (between 60n-110n), V_{out} is equal to zero.

3.10 Design requirements

In this project the lock-in amplifier needs a reference channel, which is supplied by a signal generator, a comparator to prevent signal distortion, and an input offset voltage adjustment circuit.

Although generally lock-in amplifiers use their own reference channel, which includes variable phase shifter, in order to provide exact same on-phase situation for both input and reference signal, in this work both input and reference signal are supplied by same source. Hence, both signals have same phase and frequency.

The input signal and the reference signal travel long way to reach both the demodulator and the LED via coaxial cables and connectors from their source signal generator. Therefore, signal is disturbed somewhere in the system. In order to prevent this problem, we had to use a comparator. National Semiconductor LM 311N comparator helps reshaping the signal [16].

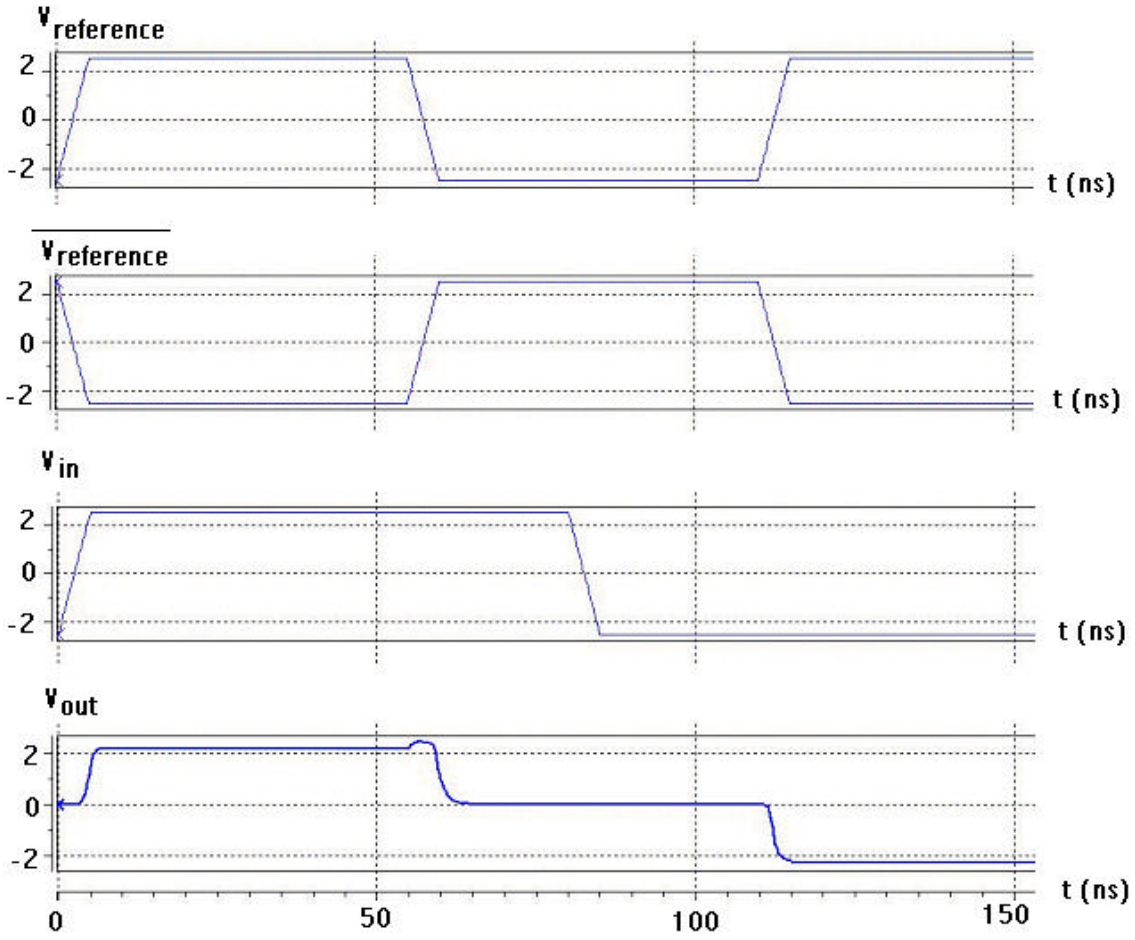

Figure 3.9.4 V_{in} and V_{out} HSPICE transient analysis characteristics of the CMOS switch

Another trade off in this system is input offset adjustment. R4BS op-amp has approximately 1 mV input offset voltage. Although this is a very small value, we are measuring very small signals and these signals may be smaller than the input offset voltage. In addition 1 mV input offset voltage can be 100 mV after the gain stage (gain stage has x100 gain). To provide input offset adjustment, we used Maxim OP 27 op-amp followed by the gain stage.

Chapter 4

Experimental Testing and Results

4.1 Layout Process

The first step in testing was to observe the performance and accuracy of each system block separately. For this reason, the demodulator chip was built as independent blocks. Figure 4.1.1 shows the lock-in amplifier's stages and connection scheme. The signal channel is totally independent from the chip. Figure 4.1.2 shows the lock-in amplifier and its off-chip elements. Using off-chip elements is more practical than using on-chip elements due to the necessity of putting very large resistors for pre-amplifier, gain, and low pass filter stages for adjusting filter time constants. Although it is also possible to use off-chip elements for the demodulators, we used on-chip elements for both demodulators (figure 4.1.3).

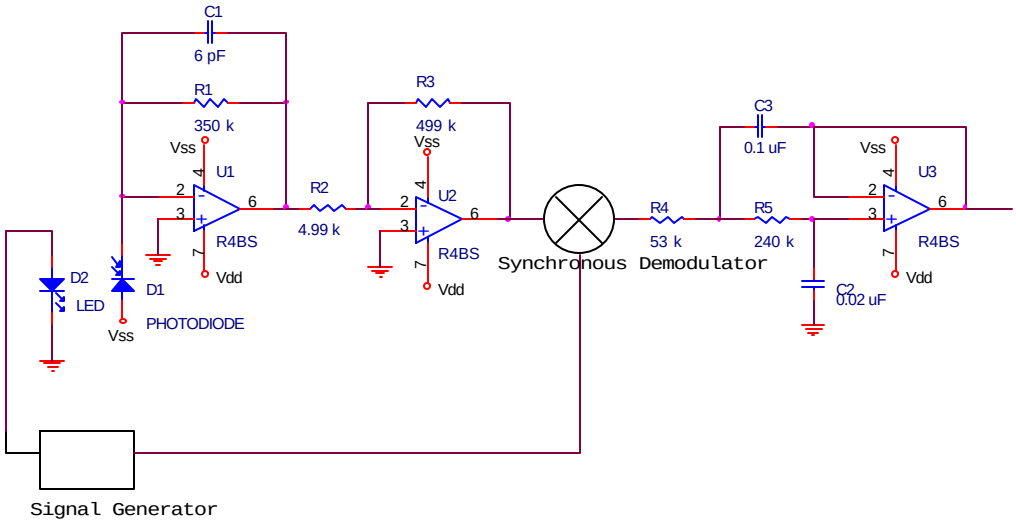

Figure 4.1.1 General block diagram of the lock-in amplifier system

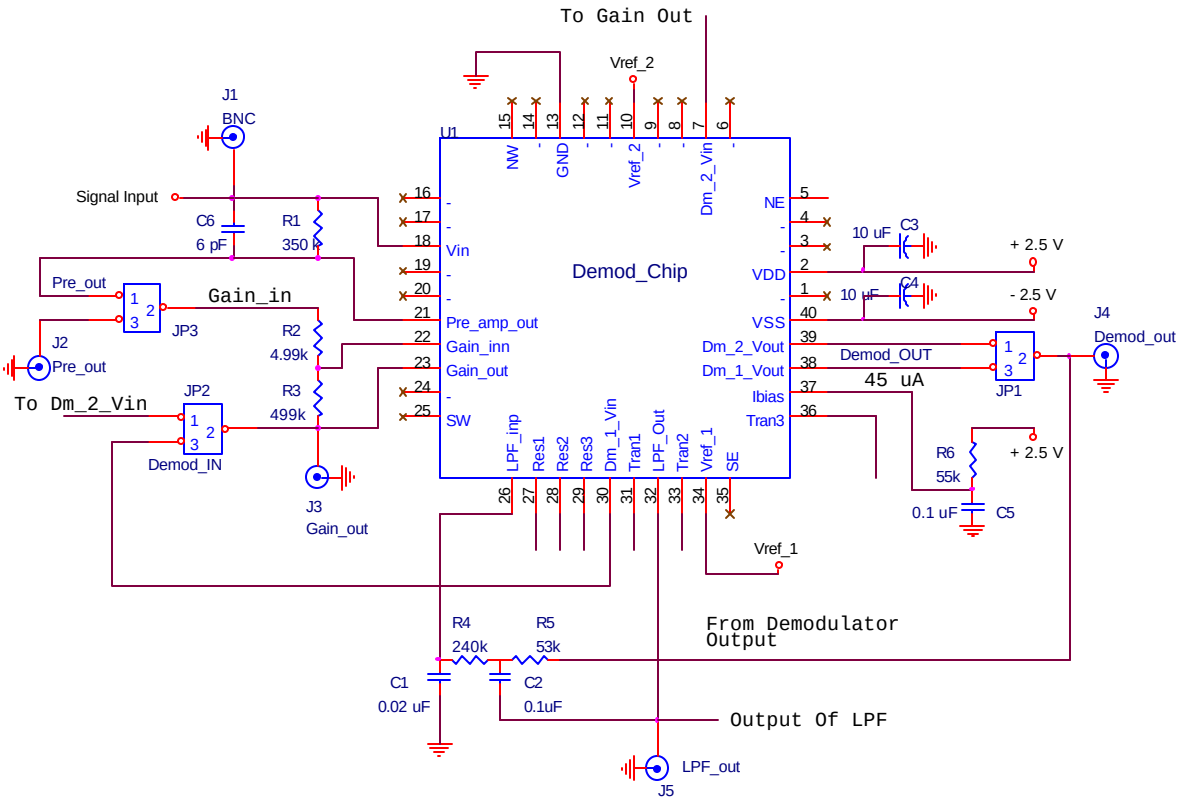

Figure 4.1.2 Optimization of the off-chip elements

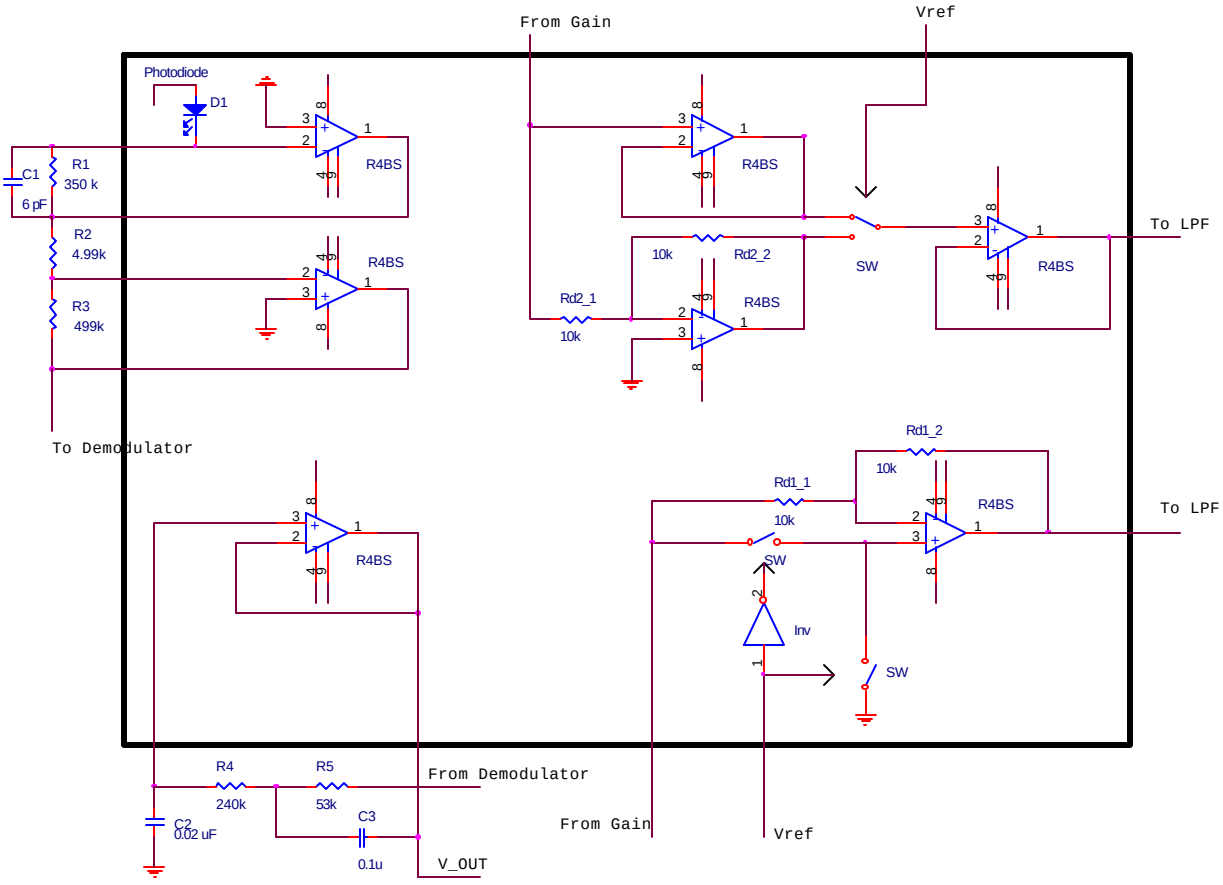

Figure 4.1.3 Representation of the layouts

Figures 4.1.4, 4.1.5, 4.1.6, 4.1.7 and 4.1.8 show the output responses of the each system block. At 6 kHz gain stage output has exactly equal to x100 the input signal. This output has 4.07 μs fall time and 4.11 μs rise time (figure 4.1.4). We applied ± 2V input signal at 6 kHz for demodulator stages. Demodulators were built by inverting gain amplifiers, therefore, demodulators must rectify this input signal at –2 V level. Both demodulators have almost same output response (figures 4.1.5 and 4.1.6). For low pass filter stage, the input signal comes from the demodulator output, which is equal to – 2 V level. The low pass filter cuts off all frequencies beyond 31.6 Hz and its output is equal to – 2 V dc level (figure 4.1.7 and 4.1.8).

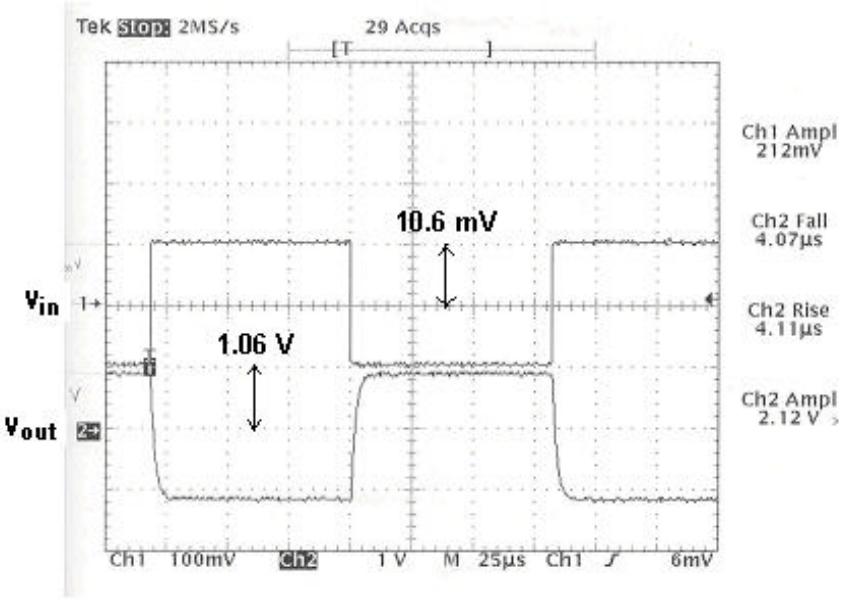

Figure 4.1.4 V_{in} and V_{out} signals of the gain stage

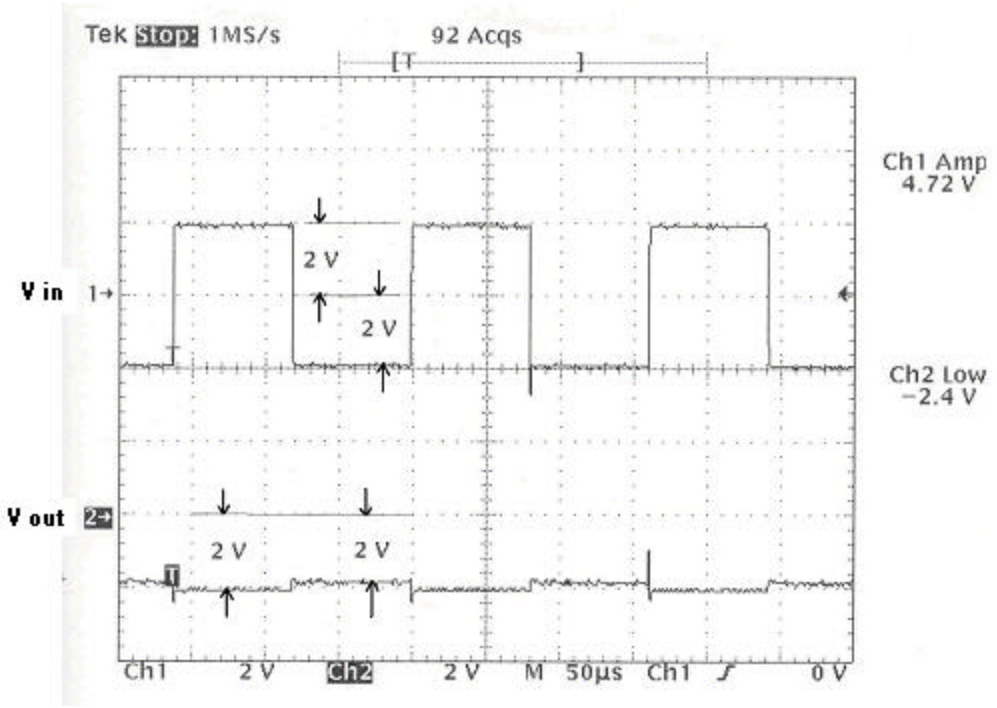

Figure 4.1.5 V_{in} and V_{out} signals of the demodulator_1

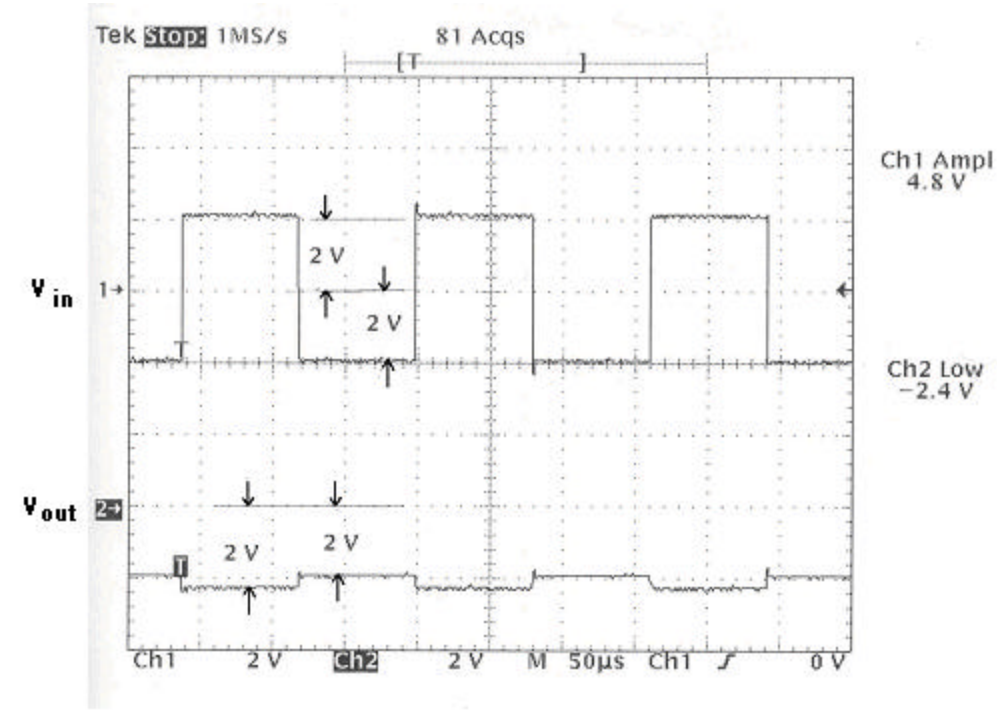

Figure 4.1.6 V_{in} and V_{out} signals of the demodulator_2

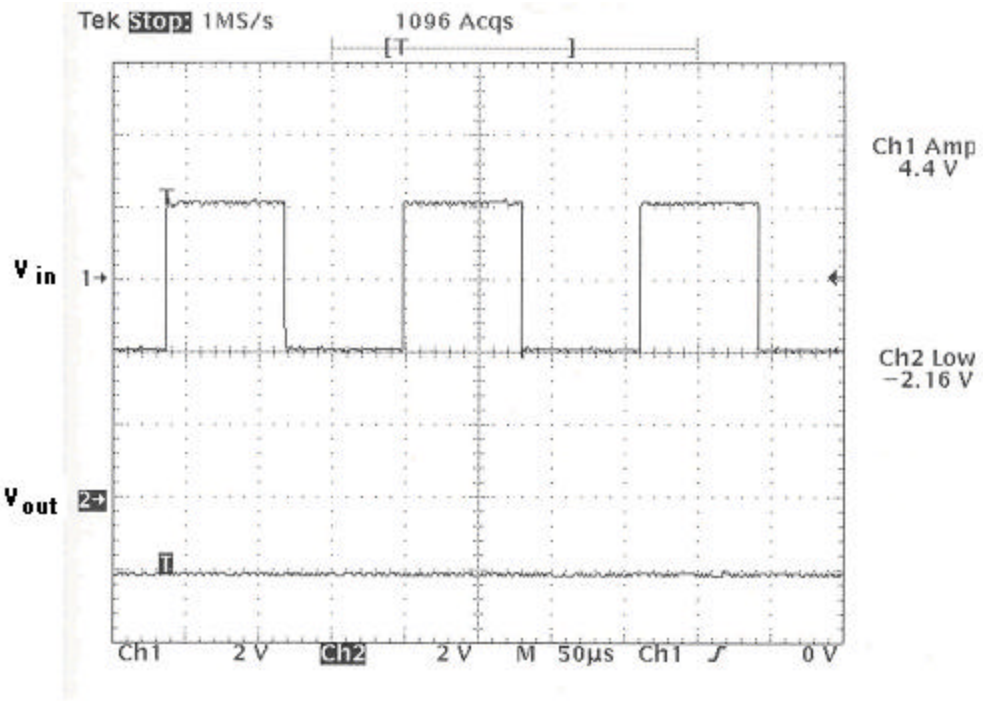

Figure 4.1.7 V_{in} for the demodulator_1 and V_{out} for the LPF

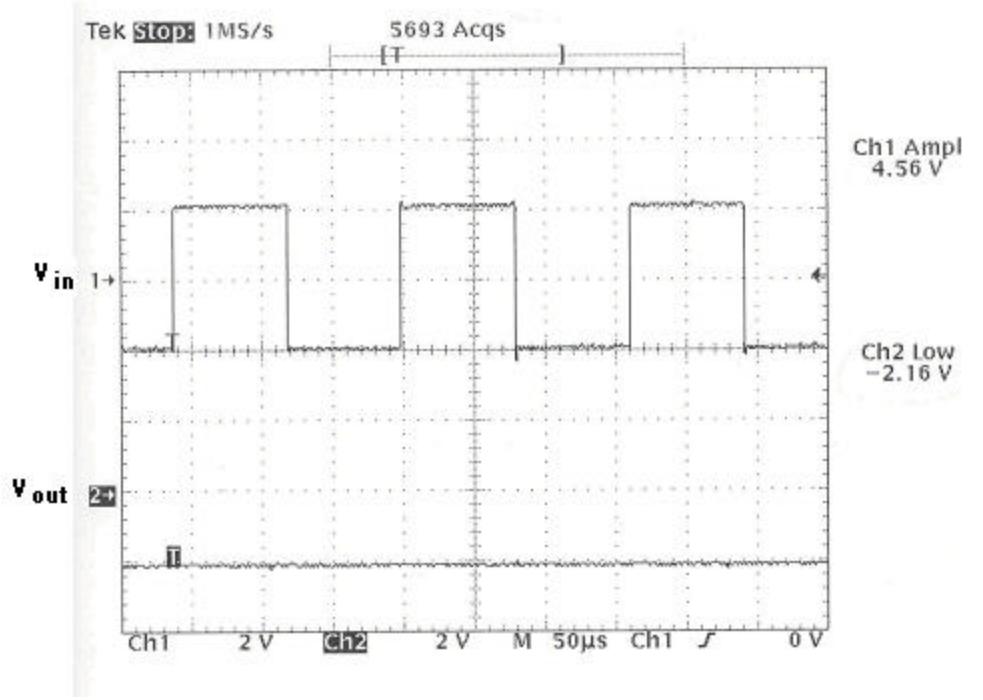

Figure 4.1.8 V_{in} for the demodulator_2 and V_{out} for the LPF

Demodulator_1 and demodulator_2 stages are the principal building blocks of the IC. Hence, these two blocks were tested separately for their accuracy and linearity. Figure 4.1.9 shows the input and the output voltage characteristics of the demodulators when they are independent from the other stages. Figure 4.1.10 displays linearity of the demodulators. The linearity errors are not same for both demodulators. As an example, while 1st demodulator has –1 % error at ± 2.5 V input signal, 2nd demodulator has -5 % error at the same point. Figure 4.1.11 shows these linearity errors as a percentage.

The low pass filter outputs for both demodulators are almost constant until 20 kHz (figure 4.1.12). After that point, dc outputs of the low pass filter for the demodulator decrease very sharply. Although, both demodulators can work precisely until 20 kHz for this case, their accuracy will change by applying the other stages to the demodulator blocks.

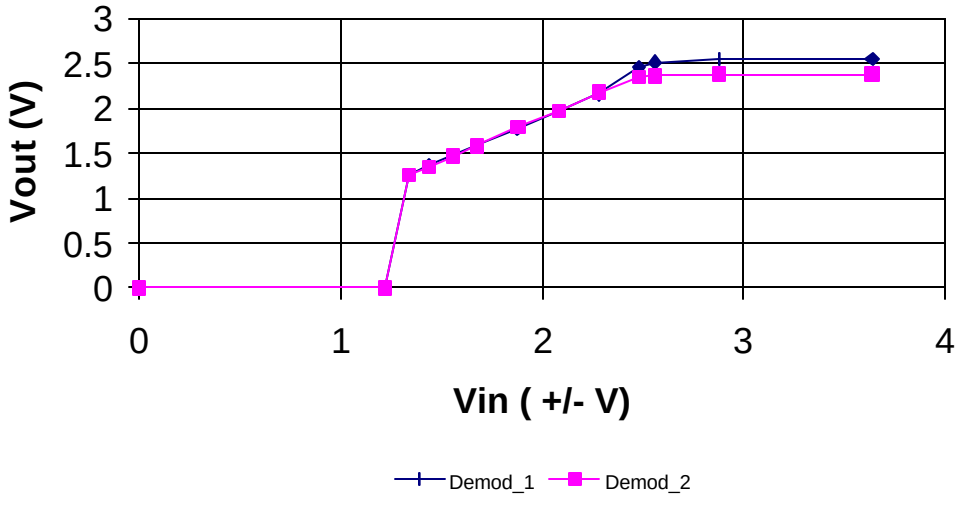

Figure 4.1.9 Voltage transfer characteristics of both demodulators

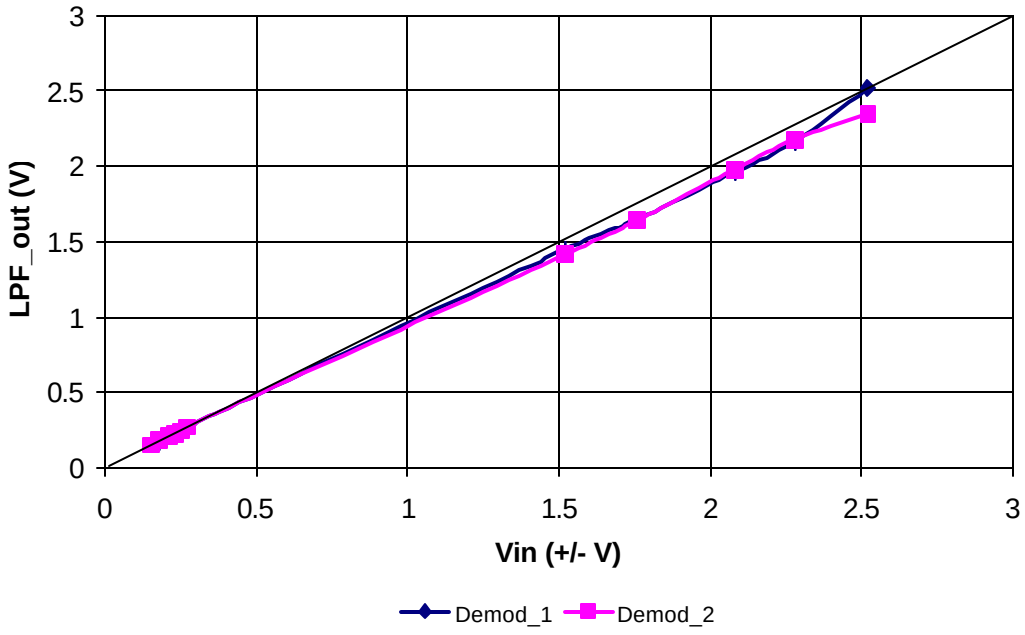

Figure 4.1.10 Voltage transfer characteristics show the linearity errors

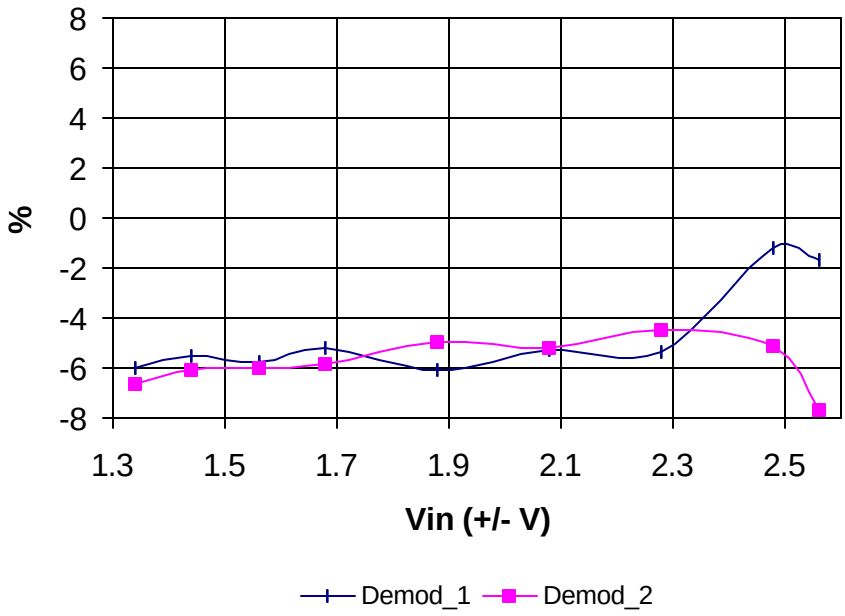

Figure 4.1.11 Linearity errors as a percentage

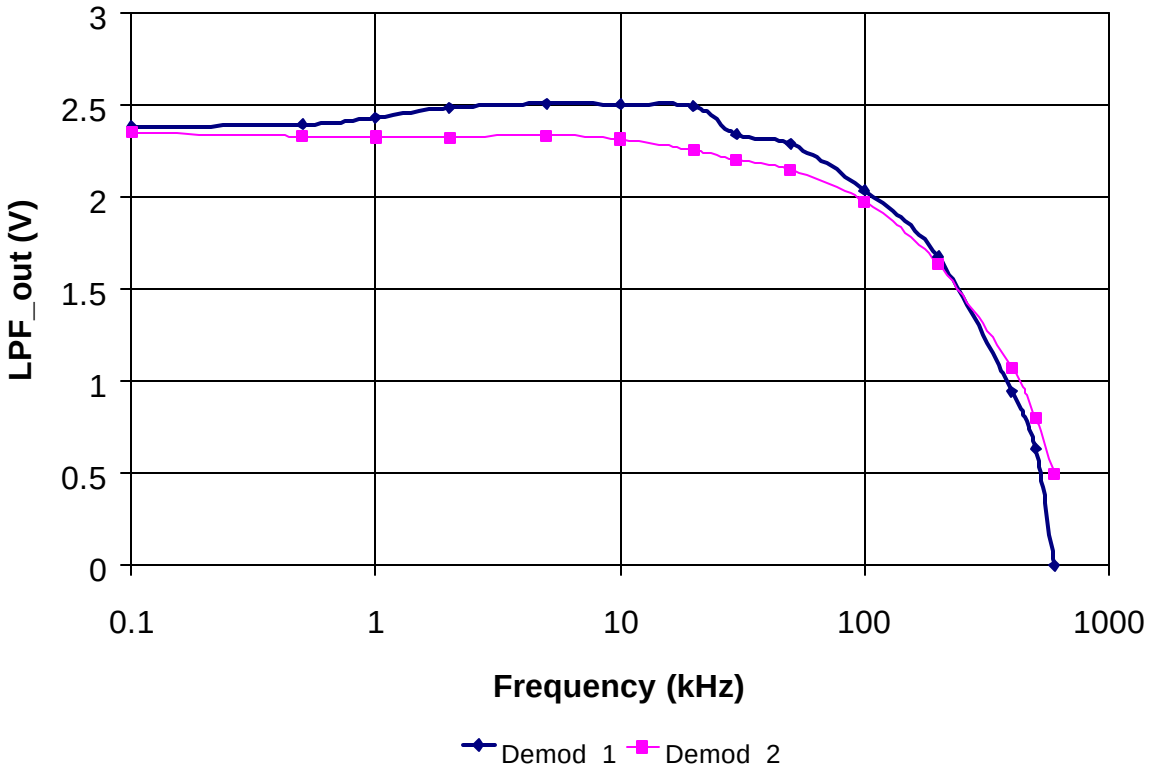

Figure 4.1.12 Outputs of the LPF for both demodulators by frequency change

(Vin » ± 2.5 V)

4.2 HSPICE Analysis

An HSPICE simulation was performed on the whole demodulator chip before the chip was fabricated. A current source was used to simulate the current of the photodiode. Figure 4.2.1 illustrates the HSPICE transient analysis for a square wave detected input signal and the resulting output responses for each stage at 1 kHz.

The demodulator output is equal to 1 V amplitude and there is no negative side value (figure 4.2.2). Therefore its low pass filter output is expected to be half value of the demodulator output, which is 500 mV for perfect conditions. In HSPICE transient analysis, the low pass filter output is around 490 mV (figure 4.2.4) because there are charge injection errors due to unwanted charges being injected into the circuit when the transistors turn off. As a result of charge injection some glitches occur during the switching (figure 4.2.3). CMOS complementary switch architecture and 2.5 size ratio between the n-mos and p-mos devices inside of the switch help minimize these charge injection errors during the switching.

4.3 Laboratory Testing

In experimental laboratory testing, we used 1 kHz square wave input and reference signal for the lock-in amplifier. The pre amplifier output has 6 mV amplitude with 1 mV offset voltage (figure 4.3.1). So, its actual value is equal to 5 mV amplitude. We eliminated this offset voltage by using the offset adjustment circuit. The gain output has 450 mV amplitude with no offset voltage (figure 4.3.2). The demodulator rectifies this input by inverting it on the negative side, which is around –450 mV amplitude. Both

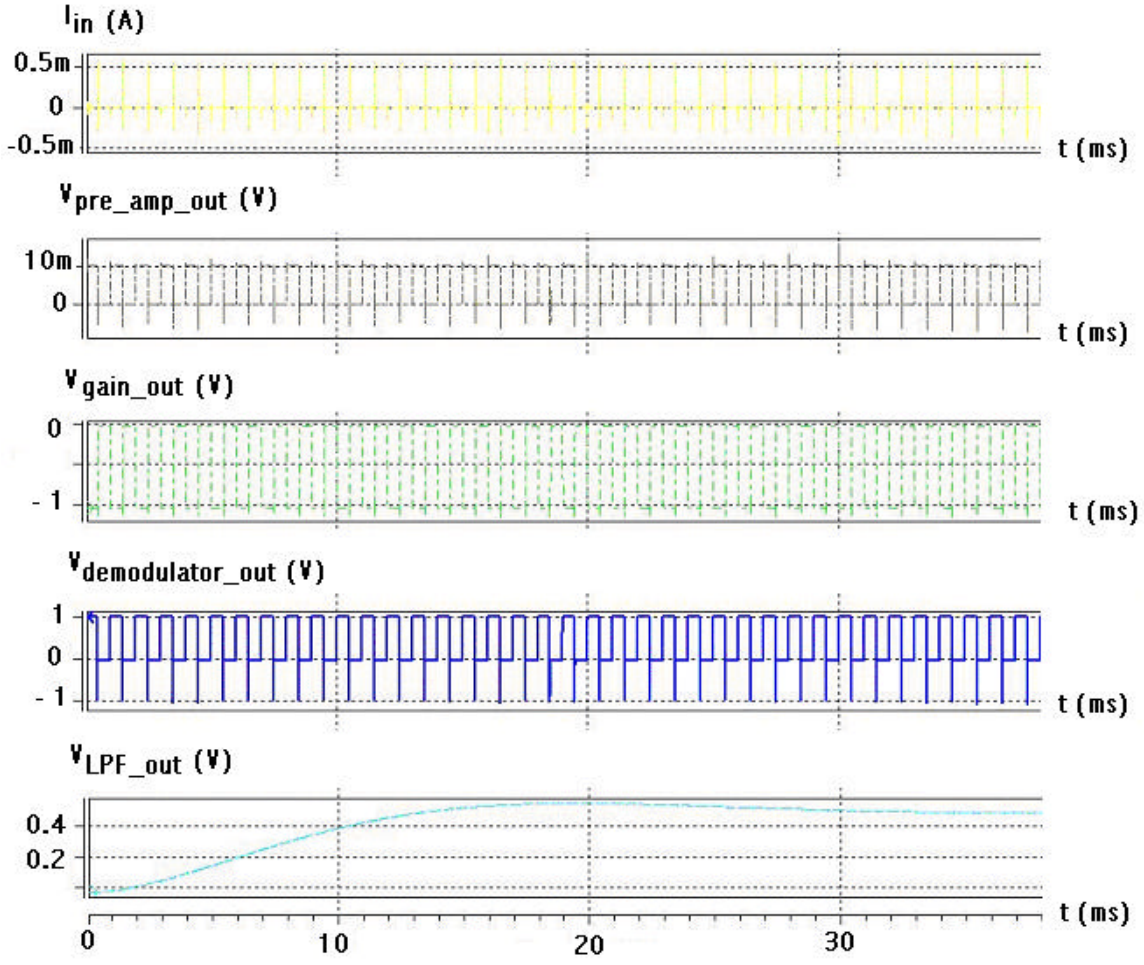

Figure 4.2.1 HSPICE transient analysis for the demodulator chip

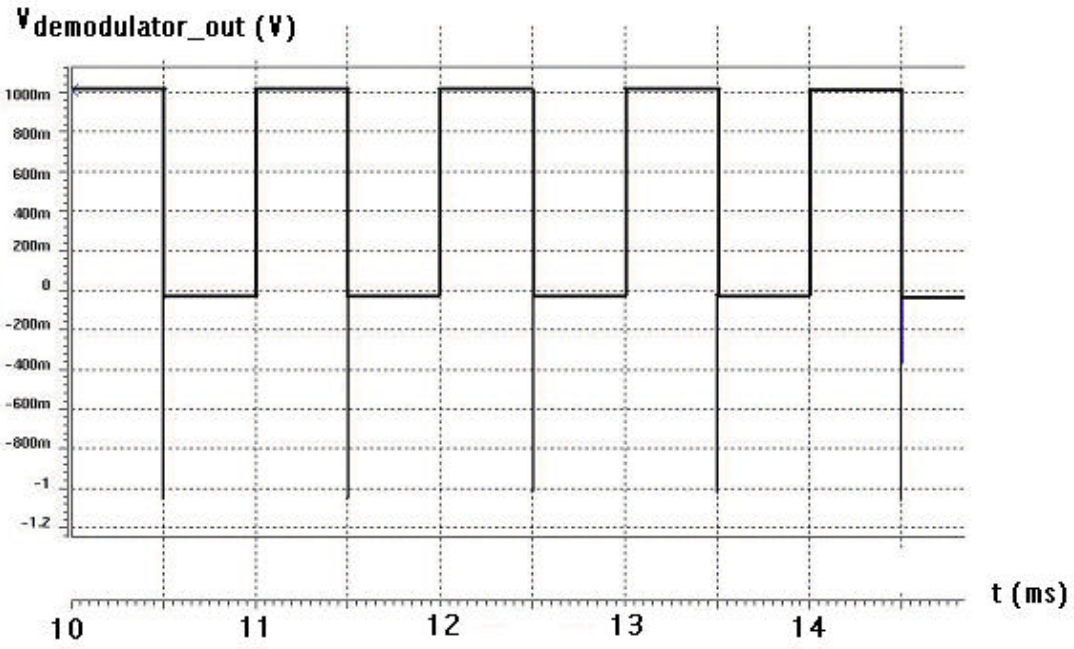

Figure 4.2.2 HSPICE transient analysis for demodulator output

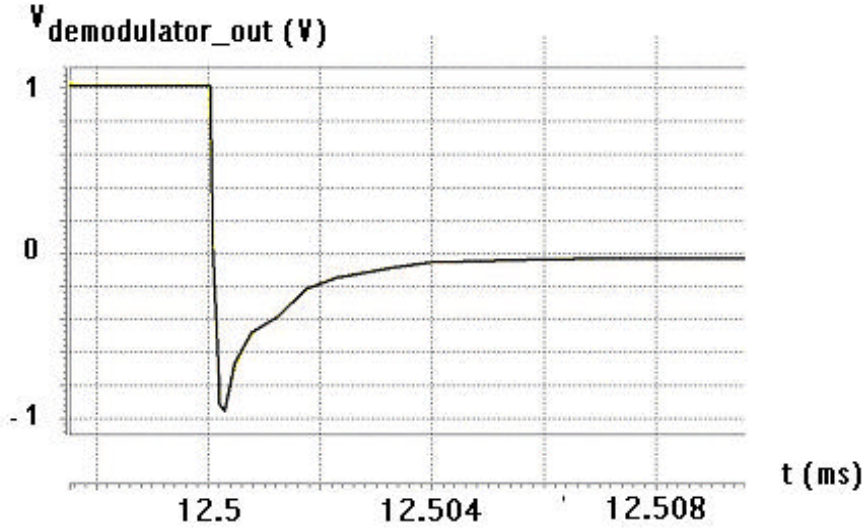

Figure 4.2.3 Charge injection error

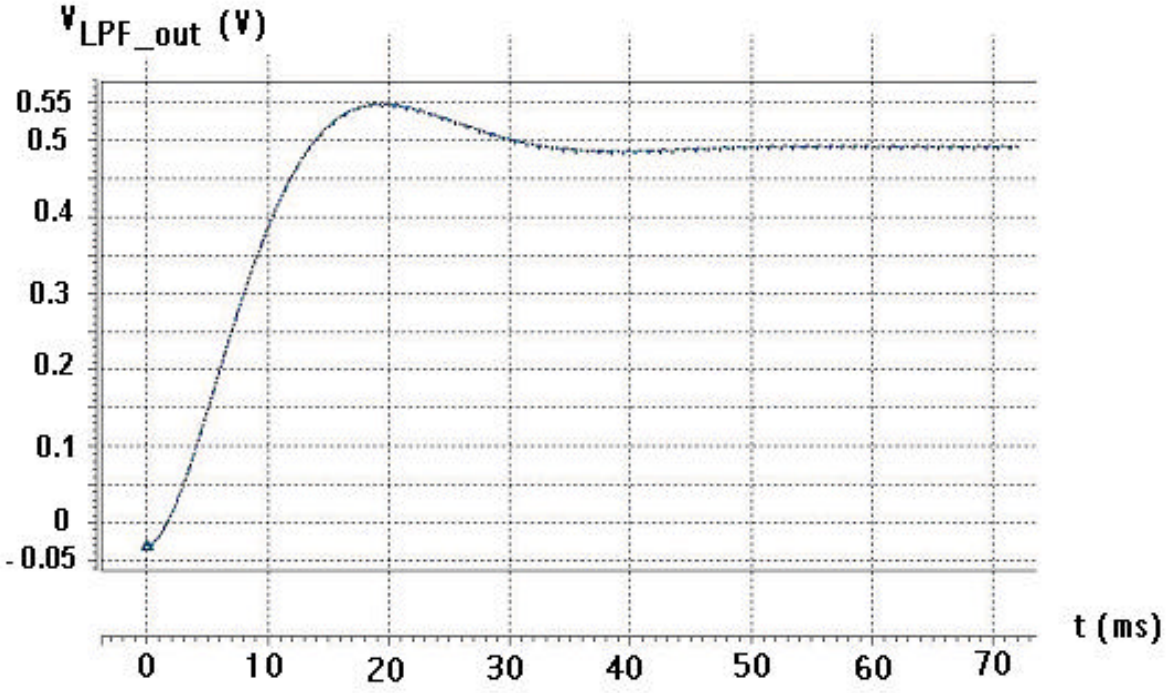

Figure 4.2.4 HSPICE transient analysis for the LPF output

demodulators almost have same output for this input signal (figures 4.3.3 and 4.3.4). Followed the demodulator stage, the low pass filter has around –225 mV dc output for both demodulators (figures 4.3.5. and 4.3.6).

4.4 Additional Analysis

The synchronous demodulator of the lock-in amplifier will give a phase sensitive dc output in response to signals at odd multiple frequencies, such as $3f_{ref}$, $5f_{ref}$, etc [1]. This is shown in figure 4.4.1 for a sine wave signal at the third odd multiple of the reference frequency. The relative sensitivity of the detection system at these additional

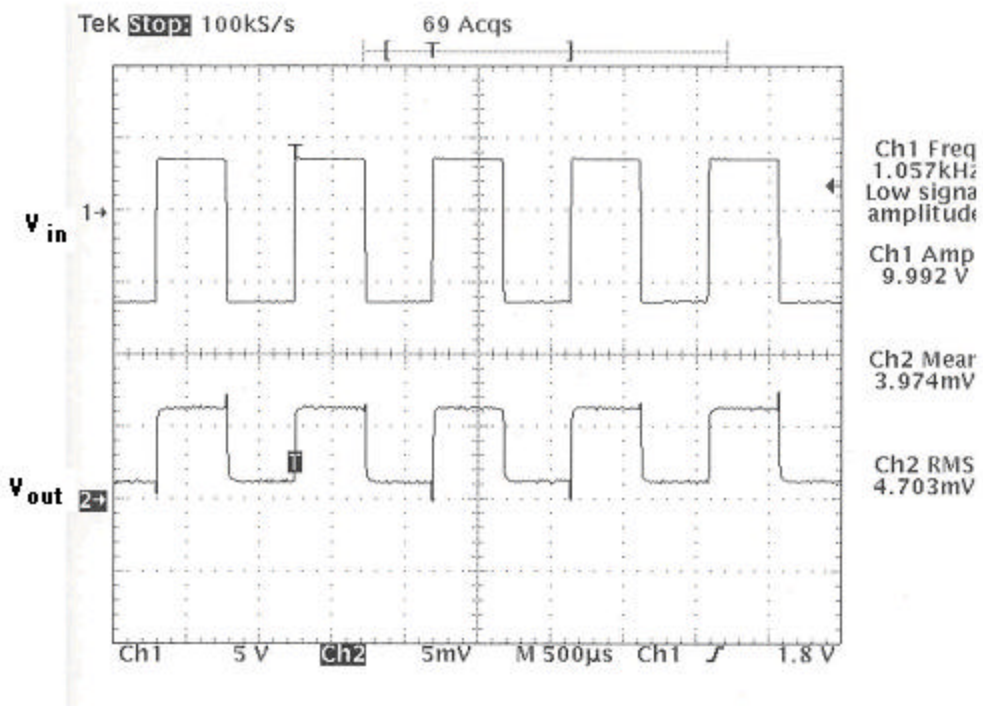

Figure 4.3.1 V_{in} for the LED and V_{out} for the pre-amplifier stage

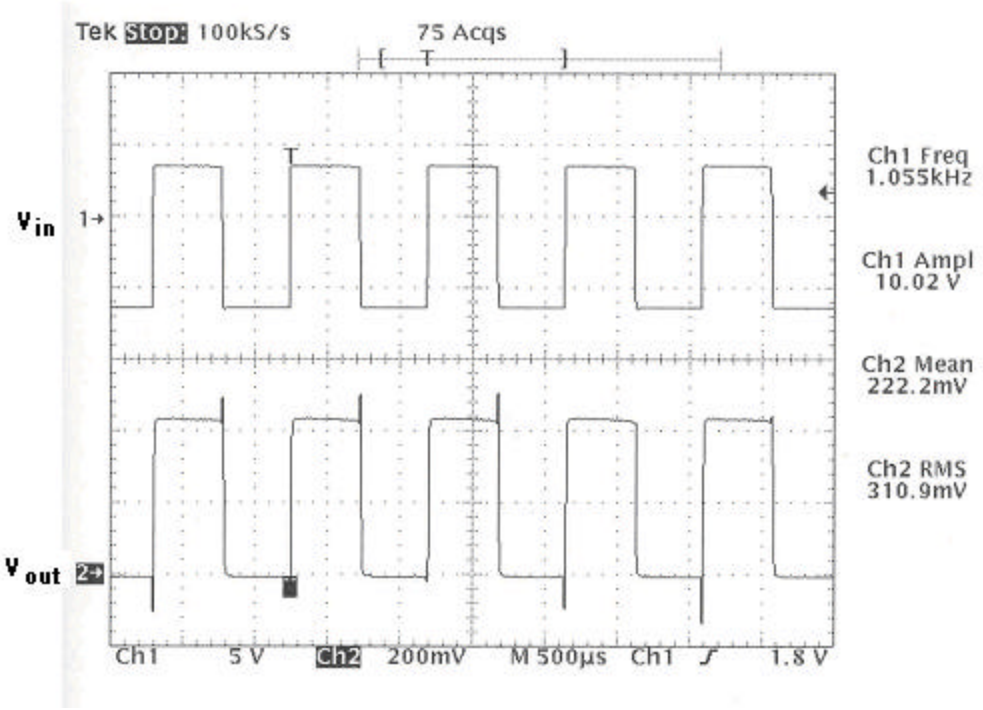

Figure 4.3.2 V_{in} for the LED and V_{out} for the gain stage

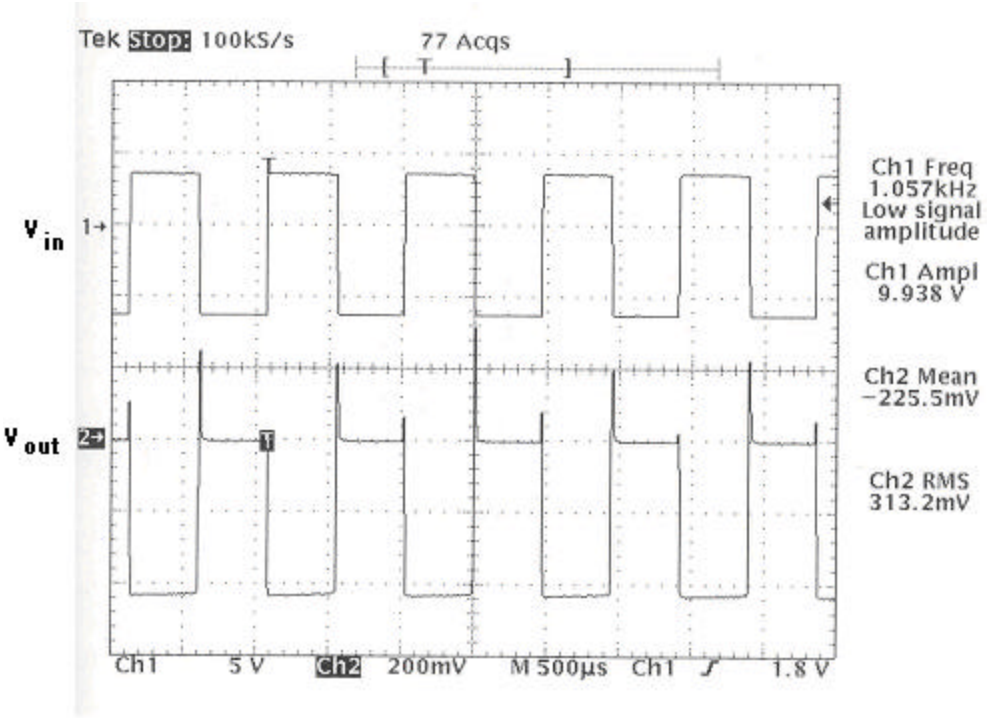

Figure 4.3.3 V_{in} for the LED and V_{out} for the demodulator_1 stage

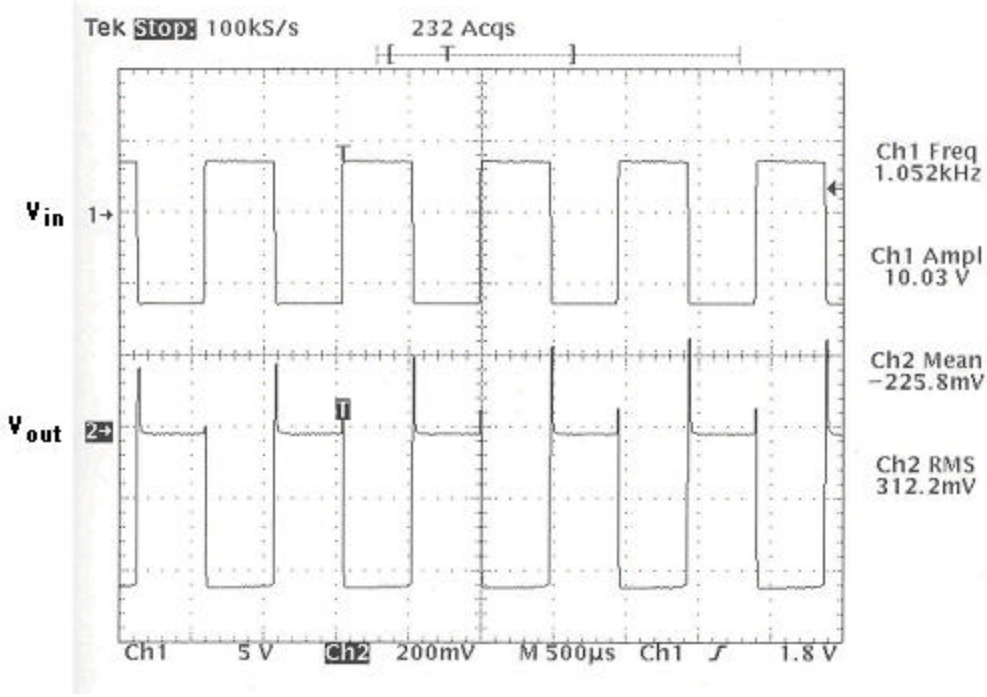

Figure 4.3.4 V_{in} for the LED and V_{out} for the demodulator_2 stage

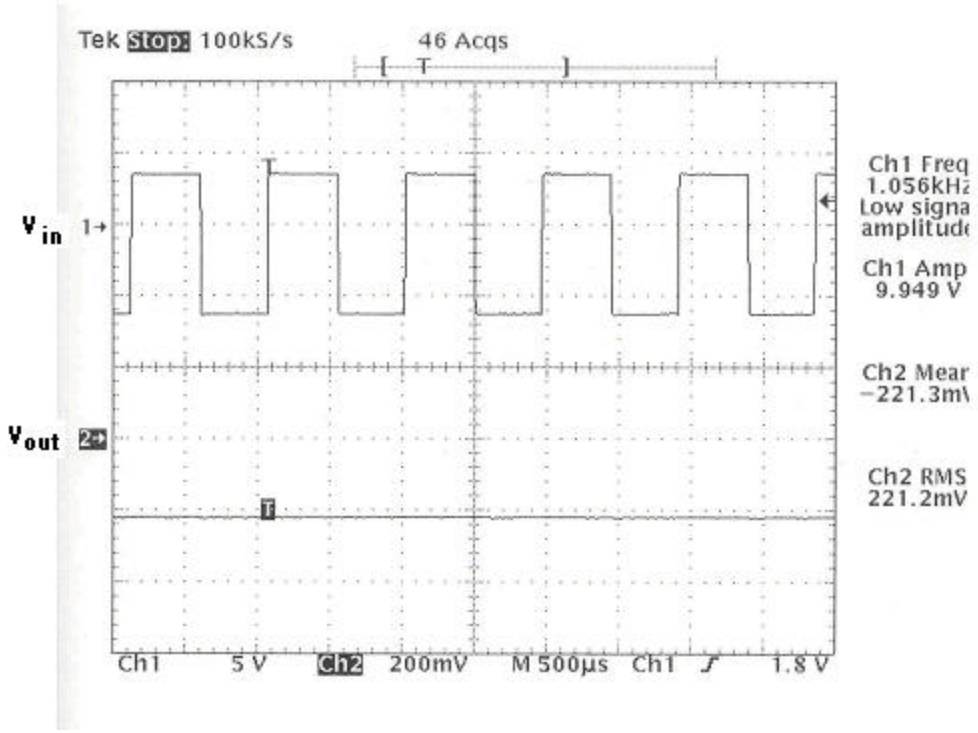

Figure 4.3.5 V_{in} for the LED and V_{out} for the LPF stage of the demodulator_1

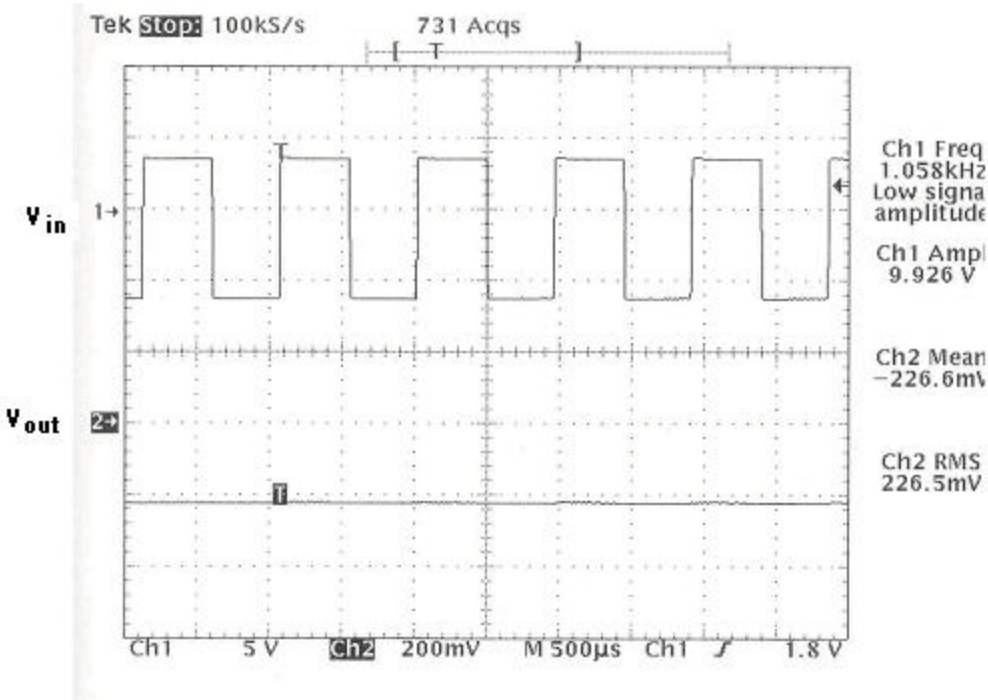

Figure 4.3.6 V_{in} for the LED and V_{out} for the LPF stage of the demodulator_2

frequencies is 1/3, 1/5 and so on, corresponding to the relative magnitudes of the reference Fourier components. A detection system with this property is said to be harmonically responding. Other than these odd harmonics, low pass filter output is essentially zero for all other frequencies, even for very close values to reference frequency (figure 4.4.2).

A convenient way of representing the lock-in amplifier outputs is frequency difference existing between input and reference signals. We found additional odd harmonic components by using square wave reference signal as shown in figure 4.4.3. These are centered on the odd harmonics of the reference frequency and the maximum magnitude of each peak is weighted by the magnitude of its associated reference Fourier component. Before a signal can produce a response at the output lock-in amplifier, it must lie within one of the odd harmonics of the reference frequency. In order to produce a true 'dc' response a signal must be synchronous with one or more of the reference Fourier components. Figure 4.4.3 shows the test results of the low pass filter output for demodulator chip where $f_{ref} \approx 2$ kHz.

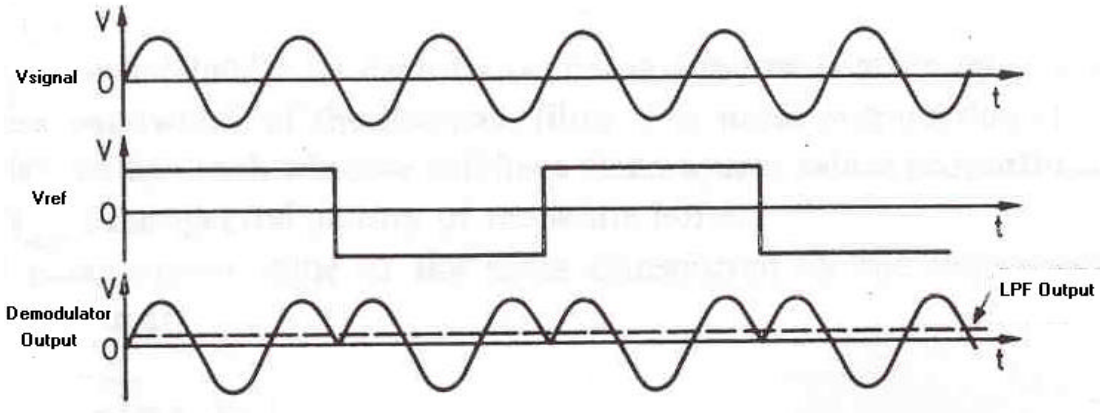

Figure 4.4.1 Output of the LPF for $f_{in} = 3f_{ref}$

At the first odd multiple, low pass filter output rms value is equal to 110 mV. At the third odd multiple, its value is equal to 1/3 value of the first odd multiple, which is around 36 mV. At the fifth odd multiple, it becomes 1/5 value of the first odd multiple, 22 mV. The practical significance of using these results is representing the frequency regions, where the lock-in amplifier is susceptible to large-scale discrete interference components.

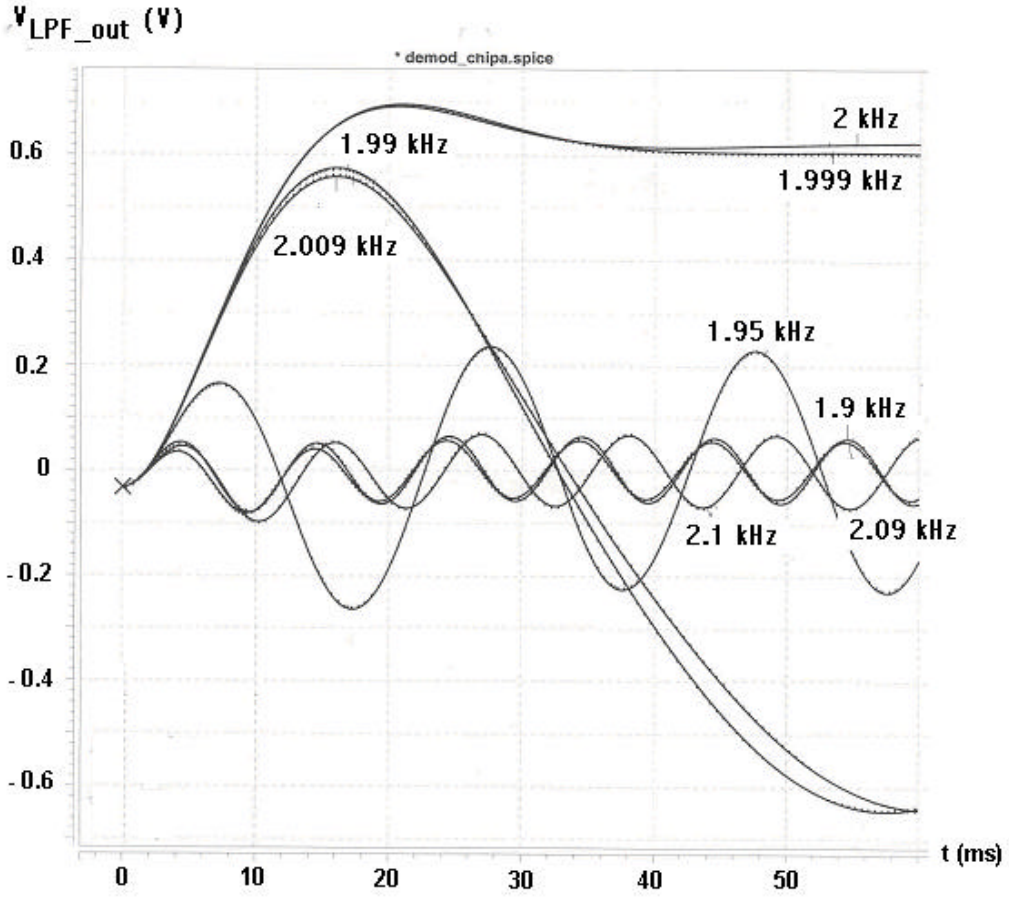

Figure 4.4.2 LPF outputs for different input frequencies where f_{ref} = 2 kHz

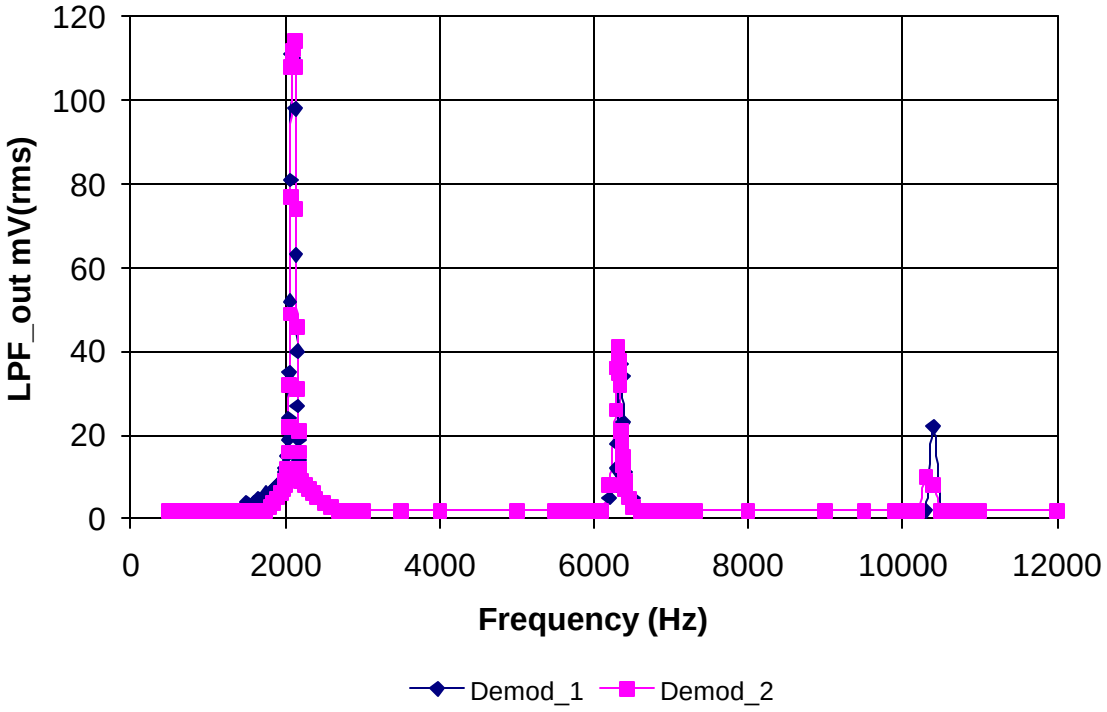

Figure 4.4.3 Outputs of the demodulator chip with odd harmonics of the reference frequency

When a signal with noise is measured by using lock-in amplifier, cut off frequency of the low pass filter has great effect of the result. Figure 4.4.5 shows the low pass filter rms output response for $f_o = 316\ Hz$ and $f_o = 31.6\ Hz$. For $f_o = 31.6\ Hz$ (figure 4.4.4), the low pass filter eliminates more noise components. Noise bandwidth of the lock-in amplifier has strong relationship with the low pass filter noise bandwidth (NB). The noise bandwidth of the second order low pass filter is

$$NB = \frac{2pf_0}{8} \qquad (4.1)$$

where $f_0 = w_0 / 2p$ (4.2)

f_o is the cut off frequency of the low pass filter.

Then, the noise bandwidth of the lock-in amplifier is

$$NB_{lock\_in} = 2\ NB. \qquad (4.3)$$

The noise bandwidth of the first case is equal to 495.66 Hz while in the second case it is 49.56 Hz. As shown in figure 4.4.5 the narrow noise bandwidth has sharper response.

Photodiode response is not same for different light intensities. As a result low pass filter output varies by depending on photodiode reverse bias current. Until around ± 1.5 V LED drives, the photodiode has only dark current (thermally generated), and as a result very small linear low pass filter output. After this point, the photodiode starts to give some response to the incident light (figure 4.4.6). The distance between photodiode and light source, LED, also affects this response.

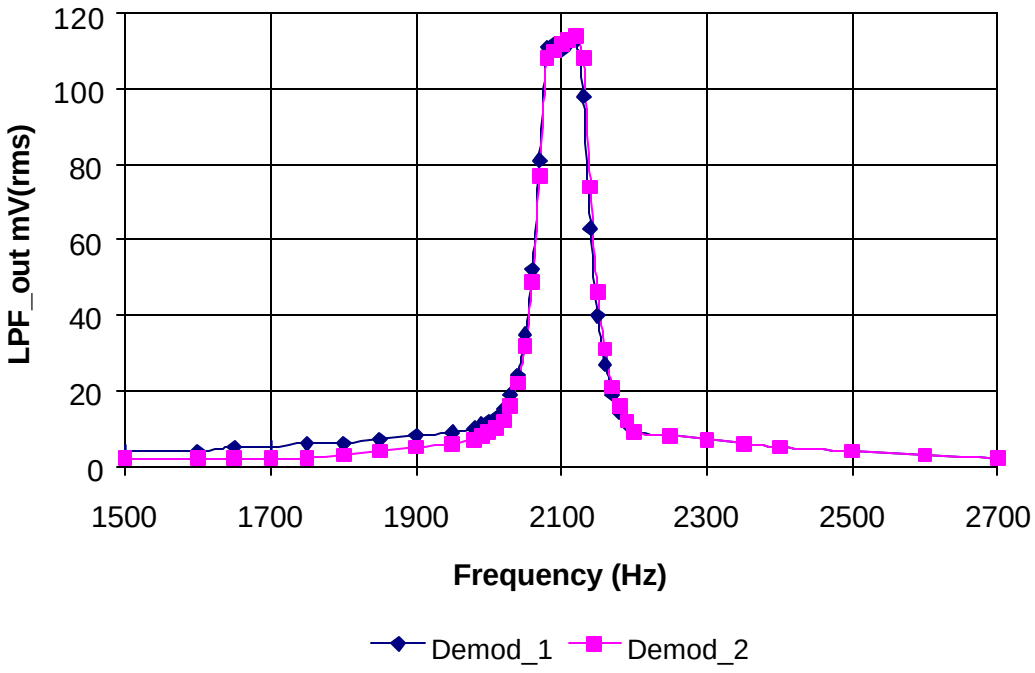

Figure 4.4.4 Representation of the noise bandwidth for the demodulators

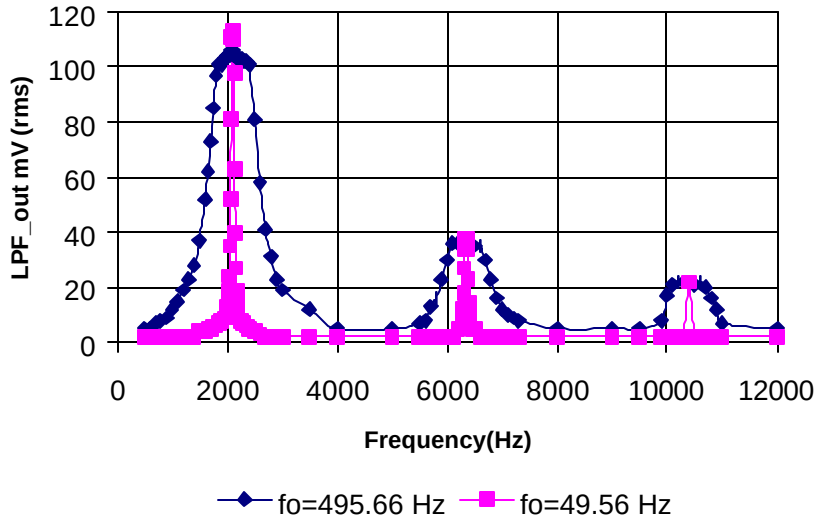

Figure 4.4.5 Outputs of the demodulator chip for different cut-off frequencies

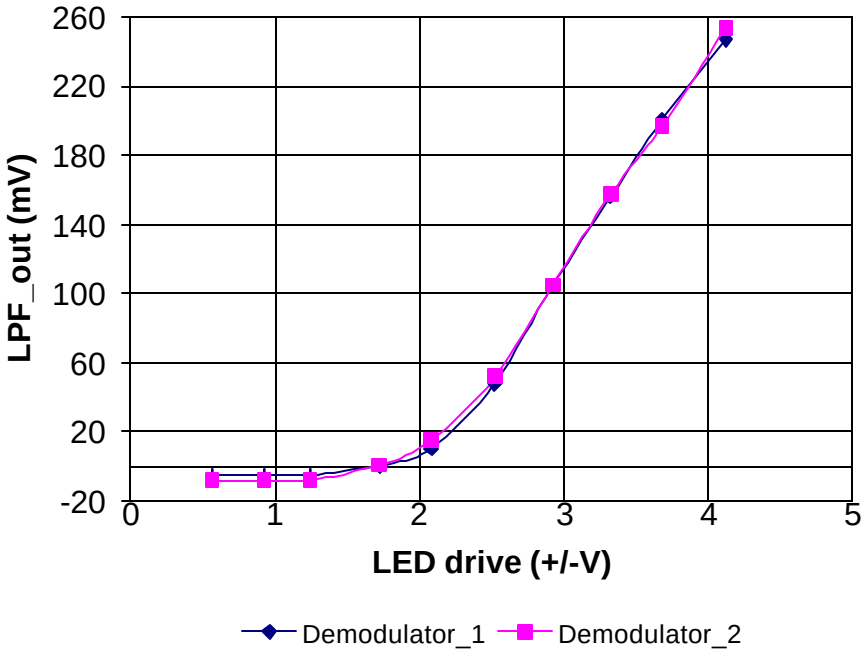

Figure 4.4.6 Output of the LPF changes by intensity of light

In practice, problems arise at high frequencies. For sine wave 1000 mV signal at 1 kHz, the output of low pass filter is equal to 640 mV, but for higher frequencies, this value will be reduced, such as at 50 kHz it is 560 mV. As a note these results are HSPICE simulation results for perfect conditions. In real experiment, differences become more significant. Although these two signals appear at same phase and frequency, there will be some non-equality at higher frequencies (figure 4.4.7). Figure 4.4.8 shows the demodulator chip output for different frequencies. While the system works very accurately at 1 kHz, system quality drops sharply in higher frequencies. There are several reasons of these errors such as switching errors due to charge injection, input signal and reference signal are not strictly in-phase because of long cables and connection errors and distance between the devices and errors due to signal generator distortion, etc.

The signal-to-noise ratio was found by measuring the output signal of demodulator chip in light and dark conditions. The output of the low pass filter is equal to 0.55 mV (rms) in dark conditions and is called the noise output. When we drive the LED by applying the reference voltage, the demodulator chip responds to the light. We measured 230 mV (rms) this output signal. Therefore,

$$SNR = 20\log\frac{V_{signal}(rms)}{V_{noise}(rms)} = 20\log\frac{230mV}{0.55mV} \tag{4.4}$$

SNR ≈ 52 dB .

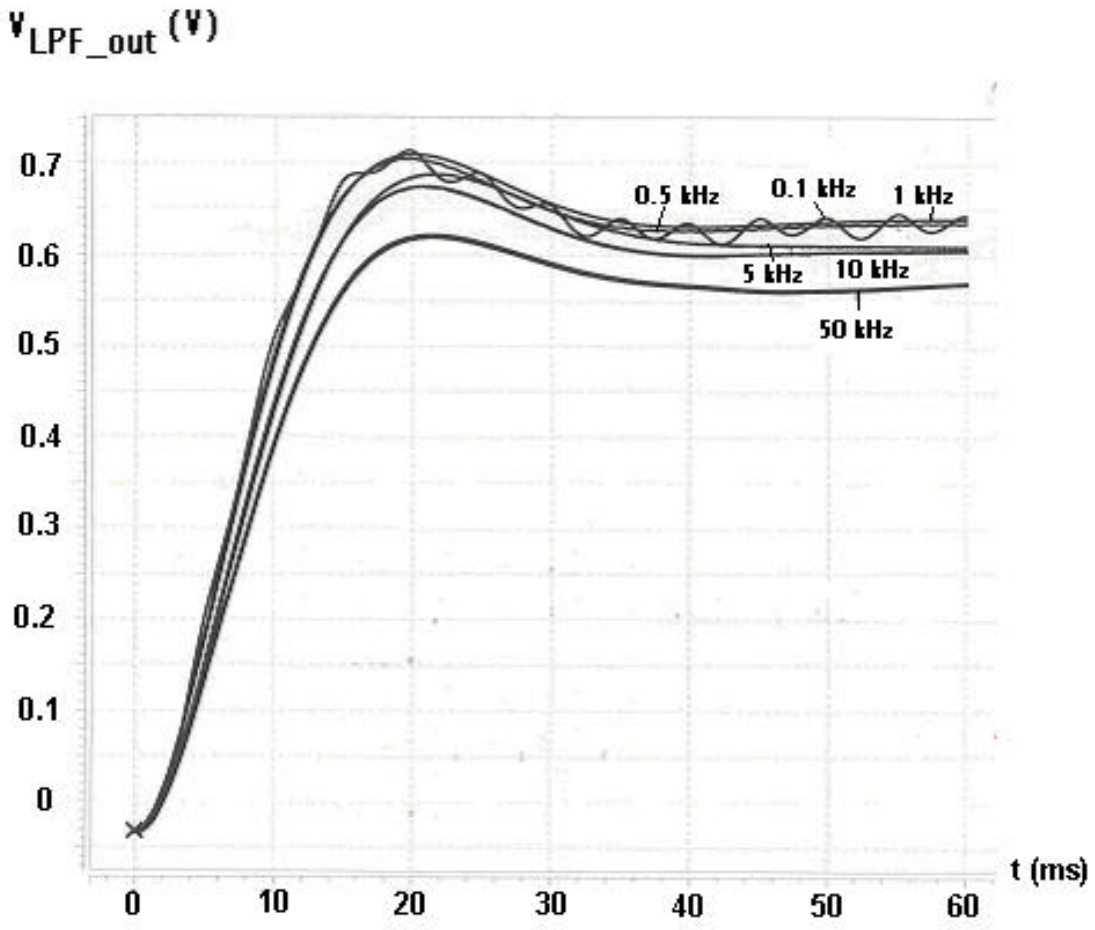

Figure 4.4.7 HSPICE transient analysis for different frequencies where $f_{ref} = f_{sig}$

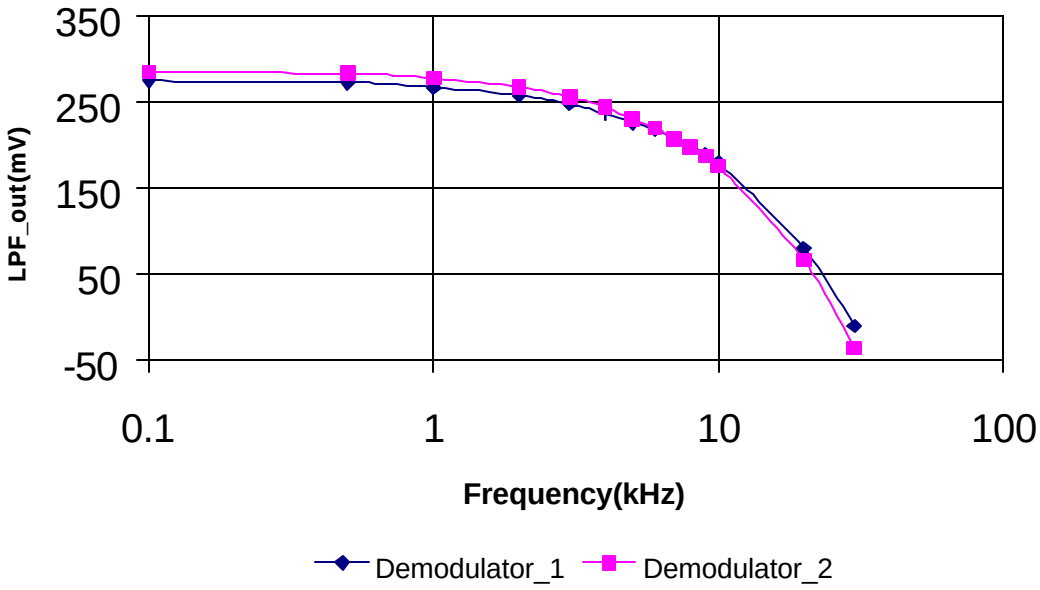

Figure 4.4.8 Final test of the chip for both demodulators

4.5 Demodulator Chip

Integration allows complex circuits, which consists of thousands of devices such as transistors, resistors, capacitors, and diodes, to be realized in a single semiconductor chip. In addition to advantages of miniaturization, fabrication of many integrated circuits on a single silicon (Si) wafer greatly reduces the cost.

MAGIC CAD software was used to implement this project for integrated circuits. AMI 1.5 µm CMOS technology was used. Figure 4.5.1 and 4.5.2 shows the general MAGIC layout placement of the chip. The first demodulator takes 1/3 less area than that of the second demodulator. It gives more area considerations for future work.

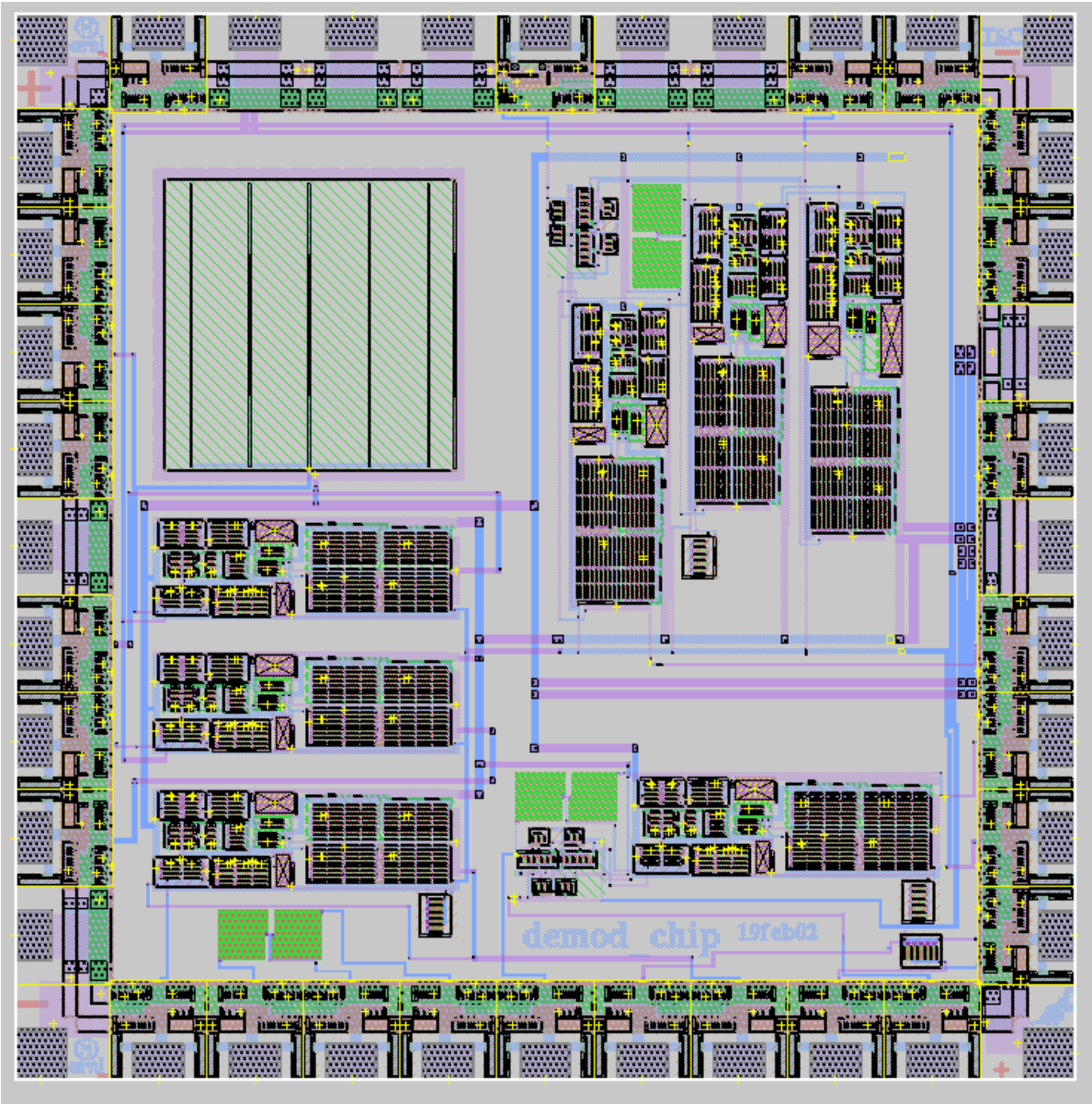

Figure 4.5.1 Demodulator chip MAGIC layout

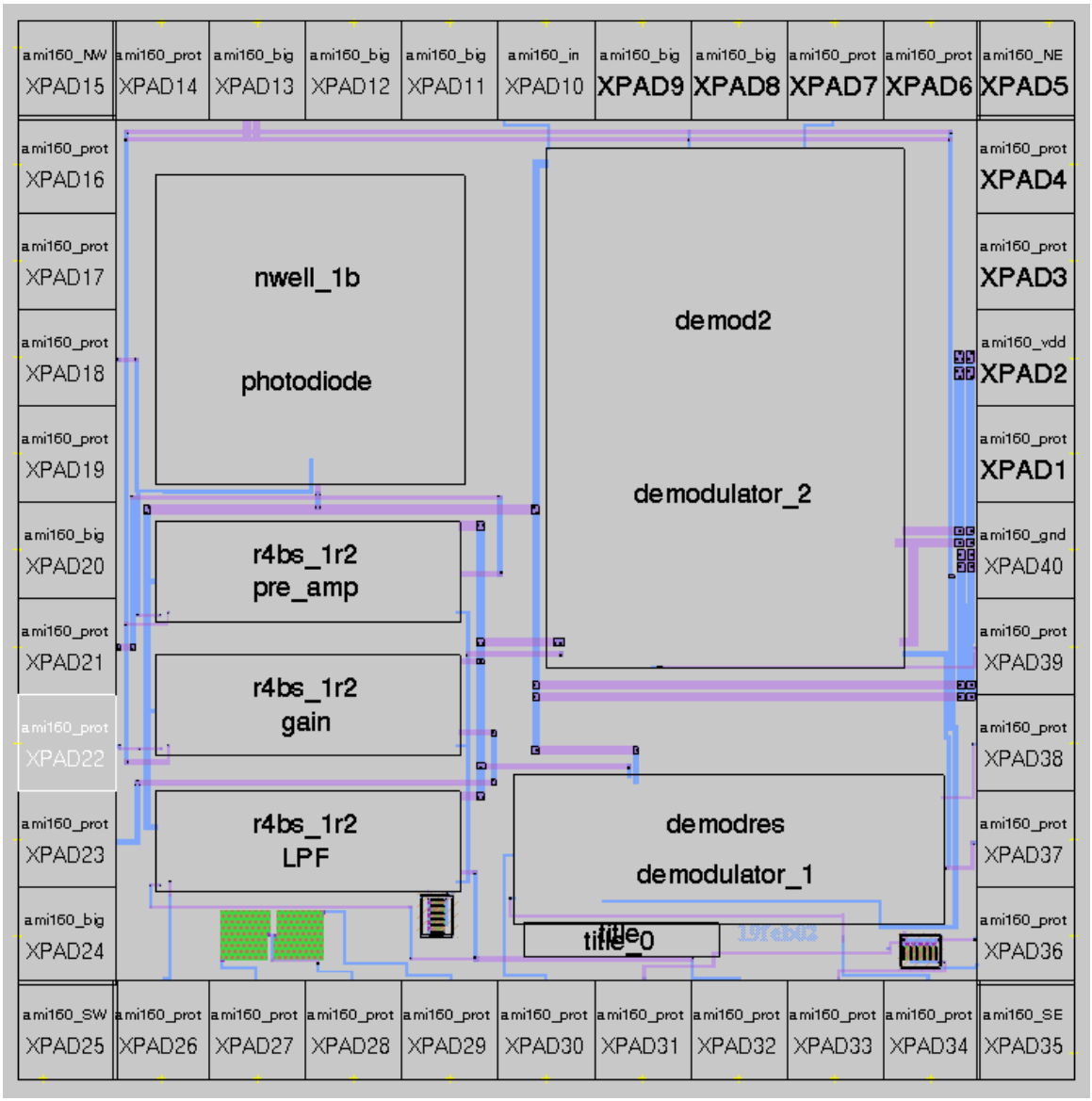

Figure 4.5.2 Representation of the blocks for the demodulator chip

The best way to prevent our chip from the outside effects such as bad connection effects is to use the elements inside of the chip. This way may not be possible for large value devices, such as MΩ level resistors or μF level capacitors, because of the area considerations. In this case, off-chip elements are preferable. 10 kΩ resistors must be used inside of the chip for the demodulator stages. Integrated resistors can be realized using a wide variety of different conductors. A popular choice is polysilicon. The equations governing the resistance are given by,

$R = \tilde{n}/t$ (4.5)

Where R is the resistance per square, or sheet resistance, and ρ is the resistivity

$$r = \frac{1}{qm_n N_D} \quad (4.6)$$

t is the thickness of the conductor, and N_D is the concentration of carriers. Then, the total resistance is given by

$R = (L / W) R$ *(4.7)*

where L is the length of the resistor. To make 10 kΩ resistor which is used for demodulator chip we need to find resistance value of per square for AMI 1.5 μm CMOS process:

$W / = 25$ *(4.8)*

If we choose W=4,

will be *4 X 4 = 16 unit*.

A unit resistance is equal to 25 Ω.

Then the general expression becomes

*(L / 4) * ( ) * (W /) = 10 kW* *(4.9)*

L = 1600 Þ

= 16 Þ

L =100 (figure 4.5.3 and 4.5.4).

One of the major problems in integrated CMOS circuits especially in switching circuits is latch-up. The result of this effect is the shorting of V_{DD} and V_{SS} lines, usually resulting in chip self-destruction or malfunctioning on the circuit. The best approach for preventing the latch-up is layout techniques, such as using guard rings. Guard rings that are p^+ diffusions in the p substrate and n^+ diffusions in the n-well are used to collect the injected minority carriers. P^+ guard rings must be tied to V_{ss} and n^+ guard rings must be tied to V_{dd} (figure 4.5.4)

The final step in integrated circuit fabrication is packaging to protect the device from its environment. DIP (Dual In-line Package) packaging type, in which 40 connectors are brought out along two sides, was used.

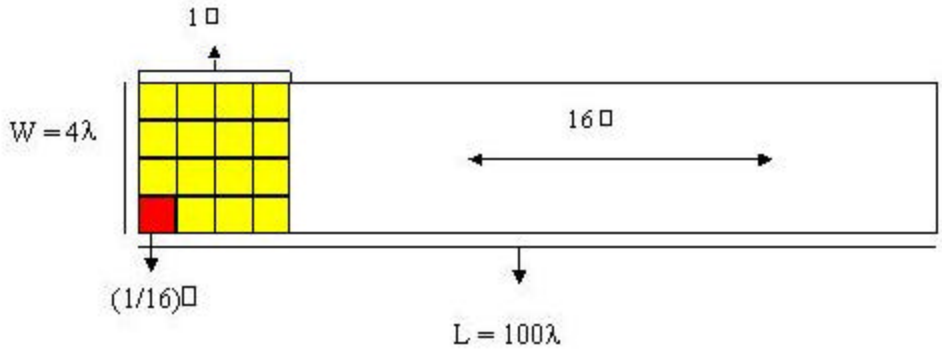

Figure 4.5.3 Polysilicon resistor layout for the demodulator chip

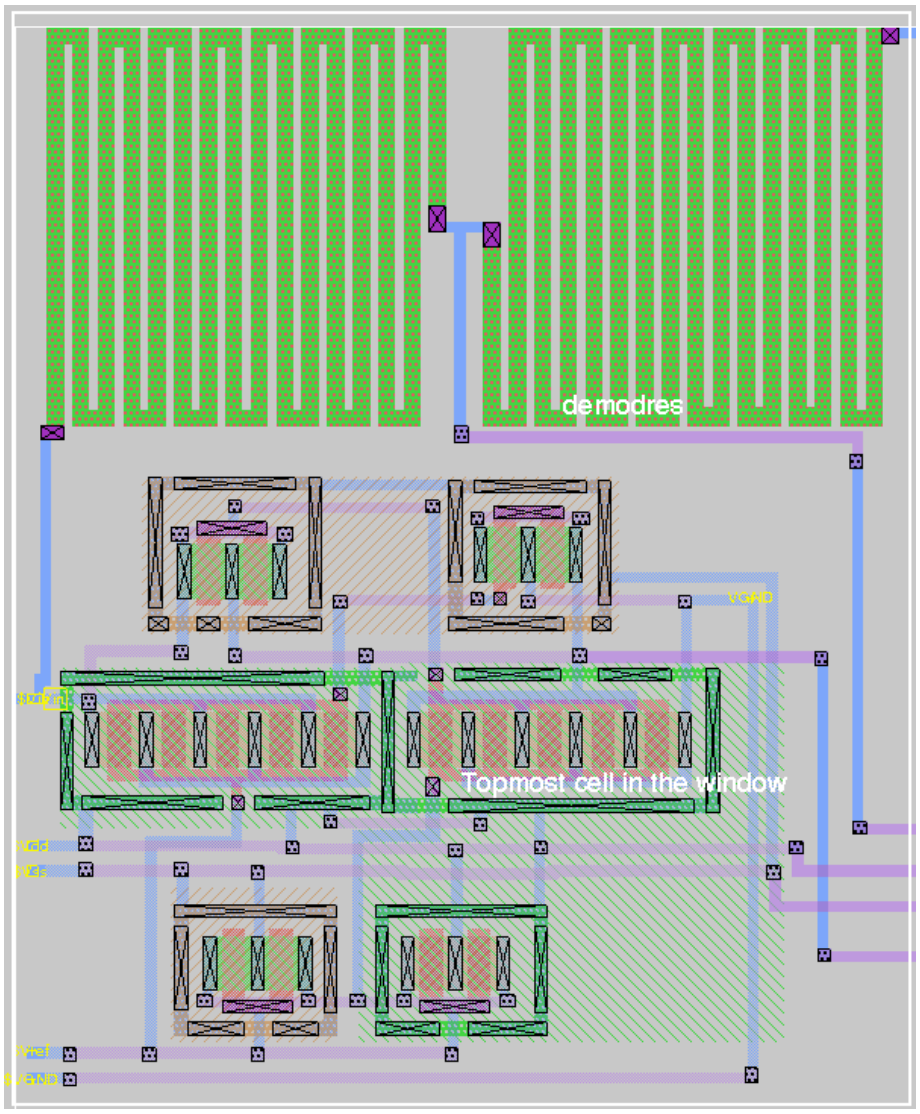

Figure 4.5.4 Representation of the switches, guard rings and resistors for the demodulator chip

Table 4.1 displays the area of each block used in the demodulator chip. The area of the first demodulator is 0.278 mm^2 while the area of the second demodulator is 0.799 mm^2. Thus, demodulator_1 is more efficient for the future implementations due to its size advantage. Table 4.2 summarizes the general specifications of each block. The input offset voltage is different for each stage because closed loop response is not the same for each block.

Table 4.1 Area of the stages

Stages	**Area**
Photodiode	640 μm * 640 μm (0.4096 mm^2)
R4BS Op-Amp	208.8 μm * 630.4 μm (0.1306 mm^2)
Demodulator_1	310.4 μm * 895.2 μm (0.278 mm^2)
Demodulator_2	742.4 μm * 1076 μm (0.799 mm^2)
Total Chip	2195 μm * 2195 μm (4.819 mm^2)

Table 4. 2 Specifications of the stages, which are used in the demodulator chip

CIRCUIT	GAIN	BANDWIDTH (Lab)	INPUT OFFSET (Lab)	SUPPLY CURRENT (HSPICE)
Pre_amp	350 kV/A	≈ 75 kHz	3 mV	
Gain	100	≈ 50 kHz	5 mV	1.545 mA
Demodulator 1	1	≈ 30 kHz	1.1 mV	1.562 mA
Demodulator 2	1	≈ 30 kHz	1.3 mV	1.794 mA
Low Pass Filter	1	≈ 32 Hz	0.5 mV	0.624 mA

Chapter 5

Conclusions and Future Work

This research is concerned primarily with two topics; optimizing the lock-in amplifier system and comparing the two different demodulators, which are used in the chip. The lock-in amplifier or the phase sensitive detector was used for signal recovery. Its ability is to measure weak signals embedded in noise. Performed tests inform that each block of the lock-in amplifier system is functioning according to the design requirements. One of the most useful characteristics is its capability of operating at supply voltages as low as ± 2.5 V. Because integrated analog circuitry is getting smaller, it becomes more difficult to modify the technology for analog needs. Therefore, modification of analog integrated circuits is necessary to operate at low voltage.

The fabricated prototype performance was reported in this thesis. Many aspects of the design can be reexamined and improved in future works. In spite of the success of the demodulator chip, couple of characteristics of the implement needs further investigation and improvement.

First, due to R4BS op-amp input offset voltage, the gain of the input signal is leading 100 times bigger than that of input offset voltage. Hence, to make zero or relax this offset voltage, it is necessary to use offset arrangement circuit outside of the chip.

Connecting variable resistor, around 5 kΩ, to the V_{dd} pin of the op-amp can easily do it. Nulling the output voltage in this manner removes the effects of input offset voltage.

Second, the charge injection issue of the CMOS switches during the switching requires additional work such as scaling or minimizing the transistors.

Another problem is encountering the oscillation in the system during the switching. Several reasons such as usage of long connection cables and difficulties with sending both reference signal and input signal to the demodulator exactly at the same time lead to the oscillation. This especially occurs when reference signal was applied to the demodulator. A comparator must be used just before the demodulator for timing relaxation or catching the exact same reference signal a. Hence, a comparator designed for the integrated circuits should be replaced inside of the chip.

Even though, both synchronous demodulators have almost same accuracy and reliability, first demodulator takes less area. So, it will be recommended for future works.

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Appendix

1. Demodulator Chip HSpice Files

```
.SUBCKT AMI160PAD 1
C1 1 0 198.6FF
.ENDS
.SUBCKT AMI160PADC 1
C1 1 0 270.7FF
.ENDS
.SUBCKT ami160_SE PAD Vss! Vssg
XPAD PAD AMI160PADC
C1 Vss! 0 170.9FF
C2 PAD 0 162.1FF
C3 PAD Vss! 168.5FF
.ENDS
.SUBCKT ami160_SW PAD 3 5 Vdd! Vssg 9
XPAD PAD AMI160PADC
C1 9 0 1.3FF
C2 Vdd! 0 36.5FF
C3 PAD 0 194.0FF
C4 5 0 12.6FF
C5 3 0 2.3FF
C6 Vdd! 3 1.4FF
C7 PAD 5 8.9FF
.ENDS
.SUBCKT ami160_gnd PAD 3 Vdd!
XPAD PAD AMI160PAD
C1 Vdd! 0 180.4FF
C2 PAD 0 250.4FF
C3 3 0 14.3FF
C4 PAD Vdd! 113.2FF
C5 PAD 3 6.8FF
.ENDS
.SUBCKT ami160_vdd PAD Vss!
XPAD PAD AMI160PAD
C1 Vss! 0 263.6FF
C2 PAD 0 202.8FF
C3 PAD Vss! 173.0FF
.ENDS
.SUBCKT ami160_NE PAD 4 6 Vdd! Vssg 12
XPAD PAD AMI160PADC
C1 12 0 2.0FF
C2 Vdd! 0 35.0FF
C3 PAD 0 188.9FF
C4 6 0 12.3FF
C5 4 0 1.9FF
```

```
C6 PAD 6 8.7FF
C7 Vdd! 12 1.2FF
C8 4 Vdd! 1.1FF
.ENDS
.SUBCKT ami160_in INunb Vss! IN Vdd! Vssg
XPAD INunb AMI160PAD
M1N INunb Vss! Vss! Vss! CMOSN M=10 W=12.80U L=1.60U AD=217.60P
M1P INunb Vdd! Vdd! Vdd! CMOSP M=10 W=19.20U L=1.60U AD=110.59P
M7N INb INunb Vss! Vss! CMOSN M=2 W=8.00U L=1.60U AD=19.20P PD=12.80U
M7P INb INunb Vdd! Vdd! CMOSP M=2 W=19.20U L=1.60U AD=46.08P PD=24.00U
M8N IN INb Vss! Vss! CMOSN M=2 W=16.00U L=1.60U AD=38.40P PD=20.80U
M8P IN INb Vdd! Vdd! CMOSP M=2 W=38.40U L=1.60U AD=92.16P PD=43.20U
C1 Vssg 0 37.0FF
C2 Vdd! 0 154.9FF
C3 IN 0 5.7FF
C4 Vss! 0 192.9FF
C5 INunb 0 135.8FF
C6 INb 0 14.7FF
C7 Vdd! Vss! 1.4FF
C8 Vdd! IN 5.5FF
C9 Vss! IN 6.1FF
C10 Vdd! INb 7.8FF
C11 Vss! INb 11.0FF
C12 Vdd! INunb 55.2FF
C13 Vss! INunb 144.7FF
.ENDS
.SUBCKT ami160_big PAD 3 Vss! Vdd!
XPAD PAD AMI160PAD
C1 Vdd! 0 217.8FF
C2 Vss! 0 231.4FF
C3 PAD 0 82.2FF
C4 3 0 17.7FF
C5 Vss! PAD 136.6FF
C6 Vdd! PAD 116.5FF
.ENDS
.SUBCKT ami160_prot PAD Vss! Vdd! Vssg
XPAD PAD AMI160PAD
M1N PAD Vss! Vss! Vss! CMOSN M=10 W=12.80U L=1.60U AD=101.10P
M1P PAD Vdd! Vdd! Vdd! CMOSP M=10 W=19.20U L=1.60U AD=55.00P
M2N PAD Vss! Vss! Vss! CMOSN M=6 W=8.00U L=1.60U AD=63.19P PD=37.38U
M2P PAD Vdd! Vdd! Vdd! CMOSP M=6 W=17.60U L=1.60U AD=50.42P PD=22.99U
C1 Vssg 0 34.2FF
C2 Vdd! 0 152.6FF
C3 Vss! 0 224.0FF
C4 PAD 0 116.0FF
```

```
C5 Vssg PAD 7.6FF
C6 Vss! PAD 202.1FF
C7 PAD Vdd! 145.8FF
C8 PAD Vss! 9.4FF
C9 Vss! PAD 8.9FF
.ENDS
.SUBCKT ami160_NW PAD 4 Vss!
XPAD PAD AMI160PADC
C1 PAD 0 157.6FF
C2 Vss! 0 164.2FF
C3 Vss! PAD 168.3FF
.ENDS
.SUBCKT demod 1 3 4 5 VGND 7
M1 4 2 3 1 CMOSN M=2 W=13.60U L=5.60U AD=65.28P PD=36.80U AS=54.40P
M2 3 5 VGND 1 CMOSN M=2 W=13.60U L=5.60U AD=54.40P PD=28.40U
M3 4 5 3 7 CMOSP M=5 W=13.60U L=5.60U AD=58.75P PD=24.96U AS=58.75P
M4 3 2 VGND 7 CMOSP M=5 W=13.60U L=5.60U AD=58.75P PD=24.96U
M5 2 5 1 1 CMOSN M=2 W=13.60U L=5.60U AD=65.28P PD=36.80U AS=43.52P
M6 2 5 7 7 CMOSP M=2 W=13.60U L=5.60U AD=65.28P PD=36.80U AS=43.52P
C1 5 0 80.4FF
C2 3 0 38.9FF
C3 2 0 59.3FF
C4 VGND 0 57.8FF
C5 1 0 53.6FF
C6 7 0 40.8FF
C7 4 0 20.5FF
C8 4 5 2.3FF
C9 7 5 2.2FF
C10 VGND 2 2.3FF
C11 5 3 4.9FF
C12 4 2 2.2FF
C13 5 2 4.5FF
C14 3 2 2.9FF
.ENDS
.SUBCKT demod2a 1 3 4 5 6 7
M1 4 2 3 1 CMOSN M=2 W=13.60U L=5.60U AD=65.28P PD=36.80U AS=43.52P
M2 6 5 3 1 CMOSN M=2 W=13.60U L=5.60U AD=65.28P PD=36.80U AS=43.52P
M3 4 5 3 7 CMOSP M=5 W=13.60U L=5.60U AD=58.75P PD=24.96U AS=58.75P
M4 6 2 3 7 CMOSP M=5 W=13.60U L=5.60U AD=58.75P PD=24.96U AS=58.75P
M5 2 5 1 1 CMOSN M=2 W=13.60U L=5.60U AD=65.28P PD=36.80U AS=43.52P
M6 2 5 7 7 CMOSP M=2 W=13.60U L=5.60U AD=65.28P PD=36.80U AS=43.52P
C1 5 0 81.0FF
C2 3 0 41.5FF
C3 2 0 59.9FF
C4 1 0 53.7FF
```

```
C5 7 0 50.3FF
C6 6 0 30.6FF
C7 4 0 21.0FF
C8 4 5 2.3FF
C9 7 5 1.5FF
C10 6 2 2.7FF
C11 5 3 2.7FF
C12 7 3 1.3FF
C13 5 6 2.4FF
C14 4 2 2.2FF
C15 5 2 4.5FF
C16 3 2 2.6FF
.ENDS
.SUBCKT r4bs_v1 3 INN 8 9 INP 110
C1 1 8 CAPAMI1r6 SCALE=6594.56
*C1=3956.74FF
C2 30 7 CAPAMI1r6 SCALE=4193.28
*C2=2515.97FF
C_C1 8 Vsub! CAPAMI1r6P SCALE=6594.56
*C_C1=85.73FF
C_C2 7 Vsub! CAPAMI1r6P SCALE=4193.28
*C_C2=54.51FF
vsub vsub! 0 dc 0
M1 4 INN 10 110 CMOSN M=4 W=33.60U L=4.00U AD=80.64P PD=38.40U
M2 5 INP 10 110 CMOSN M=4 W=33.60U L=4.00U AD=80.64P PD=38.40U
M3 4 20 3 3 CMOSP M=4 W=16.80U L=6.40U AD=46.06P PD=23.69U AS=45.31P
M4 5 20 3 3 CMOSP M=4 W=16.80U L=6.40U AD=40.32P PD=19.92U AS=45.31P
M5 20 20 3 3 CMOSP M=4 W=16.80U L=6.40U AD=40.32P PD=21.60U AS=45.31P
M6 8 5 3 3 CMOSP M=28 W=27.20U L=4.00U AD=71.50P PD=36.34U AS=73.36P
M7 21 21 3 3 CMOSP M=5 W=27.20U L=4.00U AD=73.98P PD=38.08U AS=73.36P
M8 5 110 1 3 CMOSP M=2 W=44.00U L=2.40U AD=105.60P PD=52.16U AS=176.00P
M9 7 7 110 110 CMOSN M=28 W=27.20U L=4.00U AD=71.50P PD=36.34U
M10 8 7 110 110 CMOSN M=28 W=27.20U L=4.00U AD=71.50P PD=36.34U
M11 30 110 4 3 CMOSP M=3 W=40.00U L=2.40U AD=117.33P PD=59.20U
M12 10 9 110 110 CMOSN M=5 W=27.20U L=5.60U AD=82.65P PD=43.33U
M20 20 21 22 110 CMOSN M=10 W=26.40U L=4.00U AD=71.81P PD=37.12U
M21 3 5 22 110 CMOSN M=5 W=26.40U L=4.00U AD=71.81P PD=37.12U
M22 3 4 22 110 CMOSN M=5 W=26.40U L=4.00U AD=71.81P PD=37.12U
M23 21 9 110 110 CMOSN M=5 W=27.20U L=5.60U AD=73.98P PD=38.08U
M24 22 9 110 110 CMOSN M=5 W=27.20U L=5.60U AD=73.98P PD=38.21U
M25 7 4 3 3 CMOSP M=28 W=27.20U L=4.00U AD=71.50P PD=36.34U AS=73.36P
C3 9 0 98.3FF
C4 8 0 230.5FF
C5 7 0 358.2FF
C6 5 0 217.1FF
```

```
C7 4 0 206.5FF
C8 1 0 6.8FF
C9 INP 0 33.1FF
C10 INN 0 33.5FF
C11 3 0 458.4FF
C12 30 0 14.9FF
C13 22 0 79.9FF
C14 21 0 65.9FF
C15 20 0 95.3FF
C16 10 0 42.2FF
C17 110 0 467.5FF
C18 10 INP 1.3FF
C19 20 4 1.8FF
C20 22 5 1.3FF
C21 110 7 12.3FF
C22 110 21 1.0FF
C23 22 3 3.1FF
C24 10 INN 1.3FF
C25 20 22 1.7FF
C26 4 22 1.3FF
C27 9 22 1.0FF
C28 10 110 7.3FF
C29 110 3 6.5FF
C30 3 21 3.0FF
C31 9 110 59.1FF
C32 4 7 2.2FF
C33 5 3 26.2FF
C34 8 7 3.3FF
C35 9 21 1.0FF
C36 4 5 1.8FF
C37 8 5 2.6FF
C38 22 21 1.1FF
C39 20 3 4.2FF
C40 4 3 9.5FF
C41 10 9 3.4FF
C42 8 3 3.7FF
.ENDS
.SUBCKT demod_framea vdd demod2_in gnd pre_amp_inn pre_amp_out gain_inn
+ gain_out GNDa lpf_inp spare1 swclk1 nosource demod1_in reset Vout refmode
+ vref1 powerup_out Ibias demod1_vout demod2_vout 40
XPAD1 refsample GNDa vdd GNDa ami160_prot
XPAD2 vdd GNDa ami160_vdd
XPAD3 refbias GNDa vdd GNDa ami160_prot
XPAD4 vrefout2 GNDa vdd GNDa ami160_prot
XPAD5 GNDa vdd GNDa vdd GNDa vdd ami160_NE
```

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XPAD6 linregfb GNDa vdd GNDa ami160_prot
XPAD7 demod2_in GNDa vdd GNDa ami160_prot
XPAD8 linregoutA GNDa GNDa vdd ami160_big
XPAD9 linreginB GNDa GNDa vdd ami160_big
XPAD10 vref2 GNDa 40 vdd GNDa ami160_in
XPAD11 batteryB GNDa GNDa vdd ami160_big
XPAD12 batteryA GNDa GNDa vdd ami160_big
XPAD13 gnd GNDa GNDa vdd ami160_big
XPAD14 cmp5in GNDa vdd GNDa ami160_prot
XPAD15 vdd GNDa GNDa ami160_NW
XPAD16 cmp3in GNDa vdd GNDa ami160_prot
XPAD17 cmp2in GNDa vdd GNDa ami160_prot
XPAD18 pre_amp_inn GNDa vdd GNDa ami160_prot
XPAD19 cmpbias GNDa vdd GNDa ami160_prot
XPAD20 swout GNDa GNDa vdd ami160_big
XPAD21 pre_amp_out GNDa vdd GNDa ami160_prot
XPAD22 gain_inn GNDa vdd GNDa ami160_prot
XPAD23 gain_out GNDa vdd GNDa ami160_prot
XPAD24 swin1 GNDa GNDa vdd ami160_big
XPAD25 GNDa vdd GNDa vdd GNDa vdd ami160_SW
XPAD26 lpf_inp GNDa vdd GNDa ami160_prot
XPAD27 spare1 GNDa vdd GNDa ami160_prot
XPAD28 swclk1 GNDa vdd GNDa ami160_prot
XPAD29 nosource GNDa vdd GNDa ami160_prot
XPAD30 demod1_in GNDa vdd GNDa ami160_prot
XPAD31 reset GNDa vdd GNDa ami160_prot
XPAD32 Vout GNDa vdd GNDa ami160_prot
XPAD33 refmode GNDa vdd GNDa ami160_prot
XPAD34 vref1 GNDa vdd GNDa ami160_prot
XPAD35 vdd GNDa GNDa ami160_SE
XPAD36 powerup_out GNDa vdd GNDa ami160_prot
XPAD37 Ibias GNDa vdd GNDa ami160_prot
XPAD38 demod1_vout GNDa vdd GNDa ami160_prot
XPAD39 demod2_vout GNDa vdd GNDa ami160_prot
XPAD40 GNDa GNDa vdd ami160_gnd
Vbatterya       batterya        0       dc      0
Vbatteryb       batteryb        0       dc      0
Vlinreginb      linreginb       0       dc      0
Vlinregouta     linregouta      0       dc      0
Vswin1          swin1           0       d
Vswout          swout           0       dc      0
.ENDS
.SUBCKT r4bs_1r2 3 INN 8 9 INP 110
C1 1 8 CAPAMI1r6 SCALE=3727.36
*C1=2236.42FF
```

```
C2 30 7 CAPAMI1r6 SCALE=2042.88
*C2=1225.73FF
C_C1 8 Vsub! CAPAMI1r6P SCALE=3727.36
*C_C1=48.46FF
C_C2 7 Vsub! CAPAMI1r6P SCALE=2042.88
*C_C2=26.56FF
vsub vsub! 0 dc 0
M1 4 INN 10 110 CMOSN M=4 W=33.60U L=4.00U AD=80.64P PD=38.40U
M2 5 INP 10 110 CMOSN M=4 W=33.60U L=4.00U AD=80.64P PD=38.40U
M3 4 20 3 3 CMOSP M=4 W=16.80U L=6.40U AD=46.06P PD=23.69U AS=45.31P
M4 5 20 3 3 CMOSP M=4 W=16.80U L=6.40U AD=40.32P PD=19.92U AS=45.31P
M5 20 20 3 3 CMOSP M=4 W=16.80U L=6.40U AD=40.32P PD=21.60U AS=45.31P
M6 8 5 3 3 CMOSP M=28 W=27.20U L=4.00U AD=71.50P PD=36.34U AS=73.36P
M7 21 21 3 3 CMOSP M=5 W=27.20U L=4.00U AD=73.98P PD=38.08U AS=73.36P
M8 5 110 1 3 CMOSP M=2 W=44.00U L=2.40U AD=105.60P PD=52.16U AS=176.00P
M9 7 7 110 110 CMOSN M=28 W=27.20U L=4.00U AD=71.50P PD=36.34U
M10 8 7 110 110 CMOSN M=28 W=27.20U L=4.00U AD=71.50P PD=36.34U
M11 30 110 4 3 CMOSP M=3 W=40.00U L=2.40U AD=117.33P PD=59.20U
M12 10 9 110 110 CMOSN M=5 W=27.20U L=5.60U AD=82.65P PD=43.33U
M20 20 21 22 110 CMOSN M=10 W=26.40U L=4.00U AD=71.81P PD=37.12U
M21 3 5 22 110 CMOSN M=5 W=26.40U L=4.00U AD=71.81P PD=37.12U
M22 3 4 22 110 CMOSN M=5 W=26.40U L=4.00U AD=71.81P PD=37.12U
M23 21 9 110 110 CMOSN M=5 W=27.20U L=5.60U AD=73.98P PD=38.08U
M24 22 9 110 110 CMOSN M=5 W=27.20U L=5.60U AD=73.98P PD=38.21U
M25 7 4 3 3 CMOSP M=28 W=27.20U L=4.00U AD=71.50P PD=36.34U AS=73.36P
C3 9 0 93.8FF
C4 8 0 223.2FF
C5 7 0 349.4FF
C6 5 0 210.2FF
C7 4 0 193.7FF
C8 1 0 6.8FF
C9 INP 0 33.1FF
C10 INN 0 33.5FF
C11 3 0 449.6FF
C12 30 0 14.9FF
C13 22 0 79.9FF
C14 21 0 65.9FF
C15 20 0 95.3FF
C16 10 0 42.2FF
C17 110 0 451.1FF
C18 21 3 3.0FF
C19 4 20 1.8FF
C20 21 9 1.0FF
C21 110 21 1.0FF
C22 22 3 3.1FF
```

```
C23 10 INN 1.3FF
C24 10 9 3.4FF
C25 110 10 7.3FF
C26 INP 10 1.3FF
C27 22 9 1.0FF
C28 22 5 1.3FF
C29 20 22 1.7FF
C30 4 22 1.3FF
C31 3 5 19.0FF
C32 110 3 6.5FF
C33 8 3 2.3FF
C34 20 3 4.2FF
C35 4 3 9.5FF
C36 110 9 51.7FF
C37 21 22 1.1FF
C38 110 7 11.2FF
C39 8 5 2.6FF
C40 8 7 3.3FF
C41 4 5 1.8FF
C42 4 7 2.2FF
.ENDS
.SUBCKT demodres Vdd Vout Ibias Vss Vin Vref VGND
X1 Vdd 2 Vout Ibias 5 Vss r4bs_1r2
X2 Vss 5 Vin Vref VGND Vdd demod
M1 Ibias Ibias Vss Vss CMOSN M=5 W=27.20U L=5.60U AD=117.50P PD=41.28U
R1 Vin 2 RPYAMI1r6 SCALE=395.56
* R1=10284.6 (width=4.00U)
R2 2 Vout RPYAMI1r6 SCALE=395.56
* R2=10284.6 (width=4.00U)
C1 Vss 0 35.2FF
C2 2 0 40.9FF
C3 Vout 0 82.3FF
C4 Vdd 0 37.3FF
C5 5 0 16.5FF
C6 Vin 0 12.8FF
C7 Ibias 0 18.6FF
.ENDS
.SUBCKT demod2 Vdd Vout Ibias Vss Vref VGND Vin
X1 Vdd Vout Vout Ibias 4 Vss r4bs_1r2
X3 Vdd 9 8 Ibias VGND Vss r4bs_1r2
X4 Vdd 6 6 Ibias Vin Vss r4bs_v1
M1 Ibias Ibias Vss Vss CMOSN M=5 W=27.20U L=5.60U AD=117.50P PD=41.28U
R1 Vin 9 RPYAMI1r6 SCALE=395.56
* R1=10284.6 (width=4.00U)
R2 9 8 RPYAMI1r6 SCALE=395.56
```

```
* R2=10284.6 (width=4.00U)
C1 Vdd 0 501.6FF
C2 9 0 29.9FF
C3 Vss 0 463.5FF
C4 Vout 0 104.7FF
C5 Vref 0 10.4FF
C6 4 0 17.4FF
C7 VGND 0 13.5FF
C8 Vin 0 68.3FF
C9 6 0 154.0FF
C10 Ibias 0 330.6FF
C11 8 0 107.9FF
C12 Vss Vin 2.3FF
C13 Vss VGND 2.5FF
C14 Vref Vss 1.4FF
C15 Vin Vss 2.3FF
C16 VGND Vss 1.4FF
C17 6 Vss 1.7FF
C18 Vdd Vout 1.4FF
C19 Vdd Vss 1.2FF
C20 Vdd Ibias 5.1FF
.ENDS
.SUBCKT nwell_1b 1 101
C1 1 0 95.7FF
C2 101 0 844.9FF
C3 1 101 2.8FF
.ENDS
X1 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 demod_framea
X2 1 20 19 8 13 17 3 demodres
X3 1 15 15 19 9 8 r4bs_1r2
X4 1 21 19 8 22 3 2 demod2
X5 1 6 7 19 3 8 r4bs_1r2
X6 1 4 5 19 3 8 r4bs_1r2
X7 4 8 nwell_1b
M1 19 19 8 8 CMOSN M=5 W=27.20U L=5.60U AD=117.50P PD=41.28U
M2 14 18 16 8 CMOSN M=5 W=27.20U L=5.60U AD=117.50P PD=41.28U
R1 10 11 RPYAMI1r6 SCALE=395.56
* R1=10284.6 (width=4.00U)
R2 11 12 RPYAMI1r6 SCALE=395.56
* R2=10284.6 (width=4.00U)
C1 15 0 95.3FF
C2 12 0 56.8FF
C3 7 0 46.1FF
C4 11 0 42.6FF
C5 22 0 20.9FF
```

```
C6 9 0 18.2FF
C7 10 0 18.4FF
C8 14 0 57.2FF
C9 6 0 12.1FF
C10 16 0 31.8FF
C11 8 0 898.8FF
C12 2 0 16.5FF
C13 5 0 135.9FF
C14 18 0 46.6FF
C15 13 0 28.8FF
C16 8 4 2.9FF
C17 8 1 1.7FF
C18 8 3 15.0FF
C19 8 6 1.2FF
C20 8 21 2.6FF
C21 3 22 1.1FF
C22 4 5 1.2FF
C23 19 15 1.7FF
C24 7 1 15.5FF
C25 2 3 1.1FF
C26 8 4 1.2FF
C27 8 19 7.0FF
C28 8 7 5.4FF
C29 18 14 3.2FF
C30 7 19 4.8FF
C31 5 1 4.1FF
C32 8 5 6.9FF
C33 4 3 1.5FF
C34 19 3 1.9FF
C35 8 1 8.3FF
C36 19 1 11.5FF
C37 5 3 3.7FF
C38 8 19 5.4FF
C39 3 1 7.4FF
.MODEL RPYAMI1r6 R RES=26.0
.MODEL CAPAMI1r6P C CAP=0.013FF
.MODEL CAPAMI1r6 C CAP=0.600FF
```

Vita

Osman Oguz was born in Istanbul, Turkey on June 14, 1970. He attended public schools in Istanbul, Turkey. He graduated electrics-electronics department of Haydarpasa Technical High School in June 1988. He entered Yildiz Technical University at Istanbul in September 1988 and received Bachelor of Science degree in Electrical Engineering in August 1992. After graduating, he joined Turkish Air Force as a lieutenant officer in 3rd Air Base at Konya, Turkey until December 1994, then he joined Cihan Metal Company group in Izmit, Turkey as an electrical engineer. In September 2000, he was awarded a graduate research assistant position in the UT / ORNL Joint Graduate Program in the pursuit of a Master of Science degree in Electrical and Computer Engineering at the University of Tennessee at Knoxville.

He is married and has a 5-year old daughter.