12-2006

A High Gain Multi-Stage Operational Amplifier using Compound Transconductance Element

Chandra Sekhar Acharyulu Durisety
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a dissertation written by Chandra Sekhar Acharyulu Durisety entitled "A High Gain Multi-Stage Operational Amplifier using Compound Transconductance Element." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this dissertation and recommend its acceptance:

Charles L. Britton, Syed K. Islam, Vasilios Alexiades

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

To the Graduate Council:

I am submitting herewith a dissertation written by Chandra Sekhar Acharyulu Durisety entitled "A High Gain Multi-Stage Operational Amplifier using Compound Transconductance Element." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Benjamin J. Blalock

Major Professor

We have read this dissertation
and recommend its acceptance:

Charles L. Britton

Syed K. Islam

Vasilios Alexiades

Accepted for the Council:

Linda Painter

Interim Dean of the
Graduate School

(Original signatures are on file with official student records.)

A High Gain Multi-Stage Operational Amplifier using Compound Transconductance Element

A Dissertation
Presented for the
Doctor of Philosophy Degree

The University of Tennessee, Knoxville

Chandra Sekhar Acharyulu Durisety
December, 2006

Dedication

This dissertation is dedicated to my parents,
Adharvana Acharyulu, Aparna Devi
for their inspiration,
my brother Sankhyayana Acharyulu,
especially my wife Anjani and
my best friend Dharmaji Rao (Mava)
for their faith in me and their encouragement to reach higher and achieve my goals.

ACKNOWLEDGEMENTS

I feel privileged to be part of The University of Tennessee Integrated Circuits and Systems Laboratory (UT_ICASL) research group. It is beyond my words to convey the depth of my gratitude to my advisor Dr. Benjamin J. Blalock for his confidence and faith in me. I consider myself lucky to work with him as a graduate student. I wish to thank him for his patience, support and freedom he has given me throughout this work. I would like to express to him my deep gratitude for keeping me focused, for his precious time with thoughtful discussions and his helping hand during the many tough phases I have gone through during this research. In addition to the guidance, he was the best critic and helped me improve my written and verbal communication skills.

I am very thankful to Dr. Charles L. Britton for giving me his complete confidence and support right from the first day I presented him the idea. I am grateful to Dr. Syed K. Islam for providing me support through part of the research work. A special portion of my gratitude goes to my Committee for their valuable comments and support throughout this work.

I would like to express my deepest appreciation to my friend/colleague Steve Terry for his patience, criticism and suggestions on various technical issues. Those innumerable long discussions on many concepts are priceless. He has been my dependable source for quick clarifications on some concepts and helped me fix/correct many mistakes in both

content and style. Thanks to Suheng Chen for setting up the PDKs, developing various innovative pad-frames and helping me during the layout over the years. It has been of tremendous help as we were always tight on the available silicon area.

I also appreciate Dr. J. Douglas Birdwell and Dr. Tsewei Wang who helped me out of some technical hurdles at the beginning of the work. I would also thank Dr. Michael J. Roberts whose has advised me during the '*closing path'* of my research work. I appreciate Dr. Paul B. Crilly for being patient in explaining some of the basics of control systems, which were very useful in the analysis of higher-order systems.

A special thanks to Mark D. Hale for being a good critic during many conversations on ADCs and helping me during the test board design. In addition to learning circuit design techniques, I had a great time at ICASL, where I used to sleep overnights. I will miss the dart board competitions with Steve, Suheng and Mark. It's hard to forget the discussions we had on American culture and history. Friday lunch visits to El Charro on the strip with Dr.Blalock were great as we were lost in discussion and have to hurry back for the late noon (very long and of course, sleepy) telecons. It was great to work with Suheng, Mark, James D. Vandersand and Benjamin Prothro who do not look at the watches when in need. I greatly remember my biking trips with Dr. Blalock, Mark and Suheng, water skiing attempts during Steven Bunch's lake party, and ski trips with James.

Thanks to Tony Antonacci for developing the LabVIEW programs for characterizing the amplifiers and Robert Greenwell for giving me rides home during late hours. Thanks a lot to Rajagopal Vijayaraghavan for helping me out in the layout and being a great friend.

I cannot wait to show my thankfulness and gratitude to my best friend, Dharmaji Rao Killamsetti (Mava) who has encouraged me through my hard times. His encouragement and support has helped me make tough decisions in my life. Thanks to his wife Kalpana. I wish them a happy and successful future.

Thanks to all my friends, especially Prasanth S. Venkata, Chesp, Siddhartha, Siva Kali Prasad and definitely the elite 'thebachelors' who have been with me during my higher education.

I would like to thank my family for their hearty support and belief in me during my Ph.D. I am deeply indebted to my parents for the freedom they offered at various stages of my life so that I can fulfill my dreams. Thanks a lot to my brother Sankhyayana and my sister-in-law Vijai to share the responsibilities back at home, so that I have one less thing to worry about during my research. I owe a lot to my loving wife Anjani for being patient and understanding during the final stages of this work. Once again thanks to Dad, Mom, Annay, Vadina and Anjani for everything.

To Mom, Dad and Anjani– I love you.

Abstract

The rapid increase in integrated circuit complexity attributed to the advancements in fabrication techniques combined with the increasing demand for consumer applications has created an immense demand for high performance analog systems. These analog systems include high-resolution (≥ 14-bit) and/or high-speed (≥ 1 GHz) ADCs, high-linearity filters and power management circuits. The fundamental limitations in these systems are tied to the constraints imposed by the basic design elements that tend to include amplifiers and reference generators (voltage/current). With continued technology scaling, innovative circuits and design techniques are necessary in achieving high performance analog/mixed-signal systems.

The goal of this research is to develop an operational amplifier that readily provides high open-loop gain and gain-bandwidth product for implementing high-performance analog systems. As part of this research, a 'Compound Transconductance element' has been developed that offers high transconductance with low power consumption. Furthermore, this element can function as a key element in the implementation of a multi-stage amplifier. Thus, a compound transconductance element based operational amplifier has been developed that achieves an open-loop gain in excess of 100 dB. This high-gain amplifier is applicable to continuous-time and switched-capacitor applications that require high linearity. The unique characteristics of this circuit element not only create new avenues in multi-stage amplifier design but also foster the development of a unique compensation topology for achieving feedback stability. Fabricated in a 5-V/0.5-μm bulk

CMOS process, this amplifier achieves an open-loop gain of nearly 120 dB, with a unity-gain bandwidth of 15 MHz.

TABLE OF CONTENTS

List of Tables

List of Figures

1. Introduction

1.1 Technology trends in CMOS op amp circuit design

The International Technology roadmap for Semiconductors shows that the supply voltage for high-performance/low power analog design will be scaled down to 1.1 V [53] by 2009. Though the reduction in supply voltage is advantageous for digital design, in analog circuit design it becomes increasingly difficult to achieve the performance of a similar system fabricated in earlier processes. This is because most of the circuit techniques that are being used today may become unusable in the circuit designs targeting deep sub-micron processes. To keep pace with these future demands, new circuit techniques, process options and architectures have to be developed.

The operational amplifier (op amp) forms one of the basic components in analog design and is used in reference circuits, analog-to-digital converters (ADCs), voltage controlled oscillators (VCOs), etc. Some of the recent circuit techniques in op amp design include body driving [67], [68], [69], sub-threshold designs [70], [71], [72], [73], and floating-gate designs [74], [75], [76]. Some of the process options that are available in deep sub-micron processes that are not available in earlier processes are multi-threshold voltage devices (offered as thin-oxide and thick-oxide devices) and triple well devices (isolated bodies for both the PMOS and NMOS). Architecturally, there is not much advancement in op amp design, as the folded-cascode architecture has been widely used for more than a decade. The transconductance offered by a body-driven MOSFET is roughly three

times less than that of its gate-driven counter-part. Though sub-threshold designs are power efficient, typically they require large silicon area. The post-fabrication programmability option of floating-gate devices demands a complex programming setup and it can be impractical to program/reconfigure all the individual chips during volume production. The recent process options presented above need extra mask layers reducing the cost efficiency of the fabrication. Though these circuit techniques and process options have their own disadvantages, their advantages are still significant and help in the implementation of designs to meet future demands. This work shows the potential of circuit techniques in developing high performance designs.

1.2 Research goals

The goals of this research are:

- to investigate efficient methods of achieving high gain for a given power consumption,
- to survey frequency compensation methodologies for multi-stage amplifiers, and
- to implement a fully functional high-gain multi-stage operational amplifier combining both the above methodologies.

As a part of this effort, a thorough literature survey has been done on multi-stage amplifiers and their compensation topologies to understand and analyze the problems associated with their design methodologies and limitations. This literature survey has shown that frequency compensation methods have come a long way in furthering the

overall efficiency and performance of multi-stage amplifiers. Relatively speaking, the design of the core architecture used in multi-stage amplifiers has remained somewhat stagnant for more than a decade. To improve the efficiency of these multi-stage amplifiers, a compound transconductance element that offers very high transconductance using meager power consumption is developed. The inherent characteristics of this element make this an ideal candidate for implementing multi-stage amplifiers. To prove the viability of this element, a fully functional multi-stage operational amplifier has been designed and implemented in 0.5-μm, bulk CMOS process. The unique characteristics of this op amp demanded an innovative compensation topology for achieving stability. This is the first multi-stage operational amplifier to implement a completely stable all inverting gain stage amplifier. Furthermore, in terms of open-loop gain, small-signal bandwidth, slew-rate, power consumption, input common-mode range, power supply rejection ratio and common-mode rejection ratio, this amplifier is commensurate with performance from other multi-stage amplifiers that use alternate non-inverting gain stages–thus proving the viability of this compound transconductance element and the compensation topology in the implementation of multi-stage amplifiers.

1.3 Overview of the dissertation

This dissertation presents the design of a multi-stage amplifier that can be used in the implementation of high linearity systems. In Chapter 2, literature review of previous work on multi-stage amplifiers, their classification and various compensation topologies are discussed. This review clarifies the fact that an all inverting gain stage based multi-

stage amplifier has not been implemented and also discusses the various problems associated with compensation topologies. Chapter 3 starts with the thorough introduction of the compound transconductance element, the mathematical analysis behind its efficiency in generating high gain, the inherent behavior of the element as a multi-stage amplifier, the need for designing a compensation topology and simulation results of a fully functional multi-stage amplifier from Matlab and Eldo. Chapter 4 presents the implementation, layout of the multi-stage amplifier, printed circuit board developed for characterization, analysis of measured results compared with simulation results, performance comparison of this amplifier with other multi-stage amplifiers and tools used throughout this research. Finally, Chapter 5 concludes this dissertation with the original contributions from this work and future research directions of this compound transconductance based op amp.

2. Multi-Stage Op amp Prior Art

2.1 Classification of multi-stage amplifier architectures

High-gain amplifiers can be defined as amplifiers with open-loop gains higher than 100 dB. These amplifiers can be developed to operate in voltage mode as well as in current mode. All the amplifiers discussed in this work are in voltage mode. Throughout the course of this document, only the literature with measurement results is considered for discussion and analysis. The author broadly classifies these amplifiers in four types, depending on their design architecture. They are:

a) Cascode amplifiers

b) Cascade amplifiers

c) Dynamic amplifiers

d) Positive feedback or Negative conductance amplifiers

2.2 Analysis of multi-stage architectures

All the four multi-stage amplifier architectures classified in the previous section will be discussed in detail in this section. The stability and compensation techniques for these architectures will be discussed in the later sections.

2.2.1 Cascode amplifiers

Cascode amplifiers are used for capacitive loads only, where the output impedance is very high. These achieve high gain through a ‘stacking transistor’ technique, which

dramatically increases the output impedance. A simple differential amplifier is shown in the Figure 2.1 (a). The gain of this amplifier is given by

$$Gain = g_{m2} \times r_{024} \tag{1}$$

where g_{m2} is the transconductance of the input differential pair and r_{024} is the output impedance of the amplifier, given by $r_{02} \parallel r_{04}$. For a given transconductance, the gain of the amplifier can be further increased by the cascoding technique [62]. When the transistors ($M_{5/6}$ and $M_{7/8}$) are added in series with the input differential pair ($M_{2/1}$), the output impedance is increased tremendously. A single-stage operational transconductance amplifier (OTA) with cascode load is shown in the Figure 2.1(b) and its gain is given by

$$Gain_{cascode} = g_{m2} \times r_{0dc} \tag{2}$$

where g_{m2} is the transconductance of the input differential pair and r_{0dc} is the output impedance of the amplifier and is approximately given by $\left[\left(g_{m8}r_{08}r_{02}\right) \| \left(g_{m6}r_{04}r_{06}\right)\right]$. Thus the gain of cascode amplifier (Figure 2.1 (b)) can be orders of magnitude higher than simple amplifier (Figure 2.1 (a)). By cascoding further, the output impedance and therefore the gain can be increased further.

Though the cascoding technique steadily increases the open-loop gain of the single-stage amplifier, there is a steady decrease in the dynamic swing of the output signal and input common mode range (ICMR). The output impedance in combination with the load capacitance and the output parasitic capacitance form the dominant pole in this amplifier topology.

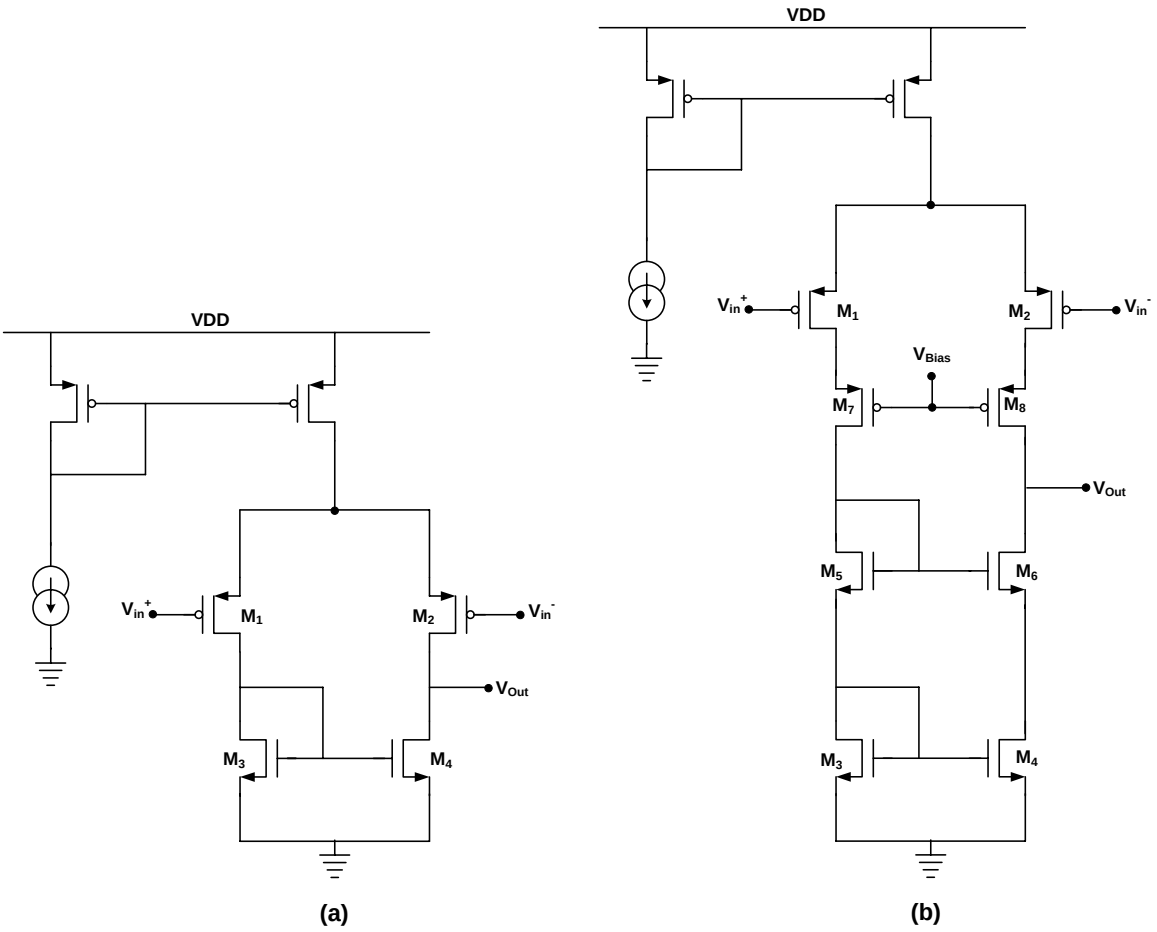

Figure 2.1 (a) Single-stage OTA and (b) Single-stage OTA with cascode load

To improve the performance characteristics of the single-stage OTA, the folded cascode architecture has been introduced by Banu *et. al* [6]. The basic topology of this amplifier is shown in Figure 2.2. This topology is referred as the folded cascode architecture because the active loads are folded down into the output branch and the output branch resembles the topology of the complementary cascode architecture. Hence, this architecture can achieve the gain of the previous cascode architecture (Figure 2.1 (b)), while improving the dynamic output swing and ICMR.

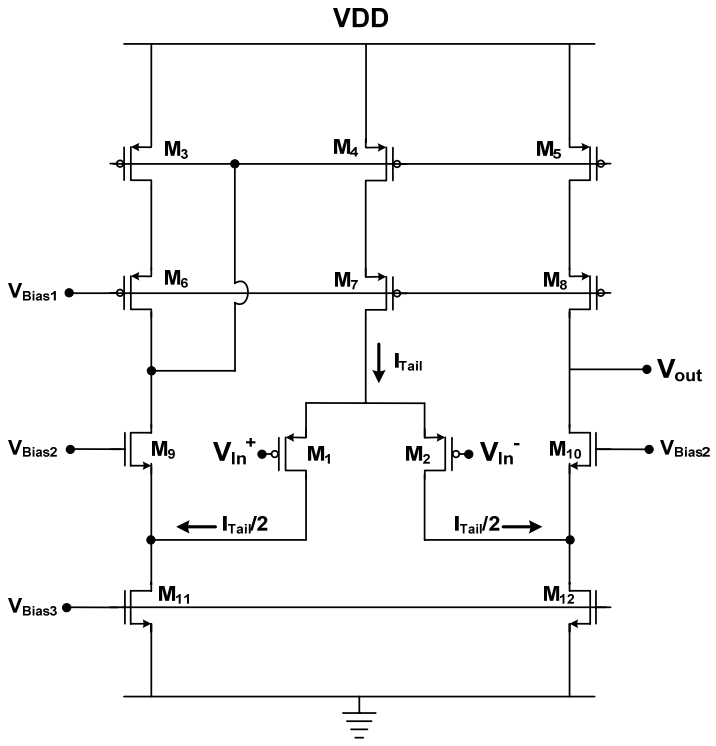

Figure 2.2. Single-stage OTA with Folded Cascode Topology

As semiconductor technology has migrated well into the deep submicron regime, supply voltages have gone down accordingly. These low voltage supplies limit the number of devices that can be stacked, thereby limiting the feasibility of this topology for future low voltage requirements.

2.2.2 Cascade amplifiers

This concept is based on cascading a series of low gain, low performance stages as to achieve the desired performance. Cascade amplifiers can be used not only for driving capacitive loads (like cascode amplifiers) but also for applications where low output impedance is desired. In cascode architectures, open-loop gain is achieved at the expense of dynamic output swing. With the advancements in semiconductor technology, the supply voltages for circuits and the channel length of the transistors have been reducing

rapidly. The reduction in the channel length reduces the output impedance of the transistor and hence the gain of the MOSFET-based amplifiers. Also, the cascode architectures cannot be readily facilitated with lower supply voltage. Hence a new architecture, wherein multiple stages are cascaded together in order to address these drawbacks has been developed.

The schematic of a 2-stage cascade amplifier is shown in Figure 2.3. The high impedance node at the output of the 1st stage, with the Miller and parasitic capacitances forms the dominant pole. The output of the 2nd stage with its load and parasitic capacitance forms the non-dominant pole. If external negative feedback is applied [24], the phase margin (PM) may not be sufficient as the non-dominant pole can be located within the unity-gain frequency (UGF). The open-loop transfer function and the unity-gain bandwidth product (UGBW) of the 2-stage cascade amplifier without the feedback capacitance C_M are given by

$$A_{OL} = \mathrm{A}_1\mathrm{A}_2 = \left(\frac{g_{m1}Z_{01}}{1+sR_1C_1}\right)\left(\frac{g_{m2}Z_{Load}}{1+sR_LC_L}\right), \Rightarrow \frac{g_{m1}Z_{01}g_{m2}Z_{Load}}{(1+sR_1C_1)(1+sR_LC_L)}. \tag{3}$$

$$UGBW = \frac{g_{m2}}{2\pi C_L} \tag{4}$$

where $g_{m1}, g_{m2}, R_1, R_L, C_1, C_L, Z_{01}$ and Z_{Load} represent transconductances, output resistances, output capacitances and output impedances for the 1st and 2nd stages, respectively.

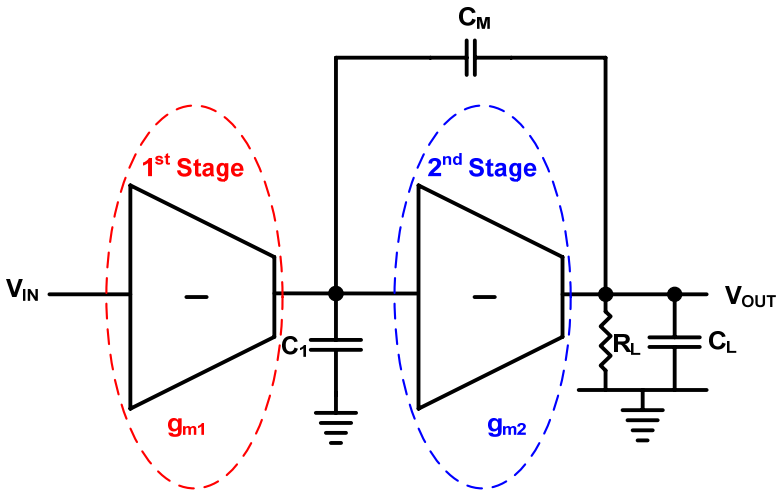

Figure 2.3. Two-stage Miller compensated cascade amplifier

The possible methods of frequency compensation [24], [44] are: a) move the non-dominant pole farther (higher in frequency) from the UGBW product, b) move the dominant pole (f_{-3dB}) lower in frequency such that non-dominant pole is outside the UGBW product, c) simultaneously move the dominant and non-dominant poles away from the UGF in opposite directions, or d) place a zero between the dominant and non-dominant pole to improve the PM or to precisely eliminate the non-dominant pole. Implementing the method recommended in (a) may not always be possible due to the design considerations. To implement the compensation using (b), the size of the output capacitance of the 1st stage (C_1) should be increased. But implementing such a large capacitor on chip would be highly area inefficient. Finally, the method recommended in (c) that achieves both (a) and (b) is analyzed in [5] and is implemented by placing a capacitor across the 2nd stage. This capacitor is referred to as a "Miller capacitor". The new transfer function, UBGW product and the new pole locations with the Miller capacitance are given by

$$A_{OL}(s) = \frac{A_{OL}\,|_{DC}\left(1-\frac{sC_M}{g_{m2}}\right)}{\left\{\left[1+sR_1\left(C_1+C_M\right)\right]\left[1+sR_L\left(C_L+C_M\right)\right]\right\}+\left[sg_{m2}C_MR_1R_L\left(1-\frac{sC_M}{g_{m2}}\right)\right]} \tag{5}$$

$$UGBW = \frac{g_{m2}}{2\pi C_M} \tag{6}$$

$$p_1' \cong \frac{1}{1+sR_1\left[C_1+C_M\left(1-A_2\right)\right]} \cong \frac{1}{1+sR_1C_M\left(1-A_2\right)} \; if \; C_1 << C_M \text{ and} \tag{7}$$
$$A_2 = -g_{m2}R_2$$

$$p_2' \cong \frac{1}{\left\{1+\frac{s^2R_1R_L\left[\left(C_1+C_M\right)\left(C_L+C_M\right)-C_M{}^2\right]}{sR_1C_M\left(1-A_2\right)}\right\}} \cong \frac{1}{1+s\frac{C_1C_L+C_M\left(C_1+C_L\right)}{g_{m2}C_M}}, \tag{8}$$
$$\text{if } C_1 << C_M, C_1 << C_L \text{ and } \left[R_1C_M\left(1-A_2\right)\right] >> \frac{C_1C_L+C_M\left(C_1+C_L\right)}{g_{m2}C_M}.$$

From (7) and (8), it can be clearly seen that the dominant pole (p_1') and the non-dominant pole (p_2') both moved away from the UGF by a factor of $\left(1-A_2\right)$. This is commonly referred to as "pole-splitting" [24]. Though this compensation simultaneously moves the dominant and non-dominant poles away from the UGF, it also introduces an undesired right-half plane (RHP) zero due to the feed-forward path at high frequencies. This RHP zero impacts the PM of the amplifier, which can be improved by adding a series resistor with Miller capacitor, effectively moving the zero from the RHP into the left-half plane (LHP). An efficient and more popular method is to eliminate the feed-forward path by placing a "virtual ground" node between the output of the 1st stage and the Miller capacitance. By properly placing the virtual ground, the RHP zero is completely eliminated from the transfer function, thus significantly improving the PM

and therefore stability of the system. This concept of eliminating the feed-forward zero by using virtual ground is widely used for compensating multi-stage amplifiers. This is also referred as "grounded-gate cascode compensation" [4]. Advanced compensation methodologies will be discussed later in this chapter.

By using Miller compensation capacitance a) the size of the compensation capacitor is reduced and the amplifier area is more efficient, and b) the amplifier has a higher slew-rate for the same power consumption.

In multi-stage amplifiers (where the number of stages ≥ 3), each stage can be individually optimized for a specific performance parameter thereby achieving an overall higher performance amplifier. Depending on the design requirements, the first stage could be optimized for

- low noise to improve the signal-to-noise ratio (SNR),
- high input impedance to avoid signal loss when a high impedance signal source drives the input node, and/or
- high ICMR to accommodate a wide range of signal amplitudes.

The second and intermediate stages could be optimized for

- high gain to further amplify the signal,
- signal conversion (single-ended to differential or vice-versa, voltage to current, etc.), and/or
- signal processing functions such as shifting the dc level of the input signal.

The final stage could be optimized for

- low output impedance to minimize signal transfer loss,
- large output swings, and/or
- drive capability for interfacing a wide range of loads.

The designer has to compromise or trade off certain performance parameters for others. In the present scenario, the desired performance parameters for the amplifiers using this topology are obtained at the cost of the complexity of the compensation architecture. The complexity of the compensation architecture increases with the number of stages. The schematic of a 3-stage amplifier with nested Miller compensation (NMC) [49] is shown in Figure 2.4, where g_{m1-3}, Z_{L1-3} and C_{M1-3} indicate the transconductance, output impedance and the Miller capacitance for each stage respectively.

The main disadvantages of the cascade topology are a) complexity of the compensation technique, b) chip area estate necessary for the compensation capacitors, and c) power

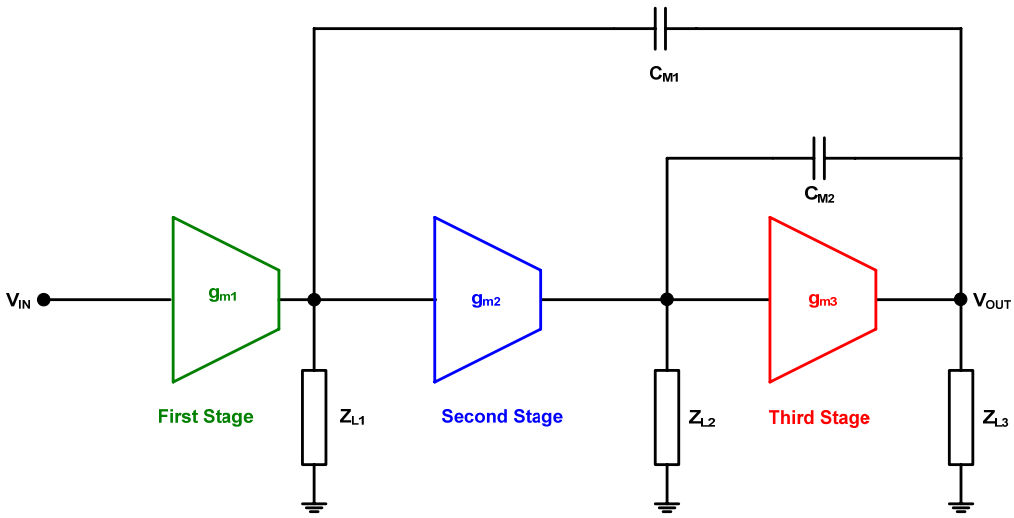

Figure 2.4. Block diagram of a 3-stage amplifier using nested Miller compensation

consumption needed for the multiple stages. A wide range of compensation techniques like simple Miller compensation (SMC) [5],[43], multi-path zero cancellation (MZC) [45], multi-path nested Miller compensation (MNMC) [48] and nested G_m-C compensation (NGCC) [46], [47] are used to optimize amplifier performance parameters such as bandwidth, power consumption and drive capability.

2.2.3 Dynamic amplifiers

The concept of dynamic amplifiers was proposed by Copeland [8]. The basic idea of this amplifier is to have a dynamically varying bias current instead of a constant bias current throughout the operation. These amplifiers are primarily targeted for extremely low power consumption and noise compared to continuous-time amplifiers. Very little literature is available in the area of dynamic amplifiers [8]-[10].

The concept of dynamic amplifiers is as follows. Initially the input differential pair is biased in strong inversion as in any other MOS op amp or OTA. Later the biasing of the input differential pair is continuously changed until the differential pair operates in the weak inversion region. Since the power consumption is minimal during sub-threshold operation, these amplifiers consume very little power compared to the previously discussed amplifiers. The basic operation of single-stage and 2-stage dynamic amplifiers is briefly discussed.

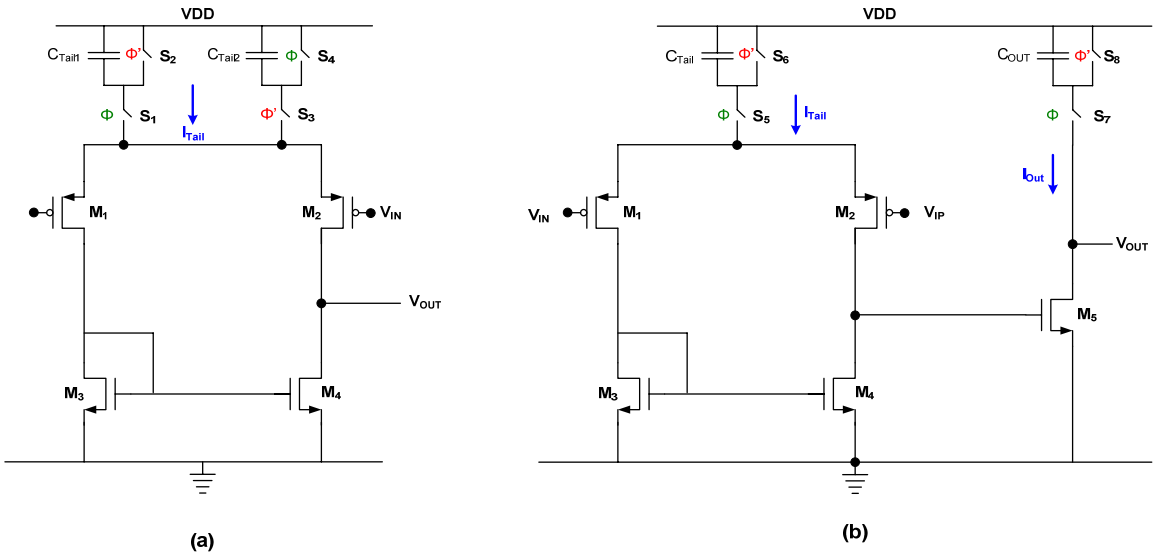

Figure 2.5. a) Single-stage dynamic amplifier [9] and b) 2-stage dynamic amplifier both with non-overlapping clock phases [9]

The schematics of single-stage and 2-stage dynamic amplifiers are shown in Figure 2.5. Assume Φ and Φ' are non-overlapping clocks and I_{Tail} is the tail current for the input differential pair. During phase-1 (when Φ is high and Φ' is low), switch S_1 is closed and switch S_2 is open and I_{Tail} is provided by the capacitor C_{Tail1}. At the end of the phase-1, the voltage across C_{Tail1} reaches close to VDD and I_{Tail} is reduced. During phase-2 (when Φ is low and Φ' is high), switch S_3 is closed and switch S_4 is open. Similar to the phase-1 operation, large current is provided at the start of phase-2 that is later reduced as the capacitor C_{Tail2} charges. During both the phases, the power consumption is highest at the start of the phase and gradually decreases to the end of the phase.

The operation of a 2-stage dynamic amplifier is slightly different from that of a single-stage dynamic amplifier. At the start of phase-1 (when Φ is high and Φ' is low), capacitors C_{Tail} and C_{Out} provide the currents necessary for the input differential pair and

output transistor M_5 respectively. As the capacitors C_{Tail} and C_{Out} start charging, the currents I_{Tail} and I_{Out} start reducing. During the phase-2 (when Φ is low and Φ' is high), both the capacitors start discharging and the output voltage and the amplifier is no longer usable. During phase-2, the amplifier consumes no power (except leakage).

The huge limitation of these amplifiers is that the bandwidth decreases drastically as the power consumption is reduced. Also, these amplifiers may be area inefficient because of the presence of on-chip capacitors per stage. With the increasing frequency of operation, the performance advantages offered by these amplifiers diminish as these amplifiers begin to operate more like continuous-time amplifiers.

2.2.4 Positive feedback or Negative conductance amplifiers

The positive feedback amplifiers are also referred to as negative conductance amplifiers. The concept of taking advantage of negative conductance to improve the gain of amplifiers was proposed by Allstot [13]. Figure 2.6 shows the schematic of a common source amplifier. The transfer function is given by

$$A_{OL}(s) = \frac{-g_m}{sC_L + \frac{1}{r_0} + \frac{1}{r_{neg}}} = \frac{-g_m}{sC_L + g_{ds,m1} + g_{neg}} \tag{9}$$

where g_m and r_0 correspond to the transconductance and output impedance of M_1, and r_{neg} represents the resistance of the element X_1.

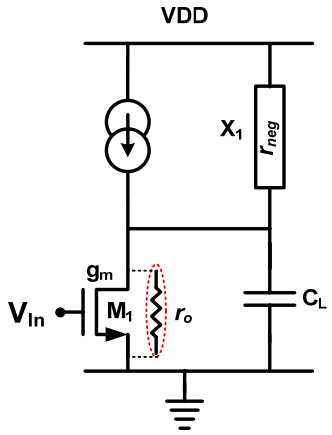

Figure 2.6. Schematic of a common source amplifier

The gain of the amplifier could be increased by canceling $g_{ds,m1}$, if the conductance (g_{neg}) of the impedance element is negative. Multiple methods have been proposed earlier to achieve negative conductance [14]-[16]. A schematic of a single-stage amplifier using negative conductance [17] is shown in Figure 2.7. The transfer function of this amplifier is given by

$$A_{OL}(s) \cong \frac{-g_{M_1}}{sC_L + \frac{1}{r_{01}} + \frac{1}{r_{02}} + \frac{(1-A_{Inner})}{r_{neg}}} = \frac{-g_{M_1}}{sC_L + g_{ds,M_1} + g_{ds,M_2} + g_{neg}(1-A_{Inner})} \tag{10}$$

By matching $(g_{ds,M_1} + g_{ds,M_2})$ with $g_{neg}(A_{Inner} - 1)$ so that they cancel each other, a very high dc gain could be theoretically achieved. In this topology, the negative conductance can be designed independently as to match the total output resistance. The main drawbacks of negative conductance amplifiers are that the a) gain is highly sensitive to the negative conductance and b) there is limited output swing [19].

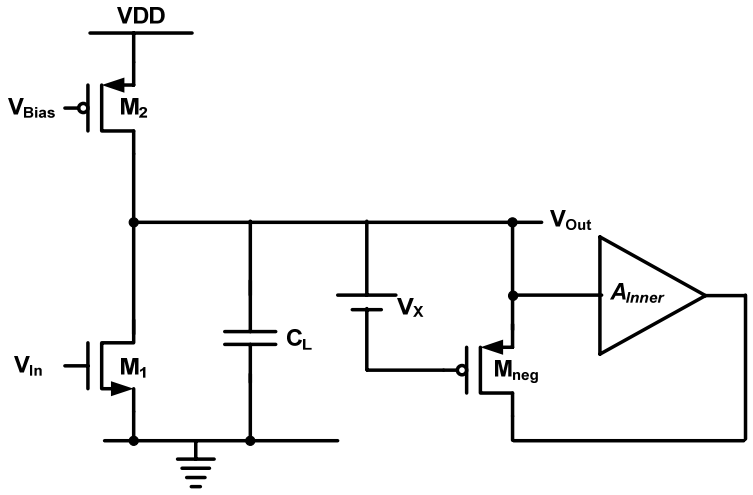

Figure 2.7. Schematic of a single-stage negative conductance amplifier

This is one of the least used architectures among all the classifications previously mentioned. Most of the literature published on positive feedback or negative conductance amplifiers is based on simulation results.

2.3 Compensation techniques

2.3.1 Necessity and motivation

The previous section discussed the necessity and demand for high-gain amplifiers and presented the classification of amplifier topologies. A challenging part of amplifier design and development is the compensation topology for achieving optimal performance. These compensation techniques evolved with the emergence of new amplifier topologies, since the stability of multi-stage amplifiers is a key concern for designers. With the increasing complexity of amplifier topologies (the open-loop transfer function of an uncompensated three-stage amplifier will have multiple poles and zeroes), the complexity of the compensation scheme increased proportionately. Very few

compensation techniques were published in the late 20th century, but with the rapidly shrinking supply voltage, cascade amplifiers have slowly gained prominence. With the increase in the number of gain stages in cascade amplifiers, the compensation topologies have become the major focus of the design. New techniques developed in the early 21st century show that the compensation techniques have a tremendous impact on various performance parameters of the amplifiers like slew-rate (SR), UGBW, PM, power consumption and the ability to drive both capacitive and resistive loads (primarily capacitive).

2.3.2 Analysis of different compensation techniques

One of the most widely used amplifier topologies (folded cascode) is based on the cascode technique, and the compensation techniques for this topology are well established. Hence this section briefly discusses the compensation techniques for cascode amplifiers before presenting the more complicated techniques.

Figure 2.1 (b) shows the schematic of a single-stage cascode amplifier. The output node of the amplifier forms the dominant pole for this system. The drain terminals of M_4, M_2 and M_1 produce the non-dominant poles of this amplifier. Load capacitance forms the compensation capacitance for this amplifier and has a significant impact on the UGBW and PM. Hence, it is important to carefully choose the size of the load capacitance.

Cascode architectures have been widely used when the available supply voltage is sufficiently high. The limitations of this architecture were discussed previously, and

cascading architectures have slowly gained prominence. The number of stages in cascade amplifiers increased with the demand for higher gains, and so does the complexity of their compensation schemes. The number of previously published multi-stage amplifiers is indicative of the complexity of the compensation topologies.

Table 2.1 provides a list of papers presenting various compensation techniques for multi-stage amplifiers. Throughout the discussion of this work, the minimum desired phase margin (PM) is 50º, unless otherwise specified.

Though the previously published compensation techniques shown in Table 2.1 are self-explanatory, the frequently referenced and widely used compensation techniques will be discussed and analyzed. The previously published multi-stage amplifier compensation topologies are categorized here based on the number of compensation capacitors used. Accordingly, the topologies can be classified into 3 broad categories: a) topologies with 2 or more compensation capacitors, b) topologies with single compensation capacitor, and c) topologies with no compensation capacitors. Most of the compensation topologies fall within the first category (i.e. with 2 or more compensation capacitors). For brevity, one topology from each category will be discussed in the subsequent sections.

The advantages and disadvantages of some of the basic widely used compensation topologies such as nested Miller compensation, multi-path nested Miller compensation,

Table 2.1. List of previously published papers on multi-stage amplifier compensation techniques

	Author	#. Stages	Gain (dB)	GBW (MHz)	SR^+ (V/µs)	SR^- (V/µs)	Supply (V)	Power (µW)	CM1/CM2 (pF)	C_L	PM (°)	Area (mm^2)	Tech. (µm)
1983	Ahuja	2	80	3.8	NA	NA	10*	NA	NA	15pF	70	165	4
1990	Opt Eynde	3	120	4.9	NA	NA	5*	NA	NA	15pF//81	58	0.28	2
1990	Bult	2	90	116	NA	NA	5	52000	NA	16pF	64	NA	1.6
1991	Fonderie	3	117	3.4	1.1	1.1	7.5	5250	NA	100pF//10KΩ	61	0.2	Bipolar
1992	Eschauzier	3	100	60	20	NA	8	76000	NA	100pF//1KΩ	40	1.8	Bipolar
1993	Pernici	4	120	2	1.5	NA	5	10000	17.5/5.0	250pF	NA	0.625	1.5
1994	Eschauzier	4	120	6	13	NA	1.5	435	0.5/1.3/1.3	10pF//10KΩ	69	NA	0.8
1997	Lahiji (Sims)	2	160	3.3	1	NA	NA	72000	NA	NA	NA	NA	Bipolar
1997	de Langden	3	76	1000	360	NA	3.6-5.5	86400	1.1/2.2	NA	47	0.26	Bipolar
1997	Fan You	4	100	1	5	NA	2*	1400	NA	20pF//10KΩ	58	0.22	2
1999	Hiok-Tiaq Ng	3	102	47	48	89	3	6900	NA	40pF	76	NA	0.6
2000	Ka Nang Leung	3	> 100	2.6	1.36	1.27	2	420	NA	100pF//25KΩ	43	0.11	0.8
2000	Ka Nang Leung	3	>100	0.82	0.31	0.4	1*	720	NA	1000pF	63	0.17	0.8
2001	Ka Nang Leung	3	> 100	1.8	0.82	0.75	2	406	NA	100pF//25KΩ	52	0.12	0.8
2002	Bouzerara	2	90	182	NA	NA	2.5	7000	NA	1pF	95	NA	0.8
2002	Mita(Sims. Only)	4	110	1.2	NA	NA	3	NA	NA	5pF	90	NA	NA
2002	Palumbo	3	>100	1.4	0.46	NA	2	NA	NA	100pF	91	NA	0.8
2003	Mita	3	91	4.5	NA	NA	1.5	NA	NA	NA	67	NA	NA
2003	Hoi Lee	3	> 100	4.5	2.2	0.78	2	400	7.0/3.0	120pF//25KΩ	65	0.06	0.8
2003	Bharat Thandri	2	90	250	NA	NA	2.5*	14000	None	12pF	> 50	0.16	0.5
2003	Hoi Lee	3	> 100	7	2.2	4.4	1.5	330	4.8/2.5	120pF//25KΩ	46	0.05	0.6
2004	Ramos	3	> 100	2.7	1	1	1.5*	275	NA	130pF//24KΩ	52	0.03	0.35
2004	Xiaohong Peng	3	> 100	1.89	0.2	1.2	2	316	NA	500pF	53	0.02	0.35
2005	Xiaohua Fan	3	> 100	9	4.8	2	2	410	4(One)	120pF//25KΩ	57	0.015	0.5
2005	Xiaohong Peng	3	> 100	2.85	0.96	1.11	1.5	45	1.1/0.92	150pF	58.6	0.02	0.35

and multi-path zero cancellation are discussed by Leung [27]. In this work more complicated compensation topologies like damping factor control frequency compensation (DFCFC), ac boosting compensation (ACBC) [29] and no capacitor feed-forward compensation (NCFF) [30] topologies are discussed. The earlier compensation topologies (primarily based on Miller compensation) have a tremendous impact on amplifier bandwidth and power consumption. This is readily understood from the fact that amplifier bandwidth is reduced by a factor of 2 for every Miller capacitor used [41]. Hence, the bandwidth of a single (i.e., one compensation capacitor) Miller compensated 2-stage amplifier has twice the bandwidth of the double Miller compensated 3-stage amplifier. The relationship is shown in the following equation:

$$BW_{no\_Miller} = 2 \times \left(BW_{single\_Miller}\right) = 2^2 \times \left(BW_{double\_Miller}\right) \tag{11}$$

This bandwidth limitation can be overcome by using various compensation topologies, some of which will be discussed below.

According to Leung [28], the bandwidth reduction in the nested Miller compensation is caused by the 2nd Miller capacitor, C_{M2} (Figure 2.4). Hence, the bandwidth can be improved by removing the nested Miller capacitor. But the absence of the 2nd Miller capacitor (C_{M2}) (a) causes "frequency peaking" close to the UGF, thereby affecting the stability of the multi-stage amplifier, and (b) reduces the magnitude of the damping factor (ζ) of the non-dominant poles from the open-loop transfer function. Leung's paper presents a method to improve the damping factor, thereby improving the stability and

bandwidth of this amplifier. This is achieved through the damping factor control (DFC) block that controls the damping factor of the non-dominant poles. The impact of damping factor can be understood from the following analysis. A typical second-order function is given by

$$non\text{-}dominant\ pole\ equation = 1 + s\left(\frac{2\zeta}{\omega_n}\right) + s^2\left(\frac{1}{\omega_n{}^2}\right) \tag{12}$$

A Matlab simulation of (12) for demonstrating the impact of damping factor is shown in Figure 2.8 for an open-loop gain of 110 dB and UGBW of 6 MHz. This shows that the peaking is inversely proportional to the damping factor, and the damping factor for which the peaking is avoided, is calculated to be $1/\sqrt{2}$. Figure 2.8 (a) shows simulation results over the complete frequency range, while Figure 2.8 (b) shows the zoom-in version of the same result.

The schematic of the DFCFC topology is shown in Figure 2.9 (i). Since there are two forms of DFCFC topologies ([28], [33]), the first case [28] is referred as DFCFC-I, while the other [33] is referred as DFCFC-II. From equation (20) in [28], the following can be derived:

$$BW_{NMC} = \frac{1}{4} \times BW_{no\_miller} \tag{13}$$

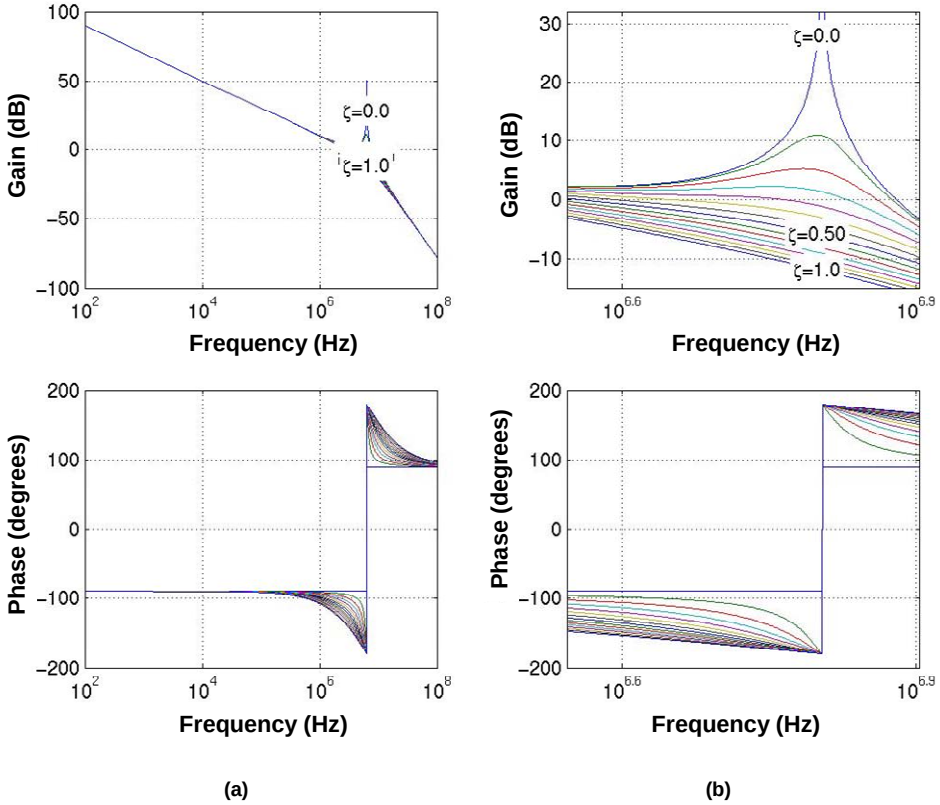

Figure 2.8. Matlab simulation of the transfer function for different damping factors showing the (a) complete frequency range and (b) zoom-in version

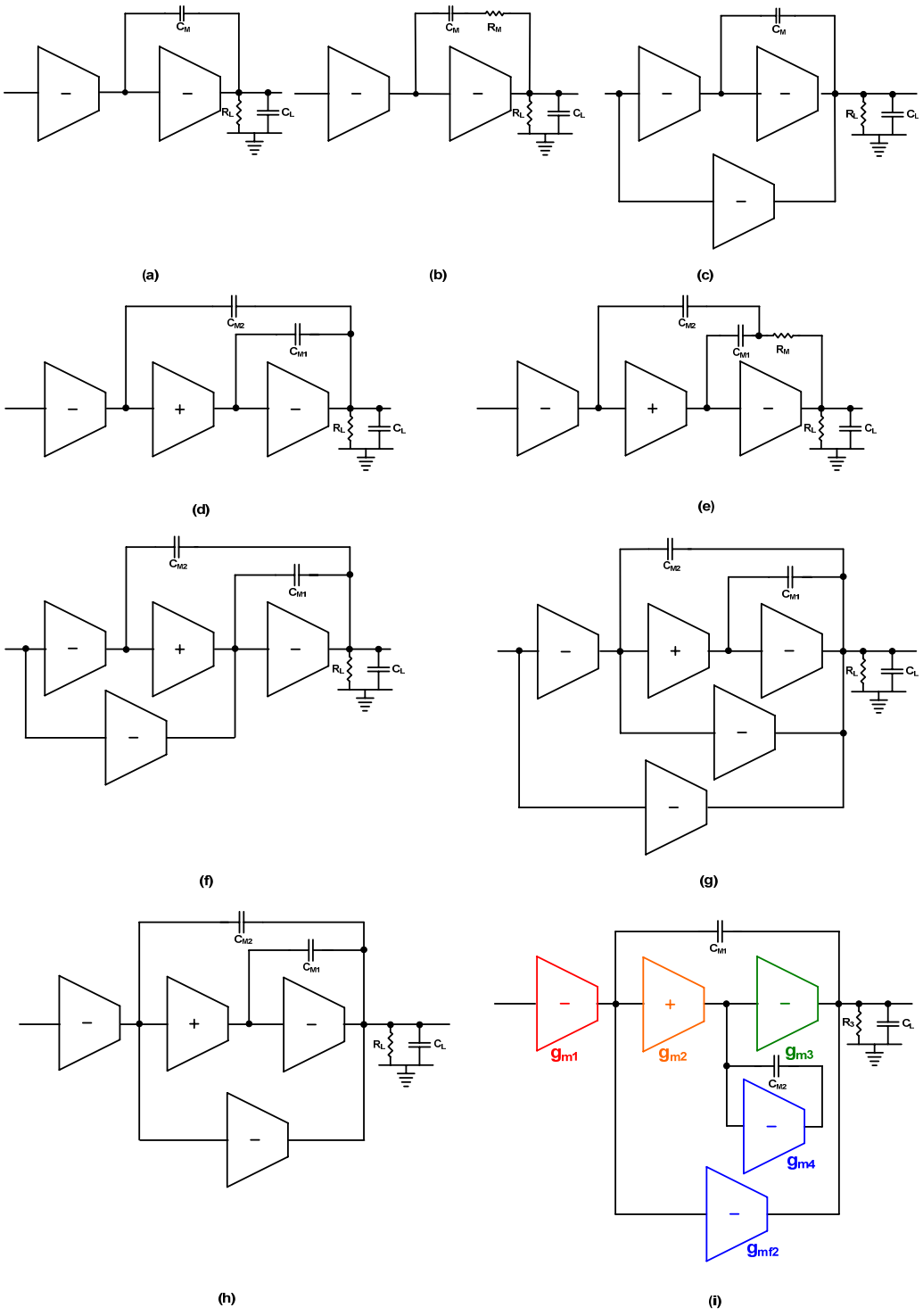

Figure 2.9. Schematics of the previously published compensation techniques for multi-stage amplifiers (a) SMC [5], [43] (b) SMCNR [50] (c) MZC [27] (d) NMC [49] (e) NMCFNR [41] (f) MNMC [48] (g) NGCC [46] (h) NMCF [27] (i) DFCFC-I [28]

$$BW_{DFCFC} = \left(\frac{1}{4} \times \frac{g_{m3}}{C_L}\right) \times \left(1 + \sqrt{\left(1 + 2\left(\frac{C_L}{C_{p2}}\right)\left(\frac{g_{m2} \times g_{m3}}{g_{mf2}^{\,2}}\right)\right)}\right) = BW_{NMC} \times \beta, \quad (14)$$

where $\beta = \left(1 + \sqrt{\left(1 + 2\left(\frac{C_L}{C_{p2}}\right)\left(\frac{g_{m2} \times g_{m3}}{g_{mf2}^{\,2}}\right)\right)}\right)$.

Mathematically, the bandwidth (BW) of the DFCFC based amplifier is equal to that of a nested Miller compensated amplifier for a β of unity. For $1 < \beta < 4$, the BW of DFCFC is smaller than that of a single-stage amplifier. For $\beta \geq 4$, the BW of DFCFC would be equal to or higher than that of a single-stage amplifier. The problems associated with this topology are a) that it is inefficient for driving small capacitive loads (i.e. advantageous only when driving heavy loads), b) increased power consumption compared to NMC, and c) complicated biasing scheme. Though this technique offers higher BW than NMC and the single-stage amplifier under certain conditions, it still needs compensation capacitors, though of smaller value than those used for NMC.

The topology to be discussed next is referred to as Single Miller capacitor Feed-Forward Compensation (SMFFC) [31]. The basic schematic of the SMFFC is shown in Figure 2.10 (l). This is the first of its kind to implement a completely compensated multi-stage amplifier using a single capacitor. The open-loop transfer function given by (13) from [31] is

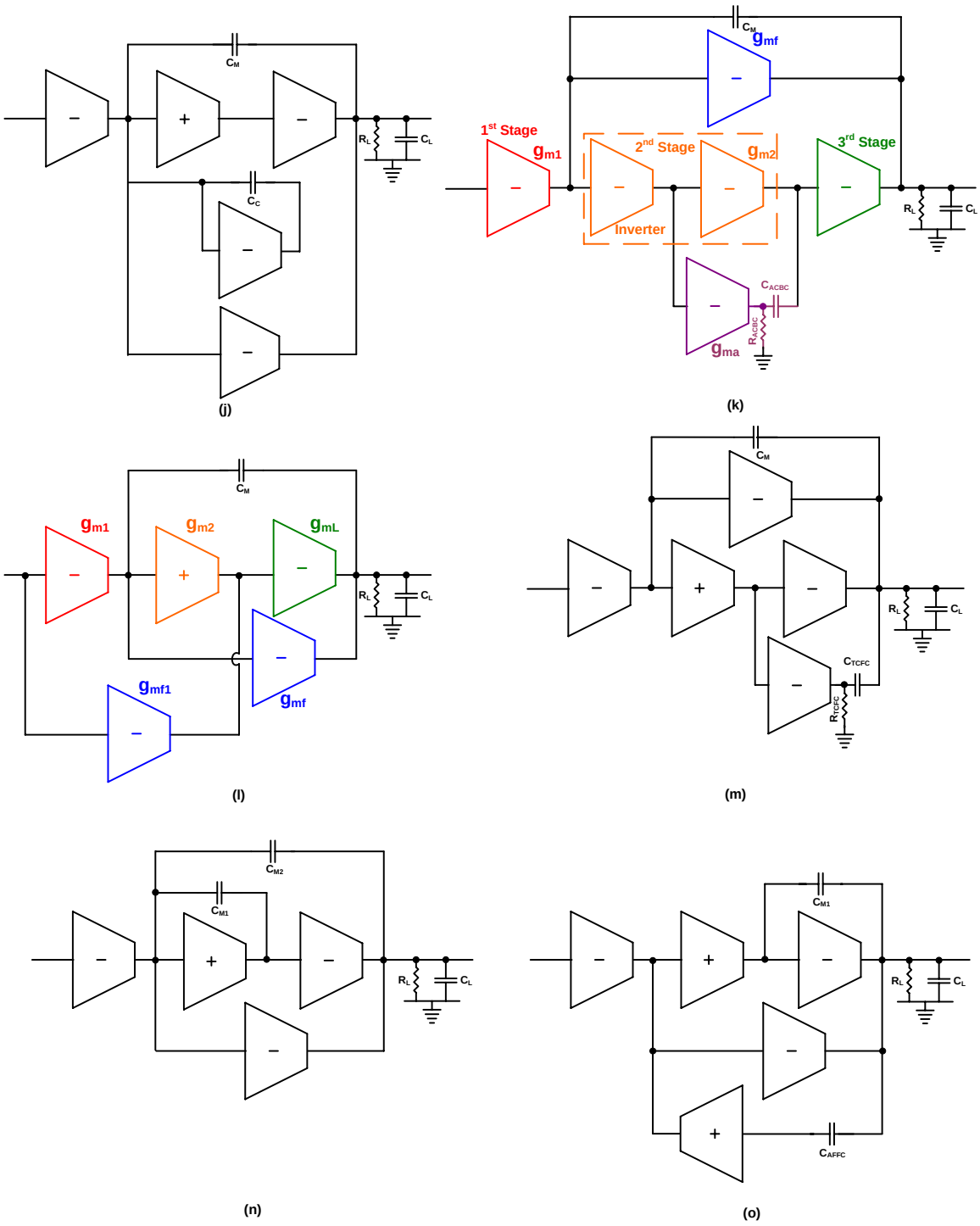

Figure 2.10. Schematics of the previously published compensation techniques for multi-stage amplifiers (j) DFCFC-II [33] (k) ACBC [29] (l) SMFFC [31] (m) TCFC [38] (n) PFFC [37] (o) AFFC [34]

$$A_{OL} = \frac{A_{DC}\left(1 + s\frac{C_m g_{mf1}}{g_{m1}g_{m2}} - s^2\frac{C_m C_{P2}}{g_{m2}g_{mL}}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \tag{15}$$

where $A_{DC} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{oL}}$, $g_{m(1,2,L)}$, $g_{o(1,2,L)}$ and $C_{p(1,2,L)}$ signify the transconductance, conductance and the parasitic capacitance at the output of each stage respectively.

The Routh-Hurwitz stability criterion [46], [29] is derived from the closed-loop transfer function of the SMFFC amplifier and is calculated to be

$$\frac{g_{o2}}{C_{p2}} > \left(\frac{g_{m1}}{C_m}\right)\left(\frac{1}{1 + \frac{g_{mf1}}{g_{m2}}}\right) \tag{16}$$

From the closed-loop transfer function, it is clear that there are two zeroes (one in left-half plane and the other in right-half plane). Since the LHP zero is present at much lower frequencies than the RHP zero, the RHP zero has very little impact on the phase response of the system. The compensation capacitor (also Miller capacitor) splits the first and third poles, while the feed-forward transconductance stage is used to improve the slew-rate. By appropriately distributing the gain across the stages and deriving the feed-forward transconductance (g_{mf1}) such that the dominant zero and the first non-dominant poles are cancelled, the need for the second Miller capacitor is eliminated. The estimated transconductance (g_{mf1}) can be mathematically calculated by

$$g_{mf1} = \left(\frac{1}{g_{m2} r_2}\right)\left(\frac{g_{m1} g_{m2} C_L}{g_{m3} C_m}\right) \tag{17}$$

The SMFFC topology is different from its predecessors in many ways. For example, a) a single Miller capacitor is used instead of the conventional two Miller capacitors, b) much smaller area utilization compared to other topologies, and c) much higher bandwidths compared to the previously published topologies. The drawbacks associated with SMFFC are: a) the overshoot in the large-signal step response, and b) large settling time. According to [32], "the time constant of the slow settling component is inversely proportional to the doublet frequency". From the measured results shown in that paper, it can be deduced that pole-zero doublets are present at relatively low frequencies.

Finally, a multi-stage amplifier with no Miller capacitors presented by Thandri [30] will be discussed. The schematic of the No-Capacitor Feed-Forward compensation (NCFF) topology is shown in Figure 2.11 (q). The presence of a Miller compensation capacitor in a multi-stage amplifier normally reduces the bandwidth, as the dominant pole is moved much lower in frequency by the factor of the gain (associated with the respective stage). Though using Miller compensation capacitors significantly reduces the complexity of the compensation topology, they in-turn increase the total area of the compensated amplifier (per the required capacitor area), reduce the bandwidth and have a significant impact on the performance of other parameters like slew-rate, power consumption, etc. The open-loop transfer function of NCFF based three stage amplifier is

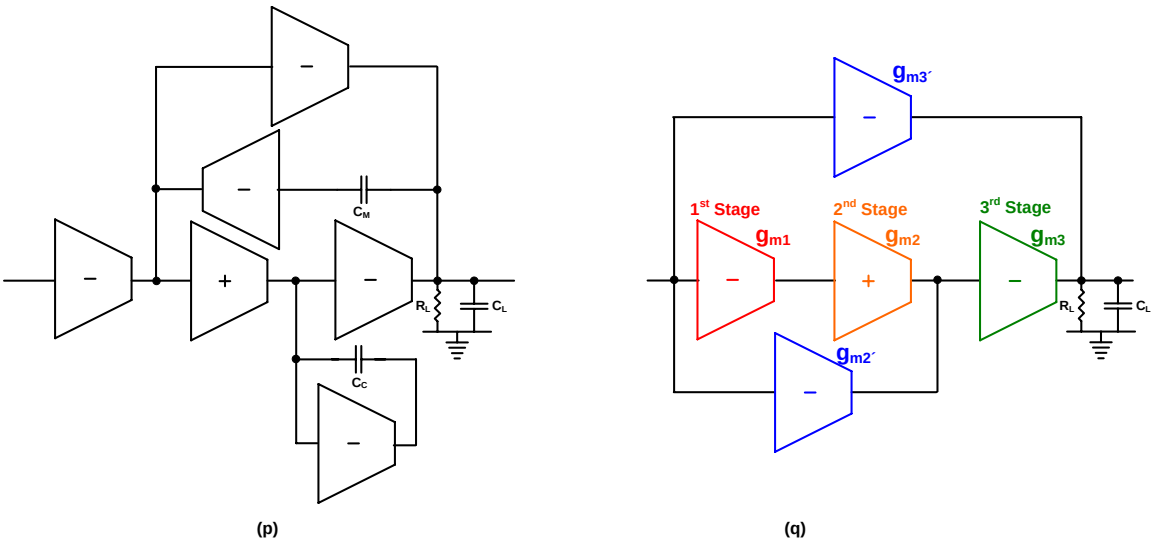

Figure 2.11. Schematics of the previously published compensation techniques for multi-stage amplifiers (p) DLPC [36] (q) NCFF [30]

$$A_{OL} = \frac{A_1 A_2 A_3 \times \left[1 + \frac{g_{m2}'\left(1+\frac{s}{\omega_{p1}}\right)}{g_{m1}R_1 g_{m2}} - \frac{g_{m3}'\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}{g_{m1}R_1 g_{m2}R_2 g_{m3}} \right]}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)} \tag{18}$$

where g_{m1-3}, R_{1-3}, and C_{1-3} indicate the transconductance, resistance and parasitic capacitance of stage$_{1-3}$, respectively, and ω_{p1}, ω_{p2} and ω_{p3} represent the first, second and third poles, respectively. Unlike other compensation topologies that use at least one Miller compensation capacitor, a significant improvement in bandwidth is achieved using the NCFF compensation topology since none of the poles (either dominant or non-dominant) are moved from their initial positions for compensation. The underlying strategy behind this topology is to place the non-dominant poles created from the feed-

forward, second and third stages at frequencies as much higher as possible compared to the desired UGBW. The feed-forward paths ($g_{m2'}$ and $g_{m3'}$) are used to create the LHP zeros at desired frequencies to improve the characteristics of the amplifier, particularly phase margin and pole-zero cancellation if desired. The drawbacks associated with this topology are a) lower phase margin, and b) that it may not be suitable for driving small loads.

The common problems associated with the multi-stage amplifiers and their compensation topologies are a) higher power consumption as to improve the slew-rate, b) bandwidth reduction caused by the usage of Miller capacitors, c) presence of closely located pole-zero pairs such that their impact is clearly seen from the step response, and d) settling time. The next chapter presents a unique "compound transconductance element" that can be used in developing a novel amplifier with much lower power consumption and better frequency performance characteristics.

3. Design of the Compound Transconductance based Operational Transconductance Amplifier

The first section of this chapter presents an overview of the design and unique performance characteristics of a compound transconductance element, which will be used in the development of a high gain amplifier. From hereon, unless otherwise mentioned, the terminology multi-stage amplifier and three-stage amplifier are used interchangeably. The second section deals with the mathematical analysis and the implementation of a novel compensation methodology necessary for the new multi-stage op amp to achieve closed-loop stability. The third section presents the simulation results of the complete op amp followed by conclusions.

3.1 Multi-stage op Amp with Compound Transconductance element

3.1.1 Circuit motivation

The conventional method to achieve high gain in a CMOS op amp is to increase the output impedance. Various circuit topologies like cascoding [44], regulated cascode [7], and composite transistor [55] based amplifiers have been developed to achieve high DC gain in single-stage amplifiers. The above topologies have been combined with multi-stage architectures to achieve much higher DC gain than those achieved through a single-stage amplifier. The DC gain equation in a single-stage amplifier can be simply written as

$$Gain_{DC} = g_m \times r_0 \tag{19}$$

where g_m is the transconductance and r_0 is the output impedance. It can be understood that the gain can be increased either by increasing the output impedance or the transconductance, though typically increasing g_m by increasing bias current can subsequently decrease r_0 depending on the circuit configuration[1]. There has been a considerable amount of effort in developing various topologies to achieve high DC gain by increasing the output impedance. But on the other hand, transconductance can be increased by increasing the bias current, though this generally affects other parameters like output impedance and power consumption. The next section describes a novel compound transconductance element that provides an efficient way to achieve higher transconductance for a given power consumption while promoting gain.

3.1.2 Circuit description

The goal of this work is develop a compound element that can help promote gain in an efficient manner, and can be used as a building block in implementing a high gain amplifier. The two basic components that make up the DC gain of an amplifier are g_m and r_0. The drawbacks associated with the methodologies in improving r_0 are discussed in the previous chapter. Instead of generating the total gain of the amplifier from a single-stage, it can be generated using multiple simple gain units. When these smaller gain units are cascaded back-to-back, the individual smaller gains are compounded, resulting in the generation of much larger net gain than the gain of the single-stage amplifier. Figure 3.1 shows the conceptual schematic of the conventional single-stage amplifier and the compound element based amplifier:

[1] In general, low-power CMOS amplifiers readily achieve high DC gain, thanks to high r_0, but suffer poor bandwidth due to low g_m.

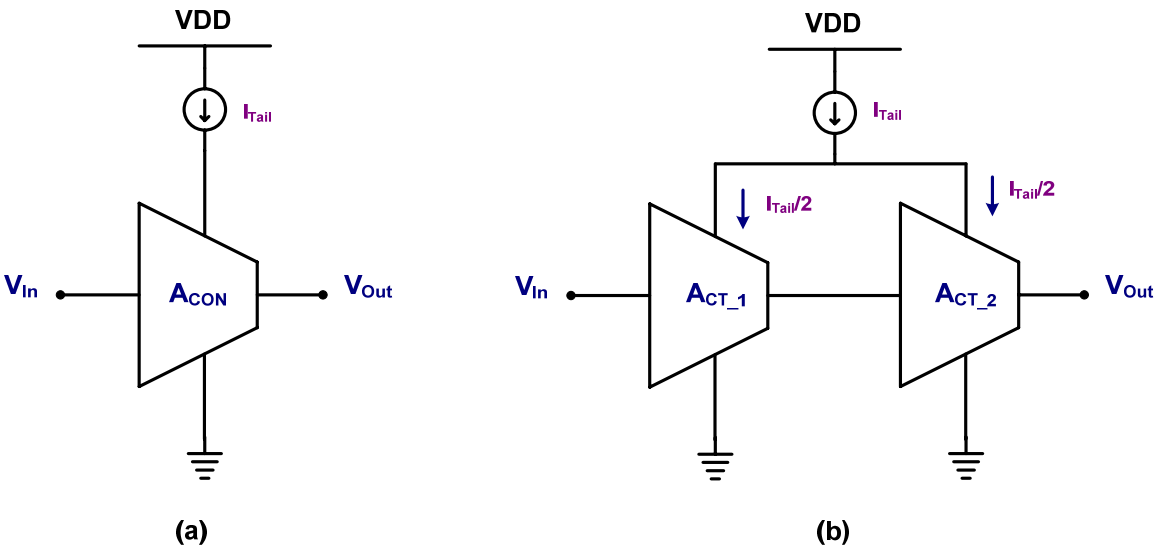

Figure 3.1. Conceptual schematic of (a) conventional single-stage amplifier and (b) compound element based amplifier

Assume the tail current (I_{Tail}), output impedance and current density (current/area) in both the amplifiers is same. Assuming the input differential pair and the tail current devices operate in strong inversion saturation, the gain of the conventional single-stage amplifier is given by

$$Gain_{\text{single-stage}} = A_{CON} = g_m \times r_0 \cong \frac{1}{\lambda}\sqrt{\frac{\beta}{I_{Tail}}} \tag{20}$$

where g_m and r_0 represent the transconductance of the input differential pair and the output impedance respectively, while $\beta = \mu C_{OX}\frac{W}{L}$. In the case of compound element based amplifier, the gain is given by

$$Gain_{\text{compound\_element}} = \left(\mathrm{A}_{\mathrm{CT\_1}}\right)\left(A_{CT\_2}\right) = \left(g_{m1}r_{01}\right)\left(g_{m2}r_{02}\right) \cong \left(\frac{1}{\lambda}\sqrt{\frac{\beta_1}{I_{Tail}/2}}\right)\left(\frac{1}{\lambda}\sqrt{\frac{\beta_2}{I_{Tail}/2}}\right), \tag{21}$$

$$\Rightarrow \left(\frac{1}{\lambda}\sqrt{\frac{\beta/2}{I_{Tail}/2}}\right)\left(\frac{1}{\lambda}\sqrt{\frac{\beta/2}{I_{Tail}/2}}\right).$$

where the device dimensions of the differential pairs in A_{CT_1} and A_{CT_2} are half the size of differential pairs in conventional amplifier, then the gain of the compound element based amplifier is given by

$$\Rightarrow Gain_{\text{compound\_element}} \cong \left(\frac{1}{\lambda}\sqrt{\frac{\beta}{I_{Tail}}}\right)^2 \tag{22}$$

Quantitatively, the gain of the compound element is square of the gain offered by the conventional single-stage amplifier for the same power consumption. This is the principle of operation of the compound element, which is hereby referred to as "Compound Transconductance Element" or simply CT element.

Figure 3.2 shows the schematics of conventional single-stage differential (SD) amplifier and the novel compound transconductance (CT) element. Assuming that the input differential pair operates in strong inversion saturation (SI sat), then for a given tail current (I_{Tail}) the DC small-signal gain for the SD amplifier can be given by

$$\mathrm{Gain}_{DC}(\mathrm{SD}) = g_m{}'r_0{}' = \left(\sqrt{\beta \mathrm{I}_{\mathrm{Tail}}}\right)\left(\frac{1}{\lambda I_{Tail}}\right) \cong \frac{1}{\lambda}\sqrt{\frac{\beta}{I_{Tail}}} \tag{23}$$

assuming ideal bias current sources.

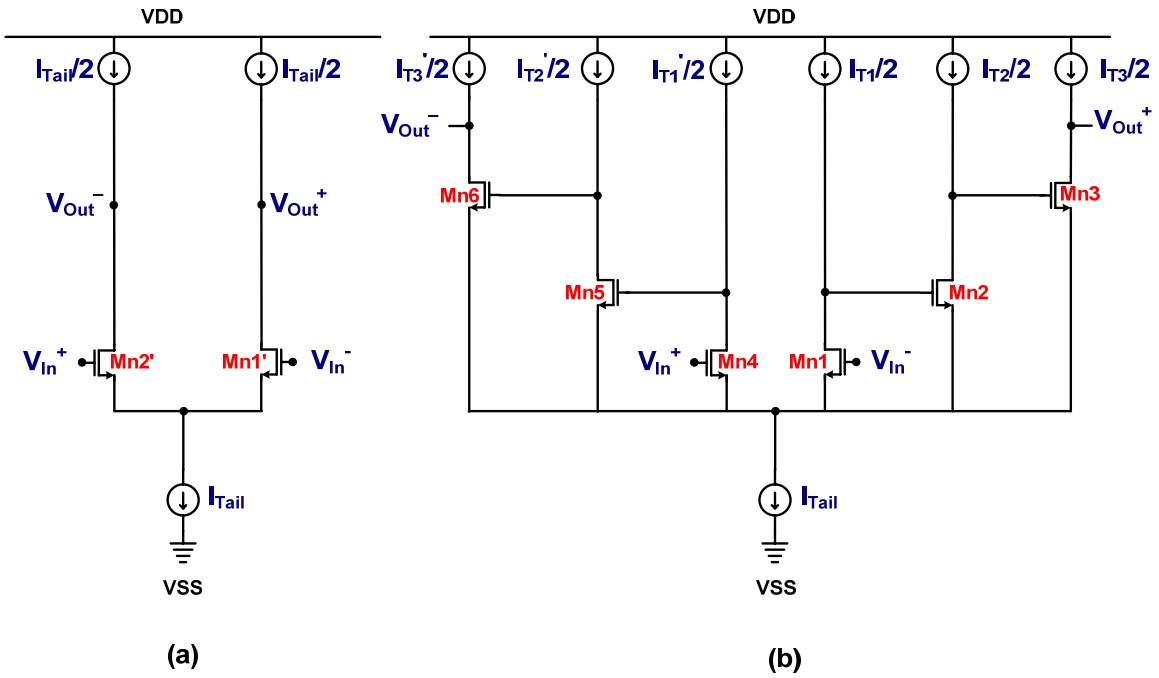

Figure 3.2. (a) Single-stage amplifier and (b) Compound Transconductance amplifier, each with active loads

Alternately, if the same tail current ('I_{Tail}') is split across the input differential pairs as shown in Figure 3.2, and assuming Mn1–Mn6 are perfectly matched and equally sized, then I_{Tail} splits evenly between the three differential pairs Mn1/Mn4, Mn2/Mn5 and Mn3/Mn6. Then the gain of compound transconductance amplifier (CT-amplifier) is given by

$$\text{Gain}_{DC}(CT\text{-}amplifier) = (g_{m1}r_{01})(g_{m2}r_{02})(g_{m3}r_{03}) \tag{24}$$

$$\text{where } g_{m1} = g_{m2} = g_{m3} = \sqrt{2\beta_1 \frac{I_{T1}}{2}} = \sqrt{2\frac{\beta}{3}\frac{I_{Tail}}{6}} = \sqrt{\frac{\beta}{3}\frac{I_{Tail}}{3}} \text{ and}$$

$$r_{01} = r_{02} = r_{03} = \frac{1}{\lambda I_{T1}} = \frac{1}{\lambda I_{T2}} = \frac{1}{\lambda I_{T3}} = \frac{3}{\lambda I_{Tail}},$$

$$\Rightarrow Gain_{DC}(CT\text{-}amplifier) = \left(\sqrt{\frac{\beta}{3}\frac{I_{Tail}}{3}} \times \frac{3}{\lambda I_{Tail}}\right)^3 \cong \left(\frac{1}{\lambda}\sqrt{\frac{\beta}{I_{Tail}}}\right)^3.$$

Hence for a given tail current (therefore equal power consumption), the ratio of the gains offered by CT-amplifier to that of a conventional differential amplifier is given by

$$\frac{Gain_{DC}(CT\text{-}amplifier)}{Gain_{DC}(\mathrm{SD})} = \frac{\left(\frac{1}{\lambda}\sqrt{\frac{\beta}{I_{Tail}}}\right)^3}{\frac{1}{\lambda}\sqrt{\frac{\beta}{I_{Tail}}}} = \left(\frac{1}{\lambda}\sqrt{\frac{\beta}{I_{Tail}}}\right)^2 \tag{25}$$

$$Ratio\ of\ gains(in\ \mathrm{dB}) = 20\log_{10}\left[\left(\frac{1}{\lambda}\sqrt{\frac{\beta}{I_{Tail}}}\right)^2\right] = 2\left[Gain_{DC}(SD)\ in\ dB\right] \tag{26}$$

From (26), it can be concluded that the gain of the compound transconductance element in dB is double that of the gain from a single differential pair amplifier. The above equation shows that gain offered by the CT-amplifier is much higher than the gain offered by the conventional differential pair for a given power consumption. This can be attributed to the efficient transconductance action offered by the CT element for a given power consumption. This forms the basic building block in the design of a very high gain amplifier, which will be discussed in the later sections.

3.1.3 Performance characteristics

The previous section demonstrated that the gain offered by the CT-amplifier is much higher than that of a conventional differential amplifier. The following performance characteristics will be discussed in detail:

1. Offset,
2. Open-Loop Gain, Phase Margin and Frequency Compensation,
3. Input Common Mode Range (ICMR),
4. Common-Mode Voltage Level (at multiple nodes), and

5. Power Supply Rejection Ratio (PSRR)

3.1.3.1 Offset

The offset of an amplifier is comprised of two basic components that are a) systematic and b) random offset. Of these, systematic offset is predominantly caused by the mismatch in the impedances encountered in the signal path from the input to the output nodes. For example, the impedances offered at various nodes in the signal path for a single-stage, single-ended output amplifier from the inverting and non-inverting input terminals will be different. Random offset is caused by mismatch in the threshold voltage, and transconductance parameter (β) of various devices in the design. Systematic offset can be reduced to a great extent through symmetric implementation of the amplifier. Random mismatch between various devices can be minimized by careful design and layout techniques [24], [58], [59], [60]. The offset of a fully differential amplifier is inherently lower than that of a single-ended output amplifier because of its structurally symmetric implementation.

Figure 3.3 shows a conventional single-stage, single-ended amplifier and a single-ended CT-amplifier. This CT-amplifier forms the building block in the implementation of the multi-stage amplifier developed in this work. The drain of the Mn2' is connected to a diode connected MOSFET while the drain of Mn1' is not, which creates a mismatch in the impedances at drain nodes. This is the major source of systematic offset in a single-stage, single-ended output differential input amplifier. In the case of CT-amplifier, the impedances offered at various nodes through the signal path for both the inverting and

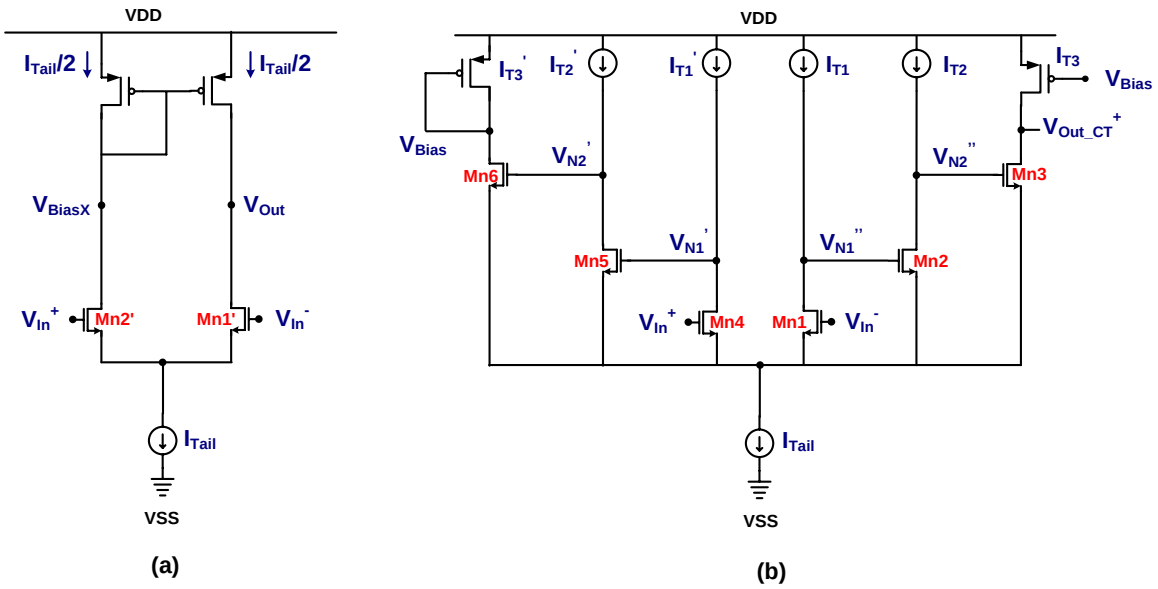

Figure 3.3. (a) Conventional single-stage, single-ended amplifier and (b) Compound Transconductance element with single-ended output

non-inverting input terminals are comparable all the way from the input terminals ('V_{In}^{+}' and 'V_{In}^{-}') to the output terminals ('$V_{Out\_CT}^{+}$' and 'V_{Bias}'). The terminals '$V_{Out\_CT}^{+}$' and 'V_{Bias}' shown in the schematic are output terminals of the CT element, but not the outputs of the CT-based op amp. A differential-to-single ended conversion to implement a single ended CT-based amplifier will be implemented in the later part of the signal path. Because of this, CT architecture based amplifiers offer much lower systematic offset than conventional amplifiers without any additional design effort. This offset can be further minimized if the CT-amplifier is used in a fully differential configuration.

3.1.3.2 Open-loop gain, Phase margin and Frequency compensation

The open-loop gain of the CT-based amplifier is much higher compared to that of a conventional amplifier, which was shown in (26). One of the reasons for this is the

presence of high impedance intermediate nodes. For more detailed analysis, a simplistic CT element based schematic is considered in Figure 3.4.

It is highlighted in Figure 3.4 that Mn1 and Mn4, Mn2 and Mn5, and Mn3 and Mn6 form the three individual stages and can be treated as first, second and third stages respectively, of a multi-stage amplifier. All these individual stages are comprised of common-source differential pair amplifiers. These individual stages transform this simple element into a complex high gain multi-stage amplifier. The various implications from this transformation are: a) the frequency compensation of the CT-based amplifier is non-trivial, and b) it is easier to analyze the CT element's behavior and characteristics when viewed as a cascaded multi-stage amplifier.

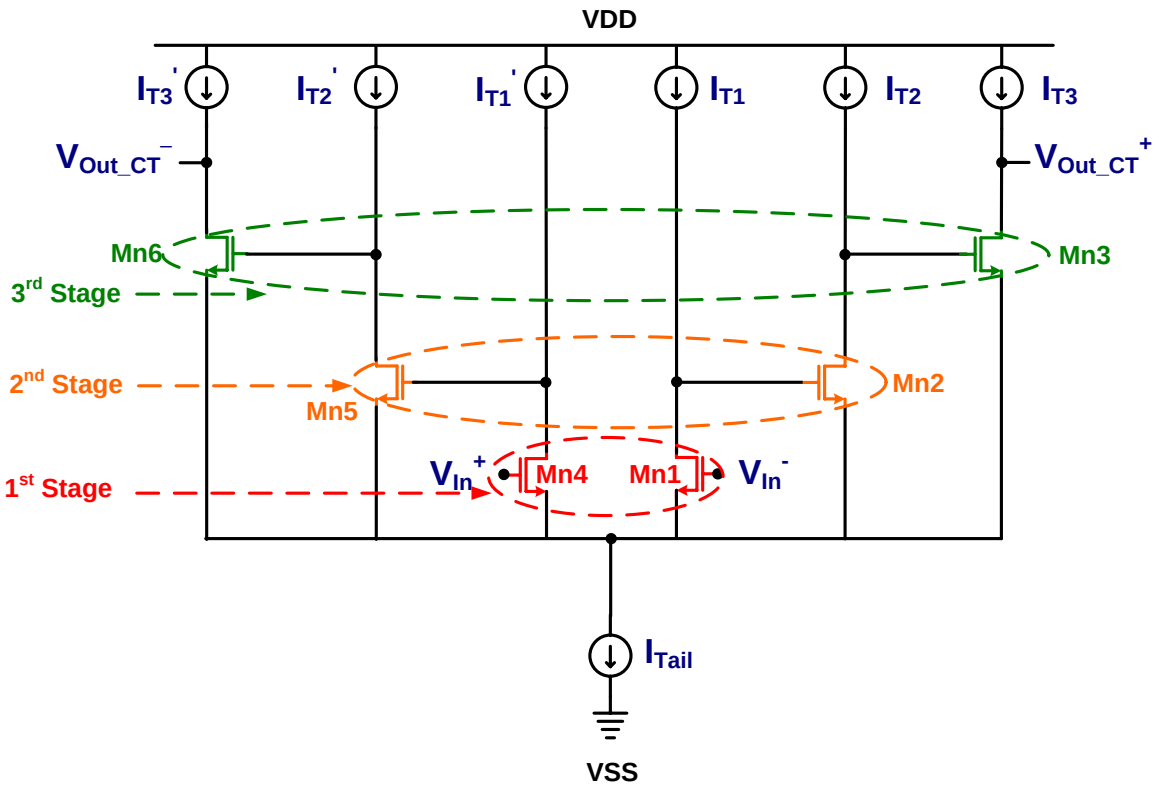

Figure 3.4. CT element as a multi-stage amplifier

Topologically, there is a significant difference between the multiple stages in a CT-amplifier to those of a conventional multi-stage amplifier. All the stages shown in the CT-amplifier have signal inversions. The topologies of previously published multi-stage amplifiers were shown and discussed in the previous chapter. In those architectures, the cascaded stages which contribute to the forward signal path have alternating inverting and non-inverting signal gains. Figure 3.5 clarifies this idea and compares the amplifier topologies.

Since the previously implemented multi-stage amplifiers (3 or more stages) use alternating non-inverting gain stages, it is relatively easier to achieve negative feedback loops across various stages during frequency compensation. This implies that none of the previously published compensation topologies can be applied to CT-based amplifier for

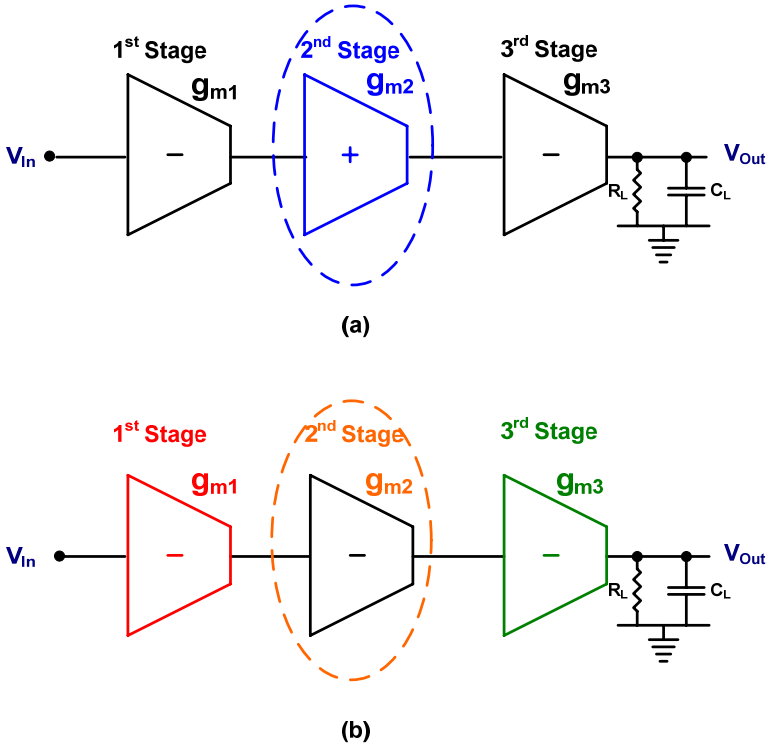

Figure 3.5. Comparison between the (a) conventional multi-stage amplifier and (b) CT-amplifier

achieving stability. Hence this CT element based amplifier demands a novel compensation topology to achieve frequency stability. The CT element's efficient production of high gain justifies this effort. The frequency compensation and small-signal analysis of the CT-amplifier will be discussed later.

3.1.3.3 Input Common Mode Range (ICMR)

Input common mode range is one of the basic performance characteristics of an amplifier that defines the conditions of inter-operability with other systems. It is commonly defined as the input voltage range for which both the input differential pair and the tail current source operate in SI saturation. Assuming a cascode tail current source and cascode load (shown in Figure 3.2), the ICMR for an n-type CT-amplifier can be calculated as

$$\begin{aligned} V_{I,MIN} = ICMR_{MIN} &= VSS + \left(2 \times V_{DS,SAT}\right) + V_{GS}\ , \\ &= VSS + \left(2 \times V_{DS,SAT}\right) + \left(V_{DS,SAT} + V_{TN}\right), \\ &= VSS + \left(3 \times V_{DS,SAT}\right) + V_{TN}\ . \\ V_{I,MAX} = ICMR_{MAX} &= VDD - \left(2 \times V_{DS,SAT}\right) - V_{GS} + V_{GS}\ , \\ &\Rightarrow VDD - \left(2 \times V_{DS,SAT}\right). \end{aligned} \tag{27}$$

where $V_{I,MIN}$, $V_{I,MAX}$, V_{TN} and $V_{DS,SAT}$ refer to the minimum and maximum allowable common-mode input voltage level, threshold voltage of the n-channel MOSFET and saturation voltage of nominal MOSFET respectively. The CT-amplifier offers comparable ICMR to a conventional n-type input differential pair OTA with an active cascode load and a cascode tail current source. But the $V_{I,MAX}$ is '$2 \times V_{DS,SAT}$' or approximately 500 mV lower than that of an input n-type folded-cascode amplifier. This

can be improved to within a '$V_{DS,SAT}$' (about 250 mV), if a single transistor load is used instead of cascode load.

3.1.3.4 Common-mode voltage level (between stages)

A common-mode voltage level stabilizer is necessary whenever the common-mode amplitude level is not easily determined by a simple "visual inspection" [56]. The nodes V_{N1}', V_{N1}'', V_{N2}', and V_{N2}'' (see Figure 3.3) are the intermediate nodes in the signal path from input to output of the CT element. Since the common-mode voltage level of these pairs is comparable to that of the input nodes (V_{In}^+ and V_{In}^-), dedicated common-mode voltage stabilizer circuitry is not necessary for the CT element based amplifier. This relieves a significant burden in the design as common-mode level stabilizers are one of the more difficult design challenges in amplifiers. These are analogous to common-mode feedback circuits, which are used to set the output common-mode level in the case of fully differential amplifiers. In the CT-amplifier, the common-mode levels of the intermediate nodes are inherently determined by the common-mode level of the differential input signals through device matching.

3.1.3.5 Power Supply Rejection Ratio (PSRR)

This is the ability of the system to reject the noise and harmonics from the power supply rails. In the case of op amps, the A_{OLDC} contributes directly in calculating *PSRR*. The mathematical relation between A_{OLDC} and *PSRR* is given by

$$PSRR^{+} = \frac{A_{OLDC}}{\left(v_{out} / v^{+} \right)} \tag{28}$$

where v_{out}/v^{+} defines the small-signal gain from the positive power rail to the output and A_{OLDC} is the open-loop gain at DC. Without any design changes specific to improving the PSRR, a sufficient PSRR for most applications can be expected from the CT-based op amp.

The schematic of a p-type input differential pair based CT-amplifier without the compensation is shown in Figure 3.6. The schematic shows various current directions but not their values, because the actual currents are dependant on the frequency compensation design. The complete schematic with the actual currents will be shown later, after discussing the frequency compensation. Instead of using the entire tail current to go through a single differential pair, it is split across multiple differential pairs, each of which operates as an individual gain stage. In a conventional folded-cascode op amp, the outputs of the differential pair fold into their complementary MOSFETs for improving the ICMR. Similarly, the outputs of the CT element, which are output terminals (n6 and n9) of the third stage p-channel transistors (Xp11 and Xp12) are folded into n-channel transistors. The compound transconductance element replaces a single differential pair and merges multiple gain stages of a conventional multi-stage amplifier into a single, compact and power efficient transconductance element, achieving the performance of a multi-stage amplifier, with the power consumption comparable to that of a single-stage folded-cascode amplifier. Though the CT element based amplifier offers enormous small-

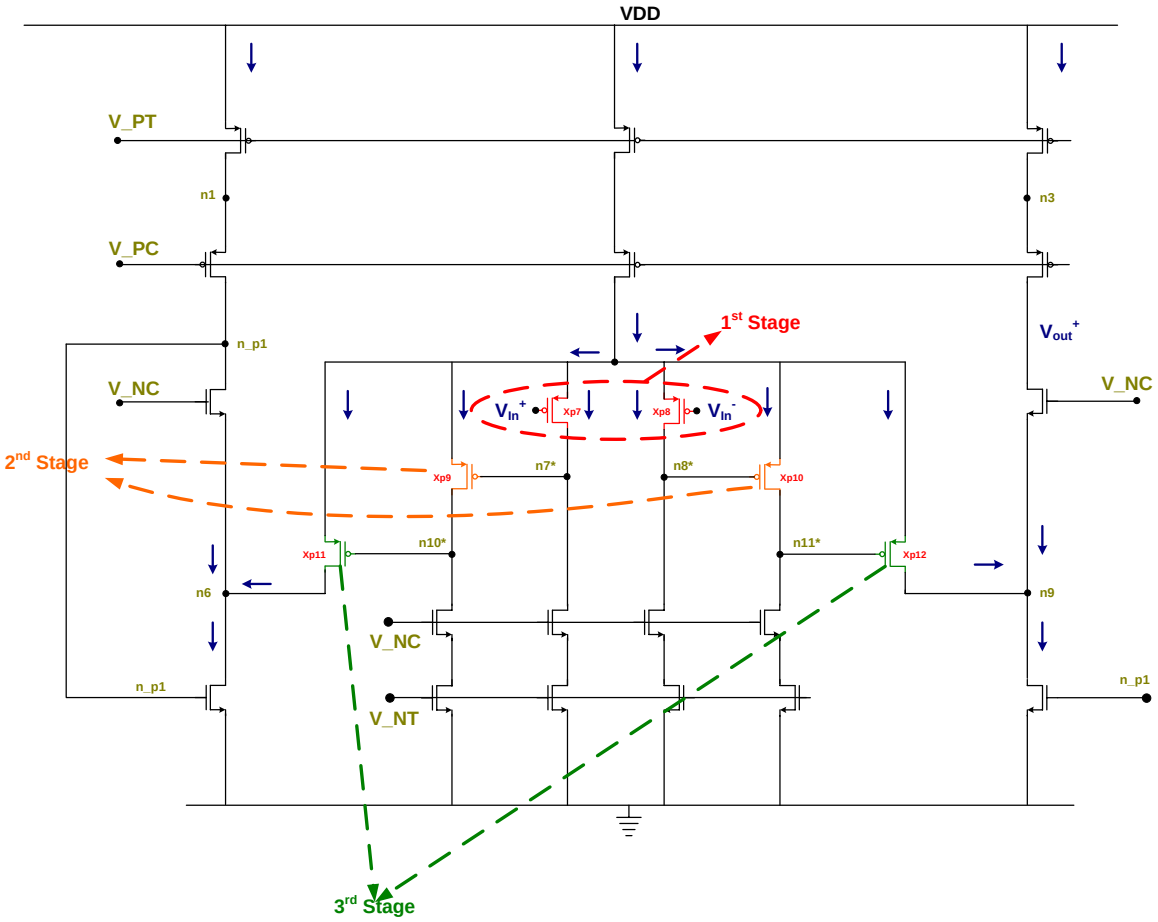

Figure 3.6. P-type input differential pair based CT-amplifier (without frequency compensation)

signal gain, there is a penalty associated with this implementation in terms of bandwidth. In the CT-amplifier, there are three poles located at the same frequency compared to a single pole in the case of a conventional single-stage amplifier. This penalty will be discussed in greater detail in Section 4.3. During this work, the CT element and CT-amplifier are implemented using p-type input differential pairs.

3.1.4 Bias generation block

This section briefly presents the bias generation circuit. Biasing has a major impact on the performance of amplifiers, as it effects the power consumption, voltage swing, node impedance and noise, etc. The Minch biasing technique [52], [54] is one such technique that can be used to help optimize numerous performance characteristics, over a wide range of bias current levels. In the present design, the Minch biasing technique is not only used to generate bias voltages but also for mirroring currents necessary during the operation of the amplifier. Figure 3.7 shows the schematic of an n-type Minch biasing circuit that is used for generating gate bias voltages for the NMOS current sink transistors. From hereon, the bias voltages for NMOS current sink transistors are referred to as 'V_NC' and 'V_NT' respectively. Similarly, its complementary p-type Minch biasing circuit is used to generate the gate bias voltages for the PMOS current source transistors and are referred to as 'V_PC' and 'V_PT', respectively. The complete compound transconductance amplifier needs an external input bias current source 'I_{IN}' for operation.

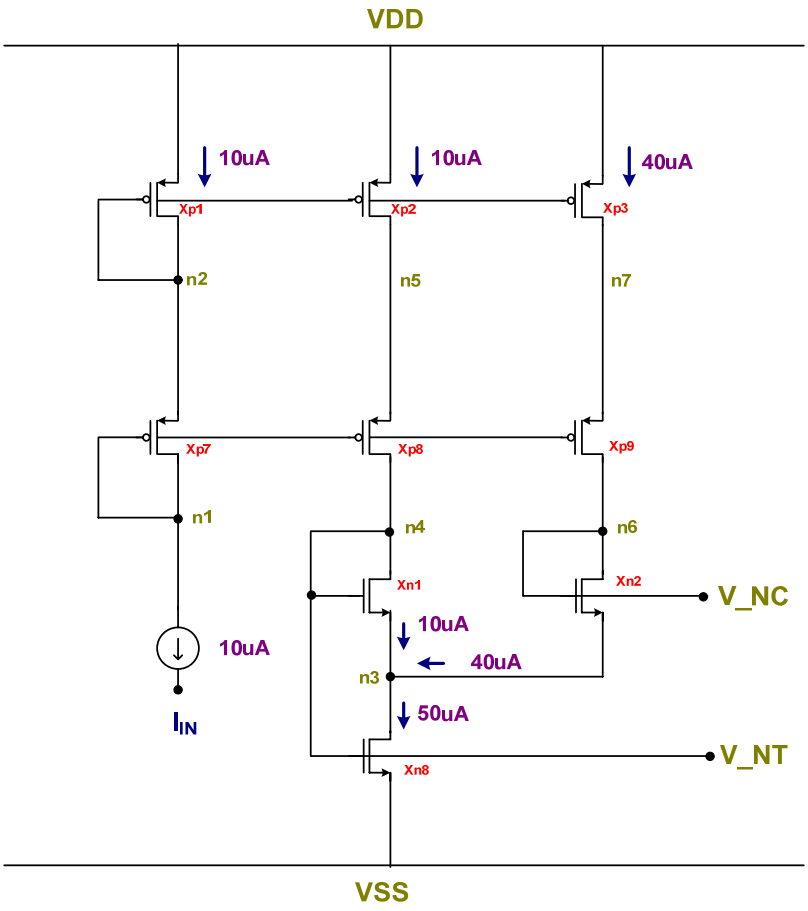

Figure 3.7. N-type Minch bias generation circuit

3.1.5 Design scalability with technology evolution

Many of the present day publications in the *IEEE Journal on Solid-State Circuits* start with either process scaling information or predictions from *International Technology Roadmap for Semiconductors* (ITRS) [53]. Both predict that electronic systems need to be designed and implemented for supply voltages less than or equal to 1 V. Currently, the CT-amplifier is implemented in a 5-V bulk CMOS process for prototyping purposes, but the circuit topology can be applied to lower voltage processes. Assuming single transistor current sources for both the I_{Tail} and $I_{T1/2/3/1'/2'/3'}$, the CT design could be readily scaled and implemented in a 1.8-V bulk CMOS process. Scaling this design for implementation in very deep sub-micron (< 1.8-V) process requires an alternative strategy. A methodology to implement this CT-based amplifier topology in a very deep sub-micron process (e.g., a 1-V process) will be briefly discussed in the future work.

3.2 Compensation technique for the Compound Transconductance amplifier

The earlier sections in this chapter discussed the unique advantages of the CT-based amplifier topology and its performance characteristics. Because all its stages have inverting signal gains, none of the previously published compensation architectures could be applied. The various challenges that need to be addressed by the compensation topology are as follows: a) pole-zero cancellation, b) feasibility in implementing the topology, c) efficient implementation (some topologies are power inefficient, some are area inefficient), d) must have some negative feedback loops for achieving stability, e) ensure a sufficient phase margin for achieving good settling time, f) ensure a good

bandwidth for a fast rise and fall time, and g) achieve a good slew-rate. This section presents the concept of the compensation topology, the mathematical analysis involved with its transfer function and a brief discussion on the stability criteria.

Figure 3.8 shows the block level schematic of the single-ended, half circuit of the frequency compensated CT-amplifier. The transconductance, conductance and parasitic capacitance at the output of the 1st, 2nd and 3rd stages are given by $g_{m(1,2,3)}$, $g_{o(1,2,3)}$ and $C_{(1,2,3)}$ respectively.

Z_{O1}, Z_{O2} and Z_{I5} represent the lumped impedances at the outputs of 1st and 2nd stages and at the input of the g_{m5} stage respectively. The output impedance (R_3 and C_3) comprises of 3rd stage output resistance, parasitic capacitance and the load capacitance (C_L).

The small-signal model of the CT-based amplifier with compensation blocks is shown in Figure 3.9. The following assumptions are made for simplification of the complicated transfer function: $Z_{I5} = g_{I5} + sC_{I5}$, $C_2 << C_6$, $C_5 << C_6$, $g_{m5} = g_{I5}$, $g_{I5} >> g_{o2}$, and without neglecting any zeroes or poles. The detailed derivation of the complete transfer function of this CT-amplifier is shown in Appendix A.

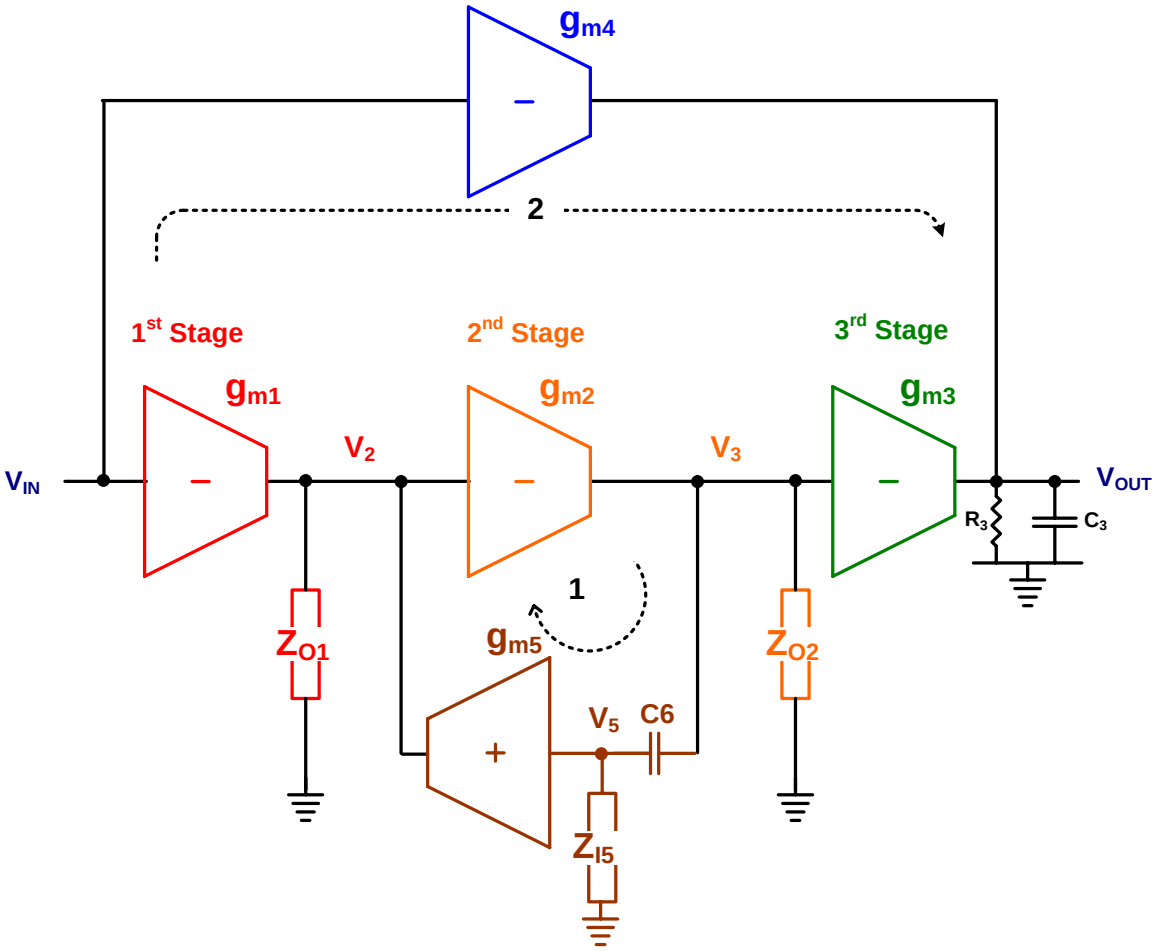

Figure 3.8. Block level schematic of the complete frequency compensated single-ended, half-circuit of the CT-amplifier

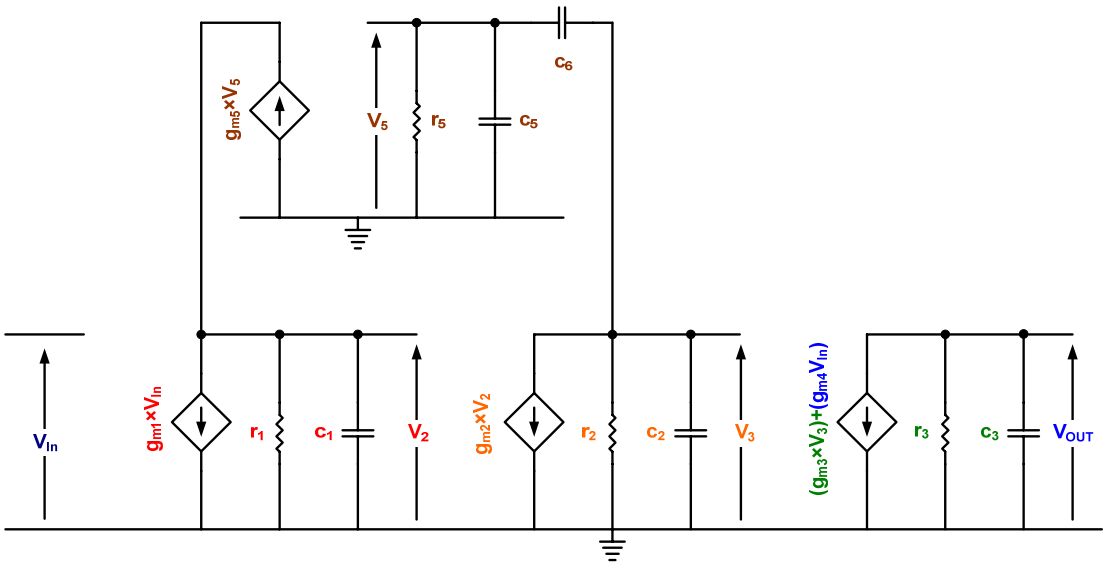

Figure 3.9. Small-signal schematic of the CT-amplifier

The complete transfer function of the CT-amplifier is simplified into

$$\frac{V_{OUT}}{V_{IN}} \approx -A_1A_2A_3 \times \frac{C_{N0}+sC_{N1}+s^2C_{N2}+s^3C_{N3}}{(1+sr_3C_3)(1+sC_{D1}+s^2C_{D2}+s^3C_{D3})} \tag{29}$$

where

$$C_{N0} = 1+\frac{g_{m4}}{g_{m1}g_{m2}g_{m3}r_1r_2},$$

$$C_{N1} = \frac{C_6}{g_{m5}}+\left\{\left(\frac{g_{m4}}{g_{m1}g_{m2}g_{m3}r_1r_2}\right)\left(r_1C_1+r_2C_6+\frac{C_6}{g_{m5}}+g_{m2}r_1r_2C_6\right)\right\},$$

$$C_{N2} = \left(\frac{g_{m4}}{g_{m1}g_{m2}g_{m3}r_1r_2}\right)\left(r_1C_1r_2C_6+\frac{r_1C_1C_6}{g_{m5}}+\frac{r_2C_2C_6}{g_{m5}}+\frac{r_2C_5C_6}{g_{m5}}\right),$$

$$C_{N3} = \left(\frac{g_{m4}}{g_{m1}g_{m2}g_{m3}r_1r_2}\right)\left(\frac{r_1C_1r_2C_2C_6}{g_{m5}}\right),$$

$$C_{D1} = r_1C_1+r_2C_6+\frac{C_6}{g_{m5}}+g_{m2}r_1r_2C_6,$$

$$C_{D2} = r_1 C_1 r_2 C_6 + \frac{r_1 C_1 C_6}{g_{m5}} + \frac{r_2 C_2 C_6}{g_{m5}} + \frac{r_2 C_5 C_6}{g_{m5}}, \text{ and}$$

$$C_{D3} = \frac{r_1 C_1 r_2 C_2 C_6}{g_{m5}}.$$

Z_{I5} and g_{I5} represent the lumped input impedance and input conductance of the g_{m5} stage, respectively. In the above list of equations, C_{N0}, C_{N1}, C_{N2}, and C_{N3} represent the coefficients of the s^0, s^1, s^2, s^3 terms of the numerator, while C_{D1}, C_{D2} and C_{D3} represent the coefficients of s^1, s^2, s^3 terms of the denominator, respectively. With the additional assumptions, $C_1 << C_6$, $g_{m4} << g_{m1}g_{m2}g_{m3}r_1r_2$, $(1+g_{m5}) << r_1r_2g_{m2}g_{m5}$, $C_1g_{m5} >> g_{m2}C_2$ and $g_{m4}g_{m5} >> g_{m1}g_{m3}$, the above transfer function can be further simplified to

$$\frac{V_{OUT}}{V_{IN}} \approx -A_1A_2A_3 \times \frac{\left(1+s\frac{C_1}{g_{m2}}\right)\left(1+s\frac{C_2}{g_{m5}}\right)\left(1+s\frac{C_6 g_{m4}}{g_{m1}g_{m3}}\right)}{\left(1+s\frac{C_1}{g_{m2}}\right)\left(1+s\frac{C_2}{g_{m5}}\right)(1+sr_3C_3)(1+sg_{m2}r_1r_2C_6)} \tag{30}$$

From the above equation, it is guaranteed that all the poles and zeroes offered by the above system lie in the left-half plane. This is an important result, as the designer need not worry about RHP zeroes when considering feedback stability. If a LHP zero is present in the transfer function, but is located far above the unity-gain frequency (UGF), then it can be simply neglected. Instead, if it is a RHP zero, then it has to be either cancelled or moved into the LHP for achieving stability since the RHP zero degrades the closed-loop stability of the system. Thus, this system with the above assumptions, eliminates the extra effort needed to either move or cancel RHP zeroes. There are multiple solutions for the original transfer function shown in (29), among which some are

power efficient while some are not. The result in (30) gives considerable flexibility while deciding on pole-zero cancellation due to the absence of RHP zeroes.

From the above equation, the first two terms get cancelled, resulting in a single zero, two-pole system. This zero could be cancelled with either of the poles, but the pole present at the output ($1+sr_3C_3$) is chosen to minimize the power consumption. The transfer function then becomes

$$\frac{V_{OUT}}{V_{IN}} \approx -A_1 A_2 A_3 \times \frac{\left(1 + s\frac{C_6 g_{m4}}{g_{m1} g_{m3}}\right)}{(1 + sr_3 C_3)(1 + sg_{m2} r_1 r_2 C_6)} \tag{31}$$

Values for g_{m4} and C_6 are calculated from the pole-zero cancellation condition given by

$$\frac{g_{m4} C_6}{g_{m1} g_{m3}} = r_3 C_3 \Rightarrow g_{m4} C_6 = g_{m1} g_{m3} r_3 C_3 \tag{32}$$

The individual values for g_{m4} and C_6 are a compromise between power consumption and area efficiency. The CT-amplifier design is prototyped in a 0.5-µm bulk CMOS process, which offers an area efficient poly-poly2 capacitor. A capacitance of 15 pF is assumed for C_6 and value for g_{m4} is calculated from the relation shown in (9). The value for g_{m5} is calculated from another assumption, $g_{m4}g_{m5} >> g_{m1}g_{m3}$, which is used in the derivation of (30). When the zero shown in (31) is cancelled with the desired pole, ideally the op amp behaves as a single-pole system with a phase margin equal to 90º, which is predicted by

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{-A_1 A_2 A_3}{(1 + sg_{m2} r_1 r_2 C_6)}. \tag{33}$$

The compensation topology has a single negative feedback loop (shown by '1' in Figure 3.8) and a single feed-forward path (shown by '2' in Figure 3.8). Typically, a capacitor is used to provide the negative feedback path, which also generates an undesirable RHP zero because of the associated small-signal feed-forward path. But in this case, the RHP zero is absent since the capacitor is isolated from the node 'V_2' through the transconductance element g_{m5}, even at high frequencies (see Figure 3.8). An alternate method commonly referred as "grounded-gate cascode compensation" was discussed by Ahuja [4]. The feed-forward path serves two purposes: a) useful for the pole-zero cancellation shown in (31), and b) improves the slew-rate of the amplifier.

In op amps, phase margin is a compromise between settling time and error tolerance. For example, if the PM is small, then the small-signal transient step response has a large overshoot but with fast rise/fall times and vice-versa. According to Yang [42], the optimal phase margin for a 1% error tolerance band with respect to overshoot and minimum settling time is approximately 70º. Ideally, the above compensation topology can achieve 90º phase margin. But any mismatch in the pole-zero cancellation will result in a phase margin that is less than 90º. The two advantages resulting from this mismatch in the pole-zero cancellation are: a) reduction in the phase margin close to about 70º, and b) reduction in the power consumption by reducing g_{m4}. The complete derivation of the transfer function is shown in Appendix A.1.

The Figure 3.10 shows the transistor-level schematic of the g_{m4} and g_{m5} blocks, whose block-level schematics are shown in Figure 3.8.

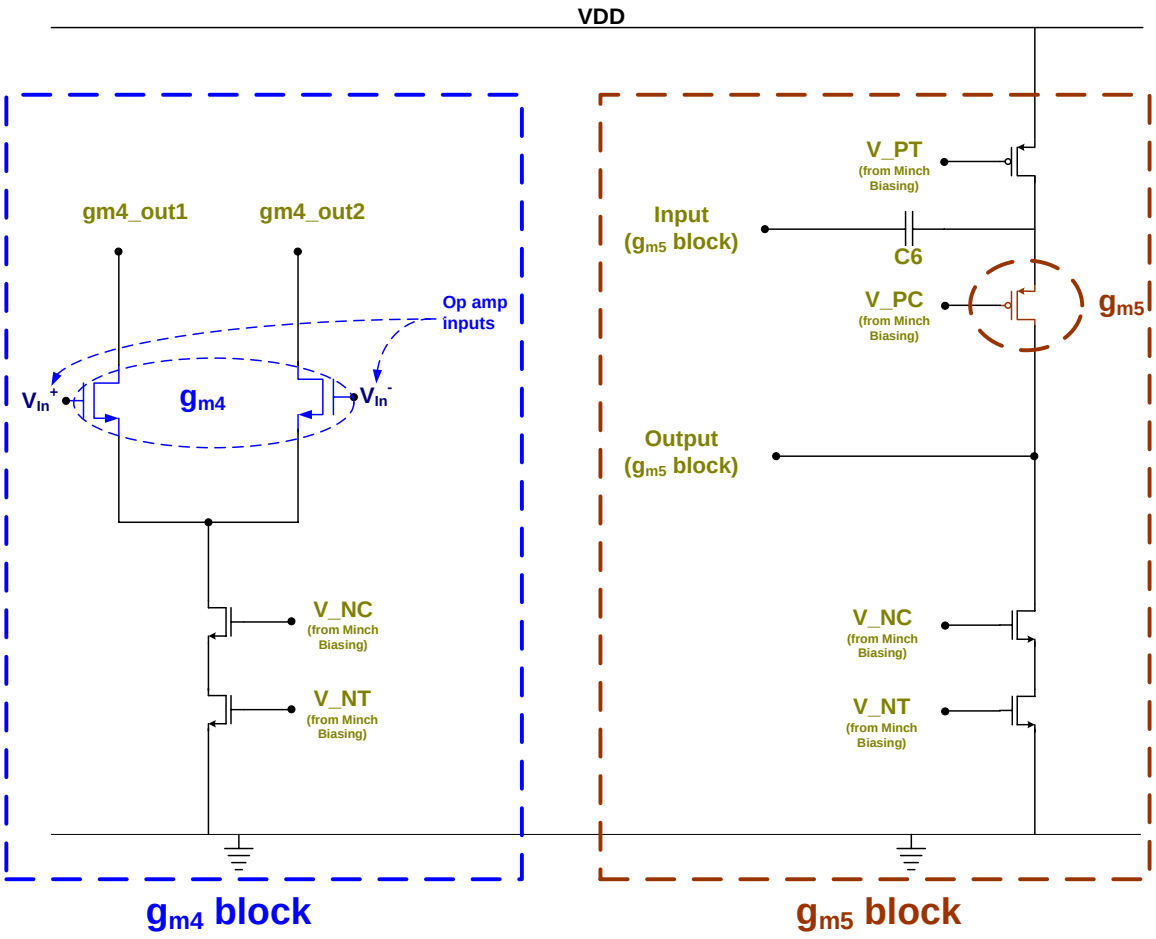

Figure 3.10. Transistor-level schematics of the g_{m4} and g_{m5} blocks

3.3 Simulation results and analysis

The earlier sections discussed the CT-amplifier architecture, its compensation topology and the stability criterion for achieving the desired phase margin. This section presents the simulation results from Matlab [63] using the transfer function shown in (29), followed by the transistor level simulation results from Eldo [64]. All the transistor-level simulation results shown in this section are obtained using the Eldo simulator with 5-V V_{DD} using the foundry models. The post layout extracted netlist is used for all the simulation results presented and discussed in this section.

Matlab is used to verify a) the functionality of the transfer function, b) the phase margin, and c) sensitivity of the pole-zero locations with different parameters. It is also used to understand the parameter sensitivity of open-loop gain and phase margin.

All the Matlab and Eldo simulations were performed with a 20 pF load. Without any random transistor mismatch, simulation results showed a very small offset. Hence, Monte Carlo simulations were performed on offset to observe more practical results and the average offset over 200 samples was −1.7 mV. Figure 3.11 shows the offset from Monte Carlo simulations with a ±4σ variation in threshold mismatch between various transistors, using Gaussian distribution. The setup used for the Monte Carlo simulations will be discussed in detail in Section 4.2.3.5.

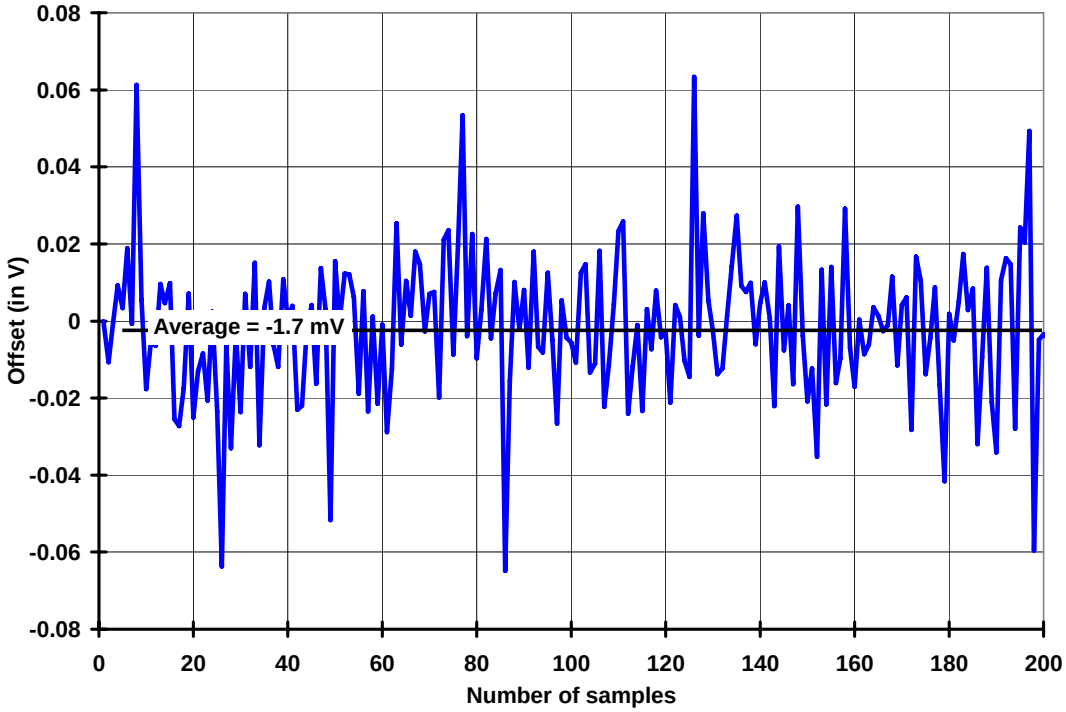

Figure 3.11. Monte Carlo simulation of offset from 200 samples

Figure 3.12 shows the simulation result of the input common mode range of the CT-amplifier. This shows that the ICMR of the CT-amplifier ranges from 0.7 V – 4.7 V for a single 5-V supply. The setup used for this simulation offers an optimistic estimate of the ICMR, as this uses the output voltage of the amplifier, rather than the operational mode of the input differential pair and tail current source transistors.

Figure 3.13 and Figure 3.14 show the open-loop gain and phase for the frequency compensated CT-amplifier from Matlab and Eldo simulations, respectively. The plots show that the amplifier has a gain greater than 120 dB, phase margin over 75º, and a bandwidth of approximately 12 MHz from both the Matlab and Eldo simulations.

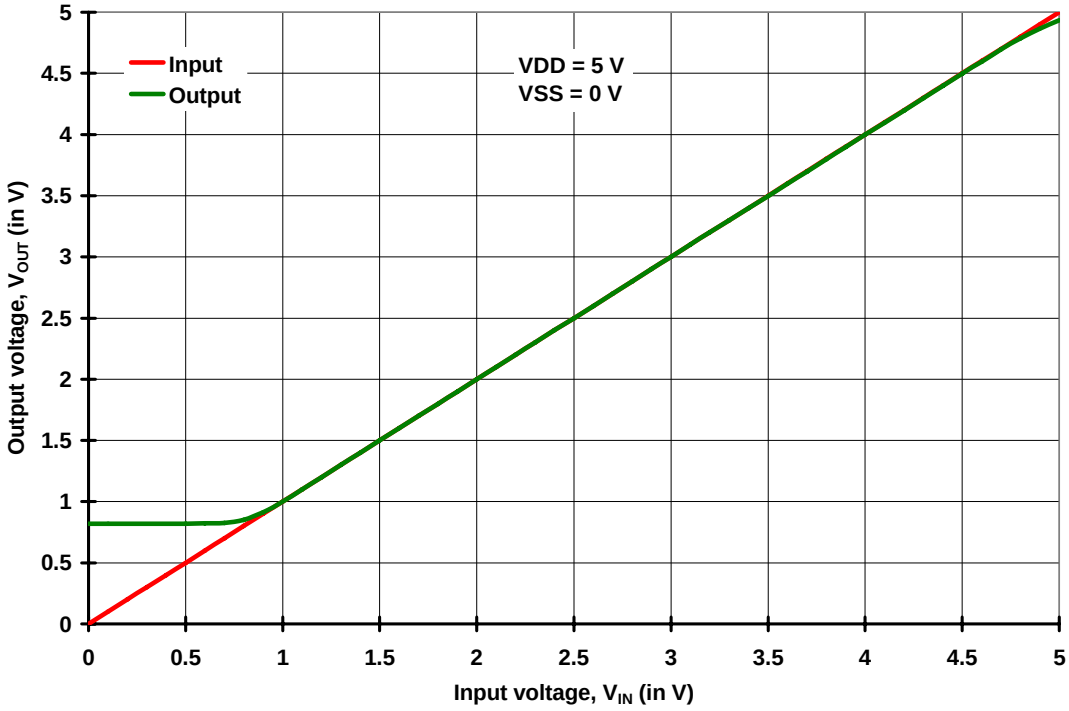

Figure 3.12. Simulation result of the ICMR from Eldo

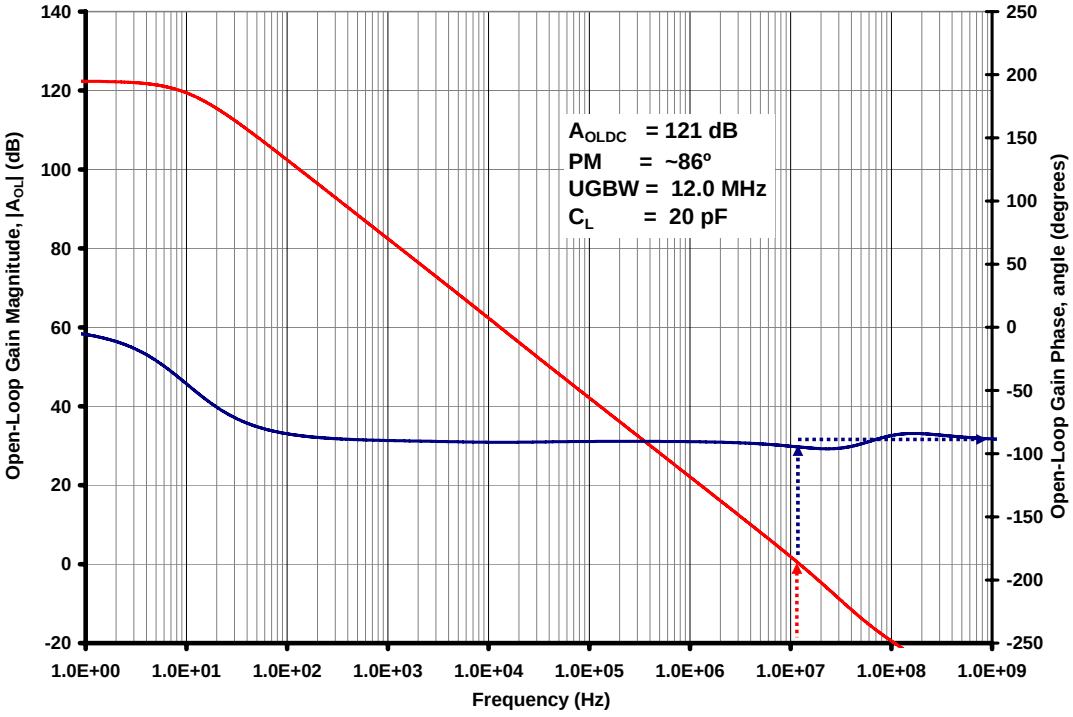

Figure 3.13. Matlab simulation results of the open-loop gain and phase

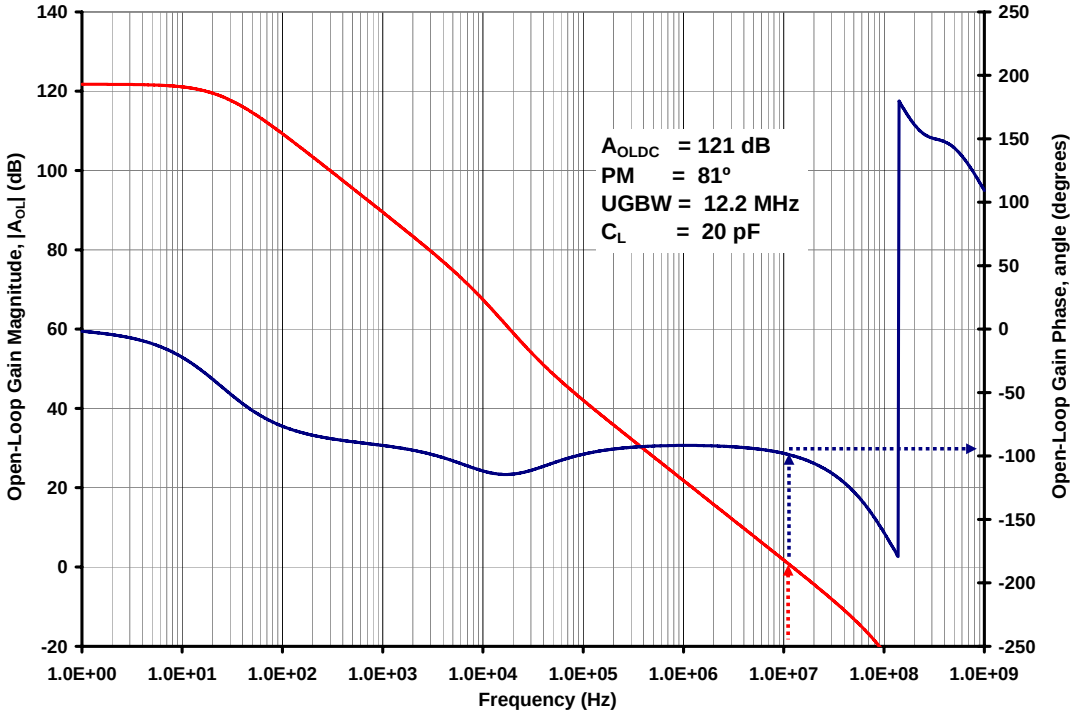

Figure 3.14. Eldo simulation results of the Open-loop gain and Phase margin

The Matlab phase plot remained flat until 10 MHz and the unevenness in the plot shows a pole-zero mismatch in the transfer function between 10 MHz and 100 MHz. Since this pole-zero mismatch is present within a decade of the UGF, it has an impact on the phase margin. The deviation in the phase margin between the Matlab simulations (86º) and the hand calculations (90º) can be attributed to the mismatch in the pole-zero cancellation at high frequency.

A pole-zero constellation map from the Matlab simulation shows a mismatched pole-zero cancellation at approximately 100 MHz. Similarly, the pole-zero analysis from the transistor level Eldo simulations showed a mismatched pole-zero around 16 kHz. This is the source of unevenness in the phase plot from the transistor-level simulations.

Figure 3.15 and Figure 3.16 show the simulated small-signal step responses of the amplifier. This simulation is performed with the CT-amplifier operating in unity-gain non-inverting feedback configuration with a load capacitance of 20 pF. The simulated 10-90% rise and fall times were 26.7 ns and 25.8 ns, respectively.

Figure 3.17 presents the simulated large-signal step response. Here the CT-amplifier is operated in a non-inverting unity gain feedback configuration with a 20 pF load. The simulated positive slew-rate was 7.4 V/μs, while the negative slew-rate was 7.5 V/ μs. It is clear from these results that this op amp offers a very symmetrical slew-rate.

Table 3.1 shows the summary of the simulation results obtained from Eldo. Simulation results of power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) without any mismatches in threshold voltage or current mirrors showed a promising though overly optimistic result. To verify the sanity of these results, Monte Carlo simulations were performed on both PSRR and CMRR, which will be presented, analyzed and compared with the measured results in Section 4.2.3.5 and Section 4.2.3.6 respectively.

Figure 3.18, Figure 3.19 and Figure 3.20 show the transistor level schematic of the CT-amplifier with frequency compensation and bias current values.

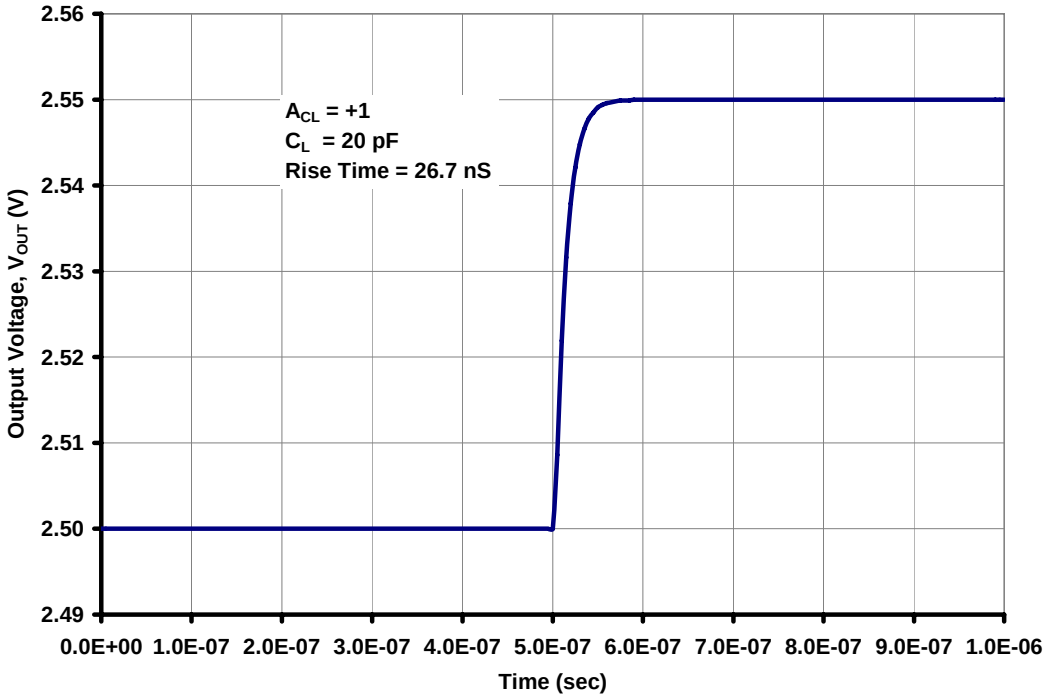

Figure 3.15. Small-signal rise-time simulation result from Eldo.

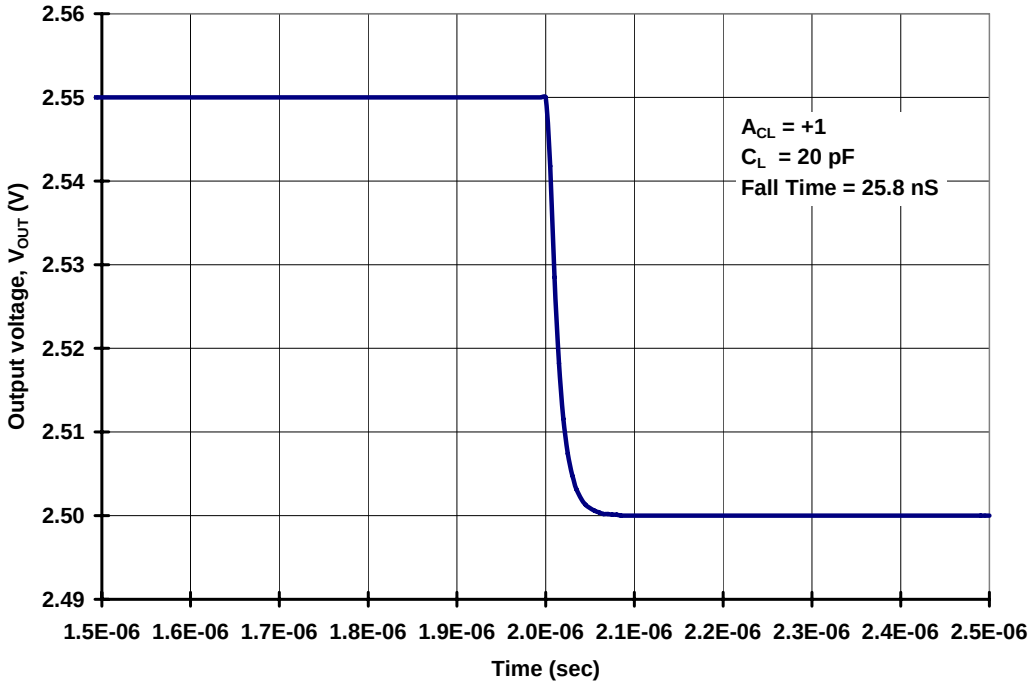

Figure 3.16. Small-signal fall time simulation result from Eldo

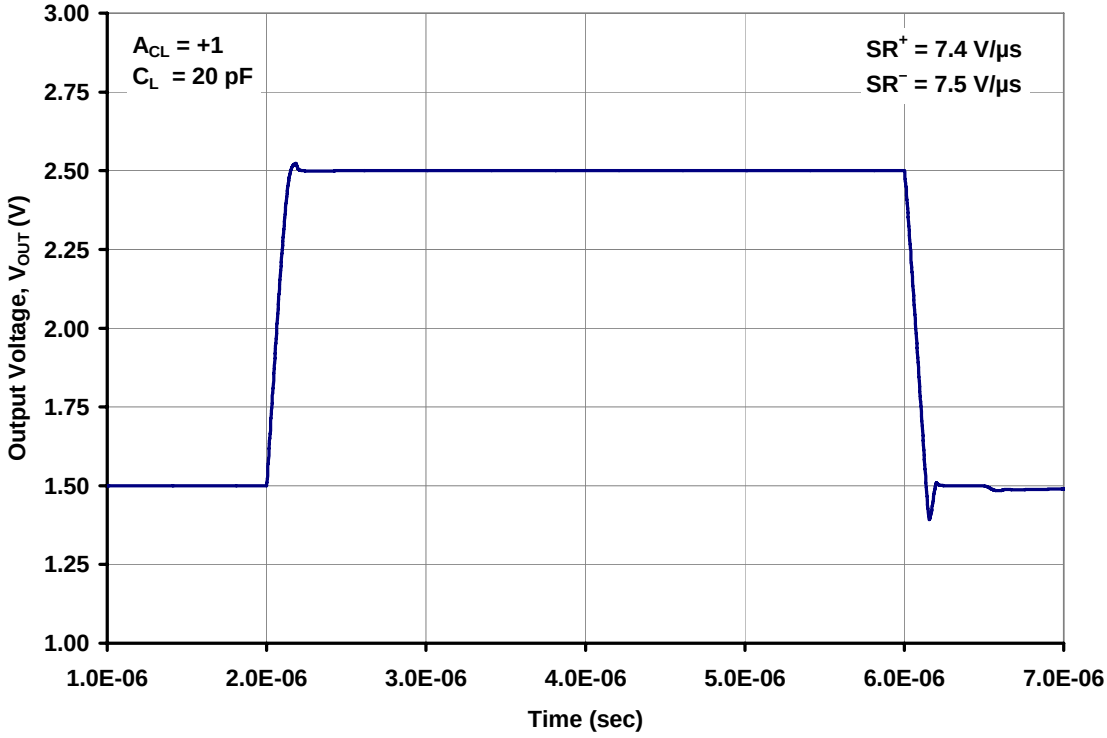

Figure 3.17. Slew-rate simulation results from Eldo.

Table 3.1. Simulated performance of the CT-amplifier from Eldo (C_L = 20 pF)

Parameter	Simulated Value
Power Supply	5.0 V
Supply Current	1.01 mA
ICMR	0.7 V - 4.7 V
Open-loop Gain	> 120 dB
Unity-Gain Bandwidth	> 12 MHz
Phase Margin (C_L = 20 pF)	≈ 90°
Slew Rate (C_L = 20 pF)	> 7 V/µs

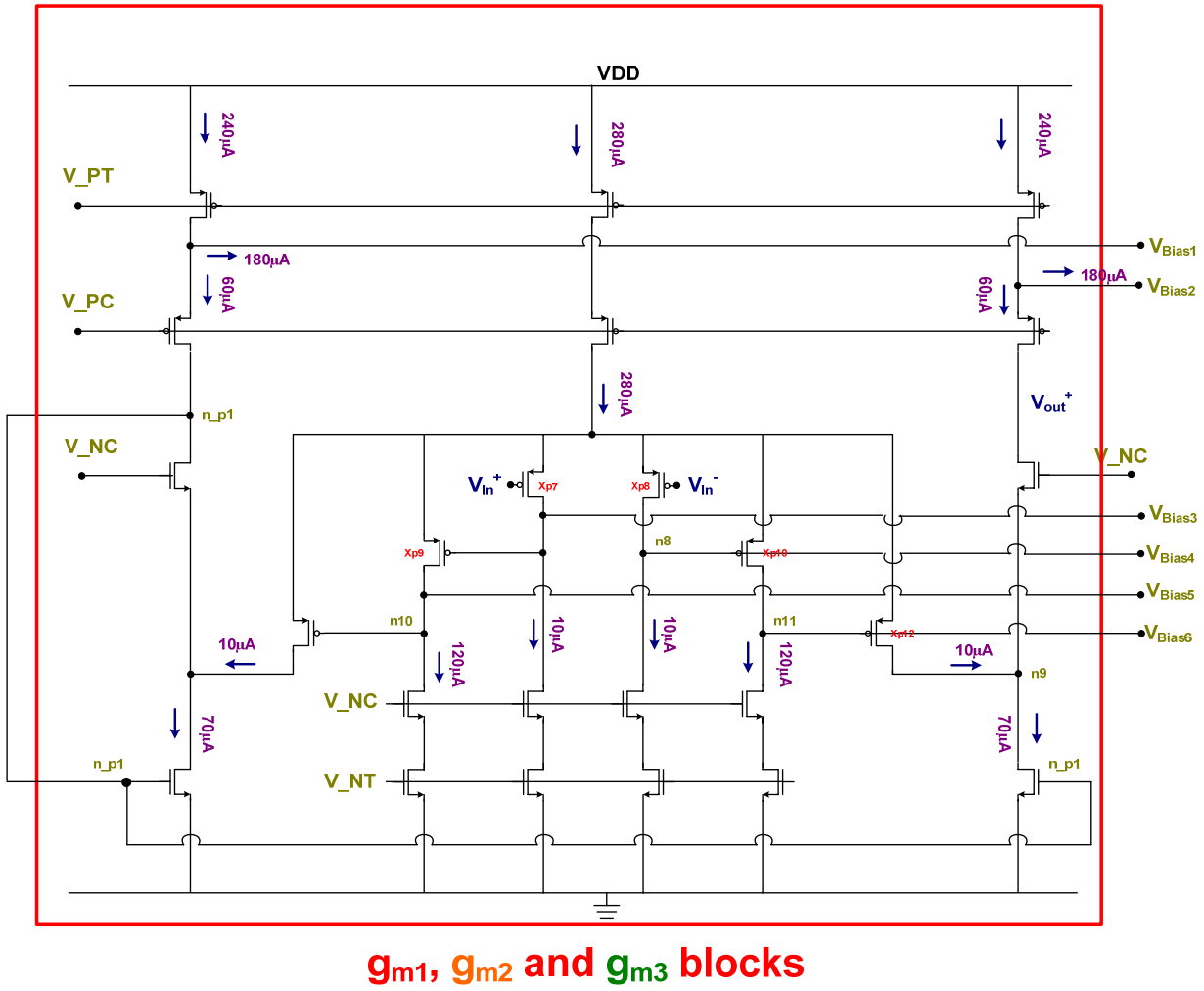

Figure 3.18. Part I of the transistor level schematic of the CT-amplifier

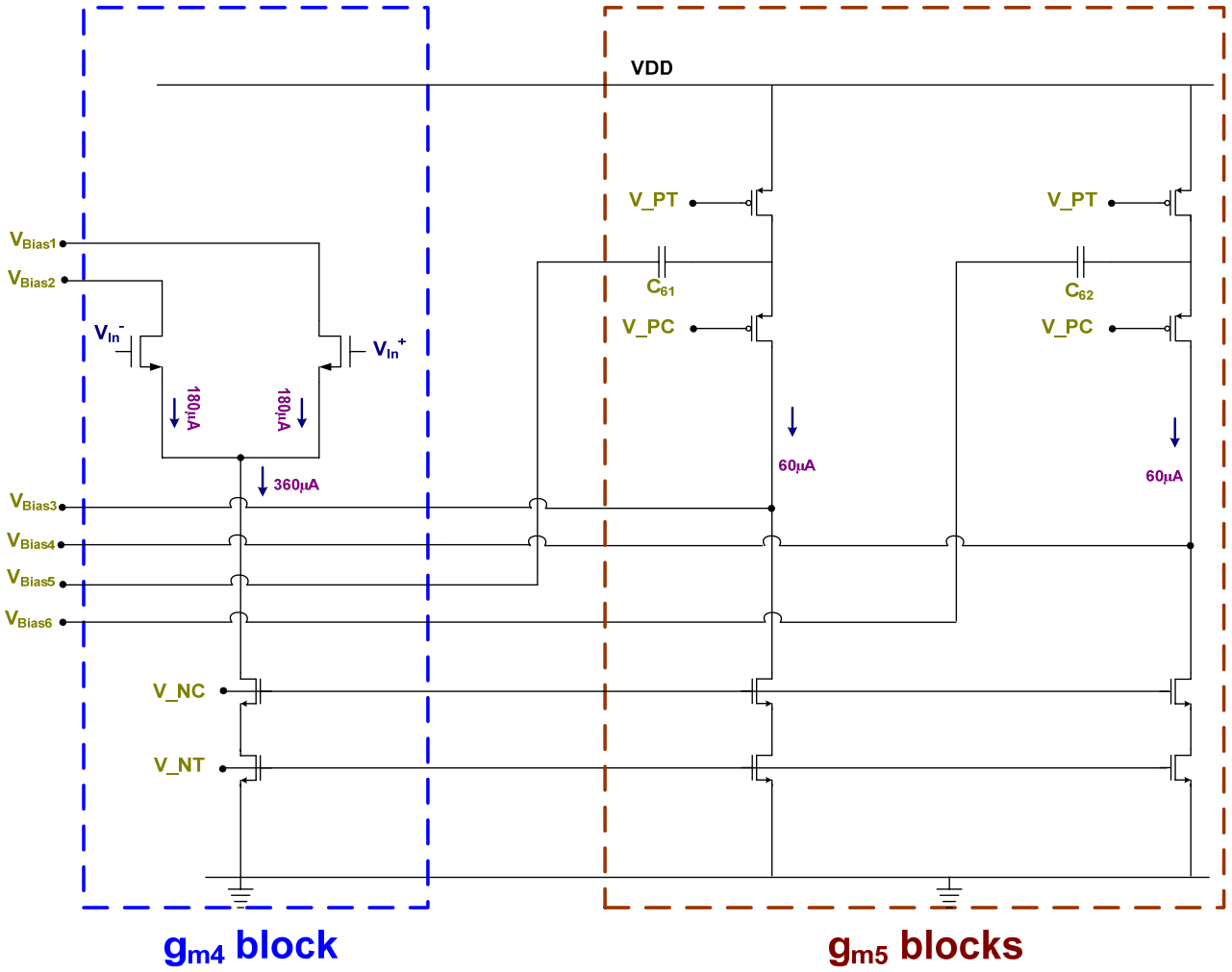

Figure 3.19. Part II of the transistor level schematic of the CT-amplifier

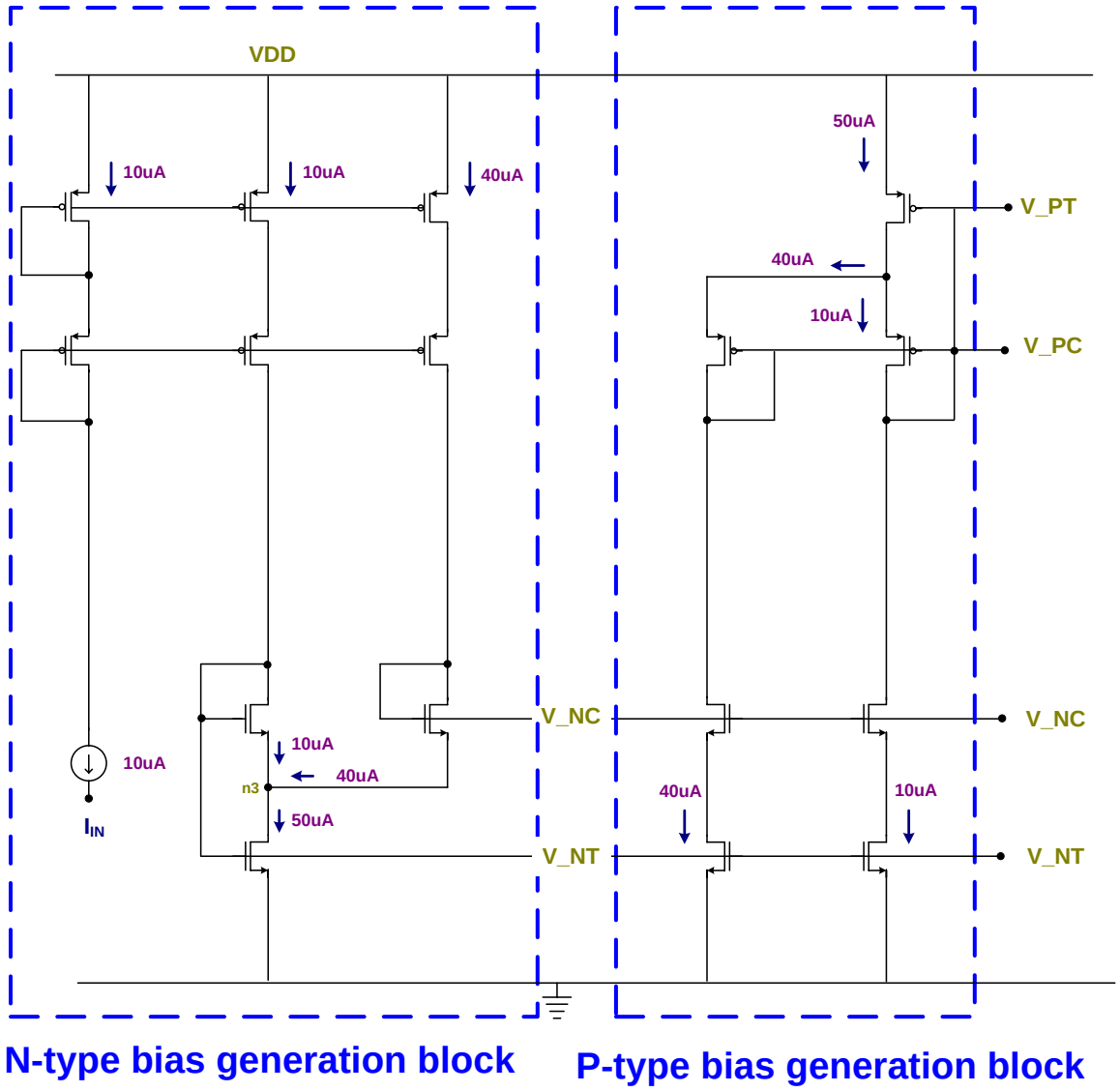

Figure 3.20. Part III of the transistor level schematic of the CT-amplifier

3.4 Conclusions

In this chapter the basic idea of the compound transconductance element and its performance characteristics were discussed. It shows the efficiency in achieving gain similar to that of previous multi-stage amplifiers with power consumption comparable to that of a conventional single-stage amplifier. Next, the architecture of the compound transconductance element was compared with that of a conventional multi-stage amplifier, and its novelty was discussed. This is supported by the literature review presented and discussed in the previous chapter. The presence of multiple high impedance nodes with poles below the UGF demanded a unique compensation topology. The mathematics underlying the transfer function of the novel compensation topology and its stability criteria was analyzed. Finally, simulation results from Matlab and Eldo were presented to show a completely functional all-inverting gain stage, compound transconductance element based operational amplifier.

4. Analysis of measurement results of the compound transconductance amplifier

This chapter presents a detailed analysis of the measurement results of the compound transconductance amplifier, which was implemented in a 0.5-μm bulk CMOS process. However, to provide context for these results, let us review the previous chapters before proceeding further. Chapter 2 discussed the basic classification of multi-stage amplifiers and analyzed each of them in detail. Later the multi-stage amplifier compensation techniques were classified based on the number of capacitors used in the compensation network. This is followed by a discussion of the various compensation topologies, analyzing one from each classification. Chapter 3 presented the motivation behind the need for high-gain multi-stage amplifiers and the mathematics involved with the CT element analysis. Later the uniqueness of the CT element that mimics the nature of a multi-stage amplifier was analyzed. This is followed by motivation, discussion and design of a novel compensation topology and its assumptions. That chapter concludes with the presentation of Matlab and Eldo simulation results of the CT-amplifier.

In this chapter, measurement results of the CT-amplifier are analyzed and compared with the simulation results. Then the performance characteristics of this amplifier are compared with prior art multi-stage amplifiers. This chapter concludes with the discussion of the tools used for this research and summary of the measurement results.

4.1 Implementation and layout

Two different versions of the design were implemented and sent for fabrication. The first version included the basic design with minimum number of pin connections while the second version had internal nodes padded out for additional analysis and debugging if needed. Since some of the debugging nodes of the CT-amplifier offer high impedance and are sensitive to loading, analog buffers were used to minimize the loading effects. Figure 4.1 shows the chip-level microphotograph of the CT-amplifier.

The design was implemented in a 0.5-µm bulk CMOS process and occupies an area of approximately 0.25 mm^2 (644 µm × 390 µm). This includes the core amplifier and its compensation network with capacitors.

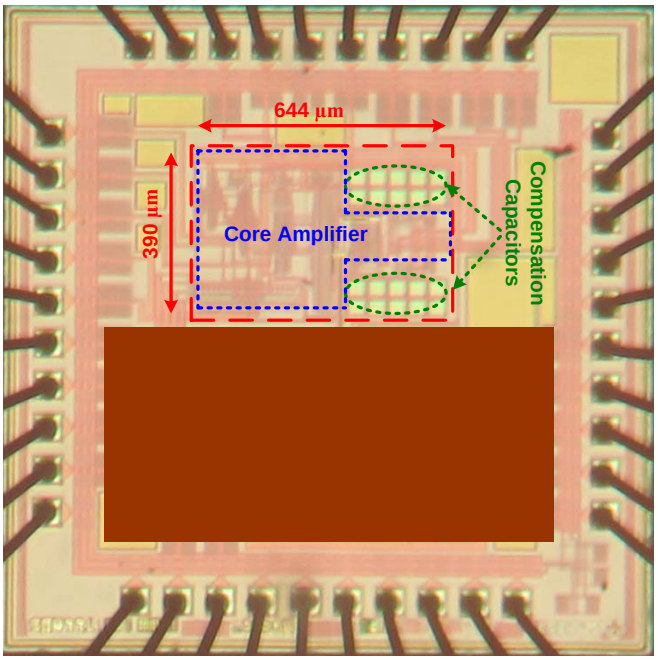

Figure 4.1. Chip-level microphotograph of the CT-amplifier

4.2 Measurement results

The fundamental contribution of this research is the development of an amplifier using the CT element with high open-loop gain for use in analog applications requiring high linearity. Design specifications were chosen to guide the design phase. The design goals for this amplifier are as follows:

- Develop an amplifier using the CT element that offers open-loop gain comparable to conventional multi-stage amplifiers,
- Develop the compensation architecture for an all inverting gain stage based op amp, and
- Develop an op amp that offers commensurate performance in all other parameters when compared to multi-stage amplifiers.

This section is broadly divided into three sub-sections: a) first sub-section discusses the description of the test setup and printed circuit board (PCB), b) DC parameter characterization results, and c) AC and transient parameter results. Throughout the course of this dissertation, a sample of 4 chips was used for characterization. The goal of the measurements section is to characterize and analyze basic parameters such as small-signal bandwidth, open-loop voltage gain, phase margin, slew-rate, power dissipation, input common-mode range, common-mode rejection ratio, power supply rejection ratio and offset voltage.

4.2.1 Test configuration and PCB

The CT-amplifier discussed above was sent for fabrication in Spring 2006 on a 0.5-µm bulk CMOS process. The amplifier requires an external 10 µA current sink and a 5-V power supply for characterization. To simplify the testing of all the performance parameters, complementary power supplies (+/– 2.5 V) were used. A printed circuit board has been developed for characterization. Figure 4.2 shows the complete schematic of the PCB used for characterizing this op amp. The external current sink is provided by a Keithley 2400 sourcemeter. Depending on the type of test being performed on the device under test (DUT), various jumpers are manually added or removed on the PCB. For the DC measurements like offset and ICMR, the inverting input of the DUT is simply shorted to the output of the DUT ('V_{OUT}'), and the input voltage is applied through the banana jack via jumper 'J3'. For offset measurements, jumper 'J2' is used instead of 'J3'. For open-loop gain measurements, 'J2' is shorted and 'J6' is used to apply the test signal from a function generator. For small-signal and large-signal step responses, the DUT receives the input signal through 'J3', and 'J1' is shorted thus buffering the DUT. The output signal 'V_{OUT_BUFFER}' is used for capturing the step responses on the oscilloscope. The mid-supply voltage ('V_{MID_SUPPLY}') is applied to the non-inverting input terminal through 'J3', while the output of the DUT ('V_{OUT}') is connected to inverting input terminal of the DUT through 'J1', during the DC PSRR measurements. The CMRR measurement setup uses both amplifiers Amp-1 and Amp-2 and is connected to the DUT via 'J1', 'J4' and 'J5'. The complete schematics of the individual setups are shown in

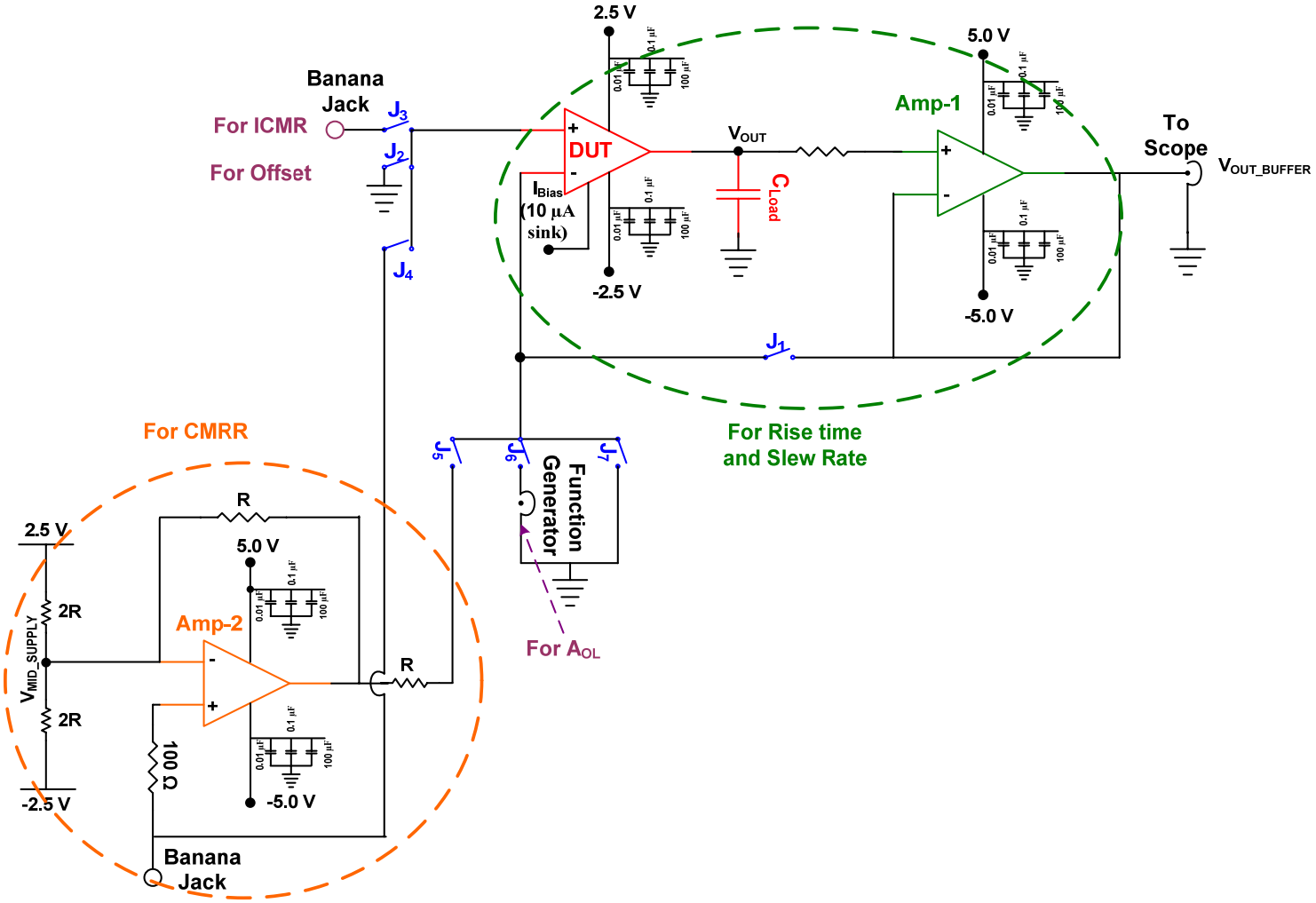

Figure 4.2. Complete schematic of the PCB for characterizing the CT-amplifier

[84] except that the DUT is buffered in the measurements performed during this research work. Amp-1 in the Figure 4.2 is used to buffer the DUT for driving large capacitive loads. The CT-amplifier is designed to drive a capacitive load of 20 pF. Since some of the measurements require the CT-amplifier to drive large capacitive loads, CT-amplifier is connected to a buffer, the output of which is monitored during these measurements. The Analog Devices parts AD829 and AD8055 were used as buffers during these experiments. From the preliminary buffer characterization experiments, it was found that the offset of the buffer is much larger compared to the offset of the DUT. Hence, during the offset and ICMR measurements, the CT-amplifier is connected in unity-gain non-inverting configuration without the buffer.

4.2.2 DC measurements

The DC parameters that are of interest are offset voltage and ICMR. The following sections discuss the individual measurement setups, the measurement results and compare them with the simulation results for analysis.

4.2.2.1 Offset

Complementary power supplies (+/– 2.5 V) were applied to the DUT during this measurement. The DUT is connected in unity-gain non-inverting configuration with the non-inverting input connected to ground while the inverting terminal tries to follow the non-inverting terminal. Twenty samples were taken and averaged to enhance the measurement accuracy. Table 4.1 shows the measured input referred offset from 4 different chips of the CT-amplifier.

Table 4.1. Measured input referred offset voltage of the CT-amplifier

	Offset
DUT #1	6.8 mV
DUT #2	-0.832 mV
DUT #3	3.3 mV
DUT #4	17.8 mV

Offset of an op amp consists of systematic (limited by the open-loop gain and asymmetry of the design and layout) and random offsets. Simulation results show a very high open-loop gain (exceeding 120 dB) and the design is inherently symmetric till the output of the CT element. Hence in the present scenario, a low offset (1 – 2 mV) was expected. On the contrary, higher offsets were measured. The higher offset in the measurement results could be attributed to the mismatch error in the current mirrors because common-centroid technique could not be applied to all the mirrors across the whole design. Random offset could be minimized by increasing the number of chips (4 chips in this case) used in the offset estimation. Increasing the number of chips would average out the random offset across multiple chips.

4.2.2.2 ICMR

The hand analysis of the CT-amplifier showed that the input common-mode range would be between ($3V_{DS,SAT} + V_{TN} + V_{SS}$) to ($V_{DD} - 2V_{DS,SAT}$). In the present case, this corresponds to approximately 1.2 V to 4.6 V (i.e., 1.2 V < ICMR < 4.6 V), assuming a $V_{DS,SAT}$ of 200 mV, $|V_{TN}| = |V_{TP}| = 600$ mV, $V_{DD} = 5$ V and $V_{SS} = 0$ V. In the measurement setup, the DUT is connected in unity-gain, non-inverting configuration and input voltage is swept from the negative supply rail to the positive supply rail. It is clear

from the measurement results that the input and output voltages track well between voltages from –1.8 V to 2.2 V (see Figure 4.3), which translates to 0.7 V – 4.7 V for a single supply voltage of 5 V. This measurement result provides an optimistic estimate of the ICMR compared to the actual ICMR of the amplifier. Simulation results from the same setup showed the ICMR to be approximately 0.7 V – 4.7 V. This shows good agreement between the simulation and measurement results.

4.2.3 AC and Transient measurements

Buffers are used to minimize the loading effect of various external parasitic capacitances on the DUT during small-signal and large-signal step responses and CMRR.

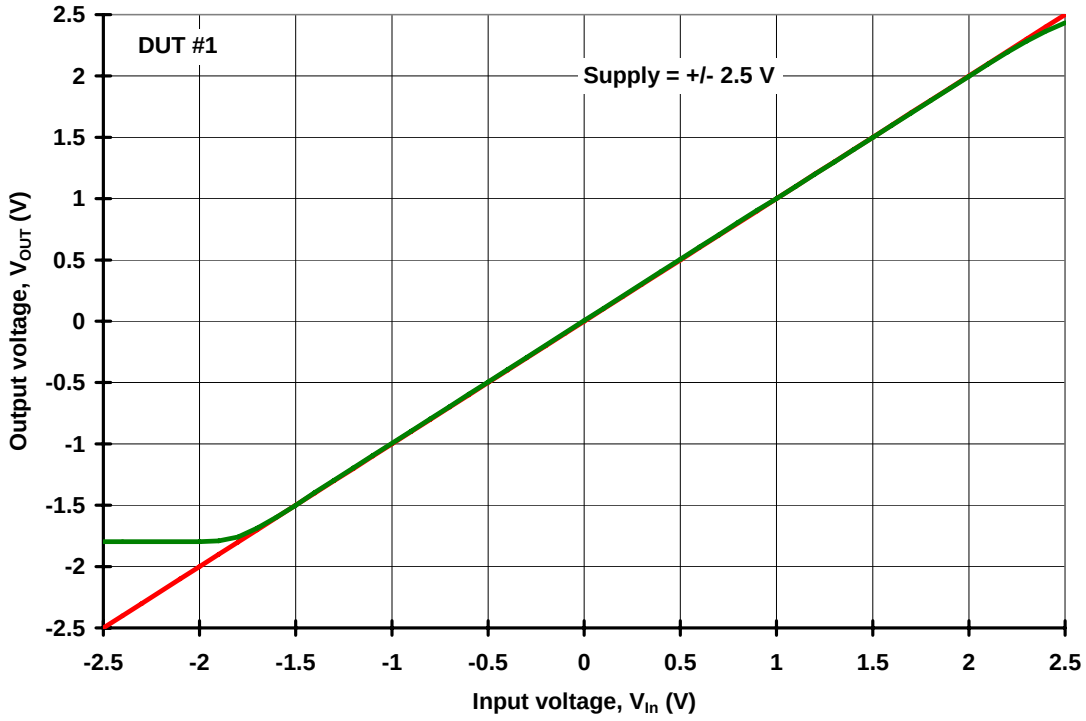

Figure 4.3. Measured ICMR from the CT-amplifier

4.2.3.1 Open-loop gain (A_{OL}) and Small-signal Unity-Gain Bandwidth (UGBW)

Open-loop gain and small-signal unity-gain bandwidth are key design parameters of this project. The CT-amplifier is designed to offer high open-loop gain which is attributed to the high transconductance of the CT element. The A_{OL} of the CT-amplifier is measured in a two step process. The first step is used to measure the low frequency gain, while the second step is used to measure the high-frequency gain. A unity gain, inverting configuration is used to measure the low-frequency gain of the amplifier. The schematics and the detailed discussion are presented in [84]. For high-frequency measurements, a buffer is used in series with the DUT. A 250 mV_{pk-pk}, sine wave was used as the input signal to the inverting terminal of the DUT, while the non-inverting terminal is connected to mid-supply. The ratio of the input voltage to the differential input voltage ('V_{Error}') gives the open-loop gain of the DUT.

The DUT (CT-amplifier) is designed for driving on-chip capacitive loads. Since the DUT has to drive resistive loads during low-frequency measurements, a high resistance (500 kΩ) is used. Alternately, smaller resistors load the CT-amplifier and the setup is unsuitable for measuring the open-loop gain. 'V_{Error}' is measured using a network analyzer. But this setup has a limitation. This can be used to measure the gain within a certain bandwidth, as the input capacitance (input capacitance of the DUT + probe capacitance) in conjunction with the net input resistance forms a pole within the UGBW. Hence, this setup is used to measure the open-loop gain up to 100 kHz. For high-frequency measurements, a buffer with good drive capability is used in series with the

DUT. The measurement results from both the setups are merged and are shown in Figure 4.4.

The plot in Figure 4.4 shows a good match between the simulated and measured results from frequencies as low as 400 Hz. A trendline with –20 dB/dec slope is drawn for comparison purposes. For frequencies below 400 Hz, the open-loop gain of the CT-amplifier is higher than 100 dB and it becomes difficult to measure the error voltage accurately. Also, the number of averages measured for frequencies between 300 Hz – 1 kHz is two in contrast to ten averages for frequencies above 1 kHz. Because of this, the measured result swings about the simulated open-loop gain for frequencies below 1 kHz. Measurement results were conducted from 300 Hz – 1 MHz and the data

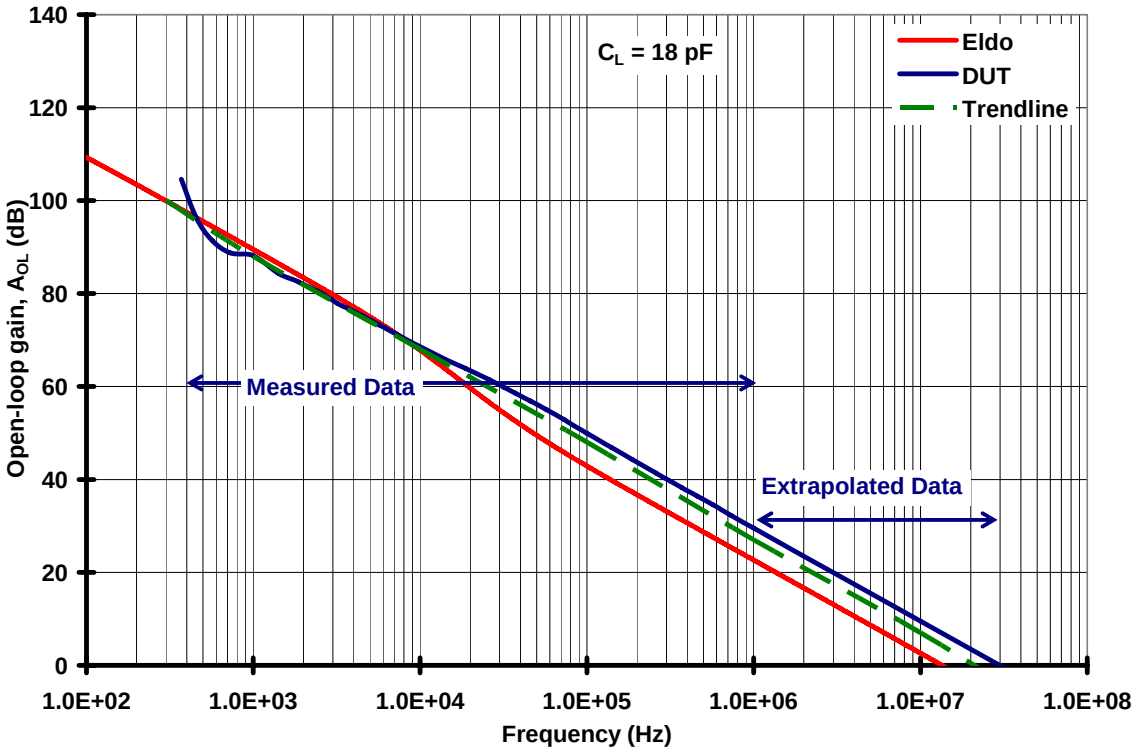

Figure 4.4. Measured open-loop gain and UGBW from the CT-amplifier

was extrapolated to estimate the UGBW. This resulted in a UGBW of approximately 19 MHz. Simulations of the CT-amplifier show that the UGBW is approximately 14 MHz for similar load conditions (18 pF instead of 20 pF as in Chapter 3). This increase in bandwidth can be attributed to mismatch in pole-zero cancellation at a frequency of approximately 16 kHz during simulations, i.e. the mismatched pole-zeroes are referred by the terms $\frac{1}{(1+sr_3C_3)}$ and $\left(1+s\frac{C_6 g_{m4}}{g_{m1}g_{m3}}\right)$ in (31) of Chapter 3. The pole-zero mismatch is much less significant in the measurement result compared to that of simulations, which contributed to an increase in the UGBW in the measurement results.

Since there is a good match between the simulation and measurement results of the CT-amplifier's open-loop gain, it can be expected that phase margin matches well between simulation and measurement results. The simulation results from both Matlab and Eldo show that this amplifier behaves as an over-damped system with a phase margin in excess of 80°. Measurement results for the phase margin will be discussed in section 4.2.3.2. Figure 4.5 shows the root-locus/pole-zero constellation of the complete transfer function shown in (29) of Chapter 3.

The poles of the transfer function are shown as '×' while the zeroes are shown as 'circle'. The root-locus shows that the dominant pole is present at 23 Hz. From the plot, it appears that the poles and zeroes cancel each other well, but there is actually a very small mismatch in the pole-zero cancellation. This can be seen from the open-loop gain plot depicted in Figure 3.14. From the simulation and measurement plots of the open-loop

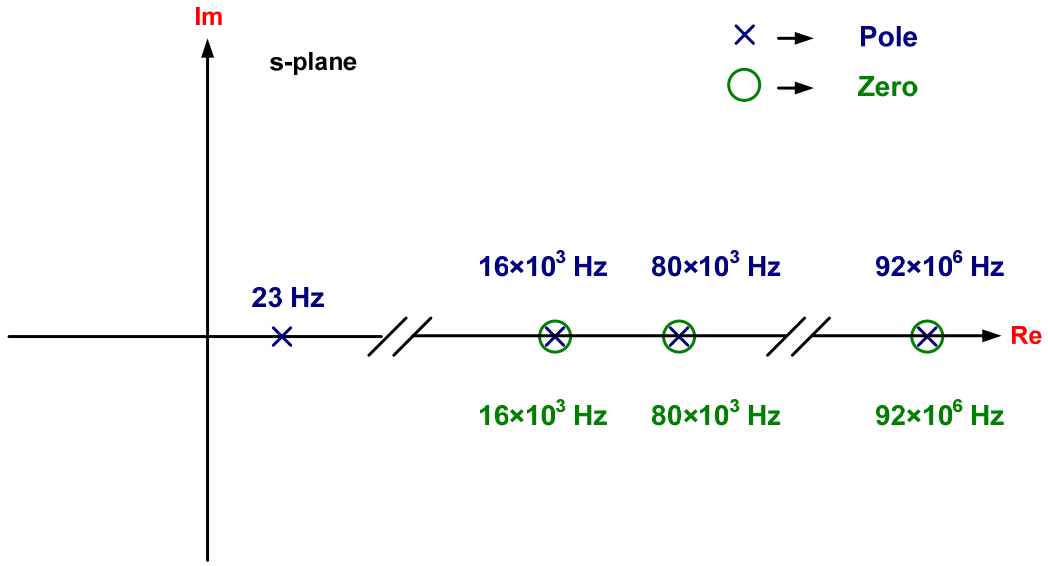

Figure 4.5. Root-locus of the compensated CT-amplifier from MATLAB

gain, it was clear that the pole-zero cancellation is better in the measurement results than in simulation results.

4.2.3.2 Small-signal rise and fall time

Small-signal step response is one of the key parameters of an operational amplifier and can be used to infer other parameters like UGBW and stability (phase margin), other than the obvious rise and fall times. During the course of this document, the time taken by the output signal ('V_{OUT}') to rise (fall) from 10% (90%) to 90% (10%) of the input signal is used to estimate the rise and fall times, respectively. The Analog Devices part AD8055 was used as buffer and the setup for the small-signal rise time measurement is shown in [84]. From the PCB schematics shown in Figure 4.2, it is clear that the buffer is present within the negative feedback loop of the system. Simulations were repeated with a 55.5 mV_{pk-pk} to match the signal amplitude used during characterization. Figure 4.6 shows the measured rise time from DUT #1 as compared to the simulation result.

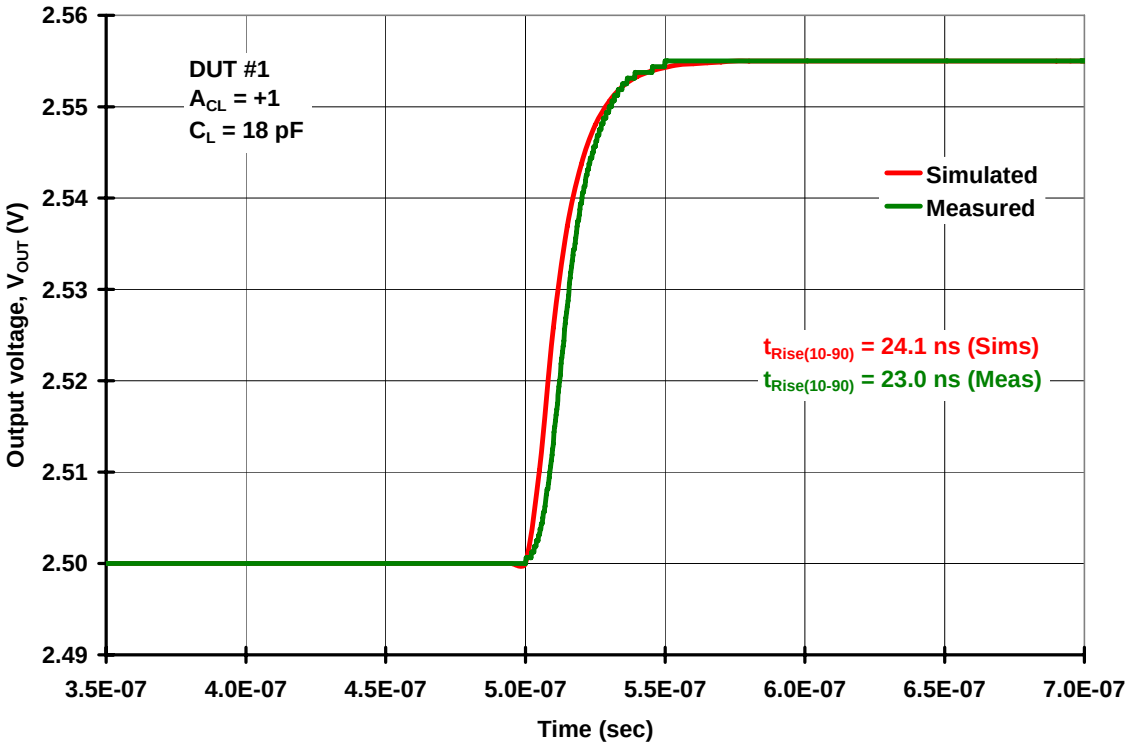

Figure 4.6. Comparison between the measurement and simulation results of the small-signal rise time

The rise time from DUT #1 was measured to be approximately 23 ns, while the simulation results show the rise time to be approximately 24.1 ns, both cases while driving a load capacitance of 18 pF. The mismatch between these results is close to 5%, indicating good agreement between the measured and simulated rise times. In the case of a single-pole system and using a first-order approximation, UGBW can be mathematically derived from the small-signal rise time with the following relation [88]:

$$UGBW = \frac{0.35}{t_{rise\,(10\%-90\%)}}$$

Using the above relation, the measured rise-time results estimate UGBW to be approximately 15.2 MHz. Repeated simulation results with a load capacitance of 18 pF show the UGBW to be approximately 14 MHz. This can be better understood by analyzing the pole-zero locations at 16 kHz in both the measurement and simulation results. The increase in UGBW in the measured results is due to the proper cancellation of pole and zero present around 16 kHz while a mismatch is present in the simulations. Also, the pole was present ahead of the zero during the simulations, which further reduced the bandwidth.

Figure 4.7 shows the measured small-signal fall time compared to simulation result.

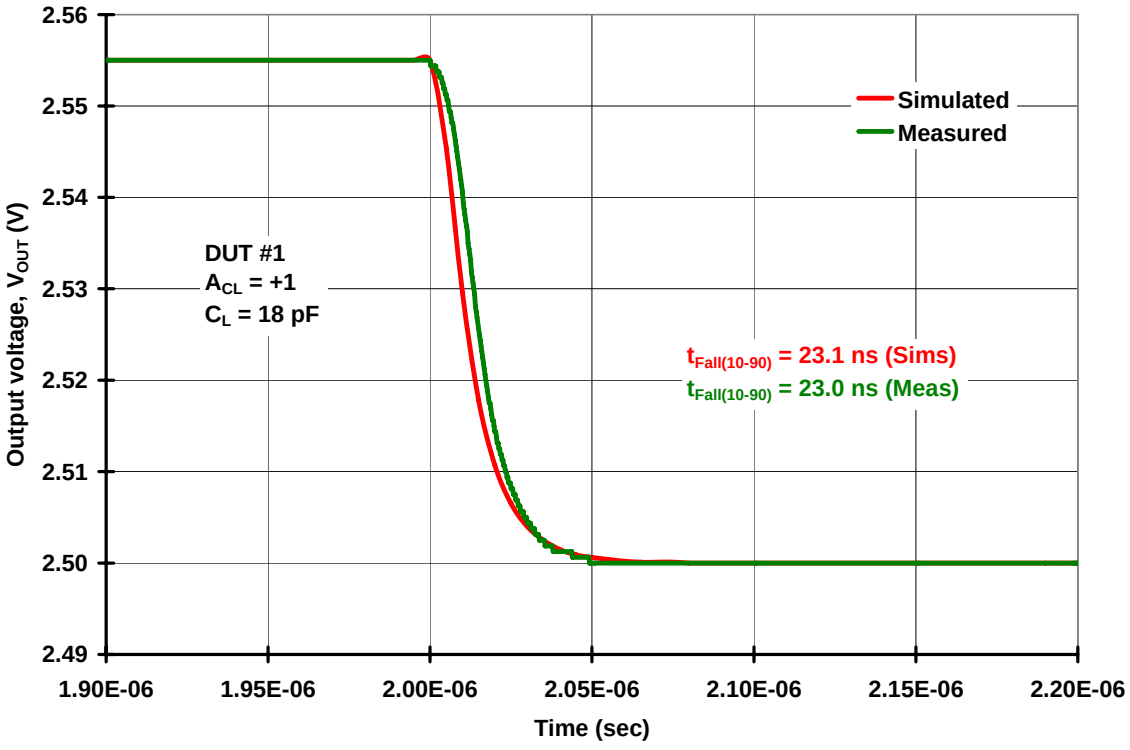

Figure 4.7. Comparison between the measurement and simulation results of the small-signal fall time

The small-signal fall time from the CT-amplifier driving a load capacitance of 18 pF was measured to be approximately 23 ns, while the simulation result shows fall time of 23.1 ns. This shows a good agreement between simulation and measurements.

Table 4.2 shows the measured rise and fall times for different chips. From the measurement results shown in Table 4.2, it is clear that the CT-amplifier offers very symmetrical rise and fall times. Phase margin can be easily estimated from the behavior of the small-signal step response of the system. Eldo simulations of the CT-amplifier indicate a stable multi-stage amplifier with a phase margin of approximately 86° while driving a load capacitance of 20 pF. This small-signal rise time simulation plot is shown in Figure 3.15. Since the system shows no ringing or peaking, it can be concluded that the CT-amplifier behaves like an overdamped system with a phase margin close to 90°. The measurement results for all the samples show a similar response to a 55.5 mV_{pk-pk} input signal.

Table 4.2. Measured small-signal rise and fall-times for various chips

	Rise-time (in ns)	**Fall-time (in ns)**
DUT #1	23	23
DUT #2	24	24.4
DUT #3	23.5	23.3
DUT #4	22.2	21

4.2.3.3 Slew rate

Slew rate is determined by the large-signal step response of the system. In this case, a 1.1 $V_{pk\text{-}pk}$ square wave is used as the input signal and the CT-amplifier is connected in non-inverting, unity-gain configuration driving a buffer. A buffer is used while characterizing the slew-rate, since the load capacitance combined with the probe capacitance might excessively load the CT-amplifier. The buffer is carefully chosen such that the measured results are not limited by its performance. The slope of the rising edge and falling edge of the large-signal step response correspond to the positive and negative slew-rates (SR^+ and SR^-) of the CT-amplifier, respectively. Figure 4.8 shows the measured rising and falling slew rates and indicate that the positive and negative slew rates for DUT #1 of the CT-amplifier is approximately 10.8 V/µs and 10.6 V/µs, respectively.

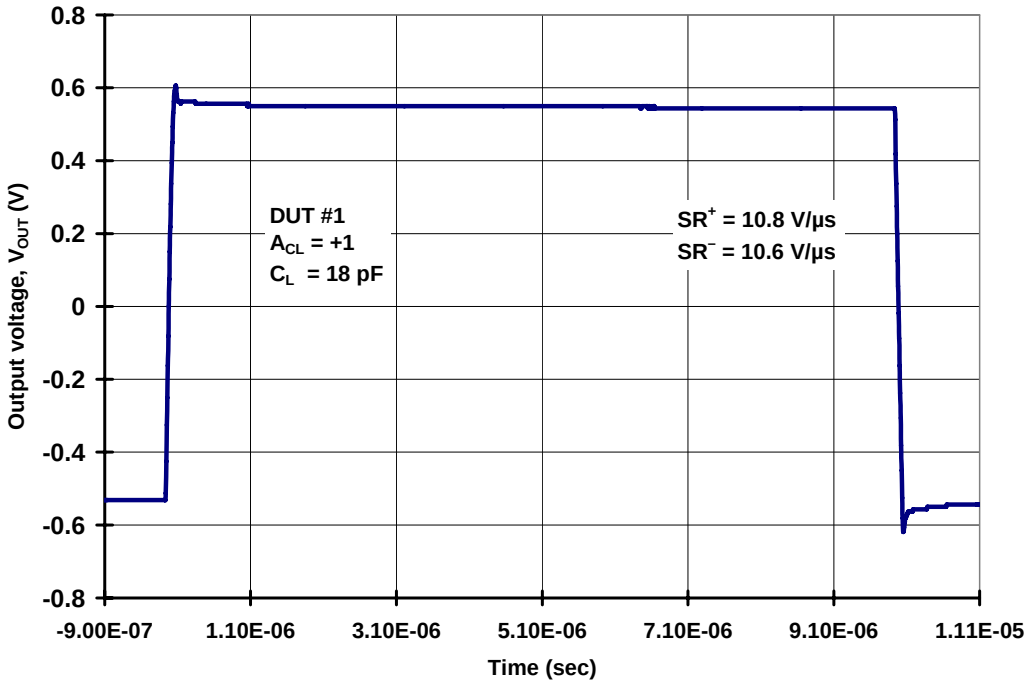

Figure 4.8. Measured slew-rate for DUT #1 of the CT-amplifier

Figure 4.9 and Figure 4.10 show a comparison between the measured and simulated positive and negative slew rates. It is clear that the slew rates from the measurements are much higher than the simulation results. Though the slew rates offered by the CT-amplifier are sufficient for general purpose applications, the measurement results are approximately 24% higher than the simulation results. As can be seen from the CT-amplifier schematic shown in Figure 3.8, the g_{m4} block primarily helps in improving the slew-rate. This discrepancy could be primarily attributed to the accuracy of the tail current of the g_{m4} block, i.e. the slew-rate of the CT-amplifier is directly dependant on the tail current of the g_{m4} block. If the tail current of the g_{m4} block is greater than 360 μA, then the amplifier will offer slew rates higher than 8.2 V/μs. From the measurement results, it could be inferred that the current through individual transistors of the differential pair of the g_{m4} block could be higher than 180 μA. This can be clearly understood from the power consumption of the complete CT-amplifier, which will be discussed in Section 4.2.3.4.

The measured positive and negative slew rates for all the samples are shown in the Table 4.3. It is clear from the measurement results that the CT-amplifier offers very symmetrical slew rates.

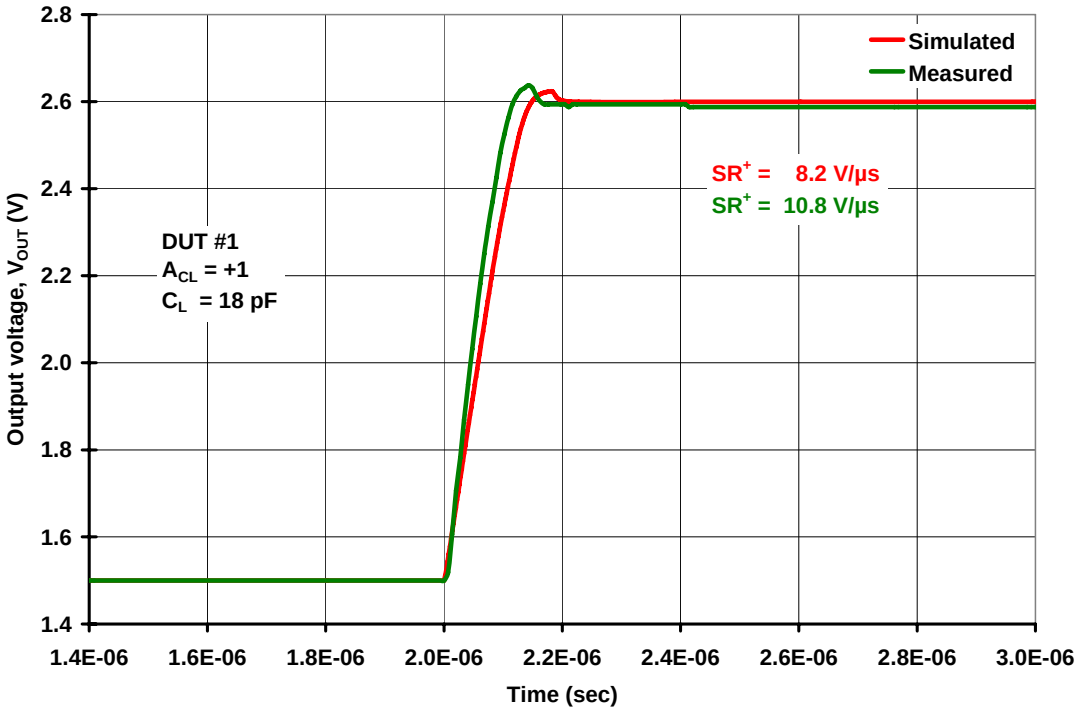

Figure 4.9. Comparison between the measurement and simulation results of the positive slew-rate

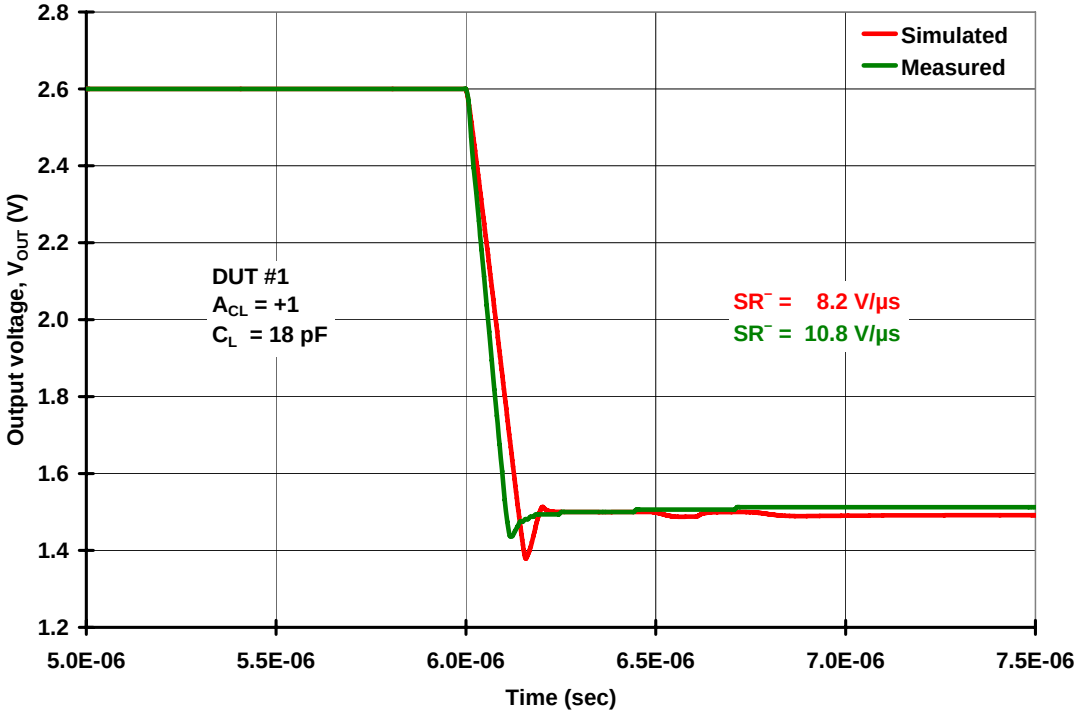

Figure 4.10. Comparison between the measurement and simulation results of the negative slew-rate

Table 4.3. Measured positive and negative slew-rate for the CT-amplifier

	SR^+ (V/µs)	SR^- (V/µs)
DUT #1	10.8	10.8
DUT #2	10.0	10.7
DUT #3	10.8	10.6
DUT #4	10.5	9.7

Table 4.4. Power consumption from 4 samples for the CT-amplifier

	I_{VDD} (mA)	Power (mW)
DUT #1	1.16	5.8
DUT #2	1.13	5.65
DUT #3	1.14	5.7
DUT#4	1.14	5.7

4.2.3.4 Power dissipation

Simulation results from Eldo show a total current dissipation of approximately 1 mA, resulting in a net power consumption of 5 mW. The net current consumption was measured through a multi-meter connected in series with the chip. In the physical layout design, care was taken to isolate the power supply pads of the CT-amplifier from the supply pads of other circuits on the chip so that the power consumption of the CT-amplifier could be accurately measured. The total current consumption was measured to be approximately 1.16 mA for DUT #1. Table 4.4 shows the power consumed by CT-amplifier from various samples.

Simulation results show a net current usage of approximately 1 mA resulting in a total power consumption of 5 mW. Measurement results show an increase of approximately 13% in the average current consumption, which could be attributed to the increased current usage by the g_{m4} block. This is the primary reason for the increased slew rates in the measurement results compared to simulation. Mismatches in the current mirrors could also contribute to the increased current consumption of the CT-amplifier. Common centroid technique is one of the many layout practices to minimize mismatch in current mirrors. But this technique could not be applied for all the mirrors in the CT-amplifier layout because the complete amplifier is partitioned based on functionality, and some of the mirrors are shared among various partitions. Common centroid technique, however, is applied to the current mirrors and other crucial elements within individual functional blocks.

4.2.3.5 Power-supply rejection ratio

Power-supply rejection ratio is another parameter that is used to analyze the performance of amplifiers. The setup used for measuring PSRR is discussed in [84]. The DC PSRR was measured for a variation of 10% of V_{DD}, which is 0.5 V. Thus the power supply is changed from 4.75 V – 5.25 V during the PSRR measurements in steps of 20 mV. Figure 4.11 shows the measured PSRR for DUT #1 of the CT-amplifier. The average PSRR measured over the desired range of the supply voltage is approximately 60 dB, which is lower than expected. Hence, an in-depth analysis was needed to understand the PSRR. Monte Carlo simulations were performed to further characterize the DC PSRR. Monte Carlo simulation is a type of analysis during which a specific or a group of parameters

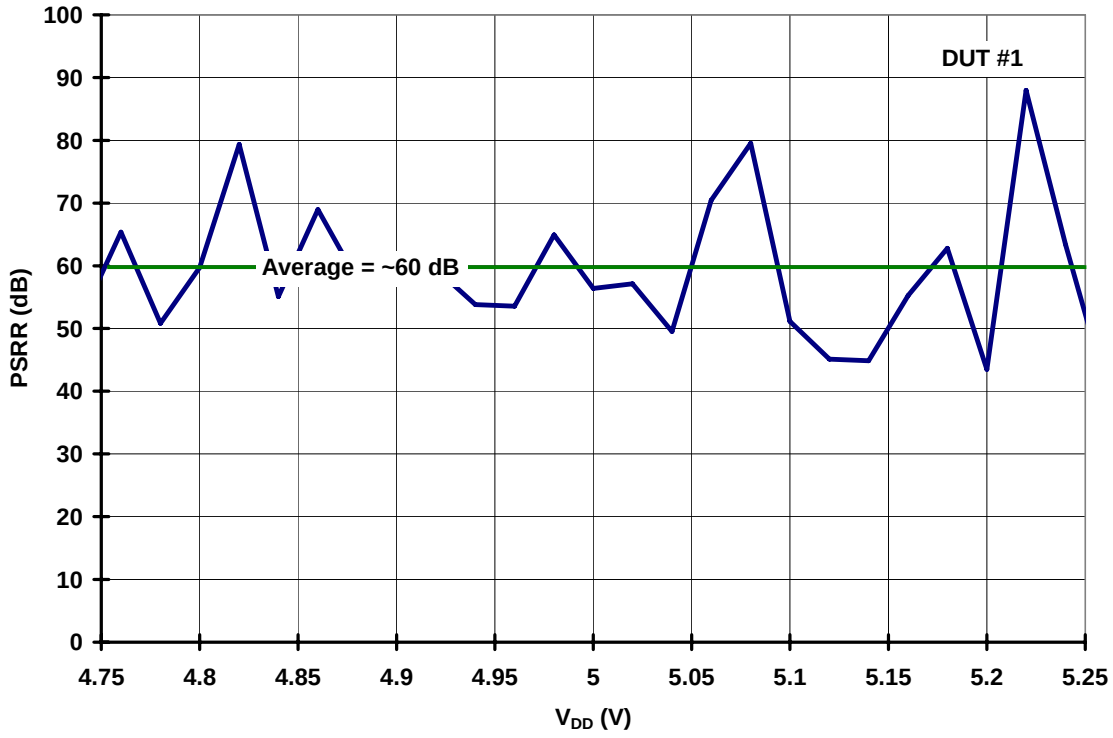

Figure 4.11. Measured PSRR vs. V_{DD} for the CT-amplifier

corresponding to either the model or circuit are varied according to a distribution (e.g. uniform), and the results are analyzed when the simulation is repeated a large number of times. BSIM3v3 level 49 models were used for the simulations throughout the course of this project.

The PSRR is given by [84]:

$$PSRR \equiv \frac{A_{DIFF}}{A_{PS}} = \frac{\frac{dV_{OUT}}{dV_{Error}}}{\frac{dV_{OUT}}{dV_{PS}}} = \frac{dV_{PS}}{dV_{Error}}$$

where 'dV_{PS}' indicates the variation in the power supply voltage while 'dV_{Error}' indicates the variation in the input referred offset as a function of supply voltage. It is clear from

the definition of the PSRR, that the offset of the amplifier plays a vital role. The offset of the amplifier is significantly impacted by mismatches in threshold voltage between the input transistors, which is dependant upon their areas. In the Monte Carlo simulations were performed on the CT-amplifier, the threshold voltage mismatch from the EKV model is used to estimate the worst case standard deviation, which is given by [85]

$$\sigma_{V_{Th}} = \frac{A_{V_{Th}}}{\sqrt{M \times W \times L}}$$

where $A_{V_{Th}}$ is a user-defined, technology dependant mismatch parameter. During the simulations performed on the CT-amplifier, a value of 15×10^{-9} Vm was used for $A_{V_{Th}}$, which was obtained from the 0.5-μm EKV model [85]. The shift in threshold voltage is incorporated in the model through the parameter 'delvto' [86]. Monte Carlo simulations were performed over confidence intervals of ±4σ so that more than 99.99% of all the samples fall within the confidence intervals. Figure 4.12 shows the result from Monte Carlo simulations performed on the post-layout netlist using the above parameters for 200 samples. The average of the DC PSRR using Monte Carlo simulations of 200 samples is approximately 63 dB, while the measurement results showed a DC PSRR of 60 dB. This indicates a good match between simulation and measurement results.

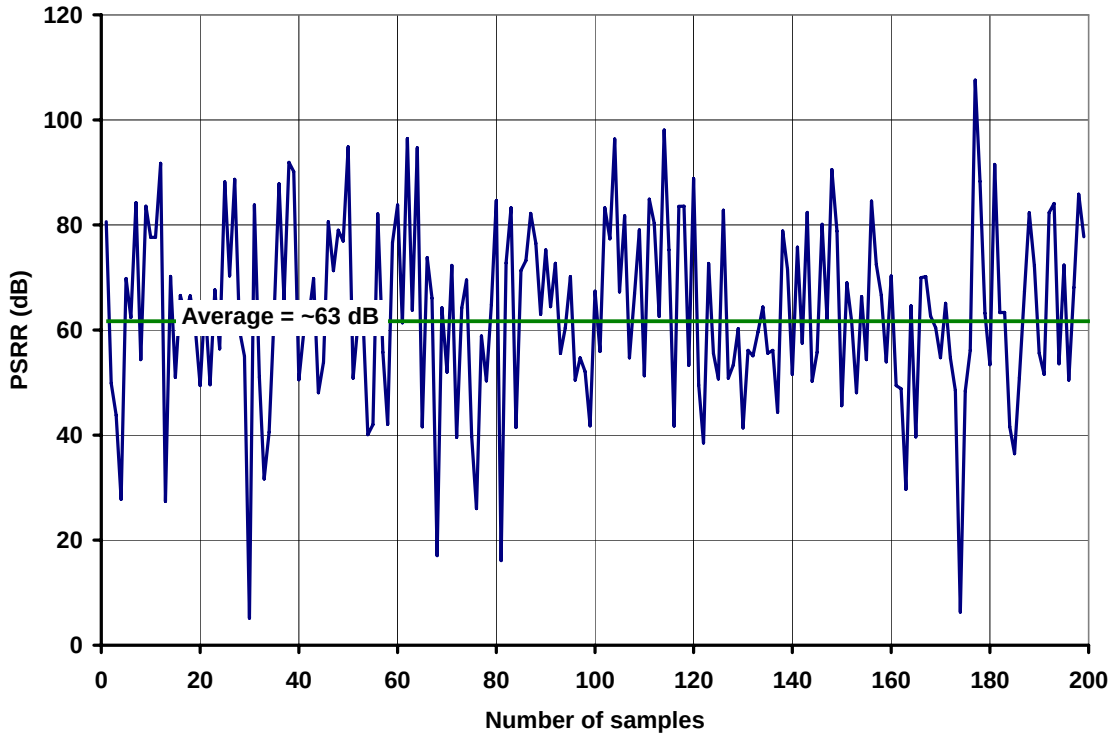

Figure 4.12. Monte Carlo simulation of the PSRR for 200 samples

4.2.3.6 Common-Mode Rejection Ratio (CMRR)

As the name suggests, CMRR can be understood as the ability of the amplifier to successfully reject signals common to both the input terminals. In a conventional amplifier, the tail current source has predominant impact on the CMRR. Since this CT-amplifier is developed on the floor-plan of a conventional folded-cascode amplifier, it is expected that the tail current of the input differential pair has similar dominant impact on the CMRR. The schematic for the setup used for measuring DC CMRR is shown in [84]. Figure 4.13 shows the measurement result of the DC CMRR for DUT #1. The average CMRR for the CT-amplifier over the input range from –1.5 V to 2.0 V is approximately 54 dB. Monte Carlo analysis was performed to estimate the CMRR with similar

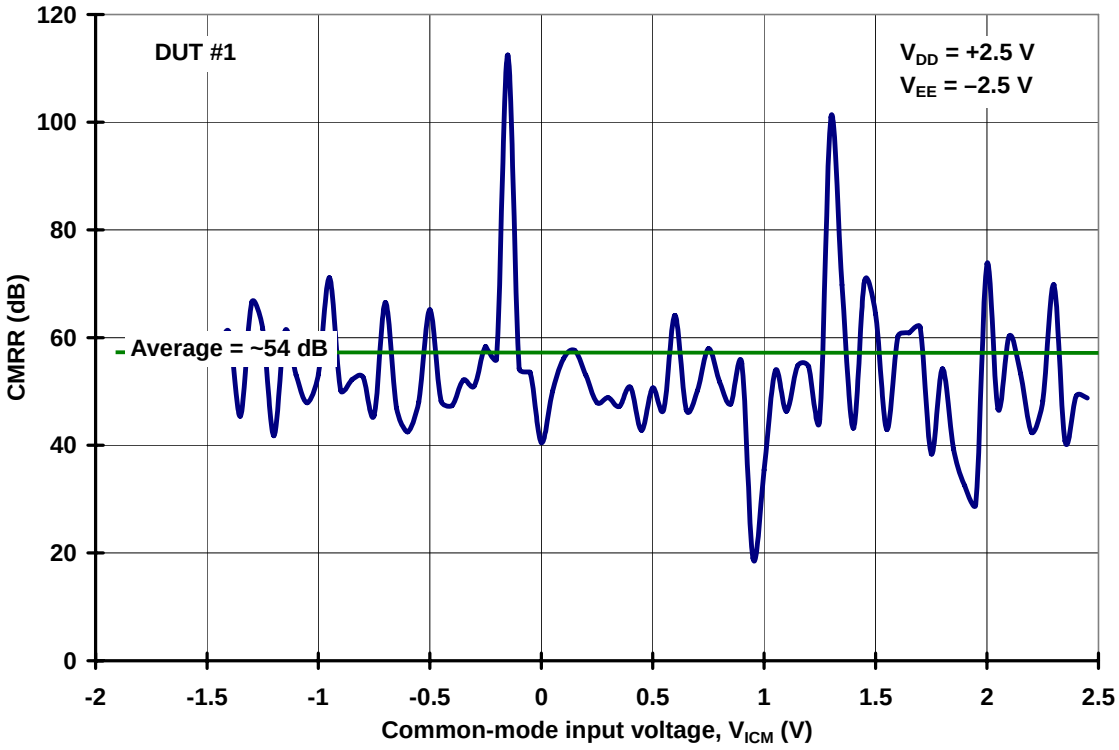

Figure 4.13. Measured CMRR vs. V_{ICM} for the CT-amplifier

simulation setup as that used during PSRR. These simulations indicate an average CMRR of approximately 69 dB. Figure 4.14 shows the simulation results from Monte Carlo analysis. The discrepancy between measured and simulated CMRR could be because the measured CMRR was an average of the CMRR over the ICMR, while the simulated CMRR was the average value recorded at mid-supply voltage over 200 samples during Monte Carlo simulations.

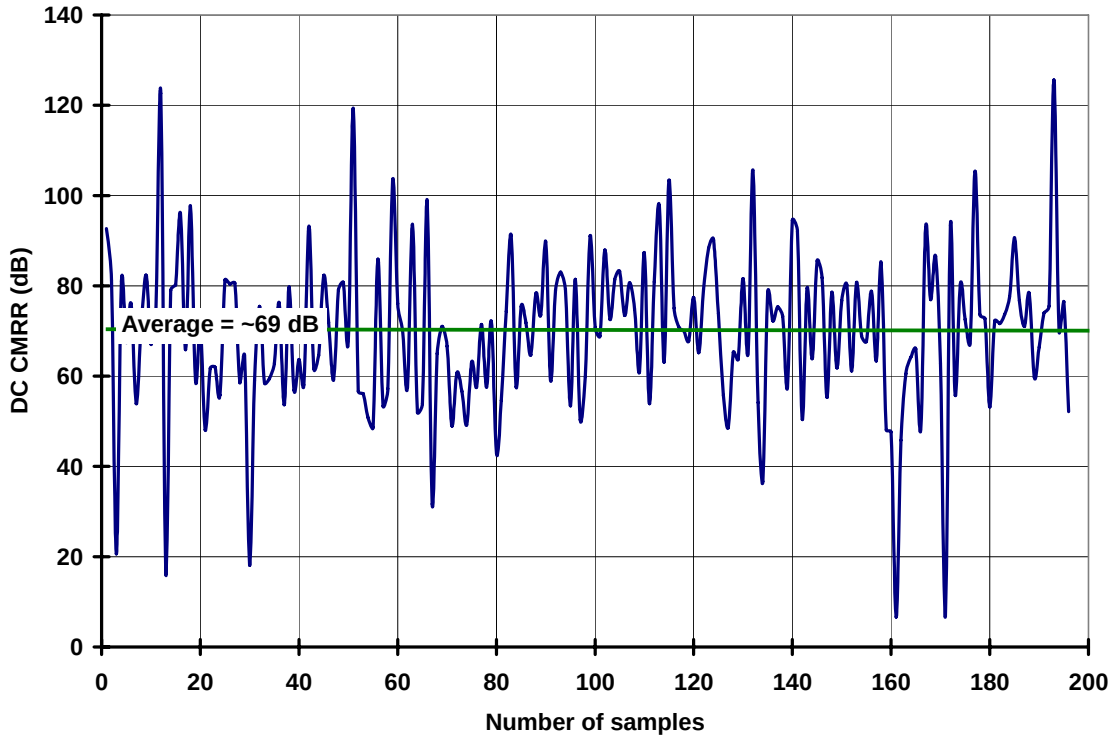

Figure 4.14. Monte Carlo analysis of the CMRR for 200 samples

4.2.3.7 Summary of the measurement results

The previous sections presented a detailed description of the measured results from the CT-amplifier. Table 4.5 summarizes these measurement results.

Reviewing the design goals discussed in Section 4.2:

- Develop an amplifier using the CT element that offers open-loop gain comparable to conventional multi-stage amplifiers
- Develop a compensation architecture for an all inverting gain stage based op amp
- Develop an amplifier that not only offers very high open-loop gain, but also offers other performance parameters comparable to conventional multi-stage amplifiers

Table 4.5. Summary of key measured parameters of the CT-amplifier (C_L = 18 pF)

Parameter	Measured Value
Power Supply	5.0 V
Supply Current	1.14 mA
ICMR	0.7 V - 4.8 V
Open-loop Gain	> 120 dB
Unity-Gain Bandwidth	> 12 MHz
Phase Margin (C_L = 18 pF)	~ 90°
Slew Rate (C_L = 18 pF)	> 10 V/μs
CMRR	> 50 dB
PSRR	> 60 dB
Area	0.25 mm^2

The CT-amplifier achieves a very high open-loop gain and phase margin, which are the primary goals of this work. In addition, the other key parameters such as UGBW, CMRR and PSRR are commensurate with other amplifiers. The design has clearly met the primary goals. Improving the CMRR, if needed for a specialized application, is discussed in Chapter 5.

4.3 Comparison of the CT-amplifier with other multi-stage amplifiers

This section presents a comparison between the performance characteristics of CT-amplifier developed in this research with previously reported multi-stage amplifiers. The parameters of interest include open-loop gain, unity-gain bandwidth, phase margin, slew-rate, load capacitance and power consumption. Additionally, a figure of merit (FOM) will be developed that normalizes these characteristics to facilitate the comparison and analysis with various amplifiers.

It could be inferred from the literature survey that small-signal parameters play a vital role in the development and comparison of FOMs for amplifiers. One such widely used FOM [36] is

$$FOM = \frac{GBW \times C_L}{Power}$$

Phase margin is one key parameter that is seemingly overlooked in the estimation of FOMs. Since higher gain-bandwidth product could be achieved with lower phase margin, the author believes that the small-signal FOM should also include the phase margin for proper comparison. Therefore, the small-signal efficiency FOM that will be used in this work will be defined as follows:

$$FOM_{CD} = \frac{GBW \times C_L \times PM}{Power}$$

Table 4.6 compares the FOM_{CD} for previously published high-gain amplifiers with the CT-based amplifier.

From the Table 4.6, it is clear that most of the amplifiers offer open-loop gains higher than 90 dB. Some of these amplifiers offer exceptionally high GBW, which under close observation can be found to be implemented in bipolar processes. Bipolar processes not only offer high unity-gain current frequency (f_T), but also offer higher g_m-efficiency than CMOS processes.

Table 4.6. Comparison of CT-amplifier with previously published high-gain amplifiers

Ref.	Author	# stages	Gain (dB)	GBW (MHz)	SR+ (V/µs)	Power (µW)	C_L (pF)	PM (°)	Tech. (µm)	FOM_{CD}	Comments
[77]	Bult	2	90	116	NA	52000	16	64	1.6	2.2	Uses gain-boost principle
[78]	Fonderio	3	117	3.4	1.1	5250	100	61	1.2	3.9	Bipolar with MPD stage
[48]	Eschauzier	3	100	60	20	76000	100	40	Bipolar	3.1	Bipolar process
[23]	Pernici	4	120	2	1.5	10000	250	80	1.5	4	Uses double Nested Miller compensation
[79]	Lahiji *	2	100	3.3	1	72000	20†	50	Bipolar	0.04	Bipolar process
[80]	de Langen	3	76	1000	360	86400	2	47	Bipolar	1.0	Bipolar process
[47]	Fan You	4	100	1	5	1400	20	58	2	0.8	Uses NGCC
[81]	Bouzerara	2	90	182	NA	7000	1	95	0.8	2.4	Uses active PFB with FF and FDCM techniques
[83]	Mita	4	110	1.2	NA	1380	5	90	NA	0.3	Uses Reverse-Nested Miller compensation
[82]	Palumbo	3	> 100	1.4	0.46	5000	100	91	0.8	2.5	Uses double pole-zero cancellation technique
	This work	**3**	**> 120**	**> 15**	**> 10**	**5650**	**18**	**~ 90**	**0.5**	**> 4.3**	**CT element based amplifier**

* - simulations only

† - assumed a capacitance based on the description in the paper

Though most of the amplifiers used for comparison use 3 or less stages, there are two amplifiers that even use 4 stages to achieve open-loop gain close to 120 dB. Most of the amplifiers use a variation of the Miller compensation architecture like nested-Miller compensation, reverse-nested Miller compensation, etc. Some of them even use positive feedback techniques for compensation, but all the amplifiers with 3 or more gain stages have gain inversions between alternate stages. Regarding UGBW, the CT-amplifier offers better bandwidth and PM when compared to most of the multi-stage amplifiers using CMOS processes. Since the CT-amplifier is targeted for use in sample and hold amplifiers, it is designed to drive small capacitive loads. SR parameters are not available for most of the amplifiers, but the CT-amplifier achieves a slew-rate higher than 10 V/μs driving a load capacitance of 18 pF.

The number of stages in a multi-stage amplifier plays a vital role in estimating the achievable bandwidth of the amplifier. This is because with the increase in the number of stages, there is an increasing possibility for the presence of multiple poles within the unity-gain bandwidth that need to be compensated to achieve stability. This not only reduces the usable bandwidth of the amplifier, but also increases the complexity of the compensation network. The following equation shows the loss in UGBW between amplifiers with multiple poles at the same frequency to other amplifiers with single-pole at the same frequency, assuming both the systems with similar open-loop gain:

$$\text{Bandwidth loss factor} = \frac{\text{Unity - gain bandwidth of an n - pole system}}{\text{Unity - gain bandwidth of a single pole system}}$$

$$= \left(|A_0|\right)^{\left\{\left(1/n\right)-1\right\}} \tag{34}$$

where A_0 indicates the dc open-loop gain of the system and 'n' indicates the number of poles. The complete derivation of this equation and a detailed analysis is shown in Appendix A. This derivation is used to analyze the reduction in achievable bandwidth by a multi-pole system, with all the poles located at the same frequency as the single-pole system. This derivation is important for this dissertation because in an ideal CT element (described in Section 3.1.2), the current through each of the differential pairs is the same, which will result in a multi-pole system with all the poles located at the same frequency. Because of this, the CT element based amplifier offers lower bandwidth compared to a similar single-pole system. The CT-amplifier implemented in this dissertation has multiple poles at different frequencies shown in Figure 4.5, which facilitates the improvement of achievable bandwidth of this system.

4.4 Tools used in this research

In accordance with the departmental requirements for a Ph.D document, the major tools used in this research will now be discussed. The design effort of this dissertation started with the intention to design a high gain, high bandwidth operational amplifier that can be used in the development of a fast settling sample and hold amplifier (SHA). This SHA was targeted for use in high resolution pipeline ADCs. Typically, one purpose of these SHAs is to amplify the input signals by an accurate factor of 2. The accuracy of the gain factor is limited by the open-loop gain of the amplifier [87]. The CT-based amplifier can be targeted to implement a highly accurate sample-hold amplifier. This was the original motivation for the development of the CT element. Later, a literature review was done to

understand and analyze the various previously published compensation topologies. The IEEE Xplore [65] search engine played a crucial role in performing this literature search. Since most of the research work on multi-stage amplifiers and their compensation topologies started from the late 1970's or early 1980's, and the electronic/online version of the IEEE Xplore archives the journals, transactions, letters and magazines with select content dating back to 1952, it is a reasonable tool to rely on for surveying the literature. The literature survey has given sufficient confidence that a multi-stage amplifier with all the gain stages offering inverting signal gains has not been previously done. The design process then demanded a novel compensation technique to achieve closed-loop stability. The development of the compensation technique involved simulations from Maple [66] and Matlab for optimizing and verifying the integrity of the complex mathematics, which were done by hand. Once the simulation results from Maple and Matlab were satisfactory, those parameters were realized into transistor-level parameters. Preliminary simulations were performed on the schematic netlist to validate the transformation from Matlab to transistor-level implementation. When the preliminary simulations were complete, the design was finalized and the circuit was entered as schematics into the Cadence schematic editor. Later the layout was done in a 0.5-µm bulk CMOS process using the Cadence Virtuoso layout editor. After the layout was complete, post layout extraction simulations from pad-to-pad (chip-level) were performed to verify the layout. The fabricated chips returned in August 2006. A custom designed PCB test-board was used during the characterization phase. During the measurement phase of this work, various instruments from Hewlett-Packard, Stanford Research Systems, Keithely and Agilent technologies were used. These instruments include the HP3589

(Spectrum/Network analyzer) and Stanford Research Systems SR770 (FFT Network analyzer) for the open-loop gain measurements, the Agilent 54622D (mixed-signal oscilloscope), Agilent E3631A (Triple output power supply), Agilent 34401A (6 ½ digit multimeter) and Agilent 33250A (80 MHz Function/Arbitrary waveform generator) during step response tests, PSRR, CMRR and offset measurements. Labview programs were used to automate the measurement procedure while conducting the experiments.

4.5 Conclusions

This chapter begins with a review of the earlier chapters followed by a discussion of the implementation and layout issues of the amplifier. The second section presents the design goals, test configuration and the PCB test board used during measurements. This includes a brief overview of the different setups for DC, AC and transient measurements. The measurement results were conducted on a sample of 4 chips for all the performance parameters, and a summary of the measured results was provided in Table 4.5. The measurement results showed a good match with the simulation results, indicating that the op amp has successfully met all the design goals. Later a figure of merit was developed and the performance of the CT-amplifier was compared with prior art amplifiers for analysis. Finally, the tools used to conduct the research were reviewed.

5. Conclusions and Future work

5.1 Anticipated original contributions of this research

The original contributions of this research are summarized as follows:

- an efficient compound transconductance element that facilitates very high gain multi-stage amplification,
- a frequency compensation topology for the compound transconductance element based amplifier,
- a power and area efficient forward gain path in a multi-stage amplifier,
- a unique frequency compensation scheme for an all inverting multi-stage operational amplifier,
- a compensation architecture that provides an all left-half-plane pole, zero transfer function in multi-stage amplifiers, and
- derivation of bandwidth loss in a system with multiple poles at the same frequency compared to that of a single-pole system.

5.2 Future research directions

This section suggests future directions in extending the concept on the CT-amplifier. Some of the improvements could be as follows:

- use complementary input pairs to provide rail-to-rail ICMR,
- develop a compatible class-AB output stage,

- implement a fully-differential CT-amplifier by analyzing various CMFB architectures,
- temperature characterization of this amplifier and analyze if this can be used over wide (beyond commercial) temperature range,
- analyze the improvement in the UGBW by reducing the available PM (currently the PM is approximately 90°) to around 55° or 60°, and
- minimize the sizes of the internal capacitors for improving the area efficiency.

Possible improvements at the system level could be as follows:

- applying this CT-amplifier architecture to the low-voltage design concept of body driving,
- use a fully-differential CT-amplifier in the implementation of switched capacitor applications such as sample-and-hold amplifiers,
- analyze the usage of the above S/H amplifier in ADCs, and
- extend this CT element in developing very high-speed (>1 GHz) analog circuits.

From the simulation results, it was observed that the compensation network (that includes g_{m4} and g_{m5} blocks) consumes almost 50% of the entire power consumed by the amplifier. This shows that the power efficiency of the amplifier can be improved by reducing the power consumption of the compensation network.

5.3 Conclusions

This research included the development of a novel compound transconductance element based amplifier that offers performance characteristics comparable to that of a multi-stage amplifier. The forward gain path of this amplifier is highly area and power efficient compared to its counter part multi-stage amplifiers.

A detailed literature review of multi-stage amplifiers shows that a multi-stage amplifier composed of all inverting gain stages has not yet been published. Therefore none of the previously published compensation topologies could be applicable for frequency compensation of this new amplifier. A novel compensation topology was developed and implemented, which is one of the unique contributions of this research. This includes the complete mathematical analysis and Matlab simulations of a 4^{th}-order transfer function. This topology not only offers an all left-half-plane poles and zeros approach, which is extremely helpful for stability optimization, but also provides the opportunity to simplify the complex transfer function into a single-pole system. The high phase margin from the compound transconductance element based amplifier can be attributed to the novel compensation topology developed as part of the stability optimization.

References

[1] W. S. Percival, “Thermionic valve circuits,” British Patent 460 562, Jan. 25, 1937.

[2] http://www.eas.caltech.edu/engenious/win03/hajimiri.pdf

[3] Adel S. Sedra and Kenneth C. Smith, *Microelectronic Circuits*, New York: Oxford University Press, 1982.

[4] B. K. Ahuja, “An improved frequency compensation technique for CMOS operational amplifiers,” *IEEE Journal of Solid-State Circuits*, vol. Sc-18, No.6, Dec. 1983.

[5] J. E. Solomon, “The monolithic opamp: A Tutorial Study,” *IEEE Journal of Solid-State Circuits*, vol.sc-9, No.6, Dec. 1974.

[6] M. Banu, J. M. Khoury, and Y. Tsividis, “Fully Differential Operational Amplifiers with Accurate Output Balancing,” *IEEE Journal of Solid-State Circuits*, vol.23, No. 6, pp.1410-1414, Dec. 1988.

[7] E. Sackinger and W. Guggenbuhl, “A High-Swing, High-Impedance MOS Cascode Circuit,” *IEEE Journal of Solid-State Circuits*, vol. 25, No.1, Feb. 1990.

[8] M. A. Copeland and J. M. Rabaey, “Dynamic amplifier for MOS technology,” *IEEE Electron Letters*, vol. 15, pp. 301-302, May, 1979.

[9] B. J. Hosticka, “Dynamic CMOS Amplifiers,” *IEEE Journal of Solid-State Circuits*, vol. sc-15, No.5, Oct. 1980.

[10] B. J. Hosticka, “Performance of integrated dynamic MOS amplifiers,” *Electron Letters*, pp. 298-300, Apr. 1981.

[11] F. Wang and R. Harjani, "Dynamic Amplifiers: Settling, Slewing and Power Issues," *IEEE International Symposium on Circuits and Systems*, pg.319-322, vol.1, Apr.13-May 3, 1995.

[12] D. Senderowicz, J. H. H. Dreyer, C. F. Rahim, and C. A. Laber, "A Family of Differential NMOS Analog Circuits for a PCM Codec Filter Chip," *IEEE Journal of Solid-State Circuits*, vol. sc-17, No.6, Dec. 1982.

[13] D. Allstot, "A Precision variable supply CMOS comparator," *IEEE Journal of Solid-State Circuits*, SC-17, No.6, pp. 1080-1087, Dec, 1982.

[14] B. Nauta and E. Seevinck, "Linear CMOS transconductance element for VHF filters," *Electron Letters*, pp.448-450, 1989.

[15] B. Nauta, "A CMOS Transconductance-C filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, vol. 27, No.2, Feb. 1992.

[16] S. L. Wong and C. A. T. Salama, "Voltage gain enhancement by conductance cancellation in CMOS opamps," *IEEE International Symposium on Circuits and Systems*, pp1207-1210, 1984.

[17] J. Yan and R. L. Geiger, "A high gain CMOS operational amplifier with negative conductance gain enhancement," *Proceedings of the IEEE 2002 Custom Integrated Circuits Conference*, pp.337-340, 2002.

[18] C.A. Laber and P.R. Gray, "A Positive Feedback Transconductance Amplifier with Applications to High-Frequency, High-Q CMOS Switched-Capacitor Filters," *IEEE Journal of Solid-State Circuits*, vol. 23, No.6, Dec. 1988.

[19] M. A. Mezyad and R. L. Geiger, "All digital transistors high gain operational amplifier using positive feedback technique," *IEEE International Symposium on Circuits and Systems*, pp.I-701 – I-704, May 2002.

[20] B. W. Lee and J. B. Sheu, "A High-speed CMOS Amplifier with Dynamic Frequency Compensation," *Proceedings of the IEEE 1990 Custom Integrated Circuits Conference*, pg.8.4/1-8.4/4, May, 1990.

[21] R. Eshcauzier and J. Huijsing, "An operational amplifier with multi-path Miller zero cancellation for RHP zero removal," *Proc. ESSCIRC*, pp. 122-125, 1993.

[22] R. Eschauzier, R. Hogervorst, and J. Huijsing, "A programmable 1.5V class-AB operational amplifier with hybrid nested Miller compensation for 120 dB gain and 6MHz UGF," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1497-1504, Dec. 1994.

[23] S. Pernici, G. Nicollini, and R. Castello, "A CMOS low-distortion fully differential power amplifier with double nested Miller compensation," *IEEE J. Solid-State Circuits*, vol. 28, pp. 758-763, July 1993.

[24] P. R. Gray and R. G. Meyer, "MOS Operational Amplifier Design–A Tutorial Overview," *IEEE Journal of Solid-State Circuits*, vol.sc-17, No.6, Dec. 1982.

[25] E. M. Cherry and D. E. Hooper, *Amplifying Devices and Low-Pass Amplifier Design*, New York: Wiley, 1968.

[26] K. Wing-Hung, D. Lawrence, and L. Steve, "Re-examination of pole splitting of a generic single stage amplifier," *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, vol.44, no.1, Jan 1997.

[27] K. L. Leung and P. K. T. Mok, "Analysis of multistage amplifier frequency compensation," *IEEE Trans. On Circuits and Systems-I*, vol. 48, no. 9, Sep. 2001.

[28] K. L. Leung, P. K. T. Mok., W. H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping factor control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, Feb. 2000.

[29] X. Peng and Sansen. W., "AC Boosting compensation scheme for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, Nov 2004.

[30] B.K. Thandri and J. Silva-Martinez, "A robust feed-forward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, Feb. 2003.

[31] X. Fan, C. Mishra, and E. Sanchez-Sinencio, "Single Miller capacitor Frequency compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, no.3, Mar 2005.

[32] Y. B. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits,* vol. sc-9, no.6, Dec. 1974.

[33] K. L. Leung, P. K. T. Mok, K. Wing-Hung, and K. O. J. Sin, "Analysis on an alternative structure of damping-factor-control frequency compensation," *IEEE International Symposium on Circuits and Systems*, May28-31, Geneva, Switzerland, 2000.

[34] H. Lee and P. K. T. Mok, "Active-Feedback Frequency Compensation for low-power multi-stage amplifiers," *IEEE Custom Integrated Circuits Conference*, pg.325-328, 2002.

[35] H. Lee, and P. K. T. Mok, "Advances in Active-Feedback Frequency Compensation with power optimization and transient improvement," *IEEE Transactions on Circuits and Systems-I*, vol.51, no.9, Sept. 2004.

[36] H. Lee and P. K. T. Mok, "A dual-path bandwidth extension amplifier topology with Dual-Loop Parallel Compensation," *IEEE Journal of Solid-State Circuits*, vol.38, no.10, Oct. 2003.

[37] J. Ramos and M. S. J. Steyaert, "Positive Feedback Frequency Compensation for low-voltage low-power three-stage amplifier," *IEEE Transactions on Circuits and Systems-I*, vol.51, no.10, Oct. 2004.

[38] X. Peng and W. Sansen, "Transconductance with Capacitances Feedback Compensation for multistage amplifiers," *IEEE Journal of Solid-Stage Circuits*, vol.40, no.7, July 2005.

[39] H. T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation," *IEEE Journal of Solid-Stage Circuits*, vol.34, no.3, Mar.1999.

[40] K. N. Leung, P. K. T. Mok, and W. Ki, "Right-half place zero removal technique for low-voltage low-power nested Miller compensation CMOS amplifier," *IEEE International Conference on Electronics, Circuits and Systems*, vol.2, Sept. 1999.

[41] K. N. Leung and P. K. T. Mok, "Nested Miller compensation in low-power CMOS design," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol.48, no.4, Apr.2001.

[42] H. Yang and D. J. Allstot, "Considerations for fast settling operational amplifiers," *IEEE Transactions on Circuits and Systems*, vol.37, no.3, Mar. 1990.

[43] W. H. Ki, L. Der, and S. Lam, "Re-examination of pole splitting of a generic single stage amplifier," *IEEE Transactions on Circuits and Systems I*, vol.44, pp.70-74, Jan. 1997.

[44] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd edition, New York: Wiley, 1984.

[45] R. G. H. Eschauzier and J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*, Boston, MA: Kluwer, 1995.

[46] F. You, S. H. K. Embabi, and E. Sanchez-Sinencio, "A multistage amplifier topology with nested Gm-C compensation for low-voltage application," *IEEE International Solid-State Circuits Conference*, pg.348-349, Feb. 1997.

[47] F. You, S. H. K. Embabi, and E. Sanchez-Sinencio, "Multistage amplifier topologies with nested Gm-C compensation," *IEEE Journal of Solid-State Circuits*, vol.32, pp.2000-2011, Dec. 1997.

[48] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dB Operational Amplifier with multipath nested Miller compensation structure," *IEEE Journal of Solid-State Circuits*, vol.27, no.12, Dec. 1992.

[49] J. H. Huijsing, R. Hogervorst, and K. J. de Landen, "Low-power low-voltage VLSI operational amplifier cells," *IEEE Transactions on Circuits and Systems-I*, vol.42, pp. 841-852, Nov. 1995.

[50] P. R. Gray and R. G. Meyer, "MOS Operational Amplifier Design – A Tutorial Overview," *IEEE Journal of Solid-State Circuits*, vol. sc-17, no.6, Dec. 1982.

[51] R. J. Reay and T. A. G. Kovacs, "An unconditionally stable two-stage CMOS amplifier," *IEEE Journal of Solid-State Circuits*, vol.30, no.5, May 1995.

[52] B. A. Minch, "A low-voltage MOS cascode bias circuit for all current levels," *Proceedings of the 2002 Integrated Circuits and Systems Symposium*, vol. III, pp. 619-622, 2002.

[53] http://public.itrs.net/

[54] B. A. Minch, "A low-voltage MOS cascode current mirror for all current levels," *The 2002 45th Midwest Symposium on Circuits and Systems*, Vol. 2, 4-7 Aug 2002.

[55] A. L. Coban and P. E. Allen, "A 1.75 V rail-to-rail CMOS op amp," *IEEE International Symposium on Circuits and Systems*, vol.5, pp.497-500, 1994.

[56] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 9th reprint, New Delhi: Tata McGraw-Hill Publishing Company Limited, 2002.

[57] B. J. Hosticka, "Improvement of the gain of MOS Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. sc-14, no.6, Dec. 1979.

[58] M. J. M. Pelgrom, H. P. Tuinhout, and M. Vertregt, "Transistor matching in analog CMOS applications," *International Electron Devices Meeting*, pg. 915-918, Dec. 1998.

[59] S. J. Lovett, M. Welten, A. Mathewson, and B. Mason, "Optimizing MOS transistor mismatch," *IEEE Journal of Solid-State Circuits*, vol.33, no.1, Jan. 1998.

[60] M. J. M. Pelgrom, A. C. J. Duimaijer, and A P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, vol.24, no.5, Oct. 1989.

[61] A. A. Abidi, "On the operation of cascode gain stages," *IEEE Journal of Solid-State Circuits*, vol.23, no.6, Dec. 1998.

[62] J. R. Baker, W. L. Harry, and D. E. Boyce, *CMOS circuit design, layout and simulation*, 1st Edition, New York: Wiley-Interscience, 1998.

[63] http://www.mathworks.com

[64] http://www.mentor.com/products/ic_nanometer_design/simulation/eldo/index.cfm

[65] http://ieeexplore.ieee.org

[66] http://www.maplesoft.com

[67] B. J. Blalock, *A 1–V CMOS Wide Dynamic Range Operational Amplifier*, Ph.D Dissertation, School of ECE, Georgia Institute of Technology, Atlanta, GA, 1996.

[68] P. E. Allen, B. J. Blalock, and G.A Rincon, " A 1-V CMOS op-amp using bulk-driven MOSFETs," *Proceeding of the 1995 International Solid State Circuits Conference*, pp. 192-193, San Francisco, CA, Feb. 1995.

[69] S. C. Terry, B. J. Blalock, L. K. Yong, B. M. Dufrene, and M. M. Mojarradi, "Complementary body driving–A low-voltage analog circuit technique for SOI," *Proceedings of the 2002 International SOI Conference*, pp. 80-82, Williamsburg, VA, 2002.

[70] A. Wang, A. Chandrakasan, and S. Kosonocky, "Optimal supply and threshold scaling for subthreshold CMOS circuits," *Proceedings. IEEE Computer Society Annual Symposium on VLSI*, Apr. 2002.

[71] B. Calhoun and A. Chandrakasan, "Characterizing and modeling minimum energy operation for subthreshold circuits," *Proc. ISLPED*, pp. 90-95, 2004.

[72] S. Francisco and J. L. Huertas, "Low-voltage CMOS subthreshold log-domain filtering," *IEEE Transactions on Circuits and Systems-II*, vol. 52, no. 10, Oct. 2005.

[73] A. Pesavento and C. Koch, "A wide linear range four quadrant multiplier in subthreshold CMOS," *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 240-243, 1999.

[74] B. K. Ahuja, V. Hoa, C. A. Laber, and W. H. Owen, "A very high precision 500-nA CMOS floating-gate analog voltage reference," *IEEE JSSC*, vol. 40, pp. 2364-2372, Dec. 2005.

[75] C. S. A. Durisety, B. J. Blalock, and B. M. Dufrene, "Analysis and characterization of single-poly floating gate device on 0.35μm partially depleted SOI," *48th Midwest Symposium on Circuits and Systems*, pp. 91-94, Aug. 2005.

[76] C. S. A. Durisety, *Analysis and Characterization of Single-Poly Floating Gate Devices in 0.3535μm PDSOI process*, Master's Thesis, University of Tennessee, Knoxville, TN, Dec. 2002.

[77] K. Bult and G. J. G. M Geelen, " A fast-settling CMOS op amp for SC circuits with 90-dB dc gain," *IEEE JSSC*, vol. 25, pp. 1379-1384, Dec. 1990.

[78] J. Fonderie and J. H. Huijsing, " Operational amplifier with 1-V rail-to-rail multipath-driven output stage," *IEEE JSSC*, vol. 26, pp. 1817-1824, Dec. 1991.

[79] G. R. Lahiji, O. Oleyaie and A. Abrishamifar, "New operational amplifier using a positive feedback," IEEE Transactions on circuits and systems-II: Analog and digital signal processing, vol. 44, no. 5, May 1997.

[80] K. Langen, R. G. H. Eschauzier, G. J. A. Dijk and J. H. Huijsing, " A 1-GHz bipolar class-AB operational amplifier with multipath nested miller compensation for 76-dB gain," *IEEE JSSC*, vol. 32, pp. 488-498, Apr. 1997.

[81] L. Bouzerara, M. T. Belaroussi and B. Amirouche, " Low-voltage, low-power and high gain CMOS OTA using active positive feedback with feedforward and FDCM techniques," Proc. 23rd International conference on Microelectronics (MIEL 2002), vol. 2, NIS, Yugoslavia, May 2002.

[82] G. Palumbo and S. Pennisi, " Design methodology and advances in Nested-Miller compensation," *IEEE Trans. on Circuits and Systems-I: Fundamental theory and applications*, vol. 49, no. 7, July 2002.

[83] R. Mita, G. Palumbo and S. Pennisi, "Design guidelines for reversed Nested Miller compensation in three-stage amplifiers," IEEE *Trans. on Circuits and Systems-II: Analog and Digital Signal Processing,* vol. 50, no. 5, May 2003.

[84] S. C. Terry, *Low-voltage analog circuit design using the adaptively biased body-driven circuit technique,* Ph.D Dissertation, Department of ECE, University of Tennessee, Knoxville, TN, 2005.

[85] The EPFL-EKV Model Website, [available online: http://legwww.epfl.ch/ekv/].

[86] Q. Zhang, J. R. McMacken, J. Thomson, and P. Layman, "SPICE modeling and quick estimation of MOSFET mismatch based on BSIM3 model and parametric tests," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 10, Oct. 2001.

[87] A. M. Abo, Design for reliability of low-voltage, switched-capacitor circuits, Ph.D Dissertation, Engineering-Electrical Engineering and Computer Sciences, California Institute of Technology, Pasadena, CA, 1992.

[88] E. J. Kennedy, *Operational amplifier circuits: Theory and applications,* New York: Oxford University Press, 1988.

[89] Personal correspondence with Tony G. Antonacci and Robert L. Greenwell

Appendix A

A. Small-signal Derivations

This appendix includes the following derivations:

- Complete transfer function of the CT-amplifier with the compensation network, and
- Loss of bandwidth between a single-pole system and a multiple-pole system with all poles at the same frequency

A.1 Transfer function for the CT-amplifier

The small-signal schematic of the CT-amplifier is shown in the Figure 3.9.

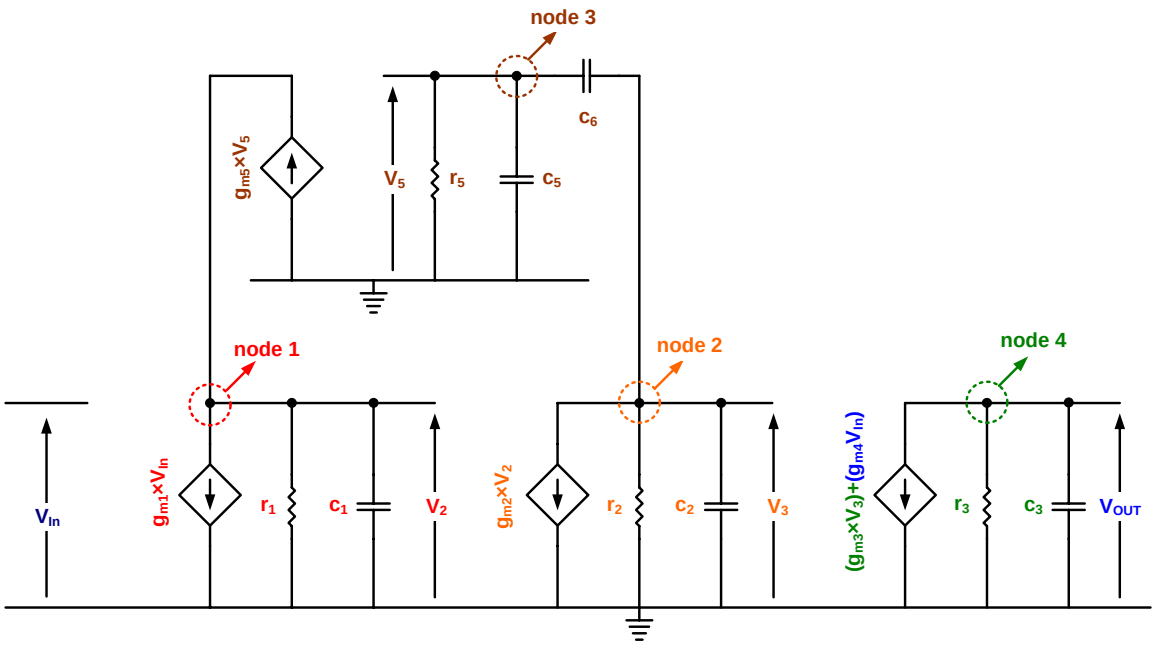

Figure A.1. Small-signal schematic of the CT-amplifier

The complete derivation for the transfer function is derived as follows:

Applying KCL at node 1, node 2, node 3 and node 4, the following equations are derived respectively.

$$(-gm_1V_{IN})+(gm_5V_5)=V_2\left(\frac{1}{r_1}+sC_1\right)$$

$$(-gm_2V_2)=V_3\left(\frac{1}{r_2}+sC_2\right)+(V_3-V_5)sC_6$$

$$(V_3-V_5)sC_6=V_5\left(\frac{1}{r_5}+sC_5\right)$$

$$(-gm_3V_3-gm_4V_{IN})=V_{OUT}\left(\frac{1}{r_3}+sC_3\right)$$

Simplifying the equation from node 3:

$$(V_3-V_5)sC_6=V_5\left(\frac{1}{r_5}+sC_5\right)$$

$$(V_3-V_5)sr_5C_6=V_5(1+sr_5C_5)$$

$$V_3(sr_5C_6)=V5(1+sr_5C_5+sr_5C_6)$$

$$V_5=V_3\left(\frac{sr_5C_6}{1+sr_5C_5+sr_5C_6}\right)$$

Simplifying the equation from node 2, using the above relation:

$$(-gm_2V_2)=V_3\left(\frac{1}{r_2}+sC_2\right)+(V_3-V_5)sC_6$$

$$(-gm_2r_2)V_2=V_3(1+sr_2C_2)+(V_3-V_5)sr_2C_6$$

$$=V_3(1+sr_2C_2+sr_2C_6)+V_5(sr_2C_6)$$

$$=V_3(1+sr_2C_2+sr_2C_6)-V_3\left[\frac{(sr_2C_6)(sr_5C_6)}{(1+sr_5c_5+sr_5c_6)}\right]$$

$$=V_3\left[\frac{(1+sr_2C_2+sr_2C_6)(1+sr_5C_5+sr_5C_6)-(sr_2C_6)(sr_5C_6)}{(1+sr_5C_5+sr_5C_6)}\right]$$

$$= V_3 \frac{1 + s\left(r_2C_2 + r_2C_6 + r_5C_5 + r_5C_6\right) + s^2\left(r_2C_2r_5C_5 + r_2C_2r_5C_6 + r_5C_5r_2C_6\right)}{\left(1 + sr_5C_5 + sr_5C_6\right)}$$

$$-gm_2r_2V_2 = V_3 \frac{1 + s\left(r_2C_2 + r_2C_6 + r_5C_5 + r_5C_6\right) + s^2\left(r_2C_2r_5C_5 + r_2C_2r_5C_6 + r_5C_5r_2C_6\right)}{\left(1 + sr_5C_5 + sr_5C_6\right)}$$

$$-A_2V_2 = V_3 \frac{1 + s\left(r_2C_2 + r_2C_6 + r_5C_5 + r_5C_6\right) + s^2\left(r_2C_2r_5C_5 + r_2C_2r_5C_6 + r_5C_5r_2C_6\right)}{\left(1 + sr_5C_5 + sr_5C_6\right)}$$

Let $X = 1 + s\left(r_2C_2 + r_2C_6 + r_5C_5 + r_5C_6\right) + s^2\left(r_2C_2r_5C_5 + r_2C_2r_5C_6 + r_5C_5r_2C_6\right)$. Then

$$-A_2V_2 = V_3 \frac{X}{\left(1 + sr_5C_5 + sr_5C_6\right)}$$

Substituting the equations from node 2 and node 3 into the equation from node 1 followed by simplification provides

$$\left(-gm_1V_{IN}\right) + \left(gm_5V_5\right) = V_2\left(\frac{1}{r1} + sC1\right)$$

$$\left(-gm_1r_1V_{IN}\right) + \left(gm_5r_1V_5\right) = V_2\left(1 + sr_1C_1\right)$$

$$\left(-A_1V_{IN}\right) = -\left(A_5V_5\right) + V_2\left(1 + sr_1C_1\right)$$

$$\Rightarrow -\left(A_5V_3\right)\left(\frac{sr_5C_6}{1 + sr_5C_5 + sr_5C_6}\right) - V_3 \frac{\left\{\left(1 + sr_1C_1\right)X\right\}}{A_2\left(1 + sr_5C_5 + sr_5C_6\right)}$$

$$\Rightarrow -V_3 \frac{A_2A_5\left(sr_5C_6\right) + \left\{\left(1 + sr_1C_1\right)X\right\}}{A_2\left(1 + sr_5C_5 + sr_5C_6\right)}$$

$$\frac{\mathrm{V}_3}{\mathrm{V}_{\mathrm{IN}}} = \frac{A_1A_2\left(1 + sr_5C_5 + sr_5C_6\right)}{A_2A_5\left(sr_5C_6\right) + \left\{\left(1 + sr_1C_1\right)X\right\}}$$

Substituting the above equation in the equation derived from node 4, and simplifying

$$-gm_3V_3 - gm_4V_{IN} = V_{OUT}\left(\frac{1}{r_3} + sC_3\right)$$

$$-gm_3r_3V_3 - gm_4r_3V_{IN} = V_{OUT}\left(1 + sr_3C_3\right)$$

$$-A_3V_3 - A_4V_{IN} = V_{OUT}\left(1 + sr_3C_3\right)$$

$$-V_{IN}\left[\frac{A_1A_2A_3\left(1+sr_5C_5+sr_5C_6\right)}{A_2A_5\left(sr_5C_6\right)+\left\{\left(1+sr_1C_1\right)X\right\}}+A_4\right]=V_{OUT}\left(1+sr_3C_3\right)$$

Let $Y=A_2A_5\left(sr_5C_6\right)+\left\{\left(1+sr_1C_1\right)X\right\}$. Then

$$-V_{IN}\left[\frac{\left\{A_1A_2A_3\left(1+sr_5C_5+sr_5C_6\right)\right\}+\left(A_4Y\right)}{Y}\right]=V_{OUT}\left(1+sr_3C_3\right)$$

$$\frac{V_{OUT}}{V_{IN}}=-A_1A_2A_3\left[\frac{1+sr_5C_5+sr_5C_6+\left(\frac{A_4Y}{A_1A_2A_3}\right)}{Y\left(1+sr_3C_3\right)}\right]$$

$$\frac{V_{OUT}}{V_{IN}}=-A_1A_2A_3\left[\frac{C_{N0}+sC_{N1}+s^2C_{N2}+s^3C_{N3}}{\left(1+sr_3C_3\right)\left(1+sC_{D1}+s^2C_{D2}+s^3C_{D3}\right)}\right]$$

where

$$C_{N0}=1+\frac{g_{m4}}{g_{m1}g_{m2}g_{m3}r_1r_2},$$

$$C_{N1}=\frac{C_6}{g_{m5}}+\frac{C_5}{g_{m5}}+\left\{\left(\frac{g_{m4}}{g_{m1}g_{m2}g_{m3}r_1r_2}\right)\left(r_1C_1+r_2C_2+r_2C_6+\frac{C_5}{g_{m5}}+\frac{C_6}{g_{m5}}+g_{m2}r_1r_2C_6\right)\right\},$$

$$C_{N2}=\left(\frac{g_{m4}}{g_{m1}g_{m2}g_{m3}r_1r_2}\right)\left(r_1C_1r_2C_2+r_1C_1r_2C_6+\frac{r_1C_1C_5}{g_{m5}}+\frac{r_1C_1C_6}{g_{m5}}+\frac{r_2C_2C_5}{g_{m5}}+\frac{r_2C_2C_6}{g_{m5}}+\frac{r_2C_5C_6}{g_{m5}}\right),$$

$$C_{N3}=\left(\frac{g_{m4}}{g_{m1}g_{m2}g_{m3}r_1r_2}\right)\left(\frac{r_1C_1r_2C_2C_5}{g_{m5}}+\frac{r_1C_1r_2C_2C_6}{g_{m5}}+\frac{r_1C_1r_2C_5C_6}{g_{m5}}\right),$$

$$C_{D1}=r_1C_1+r_2C_2+r_2C_6+\frac{C_5}{g_{m5}}+\frac{C_6}{g_{m5}}+g_{m2}r_1r_2C_6,$$

$$C_{D2}=r_1C_1r_2C_2+r_1C_1r_2C_6+\frac{r_1C_1C_5}{g_{m5}}+\frac{r_1C_1C_6}{g_{m5}}+\frac{r_2C_2C_5}{g_{m5}}+\frac{r_2C_2C_6}{g_{m5}}+\frac{r_2C_5C_6}{g_{m5}},\text{ and}$$

$$C_{D3}=\frac{r_1C_1r_2C_2C_5}{g_{m5}}+\frac{r_1C_1r_2C_2C_6}{g_{m5}}+\frac{r_1C_1r_2C_5C_6}{g_{m5}}.$$

A.2 Loss of bandwidth comparison between single and multi-pole systems

This section shows the derivation of the loss of bandwidth between a single-pole system to a multi-pole system when all the poles in the multi-pole system are at the same frequency as that of the single-pole system.

The transfer function for a single-pole system is given by $A(s) = \frac{\mathrm{A}_0}{1 + j\frac{f}{f_0}}$, where A_0 is the open-loop gain and f_0 is the frequency at which the gain is –3dB below the dc value. The unity-gain bandwidth (UGBW) can be understood as the frequency at which the open-loop gain of the system is unity.

$$|A(s)| = 1 \Rightarrow \left| \frac{\mathrm{A}_0}{1 + j\frac{f}{f_0}} \right| = 1 \Rightarrow \frac{|A_0|}{\left|1 + j\frac{f}{f_0}\right|} = 1;$$

$$\Rightarrow |A_0| = \left|1 + j\frac{f}{f_0}\right| \Rightarrow \sqrt{(1)^2 + \left(\frac{f}{f_0}\right)^2}$$

Squaring the equation on both the sides,

$$(|A_0|)^2 = (1)^2 + \left(\frac{f}{f_0}\right)^2$$

$$(|A_0|)^2 - 1 = \left(\frac{f}{f_0}\right)^2 \Rightarrow \frac{f}{f_0} = \sqrt{(|A_0|)^2 - 1}$$

$$f = f_0 \times \sqrt{(|A_0|)^2 - 1} \cong f_0 \times A_0$$

Thus it can be shown that the UGBW for a single-pole system is approximately equal to $f_0 \times A_0$.

The following derivation provides the UGBW for an *n*-pole system, where all the *n* poles are located at the same frequency, f_0.

A generalized transfer function for an *n*-pole system with all the *n*-poles at the same frequency, f_0, is given by

$$A(s) = \frac{A_0}{\left(1 + j\frac{f}{f_0}\right)^n}$$

Similar to the derivation for a single-pole system, the UGBW is the frequency at which $|A(s)| = 1$.

$$|A(s)| = 1 \Rightarrow |A_0| = \left|\left(1 + j\frac{f}{f_0}\right)^n\right|$$

It is known that $\left|(a + jb)^n\right| = \left(|a + jb|\right)^n$

$$|A_0| = \left|\left(1 + j\frac{f}{f_0}\right)^n\right| \Rightarrow \left|\left(1 + j\frac{f}{f_0}\right)\right|^n$$

$$\Rightarrow \left(|A_0|\right)^{1/n} = \left|\left(1 + j\frac{f}{f_0}\right)\right| \Rightarrow \sqrt{(1)^2 + \left(\frac{f}{f_0}\right)^2}$$

$$\Rightarrow \sqrt[n]{\left(|A_0|\right)^2} = (1)^2 + \left(\frac{f}{f_0}\right)^2$$

$$\Rightarrow \left(\frac{f}{f_0}\right)^2 = \sqrt[n]{\left(|A_0|\right)^2} - 1$$

$$\Rightarrow \frac{f}{f_0} = \sqrt{\sqrt[n]{\left(|A_0|\right)^2} - 1} = \sqrt[n]{|A_0|}, \; if \; \sqrt[n]{\left(|A_0|\right)^2} >> 1$$

$$\Rightarrow \frac{f}{f_0} = \sqrt[n]{|A_0|} \Rightarrow f = f_0 \times \sqrt[n]{|A_0|}$$

$$\Rightarrow f = f_0 \times \left(|A_0|\right)^{1/n}$$

From the above derivation, the bandwidth of an n-pole system with all the n poles at the same frequency is given by the *n*-th root of the open-loop gain multiplied by the –3dB frequency.

The bandwidth loss factor, i.e. loss in bandwidth due to the presence of multiple poles at the same frequency is given by

$$\text{Bandwidth loss factor} = \frac{\text{Bandwidth of an n - pole system}}{\text{Bandwidth of a single pole system}}$$

$$= \frac{f_0 \times \left(|A_0|\right)^{1/n}}{f_0 \times \left(|A_0|\right)}$$

$$= \left(|A_0|\right)^{\{(1/n)-1\}}$$

Assume an open-loop gain of 10^6 (i.e., 120 dB) and a –3 dB frequency of 100 Hz. Using the above derived formula, the UGBW for a single-pole system could be calculated as follows:

Using $A_0 = 10^6$, $f_0 = 100$ Hz and in a single-pole system, $n = 1$,

The unity-gain bandwidth for a single-pole system, $f_0|_1 = f_0 \times \left(|A_0|\right)^{1/n}$

$$= 100 \times \left(|10^6|\right)^{1/1}$$

$$= 100 \text{ MHz}$$

For a two-pole system (n = 2) with same open-loop gain and assuming both the poles are present at 100 Hz, the unity-gain bandwidth can be calculated as follows:

The unity-gain bandwidth for a two-pole system, $f_0|_2 = f_0 \times \left(|A_0|\right)^{1/n}$

$$= 100 \times \left(|10^6|\right)^{1/2} = 100 \times \sqrt{10^6}$$

$$= 100 \text{ kHz}$$

Similarly, for a three-pole system (n = 3) with the same parametric values as above, the unity-gain bandwidth is calculated as follows:

The unity-gain bandwidth for this three-pole system, $f_0|_3 = f_0 \times \left(|A_0|\right)^{1/n}$

$$= 100 \times \left(|10^6|\right)^{1/3} = 100 \times \sqrt[3]{10^6}$$

$$= 10 \text{ kHz}$$

The following plot shows the frequency response for all three systems and verifies the above derivation.

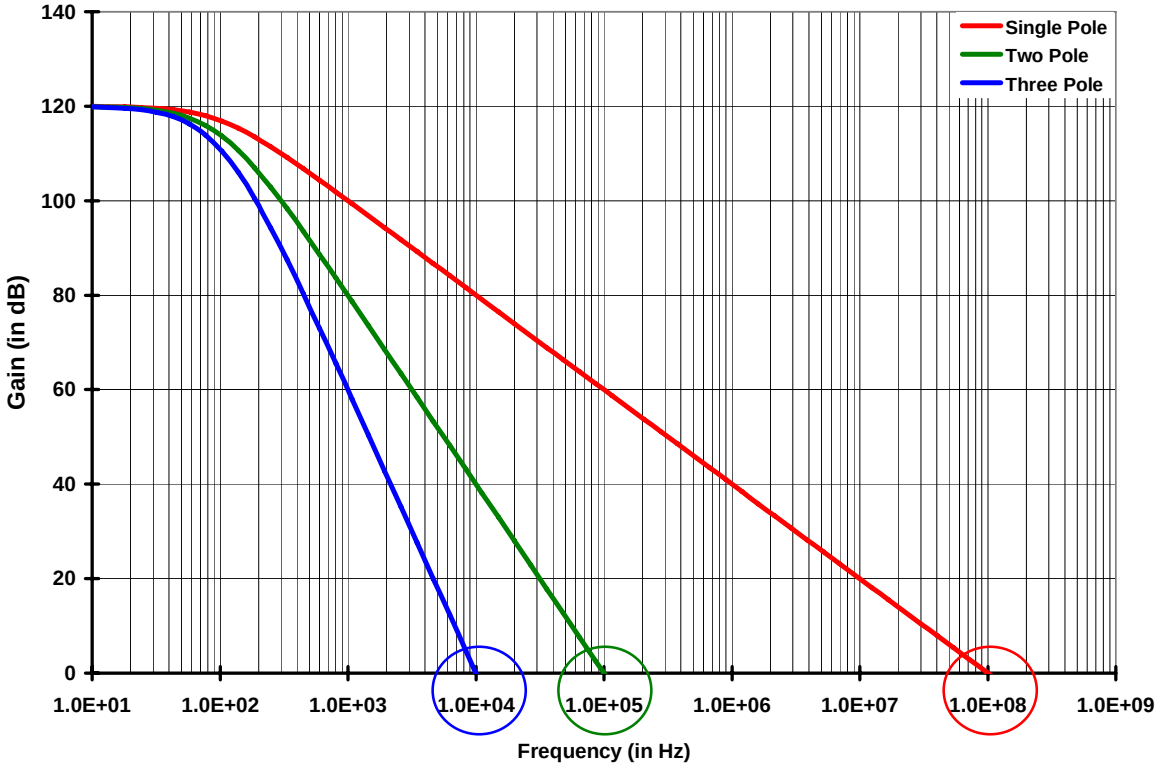

Figure A.2. Bandwidth comparison between single, double and triple pole systems

Vita

Mr. Chandra Sekhar Acharyulu Durisety was born on June 26, 1976 in Nuzvid, a small town in the state of Andhra Pradesh, India. He completed his secondary education at Andhra Muslim Sahakara Junior College, Guntur, after which he joined Birla Institute of Technology and Sciences, Pilani, one of the top-5 universities in India. Chandra got engaged to Dr. Anjani from Warangal, A.P, India on June 8th, 2006. They were married on August 5th, 2006.

Later he joined Wipro Infotech Ltd, Global R & D, Bangalore as a VLSI Design Engineer and was promoted to Sr.VLSI Design Engineer in 1999. His expertise includes implementing networking protocols in FPGA's. He lead a 4-member team to develop the generic Utopia core for interfacing ATM and Physical layers. Later he joined CMOS Chips Inc., Santa Clara, CA as Member Technical-ASIC and contracted to Toshiba America Electronic Components (TAEC), San Jose.

During his Ph.D, Chandra worked on a variety of research projects, including control circuits for use in maskless lithography using carbon nano-fibers, S/H amplifier for a 10-bit, 1.2-V pipeline ADC, digital core for the dynamic characterization of < 15-bit resolution ADC's and a perl script for automatic verilog to layout conversion. As a graduate student, Chandra published two journal papers and seven conference papers. His research interests include analog circuit design, developing algorithms for VLSI design and mixed-signal designs.