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Design and Implementation of a Complex-conjugate Shaper and Baseline Restorer for a Silicon-based Neutron Detector Front-end

Jonathan Lanier Britton
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Jonathan Lanier Britton entitled "Design and Implementation of a Complex-conjugate Shaper and Baseline Restorer for a Silicon-based Neutron Detector Front-end." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Syed K. Islam, M. Nance Ericson

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Interim Dean of the Graduate School

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A Thesis
Presented for the
Master of Science
Degree

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Jonathan Lanier Britton
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Abstract

This thesis presents the design and implementation of a CMOS shaper with baseline restoration for use in the silicon-based neutron detector front-end to be used at the Spallation Neutron Source (SNS) at the Oak Ridge National Laboratory (ORNL). The system consists of a voltage-to-current (V-to-I) converter, a four-pole complex-conjugate semi-Gaussian current-input active filter, and a ground-sensing baseline restorer (BLR) operational transconductance amplifier (OTA). The first prototype chip *Patara* has been fabricated in the TSMC 0.35-micron process, and experimental results show that proper functionality was achieved. The shaper, which is influenced by a real pole prior to the V-to-I converter, has poles at approximately 2 MHz and approximates a Gaussian output shape for an input pulse with rise time near 20 nanoseconds. The output signal has a full-width half-maximum (FWHM) of around 270 nanoseconds and a settling time of 0.6 microseconds, allowing for a 1-microsecond pulse-pair resolution. The shaper and baseline restorer have selectable polarity to accommodate input pulses of both polarities.

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Chapter 1

Overview

1.1) Introduction

Analog circuit design has always been an important part of radiation detection. In fact, many of the signal processing and pulse shaping methodologies which are today understood as fundamental to many areas of electronics were developed out of a necessity to properly collect information in radiation metrology experiments [1]. This work represents an effort to bring the current capabilities of circuit design and detector fabrication together to further the state-of-the-art in radiation detection systems, and more specifically the area of neutron imaging.

1.2) Motivation

All sectors of technology strive for the same goal – a continual increase in capability, whether it is operating speed, resolution, accuracy, or power. The field of radiation detection is no different. The Spallation Neutron Source (SNS) at the Oak Ridge National Laboratory (ORNL) is the most intense spallation source for neutrons in the world, and it brings hope of higher resolution neutron imaging that will benefit scientists of many disciplines [2]. In order to fully utilize this new research facility, new state-of-the-art high-efficiency and high-resolution neutron detectors were needed for use at the SNS facility. As a result, the High Efficiency Neutron Detector Array (HENDA) project developed silicon-based

detectors with various coatings to be used in one of the facility's test chambers [3]. These detectors have demonstrated efficiencies near 15%, with advances expected as research continues. This brought about the need for a charge-sensitive front-end with pulse-pair resolution of 1 μsec and spatial resolution of 100 microns by 500 microns. These requirements are beyond the capability of most previous and current systems [3], and so the need arose for a full-custom application-specific integrated circuit (ASIC) with these capabilities to interface with the new detectors. This work was funded under National Science Foundation Grant Number 0412208.

1.3) Scope of Thesis

The purpose of this work is to outline the design of the signal shaping section of a solid-state neutron detector front-end. This thesis will cover the design of the shaper from conception to testing of the fabricated front end, including a brief overview of phenomena occurring in radiation detection systems.

1.4) Specifications

Some performance goals were determined prior to the start of the design. Namely, system-level functionality, time response, and noise performance were dominant factors in choosing and optimizing the shaper design. The system should be able to handle both polarities of input signals, since this will be set by the type of detector used, which has not yet been finalized. Also, the detector may have one of two coatings to enhance efficiency, which has also not yet been

determined. Therefore, the total system must have a configurable scale factor. Traditionally, the noise in a particle detection system should be dominated by the charge sensitive amplifier in the front end, requiring that the noise of the shaper system should be less than 10% of the noise power spectral density (NPSD) of the preamp. Finally, each channel is mated to a specific detector pixel, which requires that the pitch between channels be 75 μm.

Some parameters, such as power consumption and power supply rejection, were not well defined and an attempt was made to make them as ideal as possible. However, design priority was given to the requirements that were defined design goals.

1.5) Organization of Thesis

Chapter two presents a review of the fundamentals of radiation detection and the associated signal processing. This is important in understanding why this project chose to diverge slightly from the classical methods. First, a brief overview of radiation detectors is given, followed by an explanation of the conventional properties and phenomena occurring in radiation detection that are typically used to characterize a system.

Chapter three outlines the design specifications of this project and observations of past designs which influenced design choices implemented in this work. Also, the preliminary design using MATLAB to optimize the pole-zero constellation of

the filter is highlighted and the results are shown. This is followed by an in-depth look at the design and operation of each of the components in the shaper system. It is shown that an operational transconductance amplifier (OTA) driving an R-lens active filter with an OTA baseline restorer is the preferred system. Finally, a brief description of the layout is given.

Chapter four presents some experimental results from the fabricated chip. These results are compared to the design requirements and the expected results from simulation.

Chapter five outlines the conclusions drawn based on the design process and the performance of the fabricated chip. Also, future work needed to improve the design and complete the system is discussed.

Chapter 2

Fundamentals of Radiation Detection and Signal Processing

2.1) Background

Radiation detection and electronics share a very rich history of innovation, likely second only to the use of electronics in communications [1]. Though not quite as sordid a story (probably because communications was more commercially lucrative), the history of analog electronics in radiation detection systems shows that numerous approaches have been used for various experiments. The following chapter outlines some of the phenomena that have been shown to occur in these systems and some conventional design techniques.

2.2) Detecting Radiation

2.2.1) Solid-state Detectors

The backbone of radiation detection systems is the detector itself. Usually, as is the case in this work, the front-end electronics are designed around the operating characteristics of the detector. Because of the breadth of information required to treat this topic, only the basic information relating to the HENDA detector is covered. HENDA will be a solid-state detector which is etched to form an array of 170 μm-deep holes filled with ^{6}LiF, a neutron-reactive material. It will be set up in a reverse-biased configuration, and will have a neutron detection efficiency

of η > 15%. HENDA is expected to have a fairly constant charge collection time of approximately 20 nsec and a detector capacitance of 5 pF to 10 pF [3].

2.2.2) Charge-sensitive Preamplifiers

In general, the detector preamplifier is the most significant block of a radiation detection system next to the detector itself. In a few cases, the charge collected by the detector produces a sufficiently large voltage pulse across its detector capacitance so that no voltage gain is necessary [4]. Typically, however, voltage gain is required to properly condition the signal. Direct voltage amplifiers can be used in some situations, employing the classical inverting amplifier concept. However, many detectors, including solid-state detectors such as the one that will be used in the present system, require charge-sensitive preamplifiers. With proper choice of input and feedback time constants, the voltage gain can be made relatively insensitive to variations in the detector capacitance during an incident signal [4]. Some of the phenomena commonly occurring in systems employing charge-sensitive amplifiers are detailed in the proceeding sections. For further reading on charge-sensitive amplifiers, see [5] - [8].

2.3) Pulse-rate and Pole-zero Cancellation

A generic detector front-end is shown in Figure 2-1. The waveform generated at the output of the preamplifier by the input signal charge from the detector has the general shape shown in Figure 2-2. This shape is caused by the long decay time for $\tau_c = 1/(RC)$ of most charge-sensitive preamplifiers, where $\tau_c >> T_{pulse\_rate}$. This

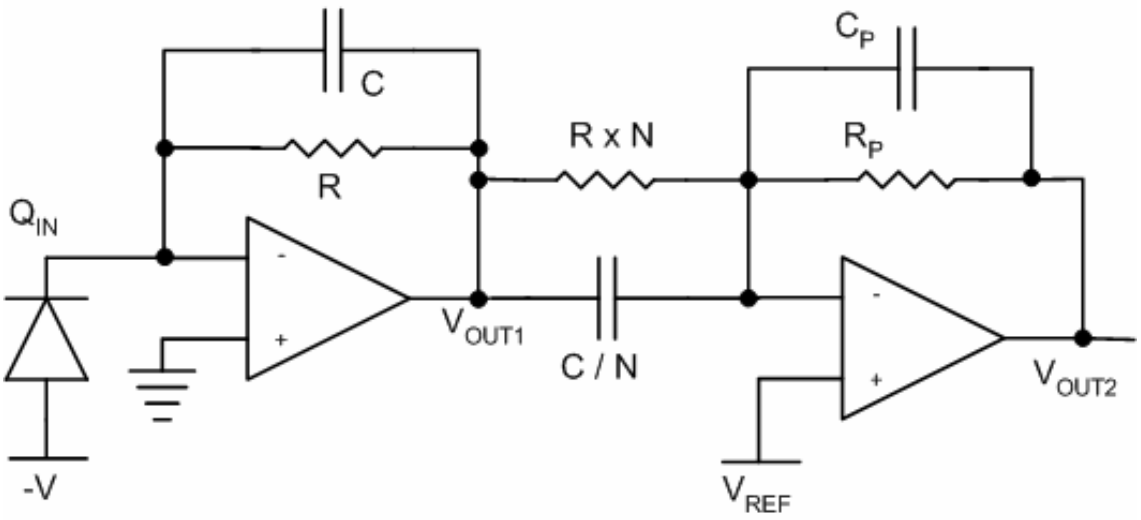

Figure 2-1 - Simplified front-end diagram

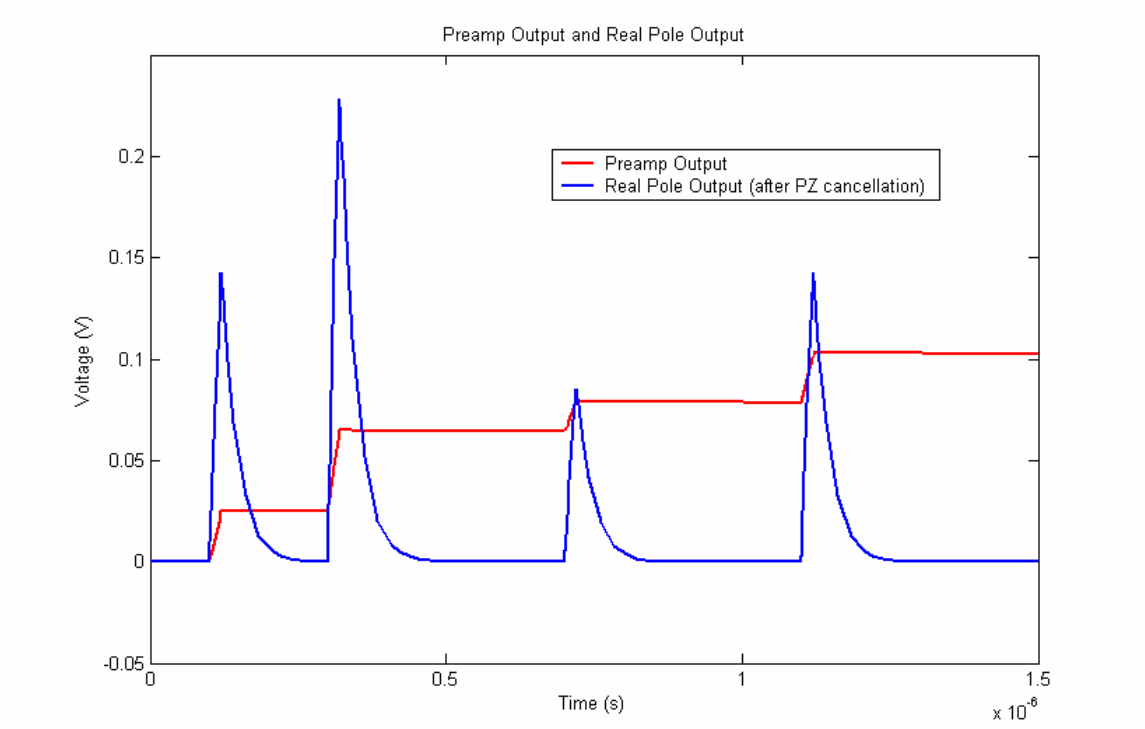

Figure 2-2 - Preamplifier output (exhibiting pulse pile-up) and low-pass filtered signal after pole-zero cancellation

large time constant aids in charge collection, but can cause the proceeding circuitry to saturate since these pulses will be coming in on top of each other, where the height of one pulse will decay very little before the peak of the next pulse is summed with it. The transfer functions for such a system are

$$\frac{V_{OUT1}}{I_{IN}} = \frac{R}{1+sRC}\ , \qquad \text{2-1}$$

$$\frac{V_{OUT2}}{V_{OUT1}} = \frac{R_P}{R \times N}\frac{\left(1+s\frac{C}{N}R \times N\right)}{\left(1+sR_PC_P\right)}\ \text{, and} \qquad \text{2-2}$$

$$\frac{V_{OUT2}}{I_{IN}} = \frac{R_PR}{R \times N}\frac{\left(1+s\frac{C}{N}R \times N\right)}{\left(1+sRC\right)\left(1+sR_PC_P\right)}\ \text{[9].} \qquad \text{2-3}$$

A very succinct solution to this problem exists that is founded in elementary frequency response principles: a pole at a given frequency can be cancelled by a zero at the same frequency, which theoretically yields a unity impulse response (or some scalar thereof) [10]. Then, the final decay time can be set by another pole at the desired frequency (set by R_P and C_P in the present example), leaving a shorter overall decay time and lesser likelihood of saturating the channel circuitry. The shape is changed, but no amplitude information is lost in the process. It will later be shown that this real pole is set, along with the shaper poles, to provide an impulse response satisfying the time resolution needed in this system. Nominally, R_P = 35 kΩ and C_P = 2 pF.

2.4) Pulse Pile-up

If the pole-zero cancellation is implemented correctly, the decay time of the pulse should be less than the reciprocal of the maximum expected pulse rate. Still, the pulse rate is simply a characteristic time measurement for a given system. There is a finite probability that two pulses will occur separated by a time less than the reciprocal of the pulse rate, leading to two types of phenomena. *Peak pile-up* occurs when two or more pulses are spaced so closely in time that they appear as one pulse with a greater magnitude than any single pulse alone. *Tail pile-up* occurs when a second pulse follows after the pulse has begun to decay, but not far enough removed so that the first pulse has had time to come sufficiently close to the baseline level [10]. Now, as long as saturation does not occur, pile-up causes no signal-handling problems internally in the circuit. Its effects are only problematic when trying to interpret pulse magnitudes and timing at the output. Post-event pile-up rejection will not be implemented in the shaper discussed in this work. Instead, the shaper will be designed to minimize the likelihood of pile-up effects from occurring to begin with.

2.5) Signal Shaping

From the previous discussion outlining detectors and charge-sensitive preamplifiers, one might conclude that these two comprise a sufficient detector front-end. Ideally, this would be true, since the output would contain the pertinent amplitude information and would consist of a signal produced by a system with a known impulse response. However, the problem arises when one attempts to

extract this information *from* the signal with non-ideal processing electronics. The following section describes the reasons and methods for shaping the input signals.

2.5.1) Ballistic Deficit

Ideally, the time constants in a shaping system would be infinite to allow a non-perfect pulse to produce a shaped signal which reaches a steady state. Unfortunately, this would only allow the amplitude detection of one pulse for all time (not very practical). *Ballistic deficit* is a measure of the difference between the real output signal amplitude and the ideal steady-state amplitude for the same input, as shown in Figure 2-3 [10].

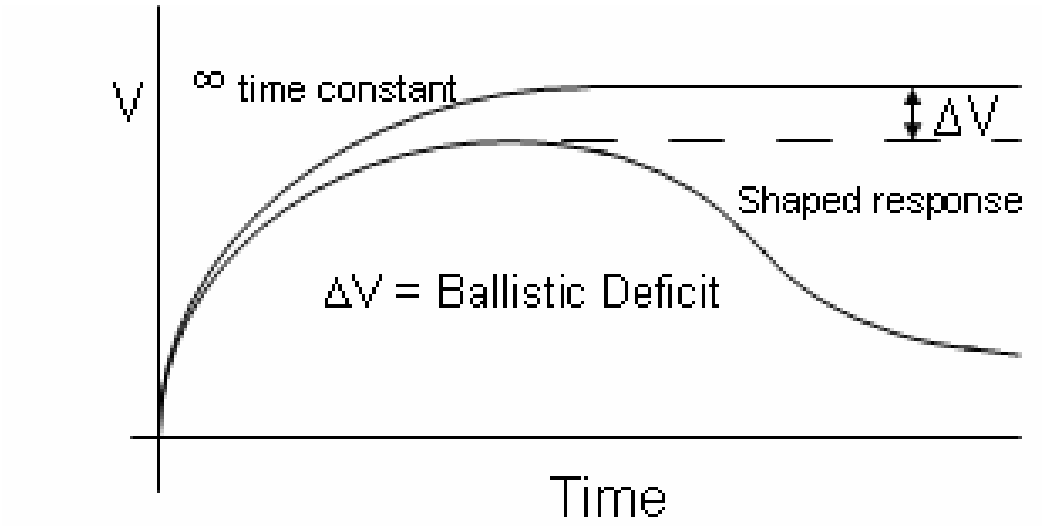

Figure 2-3 - Ballistic deficit effects

If the charge collection time in the detector is constant, then the fraction of the pulse height that is lost due to ballistic deficit is also constant, and the system can be adjusted accordingly. However, if the charge collection time is not constant, then input pulses with longer rise times will experience a greater ballistic deficit, resulting in a disproportionate amount of pulse height being lost. This non-linearity can be detrimental to the performance of some systems. Fortunately, the detector implemented in this system has a fairly constant charge collection time.

2.5.2) Pulse Shaping

If the preamplifier and pole-zero circuitry are working correctly, we should expect the input to the shaping stage to be a pulse with a fast single-pole decay to avoid pile-up. It has already been asserted that gathering pulse-height information from a fast pulse has several drawbacks and requires complex circuitry. Keeping in mind the drawbacks of the other extreme — shaping with infinite time constants — a compromise must be reached. It is subsequently desirable to pass this pulse through a shaping filter which accommodates high pulse rates, retains amplitude information, and presents the output pulse with low noise. The system characteristics which determine these properties are discussed in the following sections.

2.5.3) Full-Width Half-Maximum

Full-Width Half-Maximum (FWHM) is defined as the width in seconds of a pulse (side wall to side wall) at exactly half of the maximum (peak) value the pulse amplitude reaches. This is an important parameter in that it is a straightforward way to evaluate basic properties of Gaussian and semi-Gaussian waveforms. It also has convenient implications regarding the quantification of the noise performance of the system.

2.5.4) Time to Peak

Time to peak is a measure of the time it takes a pulse to reach its peak value, as shown in Figure 2-4. This can be measured as the 1%-to-100% rise time. Ideally, the time to peak should be constant regardless of the peak height. The system under discussion is relatively insensitive to time-to-peak variations since we are not explicitly determining peak height, but instead determining if any part of the pulse is greater than the threshold.

2.5.5) Figures of Merit

It will be noted in the next section that the Gaussian signal shape is very attractive for its noise and processing characteristics. Unfortunately, one must settle for a semi-Gaussian shape in any real system because it would require an infinite shaping time (and a non-causal system) in order to realize a Gaussian response. Therefore, as the Gaussian shape is approached, it helps to have a

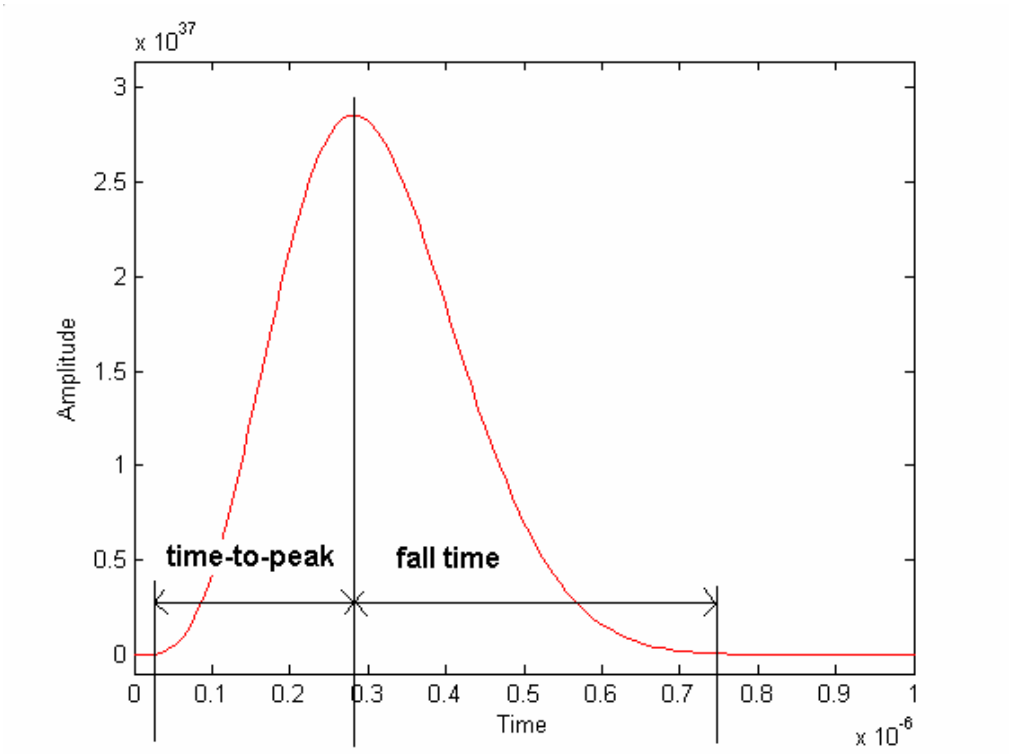

Figure 2-4 - Time-to-peak of output semi-Gaussian shape

characteristic parameter to measure against. A very simple test can be established by noting that the Gaussian shape is perfectly symmetric in time (about its peak). Its 10%-to-Peak rise- and Peak-to-10% fall- times are identical. Therefore, its 10%-to-10% time is exactly double the 10%-to-Peak rise time. For the purpose of this work, the ratio of these two quantities will be designated $R_R = Tr_y/Tr_x$, so that Gaussian shapes, by definition, entail $R_R = 2$ [11]. Semi-Gaussian shapes necessarily have $R_R > 2$.

2.6) Baseline Shift

2.6.1) Causes and Effects

As will be shown later, it is generally desirable to use a CR-$(RC)^n$ or CR-(Semi-Gaussian Lowpass) filter configuration in order to allow higher pulse resolution while still making the amplitude information within the pulse accessible in a real-world system. Further consideration, however, reveals that the average voltage (DC component) across the capacitor C must be zero, or

$$V_{out,DC} \equiv V_{in,AVG} \text{ [10].} \qquad 2\text{-}4$$

For a capacitively-coupled signal processing chain, this would present no problems since the signal will retain its shape regardless of offset, assuming it does not approach the supply rails. Remember, however, that the information is carried in the pulse amplitude, which will be compared to a DC reference using a comparator circuit to determine if the signal is large enough to be considered a

neutron ‘hit’. Assuming a train of pulses uniform in both time and amplitude, the offset will be systematic and could therefore be compensated for by changing the ‘hit’ threshold. Clearly, though, this is an unrealistic scenario. Considering a more plausible signal chain, Campbell’s theorem can be applied to show that the baseline shift for a system whose input is unit impulses randomly distributed in time is a function of the impulse response, $h(t)$, and the average pulse rate, λ [12].

$$\overline{V}_{baseline} = \lambda \int_{-\infty}^{\infty} h(t)dt \qquad 2\text{-}5$$

Further, Nicholson asserts that the baseline shift can be expressed in terms of the average pulse height [10]. For root mean square (RMS) input charge of $(Q_{mean}^2)^{1/2}$, detector input capacitance of C, and input resistance of R, the baseline RMS fluctuation is

$$V_{RMS} = \left(\overline{Q}^2 \frac{\lambda R}{2C} \right)^{\frac{1}{2}} \qquad 2\text{-}6$$

The instantaneous baseline shift at the output of the preamp will then be multiplied by the voltage gain of the system, leading to loss of resolution in the system.

2.6.2) Unipolar vs. Bipolar Shaping

Since it is obvious that the detected signals will not be uniform in both time and amplitude and the baseline problem associated with random pulses is known, some solution must be found to maintain the baseline. One way to minimize the amount of baseline shift is not actually a corrective method, but in fact an approach that fundamentally avoids baseline shift altogether. This is achieved by choosing the impulse response shape to have no DC component, that is, the impulse response has equal area above and below circuit ground. In radiation detection signal processing this is known as *bipolar shaping*, whereas a system with a positive- or negative-only response has *unipolar shaping*.

Bipolar shaping has several drawbacks though. Foremost of these is that the signal-to-noise ratio (S/N) is always worse than its unipolar counterpart [4]. Also, for a given pulse length, the bipolar pulse will have a smaller region of relative flatness, which requires the use of more complex amplitude analyzer circuits in spectroscopy measurements due to the need to measure a sharper peak. Further, the shorter time constants in the bipolar response relative to the corresponding unipolar response cause a larger ballistic deficit.

Unipolar pulse shaping also has another advantage over bipolar pulse shaping. If the signal chain is direct-coupled and the signal pulse is unipolar, the shaping filter can be set to maximize dynamic range. This is the case in the current design, as the filter is designed to receive only positive incoming signals. For a

strong negative-valued component of the signal, some devices would be pushed into the linear region.

Baseline shift is also due to several other properties of the system. These include internal offsets and charge injection into the baseline hold capacitor. Further, in direct-coupled systems, some pulses may have undershoots with long settling times.

2.6.3) Baseline Restoration

If the shaper has been designed with a pulse-pair resolution well above the mean burst rate, then it is reasonable to assume that the energy passed through the shaper will be small enough and far enough separated in time to affect the baseline by a relatively small amount, as shown in Figure 2-5 (c) and (d).

However, over time or in the presence of several large events occurring nearly simultaneously, the baseline may indeed shift by a sizeable amount, shown in Figure 2-5 (a) and (b). One solution to this is to pick some time T_r much greater than the inverse of the average pulse rate. Every T_r seconds the baseline will be forced to return to the desired zero-signal level. This obviously affects performance while signals are coming in since the output is being forced to a certain state. However, if the detection system has a known time when no neutrons will be incident on the detector, then the baseline restorer can be active during this time only, which is the case in the system under discussion.

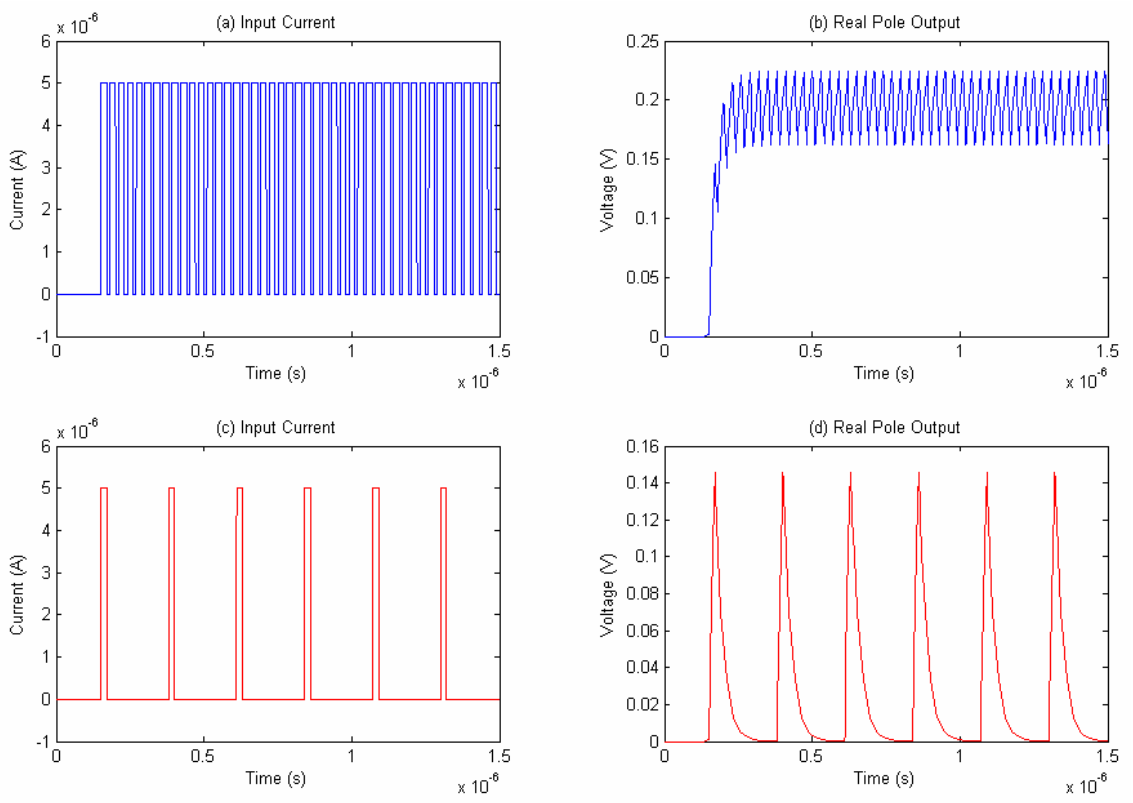

Figure 2-5 - (a) Incoming pulse train higher than pulse-pair resolution capability, (b) Resultant waveform from (a), (c) Incoming pulse train lower than pulse-pair resolution capability, (d) Resultant waveform from (c)

Chapter 3

Designing a Shaper/Baseline Restorer for the SNS Front-end

3.1) Specifications

The most important design requirements for the shaper section of the SNS front-end arise because of the need to interface with the preamp and pole-zero circuits. Design considerations are made according to the performance specifications determined by the needs of the system as a whole. Unfortunately, the system definition was not complete at the time of design because the detector itself was unfinished. Remember that part of the novelty of this work is that it will interface with a high-resolution, high-efficiency neutron detector, which is beyond the capability of most current systems [3]. Therefore, the *Patara* readout channel was designed to be as generic as possible, including adjustable gain, polarity, and leakage current cancellation. While this opens the door for a wider range of uses for *Patara*, it also added complexity to the system and greatly increased the design time. This section outlines the design process for the shaper filter and baseline restoration circuit.

3.2) Design Conclusions from Background Research

Several conclusions can be drawn from the many systems evaluated in the literature search. First, we must find a filter that can handle low frequencies as compared to most g_m-C filters. Also, since a semi-Gaussian pulse response has

been chosen, the filter topology must lend itself to a seamless implementation of complex poles. We also want to avoid complex feedback since five complex conjugate poles is a sufficient semi-Gaussian approximation [4], [13], [14]. Also, the design will consider the possibility of current-mode signals.

The signal from the front-end (Figure 3-1) that will be coming into the shaper is shown above in Figure 3-2. The pulse has, at this point, already been filtered by a single low-pass pole. This filter will serve as the lone real pole of the semi-Gaussian shaper. Therefore, recognizing the need for additional complex poles, the following generic block diagram of Figure 3-3 was proposed.

3.3) MATLAB Optimization

In preparation for the design of the shaper, it was desired that the optimum pole-zero constellation should be determined prior to the conceptual circuit schematic. For obvious reasons, the number and placement of poles have a tremendous effect on the resolution and noise performance of the shaper. MATLAB was the chosen tool for this task because of its powerful built-in functionality which aids in calculating time-domain impulse responses, as well as its plotting versatility.

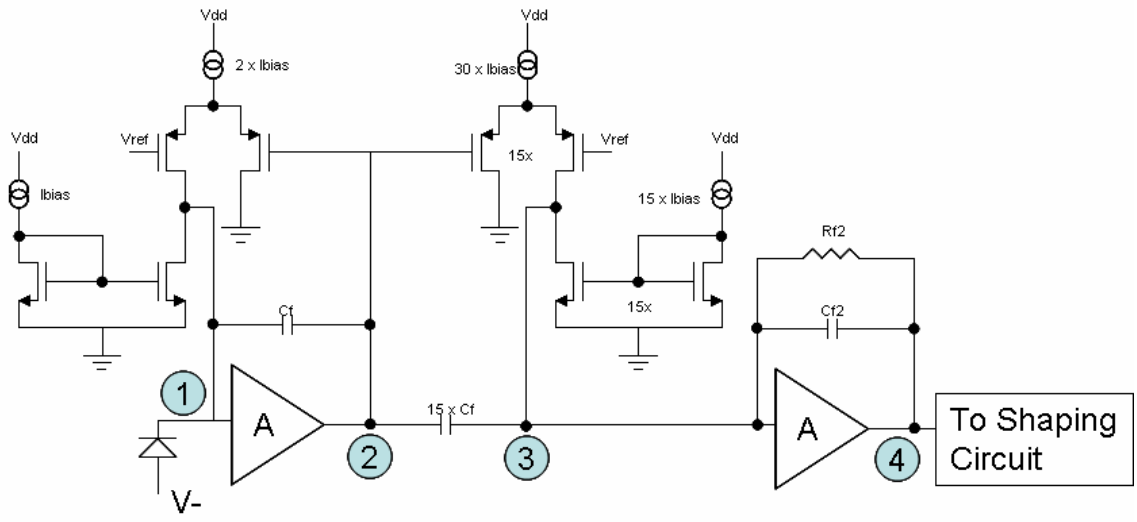

Figure 3-1 - Conceptual preamplifier / pole-zero circuitry with real-pole lowpass active filter

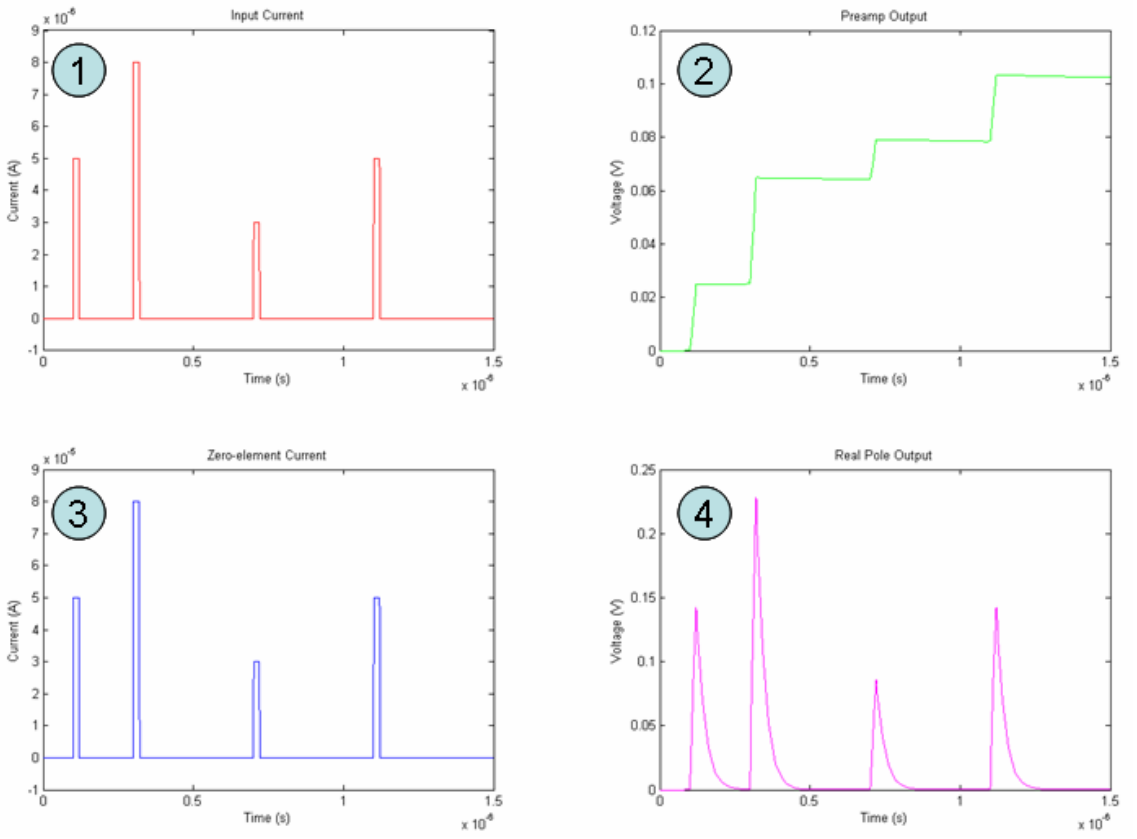

Figure 3-2 - (1) Input current signal, (2) Output of preamplifier with long tail decay time, (3) Total current through pole-zero elements, (4) Output from low-pass first real pole

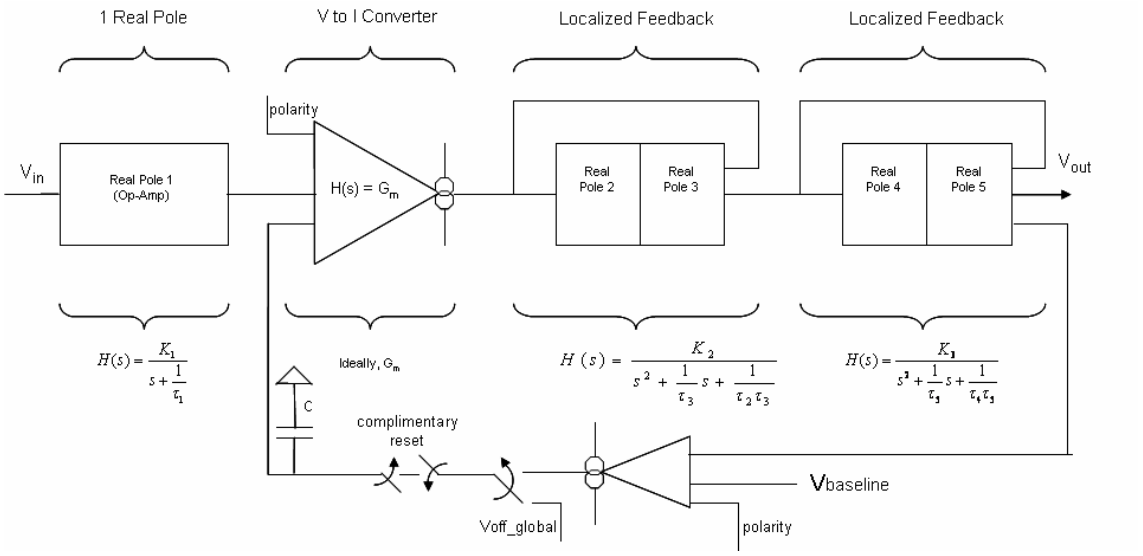

Figure 3-3 - Conceptual shaper diagram

3.3.1) Noise

Noise performance is one of the most important characteristics of charge-detection electronics. Ideally, one desires that the front-end amplifier dominate the noise of the detection channel since it typically has a much higher gain than the rest of the circuitry. However, if not designed properly the shaper can contribute appreciable noise in the signal chain. It is the case that not all response shapes are equal regarding signal-to-noise ratio (SNR) as mentioned previously, and in fact there is a signal which exhibits a maximum theoretical SNR for an input having the shape of a decaying exponential. However, this response, the *infinite cusp*, is not practically possible. Many other response shapes have been used, and some of them are shown in Figure 3-4 with their associated attributes. The semi-Gaussian response was chosen for this design for several reasons. It is a great compromise between maximum theoretical noise performance and return-to-baseline time (pulse rate capability). Also, as will be shown, it is fairly straightforward to implement.

3.3.2) Number of Poles

Obviously, to obtain a true Gaussian response requires an infinite number of poles. This is a problem in practice, since it would also mean infinite chip area and infinite power dissipation if using active filters, as well as producing a non-causal signal! However, according to Knoll, a semi-Gaussian shape can be adequately approximated using four poles [4]. Since a real pole (low-pass active

Response	τ_{opt}	F	RMS flicker noise
Infinite cusp	-	1.000	-
Triangular	$3.46\ \tau_c$	1.075	1.665
DL-RC	$1.29\ \tau_c$	1.098	1.626
Gaussian		1.120	1.773
Semi-Guassian	$0.378\ \tau_c$	1.165	1.810
CR-$(RC)^2$	$0.57\ \tau_c$	1.215	1.847
CR-RC	τ_c	1.359	1.992
$(CR)^2$-$(RC)^4$		1.380	
$(CR)^2$-RC	$1.40\ \tau_c$	1.410	-

Figure 3-4 - Normalized noise performance (F) of different impulse responses [10]

filter) has already shaped the signal before it reaches the shaper, four more poles will be implemented in the shaper. Using an even number of poles allows for the direct implementation complex-conjugate pole-pairs, which will help in more closely approximating a Gaussian shape, as shown in Figure 3-5. This allows improvement over shapes such as the one implemented in [15]. Therefore, the overall system has a five-pole complex-conjugate pole-zero constellation.

3.3.3) Radial Variation of Curvature

As shown above, the semi-Gaussian response with a finite number of poles can be made more Gaussian by using complex-conjugate poles instead of all real poles. Taking into account the figure of merit, R_R, developed earlier, the pole constellation was varied to make R_R as close to 2 as possible, since $R_R = 2$ is a desirable property of a true Gaussian shape.

MATLAB was used to perform these iterations. The method employed was to place the real pole at a set frequency. Then, a second point on the real (σ) axis away from the real pole was chosen, and an arc with a center at the second point was generated that passed through the real pole. Thus, it had a radius equal to the distance between the two points. The two sets of complex-conjugate poles were then placed on the arc, with equal spacing between poles in the $j\omega$ direction. The second point was then swept across the real axis so that the radius of the arc was changed. The ratio R_R was calculated for each, and the

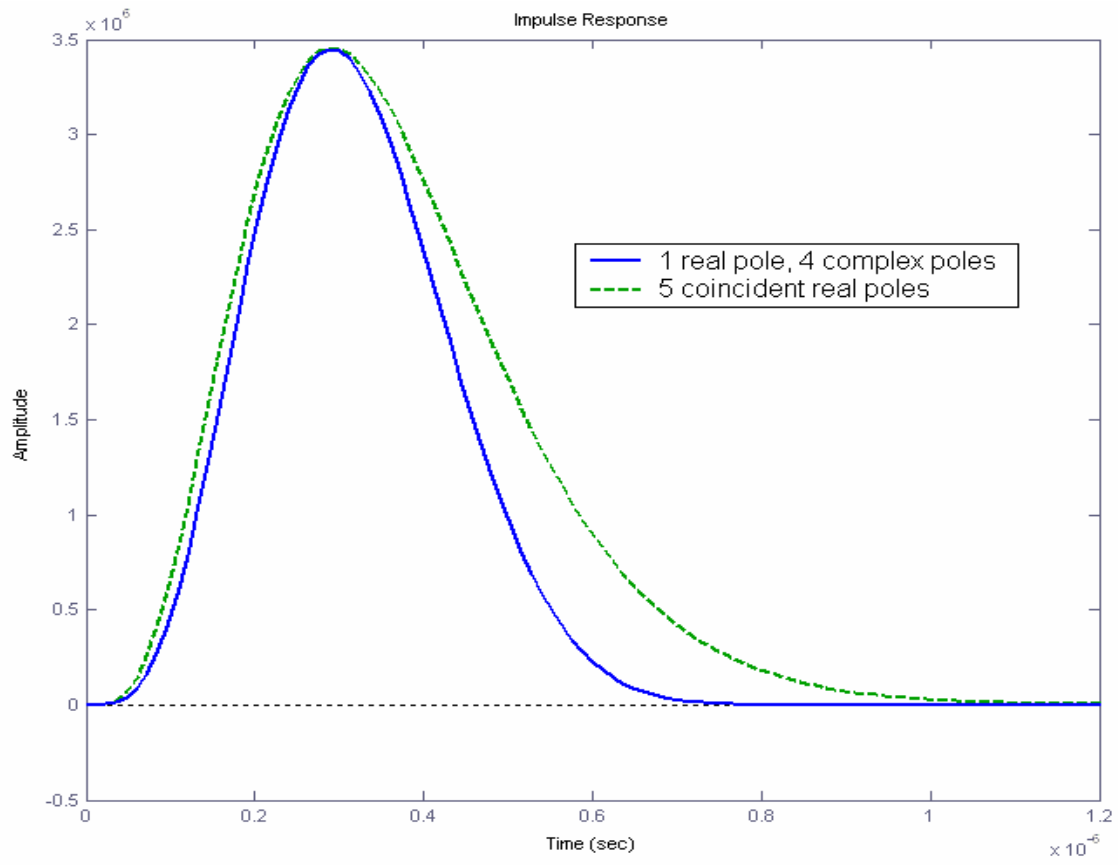

Figure 3-5 - Peak-normalized semi-Gaussian response for 5 real poles versus 1 real, 4 complex poles

best achieved ratio of $R_R \approx 2.65$ was achieved. The resultant pole-zero constellation and impulse response is shown in Figure 3-6. The frequency response of the shaper is shown in Figure 3-7.

3.4) Filter Considerations - Real Pole

The shaper section technically begins with a real pole generated by a voltage amplifier with an RC feedback path. The pole value was determined based on the MATLAB calculations presented above. As mentioned before, the resistor was chosen to be 35 kΩ, while the capacitor had a value of 2 pF.

The voltage amplifier pole is a very efficient way to transition into the shaping section of the system because in connection with the impedance from the zero, it creates a classically-connected inverting amplifier at the output of the preamp. Recall that before the first real pole after the pole-zero compensation circuit, the signal current in the passive elements creating the zero theoretically is of the same waveform as the detector pulse, and the care taken in designing the preamplifier to handle the pulse would be negated if the frequency performance limitations of a voltage-to-current conversion improperly replicated the signal. The voltage gain of the first real pole in conjunction with the zero was set to provide a peak of approximately ±325 mV for the expected peak pulse from the detector of 120 fC.

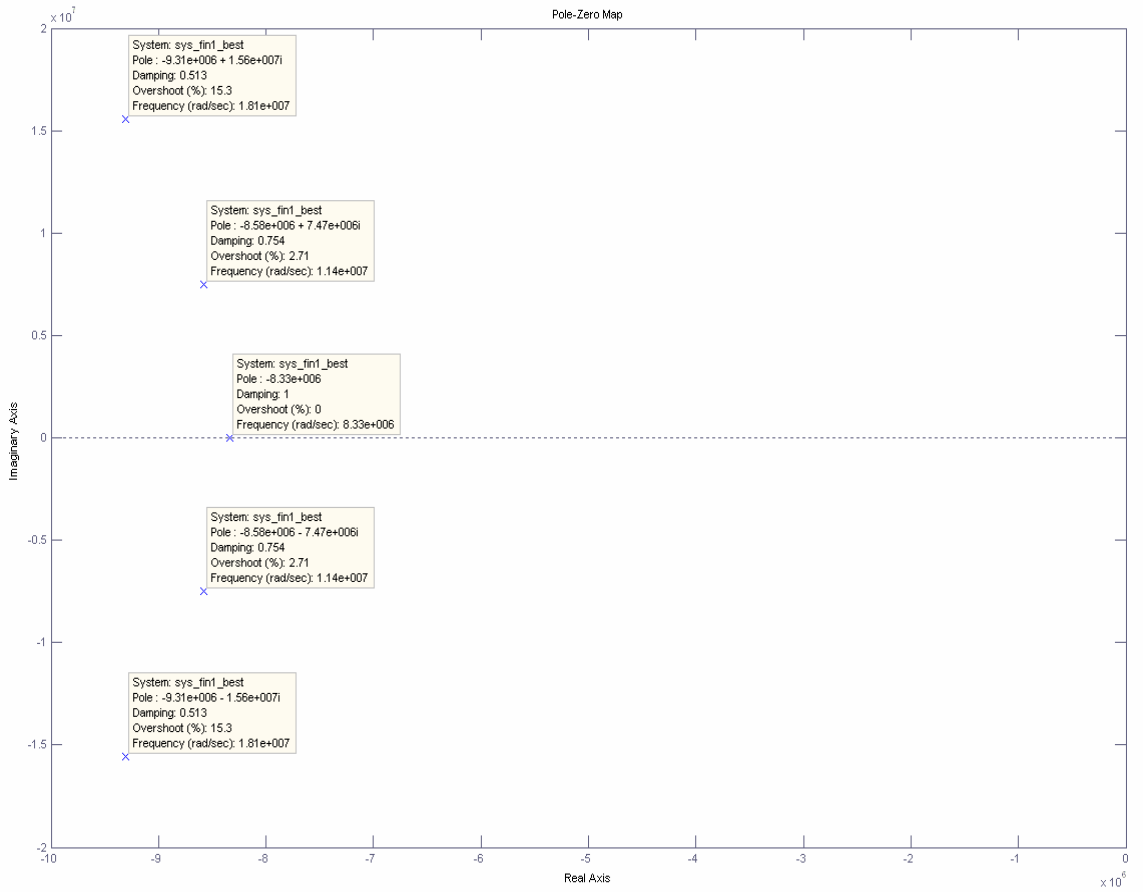

Figure 3-6 - Optimized pole constellation for complex-conjugate semi-Gaussian pulse response

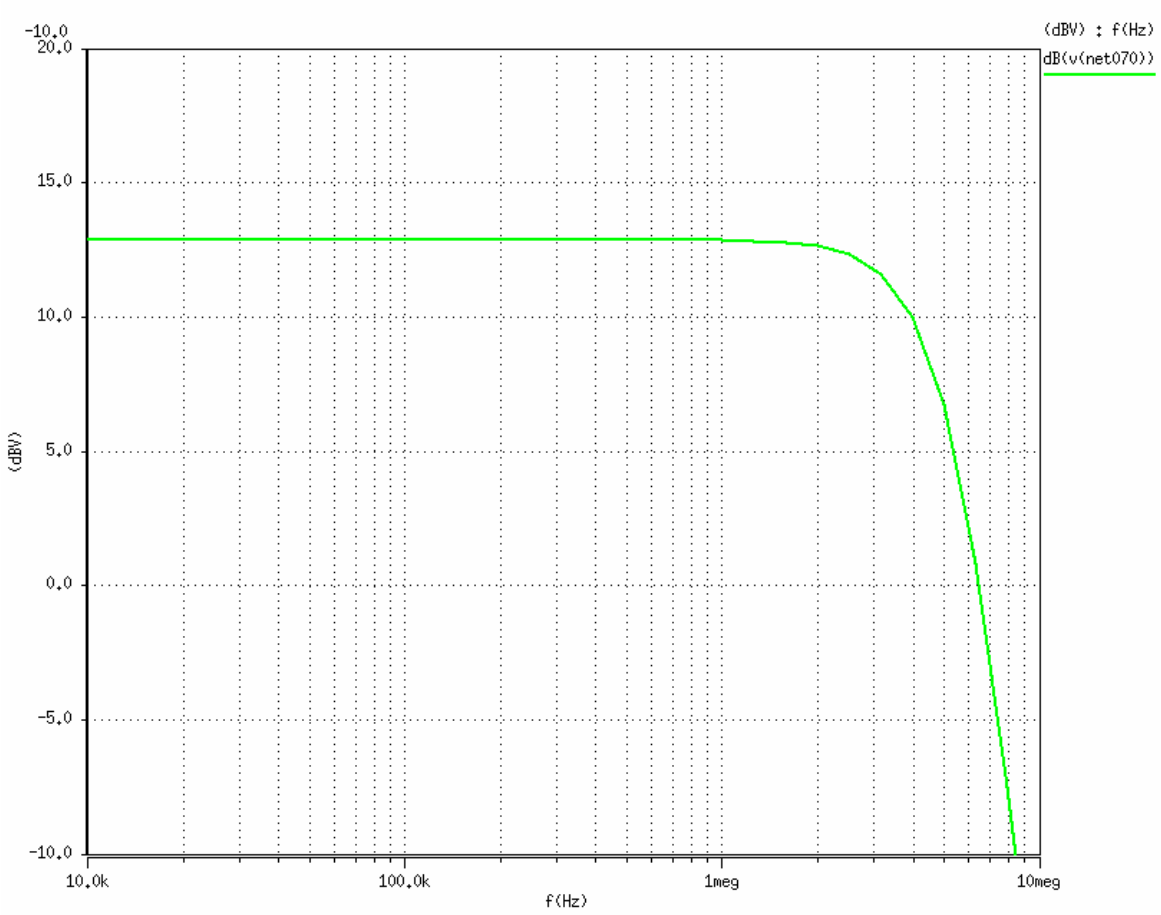

Figure 3-7 - Simulated shaper voltage gain vs. frequency

3.5) Complex-conjugate Filter Design

3.5.1) Voltage-input vs. Current-input

Strictly speaking, the inclusion of the phrase *current mode* in the description of a filter topology is a misnomer, stemming from the fact that a purposely-induced time constant is a trademark quality of filters. Therefore, the voltage across parallel resistor and capacitor elements becomes an important state-variable. Instead, Gilbert suggests the phrase *free mode* [16]. Semantics aside, it remains that the transition to *current signals* at certain points in a design can be leveraged to improve linearity and dynamic range (among other things) if used judiciously. This was given due consideration during design.

3.5.2) Explanation of R-Lens Filter Operation

The *R-Lens filter* was first reported by Bertuccio et al. [17]. This filter has several attractive features for use in radiation detection pulse shaping. Further, this filter is capable of attaining some of the design goals specific to this application. It will be shown that this filter is capable of low frequencies relative to standard g_m-C filters, high linearity, voltage or current output, and the straightforward implementation of complex poles.

The basic single-pole R-Lens filter schematic is shown in Figure 3-8. As stated previously, this filter should not be considered *current mode* because the voltage at the gate of M1 is an important state variable, but it does have a *current mode* input. The drain of the relatively V_{DS}-insensitive (due to high r_o) device M2 is held to a voltage that varies as the voltage across C and an equivalent circuit resistance; thus the small-signal input impedance of the circuit appears as a low-pass parallel RC filter. The general concept on which this filter operates is the feedback action resulting from the current-multiplication (or *magnification*, hence the term *Lens*) factors M_1 and N_1 resulting in an enhanced voltage drop across R. Small-signal analysis of the circuit is simplified by evaluating the gate to source

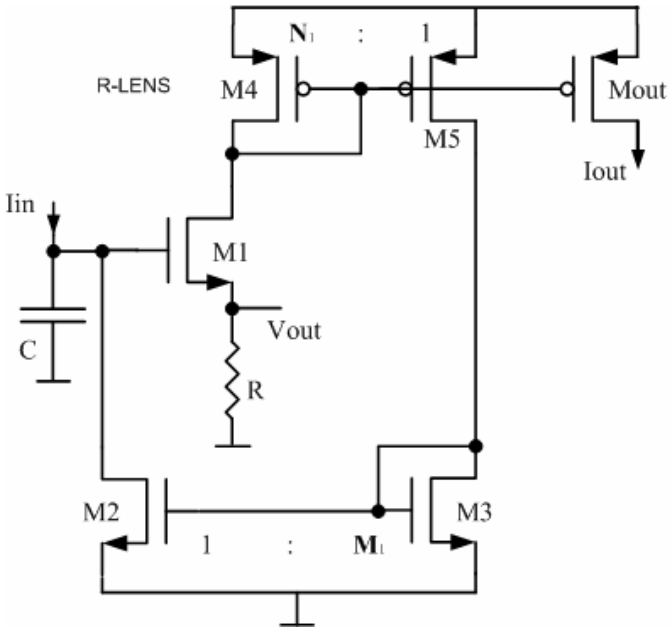

Figure 3-8 - Basic R-Lens filter schematic

voltage gain of M1 [18].

$$A_{S-G,M1} = \frac{v_{S,M1}}{v_{G,M1}} = \frac{1 + g_m R_S}{g_m R_S} \qquad 3\text{-}1$$

Assuming g_m is large, the small-signal gate voltage variation of M1 is equivalent to the small-signal voltage across R. Therefore, the source and gate of M1 can be lumped into one node. The derivation of the transfer function for the filter is shown in Appendix A, giving the final result to be later adapted to Figure 3-9,

$$\frac{v_{OUT}}{i_{IN}} = \frac{M_1 N_1 R}{1 + sM_1 N_1 RC} \ . \qquad 3\text{-}2$$

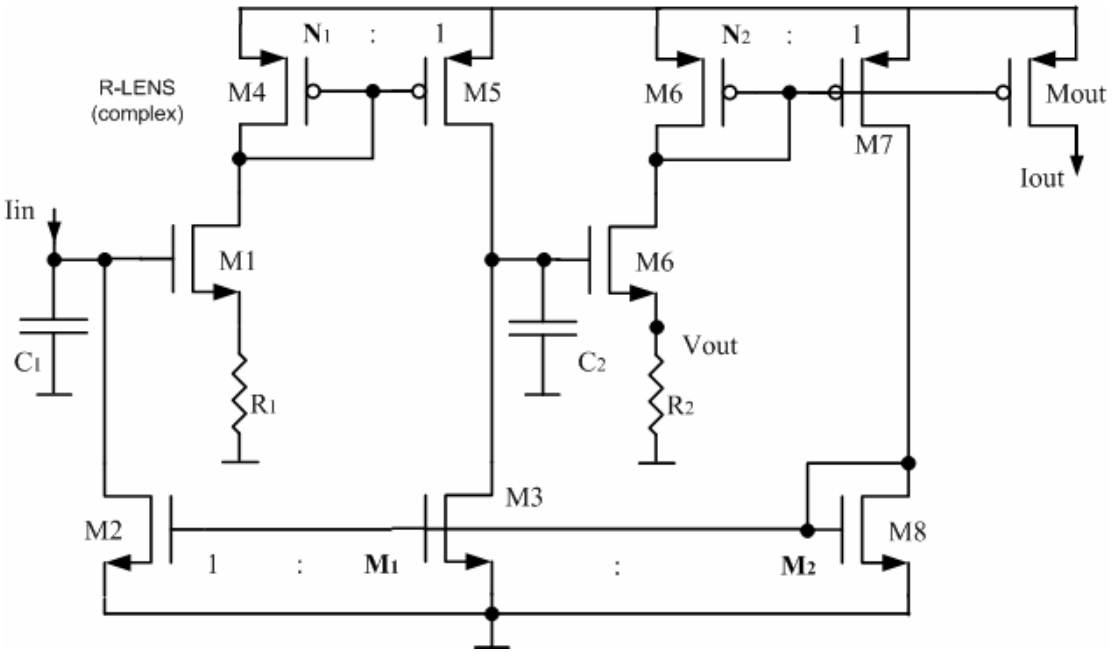

Figure 3-9 - Complex R-Lens filter schematic

Notice that the physical resistance R is enhanced by the factors M_1 and N_1, allowing the filter to use a smaller resistor to achieve the same time constant compared to passive devices, saving chip area. The circuit also adapts readily to a complex pole implementation. Following the concepts reported on by Buzzetti et al. as shown in Figure 3-9, the following transfer function can be achieved [19]. The derivations are shown in Appendix A.

$$\frac{i_{OUT}}{i_{IN}} = \frac{M_2}{M_2 s^2 (N_1 R_1 C_1)(N_2 R_2 C_2) + M_1 s(N_1 R_1 C_1) + 1} \qquad 3\text{-}3$$

Now if M_1 = M_2 = 1, the straightforward classical 2nd-order system response theory is simply related by

$$\frac{i_{OUT}}{i_{IN}} = \frac{1}{s^2 (N_1 R_1 C_1)(N_2 R_2 C_2) + s(N_1 R_1 C_1) + 1} = \frac{1}{\frac{s^2}{\omega_n^{\,2}} + s\left(\frac{2\xi}{\omega_n}\right) + 1}, \qquad 3\text{-}4$$

where

$$\omega_n = \frac{1}{\sqrt{N_1 R_1 C_1 N_2 R_2 C_2}} \quad \text{and} \quad \xi = \frac{1}{2}\sqrt{\frac{N_1 R_1 C_1}{N_2 R_2 C_2}} \text{ [20].} \qquad 3\text{-}5$$

The two poles represented in Equation 3-4 become complex conjugates if the following criterion is met:

$$4 \cdot \left(\frac{N_2 R_2 C_2}{N_1 R_1 C_1} \right) > 1. \qquad 3\text{-}6$$

The cascaded four-pole complex-conjugate filter is shown below in Figure 3-10.

3.5.3) Gain

The overall mid-band gain is controlled by several factors. The first pair of poles has a current gain set by $M_2 N_{T1}$, while the second pair of poles has a transimpedance of $M_{22} N_{22} R_{22}$. When coupled with the transconductance of the V-to-I converter, the shaper attains an overall low-frequency voltage gain of

$$\frac{v_{OUT}}{v_{IN}} = G_{m,OTA} M_2 N_{T1} M_{22} N_{22} R_{22} = 488\ \mu\text{S} \cdot (1) \cdot (1) \cdot (1) \cdot (2) \cdot 5.7\ \text{k}\Omega \approx 14.9\ \text{dB}. \qquad 3\text{-}7$$

For the threshold 'hit-level' expected shaper input of 32.5 mV, this results in an output voltage swing of ~160 mV.

The individual stage gain is as important as the overall gain of the shaping filter. Simply, the individual stage gains should be set so that one does not easily saturate the next stage. This is discussed in more detail in Section 3.5.5).

3.5.4) Linearity

The linearity of the R-lens active filter is much improved over standard g_m-C filters. Since the real resistor R_1 is effectively in series with the transconductance

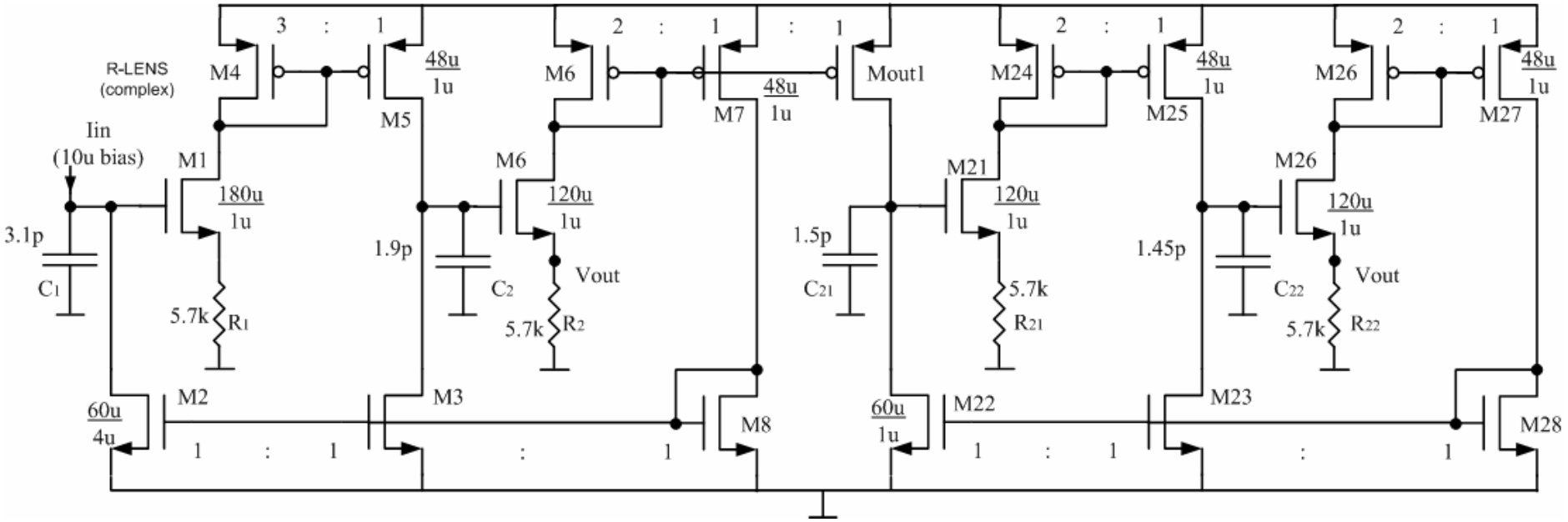

Figure 3-10 - Four-pole cascaded complex conjugate R-Lens filter schematic

of the buffer device M1 of Figure 3-8, the effective real component is $\approx M_1 N_1 (R_1 + 1/g_m)$. If ($R_1$ >> $\Delta 1/g_m$), the time constant is fairly insensitive to variations in g_m. For example, the input current signal at the threshold level is of the same order of magnitude as the bias current, yet the filter exhibits non-linearity less than a few percent until the very limits of the expected input signal. In the design of Figure 3-10, for all real resistors, R_x = 5.7 kΩ, and for transistors M1, M6, M21, and M26, $(1/g_{m,MX})_{nominal}$ = 1.2 kΩ to 1.8 kΩ. However, for very large signals, the change in (R_1 + $\Delta 1/g_m$) becomes enough to affect the pole constellation significantly. Coupled with the large-signal limitations due to the finite output resistances of the MOS devices, non-linearity greater than 5% is observed at the maximum expected signal level. The dynamic range of the filter is limited by the distortion caused by these non-linearities, but the effects this will have must be evaluated in light of the overall system functionality. Remembering that the shaper output will be sensed by a comparator, it is evident that non-linearity well past the hit threshold is inconsequential. Therefore, the signal-to-noise ratio (S/N) *at the threshold level* is more important than the overall dynamic range of the filter.

3.5.5) Power Dissipation

Each individual set of complex pole-pairs is biased by a 10-μA bias current. Therefore, in the chosen configuration, it was important that the output mirror device Mout1 have N_T = 1. This sets the mid-band current gain equal to unity so that the two stages are biased alike. This helps improve matching, as well as

keeps the first stage from easily saturating the input to the second stage. With the chosen device ratios, the two complex-conjugate pairs together dissipate 0.5 mW in their quiescent state.

3.5.6) Noise

Assuming noiseless active devices, this circuit exhibits an *improvement* in noise performance versus a passive parallel RC filter. This is due to a "noise cooling effect" [17]. The thermal noise current originating in the physical resistance R_1 is attenuated by the factors M_1 and N_1, leaving the input referred noise current as

$$i_n = \frac{4kT}{R_1 M_1 N_1} \left(\frac{A}{\sqrt{Hz}} \right) \qquad 3\text{-}8$$

However, it happens that transistors M2, M3, and M8 of Figure 3-9 actually dominate the noise performance of the circuit. This is because their noise currents are directly reflected to the input due to the 1:1 sizing of these mirror devices. Most of the noise seen at the input is due to flicker noise in these N-type elements, since the noise corner is only two decades below the -3 dB filter frequency. The noise currents of the PMOS devices M4 and M6 are diminished by the factors N_1 and N_2, respectively, while those of M5 and M7 are directly reflected. However, the flicker noise in PMOS devices, in general, is roughly an order of magnitude less relative to their NMOS counterparts in a given

technology [21]. The noise performance of the circuit could be better in a BiCMOS process using NPN transistors as mirror devices [17], [19].

Since all poles lie approximately the same distance from the origin of the *s*-plane, they all have approximately equal magnitudes. Therefore, absolute pole order is not crucial. This would be a consideration if the pole magnitudes were significantly different, and it would be optimum to have the lowest pole last since it would have the smallest noise bandwidth and would best filter out the internal noise sources of the preceding stages.

3.6) Operational Transconductance Amplifier Design

An operational transconductance amplifier (OTA), the equivalent of an unbuffered opamp, was chosen as a voltage-to-current (V-to-I) converter. This block is needed to convert the lowpass RC-filtered voltage signal into a current-mode signal to drive the current-input R-Lens filter. The OTA is unbuffered because it drives a very light load, nominally the parallel combination of small-signal resistances $r_{o,BIAS}$ and $r_{o,IN}$ of the R-Lens circuit of the next stage.

3.6.1) Topology

The topology for the V-to-I converter is a simple two-stage amplifier, as shown in Figure 3-11. The input devices are chosen with high g_m for several reasons. First, high g_m increases the OTA's overall transconductance. Typically, using diode loads in a differential-pair input stage compromises gain for symmetry. If

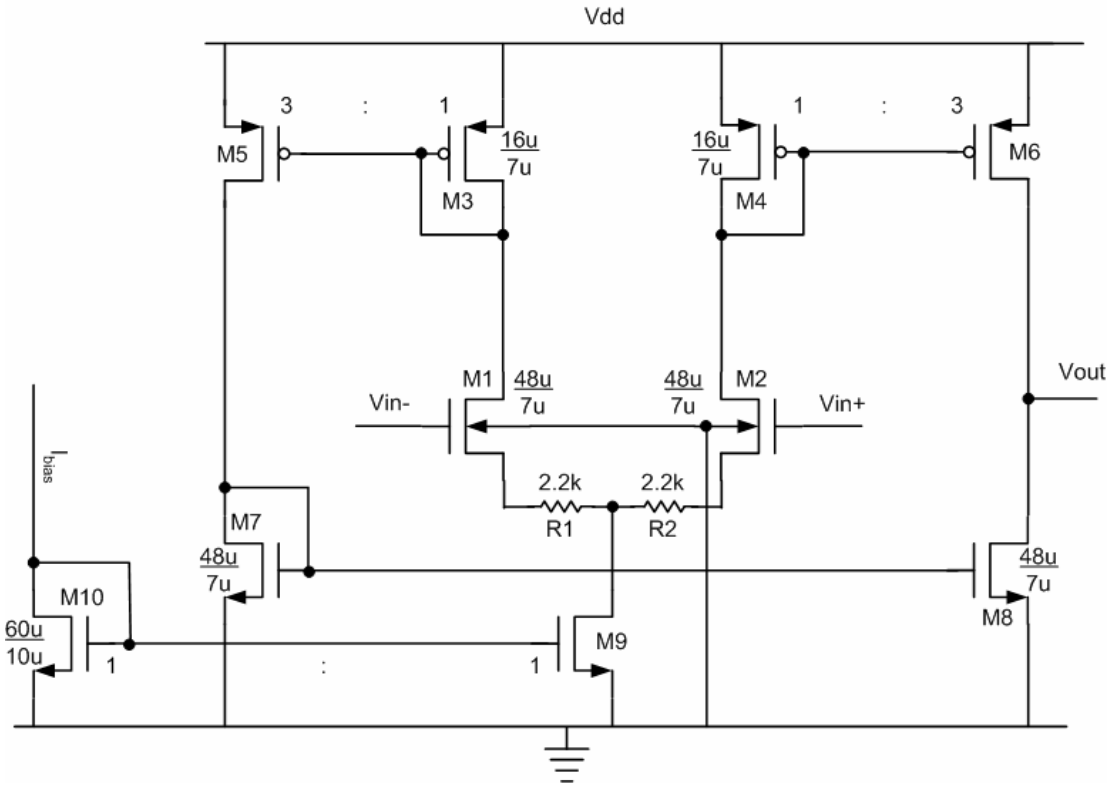

Figure 3-11 - Voltage-to-current converter operational transconductance amplifier topology

the sizing, and therefore g_m, of the input and load devices were equivalent, the stage would provide effectively no voltage gain (0 dB). By making $g_{m,IN}$ different than $g_{m,LOAD}$, gain is achieved through

$$\left|A_{v1}\right| = \frac{g_{m2}}{g_{m4}}, \qquad 3\text{-}9$$

allowing the input stage to increase or decrease the voltage gain by an order of magnitude [22]. Second, high g_m in the input stage reduces input-referred offset voltage.

Once optimum g_m was found, device size W/L was finalized. Clearly with respect to absolute W and L values, a larger WL product is important to minimize input referred flicker noise since the flicker noise bandwidth lies inside the filter's passband. However, too large a WL product decreases frequency performance via feedthrough in the C_{gs} of the differential pair. Simulations using large WL-product input devices showed degradation of the pulse shape since the OTA could not properly replicate the high-frequency signal. Therefore, W and L were reduced proportionally just until signal degradation was not evident, thereby putting priority on basic signal shape.

3.6.2) Linearity

In addition to ensuring that the V-to-I converter's frequency performance was sufficient to replicate the incoming signal, the other imperative design aspect is

the linearity of the OTA over the expected input pulse amplitude range. One simple method is to employ a source degeneration technique in the input pair. In optimizing the tail current versus source degeneration effects on linearity, the tail current was set by I_{bias} = 100 μA, while R1 = R2 = 2.2 kΩ. This greatly improves the linear input range, but does diminish the overall transconducance gain contributed by the input stage.

3.6.3) Input Common Mode Range (ICMR)

The input common mode range (ICMR) specification on this OTA is not an extremely important design aspect since the system has a flexible common-mode voltage constraint. Due to the active feedback elements around the charge-sensitive preamplifier, there is zero DC current through the feedback elements when no signal is present at the preamp input, and therefore zero voltage drop across the opamp/real pole feedback elements preceding the V-to-I converter. The virtual ground at the input of the opamp/real pole block is set to mid-supply (1.6 V) via an off-chip reference voltage. Therefore, the DC gate voltage to the input devices of the OTA is ideally constant.

3.7) Baseline Restorer (BLR) OTA Design

3.7.1) Topology

The topology for the baseline restorer amplifier is show in Figure 3-12. It is a fairly simple two-stage OTA with ground-sensing inputs, diode loads in the input

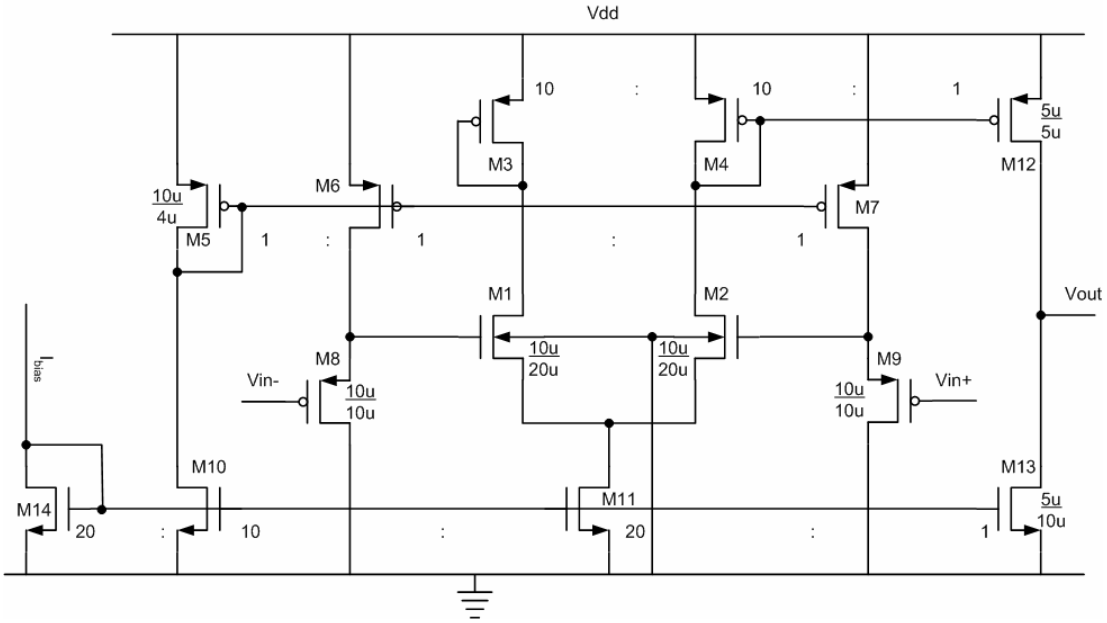

Figure 3-12 - Baseline restorer operational transconductance amplifier topology

pair, and a current mirror loaded output stage. Most importantly, the OTA needs to have a low overall transconductance, G_m, in order to ensure BLR loop stability. Due to the need for a low overall transconductance, low-g_m input devices will be used, and will be aided by the current mirror load that will provide lower overall G_m than the push-pull configuration used in the V-to-I converter's output stage.

3.7.2) Ground Sensing Capability

In contrast with the V-to-I converter, ICMR is a major design consideration for the BLR OTA. With no signal present and the V-to-I converter inputs at 1.6 V_{DC}, the voltage output of the shaping filter is approximately 100 mV. Since the BLR OTA input directly samples the DC output voltage, the common mode range input voltage must be able to sense voltages near the lower supply rail. This is

accomplished through using PMOS input devices in a source-follower configuration connected to an NMOS differential pair gain stage.

3.7.3) Loop Bandwidth

When the BLR is active, it completes a negative feedback loop so that the rest of the shaper circuitry — the V-to-I gain stage and four-pole low-pass filter — are its feedback element, while the hold capacitor is its load. Since the feedback elements have an intentionally-diminished magnitude response and phase shift at higher frequencies, the combination of phase and magnitude could make the feedback loop unstable. Therefore, certain inputs at higher frequencies will cause the BLR loop to oscillate. To avoid this problem, the dominate pole set by the BLR OTA's transconductance and load capacitance will be set at a frequency well below that of the filter, causing the BLR loop gain to drop below 0 dB well before significant phase shift is encountered in the filters. This will not affect the OTA's ability to set the baseline level, since it is a DC voltage.

Since the hold capacitor has been designed at 5 pF, we will use the g_m of the input stage to set the bandwidth of the OTA.

$$GBW = \frac{g_{m,M1}}{2\pi C_L} M, \quad M = {W_6 L_4}/{L_6 W_4} \qquad 3\text{-}10$$

Once g_m is reduced sufficiently, $g_{m,Ml}/C_L$ will set the dominate pole for the BLR loop. The frequency response of the active BLR loop is shown in Figure 3-13.

3.7.4) Diode Loads

As can be seen from the system diagram in Figure 3-3, one input of the BLR OTA samples the shaper output voltage, while the other input is connected to the *desired* baseline reference. It is obvious that for an infinite loop gain, the difference between the desired baseline and the actual output voltage is simply the input offset of the BLR OTA. Therefore, diode loads were used to provide first-stage symmetry. Unfortunately, this cuts the voltage gain in half, but does reduce the input referred offset voltage.

3.7.5) Output Stage

The conditions placed on the performance of the output stage were initially thought to be very straightforward. The $V_{OUT,SWING}$ of the amplifier will hover around mid-supply (~1.6 V), so no special considerations were taken regarding this. Also, a simple active load was used, which was fine since overall Gm needed to be low. As will be discussed later, the output resistance was lower than desired and caused some systematic offsets in the BLR loop.

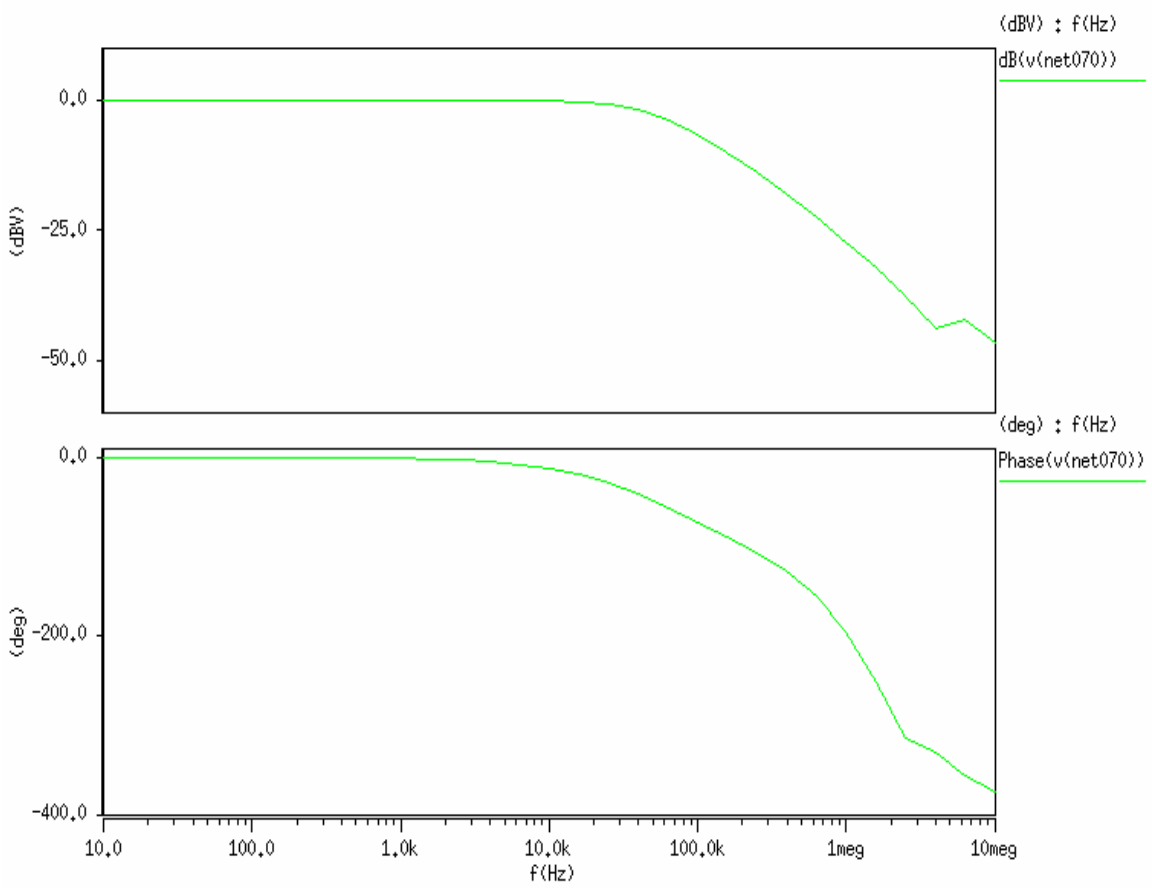

Figure 3-13 - Baseline restorer loop frequency response

3.7.6) Loop Placement Considerations

The baseline restoration loop was chosen to sense the output DC level, and wrap around to the input of the V-to-I converter OTA. Again considering Figure 3-3, note that the hold capacitor, C, is at a high-impedance node, which will allow it to ideally hold a DC voltage while the baseline restorer loop is not active. Note, however, that it is susceptible to injected noise charge from the switches and the substrate. Since the other input of the V-to-I converter is connected to the output of an operational amplifier in feedback, the performance of the operational amplifier is not greatly affected by a change in the DC voltage. However, if the hold capacitor were instead connected at the input to the operational amplifier, a change in the DC voltage would directly affect the active pole-zero cancellation circuit, leading to significant signal distortion.

3.8) CMOS Technology Chosen for this Project

The CMOS process chosen for fabricating the *Patara* chip was Taiwan Semiconductor Manufacturing Company (TSMC) 0.35-μm bulk process [23]. The reasons for choosing this process were varied. Initially, legacy issues were a major concern. The HENDA detector and associated electronics are intended to benefit researchers for years to come, so the process chosen must be a current standard, and one which will likely be offered for several years to come. Since the final 64- or 128-channel chip will be finalized 12 to 18 months after the initial prototype chip, this avoids having to re-design and re-layout the phase 2 chip. Also, the TSMC 0.35-μm process is a robust process that this particular design

group has had previous experience with. The *Patara* chip will also eventually be mated to detector strips with 100-μm pitch, therefore minimum channel length can make a significant impact on layout when the MOS input device can have a W/L ratio on the order of 1000/1. Finally, TSMC 0.35-μm is an inexpensive process.

3.9) Layout

The layout for the *Patara* chip is shown below in Figure 3-14. Layout was done using the Virtuoso layout tool in the Cadence design environment. The chip was designed for the TSMC 0.35-μm CMOS process, and measured 4.0 mm x 2.5 mm in area, including the pad frame.

3.9.1) Layout Considerations

Each channel in the *Patara* chip corresponds to a respective detector pixel. When completed, *Patara* will be physically mated to the linear detector array. Consequently, each readout channel must be narrower than the pitch between the detector pixels, which is 100 μm. To avoid cross-channel interference and sufficiently separate the power rails, the channel height was chosen to be 75 μm including the rails, leaving 69 μm of vertical space for CMOS circuitry.

Device matching was hindered to some extent by the floorplan of the design. Therefore, critically matched devices were laid out using the common-centroid technique to the maximum extent possible. Also, devices used shared-sources

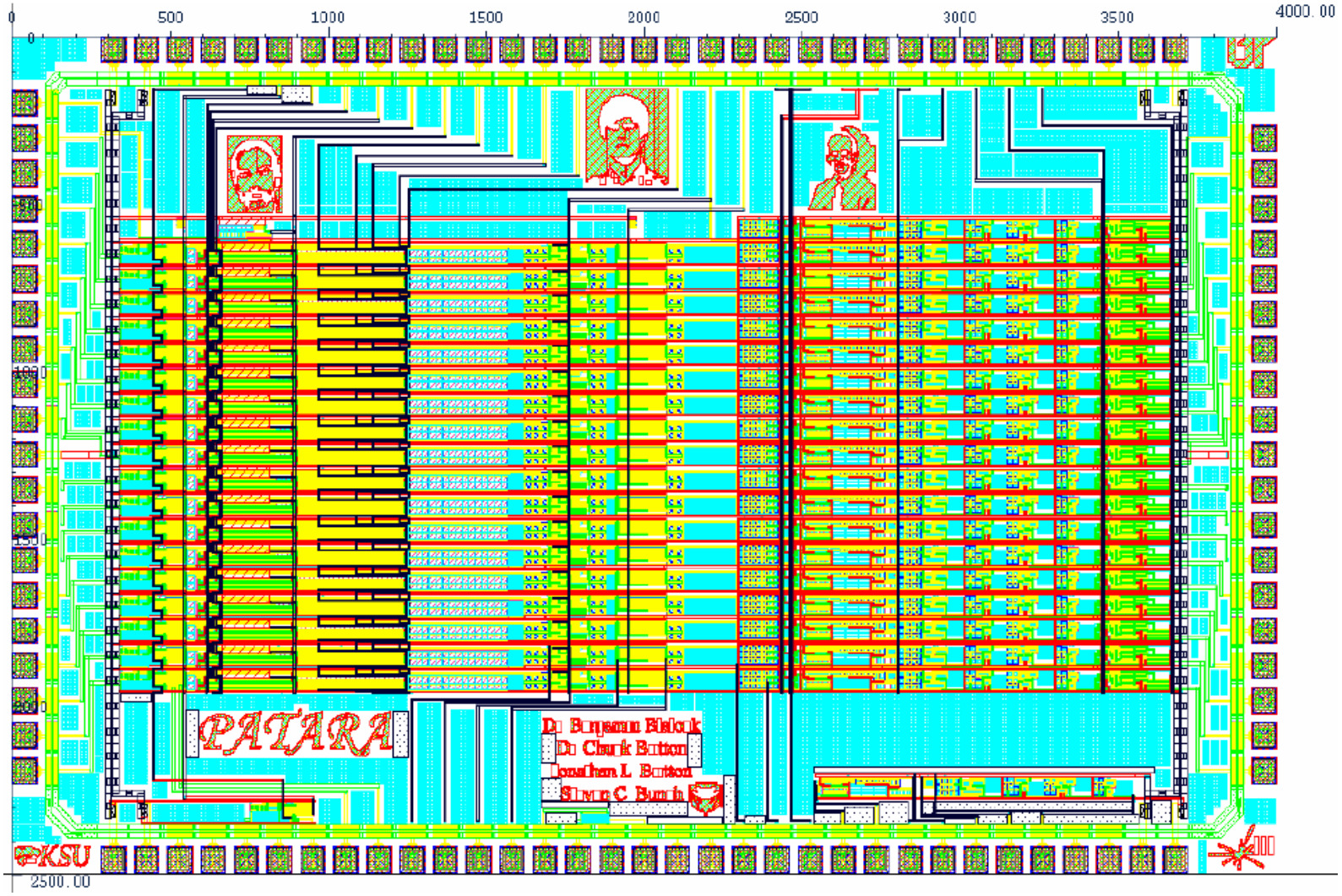

Figure 3-14 - *Patara* Layout (TSMC 0.35-μm CMOS)

and shared-drains when applicable. Capacitors and resistors were laid out in multiples of a predetermined unit-sized device, and guard rings were used on almost all active devices.

3.9.2) Switches

Transmission gates were used as switches that enable and disable the baseline restoration loop. These featured a shared drain on the PMOS device to minimize drain capacitance. The PMOS devices were also roughly twice the size of the NMOS devices (due to lower mobility). Further, charge injection is not symmetrical, and will be different depending on whether the switches are opening or closing. Simulations were iterated until total charge injection while the loop is opening was approximately zero. The transition to the open-loop state is most critical since the baseline voltage following the ‘switch opening’ transition is the baseline that incoming signals will see.

Chapter 4

Measured Results

4.1) Overview

This chapter presents the measured results from the fabricated *Patara* chip, including the shaper loop as well as end-to-end (full channel) measurements. The *Patara* chips were bonded directly to a daughterboard to avoid capacitive loading of the outputs. The main channel outputs were buffered by discreet bipolar emitter followers. This daughterboard was then mated to a motherboard, which contained readout and bias circuitry, and was then covered with a copper-plated box to isolate the chip from light and radio-frequency (RF) interference. This setup is shown in Figure 4-1. Measurements were made using a Fluke 81438 multimeter, BNC-connected coaxial cables to an oscilloscope, or with an active FET probe, depending on the application.

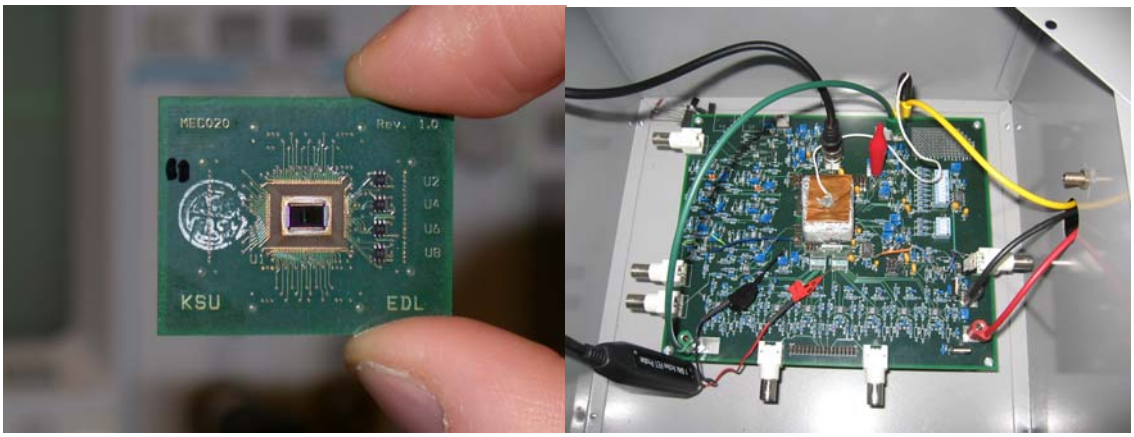

Figure 4-1 - *Patara* daughterboard and motherboard

4.2) Shaper Results

Perhaps the most telling measurement of the functionality of the shaper is the general pulse response shape itself. As is seen in the oscilloscope screen capture in Figure 4-2, the shape is a very good semi-Gaussian approximation. It has minimal undershoot and returns to the baseline very quickly. Figure 4-3 shows a comparison of the peak-normalized MATLAB predicted pulse response and the measured pulse response. These two match extremely well. Slight variations in the pulse shape are due mainly to inaccurate device models concerning absolute values of the passive devices as well as on-chip mismatch. Further, MATLAB simulations have the luxury of an ideal impulse input, while the

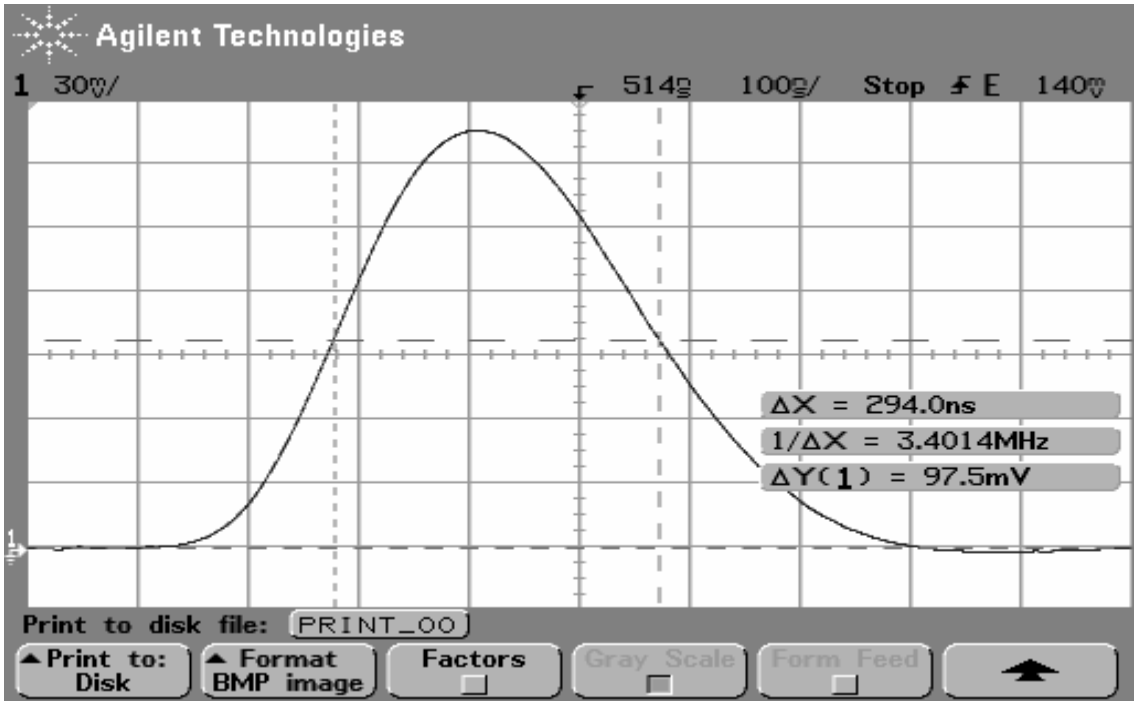

Figure 4-2 - Measured system output shape

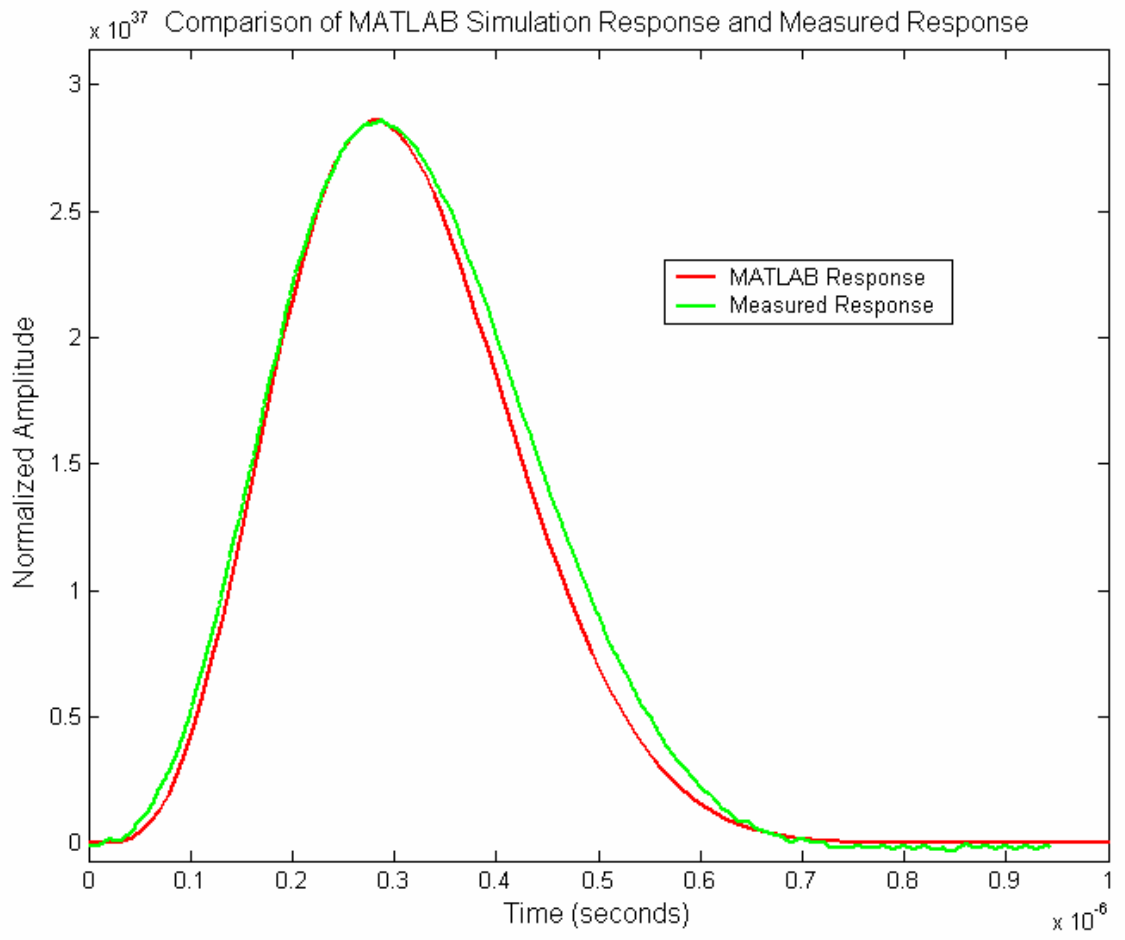

Figure 4-3 - Comparison of MATLAB predicted pulse response and measured response

pulse delivered by the channel has a finite width of approximately 20 nsec, as well as undershoot and long settling times.

Less important to this specific application, yet important to the possible use of *Patara* in other radiation detection systems and as a measure of the non-linearity of the shaper, is the shaper's time-to-peak and full-width half-maximum values over input signal range. Variations in both are due to dynamic operation. For

example, the time-to-peak will change as the pole constellation, and hence frequency response, changes due to variation in g_m of the voltage follower in the complex-conjugate circuitry. The FWHM changes as the output begins to saturate due to the finite r_o of the current mirror devices which magnify the current through the real resistors. Fortunately, both parameters, shown in Figure 4-4 and Figure 4-5, do not vary significantly until very high signal levels. To further minimize these effects, the input signal peak height should be constrained to prevent dynamic operation.

Figure 4-6 through Figure 4-9 shows the resultant output shape for different preamplifier settings – shaper settings were held constant for these measurements. These correspond with the time constant and gain settings, which are controlled by the programmable nanoampere current source. The *Patara* chip demonstrated that the large time constant / full gain setting is the best input to the shaper for the front end. This indicates that the pole-zero circuitry is optimum at this setting, and that signal distortions due to non-ideal pole-zero tracking appear at the input to the first real pole amplifier for the other settings. The main signal shape variations appear to be settling issues, such as significant undershoot.

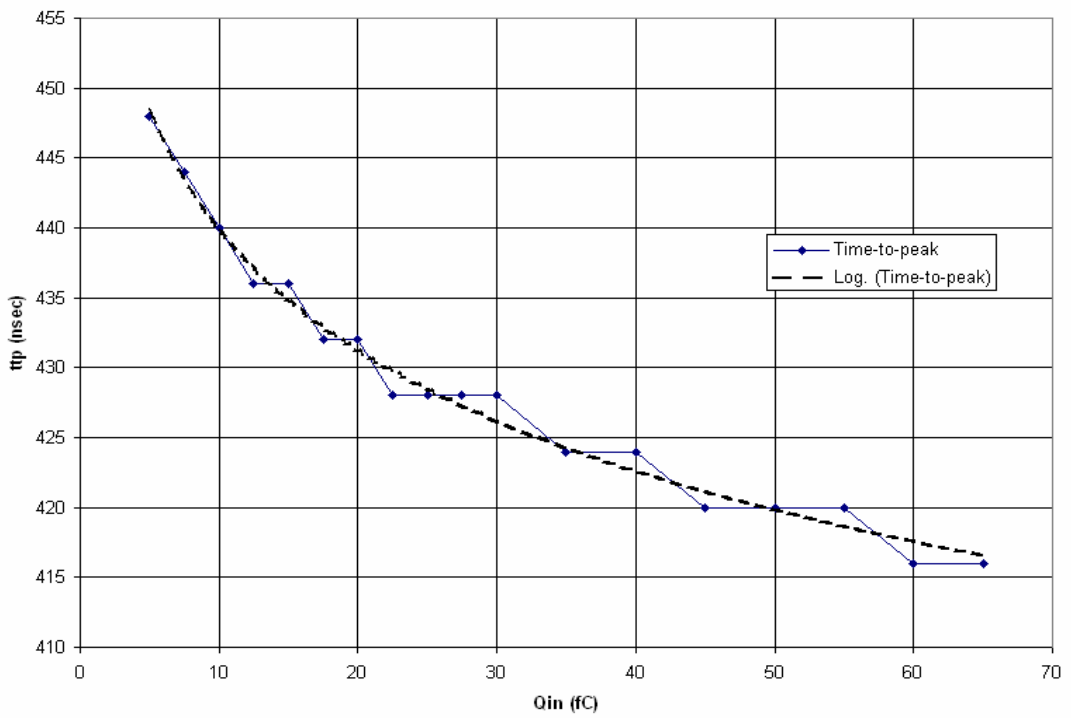

Figure 4-4 - Shaper time-to-peak versus output amplitude

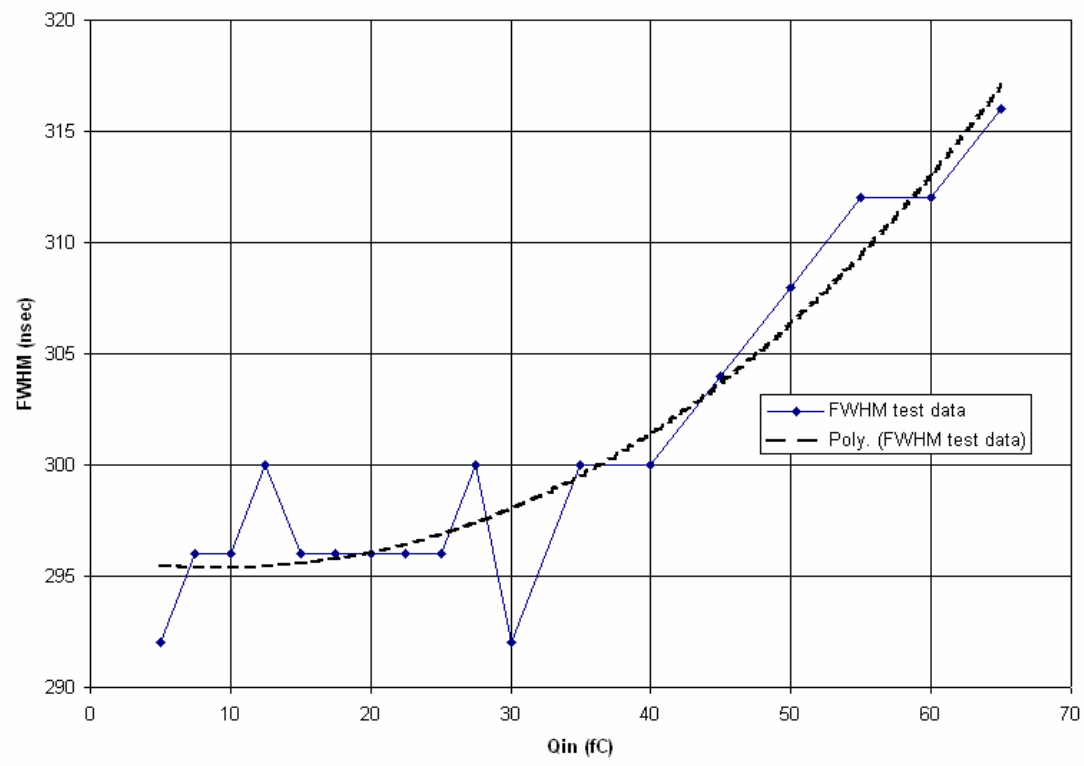

Figure 4-5 - Output shape FWHM vs. input voltage for C_{det} = 10 pF

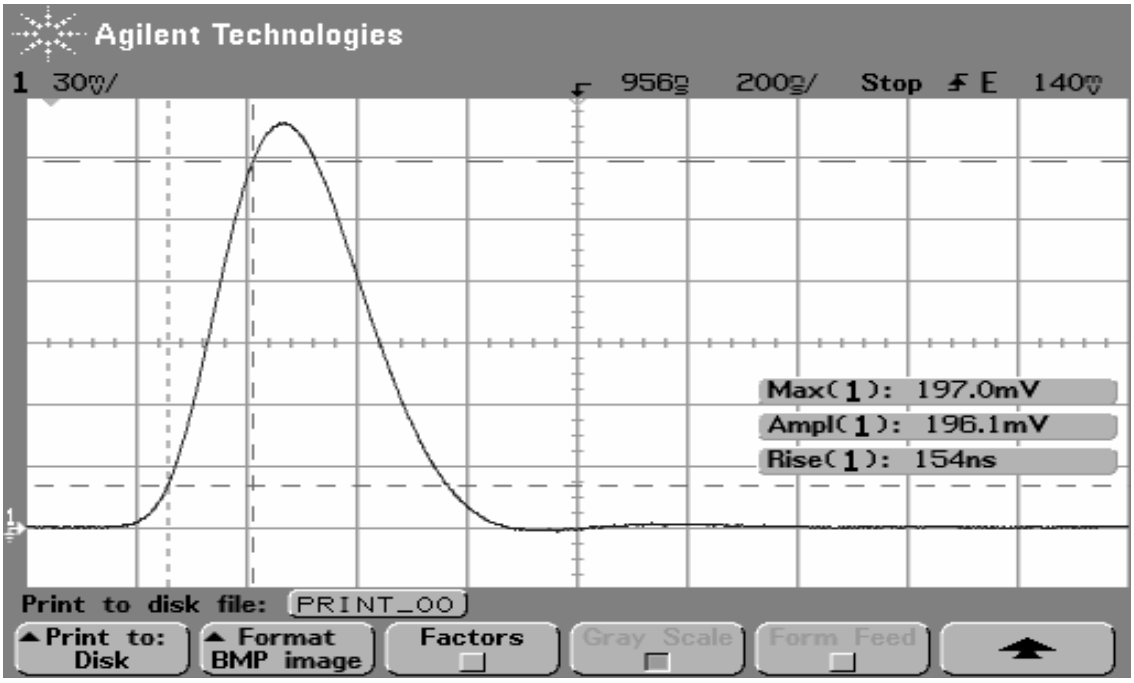

Figure 4-6 - Shaper output for large shaping time, full gain

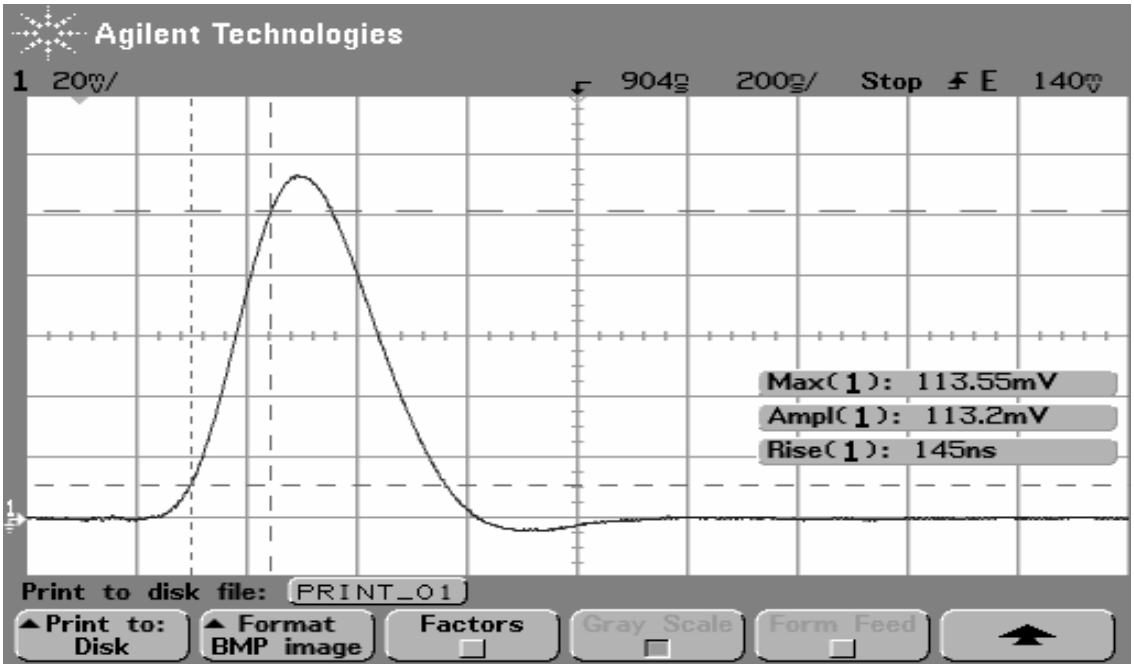

Figure 4-7 - Shaper output for large shaping time, half gain

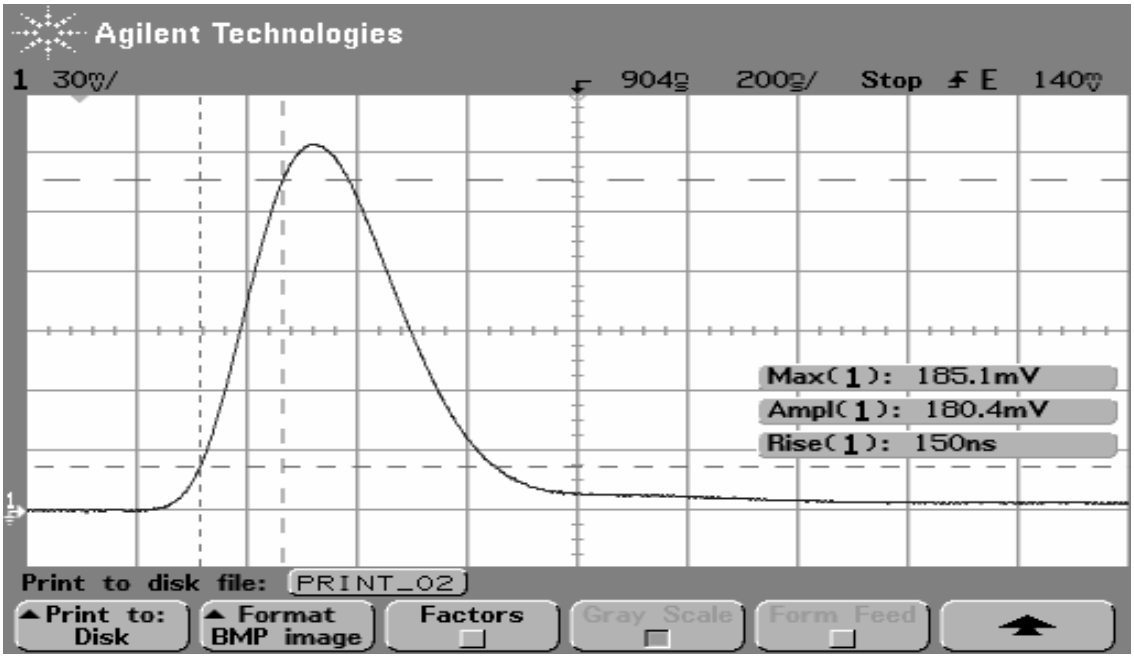

Figure 4-8 - Shaper output for small shaping time, full gain

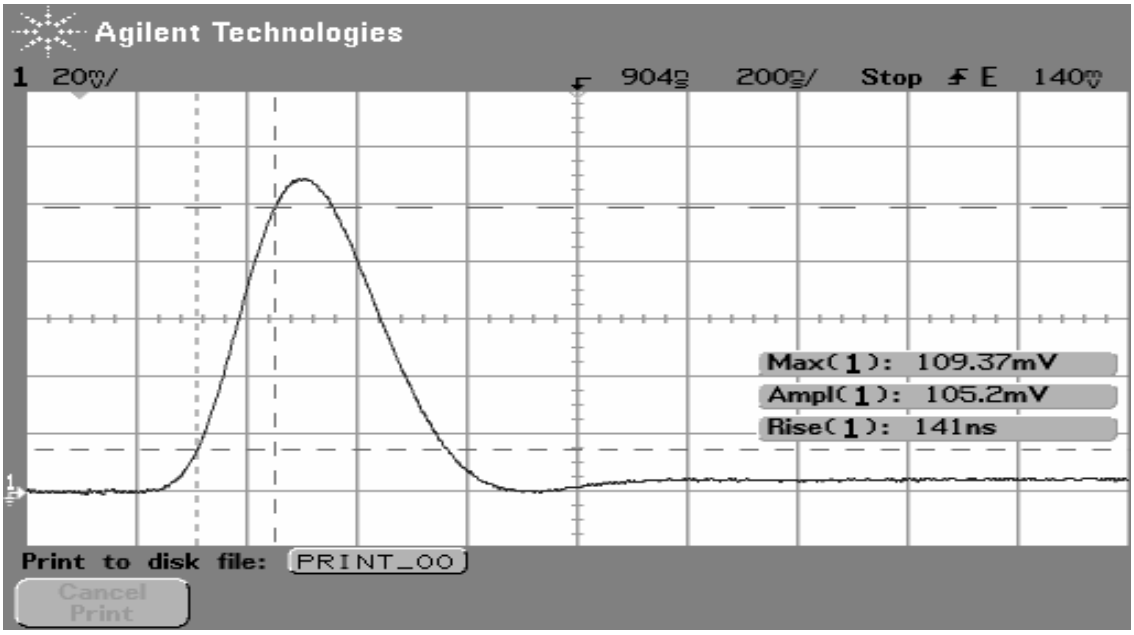

Figure 4-9 - Shaper output for small shaping time, half gain

Figure 4-10 shows the measured and simulated output noise voltage spectral densities (NVSD) for the shaper. Measurements were taken with the HP3589A spectrum analyzer. As can be seen from the plot, the simulated and measured curves have different voltage spectral density shapes. The blue trace is a fit of the square of the simulated NVSD scaled to be on the same order of magnitude as the measured NVSD, and its shape matches the measured results much more closely. There are doubts, at the present time, that the measured results are being interpreted correctly by the analysis software, mainly due to the need for a 50 Ω input resistance to the spectrum analyzer when the analyzer typically uses a 1 MΩ input resistance for calculations. This is being further investigated. However, the input-referred noise for the entire channel is better than the design specifications. Also, the ratio of the output noise measurements taken indicate that the shaper noise is indeed much less than the noise of the entire channel, indicating that the shaper noise meets the design specifications.

Most measurements taken regarding the baseliner restorer circuitry are simply tested with a multimeter. This is because the loop's main function is to set a DC level in the channel. As shown in Figure 4-11, the DC output level tracks almost perfectly linearly with a DC reference voltage input to the baseline restoration loop. This is no surprise, and indicates proper functionality well below and above the nominal baseline voltage of 110 mV. Note, however, the 15.7 mV offset present in this particular measurement.

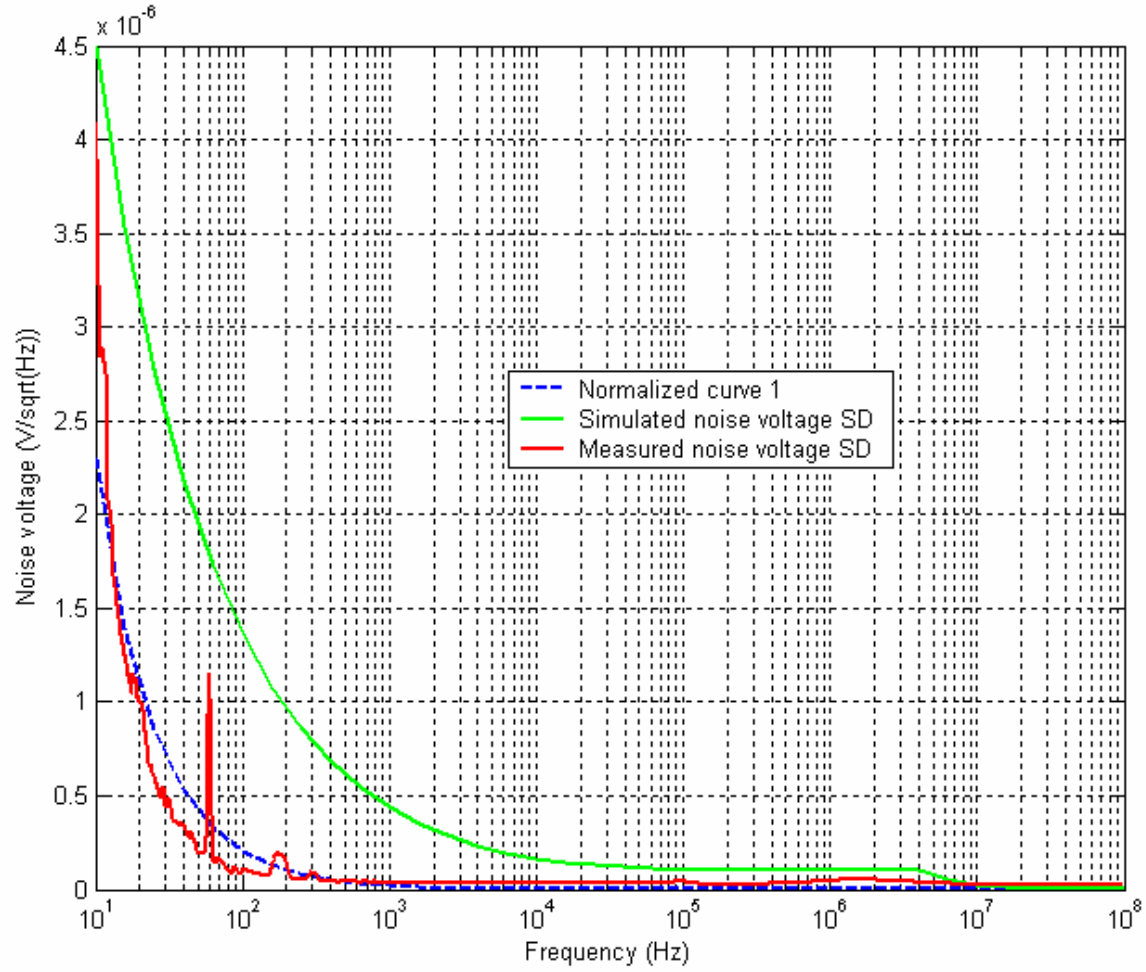

Figure 4-10 - Shaper output noise

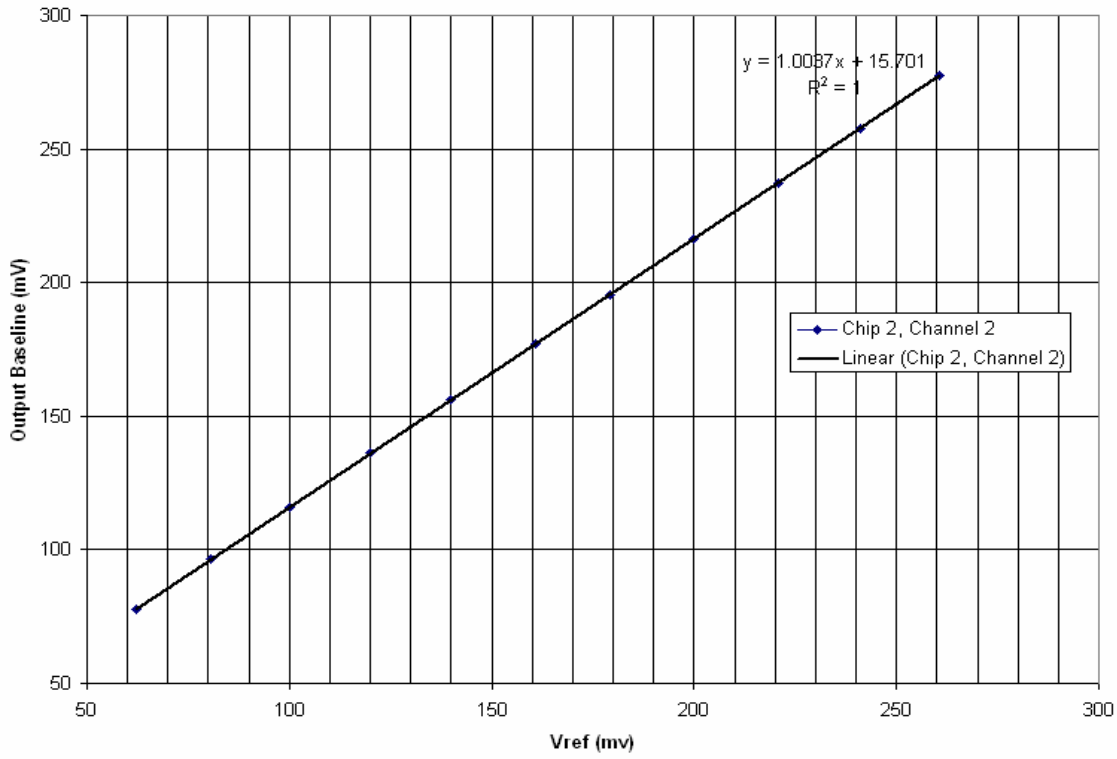

Figure 4-11 - Baseline voltage vs. Vref input voltage

This offset was not predicted in the pre-fabrication simulations performed. Further testing revealed that this offset was not only present in almost all channels, but also varied randomly across channels, as seen in Figure 4-12. It was hypothesized that these offsets were due to an insufficient loop gain.

In order to test this hypothesis, the bias current in the BLR OTA was changed in several steps to have a lower value. Since all BLR OTA devices were in saturation, this provided a larger voltage gain, which in turn increased the loop transmission value. This also placed the BLR loop's bandwidth well below the original 10-kHz mark. As the loop transmission increased, the offset in each channel decreased – or stated differently – the outputs converged to a DC voltage. This DC voltage was not specifically the reference voltage, but instead the reference voltage summed with the systematic offset. These results are shown in Figure 4-13. The systematic offset is discussed at greater length in later sections.

Another interesting phenomenon that the BLR circuitry exhibited is shown in Figure 4-14. The offset voltage is correlated to the real pole amplifier reference voltage. This phenomenon is still being investigated.

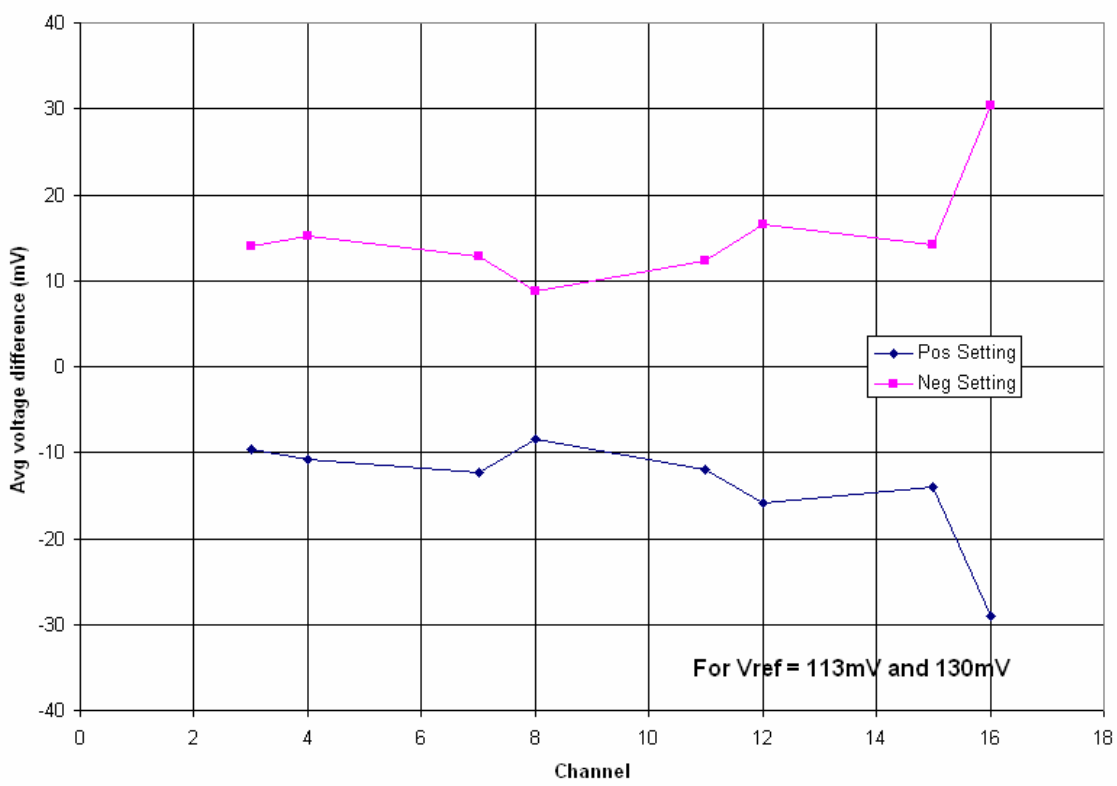

Figure 4-12 - Average BLR loop offset for all chips versus channel

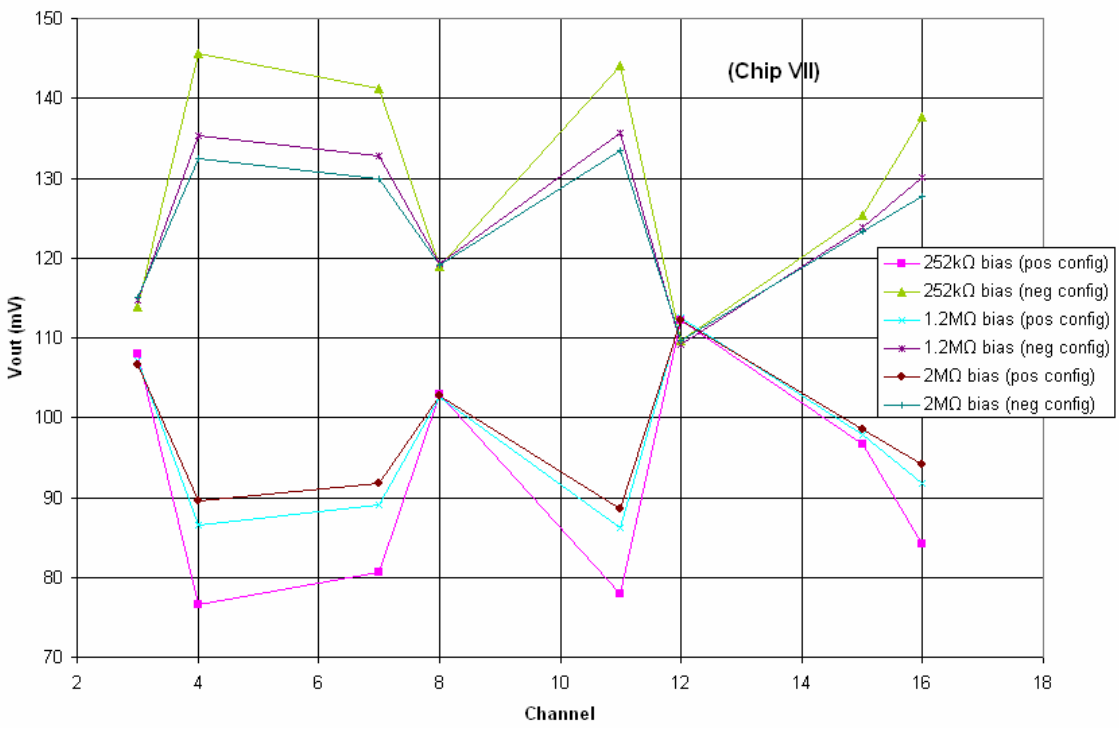

Figure 4-13 - Baseline offset over channel for different BLR OTA bias currents

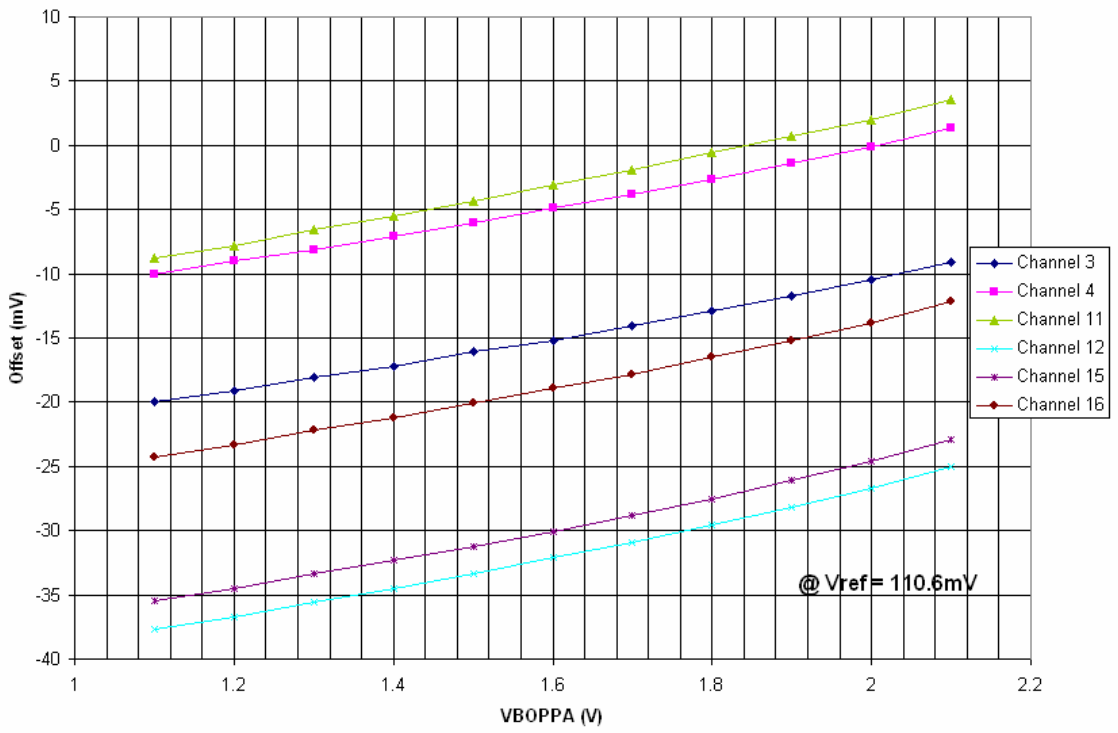

Figure 4-14 - Baseline offset vs. real pole amplifier reference voltage

4.3) Full Channel Results

Shown in Figure 4-15 is the overall system response to an input pulse when the channel is set up in its optimum configuration. One can see that the shape is very close to the designed response, with a FWHM of approximately 270 nsec and a 1%-to-1% pulse width of a little over 700 nsec, which satisfactorily accomplishes the 1-μsec pulse-pair resolution time design goal set by the SNS system.

System linearity was found to be extremely favorable. Recall from prior discussion that the channel is expected to become dynamic at higher signal levels due to the pulse shape dependence on the g_m of the NMOS follower in the complex-conjugate circuitry. However, it is still important that the system remain linear from very low signal levels until well past the threshold 'hit-level'. Figure 4-16 shows that the system non-linearity does indeed increase past 30 fC of input charge, but is negligible through the threshold level range.

Overall system noise measurements show that the noise specification was properly achieved. As shown in Figure 4-17, the measured noise in RMS electrons was actually below the simulated noise for all expected values of detector capacitance, C_{det}. This is a rare occurrence in integrated circuit design, but is probably due to the fact that the HSpice simulator and noise models were used in this design. This noise model is adequate for simple designs in strong-inversion saturation, but large deviations are seen as devices move to the limits

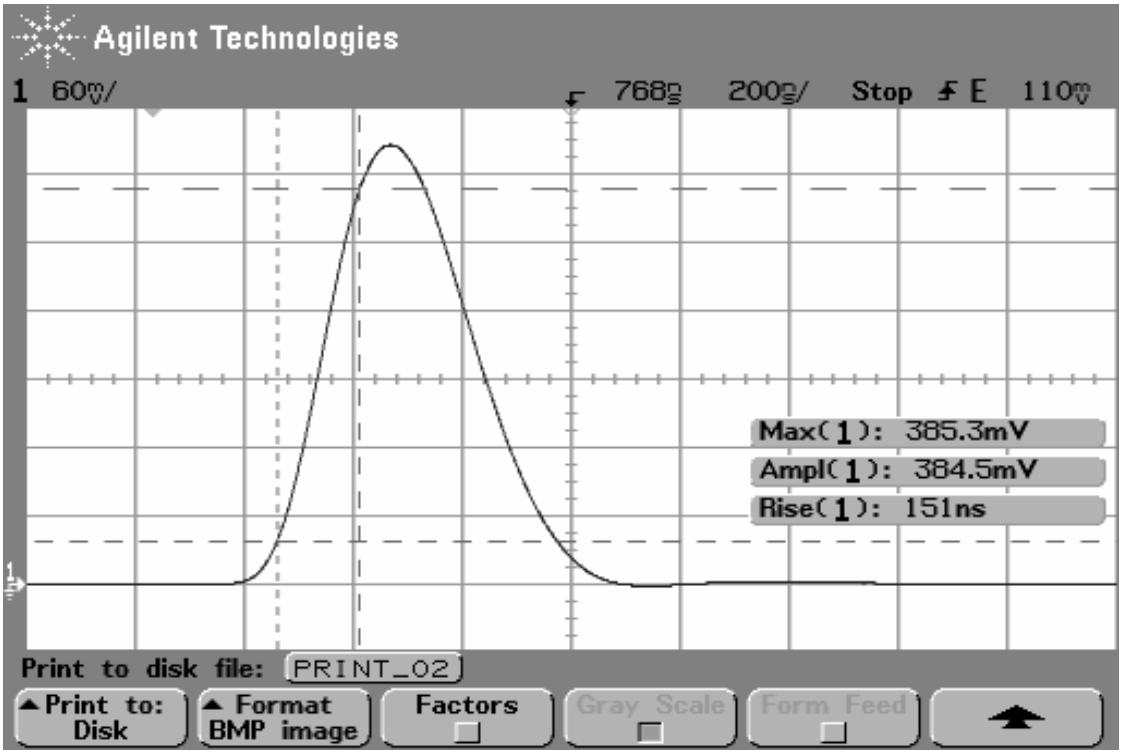

Figure 4-15 - System response to input pulse (system optimized)

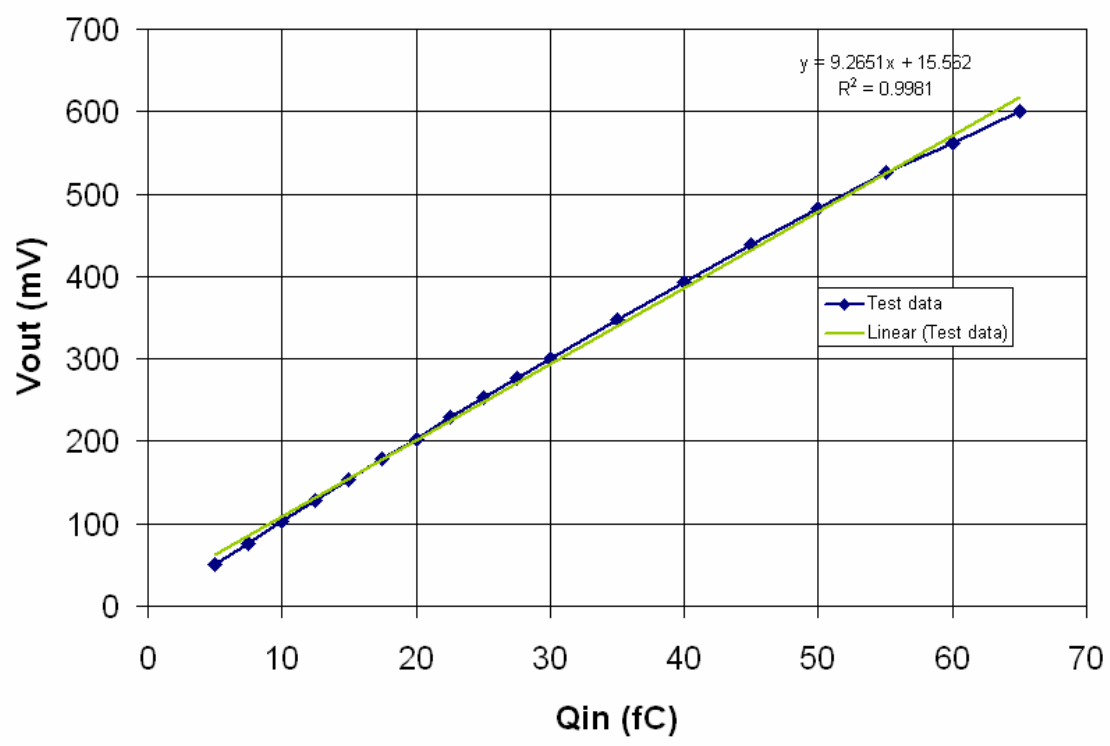

Figure 4-16 - Overall linearity (C_{det} = 10pF)

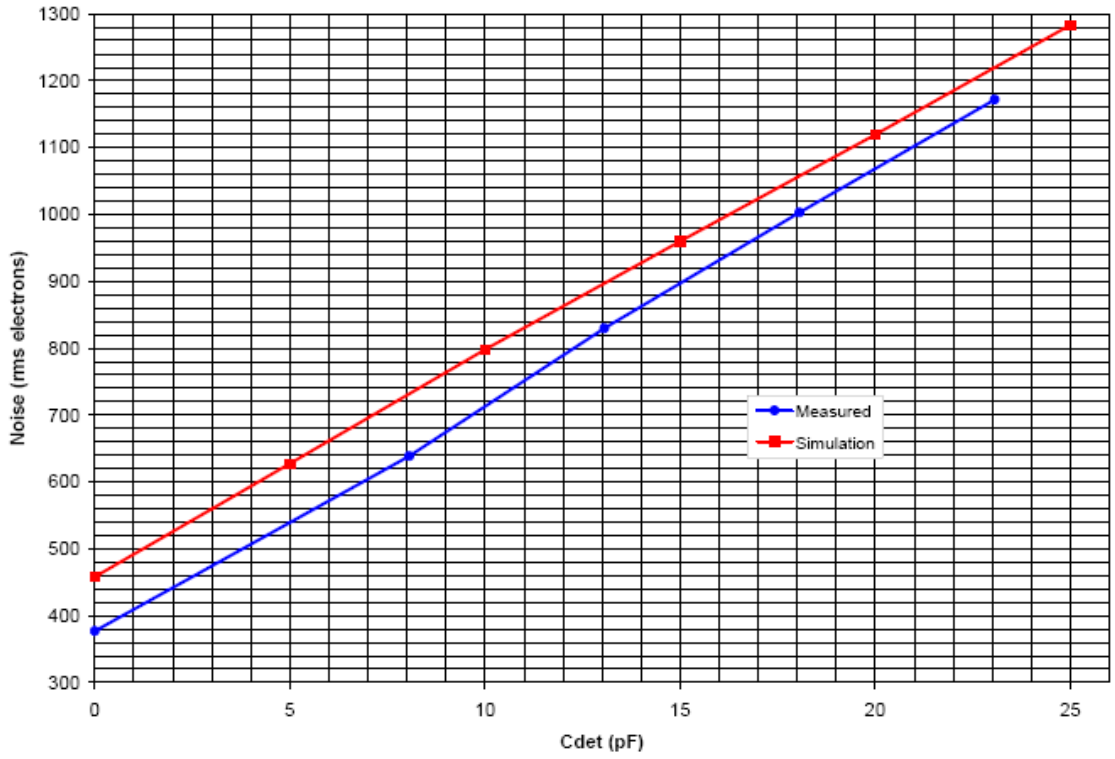

Figure 4-17 - Channel input noise versus detector capacitance [9]

and out of this operating region (e.g., the NLEV=3 model sometimes predicts NO NOISE at all in weak inversion!). Considering the measured results, the preliminary goal of input noise < 1000 RMS electrons was easily achieved. At 0 pF detector capacitance, the input referred noise is approximately 380 RMS electrons, while 1000 RMS electrons is not reached until C_{det} = 18 pF, which is beyond the expected maximum detector capacitance of 15 pF.

Overall system gain in mV/fC is shown in Figure 4-18. This gain is approximately what was expected. However, *Patara* displayed some variations across channels for a given chip. Part of this is likely due to the test setup. Since the front-end is charge-sensitive, any variation in capacitance of the leads or board traces (intended or parasitic) will affect the gain. For instance, if the added C_{det} for all channels is 5 pF, and one channel has 1 pF of parasitic capacitance on the testboard while another channel has 1.5 pF of parasitic capacitance due to trace length, the pulse gain will vary by 8% between channels. Monte Carlo simulations will be performed prior to submission of the next chip to determine if any significant variation in gain could be due to mismatch in certain devices.

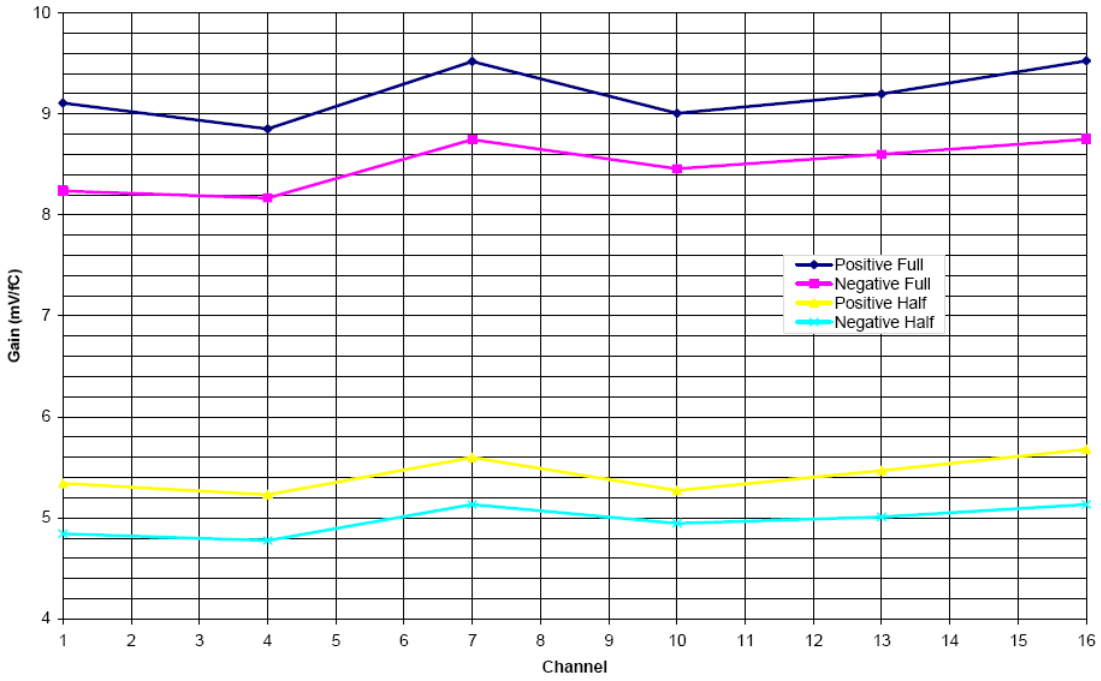

Figure 4-18 - System gain over same-chip channel [9]

4.4) Problems

Only one significant problem was found during the testing of the *Patara* prototype shaper system. In an effort to keep the bandwidth set by the BLR OTA and hold capacitor low for stability reasons, the OTA's transconductance was reduced significantly by using fractional mirror ratios to the output stage. However, since the rest of the OTA topology was left unchanged, this also reduced the voltage gain of the amplifier. Therefore a small, but acceptable, systematic offset between the actual baseline voltage and the reference was introduced due to a diminished loop transmission. Unfortunately, the effects due to physical device mismatch were also enhanced by the low loop gain of the BLR loop so that the offset varied widely (and randomly) from one channel to the next, as shown in the

measurements presented earlier. This problem probably would have been found prior to fabrication if Monte Carlo simulations had been performed. The effects of this problem are enhanced by the BLR OTA's place in the loop, since any voltage difference at the OTA's input directly affects output voltage. Fortunately, this offset is the only appreciable effect due to the low loop gain, as basic functionality and stability are acceptable.

This has already been corrected for the next phase on the *Patara* 2 chip. Recognizing the voltage gain is too low, but that it is undesirable to increase g_m, we are forced to raise r_{out} of the BLR OTA. This is achieved by using a cascoded output stage. Simulations indicate that the loop gain has been significantly increased and that the systematic offset is now less than 1 mV. Further, the layout has been modified so that the critically-matched devices are not only in a common-centroid configuration, but gate-aligned as well. Figure 4-19 shows the updated topology.

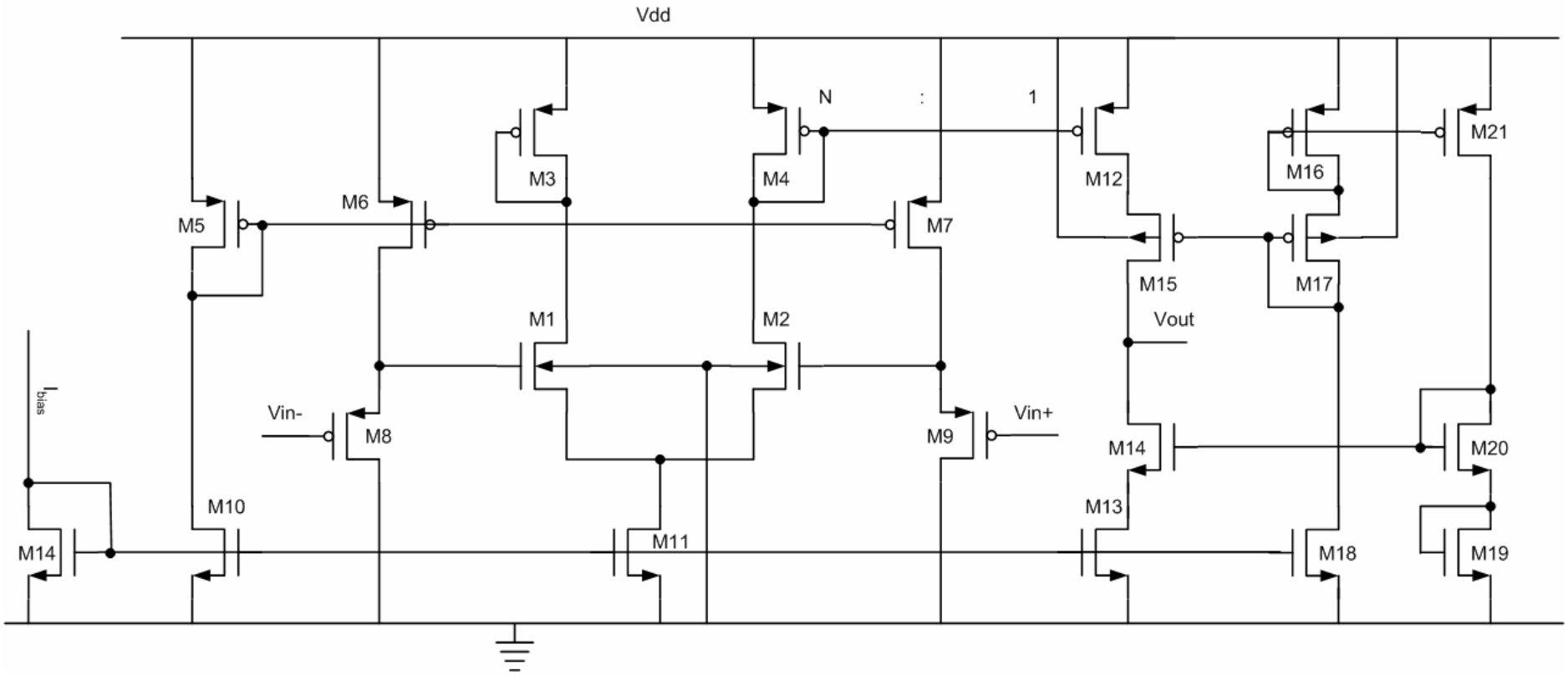

Figure 4-19 - BLR OTA topology with increased output resistance for use in *Patara 2*

Chapter 5

Conclusions

5.1) Conclusion

Patara represents the first ASIC developed for the Spallation Neutron Source at the Oak Ridge National Laboratory. Its low noise and high incident count rate make it ideal for use with high-efficiency neutron detectors such as HENDA. The *Patara* chip was fully functional on first-pass silicon. The system achieved an input-referred noise of less than 400 RMS electrons, which was better than simulations predicted. All shaper blocks worked as expected, as well. Midband shaper gain matched simulations very closely, producing a maximum voltage gain of 15 dB, also indicating that the OTA's transconductance was approximately 490 μS. The output waveform matched the intended response extremely well, with slight variations due to on-chip mismatch and a non-ideal input signal to the shaper stage. Each channel had an approximate power dissipation of 3.7 mW, with the shaper contributing 2.1 mW. One problem found during testing was random variations in the baseline restoration circuit's DC offset voltage over channel number. Although the BLR circuit tracked the input reference voltage correctly, the offset could cause problems once the comparator and proceeding circuitry are added. This was determined to be caused by an insufficient loop gain, and has been corrected for the submission of *Patara 2*.

5.2) Future Work

The circuitry reported in this work is limited to the analog front-end of the signal detection and processing chain. What remains is the digital post-processing components that will discriminate true 'hits' from signals below the threshold level and evaluate the results, as well as present the results to the SNS standard interface. This will allow the *Patara* chip to be a truly custom system on a chip (SOC). Also, some on-chip bandgap voltage reference circuits will be added, as well as several digital-to-analog blocks in order to make some of the system's internal reference voltages accurately programmable from remote locations. In early 2007 the chip *Patara 2* will be submitted, which will include the above circuitry and will be expanded to 64 channels. It will then be mated to the HENDA detector and tested at the SNS facility.

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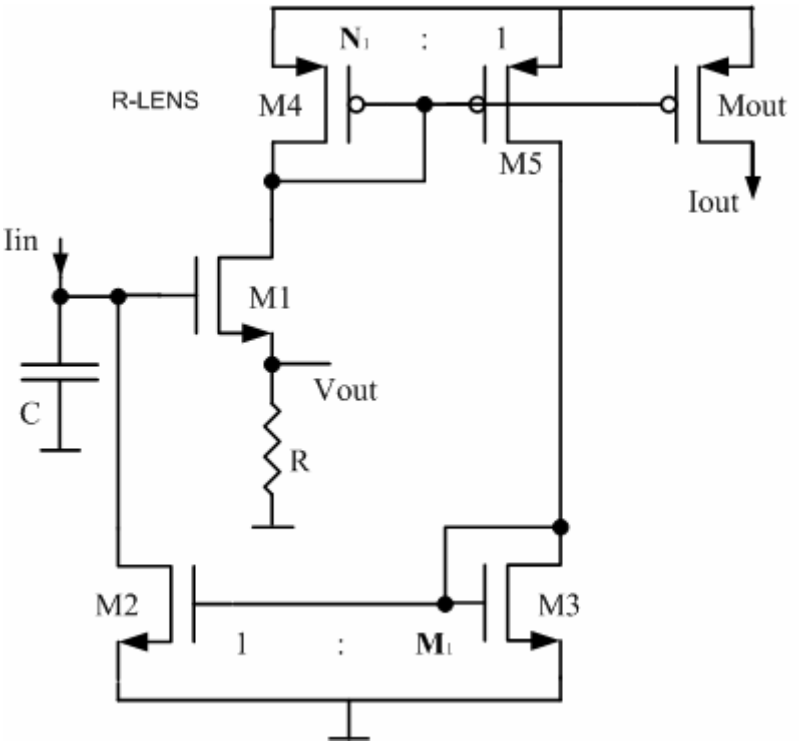
Appendix A

Derivation of R-Lens Transfer Function



Assuming an ideal follower M1, small-signal operation can be solved as

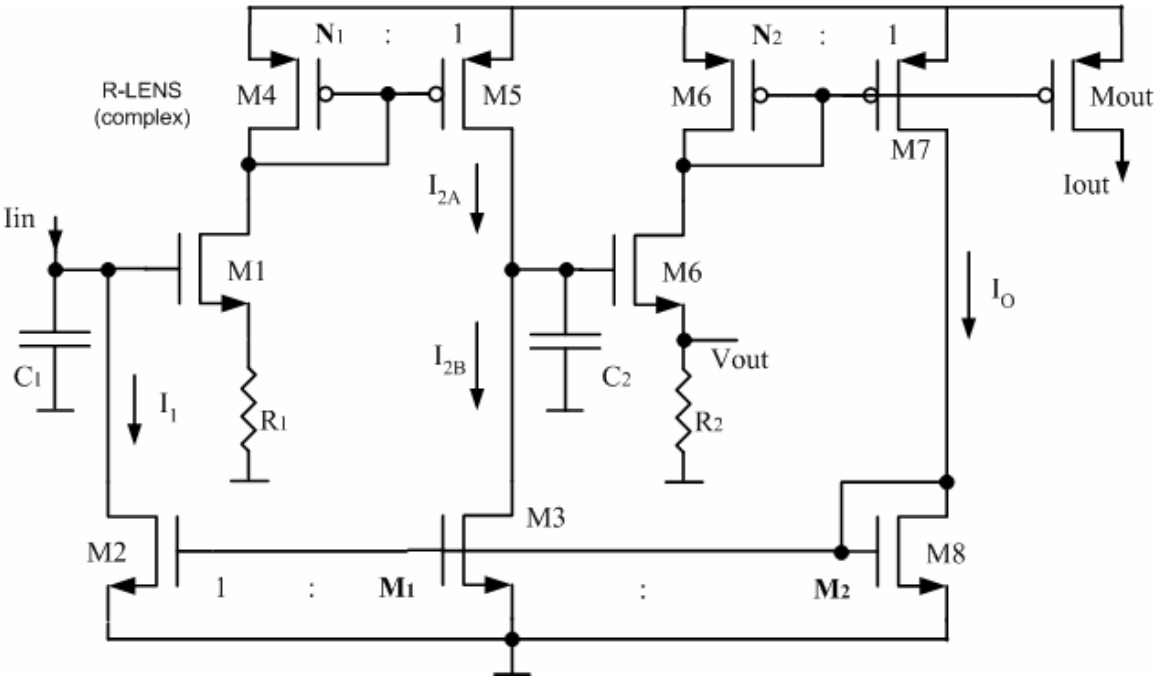
$$I_{in} = \frac{V_{out}}{1/sC} + \frac{V_{out}}{M_1 N_1 R} \qquad \text{A-1}$$

$$\frac{V_{out}}{I_{in}} = Z(s) = \left(\frac{1 + M_1 N_1 RsC}{M_1 N_1 R} \right)^{-1} = \frac{M_1 N_1 R}{1 + sCM_1 N_1 R} \qquad \text{A-2}$$

$$I_{out} = \frac{V_{out}}{N_1 R} \qquad \text{A-3}$$

$$\frac{I_{out}}{I_{in}} = H(s) = \frac{M_1}{1 + sCM_1 N_1 R} \qquad \text{A-4}$$

Derivation of Complex R-Lens Transfer Function



Defining the branch currents,

$$I_1 = \frac{V_{out}}{N_2 R_2 M_2}; \quad I_{2A} = \frac{V_{in}}{N_1 R_1}; \quad I_{2B} = I_o \frac{M_1}{M_2} = \frac{V_{out} M_1}{N_2 R_2 M_2}; \quad I_o = \frac{V_{out}}{N_2 R_2} \qquad \text{A-5}$$

the following node voltage equations are written:

$$V_{in} = (I_{in} - I_{2B}) \frac{1}{sC_1} = \left(I_{in} - \frac{V_{out}}{N_2 R_2 M_2} \right) \frac{1}{sC_1} \qquad \text{A-6}$$

$$V_{out} = (I_{2A} - I_{2B}) \frac{1}{sC_2} = \left(\frac{V_{in}}{N_1 R_1} - \frac{V_{out} M_1}{N_2 R_2 M_2} \right) \frac{1}{sC_2} \qquad \text{A-7}$$

Now, solving the equation above for V_{IN} and equating, we have

$$\left(sC_2V_{out}+\frac{V_{out}M_1}{N_2R_2M_2}\right)N_1R_1=V_{in}=\left(I_{in}-\frac{V_{out}}{N_2R_2M_2}\right)\frac{1}{sC_1} \quad \text{A-8}$$

Rearranging in terms of I_{in} and V_{out},

$$I_{in}=V_{out}\left(s^2N_1R_1C_1C_2+s\frac{M_1N_1R_1C_1}{M_2N_2R_2}+\frac{1}{M_2N_2R_2}\right) \quad \text{A-9}$$

$$Z(s)=\frac{V_{out}}{I_{in}}=\frac{M_2N_2R_2}{s^2N_1R_1C_1M_2N_2R_2C_2+sM_1N_1R_1C_1+1} \quad \text{A-10}$$

$$H(s)=\frac{Z(s)}{N_2R_2}=\frac{I_o}{I_{in}}=\frac{M_2}{M_2s^2\left(N_1R_1C_1\right)\left(N_2R_2C_2\right)+M_1s\left(N_1R_1C_1\right)+1} \quad \text{A-11}$$

Assuming $M_1 = M_2 = 1$, this leaves

$$H(s)=\frac{I_o}{I_{in}}=\frac{1}{s^2\left(N_1R_1C_1\right)\left(N_2R_2C_2\right)+s\left(N_1R_1C_1\right)+1} \quad \text{A-12}$$

Vita

Jonathan Lanier Britton (Lanie) was born in Maryville, TN on January 16, 1982 to Charles and Carol Britton. He was raised in Louisville, TN and then Alcoa, TN, where he graduated from Alcoa High School in 2000. Lanie entered the University of Tennessee that fall to pursue a degree in Electrical Engineering. While an undergraduate, he had the opportunity to intern with the Instrumentation & Controls Division at Oak Ridge National Laboratory, as well as consult with Concorde Microsystems, Inc. He was also an undergraduate research assistant in Dr. Benjamin Blalock's research group, which coincided with his undergraduate focus on analog circuit design. Lanie graduated with a Bachelor's Degree from UT in May 2004, *Summa Cum Laude*.

In the fall of 2004, he entered into the Master of Science program at the University of Tennessee, receiving the T. Vaughn Blalock Memorial Graduate Scholarship. During this time he was graduate teaching assistant to Dr. Blalock, and then a graduate research assistant in Dr. Blalock's research group, the Integrated Circuits and Systems Laboratory (ICASL).

After completing his Master's degree, he will be working with Texas Instruments in the Portable Power Management group in Knoxville, TN.