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Design of a Noise Measurement System for CMOS Transistors

Presented By:
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In fulfillment of the University Honors senior project

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Abstract

One of the fundamental limitations on all analog electronics circuits is the noise generated by the individual transistors. This project is a design of a system to allow laboratory measurements of the noise output by MOSFET transistors, of either N-channel or P-channel devices. The system currently extends frequency response to roughly 10 MHz with the possibility of a higher bandwidth amplifier easily extending this much farther. In addition, the system allows the tester to easily and accurately set the bias current flowing in the test transistor, helping to show the effects of changing the transconductance.
Introduction:

As we continue to scale electronics to ever smaller feature sizes, we are encountering many effects that make analog circuit design more difficult. One of the fundamental goals of any analog circuit is to achieve a sufficiently high signal-to-noise ratio, in order to allow the largest possible dynamic range in our signal processing. A basic consequence of shrinking feature sizes is a reduction in operating voltage. Many of the modern deep-submicron processes in use have pushed supply voltage to near 1 V, while the thermal noise produced by transistors fundamentally remains constant, which causes an inherent limitation in the maximum signal-to-noise ratio attainable.

In addition to thermal noise, all transistors exhibit a phenomenon known as 1/f noise, in which the noise contribution at the lower frequencies is much larger than that predicted by the thermal noise theory. This noise is given the name 1/f noise because it roughly rolls off proportionally to the inverse of the frequency, until it becomes covered entirely by the thermal noise, which is constant over frequency. We are finding that the deep-submicrometer transistors have 1/f noise power extending to ever higher frequencies because the gate area is correspondingly shrinking.

To be able to accurately design circuits around the effects of noise, it is important to be able to measure both the effects of the 1/f noise and the thermal noise. In addition, the input referred noise contribution of a transistor is strongly associated with the way in which it is biased, so in order to be able to accurately predict the noise performance, we must be able to measure it over a wide range of bias currents [1, 2].

This project proposes a system for measuring the noise from a transistor and includes both a bias circuit and a low-noise amplifier to provide some gain for allowing easy measurement of the noise. This system is particularly flexible, making it easy to set a current in the transistor to any amount desired, from the nanoampere through the milliampere range, allowing measurements to be made in the weak, moderate, and strong inversion regions. In addition, the choice of amplifier can be changed to provide the desired frequency response and noise characteristics to match the needs of the test.
MOSFET Noise Fundamentals

The noise components in all CMOS transistors includes both a thermal noise component, which is constant over frequency, and a 1/f noise component, which will roll off proportional to the inverse of the frequency. Thermal noise is present in all transistors (and resistors), and is caused by the random motion of free charges due to the thermal energy of the system. 1/f noise is present in many devices that contain a DC current, including CMOS devices, which have been observed to have energy as high as 10 MHz.

The typical method in which we consider noise in transistors is as an equivalent voltage referred to the gate of the device. Although we could consider the noise at any point, it is most convenient for circuit analysis and design to consider it referred as a gate voltage. In a CMOS transistor, this noise can be described by

\[ e_{DUT} \left( \frac{V}{\sqrt{Hz}} \right) = \frac{8kT}{3g_m} + \left( \frac{K_a}{C_{ox}W/L} \right) \left( \frac{1}{f} \right) \]  

where the first term describes the thermal noise in the transistor and the second term describes the 1/f noise contribution.

The \( k \) in the first term of (1) is Boltzmann's constant, \( T \) is the absolute temperature, and \( g_m \) is the test device's transconductance. The \( K_a \) value used in the second term of (1) is process dependent, \( W \) and \( L \) are the gate width and length, respectively, and \( C_{ox} \) is the gate capacitance per unit area [1]. These equations demonstrate the frequency characteristics of the different forms of noise, as well as illustrating the importance of the bias of the device to the thermal noise characteristics.

The frequency at which the 1/f noise begins to be buried in the thermal noise is referred to as the corner frequency, and is described in [1] as

\[ f_c = \left( \frac{K_a}{C_{ox}W/L} \right) \cdot \frac{g_m}{4kTn} = \left( \frac{K_a}{2C_{ox}L} \right) \cdot \sqrt{\frac{\mu_a}{kT}} \]

By this, the corner frequency will tend to increase if either \( L \) is decreased or \( I_d \) is increased, reinforcing the need for measurements over a wide range of bias currents.
Design Considerations

In designing this system, I went through several possible designs. At first, I was considering methods of having the drain of the test transistor DC coupled to the input of the amplifier. This way, the drain voltage of the test transistor could be set by the negative feedback action of the amplifier. I was also attempting to use a low frequency feedback loop to set the gate voltage such that the proper drain current would flow through the test transistor.

In practice, I discovered several problems with this arrangement. For one, because the amplifier is not an ideal amplifier, it was extremely difficult to get around the problems of offset voltage and input bias current, which made setting the current in the test transistor at low levels very difficult and inaccurate. Secondly, using relatively large currents through the test transistor required limiting the size of the feedback resistor, because the test transistor current was forced to flow through it. When large currents flow, the voltage drop across the resistor becomes very large and runs a significant chance of exceeding the maximum output voltage of the amplifier.

Another possibility I considered involved using a differential pair as the test transistor connected to an open-loop op-amp, with global feedback from the output to the input of one side of the pair. Although this gave the advantage of allowing the gain to be easily set by the feedback network, it was not without its problems. One issue is that requiring a differential pair limits the applicability of the system, because many of our current chips have only single test transistors. In addition, the gain from the differential pair becomes extremely low when a low current is used, making the feedback somewhat difficult to control.

The option I settled on is AC coupled from the drain of the test transistor to the input of a transimpedance amplifier. Among the issues that led me to this solution were a desire for independent control over the test transistor's drain current and a desire to separate the test transistor from the amplifier's characteristics such as input bias current and offsets. I also like the inherent simplicity in the circuit, which makes it much simpler to use and to diagnose problems should it fail to operate as expected.

AC coupling the drain to the amplifier is not without its penalties, of course. For
one, the coupling capacitor must be carefully chosen to not interfere with the frequency response in the desired range. For another, the circuit loses the ability to use feedback to control the drain voltage in the test transistor, forcing other methods of controlling the bias.

Description of Measurement Circuit

![Schematic of noise measurement system.](image-url)

After careful consideration, I finally settled on the circuit shown in Figure 1. By effectively grounding the gate of the test transistor through the 50 ohm resistor and applying a current source between the source and $V_{SS}$, the $V_{gs}$ voltage can be set appropriately by varying the current. Tying a resistor between $V_{DD}$ and the drain of the test transistor allows us to simultaneously set the $V_{ds}$ voltage as well as controlling the frequency characteristics of the amplifier. In order to avoid allowing source degeneration to effectively kill the gain of the test transistor, a sufficient amount of bypass capacitance must be applied at the source node.

The amplifier section is comprised of the Analog Devices AD8065 operational amplifier. This op-amp was chosen for its high gain-bandwidth product and excellent noise characteristics. The gain-bandwidth product of 145 MHz allows sufficient bandwidth that the overall frequency response of the system can be extended to nearly 10
MHz, which helps facilitate accurate measurement of the 1/f noise corner frequency. The input referred voltage noise of this op-amp is approx. 7 nV/√Hz, which, though not as low as some, is sufficiently low for this purpose. The input referred current noise, on the other hand, is an exceptionally low 600 aA/√Hz, which will significantly help to reduce the overall noise output from the system.

The amplifier is configured as a transimpedance amplifier, with the feedback resistor forcing the inverting terminal of the amplifier to a low impedance, allowing the noise current from the test transistor to be converted to a noise voltage. The selection of this resistor can aid in both setting the frequency characteristics of the amplifier as well as the gain.

**Hand Analysis of System**

The overall output noise from the system can be calculated at midband by analyzing the individual noise generators and adding the squares of their contributions, as described in [3]. This can allow us to gain some insight into the particular design requirements, telling us which factors are likely to be the most important.

The first equation to note in this analysis is the gain of the system from the gate of the test transistor to the output, which can be described as

$$A_v = g_m \cdot R_f.$$  \hspace{1cm} (3)

When (1) is multiplied, we see the output noise of the test transistor is

$$e_{\text{out}}^2 \left( \frac{V}{\sqrt{\text{Hz}}} \right) = \frac{8 \cdot k \cdot T \cdot R_f}{3} + \frac{K_a \cdot g_m \cdot R_f}{C_{ox}^2 \cdot W \cdot L} \left( \frac{1}{f} \right),$$  \hspace{1cm} (4)

suggesting that the feedback resistor should be made large to maximize the amount of noise from the test transistor in the output.

We can assume that the noise from the feedback resistor is negligible, because it couples directly to the output and thus does not experience any gain in the system. The noise from the drain resistor will be present at the output, however, and is most easily calculated using the noise model with a current source in parallel with the resistor. By the nature of the amplifier, the noise at the output from this configuration will be the current noise multiplied by the feedback resistor,
so the drain resistor should be made relatively large to minimize this effect. In addition, there will be a noise output from the 50 ohm resistor at the gate of the transistor, but this noise should be negligible due to the small value of this resistance.

The noise due to the op-amp will be its input-referred noise voltage multiplied by the equivalent non-inverting gain of the amplifier system, which, assuming that $r_o$ of the test transistor is large, will be dominated by the feedback and drain resistors, yielding

$$e_{\text{op-amp}} \left( \frac{V}{\sqrt{Hz}} \right) = \frac{e_{\text{op-amp}}}{R_d} \left( \frac{R_f}{R_d} + 1 \right)$$

which further reinforces the need for $R_d$ to be relatively large. The noise due to the input referred current noise in the op-amp, like the noise from the drain resistor, will be multiplied by the feedback resistor, for

$$e_{\text{n,op-amp}} \left( \frac{V}{\sqrt{Hz}} \right) = i_{\text{n,op-amp}} \cdot R_f.$$

Because we want the feedback resistor to be large to increase the noise contribution from the test transistor, this illustrates the importance of minimizing the input noise current of the amplifier, which was a major design consideration in the selection of the devices.

The total output noise can be found by adding the squares of each of (4-7). Each of these values will be in volts squared per hertz, so by taking the square root of the resulting number will arrive at the total output noise in the more-useful volts per root hertz. Finally, this value can be referred back to the input of the system by dividing by the overall gain, found in equation (3).

**Simulation Results**

I have simulated this system using Hspice to verify its operation and performance specifications. During simulations, I have found that the ideal values for the feedback resistor and drain resistor are 10 kΩ and 1 kΩ, respectively. These values were chosen as a compromise between good noise performance and bandwidth. While there is a slight amount of overshoot in the frequency response at low current levels, this is corrected in
calculating the input referred noise by dividing the output noise by the actual gain.

One benefit of this system is the ability to test the output noise from the amplifier with the test transistor removed. In this test, the drain resistor is connected to both the coupling capacitor to the amplifier and the current source. By being able to measure the output noise without the test transistor, I am able to determine that the device under test dominates the noise, rather than the amplifier. Experimentally, once the output noise from the amplifier is found, it can be subtracted from the noise generated with the test device, giving a more accurate test.

In addition, the input referred noise voltage starts to decrease at higher frequencies. This appears to be due to the gain rolling off before the noise bandwidth begins to roll off. This further illustrates the importance of a high bandwidth amplifier in making this measurement. Figures 2-9 demonstrate the performance of the system in simulation.
Figure 2: Gain in dB from gate to output. Lowest curve is with \( I_{\text{bias}} = 10\mu A \), increasing in decades to 100\( \mu \)A. Frequency range is from 10 Hz to 1 GHz.

Figure 3: Gain in dB from gate to output. Lowest curve is with \( I_{\text{bias}} = 10\mu A \), increasing in decades to 1 mA. Frequency range is from 10 Hz to 1 GHz.
Output Noise of Amplifier Only with $R_f=100k\Omega$, $R_d=10k\Omega$

Figure 4: Output noise when test transistor is removed, indicating noise from amplifier alone. Frequency range is from 10 Hz to 1 GHz.

Output Noise of Amplifier Only with $R_f=10k\Omega$, $R_d=1k\Omega$

Figure 5: Output noise when test transistor is removed, indicating noise from amplifier alone. Frequency range is from 10 Hz to 1 GHz.
Figure 6: Output noise with test transistor added back in, illustrating that test transistor is dominating the noise output. Highest curve is for $i_{bias} = 100\mu A$, in descending order, current decreases by decades to $10nA$. Frequency range is from $10 \text{ Hz}$ to $1 \text{ GHz}$.

Figure 7: Output noise with test transistor, illustrating that test transistor is dominating the noise output. Highest curve is for $i_{bias} = 1mA$, in descending order, current decreases by decades to $10nA$. Frequency range is from $10 \text{ Hz}$ to $1 \text{ GHz}$. 
Figure 8: Input referred voltage noise, illustrating 1/f noise and thermal noise. Highest curve is for \( i_{bias} = 10\, \text{nA} \); in descending order, current is increasing by decades to \( 100\, \text{uA} \). Frequency range is from \( 10 \, \text{Hz} \) to \( 10 \, \text{MHz} \).

Figure 9: Input referred voltage noise, illustrating 1/f noise and thermal noise. Highest curve is for \( i_{bias} = 10\, \text{nA} \); in descending order, current is increasing by decades to \( 1\, \text{mA} \). Frequency range is from \( 10 \, \text{Hz} \) to \( 10 \, \text{MHz} \).
bipolar amplifier to allow the system to operate into the hundreds of megahertz. Such a system would have enough bandwidth to facilitate accurate measurement of even the latest deep-submicrometer transistors, with their accordingly higher 1/f noise corner frequencies. Because of the simplicity of the circuit, such an amplifier would be able to be easily added, provided that it is of an inverting gain configuration. With the use of RF transistors, the system's bandwidth should be well above the highest corner frequencies found in current CMOS processes.
References

