Design Considerations for Paralleling Multiple Chips in SiC Power Modules

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I am submitting herewith a thesis written by Fei Yang entitled "Design Considerations for Paralleling Multiple Chips in SiC Power Modules." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Fred Wang, Major Professor

We have read this thesis and recommend its acceptance:

Leon M. Tolbert, Daniel J. Costinett

Accepted for the Council:

Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)
Design Considerations for Paralleling Multiple Chips in SiC Power Modules

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Abstract

With the benefits of fast switching speed, low on-resistance and high thermal conductivity, silicon carbide (SiC) devices are being implemented in converter designs with high efficiency and high power density. Consequently, SiC power modules are needed. However, some of the pre-established package designs for silicon based power modules are not suitable to manifest the advantages of SiC devices. Therefore, this thesis aims at optimizing the package design to utilize the fast switching capability of SiC devices.

First, the power loop parasitic inductance induced by the package can lead to large voltage spikes with the fast switching SiC device. It can potentially exceed the device’s voltage ratings and affect its safe operation.

Second, to achieve high power density design with SiC devices, the package’s cooling performance needs to be improved.

Third, to design a package for high current applications with multiple chips in parallel, a proper scaling method is needed to ensure all the devices undertake the same voltage stress in switching transients. For P-cell/N-cell designs with split scaling, a new parasitic parameter, namely, middle-point parasitic inductance $L_{\text{middle}}$ will be introduced. Its role should be understood.

Lastly, the unbalanced dynamic switching loss can lead to different state junction temperatures among paralleled devices. Thermal coupling can help to reduce the temperature imbalance, and its role should be quantitatively investigated.

To meet the first two requirements, a new package design is proposed with reduced parasitic inductance and double-sided cooling. Compared to a baseline package, more than 60% reduction of parasitic inductance is achieved.

The middle-point parasitic inductance’s effect on device’s switching transients is analyzed in the frequency domain. Then a dedicated power module is fabricated with the capability of
varying $L_{\text{middle}}$. Experiment results show that as $L_{\text{middle}}$ increases, different voltage stresses are imposed on the MOSFET and anti-parallel diode.

Electrothermal simulations are implemented to investigate steady state junction temperatures of paralleled devices considering unbalanced switching losses at different thermal coupling conditions. It is observed that both devices’ junction temperatures will increase as the coupling coefficient is increased. However, the junction temperature imbalance will decrease. This is verified by the experiment result.
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Chapter 1

Introduction

1.1 Background and Introduction

Power converters are widely used in various applications, e.g., industrial, aerospace, military, utility, and transportation. According to the 2012 Annual Energy Review DOE/EIA report [1], the power converters will transfer 80% of the electricity in 2030. Among those power converters, the power modules are especially used in high power applications because of their benefits of compact circuit design and integrated cooling.

1.1.1 Basic Structure of a Power Module

The power module package is the physical containment for several power semiconductor chips. It provides electrical connections, thermal conduction to heat sink, electrical insulation, and mechanical support. The basic structure for a single chip connection is shown in Figure 1.1.

Figure 1.1. The typical structure of a power module.
The chip, either Si or SiC based device, is soldered on the direct bonded copper (DBC) ceramic substrate. The DBC substrate has two layers of copper on the top and bottom side, and in the middle, is the ceramic material ($Al_2O_3$, $AlN$ or $Si_3N_4$). It conducts the heat generated by the chip to the cooling system and provides an insulation layer between the chip and the baseplate. Wire bond is typically used as the electrical interconnection between the top side of one chip and the other chips.

1.1.2 High Current Power Modules with Multiple Devices

The current rating of one device is usually determined by the device area. Considering the low yield rate in the wafer and thermal mechanical stress of the device, usually the device’s area is restricted. As a result, the current capability of a single chip is limited as well. Therefore, for high current power modules, multiple chips are paralleled to form one switch.

To be specific, a switch is realized in each substrate where the switching devices (IGBT or MOSFET) and their anti-parallel diodes are placed physically close to each together. They are laid-out on the same copper trace as they are at the same potential electrically. In fact, in most of the commercial DBC based high current power modules, multiple substrates of identical layout are paralleled as well in order to constitute one switch with high current ratings [2].

Once each switch is realized, wire bonds and other interconnection methods (ribbon wires, flexible PCBs or top DBCs) are used to realize the interconnection between different switches. In commonly used power modules, a phase leg configuration is formed where one switch is used as an upper switch and the other as a lower switch.

Figure 1.2 shows an example of a 1200V/300A module from Cree. Two identical substrates with the same layout construct the upper switch. Similarly, the lower switch is also composed of another two identical substrates. Then a phase leg configuration is realized with the aid of wire
bonds. All the substrates are soldered on the same baseplate, and only one cooling system is needed for the whole phase leg.

Figure 1.2. 1200V/300A SiC power module layout from Cree.

1.1.3 Parasitic Components of a Power Module and Their Impacts

In terms of the electrical connections, different packaging techniques are utilized to interconnect different chips to realize certain circuit topologies. However, as can be seen from Figure 1.2, these interconnections in the package will introduce some extra parasitic components, e.g., parasitic resistance, parasitic inductance, and parasitic capacitance.

All these parasitic components will affect the operation of the devices and circuits. For example, the parasitic resistance is undesirable as it will increase extra conduction losses during on-state. Therefore, the thickness of the direct bonded copper, the number, and gauge of wire bonds are all carefully selected in order to carry the desired current in package design.

The parasitic inductance, on the other hand, will affect the device’s operation during switching transients. Figure 1.3 illustrates three main parasitic inductances present in a typical
phase leg module. Namely, they are gate loop parasitic inductance $L_{gs}$, common source parasitic inductance $L_{cm}$ and power loop inductance $L_{ds}$.

![Diagram of a double-pulse test circuit](image)

*Figure 1.3. Parasitic parameters in a double-pulse test circuit.*

The gate loop parasitic inductance is mainly introduced by the gate wire bonds and external connections with the gate drive board. It will cause gate voltage swings during the switching transients, and those large gate voltage spikes can potentially exceed the limitations of the gate oxidation. Therefore, the gate drivers are located as close as possible to the devices or large external gate resistor is used to damp gate voltage ringing [3, 4].

The common source inductance $L_{cm}$ is the inductance shared by power loop and gate loop. Physically, it can be either the common connections of these two loops or the mutual inductance between them. Kelvin connected gate-source design can effectively reduce the value of $L_{cm}$ [5].

The parasitic inductance induced by the interconnections in packaging has significant effects on switching performance of the power semiconductor devices. It can lead to large voltage spikes during turn-off transients of active switches [6]. The undesired voltage spikes can potentially exceed the device’s voltage ratings and have a significant impact on the safe operation of fast
switching devices such as SiC and GaN [6, 7]. Figure 1.4 shows the simulated turn-off voltage and current waveforms of the active switch at different values of $L_{ds}$.

![Figure 1.4. Simulation of turn-off transients of active switch at various $L_{ds}$](image)

As can be seen, under the same drive condition, the voltage spikes will be larger as $L_{ds}$ increases. Meanwhile, at increased switching speed (lower external gate resistors) or higher load current condition, the voltage spikes will be more severe.

### 1.1.4 Cooling Advancement in Power Modules

For both Si and WBG based device packaging, low thermal resistance is usually preferred. With smaller thermal resistance, the junction temperature would be lower at a given operating condition, and the system efficiency would be higher. Meanwhile, from the system’s thermal stability point of view, the system’s safe operating range can be extended [8]. Different packaging methods can be used to improve the power module’s thermal performance.
The thermal grease in Figure 1.1 constitutes a significant portion of the thermal resistance from the junction to ambient [9]. Therefore, in the Infineon HybridPack2 module design shown in Figure 1.5, the baseplate and the cold plate are integrated together by using a Cu baseplate with pin-fins which can be in direct contact with the coolant [10]. Thus, the thermal interface material (TIM) layer between baseplate and cold plate can be eliminated by directly soldering the substrate to the integrated pin-fin baseplate as shown in Figure 1.5 (a).

Another example to eliminate the thermal grease is the 2010 Prius Hybrid III. A direct cooling structure is realized by directly brazing the substrates onto the cold plate as shown in Figure 1.6 (a). It is indicated in [11] that the thermal efficiency can be improved by 30% compared to its previous version with thermal grease. To relieve the thermomechanical stress between the cold plate and substrate, the interconnection between them is punched.

A similar approach is also implemented to a SiC power module shown in Figure 1.7 (a). It features an integrated direct cooling as shown in Figure 1.7 (b) where the substrate is directly soldered to the specially designed cold-baseplate. The cold-baseplate is made of a flat copper tube with crisscrossed fins shown in Figure 1.7 (c) [12]. It eliminates thermal grease and realizes integrated direct cooling.
Figure 1.6. 2010 Prius direct cooling module [13].

Figure 1.7. 1200 V, 100 A all SiC phase leg power module [12].
Apart from the typical structure with DBC substrate shown in Figure 1.1, Mitsubishi manufactured a transfer-molded power module (TPM) for use in hybrid electric vehicle [14]. Figure 1.8 (a) illustrates the structure of the module. The chip is directly soldered on the thick copper heat spreader, and a thermal conductive insulation layer (TCIL) is arranged right beneath the thick copper and above the thin copper. The TCIL is a special insulation material with large thermal conductivity. The main benefit of this design is to reduce cost. In reference [15], it is stated that the transfer mold resin is cheaper than the ceramic substrate, injection case, and gel used in common wire bond module. Note that similar to the DBC substrate structure shown in Figure 1.1, thermal grease is still needed in the transfer-molded module for connection with the heat sink as illustrated in Figure 1.8 (b).

\[(a) \text{ Cross-section view schematics} \]

\[(b) \text{ X-ray view of the cold-baseplate} \]

Figure 1.8. Mitsubishi TPM power module [9, 13].
In the Nissan LEAF pure electric vehicle [16] shown in Figure 1.9, thin Cu foil and thermal grease are eliminated to reduce the thermal resistance. The chip is soldered on the thick copper bar and the exposed Cu bar is directly mounted onto a cold plate through an electrical insulation sheet. The sheet has a special composition and offers high thermal conductivity. Note that silicone gel is used instead of the molding resin.

![Diagram of Nissan LEAF power module with Cu/thermal sheet structure](image)

*Figure 1.9. Nissan LEAF power module with Cu/thermal sheet structure [9].*

As can be seen, only the bottom side of the chip is connected to the cooling system in all the power modules discussed above and the top side is dipped into the encapsulating material.

To further improve the thermal performance, several manufacturers and research institutions have proposed the double-sided cooling concepts to utilize both sides’ contact area to conduct heat. Different realization methods of double-sided cooled power module will be discussed as follows.

The first automotive power module with double-sided cooling was introduced and implemented in the Toyota LS 600 hybrid [17] as shown in Figure 1.10. Each module unit is one switch consisting of one Si IGBT and one Si freewheeling diode (FWD). It can be observed from Figure 1.10 (a) that the top side connection is implemented with a planar connection, where both
sides of the chip are soldered directly on the copper plates. It also enables the realization of double-sided cooling as the Cu plates are fully exposed and can be connected to the cooling system directly. In this design, transfer molded material is used as encapsulation. Meanwhile, it provides mechanical support. To connect the Cu plates to the cold plate with electrical isolation and realize double-sided cooling, ceramic slices and thermal grease are used in between the cold plate and Cu plate on both sides. Figure 1.10 (b) shows the real module unit and the exposed Cu plate can be seen clearly. Twenty-four same module units were assembled on the special designed cold plate to realized double-sided cooling as shown in Figure 1.10 (c). The specially designed cooling tubes apply pressure to the module in order to reduce the contact thermal resistance [9].

![Cross section view schematics](image1)

(a) Cross section view schematics

![Real module of one switch](image2)

(b) Real module of one switch

![Modules connected with special designed cola plate](image3)

(c) Modules connected with special designed cola plate

*Figure 1.10. Double-sided cooling power module in 2008 Toyota LS600 hybrid model [9].*
However, in the previous double-sided cooling module, thermal grease is still used to join one side of the ceramic insulator to the Cu plate and the other side to the cold plate. The added thermal grease would increase the thermal resistance of the whole thermal path and impair the cooling performance.

Several companies and institutions proposed other methods to realize double-sided cooling. In Delphi’s planar package [18] published in 2011, a DBC substrate was used on both sides to provide electrical insulations as shown in Figure 1.11. It contains one switch (one IGBT and one diode) in the module and needs further assembly with other modules to function as an inverter. To realize double-sided cooling, a pressure mechanism is needed to ensure a press contact of the module with the cooling system which adds assembly complexity [9].

![Figure 1.11. Delphi planar bond power module with double-sided cooling [19].](image)

In 2012, Oak Ridge National Lab (ORNL) proposed another double-sided cooling power module named Planar-Bond-All (PBA) targeting at automobile traction drive applications [20]. In this design, a phase leg is packaged. As can be seen from the schematic of the design shown in Figure 1.12, the Si IGBTs and diodes are soldered in between two DBCs. Solder is selected to connect the two DBCs to the cold plate directly because of its high thermal conductivity compared with polyimide and thermal grease which is verified by simulation in reference [21].
A planar-bond-all SiC power module with double-sided cooling is presented. The MOSFETs and diodes are sandwiched between the top and bottom substrate through soldering. The substrates are carefully patterned to achieve the electric interconnections [22]. To be directly cooled by air, two pin-fin base plates made of copper are soldered to the two substrates. Liquid cooling can also be realized with the implementation of a specially designed coolant manifold as illustrated in Figure 1.13.
1.2 **Motivation and Objectives**

Three aspects will be discussed in the following sections based on the existing power module layouts for multi-chips. The objective, as a whole, is to provide some design considerations and guidelines when designing power modules with multi-chips in parallel.

1.2.1 *Low Parasitic Inductance Package with Double Sided Cooling*

For high current power modules with several chips in parallel, the load current is high and the voltage spikes will be more severe. To ensure safe operation of the device without sacrificing the switching speed, it is meaningful to reduce the parasitic inductance in the module design stage thus limiting the voltage spikes. In fact, with reduced power loop inductance, the dc-link voltage can be further increased to utilize the power rating of the devices fully.

Meanwhile, considering the benefits of advanced cooling, it is preferred to design a module with double sided cooling. Therefore, the first objective of the dissertation is to design a power module with both low parasitic inductance and double sided cooling.

1.2.2 *Evaluation of Middle Point Inductance’s Effect on Switching Transients*

As discussed in the introduction, most existing high current power module designs start with forming one switch (active switch device in anti-parallel with diodes) through paralleling multiple devices and substrates as shown in Figure 1.2. Then a phase leg configuration is realized by connecting among these different switches. From another angle, the layout can also be perceived as forming a phase leg as the base unit first. Then the phase leg is scaled in one dimension in order to achieve the required current ratings. Figure 1.2 is replotted below with an indication of the scaling approach.
However, as has been discussed in [23], one of the drawbacks of this phase leg layout is the large power loop inductance due to the long commutation path from the anti-parallel diodes of the upper switch and the switching device in the lower switch.

As one of the solutions, the P-cell/N-cell layout can effectively minimize the switching loop by placing the devices inside each commutating cell physically close to each other. Meanwhile, decoupling capacitors can be embedded into each cell to decouple external power loop inductances.

In most of the existing power modules with P-cell/N-cell concept, the current rating is low and only a few dies are paralleled for one switch. Consequently, most of the paralleled devices are scaled in one dimension as shown in Figure 1.15. As more devices are scaled in one dimension, the device far away from the decoupling capacitors will experience higher voltage spikes during turn-off. Therefore, given a specific voltage requirement, the maximum number of devices or the switching speed of the device will ultimately be limited. Consequently, to achieve higher power ratings with more paralleled dies, it is advisable to scale in two dimensions as shown in Figure 1.16.
Figure 1.15. Scaling of P-Cell in one dimension.

Figure 1.16. Scaling of P-Cell in two dimensions.
However, there are several fundamental knowledge needs to be understood before scaling the layout. In terms of scaling, two different methods can be used. The first method is split scaling where all the N-cells and P-cells are scaled independently at the initial stage, then their middle points are connected afterward as shown in Figure 1.17.

![Figure 1.17. Illustration of split scaling.](image)

Identical scaling, on the other hand, connects the middle point of an N-cell and the middle point of a P-cell first forming a basic scalable unit as shown in Figure 1.18. Then the basic units are scaled in two-dimensions. The identical scaling method is similar to the scaling method utilized in traditional Si IGBT module layout except that the P-cell, N-cell design concept is implemented and decoupling capacitors are embedded in each basic unit.

![Figure 1.18. Illustration of identical scaling.](image)
For both split scaling and identical scaling methods, the output or middle point of each cell needs to be connected. This is realized either through DBC-level copper trace connection or external connections. For all cases, a new parasitic inductance parameter $L_{\text{middle}}$ will be introduced as shown in Figure 1.17 and Figure 1.18. In the case of split-scaled power modules, the value of $L_{\text{middle}}$ is larger than that of identical-scaled design. Therefore, before selecting the proper scaling method for designing a power module with multi-chips, the effect of the middle-point inductance on the device’s switching performance should be evaluated. As the second objective of this dissertation, the effect of $L_{\text{middle}}$ on device’s switching transients are evaluated for the split scaling case.

1.2.3 Evaluation of Thermal Coupling’s Effect on Paralleled Devices

The uneven distribution of dynamic switching loss between paralleled devices is always a concern for paralleling multiple devices. The asymmetric power loop inductance, gate loop asymmetry and discrepancies among devices’ parameters will cause different switching timings among paralleled devices thus leading to uneven switching losses. Unlike the self-balance of conduction loss due to the positive temperature coefficient of on-resistance, this unbalanced switching loss can potentially cause temperature differences among paralleled chips in steady state.

However, previous studies only investigated the dynamic switching loss differences in one pulse. Since the paralleled devices are also thermally coupled, a complete electrothermal model is needed to discover the steady state junction temperature of each device with unbalanced dynamic switching loss. Therefore, another goal of this thesis is to implement the thermal model together with the electrical model and discover the role of thermal coupling’s effect on paralleled devices with balanced and unbalanced switching loss.
1.3 Thesis Organization

This thesis is organized as follows. Chapter 2 gives a literature review on these different topics. First, existing low parasitic inductance power modules with both single-sided and double-sided cooling are reviewed. Then a literature review on the middle-point inductance’s effect on switching transients for split scaled power modules is conducted. Thermal coupling’s effect on paralleled devices is also summarized in the end.

Based on the literature reviews, a low parasitic inductance SiC power module with double-sided cooling is designed. The detailed parasitic extraction method and experimental verification are discussed at the beginning of Chapter 3. Following that, different low parasitic layouts are compared, and a low parasitic power module with double-sided cooling is designed and fabricated. Detailed simulation and experiment results regarding the low parasitic design will also be given in Chapter 3.

Chapter 4 presents the evaluation of middle-point inductance’s effect on split scaled power module device’s switching transients. A dedicated SiC power module is designed to facilitate the research. Detailed analysis and experiment results are conducted at different conditions to evaluate the middle-point inductance’s effect on turn-off voltage spikes of active switch and turn-on voltage spikes of the synchronous device. Meanwhile, since a new chip is used (1200V SiC trench MOSFETs from Rohm), its characteristics are evaluated as well in Chapter 4.

Chapter 5 investigates thermal coupling’s effect on balancing steady state junction temperature of paralleled devices with different dynamic switching losses. Finite element analysis based simulation of coupled and decoupled thermal systems are built to evaluate the junction temperature differences among paralleled chips with and without dynamic switching loss difference. Based on the simulation result, a thermal model is extracted and used for evaluation of junction temperature differences at different coupling coefficients. Two power modules are then fabricated
with the same devices and structure except that the coupling coefficient is different. Uneven power losses are distributed to each paralleled device, and their steady state junction temperatures are recorded for comparison.

Chapter 6 summarizes the thesis and key contributions. Furthermore, some future work is covered.
Chapter 2

Literature Review

In this chapter, the state-of-art low parasitic inductance power modules with both single-sided and double-sided cooling are reviewed and summarized first. Then a literature review on the middle-point inductance’s effect on switching transients for split scaled power modules is conducted. Thermal coupling’s effect on paralleled devices is summarized lastly.

2.1 Review of Low Parasitic Inductance Power Modules

Different low parasitic inductance power modules have been designed, and these modules will be presented mostly in a chronological order in the following section. It is noted that the voltage rating of the reviewed modules is above 650 V. The IC level low-parasitic design will not be discussed in the thesis. Meanwhile, since existing low parasitic designs are mainly for SiC power modules or high current Si IGBT modules, only low parasitic inductance designs for vertical structure devices are reviewed. GaN power modules are still in the developing stage, and their lateral structure will lead to different low parasitic inductance designs. Therefore, existing low parasitic GaN designs are not included in this thesis.

2.1.1 Low Parasitic Inductance Modules with Single-sided Cooling

In 2010, Vincotech presented a low parasitic inductance design where an additional low-inductive high-resistance current path is implemented in the module in addition to the low-resistive high-inductance path for continuous operation [24]. The low inductive path is realized by adding an additional PCB bridge (with DC+ and DC- overlapped) to the substrate. The terminals of the PCB bridge are then connected to the main PCB close to the on-board capacitors. The PCB bridge helps to bypass the large parasitic inductance introduced by the long bus terminal screw connection at high frequency. As a result, the power loop inductance is mainly determined by the current path inside the substrate level. 7nH of inductance in the power loop is measured experimentally.
In the meantime, as shown in Figure 2.1 (a), GE introduced a low parasitic single switch SiC power module with power overlay [25]. A phase leg configuration can be implemented with the aid of a specially designed blade connectors shown in Figure 2.1 (b). The power loop inductance is 5 nH, and laminated bus bar can be directly connected to the module with the aid of blade connectors.

In reference [23], a low parasitic phase leg module is fabricated utilizing the P-cell/N-cell concepts. The loop inductances of these modules are 6.5 nH. A similar design is presented in a later work and 4.8 nH is achieved [26]. To eliminate the external parasitic inductance introduced by connector and external bus bars, decoupling capacitors are integrated inside the module. Figure 2.2 illustrates the fabricated module.
Utilizing gold stud bump and placing PCB on top of the devices, reference [27] further reduced the parasitic inductance to 0.86 nH by confining the commutation loop area within the thickness level of the device as shown in Figure 2.3. The decoupling capacitors are placed right on top of the PCB.

As can be seen from Figure 2.3, the current commutation path is shifted from the X-Y plane (device’s length and width dimensions) to the X-Z plane (device’s length and height dimensions). Compared with the width of the device (usually in the range of several mm), the device’s height is less than several hundred micrometers. Consequently, the current commutation loop area can be effectively reduced thus realizing low parasitic inductance. However, to realize this 3D package design, new packaging techniques are needed and their long-term reliability is a concern.

Similarly, reference [28] also minimized the commutation loop area by implementing a specialized triple-conductor double-ceramic multi-layer substrate. A laminated design is realized, and the loop inductance is 4.5 nH. Figure 2.4 shows its structure and current commutation path.

3D all-sintering low parasitic SKiN module is introduced by Semikron in 2014. As discussed in [29], a laminated structure similar to laminated bus bar is realized by utilizing the flexible PCB’s tops as the negative bus. In this way, the parasitic inductance inside the module can be significantly reduced making it especially desirable for fast-switching SiC devices. Figure 2.5
Figure 2.3. Cross section view of Fraunhofer, ETH low parasitic module [26].

Figure 2.4. Cross section view of Nissan research center, Fuji electric low parasitic module [28].

Figure 2.5. Cross section view of Nissan research center, Fuji electric low parasitic module [29].
shows its structure from cross section view. 1.4 nH loop inductance is realized for the module, and 3.2 nH is obtained from the decoupling capacitor terminal.

However, as summarized in Table 2.1, all these previous designs are only capable of single-sided cooling, and it is desirable to design a module with both low parasitic inductance and good thermal performance.

<table>
<thead>
<tr>
<th>Organization</th>
<th>$L_{ds}$</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vincotech</td>
<td>7.00 nH</td>
<td>Blade connector is used, laminated bus bar design</td>
</tr>
<tr>
<td>GE</td>
<td>5.00 nH</td>
<td>Applies P-cell, N-cell concepts to module design</td>
</tr>
<tr>
<td>UTK</td>
<td>6.50 nH</td>
<td>Embeds decoupling caps, laminated bus bar connection</td>
</tr>
<tr>
<td>CPES</td>
<td>4.80 nH</td>
<td>Embeds decoupling caps, laminated bus bar connection</td>
</tr>
<tr>
<td>Fraunhofer ETH</td>
<td>0.86 nH</td>
<td>3D design, Embeds decoupling capacitor</td>
</tr>
<tr>
<td>Nissan Fuji</td>
<td>4.50 nH</td>
<td>Multi-layer substrate is used, laminated bus bar connection</td>
</tr>
<tr>
<td>Semikron</td>
<td>3.2 nH</td>
<td>Flexible PCB on top to realize 3D design</td>
</tr>
</tbody>
</table>

2.1.2 Low Parasitic Inductance Modules with Double-sided Cooling

The loop inductance of most existing double-sided cooling module is not optimized. In a Si IGBT double-sided cooled module used in commercial hybrid electric vehicle [30], a single switch is cooled from both sides. However, long copper bars are used to realize a phase leg configuration resulting in a large value of parasitic inductance. Figure 2.6 shows the double-sided cooled switch module.
In another SiC double-sided cooled module [31], the commutation loop area is still large as it is not confined to the thickness level of the device. Figure 2.7 shows its design structure and the current commutating path.

Based on the resin mold module design in [30], a recent commercial low parasitic (7.5 nH) SiC module is developed by confining the commutation loop in the thickness level of the device [32]. A laminated design is realized as shown in Figure 2.8, and the terminal is directly connected to laminated bus bars. However, thermal grease is required as the heat spreader is used in the resin mold module thus limiting its thermal performance.
In reference [33], a low parasitic Si IGBT module is designed with double-sided cooling. Utilizing state-of-art double-etching three-layer copper substrate, the loop area is minimized as shown in Figure 2.9. In terms of system integration with the external bus bar, a specially designed power edge connector (PEC) is used and the phase-leg module can be directly inserted into the connector. Meanwhile, high-frequency decoupling capacitors with suitable size can be embedded in the connector as well as illustrated in Figure 2.9 (c). However, the design is complicated and not cost-effective as double-etching and multi-layer substrates with vias are required.

In 2016, a high-density power chip on bus (PCoB) module is introduced which also features low parasitic inductance [34]. Figure 2.10 shows the structure view for one switch. As a coefficient
Figure 2.9. Low parasitic double-sided module from University of Nottingham, and University of Parma [33].

Figure 2.10. Structure of the low parasitic design from NCSU [34].
of thermal expansion (CTE) buffer between the chip and substrate, molybdenum spacers are used which helps to reduce the thermal-mechanical stress. However, only the value of parasitic inductance of one switch is given, and the total loop inductance can be affected by external connections.

Another 3D low parasitic inductance double-sided power module is presented at the same time [35]. The power chip on chip (PCOC) concept is realized. The chips are embedded in the insulation material and then connected to the copper through micro-vias. These micro-vias are realized with the help of laser drilling and electroplated copper process. Figure 2.11 shows the structure of the power module, and no obvious voltage spike is observed from experiment results. The power loop inductance is less than 2 nH and is mainly determined by the location of decoupling capacitors.

![Figure 2.11. Structure view of the low parasitic design with embedded die technology from Univ. Grenoble Alpes, CNRS, G2Elab and Mitsubishi Electric R&D Center Europe [35].](image)

Similar to Table 2.1, the above mentioned low parasitic inductance modules with double-sided cooling are summarized in Table 2.2. It can be seen that minimizing the current commutation loop and embedding decoupling capacitors are two effective ways to reduce power loop inductance values.
Table 2.2. Summary of low parasitic inductance power modules with double-sided cooling.

<table>
<thead>
<tr>
<th>Organization</th>
<th>$L_{ds}$</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Denso</td>
<td>Not given</td>
<td>Inductance is large due to the long copper bar connection</td>
</tr>
<tr>
<td>ORNL</td>
<td>6.03 nH</td>
<td>Parasitic inductance is not optimized</td>
</tr>
<tr>
<td>Denso</td>
<td>7.50 nH</td>
<td>Parasitic inductance is reduced, but thermal grease is needed to connect the module to a heat sink</td>
</tr>
<tr>
<td>The University of Nottingham, University of Parma</td>
<td>Not given</td>
<td>Parasitic Inductance is small, Double etching and multi-layer substrate is used, Power edge connector is designed for system integration</td>
</tr>
<tr>
<td>NCSU</td>
<td>Not given</td>
<td>Molybdenum spacers are used, $L_{ds}$ for single switch is 8nH, Loop inductance will vary depending on connection between top and bottom switches</td>
</tr>
<tr>
<td>G2Elab, Mitsubishi</td>
<td>&lt; 2 nH</td>
<td>Embedded die technology is used, Micro-vias for vertical interconnection, No obvious voltage overshoot is observed</td>
</tr>
</tbody>
</table>

2.2 Middle Point Inductance’s Effect on Switching Transients

As discussed in Chapter 1, the effects of gate loop parasitic inductance, power loop parasitic inductance and common source inductance on a device’s switching have been studied previously. For power modules with multiple chips in parallel and scaled in a split way, a new parasitic inductance will be introduced between the middle points of P-cells and N-cells as shown in Figure 1.17. The middle point inductance $L_{middle}$ can be formed by either DBC level copper trace or external bus connections. For power modules with single chip or power modules with identical scaling method, $L_{middle}$ is small and can be ignored.

However, for high current multi-chip power modules with P-cell, N-cell split scaling design, a long copper trace is needed to connect the middle points of both P-cells and N-cells. In this case, the middle-point inductance should be considered during the switching transients.
Previous publications [36, 37] discussed the role of $L_{\text{middle}}$ in split converter topology. Both pointed out that the turn-on loss can be reduced in split converter designs since $L_{\text{middle}}$ helps to decouple the N-cell with P-cell thus eliminating the $C_{\text{oss}}$ losses due to the other phase leg. In reference [36], the benefits of reduced dv/dt at output terminal and decreased cross-talk effect are observed in split converters. The author also points out the turn-off loss will increase with an increase of $L_{\text{middle}}$.

However, the value of $L_{\text{middle}}$ in those split converters are large: usually in the range of tens of uH. For multi-chip power modules with P-N-cell split scaling design, $L_{\text{middle}}$ is in fact, within several hundred of nH. With a small value of $L_{\text{middle}}$, the middle point inductance will actually participate more actively in the switching transients.

Moreover, none of these aforementioned studies exploit the effect of $L_{\text{middle}}$ on a device’s voltage spikes during active switch’s switching transients. Since the voltage spike is an important factor determining the number of paralleled devices and switching speed, it is meaningful to have a better understanding of the effect of $L_{\text{middle}}$ on device’s switching transients. In Chapter 4, detailed analysis and experiment results will be provided to evaluate its effect on the voltage overshoots of both switching devices and their anti-parallel diodes.

### 2.3 Thermal Coupling’s Effect on Steady State Junction Temperature Differences among Paralleled Devices

The dynamic current distribution for paralleled devices is not always balanced during the switching transients. It has been studied that the device’s threshold voltage variation [38-41] and the circuit layout mismatches can [42, 43] lead to unbalanced dynamic current among paralleled devices during turn-on transients.

This unbalanced switching current can lead to different switching losses among paralleled devices. If the junction temperature of one device is increased because of excessive switching loss,
its threshold voltage will drop. Consequently, more turn-on loss will be generated, and this device will be more thermally stressed compared to other devices. This negative temperature coefficient attribute of turn-on loss distribution brings concern about long-term reliability for paralleling devices. Therefore, several symmetric package layout designs [44, 45] and active balancing methods [38, 46, 47] have been proposed.

Still, all these concerns are based on the testing result in one pulse. In terms of the concern for steady-state junction temperature difference, the thermal model will also play a role. Specifically, the thermal coupling’s effect on steady state junction temperature imbalance should be considered. It has also been discussed previously that thermal coupling can help to balance the junction temperature of paralleled devices [48]. However, there are no quantitative studies discussing how effective thermal coupling will affect the junction temperature imbalance. Though in a recent literature [49], a complete electrothermal model is proposed; it still does not focus on the evaluation of thermal coupling’s effect on steady state junction temperature imbalance due to unbalanced switching losses.

In Chapter 5, the effect of thermal coupling on paralleled devices is studied considering balanced and unbalanced switching loss. By introducing the coupling coefficient, a quantitative curve is derived to vividly illustrate thermal coupling’s effect on steady state junction temperature imbalance.
Chapter 3

Parasitic Inductance Extraction and Design of Low Parasitic Inductance Power Module with Double-sided Cooling

As discussed in Chapter 1, it is meaningful to reduce the parasitic inductance in the module design stage thus limiting the voltage spikes and ensuring safe operation of the device without sacrificing the switching speed. Meanwhile, it is desirable to design a module with double sided cooling as well to fully exploit the power capability of the devices. Therefore, the goal of this chapter is to design a power module with both low parasitic inductance and double sided cooling.

Chapter 3 is organized in the following sequences. To begin with, the parasitic inductance extraction method in the simulation is discussed first. The simulated parasitic inductance values are compared with theoretical calculations, and further verified in an experiment result with a 3D planar-bond SiC power module. Once the extraction method in simulation is validated, different low-parasitic inductance power module designs with double-sided cooling are compared, and one design is selected as a tradeoff between electrical and thermal performance. The proposed low parasitic inductance double-sided cooling design is implemented, and a 1200V/50A SiC power module is fabricated. Experiments are conducted to reveal the benefits of reduced parasitic inductance.

3.1 Parasitic Inductance Extraction in Simulations

The electromagnetic modeling of the interconnection configuration in a package is an effective way to calculate the value of parasitic inductance in the design stage. Previous papers [50-52] have dealt with the extraction of power loop parasitic inductance for power module packages with the aid of Ansys Q3D Extractor. However, only a single lumped value is extracted, and few studies correlate the meaning of the extracted parasitic inductance value to the switching transients. Reference [53] shows that the lumped power loop parasitic inductance for a TO-220 packaged GaN
device is different during turn-on and turn-off process. It indicates that the parameters of the parasitic components are closely related to the devices’ operation conditions.

A step-by-step procedure is taken to conduct the research. First, the validity of the simulation results is first verified through comparison with theoretical calculations for some simple geometries.

### 3.1.1 Simulation of Simple Round Wire

The parameters of a straight conduction wire are shown in Figure 3.1 and a model is built in Q3D as well. Theoretically, with and without considering the skin effect, the partial inductance expression for a round wire can be illustrated by the following two equations respectively for the high-frequency and low-frequency range [54]:

\[
L_{p, HF} = \frac{1}{5} l \cdot (ln \frac{4l}{d} - 1) \tag{1}
\]

\[
L_{p, LF} = \frac{1}{5} l \cdot (ln \frac{4l}{d} - \frac{3}{4}) \tag{2}
\]

where \( l \) and \( d \) are the length and diameter of the wire respectively.

![Figure 3.1. Straight round wire simulation.](image)

Then, considering the mutual inductance, the cases of two round straight round wires carrying current in the same direction are simulated and compared as shown in Figure 3.2. Similarly, the total partial inductance expression for two paralleled round wires is:
\[ L_{total} = 0.5(L_p + |M_p|) \]  

(3)

where \( L_p \) is obtained from equation (1) or (2) depending on the frequency range; \( M_p \) is the mutual inductance between the two wires and is calculated by [54]:

\[ M_p = \frac{1}{5} l \cdot \left( \ln \left( \frac{l}{s+r} + \sqrt{\frac{l}{s+r}}^2 + 1 \right) \right) - \sqrt{\left( \frac{s+r}{l} \right)^2 + 1} + \frac{s+r}{l} \]  

(4)

\( s \) is the spacing between two parallel wires.

Figure 3.2. Paralleled straight round wire with currents in the same direction.

The calculated theoretical result and simulated result are summarized in Table 3.1 and Table 3.2. The simulated value matches the theoretical calculations at both low frequency and high frequency range indicating a trustworthy simulation result with this software. Also, it is observed that the mutual inductance plays a role for wires carrying current in the same direction: the larger the mutual inductance, the larger the total inductance value.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Inductance Value</th>
<th>Theoretical Calculation</th>
<th>Simulations</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>24.49 nH</td>
<td>24.70 nH</td>
<td></td>
</tr>
<tr>
<td>high frequency</td>
<td>22.74 nH</td>
<td>22.98 nH</td>
<td></td>
</tr>
</tbody>
</table>
Table 3.2. Theoretical calculation and simulation result comparison for paralleled round wire with currents in the same direction.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Inductance Value</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Theoretical Calculation</td>
<td>Simulations</td>
<td></td>
</tr>
<tr>
<td>DC</td>
<td>18.46 nH</td>
<td>18.57 nH</td>
<td></td>
</tr>
<tr>
<td>high frequency</td>
<td>17.59</td>
<td>17.61 nH</td>
<td></td>
</tr>
</tbody>
</table>

3.1.2 Simulation of Paralleled Wire Bonds

Wire bonds are usually used in today’s commercial power modules as the interconnection between the device and the direct-bonded-copper substrate. The number of wire bonds is typically determined by the current rating of the device and the current capabilities of each wire bond. Usually, some design margin is considered and the number of wire bonds together with the gauge of wire bonds are varied to meet the requirement. As a result, different combinations can be obtained for the same current capability. Since all the wire bonds carry current in the same direction, the selection of the number and gauge of wire bonds will eventually affect the total inductance value. This effect is studied through simulations as follows. Figure 3.3 (a) shows two wire bonds in parallel with their parameters illustrated in Figure 3.3 (b). To obtain a fair comparison of inductance value at a different number of wire bonds, the following assumptions are made:

- The parameters of each wire bond are the same.
- The wire bonds are equally spaced along the width of the bonded chip;
- For each simulation, the width of the bonded chip is the same (8 mm is used in the simulation).

![Figure 3.3](image1.png)  
(a) Wire Parameters  
(b) Geometry in Q3D

*Figure 3.3. Parasitic inductance extraction for wire bonds.*
Figure 3.4 (a) shows the location of each wire bond in the case of 2 wire bonds in parallel and 3 wire bonds in parallel respectively. The wire bond’s material is assigned to aluminum in Q3D. When the total number approximate infinity, an aluminum bar is simulated as shown in Figure 3.4 (b). Figure 3.5 shows the simulated inductance value at 100 MHz for both 10 mil and 15 mil gauge wire bonds. The inductance value indeed decreases with increasing numbers of wire bonds. However, due to the width limitation of the chip and effect of mutual inductance, the rate of change of inductance is slower at a higher number of wire bonds. Thus, the total inductance value cannot be effectively reduced by simply increasing the number of wire bonds. For this specific case, the lowest obtainable inductance value is around 3nH as indicated by the upper triangle marker in Figure 3.5. This represents the case of aluminum bar.

(a) Location of wire bond for 2 and 3

(b) Aluminum bar in Q3D

*Figure 3.4. Location of wire bonds with different numbers.*
3.1.3 Simulation Extraction of Power Loop Inductance for a 3D Planar Bond Package

In the previous simulations of simple round wires and wire bonds, only partial inductance is simulated. The voltage spikes during the switching transients are caused by the loop inductance. This loop inductance is formed by several intervals of partial inductances and their mutual inductance’s effect. To accurately derive a lumped power loop inductance from a certain package, it is necessary to identify the partial inductance contributing to the loop inductance first. The identification procedure is related to the switching transients of the active switch. Therefore, different values of loop inductances can be obtained at different switching intervals. In this section, a 3D planar-bond package is used as an example to illustrate the procedure of power loop inductance extractions considering the switching transients.

Detailed design of the module is discussed in [31], and the double-sided planar-bond module is shown in Figure 3.6. Without taking into consideration the mutual inductance, the extracted partial parasitic values for each interconnection of the module are shown in Figure 3.7.
Figure 3.6. 3D Planar-bond-all module design and schematics.

Figure 3.7. Extracted parasitic parameters without considering mutual inductance.
However, the extracted parameters in Figure 3.7 do not determine the exact value of the total power loop inductance, which is usually a lumped parameter considering the current density distribution and the effect of mutual inductance. A detailed analysis of lower MOSFET turn-off process at heavy load is shown as follows, and the method to determine the lumped power loop inductance value will be illustrated.

In the lower device turn-off process, the drain-to-source voltage of the lower MOSFET is initially increased to the bus voltage during the $dv/dt$ period as shown in Figure 3.8. Following it, the upper diode is turned on, and the current began to shift from the lower device to the upper diode.

*Figure 3.8. Simulated switching off transients waveforms in LTspice.*
During this di/dt period, there is still some current flowing through the lower MOSFET channel. Therefore, the whole power loop is illustrated in red as shown in Figure 3.9. In other words, only those partial inductances in red contribute to the power loop inductance and the field coupling effect among those inductances should be considered.

With the help of Ansys Q3D, the lumped value of power loop inductance considering the field coupling effect can be obtained. The anti-parallel diode of the lower MOSFET is modeled as a junction capacitance with single value during the whole turn off process as indicated in Figure 3.9. The current density distribution is illustrated in Figure 3.10 as well.

**Figure 3.9.** Power loop parasitic inductance path during di/dt transient.

**Figure 3.10.** Current density distribution during di/dt transient.
During the di/dt period, the parasitic inductances adjacent to the lower diodes are not contributing to the power loop inductance calculations because the current is small compared to channel current. However, in the ringing process, the lower MOSFET is modeled as a junction capacitor. The junction capacitor of the MOSFET and diodes together resonates with the power loop inductance. Therefore, all partial inductances will contribute to the lumped power loop inductance as illustrated in red in Figure 3.11.

![Image](image.png)

*Figure 3.11. Power loop parasitic inductance path during ringing periods.*

The simulated results are obtained as summarized in Table 3.3. It can be seen that the parasitic inductance values during di/dt and the ringing period are different for both upper and lower devices. Meanwhile, due to the asymmetric package design, there is some discrepancy between the turn-off power loop inductance values of upper and lower device.

<table>
<thead>
<tr>
<th>Condition (@100MHz)</th>
<th>Upper Device</th>
<th>Lower Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn off Loop</td>
<td>During di/dt</td>
<td>6.01 nH</td>
</tr>
<tr>
<td>Inductance</td>
<td>Ring period</td>
<td>5.73 nH</td>
</tr>
</tbody>
</table>
3.1.4 Experiment Extraction of Power Loop Inductance for a 3D Planar Bond Package

Experimental parasitic extraction of the module is implemented to verify the simulation extraction method. A dedicated module is fabricated, and a double-pulse test set up is built as shown in Figure 3.12.

![Figure 3.12. Double pulse test set up.](image)

The module is specially designed with access to the device’s drain-source voltage $V_{ds,kelvin}$ directly through a kelvin connection as shown in Figure 3.13 (a). For the circuit diagram of 3D planar-bonded module’s double pulse test shown in Figure 3.13 (b), the decoupling capacitors are located on the DPT board and the drain-source current of the MOSFET can be obtained from the shunt. Only parasitic inductance and resistance of the package exist in between those two voltage sense points. Therefore, with a knowledge of the rate of change of current during turn-off, the parasitic inductance of the power can be extracted directly by comparing the kelvin sensed drain-source voltage $V_{ds,Kelvin}$ with the terminal voltage $V_{ds,PN}$. 
(a) Fabricated module

(b) Circuit diagram for $L_{ds}$ extraction

Figure 3.13. 3D planar-bond-all module.
Figure 3.14 shows the experiment turn-off waveforms of $V_{ds_{,kelvin}}$, $V_{ds_{,PN}}$ and drain current of the lower device at 600 V, 46 A load current with 10 Ω gate resistor. Both the kelvin $V_{ds_{,kelvin}}$ and terminal $V_{ds_{,PN}}$ are measured using the same probe but at different times. The kelvin $V_{ds_{,kelvin}}$ waveform is reproduced in Matlab to compare with the terminal $V_{ds_{,PN}}$. Based on the cursor data value shown in Figure 3.14, the $\frac{di}{dt}$ rate is calculated to be -4.08A/ns. The voltage difference between $V_{ds_{,kelvin}}$ and $V_{ds_{,PN}}$ is 26.90 V. Thus, the calculated power loop parasitic inductance value is:

$$L_{loop\ base} = L_{ext} = \frac{26.9V}{(4.08A/\text{ns})} = 6.59 \text{ nH}$$

(5)

Figure 3.14. Experimental turn-off waveforms of lower MOSFET in baseline module.

Compared with the simulated value 6.03nH in Table 3.3, the experiment result matched well with the simulation result. Moreover, as can be seen from Figure 3.14, the parasitic inductance of the power module only contributes to 26.90 V in terms of the voltage spikes while the total voltage overshoot is 100.6 V. The rest 73.26% of the voltage overshoot is caused by the double
pulse test board layout and connectors between DPT board and power module. To verify that, another parasitic inductance simulation is carried out including both the power modules and the PCB layout. The real PCB layout is directly exported from Altium designer, and its dielectric thickness and copper thickness are adjusted in AnsoftLinks. Afterward, the PCB geometry is imported to Ansys Q3D and physically connected to the power modules thus forming the complete power loop. In the simulation, the excitation source and sink are assigned to the positive and negative pads of the on-board ceramic capacitors. Figure 3.15 illustrates the geometry of PCB board together with the power module in Ansys Q3D.

![Figure 3.15. Simulation of real PCB layout together with power module package.](image)

Table 3.4 summarizes the simulation results considering both upper switch and lower switch turning off. The total power loop inductance is increased from 6.03 nH to 23.03 nH if the PCB boards are considered. The PCB introduced loop inductance contributes to 73.82% of the whole power loop inductance. Therefore, it is necessary to place decoupling capacitors at the terminal of the power modules to decouple those parasitic inductances introduced by either PCB
board or bus bar. A two-stage decoupling design is needed to further reduce the total parasitic inductance value. Only in this way, the total power loop inductance of the power module will be solely determined by the package’s parasitic inductance, and reducing the package’s parasitic inductance becomes meaningful.

Table 3.4. Q3D simulation results for turn-off power loop inductance values with DPT PCB.

<table>
<thead>
<tr>
<th>Condition (@100MHz)</th>
<th>Upper Device</th>
<th>Lower Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn off Loop</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inductance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>During di/dt</td>
<td>23.00 nH</td>
<td>23.03 nH</td>
</tr>
<tr>
<td>Ring period</td>
<td>21.78 nH</td>
<td>22.31 nH</td>
</tr>
</tbody>
</table>

Aside from extracting the parasitic inductance of the module, the switching loss of this 1200V/50A SiC power module is tested at various load conditions and gate resistors with a DC-link voltage of 600 V. The turn-off loss data is shown in Figure 3.16. Figure 3.17 and Figure 3.18 illustrates the turn-on and total switching loss. All loss data is tested at room temperature.

![Figure 3.16. Turn-off loss of the 3D planar-bond-all module at 600 V.](image-url)
Figure 3.17. Turn-on loss of the 3D planar-bond-all module at 600 V.

Figure 3.18. Total switching loss of the 3D planar-bond-all module at 600 V.
3.2  Low Parasitic Inductance SiC Power Module Design with Double-sided Cooling

Based on the literature reviews on low parasitic inductance power modules in Chapter 2 and the discussions in the previous section, three main techniques should be considered in designing a low parasitic inductance module:

- The current commutation loop should be confined to a small area. To realize this, the P-cell/N-cell concept layout should be adopted first. Moreover, it is preferred to utilize various packaging techniques to obtain a laminated design structure to further reduce the current commutation loop area.

- High-frequency ceramic decoupling capacitors should be embedded in the terminal of the package. Also, their location should be as close as possible to the devices. The value of these capacitors in total should be large enough to fully decouple the external parasitic inductance introduced by terminals, bus bars, and other connections.

- An easy connection between power module’s bus terminal and DC-link bus terminals is desirable.

The 3D planar-bond package is used as a baseline for improving its electrical performance: mainly reducing the value of power loop parasitic inductance. Different designs are compared first, and a final design is selected and manufactured. The fabricated SiC power module is tested in the experiment for verification purpose.

3.2.1 Preliminary Simulation Comparison of Different Layouts

At first, a simple modification is made to the baseline module by changing the location of the bus terminals. As can be seen in Figure 3.11, the current from negative terminal travels a long path to the lower switch compared to the distance between the upper switch and positive terminal. By moving the P, N terminals to the center part of the module, the power loop can be reduced slightly and the values will become more symmetric for upper and lower devices.
Figure 3.19 shows its mechanical layout in Solidworks, and all the layout dimensions remain the same for both modules. The geometry is exported to Ansys Q3D, and the power loop inductance of the lower device during $\frac{di}{dt}$ is simulated to be 5.24 nH. It is reduced slightly compared to the simulation result of the baseline module in Table 3.3. The current distribution comparison of the baseline module and modified 3D planar bond all module is shown in Figure 3.20.

Still, the commutation loop is large as it is mainly in the X-Y plane where its dimensions are determined by the length and width of the device plus spacing between devices. It is desirable to further reduce the commutation loop by shifting one of the dimensions to the Z-axis. The Z-axis length is mainly determined by the device’s thickness, and it is usually within several hundreds of um. This value is much smaller compared to the case of device’s width or length which are normally in the range of several mm. In the following section, several laminated designs are compared.
One easy solution is to stack the upper MOSFETs on the lower anti-parallel diode and place the upper anti-parallel diode on top of the lower MOSFETs. The middle-point terminal is inserted in between the upper and lower devices and extended to the outside for mechanical connection. Two conventional DBCs are used for positive and negative bus connections. The proposed layout is shown in Figure 3.21 with exploded views and different side views.

Figure 3.21. Stack design layout in Solidworks.
Similarly, the geometry is simulated in Q3D and simulation result shows 1.23 nH considering lower device turn off in $\frac{di}{dt}$ period. The current distribution of the stack design is shown in Figure 3.22. Since the layout is symmetric for both upper and lower switches’ commutation loops, only the condition of the lower device is simulated. Compared to the baseline module result, this stack design can greatly reduce the power loop inductance. Obviously, the dimensions are diminished as well in the stack design. However, the device’s dimensions, the thickness of the power terminals and the thickness of the DBCs are unchanged.

![Figure 3.22. The current distribution of stack package design.](image)

Figure 3.22 shows that bus terminal pairs are placed in the middle between the physical location of the P-cell and N-cell. This location is not optimized for each cell. Taking the N-cell commutation path, for instance, the bus terminals are misaligned to the N-cell. This will add extra current traveling paths.

To improve this, two pairs of bus terminals are used for connection with external bus bars. Each pair is aligned with the center of each commutating cell. In this way, the parasitic inductance can be reduced. Figure 3.23 shows the mechanical layout in Solidworks, and Q3D simulation result shows that the power loop inductance can be reduced from 1.23 nH to 1.03 nH.
A comparison of planar bond all design and stack design is summarized in Table 3.5. From the parasitic inductance point of view, all the stack package designs will improve the electrical performance greatly. However, there are two drawbacks with the stack designs:

- Since each device is stacked on top the other, the thermal coupling between these stacked chips is strong. Ideally, each device should be directly connected to the top and bottom substrates in the double-sided cooled power modules. In this way, each device is cooled from both sides. However, in the stack design, the devices are not directly connected to the substrates on both sides. Taking the lower MOSFETs in Figure 3.21 for example, the middle-point terminal pin and the upper anti-parallel diode are inserted in between the top substrate and the MOSFETs. Therefore, double-sided cooling is not realized for this MOSFET. The stack design, though can reduce the parasitic inductance, will make the cooling performance of each chip worse compared with the baseline packaging design.

- The other concern with the stack design is the mechanical stress on the devices introduced by the middle-point terminal pin. This pin will mechanically connect to the outside. Any
mechanical vibration on the outside will be reflected on the devices through this terminal pin as the devices are all soldered on each side of the pin. This will bring concerns about safe operation of the devices under mechanical stresses.

Table 3.5. Comparison of turn-off power loop inductance for different designs.

<table>
<thead>
<tr>
<th>Condition (@100MHz)</th>
<th>Baseline Module</th>
<th>Modified PBA Module</th>
<th>Stack Module</th>
<th>Modified Stack Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower MOSFET</td>
<td>6.03 nH</td>
<td>5.24 nH</td>
<td>1.23 nH</td>
<td>1.03 nH</td>
</tr>
<tr>
<td>Turn off Loop</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inductance during</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>di/dt</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Performance</td>
<td>Good</td>
<td>Good</td>
<td>Weakened</td>
<td>Weakened</td>
</tr>
<tr>
<td>Mechanical Stress</td>
<td>Small</td>
<td>Small</td>
<td>Large</td>
<td>Large</td>
</tr>
<tr>
<td>from Middle Point</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Terminal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3.2.2 Proposed Package Design

Since the stack design has some drawbacks, a design with both low parasitic inductance and double-sided cooling is needed. An island structure design is proposed, which can realize laminated commutation loop and double-sided cooling. Figure 3.24 (a) and (b) show two island package designs with two MOSFETs and diodes constituting a phase leg, the difference is the placement of diodes. In the island designs, a dedicated island copper trace is etched for placement of anti-parallel diodes. Meanwhile, a special interconnection shim is used as the vertical connection between top and bottom substrates for the purpose of realizing the laminated design. More details about the commutation path will be discussed in the actual module design and simulation section. In this section, the simulation results of the proposed two island designs are given as shown in Table 3.6. As can be seen, the parasitic inductance values of the proposed island designs are slightly
larger than the modified stack design. However, each device is cooled from both sides, and the mechanical stress from the middle-point terminal pin is relieved.

Figure 3.24. Island package designs.

Table 3.6. Comparison of turn-off power loop inductance for island package designs.

<table>
<thead>
<tr>
<th>Condition (@100MHz)</th>
<th>Island Package Design 1</th>
<th>Island Package Design 2</th>
<th>Modified Stack Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower MOSFET</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn off Loop</td>
<td>1.46 nH</td>
<td>1.63 nH</td>
<td>1.03 nH</td>
</tr>
<tr>
<td>Inductance during</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>di/dt</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3.2.3 Actual Low Parasitic Double-sided Cooling Module Design and Simulation

The real fabricated module uses the second island package design, and the substrate is designed for placing one anti-parallel diode to reduce the manufacturing cost. Detailed island design structure will be discussed in the following section.

One of the goals of island design is to reduce the current commutation loop area. Figure 3.25 and Figure 3.26 show the structure layout comparison of the baseline double-sided cooling module and the new design.
Projected Loop Area in X-Y Plane

Figure 3.25. Baseline 3D bond all package’s structure.

Figure 3.26. Real island design package’s structure.
The X-Y-Z coordinates are defined such that the devices are distributed in the X-Y plane for both designs. The Z-axis is utilized to realize vertical interconnections and achieve double-sided cooling.

In the baseline module, the commutation loop is formed in the X-Y plane as shown in Figure 3.25. Since the device’s width and length are usually large (in the range of several mm) compared with its thickness (in the range of several hundreds of μm), the resulting current commutation loop covers a large area in the projection of X-Y plane.

To reduce the loop area in the new design, the commutation loop is shifted to X-Z plane with the aid of an island substrate layout. Figure 3.27 illustrates the whole structure of the low parasitic double-sided cooled power module together with its circuit diagram.

To be specific, the upper switch MOSFET and lower switch diode are initially placed close to each other following the P-N cells design concept. Then a dedicated island is patterned on the substrate, and a copper-molly composite shim is used as an interconnection between the top substrate and bottom substrate. With this island design pattern and vertical interconnection, the commutation loop is projected on to the X-Z plane. As a result, the commutation loop area is reduced as it is restricted to the thickness level of devices.

However, as discussed in the previous section, the parasitic inductance of terminal connections and external bus bar will also contribute to the total power loop inductance. Although the parasitic inductance of the power module itself is small, the voltage overshoot can be large if the parasitic inductance outside the module is not decoupled. Adding decoupling capacitors on the module’s DC bus terminal side can effectively offset the parasitic inductances caused by external circuit layout. Therefore, it is important to integrate decoupling capacitors in the module.
Figure 3.27. Exploded side view of the low parasitic inductance power module and its circuit diagram.
In this design, a 7oz two-layer PCB with controlled thickness is used to solve this issue. As shown in Figure 3.27, the decoupling capacitors are easily soldered on a short laminated PCB bus bar, and the PCB is closely soldered to the bus terminals of the power module.

Another function of the PCB bus bar is to realize the easy connection of the power module with outside bus bars. In this proposed package design, the connection with external bus bars is implemented through screw-hole connections at the other end of the short PCB.

As discussed above, two conventional cost-effective AlN substrates are patterned to obtain low parasitic inductance. Phase leg configuration is realized where two 1200 V SiC MOSFETs and one anti-parallelled 1200 V SiC Schottky diode together form one switch. The MOSFETs and diodes are specially designed: both sides of the device are metallized and solderable. Gate connections are implemented with 5 mil bond wires. The whole current commutation loop is shown in Figure 3.28 assuming current is going from positive bus to negative bus.

As can be seen, the loop area is greatly reduced as it is shifted to X-Z plane. The mechanical layouts of the baseline module and new double-sided cooled module are imported into Ansys Q3D. Then the materials are added, and the power loop inductance values are simulated as summarized in Table 3.7.
Table 3.7. Comparison of power loop inductance values for proposed low parasitic package and baseline package.

<table>
<thead>
<tr>
<th>Condition (@100MHz)</th>
<th>Baseline 3D Planar Bond All Package</th>
<th>Proposed Low Parasitic Inductance Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower MOSFET Turn off Loop Inductance during di/dt</td>
<td>6.03 nH</td>
<td>1.63 nH</td>
</tr>
</tbody>
</table>

As can be seen, the power loop inductance is reduced from 6.03 nH to 1.63 nH. More than 70% reduction is achieved in the new design. Figure 3.29 illustrates the current density distributions for both modules. The loop area of the baseline module is also illustrated as indicated by the black solid line in Figure 3.29 (a). It can be observed that the commutation loop in the previous design is in the X-Y plane and contours a large area. On the contrary, as has been discussed in detail in the previous section, the loop area in the newly designed module is confined in the Z-axis where the device’s thickness is marginal.

(a) Baseline package  (b) Low parasitic inductance package

*Figure 3.29. High-frequency current density distributions of different modules.*
3.2.4 Experiment Result

Both the baseline module and low parasitic module are fabricated for experimental comparisons. Double pulse tests are performed to characterize the lower MOSFET’s switching performance and extract the module’s parasitic inductance.

Figure 3.30 shows the fabricated low parasitic inductance power module without pin-fin heat sink. The PCB bus bar is soldered in the same process the devices are soldered. The exposed pads on the PCB are used for soldering decoupling capacitors. The baseline power module is shown previously in Figure 3.13 (a). Compared with the baseline package, the substrate’s width is the same. However, the length of the low parasitic module substrate is smaller.

![Fabricated low parasitic inductance module without pin-fin heat sink.](image)

Notice that each module is fabricated with access to the device’s drain-source voltage $V_{ds,Kelvin}$ directly through a kelvin connection. The kelvin drain-source voltage is only connected
to passive voltage probe for measurement. Therefore, less current will flow in the sensing loop and $V_{ds,Kelvin}$ can represent the real voltage across the device during switching transients. Meanwhile, the voltage across the P, N terminals $V_{ds,PN}$ will also be recorded in experiments.

The experimental parasitic inductance extraction method for the baseline module has been discussed in the previous section. Knowing the current slew rate from the shunt measured data, its parasitic inductance is easily extracted by comparing the voltage difference between $V_{ds,Kelvin}$ and $V_{ds,PN}$. The extracted result is 6.59 nH for the baseline package. Similar parasitic extraction approach can be applied to the low parasitic power module if the decoupling capacitors are not added as indicated by the dashed line in Figure 3.31.

![Circuit diagrams of the extraction circuit for low parasitic inductance module.](image)

*Figure 3.31. Circuit diagrams of the extraction circuit for low parasitic inductance module.*
However, even without soldering the decoupling capacitors, the extracted parasitic inductance $L_{\text{ext}}$ will differ from the module’s power loop inductance. In fact, for the low parasitic module circuit, $L_{\text{ext}}$ consists of two parts: the power loop inductance of the power module $L_{\text{loop,low}}$ and the parasitic inductance of the short PCB bus bar $L_{\text{PCB Busbar}}$. Simply applying the same method will not provide an accurate inductance value of the power module. Therefore, a frequency domain analysis is used instead to extract the parasitic inductance of the power module solely.

To implement frequency domain analysis, six 1 kV 0.15 uF ceramic decoupling capacitors are soldered as shown in Figure 3.32. The capacitance value is selected such that the voltage across the decoupling capacitor is unchanged during the turn-off switching transients making this decoupling path effectively short at high frequency. In this way, the ringing frequency of the kelvin drain-source voltage $V_{ds,\text{Kelvin}}$ will be mainly determined by the power loop inductance of the newly designed module $L_{\text{loop,low}}$ and the junction capacitance $C_{ds}$ of the device at bus voltage.

![Fabricated low parasitic inductance power module with decoupling capacitors and fin-pin heatsinks.](image)

*Figure 3.32. Fabricated low parasitic inductance power module with decoupling capacitors and fin-pin heatsinks.*
Similar to Figure 3.12, the double pulse test bench for evaluating the parasitic inductance of the new module is shown in Figure 3.33. Aside from the film decoupling capacitors, surface mounted ceramic capacitors are soldered on the bottom side of the printed circuit board to form a two-stage decoupling network. The same gate drive circuits are used but the gate resistors are varied.

![Test bench for parasitic inductance extraction of the new module.](image)

Figure 3.33. Test bench for parasitic inductance extraction of the new module.

Figure 3.34 illustrates the experiment turn-off waveforms of the lower switch at 600 V with an external gate resistance of 5 Ω. The load current is set to 44.6 A. The blue curve indicates the terminal voltage $V_{ds,PN}$, and as expected its value is unchanged during the turn-off switching transients. The red curve ($V_{ds,Kelvin}$) denotes the real voltage across the devices which peaks to 638 V under this above-mentioned conditions. The ringing frequency $f_0$ of $V_{ds,Kelvin}$ is calculated
to be 210.5 MHz based on the experiment waveform. At 600 V, the device’s junction capacitance is ~220 pF according to the datasheet (CPM2-1200-0025B), and its value is almost unchanged when the drain-source voltage is above 500 V. Correspondingly, the parasitic inductance of the module is calculated to be:

\[
L_{\text{loop low}} = \frac{1}{4\pi^2 f_0^2 C_{ds}} = 2.60 \text{ nH}
\]  

Figure 3.34. Experimental turn-off waveforms of lower MOSFET in the low parasitic module with 5 Ω external gate resistance.

Another experiment is carried out for the same module where the external gate resistance is further reduced to 0 Ω at the same DC bus voltage and load condition. Fig. 12 shows the waveforms. Compared with Figure 3.34, the voltage overshoot is increased from 638 V to 654 V. Still, the overshoot voltage is less than 9% of the DC bus voltage at a load current of 44.6 A.
Figure 3.35. Experimental turn-off waveforms of lower MOSFET in the low parasitic module with $0 \Omega$ external gate resistance.

3.2.5 Discussion about Thermal-mechanical Stress and Reliability

Figure 3.36 summarizes the values of the coefficient of thermal expansion (CTE) of commonly used materials in a package. The CTE mismatch between different materials and temperature gradients together will cause strain on each layer of material. This strain will lead to stress on the devices. If the stress exceeds the maximum allowable stress of the device’s material, a crack can develop and damage the device. For SiC devices, though the CTE is similar (3 ppm/K for Si and 4.3 ppm/K for 4H-SiC), Young’s modulus value of SiC material is almost three times that of Si (501 GPa in SiC compared to 162 GPa in Si). As a result, given the same strain and structure, more stress will be induced on SiC devices [55]. Meanwhile, the long-term fatigue of the solder will be another concern for SiC power module package. These two issues will be more severe for power modules with double-sided cooling as the devices are stressed from both sides.
In this design, the goal is to validate the low parasitic inductance design with this island structure. Therefore, traditional solder and AlN substrate are used. For the final version of this work, the stress can be alleviated by using proper substrates with proper CTE match [28], utilizing Molybdenum CTE buffer [34] or reducing the contact area with devices. In terms of the concern for long-term reliability, silver sintering and diffusion soldering are two promising solutions. In either method, the proposed structure can still be used to achieve low parasitic inductance.

3.3 Summary

In this chapter, the parasitic inductance extraction method in Q3D simulation is first verified by comparing with theoretical calculations at different frequencies for simple geometries. Then the case of paralleled wire bonds is simulated, and the effect of mutual inductance among different partial inductance is observed.

Considering the mutual inductance effect, a method to extract the lumped power loop inductance of a package is illustrated considering the device’s switching transients. It is observed that for a certain module, the power loop inductance is a time varying parameter: it is related to the
switching transients, and different values can be obtained for different switches. However, those differences are not large for the simulated package.

A real 3D planar-bond-all package is fabricated with 1200 V SiC MOSFETs and Schottky diodes from Cree. Dedicated kelvin drain-to-source voltage sensing is realized, and a double pulse test is built to extract the parasitic values experimentally. Experiment value shows a similar result as simulation value.

Then the design of a low parasitic inductance SiC power module with double-sided cooling is discussed in detail. By introducing the island layout design with vertical interconnection and implementing decoupling capacitors with PCB bus bar, the power loop inductance of the power module is effectively reduced.

Simulation result shows a 70% reduction in parasitic inductance compared with a previously designed baseline double-sided power module. Dedicated double pulse test boards are designed to extract the parasitic inductance of each module experimentally. From the experiment result, more than 60% parasitic inductance reduction is achieved with the new design compared to the baseline module.
Chapter 4
Understanding Middle Point Inductance’s Effect on Multi-Chips Power Module
Switching Transients

In the previous chapter, low parasitic inductance module design is realized which is important for high current power modules. Still, considering multiple chips in parallel, different scaling methods will affect the voltage spikes of the devices differently.

As discussed in the introduction section, the middle-point inductance $L_{\text{middle}}$ will be introduced for both split-scaled and identical-scaled power modules. It is important to understand the role of the middle point inductance before selecting the right scaling method. Therefore, the middle point inductance’s effect on power module packages with split scaling will be discussed in this chapter.

To start with, a dedicated split-scaled power module is designed for evaluating the effect of middle point inductor on a device’s switching transients. The module is characterized first at the beginning of the chapter. Afterward, the value of the middle-point inductance is varied to identify its effect on the switching performance of switches. Specifically, the overvoltage spikes and the switching loss of the devices are recorded at different values of $L_{\text{middle}}$.

4.1 Design and Characterization of a P-cell/N-cell Split-scaled Package

1200 V SiC trench MOSFETs and 1200 V SiC trench Schottky diodes from Rohm are used as the active switching devices. A phase leg configuration is packaged for evaluation of switching performance of the devices. For each switch, six MOSFETs are paralleled, and three Schottky diodes are used as the anti-parallel diodes. To investigate middle-point parasitic inductance’s effect on switching transients, split scaling is implemented.
4.1.1 Parasitic Inductance Optimization for the Multi-Chips Phase Leg Power Module with Split Scaling

P-cell/N-cell design methodology is adopted in the split scaling. To be specific, all the devices on each P-cell are paralleled and located close together. The remaining devices belonging to N-cell are placed in a similar way. Then, the current commutation loops for both P-cell and N-cell are optimized in terms of reducing the value of power loop inductance. The middle points of the P-cell and N-cell are connected together through direct-bonded-copper (DBC) level copper traces. In this design, six MOSFETs and three diodes constitute one P (N)-cell. Figure 4.1 shows the circuit schematic of the module. $L_{ds,P}$ and $L_{ds,N}$ represent the power loop inductance of the P-cell and N-cell respectively.

![Circuit schematic of the phase leg module](image)

*Figure 4.1. The circuit schematic of the phase leg module.*
The power loop inductances of each cell are optimized in the package layout to utilize the benefits of fast-switching SiC trench MOSFETs fully. Figure 4.2 illustrates the real physical layout of the package. For both P-cell and N-cell commutation loops, the MOSFETs and diodes are physically located close to each other. Decoupling capacitors are directly embedded inside the module as well to mitigate the external parasitic inductance’s effect.

![Figure 4.2. Physical package layout of the phase leg module.](image)

### 4.1.2 Simulation of Power Loop Inductance for Phase Leg Module with Split Scaling

The physical layout is exported to Ansys Q3D, and the values of the power loop inductances for each cell are extracted in a similar manner as discussed in Chapter 3. 4.11 nH is achieved for P-cell, and the power loop inductance’s value of N-cell is 3.44 nH. The current distributions of both cells at 100 MHz are illustrated in Figure 4.3 (a) and (b), respectively.
Figure 4.3. The current distribution of the phase leg module at high frequency.
As can be seen from the layouts of both cells, all the paralleled devices are scaled in the horizontal axis, and this package design is an example of one-dimension scaled power modules as defined in Figure 1.15.

One drawback of this one-dimension design is that the values of power loop inductance for each paralleled device are not the same. As a result, those paralleled devices will have different voltage spikes during the switching transients. Take N-cell layout of this package, for example, six MOSFETs (\(M_1\) to \(M_6\)) are paralleled as the lower active switch. \(M_1\) is located closer to the decoupling capacitors while \(M_6\) is further away as shown in Figure 4.4. The power loop inductances’ values of \(M_1\) to \(M_6\) are simulated as summarized in Table 4.1.

Figure 4.4. Variation of power loop inductances for paralleled devices.
Table 4.1. Comparison of power loop inductance for paralleled devices.

<table>
<thead>
<tr>
<th>Condition (@100MHz)</th>
<th>$M_1$</th>
<th>$M_2$</th>
<th>$M_3$</th>
<th>$M_4$</th>
<th>$M_5$</th>
<th>$M_6$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn off Loop Inductance during $di/dt$</td>
<td>4.58 nH</td>
<td>4.87 nH</td>
<td>5.09 nH</td>
<td>5.78 nH</td>
<td>6.32 nH</td>
<td>6.71 nH</td>
</tr>
</tbody>
</table>

As can be seen, $M_6$ has the largest power loop inductance, and its voltage spikes during turn-off will also be more severe than other devices under the same conditions. To verify this analysis, dedicated kelvin drain-to-source sensing pins are designed to measure the real voltage across the devices accurately during switching transients. More details will be elaborated further in the experiment verification section. Figure 4.5 shows the physical location of those sensing pins along with the location of gate signal pins.

![Figure 4.5. Location of gate signal pins and kelvin voltage sensing pins for the lower switch.](image)

Only the drain-to-source voltages of the lower switch (MOSFETs and the anti-parallel diodes) are measured. For all these signals, kelvin sensing is realized to obtain the real voltage across devices. Meanwhile, for both MOSFET and anti-parallel diodes, two different sensing points...
are monitored: one is closest to decoupling capacitor and the other most distant from decoupling capacitors as illustrated in Figure 4.5. The circuit diagram of the layout is shown in Figure 4.6, and the voltage sensing points are illustrated as well.

![Figure 4.6. The circuit schematic of the phase leg module with parasitic.](image)

4.1.3 Fabrication of the Phase Leg Module with Split Scaling

3D printed case is designed to press the DBC substrate in close contact with the baseplate. Thermal grease is used in between the bottom of the DBC and the top of the baseplate. Ten screws are used at different locations to fasten the DBC to the baseplate. Figure 4.5 shows the drawing of the 3D printed high-temperature plastic case. All the gate signals and voltage sensing signals are connected to the gate drive board, which is mounted right on top of the module as shown in Figure 4.7. Mounting holes are designed on the gate drive board to provide mechanical support. The
laminated dc-link bus bar is located on the right side of the module, and the middle point output pins are on the left side.

![Diagram of assembled module](image)

*Figure 4.7. Assembly of the phase-leg power module with split scaling.*

In terms of fabrication of the module, the devices, gate, and voltage sensing pins are soldered at the first place with 183 °C solders (63Sn/37Pb) as shown in Figure 4.8. Afterward, 5-mil wire bonds are used to realize interconnections between devices. The power terminal pins are soldered in the next step, and the plastic case is mounted together with the baseplate. In the final procedure, the module is encapsulated with NuSil R-2188 silicone potting. The first fabricated module is shown in Figure 4.9. In the first module, the power terminal pins are not drilled with holes for bus bar connection. However, all the electrical connections are the same with other modules. Therefore, this module is specifically used for evaluation of the static and dynamic characteristics of the SiC trench devices with split-scaled low-inductance package design.
Figure 4.8. Soldering of devices, gate drive and voltage sensing pins.

Figure 4.9. Fabricated phase leg module with split scaling.
4.1.4 Static Characterization of the Phase Leg Module with Split Scaling

Keysight B1505a curve tracer is used to characterize the static performance of the 1200 V SiC trench MOSFETs. The power module is sitting on top of the hot plate, and its temperature dependent characteristics are evaluated. Figure 4.10 shows the test set up for static characterization.

![Static Characterization of the Phase Leg Module with Split Scaling](image)

*Figure 4.10. The test set up for static characterization of the 1200 V SiC trench MOSFET module.*

As discussed previously, six MOSFETs are in parallel for each upper and lower switch. The output characteristics of the lower MOSFET switch are measured as shown in Figure 4.11. As can be seen, as temperature increases, the on-resistance is decreasing at a high gate voltage (20 V) while its value is increasing at lower gate voltages. This can be explained by the fact that the channel resistance $R_{on,channel}$ decreases at elevated temperatures and the drift region resistance $R_{on,drift}$ increases as temperature rises. When the gate voltage $V_{gs}=20$ V, the on-resistance $R_{ds,on}$ is mainly dominated by the drift region resistance. On the contrary, the channel resistance plays a more significant role at $V_{gs} = 10$ V or lower. Similar output characteristic is obtained for the upper MOSFETs.

Figure 4.12 shows the on-resistance change versus load current at different gate voltages.
Figure 4.11. Output characteristics of lower MOSFETs.

Figure 4.12. On-resistance $R_{ds, on}$ of lower MOSFETs at different load currents.
and junction temperatures. At $V_{gs} = 20 \, V$, $R_{ds,on}$ values remain constant across a wide range of load current. However, their values will change with load current at a gate voltage of 10 V. The upper MOSFETs have the same trend.

At a gate voltage of 20 V, the junction temperature dependent on-resistance values of upper and lower MOSFETs are summarized in Figure 4.13 and Figure 4.14. Second order polynomial equation is used for curve fitting the measured temperature dependent on-resistance values.

![Image](image.png)

*Figure 4.13. Temperature dependent $R_{ds,on}$ of upper MOSFETs.*

The transfer characteristic of the lower MOSFETs is measured as shown in Figure 4.15. $V_{ds}$ is set to 5 V in this case. As junction temperature increases, the threshold voltage is decreasing. In terms of transconductance value, it is increased slightly at elevated temperatures. Upper MOSFET reveals similar characteristic.
Figure 4.14. Temperature dependent $R_{ds,\text{on}}$ of lower MOSFETs.

Figure 4.15. The transfer characteristic of lower MOSFETs at different temperatures.
The leakage current of the 1200 V SiC trench MOSFET is also tested up to 900 V at different junction temperatures as indicated in the following figures. The lower MOSFETs have a larger leakage current compared to upper MOSFETs as can be seen in Figure 4.16 (a) and (b).

![Figure 4.16. Characterization of leakage current.](image)

Meanwhile, the body diode of the MOSFETs are also evaluated at various junction temperatures with $V_{gs} = 0$ V. Figure 4.17 shows the characteristics of lower MOSFETs. Below 50 A, the forward characteristic of its body diode shows a negative temperature coefficient. Therefore, the body diodes are not suitable for paralleling in terms of current sharing.

At room temperature, the lower MOSFETs’ body diode is also characterized at various gate voltages as shown in Figure 4.18. The forward curve with $V_{gs} = 0$ V is shown in the blue line while the forward curve with $V_{gs} = -5$ V is drawn in red. Obviously, the curve shifts to the right as the gate voltage decreases as summarized in Table 4.2. Considering without anti-parallel diodes, the load current will go through the body diodes during dead time. Thus, more conduction loss will be induced in the body diode if a negative gate voltage is applied. In the case where anti-parallel diodes are used, a negative gate voltage will help to prevent body diode conduction.
Figure 4.17. Characteristics of lower MOSFETs’ body diode at different junction temperatures.

Figure 4.18. Room temperature characterization of lower MOSFETs’ body diode at different $V_{gs}$. 
Table 4.2. Parameter shift of body diode at different gate voltages.

<table>
<thead>
<tr>
<th>$V_{gs}$</th>
<th>$V_{th}$</th>
<th>$R_{diod}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 V</td>
<td>1.37 V</td>
<td>10.0 mΩ</td>
</tr>
<tr>
<td>-5 V</td>
<td>2.37 V</td>
<td>11.4 mΩ</td>
</tr>
</tbody>
</table>

The anti-parallel diodes are also characterized. As discussed previously, three devices are paralleled as one switch. The output characteristics of the lower paralleled diodes at different junction temperatures are shown in Figure 4.19. The diode is modeled as:

$$V_{ak} = V_{th_{model}} + R_{diod} \cdot I_{ak}$$ (7)

The real threshold voltage of the diodes is $V_{th}$, and $V_{th_{model}}$ is only used to characterize the diode in two segments. $R_{diod}$ is mainly from the drift region resistance, and it is measured at 30 A in this case. The threshold voltage variations and resistance changes versus junction temperatures are shown in Figure 4.20 and Figure 4.21. As expected, negative temperature coefficient is shown for threshold voltage, while the resistance shows a different trend.

Figure 4.19. Lower switch anti-parallel diode characteristics at different $T_j$. 
Figure 4.20. Resistance change of lower switch anti-parallel diode over $T_{j}$.

Figure 4.21. Threshold voltage change of lower switch anti-parallel diode over $T_{j}$. 
At this point, all the junction temperature dependent static characteristics of the 1200 V SiC trench MOSFETs and 1200 V trench Schottky diode have been evaluated. To further manifest the benefits of trench devices, the junction capacitance of the devices is tested. The value of the junction capacitance will affect the phase leg module’s switching performance. Therefore, it is meaningful to characterize these values before the pulse tests.

Figure 4.22 shows the capacitance test unit of the curve tracer. Three female banana connectors are ready for outside connections. Factory fixtures are optimized for testing TO-packaged devices only. For the specific power modules, the wire connections cannot fit the factory fixtures. To obtain an accurate value of the junction capacitance of the devices, a special fixture is designed to compensate the connection wires.

![Diagram of capacitance measurement unit of the curve tracer.](image)

*Figure 4.22. Capacitance measurement unit of the curve tracer.*

To be specific, a rectangle piece of phenolic board is cut. Then three holes are drilled with male banana connectors screwed inside. One side of the male banana connectors are mated with
the curve tracer unit, and the other side is soldered to separate magnetic wires representing gate, drain source as shown in Figure 4.23.

![Figure 4.23. A fixture in connection with the curve tracer.](image)

Afterward, the magnetic wires are bent to fit the power module’s terminals and the wires’ positions are fixed with tape. Open and short calibrations are implemented to compensate the impedance introduced by these connection wires. Figure 4.24 shows these two compensation connections. A piece of copper sheet is used for shorting the wires as indicated in Figure 4.24 (b). The power module is finally connected to the fixture for testing as shown in Figure 4.25.

![Figure 4.24. Compensation of the connection wires.](image)

(a) Open compensation  
(b) Short compensation
The nonlinear junction capacitance versus drain-to-source voltage curve of the SiC trench MOSFETs is shown in Figure 4.26. Both upper and lower MOSFETs have identical capacitance values. At a dc voltage of 600 V, the energy-equivalent capacitor value is calculated to be 807.62 pF. Considering the on-resistance value of 7.68 mΩ at room temperature, this module is more suitable for high current applications.

Similarly, the 1200V SiC trench Schottky diode is tested using the same method. The testing result is shown in Figure 4.27 for both upper and lower anti-parallel diodes. 761.92 pF is obtained for the energy-equivalent capacitor value at 600 V.
Figure 4.26. MOSFETs nonlinear junction capacitance versus drain-to-source voltage.

Figure 4.27. Schottky diode nonlinear junction capacitance versus drain-to-source voltage.
4.1.5 Comparison of Kelvin and Non-kelvin $V_{ds}$

All the static characteristics of the devices have been evaluated in the previous section. In the following section, the switching losses from different voltage measurement points are compared first. Then the temperature dependent switching loss of the power module is evaluated at different gate resistors. Since the module will be used in a boost converter from 300 V to 600 V, the dc-link voltage of the double pulse test is selected to be 600 V and the load current is varied up to 120 A.

To start with, the gate drive board is mounted on top of the power module as shown in Figure 4.28. Standard BNC connectors are positioned on the gate drive board for kelvin $V_{ds}$ measurement. Two pairs of twisted wires are located on the right for connections with dc-link capacitors.

![Gate Drive Board](image)

*Figure 4.28. Real assembly picture of the power module with gate drive board.*
The power module is then connected to the power stage board for double pulse test as shown in Figure 4.29. A 15 mΩ coaxial shunt is mounted on the power stage board for measuring the drain current of the active switch. Ceramic and film capacitors are put close to the power terminals of the module. Short circuit protection circuit presented in [56] is inserted in between the dc-link capacitors and the film decoupling capacitors.

![Double pulse test setup for #1 module.](image)

**Figure 4.29. Double pulse test setup for #1 module.**

The circuit diagram of the double pulse test is shown in Figure 4.30. The circuit is configured such that the lower MOSFETs are the active switching devices. The drain current of lower MOSFETs is measured through the on-board coaxial shunt. As discussed previously, the real device voltage is accessible through the kelvin connection as shown in Figure 4.5. Therefore, the kelvin drain-to-source voltage $V_{ds,kelvin}$ can be used to calculate switching loss. For conventional double pulse test setup for commercial power modules, the kelvin voltage is not available.
Consequently, the voltage across output point and negative bus ($V_{ON}$) shown in Figure 4.30 is usually used to calculate switching loss. This voltage cannot represent the real voltage across the devices since some parasitic inductances exist in between the device and the measuring points. These parasitic inductances will introduce extra voltages during switching transients. For the purpose of verifying the accuracy of the conventional switching loss calculation with non-kelvin drain-to-source voltage $V_{ds,\,non\,kelvin}$, this voltage is also measured, and the loss calculated from $V_{ds,\,non\,kelvin}$ is compared with the switching loss from $V_{ds,\,kelvin}$.

![Circuit diagram of the whole double pulse test set up](image)

*Figure 4.30. Circuit diagram of the whole double pulse test set up.*

The turn-off and turn-on switching waveforms are shown in Figure 4.31 and Figure 4.32 respectively for both kelvin and non-kelvin cases. The load current is 120 A and the dc-link voltage is 600 V. The external gate resistor is selected to be 5 Ω.
Figure 4.31. Experimental turn-off switching waveforms at 600 V, 120 A and $R_{g,ext} = 5 \, \Omega$. 

(a) Non-kelvin $V_{ds}$

(b) Kelvin $V_{ds}$
Figure 4.32. Experimental turn-on switching waveforms at 600 V, 120 A and $R_{g, ext} = 5 \, \Omega$. 
The current is shifting from the lower MOSFETs to the upper anti-parallel diode during turn-off. Therefore, the drain current of lower MOSFETs has negative slew rate. As a result, the kelvin voltage $V_{ds_{\text{kelvin}}}$ is larger than $V_{ds_{\text{non-kelvin}}}$ during turn-off due to the extra parasitic inductance in between. This is verified experimentally as shown in Figure 4.31 where $V_{ds}$ shoots to ~900 V in the kelvin sensed case compared to ~750 V from the non-kelvin measurement. Consequently, the turn-off switching loss is larger if it is calculated from $V_{ds_{\text{kelvin}}}$.

On the other hand, the kelvin sensed voltage is smaller during turn-on currents as the slew rate of drain current changes to a positive value. Figure 4.32 shows the comparison of voltage waveforms during turn-on. As can be seen, the shape of $V_{ds}$ is changed if the voltage is sensed from the kelvin sensing pins, and the voltage drops faster compared to $V_{ds_{\text{non-kelvin}}}$. Subsequently, the switching loss calculated from kelvin-sensed voltages is smaller.

At $R_{g_{\text{ext}}} = 10 \, \Omega$, the switching losses are compared for calculations from different voltage sensing points as shown in Figure 4.33. It can be seen though the turn-on and turn-off loss values are different; the total losses remain the same over a wide range of load current.

![Figure 4.33. Switching loss comparison of kelvin and non-kelvin voltages with $R_{g_{\text{ext}}} = 5 \, \Omega$.](image)
Another phenomenon observed from Figure 4.32 is that the kelvin sensed voltage $V_{ds,\text{kelvin}}$ during turn-on is much cleaner than the voltages from $V_{ds,\text{nonkelvin}}$. After $V_{ds}$ reaches zero, the non-kelvin voltage’s ringing still exists and the waveform is noisy. However, the kelvin-sensed voltage is noise-free, and only the on-state voltage is revealed. In terms of setting the blanking time of gate drive short circuit protection, the blanking time with non-kelvin sensing is larger than kelvin sensed voltage for a given protection value.

To verify this, the DESAT feedback signal $V_{DESAT}$ to protection circuit is measured in double pulse test with only N-cells. As shown in Figure 4.34, a dedicated probe adaptor is used to ensure measurement accuracy. At a bus voltage of 150 V, the DESAT signals and the turn-on switching waveforms of the switch at 0 A and 50 A are demonstrated in Figure 4.35 and Figure 4.36 respectively. In both cases, it is observed that under the same conditions, the DESAT feedback signal with kelvin-sensed voltage is clean while the signal from non-kelvin $V_{ds}$ has significant ringing. With 0.7 V as the protection threshold, the blanking time setting difference is 1.36 us at 0 A, and increases to 2.66 us at 50 A.
Figure 4.35. DESAT protection signal and turn-on waveforms at 150 V/50 A.

Figure 4.36. DESAT protection signal and turn-on waveforms at 150 V/0 A.
During turn-on transients, the DESAT signal experiences four intervals. The equivalent circuit diagram is drawn and analyzed in the following section.

a) Off state

When the gate input signal is low, the DESAT signal is pulled down internally by the gate driver, and the equivalent circuit is shown in Figure 4.37 (a).

b) Turn-on delay period

Once the gate input signal is high, the pull-down function is disabled. Then the DESAT pin will start to be charged by the 20 V power supply through $R_1$, $R_2$, $R_3$ and $C$ as shown in Figure 4.37 (b). This period is short, and the pull-down device’s turn-off also takes some time. Correspondingly, the voltage of DESAT sense terminal is almost unchanged.

c) Turn-on di/dt and dv/dt periods

In both di/dt and dv/dt periods, the voltage on the active device is dropping from dc-link voltage to on-state voltage. The diode in the DESAT sensing circuit is still blocking $V_{ds}$ of the active device in the transients, and can be modeled as a junction capacitor as shown in Figure 4.37 (c). However, the active device’s dv/dt will cause current to flow through the junction capacitor of
the blocking diode. This current, as indicated in the orange line, will introduce a negative voltage on the DESAT sensing point. This explains the dips observed in Figure 4.35 and Figure 4.36.

d) Ringing period and on state

After the dv/dt period comes the ringing period where lot of oscillations are occurring in the drain current of the lower MOSFET and $V_{ds}$ of the upper MOSFET. The current ringing will cause oscillations on the DESAT signal as well if the DESAT signal is coming from the non-kelvin $V_{ds}$. The ringing on DESAT signal will require a longer blanking time. In terms of DESAT protection, it will slow down protection speed. However, if the DESAT signal is from kelvin $V_{ds}$, there is less noise, and a much shorter blanking time is needed as discussed previously. Figure 4.38 shows the equivalent circuits for the DESAT detection circuits during ringing and on-state periods. The difference would be the extra parasitic inductance introduced in the power loop. Regarding selection of DESAT sensing point, kelvin $V_{ds}$ is preferred as it gives the least noise.

![Figure 4.38: Circuit diagram comparison of DESAT detection circuit during ringing period.](image)

Theoretically, the blanking time can be set as short as the turn-on delay time if the kelvin $V_{ds}$ is used as shown in Figure 4.36. In real operations, the sensing circuit will have some magnetic
couplings with the power loop. This coupled mutual inductance will also cause some noise in the DESAT signals. This noise will be large especially at high current as indicated in Figure 4.35. Therefore, depending on the layout, the blanking time should be selected wisely.

4.1.6 Temperature Dependent Switching Performance Evaluation of the Power Module

Only the kelvin voltage is used for temperature dependent switching loss characterization of the 1200 V SiC trench MOSFETs module. The gate resistor values are varied, and the junction temperature changes from 25°C to 125°C.

Figure 4.39 shows the turn-on switching waveforms of lower MOSFETs at various $T_j$ with $R_{g,ext} = 5 \Omega$. As temperature increases, gate threshold voltage $V_{th}$ will decrease and transconductance $g_m$ will increase. During the current rise time, the drain current rises more quickly at higher $T_j$ owing to a faster slew rate of transconductance as temperature increases as indicated in the equation below:

$$t_{ir} = R_g C_{iss} \ln \left( \frac{V_{cc} - V_{th}}{V_{cc} - V_{miller}} \right) = R_g C_{iss} \ln \left( \frac{V_{cc} - V_{th}}{V_{cc} - \left( V_{th} + \frac{I_L}{g_m} \right)} \right)$$

(8)

Considering the power loop inductance, the voltage across the device will also drop more quickly. Therefore, the switching loss during current rise time will be smaller as $T_j$ increases. During voltage falling period, the gate miller plateau voltage decreases as temperature increases. As a result, the gate current is larger and $V_{ds}$ drops more quickly. Therefore, the turn-on loss during voltage fall period is also smaller at higher junction temperatures. Correspondingly, the total turn-on switching loss will decrease as $T_j$ is increased. Figure 4.40 illustrates the turn-on switching loss results at different combinations of $T_j$, $R_{g,ext}$ and load current. At higher junction temperature, the turn-on switching loss is indeed decreasing which validates the previous analysis. Meanwhile, the turn-on loss $E_{on}$ is reduced with lower values of gate resistor as expected.
Figure 4.39. Turn-on waveforms at different junction temperatures with $R_{g,\text{ext}} = 5 \, \Omega$.

Figure 4.40. Turn-on loss data at different $T_j$, $R_{g,\text{ext}}$ and load current.
The turn-off waveforms at various $T_j$ with $R_{g,ext} = 5 \, \Omega$ and $I_{load} = 120 \, A$ are shown in Figure 4.41. The turn-off loss is mainly contributed by the voltage rise and current fall period as indicated in Figure 4.41. During the voltage rise period, the gate voltage is almost constant and stays at $V_{\text{miller}}$. The miller plateau voltage is mainly determined by load current and junction temperature. At the same load condition, $V_{\text{miller}}$ will be smaller as junction temperature increases as can be seen from the transfer characteristics shown in Figure 4.15. Therefore, the gate current will be smaller during the voltage rise period as $T_j$ increases. Consequently, the switching loss during voltage rise period $E_{\text{off},VR}$ will increase at elevated $T_j$ as the overlap time is larger.

During current fall period, the gate voltage is changing from $V_{\text{miller}}$ to threshold the voltage $V_{th}$ with a time constant $R_g \cdot C_{gs}$ considering a first order system in the gate loop. Both $V_{\text{miller}}$ and $V_{th}$ will decrease at higher $T_j$. However, based on the tested transfer characteristics, $|V_{\text{miller}} - V_{th}|$ will decrease as $T_j$ builds up. Correspondingly, the current fall time will be smaller as indicated in the following equation:

$$t_{if} = R_g C_{iss} \ln \left( \frac{V_{\text{miller}}}{V_{th}-V_{ee}} \right) = R_g C_{iss} \ln \left[ \frac{(V_{th}+I_L g_m)}{V_{th}-V_{ee}} \right]$$

(9)

Moreover, as can be seen from the transfer characteristics in Figure 4.15, the current slew rate will be a little bit faster as $T_j$ builds up especially during the quadratic region. Thus, the channel current slew rate will increase at higher junction temperatures. Combining the reduced current fall time together with the higher channel current slew rate, the resulting overlap loss during turn-off current fall time $E_{\text{off,CF}}$ will be smaller.

The total turn-off loss consists of $E_{\text{off},VR}$ and $E_{\text{off,CF}}$. $E_{\text{off},VR}$ is increasing while $E_{\text{off,CF}}$ is decreasing as $T_j$ elevates. Therefore, the total turn-off loss can be either positive or negative temperature coefficient. Figure 4.42 shows the experimental turn-off loss data at different conditions. For this device, the turn-off loss is decreasing as junction temperature increases.
Figure 4.41. Turn-on waveforms at different junction temperatures with $R_{g,ext} = 5 \text{ }\Omega$.

Figure 4.42. Turn-off loss data at different $T_j$, $R_{g,ext}$ and load current.
4.1.7 Parasitic Inductance Extraction of the Split-scaled Module

The parasitic inductance of the module is also extracted and compared with simulation results. To obtain the value of parasitic inductance, only the N-cell is connected to the double pulse board, and circuit diagram is drawn in Figure 4.43. $V_{PN}$ represents the bus voltage across the terminal of the power module. $V_{ds1}$ and $V_{ds2}$ are two kelvin-sensed drain-to-source voltages. Since six MOSFETs are paralleled in a row, $V_{ds1}$ represents the voltage of devices closest to the decoupling capacitors while $V_{ds2}$ is the voltage of device most far away from decoupling capacitors. Their physical locations are shown in Figure 4.5.

![Circuit diagram of the N-cell double pulse test set up.](image)

The same parasitic inductance extraction method discussed in chapter 3 is used. The voltage across $V_{PN}$ is compared with the real voltage across devices, and the parasitic inductance values are derived from the voltage difference and drain current slew rate measured from coaxial shunt. To ensure the channel $di/dt$ is dominating during the turn-off process, a large external gate resistor (10Ω) is selected, and the device is turned off at a large load current of 138 A.

Figure 4.44 illustrates the turn-off waveforms of terminal voltage $V_{PN}$, kelvin sensed voltage $V_{ds1}$ and load current $I_{ds}$. The current slew rate is calculated to be -3.18 A/ns, and the
voltage difference is 19.09 V. The power loop parasitic inductance obtained from $V_{ds1}$ is calculated to be:

$$L_{ds1} = \frac{19.09 \text{ V}}{(3.18 \text{ A/ns})} = 5.15 \text{ nH}$$  \hspace{1cm} (10)

![Figure 4.44. Turn off waveforms for extraction of $L_{ds}$ from $V_{ds1}$.](image)

Compared to the simulation values summarized in Table 4.1, this value is in between the parasitic inductance value of $M_1$ and that of $M_6$; but it is closer to the value of $M_1$. This is reasonable because all the MOSFETs ($M_1$ to $M_6$) are conducting the current, and the extracted value cannot represent the parasitic inductance value considering a single device. Therefore, the extracted value is between the parasitic inductance value of $M_1$ (4.58 nH) and that of $M_6$ (6.71 nH). Moreover, since the sensing pins are located physically closer to $M_1$, the extracted value is more approaching the parasitic value of $M_1$. 
Similarly, the power loop parasitic inductance is also extracted from $V_{ds2}$ as shown in Figure 4.45. The voltage spike is a little bit larger in the case of $V_{ds2}$, and the extracted value is:

$$L_{ds2} = 20.97 \text{ V} / (3.19 \text{ A/ns}) = 6.62 \text{ nH}$$

(11)

![Figure 4.45. Turn off waveforms for extraction of $L_d$ from $V_{ds2}$.](image)

The value of $L_{ds2}$ is also in between the values of $M_1$ and $M_6$, and it is closer to the value of $M_6$ since the sensing pins are adjacent to $M_6$.

4.2 **Evaluation of Middle Point Inductor’s Effect on Device’s Switching Performance**

As can be seen in Figure 4.1 and Figure 4.6, the middle-point inductance $L_{middle}$ is introduced because of the interconnection between the middle points of N-cell and P-cell. In the following section, the effect of $L_{middle}$ is investigated for split-scaled multiple chips power module.
4.2.1 *Observed Switching Transients with Multiple Ringing*

Figure 4.43 shows the circuit diagram with N-cell connected only. To measure the drain current, the embedded decoupling capacitors inside the power module are not assembled. During the turn-off ringing period, the high-frequency equivalent circuit is drawn in Figure 4.46 assuming the on-board decoupling capacitor’s voltage is constant and ignoring the parasitic inductances between paralleled devices. A single resonant frequency is obtained which is determined by the junction capacitance of the paralleled MOSFETs and the lumped power loop inductance.

![Circuit Diagram](image)

*Figure 4.46. High-frequency equivalent circuit of N-cell DPT during turn-off ringing period.*

The experiment turn-off switching waveform of kelvin drain-to-source voltage, drain current, and the gate voltage is shown in Figure 4.47. The load current is 100 A, dc-link voltage is 600 V, and the external turn-off gate resistor’s value is 5 Ω. The value of the lower MOSFETs’ junction capacitor is nearly flat above 500 V. Referring to Figure 4.26, the junction capacitance value of lower MOSFETs is obtained to be 644.9 pF at 600 V. The ringing frequency of $V_{ds}$ is around 22 MHz, and the power loop inductance $L_{ds}$ is calculated to be:
\[ L_{ds,N} = \frac{1}{4\cdot \pi^2 \cdot f_0^2 \cdot C_{ds}} = \frac{1}{4\cdot \pi^2 \cdot (22 \cdot 10^6)^2 \cdot 644.9 \cdot 10^{-12}} = 81.15 \text{ nH} \]  
\[ (12) \]

In the next step, both P-cell and N-cell are connected to the power stage board for double pulse test. The experiment conditions are the same as the N-cell double pulse test. The turn-off waveforms of the lower MOSFETs’ kelvin drain-to-source voltage, drain current and gate voltage are shown in Figure 4.48. Meanwhile, the kelvin voltage waveform of the lower anti-parallel diode is illustrated in the orange line. As can be seen, for both voltage waveforms of lower MOSFET and lower anti-parallel diode, two resonant frequencies are observed. One is around 24.27 MHz and the other is around 2 MHz. This multiple-frequency ringing is also observed in the drain current waveform. At another load condition of 120 A, this phenomenon is also observed as shown in Figure 4.49. The values of these resonant frequencies are the same at both load conditions.
Figure 4.48. 100 A turn-off waveforms of lower MOSFETs with P, N-cells connected together.

Figure 4.49. 120 A turn-off waveforms of lower MOSFETs with P, N-cells connected together.
4.2.2 Analysis of $L_{\text{middle}}$

To determine the cause of this multiple frequency ringing, the equivalent circuit diagram of the double pulse test with P, N cells connected is shown in Figure 4.50. On the load inductor side, its equivalent parallel capacitor is considered. During lower MOSFETs’ turn-off ringing period, both the lower MOSFETs and lower anti-parallel diodes are modeled as a capacitor with a single value. The upper MOSFETs and anti-parallel diodes are modeled as a resistor at high frequency since the body diode of the MOSFET and the anti-parallel diodes would together conduct the load current during the ringing period. Other parasitic inductances are also modeled. As the multiple-frequency ringing can potentially be contributed from the decoupling capacitor, the decoupling capacitor is also considered in the circuit diagram. The dc-link capacitor is shorted at high frequency. Meanwhile, the middle-point inductance is also shown in red.

![High-frequency equivalent circuit of the double pulse test during turn-off ringing period with P, N cells connected.](image)

Figure 4.50. High-frequency equivalent circuit of the double pulse test during turn-off ringing period with P, N cells connected.
If the decoupling capacitor’s voltage is not stable, a multiple-frequency ringing phenomenon can occur. Therefore, the voltage across the decoupling capacitor is first measured during the switching transients. Figure 4.51 shows the switching waveforms of lower MOSFETs’ voltage, drain current, gate voltage and the voltage of decoupling capacitors. The decoupling capacitor’s voltage remains a constant value during the turn-off switching transients. Therefore, the decoupling capacitor can be shorted in the high-frequency circuit diagram, and it is not the real cause of the multiple-frequency ringing.

![Graph showing waveforms](image)

*Figure 4.51. 120 A turn-off waveforms of lower MOSFETs and voltage across decoupling capacitor with P, N-cells connected together.*

Compared to the double-pulse test circuit diagram with only N-cell connected, one difference is the existence of middle-point inductance $L_{middle}$ in the P-Cell/N-cells case. To discover its effect, the equivalent circuit is analyzed in the frequency domain. Figure 4.52 shows
the equivalent circuit during ringing period. The excitation for this impedance network is the lower MOSFETs’ channel di/dt. It will generate current excitations at various frequencies. Correspondingly, these excitations will cause voltage ringing of various frequencies on both lower MOSFETs and lower anti-parallel diodes. The ringing frequencies are dominated by the network’s impedance. Therefore, the impedance of $V_{ds\_MOS}$ over $i\_channel$ is studied over a wide range of frequencies.

![Equivalent circuit during lower MOSFET turn-off ringing period](image)

**Figure 4.52. Equivalent circuit during lower MOSFET turn-off ringing period.**

To implement the frequency analysis, accurate values of all the circuit parameters are needed. Previously, the power loop inductance of the N-cell is extracted to be 81.15 nH based on the N-cell switching test. Similarly, the P-cell double pulse test is implemented. After the upper MOSFET is turned on, the power loop parasitic inductance of P-cell will resonate with the junction capacitor of the lower anti-parallel. Figure 4.53 shows the waveform of the lower anti-parallel diode during the upper MOSFET’s turn-on with a load of 100 A.
As can be seen, the ringing frequency is 21.63 MHz. Consequently, the power loop inductance of P-cell is extracted to be:

$$L_{ds_P} = \frac{1}{4\pi^2f_0^2C_{ds}} = \frac{1}{4\pi^2(21.63 \times 10^6)^2 \times 663.8 \times 10^{-12}} = 81.60 \text{ nH}$$ (13)

The equivalent parallel capacitance value of the load inductor is measured from impedance analyzer, and 3.5 pF is obtained. The middle-point inductance is formed by the DBC-level copper trance, and the value of the middle-point parasitic inductance is extracted in Ansys Q3D based on its geometry. Figure 4.54 illustrates the location of sink and source for extraction of $L_{middle}$. At high frequency, the extracted value of $L_{middle}$ is 5.47 nH. The parasitic inductance in between the on-board decoupling capacitor and dc-link capacitor is assumed to be 20 nH.
With all the circuit parameters ready, the impedance network is built in LTspice as shown in Figure 4.55. To mimic the channel $di/dt$, an ac current excitation is in parallel with the junction capacitor of the lower MOSFET. The impedances of $Z_{\text{Mos}} = V_{ds,\text{MOS}}/i_{\text{channel}}$ is obtained as shown in Figure 4.56. As can be seen, two resonant frequencies are observed. One is at $f_1 = 21.85 \, MHz$; the other one is $f_2 = 29.96 \, MHz$. The phases of these two signals are 0 and $-\pi/2$ respectively. The resulting signals will have frequencies of $f_D$ and $f_C$ expressed as:

$$f_D = \frac{f_2 - f_1}{2} = \frac{29.96 - 21.85}{2} = 4.06 \, MHz$$

(14)

$$f_C = \frac{f_1 + f_2}{2} = \frac{29.96 + 21.85}{2} = 25.91 \, MHz$$

(15)
Figure 4.55. LTspice simulation schematics.

Figure 4.56. The impedance of $V_{ds,MOS}$ over $i_{channel}$ at various frequencies.
The resulting frequencies \( f_D \) and \( f_C \) in simulation are close to the observed two ringing frequencies in experiment (\( f_1 \approx 25 \, MHz \), and \( f_2 \approx 2 \, MHz \)). However, both \( f_D \) and \( f_C \) are larger than the experiment values. The difference can be explained by the discrepancy of the distribution of power loop inductance in simulation and experiment. To be specific, \( C_1 \) (\( C_2 \)) is the percentage of power loop inductance from the middle point to negative (positive) bus over the total power loop inductance. In the simulation, an even distribution of \( L_{ds,N} \) is assumed from the middle point; therefore, \( C_1 \) and \( C_2 \) are set to 0.5. However, this even distribution does not necessarily represent the real experiment setup. Take the N-cell module layout for example; the distance from middle point to negative bus is longer than the distance from middle point to positive bus as shown in Figure 4.3 (b). Therefore, \( C_1 > C_2 \) can be obtained. To evaluate the loop inductance distribution’s effect on the impedance network, another simulation is implemented at different values of \( C_1 \) as shown in Figure 4.57.

\[ \text{Figure 4.57. The impedance of } V_{ds, MOS} \text{ over } i_{channel} \text{ at various frequencies and } C_1. \]
It can be observed that as $C_1$ increases (meaning the percentage of middle point to negative inductance over total loop inductance is increasing), $f_2$ will decrease and $f_1$ is unchanged. Consequently, both $f_D$ and $f_C$ will be smaller. In a real circuit, $C_1$ is larger 0.5 because the distance from output terminal to the negative bus is larger than that from output terminal to the positive bus. This helps to explain discrepancies between experiment and simulation results.

From the impedance network analysis, it is concluded that the middle-point inductance $L_{\text{middle}}$ is the cause of the drain-to-source voltage’s multiple-frequency ringing. This multiple-frequency ringing can potentially affect the switching transients. Figure 4.58 shows another simulation of $Z_{\text{MOS}}$ at different values of $L_{\text{middle}}$. As $L_{\text{middle}}$ increases, $f_2$ is decreasing but $f_1$ is slightly increasing. When $L_{\text{middle}}$ is above a certain value, $f_1$ and $f_2$ almost overlap and a single frequency is obtained. Considering the case of large value of $L_{\text{middle}}$, the current in $L_{\text{middle}}$ will remain its previous value during the switching transients. Accordingly, $L_{\text{middle}}$ can be treated as open circuit at high frequency. Then a single frequency will be obtained for N-cell, which is solely determined by the power loop parasitic inductance and the junction capacitance of the MOSFETs.

![Figure 4.58. The impedance of $V_{ds,\text{MOS}}$ over $i_{\text{channel}}$ at various frequencies and $L_{\text{middle}}$.](image)
Based on previous analysis, different values of middle-point inductance have different impacts on the switching transients. Therefore, its effect on voltage spikes and switching loss will be extensively investigated in the following sections considering different conditions.

4.2.3 Power Module Modification for Evaluating $L_{\text{middle}}$

Figure 4.59 demonstrates the dedicated DBC substrate for fabrication. The copper trace connecting the two middle points are cut out. Afterward, two output pins are soldered to the middle point of each cell. The middle-point inductor will be connected outside for easier variation of the value of $L_{\text{middle}}$. The remaining layout and components are the same as the power module characterized previously. The final assembled module is shown in Figure 4.60 and Figure 4.61 with gate drive board installed.

*Figure 4.59. Dedicated DBC substrate for evaluating $L_{\text{middle}}$'s effect on switching transients.*
Figure 4.60. Fabricated module for evaluating the effect of $L_{\text{middle}}$ on switching transients.

Figure 4.61. Fabricated module with gate drive board for evaluating the effect of $L_{\text{middle}}$ on switching transients.
4.2.4 Comparison of Switching Transients at Different $L_{\text{middle}}$ with Large $L_{ds}$

The fabricated module is first connected to the double pulse test board with N-cell only. The lower MOSFETs’ turn-off waveforms are shown in Figure 4.62. Like the previous module, a single resonant frequency is observed (19.81 MHz). The power loop inductance is calculated to be around 95 nH. This represents a case with a large value of power loop inductance.

![Turn-off waveforms of lower MOSFETs with N-cell connected only.](image)

Figure 4.62. Turn-off waveforms of lower MOSFETs with N-cell connected only.

Then both P-cell and N-cell are connected, and the middle-point inductor is varied. Figure 4.63 demonstrates three different middle-point inductor cases: one uses a copper sheet for connecting the two middle points while the other two use short wires for interconnection. The values of these parasitic inductances are 10 nH, 50 nH and 160 nH respectively. The length of the wires is adjusted, and more values (650 nH and 1.6 uH) are obtained for the purpose of comparison at different values of $L_{\text{middle}}$. 
(a) Middle points connected by copper sheet

(b) $L_{\text{middle}} = 50 \, nH$

(c) $L_{\text{middle}} = 160 \, nH$

Figure 4.63. Different values of $L_{\text{middle}}$. 
Before implementing the switching tests at different values of $L_{\text{middle}}$, the temperature dependent switching test is first carried out with $L_{\text{middle}} = 10\, nH$ (two middle points connected by copper sheet). At different load currents and gate resistors, the lower MOSFET is actively switched and the voltage spikes of lower MOSFET and lower anti-parallel diodes are recorded as shown in Figure 4.64 and Figure 4.65 respectively. The bus voltage is 600 V.

In both figures, the maximum voltage spikes due to lower MOSFET’s turn-off will build up with increased load current and reduced gate resistor. For this specific case with $L_{\text{middle}} = 10\, nH$, the voltage spikes of lower MOSFETs are larger than that of lower anti-parallel diodes at high load current. Additionally, it can be seen that the turn-off voltage spikes do not change over a wide range of junction temperature. Therefore, to save the test time, the switching transient comparison with different values of $L_{\text{middle}}$ is only conducted at room temperature.

\[ V_{ds\,\text{max}} \] at Various Current and Temperature

\[ \text{Current}(A) \]
\[ \text{Voltage}(V) \]

\[ R_g=5 \]
\[ R_g=7.5 \]
\[ R_g=10 \]

\textbf{Figure 4.64. Voltage spikes of lower MOSFETs at different gate resistor and temperature with } L_{\text{middle}} = 20\, nH. \]
During lower MOSFET’s turn-off, the lower MOSFETs and lower anti-parallel diodes will experience extra voltage stress during the transients. On the other hand, voltage spikes will also be induced on the lower MOSFETs and anti-parallel diodes during upper MOSFET’s turn-on process. For both cases, the value of middle-point inductance is varied (10 nH, 50 nH, 160 nH, 650 nH and 1600 nH) and the switching transients are compared.

a) Lower MOSFET turn-off

Figure 4.66 to Figure 4.69 exhibit the experimental turn-off waveforms of lower MOSFET’s gate voltage, kelvin-sensed $V_{ds}$, drain current and lower anti-parallel diode’s voltage at different values of $L_{middle}$ with $R_{g,off} = 7.5$ Ω. It can be observed that the ringing frequency of $f_2$ does change with the value of $L_{middle}$: $f_2$ drops from 1.79 MHz to 0.72 MHz as $L_{middle}$ increases from 50 nH to 650 nH. At $L_{middle} = 1600 nH$, a single resonant frequency of 20.45 MHz is observed which indicates a decouple of P-cell with the N-cell.
Figure 4.66. Lower MOSFET turn-off switching waveforms at $L_{\text{middle}} = 50\, \text{nH}$.

Figure 4.67. Lower MOSFET turn-off switching waveforms at $L_{\text{middle}} = 160\, \text{nH}$. 
Figure 4.68. Lower MOSFET turn-off switching waveforms at $L_{\text{middle}} = 650 \, \text{nH}$.

Figure 4.69. Lower MOSFET turn-off switching waveforms at $L_{\text{middle}} = 1600 \, \text{nH}$. 
The turn-on switching loss result of the lower MOSFET is shown in Figure 4.70 at different load current, gate resistor and $L_{\text{middle}}$. At different values of external gate resistor, the turn-on switching loss will eventually decrease as the value of $L_m$ goes up over a wide range of load current.

![Lower MOSFET Turn-on Loss at Various Current and $L_m$](image)

*Figure 4.70. Turn-on loss results at different $L_m$.*

Several factors contribute to the reduced turn-on loss at increased value of $L_{\text{middle}}$. Figure 4.71 illustrates the turn-on waveforms of the lower MOSFET and lower anti-parallel diode at $L_{\text{middle}} = 50 \, \text{nH}$ and $L_m = 1.6 \, \text{uH}$ with all other conditions the same. It can be observed the drain-to-source voltage falls more quickly in the case with a larger value of middle-point inductance. This can be explained by the fact that the effective output capacitance to be charged or discharged will be smaller because of the decouple effect at higher values of $L_{\text{middle}}$. Correspondingly, with the same gate drive circuit, $V_{ds}$ will drop more quickly leading to reduced power loss.
Another reason is that the peak drain current of lower MOSFET is smaller at a higher value of $L_{\text{middle}}$. To be specific, with small value of $L_{\text{middle}}$, the measured drain current spike composes of the charge current of upper anti-parallel diode, the charge current of upper MOSFET and the discharge current of lower anti-parallel diode as shown in Figure 4.72. All this charge or discharge currents will lead to excessive overlap losses since the $V_{ds}$ of active switching device has not reached zero.

On the contrary, when the value of $L_{\text{middle}}$ is large, the drain-to-source voltage of the lower anti-parallel diode is not falling together with $V_{ds}$ of lower MOSFET as indicated in Figure 4.71. Consequently, the discharge current of lower anti-parallel diode and the charge current of upper

Figure 4.71. Turn-on waveforms at $R_{g,\text{on}} = 5 \Omega, I_{\text{load}} = 110 A$ with $L_m = 50 \, \text{nH}$ and $L_m = 1.6 \, \text{uH}$ respectively.
MOSFET will not introduce extra overlap losses on lower MOSFET. Compared with the case of a small value of $L_{\text{middle}}$, only the charge current of upper anti-parallel diode within the N-cell will introduce overlap loss; thus, the overlap loss will be smaller with a large value of $L_{\text{middle}}$. In other words, $L_{\text{middle}}$ with a large value effectively decouples the P-cell with N-cell, and prevents the overlap losses due to the other phase leg.

![Diagram](image.png)

*Figure 4.72. Composition of measured drain current with small $L_m$.*

This decoupled effect at large value of $L_{\text{middle}}$ can also be observed from the fact that turn-on switching loss at 0 A is decreasing as $L_m$ goes up. Based on the double pulse test setup shown in Figure 4.50, the 0 A turn-on loss include three parts: the $C_{\text{oss}}$ charge of upper anti-parallel diode, the $C_{\text{oss}}$ charge of upper MOSFETs and the $C_{\text{oss}}$ discharge of lower anti-parallel diode. Only the $C_{\text{oss}}$ discharge of the active lower MOSFET is not measured as the real channel current cannot be measured with external inserted coaxial shunt. Note that the $C_{\text{oss}}$ discharge current of the lower
anti-parallel diode can be measured in the split-scaled design since the current path needs to go through the shunt resistor. In the extreme case when the value of \( L_{\text{middle}} \) is zero, all these \( C_{\text{oss}} \) charge and discharge energy of the switches except lower MOSFETs will be measured during the switching interval. Therefore, the initial measured turn-on loss at 0 A will at its maximum value when \( L_m \) is small. However, at another extreme case when \( L_m \) is very large, it can be regarded as open circuit. Thus, only the charge of upper anti-parallel diode’s \( C_{\text{oss}} \) will be measured. Consequently, the 0 A turn-on loss will merge at different points as indicated in Figure 4.70.

However, the energy stored in the P-cell’s switch node capacitor will eventually be dissipated through either the on-resistance of the lower MOSFET or the parasitic resistance of the connection wires. As can be seen in Figure 4.71, the drain current of the lower MOSFETs is larger at higher value of \( L_{\text{middle}} \) after the turn-on transients. In fact, this drain current is even larger than the load current. This is a caused by two reasons. First, during the lower MOSFET’s dv/dt period, the current through the middle-point inductor connected to P-cell’s switch node \( L_{\text{middle}_P} \) is still a positive value assuming all the current directions are defined as flowing into the switch nodes as shown in Figure 4.73. As a result, the switch node voltage of the P-cell is almost unchanged during the lower MOSFET’s dv/dt period. As lower MOSFET’s voltage is decreasing, the switch node voltage of P-cell is higher than the switch node of N-cell, and the current in the middle-point inductor connected to N-cell \( L_{\text{middle}_N} \) will increase and the current in the middle-point inductor connected to P-cell \( L_{\text{middle}_P} \) will decrease. This phase will end when the current in \( L_{\text{middle}_P} \) reaches zero and current in \( L_{\text{middle}_N} \) reaches load current. Afterward, a resonance of the P-cell switch node’s junction capacitance and the middle-point inductor (\( L_{\text{middle}_N} \) and \( L_{\text{middle}_P} \) in series) will occur. The starting state is \( V_{\text{sw}_P\text{cell}} = 600 \) V, and it will end when \( V_{\text{sw}_P\text{cell}} \) reaches zero as it will be clamped by the anti-parallel diode. Consequently, the resonance only happens for
a quarter of the resonant period and the resulting current in $L_{middle,N}$ will be larger than the load current.

\[ \frac{di}{dt} = \frac{V_{MOS\_on} + V_{AntiDiode\_on}}{L_{middle,N} + L_{middle,P}} \] (16)

The turn-off loss result at different values of $L_{middle}$ is summarized as shown in Figure 4.75. As can be seen, the turn-off loss is always increasing as $L_{middle}$ increases.
Figure 4.74. Turn-on equivalent circuit after $V_{sw}$ reaches zero at large value of $L_m$.

Figure 4.75. Turn-off loss results at different $L_m$.!
Two reasons contribute to the increased turn-off loss. First, because of the reduced equivalent output capacitance at larger value of $L_{\text{middle}}$, the drain-to-source voltage is increasing more quickly. This is verified through the comparison of the turn-off waveforms at $L_m = 50 \, \text{nH}$ and $L_m = 1.6 \, \mu\text{H}$ shown in Figure 4.76. Thus, more overlap loss is obtained at a given drain current.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure4_76.png}
\caption{Turn-off waveforms at $R_{\text{g,on}} = 5 \, \Omega$, $I_{\text{load}} = 110 \, \text{A}$ with $L_m = 50 \, \text{nH}$ and $L_m = 1.6 \, \mu\text{H}$ respectively.}
\end{figure}

Second, at higher values of $L_m$, more current remains to flow through the lower MOSFET in the $\text{dv/dt}$ period. The measured drain current of the lower MOSFET constitutes of three parts: the discharge of upper anti-parallel diode, the discharge of the upper MOSFET, and the charge of...
the lower anti-parallel diode. All these charge/discharge currents are shown in Figure 4.77. With a large value of $L_{\text{middle}}$, the other switching cell is decoupled. Correspondingly, more current remains in the lower MOSFET at higher a value of $L_{\text{middle}}$ for a given load current. Combining the higher $V_{ds}$ and higher drain current, the overlap loss will be larger at a higher value of $L_{\text{middle}}$.

![Figure 4.77. The composition of measured drain current during turn-off.](image)

At different values of gate resistors, the maximum voltage spike values of lower MOSFET and lower anti-parallel diode are summarized in Figure 4.78 to Figure 4.83 with the values of $L_{\text{middle}}$ varying. The voltage spikes of both lower MOSFET and lower anti-parallel diode will increase with the load current.
Figure 4.78. Maximum lower MOSFET’s voltage at different $L_m$ with $R_{g,off} = 10 \, \Omega$ during lower MOSFET turn-off.

Figure 4.79. Maximum lower anti-parallel diode’s voltage at different $L_m$ with $R_{g,off} = 10 \, \Omega$ during lower MOSFET turn-off.
Figure 4.80. Maximum lower MOSFET’s voltage at different $L_m$ with $R_{g,off} = 7.5 \ \Omega$ during lower MOSFET turn-off.

Figure 4.81. Maximum lower anti-parallel diode’s voltage at different $L_m$ with $R_{g,off} = 7.5 \ \Omega$ during lower MOSFET turn-off.
Figure 4.82. Maximum lower MOSFET’s voltage at different $L_m$ with $R_{g,off} = 5 \, \Omega$ during lower MOSFET turn-off.

Figure 4.83. Maximum lower anti-parallel diode’s voltage at different $L_m$ with $R_{g,off} = 5 \, \Omega$ during lower MOSFET turn-off.
However, as $L_{middle}$ increases, the maximum voltage of the MOSFET is increasing while the maximum voltage of the anti-parallel diode is decreasing. At $R_{g,ext}=10\ \Omega$ and $110\ \text{A}$, the lower MOSFET’s voltage overshoot increases 17% when $L_{middle}$ is increased from 10 nH to 1.6 uH. At the same condition, around 80% reduction of voltage overshoot is observed for the lower anti-parallel diode. In fact, the lower anti-parallel diode’s voltage overshoot is small and almost flat over the load current in the case of $L_{middle} = 1.6\ \text{uH}$.

From lower MOSFET’s turn-on result, the lower MOSFET and lower anti-parallel diode will have different overvoltage stress with the existence of middle-point inductance, especially at large value of $L_{middle}$.

b) Upper MOSFET turn-on

During the upper MOSFET’s turn-on transients, the lower MOSFET and lower anti-parallel diode will also experience voltage spikes. To evaluate the voltage spikes variation trend at different values of middle-point inductance. Another group of tests is implemented at various values of $L_{middle}$, where both the maximum voltage of lower MOSFET and lower anti-parallel diode are measured during turn-on of upper MOSFET. The results are demonstrated in Figure 4.84 to Figure 4.89.

Like the case of lower MOSFET’s turn-off, the voltage spikes of the lower MOSFET and lower anti-parallel diode are different because of the middle-point inductance’s effect. However, an opposite trend of voltage spike variation is observed for the case of upper MOSFET’s turn-on. To be specific, as $L_{middle}$ increases, the lower MOSFET’s voltage will decrease while the anti-parallel diode’s voltage will build up. Considering the turn-on condition at $R_{g,ext} = 10\ \Omega$ and $I_{load} = 110\text{nA}$, the induced voltage overshoot on lower MOSFET is reduced by 56% as $L_{middle}$ changes from 10 nH to 1.6 uH. On the other hand, the lower anti-parallel diode’s overshoot is increased by 40%.
Figure 4.84. Maximum lower MOSFET’s voltage at different $L_m$ with $R_{g,off} = 10 \Omega$ during upper MOSFET turn-on.

Figure 4.85. Maximum lower anti-parallel diode’s voltage at different $L_m$ with $R_{g,off} = 10 \Omega$ during upper MOSFET turn-on.
Figure 4.86. Maximum lower MOSFET's voltage at different $L_m$ with $R_{g,off} = 7.5 \, \Omega$ during upper MOSFET turn-on.

Figure 4.87. Maximum lower anti-parallel diode's voltage at different $L_m$ with $R_{g,off} = 7.5 \, \Omega$ during upper MOSFET turn-on.
Figure 4.88. Maximum lower MOSFET’s voltage at different $L_m$ with $R_{g,off} = 5 \, \Omega$ during upper MOSFET turn-on.

Figure 4.89. Maximum lower anti-parallel diode’s voltage at different $L_m$ with $R_{g,off} = 5 \, \Omega$ during upper MOSFET turn-on.
4.3 Summary

In this chapter, a 1200 V SiC trench module is fabricated based on P-cell/N-cell concept with decoupling capacitors embedded. The module is evaluated in both static and switching tests. Fast switching speed can be achieved as well as a low on-resistance. The temperature dependent test results indicate a decrease in both turn-on and turn-off loss at higher junction temperature.

The loss calculation from kelvin $V_{ds}$ is compared with that from non-kelvin loss at different load currents and different values of gate resistor. It is found that the loss from kelvin $V_{ds}$ will give a higher turn-off loss but lower turn-on loss. However, the overall loss obtained from both voltage sensing points are the same. Meanwhile, it is observed that the non-kelvin $V_{ds}$ will have lots of ringing during turn-on while kelvin $V_{ds}$ is clean. These two voltages are used for DESAT protection respectively, and it is observed that the DESAT protection signal from kelvin connection is also noise-free. Correspondingly, the minimum blanking time can be realized with this kelvin $V_{ds}$ connection.

Different values of voltage spike are observed for device close to decoupling capacitors and device distant from decoupling capacitors. The parasitic inductance of the package is also extracted based on the kelvin-sensed voltage waveforms probed at these two positions. Different values of parasitic inductance are derived.

Multi-frequency ringing is observed in the switching test. From frequency domain analysis, it is found that the middle-point inductance will also affect the switching transients actively. A dedicated module is fabricated with the capability of changing the value of middle-point inductance. Extensive switching tests are accomplished at different values of middle-point inductance, gate resistor and load current. As $L_{middle}$ increases, the turn-on loss will decrease because of the reduced charge/discharge current from the other cell. If $L_{middle}$ is large enough, a decoupled condition can be realized. Meanwhile, the turn-off will increase as $L_{middle}$ goes up.
Besides the switching loss, the voltage overshoots are also recorded. Considering lower MOSFET turn-off, its overvoltage will increase as the value of $L_{middle}$ goes up. However, the overvoltage on the lower anti-parallel diode will decrease. If upper MOSFET turn-on is considered, the voltage spikes on lower MOSFET will decrease as $L_{middle}$ increases while the voltage spikes on lower anti-parallel diode will build up.
Chapter 5

Thermal Coupling’s Effect on Steady State Junction Temperature Imbalance among Paralleled Devices

As discussed in the introduction section, previous studies only consider the dynamic switching loss distribution in one pulse and ignore thermal coupling’s effect. In this chapter, the role of thermal coupling on balancing the junction temperatures of paralleled devices is studied. Specifically, the first section of this chapter compares a thermally coupled system with a thermally decoupled system, and the steady state junction temperature differences of these two systems under unbalanced switching loss are investigated. Then combining the thermal model with the electrical model, the steady state junction temperature change at different coupling conditions is examined. Experiments are demonstrated in the last section to verify the simulation analysis.

5.1 Simulation Comparison of Fully Coupled and Fully Decoupled Cases

In real converter operations, the devices are continuously gated, and the junction temperature of each device will change according to the power loss. If there is an uneven distribution of switching loss, the devices’ junction temperature will vary. In return, the change of junction temperature will affect the switching loss. During this iteration process, the conduction loss will be redistributed to compensate the switching loss difference. Consequently, the loss distribution will be updated. Meanwhile, the thermal coupling between paralleled devices will also help to reduce the junction temperature imbalance among paralleled devices. To simulate this iteration process in real operation and obtain the corresponding steady state junction temperature, an electrothermal model is needed.

5.1.1 Electrothermal Model Iteration in Simulation

In the electrical model part, only the conduction loss distribution is considered. The temperature dependent on-resistance can be expressed as:
\[ R_{ds,\text{on}}(T) = a \cdot T^2 + b \cdot T + c \]  
\hspace{1cm} (17)

where \( a = 0.00077667 \cdot 10^{-3} \), \( b = 0.14967 \cdot 10^{-3} \) and \( c = 25.2 \cdot 10^{-3} \). Its values versus junction temperature is plotted as shown in Figure 5.1.

**Figure 5.1. On-resistance versus junction temperature used in the simulation.**

Considering an RMS current \( I_{\text{tot}} \) is going through the two devices, the current of each device is:

\[ I_1 = \frac{R_{ds,\text{on}}(T_2)}{R_{ds,\text{on}}(T_1) + R_{ds,\text{on}}(T_2)} \cdot I_{\text{tot}} \]  
\hspace{1cm} (18)

\[ I_2 = \frac{R_{ds,\text{on}}(T_1)}{R_{ds,\text{on}}(T_1) + R_{ds,\text{on}}(T_2)} \cdot I_{\text{tot}} \]  
\hspace{1cm} (19)
The total switching loss is assumed independent of the junction temperature. This is true for most SiC devices. However, it will change with the load current as expressed by:

\[ E_{\text{tot}}(I) = a_1 \cdot I^2 + b_1 \cdot I + c_1 \]  

(20)

where \( a_1 = 0.1671 \cdot 10^{-6} \), \( b_1 = 15.85 \cdot 10^{-6} \) and \( c_1 = 366.4 \cdot 10^{-6} \).

At a given load current, a constant switching loss is selected and a fixed distribution of switching loss is selected for each device. To be specific, either equal distribution (each device has the same switching loss) or fully unbalanced distribution (one device is taking all the switching loss) of switching loss is studied. In other words, the best and worst scenarios of switching loss distribution in real converter operations are evaluated in simulation. In real circuits, the junction temperature, device’s characteristics and the parasitic inductance together will determine the distribution of switching loss.

In the simulation, the RMS value of the total current is selected first. An initial junction temperature is assumed for each device, and the on-state current of each device and corresponding conduction loss are calculated. Based on the switching loss distribution scenario, the total loss of each device can be obtained. All this process is implemented in Matlab.

Then, the loss data is sent to the power loss setting of each device in Comsol. The device’s package structure, material and cooling conditions are appointed in Comsol as well. The thermal model relies on the finite element method (FEA) simulation. A stationary FEA thermal simulation is carried out, and the corresponding junction temperature of each device is derived.

The updated values of each device’s junction temperature are assigned to the Matlab for new power loss calculations, and a new junction temperature can be obtained after simulation in Comsol. This iteration continues until a stable junction temperature is reached for each device. Figure 5.2 shows this flow chart of the iteration.
Figure 5.2. Steady state junction temperature derivation with co-simulation of Matlab and Comsol.

5.1.2 Comparison of Thermally Decoupled Case with Coupled Case

In terms of the cooling condition of the parallel devices, two schemes are illustrated. In the first fully decoupled case, each device is attached to a separate direct-bonded-copper (DBC) substrate, and a separate natural convection pin-fin heat sink is used for cooling each device. The geometry and structure are shown in Figure 5.3.

Figure 5.3. Illustration of the thermally decoupled case.
For each chip, natural convection is assumed, and the thermal resistance from the chip’s junction to ambient is simulated to be:

\[ R_{th} = \frac{T_j - T_a}{P} = 12.38 \, ^\circ C/W \]  

(21)

When device 1 is heated up due to its own power loss \( P_1 \), the junction temperature of device 2 will not be affected. Therefore, the coupling thermal resistance is defined as:

\[ R_{th,21} = \frac{T_j - T_a}{P_1} = 0 \, ^\circ C/W \]  

(22)

The coupling coefficient from chip 1 to chip 2 is:

\[ C_{21} = \frac{R_{th,21}}{R_{th}} = \frac{T_j - T_a}{T_j - T_a} = 0 \]  

(23)

The coupling coefficient is a representation of how effective the device’s junction temperature will be affected by the power loss generated by other devices.

For the coupled case shown in Figure 5.4, the paralleled devices will share the same substrate and heatsink. The geometry dimensions of the DBC and heatsink are the same as that in the decoupled case. The heat convective coefficient is also identical. Correspondingly, the thermal resistance from junction to ambient of each chip would be the same as the decoupled case:

\[ R_{th1} = R_{th2} = \frac{T_j - T_a}{P} = 12.38 \, ^\circ C/W \]  

(24)

\[ Figure \ 5.4. \ Illustration \ of \ the \ thermally \ coupled \ case. \]
However, the coupling thermal resistance is not zero, and is calculated to be:

\[ R_{th21} = \frac{T_{j2}-T_a}{P_1} = 12.04 \, ^\circ C/W \] (25)

Due to the symmetrical layout, the coupling resistance value from chip 2 to chip 1 \( R_{th12} \) is the same as \( R_{th21} \). Different from the decoupled case, the coupling coefficient is calculated to be:

\[ C_{21} = \frac{R_{th21}}{R_{th}} = \frac{12.04}{12.38} = 0.97 \] (26)

For both thermally decoupled and thermally coupled case, the steady state junction temperature of each device at balanced and unbalanced switching loss is simulated in the following section. The total current RMS value of the paralleled devices is 14 A, and the total switching loss is 3 W. For balanced condition, 1.5 W switching loss is added to each device. On the contrary, 3 W switching loss will be only generated on device 2 in the unbalanced condition.

a) Thermally decoupled case with balanced switching loss

With the same switching loss, the steady state junction temperatures of both chips are 61.4 \(^\circ\)C after several iterations. Figure 5.5 illustrates the steady state temperature distribution in Comsol. The horizontal axis is the junction temperature, and the vertical axis represents the power loss. The steady state junction temperature can also be derived from the crossing point of the curves of power loss generation and cooling system. As shown in Figure 5.6, the green line characterizes the cooling system for device 1 and device 2. The power loss generated in device 1 \( P_1 \) is cooled by the heatsink with a thermal resistance of \( R_{th1} \) as indicated in the following equation:

\[ P_1 = \frac{1}{R_{th1}} \cdot (T_{j1} - T_a) \] (27)

The blue line stands for the power generation of device 1. For this device, its steady state RMS current value is 7 A and its switching loss is 1.5 W. In steady state, the power loss generation versus junction temperature can be expressed as:

\[ P_1(T_{j1}) = I_1^2 \cdot R_{ds,on}(T_{j1}) + 1.5 \] (28)
Figure 5.5. Steady state temperature distribution in Comsol for the thermally decoupled balanced switching loss case.

Figure 5.6. Representation of cooling system and power generation curve for the thermally decoupled balanced switching loss case.
b) Thermally coupled case with balanced switching loss

For the thermally coupled case, the steady state junction temperatures of both chips are 123.0 °C with 1.5 W switching loss on each device as indicated in Figure 5.7. In steady state, the power loss generation versus junction temperature curve \( P_1(T_{j1}) \) is the same as in the case of thermally decoupled case. However, the junction temperature is higher than that of thermally decoupled case. This is mainly because of the thermal coupling’s effect between these two devices. As can be seen in Figure 5.8, the cooling system (green line) is shifted to the right compared with the decoupled case (dotted green line). This shift is caused by both thermal coupling and power loss generated in the other device. Take device 1 for example, the following equation describes the cooling system with thermal coupling’s effect:

\[
P_1(T_{j1}) = \frac{1}{R_{th1}} \cdot (T_{j1} - T_a - R_{th12} \cdot P_2)
\]

(29)

*Figure 5.7. Steady state temperature distribution in Comsol for the thermally coupled balanced switching loss case.*
c) Thermally decoupled case with unbalanced switching loss

In the following sections, unbalanced switching loss case is studied for both systems. Device 2 will have 3 W switching loss in addition to the conduction loss while device 1 only has conduction loss. The on-resistance of both devices has a positive temperature coefficient. It is assumed that the current will be redistributed such that the conduction loss can compensate the switching loss difference and balance the junction temperature of both devices. However, from the steady state simulation result shown in Figure 5.9, it is observed that there is still a large junction temperature difference if solely the on-resistance's self-balance is relied on. As can be seen from Figure 5.10, the initial power loss generation curves of device 1 and device 2 are shown in the dotted red line and dotted blue line respectively. 7 A is assumed to flow through each device, and the only difference between those two curves is the 3 W switching loss. In steady state, the current
Figure 5.9. Steady state temperature distribution in Comsol for the thermally decoupled unbalanced switching loss case.

Figure 5.10. Representation of cooling system and power generation curve for the thermally decoupled unbalanced switching loss case.
in device 1 is indeed increased as indicated by the solid red line in Figure 5.10, but the increase in conduction loss is not enough to compensate the switching loss discrepancy. The system’s cooling curve is not changed over the iteration process and can be described by equation (27). Consequently, there is a large difference between these two steady state junction temperatures.

d) Thermally coupled case with unbalanced switching loss

In the thermally coupled system with uneven distribution of switching loss, the steady state junction temperatures of the devices are, contrary to the thermally decoupled case, close to each other as indicated in Figure 5.11. Almost identical current is flowing through each device while all the switching loss is on device 2. The solid red line and solid blue curve in Figure 5.12 demonstrate the power loss generation for device 1 and device 2 respectively at steady state. The cooling curves of device 1 and device 2 can be expressed as:

\[
P_1(T_{j1}) = \frac{1}{R_{th1}} \cdot (T_{j1} - T_a - R_{th12} \cdot P_2)
\]

(30)

\[
P_2(T_{j2}) = \frac{1}{R_{th2}} \cdot (T_{j2} - T_a - R_{th21} \cdot P_1)
\]

(31)

As can be seen, the zero-crossing point of the cooling curves with the horizontal axis is shifted at steady state. The variation of crossing points is caused by the thermal coupling’s effect together with the change of power loss of each chip. With a good thermal coupling, the junction temperature imbalance of the paralleled devices can be greatly reduced even when one of the devices is taking all the switching loss.

All the previous simulation results are summarized in Table 5.1. It can be seen that thermal coupling is actually more effective than conduction loss’s self-balancing in terms of reducing the junction imbalance between paralleled devices. In fact, if the junction temperature of each device is the same, the on-resistance would be the same and the conduction loss of each device is equal. As a result, simply relying on the self-balance of conduction loss cannot achieve similar junction temperatures among paralleled devices if the switching loss distribution is not balanced.
Figure 5.11. Steady state temperature distribution in Comsol for the thermally coupled unbalanced switching loss case.

Figure 5.12. Representation of cooling system and power generation curve for the thermally decoupled unbalanced switching loss case.
Table 5.1. Summary of steady state simulation results at different conditions.

<table>
<thead>
<tr>
<th>Simulation Conditions</th>
<th>Steady State Results</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulation Name</td>
</tr>
<tr>
<td>Thermally Decoupled</td>
<td>Device 1</td>
</tr>
<tr>
<td></td>
<td>Device 2</td>
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<tr>
<td>Thermally Coupled</td>
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<td>Device 2</td>
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<tr>
<td>Thermally Decoupled</td>
<td>Device 1</td>
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<td>Thermally Coupled</td>
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<td>Device 2</td>
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5.2 Simulation Evaluation of Thermal Coupling’s Effect on Steady State Junction Temperature Imbalance for Paralleled Devices

As discussed in the previous section, thermal coupling will affect both the absolute values of the two devices’ junction temperature and the junction temperature difference between these two devices. In the following section, the thermal resistance would be fixed and the junction temperature of each device will be simulated at different coupling coefficients.

5.2.1 Fast Electrothermal Model in Matlab

The previous electrothermal co-simulation using Matlab and Comsol takes a long time to achieve study state mainly because of the reliance on FEA simulation. It is needed to eliminate Comsol simulation in the iteration process. To realize that, a good thermal model is required. As discussed in [57], a linear assumption based thermal model can be used if the thermal spreading effect and heat convection effect are negligible. For the linear thermal model considering two paralleled devices, the system can be depicted using the following equation if the thermal capacitance can be ignored:

\[
\begin{bmatrix}
    T_{j1} \\
    T_{j2}
\end{bmatrix} =
\begin{bmatrix}
    R_{th1} & R_{th12} \\
    R_{th21} & R_{th2}
\end{bmatrix}
\cdot
\begin{bmatrix}
    P_1 \\
    P_2
\end{bmatrix}
+ \begin{bmatrix}
    T_{a1} \\
    T_{a2}
\end{bmatrix}
\] (32)
The values of the thermal resistance matrix can be derived from simple FEA simulations. Once these values are obtained through FEA simulation, the linear thermal model can be implemented in Matlab, and only the numerical iteration calculations will be processed in Matlab. This can greatly facilitate the calculation speed, and the iteration flow chart is summarized in Figure 5.13.

\[
\begin{bmatrix}
  T_1 \\
  T_2
\end{bmatrix} =
\begin{bmatrix}
  R_{th1} & R_{th12} \\
  R_{th21} & R_{th2}
\end{bmatrix}
\begin{bmatrix}
  P_1 \\
  P_2
\end{bmatrix} +
\begin{bmatrix}
  T_a \\
  T_a
\end{bmatrix}
\]

*Figure 5.13. Steady state junction temperature derivation with a fast electrothermal model in Matlab.*

### 5.2.2 Steady State Junction Temperature Simulation for Pin-fin Heatsink with Natural Convection

With the fast electrothermal model available, the steady state junction temperatures of the paralleled devices are simulated at different values of coupling coefficient. The thermal resistance \( R_{th1} = R_{th2} = 12.38 \, ^\circ C/\text{W} \). Due to the symmetric layout, the coupling thermal resistance \( R_{th12} = R_{th21} \). The couple coefficient \( C_{21} = R_{th21}/R_{th1} \) is varied from 0 to 1. Figure 5.14 shows the
Figure 5.14. Steady state junction temperature of each device at various values of coupling coefficient.
simulated junction temperature of each device at balanced and unbalanced conditions. The total current is 14 A, and the total switching loss is 3 W. It can be seen that the junction temperature is increased as coupling coefficient goes up in both cases. However, for the unbalanced case, the junction temperature imbalance between paralleled devices will decrease as the coupling coefficient increases.

5.2.3 Investigation of Factors Changing Coupling Coefficient

From the previous simulation results, the coupling coefficient will greatly affect steady state junction temperature of each device. Therefore, different factors affecting the value of coupling coefficient is examined.

First, the material of the baseplate is changed from copper to aluminum, and then to aluminum plus thermal grease. Comsol is used to solve all the thermal resistance values, and the coupling coefficient is calculated accordingly. Table 5.2 summarizes the simulation result. It can be seen that, with a fixed geometry and location, the coupling coefficient will drop as the thermal conductivity of the material is decreasing.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Thermal Resistance (°C/W)</th>
<th>Coupling Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper baseplate</td>
<td>12.38</td>
<td>0.97</td>
</tr>
<tr>
<td>Aluminum baseplate</td>
<td>12.68</td>
<td>0.95</td>
</tr>
<tr>
<td>Aluminum baseplate + thermal grease</td>
<td>13.20</td>
<td>0.91</td>
</tr>
</tbody>
</table>

Then forced-air convection is added and the flow rate is varied. The structure of the pin-fin heat sink and air channel is shown in Figure 5.15. The variation of thermal resistance and coupling coefficient over flow rate is summarized in Figure 5.16 and Figure 5.17. It is observed that the coupling coefficient will decrease as the flow rate is increasing for this specific structure.
Figure 5.15. The structure of pin-fin heat sink with forced convection.

Figure 5.16. Thermal resistance value at a different flow rate.

Figure 5.17. Coupling coefficient value at a different flow rate.
In the last step, the distance between the edges of paralleled devices is changed at a given flow rate (12 m/s). With an increase in distance, the thermal resistance will increase slightly while the coupling thermal resistance will decrease. Consequently, the coupling coefficient is decreasing as the distance enlarges. Figure 5.18 and Figure 5.19 demonstrate the simulation results.

![Thermal Resistance vs Distance Between Devices](image1.png)

*Figure 5.18. Thermal resistance value at a different flow rate.*

![Coupling Coefficient vs Distance Between Devices](image2.png)

*Figure 5.19. Coupling coefficient value at a different flow rate.*

As a summary, the coupling coefficient will change with the material property, the cooling condition and the physical placement of the devices. Different level of thermal coupling can be realized through substrate, baseplate or heatsink.
5.2.4 Steady State Junction Temperature Simulation for Pin-fin Heatsink with Forced Convection

For the forced convection case, the flow rate is selected to be 12 m/s and the corresponding thermal resistance is 1.15 °C/W. In the simulation, the total current is 48 A, and the total switching loss 70 A. An unbalanced switching loss is simulated where all the switching loss is on device 2. To change the coupling coefficient, the distance between the edges of paralleled devices is varied. Figure 5.20 and Figure 5.21 summarizes the junction temperature of each device and the junction temperature difference at various values of spacing.

As the spacing goes up, the coupling coefficient will decrease. Correspondingly, the junction temperature of both devices will decrease as illustrated in Figure 5.20. In the meantime, the junction temperature imbalance will be enlarged because of the reduction in coupling coefficient as indicated in Figure 5.21.

![Figure 5.20. Steady state junction temperature value at different values of spacing.](image-url)
5.3 Experiment Verification with Dedicated Modules

To verify thermal coupling’s effect on paralleled devices, two identical modules are fabricated with the exception that the distances between the paralleled devices are different as shown in Figure 5.22. The two paralleled devices share the same drain terminal; however, they have independent source terminal pins. With this configuration, different load current can go through each device and the power loss in each device can be controlled independently.

For all these paralleled chips, they are detached from the same wafer. Their temperature dependent on-resistance is obtained from the curve tracer, and the result is illustrated in Figure 5.23. It can be seen that similar characteristics are obtained for these paralleled devices. The on-resistance versus junction temperature data will be used in continuous tests for measuring the junction temperature of each device.

A bonded-fin heatsink is attached to the baseplate of the power module through four screws. Thermal grease is sputtered in between. A DC fan is mounted on one side of the heat sink channel.

**Figure 5.21. Steady state junction temperature imbalance at different values of spacing.**
(a) Module 1: Devices far away  (b) Module 2: Devices adjacent to each other

Figure 5.22. Two single-switch power modules with different values of spacing between devices.

(a) $M_1$ and $M_2$  (b) $M_3$ and $M_4$

Figure 5.23. Temperature dependent on-resistance values for $M_1$ to $M_4$.

Figure 5.24. The test set up for continuous operation.
This forced convection cooling system enables safe continuous operation of the power module. To validate thermal coupling’s effect on steady state junction temperature of paralleled devices, both modules are continuously running with uneven power losses for the paralleled devices. The uneven power loss is realized by assigning different values of load current to each device.

Before the continuous operation, the thermal resistance and the coupling coefficient of the two modules are characterized first. Figure 5.25 shows the tested thermal resistance change of $M_4$ at different values of power loss and cooling conditions. The power loss is changed by controlling the load current at different values, and the cooling condition is varied by adjusting the DC fan’s voltage. In this experiment, the fan’s voltage is varied at 0 V, 12 V and 24 V.

![M₄ Junction to ambient Thermal Resistance vs. Power Loss](image)

Figure 5.25. Thermal resistance change of $M_4$ at different power losses and cooling conditions.

It can be seen that a nonlinear thermal resistance is observed, especially at low power loss range. This can be explained by the heat-spreading effect of the heatsink. At low power loss, the heat-spreading angle is small. Correspondingly, the effective heat exchange area is reduced and the thermal resistance is large. However, above a certain value of power loss, the thermal resistance is
almost unchanged. Therefore, the assumption of the linear thermal model will still be valid at high power loss range. In terms of the characterization of the thermal model, it is mostly implemented at high power loss conditions. For both modules, one active device has a load current of 20 A while the other passive device has 0 A. In steady state, the junction temperature of the active device can be obtained by reading its terminal voltage and comparing the experimental on-resistance value with the pre-calibrated on-resistance versus junction temperature data. For the passive device, its on-resistance is tested through curve tracer at steady state. With a knowledge of the junction temperatures of both devices and the active device’s power loss, the thermal resistance and coupling coefficient can be calculated for the 0 V fan voltage case as summarized in Table 5.3.

<table>
<thead>
<tr>
<th>Table 5.3. Thermal characterization of the modules.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 V Fan Voltage Testing</td>
</tr>
<tr>
<td>Device Name</td>
</tr>
<tr>
<td>Current in Each Device (A)</td>
</tr>
<tr>
<td>Coupling/Thermal resistance ($^\circ$C/W)</td>
</tr>
<tr>
<td>Coupling Coefficient</td>
</tr>
<tr>
<td>Junction Temperature Difference ($^\circ$C)</td>
</tr>
</tbody>
</table>

It can be seen that the coupling coefficient of #2 module is a bit larger than that of #1 module. This is caused by the fact that the two devices are placed closer to each other in #2 module. However, compared to the placement in #1 module where the two devices are far away, the increase of the coupling coefficient is not significant. The majority of the coupling is through the baseplate and heatsink, instead of through the DBC substrate layer for this specific package design.
From the thermal characterization, it can be seen that both modules have almost identical thermal resistance. However, the coupling coefficient is slightly different because of the different spacings. After the characterization, a continuous operation is implemented where one device has 20 A while the other device has 10 A. For each device, the steady state junction temperature is obtained in a similar way as described in the characterization part. Table 5.4 shows the experiment result at a fan voltage of 0 V. Comparing the junction temperature of $M_2$ with $M_4$ and $M_1$ with $M_3$, the device’s junction temperature in #2 module is always higher than that in #1 module. This can be explained by the fact that the coupling coefficient in #2 module is larger than that in #1 module. Meanwhile, the junction temperature difference in #2 module is smaller compared to #1 module. The experiment result validates the simulation assumptions that, for a given thermal resistance, thermal coupling will reduce the junction temperature imbalance at the cost of raising both devices’ junction temperature.

<table>
<thead>
<tr>
<th>0 V Fan Voltage Testing</th>
<th>#1 Module</th>
<th>#2 Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Name</td>
<td>$M_2$</td>
<td>$M_1$</td>
</tr>
<tr>
<td>Current in Each Device (A)</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>Power Loss of Device (W)</td>
<td>5.30</td>
<td>24.17</td>
</tr>
<tr>
<td>Junction Temperature (°C)</td>
<td>89.7</td>
<td>115.3</td>
</tr>
<tr>
<td>Junction Temperature Difference (°C)</td>
<td>25.6</td>
<td>21.5</td>
</tr>
</tbody>
</table>

5.4 Summary

An electrothermal model based on co-simulation of Matlab and Comsol is used to compare the steady state junction temperatures of thermally coupled and thermally decoupled system. It is
found that thermal coupling will affect the junction temperature imbalance under an uneven distribution of switching loss.

To investigate thermal coupling’s effect on the temperature difference under unbalanced switching loss. A fast electrothermal model is implemented in Matlab, and the coupling coefficient is varied. From the simulation result, it is observed that the junction temperature difference between two devices will decrease as the coupling coefficient increases. Meanwhile, the junction temperatures of both devices will increase.

Afterward, several thermal simulations are implemented in Comsol, and different factors affecting the value of coupling coefficient is summarized. It is found that the package’s material, cooling condition, and spacing between devices will together determine the coupling coefficient between devices.

To validate the simulation discovery, two dedicated power modules are built with the same substrate and process. The only difference is the spacing between devices. In this way, similar thermal resistance values are achieved while the coupling coefficients are slightly different which is also verified in experimental characterization results. Different power losses are stressed on the paralleled two chips by controlling the load current independently. Experiment result validates the simulation assumption, and it is found experimentally that thermal coupling can help to reduce the junction temperature imbalance of the paralleled devices under the condition of uneven power loss distribution. However, it will make the junction temperature of both devices higher with a stronger thermal coupling.

In terms of package design, the spacing between devices is an important design parameter. A wise selection of spacing will help to improve the converter’s overall performance. If the cooling condition is not a limiting factor while the loss uneven distribution is a concern, then thermal coupling can be used as a passive method to balance the junction temperature of devices.
Chapter 6

Conclusion

6.1 Contributions

This thesis explores the package design considerations and optimization for fast switching SiC devices with multiple chips in parallel. Specifically, the key contributions of the thesis are summarized as follows.

a) To deal with the large voltage spikes during switching transients caused by fast switching and improve the package’s thermal performance. A low parasitic inductance power module with double-sided cooling is designed and fabricated. Compared with a previously designed baseline module, a 70% reduction of parasitic inductance is achieved from simulation result. The parasitic inductance value of each module is extracted experimentally. Experiment result reveals a reduction from 6.59 nH to 2.60 nH.

b) A 1200V SiC trench MOSFET with wire bond package is designed. P-cell/N-cell concept is implemented to the package layout, the devices are scaled in a split scaling method. Both static and switching characteristics of the power module are evaluated, and benefits of the low-on resistance and fast switching are validated for this state-of-art trench MOSFET. The experimental extracted parasitic value matches with the simulation result. The same module will also be served for evaluating middle-point inductance’s effect on switching transients.

c) A comparison of kelvin $V_{ds}$ and non-kelvin $V_{ds}$ is evaluated in terms of switching loss calculation and DESAT protection. It is found that the loss calculation from kelvin sensed voltage will lead to higher turn-off loss and lower turn-on loss compared with the loss calculation from non-kelvin $V_{ds}$. However, the total switching loss will be the same for both cases from experiment results. In terms of DESAT protection, it is found that the DESAT signal from kelvin $V_{ds}$ is much cleaner compared to that from non-kelvin $V_{ds}$. As a result, a minimum blanking time can be
achieved with the aid of kelvin $V_{ds}$. In terms of package design, it is important to have an access to kelvin drain-to-source for purpose of fast reaction to short circuit.

d) As a fundamental knowledge to be understood before selecting the scaling method of package layout with multiple chips in parallel, the middle-point inductance’s effect on switching transients is evaluated for a split scaled package design. A dedicated module is built with the capability of changing $L_{middle}$. Extensive switching tests are conducted for lower MOSFET turn-off at different values of gate resistor and load current. Experiment results show that as $L_{middle}$ goes up, the maximum voltage spike of the lower MOSFET will increase while the maximum voltage of the lower anti-parallel diode is decreasing. Also, at a higher value of $L_m$, the active switch’s turn-on loss will decrease while its turn-off loss will go down. Similar tests are implemented considering turn-on of upper MOSFET, an opposite trend is observed compared to lower MOSFET’s turn-off.

e) To evaluate thermal coupling’s effect on steady state junction temperature distribution of paralleled devices with an unbalanced dynamic loss, a fast electrothermal model is implemented in Matlab. It is observed that the junction temperature difference between two devices will decrease as the coupling coefficient increases. Meanwhile, the junction temperatures of both devices will increase. It is also found that the package’s material, cooling condition, and spacing between devices will together determine the coupling coefficient between devices. The thermal coupling’s effect is also validated experimentally with two modules of different spacings between paralleled devices. It is verified that the benefits of reduced junction temperature imbalance come at a cost of increasing the junction temperature of both devices.
6.2 Future Work

Some future work is summarized as follows:

a) For power modules with double-sided cooling, the thermal-mechanical stress and long-term reliability are still concerns although it can provide the thermal performance improvement. For the low parasitic inductance double-sided cooled power module design, new packaging material and bonding techniques are required.

b) In terms of selecting the proper scaling method, the middle-point inductance’s effect for identical scaled package design should also be evaluated. In package layout with identical scaling, \( L_{\text{middle}} \) is small and usually can be ignored. However, if the switching delay is considered, the device on one end to the device on the other end will have a relatively large value of \( L_{\text{middle}} \). How would \( L_{\text{middle}} \) affect the identical scaled package layout is to be understood.

c) For thermal coupling’s effect evaluation, a complete thermal model considering the thermal capacitance should be implemented. With this thermal impedance matrix, a complete electrothermal model can be obtained. This model can be used to evaluate the thermal coupling’s effect at different short intervals of loss imbalance and other conditions.
References


Vita

Fei Yang received the B.S. degree in electrical engineering from Northwestern Polytechnical University, Xi’an, China in 2011. From 2012 to 2014, he was working in APEL lab, Kettering University with Dr. Kevin Bai as a research scholar. He is currently working toward the M.S. degree at the University of Tennessee, Knoxville, TN, USA.

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