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All-SiC Three-Phase Converters for High Efficiency Applications

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To the Graduate Council:

I am submitting herewith a dissertation written by Fan Xu entitled "All-SiC Three-Phase Converters for High Efficiency Applications." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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All-SiC Three-Phase Converters for High Efficiency Applications

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Abstract

The dissertation aims to improve the efficiency of three-phase converters using SiC power devices. The methodology to design a high efficiency all-SiC three-phase converter is presented. Four aspects are included: SiC power device evaluation, power loop parasitics analysis, high efficiency current source rectifier, and paralleled current source rectifier system.

The SiC JFET and MOSFET are tested based on voltage source and current source structures respectively. The dissertation proposes a device switching test circuit based on current source topology to simulate current commutation processes. The circuit can evaluate the switching performance and calculate switching loss of a power device used in a three-phase current source converter.

The impacts of power loop parasitics on SiC devices' switching performance and switching loss are studied. The power loop parasitic inductance in a voltage source converter may cause phase-leg shoot-through during a fast switching transient. The key inductances include power device gate loop inductance and converter DC bus inductance. The influence of different parasitic capacitances on device switching loss in three-phase current source converters is analyzed. An inductive snubber circuit is proposed to reduce the impact of parasitic capacitance and reduce power device switching loss in a three-phase current source rectifier.

The design method and procedure of high efficiency three-phase converters are proposed through the development of a 7.5 kW all-SiC three-phase current source rectifier for data center power supplies as the front-end rectifier. The rectifier full load efficiency of 98.54% is obtained.

Master-slave control is proposed for paralleled three-phase current source rectifiers. The balanced output currents, rectifier module hot-swap, and paralleled rectifier system redundancy

can be achieved with this master-slave control. A 19 kW front-end rectifier system using three paralleled all-SiC current source rectifiers is developed for data center power supplies with 98.3% peak efficiency and 98.1% full load efficiency.

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Chapter 1 Introduction

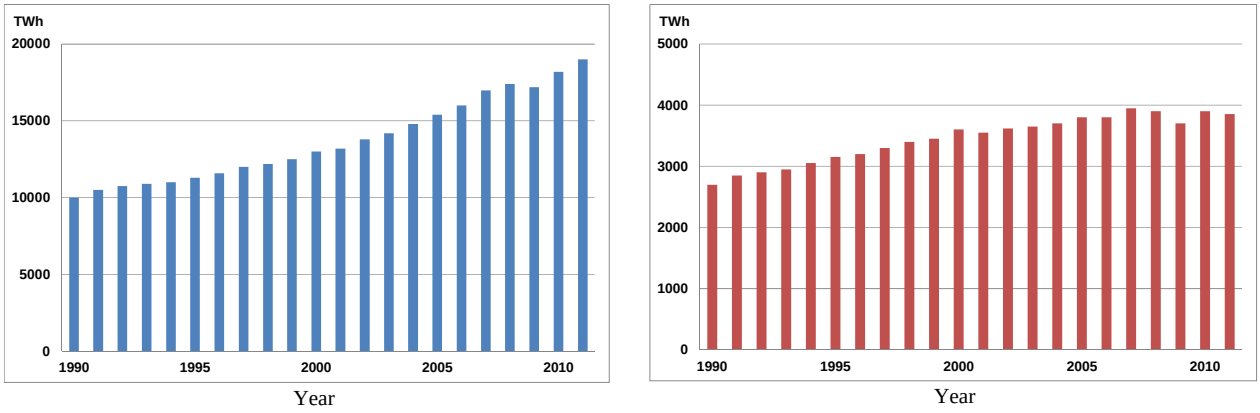
1.1 Background and Motivation

Electricity consumption continues to grow in the United States and worldwide. As shown in Figure 1-1, the electricity consumption of the world was 10,097 TWh in 1990 and increased to 19,016 TWh in 2011, an 88.33% increase in twenty one years. At the same time, the electricity consumption in the U. S. increased from 2,713 TWh to 3,852 TWh, a 41.05% increase over the same period[1]-[3]. As a result, high power conversion efficiency becomes one of the key topics for the continual development of power electronics converters in many application areas, including power supply systems (Uninterruptible Power Supply (UPS), Power Supply Unit (PSU), etc.), transportation systems (electric or hybrid electric vehicle/ship/aircraft), and renewable energy systems (photovoltaic inverter systems, wind turbine systems).Figure 1-2 shows the improvement of power conversion efficiency at full load (rated power) of telecom power supply modules and photovoltaic (PV) inverter systems [4]-[5], where η is the converter efficiency.

The low efficiency of power converters(the high power loss) will result in high utility bills, large environmental footprint, low reliability, and short lifetime of equipment [6]. In addition, higher power loss, which means more heat, requires more efforts on a converter's cooling system and increases the volume of the converter. That will bring challenges to the design of converters which will operate in harsh environment of high temperature or require high power density in vehicles and aircraft. For example,hybrid vehicles use two separate liquid cooling systems currently. One is the 105 ˚C engine coolant, and the other is the 65 ˚C coolant to cool power electronics and electric machine for the traction drive[7]-[8]. A coolant temperature requirement

of 105 °C has been established for 2015 by FreedomCAR and Fuel Partnership Program under the U. S. Department of Energy (DOE) to reduce the cost and complexity[9]. This requirement brings the issues to be solved not only in thermal management but in loss reduction as well.

From Reference [1], the power loss, including the losses on power distribution and power conversion, is 489 TWh in U. S. and 2990 TWh in the whole world. Take the energy consumption of data and telecommunication centers as an example. The data and telecommunication centers are major energy consumers, with energy consumption estimated at 40 TWh in 2005 in U. S. alone, and 120 TWh worldwide, as shown in Figure 1-3[10]. A very large data center requires on the order of 10 MW of power to support the computing infrastructure, and this is expected to increase to 50 MW in the future. In a typical data center, less than half of the power is delivered to the computer load (microprocessors, memories, disk drives, etc.). The rest of the power is lost in power conversion, distribution, and cooling [6]. It has been shown that the capital cost of the power delivery and cooling infrastructure in data centers already exceeds the purchase price of the servers they will support. In addition, it is also expected that the lifetime energy costs of a server will exceed its purchase in the future [11]. The total electricity bill for operating those servers and associated infrastructure in 2005 was about 2.7 billion dollars and 7.3 billion dollars for the U.S. and the world, respectively [10]. So for power electronic researchers, more efforts need to be done to reduce the power conversion and power distribution losses, and achieve higher efficiency converters.



(a) World (b) United States

Figure 1-1. Electricity consumption from 1990 to 2011 [1]-[3].

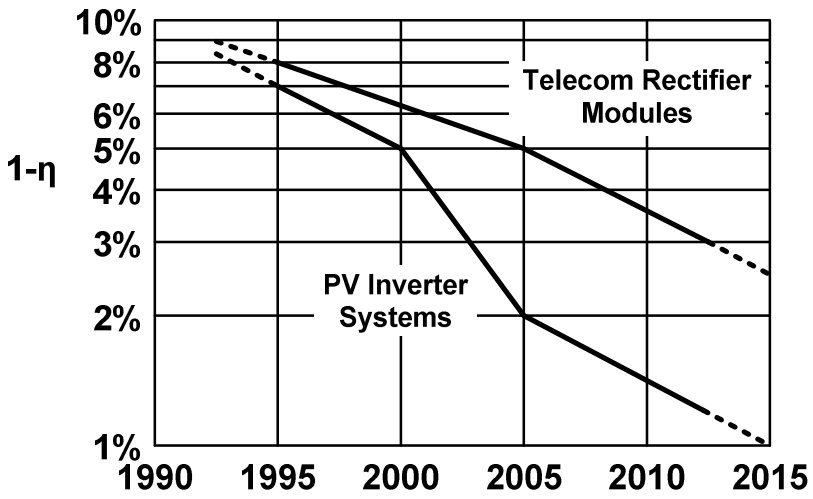


Figure 1-2. Development of power conversion efficiency at full load of telecom power supply modules and PV inverter systems [4]-[5].

The loss of power converters essentially is from three areas. There are power semiconductors, passive components, and auxiliary systems. The reduction of power semiconductors' losses is the key point of achieving high efficiency power conversion because this part of the loss is the dominant part of the total losses in a power converter. Development of power devices is a critical aspect of the power electronic applications along with new topologies and control techniques. Wide bandgap (WBD) devices making inroads into the power

semiconductor device market brings a revolutionary change in the power electronics in a few decades. Silicon carbide (SiC) is one of the WBG material based devices.

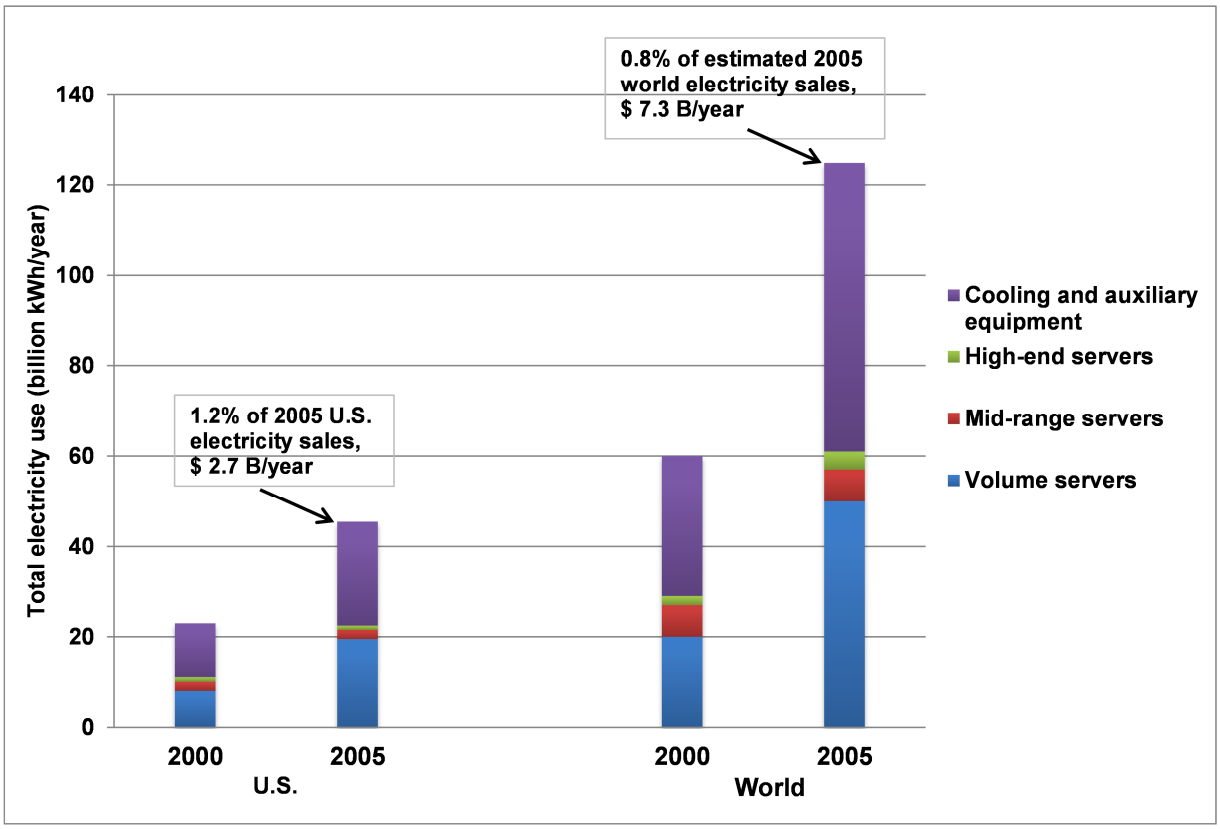


Figure 1-3. Total electricity use for servers in the U.S. and the world in 2000 and2005, including the associated cooling and auxiliary equipment [10].

SiC power electronic semiconductors provide high breakdown voltage, fast switching, low on-state resistance, and high temperature tolerance. From the loss and efficiency point of view, low on-state resistance leads to low conduction loss of power devices, and fast switching provides the possibility of the reduction of devices' switching loss. Meanwhile, SiC power devices play an important role in high switching frequency applications without significant reduction on the efficiency.Figure 1-4 compares the specific on-state resistance of SiC power semiconductors to traditional Si devices. The advantage of SiC devices are clearly shown in

Figure 1-4[12], [16]. Reference [13] gives a comparison of performance of the all-Si, hybrid (Si and SiC), and all-SiC inverters for a hybrid electric vehicle (HEV) at different operating conditions, based on their simulation and loss calculation. The comparison results in Table 2-1 provide an insight to the impact of SiC devices on overall system efficiency gains compared to Si devices.

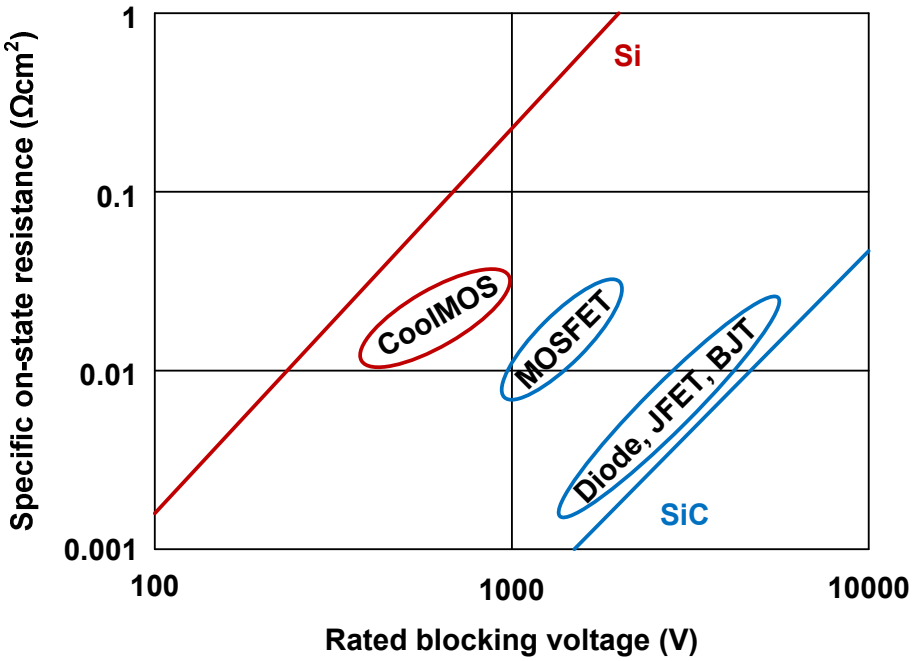


Figure 1-4. Specific on-state resistance vs. rated blocking voltage for different power devices (for IGBTs: relation of forward voltage drop to rated current) [12], [16].

This work focuses on the three-phase ac converters because they are widely used in various power electronics application areas, such as the power supply system, the electric transportation system, and the renewable energy system. Although it is clear based on the analysis above that SiC power semiconductors could help reduce power losses of the converters, the implementation of the SiC devices in high power three-phase convertersremains a challenge due to lack of experience.The overall system performance and the variables of the all-SiC converters are far

from well understood. More work on design and analysis are needed for all-SiC three-phase converters for high efficiency applications as well as the hardwareimplementation and verification.The literature review in Chapter 2 will show thestate-of-the-art status of related research for SiC power semiconductors and high efficiency three-phase converters, which will help todefine the challenges and research objectives of this work.

Table 1-1.Comparison of inverter efficiencies based on different power devices[13]

	Switching Frequency					
	10 kHz			**20 kHz**		
Temperature	**Inverter Efficiency (%)**					
	Si	**SiC**	**Hybrid**	**Si**	**SiC**	**Hybrid**
70 °C	95.10	97.10	96.00	92.20	95.70	93.82
105 °C	94.50	97.00	95.80	90.70	95.60	93.52
Temperature	**Inverter Energy Loss (kJ)**					
	Si	**SiC**	**Hybrid**	**Si**	**SiC**	**Hybrid**
70 °C	771.68	458.57	627.52	1280.70	681.69	997.23
105 °C	879.42	468.22	663.72	1552.30	691.82	1049.00

1.2 DissertationOrganization

This work provides the methodology and deals with the related issues of high efficiency three-phase ac converter's design and development using SiC power devices.The chapters are organized as follows.

Chapter 2 reviews the research activities in the corresponding areas of high efficiency three-phase ac converters and the development status of Silicon Carbide (SiC) power devices and

modules. Based on the review, the research challenges in these areas and the objectives of this dissertation are pointed out.

Chapter 3 develops and evaluates a SiC JFET and Schottky barrier diode (SBD) based six-pack power module for three-phase voltage source converters in wide temperature range. In addition, the effects of package parasitic inductance on SiC JFET behavior and converter efficiency are analyzed. Finally, a three-phase voltage source converter based on this power module is tested, and 98.5% efficiency is obtained.

Chapter 4 studies the performance of a SiC MOSFET and SBD when they are applied in three-phase current source converters. The double pulse test (DPT) circuit based on a current source circuit is developed to evaluate their switching behaviors. In addition, the effects of parasitic capacitance on power devices' behaviors in three-phase current source converters and converter efficiency are discussed. To reduce the power device switching loss, an inductive snubber is proposed for current source converters in this chapter.

Chapter 5 designs and develops a 7.5 kW three-phase current source rectifier as the front-end rectifier in high voltage DC architecture data center power supplies, using commercial SiC MOSFETs and SBDs. The methods of devices' paralleling number selection, switching frequency selection, modulation scheme, and filter design and loss minimization are presented. The converter efficiency of 98.54% is achieved in the experiment at full load.

Chapter 6 proposes a master-slave control for paralleled three-phase current source rectifiers to balance the output currents. A 19 kW front-end rectifier system, based on three paralleled all-SiC rectifiers designed in Chapter 5, is developed for data center power supplies. With proposed master-slave control, the rectifier module hot-swap and (2+1) system redundancy are achieved.

Chapter 7summarizes the work in this dissertation, and points out the future work in related areas.

Chapter 2 LiteratureReview

This chapter reviews the research activities in the corresponding areas of high efficiency three-phase ac converters, and the development status of Silicon Carbide (SiC) power devices and modules.The research challenges and objectives are proposed next to identify the originality of the work.

2.1 Silicon Carbide (SiC) Power Devices and Modules

2.1.1 SiC Power Devices

Since the early 1990's, the silicon (Si) IGBT has been the power switch of choice in industrial applications. The following development of Si IGBT technology has further enhanced the IGBT performance[14]. With increasing global emphasis on energy efficiency, improved power devices are critical to the development of the next generation of power conversion systems. The development of wide bandgap (WBG) power seimconductors are making a revolutionary change in power elctronics. Silicon carbide (SiC) is in the forefront amongst the WBG material based devices. SiC power devices are expected to replace the Si devices in high voltage, high temperature, and high frequency applications because of their advantages of high breakdown voltage, fast switching, low on-state resistance, high temperature tolerance, as well as high thermal conductivity. The key material properties are listed in Table 2-1 for main WBG semiconductors compared with Si, the most used material in power electronic devices, and GaAs which is mainly used for very high frequency applications [15]. SiC device technology has matured over the past few decades and is transitioning from research to commercial production. The main SiC power device products are rectifiers based on Schottky or junction barrier diodes.

A few companies are offering active power devices as well.

Table 2-1.Physical properties comparison of semiconductors[15]

	"Classical" Semiconductors		Wide Bandgap Semiconductors				
	Si	GaAs	3C-SiC	6H-SiC	4H-SiC	GaN	Diamond
Bandgap Energy E_g (eV)	1.12	1.4	2.3	2.9	3.2	3.4	5.6
Electron Mobility μ_n ($cm^2V^{-1}s^{-1}$)	1450	8500	1000	415	950	2000	4000
Hole Mobility μ_p($cm^2.V^{-1}.s^{-1}$)	450	400	45	90	115	350	3800
Critical Electric Field E_C ($V\cdot cm^{-1}$)	3×10^5	4×10^5	2×10^6	2.5×10^6	2.2×10^6	5×10^6	1×10^7
Saturation Velocity v_{sat} ($cm\cdot s^{-1}$)	1×10^7	2×10^7	2.5×10^7	2×10^7	2×10^7	2×10^7	3×10^7
Thermal Conductivity λ ($W\cdot cm^{-1}\cdot K$-)	1.3	0.5	5	5	5	1.3	20
Dielectric Constant ε_r	11.7	12.9	9.6	9.7	10	8.9	5.7

The specific on-state resistance $R_{on,ps}$, which tells directly how much resistive loss a device generates in the forward conduction mode, is the key property for power devices. The $R_{on.sp}$ is usually given in $m\Omega cm^2$ and can be calculated from (2-1) below [16]

$$R_{on,sp} = \frac{4V_B^2}{\varepsilon\mu_n E_C^3} \tag{2-1}$$

whereV_B denotes the breakdown voltage and E_C is the critical electrical field.Figure 2-1 schematically illustrates the electric field distribution in a one-sided abrupt junction for SiC and Si at the same breakdown voltage [17]. Since the E_C of SiC is about 8~10 times higher than that

of Si, the advantage of using SiC devices can be easily understood.

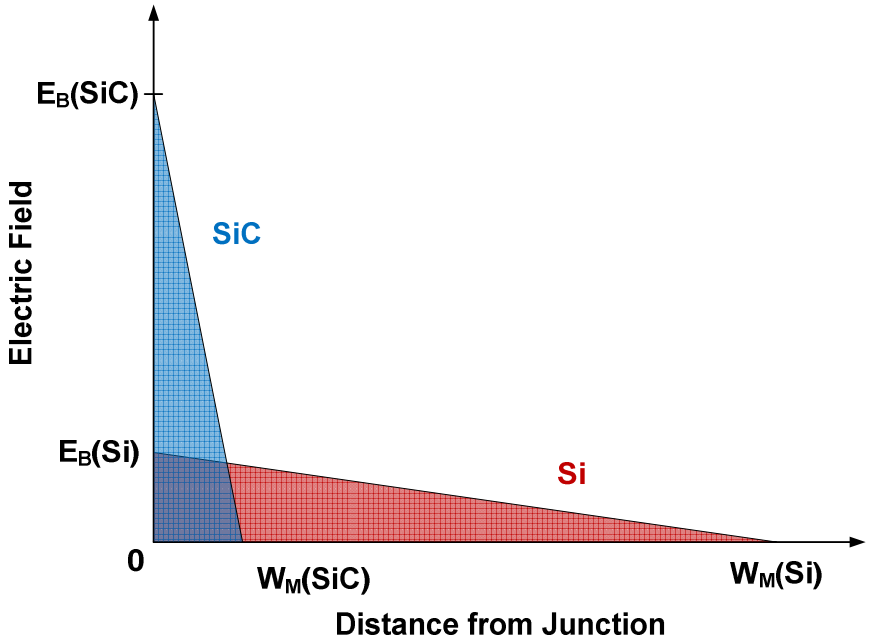


Figure 2-1. Schematic illustration of the electric field distribution in a one-sided abrupt junction for SiC and Si at the same breakdown voltage [17].

In Si, unipolar devices (mainly Schottky barrier diode and MOSFET) are not considered for operating voltage above a few hundred volts, because of their increase in resistivity. SiC, however, offers a much lower resistivity to make unipolar devices a sensible choice for high voltage [15].Figure 2-2 shows the major applications of Si and SiC power devices in terms of the rated blocking voltage. It is expected that SiC unipolar devices will replace Si bipolar devices in the blocking voltage range from 300 V to about 4500 V. For ultra-high voltage applications above 4500 V, SiC bipolar devices will be attractive [17].

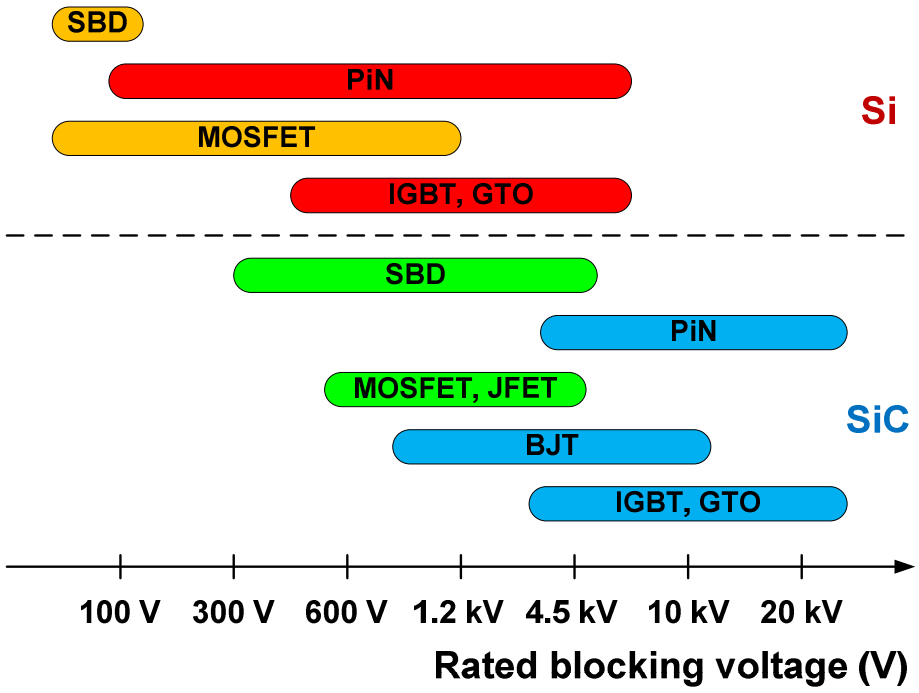


Figure 2-2. Major applications of Si and SiC power devices in terms of the rated blocking voltage [17].

A. SiC Schottky diode

SiC diode is the first commercial SiC power semiconductor and has been widely used in many application areas, such as power supplies, motor drives, and renewable energy systems. The main SiC power device providers, like Infineon and Cree, are all provide commercial SiC Schottky diodes with 600 V, 650 V, 1200 V, and 1700 V voltage rating[18]-[20]. The main advantage of the Schottky diode is the absence of reverse recovery current during switching which reduces the switching loss, hence it is possible to increase the switching frequency which significantly decreases the volume and weight of converters.

B. SiC MOSFET

The SiC power MOSFET is attractive. It operates normally-off and with little demand on the drive circuits. The drawback is its oxide layer has poor reliability under high temperature [21]-

[22]. Commercially 1200 V SiC MOSFETs are available from Cree with 24 A and 33 A current ratings [19], and higher current rating (a few hundred Amps) devices are under development [23]. Even through the characteristics and performances of different SiC MOSFET products or engineering samples are presented in many publications, most testing has been limited to the phase-leg in voltage source converters [24]-[26]. The SiC MOSFET performance in three-phase converters, especially in current source converters, still needs further evaluation.

C. SiC JFET

Currently, SiC JFET is considered good candidate of SiC controlled switch. The 1200 V and 1700 V SiC JFETs are available by SemiSouth these years [20]. In 2012, SemiSouth provided 650 V SiC JFET. In addition, Infineon also offers its own SiC JFET with 1200 V voltage rating [27]. SiC JFETs exhibit small capacitances and can thus be operated at high switching speed. From the reliability issue, JFETs are considered as very promising since they rely primarily on pn-junction operation and are not dependent on the quality of gate control dielectrics. Moreover, they provide excellent high temperature operability [16].The main drawback of SiC JFETs is that they are usually normally-on devices, which requires special care when designing gate drives and converters to avoid phase-leg shoot-through. SemiSouth has demonstrated normally-off SiC JFETs. However, the operational threshold voltage margin is limited, the on-resistance is higher because it is limited by the pinched off region, and they have a limited temperature of operation[16]. The SiC JFET/Si MOSFET cascode structure is one solution for the normally-on characteristic, where SiC JFET is packaged in a cascode connection with a Si MOSFET to provide normally-off operation [28]-[29]. However, the drawbacks of using this structure includes: 1) effective on-resistance is increased, 2) switching time and loss are increased, 3) junction temperature is limited by the Si MOSFET [30]. Although much work has been done on

gate drive circuits [31]-[33], the characteristics of normally-on SiC JFET still needs to be investigated especially in voltage source phase-leg and converters. The issues of further studies include paralleling operation, package parastics, and temperature influence, etc.

D. SiC BJT

SiC BJT is also attractive as high-voltage switching devices due to its low conduction loss combined with fast switching. The BJT operation in the forward direction is beneficial for reaching low on-state loss since the two built-in pn-junctions cancel each other, hence the on-state loss is mostly dependent on the drift layer resistance and the substrate resistance [16]. In addition, SiC BJTs have good performance for high temperature application and are easy to connect in parallel, since current gain decreases and their losses tend to reduce as temperature increases [16], [34]. Increased complexity in drive circuit and certain base current in steady state which causes high driving power are drawbacks of BJTs [35]-[37].

E. Other SiC devices

Other SiC bipolar switching devices such as thyristors and IGBTs are attractive for very high-voltage applications such as electric power transmission[17]. Reference [38] reports 6.2-12.7 kV SiC gate turn-off (GTO) thyristors and their operation at 250 °C. Fabrication of 10 kV SiC IGBTs and the performance comparison with SiC MOSFETs have been reported [39]. In addition, Cree has demonstrated both p-IGBTs and n-IGBTs with better performances than Si IGBTs with half the voltage rating[16].

2.1.2 SiC Power Modules

An interesting issue is to assemble and package the full power module based in SiC power devices in order to take full advantages of SiC devices and increase power density as well. Since

SiC diode is the first commercial SiC power semiconductor and has been widely used, many hybrid modules consist of SiC Schottky diodes and Si devices (Si MOFETs or Si IGBTs) are commercially available [40]-[41].

In recent years, with the fast development of SiC active switches, several works have been done on the design, fabrication, and test of all-SiC power modules. U. S. Army Research Lab (ARL) has reported their SiC MOSFET power modules fabricated by Powerex, including single switch module with 1200 V, 100 A rating in [42]-[43], and phase-leg modules in [44]-[45] with 400 A and 800 A current rating respectively. The high current rating is realized by paralleling power devices of SiC MOFETs and SiC junction barrier Schottky (JBS). General Electric (GE) has used internally fabricated 1200 V, 15 A SiC MOSFET devices and 1200 V, 10 A anti-parallel JBS diodes to form 150 A single switch modules[24]. In addition, Cree, GE, and Powerex also present a 10 kV, 120 A phase-leg module with SiC MOSFETs and JBSdiodes in [46]. Moreover, 1200 V, 20 A SiC MOSFETs and 1200 V JBS diodes per switch, manufactured by Cree, are used by Powerex to fabricate a dual 100 A half-bridge module evaluated in high temperature pulse testing by the Air Force Research Laboratory (AFRL)[47]-[48]. The maximum temperature of all SiC MOSFET modules mentioned above does not exceed 200 ºC.Arkansas Power Electronics International (APEI) reports their development of 250 ºC SiC MOSFET phase-leg power module in [49]-[50], with 1200 V, 160 A rating. In addition, the module of Toshiba is also reaches 250 ºC in [51].

Table 2-2. Summary of recent published all-SiC power modules

Group	V_{BR}	I	Maximum Temperature	Devices & Paralleling	Type	References
ARL	1200 V	100 A	200 ºC	MOSET × 2	Single switch module	[42], [43]
ARL	1200 V	400 A	150 ºC	MOSET × 2 JBS × 6	Phase-leg module	[44]
ARL	1200 V	800 A	150 ºC	MOSET × 11 JBS × 11	Phase-leg module	[45]
GE	1200 V	150 A	175 ºC	MOSET × 10 Schottky diode × 15	Single switch module	[24]
Cree, GE, Powerex	10 kV	120 A	125 ºC	MOSET × 12 JBS × 6	Phase-leg module	[46]
Powerex, AFRL, Cree	1200 V	100 A	200 ºC	MOSET × 5 JBS × 3	Phase-leg module	[47], [48]
				MOSET × 2 JBS × 2		
APEI	1200 V	160 A	250 ºC	MOSET × 8	Phase-leg module	[49], [50]
Toshiba	1200 V	10 A	250 ºC	MOSET × 1 JBS × 1	Phase-leg module	[51]
UTK, UI, GPE	1200 V	30 A	200 ºC	JFET × 3 SBD × 1	Phase-leg module	[52]
APEI	1200 V	5 A	250 ºC	JFET × 2 SBD × 2	Three-phase module	[53]
ARL	15 kV	3 A	200 ºC	JBS	Full-bridge rectifier module	[54]
TranSiC	1200 V	36 A	175 ºC	BJT × 6 SBD × 6	Single switch module	[55]

For a SiC JFET based power module, the University of Tennessee, Knoxville (UTK), University of Idaho (UI) and Global Power Electronics (GPE) developed a 1200 V phase-leg module using three normally-on SiC JFETs in parallel and one SiC SBD in each switching element[52]. A three-phase power module is presented in [53] by APEI, but the power rating of it is 4 kW. For other SiC power modules, reference [54] shows a full-bridge rectifier module based on SiC JBS with high blocking voltage of 15 kV. TranSiC presents a module consisting of six paralleled 6 A, 1200 V BJTs paired with six commercial SiC Schottky diodes[55]. Table 2-2summarizes some of the all-SiC power modules published in recent years.

Even through much work has been done on all-SiC power modules and great development has been achieved, three-phase, high power, and high temperature SiC power modules still need to be developed to meet the requirements of high power, high density, and high efficiency for bridge power converters. In addition, several other issues on SiC power modules should be studied, e.g. the influence of parastics, introduced by module packaging,on devices' performances especially for normally-on switches. The development of all-SiC three-phase converters based on three-phase power modules also needs more experience.

2.2 High Efficiency Converters

2.2.1 Efficiency Characteristics of Power Converters

For a power conversion system, the input power and output power are P_I and P_O, respectively. The power loss of the system is P_{loss}. They satisfy

$$P_I = P_O + P_{loss} \tag{2-2}$$

As a result, the efficiency of a power conversion system is

$$\eta = \frac{P_O}{P_I} = \frac{1}{1+\frac{P_{loss}}{P_O}} \approx 1 - \frac{P_{loss}}{P_O} \tag{2-3}$$

This section gives a brief introduction of the characteristics of $\eta = \eta(P_O)$.

Each converter is modeled as having a combination of three types of losses

$$P_{loss} = P_{loss,0} + P_{loss,1} + P_{loss,2} = k_0 + k_1 P_O + k_2 P_O^2 \tag{2-4}$$

where the parameters k_0, k_1, and k_2 are constant values.

The component $P_{loss,0} = k_0$is independent of the output power, and ismainly composed of the auxiliary system loss, caused by gate drivers, sensors, control electronics, forced cooling, etc.Furthermore, there are contributions from the capacitive switching losses of the power semiconductors.

The component $P_{loss,1} = k_1 P_O$is linearly dependent on P_O, often caused by approximately linearly current dependent switching losses of power semiconductors. Power semiconductors with largely current independent forward voltage drop (diodes and IGBTs or generally speaking bipolar semiconductor elements) also contribute to this part. In addition, $P_{loss,1}$ is caused by core losses of inductive components.

The loss component $P_{loss,2} = k_2 P_O^2$characterizes quadratically current dependent, i.e. ohmic loss components. The typical examples are conduction losses of power MOSFETs, the winding losses ofinductive components, as well as the losses in capacitorsas a result of the equivalent series resistance (ESR).

In the following, only one loss component is considered at a time, in order to show the influence of the individual power loss component contributions on the efficiency characteristic and shaping of efficiency curve.

If only the constant losses $P_{loss,0}$ is considered, from (2-3)

$$\eta_0 = \frac{1}{1+\frac{P_{loss,0}}{P_O}} \approx 1-\frac{k_0}{P_O} \tag{2-5}$$

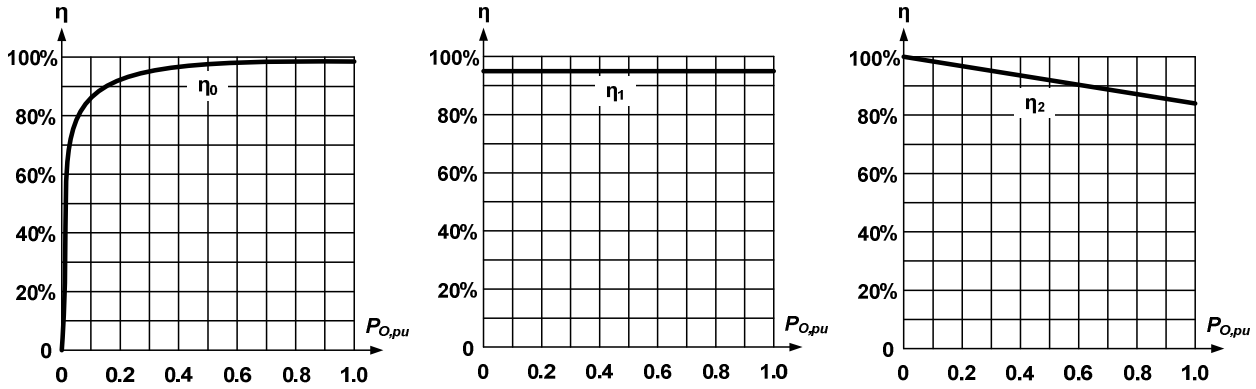
The influence of this loss component on the efficiency falls with increasing output power, as Figure 2-3(a) shows. The efficiencyη_0 reaches values near to 1 for high output power. For low output power, however, the efficiency curve is inevitably dragged to zero for P_O = 0. This component is the dominant part of loss at light load. Hence, higher light load efficiency can in any case only be attained by minimizing the constant losses.

If only the output power proportional losses $P_{loss,1}$ is considered, from (2-3) the efficiency η_1 is constant with the increasing of output power $P_{O,}$ as shown in Figure 2-3(b).

$$\eta_1 = \frac{1}{1+\frac{P_{loss,1}}{P_O}} \approx 1-k_1 \tag{2-6}$$

The the quadratically current dependent losses$P_{loss,2}$ reduces with the increasing of output power, as shown in (2-7) and Figure 2-3(c). At P_O = 0, $P_{loss,2}$related efficiency component η_2 = 1 is reached.For a high efficiency at the rated operating point, one should in all cases aim for a minimization of the conduction losses of power devices and the ohmic resistances of passive components.

$$\eta_2 = \frac{1}{1+\frac{P_{loss,2}}{P_O}} \approx 1-k_2 P_O \tag{2-7}$$



(a) Only constant losses (b) Only linear on the output power dependent losses (c) Only quadratic on the output power dependent losses

Figure 2-3. Effect of the loss components on the efficiency characteristic[5].

From the analysis above, the efficiency of a power converter is

$$\eta = \frac{1}{1+\frac{k_0}{P_O}+k_1+k_2P_2} \approx 1-(\frac{k_0}{P_O}+k_1+k_2P_O) \tag{2-8}$$

In order to obtain maximum efficiency, $\frac{k_0}{P_O}+k_1+k_2P_O$ needs to be minimized, and this happens when the loss components $P_{loss,0}$and $P_{loss,2}$are equal [5].

$$P_{loss,0}\Big|_{\eta\max} = P_{loss,2} \tag{2-9}$$

At this time, the maximum value of efficiency is

$$\eta_{\max} = 1-k_1-2\sqrt{k_0k_2} \tag{2-10}$$

whichoccurs at

$$P_O\Big|_{\eta\max} = \sqrt{\frac{k_0}{k_2}} \tag{2-11}$$

2.2.2 Power Converter Efficiency Improvement

A. Auxiliary system losses and gate drive losses

From the analysis above, the losses of an auxiliary circuit is independent of the output power and dominates the total loss of a power converter at light load operation. The power consumption of auxiliary circuits includes the losses of current/voltage sensors, digital control electronics (DSP, FPGA, etc.), and fans for forced air cooling. This part of loss could be minimized by proper control measures e. g. reduction of the clock frequency of the digital control electronics or by a temporary deactivation of the fans at partial load [5]. For systems with ultra-high efficiency, fans could be omitted completely.

If a unipolar gate drive circuit is assumed, the gate drive loss will be

$$P_{loss,G} = V_G \cdot Q_G(V_G) \cdot f_{SW} \tag{2-12}$$

whereV_G is the gate voltage after turn-on, $Q_G$is the gate charge and depends on the switched voltage. f_{SW} is the switching frequency.$P_{loss,G}$is increased by paralleling more power devices since $Q_G$also increases,and is proportional to the switching frequency.

B. Passive components losses

For the passive components, capacitors are considered first. Electrolytic capacitors achieve high power density due to their high capacitance per volume. However, the losses in the electrolytic capacitors due to the equivalent series resistance (ESR) and leakage current are significantly higher than film capacitors [56]. Thus, film capacitors are required for high efficiency converter designs. The loss of a capacitor is given by

$$P_{cap} = I_{C,rms}^2 \cdot R_{ESR} \tag{2-13}$$

R_{ESR} is dependent on the frequency and can be calculated with the dissipation factor *tan* δ[5],

$$R_{ESR}(f) = \frac{\tan\delta(f)}{2\pi fC} \tag{2-14}$$

The reduction of the capacitor losses is only possible through paralleling of multiple components in order to reduce the effective R_{ESR}.

The loss minimization can only be done based on the detailed modeling of the low and high frequency components of the iron and copper losses of magnetic components. The core loss P_{core} can be calculated using the modified Steinmetz equation [57], and it is assumed that $\beta \approx 2$ [5],

$$P_{core} \propto f_{SW}^{\alpha} \cdot \Delta B^{\beta} \cdot V_{core} \propto\approx \frac{l^3}{l^4} \propto \frac{1}{l} \tag{2-15}$$

where*l* is the dimension of the core, V_{core} is the volume of the core, ΔB is the flux density ripple caused by current ripple Δi_L

$$\Delta B = \frac{L \cdot \Delta i_L}{N \cdot A_e} \propto \frac{1}{A_e} \propto \frac{1}{l^2} \tag{2-16}$$

L is the inductance value, A_e is the inductor core cross-sectional area, and N is the number of turns. The winding loss $P_{winding}$ can be estimated according to [5], [58]

$$P_{winding} = I_{L,rms}^2 R_{L,DC} + \sum_{n=1}^{m} \frac{\Delta I_{L,n}^2}{3} R_{L,ac,n} \propto \frac{l}{A_W} \propto \frac{1}{l} \tag{2-17}$$

whereA_W is the wire cross-sectional area, $R_{L,DC}$ is the inductor dc resistance, and $R_{L,ac,n}$ is the ac winding resistance due to skin and proximity effect resulting from the *n*th harmonic of the inductor current ripple $\Delta i_{L,n}$. The $R_{L,ac,n}$ can be calculated using the Ferreira method [59] and $R_{L,DC}$ can be calculated by

$$R_{L,DC} = \frac{\rho \cdot N \cdot l_T}{A_W} \tag{2-18}$$

ρ is the resistivity of the wire and l_T is the average length of a turn.

From (2-15) and (2-17), both core and winding losses are decreasing with increasing linear dimension *l*.This tendency is shownin[60]. In some applications, e. g. transportation systems, there is the requirement of high power density. As a result, the dimension of the inductor is limited. In the real converter design, the designer should make a selection to minimize power losses and considering power density at the same time.

The selection of switching frequency determines the inductor loss directly. Generally, the optimization regarding the switching frequency must be performed for the overall system, i.e. the power devices' switching losses and power density of the converter have to be considered.

C. Power devices losses

As the dominant part of total loss of high power three-phase AC converters, the power device loss needs more efforts to minimize in order to achieve high efficiency of the whole system.

The straightforward design approach to reduce the conduction loss of a power device is to increase the semiconductor die area, by replacing devices with larger die area or paralleling devices. However, this approach has its own limitation, because with the increasing of die area and reduction of conduction loss, the parasitic capacitance of the power semiconductor, which determines the switching loss, increases.References[5] and[60]give the analysis of the influence of die area on the loss of Si power MOSFET. Based on the calculation of the energy (E_{Coss}) stored in MOSFET output capacitance (C_{oss}), the linear capacitance can be defined as

$$C_{E,eq}(V_{ds}) = \frac{4}{3} \cdot C_{oss}(V_{ds}) \tag{2-19}$$

from the relationship

$$E_{Coss}(V_{ds}) = \frac{1}{2} \cdot C_{E,eq}(V_{ds}) \cdot V_{ds} \tag{2-20}$$

where the values of $E_{Coss}$and C_{oss}depend on the MOSFET drain-source voltage V_{ds}. The power MOSFET will be

$$P_{MOSFET} = I_{ds,rms}^2 \cdot R_{ds-on} + \frac{1}{2} \cdot C_{E,eq}(V_{ds}) \cdot V_{ds}^2 \cdot f_{SW} \tag{2-21}$$

If the on-state resistance and the equivalent capacitance are set in relation to the Si power MOSFET chip area A_{Si}

$$R_{ds-on} = \frac{R_{ds-on}^*}{A_{Si}}, C_{E,eq} = C_{E,eq}^* \cdot A_{Si} \tag{2-22}$$

(2-21) will be

$$P_{MOSFET} = k_1 \cdot \frac{1}{A_{Si}} + k_2 \cdot A_{Si} \cdot f_{SW} \tag{2-23}$$

wherek_1 and k_2 are coefficients. As a result, the optimal Si power MOSFET die area of

$$A_{Si} = \sqrt{\frac{1}{f_{SW}} \cdot \frac{k_1}{k_2}} \tag{2-24}$$

can be obtained for the minimum MOSFET loss of

$$P_{MOSFET,\min} = 2\sqrt{k_1 \cdot k_2 \cdot f_{SW}} \tag{2-25}$$

For a power IGBT, there is a fixed voltage drop even at lower current region. In order to reduce the conduction loss, a hybrid switch in the form of MOSFET and IGBT parallel operation is proposed in [61]. The advantage of this switch combination is to have MOSFET conducting the current at low current and IGBT conducting the high current. The voltage drop at low

currents is proportional to current, and at high currents, it is dominated by the IGBT.

In addition, the increase of die area allows lowering the thermal impedance by increasing cooling area and thus lowering the junction temperature which helps to reduce the loss of the device.

Soft switching techniques are widely used to eliminate power device switching loss. For example, it has been used in many kinds of topologies of DC-DC converters, such as a push-pull converter [62], LLC converter [63], and full-bridge converter [64]. In [63], the zero-voltage switching (ZVS) operation is realized for all power devices under all operating conditions to make LLC converter suitable for high switching frequency operation. In [64], the proposed hybrid-switching phase-shift full-bridge DC-DC converterprovides wide ZVS range in the leading-leg switches, achieves zero-current switching (ZCS) for lagging-leg switches, and uses a hybrid-switching method to avoid freewheeling circulating losses in the primary side.

Moreover, the soft switching technique is also popular in AC converters. A typical example is the single phase PFC [65]-[68]. In addition, this approach is realized in three-phase AC inverters by introducing a quasi-resonant circuit in the DC link [69], or adding resonant magnetics, snubber capacitance, and an auxiliary switch for each main switch, to establish zero-voltage condition for the main switches [61], [70]-[72]. In [61], the 99% peak efficiency of a 55 kW three-phase voltage source inverter for hybrid electric vehicles is obtained, using ahybrid switch and soft switching techniques. The main drawback of implementing soft switching is the need for extra circuitry and components, which tends to increase the size, cost, and the complexity of the circuit and control.

Another approach to reduce power semiconductors switching loss is to improve their gate

drive circuit.The traditional method is to the reduce gate resistance to reduce switching time. Recently, significant works have been done on active gate drives to reduce power devices' switching loss. A multi-step driving technique which provides reduction of the reverse recovery current has been proposed in [73]. In [74], the gate capacitance of the IGBT is charged with relatively small current in order to limit the collector current slope and reverse recovery current as a consequence. As a result, the collector emitter voltage tail and turn on losses are reduced. A gate driver based on the gate emitter voltage measurement and the Miller's plateau detection is proposed in [75] to reduce switching loss. The collector current slope control without a feedback circuit is proposed and analyzed in [76], and the additional regulation of the collector emitter voltage slope is reported in [77]. Reference [78] controls both di/dt at turn-on and dv/dt at turn-off for an IGBT. Moreover, the gate drive which can reduce switching loss on both IGBT and MOSFET is provided in [79].

The improvement of control scheme is another approach to increase the efficiency of power converters. The proper selection of modulation scheme for a three-phase PWM converter can reduce the switching loss of power devices in the converter. One typical example is the discontinuous space-vector PWM (DPWM), which is also called minimum-loss space-vector modulation (SVM) or 60º clamped SVM. DPWM shows 50% switching loss reduction compared with continuous space-vector PWM because the phases carrying the highest current in each 60º of line cycle are not switched [80]. For current source three-phase PWM converters, the Modified Fullwave Symmetrical Modulation (MFSM) has the minimum switching losses of the current source converter (CSC) bridge irrespective of the displacement power factor angle[81]. The idea of MFSM is to avoid switch commutations which will result in unfavorable switching voltages. The switching voltage is unfavorable if the switch commutation is performed to the

bridge leg which results in the absolute value of switch voltage is the highest of all line-to-line voltages at the moment of the commutation. The method is improved for current source rectifier (CSR) with DC link freewheeling diodes in [82]-[83], and shown to minimize power devices switching loss in [84]-[85].

The control algorithm for different topologies can be improved to minimize power loss of converters in some special applications.For example, for full-bridge series resonant inverter, the asymmetrical voltage-cancellation control for different load quality factors and a power control based on pulse densitymodulation are proposed in [86] and [87] respectively, to allow the inverter to work close to the resonant frequency to minimize losses.Another example of the variable switching frequency is used in EV/HEV to minimize inverter losses [88]-[89]. This method is also proposed in other applications, like PV inverter and half-bridge series resonant inverter [90]-[91]. Some other control strategies focus on the light load efficiency improvement, like the predictive current control for single-phase PFC [92] and pulse-skipping control for grid-tied inverter [93].

Different topologies of converters show different efficiency characteristics in different applications, so the proper selection of topology is also an important step to achieve high efficiency. Take three-phase converters as an example. From reference [94], for unidirectional rectifiers, the three-level Vienna six-switch rectifier is the best solution for high switching frequencies considering power conversion efficiency. On the other hand, three-level T-type rectifiers display better efficiency for low switching frequencies[94]. In addition, three-level hybrid rectifiers (combination of line- and self-commuted rectifiers) constitute the natural choice for high switching frequency operation, while the two-level hybrid rectifiers could only be better for very low frequencies. For three-phase motor drives, reference [95]shows that multilevel

neutral point clamped voltage source inverter (NPC-VSI) has the highest efficiency for 1 MW motor rated at 2.4 kV. However, the losses of the voltage-source topology are nearly 50% higher than those of the current-source thyristor-based topology for 20 MW motor rated at 6.6 kV and 2.2 kA.

In addition, for some applications, improvement of existing topologies can also help to increase the converter efficiency, such as the improved single-phase PV inverters in [96]-[98], and bridgeless PFC with reduced conduction losses in [99]-[100].

The proper management of paralleled converters can also improve the efficiency of the whole paralleling system. The DC uninterruptable power supply (UPS) is a paralleling system of several AC-DC rectifiers. Not all of the rectifier modules provide output power at partial load, in order to achieve near-peak UPS efficiency at light system load [101]. Moreover, the interleaving of paralleled converters can reduce current and voltage ripples to reduce passive components' losses. In addition, the switching frequency can be reduced by interleaving which achieves the reduction of switching loss. Since the losses of power components are closely related to the operation temperature, good thermal design and management will help to minimize power losses too.

2.2.3 SiC Based Power Converters

The development of SiC power semiconductors provides another way to increase the power converter's efficiency due to the advantages of SiC devices discussed in 2.1. Here, only three-phase convertersbased on SiC devices, the focus of this dissertation, are surveyed and introduced.

The SiC diode is first used in three-phase converters combined with Si active switches. In [102], a 55 kW voltage source inverter (VSI) using Si IGBTs and SiC Schottky diodes is

developed for hybrid electric vehicles (HEVs) by Oak Ridge National Laboratory (ORNL). A 5 kW current source rectifier (CSR) is designed for data center and telecommunication power supplies by ETH in Switzerland in [58] using SiC Schottky diodes combined with Si MOSFETs, and 98.8% efficiency is achieved at full load.

Moreover, SiC active switches are expected to replace Si switches to further improve the performance of power converters including efficiency.The high efficiency of SiC based converters for HEV and wind turbine have been demonstrated in [103]-[104], respectively. The all-SiC three-phase converters are being developed worldwide.An AC-DC converter was designed for > 100 ºC ambient temperature by theCenter for PowerElectronics Systems (CPES)at Virginia Tech using a power module integrating three-phase diode-bridge and DC-DC boost converter [105]. Three-phase voltage source converters (VSCs) are also built up in[52],[106]-[109]. A 4 kW SiC JFET based VSI is successfully tested at 200 ºC in [106]. APEI has built a high temperature all-SiC VSI using silicon on insulator (SOI) gate driver in [107], which was tested at 4 kW. A 10 kW high power density prototype converter consists of a Vienna-type rectifier front-end and a two-levelVSIwas developed by CPES using SiC JFETs and Schottky diodes [108]. In addition, another high density VSI of 25 W/cm^3 is demonstrated by Toshiba in [109]. The 98.2% peak efficiency of a 18 kW VSI using SiC phase-leg module is achieved in [52]. Even though, quite a lot of excellent works have been done on all-SiC voltage source converters, further development of high power, high efficiency, all-SiC three-phase voltage source converters is still necessary for the applications which require high power density and high temperature. Six-pack SiC-based power module with high temperature packaging is needed for high temperature and/or high efficiency applications. The related issues of the six-pack module on the VSC efficiency should be studied.

The works on all-SiC current source converters (CSCs) are fewer than on VSCs. The main purpose of using SiC devices in CSCs is to increase switching frequency in order to reduce the large and heavy DC link inductors. A 2 kW, 100 kHz current source inverter (CSI) was developed in [110]. CPES has demonstrated current source rectifier (CSR) with 2 kW power rating, 150 kHz switching frequency in [111]. In addition, ETH has built a 3 kW, 200 kHz back-to-back (BTB) CSC in [112]. All of these CSCs use SiC JFETs and Schottky diodes. The all-SiC CSC focusing on high efficiency still needs more research and experience with hardware implementation.

2.3 Research Challenges and Objectives

According to the survey above, there are many unsolved issues on the newcharacteristics of SiC devices and the influences of their losses. The design of all-SiC three-phase converters needs more research. The main challenges include:

(1) Development of high power six-pack power module with high operating temperature capability based on paralleled SiC power devices.

(2) Understanding and explanation of parasitics' impacts on SiC devices' behaviors in both three-phase voltage source and current source converters.

(3) Evaluation of devices' performances in three-phase current source converters.

(4) Methodology to maximize the benefit of SiC devices in the design of high efficiency three-phase converters.Loss minimization of three-phase current source rectifier.

(5) Development and implementation of paralleled current source rectifiers with balanced outputs and hot-swap capability.

Corresponding to the challenges listed above, the objective of this work is to model, design, and analyze three-phase voltage source converters and current source converters using SiC power devices to achieve high power conversion efficiencies and verify the developed concepts with hardware. There are six main tasks in this dissertation:

(1) Develop a six-pack all-SiC 200 ºC power module andevaluatethe phase-leg static and dynamic characteristics. Develop a gate drive for paralleled normally-on SiC JFETs and analyze current sharing between JFETs and anti-parallel diodes.

(2) Analyze the influence of package parasitic inductance on normally-on SiC JFET switching behaviors and switching loss.

(3) Analyze current commutation in current source converters and develop double pulse test circuit based on current source structure. Evaluate behaviors of SiC MOSFET in current source converters.

(4) Analyze the influence of parasitic capacitance on the SiC power devices' switching behaviors in current source converters.

(5) Design and develop the high efficiency three-phase front-end rectifier using SiC power devices for data center and telecommunication power supplies.

(6) Design and develop the paralleled three-phase front-end rectifiers using SiC power devices to achieve high efficiency, considering output balance, system redundancy, and hot-swap.

Chapter 3 SiC JFET Power Module Evaluation for Voltage Source Converters

As discussed in Chapter 2, SiC power devices are expected to be widely used in high efficiency converters, and SiC JFET is considered a good candidate for SiC controlled switches. Many publications present SiC JFET and SiC JFET based power module and power conversion systems in recent years[52]-[53], [106], [113]-[114]. However, most of the published SiC JFET power modules are single phase-leg modules [52], [114]. The modules in [53], [106]are three-phase modules, but the power rating of them is 4 kW. Therefore, high power, three-phase SiC power modules still need to be developed for high efficiency applications, while achieving high power and high density at the same time. In addition, some issues of SiC devices based power module, such as parasitics influence and phase-leg shoot-through during fast switching [115], need to be solved.

In this chapter, a fully integrated SiC JFET based three-phase power module is designed and developed. Additionally, a three-phase two-level voltage source inverter based on this power module is tested, and high efficiency is obtained. The chapter is organized as follows: the six-pack SiC JFET power module with its assembly processes is described in 3.1.The static characteristics of the module are shown in 3.2.In 3.3, the switching test setup and test results are presented.The parasitic inductance influence on switching behavior of SiC devices in voltage source converters is discussed in 3.4. In 3.5, a three-phase voltage source inverter based on the SiC JFET power module is tested. Finally, conclusions are given in 3.6.

3.1 SiC JFET Based Six-Pack Power Module

Figure 3-1 shows the picture of a SiC JFET based power module with 1200 V and 100 A power rating. The module size is 140 mm × 70 mm × 12.7 mm. The module consists of a three-phase bridge configuration with each switching element having four 4.17 mm × 4.17 mm 1200 V normally-on SiC JFETs from SiCED and two 2.7 mm × 2.7 mm 1200 V SiC Schottky barrier diodes (SBDs) from SiCED in parallel.

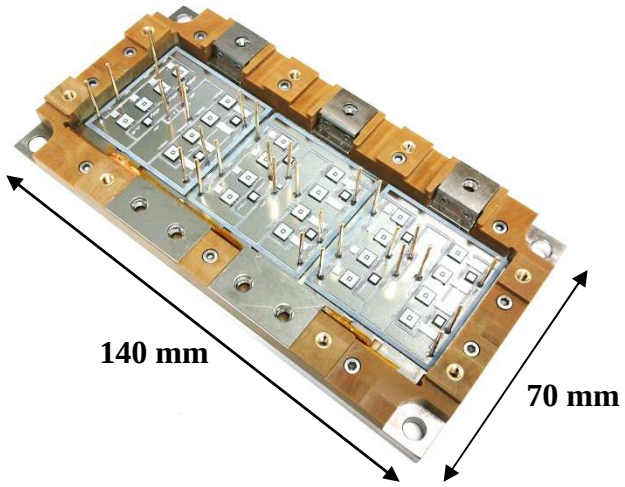
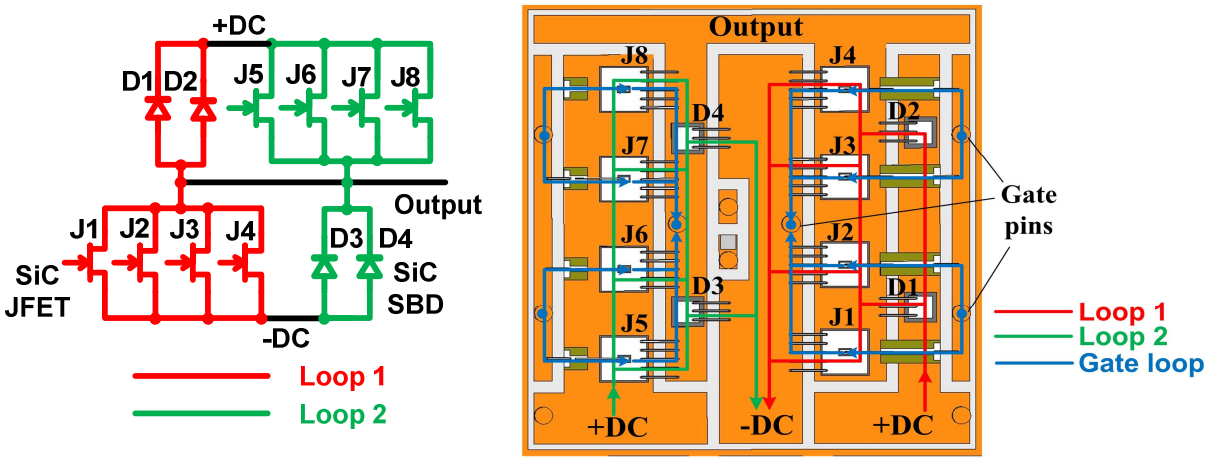


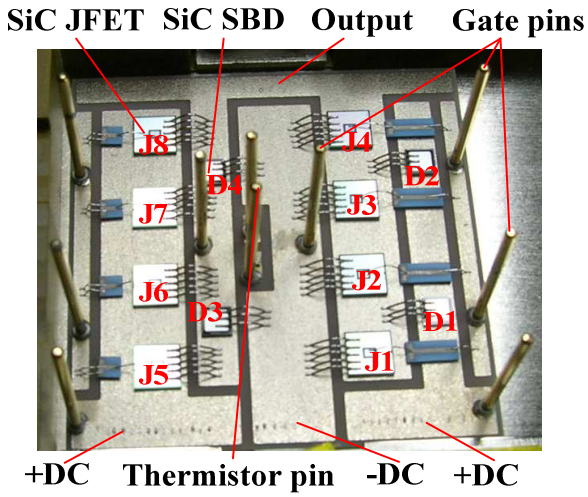
Figure 3-1. Six-pack SiC JFET based power module.

Each phase-leg is designed in a separate substrate, 38.5 mm × 38.5 mm. Figure 3-2(a) shows the phase-leg circuit. The basic switching cell theory proposed in [116] is used during the phase-leg layout design. As shown in Figure 3-2(b), the devices in the commutation loop are placed at the same side. Thus, the physical length of the commutation loop is specifically reduced compared with a conventional module layout, in which the JFET and its anti-parallel diode are seated at one side. This layout design leads to the reduction of parasitic inductance in the natural current commutation path. The gate loop layout, shown in Figure 3-2(b), is composed of two

control pins placed between the two closer JFETs to make the distance evenly distributed among four paralleled JFETs. This step is necessary in order to balance gate loop parasitics in the module. Figure 3-2(c) is the phase-leg picture.



(a) Phase-leg circuit (b) Phase-leg layout



(c) Phase-leg picture

Figure 3-2. Six-pack SiC JFET based power module structure for a single phase-leg.

The package of the module is designed to work at a junction temperature of at least 200 ºC. The components and manufacturing processes that have been used can be broken down into

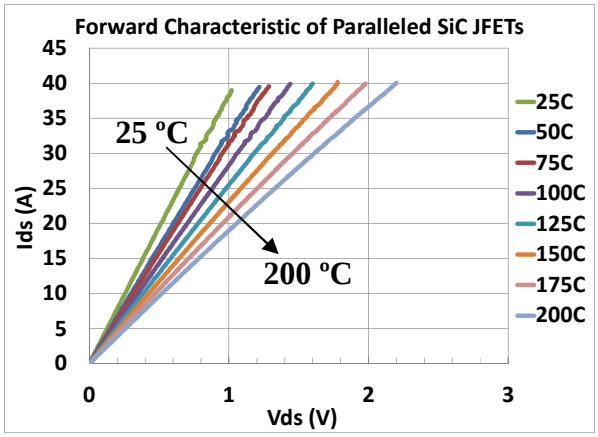
several key pieces: die-attach, wire bonding, substrates, and housing/encapsulation.The SiC JFETs and SBDs are bonded to the active metal bonding (AMB) Cu [117]-[118] on Si_3N_4substrates with lead based solder that melts at a temperature of 310 ºC.The source and gate connections for the JFETs and SBDs connections are formed using 99.99 % pure 5 mil diameter Al wire bonds. In order to avoid very long gate wire bonds, the thin film Al on ceramic or glass ceramic shunts are used.To form the complete three-phase inverter, three substrates are bonded to a Ni plated Cu molybdenum alloy base plate and connected in parallel by connecting the substrates to common +DC and -DC terminals. To sample the source voltages and control the gate-source voltages (V_{gs}), Au over Ni plated brass control pins are bonded to the metal traces on the direct bond copper (DBC) substrates. The pins are bonded with lead based solder that is used for die bonding. The housing is mounted on the baseplate that is machined from a glass filled polyimide material, torlon 5030. The housing is used to support the busbars, Ni plated Cu, and contain the encapsulation gel, Nusil Gel 8100, during the curing process.All switching components and interconnects are isolated from the heat sink baseplate. For simplifying system assembly and thermal management, the interconnection to the DC voltage input terminals and the phase-leg output terminals are assigned as a screw terminal type. The module also includes three thermistors to monitor the substrate temperature.

3.2 Static Characterization

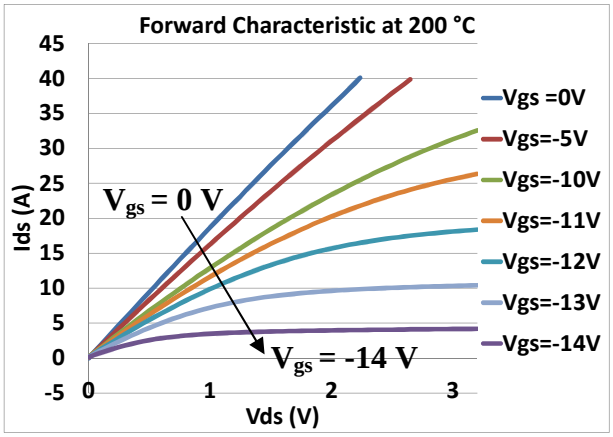
The static characteristics of the switching element in the module are obtained with a curve tracer at various temperatures from 25 °C to 200 °C, as shown in Figure 3-3. In the test, the module is heated with a hot plate with a thermocouple as the temperature monitor.The forward characteristics of switching element are obtained at JFET gate-source voltage (V_{gs}) of 0 V, as shown in Figure 3-3(a).Figure 3-3(b) shows the forward characteristics at different gate-source

voltage at 200 °C. Figure 3-3(c) illustrates the transfer characteristic at different temperatures. Since the JFETs are normally-on devices, the pinch-off voltage ($V_{pinch-off}$) is negative. From Figure 3-3(c), the pinch-off voltage is lower with increasing temperatures, from -16 V at 25 °C to -17 V at 200 °C.Figure 3-3(d) shows the reverse characteristics of the switching element measured with the JFETs blocked by V_{gs} of -22 V, in which both the anti-parallel diodes and JFET body diodes are considered. The threshold voltage (V_{th}) decreases with rising temperatures. And the slope of the linear region becomes shallower with rising temperatures, which means the series resistance (R_D) in the diode increases.

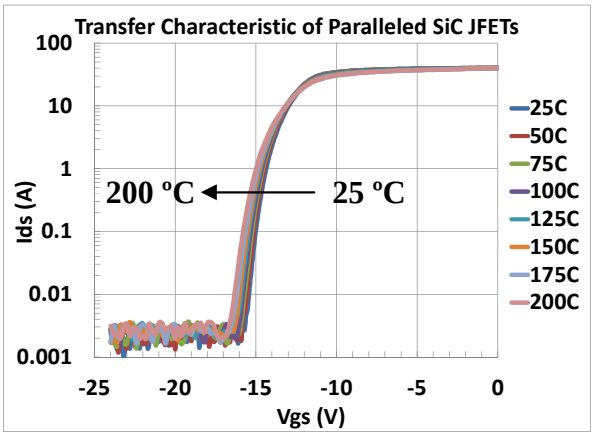
The measurement of the on-state resistance of the JFET is based on the slope of the forward characteristic in the linear region. Figure 3-4 shows that the four paralleled SiC JFETs on-state resistance (R_J) changes over a temperature range from 25 °C to 200 °C, at 60 A drain-source current (I_{ds}), at V_{gs} = 0 V. From Figure 3-4, R_J increases with higher temperature, from 25 mΩ at 25 °C to 55 mΩ at 200 °C. The low on-state resistance and high temperature tolerance determine that the low conduction loss of SiC based power module even at 200 °C.



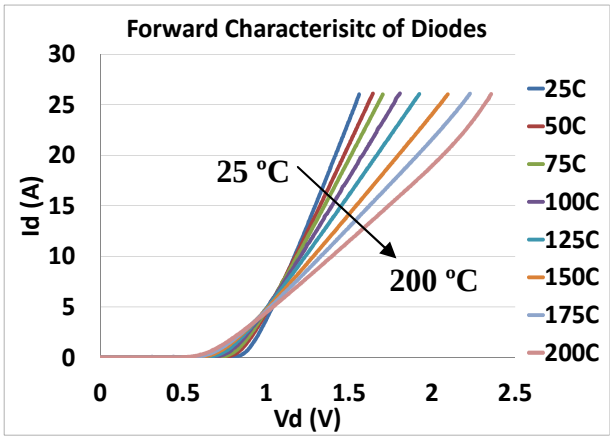
(a) Paralleled SiC JFETs forward characteristic



(b) Paralleled SiC JFETs forward characteristic at 200 °C



(c) Paralleled SiC JFETs transfer characteristic



(d) Paralleled diodes forward characteristic

Figure 3-3. Static characteristics of the switching element in the module.

For a normally-on JFET based power module, when current flows through drain-source direction, only R_J conducts the current, and the conduction loss is given in (3-1). When current flows through source-drain direction, the current will flow in two conditions: when current is smaller than a threshold value, only the JFET conducts, and when the current exceeds this threshold value, both the JFETs and the diodes will conduct current [119]. The switching cell equivalent circuit in this mode is shown in Figure 3-5, and conduction loss is given in (3-2).

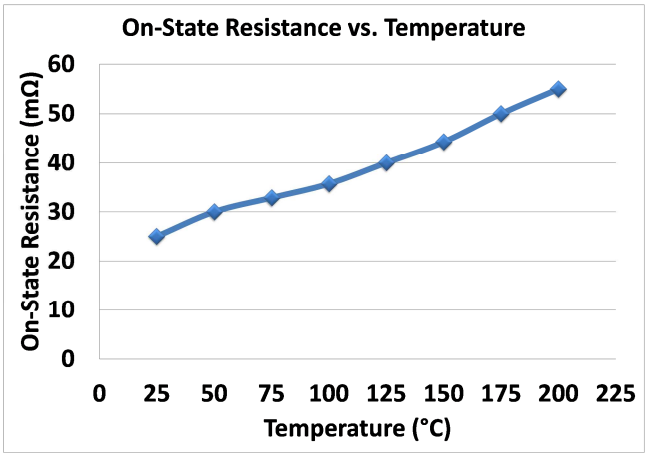


Figure 3-4. On-state resistance of four paralleled SiC JFETs in the module.

$$P_{con} = I^2 R_J \tag{3-1}$$

$$\begin{cases} P_{con} = I^2 R_J & I \le \dfrac{V_{th}}{R_J} \\ P_{con} = \dfrac{V_{th} R_J I + I^2 R_J R_D}{R_J + R_D} & I > \dfrac{V_{th}}{R_J} \end{cases} \tag{3-2}$$

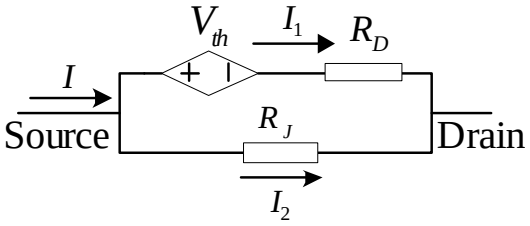
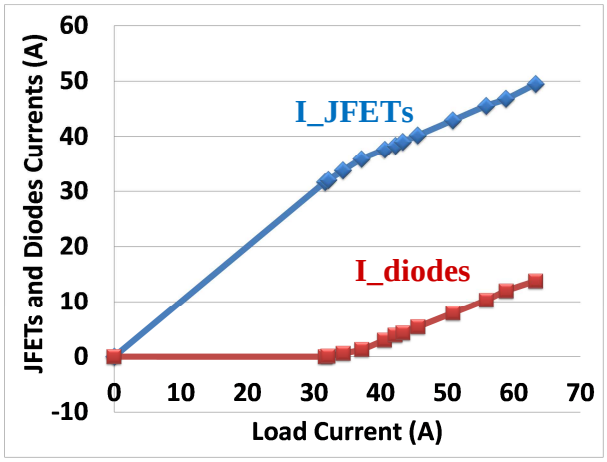


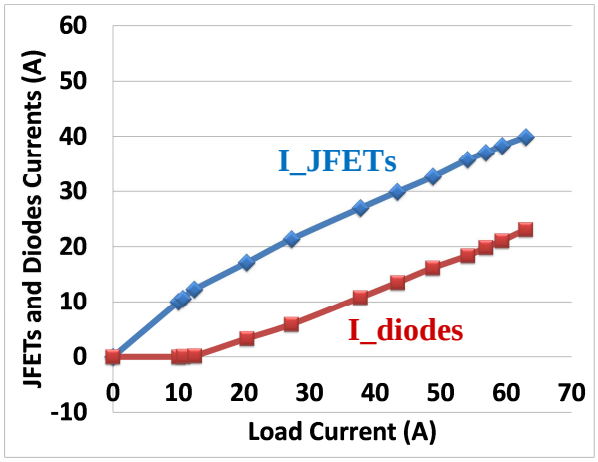
Figure 3-5. Switching cell equivalent circuit when current flows from source to drain.

From Figure 3-3(a) and (d), the reverse diodes start to conduct source-drain direction current at 36 A and 12 A, at 25 °C and 200 °C respectively. The diodes' currents include the currents flowing through both anti-parallel SBDs and JFETs body diodes. Figure 3-6(a) and (b) show the source-drain direction current sharing between JFETs and diodes at 25 °C and 200 °C at different

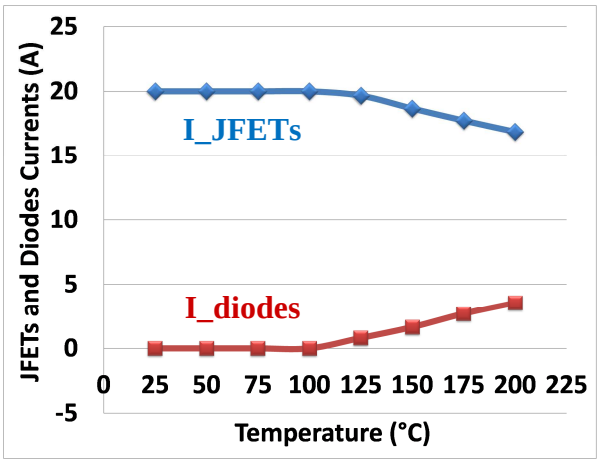
load current levels. Figure 3-6(c)-(d) show the current sharing at different temperatures at 20 A and 60 A load currents, respectively. These figures show that as the temperature increases, the reverse diodes' starting conduction current decreases and the shared current increases. In this SiC JFET based power module, the JFETs channel will conduct more current than the reverse diodes even at 200 °C, 60 A.



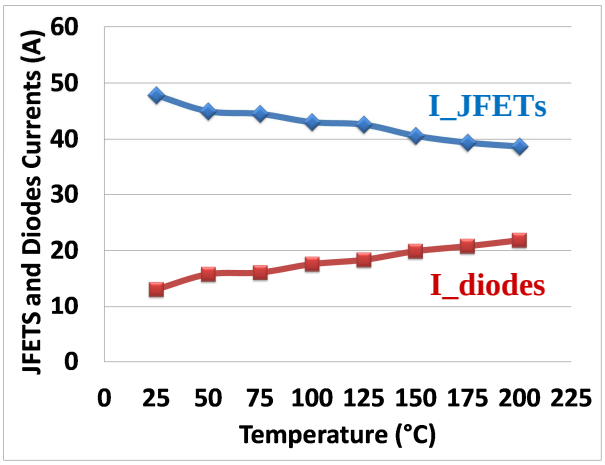
(a) Current sharing at 25 °C at different load current levels



(b) Current sharing at 200 °C at different load current levels



(c) Current sharing at different temperatures at 20 A load current



(d) Current sharing at different temperatures at 60 A load current

Figure 3-6. Source-drain direction current sharing between JFETs and diodes.

3.3 Switching Characterization

The phase-leg switching behaviors of the SiC JFET based power module are evaluated by double pulse test (DPT), at a 650 V dc bus voltage, 60 A current, and junction temperature up to 150 ºC.Figure 3-7 shows DPT circuit with gate drive schematic. Both high side and low side switching elements are four paralleled SiC JFETs with two anti-parallel SiC SBDs. In the test, the four high side JFETs are off, and the double pulse signal is applied to the low side JFETs gate terminal. As shown in Figure 3-8, the load which is a 1 mH inductor with 7 pF equivalent parallel capacitance (EPC)is charged to rated current value at the end of the first pulse.When the low side JFETs are turned off, load current commutates to the high side SBDs. The load current commutates back to the low side JFETs when they are turned on during the second pulse. The self-heating of the devices is not considered. The junction temperature is assumed to be the same as the case temperature because of the slow thermal time constant compared to the pulse duration.

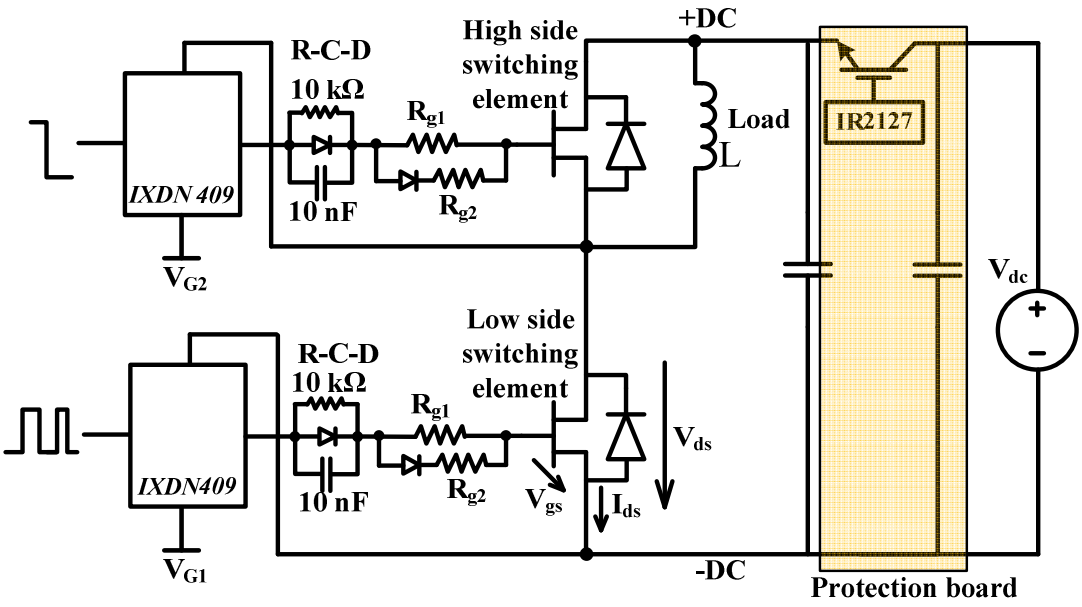


Figure 3-7. Phase-leg DPT circuit of SiC JFET power module with gate drive schematic.

Considering JFET pinch-off voltage measured above, and the devices' -25 V gate breakdown voltage, and their variation in four paralleled JFETs, a value of 0 V for V_{gs} is chosen for turn-on and -22 V for V_{gs} is used for turn-off. The driver IC in DPT is IXDN409 from IXYS. The RCD network is used between the gate driver and JFETs to adapt to the different gate characteristics in case of JFETs paralleling [31]. In Figure 3-7, the turn-on resistor is $R_{g1}//R_{g2}$ = 4 Ω, and the turn-off resistance is R_{g1} = 10 Ω.

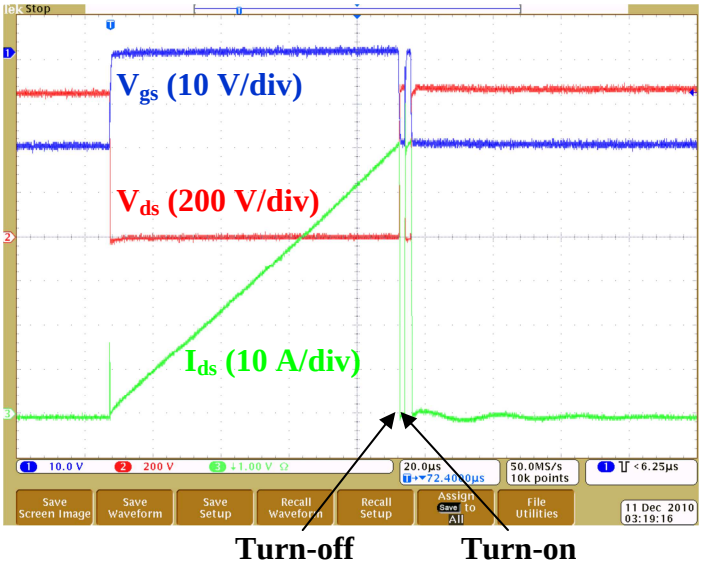


Figure 3-8. Double pulse test waveforms. (Time: 20 µs/div)

In the test, the shoot-through protection of the phase-leg is realized by an IGBT. This IGBT is connected in series with the +DC bus, as shown in Figure 3-7. Once the current exceeds the limit, the IGBT will be turned off to separate the phase-leg from the DC power supply and protect the module. Figure 3-9 shows a photograph of the high temperature testing setup. The module is heated by connecting it to the hot plate. The temperature is monitored by the thermocouple. A fan is used to cool the PCB and the shunt resistor.

For the high-speed switching transients' measurement of the SiC device, the probes should have enough bandwidth in order to capture the fast rising and falling edges of the switching waveforms with sufficient fidelity [120]. According to the signal theory, the effective bandwidth (f_{BW}) of a slope signal with a rise time (t_r) can be expressed as [121]

$$f_{BW} = \frac{0.35}{t_r} \tag{3-3}$$

Based on (3-3), a 20 ns rise time should correspond to a 17.5 MHz bandwidth. The bandwidth of the probes should not be less than 90 MHz, if leaving five times margin. The measurement apparatus used in the test are listed inTable 3-1. In addition, different types of probes possess different propagation delays which need to be compensated. In this work, the coaxial cable is used as the baseline, compared to which P6139 has 2.5 ns delay and P5100 has 9.8 ns delay.

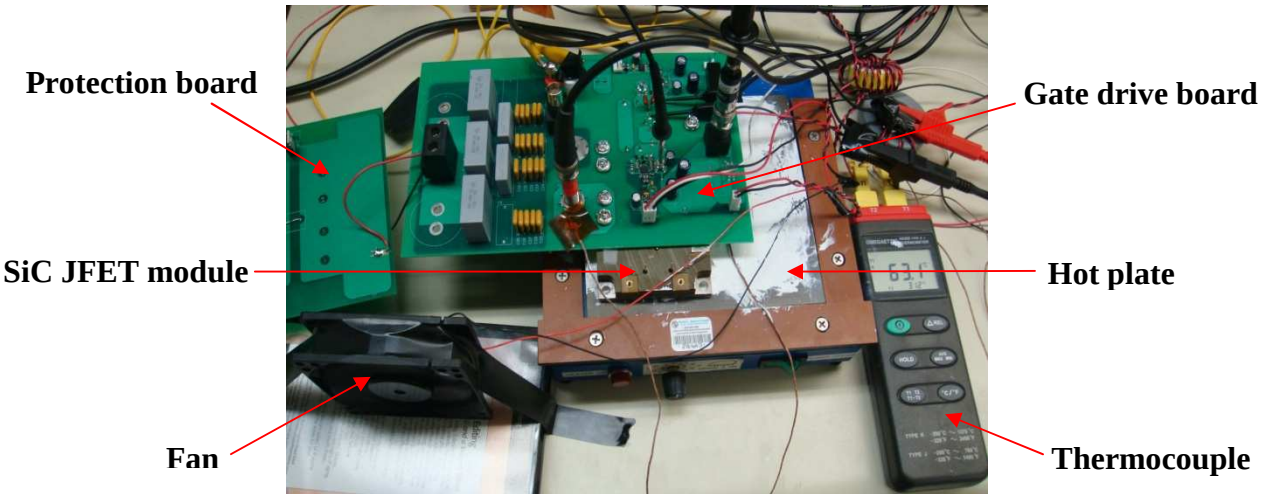
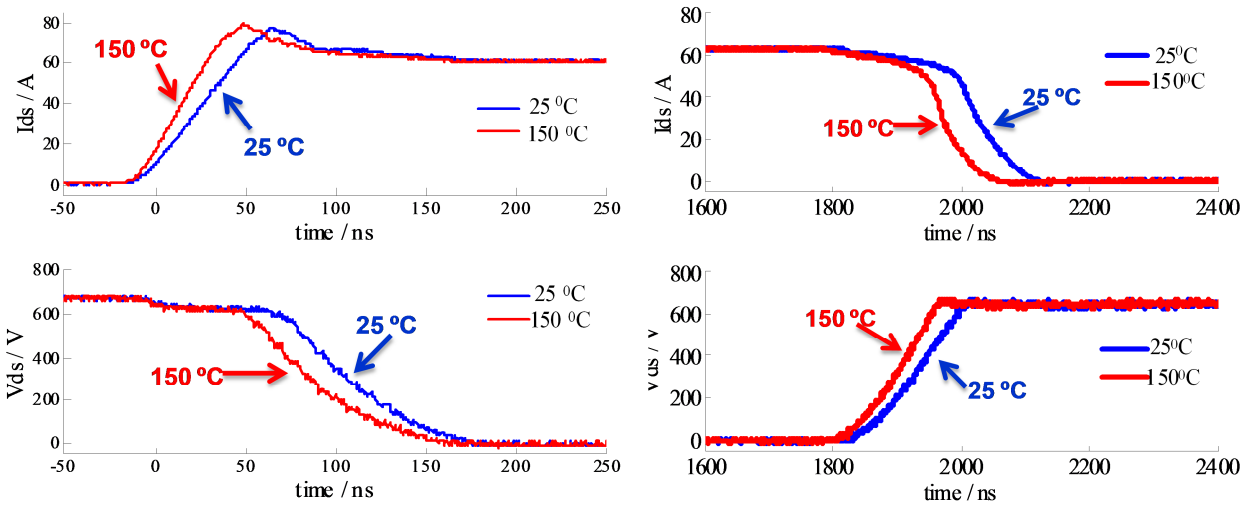


Figure 3-9. High temperature switching test setup.

Table 3-1.Measurementapparatususedinmodule DPT

	Measurement Apparatus	Bandwidth
Oscilloscope	Tektronix DPO 4104	1 GHz
V_{gs}	Tektronix P6139	500 MHz
I_{ds}	0.1 Ω coaxial shunt resistor with 2.2 nH series inductance	2 GHz
V_{ds}	Tektronix high voltage P5100	250 MHz

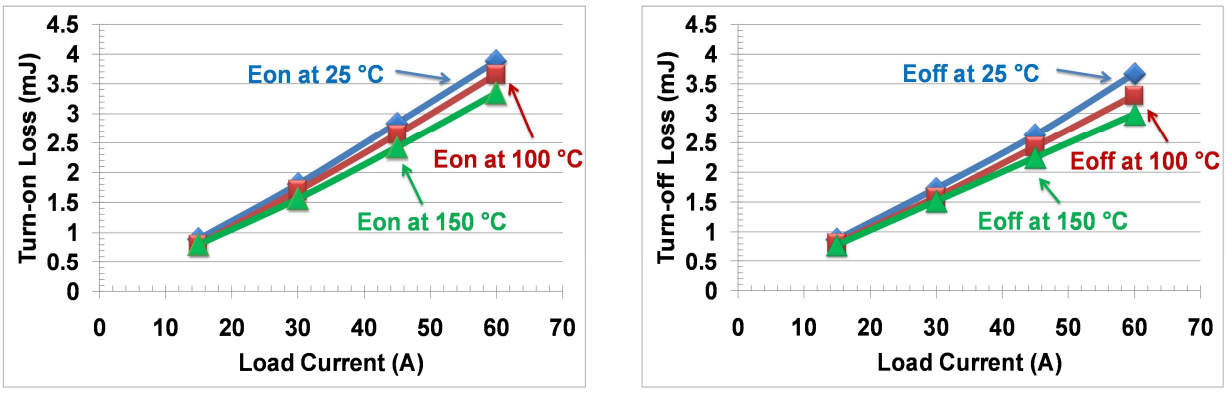


(a) Turn-on waveforms (b) Turn-off waveforms

Figure 3-10. SiC JFET based power module switching waveforms at 650 V and 60 A.

Figure 3-10(a) and (b) show the turn-on and turn-off waveforms of four paralleled SiC JFETs in the module, respectively. The waveforms are obtained with 650 V_{dc} and 60 A. The turn-on overshoot current is 18 A at 150 ºC due to the discharging current of the junction capacitance of the high side JFETs body diodes and anti-parallel SBDs. It is verified in [119] that the use of SiC SBD, which has no reverse recovery, helps to reduce the turn-on overshoot current. From the comparison of the switching waveforms at 25 ºC and 150 ºC in Figure 3-10, it is observed that the SiC JFETs, with anti-parallel SiC SBDs in the module, switch faster at 150 ºC

than at 25 ºC. The turn-on time (t_{on}) is defined as the time from the current rising to 10 % of its peak value until the voltage falls to 10 % of the dc voltage value. Similarly, the turn-off time (t_{off}) is defined from the time the current falls to 90 % until the voltage rises to 90 % of its dc value. At 150 ºC, t_{on} is 140 ns and t_{off} is 170 ns. However, t_{on} is 160 ns and t_{off} is 220 ns at 25 ºC. Fast switching leads to low switching loss. The switching loss calculation covers the whole switching transient. From the tests, the turn-on loss (E_{on}) of four paralleled SiC JFETs in the module's switching element is 3.8 mJ at 25 ºC and 3.4 mJ at 150 ºC. The turn-off loss (E_{off}) is 3.6 mJ and 2.9 mJ at 25 ºC and 150 ºC respectively. Figure 3-11(a) and (b) show the E_{on} and E_{off} as a function of load current at different temperatures, under 650 V_{dc}. Both turn-on and turn-off losses of SiC JFETs, with anti-parallel SiC SBDs in the module, decrease with the temperature increasing. The switching loss of the Si IGBT, IGW60T120 from Infineon which has the same rating as paralleled JFETs in the module, is 9.5 mJ at 25 ºC and 15.8 mJ at 150 ºC, at 600 V_{dc} and 60 A [18]. The comparison shows the low switching loss of a SiC JFET based power module and its benefits used in high efficiency converters, especially at high operating temperatures.



(a) Turn-on loss (b) Turn-off loss

Figure 3-11. Switching loss at 650 V_{dc}voltage with different temperatures.

3.4 Parasitic Inductance Influence on Switching Behavior

Parasitics play significant roles in power devices' and converters' performances. The package parasitics of the SiC JFET based power module are extracted by Maxwell Q3D parameter extractor [123]. Figure 3-12shows the phase-leg circuit with package parasitic inductances, and their values are listed inTable 3-2, which come from the L matrix extracted by Q3D AC analysis at 100 MHz operating frequency, with a 1 % margin of error.The common source inductance is the parasitic inductance shared by the JFET gate loop and the main loop, and the source inductance is the JFET source side parasitic inductance only in the main loop. The gate loop inductance value of each JFET includes the inductance shared by four paralleled JFETs, called common gate inductance, and the inductance only in each JFET gate loop. The common gate inductance includes the mutual couplings of paralleled JFETs gate loops, which are important for paralleled devices switching behaviors [123]. Due to the application of the basic switching cell theory and the devices' gate loop layout, parasitic inductances in both current commutation paths of voltage source converters and JFETs' gate loops are very small.

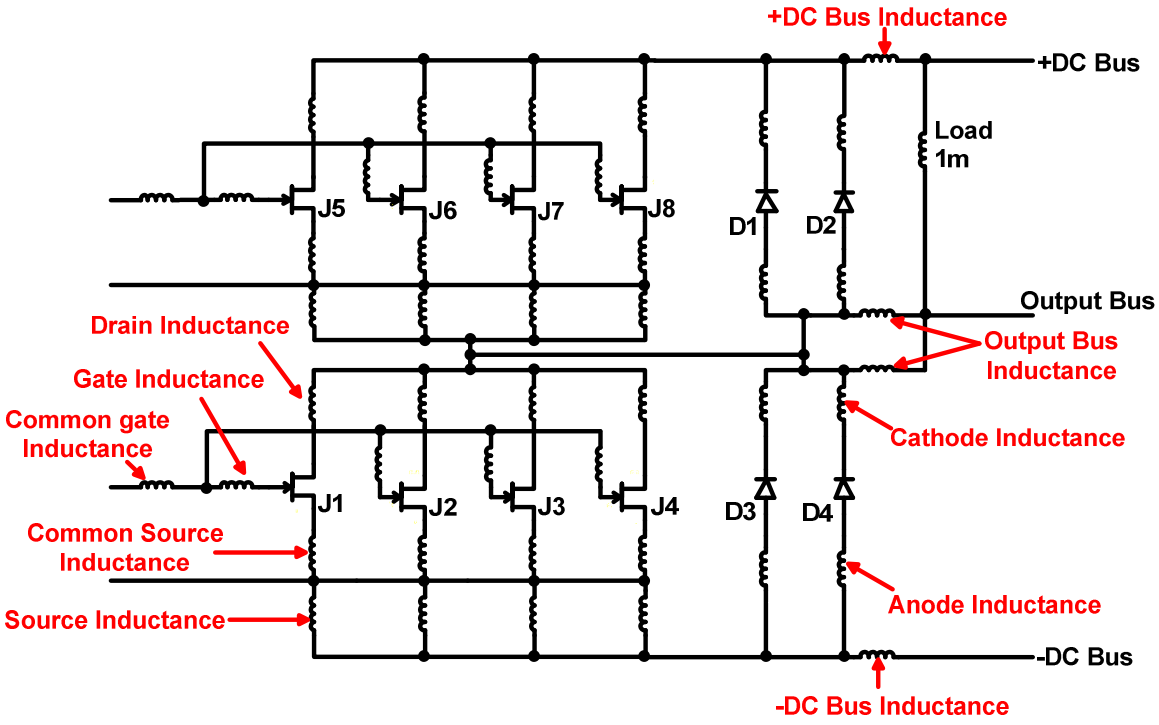


Figure 3-12. Phase-leg circuit with package parasitic inductances.

Table 3-2. Parasitic inductances of the three-phase SiC power module

	J1	J2	J3	J4	J5	J6	J7	J8
Common gate inductance (nH)	4.5				4.3			
Gate inductance (nH)	1.1	1.6	1.3	1.4	0.9	1.4	1.5	1.2
Drain inductance (nH)	3.7	0.4	0.4	3.7	0.7	4.1	8.8	10.1
Common source inductance (nH)	3.9	0.3	0.4	4.1	0.5	0.3	0.4	2.9
Source inductance (nH)	1.6	5.3	10.6	16.5	6.5	2.3	2.0	3.9
	D1		**D2**		**D3**		**D4**	
Anode inductance (nH)	4.5		4.6		6.2		14.2	
Cathode inductance (nH)	3.7		9.2		2.0		1.8	
	+DC bus		**-DC bus**		**Output bus**			
Inductance on bus (nH)	20.3		12.5		9.9		9.6	

It is demonstrated in [25] that the power devices' drain side, source side, and gate loop inductances have significant roles in their switching performances and converter loss.Furthermore, the package parastics will also increase a voltage source converter switching loss by causing phase-leg shoot-through. Shoot-through is defined as both high side and low side switches in a phase-leg being turned on at the same time. It will cause additional power dissipation in the switching devices, increase losses [124], and even damage devices.Shoot-through is mainly caused by high *dv/dt* during a switching transient. The structure of SiC JFET leads to the existence of the intrinsic capacitance, as shown in the circuit inFigure 3-13, which is a crucial factor in determining the switching speed and switching loss.For a normally-on JFET, the capacitor C_{gs} is charged during turn-on transient, and the device will be turned on after V_{gs} exceeds the pinch-off voltage. During turn-off transient, C_{gs} will discharge to reduce V_{gs}. The internal capacitance will also be charged or discharged due todrain and source terminal voltages of JFET vary when other switches are turning on and off, which causes JFET turning-on by varied V_{gs}.

According to Saber simulation of DPT based on the phase-leg circuit shown in Figure 3-12, the key parasitics, which will cause phase-leg shoot-through, include the gate loop inductances and DC bus inductances.The voltage of phase-leg output terminal drops from 650 V to 0 V during low side JFETs turning on in the switching test, shown in Figure 3-13. At this time, current i_g appears in high side JFETs' gate loops because of the existence of JFET internal capacitance. When i_g increases, there is a voltage (V_L) across the parasitic inductance (L_g). Since the external gate voltage (V_G) and V_{gs} are negative values for normally-on JFET turning-off, it is possible that V_{gs} is larger than the JFET's pinch-off voltage if V_L is large enough. Figure 3-14(a) shows the simulation results of high side JFET V_{gs} and channel current with different values of

L_g. It is obvious that large L_g in high side JFET gate loop will cause V_{gs} of JFET to be larger than its pinch-off voltage due to the large V_L.In addition, the JFET internal capacitance will have a charge current (i_{bus}) associated with it on the DC bus, and this current will cause a voltage drop (V_{bus}) across the DC bus parasitic inductance (L_{bus}), as shown inFigure 3-13. This effect may also result in shoot-through since it leads to the high side JFETs drain voltage being higher than DC voltage and therefore increases the *dv/dt* during switching. Figure 3-14(b) shows the simulation results of the high side JFET V_{gs} and channel current with different values of L_{bus}. A large L_{bus} leads to V_{gs} being more than the pinch-off voltage and causes shoot-through.

To avoid phase-leg shoot-through, *dv/dt* need to be reduced which will increase switching loss. Based on the analysis above, power devices' gate loop inductances and DC bus inductances should be kept as small as possible in a voltage converter, in order to obtain high efficiency.

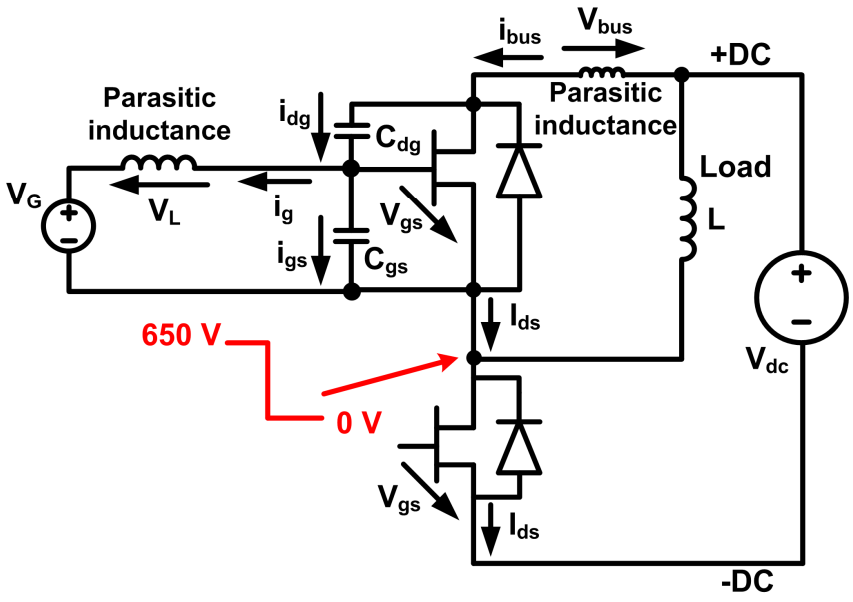
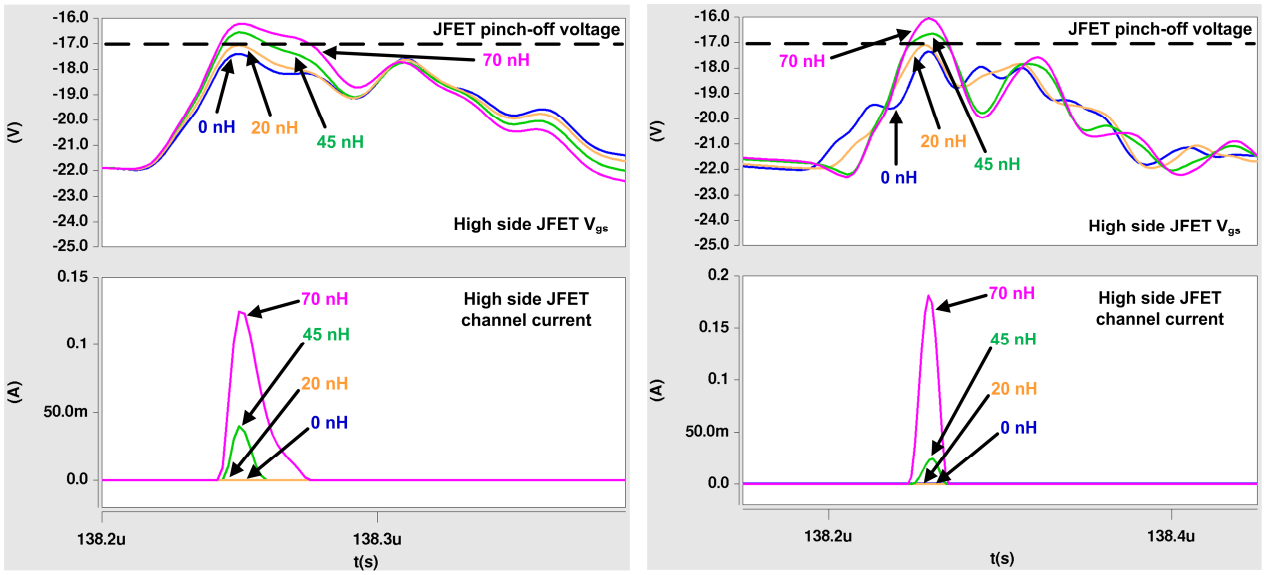


Figure 3-13. Package parasitic impact on phase-leg shoot-through.



(a) High side JFET V_{gs} and channel current with different L_g

(b) High side JFET V_{gs} and channel current with different L_{bus}

Figure 3-14. Gate loop and DC bus parasitic inductances' influence on phase-leg shoot-through.

3.5 Performance in a Voltage Source Converter

Figure 3-15 shows an all-SiC three-phase voltage source inverter, based on the six-pack power module developed and characterized above, developed for EV/HEV applications. The custom gate driver contains circuits for inherently safe operation of the depletion mode JFETs under start-up and fault modes. The DC input consists of metalized 94 μF polypropylene film capacitors with segmented foils to provide short circuit protection. There is an integral input LC EMI filter to reduce conducted line currents. The controller is a Texas Instruments Piccolo TMX320F28035 microcontroller based control card. The input and output power and signal connections are by keyed twist-lock connectors for maximum safety and convenience. This liquid cooled inverter is 22.9 cm × 22.4 cm × 7.1 cm in dimension with a volume of 3.6 liters, and a weight of 3.53 kg.

Figure 3-15. An all-SiC three-phase voltage source inverter prototype.

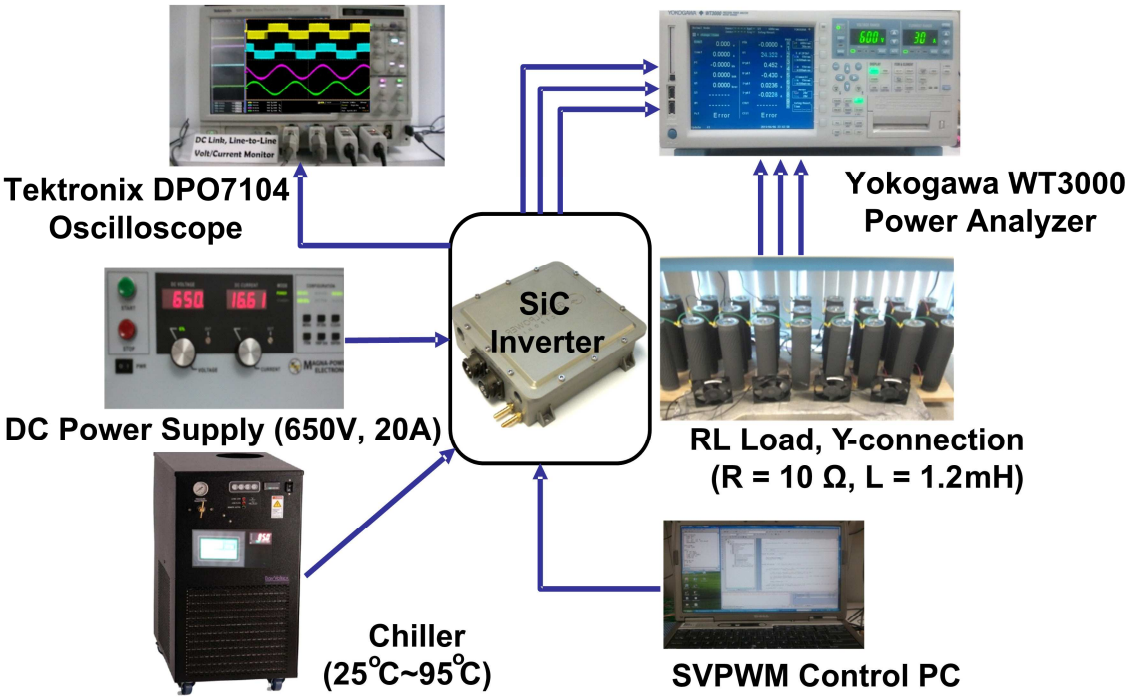
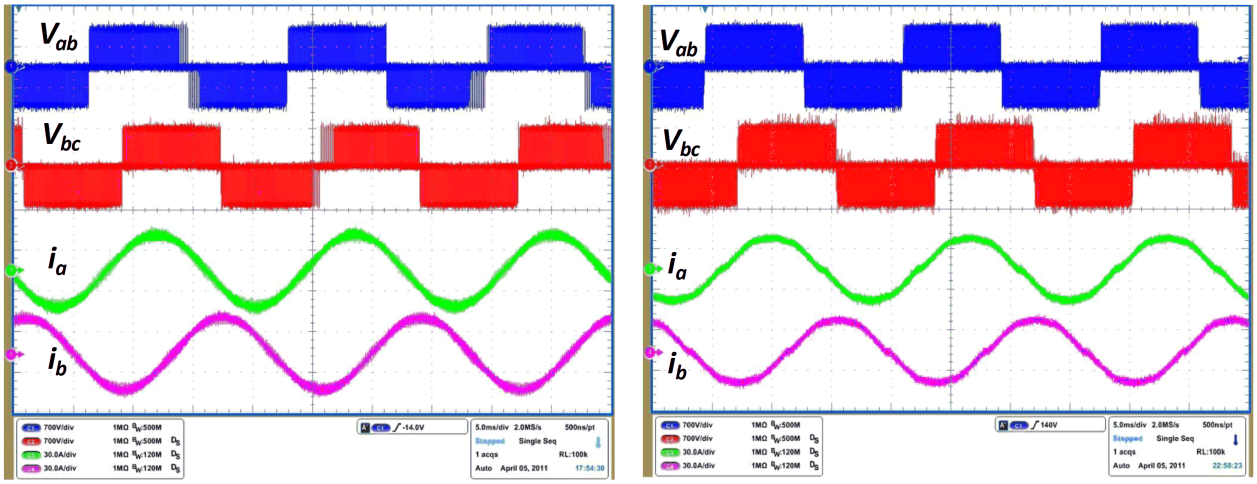


Figure 3-16. All-SiC voltage source inverter test and efficiency measurement setup.

This SiC based voltage source inverter is tested with an RL load. As shown in Figure 3-16,

the inverter is connected to a DC power supply and feeds AC power to a three-phase RL load with Y-connection, where R = 10 Ω and L = 1.2 mH. The switches in the inverter are controlled by space vector pulse width modulation (SVPWM) signals generated by the TMX320F28035 microcontroller board. The chiller changes the coolant temperature from 25 ºC to 95 ºC. The coolant flow rate is set at 6.8 liter per minute (LPM) with 50 % ethylene glycol, 50 % water at the output of the chiller. The input DC voltage (V_{dc}), the input DC current (I_{dc}), the three-phase line-to-line voltage (V_{ab} and V_{bc}), and the line current (i_a and i_b) are monitored and measured by an oscilloscope, Tektronix DPO7104. The power conversion efficiency and the quality of the inverted AC power are monitored and measured using Yokogawa WT3000 Precision Power Analyzer with an accuracy of 0.02 %. For AC side, three-phase three-wire power measurement method is used, and DC side power is obtained by multiplying DC voltage and current.

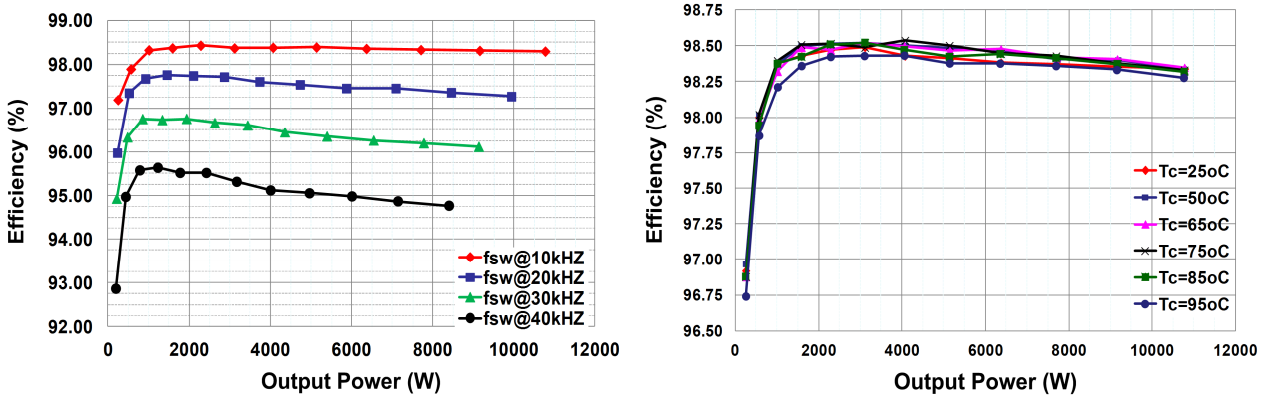


(a) f_{sw} =10 kHz (b) f_{sw} =40 kHz

Figure 3-17. Experimental waveforms of the SiC based voltage source inverter at 650 V_{dc}, f = 60 Hz, M = 0.85 with the RL load, R=10 ohm and L=1.2 mH. (Time:5 ms/div, Vab and Vbc:700 V/div, ia and ib: 30 A/div)

The experimental waveforms of V_{ab},V_{bc}, i_a, and i_b at coolant temperature of 25 ºC are shown

in Figure 3-17. The input voltage is 650 V_{dc}. The frequency of the output current is 60 Hz, and its magnitude is set by a modulation index of 0.85. Figure 3-17(a) shows the waveforms with 10 kHz switching frequency, andFigure 3-17(b) shows the waveforms with 40 kHz switching frequency.



(a) Different output power levels and switching frequencies at 25 ºC coolant temperature.

(b) Different output power levels and coolant temperatures at10 kHz switching frequency.

Figure 3-18. Efficiency of SiC based three-phase voltage source inverter.

The inverter efficiencies are measured at up to 11.4 kW output power with 60 Hz fundamental output frequency and 0.85 modulation index, shown in Figure 3-18. Figure 3-18(a) shows tested efficiencies with different switching frequencies from 10 to 40 kHz, at 25 ºC coolant temperature. The power loss at the gate driver board, which is 5 to 8.5 W depending on the switching frequency, is included in the efficiency measurement. The efficiency curves are measured by changing the DC input voltage with the fixed RL load. The maximum 98.5 % efficiency including the 5 W gate driver power loss is achieved at a switching frequency of 10 kHz at 5 kW output power, 650 V DC voltage.The inverter efficiencies with different coolant temperatures at 10 kHz switching frequency are shown inFigure 3-18(b). The conversion

efficiency degradation at coolant temperature of 95 ºC is less than 0.2 % compared to the measured data at 25 ºC. The experiment results show the benefits of SiC power devices to achieve the three-phase voltage source converter with high efficiency, even at high operating temperatures.

3.6 Summary

In this chapter, a SiC JFET based three-phase inverter power module with 200 °C packaging is designed and demonstrated. Each switching element consists of four paralleled normally-on SiC JFETs with two anti-parallel SiC SBDs. The module static characteristics are tested at temperatures up to 200 ºC, and the current sharing between JFETs' channel and anti-parallel diodes are studied. The low on-state resistance of the SiC power module illustrates the low conduction loss when it is used in voltage source converters. The switching performance of the module is evaluated by a DPT up to 150 ºC, at 650 $V_{dc}$and 60 A, and the results show the shorter transient time and lower switching loss compared with traditional Si IGBT. In addition, the influence of package parasitic inductance on phase-leg shoot-through and switching loss are analyzed. The key parasitics are parasitic inductances in JFET gate loop and module DC bus.Meanwhile, the significance of shoot-through protection and package parasitic inductance reduction for the SiC JFET module is pointed out. Finally, a liquid cooled three-phase voltage source inverter based on this power module is demonstrated, and 98.5% efficiency is obtained at 10 kHz switching frequency at 5 kW output power.

Chapter 4 SiC MOSFET Evaluation for Current Source Converters

Except for voltage source converters, three-phase current source converters are also widely used in high efficiency applications, such as telecommunication and data center power supply systems. The three-phase current source rectifier, with 480 $V_{ac,rms}$ line-to-line voltage input and 400 V_{dc} output, is preferred as the front-end converter in 400 V DC architecture power supply systems [58], since a voltage-source rectifier output is too high (typically 700 – 800 V_{dc}) when connected to 480 V_{rms} line-to-line grid. Compared to the boost rectifier, a buck rectifier provides a wide output voltage control range, and allows for current limitation in case of an output short circuit [125].

In addition, the SiC power MOSFET is the best candidate to replace the Si IGBT in demanding power electronics applications[24]. Even through the reliability of its gate oxide is a problem at high temperatures [24], the SiC MOSFET is still a good choice for high efficiency but not high temperature applications, due to its lower losses compared to Si IGBT. Thus, the characteristics of SiC MOSFETs need to be evaluated in current source converters, which have different current commutation than voltage source converters, in order to meet the requirements of high efficiency applications.

This chapter studies the performance of SiC MOSFETs and SBDs when they are applied in three-phase two-level current source converters. The static characteristics of a commercial SiC MOSFET and a commercial SBD are presented in 4.1. In 4.2, the switching performances of these devices are evaluated for current source converters, based on current source structure DPT. In addition, the parasitic capacitance influence on switching behaviors of SiC devices in current

source converters are discussed and studied in 4.3. An inductive snubber is proposed and studied to reduce SiC MOSFET turn-on loss caused by parasitic capatance in 4.4. Conclusions are given in 4.5.

4.1 Static Characterization

In a three-phase current source converter, the switching element is composed of an active switch and a diode in series, as Figure 4-1 shows. The diode is used to block the reverse voltage. For the PWM control of a current source converter, the zero vectors are always realized by conducting both high side and low side switches, which is different and not allowed in voltage source converters. Because of the series of power devices, the device conduction loss is the dominant part of the total loss in many current source converters. Thus, the SiC power devices have the advantages to reduce conduction loss and enable high efficiency in current source converters, due to their low on-state resistance.

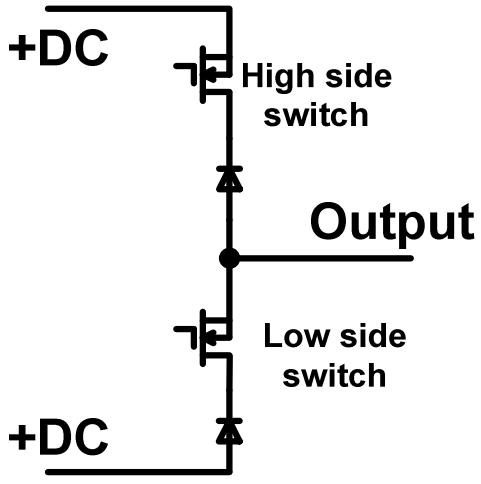


Figure 4-1. Three-phase current source converter phase-leg.

The forward characteristics of 1200 V SiC MOSFET, CMF20120D from Cree[19], shown in

Figure 4-2, is measured by a curve tracer and obtained at various temperatures from 25 °C to 125 °C, at the gate-source voltage (V_{gs}) of 20 V, up to 20 A. The on-state resistance of the MOSFET measurement is based on the slope of the forward characteristic in the linear region. Figure 4-3 shows MOSFET on-state resistance values at different temperatures. They are the average values of five test samples. From Figure 4-3, the on-state resistance of the SiC MOSFET increases with temperature, from 66 mΩ at 25 °C to 76 mΩ at 125 °C.

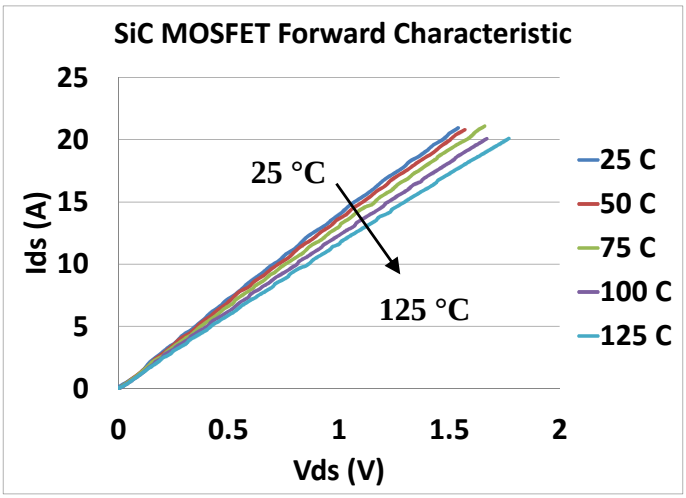


Figure 4-2. Forward characteristic of SiC MOSFET.

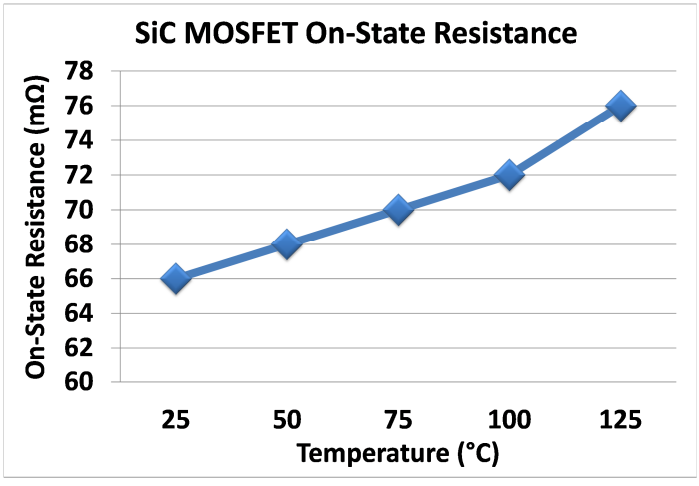


Figure 4-3. SiC MOSFET on-state ressitance.

The SiC SBDs will help to improve the efficiency of current source converters due to their low conduction loss and no reverse recovery. There are two paralleled 1200 V SiC SBDs in SDP60S120D (TO-247) from SemiSouth [20], considering its low conducation loss. Figure 4-4 shows the forward characteristic of each leg from the temperature of 25 °C to 175 °C. The threshold voltage of the diode (V_{th}) decreases with rising temperatures due to the Schottky barrier height reduction with increasing temperatures. Also the slope of the linear region becomes shallower with rising temperatures, which means the series resistance (R_D) in the diode increases.

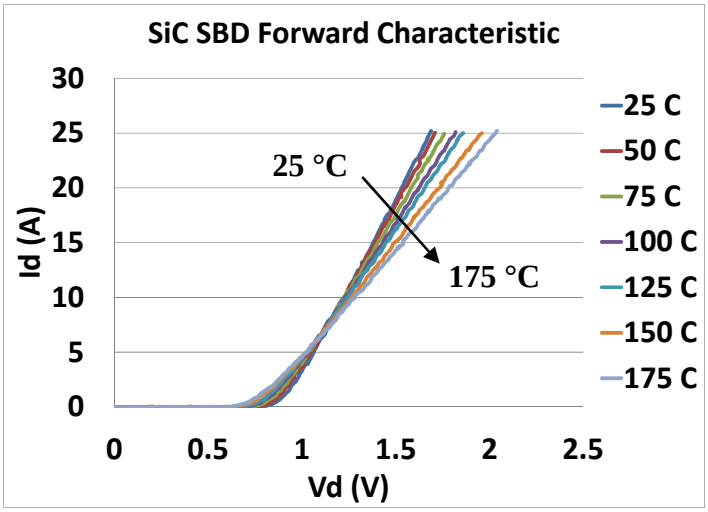


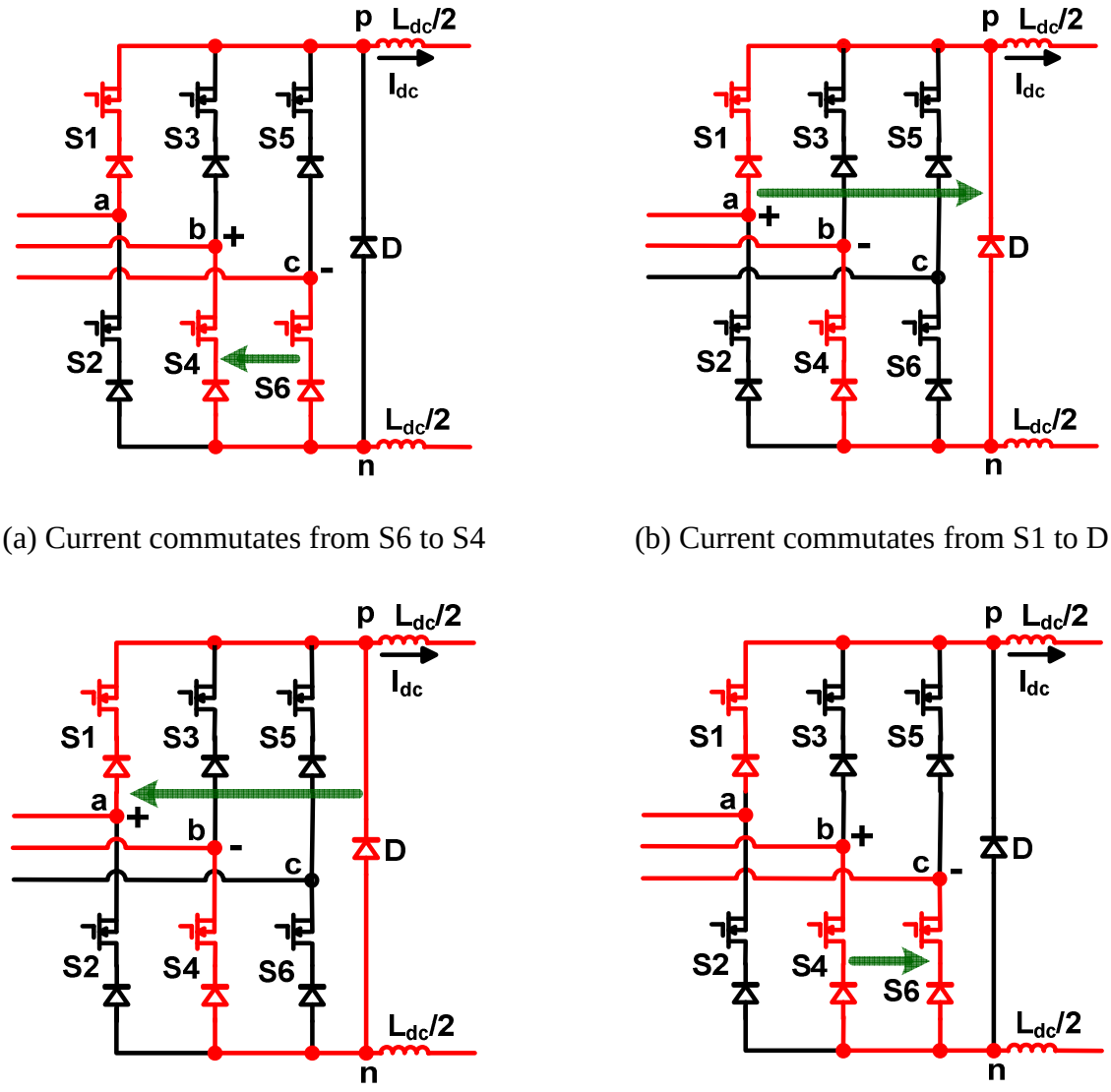
Figure 4-4. Forward characteristic of SiC SBD.

4.2 Switching Characterization

The static characteristic data are not enough for converter design and operation. The switching performances of SiC MOSFET and SBD, used in the current source converters, need to be evaluated with double pulse test (DPT) based on current source structure.

The transition process of current source converters is different with voltage source converters, in which current commutates between high side and low side switches. Figure 4-5

(a)-(d) show the transition process in a PWM sector of a current source rectifier. D is the freewheeling diode between DC buses to realize zero vectors, in order to reduce conduction loss and avoid switching of active switches at the same time. In Figure 4-5(a), S6 turns off, S4 turns on, and S1 is ON. When zero vector is used, current commutates from S1 to D, as Figure 4-5(b) shows. Figure 4-5(c) and (d) show the reverse transition process of Figure 4-5(b) and (a).



(a) Current commutates from S6 to S4

(b) Current commutates from S1 to D

(c) Current commutates from D to S1

(d) Current commutates from S4 to S6

Figure 4-5. Equivalent circuit of the transition process in the current source rectifier.

To evaluate the power device switching performance, the DPT should keep the same transition process as current source converters. The DPT circuit based on current source structure is shown in Figure 4-6, which is different with the DPT circuit based on voltage source structure, shown in Figure 3-7. In this work, the tested SiC power devices will be used in a current source rectifier with 480 V_{rms} line-to-line input voltage, and 400 V_{dc} output voltage. In the first test, the MOSFET S2 is turned off and the double pulse signal, as Figure 3-8 shows, is added to the gate of S1, current commutates between S1 and D. *V1* increases from 340 V to 680 V. In the second test, a pulse is added to the gate of S2 too. The overlap time is 1 μs. *V1* increases from 588 V to 680 V, and *V2* decreases from 588 V to 340 V. Current commutates between S1 and S2.

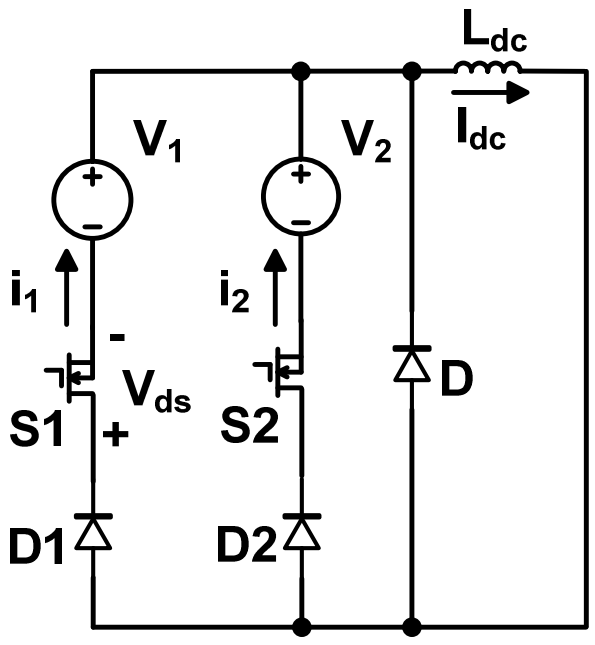


Figure 4-6. Current source double pulse test circuit.

The driver IC for the SiC MOSFET is IXDN514. The gate voltage of +20 V is selected for MOSFET turning on and -3 V is used for its turning off. The external gate resistance is 5 Ω. The passive probe, Tektronix P6139, is used to measure V_{gs}. The drain-source voltage (V_{ds}) is

measured by Tektronix high voltage probe P5100. The current probe, TCP0030 from Tektronix, is used to measure MOSFET drain current (I_{ds}).The load is a 1 mH inductor with 7 pF equivalent parallel capacitance (EPC). Figure 4-7shows the test setup.

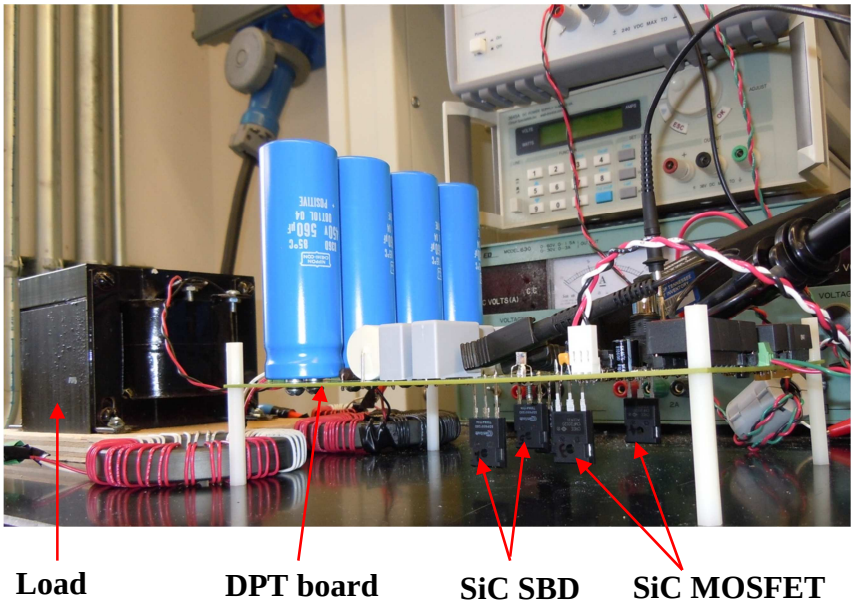
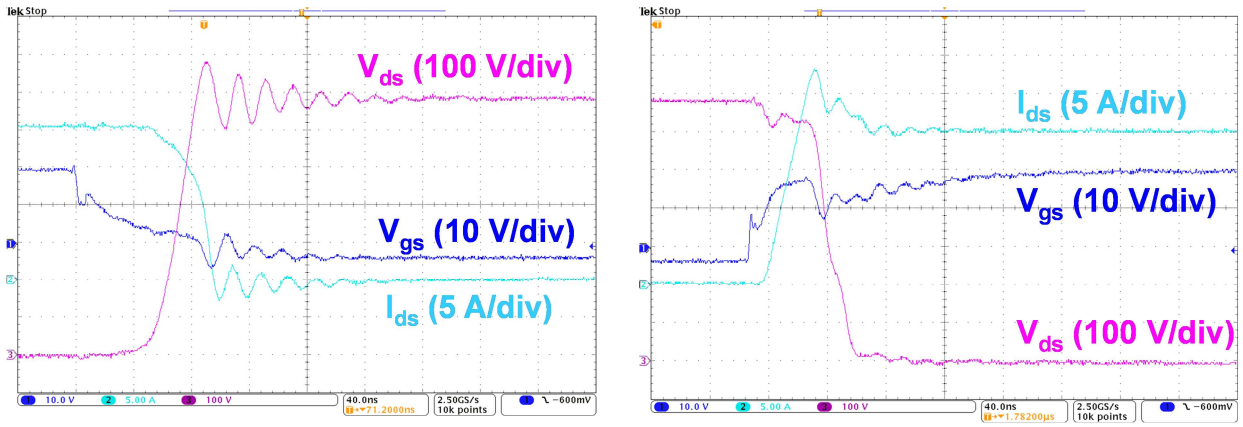


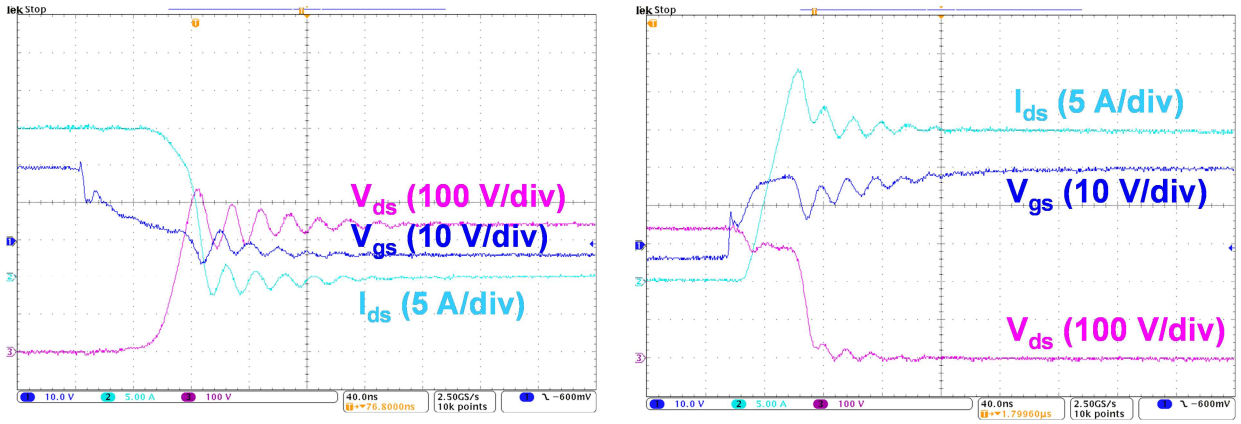
Figure 4-7. SiC MOSFET DPT setup based on current source structure.

Figure 4-8(a)-(b) are the MOSFET S1 turn-off and turn-on waveforms, respectively, when it commutates with freewheeling diode D. *V1* = 680 V, I_{dc} = 20 A, and the MOSFET S2 is turned off. The current fall time and rise time during turn-off and turn-on transient are 40 ns and 14 ns, respectively. The turn-off time is 40 ns and turn-on time is 55 ns.Figure 4-9(a)-(b) are S1 turn-off and turn-on waveforms at *V1* = 680 V, *V2* = 340 V, and I_{dc} = 20 A when it commutates with S2. The current fall time and rise time are 36 ns and 18 ns respectively. The turn-off time is 40 ns and turn-on time is 52 ns.



(a) Turn-off (b) Turn-on

Figure 4-8. MOSFET1 switching waveforms commutating with D. (Time: 40 ns/div)

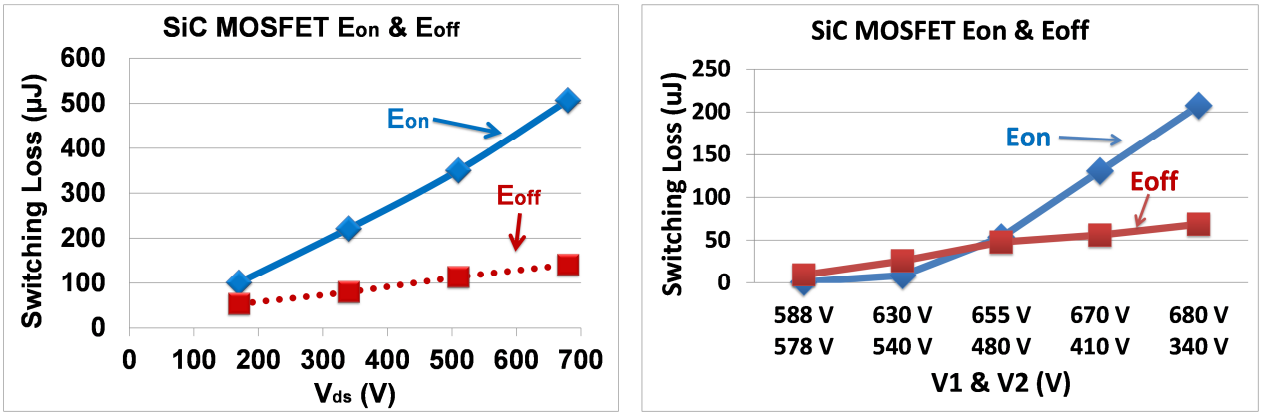


(a) Turn-off (b) Turn-on

Figure 4-9. MOSFET1 switching waveforms commutating with MOSFET2. (Time: 40 ns/div)

Based on the DPT above, the SiC MOSFET switching loss can be calculated, as Figure 4-10(a)-(b) show. Since the switching loss of the MOSFET will be used to estimate the power device loss of the current source converter, the values in Figure 4-10are obtained at different DC voltages and constant DC current I_{dc} of 20 A. The test results show the low switching loss of SiC MOSFET at the constant current value, compared with the traditional Si IGBT rated at 1200 V 30 A, IKW15N120H3 from Infineon [18], whose turn-off and turn-on loss are 0.45 mJ and 1.10

mJ at 600 V, 15 A, and 25 °C. Thus, the use of SiC MOSFETs will reduce the loss of power devices and increase the efficiency of current source converters.



(a) Commutation between S1 and D (b) Commutation between S1 and S2

Figure 4-10. SiC MOSFET switching loss as a function of DC voltages.

The measured switching energy (E_{on} + E_{off}) in the test is used to estimate the switching loss of the rectifier. During the device switching transient in current source converters, the junction capacitance of both power devices with and without switching actions are charged or discharged. The measured loss in the switching test includes the energy dissipation due to the charge/discharge of junction capacitance of devices involved in current commutations [126]. The effects generated by the remaining switch junction capacitance charge/discharge have also been included in the calculation of (E_{on} + E_{off}) from switching test results.

Figure 4-11shows the equivalent circuit during switching transients in three-phase current source rectifier. The switching elements Sx (MOSFET and diode in series) or D (freewheeling diode) involved in current commutation are modeled by a resistance, which represents devices' channels, and a capacitance, which blocks voltage during switch off state, in parallel. The remaining switching elements, which only have junction capacitance charge/discharge, are

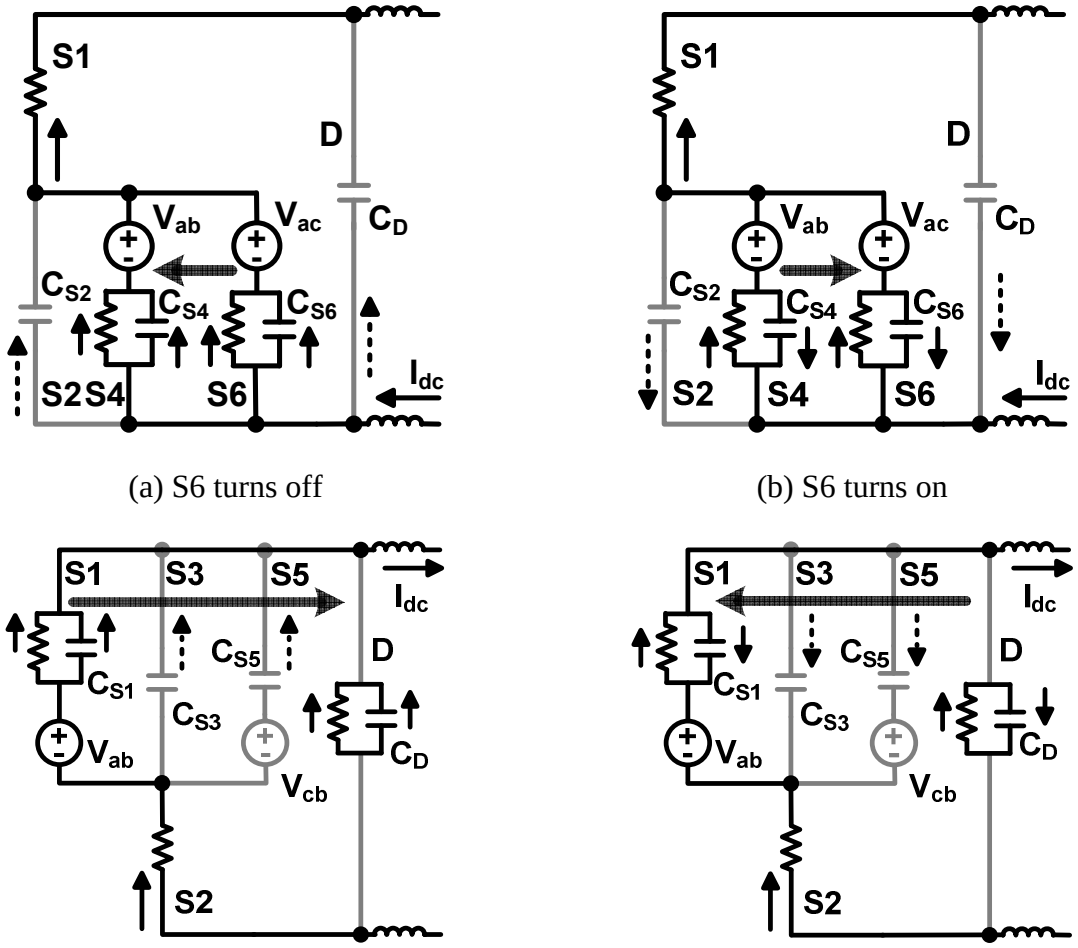
represented by a capacitance. A resistance is used for the conducted switching elements. Other switching elements are not shown in Figure 4-11. When current commutates between S4 and S6, the junction capacitance of freewheeling diode (C_D) and devices in S2 (C_{S2}), which are blocking voltages, are charged or discharged with ΔQ_D and ΔQ_{S2}. When S6 turns off (Figure 4-11(a)), C_D and C_{S2} are discharged. The discharge current reduces the turn-off current and loss of S6 considering the constant DC current. Meanwhile, the charge current of C_D and C_{S2} increases S6 turn-on current and loss (Figure 4-11(b)). Assume that E_{on} and $E_{off}$are switching energies of S6 obtained from the switching test without C_D and C_{S2} charge/discharge. The E'_{on} and E'_{off}, the S6 real switching energies with C_D and C_{S2} charge/discharge in converter operation, can be estimated as

$$\begin{aligned} E'_{off} &= E_{off} + \Delta E_{V_{ac}} + \Delta E_{C_{S2}} + \Delta E_{C_D} \\ &= E_{off} + V_{ac} \cdot [(V_{ab} - V_{ac}) \cdot C_{S2} + (V_{ab} - V_{ac}) \cdot C_D] \\ &+ \frac{1}{2} \cdot C_{S2} \cdot (V_{ab}^2 - V_{ac}^2) + \frac{1}{2} \cdot C_D \cdot (V_{ab}^2 - V_{ac}^2) \end{aligned} \tag{4-1}$$

$$\begin{aligned} E'_{on} &= E_{on} + \Delta E_{V_{ac}} + \Delta E_{C_{S2}} + \Delta E_{C_D} \\ &= E_{on} + V_{ac} \cdot [(V_{ac} - V_{ab}) \cdot C_{S2} + (V_{ac} - V_{ab}) \cdot C_D] \\ &+ \frac{1}{2} \cdot C_{S2} \cdot (V_{ac}^2 - V_{ab}^2) + \frac{1}{2} \cdot C_D \cdot (V_{ac}^2 - V_{ab}^2) \end{aligned} \tag{4-2}$$

From (4-1) and (4-2), ($E_{on} + E_{off}$) obtained from the switching test equals ($E'_{on} + E'_{off}$). Similarly, when current commutates between S1 and freewheeling diode D (Figure 4-11(c)-(d)), the same conclusion can be achieved according to (4-3) and (4-4), the switching energies of S1. For the symmetric PWM scheme used in the paper, the switching test results can be used to estimate device losses during current commutation transients in buck rectifier operation, considering junction capacitance charge/discharge of switching elements without switching actions. Here, the

loss in the charge/discharge loop resistance is neglected due to the short circuit loop of PCB layout. The influence of capacitance charge/discharge current on conduction loss of conducting devices is neglected too, considering the short switching transient compared with conduction interval and small on-state resistance of paralleled MOSFETs.



(a) S6 turns off (b) S6 turns on

(c) S1 turns off (d) S1 turns on

Figure 4-11. Equivalent circuit during switching transients in three-phase CSR.

$$\begin{aligned} E_{off}^{'} &= E_{off} + \Delta E_{V_{ab}} + \Delta E_{C_{S3}} + \Delta E_{C_{S5}} \\ &= E_{off} + V_{ab} \cdot [-V_{ab} \cdot C_{S3} + (V_{bc} - V_{ac}) \cdot C_{S5}] \\ &+ \frac{1}{2} \cdot C_{S3} \cdot (-V_{ab}^2) + \frac{1}{2} \cdot C_{S5} \cdot (V_{bc}^2 - V_{ac}^2) \end{aligned} \tag{4-3}$$

$$
\begin{aligned}
E_{on}^{'} &= E_{on} + \Delta E_{V_{ab}} + \Delta E_{C_{S3}} + \Delta E_{C_{S5}} \\
&= E_{on} + V_{ab} \cdot [V_{ab} \cdot C_{S3} + (V_{ac} - V_{bc}) \cdot C_{S5}] \\
&+ \frac{1}{2} \cdot C_{S3} \cdot V_{ab}^2 + \frac{1}{2} \cdot C_{S5} \cdot (V_{ac}^2 - V_{bc}^2)
\end{aligned} \tag{4-4}
$$

4.3 Parasitic Capacitance Influence on Switching Behavior

Parasitics play significant roles for power devices' and converters' performances. Section 3.4 has discussed the influence of parasitic capacitance in voltage source converters. In current source converters, the parasitic capacitance will influence the switching behaviors of power devices and the efficiency of the converter. Figure 4-12 shows the three-phase current source rectifier with parasitic capacitance between DC/AC buses, and how this influences converter performance is studied here. These parasitic capacitances include the junction capacitance of power devices, DC inductor equivalent parallel capacitance (EPC), and the capacitance between AC/DC buses on printed circuit boards (PCBs). Since the AC side of current source converter has AC capacitors, the parasitic capacitances between two AC buses could be considered as the AC side capacitors and are not included here.

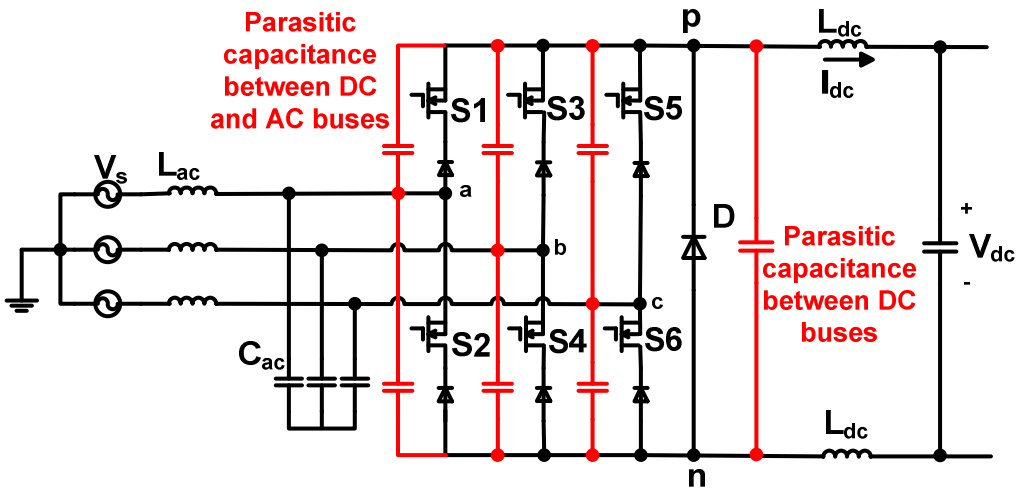


Figure 4-12. Three-phase current source rectifier with parasitic capacitance.

Figure 4-13 shows the DPT circuit based on current source circuit when a MOSFET commutates with freewheeling diode (D), with parasitic capacitance between +DC and –DC buses. Figure 4-14is the Saber simulation waveforms when the MOSFET turns on and D turns off.It is clear from Figure 4-14 that during D turns off, the parasitic capacitance is charged by +DC and the charge current I_C is added to the MOSFET current (I_{ds}), and causes the high spike of I_{ds} when a MOSFET turns on. The spike of I_{ds} increases the turn-on loss of the MOSFET. Figure 4-15 shows the DPT waveforms of a SiC MOSFET turning on at 680 V, 20 A, with 0.1 nF and 0.2 nF capacitance between DC buses. The DPT test has been described in Section 4.2. From Figure 4-15, the spike of I_{ds} increases from 28 A to 33 A, and the SiC MOSFET turn-on loss increases from 507 µJ to 636 µJ.

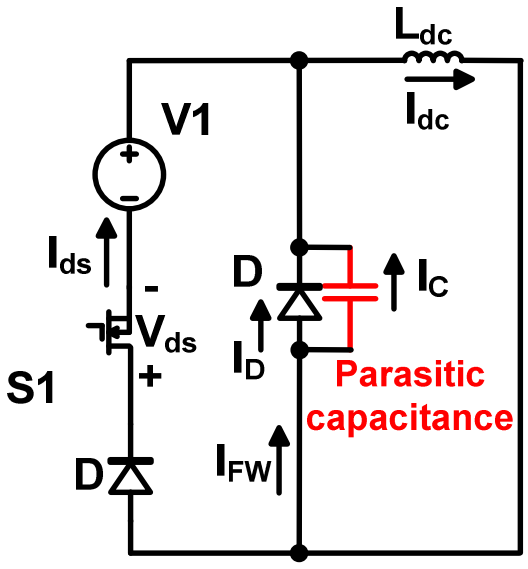


Figure 4-13. DPT circuit with parasitic capacitance between DC buses.

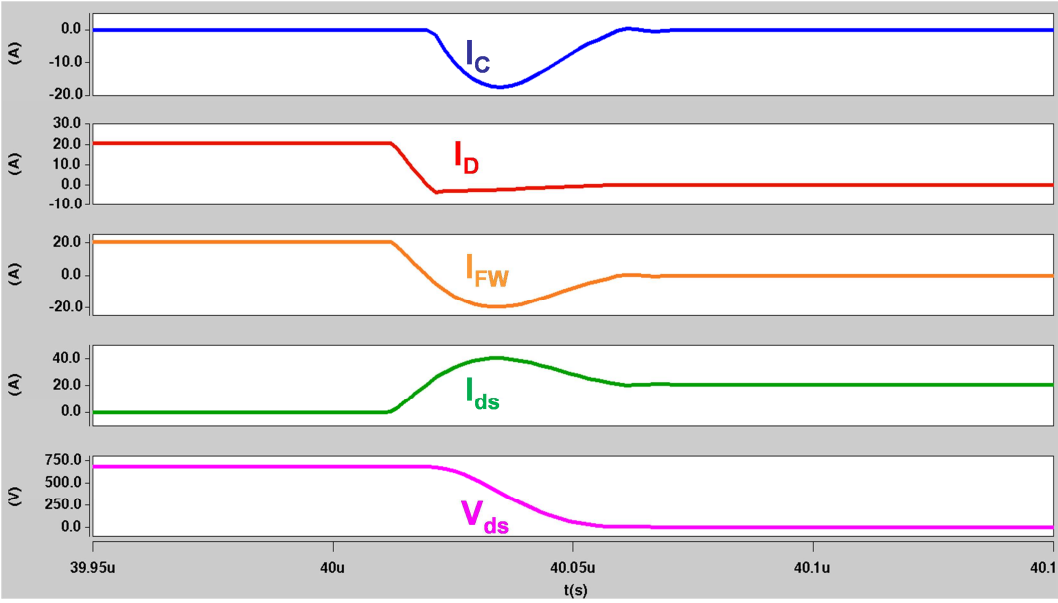


Figure 4-14. Simulation waveforms during MOSFET turn-on transient.

Figure 4-16 shows the DPT circuit based on current source circuit when two MOSFETs commutate, with parasitic capacitance between AC and DC buses. Figure 4-17 shows the S1 turn-on simulation waveforms in Saber at *V1* = 680 V, *V2* = 340 V, and I_{dc} = 20 A, with 0.6 nF and without parasitic capacitance. The I_{ds} spike of MOSFET1 is 24 A and 37 A, without and with 0.6 nF capacitance between AC and DC buses, respectively. The MOSFET S1 turn-on loss increases from 130 µJ to 214 µJ.

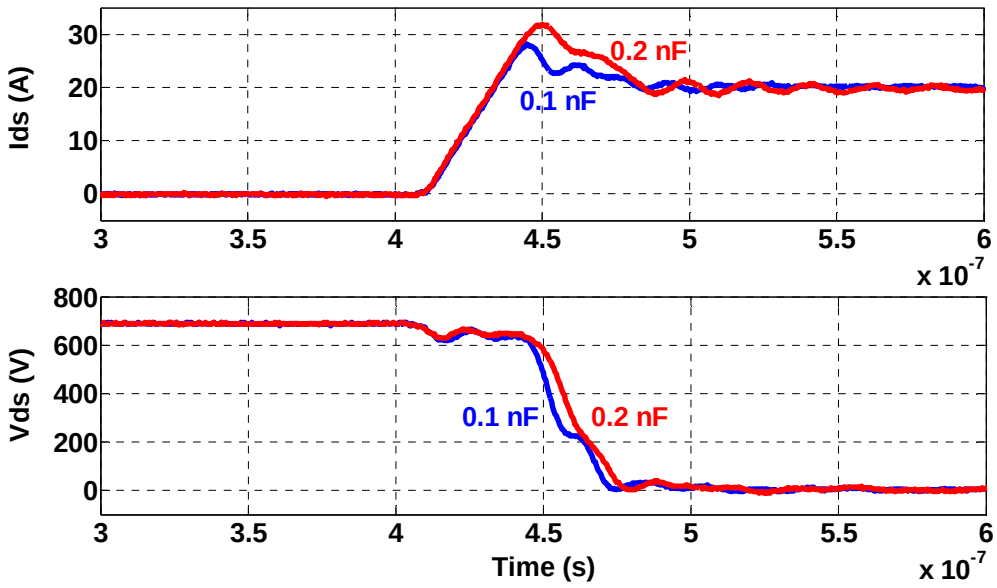


Figure 4-15. MOSFET turn-on waveforms in DPT with different parasitic capacitance.

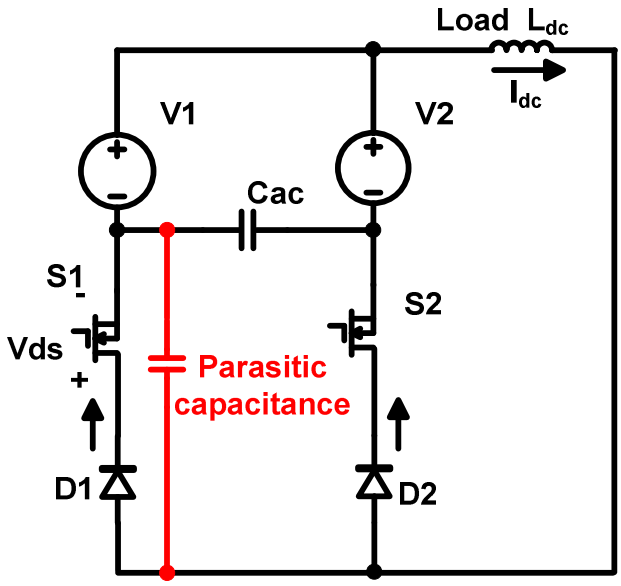


Figure 4-16. DPT circuit with parasitic capacitance between AC and DC buses.

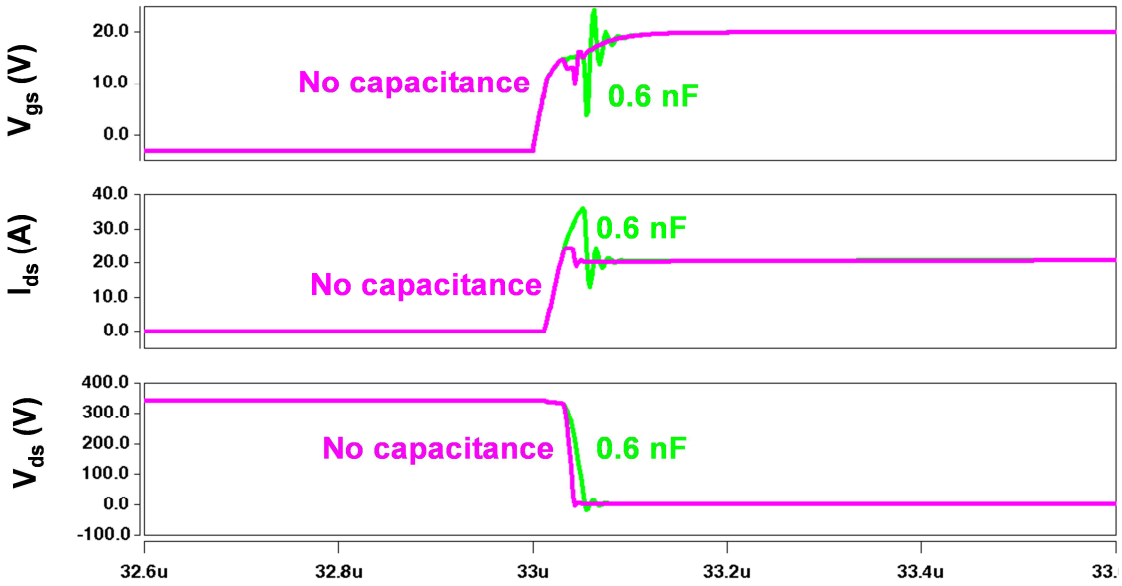


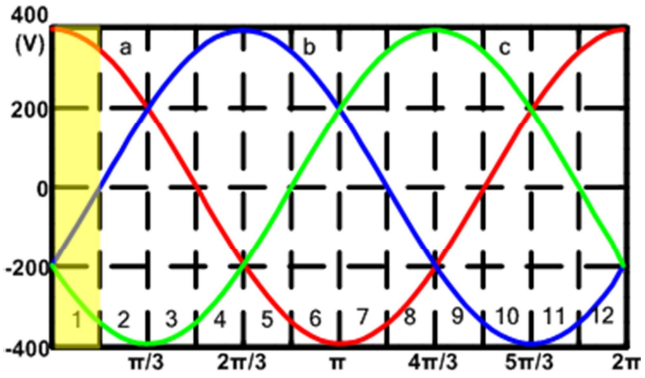
Figure 4-17. MOSFET turn-on waveforms in simulation without and with parasitic capacitance.

From the discussion above, the existence of parasitic capacitance in a current source converter increases the device switching loss and reduces the converter efficiency. Figure 4-18 analyzes the parasitic capacitance performance during commutation transient in a current source rectifier (CSR) with a freewheeling diode. Take the commutation in sector 1 of space vector modulation as an example. In this sector, the input AC phase voltages satisfy V_a> 0 >V_b>V_c,asFigure 4-18(a) shows. In this sector, according to the switching loss optimized (SLO) modulation which will be introduced in Chapter 5, the switch S1 commutates with D and S4 commutates with S6.

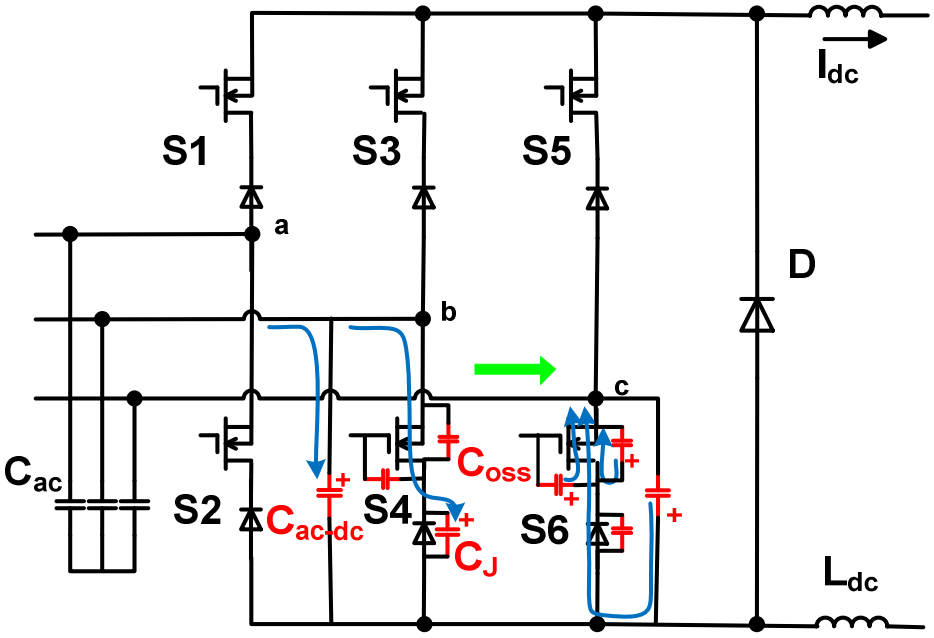
Figure 4-18(b) and (c) show the transient of S4, S6 commutation. At this time, S1 is ON and D is OFF. Since V_b>V_c, S4 turns on/off at negative voltage and S6 turns on/off at positive voltage. During S6 off, the output capacitance (C_{oss} = C_{ds} + C_{gd}) of MOSFET in S6 and the parasitic capacitance ($C_{ac\text{-}dc}$) between –DC and phase C buses are charged by V_{bc}. When S6 turns on, these capacitances discharge and the discharging current flows through the MOSFET and series diode,

causing additional loss on power devices. When S4 turns off, the junction capacitance (C_J) of the diode in S4 is charged by V_{bc} and the charging current flows through the MOSFET channel causing power loss. At the same time, $C_{ac\text{-}dc}$ between –DC and phase B buses is charged too. Figure 4-18(b) shows the process discussed above. In Figure 4-18(c), the current commutates back from S4 to S6. During this transient, S4 turns off and C_J discharges through the MOSFET. In addition, $C_{ac\text{-}dc}$between –DC and phase B buses is discharged too. Meanwhile C_{oss} of MOSFET in S6 and $C_{ac\text{-}dc}$between –DC and phase C buses are charged by V_{bc} because S6 turns off. The charging current of C_{oss} flows through the series diode and cause power loss.

Figure 4-18. Parasitic capacitance performance during commutation transient.

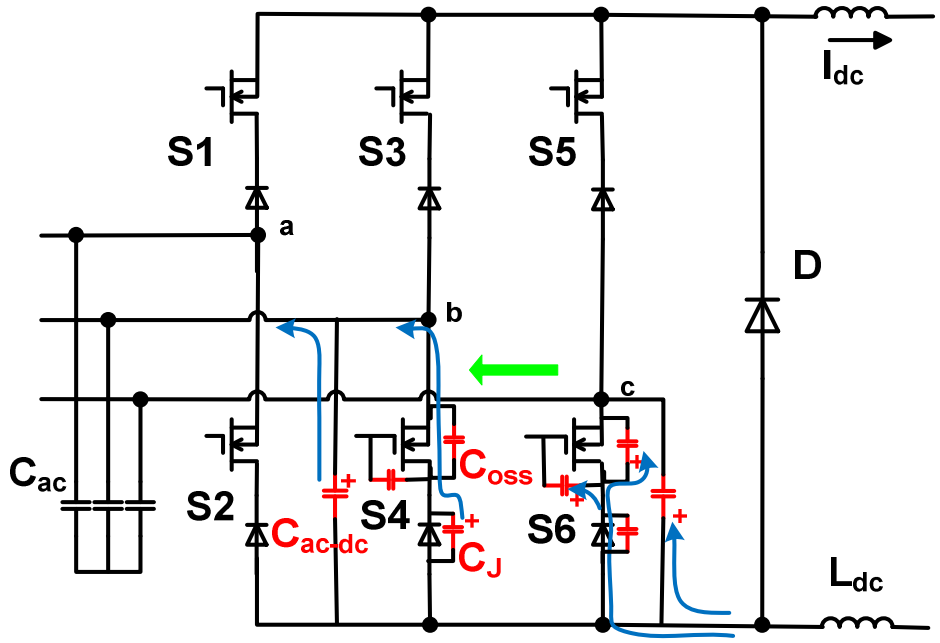


(a) AC voltage waveforms with 12 sectors of space vector modulation

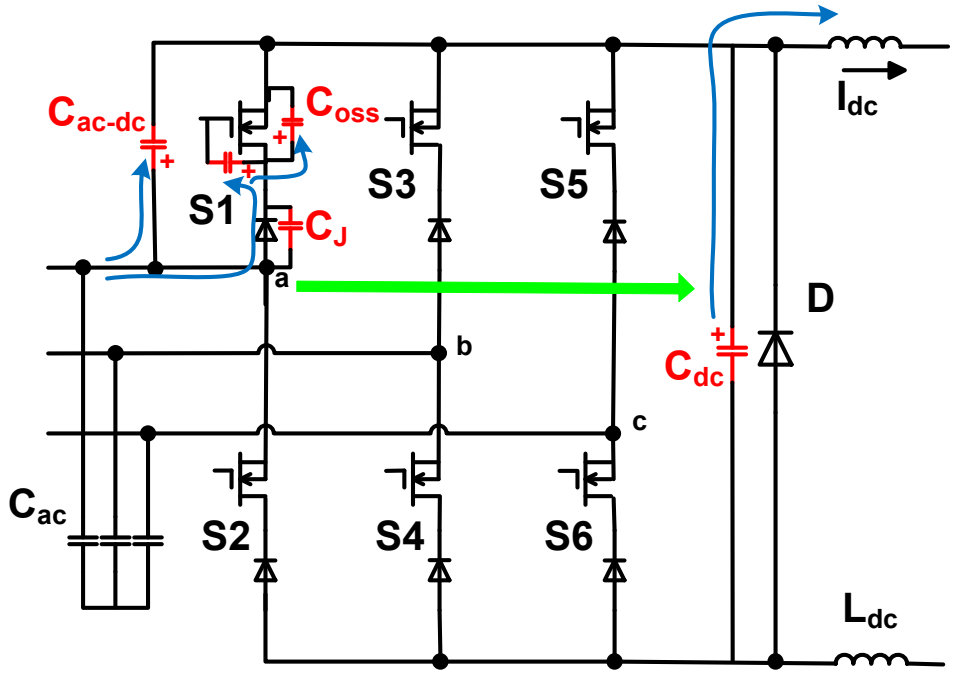


(b) Current commutates from S4 to S6

Figure 4-18 continued.

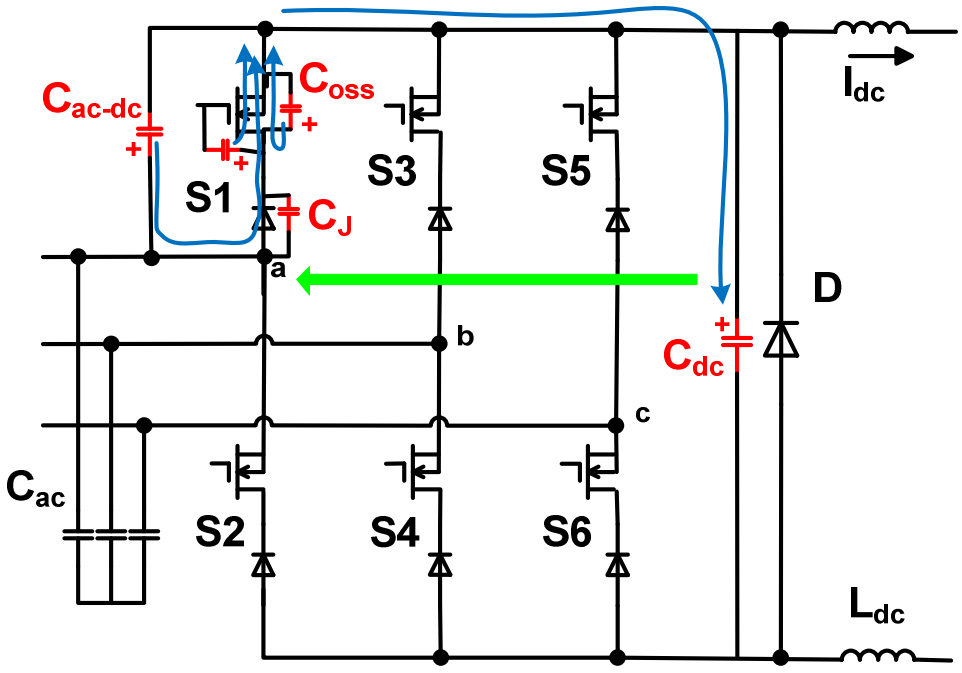


(c) Current commutates from S6 to S4



(d) Current commutates from S1 to D

Figure 4-18 continued.



(e) Current commutates from D to S1

Figure 4-18 continued.

Figure 4-18(d) and (e) show the transient of S1, D commutation. At this time, S4 is ON and S6 is OFF. S1 turns on/off at positive voltage. From Figure 4-18(d), S1 turns off the C_{oss} of MOSFET in S1 and $C_{ac\text{-}dc}$between +DC and phase A buses is charged. The charging current of C_{oss} flows through the series diode. During this transient, the parasitic capacitance between DC buses (C_{dc}) which includes the junction capacitance of D and other parasitic capacitances discharges. When the current commutates from D to S1, the discharging current of C_{oss} of MOSFET in S1 and $C_{ac\text{-}dc}$between +DC and phase A buses, and the charging current of C_{dc} flow though the power devices in S1 which will cause additional power loss and reduce the efficiency of the converter, as Figure 4-18(e) shows.

Table 4-1 show the parasitic capacitances in current source converters based on the analysis above. The capacitances, including power devices junction capacitances and parasitic capacitance between AC/DC buses, which will play an important role on power devices' switching performance at different commutation transients are summarized.

Table 4-1. Parasitic capacitances impacting power devices switching in current source converter

Current commutates between two phases		
	Turn-on	Turn-off
Switching at positive voltage	C_{oss}, $C_{ac\text{-}dc}$	C_{oss}
Switching at negative voltage	C_J	C_J
Current commutates between one phase and freewheeling diode		
	Turn-on	Turn-off
Switching at positive voltage	C_{oss}, $C_{ac\text{-}dc}$, C_{dc}	C_{oss}

Even though the devices do not switch, the parasitic capacitances are still charged or

discharged during other devices switching, due to the variation of the voltage across them. From [58], the energy loss of the capacitance (C) due to charging is

$$\Delta E_{cap} = \frac{1}{2} C (V_2 - V_1) \tag{4-5}$$

whereV_1 and V_2 are voltages across the capacitance before and after the charging. The total capacitive energy loss in sector 1 in Figure 4-17(a) is given in reference [58], only considering the parasitic capacitances of power devices

$$\begin{aligned} E_{\sec 1} &= \frac{1}{2} C_{oss1} V_{ab}^2 + \frac{1}{2} C_{oss6} V_{bc}^2 + \frac{1}{2} C_{JD} V_{ab}^2 + \frac{1}{2} C_{J4} V_{bc}^2 \\ &+ \frac{1}{2} C_{JD} V_{bc}^2 + \frac{1}{2} C_{J2} V_{bc}^2 + \frac{1}{2} C_{J3} V_{ab}^2 + \frac{1}{2} C_{J5} V_{ab}^2 \end{aligned} \tag{4-6}$$

Integrating the total losses over sector 1 gives the power loss due to the parasitic output capacitances of devices in sector 1. Since all 12 sectors are symmetric in terms of switching behavior and voltages, the total power loss will be

$$P_{cap} \approx \frac{6\sqrt{2}}{\pi} V_N^2 \left(\frac{1}{2} n_S C_{oss} + \frac{3}{2} n_D C_J \right) \left(\frac{14\pi - 9\sqrt{3}}{32} \right) f_{sw} \tag{4-7}$$

whereV_N is the rms value of the input phase voltage, f_{SW} is the switching frequency, n_S and n_D are MOSFET and diode paralleling number, respectively. If the parasitic capacitance between AC and DC buses is considered, the equation (4-7) will be

$$P_{cap} \approx \frac{6\sqrt{2}}{\pi} V_N^2 \left(\frac{1}{2} n_S C_{oss} + \frac{3}{2} n_D C_J + \frac{3}{2} C_{ac-dc} + \frac{1}{2} C_{dc} \right) \left(\frac{14\pi - 9\sqrt{3}}{32} \right) f_{sw} \tag{4-8}$$

Both (4-3) and (4-4) are approximation since the parasitic capacitance of the power device is not constant. The accuracy energy must be determined by integrating the nonlinear capacitance.

However, the parasitic capacitances between AC and DC buses which mainly come from the PCB could be considered as constant values. So the power loss due to the charging of these capacitances could be estimated accurately in (4-9)

$$P_{cap} = \frac{6\sqrt{2}}{\pi} V_N^2 \left(\frac{3}{2} C_{ac-dc} + \frac{1}{2} C_{dc} \right) \left(\frac{14\pi - 9\sqrt{3}}{32} \right) f_{sw} \tag{4-9}$$

4.4 An Inductive Snubber in a Current Source Rectifiers

The impacts of parasitic capacitance on devices' switching losses in current source rectifiers are studied in 4.3. In this section, an inductive snubber circuit will be developed. It reduces the impact of parasitic capacitance across the DC link, and reduces the switching loss in current source rectifiers.

Many studies on snubber circuits have been done. Reference [127] introduces a snubber circuit with a single capacitor and a single inductor. Capacitive snubber circuits are proposed in [128] and [129] to implement a resonant circuit with parasitic inductance in the circuit, in order to realize soft switching. References [69], [130], and [131] propose the inductive resonant snubbers using active switches which increase the control complexity. The inductive snubber circuit without active switches, dealing with the circuit parasitic capacitance in current source converters to reduce power devices' switching losses, has not been developed.

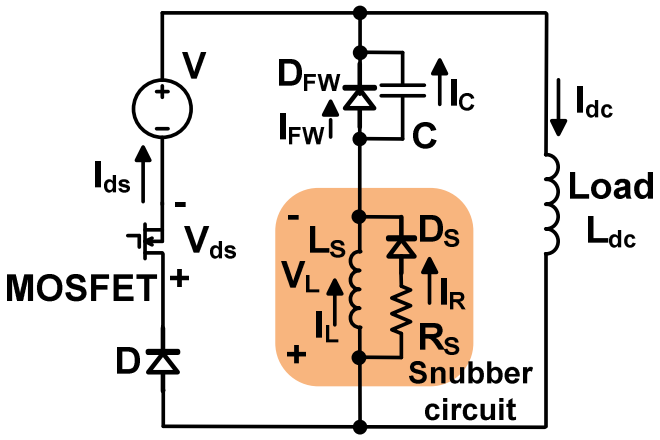
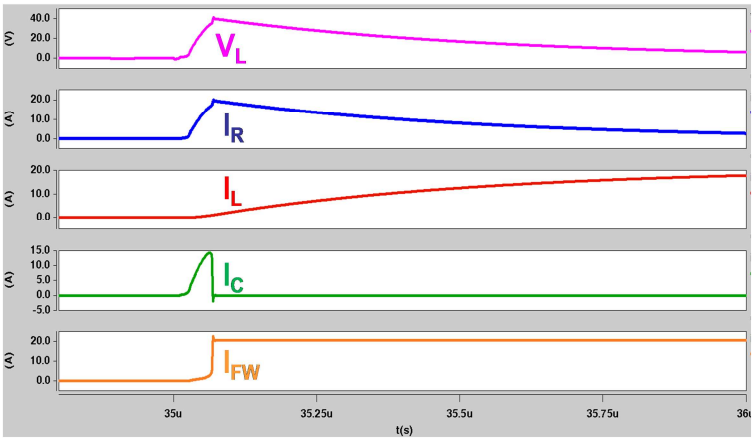
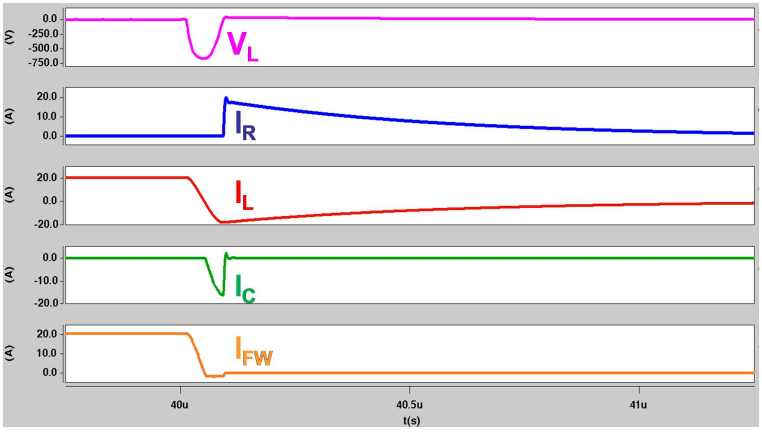


Figure 4-19. Inductive snubber in double pulse circuit.



(a) MOSFET turn-off, D_{FW} turn-on transient



(b) MOSFET turn-on, D_{FW} turn-off transient

Figure 4-20. Snubber operation waveforms.

The inductive snubber is developed to reduce the influence of parasitic capacitance (C), across the DC link, on MOSFET switching loss during commutation with a freewheeling diode (D_{FW}).Figure 4-19shows the snubber in the double pulse test(DPT) circuit based on current source topology.The inductor (L_S) is connected in series with D_{FW}, and paralleled with a path that consists of a diode (D_S) and a resistance (R_S) in series.

DuringMOSFET turning off and D_{FW} turning on transient, the load current (I_{dc}) commutates from the MOSFET loop to the freewheeling loop. The C is discharged by I_{dc} through the freewheeling loop. The current through D_S and R_S (I_R) increases fast todischarge$C$.The inductor current (I_L) increases and I_{dc} commutates from the D_S-R_S loop to the L_S loop gradually. Since the I_{dc} decreses during the freewheeling state,the voltage across the L_S (V_L) will be a negative value and the D_S will be reverse blocked after discharging of C. As a result, I_R can be neglected during steady state of freewheeling state. The simulated waveforms of this transient are shown in Figure 4-20(a).When the MOSFET turns on and the D_{FW} turns off, the $C$is charged through L_S because D_S is reversed blocked.The existence of L_S reduces the charging speed of C. It slows the increase of MOSFET drain current(I_{ds}) and delays the current overshoot during MOSFET turning on.After charging of C, L_S continues to discharge through D_S and R_S until I_L is 0. The simulated waveforms are shown in Figure 4-20(b). The V_L helps to speed up the decrease of the MOSFET voltage (V_{ds}) during MOSFET turning on. Thus, the overlap area of I_{ds} and V_{ds} is small and the MOSFET turn-on loss is reduced, shown in Figure 4-21.

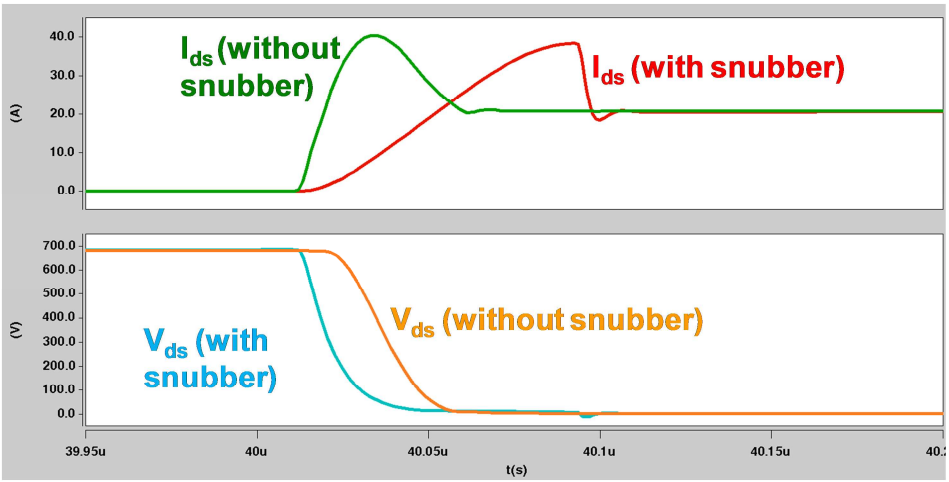


Figure 4-21. Comparison of MOSFET turn-on simulation waveforms with and without snubber.

The test of the snubber is conducted based on the DPT circuit in Figure 4-19. The power MOSFET and diodes (D and D_{FW}) used in the test are the same with DPT in 4.2. The parasitic capacitance is 0.6 nF, mainly from the junction capacitance of two paralleled freewheeling diodes. The I_{dc} is constant of 20 A in the test. The snubber parameters are L_S = 735nH, R_S = 3 Ω, and D_S is 1200 V SiC diode, C4D20120A, from Cree. The setup of DPT with snubber is shown in Figure 4-22. Figure 4-23(a) and (b) show the MOSFET turn-on waveforms without and with the snubber respectively, at V = 680 V. From Figure 4-23, the overlap area of I_{ds} and V_{ds} reduces after using the snubber. The ringing in Figure 4-23 comes from the MOSFET internal capacitance and the parasitic inductance in its loop.

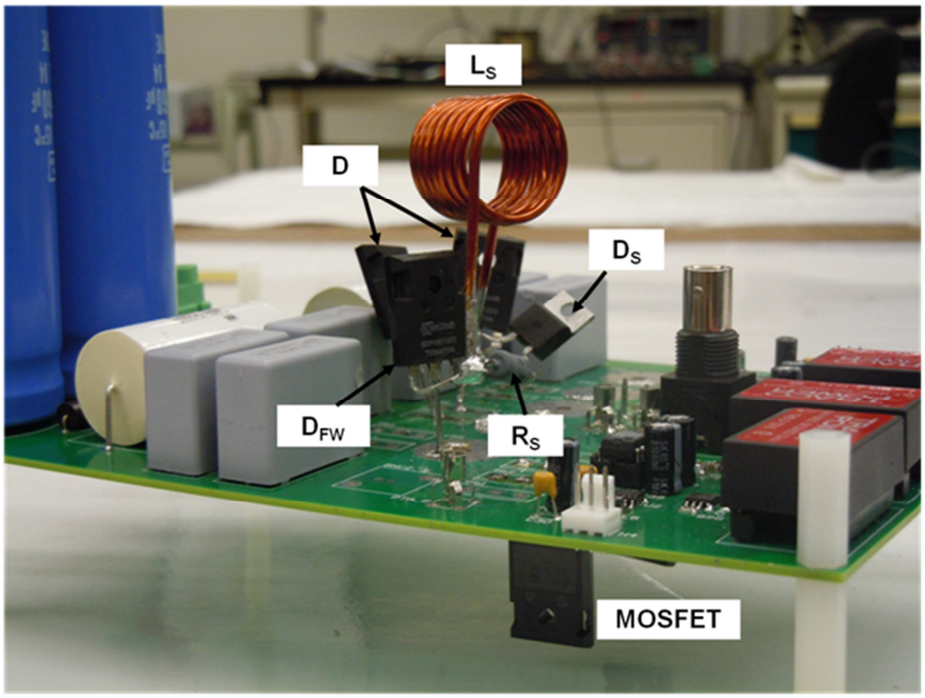
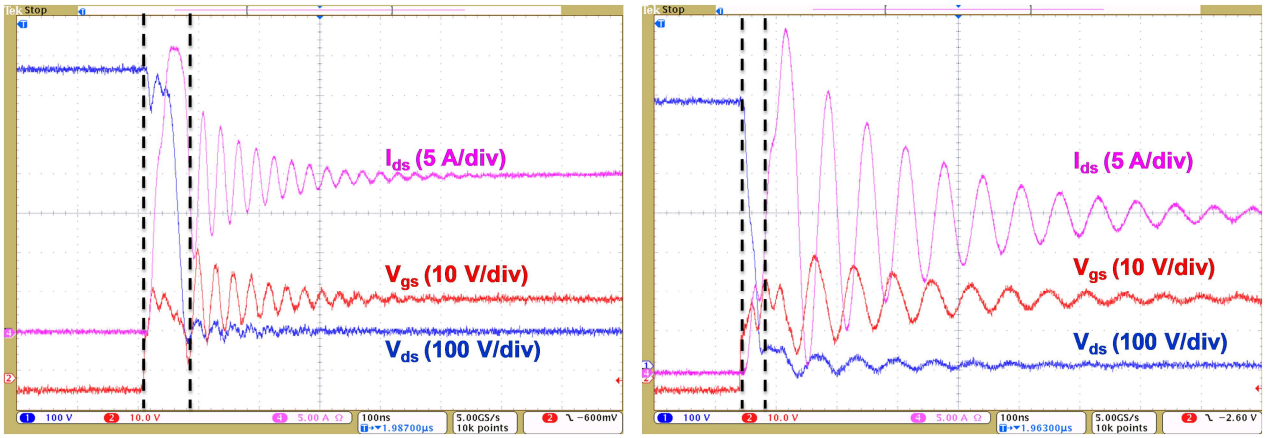


Figure 4-22. Setup of DPT with snubber.

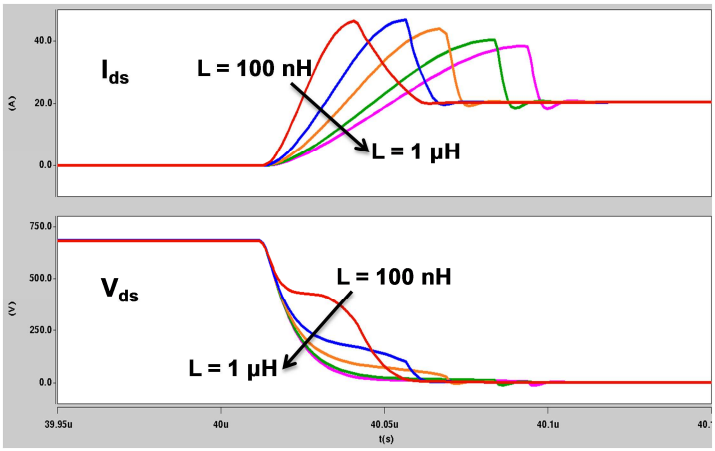


(a) Without snubber (b) With snubber

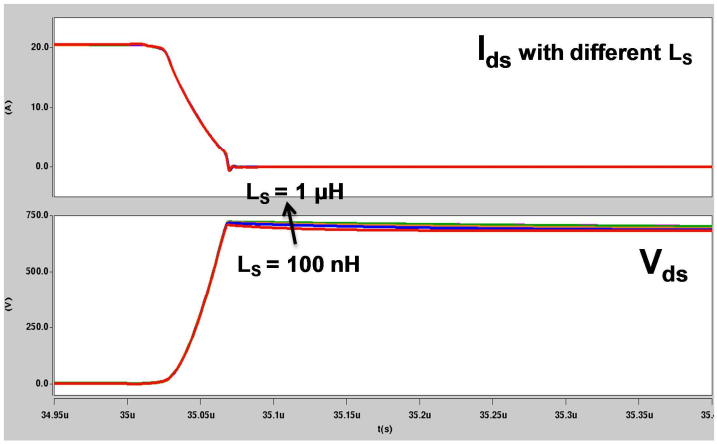
Figure 4-23. Comparison of MOSFET turn-on test waveforms with and without snubber. (Time: 100 ns/div)

Figure 4-24(a) and (b) show the simulation waveforms of MOSFET turn-on and turn-off, with the constant parasitic capacitance C = 0.6nF, resistor R_S = 2 Ω, and various inductor L_S

values of 100 nH, 300 nH, 500 nH, 800 nH, and 1 µH. The voltage V is 680 V and I_{dc} is 20 A. From Figure 4-24(a), with L_S increasing, V_{ds} decreases faster, I_{ds} increases slower and the peak of it becomes smaller. The overlap area of I_{ds} and V_{ds} is small with large L_S, resulting in small MOSFET turn-on loss. However, large $L_S$leads to large snubber loss, and the spike of V_{ds} increases slightly due to the voltage V_L, as Figure 4-24(b) shows.



(a) MOSFET turn-on waveforms with different L_S in snubber



(b) MOSFET turn-off waveforms with different L_S in snubber

Figure 4-24. Simulated MOSFET switching waveforms with different LS in snubber.

Different values of L_S are used in DPT in Figure 4-22. Because of the small inductance value

of L_S, the air core inductor can be used, shown in Figure 4-25, the inductance value of each inductor is measured by an impedence analyzer. The loss on the snubber can be estimated by $P_S = \frac{1}{2} L_S I_{dc}^2$, which is stored in L_S and lost in R_S during L_S discharging.

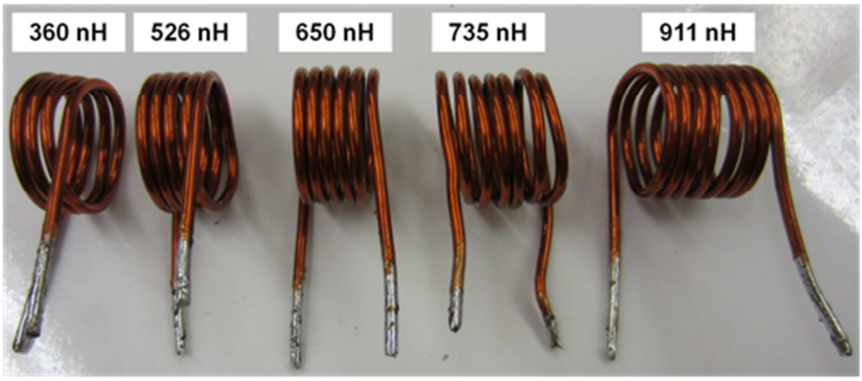
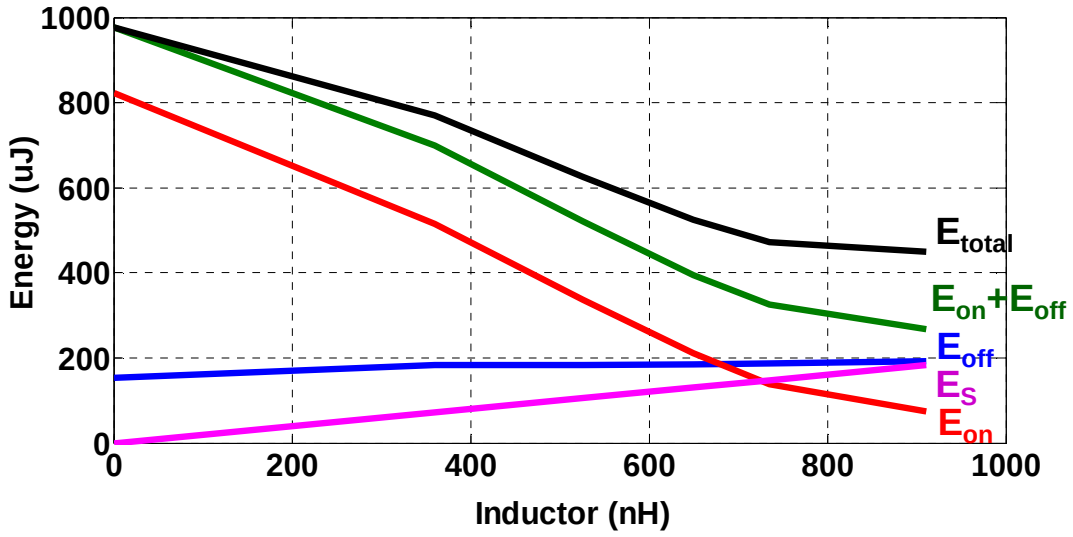
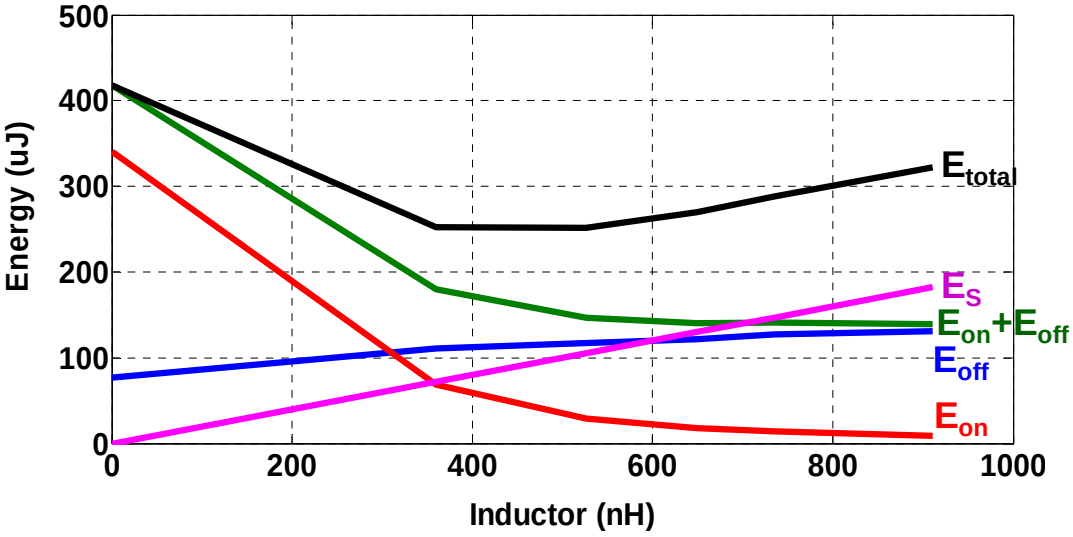


Figure 4-25.L_S in snubber.

The MOSFET switching energy (E_{on}+ E_{off}), snubber loss (E_S), and total loss from DPT results, when using different L_S values with V = 680 V, R_S = 3 Ω, I_{dc} = 20 A, are shown in Figure 4-26(a). From Figure 4-26(a), total loss (E_{total} = E_{on}+ E_{off}+E_S) reduces with the increasing of L_S value at V = 680 V. From Figure 4-26(b), there is an optimized value of L_S to minimize the total loss at V = 340 V. Figure 4-27 shows the total loss of the MOSFET and snubber at different voltage levels with different L_S values. At different voltage levels with constant I_{dc} during current source converter operation, the optimized L_S values will be different to minimize the total loss. So the selection of L_S in the snubber will depend on the voltage range of converter operation, DC current values, and the parasitic capacitance in the circuit.



(a) V = 680V



(b) V = 340 V

Figure 4-26. Energies of snubber and MOSFET with different L_S values.

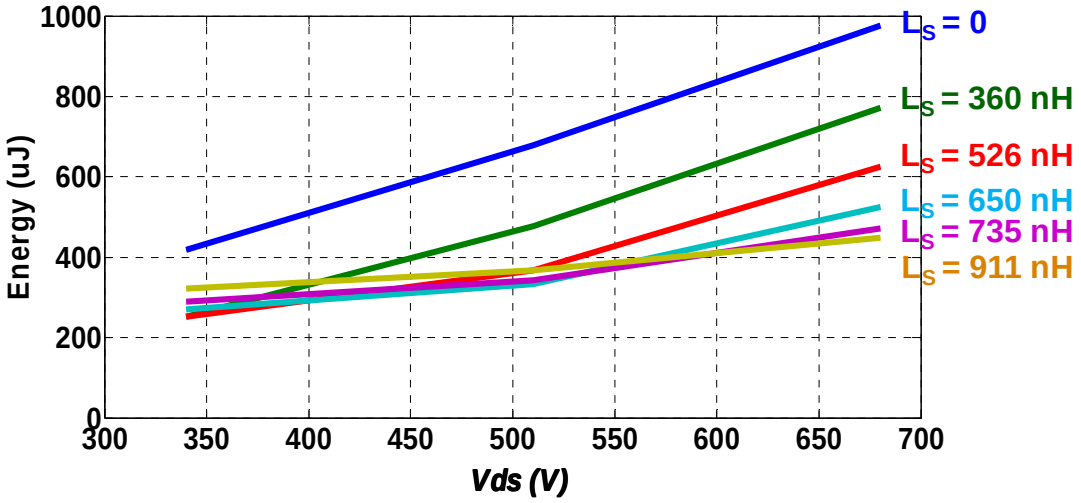


Figure 4-27. Total energy of MOSFET and snubber with different L_S at different voltage levels.

4.5 Summary

In this chapter, the performance of the commercial SiC MOSFET, CMF20120D from Cree, and SiC SBD, SDP60S120D from SemiSouth, in current source converters are studied. The static tests at various temperatures show the low on-state resistance. The low on-state resistance means low conduction loss of power devices, which is the dominant part of power losses in the current source converters. In addition, the DPT circuit based on the current source circuit is developed to evaluate the switching performances of these devices, considering current commutation process in a current source rectifier. The faster switching speed and lower switching loss of a SiC MOSFET are verified, compared with traditional Si power semiconductors. Finally, the effects of parasitic capacitance on the device switching performance and converter loss in current source converters is studied, based on the simulation and experimental results of a DPT. Furthermore, the parasitic capacitances' behavior in the current source rectifier operation and their influence on the converter efficiency are analyzed. The analysis results show that the parasitic capacitance will bring additional loss for power devices and reduce the efficiency of current source

converters. An inductive snubber connected in series with the freewheeling diode in a current source rectifier is developed. The snubber reduces the active switch turn-on loss by slowing current rise speed and decreasing voltage fall time. The performance of the snubber is proved by both simulation and experiments. In simulation, the characteristics of the snubber are studied with different parameters, and the optimized snubber shows the better performance.

Chapter 5 Front-End Rectifier for High Efficiency Data Center Power Supplies

The energy consumption of telecommunications buildings and data centers has been rapidly increasing due to the widespread use of information and communication technology equipment.Therefore, reduction in electricity consumption in the telecommunication and information industry is an important issue.In recent studies, the 400 V_{dc} distribution architecture in telecommunication and data centers has been presented to have superior efficiency and reliability, compared with the traditional AC architecture and 48 V_{dc} architecture[6], [132].

In this chapter, a high efficiency three-phase current source rectifier, based on SiC MOSFET and SBD, for 400 V_{dc} architecture data center power supply system, is designed, fabricated and tested. In 5.1, the 400 V_{dc} power distribution architecture for data centers and telecommunications buildings is introduced and compared with traditional architectures. In 5.2, two front-end rectifier topologies are compared and the three-phase current source rectifier is selected. The all-SiC three-phase current source rectifier is designed in 5.3, including devices paralleling, modulation scheme, filter design and loss calculation. Two converter prototypes are implemented and tested, in 5.4 and 5.5 respectively. Finally, conclusions are given in 5.6.

5.1 Introduction of DC Architecture Data Center Power Supplies

Data and telecommunication centers are major energy consumers, with energy consumption estimated at 40 TWh in 2005 in the United States alone, and 120 TWh worldwide [10]. A very large data center requires on the order of 10 MW of power to support the computing infrastructure and this is expected to increase to 50MW in the future [6].In a typical data center,

less than half of this power is delivered to the computing load, which includes microprocessors, memory and disk drives. The rest of the power is lost in power conversion, distribution, and cooling [6].

In the United States, the medium voltage (MV) from the utility is stepped down to 480 V_{ac} at the building entrance. Typically a double conversion Uninterruptible Power Supply (UPS) is used which supplies power to a Power Distribution Unit (PDU) where the voltage is stepped down to 208 V_{ac}. This step-down is required because the Power Supply Units (PSUs) in the servers can accept a universal input range of 90 – 264 V_{ac} and the line-to-neutral voltage in a 480 V_{ac} distribution system is 277 V_{ac}, which exceeds the input range of the PSU.

This conventional power delivery architecture is burdened with many conversion stages, shown inFigure 5-1. Inside of the double conversion UPS, the AC input is converted to a DC voltage at which point it is connected to an energy storage system, typically a battery, and then it is inverted to AC. An isolation transformer is usually included at the input or output of the UPS. Within the PSU, the AC input is converted to a DC voltage ranging from 380 V to 410 V. This DC voltage is stepped down with an isolated DC-DC converter to a low voltage, typically 12 V_{dc} or 48 V_{dc} (12V is assumed in this chapter). Some loads, such as hard drives, can accept 12 V directly while others, such as microprocessors and memory, need voltage regulators (VRs) to step the voltage down further. Server fans also run directly off 12 V.

DC distribution offers higher efficiency by eliminating the inverter (DC/AC conversion stage) in the UPS, the AC/DC converter in the PSU, as well as the transformer in the PDU. DC distribution at 48 V_{dc}, as shown inFigure 5-2, iscommon in telecommunication facilities. While it provides high efficiency,its applicability to large data and telecommunication centers is limited by thehigh currents when distributing power exceeding1MW at such a low voltage. The amount

of copper required to limit cable losses to a specified level increases with decreasing voltage, and is in theory inversely proportional to the square of the distribution voltage [6].

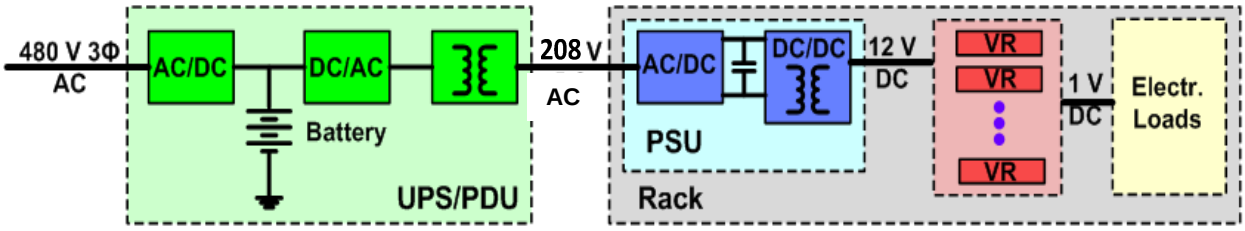


Figure 5-1. 480 V_{ac}distribution in the United States.

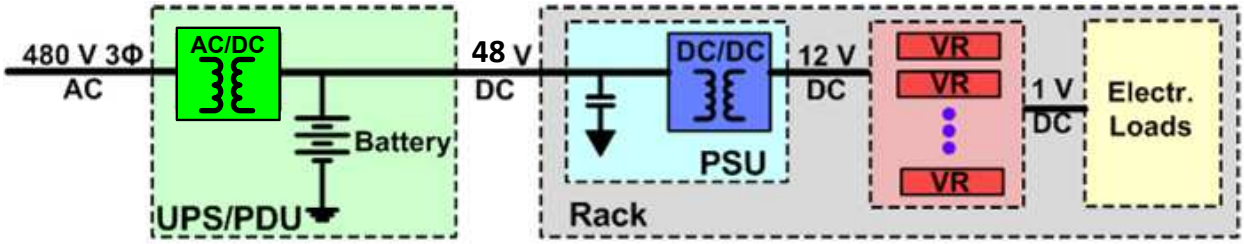


Figure 5-2. 48 V_{dc}distribution.

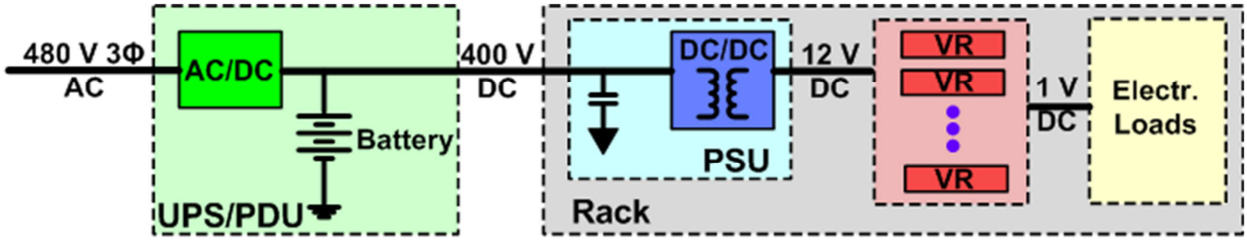


Figure 5-3. 400 V_{dc}distribution.

Currently the DC distribution directly to the PSU is limited to 48 V_{dc} as servers are only manufactured with a universal AC input range or 48 V_{dc} input. Since an AC PSU contains a DC bus voltage in the range of 400 V_{dc}, it can be seen that with simple modifications to the PSU, a ~400 V_{dc} compatible input PSU may be developed, as shown inFigure 5-3. Voltage levels

ranging from 300 V_{dc} to 400 V_{dc} have been proposed in [133]-[135]. Distribution at these higher voltages results in a slightly higher efficiency than the 48 V_{dc}distribution, since the UPS does not have to be isolated.Table 5-1compares the efficiency of each conversion stage in different architectures, using the power delivery efficiency model[6].

Table 5-1.Calculated efficiency comparison at full load

	480 V_{ac} distribution	**48 V_{dc} distribution**	**400 V_{dc} distribution**
UPS	94.00	92.86	95.32
PDU	94.03	96.11	96.78
PSU	87.56	91.54	89.05
VR	87.69	87.69	87.69
Total	**67.97**	**71.85**	**72.70**

The efficiency of each conversion stage in data center power supply system is expected to be increased in order to improve the efficiency of the whole system. Recently, Delta Electronics developed a three-phase rectifier for high voltage DC distribution of data center power supplies[136]-[137]. The AC-DC converter efficiency of 97% is achieved. In this chapter, the first stage in a 400 V_{dc} distribution system, a front-end rectifier, is designed and tested. SiC power devices are used to reduce the power semiconductors' losses.

5.2 Front-End Rectifier Topologies

In this section, two different topologies of 15 kW three-phase rectifier are designed.The goal ofdesign is high efficiency. For each topology, the losses of both Siand SiCbased converters are calculated.Table 5-2lists design specifications.

Table 5-2. Specifications of 15 kW three-phase rectifier

Power rating	15 kW
Input voltage	Three-phase 480 V_{ac}
Input range	± 10%
Output voltage	400 Vdc
Input power factor	> 0.99
Current total harmonic distortion	< 5%
Operating temperature	50 ºC

5.2.1 Two-Stage Rectifier

The topology of the three-phase rectifier consists of three single-phase converters. For each phase, there is a two-stage rectifier, as Figure 5-4shows. The first stage is a diode bridge.According to the requirements of input and output voltages, the second stage is a DC-DC converter.Both Si and SiC based rectifiers were designed.

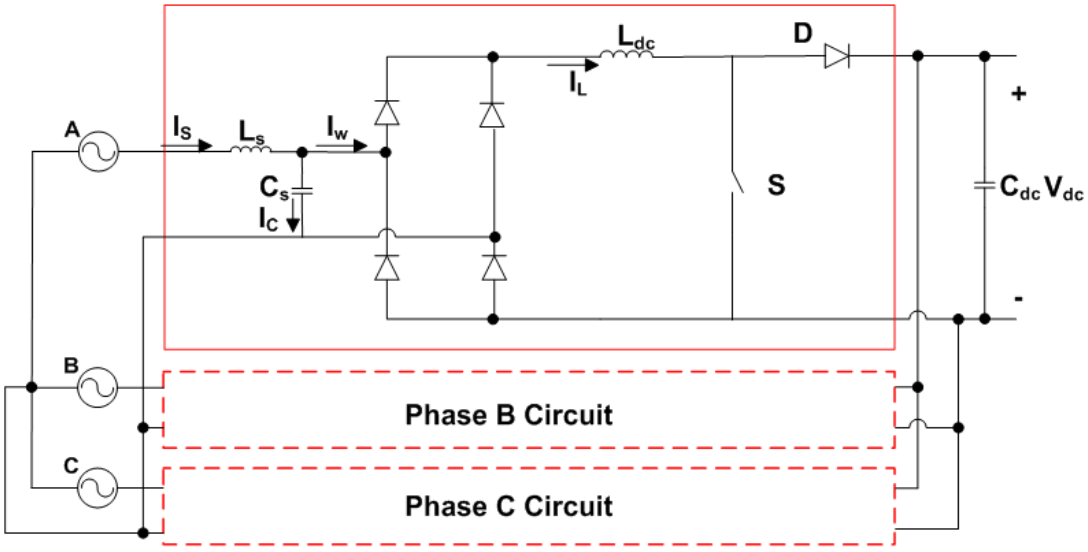


Figure 5-4. Two-stage three-phase buck rectifier topology.

The Si CoolMOS, IXKP13N60C5 from IXYS[138], was selected as the active switch, because an IGBT based converter suffers from higher switching losses than MOSFET based converter due to much higher switching energies of the IGBTs and also from higher conduction losses, as the on-state voltage drop of the IGBT does not scale down linearly with devices paralleling number. The switching frequency is 20 kHz (the method of switching frequency and device paralleling number selection will be introduced in section 5.3).The components in a Si based two-stage rectifier are listed in Table 5-3, including the devices paralleling numbers.The losses, weights and volumes of them are shown inTable 5-4. Figure 5-5shows the distribution of loss, weight and volume of Si based two-stage rectifier. The calculated efficiency of this converter is 98.29%.

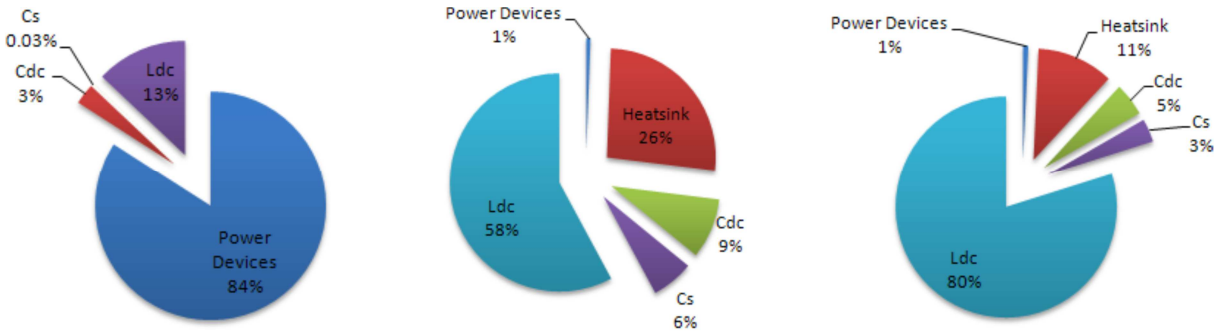
Table 5-3.Components of Si based two-stage rectifier

Component	**Value**	**Specification**	**Physical design**
Active switch		6 paralleled 600 V Si MOSFETs (CoolMOS)	IXKP13N60C5 (IXYS)[138]
Diode in DC-DC converter		600 V fast recovery diode	IDP30E60C (Infineon)[18]
Diode in diode bridge		800 V rectifier diode	DSI30 (IXYS)[138]
Heatsink			Aavid Thermalloy Extrusion 82160
C_S	20 μF × 3	400 V_{ac}	Epcos B32360
C_{dc}	1900 μF × 1	400 V_{dc}	Epcos B43750
L_{dc}	4.5 mH × 3	I_{rms} = 12.5 A	Hitachi FINEMET FT-3M EE core

* $L_S$is 1 μF and is neglected because of the existence of line impedance.

Table 5-4.Loss, weight and volume of Si based two-stage rectifier

	Power Device	**Heatsink**	**C_{dc}**	**L_{dc}**	**C_S**	**Total**
Loss (W)	218.8	0	7.6	33.6	0.1	260.2
Solid volume (cm^3)	43.8	1958.6	663.2	4299.4	463.3	7428.2
Weight (kg)	0.1	2.0	0.9	14.8	0.6	18.4



(a) Loss (b) Volume (c) Weight

Figure 5-5. Loss, volume, and weight distribution of Si based two-stage rectifier.

The SiC JFET, SJEP120R063 from SemiSouth [20] and SiC diode, C3D20060D from CREE [19] were selected as the power devices in SiC based two-stage rectifier. The switching frequency is 46 kHz.

The components' informationofSiC based two-stage rectifier are listed inTable 5-5. Table 5-6shows the loss, weight and volume of these components, and their distribution is shown inFigure 5-6. The calculated efficiency of the converter is 98.77%.

5.2.2 Single-Stage Rectifier

Three-phase current source rectifier (CSR), shown in Figure 5-7, is a selection of topology to realized 480 V_{ac} to 400 V_{dc} through one power conversion stage. Three-phase CSR does not

have phase-leg shoot-through issue and can limit inrush current.

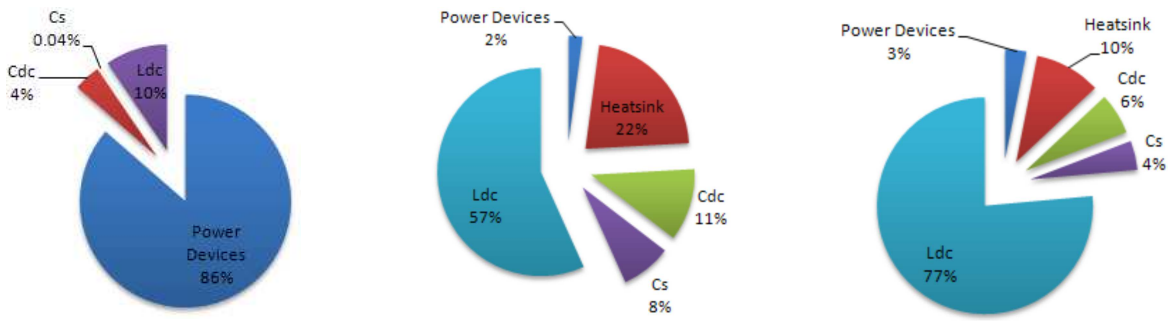
Table 5-5.Components of SiC based two-stage rectifier

Component	Value	Specification	Physical design
Active switch		4 paralleled 1200 V SiC JFETs	SJEP120R063 (SemiSouth)[20]
Diode in DC-DC converter		4 paralleled 600 V SiC diodes	C3D20060D (CREE)[19]
Diode in diode bridge		4 paralleled 600 V SiC diodes	C3D20060D (CREE)[19]
Heatsink			Aavid Thermalloy Extrusion 82590
C_S	20 μF × 3	400 V_{ac}	Epcos B32360
C_{dc}	1900 μF × 1	400 V_{dc}	Epcos B43750
L_{dc}	4.5 mH × 3	I_{rms} = 12.5 A	Hitachi FINEMET FT-3M EE core

* $L_S$is 1 μF and is neglected because of the existence of line impedance.

Table 5-6.Loss, weight and volume of SiC based two-stage rectifier

	Power Device	Heatsink	C_{dc}	L_{dc}	C_S	Total
Loss (W)	161.4	0	7.6	17.8	0.1	186.6
Solid volume (cm^3)	125.4	1297.0	663.2	3348.0	463.3	5897.0
Weight (kg)	0.4	1.4	0.9	10.5	0.6	13.8



(a) Loss (b) Volume (c) Weight

Figure 5-6. Loss, volume, and weight distribution of SiC based two-stage rectifier.

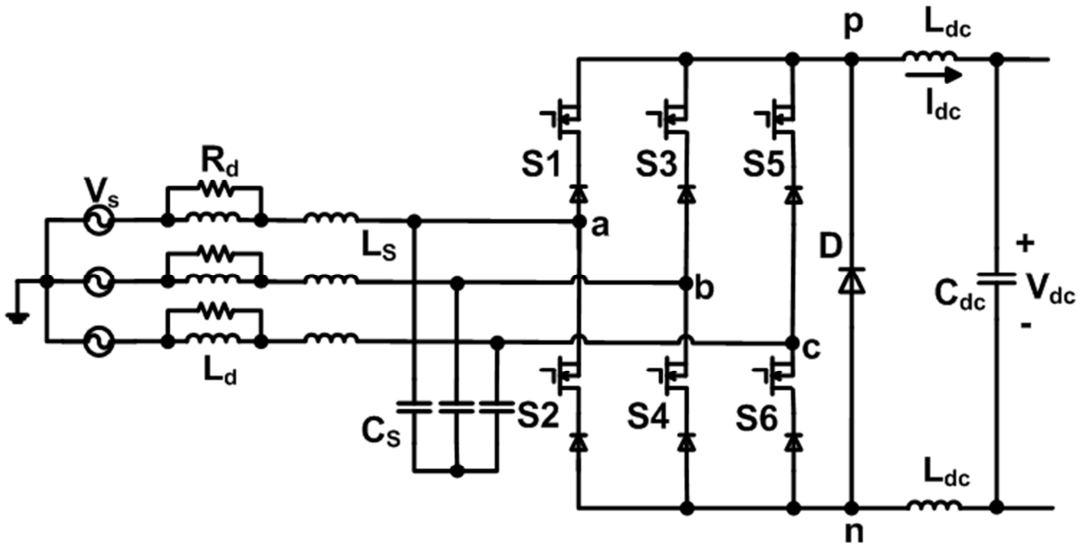


Figure 5-7. Three-phase single-stage rectifier (current source rectifier) topology.

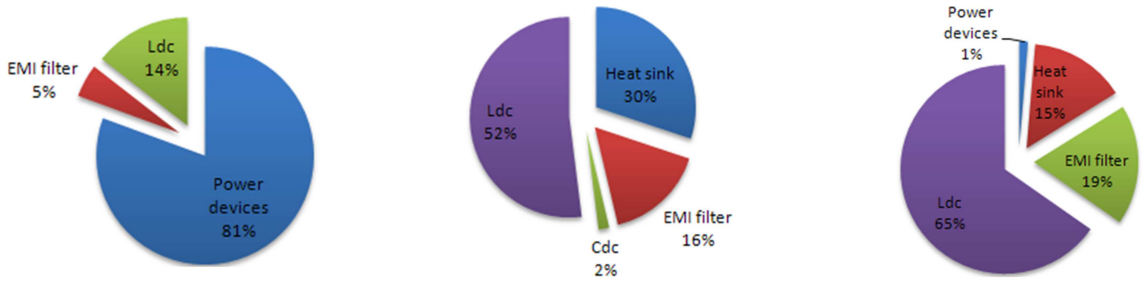
The components in the Si based single-stage rectifier are listed inTable 5-7. The switching frequency is 20 kHz.The loss, weight and volume of these components are given inTable 5-8, and the distribution is shown inFigure 5-8. The calculated efficiency of the converter is 97.85%.

Table 5-7.Components of Si based single-stage rectifier

Component	Value	Specification	Physical design
S1~S6		2 paralleled Si IGBTs + Si diode	IGBT: Infineon IKW40N120T2[18] Diode: Fairchild RHRP30120[139]
D		Si diode	Fairchild RHRG75120 [139]
Heatsink			Aavid Thermalloy Extrusion 83250
C_S	25 μF	400 V_{ac}	Epcos B32928E3256
C_{dc}	20 μF	400 V_{dc}	Epcos B32676G4206
R_d	0.47 Ω	I_{rms} = 0.87A	Rohm MCR25JZHFLR470
L_S	55 μH	I_{rms} = 18.06A	Magnetics R type Ferrite EE core, AWG#15, 19 turns
L_d	25 μH	I_{rms} = 18.06A	Magnetics R type Ferrite EE core, AWG#16, 14 turns
L_{dc}	2.3 mH	I_{rms} = 37.5A	Magnetic Metals 3% Grain Oriented Si Steel EE core, AWG#8, 56 turns

Table 5-8.Loss, weight and volume of Si based single-stage rectifier

	Power Device	Heatsink	C_{dc}	L_{dc}	Input Filter	Total
Loss (W)	265.3	0	7.6	0.5	47.7	329.7
Solid volume (cm^3)	30.0	977.6	56.7	1689.2	663.2	3280.0
Weight (kg)	0.1	1.3	0.9	0.02	5.7	8.7



(a) Loss (b) Volume (c) Weight

Figure 5-8. Loss, volume, and weight distribution of Si based single-based rectifier.

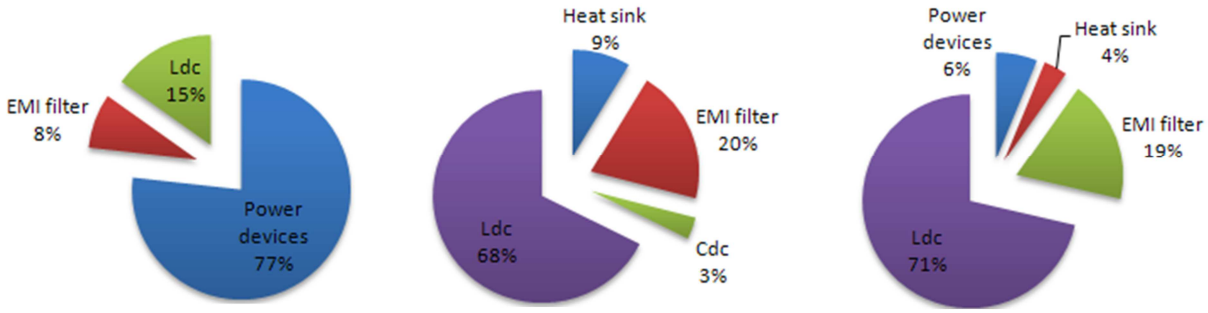
Table 5-9.Components of SiC based single-stage rectifier

Component	**Value**	**Specification**	**Physical design**
S1~S6		6 paralleled SiC JFETs + 6 paralleled SiC diodes	JFET: SemiSouth SJEP120R063[20] Diode: SemiSouth SDP30S120[20]
D		6 paralleled SiC diodes	Diode: SemiSouth SDP30S120[20]
Heatsink			Aavid Thermalloy Extrusion 83250
C_S	24 µF	400 V_{ac}	VISHAY MKP339X2 × 5
C_{dc}	75 µF	400 V_{dc}	Epcos B32778
R_d	0.39 Ω	I_{rms} = 0.27 A	Rohm Semiconductor MCR10EZHFLR390
L_S	30 µH	I_{rms} = 18.06 A	Magnetics R type Ferrite EE core, AWG#10, 10 turns
L_d	15 µH	I_{rms} = 18.06 A	
L_{dc}	1.3 mH	I_{rms} = 37.5 A	Hitachi FINEMET FT-3M EE core, AWG#4, 23 turns

The components in the SiC based single-stage rectifier are listed inTable 5-9. The switching frequency is 35 kHz.The loss, weight and volume of these components are given inTable 5-10, and the distribution is shown inFigure 5-9. The calculated efficiency of the converter is 99.03%.

Table 5-10.Loss, weight and volume of SiC based single-stage rectifier

	Power Device	Heatsink	C_{dc}	L_{dc}	Input Filter	Total
Loss (W)	112.9	0	11.8	0.1	22.4	147.1
Solid volume (cm^3)	123.6	202.0	77.6	1583.7	477.7	2464.6
Weight (kg)	0.5	0.3	1.4	0.03	5.4	7.5



(a) Loss (b) Volume (c) Weight

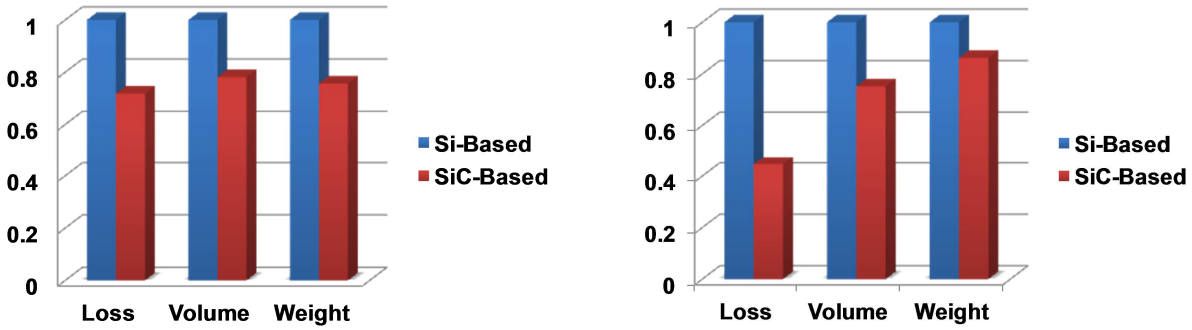
Figure 5-9. Loss, volume, and weight distribution of SiC based single-based rectifier.

5.2.3 Topologies Comparison

Based on the design results, Table 5-11compares Si and SiC based, 15 kW, AC-DC converters for the two different topologies. These two rectifiers are compared inFigure 5-10, which shows the advantages of the SiC based converter. InFigure 5-10, the loss, weight and volume of a Si devices based rectifier are normalized to unity. Figure 5-11compares two topologies based on SiC devices, in which two-stage rectifier results are normalized to unity. From Figure 5-11, a single-stage rectifier, e.g. three-phase current source rectifier, has lower losses, weight and volume. Therefore, it is selected as the topology of front-end converter in 400 V_{dc} architecture data center power supply system.

Table 5-11.Design results comparison of 15 kW rectifier

		Loss (W)	Solid volume (cm^3)	Weight (kg)	Efficiency
Two-stage rectifier	**Si based**	260.2	7384.4	18.4	98.29%
	SiC based	186.6	5771.6	13.8	98.77%
Single-stage rectifier	**Si based**	329.7	3250.0	8.7	97.85%
	SiC based	147.1	2341.0	7.5	99.03%



(a) Two-stage rectifier design results (b) Single-stage rectifier design results

Figure 5-10. Comparison of Si and SiC based rectifiers.

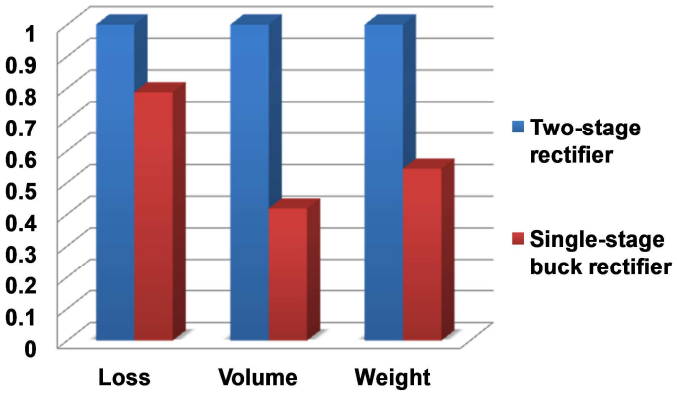


Figure 5-11. Comparison of two topologies based on SiC devices.

5.3 Three-Phase Buck Rectifier Design and Loss Calculation

In this section, a 7.5 kW three-phase current source rectifier using SiC MOSFETs and SBDs is designed and its losses are calculated. The design specifications are listed inTable 5-12, and the circuit is shown in Figure 5-12. Based on IEEE Standard on Power Quality 519, the AC side (grid side) current THD should lower than 5% and power factor should larger than 0.99.

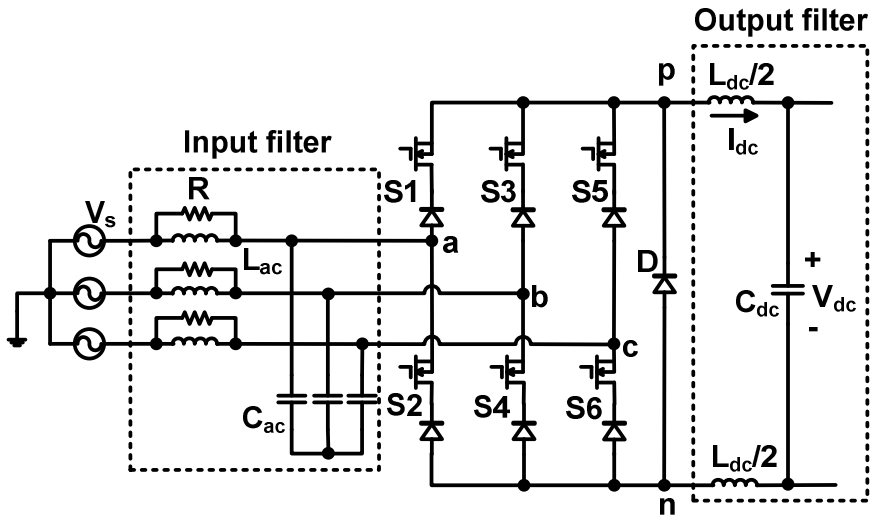


Figure 5-12. Three-phase current source rectifier.

Table 5-12.Specifications of 7.5 kW, all-SiC three-phase current source rectifier

Power rating	7.5 kW
Input voltage	Three-phase 480 V_{ac}
Input range	± 10%
Input current	9 A
Output voltage	400 V_{dc}
Output current	18.75 A
Input power factor	> 0.99
Current total harmonic distortion	< 5%
Operating temperature	50 ºC

5.3.1 Control and Modulation Scheme

The control algorithm of the CSR is shown in Figure 5-13. The main control loop includes the outer DC voltage control loop and inner DC current control loop. In the DC current control loop, the DC current in the output DC inductor is fed back to the current compensator to generate D_d, the duty cycle on the d axis. A PI compensator is derived in (5-1), with 986 Hz bandwidth and 60.8° phase margin.

$$H_{PI\_idc} = 38.33 \times \left(\frac{1 + 0.00051s}{s} \right) \tag{5-1}$$

In the outer DC voltage control loop, the DC voltage on the DC capacitor is fed back to the compensator to generate the DC current reference for the inner DC current control loop. The transfer function of the PI controller in DC voltage closed loop is given in (5-2), with 493 Hz bandwidth and 75.3° phase margin.

$$H_{PI\_vdc} = 88.587 \times \left(\frac{1 + 0.0045s}{s} \right) \tag{5-2}$$

To compensate the displacement power factor caused by the input filter, an input filter current compensation unit is introduced to generate the compensation duty cycles D_{dcomp} and D_{qcomp}, which would be added to D_d and D_{qref} (the duty cycle reference on the q axis which was 0 in the unity-power-factor rectifier) [140].

The performance and dynamic response of the controller is verified by Matlab Simulink. Figure 5-14 to Figure 5-16 show the response of step change of load, DC voltage reference, and input voltage, respectively.+10% step change happens at 0.04 s and -10% step change happens at 0.08 s.It is obvious that the designed control algorithm works well under different conditions for CSR.

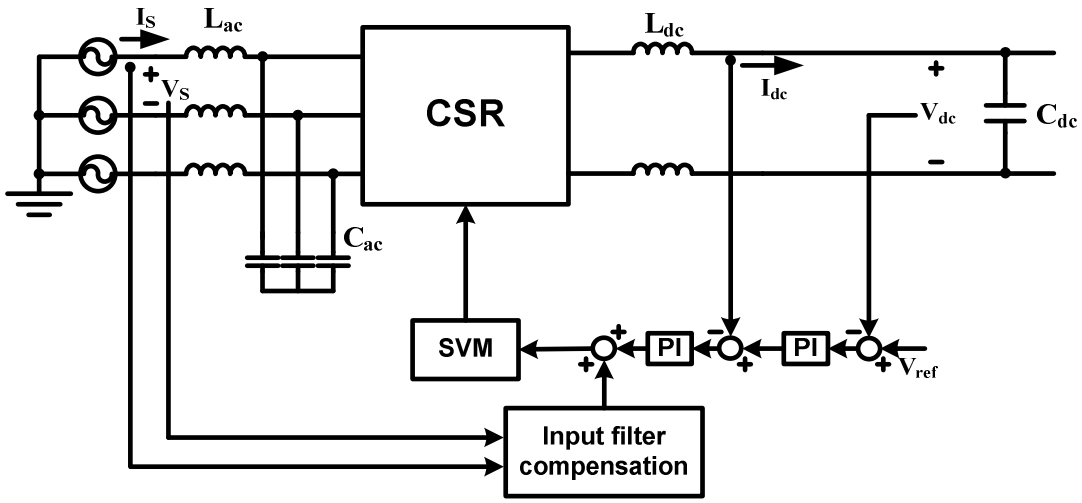
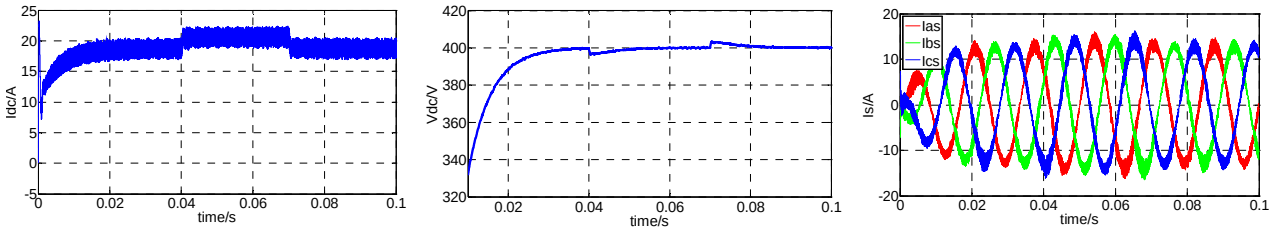
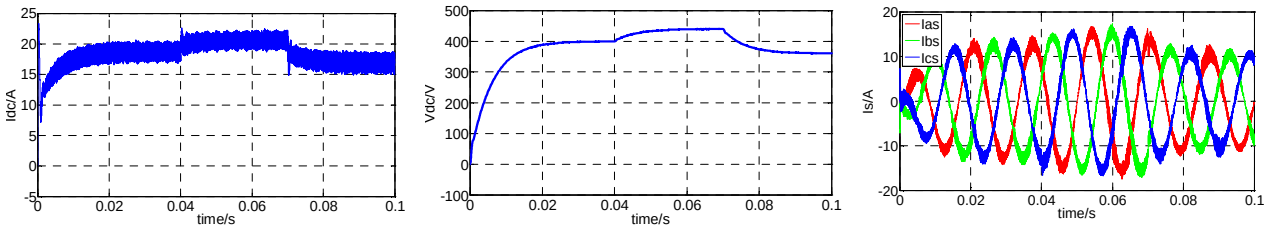


Figure 5-13. Three-phase current source rectifier control algorithm.



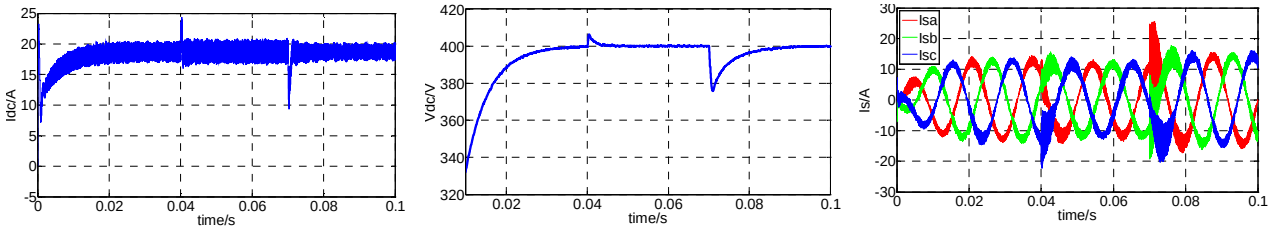
(a) DC current (b) DC voltage (c) AC current

Figure 5-14. Waveforms when load changes ±10%.



(a) DC current (b) DC voltage (c) AC current

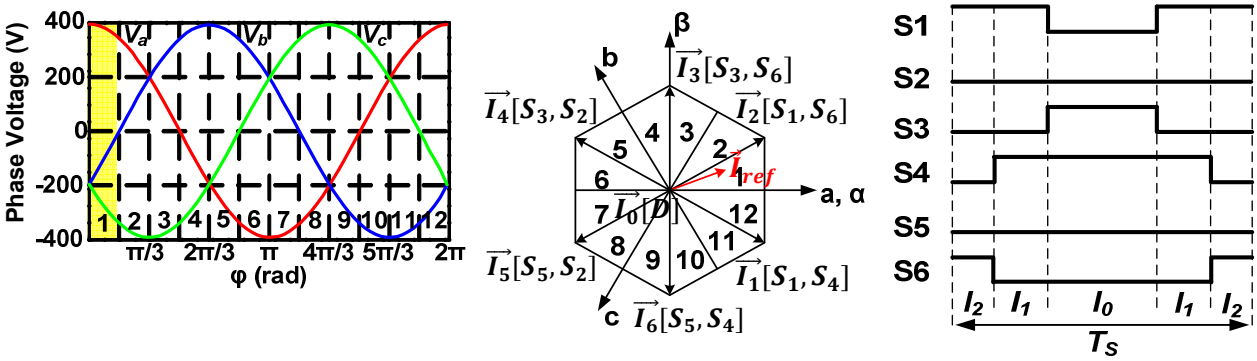
Figure 5-15. Waveforms when DC voltage reference changes ±10%.



(a) DC current (b) DC voltage (c) AC current

Figure 5-16. Waveforms when input voltage changes ±10%.

The modulation scheme used for the high efficiency buck rectifier is the switching loss optimized (SLO) modulation scheme, which has been developed in [82]-[83] and proved to be able to obtain the lowest power loss and increase rectifier efficiency [84]-[85].It is a symmetric SVPWM with 12 sectors, as shown in Figure 5-17(a) and (b). The space vectors are arranged so that the average switching voltage is lowest in symmetric modulation schemes.In sector 1, for example, the vector, commutating with zero vector (I_0), is I_1 not I_2, because the voltage $|V_{ab}| < |V_{ac}|$ in sector 1 from Figure 5-17(a).Figure 5-17(c) shows the gate signals in one switching period (T_S) in sector 1.The zero vectors are realized by conducting a phase-leg (S3 and S4).



(a) AC capacitor voltage waveforms with 12 sectors (b) Sector division (c) PWM signals in sector 10

Figure 5-17. Switching loss optimized modulation scheme for CSR.

5.3.2 Device Paralleling and Switching Frequency

The losses of a converter can be divided into three categories: losses of the semiconductors, losses of the passive components, and the losses of the auxiliary circuit. Each of them should be minimized in order to increase the efficiency of the converter.

As the dominant part of converter losses, the losses of semiconductors need to be considered first and are the main focus of the efficiency optimization for the converter. In this chapter, SiC MOSFETs tested in chapter 4 are used instead of traditional Si IGBT, due to their better switching performance and low forward voltage when paralleled to increase efficiency. In addition, the SiC SBDs measured in chapter 4 are used because of their low conduction loss and negligible reverse recovery loss.

In high efficiency converters, power devices are paralleled to reduce the power losses. Paralleling devices will reduce on-state resistance and conduction loss. However, switching loss may increase. For designed CSR in this chapter, Figure 5-18 shows the total losses of the MOSFETs and diodes with different paralleling numbers in each switching element, at switching frequency f_{SW} of 28 kHz. From Figure 5-18, the curves are nearly flat when MOSFET parallel number $n_S > 4$ and diode parallel number $n_D > 2$. Considering both efficiency and cost, $n_S = 4$ and $n_D = 2$ are selected. Based on the test results in chapter 4, the calculated loss distribution of power devices in this CSR at full load, 7.5 kW, is shown in Figure 5-19. The assumed devices' operating temperature is 50 °C.

Generally, the selection of switching frequency must be performed for the overall system. It is closely related with power devices' switching losses and passive components' losses as well. With higher switching frequency, power devices' switching is larger, but the loss of DC inductor

will be smaller because a smaller DC inductor value could be selected. For the CSR designed in this chapter, the loss comparison at different switching frequencies is shown in Figure 5-20. The converter loss at 20 kHz, 28 kHz, 35 kHz, 46 kHz, and 70 kHz are compared because the cutoff frequency EMI filter is lower when designed under these switching frequencies than their adjacent frequencies.The power devices' losses include the losses in Figure 5-19. The passive components' losses include the losses of DC inductor, DC capacitor, and EMI filter. The auxiliary circuit loss is 12 W.

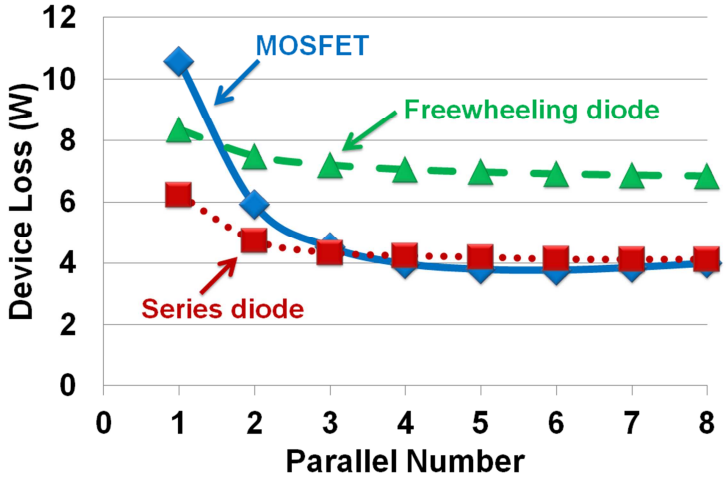


Figure 5-18. SiC devices' total losses vs. paralleled number.

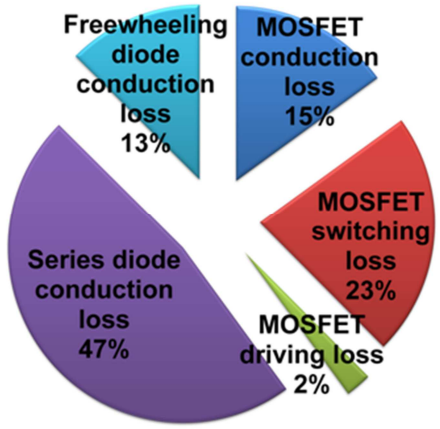


Figure 5-19. Power devices loss distribution of CSR at full load.

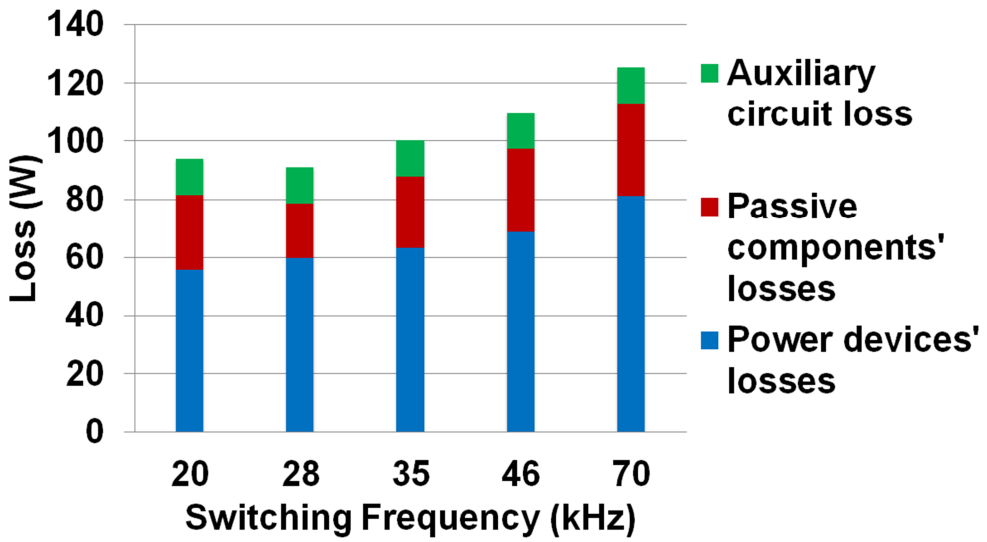


Figure 5-20. Rectifier loss vs. switching frequency.

From Figure 5-20, this CSR obtains the lowest power loss when f_{SW} = 28 kHz, so 28 kHz is selected as the switching frequency.

5.3.3 Filter Design and Loss Calculation

The filter of the three-phase current sourse rectifier includes the output DC side LC filter and the input AC side LC filter. The DC side inductor L_{dc} and capacitor C_{dc} were used as the energy storage components. AC side LC filter (L_S and C_S) is used to meet the harmonic and EMI standard. The ambient temperature in the design is assumed to be 50 ºC.

A. DC filter design and loss calculation

The DC inductorL_{dc} is designed based on the DC current ripple of 20% I_{dc} at full load and the DC capacitorC_{dc} is designed based on the output voltage ripple of 5% V_{dc}.With the method in [125], the value of L_{dc} and C_{dc}areselected to be 1.65 mH and 150 μF, respectively.

Three 50 μF/450 V_{dc} film capacitors are paralleled to build C_{dc} in order to reduce the equivalent series resistance (ESR) and capacitor's loss.

As the energy storage component, the DC inductor has significant contribution to the total loss, weight and volume of the whole CSR.There are many types of materials available for building the inductors, including tape wound material (silicon steel, supermendur, orthonol, permalloy, amorphous alloy, nanocrystalline alloy etc.), powder material (molypermalloy, nickel/iron etc.), and ferrite material.For the DC inductor design, the current is large in the inductor so that the inductor needs to bear high flux in it. By introducing an air gap, EE cores or cut cores can reduce the equivalent permeability and achieve high inductance under large current. Also the powder toroid core can be used to build DC inductors because it has a distributed air gap in the material.

In order to find a suitable core for the low loss DC inductor, different materials are compared in Figure 5-21. The design specification is 0.825 mH, 18.75 A DC current, and the switching frequency is 28 kHz. The x axis is the wire gauge and the y axis is the inductor loss. As shown in Figure 5-21, the inductor loss is different for each material under different wire gauges, and there exists a minimum point in each curve. It is obvious from Figure 5-21 that the inductor using nanocrystalline core has the lowest loss than other cores.

A nanocrystalline cut core designed and used to build the DC inductor of CSR is shown in Figure 5-22. The design data are listed in Table 5-13. The copper foil is used as the conductor instead of solid wire, because it was much easier to bend and its copper loss was smaller at high frequency. The loss of the copper foil could be calculated with the method in [141] and the core loss is calculated with GSE [142]. The kapton film is used as the insulation for the inductor. The copper foil windings, 21 turns each leg, keep away from the air gap to avoid additional loss due to the high temperature around air gap.

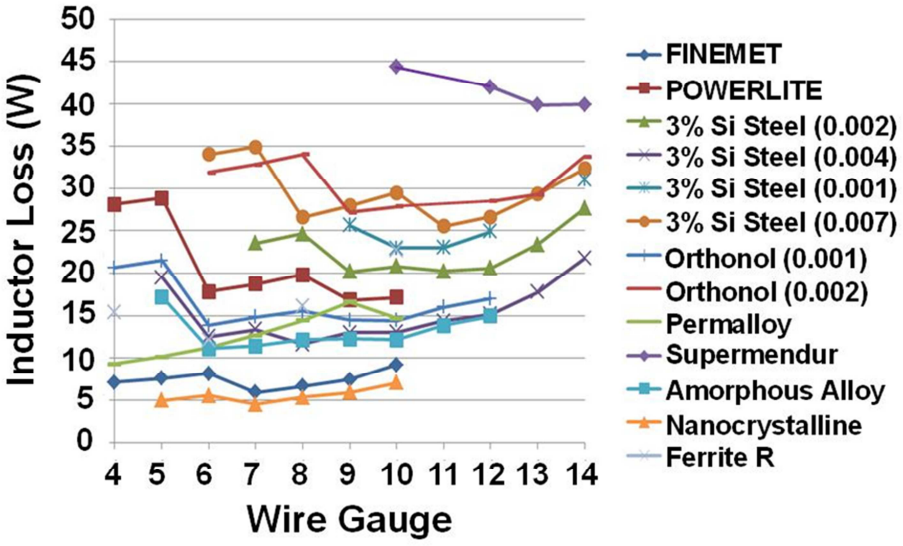


Figure 5-21. Material comparison for DC inductor design.

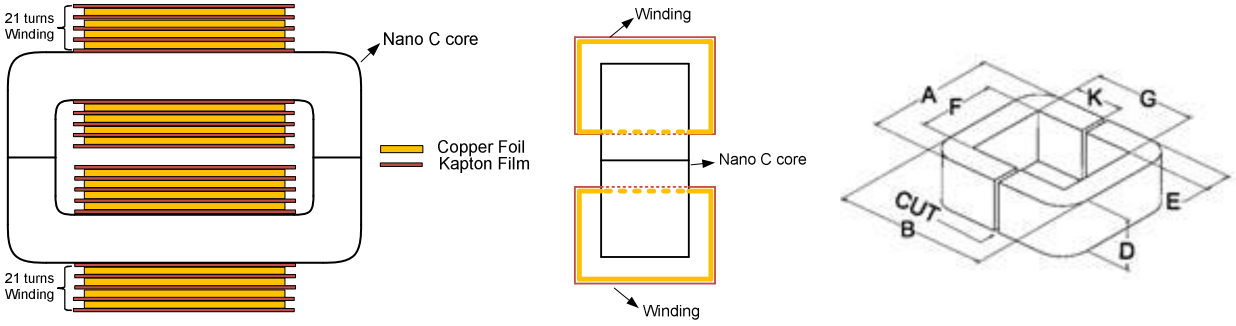


Figure 5-22. Structure of the DC inductor.

Table 5-13.Design data of DC inductor

Core	**Type**		L_{dc}	**Turn**	**Total loss**	**Weight**
Cut core	Nanocrystalline		1.65 mH	42 (21 each leg)	6.8 W	2.0kg
Dimensions						
Core	D	43 mm	E	22 mm	F	55 mm	G	22 mm
Copper foil	Thickness		0.254 mm		Width		50.8 mm	
Kapton film	Thickness		0.127 mm		Width		63.5 mm	

A photo of the constructed DC inductor is shown in Figure 5-23 and its measured value is shown in Table 5-14. The measured value of the DC inductor is higher than the designed value. That is because the air gap (0.72mm) is a little smaller than the designed value (0.75mm). Considering the permeability will be smaller under DC bias, the inductor value will be smaller under DC bias. So this value is acceptable and the winding turns can be reduced to adjust the inductor value if needed.

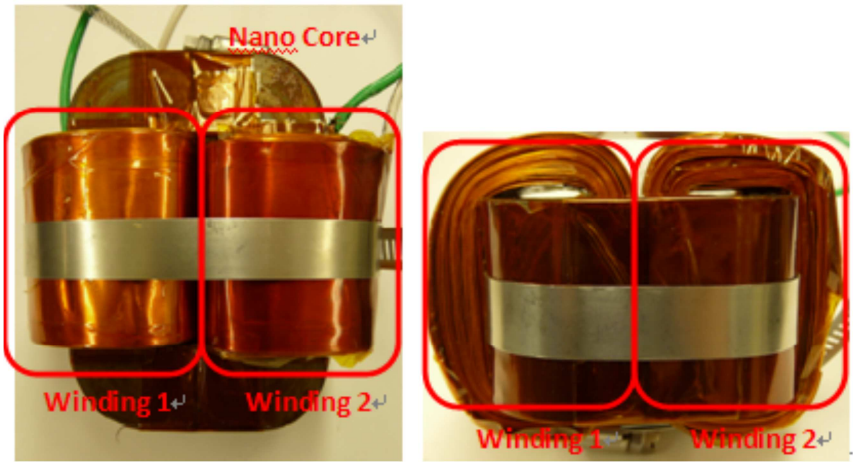


Figure 5-23. Photo of the DC inductor.

Table 5-14.DC inductor measurement results

	Inductor	**Equivalent Parallel Capacitance (EPC)**	**Resonant Frequency**
Winding 1	480 μH	132 pF	627 kHz
Winding 2	470 μH	140 pF	619 kHz
Total	1.92 mH	38 pF	587 kHz

B. AC filter design and loss calculation

The input filter is the LC filter to meet the input current harmonics lower than 5%. In each

phase, the input capacitor consists of four paralleled 1.5 μF/330 Vac film capacitors, whose loss can be neglected. The inductor cores with high permeability and low core loss are suitable to build the AC side inductors. With high permeability, fewer winding turns can be used to reduce copper loss. Ferrite R, EE coreis selected to build the AC inductors. 13 turns of #12 AWG wire are used for the inductor in each phase. The photo of AC inductors is shown in Figure 5-24. The AC inductors' total loss is 6.1 W, the weight is 0.78 kg, and the volume is 163.2 cm^3. The total power loss of these inductors with paralleled 180 Ω damping resistor in each phase is 10.57 W.

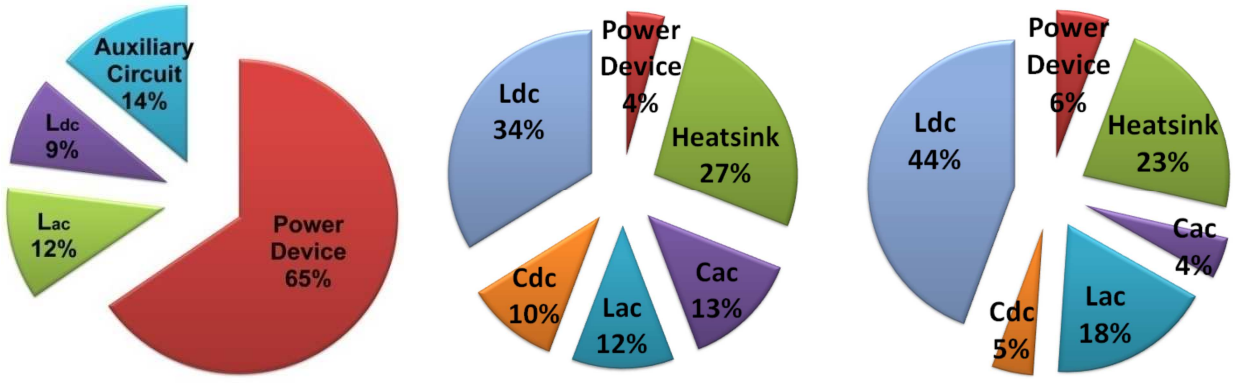
Figure 5-24. Photo of the AC inductors.

5.3.4 Design Results and Comparison

According to the design and loss calculation above, the power loss of SiC based 7.5 kW three-phase current sourcerectifier with 28 kHz switching frequency is 91.52 W at full load. The weight is 4.4 kg, and the solid volume is 1417 cm^3. The design results are listed inTable 5-15.Figure 5-25(a)-(c) show the loss, weight, and volume distribution of the rectifier, respectively.

To show the advantages of SiC power devices in development of high efficiency converters, other combinations of power semiconductors are considered for three-phase buck rectifiers for the same application. The losses of these rectifiers are calculated and compared with the all-SiC

rectifier presented above. These converters are also designed based on the specifications in Table 5-12. Considering the 680 V amplitude of input line-to-line voltage across switches and the voltage overshoot during a switching transient, only 1200 V power devices are investigated. The first rectifier is based on Si IGBTs and Si diodes (all-Si rectifier). The second one is based on Si IGBT and SiC Schottky diodes (Si-SiC rectifier). The third one is based on Si reverse blocking IGBTs (RB-IGBT rectifier). The power devices in each rectifier are selected due to their low loss. For example, 1200 V Si IGBT IKW40N120T2 [18] is used in all-Si rectifier because its power loss is smaller than other 1200 V Si IGBTs in this application according to calculation. The device paralleling number is decided by considering both conduction loss and switching loss. The switching frequency selection and comparison range is the same with the all-SiC rectifier. To avoid large passive loss and large DC inductor in this current source converter, low switching frequencies are not considered. From calculation, 20 kHz is used for these three rectifiers due to the high switching loss of Si active switches, which increases the total loss at higher switching frequencies.



(a) Loss distribution (b) Volume (c) Weight

Figure 5-25. Loss, volume, and weight distribution of 7.5 kW CSR.

Table 5-15. 7.5 kW, SiC basedCSR design results

Power device	Switching frequency	Cooling	Power loss	Solid volume	Weight
SiC MOSFET (4 in parallel) SiC diode (2 in parallel)	28 kHz	Liquid cooling	91.52 W @ full load	1417 cm^3	4.4 kg

The total loss of the all-Si rectifier is 241.1 W at full load, using 1200 V IGBT IKW40N120T2 and 1200 V diode RHRG75120 [139]. So the converter full load efficiency is 96.89%. The devices' paralleling number $n_{IGBT} = n_D = 2$, because the loss of paralleled IGBTs achieves the lower value with $n_{IGBT} = 2$ than with other paralleling numbers. Due to the high switching loss of Si IGBT, the dominant portion of power losses is the IGBT switching loss of 82.2 W, higher than IGBT conduction loss of 39.6 W and series diode conduction loss of 59.6 W.

For the Si-SiC rectifier, the use of 1200 V SiC Schottky diode SDP60S120D helps to reduce diode conduction loss and avoid losses caused by diode reverse recovery. However, most of the loss still comes from the IGBT switch loss. With devices' paralleling number $n_{IGBT} = n_D = 2$, the total loss is 171.9 W, resulting in rectifier full load efficiency of 97.76%.

The reverse blocking IGBTs (RB-IGBT) have advantages in current source converters because of their characteristic of bidirectional voltage blocking. Series diodes can be eliminated after using RB-IGBTs. However, the high current overshoot during turn-on transient and long tail current during turn-off cause high switching loss of RB-IGBT. The losses of RB-IGBT in this rectifier are estimated based on[143]. Paralleling devices will not help to reduce the total loss of RB-IGBT in this application, because the reduction of conduction loss is small due to the built-in voltage and the switching loss is large. So RB-IGBT is not paralleled in this design and $n_{RB\text{-}IGBT} = 1$. The freewheeling diode selected is SiC Schottky diode SDP60S120D and $n_D = 2$.

The total loss of RB-IGBT rectifier is 195.8 W and the full load efficiency is 97.46%.

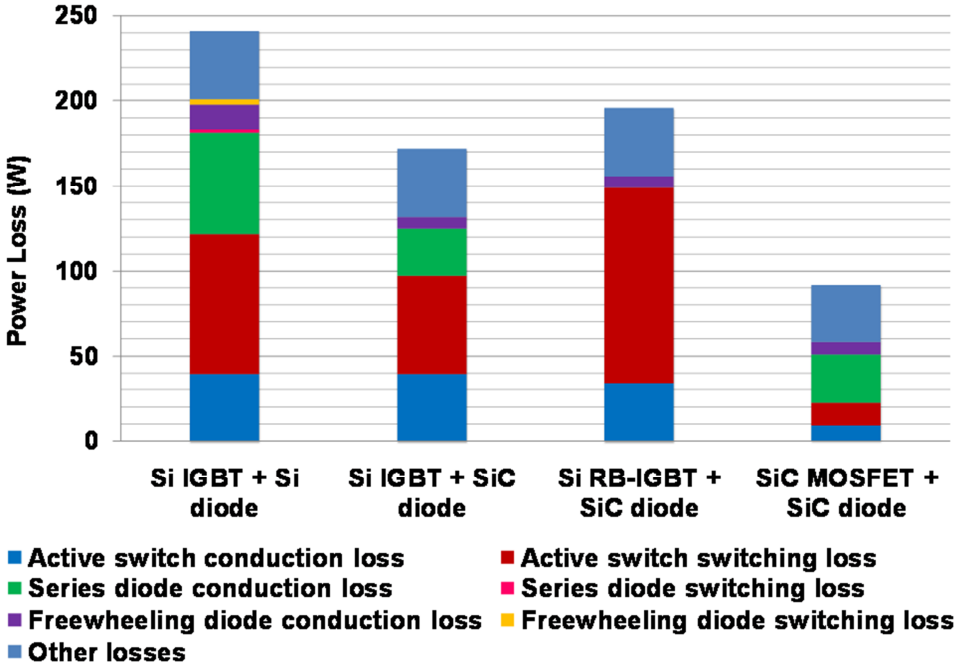


Figure 5-26.Comparison of current source rectifiers based on different power devices.

Figure 5-26 shows the power loss distribution and comparison of buck rectifiers based on different power switches combinations. Other loss in Figure 5-26 includes device driving loss, passive loss, and auxiliary circuit loss. From Figure 5-26, all-Si rectifier has mostly IGBT switching loss. The conduction losses of diodes and IGBTs are large too, which cannot be reduced significantly by paralleling due to the built-in voltage. By replacing Si diodes with SiC Schottky diodes, diode conduction loss decreases. The IGBT switching loss is also reduced because of negligible reverse recovery of SiC Schottky diode. The sum of conduction losses of active switches and diodes, which is larger than IGBT switching loss in all-Si and Si-SiC rectifiers, is significantly reduced when using RB-IGBTs. And the RB-IGBT rectifier is more efficient than all-Si rectifier. However, RB-IGBT switching loss is too large and limits converter

efficiency. In the all-SiC rectifier, power losses of active switches are much lower than other Si active switches. The switching loss decreases considerably by using SiC MOSFETs, and the series diode conduction loss becomes the dominant portion of the total loss. Thus, the all-SiC rectifier will be more efficient at light load conditions.

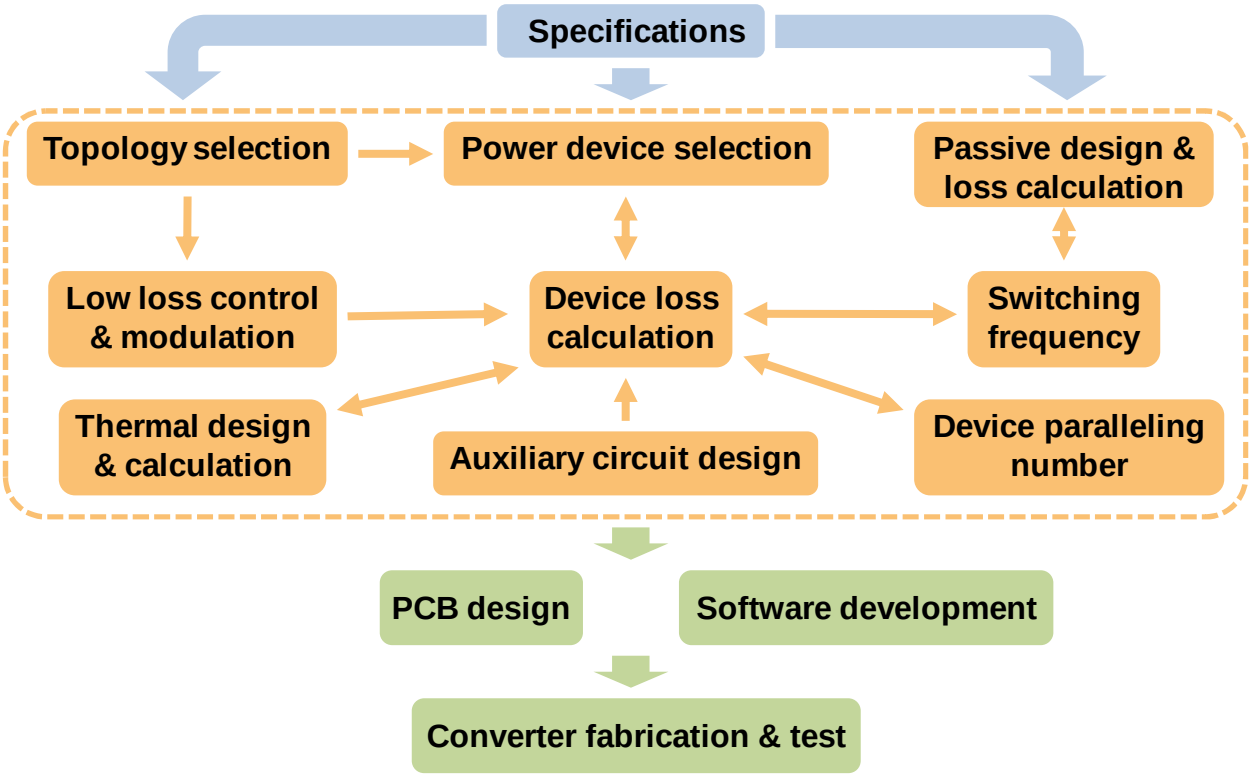


Figure 5-27. High efficiency three-phase converter design procedure.

Figure 5-27 shows the procedure of high efficiency three-phase converter design. Basedon design specifications, the low loss topology and power devices can be selected. When calculating the power devices' loss, the thermal design, switching frequency, device paralleling number, selected modulation scheme and auxiliary circuit should be considered. The devices' loss should be calculated based on its junction temperature. The device paralleling number should be decided based on calculated devices' losses considering different switching frequency. In addition,

passive components' design should considering design specification and switching frequency. The switching frequency can be selected after comparison of converter loss at different switching frequency values. Power devices may need to be reselected after the device loss calculation. After the loss calculation of the converter, PCB should be designed with minimized parasitics and control algorithm needs to be developed. Final step is the converter test and function realization.

5.4 Three-Phase Current Source Rectifier Prototype– I

5.4.1 Power Stage Design and Structure

The three-phase CSR test was conducted based on the circuit shown inFigure 5-12. Figure 5-28shows the prototype of all-SiC three-phase current source rectifier and Figure 5-29 shows the structure of it.The controller hardware includes a DSP board and an interface board. The DSP board used is the TI eZdspTM F28335 evaluation board. The control algorithm of the converter is realized on the DSP board. The interface board acts as the interface between the DSP board and the main board. It is used to realize sensor signal conditioning, PWM signal conditioning, hardware protection, and auxiliary power supply.The interface board and DSP board are attached to the top of the main board, which hosts power devices, gate drivers, sensors, AC input capacitors, and DC output capacitors.The signals from the outputs of sensors are sent to the interface board from the main board, and then sent to the DSP for calculation. The DSP outputs PWM signals to drive power MOSFETs on the main board through the interface board.The power for sensors and power devices' gate drivers on the main board is obtained from the interface board.

The cold plate is beneath the main board. The thermal structure is shown inFigure 5-30. The

power devices are under the main board and fixed on the top surface of the cold plate by screws. The thermal pad, which is put between the power device and the surface of the cold plate for insulation, is Sil-Pad 600. The cold plate selected in the test is the six-pass tube cold plate, 416101U00000G, from Aavid[144], as shown inFigure 5-31. Thermal calculation is based on the calculated power device loss. The maximum junction temperature ofthe SiC MOSFET in the converter is 125 ºC and SiC SBD maximum junction temperature is 175 ºC. Temperature rise on each part and total temperature rise at liquid temperature of 50 °C and flow rate of 5.68 liter per minute (LPM), 1.5 gallon per minute (GPM),at 28 kHz switching frequencyare shown in Table 5-16.

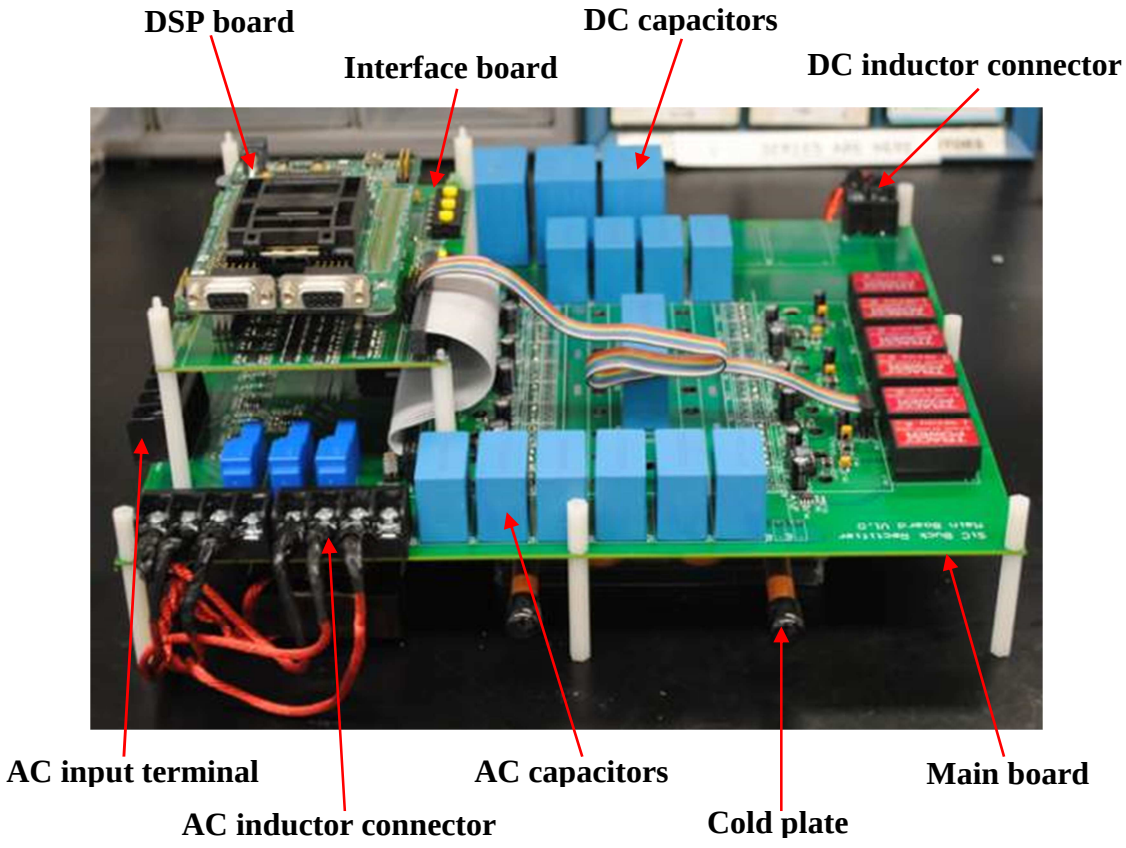


Figure 5-28. 7.5 kW, all-SiC three-phase current source rectifier prototype.

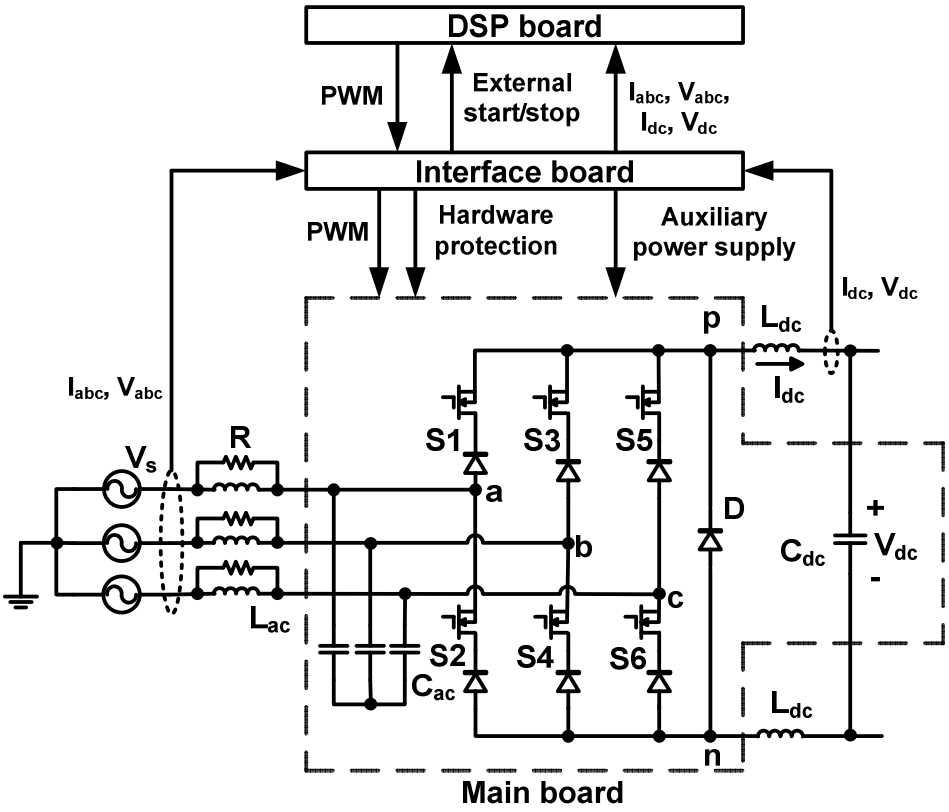


Figure 5-29. Three-phase current source rectifier structure.

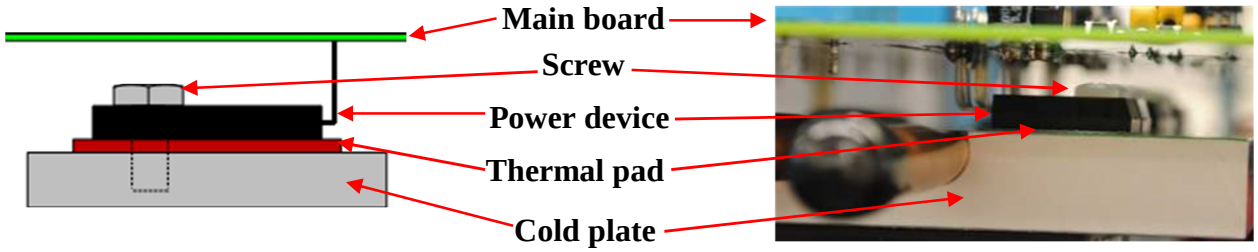


Figure 5-30. Thermal structure of three-phase current source rectifier.

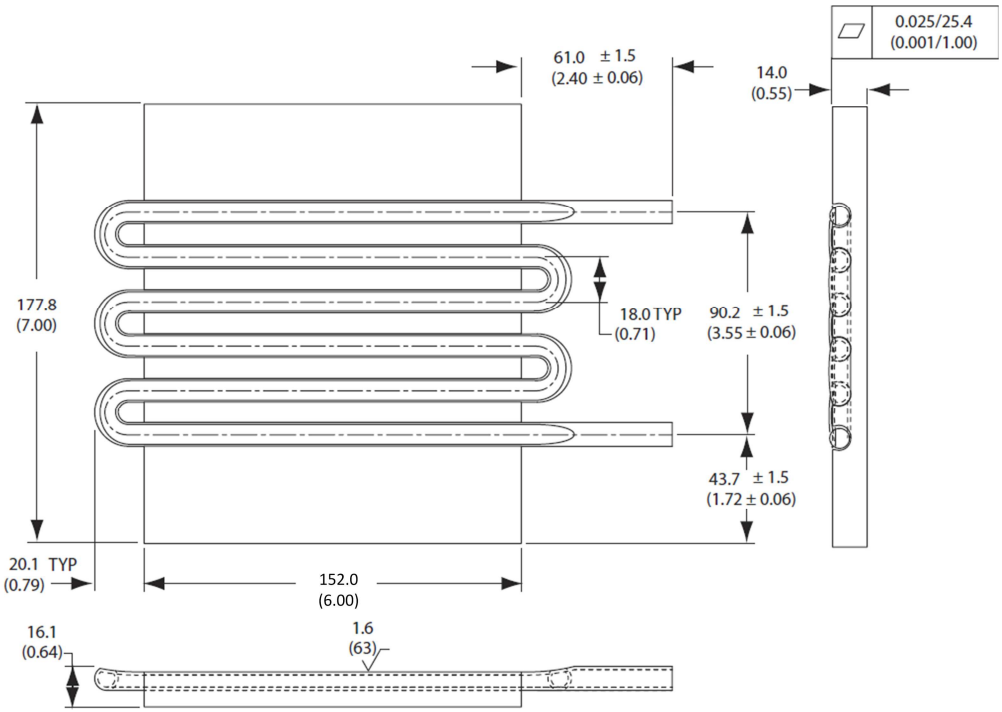


Figure 5-31.Six-pass tube cold plate.

Table 5-16. Thermal calculation with 28 kHz switching frequency and 50 ºC coolant

	Power device temperature rise ΔT (ºC)	**Thermal pad temperature rise ΔT (ºC)**	**Cold plate temperature rise ΔT (ºC)**
MOSFET	0.44	1.5	0.5
Series diode	0.70	2.3	
Freewheeling diode	1.22	4.0	

5.4.2 Experimental Results

The rectifier is tested with resistor load, 480 $V_{ac,rms}$ line-to-line input voltage and 400 V_{dc} output voltage, from 1 kW to full load. The overlap time used in the test is 400 ns to avoid DC current interruption during current commutation process. Figure 5-32 shows the test setup. The

input voltage is provided by AC power supply FCS Series II from California Instrument. The load bank is consisted by 24 10 Ω, 1 kW resistors. The power devices are cooled by the liquid with 50% ethylene glycol, 50% water, provided by a chiller. The liquid flow rate is 5.68 LPM(1.5 GMP) which is recommended by the cold plate used. The liquid temperature at the chiller output is 50 °C. The voltages are measured by differential probes Tektronix P5205, the AC current is measured by the current probe Tektronix TCP202, and the DC current is measured by the current probe Tektronix TCP305. Figure 5-33 shows the waveforms of DC voltage (V_{dc}), DC inductor current ($I_{dc,L}$), AC side phase A current (i_{as}), and voltage (v_{as}), at full load, with chiller output temperature of 50 °C.The input power factor is 0.9996 and the input current total harmonic distortion (THD) is 2.9%, which meet the requirement in Table 5-12. According to the specifications shown in Table 5-12, the converter can work with input voltage range of 480 V ± 10%. The test waveforms are shown in Figure 5-33(b) and (c).

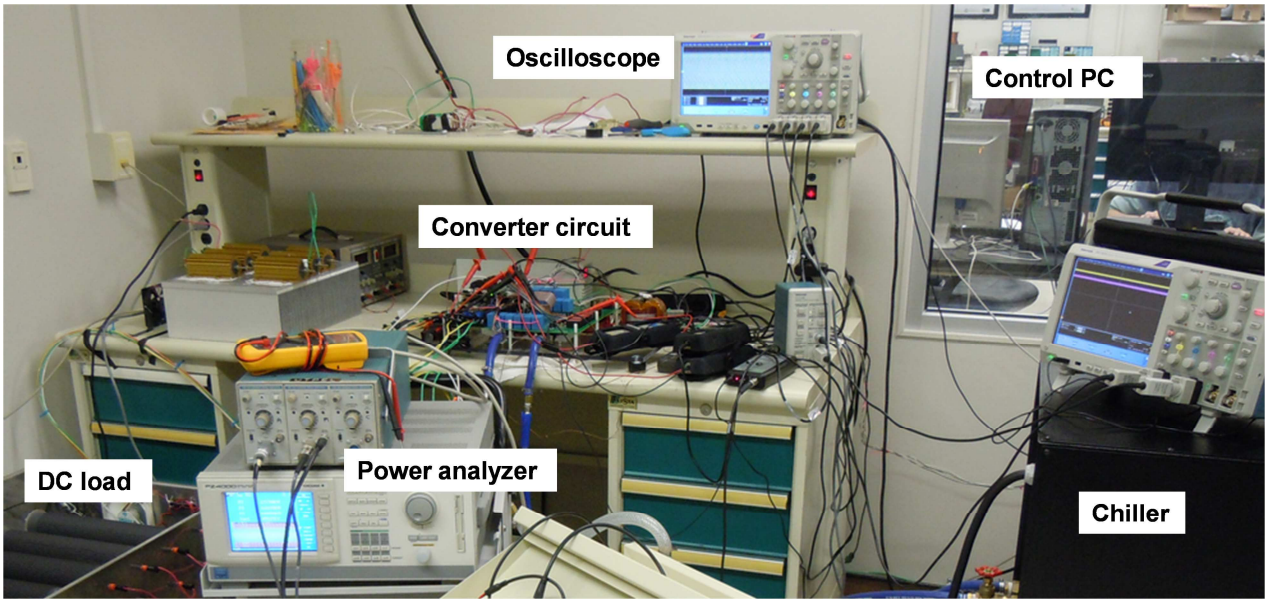
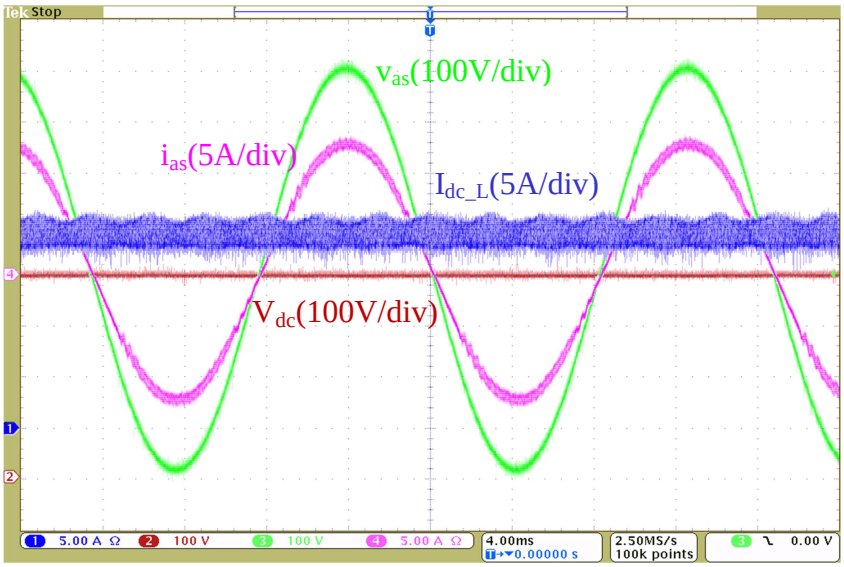
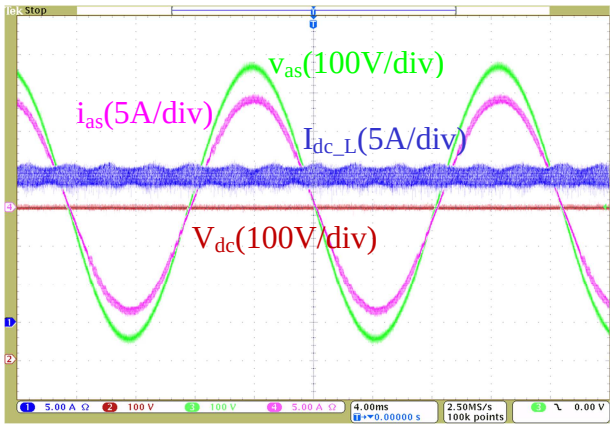


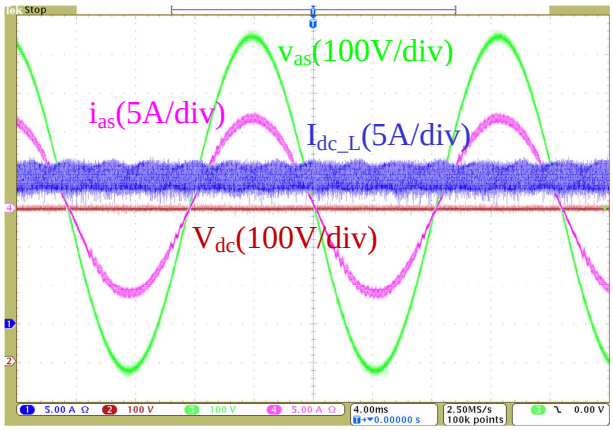
Figure 5-32. All-SiC current source rectifier test setup.



(a) Input voltage 480 V_{ac}



(b) Input voltage 432 V_{ac}



(c) Input voltage 528 V_{ac}

Figure 5-33. All-SiC current source rectifier test waveforms.

The power of the converter is measuredby the power analyzer, PZ4000, with measurement module P/N 253752 (1 kVrms and 20 Arms rating) from Yokogawa[145]. The measurement sample rate is 1 MS/s, and 10 line periods (1 ms) data are used for efficiency calculation. For the efficiency calculation, input line currents and line-to-line voltages are measured to calculate input power (P_{in}), given in (5-3), and output DC current and voltage are used to calculate output power (P_{out}), given in (5-4). The 12 W auxiliary circuit loss (P_{aux}) from the DSP evaluation board

and interface board is included in the efficiency calculation. Finally, the efficiency of the converter (η) is calculated by (5-5).

$$P_{in} = I_a \times V_{ac} + I_b \times V_{bc} \tag{5-3}$$

$$P_{out} = I_{dc} \times V_{dc} \tag{5-4}$$

$$\eta = \frac{P_{out}}{P_{in} + P_{aux}} \times 100\% \tag{5-5}$$

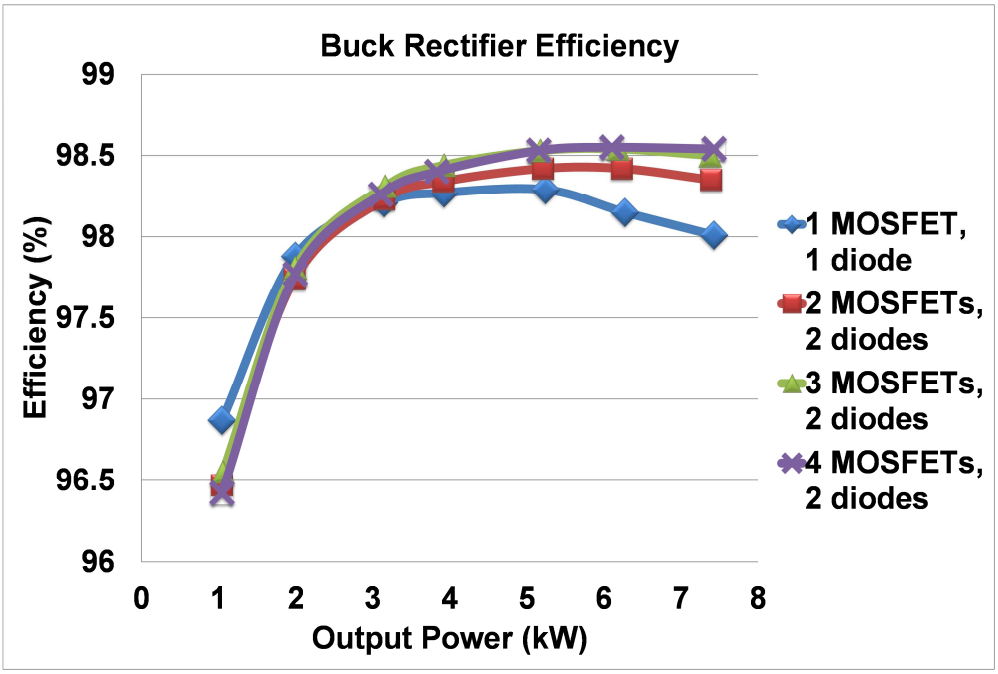


Figure 5-34. All-SiC CSR efficiency at 50 °C with different device paralleling number.

Table 5-17 shows the converter efficiency at different output power levels at 50 °C chiller output temperatures, with 4 paralleled SiC MOSFETs and 2 paralleled SiC diodes in each switching element. The full load efficiency of CSR is 98.54% and the highest efficiency is 98.55% which appears at 6.4 kW output power. From Table 5-18 which lists the full load efficiency at

50 °Cwith different device paralleling numbers, the CSR efficiencyis increased from 98.01% with single MOSFET and single diode to 98.54% with four paralleled MOSFETs and two paralleled diodes.Figure 5-34 shows the efficiency curves. From Figure 5-34, the paralleling of power devices decreases converter efficiency at low loads because the paralleling increases switching loss which is more dominant at low power levels.

Table 5-17. All-SiC CSR efficiency with 4 paralleled MOSFETs and 2 paralleled diodes

Output power	**CSR efficiency**
1 kW	96.42%
2 kW	97.77%
3.2 kW	98.26%
4 kW	98.40%
5.33 kW	98.53%
6.4 kW	98.55%
7.6 kW	98.54%

Table 5-18. All-SiC CSR efficiency at full load

Device paralleling number	**CSR efficiency at full load**
1 MOSFET and 1 diode	98.01%
2 MOSFETs and 2 diodes	98.35%
3 MOSFETs and 2 diodes	98.50%
4 MOSFETs and 2 diodes	98.54%

5.5 Three-Phase Current Source Retifier Prototype – II

An updated hardware prototype of a three-phase CSR in section 5.4 was developed and tested experimentally. The modular design is described in this section.

5.5.1 Modular Designed Current Source Rectifier

Based on the converer design in section 5.3, each switching element includes four paralleled discrete SiC MOSFETs and two paralleled discrete SiC Schottky diodes. In the hardware design in section 5.4, the main board holds all the power devices. The failure of any power device will cause the replacement of the hold board and other devices, which will increase the cost and recovery complexity. In this section, all power devices in each switching element and MOSFET gate driver are prepared on the separated module, shown in Figure 5-35.

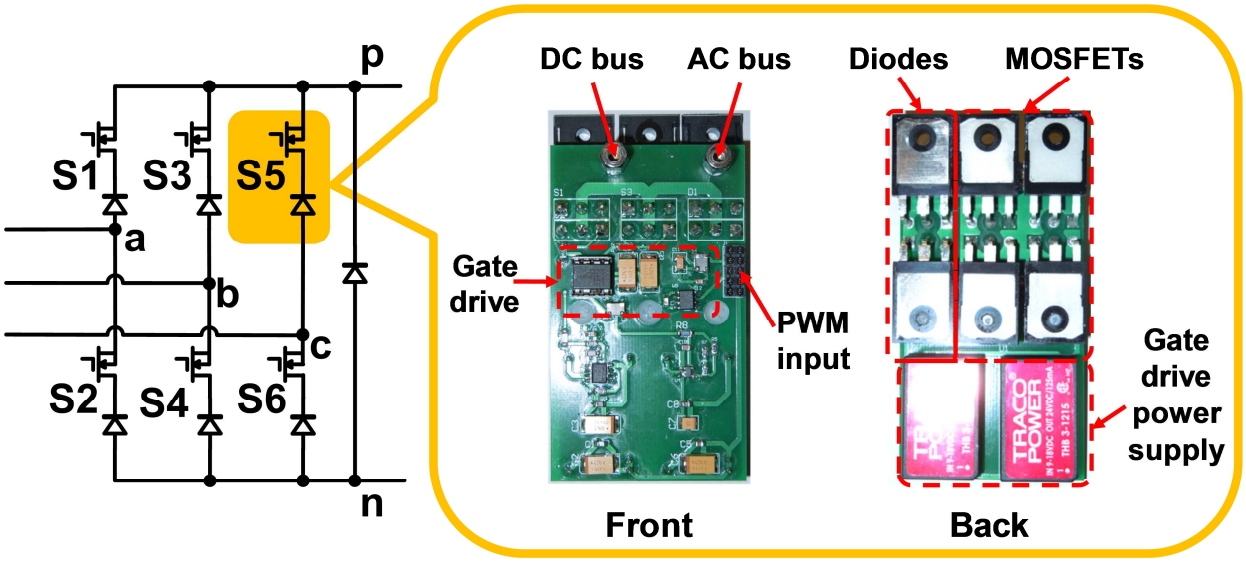


Figure 5-35. Swithing element module in CSR.

Figure 5-36 shows the structure of the CSR prototype. Each switching element module is connected to the main board through a DC bus connector and an AC bus connector. This will

simplify the DC and AC buses layout on main board to reduce the overlap area between AC and DC buses and two DC buses, in order to reduce the parasitic capacitance. The switching element module receives the PWM signals from the interface board through the main board. The separation of the gate drives from the main board helps to reduce the influence of the high power on gate drive singals. The main board only holds AC capacitors, current and voltage sensors, and the device overvoltage protection circuit. There are two DC current sensors, one is arranged in the positive DC-link and another one is arranged in the negative DC-link. With two DC current sensors, the circulating current can be sensed when several rectifiers are operated in parallel. The paralleling operation of three-phase CSRs will be discussed in Chapter 6. The device overvoltage protection circuit usesthree transient voltage suppression (TVS) diodes in series to achieve 1200 V clamping voltage. The series TVS diodes are paralleled with each switching element through the diode bridge to avoid the voltage across the power deives exceeding their rated voltage 1200 V, shown in Figure 5-37.

A picture of the updated prototype of CSR is shown in Figure 5-38. The dimension of the converter is 220 mm × 220 mm × 100mm.

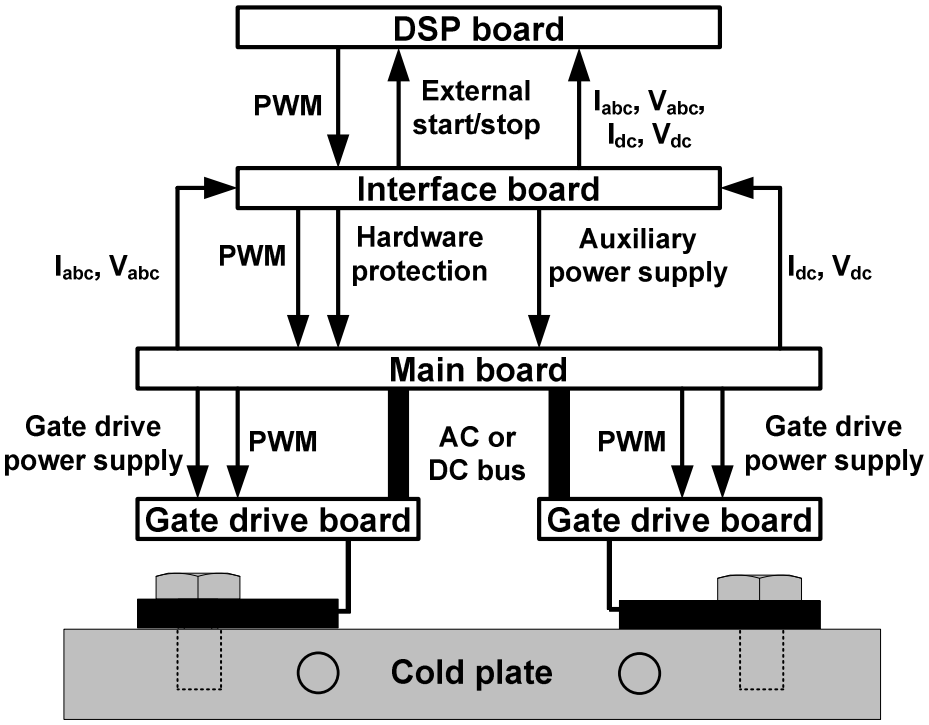


Figure 5-36. Three-phase current source rectifier structure.

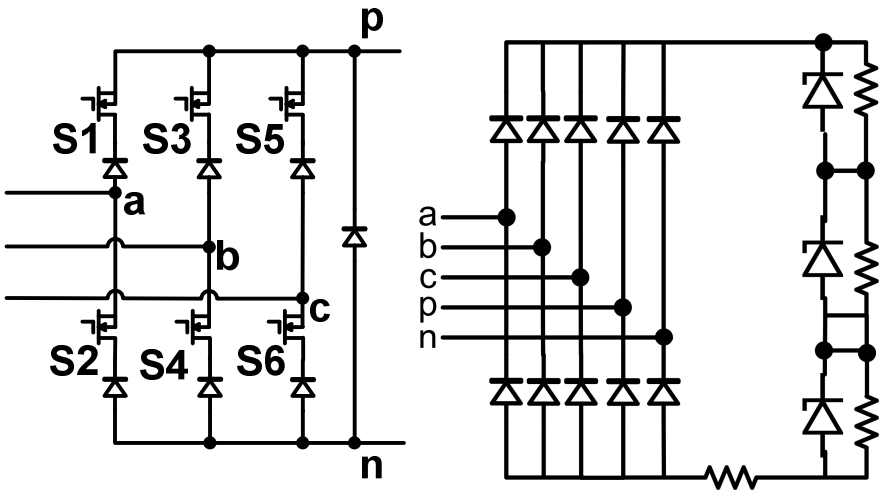


Figure 5-37. Three-phase CSR and power device overvoltage protection circuit.

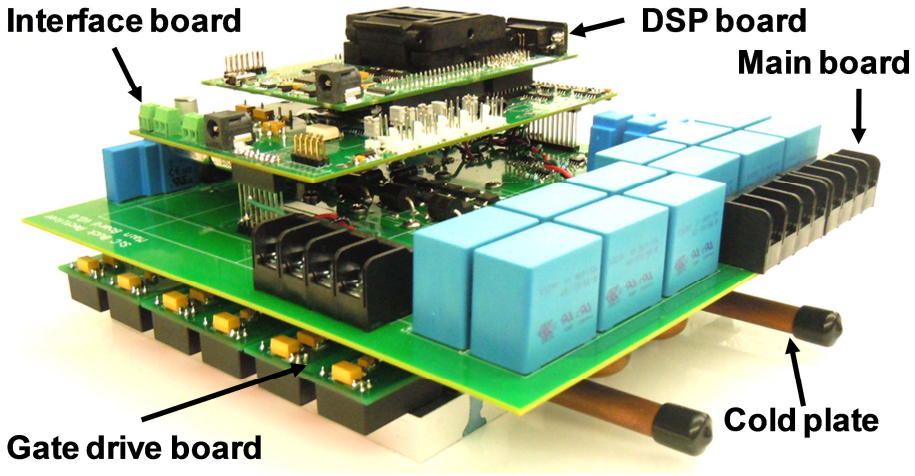


Figure 5-38. Second version of all-SiC three-phase current source rectifier prototype.

5.5.2 Experimental Results

The test setup of the second version of CSR is the same with the test setup for the first version of CSR described in section 5.4.2. The maximum output power is 10 kW. The overlap time of 400 ns is used. The converer waveforms at 10 kW is shown in Figure 5-39, with 480 V_{ac} input voltage (line-to-line voltage) and 400 V_{dc} output voltage. In Figure 5-39,I_{dc} is the current on the DC inductor, V_{dc} is the output voltage, V_{ab} is input line-to-line voltage, and I_a is input line current (phase A).

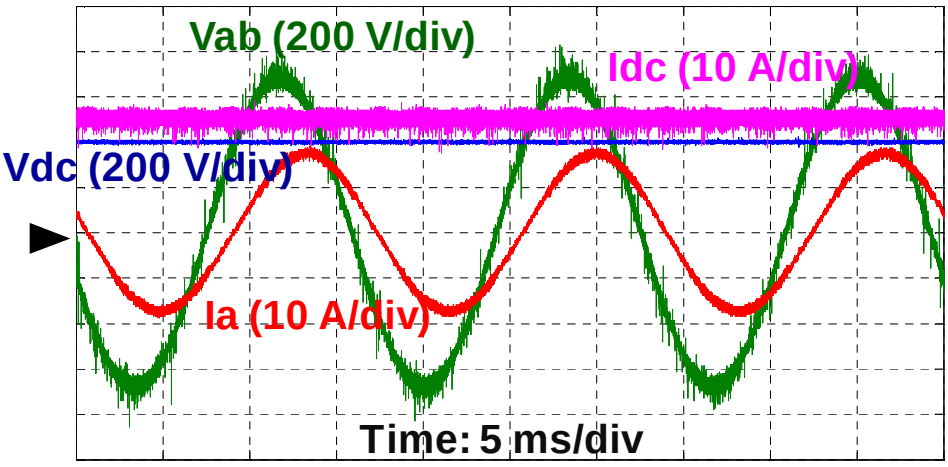
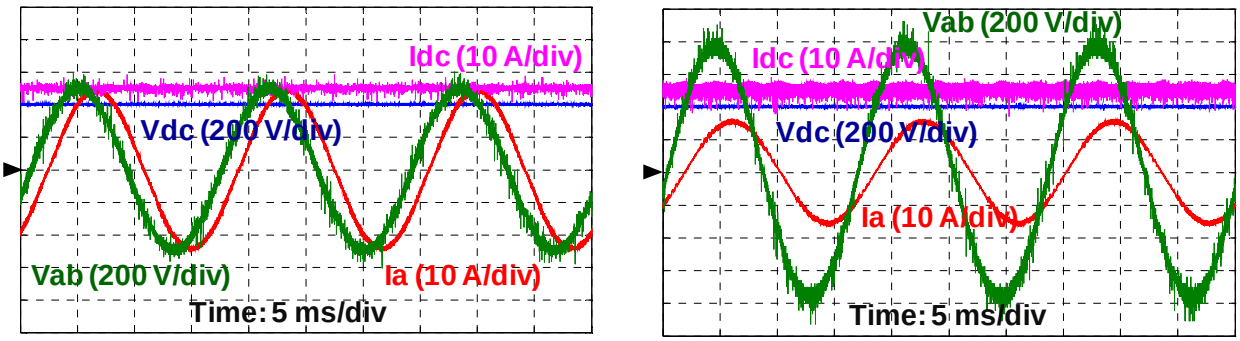


Figure 5-39. All-SiC three-phase CSR waveforms at 10 kW.

For the front-end stage of power supply systems, the input voltage range should be wide enough to meet the grid voltage levels in different countries. Based on the requirement of high voltage DC distribution architecture, the output voltage should keep 400 V_{dc} with different input voltage levels. For three-phase CSR, the output DC voltage is limited by $V_{dc} < \frac{\sqrt{3}}{2} V_m$, where V_m is the peak value of input line-to-line voltage. With this tolpology, the lowest value of input line-to-line voltage is 330 V_{ac} in order to achieve 400 V_{dc} output. With 1200 V voltage rating power devices, the converter cannot be operated with the input line-to-line voltage higher than 800 V_{ac}. However, considering the voltage overshoot during a swithing transient, the input voltage should be much lower than this value. The voltage overshoot depends on the switching speed and the parasitics in the circuit.Figure 5-40 shows the waveforms of all-SiC three-phase CSR at 10 kW output power with various input voltages.



(a) 350 V_{ac} line-to-line input voltage (b) 550 V_{ac} line-to-line input voltage

Figure 5-40. All-SiC three-phase CSR waveforms at 10 kW with various input voltages.

5.6 Summary

In this chapter,the all-SiC, liquid cooled three-phase current source rectifier is designed and developed for 400 V_{dc} architecture data center power supply systems. SiC MOSFETs and SBDs were selected for the power switches. The advantages of SiC power devices on the design of high efficiency converters are shown by comparing with traditional Si based converters, according to the paper-based design and loss calculation. Furthermore, the design methods of front-end rectifier in data center power supply systems are provided, including the methods of topology selection, modulation scheme selection, device paralleling number and switching frequency selection, filter design and loss minimization.

This current source rectifier, using four paralleled SiC MOSFETs and two SiC SBDs, with 480 $V_{ac,rms}$line-to-line input voltage, 400 V_{dc} output voltage, and 28 kHz switching frequency, achieves 98.54% efficiency and 98.55% peak efficiency in the test, including the auxiliary circuit loss on self-developed controller. Experimental results verify the functions of the designed high efficiency converter.

Chapter 6 Paralleled Current Source Rectifiers for Data Center Power Supplies

In this chapter, the front-end rectifier is formedby paralleling three current source rectifiers, described in Charter 5 for a 400 V_{dc} architecture data center power supply system. Section 6.1 gives the overview of front-end rectifier system based on three paralleled CSRs. In 6.2, the control strategy of paralleled CSRs to realize output current balancing and hot-swap is studied and implemented. In 6.3, the circulating in paralleled CSRs is discussed. A 19 kW front-end rectifier system by three paralleled CSRs with (2+1) redundancy is implemented and tested in 6.4.Finally, conclusions are given in 6.5.

6.1 Paralleled Three-Phase Current Source Front-End Rectifiers

Chapter 5 develops a three-phase current source rectifier (CSR), with 480 V_{ac} input line-to-line voltage and 400 V_{dc} output voltage, as the front-end rectifier in data center power supplies based on high voltage DC distribution architecture. The single converter will be not enough for power supply system.It is a popular choice to parallel power converters to achieve higher output power. Compared to a single high power converter, paralleled converters will bring system redundancy through (N + 1) configuration for power supply systems, as well as easy implementation of converter power management.

To implement the front-end stage using three-phase CSR, several CSRs should be operated in parallel. The paralleled CSRs are connected directly in AC side to grid with 480 V_{ac} line-to-line voltage. They provide common output, with 400 V_{dc}, for the second power conversion stage in the system.However, related issues are waiting to be solved in paralleled CSRs. For example,

among converter modules, the schemes of output power sharing and circulating current limitation need to be provided.Several publications study the paralleled three-phase voltage source converters [146]-[150]. References [151]-[153] deal with the operation of paralleled current source converters. But some features of the converter, required by power supply systems such as system redundancy and hot-swap, are not discussed and realized.

6.2 Paralleled Current Source Rectifiers with Current Balancing and Hot-Swap

6.2.1 Master-Slave Control for Paralleled Current Source Rectifiers

For the paralleled converters, current sharing is necessary, because if one converter outputs most of the power, it will be over heated and its efficiency and lifetime will reduce. There are several control schemes to achieve equal current distribution among paralleled converter, such as master-slave control (MSC)[154]-[156], central-limit control (CLC)[157], circular chain control (3C) [158], and current sharing scheme based on droop method[159]. MSC is simple, stable, and has fast dynamic response. MSC has been widely used as the current sharing scheme in UPS systems which are based on paralleled voltage source converters or DC-DC converters. In this work, MSC will be used to distribute output current of paralleled CSRs.

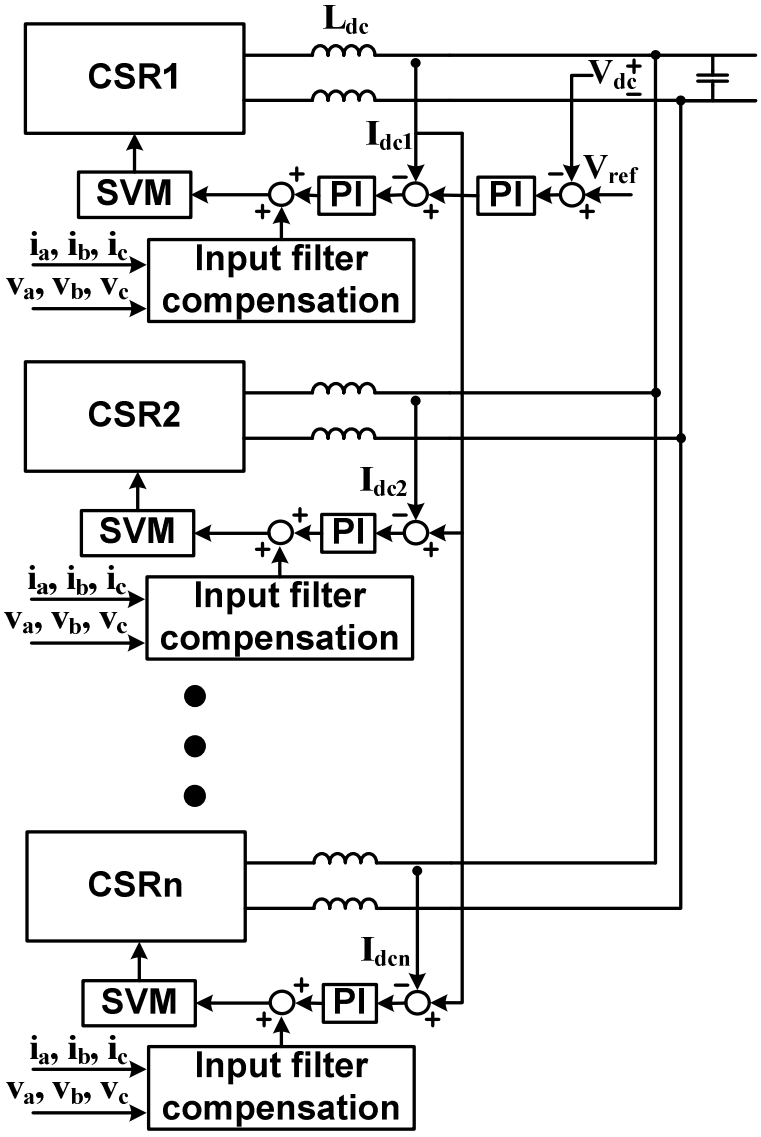


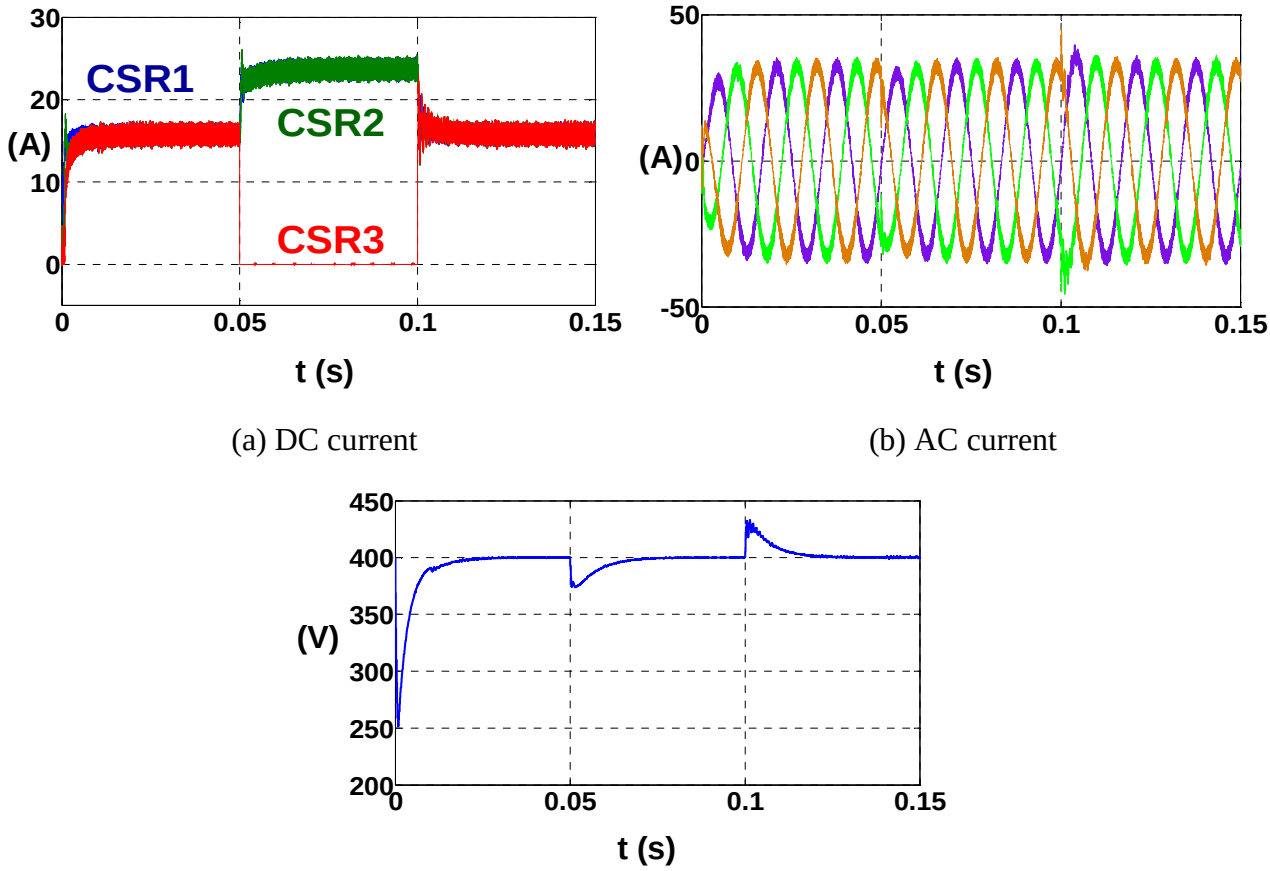
Figure 6-1. Master-slave control for paralleled CSRs.

Based on the single CSR control algorithm in Figure 5-13 for 400 V_{dc} distributed power supply system, the proposed MSC for paralleled three-phase CSRs is shown in Figure 6-1. One of the rectifiers operates as the master converter, CSR1 in Figure 6-1. The master converter has both inner DC current control loop, I_{dc} loop, and the outer DC voltage control loop, V_{dc} loop, which is the same with single CSR control algorithm shown in Figure 5-13. Other rectifiers operate as current followers (slaves), CSR2 to CSRn in Figure 6-1. The slave converters have

only I_{dc} loop and their DC output currents follow the DC current of master rectifier.

In the paralleled converters for power supply system, each converter module has its own controller. One method for the slave rectifiers to follow the master rectifier output current is using the output of master converter V_{dc} loop as the references of their own I_{dc} loops. This method requires the slave converters to obtain their DC current values from the controller of the master converter, and a communication system is needed for the I_{dc}reference values sending or receiving among paralleled converters. The development of communication system will increase the cost and complexity of the system. In this dissertation, the slave rectifiers obtain their I_{dc} references directly from the master rectifier DC current sensor through the shield signal cables. The issue of using this method is that the noise in the DC current sensor output signals may impact the control effects. After passing through a low-pass filter, the high frequency noise will not be send into the controller of slaves. By calculating the line period average value of received the master rectifier's DC current as the reference, the slave rectifiers can follow the output current of master rectifier very well. The results will be shown in next section. Finally, the master converter V_{dc} control loop output only provides a reference of its I_{dc} control loop, and the output current of the master converter provides a reference of the slave converter's I_{dc} control loop. Each rectifier module has its own input filter compensation unit.

The output currents will be balanced when each slave converter DC current follows the master converter DC current. Meanwhile,hot-swap capability can be realized using MSC, which means the rectifier module can be removed from the system or added into the system without shutting down the system and keeping other converter modules running.



(a) DC current

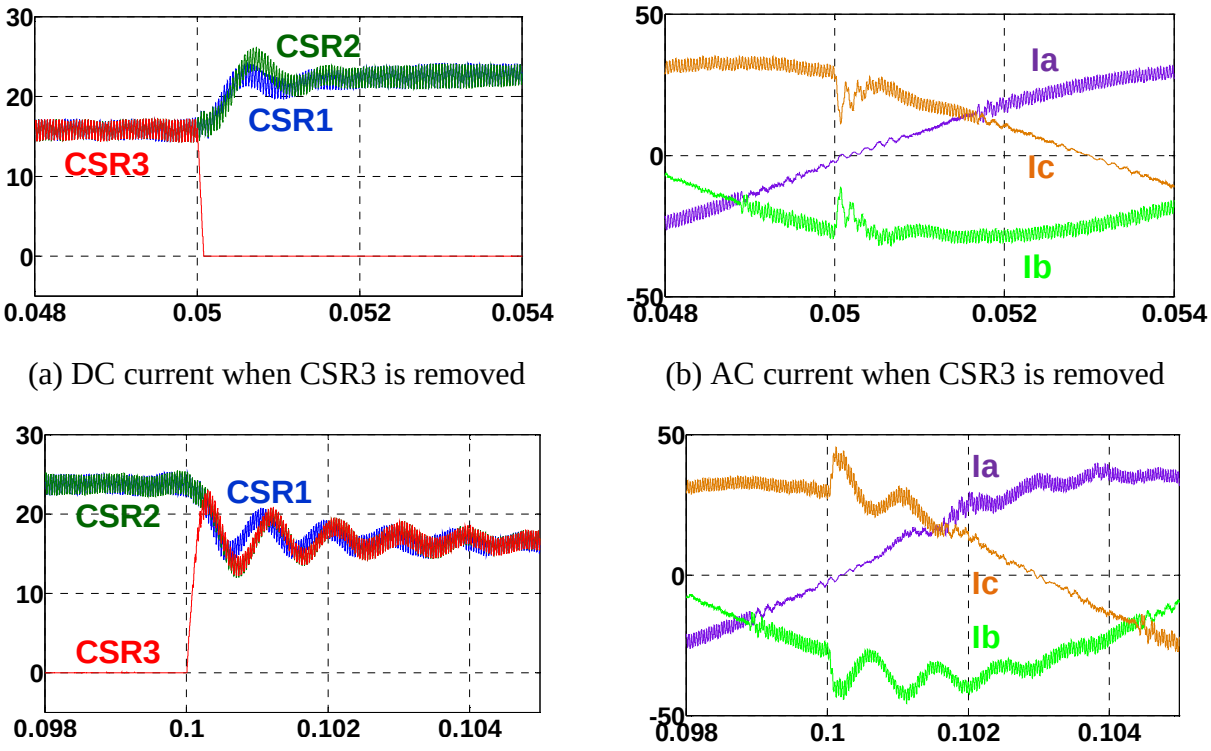
(b) AC current

(c) DC voltage

Figure 6-2. Simulation results of paralleled CSRs hot-swap using MSC.

Figure 6-2 shows the simulation results of three paralleled CSRs using MSC control and realizing hot-swap in Matlab Simulink. The CSR1 is the master converter, CSR2 and CSR3 are slaves. The input voltage is 480 V_{ac} line-to-line voltage, and the output voltage is 400 V_{dc}. The power of the system is 19 kW and the DC current of the system is 47.5 A. At the beginning, three CSRs provide full power to the load, and each rectifier outputs 15.83 A current. At t = 0.05 s in simulation, the CSR3 is removed from the system by disconnecting its AC side from the AC source. After that, only CSR1 and CSR2 provide full power to the load, each of them outputs 23.75 A DC current. The transient causes the output voltage drop to 370 V_{dc}. The DC voltage

will increase back to 400 V_{dc} due to the V_{dc} control loop in master rectifier. The system input current will have the drop too during this transient. At t = 0.1 s, the CSR3 is added into the system turning on its control loop and generating PWM signals. After that each of the three rectifiers outputs 15.83 A DC current again. During this transient, both input current and output voltage of the system will have overshoot. The peak of the DC voltage overshoot is 430 V_{dc}.



(a) DC current when CSR3 is removed

(b) AC current when CSR3 is removed

(c)DC current when CSR3 is added

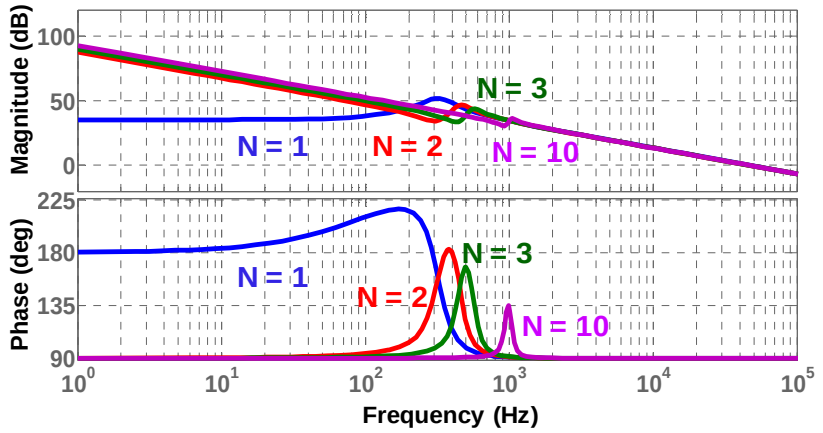
(d) AC current when CSR3 is added

Figure 6-3. Simulation results of hot-swap transients.

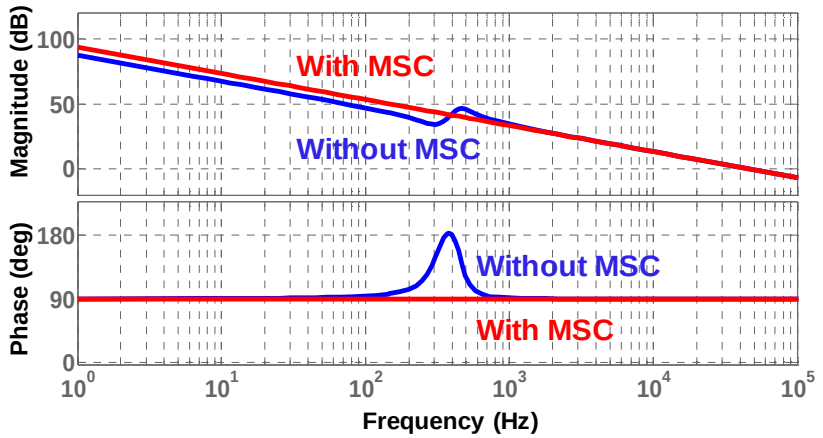
Figure 6-3 shows each rectifier DC current and system AC current at the transients of t = 0.05 s and t = 0.1 s in Figure 6-2. When CSR3 is removed from the system, the system output voltage reduces and the V_{dc} control loop in master converter increases the DC current reference value to keep 400 V_{dc} output voltage. With increased reference value, the master rectifier's DC

current is increased by its own I_{dc} control loop. Then the slave recitifer CSR2 increases its DC current because the reference of its I_{dc} control loop, the DC current of CSR1, is increased. As a result, the full load is supported by only CSR1 and CSR2, as shown in Figure 6-2(a). The change of DC currents causes distortation in AC current during this transient, shown in Figure 6-2(b).Similarly, when CSR3 is added into the system, the V_{dc} overshoot reduces the reference value of DC current of master converter. With the reduction of I_{dc} of CSR1, CSR2 reduces its output current too. The DC currents of both CSR2 and CSR3 equal the CSR1's output current, shown inFigure 6-3(c). The AC current will be distorted too during this transient, shown in Figure 6-3(d).

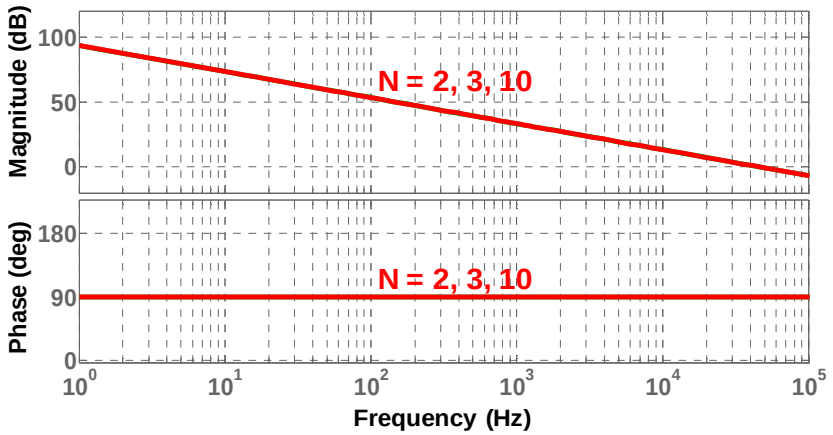
Figure 6-4 shows the d-channel control to DC current transfer function ($\tilde{i}_{dc} / \tilde{d}_d$) of paralleled three-phase current source rectifiers. N is the paralleling number. From Figure 6-4(a), the paralleled rectifiers have a pole at the DC origin due to the zero-sequence interaction when they have independent DC current control loop. The resonant frequency increases with more paralleled CSRs. Figure 6-4(b) compares $\tilde{i}_{dc} / \tilde{d}_d$ of slave rectifier in two paralleled CSRs with and without MSC. From Figure 6-4(b), the DC current loop of slave rectifier can be designed to be very fast to achieve fast dynamic response because it is a first-order system. From Figure 6-4(c), the d-channel control to DC current transfer function of slave rectifier will not change with paralleling number. This means the controller can be designed individually and paralleling number does not need to be considered. Therefore, modular design is allowed.



(a) Without master-slave control, N = 1, 2, 3, 10



(b)N = 2

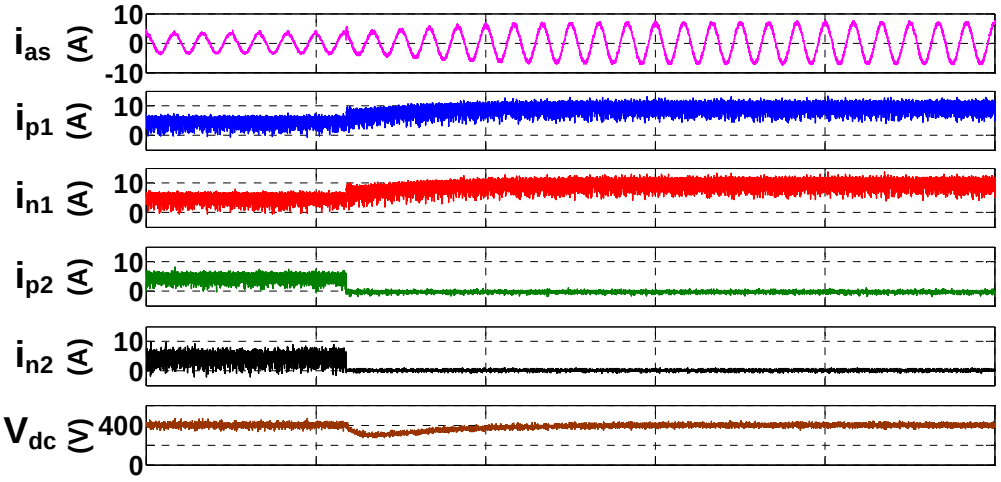


(c) With master-slave control, N = 2, 3, 10

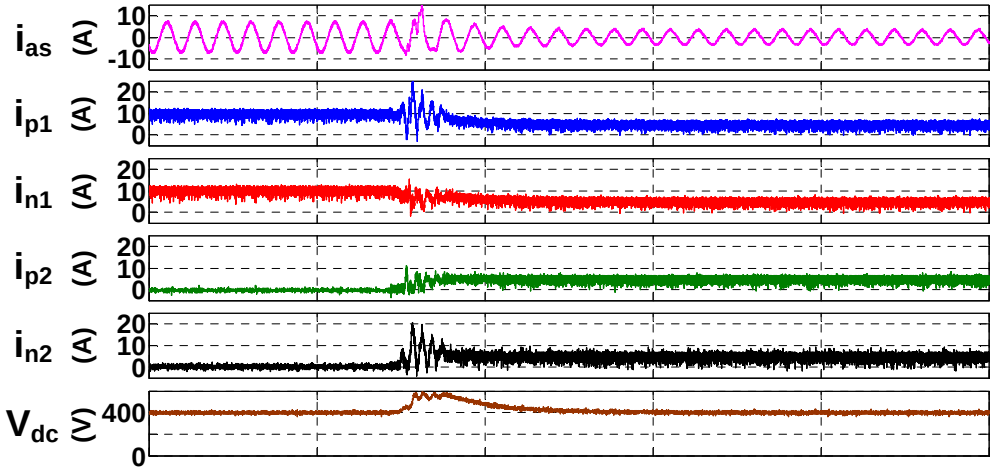
Figure 6-4. D-channel control to DC current transfer function of paralleled three-phase current source rectifiers.

6.2.2 Experimental Verification

This section shows the experimental results of two paralleled CSRs and three paralleled CSRs, using the proposed master-slave control. The CSR prototype is developed in section 5.5. The system input voltage is 480 V_{ac} line-to-line voltage and output voltage is 400 V_{dc}. The load is resistors in load bank described in Chapter 5.



(a) CSR3 is removed from the system



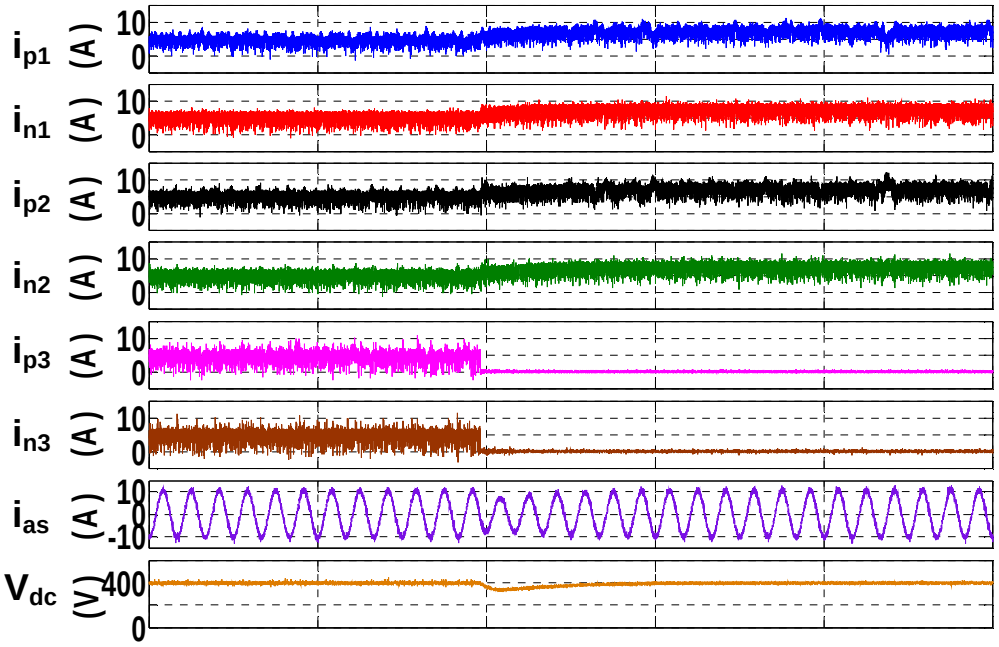
(b) CSR3 is added into the system

Figure 6-5. Hot-swap test results in two paralleled CSRs. (Time: 100 ms/div)

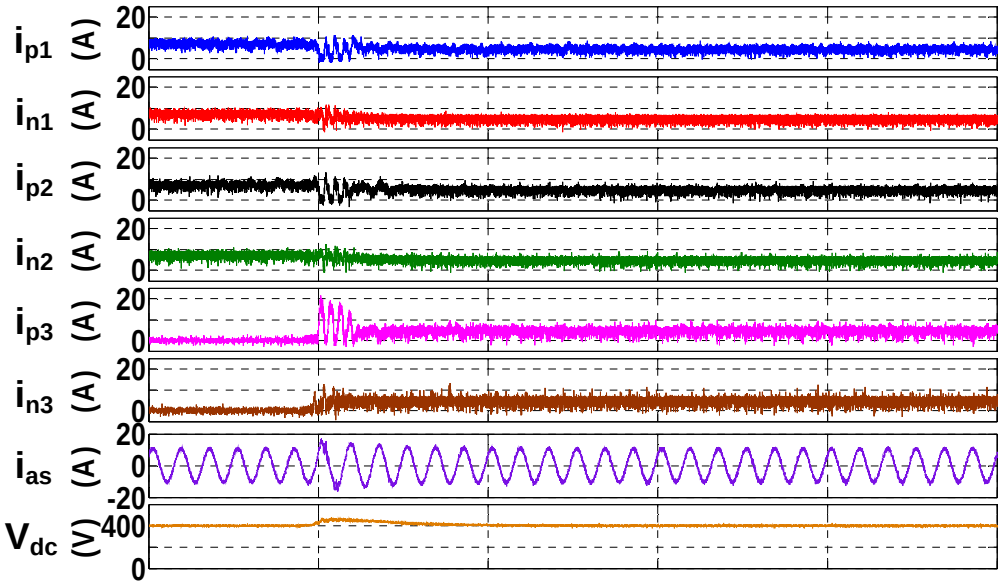
Figure 6-5 shows the hot-swap test results of two paralleled CSRs. In this chapter, i_{pi} (i = 1, 2, 3, …) is the positive DC-link current of CSRi in paralleled CSRs system, and i_{ni} (i = 1, 2, 3, …) is the negative DC-link current of CSRi. The CSR1 is the master converter and the CSR2 is the slave. Two rectifiers provide 5 A DC current each at the beginning in Figure 6-5(a). When CSR2 is removed, the DC current of CSR1 is increased to 10 A. The lowest value of V_{dc} during this transient is 300 V_{dc}. Before CSR2 is added into the system in Figure 6-5(b), CSR1 outputs 10 A DC current. The DC current of CSR1 reduces to 5 A and is followed by CSR2 when adding CSR2 into the system. The peak value of V_{dc} during this transient is 580 V_{dc}.

Figure 6-6 shows the hot-swap test results of two paralleled CSRs. CSR3 is removed and added in Figure 6-6(a) and (b) respectively. Before CSR3 is removed from the system, each rectifier outputs 5 A current in Figure 6-6(a). After that, CSR1 increase the output to 7.5 A and CSR2 follows it to output 7.5 A DC current in order to keep 400 V_{dc} output voltage. The output voltage lowest value is 340 V_{dc} during this transient. In Figure 6-6(b), after adding the CSR3, CSR1 and CSR2 reduce their output to 5 A (CSR2 follows CSR1). Since CSR3 follows CSR1, its output currentis 5 A too. The output voltage is controlled to 400 V_{dc} after a transient of overshoot with 430 V_{dc} peak value.

In the$n$ paralleled CSRs system, if there is no DC voltage control, the DC voltage will drop to (n-1)/n×V_{dc} when one CSR is removed (V_{dc} is the regular output voltage). And the DC voltage will increased to (n+1)/n ×V_{dc} when one CSR is added. The variation of output voltage during hot-swap transient will be reduced when the paralleling number n increases, using this MSC.



(a) CSR3 is removed from the system



(b) CSR3 is added into the system

Figure 6-6. Hot-swap test results in three paralleled CSRs. (Time: 100 ms/div)

6.3 A 19 kW Front-End Rectifier System for Data Center Power Supplies

6.3.1 Three Paralleled Current Source Rectifiers Prototype

A 19 kW front-end rectifier system based on three paralleled CSRs with liquid cooling will be developed for data center power supplies based on high voltage DC distribution architecture.The paralleled CSRs are directly connected on both AC and DC sides. They share one AC inductor and one DC capacitor.Each CSR holds its own AC capacitor as the voltage source in the input side and a split DC inductor as the current source in the output side. ORing diode in DC-link is used to isolate faults from DC side, and AC side fault isolation is realized by open contactor in three-phase input. Three paralleled CSRs will bring system redundancy through (2 + 1) configuration, which meanstwo CSRs can support 19 kW output power when the third one is removed from the system due to the failure. Each CSR is developed as described in Chapter 5.5, shown in Figure 5-38. The front-end rectifier system structure is shown inFigure 6-7.

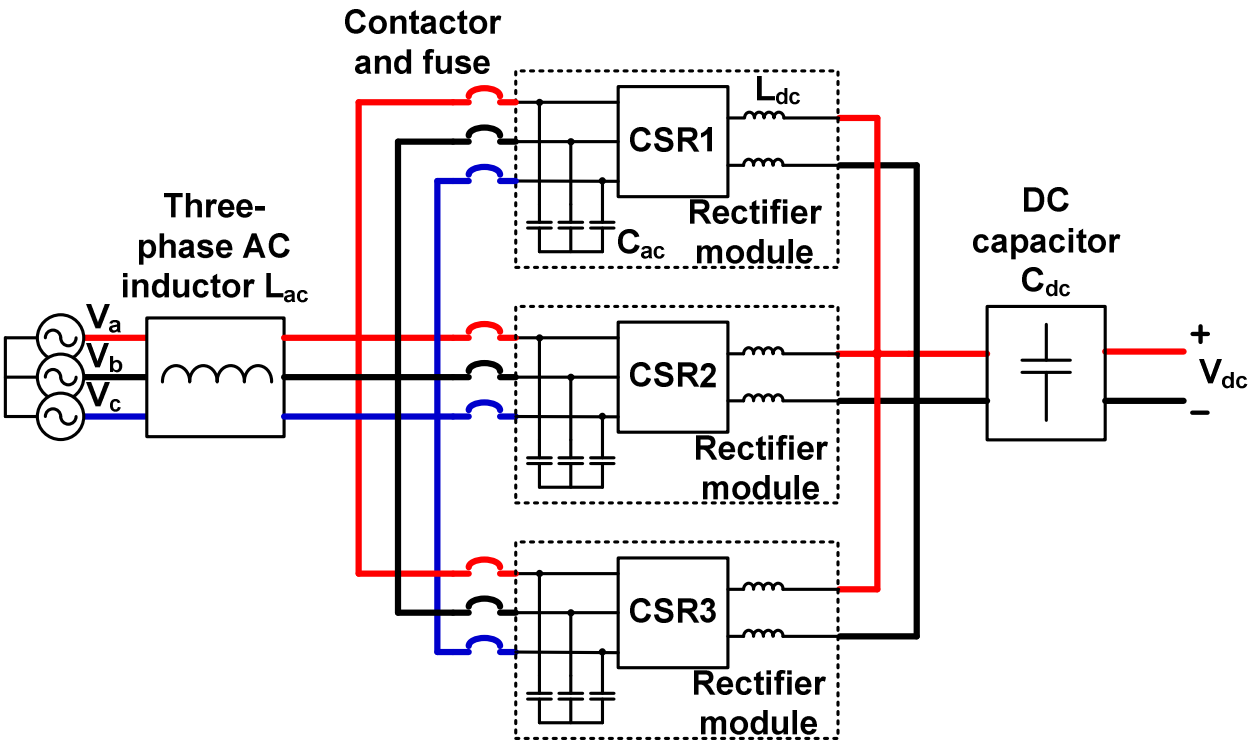
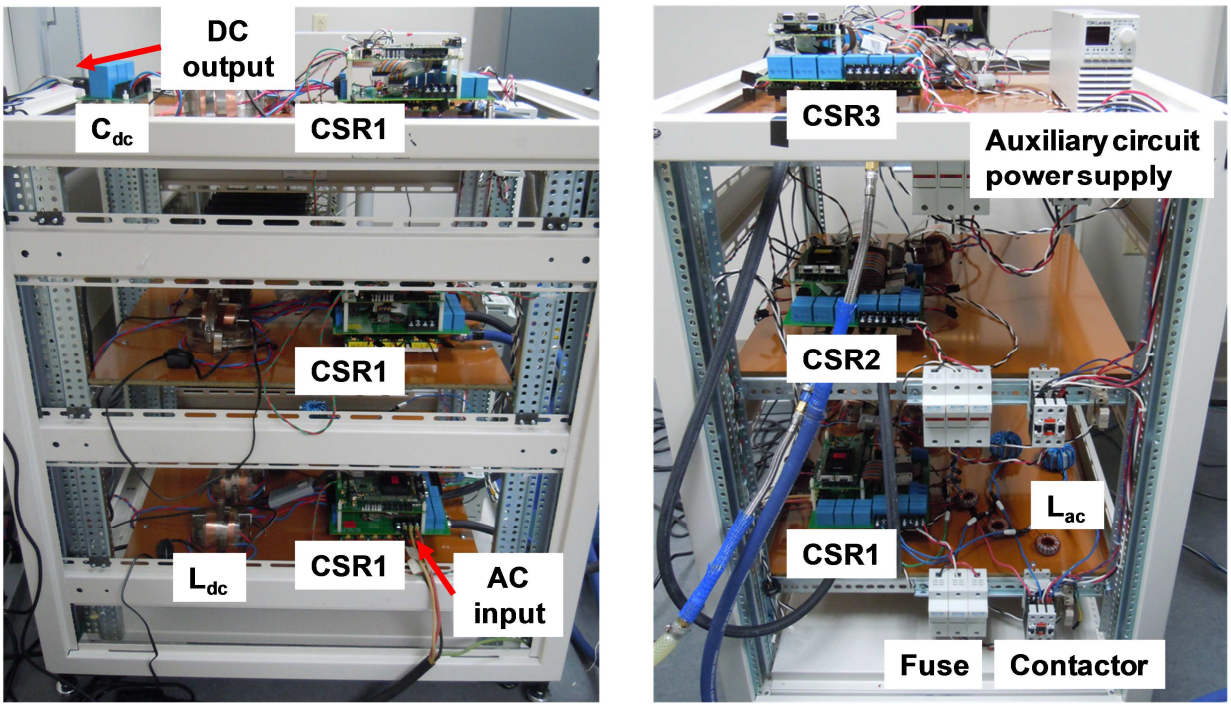


Figure 6-7. 19 kW paralleled current source rectifier system.

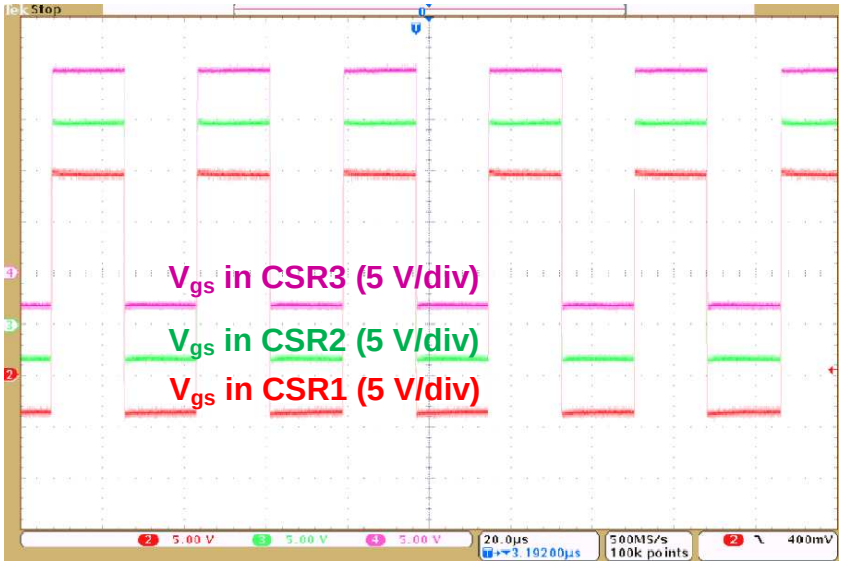
The prototype of front-end rectifier system is shown in Figure 6-8. There is the fuse and contactor in series in AC side of each CSR. The contactor is turned on when connected to 110 V_{ac}, and is turned off when disconnected to 100 V_{ac}. The relay is used to connect or disconnect the contactor from 100 V_{ac}.The control signal is 12 V_{dc} provided by interface board of each rectifier. Auxiliary circuit power supply provides the power to DSP boards, interface boards (including gate drivers and sensors), and relays in three CSRs.



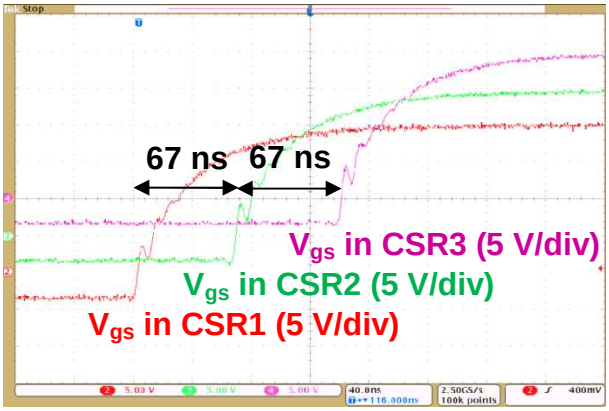
(a) Side view (b) Front view

Figure 6-8. 19 kW front-end rectifier prototype.

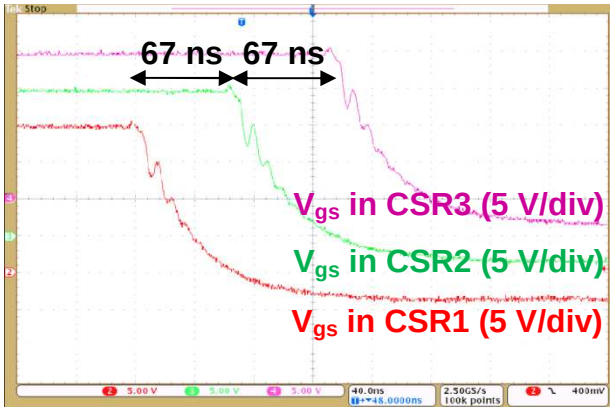
For the paralleling operation of conveters, the controllers need to be synchronized to provide the synchronized PWM signals. If the PWM signals are not synchronized, random phase-shift will exist and system cannot work normallu due to large circulating current. The PWM signals of three CSRs are synchronized by connecting their DSP ePWM module in series using shield cables. The ePWM module in master CSR sends the synchronized to the ePWM modules in slave CSRs. The delay on synchronization cable between two conveters is 67 ns, which is small enough for the converter paralleling with 36 μs switching period. The synchronized MOSFET gate signals of three paralleled CSRs and the delay are shown in Figure 6-9, where CSR1 is the master rectifier.



(a) MOSFETs' gate signals (Time: 20 µs/div)



(b) Turn-on (Time: 40 ns/div)



(c) Turn-off (Time: 40 ns/div)

Figure 6-9.Synchronized MOSFET gate signals in paralleled CSRs.

In order to use the master-slave control in section 6.2, the DC-link current of master coverter needs to be sent to the slaves. The DC current sensor output is directly connected to the input of DSP AD channels of the slave rectifiers using the shield cables. Since each rectifier could be the master converter, the DC current of each CSR will be sent to the other two CSRs in the system, shown in Figure 6-10.

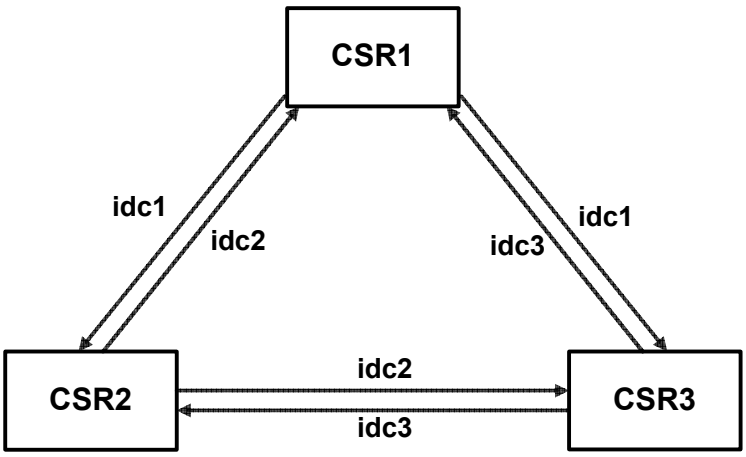


Figure 6-10. Shared DC current in paralleled CSRs.

6.3.2 Experimental Results

The test setup of data center power supply front-end rectifier stage based on three paralleled CSRs is shown in Figure 6-11. The input power of the system is from the grid through a three-phase high power variac. The load in the test is the resistor in load bank described in Chapter 5. The chiller provides 25 °C liquid (50% ethylene glycol, 50% water) with 1.5 GPM (5.68 LPM) flow rate for the cooling of CSRs. The power analyzer PZ4000 is used for the power measurement and efficiency calculation.

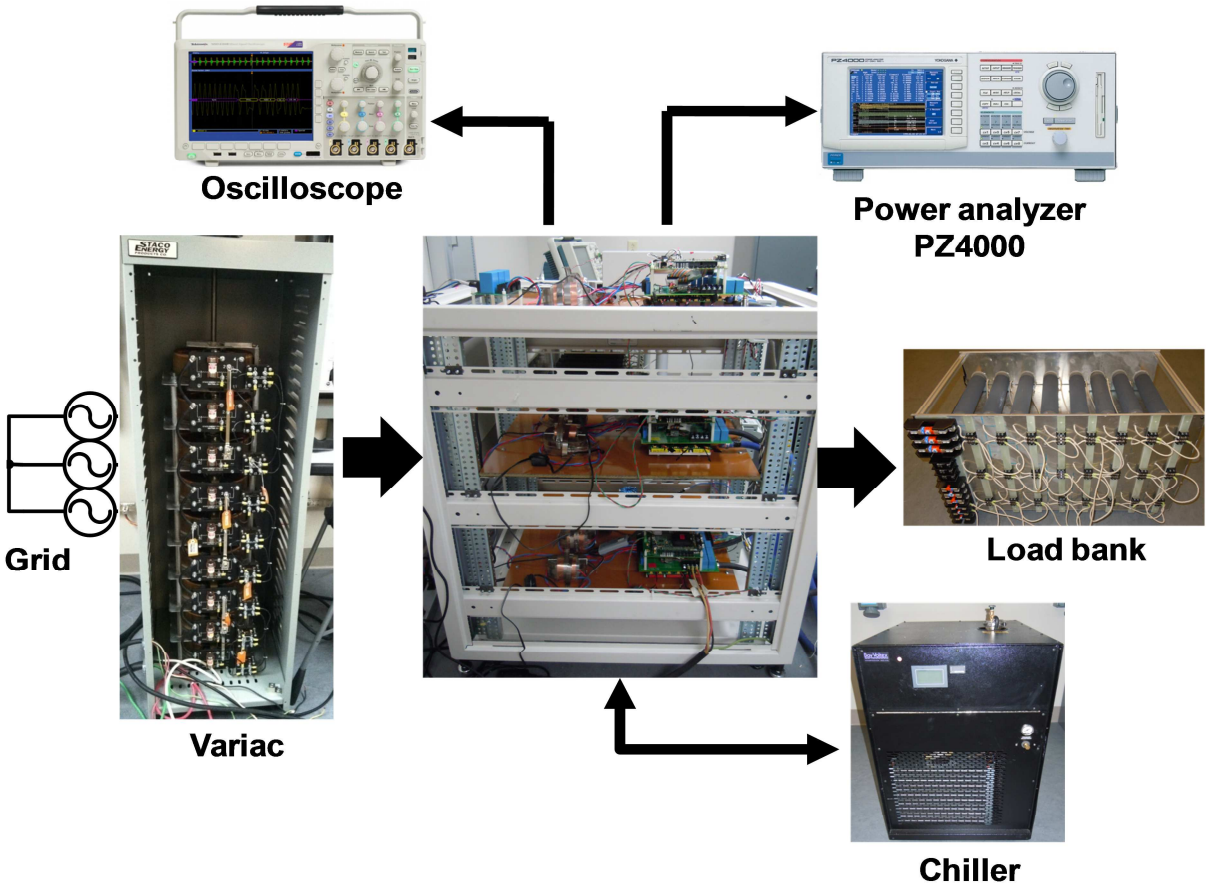


Figure 6-11. Three paralleled CSRs test setup.

Figure 6-12 shows the waveforms of the three paralleled CSRs at 19 kW output power, with 480 V_{ac} input line-to-line voltage and 400 V_{dc} output voltage. The system output DC current is 47.5 A. Each three-phase CSR provides 15.83 A output current.

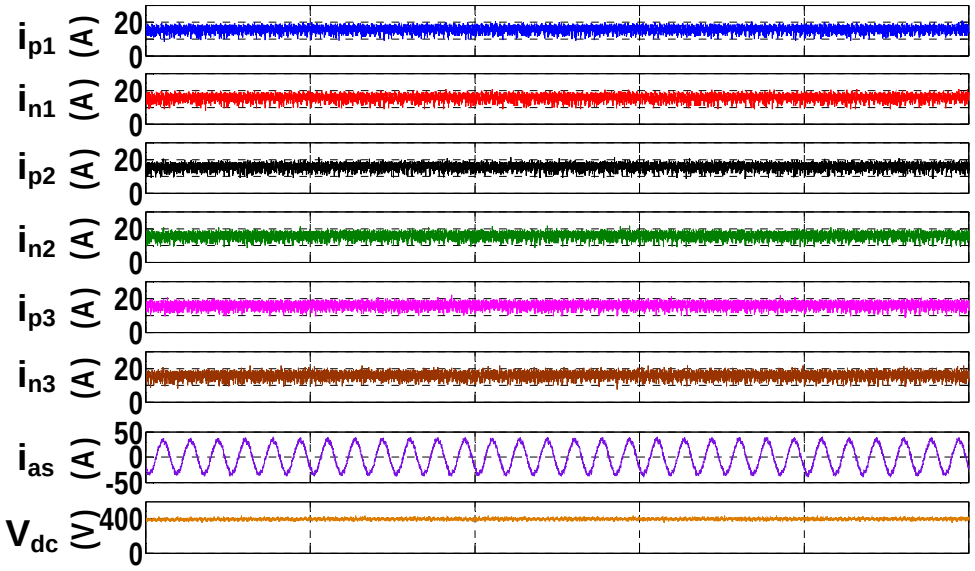


Figure 6-12. Waveforms of three paralleled CSRs at 19 kW. (Time: 100 ms/div)

The efficiency curve of front-end rectifier stage based on three paralleled CSRs is shown inFigure 6-13. The efficiency is measured by PZ4000 power analyzer. The input and output power are calculated by (5-3) and (5-4) respectively. The voltages are measured by the voltage sensor in the measurement module 253751 in PZ4000. The currents are measured by a LEM current transducer IT 60-S, current amplifier IST ULTRASTAB, and current shunt resistor in measurement module 253751. The converter efficiency is calculated by (5-5). The auxiliary circuit loss $P_{aux}$is 45 W, which is the measured result of the output power of auxiliary circuit power supply, shown in Figure 6-8. The efficiency values at different output power levels are listed in Table 6-1.The full load efficiency of the front-end rectifier system is 98.12%, and the peak efficiency is 98.25% at 12 kW output power.

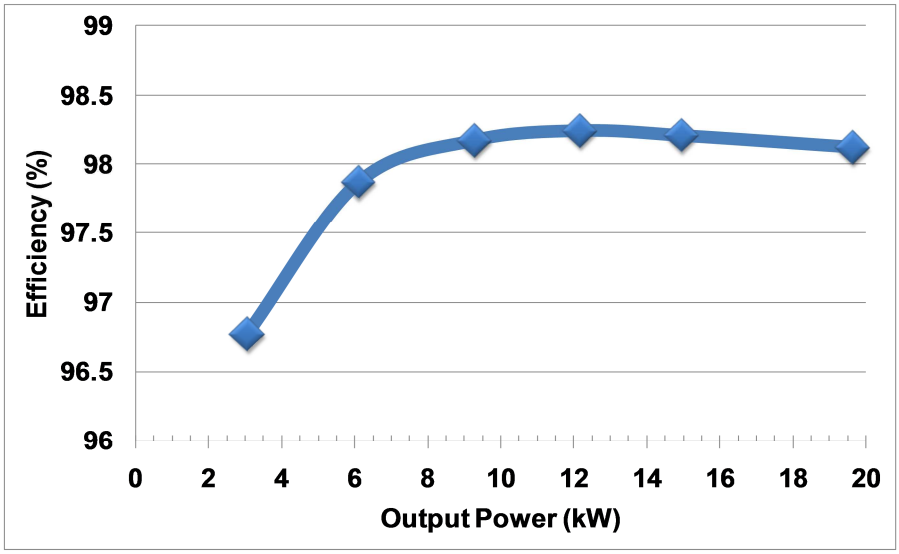


Figure 6-13. Efficiency curve of front-end rectifier stage in data center power supplies.

Table 6-1. Efficiency values of front-end rectifier stage in data center power supplies at different output power levels

Output power	CSR efficiency
3 kW	96.77%
6 kW	97.87%
9 kW	98.17%
12 kW	98.25%
15 kW	98.21%
19 kW	98.12%

The system efficiency is less than single rectifier because the losses on contactor, fuse, and overvoltage protection circuit, which are not included in single rectifier efficiency measurement, are all included in the system efficiency measurement. The auxiliary circuit loss takes a large part of total loss from the experiments. If auxiliary circuit loss is not considered, the system full load efficiency and peak efficiency will be 98.35% and 98.62%, respectively. in the future, the

minimization of auxiliary circuit loss should be researched.

In the tests, the AC voltage is obtained from the grid. The grid does not provide AC voltage without harmonics. The spectrum of AC voltage used in the test is shown in Figure 6-14. From Figure 6-14, there is large 5^{th} harmonic component. As a result, the AC side current THD is 6.8% at full load. The better control is expected for three-phase current source rectifier to reduce AC current THD with distorted AC voltages.

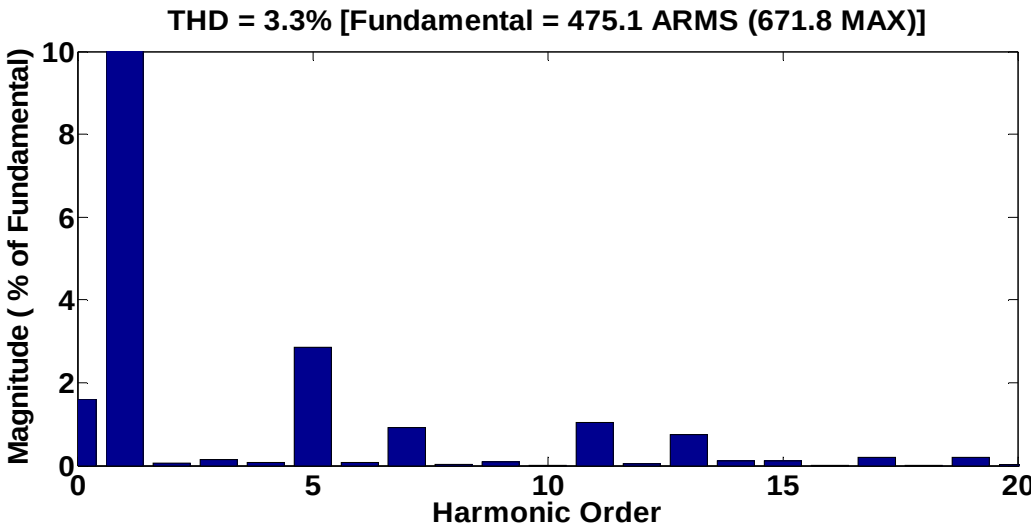


Figure 6-14. Spectrum of AC voltage in the test.

6.4 Summary

The converter paralleling is widely used for power supply system, because it can achieve high output power and system redundancy. This chapter develops the paralleled current source rectifiers (CSRs) as the front-end rectifier for data center power supplies using 400 V_{dc} bus. The related issues of paralleled CSRs are studied, including output current sharing control and circulating current limitation.

The master-slave control (MSC) is developed for paralleled CSRs to achieve output current

balance. By using the master CSR output current as the reference for slaves' DC current control loop, the balanced output current among paralleled CSRs is achieved. The sysem output voltage is controlled by a voltage control loop in master CSR. Hot-swap can be realized using this MSC. The single CSR module can be removed or added, while other CSRs keep running. During these transients, the current balance and system output power can be adjusted automatically.

An all-SiC 19 kW three-phase front-end rectifier from 480 V_{ac} to 400 V_{dc} is developed, using three paralleled CSRs based on SiC MOSFETs and Schottky diodes. The full load efficiency of the system can achieve 98.12%.

Chapter 7 Conclusion and Future Work

The conclusions of the dissertation based on the works in Chapter 3~6 will be summarized in this chapter. The related future works will be proposed too.

7.1 Conclusion

In this disseratation, the methodology of high efficiency three-phase converter designusing SiC power devices is presented. The related issues including power device evaluation, power module layout, parasitic impacts, single converter loss minimization, and high efficiency paralleled three-phase converters, are all discussed and analyzed.The following conclusions are drawn:

First, the application of SiC power devices helps converters to achieve high efficiency even at high temperatures, atwhich Si devices cannot be operated. With temperature increasing, the conduction loss of normally-on SiC JFET increases but its switching loss decreases slightly. With the help of SiC JFET and Schottky diode, a three-phase voltage source inverter peak efficiency can achieve 98.5% with 10 kHz switching frequency 95 °C coolant.

Second, the dissertation proposes a device switching test circuit based on current source topology. The circuit can simulate two different current commutation processes, the current commutation between active switches and between one active switch and one diode, in current source converters. The circuit can be used to evaluate switching performance and calculate switching loss of power devices which will be used in current source converters.

Third, the impacts of parasitics on power devices' switching performance and switching loss under fast switching conditions are studied in this dissertation. In voltage source converters, the

parasitic inductances in the gate loop and DC buses may cause the device false turn-on during the other device switching transient in a phase-leg and cause phase-leg shoot-through. The minimization of these inductances in a voltage source power module and converter design is necessary to keep the fast switching and low switching loss of SiC devices. In current source converters, the parasitic capacitances from device junction capacitance and the capacitance between power buses contribute to the power device switching loss. Different capacitances cause additional loss for different current commutation processes.The dissertation proposes an inductive snubber based on an inductor and a diode for current source converters, to reduce device switching loss. With different parasitic capacitance, there is an optimized inductor value in snuber circuit at each voltage level to minimize device switching loss.

Fouth, the dissertation provides the methodology and procedures of high efficiency three-phase current source rectifier design. The procedures include topology comparison, power device measurement and loss calculation, device paralleling and switching frequency selection, filter design, low loss control algorithm and modulation scheme. The dissertation develops a 7.5 kW all-SiC three-phase current source rectifier with 480 V_{ac} input and 400 V_{dc} output voltages as the front-end stage for data center power supplies. The 98.54% full load efficiency is achieved.

In the end, the master-slave control is developed for paralleled three-phase current source rectifiers. By sharing the DC current of master rectifier to slave rectifiers, the balanced output currents can be achieved. In addition, with this master-slave control, when a rectifier is removed or added in to the system, other converter can increase or decrease their outputs automatically to provide the power to the load without communication system. The dissertation develops a 19 kW front-end rectifier system for data center supplies based on paralleled current source rectifiers. The system has the features of (2+1) redundancy and hot-swap using the master-slave control.

7.2 Major Contributions

First, the dissertation proposes a circuit to evaluate switching performance and calculate switching loss of power devices in three-phase current source converters.

Second, the dissertation analyzes the impact of parasitic inductance on phase-leg shoot-through in three-phase voltage source converters and the impact of parasitic capacitance on devices' losses in three-phase current source converters. In addition, this dissertation analyzes the performance of an inductive snubber, identifies the relationship between snubber inductance and switching loss.

Third, the dissertation proposes a design methodology of high efficiency three-phase converters, demonstrates the benefits of SiC devices in high efficiency applications, and develops a 7.5 kW all-SiC three-phase CSR for data center power supplies with 98.54% full load efficiency.

Finally, the dissertation proposes a master-slave control for paralleled three-phase current source rectifiers to achieve balanced outputs and converter hot-swap, designs and develops a 19 kW, 98.1% efficiency front-end rectifier system with (2+1) redundancy using SiC devices for data center power supplies.

7.3 Future Work

Based on the works presented in the dissertation, several further studies could be done in the future:

(1) The active solustions for phase-leg shoot-through issue in SiC power devices based three-phase voltage source converters should be researched.

(2) The multi-chip power modules based on current source topology with better parasitic

controlshould be designed and developed for three-phase current source converters, to achieve both high efficiency and high power density. And the methodology of packaging technique to reduce parasitics for SiC based power modules should be studied.

(3) The conduction loss of power devices is the dominant part of losses in CSCs due to the series of two deives. The low loss SiC device with reverse blocking characteristic should be developed to further reduce the device switching loss. Moreover, the replacement of series SiC Schottky diodes in switching element in CSCs by low conduction loss SiC MOSFETs should be researched to reduce conduction loss.

(4) The combination of other loss reduction methods with SiC devices can obtain extra efficiency for SiC based converters should be researched. The method of reducing auxiliary circuit loss of SiC based three-phase converter and SiC MOSFET/JFET gate drive optimization need to be researched to futher increase the converer efficiency.

(5) The control method and operation performance of three-phase current source rectifier for power supplies under poor power quality conditions should be researched. For example, the reduction of input current THD under distorted AC voltage conditions should be studied, the converter control with input voltage sag/swell or lose phases should be investigated too.

(6) In power supply systems, many power converters more than three will be operated in paralleled. The issues related to the large number of paralleled CSRs should be studied. For example, the synchronization signal, the shared DC current of master rectifier when using master-slave control should be considered.

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