To the Graduate Council:

I am submitting herewith a dissertation written by Hui Zhang entitled “Electro-Thermal Modeling of SiC Power Electronic Systems.” I have examined the final electronics copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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(Original signatures are on file with official student records.)
Electro-Thermal Modeling
of SiC Power Electronic Systems

A Dissertation
Presented for the
Doctor of Philosophy Degree
The University of Tennessee, Knoxville

Hui Zhang
December 2007
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Dedication

This dissertation is dedicated to my husband as well as a fellow colleague, Haiwen. Thanks for his sincere love and great patience throughout the years. It is also dedicated to my parents, who have supported and encouraged me unconditionally all the times, and my little lovely son, Vincent, for the happiness that he brings into my life.
Acknowledgments

I would like to thank many people for their kind help during my study and research so that I could finish my dissertation.

First and foremost, I sincerely appreciate my advisor, Dr. Leon M. Tolbert, for his instruction, his supervision, and his persistent support.

Many thanks to my committee members, Dr. Jack S. Lawler, Dr. Syed Islam, and Dr. Philip D. Rack, for being on my committee, reading my dissertation and providing invaluable suggestions and comments.

Special thanks to Dr. Burak Ozpineci and Madhu Sudhan Chinthavali at Oak Ridge National Laboratory for their valuable discussion, advice and help.

Finally, I would like to thank all the people in the Power Engineering Laboratory at The University of Tennessee, who create a friendly working environment.
Abstract

As the development of Silicon (Si) semiconductor technology slows down due to its material limitations, more and more attention is being paid to wide bandgap material based semiconductor technology. Silicon Carbide (SiC) has been widely recognized as the material for next generation power electronic devices. However, a great deal of work needs to be done before SiC power devices can be widely applied. This dissertation addresses this need and has conducted research on the modeling of SiC power electronic system. More specifically, a method for system modeling of a SiC power system based on basic physics and device tests is presented here. It includes temperature-dependent single device models specified for system-level modeling, power loss models for power converters, and thermal models for cooling system. The method is verified by experimental results. Furthermore, it is used to study the system impact of SiC power devices in several different applications, which were funded by Small Business Innovation Research (SBIR) and Oak Ridge National Laboratory (ORNL). A conclusion is drawn from these studies that SiC power devices are more suitable for high-power, high-temperature, and high-frequency systems compared to Si ones. Thus, these kinds of systems will be the potential applications of SiC power devices in the near future.
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<tr>
<td>$V_{FB}$</td>
<td>Voltage drop across Schottky barrier</td>
</tr>
<tr>
<td>$\phi_b$</td>
<td>Barrier height</td>
</tr>
<tr>
<td>$q$</td>
<td>Charge of an electron</td>
</tr>
<tr>
<td>$E_c$</td>
<td>Breakdown electrical field</td>
</tr>
<tr>
<td>$V_B$</td>
<td>Breakdown voltage</td>
</tr>
<tr>
<td>$\varepsilon$</td>
<td>Dielectric constant</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>Relative dielectric constant</td>
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<tr>
<td>$\mu_e$</td>
<td>Electron mobility</td>
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<tr>
<td>$\mu_p$</td>
<td>Hole mobility</td>
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<tr>
<td>$T$</td>
<td>Temperature</td>
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<td>$N_{tot}$</td>
<td>Total doping density</td>
</tr>
<tr>
<td>$N_{ref}$</td>
<td>Reference doping density</td>
</tr>
<tr>
<td>$N_d$</td>
<td>Ionized donor density</td>
</tr>
<tr>
<td>$N_a$</td>
<td>Ionized acceptor density</td>
</tr>
<tr>
<td>$w_d$</td>
<td>Width of depletion layer</td>
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<tr>
<td>$E$</td>
<td>Applied voltage</td>
</tr>
<tr>
<td>$v_s$</td>
<td>Saturated electron drift velocity</td>
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<tr>
<td>$E_D$</td>
<td>Peak reverse recovery current in diode</td>
</tr>
<tr>
<td>$V_R$</td>
<td>Reverse voltage on diode</td>
</tr>
<tr>
<td>$t_{rr}$</td>
<td>Reverse recovery time</td>
</tr>
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<td>$S$</td>
<td>Snappiness factor</td>
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<tr>
<td>$\frac{dI}{dt}$</td>
<td>Current changing rate</td>
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<td>$P_{RR}$</td>
<td>Reverse recovery power loss</td>
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<td>$R_{sp}$</td>
<td>Specific on-state resistance</td>
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<td>$R_D$</td>
<td>On-state resistance of diodes</td>
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<td>$R_J$</td>
<td>On-state resistance of JFETs</td>
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<tr>
<td>$R_I$</td>
<td>On-state resistance of IGBTs</td>
</tr>
<tr>
<td>$V_D$</td>
<td>Voltage drop of diodes at zero current</td>
</tr>
<tr>
<td>$V_I$</td>
<td>Voltage drop of IGBTs at zero current</td>
</tr>
<tr>
<td>$E_{on}$</td>
<td>Turn on energy loss of switches</td>
</tr>
<tr>
<td>$E_{off}$</td>
<td>Turn off energy loss of switches</td>
</tr>
<tr>
<td>$V_{th}$</td>
<td>Threshold voltage of switches</td>
</tr>
<tr>
<td>$V_{GL}$</td>
<td>Lowest gate drive voltage of switches</td>
</tr>
<tr>
<td>$V_{GH}$</td>
<td>Highest gate drive voltage of switches</td>
</tr>
<tr>
<td>$g_m$</td>
<td>Transconductance of switches</td>
</tr>
<tr>
<td>$g_{ms}$</td>
<td>Specific transconductance of switches</td>
</tr>
<tr>
<td>$A$</td>
<td>Active area of device</td>
</tr>
<tr>
<td>$V$</td>
<td>DC voltage of converters</td>
</tr>
<tr>
<td>$I$</td>
<td>Peak output AC current of converters</td>
</tr>
<tr>
<td>$\phi$</td>
<td>Phase angle between current and voltage</td>
</tr>
<tr>
<td>$f_0$</td>
<td>Fundamental frequency of output current</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Switching frequency</td>
</tr>
<tr>
<td>$M$</td>
<td>Modulation index</td>
</tr>
<tr>
<td>$D$</td>
<td>Duty ratio</td>
</tr>
<tr>
<td>$P_{D,cond}$</td>
<td>Average conduction power loss of diodes</td>
</tr>
<tr>
<td>$P_{D,sw}$</td>
<td>Average switching power loss of diodes</td>
</tr>
<tr>
<td>$P_{J,cond}$</td>
<td>Average conduction power loss of JFETs</td>
</tr>
<tr>
<td>$P_{J,sw}$</td>
<td>Average switching power loss of JFETs</td>
</tr>
<tr>
<td>$P_{J\rightarrow D}$</td>
<td>Additional loss on JFETs due to diodes</td>
</tr>
<tr>
<td>$P_{I,cond}$</td>
<td>Average conduction power loss of IGBTs</td>
</tr>
<tr>
<td>$P_{I,sw}$</td>
<td>Average switching power loss of IGBTs</td>
</tr>
<tr>
<td>$P_{I\rightarrow D}$</td>
<td>Additional loss on IGBTs due to diodes</td>
</tr>
<tr>
<td>$P_{J}(t)$</td>
<td>Instantaneous power loss of JFETs</td>
</tr>
<tr>
<td>$P_{D}(t)$</td>
<td>Instantaneous power loss of diodes</td>
</tr>
<tr>
<td>$R_{jc}$</td>
<td>Junction-to-case thermal resistance</td>
</tr>
<tr>
<td>$R_{jic}$</td>
<td>JFET junction-to-case thermal resistance</td>
</tr>
<tr>
<td>$R_{djc}$</td>
<td>Diode junction-to-case thermal resistance</td>
</tr>
<tr>
<td>$C$</td>
<td>Thermal capacitance</td>
</tr>
<tr>
<td>$R_{ch}$</td>
<td>Case-to-heatsink thermal resistance</td>
</tr>
<tr>
<td>$C_{ch}$</td>
<td>Case-to-heatsink thermal capacitance</td>
</tr>
<tr>
<td>$R_{ha}$</td>
<td>Heatsink thermal resistance</td>
</tr>
<tr>
<td>$C_{ha}$</td>
<td>Heatsink thermal capacitance</td>
</tr>
</tbody>
</table>
CHAPTER 1

Introduction

World electricity consumption was 14,781 billion kilowatthours in 2003, and it will double in 2030, growing at an average rate of 2.7 percent per year [1]. Most of the electrical power is not used directly. It is re-processed to the proper types that are needed by different customers. In this process, power electronics play an important role. At present, at least 50% of all electric power generated is processed by power electronics [2]. With more requirements on effective use of electrical energy and reduction of environmental load, the number is expected to increase to 80% by 2010 [3]. An increasing need for efficient power electronics is clearly forthcoming.

The requirements for power electronics are also more and more demanding, such as more powerful, efficient, dependable and durable, smaller in size, lighter in weight, and less costly to the consumer. All these bring new challenges to present Silicon-based power electronics technology. However, the advanced and matured Si semiconductor technology has pushed Si-based power electronic devices to their material limits. Alternative materials are being developed for future power electronic devices. Silicon Carbide (SiC), a wide bandgap material, is the most promising. Power electronic devices based on SiC
material have the potential to substitute for their Si counterparts in numerous applications. This will be further discussed in the following sections.

1.1 Overview of Si power electronic devices

1.1.1 Development of Si power electronic devices

The breakthroughs in the areas of Si power semiconductor device physics and process technology in the middle of last century have accelerated the development of Si power electronic devices. Si power electronic devices started with the invention of the bipolar junction transistor (BJT) in 1950s, and have experienced three stages as shown as Figure 1-1. In the 1960s, the appearance of the thyristor started the first stage in the history of power semiconductor devices and opened up many possibilities for the growth of power electronics as a whole. In the second half of the 1970s the two controllable non-latching type devices, the bipolar transistor module and the gate turn-off thyristor (GTO), were introduced to match the growing demand for inverter-controlled power conversion.

![Figure 1-1. Time line of Si power electronic devices.](image)

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2
equipment, which quickly became the focus of power electronics growth. This started the second stage in the chronological evolution of power semiconductor devices. The introduction of power MOSFETs in the 1970s enabled compact and efficient system designs, particularly which was based on low voltage (less than 200V) applications. To improve performance and reliability, the DMOS process and trench gate technologies were adopted subsequently, and these became the predominant options for device manufacturers. The third stage in the late 1980s through early 1990s focused on MOS-gated device physics blended with the bipolar transistor. As a result, the evolutionary power device, the insulated gate bipolar transistor (IGBT) was put into practical use and has been a key component for the acceleration of the power electronics. The IGBT, by virtue of its MOSFET-like insulated gate controllability and bipolar-like conductivity modulated on-state operation, has successfully shown its ability to perform adequately in high power and high frequency fields [4-5]. However, in the recent decade, no new concepts of power electronic devices were introduced to the market though some new types of improved power electronic devices has been developed by optimal integration of the existing technologies, such as the integrated gate-commutated turn-off (IGCT) thyristor; the MOS-Controlled thyristor (MCT), the emitter turn-off (ETO) thyristor, the injection enhanced (insulated) gate transistor (IEGT), etc. The development of Si power electronic devices has slowed down.
Present status and limitations of Si power electronic devices

Presently, Si power electronic devices dominate the commercial market. They are widely utilized in industry, traction, generation, transmission and distribution, and emerging markets such as flexible AC transmission systems, power quality, and custom power. Some typical applications are listed in Figure 1-2.

However, as discussed previously, after more than one half century’s efforts, Si semiconductor technology has been highly developed. Today, the main job of researchers and manufacturers has been integrating and perfecting the features and characteristics of the existing devices. It is hard to achieve any breakthrough. Take IGBTs and GTOs as an example. The power handling of IGBTs increased initially at a rate of roughly $20 \times$ every 5 years. Around 2005, the rate of growth diminished to approximately $5 \times$ every 5 years.

Figure 1-2. Comparison of devices application fields [6].
The same thing happened to GTOs (refer to Figure 1-3) [7]. Therefore, there are good reasons to believe that the improvements will begin to saturate in the future.

A substantial reason behind this is that Si power electronic devices are reaching the fundamental limits imposed by the material of Si. More specifically, it is embodied in the following aspects:

1. Small bandgap (1.1eV) — intrinsic trigger

   Bandgap is a basic characteristic of a semiconductor, which determines its other characteristics. In this sense, small bandgap is the trigger to all other limits which will be discussed below.

2. Low breakdown electric field — limit voltage blocking capacity, efficiency

   The small bandgap leads to low intrinsic breakdown electric field, which is approximately 30 kV/cm. Correspondingly, the voltage blocking capacity of discrete Si devices is less than 12 kV. For high voltage applications, stacking packaged devices in

![Figure 1-3. The advance in power handling capacity of IGBT and GTO.](image)
series are required, e.g. series stacking of thyristors that is commonly done in high-voltage inverters of HVDC stations. Series stacking, in particular, is expensive from a packaging standpoint, and requires rather complicated design to maintain voltage-sharing between devices in the stack. Hence, there is a strong incentive to develop devices having greater voltage blocking capacity but in the same or smaller device package.

On the other hand, to compensate for the low breakdown field, the active layer is usually very thick so that the voltage drops over a long region of semiconductor, reducing the associated internal electric fields. However, this long active layer contributes to large on-state resistance and in turn large power losses, low efficiency, and also has significant influence on current density and switching speed. This is a tradeoff in device design.

3. Low thermal conductivity — limit temperature tolerance

Based on the best quality of Si power devices and packaging technology, the normal operational temperature of Si power devices determined by the thermal conductivity of Si is less than 150 °C. Thus, significant thermal management is required for most power applications. There are three standard options for cooling power devices, natural air, forced air, or liquid-cooled heatsinks. As the temperature of the environment increases, the capacity of the cooling system decreases. The power rating of the converter determines the type of heatsink to use. For low-power converters, bulky, natural-air heatsinks are sufficient, whereas high-power converters require the more expensive, but
smaller liquid-cooled heatsinks, which require a pump to circulate the coolant as well as a radiator and a fan to cool it. A heatsink typically occupies one-third of the total volume of a power converter and usually weighs more than the converter itself. Developing power electronics that can withstand higher temperatures is one way of decreasing the cooling requirements, size, and cost of the converter. To improve the temperature tolerance of devices, one way is to reduce the power losses of devices. However, as mentioned previously, the margin for the improvement in this area is rather small. The other choice is to substitute Si for some other material which has higher thermal conductivity. Wide bandgap materials have been proven to be good candidates.

4. Low radiation tolerance combined with high power losses and low thermal conductivity — limit switching frequency

The switching frequency of the devices is limited by the heat generated by the devices, primarily the switching losses. Typically, Si power devices have a switching limit less than 20 kHz for power levels in the range of a few tens of kW, and are highly susceptible to harsh environments, such as high ambient temperature and intense radiation. Generally speaking, with the less switching loss and better thermal characteristics, the higher switching speed a device can handle. Since recent development advances have driven these two factors to approach to the material limits, the margin for switching speed to improve is rather small. However, higher-frequency operation is always preferred for the
purposes of power quality (less harmonics), exact control for high performances, system compactness (smaller passive components), and user’s comfort (less audible noise).

All in all, the substantial obstacle restricting power electronic devices from meeting the future requirements is the limitations from Si material. An efficient and feasible solution is to find an alternative for Si.

1.2 Alternative materials for power electronic devices

— wide bandgap semiconductors

The slow development of Si power electronics due to the limitations from Si material has provided an opportunity for other materials. Significant technical advances are occurring for the development and process of wide bandgap semiconductor materials due to their superior electrical characteristics compared to Si. As shown in Table 1-1, wide bandgap materials have higher bandgap energy, larger electrical breakdown field, reasonably high electron mobility, higher thermal conductivity, and larger saturated electron conductivity.

Power electronics devices based on these materials will likely result in substantial improvements of power electronics systems in terms of power capacity, efficiency, reliability, and system compactness. Based on the data in Table 1-1, the characteristics of the devices made of these materials can be theoretically estimated [8].
Table 1-1. Physical characteristics of Si and main wide bandgap semiconductors [8]

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap $E_g$, (eV)</td>
<td>1.12</td>
<td>3.03</td>
<td>3.26</td>
<td>3.45</td>
<td>5.45</td>
</tr>
<tr>
<td>Dielectric constant, $\varepsilon_r$</td>
<td>11.9</td>
<td>9.66</td>
<td>10.1</td>
<td>9</td>
<td>5.5</td>
</tr>
<tr>
<td>Electric breakdown field, $E_c$ (kV/cm)</td>
<td>300</td>
<td>2500</td>
<td>2200</td>
<td>2000</td>
<td>10000</td>
</tr>
<tr>
<td>Electron Mobility, $\mu_n$ (cm$^2$/V·s)</td>
<td>1500</td>
<td>500</td>
<td>1000</td>
<td>1250</td>
<td>2200</td>
</tr>
<tr>
<td>Hole Mobility, $\mu_p$ (cm$^2$/V·s)</td>
<td>600</td>
<td>101</td>
<td>115</td>
<td>850</td>
<td>850</td>
</tr>
<tr>
<td>Thermal Conductivity, $\lambda$ (W/cm·K)</td>
<td>1.5</td>
<td>4.9</td>
<td>4.9</td>
<td>1.3</td>
<td>22</td>
</tr>
<tr>
<td>Saturated Electron Drift Velocity, $v_{sat}$ ($\times 10^7$ cm/s)</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2.2</td>
<td>2.7</td>
</tr>
</tbody>
</table>

Among these semiconductors, diamond has the widest bandgap; consequently it also has the highest electric breakdown field. Silicon carbide polytypes and gallium nitride have similar bandgap and electric field values that are significantly higher than Si. Higher electric breakdown field results in power devices with higher breakdown voltages. Assuming the same doping density, the theoretical breakdown voltage of a diamond diode is 514 times more than that of a Si diode. This number for 6H-SiC, 4H-SiC, and GaN is 56, 46, and 34 times that of a Si diode, respectively. Moreover, with higher electric breakdown field, more doping can be applied to the material which will further increase the gap between the upper breakdown voltage limits of the wide bandgap semiconductors and that of Si.

With higher electric breakdown field and higher doping, the width of the drift region in devices is reduced. As shown by the calculation in [8], diamond requires the minimum
width, while 6H-SiC, 4H-SiC, and GaN follow diamond in the order of increasing widths. Compared to these, Si requires around ten times thicker drift region than the SiC polytype and GaN devices. As a result, the on-resistance of the drift region of Si devices is also around ten times larger.

The maximum operational temperature of a semiconductor material is determined by the bandgap. The temperature limit is reached when the number of intrinsic carriers approaches the number of purposely added (extrinsic) carriers. Therefore, semiconductors with wider bandgap can operate at higher temperatures. Diamond has the widest bandgap, so its power devices have the capability to operate at higher ambient temperatures than other materials. The maximum operating temperature for each semiconductor can be estimated by assuming a maximum for Si of 150 °C and multiplying this temperature by the ratio of bandgap to that of Si as suggested by [9]. Diamond shows distinct temperature advantage, 730 °C. Then 6H-SiC, 4H-SiC, and GaN have the similar value, all above 405 °C, and much higher than 150 °C for Si. In addition, the greater the thermal conductivity is, the better the material conducts heat to its surroundings, which means device junction temperature increases more slowly. Diamond still leads the other materials (about five times of that of SiC polytypes). GaN has the worst thermal conductivity and is even lower than Si.

High-saturated electron drift velocity is another good merit of wide bandgap material. The high-frequency switching capability of a semiconductor material is directly
proportional to its drift velocity. The drift velocities of WBG materials are more than twice the drift velocity of Si. Therefore, it is expected that WBG semiconductor based power devices could be switched at higher frequencies than their Si counterparts. Especially, higher drift velocity allows charge in the depletion region of a diode to be removed faster, resulting in short reverse recovery time.

It is obvious that diamond power devices will have the best performance and can be viewed as the ultimate semiconductor. However, its processing problems have not been solved yet. There are no diamond power semiconductor devices available yet. SiC and GaN power devices have similar performances. But compared to SiC, GaN has several drawbacks. First, since there is no native oxide, which is required for MOS devices, GaN MOS devices are not possible. Second, GaN boules are difficult to grow. Therefore, pure GaN wafers are not available; instead GaN wafers are grown on sapphire or SiC. Even then, thick GaN substrates are not commercially available. As a consequence, GaN wafers are more expensive than SiC wafers. Third, the thermal conductivity of GaN is 1/4 of that of SiC. This property is especially important in high power, high temperature operation because the heat generated inside the device needs to be dissipated as quickly as possible. Therefore, most research of GaN devices is focused on optoelectronics and radio frequency uses [10-12]. At present, SiC is the best choice for power electronic devices due to its relatively mature technology. Much research has been conducted on SiC materials and devices. There are also some commercial SiC power devices currently
available. This work will also focus on issues regarding SiC power semiconductor technology.

1.3 Present status and potential applications of SiC power electronic devices

In this section, the present status of SiC power electronic devices is discussed in terms of the following aspects: SiC wafer industry, proposed device structures, and commercially-available devices and prototypes. Then, their potential applications are summarized based on analysis of device properties and literature review.

1.3.1 Overview of SiC wafer industry

Among the numerous polytypes of SiC, 6H-SiC and 4H-SiC are the most attractive. These two types of wafers were first commercially available in 1989 and 1993, respectively. 6H-SiC technique is slightly more developed and cheaper. However, 4H-SiC seems more promising, and is particularly suitable for vertical devices, because of its higher carrier mobility.

Presently, suppliers of SiC wafers are not many. Cree dominates SiC wafer production, which has about 85% of the market, and around 94% SiC wafer production is carried out in the US (other suppliers: II-VI, Dow Corning Corporation, TDI, Inc., INTRINSIC Semiconductor), with 4% in Asia (ADMAP, Japan) and 2% in Europe (SiCrystal AG, Germany). With an estimated 250,000 SiC wafers produced in 2003, the volume of SiC wafers is estimated to reach more than 600,000 units in 2007 [13].
High-power devices require large die size (>1 cm² for megawatt switching) and low-defect-density, large diameter wafers for higher yield. However, commercial SiC has been limited due to high density of defects (micropipes, dislocations, misoriented blocks, mosaicity, strain, intrinsic point defects, and foreign polytype inclusions). Micropipes are the main obstacles for growing viable large wafers. They are screw dislocations with an open core that propagate in the growth direction all the way to the surface, appearing as a hole. These hence propagate into the epilayer, causing inhomogeneity, low forward current, and low manufacturing yield. At present, most commercially available wafers are at 2″ (50.8 mm) or 3″ (76.2 mm), with 1-10 micropipes per cm². The best allowable active area is about 20 mm², which is still much less than requirements for high current power electronics. Recently, Cree announced the selling of 4″ SiC substrate and epitaxy material [14], and it is transitioning to 4-inch SiC production in 2007 [15]. This opens a new opportunity to SiC power electronic devices.

### 1.3.2 Proposed structure of SiC devices in the literature

A wide variety of SiC power devices have been proposed, including diodes, BJT, GTO, MCT, MOSFET, and IGBT. Generally, these devices fall into categories — unipolar and bipolar or two- and three- terminal devices as shown as Figure 3-1. In the following parts, each device is described in detail.
Power rectifiers

As shown in Figure 1-5, several structures have been demonstrated for SiC power rectifiers, which are categorized into two classes — the unipolar Schottky rectifiers and the bipolar junction rectifiers. Schottky rectifiers offer fast switching speed but suffer from high forward voltage drop because mostly majority carriers participate in its forward conduction. Presently, SiC Schottky diodes are commercially available in ratings up to

(a) Schottky structure  (b) PiN structure  (c) MPS/JBS structure  (d) TSBS structure

Figure 1-5. Structures of SiC power rectifiers.
1200V and 50 A. By contrast, the PiN junction rectifier has low forward voltage drop and high current capability due to conductivity modulation, but has slow reverse recovery characteristics due to minority carrier storage. To combine the good features of these two rectifiers, hybrid rectifier structures such as the Junction Barrier Schottky (JBS), Merged PiN/Schottky (MPS), and trench MOS Barrier Schottky (TMBS) rectifiers were also proposed to use in SiC power rectifiers by researchers. Paper [21] also pointed out a Trench Schottky Barrier Schottky (TSBS) is particularly suitable for SiC devices.

Power Transistors

Similarly, power transistors have two categories — unipolar and bipolar devices. MOSFETs and JFETs are unipolar devices, while BJT, IGBT, and MCT are bipolar devices.

Figure 1-6 illustrates two basic designs of the power MOSFET, namely vertical trench U-shape MOSFETs (UMOSFET) and double-diffused MOSFET (DMOSFET). The first SiC power transistors were UMOSFET reported by Cree in 1992. Compared to
DMOSFET, it has a higher channel density (channel width per unit active area), and its gate oxide is subject to rupture due to the high electric fields developed at the trench corners as a result of the high breakdown electric field strength of the underlying semiconductor. Therefore, DMOSFET with the planar gate structure is preferable for SiC. However, the DMOSFET is not without its own problems. Activation of the implants that form the base and source regions requires annealing at temperatures in excess of 1500 °C. Depending upon the precise annealing conditions (time, temperature, and ambient), this anneal can create surface roughness through a process called step bunching. The surface roughness has been shown to severely degrade channel mobility in MOSFETs [16]. To overcome the high electric field in gate oxide and the poor inversion layer mobility in the channel of these two structures, a new design for SiC MOSFET is required.

Using a pn junction gate to take the place of a MOS-gate to control the carrier flow in the channel of the FET, then a JFET is formed. Figure 1-7 gives the basic structures of a

(a) Trench VJFET  
(b) MOS-enhanced JFET  
(c) SEJFET

Figure 1-7. Basic structures of SiC JFET.

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SiC JFET. JFETs have no critical gate oxide. This avoids several material science issues peculiar to MOSFETs, including channel mobility, oxide breakdown, and long-term reliability of the oxide. It can be said that JFETs are the easiest to fabricate among all the switches. However, JFETs are normally-on devices. Most power control systems require normally-off devices so that the system has a safe condition (off) if no control signal exists. One way to solve this problem is to connect a SiC JFET in cascade with a normally-off device, such as a Si MOSFET [22]. As shown in Figure 1-8 (a), the SiC JFET blocks the high voltage, while the Si MOSFET provides normally-off gate control. One problem of this structure is that the Si part has a relatively low temperature limit. The structure shown in Figure 1-8 (b) is another normally-off design for an all-SiC device, called static expansion channel JFET (SEJFET). In addition, Semisouth has demonstrated a JFET structure which is between normally-on and normally-off, called ‘quasi-off’.

![SiC JFET/Si MOSFET Cascade](image)

(a) SiC JFET/Si MOSFET Cascade

![SEJFET](image)

(b) SEJFET

Figure 1-8. Two normally-off structures of SiC JFETs.
These ‘Quasi-Off’ devices are designed to block half of the rated blocking voltage at zero gate bias and achieve full rated blocking voltage with a modest negative bias, typically between 0 and -5 V [23].

Compared to the unipolar devices, the research on bipolar devices is not as much. Although several structures such as BJT, IGBT, MCT, GTO are also proposed for SiC devices, the development of these devices has been slow because of the relative complexity and difficulty of device processing. For more details, please refer to [24].

1.3.3 Commercially available SiC devices and prototypes

As discussed previously, many devices have been proposed for SiC. But only SiC Schottky diodes have already been commercially available since 2001. Single device rating is up to 1200V/50A [25]. The main suppliers include Cree, Rockwell, Advanced Power Technology, SemiSouth, Infineon, and IXYS. These devices have been reported to be used in some real applications [26]. Yole development forecast shows that the devices market for SiC Schottky diodes will reach about $45M by 2010. The target price for such a component is expected to decrease down to $0.2/Amp (present ~$0.45/Amp) [27].

SemiSouth began to provide sample SiC JFETs in 2005. SiCED and Rockwell have also developed some SiC JFET prototypes. Recently, SiC MOSFETs (from Cree) are also available for research purpose. It is promising for SiC MOSFETs to enter the market following SiC JFETs. Moreover, some high power modules have been fabricated and tested, such as 1200V/300A Si IGBT/SiC Schottky diode single phase module (Cree) [28].
and 55kW Si IGBT/SiC Schottky diode inverter [29]. At the end of 2006, Cree announced the first Si IGBT/SiC Schottky diode co-package products (CID150660) [30].

1.3.4 System benefits and potential applications of SiC power devices

As discussed in the previous section, the superior properties of SiC material result in a series of superior performances of power electronics made of SiC. Consequently, systems based on SiC devices have substantial improvements in efficiency, reliability, size, and weight even in harsh environments. Therefore, they are attractive especially for high-voltage, high-temperature, high-efficiency, or high-radiation applications. Table 1-2 summarizes the advantages and application scopes of SiC devices. Much work has been conducted in the areas of military, aerospace, and energy utilities [31-36], where the cost is not a main concern. As the cost of SiC power devices decrease, more and more applications for vehicles, motor drives, and industry will be considered [37-39].

<table>
<thead>
<tr>
<th>Device Characteristics</th>
<th>System Benefits</th>
<th>Application Scope</th>
</tr>
</thead>
<tbody>
<tr>
<td>High breakdown voltage</td>
<td>Large power capacity</td>
<td>Military: combat vehicles, weapons, electric ships</td>
</tr>
<tr>
<td>High current density</td>
<td>High reliability, compactness</td>
<td>Aerospace: spacecraft and satellite applications</td>
</tr>
<tr>
<td>High operational temperature</td>
<td>Less cooling requirements</td>
<td>Energy: power transmission and distribution</td>
</tr>
<tr>
<td>High switching frequency</td>
<td>Reduced passive components</td>
<td>Industry: deep earth drilling for energy exploring</td>
</tr>
<tr>
<td>Low power losses</td>
<td>High efficiency</td>
<td>Future: domestic automobiles, motor drives</td>
</tr>
</tbody>
</table>
1.4 Challenges of SiC power electronic technology

Although Si semiconductor technology has been highly developed, the fabrication of SiC semiconductors is not one-to-one duplication of Si semiconductors, and the implementation of SiC semiconductors is not chip-to-chip replacement of Si semiconductors either. New device structures, processing technology, and electric circuits are required in order to take advantage of SiC semiconductors. Therefore, a series of issues needs to be solved before the era of SiC devices comes.

1. Cost

High cost is one of the barriers limiting the development of SiC devices. Currently, the price of SiC devices is 5-10 times of that of Si devices. As shown as Figure 1-9, 40% of the total of SiC devices comes from SiC material, 50% from process, and 10% from packaging & testing. Thus, SiC material and processing technology are critical factors which dominate the cost of SiC devices and influence their prospects in the future market.

Figure 1-9. Typical cost breakdown for SiC devices [40].
2. Material availability and quality

Now, most of available SiC wafers are in 3 inch or 2 inch size. The emergence of 4-inch wafers is expected to bring a cost breakthrough because they are compatible with standard semiconductor tool sets. Cree has announced the capability to produce 4-inch SiC wafers. The quality of the wafers is also improved. Micropipe is no longer the main defect that limits the size of the SiC wafer. However, the approach called physical vapor transport (PVT) which is being used to produce all industrial standard SiC wafers is far from mature. It still has problems such as direction control of the gas-phase composition and control of dopant feeding, which degrade the quality of SiC wafers [17].

3. Device design and fabrication

All the basic process steps of SiC devices have been demonstrated. But many problems need to be dealt with. First, to minimize parasitic substrate resistance and maximize carrier concentration, a doping of \(10^{19} \text{ cm}^{-3}\) would be desired. Such a high level is difficult with P\(^+\) substrate. Also, high temperature annealing at 1500 °C -1700 °C is required. Second, SiC-SiO\(_2\) interface has a poor quality that results in poor channel mobility and low transconductance. Third, ohmic contact requires high-temperature annealing and its stability at high temperature needs further examination. Fourth, surface charges and surface states of SiC have different properties. Different control strategy should be used, which is critical to suppress the breakdown near the surface [19]. On the other hand, most of the device structures tried as of present time is copied from Si
technologies. Although these structures have been proved in Si, they are not necessarily transposable to SiC. New device structures may be developed in order to fit SiC material.

4. Device packaging technology

High temperature, high power density packaging techniques are required to take full advantage of SiC capabilities. The currently available packaging techniques are for the application of Si devices, which generally has power density limit of \(200 \text{ W/cm}^2\) and/or a use temperature of less than 125 \(^\circ\text{C}\), while the SiC device may require a power density of \(1,000 \text{ W/cm}^2\) and/or a use temperature of 250 \(^\circ\text{C}\) or more.

5. Application

Although SiC devices are supposed to be a substitution for Si devices, it is impossible to do a chip-to-chip replacement. New circuit, gate drive, microprocessor and passive components are needed in order to take the advantages of SiC device and adapt to harsh application environments like high temperature, high radiation. Device characterization, testing and modeling are needed in order to guide device designers, as well as system modeling to direct system design and explore suitable applications for SiC power devices. The work in this dissertation is focused on this.

1.5 Summary of the content of this dissertation

In this work, a method for system modeling of a SiC power system based on basic physics and device tests is presented. It includes temperature-dependent single device models specified for system-level modeling, power loss models for power converters, and
thermal models for cooling system. The method was verified by experimental results, and used to study the system impact of SiC power devices in several different applications.

Specifically, the content of each chapter is as follows:

Chapter 1  Introduction

This chapter introduces the background of the research on SiC power devices. It points out that Si power devices have been driven to its material limitations, and SiC is promising to take the place of Si to be the material for next generation power electronic devices. The present status, potential applications, and obstacles of SiC power devices are also discussed.

Chapter 2  Motivation of this work

This chapter reviews the previous work in the area of power electronics and system modeling. No intact electro-thermal system modeling method was presented. There are no suitable device models for system simulation, and few models considering temperature impact, especially for SiC devices.

Chapter 3  Electro-thermal modeling of SiC power systems

A method for electro-thermal modeling of a SiC power system is presented, which includes temperature-dependent analytical device models for most popular SiC power devices and comparable Si power devices, mathematical power loss models of converters, and thermal system models.
Chapter 4  Experimental verification

The models presented in chapter 3 are verified with single device tests and converter tests.

Chapter 5  System-level evaluation of SiC-based converters in different applications

The chapter is the practical applications of the modeling method presented in chapter 3. Four applications have been studied. They are Navy’s motion control application, wind generation application, battery-utility interface application, and hybrid electric vehicle application. Advantages are found for SiC-based system compared to Si-based system.

Chapter 6  Contributions and future work

Main contributions of the dissertation are summarized in this chapter. Future work is also recommended.
CHAPTER 2

Motivation of this work

Today, more and more attention is being paid to modeling and simulation, not only of power electronics devices but also of power electronic systems. The traditional development method “design → prototype → debug → redesign → reprototype → repeat until a new product is achieved,” is no longer as competitive or efficient as the method incorporating modeling and simulation into the design process, which saves both time and expense. This is the case, especially for complex or large systems, like power transmission system.

2.1 Introduction of electro-thermal modeling for power electronic systems

Due to the increasing requirements for high power density, high frequency, and integration in power electronic systems, a good estimation of power losses enables the access to system performance and optimization of system design. For an instance, thermal management and maximum allowable switching frequency are two issues directly related to the power dissipation of power devices. An accurate predication of power losses in power electronic systems is an important guide to select proper thermal
management and switching frequency, and ensure the reliable operation of the systems. Therefore, electro-thermal analysis for a power electronic system becomes extremely important.

Figure 2-1 demonstrates the structure of electro-thermal modeling for power electrical systems. It deals with the analysis of both electrical and thermal performances, which interacts with each other by the power dissipation in power electronics. Except electrical system models (this is not in the scope of this work), three types of models are involved. They are device models, power loss models and thermal system models. The setup of a system electro-thermal modeling is not a simple mix of these models because they deal with different issues using different methods and simulation tools, and usually they are not compatible with each other. The following requirements need to be met:
1. Device models must consider temperature impact.

2. Each model should have relatively high computation efficiency.

3. The time constant difference between the models should be as small as possible.

4. It is better that these models can be implemented in the same simulation environments or have a convenient interface.

Reviewing the literature, hundreds of articles have been published in the area of power electronic modeling. But most of them focus on one or two of the aforementioned modeling issues. No intact electro-thermal modeling method was presented. Thus, more efforts are needed to fulfill the electro-thermal modeling, such as revise, supplement the existing models, or create new models.

In the next section, the previous work will be reviewed. It will include not only the papers on SiC devices but also Si devices. On one hand, it is because the research on SiC devices is limited. On the other hand, most modeling methods of Si devices can be applied to the research of SiC devices with proper modification.

### 2.2 Existing models and limitations

As mentioned previously, most power loss related papers can not cover all the issues in electro-thermal modeling. Some papers focus on the calculation of power loss without giving concrete device models [41-43]. Some focus on thermal system models [44-51]. The others cover device and power loss models [52-56], or power loss and thermal models [57-59]. Only a few try to cover all of them, but fail to include enough details
[60], or some part of models are too simple [61]. As for SiC power electronic systems, only a few publications were found [62-67].

More specifically, power loss models mainly fall into two types. The first type is experiment-based models. They are based on power loss data from virtual system tests. They are used in simulations as either look-up tables [69] or curve-fitting equations [68]. The weaknesses of this type models are as follows. First, the virtual system has to be built. Second, accuracy is limited by tests. Third, it is time-consuming. Fourth, it is not applicable except under the conditions for which tests were carried out. Compared to experiment-based models, the other model type — mathematical models are more efficient. In these models, the load current usually is regarded as current source, and does not change in a short period, such as a switching period or a fundamental wave period. Then the power loss is computed based on the instantaneous current, voltage, and device characteristics, and averaged in the period [68-71]. For more complex power electronic circuits, like PWM controlled inverters, the real current and voltage are not easy to simulate. Instead of using instantaneous current and voltage, the average value of the current is computed based on specific control information. The control related parameter — modulation index comes into the model equations [41-43][82]. This method not only solves the problem in complex systems but also integrates control strategy and dramatically improves computation efficiency. Therefore, it is a good choice for electro-thermal system modeling.
For thermal models, many researchers have used similar approaches. Most of them use thermal equivalent circuit to study temperature change in power electronic systems [44-51]. The differences only lie in how to get thermal parameters and solutions. Most use curve fitting method to get thermal parameters, like [46]. Some solve the circuit in time domain [45], and some in frequency domain [49].

For device models, most models involved in electro-thermal research of power electronic systems are experiment-based models, because they are simple and easy to include temperature impact [58][59][72-76]. There are also some simulator-based models, which usually are solved off-line and temperature dependency are not included [53][54][61]. A few papers use analytical models, which also neglect the influence of temperature [55-56]. Therefore, device model is the weakest link in the system modeling. The following paragraphs covers more details on device model research.

In recent years, many of papers have been published on device models. The variation of the models and solving methods are complex enough to confuse the users. Unlike some previous review articles [77-80] intending to categorize these modeling efforts thoroughly, this work tries to discuss the speciality and weakness of some widely used models.

1. Physics-based models

This kind of model is usually developed for the purpose to understanding the performance of devices. These models use the partial differential equations of the
semiconductor physics, which describe potential distribution, carrier concentrations and current flow [78]. These nonlinear partial differential equations have no close mathematical solution. Different approaches are proposed to solve the equations, such as approximate solution, finite difference method, Laplace transformation, and lumped-charged method [77][79][81][82]. Although all these models have good physical significance and forecasting ability, the solving process is too complicated and time-consuming. In addition, the accuracy of a model depends on the quality of its parameters. The models in this category usually involve a great amount of parameters ranging from structural parameters (related to device design), physical parameters (related to material, physical phenomena), electrical parameters, to thermal parameters, etc. Thus, the extraction of parameters is another difficulty. Only part of the modeling papers declared required parameters and their extraction [83][84], and thus some other papers have to focus only on parameter extraction [85-88]. It could be said that from an engineering view, this kind models are the hardest to be applied though they are the basis of many other types of models.

2. SPICE-type models

These models are attached to some kind of simulators, such as SPICE, Saber, MEDICI, etc. The device analysis is based on the special compact models available in the simulator. Most research conducted in the literature was based on these models [89-98]. But they are originally designed for microelectronic devices and poorly describe the
dynamic and static behavior of power devices [77]. To solve the problem, so-called subcircuit models were constructed to count the special effects in power devices by using built-in models in simulators and introducing some passive component, switches, and controlled current or voltages, such as [89]. But this method leads to very complex and time-consuming models. Moreover, these simulators are developed particularly for assisting device design. They require design parameters, like structural parameters and doping density. These parameters are unknown to the device users. Even if these parameters are available, it is also hard for system designers to integrate these models directly into system simulation. Because device simulators lack the capacity of implementing mathematical functions, this is not a good choice for system simulation.

3. Experiment-based models

These models are the simplest. They define equations based on curve fitting of tested results rather than device physics [77]. It is easy to consider the temperature impact and be implemented in system simulation tools. The accuracy is limited by the number of tests, test circuit, and test conditions. They may vary from case to case, and are not universally applicable. Even for the same case, it lacks of the capability to predict the device behaviors outside the test scope. If the number of samples and tests increase, the models can be more representative. However, many experiments can be time-consuming and impractical.
4. Table models

Table models are based on the storage of relevant device characteristics [77]. The table can be filled by experimental test points or data from device simulations. Then, it is inevitable for table models to have the same problems with these methods. But due to simple concept and high computation-efficiency, like the experiment-based models, they are most widely used in the evaluation of device performances.

5. Analytical models

These models use a set of mathematical expressions to describe device behaviors. They are usually simplified fundamental physics equations under specific assumption [99-104]. The format and complexity of these models vary considerably, depending on what kind of characteristic they describe and how many factors they consider. Although these models can only be applied under assumed conditions and describe some aspect of characteristics, it could be most useful and flexible for system simulations because these models can be simplified to only predict the characteristics of interests. By careful design, a small set of parameters and reasonable accuracy with good computation efficiency can also be achieved.

In summary, since electro-thermal system modeling mainly focuses on the issues of power loss and temperature of power electronic systems, analytical device models specialized for these characteristics normally work well. For SiC Schottky diodes, many papers give the analytical equation of on-state resistance [105-108], and a few mention
the influence of temperature. However, there is no such model describing their reverse recovery characteristics. For SiC JFETs, most models are SPICE-type models [89], and also there is a lack of analytical models.

2.3 Proposed models

Based on the above discussion, the electro-thermal models of SiC power electronic systems should be composed of:

1. Temperature-dependent analytical device models describing both static and dynamic characteristics with a small set of easy-obtained parameters

2. Mathematical power loss models based on small period average value under a specific control strategy

3. Thermal network models based on thermal equivalent circuit

They will be presented in the next chapter.
CHAPTER 3

Electro-thermal modeling of SiC power electronic systems

A method for electro-thermal modeling of SiC power systems is presented, which includes temperature-dependent analytical device models for most popular SiC power devices and comparable Si power devices, mathematical power loss models based on converter application, and thermal system models.

As shown as Figure 3-1, the single device models are analytic models combined with...
some test results, which describe devices’ characteristics in both conduction and switching periods under different temperatures. The converter power loss models use an average technique to estimate the system power loss under a specific control strategy. Their inputs are device characteristics given by single device models, and the system operation variables (converter dc side current and voltage, ac side current and voltage, and the modulation index, power factor) calculated by application models. Their outputs are power losses of switches and diodes. Then, the power losses are input into the thermal models to get real-time junction temperatures of devices. At the same time, the temperatures are fed back to the single device models in order to update devices’ characteristics. All these models will be discussed in detail in the following parts.

3.1 Single device models

In this section, single device models for SiC Schottky diodes and SiC JFETs are presented. These models describe both static and dynamic characteristics of the devices. Temperature impact on their behaviors is also considered. In addition, for the purpose to compare with Si power devices, models for Si diodes and Si IGBTs are also presented briefly.

3.1.1 Models for SiC Schottky diodes

1. Static State

The structure of a SiC Schottky diode and its equivalent circuit are shown in Figure 3-2. $V_{FB}$ is the voltage drop across the Schottky barrier; $R_D$ is the resistive voltage drop
across the lightly doped drift region; $R_S$ and $R_C$ are the resistance of substrate and contact, respectively.

In a SiC Schottky diode, the thermionic emission process dominates in the transport of current across a metal $n$-type semiconductor contact. Under the forward bias condition, the current flow across the Schottky barrier is given by

$$J_F = CT^2 e^{q(V_{FB} - \phi_B)/kT},$$

where $\phi_B$ is the barrier height between the metal and $n$-type semiconductor, $T$ is the absolute temperature, $q$ is the charge of an electron, $k$ is Boltzmann’s constant, $C$ is Richardson’s constant, which is given by

$$C = \frac{4\pi mk^2 q}{h^3},$$

where $m$ is the effective mass of an electron, and $h$ is Plank’s constant. For 4H-SiC, the theoretical value of Richardson’s constant is 146 A·cm$^{-2}$·K$^{-2}$ [110].

Solve (3-1) for $V_{FB}$, and neglect $R_S$ and $R_C$ (because they are usually small compared to $R_D$ for power devices with breakdown voltage larger than 200V), then the total voltage across the lightly doped drift region.
drop across a Schottky power diode can be expressed as

\[ V_F = \phi_B + \frac{kT}{q} \ln \left( \frac{J_F}{C T^2} \right) + J_F R_D, \]  

(3-3)

Since SiC Schottky diode is a majority carrier device, its drift region specific on-state resistance \( R_D \) can be presented by \[111\]

\[ R_D = \frac{4V_B^2}{\varepsilon E_c^3 \mu_n}, \]  

(3-4)

where \( V_B \) is the breakdown voltage; \( E_c \) is the breakdown electrical field; \( \mu_n \) is electron mobility.

Differentiation of Eq. (3-3) with respect to \( J_F \) yields the on-state specific resistance of a Schottky power diode:

\[ R_{sp} = \frac{dV_F}{dJ_F} = \frac{kT}{q} \left( \frac{1}{J_F} \right) + R_D. \]  

(3-5)

It indicates the dependence of this on-state specific resistance with respect to temperature and forward current. Moreover, as the forward current increases, the contribution of the first component in (3-5) becomes smaller and can be neglected. This means that the on-state resistance is nearly constant regardless of forward current and only changes with temperature at a relative high current region (>1A in this case), which corresponds to the linear region in Figure 3-3. Most SiC Schottky power diodes operate in this region. Thus, it is reasonable to only consider resistive loss due to the drift region resistance \( R_D \) and the loss due to the voltage drop \( V_D \) (which is shown in Figure 3-3) in system modeling. The
expression for the conduction losses of a Schottky diode is given by

\[ P_{D,\text{cond}} = I_{D,rms}^2 R_D + I_{D,\text{ave}} V_D, \]  

Equation (3-6)

where \( I_{D,rms} \) and \( I_{D,\text{ave}} \) are the rms and average value of the current flowing through the diode, respectively.

**Temperature dependency**

Equation (3-4) indicates that the temperature dependency of the on-state resistance is determined by the change of \( \mu_n \) with temperature. By Caughey and Thomas’ model [112, 113], \( \mu_n \) is dependent on doping density as shown in (3-7). This model counts the combined lattice and ionized impurity mobility. Another model reported by Sabnis and Clemens [113] considers the mobility due to carrier heating and is shown in (3-8). It reflects the effects of applied electrical field and saturation velocity. Combining Caughey and Thomas’ model with Sabnis and Clemens’ model, the resistances can be estimated
more exactly. $\alpha$ and $\beta$ are empirical coefficients, please refer to List of Symbol at the beginning for symbol definitions.

$$\mu_0 = \mu_{\text{min}} + \frac{\mu_{\text{max}} - \mu_{\text{min}}}{1 + \left( N_{\text{tot}} / N_{\text{ref}} \right)^{\alpha}}$$  \hspace{1cm} (3-7)

$$\mu_n(E) = \frac{\mu_0}{1 + \left( \frac{\mu_0 E^{\beta}}{v_s} \right)^{1/\beta}}$$  \hspace{1cm} (3-8)

In (3-7) and (3-8), $\mu_{\text{max}}$, $\mu_{\text{min}}$, $N_{\text{ref}}$, and $v_s$ are temperature-dependent. They can be approximated using simple power expressions of temperature, as shown in (3-9) - (3-12). $A_{\mu_{\text{max}}}$, $A_{\mu_{\text{min}}}$, $A_{N_{\text{ref}}}$, $B_{\mu_{\text{max}}}$, and $B_{\mu_{\text{min}}}$ are the parameters that can be obtained by fitting experimental data, such as in papers [114-116]. The parameters used in this work are given in Table 3-1.

$$\mu_{\text{max}} = A_{\mu_{\text{max}}} \times \left( \frac{T}{300} \right)^{-B_{\mu_{\text{max}}}}, \hspace{1cm} (3-9)$$

$$\mu_{\text{min}} = A_{\mu_{\text{min}}} \times \left( \frac{T}{300} \right)^{-B_{\mu_{\text{min}}}}, \hspace{1cm} (3-10)$$

$$N_{\text{ref}} = A_{N_{\text{ref}}} \times \left( \frac{T}{300} \right)^{-B_{N_{\text{ref}}}}, \hspace{1cm} (3-11)$$

$$v_s(T) = \frac{v_{\text{max},600K}}{1 + 0.8 \cdot \exp \left( \frac{T}{600} \right)}, \hspace{1cm} (3-12)$$
### Table 3-1. Parameters used in the models [109][115]

<table>
<thead>
<tr>
<th>Property</th>
<th>4H-SiC</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Electron</td>
<td>Electron</td>
</tr>
<tr>
<td>Breakdown electric field, $E_c$ (kV/cm)</td>
<td>2200</td>
<td>300</td>
</tr>
<tr>
<td>Relative dielectric constant, $\varepsilon_r$</td>
<td>10.1</td>
<td>11.9</td>
</tr>
<tr>
<td>Doping coefficient of $\mu$, $\alpha$</td>
<td>0.76</td>
<td>0.91</td>
</tr>
<tr>
<td>Electric field Exponent of $\mu$, $\beta$</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Coefficient of $\mu_{\text{max}}, A_{\mu_{\text{max}}}$</td>
<td>950</td>
<td>1350</td>
</tr>
<tr>
<td>Exponent of $\mu_{\text{max}}, B_{\mu_{\text{max}}}$</td>
<td>2.4</td>
<td>2.5</td>
</tr>
<tr>
<td>Coefficient of $\mu_{\text{min}}, A_{\mu_{\text{min}}}$</td>
<td>40</td>
<td>92</td>
</tr>
<tr>
<td>Exponent of $\mu_{\text{min}}, B_{\mu_{\text{min}}}$</td>
<td>0.5</td>
<td>0.91</td>
</tr>
<tr>
<td>Coefficient of $N_{\text{ref}}, A_{N_{\text{ref}}}$</td>
<td>$2 \times 10^{17}$</td>
<td>$1.3 \times 10^{17}$</td>
</tr>
<tr>
<td>Exponent of $N_{\text{ref}}, B_{N_{\text{ref}}}$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Maximum saturated velocity, $v_{\text{max}}$ (cm/s)</td>
<td>$4.77 \times 10^{17}$</td>
<td>$2.4 \times 10^{17}$</td>
</tr>
</tbody>
</table>

Similarly, for Si $pn$ diodes, the static loss is also dominated by the loss due to drift region resistance. The only difference is that Si $pn$ diodes are minority carrier bipolar devices. The mobility of holes must be considered when calculating the drift region resistance. Like electrons, the mobility of holes can be expressed by a set of equations with the same format as equations (3-7)-(3-12) [113], and the parameters involved are also listed in Table 3-1. Here, Si $pn$ diodes are considered instead of SiC Schottky diodes because Si Schottky diodes are limited by small voltage rating (<300V) and not used as widely as Si diodes are.

#### 2. Dynamic State

Although the reverse recovery current is much smaller for Schottky diodes than that of $pn$ diodes, the reverse recovery loss dominates its switching losses. So in this model,
the other losses are neglected and only reverse recovery loss is considered.

Figure 3-4 is the typical turn-off waveform of a diode. From the figure, the reverse recovery power loss during one switching period is [111]

\[ P_{rr} = f_s \cdot \frac{V_R I_R t_b}{2}. \]  \hspace{1cm} (3-13)

where

\[ S = \frac{t_b}{t_a}, \]  \hspace{1cm} (3-14)

\[ t_{rr} = t_a + t_b, \]  \hspace{1cm} (3-15)

\[ t_a = \left( \frac{1}{S + 1} \right) t_{rr}, \]  \hspace{1cm} (3-16)

\[ t_b = \left( \frac{S}{S + 1} \right) t_{rr}, \]  \hspace{1cm} (3-17)

\[ I_R = \frac{dI}{dt} \cdot t_a = \frac{dI}{dt} \cdot \frac{t_{rr}}{S + 1}. \]  \hspace{1cm} (3-18)

Substitute (3-14)-(3-18) into (3-13) to obtain

\[ P_{rr} = f_s \cdot \frac{V_R}{2S} \left( \frac{dI}{dt} \right) \left( \frac{St_{rr}}{S + 1} \right)^2. \]  \hspace{1cm} (3-19)

Voltage, current, and temperature dependency
Reverse recovery is the most important dynamic behavior of Schottky power diodes. Since there is no minority carrier injection in Schottky power diodes, the depletion layer capacitance determines their behavior during reverse recovery. When a reverse biased voltage $V_R$ is applied to a Schottky power diode, from well-known device theory [111], the width of its depletion layer can be calculated by

$$w_d = \sqrt{\frac{2\varepsilon (V_R + \phi_B)}{qN_d \varepsilon}}.$$  \hspace{1cm} (3-20)

Then, the specific depletion layer capacitance can be presented as

$$C_d = \frac{\varepsilon}{w_d} = \frac{qN_d \varepsilon}{\sqrt{2(V_R + \phi_B)}}.$$ \hspace{1cm} (3-21)

As shown by (3-21), $C_d$ is a strong function of $V_R$, but is not affected by the current flowing through it. That is to say, the switching loss of a SiC Schottky diode mainly depends on the reverse voltage. Thus, in system modeling, it is reasonable to model the reverse recovery charge of SiC Schottky diodes as a function of their reverse voltage. Specifically, the reverse-recovery charge increases almost linearly with $V_R^{0.5}$, and the energy loss during this period increases linearly with $V_R^{1.5}$.

Further, if the slight changes of $\varepsilon$ and $\phi_B$ with temperature are not considered, the reverse recovery behavior of SiC Schottky diodes will be the same at any temperature. This is also consistent with the test results in paper [117]. Thus, in system modeling, the influence of temperature on the reverse recovery characteristics of SiC Schottky diodes can be neglected.
Compared to SiC Schottky diodes, the switching loss of Si diodes during reverse recovery is much larger. This is because most of the Si diodes used in power applications have a \( p-n \) junction structure. For this type of diode, besides the depletion layer capacitance, there is an additional capacitance due to the minority carrier injection under reverse biased condition. As shown in [118], the injected minority carrier density in a reverse-biased \( p-n \) junction decreases approximately linearly through the distance \( w \) (shown in Figure 3-5) and becomes negligible at the edge of the junction. The total charge and the capacitance due to minority carrier injection can be therefore expressed as

\[
Q_I = \frac{J_F w}{2D_p}, \quad (3-22)
\]

\[
C_I = \frac{\partial Q_I}{\partial V_R} = \frac{J_F w}{D_p} \sqrt{\frac{\varepsilon(N_d + N_a)}{2qN_d N_a (V_R + \phi_R)}}, \quad (3-23)
\]

where \( N_d \) and \( N_a \) are the doping density in n-type and p-type regions, respectively. \( D_p \) is the diffusion constant of holes.

Figure 3-5. Injected minority carrier (holes) density vs. position in reverse-biased \( p-n \) junction.
In accordance with the above two equations, the capacitance due to minority carrier injection dominates the reverse recovery characteristic, especially for high current level. As a result, for Si diodes, the total charge swept out during turn off is more dependent on the forward current than the reverse voltage. Therefore, for a system with current changing from time to time, the influence of the forward current on the reverse recovery of Si diodes must be considered. This is one of the important factors that account for the larger power loss of Si diodes compared to SiC Schottky diodes.

Moreover, it should be noted that $D_p$ is a function of temperature and mobility of holes:

$$D_p = \frac{kT}{q}\mu_p.$$  \hfill (3-24)

Due to the dependence of $\mu_p$ on temperature as discussed previously, $Q_I$ increases as temperature increases. Consequently, the power loss during the reverse recovery of Si diodes increases with temperature, which is another reason for the large switching power losses in Si diodes.

### 3.1.2 Models for SiC JFETs

#### 1. Static state

The on-state resistance of SiC JFETs is mainly composed of channel resistance, substrate resistance, contact resistance, and drift region resistance. For high power devices, it is dominated by drift region resistance. Then the other components can be
neglected in the system simulation.

Like SiC Schottky diodes, SiC JFETs are also majority carrier devices. Their on-state resistances can be estimated by the same method with that of SiC Schottky diodes.

2. Dynamic state

An ideal inductive switching circuit as shown in Figure 3-6 is considered in this analytical model. A normally-on JFET is very similar to a MOSFET as far as the switching characteristics are concerned. Its equivalent circuit is identical to that of the MOSFET, and switching waveforms will be similar to that of a comparable MOSFET [111].

Figure 3-7(a) shows the simplified equivalent circuit of a normally-on JFET without considering all the parasitic inductors. This model also assumes that gate drive resistance, $R_G$, is 0, and the applied gate voltage, $V_G$, is a step signal changing from $V_{Gl}$ to $V_{GH}$ and vice versa. Then the Miller effect is minimized in the JFET, and the current rises and falls very quickly. The switching loss of the JFET can be assumed as the charging and discharging of the drain-to-source and drain-to-gate capacitance under the control of the
gate drive current [109]. Under these assumptions, the typical switching waveform of a JFET is as shown in Figure 3-7 (b).

During turn-on transition, the depletion layer capacitance \( C_d \) is discharged. The effective current is calculated by

\[
    J_{\text{eff}} = g_{ms} (V_{GH} - V_{th}) - J = (K_1 - 1)J, \]

where \( K_1 = g_{ms} (V_{GH} - V_{th}) / J \). Then,

\[
    \frac{dV(t)}{dt} = \frac{(K_1 - 1)J}{C_d(t)} \Rightarrow V(t) = \frac{[(K_1 - 1)J]^2}{2qN_d \varepsilon} t^2
\]

The discharging time of the depletion layer capacitance is

\[
    t_1 = \frac{Q_d}{I_{\text{eff}}} = \frac{\sqrt{2qN_d \varepsilon V}}{(K_1 - 1)J}.
\]

Therefore, the turn-on loss can be given by

\[
    E_{\text{on}} = \int_0^t J V(t) = \frac{1}{3(K_1 - 1)} \varepsilon E_c V \left( \frac{V}{V_B} \right)^{1/2}
\]

Figure 3-7. (a) Simplified equivalent circuit of a normally-on JFET,
(b) Typical switching waveform of a JFET under assumed conditions.
In the same way, during turn-off transition, the effective charging current is

\[ J_{\text{eff}} = g_{ms} (V_{th} - V_{GL}) - J = (K_2 + 1)J, \]  

(3-29)

where \( K_2 = g_{ms} (V_{th} - V_{GL}) / J \). Then,

\[ E_{\text{off}} = \frac{1}{3(K_2 + 1)} \varepsilon E_c V \left( \frac{V}{V_B} \right)^{1/2}. \]  

(3-30)

The total switching power loss of a JFET in one switching cycle is

\[ P_{J,\text{sw}} = f_s \left( E_{\text{on}} + E_{\text{off}} \right) = f_s \cdot \frac{1}{3} \varepsilon E_c V \left( \frac{V}{V_B} \right)^{1/2} \left[ \frac{1}{K_1 - 1} + \frac{1}{K_2 + 1} \right]. \]  

(3-31)

Since Si IGBTs are minority devices, their on-state resistance can be estimated using similarly to that of Si diodes. Unlike SiC JFETs, the voltage drop of Si IGBTs at zero current is non-zero. This is one factor that accounts for relatively large loss in Si IGBTs compared to SiC JFETs. Another reason is Si IGBTs have long tail current during turn-off transition. This has to be considered when estimating the switching loss of IGBTs.

Temperature dependency

The switching behaviors of SiC JFETs are mainly determined by their capacitances. Since the capacitances do not vary with the junction temperature, the switching power loss of SiC JFETs is almost independent of junction temperature. Examine equation (3-31). It can be found that the variation of threshold voltage and transconductance with temperature (as \[129\], they decrease approximately linearly with increasing temperature) can result in the slight change of the switching power loss. But this is usually neglected.
In this work, a standard 3-phase converter is considered, as shown in Figure 3-8. It is composed of six switches, each of which has an anti-parallel diode. The switches are driven by a three-phase PWM signal. Under a symmetrical load, the three phases are identical. The upper devices of each phase only conduct when the load currents are positive, while the lower devices only conduct when the load currents are negative. Moreover, at any time, only one of the two anti-parallel components is conducting. That means that each device can only conduct with a certain duty ratio, $D$, during a period of $\pi$ for a sinusoidal load current, and its anti-parallel device conducts complementarily with a duty ratio of $1-D$. Whether the switch or the diode conducts for more time is determined by the direction of the load current $i_L$. If the converter works as an inverter, the direction of $i_L$ is as shown in Figure 3-8, and the switch conducts more. While the converter works as a rectifier, the direction of $i_L$ is reversed, and the diode conducts more.

Based on above analysis, the total power loss of a converter is six times of the power
loss of one switch and diode pair. In order to improve the calculation efficiency, the power loss of each device is estimated as an average power loss in one fundamental cycle. This method has been proposed and proven to give a good estimation of converter behavior in [120-123]. In addition, different control strategies also affect the power loss of a converter. But the calculation method is essentially the same. This work takes a symmetrically-sampled-SPWM-controlled inverter as an example and presents derivation of models of each device.

3.2.1 Power loss models of SiC JFETs

Conduction and switching power losses of the SiC JFETs in a converter are calculated, and the additional power loss due to the reverse recovery of the diodes in the converter is also considered.

1. Conduction losses

As mentioned previously, only the conduction loss due to on-state resistance is considered. Thus, the conduction loss of SiC JFETs is

$$P_{J,\text{cond}} = I_{J,\text{rms}}^2 R_J.$$  \hspace{1cm} (3-32)

$I_{J,\text{rms}}$ are the effective current flowing in the JFET.

$$i = I \sin(\theta - \phi)$$  \hspace{1cm} (3-33)

Assume a sinusoidal load current represented by (3-33), its frequency is $f_0$. $\theta$ is equal to $2\pi f_0 t$, and $\varphi$ is the phase angle between voltage and current. The inverter switching frequency $f_s$ is far larger than $f_0$. So in each switching period, the current flowing in JFET
is approximately constant, which is calculated by (3-34).

\[ I_n = I \sin(\theta_n - \phi) = I \sin\left(\frac{2\pi n}{N} - \phi\right), \quad n = 0, 1, \ldots, N-1, \quad \text{and} \quad N = \frac{f_s}{f_0} \]  

By [120], \( I_{J,\text{rms}} \) can be found by

\[ I_{J,\text{rms}} = \sqrt{\frac{1}{N} \sum_{n=0}^{N-1} I_n^2 D_n} . \]  

(3-35)

\( D_n \) is the duty ratio in each switching period. As shown as Figure 3-9, it is

\[ D_n = \frac{t_{on}}{T_c} = \frac{T_s}{2} + 2x \quad \frac{T_c}{2} = \frac{V_{\text{control}}}{V_{\text{tri}}} \quad \frac{T_s}{4} \]  

\( = \frac{1}{2} + \frac{1}{2} M \sin \alpha \cdot \frac{1}{2} \left(1 + M \sin \theta_n\right), \]  

(3-36)

where \( M \) is the modulation index of PWM control. The upper JFET in an inverter only conducts when the load current is positive, that is, it conducts from \( \theta = \phi \) to \( \theta = \pi + \phi \).

Then

\[ \frac{\phi}{2\pi} \quad N < n < \frac{\pi + \phi}{2\pi} \quad N . \]  

(3-37)
Substitute (3-34) and (3-37) into (3-35) to get

\[ I_{J,\text{rms}} = I \sqrt{\frac{\pi + \phi}{2N} \sum_{n=-\frac{\pi}{2N}}^{\pi - \phi} \sin^2 \left( \frac{2\pi n}{N} - \phi \right) \left[ 1 + M \sin \left( \frac{2\pi n}{N} \right) \right]} . \tag{3-38} \]

Since \( f_s \gg f_0 \), (3-38) is approximately equal to (3-39).

\[ I_{J,\text{rms}} = I \sqrt{\frac{\pi + \phi}{4\pi} \int_{\phi}^{\pi} \sin^2 (\theta - \phi)(1 + M \sin \theta) d\theta = I \sqrt{\frac{1}{8} + \frac{1}{3\pi} M \cos \phi}} \tag{3-39} \]

Substitute (3-39) into (3-32) to get the expression for JFET conduction loss.

\[ P_{J,\text{cond}} = I^2 R_J \left( \frac{1}{8} + \frac{1}{3\pi} M \cos \phi \right) \tag{3-40} \]

In the same way, the total conduction loss of a Si IGBT in an inverter can be derived, which is shown as (3-41).

\[ P_{I,\text{cond}} = I^2 R_I \left( \frac{1}{8} + \frac{1}{3\pi} M \cos \phi \right) + IV_I \left( \frac{1}{2\pi} + \frac{1}{8} M \cos \phi \right) \tag{3-41} \]

2. Switching Losses

From (3-31), the switching loss in each switching period can be rewritten as

\[ P_{J,\text{sw}}(\theta_n) = H f_s \left( \frac{I \sin(\theta_n - \phi)}{G_1 - I \sin(\theta_n - \phi)} + \frac{I \sin(\theta_n - \phi)}{G_2 + I \sin(\theta_n - \phi)} \right), \tag{3-42} \]

where \( H = \frac{1}{3} \varepsilon E_c V_A \left( \frac{V}{V_B} \right)^{1/2}, \ G_1 = g_m (V_{GH} - V_{th}), \ G_2 = g_m (V_{th} - V_{GS}) \).

Therefore, the average power loss in one output fundamental period, \( T_0 \), is
For a Si IGBT, its switching loss model is very close to that of a SiC JFET, except for the loss due to the tail current during turn-off transition, corresponding to the third component in (3-44).

$$P_{J_{sw}} = \frac{1}{N} \sum_{n=0}^{N-1} P_{J_{sw}}(\theta_n)$$

$$\approx \frac{1}{2\pi} \int_{\theta}^{\pi+\phi} P_{J_{sw}}(\theta) d\theta$$

$$= \frac{Hf_s}{2\pi} \left[ \frac{G_1}{\sqrt{G_1^2-I^2}} \left( \pi + 2 \tan^{-1}\left( \frac{I}{\sqrt{G_1^2-I^2}} \right) \right) + \frac{G_2}{\sqrt{G_2^2-I^2}} \left[ -\pi + 2 \tan^{-1}\left( \frac{I}{\sqrt{G_2^2-I^2}} \right) \right] \right]$$

$$= \frac{Hf_s}{2\pi} \left[ \frac{G_1}{\sqrt{G_1^2-I^2}} \left( \pi + 2 \tan^{-1}\left( \frac{I}{\sqrt{G_1^2-I^2}} \right) \right) + \frac{G_2}{\sqrt{G_2^2-I^2}} \left[ -\pi + 2 \tan^{-1}\left( \frac{I}{\sqrt{G_2^2-I^2}} \right) \right] \right]$$

(3-43)

3. Loss due to the reverse recovery current of diodes

Besides the loss on a SiC JFET itself, the reverse recovery current of the diode connected to the JFET in the converter also contributes the losses of the SiC JFET during its turn-on period, as shown in Figure 3-10. In each switching period, the loss can be estimated by

$$P_{J_{sw}} = \frac{f_s}{2\pi} \left[ \frac{HG_1}{\sqrt{G_1^2-I^2}} \left( \pi + 2 \tan^{-1}\left( \frac{I}{\sqrt{G_1^2-I^2}} \right) \right) \right]$$

$$+ \frac{HG_2}{\sqrt{G_2^2-I^2}} \left[ -\pi + 2 \tan^{-1}\left( \frac{I}{\sqrt{G_2^2-I^2}} \right) \right] + k_i I^2 \cdot V \cdot t_{tail}$$

(3-44)

$$P_{J_{sw}} = \frac{f_s}{2\pi} \left[ \frac{HG_1}{\sqrt{G_1^2-I^2}} \left( \pi + 2 \tan^{-1}\left( \frac{I}{\sqrt{G_1^2-I^2}} \right) \right) \right]$$

$$+ \frac{HG_2}{\sqrt{G_2^2-I^2}} \left[ -\pi + 2 \tan^{-1}\left( \frac{I}{\sqrt{G_2^2-I^2}} \right) \right] + k_i I^2 \cdot V \cdot t_{tail}$$

Then the average power loss in one output fundamental period, $T_0$, is
Therefore, the total power losses of the SiC JFETs in a converter is equal to

\[ P_J = P_{J,\text{cond}} + P_{J,\text{sw}} + P_{J,\text{D}}. \] (3-47)

### 3.2.2 Power loss models of SiC Schottky diodes

1. Conduction losses

As discussed previously, the conduction loss of the SiC Schottky diode is given by (3-6). The current, \( I_{D,\text{rms}} \) and \( I_{D,\text{ave}} \), can be computed in the same way with that of the SiC JFET. The only difference is that the duty ratio of the diode is \( 1-D_n \) because it only
conduits when the JFET is off.

**Calculation of** $I_{D,\text{rms}}$

$$I_{D,\text{rms}} = \sqrt{\frac{1}{N} \sum_{n=0}^{N-1} I_n^2 (1 - D_n)}$$

$$\approx I \sqrt{\frac{1}{4\pi} \int_{\phi}^{\pi+\phi} \sin^2 (\theta - \phi) (1 - M \sin \theta) d\theta} = I \sqrt{\frac{1}{8} - \frac{1}{3\pi} M \cos \phi}$$

(3-48)

**Calculation of** $I_{D,\text{ave}}$

$$I_{D,\text{ave}} = \frac{1}{N} \sum_{n=0}^{N-1} I_n (1 - D_n)$$

$$\approx I \frac{1}{4\pi} \int_{\phi}^{\pi+\phi} \sin (\theta - \phi) (1 - M \sin \theta) d\theta = I \left( \frac{1}{2\pi} - \frac{1}{8} M \cos \phi \right)$$

(3-49)

**Total conduction loss of a SiC Schottky diode in an inverter**

$$P_{D,\text{cond}} = I^2 \cdot R_D \left( \frac{1}{8} - \frac{1}{3\pi} M \cos \phi \right) + I \cdot V_D \cdot \left( \frac{1}{2\pi} - \frac{M \cos \phi}{8} \right)$$

(3-50)

For a Si diode, its conduction loss model has the same expression with (3-50).

2. Switching Losses

The average switching loss $P_{sw}$ in one switching period of the SiC Schottky diode has been derived in 3.1.1. Like the SiC JFETs, they only conduct in one direction. For a sinusoidal current, the diodes only conduct for half period $\pi$. Thus, the average power loss in one output fundamental period, $T_0$, is

$$P_{D,\text{sw}} = \frac{1}{N} \sum_{n=0}^{N-1} P_{sw} = \frac{1}{2\pi} \int_{\phi}^{\pi+\phi} f_s V \frac{d(I)}{dt} \left( \frac{St_{rr}}{S+1} \right)^2 d\theta = f_s V \frac{d(I)}{dt} \left( \frac{St_{rr}}{S+1} \right)^2.$$  

(3-51)

In practice, a set of reverse recovery parameters must be available either by test or datasheet. Then, a reference switching power loss at a certain reverse voltage is obtained
As discussed in 3.1.1, the switching loss of a SiC Schottky diode is a function of its reverse voltage $V$, which is approximately positively proportional to $V^{1.5}$. Thus, the switching loss of a SiC Schottky diode at any reverse voltage can be expressed as

$$P_{D,sw} = \left( \frac{V}{V_0} \right)^{1.5} \times P_{D,sw0} = f_s \frac{V}{4S} \sqrt{\frac{V}{V_0}} \left( \frac{dI}{dt} \right) \left( \frac{St_{rr}}{S+1} \right)^2.$$  \hspace{1cm} (3-53)

For Si diode, the reverse recovery characteristic is more complex, which varies nonlinearly with current, voltage, and temperature. To simplify the problem, in this work, the dependencies on these parameters are assumed to be linear.

### 3.3 Thermal system models

The method used to study thermal phenomena can be classified into two groups. One is called relaxation method that combined 3-D FEM with electrical simulator (SPICE, etc). The other is the direct method, which computes thermal information based equivalent circuit. The latter is more suited for system simulation.

Figure 3-11 and Figure 3-12 are two classical equivalent circuits of junction-case thermal problem. The circuit in Figure 3-11 is based on a finite difference discretization (FDM) of heat equation [124]. Figure 3-12 is also proposed in several papers [125-127], and used by some manufacturers [128]. It has a simple RC parallel block structure.
Therefore, the impedance equation is presented as (3-54).

\[
Z_{jc}(s) = \frac{R_1}{1 + s\tau_1} + \frac{R_2}{1 + s\tau_2} + \cdots + \frac{R_n}{1 + s\tau_n}
\]  

(3-54)

where \(\tau_i = R_iC_i\), and the junction-case thermal resistance \(R_{jc} = \sum_{i=1}^{n} R_i\). This model is suitable for simulation because it has a diagonal Jordan form in state space representation with real different negative eigenvalues. By [125], \(n=2\), \(R_1=R_2\), and \(\tau_1=10\text{ms}\), \(\tau_2=70\text{ms}\) can give a good approximation for most circuit. It can be solved by using the Transfer function in Matlab Simulink; refer to the diagram in Figure 3-13.

Using the equivalent circuit in Figure 3-12 as a basic element, the thermal equivalent circuit of a converter can be drawn as Figure 3-14. In the figure, \(P_{j}(t)\) and \(P_{d}(t)\) are
Figure 3-13. Transfer function diagram of equation (3-54) in Matlab Simulink.

Figure 3-14. Thermal equivalent circuit of a converter.
the total power losses generated by a SiC JFET and a SiC Schottky diode, respectively. Assume the SiC JFET and the SiC Schottky diode are mounted on the same heatsink. Then the power losses \( P_j(t) \) and \( P_d(t) \) flow through separate ways from their own junction to case, where the temperatures are equal for contacting to the same heatsink. This forms two separate thermal loops, as shown as Figure 3-14. Afterwards, they merge with each other \( (P_j(t)+P_d(t)) \) and flow together through the heat sink to atmosphere. \( R_{jjc} = \sum_{i=1}^{n} R_{jj_i} \) is the junction-case thermal resistance of the SiC JFET, and \( R_{djc} = \sum_{i=1}^{n} R_{dj_i} \) for the SiC Schottky diode. \( R_{ch} \) and \( R_{ha} \) are the thermal resistance of thermal grease and heatsink, respectively. If all devices are on the same heatsink, the total power loss flowing through the heatsink should be \( 6 \times (P_j(t)+P_d(t)) \).

The transfer function of each branch can be expressed as (3-55)-(3-57).

**SiC JFETs junction to case:**

\[
Z_{jjc}(s) = \frac{R_{j1}}{1+st_{j1}} + \frac{R_{j2}}{1+st_{j2}} + \cdots + \frac{R_{jn}}{1+st_{jn}}, \tag{3-55}
\]

**SiC Schottky diodes junction to case:**

\[
Z_{djc}(s) = \frac{R_{d1}}{1+st_{d1}} + \frac{R_{d2}}{1+st_{d2}} + \cdots + \frac{R_{dn}}{1+st_{dn}}, \tag{3-56}
\]

**Case to ambient:**

\[
Z_{ca}(s) = \frac{R_{ch}}{1+st_{ch}} + \frac{R_{ha}}{1+st_{ha}}. \tag{3-57}
\]

58
The corresponding transfer function diagram in Matlab Simulink is shown in Figure 3-15.

3.4 Summary

The model equations derived in this chapter are summarized as follows:

1. Analytical device models:

   On-state resistance:

   \[ R_D = \frac{4V^2}{\varepsilon E_c^3 \mu_n} \]  \hspace{1cm} (for majority devices) \hspace{1cm} (3-58)

   \[ R_D = \frac{4V^2}{\varepsilon E_c^3 \left( \mu_n + \mu_p \right)} \]  \hspace{1cm} (for minority devices) \hspace{1cm} (3-59)

   \[ \mu(E) = \frac{\mu_0}{1 + \left( \frac{\mu_0 E}{v_s} \right)^{1/\beta}} \]  \hspace{1cm} (3-60)

   \[ \mu_0 = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left( \frac{N_{\text{tot}}}{N_{\text{ref}}} \right)^\alpha} \] \hspace{1cm} (3-61)

   \[ \mu_{\max} = A_{\mu_{\max}} \times \left( \frac{T}{300} \right)^{-B_{\mu_{\max}}} \]  \hspace{1cm} (3-62)

   \[ \mu_{\min} = A_{\mu_{\min}} \times \left( \frac{T}{300} \right)^{-B_{\mu_{\min}}} \]  \hspace{1cm} (3-63)

   \[ N_{\text{ref}} = A_{N_{\text{ref}}} \times \left( \frac{T}{300} \right)^{-B_{N_{\text{ref}}}} \]  \hspace{1cm} (3-64)
Figure 3-15. Transfer function diagram of a converter thermal system in Matlab Simulink.
\[
V_s(T) = \frac{V_{\text{max},600K}}{1 + 0.8 \cdot \exp\left(\frac{T}{600}\right)}.
\]  

(3-65)

The coefficients in these equations are given in Table 3-1. The other models related to the characteristics resulting in power loss have been integrated into power loss models.

2. Mathematical power loss models of converters

SiC converter:

\[
P_{\text{Con, SiC}} = 6 \times (P_{J,\text{cond}} + P_{J,\text{sw}} + P_{J\leftarrow D} + P_{D,\text{cond}} + P_{D,\text{sw}})
\]  

(3-66)

\[
P_{J,\text{cond}} = I^2 R_J \left( \frac{1}{8} + \frac{1}{3\pi} M \cos \phi \right)
\]  

(3-67)

\[
P_{J,\text{sw}} = \frac{Hf_I}{2\pi} \left\{ \frac{G_1}{\sqrt{G_1^2 - I^2}} \left[ \pi + 2 \tan^{-1}\left( \frac{I}{\sqrt{G_1^2 - I^2}} \right) \right] 
\]  

\[
+ \frac{G_2}{\sqrt{G_2^2 - I^2}} \left[ -\pi + 2 \tan^{-1}\left( \frac{I}{\sqrt{G_2^2 - I^2}} \right) \right] \right\}
\]  

(3-68)

\[H = \frac{1}{3} \varepsilon E_c VA \left( \frac{V}{V_B} \right)^{1/2} \ G_1 = g_m (V_{GH} - V_{ih}) \ G_2 = g_m (V_{ih} - V_{GL})
\]

\[
P_{J\leftarrow D} = f_s \left[ \frac{VI_{tr}}{\pi (S+1)} + \frac{V}{4 \sqrt{V_0}} \left( \frac{dI}{dt} \right) t_{tr}^2 \left( S+1 \right)^2 \right]
\]  

(3-69)

\[
P_{D,\text{cond}} = I^2 \cdot R_D \left( \frac{1}{8} + \frac{1}{3\pi} M \cos \phi \right) + I \cdot V_D \cdot \left( \frac{1}{2\pi} + \frac{M \cos \phi}{8} \right)
\]  

(3-70)

\[
P_{D,\text{sw}} = \left( \frac{V}{V_0} \right)^{1.5} \ P_{D,\text{sw}0} = f_s \frac{V}{4S \sqrt{V_0}} \left( \frac{dI}{dt} \right) \left( \frac{St_{tr}}{S+1} \right)^2
\]  

(3-71)
Si converter:

\[ P_{\text{Con, Si}} = 6 \times \left( P_{\text{I, cond}} + P_{\text{I, sw}} + P_{\text{I\kappa D}} + P_{\text{D, cond}} + P_{\text{D, sw}} \right) \]  
(3-72)

\[ P_{\text{I, cond}} = I^2 R_I \left( \frac{1}{8} \pm \frac{1}{3\pi} M \cos \phi \right) + I V_i \left( \frac{1}{2\pi} \pm \frac{1}{8} M \cos \phi \right) \]  
(3-73)

\[ P_{\text{I\kappa D}} = f_s \left[ \frac{V I_{tr} + V \left( \frac{dI}{dt} \right) t_{rr}}{4 (S + 1)} + \frac{\sin \phi}{\sin \phi} \right] \]  
(3-74)

\[ P_{\text{J, sw}} = \frac{f_s}{2\pi} \left\{ \frac{\sqrt{G_1^2 - I^2}}{I} \left[ \pi + 2 \tan^{-1} \left( \frac{I}{\sqrt{G_1^2 - I^2}} \right) \right] \right. \right. \]  
(3-75)

\[ + \frac{\sqrt{G_2^2 - I^2}}{I} \left[ -\pi + 2 \tan^{-1} \left( \frac{I}{\sqrt{G_2^2 - I^2}} \right) \right] + k_i I V \cdot t_{\text{tail}} \right\} \]

\[ P_{\text{D, cond}} = I^2 \cdot R_D \left( \frac{1}{8} \mp \frac{1}{3\pi} M \cos \phi \right) + I \cdot V_D \cdot \left( \frac{1}{2\pi} \mp \frac{M \cos \phi}{8} \right) \]  
(3-76)

\[ P_{\text{D, sw}} = f_s \cdot \frac{V \left( \frac{dI}{dt} \right) \left( \frac{S t_{rr}}{S + 1} \right)^2}{4S} \]  
(3-77)

Note: in equation (3-67), (3-70), (3-73), (3-76), the ‘+’ is for an inverter, and ‘-‘ is for a rectifier.

3. Equivalent circuit based thermal system models

The equivalent thermal circuit for a converter is shown in Figure 3-14. The mathematical expressions in frequency domain are

SiC JFETs junction to case:

\[ Z_{\text{jjc}}(s) = \frac{R_{j1}}{1 + s \tau_{j1}} + \frac{R_{j2}}{1 + s \tau_{j2}} + \cdots + \frac{R_{jn}}{1 + s \tau_{jjn}} \]  
(3-78)
SiC Schottky diodes junction to case:

\[
Z_{djc}(s) = \frac{R_{dj1}}{1 + s\tau_{dj1}} + \frac{R_{dj2}}{1 + s\tau_{dj2}} + \cdots + \frac{R_{djn}}{1 + s\tau_{djn}},
\]  
(3-79)

Case to ambient:

\[
Z_{ca}(s) = \frac{R_{ch}}{1 + s\tau_{ch}} + \frac{R_{ha}}{1 + s\tau_{ha}}.
\]  
(3-80)
CHAPTER 4

Experimental verification

Experimental verification of a model compares model simulation against test data to ensure the model file is complete and correct for intended use. In this chapter, the verification has been conducted at both single device level and converter level. Device and inverter tests were done, and compared to simulation results. As a supplement to the analytical models, some test results are used to correct simulation parameters, or provide empirical approximation to the influence of some parameters that are not included in the models.

4.1 Single device tests and simulations

This section has three parts. First, the test circuits and equipments are described. Then test results are presented. Finally, simulation results are compared to test results in order to validate the models in chapter 3.

4.1.1 Test circuits and equipments

In this work, devices are tested for both static characteristics and dynamic characteristics from room temperature to high temperature (mostly 150 °C and some up to 300 °C).
1. Static tests

Static tests include forward and transfer characteristics (for switches). Curve tracer Tektronix 371B shown in Figure 4-1 (a) is the commonly used tool. It can automatically draw the test curves and record data at room temperature. In order to get high temperature results, the devices are put into the oven shown in Figure 4-1 (b), which can raise the ambient temperature up to 300 °C.

2. Dynamic tests

In dynamic tests, switching characteristics are tested, and for diodes, especially the reverse recovery characteristics. The test circuits used are drawn in Figure 4-2. Figure 4-2 (a) is for diode tests. It has an $RL$ load. The value of $V_{dc}$ and $R$ determine the maximum current flowing through the diode. $L$ should be large enough to sustain the current until the switch turns on again. Figure 4-2 (b) is for switch (JFET, MOSFET) tests. It has a
pure inductive load, and the switch is controlled by a double-pulse signal. The current in the switch is controlled by tuning the duty ratio of the first pulse. In addition, due to no high temperature gate drive available for these devices, the gate drive circuit can not be put into the oven together with the devices. To avoid the long wire for gate drive signal, a small thermal box (see Figure 4-3) is built instead of the oven. The inside temperature is controlled by the amount of power loss dissipation of the resistors mounted inside the box. The maximum temperature this box can control is around 150 °C.

Figure 4-2. Switching characteristics test circuit.

Figure 4-3. Thermal box used in tests.
4.1.2 Test results

In this section, test results of SiC Schottky diode, Si diode, SiC JFET, SiC MOSFET, and Si MOSFET are shown and discussed.

1. Tests of the SiC Schottky diodes and Si diodes

   (a) Forward characteristics

   A SiC Schottky diode (Cree, 600V/4A) was tested for forward characteristics at a temperature range from 0 °C to 175 °C. As shown in Figure 4-4 (a), its on-state resistance increases from 0.159 Ω at 25 °C to 0.326 Ω at 150 °C. Figure 4-4 (b) compares the SiC Schottky diode to the Si \textit{pn} diode with the same rating (600V/10A) at room temperature. The on-state resistance of SiC Schottky diode is 40.6% of that of Si \textit{pn} diode. Other devices tested are presented in Figure 4-5.

   The SiC Schottky diode shown in Figure 4-4 is an up-to-date device. It is also
compared to the same device tested several years ago. As shown in Figure 4-6, the on-state resistance has been reduced by about 24%.

(b) Reverse recovery

SiC Schottky diodes from different manufacturers and Si diodes were tested. Several important conclusions of reverse recovery behaviors can be drawn from the test results.

**SiC Schottky diode reverse recovery**

- Independent of temperature (Figure 4-7 and Figure 4-8)
- Not influenced by forward current (Figure 4-9)
- Vary with the reverse voltage, $V_R$, as discussed in 3.1.1, the capacitance charge $Q_c \propto V_R^{0.5}$. Tests in Figure 4-10 and Figure 4-11 verified this argument. In Figure 4-10,
Reverse recovery current of SiC Schottky diode (600V/4A) at different temperatures

![Graph of reverse recovery current](image)

Figure 4-7. SiC Schottky diode reverse recovery waveforms at different temperatures.

On-state resistance of SiC diodes (600V/4A) at different temperatures

![Graph of on-state resistance](image)

Voltage drop at zero current of SiC diodes (600V/4A) at different temperatures

![Graph of voltage drop at zero current](image)

Figure 4-6. Comparison of up-to-date SiC diode and its old version.
Figure 4-8. Reverse recovery waveforms of the SiC Schottky diode with high-temperature package at different temperatures (up to 300 °C).

Figure 4-9. SiC Schottky diode reverse recovery waveforms at different currents.
Figure 4-10. SiC Schottky diode reverse recovery waveforms at different voltages.

Figure 4-11. SiC Schottky diode reverse recovery waveforms at different voltages.
• $350V/150V=1.452$, and $Q_{c,350V}/Q_{c,150V}=350\text{nc}/241\text{nc}=1.449$. In Figure 4-11, $250V/150V=1.118$, and $Q_{c,350V}/Q_{c,150V}=21\text{nc}/18.8\text{nc}=1.117$.

• Power loss in this period is far less than that of Si diodes (Figure 4-12 and 4-13).

Si diode reverse recovery

• Affected by temperature nonlinearly (Figure 4-14)

• Changing with both forward current and reverse voltage (Figure 4-15 and Figure 4-16)

• As the current increases, the power loss approximately increases linearly (Figure 4-17).

![Reverse recovery waveforms for SiC and Si diodes with similar ratings](image)

Figure 4-12. Reverse recovery waveforms for SiC and Si diodes with similar ratings (SiC 1200V/10A, Si 800/10A).
Figure 4-13. Reverse recovery losses of the diodes tested.

Figure 4-14. Si diode reverse recovery loss vs. temperature at different currents.
Si diode reverse recovery at different voltages (800V/20A)

Figure 4-16. Si diode reverse recovery waveforms at different voltages.

Si diode reverse recovery waveforms at different currents (800V/20A)

Figure 4-15. Si diode reverse recovery waveforms at different currents.
2. Tests of SiC JFETs

(a) Forward characteristics

A SiC JFET (1200V/2A, SiCED) was tested for forward characteristics at a temperature range from -50 °C to 175 °C, as shown in Figure 4-18 (a). Its on-state resistance increases from 0.365 Ω at -50 °C to 1.401 Ω at 175 °C (Figure 4-18 (b)).

A SiC JFET (600V/5A) from SemiSouth was tested for forward and transfer characteristics. Unlike the SiC JFET from SiCED, its current saturates quickly as temperature increases especially above 100 °C (see Figure 4-19 (a)), which results in higher resistance at high temperature than what is expected (Figure 4-19(b)) and degrades the device rating. The transconductance and the threshold voltage of the SiC JFET are

Figure 4-17. Si diode reverse recovery loss vs. current at different temperatures.
also affected by temperature. Both of them decrease with temperature (Figure 4-19 (c) and (d)).

A quasi-off SiC JFET from SemiSouth was also tested for forward and transfer characteristics. Its threshold voltage is 0.75V as shown in Figure 4-20 (b), and the suggested gate voltage is -5V to 3V.

(b) Switching characteristic

To do switching tests, a gate driver circuit is necessary. Since the SiC JFETs under testing are normally-on devices, a special design is required. In this work, a conventional gate driver IC for Si MOSFET/IGBTs is used. Due to the high turn-off voltage, the gate driver IC should have a high voltage rating. For example, if the SiC JFET is turn on by 3V and turn off by -25V, the gate driver IC should have a voltage rating of at least 28V.
Fig. 4-19. Static characteristics of the SiC JFET (Normally-on, Semisouth).
Figure 4-20. Static characteristics of the SiC JFET (Quasi-off, SemiSouth).
A gate driver IC IXDD414 is used in this work. The design is shown in Figure 4-21.

SiC JFETs (600V/5A) from SemiSouth were tested with a dc voltage of 200 V and current from 1 A to 5 A at 25 °C, 50 °C and 150 °C. As shown as Figure 4-22 (a), the JFET has acceptable performance at 2 A and 25 °C. But as current and temperature increase, some noise related to device quality occurs. At 25 °C, it started from 3 A, and 2 A for 75 °C. Finally, the device was killed at 3 A and 75 °C. This indicates that the rating of the device is far less than 5 A. As shown as Figure 4-19 (a), its rating is about 1 A.

Some bare chips of SiC JFETs (1200V/7A) and SiC diodes from SiCED (1200V/15A) shown in Figure 4-23 (a) were made into a power module (Figure 4-23 (b)). However, due to the bonding wire, the power module did not function at all. Only limit tests were done on these devices. Figure 4-24 shows the switching waveform of the SiC JFET.
Figure 4-22. Dynamic characteristics of the SiC JFET (Normally-on, SemiSouth).

(a) 2 A @ 25 °C                                           (b) 5 A @ 25 °C
(c) 2 A @ 75 °C                                           (b) 3 A @ 75 °C
Figure 4-23. SiC JFETs from SiCED.

Figure 4-24. Switching characteristics of the SiC JFET (SiCED).
3. Tests of SiC MOSFET and Si MOSFET

A SiC MOSFET (Cree, 800V/10A) was tested and compared to a Si MOSFET (FairChild, 600V/13A).

(a) Static tests

The SiC and Si MOSFETs were tested for forward characteristics at a temperature range from 25 °C to 150 °C. The results are shown in Figs. (4-25)-(4-27). As expected, the SiC MOSFET has lower on-state resistance for most of the temperature range. But, unlike the Si MOSFET, the on-state resistance of the SiC MOSFET decreases as temperature increases at middle temperature range (about < 150 °C) (Figure 4-27 (a)), then increases at high temperature range (> 150 °C). A good explanation for this is that the relative large channel resistance in the SiC MOSFET. So the channel resistance of the SiC MOSFET can not be neglected in device modeling [130]. The models presented in the previous chapter have to be modified to use for the SiC MOSFET. As for transfer characteristic, the threshold voltages decrease with temperature, and it is approximately linear as shown in Figure 4-27 (b).

(b) Dynamic tests

The switching loss of the SiC MOSFET was tested at different currents and temperatures. The switching waveform is shown in Figure 4-28. The switching losses calculated from test results are plotted in Figure 4-29 and Figure 4-30. As shown in Figure 4-29, both turn-on loss and turn-off loss increase with increasing current. For a
Figure 4-25. Characteristics of the SiC MOSFET (Cree, 800V/10A).

Figure 4-26. Characteristics of the Si MOSFET (FairChild, 600V/13A).
Figure 4-27. Comparison of the SiC and Si MOSFETs.

Figure 4-28. Switching waveform of the SiC MOSFET (Cree, 800V/10A).
SiC MOSFET Switching Loss at T=25°C

(a) At 25 °C

(b) At 125 °C

Figure 4-29. Switching loss of the SiC MOSFET at different currents.

SiC MOSFET Turn-on Loss

(a) Turn on

SiC MOSFET Turn-off Loss

(b) Turn off

Figure 4-30. Switching loss of the SiC MOSFET at different temperatures.
certain current value, the switching losses slightly decrease with temperature increasing (Figure 4-30). Comparing Figure 4-30 (a) to (b), the tendency of turn-on loss is more obvious. This is because the threshold voltage, the major factor affected by temperature, influences turn-on behavior more than that of turn-off.

4.1.3 Comparison of test results and simulation results

1. SiC Schottky diodes

(a) Simulate the forward characteristic of the SiC Schottky diode (1200V/10A, Cree)

The basic model equation is (3-3). It converts to the Matlab Simulink model shown in Figure 4-31. The Ron block calculates the diode on-state resistance based on the equations (3-4)-(3-12) using the parameters listed in Table 3-1. Comparing the simulation curve to the test curve, a good match is achieved as shown in Figure 4-32 (a).

Figure 4-31. Matlab Simulink block for computing diode forward characteristic.
(b) Simulate the on-state resistance of Cree SiC diodes at different temperatures.

Using the same method, the on-state resistances of three Cree SiC diodes (CSD05120, CSD10120, and CSD10060) are studied and compared to the values provided in datasheets. An acceptable accuracy is obtained, see Figure 4-32 (b).

2. SiC JFETs

(a) Simulate the forward characteristic of the SiC JFET (1200V/2A, SiCED)

The on-state resistance of the SiC JFET was simulated using the same method shown in Figure 4-31. Again, a good match between the test and the simulation is achieved (refer to Figure 4-33).

(b) Simulate the forward characteristic of the SiC JFET (600V/5A, SemiSouth)

The switching loss of the SiC JFET was calculated using equation 3-28 and 3-30.
The threshold voltage and transconductance were expressed as the functions of temperature based on the curve-fitting of the test results in Figure 4-19. The switching losses at 200V and 3A are plotted verses temperature in Figure 4-34. The simulation results are very close to the test results at the test points.

4.2 Hybrid inverter tests and simulations

A hybrid inverter (Si IGBT/SiC Schottky diode) and a comparable Si inverter were built and tested with $RL$ load at different voltage, current, and switching frequency. Power losses of the inverter were also estimated using the system modeling presented in chapter 3 under the specific test conditions. The details are presented below.

4.2.1 Inverter layout

The SiC/Si hybrid inverter is shown in Figure 4-35. It is composed of 3 hybrid modules, each of them is driven by a BG2A board (from POWEREX), which used two VLA502-01 gate drivers. In addition, the dc bus capacitors and snubbers are also integrated in the inverter. All these components are mounted on a heatsink with fans. The characteristics of the modules are plotted in Figure 4-36. Other components used are listed in Table 4-1. For the purpose of comparison, a Si inverter is also built by substituting the hybrid IGBT modules for the Si IGBT modules with the same package.
Table 4-1. Component list of the hybrid or Si inverter

<table>
<thead>
<tr>
<th>Name</th>
<th>Number</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hybrid IGBT module</td>
<td>3</td>
<td>1200V/300A, Cree, QID1230009-ES</td>
</tr>
<tr>
<td>Si IGBT module</td>
<td>3</td>
<td>1200V/300A, Powerex, CM300DY-24NF</td>
</tr>
<tr>
<td>Gate driver</td>
<td>6</td>
<td>Powerex, VLA502-01</td>
</tr>
<tr>
<td>Capacitor</td>
<td>4</td>
<td>450V, 5600μF</td>
</tr>
<tr>
<td>Snubber</td>
<td>3</td>
<td>PMC, 600V, 9.0μF, 10%, S4</td>
</tr>
</tbody>
</table>

Figure 4-33. Comparison of test and simulation results for the SiC JFET.

Figure 4-34. Comparison of test and simulation results for the SiC JFET.
Figure 4-35. Hybrid inverter (Si IGBT/SiC Schottky diode).

Figure 4-36. Characteristics of the IGBT modules at room temperature.
4.2.2 Experiment system setup

As shown in Fig. 4-37, the converter is connected to a DC power supply and has a 3-phase RL load. It is controlled by SVPWM signals generated by a DSP board (TMS320F2812). The control program developed in Matlab Simulink (shown in Figure 4-38) can be directly downloaded to the DSP chip by using DSP toolbox in Matlab. The input DC voltage and current and 3-phase output voltage and current are measured by Yokogawa PZ4000. Then, the power loss of the inverter is the difference between the input and output power. The experimental system setup is shown in Figure 4-39.

![Figure 4-37. Inverter test system layout.](image)
Figure 4-38. Control program developed in Matlab Simulink.

Figure 4-39. Experiment system setup.
Table 4-2. Inverter test conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC voltage, V</td>
<td>200, 325</td>
</tr>
<tr>
<td>AC current(rms), A</td>
<td>10, 20, 30, 40, 50</td>
</tr>
<tr>
<td>Switching frequency, kHz</td>
<td>5, 10, 15</td>
</tr>
<tr>
<td>Output frequency of AC current, Hz</td>
<td>25, 50, 75, 100</td>
</tr>
</tbody>
</table>

4.2.3 Experiment results and discussion

In order to study the impact of different parameters such as voltage, current, switching frequency, and the frequency of output current on the efficiency of the inverters, a series of tests were designed. Specific test conditions are summarized in Table 4-2.

Figure 4-40 shows the experimental control and gate drive signals. Under SVPWM control, the output voltage is shown as Figure 4-41, which has a sinusoidal fundamental waveform, while the output current is a sine wave (Figure 4-42).

The efficiency of the hybrid and Si inverters were calculated for each test. The results are plotted in Figure 4-43 and Figure 4-44.

Discussion

1. The efficiencies of both inverters increase as output power increases (Figure 4-43 and Figure 4-44) and decrease as switching frequency increases as expected (Figure 4-45). Specifically, from 5 kHz to 10 kHz, the efficiency of the hybrid inverter deceased by 1.78%, and decreased by 3.78% from 10 kHz to 15 kHz.
Figure 4-40. Control and gate drive signals

Figure 4-41. AC side output voltage

Figure 4-42. Ac side output current
(a) Dc voltage 200V and output frequency 25Hz

(b) Dc voltage 200V and output frequency 50Hz
(c) Dc voltage 200V and output frequency 75Hz

(d) Dc voltage 200V and output frequency 100Hz

Figure 4-43. Efficiency vs. Output power at 200V dc voltage
\( f_0 = 25\text{Hz}, \quad V_{dc} = 325\text{V}, \quad f_s = 5\text{kHz} \)

\( f_0 = 25\text{Hz}, \quad V_{dc} = 325\text{V}, \quad f_s = 10\text{kHz} \)

\( f_0 = 25\text{Hz}, \quad V_{dc} = 325\text{V}, \quad f_s = 15\text{kHz} \)

\( f_0 = 50\text{Hz}, \quad V_{dc} = 325\text{V}, \quad f_s = 5\text{kHz} \)

\( f_0 = 50\text{Hz}, \quad V_{dc} = 325\text{V}, \quad f_s = 10\text{kHz} \)

\( f_0 = 50\text{Hz}, \quad V_{dc} = 325\text{V}, \quad f_s = 15\text{kHz} \)

(a) Dc voltage 325V and output frequency 25Hz

(b) Dc voltage 325V and output frequency 50Hz
(c) Dc voltage 325V and output frequency 75Hz

(d) Dc voltage 325V and output frequency 100Hz

Figure 4-44. Efficiency vs. Output power at 325V dc voltage.
2. At low power level, the efficiency of Si/SiC hybrid inverter is close to that of Si inverter. The conduction loss due to the voltage drop at zero current is larger for the SiC carbide diode due to relatively high value of the voltage drop at zero current (Figure 4-36 (c)). But the on-state resistance of the SiC Schottky diode is far smaller than that of the Si diode, and the switching losses of the two diodes are both small at low current level. Thus, the total power losses of the diodes are pretty close, and in some situations, Si/SiC hybrid inverter may have lower efficiency than the Si inverter (like Figure 4-43 (b, d)). In addition, since the efficiencies of these two inverters are so close in lower power level, the measurement error may account for some variations of the relationship between the two efficiencies.

3. The efficiency of the Si/SiC hybrid inverter is higher than that of the Si inverter at high power level. The difference between the efficiency of these two inverters becomes
larger as output power increases. This is because the power losses of the Si inverter increase more quickly as the output power (or current) increases. In some sense, the hybrid inverter is more competitive in high power application.

4. In order to examine how much power is saved by using SiC Schottky diodes instead of Si diodes, the power losses saved by Si/SiC hybrid inverter are also presented as a percentage of the power losses of the Si inverter. For all test condition, the average power loss reduction in the hybrid inverter is about 8% - 24% of the total power loss of the Si inverter.

4.2.4 Comparison of test results and simulation results

Using the IGBT models and Schottky diode models presented in chapter 3, the power loss of the hybrid inverter at 325V DC voltage and 50Hz output frequency was estimated. The parameters used in the simulation are based on test or manufacturer datasheet [131-134].

The Matlab simulation program is shown in Figure 4-46. Three different switching frequencies were studied. Comparing the simulated inverter efficiency to test values, it is found that the simulation results fit the test results very well for most of the test points, and only deviate at the low current level (compared to the device rating 300A, see Figure 4-47). This indicates that the modeling method presented in chapter 3 is effective and accurate for inverter applications.
Figure 4-46. Matlab Simulink program for calculation of SiC inverter efficiency.
Figure 4-47. Comparison of calculated inverter efficiency and test values (325V DC voltage and 50 Hz output frequency).
4.3 Summary

SiC power devices and a hybrid converter were tested and characterized. They are proven to be superior to the comparable Si counterparts, and their quality has been improved since initial devices were produced. In addition, the comparisons of test data and simulation results indicate that the models presented in chapter 3 are effective and accurate. Some test results are also used as model parameters in the studies in the next chapter.
CHAPTER 5

System-level evaluation of SiC-based converters for different applications

System-level modeling of a SiC power system is presented in chapter 3, and verified with some experimental results in chapter 4. This chapter will be the applications of this method. That is, use simulations based on the system models to study the system impact (efficiency, temperature profile) of a SiC-based converter on potential application systems. Four proposed application systems are presented here, and operation, simulation setup, and results of each application will be discussed one by one in the following parts.

5.1 Navy’s motion control application

A motion control diagram for a naval gun turret positioning system is shown in Figure 5-1 [135]. The motion control processor determines the torque command for the motor based on present position and speed, and then the 3-phase inverter in servo amplifier unit (SAU) converts the dc power to the amount of ac power which is associated to the torque command to drive the motor. Consequently, the load is moving as expected under the drive of the motor. Figure 5-2 is the typical motor speed/torque command for one
Figure 5-1. Motion control block diagram for navel turret motor drive.
6-second drive cycle. The torque command is a short-period pulse signal, which requires the inverter to withstand an instantaneous power peak and produce as little power loss as possible, and/or have good heat removal capability. For different drive targets, there are various scalable current ratings, such as tiny (25 A), small (60 A), and large (120 A) one. Based on the tests conducted by the Navy, for the small current rating, the Si IGBT temperature was up to 60.8 °C, and temperature variation was within 21.7 °C. This is still fine for this application. While, for the large current rating, the maximum Si IGBT temperature reached 83.7 °C, and temperature variation is within 37.5 °C. This can not meet the requirements of the application. Therefore, the SiC-based inverter in this application is targeted for the motion control applications at small and large current

Figure 5-2. Motor speed/torque command.
ratings to provide the benefits of high power density, high temperature, high frequency, less cooling requirements, and compactness.

5.1.1 System modeling and simulation

The simulation diagram for this application is shown in Figure 5-3. It is mainly composed by three blocks, system parameters computation block, power losses model block, and system thermal model block. The first one is based on inductor motor equations, which calculated the system parameters (input power, phase current, modulation index, phase angle) needed by power losses models. The other two are based on the system models presented in chapter 3. Then, two things needed to be done, one is the derivation of equations for system parameter calculation, and the other is to decide what kind of devices will be used and their property parameters.

1. System parameters calculation

Assume the motor works with a dc power supply $V_{dc}$ and controlled by a SPWM inverter with a modulation index of $M$. Its number of poles is $p$, efficiency is $\eta$, and base
frequency is $f_b$. The motor is required to produce torque $T_e$ at an electrical speed of $\omega_r$.

Then the input power of the motor is

$$P_{in} = \frac{P_o}{\eta} = \frac{T_e \omega_r}{\eta}. \quad (5-1)$$

Output frequency:

$$f_o = \frac{P}{2} \cdot \frac{\omega_r}{2\pi} \quad (5-2)$$

Modulation index:

$$M = \frac{f_o}{f_b} \quad (5-3)$$

For SPWM control:

$$\sqrt{\frac{3}{2}} V_L = M \frac{V_{dc}}{2} \Rightarrow V_L = \sqrt{\frac{3}{2}} \frac{V_{dc}}{2} M \quad (0 \leq M \leq \frac{4}{\pi}) \quad (5-4)$$

In the above equation $V_L$ is the line-line voltage. If the excitation current is $I_m$, the phase current can be computed by

$$I_L = \sqrt{\left(\frac{P_{in}}{\sqrt{3} V_L}\right)^2 + I_m^2}. \quad (5-5)$$

Correspondingly, the phase angle between the voltage and current is

$$\phi = \cos^{-1}\left(\frac{P_{in}}{\sqrt{3} V_L I_L}\right). \quad (5-7)$$

In this application, the command speed and torque are shown in Figure 5-4. Other parameters used in the simulation are listed in Table 5-1. The calculated motor phase current and input power under the command is shown in Figure 5-5. The maximum current (60.4 A) and maximum input power (26.7 hp) are very close to the test results (61.2 A and 25.2 hp).
Table 5-1. Motor parameters used in the simulations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency, %</td>
<td>85</td>
<td>Base speed, r/min</td>
<td>912</td>
</tr>
<tr>
<td>Num. of poles</td>
<td>4</td>
<td>Exciting current, A</td>
<td>4.8</td>
</tr>
<tr>
<td>DC voltage, V</td>
<td>300</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(a) Motor speed       
(b) Motor torque

Figure 5-4. Motor command.

(a) Absolute value of phase current (A)  
(b) motor input power (W)

Figure 5-5. Motor current and power from the simulation vs. time (s).
Table 5-2. Devices used in the inverter

<table>
<thead>
<tr>
<th>Device Characteristics</th>
<th>SiC JFET</th>
<th>SiC diode</th>
<th>Si IGBT/diode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rating voltage (V)</td>
<td>1500</td>
<td>1200</td>
<td>1200</td>
</tr>
<tr>
<td>Rating current (A)</td>
<td>3</td>
<td>10</td>
<td>400</td>
</tr>
<tr>
<td>Number of paralleled components</td>
<td>134</td>
<td>40</td>
<td>1</td>
</tr>
<tr>
<td>Manufacture</td>
<td>SiCED</td>
<td>Cree</td>
<td>Powerex</td>
</tr>
</tbody>
</table>

2. Inverter design

As shown in Figure 5-5 (b), the maximum power of this system is about 20 kW. Currently, a Si inverter composed of Powerex IGBT/diode combo (1200V/400A) is used in this system. Thus, a SiC inverter with similar rating is designed and compared with the Si inverter. The devices used in this study are listed in Table 5-2.

Matlab simulink programs are set up for the SiC-based system and Si-based system, respectively. Figure 5-6 is the program for the SiC-based system, and marked corresponding to Figure 5-3. The simulation was run for the Si-based system at test conditions, and a comparison between the simulation results and test results is made. The instantaneous temperature response is shown in Figure 5-7. The average values are listed in Table 5-3. It is found that they are very close. Therefore, the simulation models work well in this application.

Table 5-3. Comparison of test and simulation results of the Si inverter

<table>
<thead>
<tr>
<th>Inverter performance</th>
<th>Test</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGBT average junction temperature (C)</td>
<td>41.7</td>
<td>42.2</td>
</tr>
<tr>
<td>Diode average junction temperature (C)</td>
<td>41.7</td>
<td>41.9</td>
</tr>
<tr>
<td>Average power loss (W)</td>
<td>125.8</td>
<td>123.5</td>
</tr>
</tbody>
</table>
Figure 5-6. Matlab Simulink program for naval servo drive.
Figure 5-7. Temperature response of the Si inverter.
5.1.2 Simulation results and discussion

Assume the ambient temperature is 37°C, and the inverters switch at 20 kHz, the thermal grease parameters are $R_{cb} = 0.0026$ K/W, $\tau_{cb} = 0.01$ s.

1. At the same cooling condition: $R_{ca} = 0.156$ K/W and $\tau_{ca} = 102$ s.

Figure 5-8 shows the simulated device temperature profiles for the SiC inverter and the Si inverter. It is obvious that the SiC inverter performs better than a Si inverter. The peak and average junction temperature of the SiC devices is reduced by a factor of about 10 and 8, respectively, which enable the system to perform more reliably.

2. Continuous operation

If this system operates continuously for more than one drive cycle, the device temperatures will continue to increase (Figure 5-9). The rate of temperature rise is approximately 5.5 °C/min of the Si devices, which makes the junction temperatures reach their limits quickly. The typical maximum operation temperature of Si devices is 150 °C.
Thus, the system with the Si inverter can work continuously for about 20 minutes without violating the temperature constraint. While for the SiC devices, the rate of temperature rise is approximately $0.85 \, ^{\circ}\text{C/min}$. Since no reliable high-temperature package is available for SiC devices at present, the temperature of SiC devices is also limited to 150 $^{\circ}\text{C}$. With this constraint, the system with the SiC inverter can work continuously for about 2.2 hours. But, theoretically, SiC devices can work up to at least 300 $^{\circ}\text{C}$. For this case, the SiC system would work safely for 5.2 hours. Therefore, the application of the SiC inverter in such a system can improve the system reliability without adding more strain to its cooling management.

3. Efficiency (at the same cooling condition: $R_{ha} = 0.156 \, \text{K/W, } \tau_{ch} = 102 \, \text{s}$)

The SiC inverter is more efficient than the Si inverter. On one hand, it has lower power loss, which is about 1/6th of that of the Si inverter, and in turn has a 7% advantage in efficiency (refer to Table 5-4).
Table 5-4. Average power loss and efficiency of SiC/Si inverter

<table>
<thead>
<tr>
<th>Material</th>
<th>Average power input (W)</th>
<th>Average power loss (W)</th>
<th>Inverter efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC</td>
<td>1131.2</td>
<td>15.6</td>
<td>98.6</td>
</tr>
<tr>
<td>Si</td>
<td>1131.2</td>
<td>96.9</td>
<td>91.4</td>
</tr>
</tbody>
</table>

4. Heatsink

In the above study, the size of heatsink is optimized for the Si inverter. It is oversize for the SiC inverter (see Figure 5-8 and Figure 5-9). It is reasonable to reduce the heatsink size of the SiC inverter. Table 5-5 compares the performance of the inverters with heatsink and without a heatsink. It is obvious that the heatsink dose not improve the performance of the SiC inverter much, and the efficiency remains the same. Compared to the Si inverter with the heatsink, the efficiency of the SiC inverter is still 6% higher. Therefore, in this application, using the SiC inverter can eliminate heatsink. As a result, the thermal management is simplified, and the system compactness is improved.

Table 5-5. Junction temperature and power loss

<table>
<thead>
<tr>
<th>Material</th>
<th>$R$ (K/W), $\tau$(s)</th>
<th>Maximum temperature for 1st cycle (°C)</th>
<th>Avg. temperature rise per cycle (°C)</th>
<th>Inverter power loss (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Switches Diodes</td>
<td>Switches Diodes</td>
<td>Max.</td>
</tr>
<tr>
<td>SiC</td>
<td>$R_{ha} = 0.156, \tau_{ha} = 102$</td>
<td>37.2 37.2</td>
<td>0.13</td>
<td>0.14</td>
</tr>
<tr>
<td>Si</td>
<td>$R_{ha} = 60, \tau_{ha} = 0.01$</td>
<td>47.0 41.7</td>
<td>2.2</td>
<td>1.5</td>
</tr>
<tr>
<td>SiC</td>
<td>$R_{ha} = 0.35, \tau_{ha} = 2.83$</td>
<td>39.5 46.5</td>
<td>0.35</td>
<td>2.83</td>
</tr>
<tr>
<td>Si</td>
<td>$R_{ha} = 0.01$</td>
<td>Violate temperature limit</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5.2 Wind generation application

The underlying premise of the application is that SiC devices would reduce substantially the cost of energy of large wind turbines that need power electronics for variable speed generation. Variable speed capability allows the wind turbine to operate at the speeds which produce the greatest amount of power and minimizes torque perturbations in the drive train. This capability tends to decrease the overall cost of energy because the amount of energy generated is increased, and the cost of the drive train and its maintenance are reduced. Since the voltage and frequency of the generated power vary with turbine speed, a converter is required to reconcile the output with the fixed voltage and frequency of the grid. SiC-based power devices have several advantages, including lower losses, higher temperature, and faster switching. These can be exploited to reduce losses and increase net energy production. The lower losses, along with higher temperature, can be exploited to improve the reliability of the converter, thus potentially reduce the cost of the converter.

One of the key purposes of this work is to simulate the performance of SiC-based converters that might be used in a wind turbine, and compare to the commonly used Si converters.

5.2.1 System modeling and simulation

A wind generation system is composed of wind turbine, PM generator, back-to-back converter, and utility filter, as shown as Figure 5-10. The wind energy is converted to
electricity by the PM generator, and then transferred to the utility. In this process, the back-to-back converter plays two roles, one is to control the generator to catch as much wind energy as possible (high switching speed is desirable), and the other is to deliver the energy to the utility. In both roles, the power loss in the converter is of the most concern.

Using the system modeling method, a profile of the converter power loss can be obtained. As what has been done for the motion control application, the system parameters must be obtained first.

1. System parameters calculation

In this study, the input power $P_{in}$ (kW) and the speed of the generator $n_g$ (rpm) at a certain wind speed is known. Some electrical parameters of the generator, such as rated speed $n_0$ (rpm), back Emf at rated speed (line-neutral, peak) $Emf_0$ (V), pole number $p$, stator phase resistance $R$ (Ω), stator phase inductance $L$ (H), eddy loss at rated speed $P_{le0}$ (kW), and hysteresis loss at rated speed $P_{lh0}$ (kW), are also known. Assume the generator back Emf is in phase with the generator current, then parameters for the generator

![Figure 5-10. Wind generation system.](image)
rectifier can be calculated based on PM generator theory as follows:

Generator frequency, $f_g$

$$f_g = \frac{p \cdot n}{120} \quad f_{g0} = \frac{p \cdot n_0}{120} \quad (5-8)$$

Back Emf (line-neutral, peak), $Emf$

$$Emf = Emf_0 \cdot \frac{f_g}{f_{g0}} \quad (5-9)$$

Core losses, $P_{lc}$; eddy loss, $P_{le}$; and hysteresis loss, $P_{lh}$

$$P_{lc} = P_{le} + P_{lh} \quad P_{le} = P_{le0} \cdot \frac{f_g}{f_{g0}} \quad P_{lh} = P_{lh0} \cdot \frac{f_g}{f_{g0}} \quad (5-10)$$

Phase current on $q$-axis (peak), $I_{sq}$

$$I_{sq} = \frac{1000 \cdot P_{in} \cdot 2}{3 \cdot Emf} \quad (5-11)$$

Output voltage without considering the core losses, $E_c$

$$E_c = \sqrt{(Emf - I_{sq} R)^2 + (I_{sq} X)^2} \quad X = \omega_g L \quad \omega_g = 2\pi f_g \quad (5-12)$$

Effective current due to core losses (peak), $I_c$, $I_{eq}$ ($q$-axis component), $I_{ed}$ ($d$-axis component)

$$I_c = \frac{1000 \cdot P_{lc} \cdot 2}{3 \cdot E_c} \quad I_{eq} = I_c \cdot \cos \phi_c \quad I_{ed} = I_c \cdot \sin \phi_c \quad \phi_c = \arccos \left( \frac{E_c}{Emf} \right) \quad (5-12)$$

Total phase current (peak), $I_s$

$$I_s = \sqrt{I_{sq}^2 + I_{std}^2} \quad I_{sq} = I_{sq} + I_c \cos \phi_c \quad I_{std} = I_{ed} + I_c \sin \phi_c \quad (5-13)$$

Output voltage (peak), $U_{gout}$
\[
U_{gou} = \sqrt{U_{sq}^2 + U_{sd}^2} \quad U_{sq} = E_{mf} - I_{std}X - I_{stq}R \quad U_{sd} = I_{stq}X - I_{std}R \quad (5-14)
\]

Power factor, \(\cos \phi\)

\[
\cos \phi = \cos(\alpha_I - \alpha_U) \quad \alpha_I = \arccos \left( \frac{I_{stq}}{I_{std}} \right) \quad \alpha_U = \arccos \left( \frac{U_{sq}}{U_{sd}} \right) \quad (5-15)
\]

Copper loss, \(P_{lcu}\)

\[
P_{lcu} = \frac{3 \cdot I_i^2 \cdot R}{2 \cdot 1000} \quad (5-16)
\]

Generator Efficiency, \(\eta_g\)

\[
\eta_g = \frac{P_{in} - P_{lcu} - P_l}{P_{in}} \times 100\% \quad (5-17)
\]

Modulation Index, \(M_i\)

\[
M_i = \frac{U_{gou}}{V_{dc}/2} \quad (5-18)
\]

For the grid inverter, if the power loss of the DC link capacitor is neglected, the input power of the grid inverter is equal to the output power of the generator rectifier. Then, for a certain grid output voltage \(V_{ll}\) (line-line, rms) and power factor \(\cos \phi\), the phase current (peak) \(I_o\), is

\[
I_o = \frac{\sqrt{2}P_{in}\eta}{\sqrt{3}V_{ll}\cos \phi} \quad (5-19)
\]

and its modulation index \(M_i\) is

\[
M_i = \frac{2\sqrt{2}V_{ll}}{\sqrt{3} \cdot V_{dc}} \quad (5-20)
\]

Also, the filter loss \(P_f\) is considered when calculating the system efficiency.
\[ P_{lf} = k \cdot I_{grid}^2 \]  \hspace{1cm} (5-21)

The values of parameters of the studied system are listed in Table 5-6.

2. Converter design

For this application, a 1.5MW converter is required. Because of no available SiC devices at this rating, the converter is assumed to be composed of 10 SiC-based converters rated at 150 kW in the simulation, which are based on the devices listed in Table 5-7.

<table>
<thead>
<tr>
<th>Table 5-6. Wind generation system parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Generator parameters</td>
</tr>
<tr>
<td>Rated power, MW</td>
</tr>
<tr>
<td>Nominal voltage, V</td>
</tr>
<tr>
<td>Rated speed ( n_0 ), rpm</td>
</tr>
<tr>
<td>Back Emf at ( n_0 ), ( Emf_0 ), V</td>
</tr>
<tr>
<td>Base machine pole number ( p )</td>
</tr>
<tr>
<td>Stator phase resistance ( R ), ( \Omega )</td>
</tr>
<tr>
<td>Stator phase inductance ( L ), ( H )</td>
</tr>
<tr>
<td>Eddy loss at ( n_0 ), ( P_{le0} ), kW</td>
</tr>
<tr>
<td>Hysteresis loss at ( n_0 ), ( P_{h0} ), kW</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 5-7. Devices used in the converters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Item</td>
</tr>
<tr>
<td>SiC MOSFETs</td>
</tr>
<tr>
<td>SiC Schottky diodes</td>
</tr>
<tr>
<td>Si MOSFETs</td>
</tr>
<tr>
<td>Si ultrafast recovery diode</td>
</tr>
</tbody>
</table>

* The number of devices that are paralleled per converter leg.
In addition, for the generator rectifier, as mentioned previously, it works in a complementary way to a converter, that is, the diodes in the rectifier are equivalent to the switches in a converter. Thus, the duty ratio of the switches in a rectifier is \(1-D\) instead of \(D\). Correspondingly, the inverter power loss models during conduction period (Equation (3-43) and (3-50) in chapter 3) need to be modified for a rectifier, (see equation (5-22) and (5-23)).

\[
P_{D,\text{cond}} = I^2 R_J \left( \frac{1}{8} \frac{1}{3\pi} M \cos \phi \right) \tag{5-22}
\]

\[
P_{D,\text{cond}} = I^2 \cdot R_D \left( \frac{1}{8} + \frac{1}{3\pi} M \cos \phi \right) + I \cdot V_D \cdot \left( \frac{1}{2\pi} + \frac{M \cos \phi}{8} \right) \tag{5-23}
\]

### 5.2.2 Simulation results and discussion

The simulation of this wind generation system is done for the wind speed range from 6 m/s to 11 m/s, which has the best energy density. Different switching frequencies are also studied. In order to compare the SiC converter to the Si one, the temperature limit for both systems is assumed to be 150 °C.

1. At switching frequency 3 kHz

Since most wind turbines are installed in areas where the wind speed varies from 6 m/s to 11 m/s, the generator is designed to work at rated power at the wind speed of 11 m/s, and at the above speeds, it keeps the rated speed and power. By the simulation, from 6 m/s to 11 m/s, the converter efficiency (including the power loss of the filter) is shown as Figure 5-11. At the whole speed range, the efficiency of the Si converter is lower than
that of the SiC converter. The average power loss saved by the SiC converter is about 55.1% of that of the Si converter. At the worst case (wind speed 11 m/s), it is about 59.8 kW. As the wind speed increases, the efficiency of both converters decreases, and that of the Si converter decreases more quickly. The power loss percentage of each component in the wind generation system at rated speed is shown in Figure 5-12. For the Si-based system, the converter loss accounts for the most loss, which is as large as 45.1%. Thus, it is necessary to reduce the loss in the converter in order to improve the generation system efficiency. The SiC converter is a good alternative.

2. At different frequency up to 20 kHz

On the other hand, Figure 5-12 demonstrates that the power loss of the filter even accounts for more loss than the SiC converter (26.9% vs. 17.1%) in the SiC-based system.
The size and loss of the filter is related to the switching frequency of the converter. Improving the switching frequency of the converter can reduce the size and loss of the filter, and thus the cost. Since high switching frequency is one of the merits of SiC devices, improving the switching frequency of the converter in this application might be considered. As shown in Figure 5-13, when frequency increases from 3 kHz to 18 kHz (this value is close to the limit of Si devices), the efficiency of the SiC converter is lowered by 1 %, while it is 2 % lower for the Si converter. This means that the size of the filter can be reduced at a cost of increased converter switching loss. So a balance point needs to be found between these two factors. For example, improve the switching frequency of the SiC converter to 18 kHz, its efficiency is 98.3 %, which obtains 0.4 % advantage in efficiency compared to the Si converter switching at 3 kHz, and at the same

Figure 5-12. Power loss breakdown in the wind generation system at rated speed.

![Power loss percentage of each components in the wind generation system](chart.png)
time, the size, loss, and cost of the filter are reduced, too.

3. High temperature capability of the SiC converter

The cooling requirement of the SiC converter can be less than that of the Si converter even with the same temperature limit. As calculated by the simulation, the size of the SiC converter heatsink is about 1/3 of that of the Si converter under the same ambient temperature and cooling conditions (maximal temperature 150 °C, forced convection 6.1 m/s). The efficiency is 98.5 % (the SiC converter) vs. 96.5% (the Si converter).

The temperature limit used here (150 °C) is the extreme of Si devices. But SiC devices are allowed to work at higher temperature, say 300 °C. The efficiency of the SiC converter at 300 °C is lowered by only 0.1 %, while the size of the heatsink is theoretically reduced to 1/14 of that of the Si converter with the temperature limit of 150

Figure 5-13. Efficiency of SiC and Si wind turbine converters at different switching frequency.
Therefore, the high temperature capability of SiC devices will further reduce the system size and cost.

As a summary, the simulation shown here indicated that the application of the SiC converter in the wind generation system will improve the system efficiency, conserve energy resources, and reduce system size and cost as expected due to the low-loss, high-frequency, and high-temperature properties of SiC devices.

5.3 Battery-utility interface application

Power conversion systems account for major cost and reliability issues in most distributed generation and energy storage systems. The system studied here is an example of such systems. Besides the battery, the voltage source can be microturbine, photovoltaic cell, or wind turbine; and the load can be any kind of three-phase electrical load, or electrical grid. Therefore, it can be used in motor drive, transportation, and distributed energy resources applications. Moving from Si to SiC based devices has the potential to benefit these systems with high power rating, switching frequency, efficiency, and compactness, as well as reliability.

5.3.1 System modeling and simulation

In the battery-utility interface system shown in Figure 5-14, the converter is connected to the battery bank and the utility at two ends, respectively [136]. The battery bank is to be charged and discharged from the utility via the three-phase, full-bridge
converter. The converter works as a rectifier during the charging of the batteries, and an inverter for discharging.

1. DC link voltage

The converter is controlled by Sinusoidal Pulse Width Modulation strategy (SPWM). The relationship between line voltage, $V_{ll}$, and dc link voltage, $V_{dc}$, can be expressed as (5-24), where $M$ is modulation index. If $0 \leq M \leq 1$, the minimum dc link voltage is for $M = 1$. For $V_{ll} = 480$ V, $V_{dc (min)} = 783.8$ V.

$$V_{ll} = M \cdot \frac{\sqrt{3}V_{dc}}{2\sqrt{2}} \quad (5-24)$$

2. Battery bank

The battery bank must be designed to meet the minimum requirement of the dc link voltage. A Hawker Genesis brand, 13Ah rated lead acid battery (with a nominal voltage of 12V) is considered here. Its typical property curves are shown in Figure 5-15 [137]. During discharging, the output voltage of the battery slowly decreases due to the
decrease of open-circuit voltage of the battery. Thus, at the end of discharge, the open-circuit voltage of the battery is the minimum, and this determines the number of batteries needed in series. As shown in Figure 5-15 (c), after the battery is discharged to about 40% state of charge (SOC), there will be a sharp increase in battery discharge resistance. Consequently, running the battery with a SOC lower than 40% would require a large number of batteries in series. Specifically, the number of batteries in series can be 43% more when the batteries are discharged to 20% SOC instead of 40% SOC. Therefore, the optimum number of batteries in series is 84 corresponding to the end of discharge at
40% SOC in this case. If the battery bank is discharged by a constant current of 120 A, it can last 2.33 hours from full charge to 40% SOC.

As [137], the performance of the batteries shown in Figure 5-16 can be modeled by a basic equivalent circuit shown in Figure 5-16. The $R_{\text{dis}}$ and $R_{\text{chr}}$ are discharge resistance and charge resistance, respectively. They vary as the curves shown in Figure 5-15 (c) and (d).

3. Converter

The converter has a standard 3-phase full-bridge topology with six switches and six anti-parallel diodes. To meet the requirements of this system, the ratings of these devices must be larger than the maximum of the current and the voltage that they are supposed to handle. The maximum voltage occurs when the batteries are fully charged, and this value is larger than the nominal voltage of batteries. The maximum current occurs at the beginning of the discharge of batteries. Based on the above discussion and also considering the availability of devices, the selected devices are shown in Table 5-8. Their property parameters obtained from tests used in the simulations are listed in Table 5-9.

In addition, for discharge cycle, the converter works as a inverter, its power loss
models are the same as those presented in chapter 3; for charge cycle, it works as a rectifier, like the generator rectifier in the wind turbine converter, the modulation index in its models is modified (refer to Equations 5-22 and 5-23).

### 5.3.2 Simulation results and discussion

In this work, assume that the utility has a line voltage of 480 Vrms, a frequency of 60 Hz, and the converter was controlled to produce current at unity power factor. The battery bank is composed of 84 13Ah Hawker Genesis batteries in series. The battery bank is discharged at a constant current of 120 A from full charge to 40% SOC, and the power is delivered to the utility through the converter. Vice versa, it is charged at a constant voltage of 1109 V from 40% SOC to full charge, and the power is provided by the utility through the converter. Then, the load currents for discharge and charge cycles

<table>
<thead>
<tr>
<th>Item</th>
<th>Voltage rating</th>
<th>Current rating</th>
<th>Part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC JFETs</td>
<td>1200</td>
<td>14A ×21</td>
<td>SiCED</td>
</tr>
<tr>
<td>SiC Schottky diodes</td>
<td>1200</td>
<td>10A×30</td>
<td>Cree, CSD10120</td>
</tr>
<tr>
<td>Si IGBT Module</td>
<td>1200</td>
<td>300A</td>
<td>Powerex, CM300DY-24NF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Si</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGBT/JFET on-state resistance</td>
<td>6.6 mΩ</td>
<td>7.4 mΩ (0.156Ω/21)</td>
</tr>
<tr>
<td>IGBT/JFET voltage drop when I=0</td>
<td>0.83 V</td>
<td>0.0</td>
</tr>
<tr>
<td>IGBT/JFET transconductance</td>
<td>61.2 S</td>
<td>14.7 S (0.7 S×21)</td>
</tr>
<tr>
<td>Diode on-state resistance</td>
<td>8.6 mΩ</td>
<td>2.1 mΩ (63.8mΩ/30)</td>
</tr>
<tr>
<td>Diode reverse recovery charge</td>
<td>13μC</td>
<td>0.84μC (28nC×30)</td>
</tr>
</tbody>
</table>
solved by the battery system model are shown in Figure 5-17. In Figure 5-17 (a), the peak current flowing through the converters changes slowly during the discharge cycle. The current decreases quickly as the open-circuit voltage of the battery bank increased during the charge cycle, and the average of the charge current is much lower than that of the discharge current (Figure 5-17 (b)). Thus, the charge cycle is much longer than the discharge cycle, and the instantaneous power involved in the charge cycle is much lower than that in the discharge cycle.

Two sets of simulations are designed for this study. In the first set of simulations, the ambient temperatures and the heatsink sizes were the same for the Si and SiC systems. In the second set of simulations, the heatsinks were selected to limit the maximum junction temperature to 125°C for both the SiC and Si devices. The results of the two converters will be discussed respectively, according to charge cycle or discharge cycle.
1. With the same heatsink size and ambient temperature

With variation of the system variables, power losses and device junction temperatures change dynamically. The change processes obtained from simulations are shown in Figures. (5-18)-(5-21) (for discharge) and Figures. (5-22)-(5-25) (for charge).

During discharge, the great power savings of the SiC Schottky diode due to lower on-state resistance (Figure 5-19 (b)) and better reverse recovery characteristics reduced the temperature rise of the SiC system dramatically (Figure 5-18). Temperature has a significant effect on device characteristics, especially on the mobility of electrons and holes that dominates the dependency on temperature of the on-state resistance of devices. Although the on-state resistance of the SiC JFET is larger than that of the Si IGBT at room temperature (see Table 5-9), a lower on-state resistance was found in the SiC JFET as shown in Figure 5-19 (a) because of its much lower junction temperature (see Figure 5-18 (a)). This further reduced system power losses and improved efficiency of the SiC converter (see Figure 5-20 and Figure 5-21). Consequently, the junction temperature rise of the SiC devices is less than that of the Si devices. Continuously, the junction temperatures affect the device characteristics, and repeat the above dynamic process until a steady state is reached.

During charge, a similar process exists. Again, the performance of the SiC Schottky diode is much better than that of the Si diode in both conduction and switching states (Figures. (5-22)-(5-24) (b)). For the SiC JFET, its on-state resistance is larger than that of
Figure 5-18. Device junction temperatures during discharge.

Figure 5-19. Device on-state resistances during discharge.
Figure 5-20. Device power losses during discharge (single device).

Figure 5-21. System power losses and efficiency during discharge.
Figure 5-22. Device junction temperatures during charge.

(a) SiC JFETs/Si IGBTs  
(b) Diodes

Figure 5-23. Device on-state resistances during charge.

(a) SiC JFETs/Si IGBTs  
(b) Diodes
Figure 5-24. Device power losses during charge (single device).

Figure 5-25. System power losses and efficiency during charge.
the Si IGBT as shown in Figure 5-23 (a). It seems that the conduction loss of the SiC JFET should be larger. However, this is not the only contribution to the conduction loss of a switch. The loss due to the voltage drop across Schottky barrier or $pn$-junction is also an important part, and it dominates when current is small. As shown by device characteristics provided in Table 5-9, the voltage drop across the Si IGBT at zero current is much higher than that of the SiC JFET. So the conduction loss of the Si IGBT due to this voltage drop is relatively large. Since the current during charge is small, this part of conduction loss dominates the overall conduction loss. That is to say, the overall conduction loss of the SiC JFET is smaller than that of the Si IGBT. As for switching losses, the SiC JFET can also compete with the Si IGBT because of no tail current during turn off. Thus, the total of power losses of the SiC JFET is smaller than that of the Si IGBT as shown in Figure 5-24 (a). Combining the better performances of the SiC JFET and the SiC Schottky diode, the SiC converter is better than the Si one under charge mode (see Figure 5-25).

No matter discharge mode or charge mode, the SiC converter shows better performance than the Si one in efficiency and juncture temperature. More clearly, the specific improvements are summarized in Table 5-10.

2. With different sizes of heatsinks

In high power applications, the size of a heatsink could account for 1/3 of total system volume. How to reduce the size of heatsink is always an issue. To show the
benefit of a SiC converter in this aspect, the simulation is designed to run the SiC and Si devices to the same temperature (125°C) by using different sizes of heatsinks. The results indicate that the size of the heatsink required by the SiC converter is reduced to about 1/25 of that of the Si converter under the same cooling method (forced cooling with fan) or 4/5 when the SiC inverter is naturally cooled, and at the same time the efficiency is improved by 3.1% for discharge, 5.4% for charge.

In addition, when the average junction temperatures of SiC devices change from 45°C/50°C (for the SiC JFET/the SiC Schottky diode, respectively) under Condition A (in Table 5-10) to 97°C/116°C under Condition B, the efficiency of the SiC converter during discharge is lowered by only 0.2%. This indicates that the influence of temperature on the SiC devices is very small. Thus, more benefits can be achieved if SiC devices are used in high-temperature applications.

In both charge and discharge modes, the SiC converter has a better performance over

<table>
<thead>
<tr>
<th>Condition</th>
<th>Operation Mode</th>
<th>Average Junction temperature reduction (°C)</th>
<th>Average efficiency improvement (%)</th>
<th>Average power loss reduction (kW)</th>
<th>Energy savings in one cycle (kWh)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Condition A: With the same heatsink size and ambient temperature</td>
<td>Discharge</td>
<td>56/63</td>
<td>3.3</td>
<td>3.09</td>
<td>7.20</td>
</tr>
<tr>
<td></td>
<td>Charge</td>
<td>7/11</td>
<td>5.5</td>
<td>0.45</td>
<td>8.37</td>
</tr>
<tr>
<td>Condition B: With the same maximum junction temperature (125°C)</td>
<td>Discharge</td>
<td>4/3</td>
<td>3.1</td>
<td>2.93</td>
<td>6.83</td>
</tr>
<tr>
<td></td>
<td>Charge</td>
<td>1/5</td>
<td>5.4</td>
<td>0.45</td>
<td>8.30</td>
</tr>
</tbody>
</table>

Note: The two numbers in column “Junction temperature reduced” are for JFET(IGBT) and diode, respectively.
the Si one. With the same external thermal condition (the same heatsink size and ambient temperature), great advantages in efficiency and junction temperatures were found for the SiC-based converter. On the other hand, with the same thermal limit, large savings in system weight and volume combined with a high efficiency were found in the SiC-based converter. Therefore, this SiC-based battery converter system is expected to substitute for its Si counterpart in systems like automobiles where weight and volume are the critical factors, the SiC converter can be designed to work at high temperature with a simple and compact cooling system. For solar systems where efficiency and reliability is more important, the SiC converter can work at low temperature with the same size heatsink to the Si converter in order to achieve high efficiency and reliability. Even though SiC devices are expensive, the aforementioned benefits can make them very cost-effective.

5.4 Hybrid electric vehicle application

As the issues of energy and environment are more and more important, hybrid electrical vehicles (HEV) has become a hot research topic. The application of SiC devices (as battery interface, motor controller, etc.) in a HEV is supposed to gain the benefits from their merits of high-temperature capability, high-power density, and high efficiency. Moreover, the light weight and small volume will affect the whole power train system in HEV, and thus the performance and cost. In this section, the impact of SiC devices on HEVs will be studied by using the system modeling method presented in this work combined with PSAT (Power Train Analysis Tool, vehicle simulation software).
5.4.1 System modeling and simulation

PSAT provides a programming environment based on MATLAB. All library components are open to users. That means that the library models can be modified, or new library models can be created by users. Thus, it provides good flexibility to meet the needs of different users. For this study, a model of the motor inverter is required. However, the PSAT model deals with the motor and its inverter as one unit, called “motor controller, which is based on experimental data. So it is not possible to study the impact of different inverters. New models were created to detach the inverter from the motor and the inverter. Figure 5-26 shows the change in the new model compared to the original one. In detail, the inverter model is developed using the method presented in Chapter 3 (Figure 5-27), and motor model is based on curve fitting of experimental data (Figure 5-28). The two models form a motor controller model (Fig. 5-29), which has the same inputs and outputs with the original one in order to achieve the compatibility with other models in PSAT.

Two simulation models are set up in PSAT based on the design of 2004 Toyota Prius HEV (as shown as Figure 5-30) using the new motor controller presented above. One is with SiC-based motor inverter and the other is with Si one. These inverters are composed of the devices listed in Table 5-8 and have the same design with those in Table 5-9. Then, a simulink program shown in Figure 5-31 is generated automatically by PSAT. After running the simulation, the results can be loaded into PSAT for further analysis.
Figure 5-26. Comparison of PSAT model and the new model.

Figure 5-27. Inverter model in Simulink.
Figure 5-28. Motor model in Simulink.
This is a temporary fix. At high speed the available torque goes to zero which is a problem for the control of the engine/motor 2 in the split configuration. There is overshoot in the motor 2 speed controller that causes the motor to end up at high speed in the zero torque region of its torque curve. We are currently revising the motor 2 controller, this is just a stop gap measure. This problem appears most often on US 06 cycles, i.e. high speed large acceleration cycles.

Figure 5-29. New motor controller model in Simulink.
Figure 5-30. Powertrain architecture of 2004 Toyota Prius HEV.

(a) Complete model
5.4.2 Simulation results and discussion

1. 2004 Toyota Prius HEV

Simulations are run for a UDDS (US EPA-Urban Dynamometer Driving Schedule, which represents city driving conditions of light duty vehicles, see Figure 5-32) cycle for both a HEV with a SiC inverter and one with a Si inverter. Assume the two inverters have the same size heatsink and cooling conditions, and the switching frequency is 20 kHz. The initial SOC is equal to final SOC. As for inverter itself, the benefits of the SiC devices are shown in Figure 5-33. Due to the lower power losses of the SiC devices, the...
Junction temperatures of the SiC devices are much lower than those of Si ones (see Figure 5-33 (a) and (b)). As a result, the power loss of the SiC inverter is reduced, and its efficiency is much improved (see Figure 5-33 (c) and (d)). A quantified comparison for SiC and Si inverters are listed in Table 5-11. To be noted, the efficiency of inverter varies with load in the vehicle which is changing with the drive cycle. So an average value based on one drive cycle is given in Table 5-11 with counting the efficiency at zero speed as zero.

Furthermore, the benefits of the SiC-based inverter are also seen at system level. For example, the system efficiency is improved from 31.3 % to 37.2 % (increased by 22.6 %, corresponding to 0.82 kWh), and the fuel economy is improved from 56.7 to 69.5 mpg (increased by 18.8%). More details are summarized in Table 5-11. For the Si-based

<table>
<thead>
<tr>
<th>Description</th>
<th>Si</th>
<th>SiC</th>
<th>Improvement %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device level</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JFETs/IGBTs average junction temperature (°C)</td>
<td>59</td>
<td>30</td>
<td>49.2</td>
</tr>
<tr>
<td>Diodes average junction temperature (°C)</td>
<td>57</td>
<td>30</td>
<td>47.4</td>
</tr>
<tr>
<td>Average inverter power loss (W)</td>
<td>829</td>
<td>85</td>
<td>89.7</td>
</tr>
<tr>
<td>Average inverter efficiency (%)</td>
<td>61.1</td>
<td>76.7</td>
<td>25.5</td>
</tr>
<tr>
<td>System level</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fuel economy (mile/gallon)</td>
<td>56.7</td>
<td>69.5</td>
<td>18.8</td>
</tr>
<tr>
<td>CO₂ emissions (g/mile)</td>
<td>157.8</td>
<td>128.6</td>
<td>18.5</td>
</tr>
<tr>
<td>Energy loss in generator (Wh)</td>
<td>90.3</td>
<td>76.6</td>
<td>15.2</td>
</tr>
<tr>
<td>Energy loss in motor (include inverter)(Wh)</td>
<td>555.3</td>
<td>270.7</td>
<td>51.3</td>
</tr>
<tr>
<td>Energy loss in gearbox (Wh)</td>
<td>35.5</td>
<td>35.4</td>
<td>0.3</td>
</tr>
<tr>
<td>Energy loss in final drive (Wh)</td>
<td>57.1</td>
<td>57.0</td>
<td>0.2</td>
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<td>Energy loss in mechanical accessory (Wh)</td>
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<td>36.4</td>
<td>14.4</td>
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<tr>
<td>Energy loss in engine (Wh)</td>
<td>2916.1</td>
<td>2390.8</td>
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</tr>
<tr>
<td>Total fuel energy use (Wh)</td>
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<td>3625.4</td>
<td>18.5</td>
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<tr>
<td>Percentage braking energy recuperated (Wh)</td>
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<td>80.0</td>
<td>31.8</td>
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<tr>
<td>System efficiency (%)</td>
<td>31.3</td>
<td>37.2</td>
<td>22.6</td>
</tr>
<tr>
<td>Mass of fuel needed to travel 320 miles (kg)</td>
<td>16.0</td>
<td>13.1</td>
<td>21.3</td>
</tr>
</tbody>
</table>
Figure 5-32. UDDS cycle.

(a)
system, the result of fuel economy is very close to the manufacture’s data (60 mpg) even though different Si devices and cooling method were used in the simulations. For the SiC-based system, the results were based on the predicted characteristics of future devices. They were overestimated for today’s prototype SiC devices, but are expected to be achieved in 10 years as improvements are made.

In addition, as shown in Figure 5-33 (a) and (b), the junction temperatures of the SiC devices are low. Taking the high temperature capability of the SiC devices into account, the cooling system of the SiC inverter can be downgraded. By simulation, if the size of heatsink is reduced to half, the efficiency of the inverter will have no big change and so will the efficiency of the HEV.

Figure 5-33. Comparison of the SiC and Si inverters in the HEV.
2. Plug-in HEV

A plug-in HEV is designed with all-electric operation capability and functions as a pure electric vehicle during the all-electric range (AER) in urban driving. It has similar component and powertrain architecture with a HEV, but has the ability to recharge a larger energy storage system (such as a battery bank) from off-board electrical power. Thus, plug-in HEVs are more effective in decreasing oil consumption and reducing air pollution compared to HEVs.

The plug-in studied here is designed with 30 miles AER, which is about 4 UDDS cycles. It has the same powertrain architecture and components with 2004 Toyota Prius HEVs, except the capacity of battery system is larger. By the simulations, the optimized size of battery bank for a plug-in vehicle with the SiC inverter and that with the Si inverter are 5.1 KAh and 7.8 KAh, respectively, compared to 1.1 KAh of 2004 Toyota Prius HEVs (assume initial SOC 90% and final SOC 30%). Thus, for this design, using a SiC-based inverter can reduced the size of battery bank by 34.6%. Assume the same heatsink design for both inverters, run simulations for both systems for 4 UDDS cycles. The performance of the two inverters is presented in Figure 5-34. Again, due to the lower power losses of the SiC devices, the junction temperatures of the SiC devices are much lower than those of Si ones (see Figure 5-34 (a) and (b)). As a result, the power loss of the SiC inverter is reduced, and its efficiency is much improved (see Figure 5-34 (c) and (d)). A quantified comparison for the SiC and Si inverters is listed in Table 5-12.
(a) SiC JFETs/Si IGBTs Junction Temperature

(b) Diodes Junction Temperature
Figure 5-34. Comparison of the SiC and Si inverters in the plug-in HEV during AER.
Furthermore, the benefits of the SiC-based inverter are also seen at system level. For example, the system efficiency is improved from 62.6 % to 79.6 % (increased by 27.2 %, corresponding to 1.9 kWh), and the electricity consumption is reduced from 124.4 to 83.8 Wh/km (decreased by 32.6%). More details are summarized in Table 5-12.

Since the junction temperatures of the SiC devices are low, more study is done by reducing the size of the heatsink of the SiC inverter. The junction temperature response is shown in Figure 5-35. It is found that the efficiency of SiC inverter is lowered by only 0.5 % and at system level, the system efficiency is lowered by 0.3 %. So it is feasible to use a small heatsink for the SiC inverter. Other simulation results are summarized in Table 5-13.

As a summary, for the plug-in HEVs with optimized design, the application of the SiC inverters can have a small heatsink and battery bank, but high system efficiency.
Figure 5-35. Junction temperatures of the SiC devices with a smaller heatsink.
To compare with HEVs, the equivalent fuel economy of a PHEV is estimated as follows:

a) Convert electricity economy in AER to equivalent fuel economy (Fuel efficiency of the HEV is 33866 Wh/gallon)

\[
\frac{33866 \text{ Wh/gallon}}{83.8 \text{ Wh/km}} \div 1.609 \text{ km/mile} = 251.2 \text{ mile/gallon}
\]  

(5-25)

PHEV with the SiC inverter:

\[
\frac{33866 \text{ Wh/gallon}}{124.4 \text{ Wh/km}} \div 1.609 \text{ km/mile} = 169.2 \text{ mile/gallon}
\]  

(5-26)

b) By report [138], for a PHEV with 30 miles AER, the fraction of miles potentially displaced by electricity is about 43%. Then, the equivalent fuel economy of the PHEV is
PHEV with the SiC inverter:

\[ 251.2 \times 43\% + 69.5 \times 57\% = 147.6 \text{ mile/gallon} \]  \hspace{1cm} (5-25)

PHEV with the Si inverter:

\[ 169.2 \times 43\% + 56.7 \times 57\% = 105.1 \text{ mile/gallon} \]  \hspace{1cm} (5-26)

Therefore, the application of the SiC inverter in the PHEV improves the fuel economy by 28.8 \%, which is larger than that for a conventional HEV (18.8\%). It indicates that using a SiC inverter in a PHEV can gain more than in a HEV.

5.5 Summary

For all the applications studied in this chapter, it is concluded that moving from Si converters to SiC converters can benefit the system with higher efficiency, better reliability, space-saving, light weight, and low cost. Of course, this is not to say that the SiC devices can take the place of Si devices in all systems. But it is easy to see the common aspects in the four applications. They all require high power rating, high temperature, and high frequency. Thus, at least, SiC devices are suitable for high-power, high-temperature, and high-frequency applications.
CHAPTER 6

Contributions and future work

SiC power electronics devices will be the next generation power devices due to the superior properties of SiC material. Rapid progress has been seen on SiC semiconductor technology in recent years. SiC diodes have been introduced into market since 2001, and the device quality has been greatly improved since their introduction. SiC JFETs and MOSFETs are also available from several manufacturers. Although most of the SiC devices are used in areas of military and aerospace currently, it could be expected that the applications of SiC devices will expand in the near future. There will be a great need of the modeling and simulation of SiC-device-based circuits and systems in order to guide both customers and manufacturers. There is not sufficient work conducted in this area in the literature. The dissertation systematically presents the technology to model and simulate such a system, and gives quantitative analysis on some potential applications.

6.1 Main contributions

- A survey of Si and SiC semiconductor technology, including property, history, state-of-art, and challenge.
- Derivation of temperature-dependent analytical models of SiC Schottky diode.
• Derivation of temperature-dependent analytical models of SiC JFET.
• Derivation of temperature-dependent analytical models of some Si devices.
• Derivation and adaptation of power loss models of a converter.
• Derivation and adaptation of thermal models of a converter.
• Implementation of the forementioned models in MATLAB SimuLink.
• Development of motor, generator, battery, and PSAT model for different applications.
• Simulation of a motion control application and quantitative analysis of impact of SiC devices on this system.
• Simulation of a wind generation application and quantitative analysis of impact of SiC devices on this system.
• Simulation of a battery-utility interface application and quantitative analysis of impact of SiC devices on this system.
• Simulation of a hybrid electric vehicle application and quantitative analysis of impact of SiC devices on this system.
• Tests of some SiC devices, including SiC Schottky diode, JEFT, MOSFET, and some Si devices.
• Build and test a hybrid inverter (Si IGBT/SiC diode) and control system using DSP.
• Experimental verifications of the models at device and inverter level.
• Confirmation of the advantages of SiC devices over Si devices in high-power, high-temperature, and high-frequency systems

6.2 Recommended future work

Since SiC power electronic technology is still in its infancy, there is a great deal of work needed to be done in this field. Future work recommended in this field is as follows:

• The models presented in the dissertation are based on standard 3-phase converter topology. But the methodology can be applied for other power electronic circuits which are also widely used, for example buck, boost, and dc-dc converters. The models of these circuits need to be derived.

• The dissertation gives quantitative analysis of several applications, which is based on the current device quality. Because of the rapid development of the SiC power electronic technology and industry, more and more products and prototypes become available, and the quality of devices is improved from time to time. New devices need to be tested and update the quantitative results.

• In simulations of the work, the SiC devices are paralleled to meet the power rating requirements due to the small ratings of available devices. Each device is dealt as a discrete component with separate package and gate driver. In future work, a module could be considered.
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Vita

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