To the Graduate Council:

I am submitting herewith a thesis written by Mo Zhang entitled "A Low Power CMOS Microluminometer and Transmitter for Bioluminescent Bioreporter Integrated Circuit (BBIC)." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed Kamrul Islam
Major Professor

We have read this thesis and
recommend its acceptance

Benjamin J. Blalock

Donald W. Bouldin

Accepted for the Council:

Anne Mayhew

Vice Provost and
Dean of the Graduate Studies

(Original signatures are on file with official student records.)

A LOW POWER CMOS MICROLUMINOMETER AND TRANSMITTER FOR BIOLUMINESCENT BIOREPORTER INTEGRATED CIRCUIT (BBIC)

A Thesis Presented for the Master of Science Degree
The University of Tennessee, Knoxville

Mo Zhang

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technique, layout, and testing of the VLSI chip. Finally, I would like to thank my husband, other family members and friends for their support and advice.

Abstract

This thesis is a study of the design of a low power CMOS microluminometer and transmitter for bioluminescent bioreporter integrated circuit (BBIC).

A BBIC sensor chip with lower consumption was fabricated in the 0.35μm CMOS process. This design was an improvement over a previous BBIC [1]. The previous BBIC was designed using a different CMOS process (0.5μm) and a different CAD tool (Magic). This thesis work involves redesign of the chip in 0.35μm CMOS process using Cadence design tool with improvement for power dissipation. Larger resisters are used instead of several small resisters, which were placed between power supply and ground and consumed too much power in the previous chip [1]. Also, the bias currents for several amplifiers were reduced to decrease the power consumption even further. The chip was tested under normal light condition and it was verified that the device implemented the basic functions of a sensor. The power consumption has been reduced to 3.5% of the previous chip [1], which is not because of the feature size change. Some test results of the photodiode and signal processing circuit are given. The transmitter system was designed using CAD tools Cadence following previous work [2]. The power amplifier was added to the transmitter to give larger signal out of the circuit. The simulation was run in Cadence. Appendixes show all the net list files for the sensor chip and transmitter circuit.

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CHAPTER 1

Introduction

1.1 Biosensor

Biosensors are hybrid devices combining a biological sensing component with an analytical measuring element. The biological component typically reacts and/or interacts with an analyte of interest to produce a response that can be quantified by an electronic, optical or mechanical transducer. The most common configuration uses immobilized macromolecules such as enzymes or antibodies as the biological component; another, less common, approach uses living microorganisms or sections of organs or tissues as the biological element. Originally, these biosensors sometimes referred to as whole-cell biosensors [3], used electrochemical transducers to detect the activity of growing cells [4]. Whole-cell biosensors have functioned in controlled environments but were not widely applicable, largely because of interference caused by growth on nutrients other than the target analyte.

Alternatively, molecular-biological techniques have been used to produce cells or bioreporter strains that have much greater selectivity. Typically, DNA sequences that code for a specific promoter sequence are fused with gene(s) coding for reporter enzyme(s) and introduced into a host cell. When the analyte is present, the reporter genes are expressed to produce the enzyme(s) responsible for the production of the measured signal. Thus, gene regulation (and not consequences of microbial activity) provides the selectivity.

Bioreporter technology consists of microbes that have been genetically engineered to detect and quantify specific chemical agents in air, soil, or water by giving off a measurable bioluminescent signal that is proportional to the concentration of the agent. In the process of bacterial degradation of pollutants, the induction and expression level of specific catabolic genes are often controlled by the presence and relative amounts of the pollutant to be catabolized [5]. Thus, measurement of the amount of gene expression can be used to infer the relative quantities of bioavailable contaminant in the sensing environment. Direct measurement of catabolic gene expression is often difficult, as no obvious phenotypic change may occur in the organism. Gene expression, however, may be measured by modifying an organism to use contaminant-sensitive promoters to activate genetic machinery to produce a more detectable change in the organism in response to the contaminant, i.e. by producing reporting gene products [6]. Presence of contaminant thus promotes the production of gene products that cause a more measurable phenotypic change in the organism, i.e. bioluminescence, fluorescence, etc. In our approach, the bioluminescent reporter genes, lux, produce blue-green light (490 nm) which can be measured rapidly and with high sensitivity. The lux genes were originally cloned from the marine bacterium *Vibrio fischeri*. By introducing the genes into the catabolic gene loci of bacteria without native lux sequences, the production of 490 nm light from the transformed bacteria is dependent only upon contaminant exposure. The amount of light produced is dependent upon the level of expression of the reporter gene, and thus upon the exposure level to the inducing pollutant.

Engineered bacteria containing the lux gene cassette have already been implemented as bioreporters for a wide variety of environmental contaminants. As early as 1990, whole cell bioluminescent bioreporters were developed with the appropriate regulated metabolic operons and were shown to function in complex environmental matrices as remote sensors [6]. Bioreporters for detection of zinc, cadmium, cobalt, lead, mercury, copper and nickel have also been reported in the literature [7]. The University of Tennessee pioneered the use of bioluminescence in environmental chemical sensing through development of bioreporter bacterial strains harboring bioluminescent (bacterial) lux gene fusions with promoters specific for detection of aromatic hydrocarbons [8]. Several bioluminescent bioreporters have been constructed at UT-CEB for the detection of naphthalene and salicylate BTEX compounds (benzene, toluene, ethyl benzene, xylene) [9], polychlorinated biphenyls [10], dinitrotoluene, 2,4-dichlorophenoxyacetic acid and dichlorophenol [11] and heavy metals [12]. Bioreporters have been used to screen for single or several chemically related compounds simultaneously. For example, a bioluminescent bioreporter was constructed at UT-CEB for the specific detection of toluene using the promoter from the tod operon [8]. The bioreporter demonstrated increased bioluminescence with increased concentrations of toluene. In addition to toluene, this bioreporter responded to other BTEX compounds and trichloroethylene [8] with highly sensitive detection limits of approximately 30 μg/L.

Proof-of-concept for field application of bioreporter technology has been observed in studies demonstrating reproducible bioreporter based

bioluminescence in aqueous and soil slurry samples which contained naphthalene, in complex soil leachates, and in water-soluble components of jet fuel [13]. Pseudomonas sp. bioreporter bacteria were shown to function as reagentless, living whole cell biosensors and ultimately the organisms were approved for field testing by the EPA and were environmentally released at the Y-12 facilities at ORNL [14]. Bioreporter cells in this controlled field test have maintained functional status in the environment for 3 years. Non-chip-based bioluminescent techniques for spatial characterization of naphthalene and toluene equivalents in contaminated soil at the Natural Attenuation Test Site at Columbus AFB, MS [15], have been applied with good correlation against GC/MS sample analysis.

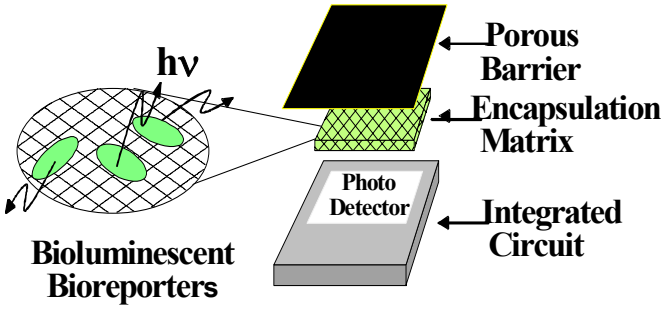
1.2 Bioluminescent Bioreporter Integrated Circuits (BBIC)

Bioluminescent Bioreporter Integrated Circuit (BBIC) contains bioluminescent bioreporters, which are bacteria that can be genetically altered to achieve bioluminescence when in contact with a targeted substance. The bioreporters are placed on a CMOS integrated circuit (IC) that detects bioluminescence, performs, signal processing and transmits the sensor data to a remote location. The basic building blocks of the integrated circuit are the microluminometer and the transmitter. The microluminometer includes integrated photo detector and signal processor and the transmitter performs wireless data transmission. The BBIC is housed in a rugged inexpensive package that can be used in many remote applications in hazardous environment. In addition, it also integrates all the features of detection, processing and transmission into one small element. The close proximity of the bioreporter and the sensing element

eliminates the need for complex instrumentation to channel light from the bioreporters to the microluminometer. In addition, the integrated wireless feature of the system will allow remote sensing without the need for bulky and costly cables to communicate with the sensors. Thus, the BBIC provides a low-power, inexpensive, selective and highly sensitive biosensor.

As shown in Figure 1.1, the whole-cell bioreporter matrix is housed in a metabolically supportive matrix that rejects ambient light while providing analyte/bioreporter interaction. The matrix also prevents the release of the microbes into the environment. The BBIC will also have contaminant mapping capabilities through incorporation of a global positioning system (GPS). In this format, BBICs could be hand placed or airdropped to conduct near real-time surveys and rapidly map contamination over large areas.

The microluminometer design is composed of three sections: photodetection, signal processing, and wireless transmission of the data. The sensor information is inherent in the intensity of light from the bioreporter. The light is then converted into an analog signal by the photodiodes. The function of the signal processing system is to convert photodetector current into a digital signal. The signal processor should be sensitive to the lowest possible intensity of light allowing the BBIC to be sensitive to the lowest possible concentration of targeted substance. The minimum detectable signal (MDS) is an important design specification. The factors affecting MDS are: quantum efficiency of the photo detector, leakage current, and the noise associated with the signal processing.



Bioreporter:
- ***lux* genes for 490 nm light**
- **gene regulation element**

Porous Barrier:
- **Blocks Light**
- **Contains bacteria**

Encapsulation Matrix:
- **nutrients**
- **hydration**
- **protection**

Integrated Circuits:
- **Inexpensive**
- **Low-noise**
- **Rugged**
- **Digital signal processing**
- **Wireless transmission**

Figure 1.1---Conceptual BBIC System Showing The Immobilized Bioreporter Inserted between A Porous Layer and The Integrated Circuit with A Photo Detector

1.3 Low Power BBIC Design

A BBIC sensor chip with lower power consumption was designed and fabricated in the 0.35μm CMOS process. This design was an improvement over a previous BBIC [1] in terms of power dissipation. Larger resisters are used instead of several small resisters, which were placed between power supply (V_{DD}) and ground to reduce power dissipation. Also, the bias currents for the amplifiers were reduced to decrease the power consumption further. The power consumption in the BBIC has been reduced to 3.5% of the previous chip [1]. The chip is tested using normal light condition and the tests demonstrated the implementation of the basic functions of the sensor. Some test results of the photodiode and signal processing circuit are presented. The transmitter system was designed following a previous work [2]. The power amplifier is added to the transmitter to give larger signal out of the circuit. The simulation has been performed using Cadence design tools.

CHAPTER 2

BBIC System Design and Requirements

2.1 Bioluminescent Bioreporter Integrated Circuits (BBIC)

Bioreporter combines a biological component with electrical circuits. The biological component acts as the measurement interface with process of interest producing a response that can be measured by an optical and electronic sensor. The most common biological component uses immobilized enzymes or antibodies tailored to measurement requirements. Other less utilized systems, referred to as whole-cell biosensors, include biological components with living microorganisms or sections of organs or tissues. Originally these biosensors were observed by detecting the activity of growing cells with electrochemical transducers. Normally, whole-cell biosensors function in controlled environments but are not applicable, because of growth on nutrients other than the target analyte causing interference in the measurement. Presently, bioluminescent bioreporters have become a popular measurement solution because a bioluminescent response is easily detected and the process under observation need not be destructive to the cells, which allows continuous real time monitoring. Bioreporters are genetically engineered for bioluminescence using both eukaryotic and prokaryotic cell lines that have been developed for the detection of water born toxins, pollutants, and soil contamination.

Bioluminescent Bioreporter Integrated Circuits (BBIC) combines genetically engineered bacteria and integrated circuit technology. BBIC consists

of three parts: (1) bioreporter and photodetector, (2) signal processing circuit, (3) RF transmitter, as shown in Figure 2.1. The bioreporters contact with analyte and produce bioluminescence, at 490nm wavelength. This bioluminescence is absorbed by the photodiodes, which produces photocurrent. Signal processing circuitry converts this photocurrent into square wave pulses, whose frequency is proportional to the photocurrent out of the photodiode. The transmitter up-converts the low frequency square wave pulses, which are about 1kHz into 916MHz RF signal [2]. The transmitter also includes a power amplifier and an antenna for signal transmission.

The electrical component of BBIC consists of a microluminometer and a RF transmitter. This project consists two tasks: (1) design of microluminometer for reduced power consumption; (2) incorporation of RF transmitter on chip.

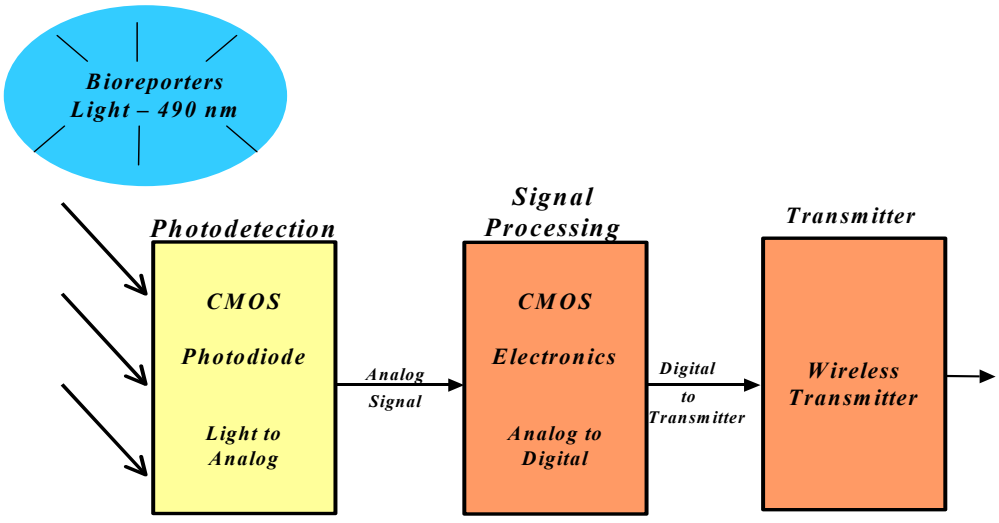


Figure 2.1---System Block Diagram of BBIC

2.2 Design Requirements for BBIC

For photo detection, since the bioluminescence is very low intensity light, the photodiode must have high efficiency to measure the smallest possible optical signal. In fact, it cannot be seen under normal light condition. Only in a dark room, with all the lights turned off, the bioluminescence can be observed as a faint green light. The photodiode for measuring the luminescence of the bioreporters can be integrated in the same CMOS chip along with other parts of the BBIC. In the new BBIC, realized in a standard 0.35μm CMOS process, the structure of *p*-diffusion/*p*-substrate/*n*-well/*n*-diffusion is used.

For signal processing part, it is important to achieve high power efficiency. This part will convert the photocurrent generated by the photodiodes into a square wave signal of variable frequency. The frequency depends on the amount of photocurrent. The larger the photocurrent, the higher is the frequency of the square wave. The square wave is modulated to transmit the information of the photocurrent by the RF circuits that follow. Because optical signals are very small, this portion of the system should introduce as little error as possible into the measurement. Since BBIC chip is designed be used in the field environment, the system must be designed to consume as little power as possible to use batteries as power supply.

The basic requirements of the transmitter include low power dissipation, small size, and the carrier frequency of 916MHz. For battery operation, a sleep mode is required to turn the transmitter off when the bioluminescent signal need not be detected and transmitted. This scheme will conserve energy as the

transmitter is extremely power hungry and dissipates most of the power in the BBIC system. Moreover, the transmitter should be designed to consume as little power as possible during its transmission mode.

Figure 2.2 shows the schematic of the BBIC. The specification of the BBIC can be summarized as follows:

Bioluminescent Bioreporters: specificity so that it produces bioluminescence when contacts with a specific pollutant.

OASIC: should be lower power, rugged construction, should be able to process analog and digital signals, and should possess high functional density.

Wireless Transmitter: should transmit the data at 916MHz carrier frequency with low power dissipation.

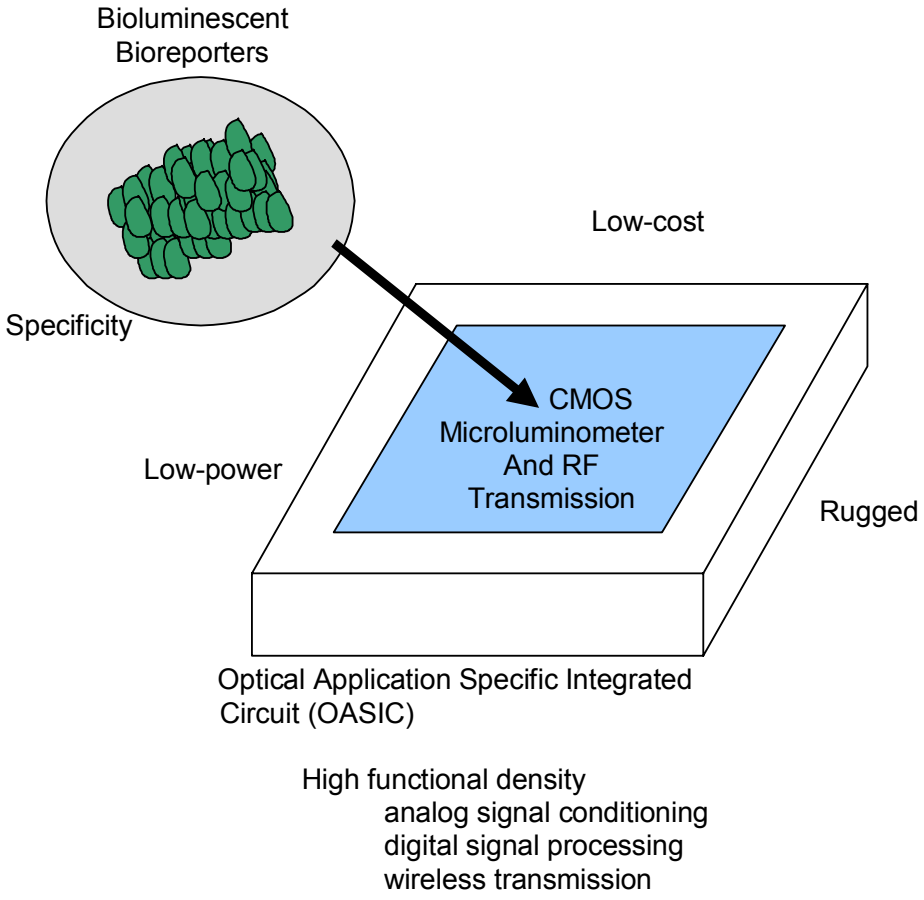


Figure 2.2---Low Power, Low Cost, and Rugged BBIC Chip [1]

CHAPTER 3

Microluminometer System and Test Results

3.1 Circuit Structure of Microluminometer System

Microluminometer system is made up of two sections: photodiodes and signal processing circuit. The intensity of light from the bioreporters represents the concentration of the targeted substance. This light is absorbed by the on chip photodiodes, which will convert the light into photocurrent. And the signal processor will convert the photocurrent into square wave pulses as the output signal of the microluminometer system.

The microluminometer has to be sensitive enough to detect the lowest possible intensity of light, or the lowest possible concentration of the targeted substance. The most important concerns about the microluminometer system are the quantum efficiency of the photo detector, the leakage current of the detector, the power consumption, and the noise of the signal processing circuit. And our future goal is to include every component in one CMOS chip.

3.1.1 Photodiode

The structure *p*-diffusion/*p*-substrate/*n*-well/*n*-diffusion is used as shown in figure 3.1. *P*-substrate/*n*-well is the essential part to generate photocurrent. *P*-diffusion and *n*-diffusion are used to collect the photocurrent more efficiently, which are also important.

Figure 3.2 and figure 3.3 shows the process of converting light into photocurrent and biasing theory. When a photodiode absorbs light, and if the

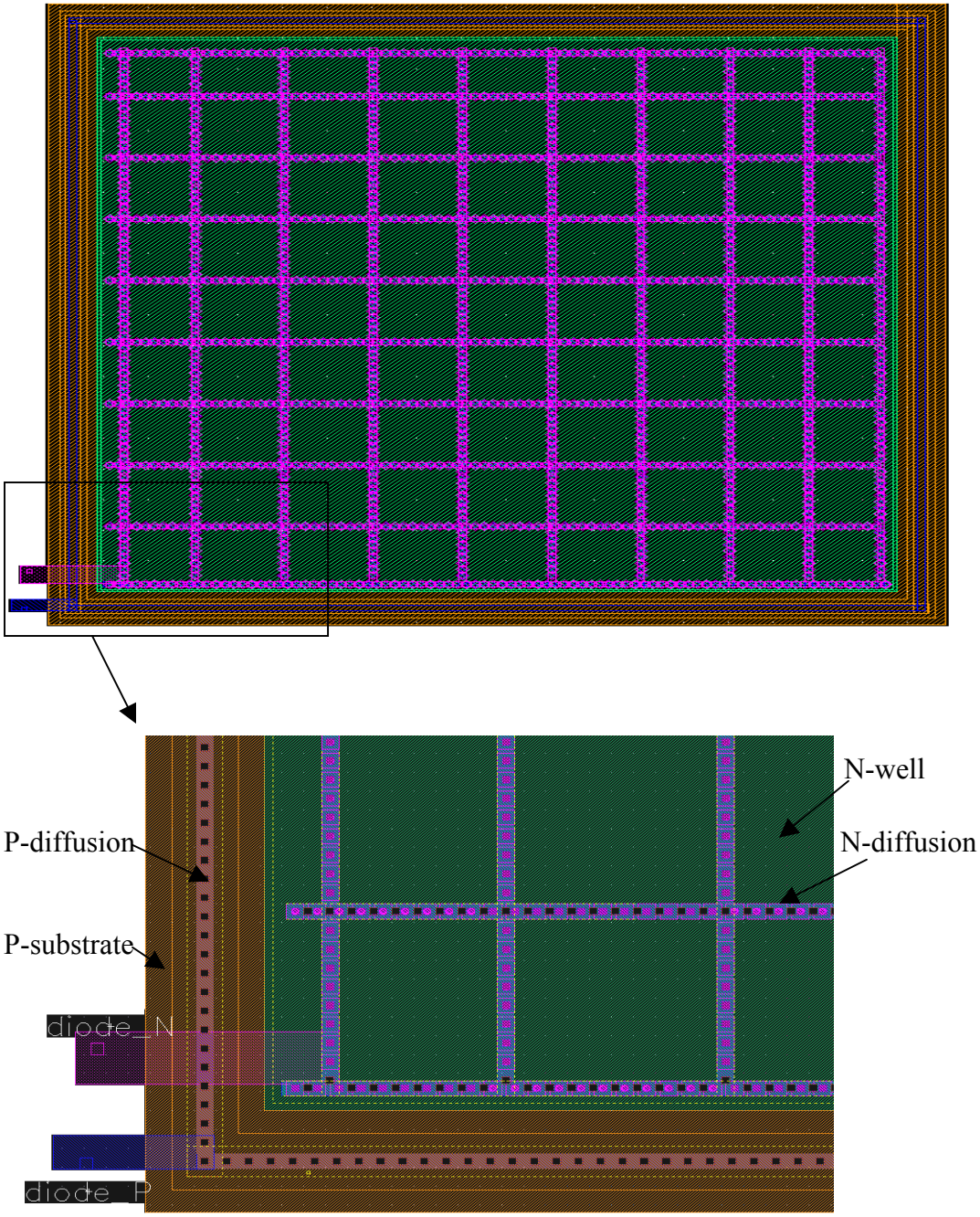


Figure 3.1---Layout of Photodiode

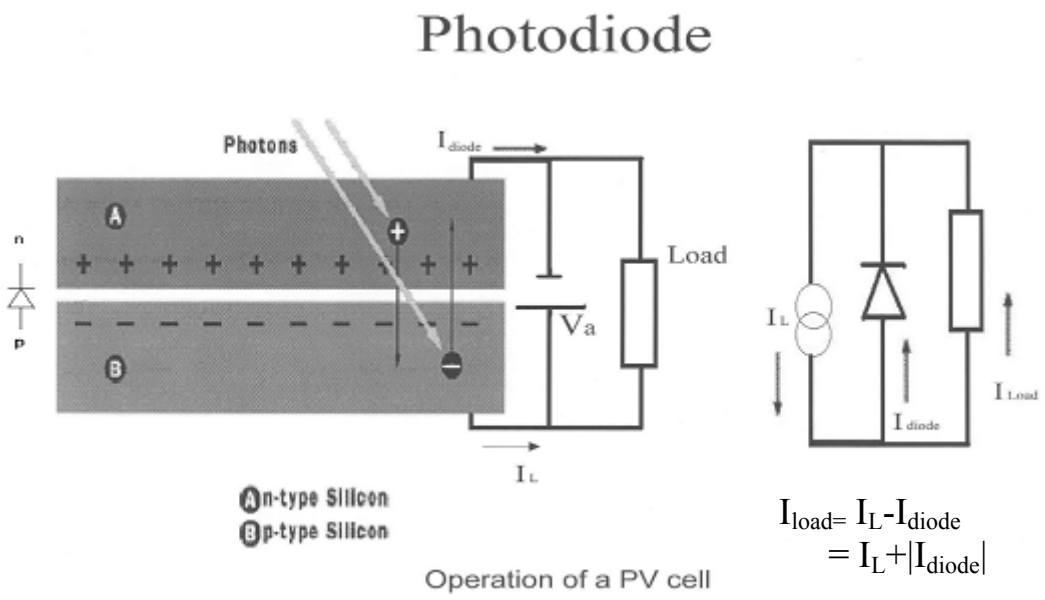


Figure 3.2---Working Process of Photodiode

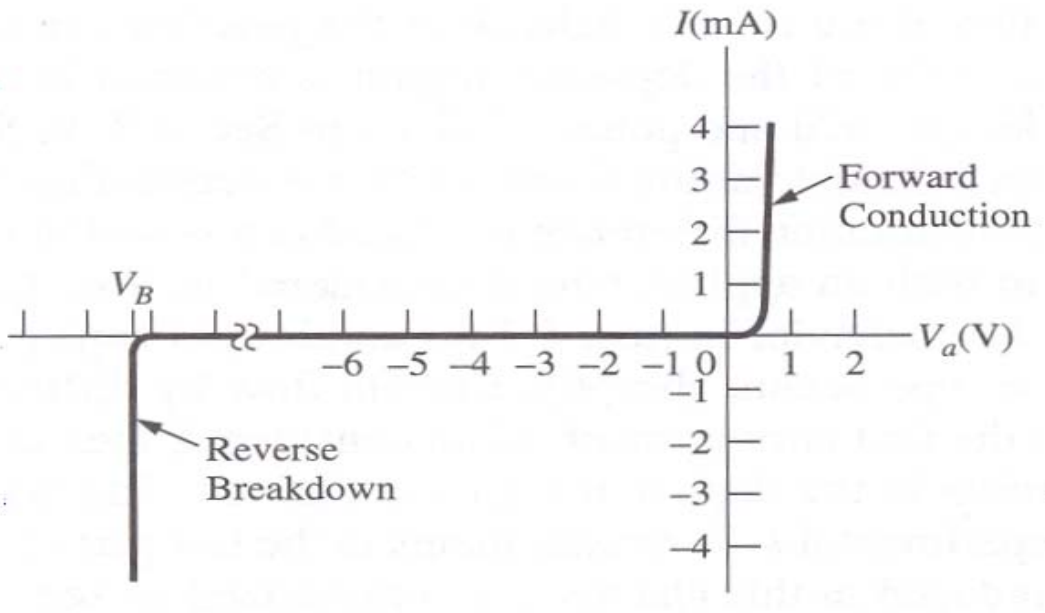


Figure 3.3--- Photodiode Biasing

photon energy exceeds the band gap energy (E_g), electrons in the valence band will jump onto the conduction band after they absorb the energy of the photons. The band gap energy of Si is typically 1.125 eV [16]. Photocurrent will be formed if these electrons cross the p-n junction. Electrons in or near the depletion region will be accelerated to the terminals of the diode by the electric field. Few carriers created at a distance greater than a diffusion length from the depletion region could be collected as the photocurrent [17].

In figure 3.2, V_a is the forward bias voltage. In BBIC sensors, V_a value is either zero or negative. So actually, I_{diode}, which is also I_d, flows in the direction as I_L, which is the photocurrent. Then the total current flow from n-type to p-type inside the photodiode is $|I_d|+I_L$. Without light incidence, there will also be $|I_d|$, which looks like a photocurrent. So $|I_d|$ here is also called leakage current for BBIC sensor. $|I_d|$ is proportional to junction area and increases quickly with an increase in temperature. So temperature fluctuations should also be concerned.

The effectiveness of a photo detector in converting light to photocurrent is known as quantum efficiency (η) as given by [18].

$$\eta = \frac{I_p \cdot h \cdot \nu}{P_{op} \cdot A_{\det} \cdot q} \cdot 100\% \tag{3.1}$$

Where I_p is the photocurrent (A), h is Planck's constant (6.626×10^{-34} J •Sec), ν is the frequency (Hz) of the incident light, P_{op} is the power (W/cm^2) of the incident light, A_{det} is the detector area (cm^2), and q is the charge of an electron (1.602×10^{-19} C).

Ideally photodiode's quantum efficiency should be 100 %. But because not all the incident light can be absorbed, real photodiodes have lower quantum efficiencies. The absorption possibility of an incident photon is related to the distance between its generation place and the depletion region [19].

$$F_{abs}(d) = F_0 \cdot [1 - e^{-(\alpha \cdot d)}] \tag{3.2}$$

Where F_{abs} (d) is the number of photons absorbed, distance d is the distance between the surface of the semiconductor and the depletion region, F_0 is the number of incident photons, and α is the absorption coefficient, and α is related to a particular semiconductor and the wavelength of incident light. Figure 3.4 [19] shows the absorption coefficient for various semiconductors. The coefficient is inversely proportional to the wavelength of light. The detectors made of Si are more effective to absorb shorter wavelengths of light. The wavelength of the light out of BBIC bioreporters is near 490nm [20]. So silicon can detect this bioluminescent efficiently.

Photodiode capacitance is an important parasitic component. This capacitance, which is in parallel with the diode, is essential the junction capacitance and proportional to photodiode area. This capacitance will make the transient response of the BBIC sensor worse.

A current source I_{ni}^2 (f) (A^2/Hz) represents the noise spectral density of the photodiode. The total diode noise includes shot noise, generation/recombination noise (g-r noise), flicker noise, and the thermal noise. Figure 3.5 [21] shows the frequency spectrum of the total noise in a photodiode. Flicker noise dominates at

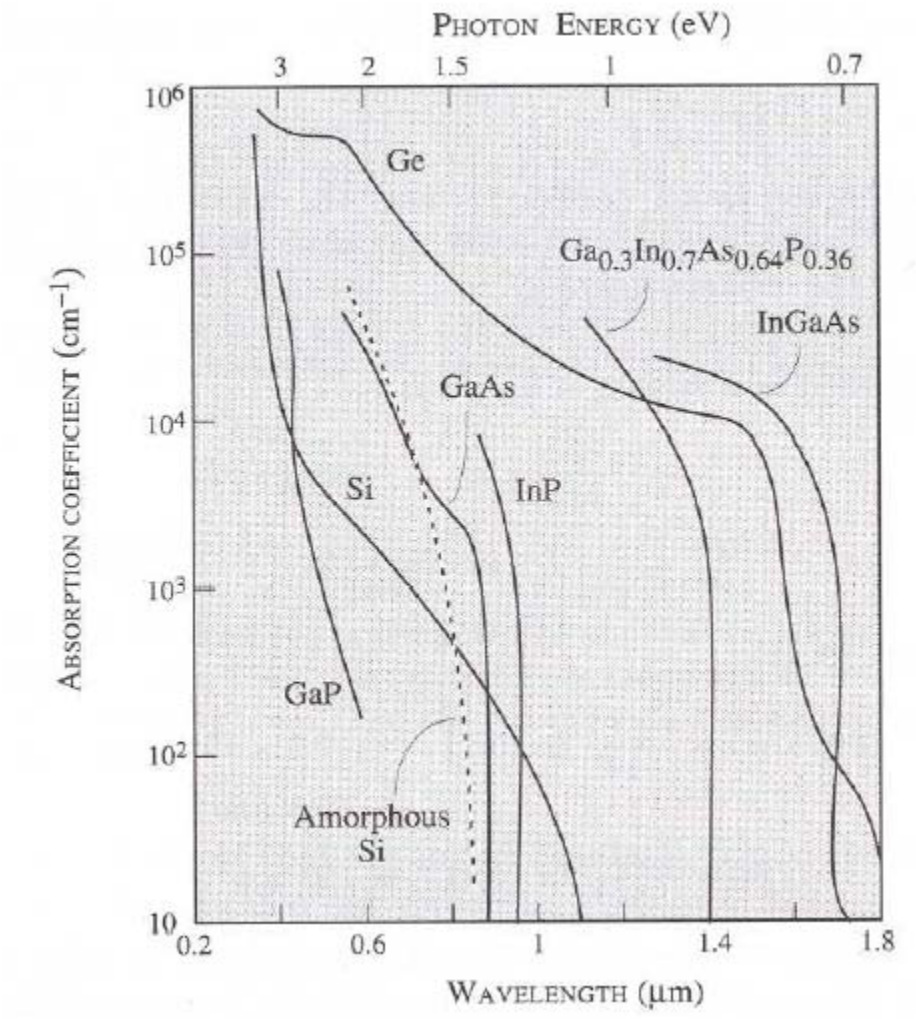


Figure 3.4---Absorption Coefficient for Various Semiconductors [19]

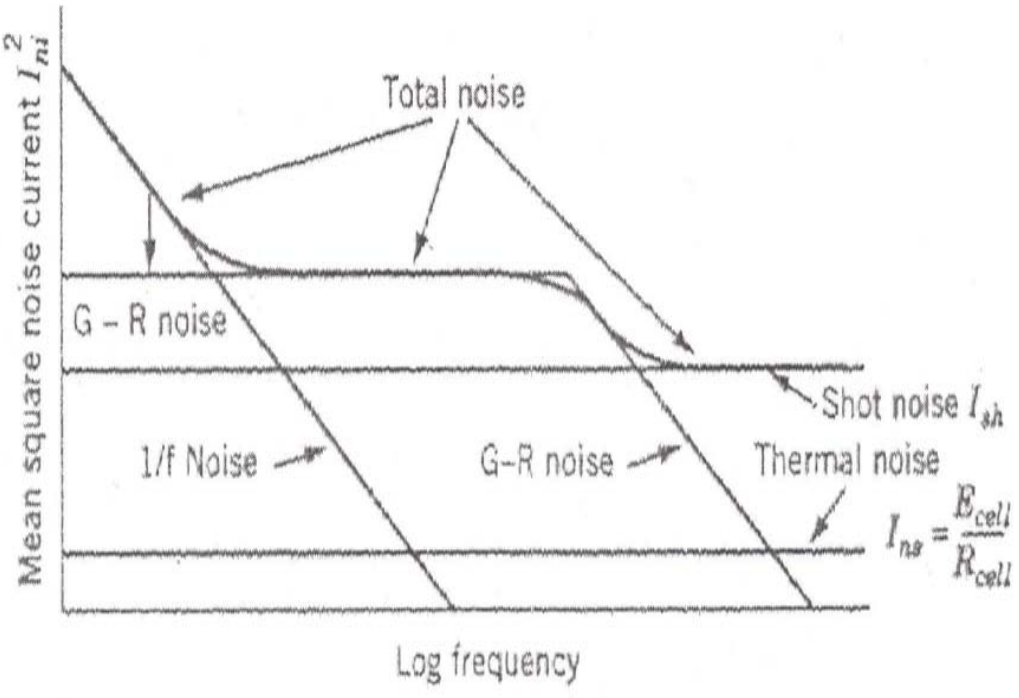


Figure 3.5---Photodiode Noise Current Spectrum [21]

low frequencies. The sum of the shot noise and g-r noise gives a flat spectrum at intermediate frequencies. The shot noise dominates at high frequencies.

3.1.2 Topology of the Signal Processing Part

The BBIC signal processing circuit converts current to frequency as shown in figure 3.6 [1]. When the photodiode is exposed to light photocurrent is created by the photodiode. The integrator then integrates the photocurrent. The output voltage of the integrator increases at a rate as given by,

$$S = \frac{I_p}{C_{\text{int}}}(\frac{V}{Sec}) \tag{3.3}$$

So the rate is proportional to the photocurrent I_p. When the output voltage increases to V_{th}, the threshold voltage of the comparator, the comparator output

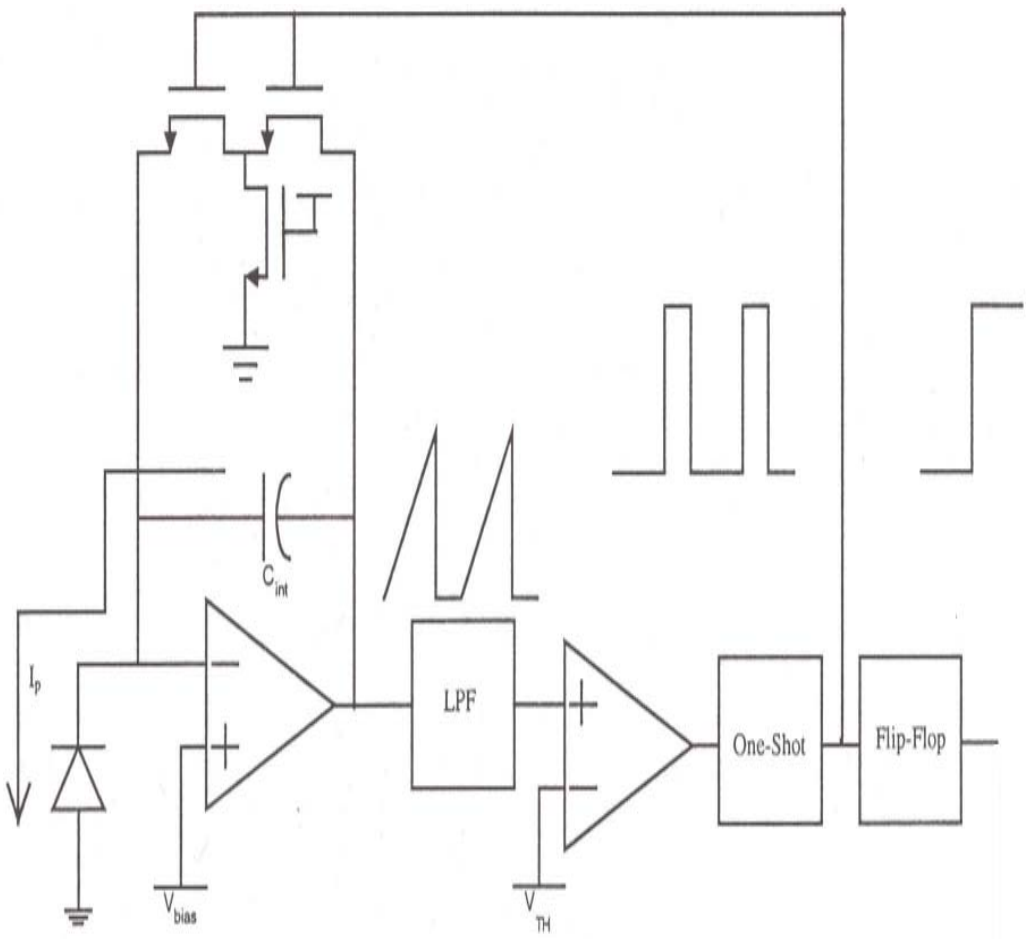


Figure 3.6---BBIC Signal Processing Circuit [1]

will give a narrow pulse. This narrow pulse will trigger a wider pulse out of the one-shot. Then this wider pulse will discharge the integration capacitor and reset the integrator. One-shot output is connected to a D flip-flop, which is working as a divide-by-2 frequency divider. So the output of the signal processing circuit will be square waves, whose frequency is proportional to the incident light to the photodiode.

Ideally, the output wave shape look like as shown in figure 3.7. The integrating time is:

$$T_{\text{int}} = \frac{C_{\text{int}} \cdot (V_{TH} - V_{bias})}{I_p} (Sec) \tag{3.4}$$

The period of the one-shot output is:

$$T_{os} = T_{\text{int}} + T_{reset} \approx T_{\text{int}} (Sec) \tag{3.5}$$

T_{reset} is the pulse width of one-shot output. During T_{reset}, the capacitor in the integrator is discharged. For BBIC chip, T_{reset} is mostly much smaller than T_{int}. So $T_{os} \cong T_{int}$. The frequency out of the D flip-flop is

$$f_{out} = \frac{2}{T_{os}} = \frac{2 \cdot I_p}{C_{\text{int}} \cdot (V_{TH} - V_{bias})} (Hz) \tag{3.6}$$

Equation (3.6) gives the relationship between I_p, the photocurrent out of photodiode, and f_{out}, the frequency out of the signal processing circuit.

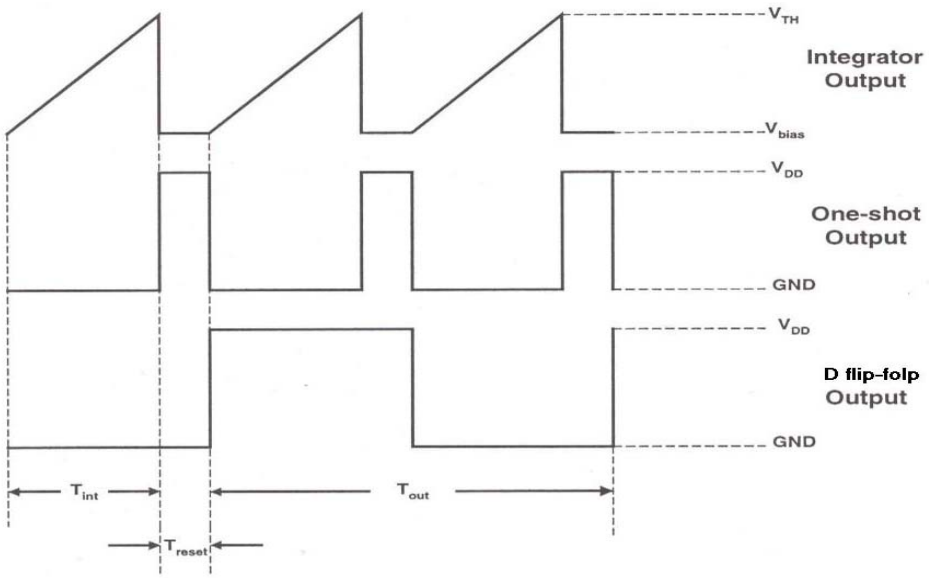


Figure 3.7---Signals in Signal Processing Circuit [1]

3.1.3 Signal Processing Components

3.1.3.1 Integrator

The integrator is composed of an amplifier, an integration capacitor and a switch as shown in figure 3.8.

In the 0.35μm technology used for realizing the BBIC, two-poly capacitor was used for the integration capacitor. The capacitance is about 0.3pF. But the previous chip uses a value of 0.5pF.

3.1.3.1.1 T-switch

T-switch is used to discharge the integration capacitor during reset. Figure 3.9 shows the T-switch circuit. The voltage on the gates of the upper two NMOS controls the operation of the T-switch. When the gate voltage is high, the gate–source voltage is higher than the threshold voltage, and these two transistors will

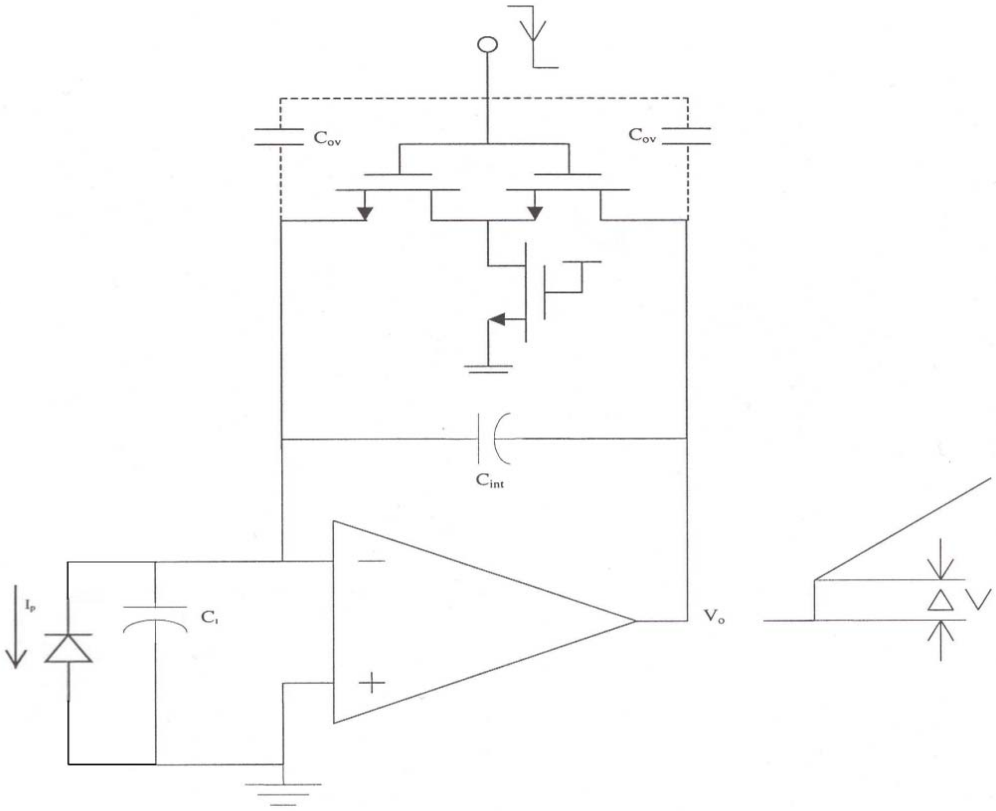


Figure 3.8---Integrator Structure [1]

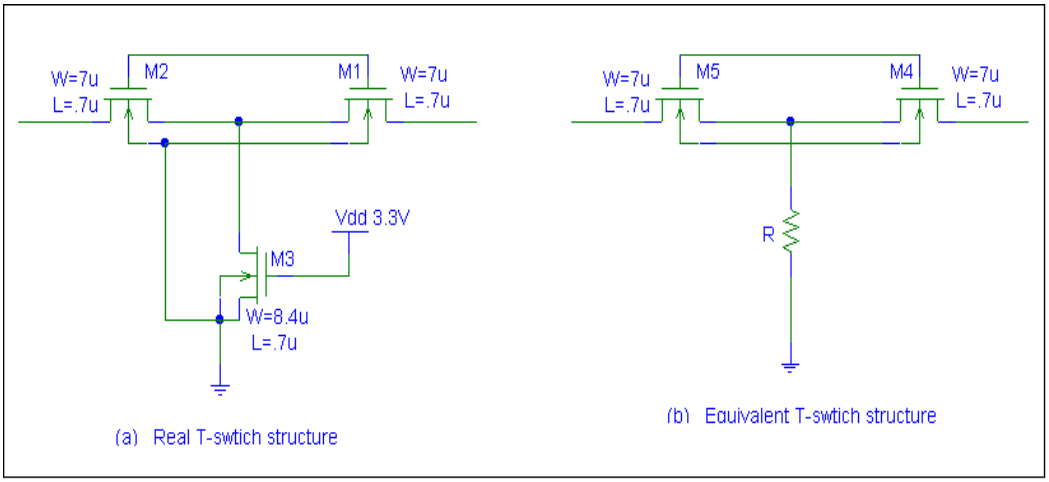


Figure 3.9---T-switch Structure

be turned on. The integration capacitor will be discharged, and the integrator will be reset. When the gate voltage is zero, the upper two transistors are turned off., and the integrator begins to integrate. T-switch will introduce some errors, charge injection and switch leakage.

When a MOS switch is opened, charge injection error will appear. When the MOS switch is closed, the gate to source voltage is higher than the threshold voltage. The channel charge of the MOS will be [22]:

$$| Q_{CH} | = W \cdot L \cdot C_{ox} \cdot (V_{GS} - V_T) \tag{3.7}$$

When the gate voltage falls to zero, the switch is opened, and the channel charge disappears from the devices. This charge flows equally into the drain and source terminals [23] if the device is switched quickly, as shown in figure 3.8. Part of the charge flows to the input. The integration capacitor will collected it, and an offset voltage will appear at the output. The offset voltage at the output is equal to

$$\Delta V_{OS1} = \frac{| Q_{CH} |}{2 \cdot C_{\text{int}}} \tag{3.8}$$

There are two error components at the output. The first is the offset due to charge injection and the integration capacitor as discussed above. The second error is related with the voltage change of the upper two transistors in T-switch. The change of the gate voltage produces a current. After it flows into the integration capacitance, an additional offset voltage will be produced, which is:

$$\Delta V_{OS2} = \frac{C_{ov} \cdot \Delta V_{sw}}{C_{\text{int}}} \tag{3.9}$$

Where C_{OV} is the gate-diffusion overlap capacitance of the MOS, ΔV_{sw} is the voltage difference at the gate. The sum of these two offset errors is the offset voltage, V_o, shown in figure 3.8.

There are two ways to reduce the offset voltage error. One is to reduce the area of switching transistors, using a low amplitude signal to turn on the transistors, and to use a large integration capacitor. Another way is to switch the transistors with a lower frequency. In this way, the channel charge will exit from each side of the switch unequally [24], and reduce the amount of charge flowing into the integration capacitor.

When the switch is open, there will still be some current that flows though the switch, which is called switch leakage. In the first version of the BBIC [25] the reset switch is a single NMOS transistor as shown in figure 3.10. When the transistor is off, the switch leakage is a big problem. The leakage current includes sub threshold current, surface leakage current and package leakage current [24]. A MOS transistor is in the deep sub-threshold region during the off condition. This sub-threshold drain current reduces the detector current. When low levels of photocurrent are detected, this effect presents a serious problem. So T-switch is used to reduce the leakage current of the transistor.

3.1.3.1.2 Amplifier

(1)Amplifier Structure

The amplifier system is comprised of three blocks. They are the first-stage amplifier, the second-stage amplifier and low-dropout output buffer.

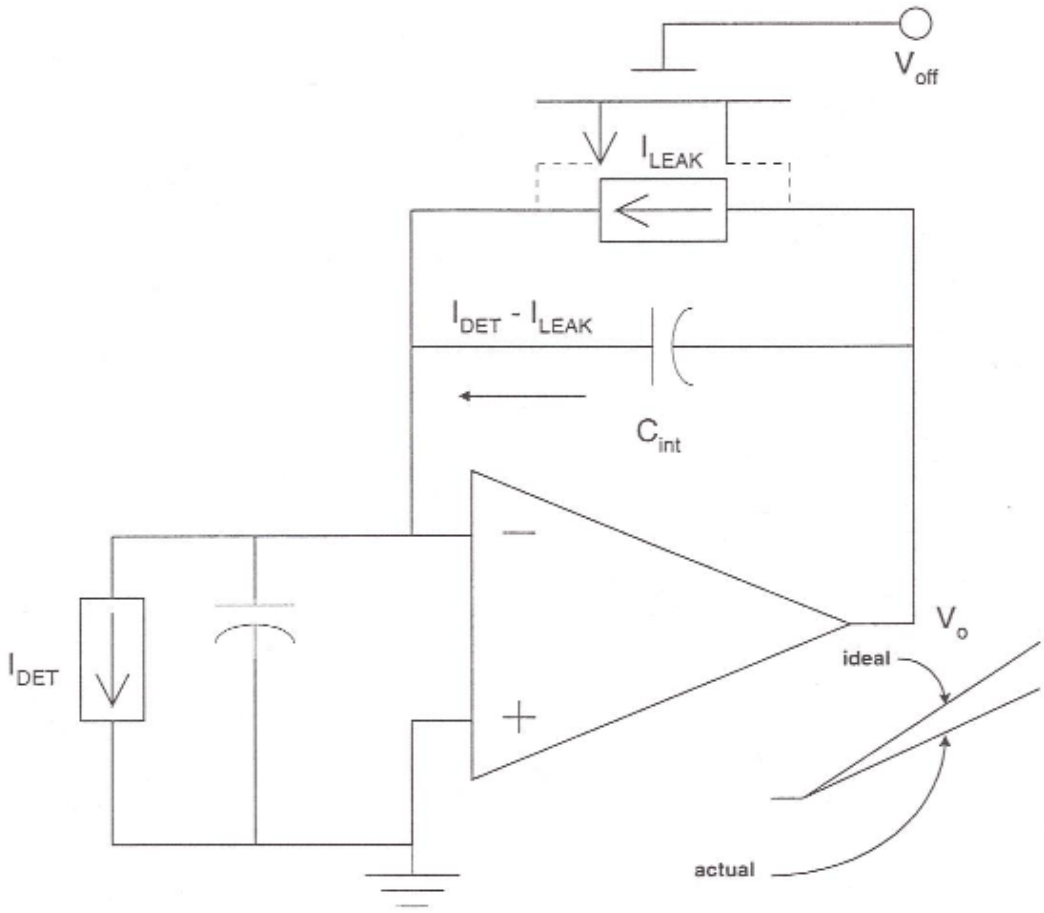


Figure 3.10---Original BBIC Switch Leakage Error [1]

The first-stage amplifier is a low-noise amplifier as shown in figure 3.11. Making the gain of the input stage very large minimized the noise contribution of the input stage. So, compared with the input stage, the noise of the rest of the amplifier is insignificant. Because a folded cascode topology has low noise characteristics, it was used as the input stage. A secondary consideration was to reduce the flicker noise of the NMOS cascode devices. This is achieved by using large cascode devices and inserting source resistors, which will minimize the noise through source degeneration.

A second gain block increases the total gain of the amplification stage. Simulations [1] were performed with the addition of an ideal gain stage with an RC low pass filter, to model a dominant pole amplifier. These simulations determined how the second gain block would affect the stability of the network. These simulations showed that a small additional gain could be between 10 and 50 with only minor changes necessary in the compensation configuration to give proper phase margin. A closed-loop feedback configuration is an easy way to establish a small accurate gain. So the second-stage amplifier, shown in figure 3.12, is an amplifier with resistive feedback connected non-inverting with a gain of 11. Figure 3.13 shows the feedback connection.

The output dynamic range of the amplifier block is important. The low-dropout output buffer [1], shown in figure 3.14, gives a dynamic range that reaches close to zero volt. The load on the output source follower is a low dropout current source. The current across R5 is about several μA. R5 is 100- ohm. So the voltage across it is less than one mV. The feedback configuration keeps the

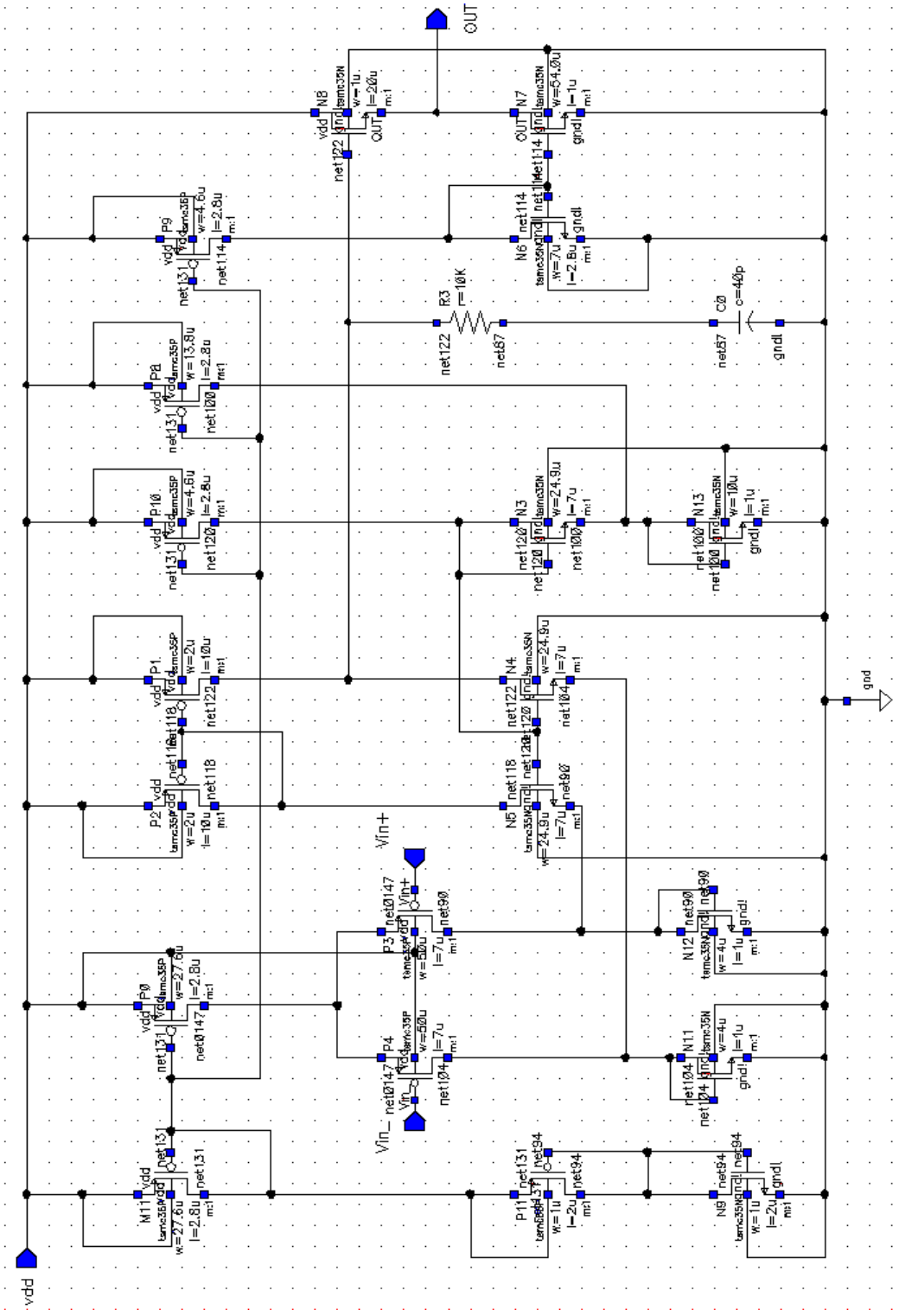


Figure 3.11---First-stage Amplifier

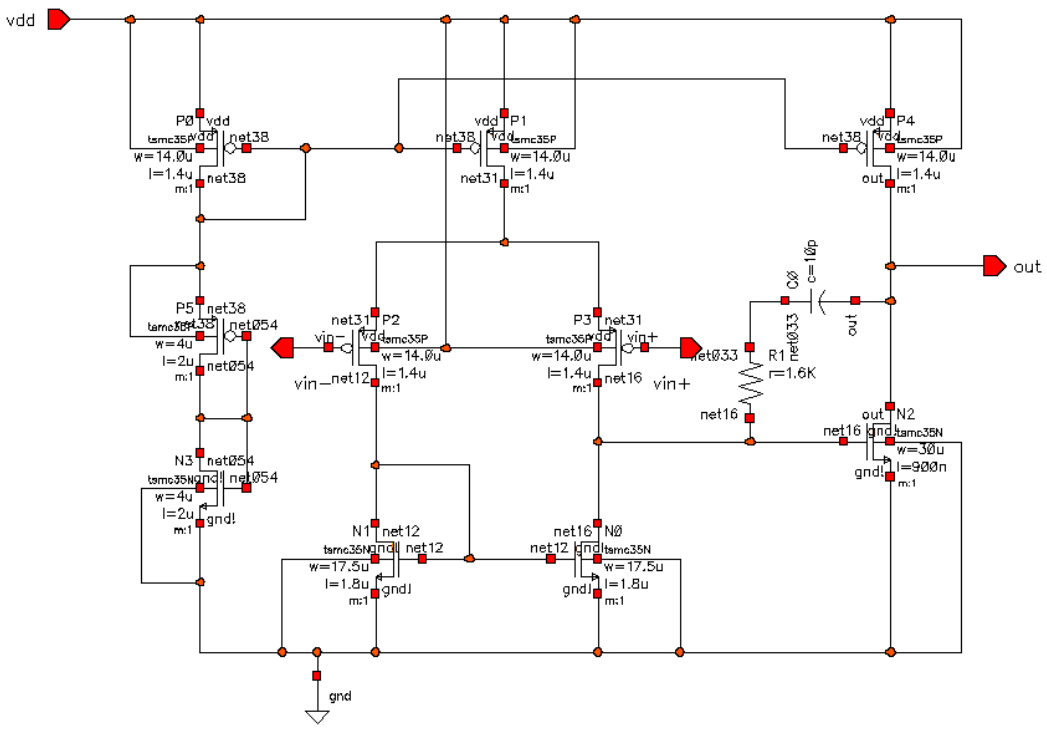


Figure 3.12---Second-stage Amplifier

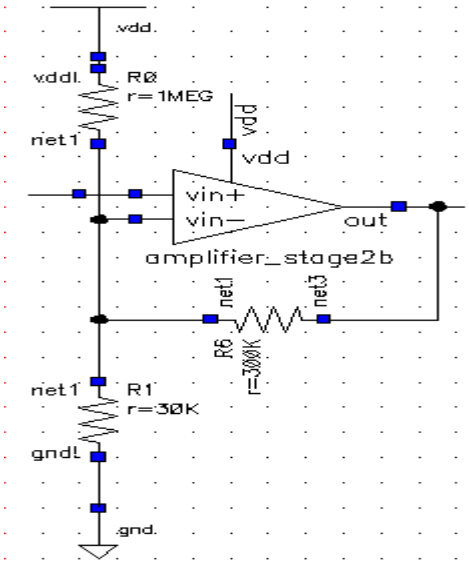


Figure 3.13---Feedback Connection of Second-stage Amplifier

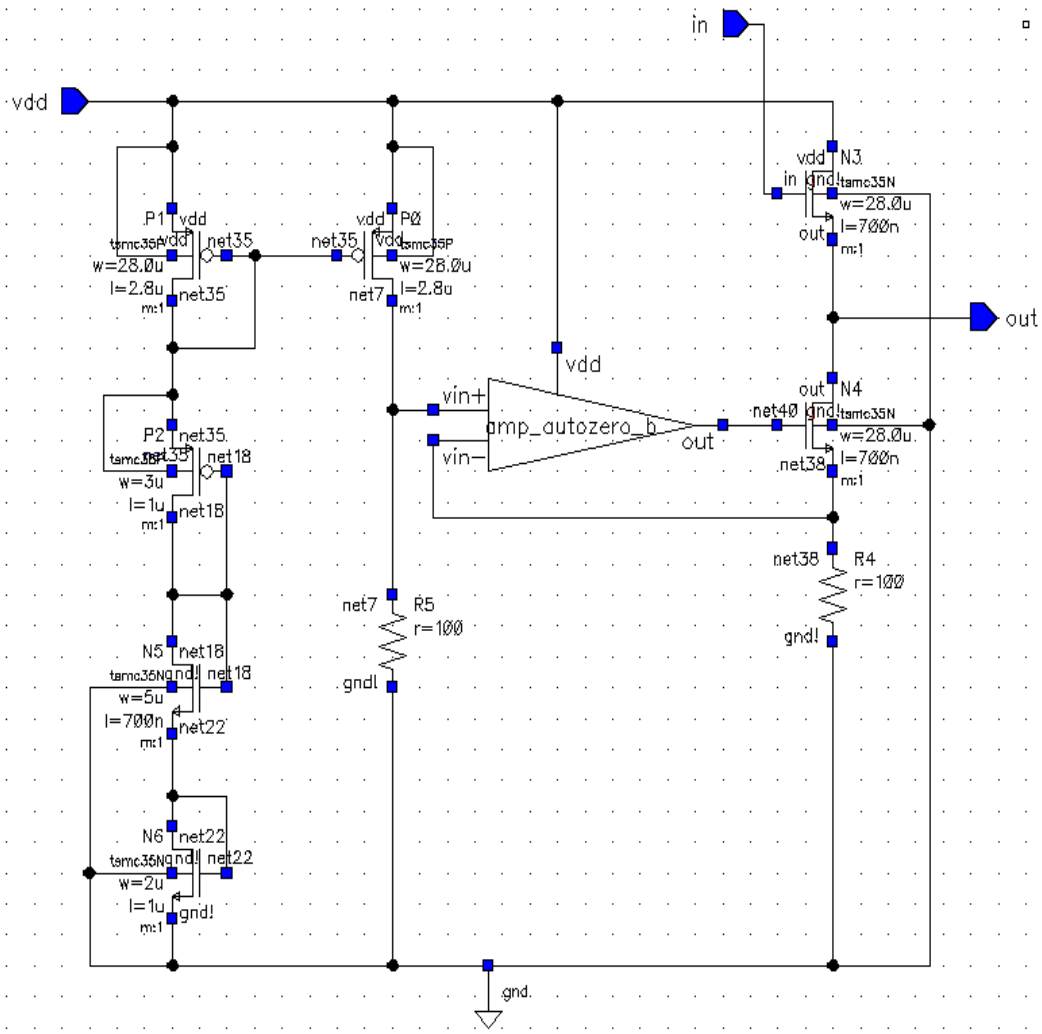


Figure 3.14---Low-dropout Output Buffer

voltage across the second 100-ohm resistor R4 to achieve low level and sets up a constant drain current for N4. So the output is the voltage drop across the 100-ohm resistor plus V_{ds} of N4. The output will be small even when the transistor N4 falls out of saturation, if input is low. Because when V_{an} is low, N3 will be turned off. The circuit includes two small, and well-matched on-chip resistors. The layout of the resistors should be done carefully to assure proper matching of the devices. Interdigitation techniques and "dummy resistors" should be used to match the two small resistors. The output voltage could be as low as 1 or 2 mill volts with the use of this output buffer.

The combination of the front-end low-noise amplifier, the second stage non-inverting feedback amplifier, and the low-dropout output buffer make up the amplification stage in the integrator. Figure 3.15 shows the amplifier in low-dropout output buffer. The gain and phase plots of the composite amplifier were shown in figure 3.16. The phase margin of the composite amplifiers is 65.5°.

The previous version of this composite amplifier used small resistors to bias the second-stage amplifiers input. R1 is 1k ohm, and R0 is 2k ohm. They consume almost half of the total power of the BBIC sensor circuit. So these two resistors were enlarged a lot to reduce the power consumption. And the bias currents for the amplifiers in the amplifier block are too large. So they were also reduced to reasonable values.

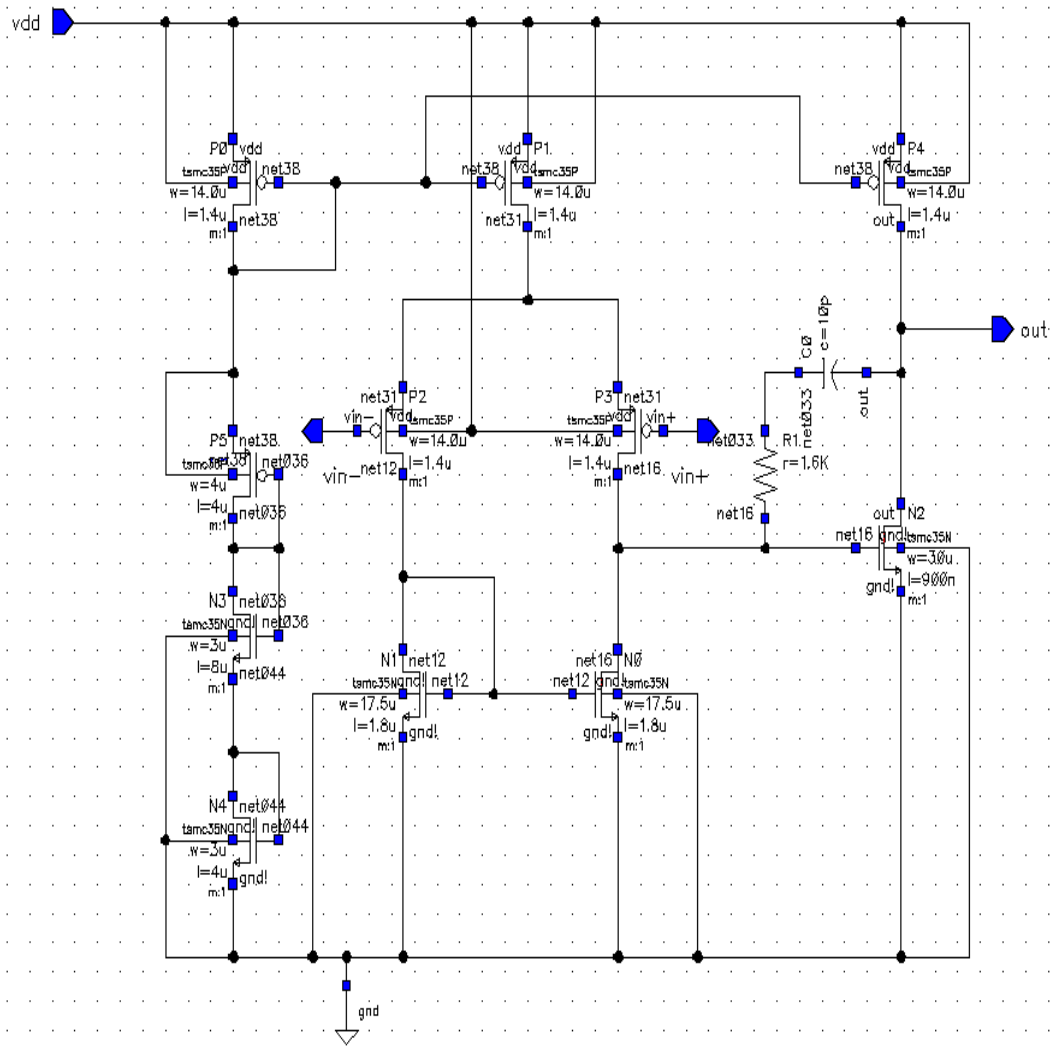


Figure 3.15---Amplifier in Low-dropout Output Buffer

Circuit schematic to measure the phase margin of the composite amplifiers

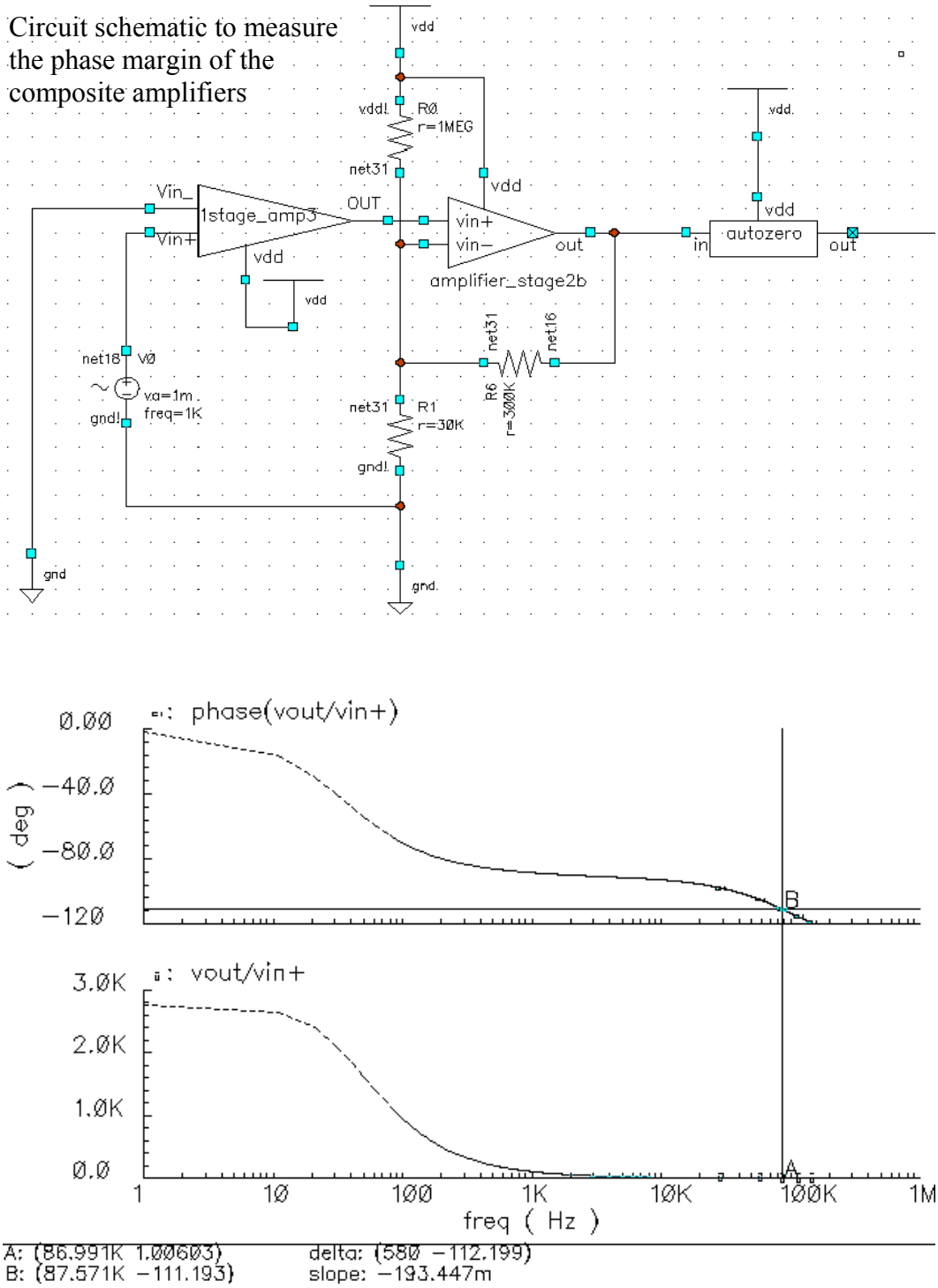


Figure 3.16---Open Loop Phase Margin of the Composite Amplifier, Phase Margin=65.5°

(2)Amplifier Noise

Amplifier noise has two parts, V_{os} and S_v (f), as shown in figure 3.17. V_{os} is the offset voltage of the amplifier. When it is applied to the amplifier input, the output will be set to zero [26]. The polarity of the offset voltage is not known and is related to different amplifiers. It includes random offset and systematic offset. Mismatches in devices causes random offset and systematic offset is inherent to the amplifier design [22]. Because the offset voltage adds an unintentional bias on the detector, it induces an error in the system. With the low bias on the detector, this error could become significant. The offset voltage also results in a shift in the lowest value of the integrator output, and causes measurement errors.

The voltage source S_v (f) in figure 3.17 is the intrinsic noise of the amplifier. The noise spectral density of the amplifier includes white thermal noise and flicker noise. The flicker noise spectrum is

$$S_v(f) = E_{th}{}^2 \cdot (1 + \frac{f_c}{f}) \qquad (\frac{V^2}{Hz}) \tag{3.10}$$

Where $E_{th}{}^2$ is the thermal noise power, and f_c is the flicker noise corner frequency. At the corner frequency, the white noise power spectral density is equal to that of the flicker noise. The intrinsic noise of the amplifier causes random voltage variations at the output of the integrator. So the integration time also varies randomly.

3.1.3.1.3 Reset Error of Integrator

Gain error will occur with insufficient gain and a large input capacitance. The input capacitance (C_1) includes both the input capacitance of the amplifier

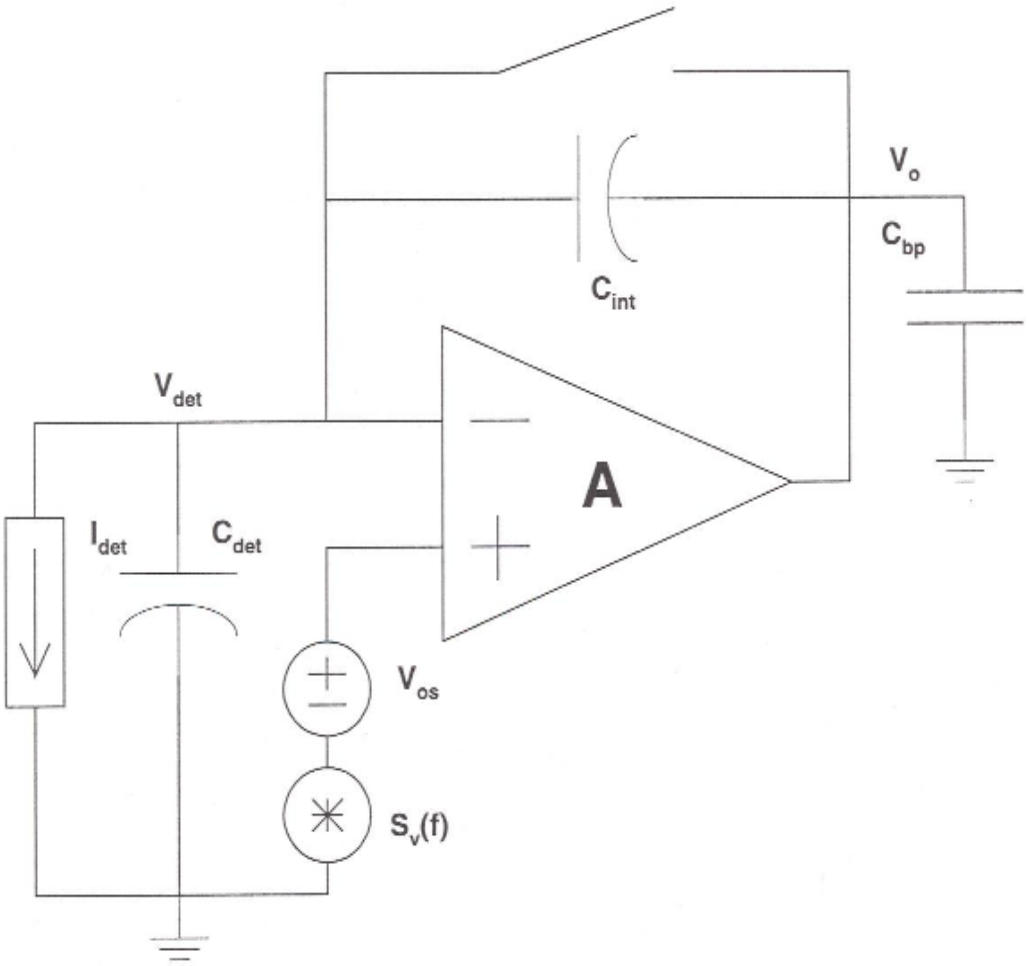


Figure 3.17---Amplifier Noise Analysis [1]

and the photodiode capacitance. For an ideal amplifier with infinite gain, the inverting input of integrator will be equal to the voltage at non-inverting input. But if an amplifier has a finite gain (A), the detector voltage will increase as the integrator output voltage increases. The relationship between these two voltages is give as:

$$V_{\text{det}} = \frac{V_0}{A} \tag{3.11}$$

The voltage change at the input causes a current to flow onto the input capacitance. So some photocurrent will not flow into the integration capacitor C_{int}. It flows into the input capacitance. The effective integration capacitance is shown as:

$$C_{eff} = \frac{C_i + C_{\text{int}} \cdot (A+1)}{A} \tag{3.12}$$

The error becomes negligible if the product of the integration capacitance and amplifier gain is much larger than the input capacitance. For BBIC system, the input capacitance is very large compared with the integration capacitance. So BBIC requires a large amplifier gain to reduce integration error.

The gain of the amplifier should always be kept constant. If the output of the integrator exceeds the dynamic range of the amplifier, the amplifier gain will decrease. So the dynamic range of the amplifier should be large enough to include the whole range of the integrator output. If temperature changes, the gain can also change. Because in the future BBIC chip will be used outdoor where temperature changes a lot, the temperature dependency of the amplifier gain is also important.

If the amplifier has a high gain this error will be greatly reduced.

3.1.3.2 Low Pass Filter

After the integrator and before the input to the comparator, the signal passes though a low-pass filter. The purpose of the filter is to remove some high frequency noise due to the integrator and detector. The basic RC low-pass filter is used. See figure 3.18. The diode in the circuit is to provide a fast discharge path for the capacitor during reset. The filter has a transfer function given by

$$H(s) = \frac{1}{1 + s \cdot R \cdot C} \tag{3.13}$$

R and C should be chosen so that the bandwidth of the filter is low enough to remove higher frequency noise. But the product of them should not be too large so that they will not distort the wanted signal out of the integrator.

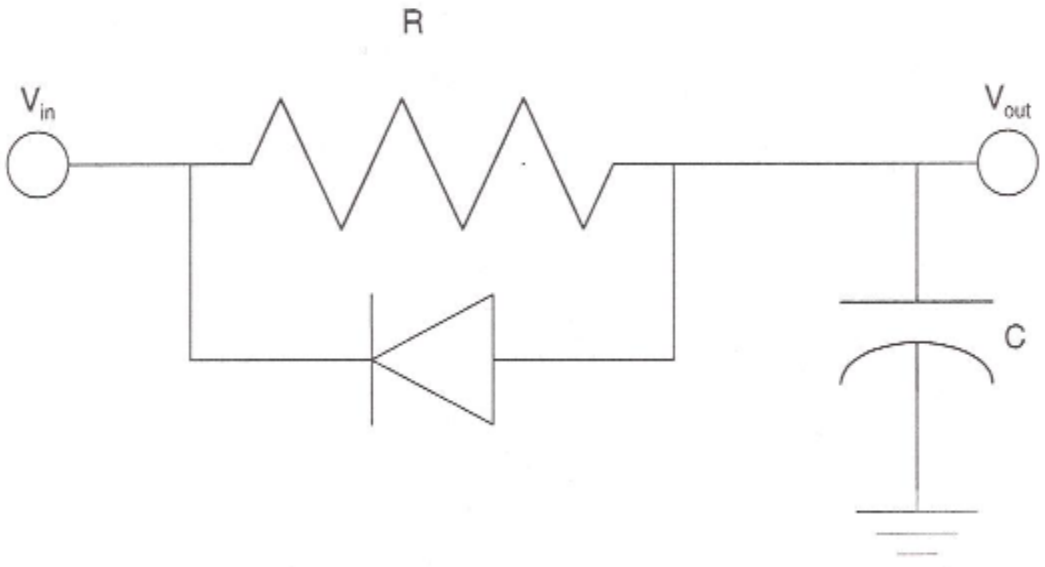


Figure 3.18---Low-Pass Filter [1]

3.1.3.3 Comparator

The comparator used in BBIC is shown in figure 3.19. When the output of the integrator reaches the threshold voltage, the comparator output becomes high. The integrator output is connected to the non-inverting inputs of the comparator and threshold voltage is connected to the inverting input. Ideally the offset voltage for a comparator should be zero, so that the output transition occurs just after the integrator output reaches the threshold voltage. With temperature changes, small offset errors can result in integration time errors.

3.1.3.4 One-shot

Figure 3.20 shows the one-shot in the previous chip. An alternate one-shot was designed for the new chip, which is shown in figure 3.21. This one-shot also works fine. Figure 3.20 is the correct schematic of the one-shot in the previous chip. This one-shot should be a better choice, because the capacitor in this circuit is small enough to be made on a chip.

3.1.3.5 D Flip-flop

The D flip-flop (DFF), see figure 3.22, performs as a frequency divide by two. Every time the one-shot output gives a pulse, the DFF output changes. The connection of the DFF is shown in figure 3.23. The “Q-bar” is connected to D. The one-shot output is used as DFF clock signal. When the clock input changes from high to low, Q output changes states. So “Q-bar” output changes, which cause the D changes. At the next falling edge of the clock input, Q, “Q-bar”, and D change states again. So the DFF output is a square wave signal with one half

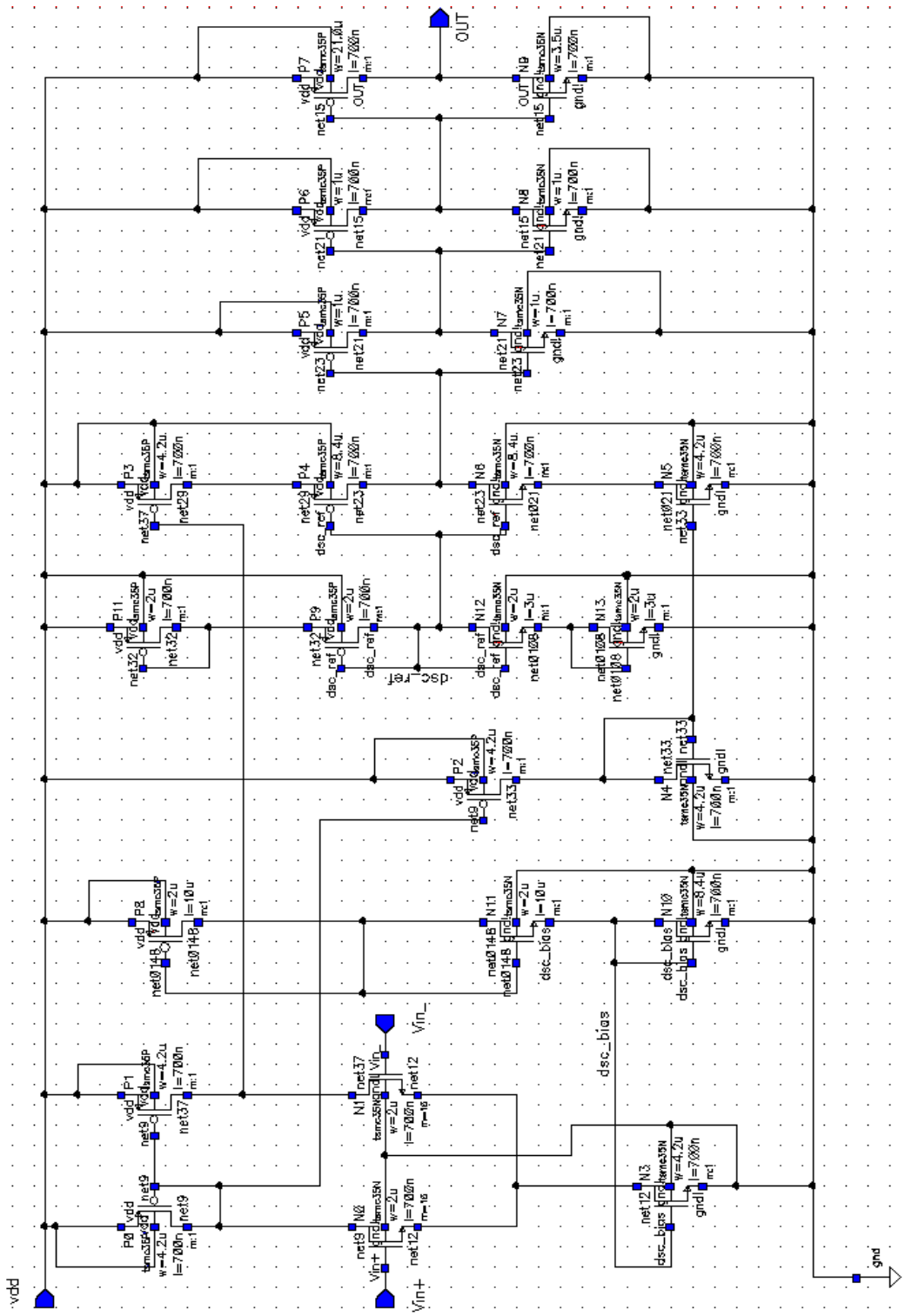


Figure 3.19---Schematic of Comparator

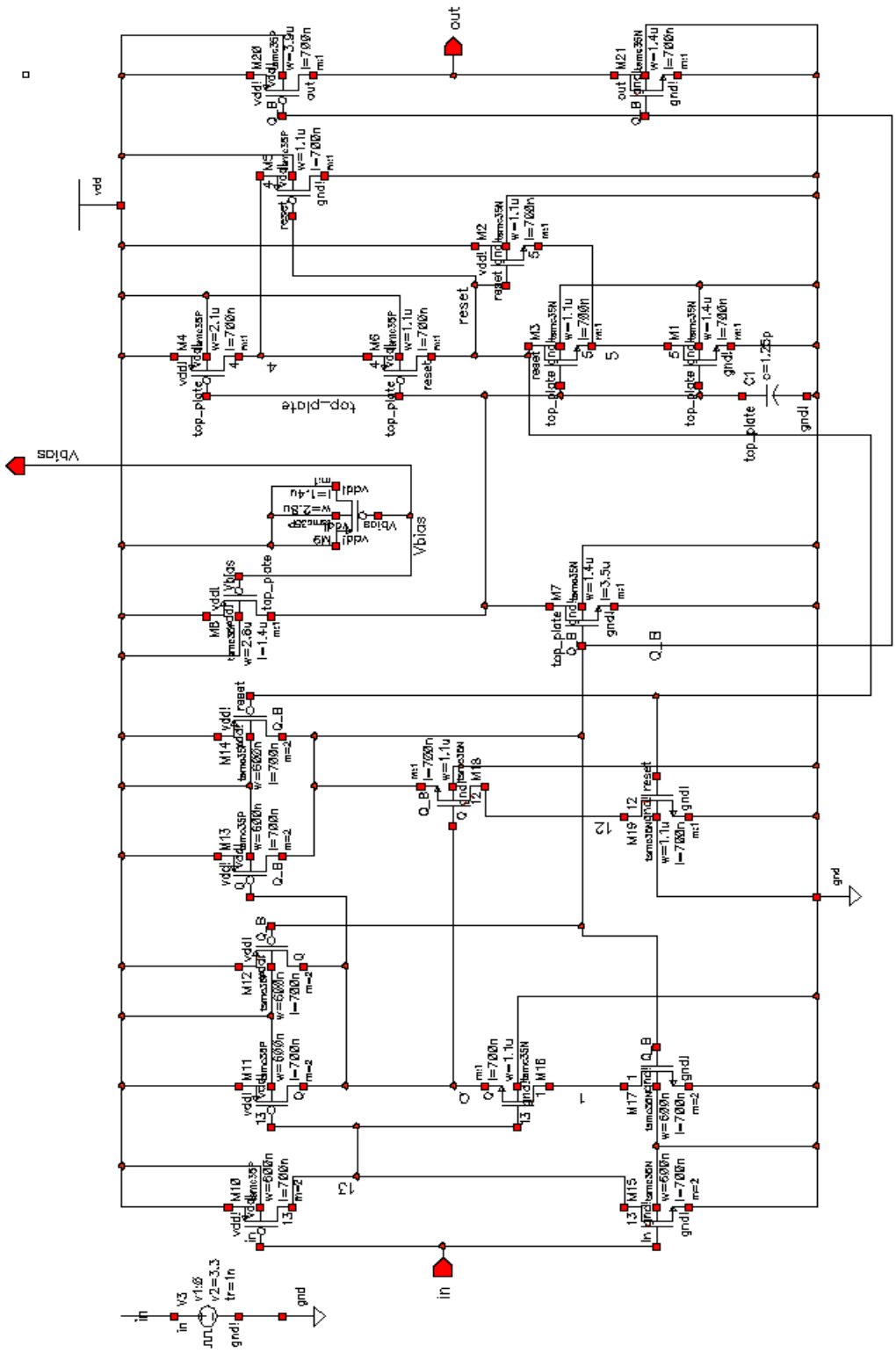


Figure 3.20---One-shot Choice 1 in Previous Chip

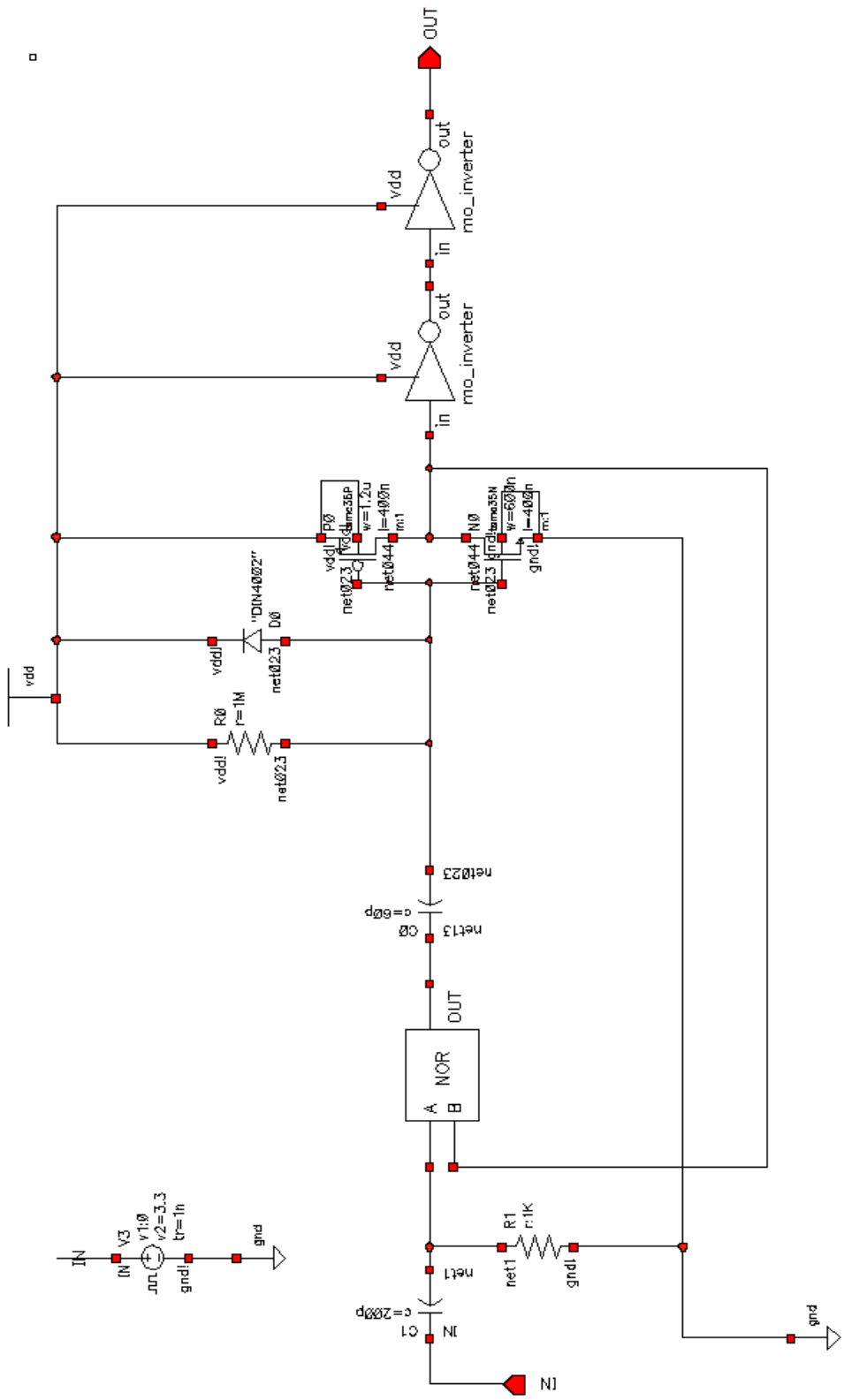


Figure 3.21---One-shot Choice 2 in New Chip

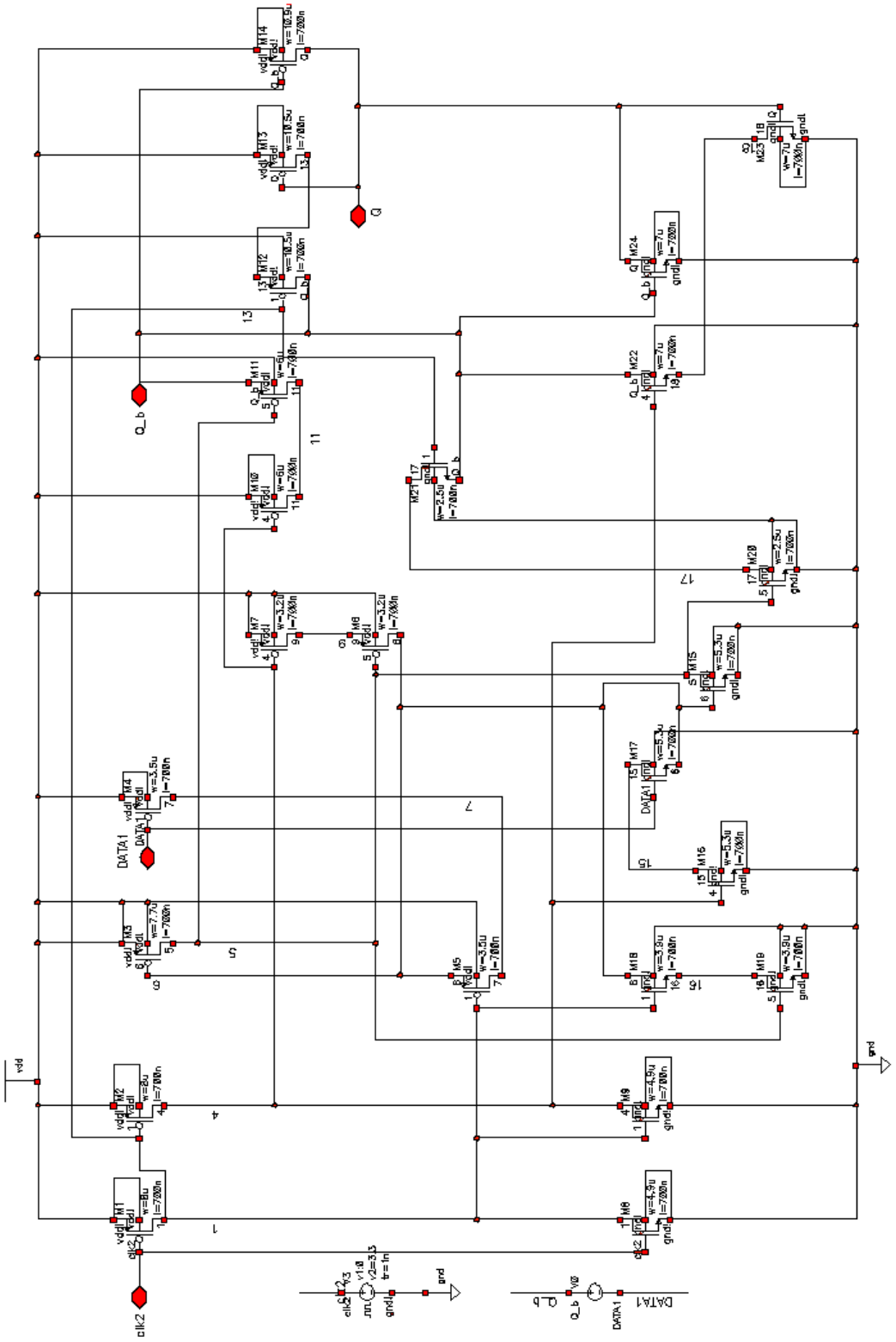


Figure 3.22---D Flip-flop Schematic

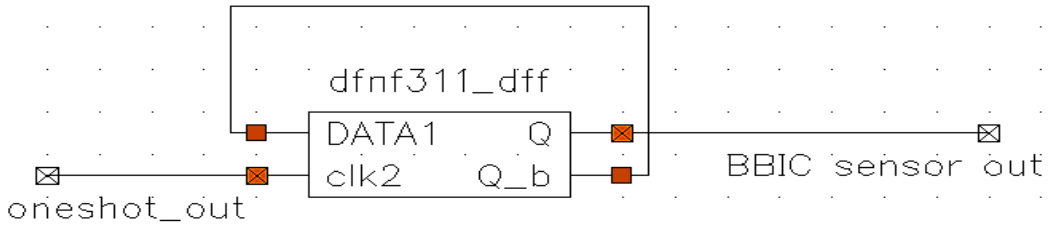


Figure 3.23---D Flip-flop Connection

the frequency of one-shot and a 50% duty cycle. The output of DFF is also the output signal of the microluminometer system whose frequency is proportional to the amount of light incident on the photo detector. And it will be modulated in transmitter.

3.1.4 The Complete BBIC Sensor Layout and Simulation

The layout is shown in figure 3.24. The simulation results are shown in figure 3.25 and 3.26.

3.2 Test Results

The previous BBIC sensor chip consumes 3.3mA current with 3.3V DC voltage source. The new chip consumes 0.115mA current with 3.3V DC voltage source. So the power consumption is reduced to about 3.5% of the previous chip. The testing was made using breadboard. Figure 3.27 shows the experimental setup for the chip. Figure 3.28 and figure 3.29 show testing results using the light of normal lamps in the lab. The integration period out of the one-shot is from 2.5millisecond—50second.

Figure 3.30 shows the testing result of the photodiode, comparing three chips. The light source is a green LED, whose light density is controlled by the

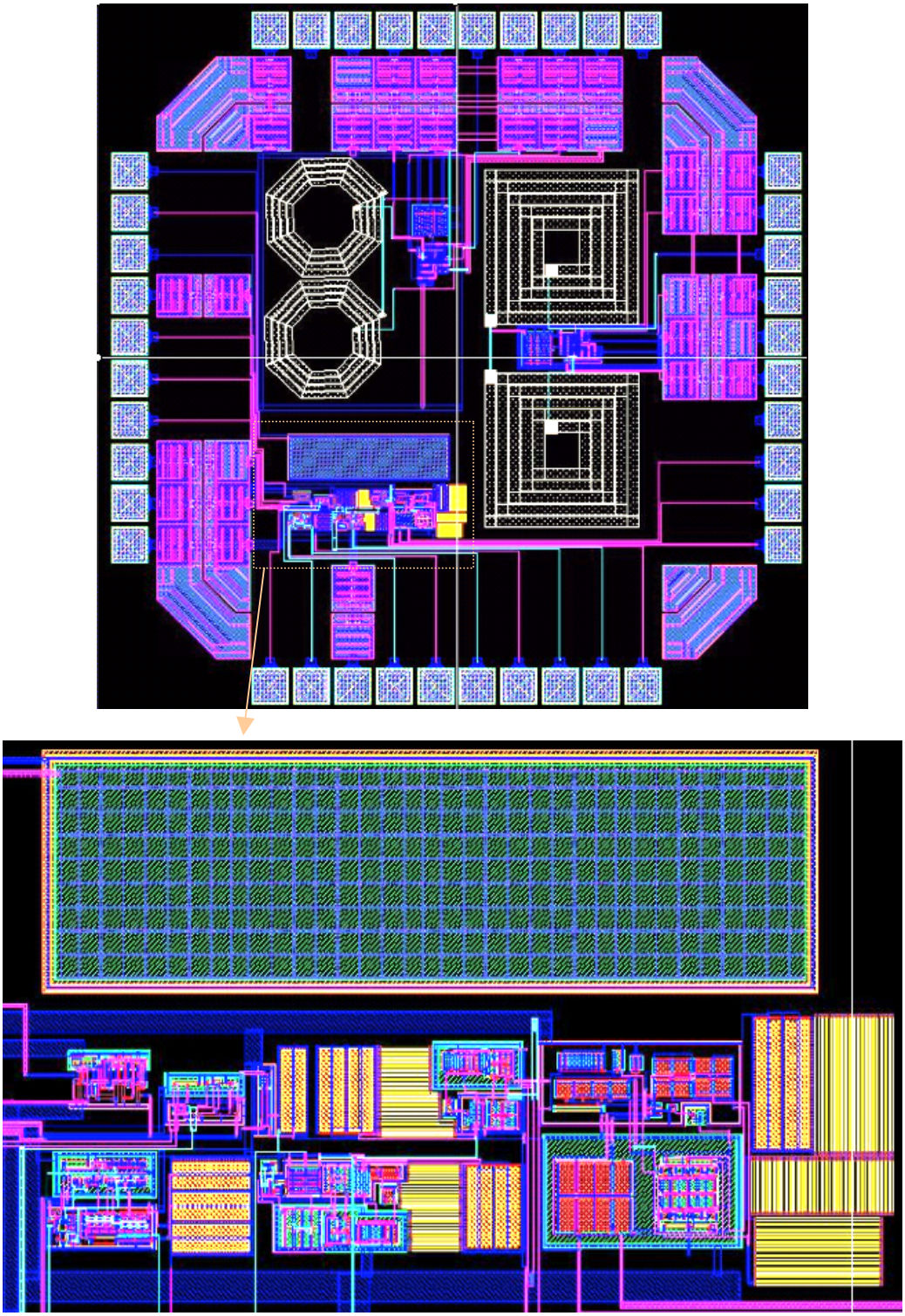


Figure 3.24---Layout of the Complete Sensor Chip

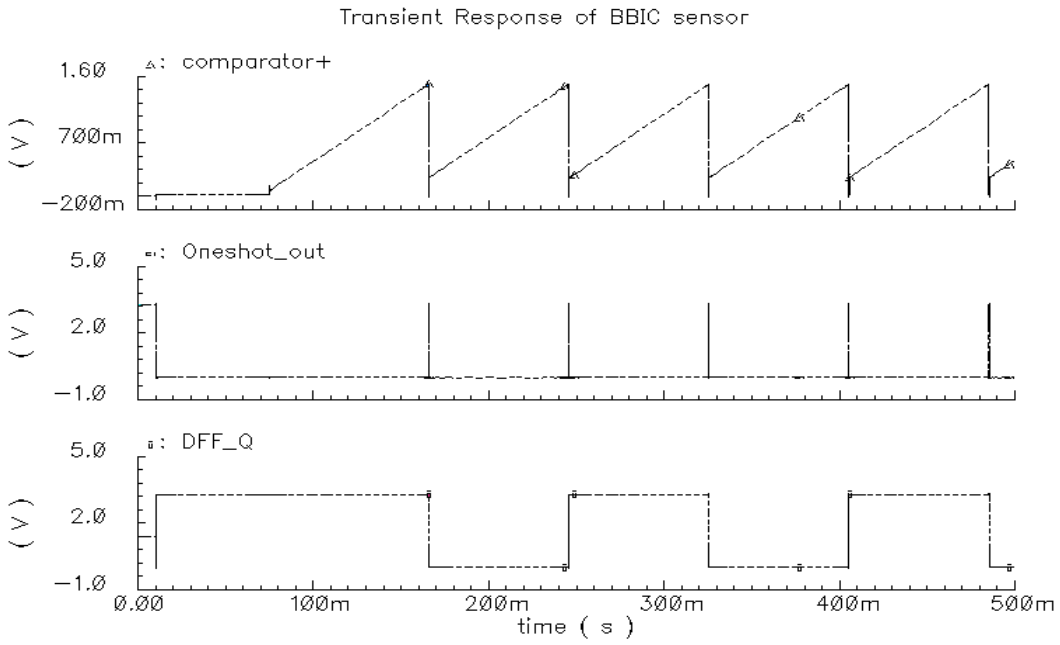


Figure 3.25---Complete BBIC Sensor Simulation (Zoom Out)

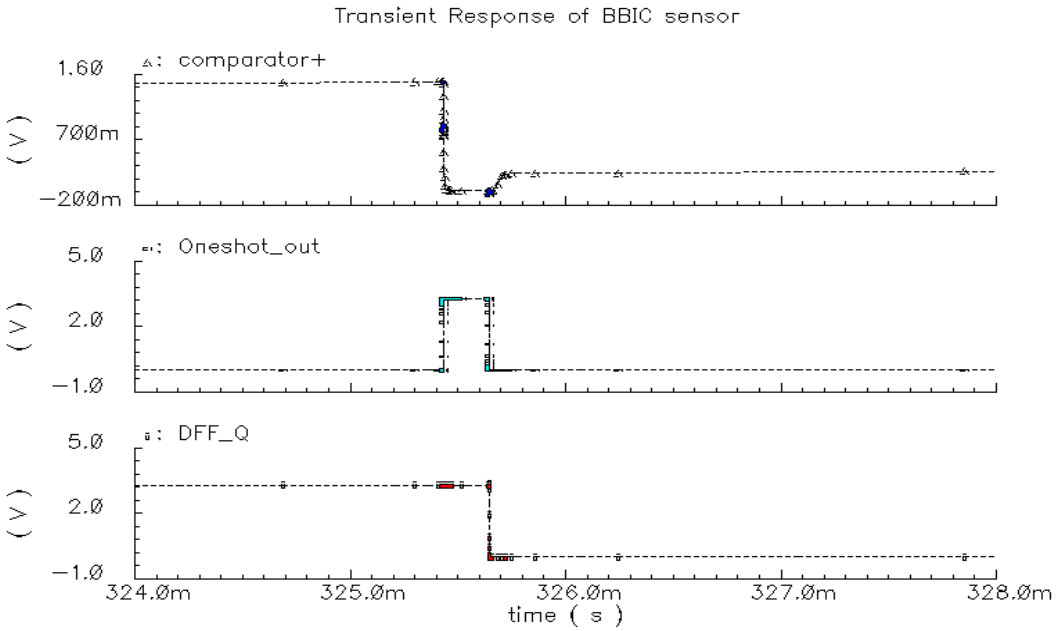


Figure 3.26---Complete BBIC Sensor Simulation (Zoom In)

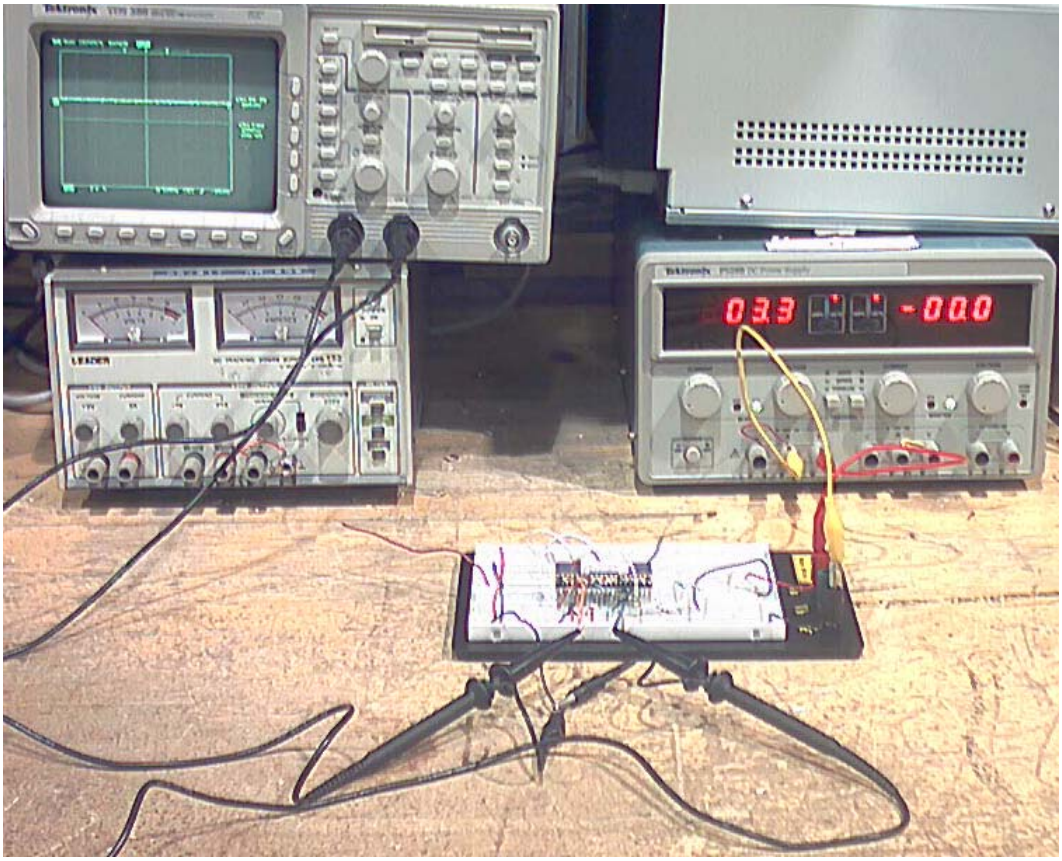


Figure 3.27---Testing Setup for the Sensor Chip

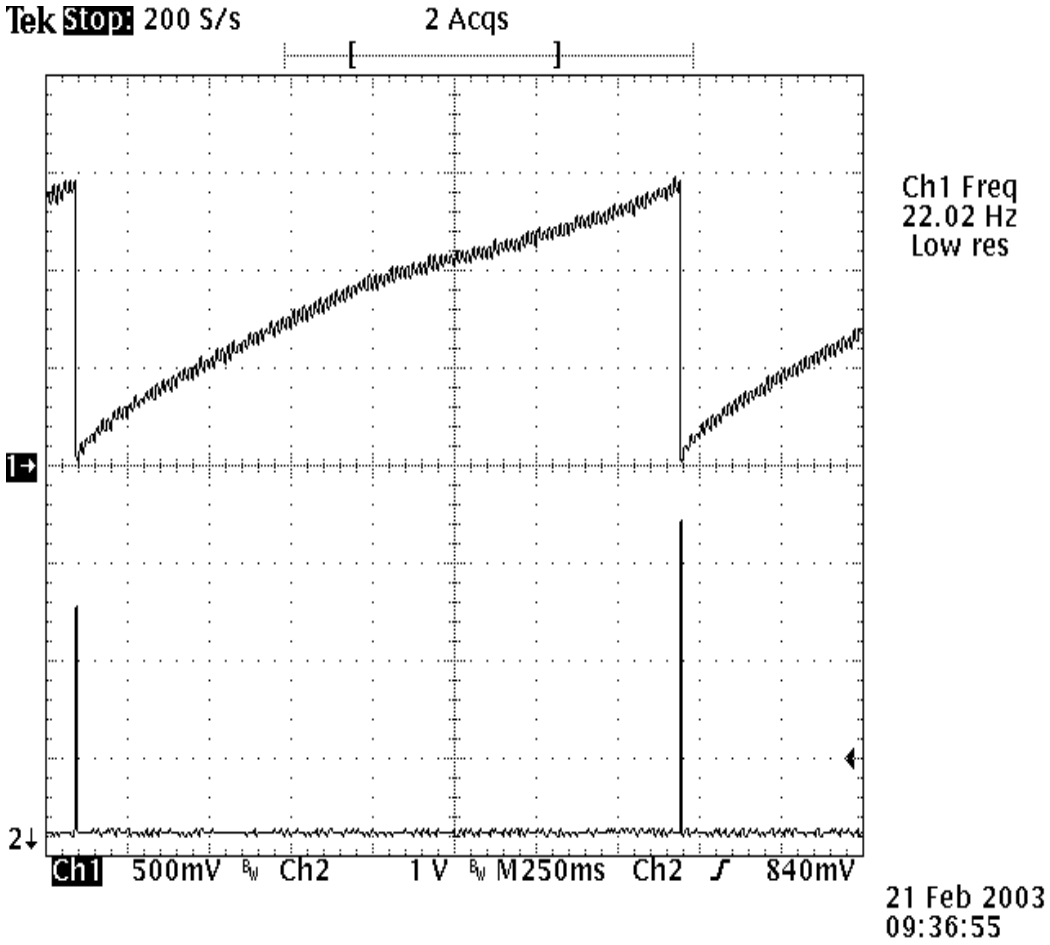


Figure 3.28---A Long Integration Period Testing Result

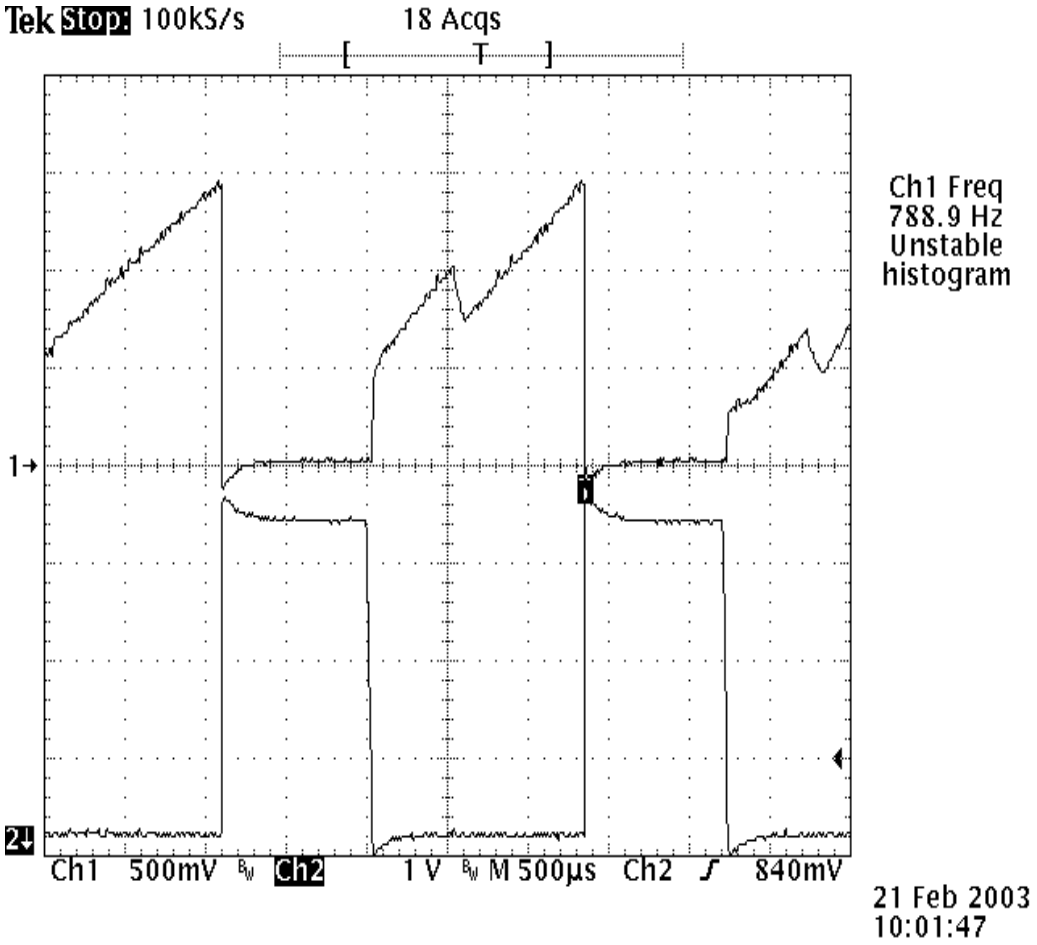


Figure 3.29---Shortest Integration Period Testing Result

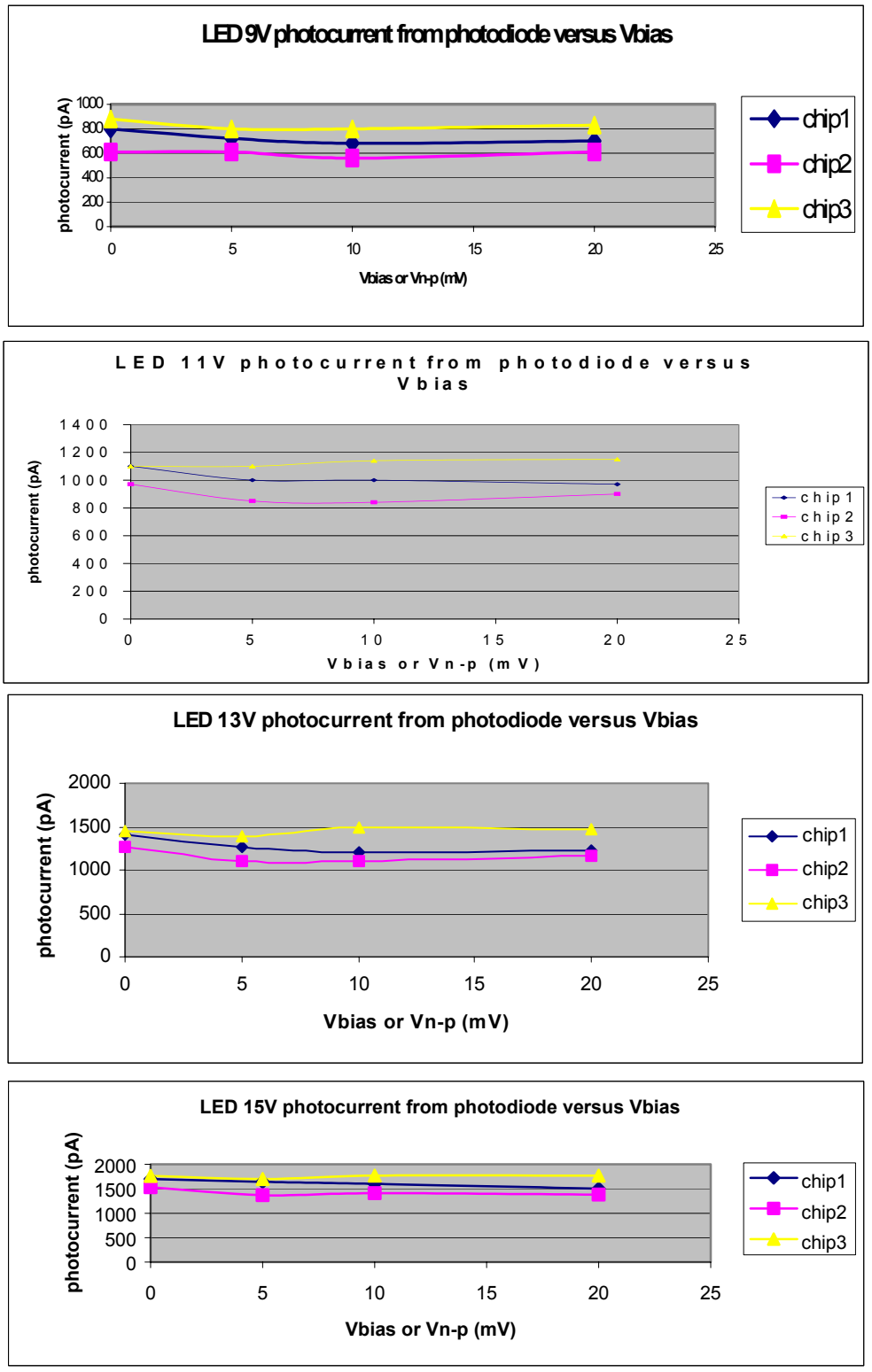


Figure 3.30---Photodiode Testing Results, Using Three New Chips

voltage on it. Figure 3.31 shows photocurrent versus V_{bias} and LED voltage. V_{bias} is the biasing voltage at the non-inverting input of the composite amplifier. LED voltage is the voltage applied to the device LED.

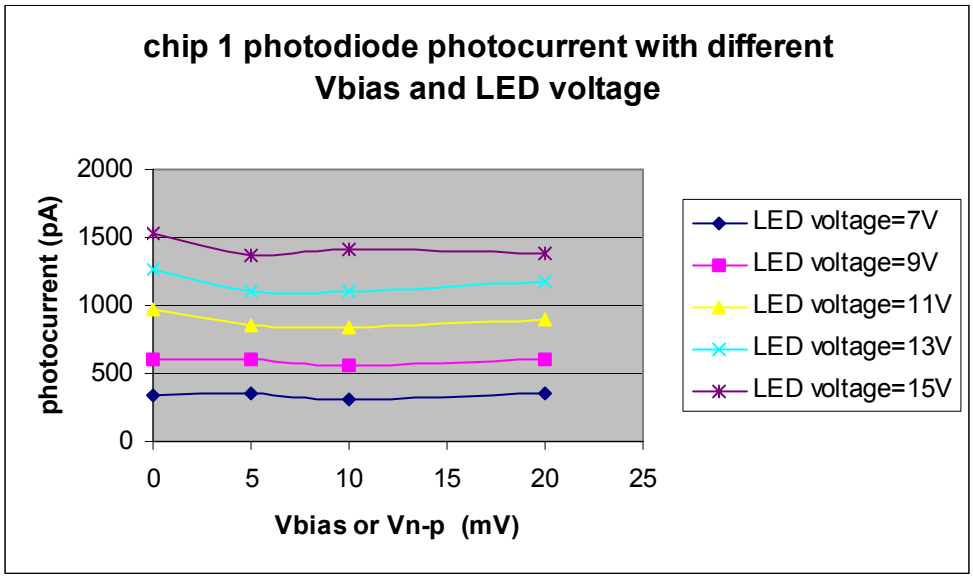


Figure 3.31---Photodiode Testing Results, Using One Chip

CHAPTER 4

Transmitter

4.1 Transmitter System

The structure of the direct conversion transmitter is shown in Figure 4.1. This system is made up of Phase Lock Loop (PLL) [27-32], Gilbert Cell mixer [32], Power Amplifier and Antenna. In the diagram, Data is the signal out of the signal processing circuit. It will be mixed with the 916MHz frequency signal generated by PLL.

PLL includes five blocks: (1) A crystal frequency reference [33]; (2) a phase/ frequency detector [22]; (3) a loop filter [34]; (4) a voltage-controlled oscillator (VCO) [34-39]; (5) a frequency divider [34] (divided by 256) as shown in figure 4.2. Phase/ frequency detector compares the phase/ frequency difference between the frequency reference and the clock signal out of the frequency divider. Then charge pump will produce a control voltage for the VCO according to the phase/ frequency difference. Loop filter will remove the high frequency components of the control voltage and give a relative stable one to adjust the frequency of VCO. The frequency divider will divide the signal frequency out of VCO by 256 to compare with the frequency reference. PLL has a feedback loop, which makes the output frequency of VCO very stable. This stable frequency is important for the RF transmission.

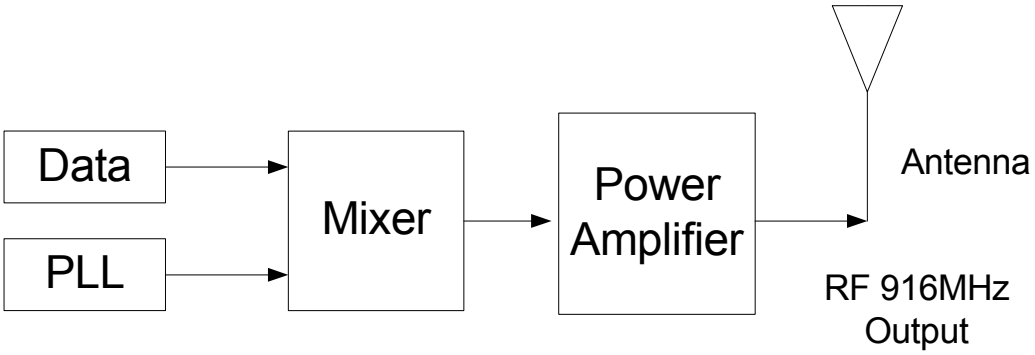


Figure 4.1---Block Diagram for Transmitter System [2]

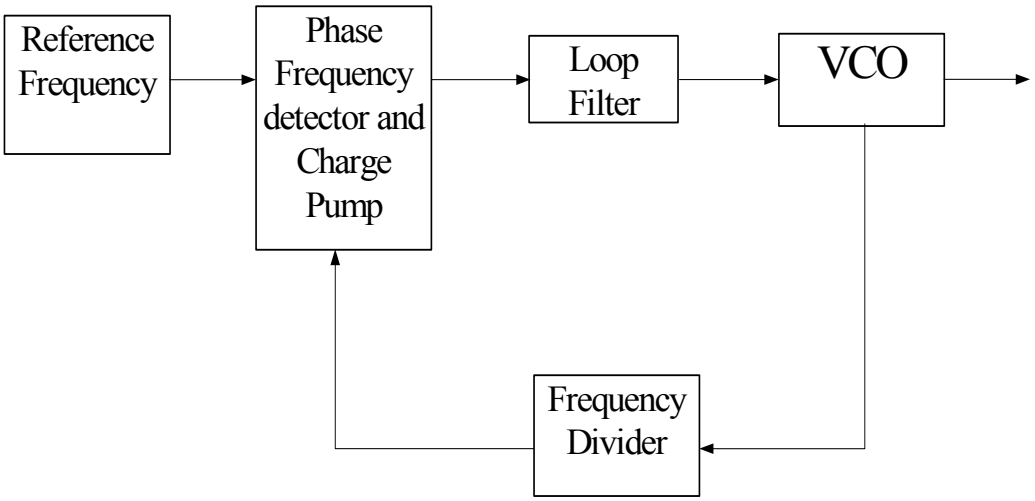


Figure 4.2---Blocks of PLL [2]

4.2 Phase Locked Loop

There are several important specifications to evaluate a PLL [40]. (1) Loop bandwidth is the frequency range, which can be got from the PLL. A small bandwidth is favorable. (2) Lock time is the settling time the phase lock loop after the start point. A short lock time is needed to stable the PLL quickly and to use the transmitter periodically for BBIC system. (3) Phase margin determines the stability of the PLL as a negative feedback system. With a high phase margin, the PLL will have small overshoot and small settling time after a step input is introduced. (4) Phase noise is the randomly fluctuations of the PLL's output frequency [41]. To get a small phase noise, we have to choose a highly precise low phase noise crystal oscillator with an operating frequency of 916MHz/256.

4.2.1 Phase / Frequency Detector with Charge Pump

Figure 4.3 is the diagram for the phase / frequency detector (PFD) and charge pump. Based on the phase/ frequency difference from the two input of PFD, the charge pump injects or absorbs current pulses from the capacitors of the loop filter [34]. The average current out of the charge pump is [31]:

$$i_d = \frac{I_p \cdot \theta_e}{2 \cdot \pi} (Amps) \tag{4.1}$$

I_p is the pump current; θ_e is the phase difference between two inputs of the phase/frequency detector. The loop filter, see figure 4.4, will create the VCO's control voltage V_c [31].

$$V_c = \frac{I_p \cdot \theta_e \cdot Z_F}{2 \cdot \pi} (Volts) \tag{4.2}$$

Z_F is the impedance of the loop filter.

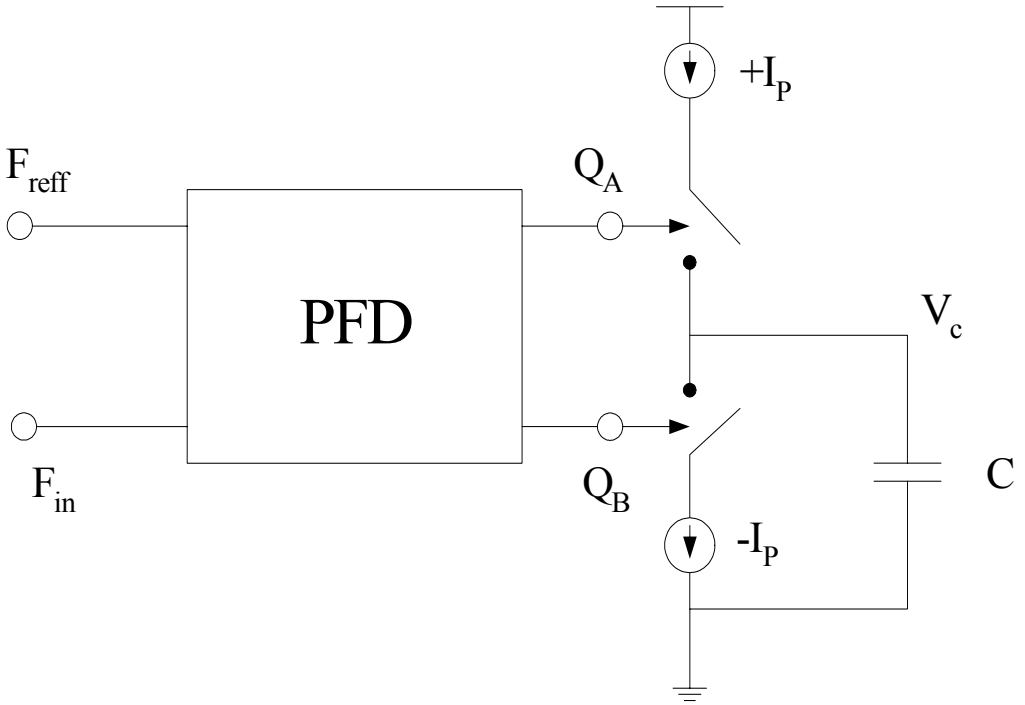


Figure 4.3---Diagram of Phase / Frequency Detector (PFD) and Charge Pump [2]

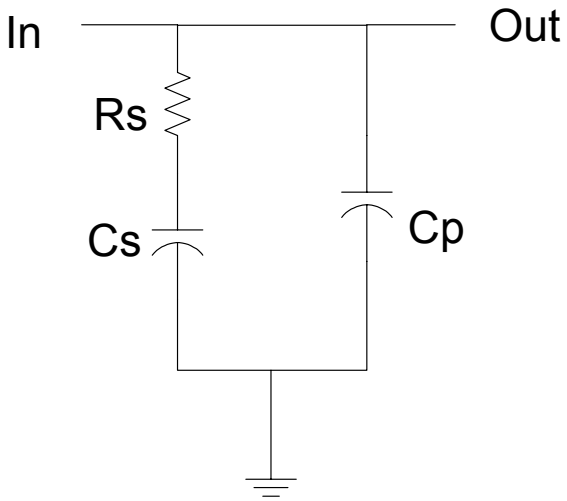


Figure 4.4---Loop Filter [2]

4.2.1.1 Phase / Frequency Detector

The phase frequency detector (PFD) compares the frequency dividers output with the frequency reference, as shown in figure 4.5. PFD measures the time difference between pulses at inputs A and B. The time difference represents the phase or frequency difference between A and B. The phase detection range of PFD is $\pm 2\pi$. The output pulse width of Q_A and Q_B is equal to the phase difference between the two input signals.

PFD has three states. When the frequencies of A and B are the same, if signal A's phase is ahead of B, output Q_A will rise to high with A's rising edge and reset to low with B's rising edge. The pulse width of Q_A is proportional to the phase difference between A and B. During the time that Q_A is high, the loop filter is injected current to increase the VCO's control voltage, and then change the frequency of VCO. This loop feedback will try to keep A and B with the same phase. IF the phase of B is ahead of A, the loop filter will be discharged and the VCO control voltage will decrease. When the frequencies of A and B are different, the output pulse will adjust the voltage of the loop filter, or VCO's control voltage, to change the frequency at VCO output. After some time the feedback loop will keep the frequencies of A and B to be the same. The two inverters following the output of the AND eliminate a phenomenon called dead zone. When the phase difference between A and B is small, the output pulses at Q_A or Q_B will be very short. Then the VCO control voltage can only be changed very slowly. With these two invertors, there will be more delay after both Q_A and Q_B arrives high. So the minimum output pulse width is increased.

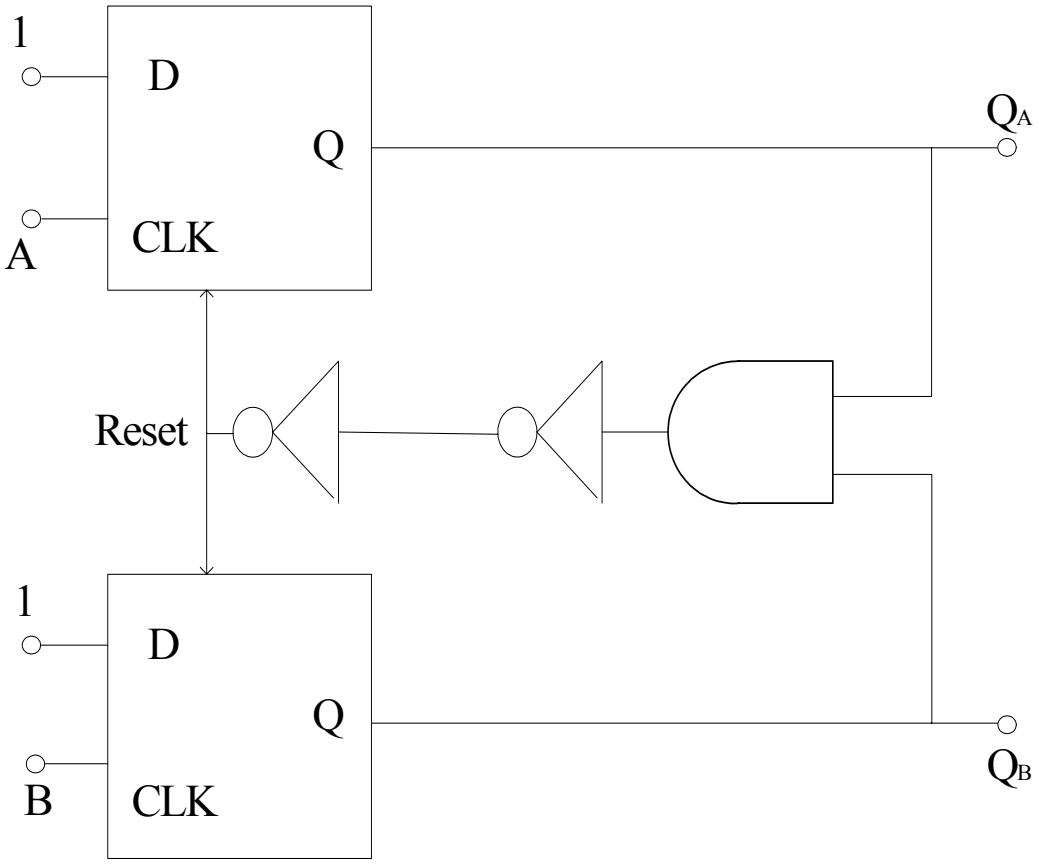


Figure 4.5---Diagram of Phase Frequency Divider [2]

4.2.1.2 Charge Pump Current Source and Switches

With the output pulses of Q_A and Q_B, the capacitor C is charged or discharged and increases or decreases the control voltage for the VCO. When Q_A is high, the capacitor C is charged and the control voltage increases. When Q_B is high, the capacitor C is discharged and the control voltage decreases.

A current source, shown in figure 4.6, will generate the constant complementary current over a wide range of output voltages. Ip+ and Ip- of figure 4.3 are represented by node 60 and 50 in figure 4.6. The current source will provide complementary current of 10μA over an output voltage swing from 0.1—3.2 volts. So the current source is very precise to give a proportional change of the control voltage according to the phase/ frequency difference of PFD's two inputs.

The switching circuit in the charge pump, as shown in figure 4.7, will turn on the switch between the loop filter and Ip+ or the switch between the loop filter and Ip-. So the charge in the loop filter will be accumulated or removed. And the resistance of the switches is very small, with large channel width and small channel length.

4.2.2 Voltage-Controlled Oscillator

The VCO has a tunable frequency range of 100 MHz and an operating frequency of 916 MHz close to the center of the tunable range. The control voltage can change from 0.1V to 3.2V. The gain of VCO or the frequency component is [27]:

$$K_v = \frac{\Delta\omega}{\Delta V_c}\left(\frac{rad/\sec}{volt}\right) = \frac{2\cdot\pi\cdot 100\cdot 10^6}{3.1}\left(\frac{rad/\sec}{volt}\right) = 202.58\times 10^6\left(\frac{rad/\sec}{volt}\right) \qquad (4.3)$$

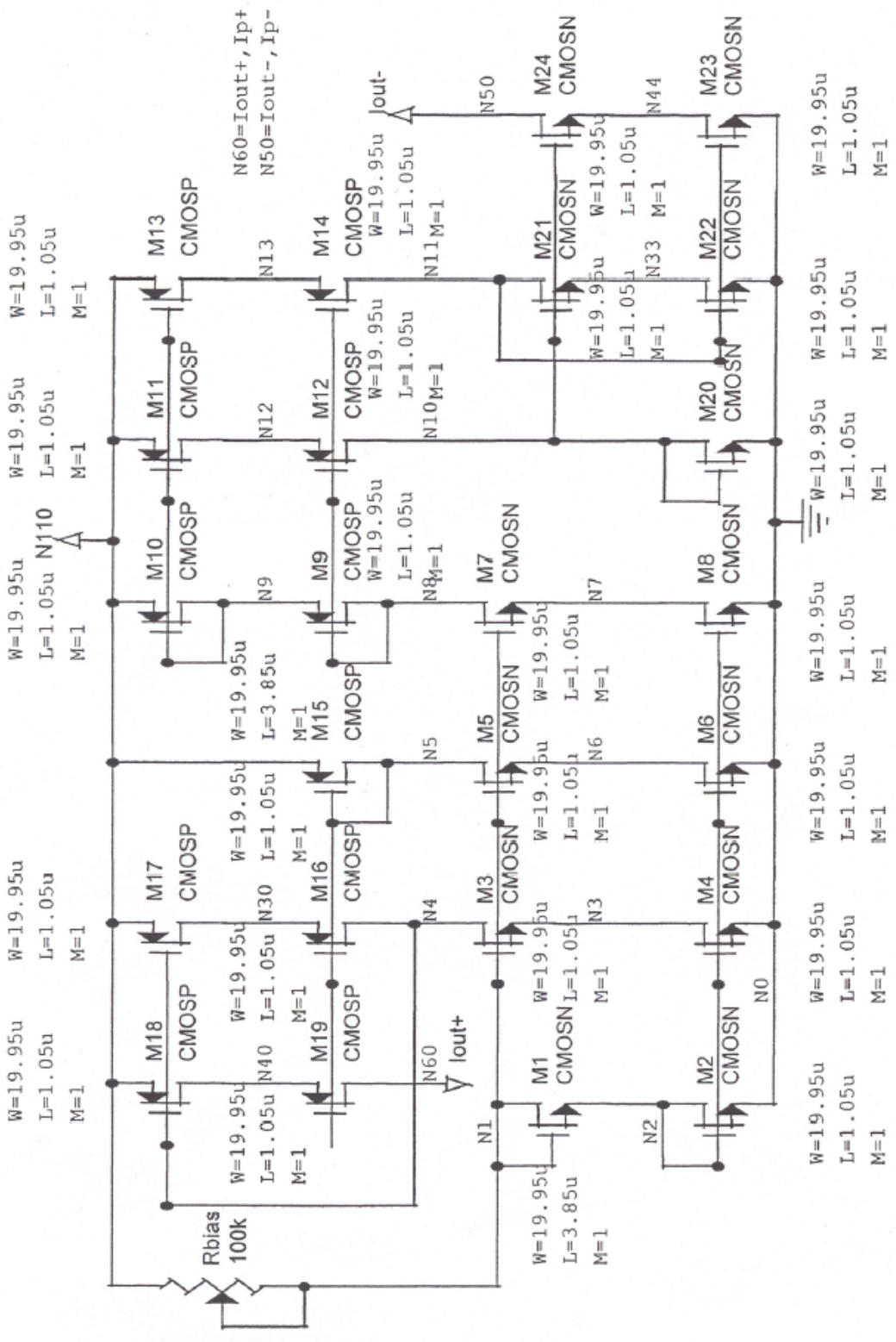


Figure 4.6---Complementary Current Source [2]

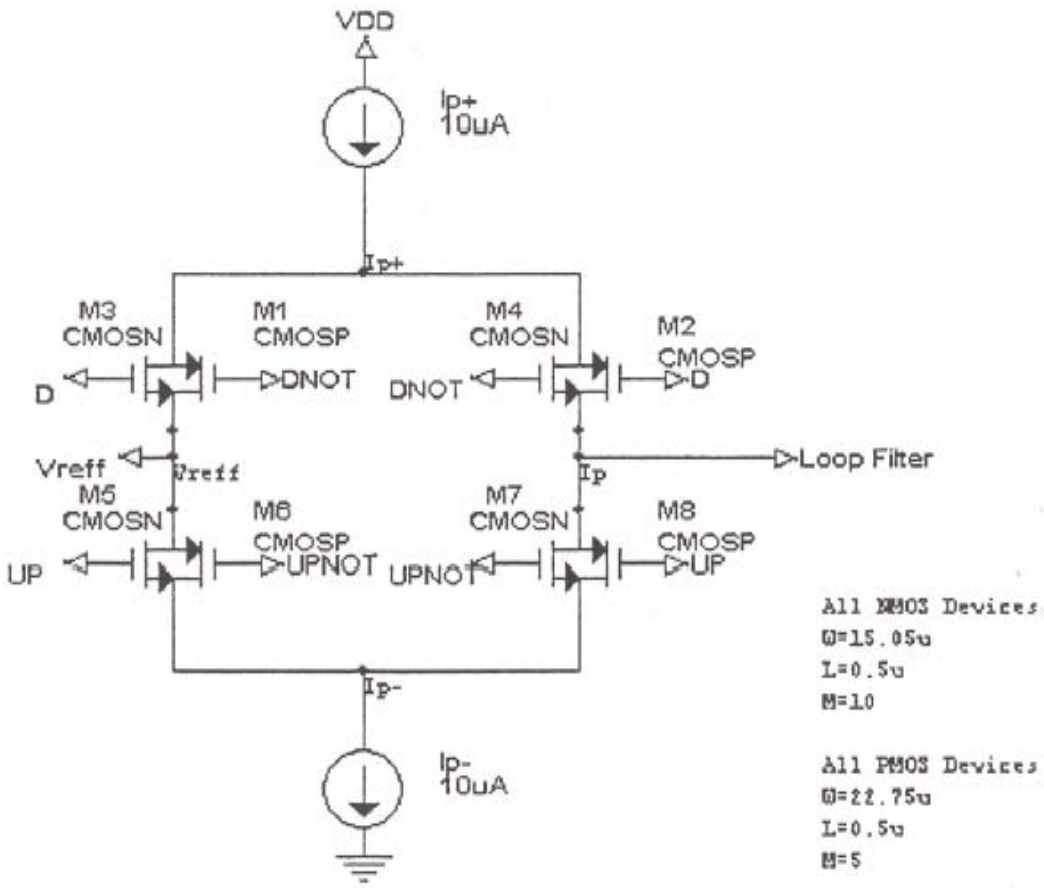


Figure 4.7---Switch Circuit Diagram [2]

Where ΔV_c is the change of VCO control voltage, $\Delta\omega$ is the change of frequency, caused by the tuning of V_c. The VCO needs a small tuning range to improve the loop stability and reduces the VCO phase noise.

The VCO includes a cross-coupled NMOS pair M1, M2 and current mirror M4. See figure 4.8. The circuit has off chip inductors and diodes. The inductor and the varactor diode capacitance control the operating frequency and tuning range of the oscillator along with stray capacitance connected in parallel with the tank circuit. The largest contributor to the stray capacitance is the chip's parasitic capacitance, which is approximately 1.5pF. Another large contributor to the tank's parasitic capacitance is the capacitance of M1 and M2, which is 0.5pF for each of them. The required capacitance value with a 4.9nH inductor is 6.16pF to be operated at 916MHz. These low parasitic contributions to the tank's capacitance allow adjusting the tuning range of the oscillator.

LC tank is an important part of VCO circuit. And a high quality factor is desired. The quality factor is the unloaded Q when the tank circuit is connected in parallel with an ideal current source.

$$Q = \frac{2 \cdot \pi \cdot Energy\ Stored\ \ per\ Period}{Energy\ Dissipated\ \ per\ Period} \tag{4.4}$$

Q is the quality factor of the tank circuit. Z is the impedance of the LC tank circuit. An ideal Q is infinite, which means no energy is lost. Real LC tank circuit has losses due to parasitic series resistances of the inductor and the capacitor [29].

$$Q = R_p \cdot \sqrt{\frac{C}{L}} \tag{4.5}$$

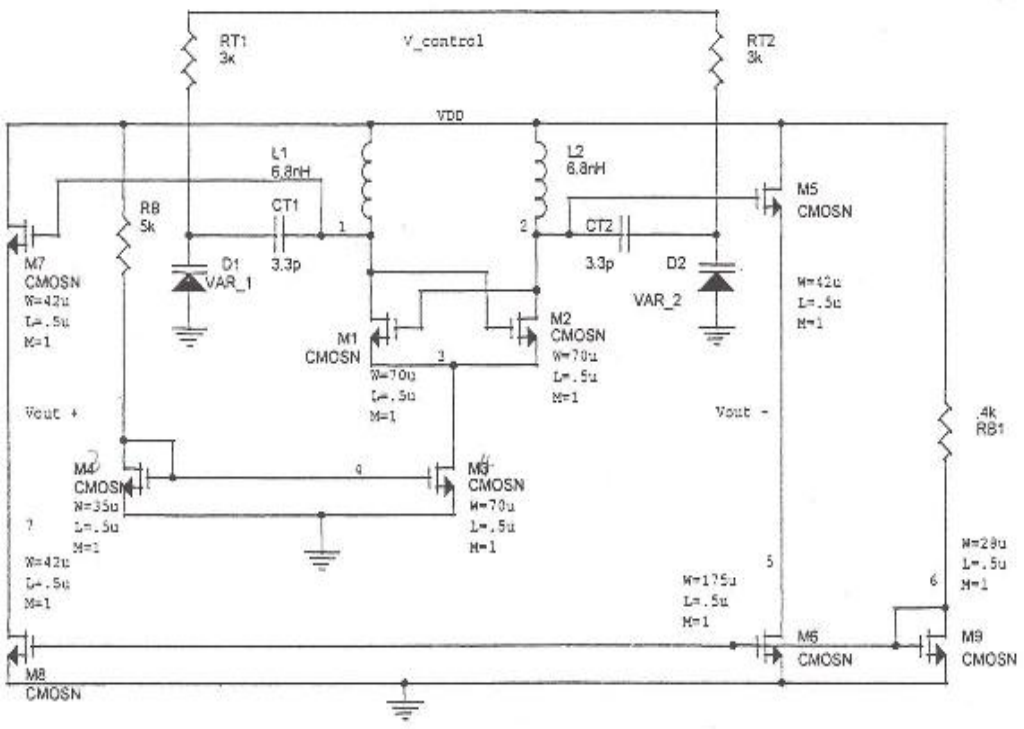


Figure 4.8---Voltage Controlled Oscillator with Output Buffer (Previous) [2]

$$R_p = \frac{L^2}{C \cdot L \cdot R_{SC} + R_{SL} / \omega_0^{\,2}} \tag{4.6}$$

Where R_p is the equivalent parallel tank resistance, and C and L are the varactor capacitance and surface mount inductance. And R_{SL} is the series parasitic resistance of the inductor, and R_{SC} is the series resistance of the capacitor. And ω_0 is the resonant frequency of the tank circuit.

The operating frequency of the oscillator is

$$\omega_0 = \frac{1}{\sqrt{L \cdot (C + C_{gs} + 2 \cdot C_{gd})}} \tag{4.7}$$

Where C_{gs} is the gate to source capacitance of a single NMOS transistor in the cross-coupled pair M1 or M2. C_{gd} is the gate to drain capacitance of M1 or M2. So with larger C_{gs} or C_{gd}, the lower operating frequency is obtained.

A cross-coupled pair connected directly to ground has a maximum peak-to-peak voltage of V_{DD} in the differential output. The maximum peak-to-peak voltage can be increased to $2V_{DD}$ by adding a current source M4 to the cross-coupled pair [30]. The current mirror M4 allows for the bias current to be completely switched between the devices in the cross-coupled pair. Compared to a cross-coupled pair connected directly to ground, this switching doubles the bias current in the cross-coupled devices and increases the voltage drop across R_p by two. When either of the cross-coupled devices is operating in the saturation region, the maximum value of the differential output voltage is valid. The transistor acts as a resistor connected in parallel with the tank circuit, if the output voltage drives one of the cross-coupled devices into the linear region. This resistor decreases the equivalent parallel resistance of the tank, reduces the tank's quality factor and stops the oscillation. This causes voltage limiting.

A varactor diode is used to vary capacitance in the LC tank circuit [42]. The applied reverse bias voltage across the diode changes the capacitance of the diode by as given by,

$$C = \frac{C_{jo}}{(1+\frac{V_{br}}{V_{bi}})^{M}} \tag{4.8}$$

Where C_{jo} is the diode's depletion capacitance at zero bias, V_{br} is the reverse bias voltage, V_{bi} is the *pn* junction barrier voltage, and M is related to the doping grading coefficient. The capacitance of varacotor diode versus voltage curve is shown in Figure 4.9. The capacitance decreases until the applied reverse voltage reduces to five volts. The adjustable range of the capacitance is corresponding to the reverse bias voltage range of 0-5V. So the varactor diode is suitable for the BBIC transmitter with a 3.3V power supply.

In figure 4.8, the resistors RT1 and RT2 are used to isolate the VCO control voltage from the tank circuit. They are added in parallel with the LC tank circuit. If the resistors are much larger than the parallel resistance of the tank circuit, the isolation resistors will not significantly affect the quality factor of the tank circuit.

Without the spice model for the varactor diode, a capacitor in series with a diode was used instead of the varactor diode as shown in figure 4.10. VCO simulation is shown in figure 4.11 and figure 4.12. The frequency range is 905M-926MHz.

4.2.3 Frequency Divider

The division factor of the frequency divider is: N=256. N is also the PLL closed-loop frequency gain. Because N is quite large, a relatively low operating frequency, approximately 3.578MHz, can be used for the highly precise crystal and phase frequency detector.

The divide-by-256 frequency divider is made up of eight-stage digital dividers. The first three stages are current mode logic (CML) D flip-flops as shown in figure 4.13. Each of the CML DFF will divide the frequency by two. So

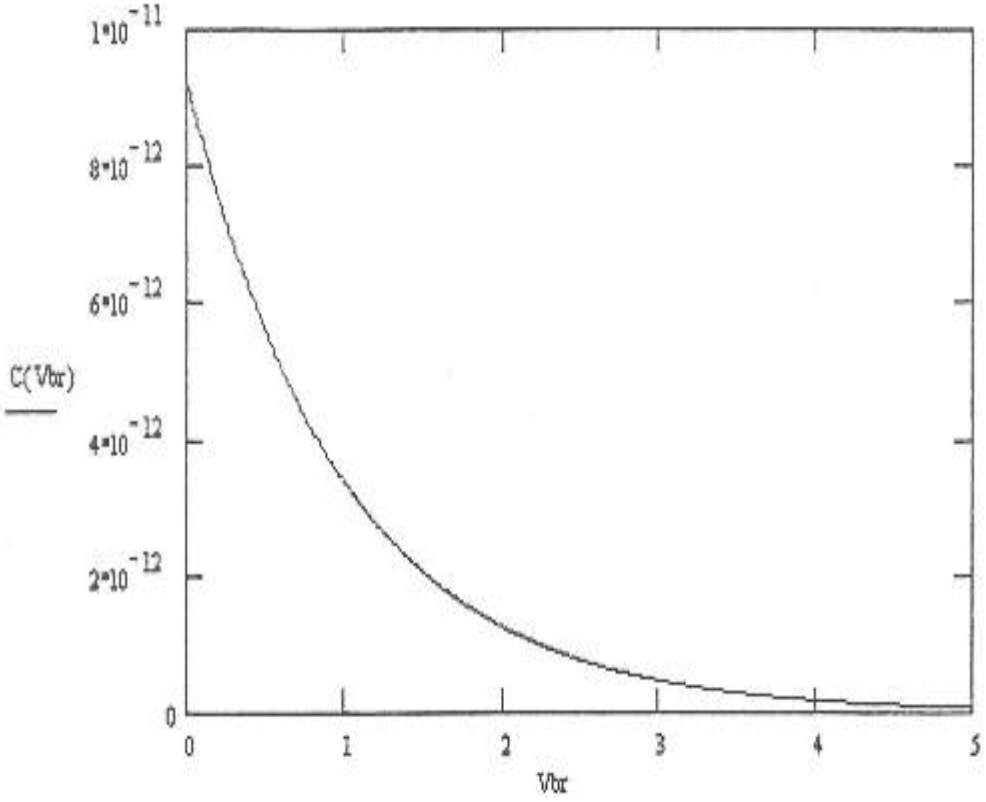


Figure 4.9---Capacitance of Varactor Diode versus Reverse Bias Voltage [2]

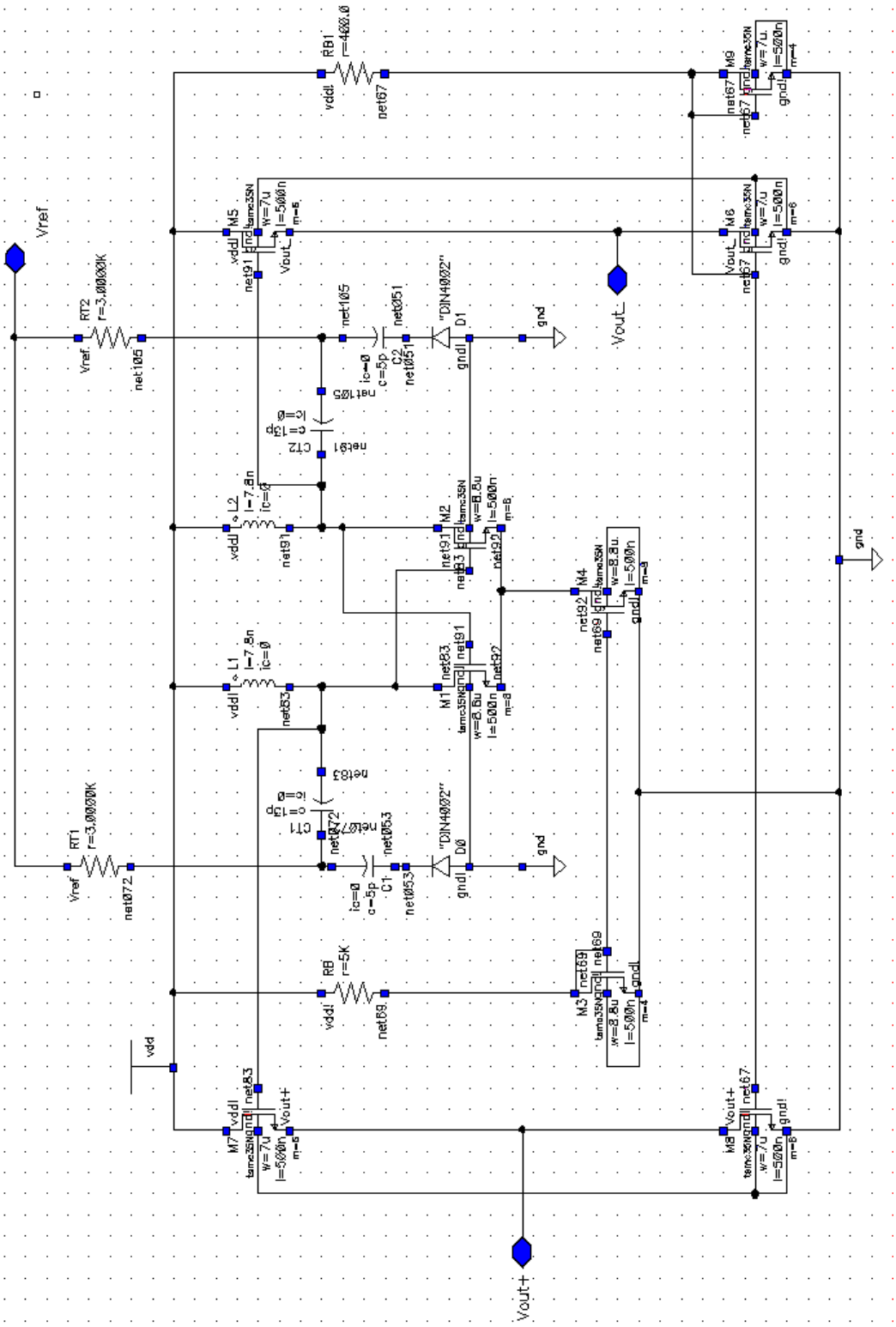


Figure 4.10---Voltage Controlled Oscillator With Output Buffer (Rebuilt)

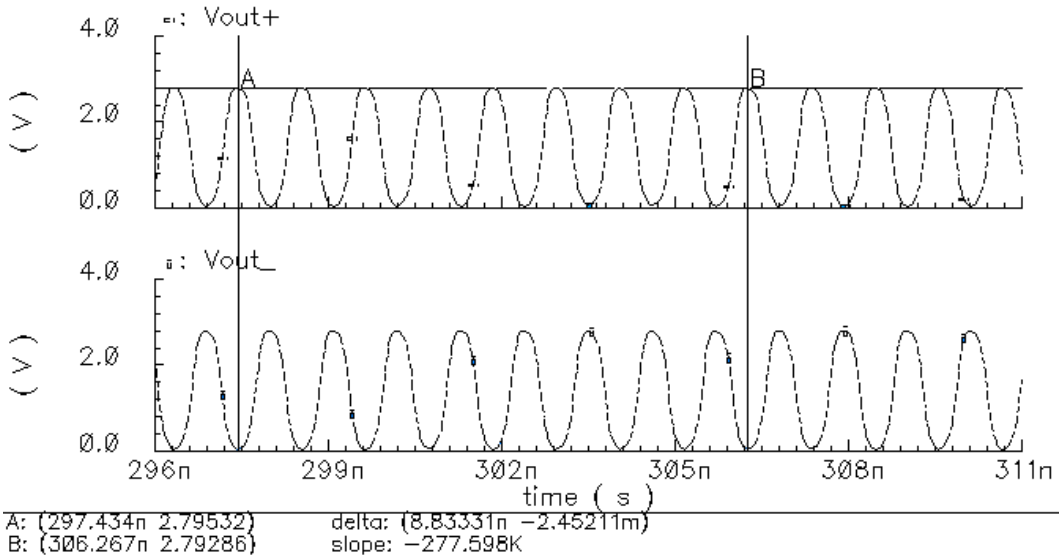


Figure 4.11---VCO Lowest Frequency (905MHz) Simulation

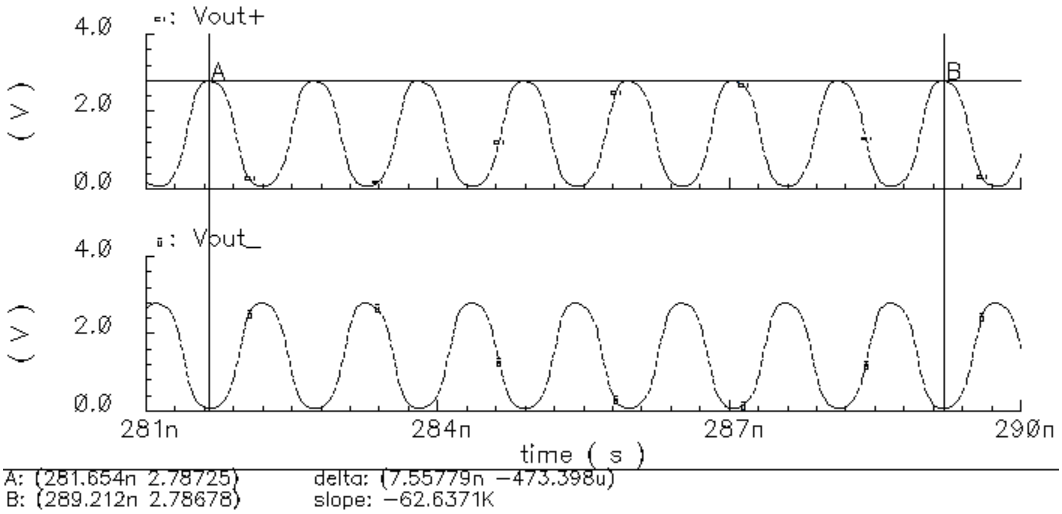


Figure 4.12---VCO Highest Frequency (926MHz) Simulation

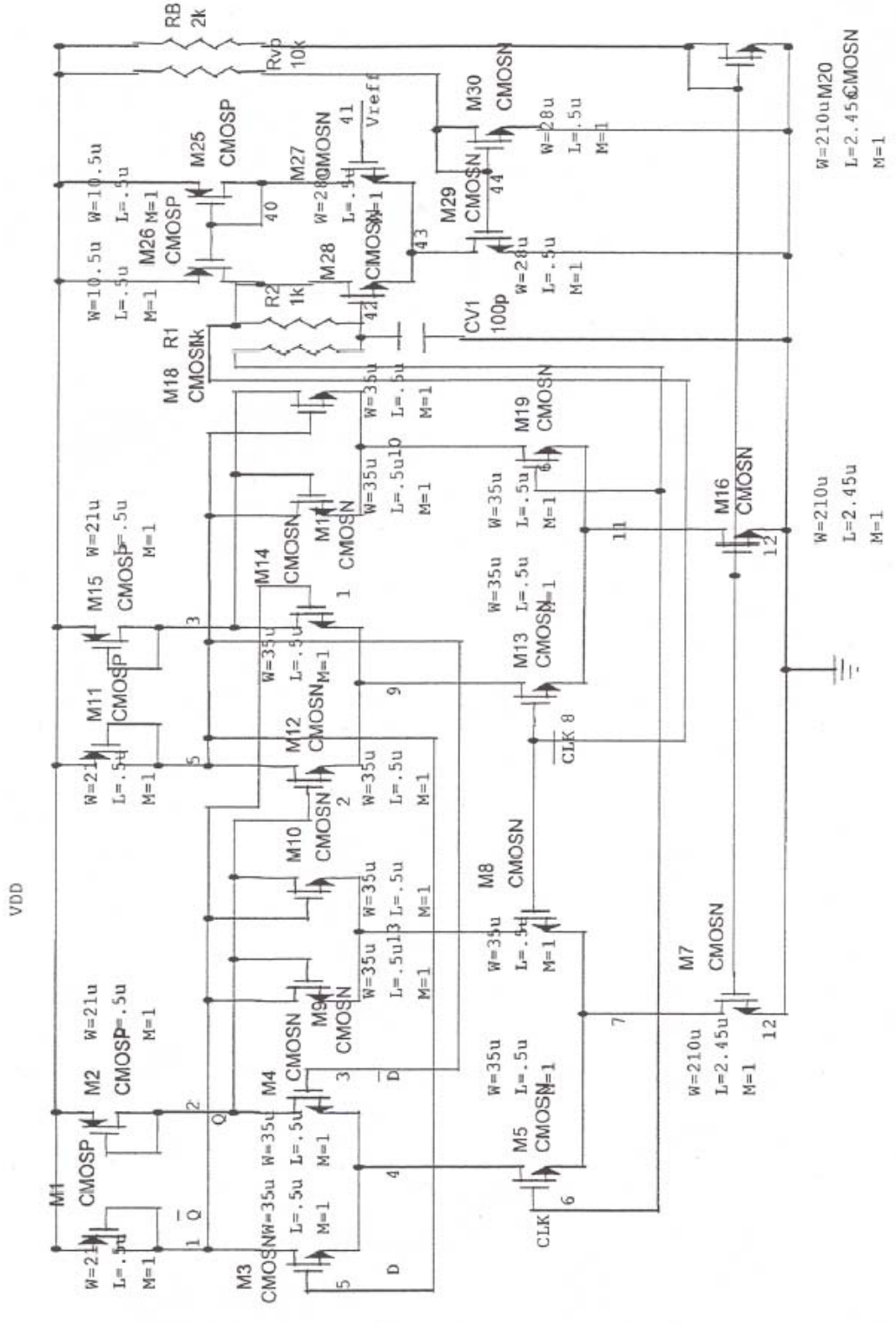


Figure 4.13---CML D Flip-flop Diagram [2]

these three stages will divide the frequency by eight totally. The remaining five divide- by-2 stages are standard cell D flip-flops. For each of these five D flip-flops, Q-, or the inverted output, is connected back to the DFF input D. So each DFF will divide the frequency by two. The total division factor of the frequency divider will be 2^8, or 256. The VCO output is the whole frequency divider's input, or the first CML DFF input.

The first three CML D flip-flops include a differential pair and a regenerative pair. These CML D flip-flops can operate at high frequency, 916MHz. But the clock and "not" clock inputs must be precisely complementary. The first stage CML D flip-flop can respond to a minimum input signal of -15dBm, or 112mVpp, with an input frequency of 1GHz. The second and third stage CML D flip-flops have the same structure as the first one, except for the bias current. The second stage has a bias current, which is 75% of the first stage. The third stage has 50% bias current of the first stage. In this way, the total power consumption can be reduced.

The successive eight stages of the divide-by-256 frequency divider are standard cell DFFs, which have not reset inputs [34]. The maximum allowable operating frequency of these DFFs is approximately 500MHz for the HP 0.5μm process. So they can perform well with the frequency of 125MHz in the PLL.

4.3 Mixer

The doubly balanced Gilbert Cell multiplier [43] is used as the mixer as shown in Figure 4.14. Transistors M7 and M8 are the RF input differential pair. They are connected to the VCO output differential pair. VCO output buffer has to

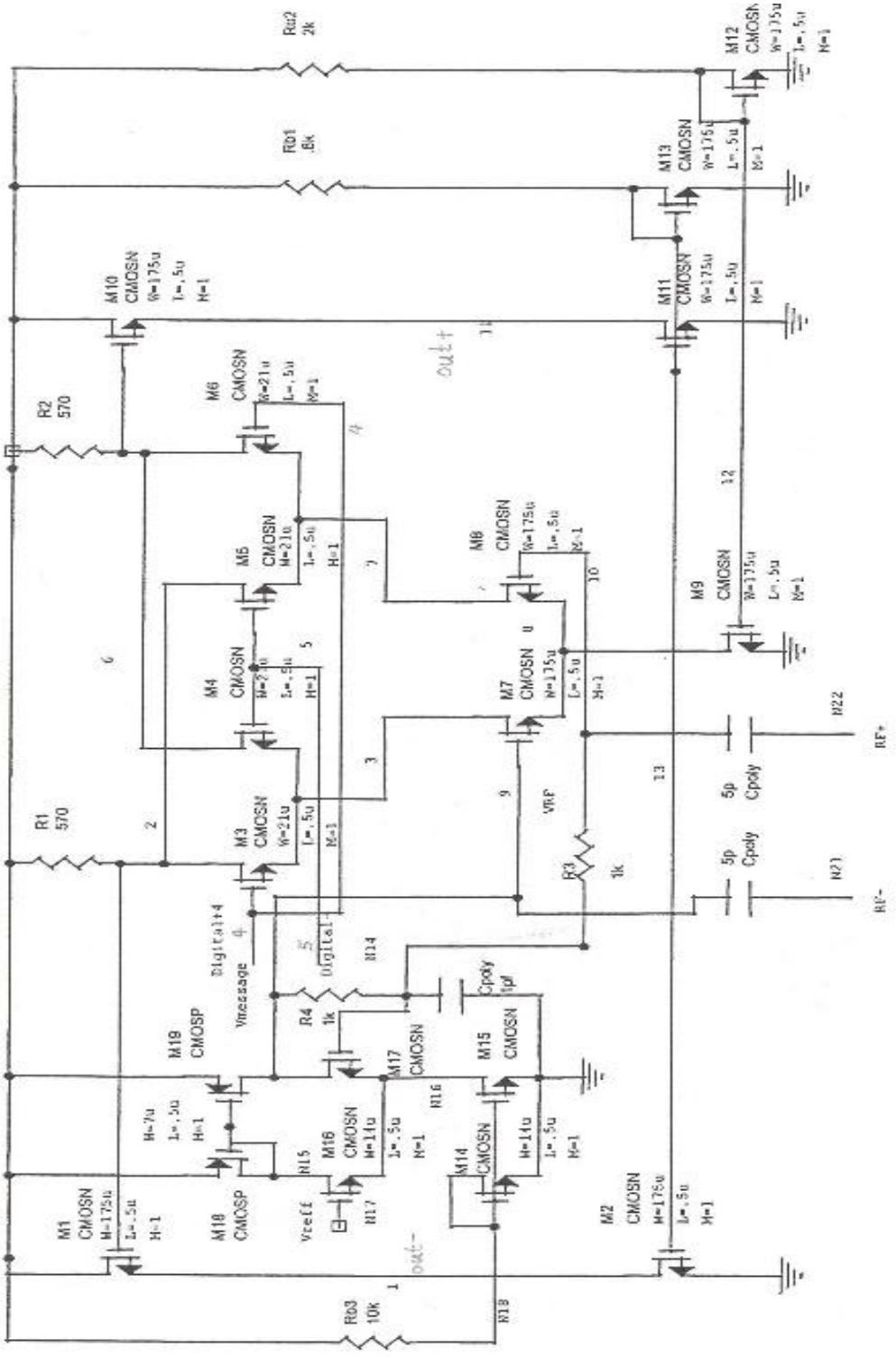


Figure 4.14---Original Double Balanced Gilbert Cell Multiplier [2]

drive the large capacitance of the mixer input devices. And the input devices M7 and M8 will decrease the input RF signal by a factor of 1dB. To reduce offset associated with the differential pairs in the mixer, transistors M7, M8, M3, M4 and M5, M6 should be laid out using a common-centric geometry.

1.5V bias voltage created by the bias circuit is applied to the gates of RF input differential pair transistors M7 and M8. The bias circuit is made up of R4, M19, M17, M15, M14, M16, and Rb3. The voltage at the gate of M17 mirror the off chip DC voltage V_{reff}, which is 1.5 V. The bias current for the bias circuit is about 10μA. It will not significantly increase the mixer power dissipation.

4.4 Power Amplifier

Power amplifier amplifies the small input RF power to a large output RF power. The power delivered to a load is the product of the voltage and current across the load. And power gain (G) is ratio of the average RF output power to the average RF input power.

$$G = \frac{P_{out,RF}}{P_{in,RF}} \tag{4.9}$$

An important characteristic of a power amplifier is the ratio of DC supply power to RF output power. It is also called DC-to-RF power conversion efficiency, or drain efficiency.

$$DE = \eta = \frac{P_{out,RF}}{P_{in,DC}} \tag{4.10}$$

The upper limit of the input value of a power amplifier is 1-dB gain compression point. This point is the point where the actual gain is 1-dB below the ideal linear gain [43].

Harmonic distortion causes non-linearity on the output signal. Total harmonic distortion (THD) is a common method to evaluate non-linearity. If input to the amplifier is a single tone, a cosine wave signal cos ($\omega_0 t$), then the output will be:

$$\text{Vout} = a_0 + a_1\cos(\omega_0 t) + a_2\cos(\omega_0 t)^2 + a_3\cos(\omega_0 t)^3 + \ldots \quad (4.11)$$

Cos $(\omega_0 t)^n$ terms will create harmonic of a frequency $n\omega_0$. And

$$THD = \frac{\sum P_{Harmonics}}{P_{Fundamental}} \quad (4.12)$$

Where $P_{Harmonics}$ is the total harmonic signal power and $P_{Fundamental}$ is the total fundamental signal power. In a power amplifier, the largest harmonic is generally the second one with $2f_0$ frequency.

This power amplifier is a Class-A amplifier. So during the full 360 degrees of the input cycle, the input signal will be amplified. The output signal also has the full 360 degrees phase like the input signal.

Figure 4.15 is the schematic of the power amplifier. N0 and N1 provide two stage amplifications. Their gate voltage is biased to be about 1V. L2 and C2 will present very high impedance to any second harmonic currents. So they will reduce second harmonic distortion in the output signal.

4.5 Simulation of Transmitter System

simulation, a square wave voltage source is used instead of the whole BBIC sensor circuit. And it is connected to the “Local-” input of the mixer. And a much higher frequency, 10MHz is used instead of the real BBIC sensor output frequency, which is lower than 1kHz. “Local+” input of mixer is connected to 3.3V. Using this circuit, the output of the mixer and power amplifier is ASK signal. And figure 4.17 is the simulation result for the transmitter.

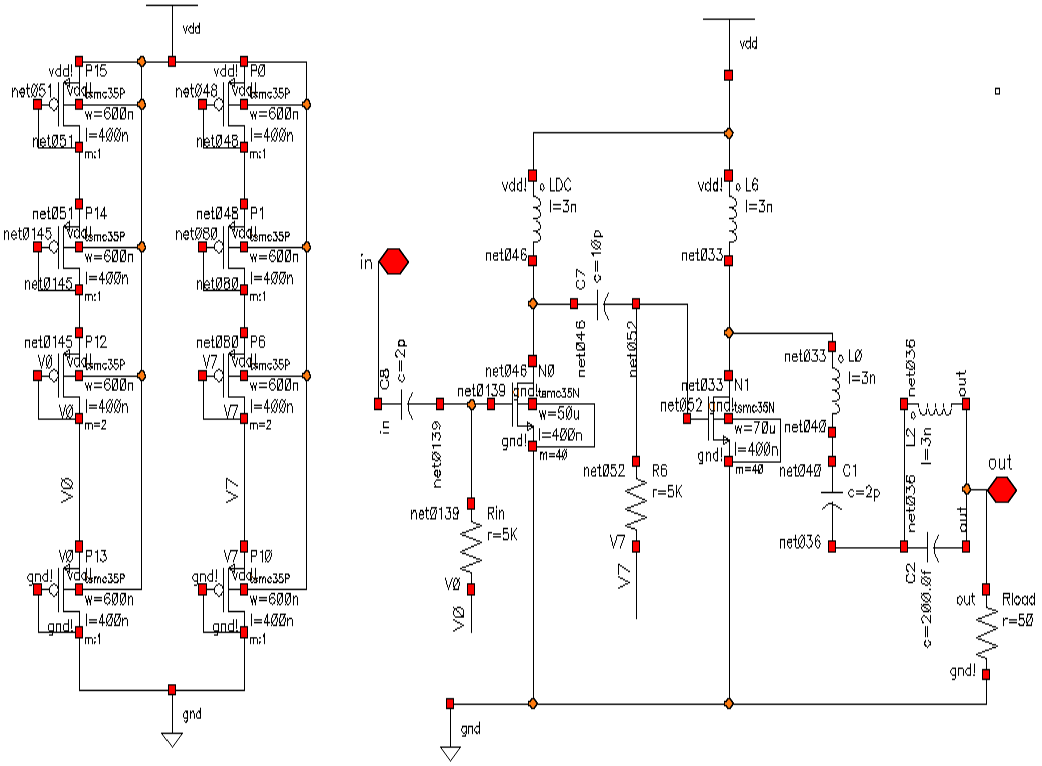


Figure 4.15---Power Amplifier

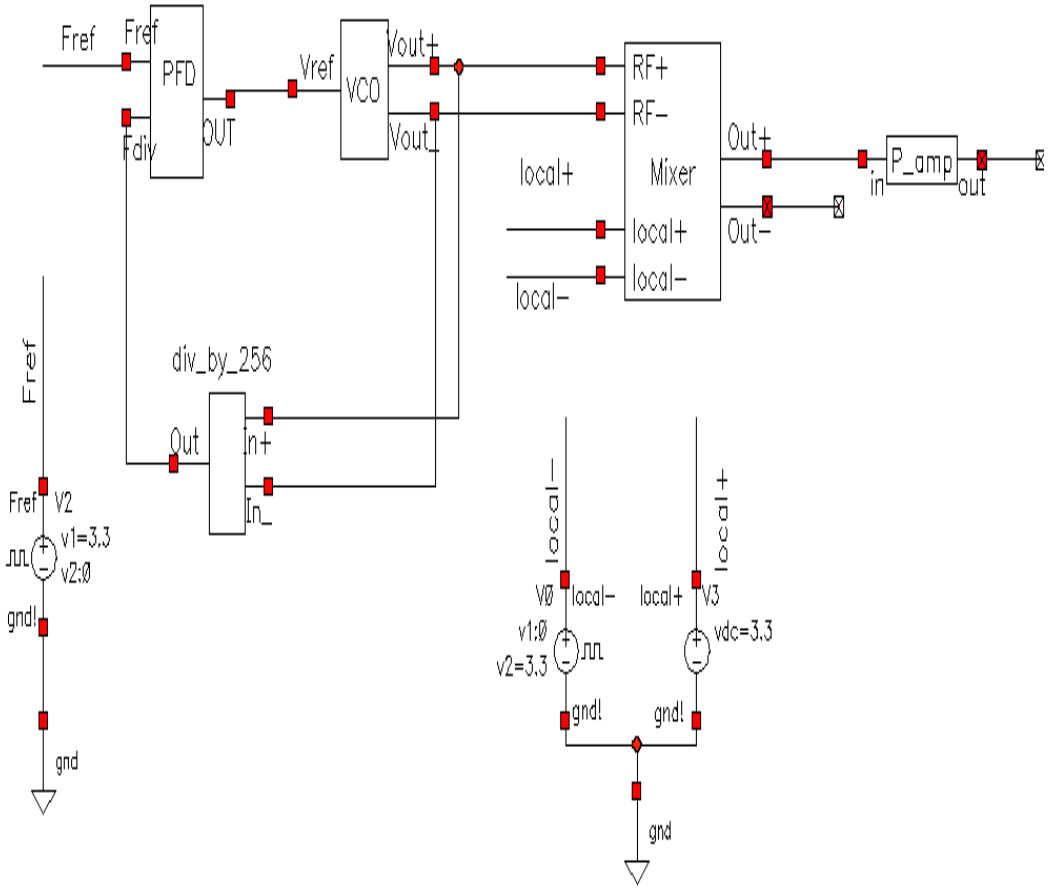


Figure 4.16---Complete Transmitter Schematic

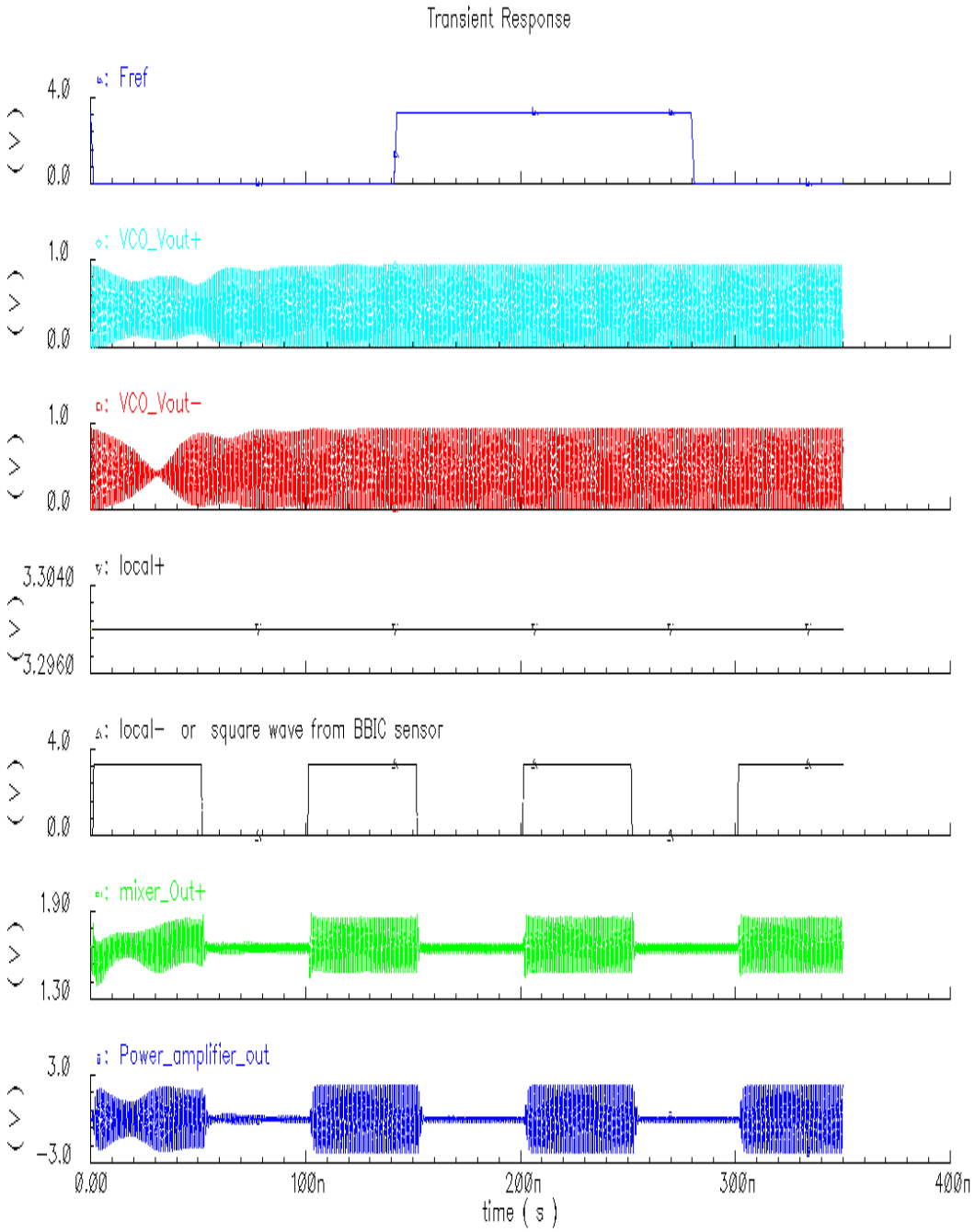


Figure 4.17---Complete Transmitter Simulation

CHAPTER 5

Conclusions and Future Work

5.1 Conclusions

A BBIC sensor chip with lower consumption was fabricated in the 0.35μm CMOS process. This design was an improvement over a previous BBIC [1]. Larger resisters are used instead of several small resisters, which were placed between power supply and ground and consumed too much power in the previous chip. Also, the bias currents for several amplifiers were reduced to decrease the power consumption even further. The chip was tested under normal light condition and it was verified that the device implemented the basic functions of a sensor. The power consumption has been reduced to 3.5% of the previous chip [1]. But the photodiode has a small area, so it cannot sense the bioluminescent come from the bioreporter. And the chip does not have protection for the pads, so it is very easy to destroy the chip. This new chip keeps most of the previous design. But to reduce the power consumption of the whole chip, larger resistors replaced several small resistors. And bias current of several amplifiers was also reduced.

The transmitter system was designed using CAD tools Cadence following previous work [2]. The power amplifier was added to the transmitter to give larger signal out of the circuit. The simulation was run in Cadence. This system performs well as expected.

5.2 Future work

Another version of BBIC sensor design is currently being developed. An OTA is used as an amplifier in the integrator. Several choices of the value of the integration capacitor, 0.5pF-1.5pF, will be fabricated in the chip and controlled by an off-chip digital control circuit. So by the testing the chip, the most appropriate value of the integration capacitor could be found. Voltage bias circuit will be built totally in the chip. A larger photodiode will be made to create enough photocurrent for the sensor. And a temperature sensor will also be made in the chip, because the biological calculation is closely related to the temperature. This new chip will also be fabricated in 0.35μm process.

The layout of the transmitter system will be performed soon, which will also be in 0.35μm process. With the fabrication of this transmitter chip in the future, the whole BBIC system will combine the bioluminescent bioreporter-sensing element with the wireless transmitter to complete the BBIC concept.

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Appendices

Appendix 1 Model Files

1. diode_model4002.txt

```
.MODEL DIN4002 D( IS=14.11E-9 N=1.984 RS=33.89E-3 IKF=94.81 XTI=3 EG=1.110
+CJO=51.17E-12 M=.2762 VJ=.3905 FC=.5 ISR=100.0E-12 NR=2 BV=100.1 IBV=10
+TT=4.761E-6)
```

2. diode_model4004.txt

```
.MODEL DIN4004 D( IS=14.11E-9 N=1.984 RS=33.89E-3 IKF=94.81 XTI=3 EG=1.110
+CJO=25.89E-12 M=.44 VJ=.3245 FC=.5 ISR=100.0E-12 NR=2 BV=400.1 IBV=10u
+TT=4.7E-6)
```

Appendix 2 BBIC Sensor Netlist

```
// Default Spectre Simulation run title card.

// Generated for: spectre
// Generated on: Mar 11 19:51:15 2003
// Design library name: mo350nm
// Design cell name: whole
// Design view name: schematic_chip3
simulator lang=spectre
global 0 vdd!

// Included Model Files
include "/home/mzhang2/research/diode_model4002.txt"
include "/sw/CDS/local/models/spectre/standalone/tsmc35P.m"
include "/sw/CDS/local/models/spectre/standalone/tsmc35N.m"
include "/home/mzhang2/research/diode_model4004.txt"

// Library name: mo350nm
// Cell name: dfnf311_dff
// View name: schematic
subckt dfnf311_dff DATA1 Q Q_b clk2
   M16 (_net0 _net1 0 0) tsmc35N w=5.3u l=700n as=5.3e-12 ad=5.3e-12 \
      ps=12.6u pd=12.6u m=1 region=sat
   M18 (_net2 _net3 _net4 0) tsmc35N w=3.9u l=700n as=3.9e-12 ad=3.9e-12 \
      ps=9.8u pd=9.8u m=1 region=sat
   M15 (_net5 _net2 0 0) tsmc35N w=5.3u l=700n as=5.3e-12 ad=5.3e-12 \
      ps=12.6u pd=12.6u m=1 region=sat
   M24 (Q Q_b 0 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 ps=16.0u \
      pd=16.0u m=1 region=sat
   M22 (Q_b _net1 _net6 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 ps=16.0u\
      pd=16.0u m=1 region=sat
   M17 (_net0 DATA1 _net2 0) tsmc35N w=5.3u l=700n as=5.3e-12 ad=5.3e-12\
      ps=12.6u pd=12.6u m=1 region=sat
   M19 (_net4 _net5 0 0) tsmc35N w=3.9u l=700n as=3.9e-12 ad=3.9e-12 \
      ps=9.8u pd=9.8u m=1 region=sat
   M8 (_net3 clk2 0 0) tsmc35N w=4.9u l=700n as=4.9e-12 ad=4.9e-12 \
      ps=11.8u pd=11.8u m=1 region=sat
   M23 (_net6 Q 0 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 ps=16.0u \
      pd=16.0u m=1 region=sat
   M20 (_net7 _net5 0 0) tsmc35N w=2.5u l=700n as=2.5e-12 ad=2.5e-12 \
      ps=7u pd=7u m=1 region=sat
   M9 (_net1 _net3 0 0) tsmc35N w=4.9u l=700n as=4.9e-12 ad=4.9e-12 \
      ps=11.8u pd=11.8u m=1 region=sat
   M21 (_net7 _net3 Q_b 0) tsmc35N w=2.5u l=700n as=2.5e-12 ad=2.5e-12 \
```

```
      ps=7u pd=7u m=1 region=sat
   M10 (_net8 _net1 vdd! vdd!) tsmc35P w=6u l=700n as=6e-12 ad=6e-12 \
      ps=14.0u pd=14.0u m=1 region=sat
   M11 (_net8 _net5 Q_b vdd!) tsmc35P w=6u l=700n as=6e-12 ad=6e-12 \
      ps=14.0u pd=14.0u m=1 region=sat
   M12 (Q_b _net3 _net9 vdd!) tsmc35P w=10.5u l=700n as=1.05e-11 \
      ad=1.05e-11 ps=23.0u pd=23.0u m=1 region=sat
   M14 (Q Q_b vdd! vdd!) tsmc35P w=10.9u l=700n as=1.09e-11 ad=1.09e-11 \
      ps=23.8u pd=23.8u m=1 region=sat
   M13 (_net9 Q vdd! vdd!) tsmc35P w=10.5u l=700n as=1.05e-11 ad=1.05e-11 \
      ps=23.0u pd=23.0u m=1 region=sat
   M7 (_net10 _net1 vdd! vdd!) tsmc35P w=3.2u l=700n as=3.2e-12 \
      ad=3.2e-12 ps=8.4u pd=8.4u m=1 region=sat
   M6 (_net2 _net5 _net10 vdd!) tsmc35P w=3.2u l=700n as=3.2e-12 \
      ad=3.2e-12 ps=8.4u pd=8.4u m=1 region=sat
   M5 (_net11 _net3 _net2 vdd!) tsmc35P w=3.5u l=700n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=1 region=sat
   M4 (_net11 DATA1 vdd! vdd!) tsmc35P w=3.5u l=700n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=1 region=sat
   M3 (_net5 _net2 vdd! vdd!) tsmc35P w=7.7u l=700n as=7.7e-12 ad=7.7e-12 \
      ps=17.4u pd=17.4u m=1 region=sat
   M2 (_net1 _net3 vdd! vdd!) tsmc35P w=8u l=700n as=8e-12 ad=8e-12 \
      ps=18.0u pd=18.0u m=1 region=sat
   M1 (_net3 clk2 vdd! vdd!) tsmc35P w=8u l=700n as=8e-12 ad=8e-12 \
      ps=18.0u pd=18.0u m=1 region=sat
ends dfnf311_dff
// End of subcircuit definition.

// Library name: mo350nm
// Cell name: one_shot_bolton
// View name: schematic
subckt one_shot_bolton Vbias Vbias_b in out
   M20 (out Q_B vdd! vdd!) tsmc35P w=3.9u l=700n as=3.9e-12 ad=3.9e-12 \
      ps=9.8u pd=9.8u m=1 region=sat
   M14 (Q_B reset vdd! vdd!) tsmc35P w=600n l=700n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=2 region=sat
   M10 (_net0 in vdd! vdd!) tsmc35P w=600n l=700n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=2 region=sat
   M12 (Q Q_B vdd! vdd!) tsmc35P w=600n l=700n as=6e-13 ad=6e-13 ps=3.2u\
      pd=3.2u m=2 region=sat
   M13 (Q_B Q vdd! vdd!) tsmc35P w=600n l=700n as=6e-13 ad=6e-13 ps=3.2u\
      pd=3.2u m=2 region=sat
   M11 (Q _net0 vdd! vdd!) tsmc35P w=600n l=700n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=2 region=sat
   M8 (top_plate Vbias vdd! vdd!) tsmc35P w=2.8u l=1.4u as=2.8e-12 \
```

```
   ad=2.8e-12 ps=7.6u pd=7.6u m=1 region=sat
M9 (vdd! Vbias vdd! vdd!) tsmc35P w=2.8u l=1.4u as=2.8e-12 ad=2.8e-12 \
   ps=7.6u pd=7.6u m=1 region=sat
M5 (0 reset _net1 vdd!) tsmc35P w=1.1u l=700n as=1.1e-12 ad=1.1e-12 \
   ps=4.2u pd=4.2u m=1 region=sat
M6 (reset top_plate _net1 vdd!) tsmc35P w=1.1u l=700n as=1.1e-12 \
   ad=1.1e-12 ps=4.2u pd=4.2u m=1 region=sat
M4 (_net1 top_plate vdd! vdd!) tsmc35P w=2.1u l=700n as=2.1e-12 \
   ad=2.1e-12 ps=6.2u pd=6.2u m=1 region=sat
N27 (net0193 net0193 net0189 0) tsmc35N w=600n l=400n as=6e-13 \
   ad=6e-13 ps=3.2u pd=3.2u m=1 region=sat
N24 (net0184 net0184 net0188 0) tsmc35N w=600n l=400n as=6e-13 \
   ad=6e-13 ps=3.2u pd=3.2u m=1 region=sat
N36 (net0153 net0153 net0152 0) tsmc35N w=600n l=400n as=6e-13 \
   ad=6e-13 ps=3.2u pd=3.2u m=1 region=sat
M19 (_net2 reset 0 0) tsmc35N w=1.1u l=700n as=1.1e-12 ad=1.1e-12 \
   ps=4.2u pd=4.2u m=1 region=sat
N26 (vdd! vdd! Vbias_b 0) tsmc35N w=600n l=400n as=6e-13 ad=6e-13 \
   ps=3.2u pd=3.2u m=4 region=sat
N28 (net0189 net0189 net0153 0) tsmc35N w=600n l=400n as=6e-13 \
   ad=6e-13 ps=3.2u pd=3.2u m=1 region=sat
N37 (net0152 net0152 0 0) tsmc35N w=600n l=400n as=6e-13 ad=6e-13 \
   ps=3.2u pd=3.2u m=1 region=sat
M17 (_net3 Q_B 0 0) tsmc35N w=600n l=700n as=6e-13 ad=6e-13 ps=3.2u \
   pd=3.2u m=2 region=sat
M21 (out Q_B 0 0) tsmc35N w=1.4u l=700n as=1.4e-12 ad=1.4e-12 ps=4.8u \
   pd=4.8u m=1 region=sat
N25 (Vbias_b Vbias_b net0184 0) tsmc35N w=600n l=400n as=6e-13 \
   ad=6e-13 ps=3.2u pd=3.2u m=1 region=sat
M16 (_net3 _net0 Q 0) tsmc35N w=1.1u l=700n as=1.1e-12 ad=1.1e-12 \
   ps=4.2u pd=4.2u m=1 region=sat
M18 (_net2 Q Q_B 0) tsmc35N w=1.1u l=700n as=1.1e-12 ad=1.1e-12 \
   ps=4.2u pd=4.2u m=1 region=sat
M7 (top_plate Q_B 0 0) tsmc35N w=1.4u l=3.5u as=1.4e-12 ad=1.4e-12 \
   ps=4.8u pd=4.8u m=1 region=sat
M15 (_net0 in 0 0) tsmc35N w=600n l=700n as=6e-13 ad=6e-13 ps=3.2u \
   pd=3.2u m=2 region=sat
N23 (net0188 net0188 net0192 0) tsmc35N w=600n l=400n as=6e-13 \
   ad=6e-13 ps=3.2u pd=3.2u m=1 region=sat
N22 (net0192 net0192 net0193 0) tsmc35N w=600n l=400n as=6e-13 \
   ad=6e-13 ps=3.2u pd=3.2u m=1 region=sat
M3 (reset top_plate _net4 0) tsmc35N w=1.1u l=700n as=1.1e-12 \
   ad=1.1e-12 ps=4.2u pd=4.2u m=1 region=sat
M1 (_net4 top_plate 0 0) tsmc35N w=1.4u l=700n as=1.4e-12 ad=1.4e-12 \
   ps=4.8u pd=4.8u m=1 region=sat
```

```
    M2 (vdd! reset _net4 0) tsmc35N w=1.1u l=700n as=1.1e-12 ad=1.1e-12 \
       ps=4.2u pd=4.2u m=1 region=sat
    C1 (top_plate 0) capacitor c=1.25p m=1
ends one_shot_bolton
// End of subcircuit definition.

// Library name: mo350nm
// Cell name: amplifier_autozero_b
// View name: schematic
subckt amplifier_autozero_b out vdd _net0 _net1
    C0 (net033 out) capacitor c=10p m=1
    R1 (net033 net16) resistor r=1.6K m=1
    N4 (net044 net044 0 0) tsmc35N w=3u l=4u as=3e-12 ad=3e-12 ps=8u pd=8u \
       m=1 region=sat
    N3 (net036 net036 net044 0) tsmc35N w=3u l=8u as=3e-12 ad=3e-12 ps=8u \
       pd=8u m=1 region=sat
    N2 (out net16 0 0) tsmc35N w=30u l=900n as=3e-11 ad=3e-11 ps=62.0u \
       pd=62.0u m=1 region=sat
    N1 (net12 net12 0 0) tsmc35N w=17.5u l=1.8u as=1.75e-11 ad=1.75e-11 \
       ps=37.0u pd=37.0u m=1 region=sat
    N0 (net16 net12 0 0) tsmc35N w=17.5u l=1.8u as=1.75e-11 ad=1.75e-11 \
       ps=37.0u pd=37.0u m=1 region=sat
    P5 (net036 net036 net38 net38) tsmc35P w=4u l=4u as=4e-12 ad=4e-12 \
       ps=10u pd=10u m=1 region=sat
    P4 (out net38 vdd vdd) tsmc35P w=14.0u l=1.4u as=1.4e-11 ad=1.4e-11 \
       ps=30u pd=30u m=1 region=sat
    P3 (net16 _net0 net31 vdd) tsmc35P w=14.0u l=1.4u as=1.4e-11 \
       ad=1.4e-11 ps=30u pd=30u m=1 region=sat
    P2 (net12 _net1 net31 vdd) tsmc35P w=14.0u l=1.4u as=1.4e-11 \
       ad=1.4e-11 ps=30u pd=30u m=1 region=sat
    P1 (net31 net38 vdd vdd) tsmc35P w=14.0u l=1.4u as=1.4e-11 ad=1.4e-11 \
       ps=30u pd=30u m=1 region=sat
    P0 (net38 net38 vdd vdd) tsmc35P w=14.0u l=1.4u as=1.4e-11 ad=1.4e-11 \
       ps=30u pd=30u m=1 region=sat
ends amplifier_autozero_b
// End of subcircuit definition.

// Library name: mo350nm
// Cell name: autozero
// View name: schematic
subckt autozero in out vdd
    R4 (net38 0) resistor r=100 m=1
    R5 (net7 0) resistor r=100 m=1
    N3 (vdd in out 0) tsmc35N w=28.0u l=700n as=2.8e-11 ad=2.8e-11 \
       ps=58.0u pd=58.0u m=1 region=sat
```

```
    N4 (out net40 net38 0) tsmc35N w=28.0u l=700n as=2.8e-11 ad=2.8e-11 \
       ps=58.0u pd=58.0u m=1 region=sat
    N5 (net18 net18 net22 0) tsmc35N w=5u l=700n as=5e-12 ad=5e-12 \
       ps=12.0u pd=12.0u m=1 region=sat
    N6 (net22 net22 0 0) tsmc35N w=2u l=1u as=2e-12 ad=2e-12 ps=6u pd=6u \
       m=1 region=sat
    P0 (net7 net35 vdd vdd) tsmc35P w=28.0u l=2.8u as=2.8e-11 ad=2.8e-11 \
       ps=58.0u pd=58.0u m=1 region=sat
    P1 (net35 net35 vdd vdd) tsmc35P w=28.0u l=2.8u as=2.8e-11 ad=2.8e-11 \
       ps=58.0u pd=58.0u m=1 region=sat
    P2 (net18 net18 net35 net35) tsmc35P w=3u l=1u as=3e-12 ad=3e-12 ps=8u \
       pd=8u m=1 region=sat
    I8 (net40 vdd net7 net38) amplifier_autozero_b
ends autozero
// End of subcircuit definition.

// Library name: mo350nm
// Cell name: comparator2
// View name: schematic
subckt comparator2 OUT _net0 Vin_ vdd
    N13 (net0108 net0108 0 0) tsmc35N w=2u l=3u as=2e-12 ad=2e-12 ps=6u \
       pd=6u m=1 region=sat
    N12 (dsc_ref dsc_ref net0108 0) tsmc35N w=2u l=3u as=2e-12 ad=2e-12 \
       ps=6u pd=6u m=1 region=sat
    N11 (net0148 net0148 dsc_bias 0) tsmc35N w=2u l=10u as=2e-12 ad=2e-12 \
       ps=6u pd=6u m=1 region=sat
    N10 (dsc_bias dsc_bias 0 0) tsmc35N w=8.4u l=700n as=8.4e-12 \
       ad=8.4e-12 ps=18.8u pd=18.8u m=1 region=sat
    N9 (OUT net15 0 0) tsmc35N w=3.5u l=700n as=3.5e-12 ad=3.5e-12 ps=9u \
       pd=9u m=1 region=sat
    N8 (net15 net21 0 0) tsmc35N w=1u l=700n as=1e-12 ad=1e-12 ps=4u pd=4u \
       m=1 region=sat
    N7 (net21 net23 0 0) tsmc35N w=1u l=700n as=1e-12 ad=1e-12 ps=4u pd=4u \
       m=1 region=sat
    N6 (net23 dsc_ref net021 0) tsmc35N w=8.4u l=700n as=8.4e-12 \
       ad=8.4e-12 ps=18.8u pd=18.8u m=1 region=sat
    N5 (net021 net33 0 0) tsmc35N w=4.2u l=700n as=4.2e-12 ad=4.2e-12 \
       ps=10.4u pd=10.4u m=1 region=sat
    N4 (net33 net33 0 0) tsmc35N w=4.2u l=700n as=4.2e-12 ad=4.2e-12 \
       ps=10.4u pd=10.4u m=1 region=sat
    N3 (net12 dsc_bias 0 0) tsmc35N w=4.2u l=700n as=4.2e-12 ad=4.2e-12 \
       ps=10.4u pd=10.4u m=1 region=sat
    N1 (net37 Vin_ net12 0) tsmc35N w=2u l=700n as=2e-12 ad=2e-12 ps=6u \
       pd=6u m=16 region=sat
    N0 (net9 _net0 net12 0) tsmc35N w=2u l=700n as=2e-12 ad=2e-12 ps=6u \
```

```
      pd=6u m=16 region=sat
   P11 (net32 net32 vdd vdd) tsmc35P w=2u l=700n as=2e-12 ad=2e-12 ps=6u \
      pd=6u m=1 region=sat
   P9 (dsc_ref dsc_ref net32 vdd) tsmc35P w=2u l=700n as=2e-12 ad=2e-12 \
      ps=6u pd=6u m=1 region=sat
   P8 (net0148 net0148 vdd vdd) tsmc35P w=2u l=10u as=2e-12 ad=2e-12 \
      ps=6u pd=6u m=1 region=sat
   P7 (OUT net15 vdd vdd) tsmc35P w=21.0u l=700n as=2.1e-11 ad=2.1e-11 \
      ps=44.0u pd=44.0u m=1 region=sat
   P6 (net15 net21 vdd vdd) tsmc35P w=1u l=700n as=1e-12 ad=1e-12 ps=4u \
      pd=4u m=1 region=sat
   P5 (net21 net23 vdd vdd) tsmc35P w=1u l=700n as=1e-12 ad=1e-12 ps=4u \
      pd=4u m=1 region=sat
   P4 (net23 dsc_ref net29 vdd) tsmc35P w=8.4u l=700n as=8.4e-12 \
      ad=8.4e-12 ps=18.8u pd=18.8u m=1 region=sat
   P3 (net29 net37 vdd vdd) tsmc35P w=4.2u l=700n as=4.2e-12 ad=4.2e-12 \
      ps=10.4u pd=10.4u m=1 region=sat
   P2 (net33 net9 vdd vdd) tsmc35P w=4.2u l=700n as=4.2e-12 ad=4.2e-12 \
      ps=10.4u pd=10.4u m=1 region=sat
   P1 (net37 net9 vdd vdd) tsmc35P w=4.2u l=700n as=4.2e-12 ad=4.2e-12 \
      ps=10.4u pd=10.4u m=1 region=sat
   P0 (net9 net9 vdd vdd) tsmc35P w=4.2u l=700n as=4.2e-12 ad=4.2e-12 \
      ps=10.4u pd=10.4u m=1 region=sat
ends comparator2
// End of subcircuit definition.

// Library name: mo350nm
// Cell name: 1stage_amp3
// View name: schematic
subckt mo350nm_1stage_amp3_schematic OUT _net0 Vin_ vdd
   C0 (net87 0) capacitor c=40p m=1
   R3 (net122 net87) resistor r=10K m=1
   N12 (net90 net90 0 0) tsmc35N w=4u l=1u as=4e-12 ad=4e-12 ps=10u \
      pd=10u m=1 region=sat
   N9 (net94 net94 0 0) tsmc35N w=1u l=2u as=1e-12 ad=1e-12 ps=4u pd=4u \
      m=1 region=sat
   N13 (net100 net100 0 0) tsmc35N w=10u l=1u as=1e-11 ad=1e-11 ps=22.0u \
      pd=22.0u m=1 region=sat
   N11 (net104 net104 0 0) tsmc35N w=4u l=1u as=4e-12 ad=4e-12 ps=10u \
      pd=10u m=1 region=sat
   N8 (vdd net122 OUT 0) tsmc35N w=1u l=20u as=1e-12 ad=1e-12 ps=4u
pd=4u \
      m=1 region=sat
   N7 (OUT net114 0 0) tsmc35N w=54.0u l=1u as=5.4e-11 ad=5.4e-11 \
      ps=110.00000u pd=110.00000u m=1 region=sat
```

```
    N6 (net114 net114 0 0) tsmc35N w=7u l=2.8u as=7e-12 ad=7e-12 ps=16.0u \
       pd=16.0u m=1 region=sat
    N5 (net118 net120 net90 0) tsmc35N w=24.9u l=7u as=2.49e-11 \
       ad=2.49e-11 ps=51.8u pd=51.8u m=1 region=sat
    N4 (net122 net120 net104 0) tsmc35N w=24.9u l=7u as=2.49e-11 \
       ad=2.49e-11 ps=51.8u pd=51.8u m=1 region=sat
    N3 (net120 net120 net100 0) tsmc35N w=24.9u l=7u as=2.49e-11 \
       ad=2.49e-11 ps=51.8u pd=51.8u m=1 region=sat
    P11 (net94 net94 net131 net131) tsmc35P w=1u l=2u as=1e-12 ad=1e-12 \
       ps=4u pd=4u m=1 region=sat
    P10 (net120 net131 vdd vdd) tsmc35P w=4.6u l=2.8u as=4.6e-12 \
       ad=4.6e-12 ps=11.2u pd=11.2u m=1 region=sat
    P9 (net114 net131 vdd vdd) tsmc35P w=4.6u l=2.8u as=4.6e-12 ad=4.6e-12 \
       ps=11.2u pd=11.2u m=1 region=sat
    P8 (net100 net131 vdd vdd) tsmc35P w=13.8u l=2.8u as=1.38e-11 \
       ad=1.38e-11 ps=29.6u pd=29.6u m=1 region=sat
    P4 (net104 Vin_ net0147 vdd) tsmc35P w=50u l=7u as=5e-11 ad=5e-11 \
       ps=102.000000u pd=102.000000u m=1 region=sat
    P3 (net90 _net0 net0147 vdd) tsmc35P w=50u l=7u as=5e-11 ad=5e-11 \
       ps=102.000000u pd=102.000000u m=1 region=sat
    P2 (net118 net118 vdd vdd) tsmc35P w=2u l=10u as=2e-12 ad=2e-12 ps=6u \
       pd=6u m=1 region=sat
    P1 (net122 net118 vdd vdd) tsmc35P w=2u l=10u as=2e-12 ad=2e-12 ps=6u \
       pd=6u m=1 region=sat
    P0 (net0147 net131 vdd vdd) tsmc35P w=27.6u l=2.8u as=2.76e-11 \
       ad=2.76e-11 ps=57.2u pd=57.2u m=1 region=sat
    M11 (net131 net131 vdd vdd) tsmc35P w=27.6u l=2.8u as=2.76e-11 \
       ad=2.76e-11 ps=57.2u pd=57.2u m=1 region=sat
ends mo350nm_1stage_amp3_schematic
// End of subcircuit definition.

// Library name: mo350nm
// Cell name: amplifier_stage2b
// View name: schematic
subckt amplifier_stage2b out vdd _net0 _net1
    C0 (net033 out) capacitor c=10p m=1
    R1 (net033 net16) resistor r=1.6K m=1
    N3 (net054 net054 0 0) tsmc35N w=4u l=2u as=4e-12 ad=4e-12 ps=10u \
       pd=10u m=1 region=sat
    N2 (out net16 0 0) tsmc35N w=30u l=900n as=3e-11 ad=3e-11 ps=62.0u \
       pd=62.0u m=1 region=sat
    N1 (net12 net12 0 0) tsmc35N w=17.5u l=1.8u as=1.75e-11 ad=1.75e-11 \
       ps=37.0u pd=37.0u m=1 region=sat
    N0 (net16 net12 0 0) tsmc35N w=17.5u l=1.8u as=1.75e-11 ad=1.75e-11 \
       ps=37.0u pd=37.0u m=1 region=sat
```

```
    P5 (net054 net054 net38 net38) tsmc35P w=4u l=2u as=4e-12 ad=4e-12 \
       ps=10u pd=10u m=1 region=sat
    P4 (out net38 vdd vdd) tsmc35P w=14.0u l=1.4u as=1.4e-11 ad=1.4e-11 \
       ps=30u pd=30u m=1 region=sat
    P3 (net16 _net0 net31 vdd) tsmc35P w=14.0u l=1.4u as=1.4e-11 \
       ad=1.4e-11 ps=30u pd=30u m=1 region=sat
    P2 (net12 _net1 net31 vdd) tsmc35P w=14.0u l=1.4u as=1.4e-11 \
       ad=1.4e-11 ps=30u pd=30u m=1 region=sat
    P1 (net31 net38 vdd vdd) tsmc35P w=14.0u l=1.4u as=1.4e-11 ad=1.4e-11 \
       ps=30u pd=30u m=1 region=sat
    P0 (net38 net38 vdd vdd) tsmc35P w=14.0u l=1.4u as=1.4e-11 ad=1.4e-11 \
       ps=30u pd=30u m=1 region=sat
ends amplifier_stage2b
// End of subcircuit definition.

// Library name: mo350nm
// Cell name: whole
// View name: schematic_chip3
I31 (net081 net044 net081 net071) dfnf311_dff
I29 (net042 net042 net063 net071) one_shot_bolton
V1 (vdd 0) vsource type=pulse val0=0 val1=3.3 delay=10m rise=1m
I21 (net3 net049 vdd) autozero
D0 (net0103 net049) DIN4004 m=1 region=on
I15 (net063 net0103 net0138 vdd) comparator2
I14 (net6 0 net025 vdd) mo350nm_1stage_amp3_schematic
I7 (net3 vdd net6 net1) amplifier_stage2b
I0 (net025 0) isource dc=8p m=1 type=dc
N2 (net017 vdd 0 0) tsmc35N w=8.4u l=700n as=8.4e-12 ad=8.4e-12 ps=18.8u \
      pd=18.8u m=1 region=sat
N0 (net049 net071 net017 0) tsmc35N w=14.0u l=700n as=1.4e-11 ad=1.4e-11 \
      ps=30u pd=30u m=1 region=sat
N1 (net017 net071 net025 0) tsmc35N w=14.0u l=700n as=1.4e-11 ad=1.4e-11 \
      ps=30u pd=30u m=1 region=sat
C2 (0 net025) capacitor c=8p m=1
C1 (net0103 0) capacitor c=900.0f m=1
C0 (net025 net049) capacitor c=500.0f m=1
V4 (net0138 0) vsource dc=1.5 type=dc
R1 (net1 0) resistor r=30K m=1
R0 (vdd! net1) resistor r=1MEG m=1
R6 (net1 net3) resistor r=300K m=1
R7 (net049 net0103) resistor r=7.2K m=1

// Spectre Source Statements

// Spectre Analyses and Output Options Statements
```

```
// Output Options
simOptions options
//+      reltol = 1.00000000E-03
//+      vabstol = 1.00000000E-06
//+      iabstol = 1.00000000E-12
//+      temp = 27
//+      save = allpub
//+      currents = selected



//   /home/mzhang2/research/ad8532.cir

Vconnect_vdd (vdd! vdd) vsource dc=0 type=dc
VGND (gnd! 0) vsource dc=0 type=dc
// Analyses
 dc1 dc oppoint=logfile homotopy=all
tran1 tran step=0.1e-4 stop=5e-1 errpreset=moderate
Format=UNORM

// End of Netlist
```

Appendix 3 Transmitter Netlist

```
// Default Spectre Simulation run title card.

// Generated for: spectre
// Generated on: Mar 11 20:49:59 2003
// Design library name: transmitter_350nm
// Design cell name: whole
// Design view name: schematic
simulator lang=spectre
global 0 vdd!

// Included Model Files
include "/home/mzhang2/research/diode_model4002.txt"
include "/sw/CDS/local/models/spectre/standalone/tsmc35P.m"
include "/sw/CDS/local/models/spectre/standalone/tsmc35N.m"
include "/home/mzhang2/research/diode_model4004.txt"

// Library name: transmitter_350nm
// Cell name: invertor_fast2
// View name: schematic
subckt invertor_fast2 in out vdd
    N0 (out in 0 0) tsmc35N w=10u l=400n as=1e-11 ad=1e-11 ps=22.0u \
        pd=22.0u m=1 region=sat
    P0 (out in vdd vdd) tsmc35P w=10u l=400n as=1e-11 ad=1e-11 ps=22.0u \
        pd=22.0u m=1 region=sat
ends invertor_fast2
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: mixer
// View name: schematic
subckt mixer _net19 _net17 _net10 _net11 _net18 _net0
    I19 (_net0 net100 vdd!) invertor_fast2
    I18 (net100 net97 vdd!) invertor_fast2
    I17 (net97 _net1 vdd!) invertor_fast2
    Rb2 (vdd! _net2) resistor r=2K m=1
    R7 (vdd! _net3) resistor r=570.00 m=1
    R5 (_net4 _net5) resistor r=1K m=1
    R0 (_net5 _net6) resistor r=1K m=1
    Rb3 (vdd! _net7) resistor r=10K m=1
    R8 (vdd! _net8) resistor r=800.0 m=1
    R6 (vdd! _net9) resistor r=570.00 m=1
    C3 (_net6 _net10) capacitor c=1p m=1
    C4 (_net5 0) capacitor c=1p m=1
```

```
   C5 (_net4 _net11) capacitor c=1p m=1
   V1 (Vreff 0) vsource dc=1 type=dc
   N30 (_net12 _net6 _net13 0) tsmc35N w=17.6u l=600n as=1.76e-11 \
      ad=1.76e-11 ps=37.2u pd=37.2u m=10 region=sat
   N21 (_net14 _net4 _net13 0) tsmc35N w=17.6u l=600n as=1.76e-11 \
      ad=1.76e-11 ps=37.2u pd=37.2u m=10 region=sat
   N34 (_net8 _net8 0 0) tsmc35N w=17.5u l=600n as=1.75e-11 ad=1.75e-11 \
      ps=37.0u pd=37.0u m=10 region=sat
   N33 (_net3 _net1 _net14 0) tsmc35N w=3.5u l=600n as=3.5e-12 ad=3.5e-12 \
      ps=9u pd=9u m=6 region=sat
   N37 (_net15 Vreff _net16 0) tsmc35N w=3.5u l=600n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=4 region=sat
   N36 (_net4 _net5 _net16 0) tsmc35N w=3.5u l=600n as=3.5e-12 ad=3.5e-12 \
      ps=9u pd=9u m=4 region=sat
   N31 (_net9 _net1 _net12 0) tsmc35N w=3.5u l=600n as=3.5e-12 ad=3.5e-12 \
      ps=9u pd=9u m=6 region=sat
   N29 (vdd! _net9 _net17 0) tsmc35N w=17.5u l=600n as=1.75e-11 \
      ad=1.75e-11 ps=37.0u pd=37.0u m=10 region=sat
   N35 (_net16 _net7 0 0) tsmc35N w=3.5u l=600n as=3.5e-12 ad=3.5e-12 \
      ps=9u pd=9u m=4 region=sat
   N32 (_net3 _net18 _net12 0) tsmc35N w=3.5u l=600n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=6 region=sat
   N24 (vdd! _net3 _net19 0) tsmc35N w=17.5u l=600n as=1.75e-11 \
      ad=1.75e-11 ps=37.0u pd=37.0u m=10 region=sat
   N22 (_net19 _net8 0 0) tsmc35N w=17.5u l=600n as=1.75e-11 ad=1.75e-11 \
      ps=37.0u pd=37.0u m=10 region=sat
   N25 (_net17 _net8 0 0) tsmc35N w=17.5u l=600n as=1.75e-11 ad=1.75e-11 \
      ps=37.0u pd=37.0u m=10 region=sat
   N28 (_net2 _net2 0 0) tsmc35N w=17.5u l=600n as=1.75e-11 ad=1.75e-11 \
      ps=37.0u pd=37.0u m=10 region=sat
   N27 (_net7 _net7 0 0) tsmc35N w=3.5u l=600n as=3.5e-12 ad=3.5e-12 \
      ps=9u pd=9u m=4 region=sat
   N26 (_net13 _net2 0 0) tsmc35N w=17.6u l=600n as=1.76e-11 ad=1.76e-11 \
      ps=37.2u pd=37.2u m=10 region=sat
   N23 (_net9 _net18 _net14 0) tsmc35N w=3.5u l=600n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=6 region=sat
   P8 (_net15 _net15 vdd! vdd!) tsmc35P w=3.5u l=600n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=2 region=sat
   P9 (_net4 _net15 vdd! vdd!) tsmc35P w=3.5u l=600n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=2 region=sat
ends mixer
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: power_amp
```

```
// View name: schematic
subckt power_amp in out
   P15 (net051 net051 vdd! vdd!) tsmc35P w=600n l=400n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=1 region=sat
   P13 (0 0 V0 vdd!) tsmc35P w=600n l=400n as=6e-13 ad=6e-13 ps=3.2u \
      pd=3.2u m=1 region=sat
   P10 (0 0 V7 vdd!) tsmc35P w=600n l=400n as=6e-13 ad=6e-13 ps=3.2u \
      pd=3.2u m=1 region=sat
   P14 (net0145 net0145 net051 vdd!) tsmc35P w=600n l=400n as=6e-13 \
      ad=6e-13 ps=3.2u pd=3.2u m=1 region=sat
   P0 (net048 net048 vdd! vdd!) tsmc35P w=600n l=400n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=1 region=sat
   P1 (net080 net080 net048 vdd!) tsmc35P w=600n l=400n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=1 region=sat
   P6 (V7 V7 net080 vdd!) tsmc35P w=600n l=400n as=6e-13 ad=6e-13 ps=3.2u \
      pd=3.2u m=2 region=sat
   P12 (V0 V0 net0145 vdd!) tsmc35P w=600n l=400n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=2 region=sat
   V8 (vdd! net035) vsource dc=0 type=dc
   V6 (net020 0) vsource dc=0 type=dc
   L6 (net035 net033) inductor l=3n m=1
   L0 (net033 net040) inductor l=3n m=1
   L2 (net036 out) inductor l=3n m=1
   LDC (vdd! net046) inductor l=3n m=1
   N1 (net033 net052 0 0) tsmc35N w=70u l=400n as=7e-11 ad=7e-11 \
      ps=142.000000u pd=142.000000u m=40 region=sat
   N0 (net046 net0139 0 0) tsmc35N w=50u l=400n as=5e-11 ad=5e-11 \
      ps=102.000000u pd=102.000000u m=40 region=sat
   Rin (net0139 V0) resistor r=5K m=1
   R6 (net052 V7) resistor r=5K m=1
   Rload (out net020) resistor r=50 m=1
   C7 (net046 net052) capacitor c=10p m=1
   C2 (net036 out) capacitor c=200.0f m=1
   C1 (net040 net036) capacitor c=2p m=1
   C8 (in net0139) capacitor c=2p m=1
ends power_amp
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: nanf401
// View name: schematic
subckt nanf401 A B C D Out
   M8 (_net0 A 0 0) tsmc35N w=8.4u l=700n as=8.4e-12 ad=8.4e-12 ps=18.8u \
      pd=18.8u m=1 region=sat
   M7 (_net1 B _net0 0) tsmc35N w=8.4u l=700n as=8.4e-12 ad=8.4e-12 \
```

```
      ps=18.8u pd=18.8u m=1 region=sat
   M6 (_net2 C _net1 0) tsmc35N w=8.4u l=700n as=8.4e-12 ad=8.4e-12 \
      ps=18.8u pd=18.8u m=1 region=sat
   M5 (Out D _net2 0) tsmc35N w=8.4u l=700n as=8.4e-12 ad=8.4e-12 \
      ps=18.8u pd=18.8u m=1 region=sat
   M4 (Out A vdd! vdd!) tsmc35P w=7.7u l=700n as=7.7e-12 ad=7.7e-12 \
      ps=17.4u pd=17.4u m=1 region=sat
   M3 (Out B vdd! vdd!) tsmc35P w=7.7u l=700n as=7.7e-12 ad=7.7e-12 \
      ps=17.4u pd=17.4u m=1 region=sat
   M2 (Out C vdd! vdd!) tsmc35P w=7.7u l=700n as=7.7e-12 ad=7.7e-12 \
      ps=17.4u pd=17.4u m=1 region=sat
   M1 (Out D vdd! vdd!) tsmc35P w=7.7u l=700n as=7.7e-12 ad=7.7e-12 \
      ps=17.4u pd=17.4u m=1 region=sat
ends nanf401
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: nanf301
// View name: schematic
subckt nanf301 A B C Out
   M6 (_net0 C Out 0) tsmc35N w=8.1u l=700n as=8.1e-12 ad=8.1e-12 \
      ps=18.2u pd=18.2u m=1 region=sat
   _inst1 (_net2 B _net0 0) tsmc35N w=8.1u l=700n as=8.1e-12 ad=8.1e-12 \
      ps=18.2u pd=18.2u m=1 region=sat
   M4 (_net2 A 0 0) tsmc35N w=8.1u l=700n as=8.1e-12 ad=8.1e-12 ps=18.2u \
      pd=18.2u m=1 region=sat
   M3 (Out C vdd! vdd!) tsmc35P w=8.4u l=700n as=8.4e-12 ad=8.4e-12 \
      ps=18.8u pd=18.8u m=1 region=sat
   M2 (Out B vdd! vdd!) tsmc35P w=8.4u l=700n as=8.4e-12 ad=8.4e-12 \
      ps=18.8u pd=18.8u m=1 region=sat
   M1 (Out A vdd! vdd!) tsmc35P w=8.4u l=700n as=8.4e-12 ad=8.4e-12 \
      ps=18.8u pd=18.8u m=1 region=sat
ends nanf301
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: nanf201
// View name: schematic
subckt nanf201 A B Out
   M4 (_net0 B Out 0) tsmc35N w=7.4u l=700n as=7.4e-12 ad=7.4e-12 \
      ps=16.8u pd=16.8u m=1 region=sat
   M3 (_net0 A 0 0) tsmc35N w=7.4u l=700n as=7.4e-12 ad=7.4e-12 ps=16.8u \
      pd=16.8u m=1 region=sat
   M2 (Out B vdd! vdd!) tsmc35P w=8.8u l=700n as=8.8e-12 ad=8.8e-12 \
      ps=19.6u pd=19.6u m=1 region=sat
```

```
    M1 (Out A vdd! vdd!) tsmc35P w=8.8u l=700n as=8.8e-12 ad=8.8e-12 \
        ps=19.6u pd=19.6u m=1 region=sat
ends nanf201
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: invf101
// View name: schematic
subckt invf101 In Out
    M1 (Out In vdd! vdd!) tsmc35P w=9.1u l=700n as=9.1e-12 ad=9.1e-12 \
        ps=20.2u pd=20.2u m=1 region=sat
    M2 (Out In 0 0) tsmc35N w=4.2u l=700n as=4.2e-12 ad=4.2e-12 ps=10.4u \
        pd=10.4u m=1 region=sat
ends invf101
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: phfdet
// View name: schematic
subckt phfdet D_not Down Fdiv Fref UP UP_not
    X11 (_net0 _net1 _net2 _net3 _net4) nanf401
    X8 (_net5 _net1 _net0 D_not) nanf301
    X12 (_net3 _net2 _net5 UP_not) nanf301
    X13 (Fref UP_not _net3) nanf201
    X6 (_net3 _net6 _net2) nanf201
    X5 (_net2 _net5 _net6) nanf201
    X4 (_net5 _net1 _net7) nanf201
    X7 (D_not Fdiv _net0) nanf201
    X3 (_net7 _net0 _net1) nanf201
    I7 (_net4 _net8) invf101
    X9 (_net8 _net5) invf101
    X2 (UP_not UP) invf101
    X1 (D_not Down) invf101
ends phfdet
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: isource
// View name: schematic
subckt isource _net0 IOUT_
    M8 (net061 net071 0 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 ps=42.0u \
        pd=42.0u m=1 region=sat
    M1 (net21 net21 net071 0) tsmc35N w=20u l=3.9u as=2e-11 ad=2e-11 \
        ps=42.0u pd=42.0u m=1 region=sat
    M22 (net049 net0157 0 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 ps=42.0u \
```

```
   pd=42.0u m=1 region=sat
M23 (net044 net0157 0 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 ps=42.0u \
   pd=42.0u m=1 region=sat
M20 (net057 net057 0 0) tsmc35N w=20u l=3.9u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M7 (net065 net21 net061 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M3 (net15 net21 net077 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M21 (net0157 net057 net049 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M24 (IOUT_ net057 net044 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M2 (net071 net071 0 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 ps=42.0u \
   pd=42.0u m=1 region=sat
M5 (net3 net21 net069 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 ps=42.0u \
   pd=42.0u m=1 region=sat
M6 (net069 net071 0 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 ps=42.0u \
   pd=42.0u m=1 region=sat
M4 (net077 net071 0 0) tsmc35N w=20u l=1u as=2e-11 ad=2e-11 ps=42.0u \
   pd=42.0u m=1 region=sat
P6 (net21 net21 vdd! vdd!) tsmc35P w=1.2u l=3.7u as=1.2e-12 ad=1.2e-12 \
   ps=4.4u pd=4.4u m=1 region=sat
M14 (net0157 net065 net025 vdd!) tsmc35P w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M9 (net065 net065 net031 vdd!) tsmc35P w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M12 (net057 net065 net021 vdd!) tsmc35P w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M11 (net021 net031 vdd! vdd!) tsmc35P w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M10 (net031 net031 vdd! vdd!) tsmc35P w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M13 (net025 net031 vdd! vdd!) tsmc35P w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=1 region=sat
M15 (net3 net3 vdd! vdd!) tsmc35P w=20u l=3.9u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=4 region=sat
M16 (net15 net3 net8 vdd!) tsmc35P w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=4 region=sat
M19 (_net0 net3 net12 vdd!) tsmc35P w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=4 region=sat
M17 (net8 net15 vdd! vdd!) tsmc35P w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=4 region=sat
M18 (net12 net15 vdd! vdd!) tsmc35P w=20u l=1u as=2e-11 ad=2e-11 \
   ps=42.0u pd=42.0u m=4 region=sat
```

```
ends isource
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: switch_core
// View name: schematic
subckt switch_core DOWN DOWN_NOT Iout UP UP_NOT
   N0 (net058 net058 net040 0) tsmc35N w=600n l=400n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=1 region=sat
   N1 (net040 net040 0 0) tsmc35N w=600n l=400n as=6e-13 ad=6e-13 ps=3.2u \
      pd=3.2u m=1 region=sat
   N2 (net044 net044 net058 0) tsmc35N w=600n l=400n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=1 region=sat
   M7 (Iout UP_NOT net018 0) tsmc35N w=15.0u l=700n as=1.5e-11 ad=1.5e-11
\
      ps=32.0u pd=32.0u m=10 region=sat
   M5 (net044 UP net018 0) tsmc35N w=15.0u l=700n as=1.5e-11 ad=1.5e-11 \
      ps=32.0u pd=32.0u m=10 region=sat
   M4 (net023 DOWN_NOT Iout 0) tsmc35N w=15.0u l=700n as=1.5e-11 \
      ad=1.5e-11 ps=32.0u pd=32.0u m=10 region=sat
   M3 (net023 DOWN net044 0) tsmc35N w=15.0u l=700n as=1.5e-11 ad=1.5e-
11 \
      ps=32.0u pd=32.0u m=10 region=sat
   P0 (net068 net068 vdd! vdd!) tsmc35P w=600n l=400n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=1 region=sat
   P1 (net044 net044 net068 vdd!) tsmc35P w=600n l=400n as=6e-13 ad=6e-13 \
      ps=3.2u pd=3.2u m=1 region=sat
   M8 (net018 UP Iout vdd!) tsmc35P w=22.7u l=700n as=2.27e-11 \
      ad=2.27e-11 ps=47.4u pd=47.4u m=5 region=sat
   M6 (net018 UP_NOT net044 vdd!) tsmc35P w=22.7u l=700n as=2.27e-11 \
      ad=2.27e-11 ps=47.4u pd=47.4u m=5 region=sat
   M2 (Iout DOWN net023 vdd!) tsmc35P w=22.7u l=700n as=2.27e-11 \
      ad=2.27e-11 ps=47.4u pd=47.4u m=5 region=sat
   M1 (net044 DOWN_NOT net023 vdd!) tsmc35P w=22.7u l=700n as=2.27e-11
\
      ad=2.27e-11 ps=47.4u pd=47.4u m=5 region=sat
   I3 (net023 net018) isource
ends switch_core
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: charge_pump_core
// View name: schematic
subckt charge_pump_core Fdiv Fref OUT
   I2 (net012 net2 Fdiv Fref net07 net06) phfdet
```

```
    ROUT (OUT net011) resistor r=203K m=1
    CF (net011 0) capacitor c=22.3p m=1
    CF1 (OUT 0) capacitor c=1.58p m=1
    I0 (net2 net012 OUT net07 net06) switch_core
ends charge_pump_core
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: cmldff2
// View name: schematic
subckt cmldff2 _net4 _net1 _net10 _net14 _net3 _net6 _net11
    M15 (_net0 _net0 _net1 _net1) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=3 region=sat
    M11 (_net2 _net2 _net1 _net1) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=3 region=sat
    M2 (_net3 _net3 _net1 _net1) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=3 region=sat
    M1 (_net4 _net4 _net1 _net1) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=3 region=sat
    M18 (_net0 _net2 _net5 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M19 (_net5 _net6 _net7 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M14 (_net0 _net4 _net8 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M17 (_net2 _net0 _net5 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M12 (_net2 _net3 _net8 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M9 (_net4 _net3 _net9 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M16 (_net7 _net10 0 0) tsmc35N w=26.3u l=2.5u as=2.63e-11 ad=2.63e-11 \
        ps=54.6u pd=54.6u m=6 region=sat
    M8 (_net9 _net11 _net12 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M10 (_net3 _net4 _net9 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M13 (_net8 _net11 _net7 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M5 (_net13 _net6 _net12 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M4 (_net3 _net0 _net13 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
    M3 (_net4 _net2 _net13 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
        ps=16.0u pd=16.0u m=5 region=sat
```

```
   M7 (_net12 _net10 0 0) tsmc35N w=26.3u l=2.5u as=2.63e-11 ad=2.63e-11 \
      ps=54.6u pd=54.6u m=6 region=sat
ends cmldff2
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: cmldff1
// View name: schematic
subckt cmldff1 _net8 _net4 _net15 _net7 _net11 _net1 _net10 _net2 _net0
   R1 (_net0 _net1) resistor r=1.152K m=1
   R2 (_net2 _net1) resistor r=1.152K m=1
   M25 (_net3 _net3 _net4 _net4) tsmc35P w=3.5u l=700n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=3 region=sat
   M26 (_net2 _net3 _net4 _net4) tsmc35P w=3.5u l=700n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=3 region=sat
   M15 (_net5 _net5 _net4 _net4) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=3 region=sat
   M11 (_net6 _net6 _net4 _net4) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=3 region=sat
   M2 (_net7 _net7 _net4 _net4) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=3 region=sat
   M1 (_net8 _net8 _net4 _net4) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=3 region=sat
   M28 (_net2 _net1 _net9 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=4 region=sat
   M30 (_net10 _net10 0 0) tsmc35N w=7u l=2.5u as=7e-12 ad=7e-12 ps=16.0u \
      pd=16.0u m=4 region=sat
   M27 (_net3 _net11 _net9 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=4 region=sat
   M18 (_net5 _net6 _net12 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M29 (_net9 _net10 0 0) tsmc35N w=7u l=2.5u as=7e-12 ad=7e-12 ps=16.0u \
      pd=16.0u m=4 region=sat
   M19 (_net12 _net2 _net13 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M14 (_net5 _net8 _net14 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M17 (_net6 _net5 _net12 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M12 (_net6 _net7 _net14 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M6 (_net15 _net15 0 0) tsmc35N w=3.5u l=2.5u as=3.5e-12 ad=3.5e-12 \
      ps=9u pd=9u m=6 region=sat
   M9 (_net8 _net7 _net16 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
```

```
   M16 (_net13 _net15 0 0) tsmc35N w=35.0u l=2.5u as=3.5e-11 ad=3.5e-11 \
      ps=72.0u pd=72.0u m=6 region=sat
   M8 (_net16 _net0 _net17 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M10 (_net7 _net8 _net16 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M13 (_net14 _net0 _net13 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M5 (_net18 _net2 _net17 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M4 (_net7 _net5 _net18 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M3 (_net8 _net6 _net18 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M7 (_net17 _net15 0 0) tsmc35N w=35.0u l=2.5u as=3.5e-11 ad=3.5e-11 \
      ps=72.0u pd=72.0u m=6 region=sat
ends cmldff1
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: div_by_4
// View name: schematic
subckt div_by_4 _net7 _net10 _net3 _net1 _net2 _net8 _net9 _net6 _net12 \
      _net5 _net11 _net4 _net0
   I4 (_net0 _net1 _net2 _net3 _net4 _net5 _net6) cmldff2
   I5 (_net6 _net1 _net7 _net5 _net8 _net9 _net10 _net11 _net12) cmldff1
ends div_by_4
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: cmldff
// View name: schematic
subckt cmldff _net6 _net1 _net14 _net5 _net8 _net2 _net10 _net15
   M25 (_net0 _net0 _net1 _net1) tsmc35P w=3.5u l=700n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=3 region=sat
   M26 (_net2 _net0 _net1 _net1) tsmc35P w=3.5u l=700n as=3.5e-12 \
      ad=3.5e-12 ps=9u pd=9u m=3 region=sat
   M15 (_net3 _net3 _net1 _net1) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=3 region=sat
   M11 (_net4 _net4 _net1 _net1) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=3 region=sat
   M2 (_net5 _net5 _net1 _net1) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=3 region=sat
   M1 (_net6 _net6 _net1 _net1) tsmc35P w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=3 region=sat
```

```
   M28 (_net2 _net6 _net7 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=4 region=sat
   M30 (_net8 _net8 0 0) tsmc35N w=7u l=2.5u as=7e-12 ad=7e-12 ps=16.0u \
      pd=16.0u m=4 region=sat
   M27 (_net0 _net5 _net7 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=4 region=sat
   M18 (_net3 _net4 _net9 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M29 (_net7 _net8 0 0) tsmc35N w=7u l=2.5u as=7e-12 ad=7e-12 ps=16.0u \
      pd=16.0u m=4 region=sat
   M19 (_net9 _net10 _net11 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M14 (_net3 _net6 _net12 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M17 (_net4 _net3 _net9 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M12 (_net4 _net5 _net12 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M9 (_net6 _net5 _net13 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M16 (_net11 _net14 0 0) tsmc35N w=17.5u l=2.5u as=1.75e-11 ad=1.75e-11 \
      ps=37.0u pd=37.0u m=6 region=sat
   M8 (_net13 _net15 _net16 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M10 (_net5 _net6 _net13 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M13 (_net12 _net15 _net11 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M5 (_net17 _net10 _net16 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M4 (_net5 _net3 _net17 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M3 (_net6 _net4 _net17 0) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
      ps=16.0u pd=16.0u m=5 region=sat
   M7 (_net16 _net14 0 0) tsmc35N w=17.5u l=2.5u as=1.75e-11 ad=1.75e-11 \
      ps=37.0u pd=37.0u m=6 region=sat
ends cmldff
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: dfnf311
// View name: schematic
subckt dfnf311 _net2 _net8 _net7 _net11 _net14 _net10
   M16 (_net0 _net1 _net2 _net2) tsmc35N w=5.3u l=700n as=5.3e-12 \
      ad=5.3e-12 ps=12.6u pd=12.6u m=1 region=sat
```

```
M18 (_net3 _net4 _net5 _net2) tsmc35N w=3.9u l=700n as=3.9e-12 \
   ad=3.9e-12 ps=9.8u pd=9.8u m=1 region=sat
M15 (_net6 _net3 _net2 _net2) tsmc35N w=5.3u l=700n as=5.3e-12 \
   ad=5.3e-12 ps=12.6u pd=12.6u m=1 region=sat
M24 (_net7 _net8 _net2 _net2) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
   ps=16.0u pd=16.0u m=1 region=sat
M22 (_net8 _net1 _net9 _net2) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
   ps=16.0u pd=16.0u m=1 region=sat
M17 (_net0 _net10 _net3 _net2) tsmc35N w=5.3u l=700n as=5.3e-12 \
   ad=5.3e-12 ps=12.6u pd=12.6u m=1 region=sat
M19 (_net5 _net6 _net2 _net2) tsmc35N w=3.9u l=700n as=3.9e-12 \
   ad=3.9e-12 ps=9.8u pd=9.8u m=1 region=sat
M8 (_net4 _net11 _net2 _net2) tsmc35N w=4.9u l=700n as=4.9e-12 \
   ad=4.9e-12 ps=11.8u pd=11.8u m=1 region=sat
M23 (_net9 _net7 _net2 _net2) tsmc35N w=7u l=700n as=7e-12 ad=7e-12 \
   ps=16.0u pd=16.0u m=1 region=sat
M20 (_net12 _net6 _net2 _net2) tsmc35N w=2.5u l=700n as=2.5e-12 \
   ad=2.5e-12 ps=7u pd=7u m=1 region=sat
M9 (_net1 _net4 _net2 _net2) tsmc35N w=4.9u l=700n as=4.9e-12 \
   ad=4.9e-12 ps=11.8u pd=11.8u m=1 region=sat
M21 (_net12 _net4 _net8 _net2) tsmc35N w=2.5u l=700n as=2.5e-12 \
   ad=2.5e-12 ps=7u pd=7u m=1 region=sat
M10 (_net13 _net1 _net14 _net14) tsmc35P w=6u l=700n as=6e-12 ad=6e-12 \
   ps=14.0u pd=14.0u m=1 region=sat
M11 (_net13 _net6 _net8 _net14) tsmc35P w=6u l=700n as=6e-12 ad=6e-12 \
   ps=14.0u pd=14.0u m=1 region=sat
M12 (_net8 _net4 _net15 _net14) tsmc35P w=10.5u l=700n as=1.05e-11 \
   ad=1.05e-11 ps=23.0u pd=23.0u m=1 region=sat
M14 (_net7 _net8 _net14 _net14) tsmc35P w=10.9u l=700n as=1.09e-11 \
   ad=1.09e-11 ps=23.8u pd=23.8u m=1 region=sat
M13 (_net15 _net7 _net14 _net14) tsmc35P w=10.5u l=700n as=1.05e-11 \
   ad=1.05e-11 ps=23.0u pd=23.0u m=1 region=sat
M7 (_net16 _net1 _net14 _net14) tsmc35P w=3.2u l=700n as=3.2e-12 \
   ad=3.2e-12 ps=8.4u pd=8.4u m=1 region=sat
M6 (_net3 _net6 _net16 _net14) tsmc35P w=3.2u l=700n as=3.2e-12 \
   ad=3.2e-12 ps=8.4u pd=8.4u m=1 region=sat
M5 (_net17 _net4 _net3 _net14) tsmc35P w=3.5u l=700n as=3.5e-12 \
   ad=3.5e-12 ps=9u pd=9u m=1 region=sat
M4 (_net17 _net10 _net14 _net14) tsmc35P w=3.5u l=700n as=3.5e-12 \
   ad=3.5e-12 ps=9u pd=9u m=1 region=sat
M3 (_net6 _net3 _net14 _net14) tsmc35P w=7.7u l=700n as=7.7e-12 \
   ad=7.7e-12 ps=17.4u pd=17.4u m=1 region=sat
M2 (_net1 _net4 _net14 _net14) tsmc35P w=8u l=700n as=8e-12 ad=8e-12 \
   ps=18.0u pd=18.0u m=1 region=sat
M1 (_net4 _net11 _net14 _net14) tsmc35P w=8u l=700n as=8e-12 ad=8e-12 \
```

```
      ps=18.0u pd=18.0u m=1 region=sat
ends dfnf311
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: div_by_256
// View name: schematic
subckt div_by_256 _net15 In_ Out
   I8 (_net0 _net1 _net2 _net3 _net2 _net4 _net5 _net6 _net7 _net8 _net9 \
      _net10 _net11) div_by_4
   I7 (_net12 _net3 _net2 _net13 _net1 _net4 _net10 _net11) cmldff
   Vref (_net4 0) vsource dc=1.5 type=dc
   Vdd (_net14 0) vsource dc=3.3 type=dc
   V0 (_net3 0) vsource dc=3.3 type=dc
   RM1 (_net15 0) resistor r=50 m=1
   Rvb (_net1 _net14) resistor r=8K m=1
   RB (_net0 _net14) resistor r=3K m=1
   RM2 (In_ 0) resistor r=50 m=1
   Rvb3 (_net2 _net14) resistor r=8K m=1
   CV1 (_net5 0) capacitor c=100p m=1
   CC1 (_net9 In_) capacitor c=5p m=1
   CC2 (_net7 _net15) capacitor c=5p m=1
   X7 (0 _net16 Out _net17 _net14 _net16) dfnf311
   X6 (0 _net18 _net17 _net19 _net14 _net18) dfnf311
   X5 (0 _net20 _net19 _net21 _net14 _net20) dfnf311
   X4 (0 _net22 _net21 _net23 _net14 _net22) dfnf311
   X3 (0 _net24 _net23 _net12 _net14 _net24) dfnf311
ends div_by_256
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: VCO
// View name: schematic
subckt VCO_schematic _net0 Vout_ Vref
   D1 (0 net051) DIN4002 m=1 region=on
   D0 (0 net053) DIN4002 m=1 region=on
   M7 (vdd! net83 _net0 0) tsmc35N w=7u l=500n as=7e-12 ad=7e-12 ps=16.0u \
      pd=16.0u m=6 region=sat
   M6 (Vout_ net67 0 0) tsmc35N w=7u l=500n as=7e-12 ad=7e-12 ps=16.0u \
      pd=16.0u m=6 region=sat
   M5 (vdd! net91 Vout_ 0) tsmc35N w=7u l=500n as=7e-12 ad=7e-12 ps=16.0u
\
      pd=16.0u m=6 region=sat
   M3 (net69 net69 0 0) tsmc35N w=8.8u l=500n as=8.8e-12 ad=8.8e-12 \
      ps=19.6u pd=19.6u m=4 region=sat
```

```
    M4 (net92 net69 0 0) tsmc35N w=8.8u l=500n as=8.8e-12 ad=8.8e-12 \
       ps=19.6u pd=19.6u m=8 region=sat
    M1 (net83 net91 net92 0) tsmc35N w=8.8u l=500n as=8.8e-12 ad=8.8e-12 \
       ps=19.6u pd=19.6u m=8 region=sat
    M2 (net91 net83 net92 0) tsmc35N w=8.8u l=500n as=8.8e-12 ad=8.8e-12 \
       ps=19.6u pd=19.6u m=8 region=sat
    M8 (_net0 net67 0 0) tsmc35N w=7u l=500n as=7e-12 ad=7e-12 ps=16.0u \
       pd=16.0u m=6 region=sat
    M9 (net67 net67 0 0) tsmc35N w=7u l=500n as=7e-12 ad=7e-12 ps=16.0u \
       pd=16.0u m=4 region=sat
    C1 (net053 net072) capacitor c=5p m=1 ic=0
    C2 (net051 net105) capacitor c=5p m=1 ic=0
    CT2 (net91 net105) capacitor c=13p m=1 ic=0
    CT1 (net072 net83) capacitor c=13p m=1 ic=0
    L2 (vdd! net91) inductor l=7.8n m=1 ic=0
    L1 (vdd! net83) inductor l=7.8n m=1 ic=0
    RB1 (vdd! net67) resistor r=400.0 m=1
    RB (vdd! net69) resistor r=5K m=1
    RT2 (Vref net105) resistor r=3.0000K m=1
    RT1 (Vref net072) resistor r=3.0000K m=1
ends VCO_schematic
// End of subcircuit definition.

// Library name: transmitter_350nm
// Cell name: whole
// View name: schematic
I3 (net033 net074 net12 net11 _net0 _net1) mixer
I8 (net033 net016) power_amp
V3 (_net0 0) vsource dc=3.3 type=dc
I0 (net9 Fref net7) charge_pump_core
I1 (net12 net11 net9) div_by_256
I2 (net12 net11 net7) VCO_schematic
V0 (_net1 0) vsource type=pulse val0=0 val1=3.3 period=100.0n delay=1n \
       width=50.0n
V2 (Fref 0) vsource type=pulse val0=3.3 val1=0 period=279.476n \
       width=139.737n

// Spectre Source Statements

// Spectre Analyses and Output Options Statements

// Output Options
simOptions options
//+      reltol = 1.00000000E-03
//+      vabstol = 1.00000000E-06
```

```
//+      iabstol = 1.00000000E-12
//+      temp = 27
//+      save = allpub
//+      currents = selected

vdd (vdd! 0) vsource dc=3.3 type=dc
VGND (gnd! 0) vsource dc=0 type=dc
// Analyses
 dc1 dc oppoint=logfile homotopy=all
tran1 tran step=0.1e-6 stop=0.35e-6 errpreset=moderate
Format=UNORM

// End of Netlist
```

Vita

Mo Zhang was born in Zhengzhou, China on April 22, 1977. She participated the Chinese Physics Competition for High School Students in 1994. And she was the only girl that was listed in the first prize in her province. In September 1995, she enrolled at Tsinghua University in Beijing. When attending Tsinghua University, she was a member of chorus group for five years. She received a Bachelor of Science Degree in Electrical Engineering from Tsinghua University in July 2000. She began her graduate work at the University of Tennessee in Knoxville in August of 2001. She was a research assistant in Analog VLSI and Devices Laboratory and awarded fellowships from UT CEB. She will receive a Master of Science degree in Electrical Engineering in May 2003. Mo Zhang is interested in singing, chatting and reading.