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A CONTROLLABLE POWER TAKE-OFF FOR MAGNETOHYDRODYNAMIC GENERATORS

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Kin Chun Kwong

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ABSTRACT

Electrical power must be extracted from a magnetohydrodynamic (MHD) generator by a power take-off (PTO) system that consolidates the current from the MHD channel's electrodes into a single load current.

In the conventional PTO system constructed from diodes and resistors, desired electrode currents cannot be maintained when generator conditions vary. In addition, significant power is dissipated in the resistors used. To overcome these problems, a controllable PTO circuit has been proposed using switching transistors to control the electrode currents.

To study the behavior of the switching PTO, a representative model using a proportional-integral controller was simulated and its operation examined. Simulation results verify that the controlled switching method can force the average electrode currents to their desired values as generator parameters vary. It is also found that there is a reduced power loss with the switching PTO circuit. These results indicate that it would be advantageous to replace the conventional PTO method by the controlled switching transistor system.

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NOMENCLATURE

A	System matrix
a	Cross-sectional area of DCW channel (m^2)
B	Input matrix
$\underline{B}$	Magnetic flux density (tesla)
c_{aj}, c_{bj}	Filter capacitors (F)
HR,LR	Resistances to simulate on/off state of switch (ohm)
i_L	Load current (amp)
i'_j	Electrode currents (amp)
i''_j	Switching currents (amp)
i'_j	Inductor currents (amp)
K	Load factor
K_1, K_2, K_3	Gain constant
R_j	Variable resistors (ohm)
T_j	Switching transistor
$\underline{u}$	Input vector
v	Velocity of plasma (m/s)
V_{aj}	Voltages across capacitors c_{aj}
V_{bj}	Voltages across capacitors c_{bj}
$\underline{x}$	State vector
α	Duty cycle (percent)
σ	Electric conductivity ($ohm^{-1}m^{-1}$)
Δ	Lumped effective voltage drop
ϕ	Direction of electric field
γ_j	Internal resistors (ohm)

CHAPTER I

INTRODUCTION

In the present energy crisis, a coal-fired magnetohydrodynamic (MHD) steam power plant holds great promise for electrical power generation. It has the potential to burn coal and produce electric power economically while meeting proposed Environmental Protection Agency (EPA) standards [1, 2, 3, 4][1]. A major problem with such a plan is the extraction of useful electrical power from the MHD channel. The power take-off (PTO) system consolidates the electrical output from the MHD channel into a single load. The purpose of this work is to demonstrate the feasibility of a controlled switching PTO.

Figure 1 is a block diagram of an open-cycle MHD steam power plant. Within the combustor, coal is burned with highly preheated air (1,600 to 2,000°K) at approximately 7 atm pressure. This combustion gas (2,500 to 2,800°K) is seeded with easily ionizable materials such as potassium carbonate (K_2CO_3) or potassium sulphate (K_2SO_4) to increase its conductivity. It is then accelerated through a nozzle and enters the MHD channel where electrical power is generated and extracted from a series of electrodes.

[1]Numbers in brackets refer to similarly numbered references in the Bibliography.

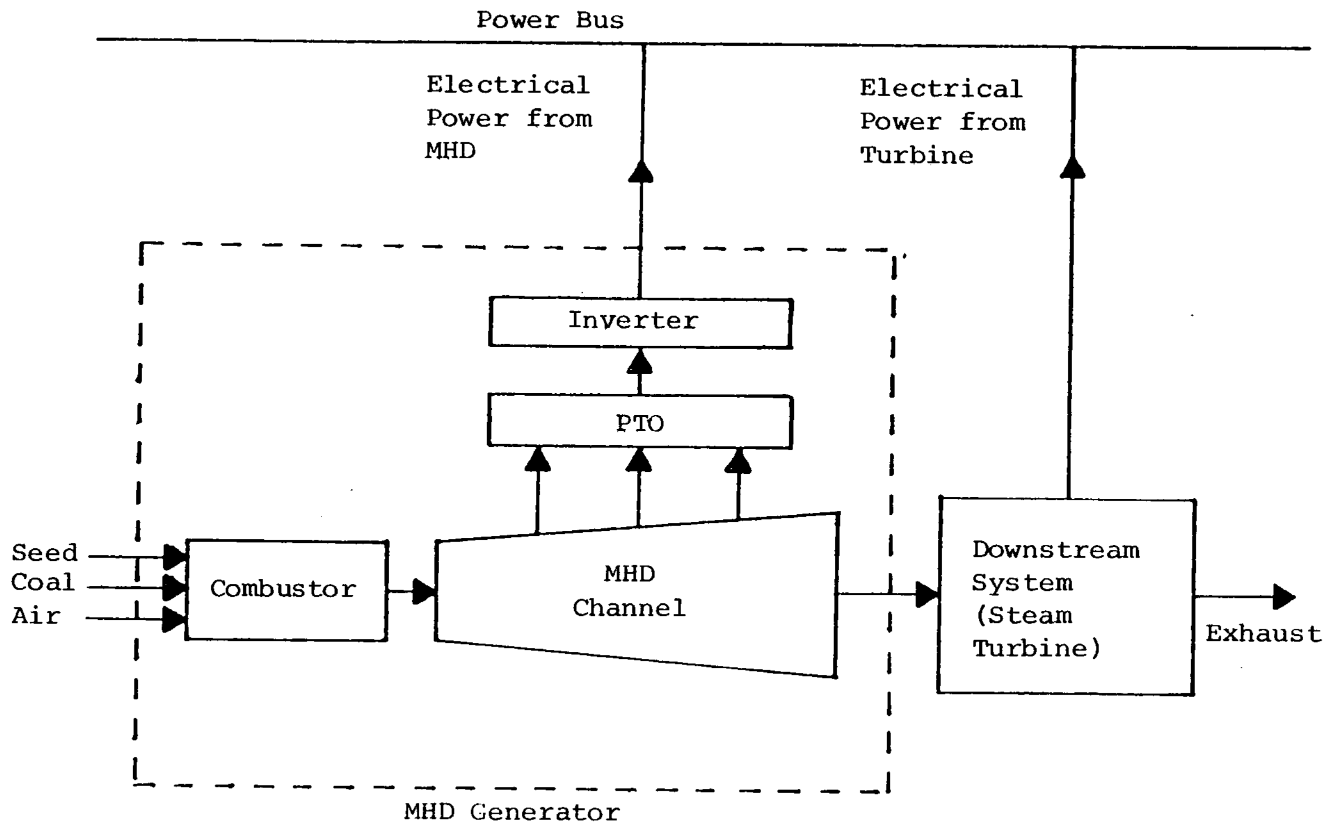


Figure 1. Open-Cycle MHD Steam Plant.

The PTO system must collect and consolidate this power and transform it into a useful form for the inverter, which ultimately converts the channel's direct current to an alternating current suitable for a large power grid [5]. Power is also produced by a steam turbine in the downstream system where heat is extracted from the plasma. The concern here is only with power removed from the MHD channel itself.

The amount of useful electrical power that can be extracted from an MHD channel depends on the design of the PTO scheme. In the conventional system, the direction and magnitude of electrode currents from the channel are governed by a set of diodes and resistors. Also note that the voltages of different electrodes are consolidated into a single load voltage. Because this consolidation involves a set of resistors, a significant I^2R power loss occurs. Since the required resistors are functions of the channel parameters, such as voltages and internal resistances, the conventional PTO system also fails to regulate the electrode currents as channel conditions vary [6].

To reduce this power loss and allow for the control of electrode currents under varying generator conditions, an active PTO circuit has been proposed using switching transistors [7]. In this case the average electrode current is determined by the switching transistor's duty cycle (i.e., the ratio of a transistor's ON time to its switching period). The duty cycle is controlled in a feedback arrangement utilizing the error between the average electrode currents and their desired values (i.e., the set points).

No previous investigation has been reported in the literature for the controlled switching PTO system. As a preliminary study of such a system, this work provides an analytical description for the switching PTO. Furthermore, the behavior of the conventional diode/resistor PTO and the controlled switching PTO are evaluated and compared under simulated load conditions.

For a representative MHD channel, a simulation involving a limited number of PTO electrodes was used so that the switching transistor's effects on all electrode currents could be investigated. The results of the simulation show that it is possible to replace the conventional technique by the controlled switching technique and obtain significantly better performance in the consolidation of electrical output from the MHD channel.

An equivalent circuit for a diagonally conducting wall (DCW), MHD channel and the conventional diode/resistor PTO is presented in Chapter II. A representative DCW channel is used to illustrate the performance of the diode/resistor PTO. Chapter III discusses the basic principles of the switching PTO, while in Chapter IV an analytical description of the switching PTO circuit is given. The controlled switching PTO circuit is then simulated using the Continuous System Modeling Program (CSMP). In Chapter IV, results from the simulation of the switching PTO are examined and compared with those from the diode/ resistor PTO. Concluding remarks and recommendations are given in Chapter VI.

CHAPTER II

DIAGONALLY CONDUCTING WALL CHANNEL AND DIODE/RESISTOR POWER TAKE-OFF

For the study of power take-off (PTO) systems, the magnetohydrodynamic (MHD) channel is modeled using an equivalent circuit. This chapter examines the basic equivalent circuit for the diagonally conducting wall (DCW) channel currently in use at The University of Tennessee Space Institute (UTSI).

The conventional PTO technique is then explored through the analysis and design of a diode/resistor PTO for a DCW channel like that used at UTSI. Using a simple, representative test case, the performance of the diode/resistor PTO is evaluated.

II.1. Equivalent Circuit for Diagonally Conducting Wall Channel

The DCW channel was first proposed by De Montardy [8] and Dicks [9]. Since then its performance has been studied extensively and promising results have been obtained [10, 11]. The generation of electricity in the DCW channel is based on the Faraday effect; that is, voltage is generated across a conductor when it moves through a magnetic field. Within the DCW channel, the conductor is plasma and the magnetic field is generated by a superconducting magnet [12].

To study PTO problems, a quasi-one-dimensional model for a DCW channel is used. This model has shown qualitative agreement with experimental data under steady-state conditions [6, 13]. Consider the DCW channel shown in Figure 2, where individual window-frame electrodes of pitch s (cm) are insulated from one another. The magnetic field $\underline{B}$ (tesla) is in the negative z-direction, while the plasma is flowing at velocity v (m/sec) in the x-direction.

Using the work of Wu [14], the channel can be analyzed as follows. In steady-state, the average Hall electric field intensity within the channel (in the x-direction) can be expressed as

$$E_x = \frac{vB(1-\Delta)(\Omega+\phi)}{(1+\phi^2)} (I/I_s - 1) , \qquad (2.1)$$

where Ω is the Hall parameter, ϕ is the direction of the electric field (i.e., $E_y/E_x = \phi$), Δ is the lumped effective voltage drop, I (amp) is the effective channel current, I_s (amp) is the short circuit current given by

$$I_s = \sigma avB(1-\Delta) \frac{(\Omega+\phi)}{(1+\Omega^2)} , \qquad (2.2)$$

where σ is the electrical conductivity of the plasma

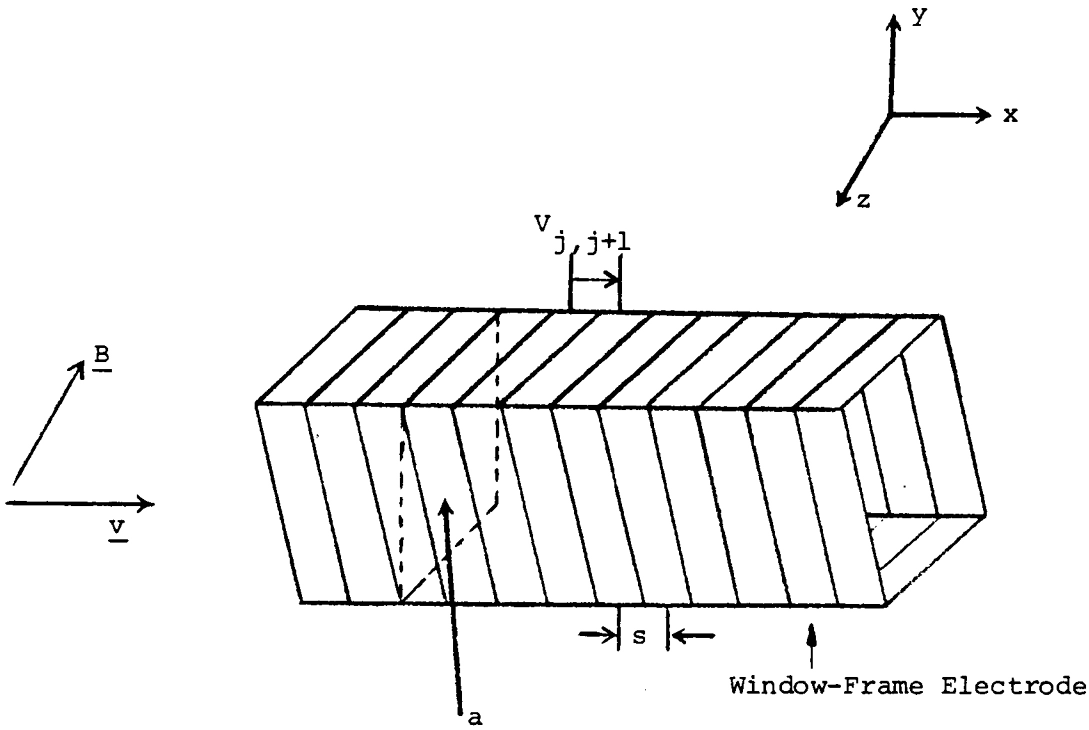


Figure 2. Schematic of a DCW Channel.

($ohm^{-1}m^{-1}$) and a is the cross-sectional area of the channel (m^2).

For the channel to operate in the "generator" mode, that is, for voltage to increase in the direction of current, E_x must be negative, so one must have

$$I \leq I_s \quad . \tag{2.3}$$

If the channel current is greater than the short-circuit current, then E_x is positive and there is field reversal; that is, voltage decreases in the direction of current flow.

Substituting Eq. (2.2) into Eq. (2.1) yields

$$E_x = \frac{(1+\Omega^2)}{\sigma a(1+\phi^2)} (I - I_s) \quad . \tag{2.4}$$

As illustrated in Figure 2, over one electrode pitch, the interelectrode voltage (voltage drop between two adjacent electrodes) $V_{j,j+1}$ is given by

$$V_{j,j+1} = -\int_{o}^{s} \underline{E} \cdot d\underline{s} \tag{2.5}$$

$$= - E_x \, s \tag{2.6}$$

$$= \frac{(1+\Omega^2)\, s}{\sigma a(1+\phi^2)} \, (I_s - I_j) \tag{2.7}$$

$$= r(I_s - I_j) \tag{2.8}$$

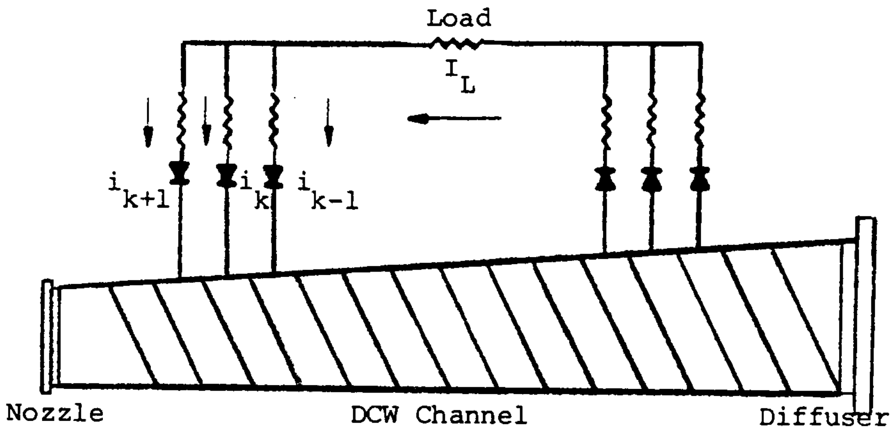
$$= V_{ocj} - r \, I_j \, , \tag{2.9}$$

where

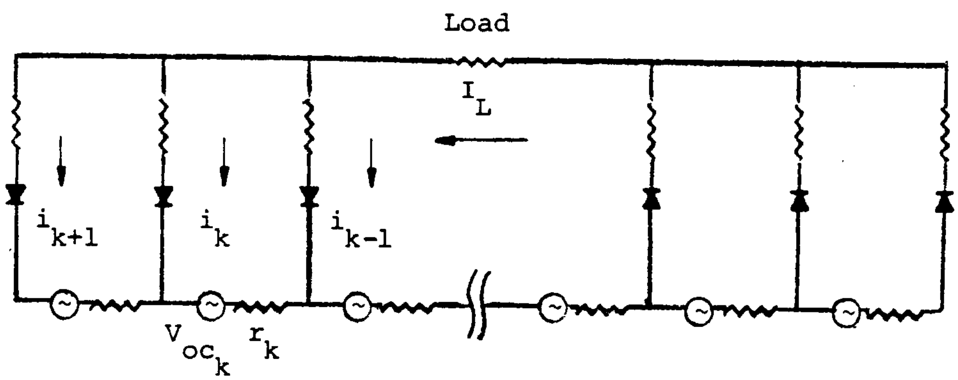
$$r = \frac{(1+\Omega^2)\, s}{\sigma a(1+\phi^2)} \tag{2.10}$$

is the equivalent resistance (ohm) of the plasma as it conducts current from one electrode to the other, and I_j is the channel current flowing between the j^{th} and the $j+1^{th}$ electrode.

A general loading scheme for a DCW channel is depicted in Figure 3a. The current from/to each electrode is carried to/from the external load through the PTO. The purpose of the PTO is to fix the direction and magnitude of the current to/from each electrode so that the current distribution of I_j along the channel can be set at desired values. Furthermore, it combines the voltages of different electrodes into a single voltage at the load.



(a) Schematic



(b) Equivalent Circuit

Figure 3. Electrical Loading for a DCW Channel.

Diodes and resistors are currently used for the PTO at UTSI. With Eq. (2.9), an equivalent electric circuit for the loading of a DCW channel can be obtained as shown in Figure 3b. The voltage source (V_{OC}) and the internal resistor (r) are connected in series between two adjacent electrodes. Six diodes and resistors are chosen arbitrarily to provide a simple illustration of the loading for the DCW channel.

II.2. Diode/Resistor Power Take-Off

In this section, the design of a diode/resistor PTO is illustrated by an example. Each electrode is connected to the bus bar through a diode and resistor in series. The direction of the current is fixed by the diode and the magnitude of the current is determined by the value of the resistor used. A single load current is formed by collecting all electrode currents.

From Galanga et al. [15], the effective channel current in Eq. (2.7) can be expressed as

$$I_j = I_s (1 - K) , \qquad (2.11)$$

where K is the Hall load factor. Equation (2.11) can be used to specify a desired distribution of I_j by a proper choice of the load factor K.

Given a preselected current distribution along the channel,

$$I = f(x) \ , \qquad (2.12)$$

the Hall field distribution throughout the generator can be determined from an appropriate analytical model [15] as

$$E_x = g(x) \ . \qquad (2.13)$$

Figure 4 shows the equivalent circuit for a diode/resistor PTO with six electrodes: e_k (k=1 to 5) represents the voltage source (i.e., V_{ocj} in Eq. (2.9)); r_k (k=1 to 5) represents the internal resistance of the plasma; and R_j (j=0 to 5) represents the PTO resistor. Across the load resistor R_L, the following can be written:

$$V_L = I_L R_L = V_{23} - R_3 i_3 - R_2 i_2 \ , \qquad (2.14)$$

while other loops yield

$$R_{j+1}\, i_{j+1} - R_j i_j = V_{j,j+1} \qquad j = 3,4 \ , \qquad (2.15)$$

$$R_j i_j - R_{j+1}\, i_{j+1} = V_{j,j+1} \qquad j = 0,1 \ , \qquad (2.16)$$

where i_j is the current flowing through the corresponding diode. The channel and diode currents are related by:

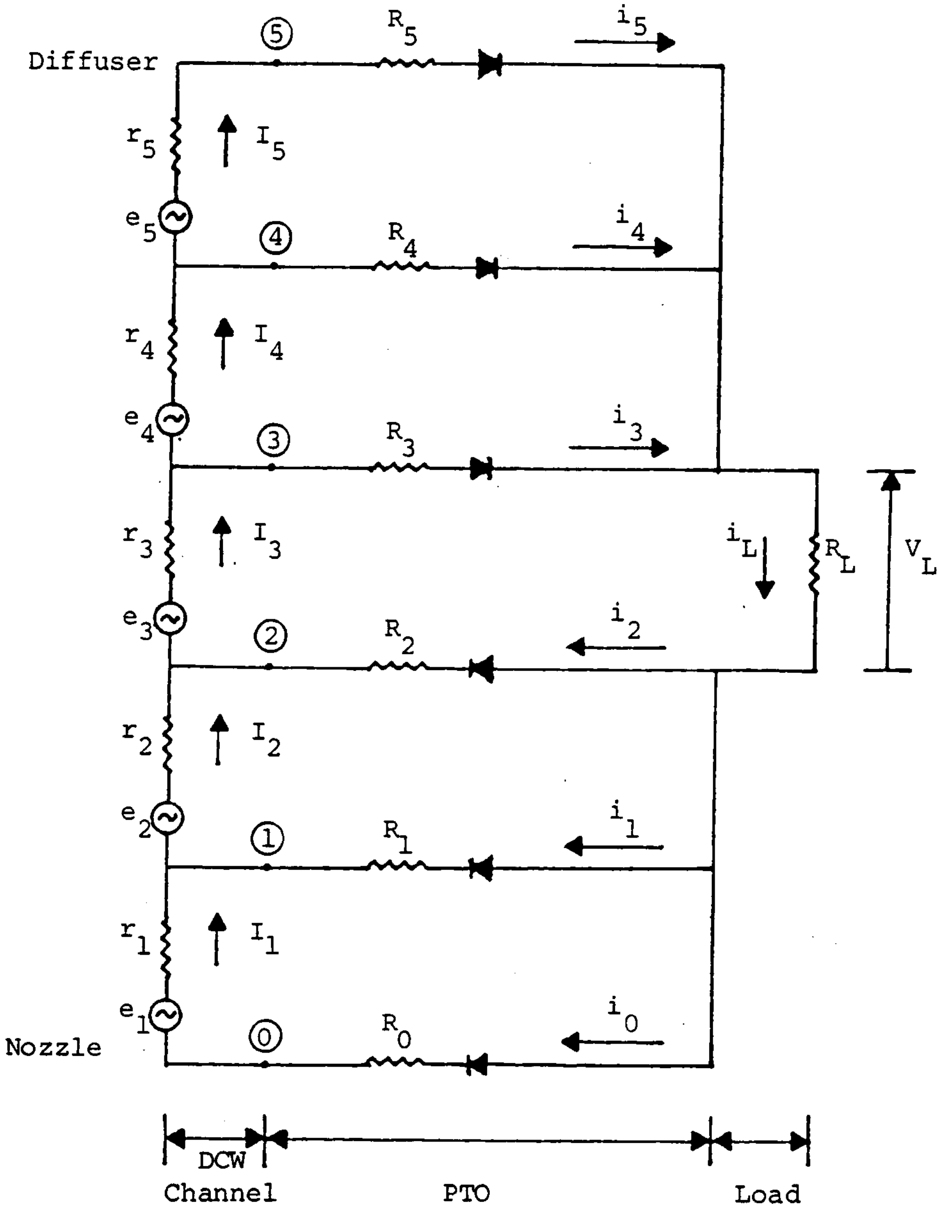


Figure 4. Diode/Resistor PTO Model (Six Electrodes).

$$i_j = I_j - I_{j+1} \qquad j = 3,4 \ , \tag{2.17}$$

$$i_j = I_{j+1} - I_j \qquad j = 1,2 \ , \tag{2.18}$$

$$i_5 = I_5 \ , \tag{2.19}$$

$$i_0 = I_1 \ . \tag{2.20}$$

Note that only five diode currents are independent since

$$i_0 + i_1 + i_2 = i_3 + i_4 + i_5 \ .$$

This yields a total of five linearly independent equations (Eqs. (2.14), (2.15), (2.16)) for the seven unknowns (all R_j values and R_L). Therefore, it is necessary to impose two additional constraints to find the resistors that yield a given i_j (or I_j). This can be done by setting the load voltage V_L and the voltages across the PTO resistors R_2 and R_3.

The DCW channel's parameters (e_k's and r_k's) are obtained by using a program called DESIGN 3 [16], a steady-state channel simulation utilizing a quasi-one-dimensional model, as discussed in Section II.1. It is operated using the design conditions for the Coal-Fired Flow Facility (CFFF) at UTSI. Table 1 lists the circuit parameters for a representative channel with the characteristics given in Table 2.

The current distribution for this channel is chosen to be half the short circuit (i.e., K=0.5 in Eq. (2.11)).

Table 1. Equivalent Circuit Parameters for DCW Channel

k	Voltage Sources (V) e_k	Internal Resistance (ohm) r_k	Short Circuit Current (amp) Is_k
5	187	3	62.4
4	730	3.36	217.2
3	6,090	25.91	235.4
2	410	3.07	133.54
1	54.3	5.03	10.8

Table 2. Operating Conditions for DCW Channel

	Value	Unit
Mass Flow Rate	3.5617	K_g/sec
Temperature Entrance	2,696	^oK
Pressure Entrance	40.381	psia
Magnetic Field (B)	3.2	tesla

For this value of K, Eq. (2.3) is satisfied and there will be no field reversal. Furthermore, this current corresponds to the condition when maximum power is transferred by two adjacent electrodes [14]. The current flowing through each PTO resistor, i_j, can then be obtained from the desired current distribution and Eqs. (2.17) through (2.20):

$$i_0 = 5.4 \text{ A} \quad ; \quad i_1 = 61.37 \text{ A} \quad ; \quad i_2 = 50.75 \text{ A}$$

$$i_3 = 8.92 \text{ A} \quad ; \quad i_4 = 77.4 \text{ A} \quad ; \quad i_5 = 31.2 \text{ A} .$$

Since the voltage source e_3 is more than ten times larger than the others, it can be assumed that it has a dominant effect on the load voltage. In a circuit of e_3, r_3, and R_L connected in series, maximum power output to R_L can be obtained when the voltage across R_L is half the value of e_3. For convenience, V_L is chosen to be 3,000 V. This also allows sufficient voltage drops across R_2 and R_3 in the circuit shown in Figure 4, page 14.

It is noted from Figure 4 that the load current is the same as I_3; that is, i_L=117.52 amps. The value of the load is then calculated as

$$R_L = V_L/i_L = 25.52 \text{ ohms} .$$

Equation (2.14) with $R_3 i_3 = R_2 i_2$ then gives

$$R_2 = 0.96 \text{ ohm}$$

$$R_3 = 2.03 \text{ ohms} .$$

The remaining PTO resistors can be calculated from Eqs. (2.15) and (2.16):

$$R_5 = 15.4 \text{ ohms} ,$$

$$R_4 = 5.0 \text{ ohms} ,$$

$$R_1 = 3.7 \text{ ohms} ,$$

$$R_0 = 47.2 \text{ ohms} .$$

Using these values for the load and PTO resistors, the performance of this diode/resistor PTO model can be examined. The power dissipated in the PTO and the load resistor, as well as the overall performance of the model, are shown in Table 3. There is significant power dissipated in the PTO resistors (15% of the power available to the load from the channel). If more PTO resistors are used, the power dissipated in these resistors would become even greater.

Since the PTO resistors are matched to the MHD channel, the desired current distribution cannot be achieved when there are changes in the channel characteristics. Therefore, if the plasma conditions change, the

Table 3. Overall Power Performance for the Diode/Resistor Model

Resistor	Power Dissipation (watt)	Power Dissipation (percent)
R_5	14,952.56	
R_4	30,008.0	
R_3	199.95	
R_2	1,184.76	
R_1	13,939.8	
R_0	1,372.4	
Total	61,657.47	14.89
R_L	352,455.45	85.11
Total Power Output from Electrodes	414,112.93	100.0

Hall field intensity and thus, the internal voltage, will be altered. Since the channel is continuous, it can be assumed that the changes are uniform; that is, all voltages will increase or decrease in the same proportion. For the linear PTO circuit shown in Figure 4, page 14, the currents will also increase or decrease in the same proportion as the changes in the voltages. For example, a 10% increase in the voltages (e_k ; k=1 to 5) will result in a 10% increase in the currents.

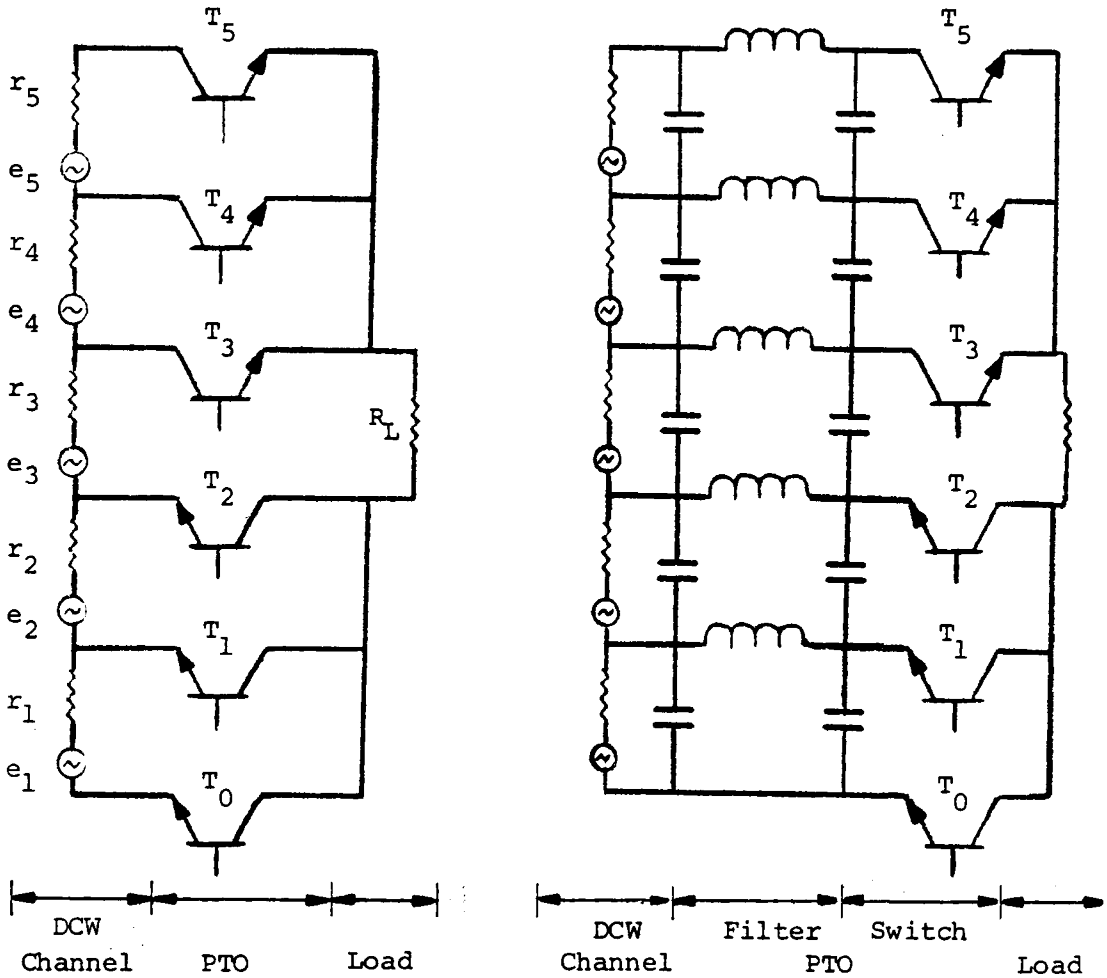
Since the diode/resistor PTO produces a significant power loss and is unable to control electrode currents under varying channel conditions, an alternative method has been sought. Recently, a technique used in switched power regulators was suggested by Fowler [7] for the PTO. The resistor and diode in each branch of the diode/resistor PTO (Figure 4) is replaced by a switching transistor. Since the average current flowing through the transistor can be controlled, the system can be made to react to changes in channel conditions and return the average electrode currents to their desired values. In addition, the switching arrangement produces a minimal power loss. This active PTO is the subject of Chapter III.

CHAPTER III

PRINCIPLES OF SWITCHING POWER TAKE-OFF SYSTEM

Since the primary purpose of the PTO is to regulate the current flowing from individual electrodes toward the load, an active current controller (controlled switching transistor) can be used to replace each series diode/ resistor combination in Figure 4, page 14. This chapter presents the essential details of this switching PTO starting with the basic circuit of Figure 5a. In this circuit the current from each electrode flows through a transistor whose on/off switching controls the average current through that branch. The transistor also determines the direction of the current flowing in that branch. Since the switch's pulsing effect on the MHD channel is not desirable, it must be minimized by inserting a suitable filter between the electrode and the transistor in each branch [7]. The overall circuit is shown in Figure 5b.

To control the current flowing in each branch, the error between the average electrode current and the corresponding set point value is transmitted to a device which sets the on/off function of the switching transistor. This controlling device operates to force the error to zero and thus regulates the average current to its desired value.



(a) Without Filter (b) With Filter

Figure 5. Controlled Switching PTO.

The switching PTO has three major components: the switching transistor which determines the average current, the controller which sets the on/off of the transistors, and the filter which isolates the pulsing transistor from the channel's electrode. The following sections describe the operation of each part in detail.

III.1. Switching Transistor

A base current-controlled switching transistor circuit is shown in Figure 6a. The pulse train input to the base, as shown in Figure 6b, controls the switching transistor. When the base voltage of the transistor of Figure 6a is negative, the transistor is cut off and no collector current flows [17]. If a large enough current is driven into the base to saturate the transistor, which now resembles a closed switch, collector current flows. The collector's response to the input pulse train of Figure 6b is shown in Figure 6c. Compared to a resistor, the power dissipated in the switching transistor is very small, since the transistor is always in the saturated state when it is conducting, and otherwise is completely nonconducting [17].

For a periodic pulse train, the duty cycle (α) is defined as the ratio of the ON-time (t_{ON}) to the period (τ),

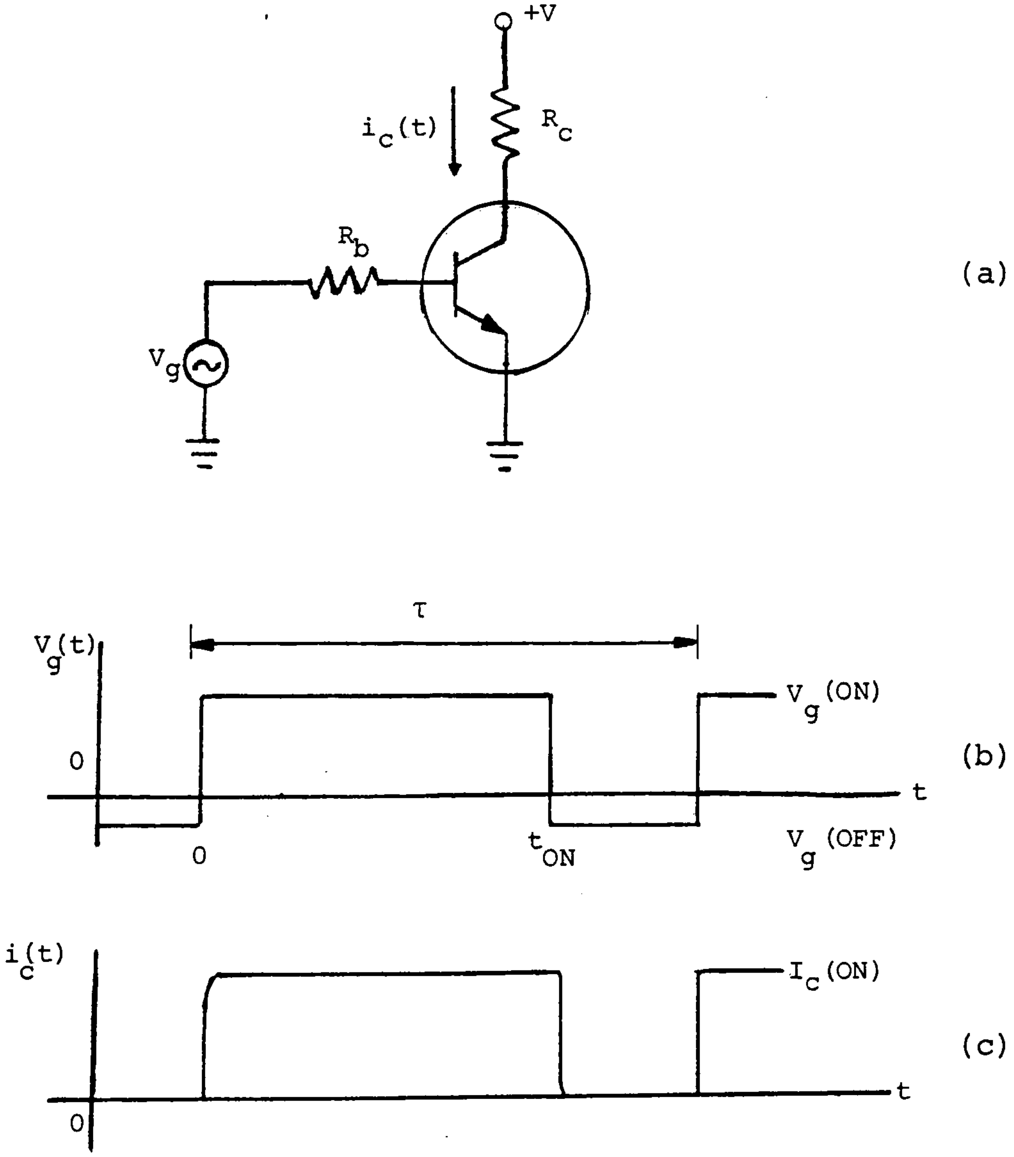


Figure 6. Controlled Switching Transistor.

$$\alpha = t_{ON}/\tau = t_{ON}\, f \;, \tag{3.1}$$

where f is the switching frequency; that is, $f=1/\tau$.

Consider $V_g(t)$ and $i_c(t)$ in Figure 6c to be periodic; the average value of I_c can then be obtained by [18]

$$\langle i_c \rangle = \frac{1}{\tau}\int_0^{\tau} i_c(t)\,dt \tag{3.2}$$

$$= \frac{1}{\tau}\, I_c\, t_{ON} \tag{3.3}$$

$$= \alpha\, I_c \;, \tag{3.4}$$

where I_c is the magnitude of $i_c(t)$ when the transistor is ON. Thus, the average current is directly proportional to the duty cycle.

To simplify the analysis of switching PTO, it is assumed that the switches are characterized as follows:

1. The switches have low resistances when they are conducting and high resistances when they are nonconducting.
2. Transitions between the ON and OFF states are instantaneous.

When such a switch is placed in series with an electrode, as shown in Figure 5a, page 23, the average current flowing through the switch can be set to the desired value with proper control of the switching duty cycle. Section II.2

describes a device which will control the duty cycle of the switching transistor.

III.2. Controller

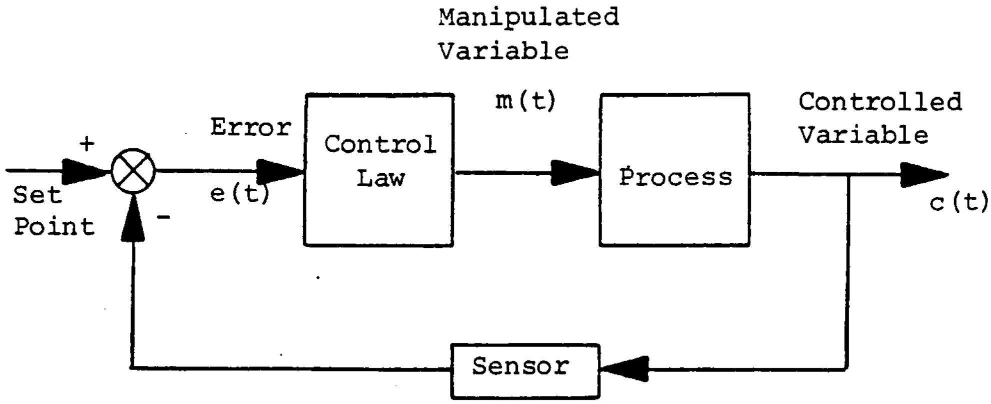
Figure 7 illustrates a control system with a single feedback loop. The controlled variable c(t)is detected by a sensor and then compared to the desired value to generate an error e(t). The controller generates a change in the manipulated variable, m(t), which is used as the input to the process so as to drive this error to zero.

A commonly used controller is the proportional-integral (P-I) form [20]. That is, the manipulated variable m(t) is related to the error e(t) by the equation

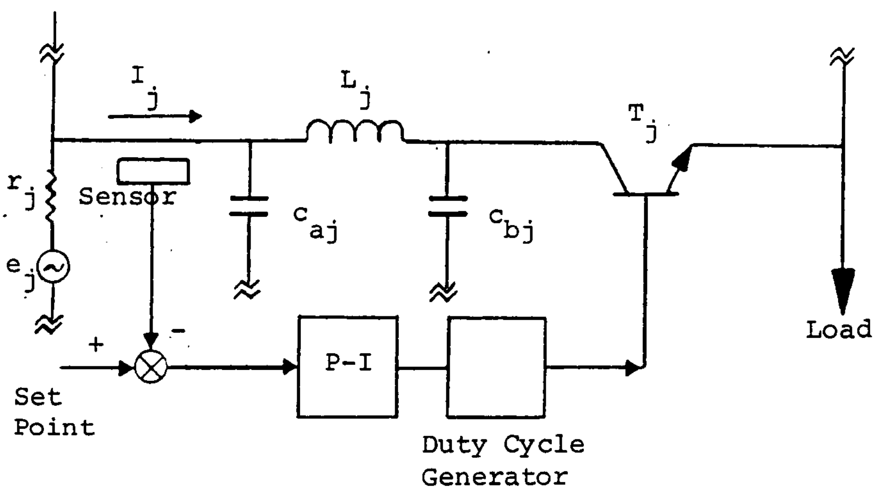
$$m(t) = K_1 e(t) + K_2 \int_0^t e(\tau) d\tau + m_R , \qquad (3.5)$$

where K_1 is the proportional gain, K_2 is the integral gain, and m_R is the reference value at which the control action is initialized.

The action of this controller in response to a change in the controlled variable is initially similar to that of a proportional controller (i.e., fast transient response). As the new equilibrium point is reached, the control action becomes the same as that of an integral controller; namely, no steady-state error. Thus, the P-I controller combines the desirable transient characteristics



(a) Schematic



(b) Switching PTO Control Circuit

Figure 7. Single-Loop Control System.

of a proportional controller and the steady-state characteristics of the integral controller [21].

The control circuit for one branch of the switching PTO is shown in Figure 7b. To obtain the desired current distribution within the channel, the average current flowing from the electrode is chosen to be the controlled variable. The error between the average electrode current and its corresponding set point is transmitted to the controller, which in turn determines the duty cycle of the switching transistor in that branch. Even though the transistor current and electrode current are not the same (Figure 7b) because of the presence of the LC filter, it is assumed that the switching transistor nearest the electrode affects that current most significantly. In addition, since feedback is used, the controller will search for a duty cycle that forces the electrode current to its set point.

The control action on the switches is limited by the structure of the switching PTO itself. Not all the switches can conduct the correct duty cycle determined by the controller. Consider the switching transistors in Figure 5, page 23; they are in either common-collector connection or common-emitter connection. Since a transistor conducts when it is forward biased, the switches in the PTO circuit cannot all turn on at the same time. When switch T_0 is ON, it lowers the voltage at the collector and, hence, turns off Switch T_1.

Because of this biasing effect, there is a sequential order for the switching transistors to conduct. In Figure 5, page 23, T_0 and T_5 turn on at the beginning of each period and turn off according to the duty cycle signal from the controller. Meanwhile, T_4 can be ON only when T_5 is not conducting, and so forth for the other transistors. Therefore, the duty cycle (ON time) of the inner switching transistors (e.g., T_1) as set by the controller must be longer than that of the outer transistors (e.g., T_0) in order to conduct at all. It is possible that the innermost transistors cannot be turned on when the outer transistors have 100% duty cycle. This deficiency reduces the ability of the controller to regulate the currents to their set points.

Although this controller may set the duty cycle to yield the desired average electrode current, the pulse loading by the switching transistors may have an adverse effect on the DCW channel. Therefore, continuous loading of the channel is desirable and is achieved by placing a suitable filter between the electrodes and the transistors.

III.3. Filter

An ideal filter would isolate the switches' pulsing effect from the electrodes completely. In the switching

PTO circuit shown in Figure 5b, page 23, a capacitor-input (LC-π) filter is inserted in each branch of the switching PTO.

The capacitors charge and discharge as required to prevent any significant change in voltage. The magnetic field of the inductor stores or releases energy as required in an effort to prevent changes in the magnitude of the current flowing through it [22]. The smoothing actions of capacitors and inductors are combined in the LC-π filter.

With the filter circuit, the electrode is supplying continuous current when the switch is either ON or OFF. Hence, there is a continuous load as seen from the electrode side and there is a voltage source (Capacitor C_{bj}) as seen from the transistor side. In general, the LC filter is selected so its cutoff frequency is well below the lowest frequency generated by the switching transistor.

When the assumptions in Section III.1 for the switching transistors are satisfied, the switching PTO circuit (Figure 5b) becomes a linear, periodically time-varying network. Stated another way, in each regime, ON or OFF, the network is linear and time-invariant. Thus, conventional analytical techniques for linear time-invariant systems apply. In Chapter IV these techniques will be used to analyze the switching PTO circuit and simulate its operation.

CHAPTER IV

SIMULATION OF A SWITCHING POWER TAKE-OFF CIRCUIT

Having discussed the basic principles of the switching PTO, an analytical description for a representative switching PTO circuit is developed to investigate its performance. Using this description, the dynamic behavior of the circuit is studied by means of a computer simulation. The results obtained from this simulation are then compared with those in Chapter II, where the behavior of a diode/resistor PTO scheme was examined.

Consider the controlled switching PTO circuit shown in Figure 5b, page 23. This PTO circuit is first analyzed assuming the controller is not operating; that is, each transistor has a fixed duty cycle. The control action is then added to complete the description.

Since a switching transistor's resistance is very low when it is ON (i.e., saturated) and very high when it is OFF (i.e., cut off), each transistor T_j (j=0 to 5) in Figure 5b can be replaced by a variable resistor R_j (j=0 to 5). These resistors have either very high or very low values, depending on the state of the transistors they simulate. For a set of fixed transistor duty cycles, an equivalent circuit for this switching PTO is shown in Figure 8. This is the circuit that will be used in the simulation of the switching PTO.

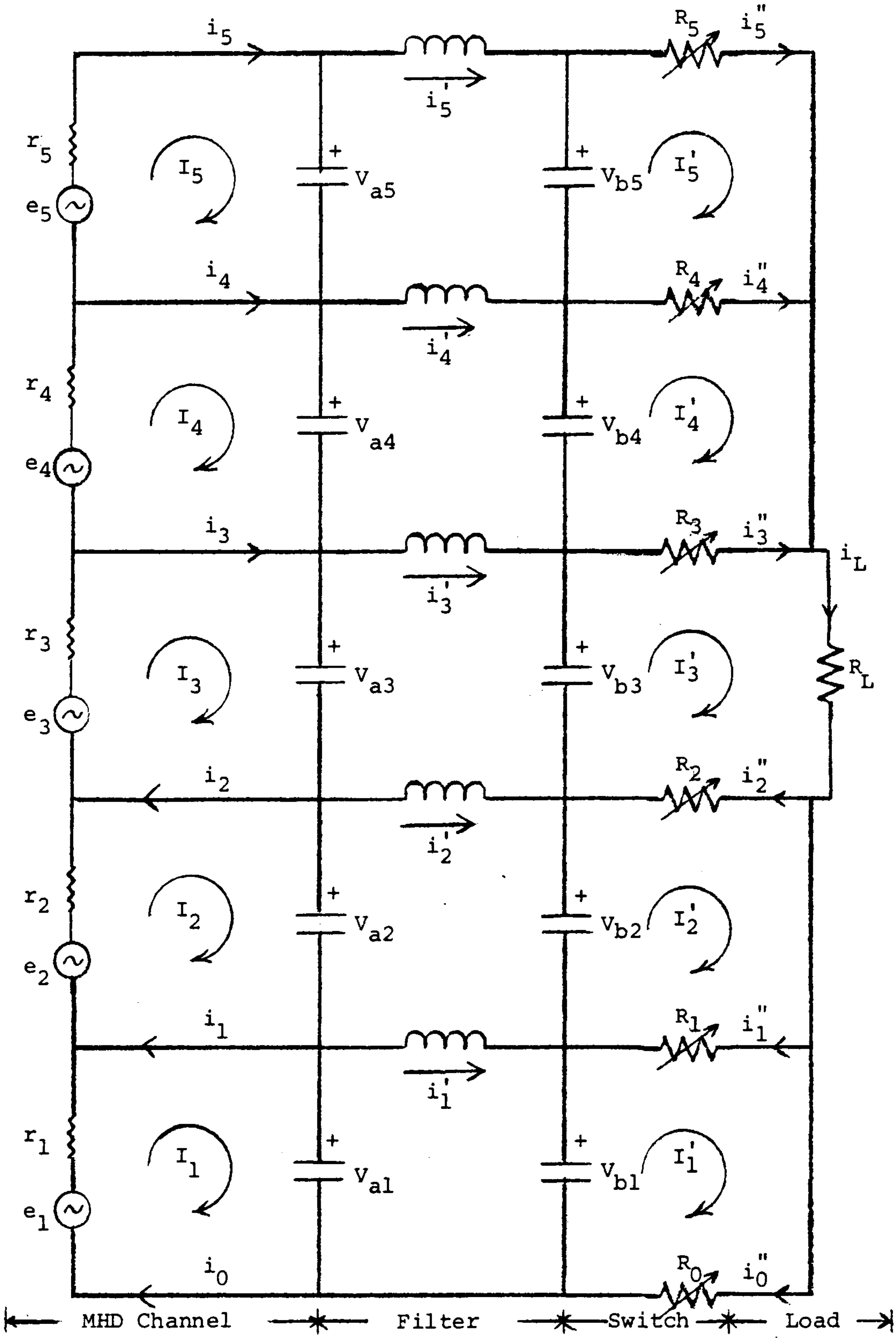


Figure 8. Equivalent Circuit for the Switching PTO Circuit.

Several computer software packages are available for simulating a physical system such as Figure 8. One of the most widely used is the Continuous System Modeling Program (CSMP), which was developed by International Business Machines (IBM) [23]. It is a computer program especially designed to allow users to simulate all types of physical systems with a minimum of programming difficulty.

The language of CSMP employes user-oriented statements for formulating numerically complicated mathematical operations such as integration and differentiation. To use this program most effectively, the PTO circuit in Figure 8 must be described in state-variable form. This is the case since CSMP is designed to integrate the resultant differential equations in a step-wise fashion with fixed time increments. Several special CSMP functions must also be used to simulate the operations that would be performed by an actual digital control system.

IV.1. Analytical Description

Since they correspond to the independent energy storage elements in a resistor-inductor-capacitor (RLC) network, the state variables for Figure 8 are chosen as the voltages across the capacitors and the currents through the inductors [24]. Hence, there are 15 state variables (i_j', V_{aj}, V_{bj}; j=1 to 5), producing a 15th-order differential system. This system is specified completely at any time t, provided the 15 independent states of the system are known at that time. Let these states be elements of the state vector $\underline{x}$, then the governing state equation must be found. It will have the form [25]

$$\dot{\underline{x}} = A\,\underline{x} + B\,\underline{u}\ , \tag{4.1}$$

where

$\underline{x}$: 15 x 1 state vector

A : 15 x 15 system matrix

$\underline{u}$: 5 x 1 input vector

B : 15 x 5 input matrix .

The elements of these matrices and vectors will now be determined. To find 15 independent equations for Eq. (4.1), a modified proper tree diagram for the circuit (Figure 8) is drawn in Figure 9 with all the tree branches containing only capacitive and resistive elements [24]. The required state equations are then obtained by writing voltage equations for the loops determined by the links of the modified proper tree diagram. All the elements of Eq. (4.1) can then be obtained as follows.

From Figures 8 and 9, Kirchhoff's voltage law written around Loops 1 to 5 yields the following equation:

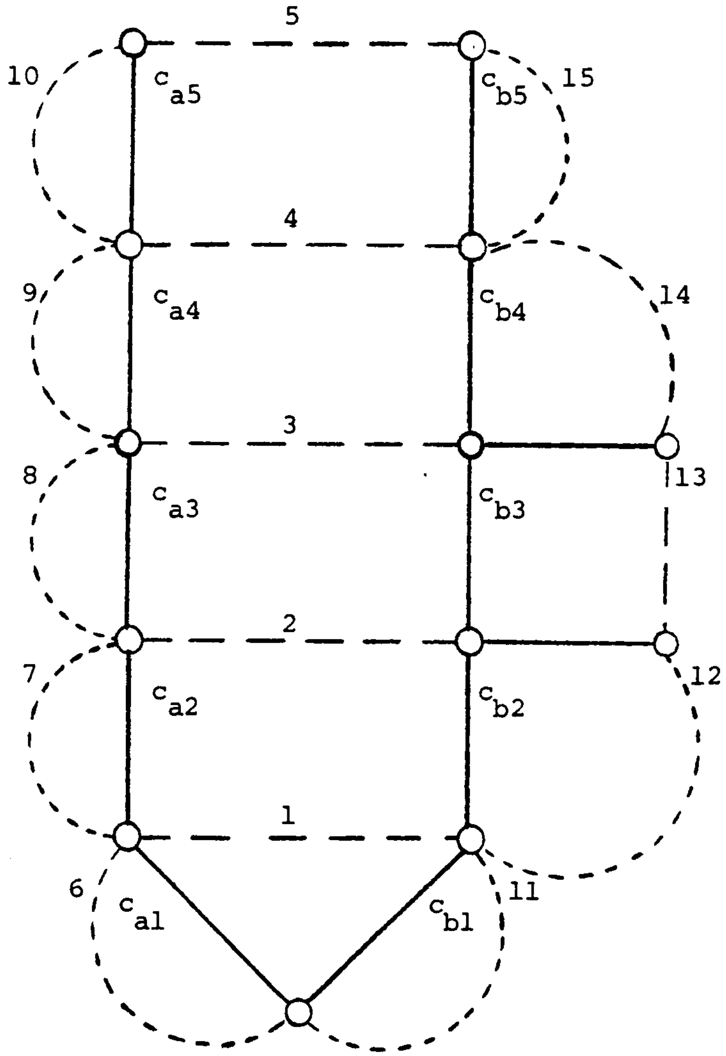


Figure 9. Modified Proper Tree Diagram for the Switching PTO Circuit.

$$\dot{\underline{I}} = G\,\underline{V_a} - G\,\underline{V_b}\ , \tag{4.2}$$

where

$$\underline{I} = \begin{bmatrix} i_1' \\ i_2' \\ i_3' \\ i_4' \\ i_5' \end{bmatrix};\ \underline{V_a} = \begin{bmatrix} V_{a1} \\ V_{a2} \\ V_{a3} \\ V_{a4} \\ V_{a5} \end{bmatrix};\ \underline{V_b} = \begin{bmatrix} V_{b1} \\ V_{b2} \\ V_{b3} \\ V_{b4} \\ V_{b5} \end{bmatrix} \tag{4.3}$$

and all inductors are assumed to be the same, g(H)

$$G = \frac{1}{g}\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix}. \tag{4.4}$$

Similarly, from Figure 8, page 33, and Figure 9, Kirchhoff's voltage law written around Loops 6 to 10 yields:

$$\dot{\underline{V_a}} = H\,\underline{I} - M\,\underline{V_a} + M\,\underline{u}\ , \tag{4.5}$$

where

$$\underline{u} = \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \\ e_5 \end{bmatrix}, \tag{4.6}$$

$$M = \frac{1}{c} \operatorname{diag} \left[\frac{1}{r_1}, \frac{1}{r_2}, \frac{1}{r_3}, \frac{1}{r_4}, \frac{1}{r_5} \right], \tag{4.7}$$

and

$$H = \frac{1}{c} \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}. \tag{4.8}$$

All capacitors are assumed to have the value c(F). The equation for the last five state variables can be obtained using Kirchhoff's voltage law around the five loops containing the capacitors C_{bj} (j=0 to 5) and the resistors R_j (j=0 to 5) in Figure 8, page 33, (i.e., Loops 11 to 15 in Figure 9):

$$\underline{\dot{V}_b} = N\ \underline{I} - Q\ \underline{V_b}, \tag{4.9}$$

where

$$N = \frac{1}{c} \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{4.10}$$

and

$$Q = \begin{bmatrix} R_6+R_5 & -R_5 & 0 & 0 & 0 \\ -R_5 & R_5+R_4 & -R_4 & 0 & 0 \\ 0 & -R_4 & R_4+R_3 & -R_3 & 0 \\ 0 & 0 & -R_3 & R_3+R_2 & -R_2 \\ 0 & 0 & 0 & -R_2 & R_2+R_1 \end{bmatrix}^{-1} . \quad (4.11)$$

As mentioned in the beginning of this chapter, the resistors R_j (j=0 to 5) represent the switching transistors T_j (j=0 to 5). Since the duty cycle of each switch governs its on/off time, the corresponding value of the resistor is also a function of time; that is, it is either very high or very low, depending on whether the switch is ON or OFF. Therefore, the matrix Q is a function of time, depending on the switch's duty cycle.

Combining Eqs. (4.2), (4.5), and (4.9), Eq. (4.1) (i.e., $\dot{\underline{x}} = A\,\underline{x} + B\,\underline{u}$) can be expressed for the circuit. The state vector is

$$\underline{x} = \begin{bmatrix} \underline{I} \\ \underline{V_a} \\ \underline{V_b} \end{bmatrix} , \quad (4.12)$$

while the input vector $\underline{u}$ is

$$\underline{u} = \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \\ e_5 \end{bmatrix} . \tag{4.13}$$

Finally, the system matrix is given by

$$A = \begin{bmatrix} O & G & -G \\ H & -M & O \\ N & O & -Q(t) \end{bmatrix} , \tag{4.14}$$

where each O is a 5x5 null matrix, and the input matrix is

$$B = \begin{bmatrix} O \\ M \\ O \end{bmatrix} . \tag{4.15}$$

With the expressions for A, B, $\underline{x}$, and $\underline{u}$ known, the dynamic behavior of the system can be obtained by solving Eq. (4.1) for the state vector $\underline{x}$. To complete the analysis of the controlled switching PTO, a suitable control algorithm must be used to determine Q(t).

A control algorithm, by which the manipulated variable (duty cycle in case of PTO circuit) is calculated from the set point and controlled variable, is necessary for a digital control system. The control algorithm of the P-I controller, as suggested in Section III.2, is the following discrete equivalent to Eq. (3.5) [20]:

$$m_n = K_1 e_n + K_3 \sum_{i=0}^{n} e_i + m_R ; \qquad (4.16)$$

m_n represents the value of the manipulated variable at the n^{th} sampling instant (i.e., the ON time τ_{ON} of the switch); e_n is the value of the error at the n^{th} sampling instant (i.e., $e_n = (i_{sp})_j - \langle i_j \rangle_n$); and j=0 to 5 in Figure 8, page 33. The gain constant K_3 is equal to K_2T; T is the sampling interval. Other parameters in Eq. (4.16) are defined as before. This equation is called the position form of the control algorithm, since it uses the actual value of the manipulated variable.

If Eq. (4.16) is written for m_{n-1} and subtracted from Eq. (4.16) as given above, the result is

$$\Delta m_n = m_n - m_{n-1} = K_1(e_n - e_{n-1}) + K_3 e_n . \qquad (4.17)$$

Equation (4.17) is called the velocity form of the control algorithm. The significant difference between Eqs. (4.16) and (4.17) is that Eq. (4.17) does not contain the term m_R. Hence, Eq. (4.17) is more convenient, since the computer does not need the initial reference value at each calculation. The term Δm_n is designated as the change in the switch's ON time ($\Delta\tau_{ON}$). The required ON time of the switch can be obtained by adding $\Delta\tau_{ON}$ to the required ON time at the previous sampling instant; that is,

$$(\tau_{ON})_n = (\tau_{ON})_{n-1} + (\Delta\tau_{ON})_n \cdot \qquad (4.18)$$

A block diagram for the closed loop control of this switching PTO system is shown in Figure 10. The average value of each electrode current i_j (j=0 to 5) in Figure 8, page 33, is compared to its corresponding set point. The error is then sent to the P-I controller for that branch, and the required change in the ON time of that switch is calculated. From the calculated ON time, the resistances R_j (j=0 to 5) shown in Figure 8 can be determined. Therefore, the control circuit varies the system matrix A (or specifically, Q in Eq. (4.11)) until each error settles to zero.

With this analytical description of the controlled switching PTO circuit, a computer simulation can be made. Section IV.2 presents a simulation for a controlled PTO system that directly replaces the diode/resistor system discussed in Chapter II. The result can be examined to determine the relative merits of the two PTO systems.

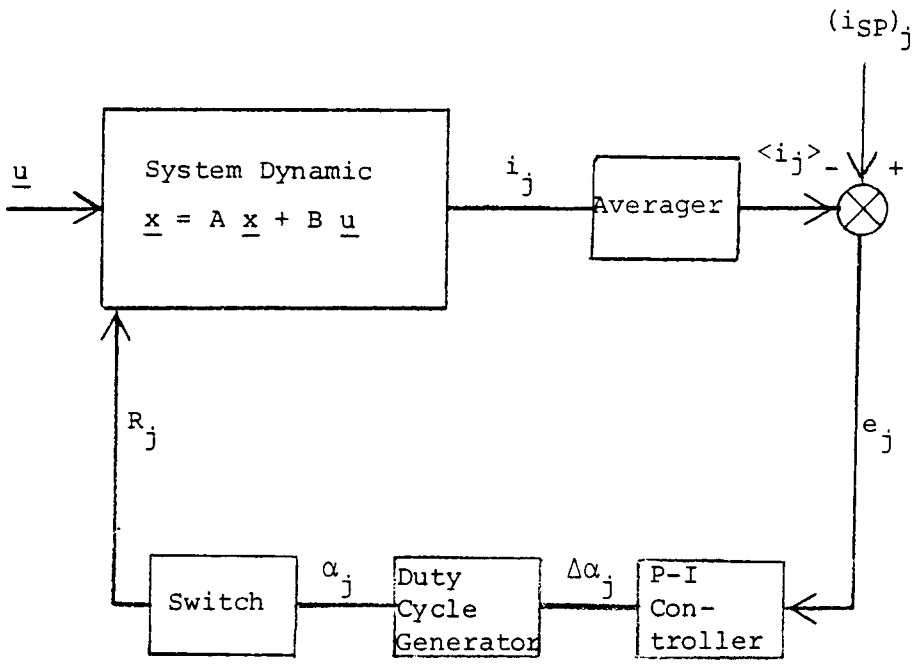


Figure 10. Block Diagram of General Control Scheme.

IV.2. Computer Simulation

In the computer simulation of the switching PTO circuit in Figure 8, page 33, the channel parameters used were the same as those used in the example of Chapter II (Table 1, page 16). The set points for the desired current distribution are listed on page 18. The frequency of the switches is chosen to be 500 Hz, the rate commonly used in switching regulators. All capacitors are 1,000 μF and all inductors are 1 mH, which provides satisfactory filtering for a 500-Hz switching frequency.

The resistance values chosen to simulate the on/off conditions are HR (1,000 ohm) for OFF state and LR (0.1 ohm) for ON state. Those represent typical values for switching transistors. Increasing the value of HR or decreasing the value of LR has little effect on the overall results. The values of the gain constants for the controllers are selected experimentally such that the average electrode current reaches a steady-state value. The proportional gain (K_1) is 1.0×10^{-8} (sec/amp) and the integral gain (K_3) is 5×10^{-8} (sec/amp).

Using the given parameters, the system matrix A and the input matrix B can be expressed as in Eqs. (4.14) and (4.15) where the matrices G, H, M, N are:

$$G = 1{,}000 \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix};$$

$$H = 1{,}000 \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix};$$

$$M = \begin{bmatrix} 333 & 0 & 0 & 0 & 0 \\ 0 & 297 & 0 & 0 & 0 \\ 0 & 0 & 38.6 & 0 & 0 \\ 0 & 0 & 0 & 325 & 0 \\ 0 & 0 & 0 & 0 & 199 \end{bmatrix};$$

$$N = 1{,}000 \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Hence, Eq. (4.1) becomes

$$\underline{\dot{x}} = \begin{bmatrix} O & G & -G \\ H & -M & O \\ N & O & -Q(t) \end{bmatrix} \underline{x} + \begin{bmatrix} O \\ M \\ O \end{bmatrix} \underline{u} , \qquad (4.19)$$

where Q(t) is determined by the control algorithm as follows.

The controlled variables i_j (j=0 to 5) can be obtained from the loop currents I_j (j=1 to 5), as shown in Figure 8, page 33; that is,

$$I_j = (V_{aj} - e_j)/r_j \tag{4.20}$$

and

$$\begin{aligned} i_5 &= I_5 \\ i_j &= I_j - I_{j+1} \quad j = 3,4 \\ i_j &= I_{j+1} - I_j \quad j = 1,2 \\ i_0 &= I_1 \ . \end{aligned} \tag{4.21}$$

Each electrode current i_j (j=0 to 5) is then averaged over one switching period (i.e., 2 mS). The error $(e_n)_j$ between the average of each electrode current and its set point is transmitted to the control algorithm (Eq. (4.17)). The required change in the ON time $\Delta\tau_{ON}$ for each switch is set by the following equation:

$$(\Delta\tau_{ON})_j = 1.0\mathrm{x}10^{-8}((e_n)_j - (e_{n-1})_j + 5(e_n)_j) \ ; \tag{4.22}$$

the actual ON time for the switch can then be calculated by adding the previous ON time to the change; that is,

$$(\tau_{ON})_j = (\tau'_{ON})_j + (\Delta\tau_{ON})_j \quad ; \quad j = 0 \text{ to } 5 , \qquad (4.23)$$

where $(\tau'_{ON})_j$ is the ON time at n-1th sampling instant for the jth switch, and $(\tau_{ON})_j$ is the ON time at nth sampling instant for the jth switch.

A digital control system would use Eq. (4.23) to set the duty cycle directly. However, in this simulation using CSMP, the variable duty cycle is generated by using the IMPULS and PULSE functions. IMPULS generates a periodic impulse at a specified frequency f. The function, IMPULS, is described below:

$$\text{TRIG} = \text{IMPULS (D,T)}$$
$$= \begin{cases} 0 \text{ for } t < D \\ 1 \text{ for } t = D + NT \quad ; \quad N = 0,1,2,\ldots \\ 0 \text{ for } t \neq D + NT , \end{cases} \qquad (4.24)$$

where D is the time when first pulse is applied and T is the period of the impulse; that is, T = 1/f.

Using the periodic pulse obtained from IMPULS, the desired duty cycle can then be generated by PULSE. The function, PULSE, is

$$\alpha = \text{PULSE}(P, \text{TRIG})$$

$$= \begin{cases} 1 \; ; & \text{for the time duration P following} \\ & \text{the application of TRIG} \\ 0 \; ; & \text{for all other time .} \end{cases} \qquad (4.25)$$

where P is the pulse width (i.e., τ_{ON}) and TRIG is the trigger starting each pulse.

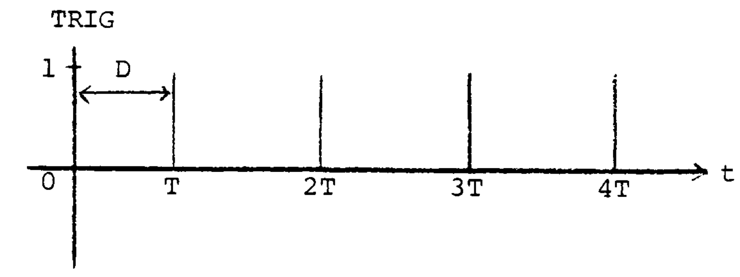
The entire procedure to generate a fixed duty cycle is shown in Figure 11. A periodic pulse train, obtained from IMPULS, is shown in Figure 11a. The function of PULSE is illustrated in Figure 11b. By combination, the duty cycle is obtained and the waveform is shown in Figure 11c. To use INSW to simulate the switch, the waveform described in Figure 11c must be shifted by -1/2, as shown in Figure 11d. The INSW function is used as

$$R_j = \text{INSW}(x1, HR, LR)$$

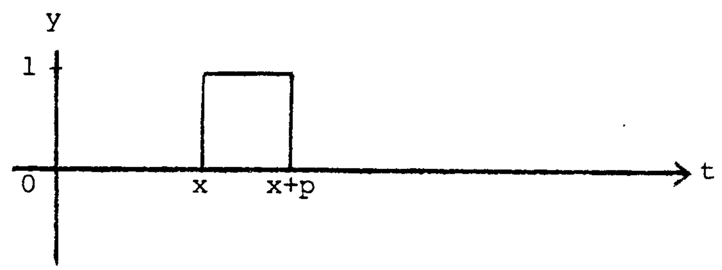
$$= \begin{cases} HR \; ; & x1 < 0 \\ LR \; ; & x1 \geq 0 \; , \end{cases} \qquad (4.26)$$

where HR and LR represent the high and low resistance values for the switching transistors; x1 is set equal to the shifted duty cycle generated by PULSE (i.e., Figure 11d).

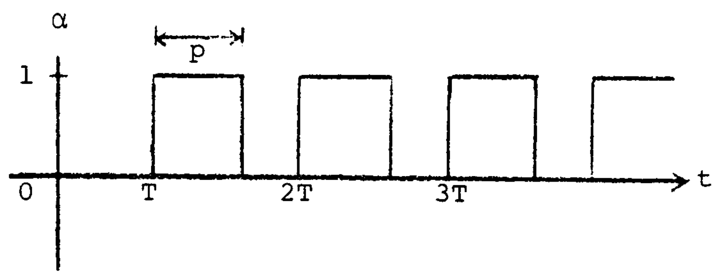
Using the given switching frequency and the ON time calculated from the control algorithm, the required duty cycle is generated by



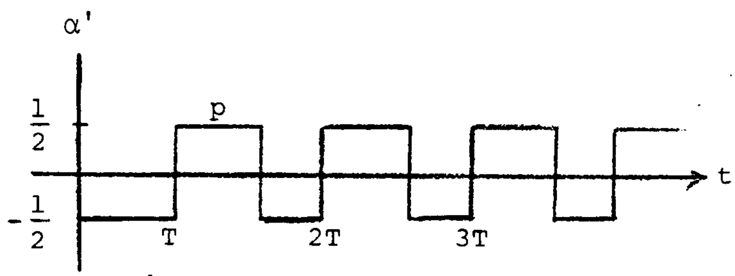
(a) TRIG = IMPULS (D,T)



(b) y = PULSE (P,x)



(c) α = PULSE (P,TRIG)



(d) $\alpha' = \alpha - 1/2$

Figure 11. Generation of Duty Cycle via CSMP.

$$\text{TRIG} = \text{IMPULS}(0.0,\ 2\text{mS}) \ , \tag{4.27}$$

$$\alpha = \text{PULSE}((\tau_{ON})_j,\ \text{TRIG}) \ . \tag{4.28}$$

The resistors R_j (j=0 to 5) are obtained from

$$R_j = \text{INSW}(\alpha - \frac{1}{2},\ 1{,}000,\ 0.1) \ . \tag{4.29}$$

Finally, the biasing effect of the switching transistors is simulated by requiring

$$I_3' \geq I_4' \geq I_5' \geq 0$$

and (4.30)

$$I_3' \geq I_2' \geq I_1' \geq 0 \ ,$$

where I_j' (j=1 to 5) are shown in Figure 8, page 33. This can be done by using LIMIT in CSMP; that is,

$$I_j' = \text{LIMIT}(0.0,\ \text{P1},\ I_j') \quad ; \quad j = 1,2,4,5$$

$$= \begin{cases} 0 & ; \quad \text{for } I_j' < 0 \\ \text{P1} & ; \quad \text{for } I_j' > \text{P1} \\ I_j' & ; \quad \text{for } 0 \leq I_j \leq \text{P1} \end{cases} \ , \tag{4.31}$$

where

$$\text{P1} = \begin{cases} I_{j-1}' & ; \quad j = 4,5 \\ I_{j+1}' & ; \quad j = 1,2 \end{cases}$$

is the upper limit for I_j'.

Assuming that initially there is no voltage across the capacitors and no current through the inductors, the dynamic behavior of the switching PTO circuit is obtained by solving the state equation (Eq. (4.19)) for $\underline{x}$. This is done in CSMP by integrating $\dot{\underline{x}}$. For example,

$$V_{aj} = \text{INTGRL}(0.0,\ \dot{V}_{aj})$$

$$V_{bj} = \text{INTGRL}(0.0,\ \dot{V}_{bj})\quad, \qquad (4.32)$$

$$i_j' = \text{INTGRL}(0.0,\ \dot{i}_j')$$

where j=1 to 5 and INTGRL is the integration function in CSMP with initial conditions 0.0. The fourth-order Runge-Kutta method with fixed integration interval (0.1 msec) is used in the simulation program. The complete simulation is listed in the Appendix; the results are analyzed in Chapter V.

CHAPTER V

SIMULATION RESULTS

The preceding chapter describes the simulation program for the switching PTO circuit pictured in Figure 8, page 33. Although the simulation was made for a simplified switching PTO circuit, it can be generalized to any switching PTO system. The program does provide useful results for a preliminary study of the switching PTO system.

The purpose of this chapter is to study the current regulation and power loss of the switching PTO circuit. Attention is focused on the variation of electrode currents i_j (j=0 to 5) and the power dissipated in the switching transistors T_j (j=0 to 5), as well as the load R_L. The biasing effect, which is a special characteristic of the switching PTO circuit, is also studied.

To compare the switching PTO circuit to the diode/resistor PTO analyzed in Chapter II, the parameters used for the DCW channel and the load are chosen to be the same. The characteristics of the filter circuit, control algorithm, and the simulated switching transistors are given in Section IV.2. The simulation program was run assuming all the initial conditions were zero. Results obtained are analyzed in the following sections.

V.1. Power Dissipation Under Steady-State

Since the capacitors are not initially charged, it takes about 0.15 second to accomplish this. To allow for the charging of the capacitors, the switches are set to 50% duty cycle at t=0. The controllers are applied at t=0.15 second to regulate the average electrode currents at their set points. The required duty cycle for each switch is calculated by the control algorithm given in Eq. (4.22). The variation of the load current is obtained and plotted from 0 to 0.4 second in Figure 12. The load current reaches steady-state around 0.2 second. A more detailed picture of the load current in steady-state is given in Figure 13, which shows the waveform during five switching periods. The average load current in steady state is found to be 124 amp.

Because of the biasing of the transistors, only the outermost switches (T_0 and T_5) are actually conducting at 50% duty cycle during the capacitors' charging period. At the same time, the channel currents I_j (j=1 to 5) in Figure 8, page 33 , increase to charge the capacitors. Hence, the voltage at the diffuser is increased. This results in an overshoot of the load current. A peak value of 145 amp at 0.02 second is observed in Figure 12. When the controllers are activated, they bring the load current to its desired value.

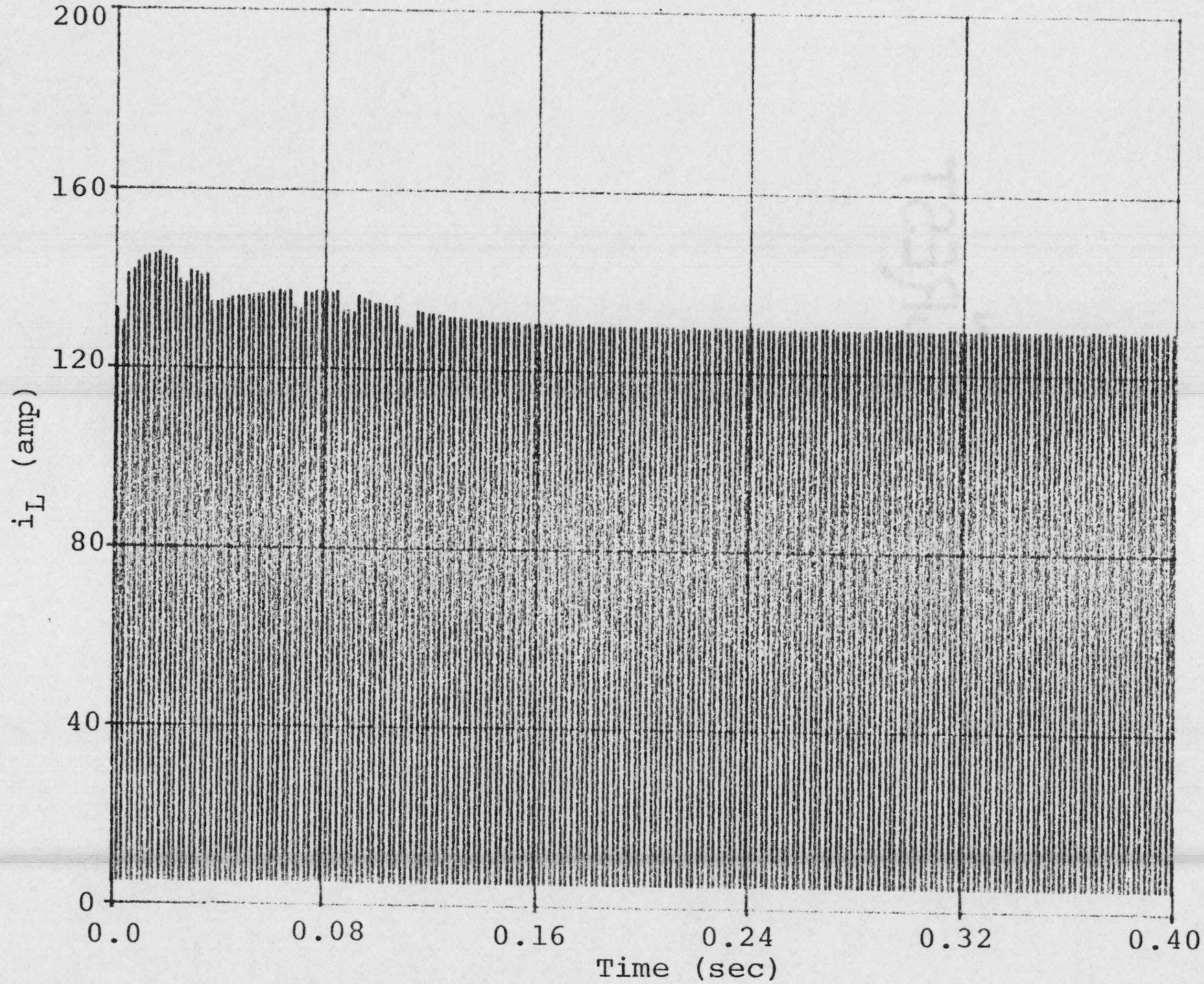


Figure 12. Variation of Load Current under Designed Conditions.

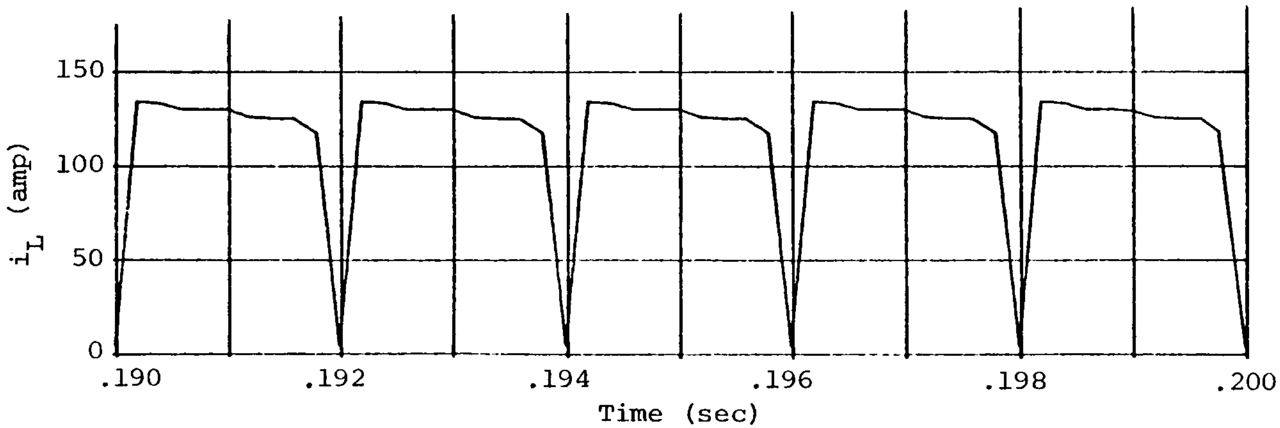


Figure 13. Load Current under Steady-State Conditions.

The overall power performance of the switching PTO circuit in steady-state was calculated and is listed in Table 4. The power dissipated in the switching transistors P_D can be obtained by calculating the difference between the total average power from the channel P_T and the power delivered to the load P_L (i.e., $P_D = P_T - P_L$), where P_T is obtained by summing the average power output from each pair of electrodes. It can be described as

$$P_T = \sum_{j=1}^{5} \langle P_j \rangle$$

$$= \sum_{j=1}^{5} \left(e_j \, I_{(rms)_j} - I^2_{(rms)_j} \, r_j \right) . \qquad (5.1)$$

A comparison of the diode/resistor PTO and the switching PTO is given in Table 5. The power loss in the diode/resistor PTO circuit is about 15% of the total power available to the load from the DCW channel. For the switching PTO, power loss in the PTO circuit itself is only 2.2%. These results are as expected from the discussion in Section III.1.

V.2. Current Regulation

To test the current regulation of the switching PTO, a change ($\pm$10%) in the normal generator voltage was made at t=0.4 second. Figures 14 and 15 show the variation

Table 4. Overall Power Performance for the Switching PTO Circuit

j	e_j (V)	$I_{(rms)j}$ (amp)	r_j (ohm)	$\langle P_j \rangle$ (watt)
1	187	32.98	3.0	2,904
2	730	109.53	3.36	39,648
3	6,090	117.4	25.91	357,850
4	410	68.72	3.07	13,677
5	54.3	7.11	5.03	131.67
			Total P_T	414,210.87

Power Output to Load

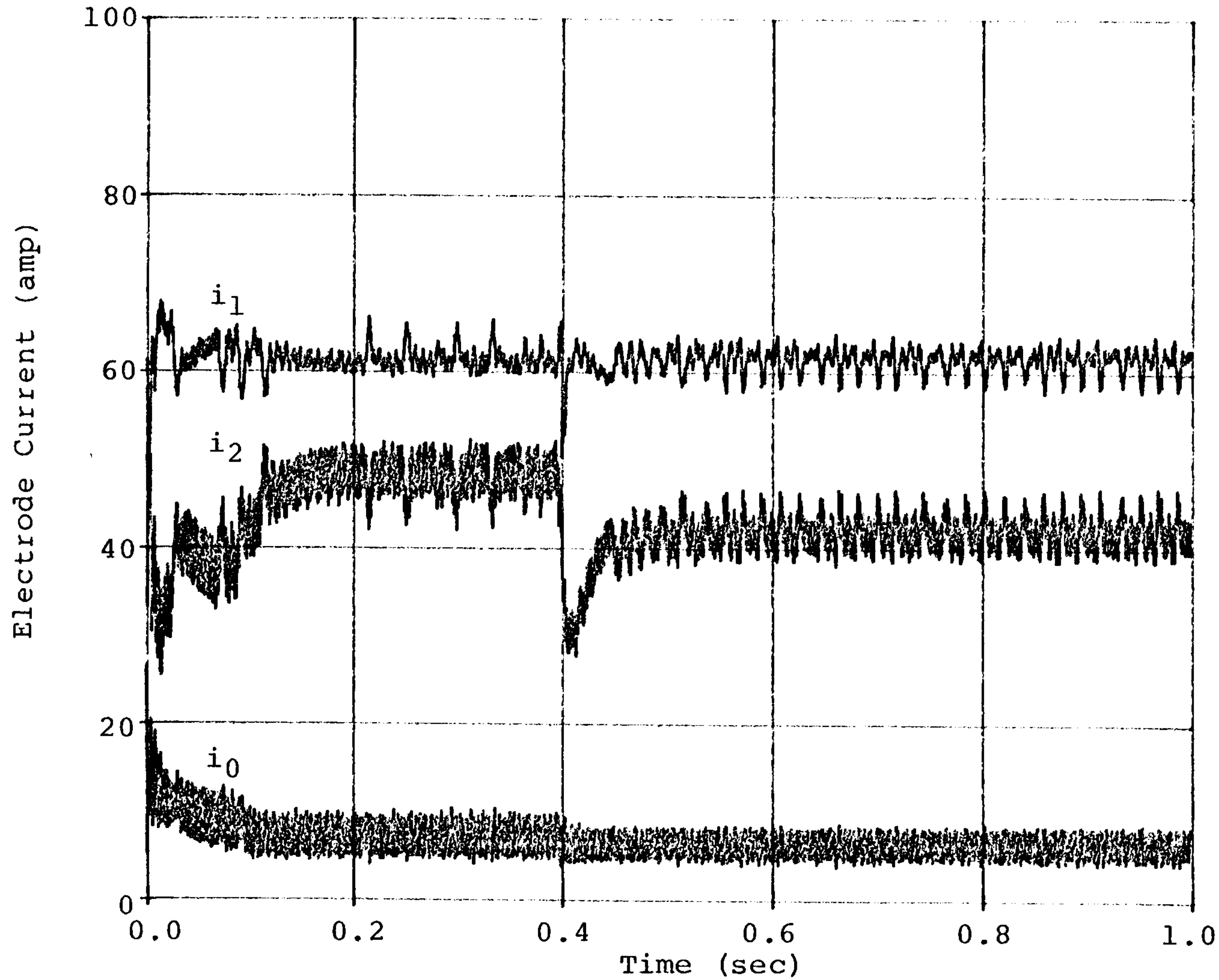
$P_l = I^2_{L(rms)} \times R_L = 40{,}5060$

Power Loss in PTO

$P_D = P_T - P_L = 9{,}150.87$

Table 5. Comparison of Power Performance of Switching and Diode/Resistor PTO

	D/R PTO	Switching PTO
Total Power from DCW Channel (watt)	414,112.93	414,210.87
Power Output to Load (watt)	352,455.45	405,060
Power Loss in PTO (watt)	61,657.47	9,150.87
Percentage of Power Loss	15	2.2



(a)

Figure 14. Variation of Instantaneous Electrode Current under 10% Decrease of Voltage at 0.4 sec.

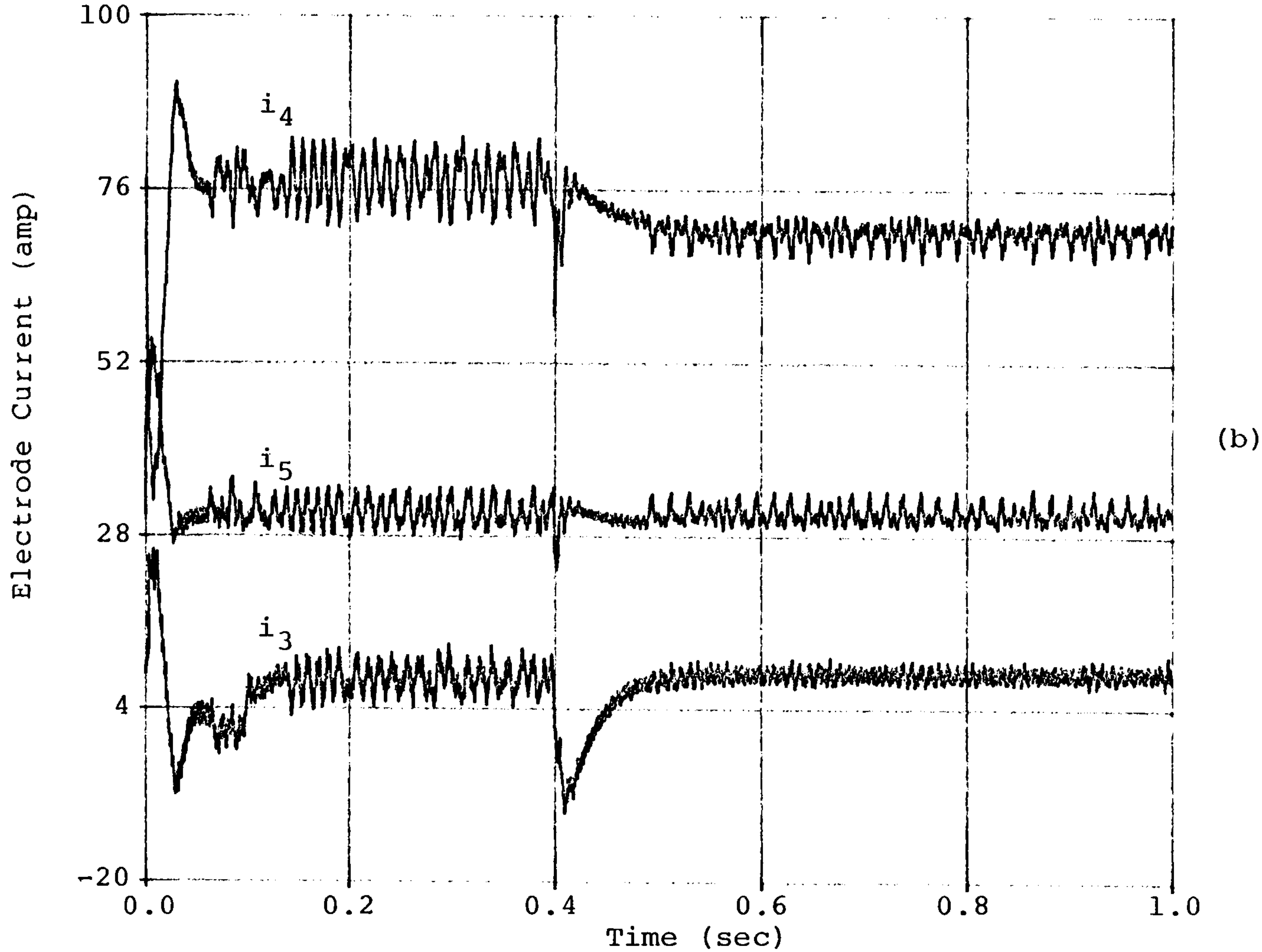
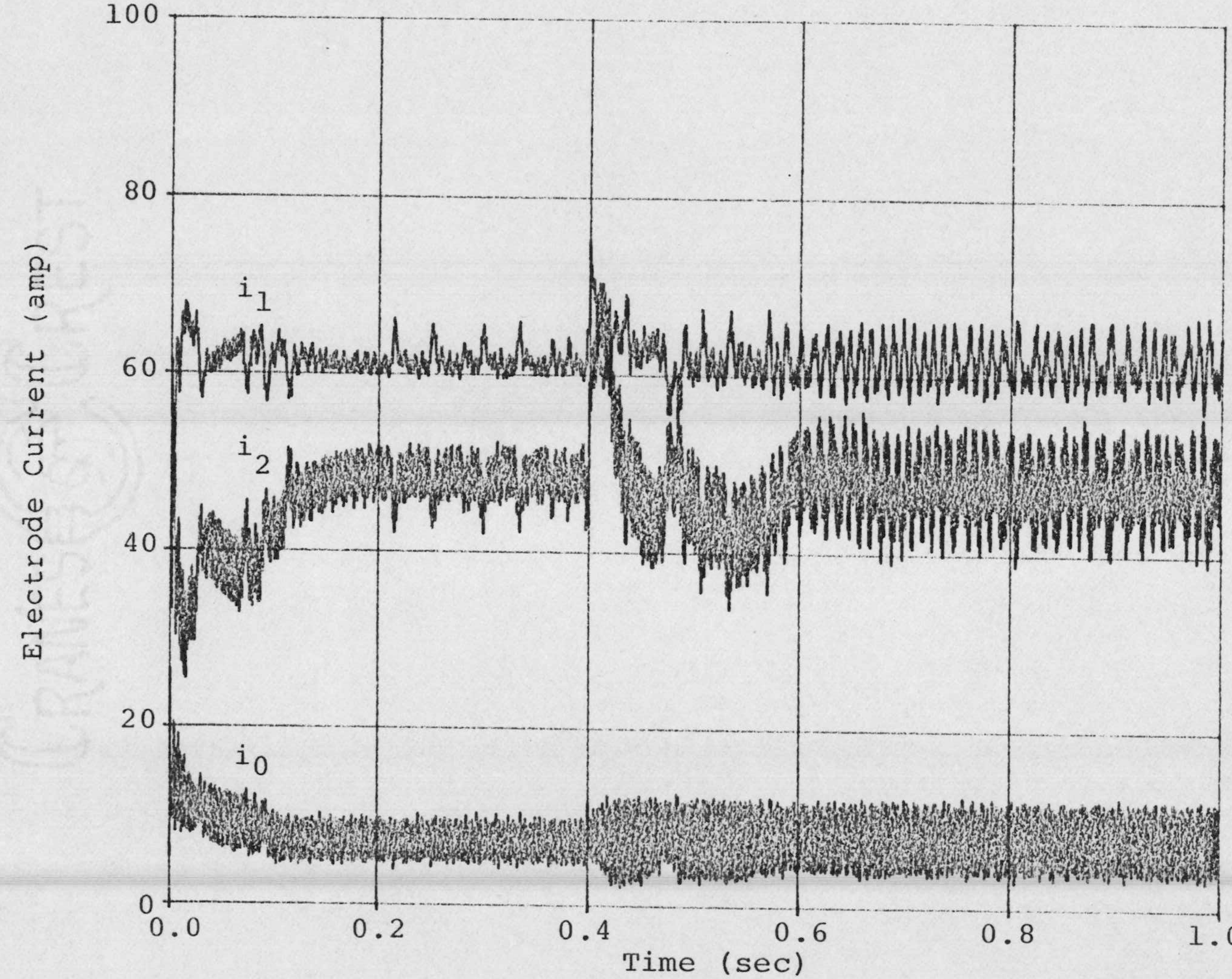


Figure 14. (continued)



(a)

Figure 15. Variation of Instantaneous Electrode Current under 10% Increase of Voltage at 0.4 sec.

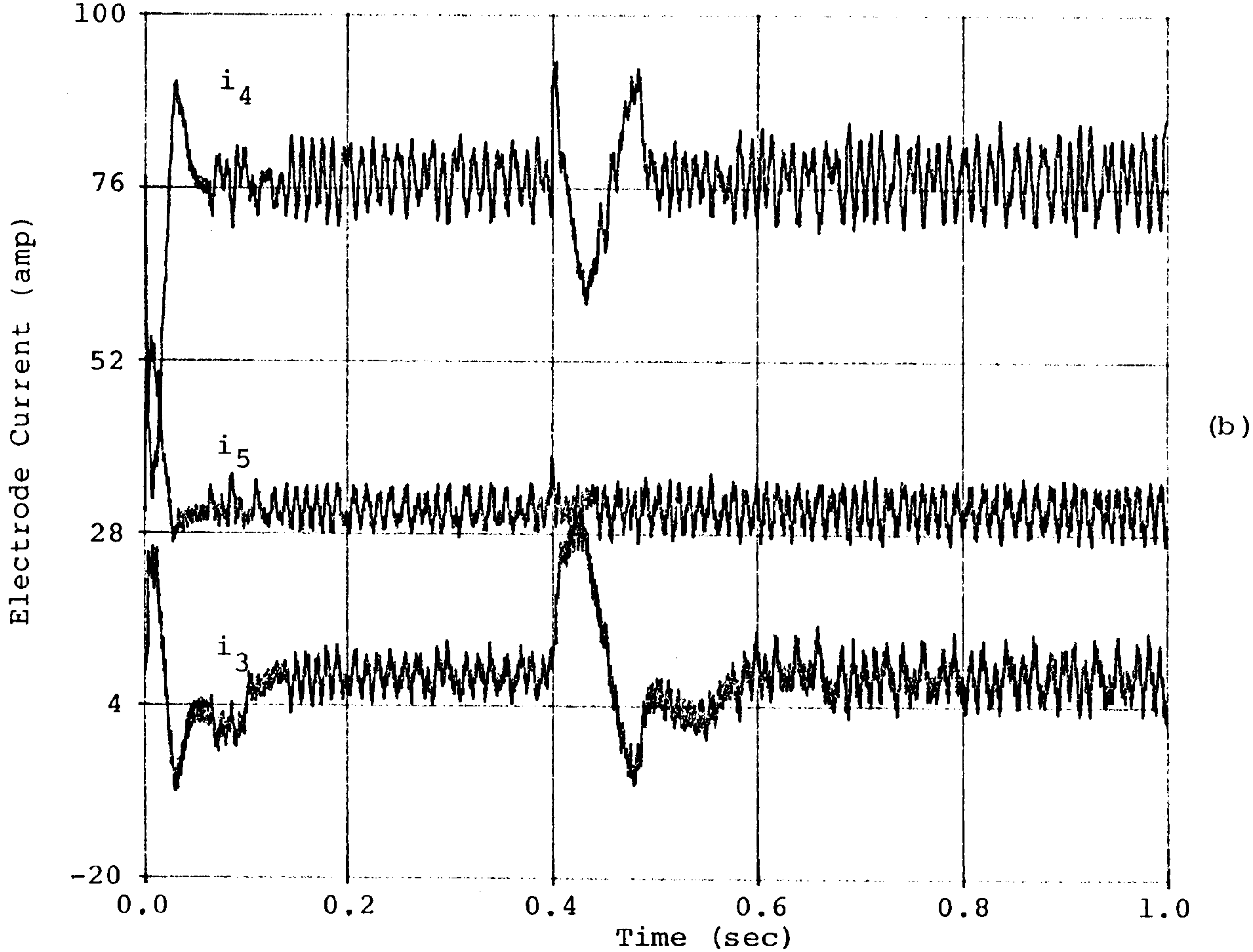


Figure 15. (continued)

of the instantaneous electrode current i_j (j=0 to 5) with time. The steady-state average electrode current is listed in Table 6. Since the average electrode current is controlled by the transistor's duty cycle, its change is not proportional to the change in the channel voltages. As seen in Figure 14, page 59, the switching PTO has difficulty bringing the electrode current back to the set points when the channel voltages are decreased by 10%.

A comparison of the current regulation by the switching PTO and the diode/resistor PTO is given in Table 7. For the diode/resistor system, a 10% increase or decrease of the channel voltages results in a similar 10% change of the electrode current. For the switching PTO system, the variation of the average electrode current due to a 10% increase of channel voltage is considerably less than 10%. However, for a 10% decrease of channel voltages, the percentage error of the innermost electrode currents i_2 and i_3 are greater than 10%. This is due to the biasing effect of the transistors, as discussed in Section III.2. Transistors T_2 and T_3 are not able to conduct sufficiently long to produce the desired current even though the controller signals them to do so. This is examined more carefully in Section V.3.

Table 6. Variation of Average Electrode Currents (Switching PTO)

Current	Set Point	Average Value of Electrode Current: Normal Generator Voltage	Normal Voltage (-10%)	Normal Voltage (+10%)
$\langle i_5 \rangle$	31.2	30.2	29.5	32.4
$\langle i_4 \rangle$	77.46	75.7	71.3	80.0
$\langle i_3 \rangle$	8.86	9.1	6.8	9.5
$\langle i_2 \rangle$	50.58	51.3	43.3	51.6
$\langle i_1 \rangle$	61.55	60.3	61	63.4
$\langle i_0 \rangle$	5.4	5.5	5.2	5.8

Note: All values are currents in amperes.

Table 7. Comparison of Current Regulation between D/R PTO and Switching PTO

	Error of Electrode Currents (percent)					
	D/R PTO			Switching PTO		
Current	Designed Voltage	Designed Voltage (+10%)	Designed Voltage (-10%)	Designed Voltage	Designed Voltage (+10%)	Designed Voltage (-10%)
i_5	0	10	-10	3.2	3.8	-5.4
i_4	0	10	-10	2.3	3.3	-9.6
i_3	0	10	-10	2.7	7.2	-12
i_2	0	10	-10	1.4	2	-11
i_1	0	10	-10	2	3	-0.2
i_0	0	10	-10	1.9	7.4	-3.7

V.3. Biasing Effect

The biasing effect of the switching transistors can be verified by observing the currents flowing through the switch; that is, i_j'' (j=0 to 5). Figures 16 and 17 show the i_j'''s from t=0.192 to 0.2 second (i.e., four switching periods). By this time, the system has reached steady-state conditions. The corresponding load current i_L during that period would be the sum of the three switch currents.

At the beginning of every period, i_0'' and i_5'' start to rise and are followed by i_1'' and i_4''; i_3'' is the last to rise to its complete ON value. Ideally, there would be no two currents conducting at the same time in either Figure 16 or 17; however, there is overlap between two waveforms because the switching transistors are simulated by resistors of 1,000 ohm or 0.1 ohm. When the voltage across the 0.1-ohm resistor becomes sufficiently large, it can forward-bias the simulated switch next to it.

The performance of the switching transistors at steady-state condition is summarized in Table 8. Because of the biasing effect, only T_0 and T_5 conduct exactly the corresponding on-time calculated by the controller; T_4 conducts at the difference of the on-time of Switch 4 and Switch 5. This applies to the rest of the switches, as expected. Since the actual on-time of Switch 2 is less

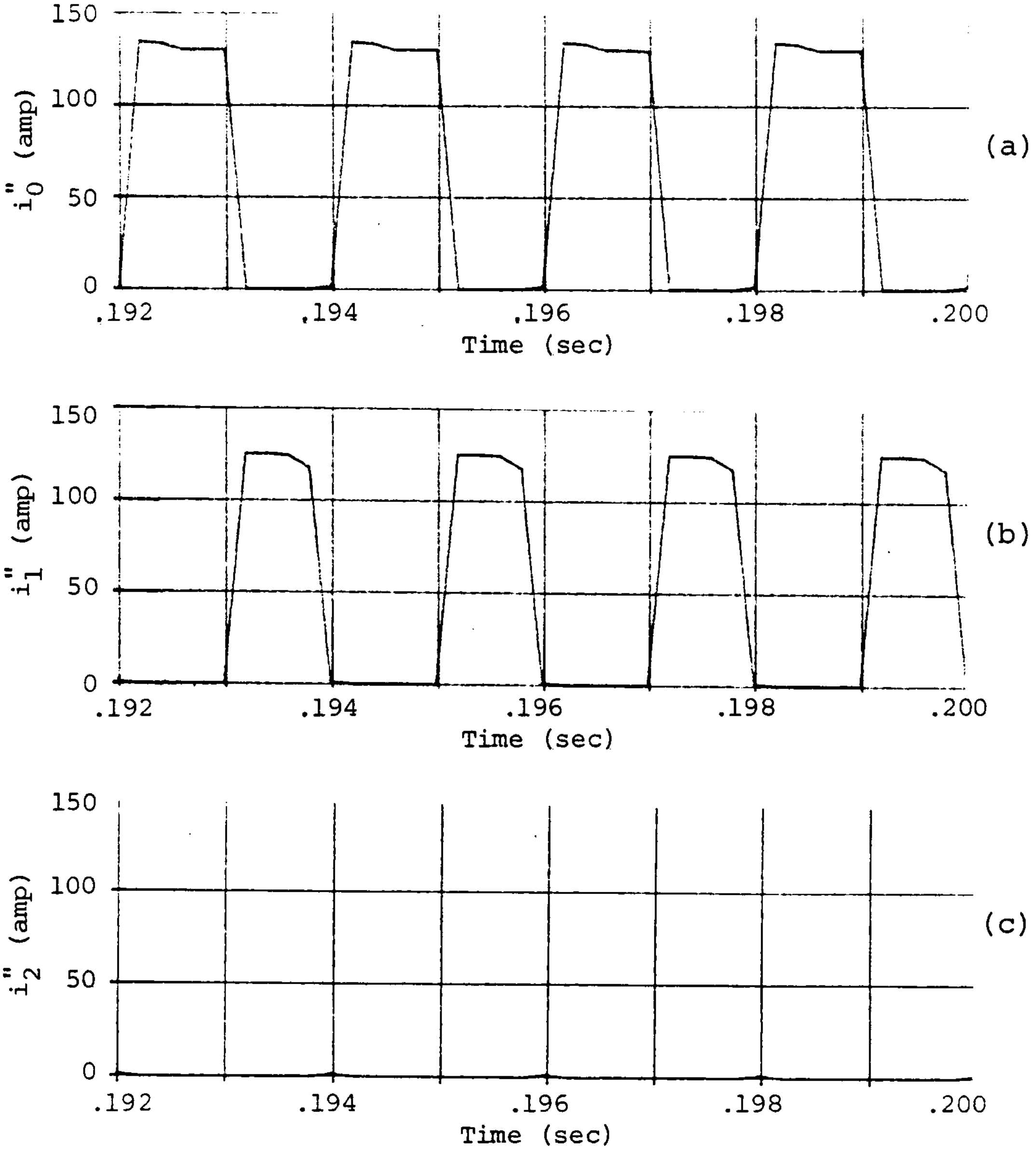


Figure 16. Transistor Currents under Steady-State Conditions (i_0'', i_1'', i_2'').

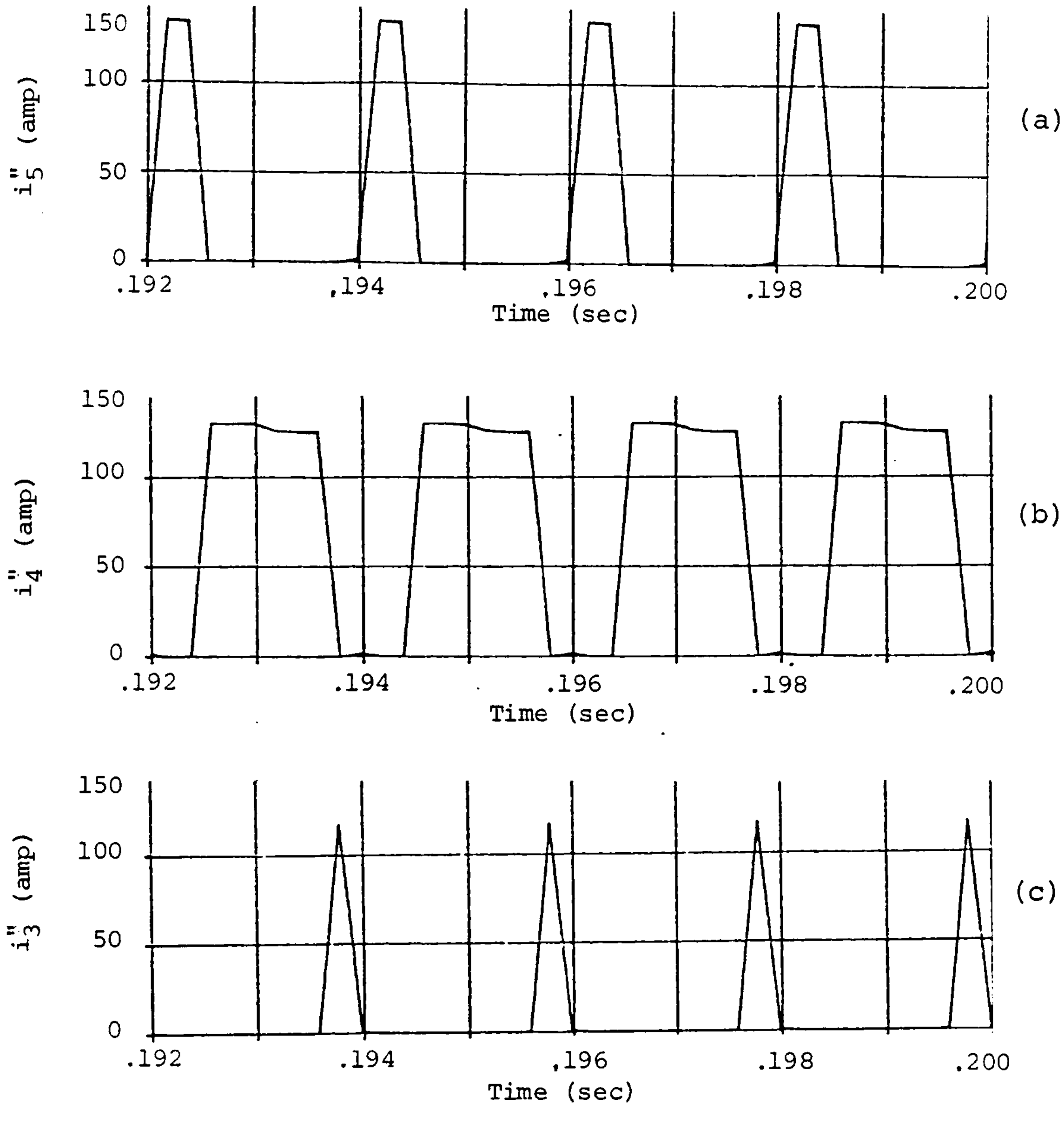


Figure 17. Transistor Currents under Steady-State Conditions (i_5'', i_4'', i_3'').

Table 8. Performance of Switching Transistors at Steady-State Conditions

Transistor	T_{ON} from Controller (sec)	Actual T_{ON} (sec)	Actual Duty Cycle (%)
T_5	$6.2x10^{-4}$	$6.2x10^{-4}$	31
T_4	$1.76x10^{-3}$	$1.14x10^{-3}$	57.1
T_3	$2x10^{-3}$	$2.4x10^{-4}$	12
T_2	$2x10^{-3}$	0	0
T_1	$1.9x10^{-3}$	$0.73x10^{-3}$	36.5
T_0	$1.17x10^{-3}$	$1.17x10^{-3}$	58.6

Note: Normal voltage conditions.

than the integration interval, which is the smallest value CSMP can distinguish, i_2'' is zero all the time.

In this chapter, the performance of the switching PTO circuit was studied and compared to the diode/resistor PTO. As expected, the power loss in the switching PTO circuit is significantly less than that in the diode/resistor PTO circuit. In handling changes in channel voltages, the switching PTO seems quite able to regulate desired currents for an increase in generator voltages. However, due to the biasing effect of the transistor, the switching PTO has trouble coping with a significant decrease in channel voltages. It should be noted, however, that currents are regulated to a point less than their desired values.

CHAPTER VI

CONCLUSIONS AND RECOMMENDATIONS

To extract useful electrical power from the DCW channel, it is necessary to use an efficient PTO mechanism. This PTO mechanism should be able to maintain the electrode current output at the desired value and consume as little power as possible, while consolidating different electrode voltages to a single load. A PTO which uses switching transistors and exhibits these desirable properties was recently proposed as a replacement for the conventional diode/resistor PTO circuit.

A direct comparison of the switching PTO and the diode/resistor PTO is presented in this study. To facilitate the analysis of the problem, only a simple representative model was considered. The six-electrode model provides the information needed to estimate the performance of the system. This model could easily be enlarged for a detailed evaluation of a more complex PTO circuit.

Compared with the diode/resistor PTO system, the power dissipated in the switching PTO is quite small. The diode/resistor PTO dissipated 15% of the total power output from the given DCW channel, while the switching PTO dissipated only 2.2%. Hence, a much larger portion of the available power is delivered to the load when a switching PTO is used.

Under normal circumstances, the switching PTO investigated has the ability to bring the electrode currents back near their nominal values when channel conditions vary. Because of the structure of the switching PTO circuit itself, it cannot regulate the electrode currents when the channel voltage decreases a large amount. The switching PTO exhibits very good electrode current regulation when channel voltages increase, while the diode/resistor PTO provides no control over the electrode currents under any channel variation.

The comparison presented here indicates that it is quite feasible to replace the diode/resistor PTO by the controlled switching transistor technique. The actual performance of the switching PTO should be improved after further study is completed with both the computer simulation and the hardware implementation of such a circuit.

An actual DCW channel may have hundreds of electrodes. In consolidating electrode voltages from such a channel, the transistor biasing problem needs to be minimized. One possible method is to use several PTO circuits, each of which consolidates six to ten electrode voltages. A single load is then obtained by collecting the load current from individual PTO circuits.

The biasing problem with the transistor may also be alleviated by reducing the set points for the electrode currents, even though maximum power output would then not be obtained. These alternate set points must be chosen such that the switching PTO can provide regulation when the channel voltages vary within a certain range (e.g., $\pm$10%); sufficient time must be allowed for the innermost switches to conduct. Hence, the deficiency in handling a decrease in channel voltage can be overcome by designing the controller for minimum channel voltages and maximum electrode current set points.

To improve the control of the average electrode current, the controller could be designed to average over a longer time period. Instead of averaging the electrode current over only one switching period, an average over 10 or more switching periods could be used. In this case, the controller would have a longer term effect on the electrode current and a smoother instantaneous electrode current would result.

BIBLIOGRAPHY

BIBLIOGRAPHY

1. Chapman, J. N., et al. "MHD Steam Power--Promise, Progress, and Problems," Mechanical Engineering, 30-37, September 1981.

2. Evaluation of Phase 2 Conceptual Designs and Implementation Assessment Resulting from the Energy Conversion Alternatives Study. NASA TM X-73515. Cleveland, Ohio: National Aeronautics and Space Administration, 1977.

3. Pepper, J. W. "Effect of Nitric Oxide Control on MHD-Steam Power Plant Economics and Performance," Institute for Plasma Research Report No. 614, Stanford University, Stanford, California, December 1974.

4. Chapman, J. N. "On the Economic Optimization of the MHD-Steam Power Plant." Ph.D. dissertation, The University of Tennessee, Knoxville, 1977.

5. Agarwal, Anant. "On Modeling and Control of MHD-Steam System." Unpublished Master's thesis, The University of Tennessee, Knoxville, 1980.

6. Pan, Y. C., and E. D. Doss. "Power Take-Off Analysis for Diagonally Connected MHD Channels." Paper AIAA-80-0253 presented at the American Institute of Aeronautics and Astronautics Eighteenth Aerospace Sciences Meeting, Pasadena, California, January 14-16, 1980.

7. Fowler, Riley. "A Survey of Power Conditioning and Consolidation Methods Utilized for MHD Generators." Paper No. 1F9 presented at the 1981 Institute of Electrical and Electronic Engineers International Conference on Plasma Science, Santa Fe, New Mexico, May 18-20, 1981.

8. De Montardy, A. "MHD Generators with Series-Connected Electrodes." Paper No. 9 presented at the International Symposium on MHD Electrical Power Generation, New Castle-Upon-Tyne, England, September 6-8, 1962.

9. Dicks, J. B. "Design and Operation of Open Cycle Hall Current Neutralized MHD Accelerators and Generators with Diagonal Conducting Strip Walls." Paper presented at the Fifth Symposium on Engineering Aspects of MHD, Massachusetts Institute of Technology, Cambridge, Massachusetts, April 1-2, 1964.

10. Dicks, J. B., et al. "Characteristics of a Family of Diagonal Conducting Wall MHD Generators." Paper presented at the Eighth Symposium on Energy--Aspects of MHD, Stanford, California, March 28-30, 1967.

11. Dicks, J. B., et al. "Theoretical and Experimental Studies of Two-Terminal MHD Generators." Paper presented at the Fourth International Conference on MHD Electrical Power Generation, Warsaw, Poland, July 24-30, 1968.

12. Walsh, Edward M. Energy Conversion. New York: The Ronald Press, 1967.

13. Dicks, J. B., et al. "Diagonal Conducting Wall Generators," Air Force Aeropropulsion Laboratory Report AFAPL-TR-67-25, Wright-Patterson Air Force Base, Ohio, 1967.

14. Wu, Y. C. L. "Performance Theory of Diagonal Conducting Wall Generators," AIAA Journal, 14(No. 10): 1362-1368, October 1976.

15. Galanga, F. L., et al. "Experimental Results of the UTSI Coal-Fired MHD Generator and Investigations of Various Power Take-Off Schemes." Paper presented at the American Institute of Aeronautics and Astronautics Nineteenth Aerospace Sciences Meeting, St. Louis, Missouri, January 12-15, 1981.

16. Wu, Y. C. L. "Design 3: Numerical Solution Program," Computer Program, The University of Tennessee Space Institute, Tullahoma, Tennessee, 1980.

17. Comer, David J. Modern Electronic Circuit Design. Reading, Massachusetts: Addison-Wesley, 1968.

18. Kuo, Franklin F. Network Analysis and Synthesis. New York: John Wiley and Sons, Inc., 1962.

19. Temes, Tabor C., and Sanjit K. Mitra (eds.). Modern Filter Theory and Design. New York: John Wiley and Sons, Inc., 1973.

20. Smith, Cecil L. Digital Computer Process Control. New York: International Textbook Company, 1972.

21. Raven, Francis H. Automatic Control Engineering. New York: McGraw-Hill, 1961.

22. Thyristor and Rectifier Manual. Radio Corporation of America, Solid-State Division, Somerville, New Jersey, 1975.

23. Speckhart, F. H. A Guide to Using CSMP. Englewood Cliffs, New Jersey: Prentice-Hall, Inc., 1976.

24. Kuo, Benjamin C. Linear Networks and Systems. New York: McGraw-Hill, 1967.

25. Gupta, S. C. Transform and State Variable Methods in Linear Systems. Huntington, New York: R. E. Krieger Publishing Co., 1971.

APPENDIX

APPENDIX

SIMULATION PROGRAM FOR SWITCHING POWER TAKE-OFF

```
IIOIXII      II   I
//EGCON12  JOB (00R893,064818,REMOTE3,R-192K,T-2,C-8000),'KWONG'
//STEP1 EXEC CSMP3,REGION=192K
//FT20F001 DD SYSOUT=B
//SYSIN DD    *
*
*   THIS SIMULATION DEALS WITH POWER TAKEOFF
*   OF A MHD GENERATOR USING STATE EQUATIONS
*  OF 15 LOOPS WITH CONTROL ON ALL SWITCHES
*
INITIAL
/       DIMENSION DC(6),DDC(6),CE(6),SP(6),IB(6),DE(6)
/       DATA SP/31.21,77.46,8.86,50.58,61.55,5.4/
/       DATA DC/6*0.9E-03/
/       DATA CE/6*0.0/
        CONSTANT C=0.001,L=0.001,RA101=3.36,RA100=25.91,RA102=3.,...
        RA99=3.07,V101=730.,V100=6090.,V99=410.,V102=187.,V98=54.3,...
        RL=25.52,XTPL=-0.0000001,RA98=5.03,XK=1.0E-8
    NOSORT
        WRITE(20,1) FINTIM,OUTDEL,PRDEL,DELT
    1   FORMAT(4E20.10)
DYNAMIC
  NOSORT
*
*
*     START TO CONTROL
*
*
        IF (TIME-0.15) 60,70,70
  70    IB(1)=IA102
        IB(2)=IDA102
        IB(3)=IDA101
        IB(4)=IDA99
        IB(5)=IDA98
        IB(6)=IA98
        DO 50 I=1,6
        DE(I)=SP(I)-IB(I)-CE(I)
        CE(I)=SP(I)-IB(I)
        DDC(I)=XK*(5*CE(I)+DE(I))
*         DDC(I)=XK*CE(I)
*         DDC(I)=XK*(CE(I)+100*DE(I))
        DC(I)=DC(I)+DDC(I)
        IF (DC(I)-.0018) 45,40,40
  40    DC(I)=0.0018
  45    CONTINUE
        IF(DC(I)-.0001) 85,85,80
  85    DC(I)=0.0001
  80    CONTINUE
  50    CONTINUE
  60    CONTINUE
        DC1=DC(1)
        DC2=DC(2)
        DC3=DC(3)
        DC4=DC(4)
        DC5=DC(5)
        DC6=DC(6)
*
  SORT
        TRIG=IMPULS(0.0,0.002)
        U1=-0.5+PULSE(DC(1),TRIG)
        U2=-0.5+PULSE(DC(2),TRIG)
        U3=-0.5+PULSE(DC(3),TRIG)
        U4=-0.5+PULSE(DC(4),TRIG)
        U5=-0.5+PULSE(DC(5),TRIG)
        U6=-0.5+PULSE(DC(6),TRIG)
```

```
      HZ=1000.0
      LZ=0.1
      RC102=INSW(U1,HZ,LZ)
      RC101=INSW(U2,HZ,LZ)
      RC100=INSW(U3,HZ,LZ)
      RC99=INSW(U4,HZ,LZ)
      RC98=INSW(U5,HZ,LZ)
      RC97=INSW(U6,HZ,LZ)
*
*  START OF STATE EQUATIONS
*
      DI98=(VA98-VC98)/L
      I98=INTGRL(0.0,DI98)
      DI99=(VA99+VA98-VC98-VC99)/L
      I99=INTGRL(0.0,DI99)
*
      DI100=(VA99+VA100+VA98-VC98-VC99-VC100)/L
      I100=INTGRL(0.0,DI100)
*
      DI101=(VA99+VA100+VA101+VA98-VC98-VC99-VC100-VC101)/L
      I101=INTGRL(0.0,DI101)
*
      DI102=(VA98+VA99+VA100+VA101+VA102-VC98-VC99-VC100-VC101-VC102)/L
      I102=INTGRL(0.0,DI102)
*
      DVA98=(V98/RA98-I98-I99-I100-I101-I102-VA98/RA98)/C
      VA98=INTGRL(0.0,DVA98)
*
      DVA99=(V99/RA99-I99-I100-I101-I102-VA99/RA99)/C
      VA99=INTGRL(0.0,DVA99)
*
      DVA100=(V100/RA100-I100-I101-I102-VA100/RA100)/C
      VA100=INTGRL(0.0,DVA100)
*
      DVA101=(V101/RA101-I101-I102-VA101/RA101)/C
      VA101=INTGRL(0.0,DVA101)
*
      DVA102=(V102/RA102-I102-VA102/RA102)/C
      VA102=INTGRL(0.0,DVA102)
*
      S1=RC102+RC101
      S2=RC101+RC100
      S3=RL+RC100+RC99
      S4=RC99+RC98
      S5=RC98+RC97
      S6=S2-RC101**2./S1
      S7=S4-RC98**2./S5
      S8=S3-RC99**2./S7-RC100**2./S6
*
      T1=RC99*(VC99+RC98*VC98/S5)/S7
      T2=RC100*(VC101+RC101*VC102/S1)/S6
*     IC100=(VC100+T1+T2-VL)/S8
      IC100=(VC100+T1+T2)/S8
      VL=INTGRL(0.0,DVL)
      ICF=IC100-VL/RL
      DVL=ICF/C
      IL=VL/RL
      IAV=(IC100-AVG)/0.001
      AVG=INTGRL(0.0,IAV)
      P=1.0E-3*VL*IL
*
*
      JC99=(VC99+RC98*VC98/S5+IC100*RC99)/S7
      IC99=LIMIT(0.0,IC100,JC99)
      JC101=(VC101+RC101*VC102/S1+IC100*RC100)/S6
```

```
      IC101=LIMIT(0.0,IC100,JC101)
*
      JC102=(VC102+IC101*RC101)/S1
      IC102=LIMIT(0.0,IC101,JC102)
      JC98=(VC98+IC99*RC98)/S5
      IC98=LIMIT(0.0,IC99,JC98)
*
      DVC102=(I102-IC102)/C
      VC102=INTGRL(0.0,DVC102)
*
      DVC101=(I102+I101-IC101)/C
      VC101=INTGRL(0.0,DVC101)
*
      DVC100=(I102+I101+I100-IC100)/C
      VC100=INTGRL(0.0,DVC100)
*
      DVC99=(I102+I101+I100+I99-IC99)/C
      VC99=INTGRL(0.0,DVC99)
*
      DVC98=(I102+I101+I100+I99+I98-IC98)/C
      VC98=INTGRL(0.0,DVC98)
      IA101=(V101-VA101)/RA101
      IA100=(V100-VA100)/RA100
      IA99=(V99-VA99)/RA99
      IA98=(V98-VA98)/RA98
      IA102=(V102-VA102)/RA102
*
      IDA101=IA100-IA101
      IDA99=IA100-IA99
      IDA98=IA99-IA98
      IDA102=IA101-IA102
      IDC101=IC100-IC101
      IDC99=IC100-IC99
      IDC98=IC99-IC98
      IDC102=IC101-IC102
*
   NOSORT
      IF(XTPL-TIME) 10,10,100
   10 WRITE(20,11) TIME,IA98,IC98,IL
      WRITE(20,11) IDA102,IDA101,IDA99,IDA98
      WRITE(20,11) IDC102,IDC101,IDC99,IDC98
      WRITE(20,11) IA102,IA101,IA100,IA99
      WRITE(20,11) IC102,AVG,IC100,P
      XTPL=XTPL+OUTDEL
   11 FORMAT(4E20.10)
  100 CONTINUE
TERMINAL
      TIMER FINTIM=0.6,OUTDEL=0.6E-3,PRDEL=2.0E-2,DELT=1.0E-4
      METHOD RKSFX
      PRINT AVG,IA102,IC100,IDA102,IDA101,IDA99,IDA98,IA98,...
      DC1,DC2,DC3,DC4,DC5,DC6,IC102,IDC102,IDC101,IDC99,IDC98,IC98,...
      VC102,VC101,VC100,VC99,VC98,VA102,VA101,VA100,VA99,VA98,IL,P
END
STOP
ENDJOB
```

VITA

Kin Chun Kwong was born in Macao, a Portuguese Colony in the Far East, on August 24, 1956. He passed the Hong Kong School Certificate Examination. He entered Hong Kong Baptist College in September 1974 to pursue studies towards the Diploma of Science and Engineering with a major in Physics. After he received the Diploma, he entered Seattle University in January 1979 to study for the degree of Bachelor of Electrical Engineering. In September 1980, he joined The University of Tennessee Space Institute and completed the requirements for the Master of Science degree with a major in Electrical Engineering in June 1982. He is working as an Electronic Engineer for Precision International, Inc., in Tullahoma, Tennessee.