Design Considerations for GaN-based Photovoltaic Inverter and Solid-State Circuit Breaker

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Abstract

Featuring low specific on-state resistance, high switching speed, and zero reverse recovery current, Gallium Nitride (GaN) transistor is becoming one of the most promising devices for power electronic applications. This dissertation presents some design considerations for photovoltaic (PV) inverters and solid-state circuit breakers (SSCBs) using GaN devices. Several related challenges and solutions will be discussed in this dissertation.

First, the filter design for full bridge PV inverter is discussed, which includes the design and optimization of individual inductor and overall power filter. The inductor design takes the fringing effect into account, and achieves optimal design with simple algorithm. Then, the design method is applied to the power filter which consists of both coupled and non-coupled inductors. The modeling of the power filter and the optimal ratio between coupled and non-coupled inductors are also presented.

Second, the inductive coupling between components, and its impact on EMI performance is studied. An improved design procedure which identifies and models the critical couplings is proposed. The design procedure models the impact of inductive coupling on the performance of the EMI filter and provides guidelines to achieve sufficient EMI noise suppression.

Third, some often-neglected factors on loss modeling of the converter are quantified, including parasitic capacitance across the devices, on-state resistance (R_{dson}) variation against drain current (I_d) and junction temperature (T_j), dynamics of T_j under time-varying power dissipation (P_{loss}), thermal coupling among nearby GaN devices, and detailed considerations of the passive components. A systematic approach to implement a detailed loss model is also presented.

Fourth, GaN-based and Silicon (Si)-based PV inverters are designed and compared based on the same specification derived from a commercial product. Compared to the Si-based inverter, the GaN-based version can achieve lower cost by using higher switching frequency, which shrinks the filtering components. The result justifies using GaN devices in PV inverters.

Finally, dc overcurrent capability of GaN devices is evaluated, which is a critical characteristic in the design of a dc circuit breaker. The test setup and procedures are discussed, which can evaluate the dc overcurrent capability under different junction temperature, different current levels, and time durations.

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Chapter 1 Introduction

This chapter introduces the background and recent development of Gallium Nitride power devices, solar inverters, and solid-state circuit breakers. The research objectives, approaches, as well as the organization of this dissertation are presented.

1.1 Application Background

1.1.1 Gallium Nitrite High Electron Mobility Transistor

As shown in Figure 1-1, GaN is one of the wide bandgap (WBG) materials featuring higher electrical field, energy gap, electron velocity and melting point than Silicon. The advantages at material level potentially enable power semiconductor devices, including transistors and diodes, to achieve higher breakdown voltage, lower specified on-state resistance (R_{dson}), higher switching speed, smaller footprint, and higher temperature operation. These advantages can be leveraged to improve the performance of power converters.

GaN high electron mobility transistor (HEMT) is originally normally-on or depletion mode (D-mode), which is undesirable for most power electronics applications. Several technologies have been developed to design and fabricate the normally-off devices, such as using cascode configuration [3-6] and enhancement-mode (E-mode) GaN transistors [7-10]. E-mode devices rated at 200 V and 650 V GaN were commercialized in 2010 and 2014, respectively [11]. Due to the advantages, the market share of GaN power devices is expected to grow tremendously, reaching more than 100 million dollars in 2023 [12].

To understand the behaviors and fully utilize the advantages of GaN HEMTs, the characterization and modeling of GaN devices have been intensively studied in the last two decades. This includes the fabrication, characterization, as well as qualification of GaN devices.

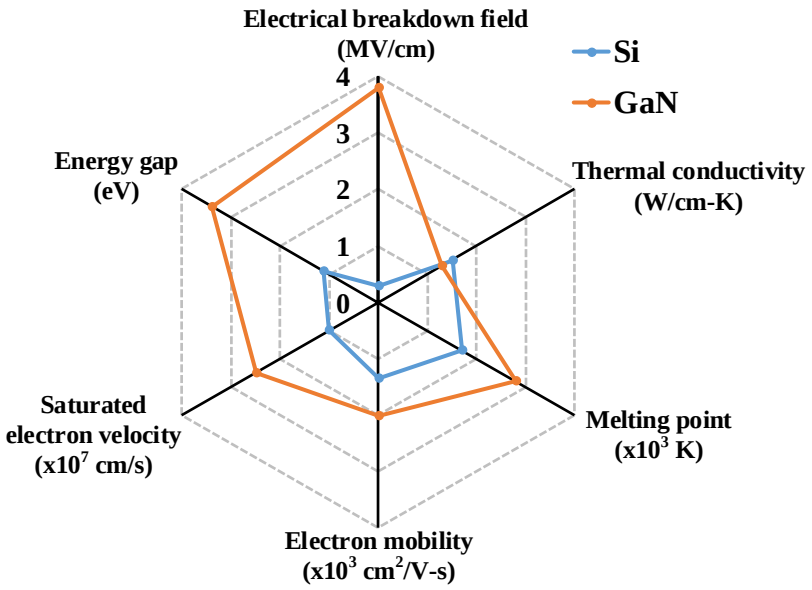


Figure 1-1. Comparison of some properties of Si and GaN materials [1, 2].

Meanwhile, GaN transistors also bring several opportunities and challenges to power converters. Intensive research has also been conducted to study GaN-based power converters. In this work, some characteristics of GaN devices and challenges of GaN-based converters related to photovoltaic inverter and dc solid-state circuit breaker are studied.

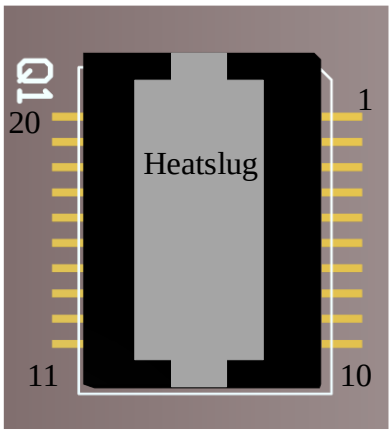
The device used throughout this work is IGOT60R070D1, a 600V top-cooled GaN transistor from Infineon. The top view and pin assignment of this device are shown in Figure 1-2. The exposed metal heatslug on the top side of the device is electrically connected to the source terminals inside the device package.

1.1.2 String Photovoltaic Inverter

One potential application of GaN HEMTs is in power converters for PV systems. PV is one of the feasible technologies to convert solar energy into direct current (dc) electricity. It is expected that PV capacity will exceed 400 GW in US by 2050 [14]. In this study, the focus is residential PV applications, which are typically rated between 2 and 10 kW [15].

String PV system, consisting of series-connected set of solar cells or modules, is one of the technologies in residential PV application. A typical structure of string PV system is shown in Figure 1-3 [16]. In this PV system, a dc-dc power converter is used to maximize the power output of PV panels, while the dc-ac power conversion transfers the generated dc electricity to the alternating current (ac) power grid. This dissertation focuses on two aspects of the string PV system: dc-ac inverter and ac-side filters.

For dc-ac inverter and ac-side filter, GaN devices can also bring numerous benefits. For instance, by switching at higher frequency, the size of some components, such as capacitors and inductors, can be reduced. This can improve the power density and efficiency of the inverter. The



Gate	9,10
Drain	13,14,15,16,17,18
Kelvin Source	8
Source	3,4,5,6,7,heatslug
Not connected	1,2,11,12,19,20

Figure 1-2. Top view and pin assignment of a GaN transistor, IGOT60R070D1 [13].

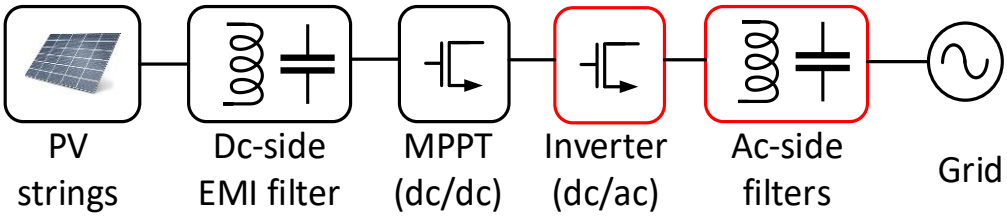


Figure 1-3. Structure of string PV inverter systems, with the focuses of this dissertation highlighted in red.

cost of the inverter can also be potentially reduced by lowering the cost of filters. However, GaN devices can also introduce some new challenges to the inverter and filter design. Some often-neglected factors can become more critical due to the features of GaN devices. Quantifying the impacts of these factors can be useful a design guideline for GaN-based converters. As for the filters, components can interfere with each other through high-frequency magnetic field, which can significantly alter the performance. This factor needs to be considered in the design process of the filter.

1.1.3 Solid-State Circuit Breaker for Dc Systems

Dc power systems have been intensively studied in power transmission and distribution, due to its low loss, low cost, and avoidance of grid synchronization. Protection is one of the most essential elements in dc systems, including dc microgrids [17, 18], dc shipboard power systems [19-22], electric aircraft [23, 24], datacenter [25], and so on. Conventionally, circuit breaker is implemented by a mechanical circuit breaker (MCB). However, MCB has relatively long response time due to the mechanical movement. As a result, the fault current can increase to a high level when the breaker starts to react. Another drawback of MCB is arcing since dc current does not have zero crossing like its ac counterpart. In contrast, a solid-state circuit breaker, offering high protection speed and free of arcing, is regarded as a promising candidate as a protection device in dc systems. The main characteristics MCB and SSCB are summarized and compared in Table 1-1. Comparing with the MCB which typically responds in the range of a few to tens of ms, SSCB can achieve a response time less than 100 μs.

Since the circuit breaker is in the conduction state during most of the operating time, low conduction loss and high efficiency are key requirements. Therefore, GaN devices can be favorable

Table 1-1. Comparison between MCB and SSCB [26]

	MCB	**SSCB**
Response time	Slow, tens of ms	Very fast, <100 µs
Losses	Very low, few Watts	Very high, hundreds of Watts
Weight and volume	Small and compact	Large due to heatsink needed
Cost	Relatively low	High

in SSCB applications thanks to lower specific on-state resistance compared with Si counterparts.

In order to apply GaN devices to dc SSCB applications, some related characteristics of the devices need to be thoroughly studied. In addition to the normal operation, devices can also be subject to voltage and current stresses in faulty condition. Therefore, the overvoltage and overcurrent capability of the devices also need to be understood [27-29].

1.2 Research Objectives and Approaches

The objectives of this research work include filter design, converter loss modeling and cost analysis for a GaN-based PV inverter, and evaluation of dc overcurrent capability of GaN devices. The approaches are:

1. To develop an improved design method that considers fringing effect for air-gapped inductor, and apply the method to optimize overall performance of the power filter.
2. To model the self-parasitic and coupling and their impacts in a high-density multi-stage filter, and propose an accurate and efficient design method for the EMI filter.
3. To systematically quantify some often-neglected factors and their impacts in loss modeling of a GaN-based converter.
4. To compare the cost of GaN-based and Si-based PV inverters based on the same specifications.
5. To characterize the dc overcurrent capability of GaN devices, and apply the results to the design of a GaN-based dc SSCB.

1.3 Dissertation Organization

This dissertation is organized as follows:

Chapter 2 gives a detailed literature review on some of the key issues in the design of a GaN-based PV inverter and GaN-based SSCB. For the PV inverter, the issues include filter design, loss modeling, and cost optimization. Then, the evaluation methods for overcurrent capability of power devices are reviewed. Such capability is an important consideration for the design of SSCB.

Chapter 3 gives an improved design method for individual inductor as well as the design of power filter containing multiple inductors. The inductor design method considers the fringing effect caused by the air gaps and finds the optimal design which has the lowest turn number and the smallest core size. The second half of this chapter presents the overall design of the power filter which consists of both coupled and non-coupled inductors for PV inverter. The ratio between coupled and non-coupled inductors and its effects on the performance of the filter is modeled in a GaN-based single-phase inverter.

Chapter 4 discusses the inductive coupling in high-density multi-stage EMI filters. It is identified that certain couplings can significantly worsen the filtering performance, while some couplings have less impacts. To consider inductive coupling at the design stage, an accurate and efficient design method is proposed to design the EMI filter, which also provides guidelines for better PCB layout.

Chapter 5 discusses some often-neglected factors and consideration in the converter loss modeling. The impact of each factor on the converter loss is quantified at different loading conditions. A systematic approach is also proposed to model these factors.

Chapter 6 presents the design and cost comparison of GaN-based and Si-based PV inverters using the same specifications. The cost breakdown of both inverters is presented, and the methodology to reduce the overall cost of GaN-based inverter is revealed.

Chapter 7 presents the test and analysis of dc overcurrent capability of GaN device. The test setup and procedures are developed, which allows the device to operate close to its limit without degrading the device. The results are also applied to the design of a GaN-based SSCB and demonstrated in a prototype.

Chapter 8 concludes this dissertation and recommends future work that may be undertaken in this area.

Chapter 2 Literature Review

2.1 Ac-side Filter Design in PV Inverter

Filters, which can be used for harmonic and electromagnetic interference (EMI) suppression, is one of the indispensable elements in a power converter. The filter also takes up a considerable portion of the loss, cost, mass, and volume in the converter [30-34]. For example, it is shown in [32] that the filter contributes more than 75% of volume and 80% of weight in Si IGBT based 3-phase dc-ac converter. The numbers become 65% and 75% in Silicon Carbide (SiC) MOSFET based counterpart. Thus, improvement and optimization of the filter design can be critical to the overall design of converter. In this dissertation, an improved design method for the individual inductor is developed, and then the optimization of the overall filter consisting of multiple inductors is presented.

2.1.1 Design of Inductor with Fringing Effect

There are two widely used design methods in the literature: core geometry (K_g) method and Area Product (A_P) method [35, 36]. Although these methods only require simple algorithms and equations, they become complex once fringing effect, which is induced by the air gap, is considered. Fringing effect increases the effective cross-sectional area of the air gap and hence decreases the magnetic reluctance of the air gap, which eventually leads to increased inductance and flux density in the magnetic cores [37-39]. In particular, for high-frequency and high-current converters where the required inductance is small, and the air gap is relatively large, fringing effect can significantly affect the performance of inductors.

One conventional approach to consider fringing effect is to calculate the fringing flux factor (F_r) and iteratively adjust the length of the air gap, such that the desired inductance value can be

achieved. However, the possible reduction in core size and turn number is not considered since this method only adjusts the air gap. An alternative way is to iteratively change the turn numbers and core size in addition to the air gap, which complicates the algorithm. Also, the impacts of fringing effects on flux density are not considered in this method. Lastly, convergence of air gap length and fringing flux factor is not always guaranteed.

2.1.2 Output Filter using Coupled and Non-Coupled Inductors

Single-phase dc-ac inverter is one of the most widely used power converters. It typically serves as an interface between dc sources, such as PV panels and batteries, and ac systems. Since the inverter usually uses PWM control, the output contains a wide range of harmonics [40, 41]. Therefore, ac-side filter is added to meet the harmonic requirement. In fact, this filter is one of the bulkiest, costliest, and most lossy components in a power inverter [42].

To filter the harmonics generated from the PWM switching of the inverter, several filter topologies have been proposed. Specifically, the method proposed in [43] modifies the conventional *LCL* filter by connecting the midpoint of the output filter to the midpoint of the dc-link capacitors and adding a coupled inductor. The topology is shown in Figure 2-1. This method features simple topology, low leakage current and low converter loss.

For the design reported in [43], it makes use of large coupled inductor to achieve high attenuation of CM noise, and to reduce the current ripple of the inductors. However, the optimal ratio between coupled and non-coupled inductors and the holistic design for the ac-side filter have not been studied for single phase dc-ac converter. In fact, the ratio not only affects the current in both the coupled and non-coupled inductors, but also determines the performance of the filter, including the size, weight, loss and EMI attenuation [44]. For example, if the coupled inductor is

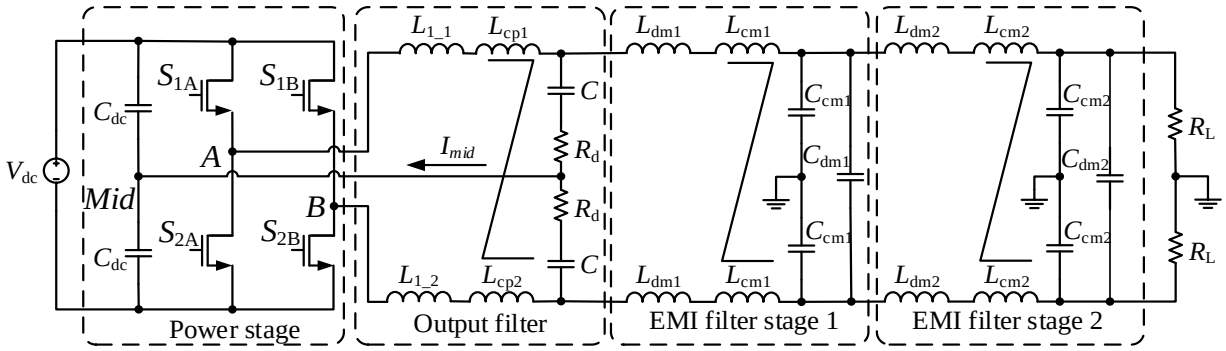


Figure 2-1. Topology of single-phase full bridge inverter, using output filter topology proposed in [43].

designed to be much larger than the non-coupled one, ripple current reduces, and EMI attenuation increases. However, the overall weight, loss and size of the filter can also increase. Therefore, a holistic design considering both coupled and non-coupled inductors is needed.

2.1.3 Design of EMI Filter with Self-Parasitics and Inductive Couplings

Several international standards specify the noise levels and associated frequency ranges based on the applications. The purpose of the EMI filter is to attenuate the electromagnetic noise generated by the high-speed switching in the converter, such that the regulatory level can be satisfied. For residential PV application, FCC part 15 Class B standard is considered, which specifies the conductive EMI level from 150 kHz to 30 MHz. Design of the EMI filter at such frequency range can be challenging due to the non-linearity of the materials, self-parasitic of the components, as well as coupling among components [45]. For example, the permeability of the magnetic material can change drastically as the frequency increases, which leads to the change in inductance. For self-parasitic, the equivalent series inductance (ESL) of the capacitor and the equivalent parallel capacitance (EPC) of the inductor can also alter the performance of the filter starting at several hundred kHz. In addition, the inductive coupling and capacitive coupling can also significantly affect the attenuation of the filter, especially in high-density converters where multi-stage EMI filters and dense PCB layout are employed. As a result of these factors, the design of an EMI filter is usually a time-consuming process involving iteration and tuning.

Based on [46], a step-by-step method to design an EMI filter is summarized in flowchart in Figure 2-2. First, the EMI noise without using EMI filter is obtained in time domain simulation, which is also known as ‘bare noise’. The second step is to convert the time-domain noise into frequency domain. Afterwards, the required attenuation can be calculated by comparing the bare

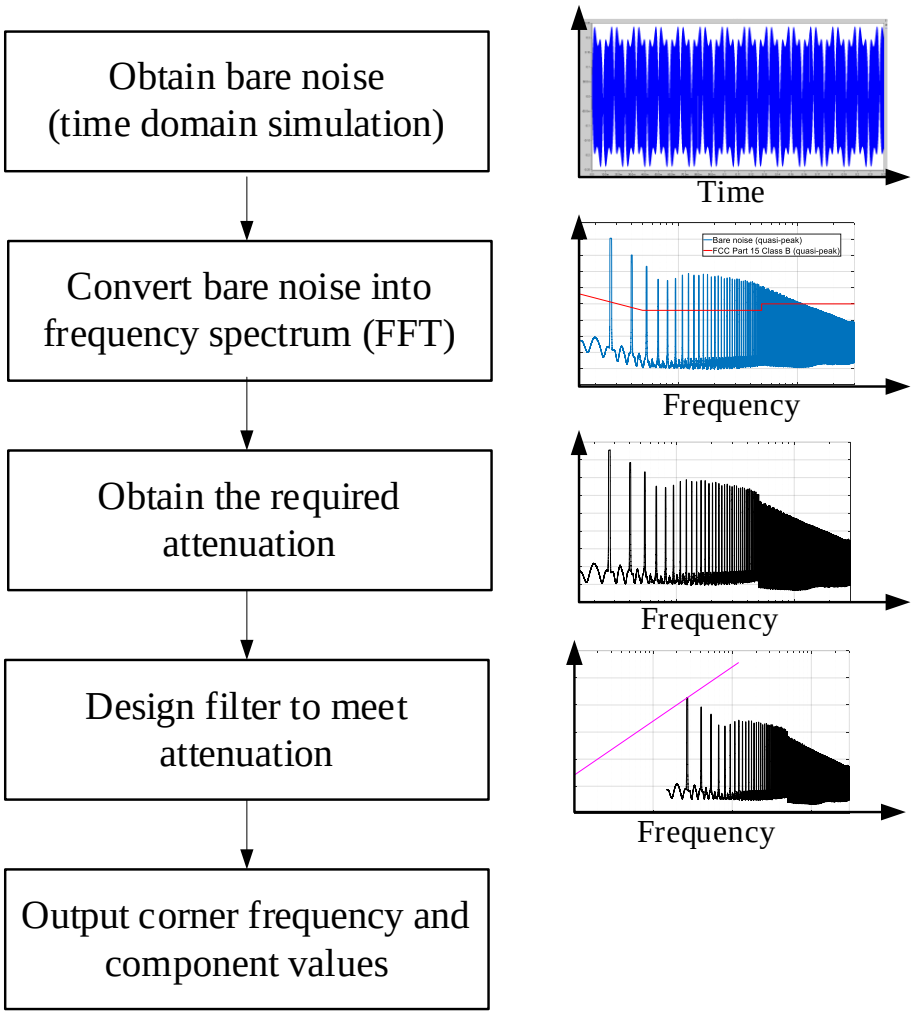


Figure 2-2. Conventional method to design EMI filter.

noise with the EMI standard and applying certain design margin. For an n-stage EMI filter, a 40*n dB/dec line tangential to the peak of the required attenuation can be applied. The intersection between this line and $y = 0$ dB is the corner frequency of the designed EMI filter, from which the component values can be derived [47]. The filter topology can be determined based on the impedance mismatch theory [48].

A similar method with some improvement has been proposed in [44, 49]. Instead of assuming 40*n dB/dec attenuation for n-stage EMI filter, this method uses the equivalent circuit to calculate the exact attenuation of the filter. The impacts due to the source and load impedance can be considered. However, the measurement results can still deviate from the prediction at frequencies above 200 kHz. Although these methods are simple and no iteration is required, it is only accurate for relatively low frequency range and certain applications. In [46], it is shown that for the basic design procedures without considering the non-linearity of the components, parasitic, or coupling, the measured attenuation of the EMI filter can only match with calculation values up to 260 kHz (2nd harmonic of the 130 kHz switching frequency).

The equivalent circuit of an inductor is shown in Figure 2-3 [50]. In addition to inductance (L), there are also series resistance (R_{ac}) and equivalent parallel capacitance (EPC). The inductance can change with current and/or frequency depending on the material. The series resistance represents the combination of the winding and core loss of the inductors. Since the winding and core losses are frequency-dependent, series resistance also changes with frequency. As for the EPC, it is mainly due to the core-to-winding, and winding-to-winding capacitance [51]. In case grounding and shielding are used, there can be extra capacitance [52].

The equivalent circuit for a capacitor is shown in Figure 2-4 [14]. The self-parasitics

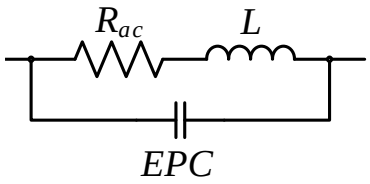


Figure 2-3. Equivalent circuit of an inductor.



Figure 2-4. Equivalent circuit of a capacitor.

include ESR and ESL. They are both mainly due to contact leads. The values of ESR and ESL can be derived from the impedance curve in the datasheet [15].

The impacts of self-parasitics are addressed, and a high frequency filter model is proposed in [45]. Methods are also proposed to cancel the self-parasitic of inductors and capacitors [53, 54]. Furthermore, design methods that consider the self-parasitics of the components are proposed in [55, 56].

The performance of EMI filter depends not only on the characteristics and self-parasitic of individual component, but also the interference between components. As dense PCB layout and multi-stage EMI filter are desirable to increase the power density of converters, inductive couplings among nearby components can also increase, which significantly alters the characteristic of the filter from ideality. Inductive couplings can occur between two inductors, between the ESLs of two capacitors, and between inductor and ESLs of capacitor [57-60]. In addition, PCB traces can also couple with other inductive components [58]. The inductive coupling is usually modeled by mutual inductance between two involved elements. For inductive coupling between two nearby components connected in series, the equivalent circuit is shown in Figure 2-5. For coupling between two components that are not directly connected, some approximation can be made to simplify the analysis [58].

To model the inductive coupling and extract the mutual inductance between two components, measurement and FEA simulation can be used. In [58, 61], the mutual inductance between two components is extracted using scattering parameters. In [62-64], the coupling value is simulated in Partial Element Equivalent Circuit (PEEC) software. The impacts of inductive coupling on the EMI noise are experimentally studied in [65].

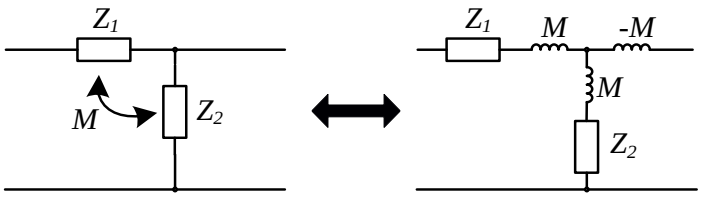


Figure 2-5. Equivalent circuit for two inductively coupled components.

There are also several methods proposed in the literature to reduce the couplings and its impacts, including:

1) Increasing the distance between components, such as separating inductors and capacitors into different PCBs or different sides of the PCB [65, 66];

2) Using shielding [56];

3) Using small-sized components, such as ceramic capacitor [66];

4) Adjusting the orientation of components [57, 67];

5) Adjusting winding orientation and arrangement [68];

6) Introducing extra coupling to cancel the effects of coupling [68].

Some design methods in the literature have been proposed to take both self-parasitic and inductive coupling into consideration. For example, to improve the filter performance and reduce the coupling, several design rules on the PCB layout and a component placement software are proposed in [62]. Another software GeckoEMC based on the 3D models of components is proposed in [69]. These methods can accurately predict the overall performance of an EMI filter since each component and coupling is included. However, it can be a complex and time-consuming design process to consider and model all filtering components and their couplings, especially for multi-stage EMI filter involving many components. Also, if the initial design fails to meet the requirement, it would be a trial-and-error process for designers to tune many components in the simulation or software. A better solution should provide more specific guideline for the designer to identify and tackle certain self-parasitics and couplings that have more impacts on the filter performance at the early stage of the design process, so that the design complexity can be reduced.

2.2 Considerations for Converter Loss Modeling

Accurate modeling of the converter loss is critical to the converter design. This requires not only the characteristics of each component in the circuit normally from component data sheet, but also understanding of converter operation and consideration of the practical issues such as parameter variations during operation, and parasitic elements. Typically, calculation of converter loss is based on the datasheet of active devices and passive components, considering the operating conditions, such as temperature, current and voltage. Some approximations are commonly used to simplify the loss model. For example, the parasitic capacitance is usually small and has negligible impact on the switching loss. The junction temperature of switches is assumed constant at thermal steady-state. While GaN devices can improve the performance of converters, new challenges are also introduced, and some approximations commonly used for Si-based converters need to be revisited.

As the GaN devices have relatively small junction capacitance (C_{oss}), the external parasitic capacitance (C_p) introduced by the filters, heatsinks, and PCBs becomes comparable to C_{oss}. As a result, the switching loss of GaN devices become more sensitive to parasitic elements compared to Si counterparts, and its impacts are no longer negligible. It has been reported that the C_p introduced by filters and heatsinks can have a noticeable impact on the switching performance of the power devices, such as the switching speed, switching loss, and voltage overshoot [70-72]. Additionally, due to the relatively small die size and package of GaN devices, the thermal capacitance between the junction and the case of the devices ($C_{\theta,j\text{-}c}$) can be low. Thus, the junction temperature can have fast response to time-varying power loss. In particular, variation of T_j can be significant for an inverter where the instantaneous power loss changes in a wide range within one

50/60 Hz line cycle [73-77]. This time-varying T_j along with time-varying I_d need to be treated carefully in loss calculation, because both switching loss and $R_{ds,on}$ depend on temperature and current.

Another challenge is to accurately estimate the temperature of switches. On one hand, GaN devices usually require dense PCB layout to reduce the parasitic inductance and improve the switching performance [78, 79]. This can lead to strong thermal coupling among the nearby devices, which can be complex using lumped thermal resistance as in conventional thermal models [80]. One the other hand, it has also been shown that thermal resistance of heatsink ($R_{\theta,hs}$) is highly dependent on the temperature rise of heatsink (ΔT_{hs}) and power loss, especially in natural convection with no forced airflow. Methods have been proposed to experimentally derive the relationship between $R_{\theta,hs}$ and $\Delta T_{hs}/P_{loss}$ for specific heatsinks and thermal loads [75, 80]. A more general method is to use finite element analysis (FEA) simulation to estimate the device temperature.

Finally, approximations on passive components, including inductors and capacitors, can also become important contributors to converter loss. For example, the loss density of magnetic cores at low temperature can be much higher than that at high temperature where the Steinmetz parameters are usually specified [81-84]. As the size of inductors decreases in high-frequency converter, the fringing effect due to air gap can significantly affects flux density and core loss [37, 38, 85]. Also, the loss of capacitors is no longer negligible as the loss from other components decrease [86].

Although some of the above issues have been individually studied at component level in previous literature, there is no systematic evaluation to consider all the possible factors and quantify the impacts of each factor in a GaN-based inverter.

2.3 Cost Comparison between GaN-based and Si-based Dc-ac Inverters

In the previous literature, various research has studied the benefits of GaN-based power converters. For instance, it has been demonstrated that compared with Si devices, GaN devices have lower conduction, switching and driving losses, and also reduce the transformer winding loss because lower total device charge is required during soft-switching transient [87]. In [4], GaN devices are proved to improve the efficiency of buck and LLC converter due to zero reverse recovery and low junction capacitance. In [42], it was shown that GaN-based single-phase T-type inverter can reduce the power loss and volume of heatsink, compared to Silicon Carbine (SiC)-based and Si-based counterparts. Some proposed converters in Little Box Challenge also use GaN devices and high switching frequency to shrink the size of passive component and increase the power density of an inverter [88-90].

However, there is a lack of study on the cost of GaN-based converters, with a fair comparison to Si-based counterparts, which can be useful for some cost sensitive applications, such as PV application. In fact, cost is a critical consideration for PV application. Although the cost is still relatively high compared to mature Si devices, GaN transistors enable higher switching frequency, which shrinks the passive filters. Meanwhile, as shown in Figure 2-6, the cost of heatsink can either increase or decrease depending on how high the switching frequency is and the thermal characteristics of the devices. Also, the harmonics at EMI range can be higher as switching frequency increases, which can increase the cost of EMI filter. Therefore, the overall cost of the

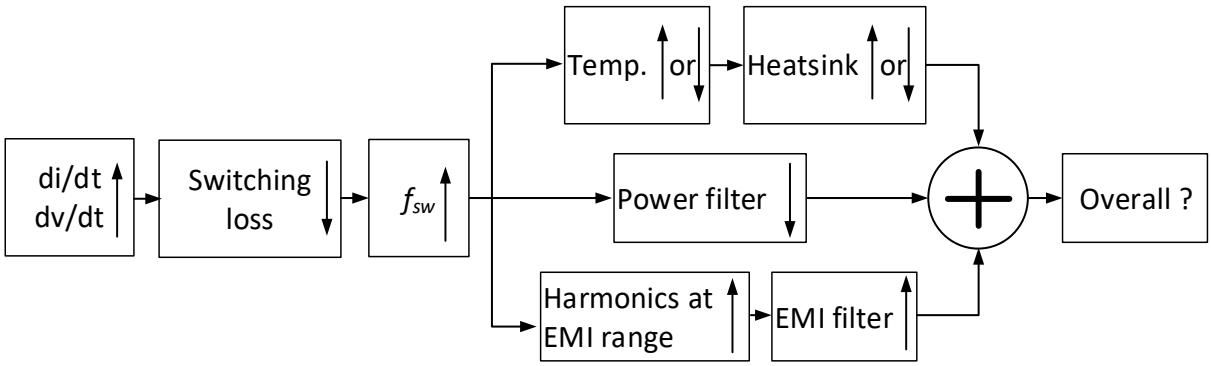


Figure 2-6. Potential impacts on the cost of power converter due to the application of GaN devices.

GaN-based converter needs to be studied and compared with the Si-based counterpart under the same requirement.

To study the cost benefits introduced by GaN transistors, this work compares the cost of single-phase inverters using both GaN and Si transistors. Two converters are designed to meet the same requirement, which is derived based on a commercial PV inverters of similar power rating.

2.4 Dc Overcurrent Capability of GaN Transistor

One important characteristic of power devices is overcurrent capability for short durations, since overcurrent often occurs during overload and transient states of the converters. In fact, power converters for applications such as uninterruptible power supply (UPS) for datacenters and solid-state circuit breakers require intense overload capability. This needs to be considered when selecting power semiconductor devices and converter topologies [29, 91, 92]. In the previous literature, surge current capability of GaN devices in the third quadrant has been experimentally determined for half of ac line cycle, 10 ms [93]. The short circuit capability of GaN transistors up to 14 μs have also been studied [94, 95]. However, there is a lack of research on dc overcurrent capability of GaN transistors at longer durations ranging from 10s of ms to several seconds, which can be useful for the design of dc SSCB.

One solution is to set the maximum junction temperature of the devices to certain level, e.g., 150 °C, and use transient thermal impedance and electrical characteristic of the devices to determine overcurrent capability. However, this can underestimate the overcurrent capability of the device, since the device can withstand excessive temperature and high current for short period of time. Also, the thermal and electrical characteristics of the GaN devices are usually not available for junction temperature above 150 °C. In this work, the dc overcurrent capability of the GaN

devices is experimentally determined, and the results are applied to the design of a GaN-based SSCB.

Chapter 3 Modeling and Design of Ac-side Power Filter in GaN-based Inverter

3.1 Inductor Design Considering Fringing Effect

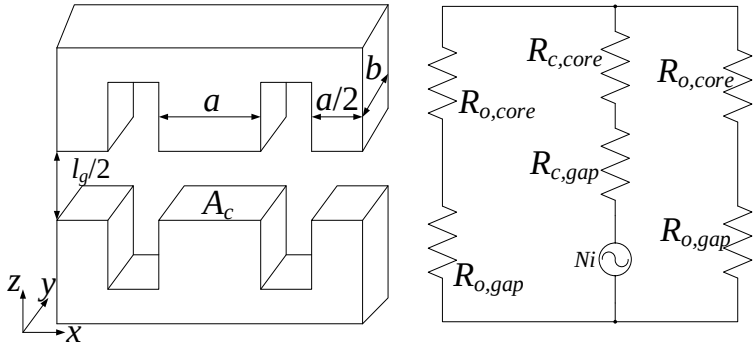
3.1.1 Inductor Modeling with Fringing Effect

In this work, single-phase EE cores are used as an example to illustrate the inductor modeling and design method, and the same method can be applied to other shapes of magnetic cores. Figure 3-1 shows the geometry of one pair of single-phase EE cores and its equivalent magnetic circuit, assuming that the fringing effect is neglected, and the wire is wound on the center post of the core. The cross-sectional area of outer posts is identical, and it is half of the center post. In the figure, $R_{c,core}$ and $R_{c,gap}$ are the magnetic reluctance of the core and airgap of the center post, while $R_{c,core}$ and $R_{c,gap}$ are of outer posts. It is assumed that the center post and two outer posters have the air gaps of the same length. However, the modeling and design methodology are still valid if center and outer poster have different lengths of air gap.

The reluctance of the core is typically much higher than that of the air gap because $\mu_{core} \gg \mu_0$. Therefore, the reluctance of the magnetic core can be neglected. The inductance without considering fringing effect can be approximated by

$$L \approx \frac{N^2}{R_{c,gap}+\frac{R_{o,gap}}{2}} = \frac{N^2 \mu_o A_c}{l_g}, \tag{3-1}$$

where N is the number of turns, $R_{c,gap} = \frac{l_g/2}{\mu_o A_c}$ and $R_{o,gap} = \frac{l_g}{\mu_0 A_c}$ is the reluctance of the air gap in center post and outer posts when neglecting the fringing effect, l_g is the total length of the air gaps, $\mu_0 = 4\pi * 10^{-7}\ H/m$ is the permeability of air and, $A_c = a * b$ is the cross sectional area of center



(a) (b)

Figure 3-1. One pair of single-phase EE cores: (a) geometry, (b) equivalent magnetic circuit.

post, which is also equal to two times the cross-sectional area of each outer post.

Another important design consideration for inductors is that the peak flux density in magnetic core (B_{pk}) should not exceed the maximum flux density (B_{max}), such that the intended operation can be ensured, and core saturation can be avoided. The peak flux density occurs at peak current, I_{pk}, and can be calculated by

$$B_{pk} = \frac{NI_{pk}}{A_c(R_{c,gap}+\frac{R_{o,gap}}{2})} = \frac{\mu_0 NI_{pk}}{l_g}. \quad (3\text{-}2)$$

To account for fringing effect, the magnetic circuit of single-phase EE core becomes Figure 3-2 (a). The extra magnetic reluctance, $R_{o,fr}$ and $R_{c,fr}$, is to model the effectively enlarged cross sectional area of the outer and center posts (shaded areas in Figure 3-2 (b)) due to fringing flux.

Considering the extra magnetic reluctance due to fringing effect, the inductance becomes

$$L = \frac{N^2}{R_{c,gap}//R_{c,fr}+\frac{R_{o,gap}//R_{o,fr}}{2}}. \quad (3\text{-}3)$$

a) Fringing effect model 1

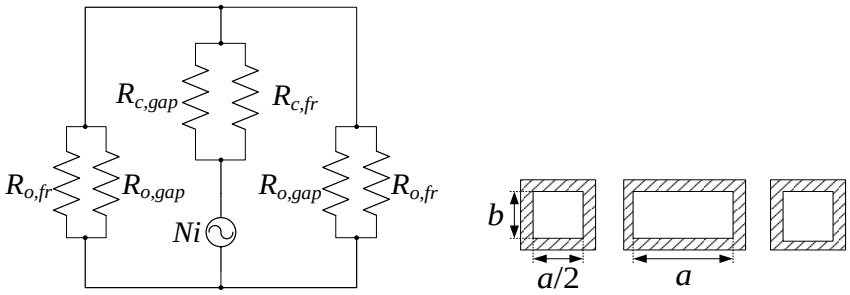
In the literature, some closed-form models have been proposed to calculate the enlarged cross-sectional area and reluctance of the air gap under the consideration of fringing effect [36, 85, 96, 97]. One model is to increase each edge of the cross section by the same amount as the length of air gap. In this case, the effective cross-sectional areas of the center post and outer posts become

$$A_{ce,c} = (a + l_g)(b + l_g), \quad (3\text{-}4)$$

and

$$A_{ce,o} = \left(\frac{a}{2} + l_g\right)(b + l_g). \quad (3\text{-}5)$$

Therefore, the total reluctance in the center and outer posts becomes



(a) (b)

Figure 3-2. Fringing effects: (a) magnetic circuit (b) cross sectional area of magnetic core (unshaded areas) and, enlarged cross sectional areas of outer legs and center leg (shaded area).

$$R_{c,total} = R_{c,gap} // R_{c,fr} = \frac{l_g/2}{\mu_0 A_{ce,c}}, \tag{3-6}$$

and

$$R_{o,total} = R_{o,gap} // R_{o,fr} = \frac{l_g/2}{\mu_0 A_{ce,o}}. \tag{3-7}$$

The maximum flux density in the center leg and outer legs are equal and can be calculated by

$$B_{o,pk} = B_{c,pk} = \frac{NI_{pk}}{A_c(R_{c,total} + \frac{R_{o,total}}{2})}. \tag{3-8}$$

b) Fringing effect model 2

Another approach was proposed in [85, 97], which calculates the reluctance based on Schwarz–Christoffel Transformation. In this method, the reluctance of a two-dimensional (2D) basic geometry was calculated. Then, other complex geometries can be decomposed into parallel and series combination of this basic geometry, and each part can be calculated. One typical 2D basic geometry is shown in Figure 3-3, and the per unit length reluctance for this basic geometry is

$$R_b = \frac{1}{\mu_0[\frac{w}{2l} + \frac{2}{\pi}(1 + \ln\frac{\pi h}{4l})]}. \tag{3-9}$$

Each air gap in the center and outer posts in single-phase EE cores can be decomposed into four basic geometries in both x- and y-directions. As an example, the center post in x-direction is shown in Figure 3-4. The 2D reluctance of the center leg in x- and y-directions can be calculated according to (3-9). The 2D fringing factors in these two directions ($F_{c\text{-}x}$ and $F_{c\text{-}y}$), which are defined by the ratio between reluctance with and without fringing effect considered, can be calculated by

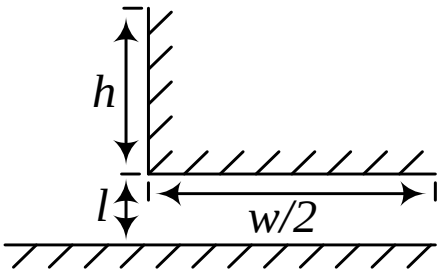
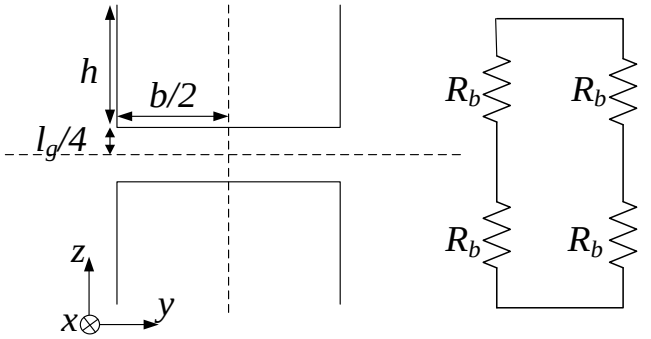


Figure 3-3. One 2D basic geometry for reluctance calculation.



(a) (b)

Figure 3-4. Decomposition of the center post of EE core into four 2D basic geometries: (a) center post in x-direction, (b) equivalent magnetic circuit.

$$F_{c-x} = \frac{R_b}{\frac{l_g}{\mu_0 \frac{2a}{}}} = \frac{2a/l_g}{\frac{2a}{l_g}+\frac{2}{\pi}\left(1+\ln\frac{\pi h}{l_g}\right)}, \tag{3-10}$$

and

$$F_{c-y} = \frac{R_b}{\frac{l_g}{\mu_0 \frac{2b}{}}} = \frac{2b/l_g}{\frac{2b}{l_g}+\frac{2}{\pi}\left(1+\ln\frac{\pi h}{l_g}\right)}. \tag{3-11}$$

The 3D fringing factor is obtained by multiplying the 2D fringing factors in x- and y-directions. Therefore, in the single-phase EE cores, 3D reluctance of the center post and outer posts are

$$R_{c,total} = R_{c,gap} // R_{c,fr} = F_c \mu_0 \frac{l_g}{2ab}, \tag{3-12}$$

where $F_c = F_{c-x}F_{c-y}$ is the 3D fringing factor of the center post, and

$$R_{o,total} = R_{o,gap} // R_{o,fr} = F_o \mu_0 \frac{l_g}{4ab}, \tag{3-13}$$

where $F_o = F_{o-x}F_{o-y}$ is the 3D fringing factor of the outer posts, and F_{o-x} and F_{o-y} are the 2D fringing factors of the outer posts in x- and y-directions, respectively.

In this model, the effective cross-sectional areas of the center and outer posts are

$$A_{ce,c} = \frac{l_g/2}{\mu_0 R_{c,total}}, \tag{3-14}$$

and

$$A_{ce,o} = \frac{l_g/2}{\mu_0 R_{o,total}}. \tag{3-15}$$

In method 2, the peak flux density can also be calculated by (3-8). Since the fringing flux effectively increases the cross-sectional area of the air gap and decreases the reluctance, the flux density increases, which has also been experimentally confirmed in [98, 99].

3.1.2 Proposed Design Procedures

The proposed design method can be divided into two parts. The first part is to use the equations discussed in 3.1.1 and systematically evaluate all the combinations of cores, turn numbers and air gap lengths. Then, under the given inputs and constraints, the optimal solution that has the least number of turns is selected for each core. The second part is to determine the wire gauge and output the final design based on thermal and/or loss considerations. The flowchart of the proposed design procedures is shown in Figure 3-5.

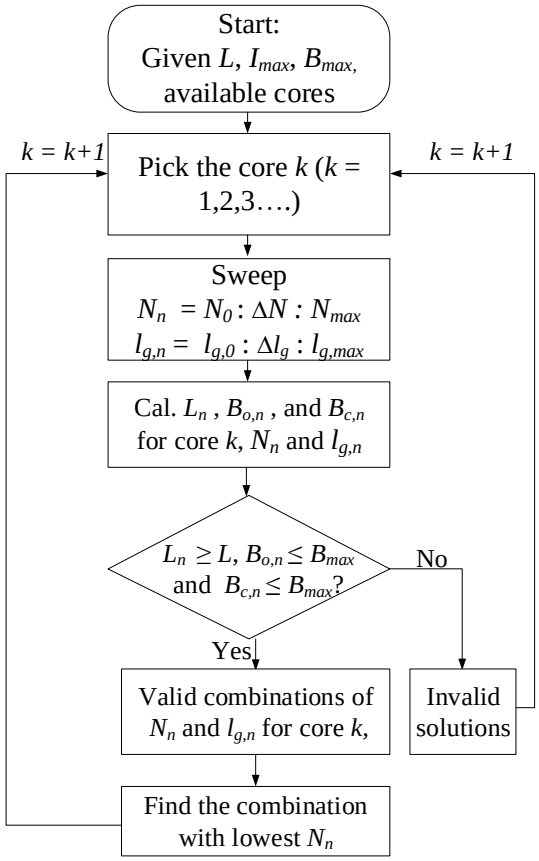
In Part 1, the design starts with the design objective of targeted inductance and the constraint of maximum allowed flux density. The peak current of the inductor and a database of magnetic cores are given as inputs. The following steps in Part 1 are:

Step 1.1: Pick the core *k*, from the database.

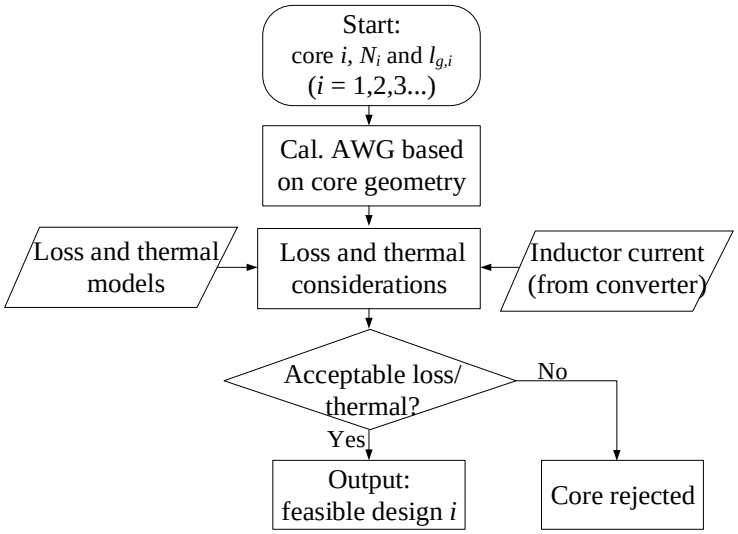
Step 1.2: For this core, sweep the turn number from the initial value (N_0) to the maximum possible turn number (N_{max}) with the step size of ΔN, and sweep the air gap length from the initial value ($l_{g,0}$) to the maximum possible length ($l_{g,max}$) with the step size of Δl_g. The initial values and step sizes can be small, e.g, $N_0 = \Delta N = 1$ and $l_{g,0} = \Delta l_g = 0.01$ mm, while the maximum values should be sufficiently large.

Step 1.3: For each combination of turn number and air gap length, calculate inductance and the peak flux density in center and outer legs based on (3-3) and (3-8). Depending on the selected inductor model, either (3-4) to (3-7) or (3-10) to (3-13) can be used.

Step 1.4: If the inductance and flux density calculated in Step 1.3 can meet the targeted inductance and flux density in each leg does not exceed B_{max}, then the combination is valid.



(a)



(b)

Figure 3-5. Design flow chart for an air-gapped inductor: (a) Part 1 and (b) Part 2.

Otherwise, the combination does not meet the constraints and is no longer considered. The design will move on to the next core, core $k + 1$, if no valid combination is found.

Step 1.5: For all the valid combinations of turn number and air gap length, select the one with the least number of turns, which is also the optimal design for core k. Note that other objectives can also be used in this step, such as selecting the combination that has the smallest air gap.

Step 1.6: Move to the next core, core $k + 1$, and return to Step 1.1 until every core in the database has been considered.

In Part 2, the valid combinations of cores, turn numbers and air gaps obtained in Part 1 are considered one by one. The wire gauge, loss and temperature are determined based on the core geometry and inductor current. There are four steps in Part 2:

Step 2.1: For each valid combination, select the thickest possible wire, i.e., the lowest AWG number, that satisfies the geometrical limitations, including the height and width of the core and bobbin, as well as insulation of wire.

Step 2.2: Calculate the copper and winding losses, and subsequently the temperature rise of inductors. In this step, the inductor current, which is determined by the converter operation, is needed as input. In addition, the loss and thermal models for the inductors are needed. To accurately calculate the loss and temperature, iteration is usually required since both core and winding losses are dependent on temperature.

Step 2.3: Output the feasible designs that meet the loss budget and/or thermal requirement. Otherwise, reject the core candidate.

Step 2.4: Finally, an optimal design can be selected from the feasible design set under a

given optimization objective, such as minimum loss, cost, size, etc.

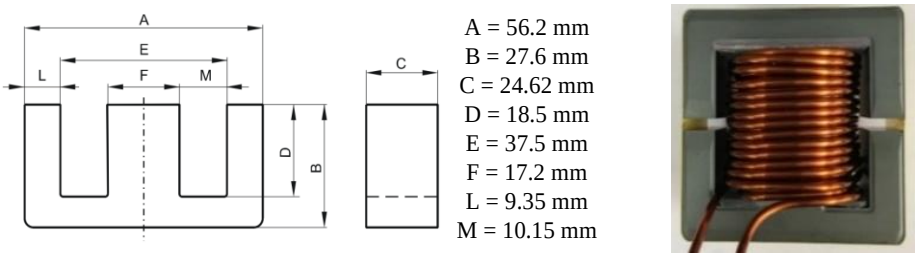
It should be noted that different types of core geometry can be included in the core database, and different thermal and loss models, such as those in [38, 39, 98-100], can also be used in Step 2.2 without changing the overall design procedures. Using this method, optimal inductor designs are calculated for a variety of core dimensions. This approach can be easily integrated into larger scale converter system design optimization studies. In [101] for example, a physics based meta-model is developed for a class of inductors to enable integrating inductor designs in a larger scale converter optimization. Such methods are valuable, but a simpler and more straightforward method is proposed in this work.

3.1.3 Models Verification and Methods Comparison

a) Verification of fringing effect models

A pair of single-phase ferrite EE cores 0R45530EC from Magnetics, Inc. was used as an example to verify the inductance models discussed in Section II. The magnetic wire was wound on the center leg in two layers and turn number is 30. The total length of air gaps, l_g, is swept between 2 mm to 10 mm. The core geometry and the inductor prototype are shown in Figure 3-6.

The calculated inductance and measurement results using different air gap lengths are shown in Figure 3-7. It can be seen that the models with fringing effect show better agreement with the measured values and have higher inductance compared to the model neglecting fringing effect. In other words, if fringing effect is considered in the design, it is possible to reduce the turn numbers and core size. Since both models can accurately predict the inductance, model 1 is used in the following two design examples.



(a) (b)

Figure 3-6. Inductor prototype using 0R45530EC: (a) geometry [102], (b) prototype.

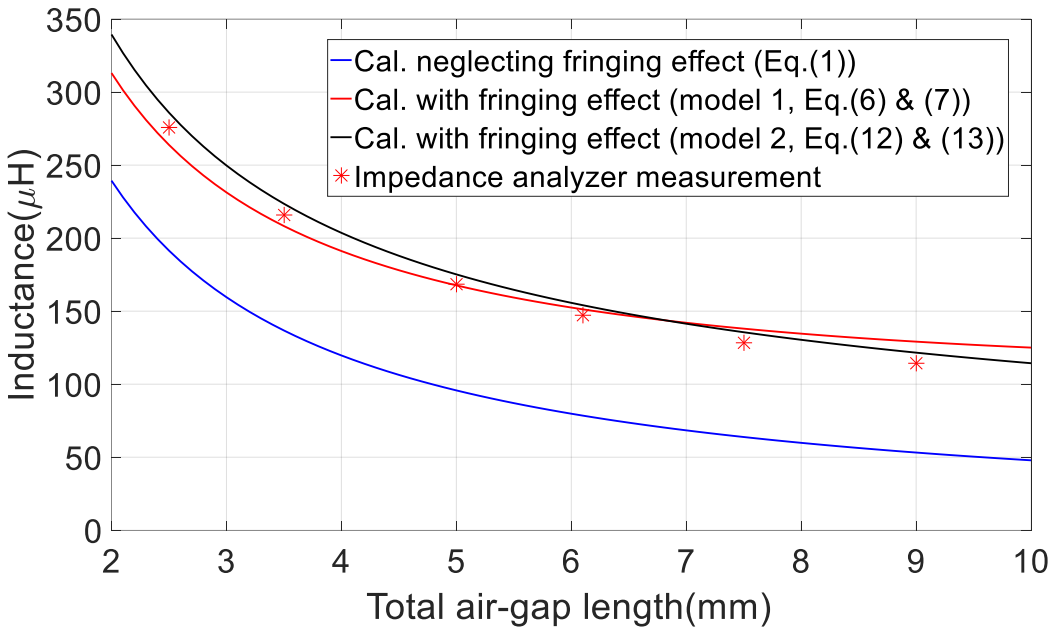


Figure 3-7. Measured and calculated inductance of the inductor prototype in Figure 3-6 using different models. Blue curve: calculation neglecting fringing effect; Red curve: calculation using model 1; Black curve: calculation using model 2; Red dots: measured results.

a) Design example 1

This design example aims to show that the proposed method can reduce turn number and core size compared to the conventional design method. The design requirement is based on [36]: L = 557 μH, I_{pk} = 1.51 A, B_{max} = 0.2 T, window utilization factor is 0.4, and current density of wire is below 5A/mm^2.

The design results from the conventional method and the proposed method are summarized in Table 3-1. For the conventional method, the inductor was designed by A_p method first, and then fringing factor was used to iteratively adjust the length of the air gap. It can be seen that the proposed method can reduce the turn number by 6% while achieving the same requirement. Theoretically, the core size can also be shrunk due to reduced turn number. In this case, the next smaller core is not large enough to meet the requirement.

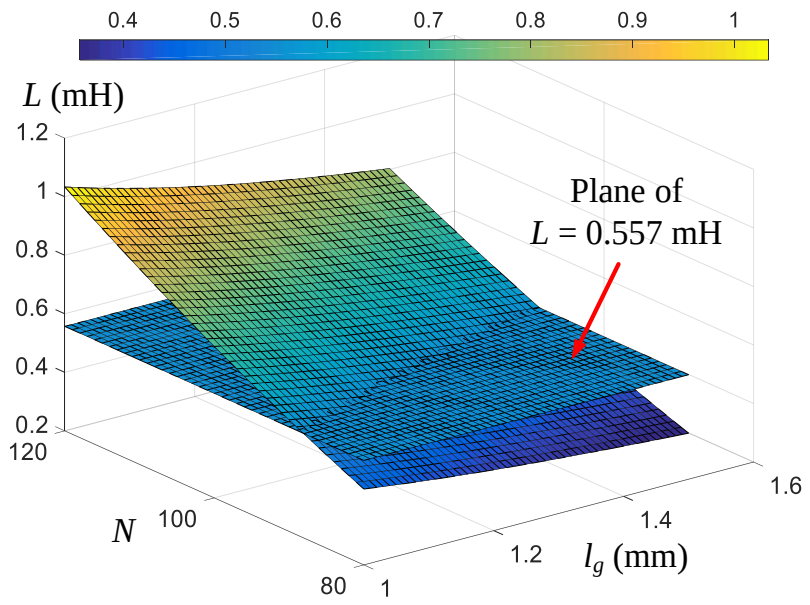
It should be noted that, the flux density in the conventional method is calculated by (3-2), which underestimates the peak flux density, and the calculated B_{pk} is lower than 0.2 T. However, B_{pk} becomes 0.223 T when (3-8) was used. Therefore, to have a fair comparison, B_{max} was adjusted to be 0.223 T for both methods.

The different results from the two design methods can be explained by examining the combinations of air gap lengths and turn numbers. For the selected core E 25/16/6, the inductance and peak flux density are shown in Figure 3-8, under a specific range of air gap lengths and turn numbers. The step size for turn number (ΔN) is set to one turn, and for air gap length (Δl_g) is 0.01 mm.

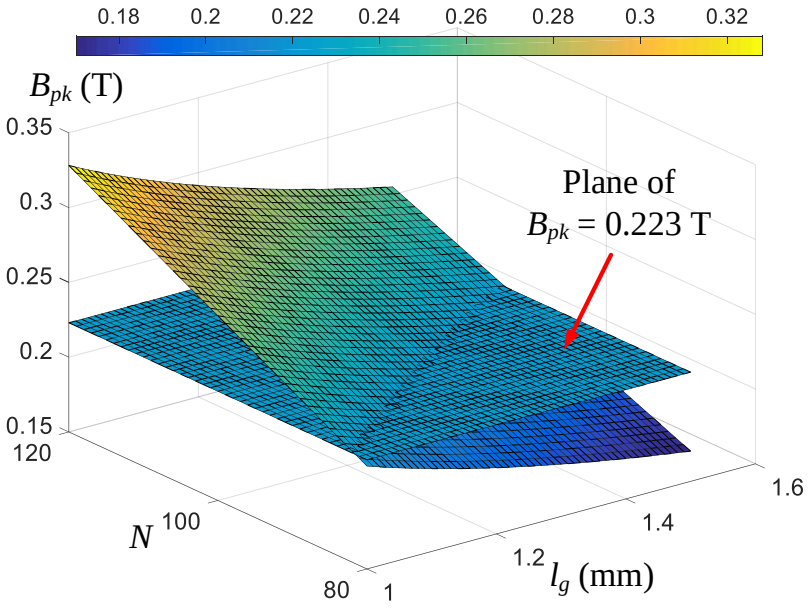
The valid combinations of N and l_g need to achieve inductance above 0.557 mH and have peak flux density below 0.223 T. These valid combinations are shown in Figure 3-9. From the plot, it can be observed that there are multiple combinations of turn number and air gap length that can

Table 3-1. Results of design example 1

	Conventional [36]	**Proposed**
Core type	E 25/16/6	E 25/16/6
Turn number	102	96
l_g **(mm)**	1.43	1.29
AWG	21	21
B_{pk} **(T)**	0.223	0.223

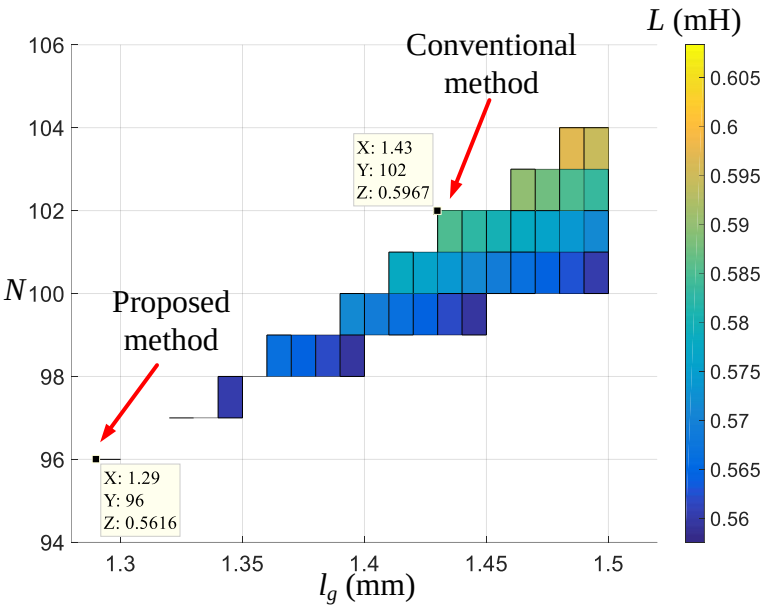


(a)

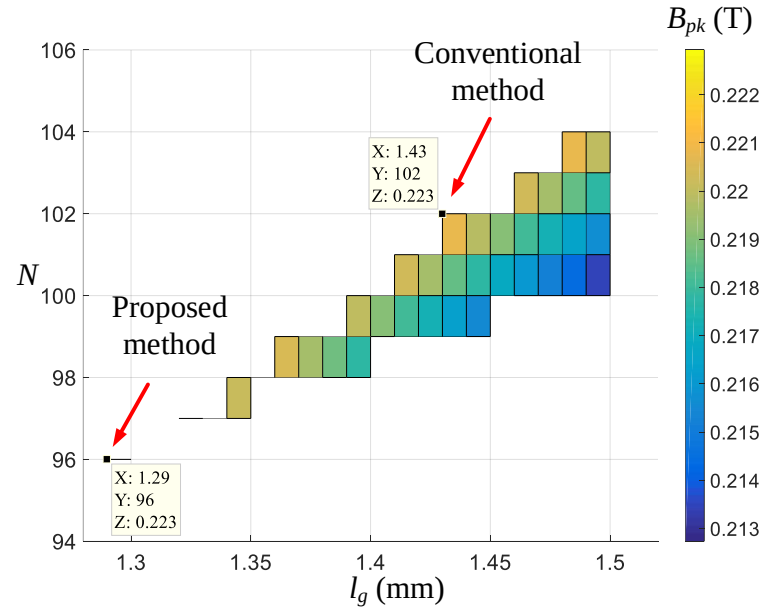


(b)

Figure 3-8. Calculated (a) inductance and (b) peak flux density using core E 25/16/6.



(a)



(b)

Figure 3-9. Valid combinations of N and l_g in design example 1: (a) inductance, (b) peak flux densities.

meet the design constraints. The conventional method finds one of the valid combinations, i.e., N = 102 and l_g = 1.43 mm. However, the least turn number is 96 and correspondingly, l_g is 1.29 mm, which can be obtained by the proposed method. This is because the conventional method only iteratively adjusts the length of the air gap, but turn number is unchanged. Therefore, one advantage of the proposed method over the conventional method is that the optimal combination can always be identified.

b) Design example 2

The second example aims to demonstrate that the conventional method can encounter issue of convergence or complex iteration while the proposed method can work effectively. The designed inductor is 80 μH, I_{pk} is 35 A and B_{max} is 0.37 T.

From Step 1.5, the minimum turn number and corresponding air gap length for each core are determined. In this study, 27 single-phase EE cores are considered. The results output from Step 1.5 are summarized in Table 3-2. For some of the cores (e.g., 1 ~ 18 and 22), no valid combination of turn number and air gap length is available. For example, the inductance value and maximum flux density for core 1 under different turn number and length of air gap are shown in Figure 3-10. It is obvious that there is not valid combination of turn number and air gap length that can meet both inductance and flux density requirement. For cores 19 ~21 and 23~27, valid combinations are available. As an example, the calculated results for core 19 are plotted in Figure 3-11. The valid combination for core 19 will be examined later.

The second part of the design is to calculate the AWG number for each valid core, and find the optimal design with consideration of the temperature rise and/or loss of the core and winding. For the valid cores, the lowest AWG number is calculated based on the height and width of core window, which is summarized in Table 3-3. In this work, the total height of winding is limited to

Table 3-2. Combinations of minimum turn number and corresponding air gap length from Step 1.5

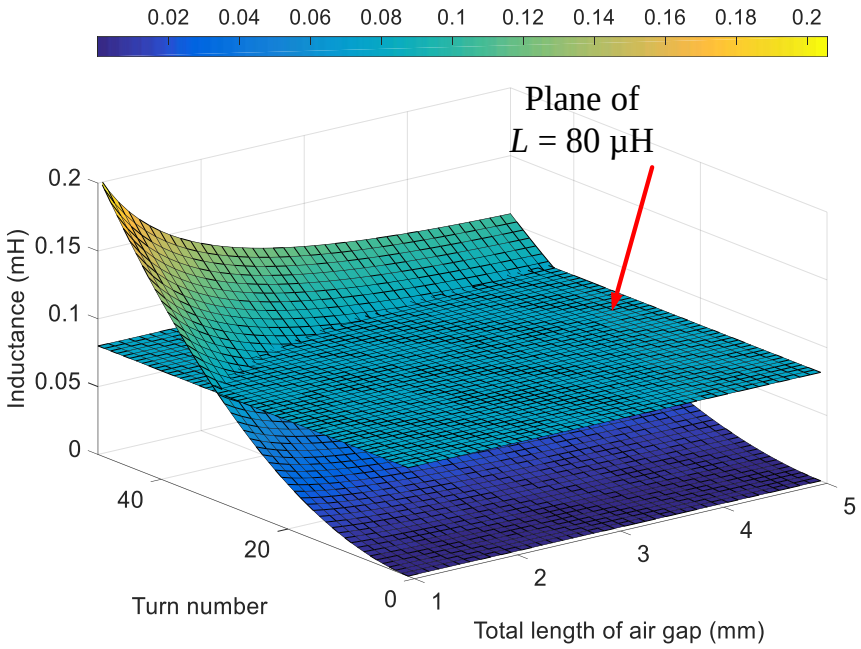
Core index	**Core size**	**Output at Step 1.5**		**Inductance (μH)**	**Peak flux density at I_{pk} (T)**
		Min. turn number	l_g (mm)		
1	E 19/8/10	N/A	N/A	N/A	N/A
2	E 25/10/7	N/A	N/A	N/A	N/A
3	E 25/13/7	N/A	N/A	N/A	N/A
4	E 25/16/6	N/A	N/A	N/A	N/A
5	E25/10/13	N/A	N/A	N/A	N/A
6	E 25/13/11	N/A	N/A	N/A	N/A
7	E 25/16/13	N/A	N/A	N/A	N/A
8	E 31/15/7	N/A	N/A	N/A	N/A
9	E 31/13/9	N/A	N/A	N/A	N/A
10	E 34/14/9	N/A	N/A	N/A	N/A
11	E 35/21/9	N/A	N/A	N/A	N/A
12	E 40/17/11	N/A	N/A	N/A	N/A
13	E 42/21/9	N/A	N/A	N/A	N/A
14	E 43/21/15	N/A	N/A	N/A	N/A
15	E 43/21/20	N/A	N/A	N/A	N/A
16	E 42/33/20	N/A	N/A	N/A	N/A
17	E 41/17/12	N/A	N/A	N/A	N/A
18	E 47/20/16	N/A	N/A	N/A	N/A
19	E 56/28/21	22	4.5	83.9	0.37

Table 3-2 continued

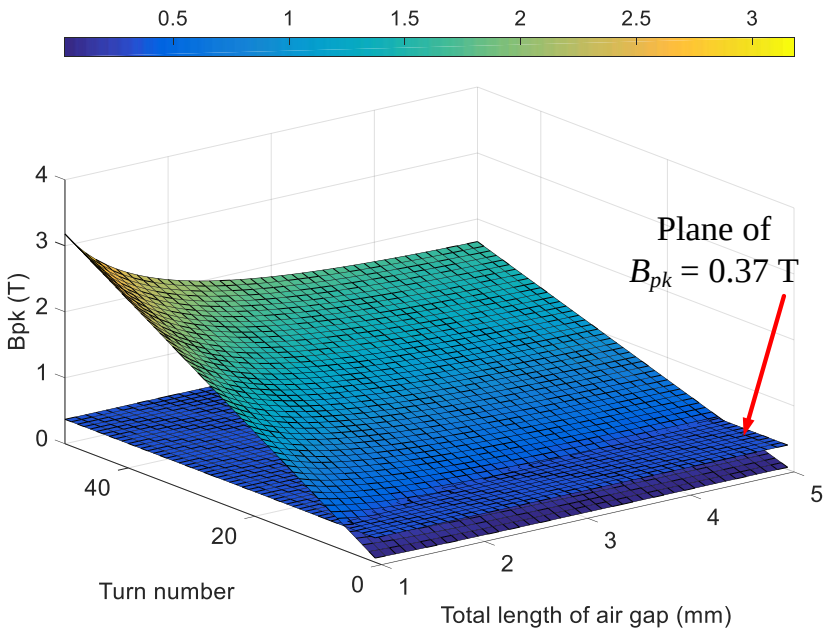
Core index	**Core size**	**Output at Step 1.5**		**Inductance (μH)**	**Peak flux density at I_{pk} (T)**
		Min. turn number	l_g (mm)		
20	E 56/28/25	19	3.5	83.5	0.36
21	E 56/24/19	22	4.3	82.2	0.37
22	E 60/22/16	N/A	N/A	N/A	N/A
23	E 65/32/27	15	2.3	85.2	0.36
24	E 70/33/32	12	1.7	88.8	0.37
25	E 72/28/19	22	4.3	83.3	0.37
26	E 80/38/20	20	3.8	82.6	0.37
27	E 100/59/27	11	1.5	87.4	0.37

Table 3-3. Lowest AWG number for the valid cores

Core index	**Core size**	**Minimum Turn number**	**Air gap length (mm)**	**Lowest AWG number**
19	E56/28/21	22	4.5	10
20	E 56/28/25	19	3.5	9
21	E 56/24/19	22	4.3	12
23	E 65/32/27	15	2.3	7
24	E 70/33/32	12	1.7	7
25	E 72/28/19	22	4.3	8
26	E 80/38/20	20	3.8	10
27	E 100/59/27	11	1.5	11

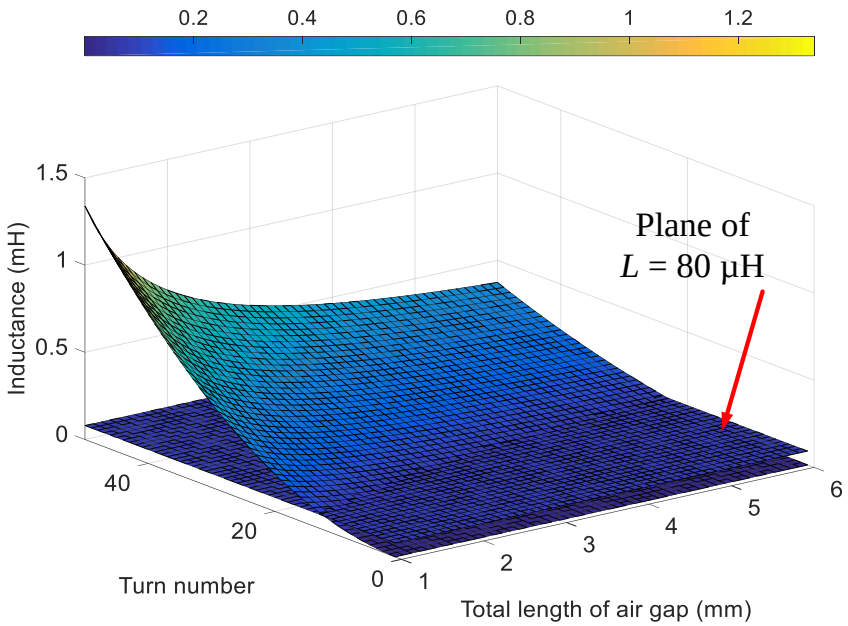


(a)

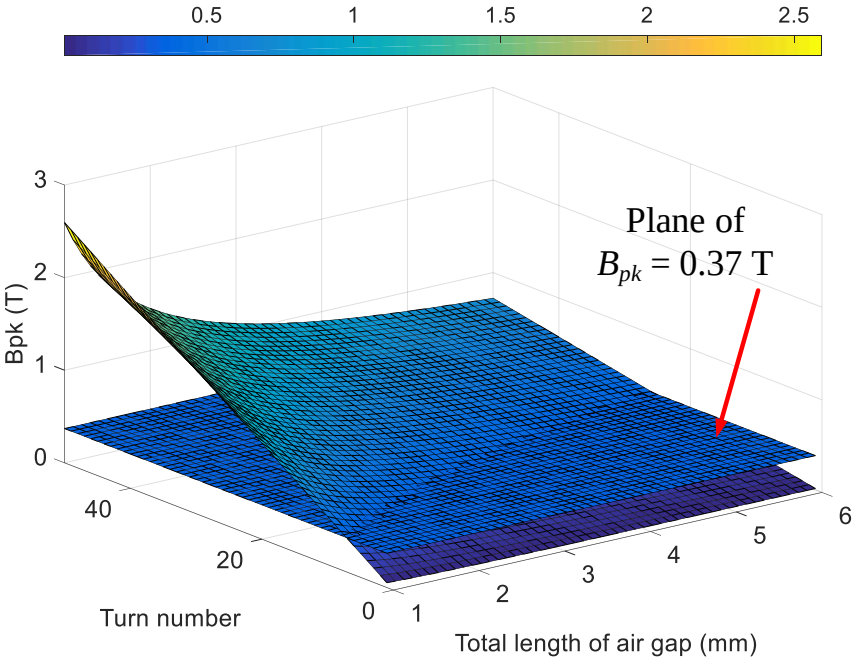


(b)

Figure 3-10. Calculated (a) inductance and (b) peak flux density of core 1 (E 19/8/10).



(a)



(b)

Figure 3-11. Calculated (a) inductance and (b) peak flux density using core 19 (E 56/28/21).

80% of the height of the core window, and total width of winding is limited to 60% that of the core window. Some other criteria such as form factor of the window area can also be used depending on the applications.

Since the thermal and loss models are not the focus in this study, wire of AWG 10 was selected for thermal and loss consideration. Thus, cores 19, 20, 23, 24, 25 and 26 can meet the requirement. Core 19 is considered as the optimal design as it can achieve the smallest core size. The design results from the conventional method and the proposed method are summarized in Table 3-4.

The results for design example 2 can also be examined in the same way as example 1. Valid combinations for core E 56/28/21 are plotted in Figure 3-12. It can be seen that the proposal method successfully identifies the optimal combination of N and l_g.

3.2 Design and Optimization of Ac-side Filter using Coupled and Non-coupled Inductors

3.2.1 Modeling of Output Filter

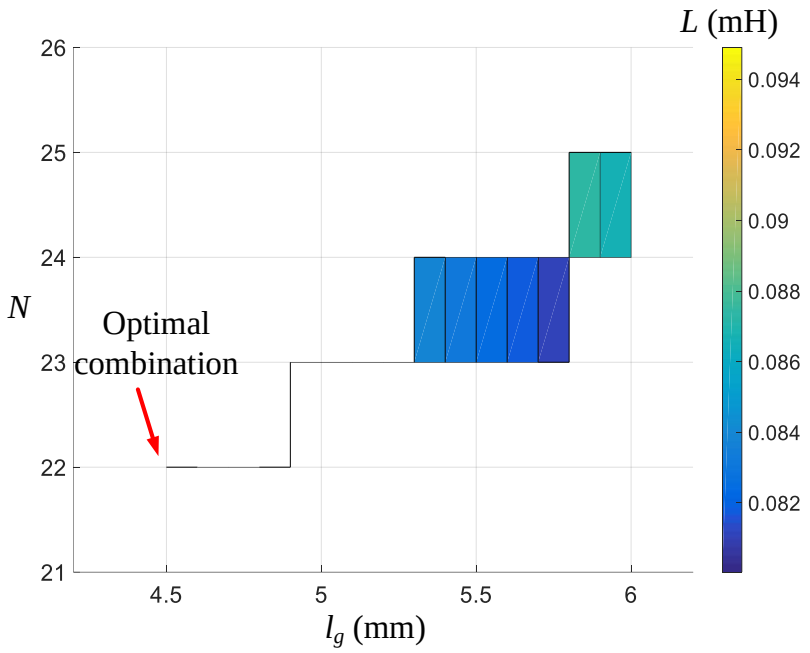
The converter and filter topology discussed is shown in Figure 2-1, the specifications of the converter are summarized in Table 3-5. The filter topology is *LCL* with passive damping. The capacitance is formed by two capacitors connected in series. The midpoint of the ac-side capacitors is connected to the midpoint of the dc-link capacitors. This connection forms a bypass path for the leakage current, and effectively reduces the CM noise. The load-side inductors are provided by the EMI filter (L_{dm1} and L_{dm2}). For the converter-side inductors, both coupled inductors (L_{cp1} and L_{cp2}) and non-coupled inductors (L_{1_1} and L_{1_2}) are used, which determines EMI attenuation and the current ripple appearing in inductors. To ensure symmetrical operation, coupled and non-coupled

Table 3-4. Results of design example 2 using the conventional and proposed methods

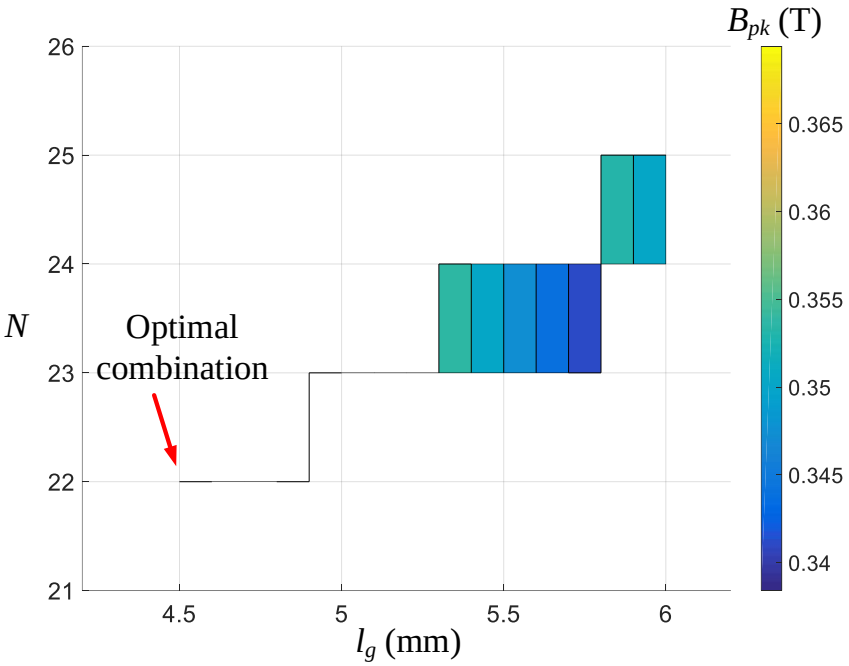
	Conventional method	**Proposed method**
Core type	E 65/32/27	E 56/28/21
Core size (mm^3)	79000	44000
Turn number	24	22
l_g (mm)	N/A due to divergence	4.5
AWG	10	10
Measurement (μH)	N/A	82.1 @ 60Hz; 77.9 @100k Hz

Table 3-5. Specifications of the inverter

Input voltage (V_{in})	450 V
Output Voltage (V_o)	210 - 230 V_{rms}
Output power (P_o)	0 - 4.5 kW
Switching frequency (f_{sw})	135 kHz
Modulation	Unipolar
Switches (S1A ~ S2B)	IGOT60R070D1



(a)



(b)

Figure 3-12. Valid combinations of N and l_g in design example 2 using core E 56/28/21: (a) inductance, (b) peak flux densities.

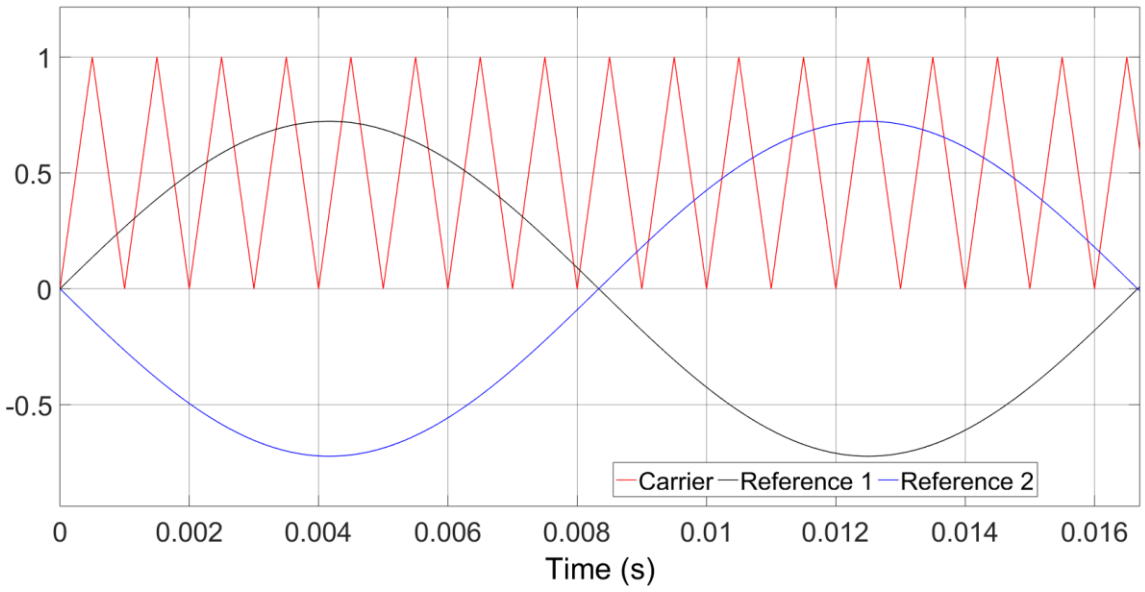
inductors in phase legs *A* and *B* are designed to be identical, i.e., $L_{1_1} = L_{1_2} = L_1$, and $L_{cp1} = L_{cp2} = L_{cp}$.

Unipolar modulation is used to reduce the current ripple and inductance value. The switching signals for four switches (S1A, S2A, S1B, and S2B) are generated by comparing the high-frequency triangle carrier wave with two sinusoidal references which are 180 º out of phase. For illustration purpose, unipolar modulation with 1 kHz switching frequency is shown Figure 3-13. The switching signals for S1A and S2A are complimentary and generated by comparing carrier and reference 1. Similarly, switching signals for S1B and S2B are generated by comparing carrier and reference 2.

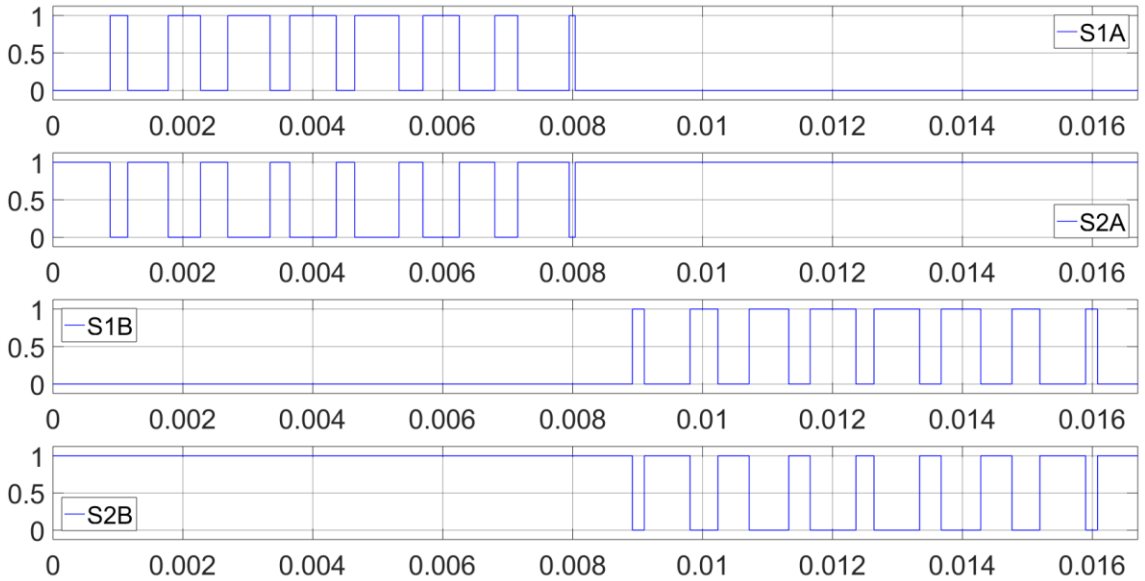
In the output filter, the capacitors are designed based on the 5% reactive power requirement, and the damping resistors are designed to reduce the oscillation between inductors and capacitors. There are two parameters to be discussed in detail: converter-side non-coupled inductor L_1, and the ratio between L_{cp} and L_1 ($k = L_{cp}/L_1$).

Due to the symmetric operation, only the current in L_{1_1} (i_{L1_1}) is discussed. The current in L_{1_2} is 180° phase shift of i_{L1_1}. During the positive ($0 < t < \frac{T}{2}$) and negative half cycle ($\frac{T}{2} < t < T$), the impedance between node *A* and nodes *B/Mid* is shown in Figure 3-14. At switching frequency and above, the impedance of capacitors is relatively small compared to that of the inductors, and it is therefore neglected in the model.

The impedance also determines the instantaneous current in L_{1_1}. During the positive half cycle, $i_{L1_1}(t)$, which consists of high frequency ripple current and line frequency fundamental current, is



(a)



(b)

Figure 3-13. Unipolar modulation for converter in Figure 2-1: (a) carrier and reference waveforms; (b) switching signals for four devices.

$$i_{L1_1}(t) = \alpha \frac{V_{dc} d(t)(1-d(t))}{L_1 f_{sw}} + I_{o,pk} \sin(2\pi f t) \text{ for } (0 \le t < \frac{T}{2}), \quad (3\text{-}16)$$

where $\alpha = \frac{L_1 + L_{cp}}{2L_{cp} + L_1}$, $d(t)$ is the duty cycle of phase leg *A*, and $I_{o,pk}$ is peak of load current.

Similarly, during the negative half cycle, $i_{L1_1}(t)$ becomes

$$i_{L1_1}(t) = \beta \frac{V_{dc} d(t)(1-d(t))}{L_1 f_{sw}} + I_{o,pk} \sin(2\pi f t) \text{ for } \left(\frac{T}{2} \le t < T\right), \quad (3\text{-}17)$$

where $\beta = \frac{L_{cp}}{2L_{cp} + L_1}$.

The current in the middle return path, $i_{mid}(t)$, is

$$i_{mid}(t) = \gamma \frac{V_{dc} d(t)(1-d(t))}{L_1 f_{sw}}, \quad (3\text{-}18)$$

where $\gamma = \alpha - \beta = \frac{L_1}{2L_{cp} + L_1}$.

According to (3-16) to (3-18), the maximum peak-to-peak current ripple of $i_{L1_1}(t)$ and $i_{mid}(t)$ occurs when $d(t) = 0.5$:

$$I_{L1_1,ripple,max} = \alpha \frac{V_{dc}}{4L_1 f_{sw}}, \quad (3\text{-}19)$$

and

$$I_{mid,ripple,max} = \gamma \frac{V_{dc}}{4L_1 f_{sw}}. \quad (3\text{-}20)$$

Current $i_{mid}(t)$ is used for calculation of the flux density and core loss of L_{cp}, since it equals to the sum of the currents in two windings. Current $i_{L1_1}(t)$ is used for calculation of the winding loss of L_{cp}.

The differential mode (DM) impedance between node *A* and *B* can also be derived from Figure 3-14:

$$L_{dm} = \frac{L_1}{\alpha}, \quad (3\text{-}21)$$

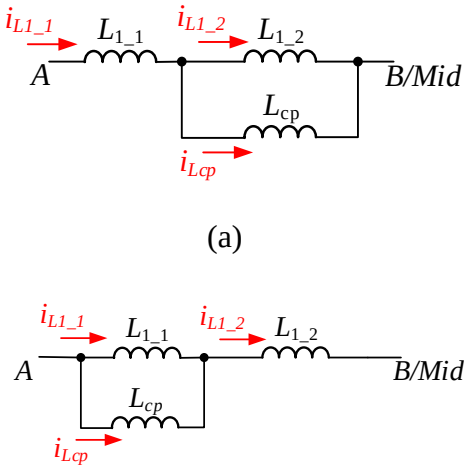


Figure 3-14. Impedance between node *A* and nodes *B/Mid* of the converter in Figure 2-1 during (a) positive half of line cycle (b) negative half of line cycle.

The equivalent circuit for CM noise is shown in Figure 3-15, and the CM mode impedance from node *A/B* to node *Mid* is approximated by

$$L_{cm} = \frac{L_1}{2} + L_{cp}. \tag{3-22}$$

The equations (3-16) to (3-20) are verified by simulation using MATLAB/SIMULINK. shows the simulated current waveforms at steady state in three cases (k = 0, 1, 10). The results from calculation and simulation are summarized Figure 3-16 and compared in Table 3-6.

From the above results, it can be seen that for the given L_1, if L_{cp} increases, the equivalent impedance in the middle return path increases. Thus, the high frequency current ripple tends to flow in L_{1_1} and L_{1_2}, rather than the middle return path. In such case, the sum of currents in two windings of the coupled inductor also decreases. This reduces the loss of L_1, as well as core loss of L_{cp}, and is beneficial for the EMI performance. However, larger L_{cp} also requires more turns and incurs more winding loss for L_{cp}. Considering the tradeoff among these factors, a holistic design considering both the coupled and non-coupled inductors is necessary.

3.2.2 Design and Optimization

To design an optimal filter for the inverter, physical models of the inductors, such as loss, size, weight and temperature rise, need to be incorporated as design objectives and constraints. In this study, the total weight of inductors, including the magnetic cores and magnet wire, is used as the design objective. The core loss density is calculated by using Generalized Steinmetz's Equation (GSE) [103]:

$$P_{core} = \frac{1}{T}\int_0^T k \left|\frac{dB}{dt}\right|^{\alpha} |B(t)|^{\beta-\alpha} dt, \tag{3-23}$$

where T is the line frequency (60Hz); k, α, and β are Steinmetz parameters from datasheet.

Due to fringing effect, the increase of effective cross-sectional area and flux density is

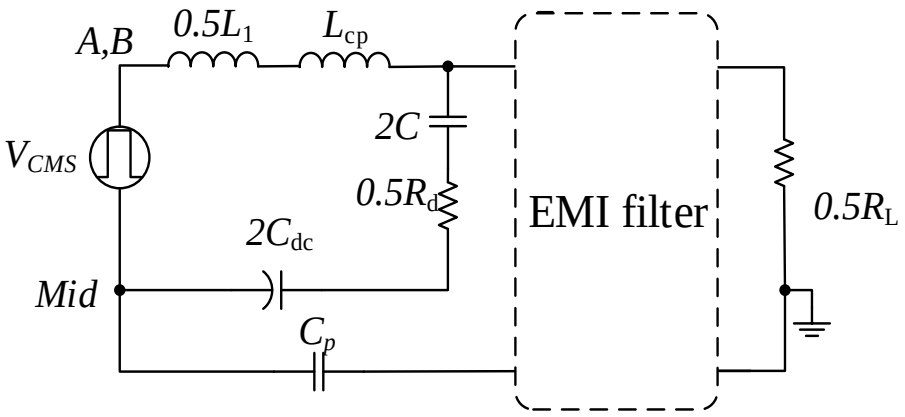
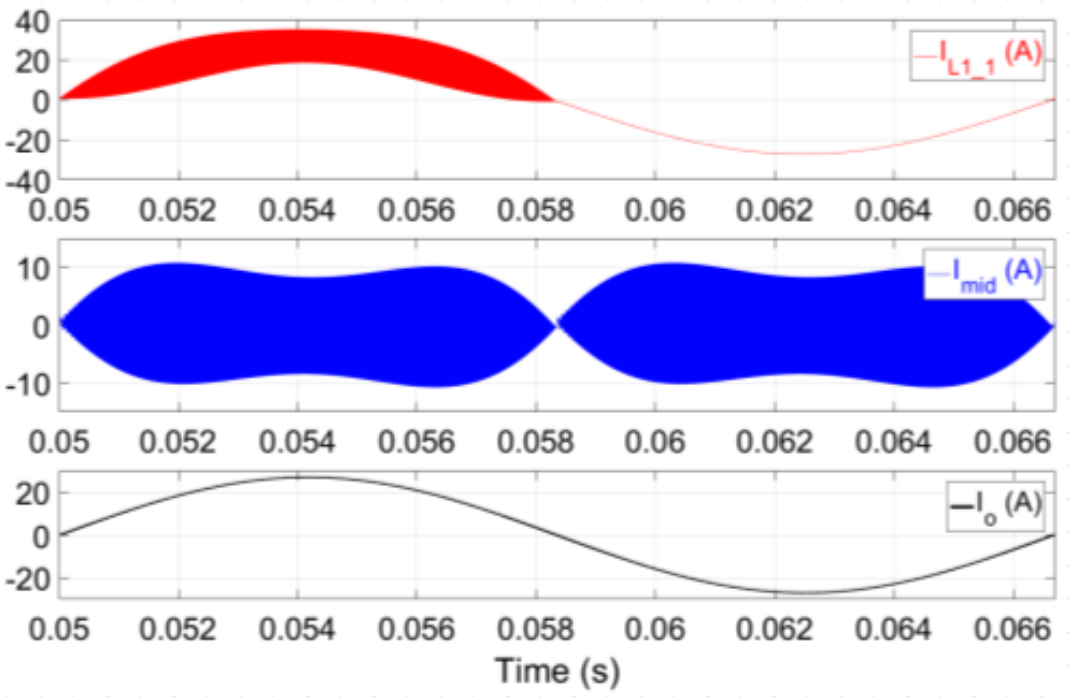
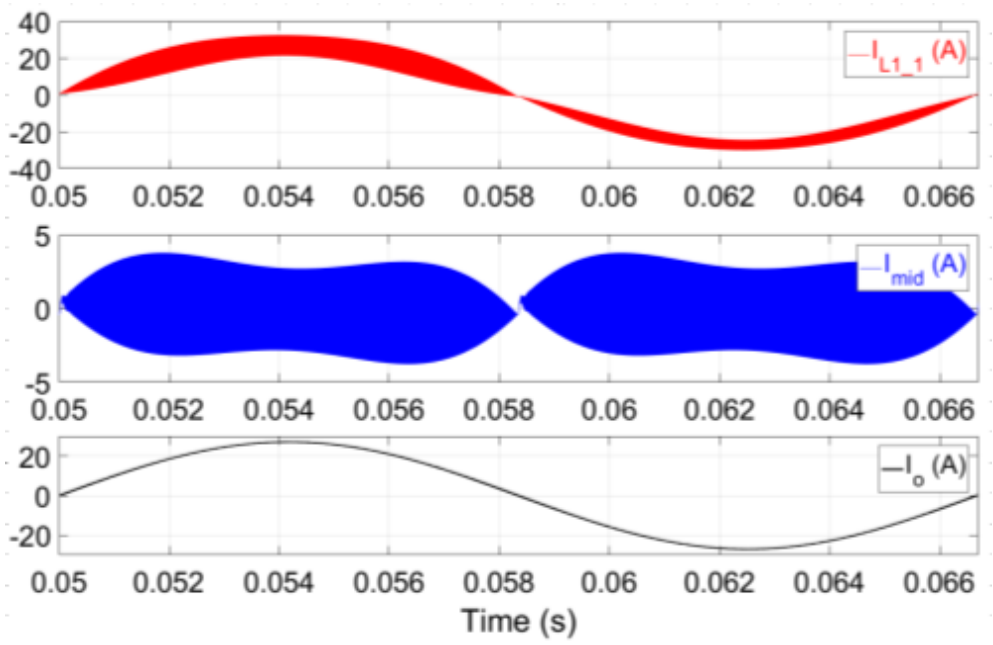


Figure 3-15. Equivalent circuit for CM noise.

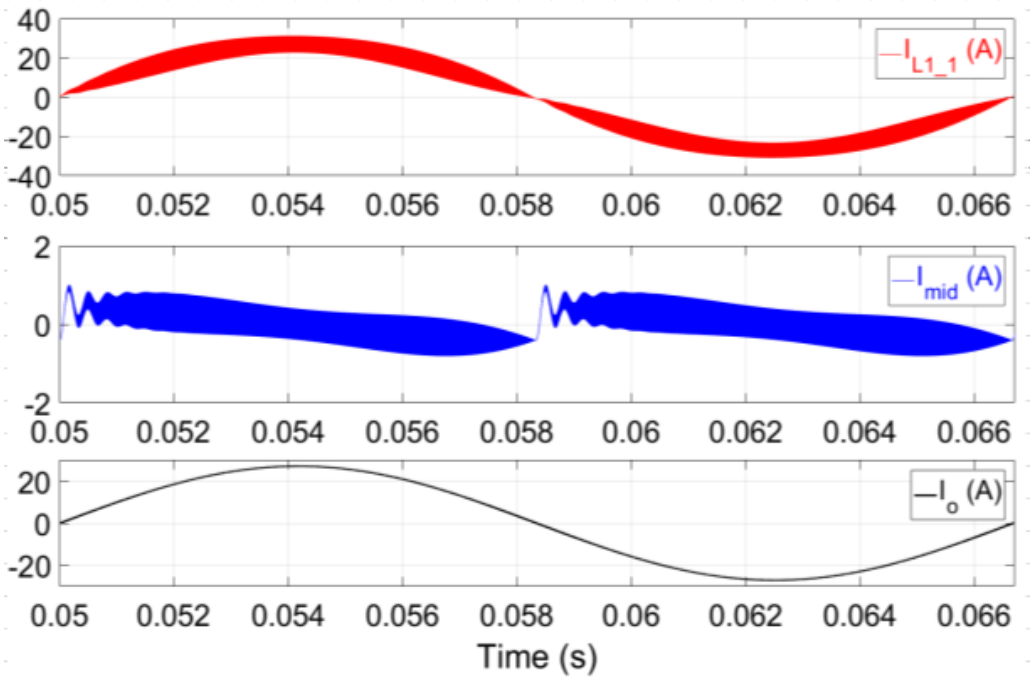


(a)

Figure 3-16. Simulated current waveforms of non-coupled inductor L_{1_1}, middle return path and ac output for converter in Figure 2-1, using (a) k = 0, (b) k = 1, and (c) k = 10. In all three cases, L_1 = 40 μH, V_{in} = 450V, V_o = 230Vrms, P_o = 4.5 kW.



(b)



(c)

Figure 3-16 continued.

Table 3-6. Summary of calculation and simulation results

k		*k = 0*	*k = 1*	*k = 10*
L_1		40 μH	40 μH	40 μH
L_{cp}		0 μH	40 μH	400 μH
α		1	2/3	≈ 1/2
β		0	1/3	≈ 1/2
γ		1	1/3	≈ 0
$I_{L1_1,ripple,max}$	**Cal.**	20.8 A	13.9 A	10.9 A
	Sim.	20.6 A	14.0 A	10.8 A
$I_{mid,ripple,max}$	**Cal.**	20.8 A	6.9 A	1.0 A
	Sim.	20.5 A	6.9 A	1.0 A

considered. The flux density used in (3-23) is

$$B = \frac{\mu_o N(a+l_g)(b+l_g)}{abl_g} i, \tag{3-24}$$

where a and b are the length and width of the cross section of winding post, l_g is the total length of air gap, and i is the current of the inductor.

The winding loss at each frequency is calculated by Dowell's Equation [37, 104]:

$$R_w = R_{wDC} A[\frac{\sinh(2A)+\sin(2A)}{\cosh(2A)-\cos(2A)} + \frac{2(N_l^2-1)}{3}\frac{\sinh(A)-\sin(A)}{\cosh(A)+\cos(A)}], \tag{3-25}$$

where $R_{wDC} = \rho_w MN/A_w$ is the dc resistance of conductor; ρ_w is specific resistivity of copper; M is mean length per turn; N_l is number of turns; A_w is cross-sectional area of conductor; $A = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \frac{d}{\delta_w}\sqrt{\frac{d}{p}}$ for round conductor; d is diameter of conductor; $\delta_w = \sqrt{\rho_w/\pi\mu_0 f}$ is the skin depth of conductor at the frequency under consideration; p is the distance between the centers of the adjacent winding round conductor in the same layer; and μ_0 is permeability of free space, $4\pi \times 10{-}7$ H/m.

The temperature rise of inductor ($\triangle T_{ind}$) under natural convection is estimated by the empirical equation [44, 105]:

$$\Delta T_{ind} = \left(\frac{P_{total}}{A_T}\right)^{0.833}, \tag{3-26}$$

where P_{total} is the total loss of inductor including core and winding losses, and A_T is the surface area of inductor in cm^2.

In the design process, L_1 is swept from 40 μH to 100 μH with the step size of 2 μH. The ratio between L_{cp} and L_1 ranges from 0 to 5. Single-phase EE cores are used for the design of non-coupled inductors, and U cores are used for coupled inductor. The maximum flux density for L_1 is limited to 0.35 T, while it is 0.25 T for L_{cp}. Although a higher limit can be used for L_{cp}, it leads to

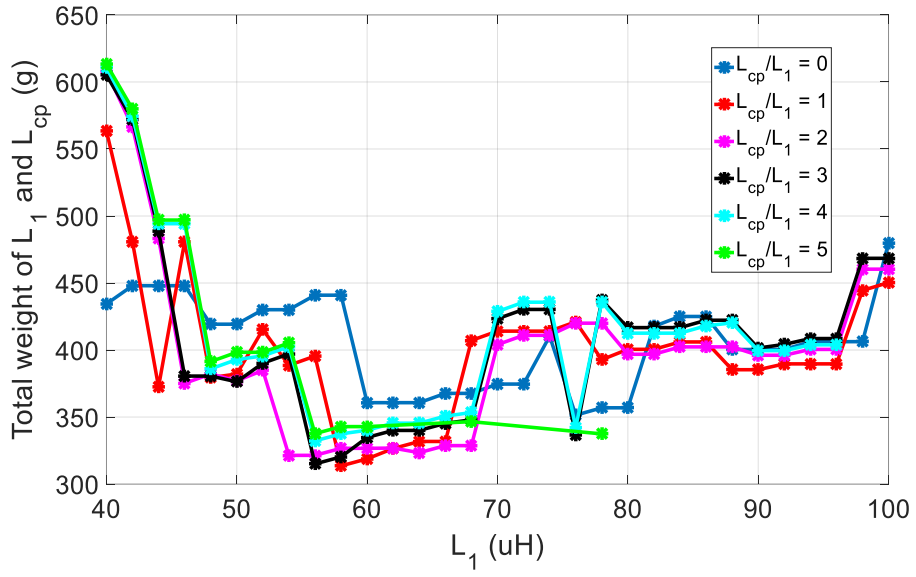
small air gap, which is hard to control precisely in the implementation. The maximum allowable temperature rise is limited to 45 °C.

For each combination of L_1 and L_{cp}, the design process sweeps the magnetic cores and wire gauges in the database. It selects the design that meets the thermal constraints and has the lightest weight for this specific set of L_1 and L_{cp}. The loss of L_1 and L_{cp} is also recorded.

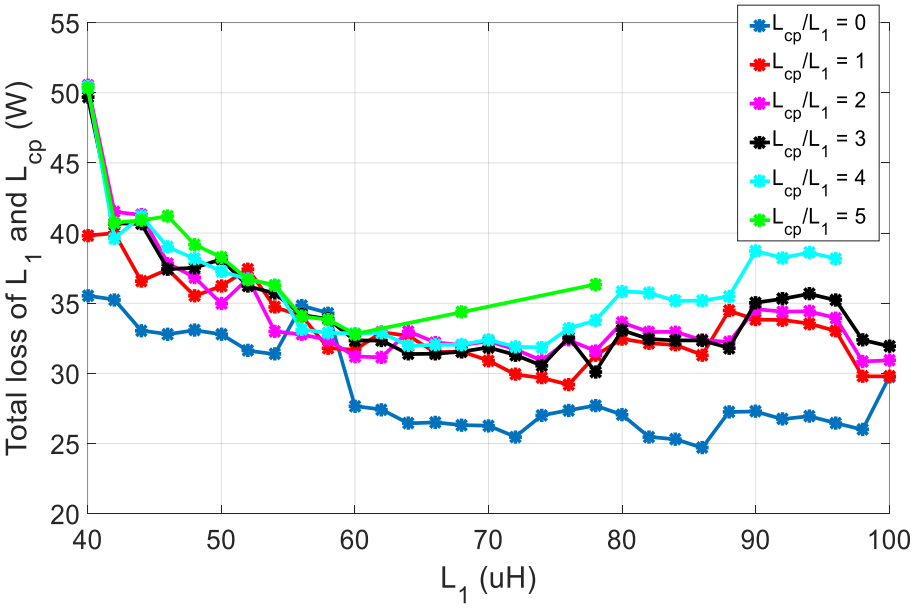
Total weight and total loss of the selected designs are summarized in Figure 3-17 and Figure 3-18. In general, both weight and loss are high when L_1 is too small or too large. When L_1 is small, the magnitude of high-frequency ripple current is high, which causes high winding and core losses for L_1 and L_{cp}. To meet the temperature rise constraint, this can lead to thicker wire and larger core size. When L_1 becomes large, the required core size and turn number also increase. This also results in higher loss and weight.

As can be seen from Figure 3-17(a), adding L_{cp} can effectively reduce the total weight of the inductors at certain range. This is because the flux density in L_{cp} is generated by the sum of currents in two windings, which can be relatively small. So, L_{cp} can be implemented by small air gap and small magnetic cores. Using such L_{cp} only adds small weight, but it can reduce the weight of L_1 by lowering the loss and wire gauge. In Figure 3-17(b), the total loss of inductors increases with larger ratio of L_{cp} and L_1. This is mainly due to the winding loss of L_{cp}. More winding is needed to implement larger L_{cp}, and the winding of L_{cp} needs to conduct the main current.

Design #1 is regarded an optimal design because the lightest weight is achieved. Design #2 is selected as a reference for comparison purpose, since it does not use a coupled inductor. The two selected designs are summarized in Table 3-7.



(a)



(b)

Figure 3-17. (a) Total weight, and (b) total loss for each combination of L_{cp} and L_1 for the ac-side output filter.

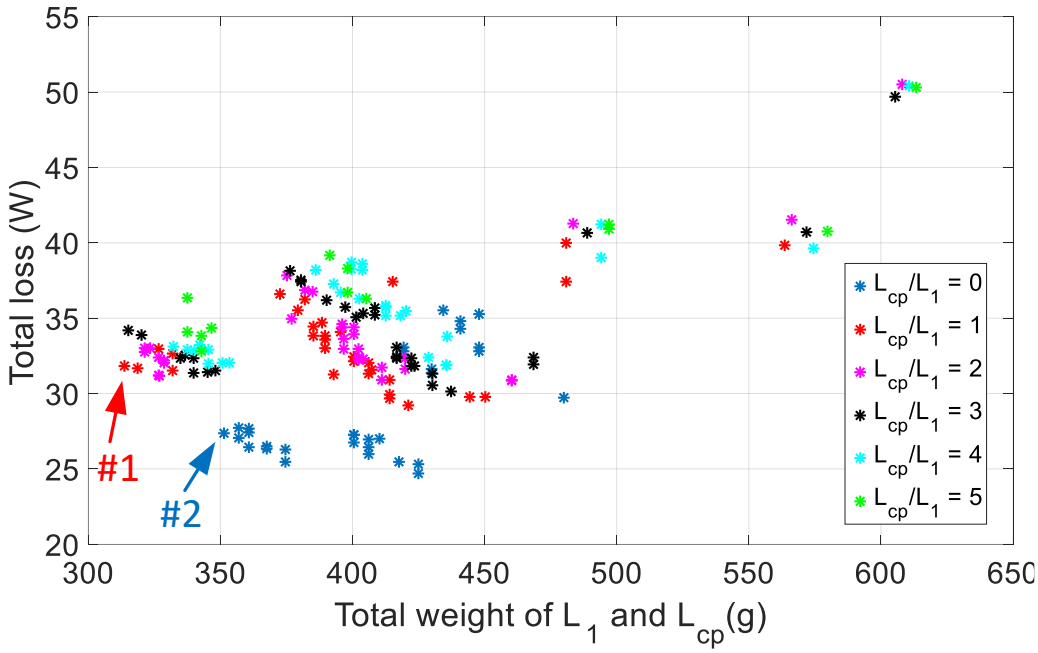


Figure 3-18. Total weight and total loss for each combination of L_{cp} and L_1 for the ac-side output filter.

Table 3-7. Summary of two selected designs for the ac-side output filter

Design results	**#1**	**#2**
***k* (L_{cp}/L_1)**	1	0
L_1 (µH)	58	76
L_{cp} (µH)	58	0
$L_{dm,eq}$ (µH)	87	76
$L_{cm,eq}$ (µH)	87	38
L_1 and L_{cp} total weight (g)	313.6	351.4
L_1 and L_{cp} total loss @ 4.5 kW (W)	31.8	27.7

3.2.3 Experimental Results

Based on the designs selected in the previous section, two sets of filters are implemented. The inductors in these two designs are shown in Figure 3-19, and the parameters of the inductors are summarized in Table 3-8.

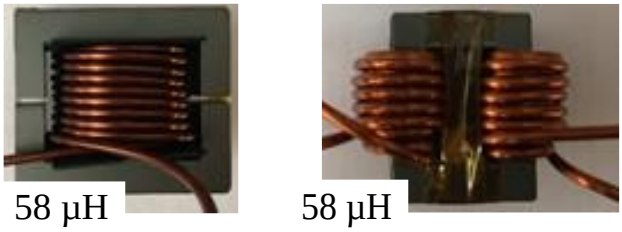
As shown in Figure 3-20, a 4.5-kW single-phase inverter using GaN devices was built to test the filters. The measured current waveforms at V_{dc} = 450 V, V_o = 230 V_{rms} and P_o = 4.5 kW are shown in Figure 3-21. To have a fair comparison between two designs, the same EMI filter was used.

To verify the EMI performance of these two designs, the same EMI filter was added. The measurement was setup according to FCC part 15 class B. The measured CM and DM noise in the two designs are summarized in Figure 3-22. Design #1 achieves much lower CM noise because by using L_{cp}, the equivalent CM inductance is much larger than Design #2. As for the DM, both designs have similar DM equivalent inductance and DM performance.

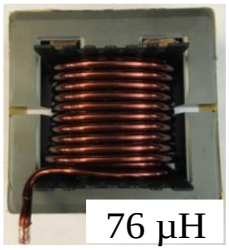
The measured converter losses for the two designs at P_o = 4.5 kW are 142.5 W (Design #1) and 138.6 W (Design #2). The loss difference between the two designs is very close to the expected value of 4.1 W.

3.3 Summary

The first part of this chapter proposes a simple and improved design method for gapped inductors. The method considers fringing effect and its impacts on the inductance and flux density. The proposed method sweeps the available cores and finds an optimal combination of turn number and air gap length that satisfies design requirements. It is shown that the method considers the possible reduction in turn number and core size. The method also features a small number of



(a)



(b)

Figure 3-19. Inductors for the ac-side output filter, (a) Design #1, and (b) Design #2.

Table 3-8. Parameters of inductors for the ac-side output filter

Inductors	***L*₁ in Design #1**	***L*_{cp} in Design #1**	***L*₁ in Design #2**
Core	E 56/24/19	9077025002	E55/28/21
Turn number	18	11	22
AWG of winding	10	12	10
Total length of air gap	3.8 mm	0.5 mm	4.5 mm

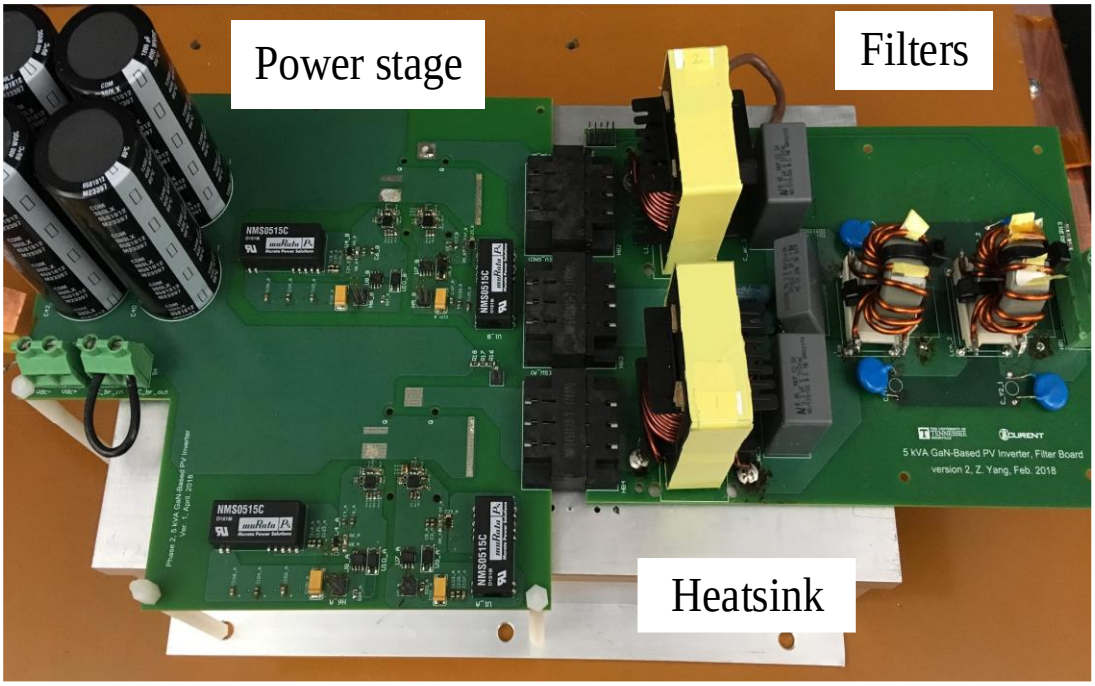
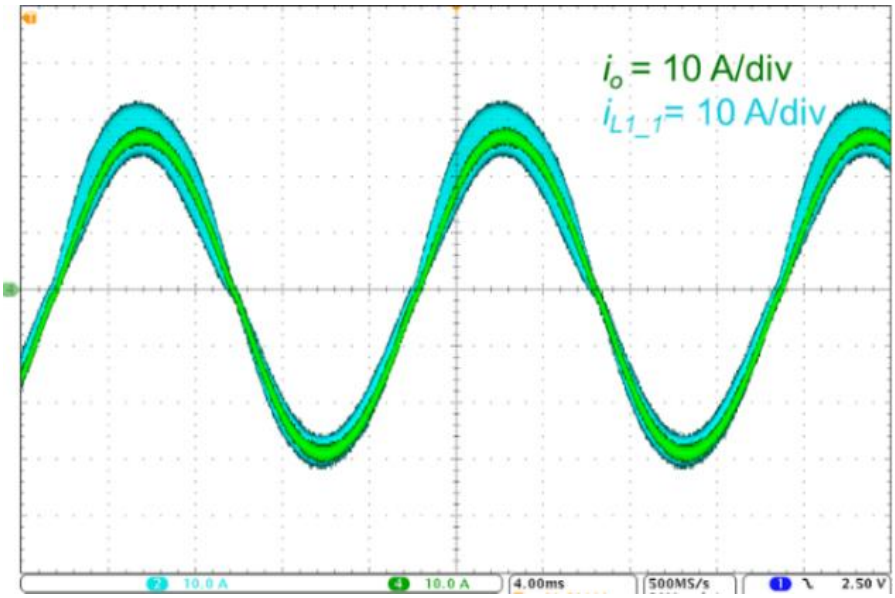
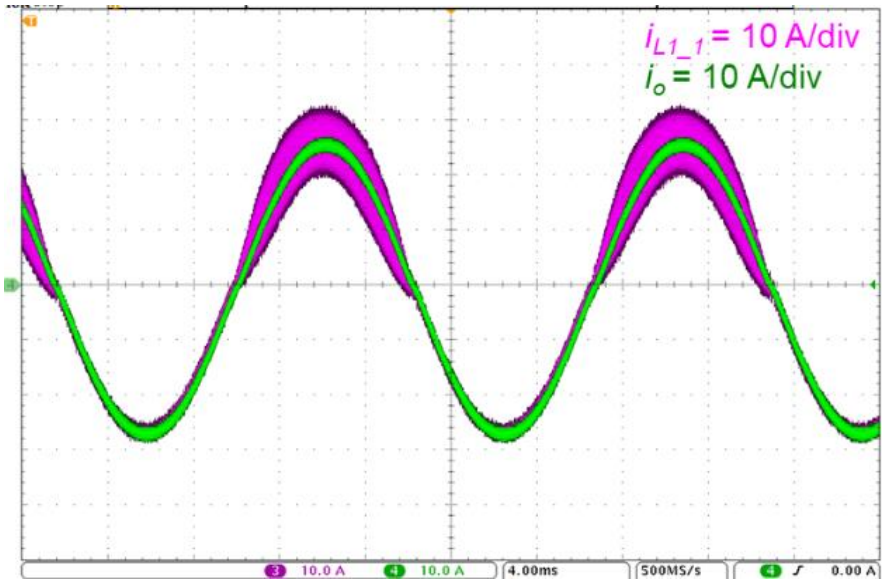


Figure 3-20. A 4.5-kW GaN-based inverter for testing filters. Four GaN devices are on the bottom side of power stage PCB.

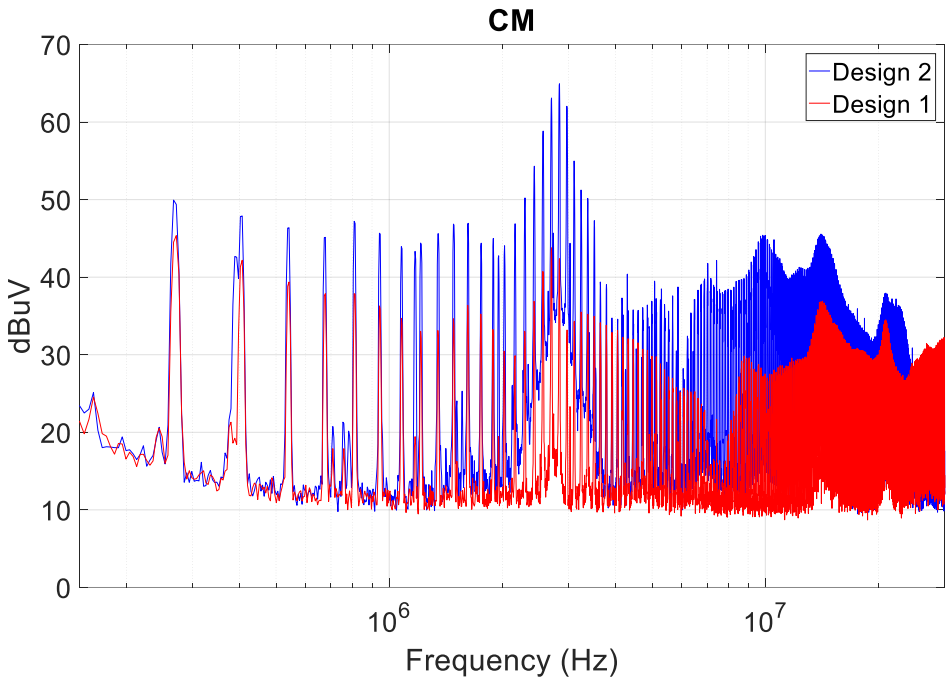


(a)

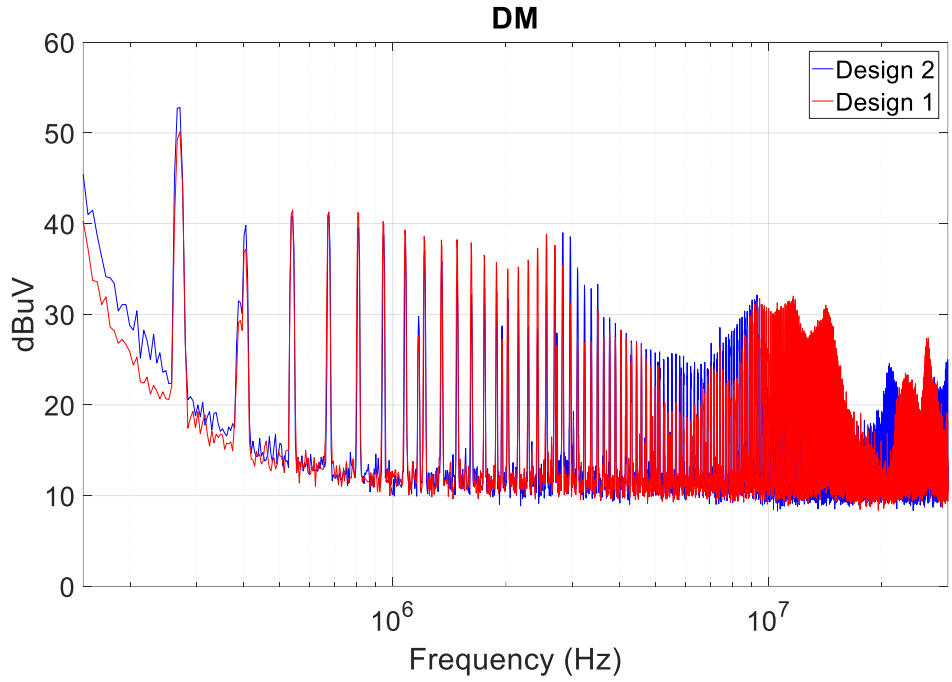


(b)

Figure 3-21. Measured current waveforms using (a) ac-side output filter Design # 1 (L_1 = 58 μH and k = 1), (b) ac-side output filter Design # 2 (L_1 = 76 μH and k = 0).



(a)



(b)

Figure 3-22. Measure EMI performance of two ac-side output filter designs: (a) CM, (b) DM.

iteration loops, accuracy, and simple implementation. The models for calculating the fringing effect are evaluated and experimentally verified. Two design examples demonstrate that the proposed method is able to find the optimal design, which has fewer turn number and potentially smaller core size compared to the design results obtained by conventional methods.

The second part of this chapter discusses the design of output filter using both non-coupled and coupled inductors for the single-phase full-bridge inverter. The design algorithm for individual inductor described in the first part of this chapter is used. It is shown that the ratio between coupled and non-coupled inductance determines the performance of the filter, including the weight, loss and EMI performance. The relationships and tradeoffs among different parameters are derived. In general, a coupled inductor contributes to lower total weight and better CM performance, but also induces more loss mainly because of winding loss.

Furthermore, a holistic design and optimization procedures considering the total weight of inductors are also presented. The lightest weight design is achieved when L_{cp} and L_1 have the same inductance. Based on the design results, an optimized and a referenced ac-side filters are tested and compared in a 4.5 kW GaN-based inverter, which validates the analysis and design.

Chapter 4 Design of High-density Multi-stage Ac-side EMI Filter

4.1 Design and Test of EMI Filter

In this chapter, a two-stage EMI filter, as shown in Figure 4-1, is designed for a GaN-based inverter. The design of the EMI filter is split into common-mode (CM) and differential mode (DM) filters. The noise without EMI filter, which is also known as bare noise, was measured in the GaN-based inverter. By comparing the bare noise with the EMI regulatory standard, the required attenuation can be derived. For the design of the CM filter, the equivalent circuit for CM noise was derived first. Then, CM filters were designed based on the required attenuation for harmonics at and below 675 kHz, which is the 5th harmonic of switching frequency. As for the design of DM filter, each stage is assumed to have an attenuation of 40 dB/dec.

The equivalent CM circuits of the inverter without the EMI filter, and with two-stage EMI filter are shown in Figure 4-2. The load resistance for CM noise is equal to half of the resistance of LISN. The power filter designed in Chapter 3 is used. $Z_{cm1}(\omega)$ and $Z_{cm2}(\omega)$ are the impedance of CM inductors, which are frequency-dependent due to the magnetic material. C_{cm1} and C_{cm2} are the CM capacitors. It is assumed that the components in two stages are the same, i.e., $Z_{cm1}(\omega) = Z_{cm2}(\omega)$ and $C_{cm1} = C_{cm2}$.

The CM voltage without EMI filter (V_{CM0}) is

$$V_{CM0}(\omega) = V_{CMS}(\omega)\frac{(0.5R_{LISN}+1/(2j\omega C_p))//Z(\omega)}{(0.5R_{LISN}+1/(2j\omega C_p))//Z(\omega)+0.5j\omega(L_1+2L_{cp})}\frac{0.5R_{LISN}}{0.5R_{LISN}+1/(2j\omega C_p)}, \quad (4\text{-}1)$$

where $Z(\omega) = \frac{1}{2j\omega C_{dc}} + \frac{1}{2j\omega C} + \frac{1}{2}R_d$.

The CM voltage across $0.5R_{LISN}$ after using two-stage EMI filter can be calculated by

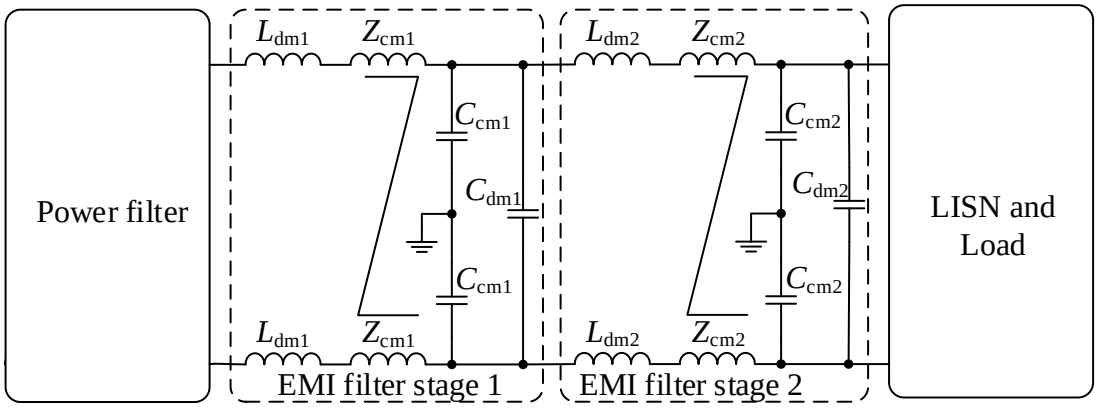
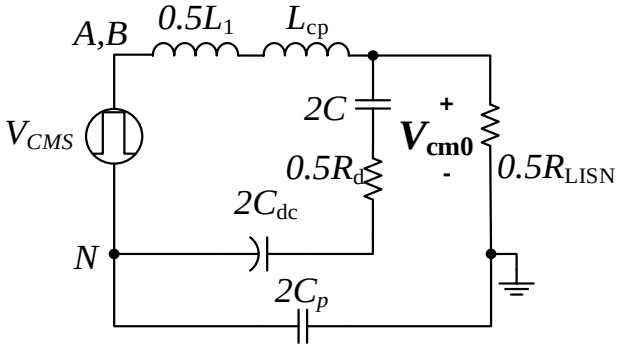
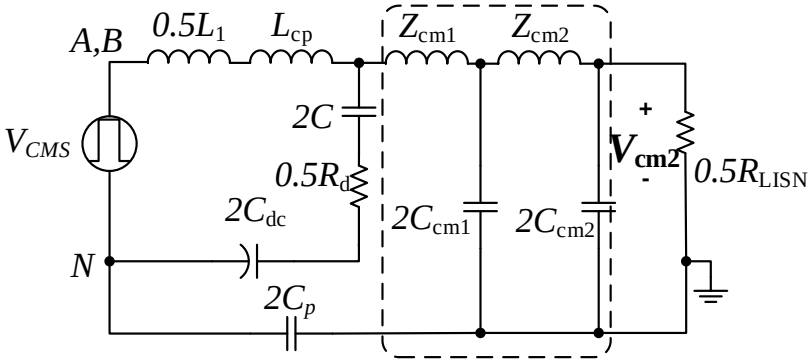


Figure 4-1. Topology of a two-stage EMI filter for the GaN-based inverter prototype.



(a)



(b)

Figure 4-2. Equivalent CM circuit: (a) without CM filter, and (b) with two-stage *LCLC* CM filter.

$$V_{CM2}(\omega) = V_{CMS}(\omega)\frac{((0.5R_{LISN}//(\frac{1}{2j\omega C_{cm2}})+Z_{cm2}(\omega))//(\frac{1}{2j\omega C_{cm1}})+Z_{cm1}(\omega)+\frac{1}{2j\omega C_p})//Z(\omega)}{((0.5R_{LISN}//(\frac{1}{2j\omega C_{cm2}})+Z_{cm2}(\omega))//(\frac{1}{2j\omega C_{cm1}})+Z_{cm1}(\omega)+\frac{1}{2j\omega C_p})//Z+0.5\omega(L_1+2L_{cp})} * \frac{(0.5R_{LISN}//(\frac{1}{2j\omega C_{cm2}})+Z_{cm2}(\omega))//(\frac{1}{2j\omega C_{cm1}})}{(0.5R_{LISN}//(\frac{1}{2j\omega C_{cm2}})+Z_{cm2}(\omega))//(\frac{1}{2j\omega C_{cm1}})+Z_{cm1}(\omega)+\frac{1}{2j\omega C_p}} \frac{0.5R_{LISN}//(\frac{1}{2j\omega C_{cm2}})}{0.5R_{LISN}//(\frac{1}{2j\omega C_{cm2}})+Z_{cm2}(\omega)}, \quad (4\text{-}2)$$

where $Z(\omega) = \frac{1}{2j\omega(C+C_{dc})} + 0.5R_d$.

The attenuation of the EMI filter for CM noise is

$$Att_{CM2}(\omega) = 20\log\left(\left|\frac{V_{CM2}(\omega)}{V_{CM0}(\omega)}\right|\right). \quad (4\text{-}3)$$

As for the DM part of the EMI filter, 80dB/dec attenuation was applied to the two-stage filter. In addition, *LCLC* structure is selected since it can guarantee impedance mismatch with power filter and LISN. Therefore, the DM attenuation two-stage filters is

$$Att_{DM2}(\omega) = 80\log\left(\frac{\omega_{c2}}{\omega}\right). \quad (4\text{-}4)$$

With the above equations, the design of the EMI filter can be equivalent to the design of Z_{cm}, C_{cm}, C_{dm}, and L_{dm} such that the filter attenuation is larger than required attenuation. In the design, C_{cm} is limited by leakage current requirement of 30 mA, and 10 nF was selected. To achieve high-density design L_{dm} is the leakage of CM inductor, and no separate inductor is needed for L_{dm}. To obtain the required attenuation, the bare noise was measured in the prototype and compared with the EMI standard. The test platform was setup according to EMI standard FCC Part 15 Class B, and is shown in Figure 4-3. The CM and DM bare noise is shown in Figure 4-4, and the required attenuation is summarized in Table 4-1, which was obtained from comparing the bare noise and EMI standard, with design margin of 6 dB. Since the switching frequency was selected to be 135 kHz, which is below the starting frequency of EMI standard, the design only considers noise at and above 270 kHz.

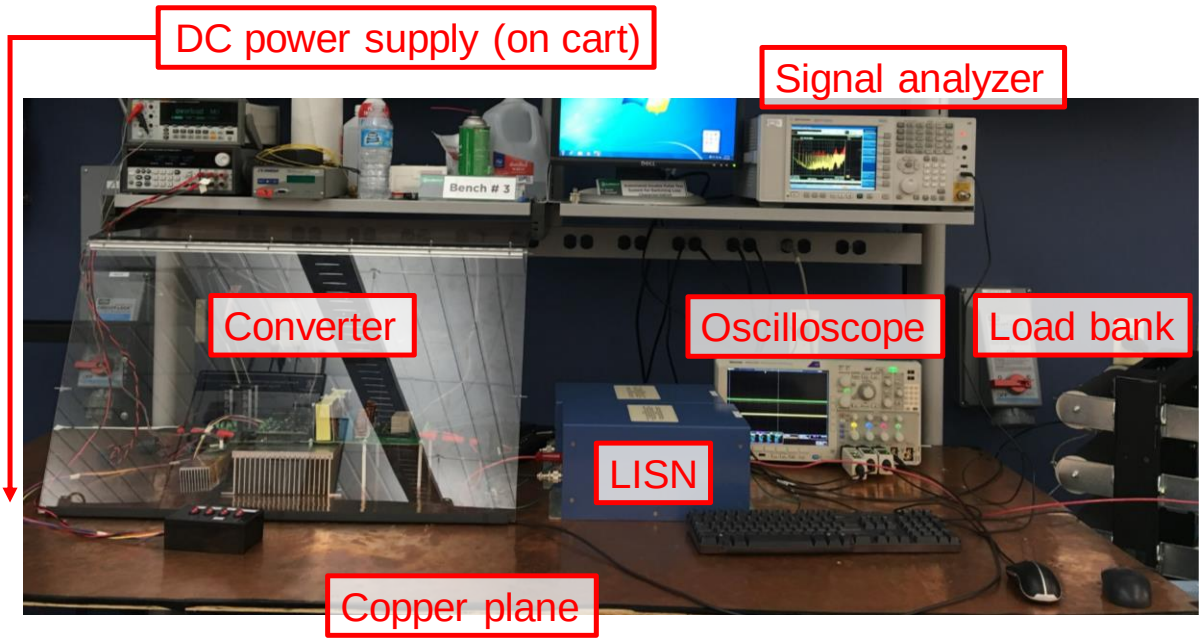
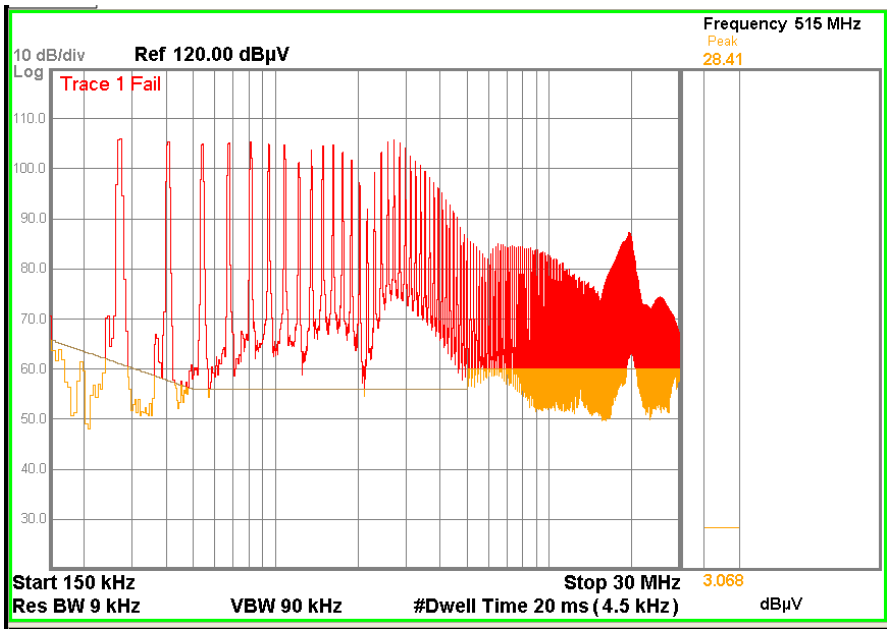


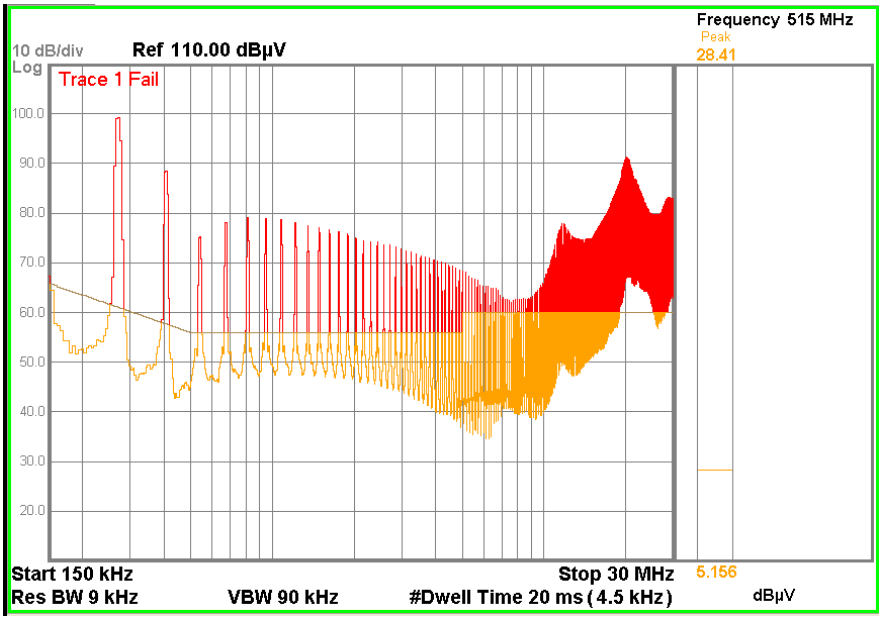
Figure 4-3. Setup for testing the EMI noise of the converter.

Table 4-1. Required CM and DM attenuations for the 4.5kW GaN-based inverter prototype

Frequency (kHz)	**Required CM attenuation (dB)**	**Required DM attenuation(dB)**
270	44.9	42.7
405	51.2	33.7
540	53.2	20.9
675	53.5	23.7



(a)



(b)

Figure 4-4. Bare EMI noise of the 4.5kW GaN-based inverter prototype: (a) CM bare noise, and (b) DM bare noise. Note that actual noise is 3 dB lower than the measurement due to the attenuation of CM and DM splitters.

The parameters of the two-stage EMI filter are summarized in Table 4-2, and the top view of the two-stage EMI filter is shown in Figure 4-5.

The designed EMI filter was tested in the GaN-based inverter prototype. To improve the CM performance of the filter, a copper shield shown in Figure 4-6 was added. CM and DM noise after using the designed EMI filter is shown in Figure 4-7.

4.2 Coupling Identification

From the test, it is obvious that the DM noise after using the designed EMI filter is above the limit. Due to the high-density layout and component location, coupling among inductors and capacitors is founded to be the root cause of the insufficient attenuation.

Coupling can occur between large-sized DM capacitors and inductors that are close to each other. One example is the coupling between the last DM capacitor and power inductor, which is shown in Figure 4-8. The coupling between the last DM capacitor and power inductor in Figure 4-8 can be explained by Figure 4-9. The current path in the DM capacitor is based on the internal structure of the film capacitor [68, 106, 107]. The leakage flux generated by the power inductor (Φ_{ind}) orthogonally intersects with the capacitor current path and induces current in the capacitor, which eventually causes extra noise in the last DM capacitor. Similar coupling can occur between L_{cm1} and C_{dm2} and between L_{cm2} and C_{dm2}. A simplified schematic of the filter considering these couplings is shown in Figure 4-10.

The DM noise after EMI filter is the same as the voltage across the last DM capacitor C_{dm2}. The impacts of three couplings which are between three inductors and the last DM capacitor can be calculated by:

Table 4-2. Parameters of the two-stage EMI filter for the 4.5kW GaN-based inverter prototype

CM inductor	Core part number	ZW42915TC
	OD/ID/Ht	29.0/19.0/15.2 mm
	Core volume	5481 mm^3
	AWG	5
	Turn number	5 for each winding
	Leakage	1.7 µH
	C_{para}	5.0 pF
CM capacitor	Part number	C981U103MYVDBA7317
	Capacitance	10 nF
DM capacitor	Part number	R463R422000M2M
	Capacitance	2.2 µF

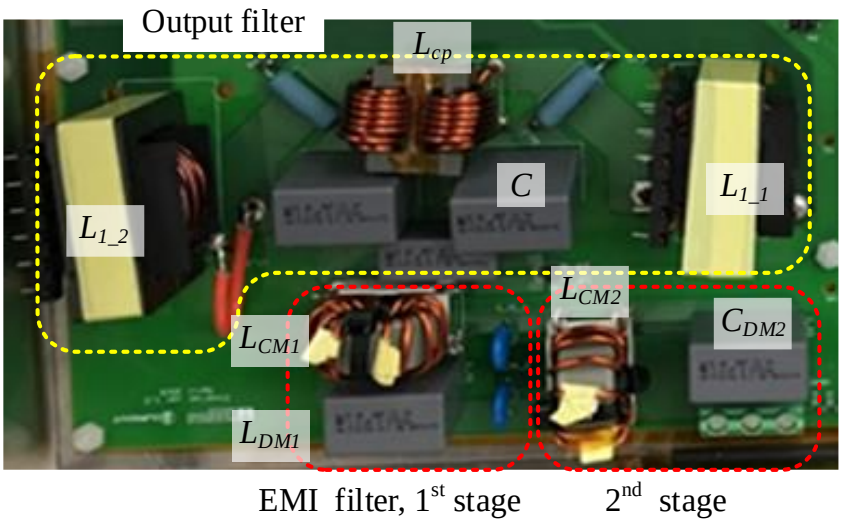
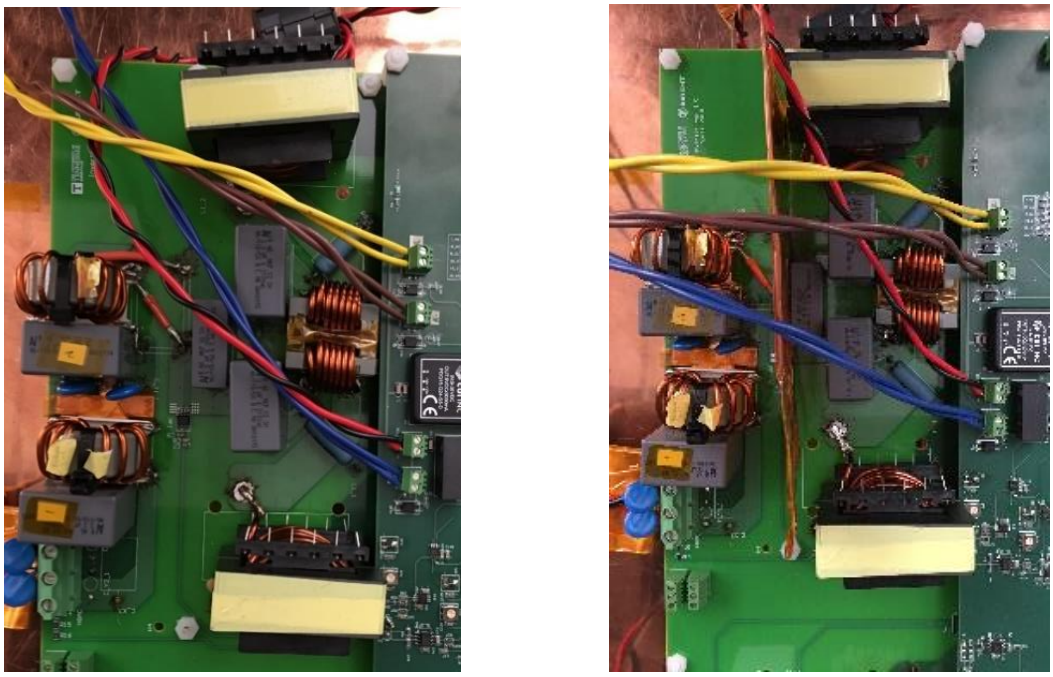
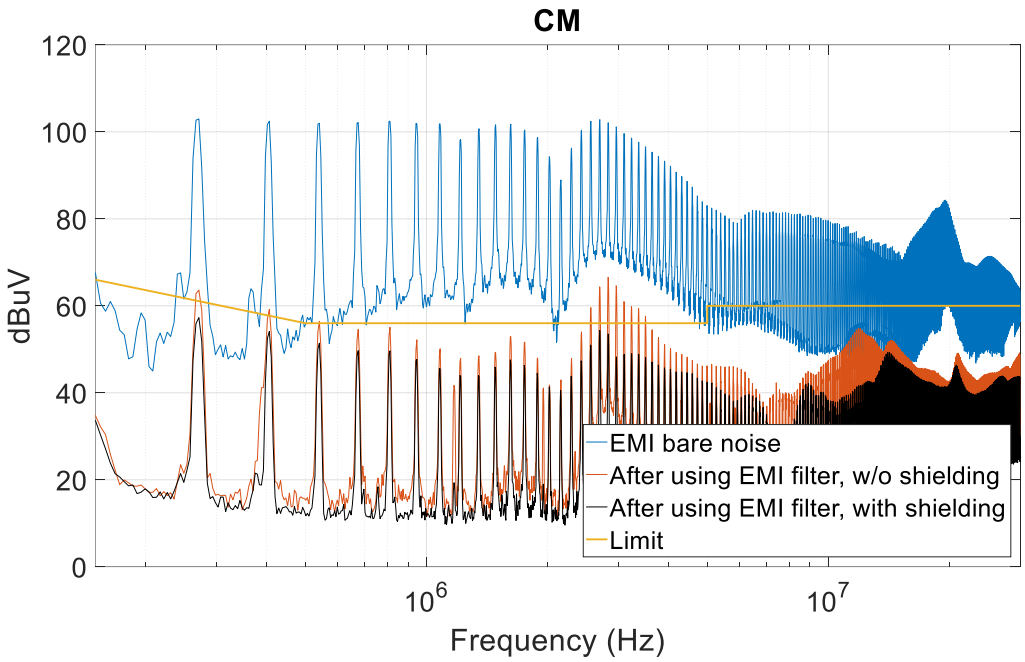


Figure 4-5. Top view of the power filter and two-stage EMI filter for the 4.5kW GaN-based inverter prototype.

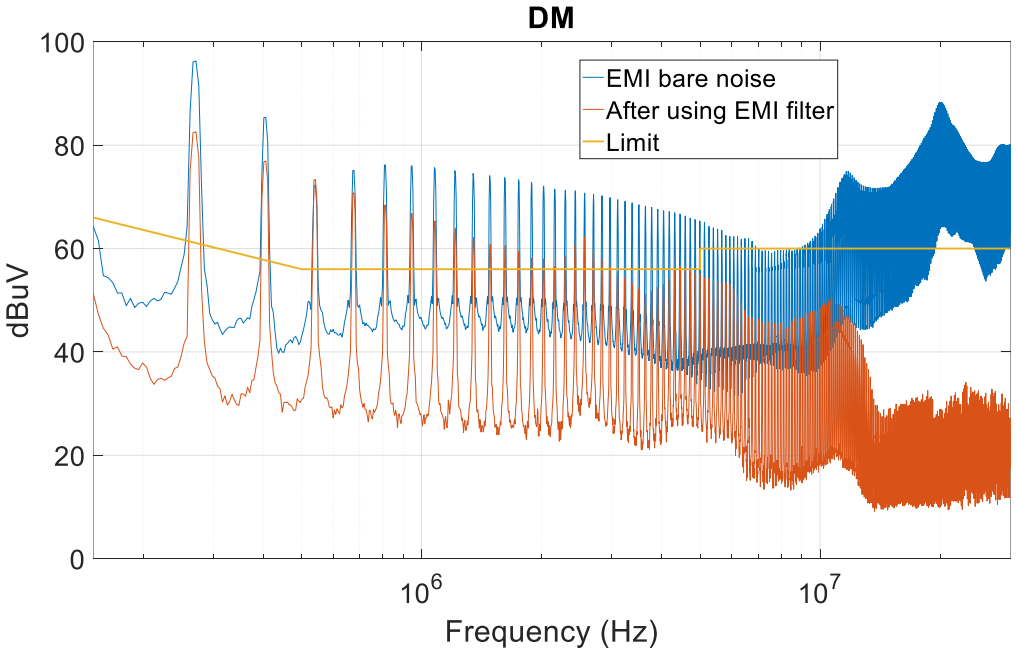


(a) (b)

Figure 4-6. Copper shield between power filter and EMI filter: (a) before using copper shield; (b) after using copper shield.



(a)



(b)

Figure 4-7. CM and DM noise after using the designed EMI filter.

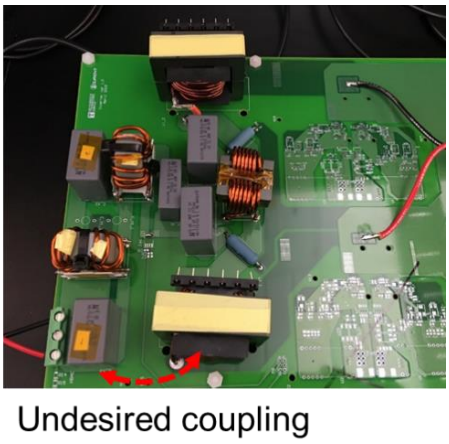


Figure 4-8. Coupling between last DM capacitor and power inductor for the GaN-based inverter prototype.

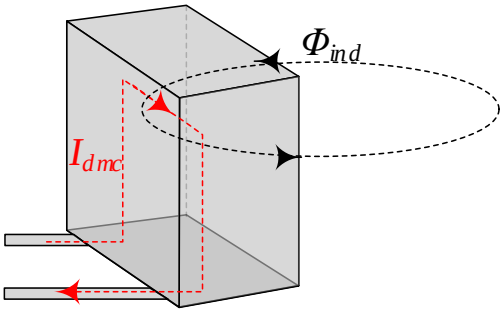


Figure 4-9. Current inside the last DM capacitor and leakage flux of power inductor.

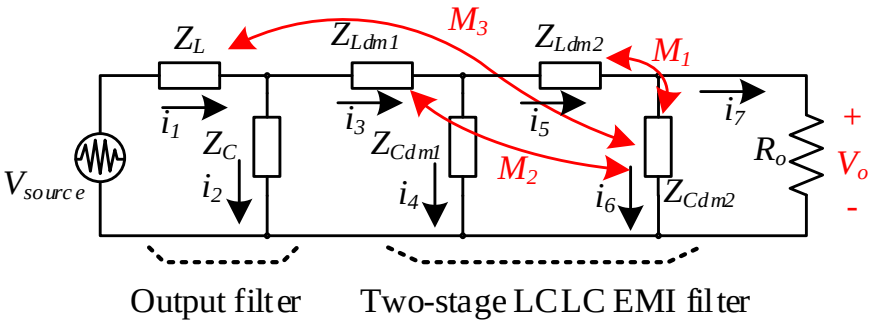


Figure 4-10. DM equivalent circuit of the overall filter, including output filter and two-stage LCLC EMI filter.

$$V_o = i_6 Z_{cdm2} + i_5 \omega M_1 + i_3 \omega M_2 + i_1 \omega M_3. \quad (4\text{-}5)$$

For currents i_1, i_3, i_5 and i_7, there are high frequency components at or above switching frequency and line frequency components. As for i_2, i_4 and i_6, there are mainly high frequency components. In the following analysis, only the high frequency components above 150kHz are considered. The high frequency components of the current and voltage are denoted as i^{HF} and v^{HF}.

At frequencies between 150 kHz and 1 MHz, it can be assumed that impedance of a capacitor is much smaller than an inductor, i.e., $Z_c << Z_L$, $Z_{cdm1} << Z_{Ldm1}$, and $Z_{cdm2} << Z_{Ldm2}$. Therefore, the high frequency component of the currents can be approximated by $i_1^{HF} \approx i_2^{HF}$, $i_3^{HF} \approx i_4^{HF}$ and $i_5^{HF} \approx i_6^{HF}$. Also, $i_2^{HF} Z_C \approx i_3^{HF} Z_{Ldm1}$, $i_4^{HF} Z_{Cdm1} \approx i_5^{HF} Z_{Ldm2}$. Therefore, high frequency component of voltage at the output of the filter becomes

$$V_o^{HF} \approx i_6^{HF} Z_{cdm2} + i_6^{HF} \omega M_1 + i_6^{HF} \omega M_2 \frac{Z_{Ldm2}}{Z_{Cdm1}} + i_6^{HF} \omega M_3 \frac{Z_{Ldm2}}{Z_{Cdm1}} \frac{Z_{Ldm1}}{Z_C}. \quad (4\text{-}6)$$

Since $Z_{Ldm2} \gg Z_{Cdm1}$ and $Z_{Ldm1} \gg Z_C$ at the frequency under consideration, the last term in (4-6) dominates the output voltage, which indicates that M_3 is the dominating coupling that has the most impact on the filter performance. To confirm that M_3 is the dominant coupling and other couplings can be ignored, the insertion loss of the output filter and EMI filter is calculated and measured. For insertion loss calculation and measurement, both the source and load resistance are set to 50 Ω. The insertion loss is defined as

$$IL = 20\log\left(\frac{V_{o,w/\ filters}}{V_{o,w/o\ filters}}\right) = 20\log\left(\frac{2V_{o,w/\ filters}}{V_{source}}\right). \quad (4\text{-}7)$$

where $V_{o,w/\ filters}$ is the output voltage at the 50Ω load resistance when filters are used, and $V_{o,w/o\ filters}$ is the output voltage at the 50 Ω load resistance when filters are not used, which half of the source voltage V_{source}.

The calculation results in Figure 4-11 show the insertion loss of the filters with different coupling values. The results confirm that M_3 is the coupling that dominates the filter characteristics. Therefore, in the following design, only M_3 needs to be considered and other couplings can be neglected. This also greatly improves the efficiency of the design since only one mutual coupling needs to be modeled.

Similar analysis can be applied to the coupling between other capacitors and the last DM capacitor. In this work, these couplings are relatively low since the distance is large, as can be observed in Figure 4-5.

4.3 EMI Filter Design Considering Self-parasitics and Couplings

For multi-stage EMI filter, the design can be complex and inefficient if all the factors are taken into account without identifying the critical ones. To improve the design method and predict the filter performance more accurately and efficiently, a new design method is proposed. The design flow chart is summarized in Figure 4-12. To achieve good accuracy, it includes self-parasitic and inductive coupling. Meanwhile, the proposed method also analyzes the importance of each consideration, so that only the critical issues need to be modeled, which improves the efficiency of the method.

After identifying the critical coupling, the next step is to determine the maximum allowable value. If the critical coupling is below this maximum allowable value, the noise should be sufficiently suppressed. To estimate the noise after filter, the DM equivalent circuit in Figure 4-10 can be used. Source voltage, $V_{_source}$ is the average of two switching nodes in Figure 2-1, e.g., $1/2(V_A+V_B)$. This can be obtained from analytical calculation, simulation, or measurement. In this work, simulation was used to obtain source voltage. The DM noise is the voltage across output

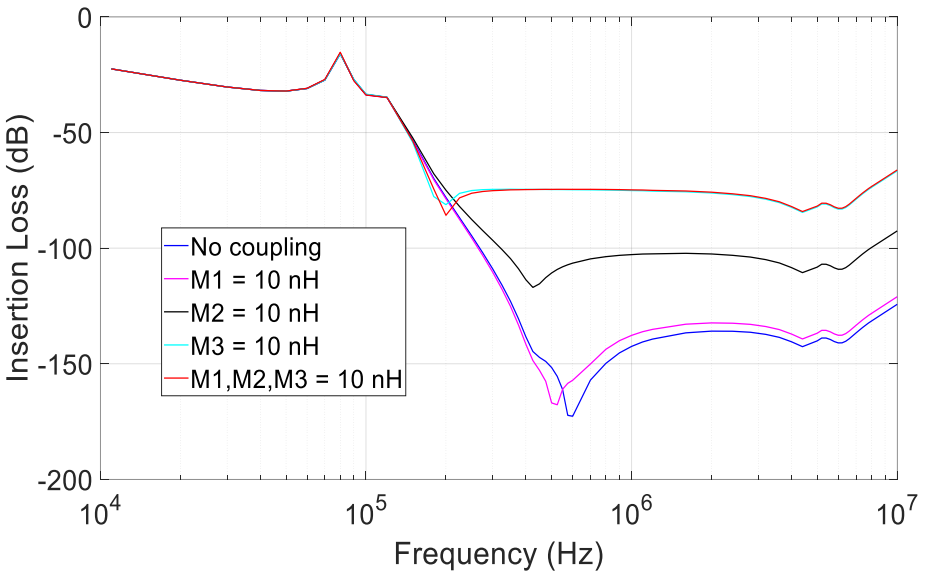


Figure 4-11. Calculation results of the insertion loss of the output and EMI filters for the GaN-based inverter prototype, using different coupling values.

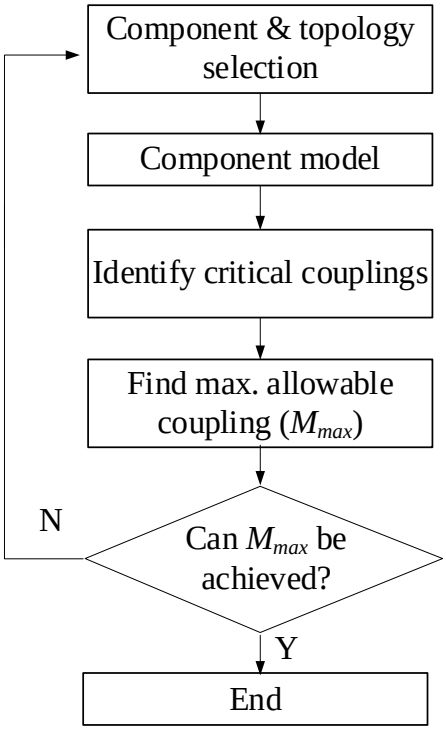


Figure 4-12. Proposed EMI filter design method.

resistance, which is 100 Ω for DM noise.

The calculated DM noise after the EMI filter with different values of M_3 are summarized in Figure 4-13. It can be seen that the maximum allowable M_3 for the EMI noise to meet the standard is 0.9 nH. The difference of DM noise between M_3 = 10 nH and M_3 = 0.9 nH is around 21 dBuV, which again confirms the dominance of M_3.

To achieve $M_3 \leq 0.9$ nH, methods for inductive coupling reduction discussed in 2.1.3 can be used. In this study, a better PCB layout with lower M_3 is considered. For the original layout shown in Figure 4-5, the coupling M_3 is modeled and simulated in FEA software ANASYS MAXWELL. The simulation setup is shown in Figure 4-14. The inductor is drawn based on the geometry and materials, while the capacitor is simplified as a round wire. The simulation result shows that the mutual inductance is 10 nH. The coupling is relatively high because the leakage flux of the power inductor (L_{1_1}) is orthogonal to the current path of C_{dm2}. To reduce this coupling, C_{dm2} is rotated by 90°, so that the leakage flux of L_{1_1} is parallel to the current path of C_{dm2}, and less flux is coupled between inductor and capacitor. The layout is shown in Figure 4-15 and the simulation setup is shown in Figure 4-16. As a result, M_3 is reduced to 0.8 nH, which is lower than 0.9 nH. In case M_3 cannot be reduced to below 0.9 nH, larger capacitance or inductance need to be selected.

4.4 Experimental Results and Verification

To verify the analysis and design, measurement of both small-signal insertion loss and DM noise in converter is compared with the theoretical calculation, for two layouts in Figure 4-5 and Figure 4-15.

a) Insertion Loss of the Filters

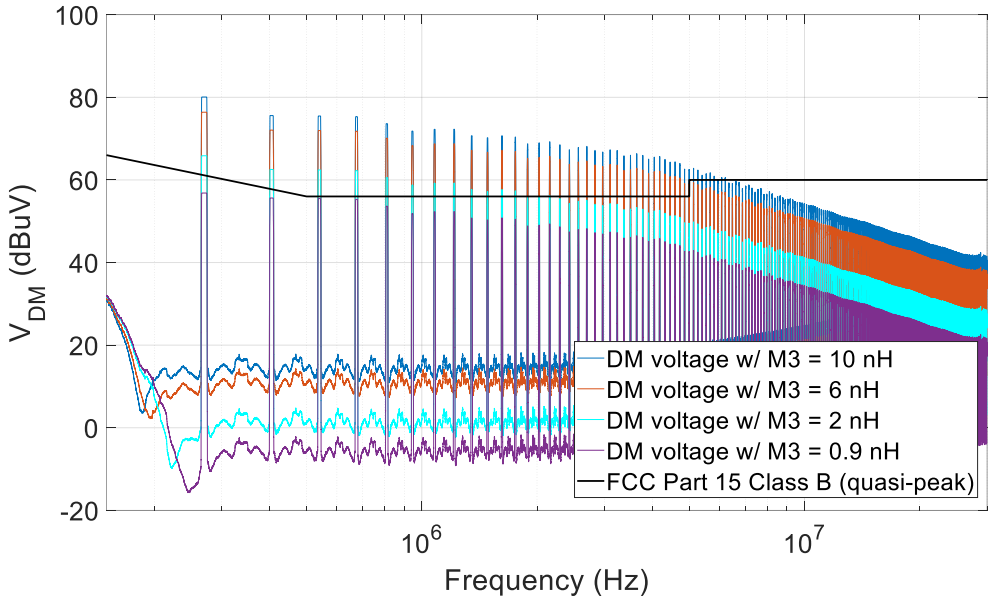


Figure 4-13. Calculation results of the DM noise of the GaN-based inverter prototype with f_{sw} = 135 kHz, using different M_3 values.

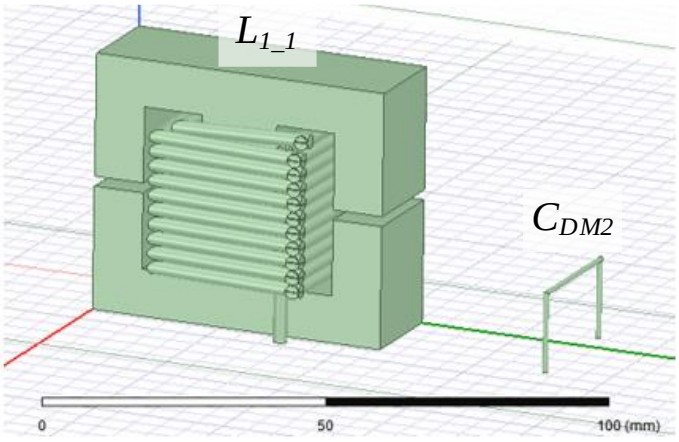


Figure 4-14. Setup in ANSYS MAXWELL to simulate the coupling between L_{1_1} and C_{dm2} using layout in Figure 4-5.



Figure 4-15. Improved layout with C_{dm2} rotated by 90°.

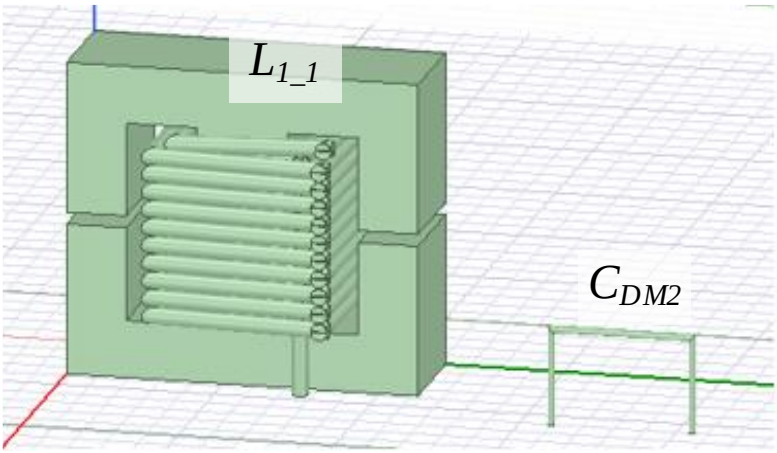


Figure 4-16. Setup in ANSYS MAXWELL to simulate the coupling between L_{1_1} and C_{dm2} using the layout in Figure 4-15.

To measure the insertion loss of output filter and EMI filter, the input and output terminals of the filters are connected to the network analyzer through isolators. The measurement setup and connection are shown in Figure 4-17. The splitter is ZSC-2-2+, a 0° two ways power splitter, and the isolator is WB1010. The magnitude and phase angle insertion loss of the filters in this measurement setup are

$$IL_{mag} = 20\log\left(\frac{|V_T|}{|V_R|}\right)\text{(dB)}, \tag{4-8}$$

and

$$IL_{angle} = angle\left(\frac{V_T}{V_R}\right). \tag{4-9}$$

The calculation results using (4-6) and the measurement results are summarized in Figure 4-18 and Figure 4-19 for two layouts in Figure 4-14. For M_3 = 0.8 nH, the voltage at the output is too small at a few kHz and therefore, the measurement contains more noise.

b) Noise in Converter

Two layouts of the filter were also tested in a single-phase dc-ac inverter to verify the analysis. The calculated DM noise of the converter after using the filter can be obtained based on the DM equivalent circuit in Figure 4-10. The comparison between measurement and calculation results for two layouts is shown in Figure 4-20 and Figure 4-21, respectively. It can be seen that the discrepancy between measured and calculated noise envelope is less than 6 dBμV up to 1 MHz.

c) Comparison with Fully Modeled Filter

To demonstrate that the proposed method can reduce the design time and maintain good accuracy, another design method that includes more couplings is compared. Based on the layout in Figure 4-5 and Figure 4-15, coupling between two nearby components are modeled in an FEA simulation, and the results are summarized in Table 4-3. Couplings between components that are

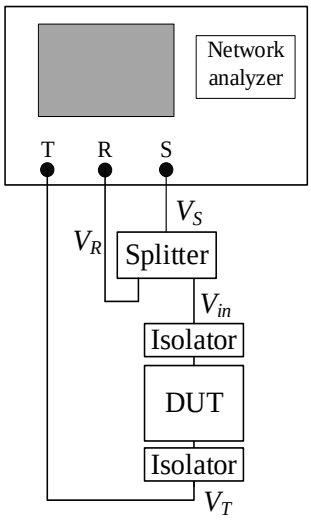


Figure 4-17. Setup for insertion loss measurement.

Table 4-3. Mutual inductance between two adjacent components for the GaN-based inverter prototype

Layout	**Component 1**	**Component 2**	***M* (nH)**	**Simulation time (min)**
Figure 4-5 and Figure 4-15	L_{CM1}	L_{DM1}	8.5	19
	C	L_{CM1}	7.0	18
	C	L_{1_1}/ L_{1_2}	1.6	185
Figure 4-5	L_{1_1}	C_{DM2}	10.2 (M_3)	182
	L_{CM2}	L_{DM2}	-1.5	19
Figure 4-15	L_{1_1}	C_{DM2}	0.8 (M_3)	113
	L_{CM2}	L_{DM2}	8.5	19

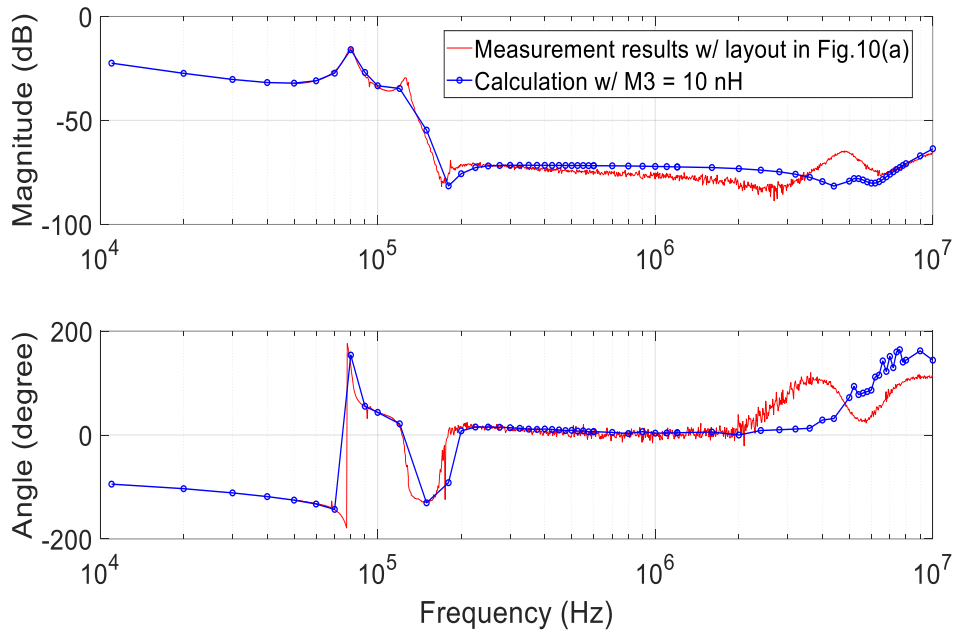


Figure 4-18. Calculation and measurement results of insertion loss of the filter using M_3 = 10 nH and layout in Figure 4-5.

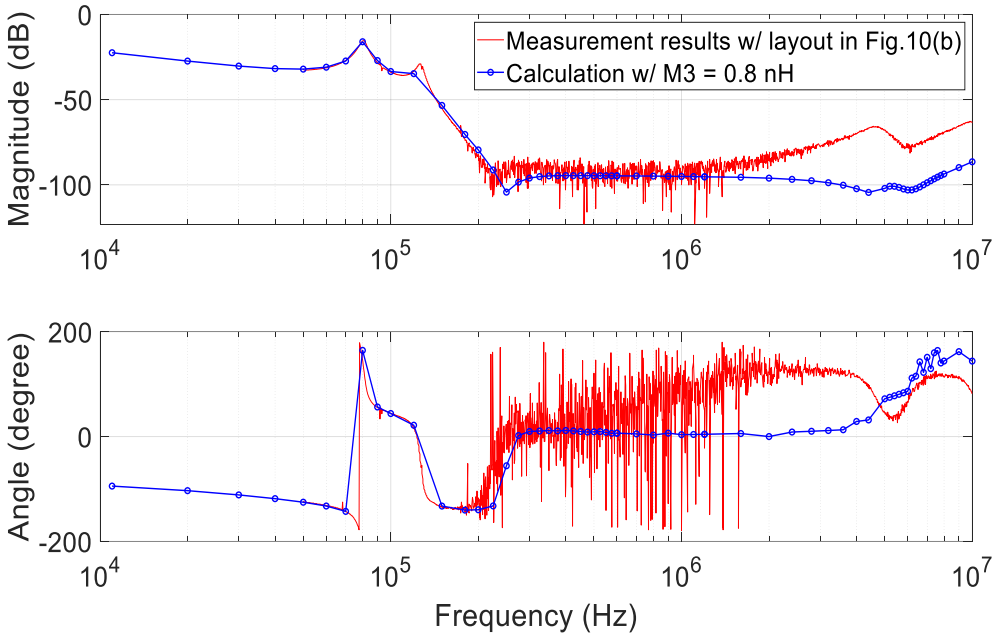


Figure 4-19. Calculation and measurement results of insertion loss of the filter using M_3 = 0.8 nH and layout in Figure 4-15.

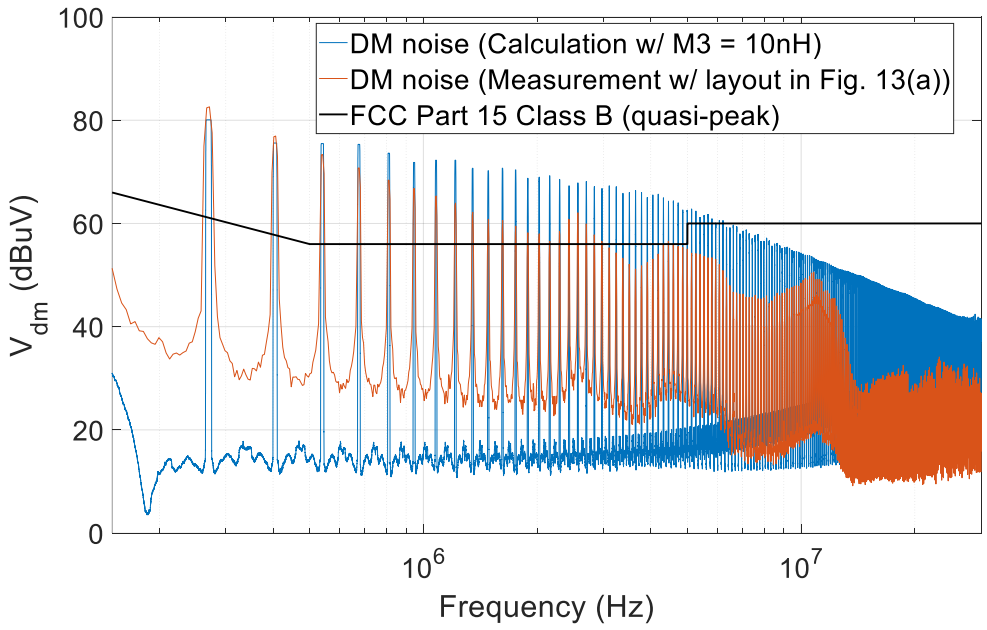


Figure 4-20. Calculated and measured results of DM noise in converter using M_3 = 10 nH and layout in Figure 4-5.

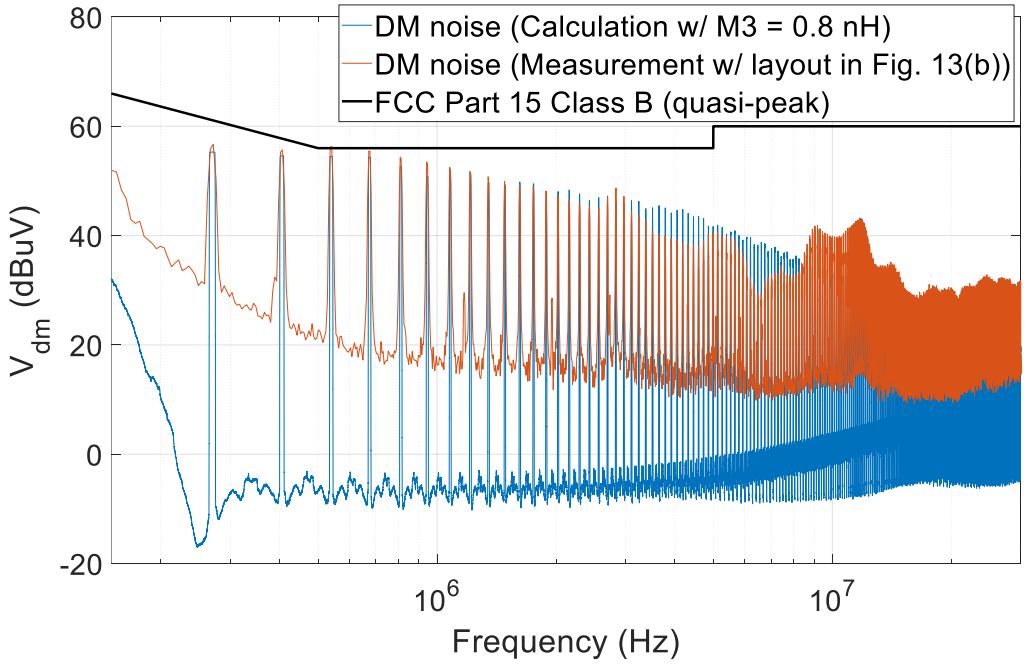
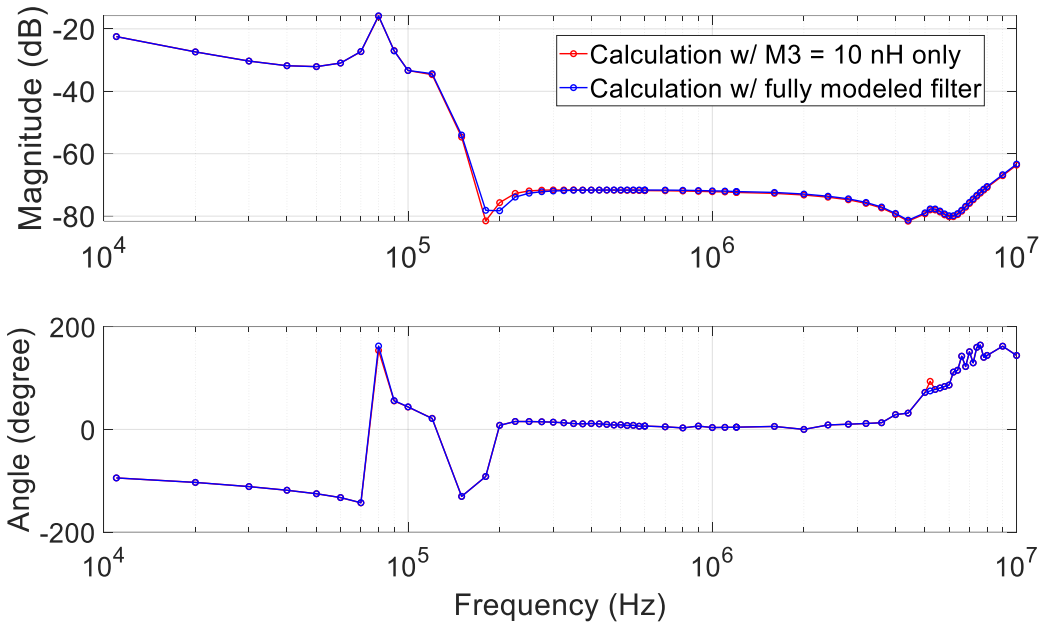
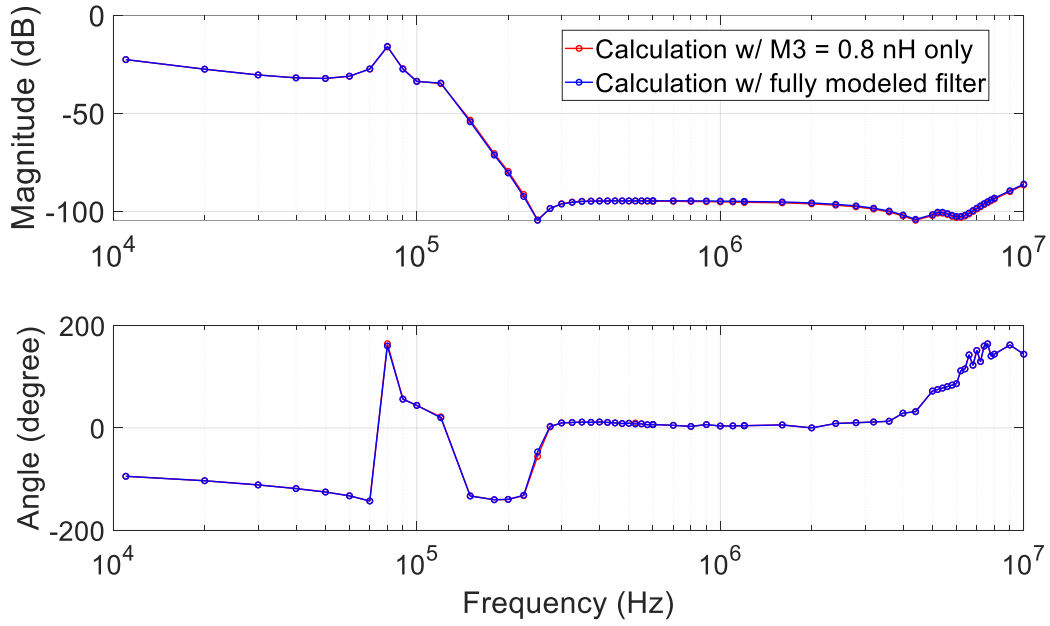


Figure 4-21. Calculated and measured results of DM noise in converter using M_3 = 0.8 nH and layout in Figure 4-15.



(a)



(b)

Figure 4-22. Calculated insertion loss of the filter, with considering M_3 only and considering more couplings, (a) layout in Figure 4-5; and (b) layout in Figure 4-15.

not physically close to each other are neglected.

Considering the couplings in Table 4-3, the insertion loss of the filter is calculated again based on the equivalent circuit in Figure 4-10. In Figure 4-22, the results are compared with the calculation that considers M_3 only, i.e., results in Figure 4-18 and Figure 4-19. The comparison shows that in both layouts, only modeling the critical coupling can still guarantee the accuracy of the design, while less simulation is needed.

4.5 Summary

In this chapter, an accurate and efficient design procedure is proposed to design high-density multi-stage EMI filter for single-phase inverter. To achieve accurate design, the procedure considers both self-parasitics of the components as well as the inductive coupling between components. As numerous self-parasitic and couplings can occur in multi-stage EMI filter, the critical ones that have more impacts at certain frequency range are identified first. Then, only these parasitic and couplings need to be modeled in the design. In the multi-stage EMI filter, it shows that the coupling between components with different noise level has significant impact on the filter performance, and it is considered to be critical coupling. The proposed method is demonstrated and verified in the ac-side filter of a single-phase dc-ac inverter. By relocating these components, the critical coupling can be reduced from 10 nH to 0.8 nH, and the EMI noise can be largely suppressed. The discrepancy between experimental and predicted results is less than 6 dBμV up to 1 MHz. The design procedure provides specific guidelines for the designers to tackle certain coupling and improve the filter performance effectively.

Chapter 5 Factors and Consideration in Loss Modeling of GaN-based Inverter

5.1 Basic Modeling of Converter Loss

a) Converter Requirement

The converter prototype discussed in this paper is a single-phase full-bridge inverter using a virtual ground connection [43]. As shown in Figure 2-1, an *L-C* power filter and a two-stage electromagnetic interference (EMI) filter are designed to meet 5% THD requirement and EMI standard of FCC part 15 class B. Note that coupled inductor is not used for the prototype. The converter design methodology has been outlined in [108], and the specifications and parameters are summarized in Table 5-1. The selected GaN device for all four switches (S_{1A}, S_{2A}, S_{1B}, and S_{2B}) is IGOT60R070D1, a top-cooled gate injection transistor (GIT) from Infineon, and the on-state gate current (i_g) is set to 20 mA. Discontinuous modulation was selected due to consideration of filtering requirement [41]. Phase leg A is modulated in the positive half of the fundamental cycle, while phase leg B is modulated in the negative half cycle. Synchronous switching is used to reduce the loss during reverse conduction.

b) Basic Loss Model

Based on the requirement, a prototype is designed with a basic loss model. The assumptions used for the basic model are:

1) Parasitic capacitance is negligible and does not affect switching loss of devices;

2) Junction temperature of device is constant during one line cycle at thermal steady-state;

3) Lumped thermal resistance is used for calculating the temperature of devices;

4) Magnetic core loss is independent of temperature;

Table 5-1. Specifications and parameters of the inverter

Input voltage (V_{in})	450 V
Output Voltage (V_o)	230 V_{rms}
Output power (P_o)	0 - 4.5 kW
Switching frequency (f_{sw})	135 kHz
Input capacitance (C_{dc})	1.2 mF
Power filter inductor (L_1, L_2)	78 μH
Power filter capacitor (C)	3.3 μF
Damping resistor (R_d)	0.25 Ω
DM inductor (L_{dm1}, L_{dm2})	1.7 μH
CM inductor (L_{cm1}, L_{cm2})	322 μH
DM capacitor (C_{dm1}, C_{dm2})	2.2 μF
CM capacitor (C_{cm1}, C_{cm2})	10 nF

5) Fringing effect is not considered for magnetic cores;

6) Capacitor loss is negligible.

To model the device loss, static and dynamic characterization of the GaN devices were performed on a curve tracer and double pulse testing (DPT) platform, respectively, according to the methodology presented in [75, 109]. The range of testing temperature is between 25 °C and 150 °C, with temperature step of 25 °C. For static characterization, the devices were placed inside a temperature-controlled chamber. As for dynamic characterization, a hot plate was used, and a copper block was located between case of the devices and surface of the hot plate for heat transfer, as shown in Figure 5-1. To ensure effective heat transfer, thermal grease was used between hotplate and copper block, and solder was used between device and copper block. Since the temperature of the hot plate is not the same as junction temperature of the device. The temperature setting of the hot plate was calibrated by using the on-state resistance of the device. The hot plate temperature setting and the corresponding junction temperature are summarized in Table 5-2.

To minimize the impact of power loop inductance on switching loss and voltage overshoot, vertical power loop shown in Figure 5-2 is used for the two devices in the same phase-leg [78]. Also, the same power loop is used in DPT and converter, so that the impacts on the switching loss and voltage overshoot due to power loop inductance can be maintained the same in both cases.

Another factor that affects the switching loss is gate driver parameter. The schematic of gate driver circuit and parameters of main components are summarized in Figure 5-3 and Table 5-3, which is used in both DPT and converter. Gate driver is AN34092B, from Panasonic.

A model using curve-fitting for $R_{ds,on}$ involving both T_j and I_d is derived based on the static testing results:

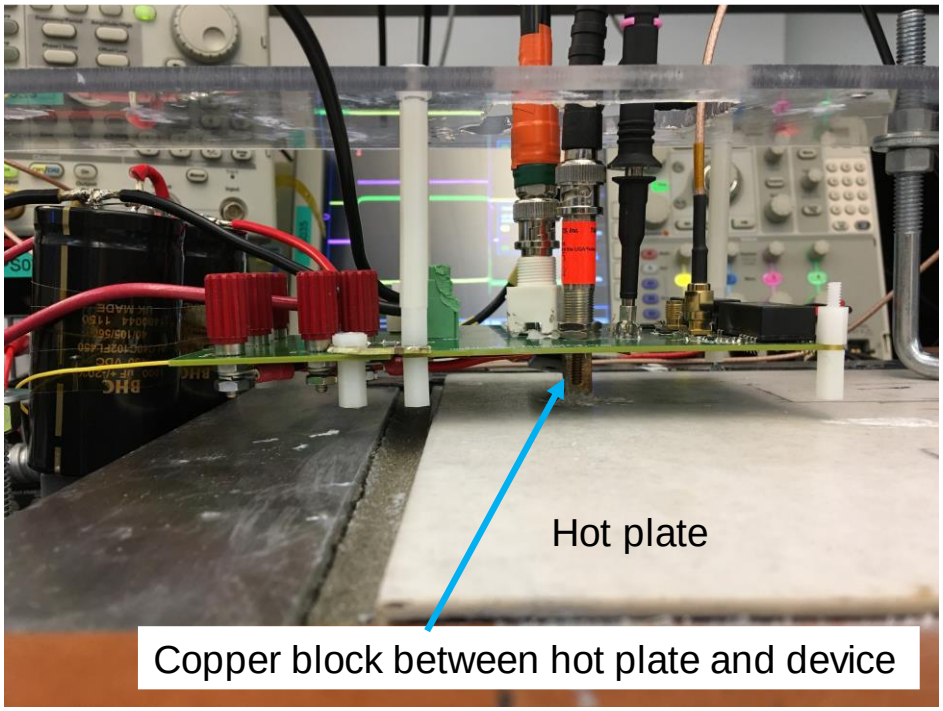


Figure 5-1. DPT setup for test at elevated temperature.

Table 5-2. Relationship between junction temperature of device and temperature setting of the hot plate

Junction temperature of devices (°C)	**Temperature setting of hot plate (°C)**
25	25
50	55
75	85
100	120
125	145
150	175

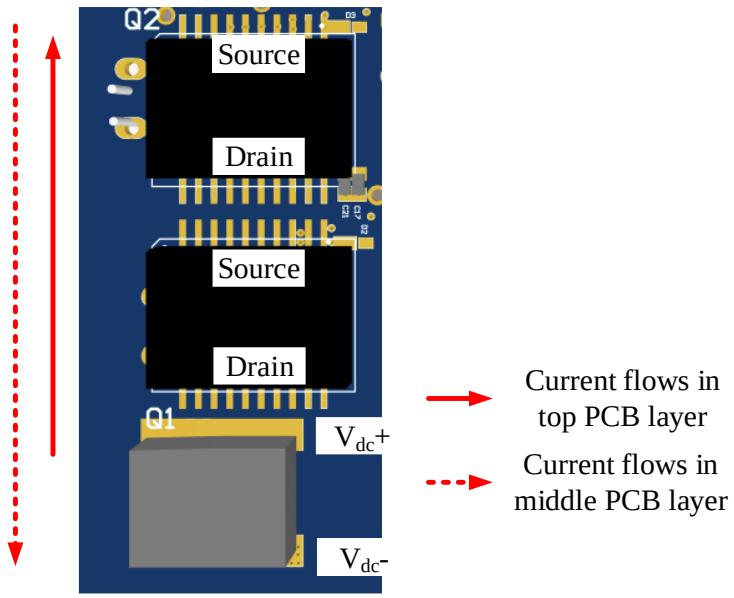


Figure 5-2. Vertical power loop layout for two devices in the same phase-leg.

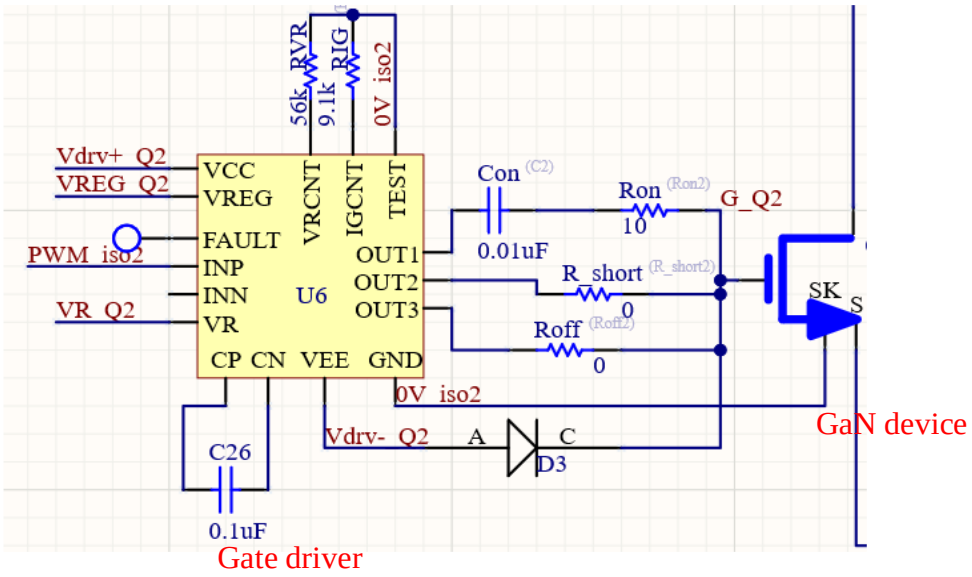


Figure 5-3. Schematic of gate driver circuit.

Table 5-3. Parameters of main components of the gate driver.

Parameters	**Values**
C_{on}	10 nF
R_{on}	10 Ω
R_{short}	0 Ω
R_{off}	0 Ω
R_{VR}	56 kΩ
R_{IG}	9.1 kΩ

$$R_{dson}(T_j, I_d) = (a_1 T_j^3 + a_2 T_j^2 + a_3 T_j + a_4) I_d^2 + (b_1 T_j^3 + b_2 T_j^2 + b_3 T_j + b_4) I_d + (c_1 T_j^2 + c_2 T_j + c_3)(\Omega), \quad (5\text{-}1)$$

where a_1 = 1.067*10^{-11}, a_2 = -2.653*10^{-9}, a_3 = 2.325*10^{-7}, a_4 = -6.214*10^{-7}, b_1 = -2.789*10^{-10}, b_2 = 7.690*10^{-8}, b_3 = -4.467*10^{-6}, b_4 = 37.199*10^{-6}, c_1 = 8.663*10^{-7}, c_2 = 2.905*10^{-4}, c_3 = 4.740*10^{-2}.

The results from curve tracer testing and the derived curve-fitting model using 20 mA gate current at different T_j are summarized in Figure 5-4.

The impact of dynamic R_{dson} is not considered in this converter, since this GaN device has negligible dynamic R_{dson} up to the rated voltage of 600 V [110].

Similarly, the drain-source voltage during reverse conduction is modeled by curve-fitting equations based on the testing results:

$$V_{ds,rev}(T_j, I_d, V_{gs}) = -(0.3942 T_j + 57.87) I_d * 10^{-3} + V_{gs} - 1.7(V). \quad (5\text{-}2)$$

The switching loss is characterized in double pulse test (DPT) at different drain currents, dc voltages and junction temperatures. The switching loss is the sum of turn-on and turn-off losses. The curve-fitting for switching loss, as a function of dc voltage (V_{dc}), drain current (I_d), and T_j, is

$$E_{sw}(V_{dc}, I_d, T_j) = (k_1 V_{dc} T_j I_d^2 + k_2 I_d^2 V_{dc}^2 - k_3 I_d^2 V_{dc} + k_4 I_d V_{dc}) * 10^{-9} + (k_5 V_{dc}^2 + k_6 V_{dc}) * 10^{-6} \ (J) \quad (5\text{-}3)$$

where k_1 = 8.0*10^{-4}, k_2 = 3.0*10^{-4}, k_3 = 950.0*10^{-4}, k_4 = 2.5, k_5 = 1.0*10^{-4}, k_6 = 350.0*10^{-4}.

The results from testing and the derived curve-fitting models at different T_j are summarized in Figure 5-5 and Figure 5-6.

Another part of device loss occurs during the dead-time interval, which is between turning off active switch and turning on synchronous switch. If the drain current is high enough to fully discharge output capacitance of devices before dead time ends, synchronous switches (S_{2A} and S_{2B}) experience reverse conduction for interval $t_{rev,cond}$:

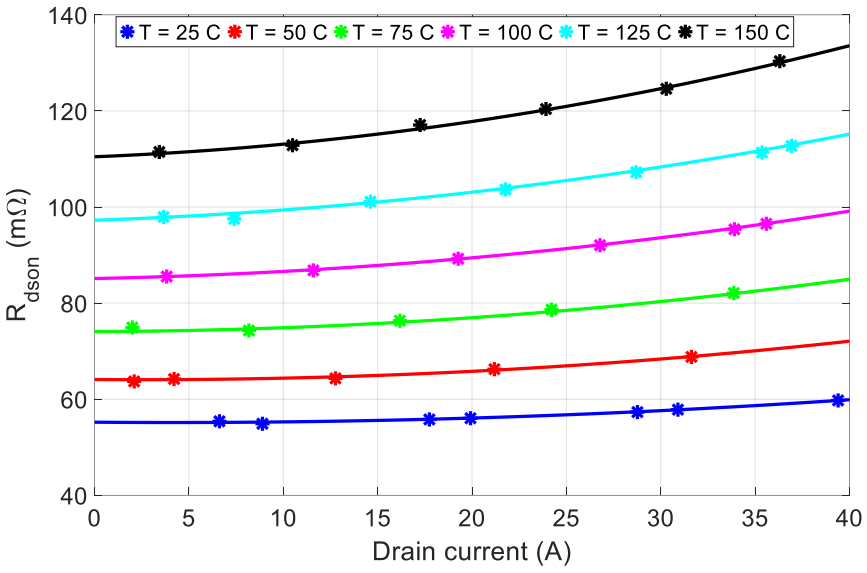


Figure 5-4. On-state resistance of the GaN GITs under different drain currents and junction temperatures with i_g = 20 mA. Circles: testing results; solid line: curve-fitting equations.

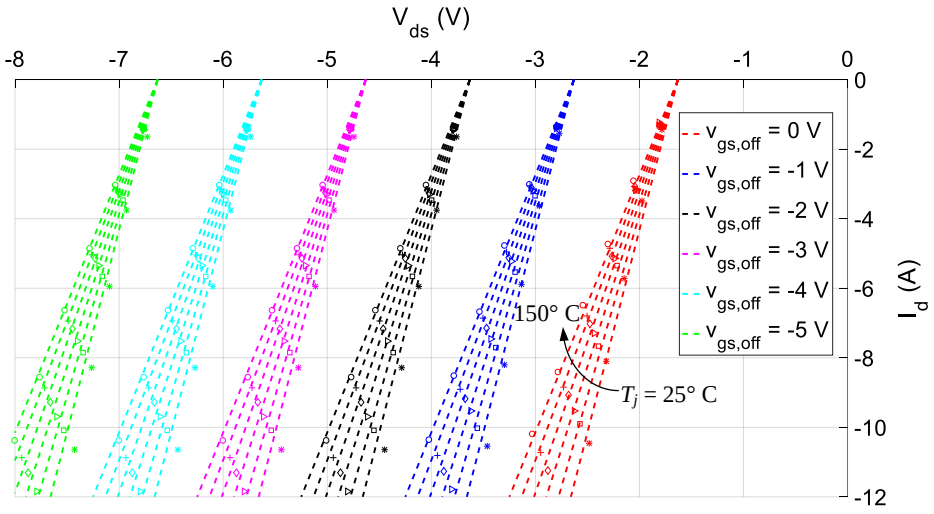


Figure 5-5. Relationship between v_{ds} and i_d of GaN GITs during reverse conduction, as function of off-state gate-source voltage (v_{gs_off}) at T_j = 25 °C, 50 °C, 75 °C, 100 °C, 125 °C and 150 °C. Markers: test results from curve tracer; dashed lines: curve-fitting results.

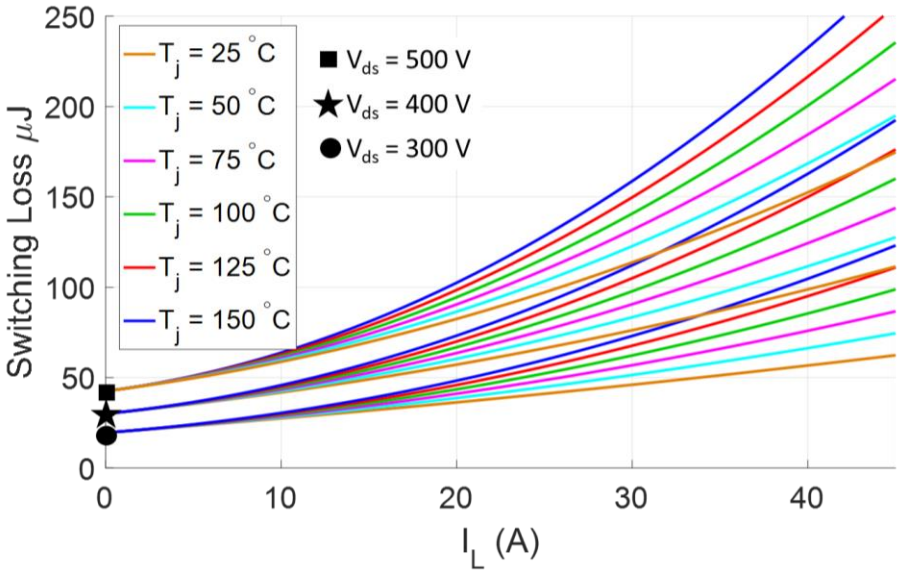


Figure 5-6. Curve-fitting of switching loss of GaN GITs at different junction temperature and drain-source voltage.

$$t_{rev,cond} = t_{dt} - \frac{2C_{oss}}{I_d} V_{dc}, \tag{5-4}$$

where t_{dt} is the dead-time setting.

Around zero crossing, I_d becomes low and cannot fully discharge C_{oss} by the end of dead-time interval, which induces extra hard switching loss known as "double switching" [111] or "incomplete zero voltage switching (iZVS)" [112]. Considering reverse conduction loss and "double switching" loss, the loss during dead-time was experimentally characterized for t_{dt} = 100 ns according to [111]. A piecewise function was developed to model the energy dissipated during dead-time interval:

$$E_{dt} = \begin{cases} V_{ds,rev} * I_d * t_{rev,cond} & if\ I_d > I_{th} \\ (\alpha_1 V_{dc} + \alpha_2) * I_d^2 + (\alpha_3 V_{dc} + \alpha_4) * I_d & (J), \\ +(\alpha_5 V_{dc} + \alpha_6) & if\ I_d < I_{th} \end{cases} \tag{5-5}$$

where $I_{th} = \frac{2C_{oss}}{t_{dt}} V_{dc}$ is the minimum current that can fully discharge output capacitance of devices by the end of dead-time interval, α_1 = 5.425*10^{-8}, α_2 = -5.425*10^{-6}, α_3 = -1.128*10^{-7}, α_4 = 1.4*10^{-5}, α_5 = 5.689*10^{-8}, and α_6 = -9.504*10^{-6}.

To calculate the switching loss and deadtime loss, the turn-on and turn-off currents are needed for each switching cycle. In this case, current ripple is also considered. The turn-on current for hard-switching devices is

$$I_{act,on} = I_{o,pk} \sin(2\omega f t) - \frac{V_{dc}}{4L_1}(1-d)dT_{sw}\ (\text{A}), \tag{5-6}$$

and the turn-off current hard-switching devices is

$$I_{act,off} = I_{o,pk} \sin(2\omega f t) + \frac{V_{dc}}{4L_1}(1-d)dT_{sw}\ (\text{A}), \tag{5-7}$$

where $d = \sin(2\omega f t)$.

Similarly, the dead-time loss during the turn-on transient of synchronous devices depends on the drain current according to (5-4) and (5-5). The load current at the turn-on of synchronous device is

$$I_{syn,on} = -I_{act,off} = -I_{o,pk}\sin(2\omega ft) - \frac{V_{dc}}{4L_1}(1-d)dT_{sw} \text{ (A).} \quad (5\text{-}8)$$

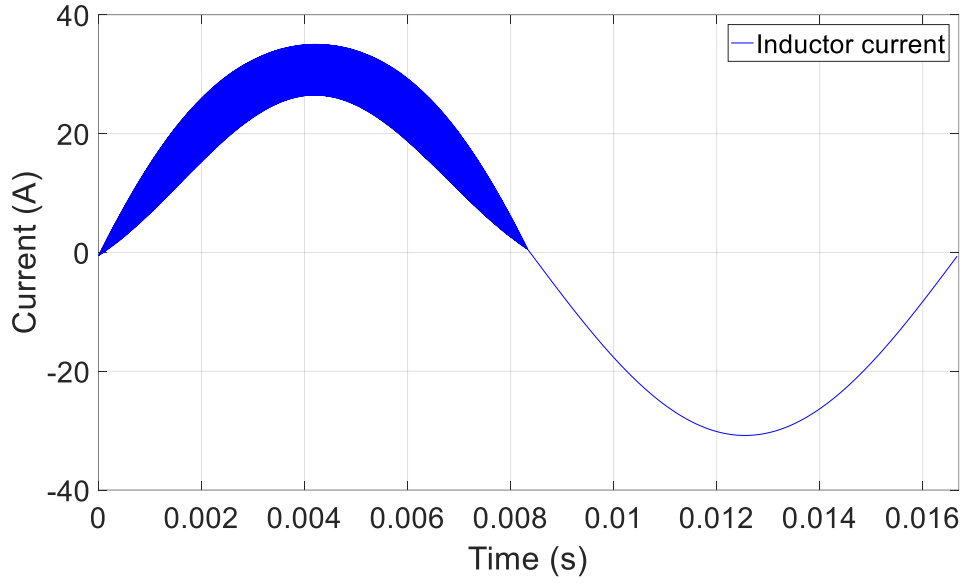
The inductor current for L_1, turn-on and turn off currents for S1A and S2A at heavy load condition are illustrated in Figure 5-7. At heavy load condition, S1A and S1B are hard-switching devices, incurring both turn-on and turn-off losses, while S2A and S2B are synchronous devices incurring reverse conduction loss and "double switching" loss.

It can be observed that the turn-on and turn-off currents are not the same. However, the results in Figure 5-6 and (5-3) are the total switching losses at the same turn-on and turn-off currents. The solution is to use the turn-on current to calculate the total switching losses because the turn-off loss has smaller dependence on the turn-off current.

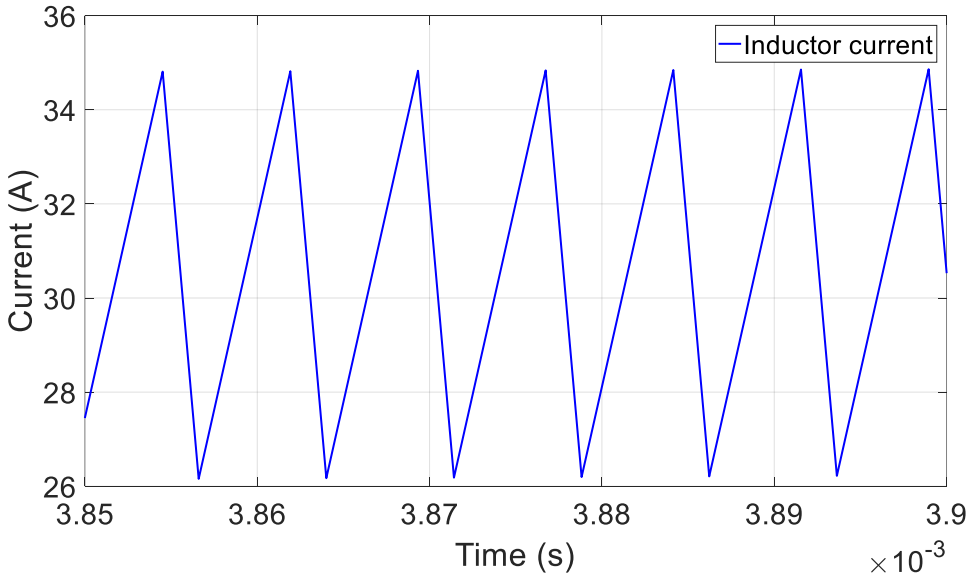
At the light load condition, both S1A and S2A turn on at negative current and turn off at positive current, as shown in Figure 5-8. Thus, both devices have reverse conduction loss and "double switching" loss at the turn-on transient and turn-off switching loss at the turn-off transient. Since the turn-off switching loss is relatively small, it is neglected in the calculation.

In this design, natural convection is employed, and one single heatsink is used for all four devices in the circuit. Since the case of the devices is internally connected to the source terminals, and the heatsink is grounded, a thermal interface material (TIM) is inserted between the case of devices and the heatsink to provide galvanic isolation.

The static thermal model containing four GITs, TIM, and heatsink is shown in Figure 5-9, and the thermal resistance of each component is listed in Table 5-4. The selected heatsink is Aavid

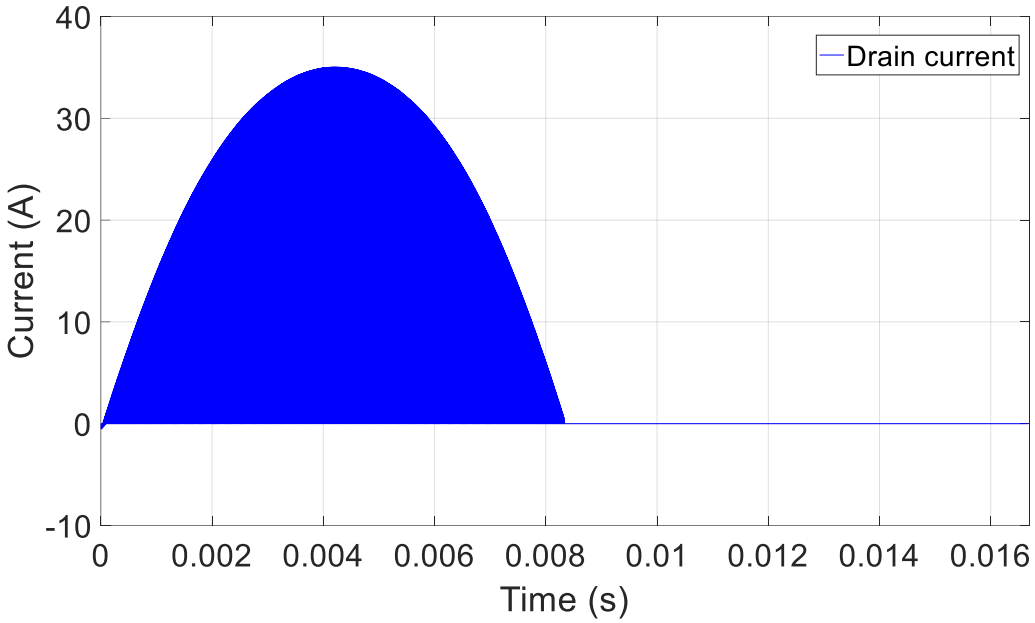


(a)

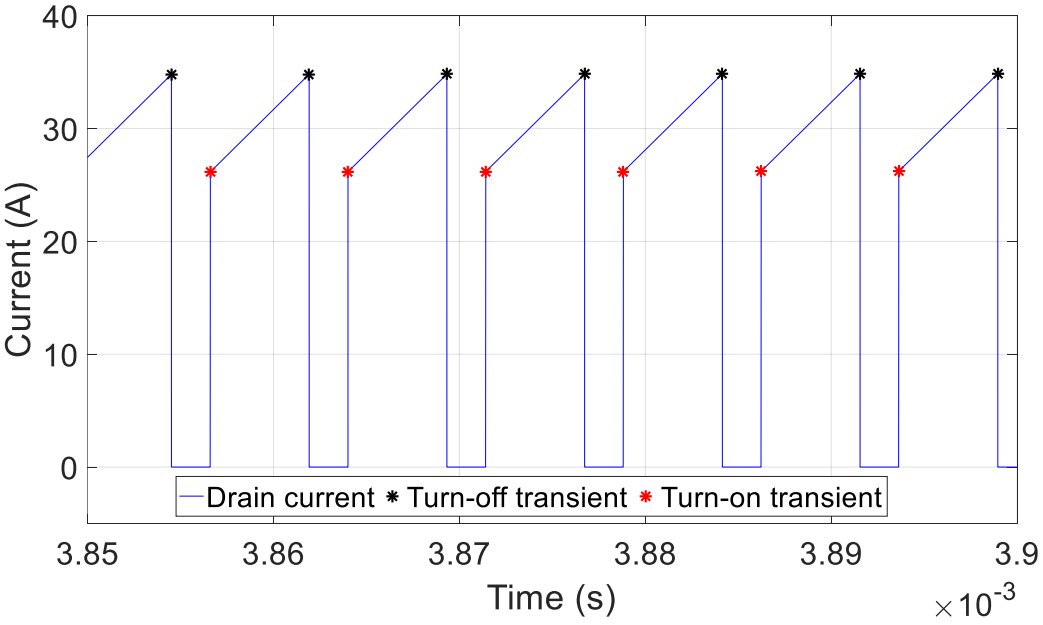


(b)

Figure 5-7. Currents at 5000 W, 230 V_o, 450 V_{in} :(a) Inductor current in a line cycle; (b) Zoomed-in inductor current; (c) Drain current of S1A in a line cycle; (d) Zoomed-in drain current of S1A; (e) Drain current of S2A in a line cycle; (f) Zoomed-in drain current of S2A.

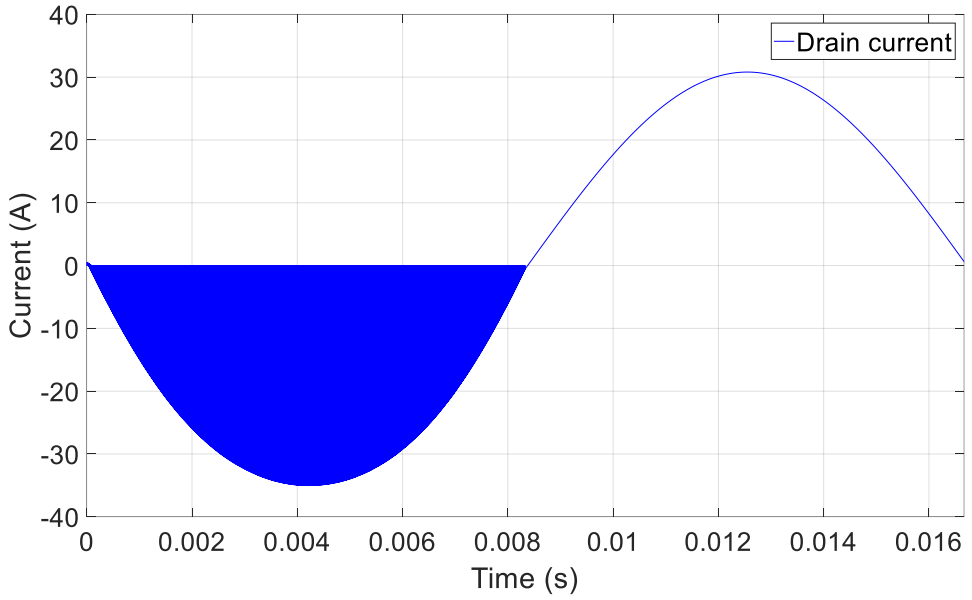


(c)

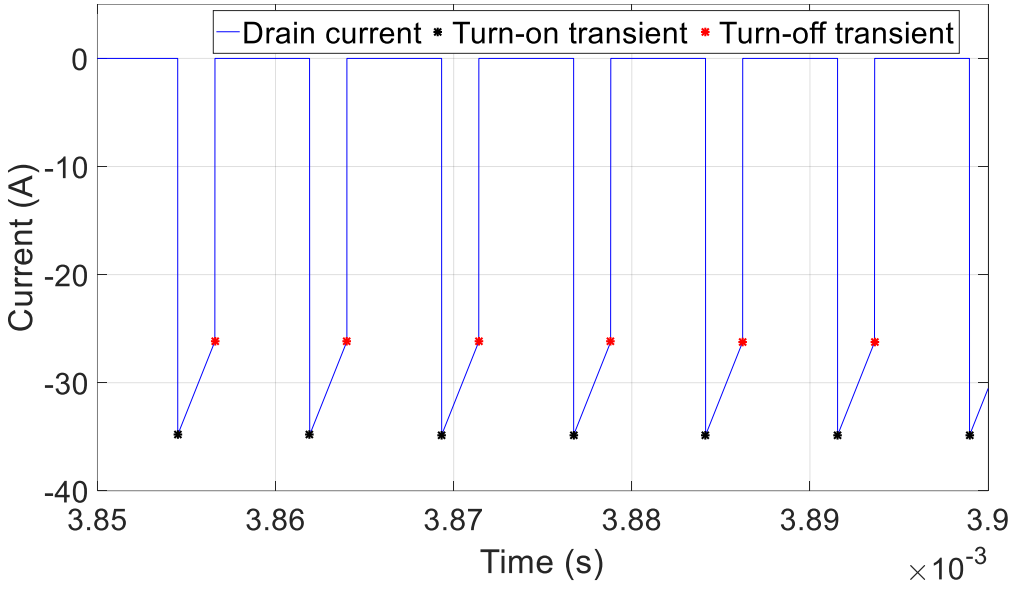


(d)

Figure 5-7 continued.

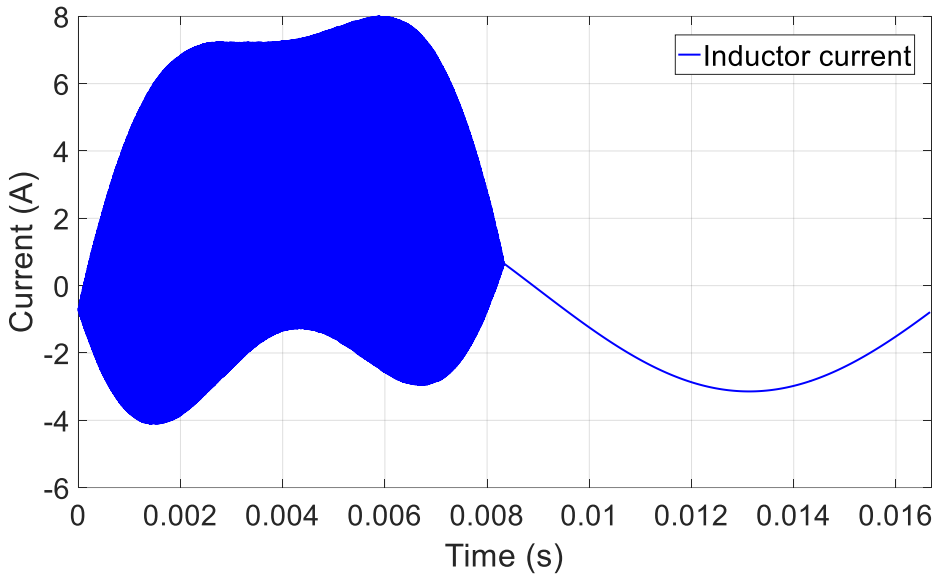


(e)

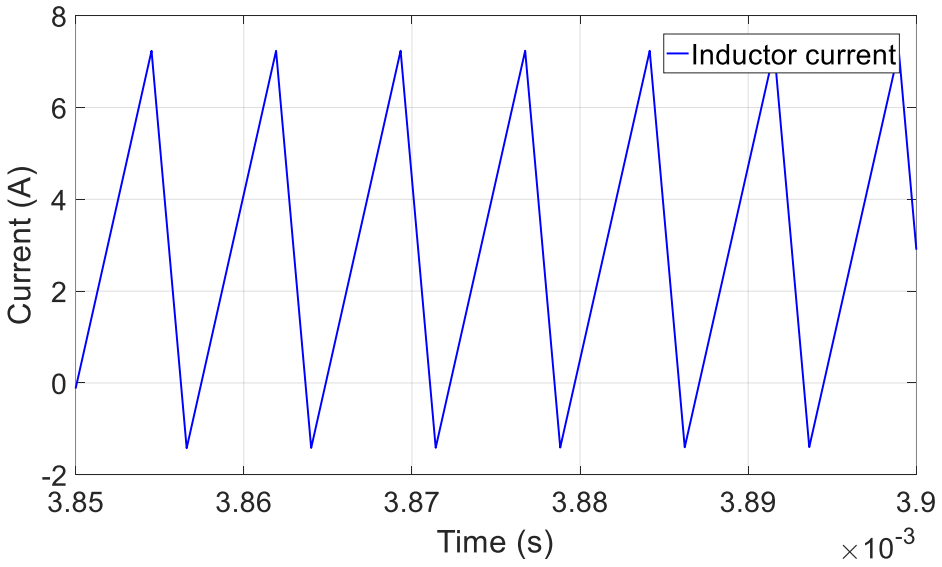


(f)

Figure 5-7 continued.

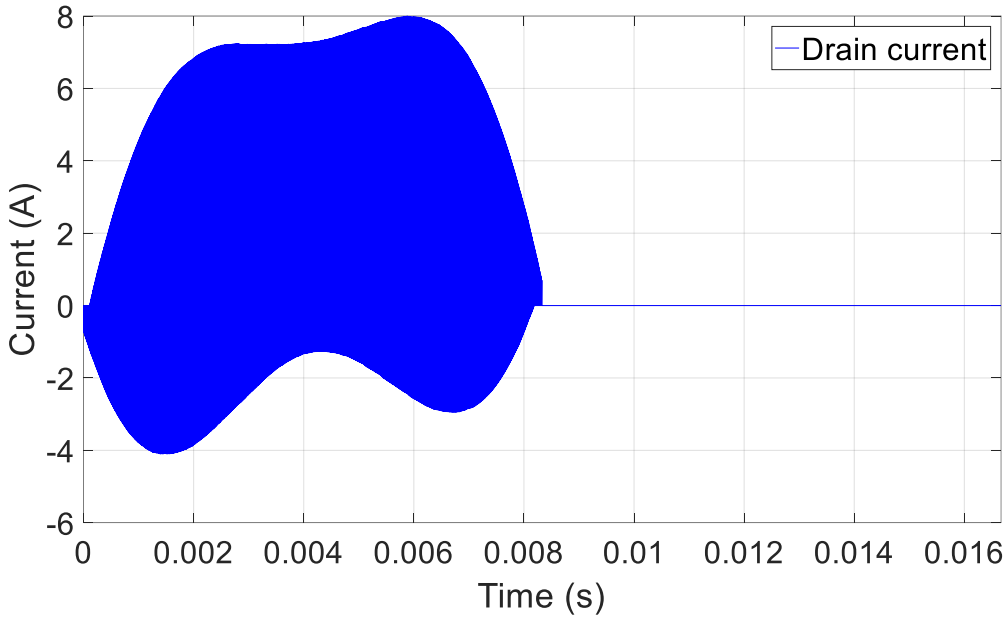


(a)

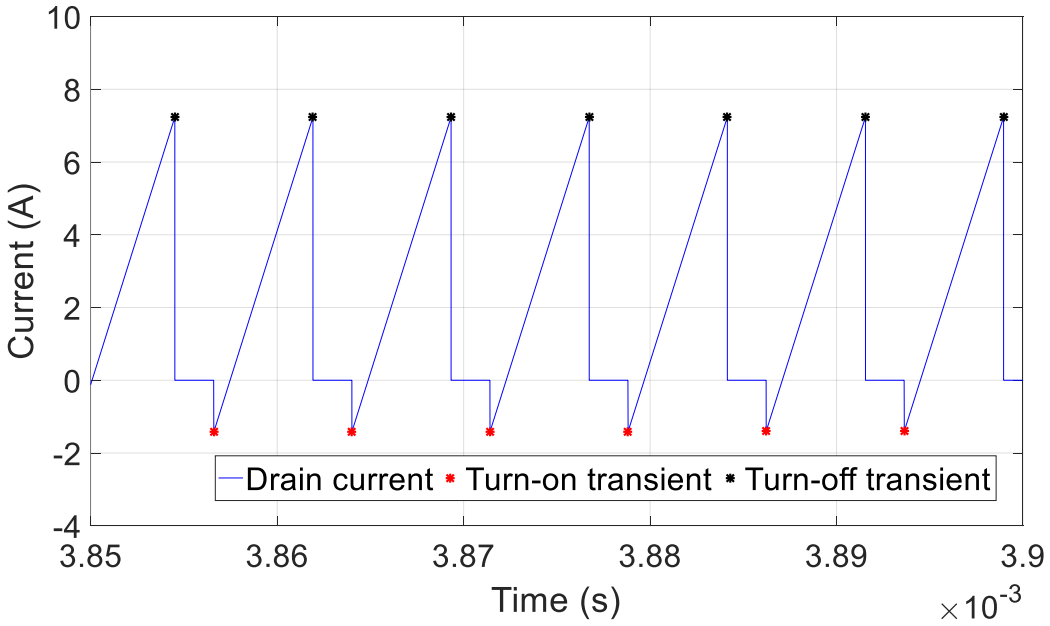


(b)

Figure 5-8. Currents at 500 W, 230 V_o, 450 V_{in} :(a) Inductor current in a line cycle; (b) Zoomed-in inductor current; (c) Drain current of S1A in a line cycle; (d) Zoomed-in drain current of S1A; (e) Drain current of S2A in a line cycle; (f) Zoomed-in drain current of S2A.

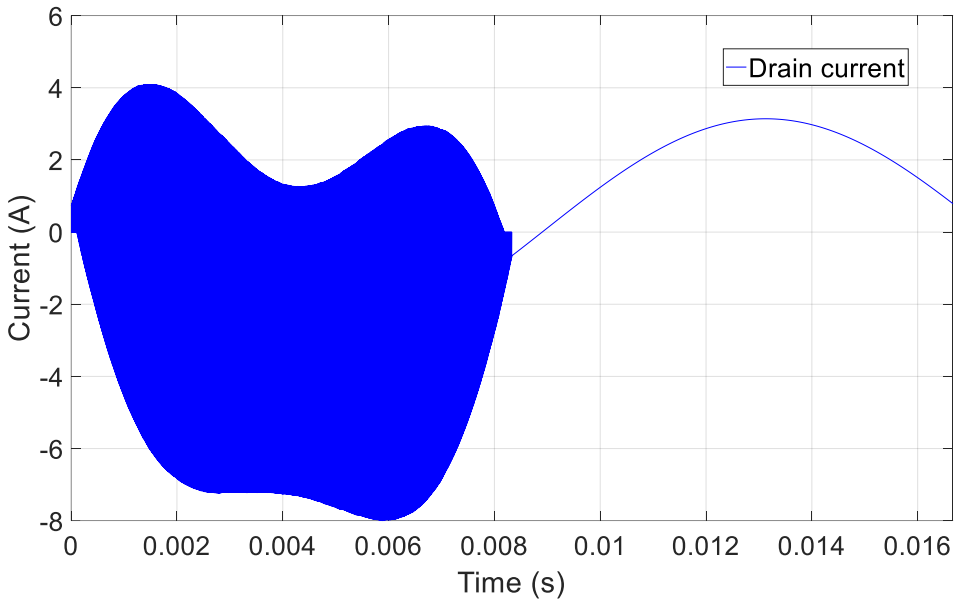


(c)

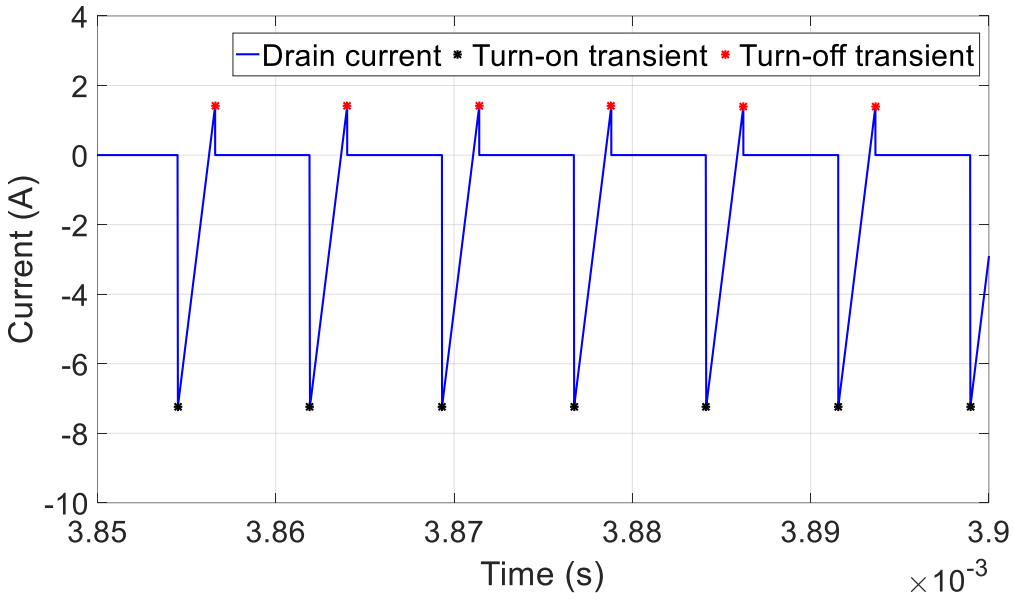


(d)

Figure 5-8 continued.



(e)



(f)

Figure 5-8 continued.

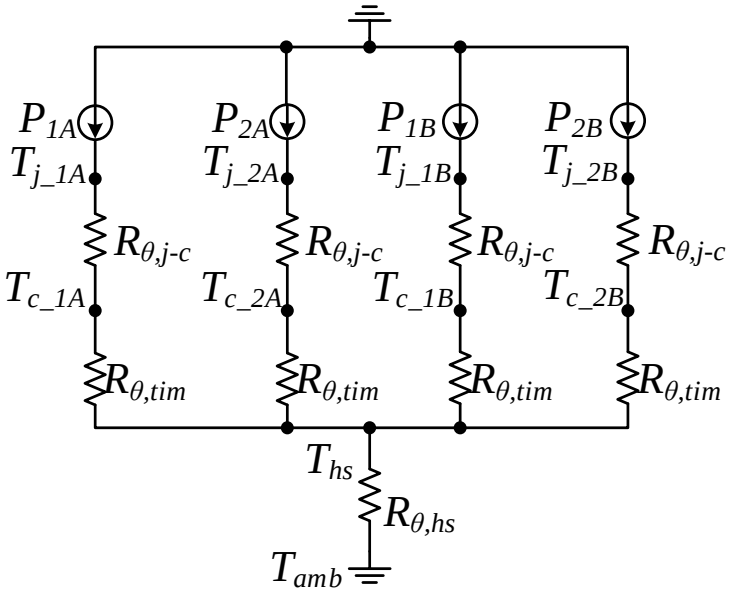


Figure 5-9. Static thermal model for loss and temperature calculation.

Table 5-4. Thermal resistance of components

Junction to case, ($R_{\theta,j-c}$)	TIM, ($R_{\theta,tim}$)	Heatsink, ($R_{\theta,hs}$)
1.0 °C/W	0.57 °C/W	0.22 °C/W

477000, and the selected TIM is TG-A126X. The thermal resistance of the TIM is calculated by

$$R_{TIM} = \frac{r_{TIM}}{A_{device}} (^{o}C/W), \tag{5-9}$$

where r_{TIM} is the specific thermal resistance of the TIM, and A_{device} is the area of the device surface that is attached to the TIM. In this case, r_{TIM} = 0.4 ºC*cm^2/W and A_{device} = 5.9 mm * 13.7 mm = 80.8 mm^2.

In Figure 5-9, P is the average power loss of each device over one line cycle; T_j is the junction temperature of each device; $R_{\theta,j-c}$ is the thermal resistance of the device, from junction to case; T_c is the case temperature of each device; $R_{\theta,tim}$ is the thermal resistance of the TIM; T_{hs} is the temperature of the heatsink surface near the devices; $R_{\theta,hs}$ is the thermal resistance of the heatsink; and T_{amb} is the ambient temperature.

In the static thermal model, T_j is assumed to be constant when the converter operates at thermal steady-state. The loss and junction temperature of devices can be calculated iteratively using the loss and thermal models of the device.

As for the passive components, the major loss is from inductors, including winding loss and copper loss. In this cases, GSE is used for core loss calculation [103]:

$$P_{core} = \frac{1}{T}\int_0^T k \left|\frac{dB}{dt}\right|^{\alpha} |B(t)|^{\beta-\alpha} dt \tag{5-10}$$

where T is the line frequency (60Hz); k, α, and β are Steinmetz parameters from datasheet.

As for the winding loss, the inductor current is first decomposed into components of different frequencies by Fast Fourier Transform (FFT), and then the loss at each frequency is calculated. The resistance at each frequency is calculated by Dowell's Equation:

$$R_w = R_{wDC} A\left[\frac{\sinh(2A)+\sin(2A)}{\cosh(2A)-\cos(2A)} + \frac{2(N_l^2-1)}{3}\frac{\sinh(A)-\sin(A)}{\cosh(A)+\cos(A)}\right] \quad (5\text{-}11)$$

where $R_{wDC} = \rho_w MN/A_w$ is the dc resistance of conductor; ρ_w is specific resistivity of copper; M is mean length per turn; N_l is number of turns; A_w is cross-sectional area of conductor; $A = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \frac{d}{\delta_w}\sqrt{\frac{d}{p}}$ for round conductor; d is diameter of conductor; $\delta_w = \sqrt{\rho_w/\pi\mu_0 f}$ is the skin depth of conductor at the frequency under consideration; p is the distance between the centers of the adjacent winding round conductor in the same layer; and μ_0 is permeability of free space, $4\pi \times 10^{-7}$ H/m [37, 104].

c) Converter Loss of Prototype

A prototype was built based on the selected components, as shown in Figure 3-20. The measured converter loss and calculation results using the basic loss model are summarized in Figure 5-10. In the testing, the dc input voltage is 450 V, RMS of output voltage is 230 V, and the ambient temperature is 25 °C. In the testing, the voltage, current, and power at the input and output terminals of the converter were measured by WT3000E, High Accuracy Power Analyzer from Yokogawa, using four-wire Kelvin connection. The power loss and efficiency of the converter are calculated accordingly. Compared to the testing results, the calculation shows 28% discrepancy at both heavy load (P_O = 4.5 kW) and light load (P_O = 500 W). The maximum loss difference between testing results and calculation is 30.6 W when the output power is 4.5 kW.

During testing, thermocouples were attached to the source terminals of the devices to estimate the case temperature, since the source terminals and case are connected internally by the device lead frames. The case temperature measurement setup is shown Figure 5-11.

The measured and calculated case temperatures of GaN transistors are summarized in

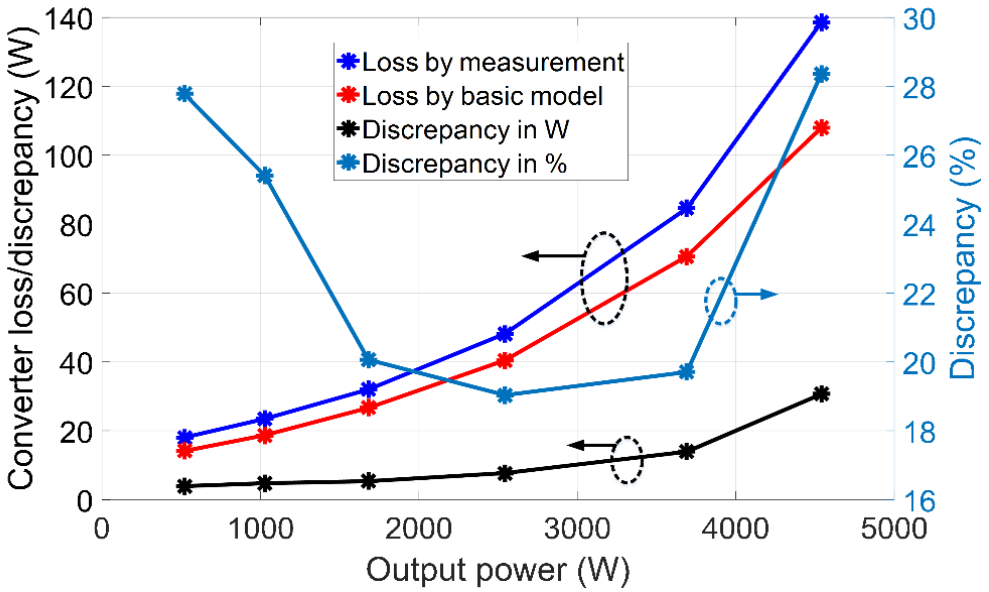


Figure 5-10. Converter loss of measured and calculated results using basic loss model.

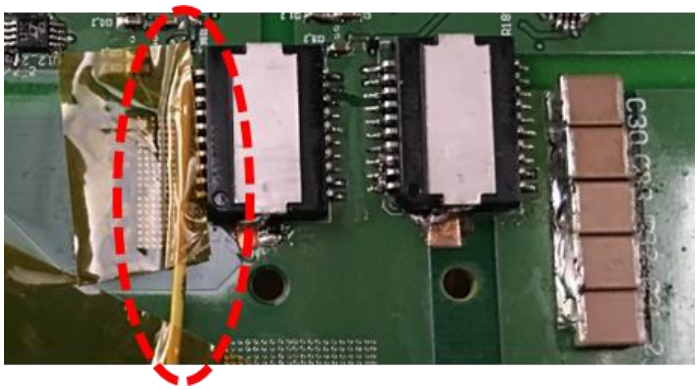


Figure 5-11. Case temperature of GaN GITs measured by thermocouple (highlighted by red circle).

Figure 5-12. In calculation, loss and case temperature of device S_{1A} are the same as device S_{1B}, and S_{2A} are the same as S_{2B}, due to the symmetry of the modulation. Also, calculated case temperature of S_{2A}/S_{2B} is higher than S_{1A}/S_{1B}, which is inconsistent with the measured results.

5.2 Factors and Considerations

From the results in last section, it is obvious that there are significant discrepancies between testing and calculation results when a basic loss model is used for the GaN-based inverter. This indicates that some factors about passive and active components need to be considered, and the thermal model of device also needs to be improved since temperature also affects the loss.

a) Impact of Parasitic Capacitance

In the DPT, C_p is typically minimized such that the intrinsic characteristics of the devices can be studied [109]. For example, four toroidal inductors are connected in series in the DPT, so that the EPC is only 11 pF. Also, a heatsink is not required in DPT, since the power dissipation is small.

However, in practical converters, heatsinks are needed for thermal design, which causes extra C_p across the devices. The power inductors are designed to meet filtering requirement. In the converter, power inductors are designed using air-gapped EE cores with two-layer windings, and the EPC is 33 pF. In addition, the PCB copper pour in the converter is larger compared to that in DPT, which causes additional C_p. Therefore, the switching loss results obtained from DPT need to be adjusted by considering the impacts of extra C_p.

The parasitic capacitance of the power inductor L_{1_1} (C_{p1_1}) is used as an example to derive the extra switching loss incurred by parasitic capacitance. During the positive half line cycle, S2B is constantly on, and S1A and S2A turn on and turn off alternatively, according to Figure 3-13.

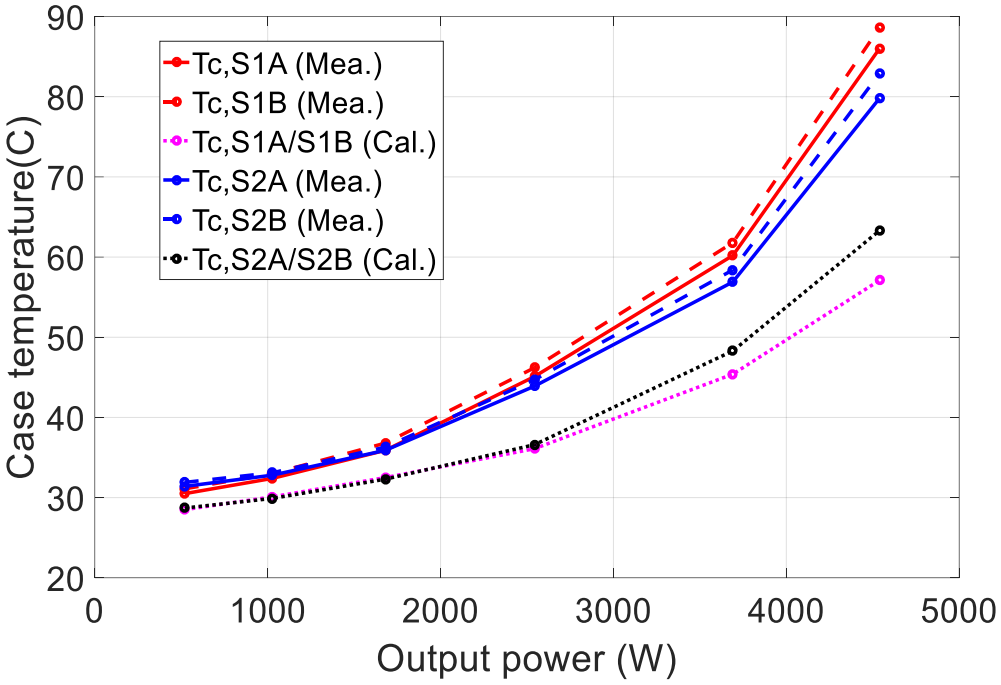


Figure 5-12. Case temperature measurement (solid and dashed lines) and calculation (dotted line).

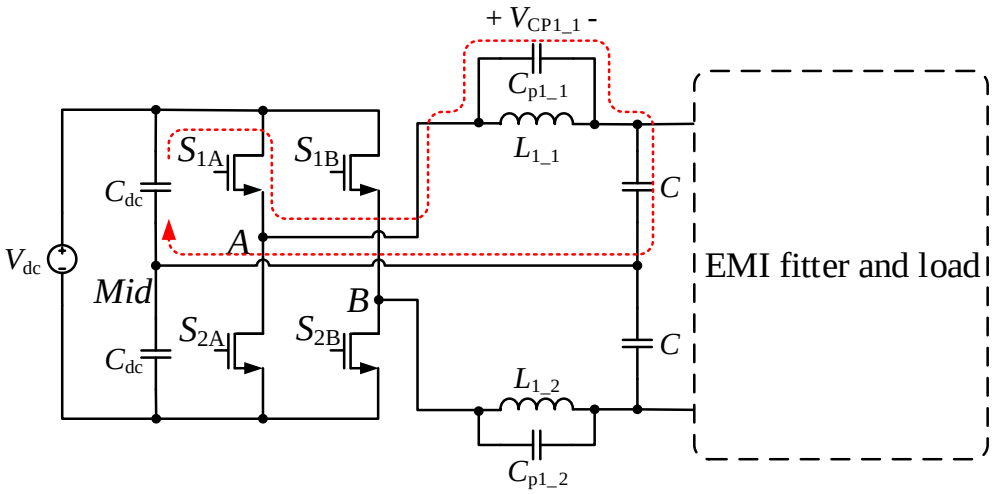


Figure 5-13. Charging process of C_{p1_1} during the turn-on transient of S1A.

The charging of C_{p1_1} occurs at the turn-on transient of S1A. The charging path and schematic of related components are shown in Figure 5-13. The voltage across C_{p1_1} increases from $-\frac{1}{2}V_{dc}-\frac{1}{2}V_{ac}$ to $\frac{1}{2}V_{dc}-\frac{1}{2}V_{ac}$ before and after turn-on of S1A. The main resistance in the charging path is the on-state resistance of S1A. Therefore, the extra loss to S1A due to C_{p1_1} is

$$E_{CP1_1}=\int_0^{\infty} v_{S1A}i_{S1A}\,dt=\int_{-\frac{1}{2}V_{dc}-\frac{1}{2}V_{ac}}^{\frac{1}{2}V_{dc}-\frac{1}{2}V_{ac}}\left(\frac{1}{2}V_{dc}-\frac{1}{2}V_{ac}-v_{cp1_1}\right)C_{p1_1}\,dv_{cp1_1}=\frac{1}{2}C_{p1_1}V_{dc}^2. \tag{5-12}$$

The above question shows that the extra loss to S1A due to C_{p1_1} is the same as that of parasitic capacitance in parallel to S1A.

Similarly, parasitic capacitance due to heatsink and PCB can also be modeled as the parallel capacitance of two devices in the same phase leg. Thus, the extra switching loss incurred by the parasitic capacitance when turning on active switch can be estimated by

$$E_{cap}=\frac{1}{2}C_{p,s1}V_{dc}^2+\frac{1}{2}C_{p,s2}V_{dc}^2=\frac{1}{2}C_{p,total}V_{dc}^2, \tag{5-13}$$

where $C_{p,s1}$ and $C_{p,s2}$ is the parasitic capacitance of two devices in the same phase leg, and $C_{p,total}$ = $C_{p,s1}$ + $C_{p,s2}$ is the total parasitic capacitance.

For a specific dead-time setting, the threshold load current that can fully recover the energy stored in the C_{oss} and achieve soft switching increases with C_p, since it effectively increases C_{oss} of the devices. Considering C_p, the minimum current that can fully discharge capacitance increases to

$$I_{th}=\frac{(2C_{oss}+C_{p,total})V_{dc}}{t_{dt}}. \tag{5-14}$$

For $I_d < I_{th}$, the voltage across synchronous switch when turning on is

$$\Delta V = V_{dc} - I_d \frac{t_{dt}}{2C_{oss}+C_{p,total}}. \quad (5\text{-}15)$$

Therefore, the "double switching" loss at the end of dead-time interval becomes

$$E_{dt_sw} = -\int_{\Delta V}^{0}\left(C_{oss}(v_c) + C_{p,syn}\right)v_c dv_c + \int_{V_{dc}-\Delta V}^{V_{dc}}\left(C_{oss}(v_c) + C_{p,act}\right)(V_{dc} - v_c)dv_c, \quad (5\text{-}16)$$

where $C_{oss}(v_c)$ is the voltage-dependent output capacitance of device, $C_{p,syn}$ and $C_{p,act}$ is the parasitic capacitance of synchronous and active devices, respectively.

b) Junction Temperature Variation

As the power loss is varying in one line cycle, and the thermal time constant of the device is comparable to the time duration of one line cycle, T_j can also vary significantly within one line cycle.

To model the dynamics of T_j and its impact, a dynamic thermal model using a multi-stage *R-C* network can be used for each device. As shown in Figure 5-14, it incorporates the thermal capacitance ($C_{\theta,i}$) in addition to thermal resistance ($R_{\theta,i}$).

During one line cycle, the case temperature has negligible variation due to the large thermal capacitance of the heatsink, and it can be assumed constant. Based on the thermal model in Figure 5-14, the transient thermal impedance from junction to case of the devices ($Z_{\theta,j\text{-}c}(t)$) is governed by

$$Z_{\theta,j-c}(t) = \frac{T_j(t)-T_c}{P(t)} = \sum_{i=1}^{i=n}(1 - e^{-\frac{t}{\tau_i}})R_{\theta,i}\ (°C/W), \quad (5\text{-}17)$$

where $\tau_i = C_{\theta,i} R_{\theta,i}$; T_c is case temperature of the device; $T_j(t)$ is the instantaneous junction temperature; $T_i(t)$ is the temperature of each node in the thermal model; and $i = 1,2,\ldots n$.

The thermal resistance and capacitance can be derived from the datasheet using curve fitting. In this case, the transient thermal impedance of the devices can be precisely modeled by a

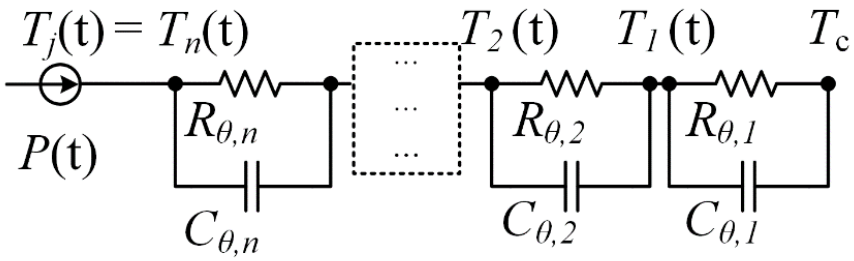


Figure 5-14. Dynamic thermal model of the device with *R*-*C* network.

three-stage *R*-*C* network as shown in Figure 5-15, and the derived parameters are listed in Table 5-5.

Therefore, each $R_{\theta j\text{-}c}$ in Figure 5-9 can be replaced by three pairs of *R*-*C* networks in series and the dynamic thermal model from the junction to the case for all four devices is depicted in Figure 5-16.

Based on the dynamic thermal model and time-varying power loss $P(t)$, the time-varying temperature at each node can be progressively calculated from the following set of discrete-time equations:

$$P(t+\Delta t)=\frac{T_1(t+\Delta t)-T_c}{R_{\theta,1}}+C_{\theta,1}\frac{T_1(t+\Delta t)-T_1(t)}{\Delta t}, \tag{5-18}$$

$$P(t+\Delta t)=\frac{T_2(t+\Delta t)-T_1(t)}{R_{\theta,2}}+C_{\theta,2}\frac{T_2(t+\Delta t)-T_2(t)}{\Delta t}, \tag{5-19}$$

$$P(t+\Delta t)=\frac{T_3(t+\Delta t)-T_3(t)}{R_{\theta,3}}+C_{\theta,3}\frac{T_3(t+\Delta t)-T_3(t)}{\Delta t}, \tag{5-20}$$

which can be simplified to:

$$T_1(t+\Delta t)=\frac{R_{\theta,1}P(t+\Delta t)+T_c+R_{\theta,1}C_{\theta,1}\frac{T_1(t)}{\Delta t}}{1+\frac{R_{\theta,1}C_{\theta,1}}{\Delta t}}, \tag{5-21}$$

$$T_2(t+\Delta t)=\frac{R_{\theta,2}P(t+\Delta t)+T_1(t+\Delta t)+R_{\theta,2}C_{\theta,2}\frac{T_2(t)+T_1(t+\Delta t)-T_1(t)}{\Delta t}}{1+\frac{R_{\theta,2}C_{\theta,2}}{\Delta t}}, \tag{5-22}$$

$$T_3(t+\Delta t)=\frac{R_{\theta,3}P(t+\Delta t)+T_2(t+\Delta t)+R_{\theta,3}C_{\theta,3}\frac{T_3(t)+T_2(t+\Delta t)-T_2(t)}{\Delta t}}{1+\frac{R_{\theta,3}C_{\theta,3}}{\Delta t}}. \tag{5-23}$$

Since the thermal time constant of the devices is much larger than the time duration of one switching cycle (7.41 μs), it is assumed that $T_i(t)$ is constant within one switching cycle, and therefore $\Delta t = 1/f_{sw}$. When the converter operates at thermal steady-state, the initial condition for $T_i(t)$ is

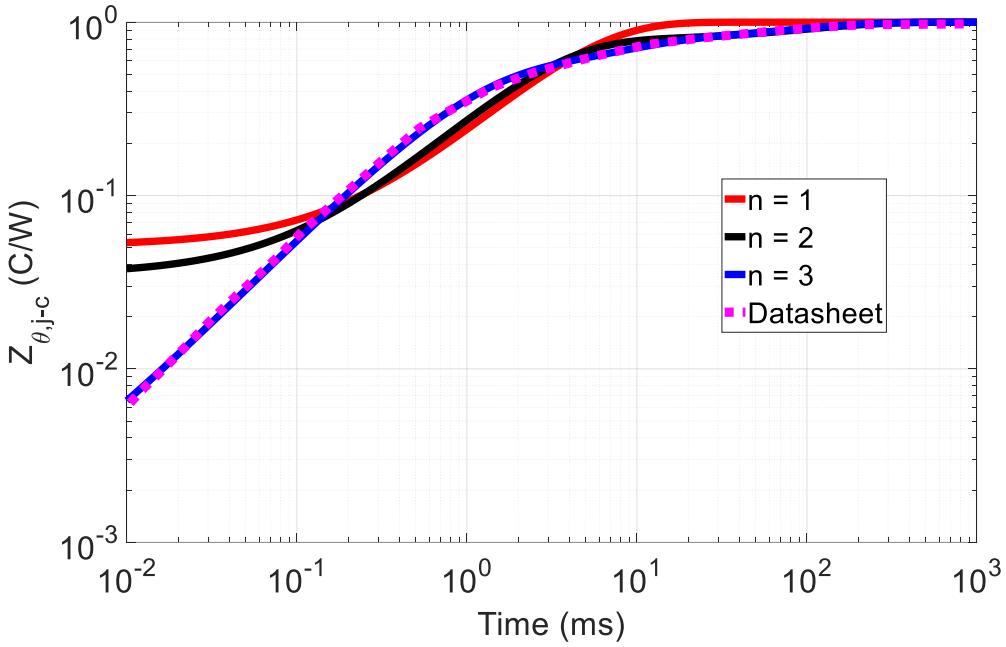


Figure 5-15. Curve fitting results of the thermal model for GIT devices.

Table 5-5. Parameters of the transient thermal model

i	Thermal resistance, $R_{\theta,i}$ (°C/W)	Thermal capacitance, $C_{\theta,i}$ (W·ms/°C)	Thermal time constant, τ_i (ms)
1	0.4724	1.9	0.896
2	0.3052	26.7	8.14
3	0.2215	432	96

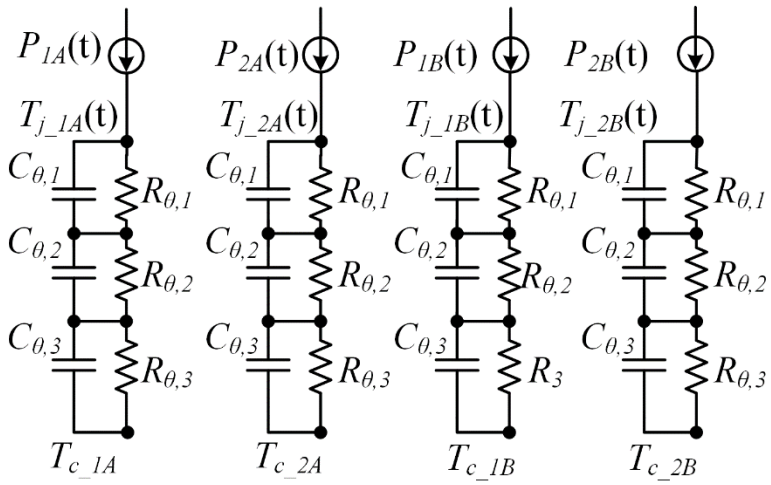


Figure 5-16. Dynamic thermal model from the junction to the case of the devices.

$$T_i(0) = T_i\left(\frac{1}{f}\right), i = 1, 2, 3. \quad (5\text{-}24)$$

where f is the line frequency, and it is 60 Hz in this converter.

It can be seen from above equations that time-varying power loss, $P(t)$, needs to be calculated for each switching cycle, including the conduction loss and switching loss.

For the conduction loss calculation, it is related to R_{dson}, drain current and junction temperature. Within each switching cycle, the junction temperature can be assumed constant, but the drain current is not constant. Therefore, to calculate the conduction loss, each switching cycle is equally divided into N sections. This is illustrated in Figure 5-17. Considering the current ripple, N needs to be sufficiently large such that the drain current can be approximately constant within each section. The instantaneous drain current in n^{th} section is denoted as $I_d(n)$. Then, the corresponding on-state resistance in this section, $R_{ds,on}(n)$, can be determined from (5-1). Finally, the conduction loss in the nth section, $P_{cond}(n)$, is calculated by

$$P_{cond}(n) = I_d^2(n) * R_{ds,on}(n) \text{ (W)}. \quad (5\text{-}25)$$

The average conduction loss in one switching cycle, $\overline{P_{cond}}$, is the average of conduction loss in these N sections:

$$\overline{P_{cond}} = \frac{1}{N}\sum_{n=1}^{N} P_{cond}(n) \text{ (W)}. \quad (5\text{-}26)$$

In this work, N is selected to be 50, since a larger N has negligible impact on the conduction loss calculation.

As for the switching loss and dead-time loss, the instantaneous current and junction temperature in each switching cycle is used for the calculation, based on (5-3) to (5-8). The total loss for one switching cycle is the sum of conduction loss, switching loss and dead-time loss. In

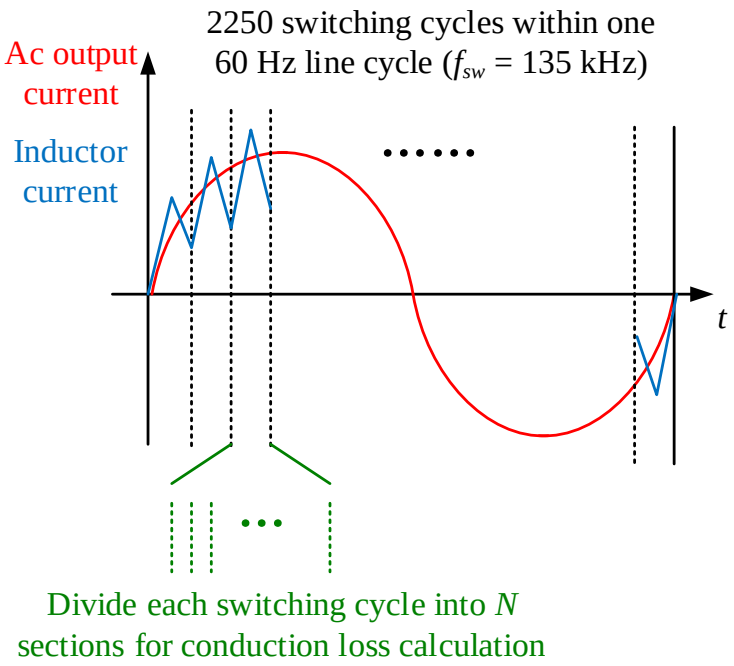


Figure 5-17. Loss calculation for one line cycle.

this case, there are 2250 switching cycles within one line cycle since the line frequency is 60 Hz and switching frequency is 135 kHz. Within one 60 Hz line cycle, the switching loss and dead-time loss are calculated 2250 times, while conduction loss is calculated 2250*50 = 112500 times.

c) Estimation of Case Temperature

According to (5-21) to (5-23), T_c is needed as an input to calculate $T_j(t)$. Therefore, it is critical to have an accurate estimation of T_c, which requires an accurate thermal model from the case of the devices to the ambient.

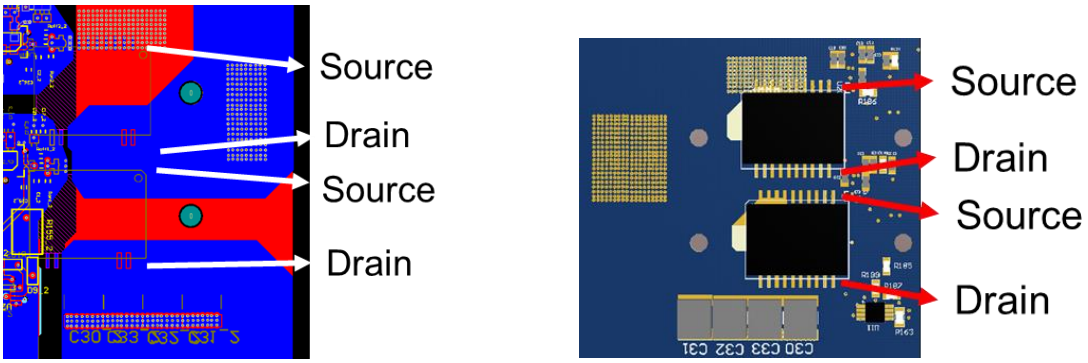
In this study, FEA software COMSOL is used for the case temperature estimation. Since GaN-based converters typically employ high-density layouts, thermal coupling and heat transfer through PCB copper pour need to be modeled in COMSOL. The 2D and 3D views of the PCB copper pour around two devices are shown in Figure 5-18, which is exported to the COMSOL simulation setup. The simulation setup and simulated temperature profile at P_o = 4.5 kW is shown in Figure 5-19.

d) Calcluation of Instantaneous Junction Temperature and Device Loss at Thermal Steady-State

The case temperature, instantaneous power loss, and junction temperature of each device at thermal steady-state can be calculated iteratively using COMSOL simulation and the dynamic thermal model, which is summarized by the flow chart in Figure 5-20. In the flow chart, subscript '*it*' denotes the iteration number, *k* is the notation of devices, P_{avg} is the average power loss of the device over one line cycle, including the switching and conduction loss, and $T_{tolerance}$ is the predefined tolerance for the case temperature.

The procedures to calculate the device loss can be explained by the following steps:

Step 1: Initialize T_c and T_j for each device. To reduce the number of iterations, the initial



(a) (b)

Figure 5-18. PCB copper pour around two devices in the same phase leg: (a) 2D view, and (b) 3D top view.

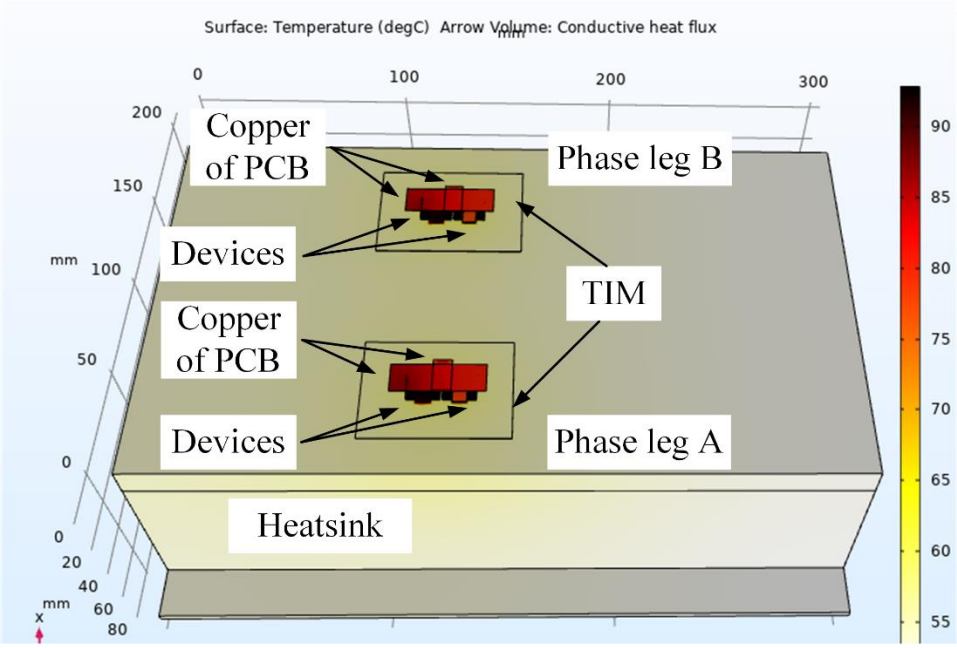


Figure 5-19. Simulation for case temperature in COMSOL.

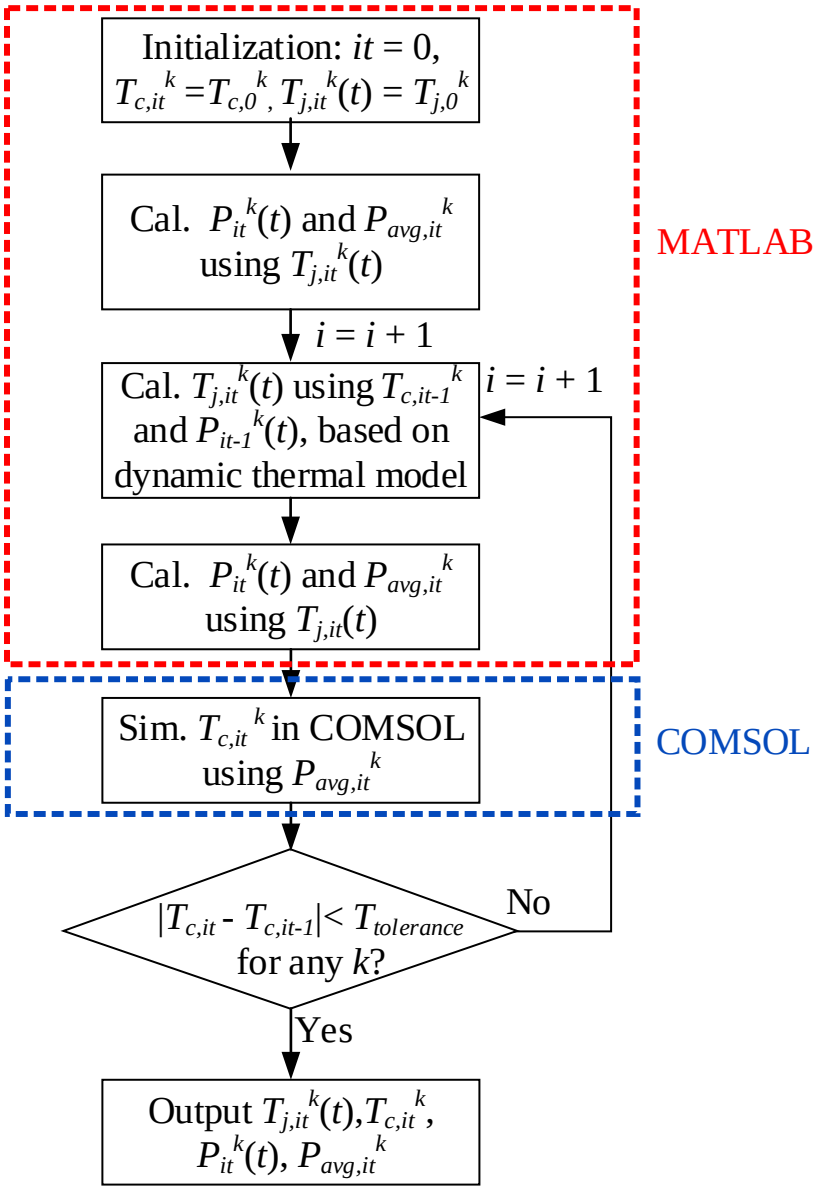


Figure 5-20. Flow chart for device loss and temperature calculation.

values can be the results obtained from the conventional thermal model which assumes that junction temperature is constant (Figure 5-9) At this step, it is also assumed that T_j is constant in the whole line cycle.

Step 2: Based on the initial constant T_j, calculate time-varying power loss $P(t)$ and average power loss of one line cycle for each device, P_{avg}.

Step 3: Using T_c, $P(t)$, and (5-21) to (5-24), calculate the time-varying junction temperature, $T_j(t)$, for each switching cycle.

Step 4: Based on $T_j(t)$ obtained in Step 3, calculate $P(t)$ for each switching cycle and update P_{avg} by using (5-1), (5-3), (5-25), and (5-26). In each switching cycle, conduction loss is the average of 50 sections, while switching and dead-time losses are calculated once.

Step 5: Simulate case temperature T_c using the P_{avg} obtained in Step 4.

Step 6: If T_c converges, stop calculation and output results; otherwise, go back to Step 3 with the updated T_c and $P(t)$.

Steps 1 to 4 were implemented in MATLAB while Step 5 in COMSOL.

Figure 5-21 shows the simulated case temperature and calculated loss of devices at the heavy load condition. To speed up the convergence, the initial case temperature was set to that obtained based on the static thermal model. It can be seen that the case temperature and device loss converge in 3 iterations, given that the tolerance of case temperature is 1 °C. Devices S_{1A} and S_{1B} have smaller loss but slightly higher case temperature than S_{2A} and S_{2B}, because of the PCB copper pour and strong coupling between S_{1A}/S_{1B} and S_{2A}/S_{2B}, which also agrees with the measurement.

To validate the accuracy of loss and thermal model, the case temperature obtained from measurement and FEA simulation are summarized in Figure 5-22. The maximum discrepancy on

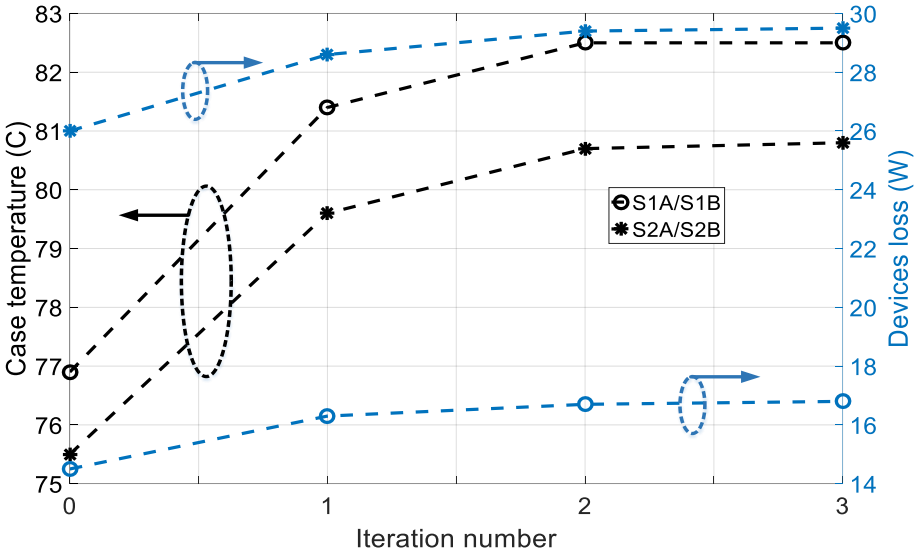


Figure 5-21. Simulated case temperature and calculated device loss in the first three iterations at P_o = 4.5 kW, V_{in} = 450 V, and V_o = 230 V_{rms}, using $T_{tolerance}$ = 1 °C.

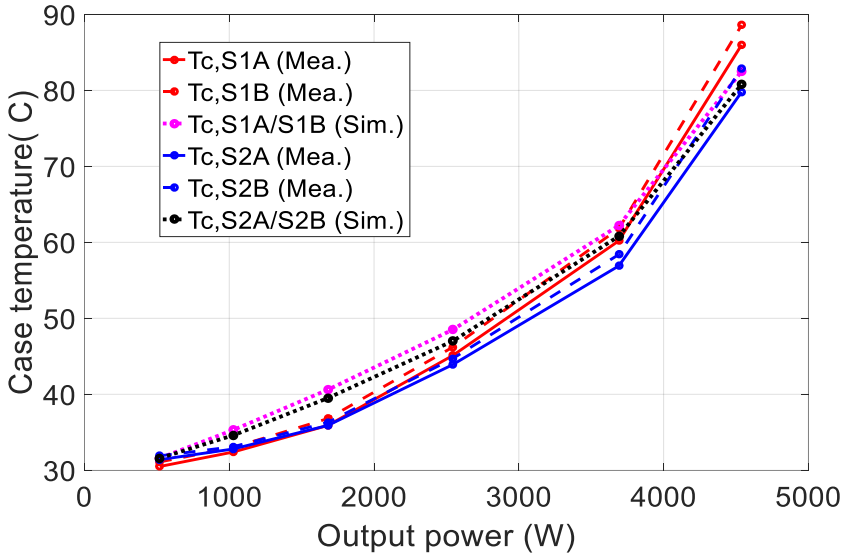


Figure 5-22. Case temperature of four devices in measurement (solid lines) and COMSOL simulation (dashed and dotted lines).

the case temperature between estimation and measurement is less than 6 °C.

Figure 5-23 and Figure 5-24 show the calculated instantaneous junction temperature and power loss of each device within one 60 Hz line cycle at the thermal steady-state, using the dynamic thermal model and measured T_c at P_o = 4.5 kW. Each junction temperature and power loss curve contains 2250 data points.

a) Filter Loss Considerations

An air gap is often used for inductors to avoid saturation. For a high-frequency, high-current converter, the air gap of the inductors can become non-negligible compared to the core size. The flux density of the single-phase EE core after considering the fringing effect can be approximated by

$$B = \frac{\mu_o N(a+l_g)(b+l_g)}{abl_g} i, \tag{5-27}$$

where a and b are the length and width of cross section of middle post, and l_g is the total length of air gap.

For the cores used in the prototype, E 55/28/21, and l_g of 4.5 mm, flux density increases by 53%, compared to the case when fringing effect is not considered. The core loss also increases as flux density increases.

Another important factor is the strong relationship between core loss density and core temperature. The Steinmetz parameters in the datasheet are typically specified at a certain temperature, and the core loss needs to be adjusted if operating at other temperatures. For example, the core loss density of R-material at 25 °C is more than two times higher compared to the value at 100 °C where the Steinmetz parameters are specified [102].

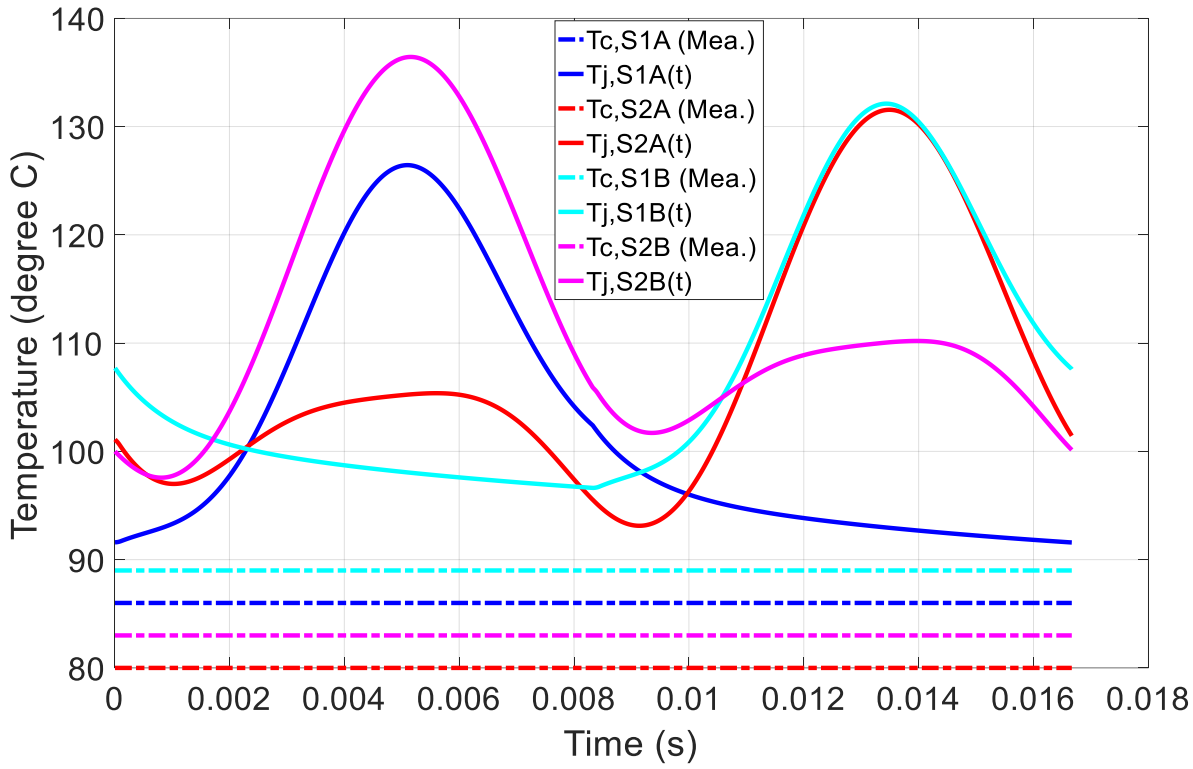


Figure 5-23. Dash-dot lines: constant case temperature of four devices at thermal steady-state from the measurement; Solid lines: calculated time-varying junction temperature of four devices using the measured T_c and thermal model in Figure 5-16, at P_o = 4.5 kW, V_{in} = 450 V, and V_o = 230 V_{rms}.

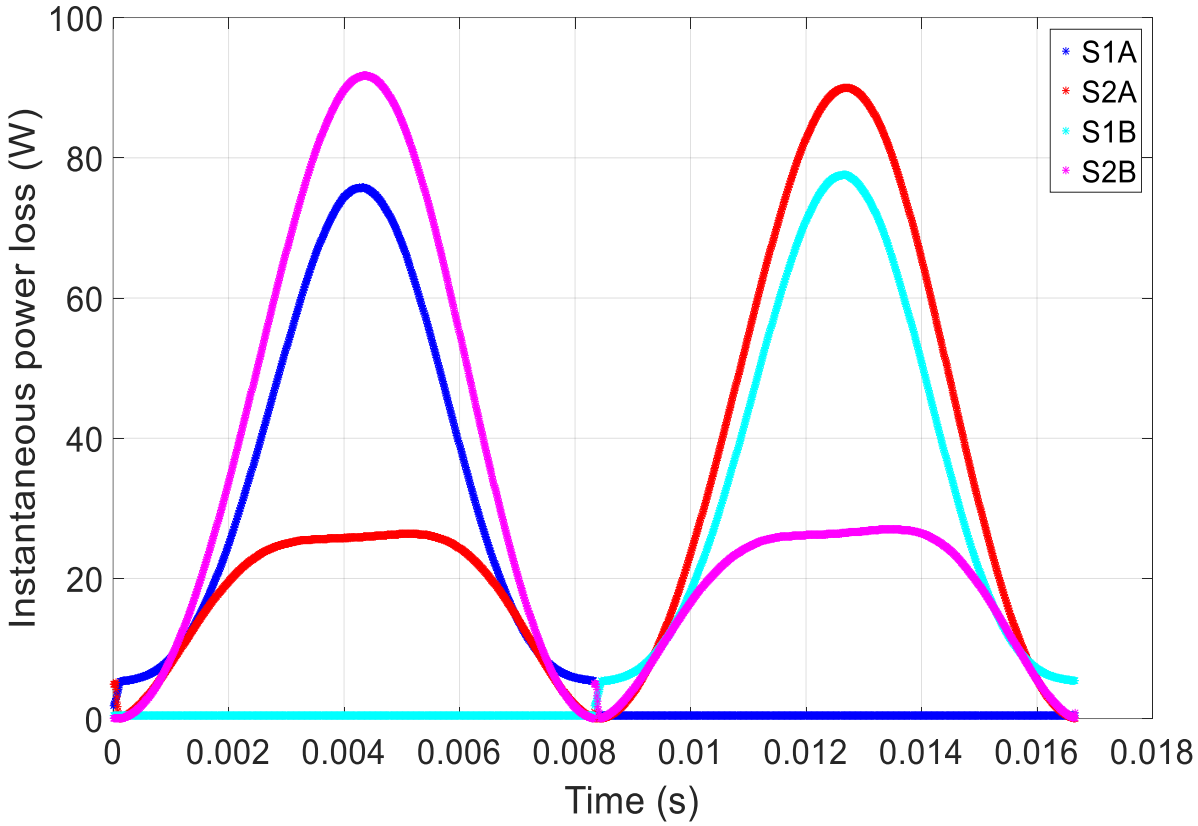


Figure 5-24. Calculated instantaneous power loss of each device at thermal steady-state based on the calculated instantaneous junction temperature in Figure 5-23, at P_o = 4.5 kW, V_{in} = 450 V, and V_o = 230 V_{rms}.

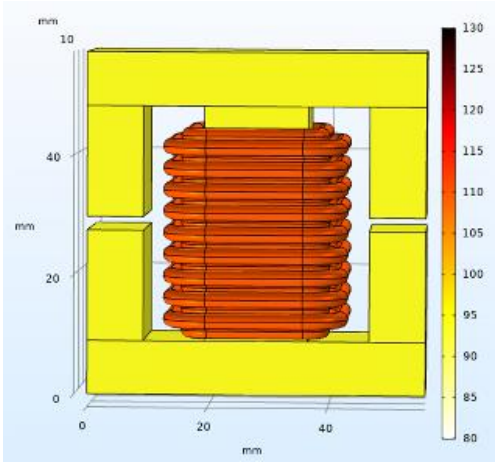
To estimate the core temperature, various thermal models of the magnetic components can be employed [38, 113]. In this work, the temperature of the magnetic core was simulated by COMSOL. During the test, core temperature was also measured by thermal camera when the converter reached thermal steady-state. The simulation setup and results are shown in Figure 5-25. The calculated core loss was adjusted according to the simulated core temperature and datasheet [114].

5.3 Impact of Each Factor

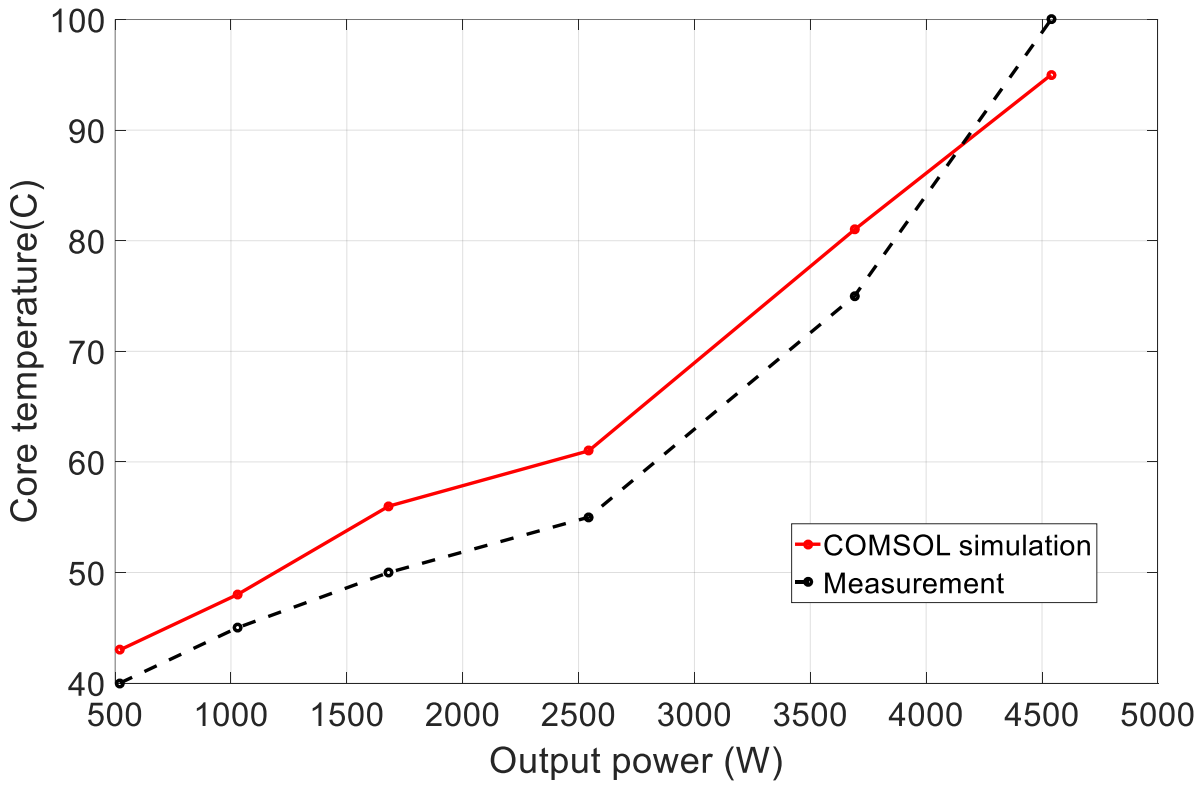
The factors discussed in the previous sections and the implementation methods are summarized in Table 5-6.

The converter loss discrepancy between measurement and calculation using basic and detailed models are plotted in Figure 5-26. The contribution of each factor to the original loss discrepancy is summarized in Figure 5-27. The loss discrepancy is the difference between measured loss and calculated loss. As more factors are considered, the loss discrepancy becomes smaller. At P_o = 2500 W and 3700 W, the remaining discrepancy becomes negative since the calculated converter loss is slightly higher than measured loss. The remaining discrepancy is within the error margin of power analyzer except at lightest load condition.

The results indicate that at the light load condition, passive components are the significant contributors to the discrepancy between basic model and measured results. Specifically, the inductor loss is sensitive to the core temperature at light load condition because core loss is inversely related to temperature. The thermal model and variation of T_j are not critical at light load. The impact of parasitic capacitance is also relatively small, because all four GITs are soft-switching due to current ripple during most of the line cycle. But the impact is expected to increase if higher



(a)



(b)

Figure 5-25. Thermal model of the magnetic core: (a) COMSOL simulation at P_o = 4.5 kW, V_{in} = 450 V, and V_o = 230 V_{rms}, and (b) comparison between simulation and measurement.

Table 5-6. Summary of factors and implementations

Factors	Basic model	Detailed model
Parasitic capacitance	Not considered	Equation (5-13)
T_c estimation	Thermal resistance	FEA Simulation
T_j variation	Constant T_j	Equations (5-21) and (5-24)
Inductor core flux	Fringing effect not considered	Equation (5-27)
Inductor core temperature	Temperature effect on loss not considered	Adjusted based on temperature and datasheet
Dc link capacitors	Not considered	Loss calculation tool [114]

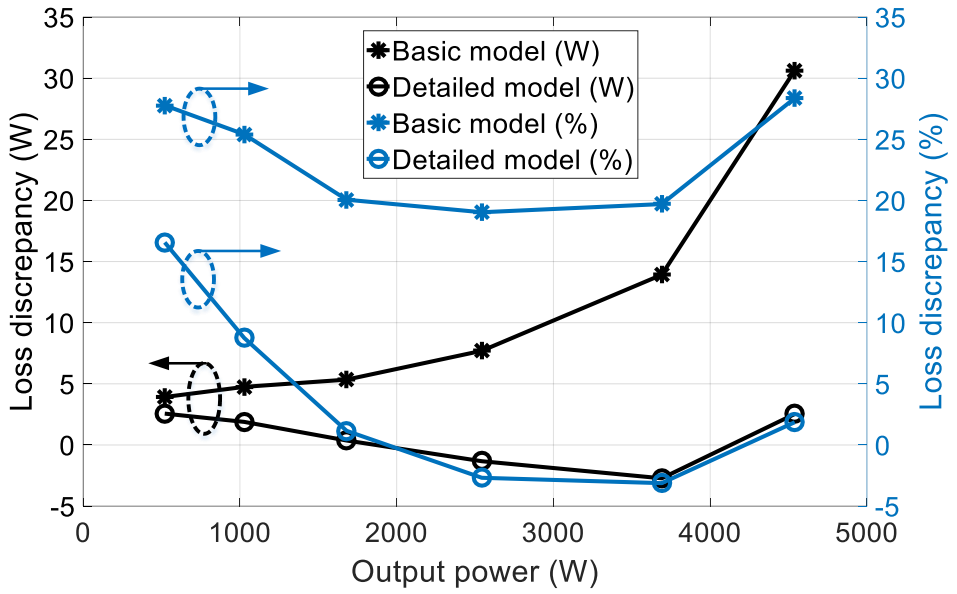
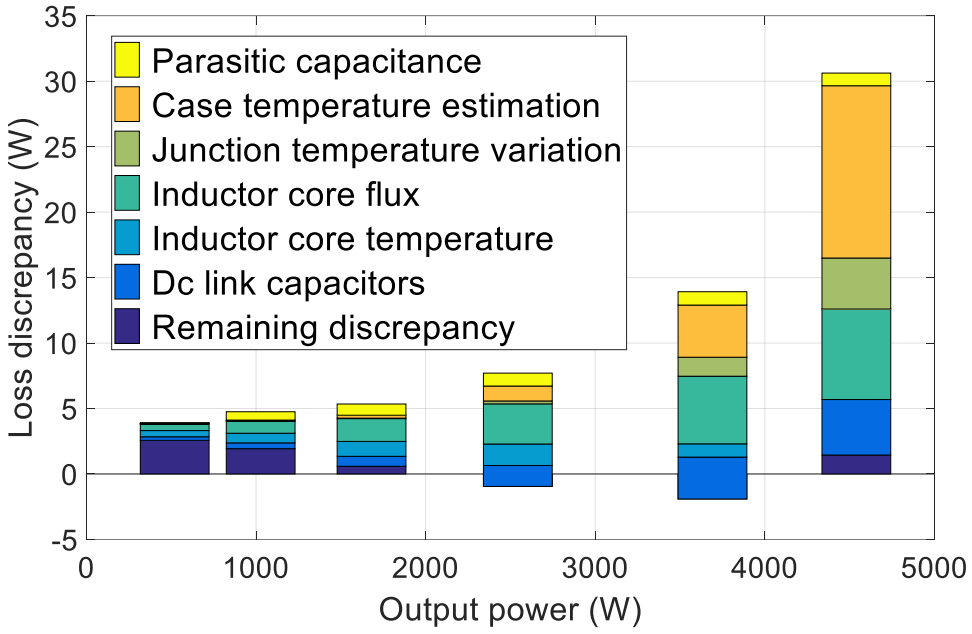
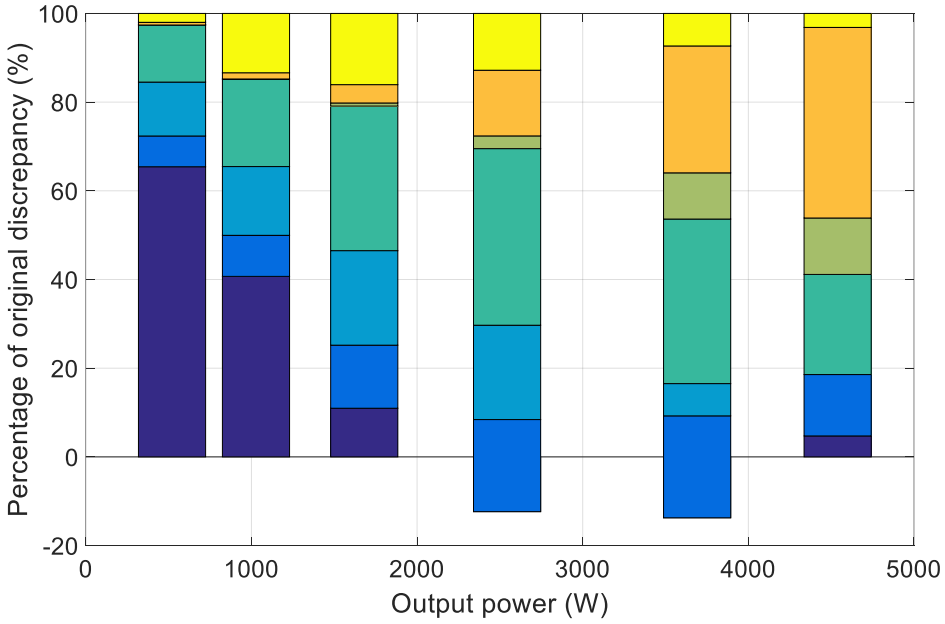


Figure 5-26. Converter loss discrepancy between measurement and calculation using basic and detailed loss models, in Watt and percentage.



(a)



(b)

Figure 5-27. Contribution of each factor to the original loss discrepancy: (a) in Watt, and (b) in percentage (%).

switching frequency is used.

As the loading increases, the estimation of case temperature, R_{dson} variation, and T_j variation become more important. R_{dson} increases significantly at high T_j and I_d, as can be seen in Figure 5-4. Since the device temperature is underestimated in the basic model using lumped thermal resistance, the loss discrepancy can be significantly reduced when more accurate case and junction temperatures are used. For parasitic capacitance, it causes similar among of loss when output power is 1000W or above because of hard switching.

5.4 Impact of Varying Junction Temperature on Loss for Different devices

a) Device selection

To have more generic conclusions about the impacts of varying junction temperature on the loss of dc-ac converter, and to provide more general guidelines for modeling the device loss, the impacts of varying junction temperature on converter loss are studied in other devices. A more generic single-phase full-bridge dc-ac converter shown in Figure 5-28 is used. The parameters of the converter are listed Table 5-7.

Four devices with similar voltage and current ratings but different dynamic thermal impedance and electrical characteristics were selected, which is summarized in Table 5-8 and Figure 5-29. Devices #1 and #2 are both GaN device, but the thermal impedances and the relationship between on-state resistance and junction temperature are different. These two devices will show how static thermal impedance and on-state resistance affect the variation of junction temperature and the associated conduction loss change. For devices #1, #3 and #4, the static thermal resistance is similar, so the impacts due to dynamic thermal impedance and on-state resistance can be evaluated.

a) Parameters of Four Devices

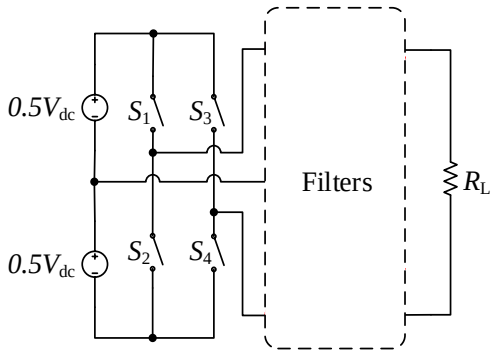


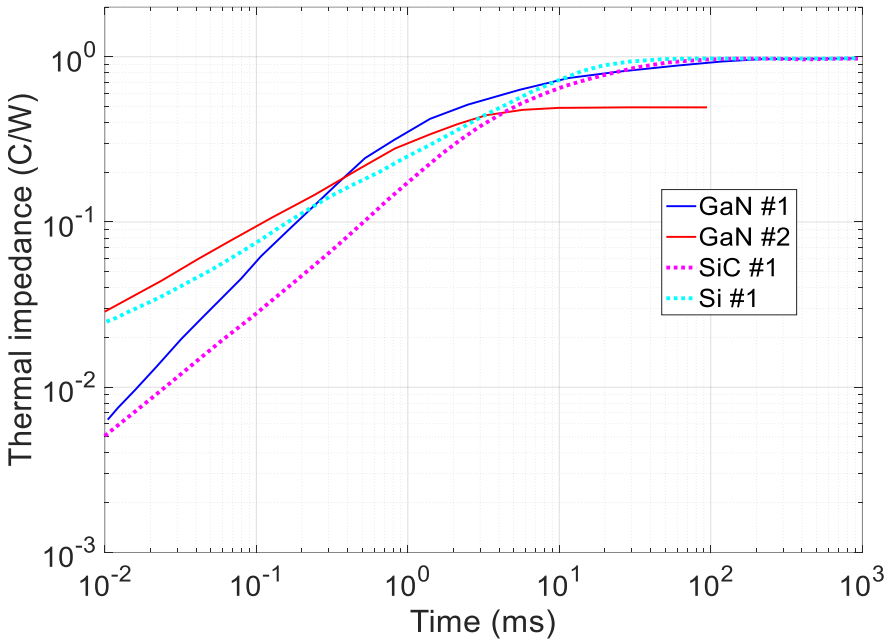
Figure 5-28. Topology of single-phase FB dc-ac inverter.

Table 5-7. Parameters of single-phase FB dc-ac converter

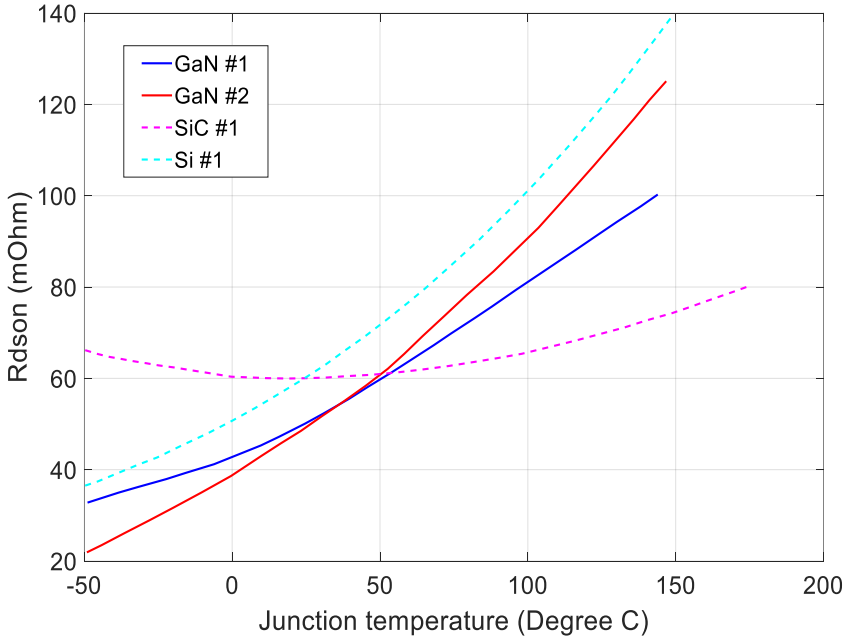
Parameters	**Values**
Input voltage, V_{in} (V)	450
Output voltage, V_o (V_{rms})	230
Output power, P_o (W)	4000
Inductor peak-to-peak current ripple (%)	20

Table 5-8. Thermal and electrical characteristics of selected devices

	GaN #1	**GaN #2**	**SiC #1**	**Si #1**
V/I ratings	600V/31A	650V/30A	650V/37A	650V/37A
Thermal resistance	1 °C/W	0.5 °C/W	0.99 °C/W	0.97 °C/W
R_{dson} @25°C	55 mΩ	50 mΩ	60 mΩ	69 mΩ
ton/toff	24 ns/28 ns	9.2 ns/11.6 ns	19 ns/22 ns	25 ns/75 ns



(a)



(b)

Figure 5-29. Characteristics of four selected devices: (a) dynamic thermal impedance; (b) on-state resistance vs. junction temperature.

Each curve in Figure 5-29 is approximated by exponential or polynomial equations using curve-fitting methods, so that the data can be used in the calculation. For thermal impedance, (5-17) can be applied, and 3 to 5 orders are used. As for on-state resistance, the dependence of R_{dson} on drain current is neglected since the data is not always available in device datasheet. Polynomial equations of 3rd or 2nd order are used for modeling the relationship between drain current and junction temperature.

$$R_{dson} = a * T_j^3 + b * T_j^2 + c * T_j + d. \tag{5-28}$$

The parameters for all four devices are summarized in Table 5-9 and Table 5-10.

b) Calculation of Junction Temperature and Loss

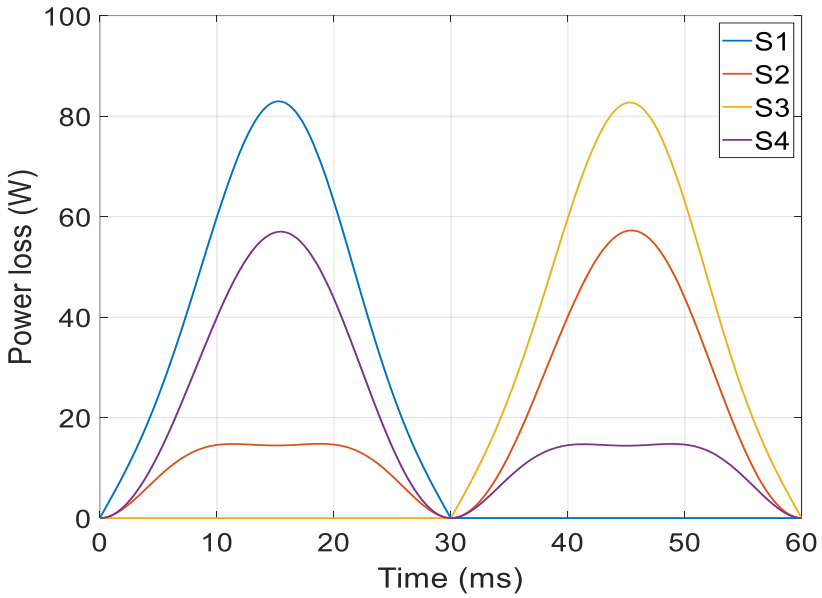
To evaluate the impacts of varying junction temperature, the results with varying junction temperature and constant junction temperature are compared. In the calculation, it is assumed that that the case temperature is 80°C. Note that the switching frequency of GaN and SiC converters are 135kHz, while Si converter is 20 kHz due to the maximum junction temperature of S1/S3. But this does not affect the results of S2/S4. The instantaneous junction and power loss of S1 to S4 in the four converters are plotted in Figure 5-30 to Figure 5-33, and a summary is in Table 5-11. The peak power loss and junction temperature both occur around the peak of current, and minimum values occur around zero crossing. Take GaN #1 as an example, the maximum and minimum junction temperature of S2/S4 is 115 °C and 88.5 °C, respectively. The average junction temperature of S2/S4 over one line cycle is 98 °C after considering junction temperature variation. The calculated conducted loss of S2/S4 is 19W and 19.5W for with and without considering the junction temperature, which is around 3% increase. There is more increase for S1/S3 since the temperature variation is larger due to switching loss, but the amount depends on the switching

Table 5-9. Coefficients for curve-fitting thermal impedance

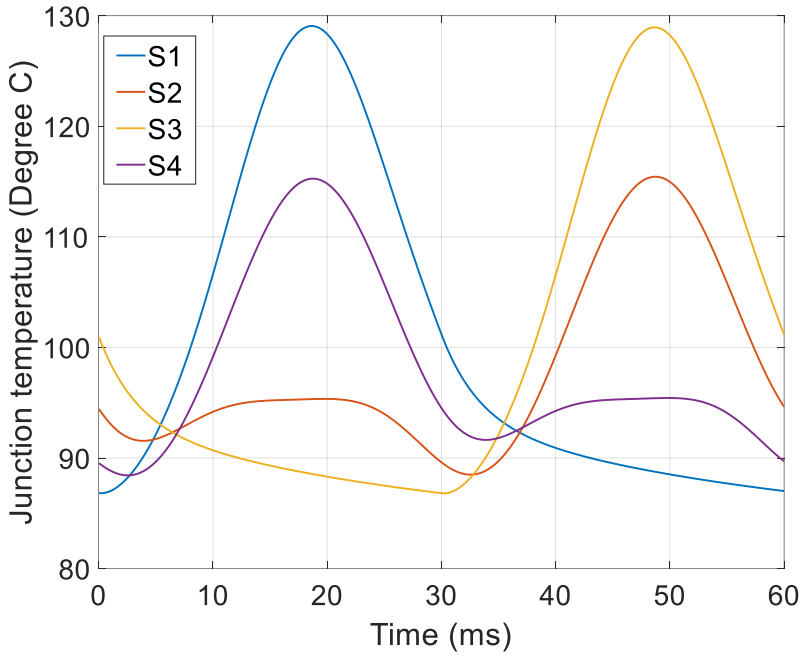
	GaN #1	**GaN #2**	**SiC #1**	**Si #1**
$R_{\theta,1}$ **(°C/W)**	0.47	0.20	0.47	0.72
$R_{\theta,2}$ **(°C/W)**	0.31	0.16	0.46	0.13
$R_{\theta,3}$ **(°C/W)**	0.22	0.09	0.04	0.10
$R_{\theta,4}$ **(°C/W)**	N/A	0.03	0.03	N/A
$R_{\theta,5}$ **(°C/W)**	N/A	0.008	N/A	N/A
$C_{\theta,1}$ **(W·ms/°C)**	1.9	10.3	47.7	12.9
$C_{\theta,2}$ **(W·ms/°C)**	26.7	7.1	7.1	14.4
$C_{\theta,3}$ **(W·ms/°C)**	432	2.4	16.7	2.0
$C_{\theta,4}$ **(W·ms/°C)**	N/A	0.42	$2.36*10^{5}$	N/A
$C_{\theta,5}$ **(W·ms/°C)**	N/A	25920	N/A	N/A

Table 5-10. Coefficients for curve-fitting on-state resistance

	GaN #1	**GaN #2**	**SiC #1**	**Si #1**
a	$-5.14*10^{-3}$	0	0	0
b	$1.7*10^{-3}$	$1.4*10^{-3}$	$9.16*10^{-4}$	$1.66*10^{-3}$
c	0.299	0.390	0.047	0.346
d	46.55	38.48	61.01	50.28

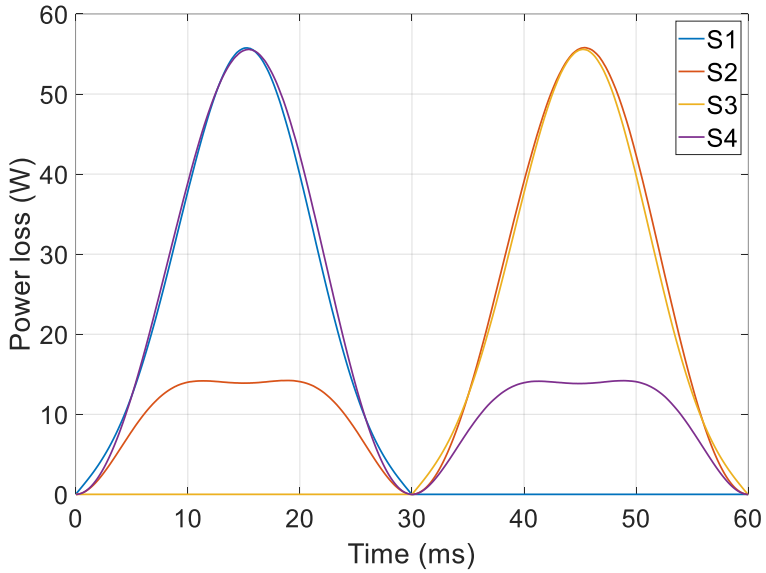


(a)

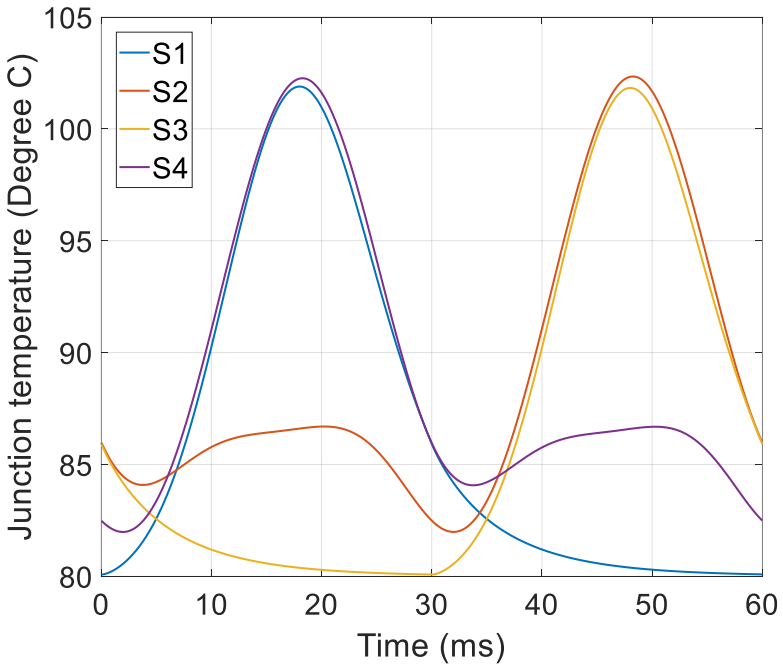


(b)

Figure 5-30. Converter using GaN #1 (a) instantaneous power loss, and (b) instantaneous junction temperature.

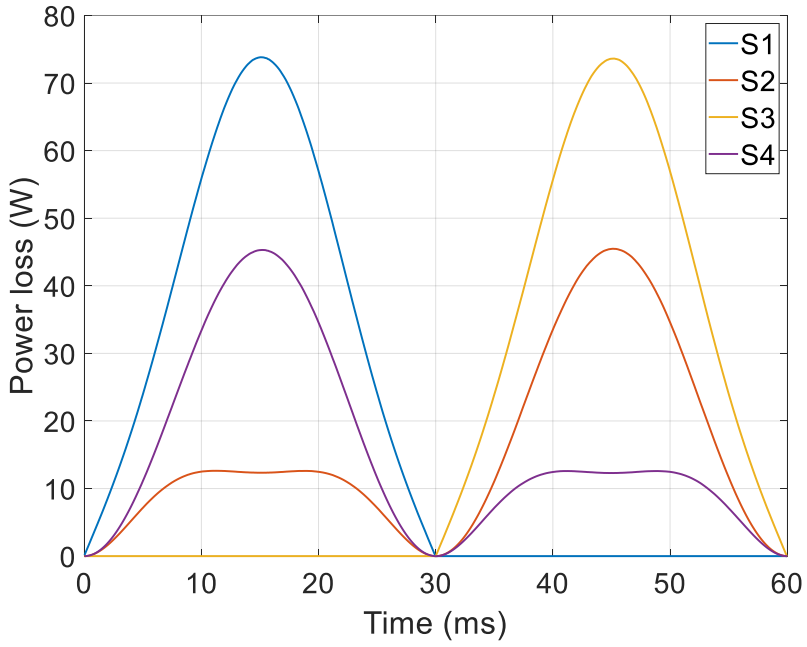


(a)

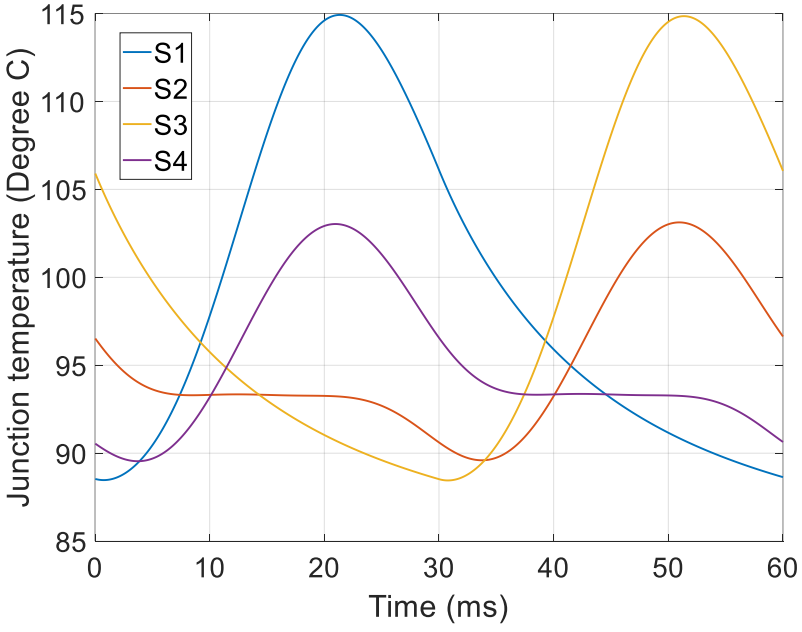


(b)

Figure 5-31. Converter using GaN #2 (a) instantaneous power loss, and (b) instantaneous junction temperature.

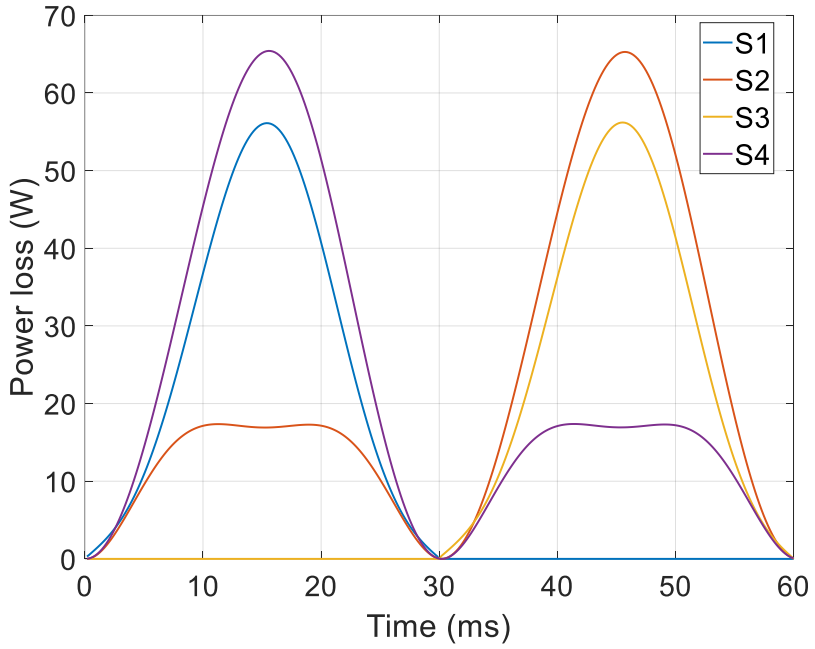


(a)

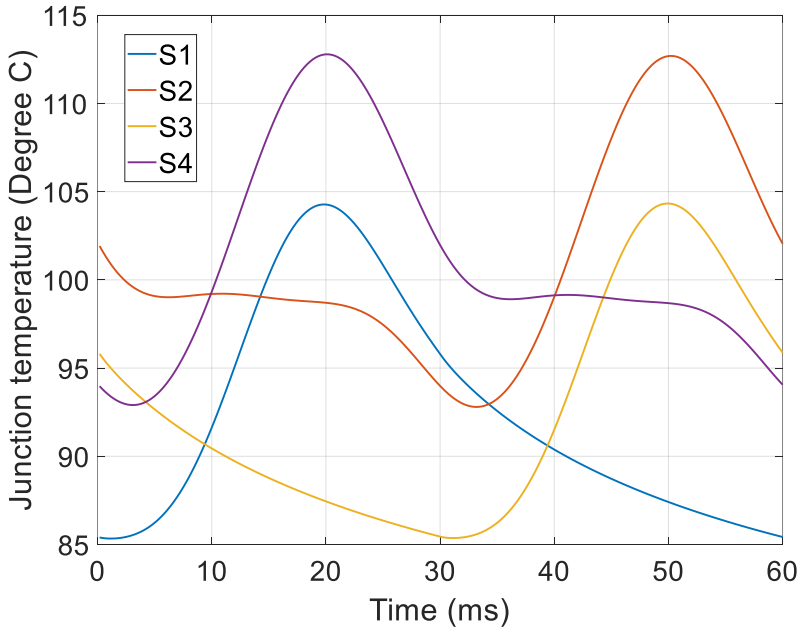


(b)

Figure 5-32. Converter using SiC #1 (a) instantaneous power loss, and (b) instantaneous junction temperature.



(a)



(b)

Figure 5-33. Converter using Si #1 (a) instantaneous power loss, and (b) instantaneous junction temperature.

Table 5-11. Summary of results for four devices

	GaN #1	**GaN #2**	**SiC #1**	**Si #1**
T_{max}, T_{min}, **and** T_{max} - T_{min} **of S2/S4 (°C)**	115, 88, 27	102, 82, 20	103, 90, 13	113, 93, 20
Loss of S2/S4 (W)	19	18.5	15.7	22.1
S2/S4 loss increase (W, %)	0.5 W, 3%	0.7 W, 4%	0.1 W, 0.6%	0.6 W, 3%

frequency and switching loss

c) Guidelines to Consider the Impacts

From the above results, some guidelines on the varying junction temperature and the corresponding impacts can be generated:

1) Devices with smaller thermal resistance, such as GaN #2, can reduce the average junction temperature, and therefore also reduce the variation of temperature;
2) If thermal resistances of the devices are similar, such as GaN #1, SiC #1 and Si #1, higher the transient thermal impedance at time around 1/2T, larger the junction temperature variation;
3) For R_{dson} with low dependence on T_j, such as SiC #1, temperature variation causes slight change on the conduction loss, and vice versa.

5.5 Summary

In this chapter, several factors and considerations in the converter loss calculation are systematically investigated. The factors include impact of parasitic capacitance, dynamics of junction temperature due to time-varying power loss, case temperature estimation, and detailed considerations of the filter loss. The impact of each factor is quantified at both light and heavy load conditions. It is found that at light load condition, the inductor loss is the main contributor to the loss discrepancy, while the devices loss and thermal model become more critical as loading increases.

Also, the implementation of each factor, including the equations and simulation setups are presented in detail. A method to calculate the time-varying power dissipation and junction temperature is proposed and implemented. Compared to the basic loss model, the loss discrepancy between measurement and calculation has been reduced from 28% to less than 3% at light load.

Moreover, the case temperature of the GaN devices in the measurement and estimation is within 6 °C. The methods and results enable a more accurate design for GaN-based converters.

To provide more general guidelines for converter designers, one of the factors, dynamics of junction temperature due to time-varying power loss, is also applied to generic single-phase full-bridge dc-ac inverter. Four different devices, including two GaN devices, one SiC and one Si, are selected and compared. The impacts of varying junction temperature and power loss are quantified. From the calculation results, the guidelines for proper device selection are generalized considering this factor.

Chapter 6 Cost Comparison between GaN-based and Si-based PV Inverters

6.1 Converter Overview

As shown in Figure 6-1, the topology used is a single-phase full-bridge inverter with virtual ground connection, which can effectively reduce the leakage current. Each parasitic capacitance between dc input and ground (C_{dc}) is 200 nF. Si IGBTs, Si MOSFETs, GaN high-electron-mobility transistors (HEMTs), and combinations of these devices are considered for four switches (S_{1A}, S_{2A}, S_{1B}, and S_{2B}).

To meet total harmonics distortion (THD) requirement and electromagnetic interference (EMI) standard, the filters consist of an *LC* power filter and EMI filters. Both one-stage *LC* and two-stage *LCLC* are considered for EMI filters. Based on the commercially available Si-based inverter, the specifications are listed in Table 6-1.

Discontinuous modulation was selected due to consideration of filtering requirement. Phase leg A is modulated in the positive half of the fundamental cycle, while phase leg B is modulated in the negative half cycle. When S_{2A} and S_{2B} are implemented by Si MOSFETs or GaN HEMTs, synchronous switching is used to reduce the loss during reverse conduction.

6.2 Cost Models

Since Si and GaN devices have different switching loss, the feasible range of switching frequency is different. Therefore, the components that are not significantly affected by the switching frequency are not considered, such as dc-link capacitors. The cost of auxiliary circuits, including isolated power supply and gate driver, are also not quantified in this study. The cost of

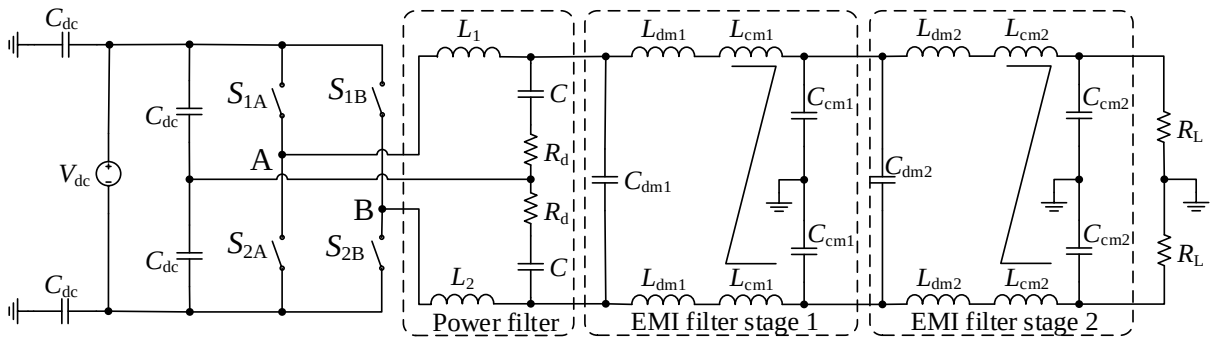


Figure 6-1. Topology of single-phase full bridge inverter. Four switches (S_{1A}, S_{2A}, S_{1B}, and S_{2B}) are implemented by Si MOSFETs, Si IGBTs, or GaN HEMTs.

Table 6-1. Specifications and parameters of the inverters

Input voltage (V_{in})	450 V
Output voltage (V_o)	210 - 230 V_{rms}
Output frequency (f_o)	60 Hz
Output power (P_o)	0 - 4.5 kW
CEC efficiency	> 97.8%
THD	< 3%
EMI standard	FCC part 15 Class B
Ambient temperature (T_{amb})	45 °C
Cooling	Natural convection

the components under consideration are based on the unit price at high quantity from manufacturers and distributors. The prices were quoted in Summer 2020.

a) Devices

Considering the dc input voltage, 600/650V devices are selected for the implementation of the four switches. For the Si-based converter, twelve different Si MOSFETs from three companies (Infineon, ON Semiconductor, and Vishay) are considered for the active switches (S_{1A} and S_{1B}) and the synchronous switches (S_{2A} and S_{2B}). Eight different Si IGBTs from three companies (Infineon, ON Semiconductor, and STMicroelectronics) are considered for the synchronous switches only, because IGBTs have high switching loss due to low switching speed and large tail current.

As for GaN-based converter, 600V, 31 A-rated top-cooled gate injection transistor (GIT), IGOT60R070D1, from Infineon is selected for all four switches.

The major characteristics and cost of the twelve pre-selected Si MOSFETs and Si IGBTs are listed in Table 6-2 and Table 6-3, respectively. For GaN devices, the cost is $15.04. The costs of the Si and GaN devices were quoted from Digi-Key [115], based on the unit price of 1000 devices.

b) Filters

The main components for filters include inductors, capacitors, and damping resistors. For inductors, costs of various magnetic cores and magnet wire are considered. Specifically, for power filter inductors, both single-phase EE ferrite cores and toroidal powder cores are considered. Toroidal ferrite cores with high permeability are selected to design common mode (CM) inductors. Differential mode (DM) inductance is provided by the leakage inductance of CM inductors [116]. All the cores are from Magnetics [117]. The magnetic cores considered in this study are

Table 6-2. Preselected Silicon MOSFETs

Manufacturer	#	Part number	Q_{rr} (µC)	R_{dson} (mΩ)	Cost ($/1k)
Infineon (CoolMOS)	1	IPW65R019C7	20	17	12.79
	2	IPW65R045C7	13	40	6.57
	3	IPW65R037C6	36	33	8.78
	4	IPW65R070C6	19	63	5.21
ON Semiconductor (SuperFET)	5	FCH023N65S3	17.9	19.5	7.16
	6	FCH041N65EF	1.5	36	5.48
	7	FCH040N65S3	13.6	35.4	4.49
	8	FCH067N65S3	9.2	59	2.67
Vishay (E series)	9	SiHS90N65E	26	25	12.82
	10	SiHG61N65EF	2.1	41	8.11
	11	SiHG64N65E	18	47	8.77
	12	SiHG44N65EF	1.5	63	5.32

Table 6-3. Preselected Si IGBTs

Manufacturer	#	Part number	Q_{rr} (µC)	V_{CES} (V)	V_F (V)	Cost ($/1k)
Infineon	a	IKZ75N65EL5	1.3	1.1	1.4	5.10
	b	IKW50N65WR5	1.8	1.4	1.4	2.36
	c	IKW40N65WR5	1.6	1.4	1.4	1.98
	d	IKW30N65EL5	0.91	1.05	1.35	2.78
ON Semiconductor	e	FGA40T65UQDF	0.29	1.33	1.5	2.31
	f	FGA40T65SHDF	0.34	1.45	1.5	2.7
STMicroelectronics	g	STGW75M65DF2	1.7	1.65	2	2.85
	h	STGWA50M65DF2	1.4	1.65	1.85	2.03

summarized in Table 6-4.

The other part of inductor is winding, which is implemented by round magnet wire. The insulation material is polyurethane with thermal class of 200 °C. The price at high-quantity was quoted from Bulk Wire [118]. and the cost for AWG from 10 to 20 are summarized in

Table 6-5. For other gauge numbers, the cost is scaled based on price at AWG 10 and the cross-sectional area.

The capacitors in power filters and DM capacitors in EMI filters are film capacitors. CM capacitors are disc ceramic capacitors. Both CM and DM capacitors are safety certified. The cost of capacitors was based on the unit price on Digi-Key.

c) Heatsinks

The selected heatsink type is extrusion fin made of aluminum. Considering the loss of devices, the thermal resistance under natural convection ranges from 0.14 to 0.95 °C/W.

To establish the cost model of heatsinks, 33 commercial heatsinks are surveyed, and the relationship between the unit price at high-quantity and thermal resistance under natural convection is modeled using curve-fitting method

$$y = 127.19x^2 - 241.58x + 139.12 \ (\$) \tag{6-1}$$

where x is the thermal resistance under natural convection (°C/W) and y is the cost of heatsink.

6.3 Electrical and Thermal Models

a) Devices Losses

The main loss mechanisms of the devices are switching loss and conduction loss. The losses of Si devices are calculated based on the datasheet, while for GaN devices, the losses are characterized experimentally.

Table 6-4. Preselected magnetic cores

Inductors	Core shapes	Materials	Core sizes
Power filter inductors	Single-phase EE cores	Ferrite (R material)	EE 25/10/13 ~ EE 100/59/27
	Toroidal	Powder (Kool Mμ)	OD = 21.1 ~ 134 mm
CM inductors	Toroidal	Ferrite (W material)	OD = 2.54 ~ 140 mm

Table 6-5. Cost of round magnet wire from Bulk Wire

AWG	10	12	14	16	18	20
Cost ($ per m)	1.86	1.22	0.78	0.50	0.33	0.21

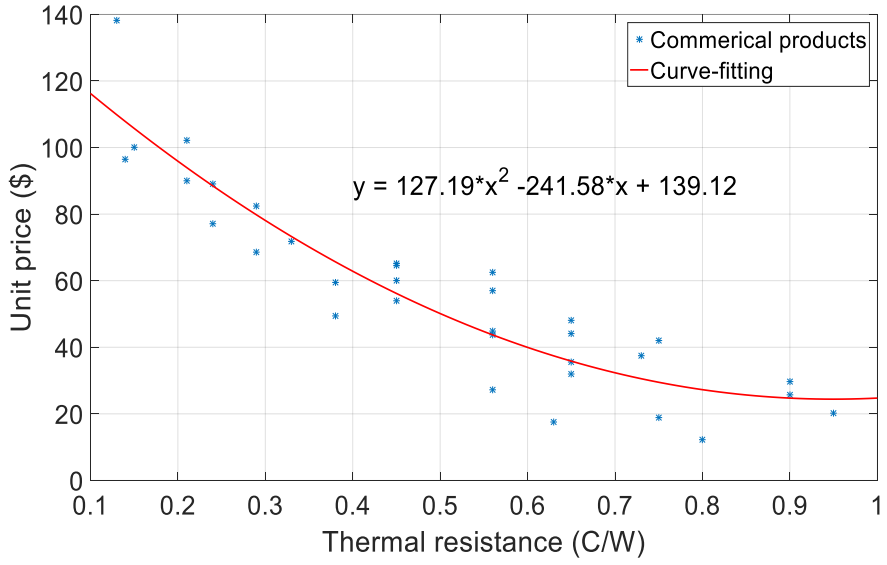


Figure 6-2. Relationship between thermal resistance under natural convection and unit price at high quantity for 33 commercial aluminum extrusion fin heatsinks.

In all Si MOSFETs case, the MOSFET has both conduction and switching loss. The switching loss was calculated by:

$$E_{sw,MOS}(i_d, v_{dc}) = E_{on} + E_{off} = (a * i_d + b) + \frac{v_{dc}}{v_a} E_{off@v_a} \quad (6\text{-}2)$$

where a and b are device-specific coefficients for turn-on energy, and $E_{off@v_a}$ is the turn-off energy loss at $v_{dc} = v_a$, which is obtained from device datasheet.

In Si MOSFETs and IGBTs case, Si MOSFET has both switching and conduction loss, while IGBT, as synchronous devices, has conduction loss only. The conduction loss of IGBT is dissipated either in the channel or anti-parallel diode:

$$P_{cond,IGBT} = \begin{cases} I_{rms,pos}^2 R_{ce}(T_j) + \frac{1}{T}\sum i_d v_{ce}(T_j)\Delta t_i, \ for\ i_d > 0 \\ I_{rms,neg}^2 R_d(T_j) + \frac{1}{T}\sum i_d v_f(T_j)\Delta t_d, \ for\ i_d < 0 \end{cases} \text{(W)} \quad (6\text{-}3)$$

where $I_{rms,pos}$ and $I_{rms,neg}$ are the RMS value of positive and negative current flowing through the device, $R_{ce}(T_j)$ and $R_d(T_j)$ are the temperature-dependent on-state resistance of IGBT channel and diode, $v_{ce}(T_j)$ is the temperature-dependent collect-emitter voltage during on-state of IGBT, $v_f(T_j)$ is the temperature-dependent forward voltage of diode, Δt is the time duration of each conduction period, and T is the line frequency.

In GaN HEMTs case, R_{dson} of the devices and switching loss were characterized by using curve tracer and double pulse tester (DPT). The testing results are shown in Figure 5-4 and Figure 5-6, and the models are derived by curve-fitting (5-1) and (5-3).

b) Filters Model and Design

For the power filter, the value of converter-side inductor (L_1) determines the maximum peak-to-peak current ripple ($I_{p\text{-}p,max}$):

$$i_{p-p,max} = \frac{V_{dc}}{4L_1 f_{sw}}. \quad (6\text{-}4)$$

The capacitors are designed such that corner frequency of *LC* filter is 1/10 of the switching frequency, and within the 5% reactive power requirement [40].

The design of EMI filter is separated into CM and DM part [46]. For each part, the EMI noise without using EMI filter (also known as "bare noise") is first determined in simulation. Then, the required attenuation can be derived from the difference between the bare noise and EMI standard, with 6 dB margin applied. Finally, the corner frequency (f_c) of the CM and DM filters can be calculated by:

$$f_c = f_{req} \cdot 10^{\frac{A_{req}}{40 \cdot X_f}} \quad (6\text{-}5)$$

where f_{req} is the frequency where the highest attenuation is required, A_{req} is the highest required attenuation and X_f is the order of filter. For single-stage filter, X_f is 1 and for two-stage filter, X_f is 2.

To limit the leakage current, each CM capacitor is designed to be 10 nF. DM inductance is from the leakage inductance of CM inductor. Therefore, the required CM inductance and DM capacitance can be calculated by following two equations

$$f_{CM} = \frac{1}{2\pi\sqrt{2L_{CM}C_{CM}}}, \quad (6\text{-}6)$$

and

$$f_{DM} = \frac{1}{2\pi\sqrt{L_{DM}C_{DM}}}. \quad (6\text{-}7)$$

For the inductors in both power filter and EMI filter, the losses of magnetic core and winding are calculated by GSE and Dowell's Equation, i.e., (5-10) and (5-11).

c) Thermal Model and Design

In the design, a single heatsink is used to transfer the heat generated by four devices. To maintain electrical isolation among the four devices and improve the heat transfer between devices and heatsink, thermal interface material (TIM) is inserted between heatsink and each device. The heatsink was selected to maintain junction temperatures of Si MOSFETs, Si IGBTs and GaN HEMTs at full load condition to be 125 °C, 150 °C and, 125 °C, respectively, which is 25 °C below the maximum junction temperature of the respective devices. At other loading condition, the junction temperature and devices loss are calculated iteratively based on device loss model and thermal model.

To calculate the temperature rise of the inductor, empirical equation (3-26) is used. The maximum temperature rise of the inductor is limited to 45 °C at the full load condition.

6.4 Design and Verification

a) Design Results and Comparisons

In the design, a few switching frequencies are firstly selected based on the corner frequency of EMI filters. Assuming the maximum peak-to-peak current ripple for L_1 is 20%, the calculated corner frequencies of EMI filter under different switching frequencies are shown in Figure 6-3. Higher corner frequency is desirable because it requires lower capacitance and inductance. Therefore, switching frequencies of 20 kHz, 28 kHz, and 35 kHz are selected for Si-based inverter, while 70 kHz and 140 kHz are for GaN-based counterpart.

After identifying the switching frequency candidates for Si-based and GaN-based inverters, the optimization at each frequency candidate is conducted. At each selected switching frequency, the maximum peak-to-peak current ripple in L_1 is set to three different values: 20%, 30% and 40%, which also affects the corner frequency of EMI filter. The parameters of L_1 and EMI filter are

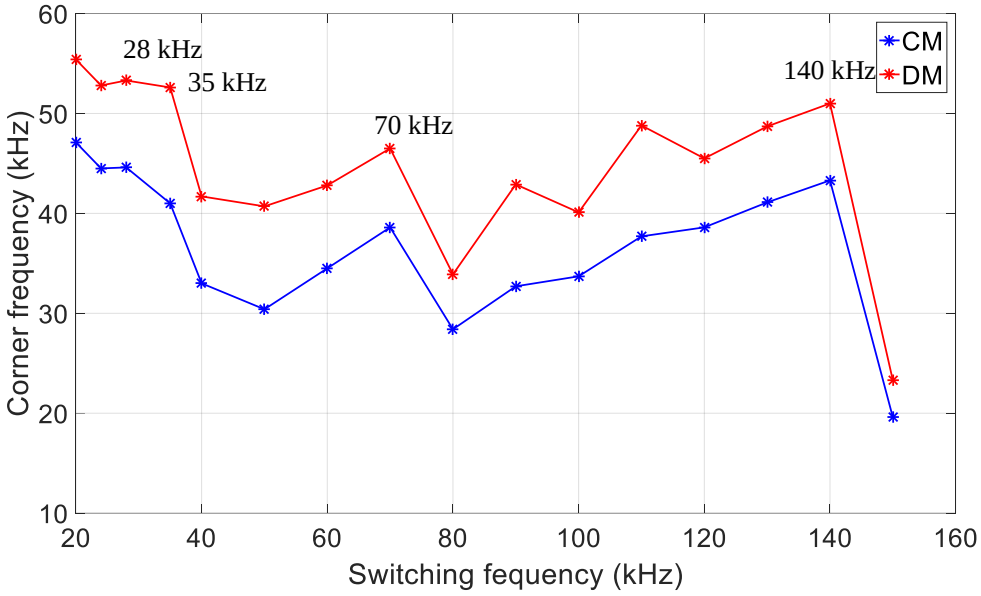


Figure 6-3. Calculated filter corner frequencies *vs* switching frequencies.

designed based on the constraints and models presented in Section IV. For Si-based design, different combinations of Si MOSFETs and Si IGBTs are swept. The losses of devices determine the required thermal resistance of the heatsink.

The design results at five different switching frequencies and three values of current ripple are summarized in Figure 6-4. The breakdown of lowest cost design at each switching frequency is shown in Figure 6-5.

The comparison for Si-based inverter using f_{sw} = 20 kHz and GaN-based counterpart using f_{sw} = 140 kHz is summarized in Table 6-6. Although the cost of switches and heatsink is higher, the overall cost of GaN-based converter using f_{sw} = 140 kHz is $19 (10%) lower than Si-based counterpart using f_{sw} = 20 kHz, mainly due to the lower cost of filters.

b) Experimental Verification

To verify the design, a 4.5 kW GaN-based prototype was built and tested using f_{sw} = 140 kHz. The prototype and the key waveforms are shown in Figure 3-20 and Figure 3-21, respectively. The efficiency of the prototype was measured and compared with the calculation results in Figure 6-6.

6.5 Summary

In this Chapter, the cost of Si-based and GaN-based single-phase inverters are designed and compared. The cost models of the main components are established based on the prices of commercial products at high quantity. After considering different switching frequencies, ripple currents, and devices combinations, optimal Si-based and GaN-based converters with switching frequencies of 20 kHz and 140 kHz are designed. It is found that the cost of filtering component in GaN-based inverter can be drastically reduced by using switching frequency of 140 kHz, which

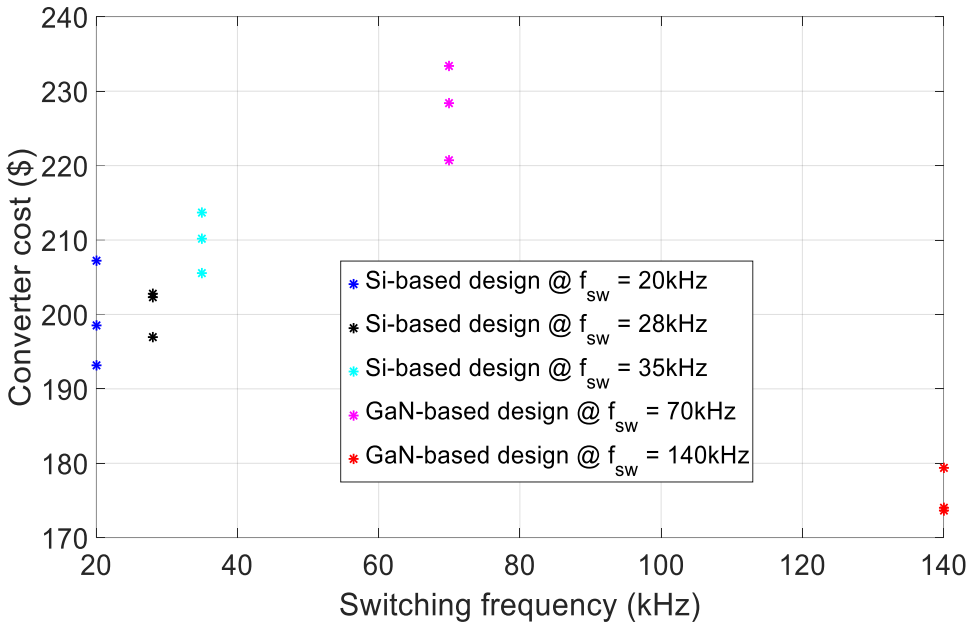


Figure 6-4. Converter cost at five switching frequencies and three current ripples (20%, 30%, and 40%).

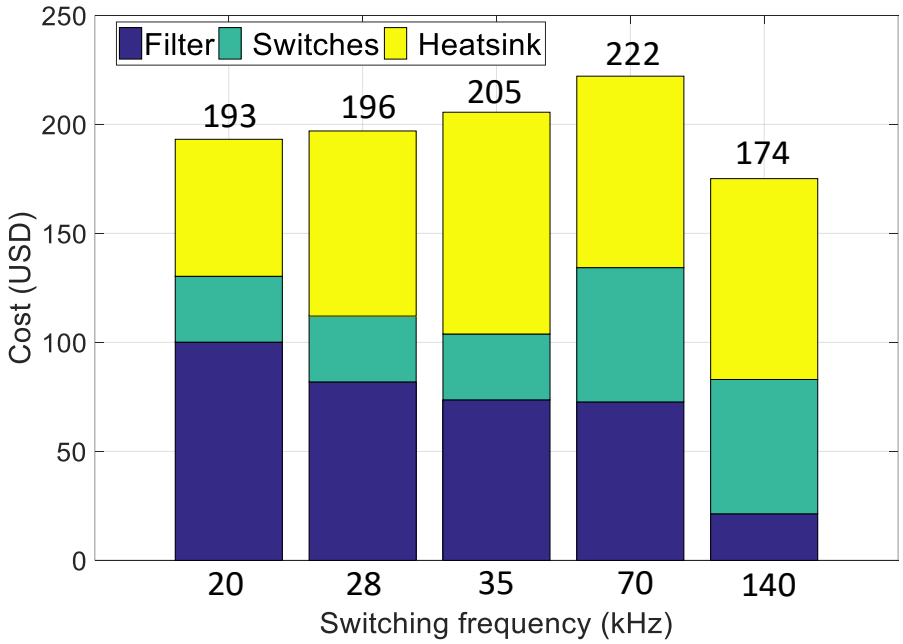


Figure 6-5 . Cost comparison between Si-based and GaN-based converters. 20 kHz, 28 kHz and 35 kHz are used for Si-based designs, and 70 kHz and 140 kHz are for GaN-based designs.

Table 6-6. List of major components for 20kHz Si-based and 140kHz GaN-based designs

	20 kHz Si-based design	**140 kHz GaN-based design**
Devices	IPW65R019C7 + FGA40T65UQDF ($12.79 each + $2.31 each)	IGOT60R070D1 ($15.04 each)
Magnetic Cores of L_1	E 100/59/27 ($8.60 each)	E 56/28/21 ($1.04 each)
Winding of L_1	10.2 m, AWG 8 ($30.2)	2.6 m, AWG 10 ($4.8)
Heatsink	R_{th} = 0.4 °C/W ($62.8 each)	R_{th} = 0.22 °C/W ($92.2 each)

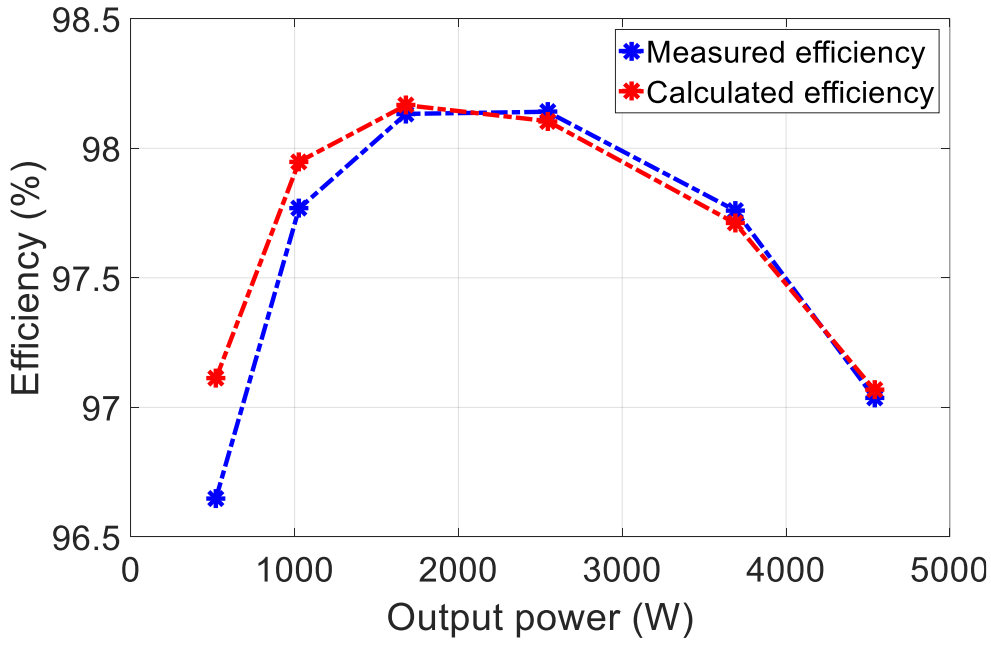


Figure 6-6. Efficiency of the prototype at V_{in} = 450V and V_o = 230 V_{rms}. CEC efficiency = 97.8% for both measurement and calculation.

is 6 times higher than optimal Si-based design. Although the costs of GaN devices and heatsinks are higher for GaN-based inverter, the overall cost can be reduced by $19 (10%) compared with Si-based counterpart. As the GaN transistors become more mature and more manufacturers of GaN devices will be available, it is anticipated that the cost advantage of GaN-based inverter will continue increasing.

Chapter 7 Evaluation of Dc Overcurrent Capability for 600 V GaN GIT

7.1 Test Setup and Procedures

The circuit used for overcurrent capability test, test circuit and the photo of test setup are shown in Figure 7-1, Figure 7-2, and Figure 7-3, respectively. The main components of the test circuit are freewheeling diode, shunt resistor for current measurement, device under test (DUT) and the protection circuit for DUT. Passive voltage probes are used to measure drain-source voltage (V_{ds}) and gate-source voltage (V_{gs}) of DUT.

Since overload condition can occur at various junction temperatures in practical applications, a range of initial junction temperature of DUT needs to be evaluated. In this test, the initial junction temperature is set to 25 ℃ to 150 ℃ using the hot plate, with step size of 25 ℃. Before each test, a hot plate heats up the device to the desirable initial junction temperature according to the setting in Table 5-2.

In the test, a single pulse is used to turn on DUT and the current in the circuit is determined by dc voltage and load resistor. The pulse is generated by the function generator, and durations were selected to be 10 ms, 20 ms, 100 ms, 1 s and 3 s [29]. For each pulse duration, the test starts with relatively low dc voltage and current. Drain current is slowly increased by adjusting the dc voltage, until the maximum withstand current is reached. The dc current in the last successful test is recorded as the maximum overcurrent capability of the DUT.

There are two objectives for the protection circuit of DUT: 1) it allows DUT to operate close to the limit, and 2) it protects DUT from degradation or failure. In the next section, the test results show that the limit of DUT is reached right after saturation occurs. Therefore, desat

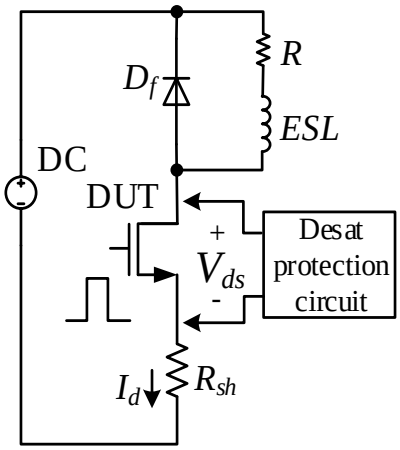
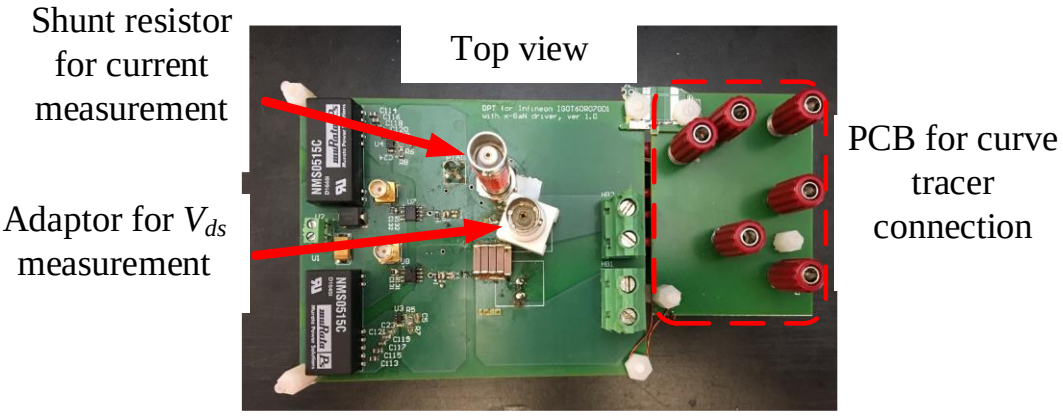
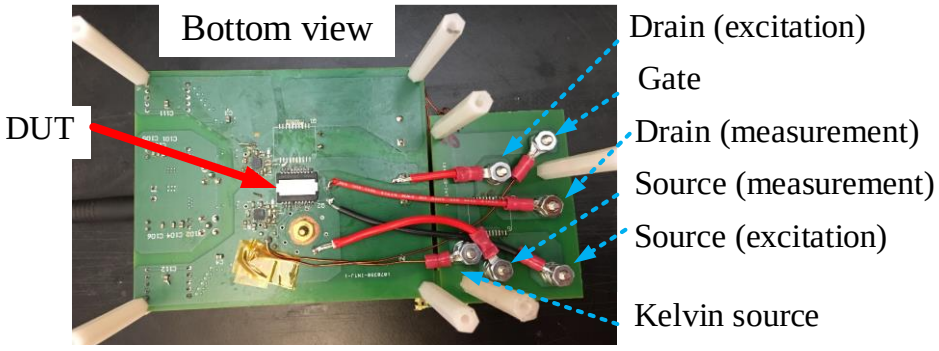


Figure 7-1. Overcurrent capability test circuit.



(a)



(b)

Figure 7-2. Test circuit for GIT overcurrent capability evaluation: (a) top view, (b) bottom view.

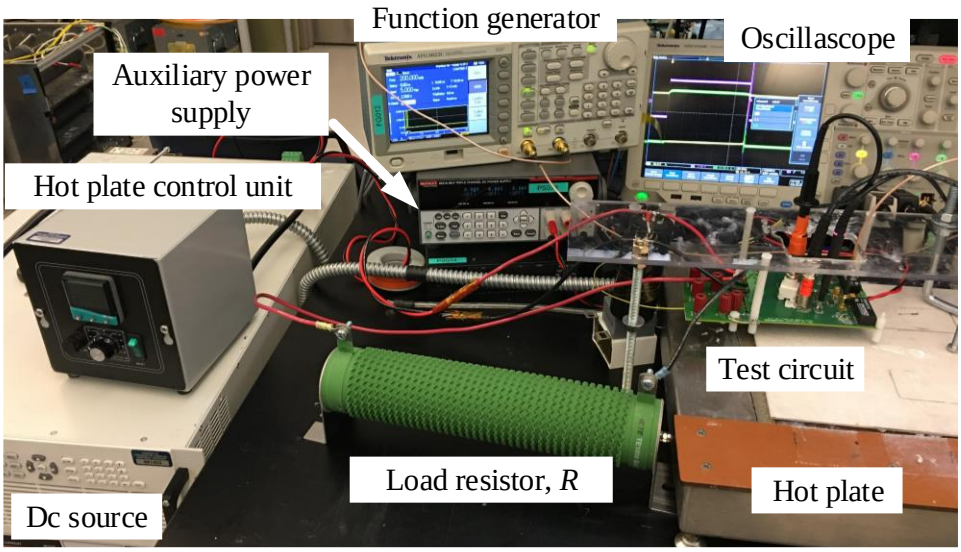


Figure 7-3. Setup for overcurrent capability test. A small copper block is located between surface of hot plate and case of the DUT for heat transfer, as shown in Figure 5-1 and Table 5-2.

protection with high v_{ds} triggering threshold is used ($V_{ds,th}$ = 10V). This setting can turn off the device at the onset of the saturation while protecting the device from failure.

Another procedure in the test is to examine the possible degradation of the devices, since each test causes thermal stress to the devices. In this study, curve tracer is used to measure the static characteristics of DUT before and after each overcurrent test. The static characterization includes output characteristic (I_d - V_{ds}), transfer characteristics (I_d - V_{gs}), and leakage current. For this purpose, another PCB is connected to the terminals of DUT. This facilitates the static characterization of DUT using curve tracer, because DUT does not have to be de-soldered before static characterization. The connection between test circuit and curve tracer is shown in Figure 7-4. It should be noted that the static characterization results using this setup include the characteristics of both DUT and the test setup. Due to relatively high current in the static characterization, Kelvin connection was used for the source and drain terminals of DUT, in order to improve the accuracy of measurement. Therefore, one connector is used for excitation, while the other is for measurement. For gate and kelvin source terminals, current is relatively small in the static characterization, and one connector can be used for both excitation and measurement.

7.2 Experimental Results

First, to verify that the limit of device is reached once saturation occurs, high-current test is performed without using desat protection. The duration of turn-on pulse generated by function generator is 10 ms. As shown in Figure 7-5, DUT conducts drain current of 45 A until it saturates at 9.9 ms. After the saturation, gate oscillation occurs and drain current of DUT drops to zero. It takes less than 10 μs from v_{ds} reaching 10 V to the onset of gate oscillation. This time period is much shorter than the intended pulse durations in the test (10 ms ~ 3 s). Therefore, setting desat

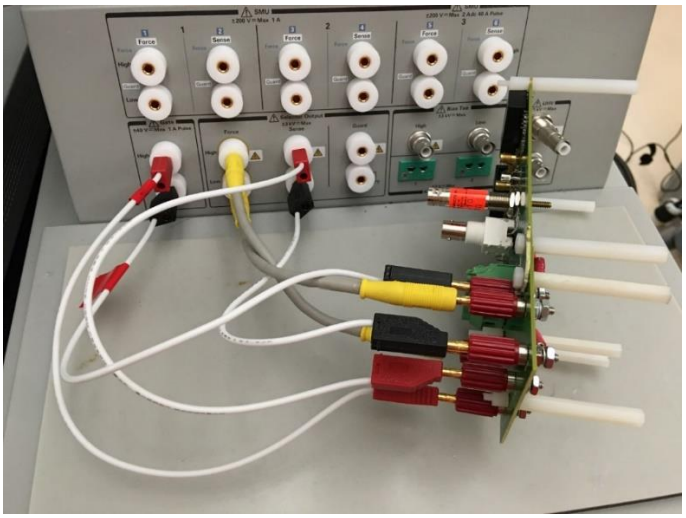
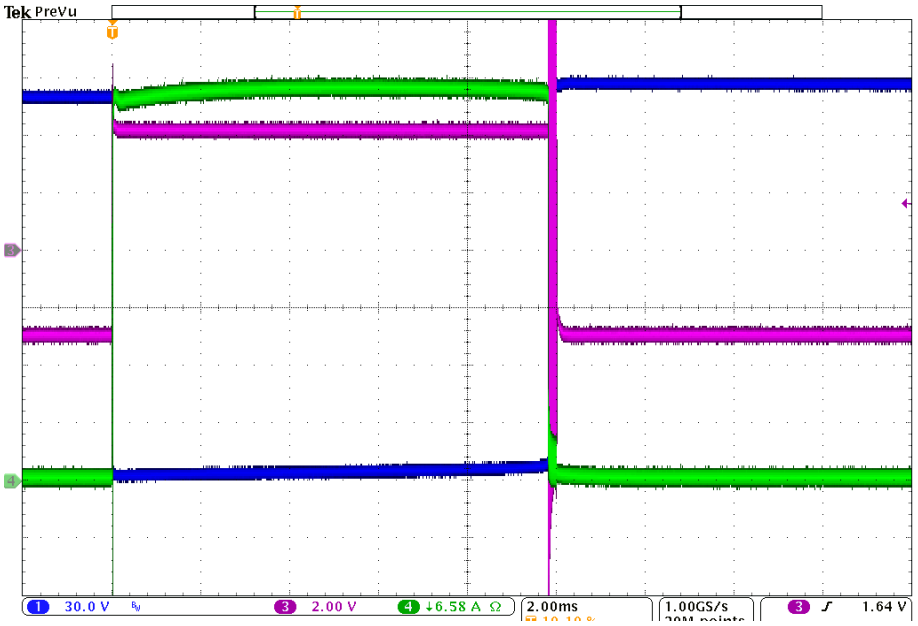
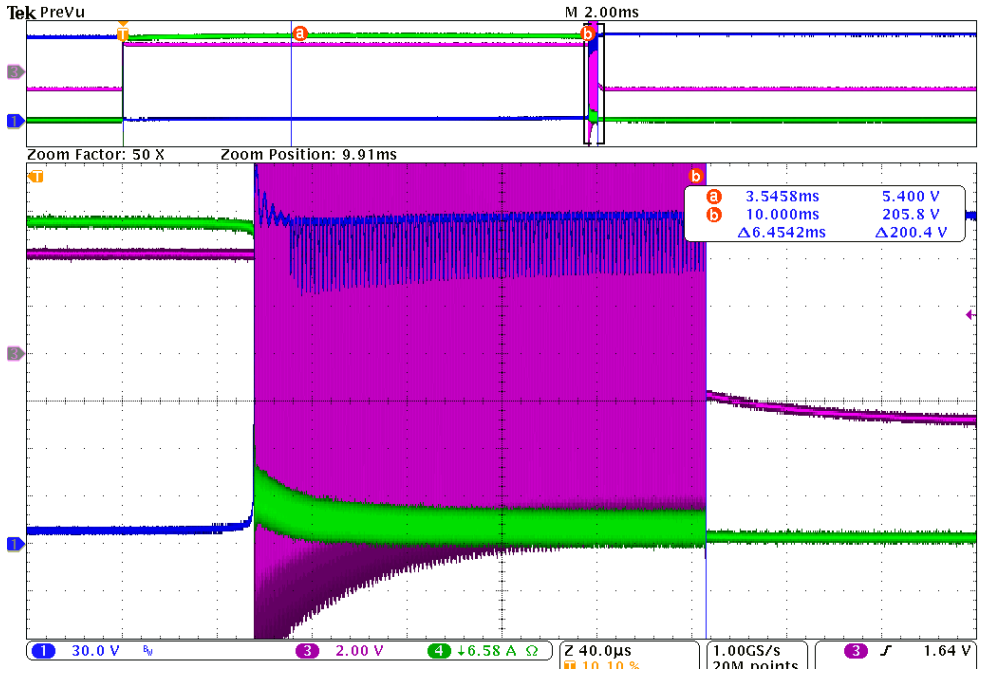


Figure 7-4. Connection between test circuit and curve tracer for static characterization of DUT.



(a)

Figure 7-5. Waveforms of DUT conducting 42 A drain current without using desat protection, (a) 2 ms/div; (b) zoomed-in view, 40 µs/div; (c) further zoomed-in view, 200 ns/div. Blue: drain-source voltage of DUT (30V/div), magenta: gate-source voltage of DUT (2V/div), and green: drain current of DUT (6.58A/div).



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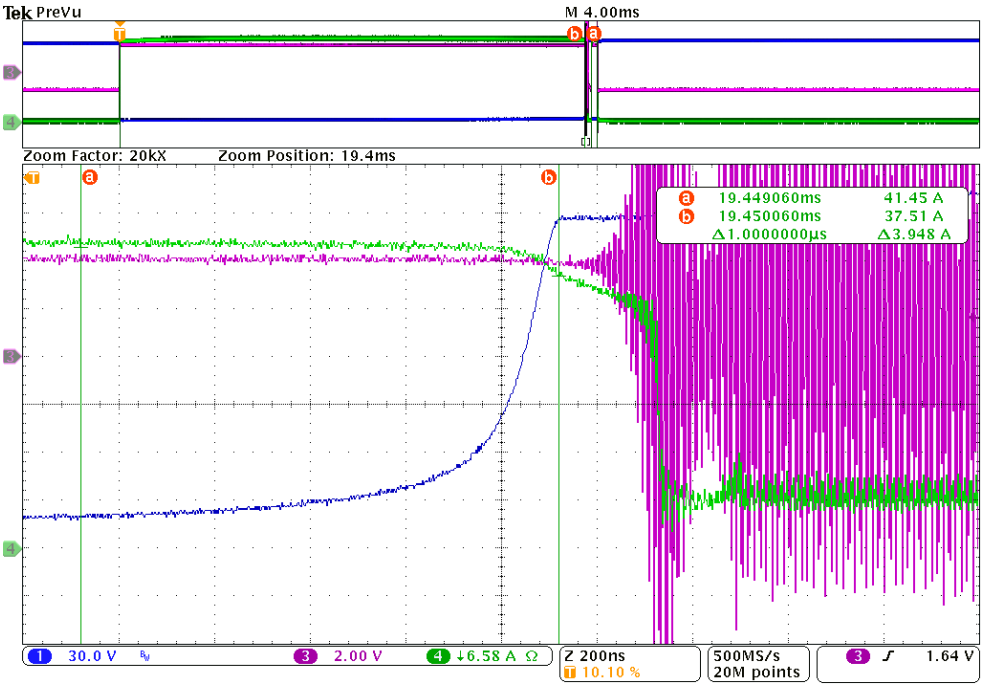

(c)

Figure 7-5 continued.

protection with relatively high threshold voltage, such as 10 V, has minimal impact on the test results of overcurrent capability, while it can also prevent the gate oscillation and potential failure of device which occurs after device saturation. In the following test, desat protection is used, and the protection threshold is set to v_{ds} = 10 V.

The tests are conducted for five different pulse durations, and the junction temperature before test ranges from 25 °C to 150 °C. The output characteristic, transfer characteristic, and leakage current of DUT before and after overcurrent capability are shown in Figure 7-6, Figure 7-7, and Figure 7-8, respectively. Consistent static characterization results before and after the test confirm that there is no degradation caused.

The highest currents that do not trigger desat protection are plotted in Figure 7-9, and the energy dissipated in the devices are summarized in Figure 7-10. The energy is calculated by

$$E = \int i_d(t)\, V_{ds}(t) dt, \tag{7-1}$$

It can be observed that under the same pulse duration, the maximum withstand current of DUT depends on the T_{j0}, but energy is almost the same under different T_{j0}. This indicates that overcurrent capability of DUT can be limited by the local hotspot at temperature much higher than 150 °C [119, 120].

For converter and SSCB applications, if high precision measurements of drain-source voltage and drain current are both available, the energy of the devices can be calculated, and protection can be implemented based on the maximum withstand energy of devices. In case drain-source voltage is not available, overcurrent capability needs to be determined based on drain current. The overcurrent capability in terms of It and I^2t integral can be calculated based on the measured current:

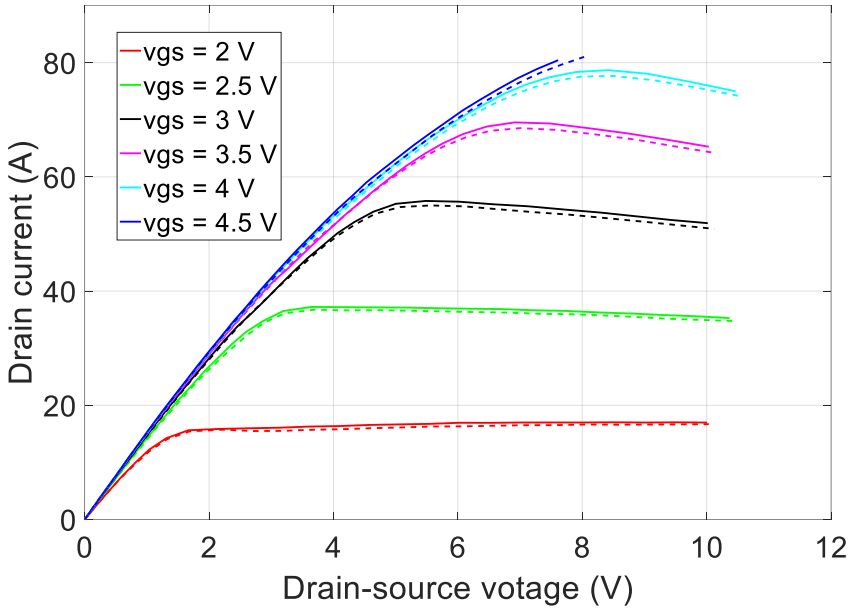

Figure 7-6. Output characteristic (i_d - v_{ds}) of DUT before and after the overcurrent capability test.

Solid lines: before test, dashed lines: after test.

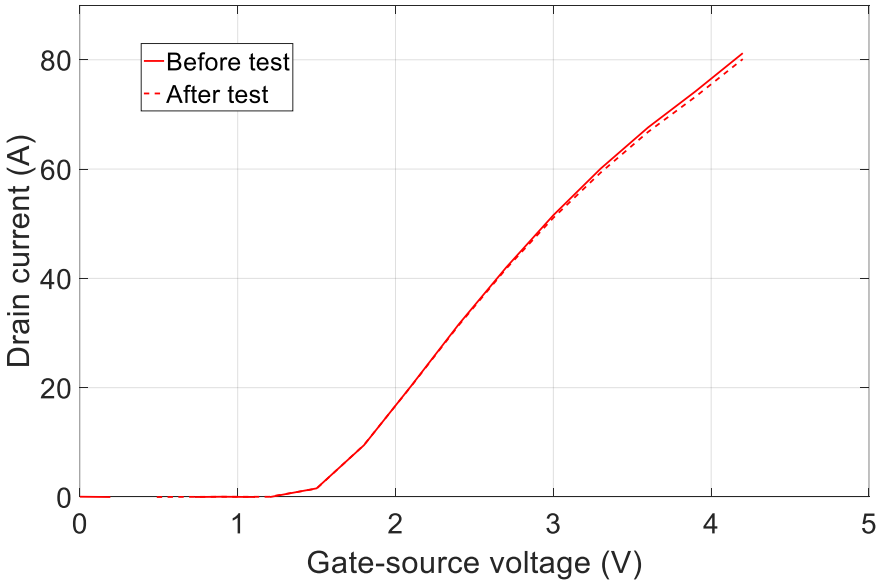

Figure 7-7. Transfer characteristic (i_d – v_{gs}) of DUT before and after the overcurrent capability test. Solid lines: before test, dashed lines: after test.

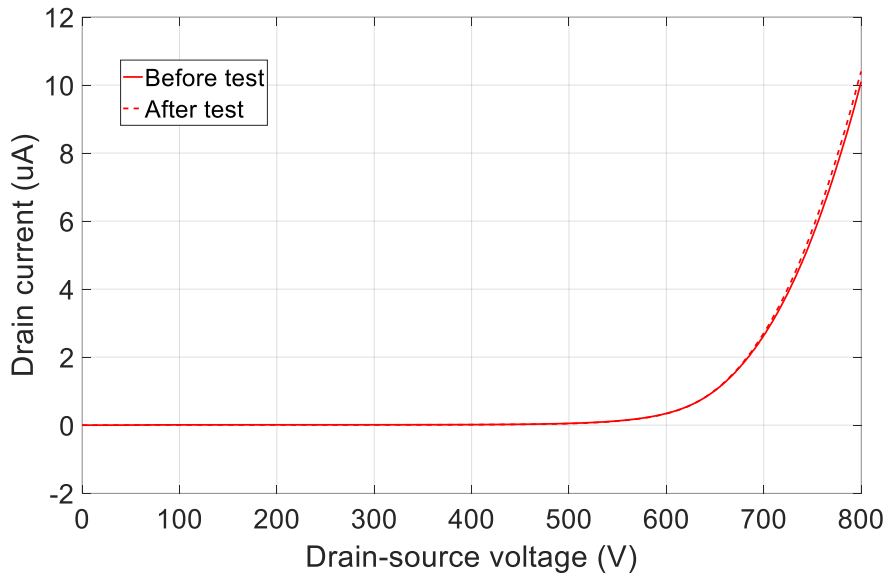

Figure 7-8. Leakage current of DUT before and after the overcurrent capability test. Solid lines: before test, dashed lines: after test.

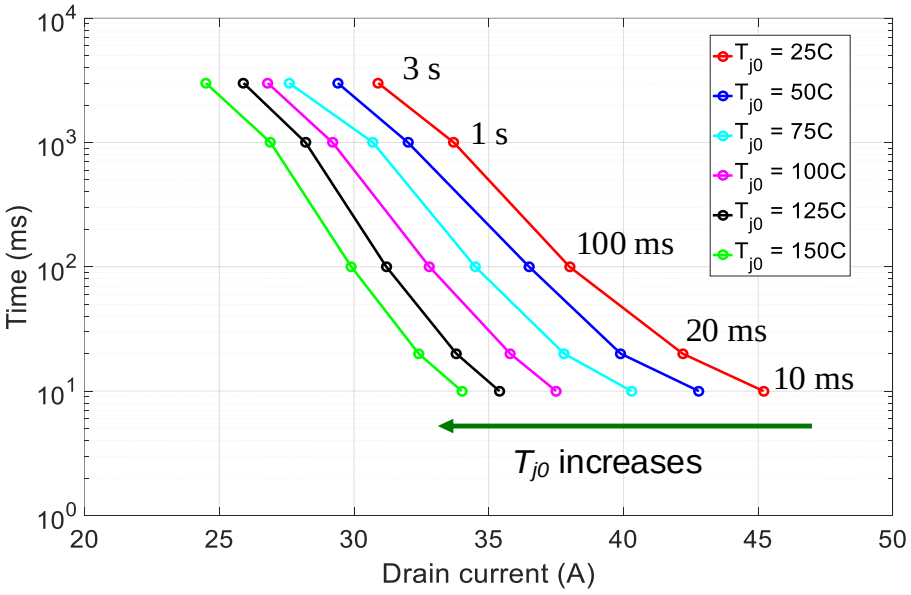

Figure 7-9. Maximum withstand current of DUT at different initial junction temperatures and pulse durations.

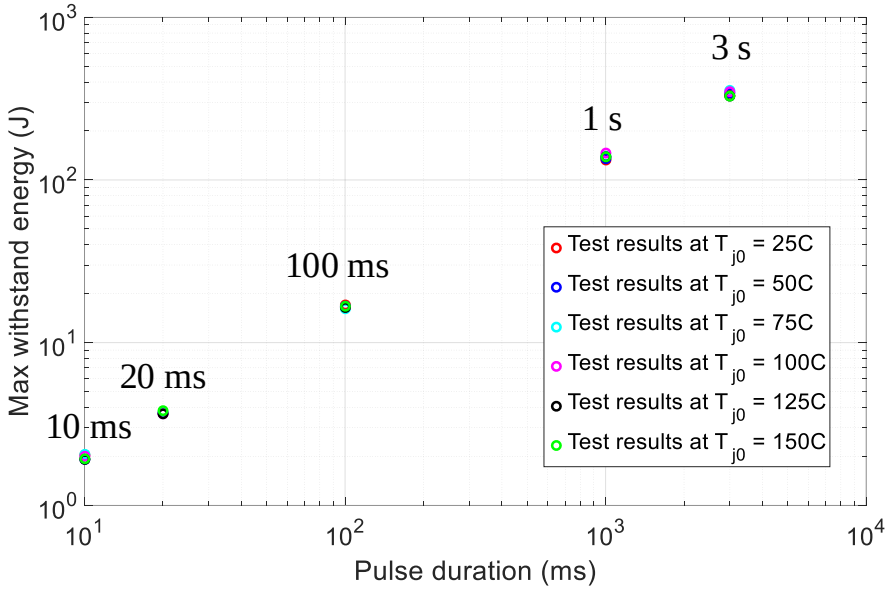

Figure 7-10. Maximum withstand energy of DUT at different initial junction temperatures and pulse durations.

$$i * t = \int i_d(t)\, dt, \tag{7-2}$$

and

$$i^2 t = \int i_d(t)^2\, dt. \tag{7-3}$$

The measured results are shown in Figure 7-11 and Figure 7-12.

7.3 Comparison with Calculated Overcurrent Capability

One alternative way to obtain the overcurrent capability of transistor is to use the transient thermal impedance and maximum allowable junction temperature. The power loss can be calculated by (5-1), and the junction temperature by (5-21) to (5-24) with parameters in Table 5-5. Since the time duration is relatively short, the case temperature is assumed to be unchanged. The maximum allowable junction temperature ($T_{j,max}$) is set to 150 ºC. One example is shown in Figure 7-13. The junction temperature reaches 150 ºC at 100 ms as the drain current is 33.2 A. The overcurrent capability at other case temperature and time duration can be calculated in the same way.

The calculation results and the experimental results at 25 ºC and 100 ºC case temperature are summarized in Figure 7-14 and Figure 7-15. There are a few observations:

1. Calculated overcurrent capability by assuming $T_{j,max}$ = 150 ºC underestimates the real capability of the devices, especially at higher initial junction temperature. In fact, for T_{j0} = 150 ºC, the calculated overcurrent capability is zero, while this contradicts with the test results. This again indicates that the overcurrent capability of the device is limited by high temperature local hotspot.
2. The calculated overcurrent capability for 1 s and 3 s is identical, because the device reaches thermal steady state at 1 s (see Figure 5-15).

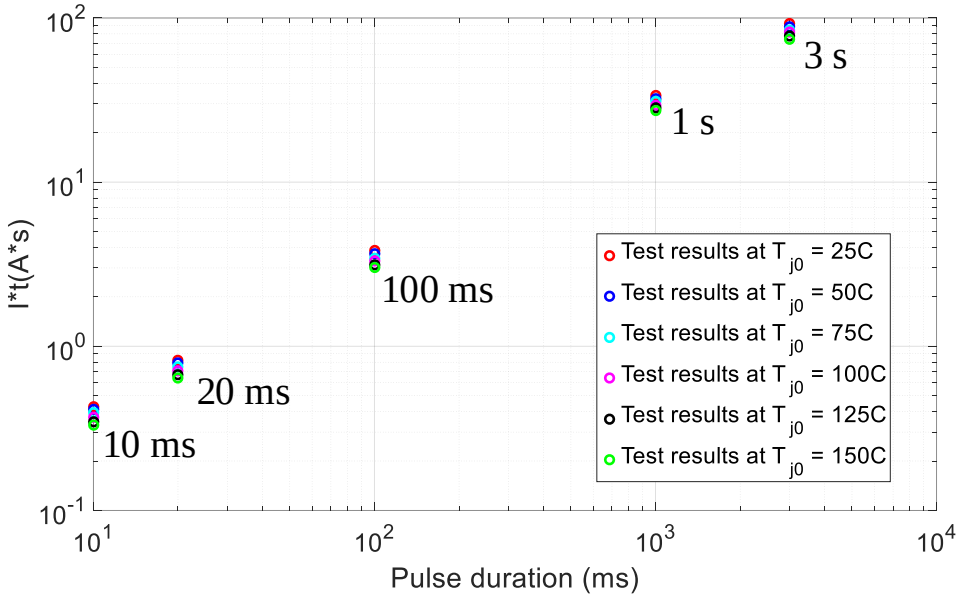

Figure 7-11. Current-time integral (*It*) curve of DUT at different initial junction temperatures and pulse durations.

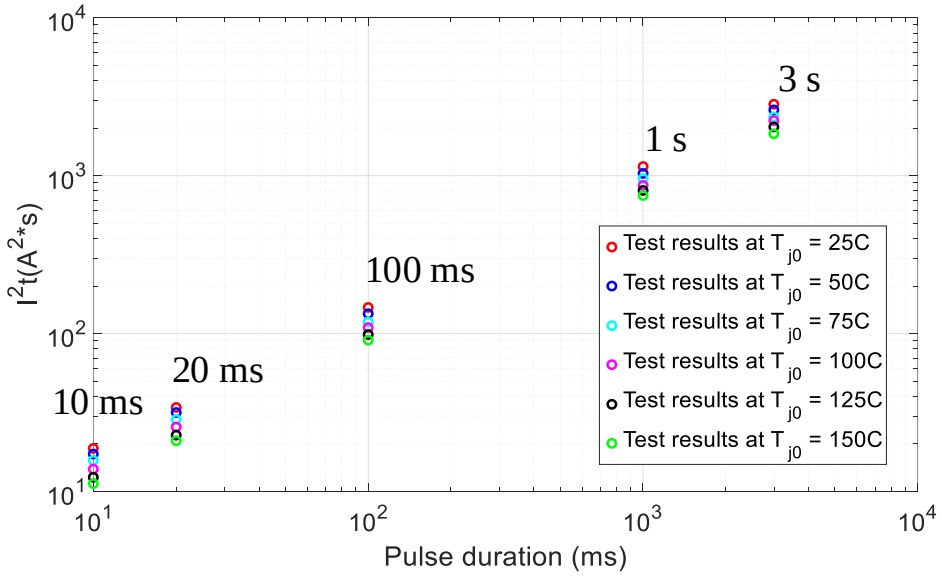

Figure 7-12. Current-square-time integral (I^2t) curve of DUT at different initial junction temperatures and pulse durations.

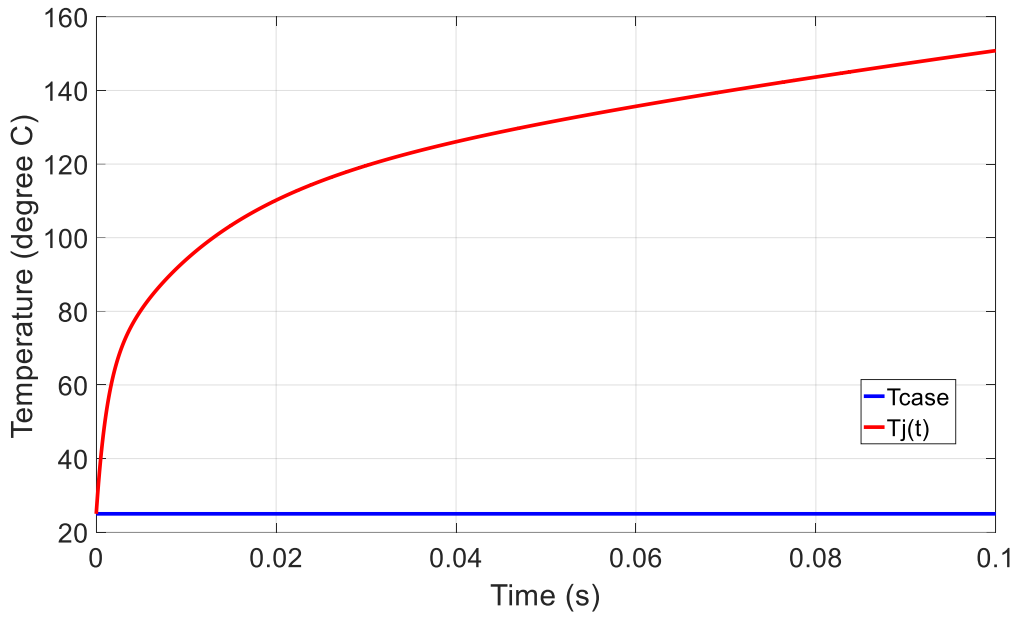

Figure 7-13. Calculated junction temperature of the GaN transistor for I_d = 33.2 A, time duration 100 ms, and T_{j0} = 25 ºC.

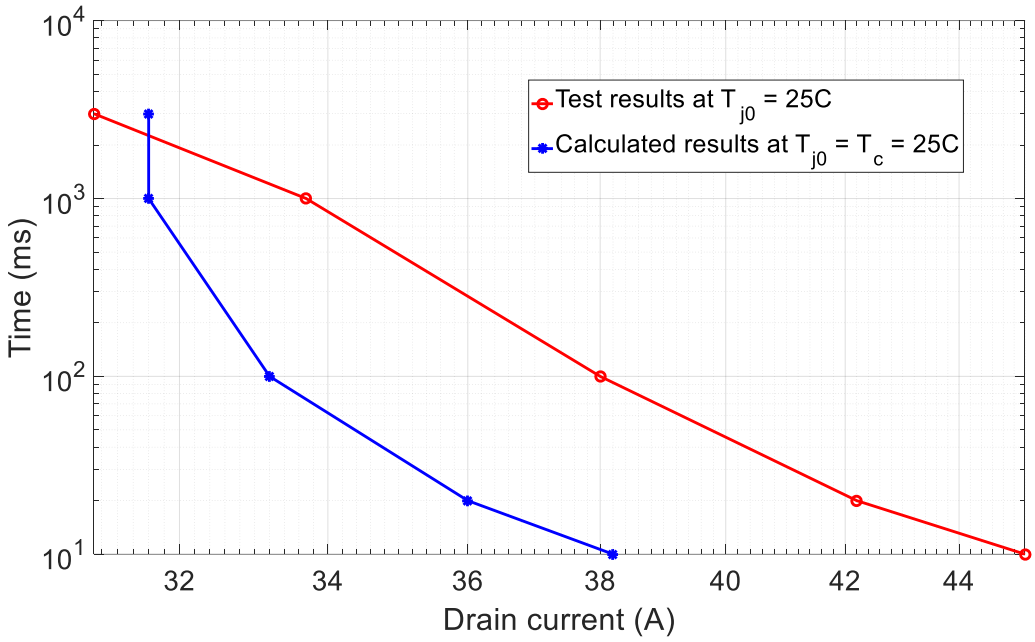

Figure 7-14. Calculated and test results of the GaN transistor at T_{j0} = 25 ºC.

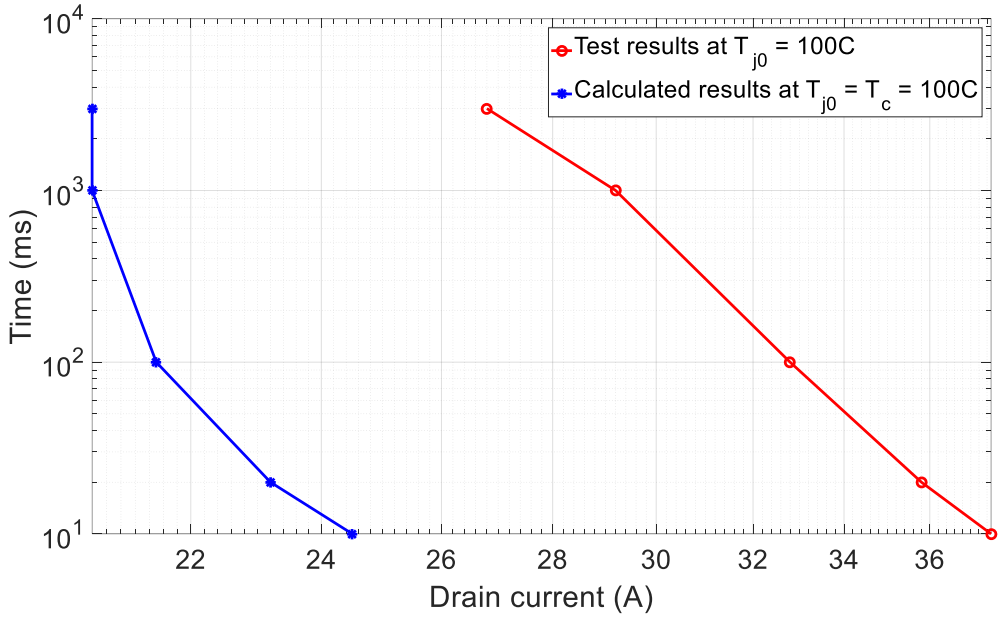

Figure 7-15. Calculated and test results of the GaN transistor at T_{j0} = 100 ºC.

3. At T_{j0} = 25 ºC and time duration = 3 s, the calculated overcurrent capability is higher than the test result. This is because the case temperature has changed as time duration increases. The assumption that case temperature is constant leads to more error in such case.

7.4 Application to SSCB

A GaN-based SSCB prototype was built with consideration of the overcurrent capability of the devices. The design specifications shown in Figure 7-1 are derived based on the device capability and data center application.

The schematic of bidirectional SSCB and a picture of the prototype are shown in Figure 7-16 and Figure 7-17, respectively. To ensure bidirectional voltage blocking, it consists of two GaN GIT devices in series with drain terminals connected. Each device is driven by one isolated gate signal across Gate (G) and Kelvin Source (KS) terminals.

There are three operation and protection scenarios: normal operation, overload condition and short circuit condition. For normal operation, the current of the SSCB is equal to or below the nominal current of 8 A. SSCB is expected to conduct the current during normal operation. For overload condition, the SSCB conducts current between 8 and 32 A for certain period of time. If the overload condition sustains and goes beyond the overload setting, SSCB will be shut down. The overload setting is adjustable, and the upper boundary of the setting is limited by the overcurrent capability of the devices. In the short circuit condition, the SSCB current increases to above 32 A drastically within very short period of time, depending on the dc voltage and inductance in the system.

Table 7-1. Design target of the GaN-based SSCB

Dc voltage	400 V
Nominal current	8 A
Overload current	8 – 32A, durations depend on current level
CEC Efficiency	> 99.6 % (loss < 13 W)
Cooling method	Natural convection
Size	< 300 cm^3

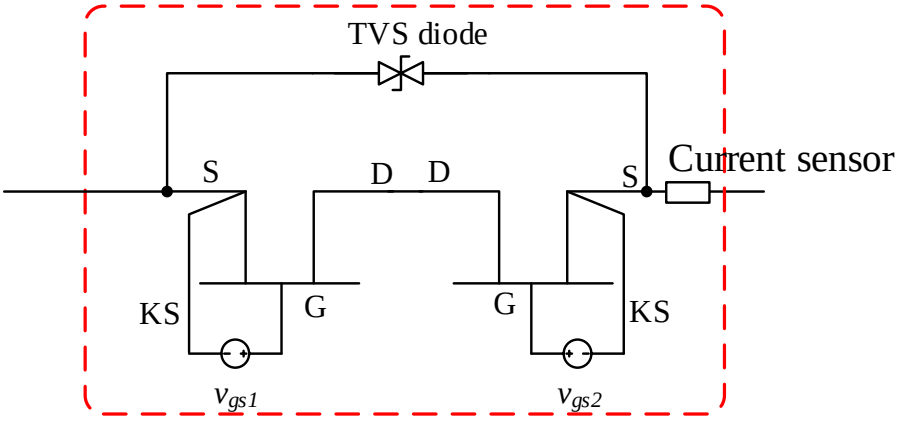

Figure 7-16. Schematic of the GaN-based bidirectional SSCB. D: Drain terminals; S: Source terminals; G: Gate terminals; and KS: Kelvin Source terminals



Figure 7-17. A GaN-based SSCB prototype with 8 A nominal current and 8 – 32 A overload capability.

Three protection schemes were developed for the prototype, which are summarized in Table 7-2.

The DSP-based overload protection aims to react if sustained overload condition occurs. This protection can have adjustable time delay and react when the duration of overcurrent is higher than the pre-set time duration. The maximum possible time delay under different overloads is constrained by the overcurrent capability of the switches. Once this protection is triggered, DSP sends turn-off signal to the switches. In this work, *i*t* integral was used to present the overcurrent capability of switches. DSP constantly calculates the *i*t* integral for SSCB and compares to the *i*t* capability of switches during the overload condition.

In this work, the curve-fitting of *i*t* integral was derived for the selected GaN devices, based on the measured results in Figure 7-11. The maximum *i*t* integral for the device is:

$$it_{max} = (0.95\log_{10}(t) - 1.43), \tag{7-4}$$

where *t* is the time duration of overload, between 10 ms to 3 s.

Theoretically, (7-4) can be the threshold for turning off the SSCB. To ensure the safe operation of SSCB, 30% margin was added. Thus, the threshold for turning off becomes:

$$it_{th} = 0.7 * (0.95\log_{10}(t) - 1.43), \tag{7-5}$$

The schematic and setup of the test circuit are shown in Figure 7-18 and Figure 7-19, respectively. Before overload condition occurs, auxiliary switch is off and the current only goes though R_{L1}. Overload condition is generated by turning on auxiliary switch, and the load resistance becomes R_{L1} in parallel with R_{L2}.

Exemplary waveforms for overload test are shown in Figure 7-20. The prototype operates

Table 7-2. Protection schemes and current range

Protection Schemes	Current Range
DSP-based overload protection	8 – 32A
Comparator-based instantaneous protection	> 32A
Desat protection	All current range

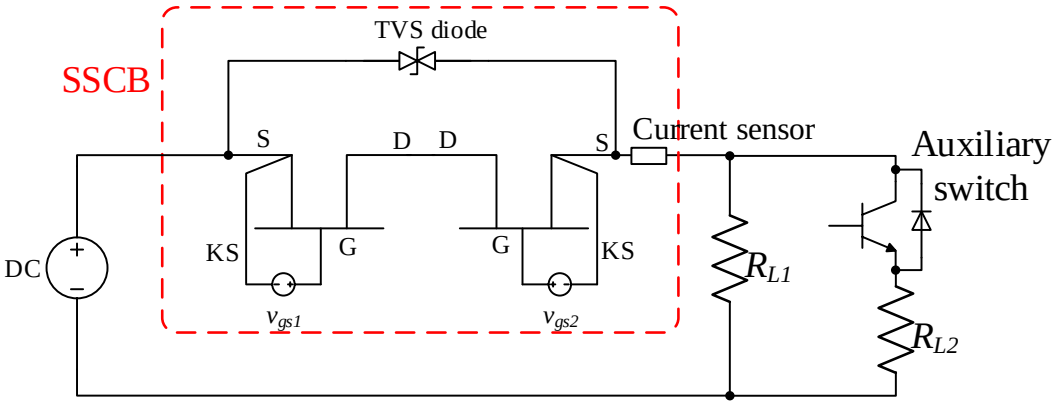

Figure 7-18. Schematic for overload test of the GaN-based SSCB.

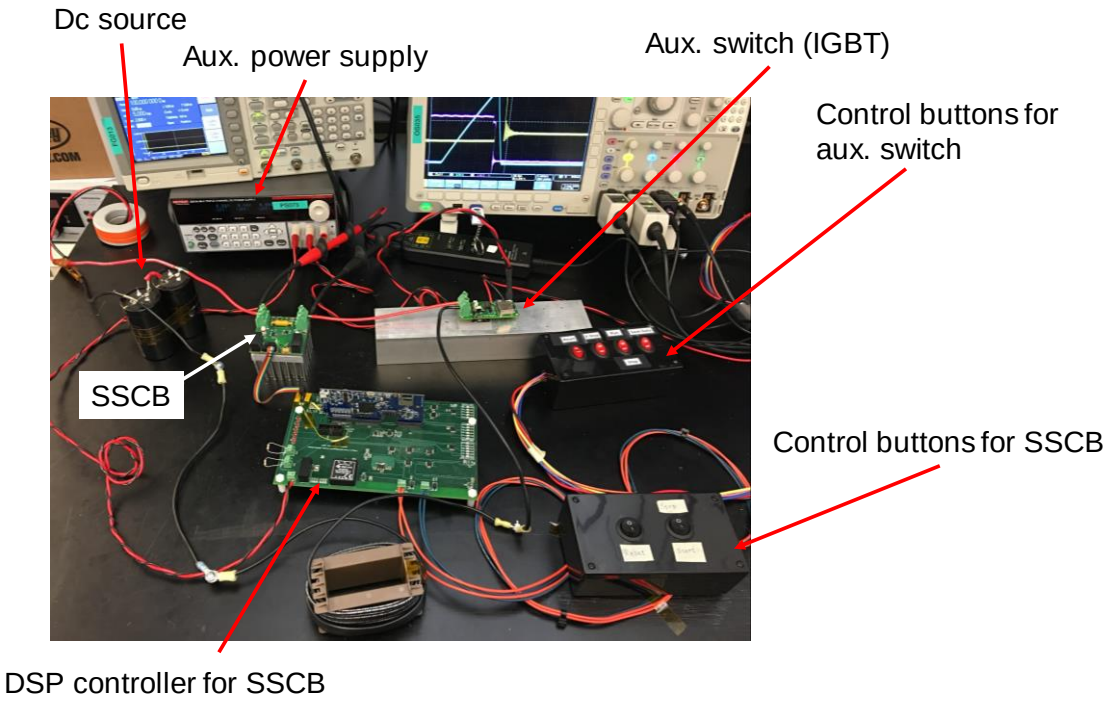

Figure 7-19. Setup for overload test of the GaN-based SSCB.

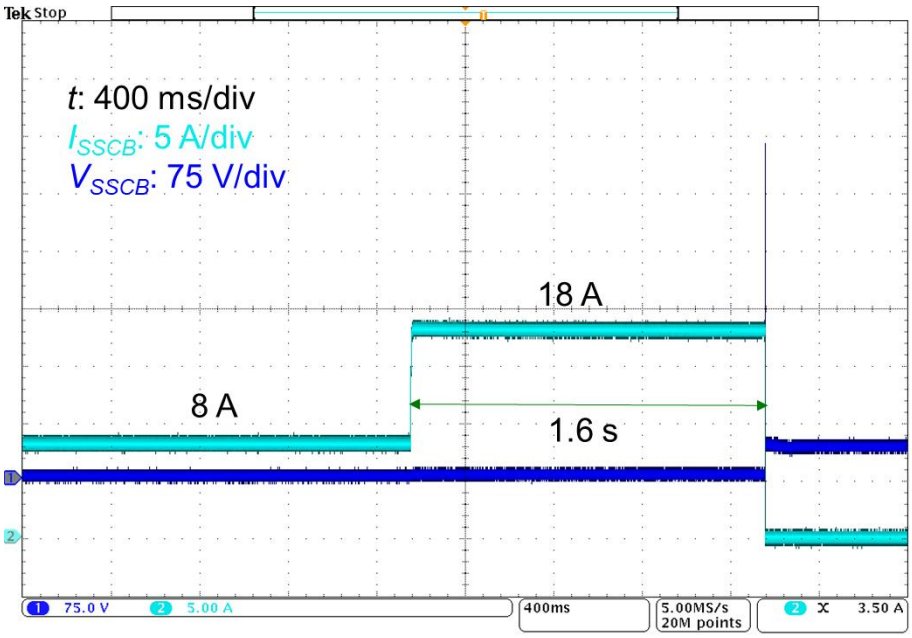

Figure 7-20. Waveforms in overload test (18A, 1.6s) of the GaN-based SSCB.

at nominal current, and then current increases to 18 A. The SSCB is tripped after the overcurrent sustains for 1.6 s which reaches the threshold given by (7-5). Nine overload conditions with current level between 17A and 25A were tested, and the results are summarized in Figure 7-21.

7.5 Summary

In this chapter, the test setup and procedures are developed for the overcurrent capability of a 600 V GaN HEMT. The test ensures the device limited can be reached without destroying or degrading the devices. The time-current curve, maximum withstand energy, *it* integral and i^2t integral are derived based on the measured results. Comparing with the calculated results, the measurement can reveal the true capability since the devices can withstand more than 150 °C junction temperature for short period of time. Finally, the overcurrent capability results are implemented and demonstrated in a GaN-based SSCB.

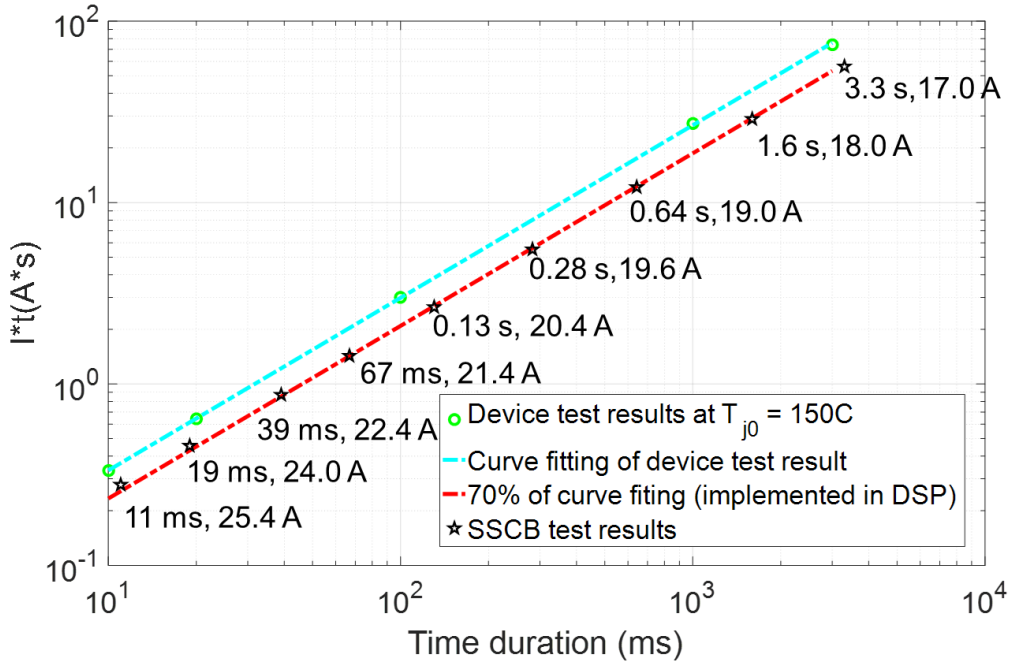

Figure 7-21. Test setting and results for nine different overload conditions of the GaN-based SSCB.

Chapter 8 Conclusions and Future Work

8.1 Conclusions

This dissertation presents the filter design, loss model, cost of the GaN-based PV inverter, and dc overcurrent capability of GaN devices. The main conclusions and contributions are as follows.

- A method to design an air-gapped inductor with consideration of fringing effect is proposed. The method uses bottom-to-top approach to evaluate the possible combinations of turn number and airgap length. This approach can easily incorporate various fringing effect models without iteration. Also, it ensures the optimal design is obtained.
- The design and optimization of ac-side filter using both coupled and non-coupled inductors are developed. The relationship between the ratio of inductors and filter performance, including loss, weight, and EMI attenuation, is established. A design example is demonstrated in a 4.5 kW GaN-based inverter by using the optimal ratio between coupled and non-coupled inductors.
- An accurate and efficient design procedure is proposed to design high-density multi-stage EMI filter for a single-phase inverter. The procedure considers self-parasitic and inductive coupling and identifies the critical coupling that dominates the filter performance. This provides specific guidelines for the designers to tackle certain coupling and improve the filter performance.
- The impacts of some often-neglected factors in the loss model of GaN-based inverter are quantified. The important factors at light load and heavy load conditions are identified. In

addition, a simple yet accurate method to calculate the time-varying power loss and junction temperature of the switches is developed.

- The cost breakdown of GaN-based and Si-based inverters are studied and compared. By using high-speed GaN devices and 6 times higher switching frequency, the cost of the filter can be significantly reduced. This leads to lower overall cost for GaN-based inverter, although the cost of GaN devices is higher than Si devices.
- The dc overcurrent capability of GaN GIT is experimentally evaluated. The test setup is developed to ensure the device limit is reached without degrading or destroying the devices. The test shows the overcurrent capability of GaN devices at various junction temperature and time durations. The results are also applied to the design of a GaN-based dc SSCB.

8.2 Future Work

1) Design automation of power converter with detailed power loss and filter design

In this dissertation, several design considerations regarding power loss and filter design of the GaN-based converter are discussed. Some often-neglected factors in the power loss calculation are found to be important in GaN-based inverter. Also, the self-parasitic and coupling between components can significantly affect the performance of filter. These aspects need to be taken into consideration in the design process of the power converter.

Other design considerations such as thermal management and device selection are also essential to the design of power converters. These considerations are strongly coupled with each other, and the design space can be large considering a large number of design variables. This usually leads to a time-consuming iterative design process. To solve this problem, a design automation tool considering each aspect of the power converter has been proposed [121]. The

accuracy of design automation tool can be further improved by incorporating detailed power loss and filter design, especially for a GaN-based power converter.

2) Overcurrent capability of GaN device for power converter application

Dc overcurrent capability of GaN devices has been covered in this research work. Such characteristics can be useful for design of a dc SSCB. However, overcurrent can also occur in a power converter due to overload or fault. In some cases, the other unfaulty converter is required to ride through short-term overcurrent or remain connected for certain time duration given that the protection strategy will react and isolated the fault locations. Therefore, it is also necessary to understand the overcurrent capability of the devices under pulsating current with constant or varying widths.

In addition, overcurrent conditions can occur more frequently in some applications which have more stringent requirement for overload. This requires more study on the long-term reliability of GaN devices under overcurrent stress.

8.3 Publication List

Journal Paper

- **Z. Yang**, P. Williford, E. A. Jones, J. Chen, F. Wang, S. Bala and J. Xu, "Factors and Considerations for Modeling Loss of a GaN-based Inverter," in *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 3042-3052, March 2021.

Conference Papers

- **Z. Yang**, P. Williford, F. Wang, U. Raheja, J. Xu, X. Song and P. Cairoli, "Overcurrent Capability Evaluation of 600 V GaN GITs under Various Time Durations," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 376-381

- **Z. Yang**, P. Williford, F. Wang, S. Bala and J. Xu, "Design and Optimization of Ac-side Filter using Coupled Inductor for Single-phase Full-bridge Inverter," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 5386-5392.

- **Z. Yang**, J. Chen, P. Williford and F. Wang, "Cost Comparison Between GaN-based and Si-based 4.5-kW Single-phase Inverters," *2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2020, pp. 1-6.

- **Z. Yang**, P. Williford, E. A. Jones, J. Chen, S. Bala and J. Xu, "Resolving Loss Discrepancy between Calculation and Measurement in a 4.5 kW GaN-based Inverter," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 4409-4414.

- **Z. Yang**, H. Suryanarayana and F. Wang, "An Improved Design Method for Gapped Inductors Considering Fringing Effect," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 1250-1256

- P. Williford, E. A. Jones, **Z. Yang**, J. Chen, S. Bala and J. Xu, Optimal Dead-time Setting and Loss Analysis for GaN-based Voltage Source Converter," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 898-905.

- E. A. Jones, P. Williford, **Z. Yang**, J. Chen, S. Bala, J. Xu and J. Puukko, "Maximizing the voltage and current capability of GaN FETs in a hard-switching converter," *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, 2017, pp. 740-747.

- R. Chen, **Z. Yang** and F. Wang, "Overcurrent and Short-circuit Capability Experimental Investigation for GaN HEMT at Cryogenic Temperature," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 382-388.

- Z. Gao, P. Yao, H. Li, S. Ji, **Z. Yang**, F. Wang and Y. Ma, "A Transformer Flux Balancing Scheme Based on Magnetizing Current Harmonic in Dual-Active-Bridge Converters," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 1894-1899.

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