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I am submitting herewith a thesis written by Jeffrey Edward Eagen entitled "Design of a Micro-power Control System for the RSVP Program." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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Design of a Micro-power Control System for the RSVP Program

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Jeffrey Edward Eagen
December 1999

Dedication

This thesis is dedicated to my beautiful fiancé

Kari Michelle Karwedsky

for her support, friendship, and most of all her beautiful smile.

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Most of all, thanks to God, my family, and the love of my life, Kari.

Abstract

A micro-power control system has been developed for the RSVP program. RSVP is an acronym for Removal of Ship's personnel by Virtual Presence Program that involves replacing personnel by data-acquisition modules. Consisting of two ASICs and a re-configurable test board, the control system provides a regulated 3.3-volt supply as well as provides an optional 9-volt supply. It is capable of monitoring three input sources of scavenged power, then converting that power via a Buck converter into a useful regulator supply. In the case when no scavenge-able power is available, an on-board battery provides the regulator supply. In this first generation design, the digital control logic is implemented via a programmable logic device. The logic controls the monitoring of the input sources, operation of the converter, and control of the regulator. An off-chip clock oscillator provides a 32.786 kHz clocking frequency. Unique compared to most Buck converter systems is the control system. A system of comparators and digital logic maintain converter operation via a fixed duty cycle clock.

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Abbreviations

ASIC	Application Specific Integrated Circuit
HP	Hewlett Packard
RSVP	Removal of Ship's Personal by Virtual Presence Program
IC	Integrated Circuit
PLD	Programmable Logic Device
LED	Light Emitting Diode

1.0 Introduction

1.1 What is RSVP?

RSVP is an acronym for Removal of Ship's personnel by Virtual Presence Program. The main element of RSVP is the creation of a wireless sensor cluster in a small package which can be mounted anywhere in a Naval vessel's hull. The sensor cluster will monitor such environmental items as humidity, temperature, fire and flooding. Each sensor cluster will then transmit wirelessly to a central control unit in the room, which then transmits data through wire-line to a ship's control room. From this control room, information on whether or not there is an environmental hazard such as a fire or flooding can be obtained. Each sensor cluster package will provide its own power, scavenging it from the environment and an in-package primary battery.

1.1.1 General Information

RSVP is a cooperative effort between Charles Stark Draper Laboratory of Massachusetts Institute of Technology and the Monolithic Systems Development group at the Oak Ridge National Laboratory, Tennessee. The United States Navy funds the RSVP program. Draper's role in RSVP is the development of the sensor cluster and package. ORNL's role is to develop a power module ASIC which monitors and controls the power scavenging devices and the primary battery in an overall effort to efficiently provide regulated power to the sensor cluster. Since new scavenging methods are developed with advances in technology, provisions are to be made to accommodate these future sources.

1.1.2 Goals and Specifications

The overall goal of RSVP is to reduce the number of ship's personnel by using wireless sensor clusters. In today's modern age, the main purpose of a ship's personnel is damage control, specifically the fighting of fires during a wartime situation. The largest cost of maintaining a running vessel is the human support cost. Simple personnel reduction will not solve the problem, since there are still manpower requirements to support and maintain the vessel as well as to fight and save the ship. If a device could be designed to monitor such items as environmental conditions and machinery, then a smaller crew could be utilized more efficiently. This smaller complement could be sent to areas where problems occur, rather than being used for observational needs.

With a sensor array cluster, which can provide the appropriate data to a central monitoring room, ship assessment time can be greatly reduced and manual investigation can be eliminated. During a damage control scenario, improving response time from hours and minutes to seconds will not only save money, it can save lives. If the overall crew can be reduced by 70%, an early prediction of $2.5 - $4 billion in life cost savings is possible.[1]

One of the operating goals of the RSVP program implementation is to show that power can be scavenged from environmental sources, i.e. such as ambient light or vibration, which would allow the cluster array to be self-powered. By utilizing micro-power electronics, and cycling power on components, low power self-consumption can be achieved. The current design is working towards an eventual migration to a self-contained ASIC in which the total power consumption can be reduced.

[1] As estimated in the RSVP Execution Plan, 1/28/99

For ORNL's involvement in development of the power module ASIC, there are several specifications that must be met. First, a well-regulated 3.3-volt supply voltage must be maintained. This will be accomplished with the use of a low-dropout linear regulator. The stable supply need is created with the use of a ratio-metric A-D converter in the sensor cluster, which uses the supply voltage as a measuring reference. For this reason the supply voltage needs to be stable over one conversion. In future generations, the use of high supply voltages may be required, so plans for a step-up converter have been made.

Next, the electronic current needs of the sensor array cluster must be provided. The average current requirement of the cluster is 330 micro-amps. On start-up and during periods of wireless communication interruption, the transmitter of the sensor array cluster must establish communications with a central unit in the room in which they are placed. This central unit communicates with the ship's control room. During this period, the transmitter uses an average current of 100 mA to select its transmit channel. A primary battery, capable of providing this short-term current load is used. For the listed current needs, the load regulation provided at the output should be 100mV for Iout in the range of 10mA < Iout < 100mA and 5mV for current loads less than 10mA.

The overall average power delivery goal is 2mW. This goal would provide the power needs of the sensor array cluster. Since power that can be scavenged from the environment is limited, and the general need is to increase efficiency, self-power consumption must be reduced. The overall goal of self-consumption is 100 microwatts, with power transfer efficiency from scavenged source to regulated output of 50 percent.

1.1.3 General System Design

Figure 1.1 below shows a simplified diagram of the power module concept. Upon start-up the voltage regulator will be connected to the primary battery. The power module ASIC monitors the scavenged power sources, one of which is a photovoltaic array. When any source reaches a supply voltage of 4 volts, the control logic will start the DC-to-DC converter and charge the energy storage capacitor. When its level has reached a minimum of 3.6 volts, then the linear regulator input would be switched to the capacitor. If at any moment the voltage across the capacitor drops below the 3.6-volt level, then the regulator is switched back to the primary battery. When required by the sensor cluster, the step-up regulator will be switched on to produce a secondary output voltage.

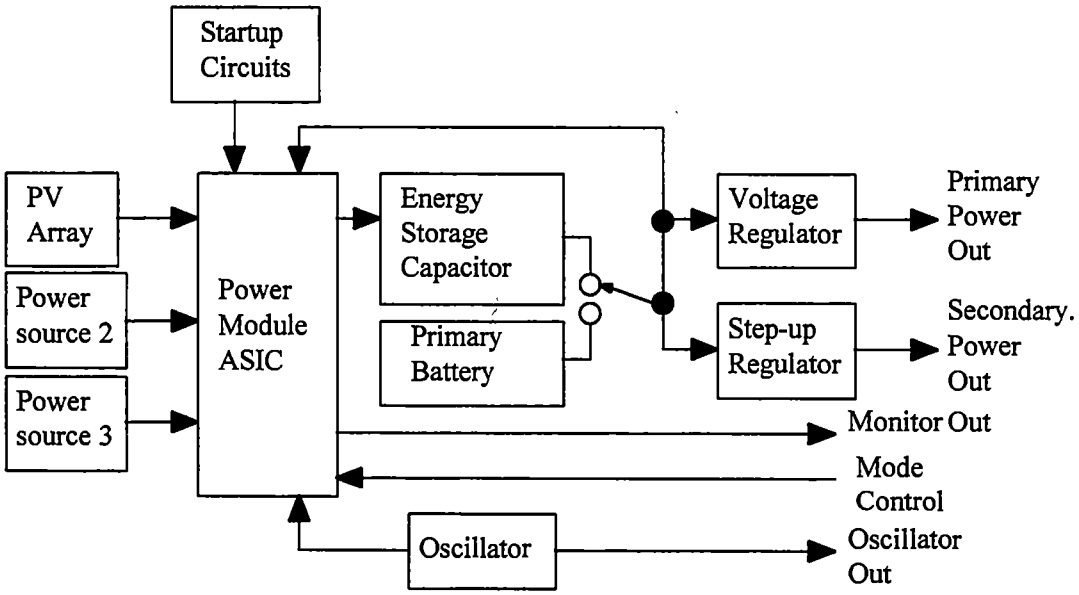


Figure 1.1 System Block Diagram.[2]

[2] from the RSVP Module Concept Design, Rev 1.2

In the heart of the power module ASIC, is a step-down switching regulator. The basic switching regulator consists of switch and energy storage units, which are used to transfer charge between voltage potentials. Voltage control by varying the switching duty cycle allows the switching regulator to be more power efficient. A step-down regulator was chosen with the assumption that the scavenged sources will be higher than the regulated 3.3 volts.

1.2 The Power Module ASIC and Test Board

The power module ASIC is the main component of the RSVP project. It consists of electronics that monitor and control the scavenging devices as well as the DC-to-DC converter. In this first generation rendition, two ASIC's have been fabricated. The first ASIC contains the linear regulator, power switch for capacitor and battery, voltage reference, and the DC-to-DC converter switch. The second ASIC contains several low voltage comparators and two more voltage references. In the early stages of design, it is beneficial to split up a design into its separate components. This allows the testing of these components on an individual basis as well as alternate designs. All designs require both theoretical and practical engineering investigations before a full implementation can be achieved.

A re-configurable test board was designed to test both ASIC's as well as simulate the final system design for which the final generation power ASIC module would be used. On this test board, the off-chip components such as the step-up regulator, oscillator and digital control logic, in the form of an ALTERA programmable part, are placed and can be changed out if necessary. In the final generation the majority of components

would be self-contained within one ASIC. The test board and ASICs when configured will regulate the 3.3-volt supply, as well as communicate with the sensor cluster micro-controller, and monitor the cluster's power needs.

1.2.1 DC-to-DC Conversion

DC-to-DC conversion involves the transformation of one voltage level to another, and there are several methods available to the designer. A switching mode voltage regulator such as a buck or boost converter can be used to step-down or step-up the supply voltage in any ratio. A charge pump can often be implemented if the goal is to double the supply voltage or to invert it. Linear regulators require a voltage drop from input to output to maintain a lower output voltage potential, and are therefore sometimes referred to as dissipative regulators.

1.2.2 Regulation

A power supply that is regulated provides an output voltage, Vout, which is essentially independent of the load current, I_L, drawn from the supply and also nearly independent of operating temperature. The majority of voltage regulation applications involve the stepping down of the primary voltage source. There are two basic types of voltage regulators, linear and switching.

The method of linear regulation involves the use of a voltage reference, a series pass transistor to provide current, and an error amplifier (in the basic sense). The linear voltage regulator compares a sample of the output voltage to a reference voltage and uses negative feedback to correct the output voltage value. The sample is usually determined

by the ratio of two feedback resistors. The error amplifier compares the sampled voltage from the output to the voltage reference, amplifying the difference between the two. The accuracy of the output voltage is primarily based on the accuracy of its voltage reference. Although a linear regulator can perform a step-down conversion, it has inherent power inefficiency. Even with ideal components in a linear regulator, 100 % efficiency cannot be reached. Assuming that the regulator used no current, such that I_{IN} equals I_{OUT}, then the efficiency is *Vout* divided by *Vin*.

A switched mode converter uses inductors and capacitors as energy storage units, and a power switch. Switch-mode converters are advantageous because they have very high power efficiency. An ideal converter uses no power (assuming an ideal switch and no circuit resistance). In switched mode power conversion, if ideal components were used, a theoretical 100% efficient converter could be designed.

1.2.2.1 Basic Switch Mode Converters

There are three basic types of switched mode converters, Buck, Boost and the Buck-Boost.[3] These are termed "basic" in the sense that they utilize some simple components such as a switch, inductor, diode and capacitor. The Buck converter takes a voltage and reduces it down to a smaller potential. The Boost switched mode converter, as its name implies, takes a lower voltage and boosts it up to a higher value. The Buck-Boost converter is configurable to perform as a buck or a boost converter, but is unique in that it can generate a negative voltage supply from a single positive voltage supply.

The Buck, or step-down converter, as viewed in Figure 1.2, produces a lower average output voltage than its input voltage. This mode of operation is known as the forward mode, with a LC filter section directly after the power switch. Operation of the Buck converter consists of closing the switch so that charge flows through the inductor and into the capacitor and load. The current passing through the inductor increases linearly resulting in increasing energy storage in the inductor. When the switch is opened, the energy stored in the inductor cannot change instantaneously, so that current must still continue to flow. This causes the voltage at the input of the inductor to fall below ground potential. The diode, therefore, becomes forward biased which provides a current path. As the current decreases due to the open switch, a reduction occurs in the voltage across the load capacitor. The variation of the duty cycle of the switch controls the magnitude of the output voltage.

This type of converter is highly efficient and simple to design. There are some disadvantages to the Buck converter: high capacitor ripple, no isolation between input and output, and a possibility of damage due to short-circuiting the output.

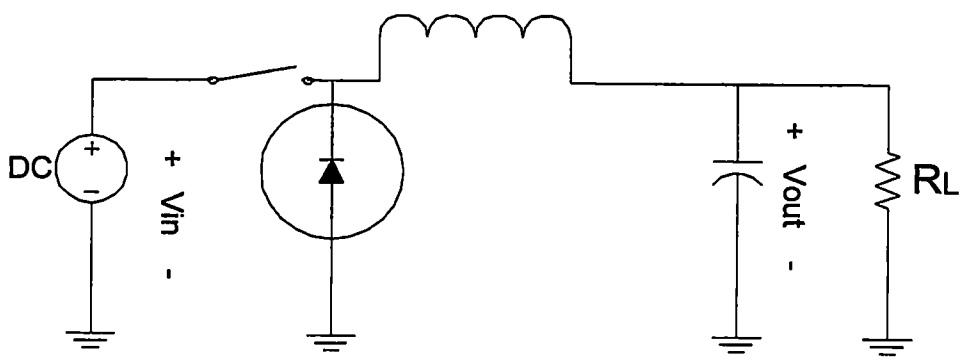


Figure 1.2 Buck Converter.

The Boost, or step-up converter in Figure 1.3, produces an output voltage, which is always larger than its input. When the switch is closed, a circuit loop is formed with the source and inductor, and inductor current ramps up. When the switch is opened, the magnetic flux previously established in the inductor produces a voltage across the inductor that increases to a higher potential than that of the input source. This causes the diode to become forward biased. The energy stored in the inductor is transferred to the output capacitor, which adds to the output voltage. The overall efficiency of the boost converter is typically about 80 percent.

The Boost is also a simple converter to design, and can operate at high switching frequencies. The Boost converter shares the same disadvantage as the Buck, as there is no isolation between the input and output. The diode does provide limited short circuit protection, since a diode is typically current limited and will self-destruct when that current limit is exceeded. The Boost has a poor transient response and suffers also from high peak currents.

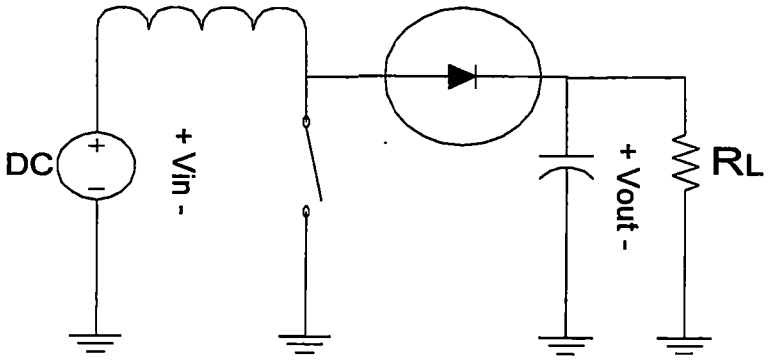


Figure 1.3 Boost Converter.

The Buck-Boost converter can provide either step-up or step-down of the voltage supply is seen in Figure 1.4. When the switch is closed, a loop is again formed with the inductor and it stores energy. When the switch is opened, the inductor voltage falls below ground, which pulls charge through the diode out of the capacitor. This allows for a negative voltage potential and that potential is controlled by the duty cycle, as with the other two converters.

The main advantage to the Buck-Boost is the availability of having a negative polarity with just a positive supply and without a transformer. In this design *Vin* is always greater than *Vout* Again, the switch must be able to handle high peak currents and this converter also has a poor transient response. All three converters share the same deficiency of only being able to provide a single output. There is no isolation between input and output, yet current load is limited by the diode.

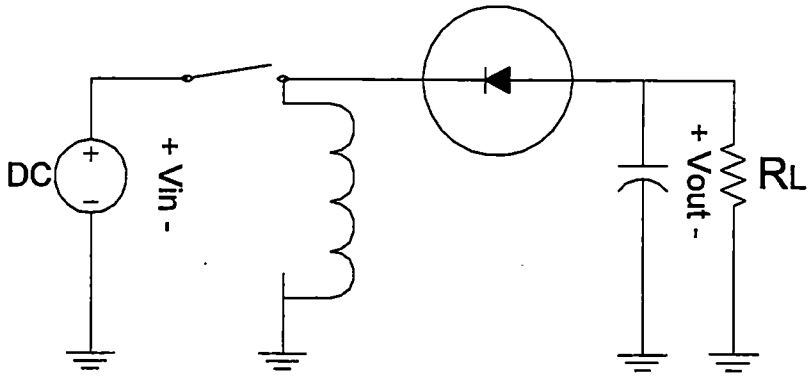


Figure 1.4 Buck-Boost Converter.

1.3 Scope of Thesis

The primary topic of this thesis is the system design of the power module ASICs and re-configurable test board for the RSVP project. Emphasis within this thesis will be given to the design of a micropower CMOS buck regulator. In this Chapter 1 a discussion of the goals of the RSVP project has been provided. In the following chapters, which focus on the overall system design, operation, and performance, this thesis will describe how those goals were met.

A general introduction to basic DC-to-DC conversion techniques was provided. In Chapter 2 a theoretical analysis of the Buck converter is performed. From this analysis, equations giving output voltage and ripple based on input voltage and load current are provided. A new way of regulating the converter supply voltage, necessary to minimize power consumption, is shown. Circuit simulation and theoretical comparisons will be presented in Chapter 3.

Chapter 4 provides results from component and the system testing. Critical to the design of the Buck converter switch was the use of poly2 transistors, due to their higher voltage application. Parameter testing of these transistors, using the HP4156A Precision Semiconductor Parameter Analyzer was performed and data is provided from the test results.

The topics of Chapter 5 will be a final discussion of the performance of the system as well as the modifications towards a next generation design.

2.0 Design of the Power Module ASICs and System

2.1 Scavenging Methods

One of the main goals of RSVP is to demonstrate power scavenging from the environment. There are several sources of power in a ship's environment from which power can be scavenged. Photovoltaic energy can be scavenged from the overhead lights in the vessel's various hulls. Thermal energy can be scavenged from temperature gradients at different mounting points. Vibrational energy can be scavenged from the various rocking movements caused by the ocean motion. The power module ASIC chip is designed to monitor and control the scavenging of photovoltaic energy, but the options for adding any additional scavenging methods are included in the chip development.

2.1.1 Photovoltaic Energy

Photovoltaic energy is readily available wherever there is a light source. How much energy can be harvested depends on the lighting level, the type of light, and the type of photovoltaic cells used. Photovoltaic systems today are very advantageous and are always improving. First, a PV system has no moving parts, no fuel needs, and low maintenance costs. Typical photovoltaic cells that are commercially available are warranted for 25+ years. Most cells are configured into array modules, and these modules are easily expanded onsite.

A photovoltaic cell, at the basic level, is a pn junction [1]. The junction absorbs a photon, which in turn frees an electron/hole pair. When enough photons have been

absorbed, a small current is generated. Each cell is made up of these junctions and by arraying cells in parallel or series, a higher current or voltage can be achieved.

Unfortunately, even with today's technology and the current developments in design processes, the average efficiency is around 25 percent for photovoltaics. Even in the brightest environment, not all-photovoltaic energy is absorbed. A single pn junction will only absorb a small range of wavelengths of the incoming light. More than half of the energy that is generated is lost to heat in the lattice structure. Even with modern silicon processes, which are extremely contamination free, there are still surface defects in the silicon crystal. These surfaces defects can inhibit the absorption of light. Power can also be lost due to resistive mechanisms in the structure. When PV modules are arrayed, there are often mismatches due to different process runs.

As chip processes continue to improve, so will the development of PV's. Design concepts such as cascading two different wavelength absorbing pn junctions have been tested and shown to produce more energy. Non-reflective coatings help reduce surface reflections which stop light penetration. Photovoltaics are proving to be reliable energy sources for a scavenging system.

2.1.2 Future Scavenging Methods

Currently under way are new developments in power scavenging. The method of vibrational scavenging is being tested at Massachusetts Institute of Technology. Vibrational energy is readily available aboard a Naval Vessel. First, due to ocean currents, a ship will rock from bow to stern. The use of a pendulum connected to a generator, could generate some power due to this rocking motion. There is vibration

energy available in other forms, such as the ventilation system and steam pipes. Some sensor clusters will be mounted on machinery, which is also a vibrational energy source.

Another scavenging source is thermal energy. This energy is available wherever there is a temperature gradient. If a sensor cluster were mounted on the interior hull of a ship, there would be a significant temperature gradient between interior temperature and ocean temperature. A heating duct or steam pipe will also provide a harvestable temperature gradient. There may be additional future sources that can be scavenged, so RSVP was designed with that in mind. For the present, a primary battery and photovoltaic cells will provide the energy needs of the sensor cluster.

2.2 The Buck Converter

The Buck converter is a switch mode converter, which transforms a higher voltage to a lower voltage. The basic components to form the Buck converter are a switch, diode, inductor and capacitor. The Buck converter was chosen for its simple circuit design and high efficiency. In the ideal case, the circuit dissipates no power, and therefore has a theoretical efficiency of 100 percent. In the actual circuit there will be some losses due to the resistance of the switch, diode, and inductor, and also due to the leakage current of the diode and capacitor.

Due to modern processing limitations, only the switch and diode can be made internally to the ASIC. Capacitors can be constructed using two layers of polysilicon, but are limited to a few pF. No inductors are available in today's chip processes. There have been cases in which, wire bond inductance has been used, but the resulting inductor values are too small to meet the needs of RSVP. Diodes can be made on a chip, but often

take up large amounts of space. For these reasons, the 20,000 μF capacitor, 1mH inductor and Schottky diode are all located off chip.

2.2.1 Theoretical Analysis

Since the Buck converter is a switch mode converter, switching action is the way power is transferred. Figure 2.1 is a basic circuit for the Buck converter. We will assume an ideal case with no resistance loss due to the switch or diode. For this theoretical analysis, it is assumed that an ideal inductor and capacitor are used. The voltage V_L will be defined as the inductor voltage, with i_L the current through it. The output voltage across the capacitor and load resistor R_L will be defined as $Vout$. I_O is the average load current through R_L.

In analyzing the Buck converter, one must first know the mode of operation. There are two modes, continuous and discontinuous conduction. In continuous conduction, the current $i_L(t)$ is never less than zero. In the discontinuous conduction mode, the inductor current does reach zero; in this mode, the energy in the inductor is fully removed.

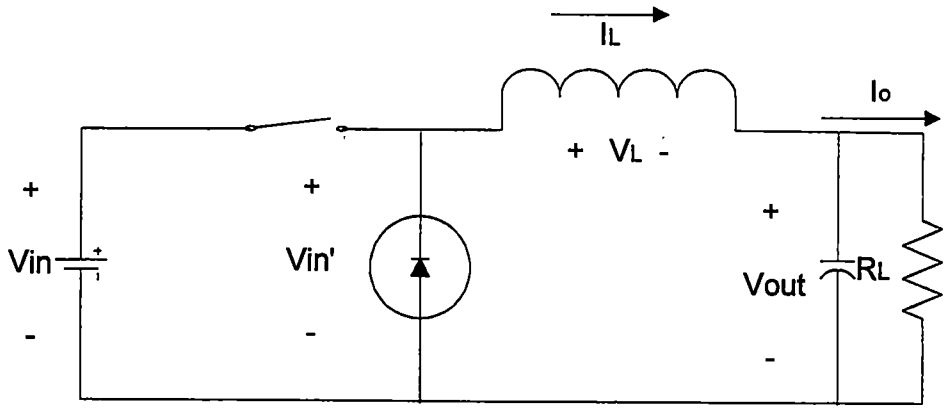


Figure 2.1 Buck Converter Circuit.

In the overall effort to reduce self-power consumption in the RSVP project, components are switched on and off for certain time intervals. These components include the comparators and references. Since the comparators will only be on for a limited time, the output will be held constant with the use of a flip-flop. The DC-to-DC converter will run until it receives a shutdown signal from the control logic. When the converter is needed again, it will be restarted with the clock signal.

The ideal Buck converter creates an average output voltage, which varies with the clock signal's duty cycle. Figure 2.2 is representative of a possible switching cycle for the Buck converter operating in the continuous mode. [3] During the period T_{ON}, the switch is closed and voltage is applied across the inductor. During T_{OFF} the switch is in the open position and the rest of the circuit is isolated from the input. The two times T_{ON} and T_{OFF} combine to form the period T_s, which is equivalent to $1/f_s$ where f_s is the switching frequency. The switching frequency chosen for RSVP is 32.768kHz, which is a standard clock frequency. The duty cycle was chosen to be 50%.

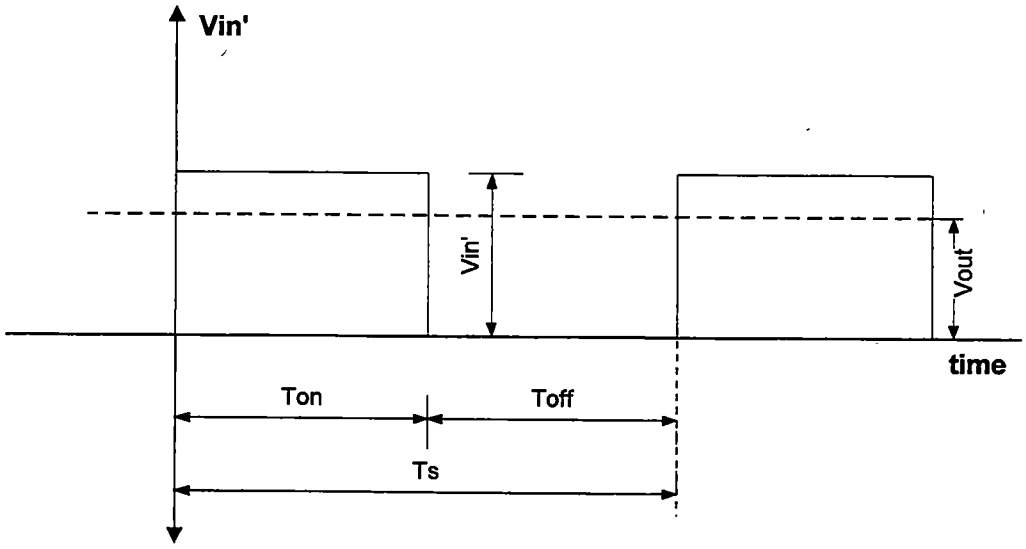


Figure 2.2. Typical Cycle for a Buck Converter.

To calculate the total average voltage, the time varying output *Vout(t)* can be integrated over one switching cycle. Equation 2.1, known as the mean value theorem, shows the

$$Vout\,(avg.) = \frac{1}{Ts} \cdot \int_{0}^{Ts} Vout\,(t)dt \qquad (2.1)$$

integral of *Vout(t)* from the initial start of conversion, t=0 to the end of one cycle t=*Ts*.

One of the assumptions made in this analysis is steady state operation; the waveform repeats from one cycle to another. In this analysis the integral of the inductor voltage, V_L, over one time period, T_s, must be equal to zero.[4] This is defined by Faraday's Law in which the average voltage across the inductor over one complete period is zero. The next assumption is that the circuit will be operating in the discontinuous mode. To prove this, we will look at the analysis from the standpoint that the circuit is operating at the boundary between discontinuous and continuous conduction. In this instance all the current in the inductor is drained at the end of the cycle as seen in Figure 2.3.

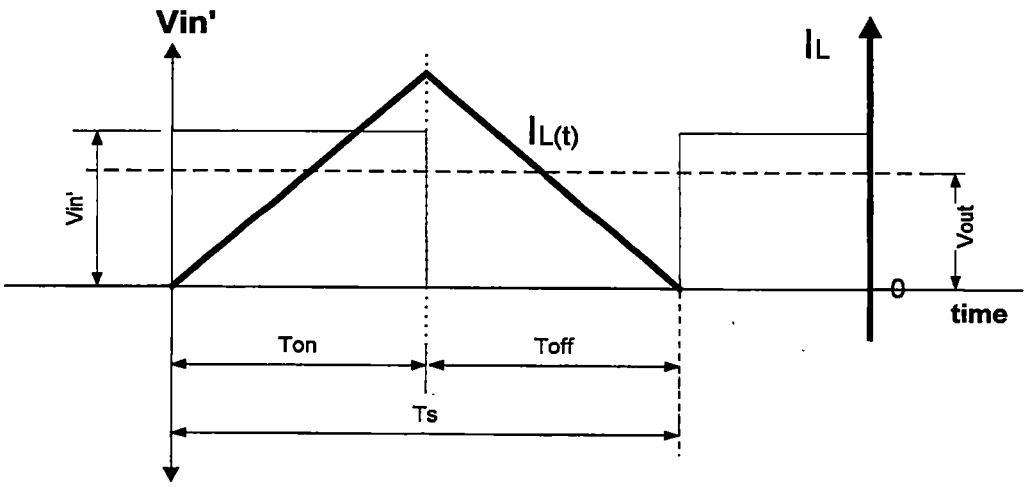


Figure 2.3 Boundary Between Continuous and Discontinuous Conduction.

The equation for the current $I_{OBoundary}$, is ½ the peak inductor current i_{Lmax}. [4] The equation for the inductor current is the slope of the current times time, t, as seen in

$$i_L(t) = \frac{Vin - Vout}{L} \cdot t \quad \text{for } 0 < t < T_{ON} \tag{2.2}$$

Equation 2.2. The peak current occurs at the end of time T_{ON}. Substituting this time into (2.2), the current at the mode boundary is defined as Equation 2.3. The duty cycle, D, is

$$I_{OBoundary} = \frac{(Vin - Vout)}{2L} \cdot T_{ON} \tag{2.3}$$

defined as T_{ON}/T_s, the period that the switch is on, over the total time. Substituting this back into (2.3), I_O in terms of the duty cycle is Equation 2.4.

$$I_{OB} = \frac{(Vin - Vout)}{2L} \cdot D \cdot T_s \tag{2.4}$$

If the average current in the load becomes less than I_{OB}, then the inductor current is discontinuous. The current, I_{OB}, can be written in terms of the input voltage:

$$I_{OB} = \frac{Vin \cdot Ts \cdot D \cdot (1 - D)}{2L}. \tag{2.5}$$

We can substitute the values used for RSVP into (2.5) to simply it, arriving at Equation 2.6. Next, we need to define the variable R_{max}, which will be the resistance of the load R_L

$$I_{OB} = \frac{Vin}{262.1\Omega} \tag{2.6}$$

at the maximum load current, I_O, for the converter, which is 10 mA. Assuming the output is sitting at 3.6 volts, then R_{max} is 360 ohms. A second variable R_{avg} will be defined as the load resistance for the average current draw of 330 μA. With the same voltage level, R_{avg} is 10.9 k.

The variable L_B is defined as the minimum size inductor required for a specific load to maintain continuous conduction. If it can be shown that with the chosen 1mH inductor at both R_{max} and R_{avg} values is smaller than L_B, then the converter will run in discontinuous mode. Equation 2.7 defines L_B in terms of R_{max}. The duty cycle was chosen

$$L_B \approx \frac{R_{MAX} \cdot T_S \cdot (1-D)}{2} \tag{2.7}$$

to be 50%. For the R_{max} of 360 ohms, L_B is 2.74 mH. Next taking Equation 2.6 and substituting in R_{avg} for R_{max}, the L_B is calculated to be 83.1mH. In either case the 1mH inductor chosen is smaller than each respective L_B and the converter will operate in discontinuous conduction mode.

Another check for discontinuous conduction is that the maximum load current, I_{OMAX}, will be less than the V_{IN}/ 262.1 term. If the maximum load current the converter will have to source is 10 mA, then V_{IN} must be greater than 2.62 volts. This has already been established since the input source will not be connected to the converter until the source voltage has reached 4 volts.

With discontinuous conduction, the current in the inductor is drained before $t = T_s$. Figure 2.4 shows one cycle of the converter and shows a plot of the inductor voltage V_L and a plot of the inductor current $i_L(t)$. In the Figure, area **A** is the voltage-time product in the inductor during time T_{ON}. This occurs when the switch is on, and energy builds in the inductor. Area **B** is the voltage-time product in the inductor during the time X_1 of T_{OFF}. During this time, the switch has opened. These two areas must be equal. Since the switch has opened, the magnetic field of the inductor collapses.

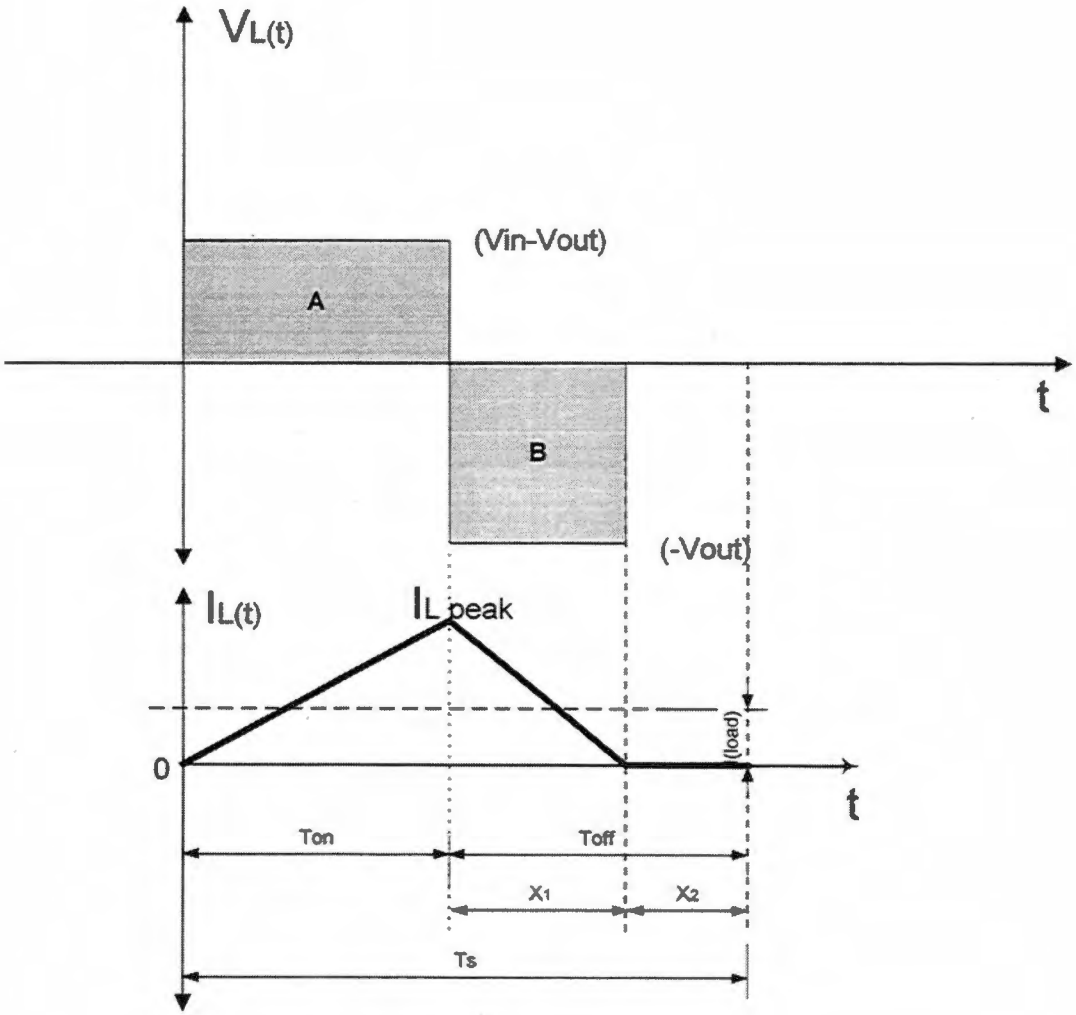


Figure 2.4. Buck Converter, Inductor Voltage and Current States for One Cycle.

By Faraday's law, this collapsing magnetic field induces a voltage, which is opposite in polarity to the originally applied voltage [2]. The voltage at the left side of the inductor is clamped to ground by the diode. This causes the capacitor voltage to decrease to a lower value. In viewing the characteristics of the inductor current of Figure 2.4, it can be seen that during T_{ON} the current ramps to a maximum. At the end of T_{ON} the current decays for the time $T_{ON} < t < T_{OFF}$. Figure 2.4 shows that the inductor current reaches zero in the discontinuous conduction mode.

Equation 2.8 equates the areas A and B from Figure 2.4, in terms of the slope of

$$\frac{Vin - Vout}{L} \cdot T_{ON} = \frac{Vout}{L} \cdot X_1 \tag{2.8}$$

the current and the time the inductor is conducting. The variable X_1 is defined as the time it takes for the inductor current to be drained during $T_{ON} < t < T_{OFF}$. Taking (2.8) and simplifying it, we arrive at Equation 2.9 and through further simplification the output

$$(Vin - Vout) \cdot T_{ON} \cdot Ts + (-Vout) \cdot X_1 \cdot Ts = 0 \tag{2.9}$$

$$\frac{Vout}{Vin} = \frac{T_{ON}}{T_{ON} + X_1} \tag{2.10}$$

voltage in terms of the input voltage can be found in Equation 2.10. Varying the duty cycle will vary the output voltage. Using some definitions, T_{ON} is $D * T_s$ and X_1 is equivalent to Δ_1 times Ts, where Δ_1 is a fraction of T_S, then substituting D and Δ_1, Equation 2.10 can be rewritten as Equation 2.11:

$$\frac{Vout}{Vin} = \frac{D}{D + \Delta_1}. \tag{2.11}$$

In the discontinuous mode operation, both *Vin* and *Vout* remain nearly constant, over a period of the clock because of the large input and load capacitors.

Two design equations that are beneficial in converter applications are the ripple voltage and output voltage in terms of input voltage and load current. Observing the typical inductor current cycle in Figure 2.4, the average load current I_O would be equal to ½ the area under the current function divided by the total time as shown in Equation 2.12.

$$I_O = \frac{i_{L\max}}{2} \cdot (D + \Delta_1) \tag{2.12}$$

The peak current at T_{ON} is equal to the peak current during T_{OFF} and can be written as Equation 2.13. Taking (2.13) and substituting it into (2.12), current I_O can be written in

$$i_{L\max} = \frac{Vout}{L} \cdot \Delta_1 \cdot Ts \tag{2.13}$$

terms of the output voltage in Equation 2.14. The equation for *Vout* (2.11) can be

$$I_O = \frac{Vin \cdot D \cdot \Delta_1 \cdot T_S}{2 \cdot L} \tag{2.14}$$

substituted into (2.13) and we have an equation for I_O in terms of *Vin*.(Equation 2.14) Next, we solve for Δ_1 in terms of *Vin* and I_O to obtain Equation 2.15, which now

$$\Delta_1 = \frac{I_O \cdot 2 \cdot L}{Vin \cdot D \cdot T_S} \tag{2.15}$$

provides a way for determining the part of T_{OFF} that the inductor is conducting based on the load current. We can now substitute the equation for Δ_1 back into the original *Vout* Equation (2.11) and have *Vout* in terms of I_O the load current and the input voltage *Vin* in

Equation 2.16. It is evident from this equation that there is a non-linear dependence of

$$Vout = Vin \cdot \left(\frac{D}{D + \frac{2 \cdot I_O \cdot L}{Vin \cdot T_S \cdot D}} \right) \tag{2.16}$$

Vout on the input voltage and duty cycle, though for RSVP, the duty cycle is fixed at 50%.

Next, we derive the equation for the ripple voltage. The change in output voltage *ΔVout* can be written as Equation 2.17. Figure 2.5 represents one converter cycle and an example of the load capacitor ripple. During the initial part of the cycle, i_L is less than the

$$\Delta Vout = \frac{\Delta Q}{C} \tag{2.17}$$

load current so the capacitor sources part of the load current and its voltage drops. When i_L is greater than the I_O, at time t_1, then the load capacitor voltage increases. The inductor current begins to decrease at the end of T_{ON} therefore the charge passed to the capacitor also decreases. When i_L reaches t_2, the inductor current falls below I_O, so the voltage across the capacitor begins to decrease. At the end of time X_1, the inductor current is zero, and the load capacitor voltage falls off at a greater rate as it sources all of the load current. The process starts all over again at the beginning of the new cycle.

To find the ripple we need to find the *ΔQ* in (2.17). This is given by Equation 2.18 where we integrate the current that flows into the load capacitor from time t_1 to t_2.

$$\Delta V = \frac{1}{C} \int_{t_1}^{t_2} \left[i_L(t) - I_O \right] \cdot dt \tag{2.18}$$

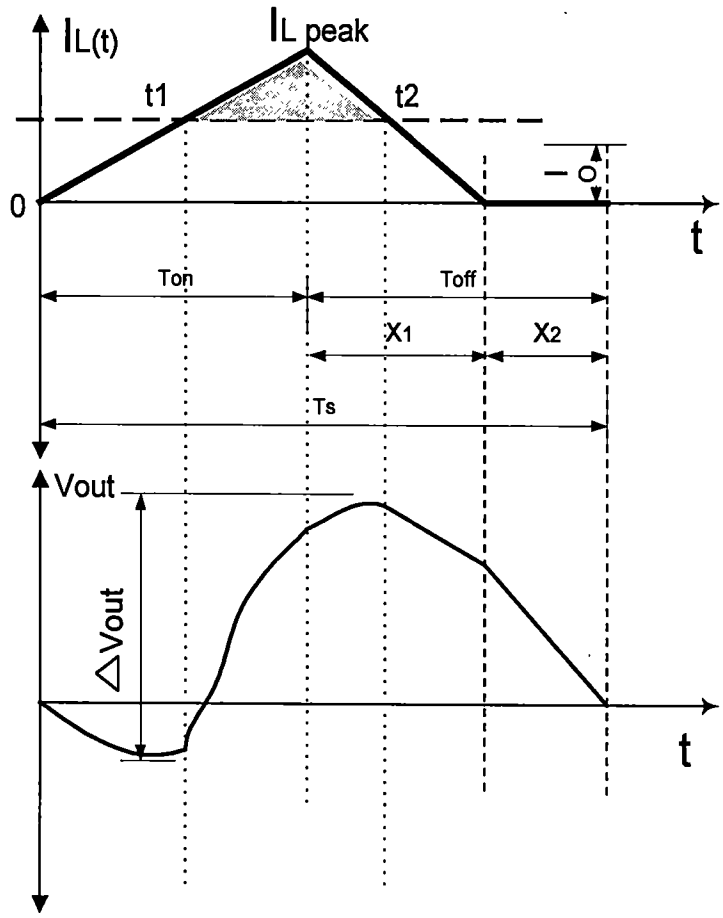


Figure 2.5. Example Ripple Voltage Vs Inductor Current.

To determine ΔQ, the times t_1 and t_2 from the figure must be determined. At these points the load current is equal to the inductor current. During the period $0 < t < T_{ON}$ the inductor current i_L is determined by (2.2). Substituting in t_1, and setting the current i_L equal to the load current I_O yields Equation (2.20). Next, we can re-arrange terms and

$$\frac{Vin - Vout}{L} \cdot t_1 = I_O \tag{2.20}$$

find t_1 in terms of *Vin, Vout* and load current I_O in Equation 2.21. To determine t_2 we

$$t_1 = \frac{I_O \cdot L}{Vin - Vout} \tag{2.21}$$

know that the current during the period $T_{ON} < t < T_{OFF}$ is the peak current minus the inductor current defined by Equation 2.22. At time t_2 the load current I_O is equal to

$$i_L(t) = i_{L\max} - \frac{Vout}{L} \cdot (t_2 - T_{ON}) \tag{2.22}$$

(2.22) and we can once again re-arrange terms and solve for t_2 in Equation 2.23.

$$t_2 = \frac{(i_{L\max} - I_O) \cdot L}{Vout} - T_{ON} \tag{2.23}$$

We now have the two times t_1 and t_2 defined and can substitute them back into (2.18) and solve for the ripple. Rather than integrating we can use geometry to arrive at a final solution. Referring back to Figure 2.5, we stated that the ripple occurs between the time's t_1 and t_2. The ripple is defined by the shaded area under the inductor current waveform in the figure. We can defined the ripple in terms of this area in Equation 2.24.

$$\Delta V = \left[\frac{t_2 - t_1}{2 \cdot C} \right] \cdot (i_{L\max} - I_O) \tag{2.24}$$

The ripple is 1/C times the area of the triangle, which is ½ base * height. The height is the difference between the inductor and load current while the base is the difference in the two time's t_1 and t_2. Now we can substitute the values in (2.24) and we arrive at Equation 2.25. From (2.25) we can make some variable substitutions and re-arrange terms. The

$$\Delta V = \left[\frac{\frac{(i_{L\max} - I_O)\cdot L}{Vout} + T_{ON} - \frac{L \cdot I_O}{Vin - Vout}}{2 \cdot C} \right] \cdot (i_{L\max} - I_O) \qquad (2.25)$$

current i_{Lmax} is defined by (2.2) and reaches a maximum at T_{ON}. Substituting values in (2.25) we arrive at a simpler solution in Equation 2.26.

$$\Delta V = \frac{1}{2 \cdot C} \left[\frac{(Vin - Vout)}{L} \cdot T_{ON} - I_O \right] \cdot \left[\frac{Vin}{Vout} \cdot (T_{ON} - \frac{L \cdot I_O}{Vin - Vout}) \right] \qquad (2.26)$$

It would be beneficial to the reader to see some numerical values so the cases of 330 μA, the average load current, and 10 mA the maximum load current for the converter are examined. The assumptions we will make for each case is Vin = 5 volts, L = 1 mH, C = 20,000 μF, and the clock of 32.768 kHz with a fixed duty cycle of 50%. For each case, we can calculate *Vout* by Equation 2.16. *Vout* can then be used to determined the peak current i_{Lmax} and the two times t_1 and t_2. For the case of 330 μA load current, we assume steady-state. Entering in the values above into the pre-mentioned equations we arrive at the data results below.

Values for 330 μA.

Vout	i_{Lmax}	t_1	t_2	ΔV
4.915 V	1.3 mA	3.88 μs	15.45 μs	0.279 μV

For the maximum current case of 10 mA, we assume that the current suddenly changes from the average current to a maximum. Once again we can find the steady state solution, using (2.16) to solve for *Vout* and (2.20) thru (2.23) to find the other values listed below. As expected, the sudden demand for current creates a much higher ripple than that of the average load current case.

Values for 10mA.

Vout	i_{Lmax}	t_1	t_2	ΔV
3.28 V	26.2 mA	5.81 μs	20.2 μs	5.84 μV

2.2.2 Physical Design

There are several considerations required for the converter design. Since an ASIC implementation is sought, the correct design process must be selected. In the overall system design, a small package for the sensor array and power control module ASICs is required to allow for accessible mounting throughout the naval vessel. Any off-chip components, such as the capacitors need to be chosen to accommodate the package size.

2.2.2.1 Process Selection

In the typical chip process today, supply voltages are in the 2.2 to 5-volt range, with the trend towards even lower voltages. Lower voltages translate to lower power consumption. The scavenged power for RSVP may have a voltage higher than 5 volts. Most modern processes anticipate a low supply voltage. For RSVP, AMI's 1.2-micron ABN process was chosen. This is an N-well, 14-mask process with 2 metals and 2 poly-

silicon layers available. This process allows, with the use of Poly2 transistors, supply voltages in the range of 2.5 to 11 volts. With this accessibility to the higher voltages, larger transistors are required with a minimum gate length of 3.5 microns.

2.2.2.2 Component Selection

The switch plays an important role in the converter. It must be capable of handling a higher than normal chip voltage, as well as some high peak currents due to the switching action. Resistivity of the switch is also important. The smaller the voltage drop across the switch, the greater the efficiency. Since the inductor and diode components will have some parasitic resistance, the size of the switch should be large to decrease its series resistance. An overall goal was to set the voltage drop less than 250mV for maximum current. A NMOS and PMOS complementary pair was used to meet this goal.

The non-ideal diodes will both suffer from some parasitic resistance, leakage current, and forward voltage drop. The diode also needs to have a fast time response to allow rapid change from forward to reverse bias. The Schottky diode family characteristics include a low forward voltage drop and low leakage current. They are often selected for DC-to-DC conversion applications and, therefore, one was chosen for RSVP.

It has been discussed how the inductor plays an important role in the conversion process. A fairly large value inductor, in terms of board components, is required for two reasons. The first is the slow clock frequency. Related to this is the current requirement. A smaller inductor at the 32.786kHz clock frequency will provide a larger peak current than desired. This larger current could damage the circuit or create too large of a voltage

drop across the resistances of the switch, diode and inductor. A large inductor, 1 mH, will have a smaller current and resistance typically less than 15 ohms. This large inductance value will also reduce ripple voltage.

For the capacitor, ideally, a large value would be preferred, but is unrealistic. The capacitor size influences the ripple as well as linear regulator performance. When a load is drawn from a battery, its voltage remains relatively constant until the battery has lost most of its energy. A capacitor's voltage will slowly decrease with the energy taken from it. To determine the proper capacitor value, the current needs of the system are considered. At one instance during the sensor cluster operation, there is a current drain of 100 mA for 10 milliseconds. Using Equation 2.27, the charge change is found to be 0.001

$$Q \approx i \cdot \Delta t \tag{2.27}$$

coulombs.

An ideal linear regulator would be immune to small changes in input voltage. If the linear regulator is stable against voltage changes less than 100 mV, then solving Equation 2.28, the capacitance required is 10,000 μF. A conservative value of 20,000 μF was chosen.

$$Q \approx C \cdot \Delta V \tag{2.28}$$

Using a 10,000 and 20,000 μF capacitor on the input and output respectively provides more validity to the assumptions that *Vin* and *Vout* remain relatively constant. Due to package size restrictions, these capacitance values will more than likely be composed of paralleled elements, which would also aide in reducing ESR.

2.3 System Design

The Buck converter is a critical part of the RSVP power control module. Figure 2.6 is an overall system view. There are three sources, one of which is predetermined to be a photovoltaic cell array, from which power can be scavenged. Each source has its own DC-to-DC converter switch in which all three switch outputs are tied together. During each conversion process, only one source will be enabled at a time. This allows scavenging from three sources, yet only utilizing a single Buck converter.

There is one major storage capacitor for the output of the DC-to-DC converter, which is 20,000 μF. This capacitor was chosen such that it could supply the raw power needs of the linear regulator over a long period of time. Three alkaline batteries form the primary battery, which is a raw supply source of 4.5 volts. A power switch to the linear regulator connects each of these sources. This power switch is controlled by a programmable part, which toggles between the two sources. The switch will toggle to the power capacitor when enough energy is available and toggle back to the battery when a low supply exists or high current demand by the sensor cluster transmitter is required.

In this first generation of the RSVP control module, the digital logic is placed in an ALTERA programmable logic part. This allows the functionality to be changed after testing. There are several inputs to the programmable part. First, there is a clock signal from an off-chip oscillator. The ALTERA part will send an appropriate clock signal to the respective DC converter switch. Other inputs to the part are control signals from the sensor array cluster. One of these signals will notify the ALTERA logic of a high current drain. This occurs whenever the sensor array cluster needs to scan for a new wireless transmission channel.

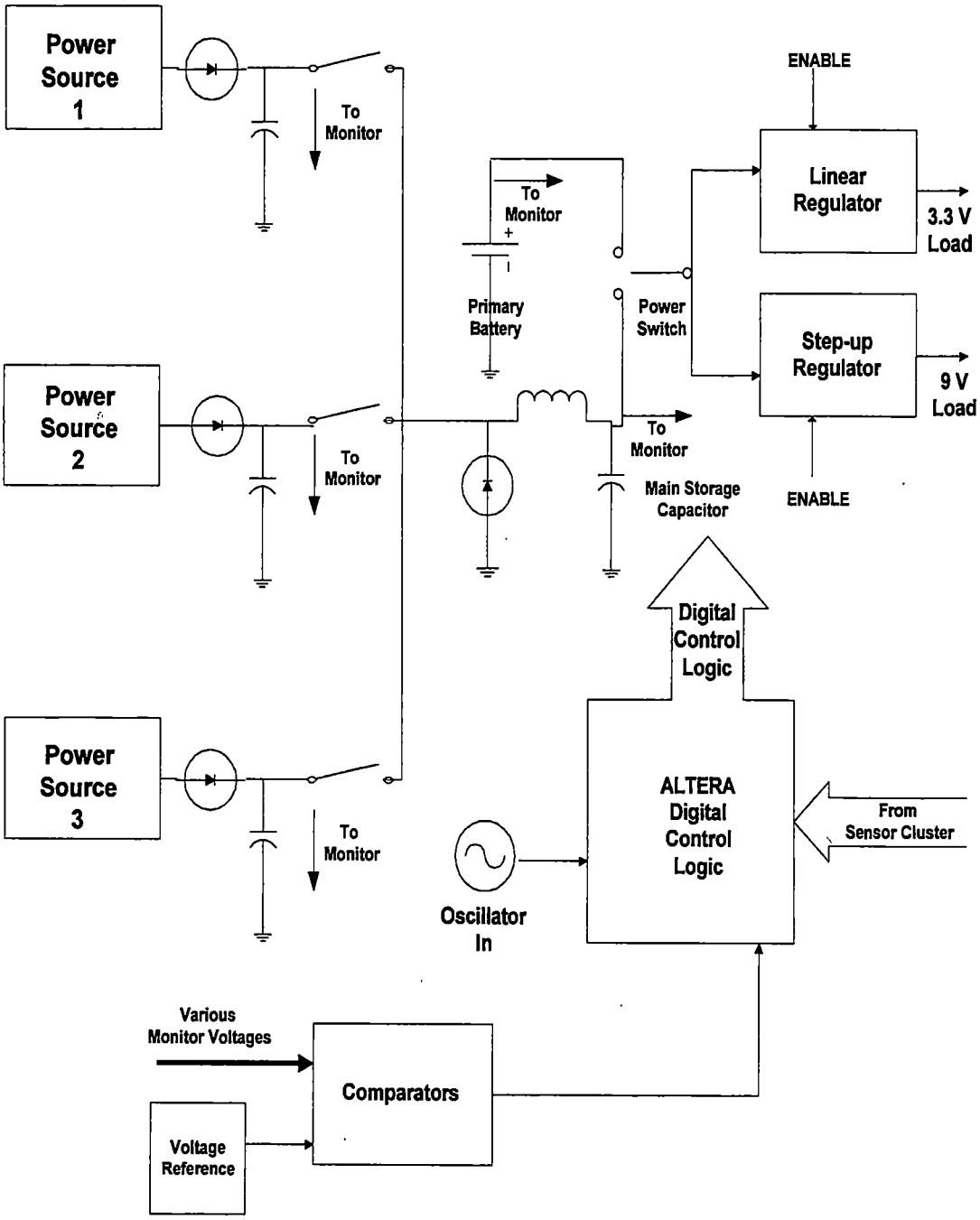


Figure 2.6 System Diagram.

The part can then send a signal to the power switch to toggle to the battery to accommodate this current load.

The comparators, which monitor the voltage levels in the system, also send their output signals to the programmable part. From these output signals, the part determines whether or not to start the Buck regulator and which supply to toggle for the linear regulator. In the next generation design, the digital logic will be implemented via low power standard cells in the ASIC itself.

Both step-up regulator and oscillator are off-chip components that are commercially available. Several types were purchased for RSVP, to compare the efficiencies of each. The step-up regulator is currently configured for 9 volts, but additional voltage options are available.

2.3.1 Converter Control

At the heart of the power control module is the DC-to-DC converter and its monitoring system. Figure 2.7 is a simplified diagram for the converter monitoring

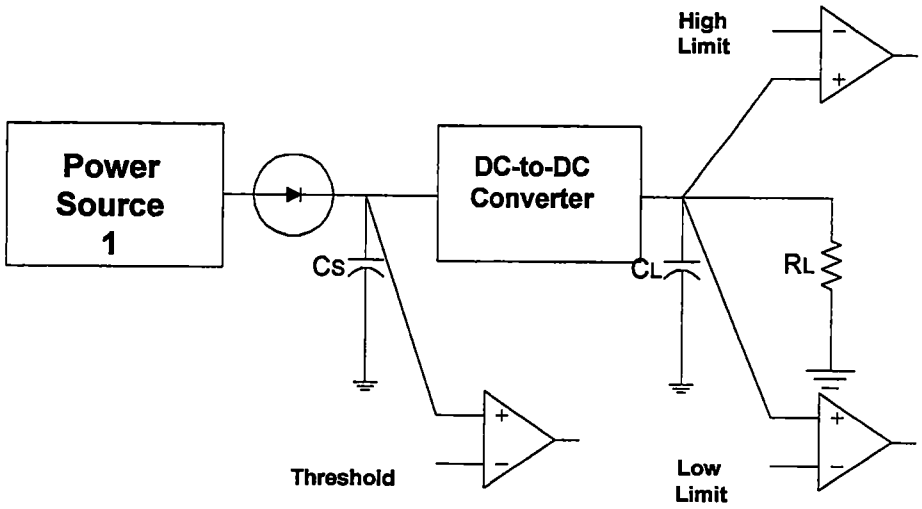


Figure 2.7 Converter and Monitors.

system. Each of the three possible input sources, including the photovoltaic array, is connected through a Schottky diode into a large filter capacitor. The capacitor, 10,000 μF, is used as a storage device for the input sources. Any available energy from the scavenging sources will charge the capacitors to provide a source for the Buck converter. The Schottky diode prevents the flow of current from the capacitor and converter back into the power source.

There are three comparators used for the monitoring system for controlling the conversion process. The first comparator monitors the input source capacitor. When this voltage has surpassed the threshold limit, the comparator notifies the ALTERA part. This threshold limit is the minimum voltage needed to start conversion. Since components are not ideal, there will be some losses. This voltage level needs to be high enough to accommodate these losses and the minimum voltage required for proper linear regulation.

A second comparator monitors the load capacitor of the converter, checking for a low limit. This low limit is the minimum voltage required by the linear regulator to maintain proper regulation. When this limit has been surpassed, a signal is sent to the ALTERA part, which then instructs the power switch to change connections from the battery to the filter capacitor. This comparator has no effect on whether or not conversion will take place.

The final comparator in Figure 2.7 is also monitoring the load capacitor. This device is comparing the load voltage to a high limit. This limit is the maximum allowable voltage at the converter output. Since a N-well process was used, compensation is required for the substrate diodes. Since the battery supply is 4.5 volts, this is the highest potential in the ASIC, and the PMOS transistor substrates are tied to this potential. If the

load capacitor voltage should rise above the battery supply, then there arises a potential for leakage to occur from the capacitor through the power switch substrate diodes into the battery. This would cause permanent circuit damage and the ASIC would become inoperable.

An example of a timing diagram for the monitoring system can be found in Figure 2.8. First, it is assumed that some arbitrary input source, perhaps the photovoltaic array, is charging the input capacitor. As seen in Figure 2.8, the voltage slowly increases to some steady state value in plot A. Plot B shows the comparator control signals. At initial startup, the comparators are cycled on and off at a fixed rate, 2 kHz, for example.

In Figure 2.8c, when the source voltage has reached the threshold and comparator is powered on, a high signal is established. The ALTERA part reads this signal and ANDs it with the high limit signal, found in Figure 2.8g. Since the high limit has not been reached, the digital logic sends the clock signal to the Buck converter, as shown in Figure 2.8f. With the Buck converter receiving its clock signal, it begins converting the voltage from the source capacitor. Figure 2.8d shows the increase in the load capacitor voltage.

When the load voltage reaches the minimum limit and the comparator fires, a high signal, which signifies that the low limit has been reached, is sent to the digital part. This signal now notifies the logic that it is acceptable to switch the power switch over from the battery to the load capacitor. The converter continues to supply power until the maximum limit is reached as seen in Figure 2.8d. At this point, when the comparator fires, a low is sent to the AND-ing logic. This in turn causes the clock signal to be removed from the converter and the conversion process stops (Figure 2.8f).

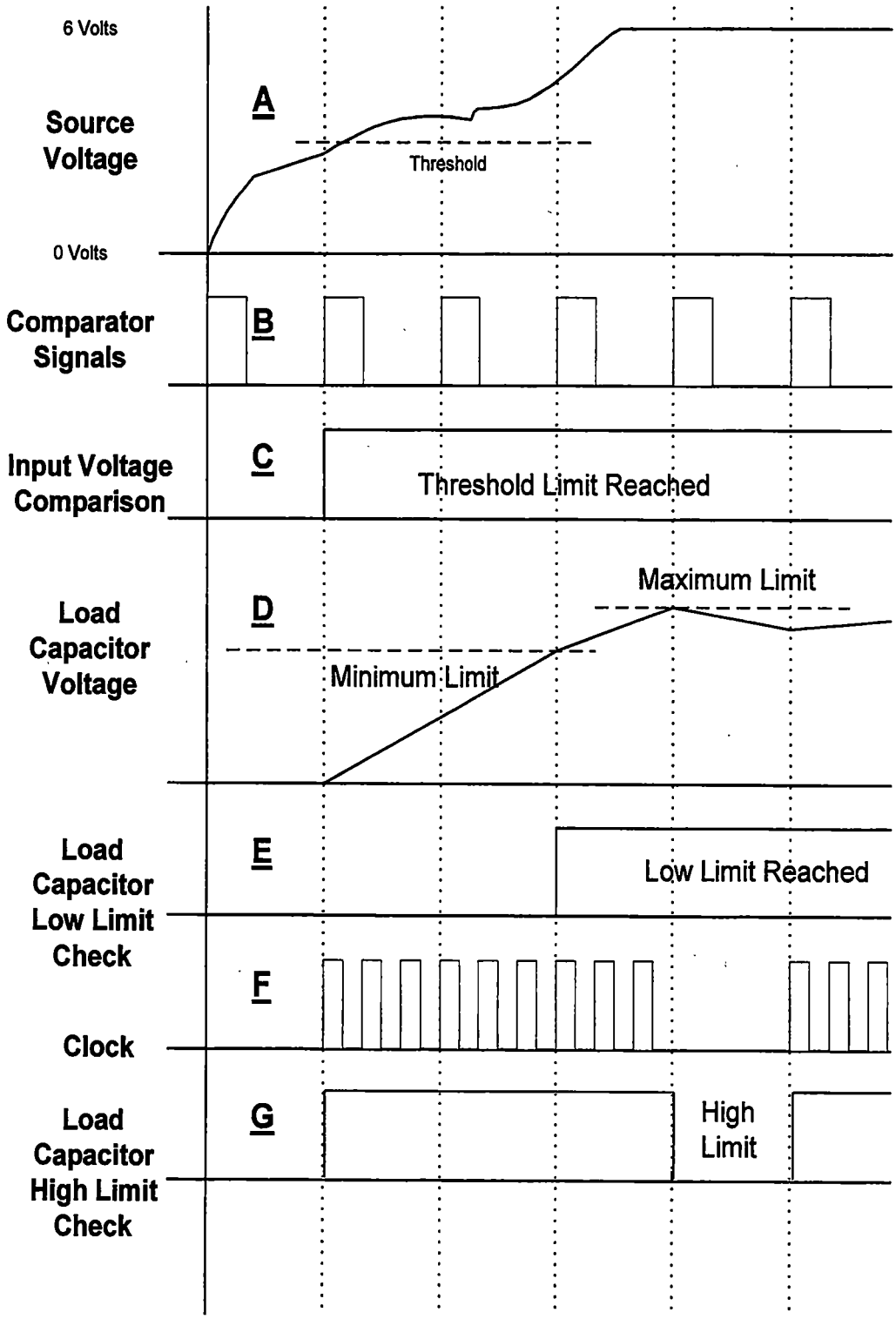


Figure 2.8 Sample Timing Diagram.

Since the load capacitor voltage decays due to the load current, the voltage will eventually fall below the maximum limit. When the comparator fires again, it passes a high signal to the AND-ing logic and the conversion process will start up again. As long as the threshold and maximum limit criteria have been met, the DC-to-DC conversion process will take place.

In typical applications of switched mode converters, the process of controlling the output voltage is performed with varying the duty cycle of the switch. By changing the D from Equation 2.11, the output voltage is changed. Varying the duty cycle does take some extra components. First, a ramp signal must be generated, which is formed from the oscillator signal. Next, a comparator and sampling resistors are used to sample the output and compare it to a reference. Since the input can change, there needs to be a sampling scheme for it also. This additional circuitry will allow a more accurate regulation of the supply voltage, but at the cost of additional components and most importantly, power. In the method chosen for RSVP, the micropower dissipation needs are met.

2.2.2 Determining Comparator Timing

Powering the comparators on and off allows lower power dissipation in the circuit. Since every μA consumed is one less available for the sensor cluster, reducing the average current in the comparators is beneficial. Each comparator uses a few μA for biasing, and if they were cycled on and off, the average current would be in the nano-amp range. Unfortunately, the power cycle is not arbitrary and is determined by several factors.

There are two limits that are used to determine the comparator timing. These are the high limit and the battery voltage. Due to the N-well process and the parasitic substrate diodes, the load capacitor supply must never surpass the battery voltage. The high limit is the maximum point the Buck converter should charge to before it is disengaged. To determine the comparator power-up cycle, a worst-case scenario must be examined.

Suppose that the comparator is powered up and it reads the output voltage as 3.999 volts. In actuality, there will be some error with a non-deal comparator and the voltage reference, and this value would change. The reading of 3.999 volts would be less than the high limit of 4 volts. The comparator would output logic high to the logic to allow conversion to continue, then power-off at X_{time} later, the comparator will power up again and read the output. This new output would be greater then the high limit, but is it higher than the 4.5-volt battery voltage?

To ensure that this new voltage is less than the battery voltage, X_{time} must be determined. If the energy transferred for one switching cycle were known, taking this value and dividing it into the voltage difference between the high limit and the battery voltage would yield X_{time}. There are several assumptions that are made to aide analysis. Any losses due to the inductor, diode and switch resistances are assumed negligible. The losses due to leakage currents are disregarded as being negligibly small. The assumption, for one switching cycle, is made that both *Vin* and *Vout* remain constant. In a normal conversion process during each switching cycle the load capacitor voltage would slowly increase, therefore the amount of charge transmitted per cycle would reduce. In this case, that is being neglected and it is assumed in worst-case scenario, that the amount of charge

moved per cycle remains constant. The load R_L during conversion would also reduce the voltage at the capacitor. For this worst-case scenario analysis, we are assuming a "no-load" situation. These two factors would allow a very conservative estimate of the charge transferred and therefore add a safety factor to the comparator timing.

The amount of voltage change per cycle is fined by Equation 2.29, which is the integral of current (ΔQ) across the inductor conduction time divided by the capacitance.

$$\Delta V_{per_cycle} = \frac{1}{C}\int_{0}^{T_{OUT}+X_1} i_L(t)\cdot dt \tag{2.29}$$

Solving this integral yields Equation 2.30 that gives the ΔV_{per_cycle} in terms of the peak

$$\Delta V_{per_cycle} = \frac{1}{C}\left[\frac{i_{L\max}\cdot T_{OFF}}{2}\right] \tag{2.30}$$

current and $T_{OUT}+X_1$ the total time the inductor conducts. This is the total area under the inductor current waveform in Figure 2.5 divide by C. The time T_{OFF} is given by Equation

$$T_{OFF} = T_{ON} + \frac{L}{Vout}\cdot i_{L\max} \tag{2.31}$$

2.31. We can take (2.31) and substitute it into (2.30) to arrive at Equation 2.32 where i_{Lmax} is defined by Equation 2.2 at t = T_{ON}.

$$\Delta V_{per_cycle} = \frac{i_{L\max}^2\cdot L}{2\cdot C\cdot Vout} + \frac{i_{L\max}\cdot T_{ON}}{2\cdot C} \tag{2.32}$$

This final equation is written for the worst-case amount of charge transferred during a "no-load" situation. This equation is only valid with assumptions that were made, and in actuality the amount of charge transferred will change with each consecutive cycle. Since our biggest concern is the load capacitor voltage surpassing the battery voltage, using this worst-case scenario will provide a greater safety margin.

3.0 Design Verification via Circuit Simulation

3.1 Using HSPICE for Circuit Verification

All monolithic circuit designs should be verified in a circuit simulation program before layout, and then re-simulated during post layout. In the pre-layout stage, designs are transferred to a simulation tool that could be either schematic capture or text based, then simulated using current device models. This tool is used to verify functionality as well as fine-tune the performance of the circuit. Next, the design is transferred to layout with a software package such as MAGIC. After the layout process, the circuit is extracted then re-simulated. The extraction process allows parasitic resistances and capacitances associated with the circuit layout to be considered. The post-layout simulations allow the designer to examine issues such as speed and power consumption that may not have been accurately simulated during pre-layout analysis.

For the RSVP project, AVANTI's HSPICE version 98.2 was used for pre-layout and post layout simulations. First, individual components were entered in HSPICE, and then analyzed separately. Next, individual components were grouped with ideal components to form sub circuits and tested for functionality. Once that functionality was verified, the designed components that were to be used in the final design were grouped together and simulated. After these simulations were evaluated and revisions made, layout in MAGIC version 6.0 was performed. After layout, circuits were extracted and post-layout simulations were performed.

3.1.1 Buck Converter Simulations

The first step for the converter design was performing an ideal simulation. All components were considered ideal, with no parasitic resistances or capacitances. The general functionality of the converter was verified. As previously discussed, a 1 mH inductor, Schottky diode and 20,000 μF capacitor were chosen. A 10-k load resistor was used to simulate the average load current of 330 micro-amps. A capacitor and load resistor forms a RC time constant. For purposes of attaining a decreased solution time, a smaller load capacitor value was used in several simulations. This capacitor size does not interfere in the calculations of general operation, but its size does play a role when testing for the movement of charge. Using initial voltages on the capacitors also decreased the simulation time.

For the inductor, a parasitic resistance of 15 ohms was estimated. This value was greater than typical values for standard industrial components, which allows for a larger error margin in HSPICE. A Schottky diode, with a forward voltage of 0.34 volts was used. This device was readily available, inexpensive, and met the design criteria for the first generation design. A SPICE model was available and downloaded.

The real switch in the RSVP project should be assigned some series resistance. As a goal, the voltage across the switch due to its resistance was to be less than 250 mV for maximum current. Since increasing the gate width of a CMOS switch would reduce the resistance, the switch was designed to be 6,000/3.5 microns. Using a typical load current maximum of 16 mA, a 10k load resistor, and an input signal of 4 volts, the switch voltage drop is approximately 190 mV.

Figure 3.1 is a plot of the voltage drop across the load resistor, as the load current is ramped up to 16 mA. The resistance of the switch was calculated to be approximately 11.9 ohms. The switch was laid out in MAGIC, using poly2 transistors. As referred to earlier in chapter two, the poly2 transistors provide the higher voltage limits required. Next, the switch was extracted and again verified.

A simulation involving the extracted switch and ideal comparators was performed. An "E" element, otherwise known as a voltage-controlled voltage source in HSPICE was used for an ideal comparator. This element allows the user to define upper and lower limits and what the output response should be if one of these limits is reached. Using these elements and the extracted switch, simulation to verify general operation was performed.

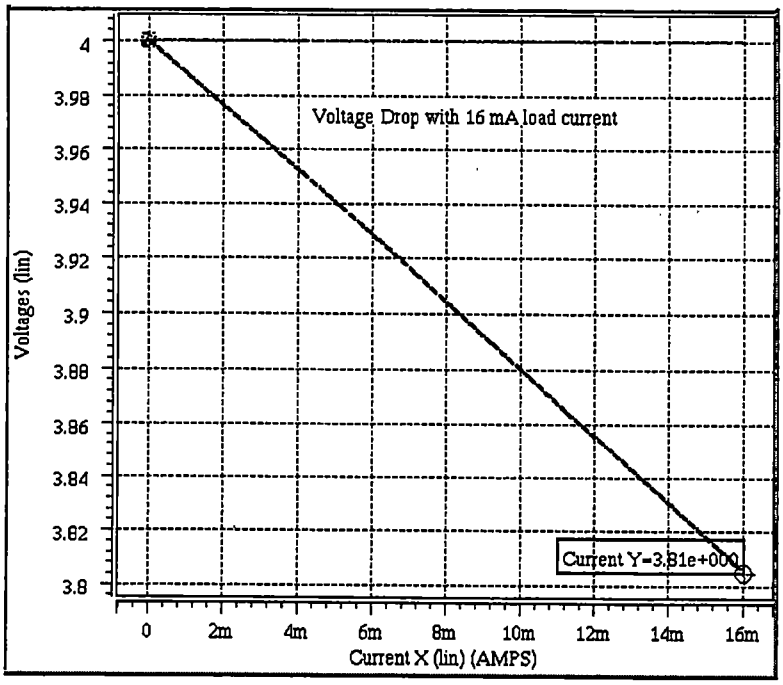


Figure 3.1 Buck Converter Load Resistor Voltage Drop Vs. Current.

First, there is an initial voltage placed on the input and output capacitors. This initial charge yields a decreased solution time, yet the general operation of the circuit is undisturbed. Next, the input is fed with a ramped supply voltage. This idea of a supply voltage slowly rising, settling out, then decaying, was used to test the threshold and high limits of the comparator. In actual operation, a source may settle out to a steady state voltage.

As the input supply is ramped up, the input capacitor will charge. When the capacitor voltage surpasses the threshold limit, the ideal comparator on the input will output logic one. If the output voltage is less than the high limit, then its comparator will also output logic one. Both inputs are passed through an AND gate whose output response is the input of a second AND gate. The second input to this gate is the oscillator signal of 32.768 kHz. When both comparators yield the logic one, or "okay" signal, the oscillator clock is transmitted to the Buck converter.

As seen in Figure 3.2 there was an initial charge on the load capacitor. While the converter is in the "off" state, the load resistor decreases the output voltage. Meanwhile,

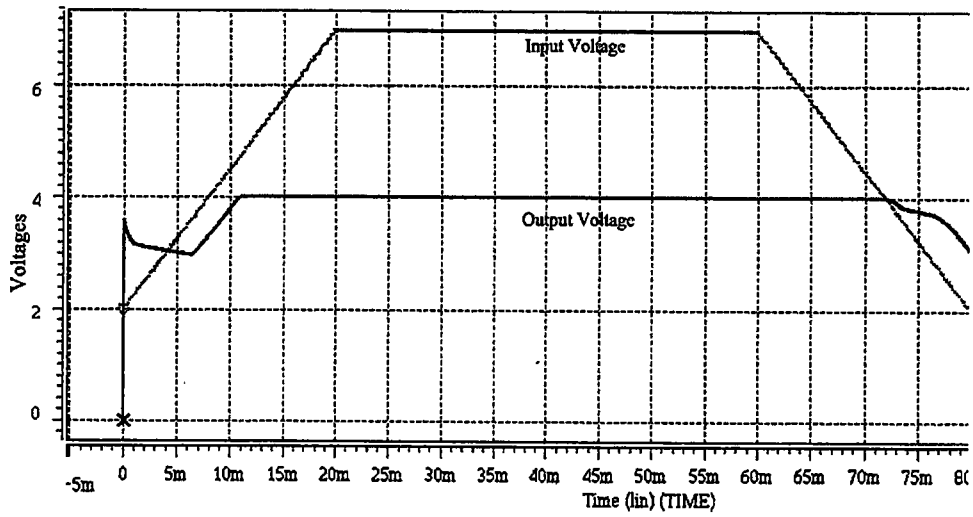


Figure 3.2 General Operation Using Ideal Comparators.

the voltage of the input source (top line) has increased above the threshold limit, which for simulation purposes is set at 3.6 volts. Since the output on the load capacitor is lower than the high limit of four volts, the clock signal is passed to the converter. As seen in the figure, the load capacitor voltage slowly increases until the high limit is reached. As required, the clock signal is removed from the converter and operation stops. Since the comparator was always on in this simulation, it held the voltage at the high limit. In the actual application the comparators will be enabled at intervals. When the input voltage drops below the threshold limit, the clock is removed from the converter, and the output decays as seen in the figure.

In the next simulation, Figure 3.3, the ideal comparators are replaced with the designed micro-amp biased comparators. The same general operation was verified. Next, some standard cell flip-flops were added to the circuit. These flip-flops will hold the comparator signal, when the comparator is off. An AND gate is placed in series with the clock input of the flip-flop. By AND-ing the clock signal with the comparator enable line, the flip-flop will hold the output after the comparator fires and hold it until the

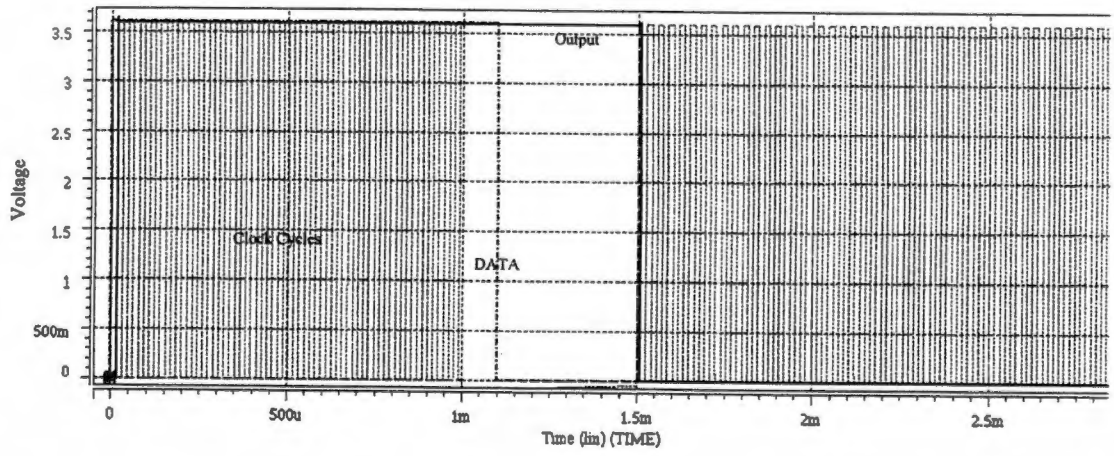


Figure 3.3 RSVP Flip-Flop Operation.

comparator is enabled once more. The clock signal is shown in Figure 3.3 by a dotted line. The clock, which was being transmitted to the flip-flop, is removed after 1 millisecond. The output, represented by a solid line, holds the data value of the 3.6 volts. Suddenly, the data changes to a low,(dashed-dot line) but since there is no applied clock signal to the flip-flop it continues to maintain the 3.6 volts. When the clock signal is once again applied to the flip-flop, it now reads the new data, which is a low, so it outputs a low. Using this technique, the Buck converter voltage can be adjusted and low power consumption maintained.

The next simulation involved using the extracted flip-flop and ideal comparators to verify general operation (Figure 3.4). A comparator power-up interval of 4 ms was arbitrarily chosen and is represented with vertical pulses. Again an initial voltage was placed on both the input and output capacitors for ease of simulation. The solid line is a plot of the load capacitor (200μF) voltage. First, the voltage is falling due to the load resistor. Next, the comparator is powered up as seen by the first pulse. The determination is made that the input source (constant 5 volts, not shown) is greater than the threshold

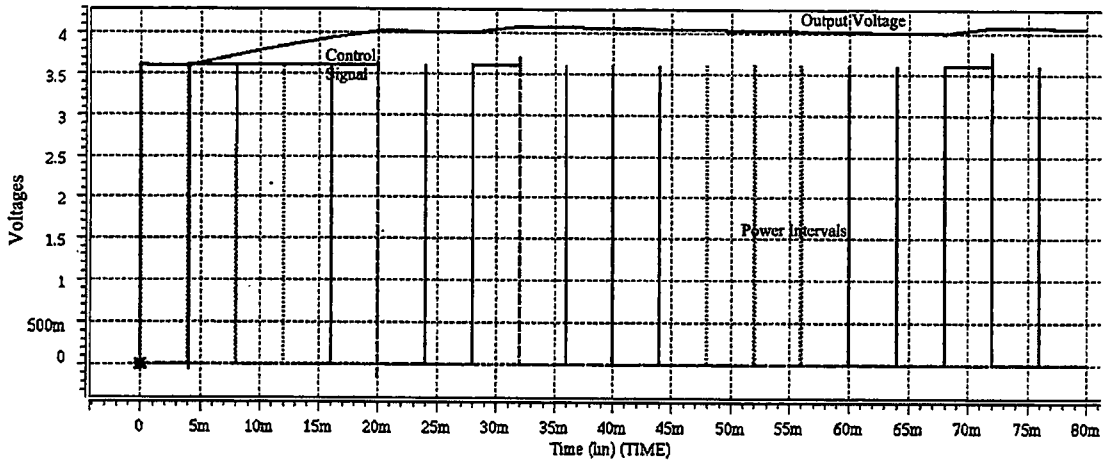


Figure 3.4 Full Simulation with Ideal Comparators.

limit. Since the output is also less than the high limit, its comparator outputs logic one. An AND-ed combination of both comparator outputs, the control signal, goes high. Dash-dot lines in the figure represent the control signal. This control signal is AND-ed with the oscillator signal that is sent to the converter. The conversion process begins and the output voltage slowly increases.

At each 4 ms interval, the comparators are powered up again and the control signal is updated. When the load voltage reaches the high limit and the comparator fires, the control signal goes low. In Figure 3.4, the control signal goes low and conversion stops, and then the load resistor causes the output voltage to decay below the high limit. When the comparator fires again, the control signal goes high. Due to the small capacitor and the frequency of the comparator power-ups, there is quite a bit of ripple on the converter output. As was discussed in section 2.2.2, if the comparator fires and the load voltage is just below the high limit, the control signal may remain high until the comparator fires again.

Next, the ideal comparator was replaced with the designed one. Figure 3.5 is the

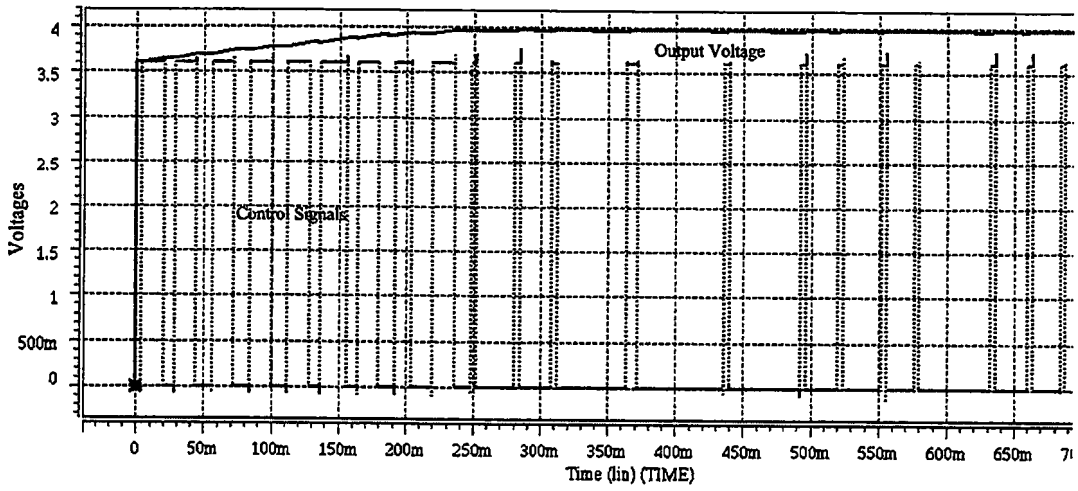


Figure 3.5 Full Simulation with Designed Comparators.

final simulation performed for general operation. This time a 2000 μF load capacitor was used to demonstrate the voltage ripple.

3.1.2 Verification of Discontinuous Mode Operation

To justify the theoretical analysis, it is necessary to show that discontinuous mode operation is valid at the different load capacitances. If this can be shown in HSPICE, then it can be argued that the capacitor size is a scaling factor when determining the charge per cycle. *Vout* is regulated to 3.6 volts with a *Vin* equivalent to 5 volts. A 10k load used for all cases simulated the average current requirement. First, a simulation using a 20 μF capacitor was performed. In Figure 3.6, the dark line represents the load current through the inductor. The dotted line represents each cycle of the clock. As seen the plot correlates with theory and during the first half of the cycle when the switch is closed the current ramps up to a maximum (around 14 mA). During the second half, the current decays to zero. The inductor current is zero until the start of the next cycle. Figure 3.7 contains three plots, a, b, and c of which are representative of the inductor current for the capacitance values of 200 μF, 2000 μF and 20,000 μF.

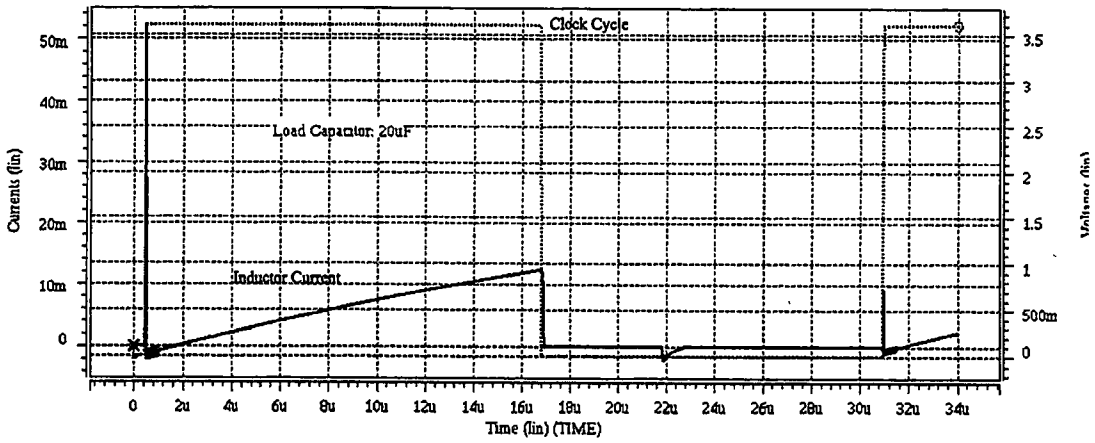
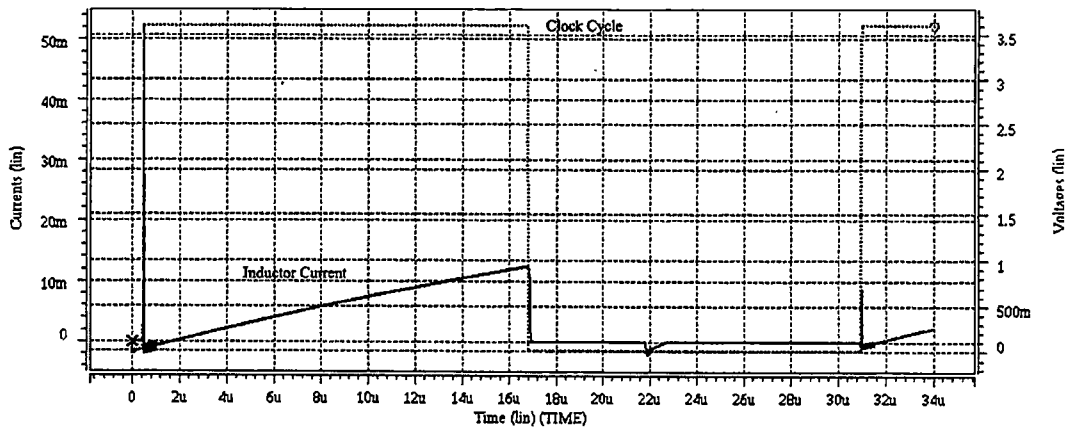
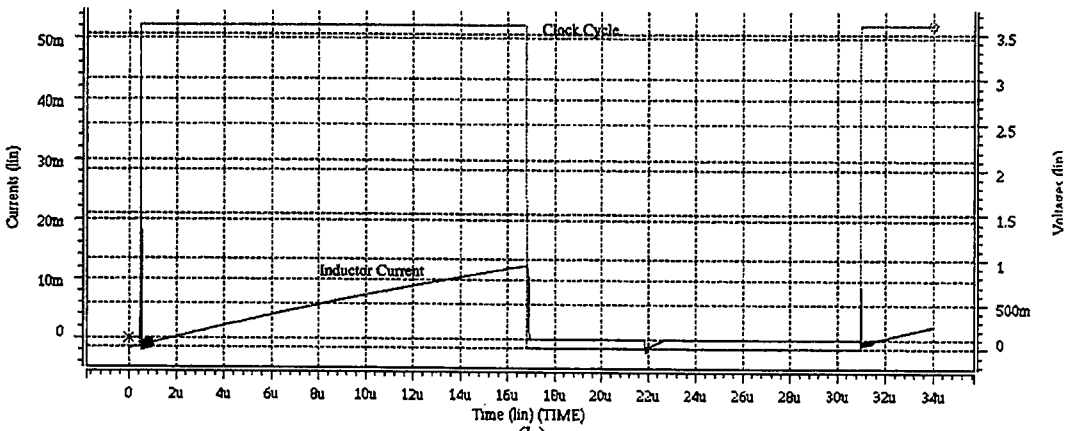


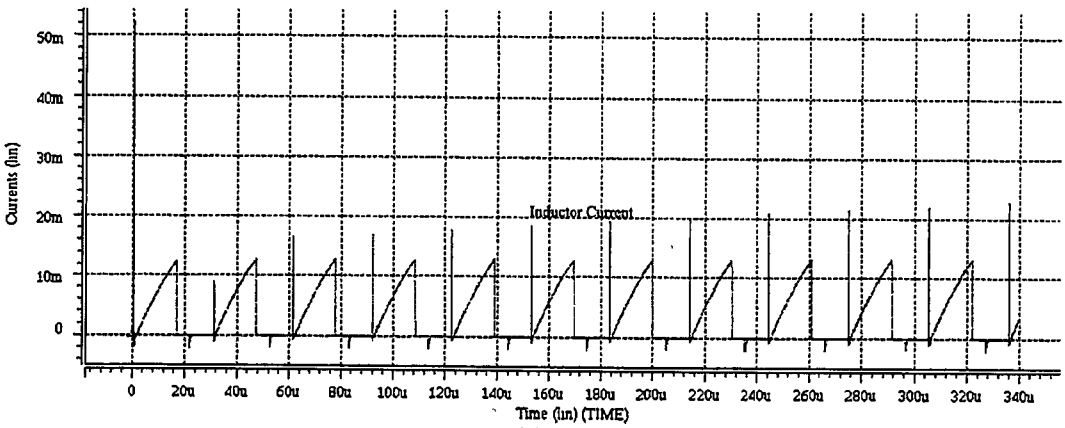
Figure 3.6 Inductor Current with a 20 μF Load Capacitor.



(a)



(b)



(c)

Figure 3.7 Inductor Current Plots.
(a) 200 μF, (b) 2,000 μF (c) 20,000 μF

In Figure 3.7c, several clock cycles are shown. As seen in all plots, the inductor current ramps up during the first half cycle and decays before the end of the second cycle. This is theoretically consistent with a Buck converter working in the discontinuous mode. Unlike the figures in chapter 2, the decay period during $T_{ON} < t < T_{OFF}$, the current decays quickly and is almost unnoticeable.

3.2 Movement of Charge

Comparator timing depends on the amount of charge that can be passed during one clock cycle. A theoretical analysis was performed in Chapter 2, based on the theory that the converter is operating in discontinuous mode. In section 3.1.2, HSPICE showed that even at smaller capacitor levels, with all other elements constant, the circuit did work in this mode of operation. HSPICE was next used to measure the movement of charge during one cycle for comparison to theoretical analysis. We assumed in the theoretical analysis that we were dealing with a "no-load" situation, so it is expected that HSPICE results would give a smaller voltage change in the given time period.

3.2.1 HSPICE Charge Measurements

To simulate the movement of charge, several constants were set. First, a constant input supply voltage of 5 volts was used. The input load capacitor of 10,000 μF would serve the assumption that *Vin* was held constant. This capacitor was set with the initial voltage of 5 volts to remove the RC time constant associated with charging this capacitor by the input source. The load capacitor was set with a 4 volt initial charge. Each simulation involved the input source and load capacitors, the Buck converter and a 10k

load. The load provided an I_O of 400 uA. The clock signal was applied directly to the switch. Since we are interested in the worst-case voltage change after the load capacitor reaches 4 volts, only the first switch cycle is examined.

The first simulation involved the load capacitor being set to 20 μF. Figure 3.8 shows how the voltage on the load capacitor is increasing. After one clock cycle, the total voltage change is roughly 5.8 mV. For a comparison, Figure 3.9 contains the plots of voltage changes for the three load capacitances of 200 μF, 2,000 μF, and 20,000 μF. In Figure 3.9a, the voltage increases by 0.58 mV. This change is a factor of 10 less than Figure 3.8, which has a capacitor 10 times smaller. In Figures 3.9b and c, the voltage increases by 57.7 μV and 5.72 μV respectively. Each of these values is also a factor of 10 less than the previous simulation that used a capacitor that was a factor of 10 larger. These results are similar for the four sets of values: 20 μF/200 μF/2,000 μF/20,000 μF showing that since the capacitor is in the denominator of the voltage-change- per-cycle equation, it is a scaling factor.

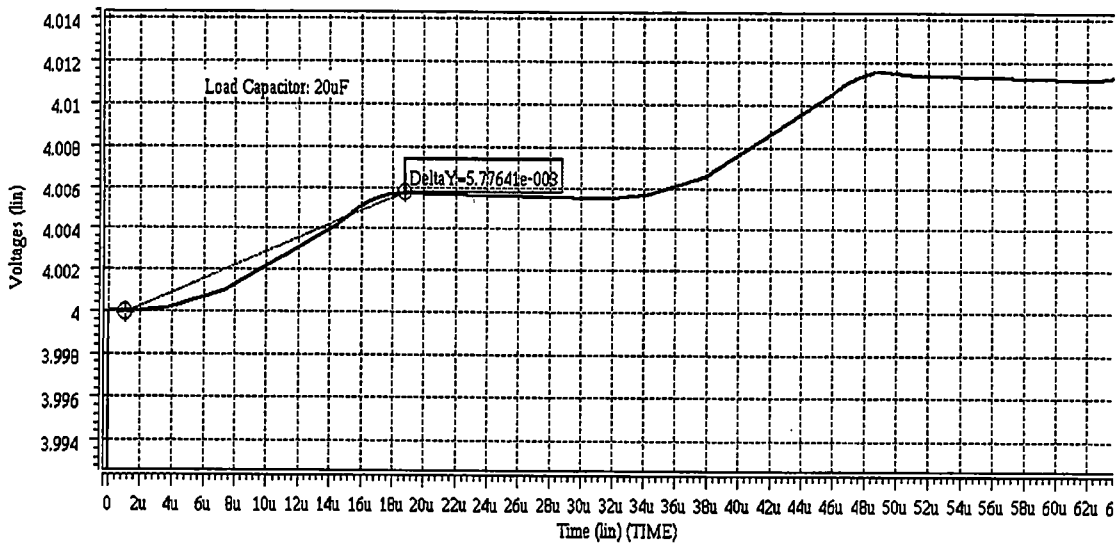
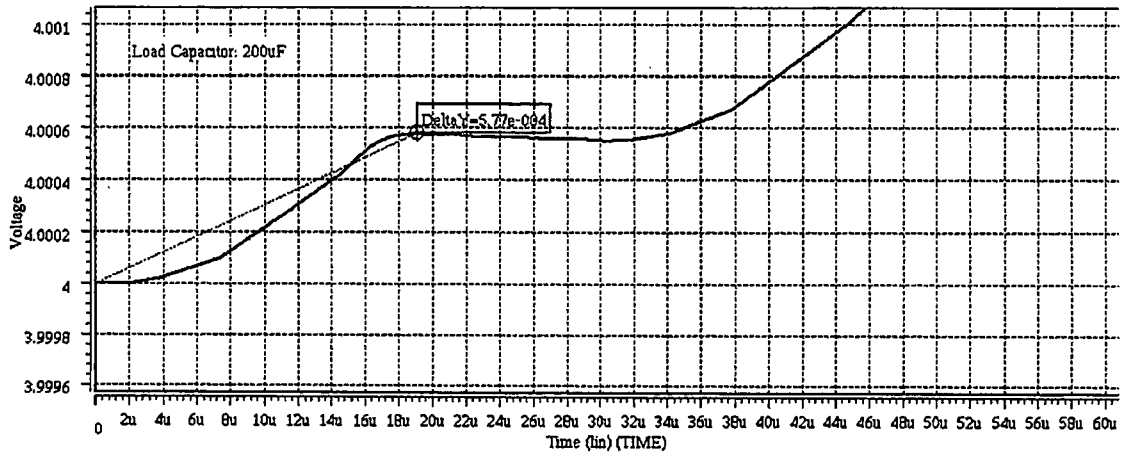
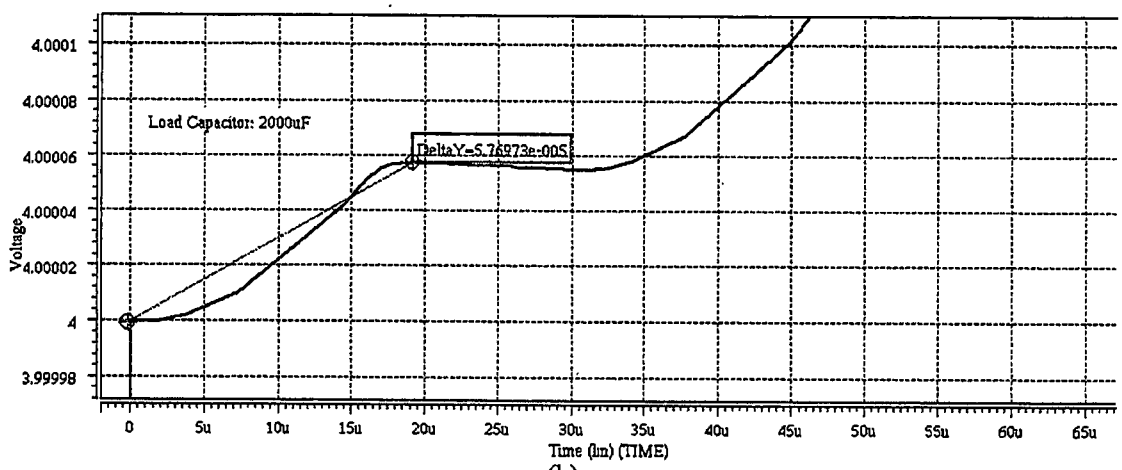


Figure 3.8 Change in Output Voltage for 20 μF.



(a)



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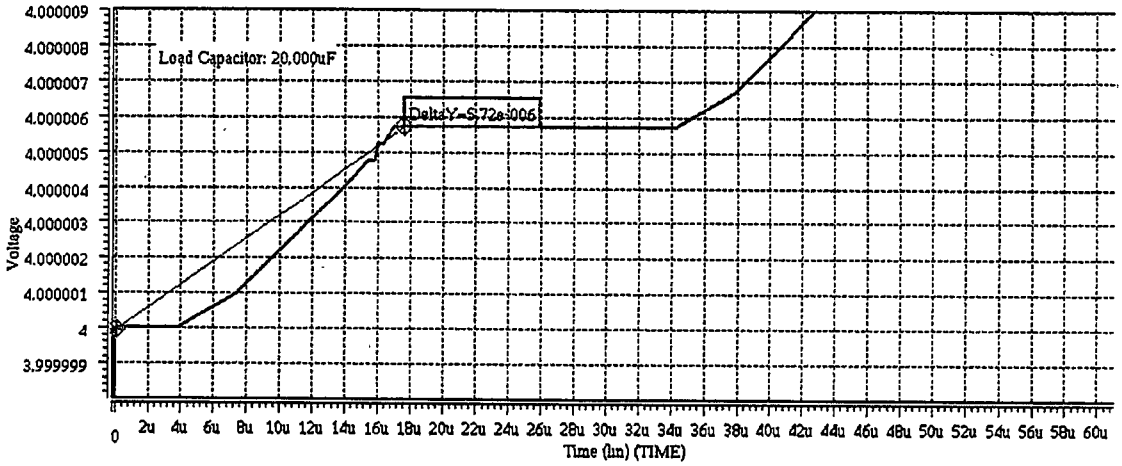


(c)

Figure 3.9 Change in Output Voltage.
(a) 200 μF, (b) 2,000 μF, (c) 20,000 μF

3.2.2 Comparison of Theoretical and Simulations Values

For a comparative discussion, the data below represents theoretical calculations versus HSPICE simulation results. For all four cases the percent difference from theoretical values is 20%. These are acceptable results. The theoretical analysis assumed a worst-case scenario with a "no-load" situation and factors such as ohmic resistances and leakage currents were not considered.

Comparisons of Voltage Changes for Vin=5 volts, Vout=4 volts, I_O=400uA.

Capacitance	Theoretical	HSPICE
20 uF	7.27 mV	5.77 mV
200 uF	.727 mV	577 uV
2,000 uF	72.7 uV	57.7 uV
20,000 uF	7.27 uV	5.72 uV

Simulations showed that regardless of the capacitor value, the circuit operated in the discontinuous mode. What can be concluded is, that the assumption of *Vout* and *Vin* remaining relatively constant during one clock cycle, for the simulation is reasonably valid for all cases of capacitance. The capacitor value that is in the denominator of Equation 2.41, acts as a scaling factor for determining the total voltage change per cycle.

$$\Delta V_{per_cycle} \approx \frac{L \cdot i_{L\max}{}^{2} \cdot}{2 \cdot C \cdot Vout} + \frac{Vin - Vout}{2 \cdot L \cdot C} \cdot T_{ON}^{2} \qquad (2.32)$$

Therefore in the design, the larger capacitor size also limits the amount of voltage that can be moved in one cycle.

3.3 Circuit Layout

Before performing any circuit layout, a preliminary sketch may prove beneficial to the designer. There are several factors that must be considered before layout. After the design process has been chosen, the chip package must be selected. The chip package size will determine the number of pins available on the package. Often, the four corner pins are automatically lost due to power and ground connections required by the many ASIC protection circuits.

The process will also define the type of materials that can be used in the layout. For example, in AMI's 1.2-micron process, two metals and two polysilicon layers are available. This allows more interconnects within the ASIC. The process will also dictate what minimum gate lengths should be specified; for AMI 1.2 micron Lambda is defined as 0.6 microns. For a minimum gate length of 1.2 microns, the required Lambda is two.

3.3.1 Poly2 Transistors

In order to achieve such high voltages for the RSVP power module ASIC, the use of AMI's 1.2-micron process and poly2 transistors are required. The use of poly2 transistors with a minimum gate length of 3.5 microns allows a voltage range from 2.5 to 11 volts. These transistors were used in the DC-to-DC converter switches where the source voltage may exceed 5 volts. Currently, there are no SPICE models available for poly2 transistors. The latest process information is available in the Appendix, page 86.

3.3.2 Layout Restrictions

One of the problems encountered in the RSVP ASIC design was dealing with the parasitic substrate diodes. In a dual well process, each well can be biased separately, and these diodes can be kept reversed biased. In the single N-well process, the substrate is at one potential, ground. The input sources can vary up to ten volts, yet the battery voltage is only 4.5 volts. The voltage at the input may be less than this voltage, so the question arises as to what rail to tie the chip guard ring to. There are several different voltage potentials in the ASIC which cause several problems.

An example of a problem caused by these different potentials occurs at the input to the converter switch. The input voltage can have a higher potential than any voltage on the ASIC, so normal protection pads could not be used. Instead, a protection circuit off the chip in the source is used to limit the voltage into the ASIC. The next problem is how to switch the converter switch. The clock needs to be high enough potential or the switch will never fully turn off. Creating a weak PMOS, strong NMOS inverter as seen in Figure 3.10, solves this problem. In the normal inverter a "low" input will turn off the NMOS

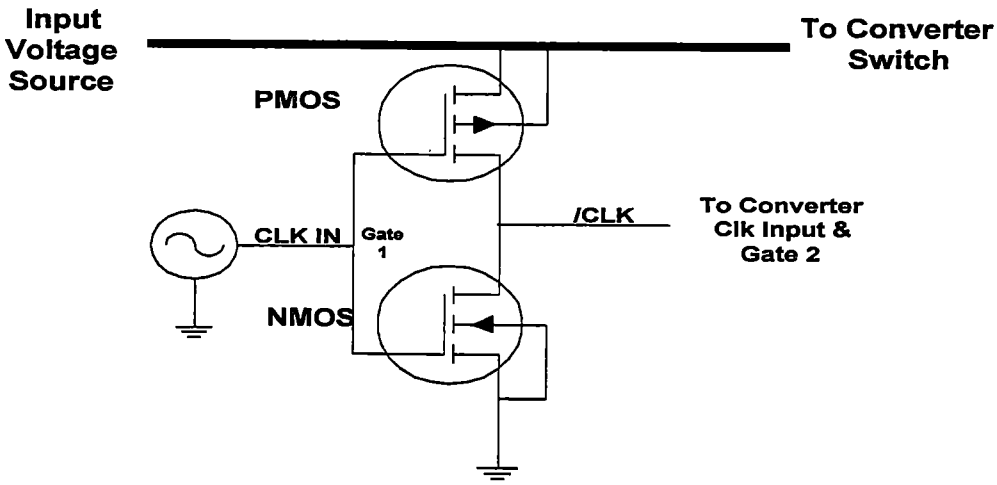


Figure 3.10 Weak PMOS inverter for the Buck Converter.

and fully turn on the PMOS, therefore a "high" appears at the output. With logic "one" at the input, the PMOS is turned off but the NMOS is turned fully on and logic zero or "low" appears at the output.

In RSVP, the input supply voltage would be higher than the clock signal of 3.3 volts. The inverter in Figure 3.10 has the PMOS source tied to the input rail. The NMOS transistor is a larger device, while in typical inverters the role is reversed. When the clock signal is a high, it fully turns on the NMOS device, which will dominate the pair, even though the PMOS transistor may not be fully off. A low will always fully shut off the NMOS and fully turn on the PMOS device.

4.0 System and Component Testing

4.1 ASIC Component Testing

There was a great advantage to separating components on two individual ASICs for the first generation of RSVP. Each component's inputs and outputs could be tied to an individual pin. This provides several test-points that will only be internal to the ASIC in the next generation design. Each component can be individually biased in order to accommodate the differences between theoretical design and processing run variations. If it were found that any of these individual components didn't work, only a small part of the ASIC is unusable. That part could be replaced with an off-chip component and the overall system functionality could be salvaged.

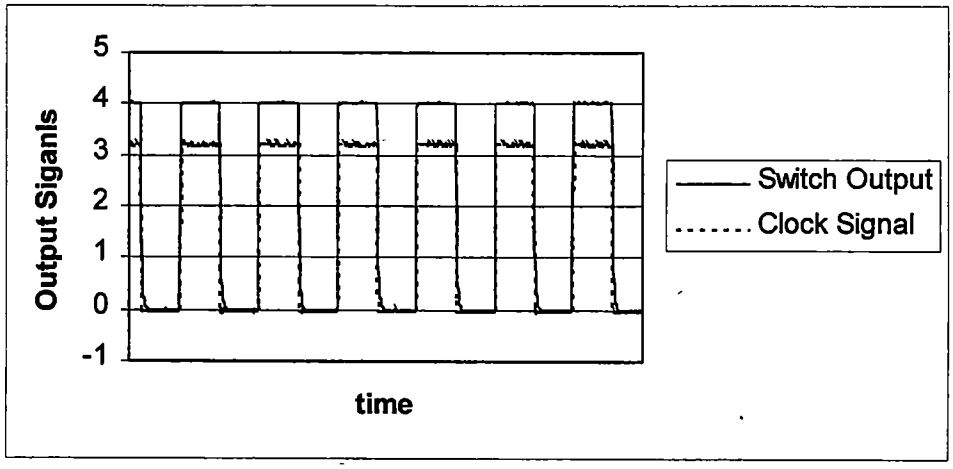
With each component having its own I/O pin, a greater depth of testing can be performed such as varying bias, changing references, etc. Having two ASICs rather than one does increase the fabrication cost, but the money is saved in time, both in terms of design and testing. For the first generation of RSVP, separating components proved cost effective. It also allowed the testing of additional components, such as 3 separate references to find out the best performance. This is very important since a voltage reference tends to vary of one processing run to the next. A good sampling of ASICs is required to validate any test, and a 50% sampling was chosen for RSVP. A total of five samples from each ASIC chip were tested, though results posted usually are from one chip. In testing the ASICs and their components, the Hewlet Packard 4156A Precision Semiconductor Analyzer was used for many of the test procedures. With this analyzer, the designer can define several inputs and outputs and functions such as *gm*.

4.1.1 Converter Switch

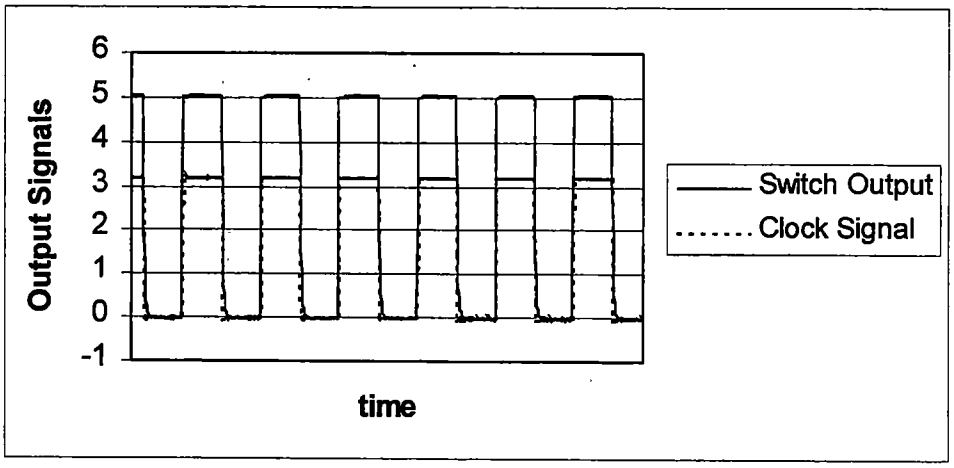
The Buck converter switch consisted of a complementary CMOS pair that is composed of an NMOS and PMOS transistor. There are two ways to design the switch either equal W/L, to give equal gate-to-source capacitance which in turn minimizes switching transients or design with mismatched W/L to give a flatter R_{ON} at the expense of more switching noise. The switch was designed to equalize capacitance, with equivalent gate widths. The parallel combination of the CMOS pair would reduce the overall switch resistance over a wide range of input and output voltages.

As discussed in Section 3.3, one of the problems encountered in RSVP is switching an input voltage that is higher than the amplitude of the clock signal. This was resolved by using a weak PMOS, strong NMOS transistor pair. By using this combination, and tying the rail of the inverter to the input supply, the 3.3-volt magnitude clock would be able to switch voltages twice its magnitude.

In Figure 4.1, tests for three different input voltages are shown in plots a, b and c. A 32.768kHz clock signal, represented in each plot by the dotted line, was applied to the switch, with a magnitude of 3.3 volts. The output of the switch was tied to a 10k-load resistor to reduce the RC time constant of the oscilloscope probes. Three supply voltages, 4 volts, 5 volts and 8 volts were used as test cases. As visible in the figure, with the use of the special transistor pair, all three input source voltages are easily switched. In testing, these sources could be switched with voltages as low as 2 volts.



(a)



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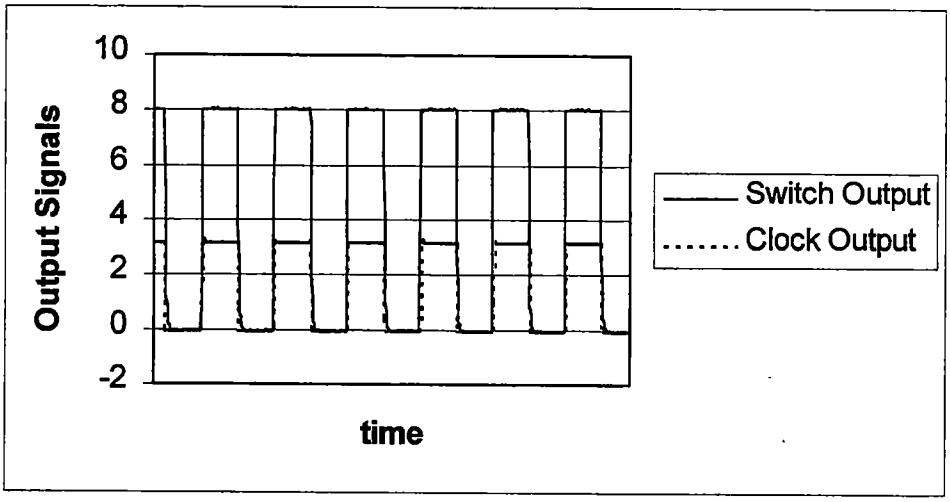


(c)

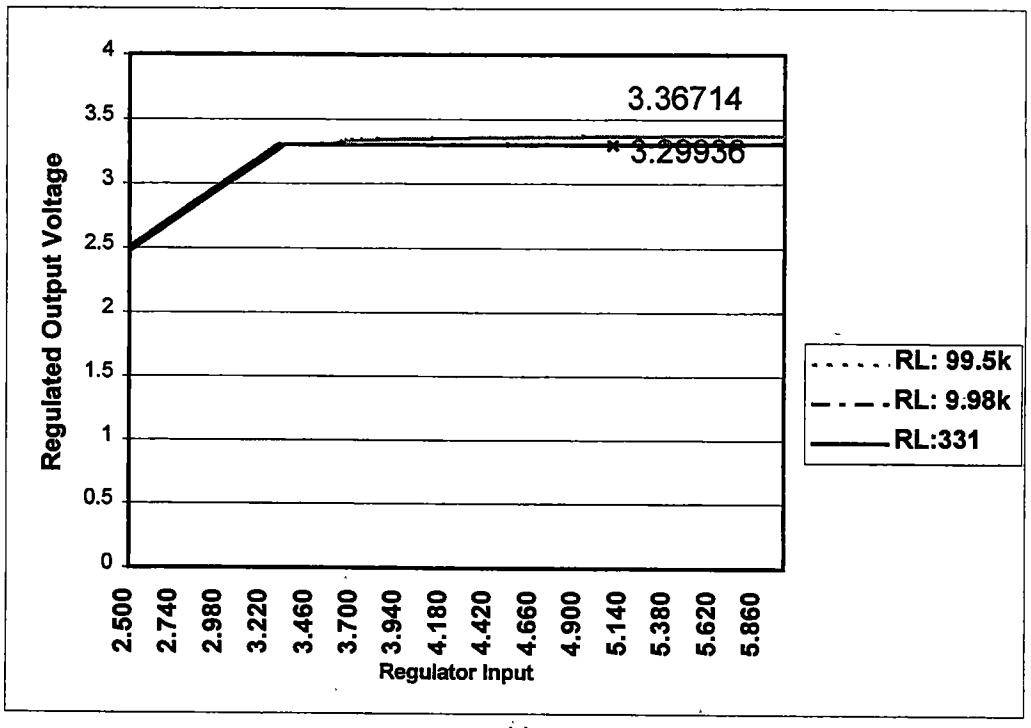
Figure 4.1 Switch Functionality Tests.
(a) 4 Volts In (b) 5 Volts In (c) 8 Volts In

4.1.2 Linear Regulator

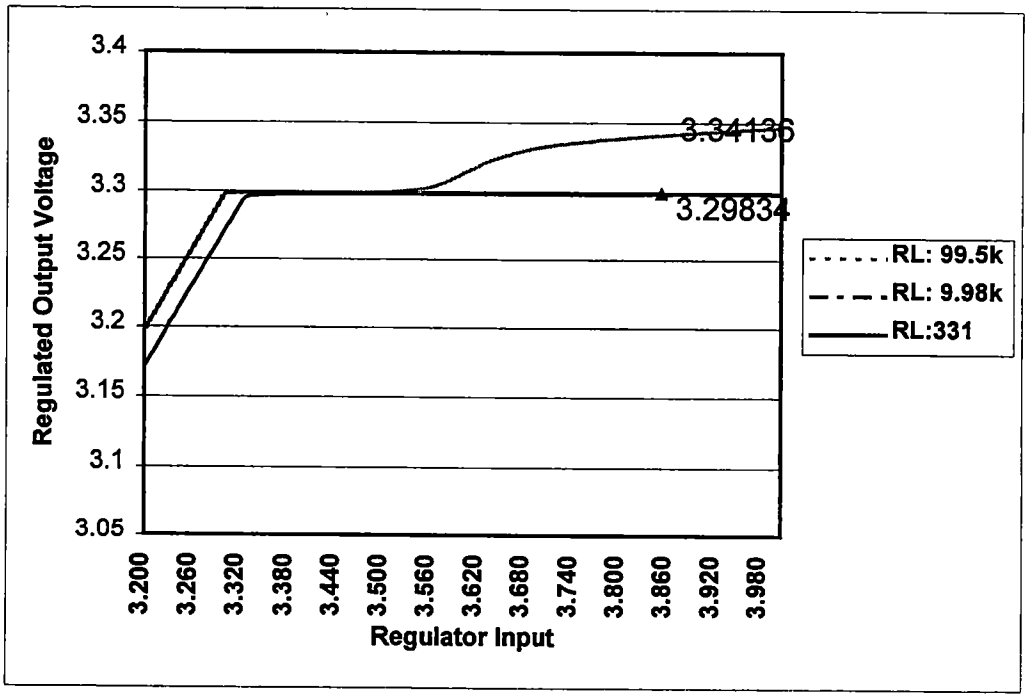
The next component tested was the linear regulator, utilizing the HP 4156A analyzer. With this tool, the input voltage was ramped up slowly in increments of 5 mV, to precisely see the transition point into regulation. Figure 4.2 contains the plots for this test. The input voltage is swept from 2.5 to 6 volts. In actual practice there will be a smaller range of input voltages, 3.6 to 4.5 volts that the regulator will be subject to due to the limiting mechanism of the comparator-monitoring scheme. Three test loads were used, 99.8k, 9.98k and 331 ohms. These load resistances were used to simulate the load currents of 33 μA, 330 μA, and 10 mA respectively, for a regulated output of 3.3 volts.

In Figure 4.2a the entire range of input voltages are shown. When the input reaches approximately 3.34 volts, regulation begins. With a load current of 10 mA, the regulated output is approximately 3.3 volts for a input of 5.1 volts. For the same input voltage, but a reduced load current of 33 μA, the output is regulated at 3.67 volts. Figure 4.3b is a zoomed in view of the regulation transition area. It can be clearly seen that when the input voltage rises above 3.5 volts, there is a tendency for the regulator to drift away from the 3.3-volt regulation with the smaller load current due to the decrease in closed loop gain.

In Figure 4.3, the same tests were performed but at a smaller resolution and voltage range. This time the input is swept from 3 volts to 4 volts with a 1-mV resolution (Figure 4.3a). Figure 4.3b expands this view about the regulation transition points, which appear to be comparable values for the different load currents. As expected, this micro-power regulator transitions into regulation when the input rises slightly above the regulated output voltage of 3.3 volts.

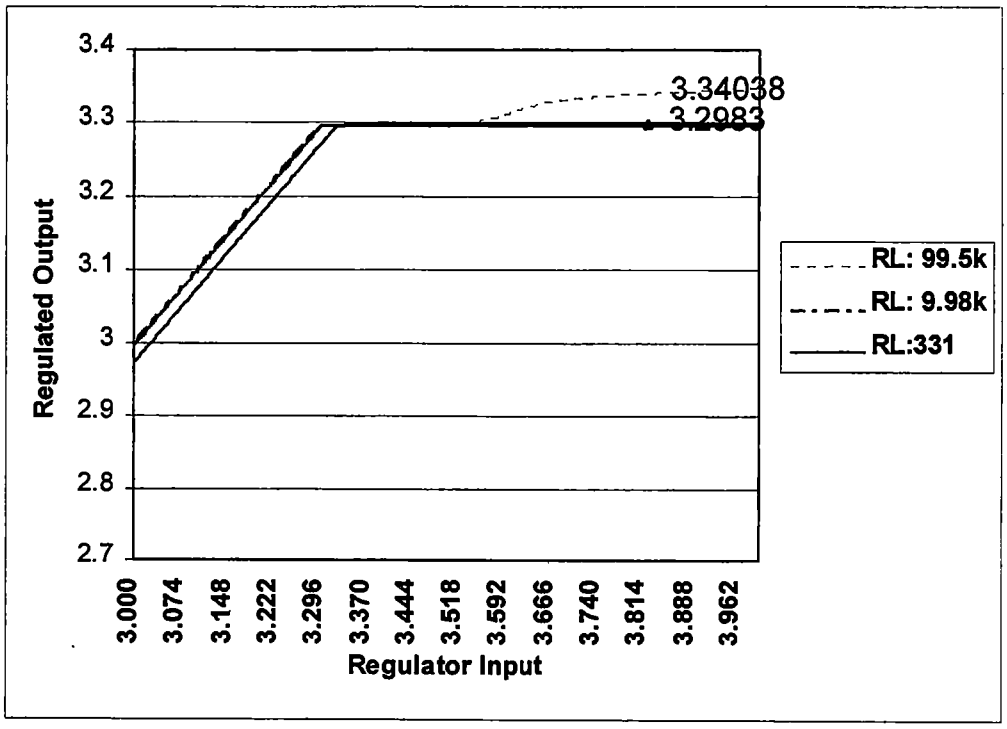


(a)

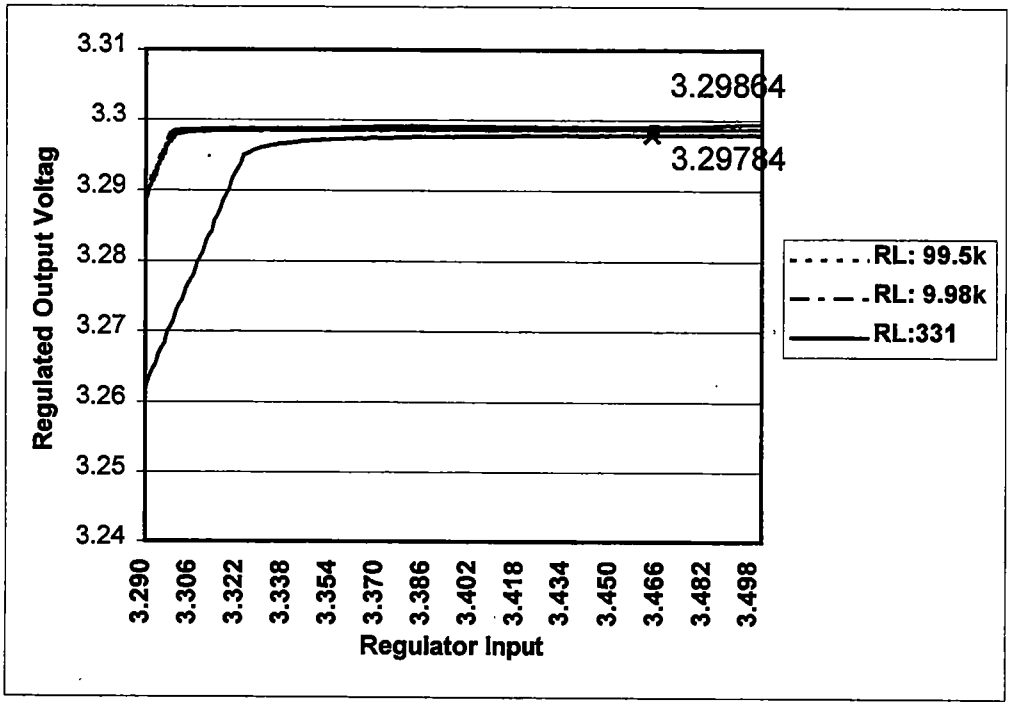


(b)

Figure 4.2 Linear Regulator Tests: 5 mV Resolution.
(a) Full View (b) Zoomed in View



(a)



(b)

Figure 4.3 Linear Regulator Tests: 1 mV Resolution.
(a) Full View (b) Zoomed in View

4.1.3 Comparator Testing

Next, the comparators were tested using the HP 4156A analyzer. In testing the comparator, besides verifying the general functionality, its switching characteristics were required. When the input surpasses its reference voltage, the comparator output will switch states. When this input decays below the reference, the comparator output will return to its original state. Since the comparator is non-ideal, these switching points will vary slightly. The input voltages to the comparators were swept with the analyzer to perform this test.

A 2 volt reference signal was applied to the inverting terminal and the non-inverting terminal input was swept from 0 to 4 volts in 5 mV increments. Figure 4.4a displays the comparator output voltage versus the applied input voltage. There is an offset of 5 mV before the comparator output switches states. The comparator is powered by 3.3 volts whereas the I/O pads are powered by 4.5 volts, hence the larger output signal. In Figure 4.4b the input voltage is swept from the other direction to test the high to low voltage transition. The comparator toggles at 2 volts.

Next, the reference voltage was applied to the non-inverting terminal and the inverting terminal input was swept from 4 to 0 volts as seen in Figure 4.3c. In this case, comparator output transitions to high, at 5 mV before the reference voltage. Again, this 5-mV offset is visible. Figure 4.4d, when the input is ramped from 0 up to 4 volts, the comparator output transitions at the 2 volt reference point. An interesting point to note is in both Figure 4.4b and 4.4d, there is a short period before the output stabilizes on the comparator, which is caused by the input voltage being greater than the supply voltage.

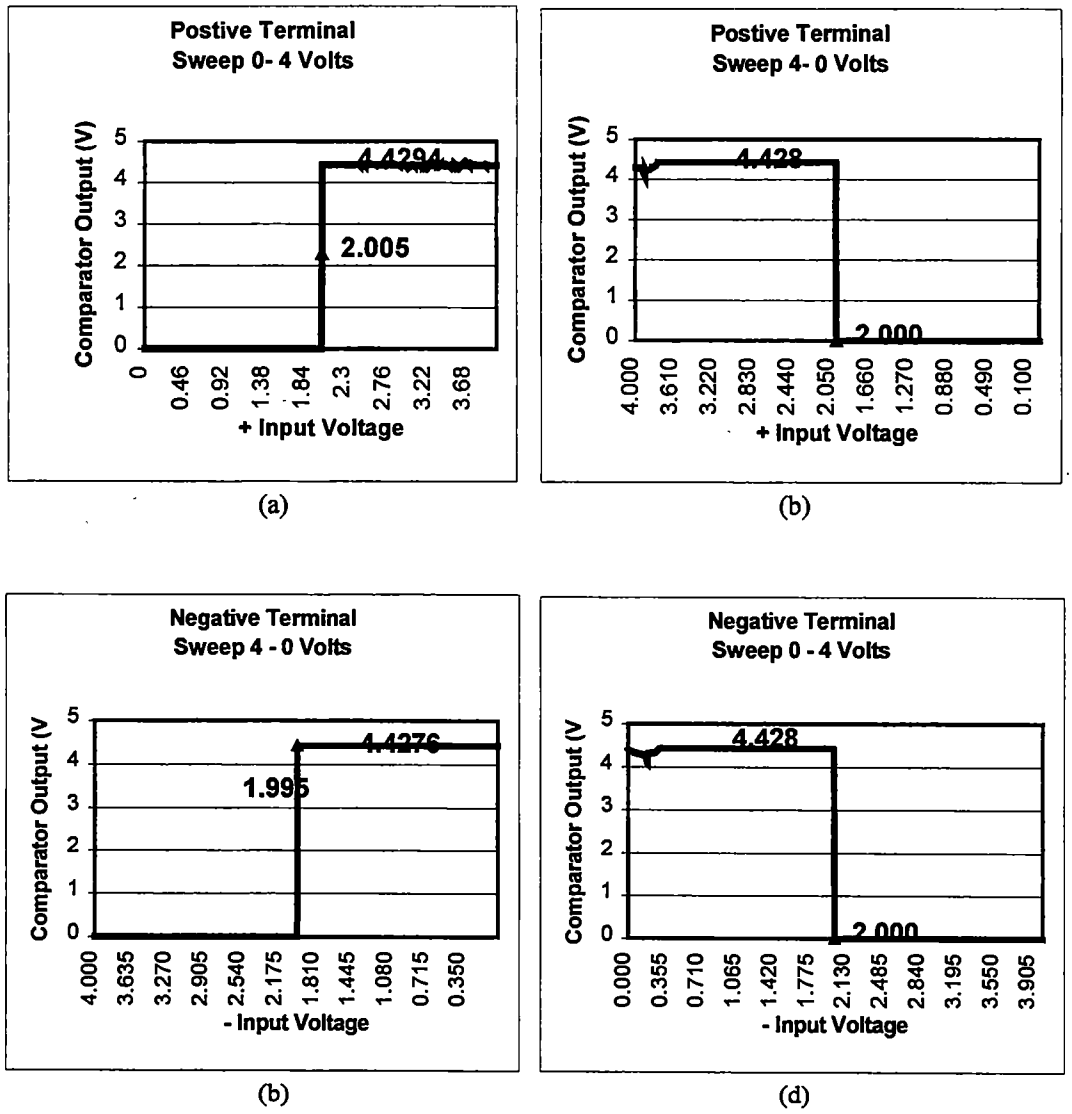


Figure 4.4 Comparator Switching Tests.

(a) Sweep of Positive Terminal 0 to 4 volts (b) Sweep of Positive Terminal 4 to 0 volts
(c) Sweep of Negative Terminal 4 to 0 volts (d) Sweep of Negative Terminal 0 to 4 volts

4.1.4 Remaining Components

The remaining components were analyzed for functionality only. First, the power switch was tested to see if it would toggle correctly between the load capacitor and battery voltage. All five chip samples worked according to design. Next, the three voltage references were tested. Parameters vary from run to run, as well as on the wafer itself, so it was to be expected that the reference voltages would have some variance. Table 4.1 is a plot of 3 different references with 5 different chip samples. Reference II is a lower powered reference and its results are of particular interest to maintain the goal of low power consumption.

Table 4.1 Voltage Reference Comparisons.

Reference:	Chip A	Chip B	Chip C	Chip D	Chip E
I	2.229	2.245	2.174	2.254	2.223
II	2.383	2.239	2.279	2.269	2.308
III	2.453	2.492	2.470	2.423	2.416

In the system configuration, the various components will be swapped in and out to examine which ones will provide a better overall system performance. Additional components have been replicated, such as an external reference and two more clock devices. Using a re-configurable test board allows the freedom to make changes to the system design without the down time of waiting for a new ASIC.

4.2 Poly2 Transistors

The usage of the poly2 transistors allowed a higher voltage than normal poly1 transistors. MOSIS does not provide an individual SPICE file listing for the poly2, but

does provide some general information such as threshold voltages and gate capacitance that are retrieved from their testing process. For some general reference, some basic testing, V_{DS} vs I_D and V_{GS} vs I_D was performed on the 6000μ / 3.5μ transistors via the HP 4156A analyzer. This has been the first time poly2 transistors have been used here at ORNL.

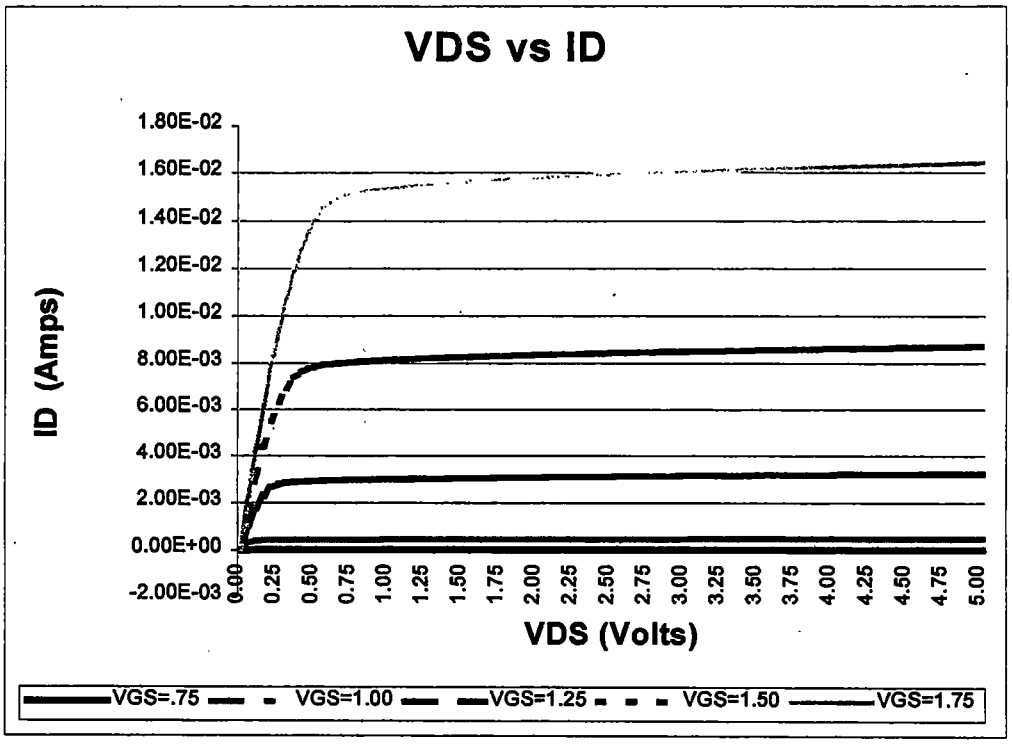
4.2.1 V_{DS} *vs* I_D

To test the NMOS device, the source was tied to ground and V_{DS} was swept from 0 to 5 volts at varying V_{GS} voltages. V_{GS} was set initially at 0.75 volts to insure the device was off, then its voltage was increased in 0.25 volt increments. Figure 4.5 contains plots for a NMOS device (a) and a PMOS device (b). For testing the PMOS device, the drain was tied to ground, and the gate is swept from 0 to 5 volts, varying V_{SG} in 0.25 volt increments starting at 1.25 volts.

From the V_{DS} *vs* I_D plots, linear regression can be performed on the curves in their saturation region to determine output resistance. Ideally in saturation I_D is independent of V_{DS}. The output resistance is defined by Equation 4.1, the inverse of the small change in

$$R_O \approx \left(\frac{\Delta id}{\Delta vds}\right)^{-1} \tag{4.1}$$

drain current over the small change in drain-to-source voltage. In an ideal transistor $\Delta\, id$, the small signal drain current, would be zero in the saturation therefore creating infinite impedance. For the case of the largest V_{GS} curve, the NMOS transistor has an R_O of approximately 5.7k and 4.4k for the PMOS device.



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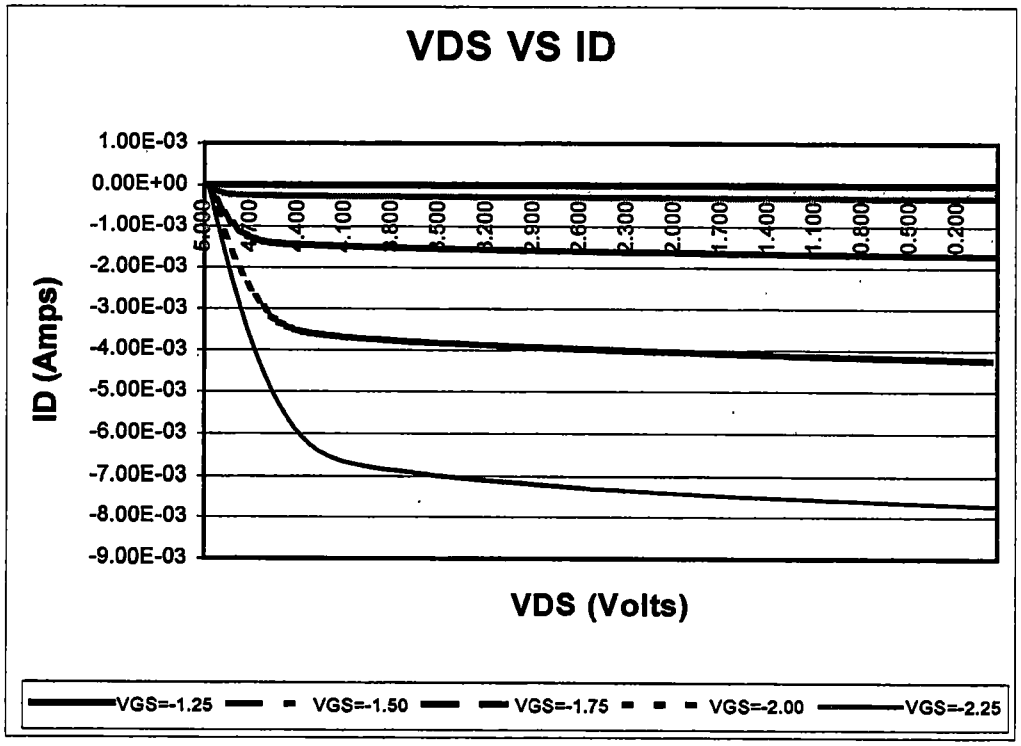


(b)

Figure 4.5 V_{DS} vs I_D Transistor Curves.
(a) NMOS (b) PMOS

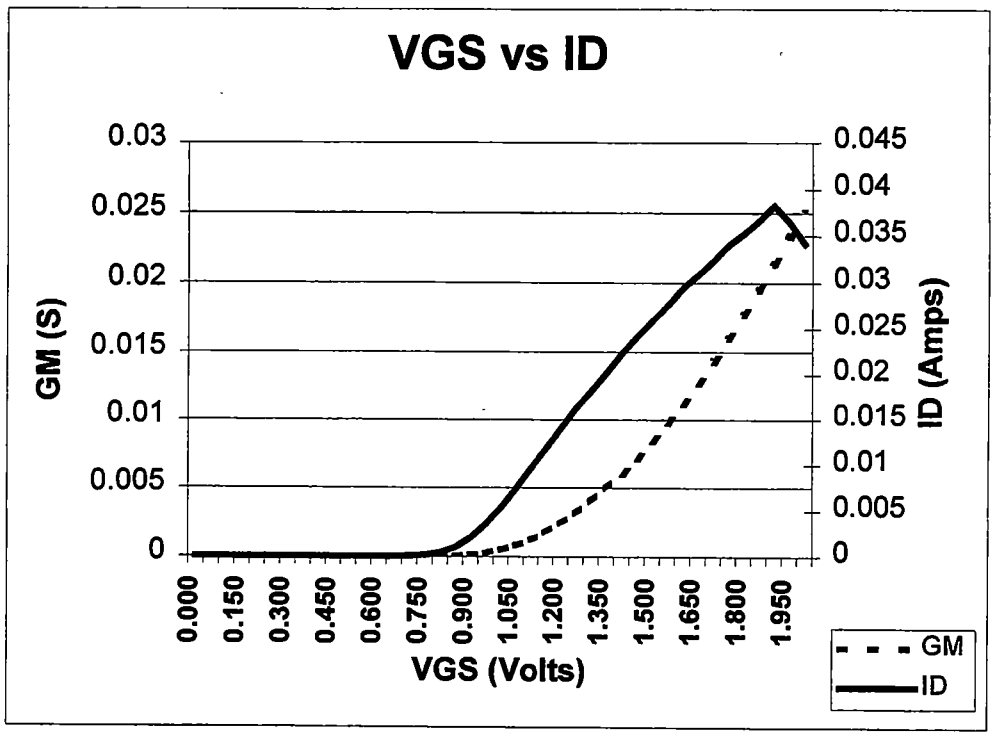
4.2.2 V_{GS} *vs* I_D

Next, the plots for V_{GS} *vs* I_D were performed using the HP 4156A analyzer and the results can be seen in Figure 4.6. The analyzer was used to plot the *gm* of the devices. The *gm* curves shown in the figure are a rough estimate due to the limited derivative scheme the analyzer uses. This was adequate enough for our purposes since we are only interested in these devices for use as a linear switch. From these curves, a tangent line can be drawn from the I_D curve to where it intersects the X-axis to get an estimate of the threshold voltage. In Figure 4.6a, the NMOS device threshold is about 0.9 volts while in Figure 4.6b; the PMOS threshold is approximately -1.1 volts. This corresponds well with the latest lot information from MOSIS with a NMOS having a threshold of 0.90 volts and a PMOS –1.16 volts for a large poly2 device.

4.3 Solar Cell Performance

Current photovoltaic cells have a maximum efficiency of 25%, and that is in a pure sunlight environment. In an incandescent or fluorescent-lighted environment, a PV's efficiency drops to less than 10%. Regardless of the quality of the PV, if the lighting level is too low, then no power can be harvested. On June 30th, the USS Supply (AOE 6), was visited to perform lighting measurements. [7] These measurements involved a photo-diode, which served as reference, and two commercially available PV arrays.

During these tests, the devices were placed in various areas in the ship to simulate the real world application of the sensor array placements. From these positions, the PV's V_{OC}, open-circuit voltage, and I_{SC}, the short-circuit current were measured.



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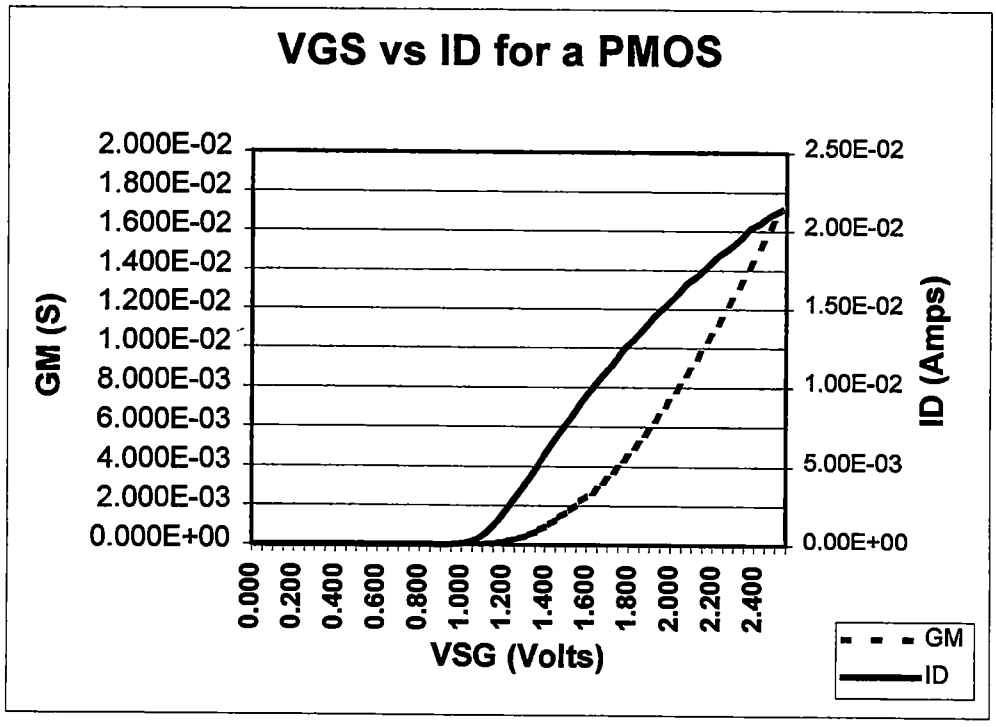


(b)

Figure 4.6 V_{GS} vs I_D Transistor Curves.
(a) NMOS (b) PMOS

The open circuit voltage test is a reasonable measurement of PV quality, while I_{SC} is a measurement of light intensity. The measurements performed on the USS Supply had been previously made at ORNL with the same type of fluorescent lighting.

From these measurements, some preliminary conclusions have been drawn. First, the lighting level available in the test vessel ranges in 100 to 1000 times less than sunlight. The ability for the PV's to produce power decrease due to the low light intensity. Assuming that 4 volts is the minimum requirement for conversion, then only 20% of the available mounting areas provide adequate lighting for the required V_{OC}. For the current RSVP power requirements, the photovoltaic cells will provide little or no power scavenging, and the primary battery will become the most dependent source. Hence, the need to reduce self-power consumption becomes more important.

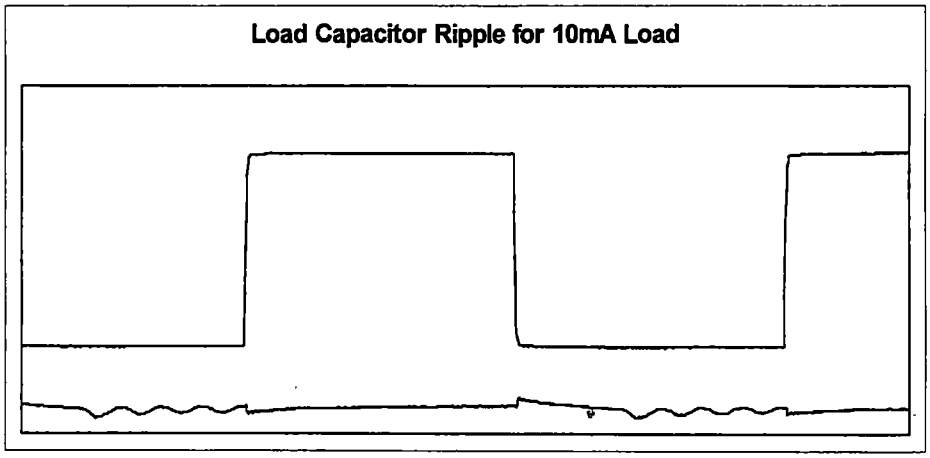
4.4 Buck Converter Testing

A portion of the test board was configured for the clock, input circuit, load capacitor and ASIC containing the converter switch. A surface mount inductor, which measured 852 μH and 3.5 ohms series resistance by a HP 4192A LF Impedance Analyzer, was used. The testing frequency was set to 32 kHz to obtain these values. Several tests were designed to test the performance of the converter while in the system where the input and output capacitors were 10,000 μF and 20,000 μF respectively.

The ripple on the capacitor was measured for three load currents. In these tests, the oscilloscopes were configured to trigger off the clock signal on one channel while the other channel was used to monitor the load capacitor voltage via AC coupling. Figure 4.7 contains three plots for the load currents of 10mA, 3.3mA and the average load current of 330μA.

Figure 4.7a contains a plot for the load current of 10mA. During the initial cycle T_{ON} the voltage begins to slowly increase. This would correspond with the period when $i_L(t)$ the inductor current is more than the load current I_O. Once $i_L(t)$ rises above I_O, the load voltage increases in a more linearly fashion to when it peaks at the end of T_{ON}. There is an initial rise, caused by the switching action and the Schottky diode, in capacitor ripple as the T_{OFF} cycle begins. As the current $i_L(t)$ falls below I_O there is a decrease in the voltage until the point when $i_L(t)$ becomes zero, then the output appears oscillatory.

In Figures 4.7b and 4.7c, with each respective decrease in load current there is a decrease in voltage ripple. Since the load resistance, and therefore the load current decreased, the transition of voltage during T_{ON} becomes a more linear function since $i_L(t)$ rises above I_O quicker. There is also some oscillations in these plots, at the end of inductor current conduction. When examined closer, this oscillation has a frequency of approximately 300 kHz. The self-resonance frequency of the inductor was tested at 1 MHz, so currently the oscillations are unexplained.



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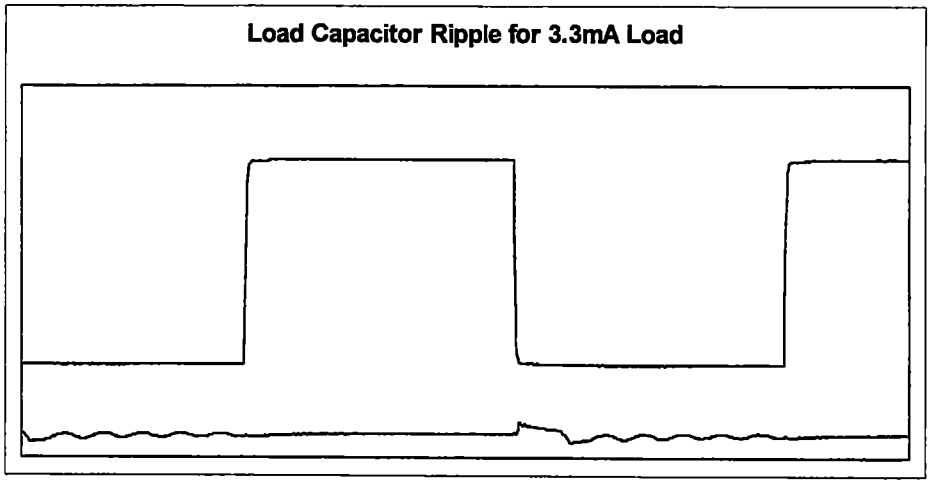

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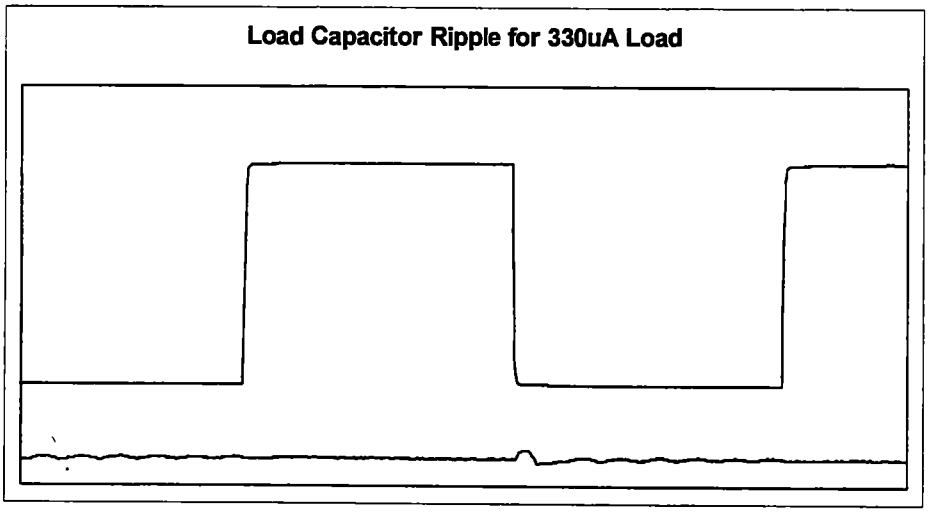


(c)

Figure 4.7 Load Capacitor Voltage Ripple.
(a) 10mA Load (b) 3.3mA load (c) 330μA Load

The next test performed on the converter was to measure the charge moved per cycle. This was performed in two parts, first with the load capacitor being isolated from the regulator and the second case when the regulator was connected. The load capacitor in the system was 20,000μF. In Figure 4.8, the load voltage can be seen plotted versus time. Initially, the source voltage was set to 5 volts, and the load capacitor was drained to zero potential. The test was stopped when the signal was about to run off the oscilloscope screen. As expected, during the initial phase of the test, the voltage in the load capacitor increased quickly and almost linearly. The first transition point occurs around 700ms at approximately 1.88 volts. As the load capacitor voltage increased, the difference between the input source voltage and load capacitor voltage decreased, therefore the energy transferred per cycle also decreased. The voltage increases to a steady-state value of approximately 4.5 volts after an elapsed time of 14 seconds.

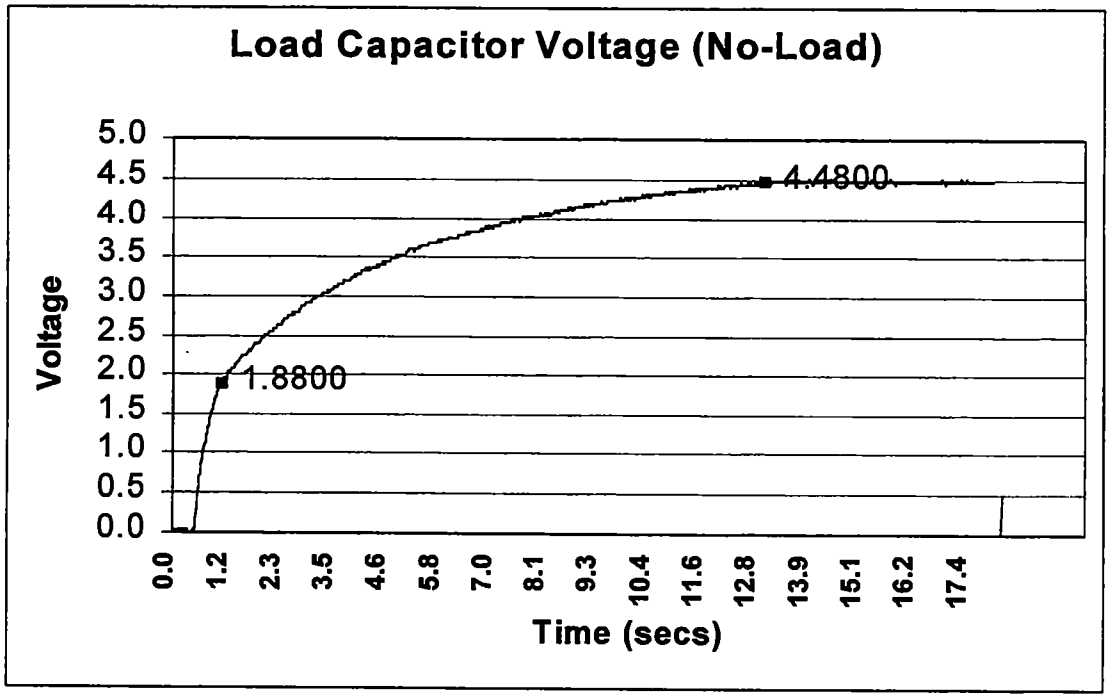


Figure 4.8 Load Capacitor Voltage Change (no-load).

For the no-load case, to calculate the voltage change per clock cycle, we examine the output voltage during the 9-10 second period. Taking the time period of 9.5 to 10 seconds, the voltage increases by 80mV. Dividing this change in voltage by the time to achieve it yields a voltage per second value. Next, we multiply this number by the inverse of the clock frequency to yield a voltage per cycle value. For a clock value of 32.768kHz and the above values, an estimate of the voltage change per clock cycle is 4.88μV/cycle.

Next, the logic was given permission to connect to the load capacitor when its voltage met the minimum input. Figure 4.9 plots the load capacitor voltage when it is connected in the linear regulator circuit. In comparison to the first test, the voltage increases quickly to the 1.88-volt transition point; then the voltage rate decreases. At approximately 3.6 volts, the voltage change begins to decrease even more. At this point, the comparator has fired signaling the PLD that there is adequate voltage for the regulator

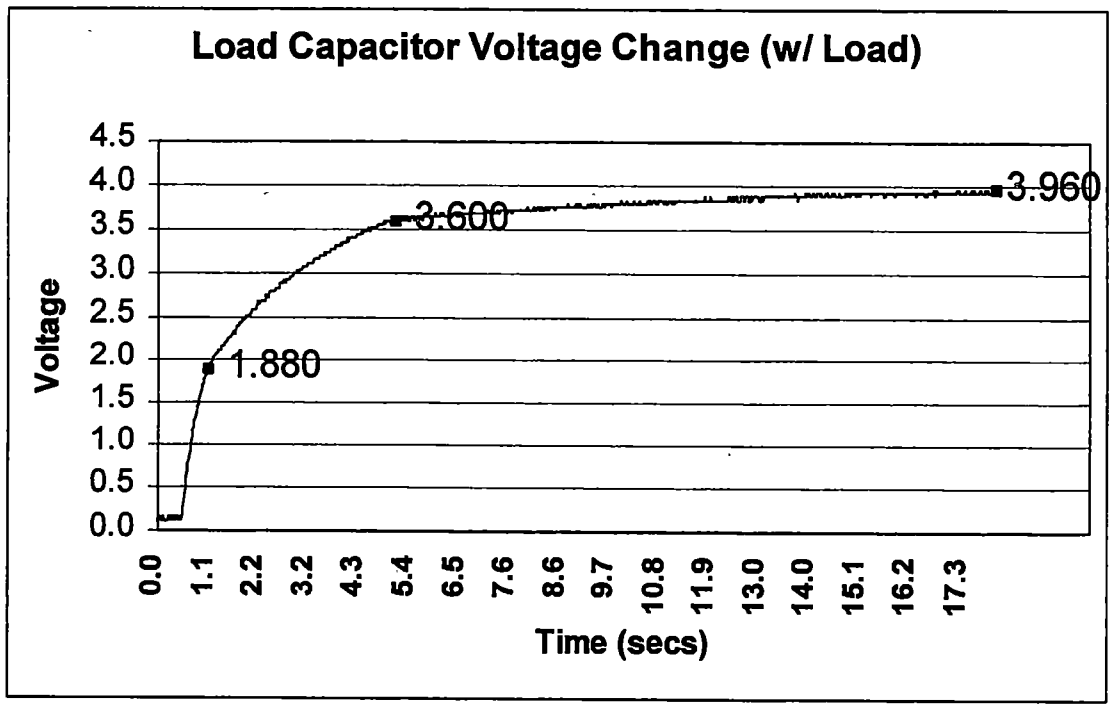


Figure 4.9 Load Capacitor Voltage Change (regulator load).

to use; therefore it switches to the load capacitor. Using the same analysis as the no-load case, and looking at the 17-18 second transition area, the voltage change is 2.44μV/cycle.

In the next test, the input source capacitor and output load capacitor were monitored to verify the earlier analysis assumptions that *Vin* and *Vout* remain relatively constant during one clock cycle. An initial charge of 5 volts was placed on the input while the output was drained to ground potential. The clock signal was applied and the results from the test are seen in Figure 4.10. The plots in the figure have been normalized such that as the load capacitor voltage increases, the decrease in the input source capacitor voltage is visible. After a period of 400 milliseconds the test is stopped and the output is isolated from the input. The natural decay of the capacitors can be seen in each plot. For this period of 400 milliseconds, the input source voltage decays 2.08 volts while the load capacitor voltage increases by 1.48 volts. If we compute the $\Delta V_{LOST\text{-}PER_CYCLE}$

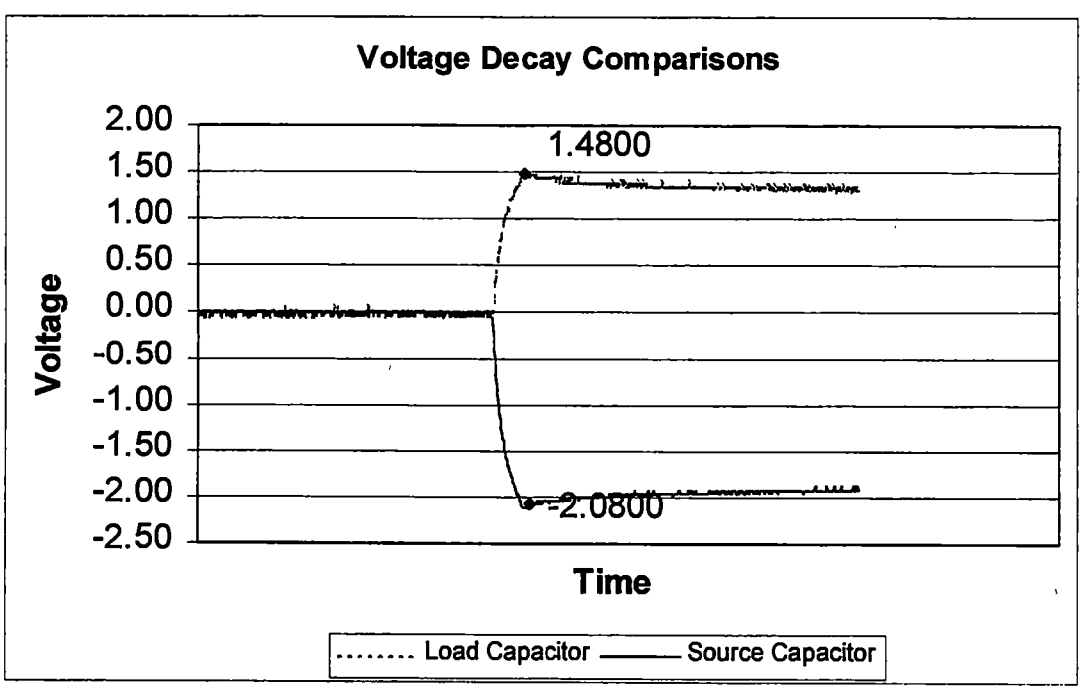


Figure 4.10 Voltage Decay Comparisons.

for each capacitor, then the percentage change from the original value per cycle can be determined. For the input source voltage, $\Delta V_{LOST\text{-}PER_CYCLE}$ is 1.587 mV/cycle while for the output $V_{LOST\text{-}PER_CYCLE}$ is 1.13 mV/cycle. These values are less than 0.05% of the original starting voltage in each case. This verifies that it is reasonable to assume that *Vin* and *Vout* remain relatively constant during one clock cycle.

4.5 System Testing

Various options were available for system testing. With the re-configurable test board, the various components on the two ASICs could be linked together to create the micro-power control system. The different voltage references that were designed could be swapped in and out to find out which one performed best in the overall system. The test board had designed into it a special area that would allow series and paralleling of capacitors to provide better ripple response as well as test components from different manufacturers. Paralleling capacitance would reduce items such as ESR and four 5,000 μF capacitors may perform better than a single 20,000 μF device. Since the digital logic is comprised of a PLD, the logic could be changed quickly and easily. Testpoints and in-line connectors provided readily available circuit access points that aided in trouble-shooting. Sockets were used for the chips and certain resistors to allow replacements. A LED bank provided a visual means of monitoring some of the digital logic signals that are transmitted to the ASICs.

4.5.1 System Results

The first test performed was for the overall system functionality. In the first generation design, our concerns involved the general operation. Power dissipation could not be properly measured with the current layout; this was not our intent in the first generation design. In the next generation ASICs, the power measurement testing will be addressed.

The test board was configured in the following manner. Three "AA" batteries provided a 4.75-volt battery supply voltage. A DC power supply was connected to input source 1. When the board supply powers up, the PLD will become active and begin assessing the situation. As a default set-up, the power switch starts up on the battery supply, and the linear regulator begins to regulate. It was found early in the testing process that the PLD had some incorrect programming. Since this part was removable and re-programmable these errors were easily corrected.

Next, input source 1 was slowly increased to trip the first comparator. Since the load capacitor was initially at ground potential, and the source voltage increased past the minimum 4 volts required for conversion, the DC converter began to transfer voltage to the load capacitors. When the load capacitor voltage reached the 3.5-volt requirement, another comparator fired, signaling the PLD that there was enough voltage for the linear regulator to switch from the battery to load capacitor supply. While the load capacitor voltage remained large enough to maintain the minimum linear regulator input voltage, the power switch stayed connected. This was visibly verifiable as the MODE signal that controls the power switch was tied to an LED.

When the load capacitor voltage reaches the maximum limit, arbitrarily set to 4.4 volts, the clock signal was removed from the converter. As the load capacitor voltage fell below the comparator trip point, the clock signal was once again passed to the converter. Input source 1 was disconnected from the circuit. Slowly, due to the large capacitance, the load capacitor voltage decreased, and tripped another comparator. A signal was sent to the power switch to toggle it back to the battery supply.

The general operation of the system proved successful. Once the PLD logic was re-configured, the system operated as designed, previously described in Chapter 2, Section 2.3. Several factors were noted. When the load capacitor voltage decays to the point of tripping the comparator, there is a period of output jitter. The mode signal toggles between high and low. This problem occurs mainly due to the fact that the comparator has no hysteresis. When the capacitor voltage reaches the trip point, the comparator signal tells the PLD logic to switch to the battery. A large capacitor causes a long decay time. The voltage tends to dwell near the comparator trip point for a short period of time causing this jitter. This problem can be resolved by using some hysteresis.

Several measurements were made on the system operation. Each pin was monitored with the oscilloscope to verify logic transitions. The different references were utilized with the final decision being made to use the low power device. An off-chip step-up converter employing a Linear Technology LT1303 provided the required second source of 9 volts when enabled.

In the efforts to save power, the comparators are enabled on a time interval. Figure 4.11 is a plot of the comparator enable interval used. The frequency is approximately 8.2kHz. Currently, only one interval is designed in the logic, but

considerations are being made for a selectable range of intervals for the next generation. A range of intervals could offer increased power savings. For example, if after a defined number of counts, no input source was available, and then the 8.2kHz frequency could be changed to16.2kHz.

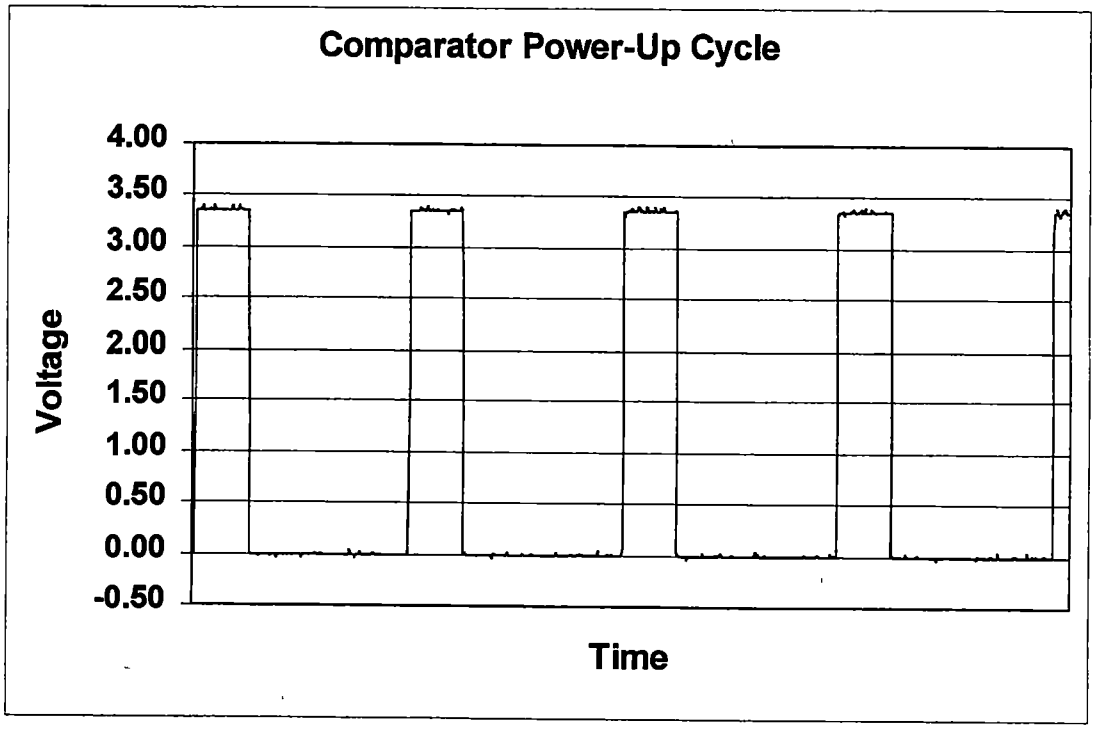


Figure 4.11 Comparator Enable Cycle.

5.0 Conclusions and The Next Generation

5.1 Conclusions

The RSVP test board and ASICs are a completely functioning micro power control system. The system has the ability to monitor up to three input voltage sources, and from these inputs decide which one to use for converter power. In the absence of usable power sources, the ASICs and test board will regulate the on-board battery supply to the required 3.3 volts, and upon a control signal from the sensor cluster (via an on-board interface) will provide a step-up voltage conversion of 9 volts.

The usage of the re-configurable test board allowed experimentation with different components. Utilizing the ALTERA programmable logic device permitted the control logic to be changed when needed. From the system tests, information useful for the next generation implementation was obtained.

One important contribution of this design was the use of a Buck converter in the non-classical style. In the general DC-to-DC converter, there is a feedback mechanism that monitors the input and output voltages, then adjusts the duty cycle of the converter to hold the output voltage constant. The classical feedback usually involves error amplifiers and ramp generators. The additional circuits needed require additional power. In the case of RSVP, self-power consumption needed to be minimized.

The feedback mechanism chosen in RSVP was digital. Comparators monitored voltage levels at critical points and send their outputs to the PLD. From this data, the PLD made the decision whether or not to send the clock signal to the converter. The power-up interval of the comparators limits the amount of charge that could be passed

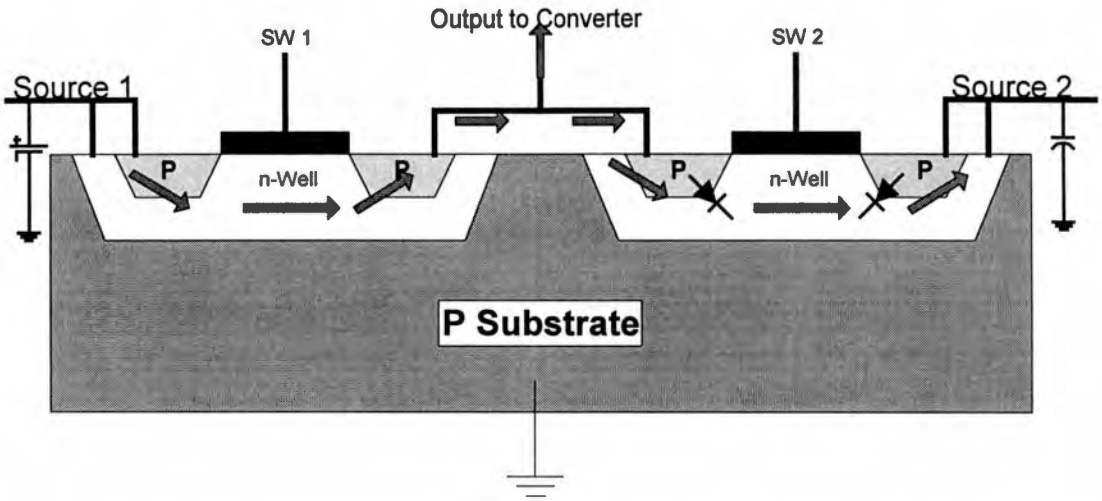
during a period of time. This digital feedback maintained the converter voltage between the voltage levels required for regulation.

5.2 The Next Generation Design

In the second-generation design, the two ASICs were combined to form a single ASIC. The single ASIC included all the system chip components with the exception of the digital control logic. This logic is once again implemented with an off-chip programmable logic device.

One of the important modifications in the next generation design was modifying the well bias on the PMOS transistors of the converter switches. In the original design, the N-well was tied to the input source, since it was assumed that the source would be the highest potential in the chip. During testing, a problem arose with this configuration that could best be described by Figure 5.1a. Suppose we have the case in which source 1 has some voltage, for example 5 volts, but source 2 is unconnected. The input source capacitor of source 2 would be at ground potential. When SW1 (which represents switch 1) is turned on, current will flow (represented by the light gray arrows) from the source to the drain, which is connected to the input of the Buck converter. Since the drain of SW2 is connected to this same node, some of that current will flow into it.

The N-Well of SW2 is connected to its input source. Since the source is at ground, so is the well. Having the well at ground potential causes the drain-to-well pn junction to be forward biased and current flows through the well into the input source 2 capacitor. A Schottky diode (not shown) prevents this current from flowing into source 2.



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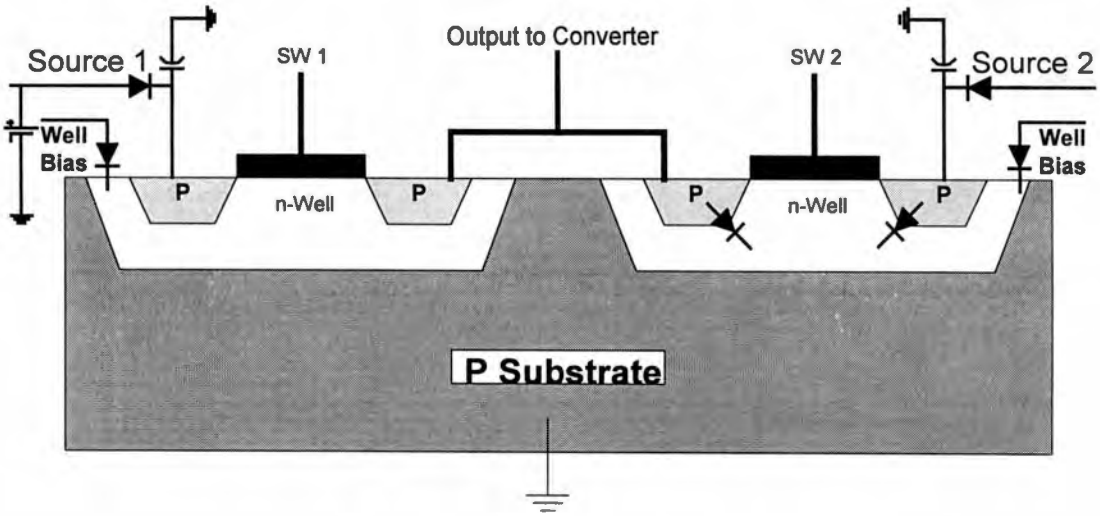

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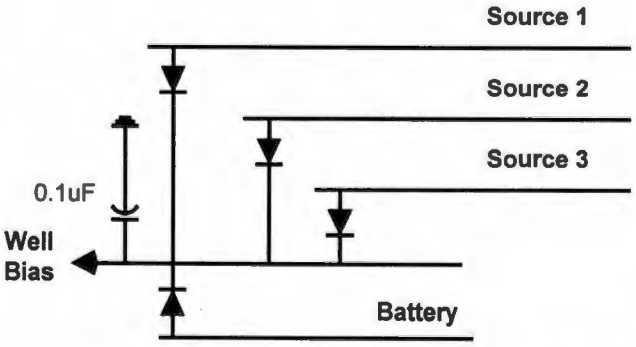

(c)

Figure 5.1 N-Well Problem and Solution.
a) Original Problem b) Solution c) Implementation

This problem was resolved by a special bias scheme, shown in Figure 5.1b. In this new design, the N-wells of all the converter PMOS transistors are tied together to a separate bias line. The implementation of this is shown in Figure 5.1c. Each of the inputs sources as well as the battery voltage is connected to the well bias and a capacitor via a diode. Whichever source has the highest potential bias the well at one diode drop less than that potential. This in essence eliminates the problem of Figure 5.1a, and the wells remain biased at all times. During the initial start-up, the battery biases the well. The 0.1μF helps maintain the well bias in such an event that one input source voltage should increase suddenly, since its capacitor RC time-constant is many times smaller than the input time-constant, the well voltage would change first.

References

References

1. Benner, J.P., and Kazmerski, L., "PHOTOVOLTAICS- Gaining greater visibility," IEEE Spectrum, vol.36, September 1999, p. 34-42.
2. Sum, K.K., *Switch Mode Power Conversion-Basic Theory and Design*, Marcel Dekker, Inc., New York, 1984.
3. Mohan, N., Robbins, W., Undeland, T., *POWER ELECTRONICS: Converters, Applications and Design*, John Wiley & Sons, New York, 1989.
4. Linear Technology Application Note 35, August 1989.
5. Kularatna, N., *Power Electronics Design Handbook- Low-Power Components and Applications*, Butterworth-Heinemann, Boston, 1998.
6. Neff Jr., H.P., *Introductory Electromagnetics*, John Wiley & Sons, New York, 1991.
7. Jellison Jr., G.E. "Report of photovoltaic measurements for RSVP," Internal Report for RSVP, July 1999.
8. Jaeger, R.C., *Microelectronic Circuit Design*, McGraw-Hill, New York, 1997.
9. Kazimierczuk, M.K., Massarini, A., "Feedforward Control of DC-DC PWM Boost Converter," IEEE Transactions On Circuits and Systems, vol. 44, February 1997, p. 143-148.
10. Liu, Y., Sen, P.C., "A Novel Method to Achieve Zero-Voltage Regulation in Buck Converter," IEEE Transactions on Power Electronics, vol. 10, May 1995. p. 292-301.
11. Lee, Y.S., Hui, S.Y.R., "Modeling, Analysis, and Application of Buck Converters in Discontinuous-Input-Voltage Mode Operation," IEEE Transactions on Power Electronics, vol. 12, March 1997, p. 350-360.
12. Ishibashi, K., Sasaki, K., Toyoshima, H., "A Voltage Down Converter with Submicroampere Standby Current for Low-Power Static RAM's," IEEE Journal of Solid-State Circuits, vol. 27, June 1992, p. 920-926.
13. Liu, K., Lee, F, "Zero-Voltage Switching Techniques in DC/DC Converters," IEEE Transactions on Power Electronics, vol. 5, July 1990, p. 293-304.

14. Edminister, J.A., *Theory and Problems of Electromagnetics,* Second Edition, Schaum's Outline Series, McGraw-Hill, New York, 1993.

15. Johns, D.A., Martin, K., *Analog Integrated Circuit Design*, John Wiley & Sons, New York, 1997.

16. Kennedy, E. J., *Operational Amplifier Circuits- Theory and Applications*, Holt, Reinhart and Winston, INC., Fort Worth, 1988.

17. Neamen, D.A., *Electronic Circuit Analysis and Design*, IRWIN, Chicago, 1996.

18. Young, H.D., *University Physics*, Eighth Edition, Addison-Wesley, Reading, Massachusetts, 1992.

19. Hayt, W. H., Kemmerly, J.E., *Engineering Circuit Analysis*, McGraw-Hill, New York, 1993.

20. Allen, P.E., Holberg, D.R., *CMOS Analog Circuit Design*, Oxford University Press, New York, 1987.

21. Laker, K.R., Sansen, W.M.C., *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, New York, 1994.

Appendix

MOSIS SPICE File

```
*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Apr  5/99
* LOT: n92d              WAF: 07
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                        LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 3.24E-8
+XJ      = 3E-7         NCH     = 7.5E16        VTH0    = 0.6075747
+K1      = 0.9566173    K2      = -0.0683927    K3      = 5.0549828
+K3B     = -1.8674576   W0      = 8.28218E-7    NLX     = 1E-9
+DVT0W   = 0            DVT1W   = 5.3E6         DVT2W   = -0.032
+DVT0    = 0.6088937    DVT1    = 0.259137      DVT2    = -0.15
+U0      = 692.4343999  UA      = 2.309878E-9   UB      = 4.260161E-20
+UC      = 5.040994E-11 VSAT    = 1.125047E5    A0      = 0.6801925
+AGS     = 0.1260542    B0      = 1.270651E-6   B1      = 5E-6
+KETA    = -7.926928E-3 A1      = 0             A2      = 1
+RDSW    = 2.360242E3   PRWG    = -1.882869E-3  PRWB    = -5.073137E-6
+WR      = 1            WINT    = 7.098447E-7   LINT    = 2.24693E-7
+XL      = 0            XW      = 0             DWG     = -2.043475E-8
+DWB     = 3.429039E-8  VOFF    = -0.15         NFACTOR = 6.506214E-3
+CIT     = 0            CDSC    = 1.506004E-4   CDSCD   = 0
+CDSCB   = 0            ETA0    = 1.018881E-3   ETAB    = -0.0903072
+DSUB    = 1.0165162    PCLM    = 0.966337      PDIBLC1 = 0.0166619
+PDIBLC2 = 8.257221E-3  PDIBLCB = -1E-3         DROUT   = 0.2122937
+PSCBE1  = 2.419328E9   PSCBE2  = 1.079172E-8   PVAG    = 0.010096
+DELTA   = 0.01         MOBMOD  = 1             PRT     = 0
+UTE     = -1.5         KT1     = -0.11         KT1L    = 0
+KT2     = 0.022        UA1     = 4.31E-9       UB1     = -7.61E-18
+UC1     = -5.6E-11     AT      = 3.3E4         WL      = 0
+WLN     = 1            WW      = 0             WWN     = 1
+WWL     = 0            LL      = 0             LLN     = 1
+LW      = 0            LWN     = 1             LWL     = 0
+CAPMOD  = 2            XPART   = 0.4           CGDO    = 1.61E-10
+CGSO    = 1.61E-10     CGBO    = 0             CJ      = 2.801657E-4
+PB      = 0.9892366    MJ      = 0.5357554     CJSW    = 1.44905E-10
+PBSW    = 0.9899903    MJSW    = 0.1           PVTH0   = 0.048707
+PRDSW   = -816.757313  PK2     = -0.0211242    WKETA   = 3.473399E-3
+LKETA   = -0.0148621   )
*
.MODEL CMOSP PMOS (                        LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 3.24E-8
+XJ      = 3E-7         NCH     = 2.4E16        VTH0    = -0.8325178
+K1      = 0.473213     K2      = -6.767284E-5  K3      = 10.9871814
+K3B     = -2.5253874   W0      = 1.386173E-6   NLX     = 5.898689E-7
+DVT0W   = 0            DVT1W   = 5.3E6         DVT2W   = -0.032
+DVT0    = 0.8176342    DVT1    = 0.4022741     DVT2    = -0.135001
+U0      = 285.7020867  UA      = 5.529914E-9   UB      = 2.542638E-19
+UC      = -9.57127E-11 VSAT    = 1.892611E5    A0      = 0.9669059
+AGS     = 0.1556695    B0      = 4.487494E-6   B1      = 5E-6
+KETA    = -1.385857E-3 A1      = 0             A2      = 1
+RDSW    = 1.820034E3   PRWG    = -3.433422E-3  PRWB    = -0.0324413
+WR      = 1            WINT    = 8.158914E-7   LINT    = 1.616486E-8
```

```
+XL    = 0          XW    = 0          DWG    = -3.942453E-8
+DWB   = 2.383052E-8  VOFF  = -0.0974516  NFACTOR = 1.5
+CIT   = 0          CDSC  = 8.97355E-4   CDSCD  = 0
+CDSCB  = 0          ETA0  = 0.022023     ETAB   = 7.261928E-4
+DSUB  = 0.0120319   PCLM  = 8.7451558    PDIBLC1 = 9.081258E-4
+PDIBLC2 = 2.315992E-4  PDIBLCB = -2.370143E-8  DROUT  = 0.1077312
+PSCBE1 = 1.80586E10  PSCBE2 = 4.931801E-9  PVAG   = 1.7473999
+DELTA  = 0.01       MOBMOD = 1          PRT    = 0
+UTE    = -1.5       KT1   = -0.11       KT1L   = 0
+KT2    = 0.022      UA1   = 4.31E-9     UB1    = -7.61E-18
+UC1    = -5.6E-11   AT    = 3.3E4      WL     = 0
+WLN    = 1          WW    = 0          WWN    = 1
+WWL    = 0          LL    = 0          LLN    = 1
+LW     = 0          LWN   = 1          LWL    = 0
+CAPMOD = 2          XPART = 0.4        CGDO   = 2.04E-10
+CGSO   = 2.04E-10   CGBO  = 0          CJ     = 2.949728E-4
+PB     = 0.7592448  MJ    = 0.4469704  CJSW   = 1.901925E-10
+PBSW   = 0.99       MJSW  = 0.1        PVTH0  = 0.1143307
+PRDSW  = -581.5148875  PK2  = 0.0130225  WKETA  = 0.0141729
+LKETA  = -9.713213E-3  )
*
```

SPICE file for Switch Resistance Test

```
.current
* Jeff Eagen
*Extracted Switch
*Operating Point Analysis

.option MEthod=gear
.OP
.DC Iload 0 16m .001m

xswitch 1 3 1 0 swarray2

*********MAIN Switch w/ inverter*********************
.subckt swarray2 swin swout clkin gnd!
* swarray2.spice
*
* File Location       /msd25/eagen/RSVP
* File Created        Thu Jul  8 17:18:57 1999
* Ext2spice Version   ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*        Options   -m -n -M -N -m -n -mg -M -N -h -g -n -mm -V
*
****** top level cell is /msd25/eagen/RSVP/swarray2.ext
M1 swin NSIG swout gnd! CMOSN M=40 W=150.00U L=3.60U GEO=0
M2 swout M3 swin swin CMOSP M=40 W=150.00U L=3.60U GEO=0
M3 M3 clkin swin swin CMOSP W=36.00U L=3.60U GEO=0
M4 NSIG M3 swin swin CMOSP W=36.00U L=3.60U GEO=0
M5 M3 clkin gnd! gnd! CMOSN W=46.80U L=3.60U GEO=0
M6 NSIG M3 gnd! gnd! CMOSN W=46.80U L=3.60U GEO=0
C1 NSIG swout 20.1F
C2 gnd! NSIG 2.1F
C3 swin NSIG 27.0F
C4 swin 0 194.8F
C5 gnd! 0 60.2F
C6 clkin 0 11.5F
C7 M3 0 99.6F
C8 NSIG 0 137.3F
C9 swout 0 84.4F
*************************************************************
.ends


Vpv 1 0 4                    $ constant Photovoltaic Supply
Iload 3 0 16m                $ Load Current

.END
```

Extracted Flip-Flop SPICE File

```
.flip-flop

*This is test of flip flop
* Jeff Eagen
*Operating Point Analysis
*.option converge=1 post
.option MEthod=gear
*.option node
.OP
.tran 100us 10ms
.nodeset V(output1)=0

xffp1 oscsig data 100 100 output1 100 0 eagenffp

 r output1 0 1000k
vpwr 100 0 3.6
vdata data 0 pulse(0 3.6 0us 200ns 200ns 1.1ms 4ms)

vcntrl cntrl 0 pulse(0 3.6 1000us 200ns 200ns .5ms 4ms)
m1 cntrl2 cntrl 100 100 cmosp w=30u l=1.5u
m2 cntrl2 cntrl 0 0 cmosn w=15u l=1.5u
m1A osc cntrl oscsig 100 cmosp w=62u l=2u
m2A osc cntrl2 oscsig  0 cmosn w=48u l=2u

.subckt eagenffp clk data rst set q 3 9
* flip_flop.spice              3 is power

** Subcircuit definition for dfbf311
** Extraction file is /msd15/belakbir/current_source/dfbf311.ext
*.SUBCKT dfbf311 3 9
*.nodset clk 0 data 0 rst 1 set 1
M1 1 2 3 3 CMOSP W=14.40U L=1.20U GEO=0
M2 2 clk 3 3 CMOSP W=14.40U L=1.20U GEO=0
M3 5 data 3 3 CMOSP W=19.20U L=1.20U GEO=0
M4 5 2 7 3 CMOSP W=19.20U L=1.20U GEO=0
M5 7 1 8 3 CMOSP W=12.60U L=1.20U GEO=0
M6 1 2 9 9 CMOSN W=10.80U L=1.20U GEO=0
M7 2 clk 9 9 CMOSN W=10.80U L=1.20U GEO=0
M8 7 1 10 3 CMOSP W=6.60U L=1.20U GEO=0
M9 10 11 3 3 CMOSP W=6.60U L=1.20U GEO=0
M10 8 rst 3 3 CMOSP W=21.00U L=1.20U GEO=0
M11 11 7 3 3 CMOSP W=14.40U L=1.20U GEO=0
M12 11 set 3 3 CMOSP W=13.80U L=1.20U GEO=0
M13 14 11 3 3 CMOSP W=12.00U L=1.20U GEO=0
M14 14 1 15 3 CMOSP W=12.00U L=1.20U GEO=0
M15 15 2 16 3 CMOSP W=16.20U L=1.20U GEO=0
M16 16 rst 3 3 CMOSP W=16.20U L=1.20U GEO=0
M17 16 q 3 3 CMOSP W=16.20U L=1.20U GEO=0
M18 q 15 3 3 CMOSP W=17.40U L=1.20U GEO=0
M19 q set 3 3 CMOSP W=16.20U L=1.20U GEO=0
M20 18 data 9 9 CMOSN W=10.20U L=1.20U GEO=0
M21 18 1 7 9 CMOSN W=10.20U L=1.20U GEO=0
M22 7 2 19 9 CMOSN W=10.20U L=1.20U GEO=0
```

```
M23 19 11 20 9 CMOSN W=6.60U L=1.20U GEO=0
M24 20 rst 9 9 CMOSN W=11.40U L=1.20U GEO=0
M25 11 7 21 9 CMOSN W=10.80U L=1.20U GEO=0
M26 21 set 9 9 CMOSN W=10.80U L=1.20U GEO=0
M27 22 11 9 9 CMOSN W=6.60U L=1.20U GEO=0
M28 22 2 15 9 CMOSN W=6.60U L=1.20U GEO=0
M29 15 1 16 9 CMOSN W=11.40U L=1.20U GEO=0
M30 16 rst 23 9 CMOSN W=13.20U L=1.20U GEO=0
M31 23 q 9 9 CMOSN W=8.40U L=1.20U GEO=0
M32 24 15 9 9 CMOSN W=13.80U L=1.20U GEO=0
M33 24 set q 9 CMOSN W=13.80U L=1.20U GEO=0
C1 3 q 1.8F
C2 9 16 1.3F
C3 9 7 1.4F
C4 7 8 2.5F
C5 9 q 1.2F
C6 3 8 4.1F
C7 9 19 1.5F
C8 3 2 1.8F
C9 3 11 2.8F
C10 9 2 3.5F
C11 15 16 1.6F
C12 9 11 2.7F
C13 3 1 2.1F
C14 9 20 1.1F
C15 3 15 1.6F
C16 9 1 1.2F
C17 3 16 1.8F
C18 3 7 2.9F
C19 16 0 16.4F
C20 data 0 6.1F
C21 2 0 27.9F
C22 rst 0 11.4F
C23 11 0 18.2F
C24 q 0 13.3F
C25 set 0 11.5F
C26 15 0 13.1F
C27 1 0 32.2F
C28 7 0 19.1F
C29 clk 0 6.1F
C30 9 0 26.9F
C31 3 0 40.5F
.ENDS

Vosc osc 0 pulse(0 3.6 0us 100ns 100ns 15.25us 30.5us)        $assumption, run of battery

vcontrol ncntrl 0 pulse(0 3.6 4ms 100ns 100ns 2ms 4ms)

.END
```

SPICE file for Ideal Operation

```
.Non-deal Circuit 1
*Test for general performance with extracted switch and ideal comparators
*Comparators are constantly on
* Jeff Eagen
*        Operating Point Analysis
.option converge=1 post
.OP
.tran 2000us 200ms
.option fast

xswitch 2 3 oscout 0 swarray2

*********MAIN Switch w/ inverter********************
.subckt swarray2 swin swout clkin gnd!
* swarray2.spice
*
* File Location      /msd25/eagen/RSVP
* File Created       Thu Jul  8 17:18:57 1999
* Ext2spice Version   ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*        Options   -m -n -M -N -m -n -mg -M -N -h -g -n -mm -V
*
****** top level cell is /msd25/eagen/RSVP/swarray2.ext
M1 swin NSIG swout gnd! CMOSN M=40 W=150.00U L=3.60U GEO=0
M2 swout M3 swin swin CMOSP M=40 W=150.00U L=3.60U GEO=0
M3 M3 clkin swin swin CMOSP W=36.00U L=3.60U GEO=0
M4 NSIG M3 swin swin CMOSP W=36.00U L=3.60U GEO=0
M5 M3 clkin gnd! gnd! CMOSN W=46.80U L=3.60U GEO=0
M6 NSIG M3 gnd! gnd! CMOSN W=46.80U L=3.60U GEO=0
*C1 NSIG swout 20.1F
*C2 gnd! NSIG 2.1F
*C3 swin NSIG 27.0F
*C4 swin 0 194.8F
*C5 gnd! 0 60.2F
*C6 clkin 0 11.5F
*C7 M3 0 99.6F
*C8 NSIG 0 137.3F
*C9 swout 0 84.4F
.ends
*************************************
Cpv 2 0 1uf ic=3.4          $ simultating the photo voltaic
Rs 1 2 1k                   $ 1k ohms to simulate current draw
d1 0 3 D10bq015             $ model for a schotky diode
L1 3 4 1000u R=10           $ series inductor

Cbattery out 0 20uf ic=3.0 $ simultating the output battery
Rload out 0 10k             $ simulating output load

******* voltage monitor ***************************

ecomp1 output1 0 ref1 out 1e5 max=3.6 min=0        $This comparator monitors outpit < 4
* Output1 is output of comparator, referenced to ground

ecomp2 output2 0 1 ref2  1e5 max=3.6 min=0         $This comparator monitors input >3.8
```

```
* Output2 is output of comparator, referenced to ground

x1 osc CNTRL 500 oscout 100 nandand          $This is the AND for clock and control signal
x2 output1 output2 80 CNTRL 100 nandand      $this is AND for input/output checks

.subckt nandand IN1 IN2 OUTN OUTINV PWR
m1 2 IN2 0 0 cmosn w=15u l=1.5u m=1
m2 OUTN IN1 2 0 cmosn w=15u l=1.5u m=1
m3 OUTINV OUTN 0 0 cmosn w=15u l=1.5u

m4 OUTN IN1 PWR PWR cmosp w=30u l=1.5u m=1
m5 OUTN IN2 PWR PWR cmosp w=30u l=1.5u m=1
m6 PWR OUTN OUTINV PWR cmosp w=30u l=1.5u
.ends

**** DC Bias Voltages ********
Vpv 1 0 pulse(2 7 0ms 20ms 20ms 40ms 80ms)          $ ramped photo voltaic supply
Vosc osc 0 pulse(0 3.6 0us 100ns 100ns 15.25us 30.5us)  $assumption, run of battery
Vconst 100 0 3.6                                    $a constant supply voltage
VIS 4 out dc 0                                      $dummy voltage source to test currents
vref1 ref1 0 dc 4                                   $Set up the voltage reference1
vref2 ref2 0 dc 3.6                                 $Set up the voltage reference2


*SETTING UP THE MODELS      PART
.MODEL D10bq015 d
+IS=1.66692e-05 RS=0.0549971 N=1.0339 EG=0.6
+XTI=0.5 BV=15 IBV=0.001 CJO=4.70891e-10
+VJ=1.5 M=0.699718 FC=0.5 TT=0
+KF=0 AF=1
* Model generated on May 28, 96
* Model format: SPICE3


.END
```

SPICE File for Extracted Comparators

```
.Non Ideal Circuit 2
*This is the entire regulator with extracted switchwith built in inverters, uses shanes comparators
*No flip-flops, comparators are constantly on
* Jeff Eagen
*Operating Point Analysis

.OP
.tran 1000us 2000ms
*.option fast
.option accurate=1
 .OPTION CONVERGE=1 GMINDC=   1.0000E-12

xswitch 2 3 oscout 0 swarray2

*********MAIN Switch w/ inverter*********************
.subckt swarray2 swin swout clkin gnd!
* swarray2.spice
*
* File Location       /msd25/eagen/RSVP
* File Created        Thu Jul  8 17:18:57 1999
* Ext2spice Version   ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*        Options    -m -n -M -N -m -n -mg -M -N -h -g -n -mm -V
*
****** top level cell is /msd25/eagen/RSVP/swarray2.ext
M1 swin NSIG swout gnd! CMOSN M=40 W=150.00U L=3.60U GEO=0
M2 swout M3 swin swin CMOSP M=40 W=150.00U L=3.60U GEO=0
M3 M3 clkin swin swin CMOSP W=36.00U L=3.60U GEO=0
M4 NSIG M3 swin swin CMOSP W=36.00U L=3.60U GEO=0
M5 M3 clkin gnd! gnd! CMOSN W=46.80U L=3.60U GEO=0
M6 NSIG M3 gnd! gnd! CMOSN W=46.80U L=3.60U GEO=0
*C1 NSIG swout 20.1F
*C2 gnd! NSIG 2.1F
*C3 swin NSIG 27.0F
*C4 swin 0 194.8F
*C5 gnd! 0 60.2F
*C6 clkin 0 11.5F
*C7 M3 0 99.6F
*C8 NSIG 0 137.3F
*C9 swout 0 84.4F
.ends

Cpv 2 0 1000uf ic=3.4          $ simultating the photo voltaic
Rseries 1 2 1k                 $ 1k ohms to simulate current draw
Vtest 3 4 DC 0                 $ Test source to see if current is drawn when the switch is open

D1 0 4  D10bq015               $ model for a schotky diode
L1 4 out 1000u R=10            $ series inductor

Cbattery out 0 2000u ic=3.0    $simultating the output battery
Rload out 0 10k                $ simulating output load
```

```
**********************COMPARATORS*************************************************
compar1 ref1 out out1 100 200 shancomp    $This is comparator for output less<4
*        ref1 is reference of 4 volts     out1 is output of the comparator
*        out is the output node sampling  VDDC/200 are power and neg supply

xcompar2 1 ref2 out2 100 200 shancomp          $This is comparator for input power >3.6
*        ref2 is reference of 3.6 volts        out2 is output of the comparator
*        1 is the input node sampling          VDDC/200 are power and neg supply


********************AND GATES*************************************************

x1 osc CNTRL 500 oscout 100 nandand            $This is the AND for clock and control signal
x2 output1 output2 80 CNTRL 100 nandand        $this is AND for input/output checks

*******************SUPPLY VOLTAGES/CURRENTS*********************************

Vpv 1 0 pulse(2 7 0ms 20ms 20ms 40ms 80ms)       $ ramped photo voltaic supply
Vosc osc 0 pulse(0 3.6 0us 1000ns 1000ns 15.25us 30.5us)    $32.768 oscilltator
Vconst 100 0 3.6                         $a constant supply voltage
vss 200 0 dc 0                                 $comparator negative supply
vref1 ref1 0 dc 4                        $Set up the voltage reference, "MAX OUTPUT"
vref2 ref2 0 dc 3.6                            $Set up the voltage reference, "MIN INPUT"

**********************MISCELLANOUS SUB CIRCUITS*********************************

*****************SHANE'S COMPARATOR ******************************************
.subckt shancomp in+ in- out 100 200       $where 100 is + supply, 200 is - supply
***************** Shane's Comparator
****************************************************
* File Location       /users2/frank/ic/RSVP/compare
* File Created        Wed Jun  9 15:20:04 1999
* Ext2spice Version   ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*        Options   -m -n -M -N -m -n -mg -M -N -h -g -n -mm -V
*
****** top level cell is /users2/frank/ic/RSVP/compare/cmph2b.ext
M1 4 in- 3 200 CMOSN M=2 W=12.00U L=3.00U
M2 5 in+ 3 200 CMOSN M=2 W=12.00U L=3.00U
M3 4 4 100 100 CMOSP W=6.00U L=3.00U
M4 5 5 100 100 CMOSP W=6.00U L=3.00U
M5 3 10 200 200 CMOSN M=2 W=6.00U L=3.00U
M6 out 5 100 100 CMOSP W=24.00U L=3.00U
M7 out 9 200 200 CMOSN W=19.80U L=3.00U
M8 9 4 100 100 CMOSP W=6.00U L=3.00U
M9 9 9 200 200 CMOSN W=6.00U L=3.00U
M10 5 4 100 100 CMOSP W=6.0U L=3.00U
M11 4 5 100 100 CMOSP W=6.0U L=3.00U
*M10 5 4 100 100 CMOSP W=9.60U L=3.00U
*M11 4 5 100 100 CMOSP W=9.60U L=3.00U
M12 10 10 200 200 CMOSN M=2 W=6.00U L=3.00U
*C1 200 in+ 8.5F
*C2 100 out 1.2F
*C3 200 out 1.3F
```

```
*C4 9 in+ 1.4F
*C5 in- 3 3.2F
*C6 4 5 1.5F
*C7 200 0 8.7F
*C8 10 0 10.0F
*C9 in- 0 13.4F
*C10 in+ 0 12.1F
*C11 3 0 10.9F
*C12 4 0 14.5F
*C13 5 0 17.6F
*C14 out 0 3.5F
*C15 9 0 11.8F
*C16 100 0 4.6F

Ibias 100 10 dc 1u
*** Node Listing for subckt:  cmph2b
** N0                    == IdealGND
** N1          [U=1]    == N1
** N2          [U=1]    == N2
** N3          [U=3]    == N3
** N4          [U=6]    == N4
** N5          [U=6]    == N5
** N6          [U=2]    == N6
** N9          [U=4]    == N9
** N10          [U=3]    == N10
** N100         [U=12]   == N100
** N200         [U=10]   == N200
.ends
*************************************************************


*************************NANDAND GATE ****************************
.subckt nandand IN1 IN2 OUTN OUTINV PWR
m1 2 IN2 0 0 cmosn w=15u l=1.5u m=1
m2 OUTN IN1 2 0 cmosn w=15u l=1.5u m=1
m3 OUTINV OUTN 0 0 cmosn w=15u l=1.5u

m4 OUTN IN1 PWR PWR cmosp w=30u l=1.5u m=1
m5 OUTN IN2 PWR PWR cmosp w=30u l=1.5u m=1
m6 PWR OUTN OUTINV PWR cmosp w=30u l=1.5u
.ends
*****************************************************************

*SETTING UP THE MODELS      PART
.model eagen d (is=1e-15 rs=10)
.MODEL D10bq015 d
+IS=1.66692e-05 RS=0.0549971 N=1.0339 EG=0.6
+XTI=0.5 BV=15 IBV=0.001 CJO=4.70891e-10
+VJ=1.5 M=0.699718 FC=0.5 TT=0
+KF=0 AF=1
* Model generated on May 28, 96
* Model format: SPICE3

.END
```

Entire System SPICE File

```
. Entire System
*This is the entire regulator with extracted switch
*with built in inverters and extracted opamps/includes flip-flops
* also includes switched comparators
* Jeff Eagen

*Operating Point Analysis
.OP
.tran 1ms .8
.option fast
.OPTION CONVERGE=1 GMINDC=  1.0000E-12

xswitch 2 3 oscout 0 swarray2
Cpv 2 0 10000uf ic=5              $ simultating the photo voltaic
Rseries 1 2 1                     $ 1k ohms to simulate current draw
Vtest 3 4 DC 0                    $ Test source to see if current is drawn when the switch is open
D1 0 4  D10bq015                  $ model for a schotky diode
L1 4 out 1000u R=15               $ series inductor
Cbattery out 0 2000u ic=3.6       $simultating the output battery
Rload out 0 10k                   $ simulating output load

************COMPARATORS*********************************************
xcompar1 ref1 out out1 pwr 200 shancomp  $This is comparator for output less<4
*        ref1 is reference of 4 volts    out1 is output of the comparator
*        out is the output node sampling VDDC/200 are power and neg supply

xcompar2 1 ref2 out2 pwr 200 shancomp    $This is comparator for input power >3.6
*        ref2 is reference of 3.6 volts  out2 is output of the comparator
*        1 is the input node sampling    VDDC/200 are power and neg supply
**************************AND GATES*****************************************

x1 osc CNTRL 500 oscout 100 nandand          $This is the AND for clock and control signal
x2 output1 output2 80 CNTRL 100 nandand      $this is AND for input/output checks

********************FLIP-FLOPS**********************************************

xffp1 oscinfp out1 100 100 output1 100 0 eagenffp
*this is flip flop for comparator 1
xffp2 oscinfp out2 100 100 output2 100 0 eagenffp
*this is flip flop for comparator 2

* clk data rst set q 3 9
xgate1 osc oscinfp pwr psig 100 0 TGATE      $This is the control logic used for enabling
                                             $the clock on Flip/Flop
m100 psig pwr 0 0 cmosn w=15u l=1.5u
m101 psig pwr 100 100 cmosp w=30u l=1.5u m=1

****************SUPPLY VOLTAGES/CURRENTS*********************************
Vpv 1 0 5                                          $ constant photo voltaic supply
*Vpv 1 0 pulse(2 7 0ms 20ms 20ms 40ms 80ms)        $ ramped photo voltaic supply
Vosc osc 0 pulse(0 3.6 0us 1000ns 1000ns 15.25us 30.5us)  $32.768 oscilltator
Vconst 100 0 3.6                                   $a constant supply voltage
vss 200 0 dc 0                                     $comparator negative supply
```

```
*vpwr pwr 0 dc 3.6
vpwr pwr 0 pulse (0 3.6 0us 1000ns 1000ns 15.25us 4000us) $power up cycle comparators
*VIS 4 out dc 0                                  $Just a dummy voltage source to test L currents
vref1 ref1 0 dc 4                                $Set up the voltage reference, "MAX OUTPUT"
vref2 ref2 0 dc 3.6                              $Set up the voltage reference, "MIN INPUT"

******************MISCELLANOUS SUB CIRCUITS*********************************

*********MAIN Switch w/ inverter********************
.subckt swarray2 swin swout clkin gnd!
* swarray2.spice
*
* File Location       /msd25/eagen/RSVP
* File Created        Thu Jul  8 17:18:57 1999
* Ext2spice Version   ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*        Options    -m -n -M -N -m -n -mg -M -N -h -g -n -mm -V
*
****** top level cell is /msd25/eagen/RSVP/swarray2.ext
M1 swin NSIG swout gnd! CMOSN M=40 W=150.00U L=3.60U GEO=0
M2 swout M3 swin swin CMOSP M=40 W=150.00U L=3.60U GEO=0
M3 M3 clkin swin swin CMOSP W=36.00U L=3.60U GEO=0
M4 NSIG M3 swin swin CMOSP W=36.00U L=3.60U GEO=0
M5 M3 clkin gnd! gnd! CMOSN W=46.80U L=3.60U GEO=0
M6 NSIG M3 gnd! gnd! CMOSN W=46.80U L=3.60U GEO=0
*C1 NSIG swout 20.1F
*C2 gnd! NSIG 2.1F
*C3 swin NSIG 27.0F
*C4 swin 0 194.8F
*C5 gnd! 0 60.2F
*C6 clkin 0 11.5F
*C7 M3 0 99.6F
*C8 NSIG 0 137.3F
*C9 swout 0 84.4F
.ends

*******SHANE'S COMPARATOR ********************************************
.subckt shancomp in+ in- out 100 200          $where 100 is + supply, 200 is - supply
************** Shane's Comparator ******************************************************
* File Location       /users2/frank/ic/RSVP/compare
* File Created        Wed Jun  9 15:20:04 1999
* Ext2spice Version   ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*        Options    -m -n -M -N -m -n -mg -M -N -h -g -n -mm -V
*
****** top level cell is /users2/frank/ic/RSVP/compare/cmph2b.ext
M1 4 in- 3 200 CMOSN M=2 W=12.00U L=3.00U
M2 5 in+ 3 200 CMOSN M=2 W=12.00U L=3.00U
M3 4 4 100 100 CMOSP W=6.00U L=3.00U
M4 5 5 100 100 CMOSP W=6.00U L=3.00U
M5 3 10 200 200 CMOSN M=2 W=6.00U L=3.00U
M6 out 5 100 100 CMOSP W=24.00U L=3.00U
M7 out 9 200 200 CMOSN W=19.80U L=3.00U
M8 9 4 100 100 CMOSP W=6.00U L=3.00U
M9 9 9 200 200 CMOSN W=6.00U L=3.00U
M10 5 4 100 100 CMOSP W=6.0U L=3.00U
M11 4 5 100 100 CMOSP W=6.0U L=3.00U
```

```
*M10 5 4 100 100 CMOSP W=9.60U L=3.00U
*M11 4 5 100 100 CMOSP W=9.60U L=3.00U
M12 10 10 200 200 CMOSN M=2 W=6.00U L=3.00U
*C1 200 in+ 8.5F
*C2 100 out 1.2F
*C3 200 out 1.3F
*C4 9 in+ 1.4F
*C5 in- 3 3.2F
*C6 4 5 1.5F
*C7 200 0 8.7F
*C8 10 0 10.0F
*C9 in- 0 13.4F
*C10 in+ 0 12.1F
*C11 3 0 10.9F
*C12 4 0 14.5F
*C13 5 0 17.6F
*C14 out 0 3.5F
*C15 9 0 11.8F
*C16 100 0 4.6F

Ibias 100 10 dc 1u
*** Node Listing for subckt:  cmph2b
** N0                  == IdealGND
** N1          [U=1]   == N1
** N2          [U=1]   == N2
** N3          [U=3]   == N3
** N4          [U=6]   == N4
** N5          [U=6]   == N5
** N6          [U=2]   == N6
** N9          [U=4]   == N9
** N10         [U=3]   == N10
** N100        [U=12]  == N100
** N200        [U=10]  == N200
.ends
*************************************************************

************************NANDAND GATE ***************************
.subckt nandand IN1 IN2 OUTN OUTINV PWR
m1 2 IN2 0 0 cmosn w=15u l=1.5u m=1
m2 OUTN IN1 2 0 cmosn w=15u l=1.5u m=1
m3 OUTINV OUTN 0 0 cmosn w=15u l=1.5u

m4 OUTN IN1 PWR PWR cmosp w=30u l=1.5u m=1
m5 OUTN IN2 PWR PWR cmosp w=30u l=1.5u m=1
m6 PWR OUTN OUTINV PWR cmosp w=30u l=1.5u
.ends
*****************************************************************

*****************TRANSMISSION GATE*********************************************
.subckt TGATE  in out nsig psig vdd vss
*high on NSIG turns switch on
m1 in nsig out vss cmosn w=3u l=1.5u m=1
m2 in psig out vdd cmosp w=3u l=1.5u m=1
```

```
.ends


*********************FLIP_FLOP ************************************************
.subckt eagenffp clk data rst set q 3 9
* flip_flop.spice            3 is power 9 is ground

** Subcircuit definition for dfbf311
** Extraction file is /msd15/belakbir/current_source/dfbf311.ext
*.SUBCKT dfbf311 3 9
*.nodset clk 0 data 0 rst 1 set 1
M1 1 2 3 3 CMOSP W=14.40U L=1.20U GEO=0
M2 2 clk 3 3 CMOSP W=14.40U L=1.20U GEO=0
M3 5 data 3 3 CMOSP W=19.20U L=1.20U GEO=0
M4 5 2 7 3 CMOSP W=19.20U L=1.20U GEO=0
M5 7 1 8 3 CMOSP W=12.60U L=1.20U GEO=0
M6 1 2 9 9 CMOSN W=10.80U L=1.20U GEO=0
M7 2 clk 9 9 CMOSN W=10.80U L=1.20U GEO=0
M8 7 1 10 3 CMOSP W=6.60U L=1.20U GEO=0
M9 10 11 3 3 CMOSP W=6.60U L=1.20U GEO=0
M10 8 rst 3 3 CMOSP W=21.00U L=1.20U GEO=0
M11 11 7 3 3 CMOSP W=14.40U L=1.20U GEO=0
M12 11 set 3 3 CMOSP W=13.80U L=1.20U GEO=0
M13 14 11 3 3 CMOSP W=12.00U L=1.20U GEO=0
M14 14 1 15 3 CMOSP W=12.00U L=1.20U GEO=0
M15 15 2 16 3 CMOSP W=16.20U L=1.20U GEO=0
M16 16 rst 3 3 CMOSP W=16.20U L=1.20U GEO=0
M17 16 q 3 3 CMOSP W=16.20U L=1.20U GEO=0
M18 q 15 3 3 CMOSP W=17.40U L=1.20U GEO=0
M19 q set 3 3 CMOSP W=16.20U L=1.20U GEO=0
M20 18 data 9 9 CMOSN W=10.20U L=1.20U GEO=0
M21 18 1 7 9 CMOSN W=10.20U L=1.20U GEO=0
M22 7 2 19 9 CMOSN W=10.20U L=1.20U GEO=0
M23 19 11 20 9 CMOSN W=6.60U L=1.20U GEO=0
M24 20 rst 9 9 CMOSN W=11.40U L=1.20U GEO=0
M25 11 7 21 9 CMOSN W=10.80U L=1.20U GEO=0
M26 21 set 9 9 CMOSN W=10.80U L=1.20U GEO=0
M27 22 11 9 9 CMOSN W=6.60U L=1.20U GEO=0
M28 22 2 15 9 CMOSN W=6.60U L=1.20U GEO=0
M29 15 1 16 9 CMOSN W=11.40U L=1.20U GEO=0
M30 16 rst 23 9 CMOSN W=13.20U L=1.20U GEO=0
M31 23 q 9 9 CMOSN W=8.40U L=1.20U GEO=0
M32 24 15 9 9 CMOSN W=13.80U L=1.20U GEO=0
M33 24 set q 9 CMOSN W=13.80U L=1.20U GEO=0
*C1 3 q 1.8F
*C2 9 16 1.3F
*C3 9 7 1.4F
*C4 7 8 2.5F
*C5 9 q 1.2F
*C6 3 8 4.1F
*C7 9 19 1.5F
*C8 3 2 1.8F
*C9 3 11 2.8F
*C10 9 2 3.5F
```

```
*C11 15 16 1.6F
*C12 9 11 2.7F
*C13 3 1 2.1F
*C14 9 20 1.1F
*C15 3 15 1.6F
*C16 9 1 1.2F
*C17 3 16 1.8F
*C18 3 7 2.9F
*C19 16 0 16.4F
*C20 data 0 6.1F
*C21 2 0 27.9F
*C22 rst 0 11.4F
*C23 11 0 18.2F
*C24 q 0 13.3F
*C25 set 0 11.5F
*C26 15 0 13.1F
*C27 1 0 32.2F
*C28 7 0 19.1F
*C29 clk 0 6.1F
*C30 9 0 26.9F
*C31 3 0 40.5F
*** Node Listing for subckt:  dfbf311
** N0                    == IdealGND
** N1          [U=7]    == 24
** N2          [U=8]    == 21
** N3          [U=30]   == Vdd!
** N4          [U=2]    == CLK2
** N5          [U=2]    == 120
** N6          [U=2]    == DATA1
** N7          [U=7]    == 25
** N8          [U=2]    == 122
** N9          [U=25]   == GND!
** N10         [U=2]    == 121
** N11         [U=7]    == 23
** N12         [U=4]    == RST3
** N13         [U=4]    == SET4
** N14         [U=2]    == 123
** N15         [U=6]    == 33
** N16         [U=5]    == Q_b
** N17         [U=5]    == Q
** N18         [U=2]    == 150
** N19         [U=2]    == 151
** N20         [U=2]    == 152
** N21         [U=2]    == 153
** N22         [U=2]    == 154
** N23         [U=2]    == 155
** N24         [U=2]    == 156
.ENDS

*****************************end of flip flop ***************

*SETTING UP THE MODELS      PART
.model eagen d (is=1e-15 rs=10)
.MODEL D10bq015 d
```

```
+IS=1.66692e-05 RS=0.0549971 N=1.0339 EG=0.6
+XTI=0.5 BV=15 IBV=0.001 CJO=4.70891e-10
+VJ=1.5 M=0.699718 FC=0.5 TT=0
+KF=0 AF=1
.ends
.END
```

Vita

Jeff Eagen was born in Perth Amboy, New Jersey on January 19th, 1973. After several years of relocating, he graduated from Upland High School in Upland, California in June 1991. He entered the University of Tennessee in the Spring 94 semester where after a near-fatal car accident and later the death of his younger sibling graduated with a Bachelor of Science in Electrical Engineering in August 1998. In August 1998 he was awarded a Graduate Research Assistant position in the UT/ORNL Joint Graduate Program in pursuit of a Master of Science degree in Electrical Engineering. The Master's degree was received December 1999.