DESIGN AND IMPLEMENTATION OF ENERGY HARVESTING CIRCUITS FOR MEDICAL DEVICES

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ABSTRACT

Technological enhancements in a low-power CMOS process have promoted enhancement of advanced circuit design techniques for sensor related electronic circuits such as wearable and implantable sensor systems as well as wireless sensor nodes (*WSNs*). In these systems, the powering up the electronic circuits has remained as a major problem because battery technologies are not closely following the technological improvements in semiconductor devices and processes thus limiting the number of sensor electronics modules that can be incorporated in the design of the system. In addition, the traditional batteries can leak which can cause serious health hazards to the patients especially when using implantable sensors. As an alternative solution to prolonging the life of battery or to mitigate serious health problems that can be caused by battery, energy harvesting technique has appeared to be one of the possible solutions to supply power to the sensor electronics. As a result, this technique has been widely studied and researched in recent years. In a conventional sensor system, the accessible space for batteries is limited, which restricts the battery capacity. Therefore, energy harvesting has become an attractive solution for powering the sensor electronics. Power can be scavenged from ambient energy sources such as electromagnetic signal, wind, solar, mechanical vibration, radio frequency (RF), and thermal energy etc. Among these common ambient sources, RF and piezoelectric vibration-based energy scavenging systems have received a great deal of attention because of their ability to be integrated with sensor electronics modules and their moderate available power density. In this research, both RF and piezoelectric vibration-based energy harvesting systems have been studied and implemented in 130 nm standard CMOS process.

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CHAPTER 1 – INTRODUCTION

1.1 Motivation

In 1989, the *World Wide Web* (*WWW*) was developed by Tim Berners Lee. Since then, the internet technology has rapidly spread throughout the world and has become an essential part of our daily lives [1]. In addition, the internet technology has triggered technological advancements in various fields. With the help of wireless technology, the internet technology is now more and more expanding its territories into various fields. For example, as one of the products of this expanding technology, called Internet of Things (*IoT*) has emerged in recent years. The definition of *IoT* in Wikipedia states it as following; "The Internet of Things (*IoT*) is the network of physical devices vehicles, and other items embedded with electronics software, sensors, actuators, and network connectivity which enable these objects to collect and exchange data [2]." As stated above, the *IoT* utilizes computer-based system to allow direct access to various devices through the existing network infrastructures wirelessly. By accessing remotely into various systems or system components such as sensor electronics, one can do more things than ever imagined before. For examples, using the electronic systems in an automobile, one can measure numerous parameters such as tire pressure, temperatures etc. in various hard to reach places inside the vehicle, and can perform diagnostics of various automotive issues and so forth. In medical sensor systems, the doctors can monitor patients remotely with the help of various sensors that monitor health issues of the patients [3]. However, powering up these sensors or wireless devices is a major problem associated with the *IoT* systems. In the above example of an automobile, most sensors are located in hard to reach places and thus replacing or extending life of a battery is one of the major problems.

For sensors used particularly in medical devices, it is not only difficult to change the battery but also a battery itself can be harmful to human body and can even be fatal in some cases. As a result, researchers have explored various solutions including the idea of the energy harvesting. In general, energy harvesting, alternatively knows as energy scavenging or power harvesting, exploits existing ambient energy such as solar, thermal, wind, kinetic, or radio frequency etc. The mechanism of acquiring or capturing such wasted or free energy from the ambient environment is called energy harvesting or energy scavenging [4]. Table 1.1 shows typical power density available in ambient energy sources [4,8,9,10].

Energy harvesting was not feasible for CMOS circuits in the past due to the low harvestable energy density associated with the traditional ambient energy sources as well as high transistor turn-on voltage of common CMOS processes. However, recent advancements in semiconductor device technologies have resulted in highly advanced low power CMOS processes requiring power supplies below 1.2 V. Combination of low-current, low-threshold requirements of the transistors, and the low power supply voltages allows energy harvesting technology to be utilized in various miniaturized low-power CMOS electronic systems. This research is focused on energy harvesting utilizing vibrational and radio frequency energy sources. Due to the limitation of the energy density of the harvested or scavenged energy from vibration and radio frequency sources, the battery used in the medical system cannot be completely replaced with harvested energy sources. However, the harvested energy can be utilized to extend the life of the battery in applications involving small scale electronic systems.

Table 1.1 Various Types of Ambient Energy Sources [4,8,9,10]

Energy Sources	Performance
Solar (Direct sunlight)	100 mW/cm^2
Solar (Illuminated office)	100 mW/cm^2
Thermoelectric	60 µW/cm^2 at 5 °C gradient
Blood Pressure	0.93 W at 100 mmHg
Vibrational Micro-Generator	4 µW/ cm^2 (Human motion ~ Hz) 800 µW/ cm^2 (Machines ~ KHz)
Piezoelectric Push Buttons	50 µJ/N
Ambient Radio Frequency	1 µW/cm^2

1.2 Research Goal

The goal of this research is to design a vibration-based energy harvesting circuit using a piezoelectric transducer, as well as a radio frequency-based energy harvesting circuit with DC-DC converter incorporated with maximum power point tracking (MPPT) system. In the first part of this work, a piezoelectric transducer-based energy harvesting system has been proposed and designed. A piezoelectric transducer-based energy harvesting system is much simpler to design compared to an electrostatic based system because of its simpler system architecture. In addition, a piezoelectric transducer-based energy harvesting system can provide moderate power density. In addition, a piezoelectric transducer-based energy harvesting system can be easily utilized in our daily lives because of its small size. Table 1.2 shows the advantages versus disadvantages of the three vibration-based material systems.

Table 1.2 Advantages and Disadvantages of Vibration-Based Materials [7,8,9]

Type	Advantages	Disadvantages	Practical max. energy density (mJ/cm^3)
Piezoelectric	1. No external energy sources 2. Output voltage range of 1 to 10 volts 3. Do not require mechanical stops 4. Highest energy density	1. Difficult to integrated with micro-system 2. Need high frequency and stress	35
Electrostatic	1. Easy to merge with microsystems or small-scale electronics 2. Output voltage range of 2 to 10 volts	1. External voltage source required 2. Mechanical stops required	4
Electromagnetic	1. No external voltage source 2. Do not require mechanical stops 3. High output power	1. Maximum output voltage of 0.1 volt 2. Difficult to integrated with micro-system 3. Complex design	25

As can be seen from Table 1.2 [7.8.9], a piezoelectric transducer-based energy harvesting system is more advantageous compared to the other two systems. Therefore, in this dissertation, an extensive research has been performed to the development of energy harvesting system for the piezoelectric transducer and will be presented in the next chapter.

In the second parts of this dissertation, a radio frequency (RF) based energy harvesting utilizing another freely available source with DC-DC boost converter will be presented. In a RF energy harvesting, a DC-to-DC boost converter with maximum power point tracking (MPPT) will be integrated to achieve a maximum power output of a radio frequency signal. An impedance matching circuitry to match a RF rectifier with a DC-to-DC converter will be employed so that the maximum available power from a RF rectifier can be squeezed out.

1.3 Original Contribution

In this dissertation, new and improved architectures of a piezoelectric transducer-based energy harvesting circuit will be presented. By adding a switching signal on a PMOS switch, there will be significantly reduced leakage current resulting in reduction of energy loss especially in low available input power from a piezoelectric transducer. In a radio frequency energy harvesting design, a new way of controlling zero current detection for a DC-DC converter will be presented, which enhances the total efficiency of the RF energy harvesting circuit. In addition, a simple but effective way of controlling the maximum power point tracking (MPPT) with wide range of the input impedance in a DC-DC converter will be presented.

1.4 Thesis Overview

The remaining chapters of this research will cover followings. Chapter 2 will cover the general information regarding ambient energy sources for the energy harvesting system. In this chapter, a reader can find information on the general sources for energy harvesting system, reasons to develop such ideas, and the advantages of each ambient energy sources. Chapter 3 will cover the vibration-based energy harvesting materials. In this chapter, a reader can find the information regarding various materials that are currently used and researched as energy sources based on the vibration by many scholars. In addition, a reader can find the advantages and disadvantages of each vibration-based energy source. In Chapter 4 the actual implementation of energy harvesting circuits based on vibration will be presented. In this chapter, a reader can find the reasons for choosing a piezoelectric transducer as energy source for the vibration-based energy harvesting system. In addition, a detailed analysis of design and implementation of the proposed AC-to-DC rectifier for the piezoelectric transducer will be presented. Chapter 5 will cover background information and details of radio frequency-based energy harvesting circuits. In this chapter, a reader can find the general information regarding what the radio frequency energy harvesting is as well as detailed analysis of a radio frequency (RF) energy harvesting system. Chapter 6 will cover conclusion and future works for this proposed research.

CHAPTER 2 – BACKGROUND OF ENERGY HARVESTING

2.1 Typical Ambient Energy Sources

There are many kinds of available ambient sources for energy harvesting systems around us. Among them, the following sources are the most popular and have been researched by many researchers because of its ease of accessibility and availability. These energy sources are solar, thermal, electrostatic, acoustic noise, human generated, nuclear power, wind, radio frequency, and mechanical vibration [4,8,9,10]. Among these energy sources, electromagnetic, electrostatic, thermal, chemical and mechanical based energy harvesting systems are the ones typically used for small scale power required by electronic systems [7,8,9]. In addition, such power sources are small enough to be used in such system due to their ease of integration.

2.2 Ambient Energy Resources

As discussed in section 2.1, electromagnetic, electrostatic, thermal, chemical and mechanical based ambient energy sources are the general categories of energy harvesting sources and are applicable to the small electronics or sensor application where relatively small amount power is required to power up and operate the systems. In this section, a brief introduction to these ambient energy sources will be presented.

2.2.1 Thermal Energy Sources

Thermal device is the one which converts the temperature difference into an electrical energy. The potential thermal based energy sources are power plant generated wasted heat, heated ocean water, etc. A CMOS based thermoelectric device or generator is composed of an electrically connected *p*-type and *n*-type silicon in series. In general, this kind of device or generator generates a current proportional to the temperature deviation, due to the temperature difference between the hot side and the cold side of the device or the generator. The general efficiency equation of the thermoelectric device can be driven by the *Carnot cycle* and the maximum available power can be written as following [11],

$$P_{MAX} = Q\frac{T_H - T_L}{T_H} \tag{2.1}$$

where, T_H is high temperature of the hot side,

T_L is the low temperature of the cold side, and Q is the temperature source.

In real life, the conversion efficiency of the thermal energy is much lower than $P_{MAX,}$ and even in ideal calculation using equation (2.1), P_{MAX} is lower than 100 %. The major drawback of using the thermal energy harvesting is that the temperature deviation between the hot and the cold sides should be large enough to achieve adequate harvested energy. An example of the thermal energy harvesting involving a wristwatch operated by the temperature difference between the human body and room temperature has been presented in [12].

2.2.2 Kinetic Energy Sources

The kinetic energy is associated with any moving object with movement or motion. The main advantages of the kinetic energy are the availability of many forms of these sources in the ambient. Therefore, it is very common energy source that can be easily fond and reused as a source of energy harvesting. Since the kinetic energy has the force (F), which makes an object to move, and the distance (d), which is the actual distance traversed, it follows the simple laws of physics. As a result, the equation of the instantaneous power (P_{inst}) as well as average power that a kinetic energy has generated can be written as following [13];

$$P_{inst} = Fd \tag{2.2}$$

Since the kinetic energy is one of the most common energy sources available and due to its ability to adapt to a small scale electric devices or sensors, many researchers are focusing on this energy source for future energy harvesting. As an example, in [14], a wearable sensor using a rotor kinetic energy generator as a power source is presented. In addition, there are many real-world products available out there and one of those involves a watch manufactured by Seiko which uses human motion to translate it into an electrical energy to power up the watch. Since the kinetic energy is one of the topics in this research, further details regarding the energy source will be discussed in the following sections.

2.2.3 Electromagnetic Energy Sources

There are many different forms of electromagnetic energy sources. Among these, radio frequency and light have received the most attention from the researchers. The radio frequency form of electromagnetic energy is nowadays receiving a lot of attention since the radio signals are omni present in home, school, café, airport and so forth [15]. Therefore, it is very easy to access and utilize this energy source. On the other hand, light energy has been used and researched for a long time due to its ease of implementation and ability for miniaturization. As a good example, solar panels used for powering up the street lights or a home are widespread. In addition, there are many small electronics that are powered by solar panel such as a calculator. As can be seen from the examples, the light energy source is the most commonly used and can be found easily in our daily life. However, there are several problems with the light sources which make them less attractive compared to other ambient sources of energy. The typical efficiency of a photovoltaic cell, also called a solar cell, is not more than roughly 20 percent, and it is also achievable only when the cell gets sun light directly. In addition, the power generated by the solar cell depends mostly on its size [16]. Because of these reasons, many researchers are trying to find a better solution in terms of solar cell materials which can result in improved efficiency. Since a radio frequency is one of the topics in the research, radio frequency energy harvesting system will be covered in more details in later chapters.

CHAPTER 3 – VIBRATION BASED ENERGY HARVESTING MATERIALS

3.1 Ambient Energy Sources Based on Vibration

Kinetic energy based on vibration can be found in many different forms. For example, a human while walking can produce kinetic energy based on vibration. Table 3.1 shows different types of vibration energy generated based on frequency and amplitude of acceleration at the fundamental frequency.

As can be seen from Table 3.1, there are many forms of vibration based kinetic energy present around us.

Table 3.1 Peak Frequency and Acceleration Amplitude of Various Vibration-Based Energy Sources [6,17,18,19]

Vibration Sources	Peak Frequency (Hz)	Acceleration Amplitude (m/s^2)
Clothes dryer	121	3.5
Small microwave oven	121	2.25
Washing machine	109	0.5
Computer CD R/W	75	0.6
Car engine	200	1.2
Vehicles	5 ~ 2000	0.5 ~ 110
Kitchen blender	121	3.4
Refrigerator	240	0.1

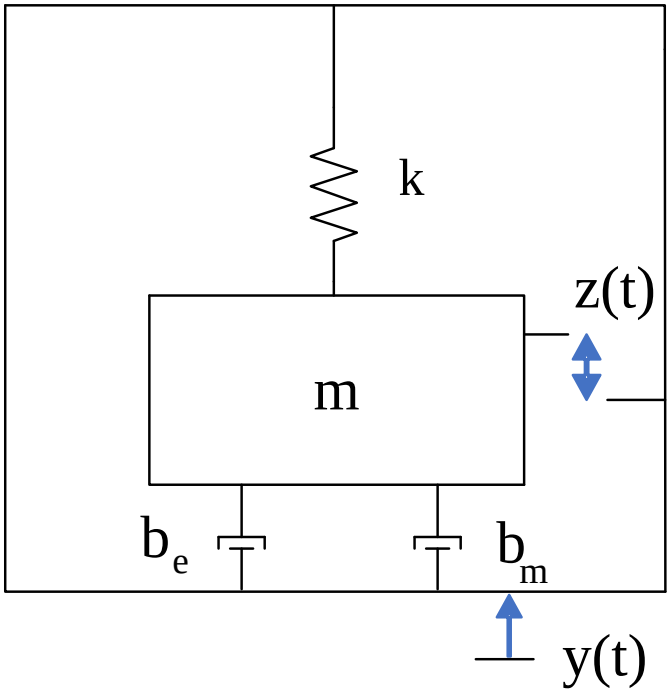


Fig. 3.1 A general simplified model of a vibration translator [8].

In addition, the operating frequency of devices is relatively low. Fig 3.1 shows the simplified model of a vibration translator [8].

From Fig. 3.1, the power translated from vibration energy can be written as (3.1) [6].

$$Power = \frac{1}{2} b_e \dot{z}^2 \tag{3.1}$$

where b_e is representing the coefficient of an electrically generated damping,

b_m is representing the coefficient of a mechanical damping,

k is representing the coefficient of spring constant,

m is representing the mass.

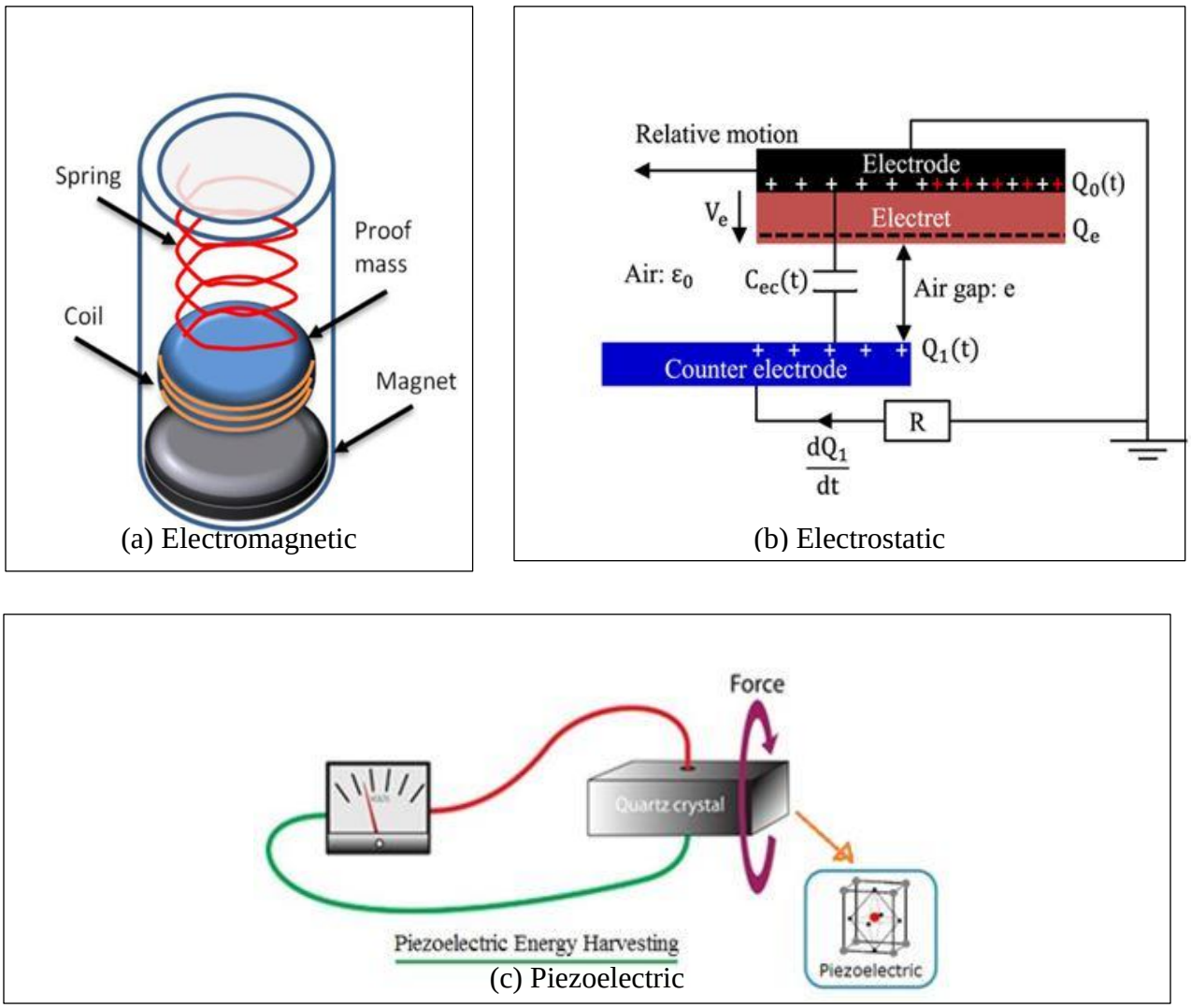


Fig. 3.2 Three types of vibration based energy sources:

(a) Electromagnetic, (b) Electrostatic, (c) Piezoelectric [27,28,29].

There are three general types of widely used energy sources out there, which are derived from vibration-based energy sources such as electromagnetic, electrostatic, and piezoelectric. Fig. 3.2 illustrates the three types of vibration-based energy sources [27,28,29].

As shown in Table 3.2, there are several ongoing research efforts by numerous groups on electromagnetic and electrostatic energy sources. However, due to their inherent limitation of available power as well as problems associated with the operation of electrostatic and electromagnetic sources shown in Table 3.2, quite a few researchers are focused more on piezoelectric based energy sources compared to the other two. The detailed literature review will be discussed in the next section.

Table 3.2 Summary of Power Generated by Various Vibration-Based Energy Sources

Energy Sources	Power Harvested	Resonant Frequency	References
MEMS	4.29 µW	_	[24]
Variable-resonating Capacitor	120 nW	50 Hz	[25]
Electromagnetic micro-generator	1 µW	70 ~ 200 Hz	[26]
Electromagnetic micro-generator	400 µW	_	[20]
Parametric Frequency-Increased Generator	13.6 µW	50 Hz	[27]
MEMS based laser-micro generator	~ 830 µW	60 ~ 110 Hz	[28]

3.2 Theoretical Background of Piezoelectricity

In this section, short introduction of a piezoelectric material will be presented.

3.2.1 Piezoelectric Effect

The word "*piezo*" came from the Greek word meaning "*pressure*" [23]. The phenomenon of the piezoelectric effect was discovered by Jacques and Pierre Curie brothers in 1880, and demonstrated piezoelectric effect using a quartz and a tourmaline [23]. Piezoelectric materials can be demonstrated by means of a piezo-effect when subjected to electrical force or mechanical bending or stretching [23]. Such behavior will cause a piezoelectric material to undergo a change in electrical polarization. A direct piezoelectric effect is called a generator or a sensor effect, which converts mechanical energy into electrical energy [23]. In addition, an electrical potential can be applied causing a change in length or deformation of the shape of the piezoelectric material. This is called as the inverse piezoelectric effect or the actuator effect [23]. The reverse piezoelectric effect converts electrical energy into mechanical energy. There are numbers of common applications where the piezoelectric effect can be employed such as microphones, cigarette lighters, piezoelectric motors, ear phones, combustion engines, speakers, and signal transducers, etc.

3.2.2 Piezoelectric Materials

There are diverse types of natural or synthetic piezoelectric materials currently available for commercial applications. Typical natural piezoelectric materials are quartz, salt, cane sugar, tourmaline etc. [23]. Examples of typical man-made or synthetic piezoelectric materials are lead zirconate titanate (PZT), barium titanate ($BaTiO_3$), polyvinylidenefluoride (PVDF), ZnO etc. [23]. From industrial as well as research point of view, breakthrough of piezoelectric materials technology begins with the development of piezoelectric ceramics.

Table 3.3 Properties of Popular Piezoelectric Materials

Materials	**Shapes or Forms**	d_{31} **(m/V or C/N)**[1]	$(\varepsilon_{33} / \varepsilon_0)$[2]	k_{31}[3]	T_C(ºC)[4]	**Reference**
Quartz	Single Crystal	2.3	4.4	-	-	[29]
PZT	Sol-gel thin film	190 ~ 250	800 ~ 1100	-	-	[30]
PZT	Polycrystalline	-190 ~ 320	1800 ~ 3200	0.32 ~ 0.44	230 ~ 350	[31]
PZT	Sputtered thin film	100	-	-	-	[32]
PVDF	Film	23	12 ~ 13	0.12	80 ~ 100	[35]
ZnO	Sputtered thin film	10.5 ~ 11.5	10.8 ~ 11	-	-	[30]

[1] d_{31} denotes the piezoelectric coefficient.

[2] $\varepsilon_{0 = 8.854 \times 10^{-12}}$ F/m which is the permittivity of the empty space, ε is the dielectric constant.

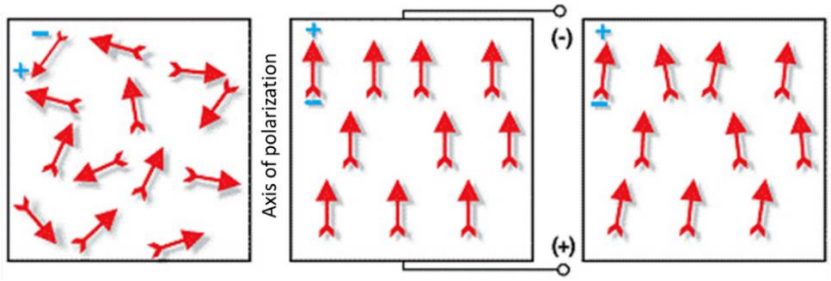
[3] k_{31} denotes the electromechanical coupling coefficient.

[4] T_C is the Curie temperature.

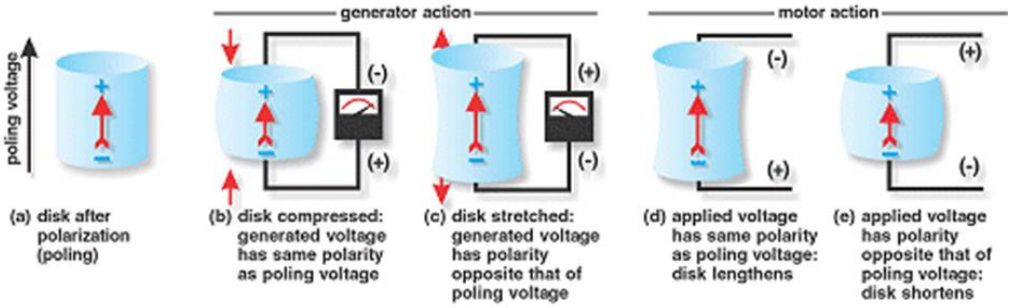
Table 3.3 lists the most commonly used piezoelectric materials. From the table, it can be easily seen that there is one particular material, which has superior properties compared to the others.

The superior material is PZT. Usually, a PZT has the highest Curie temperature as well as the largest electromechanical coefficient. Fig. 3.3 shows how the piezoelectric material acts with different applied forces or strains [33,34].

In general, a piezoelectric crystal is in non-symmetrical form and is electrically neutral as well. Therefore, electrons in piezoelectric materials have perfectly balanced charges. However, when a piezoelectric material is squeezed or stretched, atoms inside of piezoelectric crystals are getting closer together or fall apart from each other. Such action causes upsetting of the balance of positive and negative charges. As a result, a piezoelectric material emits electrical charges. For commercial applications, two types of PZT materials are available right now. One is a hard type PZT, and the other is a soft type PZT [23,34]. Usually, a PZT ceramic is doped with either acceptor dopants or donor dopants. If a PZT is doped with an acceptor dopant, then it is called as a hard type PZT, and if it is doped with a donor dopant, then it is called as a soft type PZT. The difference between a hard and a soft type of PZT is whether a piezoelectric constant is higher or not. Since the domain wall motion of a hard type of a PZT is blocked or disrupted by its impurities, it has a lower piezoelectric constant but has lower loss. On the other hand, a soft type of PZT has a higher piezoelectric constant but higher loss as well. This is due to the fact, that an acceptor dopant creates an oxygen vacancy, while a donor dopant creates a metal vacancy. When the polarization process is performed with strong electrical field applied to two electrodes, the directions of polarization is determined to be the axis 3.



(a)



(b)

Fig. 3.3 (a) Polarizing (Poling) a piezoelectric ceramic
(b) generator and motor (actuator) action of a piezoelectric material [33,34].

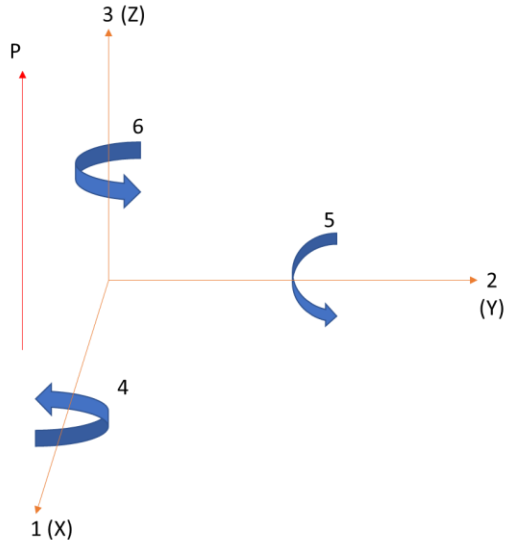


Fig. 3.4 The properties of a polarized piezoelectric ceramic in an orthogonal system [36].

Fig. 3.4 shows this polarized piezoelectric ceramic in orthogonal system. The polarized piezoelectric material can be characterized by several coefficients [36].

The basic simplified form of the polarized piezoelectric ceramic with respect to the relationship of the electrical charge and the mechanical strain, which describe the piezoelectric effect and can be formulated as followings [36],

$$D = d * T + \varepsilon^T * E \tag{3.2}$$

$$S = S^E * T + d * E^T \tag{3.3}$$

where D is the coefficient of an electrical flux density,

T is the coefficient of a mechanical stress,

E is the coefficient of an electric field,

S is the coefficient of a mechanical strain,

D is the coefficient of a piezoelectric charge,

ε^T is the coefficient of a permittivity,

S^E is the coefficient of a compliance or elasticity.

These simplified equations (3.2) and (3.3) can be applied to the small signal model. In addition, mechanical strain (S), electrical field (E), stress (T), and electrical flux density (D) are linear and the coefficients are constant. The coefficients are usually obtained from the piezoelectric material data sheet, and are permittivity (ε), piezoelectric charge, deformation and modulus (d_{ij}), voltage (g_{ij}), elastic compliance (s_{ij}), frequency (N_i), mechanical quality factor (Q_m), and coupling factor (k) [36]. Among these various coefficients, the electromechanical coupling coefficient, k, is

the most important since it denotes how much mechanical energy can be changed into electrical energy or vice versa.

3.2.3 Piezoelectric Materials as Energy Sources

As explained in section 3.2.2, a piezoelectric material can be used as a generator, which converts mechanical energy into electrical energy, as well as an actuator, which converts electrical energy into mechanical. Since this research is focused on energy harvesting from an electrical energy of a piezoelectric material, therefore, this section concentrates on the mechanism of transformation of mechanical energy into electrical energy in piezoelectric materials. Fig. 3.5 shows various working (energy generator) modes of a piezoelectric material [37]. As shown in Fig. 3.5, there are three general directions of force for the material to be working as a generator. Among these, the longitudinal compression mode produces the highest amount of electrical energy conversion and this direction is also called *33*-mode.

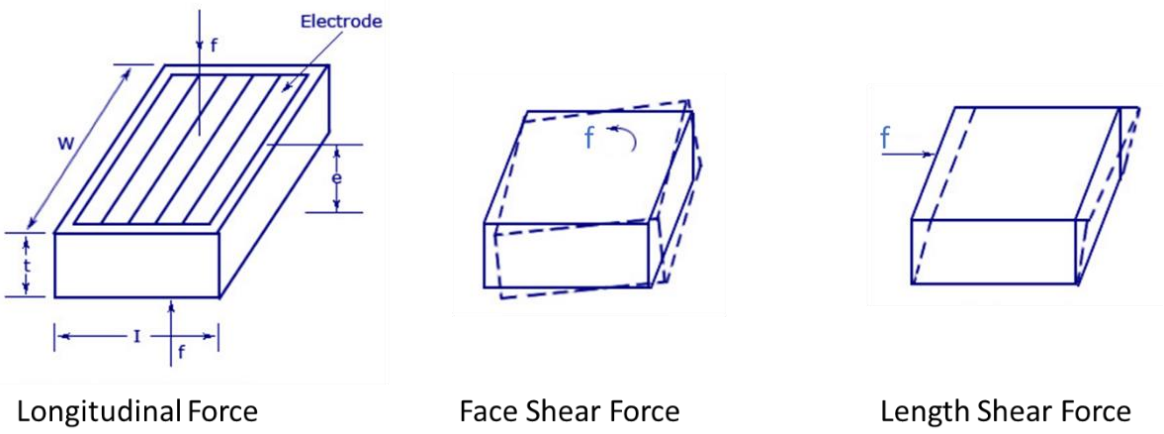


Fig. 3.5 Various working modes of a piezoelectric material [37].

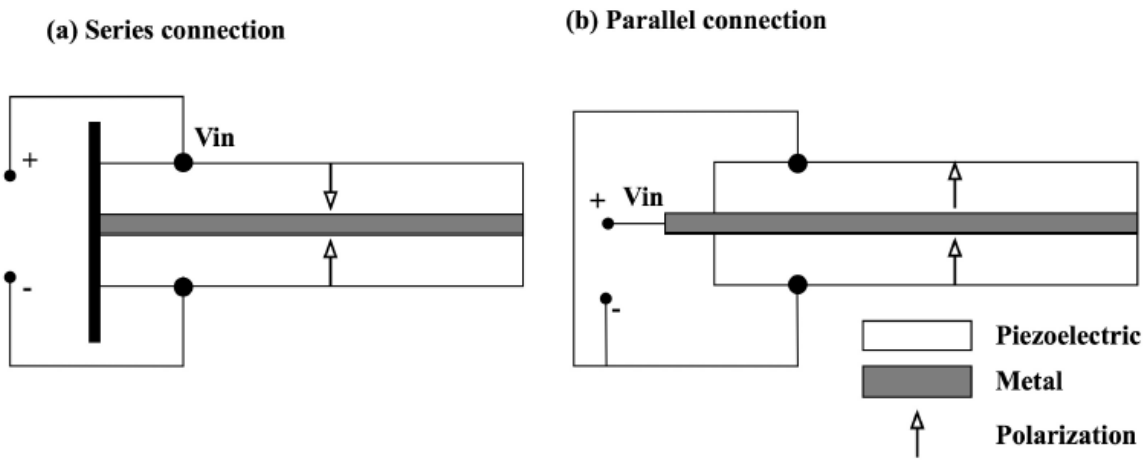


Fig. 3.6 The series and parallel operation of a piezoelectric material [38].

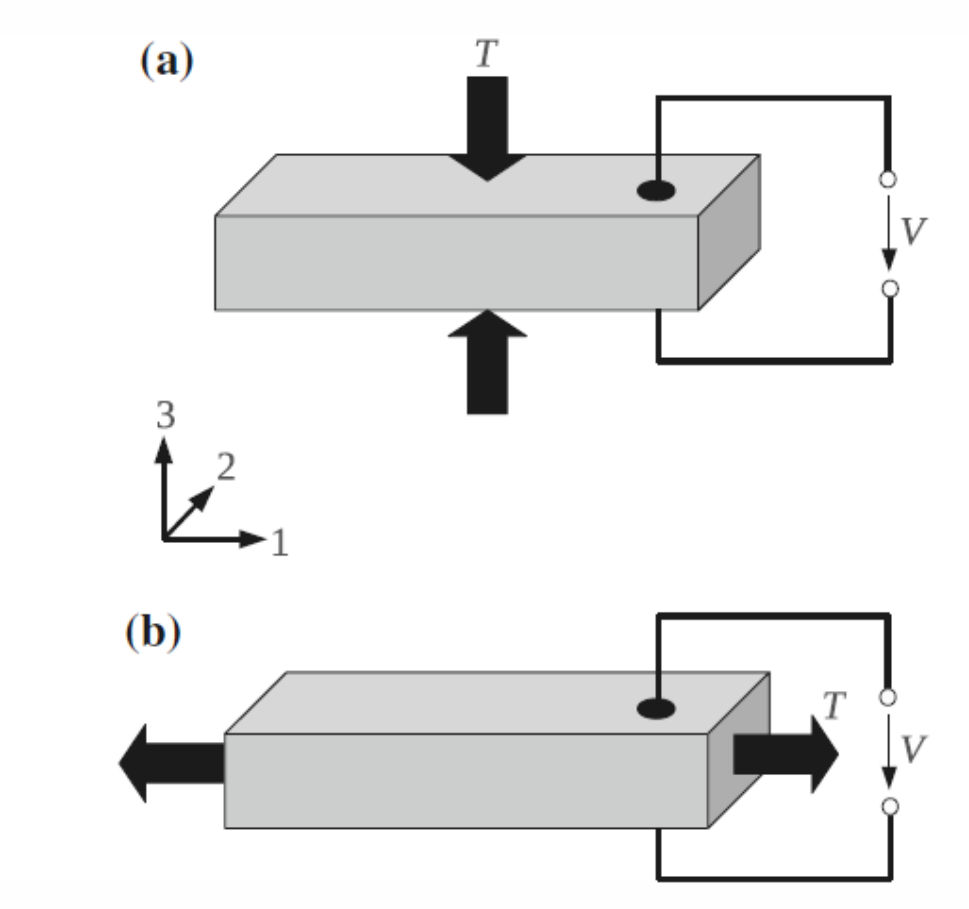


Fig. 3.7 A piezoelectric material operating in (a) *33* mode, and (b) *31* mode [39].

Fig 3.7 shows the two modes of operation, which are *33* and *31* modes [39]. In addition to the direction of the force, there are two modes of operation in a piezoelectric material as an actuator: one is series and the other is parallel. The series and the parallel operations depend on the polarization and wiring shape or configuration of the piezoelectric material layer. If the voltage is applied over the entire piezoelectric layer, then it is called as series operation. If the voltage is applied on each layer of a piezoelectric material, then, it is called as a parallel operation. Fig. 3.6 illustrates the series and parallel operations of a piezoelectric material [38].

CHAPTER 4 – VIBRATION BASED ENERGY HARVESTING CIRCUIT

4.1 Piezoelectric Transducer Modeling

As stated in the previous chapter, a piezoelectric material can be used as a generator, which produces electrical energy by applying mechanical energy as well as an actuator or a motor, which produces mechanical energy by applying electrical energy. In this section, a brief introduction of to the modeling of a piezoelectric material for transforming mechanical energy into electrical energy is presented. Fig. 4.1 shows the models of a piezoelectric transducer in mechanical and electrical domains [39].

In Fig. 4.1, L_M denotes the mechanical mass, C_M represents the mechanical stiffness, and R_M denotes the mechanical losses. A transformer presented in the mechanical domain in Fig. 4.1 allows for conversion of the mechanical stress into current. C_P represents the parasitic capacitance of the piezoelectric material, and R_P denotes the internal loss in an electrical domain.

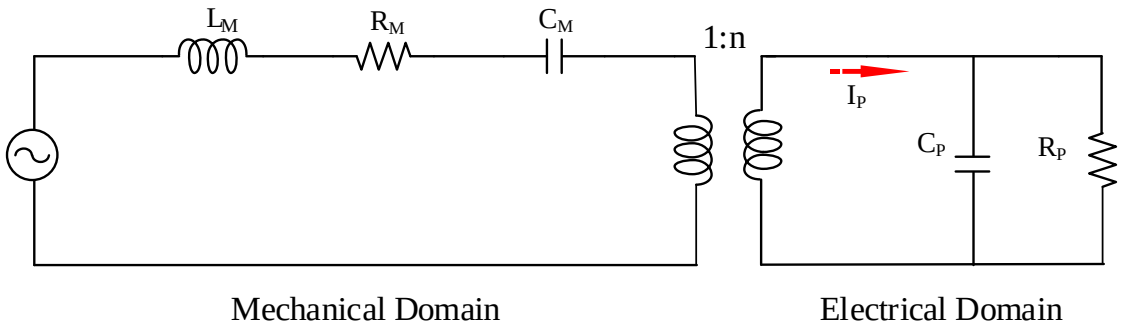


Fig. 4.1 A piezoelectric transducer modeling in a mechanical domain and an electrical domain [39].

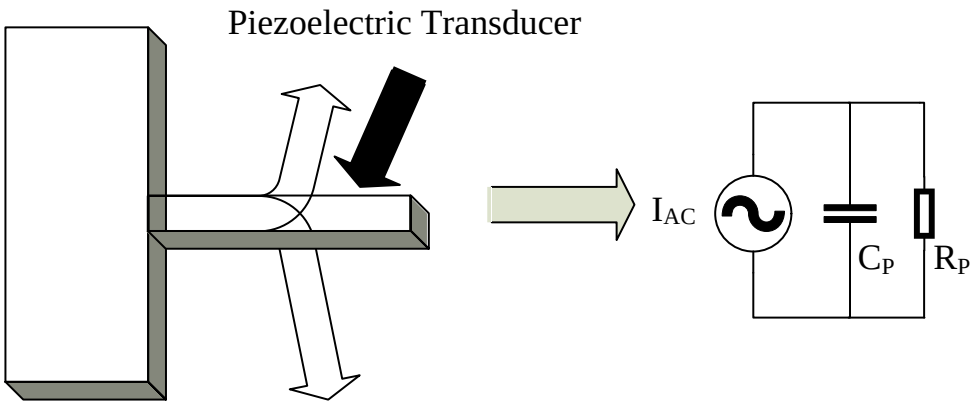


Fig. 4.2 A simplified electrical domain modeling at or close to resonance frequency [40,41].

An electrical domain is transformed at or close to the resonance frequency of a piezoelectric material. Fig. 4.2 shows the simplified electrical domain modeling at or close to resonance frequency of a piezoelectric material [40,41].

When a piezoelectric transducer is agitated by sinusoidal vibrations, it can be modelled by a sinusoidal current source in parallel with a parasitic capacitance, C_P and a parasitic resistance, R_P. The model shown in Fig. 4.1 and Fig. 4.2 represent the general vibration-based piezoelectric energy harvester, which is based on the cantilever design [40,41]. Usually, a cantilever design requires resonance frequency which is based on the working environmental vibration frequency.

In general, a typical power supply or a battery has a very low internal impedance. However, as shown in Figs. 4.1 and 4.2, the internal impedance of a piezoelectric transducer, R_P, has a very high value. As a result, the amount of output current produced by the piezoelectric transducer is limited by this high internal impedance, R_P. The common value of the output current produced by a piezoelectric transducer is in the micro-ampere range. In addition, because of this low current, the output voltage of a piezoelectric transducer is low as well.

The output current of a piezoelectric transducer is proportional to the input vibration amplitude and can be expressed by the following equation which assumes that the input vibration is sinusoidal and therefore,

$$i_P = I_P \sin \omega_P t \tag{4.1}$$

where i_P is equal to I_{AC} in Fig. 4.2, I_P is the peak current of the sinusoidal current source, $\omega_P = 2\pi f_P$, and f_P is the excited frequency of the piezoelectric transducer [42].

4.2 Design of a Piezoelectric Energy Harvester

4.2.1 An AC-to-DC Rectifier Design

There are two kinds of conventional rectifier structures: diode full bridge rectifier and voltage doubler as illustrated in Fig.4.3. The drawback of a conventional structures is the high value of diode turn-on voltage. Since the charging current is the piezoelectric current, i_P, where $i_P = I_P \sin(\omega_P t)$, $\omega_P = 2\pi f_P$ as shown in equation (4.1), is a sinusoidal signal, it needs to charge a parasitic capacitor, C_P before a piezoelectric transducer can transfer the energy to the output. As a result, it causes a problem of wasting energy by charging the parasitic capacitor, C_P.

In addition, due to the diode turn-on voltage, which is in the range of 0.5 V ~ 0.7 V for a conventional diode, a piezoelectric transducer has to overcome this voltage to transfer the power to the output or a load.

In Fig. 4.4, the shaded regions of the red and the blue show the energy loss due to charging and discharging of a parasitic capacitor, C_P, as well as a diode turn-on voltage.

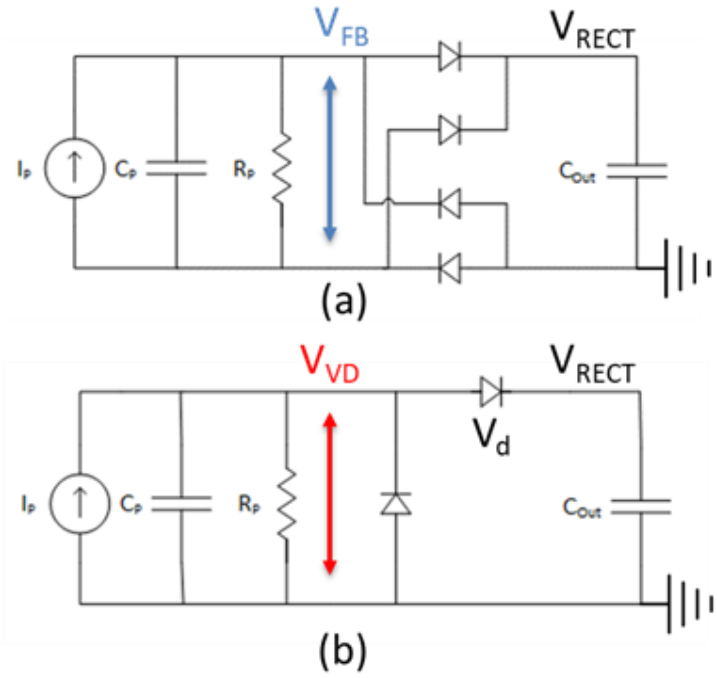


Fig. 4.3 Conventional rectifiers. (a) a full-bridge rectifier (b) a voltage-doubler.

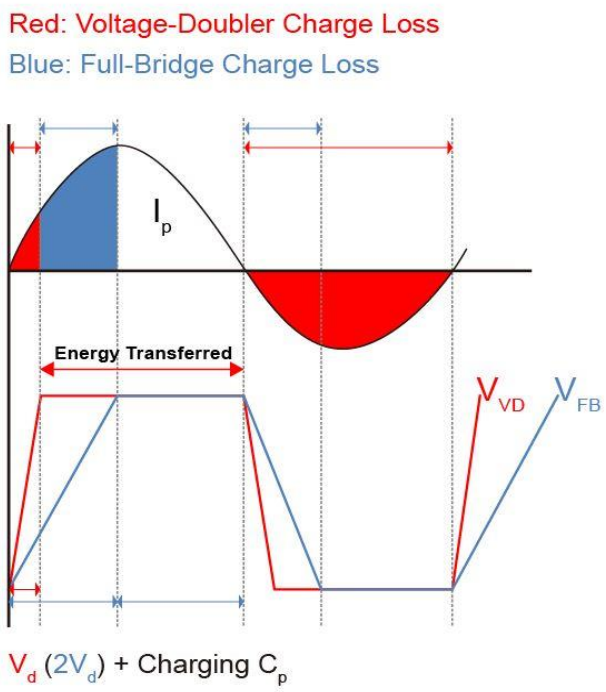


Fig. 4.4 Waveforms of conventional rectifiers.

Fig. 4.4 shows the wave forms of conventional rectifiers. The available power from a conventional full-bridge rectifier as well as a voltage-doubler can be written as following equations (4.2) and (4.3) [42],

$$P_{RECT,FB} = 4C_P V_{RECT} f_P (V_P - V_{RECT} - 2V_d) \quad (4.2)$$

$$P_{RECT,VD} = C_P V_{RECT} f_P (2V_P - V_{RECT} - 2V_d) \quad (4.3)$$

where V_P is the open circuit voltage amplitude of a piezoelectric transducer,

f_P is the resonance frequency of a piezoelectric transducer,

V_d is the diode forward voltage drop,

V_{RECT} is the output voltage of a rectifier,

C_P is a parasitic capacitor of a piezoelectric transducer.

The maximum power that can be harvested from those two topologies can be expressed by following equations (4.4) and (4.5) [42],

$$P_{RECT,FB}\ (MAX) = C_P (V_P - 2V_d)^2 f_P \quad (4.4)$$

$$P_{RECT,VD}\ (MAX) = C_P (V_P - V_d)^2 f_P \quad (4.5)$$

$P_{RECT,FB}$ *(MAX)* and $P_{RECT,VD}$ *(MAX)* occur at $V_{RECT,FB} = \frac{V_P}{2} - V_d$, and $V_{RECT,VD} = V_P - V_d$ respectively.

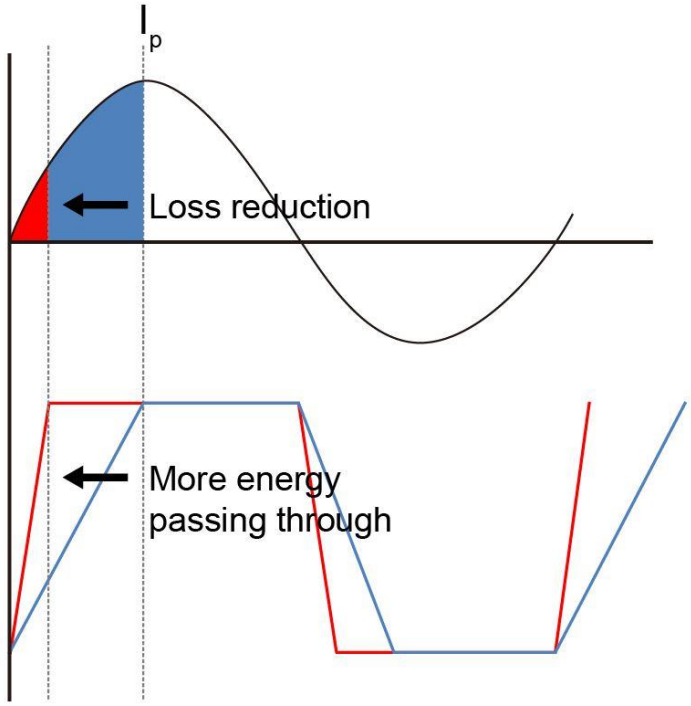


Fig. 4.5 Waveforms showing reduction of energy loss in the proposed rectifier.

As can be seen in Fig. 4.5, reduction of the loss described above and represented by the shaded regions in Fig. 4.3, can result in more energy output from a piezoelectric transducer.

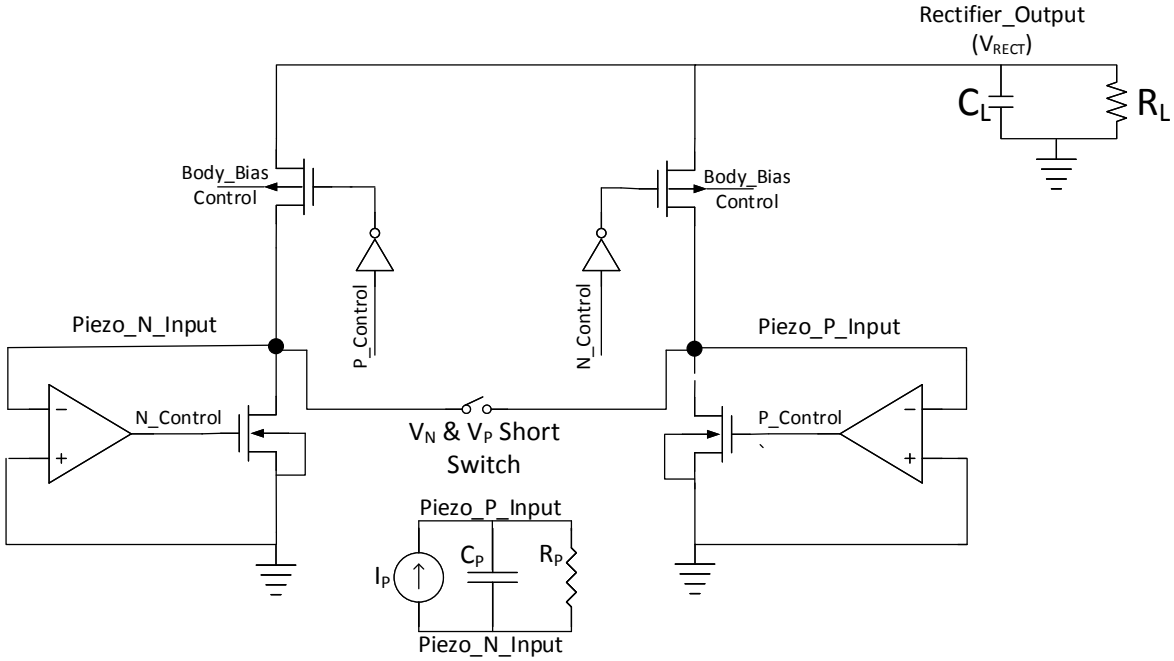
4.2.2 The Proposed AC-to-DC Rectifier Design

As shown in section 4.2.1, conventional structures have problems of a high diode turn-on voltage, which causes a voltage conversion loss as well as charging and discharging a parasitic capacitance C_P, which results in a charge loss. As can be seen in Fig. 4.5, if there is a way to reduce the charging time of a parasitic charge C_P, then one can save quite a bit of energy generated by the piezoelectric transducer. In [43] - [47], researchers presented various techniques. One of the common technique involves lowering of the diode turn-on voltage drop loss. This is typically

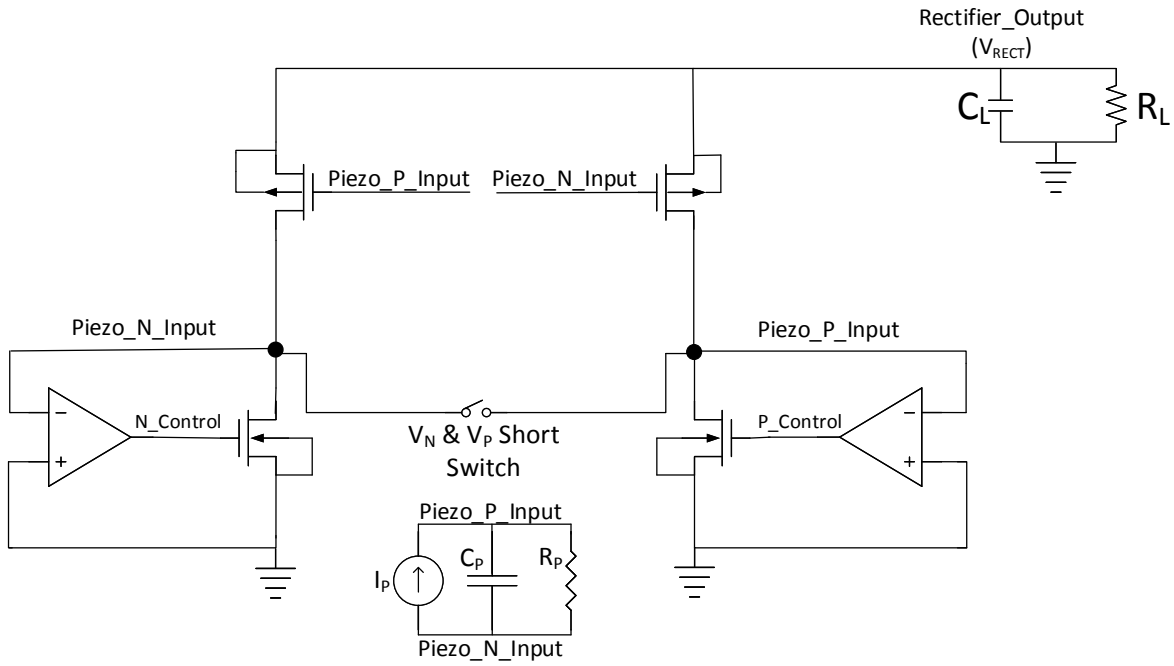
achieved by replacing of the off-chip diode with CMOS switches so that loss due to the high voltage drop can be significantly reduced since the typical diode turn-on voltage is in the range of 0.5 V ~ 0.7 V, which is usually larger than typical threshold voltage, V_{th}, of the MOSFET. Researchers have also proposed various techniques such as a switch-only, a SSHI, a bias-flip, a DSSI, a capacitor integrated switch and so forth. Except for the switch-only topology, all other topologies use either an inductor or a capacitor to store the energy from a piezoelectric transducer whenever it changes polarity. As explained earlier, before the energy can be transferred to the output load, C_P has to charge from zero up to $+(V_{RECT} + 2V_d)$ when I_P is in positive state, while the C_P has to be discharged from $-(V_{RECT} + 2V_d)$ to zero when I_P is in negative state. Therefore, flipping such stored voltage from one end to the other is considered as wasted energy (the energy is used only for charging and discharging of C_P of the piezoelectric transducer). As a result, the above enhanced energy storing topologies have been developed. However, the major problem of such topologies is that they require a large inductor or a capacitor to store energy up to $V_{RECT} + 2V_d$ so that it does not have to suffer from charging and discharging all the way to the end of each positive and negative cycle. In addition, such topologies require very complex circuits to detect and manage inductor and the stored energy in a capacitor. Such complex circuits consume significant amount of energy from a stored output capacitor to control such complex control circuits or even in worst case, they require external voltage source to power up the control circuits.

The proposed active rectifier with switch-only scheme requires no external components other than a piezoelectric transducer and an output load capacitor.

In addition, the harvested power level is moderate compared to such power enhanced topologies. Fig. 4.6 shows the switch-based topologies.



(a)



(b)

Fig. 4.6 An active rectifier (a) the proposed rectifier (b) a cross-coupled rectifier [20], [43], [45].

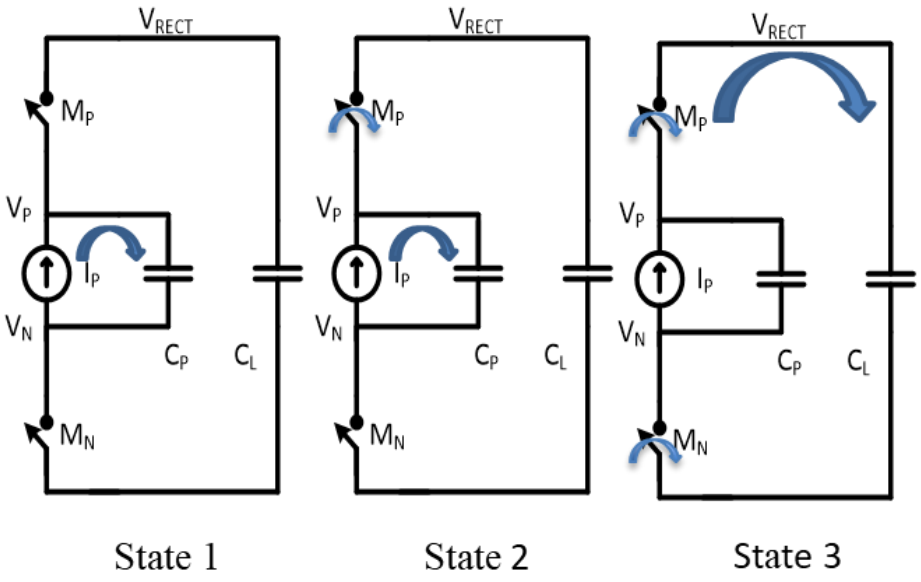
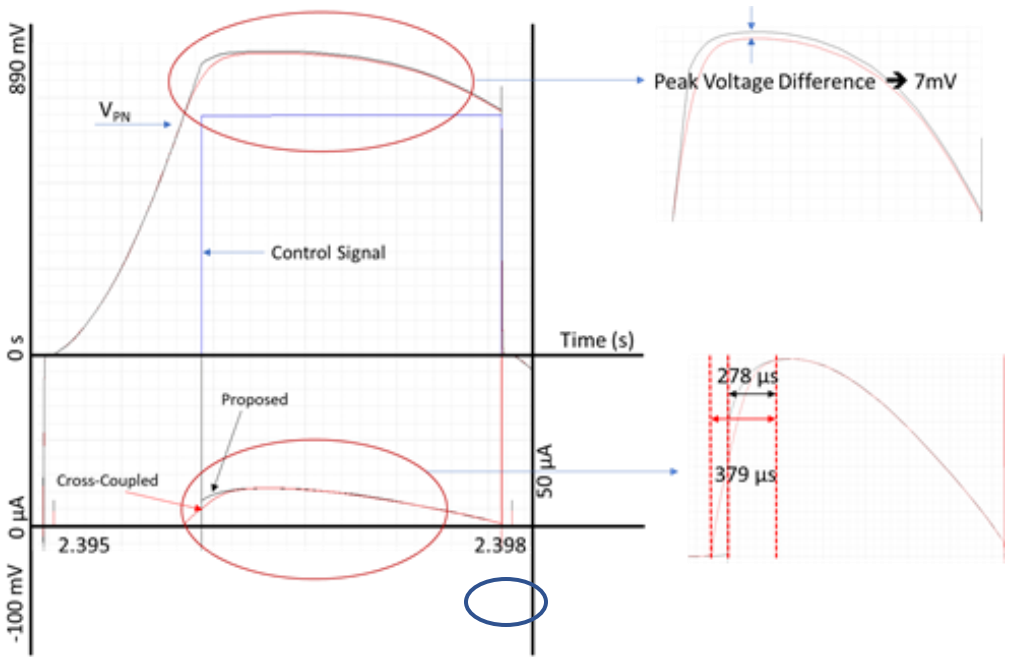


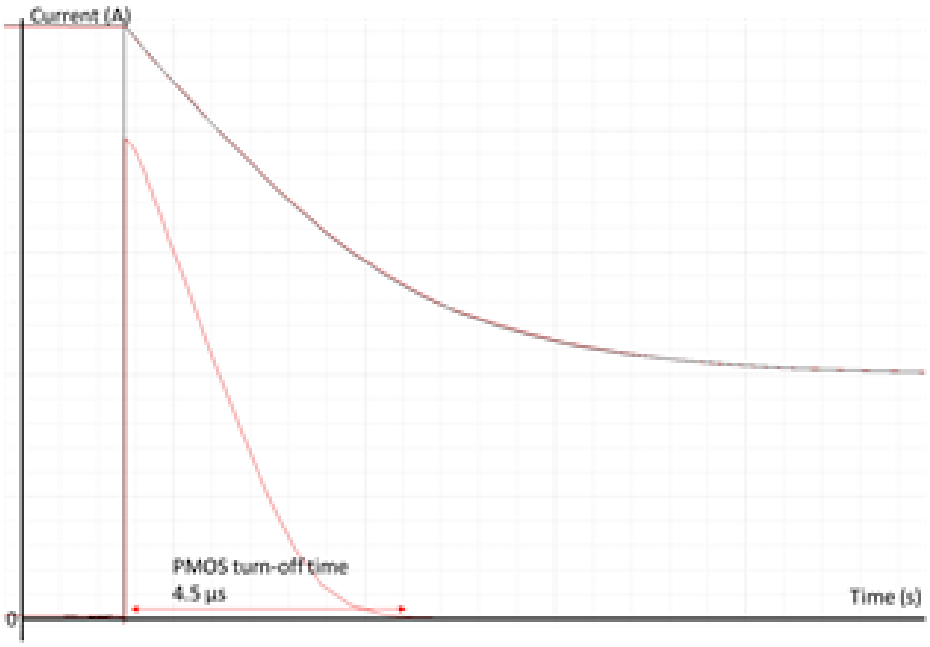
Fig. 4.7 Rectifier operating states.

Fig. 4.6 (a) shows the proposed architecture, and Fig. 4.6 (b) shows the cross-coupled based architecture, and both rectifier circuits are based on a switch topology [20], [43], [45].

The main difference between the schemes shown in Fig. 4.6 (a) and Fig. 4.6 (b) is the method of activating or turning on of the PMOS switches. In Fig. 4.6 (a), a PMOS switch is turned on by the signal of a NMOS switch, which is controlled by the comparator. On the other hand, the circuit shown in Fig. 4.6 (b) is turned on by the threshold voltage of a PMOS. That means, if either V_N or V_P is greater than $|V_{thp}|$ of a PMOS transistor, then a PMOS switch is turned on. The basic operation of the two configurations is same. In the first phase of operation, I_P, the charging current from a piezoelectric transducer charges C_P, which is a parasitic plate capacitor of a piezoelectric transducer and the voltage V_{PN} starts to increase. As soon as I_P finishes charging C_P, it goes to next phase.



(a)



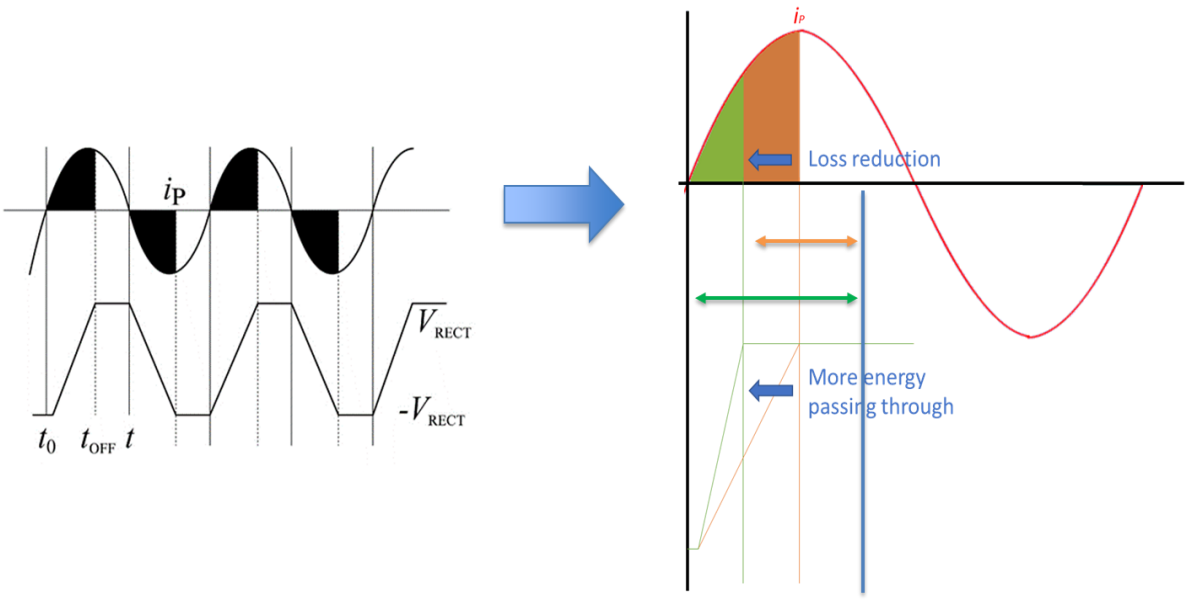
(b)

Fig. 4.8 A comparison of a cross-coupled and the proposed structure. (a) V_{PN} vs. I_P, (b) magnified of blue circle in (a)

At the phase two, V_{PN} of a piezoelectric transducer will be increased further, and if V_{PN} is larger than $|V_{thp}|$, then a PMOS switch starts turning on and begins to transfer the energy into the output capacitor, C_L, of the rectifier. In phase 3, if V_{PN} further increases, then it causes V_N goes to zero or below zero.

As a result, the comparator starts turning on. Therefore, a NMOS switch is turned on as well. Fig. 4.7 shows the active rectifier working states. The states 1 through 3 apply to the cross-coupled active rectifier reported in [20], [43], [45], as well as in the most of systems, which utilize active rectifier structures. However, there is a minor difference between the proposed and the power enhanced structures mentioned previously. The proposed structure goes though the state one, but state two and three are merged together in the proposed structure, which saves available input amplitude or power from a piezoelectric transducer. Since the PMOS switch of the proposed active rectifier is controlled by the NMOS turn-on signal, it does not have to go through state 2 in the ideal case. Even, in real case, the delay due to the buffer is very short (~ 10 ns) resulting in very short duration of the state 2. In state 2, a cross-coupled structure has to wait until V_{PN} is large enough to exceed the $|V_{thp}|$ of a PMOS so that it can turn on PMOS switch properly. In addition, the current from a piezoelectric transducer has to charge C_{sg} of the PMOS switch. This charging action of a parasitic capacitance, C_{sg} causes two problems. First, from the stand point of a piezoelectric transducer, C_{gs} can be considered as another load. Second, since a piezoelectric transducer should charge the gate capacitance, C_{sg}, the available current from a piezoelectric transducer is reduced by the amount of wasted charges to charge C_{sg}. Therefore, the total available time to transfer the power to the output has been reduced.

Fig. 4.8 shows the comparison of V_{PN} versus I_P of a piezoelectric transducer. The time to reach to peak available current from a piezoelectric transducer is indicated in Fig. 4.8 (a).



(a) (b)

Fig. 4.9 Loss reduction in the parasitic plate capacitance, C_P.

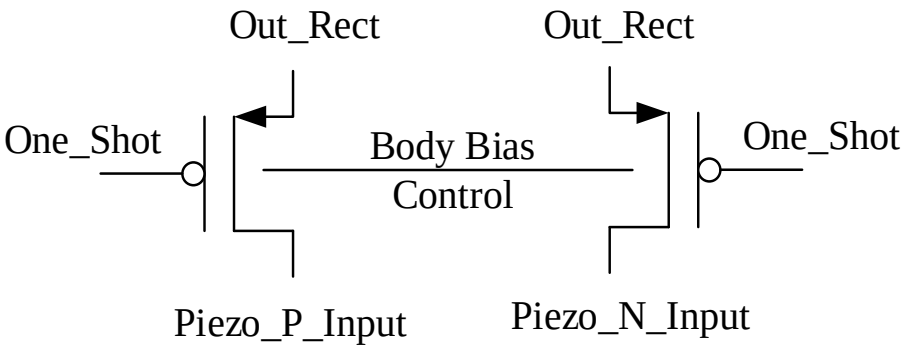
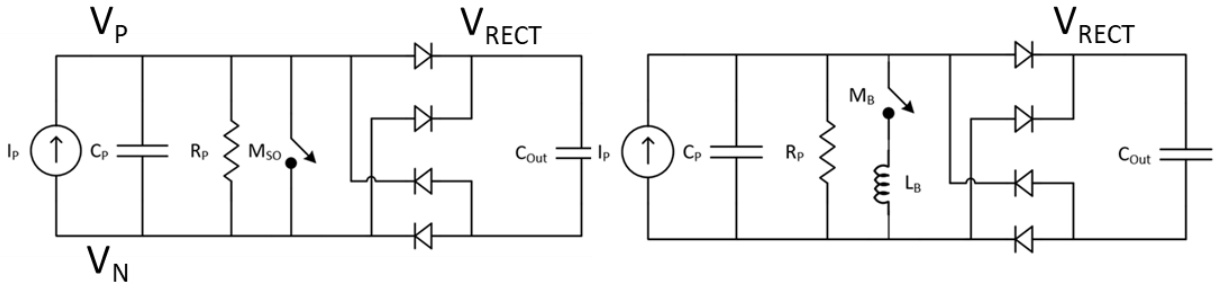


Fig. 4.10 A schematic of the piezoelectric transducer switch.

From this waveform, it can be observed that the proposed system shows that the time to reach the peak current reaching is 100µs lower than the proposed system in [20], [43], [45]. This means that the total available time of power to transfer to the output of the active rectifier has been increased.

In addition, this shortening of the time to reach the peak current can slightly boost the output voltage of the active rectifier. Therefore, more available power can be transferred in respect to the load. Fig. 4.8 (b) shows the off-time of a PMOS switch. This figure indicates that turning-off time is also significantly reduced. Therefore, possible loss of power induced by this discharging action can be reduced as well compared to other proposed structures in [20], [43], [45].Fig. 4.10 shows the switch inserted in between V_N and V_P of a piezoelectric transducer input. As explained earlier, a parasitic plate capacitor of C_P should charge up to $+(V_{RECT} + 2V_d)$ in a positive cycle of I_P and discharge down to $-(V_{RECT} + 2V_d)$ in a negative cycle of I_P before a piezoelectric transducer can transfer energy to the output load capacitor, C_L. This means that in every cycle, C_P causes the problem of wasting charges. Therefore, many researchers try to find a way to reduce this charging and discharging time [39] – [47].



(a) (b)

Fig. 4.11 (a) A switch-only configuration (b) An inductor based bias-flip configuration [20], [48].

Fig. 4.9 (a) shows a conventional rectifier waveform with charge losses in black shaded region, and Fig. 4.9 (b) shows the charge reduction in green shaded region. As shown in Figs. 4.9 (a) and 4.9 (b), if the shaded region can be reduced from the orange shaded region to the green shaded region as shown in Fig. 4.9 (b), the available power transfer time can be increased.

Therefore, more power can be transferred to the output load capacitor, C_L. In order to achieve this reduction of wasting charges caused by a C_P can be achieved by inserting a switch in between V_N and V_P of a piezoelectric transducer input as shown in Fig. 4.10 charges [14].

Fig. 4.11 shows the two example of reduction techniques of charging and discharging of C_P. In Fig 4.11 (a) is the technique that has been used in this proposed active rectifier, and Fig. 4.11 (b) in another example of enhancing the power extraction using an inductor [14], [40]. The switch shown in Fig. 4.10 is inserted in between V_P and V_N as shown in Fig. 4.11. From Fig. 4.9 (a), a charge loss in every cycle for a conventional rectifier can be calculated following equation,

$$Q_{\frac{\text{lost}}{\text{cycle}}} = 2C_P\left(V_{RECT} - (-V_{RECT})\right) = 4C_P V_{RECT} \tag{4.6}$$

And, a charge loss in every cycle for a switch-only rectifier as shown in Fig. 4.11 (a) can be calculated as,

$$Q_{\frac{\text{lost}}{\text{cycle}}} = 2C_P V_{RECT} \tag{4.7}$$

Similarly, a charge loss in every cycle for a bias-flip rectifier as shown in Fig. 4.11 (b) can be calculated as,

$$Q_{lost/cy} = 2C_P V_{RECT}(1 - \varepsilon^{\frac{-\pi\beta}{\omega}}) \quad (4.8)$$

$where\ \beta = \frac{R_B}{2L_B},\ \omega = \sqrt{(\omega_o^2 - \beta^2)},\ \omega_o = \frac{1}{\sqrt{L_B C_P}}$

R_B is a parasitic resistance of an inductor, L_B.

From equations (4.6) through (4.8), it can be observed that the bias-flip rectifier topology has the lowest charge loss. However, there is one problem with Fig. 4.11 (b) configuration. The problem is that since this topology uses an inductor, the charge loss totally depends on an inductor. That means, if an inductor is large enough, this topology can significantly reduce charge loss due to the action of charging and discharging of C_P and store this energy into an inductor. However, for a small inductor, the improvement is only slight. As a result, to make it work properly, size of an inductor should be large enough and this causes significant amount of space taken by an inductor. In addition, since this kind of topology uses an inductor, very complex control circuit is required to detect the inductor current as well as turn on/off the switch inserted in between an inductor. Therefore, in a low available input power in the proposed structure, the switch-only topology is better option since it requires less complex control circuit compared to bias-flip one as well as it does not require any off-chip components other than the input piezoelectric transducer and an output load capacitor, C_L.

The control signal generator that is used for controlling a circuit shown in Fig. 4.10 is relatively simple. It takes the signal from two comparators, which control the bottom NMOS in Fig. 4.6 (a), and are fed into the one-shot generator. Whenever I_P crosses a zero point, the one-shot signal generator generates a short pulse which allows to turn on the circuit shown in Fig. 4.10. As a result, this short pulse helps shorten the voltage between V_P and V_N, and it allows reduction of

the time to charge C_P as explained earlier. Fig. 4.13 shows the simulation results of an active rectifier with switch-only configuration. The operation states of the proposed full-wave rectifier can be broken down into three parts. In phase 1 of interval at t_0 to t_1, the sinusoidal current of a piezoelectric transducer, i_P starts charging the parasitic capacitor, C_P.

In contrast to a conventional piezoelectric transducer as shown in Fig. 4.6 (b), charging time of C_P has been cut down significantly because of the inserted switch in between V_P and V_N nodes.

In Fig. 4.12, it can be observed that as the one-shot is turned on, V_P and V_N nodes are shorted instantly. As a result, it does not have to charge or discharge from its previous stored value in C_P, but rather it begins from zero. For example, in a typical rectifier, when i_P is flipping its polarity from positive to negative, C_P should release its stored charges from ($V_{RECT} + 2V_d$) to zero and it should be charged back from zero to $-(V_{RECT} + 2V_d)$. In phases 2 and 3, because charging a parasitic capacitor C_P has been acquired, the energy can be delivered to the output capacitor, C_L through the proposed full-wave rectifier.

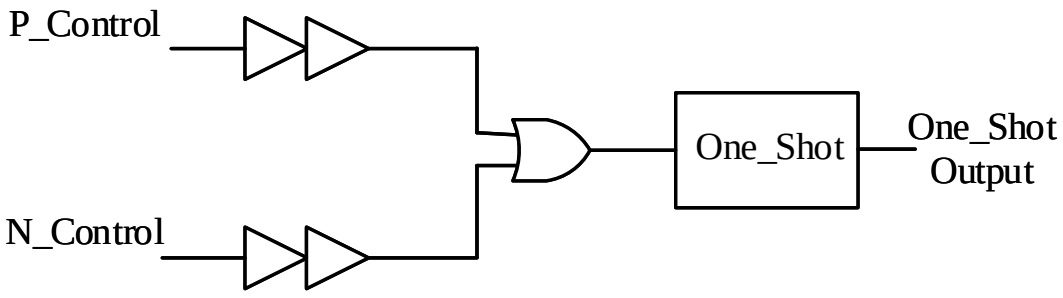


Fig. 4.12 A schematic of the one-shot control circuit.

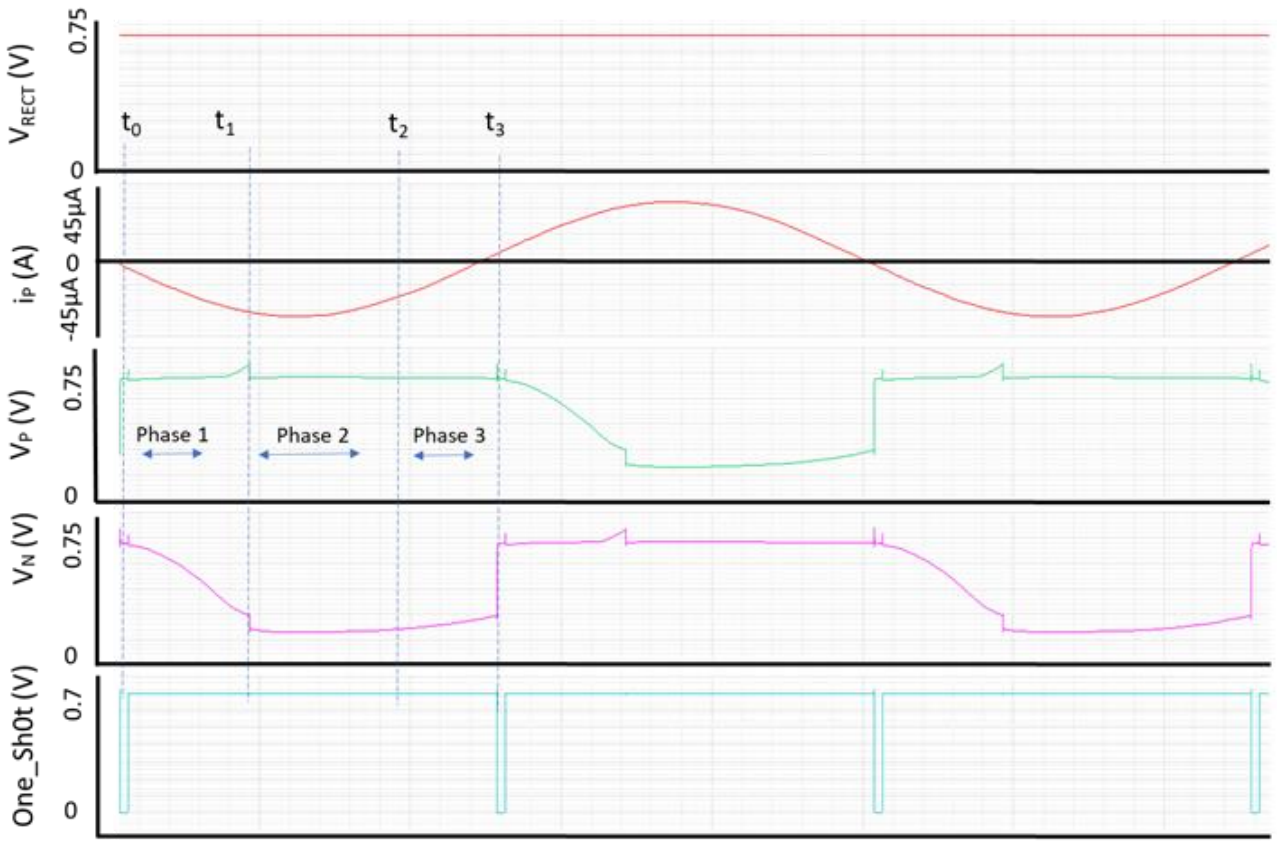


Fig. 4.13 Simulated waveforms of a piezoelectric transducer.

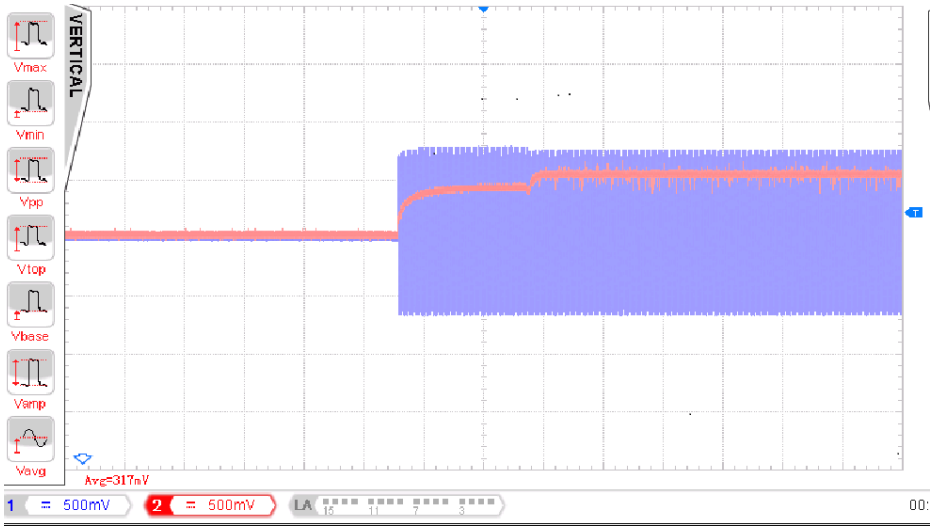


Fig. 4.14 Measured waveforms of V_{RECT} and input voltage from a piezoelectric transducer.

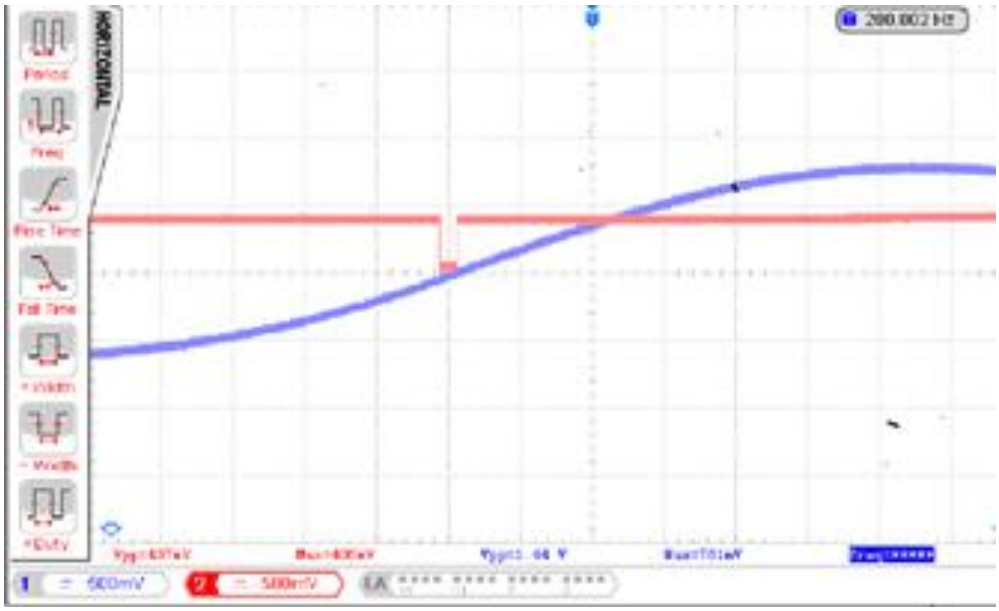
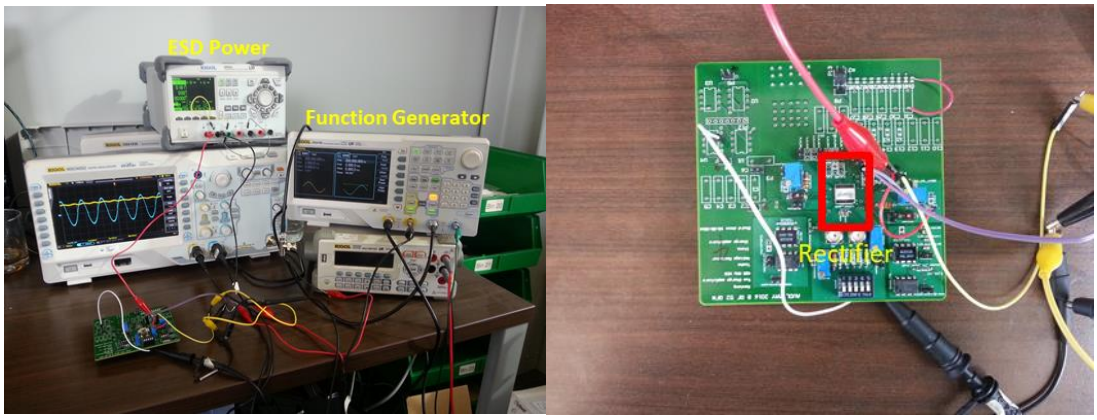


Fig. 4.15 Measured waveforms of one-shot voltage and input voltage from a piezoelectric transducer.



(a) Test set-up (b) PCB

Fig. 4.16 Test set-up and PCB.

Fig. 4.10 shows the inserted switch between V_P and V_N nodes of a piezoelectric transducer which helps capacitor to discharge to zero quickly.

The working principle of the one-shot signal generator is fairly simple. Whenever a piezoelectric transducer voltage swing is crossing the zero voltage, the one-shot control circuit is producing a short one-shot pulse which allows shorting the input ports of a piezoelectric transducer and this one-shot signal resets the voltage of V_P and V_N.

The output voltage in Fig. 4.13 is 0.694 V, and the voltage conversion efficiency is 98.7 %. The power conversion of this systems is 52.2 %.

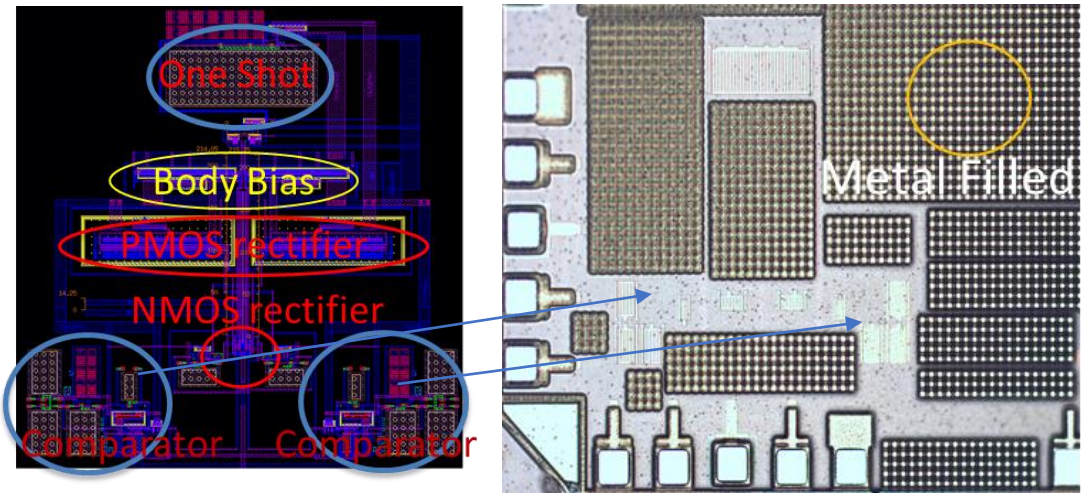
In Fig. 4.14, the red line represents the output voltage of the proposed system, which is V_{RECT}, and blue line represents the input voltage from the piezoelectric transducer.

Fig. 4.15 shows the waveform of a piezoelectric transducer as well as one-shot pulse signal. As can be seen from this waveform, one-shot generates low signal when the piezoelectric transducer crosses a zero point, which will save power by shorting the piezoelectric transducer inputs, V_P and V_N.

Fig. 4.16 shows the test sets up as well as the PCB for the proposed rectifier, and Fig. 4.17 shows the layout as well as the chip microphotograph. The overall size of chip is 540 µm x 540 µm. Table 4.1 shows the performance comparison.

As can be seen from the table, the input voltage of the proposed full-bridge rectifier is the lowest. In addition, the input power from a piezoelectric transducer is the lowest. However, the overall efficiency of a proposed system is very comparable with other systems reported in literature. In addition, this proposed system demonstrates that it can take very low input available power and convert it to moderate usable power. The proposed system does not require any external

component except for the output load capacitor. In addition, the proposed system is powered by the output voltage generated by itself.



(a) Layout (b) Chip

Fig. 4.17 (a) Layout and (b) chip microphotograph.

Table 4.1 Performance Comparison

Publications	**[14],SO**	**[35]**	**[37]**	**This Work**
Inductor and External Components	No	Yes	No	No
External Power	No	Yes	No	No
Amplitude of I_P by PD or Applied force	3.35 g	2 mA	188 µA	45 µA
Parasitic Capacitance of PD	12 nF	330 nF	25 nF	25 nF
Vibration Frequency	225 Hz	185 Hz	200 Hz	200 Hz
$V_{IN,Peak}$	2.4	3.5	3	0.704
V_{OUT} (V)	2	3.34	2.9	0.694
R_L (KΩ)	75	3.51	50	45
PCE (%)	53	53.4	65	52.2

CHAPTER 5 – RADIO FREQUENCY BASED ENERGY HARVESTING CIRCUIT

5.1 Radio Frequency Energy Harvesting

Radio frequency (RF) is one of the most widely used technology nowadays. RF or wireless energy in the electromagnetic waveform can be divided into two categories: non-radiative energy, and the radiative energy [49]. The example of a non-radiative energy is magnetically coupled near-field inductive coils [49]. A non-radiative energy transfer demands that to transfer the energy in between the devices, two devices must be in close proximity to each other for proper energy transfer operation. In addition, the operating frequency of this method is limited to around a few MHz ranges. In general, a non-radiative method of energy transfer has relative high efficiency since the air loss or energy transfer loss in between the devices is relatively low compared to a radiative energy transfer method [49,50]. The example for a radiative or far-fields energy transfer method is the one that will be discussed and explored in this research.

Since the radiative energy transfer typically occurs between the two devices which are farther apart compared to those in a non-radiative or near-field energy transfer method, there exists significant amount of air or energy transfer loss as well as low energy density of the received energy. However, despite the low available energy density and low efficiency of a far-field energy transfer method, a radiative or far-field energy transfer method has been receiving its own attention because of the advantage that it can transfer energy or receive energy remotely as well as in all directions. Currently, RF or far-field radiative technology is available basically everywhere in the forms of wireless internet connections, and mobile communications [51]. In addition, there are various applications such as medical sensors, commercial sensors and industrial sensors etc. Since

the development of the concept of IoT, researchers are trying to deploy RF into more electronic devices and applications which was never thought to be possible before [51]. In addition, the communication systems that we are currently used is within the license-free Industrial, Scientific and Medical (ISM) frequency band (300 MHz to 3 GHz). Therefore, plenty of RF energy can be accessed wherever the wireless technology is deployed [52,53]. Despite of such advantages of the availability of RF signals many problems associated with RF signals still exist. A major problem associated with design of a RF energy harvesting system is that there is a free-space path loss over the distance through the air. A free-space loss is called as the Friis transmission loss which can be formulated by equation (5.1). Therefore, the free-space path loss is [53],

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi d}\right)^2 \tag{5.1}$$

where P_r denotes a received power,

P_t denotes a transmitted power,

G_t and G_r denote the antenna gain for both transmitter and receiver,

λ denotes a signal wavelength, and

d denotes a distance between antennas.

From the equation (5.1), it is easy to notice that the received power is inversely proportional to the distance, d. In addition, the available received power depends on the wavelength, λ and the antenna gains, G_t and G_r. The antenna gains as well as the wavelength are typically fixed. As a result, the distance, d, is very important factor that determines the maximum available power with respect to the receiver side. Therefore, as a distance between the transmitter and the receiver increases, the available maximum power in a receiver side decreases significantly. In addition,

according to the U.S. Federal Communications Commission (FCC) regulations, there exists a maximum transmittable power limitation in every frequency bands [54]. For example, frequency ranges from 300 MHz to 1.5 GHz, power density should not exceed $\frac{f}{300}$ mW/cm^2, where f is frequency [54]. Therefore, the maximum available power at around 900MHz, which is the frequency range of interest for this work, is about 4W, and the same power level is applied to 2.45 GHz as well according to the FCC regulations [54]. As a result, for example the maximum available power at 2.4 GHz will go down to approximately 100 μW at 10 m and 10 μW at 20 m away from a transmitter, which usually depends on the antenna gain and other factors usually.

In this chapter, the energy harvesting using this widely available but limited RF energy source with a DC-to-DC boost converter will be implemented with the idea of a maximum power point tracking method to achieve the maximum available power from the receiver.

5.2 The Antenna Modeling

In a transmitter as well as in a receiver side, radio frequency is transmitted and received in the form of basically a sine wave signal. Therefore, to utilize this sine wave signal as a power source, an AC-to-DC rectifier is required. There are many ways to rectifying AC signal but because of the available frequency ranges, which are usually in the range of 800 MHZ to 3 GHz, the commonly used techniques of rectifying RF AC signal cannot be implemented simply because of high frequency of the signal. Since the signal from a transmitter is usually very weak in terms of the voltage amplitude level, there should a way to boosting such a low-level voltage amplitude signal into proper voltage amplitude level so that a rectifier composed with CMOS transistors can

operate. In addition, as can be seen in equation (5.2), the overall efficiency of the rectified power versus received power depends on the efficiency of a rectifier if received power is fixed [55],

$$\eta_{eff} = \frac{P_{Rect}}{P_r} * 100 \tag{5.2}$$

where P_{Rect} is rectified power, and

P_r is received power from an antenna.

Therefore, designing an efficient RF rectifier is very important part of the work. Before discussing the actual design of a RF AC-to-DC rectifier, one needs to understand the role of an antenna since it is the first and the beginning point of a RF energy harvesting system. An antenna is that facilitaes the interconnection of wireless energy and a RF energy harvesting system. That means, an antenna works as a transducer by converting electromagnetic energy into electrical energy on a receiver side, and vice versa on a transmitter side. Therefore, choosing or designing a right antenna is very crucial issue even though designing an antenna is out of scope in this research. Equation (5.1) expresses the actual received power from the antenna. In addition to the received power efficiency, the antenna radiation efficiency can be calculated using equation (5.3) [55],

$$\eta_{rad-eff} = \frac{P_{rad}}{P_{received}} \tag{5.3}$$

where P_{rad} is representing the radiated power by the antenna, and

$P_{received}$ is representing the power received or accepted by the antenna.

P_{rad} can be calculated by integrating the power density in a closed surface with radius, r [55]. $P_{received}$ is the actual power that the antenna receives or transmitts. The radiation efficiency of an antenna can be further divided into two parts: η_{cond} and $\eta_{eleelectric}$. Therefore, $\eta_{rad\text{-}eff}$ can be expressed as $\eta_{rad\text{-}eff} = \eta_{cond} * \eta_{dielectric}$. The conductivity efficiency, η_{cond}, can be modeled with the antenna radiation resistance, R_{rad}, and the loss resistance, R_{loss}. The antenna radiation resistance, R_{rad}, represents only the dissipated power into free-space or so called, air, and it is not incorporated with any structural resistance in the antenna. The loss resistance, R_{loss}, represents the power dissipated by the antenna itself. As a result, it could be considered as a conduction loss in the antenna. Therefore, the conductivity efficiency, η_{cond}, can be expressed as in equation (5.4) [55],

$$\eta_{cond} = \frac{R_{rad}}{R_{rad}+R_{loss}} \tag{5.4}$$

The dielectric efficiency, $\eta_{eleelectric}$, is very hard to calculate and is intensively depends on element around an antenna. Therefore, in this dissertation, it is assumed that that antenna is surrounded by air, which is considered as free-space. In free-space, the dielectric efficiency, $\eta_{eleelectric}$, is considered as 1. As a result, $\eta_{rad\text{-}eff}$ becomes $\eta_{rad\text{-}eff} = \eta_{cond}$.

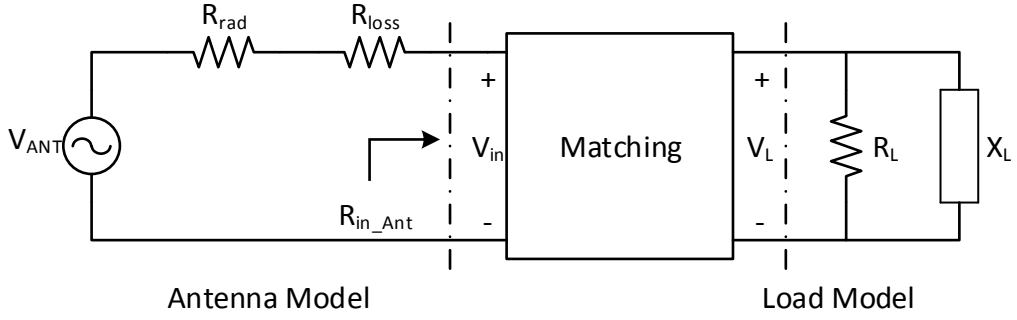


Fig. 5.1 The antenna and the load model.

To better understand the antenna, the simplified antenna model as shown in Fig. 5.1 can be used. As can be seen in Fig. 5.1, the antenna has its own internal loss, R_{ANT}, where the R_{ANT} is R_{rad} + R_{loss}.

In addition, the power achieved by the antenna can be calculated as the following equation in (5.5) [55],

$$P_{ANT} = \frac{(V_{in})^2}{2R_{ANT}} \tag{5.5}$$

where V_{in} can be expressed as V_{ANT} / 2, and

R_{ANT} is R_{rad} + R_{loss}.

Combing the equation (5.1) and the equation (5.5), one can get V_{ANT} as following equation (5.6) [55].

$$V_{ANT} = \sqrt{(8P_{ANT}R_{ANT})} \tag{5.6}$$

From the equation (5.6), it can be concluded that the lower value of P_{ANT} due to decreasing $\eta_{rad\text{-}eff}$ will result in a lower V_{ANT}. Lowering the efficiency of the antenna comes from the additional $R_{loss.}$ As a result, designing an antenna or finding a proper antenna should be carefully considered with minimum R_{loss} coefficient. Using the equation (5.6), estimate the voltage from the antenna can be estimated according to the power received. For example, if a received power in the antenna is -10 dBm (100 μW), the voltage, V_{ANT}, will be around 99.9 mV with a 50 Ω antenna system. In

section 5.2.1, design a RF AC-to-DC rectifier and impedance matching, which is very important in a RF energy harvesting system design, are discussed.

5.3 A Radio Frequency Rectifier

As shown in Fig. 5.2, a RF AC-to-DC rectifier that composed of CMOS transistors or passive elements should be presented in between an antenna, a matching network and a storage device or a regulator [56]. Since the RF signal received through the antenna is an AC signal, a rectifier should be placed so that receiving AC signal can be properly rectified to a DC source to be used as power sources for the subsequent system modules or for charging the storage devices. In reference [57], the author demonstrated that at -15 dBm of an input power, the end-to-end power conversion efficiency (PCE) of the system can be around 7 % with this topology.

However, the problem is that as the input power is getting higher and higher, the leakage current will be also increase. This higher leakage is induced because of the turn-on mechanism of a NMOS and a PMOS transistor. Since in this structure, there is a time when a NMOS and a PMOS transistors are turned on simultaneously, as a result, a shoot-through current will exist.

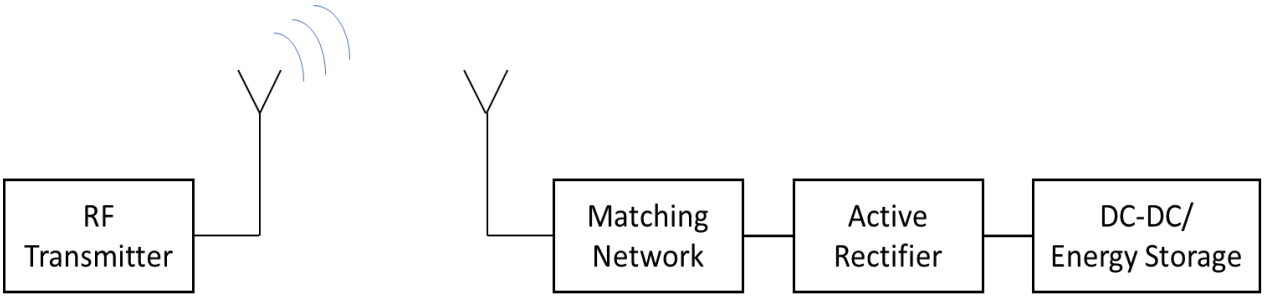


Fig. 5.2 A general wireless power transfer scheme.

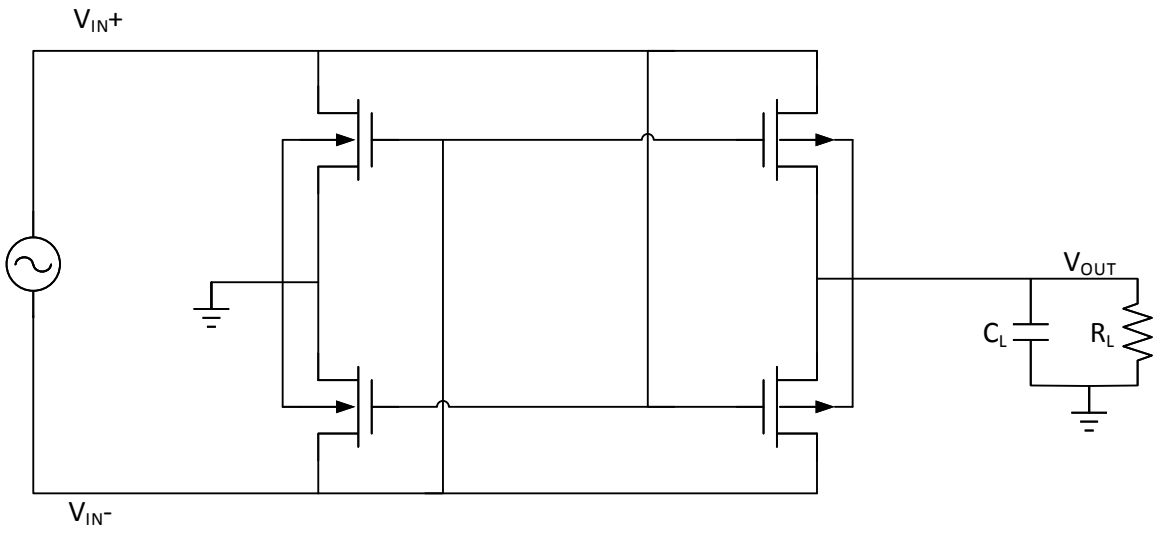


Fig. 5.3 A conventional cross-connected active rectifier [56].

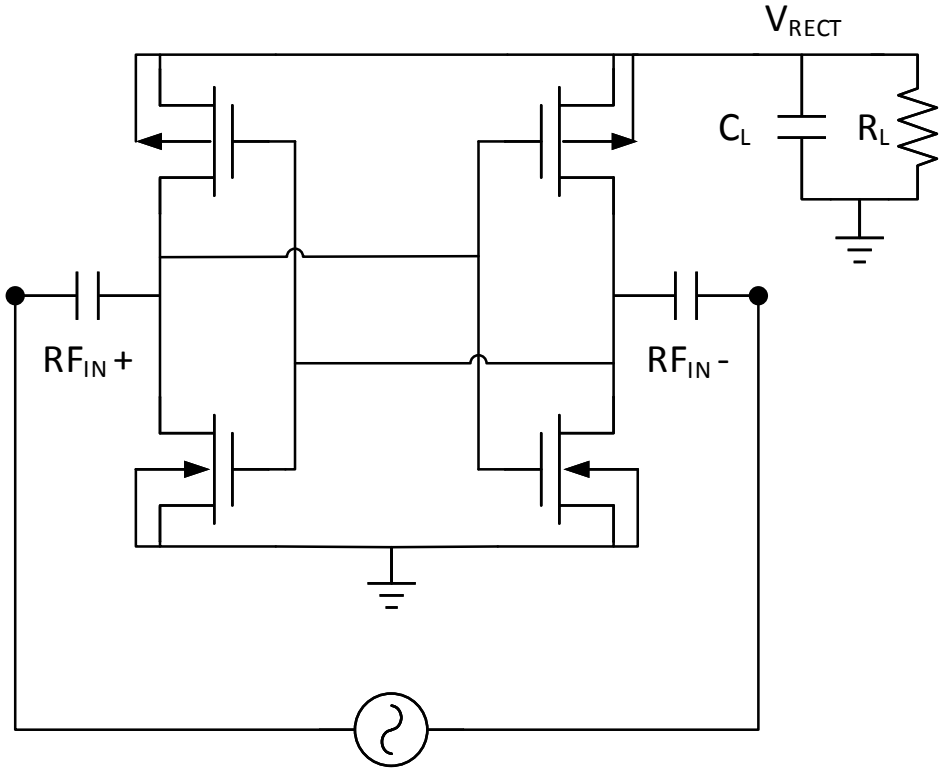


Fig. 5.4 A RF cross-coupled active rectifier used in the proposed RF energy harvesting system.

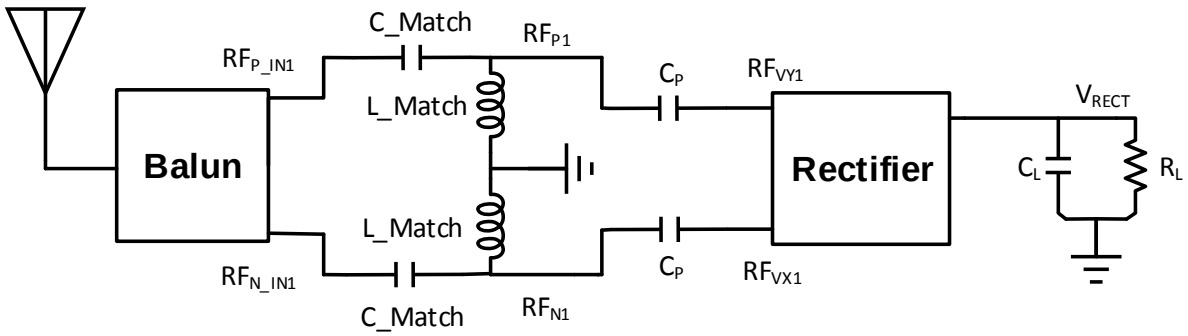


Fig. 5.5 The complete circuit of front end of a RF energy harvesting system.

Fig. 5.5 shows the complete circuit diagram of the input part RF energy harvesting system including an active rectifier as well as a matching network in between the antenna and the RF AC-to-DC rectifier.

The power from an antenna can be modelled as an AC sinusoidal voltage source (V_{ANT}) in series with a resistance loss, R_{ANT}. The voltage amplitude generated by the antenna can be expressed as [57,58],

$$V_{ANT} = 2\sqrt{2R_{ANT}P_{ANT}} \tag{5.7}$$

where P_{ANT} is power from the antenna.

In addition, the minimum power that should be applied to achieve a required V_{in_RECT} can be calculated in equation (5.8) [57,58],

$$P_{ANT} = \left(\frac{R_{ANT}+R_{real_RECT}}{X_{imag_RECT}}\right)^2 \left(\frac{V_{in_RECT}^2}{8R_{ANT}}\right) \quad (5.8)$$

where R_{ANT} is the sum of internal resistances, R_{loss} and R_{rad},

R_{par_RECT} is the input impedance real part of a RF rectifier, and

X_{imag_RECT} is the input impedance imaginary part of a RF rectifier.

Due to the fact explained above, a high PCE can be obtained from this structure but the range of the high PCE will be limited. Fig. 5.3 shows the rectifier structure that has been used in reference [56].

Fig. 5.4 shows the rectifier used in this proposed RF energy harvesting system. As explained before, a cross-connected structure can produce relatively high PCE with limited available input power ranges.

From equation (5.7), it can be seen that as P_{ANT} is getting lower, V_{ANT} is also reduced. From Table 5.1, if the available power from an antenna is below -6 dBm, the voltage coming from an antenna is too low to operate a rectifier [59]. For example, at -11 dBm, the amplitude of voltage from an antenna is only 89mV and obviously, this voltage is not enough to turn-on a MOSFET.

From equation (5.8), it is easy to notice that the real part of the input impedance, R_{real_RECT}, and imaginary part, X_{imag_RECT} can be adjusted to achieve a proper value of P_{ANT}. Therefore, the equation (5.8) indicates that proper sizing of a MOSFET is very important. As it has been shown in equation (5.7), with such a low available voltage amplitude from RF rectifier input, operating a RF rectifier is a major problem. To resolve this low available input voltage amplitude from a RF rectifier, an impedance matching network is used which acts as one of the most important parts in a RF rectifier design.

Table 5.1 RF Power Versus Voltage in 50 Ω Systems [59]

Input (dBm)	Power (mW)	V_{rms} (mV)	V_{peak} (mV)	V_{pk-pk} (mV)
-11	0.0794	63.021	89.112	178.223
-10	0.1	70.711	99.985	199.97
-9	0.126	79.339	122.185	224.37
-8	0.158	89.019	125.874	251.747
-7	0.2	99.881	141.232	282.465
-6	0.251	112.069	158.465	316.931
-5	0.316	125.743	177.801	355.602
-4	0.398	141.086	199.496	398.992
-3	0.501	158.301	223.838	447.677
-2	0.631	177.617	152.151	502.301
-1	0.974	199.29	281.796	563.591
0	1	223.607	316.18	632.36
1	1.26	250.891	354.76	709.094

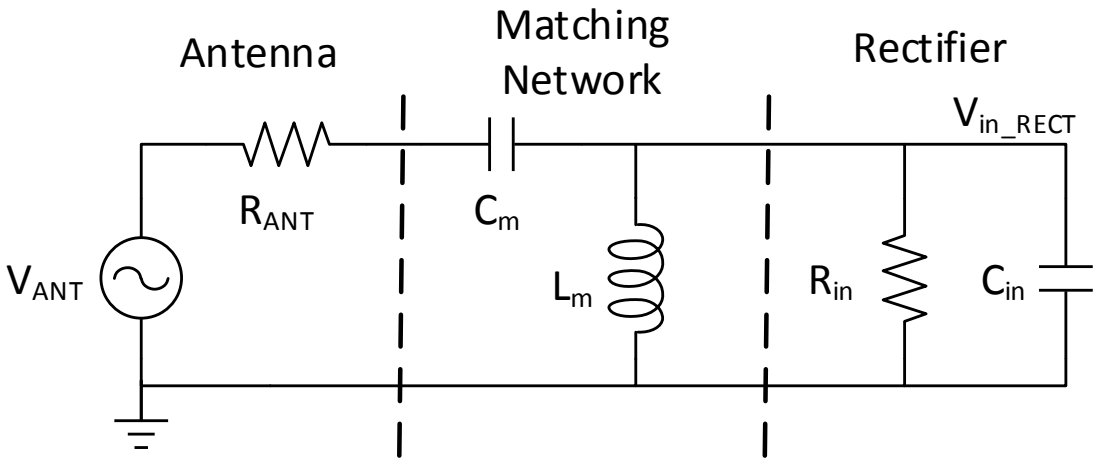


Fig. 5.6 A matching network in between an antenna and a rectifier.

There are two roles for a matching network: serving as a matching impedance between the antenna and the input of a RF rectifier and working as a voltage boosting from a RF rectifier. Matching an impedance in between the antenna and the RF rectifier is very important to minimize loss due to mismatch of two different impedances. As mentioned earlier, because of the low available input voltage from an antenna, it is very important to increase such low voltage to an adequate voltage level so that a RF rectifier can properly work.

There are several types of impedance matching networks such as shunt inductor, *L* network, and transformer [60]. In this design, L-matching network has been chosen as shown in Fig. 5.6 because of its simplicity as well as ease of tuning a network. The matching network C_m and L_m can be calculated using equation (5.9) through (5.11) [60,61],

$$C_m = \frac{1}{\omega_r R_{ANT}} \sqrt{\frac{R_{ANT}}{R_{in} - R_{ANT}}} \tag{5.9}$$

$$L_m = \frac{R_{in}}{\omega_r} \frac{1}{\omega_r R_{in} C_{in} + \frac{1}{\sqrt{\frac{R_{ANT}}{R_{in} - R_{ANT}}}}} \tag{5.10}$$

where $\omega_r = \frac{1}{\sqrt{LC}}$

$$\text{Gain} = \frac{V_{in_RECT}}{V_{ANT}} = \frac{1}{2}\sqrt{\frac{R_{in}}{R_{ANT}}} \tag{5.11}$$

From equations (5.9) through (5.11), it can be concluded that if $R_{in} > R_{ANT}$, then, the voltage from a matching network can be boosted. To calculate a proper value of C_m and L_m, following calculation procedure need to be processed.

1. Select a suitable gain to get a desired value of $V_{in_RECT.}$
2. From the equation (5.11), select an arbitrary R_{ANT}. From this R_{ANT}, the R_{in} can be calculated.
3. From given value of $\boldsymbol{\omega}_r$, and C_{in}, C_m and L_m can be evaluated from the equation (5.9) and (5.10).
4. Go back and start from 1 following proper simulation.

From above steps of calculation and by trial and error simulation, the proper value of network can be obtained. The values, which has been chosen in this design are that C_m is 550 fF, and L_m is 45 nH. In addition, a capacitor C_p has been chosen as 45 nF in Fig. 5.5. Further trimming is required with the impedance measurement tool so that the impedance of rectifier can be measured exactly. In Fig. 5.7, sizes of PMOS and NMOS should be chosen carefully since if the size of the MOSFET is too big then, the input power will be wasted or dissipated by charging C_{sg} of a PMOS transistor and C_{gs} of a NMOS transistor.

Table 5.2. Transistor Sizes for RF Rectifier Circuit

MOSFET	Size (µm)	Number of Fingers
PMOS	50/0.12	100
NMOS	20/0.12	40

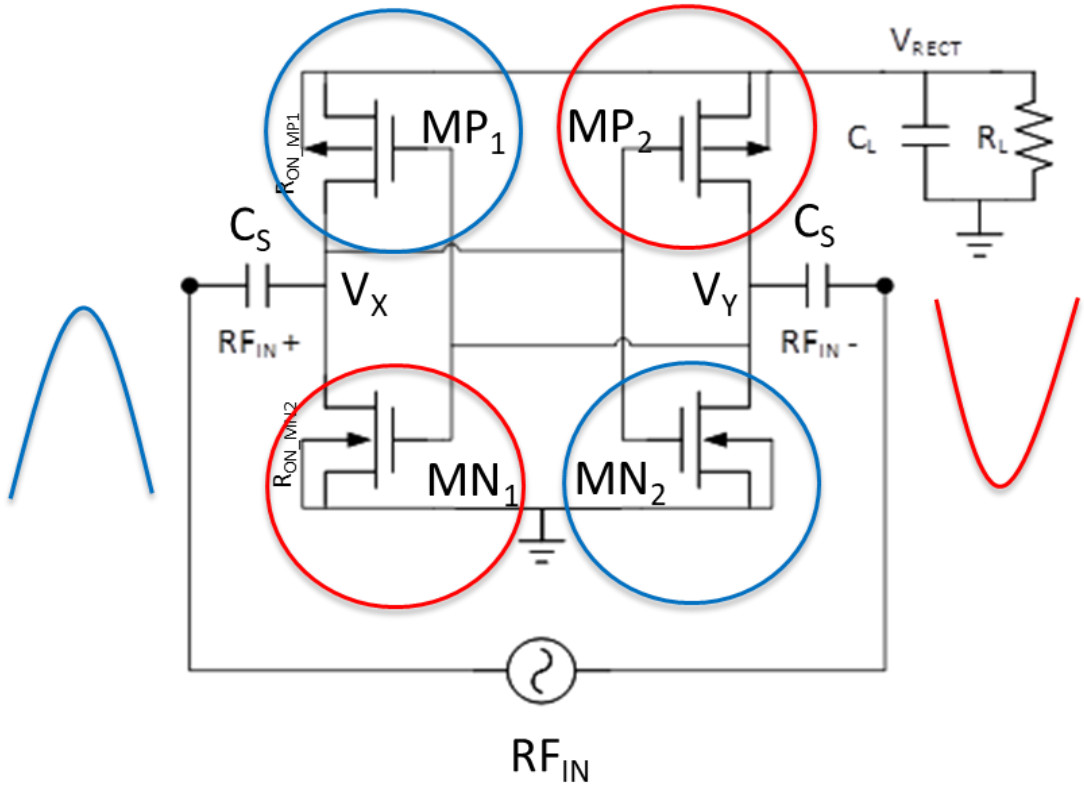


Fig. 5.7 Operation of the proposed RF rectifier in each input cycle.

Similarly, if MOSFET sizes are too small then it will increase R_{on}. As a result, this increased R_{on} will result in higher loss in V_{ds}, which will cause lower output voltage, V_{RECT} in Fig.5.7. With all the reasons that explained above, careful simulation is also required to achieve right sizes of MOSFET switches.

Using trial and error simulations with arbitrary sizes of PMOS and NMOS, the optimized sizes PMOS and the NMOS have been chosen as shown in Table 5.2.

Fig. 5.7 shows the operation of the proposed RF rectifier in each cycle of the RF input. A blue circle shows the positive cycle or a discharging phase, and a red circle shows the negative cycle or a charging phase. Fig. 5.8 shows the circuit diagram in half-wave (RF input) as well as the charging and discharging phase in each RF input cycle.

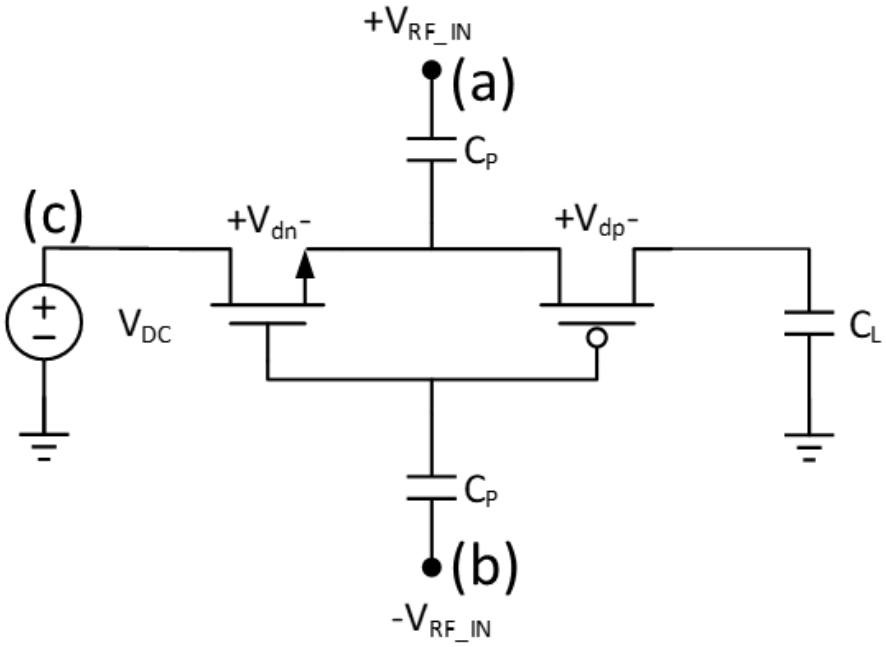
The output voltage of a proposed RF rectifier can be calculated by applying a KVL, and it is shown in the following equations (5.11) and (5.12). At charging state shown in Fig. 5.8 (b), V_{cp} can be expressed as,

$$V_{cp} = -V_{RF_IN} + V_{dn} - V_{DC} \tag{5.11}$$

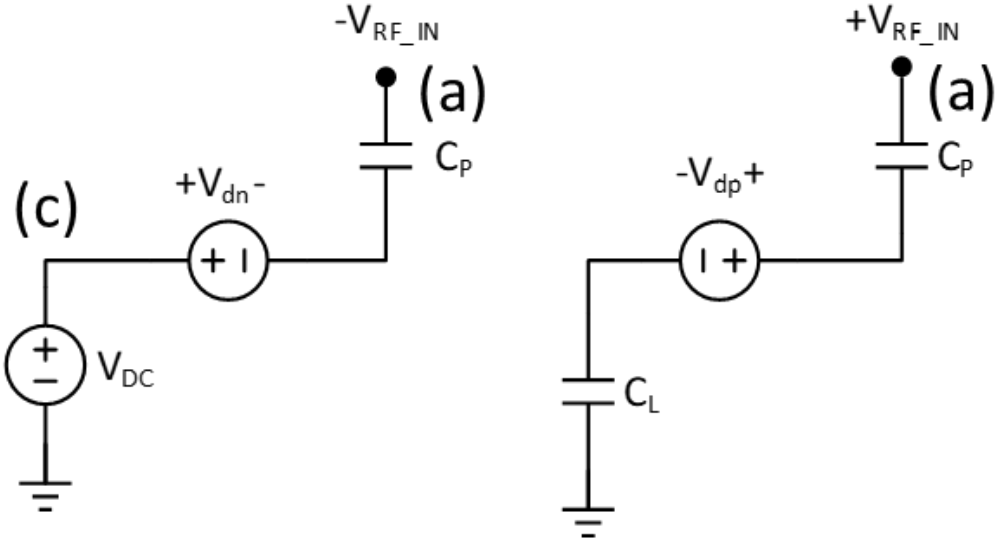
At discharging state shown in Fig. 5.8 (c), V_{RF_IN} can be expressed as,

$$V_{RF_IN} = V_{cp} + V_L + V_{dp} \tag{5.12}$$

To obtain the load voltage V_{Cap} at load capacitor C_L or V_{RECT} of the proposed RF rectifier, the equation (5.11) should be combined with the equation (5.12). Therefore, V_{Cap} or V_{RECT} can be expressed as,



(a) Half-circuit



(a) Charging Phase (c) Discharging Phase

Fig. 5.8 Break down of the proposed RF rectifier, (a) Half-cycle schematic (b) Half-cycle voltage operation.

$$V_{Cap}\ or\ V_{RECT} = 2V_{RF_IN} + V_{dc} - (V_{dn} + V_{dp}) \tag{5.13}$$

As it can be seen from the equation (5.13), the final output voltage, V_{RECT}, of the proposed RF rectifier is twice that of an input voltage, RF_{Input}. In addition, equation (5.13) shows that if the voltages V_{dn} and V_{dp} which are related to the R_{on} of a PMOS as well as a NMOS (MP_1, MP_2, MN_1, and MN_2 in Fig. 5.7) are reduced, the output voltage can be even more optimized or reach higher value. From. Fig. 5.8, it can be recognized that the available voltage to turn on the MOSFET in each cycle is only around 300 mV or less. As a result, MP_1, MP_2, MN_1, and MN_2 are in subthreshold region during most of their operating ranges. The drain-to-source current in subthreshold operation is shown in equations (5.11) through (5.12),

$$I_{DS-MP1_MN2} = \mu_{0-MP1,MN2} C_{ox-MP1,MN2} \left(\frac{W_{MP1,MN2}}{L_{MP1,MN2}}\right)\left[(V_{GS-MP1,MN2} - V_{th-MP1,MN2})V_{DS-MP1,MN2} - \left(\frac{V_{DS-MP1,MN2}}{2}\right)^2\right] \tag{5.14}$$

$$I_{DS-MP2_MN1} = \mu_{0-MP2,MN1} C_{ox-MP2,MN1} \left(\frac{W_{MP2,MN1}}{L_{MP2,MN1}}\right)\left[(V_{GS-MP2,MN1} - V_{th-MP2,MN1})V_{DS-MP2,MN1} - \left(\frac{V_{DS-MP2,MN1}}{2}\right)^2\right] \tag{5.15}$$

Equations (5.5) and (5.6) express R_{on} of MP_1, MP_2, MN_1, and MN_2.

$$R_{ON-MP1,MN2} = \left(\frac{1}{\frac{\partial(I_{DS-MP1,MN2})}{\partial(V_{DS-MP1,MN2})}}\right) = \frac{\left(\frac{L_{MP1,MN2}}{W_{MP1,MN2}}\right)}{\mu_{0-MP1,MN2} C_{ox-MP1,MN2}(V_{GS-MP1,MN2} - V_{th-MP1,MN2} - V_{DS-MP1,MN2})} \tag{5.16}$$

$$R_{ON-MP2,MN1} = \left(\frac{1}{\frac{\partial(I_{DS-MP2,MN1})}{\partial(V_{DS-MP2,MN1})}} \right) = \frac{\left(\frac{L_{MP2,MN1}}{W_{MP2,MN1}}\right)}{\mu_{0-MP2,MN1} C_{ox-MP2,MN1} \left(V_{GS-MP2,MN1} - V_{th-MP2,MN1} - V_{DS-MP2,MN1}\right)} \quad (5.17)$$

Equations (5.16) and (5.17) can be used to calculate the desired W/L ratio to achieve a proper R_{on} of all MOSFETs. In addition, equations (5.14) through (5.17) indicate that choosing right MOSFET transistors such as low-threshold MOSFETs can help achieve better low-input power sensitivity as well as proper operation of MOSFETs. After all the MOSFET sizing as well as the passive elements values of the matching network are calculated, the simulated impedance versus input power is obtained as shown in Fig. 5.9.

Finally, the RF_{VX1} and RF_{VY1}, which are the inputs of a RF cross-connected rectifier show roughly two times of the RF_{P1} and RF_{N1} since this cross-connected configuration has the output of $2V_{in}$ approximately. In designing a RF rectifier, choosing a right MOSFET is very important. If the voltage from a matching network is low, which comes from the low available input power of an antenna, then this input voltage may not sufficient to turn on the MOSFET switches in a rectifier.

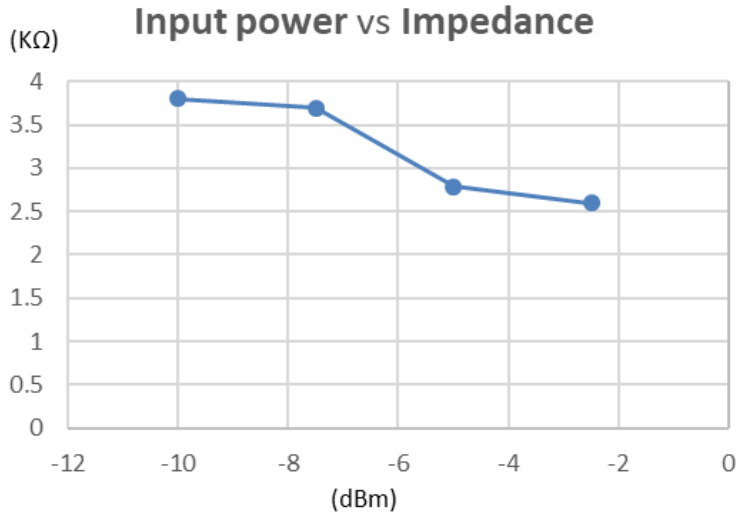


Fig. 5.9 Input power versus impedance of the RF rectifier

Therefore, low threshold MOSFET transistor should be chosen to guarantee operation even in a low available input voltage. However, as the voltage from an antenna is increased, because of the natural structural problem of a cross-connected rectifier, a leakage current or a shoot-though current will be increased resulting in even higher leakage current with low threshold voltage devices. If a normal or a high threshold voltage MOSFET is used, then a rectifier cannot take a low input voltage from an antenna. In this design, a low threshold design has been chosen because of a low input available voltage from an antenna. Fig. 5.12 shows the simulation of a rectifier representing a load versus efficiency. The simulation has been done with 1.5dB loss of a balun at 920MHz of a RF input frequency. In this RF energy harvesting system, finding an optimum load impedance is one of the most important tasks for designing the energy harvesting system.

As can be seen from waveforms, as the loads of a rectifier changes, the efficiency also changes due to the change of an impedance in the RF rectifier. Table 5.3 shows that the efficiency is getting lower as expected. Highest efficiency can be achieved at -10 dBm of the input available RF power.

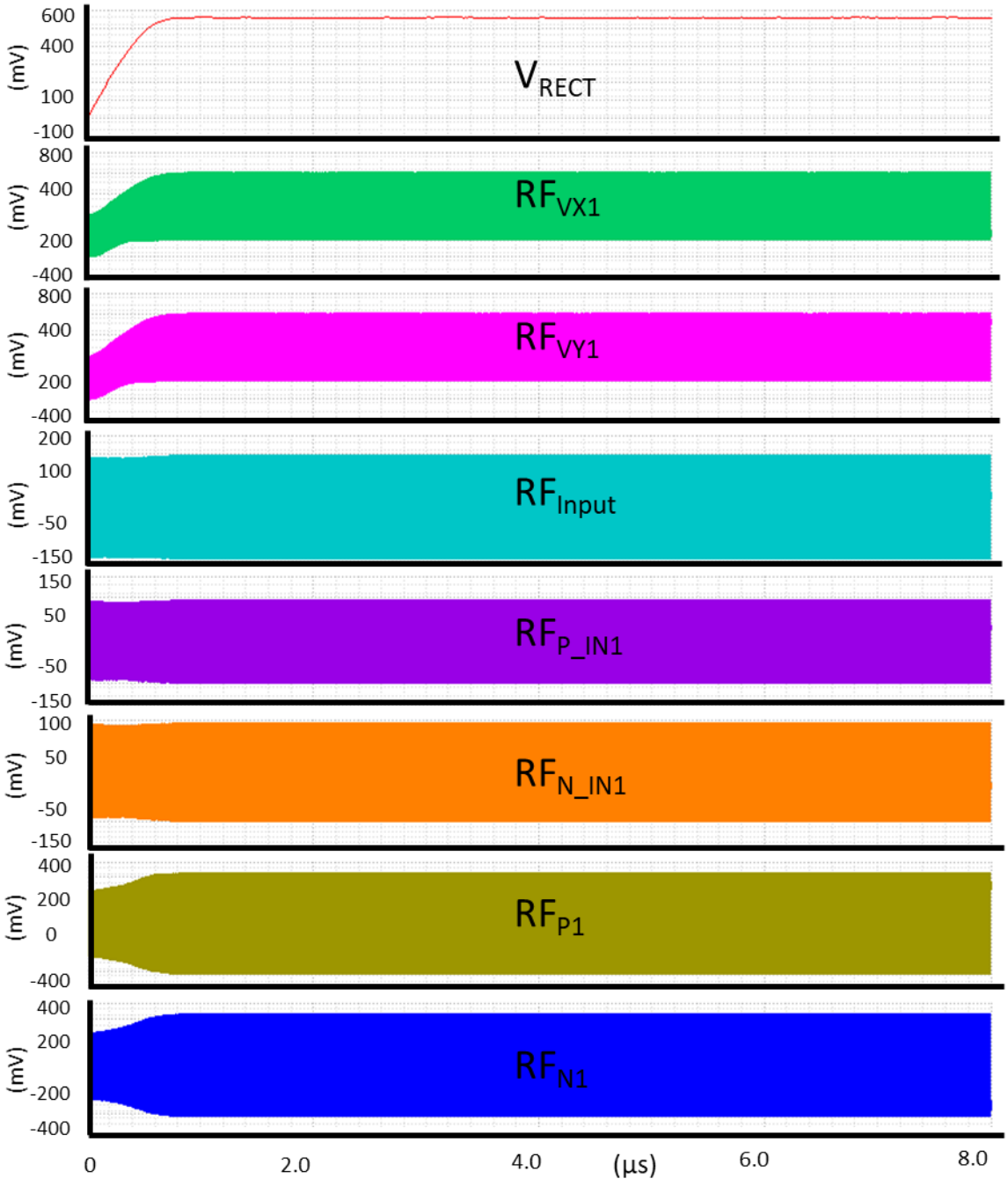


Fig. 5.10 Waveforms of the circuits in Fig. 5.4 at -10 dBm.

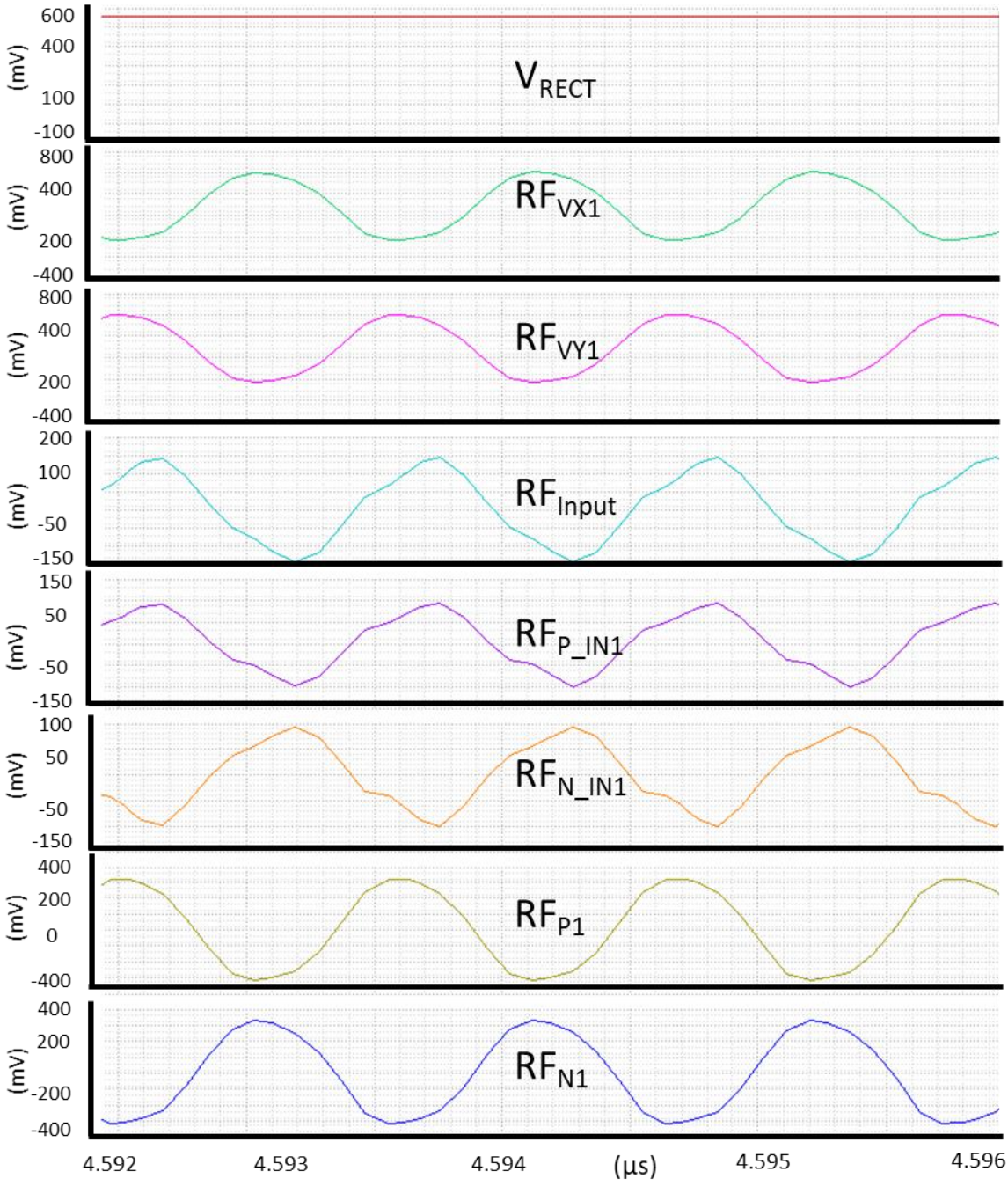
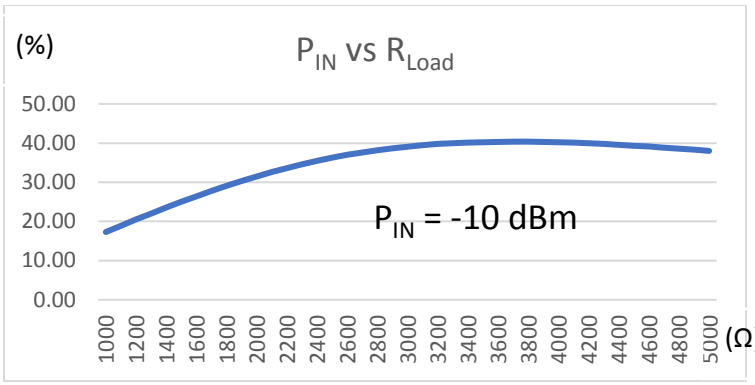
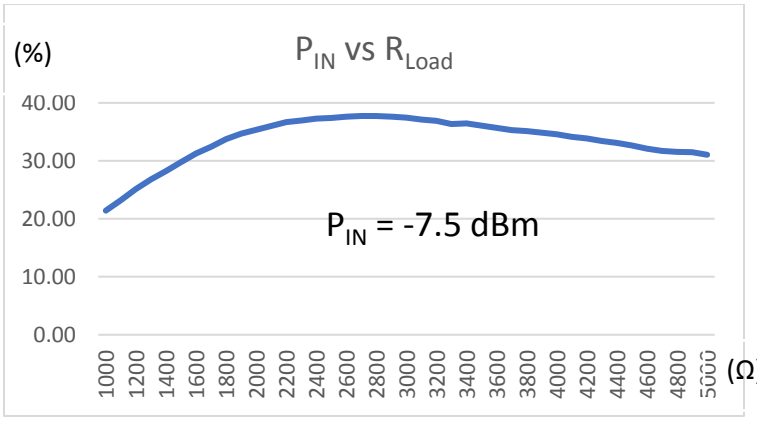


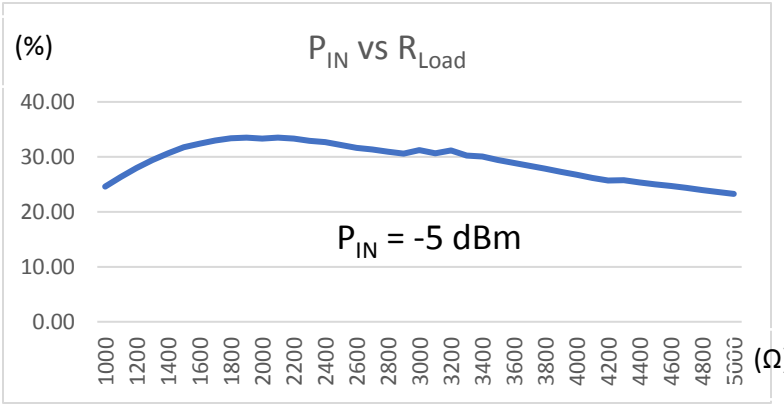
Fig. 5.11 Magnified waveforms of the circuits in Fig. 5.10 at -10 dBm.



(a)

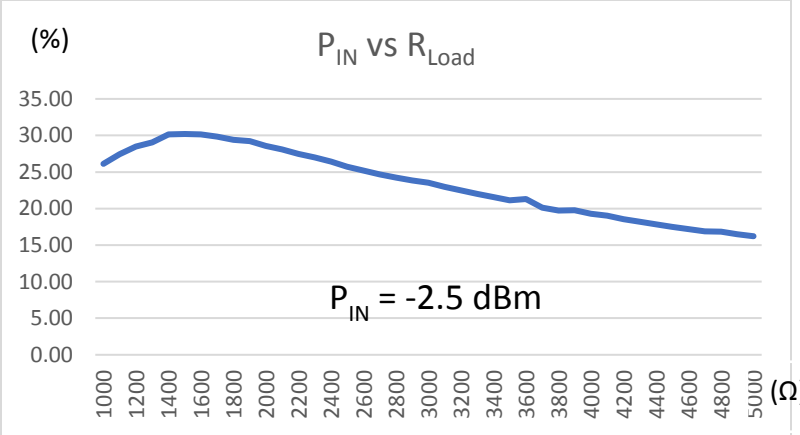


(b)



(c)

Fig. 5.12 Simulation results of loads versus efficiency plots for RF rectifier circuit.



(d)

Fig. 5.12 Continued

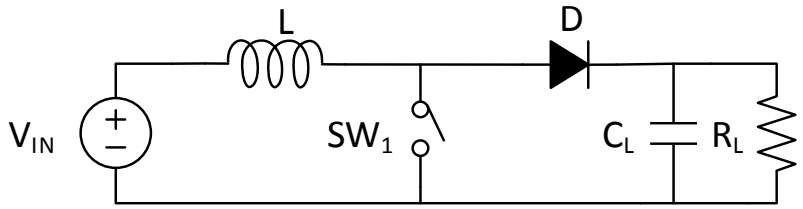
Table 5.3 Summary of Simulated Loads Versus Efficiency of RF Rectifier

Input Power	Load Range (Ω)	V_{RECT} Range (V)	Efficiency Range (%)
-10	3.4 K ~ 4.1 K	0.37 ~ 0.41	40.36 ~ 40.11
-7.5	2.4 K ~ 3.1 K	0.39 ~ 0.45	37.6 ~ 37.1
-5	1.7 K ~ 2.4 K	0.42 ~ 0.49	32.67 ~ 33.5
-2.5	1.4 K ~ 1.9 K	0.48 ~ 0.56	29.24 ~ 30.2

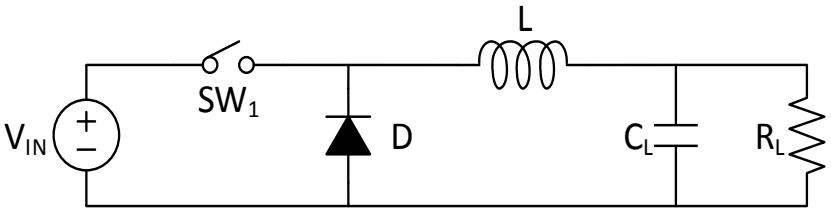
5.4 DC-DC Converters

5.4.1 The Fundamentals of DC-DC Converters

Generally, a DC-DC converter converts one voltage level of a direct current source (DC) into different levels of voltage sources to power up electrical or electronic systems [62]. There are three general types of DC-to-DC converters: boost, buck, and buck-boost DC-DC converters [63]. Among these, a boost and a buck type of a DC-DC converter are the most widely used to power up systems, where a higher output voltage compared to the input voltage is required (boost type) or vice versus (buck type), as well as, where a system requires a high efficiency [63].



(a)



(b)

Fig. 5.13 General schemes of (a) a Boost DC-DC converter, and (b) a Buck DC-DC converter [63].

Fig. 5.13 shows the general DC-DC converter schematics of (a) a boost configuration, and (b) a buck configuration.

In general, if a system requires a higher output voltage than input voltage, then a boost DC-DC converter is chosen. If a system requires lower output voltage than input voltage, then a buck DC-DC converter is the choice to power up the system. Especially in a buck regulator case, a low drop-out voltage regulator can be used instead of a buck converter. However, if a system requires high output load current as well as a high efficiency, then usually, a buck DC-DC converter is the one that delivers such requirements.

5.4.2 A PFM Type of a DC-DC Converter

There are two distinct more of operations in DC-DC converters. First is a pulse width modulation (PWM), and second is a pulse frequency modulation (PFM) [64]. A PWM operation is the most general control method used in a DC-DC converter [65]. A PWM is based on a fixed frequency [65]. Therefore, the amount of energy stored in an inductor is determined by the duty cycle. Fig. 5.14 shows the waveform of a PWM controlled DC-DC converter. In Fig. 5.14, "*ON*" denotes the on-time of a low side switch, which is representing the charging state of an inductor. "*OFF*" denotes the off-time of a low side switch. In addition, this off-time means on-time of a high-side switch, which is presenting energy transfer or discharging state through an inductor. The most important advantage of using this controlling method is that because it uses a fixed frequency a PWM based DC-DC converter can predict EMI (Electromagnetic Interface) noise [66]. As a result, a filter design can be easily done. The disadvantage is that since its frequency is fixed, at light load or at standby, the efficiency is degraded because of unnecessary switching actions [66].

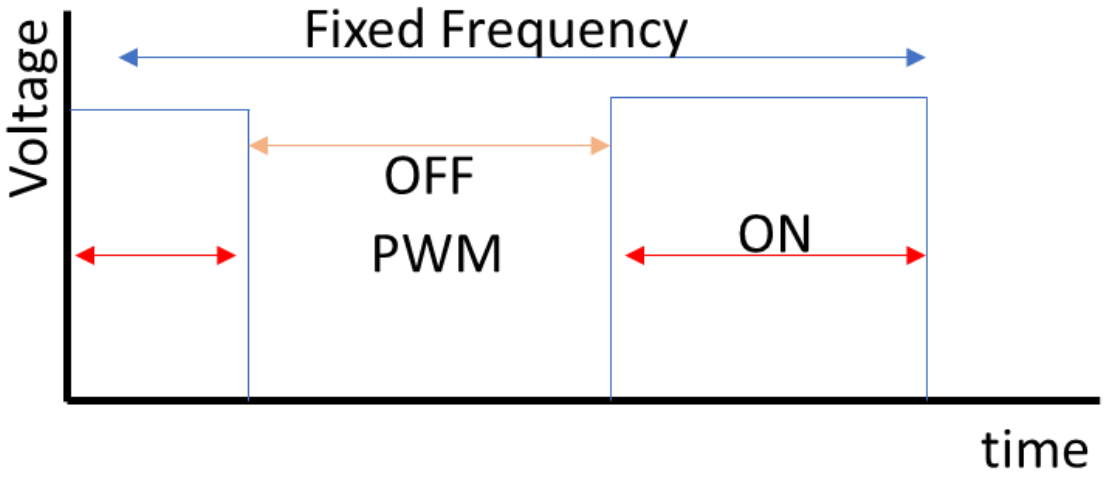


Fig. 5.14 A general waveform of a PWM control [64].

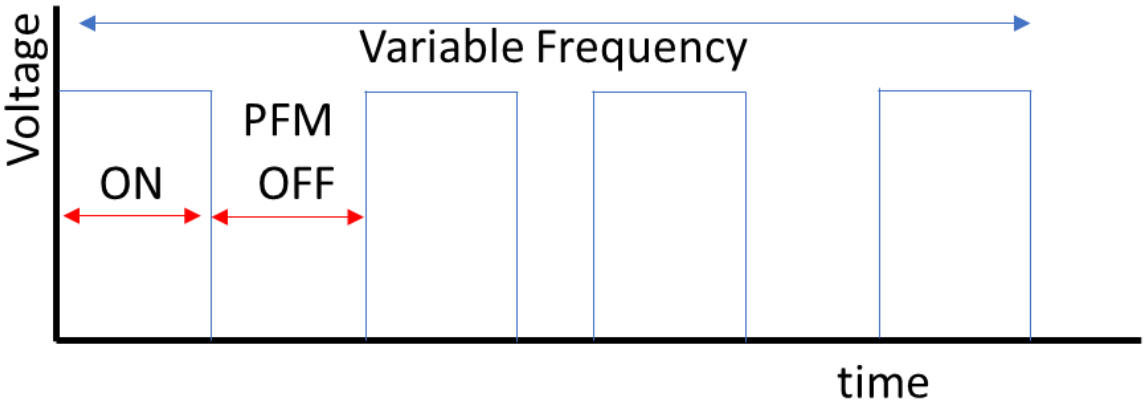


Fig. 5.15 A PFM mode operation [64].

A PFM control technique can be divided into two types. First is a fixed on-time type, and second is a fixed off-time type [66]. Fig. 5.15 shows the PFM mode operation [64]. A fixed on-time means its charging time is fixed and discharging through high side switch is controlled by varying its time or duty. A fixed off-time means discharging time is fixed and its charging time is varying. The advantage of a PFM mode control is that since its switching frequency can be varied, at light load or standby, the number of switching can be decreased so that its switching loss can be reduced [66]. However, also because of this variable switching frequency, an EMI filter is very hard to design and even at lower than 20 kHz, which produces audible noise, it can affect other electronic devices [66].

5.4.3 Input Impedance Control of a DC-DC Converter

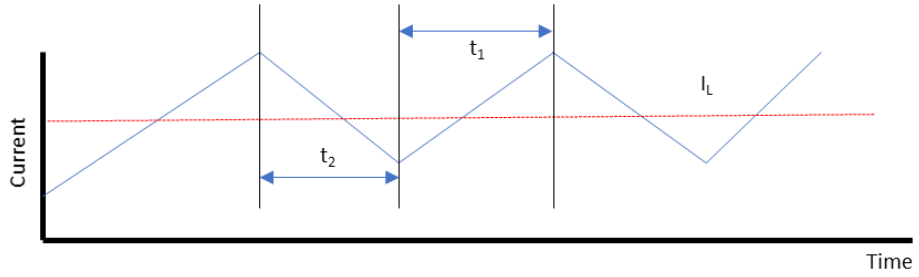
As explained in section 5.2.1, a cross-connected rectifier has an optimum load resistance value R_{opt}. In addition, a matching network in between an antenna and the input of a cross-connected rectifier is required to deliver an optimum power from the antenna to the RF rectifier circuit. Likewise, a cross-connected rectifier should be connected to the input of a DC-DC converter with an optimum input impedance so that the DC-DC converter can receive maximum available power from a RF rectifier. This idea of transferring or receiving maximum power is coming from the idea of a Maximum Power Point Tracking (MPPT) [67]. The MPPT technique has been used in a solar system for the first time [68]. The reason to deploy the idea of a MPPT is that a solar cell has a different load impedance as light strength has been changed [68]. Therefore, to send out the maximum power to the following loads such as a battery, a supercapacitor (storage devices), or a system, tracking an optimal impedance is very important point to have maximum

possible power to various kinds of loads. If the impedance in between a solar panel and a power extractor or power sender is not matched properly, then there will be significant amount of energy loss before energy is transferred from the extractors to the loads. This phenomenon can be applied into a RF energy harvesting system as well. If the impedance of between the output of a rectifier and the input of a DC-DC converter is not matched properly, then there is no way to transfer maximum available power from a rectifier into a DC-DC converter. That is why in section 5.2.1, the optimum impedances for the cross-connected RF rectifier at various available input RF powers is discussed. Since the optimum output impedance of a cross-connected rectifier at specific available input RF power is known, then the following work involves control of an input impedance of a DC-DC converter so that the regulator can receive maximum available power with well-matched impedance.

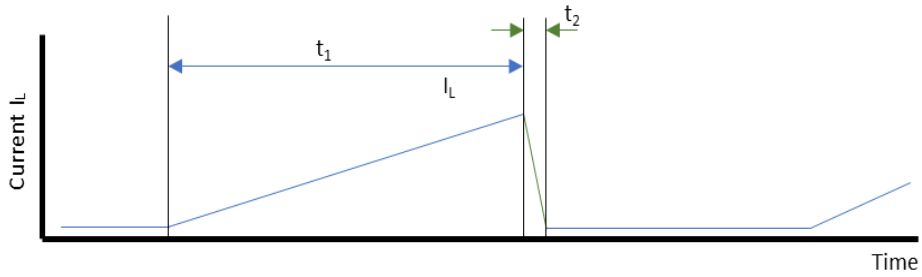
5.4.3.1 Input Impedance Control of Various Kinds of DC-DC Converters

To transfer or to extract maximum available power from a rectifier, which converts AC signal from RF input signal to DC signal, the input impedance of a DC-DC converter should be matched with the one from a rectifier. This section describes how the input impedance of different topologies can be calculated. The calculation of the input impedance for different topologies of DC-DC converters will be based on the Continuous Conduction Mode (CCM), and the Discontinuous Conduction Mode (DCM) [69]. In general, a CCM operation means that an inductor current during a switching cycle is always higher than zero. On the other hand, a DCM operation means that an inductor current during a switching cycle hits zero current level [69].

In Fig.5.16, t_1 and t_2 represent the on-time of a NMOS and a PMOS switch respectively. The input impedance as well as the output voltage conversion ratio are affected by the operation of CCM and DCM in all DC-DC converter topologies. As stated in [69], the input impedance of DC-DC converter in steady-state condition is based on the average inductor current waveform. The input impedance as well as output voltage conversion ratio presented in this dissertation will be verified in simplified form.



(a)



(b)

Fig 5.16. An inductor current waveforms of (a) a CCM operation, and (b) a DCM operation.

5.4.3.1.1 A Buck Type DC-DC Converter

A DC-DC buck converter is used when the input voltage sources such as a battery or supercapacitor are higher than the required output voltage. Fig. 5.17 shows the conventional buck converter. The input to output voltage conversion ratio in CCM can be calculated as shown in equation (5.18) [70],

$$\frac{V_{out}}{V_{in}} = D \tag{5.18}$$

The output current of a buck converter can be denoted as shown in (5.19)

$$I_{out} = \frac{I_{in}}{D} \tag{5.19}$$

where *D* represents a duty cycle of the buck converter.

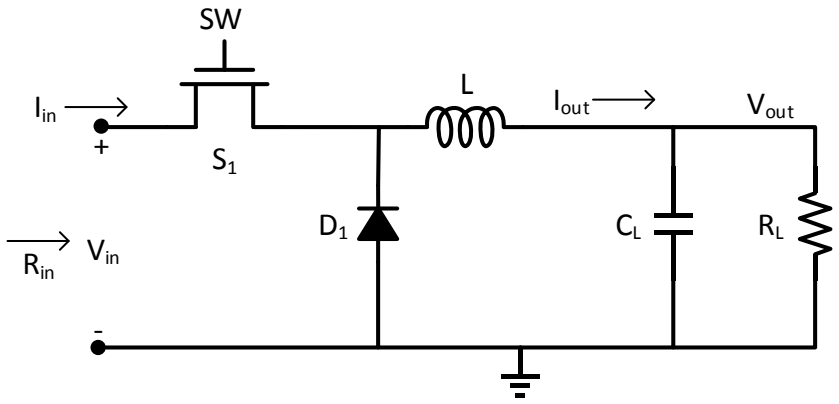


Fig. 5.17 A conventional DC-DC buck converter.

In steady-state, the average charge Q, which charges the output load capacitor, C_L, is zero. Therefore, the output current, I_{out}, can be calculated as shown in equation (5.20),

$$I_{out} = \frac{I_{out}}{R_L} \tag{5.20}$$

The input impedance of a buck converter can be calculated using equations (5.18) through (5.20). Therefore, the input impedance of a buck converter is,

$$I_{in} = \mathrm{D}\left(\frac{V_{out}}{R_L}\right) or\ D(\frac{DV_{in}}{R_L})$$

$$R_{in,CCM} = \left(\frac{V_{in}}{I_{avg}}\right) = (\frac{R_L}{D^2}) \tag{5.21}$$

From equation (5.21), it can be concluded that the input impedance of a buck converter in CCM depends only on the output load resistance, R_L, and the duty cycle, D [70]. Similarly, the input impedance of a buck converter in DCM can be calculated as CCM. First, the peak current, I_{in} can be computed by the maximum inductor current during the on-time of S_1 and then, this can be averaged over the entire duty cycle, T_s to obtain the average input current, I_{avg}.

$$I_{peak} = \frac{(V_{in}-V_{out})D_1T_s}{L}$$

$$I_{avg} = \frac{I_{peak}D_1}{2} = \frac{(V_{in}-V_{out})D_1^2T_s}{2L} \tag{5.22}$$

The output to input voltage conversion ratio of the buck converter in DCM can be calculated as follow [70].

$$\frac{V_{out}}{V_{in}} = V_{conv} = \frac{2}{1+\sqrt{1+\frac{8L}{D_1^2 R_L T_s}}} \tag{5.23}$$

To obtain the input impedance of a buck converter, the voltage conversion ratio needs to be submitted, and therefore, the input impedance is,

$$R_{in,DCM} = \frac{V_{in}}{I_{avg}} = \frac{2L}{(1-V_{conv})D_1^2 T_s} \tag{5.24}$$

From the equation (5.24), it can be easily observed that unlike CCM operation in a buck converter, the input impedance of a buck converter depends on the on-time periods, D_1 of the converter, the inductance value, L, and the load resistance, R_L. In addition, since the input impedance is affected by the output load, R_L, it is very important to monitor the output load resistance to achieve an accurate controlling of an input impedance, which is controlled by the on-time of switching periods D_1 [70].

5.4.3.1.2 A Boost Type DC-DC Converter

A DC-DC boost converter is used when the input voltage sources such as a battery or supercapacitor is lower than the required output voltage.

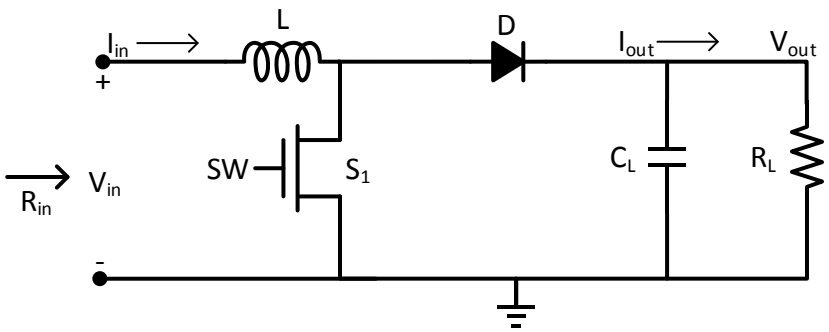


Fig. 5.18 A conventional DC-DC boost converter.

Fig. 5.18 shows the conventional DC-DC boost converter. The input to output voltage conversion ratio of a DC-DC boost converter operating in CCM can be expressed as shown in equation (5.25) [70],

$$V_{out} = \frac{1}{(1-D)} V_{in} \tag{5.25}$$

where *D* is the duty cycle, which is turn-on time of S_1.

The inductor current, I_L, is equal to the input current, I_{in}, so the average inductor current can be expressed as shown in equation (5.26),

$$I_{avg} = \frac{V_{in}}{R_L(1-D)^2} \tag{5.26}$$

To obtain the input impedance of a DC-DC boost converter in CCM operation, equations (5.25) and (5.26) should be combined. Therefore, the input impedance, $R_{in,CCM}$ can be denoted as following equation (5.27),

$$R_{in,CCM} = \frac{V_{in}}{I_{avg}} = R_L(1-D)^2 \tag{5.27}$$

From equation (5.27), it can be concluded that the input impedance of a DC-DC boost converter in CCM operation depends on the output load resistance, R_L, as well as the duty cycle of a boost converter [70].

On the other hand, the input impedance of a boost converter in DCM operation can be calculated in a similar manner as in CCM operation. The inductor peak current in DCM operation of a boost converter can be expressed as following equation (5.28) [67,70,71],

$$I_{peak} = \frac{V_{in}D_1T_s}{L} \tag{5.28}$$

where D_1 is the duty cycle of S_1.

The average inductor current of a boost converter in DCM operation can be divided into two parts. First, during the charging state, which is D_1, and second is during the discharging state, which is D_2 as can be seen in Fig. 5.16 (b).

Therefore, the average inductor during D_1 and D_2 can be calculated using the following equations (5.29) and (5.30) [67,70,71],

$$I_{avg,D_1} = \frac{V_{in}D_1^2T_s}{2L} \tag{5.29}$$

$$I_{avg,D_2} = \frac{V_{in}D_1D_2T_s}{2L} \tag{5.30}$$

where T_s is switching periods of a boost converter.

To obtain the input impedance of a boost converter in DCM operation, the total average current over the total switching period, T_s needs to be calculated. Therefore, the average inductor in the period of T_s can be expressed as following equation (5.31) [67,70,71],

$$I_{avd,T_s} = \frac{V_{in}D_1T_s}{2L}(D_1 + D_2) \tag{5.31}$$

As a result, the input impedance of a boost converter in DCM operation can be denoted as following equation (5.32) [67,70,71].

$$R_{in,DCM} = \frac{V_{in}}{I_{avg,T_s}} = \frac{2L}{D_1T_s(D_1+D_2)} \tag{5.32}$$

From equation (5.32), it can be concluded that the input impedance of a boost converter in DCM operation depends on the total switching period, T_s, the charging state, D_1, the discharging state, D_2, as well as the in ductor value. Therefore, to control the input impedance of a boost

converter in DCM operation, it is very important to control D_1 as well as D_2 precisely to achieve a proper value of the input impedance.

5.4.3.1.3 A Buck-Boost Type DC-DC Converter

A DC-DC buck-boost converter is used when the input voltage sources such as a battery or supercapacitor is lower than the required output voltage. In addition, it can be used when the output is lower than the input.

Therefore, it looks more like combing a buck and a boost converter into one topology. However, as can be seen in Fig. 5.19, the output voltage, V_{out}, polarity is flipped unlike the other two topologies.

Fig. 5.19 shows the conventional DC-DC buck-boost converter. The input to output voltage conversion ratio can be expressed like equation (5.32) [70,72],

$$V_{out} = -\frac{D}{(1-D)} V_{in} \tag{5.32}$$

The inductor can be calculated as following equation (5.33)

$$I_L = -\frac{V_{out}}{R_L} \tag{5.33}$$

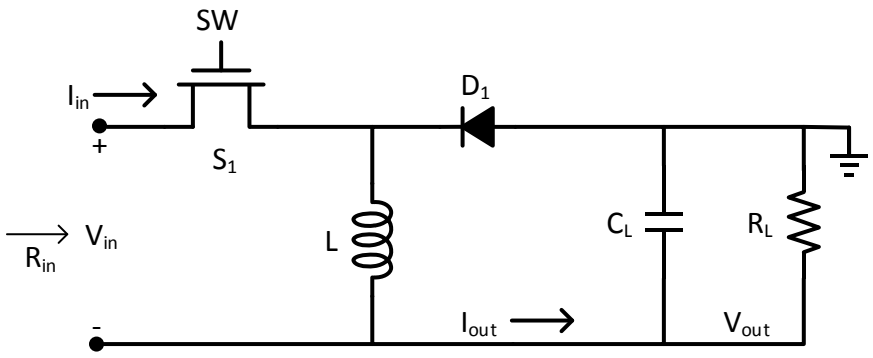


Fig. 5.19 A conventional DC-DC buck-boost converter.

The average input current can be calculated using equation (5.33) with charging state of switching cycle of a buck-boost converter and it is shown in equation (5.34) [70,72].

$$I_{avg} = -\frac{DV_{out}}{R_L(1-D)} \tag{5.34}$$

To obtain the input impedance of a buck-boost converter in CCM operation, the equations (5.32), and (5.34) should be combined, and the result is shown in equation (5.35) [70,72],

$$R_{in,CCM} = \frac{V_{in}}{I_{avg}} = R_L \frac{(1-D)^2}{D^2} \tag{5.35}$$

From equation (5.35), it can be seen that the input impedance of a buck-boost converter operating in CCM depends on a load resistor, R_L as well as a duty cycle, D.

The buck-boost converter operating in DCM can be analyzed in a similar manner as operating in CCM. First, a peak inductor in a buck-boost converter in DCM operation can be expressed as following equation (5.36) [70,72],

$$I_{peak} = \frac{V_{in} D_1 T_s}{L} \tag{5.36}$$

where D_1 is the duty cycle of switch S_1.

The average current of a buck-boost converter in DCM operation is same as the input inductor current over the inductor charging state, which is the turn on cycle of S_1 and it is defined as D_1. Therefore, the input impedance of a buck-boost converter in DCM operation can be calculated with the average inductor current over the input voltage, V_{in}. First, the average inductor current can be expressed as following equation (5.37) [70,72],

$$I_{avg} = \frac{I_{peak} D_1}{2} \tag{5.37}$$

Second, the input impedance of a buck-boost converter over the entire switching period can be expressed in equation (5.38) [70,72].

$$R_{in,DCM} = \frac{V_{in}}{I_{avg}} = \frac{2L}{D_1^2 T_s} \tag{5.38}$$

As can be seen from equation (5.38), the input impedance of a buck-boost converter in DCM operation depends on the inductor, L, a charging cycle, D_1, and an entire switching cycle, T_s. The advantage of a buck-boost converter in DCM is that since the variables, which affect the changing of the input impedance are easy to keep constant. It can therefore be concluded that a buck-boost converter in DCM can have a decent constant input impedance.

5.5 Overall Operation of the Proposed DC-DC Converter

Fig. 5.20 shows the simple flow chart describing the operation of the proposed DC-DC boost converter. Since the proposed DC-DC boost converter does not have an internal reference, which is usually used as a reference voltage to determine the duty cycle of a DC-DC converter, the proposed DC-DC converter needs to have a reference voltage from outside unlike an ordinary DC-DC boost converter. As can be seen from Fig. 5.20, the operation of a DC-DC boost converter starts from sampling the open circuit voltage of a RF rectifier, where a RF rectifier is working as an input power source of a DC-DC boost converter. The sampling frequency of a sample and hold (S&H) circuit is approximately 5 Hz.

The operating frequency of a S&H is determined based on the time in which a S&H can store a proper open circuit voltage from a RF rectifier and this frequency should not affect the operation of a DC-DC boost converter. Once a S&H circuit finishes its sampling job, then the inverted sampling frequency generator or so called the inverted signal of an oscillator (*OSCB*) will turn on the switch in between a RF rectifier and a DC-DC converter so that the RF rectifier can supply the input power to a DC-DC boost converter. Therefore, the DC-DC converter of an energy harvesting system is turned on whenever the oscillator generates the inverted oscillator signal.

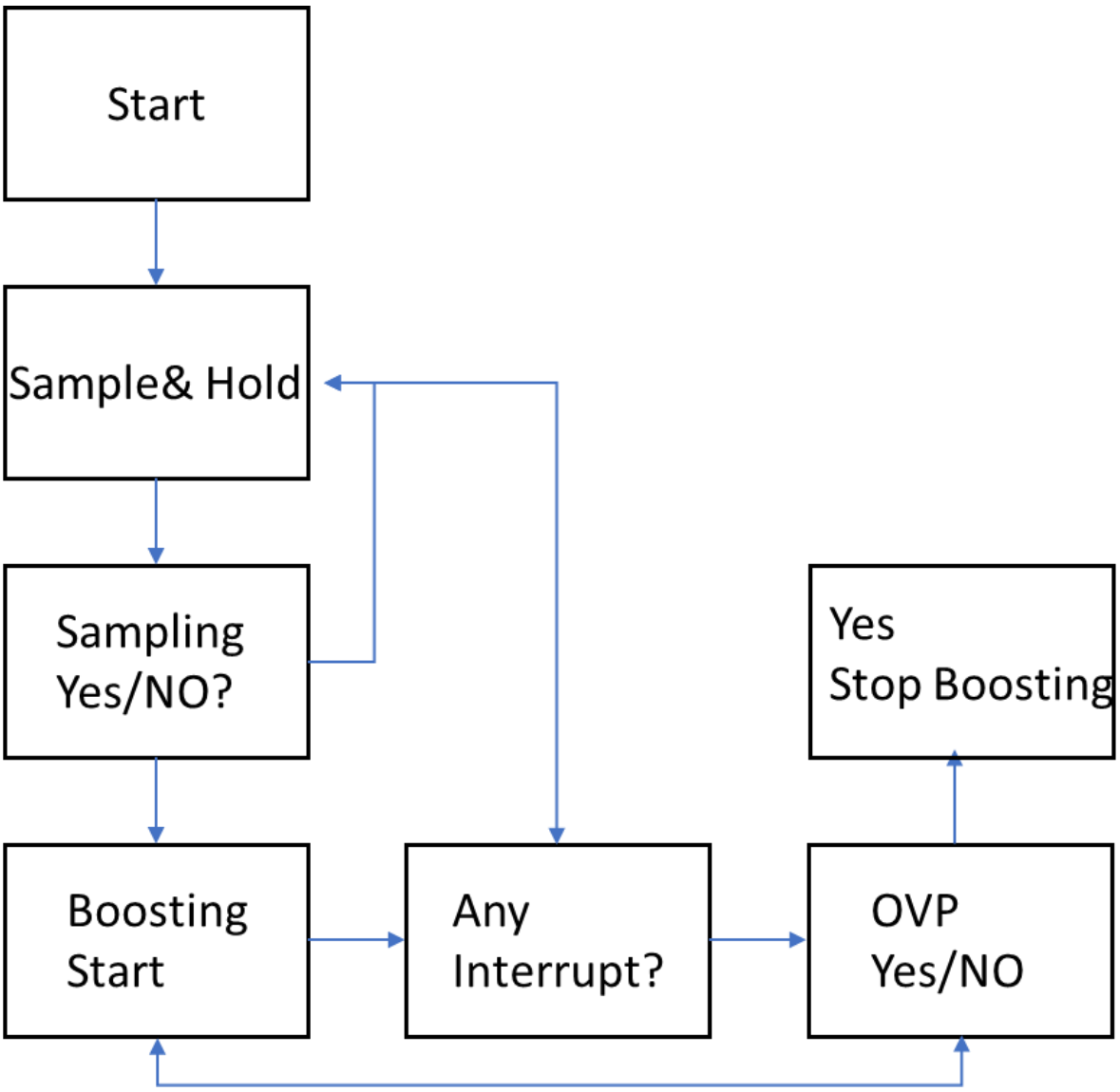


Fig. 5.20 A flow chart of the proposed RF energy harvesting system.

Otherwise, the system falls into the sampling stage. The protection function of the proposed DC-DC boost converter can be implemented externally. The internal protection triggering bit sets as 0. As a result, if the protection is detected and logic low signal is generated and the boosting action will be halted until the protection bit is cleared.

5.5.1 Input Impedance Control of the Proposed DC-DC Converter

Fig. 5.21 shows the structure of the proposed DC-DC converter. Usually, the output voltage from a RF cross-connected rectifier which generally depends on the distance between the transmitter and the receiver as well as the available transmittable power from a transmitter, is too low to be used directly as a voltage source for the subsequent blocks of the system. In addition, the output voltage is not properly regulated as well. Therefore, a boost converter can be used to boost up the input voltage up to usable output voltage level as well as to get a regulated output voltage for the system

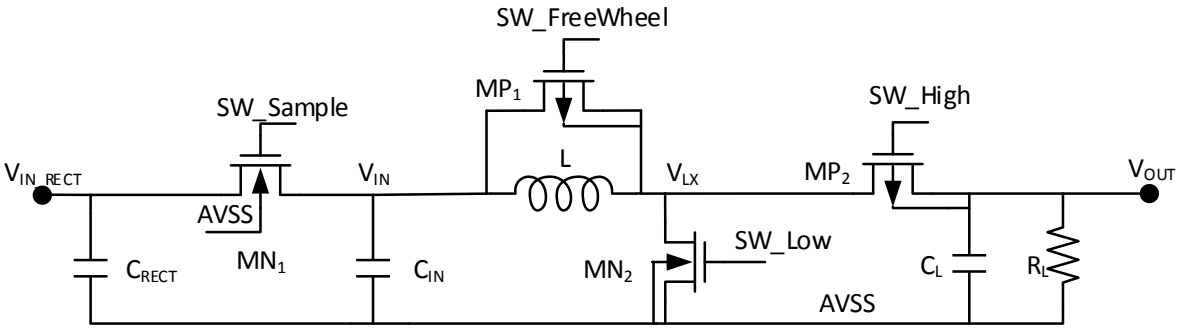


Fig. 5.21 The schematic of the proposed DC-DC boost converter.

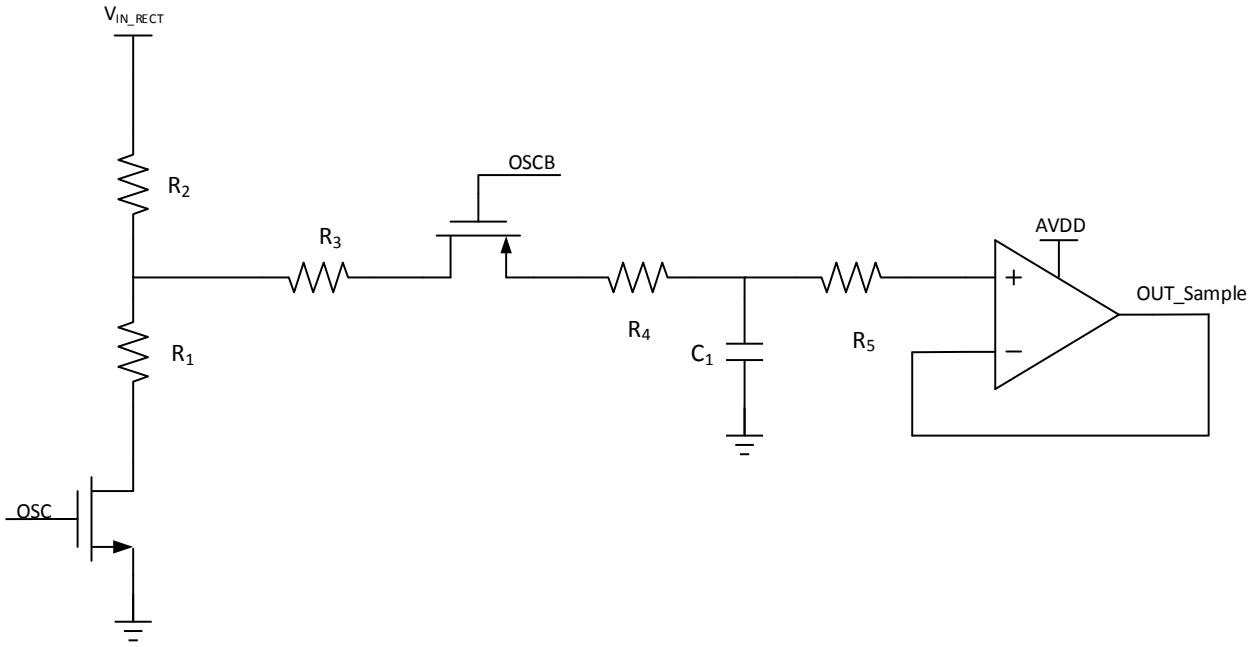
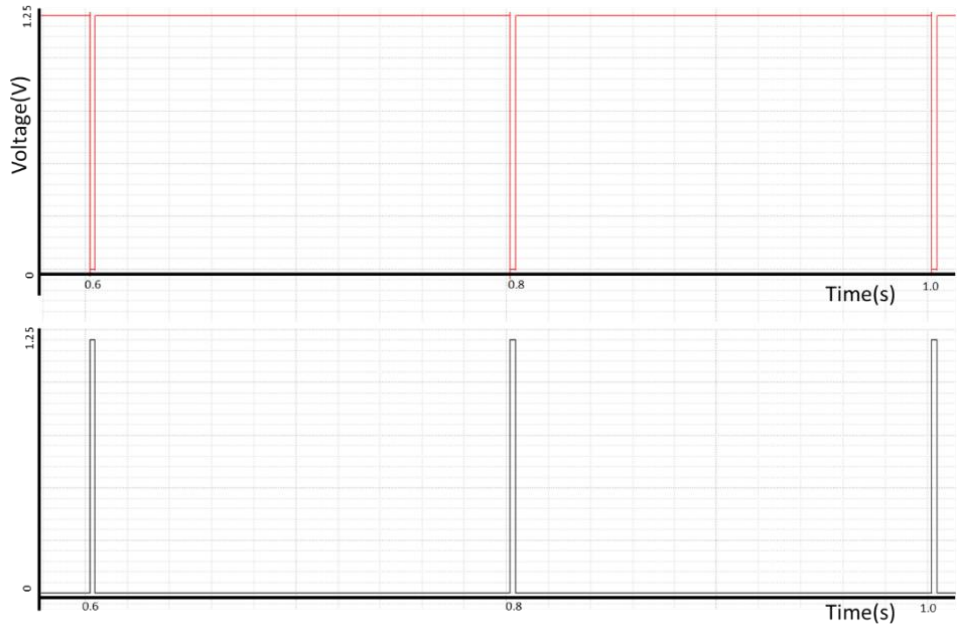


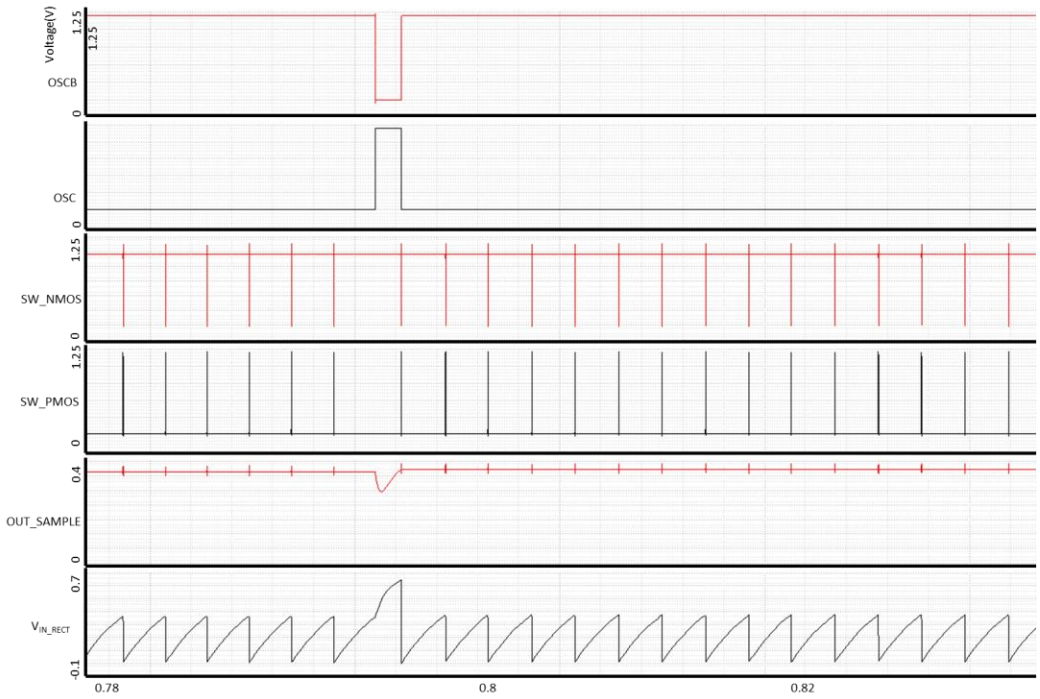
Fig. 5.22 The proposed sample and hold circuit.

The boost converter architecture is composed of an NMOS low side switch, MN_2, a PMOS high side switch MP_2, an inductor free-wheeling current switch, MP_1, and a sample and hold switch, MN_1. Fig. 5.22 shows the schematic of the sample and hold circuit. This circuit measures the open circuit output voltage of a RF rectifier and stores this sampled open circuit voltage into an external storage capacitor, C_1. When the system falls into the sampling stage, MN_1, MN_2, and MP_2 as shown in Fig. 5.21, are falling into the *off-state*. Therefore, a boost converter stops its boosting operation. This action of sampling the output voltage of a RF rectifier is controlled by the sampling oscillator signal.

Fig. 5.23 shows the output of waveform in a sample and hold circuit.



(a)

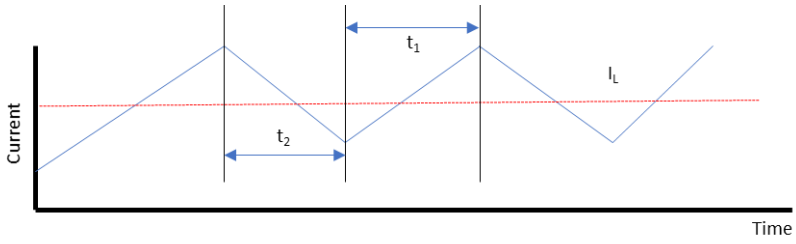


(b)

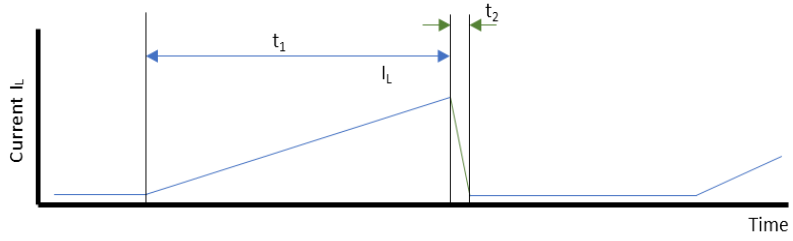
Fig. 5.23 Sample and Hold waveforms of (a) *OSC* and *OSCB*, (b) sampling waveform.

In Fig 5.23, (a) shows the waveform of an oscillator where a red waveform shows the inverted oscillator waveform (*OSC* and *OSCB*), and Fig. 5.23 (b) represents the oscillator signal as well as the sampling action of the output voltage from a RF rectifier. The pulse width of the oscillator is 2.5 ms, and the frequency of this sampling is 5 Hz.A sampling frequency as well as the width of turn on-time should be carefully chosen so that the output voltage of the sample and hold should maintain proper value in between sampling periods. That means the leakage from a capacitor, C_1, should not affect the proper sampling voltage from a capacitor, C_1, during its DC-DC booster operation. Otherwise, it will generate errors for the reference voltage, which is generated by C_1 due to the lower sampling voltage than the actual sampling voltage.

In addition, if the sampling output voltage periods from a RF rectifier is too frequent, then it could interrupt the switching action of a DC-DC boost convert since whenever sampling action kicks in, the operation of a DC-DC converter stops until the sampling action is finished and could cause improper operation of a DC-DC converter. In Fig. 5.23, (b) shows this action. When *OSC* or *OSCB* falls into a *ON*-state, *SW_NMOS* (MN_2), and *SW_PMOS* (MP_2), which are the switching MOSFETs of a DC-DC converter, are falling into *OFF*- state, and only a sampling and hold circuit (S&H) is falling into working state. As a result, the *OUT_SAMPLE* voltage is increased with respect to the voltage, V_{IN_RECT} in open circuit sampling voltage state. Since a sampling circuit is working only during a sampling period, the current consumption needs to be minimized so that its static current consumption can be optimized as well. To minimize the static current, a switch controlled by the *OSC* signal in Fig. 5.22 has been used. As a result, S&H current consumption range is only in ~ 100's nA.



(a)



(b)

Fig. 5.24 Inductor current waveforms in (a) a CCM operation, and (b) a DCM operation.

Turning *on/off* action of a S&H circuit is done by the NMOS and the PMOS of a sampling circuit, which are controlled by the oscillator signal *OSC* and *OSCB* as shown in Fig. 5.22. R_1 and R_2 values are carefully chosen for proper reference voltage as well as to prevent drawing too much current from a rectifier voltage storage capacitor, C_{RECT} in Fig. 5.21.

The actual current flows through the external resistors, R_1 and R_2 will be about 410 nA, and C_1 will be used as a storage capacitor for a sampling voltage. Internal resistors, R_3, R_4, and R_5 are used as protection resistors which protect the input MOSFETs of an operational amplifier buffer as well as the drain and the source of a switch MOSFET that is controlled by the OSCB signal since C_1 is an externally connected storage capacitor.

Before discussing the detailed design of an input impedance control of a proposed DC-DC boost converter, the modes of operation in a DC-DC converter are studied briefly. There are basically two modes of operation in a DC-DC converter: CCM (Continuous conduction mode), and DCM (Discontinuous conduction mode).

Fig. 5.24 shows the inductor current waveforms in (a) CCM and (b) DCM. The typical advantages of a CCM mode of operation are summarized below:

1) The voltage gain is function of duty cycle.
2) The input current is continuous.
3) The ripple component of inductor current is lower than other component average current.
4) Higher efficiency can be achieved compared to a DCM mode of operation.

However, the major drawback of a CCM operation is that since the inductor current is always greater than zero even though it has a small ripple current, the efficiency in light load is very low. In addition, if the input available power is low, then CCM is very hard to maintain its original waveform as shown in Fig. 5.24 (a).

Fig. 5.24 (b) shows the waveform of the DCM mode operation. The advantages of DC mode operation are:

1) The voltage gain is function of load as well as frequency.
2) An inductor component size usually smaller than a CCM mode.
3) At light load, the efficiency is higher than a CCM mode of operation.

Other than abovementioned advantages of a DCM mode operation, it can perform better with respect to its efficiency as well as design of the system if the input available power is low.

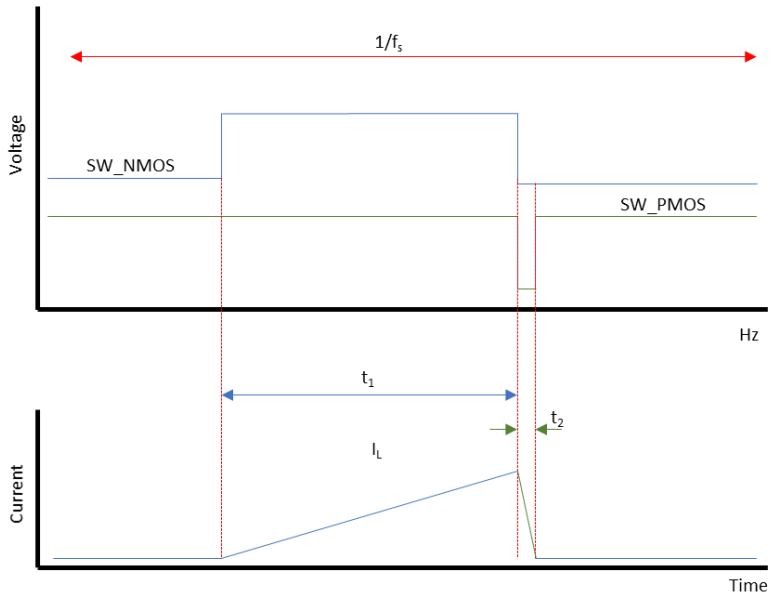


Fig. 5.25 Switch and inductor current waveforms in a DCM operation.

Since the input available power of the proposed RF energy harvesting circuit is very small and is limited by the available RF transmittable power as well as the distance between a transmitter and a receiver, a DCM mode of operation is chosen in this design due to the reasons explained above.

From Fig. 5.25, the inductor current, I_L can be calculated using the following equation. At the end of *SW_NMOS* switching period, I_{L_peak} is,

$$I_{L_peak} = \frac{t_1}{L} \tag{5.39}$$

This current is back to zero at the end of *SW_PMOS* switching. Therefore, the average current of I_L can be expressed as following,

$$I_{L_avg} = \frac{V_{IN} t_1 (t_1 + t_2) f_s}{2L} \tag{5.40}$$

where V_{IN} is input voltage of a DC-DC converter (output voltage of a RF rectifier),

t_1 is rising time (*SW_NMOS ON*-time),

t_2 is falling time (*SW_PMOS ON*-time),

f_s is switching frequency of a DC-DC converter,

L is a value of the inductor.

The input impedance of a DC-DC boost converter can be expressed as the ratio of the input voltage, V_{IN}, to the average inductor current, I_{L_avg}. Aa a result, the input impedance of a DC_DC boost converter can be expressed as,

$$\frac{V_{IN}}{I_{L_avg}} = \frac{2L}{t_1^2 f_s} \left(1 + \frac{t_2}{t_1}\right)^{-1} \tag{5.41}$$

If the boost conversion ratio is high enough (for example, conversion ratio is greater than 3), then the equation (5.41) can be further simplified as shown below,

$$\frac{V_{IN}}{I_{L_avg}} = \frac{2L}{t_1^2 f_s} \tag{5.42}$$

Equation (5.42) is good as long as $t_1 \gg t_2$.

Table. 5.4 Simulated Values of the Input Impedance of the Proposed DC-DC Boost Converter

dBm	**L (μH)**	**t_1 (μs)**	**f_s (Hz)**	**$R_{IN_simulated}$** of a DC-DC Converter **(KΩ)**	**$R_{Rectifier_opt_Range}$** of a RF Rectifier **(KΩ)**
-10	30	7.87	250	3.87	3.4 ~ 4.1
-7.5	30	7.86	316	3.07	2.4 ~ 3.1
-5	30	7.28	406	2.79	1.7 ~ 2.4
-2.5	30	6.95	478	2.6	1.4 ~ 1.9

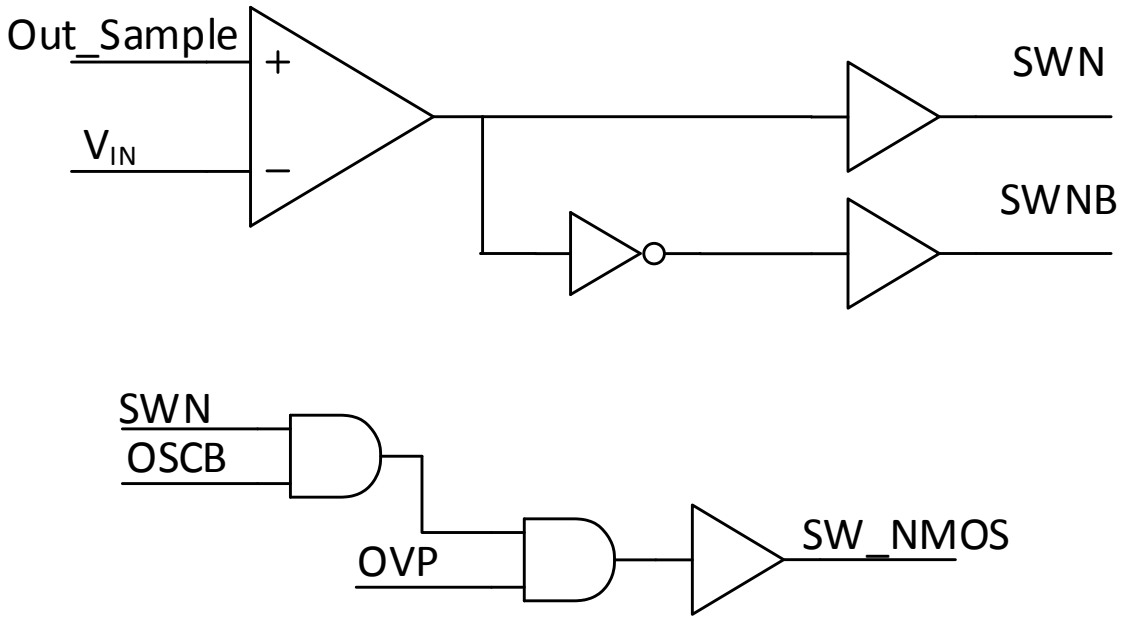


Fig. 5.26 A low-side switch control scheme.

From equation (5.42), it can be easily observed that the input impedance is a function of the inductor value, the switching frequency as well as *SW_NMOS* on-time, t_1. In addition, the equation shows that for the cases of fixed switching frequency, f_s, and on-time, t_1, an increase in the value of an inductor, L can increase the input impedance of a DC-DC boost converter.

The simulation is performed with following external components values,

The inductor, L, is 30 µH.
The capacitor, C_{RECT}, is 0.7 µF.
The capacitor, C_{in}, is 0.2 µF.

The schematic of the proposed DC-DC boost converter is shown in Fig. 5.21.

From Table 5.4, it can be seen that the input impedance of the proposed DC-DC boost converter closely follows the output impedance of a RF rectifier for the maximum power transfer from a RF rectifier to a DC-DC boost converter.

Table 5.4 shows the simulated input impedance of the DC-DC boost converter, $R_{IN_simulated}$, and the optimum output impedance of a RF rectifier, $R_{Rectifier_opt_Range}$. The input impedance of a DC-DC boost converter is determined by the circuit shown in Fig. 5.26. The sampled voltage from a sample and hold circuit is used as reference in comparator shown in Fig. 5.26. The reference voltage is compared with the input voltage, V_{IN} of a DC-DC boost converter. The comparator provides high value if a *OUT_Sample* is higher than V_{IN}, otherwise, it produces a low output signal. The switching frequency of a DC-DC boost converter is determined by this low or high voltage of the comparator output signals, and these output voltage signals are fed into and *AND* gate with the inverted oscillator output frequency.

Whenever a sample and hold circuit is in action, a switching action from a DC-DC boost converter should be stopped so that the inverted oscillator frequency, *OSCB*, can be used as enable signal with a switching input signal, *SWN*, which is coming from a comparator that compares *OUT_Sample* voltage with V_{IN}.

5.5.2 The Proposed DC-DC Boost Converter Switch Controls

Since the proposed DC-DC boost converter is a synchronous type, there should be two MOSFETs working as switches. One is called as a low-side MOSFET, which is a switch to be used as charging an inductor and the other is called as a high-side MOSFET, which is a switch to be used as discharging an inductor. The low and the high side MOSFETs are presented as MN_1 and MP_1 respectively in Fig. 5.21. The advantage of using two low and high side MOSFETs is that the turn-on or threshold voltages (V_{th}) of both MOSFETs are lower than that of a conventional diode, which is trypically around 0.7V. Therefore, in general, a synchronous type of a DC-DC converter can achieve higher voltage conversion efficiency than a conventional asynchronous type DC-DC converter which uses a diode in a high-side MOSFET location (Refer to Fig. 5.21, a MP_1 is a high-side MOSFET). In addition, since R_{on} of low and high side MOSFETs can be adjusted by the designer (as R_{on} depends on the size of the MOSFET), the power loss (or, also called as conduction loss) due to the R_{on} is less than a conventional asynchronous DC-DC converter as well and can be expressed as,

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \tag{5.43}$$

where μ_n is representing an electron mobility

C_{ox} is representing an oxide capacitance

W is representing the width of gate

L is representing the length of gate

V_{GS} is representing the gate-source voltage

V_{th} is representing the threshold voltage of a MOSFET.

Equation (5.43) can be used for calculation of typical R_{on} values. This equation can be applied to both *N*-type as well as *P*-type MOSFETs. As it can be seen from the equation (5.43), R_{on} will be lower if the aspect ratio of a MOSFET is increased.

The NMOS control signal is generated by the comparator as shown in Fig. 5.26. The comparator is comparing two voltages coming from a sample and hold circuit, *OUT_Sample* and the input voltage of a DC-DC converter, V_{IN}.

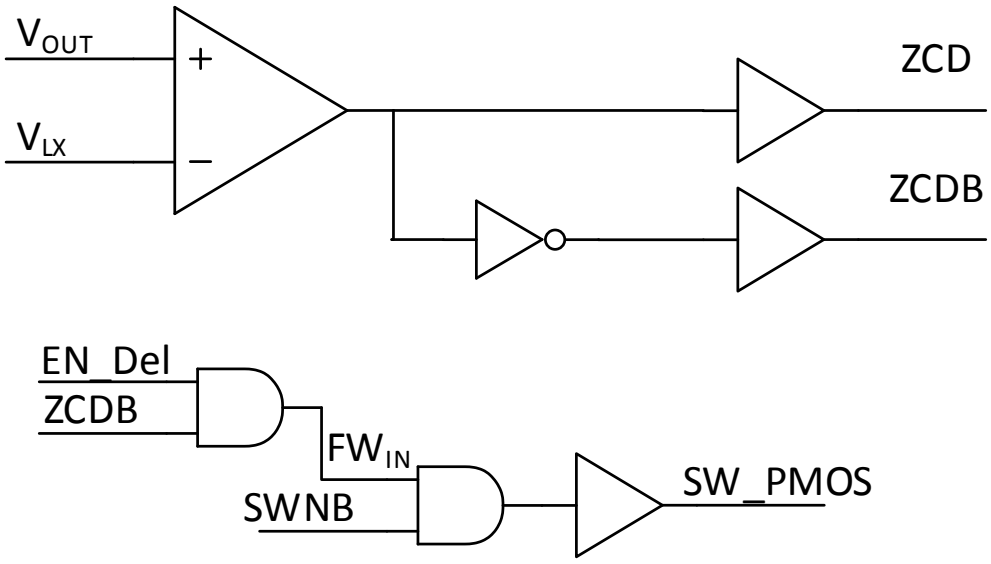


Fig. 5.27 A high-side switch control scheme.

This signal is them combined logically with an inverted sample and hold sampling oscillator signal, *OSCB* and over voltage protection signal. This combined signal finally produces the switching signal for the low side MOSFET, which is a MN_1 in Fig. 5.21. Fig. 5.27 shows the circuit scheme for the high-side switching control. The PMOS switch control scheme is very similar to the NMOS switch control circuit. A PMOS switch (or a high-side switch) should be turned off whenever the current through the high-side MOSFET current is crossed the zero point.

This is because if a high-side PMOS switch is not turned off properly whenever an inductor completely discharges its stored energy, there will be a reverse current flowing through a high-side switch, which will cause several problems.

Therefore, turning *on/off* a PMOS switch is one of the important design points in a synchronous DC-DC boost converter. One of the problems with detecting an inductor current is that it requires very complex and medium to high current (several tens of micro-amperes to hundreds of micro-amperes) consumed by control circuits. As a result, it is not realistic using such a method to apply in a low power DC-DC converter like the one proposed in this research. Therefore, in this proposed DC-DC boost converter, the simplistic way of detecting a zero-current sensing circuit is applied.

Zero-current in an inductor means that it finishes discharging stored current. Therefore, even though there exists some delay time in between zero inductor current and zero inductor voltage, it is still fine to use a simple method of detecting zero voltage of an inductor because of low switching frequency (~ 10 to 100's of Hz). The proposed simple method of detecting zero inductor current starts from a comparator. By comparing output voltage of a DC-DC boost converter, V_{OUT}, with an inductor node voltage, V_{LX} (refer to Fig. 5.21), the comparator output produces a signal for controlling a high-side switch. When the inductor node voltage V_{LX} goes

below V_{OUT}, it means that an inductor current is fully discharged. Therefore, the high side PMOS switch should be turned off immediately. Otherwise, there will be reverse current flowing through the output of a DC-DC boost converter, V_{OUT}, to the input of a DC-DC boost converter. However, a problem still exists when V_{OUT} starts charging from zero. Since a load capacitor or an output storage capacitor, C_L in Fig. 5.21, is discharged completely in the beginning of a DC-DC boost operation, initial charging current from an inductor is not enough to increase the voltage of a capacitor if a load capacitor value is too large similar to a super capacitor. Therefore, there should some sort of a pseudo signal generator for a high-side PMOS control signal. In addition, a high-side switch control signal should remain off when a low-side switch control signal is active. As a result, *SW_NMOS* signal, which is a control signal for a low-side switch should be implemented into controlling a high-side switch control signal generator.

Fig. 5.28 shows the pseudo signal generator for a high-side switch control. In Fig. 5.28, INV_1, INV_2, and INV_3 are current controlled inverter so that C_1, C_2, and C_3 can be as small as possible. The current flowing through INV_1 through INV_3 are about 6 nA.

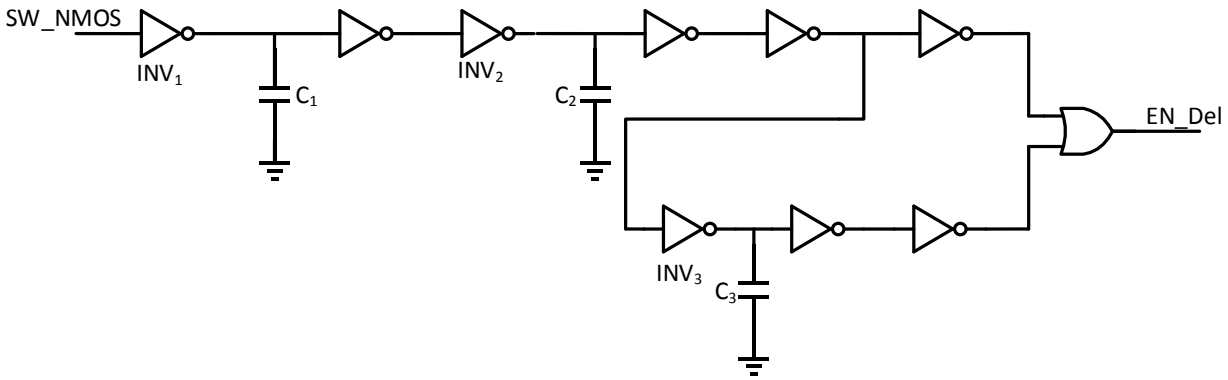


Fig. 5.28 A zero current control signal, *EN_Del*, generator circuit.

C_1 is an external capacitor with value of 4 pF. C_2, and C_3 values are 1.4 pF and 2 pF, respectively. The reason for using an external capacitor is that it provides a convenient means of tuning the delay and the width of an *EN_Del* signal. All the external capacitors will be integrated into chip later on after finding an optimum value so that the area of PCB can be optimized later.

Fig. 5.29 shows the simulation waveform of a low-side switch control signal. As can be seen from this waveform, whenever an *OCSB* control signal is kicked in (active low), all the control signal including a low-side switching control signal are stopped so that a sample and hold circuit can start sampling the open circuit voltage of the RF rectifier.

Otherwise, all control circuits are working as normal so that a DC-DC boost converter can do its work. Fig. 5.30 shows the simulation waveform of a high-side switch control signal. An *EN_Del* signal gives enough masking or delaying time for a *ZCDB* signal, which can provide a fault signal especially when the output voltage, V_{OUT} is very low. Fault signal is mainly due to tight hysteresis of a comparator. Large hysteresis voltage of a comparator can solve this problem but large hysteresis means it will produce more errors in the switching time. Therefore, instead of using large hysteresis comparator voltage, using an *EN_Del* signal can eliminate fault comparator signal during the operation of a low-side switching circuit especially in low DC-DC boost output voltage.

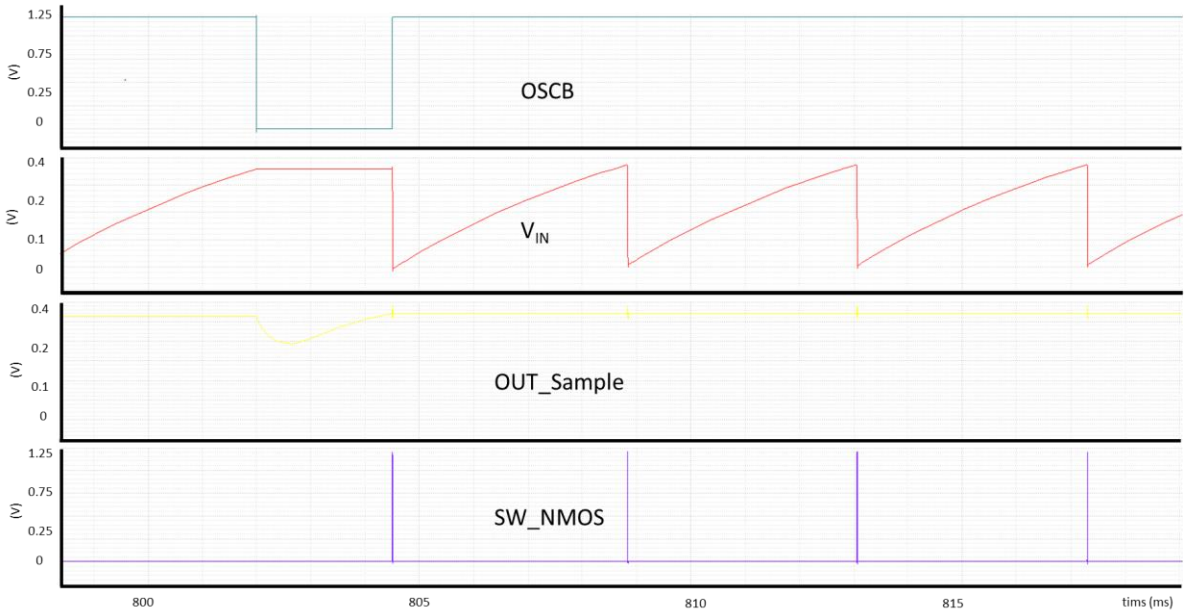


Fig. 5.29 A low-side switch control waveforms.

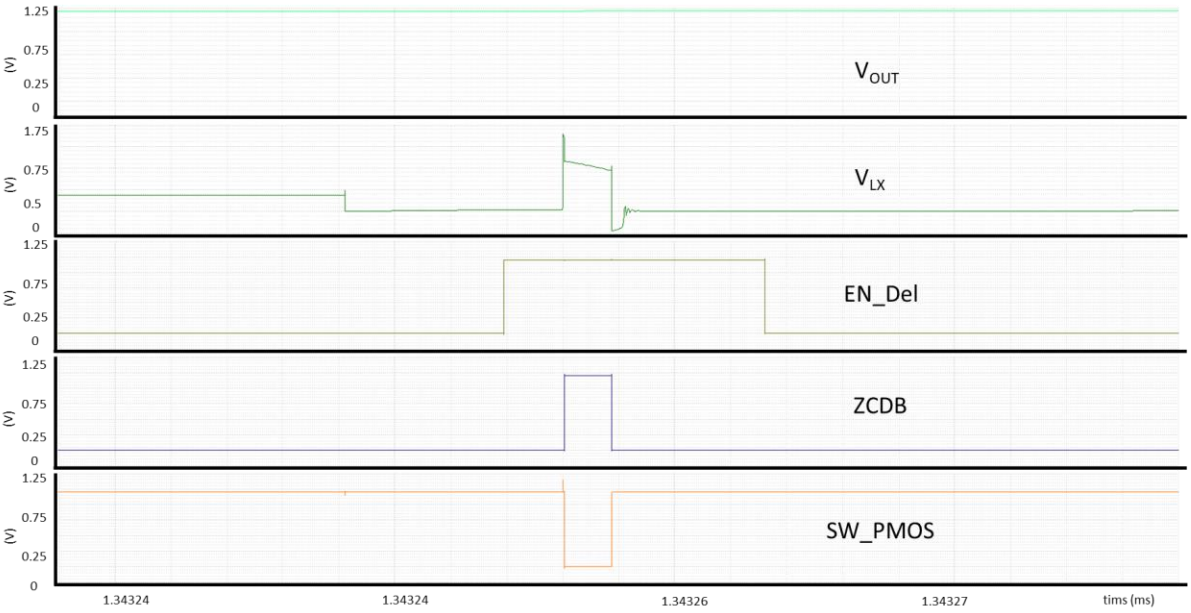


Fig. 5.30 A high-side switch control waveforms.

5.5.3 Power Conversion Efficiency

One of the most important design points involves reducing the power loss in various parasitic components as well as power consumed by the control circuits. The power conversion efficiency is getting more and more attention in designing a DC-DC power converter since there are more devices out there using a battery as a primary power source [73]. Likewise, since the proposed RF rectifier produces limited available power, which depends on the available output power from a transmitter and the distance between transmitter and receiver at the same time, reducing a power loss in a DC-DC converter is also one of the important design factor to produce maximum available output power from the RF energy harvesting system. To reduce or to minimize the power loss in a DC-DC boost converter, it is important to understand the basics of the power loss mechanism.

In general, there are two major power losses in a DC-DC converter, one is called as the conduction loss while the other is called as the switching loss. In general, a DC-DC converter has many integrated internal and external components and the DC current is always flowing through such components. Whenever DC current is flowing through them, so called conduction loss occurs because of the parasitic or equivalent resistors of these components. The switching loss mechanism is similar to the conduction loss. The main difference between the conduction loss and the switching loss is that the switching loss is due to the periodical changes of the current in components such as switching devices in a DC-DC converter.

The main switching components in a DC-DC converter is an inductor and the power switches. Since an inductor and the power switches in a DC-DC converter have parasitic capacitors, these capacitors are the main components causing the switching loss. In reference [74], the

conduction loss calculation is fairly simple. The required values to calculate the conduction loss are the average current flowing through the devices and the on-resistance or the parasitic resistance of the components. However, unlike the conduction loss, the switching loss calculation is very complex since it depends on many parasitic capacitances as well as the frequency of operation of the devices. Therefore, it is almost impossible to calculate the exact value of the switching loss and typically approximation values are used [75]. As a result, the calculated value of the switching loss has fairly large error compared to its actual measured value.

Because of the facts mentioned above, the designer of a DC-DC converter usually, considers following seven loss terms for the analysis of the power loss in a DC-DC converter. First is the conduction loss of an inductor incorporated with a DCR (DC resistance of the inductor and it can be found on the spec. sheet usually). Second is the loss of a load capacitor due to the ESR (equivalent series resistance of a load capacitor which can be found also in specification sheets of the capacitor). Third is the loss due to the power consumption of the control circuits in a DC-DC converter. Fourth is the conduction loss of power switches. Fifth and the sixth is the gate charging loss and the inductor switching loss, and the last is the switching loss of the MOSFET switches.

Every single inductor used in a DC-DC converter has its own DC resistance (DCR) which depends on the winding size as well as its structure. The DCR of an inductor is the main problem causing the conduction loss during its charging and discharging operating phases. Therefore, whenever current is flowing through an inductor in phase of charging or discharging, the DC resistance dissipates some energy and it causes the conduction loss of an inductor. The equation (5.44) shows the calculation of the inductor conduction loss [76],

$$P_{L_{DRC}} = \frac{R_{L_{DCR}}}{T} \int_0^T i_L^2(t)dt \tag{5.44}$$

where $R_{L_{DCR}}$ is the DCR of an inductor,

i_L is the inductor current,

T is the operating or switching frequency of a DC-DC converter.

It can be very clearly observed from the equation (5.44) that the main conduction loss is coming from the DCR of an inductor. Therefore, to minimize the conduction loss of an inductor, it is very important to choose the low DCR inductor component.

The loss due to the load capacitor is very complex to calculate since a capacitor has various kinds of parasitic components and related loss terms on its own such as temperature effect, leakage and dielectric losses, contact resistance etc. Therefore, to simplify such complex loss terms, the ESR from a datasheet is used instead since almost of all the complex variables of loss incorporated with a capacitor are reflected into the value of the ESR. With the ESR value, the loss of a load capacitor can be calculated as shown in equation (5.45) [76],

$$P_{C_{ESR}} = \frac{R_{C_{ESR}}}{T} \int_0^T i_o^2(t)dt \tag{5.45}$$

where $R_{C_{ESR}}$ is the ESR of a load capacitor,

i_o is the output current flowing into a load capacitor,

T is the operating or switching frequency of a DC-DC converter.

It can be also very clearly observed from the equation (5.45) that the main load capacitor loss is coming from the ESR of a load capacitor. Therefore, to minimize the load capacitor loss, it is very important to choose the low ESR capacitor component.

The power loss due to the power consumption of the control circuits can be optimized by reducing the static current of the control circuits. Usually, digital circuits are not consuming any

static current, it is desired to use digital circuits as much as possible. In addition, for the analog control circuits, it is very important to optimize the static current used for biasing.The conduction loss of switches is due to R_{on} resistance or turn-on resistance of the MOSFET transistors. In an asynchronous DC-DC converter, a low-side switch has R_{on} due to the MOSFET but the on resistance of the high-side switch is due to the R_{on} of the diode. Thus, the designer does not have any control over the R_{on} value of the high-side switch. Therefore, it is very important to choose right R_{on} for high-side diode switch similar to an inductor or a load capacitor. In a synchronous DC-DC converter it is very important to control the optimum size of MOSFET transistors since in this type of a converter there are two switches formed with MOSFET transistors. Since the energy wasted by R_{on} of both a high-side as well as a low-side switches occurs whenever current is flowing through the switches. The dissipated energy by the both switches can be calculated with following equations (5.46) and (5.47) [76],

$$P_{LSW} = \frac{R_{on_{LSW}}}{T} \int_0^{t_{ON_{LSW}}} i_L^2(t)dt \tag{5.46}$$

$$P_{HSW} = \frac{R_{on_{HSW}}}{T} \int_0^{t_{ON_{HSW}}} i_L^2(t)dt \tag{5.47}$$

where $R_{on_{LSW}}$,and $R_{on_{HSW}}$ are the R_{on} of the low-side and the high-side MOSFET transistors,

$t_{ON_{LSW}}$, and $t_{ON_{HSW}}$are the *ON*-time of the low-side and the high-side MOSFET switches,

i_L is the inductor current flowing through both low-side and high-side MOSFET transistors,

T is the switching periods of a DC-DC converter.

In addition, R_{on} of both the low-side and the high-side MOSFET switches can be calculated using following equation (5.48) [76],

$$R_{on} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{th})} \tag{5.48}$$

From equations (5.46) through (5.48), it can be clearly seen that the conduction losses of both the low and the high-side switches depend on the value of R_{on} as well as current flowing through switches, i_L. In case of a R_{on} value, as can be seen from equation (5.48), if the gate bias voltage, V_{GS}, is limited by the supply voltage of the system, and the values of μ, C_{ox}, and V_{th} are known and fixed by the design variable, then only term that a designer can deal with is the value of width, W, and length, L. Therefore, by optimizing the size of the transistors, a designer can achieve optimum R_{on} value for both the low and the high-side MOSFET switches. In general, with minimum size of L, larger W will give lower R_{on} value. To optimize the inductor current, i_L, one needs to deal with various terms since the inductor current depends not only on the turn-on time of the switches but also on the operating frequency of a DC-DC converter. In addition, the inductor current depends on the input and the output voltages of a DC-DC converter, Therefore, it is a very difficult and tedious procedure to get the right and the optimum value of it. As an example of the inductor current flowing through the switches, equations (5.49) and (5.50) show inductor current of DC-DC boost converter at a continuous conduction mode (CCM) and a discontinuous conduction mode (DCM), respectively.

$$I_{L_Avg} = \frac{V_{in}}{R_L(1-D)^2} \tag{5.49}$$

$$I_{L_Avg} = \frac{V_{in}D_1T}{2L}(D_1 + D_2) \quad (5.50)$$

where I_{L_Avg} is the average inductor current of CCM (5.49), and DCM (5.50),

D is the duty cycle of a DC-DC boost converter,

D_1 is the low-side duty cycle of a DC-DC boost converter,

D_2 is the high-side duty cycle of a DC-DC boost converter,

V_{in} is the input voltage of a DC-DC boost converter,

L is an inductor,

T is the period of a DC-DC boost converter,

R_L is the load resistor of a DC-DC boost converter.

As can be observed from equations (5.49) and (5.50), an inductor current depends on various parameters such as input voltage, switching frequency, on-time of low and high-side switches, inductor value as well as the load resistor value. In addition, an inductor current is varied by the mode of a DC-DC boost converter operation.

The gate and the inductor switching losses come from the fact that the gate of MOSFET transistor switches and other parasitic capacitances need to go through the phase of charging and discharging whenever switches are going through their *on*/*off* states. To calculate the gate switching power loss, the gate parasitic capacitance should be calculated first. The calculated gate parasitic capacitance is [77],

$$C_{Gp} = C_{ox}W_pL_p + 2C_oW_p \quad (5.51)$$

$$C_{Gn} = C_{ox}W_nL_n + 2C_oW_n \quad (5.52)$$

where C_{ox} is representing the gate oxide capacitance,

W is representing the width of a MOSFET transistor,

L is representing the length of a MOSFET transistor.

Using the value calculated in equations (5.5117) and (5.5218), the power loss due to the gate capacitance can be calculated with help of the following equation (5.5319) [78],

$$P_{Loss-Gate} = \left(C_{Gp} + C_{Gn}\right)V_{GS}^2 f \tag{5.53}$$

where C_{Gp} is representing the total gate capacitance of a *P*-type MOSFET transistor,

C_{Gn} is representing the total gate capacitance of a *N*-type MOSFET transistor,

V_{GS} is representing the voltage of gate-source,

f is representing the switching frequency of a DC-DC converter.

From equation (5.53), it can be observed that the loss due to the gate capacitance depends on the total parasitic gate capacitances as well as the switching frequency of a DC-DC converter. Therefore, to minimize the gate capacitance loss, it is important to reduce the switching frequency as well as the size of the switching MOSFET. However, as stated earlier, if a designer reduces the size of the switching MOSFET, then it will increase the conduction loss due to the increased R_{on}.

In addition, depending on the system requirement, it may not possible to reduce the switching frequency of a DC-DC converter. Decreasing switching frequency means increasing size of an inductor. Therefore, a designer should carefully decide between the conduction loss and the gate capacitance switching loss since there is trade-off them. In addition, at the point of V_{LX} in Fig. 5.21, there is a parasitic capacitance of an inductor as well as the switching MOSFET parasitic capacitance. The parasitic capacitance of an inductor can be calculated using equation (5.54) [79],

$$C_{par-ind} = \frac{\epsilon LW}{2t_{di}} \tag{5.54}$$

where ϵ is the permittivity of the surroundings and it can be expressed as $\epsilon = \epsilon_r \epsilon_o$,

L is the length of the spiral,

W is the width of the spiral,

t_{di} is the dielectric thickness in between the spiral inductor and substrate.

In addition, the total parasitic capacitance seen in the point of V_{LX} can be calculated as following equation (5.55) [78].

$$C_{par-s} = C_o(W_n + W_p) \tag{5.55}$$

Therefore, the loss due to the parasitic capacitance of an inductor as well as parasitic capacitances of switches can be calculated using equation (5.56) [78],

$$P_{L-M} = \left(C_{par-ind} + C_{par-s}\right)V_{out}^2 f \tag{5.56}$$

where V_{out} is the output voltage of a DC-DC converter.

Therefore, the total gate switching loss and an inductor switching loss can be calculated using equation (5.57) [78],

$$P_{sw-ind-gate} = \left(C_{par-s} + C_{par-ind} + C_{Gp} + C_{gn}\right)V_{GS}^2 f \tag{5.57}$$

The switching loss occurs because of the charging and discharging of the parasitic capacitance of MOSFET switches during a switching action. The switching loss depends on various kinds of parameters such as the time to charge, t_{on}, and the time to discharge, t_{off}. Therefore, the switching loss can be expressed as [80],

$$P_{sw} = \frac{I_L V_{DS}(t_{on}+t_{off})f}{2} + \frac{(C_{par-s}+C_{Gp}+C_{Gn})f}{2} \tag{5.58}$$

Therefore, the total loss of a switching DC-DC converter can be calculated by combing all the equations shown from (5.44) through (5.58).

5.5.4 RF Rectifier Test Results

5.5.4.1 Test Set-Up

Fig. 5.31 shows the chip layout as well as the chip microphotograph of the RF rectifier. The blue square shows the RF rectifier. It has been fabricated in a standard 130 nm CMOS process. The area of the RF rectifier is 232 µm x 662 µm approximately.

Since the RF rectifier operates at the frequency ranges of 895 MHz to 920 MHz, all the ESD pads are separated from other circuits used in a DC -DC boost converter so that its frequency cannot affect the operation of other circuits associated with a DC-DC converter.

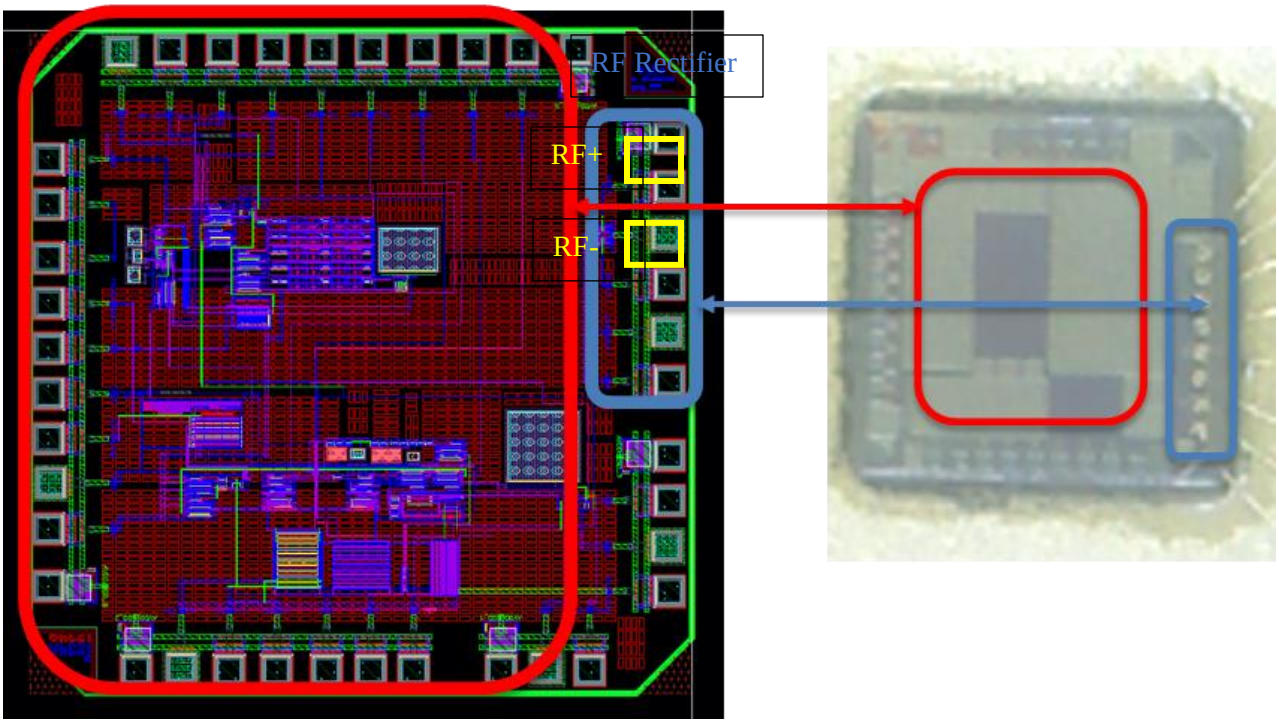


Fig. 5.31 Layout and photograph of a RF rectifier.

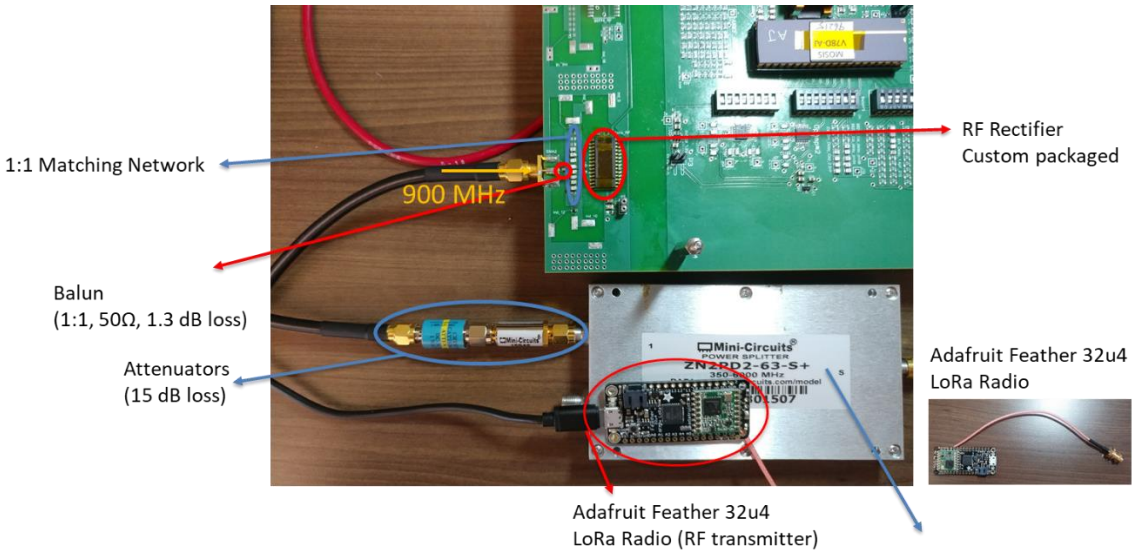


Fig. 5.32 RF rectifier test set-up.

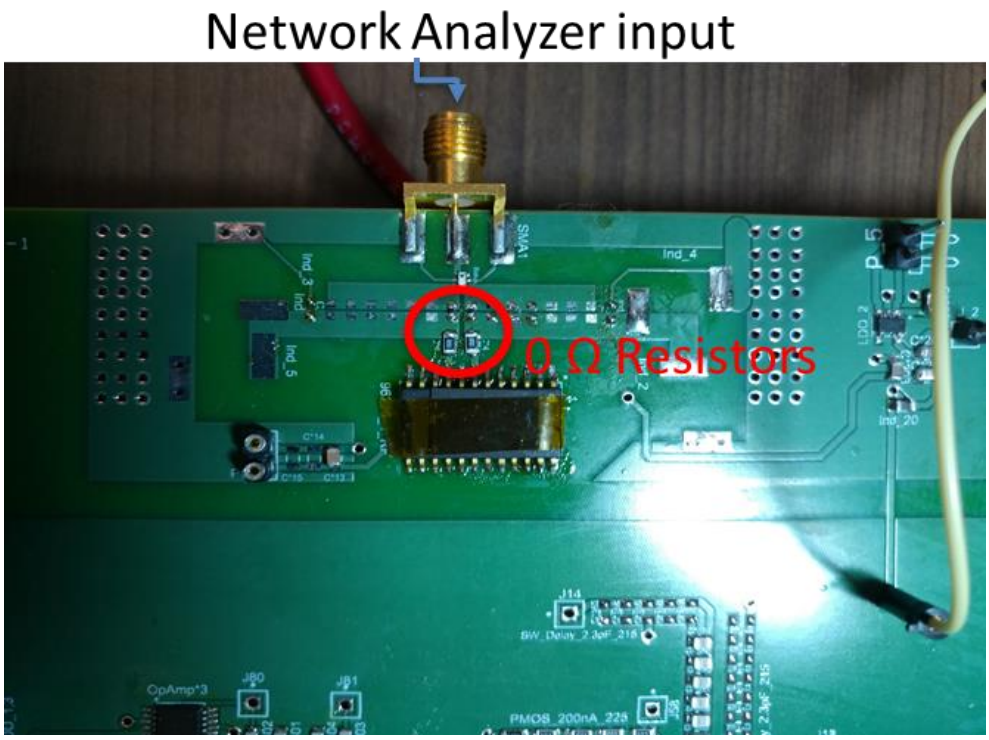


Fig. 5.33 The RF rectifier input impedance test set-up.

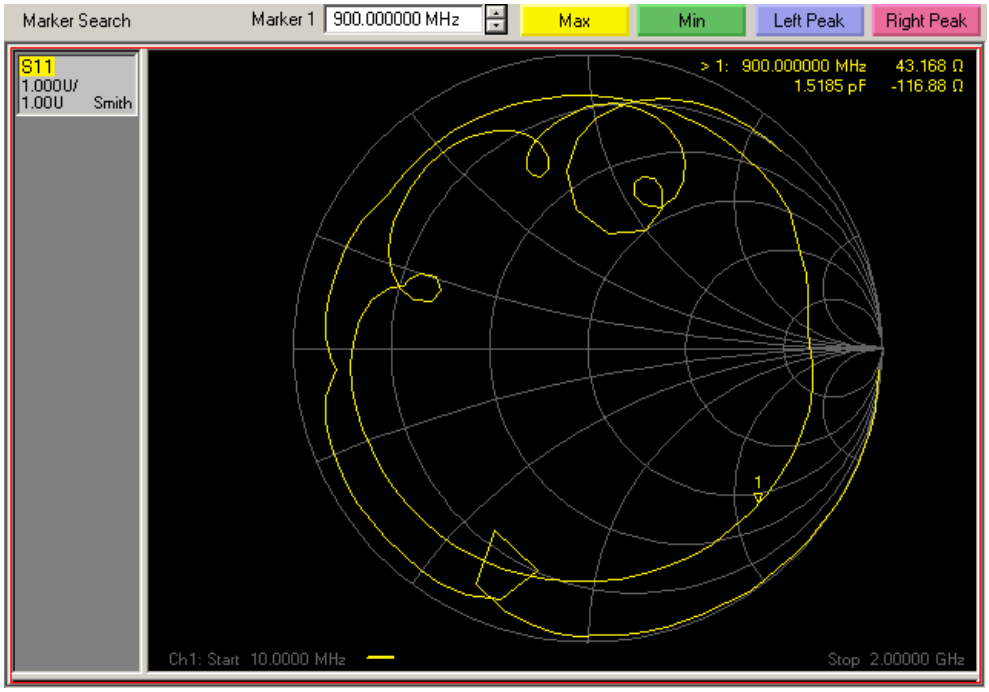


Fig. 5.34 RF rectifier input impedance testing with a network analyzer.

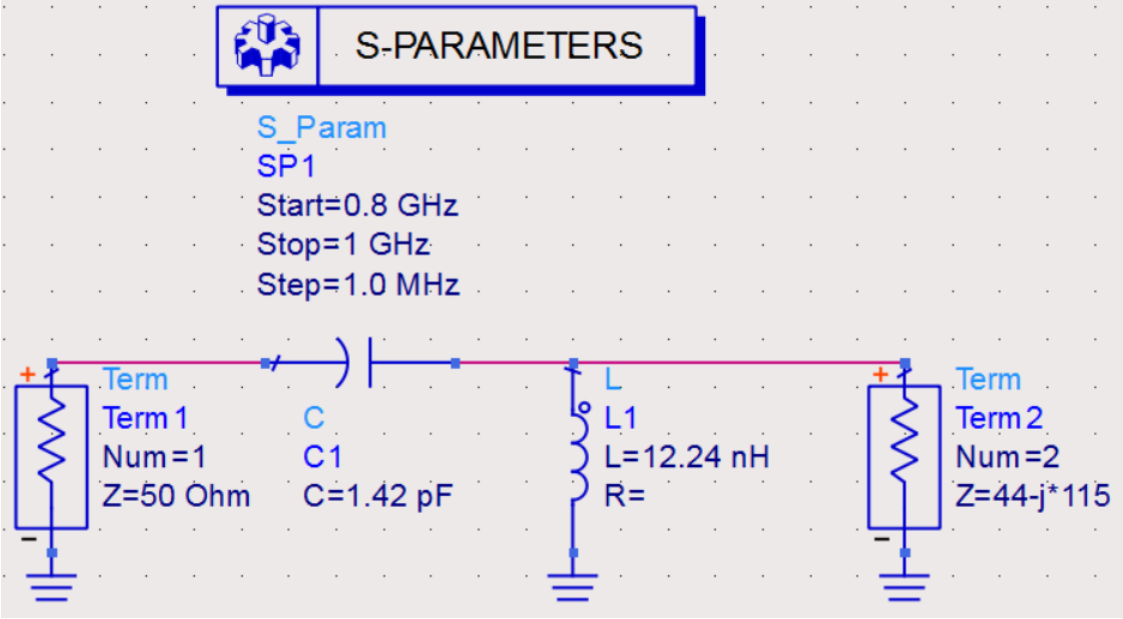


Fig. 5.35 RF rectifier matching circuit.

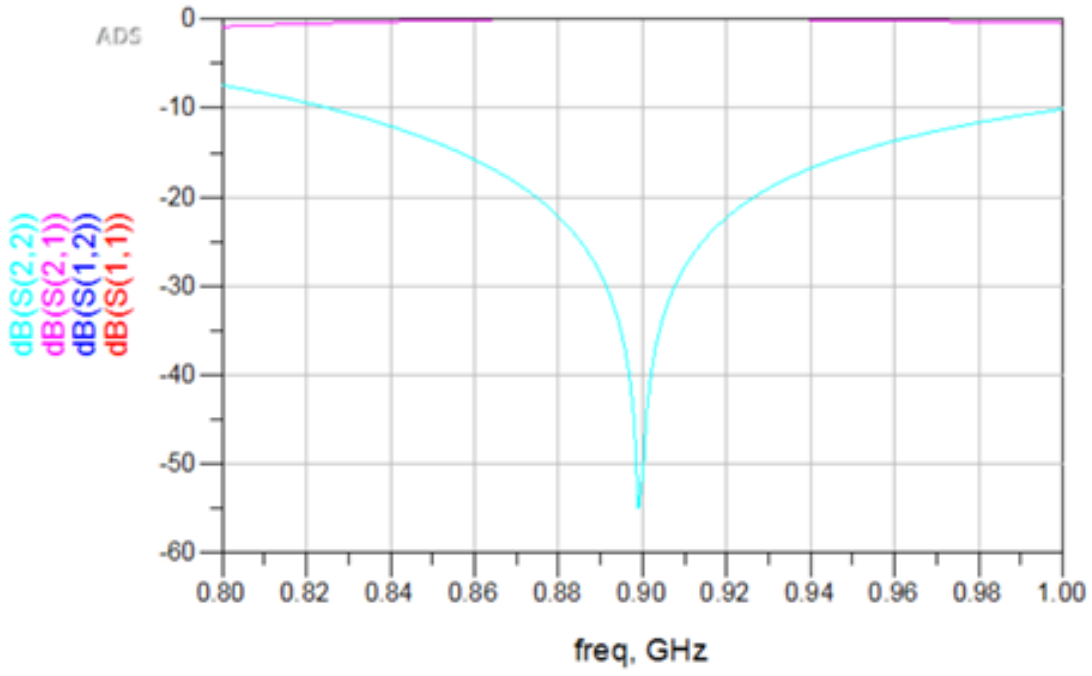


Fig. 5.36 S-parameter matching circuit simulation.

In addition, RF+ and RF- input ports are shielded with ground pads in between each RF input ports so that the signals cannot interfere with each other. Fig. 5.32 shows the test set-up of the RF rectifier.

The RF signal is coming from an Adafruit Feather 32u4 SX1276 Lora based RF signal generator. Its control unit is based on ATmega32u4 8-bit microcontrollers with Arduino libraries. Feather 32u4 can generator RF signal ranges from 868 MHz to 915 MHz. The power generated by Feather 32u4 is from + 5 dBm to + 23 dBm.

The brief specifications of the Feather 32u4 signal generator are listed below [81].

- SX1276 LoRa® based module with SPI interface
- Packet radio with ready-to-go Arduino libraries
- Uses the license-free ISM bands (ITU "Europe" @ 433MHz and ITU "Americas" @ 900MHz)
- +5 to +20 dBm up to 100 mW Power Output Capability (power output selectable in software)
- ~300uA during full sleep, ~120mA peak during +20dBm transmit, ~40mA during active radio listening.
- Simple wire antenna or spot for uFL connector

As can be seen from the specifications of the Feather 32u4 that the attenuators should be used to have desired power ranges of – 10 dBm to -2.5 dBm. Before the RF rectifier testing is performed, the input impedance of the RF rectifier should be measured so that a matching circuit can be implemented into the PCB board.

Fig. 5.33 shows the test set-up for the impedance testing. A signal from a network analyzer is connected by using a SMA connector with -10 dBm of input power with frequency ranges of 100 MHz to 2 GHz. Pre-printed PCB board is wired with 0 Ω resistors. The balun used in a PCB

is single to differential ended with 1.3 dB loss. Its input and output impedances are 50 Ω and it is 1-to-1 type of a balun.

Fig. 5.34 shows the input impedance of the RF rectifier. The measured value of the input impedance through the balun is 43 – 116j. As a next step of making a matching network, this measured value is plugged into ADS program so that the matching network can be calculated. Fig. 5.35 shows the ADS circuit simulation of the matching circuit. The matching network is formed with a simple *LC* network and the value plugged into ADS program is following.

C_{Match} is 1.42 pF, and
L_{Match} is 12.24 nH.

Fig. 5.36 shows the simulation results of S-parameter matching circuit. As it can be seen from Fig. 5.36, the calculated and the simulated values of the matching network suggest a well-designed circuit and frequency at 900 MHZ shows about -55 dBm gain.

5.5.4.2 Test Constraint of the RF Rectifier

Fig. 5.37 shows the circuit diagram of the ESD protection used in this RF rectifier while Fig. 5.38 shows the test set-up for the ESD leakage.

In Fig. 5.37, I/O pad are used at the output of the RF rectifier and the power protection is used at V_{DD_ESD} port which supplies voltage for the ESD power. In addition, *R* and *C* values used in the power protection pad are 1 MΩ and 1 pF, respectively, which will give time constant of approximately 1 μs.

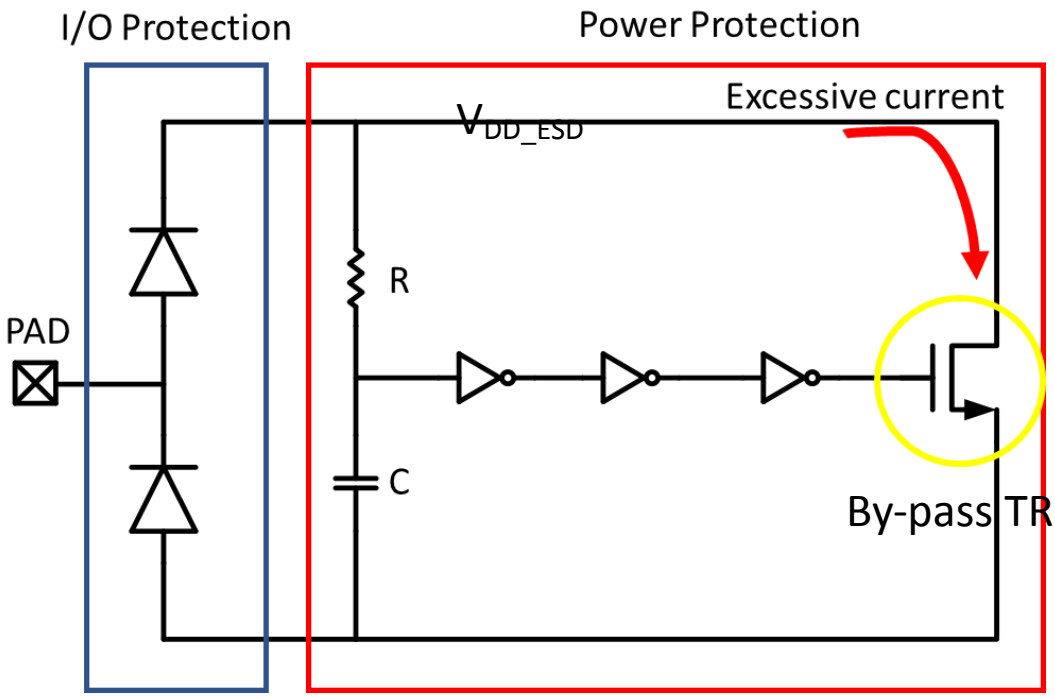


Fig. 5.37 ESD protection used in the RF rectifier.

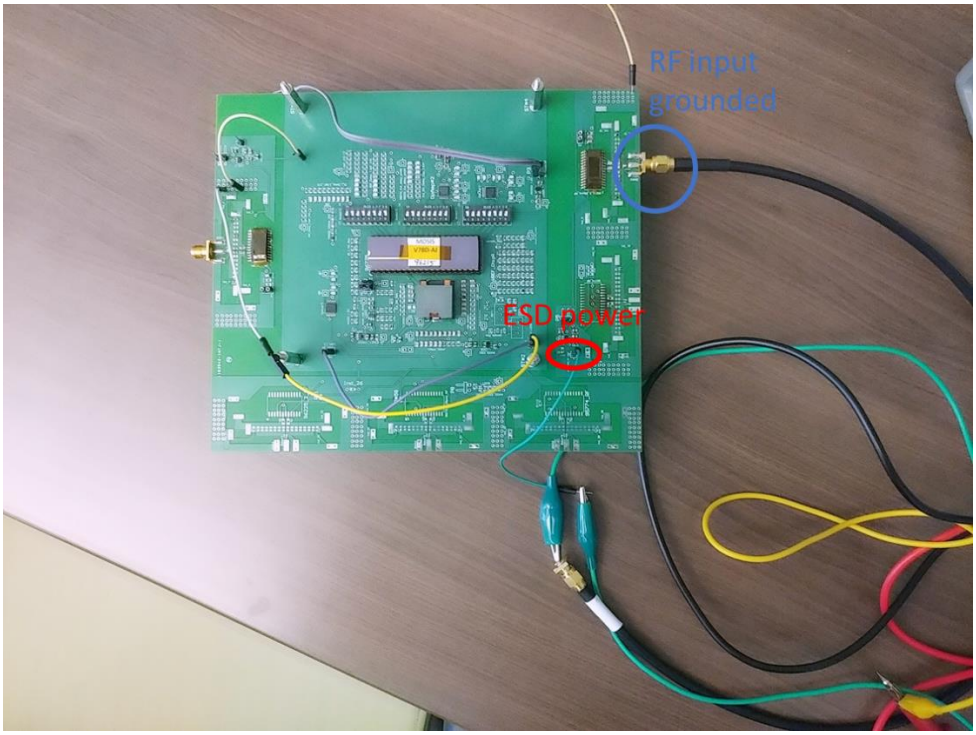


Fig. 5.38 ESD leakage testing set-up.

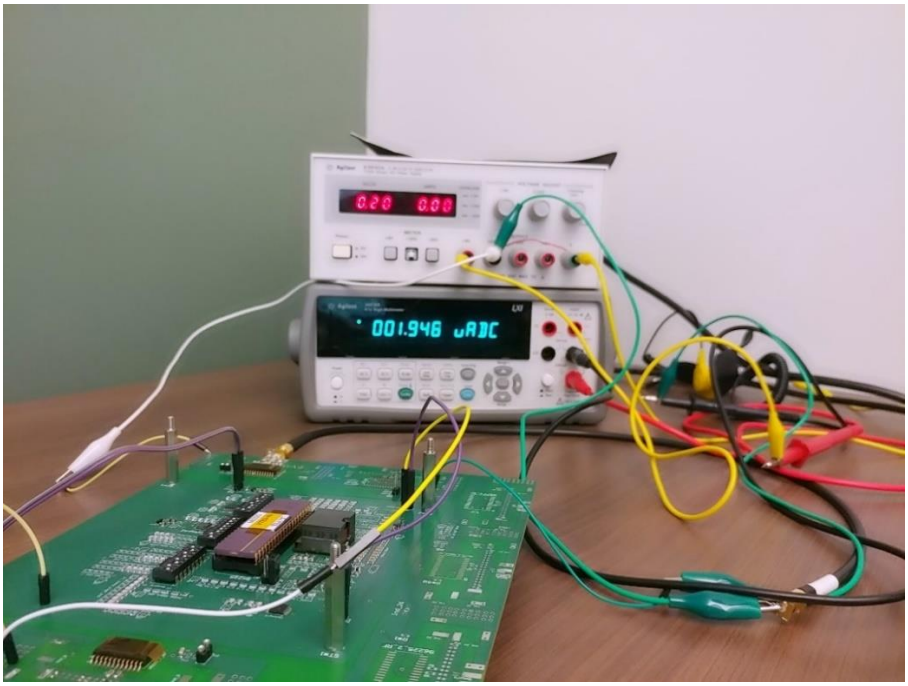


Fig. 5.39 ESD leakage testing at 0.2 V.

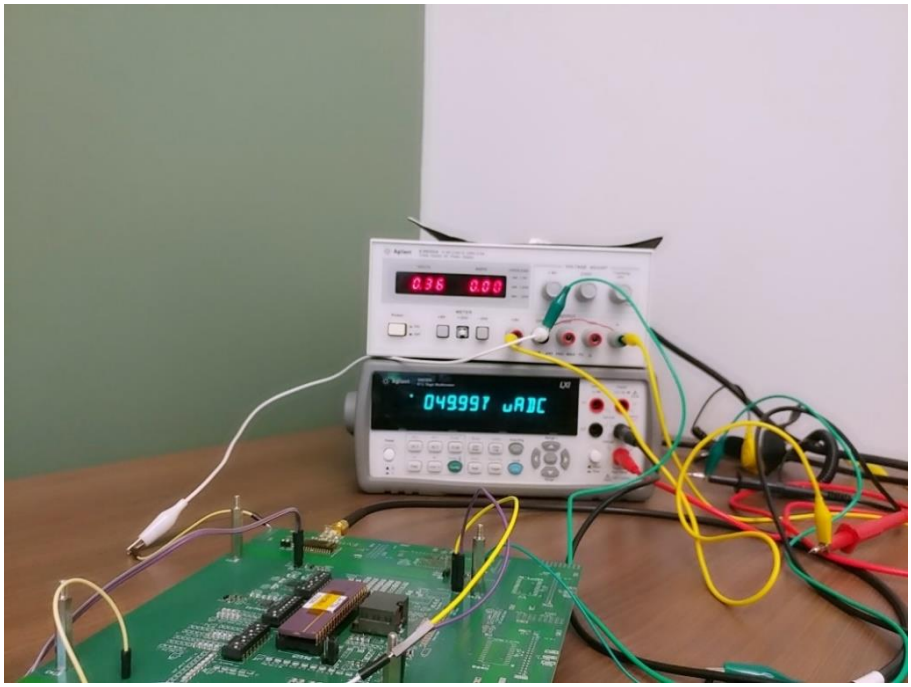


Fig. 5.40 ESD leakage testing at 0.36 V.

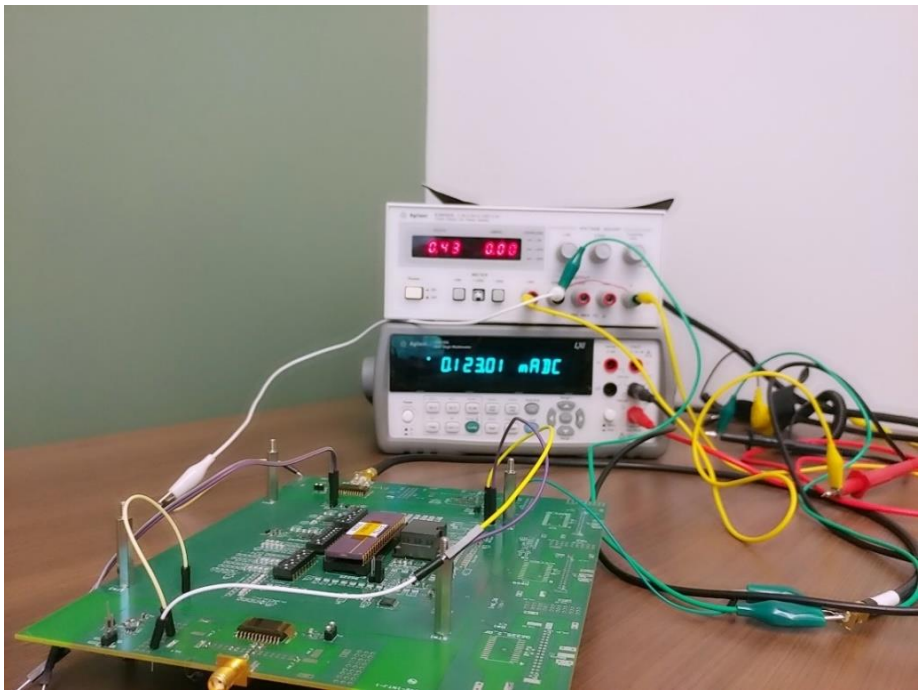


Fig. 5.41 ESD leakage testing at 0.43 V.

To test the ESD leakage, the input port of the RF rectifier is grounded through the SAM connected wire, and the ESD power is applied through the power supply to the ESD power port pin as shown in Fig. 5.38.

Fig. 5.39 through Fig. 5.41 shows the ESD test results at 0.2, 0.36, and 0.43 Volts respectivelyThe leakage current though the ESD at each ESD power is shows below. At 0.2 V, the leakage is about 1.9 µA, at 0.36 V the leakage current is about 50 µA, and at 0.43 V the leakage current is about 123 µA.

As can be seen from the test results, as the ESD power is increased, the leakage is also increased. Therefore, it can be concluded that the ESD cell is partially damaged and the cell is working as resistive network rather than a protection cell. The possible causes of such problem can be driven from the tested phenomena.

There are two problems that can hurt the ESD cell. Electrical overstress (EOS) and electrostatic discharge (ESD) are the two major problems that cause failure of the ESD cell. Usually, the duration of EOS is longer than the ESD time. As shown in Fig. 5.37, if very high voltage is applied through the V_{DD_ESD} in short time of nano-seconds, then the bypass TR should absorb all the excessive current so that the high current does not pass through the circuit to prevent the breakdown of the internal circuits. However, if the bypass TR is not capable of absorbing such high leakage current, then it will breakdown partially or completely. On the other hand, if the time constant formed by *RC* network is not long enough in ESD or EOS situation, it could also destroy the bypass TR because of lack of absorption of such high current for a long time. In addition, if excessive heat is applied during the packaging, it will cause breakdown of the protection cell as mentioned in reference [82]. Another possibility of destroying or partially destroying the ESD cell is that while packaging a chip or soldering a chip, excessive voltage applied into the pad can breakdown the back-to-back diode if the diode sustainable voltage is less than the applied excessive voltage, which will eventually make reverse biased the diode. To further observe the exact cause of the ESD cell problem, dissection of the chip will be required so that exact place of ESD failure can be pointed out and the causes of failure can be identified.

5.5.4.3 Testing the RF Rectifier

Section 5.5.4.1 discusses design of the matching network. The calculated values for C_{Match} and L_{Match} are 1.42 pF and 12.24 nH, respectively. The real value plugged into a PCB is 1.4 pF and 12 nH.

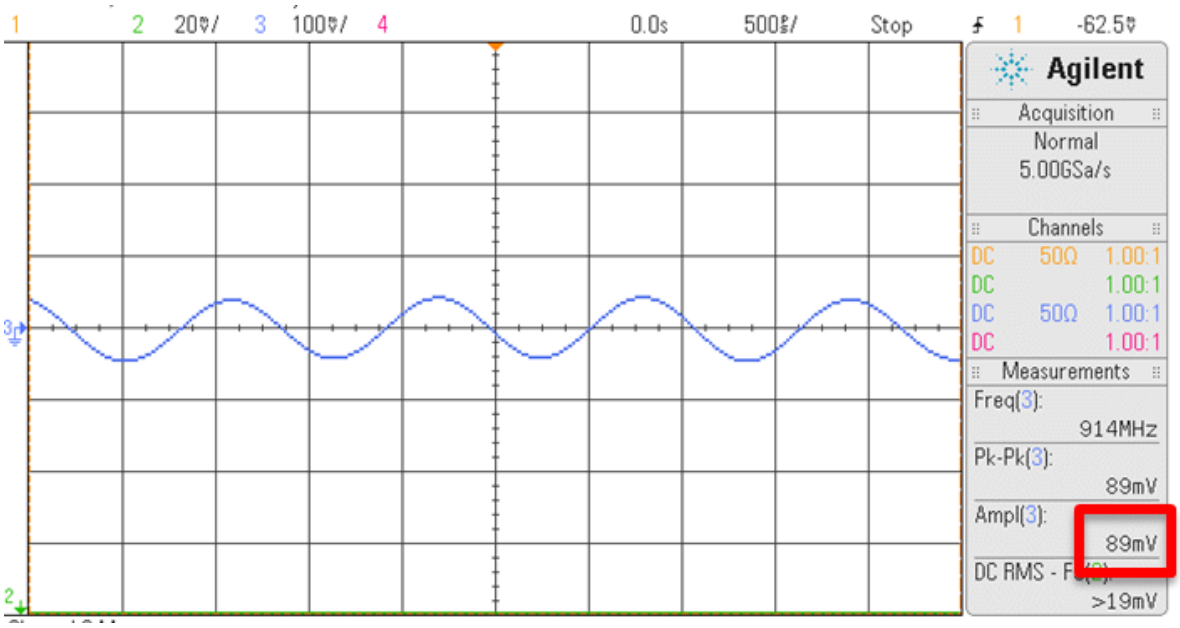


Fig. 5.42 RF rectifier input voltage (Both RF + and RF – sides).

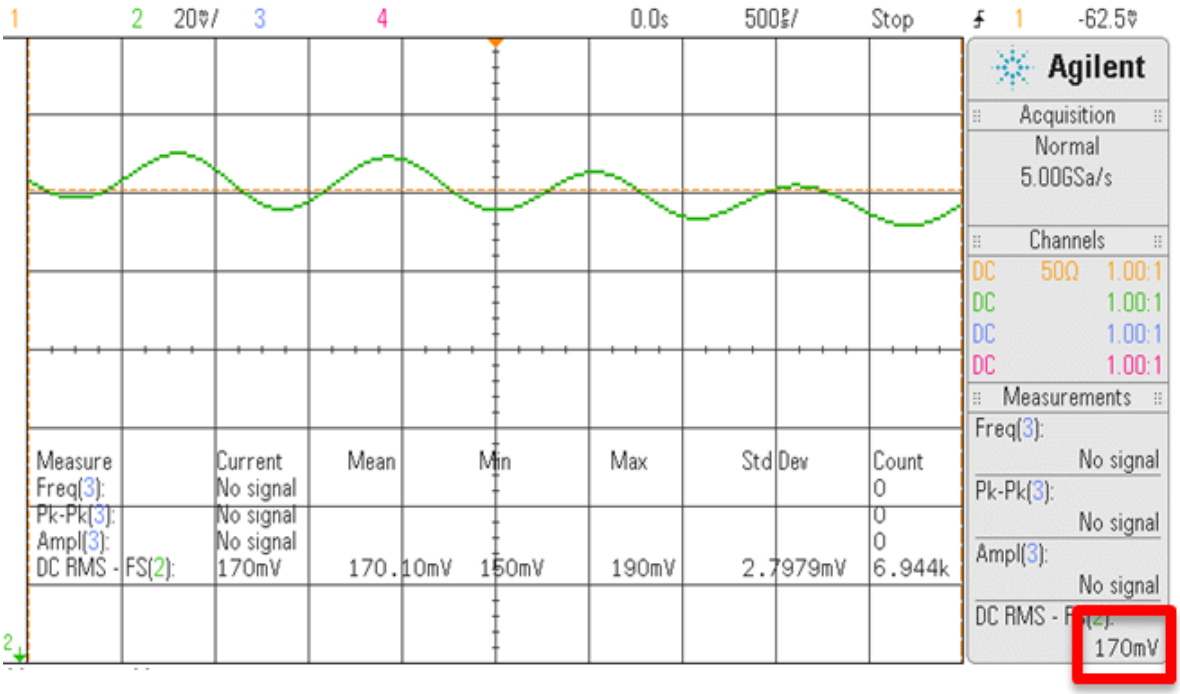


Fig. 5.43 RF rectifier output voltage.

In addition, as explained as in section 5.5.4.2, because of the ESD problem in the RF rectifier, testing of the RF rectifier cannot be performed properly. Therefore, testing has only been performed to check the functionality of the RF rectifier.

Fig. 5.42 shows the input voltage of the RF rectifier, which are RF+ and RF-. Fig. 5.43 shows the output voltage from the RF rectifier. With the input voltage of approximately 89 mV, the output voltage from the RF rectifier is about 170 mV. This means that the RF rectifier is working as expected. Recalling from the equation (5.13) in section 5.2.1 the output voltage of the RF rectifier is approximately twice of whatever the input voltage for the RF rectifier.

The equation of (5.31) can be rewritten approximately as equation (5.59),

$$V_{RECT} = 2V_{RF_IN} \tag{5.59}$$

5.5.5 Testing the DC-DC Boost Converter

Fig. 5.44 shows the layout as well as the chip photograph of the proposed DC-DC boost converter with MPPT. The red box shows the DC-DC boost converter and yellow box shows the proposed maximum power point tracking (MPPT) system in the proposed DC-DC boost converter. The chip size of the DC-DC boost converter is approximately 1500 µm x 1500 µm, and the MPPT is about 253 µm x 230 µm. The chip has been fabricated in a standard 130 nm CMOS process. Due to the ESD problem with the RF rectifier circuit, the input power for the DC-DC boost converter is coming from the equivalent RF rectifier model.

Fig. 5.45 shows the equivalent circuit of the RF rectifier used for the input of the DC-DC boost converter.

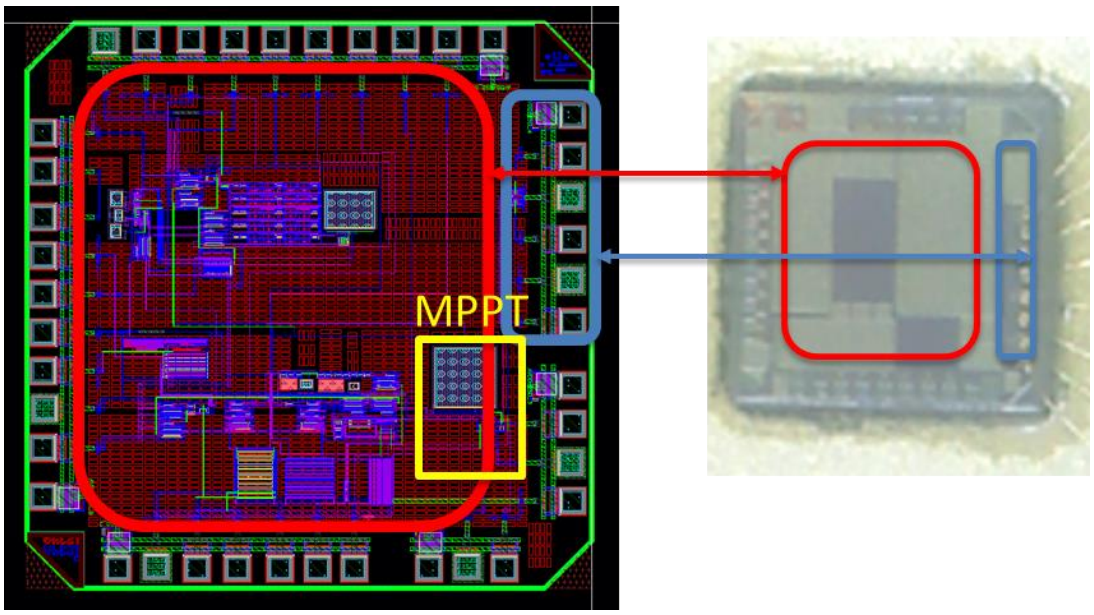


Fig. 5.44 RF DC-DC boost converter layout and chip photograph.

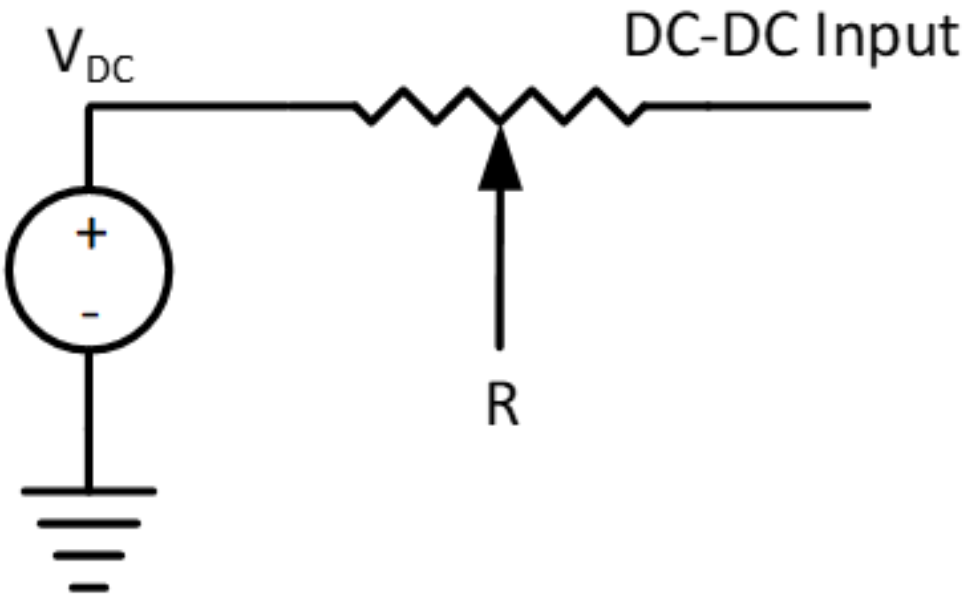


Fig. 5.45 The RF equivalent circuit used for the input of the boost converter.

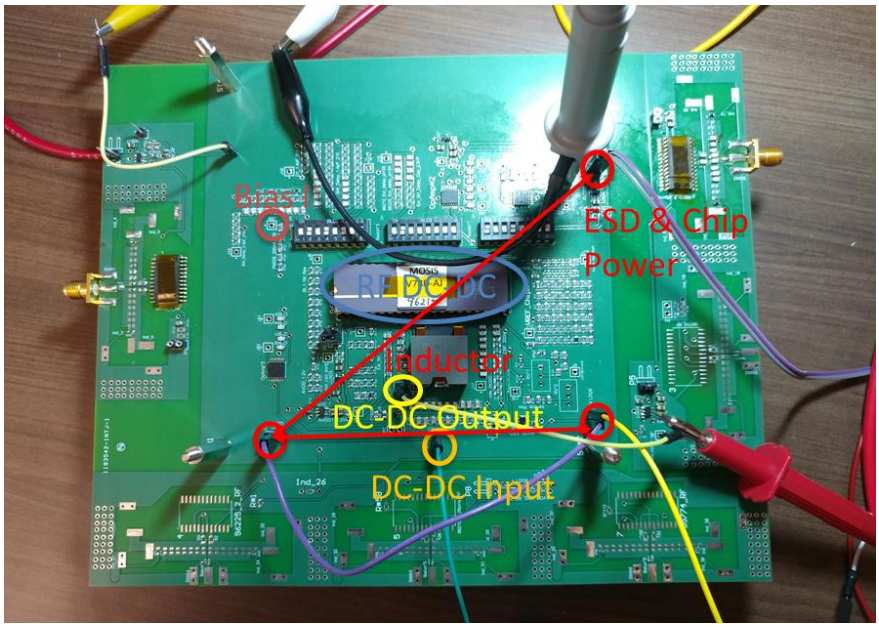


Fig. 5.46 The RF DC-DC boost converter test set-up.

The V_{DC} ranges used for the input of the boost convert is from 0.62 V to 0.78 V, and the variable resistor, R ranges from 10 KΩ to 20 KΩ.

Fig. 5.46 shows the test set-up. The blue circle shows the RF DC-DC boost converter chip and the inductor used in the system is 30 µH. The red circle shows the ESD power as well as chip power sources which are provided by the low-drop regulator.

The ESD power is 1.5 V and the chip power is 1.2 V. The DC-DC input power is coming from the circuit shown in Fig. 5.45 to the point shown in the orange circle in Fig. 5.46.

First, the testing of the bias current generator is performed. Since the bias current is one of the core circuits that provides all the necessary bias current for the comparator, buffers, and oscillator, the accuracy of the bias current is important to measure. Fig. 5.47 shows the test result of the bias current.

The biasing current is measured through 5 MΩ of externally-connected resistor, as shown in Fig. 5.46 indicated with light red circle.

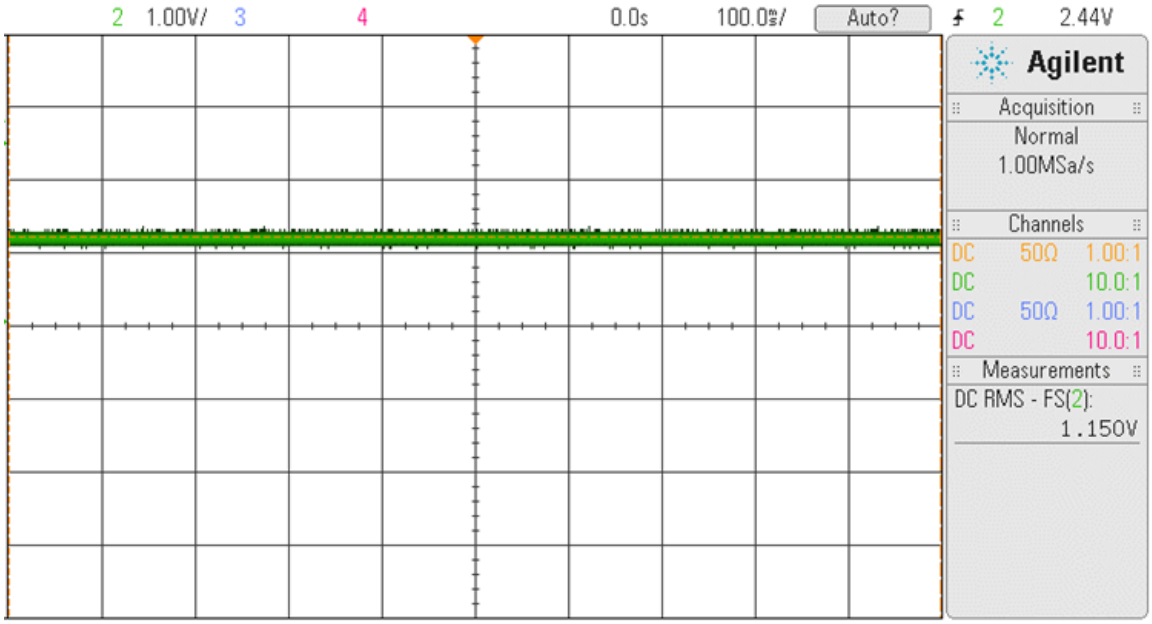


Fig. 5.47 The bias current test.

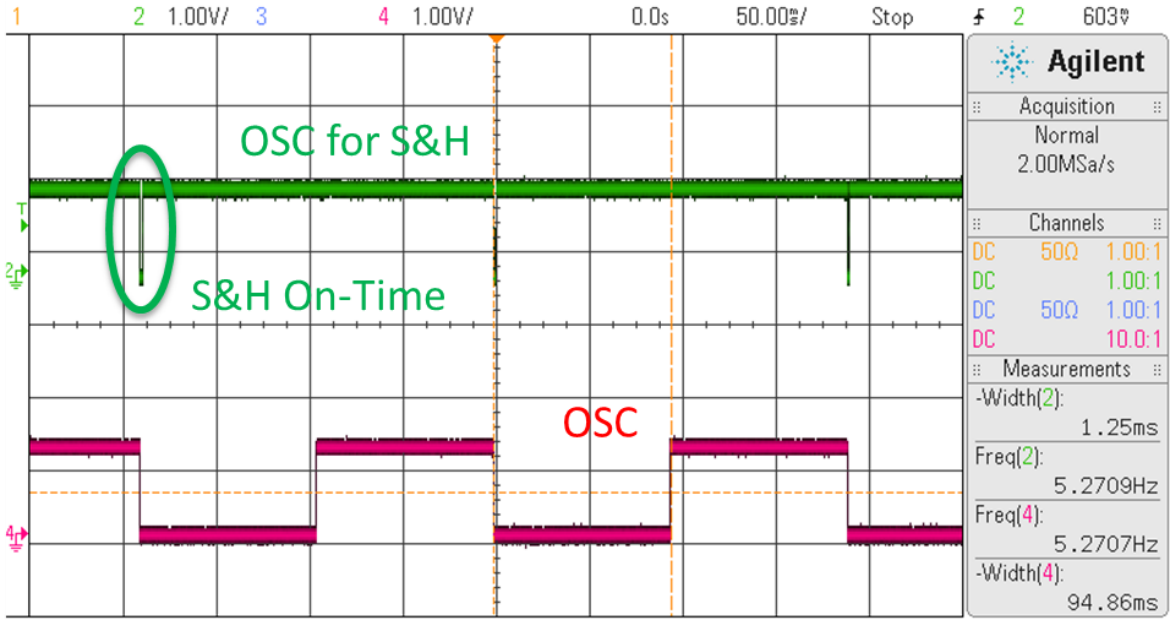


Fig. 5.48 Sample and hold control signal (Oscillator) test.

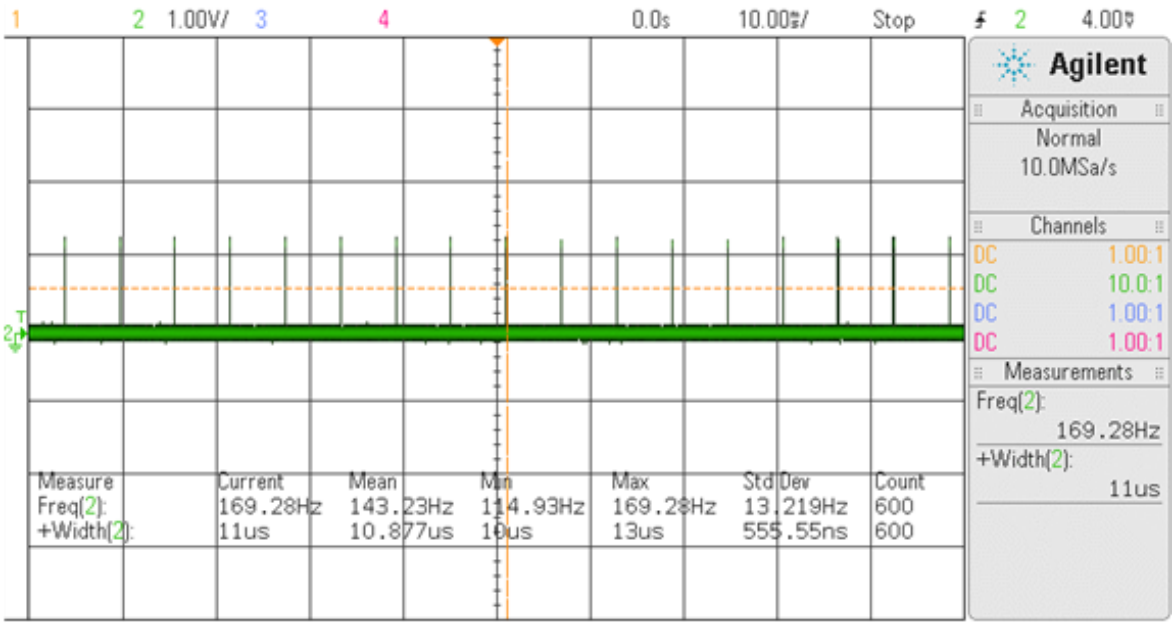


Fig. 5.49 NMOS on-time waveform at – 7.5 dBm.

Fig. 5.48 shows the waveform of the oscillator used in sample and hold circuit of the MPPT. The simulated frequency of the oscillator is 5 Hz and the measured frequency is 5.2 Hz. The difference is only 0.2 Hz and it is due to the parasitics associated with the PCB, the socket and the chip package. This measured frequency also verifies that the current generated by the biasing circuit, which is 200 nA is very close to the original value.

The red waveform is the oscillator and the green waveform shows the actual oscillator signal used in the MPPT system in Fig. 5.48.

In green waveform of oscillator for the MPPT, the pulse width is about 1.25 ms while the simulated value is 2 ms. This pulse width of the oscillator signal is for due to the charging time of the sampling capacitor as shown in Fig. 5.22 as C_1. In the testing procedure, 1.25 ms of width was sufficient time to charge, C_1, so it was not necessary to increase the width of the oscillator. Since the width of oscillator signal is externally programmable, it can be increased or decreased by using the external capacitor whose value used in the test board is 2.5 nF.

Since one of the current mirror legs is pulled out to measure the current, the external resistor is used to measure the current that is generated by the current bias circuit.

The internal current biasing circuit generates 200 nA. As a result, with 5 MΩ of external resistor, the biasing circuit should generate 1 V. However, due to the parasitics generated by the PCB, the chip package as well as the socket used to connect the chip, the final measured result for the biasing circuit is 1.15 V, which is considered as very close to the actual design value of 200 nA.

Figs. 5.49 and 5.50 show the on-time waveform of the proposed DC-DC boost converter. Since the on-time of NMOS switch is one of the important parameters along with inductor value as well as the switching frequency, which determines the actual input impedance of the boost converter, it is important to measure the on-time of the NMOS switch width. Fig. 5.49 shows the measured waveform at – 7.5 dBm and Fig. 5.50 shows the measured waveform at –10 dBm.

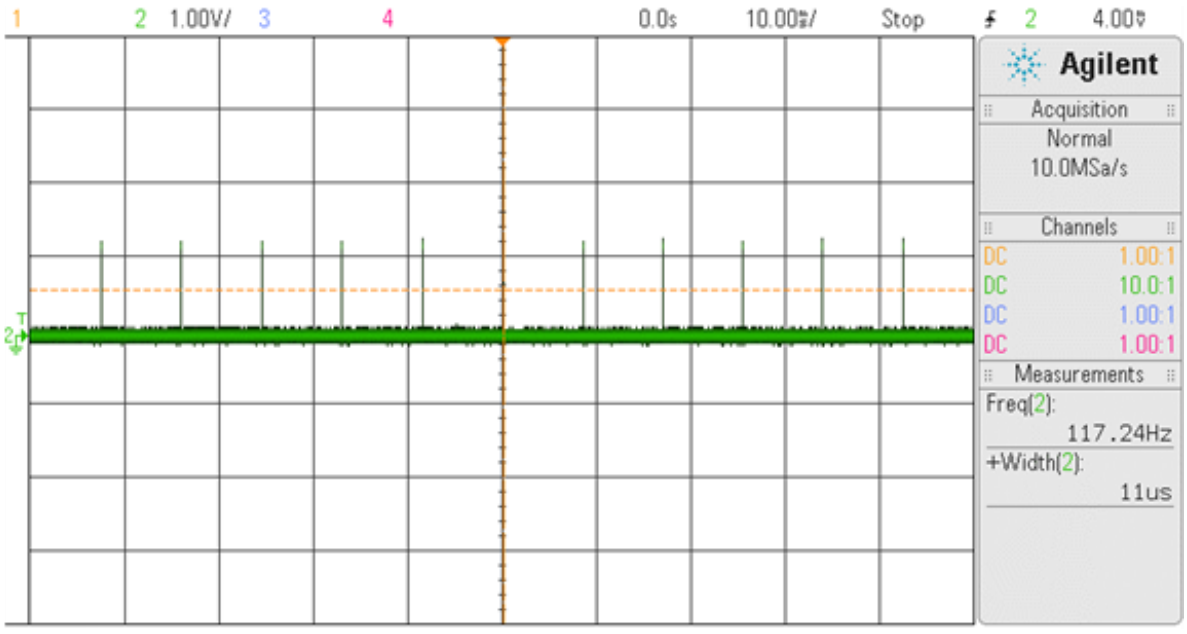


Fig. 5.50 NMOS on-time waveform at – 10 dBm.

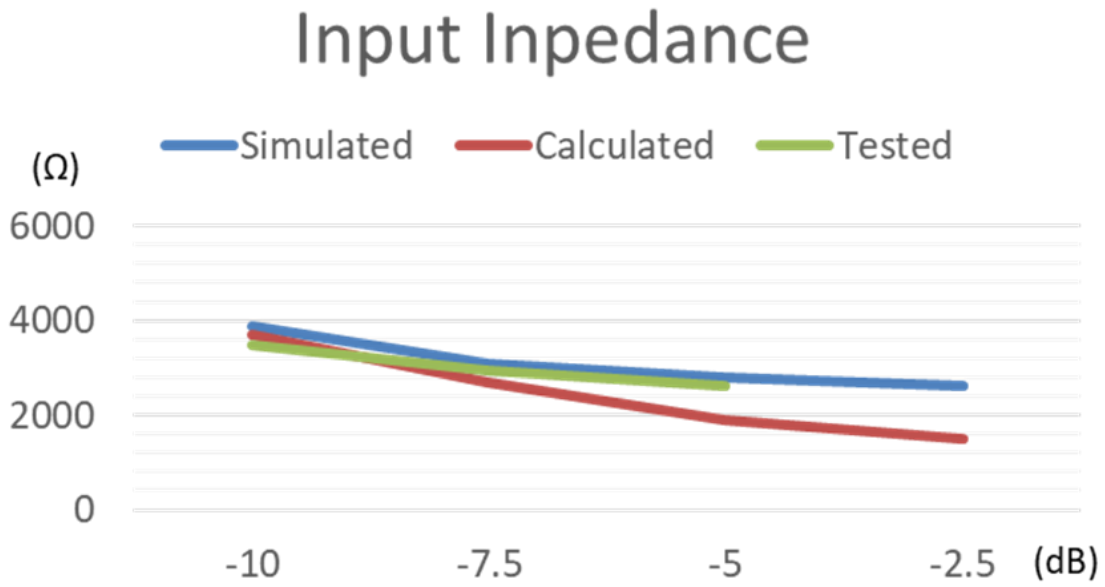


Fig. 5.51 Comparison of the input impedance of DC-DC boost converter.

Table 5.5 Measured Input Impedance of the Proposed DC-DC Boost Converter

Input Power (dBm)	L (µH)	t_1 (µs)	f_s (Hz)	R_{input_tested} **(Ω)**	R_{opt} **(Ω)**	Difference R	C_{Rect} (µF)	C_{IN} (µF)	C_L (µF)
-10	30	12	120	3470	3700	228	0.9	0.2	5
-7.5	30	11	169	2930	2700	234	0.9	0.2	5
-5	30	11	189	2620	1900	724	0.9	0.2	5

where R_{input_test} is measured input impedance of the proposed DC-DC converter,

R_{opt} denotes the optimum output impedance of the RF rectifier,

and *Difference R* denotes the difference between R_{input_tested} and R_{opt}.

Table 5.5 shows the summary of the measured input impedance of the proposed DC-DC boost converter. Fig. 5.51 shows the comparison of calculated, simulated and test values of the input impedance. As can be seen from Fig. 5.51 as well as Table 5.5, the proposed MPPT structure is very effective design in terms of controlling the input impedance of a DC-DC boost converter compared with a conventional MPPT system controlled by an ADC. Since the proposed architecture of the MPPT system is consuming only less than 1 µA of current, it has a lot of advantage in terms of current consumption with comparable input impedance control for the maximum matching between the RF rectifier and the DC-DC boost converter.

In addition, this measured width of the DC-DC boost converter with the frequency verifies the equation (5.42), which is $R_{in} \approx \frac{2L}{t_1^2 f_s}$.

Fig. 5.52 shows the output waveform of the DC-DC boost converter at –10 dBm. The simulated output voltage is about 0.98 V but the measured value is about 1.3 V.

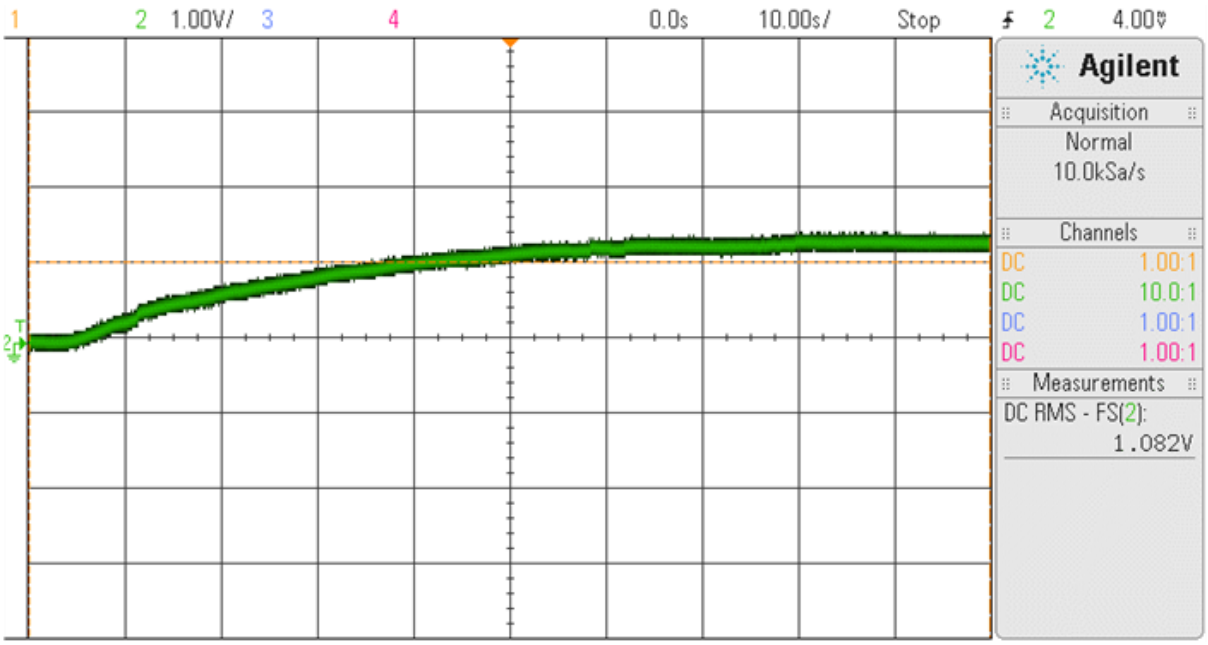


Fig. 5.52 The output voltage of the DC-DC boost converter at – 10 dBm.

The difference is due to the high parasitic component of the socket. Usually, the parasitic components of the connecting socket are very high. As a result, the output voltage of the proposed DC-DC boost converter is higher than the simulated value. Fig. 5.53 shows the inductor switching node, V_{LX} voltage. As can be observed from Fig. 5.53, the peak voltage is over 3 V which is much higher than the ESD limiting voltage, which is 1.5V. Therefore, the energy that is supposed to be stored into an inductor is limited by this peak voltage since over 1.5 V of peak voltage will be wasted by the ESD power.

As a result, huge loss occurs because of this very high peak voltage at the switching node, V_{LX}. The high peak voltage is coming from the parasitic components of the PCB, package and socket used in the testing. The main parasitic that causes this high peaking voltage is coming from the socket. Therefore, socket should be removed for the future revised version.

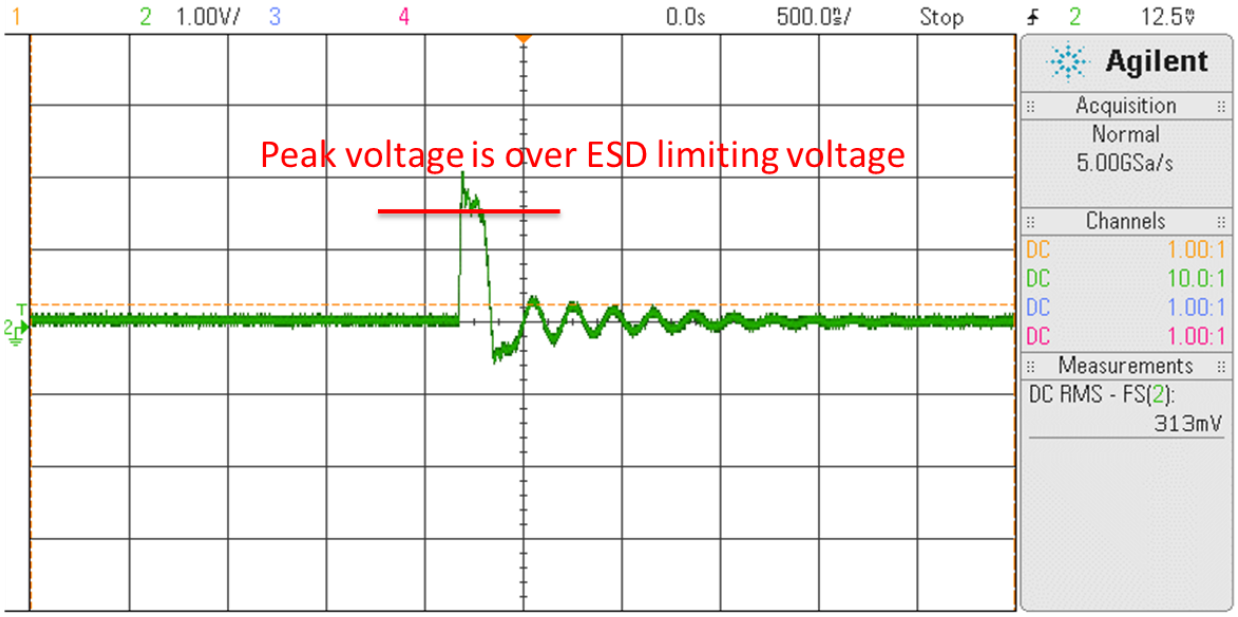


Fig. 5.53 The switch node, V_{LX} voltage of the DC-DC boost converter at – 10 dBm.

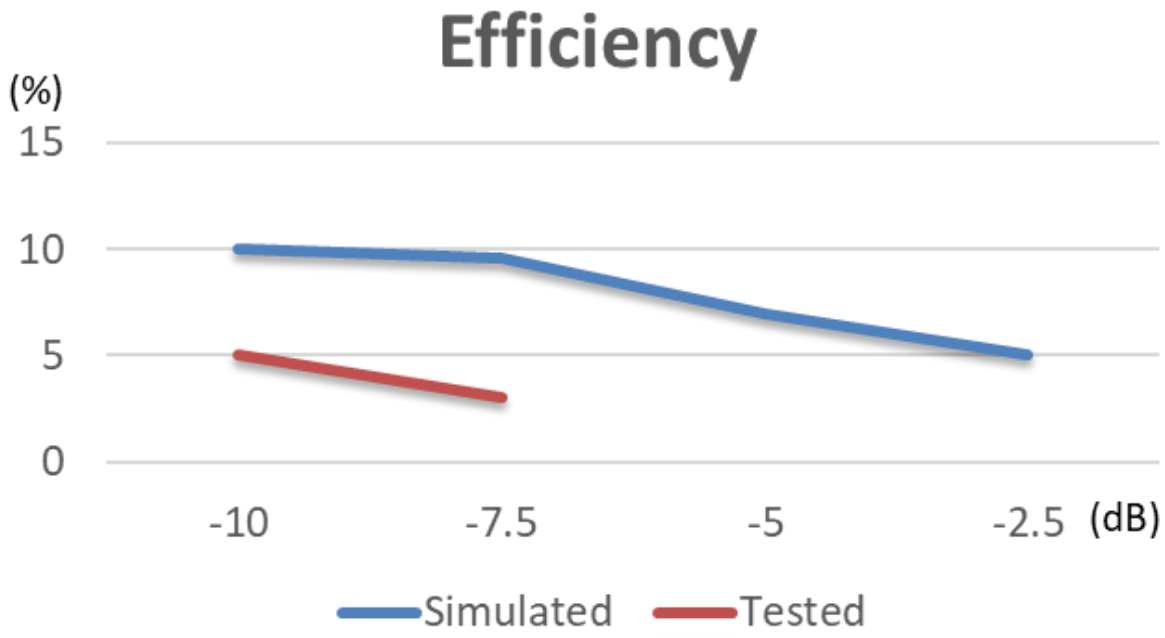


Fig. 5.54 The measured and simulated efficiency of the DC-DC boost converter.

Fig. 5.54 shows the efficiency of the proposed DC-DC boost converter. As explained in previous paragraph, due to the high peak voltage at the switching node, the energy loss is very high. As a result, the efficiency is degraded, and even at higher input power of – 7.5 dBm, the efficiency cannot be measured due to this high peak voltage.

CHAPTER 6 – CONCLUSION AND FUTURE WORKS

6.1 Conclusion

In this research, a piezoelectric transducer-based energy harvesting as well as radio frequency-based energy harvesting systems have been presented. A piezoelectric transducer-based energy harvesting system can be implemented into a system where a moving or shaking is utilized such as in wrist watches, shoes, automobiles, bridges etc. An energy harvesting system based on vibration presented in this research is focused on very low input power. The reason for focusing on very low input power is that the input power from a vibration-based energy source is not always adequate. Even with very low available input power, if the system can harvest the energy it can contribute to extension of the life of battery. The proposed piezoelectric transducer-based energy harvesting system shows this possibility of harvesting even very low available input power. In the second part of this dissertation, a RF based energy harvesting system has been presented. The proposed system showed the new approach of maximum power point tracking (MPPT). Unlike previous reported RF energy harvesting systems using ADC as the main controlling source of MPPT, the proposed MPPT system is composed with simple resistive network with storage capacitor and buffer. With this simple design, the proposed MPPT system does not require any calibration whenever the system is powered off. The conventional MPPT system with ADC actually requires calibration if there is no stored calibration data such as MCU or memory. In addition, the proposed system is using only less than 1 μA of current consumption, which is substantially less than typical ADC controlled MPPT system.

6.2 Future Works

For the future works, a piezoelectric transducer with specific parasitic components value such as C_P and R_P can be made and calibrated. With this specially made piezoelectric transducer, the energy harvesting system based on a vibration can be tested properly. In addition, for the RF energy harvesting system, a well-made ESD for the RF rectifier should be used. In addition, the ESD cells used in the switching node, V_{LX} should be replaced with metal pads so that the peak voltage does not affect the overall system efficiency.

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VITA

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