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Characterization of Processes used in Nanofabrication of Digital Electrostatic E-Beam Array Lithography (DEAL) Devices

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Ryan Benjamine Rucker

December 2006

Dedication

I want to give all the credit of my accomplishments to the Lord for giving me the ability to do this research. This thesis is dedicated to my girlfriend, Brittany Taylor, and my family for their continuous encouragement during the course of my research. I want to also dedicate this thesis to my grandparents, Gene and Betty Helton, for their continuous prayer and interest in the importance of my success. I want to give dedication to my good friend, Erin Amanda Kapp, for her support and encouragement for my success in my research, while helping me not to loose focus on the Lord. I want to give a dedication to Dr. Steven Randolph for his teaching and interest to see me succeed in my research. Finally, I want to dedicate this thesis to my advisor and good friend, Dr. Philip Rack. His support and belief in my abilities to succeed are why I have made it to this point in my life.

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I would like to thank Dr. Steven Randolph for assisting me and my research during my graduate work. Dr. Randolph has been a friend and a wonderful mentor to me and many thanks are due him. I would like to thank the members of our research group, Dr. Yingfeng Guan, Jon Peak, Jungwon Park, Matthew Lassiter, and Daryl Smith along with all past members of the group, Dr. Yuepeng Deng, Dr. Jason Folwkes, Dr. Steven Randolph, and Dr. Seung-Ik Jun. For the help that I received at Oak Ridge National Laboratory, I would like to thank Dr. Steven Randolph, Dr. Larry Baylor, Dale Hensley, and Darrell Thomas. Without their teaching and guidance, this work would not be possible. Finally, I would like to thank my committee members: Dr. Philip Rack, Dr. Tom Meek, and Dr. Syed Islam. Their encouragement and expertise were essential for my achievements.

Abstract

The ultimate goal of this research was to nanofabricate an advanced field emission electron beam lithography platform using an electron beam induced deposition process (EBID) to deposit tungsten (W) nanofibers cathodes. In order to fabricate the devices, it was necessary to characterize the reactive ion etching (RIE) processes for the fabrication of the Digital Electrostatic e-beam Array Lithography (DEAL) device. To optimize the reactive ion etch processes of the silicon and silicon dioxide layers, a JMP desktop statistical discovery software from SAS® was employed to design a set of experiments. The design of experiments (DOE) employed variable conditions of R.F. power, gas pressure, and gas ratios. Specifically for the silicon etch DOE the R.F. power ranged from 100 to 400 (W), the gas pressure ranged from 75 To 400 (mTorr) and a SF_6/O_2 gas flow ratio varied from 2 to 10. Single crystal silicon wafers were used due to the thickness of the n^+ polycrystalline silicon film and the effectiveness of characterizing such a thin film. The responses that were measured included the silicon etch rate, the silicon to silicon dioxide etch selectivity, the silicon to photoresist etch selectivity, and the silicon etch profile. For the silicon oxide etch DOE, the R.F. power ranged from 200 to 300, the gas pressure ranged from 30 to 70 and a CF_4/CHF_3 gas flow ratio varied from 0.34 to 1.34. The responses that were measured included the silicon oxide etch rate, the silicon oxide to silicon etch selectivity, and the silicon oxide to photoresist etch selectivity. The results from both experimental designs adequately optimized the etch processes for the n^+ polycrystalline silicon and silicon oxide and will be used for

subsequent nanofabrication of DEAL devices. A DOE for the growth of tungsten nanopillars via electron beam induced deposition (EBID) was also performed as a method to deposit nanoscale field emission cathodes. The goal was to correlate the growth parameters to the nanopillar structure and ultimately the structure to the field emission properties. The DOE varied the precursor pressure, beam energy, and specimen current, and the responses were growth rate, nanopillar width, and the sharpness of the nanopillar tip. An optimum high growth rate, sharp pillar process was determined, however field emission the field emission measurements could not be made.

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Chapter 1—Introduction

1.1 Introduction

The need to revolutionize fabrication processes of nanoscale devices is critical for the enhancement of nanotechnology. Nanotechnology processing incorporates a variety of different steps to produce a device. The processes include: thin film deposition, optical and immersion lithography, dry and wet etching, and a variety of other procedures that are depictive of the fabricated device. The ultimate goal of this research was to nanofabricate an advanced field emission electron beam lithography platform using an electron beam induced deposition process to deposit tungsten nanofibers cathodes. Subsequently, this introduction will review electron beam induced deposition (EBID), advancements in lithography, and the study of field emission in electronic devices.

1.2 Electron Beam Induced Deposition (EBID)

Advanced processes for the development of nanoscale materials is a critical component in the world of nanotechnology. Therefore, new and existing techniques need to be developed and advanced, respectively. An area that has received considerable attention is electron-beam-induced deposition (EBID). The EBID technique employs an electron beam to decompose a pre-cursor molecule (the compound or species to be deposited) leaving a non-volatile material on a solid substrate. The EBID pre-cursor molecule is classically a vapor, but the process can also use a precursor of a liquid or

viscous solid deposited on a substrate. EBID has the advantage of direct deposition of three-dimensional structures on almost any target geometry.

The EBID process was first introduced as a common effect in electron microscopy identified as carbon contamination or carbon staining.[1] Carbon contamination occurs as an electron beam is directed towards a surface in an electron microscope in the existence of a carbonaceous species such as oils found in vacuum pumps.[1] Hart *et al.* described the results of carbon contamination of a substrate surface from high-energy electron bombardment on the surface of a substrate in the presence of a carbon-containing gas.[2] The research demonstrated that contamination is the product of an electron interaction with the precursor material.[2] The EBID process is shown in Figure 1-1.

1.2.1 EBID Applications

Because of its versatility to deposit many different materials and the need for a high-resolution process, EBID is a unique technique for a variety of nanoscale applications. Not only has EBID demonstrated 1nm resolution capabilities, it also has the capability of fabricating three dimensional features.[3] EBID is a top-down technique (a top-down nanofabrication technique is the process of taking any application and shrinking it down to the nanoscale), which may not immediately be used in high-throughput applications because of its serial nature, but the technique can contribute significantly to the development of two-dimensional and three-dimensional nanostructures, such as conductive wires [4] and tips for scanning probe microscopes.[5]

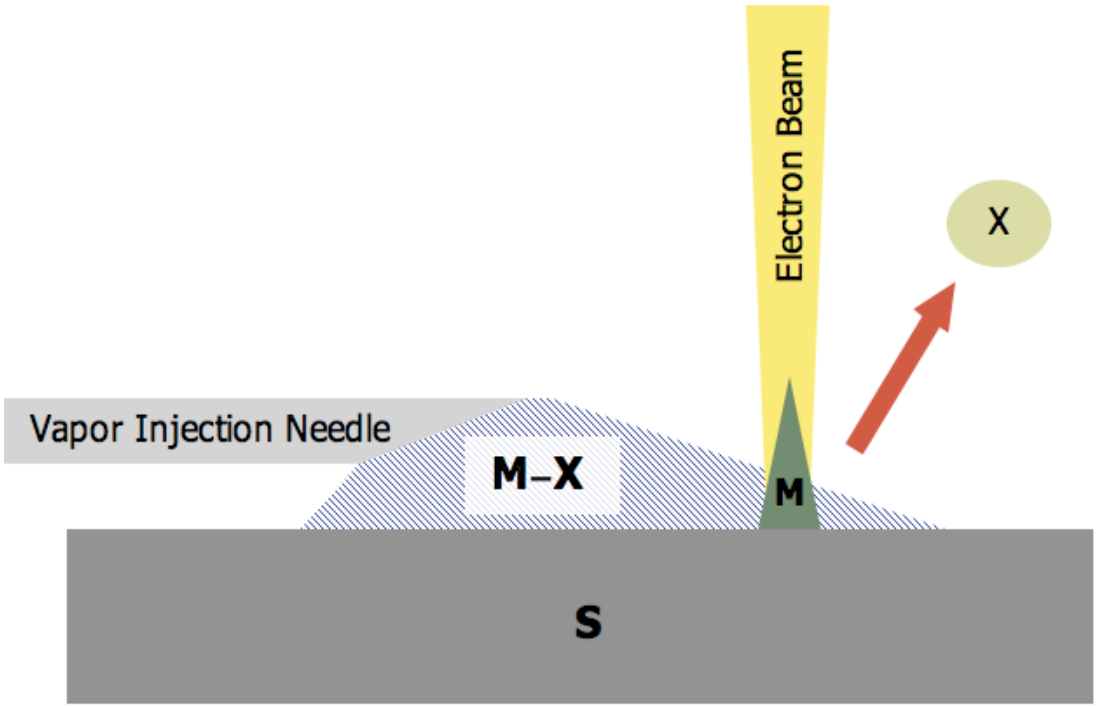

Figure 1-1 Schematic of the EBID Process.

Reused with the permission from S.J. Randolph, Experimental, Theoretical, and Device Application of Nanoscale Focused Electron-Beam-Induced Deposition, Ph.D. Dissertation, December (2005).

EBID has recently demonstrated excellent results in the area of photolithographic mask repair. The repairing of the photolithographic masks saves in production down-time of re-writing the mask and consequently saves cost. Clear defect repair of an extreme ultraviolet (EUV) mask is currently being performed using focus ion beam (FIB) techniques.[6] Using focused ions can create problems when ion implantation inherent to FIB mask repair disrupts the highly sensitive optical properties of the transparent region.[6] Liang *et al*. reported utilizing focused electron beam to deposit materials for clear defect mask repair.[7] The use of electron bombardment causes less damage and has a greater spatial resolution for high edge placement precision. Therefore, EBID can be used as a damage-free clear defect repair technique using opaque EBID materials.[8]

Koops *et al*. reported three-dimensional ultra fast vacuum microelectronic and focusing lenses were made utilizing EBID. The lenses allow for electron optical probe forming and imaging systems.[9] Koops *et al*. also reported on the two-dimensional rastering fabrication of leaning nanofibers and a helix using a pattern generator[10], and Utke *et al*. reported the deposition of three-dimensional copper nanostructures made of a vertical fiber deposited on the flanks of a horizontal fiber as shown in Figure 1-2.[11] The horizontal fibers shown in Figure 1-2 were fabricated using the EBID process of a slow linear scan.[11]

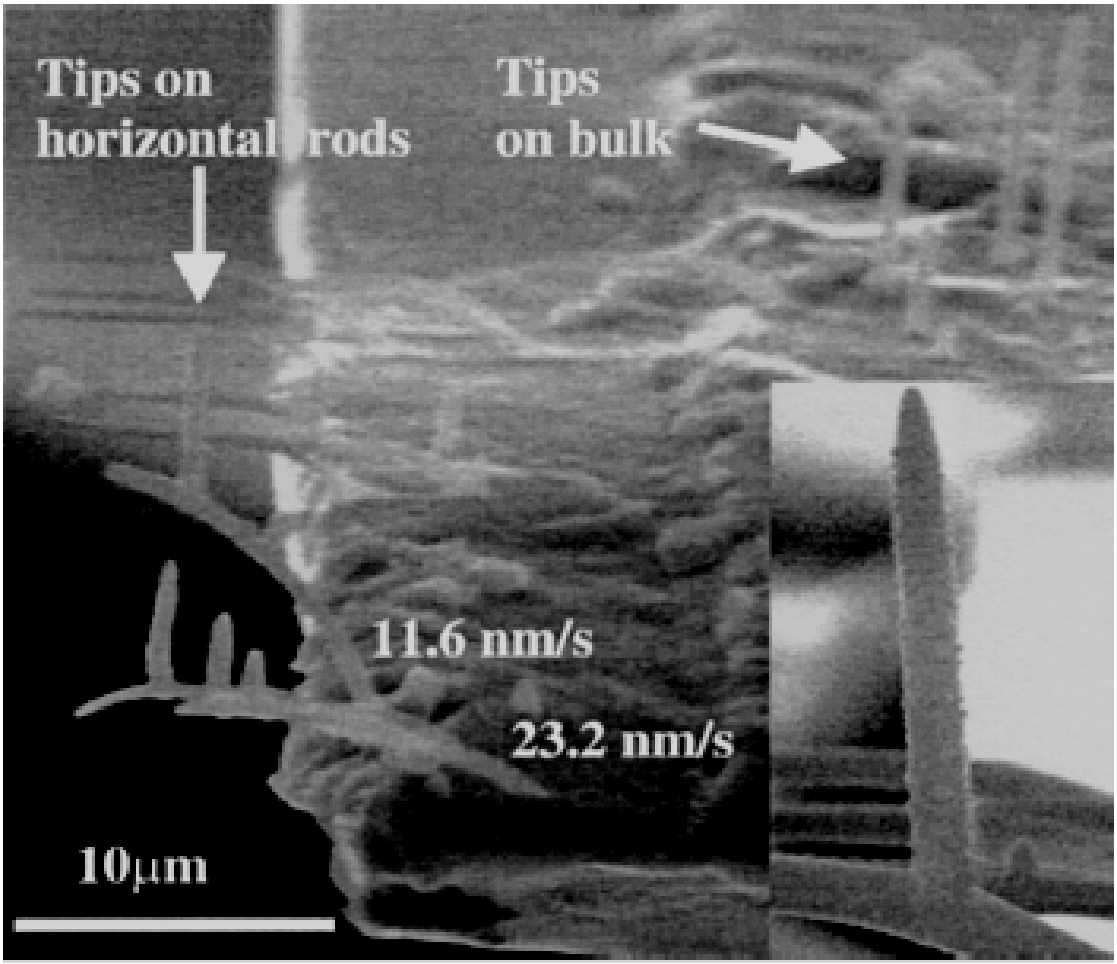

Figure 1-2, The deposition of three-dimensional copper nanostructures made of a vertical fiber deposited on the flanks of a horizontal fiber.

Reused with permission from I. Utke, A. Luisier, P. Hoffmann, D. Laub, and P. A. Buffat, Applied Physics Letters, 81, 3245 (2002). Copyright 2002, American Institute of Physics.

1.2.2 Fundamental Studies of EBID

The previous section illustrated an overview of the experimental applications of EBID. The study of EBID is a growing topic in present nanotechnology that is continually being studied to optimize the process for more improved applications. Therefore, a number of physical and experimental investigations have been performed; some of the ideas and results are discussed in detail in the remainder of this section.

The development of *in-situ* rate monitoring of the EBID technique is critical to understanding some of the fundamentals of EBID. Perentes *et al*. presented a method of monitoring the growth rate and optical properties of transparent EBID depositions by utilizing the combination of a photodiode, a silicon mirror, and a 514-nm wavelength laser.[12] The density and real elements of the refractive indices of SiO_x, TiO_x, and carbon and the deposition thickness were characterized from the reflectivity data collected.[12] Utke *et al.* reported a quantitative method for *in-situ* control of the focused electron beam induced deposition process. A picoamperemeter is used to monitor the electron current flowing through the sample, which reproducibly drops at a characteristic rate to a plateau value during deposition.[13]

In the attempt to institute the EBID technique in nanotechnology, it is necessary to produce smaller, higher-resolution features. The EBID resolution is dependent upon a combination of system variables and physics.[14] Djenizian *et al.* observed that higher beam energies produce smaller electron probe sizes resulting in smaller features.[15] Rack *et al.* also described an effort to increase process control using an energy dispersive x-ray

spectrometer (EDS) connected to a Hitachi S-3500N ESEM.[16] The experiment supplied concurrent, *in-situ* compositional measurements during the process of tungsten EBID.[16]

Increasing the accelerating voltage generates a smaller beam and, in return, produces smaller features. Shimojo *et al.*, Liu *et al.*, and van Dorp *et al.* have reported producing features of tungsten dots that are 3.5 nm and 1nm in diameter utilizing the EBID technique at a high-energy electron beam of 200Kev in a TEM.[17, 18, 3]

1.3 Lithography

First introduced by Alois Senefelder in Bohemia in 1798, lithography was first enabled by writing on a smooth piece of limestone. The Greek word for stone is "lithos" hence the name "lithography". The Alois' process featured water adhering to the gum Arabic surfaces and avoiding the oily parts, while the oily ink used for printing did the opposite.[19] By the middle of the 19th century, a new invention of lithography was chromolithography. This process used a different stone for each color in the process. The modern process of lithography relies on a photographic process. This is typically referred to as Photolithography.

In semiconductor device fabrication, photolithography is used to transfer a pattern design from a reticle (photomask) to a surface on a substrate. Typically, in semiconductor fabrication, the substrate is crystalline silicon formed into a wafer. Other substrate materials could be glass, sapphire and various metals. The basic photolithography procedure includes depositing a thin film layer typically several nanometers to hundreds of nanometers in thickness on the substrate. Then a layer of

photoresist is spun-cast on the top of the thin film layer. The wafer is then exposed to a light source that typically de-magnifies the reticle image and transfers the pattern from the reticle to the substrate. Different resists can be used to allow for different exposing techniques like, ultraviolet radiation, X-Rays and electron beam.

1.3.1 Optical Lithography

The importance of constantly minimizing the critical dimensions (CD) in nanotechnology fabrication applies continual pressure on optical lithography. The Rayleigh's resolution formula,

$$\mathbf{CD} = \kappa_1 \frac{\lambda}{NA}$$

Equation 1-1: Rayleigh's Resolution Formula

where κ_1 is a process factor, λ is the optical wavelength, and NA is the numerical aperture of the lens expresses the diffraction limited resolution of optical lithography. Wavelengths have decreased from 436nm, 365 nm, 248 nm to current processes at 193 nm. Additionally, the numerical aperture has continued to increase from 0.1 to 0.65. Brueck *et al.* has demonstrated that available optical materials will limit the wavelength of an optical system for transmitting around 193 nm or eventually 157 nm.[20] Therefore,

the attention has shifted to reducing κ_1. Brueck et al. presented results of the effects of optical lithography resolution enhancement techniques including optical proximity correction, off-axis illumination, phase-shift masks, and imaging interferometric lithography. Improving these techniques depend on the enhanced frequency-space coverage allowed. Optical proximity correction expands the frequency-space coverage to ~ 1.2-1.3 x NA/λ allowing κ_1's of ~ 0.45.[20] Off-axis illumination configurations demonstrated the maximum spatial frequency is expanded to (2)^(1/2)*NA/λ and allowing κ_1's of ~ 0.43.[20] Pupil plane filters were then added to the system expanding frequencies to 2NA/λ and allowing κ_1's ~ 0.3.[20] In the case of phase shifts at the masks, the importance of the quadratic imaging terms were increased allowing frequencies to2NA/λ allowing κ_1's out to ~ 0.35.[20] Imaging interferometric lithography further expands the frequency coverage out to either (1 + NA)/λ or 3NA/λ based on the details that correspond to the κ_1's of ~ 0.23 – 0.2.[20]

1.3.2 Electron Beam Lithography

Electron beam lithography (EBL) was developed soon after the scanning electron microscope (SEM) was introduced in 1955 [21] and acted as one of the earliest processes used for fabricating integrated circuits dating back to 1957.[22] EBL was used in 1965 to produce sub-100 nm resolution [23] and then optimized in 1976 from improved electron optics.[24] Presently, EBL widely used to produce features in the sub-100 nm regime.[25] The purpose for EBL over standard optical lithography systems is the ability to produce

higher resolution because of the beam of electrons can be focused to create a probe size as little as 1 nm and these electrons do not suffer from optical thin-film interference.[25] The accelerating voltage, the electron scattering, and the resist thickness are important factors that affect the intended application.[26] The resolution of the feature produced from EBL is depicted from the chemical nature of the resist.[26] Golzhauser *et al.* has reported the development of a new resist composed of organic self-assembled mono layers (SAMs) to fabricate features below 10 nm.[27] The resolution of the EBL has been unmatched to any other form of lithography.[28] One major limiting factor of EBL is the inability to mass produce devices because current systems utilize a single electron beam and it is a serial process. Discussed in later sections are the techniques being studied to resolve this problem. Figure 1-3 illustrates the process of EBL.

1.3.3 Future Techniques in Lithography

As optical lithography reaches it limits, it is necessary to explore other possible areas of lithography. Emerging ideas of maskless and immersion lithography are being explored as possible techniques to replace optical lithography.

During the past few decades, the integration of immersion optics and photolithography has not been researched because of the alternative technology techniques. However, with the difficulty of obtaining shorter wavelengths becoming increasingly complex, the immersion assisted lithography has grown to become realistic. The basic idea of immersion lithography is filling the gap between the lens and photoresist as illustrated in Figure 1-4.

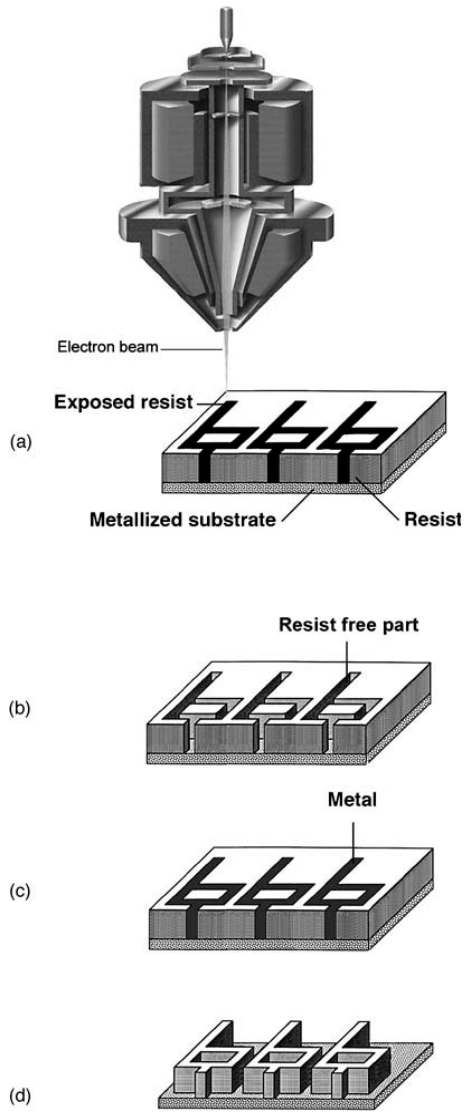

Figure 1-3: Principle of the nanostructuring of surfaces using conventional EBL technique and electroplating, (a) e-beam exposure of a positive resist, (b) removal of the exposed resist, (c) filling of the resist-free locations with metal using electroplating technique, and (d) removal of the unexposed resist leaving high aspect ratio metallic nanostructures at the surface. Reused with the permission from T. Djenizian and P. Schmuki, J. Electroceram 16:9-14, (2006).

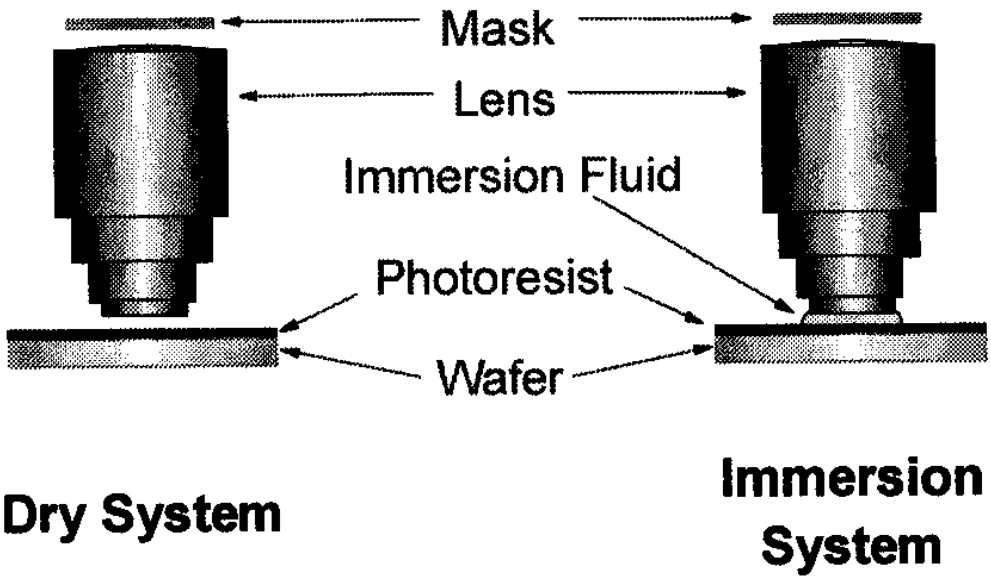

Figure 1-4: Schematic of dry and immersion systems.[17]

Reused with the permission from B.J. Lin, Optical Microlithography XVII, SPIE Vol. 5377, 2004.

Smith *et al.* have demonstrated the development of oblique angle imaging, numerical apertures of 1.44 in water are feasible at a wavelength of 193 nm.[29] This process has led to κ_1's of .25 and half-pith resolution approaching 35 nm.[29] Smith *et al.* has also explored the techniques to improve the refractive index of water through the use of sulfate and phosphate additives.[29] Lin *et al.* presented techniques to 193 nm immersion lithography to 45nm and beyond utilizing a high index immersion fluid, lens material, polarized illumination, mask solid immersion, double exposures, and pitch splitting.[30]

Immersion lithography offers the semiconductor industry a next generation lithography process without requiring a large shift in the system design. However, there are challenges with this process. Shedd *et al.* has studied the effect of residual liquid deposited onto the substrate.[31] The result of this liquid on the substrate leads to defects in the device. An experimental investigation was made to predict the amount of liquid that is deposited by a immersion lithography process.[31] The semi-empirical method supplies the semiconductor industry with important information that reduces defects in nanoelectronic devices.[31]

Baylor *et al.* have presented a conception for maskless digital electrostatically focused electron beam array direct-write lithography (DEAL).[32] The idea encompasses a digitally addressable field-emission array (DAFEA) integrated into a logic and control circuit that is implemented as an integrated circuit.[32] The goal is to suspend a parallel array of integrated circuits on a back plane ~100μm above a 300mm semiconductor wafer.[32] The process could possibly expose a 300 nm semiconductor wafer in less than 45 seconds. The DEAL concept has been modeled and it is suggested that it can be extended to the 10 nm linewidth regime.[32] Figure 1-5 shows a schematic of the proposed DAFEA.

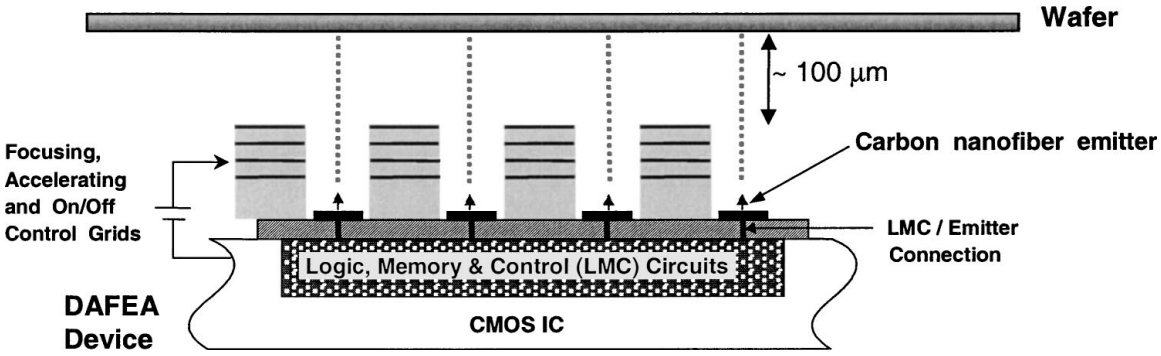

Figure 1-5: Schematic diagram of the proposed DAFEA structure

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1.4 Field Emission

The fabrication of vacuum microelectronic devices employing field emission (FE) cathodes of different types has been a promising area for very high speed electronics, signal amplification, and switching applications. Often referred to as Fowler-Nordhiem field emission is a form of quantum tunneling in which electrons pass through a barrier in the presence of a high electric field. This occurrence is highly dependent on both the properties of the material and the shape of the particular cathode, so that higher aspect ratios produce higher field emission currents. The current density produced by a given electric field is controlled by the Fowler-Nordheim equation

$$J_{field\text{-}emission} = BE^2 \exp\left(- E_c / E \right)$$

Equation 1-2:. Fowler-Nordheim Equation.

These FE devices are applied in a wide range of areas from miniature mass spectrometers and pressure sensors to consumer products such as full color flat-panel displays.[33] The important aspect of a FE device is the electron emitter. These cathodes need to be long-lived, stable, and possess a low threshold voltage for the start of FE.[33]

1.4.1 Field Emission Devices

FE from many different devices has been studied in recent years. Guillorn *et al.* presented the operation of an integrated gated cathode device using a single vertically aligned carbon nanofiber (VACNF) as the field emission source.[34] The device is able to perform under moderate vacuum levels for extensive periods without the degradation in performance.[34] The experiment collected quality field emission characteristics that satisfied the Fowler_Nordheim model of emission.

One-dimensional wide band-gap nanowires have gained much attention because of their excellent physical and chemical properties.[35, 36] Of these nanowires, zinc oxide (ZnO), has demonstrated excellent properties for stable field emission. Huang *et al.* demonstrated that ZnO nanowires had a wide band-gap of 3.37 eV and a large exciton binding energy of 60 meV illustrating considerable significance for practical applications of ultraviolet/blue emission devices, piezoelectric devices, acousto-optical devices, and chemical sensors.[37] Lee *et al.* presented field electron emission from vertically well-aligned ZnO nanowires.[38] The nanowires were grown at a low temperature of 550 ^{o}C by vapor deposition.[38] Turn-on voltage for the ZnO nanowires was around 6.0 V/μm at a current density of 0.1 μA/cm^2.[36] The emission current density of the ZnO nanowires was collected and reached 1 mA/cm^2 at a bias field of 11.0 V/μm.[38] This data represents excellent qualities that would give sufficient brightness as a field emitter in flat panel displays.[38] Figure 1-6 shows a scanning electron microscope (SEM) image of these ZnO nanowires.

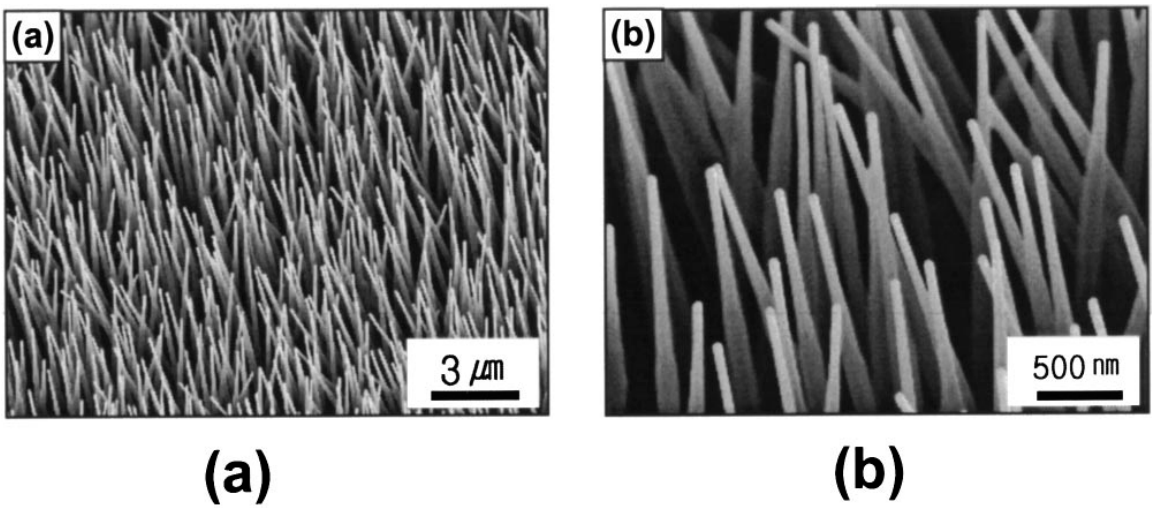


Figure 1-6, (a) SEM micrographs of well-aligned nanowires grown on *n*-type silicon substrate and (b) a magnified SEM image of well-aligned nanowires.
Reused with the permission from C.J. Lee, T.J. Lee, S.C. Lyu, Y. Zhang, H. Ruh, and H.J. Lee, Applied Physics Letters, Volume 81, Number 19, 2002

Yang *et al.* reported the fabrication and operation of integrated field emission cathodes containing single tungsten (W) nanofibers grown by nanoscale EBID.[39] The EBID process incorporated a nonorganometallic precursor, tungsten hexafluoride (WF_6) to deposit the metallic W fibers. The field emission data collected exhibited Fowler-Nordheim behavior. Electrical testing of the device signifies that the EBID direct-write technique is capable for direct production or repair of field emission cathodes.[39] Figure 1-7 illustrates Yang's *et al.* completed device.

EBID has been used to rapidly fabricate field emission device prototypes. Murakami *et al.* fabricated an platinum nanofiber-based field emission device utilizing EBID.[40] EBID was used first to deposit an insulating SiO_2 aperture, then the deposition

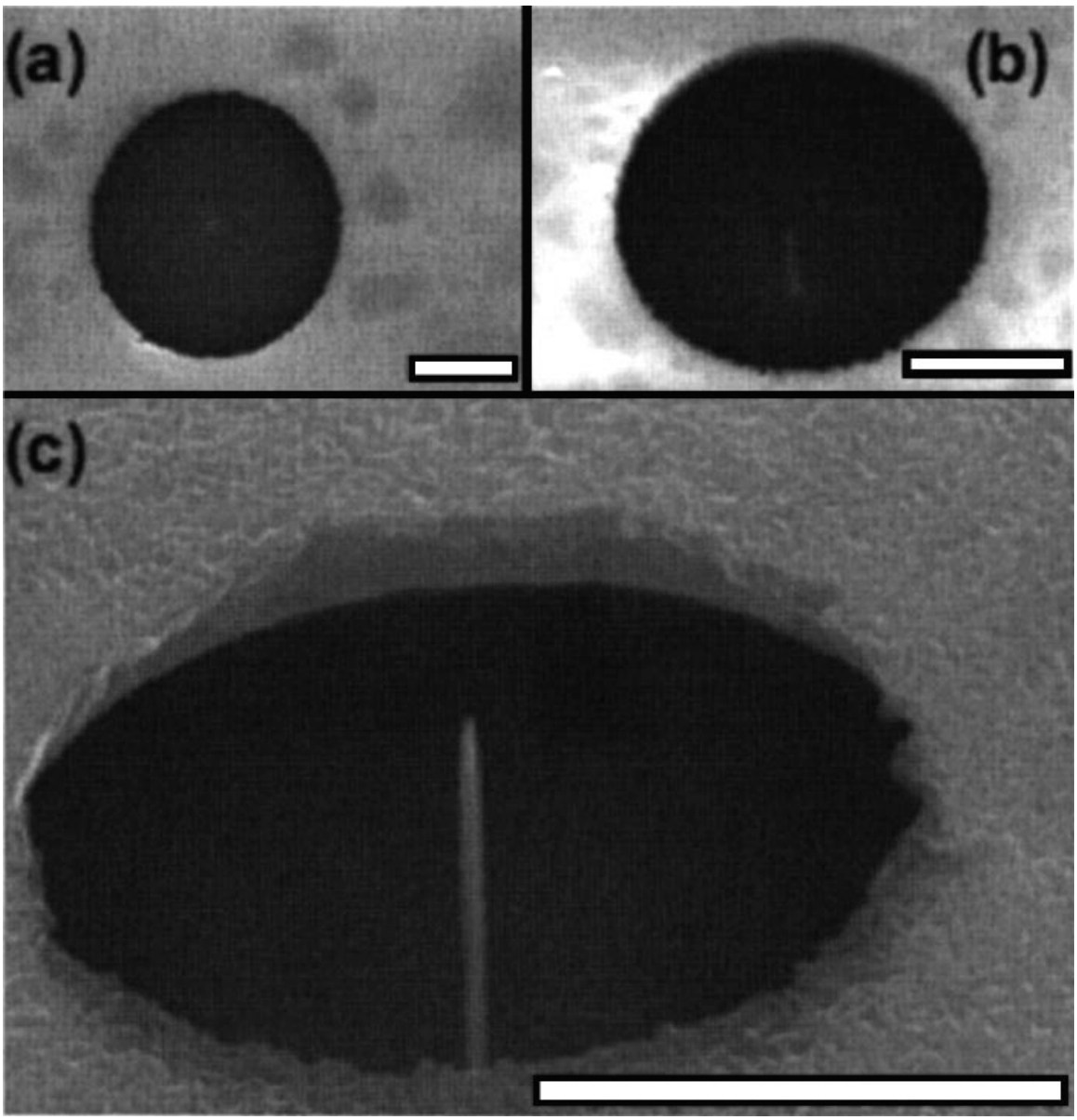


Figure 1-7, SEM micrographs of completed devices. Image (a) as taken at normal beam incidence. Image (b) an oblique angle micrograph taken at 45° incidence angle. Image (c) is a higher magnification SEM of the finished device. All scale bars are 1 µm.

Reused with the permission from X. Yang, M.L. Simpson, S.J. Randolph, P.D. Rack, L.R. Baylor, H. Cui, and W.L. Gardner, Applied Physics Letters 86, 2005

of a platinum gate. The platinum nanofibers emitter was deposited in the aperture and the connection of the gate was made to an electrical lead with a focused electron beam deposited platinum wire. The device exhibited Fowler-Norheim behavior.[40] Lehre *et al.* used EBID to integrate field emission devices with scanning probes for localized electron delivery in scanning probe microscopes. Lehrer *et al.* process showed the replacement of the apex of a basic silicon probe with a flat "mesa".[41]

1.4.2 Field Emission Applications

As described previously, field emission devices have been explored for many decades and have been used in various applications. While an exhaustive review is beyond the scope of this survey, below is a survey of several recent applications.

Bonard *et al.* illustrated the application of cold electron film emitters extended to non-planar geometries by demonstrating a cylindrical field emission source.[42] The cathode consists of a metallic wire with multi-wall carbon nanotubes grown by the catalytic decomposition of acetylene over a Fe catalyst.[42] The emitter demonstrated good field emission characteristics that were used to to realize a luminescent, mercury-free, light source.[42] Li *et al.* reported the use of gate-controlled ZnO nanowires field emission devices for the application of bright electron source for flat panel displays.43 The devices were fabricated using a lift-off fabrication process.[43] Emission characteristics were measured and compared with standard carbon nanotubes (CNT) devices and exhibited better Fowler-Nordheim characteristics.[43] Koops *et al.* demonstrated the deposition and field emission characterization of gold "supertips" having tips of less than

7 nm. All the tips demonstrated field emission starting at an extraction voltage of about 800 V. Some of the tips showed stable emission at an extraction voltage of 210 V. After annealing, the confined emission pattern of the gold "supertip" had an emission angle of ± 7.2.[44] Koops *et al.* also reported that gold and platinum tips demonstrated excellent field emission properties after an emission site forming process, where the emission was localized.[45] As mentioned earlier in this chapter, Yang e*t al.* reported the deposition of tungsten field emission cathodes from a tungsten hexafluoride precursor.[46] The cathodes were deposited into gated apertures intended for use with the Digital Electrostatic Beam Array Lithography (DEAL) devices.[47,48] Sellmair *et al.* demonstrated the use of platinum EBID nanostructures as field emission cathodes for planar micro-triode arrays.[49]

Chapter 2—Experimental Procedure

2.1 DEAL Device Fabrication

The DEAL electron beam lithography system is fabricated by utilizing both standard and non-standard semiconductor nanofabrication techniques. Below describes the detailed process flow that is used to make the device.

Fabrication of the device was achieved on 100mm diameter, device quality silicon wafers [Figure. 2-1(a)]. The wafers were pre-deposited with a 1μm layer of thermal oxide [Figure. 2-1(b)] and 500nm of n-Poly-Si [Figure. 2-1(c)]. The wafer was spun with a Shipley® SPR 955cm positive photoresist [Figure. 2.1(d)]. Alignment marks were then patterned utilizing a GCA 500 Auto stepper [Figure. 2-1(e)] and developed with CD-26. The wafer was then etched using a reactive ion etch process [Figure. 2-1(f)]. The resist was stripped with NMP 1165 resist stripper and the wafer was meticulously rinsed with deionized water and dried with N_2 [Figure. 2-1(g)]. The wafer was re-spun with Shipley® SPR 955cm photoresist [Figre. 2-1(h)] and the gate electrodes were patterned using the same photolithography technique [Fig. 2-1(i)]. The RIE was used to etch the gate pattern through the n-Poly-Si layer down to the thermal oxide layer [Fig. 2-1(j)]. The resist was then stripped with NMP 1165 resist stripper and the wafer was meticulously rinsed with deionized water and dried with N_2 [Fig. 2-1(k)]. The wafer was primed using a HMDS primer and deposited with a 100nm SiO_2 film using a silane-based R.F. Plasma Enhanced Chemical Vapor Deposition (PECVD) process [Fig. 2-1(l)]. The Shipley SPR 955cm positive photoresist was re-spun Fig. 2-1(m)] and the same photolithography technique

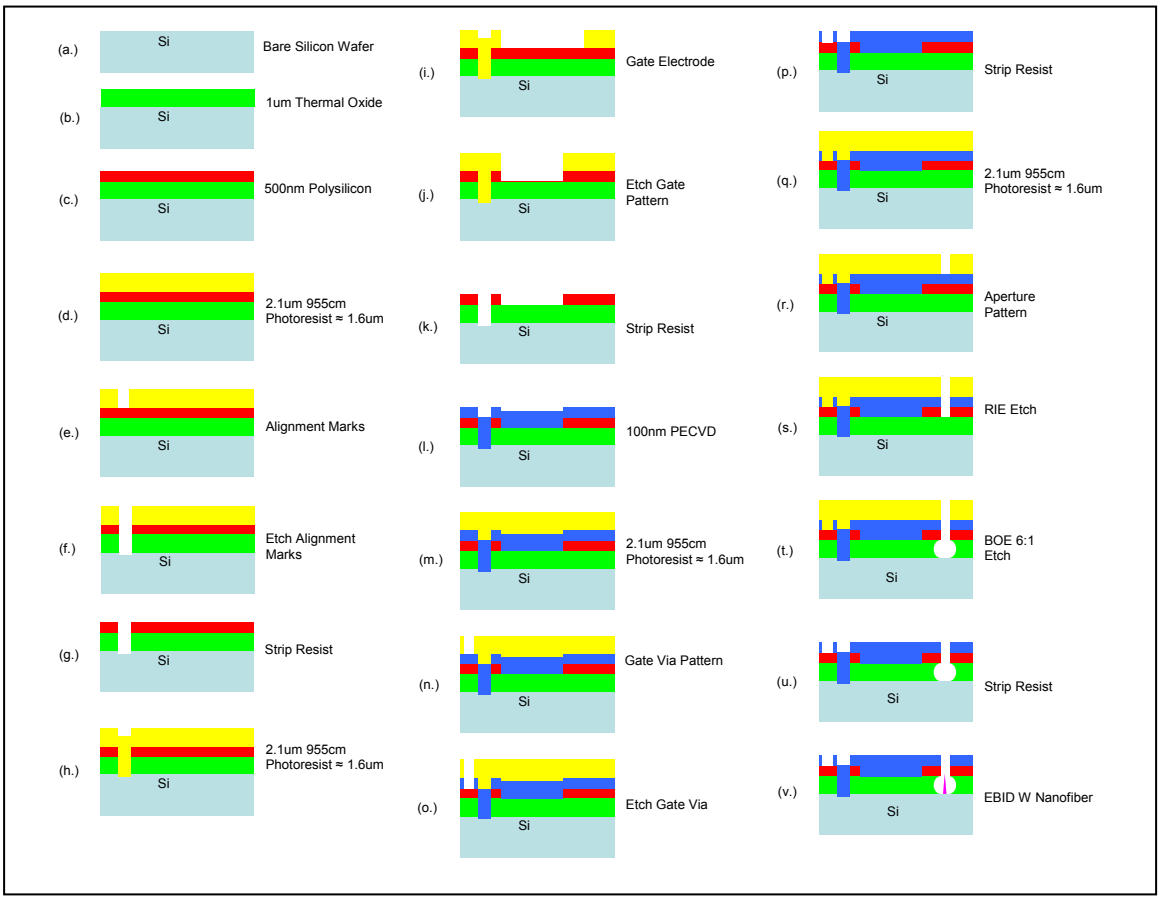


Figure 2-1: Process Flow of the DEAL device.

was used to pattern the gate via electrodes Fig. 2.1(n)]. The structures were then immersed in a hydrofluoric acid (buffered oxide etch (BOE), water: HF=6:1) in order to etch the thermal oxide layer on the back of the polycrystalline silicon Fig. 2-1(o)]. The resist was then stripped with NMP 1165 resist stripper and the wafer was meticulously rinsed with deionized water and dried with N_2 [Fig. 2-1(p)]. The wafer was re-spun with Shipley® SPR 955cm photoresist Fig. 2-1(q)] and the aperture was patterned utilizing the same photolithography technique Fig. 2-1(r)]. The RIE process was executed to etch the apertures to the thermal oxide layer Fig. 2-1(s)]. The structures were then immersed in a hydrofluoric acid (buffered oxide etch (BOE), water: HF = 6:1) in order to produce an isotropic thermal oxide layer back to the silicon layer Fig. 2-1(t)]. The resist was then stripped with NMP 1165 resist stripper and the wafer was thoroughly rinsed with deionized water and dried with N_2 [Fig. 2-1(u)]. EBID was executed to produce tungsten nanofibers approximately 1 μm in height on the bare silicon layer. In Appendix A, are larger views of Figure 2-1.

2.2 Reactive Ion etching

One of the critical factors studied in this thesis is the reactive ion etching (RIE) of the n^+ polycrystalline silicon and silicon oxide layers in the DEAL device.

The driving force behind the advancements in dry etching is the ability to produce devices with smaller dimensions with higher fidelity. Dry etching has developed into an important process in the production of nanostructures, semiconductor devices, and ultra large scale integrated circuits.[50-52] The reactive ion etching (RIE) technique is a

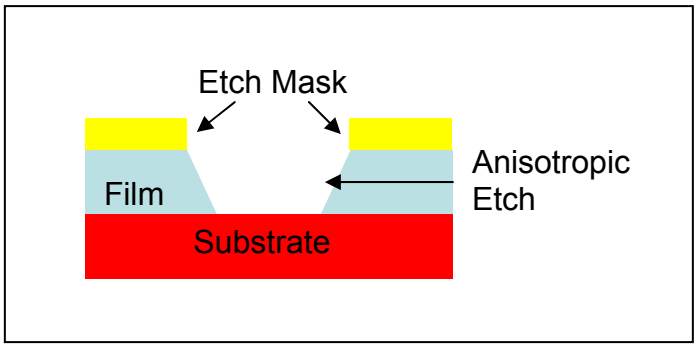


Figure 2-2: Diagram of anisotropic etching.

glow discharge processing technique.[53-55] The advantages of utilizing reactive ion etching for nanofabrication is its ability to have anisotropic and selective etching.[56-58] Anisotropic etching is etching occurs at different rates and in all directions. Selective etching stops on certain crystal planes in the substrate. Figure 2-2 illustrates anisotropic and selective etching.

The process of effectively employing reactive ion etching in integrated circuit manufacturing and nanofabrication requires careful attention to optimize the process parameters of the etcher. This chapter discusses the experimental procedure and process design conditions for the etch optimization of silicon and silicon dioxide (SiO_2) to be used in the digital electron beam array lithography device. The objective for this research was to initially optimize the etch process using readily available single crystal silicon wafers, and then test the optimum condition for a polycrystalline thin film. The second objective was to optimize a silicon oxide thin film insulator etch process. The factors that control the etch rate, selectivity, and profile of single crystal silicon etched with SF_6 and O_2 chemistry is examined. Additionally the factors that control the silicon oxide etch

rate, and selectivity in CHF_3 and CF_4 are described. These experiments were performed to solve device processing issues related to the DEAL device.

2.3 Materials

2.3.1 Silicon Etch DOE

Samples consisted of a photoresist patterned 4 inch diameter bare silicon wafer. Commercially produced 4-in. wafers with 1 μm films of SiO_2 that were grown by thermal oxidation were also used to determine the etch rate of the silicon oxide during the silicon design of experiment (DOE). Both sets of wafers were scribed and broken into quarter pieces to minimize the number of wafers used (Figure 2-3). The specimens of SiO_2 were scribed with a small circle in the middle of the specimen for orientation of the specimen before and after each etching (Figure 2-3g).

2.3.2 Silicon Oxide Etch DOE

Samples of commercially produced thermal oxide (SiO_2) 4 inch wafers were used. The specimens of SiO_2 were scribed with a small circle in the middle of the specimen for orientation of the specimen before and after each etching. Commercially produced n^+ polycrystalline silicon wafers were used to determine the etch rate during the silicon oxide DOE. The n^+ polycrystalline silicon DEAL patterned wafer process is discussed in

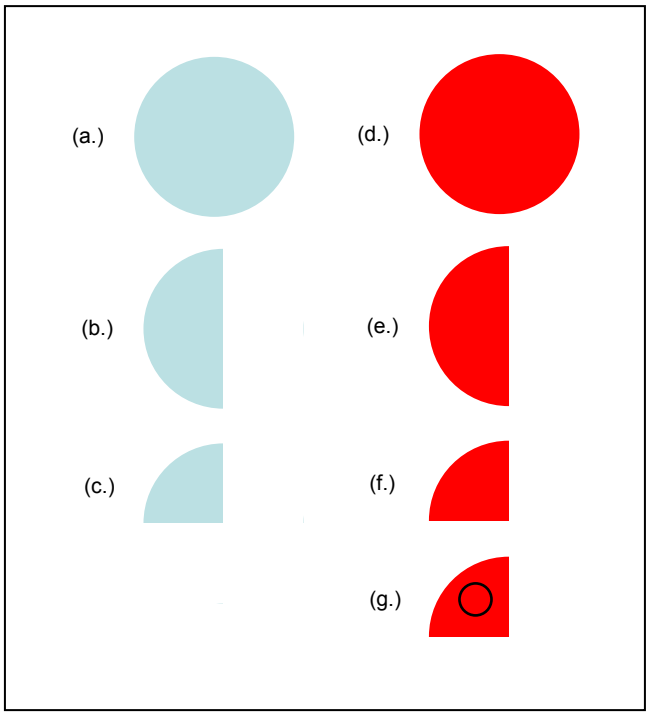


Figure 2-3: Process of preparing the specimens – (a.) 4 inch silicon wafer, (b.) Silicon wafer scribed into half piece, (c.) Silicon wafer scribed into quarter piece, (d.) 4 inch silicon oxide wafer, (e.) Silicon oxide wafer scribed into half piece, (f.) Silicon oxide wafer scribed into quarter piece, (g.) Silicon oxide quarter piece scribed with reference circle.

section 2.1. Both sets of wafers were scribed and broken into quarter specimens as shown in Figure 2-3.

2.3.3 DEAL Gate Pattern

The DEAL device patterning was discussed in detail at the beginning of the chapter (2.1). However, the DEAL gate pattern is described below and shown in Figure 2.4. For the etching study, a bare silicon wafer (2.4a) was patterned with the DEAL gate pattern. The patterning process briefly requires that the wafer be spun using a Reynoldstech® spin coater in two stages (5seconds, 5 step, 250 rpm and 45 seconds, 5 step, 4000 rpm) with Shipley® SPR 955cm positive photoresist (Figure 2.2b). The wafer is soft baked for 90 seconds at 90°C. Next, the wafer is loaded into the GCA Autostep 200 5x reduction step and repeat photolithography system. The command for running the gate pattern is DEAL15B/GATE. The wafer was exposed under a (-) 13 focus offset with an exposure time of 0.8 seconds (Figure 2.4c). A post exposure bake is done for 90 seconds at 120°C. After the bake, the wafer is developed in Microposit® MF CD-26 Developer for 75 seconds with little agitation. The wafer is rinsed with deionized water and dried with compressed nitrogen (N_2).

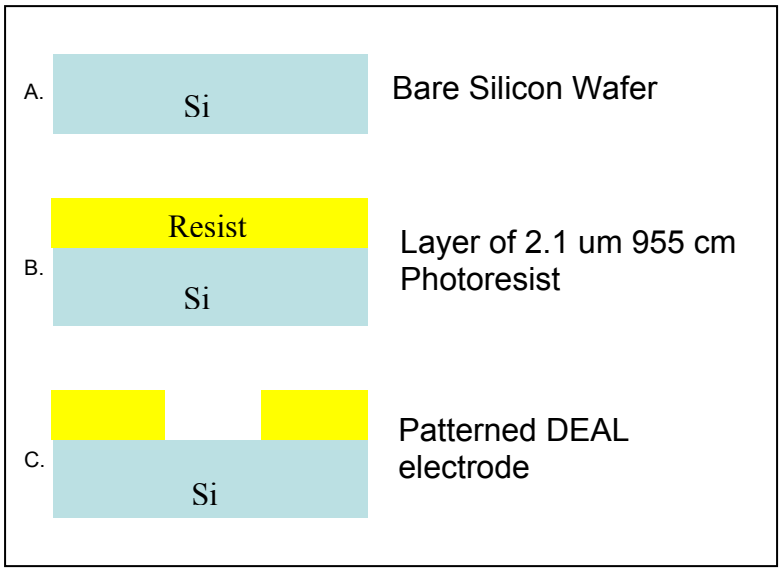


Figure 2-4: Process Flow Diagram of the DEAL gate electrode pattern.

2.4 Equipment

The Trion Technologies Oracle RIE single-wafer etching system was employed for the different optimal etch conditions on the silicon and SiO_2 specimens. The system operates in a conventional planar plasma mode utilizing electrodes that are circular and of equal area (maximum diameter of 8 inches), with the lower electrode composed of anodized aluminum and the upper R.F. - powered electrode formed from anodized aluminum that is coated with silicon. The distinctively designed matching network is built in as an integral part of the bottom electrode assembly to guarantee accurate R.F. tuning, low transmission loss, and virtually no R.F. radiation outside the network itself. The network uses a phase magnitude sensor and amplifiers to provide instantaneous feedback for quick and precise tuning. The system has a 600 watt, 13.56 MHz, solid state

R.F. generator. The computer process controller provides simple and reliable system control over the different recipes. The pressure in the system is controlled by a butterfly pressure control valve operated directly by the process controller in conjunction with a baratron gauge. This provides independent pressure control separate from all other processing parameters. The gas flow rates are precisely controlled with mass flow controllers. The system is evacuated by means of a mechanical pump and then a turbo pump to achieve a low pressure at high gas flow rates. Process gases are introduced into the chamber by a showerhead manifold. An image of the system is shown in Figure 2.5.

Measurements of the wafer specimens were taken using two different tools. The thermal oxide specimens were measured with a Filmeterics F20 Advanced Thin-Film Measurement System. The tool measures thickness and optical constants (n and k). The Filmeterics provides a thickness, refractive index, and extinction coefficient measurements of the spectral analysis of reflectance from the top and bottom of the thin film. Nearly any smooth, translucent, or lightly absorbing film can be measured, including most dielectrics and semiconductors. The quarter wafer specimens of the two types of silicon were each measured before and after each etch using a KLA Tencor Alpha-Step 500 Surface Profilometer measuring tool. Profilometry is another very useful metrology tool commonly used in micro and nanofabrication labs. The tool provides accurate information on the topology of large sample features (>100 nm).

Figure 2-5: Trion Technologies Oracle RIE System.

2.5 Procedure and Design of Experiment

The following paragraphs provide the detailed procedure of the processes used in this design of experiment. Figure 2.6 is a quick reference guide for the steps taken for the DOE's.

2.5.1 Silicon DOE

The experiment started with a programmable design imploring design parameters of gas composition of SF_6 and O_2, pressure, flow rate, and R.F. power. In order to optimize the silicon etch, oxide selectivity, and resist selectivity a JMP desktop statistical discovery software from SAS® was used. The program utilizes a structured, problem-

1. Section the thermal oxide pieces into quarter pieces.
2. Scribe reference circle on each thermal oxide piece.
3. Pattern the desired silicon wafer with the DEAL gate pattern using photolithography techniques.
4. Section the desired silicon wafer into quarter pieces.
5. Use Reflectometer to measure the thickness of the SiO2 quarter specimens before each etch.
6. Use the Profilometer to measure the desired silicon specimens.
7. Put the desired silicon and silicon oxide specimens in the RIE chamber.
8. Run desired process.
9. Unload specimens.
10. Use the Reflectometer to measure the thickness of the SiO_2.
11. Use the Profilometer to measure the silicon + photoresist layer thickness.
12. Strip the silicon piece with ultrasonic acetone bath.
13. Use the Profilometer to measure the silicon thickness silicon.

Figure 2-6: Quick Reference guide for the DOE process.

centered approach for exploring and analyzing data on Windows, Macintosh, or Linux. The intelligent system interface directs users to the right design analysis. JMP automatically displays figures with statistics, enabling users to visualize and uncover data trends. Commercially produced 4 inch wafers of single crystal silicon and films of SiO_2 that were grown by thermal oxidation were used in this DOE. Both sets of wafers were scribed and broken into sixteen different specimens as described in section 2.3.1.

After the programmable design was implemented, it was determined to run sixteen different process conditions. The trials utilized the quarter pieces of bare silicon with the DEAL gate pattern (described in section 2.3.3) and thermal oxide silicon. The quarter pieces of silicon wafers positive photoresist were measured before each etch using the KLA Tencor Alpha-Step 500 Surface Profilometer. The quarter pieces of thermal oxide wafers were measured before each etch utilizing the Filmeterics F20 Advanced Thin-Film Measurement System. Before each etch, an O_2 based clean recipe was performed on the chamber for 2 minutes to remove any contaminates. The pieces were loaded into the Technologies Oracle RIE single-wafer etching system. The different parameters that were implemented are shown in Table 2-1. All the samples were etched for 90 seconds (1.5 minutes).

After each different etch, the specimens were re-measured. The silicon specimen was measured using the KLA Tencor Alpha-Step 500 Surface Profilometer and the silicon oxide specimen with the Filmeterics F20 Advanced Thin-Film Measurement System. The etch rates were calculated using the equations shown in Figure 2-7.

Table 2-1: Process Parameter for Silicon DOE.

Run	RIE Power (W)	Pressure (mTorr)	SF_6 (sccm)	O_2 (sccm)
1	250	238	30	5
2	100	400	30	5
3	250	238	30	5
4	400	75	50	5
5	100	238	50	5
6	100	238	10	5
7	250	75	10	5
8	100	238	10	5
9	400	75	30	5
10	400	238	10	5
11	400	400	50	5
12	250	400	10	5
13	250	238	30	5
14	100	75	30	5
15	400	400	30	5
16	250	238	50	5

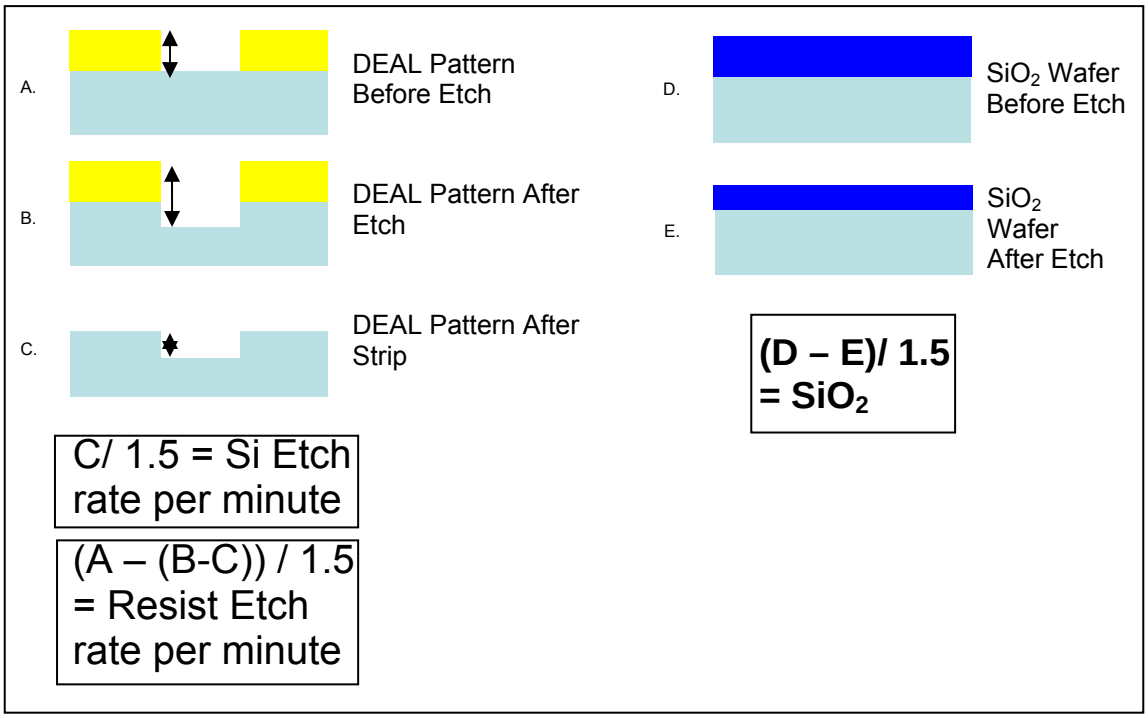


Figure 2-7: Process of Etch Calculations.

After Figure 2-7(b) was measured, the specimen was put in an acetone ultrasonic bath for 5 minutes and then rinsed with deionized water and dried thoroughly with compressed nitrogen. Figure 2-7(c) was measured to determine the silicon etch depth. These steps were performed for all sixteen runs.

The specimens from the sixteen processes were analyzed and imaged using a scanning electron microscope. The imaging was performed at 10 keV and a magnification of 9 kX for all images. Three sets of images (top down, 9 kX, and 35 kX of the side-wall) were taken. For the 9 kX and 35 kX images, the specimens were tilted at an angle 45°. The scanning electron micrographs were used for determining profile angle quality.

2.5.2 Silicon Oxide DOE

The experiment started with a programmable design imploring design parameters of gas composition of CF_4 and CHF_3, pressure, flow rate, and R.F. power. In order to optimize the silicon oxide etch rate, and silicon oxide to n^+ polycrystalline silicon selectivity, and resist selectivity a JMP desktop statistical discovery software from SAS (that was described in section 2.5.1) was also used. Commercially produced 4 inch wafers with films of SiO_2 that were grown by thermal oxidation and commercially produced n^+ polycrystalline silicon were used for this DOE. Both sets of wafers were scribed and broken into nine different specimens as described in section 2.3.2.

After the programmable design was implemented, it was necessary to run nine different processes. The processes utilized the quarter piece wafers of thermal oxide silicon and n^+ polycrystalline silicon with the DEAL gate pattern. The process by which the pieces were fabricated and prepared was discussed in section 2.3.3. The quarter pieces of thermal oxide wafers were measured before each etch process using a Filmeterics F20 Advanced Thin-Film Measurement System. The quarter pieces of n^+ polycrystalline silicon wafers were measured before each etch using the KLA Tencor Alpha-Step 500 Surface Profilometer. Before each run, an O_2 clean recipe was performed on the chamber for 2 minutes to remove any contaminates. Table 2-2 shows the nine processes that were performed in the DOE.

Table 2-2: Silicon Oxide Experimental Factors.

Experimental Constants							
CHF3=50 sccm							
ICP Power = 0 W							
Etch Time = 90 seconds							
	Variable Factors			Constant Factors			
Run	RIE Power (W)	Pressure (mTorr)	CF4 (sccm)	CHF3 (sccm)	Etch Time (sec)	ICP Power	CF4/ CHF3
1	300	70	17	50	90	0	0.333
2	300	70	67	50	90	0	1.33
3	200	30	67	50	90	0	1.33
4	300	30	17	50	90	0	0.333
5	300	30	67	50	90	0	1.33
6	250	50	42	50	90	0	0.832
7	200	70	67	50	90	0	0.333
8	200	70	67	50	90	0	1.33
9	200	30	17	50	90	0	0.333

After each different etch, the specimens were re-measured. The silicon oxide specimen was measured with the Filmeterics F20 Advanced Thin-Film Measurement System and the n^+ polycrystalline silicon specimen was measured using the KLA Tencor Alpha-Step 500 Surface Profilometer. The etch rates were calculated using the equations shown in Figure 2-8.

After Figure 2.8(b) was measured, the specimen was put in an acetone ultrasonic bath for 5 minutes and then rinsed with deionized water and dried thoroughly with compressed nitrogen. Figure 2.8(c) was measured to determine the silicon etch depth. These steps were performed for all nine runs.

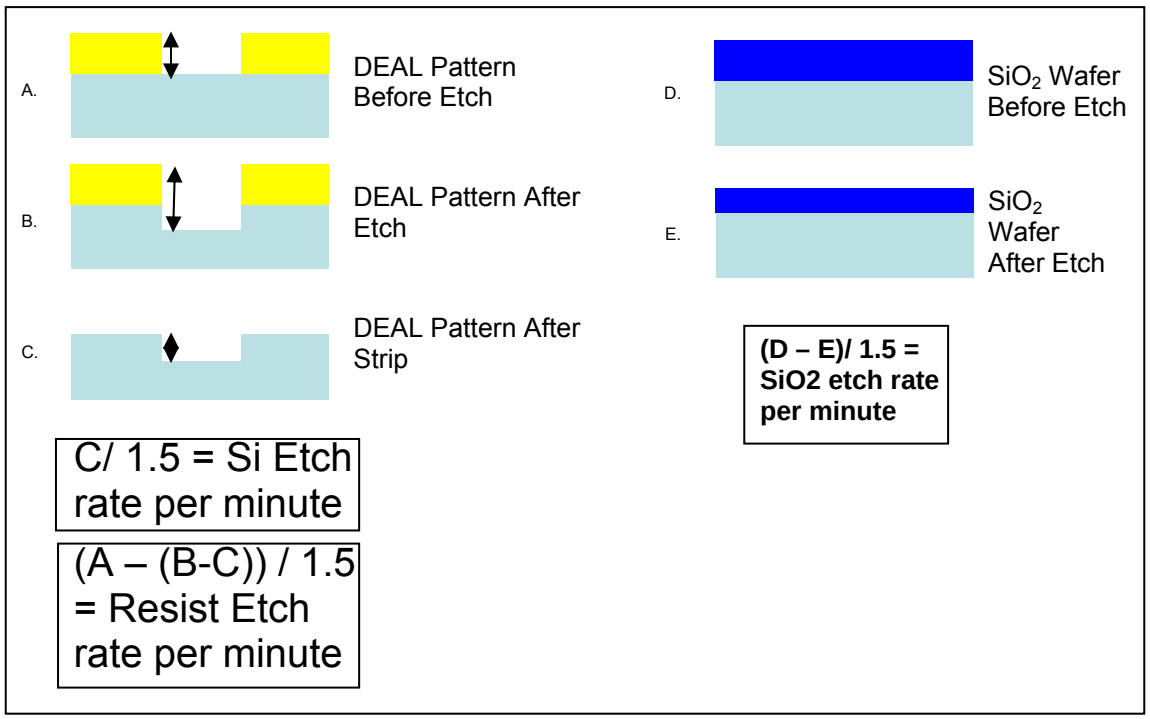


Figure 2-8: Process Flow of Etch Calculations.

2.5.3 DEAL Experimental

Introduction

The characterization of the tungsten nanofibers for the DEAL device was performed as described below. The growth of the fibers for field emission was achieved utilizing an EBID system shown in Figure 2-9. The system is a Hitachi S-4300SE/N variable pressure scanning electron microscope (VPSEM) that employs a Schottky emission electron gun. These system variables are discussed in detail below. In order to test these fibers, a DEAL device is fabricated. The DEAL device fabrication process is described later in this section.

The Vacuum System

The EBID vacuum system integrates three roughing pumps, three ion pumps, and two turbo-molecular pumps. The Schottky emitter gun is under ultra-high vacuum and is separate from the specimen chamber by several intermediate chambers. Ion pumps back the intermediate chambers, and one of the turbo-molecular pumps back the ion pumps which is also backed by a roughing pump. The bottom intermediate chamber is maintained by the turbo-molecular pump. This chamber is directly connected to the

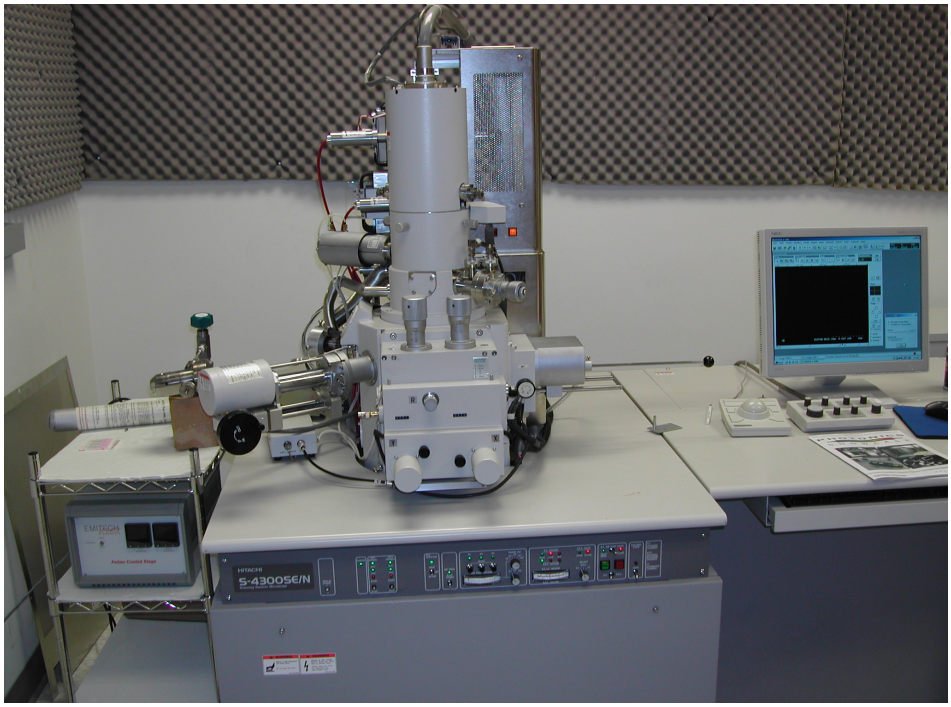


Figure 2-9: The EBID system. It is modified from a Hitachi S-4300SE/N variable pressure scanning electron microscope (VPSEM) equipped with a Schottky field emission electron gun.[59]

specimen chamber through a differential aperture that permits the passing of electrons simultaneously keeping the electron gun from contamination. The second turbo-molecular pump is attached to the the specimen chamber and is backed by a rough pump. The third rough pump is also connected to the main chamber and is used to maintain the vacuum in the so-called variable pressure operation mode of the SEM.

The Electron Optics System

The EBID system uses a Schottky emission electron gun because of its stable emission current. The Schottky electron gun has a cathode, suppressor electrode, and first and second anodes. The electron beam uses a raster motion to scan across the specimen. The EBID system allows the beam to be rastered at different speeds. The EBID system is capable of producing three scan modes: line, spot and box mode. The spot mode is used for the deposition of the tungsten nanofibers.

The Temperature-Controlling System

The EBID temperature of the original specimen stage is controlled by an Emitech K25X Peltier cooling stage, which is shown in Figure 2-10. The cooling stage is connected to the specimen chamber wall through a port which is connected to an external control unit and water chiller. The cooling stage has a temperature range that varies from -30 to 75 ^{o}C and is monitored via an electrical lead.

Figure 2-10: The Emitech K25X Peltier cooling stage installed on the EBID system.[59]

The Gas Delivery System

Figure 2-11 shows the gas delivery system. The system consists of a bottle of the precursor gas, a leak valve, and a wobble stick. The precursor gas that was chosen for the deposition of the fibers was tungsten hexafluoride (WF_6). WF_6 was chosen for this work because of it being an ideal gas for EBID mask repair. The gas flow was controlled by the leak valve. The wobble stick allowed for the delivery of the gas to a localized position via a hypodermic needle at the end of the stick. The wobble stick also is capable of changing the distance and angle of the needle.

The Imaging and Analysis System

The imaging system integrates a secondary electron (SE), back scattered electron (BSE), environmental secondary electron (ESE), and an energy dispersive X-Ray spectrometry) (EDS) detectors for the in-situ analysis of the specimen.

DEAL Tungsten Nanofiber Characterization DOE

Characterization of the EBID W nanofibers was performed. A DOE was implemented utilizing the EBID system discussed in this section to initially correlate the structure of the resultant tungsten nanofibers to their processing parameters. Subsequently, the goal was to correlate the electrical properties of the W nanofibers to

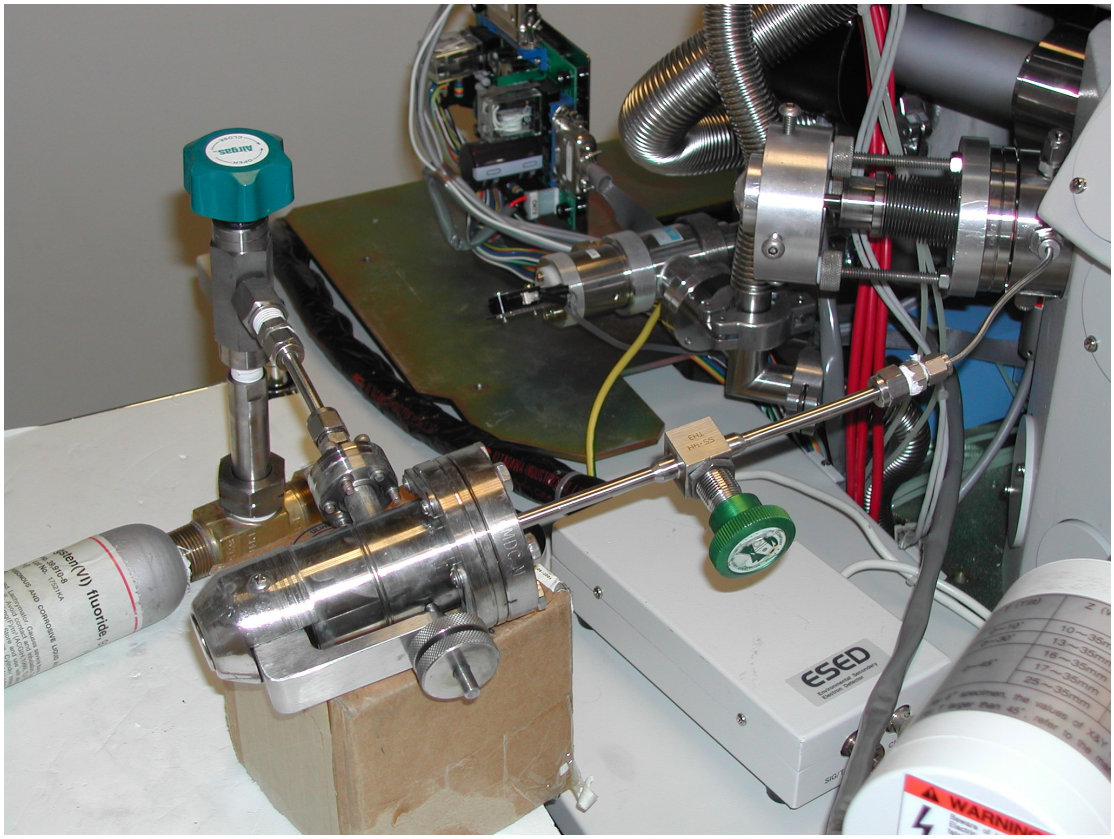


Figure 2-11: The gas delivery system consists of (a) a reservoir, (b) a leak valve and (c) a wobble stick with a hypodermic needle on the end.[59]

their structure. The nanofibers were grown in DEAL devices utilizing the EBID system and WF_6 as a precursor gas. The variable conditions were chamber pressure (controlled by the flow of the gas), electron beam energy, and specimen beam current. Deposiiton time was constant at 30 seconds. The DOE was designed for nine different growth parameters. After the deposition of the nanofibers, the specimen was tilted 30° to measure the height, length, width, and tip angle of the fibers. These measurements were made using Microsoft® PowerPoint software. Table 2-3 shows the nine different deposition parameters of the DOE.

Table 2-3: Process parameters of the EBID DOE.

Run	Pressure $x10^{-3}$	Current (pA)	Energy
1	4	25	5
2	4	75	15
3	4	125	25
4	6	25	15
5	6	75	25
6	6	125	5
7	8	25	25
8	8	75	5
9	8	125	15

Chapter 3—Results

3.1 Silicon DOE

The JMP desktop statistical discovery software from SAS® design of experiments (DOE) was performed to investigate the effects that power, pressure, and SF_6/O_2 gas mixtures have on the etch rate of silicon, the etch selectivity of Si to SiO_2 and Si to photoresist, and the sidewall angle of the resultant silicon etch. The results of this silicon DOE are presented below. The tables and figures will be discussed in chapter 4.

Figure 3-1 shows scanning electron micrographs of the profiles of the etched silicon for each of the specific etch conditions. Of particular interest, was the etch taper angle of the etched silicon.

Table 3-1 shows the characterization of the scanning electron micrographs. The images were visually categorized with either a poor, good, or excellent label. These results were used to compose the prediction profiles shown in a later figure.

Figure 3.2 are silicon etch rate contour plots of R.F. power (x-axis), total gas pressure (y-axis), etch rate (z-axis or shaded contour) for three different SF_6/O_2 gas ratios.

Figure 3-3 are silicon to silicon oxide selectivity response contour plots of R.F. power (x-axis), total gas pressure (y-axis), Si to SiO_2 selectivity rate (z-axis or shaded contour) for three different SF_6/O_2 gas ratios.

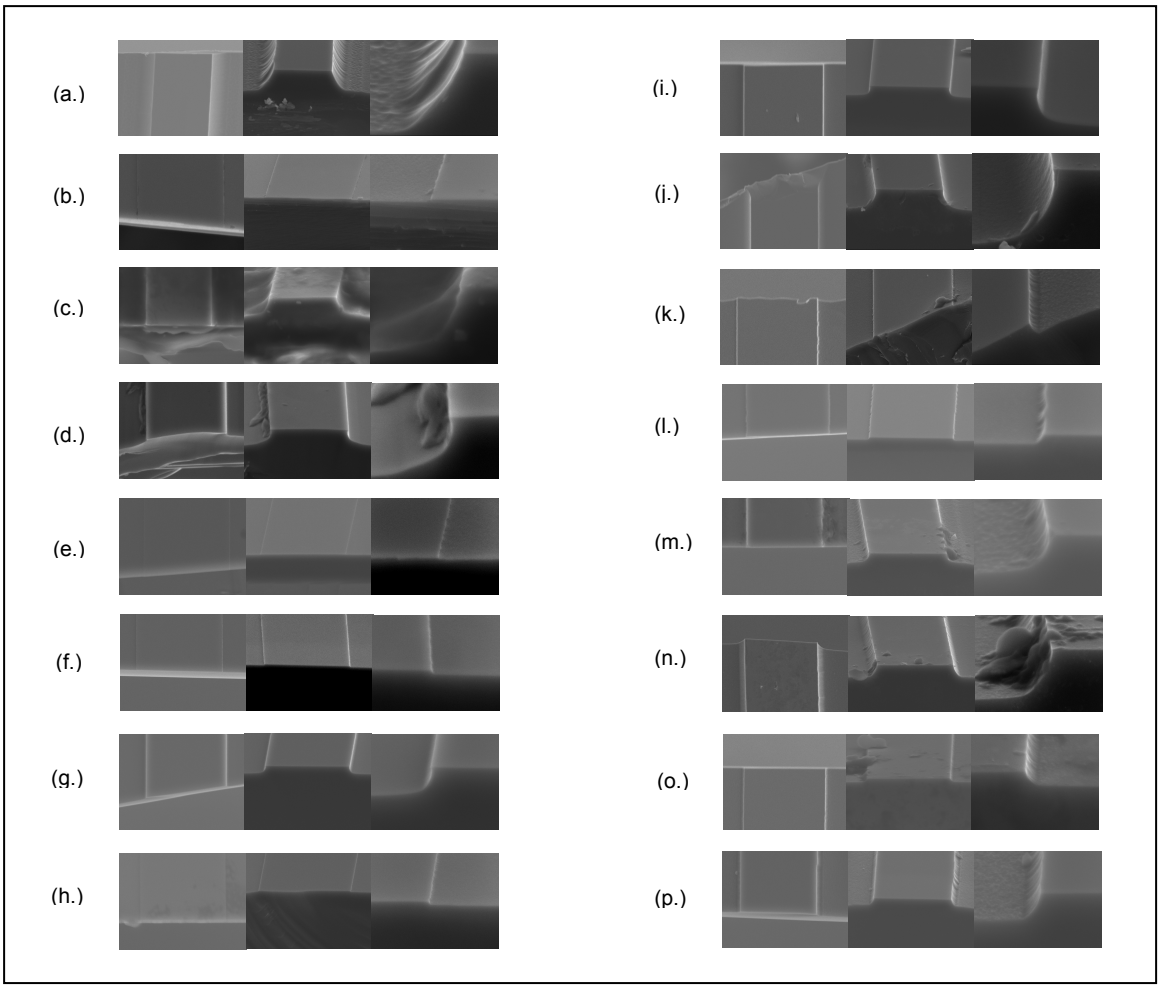
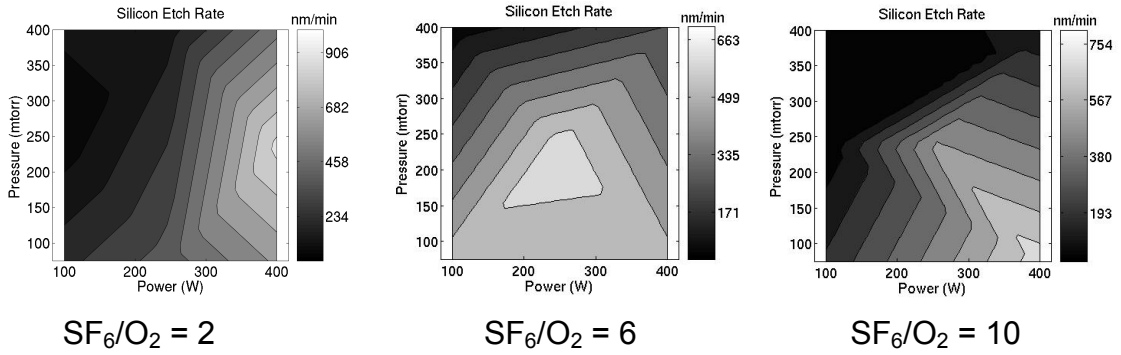


Figure 3-1: SEM images of silicon DOE etch process Power (W), Pressure (mTorr), and SF_6/O2 (sccm) – (a.) 250, 238, 6 (b.) 100, 400, 6 (c.) 250, 238, 6 (d.) 400,75, 10 (e.) 100, 238, 10 (f.) 100, 138, 2 (g.) 250, 75, 2 (h.) 100, 238, 2 (i.) 400, 75, 6 (j.) 400, 238, 2 (k.) 400, 400, 10 (l.) 250, 400, 2 (m.) 250, 238, 6 (n.) 100, 75, 6 (o.) 400, 400, 6 (p.) 250, 238, 10.

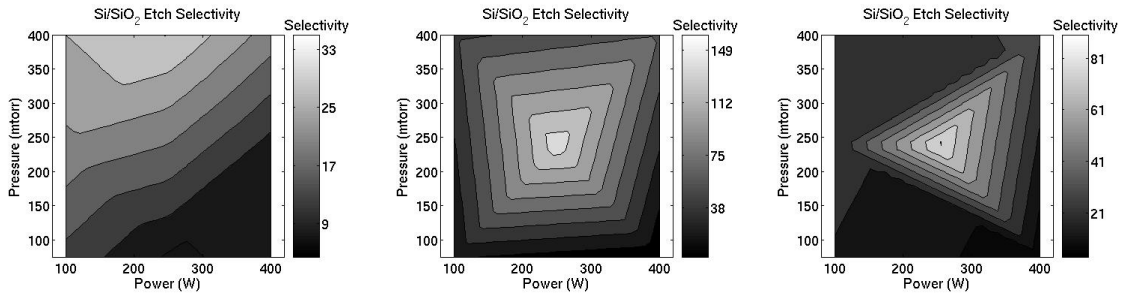
Table 3-1: Characterization table of the images in Figure 3-1.

Profile Angle				
Run	Image	Poor	Good	Excellent
1	a			
2	b			
3	c			
4	d			
5	e			
6	f			
7	g			
8	h			
9	i			
10	j			
11	k			
12	l			
13	m			
14	n			
15	o			
16	p			



$SF_6/O_2 = 2$ $SF_6/O_2 = 6$ $SF_6/O_2 = 10$

Figure 3-2: Silicon Etch Rate Response Contours.



$SF_6/O_2 = 2$ $SF_6/O_2 = 6$ $SF_6/O_2 = 10$

Figure 3-3: Si to SiO_2 Selectivity Response Contours.

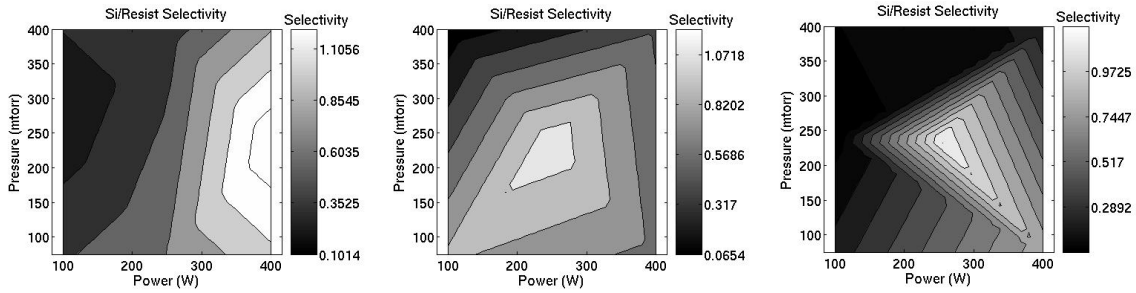
Figure 3-4 are silicon to resist selectivity response contour plots of R.F. power (x-axis), total gas pressure (y-axis), Si to photoresist etch selectivity rate (z-axis or shaded contour) for three different SF_6/O_2 gas ratios.

Figure 3-5 are the prediction profiles from the results of the silicon DOE. Along the y-axis are the silicon etch rate, oxide selectivity, profile angle quality, and photoresist selectivity. Along the x-axis, are the R.F. power, pressure, and SF_6/O_2 ratios. The red values indicate the predicted responses for the optimized factor settings. The blue values indicate the deviation in the predicted response for the optimized factor settings.

Table 3-2 represents the data collected from the sixteen processes in the silicon DOE. Variable factors were RIE power (W), pressure (mTorr), and SF_6 (sccm) gas. Constant factors were O_2 (sccm) gas, etch time (seconds), and inductively coupled plasma (ICP) power. The measurements were taken of the photoresist pre-etch (nm), resist post etch (nm), oxide etch depth (nm), silicon etch depth (nm), SF_6 %, O_2 %, and Flourine/Carbon ratio. The calculations were the silicon etch rate (nm/min), oxide etch rate (nm/min), photoresist etch rate (nm/min), photoresist selectivity, and oxide selectivity.

Table 3-3 shows the optimized process. Run 1 was performed on single crystal silicon. Run 2 was performed on n^+ polycrystalline silicon. The different parameters listed are described as those used in Table 3-2.

Figure 3-6 shows a scanning electron micrograph of the optimized process condition of the silicon etch DOE. The image is of the single crystal silicon etch.



$SF_6/O_2 = 2$ $SF_6/O_2 = 6$ $SF_6/O_2 = 10$

Figure 3-4: Silicon to Photoresist Selectivity Response Contours.

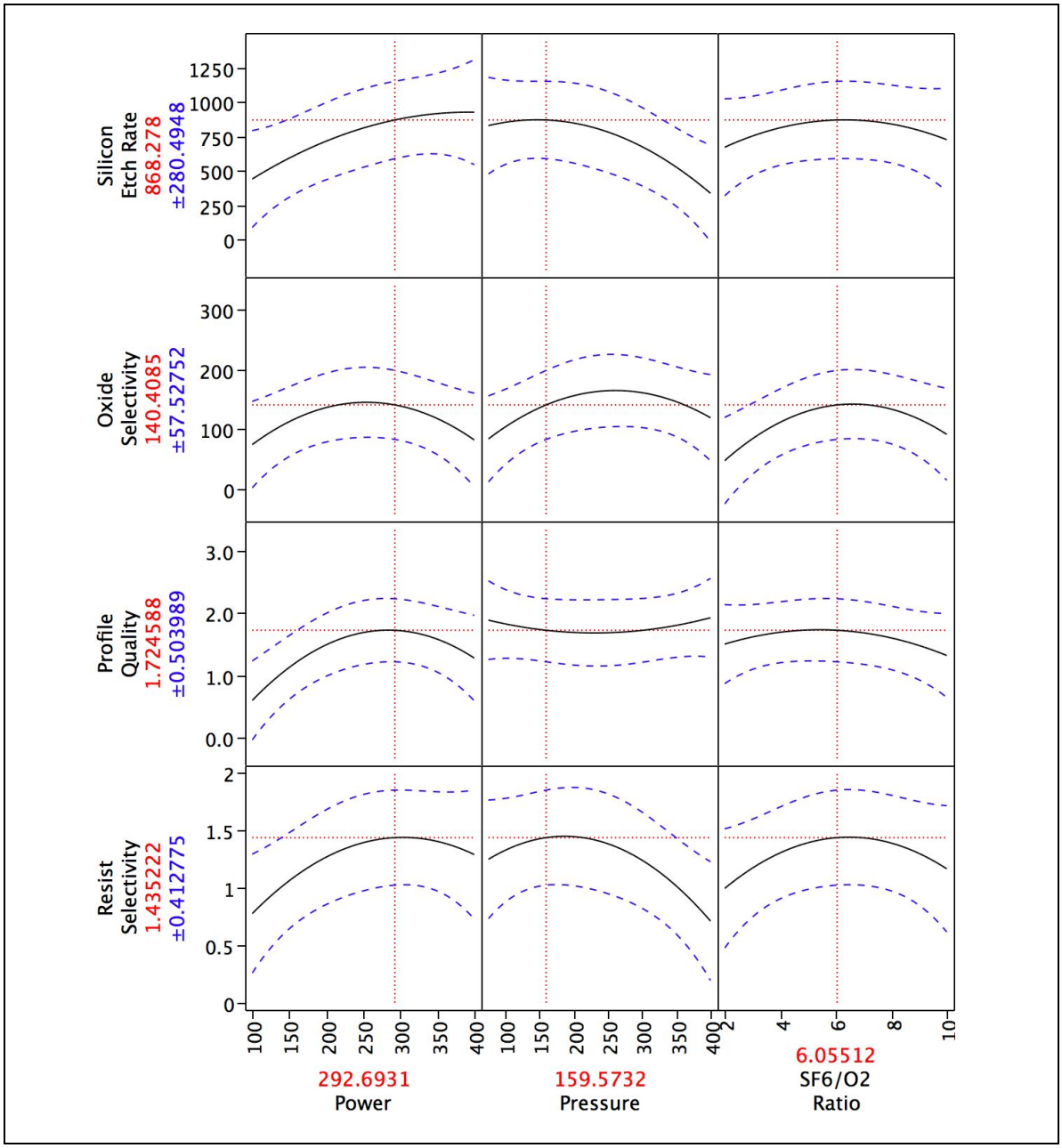


Figure 3-5: Prediction Profiles.

Table 3-2: Data from Si DOE.

	Variable Factors			Constant Factors				Measurements						
Run	RIE Power (W)	Pressure (mTorr)	SF_6 (sccm)	O_2 (sccm)	Etch Time	ICP Power	SF_6/O_2	Resist pre-etch (nm)	Resist post-etch (nm)	Oxide etch depth (nm)	Si etch depth (nm)	$\%SF_6$	$O_2\%$	F/C
1	250	238	30	5	90	0	6	1680	2710	7	1020	0.14	0.86	3.71
2	100	400	30	5	90	0	6	1641	1680	1	54.7	0.14	0.86	3.71
3	250	238	30	5	90	0	6	1730	2960	9	1220	0.14	0.86	3.71
4	400	75	50	5	90	0	10	1678	2210	312	1303	0.09	0.91	3.82
5	100	238	50	5	90	0	10	1523	1550	2	47	0.09	0.91	3.82
6	100	238	10	5	90	0	2	1452	1530	2	88	0.33	0.67	3.33
7	250	75	10	5	90	0	2	1570	1900	155	681	0.33	0.67	3.33
8	100	238	10	5	90	0	2	1518	1560	16	59	0.33	0.67	3.33
9	400	75	30	5	90	0	6	1680	2190	278	947	0.14	0.86	3.71
10	400	238	10	5	90	0	2	1593	2810	190	1554	0.33	0.67	3.33
11	400	400	50	5	90	0	10	1554	1780	6	237	0.09	0.91	3.82
12	250	400	10	5	90	0	2	1550	1730	7	247	0.33	0.67	3.33
13	250	238	30	5	90	0	6	1710	2860	9	1150	0.14	0.86	3.71
14	100	75	30	5	90	0	6	1740	2760	44	1111	0.14	0.86	3.71
15	400	400	30	5	90	0	6	1571	2060	5	497	0.14	0.86	3.71
16	250	238	50	5	90	0	10	1492	2400	10	925	0.09	0.91	3.82

Table 3-2: Continued.

	Variable Factors			Constant Factors				Calculations				
Run	RIE Power (W)	Pressure (mTorr)	SF_6 (sccm)	O_2 (sccm)	Etch Time (sec)	ICP Power	SF_6/O_2	Si Rate (nm/min)	Oxide rate nm/min	Reist rate nm/min	Resist Selectivity	Oxide Selecivity
1	250	238	30	5	90	0	6	680.00	4.67	553.33	1.23	145.71
2	100	400	30	5	90	0	6	36.47	0.67	557.47	0.07	54.70
3	250	238	30	5	90	0	6	813.33	6.00	570.00	1.43	135.56
4	400	75	50	5	90	0	10	868.67	208.00	1073.33	0.81	4.18
5	100	238	50	5	90	0	10	31.33	1.33	521.00	0.06	23.50
6	100	238	10	5	90	0	2	58.67	1.33	490.67	0.12	44.00
7	250	75	10	5	90	0	2	454.00	103.33	757.33	0.60	4.39
8	100	238	10	5	90	0	2	39.33	10.67	517.33	0.08	3.69
9	400	75	30	5	90	0	6	631.33	185.33	851.33	0.74	3.41
10	400	238	10	5	90	0	2	1036.00	126.67	755.67	1.37	8.18
11	400	400	50	5	90	0	10	158.00	4.00	525.33	0.30	39.50
12	250	400	10	5	90	0	2	164.67	4.67	561.33	0.29	35.29
13	250	238	30	5	90	0	6	766.67	6.00	570.00	1.35	127.78
14	100	75	30	5	90	0	6	740.67	29.33	640.67	1.16	25.25
15	400	400	30	5	90	0	6	331.33	3.33	529.00	0.63	99.40
16	250	238	50	5	90	0	10	616.67	6.67	508.67	1.21	92.50

Table 3-3: Optimum Data of Si DOE.

	Variable Factors			Constant Factors				Measurements						
Run	RIE Power (W)	Pressure (mTorr)	SF_6 (sccm)	O_2 (sccm)	Etch Time	ICP Power	SF_6/O_2	Resist pre-etch (nm)	Resist post-etch (nm)	Oxide etch depth (nm)	Si etch depth (nm)	$\%SF_6$	$O_2\%$	F/C
1	294	160	30	5	90	0	6	1710	3320	152	1888	0.14	0.86	3.71
2	294	160	30	5	30	0	6	1500	1907	152	500	0.14	0.86	3.71
	Variable Factors			Constant Factors				Calculations						
Run	RIE Power (W)	Pressure (mTorr)	SF_6 (sccm)	O_2 (sccm)	Etch Time (sec)	ICP Power	SF_6/O_2	Si Rate (nm/min)	Oxide rate (nm/min)	Reist rate (nm/min)	Resist Selectivity	Oxide Selecivity		
1	294	160	30	5	90	0	6	1258.67	101.33	185.33	6.79	12.42		
2	294	160	30	5	30	0	6	1000.00	101.33	186.00	5.38	9.87		

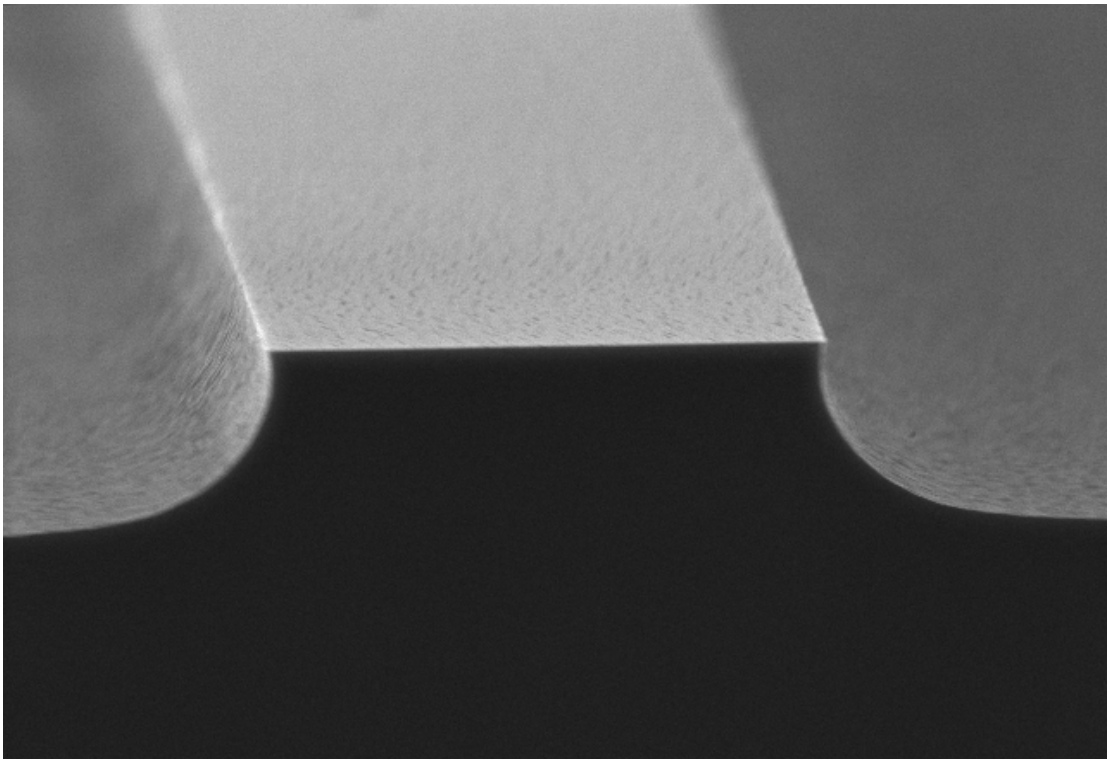


Figure 3-6: Scanning electron micrograph of the optimized process.

3.2 Silicon Oxide DOE

Table 3-4 represents the data collected from the silicon oxide DOE. The variable factors are highlighted in yellow, constant factors in blue, and the measurements and calculations in green. The process details of the experiments were discussed in chapter 2 and the interpretation of the results are discussed in chapter 4.

Figure 3-7 are the prediction profiles from the silicon oxide etch DOE. Along the y-axis are the two responses – silicon oxide etch rate and resist selectivity, and the desirability associated with each response. Along the x-axis, are the three experimental variables: R.F. power, pressure, and SF_6/O_2 ratios. The red values indicate the predicted responses for the optimized factor settings. The blue values indicate the deviation in the predicted response for the optimized factor settings.

Table 3-5 represents the data collected from the optimum silicon oxide DOE condition. The different parameters listed are described as those used in Table 3-5.

3.3 Tungsten (W) Nanofiber DOE

Table 3-6 Represents the data collected from the W nanofiber characterization DOE. The measured data were the fiber height, fiber width, tip width, and tip angle.

Figures 3-8 – 3-16 are scanning electron micrographs of the nine different W nanofibers grown in the DOE. The deposition parameters are listed below each image. Figure 3-8 (run #1) is the only figure grown for 60 seconds, all the other fibers were grown for 30 seconds.

Table 3-4: Experimental Data of the Silicon Oxide DOE.

	Variable Factors			Constant Factors				Measurements						
Run	RIE Power	Pressure	CF_4 sccm	CHF_3 sccm	Etch Time	ICP Power	CF_4/CHF_3	Resist pre-etch	Resist post-etch	Oxide etch depth	polySi etch depth	$\%CHF_3$	$\%CF_4$	F/C
1	300	70	17	50	90	0	0.34	1550	1520	98	0	0.746269	0.25373	2.51
2	300	70	67	50	90	0	1.34	1510	1440	176	5	0.42735	0.57265	3.15
3	200	30	67	50	90	0	1.34	1600	1570	112	5	0.42735	0.57265	3.15
4	300	30	17	50	90	0	0.34	1510	1480	130	0	0.746269	0.25373	2.51
5	300	30	67	50	90	0	1.34	1510	1450	168	10	0.42735	0.57265	3.15
6	250	50	42	50	90	0	0.84	1570	1540	167	10	0.543478	0.45652	2.91
7	200	70	17	50	90	0	0.34	1450	1460	72	0	0.746269	0.25373	2.51
8	200	70	67	50	90	0	1.34	1450	1530	111	0	0.42735	0.57265	3.15
9	200	30	17	50	90	0	0.34	1490	1460	76	0	0.746269	0.25373	2.51

	Variable Factors			Constant Factors				Calculations				
Run	RIE Power	Pressure	CF_4 sccm	CHF_3 sccm	Etch Time	ICP Power	CF_4/CHF_3	Oxide Rate	polySilicon rate	reist rate	Resist Selectivity	poly selecivity
1	300	70	17	50	90	0	0.34	65.33	0.00	20.00	3.27	0.00
2	300	70	67	50	90	0	1.34	117.33	3.33	50.00	2.35	35.20
3	200	30	67	50	90	0	1.34	74.67	3.33	23.33	3.20	22.40
4	300	30	17	50	90	0	0.34	86.67	0.00	20.00	4.33	0.00
5	300	30	67	50	90	0	1.34	112.00	6.67	46.67	2.40	16.80
6	250	50	42	50	90	0	0.84	111.33	6.67	26.67	4.18	16.70
7	200	70	17	50	90	0	0.34	48.00	0.00	-6.67	-7.20	0.00
8	200	70	67	50	90	0	1.34	74.00	0.00	-53.33	-1.39	0.00
9	200	30	17	50	90	0	0.34	50.67	0.00	20.00	2.53	0.00

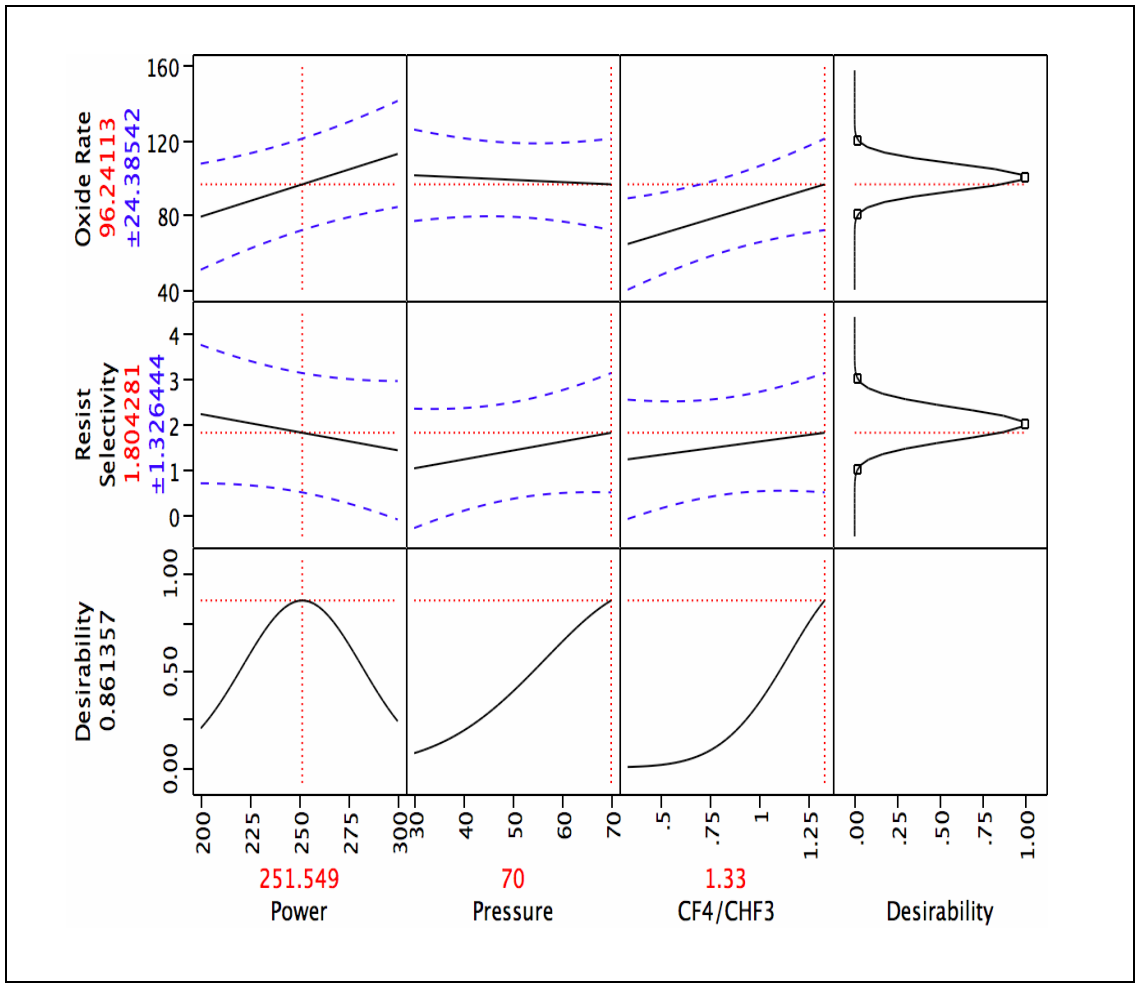


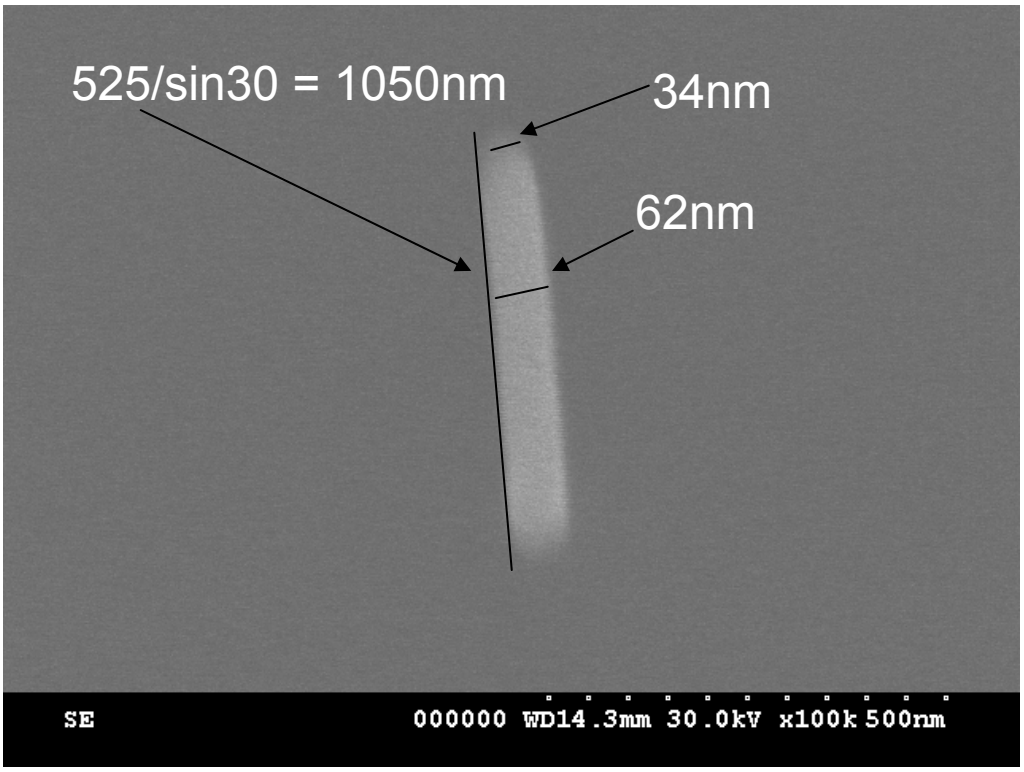
Figure 3-7: Silicon Oxide Etch Response Profiles.

Table 3-5: Optimal Silicon Oxide Process Data.

Optimum Condidtion														
	Variable Factors			Constant Factors				Measurements						
Run	RIE Power (W)	Pressure (mTorr)	CF_4 (sccm)	CHF_3 (sccm)	Etch Time (sec)	ICP Power (W)	CF_4/CHF_3	Resist pre-etch (nm)	Resist post-etch (nm)	Oxide etch depth (nm)	polySilicon etch depth (nm)	$\%CHF_3$	$\%CF_4$	F/C
1	252.00	70.00	67.00	50.00	90.00	0.00	1.34	1530.00	1490.00	144.00	10.00	0.43	0.57	3.15
	Variable Factors			Constant Factors				Calculations						
Run	RIE Power (W)	Pressure (mTorr)	CF_4 (sccm)	CHF_3 (sccm)	Etch Time (sec)	ICP Power (W)	CF_4/CHF_3	Oxide Rate (nm/min)	polySilicon rate (nm/min)	reist rate (nm/min)	Resist Selectivity	poly selecivity		
1	252.00	70.00	67.00	50.00	90.00	0.00	1.34	96.00	6.67	60.67	1.58	14.40		

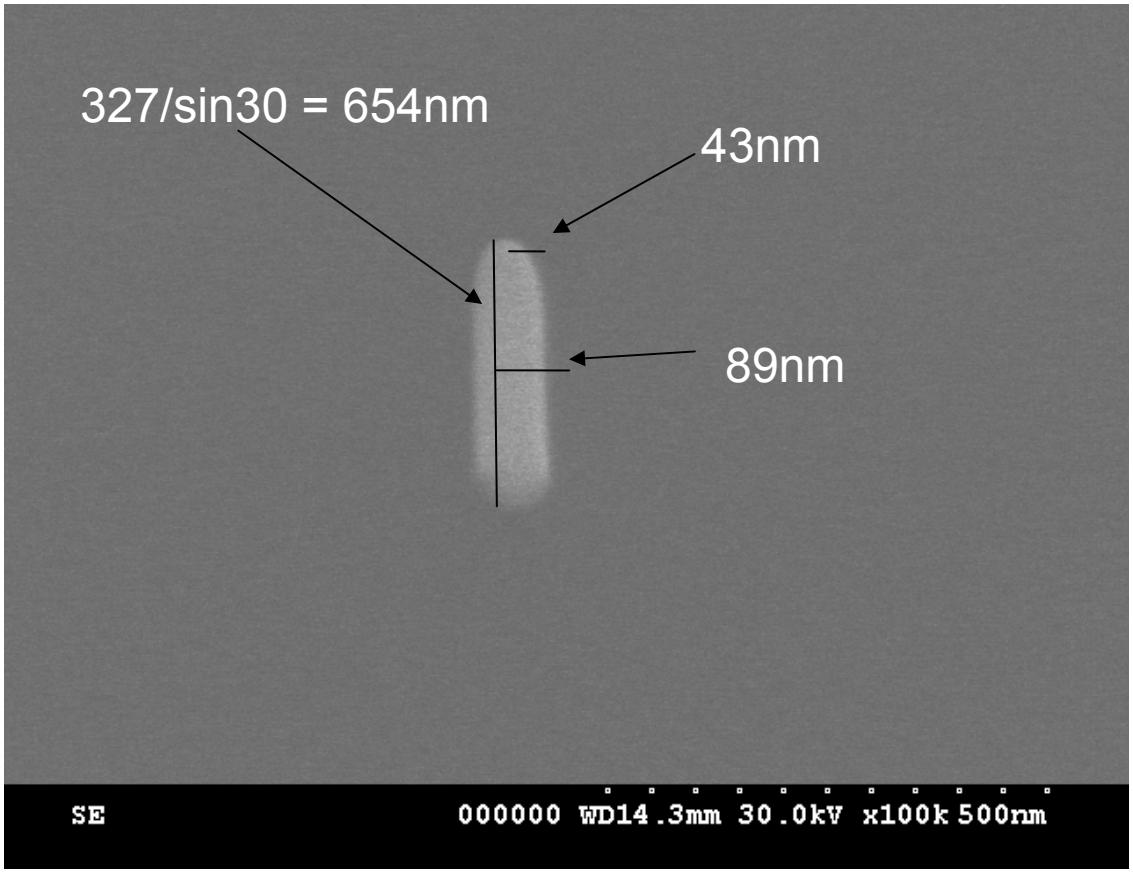
Table 3-6: Experimental Data of the W Nanofiber DOE.

Run	Pressure x10-^{3}	Current (pA)	Energy	Fiber Width (nm)	Fiber Length (nm) for 30 seconds	Fiber Tip (nm)	Tip Angle (degrees)
1	4	25	5	62	525	34	27.89
2	4	75	15	89	654	43	30.96
3	4	125	25	52	728	32	36.02
4	6	25	15	71	538	34	21.44
5	6	75	25	80	769	39	20.69
6	6	125	5	39	712	25	24.22
7	8	25	25	18	920	16	22.61
8	8	75	5	89	688	44	27.25
9	8	125	15	76	1036	32	19.44



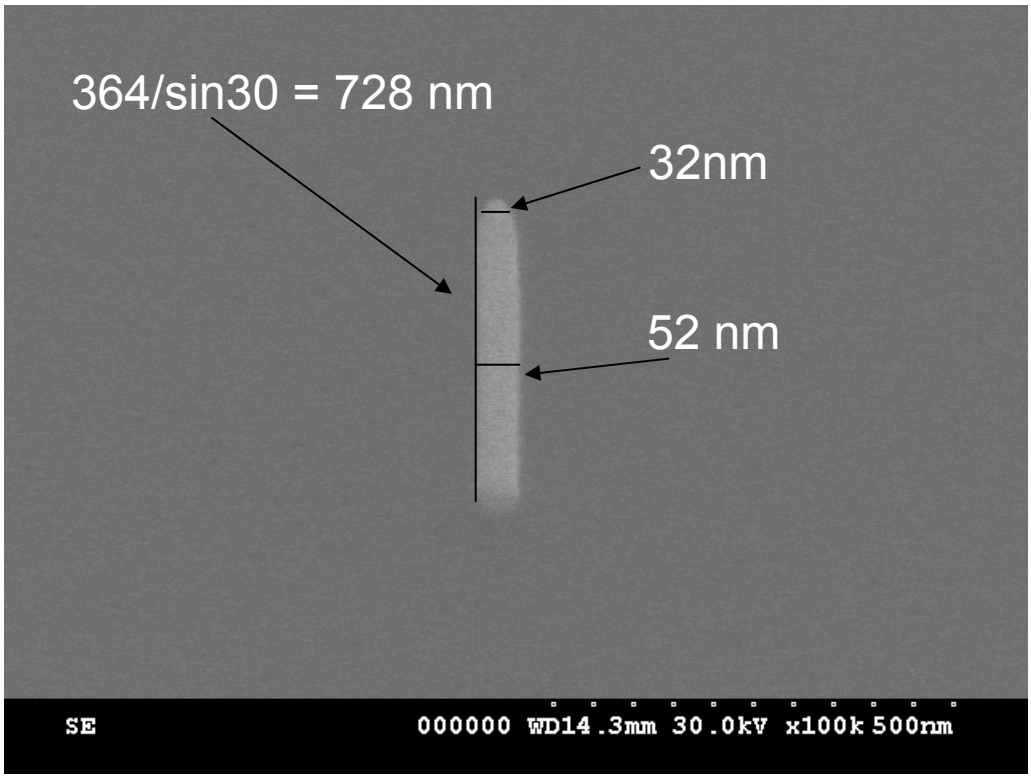
Growth Conditions: $4x10^{-3}$,75pA, WD=1.8, 15KeV, Time=60sec

Figure 3-8: Growth parameter number 1.



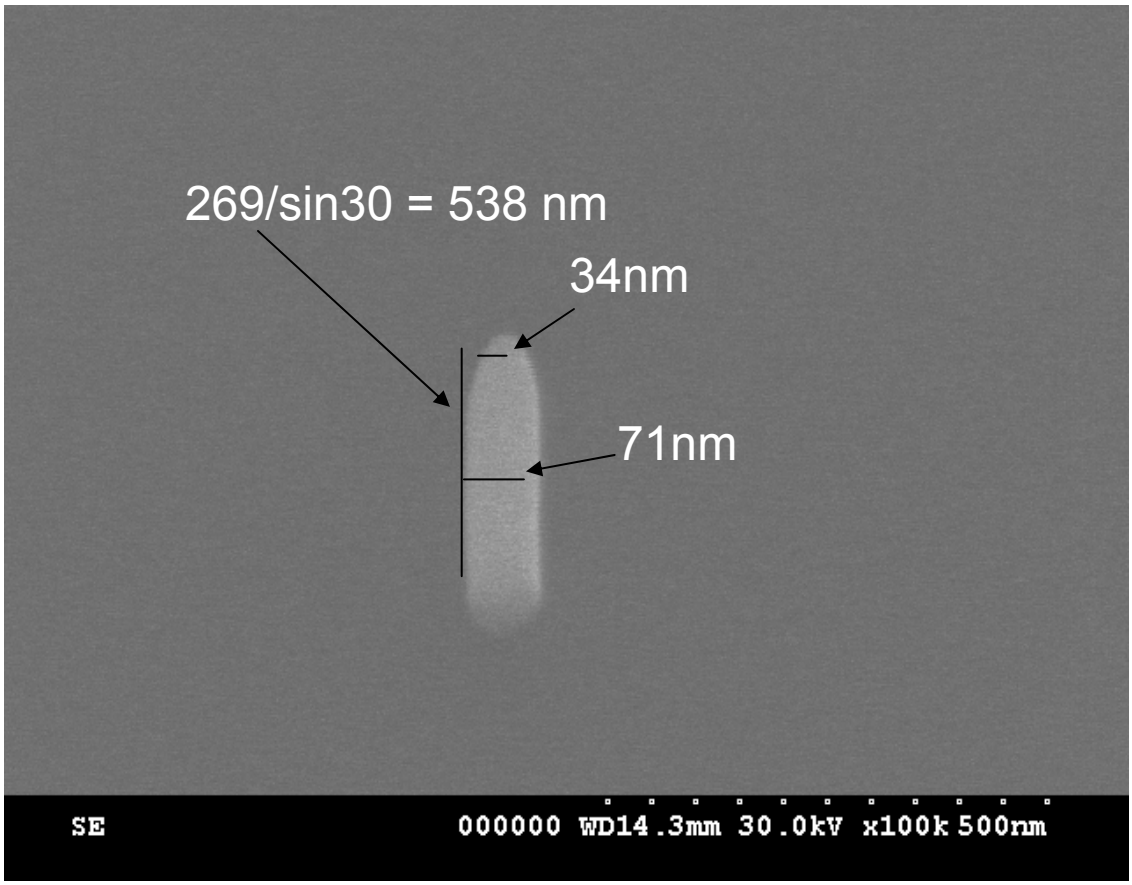
Growth Conditions: $4x10^{-3}$,75pA, WD=1.8, 15KeV, Time=30secs.

Figure 3-9: Growth parameter number 2.



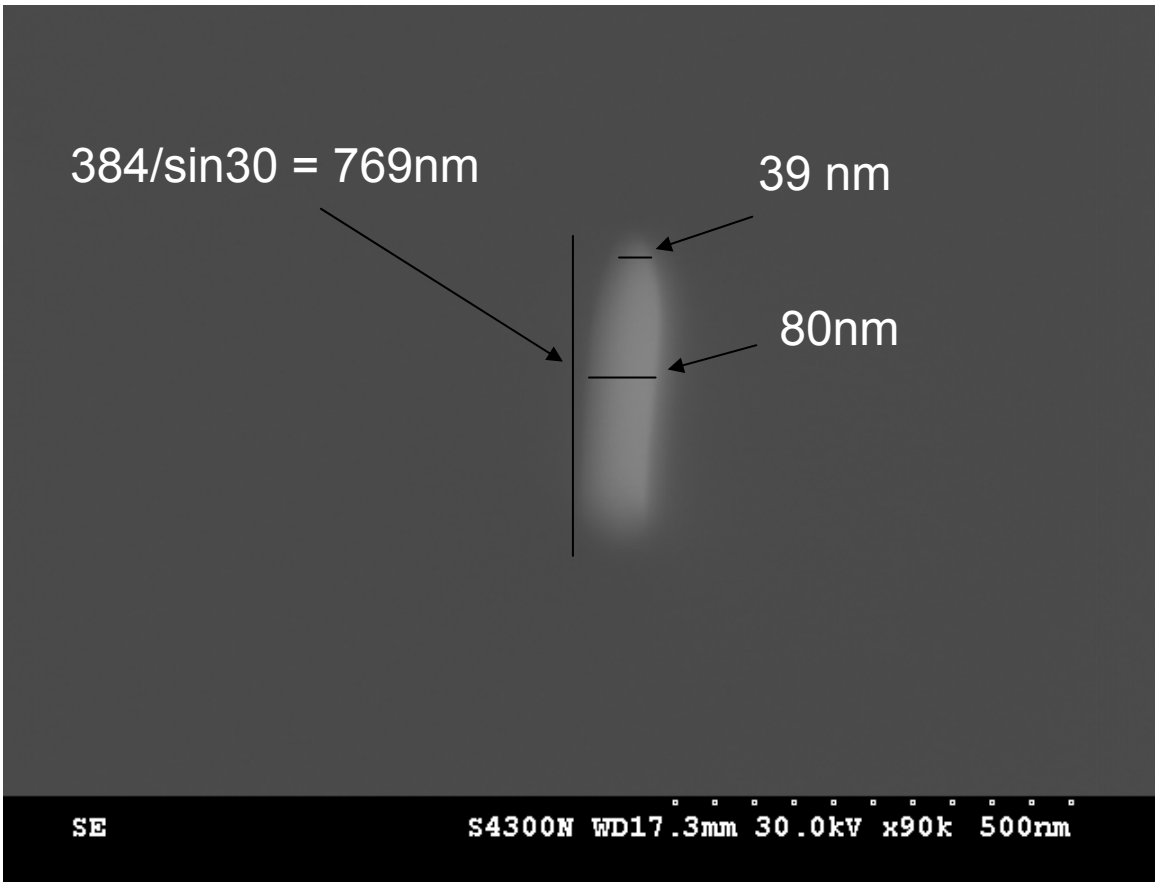
Growth Conditions: 4x10-3,125pA, WD=1.8, 25KeV, Time=30secs.

Figure 3-10: Growth parameter number 3.



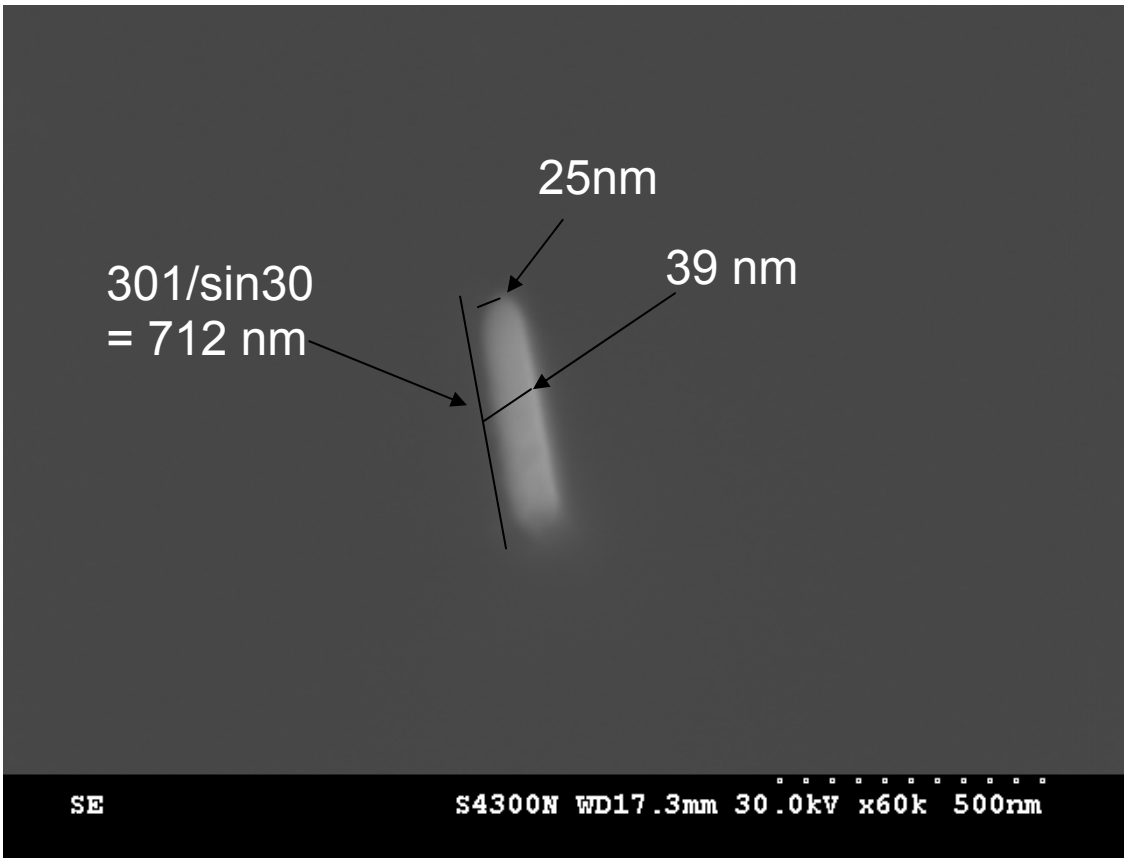
Growth Conditions: 6x10-3,75pA, WD=1.8, 25KeV, Time=30secs.

Figure 3-11: Growth parameter number 4.



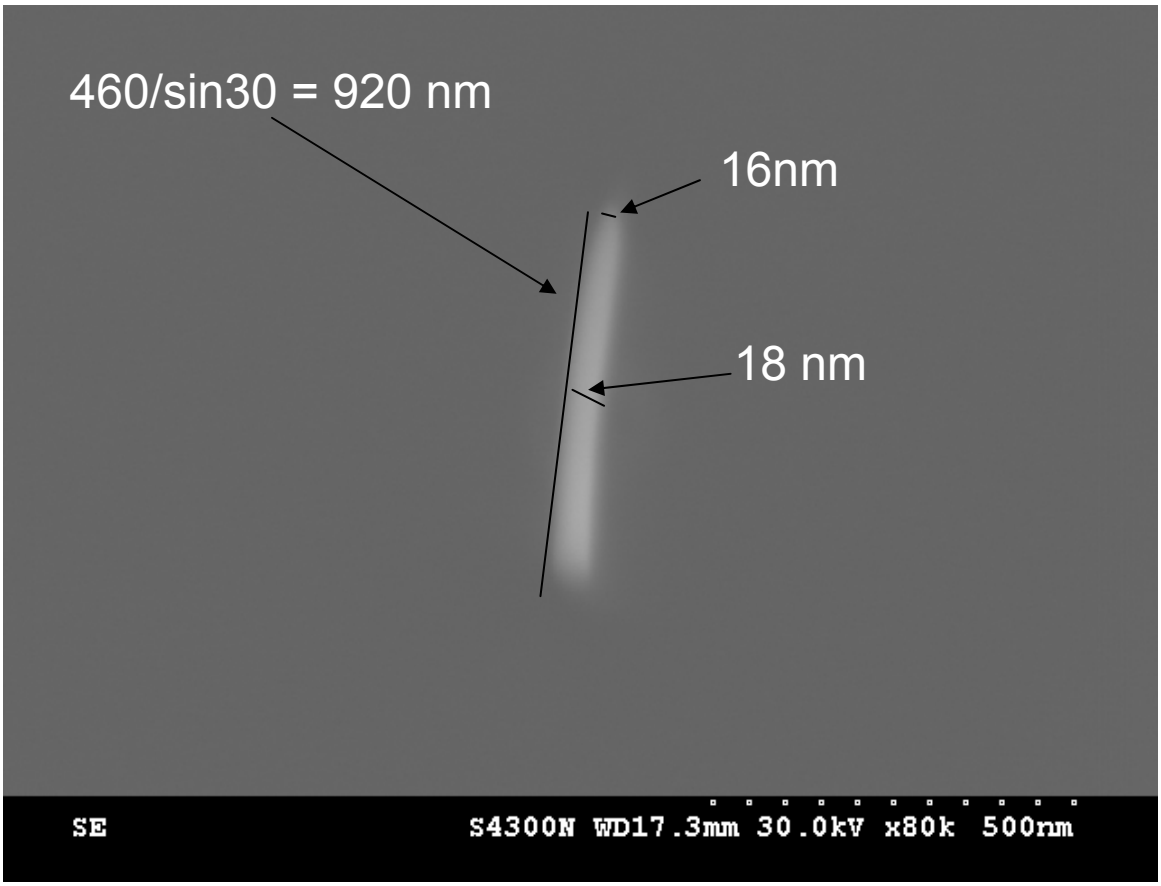
Growth Conditions: 6x10-3,125pA, WD=1.8, 5KeV, Time=30secs.

Figure 3-12: Growth parameter number 5.



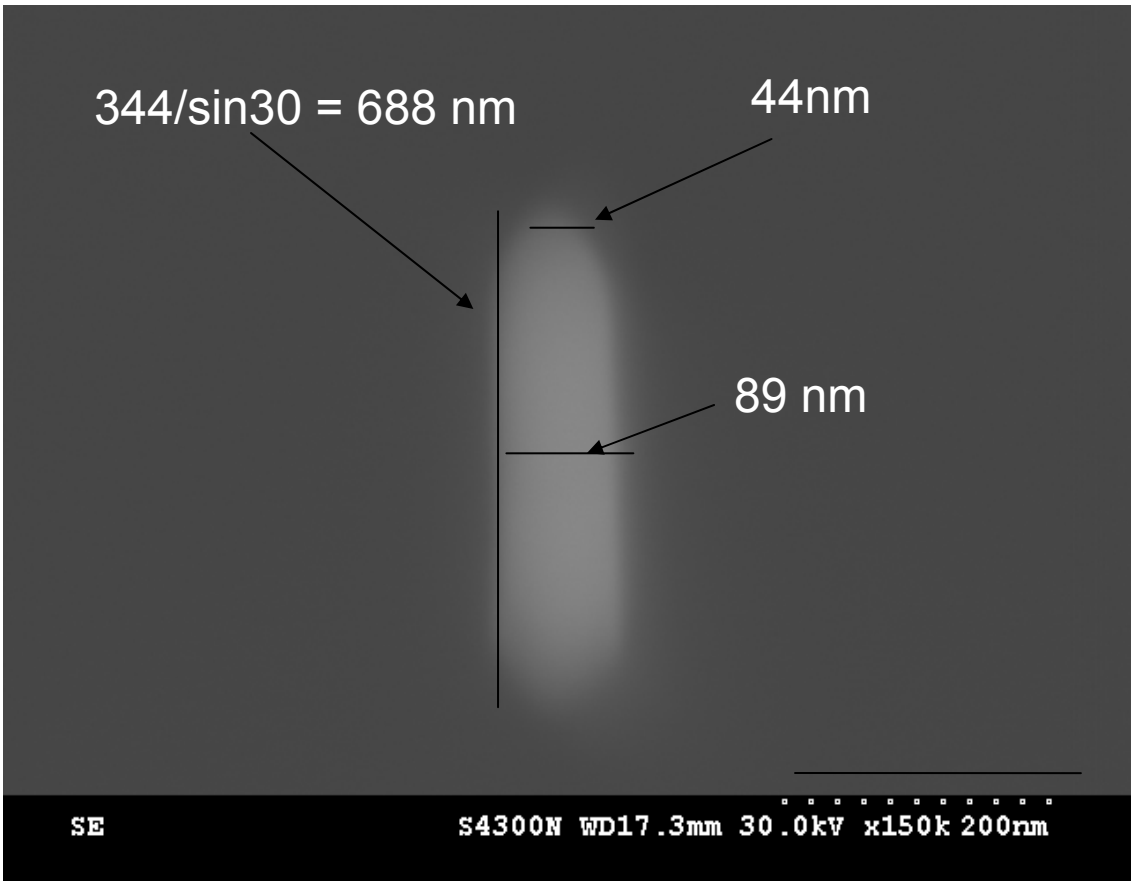
Growth Conditions: 6x10-3,125pA, WD=1.8, 5KeV, Time=30secs.

Figure 3-13: Growth parameter number 6.



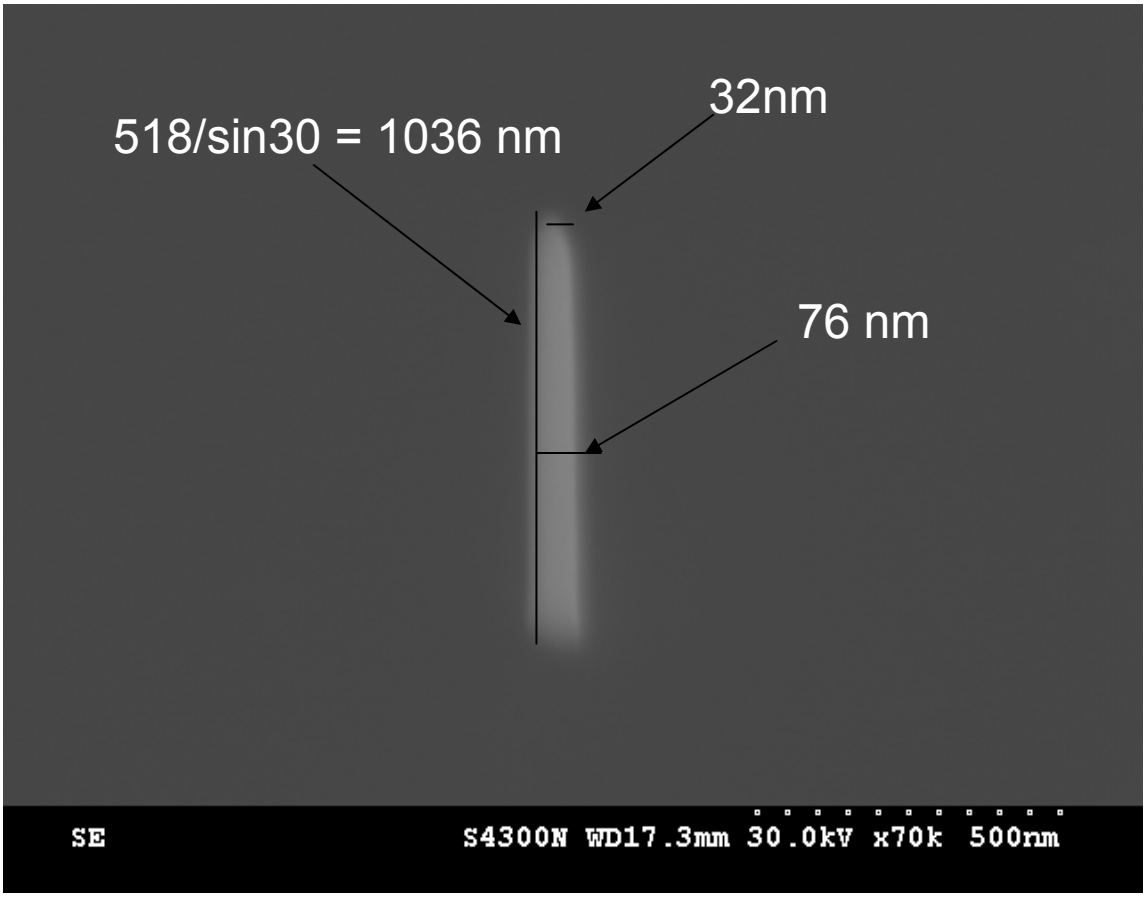
Growth Conditions: 8x10-3,25pA, WD=1.8, 25KeV, Time=30secs.

Figure 3-14: Growth parameter number 7.



Growth Conditions: 8x10-3,75pA, WD=1.8, 5KeV, Time=30secs.

Figure 3-15: Growth parameter number 8.



Growth Conditions: 8x10-3,125pA, WD=1.8, 15KeV, Time=30secs.

Figure 3-16: Growth parameter number 9.

Chapter 4—Discussion

4.1 - Silicon DOE

4.1.1 Introduction

Reactive ion etching (RIE) is a plasma-based dry etching method that is characterized by a combination of physical sputtering from energetic ions and chemical etching from typically reactive radical species.[60] The RIE process allows a material to have a selective etch anisotropy, etches directionally without the use of crystal orientation, transfers lithographically defined photoresist patterns into underlying layers, is a relatively clean process, and is compatible with vacuum-processing technologies.[61] Thus, the dry etching technology is important for the fabrication of all types of micro- and nanoscale devices.[62] High anisotropy is typically achieved by using chlorine and bromine gases in an RIE system. However, these gases are extremely corrosive to a load lock and reactor chamber. Therefore, a less corrosive gas, for instance Sulfur Hexafluoride (SF_6), is desirable which is also less toxic and environmentally better while continuing to provide high etch rates and selectivities.[63]

4.1.2 Sidewall Profile

Figure 3-1 is a series of images of the silicon profile from the different reactive ion etch experiments. Table 3-1 shows the characterization of the scanning electron micrographs. Figure 3-5 illustrates that the pressure has a slight effect on the side-wall angle (Figure 4-1) for single crystal silicon. The side-wall slope is also affected by the interaction of power and pressure (Figure 3-5). The interaction of higher power and pressure decreases the sidewall angle of single crystal silicon. This can be understood by considering the magnitude of the different variables governing the sidewall slope. The experiment desired a 90° side-wall for optimum conditions.

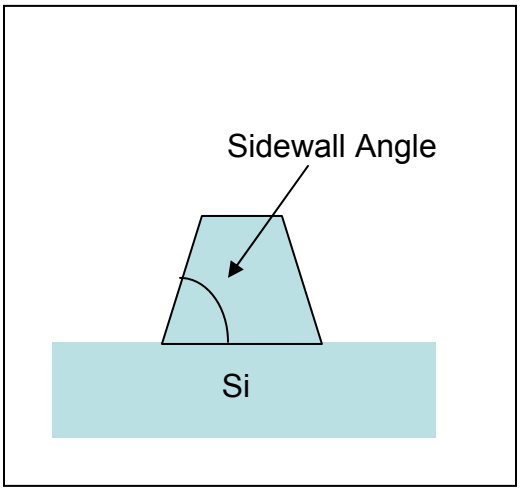


Figure 4-1: Illustration of the sidewall angle that is referenced.

Power

Winderbaum *et al.* showed that increasing power has an important and large effect on the sidewall angle.[64] Initially the sidewall angle is improved, but at higher powers there is some undercutting observed similar to the trends observed in this study. Intially as power is increased, the sidewall angle improves due to an increase in the energetic ion energy which preferentially increases the vertical etch rate. Forte *et al.* explained that as the power increased further the sidewall undercutting is increased. This is because the increased energy is imparted to both the direct and reflected ion radicals impinging on the sidewall during etching. This effect reduces the formation of the sidewall passivation layer of oxide and causes a loss of anisotropy in the sidewall.[65]

Figure 3-5 illustrates that at higher powers the sidewall angle decrease because of the energy that is carried to both the direct and reflected ion radicals impinging on the sidewalls. This is a similar result that Forte *et al.* illustrated.[65] A decrease in power results in a more anisotropic sidewall, because of the decrease in the vertical etch rate.

Pressure

Winderbaum *et al.* demonstrated that pressure has a effect on the sidewall slope because of the change that occurs to the ratio between the lateral and vertical etch rate that is due from the reduction in the mean free path (MFP) when pressure increases.[64]

This reduction causes the etch to become more isotropic. This trend is consistent with the observations from this DOE.

SF_6/O_2 Ratio

The effect of O_2 being added to the system is that the etch profile is improved (higher sidewall angle) which is a result of oxygen passivating the sidewalls and minimizes lateral etching from fluorine radicals.[65] The results from Table 3-2 and Figure 3-5 show that SF_6/O_2 ratio is an important factor for the control of the sidewall slope in single crystal silicon. For many applications it is desirable to have a vertical sidewall. Figure 3-1 (l) represent visually the best profile quality, and Table 3-2 shows that the etch rate for this process was 158 nm. This shows that a more vertical side-wall correlates to a slower etch rate. This is because the higher pressures allow for more reactive species which increases the silicon etch rate, however higher pressure decreases MFP and causes the gas to arrive at diffuse angles which decreases the sidewall angle (Figure 4-2). An increase in the oxygen content in the gas mixture affects the etching profile process in two different ways. First, the oxygen gas reduces the recombination rate of SF_x with free fluorine in the plasma, which increases available fluorine for etching and increases the etch rate. Second, the oxygen molecules compete with fluorine atoms chemisorbing on the silicon surface which reduces the surface fluorine concentration and decreases the etch rate. [61,62] This effect is shown in Figures 3-1 and 3-5, the smaller the ratio of oxygen gas content to the SF_6 shows a strong effect on the slope of single crystal silicon. Figure 4-2 illustrates how an increase in O_2 concentration causes the O_2 radicals to compete with

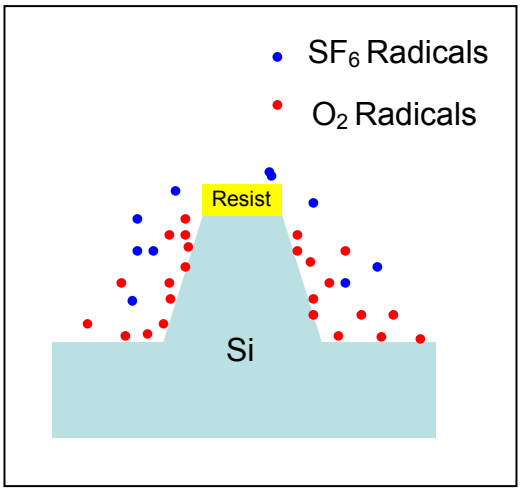


Figure 4-2: Diagram illustrating the effect of an increase in O_2 concentration.

the F for Si sites leading to a decrease in silicon etch rate and an increase on the sidewall etch.

4.1.3 Silicon Etch Rate

Power

Figure 3-5 shows that increasing R.F. power leads to an increase in the silicon etch rate. In general, an increase in R.F. power leads to the formation of more fluorine radicals and ions because at higher R.F. power there is an increase in ionization and dissociation of SF_6 gas which increases the silicon etch rate.[64] In this case, ion induced etching and chemical induced etching are both increased.

Hotovy *et al.* demonstrated that increasing R.F. power linearly increases the etch rate of silicon.[60] Legtenberg *et al.* showed that the silicon etch rate increase with R.F. power as a result of a significant increase of atomic fluorine concentration.[62] Winderbaum *et al.* explained that this increase in silicon etch rate with an increase in R.F. power is dependent on the concentration of F radicals.[64] Paul *et al.* showed that the increase in R.F. power results in the formation of more fluorine radicals with increased ionization and dissociation of SF_6 gas leading to an increase in the silicon etch rate.[66]

The experimentally observed difference in the silicon etch rate is also shown in the contour plots in Figure 3-2 as a function of different SF_6/O_2 gas flow ratios. Figure 3-2, SF_6/O_2 ratio = 2, illustrates that an increase in R.F. power to the highest limit increases the etch rate. Figure 3-2, SF_6/O_2 ratio = 6, shows a maximum in the etch rate at the middle R.F. power level of 300 W and decreases at higher power. Figure 3-2, SF_6/O_2 ratio = 10, shows that an increase in power to the highest limit increases the etch rate. The effect that the SF_6/O_2 ratio has on the overall etch rate is a complex interaction of oxygen dilution which lowers the etch rate and oxygen interactions with SF_x radicals which liberates fluorine and increases the etch rate. Oxygen reacts with SF_x radicals and prevents their recombination with fluorine to reform SF_6. This leads to a net increase in F radical density, and hence an increase in silicon etch rate with the addition of oxygen.[60]

Pressure

Syau *et al* demonstrated that the etch rate of single crystal silicon decreases as the pressure is increased, which is consistent with this study.[67] Typically as pressure

increases, the mean free path of ions and reactive radicals decreases. Consequently, while there is also typically more ionization and dissociation at higher pressure, there is also more recombination of reactive species. Furthermore, ions are generated and accelerated towards the surface to induce sputtering and by-product desorption, and higher pressure effectively lowers there kinetic energy and decreases the silicon etch rate.

In Figure 3-5 and Table 3-2, SF_6/O_2 ratio = 2, illustrates that an increase in pressure increases the silicon etch rate at higher R.F. powers. This rise in silicon etch rate is likely related to the concomitant increase in the fluorine concentration availability as the total pressure is increased. This is because there is more dissociation of SF_6 molecules leading to more etchant fluorine atoms. Also at higher powers the energy of the generated ions increases and even though they will suffer collisions in route to the substrate, the average energy increases as R.F. power increases. At SF_6/O_2 ratio = 6, illustrates that as the pressure increases, the etch rate of silicon decreases at low and high pressures and R.F. power values except for the middle range (150 – 250 mTorr and 200-300W). At this SF_6/O_2 ratio there are obviously competing effects going on. The optimum power/pressure is likely due to competing SF_6 production, SF_x – fluorine recombination, and total ion energy. As previously described, as pressure increases, even though more SF_6 is available for etching, there will be more recombination and the overall ion energy will decrease due to the shorter mean free path. It is interesting that at higher powers there is actually a decrease in the etch rate. This suggests that fluorine – SF_x recombination is occurring. The SF_6/O_2 ratio = 10, illustrates that at low power the silicon etch rate remains relatively constant as pressure is increased, but at high power the etch rate of silicon decreases as pressure is increased. Conversely, at low pressure and

increasing power the etch rate continuously increases, however, at higher pressure the etch rate saturates and is relatively constant with increasing power. This trend could be due to excessive recombination that occurs at this flow ratio because there is very little oxygen present to mitigate the fluorine radical recombination.

SF_6/O_2 Ratios

Figure 3-5 illustrated that as the O_2 concentration increases the silicon etch rate increased until a middle plateau was reached. Hotovy *et al* explained that as the oxygen content is increased the silicon etch rate increases.[60] After the a certain oxygen flow rate, the silicon etch rate decreases slightly due to the result of the competition of oxygen atoms with fluorine atoms for chemisorption (the adsorption in which the forces used are valence forces of the same kind as those operating in the formation of chemical compounds) on the silicon surface.[60] Paul *et al.* demonstrated that the silicon etch rate increases continuously until a maximum is reached at a moderate oxygen flow regime.[66] Initially as the oxygen flow rate increases, the etch rate of silicon increases because the oxygen reduces the recombination of fluorine radicals with SF_x. At higher oxygen flow rates, the oxygen competes with F radical chemisorption on the silicon surface, which decreases the silicon etch rate.[64]

4.1.4 Silicon to Silicon Oxide Selectivities

Figure 3-3 represents the experimental Si to SiO_2 selectivities for the silicon DOE. The Si to SiO_2 selectivity is the silicon etch rate divided by the silicon oxide etch rate. The selectivity is very important because it represents the effect of the silicon etch recipe on silicon oxide which for the DEAL device is the underlayer to the intended silicon electrodes. It is desired to have a high silicon to silicon oxide selectivity. Table 3-2 represents the measured data collected from the experiments.

Figure 3-5 and Figure 3-3 both show that the Si to SiO_2 selectivity all peaked in the mid-range of the variables that were studied. Of course this response is a function of the differentia etch rate of silicon and silicon dioxide at each specific etch recipe. At high powers, physical sputtering typically dominates which in general lowers the selectivity of an etch process. For the pressure variable, it is surmised that the selectivity goes down because the recombination and passivation effects likely reduce the silicon etch rate more severely than the silicon oxide. Similarly, higher SF_6 ratios likely compromise the silicon etch rate more, because near the silicon oxide surface, oxygen liberated from the etched film can help mitigate recombination effects whereas for the silicon film no oxygen is present.

In Figure 3-3 and Table 3-2 SF_6/O_2 ratio = 2, the Si to SiO_2 selectivity increases with an increase in pressure and a decrease in power. Overall, the selectivity for this flow ratio is lower than the other flow ratios. In general the selectivity for silicon to silicon

oxide etching in an SF_6/O_2 RIE is dependent on power and SF_6/O_2 ratios. Figure 3-3 SF_6/O_2 ratio = 6, illustrates that the selectivity increases when the pressure and power are in the middle regime. Figure 3-3 SF_6/O_2 ratio = 10, shows a similar trend as that of Ratio 6 except the range is not as high as for the gas ratio = 6. The Si to SiO_2 selectivity increases only in the middle of the power and pressure range. SF_6 is known to give high Si to SiO_2 selectivities.[66] This is related to the generation of large F atom density in the SF_x plasma resulting in high silicon etch rates. However, the large F atom density results in the RIE process to be more chemical, and therefore, less anisotropic.[67] As mentioned in section 4.1.2, the increase in anisotropy with SF_6 can be realized, by increasing the sputtering or ion bombardment during etching. Therefore, an exchange between selectivity and anisotropy is necessary. Figure 3-3 and the Si to SiO_2 selectivities with SF_6/O_2 gas mixtures in Table 3-2 are compared and show that the high Si to SiO_2 selectivities correspond to the profiles that demonstrate the desirable profile. The highest selectivity is found to be at a pressure of 238 mTorr, SF_6/O_2 gas mixture of 6, and a power of 250 W, which agrees with the contour maps of Figure 3-3. From Figure 3-3 and Table 3-2, the low selectivity values are related to the fact that SiO_2 etch rate increases faster than the silicon etch rate with increasing R.F. power density.[67] Both from a selectivity and anisotropy perspective, excessive R.F. power can be undesirable.[67]

4.1.5 Silicon to Photoresist Selectivities

The experimental silicon to photoresist selectivities are shown in Figure 3-5 and the measured silicon to photoresist selectivities are presented in Table 3-2.

Figure 3-5 shows that the Si to photoresist selectivity increases with R.F. power until a maximum is reached around 300 W. At the low R.F. power, the Si to photoresist selectivity is lower because of the R.F. power preferentially ionizes and dissociates the O_2 gas which attacks the resist leading to the lower silicon to photoresist selectivities.[68] In Figure 3-5, with an increase in pressure to around 200 mTorr, the silicon to photoresist selectivity increases and then decreases with an increase in pressure beyond this pressure. This is explained by the continual increase in pressure leads to the reduction in energy of bombarding ions affecting the physical contribution to the silicon etching. The sharp drop in Si to photoresist selectivity at high pressures is due to the sharp change in silicon etch rate at high pressures.

Figure 3-5, shows with an increase in SF_6/O_2 ratio to a maximum around 6, the silicon to photoresist selectivity increases, and subsequently decreases at higher SF_6/O_2 ratios. The selectivity of silicon to photoresist is of course a balance between the two etching rates of the materials. However, the etching rates can be coupled to the processing parameters. For instance in the case of adding oxygen to the gas mixture (decreasing SF_6/O_2), initially as O_2 is added to SF_6, the silicon etch rate is increases significantly due to effects described earlier. However, the resist etch rate also increases albeit at a lower rate. Eventually at higher oxygen flow rates, the silicon etch rate decreases and the resist etch rate increases leading to a more severe compromise in the selectivity at higher oxygen flows.

Figure 3-4 shows that as the O_2 ratio levels decrease the higher Si to photoresist selectivity becomes more localized in the middle. From Figure 3-4 SF_6/O_2 ratio = 2, the silicon to photoresist selectivities increase at high powers and middle pressures. To have

high silicon to photoresist selectivities at this flow ratio, the power and pressure should be increased to form more fluorine atoms with an increased ionization and dissociation of SF_6 gas molecules which bombard silicon but does not etch the resist proportionately resulting in higher silicon to photoresist selectivity. Figure 3-4 SF_6/O_2 ratio = 6, illustrates that the silicon to photoresist selectivities increases proportionally to the increase in power and pressure until a plateau is reached at 250 W and 250 mTorr. After this plateau, a decrease in selectivity is observed. This could be related to when the power and pressure are either low or high they have a reduction in energy affecting physical contributions that result in the etching of resist at a higher rate. Figure 3-4 SF_6/O_2 ratio = 10, illustrates that when the pressure is high the selectivities are very low, but as the pressure is decreased and power is increased the selectivity forms a median at 250 W and 250 mTorr.

4.1.6 Optimum Condition for Silicon DOE

After the analysis was done on the DOE, an optimum condition was determined. The optimum condition was applied to single crystal silicon, n^+ polycrystalline silicon, and silicon oxide wafers. It was also necessary to know the etch characteristics of the n^+ polycrystalline for the application in the DEAL devices. The optimum condition process (293 W, 160mTorr, and ratio = 6 of SF_6 to O_2 gas mixture) is given in Table 3-3 and in Figure 3-5. Figure 3-5, also shows on the y-axis the target values (in red) based on the optimum condition with the variation listed (in blue). The optimum process for single crystal silicon yielded an experimental etch rate = 1258 nm/min, 12.42 Si to silicon oxide

selectivity, profile quality = good/excellent, and 6.79 Si to photoresist selectivity compared to an expected value of silicon etch rate of 868 nm/min, 140 Si to silicon oxide selectivity, profile quality = Poor/Good, and 1.43 Si to photoresist selectivity. The optimum process for n^+ polycrystalline silicon yielded a silicon etch rate of 1000 nm/min, n^+ polycrystalline silicon to silicon oxide selectivity = 9.87, and a n^+ polycrystalline silicon to photoresist selectivity = 5.38. Figure 3-8 shows profile angle of the optimum process in the single crystal silicon. The image illustrates an excellent etch profile.

4.2 Silicon Oxide DOE

4.2.1 Introduction

An important aspect of nanofabrication is the ability to effectively etch vias and trenches in silicon oxide. Silicon oxide is commonly used in nanotechnology as a substrate, a masking material, or for electrical insulation.[69] The method of utilizing a wet etch for the etching of silicon oxide has grown less effective due to the dimensions of the devices entering micron and nanometer scales. Wet etching only provides an isotropic etch. Many nanotechnology devices require an anisotropic profile leading to the necessity of developing an optimum dry silicon oxide etch process. Current etching techniques utilize a fluorocarbon plasma to achieve a silicon oxide etch with excellent profiles and selectivities. This chapter and section discusses the theoretical and analytical results of the DOE for an optimal fluorocarbon etch for silicon dioxide for the DEAL

device. The design utilized silicon oxide and n^+ polycrystalline silicon substrates to optimize design parameters that included: R.F. power, pressure, and CF_4 to CHF_3 ratio.

4.2.2 n^+ Polycrystalline Silicon

Table 3-4 illustrates that the effect of all the variables on the n^+ polycrystalline silicon was negligible. There was no silicon oxide to n^+ polycrystalline silicon selectivity below a ratio of 10:1 that was observed. This could be caused from a low fluorine concentration in the plasma and a thick fluorocarbon interaction layer on the n^+ polycrystalline silicon surface. Therefore, the silicon oxide to silicon selectivity response was disregarded in the optimal design as all of these values were acceptable.

4.2.3 Silicon Oxide Etch Rate

The etch of silicon oxide in a CF_4 and CHF_3 gas mixture happens through a relatively thin fluorocarbon reaction layer.[70] Controlling the deposition and etching of this reaction layer has profound effects on the total etch rate and selectivity versus silicon and resist. Table 3-4 represents the experimental data collected from the DOE. Figure 3-7 shows the responses from the different processes performed for this DOE.

Power

The effect of R.F. power on the SiO_2 etch rate has a profound effect. The role that R.F power has is both chemical and physics. The plasma power provides energy for

electron impact reactions which produce radicals, atoms, and ions that react with the substrate atoms to form volatile products or polymerize as $(CF)_x$ films on the substrate surfaces.[71] The increase in R.F. power leads to more dissociation and ionization of the fluorocarbon species which also increases the number and energy distribution of ion bombardment on the wafer surface.[71] Figure 3-7 illustrates that the silicon oxide etch rate increases linearly with an increase in R.F. power. The increase in R.F. power also increases the ion energy to activate the reaction process resulting in a higher SiO_2 etch rate. Gaboriau *et.al.* showed that the SiO_2 etch rate is mainly dependent on the ion energy.

Pressure

At the higher pressures, the possibility for polymerization or radical recombination increases. Furthermore because the mean free path of ions decreases at higher pressures, the physical sputtering component also decreases.[72] Subsequently, these factors result in a decline in SiO_2 etch rate at higher pressures.[72] The affect of the H atoms from CHF_3 at high pressures can also facilitate $(CF)_x$ polymerizations on the substrate surfaces. These reactions inhibit the formation of volatile Si-F radicals (SiF_2, SiF_3, SiF_4) which results in lower SiO_2 etch rates.[72,73] Consistent with these expectations, Figure 3-7 and Table 3-4 illustrates that an increase in pressure slightly decreases the etch rate of silicon oxide.

CF_4/CHF_3 Ratios

The addition of hydrogen-containing molecules has been shown to reduce the concentrations of the reaction products as well as to increase the variety reactant and product species.[72] The experimental difference with CF_4/CHF_3 ratios in the silicon oxide etch rate is shown in Figure 3-7 and Table 3-4. The results show that the silicon oxide etch rate increases with an increase in CF_4/CHF_3 ratio. This increase in the CF_4/CHF_3 ratio leads to a decrease in the H atom concentration. Higher concentrations of H atoms decrease the effective F/C ratio resulting in the decrease in formation of SiF_4 and consequently a decrease in the etch rate of SiO_2. Lower F/C ratios also leads to polymerization which is demonstrated in the negative photoresist etch rate (growth) that occurred in process 7 in Table 3-4. This lower F/C ratio enhances polymerization which also forms on the n^+ polycrystalline surface and inhibits silicon etching. The silicon oxide etch rate is lower, but still positive because on the SiO_2 surface the oxygen in the film reacts with the carbon (C) forming CO and CO_2. This inhibits the polymerization reaction on the oxide surface. In process 8, unexpected polymerization occurred. The only factor that would favor polymerization was the low power.

4.2.4 Silicon Oxide to Photoresist Selectivities

The experimental silicon oxide to photoresist selectivities are shown in Figure 3-7 and the measured silicon oxide to photoresist selectivities are presented in Table 3-4.

Power

Figure 3-7 shows that as the R.F. power is increased the SiO_2 to photoresist selectivity decreases even though there is an increase in SiO_2 etch rate at higher power. Table 3-4 illustrates that the resist etch rate increases faster with R.F. power than does the oxide etch rate. The faster resist etch rate in the fluorocarbon chemistry causes the overall silicon oxide to resist selectivity to decrease at higher power.

Pressure

Photoresist etch rates typically decrease with high amounts of carbon-rich molecules due to polymerization.[73] Figure 3-7 illustrates the SiO_2 to photoresist selectivity increases with an increase in pressure. This is due to the increase in pressure preferentially causes polymerization on the photoresist relative to the silicon oxide surface which has the oxygen source to mitigate polymerization. As mentioned earlier, at lower pressures the ion energy also increases which inhibits polymerization and decreases the selectivity.

CF4/CHF3 Flow Ratios

Riley *et al.* demonstrated an increase in F/C ratio leads to an increase in photoresist etch rate.[71] In Figure 3-7 the SiO_2 to photoresist selectivity increases as the CF_4/CHF_3 ratio increases. This result suggests that as the CF_4/CHF_3 ratio increases, the

oxide etch rate increases faster than the resist which causes the overall selectivity to increase. As discussed earlier in this section, the increase in the CF_4/CHF_3 ratio leads to an increase in the F/C ratio, which increases the SiO_2 etch rate.

4.2.5 Optimum Condition for Silicon Oxide DOE

The optimum prediction profiles are illustrated in Figure 3-7. The actual data measured is presented in Table 3-5. It is necessary to know the etch characteristics of silicon oxide for the DEAL devices. The optimum condition was at 252 W, 70 mTorr, and a 1.34 ratio of CF_4/CHF_3 gas mixture. Table 3-5 shows that the ideal conditions yielded an oxide rate of 96 nm/min and a SiO_2 to photoresist selectivity of 1.58. These results are very close to the optimum predicted values of Figure 3-7.

4.3 Tungsten Nanofiber EBID DOE

Figures 3-8 – 3-16 show the nine different SEM images of the different EBID processes performed in this DOE in Table 3-6. The goal of the EBID DOE was to determine the optimum parameters that would yield a sharp fiber structure that would enhance the field emission characteristics of the DEAL device. Due to the problems of effectively fabricating the DEAL devices, only the structure characteristics were studied. It was desired to deposit a nanofiber having a high deposition rate, and a sharp tip angle yielding optimum electrical properties. The condition that yielded the best characteristics is shown in Figure 3-14 and is run number 7 in Table 3-6. The growth conditions were a

pressure of 8 x 10^{-3} Pascal (high pressure), beam energy of 25 keV (high-energy), beam current of 25 pico Amps (low current), and a time of 30 seconds. Though beyond the scope of this thesis, the optimum conditions are consistent with a recently developed EBID simulation that our group has developed.[74] The nanofiber was 18 nm wide, 980 nm tall, had a tip diameter of 16 nm, and the distance between the substrate sample and the vapor injection nozzle of 1.8 mm. The goal was to then deposit high-quality tungsten cathodes into the aperture well of the DEAL device as the field emitting element.

Chapter 5—Conclusion

The problems with the RIE processes effectively etching the n^+ polycrystalline silicon and thermal oxide layers of the DEAL devices instigated the need for the research presented in this thesis. An effective DOE of the reactive ion etch processes for the n^+ polycrystalline silicon and thermal oxide silicon layers were performed. The DOE implemented a JMP desktop statistical discovery software from SAS® for the characterization and analysis for the two etch chemistries. The characterization and analysis of these two etches are critical to the fabrication of the DEAL devices.

Single crystal silicon wafers with the DEAL gate electrode pattern were used for the characterization of the n^+ polycrystalline silicon etch process. The single crystal silicon material was used because the etch rate varied significantly and to determine with reasonable accuracy the etch rate, materials thicker than the 500 nm layer of n^+ polycrystalline silicon specimens were needed. Silicon wafers with a 1 micron thermally oxidized silicon oxide layer were used for determining the silicon to silicon oxide selectivity. The DOE of silicon varied R.F. power, pressure, and SF_6 gas. Constant variables included: time (90 seconds), ICP power (0), and O_2 gas flow (5 sccm). The DOE consisted of sixteen different processes to effectively optimize the silicon etch rate, silicon to silicon oxide selectivity, silicon to photoresist selectivity, and the etch profile angle quality. The processes yielded an optimum condition of a power = 294 W, pressure = 160 mTorr, and SF_6 gas flow = 30 sccm with the equivalent constant variables. The research showed an increase in power lead to an increase in silicon etch rate, an increase and then a decrease in silicon to silicon selectivity, an increase in profile angle quality,

and a relative increase in silicon to resist selectivity. An increase in pressure, resulted in a decrease in silicon etch rate, a relative increase in silicon to silicon oxide selectivity, the profile angle decreased and then increased, and an increase then a decrease in silicon to photoresist selectivity. The increase in SF_6/O_2 gas ratio lead to an increase then a decrease in silicon etch rate, an increase then a decrease in silicon to silicon oxide selectivity, a decrease in profile angle quality, and an increase then a decrease in silicon to photoresist selectivity. The optimum condition yielded a silicon etch rate of 971 nm/min, an oxide selectivity of 12.42, a profile angle quality of excellent, and silicon to photoresist selectivity 6.79. It was necessary to perform the optimum process on n^+ polycrystalline silicon which will be used for the DEAL devices. The optimum recipe was only performed for 30 seconds due to the thickness of the n^+ polycrystalline film. The optimum recipe was performed on n^+ polycrystalline silicon to yield an etch rate of 1000 nm/min, an oxide selectivity of 9.87, and an n^+ polycrystalline silicon to photoresist selectivity of 5.38. The profile angle quality was not analyzed because of the similar sidewall characteristics of single crystal silicon etch. The specific etching trends were correlated to literature values and understood based on fundamental physics of SF6/O2 plasmas.

Thermally grown oxide coated wafers were used for the characterization of the silicon oxide etch process. Wafers of n^+ polycrystalline silicon with the DEAL gate electrode pattern were utilized to characterize the silicon oxide to n^+ polycrystalline silicon selectivity. The experimental data showed the silicon oxide to n^+ polycrystalline silicon selectivity was greater than 10:1 (more than sufficient), so it was neglected as part of the optimization calculation. The DOE of silicon varied R.F. power, pressure, and CF_4

gas. Constant variables included: time (90 seconds), ICP power (0), and CHF_3 gas (50 sccm). The DOE used nine different processes to optimize the silicon oxide etch rate and silicon oxide to photoresist selectivity. The processes yielded an optimum condition of a power = 252 W, pressure = 70 mTorr, and 67 sccm of CF_4 gas with equivalent constant variables. The DOE processes showed an increase in power lead to an increase in silicon oxide etch rate and a decrease in silicon to photoresist selectivity. The increase in pressure resulted in a decrease in the silicon oxide etch rate and the silicon oxide to photoresist selectivity. An increase in the CF_4/CHF_3 ratio lead to an increase in silicon oxide etch rate and an increase in silicon oxide to photoresist selectivity. The optimum condition yielded a silicon oxide etch rate of 96 nm/min and a silicon oxide to photoresist selectivity of 1.58. Again the results were compared to other fluorocarbon reactive ion etching studies and the basic trends were understood based on the physics of fluorocarbon plasmas.

An EBID characterization DOE was employed for studying the structure characteristics of W field emitting nanofibers. The DOE implemented a design varying chamber pressure, electron beam energy, and specimen beam current. It was determined that the optimum conditions that lead to a high growth rate and a sharp nanofiber structure occurred at high pressure (8x a10^{-3}), high beam energy (25 keV), and low beam current (25 pico Amps) which was consistent with the literature and recently simulated EBID growth.[74]

Finally, these results are of excellent importance for the DEAL device fabrication and should lead to an increase in effectively fabricating DEAL devices.

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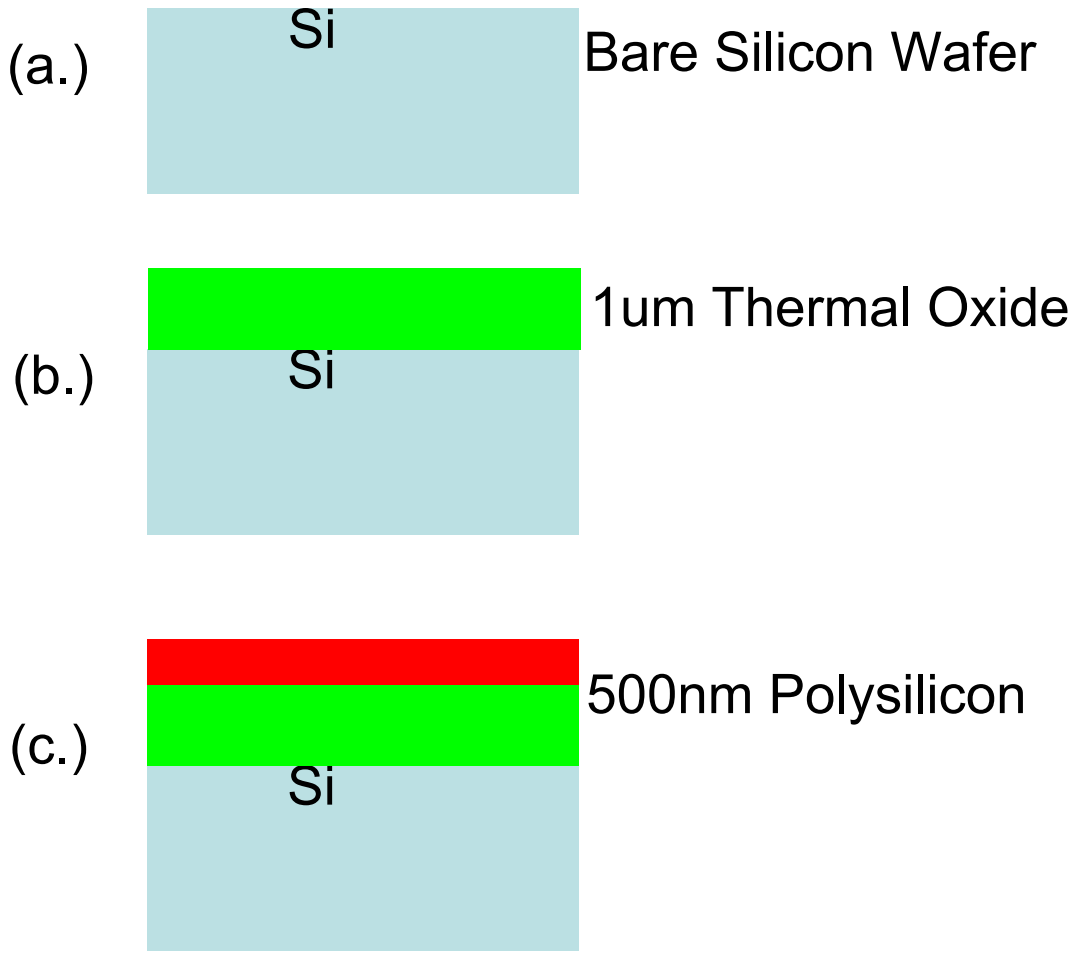
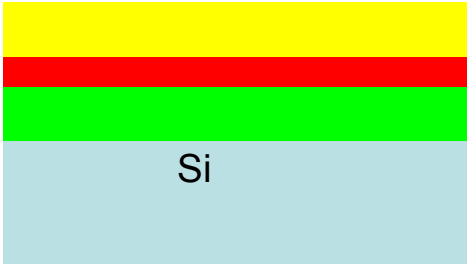
Appendix A

Figure 2-1

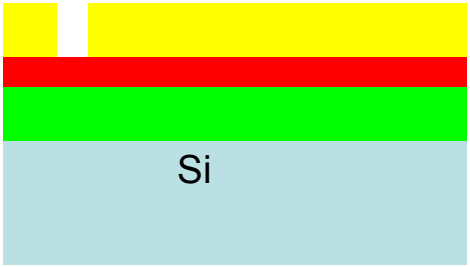

(a.)
Si
Bare Silicon Wafer
(b.)
1um Thermal Oxide
Si
(c.)
500nm Polysilicon
Si

(d.)



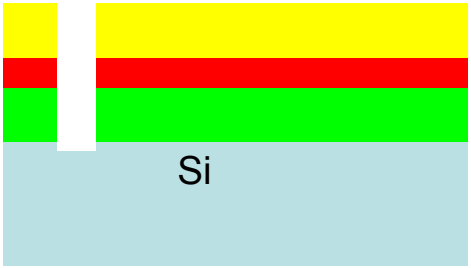
2.1um 955cm Photoresist
≈ 1.6um

(e.)



Alignment Marks

(f.)

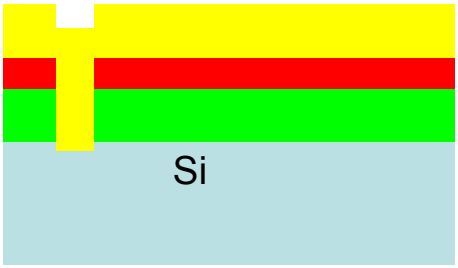


Etch Alignment
Marks

(g.)

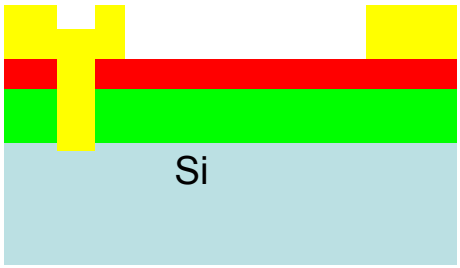
Strip Resist

(h.)



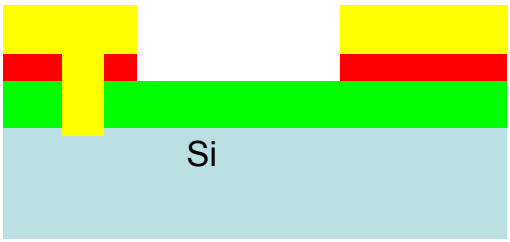
2.1um 955cm Photoresist
≈ 1.6um

(i.)



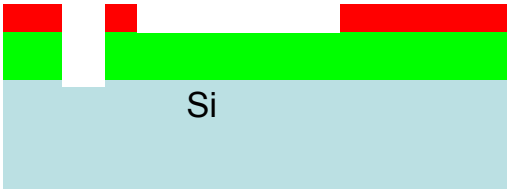
Gate Electrode

(j.)



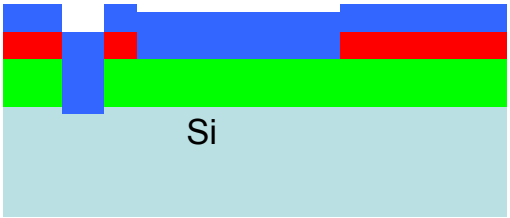
Etch Gate Pattern

(k.)



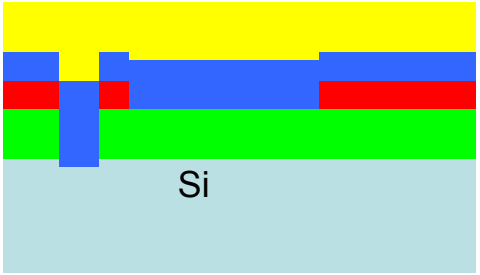
Strip Resist

(l.)



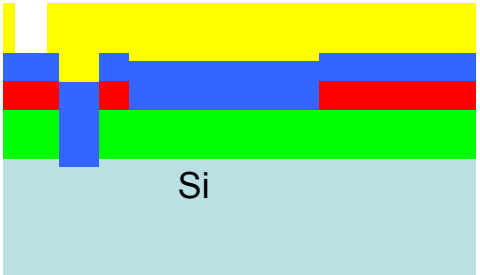
100nm PECVD SiO_2

(m.)



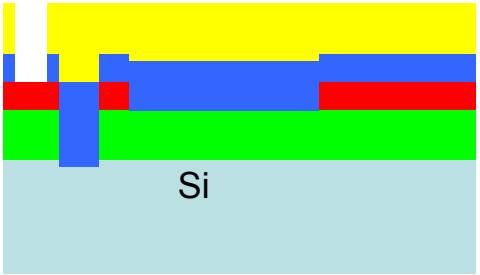
2.1um 955cm Photoresist ≈ 1.6um

(n.)



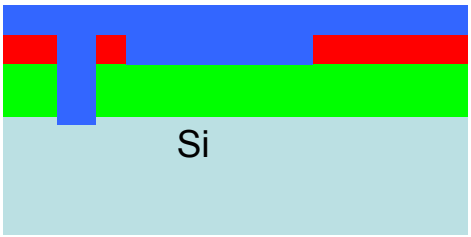
Gate Via Pattern

(o.)



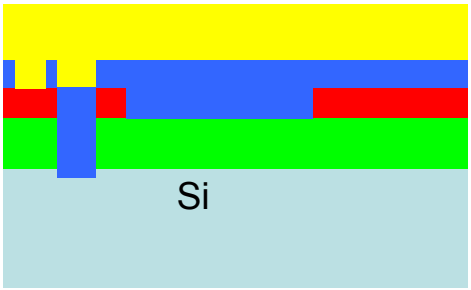
Etch Gate Via

(p.)



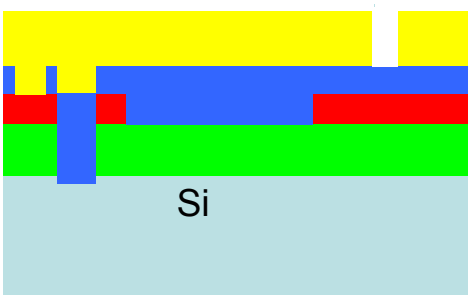
Strip Resist

(q.)



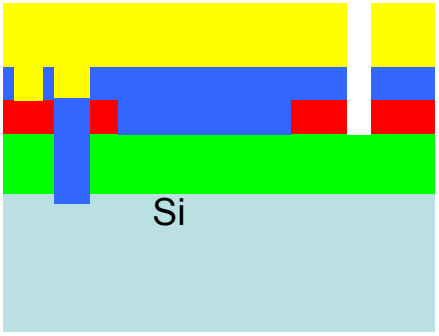
2.1um 955cm Photoresist ≈ 1.6um

(r.)



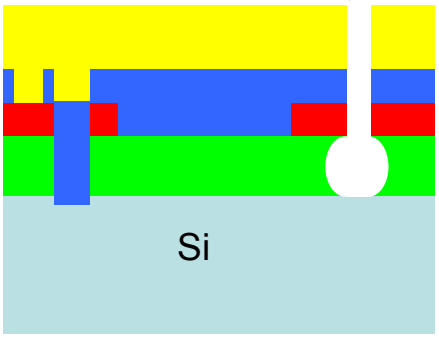
Aperture Pattern

(s.)



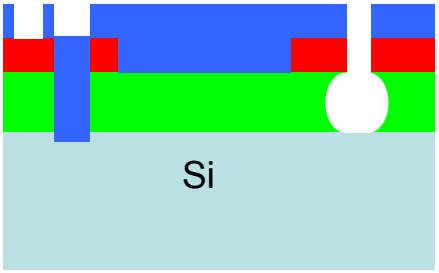
RIE Etch

(t.)



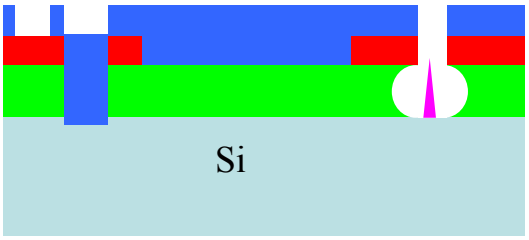
BOE 6:1 Etch

(u.)



Strip Resist

(v.)



EBID W Nanofiber

Vita

Ryan B. Rucker was born on June 2, 1982 in Knoxville, Tennessee. He graduated from Berean Christian High School, in Knoxville, Tennessee, in 2000. Ryan obtained Bachelor of Science from the University of Tennessee, Knoxville in 2005. He graduated with a major in Materials Science and Engineering. Upon completion of his undergraduate work, Ryan continued his work at the University of Tennessee by entering the graduate program in Materials Science and Engineering. He obtained a Master of Science.