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I am submitting herewith a thesis written by John Kevin Behel entitled "*A Bipolar, Semi-Gaussian Pulse Shaping Amplifier Based on Transconductance-C Continuous Time Filters for use in a High Resolution, Small Animal X-ray CT System.*" I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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A Bipolar, Semi-Gaussian Pulse Shaping Amplifier Based on Transconductance-C Continuous Time Filters for use in a High Resolution, Small Animal *X-ray* CT System

A Thesis

Presented for the

Master of Science

Degree

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Dedication

This thesis is dedicated to my wife Kris, who always gave me the support and encouragement necessary during this hectic and stressful time.

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Abstract

A new bipolar, semi-gaussian pulse shaping amplifier using transconductance-C (G_m-C) filters has been developed for use with the Oak Ridge National Laboratory (ORNL) MicroCAT small animal *x-ray* CT imaging system. The MicroCAT system employs Cadmium Zinc Telluride (CZT), a relatively new semiconductor detector material. The pulse shaping amplifier is based on a G_m-C filter topology and has adjustable gain, tunable filter time constants and quality factors as well as a differential signal path. The transconductor circuit design is also presented with emphasis placed upon the noise and linearity of the circuit. The architecture and experimental results for the prototype pulse shaping amplifier are also presented. The prototype was fabricated in the 1.2μ AMI NWELL CMOS process through the MOSIS program.

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Chapter 1 – Introduction to the MicroCAT Project

1.1 MicroCAT Overview

1.1.1 Historical Overview

The MicroCAT system is a new, high-resolution, *x-ray* computed tomography system under development at the Oak Ridge National Laboratory for use in small animal imaging. The first phase of the system was developed to screen mutagenized mice in the Oak Ridge National Laboratory Mammalian Genetics Research Facility, one of the largest experimental mouse colonies in the world. This colony was established after World War II to evaluate the effects of ionizing radiation on animals and currently houses more than 70,000 mice representing about 400 different mutant strains. In order to identify when a new mutant strain has developed from a mutagenesis experiment, an average of more than 500 mice must be screened for each observed phenotype. At present, this screening process relies largely upon time consuming behavioral analysis or physical examinations. The MircoCAT program was initiated in an effort to accelerate the screening process. The program is unique among small animal imaging programs in that its objectives are to provide high-throughput data acquisition (nominally one minute per mouse) along with high-resolution structural images of about 50 μm full-width at half max (FWHM). Current results are promising, with image spatial resolutions of 100 μm and low-resolution screening data sets (~180 projections) requiring approximately 7 minutes for acquisition [1.1].

The first phase of the MicroCAT uses a commercial multi-element CCD mammography detector for data acquisition. This CCD detector does not measure the energy of the *x-ray* once it has passed through the subject of interest, but instead integrates the absorbed *x-ray* energy charge over an interval of time. The second phase will involve the use of a new cadmium zinc telluride (CZT) detector array used in a pulse counting architecture, allowing the incorporation of the energy dependence of the *x-ray* attenuation into the acquired data. While the pulse counting system will provide poorer statistical information than an energy integration system, the additional *x-ray* photon energy information should provide greater contrast between soft tissue types and may allow for beam hardening correction [1.16-1.18]. As a part of this second phase, custom integrated electronics for the new detection system is under development.

1.1.2 Overview of X-ray CT

Before selecting *x-ray* CT for this work, several different medical imaging modalities were considered. Among those considered were magnetic resonance imaging (*MRI*), nuclear medicine including positron emission tomography (*PET*) and single photon emission tomography (*SPECT*), and *x-ray* computed tomography (*X-ray CT*). Each of these has applications where they are best suited; therefore, this was taken into consideration in determining the modality most suitable for mouse screening needs. The modality selected was *x-ray* CT due to its fast image acquisition time, low cost, differentiation between skeletal and soft tissue, and its high-resolution capabilities [1.1].

The foundation for *x-ray* CT, as presented in [1.2], is the attenuation of photon flux when x-*rays* pass through an object. When the *x-rays* are monoenergetic, this

attenuation is effectively proportional to the atomic number of the object, Z, raised to the 3.4 power. For an *x-ray* source that is not monoenergetic, undesirable effects such as beam hardening [1.3] can occur. As the attenuation is still largely related to the atomic number, these effects can be ignored for purposes of this discussion. When the object is not homogeneous, the attenuation is a space-variant function dependent on the distribution of the material along the line of the incident *x-ray* beam. If the beam is scanned linearly along the object in one plane, or parallel *x-ray* beams are used, then a 1-dimensional projection of the object at that position can be acquired (Figure 1*). Thus, each projection is a plot of the received photon flux, I, as a function of position on the detector surface (u):

$$I(u) = I_o(u)\exp\left[-\int_L \mu(x,y)dL\right] \tag{1.1}$$

$$\mu \cong constant \times \frac{Z^{3.4}}{E^{3.1}} \tag{1.2}$$

where I_o is the unattenuated *x-ray* flux, μ is the position dependent *x-ray* attenuation coefficient, E is the energy of the incident *x-ray* photon, x and y are the spatial coordinates of the object, and L is the line along which the *x-ray* flux is being integrated. The higher the material's atomic number, the more photons the material will absorb. Therefore, each projection is a function of the average atomic number of the material between the *x-ray* source and detector [1.2].

An *x-ray* CT system acquires a series of these 1-dimensional projections at various angles around the object (typically through 180°), then uses filtered back-

* All figures can be found in Appendix A.

projection [1.22] or similar software algorithms to "reconstruct" a 2-dimensional image from the projection curves. If the projection acquisition is repeated along the length of the object, or an *x-ray* tube and detector array are used, then projections can be acquired along the length of the object and the reconstructions can be combined to produce a 3-dimensional image. Several examples of reconstructed images can be seen in Figure 2 and Figure 3.

1.2 System Overview

1.2.1 System Description

A block diagram of the MicroCAT system is shown in Figure 4. The key components of the system are the (A) work station, (B) motion controllers, (C) *x-ray* tube, (D) subject bed, (E) rotating stage, and (F) CCD or CZT detector with integrated electronics. Figure 5 shows four key components of the system: the mechanical assembly and motion control, *x-ray* source and detector, integrated read-out electronics (CZT detector only), and the image processing stage. The motion control stage consists of the rotating stage, subject bed, and their motion controllers. The detector and *x-ray* tube are mounted on the rotating stage, which has computer controlled stepper motors to rotate them around the subject. Additionally, the subject bed and detector have stepper motors to allow proper positioning of the subject in the detector's field of view. A Windows NT computer system with custom software handles the motor control and data acquisition, as well as the image reconstruction using software designed by ORNL's Image Science and Machine Vision Group [1.23]. With the exception of the work station, the system is

inside an enclosure with tin-impregnated doors to protect the operator from the *x-rays*. In the phase two project, the CCD detector will be replaced with a Cadmium-Zinc Telluride (CZT) strip detector and custom designed integrated read-out electronics will be added to the system. Figure 6 shows a picture of the current MicroCAT system. In Figure 7, the CCD detector, fan beam *x-ray* tube, rotating stage, and subject bed can be seen.

1.2.2 X-ray Source and Detector

The *x-ray* source used in the MicroCAT project is an Oxford XTF5011 50kV, 50W *x-ray* tube. While the *x-rays* generated by this source are not monoenergetic, the maximum energy and flux of the *x-rays* can be controlled by setting the voltage and current in the tube. Thus, for the different detector technologies, it has been possible to experimentally determine the operating region of the source that yields the desired tissue contrast in the reconstructed image (Figure 8) [1.1].

The conventional *x-ray* CT detection method in use today involves the use of a scintillator and a photodiode. A scintillator is a material, such as bismuth germanate (BGO), that converts the kinetic energy of charged particles into visible light, which is then converted to a current by the photodiode [4]. In this mode of operation, the mean *x-ray* flux per detector pixel is measured; therefore this method is often referred to as "current mode" detection. The Phase II MicroCAT design calls for use of a "pulse counting" architecture. In this configuration, the position, and energy of each *x-ray* photon reaching the detector is recorded [1.5]. It is has been shown that such information will allow greater soft-tissue contrast [1.16-1.18].

Cadmium Zinc Telluride (CZT) is a new semiconductor detector material that has emerged in recent years with characteristics favorable for use in the direct detection of *x-rays*. Among the promising properties of CZT detectors are room temperature operation, high atomic number sufficient to absorb diagnostic *x-rays* directly without the use of a scintillator, and high counting rates [1.6,1.7]. The use of a scintillator to convert the *x-rays* to visible light when using a silicon photodiode causes a reduction in the received electrical signal of greater than an order of magnitude. This reduction occurs because only a small fraction of the *x-ray* photon's kinetic energy is actually converted into visible light. The rest is dissipated in the form of lattice vibrations or heat [1.5,1.8]. Therefore the increase in received electrical signal per *x-ray* by elimination of a scintillator will allow the energy of the individual *x-ray* photons to be measured. Since the attenuation of *x-ray* flux is related to the atomic number of the material it passes through, by measuring and sorting the received information into energy dependent images, greater contrast between different type of soft tissues can be obtained [1.16-1.18]. As this attenuation is also dependent upon the energy of the *x-ray*, the energy sorting will also provide some error correction by making the *x-ray* source look more monoenergetic.

The use of a CZT detector has been explored in two stages. The initial proof of concept experiments employed a single CZT pixel detector with a collimator (Figure 9). The images in Figure 2 were taken using this detector. The disadvantage of a single pixel detector were the long image acquisition times (~2 hours for one projection). In order to improve the acquisition time for a complete full body scan, a double sided strip detector has been proposed (Figure 10) [1.9]. This detector consists of a CZT substrate with orthogonal contract strips along the top and bottom. The detector will be biased with a

resulting electric field between the cathode (top) and the anode (bottom). An incident *x-ray* will create a mobile electron-hole pair in the substrate. A current pulse will be generated in the contacts as the electrons drift toward the anode strips and the holes drift toward the cathode strips. Custom integrated electronics will be used to detect and measure the energy in the resulting pulse. Additional electronics will also be used to determine which strips carried the resulting information, determining the position on the CZT strip detector where the *x-ray* photon was absorbed. By comparing the ratio of the absorbed energy in adjacent stripes, resolution up to half the stripe spacing will be possible.

1.2.3 Analog Signal Detection Channel Overview

As a part of the MicroCAT Phase 2 system development, integrated read-out circuitry has been developed for use with the CZT detector array. This application specific integrated circuit (ASIC) will incorporate an analog channel used for signal detection and amplification, along with the associated digital circuitry to allow pulse timing and location information. The energy of the detected pulses will also be measured. This information will be collected by a workstation and used in the reconstruction process.

The integrated analog channel consists of four components. A low noise charge sensitive preamplifier [1.10], a pulse shaping amplifier [1.11,1.12], a discriminator [1.13], and a peak-stretcher [1.14]. The preamplifier will integrate the charge pulse from the stripes and amplify it to a level well above the noise floor of the system. The pulse shaping amplifier will take the integrated voltage pulse from the preamplifier and shape it

into a bipolar, semi-gaussian voltage pulse with an amplitude proportional to the energy in the input *x-ray*. The discriminator will provide the actual thresholding used to determine if an event is of sufficient energy to have been caused by an *x-ray* photon absorption in the detector. The peak stretcher will find and hold the peak of the pulse from the pulse shaping amplifier when the discriminator signals that an *x-ray* absorption has occurred. Finally, the signals from the peak stretcher and discriminator will be processed by additional electronics to determine the energy and position information of interest. Figure 11 shows a schematic diagram of two channels of the proposed integrated electronics circuit for the double sided CZT strip detector.

1.3 Scope of Thesis

1.3.1 Overview of Thesis

The objective of this thesis project was the development of a CMOS based pulse shaping amplifier for use in the integrated electronics channel. So that the same circuitry can be used for both the cathode and anode strips, which generate opposite polarity pulses, a bipolar shaping amplifier was chosen. The generation of the desired pole-zero constellation for the pulse shaping is achieved using transconductor-capacitor (G_m-C) filters [1.15] rather than a more traditional operational amplifier design [1.19,1.20]. The transconductors were designed using a triode region transistor operating as a resistor to set the nominal transconductance. To compensate for process variations influencing the fabricated transconductance, the transconductors were designed to allow the channel resistance of this device to be adjusted. This allowed for fine-tuning of transconductance values, filter quality factor, and filter time constants. As the distortion of the shaper is

dependent upon the linearity of the individual transconductors used in the filters, the linearity of the transconductor design was evaluated. Finally, to improve noise immunity and distortion properties, the transconductors and internal shaper signal path is fully differential, with single-ended input and output. This introduced the need for common mode feedback in the design as well. The final shaper should meet the following specifications:

- Generate a bipolar shaped pulse with a peak-to-peak range of at least ±1V.
- Implement a transfer function of the following form:

$$H(s) = \frac{K \cdot s^2 \cdot \left(\frac{1}{\tau}\right)^4}{\left(s + \frac{1}{\tau}\right)^6}, \tag{1.3}$$

where K is the midband gain.

- Input pulse from the preamplifier of 1-16mV (1000 –10,000 electrons and a feedback capacitor of 100fF).
- Use transconductance-capacitor (G_m-C) filters to generate most or all of the transfer function.
- Use fully differential transconductors.
- The transconductor should be nearly linear in their region of operation.
- Adjustable forward gain in the system.
- The quality factor and time constants of the filter should be adjustable. The quality factor, Q, should be adjustable over a range sufficient to improve the output's amplitude symmetry and time for return to baseline by introducing

overshoot in the second lobe of the bipolar pulse. This range should be from $Q \cong 0.5$, for real poles and no overshoot, to $Q \cong 0.7$, with the final value for Q experimentally determined. The time constants should be adjustable to allow fine tuning of the shaping time as process variations change the actual value of the transconductor's nominal transconductance. This should be accomplished by a filter topology that uses the product of two transconductances in setting the time constant so the product can be maintained as one transconductance increases and the other decreases. As the transconductance is related to both the time constants and quality factor, the range over which the time constants can be adjusted will be dependent upon process variations and the quality factor's adjustable range. Therefore the range over which the time constant can be adjusted will be determined by these two factors.

- Noise should be sufficiently low so that the signal-to-noise ratio set by the preamplifier will not be degraded by the shaping amplifier.

This document is organized in the following manner:

Chapter 2: Background information on pulse shaping and G_m-C filters.

Chapter 3: Detailed analysis of the stability and noise of the transconductors, Gain cells, the common-mode feedback circuit, and the shaper.

Chapter 4: Simulation and layout details.

Chapter 5: Experimental results.

Chapter 6: Conclusion.

Chapter 2 - Pulse Shaping Filter Amplifier Background

2.1 Detector and Electronics Channel Overview

2.1.1 Analog Channel Overview

Custom integrated read-out circuitry has been developed for use with the CZT detector array. An overview of this circuitry, or analog channel, can be seen in Figure 12. When an incident *x-ray* is absorbed by the CZT detector, a mobile electron-hole pair is created. The electrons and holes drift toward the anode and cathode stripes respectively, generating a current pulse. This current pulse is integrated by the low-noise preamplifier and amplified above the noise floor of the system. The pulse shaping amplifier improves the signal-to-noise ratio of the system by shaping the integrated voltage pulse from the preamplifier into a bipolar, semi-gaussian pulse with an amplitude proportional to the energy in the absorbed *x-ray* photon. The discriminator provides the actual thresholding used to determine if a pulse is of sufficient energy to have been caused by an absorbed *x-ray* photon or is merely noise. When the discriminator signals that an *x-ray* photon absorption has occurred, the peak stretcher finds and holds the peak of the voltage pulse from the pulse shaping amplifier. Finally, the signals from the peak stretcher and discriminator are processed by additional electronics to determine the energy and position of the events in the CZT strip detector.

2.1.2 Detector and Preamplifier Overview

The CZT strip detector generates roughly one electron-hole pair for every 5eV of absorbed *x-ray* photon energy [2.24]. These pairs will deposit charge on the anode and cathode terminals - positive charge on the cathode terminal and negative charge on the anode terminal. As the charge collection time at these terminals is fast compared to later signal processing time, this process is often modeled as a current impulse, $Q\delta(t)$, with strength equal to the injected charge [2.1]. This charge, Q, is then injected into the next stage, the charge sensitive preamplifier (Figure 13). The charge sensitive preamplifier integrates the charge, producing a voltage step at the output proportional to the absorbed charge

$$V_{out} = \frac{Q}{C_F} \cdot u(t), \tag{2-1}$$

where C_F is the preamplifier feedback capacitor and Q is the injected charge. Thus, the preamplifier has the following transfer function

$$H(s) = \frac{1}{sC_F}, \tag{2-2}$$

and an output that is ideally a step function of amplitude Q/C_F. In reality the detector electron-hole pair charge collection time will not be instantaneous, and the preamplifier's output voltage pulse height will be influenced by parasitic capacitance. Additionally, the feedback resistor will provide a charge leakage path that causes the output pulse to decay slowly over time. In practice, this resistor is very large, so that the decay of the preamplifier's output pulse occurs very slowly. While these issues can affect the overall system performance, they are neglected here for the purpose of a first order analysis.

For the MicroCAT system, the *x-ray* photon energy absorbed by the CZT detector has an energy of approximately 20keV. As the *x-ray* tube is capable of emitting *x-ray* photons with a maximum energy of 50keV, a reasonable assumption used in the design of the integrated electronics channel was a collected detector charge corresponding to 1,000 to 10,000 electrons, or 5-50keV of absorbed energy. The charge sensitive preamplifier integrates this charge, producing an output voltage step of height Q/C_F. Thus for 1,000 to 10,000 electrons, and a feedback capacitor C_F=100fF, the input to the pulse shaping amplifier would be a step voltage with an amplitude from 1.6mV to 16mV. This is the input signal that was assumed in the initial design definition stage of the pulse shaping amplifier [2.9].

2.1.3 Filter Amplifiers Overview

The next component in the signal processing channel is the pulse "shaping" filter amplifier, which is often simply referred to as a pulse shaper. The pulse shaper has several purposes in the signal processing channel, although its primary and most important purpose is to improve the system signal-to-noise ratio. Additionally, the pulse shaper should also be designed to reduce pulse pile up and ballistic deficit (detailed later), often conflicting design goals [2.3]. This section will outline some of the important pulse shaper design issues; for more detailed information beyond that presented here, the reader is referred to references [2.2], [2.3] and [2.4].

As outlined in [2.5], noise introduced into a nuclear spectroscopy system causes random fluctuations in the amplitude information carried by the pulses from a radiation detector (Figure 14). These random fluctuations degrade the system performance and

energy resolution. The primary noise contributors in a radiation detection system are the detector and the preamplifier. Noise introduced by these stages receives the same total amplification through the system as the signal of interest; whereas noise introduced later in the system receives much less gain than the signal of interest. To a first order analysis, the purpose of the pulse shaping filter amplifier is to band-limit this noise while allowing the desired signal to pass through with maximum amplification.

The primary purpose of the pulse shaper is to provide a signal-to-noise ratio (SNR) as high as possible. While additional system design constraints often force trade-offs to be made between SNR, system cost, counting rate, etc [2.3, 2.5], an important figure of merit in a pulse shaping system is how the system's SNR ratio compares to the optimum attainable SNR. A extensive amount of literature exists on this subject ([2.5], [2.6], [2.18], [2.19], [2.20]) in which it has been shown that the best SNR can be attained by shaping the signal pulses into the shape of an infinite cusp. As an infinitely long pulse width is impossible to yield, practical systems must limit themselves to pulse shapes that are physically realizable. Several examples of different pulse shapes and the resulting SNR relative to the infinite cusp can be seen in Figure 15.

As will be illustrated in the following example, the time constant used in the pulse shaper can have a large impact upon the output signal-to-noise ratio. For a given detector-preamplifier-shaper system, there is an optimum shaper time constant, τ_{opt}, that will give a maximum total output signal-to-noise ratio. Consider the detector and charge sensitive preamplifier shown in Figure 19 with the series and parallel noise generators. The series noise voltage spectral density, defined here as ENV_{ins}^2 (V^2/Hz), is associated with the

preamplifier's equivalent input noise voltage. This series noise also includes the flicker noise associated with the preamplifier's input FET. For the case of a MOSFET input preamplifier, the preamplifier's noise current will be negligibly small. Thus, the parallel noise current spectral density, ENI_{inp}^2 (A^2/Hz), is primarily associated with the current noise spectral density from the semiconductor detector [2.6, 2.22].

Considering first the equivalent input noise voltage generator (Figure 20), it can be shown that the output noise voltage spectral density, $ENV_{os,w}^2$ due to a white noise $ENV_{ins,w}^2$ is

$$ENV_{os,w}^2 = ENV_{ins,w}^2 \cdot \left| \frac{Z_f + Z_d}{Z_d} \right|^2 \text{ V}^2\text{/Hz.} \tag{2-3}$$

Letting $R_f \rightarrow \infty$, and substituting $Z_d = \frac{1}{sC_d}$ and $Z_f = \frac{1}{sC_f}$ results in

$$ENV_{os,w}^2 = ENV_{ins,w}^2 \cdot \left(\frac{C_f + C_d}{C_f} \right)^2 \text{ V}^2\text{/Hz,} \tag{2-4}$$

which shows that for a white noise ENV_{ins}^2 the output noise voltage spectral density is also white. For the case of flicker noise

$$ENV_{ins,f}^2 = \frac{K}{f} \qquad K \text{ is a constant} \tag{2-5}$$

$$ENV_{o,f}^2 = \frac{K}{f} \cdot \left(\frac{C_f + C_d}{C_f} \right)^2 \text{ V}^2\text{/Hz,} \tag{2-6}$$

so the output noise voltage spectral density due to flicker noise retains its $\frac{1}{f}$ relationship. Similarly the mean squared output noise voltage due to the parallel noise current (Figure 21), ENI_{inp}^2, can be shown to be

$$ENV_{op}^2 = ENI_{inp}^2 \cdot \left|\frac{1}{sC_f}\right|^2 = ENI_{in}^2 \cdot \left(\frac{1}{\omega^2 C_f^2}\right) \text{ V}^2\text{/Hz.} \qquad (2\text{-}7)$$

Equation (2-7) shows that the output noise voltage spectral density due to the parallel noise current has a $\frac{1}{f^2}$ relationship.

Typical plots of the noise voltage spectral density at the output of the preamplifier from the white series noise voltage, the flicker series noise voltage, and the parallel noise current can be seen in Figure 22. The output mean squared noise voltage for each component can be obtained by integrating the noise voltage spectral density over the frequency range zero to infinity. It can be seen that the flicker series noise will contribute the same amount of noise voltage to the total in each frequency decade, the white series noise voltage will contribute a larger component in each decade as the frequency increases, and the parallel noise current's contribution will decrease as the frequency increases. These observations suggest the minimum noise is achieved with a filter function centered around the frequency where the white series output noise component is approximately equal to the parallel output noise component. This will also give the maximum SNR if the shaper's output pulse amplitude is independent of τ - as is the case for the CR-RC shaper. The optimum shaper time constant for minimum total output noise voltage will depend on the method of pulse shaping chosen [2.21]. As an illustration of this, the total mean squared output noise voltage as a function of τ for a CR-RC pulse shaper (Figure 23) can be shown to be

$$\overline{v_o^2}(\tau) = ENV_{ins,w}^2 \cdot \left(\frac{C_f + C_d}{C_f}\right)^2 \cdot \left(\frac{\pi}{4 \cdot \tau}\right) + \frac{ENI_{inp}^2}{C_f^2} \cdot \left(\frac{\pi \cdot \tau}{4}\right) + C \text{ V}^2, \qquad (2\text{-}8)$$

where the constant C comes from the flicker noise. The optimum time constant, τ_{opt}, for the system can be found by finding the τ where $\overline{v_o^2}$ is at a minimum. Solving for this gives

$$\tau_{opt} = \frac{ENV_{ins,w}}{ENI_{inp}} \cdot \left(C_d + C_f\right). \tag{2-9}$$

Putting (2-9) into (2-8) gives the minimum value of $\overline{v_o^2}$:

$$\overline{v_o^2}\left(\tau_{opt}\right) = \frac{\pi}{2} \cdot \frac{ENV_{ins,w} \cdot ENI_{inp} \cdot \left(C_d + C_f\right)}{C_f^2} \text{ V}^2. \tag{2-10}$$

Figure 24 shows an example graph of the total mean-squared output noise voltage vs. τ, illustrating the location of an optimum shaper time constant, τ_{opt}. Thus it can be seen that choosing a shaper time constant greater or less than τ_{opt} to meet pulse pileup or ballistic deficit design considerations will result in an increase in the total output noise voltage.

One other key issue that affects the pulse shaper's complexity and desired pulse shape is baseline shift. Baseline shift occurs in an AC coupled amplifier due to the fact that a capacitor will not transmit any DC signal component, therefore the mean output voltage of a transmitted pulse must be zero. Consider the case of a CR differentiator stage. If a narrow pulse is transmitted through a CR stage with relatively little distortion (corresponding to a large RC time constant) this pulse must be followed by a long, shallow undershoot of equal area in order to maintain a zero mean output voltage (Figure 16). Additionally, this undershoot is rate dependent, with a minimum peak $nTV_{pk\text{-}pk}$ volts below the baseline (where n is the pulse rate and T is the pulse period). If additional pulses occur during this undershoot period, the measured pulse amplitude will be in error by this amount [2.7]. This problem is frequently overcome through the use of a "baseline

restorer" to return the output pulse level to the baseline significantly faster than the mean event rate. Another way to overcome this problem without the additional "baseline restorer" is to use a pulse shape that has no DC component. Such a pulse shape has, ideally, equal areas both above and below the baseline and is typically referred to as a bipolar pulse (Figure 17). While the use of a bipolar pulse reduces system complexity by eliminating the need for a baseline restorer, it does entail a reduction in SNR over the unipolar shaping methods (Figure 15).

Another important issue in a nuclear spectroscopy system is the accuracy of the measurement of the shaped pulse's height. If the pulse's peak dwell time is too short, later measuring circuitry may not accurately record the actual pulse height. Such a condition occurs for the shapes in Figure 15 with a sharp, short peak. In order to minimize this problem, pulse shapes with a longer peak dwell time such as a semi-gaussian, are frequently used, where the improved measurement accuracy offsets the reduction from the optimum pulse shape SNR. A semi-gaussian pulse shape, like the $CR\text{-}RC^4$ in Figure 15, can be realized by one stage of CR differentiation and several stages of RC integration. As the number of integrations increases, the pulse shape begins to more closely approximate a true gaussian shape. By adding another stage of differentiation, $CR^2\text{-}RC^4$ in Figure 15, a bipolar semi-gaussian pulse shape can be realized. While this pulse shape has a lower SNR than the unipolar semi-gaussian, it does eliminate the need for a "baseline restorer."

Another part of the amplitude measurement problem occurs due to the relationship between the detector charge collection time and the shaped pulse's time-to-peak. Ideally, the signal from the pulse shaper should have amplitude proportional to the

energy of the absorbed *x-ray* photon. If the integrating preamplifier collects all of the charge produced in the detector by the x-ray absorption, then there is no "ballistic deficit" in the peak pulse amplitude. Thus, the shaped pulse's time-to-peak should be longer than the longest detector charge collection time. If it is not, there will be a fluctuating "ballistic deficit" which will cause an uncertainty in the energy measured [2.8].

The final key performance issue relates to the frequency of events from the preamplifier. If the mean time between events is less than the pulse shaping time, successive pulses can occur on top of each other (Figure 18), resulting in measured pulse amplitudes that are inaccurate. In order to prevent this from happening, the pulse shaping time should be short - a condition that often conflicts with minimizing ballistic deficit and maximizing SNR.

All of these issues represent trade-offs that must be made when choosing a topology for the pulse shaping amplifier. High signal-to-noise ratios argue for a pulse shape that closely resembles the infinite cusp, and ballistic deficit reduction requires that the charge collection time of the detector be shorter than the shaped output pulse peaking time. Finally, pulse pileup argues for short shaping times and pulse shapes that quickly return to the baseline. All of these issues should be considered in the design of a pulse shaping amplifier, although experimental measurements are often used to help determine the desired shaping time for a given detector, preamplifier and pulse shaper.

2.2 Initial Filter Amplifier Decisions for Implementation

2.2.1 Decision to Use Bipolar Filtering

In order to allow the same electronics to be used for both sides of the CZT strip detector, the integrated electronics had to be capable of processing pulses of either polarity. This requirement introduced a few additional design issues into the analog processing channel. First, the preamplifier was designed to accept pulses of either polarity [2.9]. The design of the later electronics was dependent upon the pulse shape implemented by the pulse shaper. If a unipolar pulse shape was implemented, the pulse shaper would need to have a baseline restorer capable of dealing with pulses of either polarity. Additionally, the peak-stretcher and discriminator would also need to be capable of responding to pulses of either polarity. One way to minimize the additional complexity introduced by this requirement is to trade some pulse shape signal-to-noise ratio for a reduction in overall system complexity. This can be accomplished by differentiating the unipolar pulse to produce a bipolar output pulse shape (Figure 17). With a bipolar pulse shape, the peak-stretcher and discriminator only needed to respond to the positive pulse lobes. Depending upon the polarity of the preamplifier output pulse, this positive lobe would be located either in the first or the second half of the resulting bipolar pulse period. Thus, the need for dual polarity discriminator and peak stretcher circuits and a complicated baseline restorer was eliminated.

Finally, it is important to note that since the unipolar pulse shape has a long tail, the bipolar pulse resulting from the differentiation also has a long tail. This results in a relatively long time for the second lobe to return to the baseline. As the total area under

each lobe must still be the same, this "tail" also reduces the amplitude of the second lobe [2.7]. This lack of symmetry between the two lobes will result in measurement errors if the second lobe is the positive going lobe. Additionally, a long "tail" increases the channel "dead time", in which a new pulse cannot be processed. It is possible to reduce this "tail" time and improve pulse symmetry by making some of the transfer function poles complex. This is the same thing as adjusting the quality factor, Q, of a filter. This results in a quicker return to baseline, and hence, a larger second lobe amplitude to maintain the same area under the two lobes. This also causes overshoot as the signal returns to the baseline, so it is important that this overshoot is below the discriminator's threshold – otherwise it will be mistaken for another signal pulse.

2.2.2 Pulse Shaper Design Specifications

In order to meet the bidirectionality requirements for the shaper, a bipolar pulse shape was selected for the design. The desired shaping time constants and pulse width were determined from experimental measurements using a single-pixel CZT detector, an ORTEC 142A low-noise preamplifier, and an ORTEC 571 pulse shaper. The pulse shaper's time constants were to be between 100nsec and 125nsec, and the shaped pulse's return to baseline was to occur within 2μsec [2.24]. An adjustable quality factor was desired to improve the bipolar pulse amplitude symmetry and to reduce the complete pulse shaping time. Finally, an adjustable gain was desired to provide greater control over the peak of the shaper's output pulse.

2.2.3 Shaper Transfer Function and Physical Topology

Given the requirements for a bipolar pulse with variable gain and quality factors and a maximum pulse width of 2μsec, a semi-gaussian bipolar shaper topology was selected. As mentioned earlier, a bipolar semi-gaussian pulse shape can be realized using two CR differentiating stages and n-stages of integration, with four typically being sufficient to achieve a reasonable semi-gaussian pulse shape [2.10]. The resulting transfer function desired for implementation is then

$$H(s) = \frac{K \cdot s^2 \cdot \left(\frac{1}{\tau_b}\right)^4}{\left(s + \frac{1}{\tau_a}\right)^2 \left(s + \frac{1}{\tau_b}\right)^4}, \tag{2-11}$$

where K is an adjustable forward gain, τ_b is the adjustable time constant, and τ_a is the time constant for the CR stages used to AC couple the input and output of the pulse shaper.

Since the CR stages are typically implemented using passive components, the active portion of the desired transfer function consists of two low-pass filters, each with a transfer function of

$$H(s) = \frac{\left(\frac{1}{\tau_b}\right)^2}{\left(s + \frac{1}{\tau_b}\right)^2}, \tag{2-12}$$

and some adjustable forward gain, K, implemented either as a part of the low-pass filters or using separate gain devices. Thus, the major circuit blocks to be implemented are two low-pass filters with gain and two AC coupling CR differentiator stages.

Candidate filter topologies for the low-pass filter design include Sallen-Key and G_m-C based approaches. While the Sallen-Key low-pass filter offers ease of implementation, it does not offer readily adjustable gains, filter time constants, and quality factors. The G_m-C topology, on the other hand, does provide adjustable gains, time constants, and quality factors; for this reason, it was decided to implement the low-pass filters using G_m-C based filters. As can be seen in Figure 25, the selected shaper topology consists of two gain blocks and two low-pass G_m-C filter biquads, AC coupled at the input and output by the CR stages. Additionally, as a fully differential signal path was used in the intermediate stages, a differential-to-single-ended converter was included before the final CR stage. Finally, it should be noted that the gain blocks were also implemented using transconductors.

2.3 G_m-C Filter Background

2.3.1 Theory of Operation

A G_m-C filter is a type of continuous-time filter employing a transconductor-based integrator. The literature contains a great deal of information on G_m-C feedback topologies for implementing different filter transfer functions, as well as filter synthesis methods such as the signal-flow graph. [2.11, 2.14]. One of the more common feedback arrangements used in G_m-C filters is a second-order, or biquad, filter [2.11- 2.15], which may be used to implement low-pass, bandpass, and high pass filters. Biquads are discussed in greater detail in Section 2.4.

The discussion below closely follows information presented in [2.11-2.12]. A transconductor is a circuit that produces an output current related to the input voltage by

$$I_{out} = G_m \cdot V_{in}, \tag{2-13}$$

where G_m is the transconductance of the circuit. When the output current is applied to an integrating capacitor (Figure 26) the output voltage is

$$V_{out} = \frac{I_{out}}{s \cdot C_{int}} = \frac{G_m \cdot V_{in}}{s \cdot C_{int}} = \frac{\omega_o}{s} V_{in}; \qquad \omega_o = \frac{G_m}{C_{int}}, \tag{2-14}$$

where ω_o is the integrator unity gain frequency. Therefore, the output voltage is the integration of the input differential voltage multiplied by the integrator's unity gain frequency, ω_o.

In order to improve the filter's noise immunity and distortion properties, fully differential transconductors are often used [2.23]. In a fully differential transconductor there are two outputs - one current source output and one current sink output. The fully differential integrator is similar to its single-ended counterpart, although there are two different ways it can be implemented. Figure 27a shows a fully differential integrator using a single capacitor connected between the transconductor outputs. This offers the advantage of reduced overall capacitance over the second method (Figure 27b), in which the capacitors are connected to AC ground.

It is important to note that while the total capacitance is reduced, floating capacitors implemented in CMOS processes tend to have rather significant back plate capacitances between the bottom plate and the substrate. These parasitics add unevenly to the capacitance at the output of the differential integrator. In order to balance and minimize this parasitic contribution, the capacitor can be split in two and connected so that the back plate capacitances add evenly to both outputs. This results in a total effective capacitance at the output of

$$C_{int} = C + \frac{C_p}{2} \quad , \tag{2-15}$$

where C_p is the parasitic contribution from the back plate. The output signal is then

$$V_{out} = \frac{G_m \cdot V_{in}}{s \cdot \left(C + \frac{C_p}{2}\right)}; \quad \omega_o = \frac{G_m}{\left(C + \frac{C_p}{2}\right)}. \tag{2-16}$$

2.3.2 Transconductors

There are two principle methods used in realizing CMOS transconductors. The first relies on the properties of transistors operating in the linear, or triode, region of operation. Triode region transconductors offer the advantage of high linearity although they are often slower than the second type of transconductor based on active region transistors. This second type relies upon cancellation of the nonlinear terms in the square law model of MOS transistors. As the square law model is not very accurate, these transconductors typically have poorer linearity than triode-based transconductors. For this reason, the transconductor developed for use in the pulse shaper was based upon triode region designs [2.11].

A triode-region transconductor uses a transistor operating in the triode region to set the circuit's transconductance, or G_m. Consider the "Shichman-Hodges", or SPICE Level 1, MOSFET modeling equation for an n-channel transistor operating in the triode region [2.16]

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_m) V_{DS} - \frac{V_{DS}^2}{2} \right] \text{A}. \tag{2-17}$$

The transistor remains in the triode region as long as

$$V_{DS} < V_{eff} \text{ where } V_{eff} = V_{GS} - V_{tn}. \tag{2-18}$$

Similarly, for a p-channel transistor

$$I_D = \mu_p C_{ox} \frac{W}{L}\left[(V_{SG} + V_{tp})V_{SD} - \frac{V_{SD}^2}{2}\right] \text{A}, \tag{2-19}$$

which remains in the triode region as long as

$$V_{SD} < V_{eff} \text{ where } V_{eff} = V_{SG} + V_{tp}. \tag{2-20}$$

For small drain-source voltages, V_{DS}, the V_{DS}^2 term in equations (2-17) and (2-19) can be ignored, which leaves a transistor drain current that is approximately linear with respect to the voltage across the drain and source terminals. Differentiating equation (2-19) yields the approximate transistor channel conductance in siemens

$$g_{ds} = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{r_{ds}} = \mu_p C_{ox} \frac{W}{L}(V_{SG} + V_{tp}), \tag{2-21}$$

where g_{ds} is linearly controlled by V_{SG}.

Consider the simplified triode region transconductor in Figure 28 based on a design presented in [2.11] and [2.17]. The p-channel transistor M_{11} will operate in the triode region if its gate is connected to V_{SS} and $V_{SD} < V_{eff}$. M_{11} then acts as a resistor between nodes (3) and (4). Assuming the g_m of transistors M_1 and M_2 is infinite, then the entire input differential signal will appear across the resistor formed by M_{11}, causing current to flow through M_{11} from the source (node 3) to the drain (node 4). The current in the drain of M_3 will then be $I1$-$I2$-i_o, while the current in the drain of M_4 will be $I1$-$I2$+i_o. Assuming ideal transistors again, the output current will then be $+i_o$ (node 8) and $-i_o$ (node 7), or a total differential output current of simply i_o. Thus, the small signal transconductance is

$$G_m = \frac{\partial I_o}{\partial V_{diff}} = \mu_p C_{ox} \left(\frac{W}{L}\right)_{11} \left(V_{sg11} + V_{tp}\right) \text{ S}, \tag{2-22}$$

where the designation G_m will be used when referring to the transconductance of a transconductor circuit.

From the circuit in Figure 28, it is obvious that there will be parasitics that will impact the transconductor design. Figure 29 shows a fully differential transconductor, (a), and the small signal model including parasitics, (b). From this it can be seen that the input and output parasitics could introduce additional poles that could become significant at high frequencies. For a MOS based transconductor, the input impedance, R_{in}, goes to infinity, and the input parasitic capacitance can be ignored for now; however, R_{out} and C_{out} will not be negligible and should be taken into consideration when designing the G_m-C filter. As C_{out} will add to the integrating capacitor at the output, it should either be kept much smaller than C_{int} or used in calculating the total C_{int} at the output. Additionally, as a transconductor sources current, the output impedance, R_{out}, should be large.

Another issue of concern in the transconductor design is the input and output voltage dynamic range. For a triode region transconductor, the input dynamic range is usually limited by how deep in the linear region the designer wants the triode region transistor to be. When the input signal increases, the transistor begins to leave the linear region of operation as V_{DS} approaches V_{eff}. Additionally, because of the V_{DS}^2 term (equation 2-19), the transistor drain current becomes increasingly nonlinear as V_{DS} increases. These effects can be reduced by keeping a large V_{eff} (i.e. a large V_{GS}) on the triode region device. Thus, the input dynamic range is limited more by how nonlinear the designer allows the I_o vs. V_{diff} relationship to become than by V_{eff} itself.

The desired output voltage dynamic range is often harder to quantify. In applications where the differential output voltage is not expected to be very large, simple transconductor output stages can often be used. For applications where the differential output voltage is expected to be larger, more complicated output stages are desirable to keep the transconductor output impedance high over the full signal range. Experience has shown that a good guideline, particularly when using transconductor gain stages, is to make the output signal dynamic range and output impedance large over the same range the designer considers the triode region transconductor appropriately linear. This will ensure that a transconductor's output can provide a "full" range signal to the next transconductor while still maintaining a large output impedance.

Finally, there are a few other issues of concern in designing transconductors. For a fully differential transconductor design it becomes necessary to include a common mode feedback circuit to allow control over the common mode output voltage level. Such a circuit can be used to adjust the gate voltage of transistors M_5 and M_6 to keep the output at the desired common mode voltage level. Two additional issues of concern are bias currents sufficient to provide the transconductor's output current over the desired range of input differential voltage, and internal dominant poles that are at least an order of magnitude higher than the ω_o of the filters.

2.3.3 Transconductor Based Gain Block

When the outputs of a transconductor are tied to its inputs as shown in Figure 30, the circuit acts as a resistor of value $\frac{1}{G_m}$. This can be easily seen by noting that the

voltage across the shorted input-output nodes is equal to the current supplied by the circuit, I_o, divided by G_m. Reversing the connections will simulate a negative resistance [2.13]. If a transconductor is followed by another connected in this manner (Figure 31), then the gain of the circuit is

$$G = \frac{V_o}{V_{in}} = \frac{G_{m1}}{G_{m2}}. \tag{2-23}$$

As mentioned in section 2.3.2, the value of G_m is proportional to the size of the triode region transistor. By selecting appropriate ratios for the triode region transistors, a nominal value of gain for the gain block can be set. The gain can then be increased or decreased by adjusting the gate voltages of these two transistors. Additionally, since the transconductors are differential, the gain is also differential. This means the noise and distortion reducing properties of a fully differential channel are provided while the gain helps to raise the signal level even further above the noise present later in the circuit. These transconductor based gain blocks were used to provide the adjustable gain in the pulse shaper.

2.4 Biquad Filter Networks

2.4.1 Introduction and Background

One of the more popular methods of implementing G_m-C based filters is through the use of the second-order, or biquad, filter. Transconductor biquads are based upon the G_m-C integrator and resistor connected transconductors. As will be seen, these filter biquads can offer several advantages over first order filters by providing greater control over the undamped natural frequency, ω_o, and the filter quality factor, Q. Higher order

transfer functions can then be easily implemented by connecting several biquads in series [2.11,2.13].

2.4.2 Low-pass Filter Biquad

As mentioned in section 2.2.2, the pulse shaper must have a transfer function of the form

$$H(s) = \frac{K \cdot s^2 \cdot \left(\frac{1}{\tau_b}\right)^4}{\left(s + \frac{1}{\tau_a}\right)^2 \left(s + \frac{1}{\tau_b}\right)^4}. \tag{2-24}$$

The CR stages at the input and output provide the zeros and two of the poles, while two adjustable gain stages provide the gain K. Therefore, each of the two low-pass filter biquads must implement the following transfer function:

$$H(s) = \frac{\left(\frac{1}{\tau_b}\right)^2}{\left(s + \frac{1}{\tau_b}\right)^2}. \tag{2-25}$$

One biquad network for implementing this transfer function is shown in Figure 32. From a Nodal analysis, it may be shown that the biquad transfer function, assuming ideal transconductors with no parasitics, is

$$H_{LP}(s) = \frac{\omega_o^2}{s^2 + \frac{s \cdot \omega_o}{Q} + \omega_o^2} = \frac{\frac{G_{m1} \cdot G_{m2}}{C_1 \cdot C_2}}{s^2 + \frac{s \cdot G_{m2}}{C_2} + \frac{G_{m1} \cdot G_{m2}}{C_1 \cdot C_2}}, \tag{2-26}$$

where

$$Q = \sqrt{\frac{G_{m1} \cdot C_2}{G_{m2} \cdot C_1}} \qquad \omega_o = \sqrt{\frac{G_{m1} \cdot G_{m2}}{C_1 \cdot C_2}} . \tag{2-27}$$

From the above, it can be seen that the undamped natural frequency of the filter, ω_o, can be adjusted by changing the product of the transconductor G_m's (assuming fixed capacitance) while the quality factor, Q, can be controlled by changing the ratio of the G_m's. Thus, with this biquad network, it is possible to tune the filter's quality factor while maintaining a constant ω_o (Figure 33). Finally, the poles of the transfer function can be made real by setting Q to 0.5,

$$H_{LP}(s) = \frac{\left(\frac{1}{\tau}\right)^2}{\left(s + \frac{1}{\tau}\right)^2} \qquad \tau = \sqrt{\frac{C_1 \cdot C_2}{G_{m1} \cdot G_{m2}}}, \tag{2-28}$$

where $G_{m1} = G_{m2}$ and $C_1 = 4C_2$.

Thus, this biquad implements the desired transfer function. Additionally, by increasing Q above 0.5, the second lobe of the bipolar pulse will have some overshoot in the transient response, providing the desired faster return to baseline and improved pulse symmetry. Finally, by adjusting the value of the G_m product, ω_o can be maintained at a constant value while Q is increased.

2.4.3 Non-ideal Effects in the Low-pass Biquad

As mentioned in section 2.3.2, a real transconductor circuit has parasitics that must be considered when designing G_m-C filters (Figure 34). For a circuit using MOSFET input transistors, R_{in} can be considered infinite; meaning the dominant parasitic at the input will be the stray capacitance, C_{in}. Similarly, stray capacitance, C_{out}, will also exist at

the output nodes. Both of these stray capacitances will add to the filter capacitors C_1 and C_2 in the biquad (Figure 35). As a result, these parasitic capacitances should be considered when selecting the values of C_1 and C_2. This is particularly important when the sum of these parasitics capacitances will contribute a large percentage of the total values of C_1 and C_2, as this could cause an undesirably large shift in ω_0 and Q [2.13].

As an illustration of this, consider the biquad shown in Figure 35 with the associated transconductor parasitics. Since the circuit is fully differential, it is possible to look at a half-mode equivalent of the circuit for analytical purposes. The validity of this approach can be seen by considering the equivalent circuit for a fully differential transconductor (Figure 36). An internal node between the two outputs is treated as AC ground, with the result being that the half-mode circuit's parasitic resistances are halved while the parasitic capacitance is doubled over that of the fully differential circuit.

Using the half-mode circuit to analyze the biquad network yields the biquad equivalent circuit of Figure 37. Using this model, the transfer function becomes

$$\frac{V_{od}}{V_{id}} = \frac{4G_{m1}G_{m2}R_{out}^2}{(C_aC_bR_{out}^2)s^2 + (4C_aR_{out} + 4R_{out}C_b + 2C_aG_{m2}R_{out}^2)s + (4G_{m2}G_{m1}R_{out}^2 + 8G_{m2}R_{out} + 16)} \quad (2\text{-}29)$$

where the relation $G_{m1}=G_{m4}$ and $G_{m2}=G_{m3}$ was used to maintain a form similar to the ideal transfer function. Thus, a finite output impedance will result in a transfer function that deviates from the ideal one presented earlier. This illustrates the importance of designing the transconductor with a large output impedance. As R_{out} approaches infinity, the transfer function takes on the form of

$$\frac{V_{od}}{V_{id}} = \frac{4 \cdot G_{m1} \cdot G_{m2}}{\left(s^2 \cdot C_a \cdot C_b + 2 \cdot C_a \cdot G_{m2} \cdot s + 4 \cdot G_{m2} \cdot G_{m1}\right)} \quad (2\text{-}30)$$

Substituting for C_a and C_b yields

$$\frac{V_{od}}{V_{id}} = \frac{G_{m1}G_{m2}}{(C_1^2 + 4C_1C_{out} + 3C_1C_{in} + 4C_{out}^2 + 6C_{out}C_{in} + 2C_{in}^2)s^2 + (C_{in} + C_1 + 2C_{out})G_{m2}s + G_{m1}G_{m2}}, \quad (2\text{-}31)$$

where

$$C_a = 2 \cdot C_1 + 4 \cdot C_{out} + 2 \cdot C_{in} \quad \text{and} \quad C_b = 2 \cdot C_1 + 4 \cdot C_{out} + 4 \cdot C_{in}. \quad (2\text{-}32)$$

This illustrates that if R_o is made sufficiently large, the dominant parasitic becomes the stray input and output capacitances of the transconductor. Thus, if R_{out} is large and the parasitic capacitances are either negligible compared to C_1 and C_2, or are included in the calculation of the total desired filter capacitance, then the resulting biquad transfer function will approach the ideal function (equation 2-26).

Chapter 3 - Theory of Design and Analysis

3.1 Implemented Pulse Shaping Amplifier

The pulse shaping amplifier was implemented using 100-125nsec transfer function time constants. This choice was based upon measured results using a single pixel CZT detector, an ORTEC 142 preamp, and an ORTEC 571 pulse shaping amplifier (Table 1). This choice yields a simulated complete pulse shaping time (return to baseline after the second lobe) of ~1.5μsec. The time to zero crossing (which corresponds to the time-to-peak of a unipolar semi-gaussian shaper), was simulated to be approximately 700nsec. As can be seen in Table 1, this time constant was less than the optimum time constant measured using a capacitance equal to the CZT pixel detector capacitance and the ORTEC 571 pulse shaping amplifier (a shaper that implements a similar transfer function) [3.11]. As shown in section 2.1.3, this smaller τ will result in a smaller signal-to-noise ratio than for the case of $\tau=\tau_{opt}$. However, experimental measurement showed that time constants in the 100-125nsec range provided good results in light of the considerations of pulse pile up and ballistic deficit [3.1].

3.1.1 Overview of Shaper implementation

Figure 38 shows a block diagram of the final pulse shaping filter amplifier. Two AC coupling, CR differentiator stages were used to implement the transfer function zeros and the two non-adjustable poles. Two gain stages were used to provide the desired

* All tables can be found in Appendix B.

adjustable gain. These were positioned before each G_m-C biquad to minimize the noise contribution from the active transconductors in later stages (more on this in section 3.3). The differential-to-single-ended conversion was accomplished using two RHIC4B [3.2] operational amplifiers as buffers and a third op amp to perform the conversion. This multiple op amp conversion was used to minimize distortion and common-mode noise during the development and measurement process. In future implementations, it would be more efficient to use a single output of the last biquad and one op amp acting as a gain-buffer instead of the three op-amp differential to single-ended conversion system. Finally, a RHIC4B output driver op amp was used to buffer and drive the signal off the prototype chip during testing. This device would not be necessary in a complete, integrated analog channel.

3.2 Transconductor Design Theory and Development

3.2.1 Design Overview

The circuit used to implement the transconductor can be seen Figure 39. The circuit was partially based on a design by Kwan presented in [3.3]. A single triode region transistor (M_5) acting as a resistor is used to establish the G_m of the transconductor - where G_m will approach the transistor's g_{ds}. As the g_{ds} of a triode region transistor is proportional to the mobility (equation 2-12), the lower mobility of a PMOS device will result in a lower g_{ds}. This will result in a lower G_m, which will reduce the size of the capacitance necessary in the filter biquads.

The current sources I_1 and I_2 provide biasing for the circuit, where $I_1 > I_2$. Current I_1 flows in transistors M_{13} and M_{14}, current I_2 in M_1, M_2, M_{10}, and M_{12}, and the difference

in the output branches. Transistors M_{16}-M_{23} are used to provide bias voltages at the gates of M_{24}-M_{27}. When a positive input voltage is applied to the gate of M_1, the current $|I_{D1}|$ will decrease below I_2 due to the lower V_{SG1}. This will result in a decrease in the voltage at the gate of transistor M_3 as the drain current I_{D10} equals I_2. This lowered gate voltage will result in an increase in the voltage at node 3, increasing V_{SG1} and returning $|I_{D1}|$ back to I_2. Correspondingly, as a voltage is developed across M_5, a small signal current i_o will flow through M_5, resulting in $I_{D3}=I_1-I_2-i_o$ and $I_{D4}=I_1-I_2+i_o$. Thus, the two local feedback loops of M_1, M_3 and M_2,M_4 act to ensure that the small signal current i_o flows in transistors M_3 and M_4, and in the corresponding output transistors M_6 and M_7, while keeping M_1 and M_2 properly biased.

An examination of one of the local feedback loops (Figure 40) using the methods outlined in [3.4] shows that the loop transmission is

$$T = \frac{-44.5 \cdot (1 - \frac{jf}{3.7GHz})}{(1 + \frac{jf}{4MHz}) \cdot (1 + \frac{jf}{338MHz})}, \qquad (3\text{-}1)$$

where the dominant pole comes from the large impedance at node 5. Equation (3-1) shows that the loop transmission effectively has a single pole response, with phase margin (PM) ≅ 67° and gain margin (GM) ≅ 25dB. Figure 41 and Figure 42 show Bode plots of the predicted behavior of the local feedback loop transmission $T(f)$. SPICE plots of $T(f)$ are shown in Figure 43 and Figure 44.

As an additional observation, Blackman's theorem shows that the impedance looking into node 3 should be [3.5]

$$R_3^{cl} = \frac{R_3^{ol}}{(1+|T_{oc}|)}\Omega. \tag{3-2}$$

Using the DC operating point values included in Table 20, it can be shown that

$$R_3^{ol} = r_{ds13} \parallel r_{ds3} \parallel R_{s1} \parallel r_{ds5} \cong 17.1k\Omega \tag{3-3}$$

$$R_{s1} = \frac{\left(1+\frac{r_{ds10}}{r_{ds1}}\right)}{g_{m1}+g_{mb1}+g_{ds1}}\Omega \tag{3-4}$$

$$T_{oc} \cong T_{dc} = -g_{m3}\cdot R_3^{ol}\cdot(g_{m1}+g_{mb1})\cdot(r_{ds1} \parallel r_{ds10}) \cong - = -44.5 \tag{3-5}$$

and the following values were used:

$$r_{ds13} = \frac{1}{7.84\mu S} \quad r_{ds13} = \frac{1}{1.02\mu S} \quad r_{ds10} = \frac{1}{788nS} \quad r_{ds5} = 28.7k\Omega \tag{3-6}$$

$$g_{ds1} = 4.257\mu S \quad g_{m1} = 79.6\mu S \quad g_{mb1} = 12.3\mu S \quad g_{m3} = 144\mu S. \tag{3-7}$$

Putting these into (3-2) gives

$$R_3^{cl} = \frac{R_3^{ol}}{(1+T_{oc})} = \frac{17k}{45.5} = 375.8\Omega, \tag{3-8}$$

which shows that the local feedback loop reduces the impedance at nodes 3 and 4 by a significant amount.

As discussed in chapter 2, since the output of a transconductor is a current, it is desirable that the circuit has a large output impedance. This helps to minimize the undesirable effects that can occur in a biquad due to small output impedance. If the output stage (one side) consisted only of transistors M_6 and M_8, the output impedance would be $r_{ds6}||r_{ds8}$ - a rather small value for a current source. By including M_{24} and M_{26} to form a cascode configuration (gate bias voltages set by M_{16}-M_{19}), the output impedance increases to

$$Rout = R_{d26}^{eff} \parallel R_{d24}^{eff} \cong 4.7M\Omega, \tag{3-9}$$

where

$$R_{d26}^{eff} = r_{ds26}\left[1 + \left(g_{m26} + g_{mb26}\right) \cdot r_{ds6}\right] + r_{ds6} \cong 109M\Omega \tag{3-10}$$

$$R_{d24}^{eff} = r_{ds24}\left[1 + \left(g_{m24} + g_{mb24}\right) \cdot r_{ds8}\right] + r_{ds8} \cong 4.7M\Omega \tag{3-11}$$

$$r_{ds24} \cong 215.5k\Omega \quad r_{ds8} \cong 211.4k\Omega \quad r_{ds26} \cong 990k\Omega \quad r_{ds6} \cong 617.3k\Omega \tag{3-12}$$

$$g_{m24} = 79.2\mu S \quad g_{mb24} = 14.6\mu S \quad g_{m26} = 132.8\mu S \quad g_{mb26} = 43.3\mu S. \tag{3-13}$$

This large output impedance helps to reduce the undesirable 2nd order effects in the filter biquads due to low output impedance (section 2.4.3). This makes the implemented transfer function more closely approximate the ideal transfer function with, therefore, less distortion.

As a part of using a cascode stage for increased output impedance, it becomes very important to keep in mind the maximum current expected to flow in the output stage transistors: I_1-I_2+i_{oMAX}. As i_o increases from zero to i_{oMAX}, the gate to source voltage of transistor M_{26} will increase, reducing the voltage at the drain of M_6. If the drain voltage of M_6 goes below $V_{DS(sat)}$, it will fall out of saturation and the current mirroring will become nonlinear. Once this occurs, $I_{out}(V_{diff})$ will become increasingly nonlinear and $G_m(V_{diff})$ will have a much sharper roll off as V_{diff} increases than would occur if M_6 is not allowed to come out of saturation. Finally, the small signal output impedance of the transconductor will drop sharply as r_{ds6} decreases - an effect consistent with a nonlinear output current. Conversely, the same effect would occur when the current through M_{27} and M_7 increased to I_1-I_2+i_{oMAX}. In order to prevent this from happening, the gate voltages

of M_{26} and M_{27} set by M_{16}-M_{23} should be large enough to allow for the maximum V_{gs} at i_{oMAX} without pushing M_6 and M_7 out of saturation.

3.2.2 Transconductor Linearity

The key characteristic of a transconductor is the linearity of the output current, I_{out}, as a function of the differential input voltage. Ideally, $I_{out}(V_{diff})$ should be perfectly linear. In practice, nonlinearity will exist due to 2nd order effects in current mirroring and the g_{ds} of the triode region transistor. To what extent this nonlinearity is acceptable depends upon the application [3.6-3.7,3.12]. Often a "reasonably" linear response is sufficient. In other applications, linearity is more critical and it is necessary to minimize undesirable 2nd order effects. For the pulse shaping amplifier, the principle concern for linearity was the filter transfer function. A perfectly linear $I_{out}(V_{diff})$ would yield $G_m(V_{diff}) = \frac{\partial Iout}{\partial Vdiff} = G_m(0)$ - a constant. A G_m that changes with the signal level causes I_{out} to be a nonlinear function of V_{diff}. As $I_{out}(V_{diff})$ becomes increasingly nonlinear, so does $G_m(V_{diff})$ [Figure 45 and Figure 46]. This non-constant $G_m(V_{diff})$ will result in biquad filter poles that are actually functions of the input signal rather than fixed. Examining $G_m(V_{diff})$ makes it easier to determine the suitability of a transconductor for the pulse shaper than examination of the $I_{out}(V_{diff})$ information since $G_m = \frac{\partial Iout}{\partial Vdiff}$. From Figure 47 it can be seen that $G_m(V_{diff})$ is nearly constant in the ±250mV range around V_{diff}=0V, with a variation of approximately 1.2%. Additionally, Figure 48 shows that $I_{out}(V_{diff})$ is nearly linear in this range, with a nonlinearity of ~0.5%. Finally, it should be mentioned that the inclusion of the cascode transistors M_{26} and M_{24} significantly improves the linearity of $I_{out}(V_{diff})$ by

reducing the contribution of the channel length modulation of M_6 and M_7. Intuitively this makes sense because as R_{out} increases, so does the circuit's ability to behave more like an ideal linear current source.

Because of the relationship between G_m and the g_{ds} of the triode region transistor, the fabricated transconductor G_m becomes highly process dependent. Therefore, the transconductors were designed for a nominal value of transconductance with the gate of the triode region device at 0.5V. This allowed the final transconductance to be increased or decreased around this point by lowering or raising this voltage. This was done with the intent to provide an easy method of adjusting the transconductor G_m to the desired point in spite of process variations. Additionally, an effect not shown in the first order model for g_{ds} (equation 2-12), is the process dependence of g_{ds} upon the actual physical dimensions of the transistor and not just the W/L ratio. To provide further protection against this, the dimensions of the triode region device were selected by performing SPICE simulations using BSIM3v3 models to select dimensions that appeared to be more stable across multiple process runs (Table 2). From the table, it can be seen that the value of g_{ds} is simulated to be highly susceptible to process variations when W and L are small. By using W/L=14.4μ/14.4μ, a fairly repeatable g_{ds} was predicted. The range over which g_{ds} was observed to vary was 30-40μS, so the nominal value of G_m designed for was ~35μS. The filter capacitors were selected as C_1=6.1pF and C_2=1.9pF, giving nominal values of $Q \cong 0.56$ and τ=~97nsec for the biquad low-pass filter (Table 3). As can be seen from Figure 46, the transconductor G_m was less than g_{ds}, about 27μS, resulting in an actual τ of ~125nsec. This was a little higher than originally intended, but still within the

desired time constant range of 100-125nsec. Finally, the G_m of the transconductors in the gain stages was set using different values of W/L for M_5, such that the ratio of $(W/L)_5$ in G_{m1} was ten times larger than that in G_{m2} – hence the nominal 10X gain.

3.2.3 Transconductor Noise Analysis

As discussed in chapter 2, one of the primary motivations for using a pulse shaping amplifier is to improve the system SNR. It therefore becomes important to calculate the noise contribution from the transconductors and to estimate the total RMS noise voltage at the output of the shaper. The first part of this, calculation of the transconductor noise, is performed below. This noise is calculated at the output of the transconductor and is then referred back to one input as an equivalent input noise voltage spectral density.

Due to the differential nature of the circuit, the noise from any transistor could contribute to either one or both outputs. For ease of analysis, the differential signal was converted back to a single-ended signal at the transconductor output (see Figure 49). Thus, the noise sources that produced output differential noise resulted in output noise voltage generators and those that produced common mode noise could be ignored. The noise voltage spectral densities at the output were then summed and referred back to the input by dividing by the differential gain from V_{in+} to V_{out}. As outlined in [3.9], taking the sum of the noise voltage spectral densities is valid only if each of the noise generators is independent from all of the other generators. If any two generators are not independent then they are correlated and this component will add to the total noise voltage. Often, when correlation is small, it can be neglected if its contribution is negligible compared to

the other noise generators. For the transconductor circuit, it will be shown that the majority of the transistor noise generators produce uncorrelated noise at the single-ended output – meaning that, effectively, they contribute noise to only one of the two differential transconductor output nodes.

The noise sources for a MOSFET transistor consists of the channel thermal and flicker noise [3.9]. The thermal noise exists because the channel material is resistive. This noise can be modeled as a noise current generator in parallel with the drain to source resistance. Similarly, the flicker noise can also be modeled as a drain to source current generator. Both of these can be combined into one noise generator, i_d^2, with a noise spectral density of

$$i_d^2(f) = 4kT\left(\frac{2}{3}g_m\right) + \frac{K_f \cdot g_m^2}{W \cdot L \cdot C_{ox} \cdot f} \quad \text{A}^2\text{/Hz.} \tag{3-14}$$

In order to calculate the flicker noise, a value for K_f was necessary. As the models provided by AMI did not include this information, data provided in [3.10] was used to calculate reasonable values of K_f for the AMI 1.2μ process:

$$K_{fn} = 4.4\text{x}10^{-24}\ \text{V}^2\text{F} \quad \text{NMOS} \tag{3-15}$$

$$K_{fp} = 1.76\text{x}10^{-25}\ \text{V}^2\text{F} \quad \text{PMOS} \tag{3-16}$$

By examining Figure 39, the transistors with the most significant contribution to the total output noise can be identified. In order to simplify the analysis, the transistors on one side of the circuit will be examined first. Because of the circuit's large output impedance, it can easily be shown that almost all of the current noise, i_d^2, of transistors

M_6 and M_8 will generate a noise voltage at the outputs. Thus, the noise spectral density from these transistors will appear at the nearest output, node 7, as

$$v_{o6}^2(f) = v_{o8}^2(f) = (R_{out})^2 \cdot i_d^2(f) = (R_{out})^2 \cdot \left[4kT\left(\frac{2}{3} g_m\right) + \frac{K_f \cdot g_m^2}{W \cdot L \cdot C_{ox} \cdot f} \right] \text{V}^2/\text{Hz}. \quad (3\text{-}17)$$

Keeping Figure 49 in mind, the noise at node 7 will then refer directly to the single-ended output. The noise at the output was then referred back to the input as

$$v_{in6}^2(f) = v_{in8}^2(f) = \frac{v_o^2(f)}{(A_{vin,o})^2} \ \text{V}^2/\text{Hz}, \quad (3\text{-}18)$$

where the gain from the input to the output was calculated as $A_{vin,o}$=250 (hand) and $A_{vin,o}$=~244.6 (SPICE).

As noted earlier, the local feedback loop will make the resistance looking into nodes 3 and 4 very small – on the order of ~376Ω. Conversely, the resistance looking into the source of M_5 will then be r_{ds5}+376 ohms, where $r_{ds5} \cong$ 28.7kΩ. Therefore almost all of the noise current i_d^2 from M_{13} will flow into the low impedance point at node 3 rather than go through M_5. Consequently, the resulting noise voltage at the outputs due to M_{13} will appear almost entirely at output node 7 – meaning that the component at output node 8 can be ignored for purposes of a first order analysis. The noise voltage spectral density at the single-ended output will then come from node 7 as

$$v_{o13}^2(f) = (R_{out})^2 \cdot i_{d13}^2(f) \ \text{V}^2/\text{Hz}, \quad (3\text{-}19)$$

which can also be referred back to the input with

$$v_{in13}^2(f) = \frac{v_{o13}^2(f)}{(A_{vin,o})^2} \ \text{V}^2/\text{Hz}. \quad (3\text{-}20)$$

In a similar manner, because of the current mirroring and the local feedback loop, almost all of the noise current from M_3 can be considered to appear at output node 7, producing a noise voltage with spectral density of

$$v_{o3}^2(f) = (R_{out})^2 \cdot i_{d3}^2(f) \text{ V}^2\text{/Hz.} \tag{3-21}$$

This can also be referred to the input as

$$v_{in3}^2(f) = \frac{v_{o3}^2(f)}{(A_{vin,o})^2} \text{ V}^2\text{/Hz.} \tag{3-22}$$

The contribution from M_{10} can be calculated by considering the differential output voltage generated by a current source in parallel with M_{10}. Examination of the local feedback loop formed by nodes 5 and 3 shows that the test current, Δi, will cause a current through M_3 of

$$i_{d3} = \Delta i \cdot \left(1 + \frac{1}{g_{m1} \cdot r_{ds5}}\right). \text{ A}^2\text{/Hz.} \tag{3-23}$$

For the case of a noise current with spectral density i_d^2, this current will then appear at the output node 7 as a noise voltage with spectral density of

$$v_{o10,7}^2 = (R_{out})^2 \cdot \Delta i \cdot \left(1 + \frac{1}{g_{m1} \cdot r_{ds5}}\right) \text{ V}^2\text{/Hz.} \tag{3-24}$$

The noise current of M_{10} will also produce a noise voltage at the other output, node 8, but it will instead be

$$v_{o10,8}^2 = (R_{out})^2 \cdot \frac{\Delta i}{g_{m1} \cdot (r_{ds5} + R_{cl}^4)} \text{ V}^2\text{/Hz.} \tag{3-25}$$

Since these noise voltages will be differential, they can then be summed at the single-ended output shown in Figure 49. Finally, the contribution from transistor M_1 can be

calculated in a manner similar to the differential pair [3.9] as an input noise voltage generator at the input V_{in+}:

$$v_{g1}^2(f) = 4kT\left(\frac{2}{3}\right)\cdot\left(\frac{1}{g_{m1}}\right) + \frac{K_f}{W \cdot L \cdot C_{ox} \cdot f} \quad \text{V}^2/\text{Hz}. \tag{3-26}$$

At this point the noise contributions from the transistors in one side of the differential transconductor have been found at the single-ended output. Since the noise power is being summed at the single-ended output, the contribution from the transistors in the other side of the circuit can be included by doubling the sum of the mean-squared values for the first side. Finally, the noise from the triode region transistor M_5 needs to be included as well. As this transistor is in the triode region, it's noise can be modeled as the thermal noise of a resistor of value r_{ds5}. This noise voltage can then be directly referred to the input V_{in+}. The values calculated by hand and from SPICE at the single-ended output and at V_{in+} can be seen in Table 4. The total input noise voltage spectral density as calculated by hand was

$$S_i^{hand}(f) = 5.89 \cdot 10^{-15} + \frac{2.57 \cdot 10^{-9}}{f} \quad \text{V}^2/\text{Hz}, \tag{3-27}$$

while the sum of the SPICE spectral densities values gives an input noise voltage spectral density of

$$S_i^{SPICE-1}(f) = 5.34 \cdot 10^{-15} + \frac{2.45 \cdot 10^{-9}}{f} \quad \text{V}^2/\text{Hz}. \tag{3-28}$$

In order to provide a more accurate spectral density to compare against, the SPICE value was also extrapolated from the .NOISE analysis output. The flicker noise constant was found by examining the total input referred noise voltage spectral density at a low frequency where flicker noise dominated. Similarly, the thermal noise was found by

examining the total input referred noise voltage spectral density at a very high frequency where the contribution from flicker noise was negligible. The result was an input noise voltage spectral density of

$$S_i^{SPICE-2}(f) = 5.58 \cdot 10^{-15} + \frac{2.45 \cdot 10^{-9}}{f} \text{ V}^2/\text{Hz}. \tag{3-29}$$

From these values, it can be seen that the input noise voltage spectral density calculated by hand agrees reasonably well with the SPICE values.

3.2.4 Common Mode Feedback Circuit (CMFB)

As mentioned earlier, because of the fully differential nature of the channel, a common mode feedback circuit (CMFB) is necessary to keep the common mode level at V_{MID} (2.5V). The common mode level at the output of the transconductor can be controlled by adjusting the gate voltage of M_8 and M_9. In essence, the common mode feedback circuit adjusts $V_{SG8,9}$ to select the operating point which, for the same current $I_{D8,9}$, gives the necessary $V_{DS8,9}$ to keep the common mode output level at V_{MID}. The common mode feedback circuit used in the pulse shaper was based on a design presented in [3.8] and is shown in Figure 50. The bias current, I_{cm}, flows in transistors $M_{5'}$ and $M_{6'}$, with $I_{cm}/2$ in each of the differential pair transistors when the input common mode level equals V_{MID}. If the input common mode level increases above V_{MID}, $I_{D1',4'}$ will be greater than $I_{D2',3'}$, causing $V_{SG5'}$ to decrease, and V_{cmfb} to increase. Since V_{cmfb} is connected to the gates of M_8 and M_9 in the transconductor, their common mode current will also decrease, returning the output of the transconductor, and the input of the CMFB circuit, back to V_{MID}. Similarly, if the transconductor output is less than V_{MID}, the common mode

feedback will restore it to V_{MID}. For the case of a differential signal, $I_{D1'}$ will equal $I_{D3'}$ and $I_{D2'}$ will equal $I_{D4'}$. Thus $I_{D1'}+I_{D2'}$ and $I_{D3'}+I_{D4'}$ both still equal I_{cm}, the drain current of $M_{5'}$ is I_{cm}, and V_{cmfb} remains unchanged. Therefore, the CMFB circuit, ideally, only responds to the transconductor's differential output common mode level and not the differential signal.

Consider now the complete common mode feedback loop through the transconductor (Figure 51). The loop transmission can be found by breaking the loop at one input of the CMFB circuit (V_{in1}), injecting a test voltage, V_t, and finding the return voltage, V_r, at the transconductor output. From this, and the operating points in Appendix C, it can be shown that

$$T_{dc} = -\left(\frac{gm_{M1'}}{gm_{M5'}}\right)\cdot gm_{M8}\cdot R_{out} = \left(\frac{56\mu S}{84.3\mu S}\right)\cdot(78.4\mu S)\cdot(4.7M\Omega) = -244.8\,. \qquad (3\text{-}30)$$

Because of the large resistance at the transconductor output compared to CMFB-nodes 2 and 6, it can be seen that the dominant pole, f_{dom}, is located there. The second pole, f_{p2}, occurs at CMFB-node 6 (the V_{cmfb} control line) while the third appears at CMFB-node 2. It can be shown that for the circuit of Figure 51, these poles are

$$f_{dom} \cong 1.45MHz, \qquad f_{p6} \cong 95.4MHz, \qquad \text{and } f_{p2} \cong 551MHz. \qquad (3\text{-}31)$$

Given this, it would at first appear that the CMFB loop transmission would have a PM of about 13°; however, the specific loading that occurs for the gain or biquad configuration should actually be considered when examining the stability of the CMFB loop. For the gain stages, the two transconductors share the same outputs, which halves R_{out} and doubles the parasitic capacitance C_{out} – which, by itself, would yield no change in f_{dom}. However, the magnitude of T_{dc} will be halved due to the lower R_{out}. Also, the input

capacitance of the resistor-connected transconductor, G_{m2}, will add to C_{out}. Finally, the input capacitance of the first transconductor in the following biquad will also add to C_{out}. The result is that $T(f)$ for the gain stage is

$$T(f) = \frac{-122.4}{\left(1+\frac{j\cdot f}{650kHz}\right)\cdot\left(1+\frac{j\cdot f}{58.2MHz}\right)\cdot\left(1+\frac{j\cdot f}{551MHz}\right)} \tag{3-32}$$

which gives a PM ≅ 41° (Figure 52). This also seems low; however, the parasitic capacitance from the layout was ignored. Adding a few hundred femtofarads to C_{out} due to layout quickly shows that the PM quickly improves. Ideally, and in the future, this loop should be made more stable so there will be less chance of oscillation in the gain stage. A similar examination of the biquad shows that due to the large filter capacitance, the two CMFB loops (one for each common output) will have a PM that is approximately 90° (Figure 53 and Figure 54). The two dominant poles will be

$$fdom \cong \frac{1}{2\cdot\pi\cdot(2.35M\Omega)\cdot(12.2pF)} = 5.6kHz \tag{3-33}$$

and

$$fdom \cong \frac{1}{2\cdot\pi\cdot(2.35M\Omega)\cdot(3.8pF)} = 1.8kHz, \tag{3-34}$$

from the 6.1pF and 1.9pF filter caps, respectively.

3.3 Complete Pulse Shaping Amplifier Noise Analysis

3.3.1 Pulse Shaper Noise Analysis

Using the model for the input noise voltage spectral density calculated in section 3.2.3, it is now possible to calculate the total RMS noise voltage at the output of the pulse

shaper. This will be performed by summing the noise spectral densities at each significant node in the pulse shaper and calculating the total mean-squared noise voltage at the output:

$$\overline{v_{oT}^2} = \int_0^\infty |H_v(j \cdot f)|^2 \cdot S_i(f) \cdot df \quad \mathrm{V}^2. \tag{3-35}$$

So, for a system with multiple nodes, there will be a different $S_i(f)$ and $A_v(f)$ for each node. This analysis can be made easier by noting the points where the majority of the contribution will occur – namely those that receive the most total gain through the shaper. From Figure 38, it can be observed that the majority of the noise should be contributed by sources occurring before the output of the second gain stage. From Figure 55, it can be seen that four nodes need to be considered, and that sources at node A will receive more gain than those at nodes B-D. By summing the noise sources at each node (Figure 55), it can be shown that the equivalent noise voltage spectral density at each node is as shown in Table 5. The ideal transfer functions from each of these nodes to the output are shown in Table 6.

In calculating the transfer function from each node to the output, it should be noted that in the fabricated pulse shaper, parasitic poles will exist in the transfer function. If these poles are close to the shaper's transfer function poles, then they will need to be included in these transfer functions. From Figure 38, it can be seen that the RHIC4B op amp used for the differential to single-ended conversion will have a pole at f_{p1}=GBW/10. From [3.2] the GBW is found to be ~15MHz, meaning that f_{p1} is at 1.5MHz. Additionally, the two unity gain buffer op amps, as well as the op amp used to drive the signal off chip, will each add a pole at 15MHz. Finally, because the gain stages are not

ideal, they too will introduce poles located their f_{-3dB} point. Simulations showed that f_{-3dB} for the gain stages was ~13MHz. The simulations also showed that the actual midband gain of the gain stages was 8.27 V/V. This difference from the intended gain of 10 is to be expected due to the process and dimension dependence of the transconductor's G_m. This value was used in the transfer functions to provide meaningful comparisons between the hand calculations and SPICE. Table 7 shows the location of all of the shaper's poles and the corresponding time constants.

Table 8 and Table 9 show the final transfer functions including the effects of parasitic poles. The first table shows the functions assuming the quality factor of the biquads is 0.5 and all of poles are real. The second table includes the effect of Q in the transfer function. This accounts for the actual fabricated shaper's Q of 0.56 resulting from the values of C_1 and C_2 when $G_{m1}=G_{m2}$. The mean squared noise voltage at the output from the equivalent sources at each node was then calculated numerically using

$$\overline{v_{oT}^2} = \int_{10}^{10^7} |H_v(j \cdot f)|^2 \cdot S_i(f) \cdot df \quad \mathrm{V}^2. \tag{3-36}$$

The total output noise voltage was found by taking the sum of these four mean-square values. The results from this are shown in Table 10. The numbers in the table show that the majority of the output noise voltage will be contributed by sources before the first gain stage, with minor contribution from the other three nodes before the second gain stage. It can therefore be concluded that contributions by sources after the second gain stage will be negligible. Thus the calculated value was ~17.3 mV_{rms}, which showed very good agreement with the SPICE value of 16.2 mV_{rms}.

Chapter 4 - Layout and Simulation

4.1 Tools and Technology

4.1.1 Cell Layout and Simulation.

Prototype chips for the pulse shaping amplifier were fabricated using the 1.2μ AMI ABN process provided by MOSIS. The process is an n-well CMOS process with two polysilicon and metal layers. Process parameters and device models extracted by MOSIS from earlier fabrication runs were used to simulate the prototype chips before fabrication. Operation over processing variations was checked by simulating with several sets of extracted models. One set of parameters used for the pre-fabrication simulation (n86o) are shown in Figure 56, with the parameters from the shaper prototype run (n91a) shown in Figure 57.

The layout was done using the public domain CAD tool Magic version 6.3 [4.1]. A modified version of Magic's netlist extraction utility was used to extract the SPICE netlists from the layout information. HSPICE version 96.3.1 by Meta-Software,Inc.was used to perform the SPICE simulations. The models used were BSIM3 v3.1 models provided by MOSIS.

4.2 Pulse Shaping Amplifier

4.2.1 Layout

The top-level block layout of the G_m-C pulse shaping amplifier prototype chip can be seen in Figure 58. An expanded top level view showing the transistors and metal traces is in Figure 59. The prototype chip had a complete shaper, a biquad, and a

transconductor-CMFB cell. RHIC4B operational amplifiers with large output drivers were used as output buffers to drive the signals off chip. The transconductors and the CMFB circuits were laid out with power rails at the top and bottom and of the same heights to facilitate series connection of the cells.

4.2.2 Transconductor Layout

The transconductor circuit was laid out using a modified common centroid arrangement for the input differential pair, with the difference being in the connections at the source (Figure 38). The triode region transistor was laid out with its gate voltage accessible to allow control over the circuit's G_m. Biasing was provided by voltage control lines connected to transistors in a separate biasing circuit. The transconductor layout can be seen in Figure 60.

4.2.3 Common Mode Feedback Circuit Layout

The layout of the common mode feedback (CMFB) circuit can be seen in Figure 61. The two source connected differential pairs were laid out using a common centroid arrangement. The CMFB circuit compares a reference voltage to the common mode level of a pair of shared output lines. Therefore, these sampled output lines pass through the circuit from left to right to allow series connection of the transconductor and the CMFB circuit (Figure 62). The common mode voltage control line from the CMFB circuit to the transconductor can also be seen in the figure.

4.2.4 Gain Stage

When two transconductors are connected into a gain cell as shown in Figure 31, they share the same output connections. Thus, a common mode feedback circuit is required to keep the common mode level of this output at V_{mid}. The layout of the gain cell can be seen in Figure 63.

4.2.5 Biquad Layout

The transconductor based biquad filter layout is shown in Figure 64. Control lines for each of the transconductor pairs identified in Figure 32 were made accessible. The 6.1pF and 1.9pF filter caps can be seen at the right. Each of these were laid out as a single large capacitor to reduce total area but could have been laid out as two smaller capacitors to reduce back plate parasitics (section 2.3.1).

4.2.6 Differential to Single-Ended Converter.

The differential to single-ended conversion was performed using three RHIC4B operational amplifiers – two connected as non-inverting unity gain buffers and the third as the converter. The layout of these can be seen in Figure 65.

4.2.7 Complete Shaper Layout

Figure 66 and Figure 67 show the complete G_m-C based pulse shaping amplifier layout. The CR stages can be seen in the upper left and the lower right. The resistors were polyresistors and the capacitors were poly-poly caps. Filter capacitors for the bias lines were included in the prototype chip layout (upper left and upper middle Figure 67). The pulse shaper signal path is from the CR stage in the upper left, through the upper left gain

stage, the biquad on the right, into the lower right gain stage, and then into the biquad in the lower left. The signal is then converted to a single-ended signal by the operational amplifiers at the bottom, then goes through the CR stage in the lower right, and finally the RHIC4B off chip output driver at the top right. Voltage control lines are provided for the two transconductor pairs in the biquads, with the same lines shared by both biquads. The two transconductor control lines in each gain cell are also accessible, with the pair of control voltages from each gain cell separately accessible. This allows the gain of each of the gain cells to be controlled independently. The break down of the bias and control lines can be seen in Table 11. A pre-fabrication simulation of the shaping amplifier output pulse can be seen in Figure 68. The simulation used the AMI n86o process BSIM3 v3.1 model and a step input of 16mV with a rise time of 20nsec.

Chapter 5 - Experimental Results

5.1 Performance and Experimental Results

5.1.1 Test Board

A test board was constructed to test the devices on the prototype chip. The board provided the necessary biasing and signal buffering for testing of the chip. Additionally, adjustable voltage control lines were connected to the prototype chip's transconductor control lines. A picture of the prototype test board can be seen in Figure 69.

5.1.2 Measured Transconductance

Transconductors with three different values for the triode region device's W and L were used. The principle device was the transconductor used in both biquads, labeled Full_Gm1b, with a (W/L) for the triode region device of 14μ/14μ. The other two transconductors were in the Gain cell (Figure 31), and had a G_{m1}:G_{m2} ratio set by their triode region devices of 9:1. The first transconductor, labeled Full_Gm1c in the layout, uses a $(W/L)_5$ of 4.8μ/9.6μ, while the second transconductor, labeled Full_Gm3b, uses a $(W/L)_5$ of 21.6μ/4.8μ.The first dimension was chosen for the W/L ratio less than one to keep the actual G_m of the second device small, and hence the bias current requirements reasonable. The second dimension was inadvertently smaller than required for the originally intended G_{m1}:G_{m2} ratio of 10:1, resulting in an ideal nominal gain of 9 instead of 10. A breakdown of the prototype chip's transconductor parameters can be seen in Table 12.

The prototype chip contained a test transconductor that was used to measure the linearity of the circuit's transconductance. This measurement was made using an HP4156A semiconductor parameter analyzer. A fully differential voltage was applied to the input terminals and the differential output current was measured. The experimentally measured results were compared to the behavior predicted by SPICE for the pre-fabrication simulation using the N86O process data, and to the N91A fabrication run data provided by MOSIS. A plot of the experimentally measured $I_{out}(V_{diff})$ can be seen in Figure 70 (V_c=0.5V) and Figure 71 (V_c=0 to 1V). The measured nonlinearity of $I_{out}(V_{diff})$ with V_c=0.5V, Figure 70, was ~2.7%. Note, that due to the differential nature of the channel, the polarity of I_{out} is arbitrary. The derivative of $I_{out}(V_{diff})$ was calculated and window averaged using Excel to give the measured $G_m(V_{diff})$ (Figure 72 and Figure 73). The measured variation of G_m from G_{m0} was ~6.8%. From the $I_{out}(V_{diff})$ graph, the points where the output current becomes limited by the DC bias currents can be seen as a sharp corner in the output current. These points appear on the $G_m(V_{diff})$ graph as the drastic decrease in G_m as V_{diff} approaches ~500mV. Figure 74 and Table 13 show the measured value of $G_m(V_{diff}$=0V) as a function of the control voltage, V_c, compared to that predicted by SPICE.

The corresponding plots from pre-fabrication SPICE simulations with the N86O process data can be seen in Figure 75 and Figure 76. Simulations using the N91A fabrication run data are shown in Figure 77 and Figure 78. From these figures, it can be seen that the transconductor circuit's simulated behavior (N91A process) agrees well with the experimental measurements. Additionally, by comparing the N91A figures to the

N86O process figures, the process to process variation in G_m can be seen to be about 5% - as predicted by the data in Table 2.

At this point, it should be mentioned that the fabricated transconductors were slightly different than the transconductor circuit presented in Figure 39. The fabricated transconductor circuit (Figure 89) had an extra diode connected transistor in the series of diode-connected devices used to set the gate voltage of transistors M_{26} and M_{27}. The result was that the gate voltage of these two transistors was lower than desired. While sufficient to keep M_6 and M_7 in saturation under DC bias conditions, as $V_{GS26,27}$ increased to accommodate the small signal output current, i_o, M_6 and M_7 started to leave saturation. This is the issue discussed in section 3.2.1 with regard to the circuit's output impedance/output current linearity. This problem resulted in a $G_m(V_{diff})$ curve that was slightly lower and had a sharper roll-off than the transconductor circuit with the corrected output stage. This effect also corresponds to an $I_{out}(V_{diff})$ that has a smaller slope and is less linear than the corrected circuit's. This difference is shown in Figure 79, Figure 80, and Figure 81. From these figures, it can be seen that while the G_m of the fabricated transconductor is smaller, the two sets of curves have regions where they overlap. The noise analysis of chapter 3 was performed using a G_m of 27μS, which can be seen to be a value where there two curves overlap, and is thus a reasonably valid analysis for the fabricated transconductor circuit. Finally, even though the fabricated circuit has a less linear $I_{out}(V_{diff})$ and a $G_m(V_{diff})$ that has a sharper roll-off, it can be seen from the figures that this effect will still be minimal over the operating region of $V_{diff} \cong \pm 250$mV.

Plots of $I_{out}(V_{diff})$, $G_m(V_{diff})$ and $G_{m0}(V_c)$ for the Full_Gm1c and Full_Gm3b transconductors are shown in Figures 82 to 86. This information was used to aid in

controlling the gain of the adjustable gain cells during the experimental testing. From the figures for the first gain cell transconductor, Full_Gm3b, it can be seen that as V_c decreases (and the gain increases), the output current quickly begins to be limited by the circuit's bias current. For the first gain cell, where the largest gain is desired, this did not present a problem due to the small differential input signal. Nor was there a problem in the second gain cell, as the differential signal level after the first biquad was also well below this limit. Therefore, both gain cells could be operated at their maximum levels without concern for bias current limitations.

From the simulations, it was found that the mid-band gain of the gain cell with both control voltages set to 0.5V was ~8.27 V/V with the N86O model, and ~8.83 V/V with the N91A model. However, was the range over which the G_m ratios could be adjusted was more important. Table 13 shows the G_{m0} of the three transconductors for different values of V_c. An examination of this information shows that a minimum gain level of ~3.0V/V could be attained when G_{m1}=34.5μS and G_{m2}=11.6μS. Similarly, a maximum gain level of ~21.6V/V occured when G_{m1}=106μS and G_{m2}=4.9μS. Therefore, two operating modes for the gain cell were identified: a low gain mode and a high gain mode (Table 14). The gain in both modes of operation was measured using a prototype gain cell from an earlier fabrication run (N88Z) and compared to the gain predicted by SPICE (Figure 87 and Figure 88). The figures show that while the measured gain was more linear than the SPICE prediction, it did differ from the prediction in both modes of operation.

5.2 Pulse Shaper Experimental Testing

5.2.1 Shaper Operational Testing

The prototype pulse shaper was tested using the measured results for the transconductor's $G_m(V_{diff})$ and the gain cell operating modes. Bias points for proper operation were established and can be seen Table 15. The first gain cell was operated in the low gain mode, with a predicted gain of ~9.1 V/V. This provided the desired gain level to keep the first transconductor in the shaper as the dominant contributor to the total RMS output noise voltage (section 3.3). The second gain stage was operated in a very low gain mode in order to keep the output signal level within the output drive range of the RHIC4B differential-to-single-ended conversion stage. The total gain from the gain stages needed for this ended up being smaller than pre-fabrication SPICE simulations predicted. It is believed that this is due to a divergence between the gain cell transconductors' actual G_{m0} and that predicted by the extracted N91A SPICE model - meaning that the gain cells have an even higher gain value than that predicted in Table 14. This is supported by the measured information shown in Figure 87. Future implementations of transconductor based gain cells in a G_m-C pulse shaping amplifier should include on chip test circuits for these transconductors as well. This would allow more accurate knowledge of the actual fabricated gain of these devices. Because of the higher shaper gain, it is also observed that the large 10X gain in the differential to single-ended converter would also not be necessary in a future implementation. Finally, experimental results showed that the output swing limitations of the RHIC4B were not symmetrical. Instead of being centered around 2.5V, they were centered at 2.75V. By

increasing the common-mode level in the differential channel to V_{MID}=2.75V, a larger output pulse was possible.

The transconductor control voltage for the biquad transconductors was selected at 0.1V. This was based upon the experimental measurements (section 5.1.2) which showed that a V_c=0.1V would give a G_{m0} of 27μS. This choice would then give a higher G_{m0}; and, hence, a τ of 125nsec, as desired for the biquads to maintain consistency with the noise analysis of Chapter 3. The transient response of the prototype pulse shaper with the nominal Q of 0.56 can be seen in Figure 90 and Figure 91. The experimentally measured times from the start of the input pulse to different points in the shaped pulse are shown in Table 16. It can be seen that the time from the input step pulse to the first peak of the bipolar output is ~615nsec while the complete shaped pulse time is ~1.95μsec. As discussed in Chapter 2, the first number is important for preventing large ballistic deficits due to the detector charge collection time. The second number is important in limiting the effects of pulse pileup. The time between these two numbers, about 1.335μsec, is effectively channel "dead time", in which the system cannot be used to process another detector *x-ray* absorption event. Increasing the biquad low-pass filters' quality factor above the nominal value can reduce this time. In so doing, the second lobe of the bipolar pulse returns to the baseline (V_{MID}) faster in order to keep the same area as the first pulse lobe. This also results in improved symmetry between the two lobes. An illustration of this effect is shown in the results presented in Table 17. Because the fabricated transconductors had a lower G_{m0} than originally intended, all later experimental testing was performed using the bias values (Table 15) that gave the largest peak-to-peak output

signal swing. Figure 92 shows the shaper's output signal from a 16mV input pulse of both polarities. The maximum peak-to-peak output swing for both polarity pulses was measured as 1.02V. Finally, a plot of the shaper's measured frequency response is shown in Figure 93.

5.2.2 Shaper Noise Measurements

Before examining the noise of the shaper, it will be beneficial to recall the relationship between the total mean-squared output noise voltage and the shaper's transfer function:

$$\overline{v_{oT}^2} = \int_0^\infty |H_v(j \cdot f)|^2 \cdot S_i(f) \cdot df \quad \mathrm{V}^2. \tag{5-1}$$

From this, it can be seen that $\overline{v_{oT}^2}$ is related to the area under the shaper's frequency response curve. This observation will be important when comparing the shaper noise predictions in Chapter 3 to the prototype shaper experimental results and the N91A SPICE simulations.

The input of the shaper was shorted to ground and the total output RMS noise voltage at the output of the shaper was measured using an HP3400A true RMS volt-meter. The result of this measurement was 7.7mV$_{rms}$. The noise can also be measured another way, as discussed in [5.1], using a pulse height analyzer. A constant amplitude pulse is used as the input to the shaper, and the resulting pulse height at the output is measured. This process involves the use of an analog-to-digital conversion, so that the measurements are made with discrete height "windows". The pulse height analyzer then counts the number of times the output pulse falls within each window. If the output pulse

contains no noise, it will have a constant height and always fall within one "window" of the pulse height analyzer. If noise is present, then the output pulses will be superimposed on the noise voltage and the resulting output pulse will no longer be of a constant height. This will result in counts in the "windows" to either side of the correct noiseless "window". The result is a pulse height distribution with mean equal to the noiseless mean pulse height and a standard deviation equal to V_{rms}, the RMS noise voltage level at the output (Figure 14). The value of V_{rms} can then be found by relating the full voltage width at half max, V_{FWHM}, to V_{rms} as [5.2]

$$V_{FWHM} = 2.36 \cdot V_{rms}. \tag{5-2}$$

The value of V_{rms} measured for the prototype pulse shaper using this method was $8.52mV_{rms}$. This value is a little higher than that found using the true RMS voltmeter. This is expected as the measurements using the pulse height analyzer involve a pulse generator, which introduces some noise into the input of the shaper.

Figure 94 shows a plot of the frequency response for the prototype shaper as predicted by SPICE using the bias settings in Table 15. The total output noise voltage predicted by SPICE was $5.2mV_{rms}$. This prediction is smaller than both of the experimentally measured results. This is reasonable as the actually circuit should have a larger output noise voltage because of noise introduced through the power supplies and bias lines. Additionally, as can be seen from Figures 93 and 94, the mid-band gain of the prototype shaper is higher than the SPICE prediction, 39.8dB versus 32.0 dB. Again, this is also consistent with the earlier observations of a higher gain in the gain cells than

predicted by SPICE. This higher mid-band gain which will also increase the shaper's output noise above the value predicted by SPICE. These results can be seen in Table 18.

The noise results can also be compared to the calculations in Chapter 3 of $16.2mV_{rms}$ (SPICE) and $17.6mV_{rms}$ (hand). To do this, recall that the mid-band gain of the prototype shaper's gain stages was lower than the nominal values used in the Chapter 3 calculations. By using the bias settings from Table 15, SPICE predicts a total output noise voltage of $7.7mV_{rms}$ for the shaper based upon the corrected transconductors - a result consistent with the prototype shaper's SPICE prediction. A plot of the frequency response for this shaper is shown in Figure 95.

In order to adjust the hand calculated noise value, the mid-band gain of the shaper's transfer function (Table 9) needs to be adjusted. The nominal mid-band gain, K, of 683.9 corresponds to a gain of $8.27^{V/V}$ in both gain cells and 10 in the differential-to-single-ended converter. At the operational bias settings of Table 15, the mid-band gains are $8.93^{V/V}$ for the first gain cell, and $2.9^{V/V}$ for the second. This gives a mid-band K of ~259, which can be used to give a calculated output noise prediction of $6.5mV_{rms}$. A plot of the frequency response predicted using this new K can be seen in Figure 96. These results can also be seen in Table 18.

As discussed above, the experimental measurements yield a slightly larger output RMS noise voltage than that predicted by SPICE using the prototype fabrication run models. This increase is to be expected due to noise introduce through the power supplies and the bias lines. Additionally, it can be seen that the noise predictions from Chapter 3 are in agreement with the prototype shaper's SPICE and measured values when adjusted for the lower mid-band gain at the operational bias settings. The pulse shaper's output

signal to noise ratio was calculated as 17.8dB for the smallest anticipated input pulse of 1.6mV, and 38.1dB for the largest anticipated input pulse of 16mV (Table 19). Finally, the experimental noise measurements for the shaper can be compared to the preamplifier's output noise. This can be done using the experimental results from the HP3400A measurement by referring the shaper's total mean squared output noise back to the input by dividing by the square of the mid-band gain. This gives a 78.8μV_{rms} equivalent input noise voltage from the shaper, which can be compared to the experimentally determined 800μV_{rms} output noise voltage for the MicroCAT preamplifier [5.3]. Therefore, when compared at the input of the shaper, the preamplifier noise dominates over the shaper noise by a factor of ten.

5.3 MicroCAT Chip

Figure 97 shows a picture of the complete analog channel prototype chip implemented using a pulse shaping amplifier based upon the fixed transconductor design. The gain of the differential to single-ended converter was reduced to 1X, which should allow for the increased gain of the transconductor based gain stages mentioned in section 5.1.2. The transconductors were based upon the fixed circuit design presented in Figure 39 and analyzed in Chapter 3. Currently this chip is awaiting testing.

Chapter 6 - Summary and Future work

6.1 Summary

6.1.1 Conclusion

The prototype G_m-C based pulse shaping amplifier operated as desired with:

- An output bipolar pulse with a 1V peak-to-peak swing for a 16mV input pulse.
- Approximately 615nsec time to the first pulse peak.
- Bipolar pulse return to baseline of ~2μsec.
- Adjustable shaper gain.
- Adjustable quality factors that can be used to improve the output pulse symmetry and decrease the time for the signal to return to baseline.
- Adjustable ω_o and τ by changing the filter transconductors' $G_m(V_{diff}=0V)$.
- Fabricated transconductor G_m's that agree well with the SPICE predictions and appear reasonably stable across multiple process runs.
- Total output noise voltage ~$7.7mV_{rms}$ and an equivalent mid-band input noise voltage of $78.8\mu V_{rms}$.

The prototype shaper design could easily be improved upon by using the corrected transconductor circuit design. This circuit has a current linearity and G_m stability simulated to be ~5.5 times better than the fabricated transconductor design (sections 3.2.2 and 5.1.2). As the corrected circuit has a lower G_{m0} than the triode region transistor's g_{ds}, the filter capacitor should be adjusted to C_1=5.1pF and $C_2 \cong$1.3pF (corresponding to a

nominal G_m, with V_c=0.5V, of ~25.5μS). The back plate capacitance of the filter capacitors should be taken into account as discussed in section 2.3.1. The operational amplifier based differential-to-single ended conversion can be eliminated to reduce overall circuit size and power consumption. This can be replaced with a transconductor based gain stage and a single buffer operational amplifier, connected to a single-sided output from the gain stage. The gain stage transconductors might need to be modified if more gain is desired than the current/gain limitations will allow. This would entail larger bias currents, a larger G_{m1}:G_{m2} ratio and making sure the output transistors stay in saturation over the larger signal swing. Finally, the common mode feedback loop of the gain stages should be modified to improve the loop's stability against oscillation (section 3.2.4).

Observations taken from this design are that a G_m-C filter based pulse shaper offers several advantages over more traditional Sallen-Key based shapers. The greater control over filter parameters provides adjustable time constants and control over the bipolar pulse symmetry while the transconductor based gain stages provide an easily controlled shaper gain. In spite of these advantages, the experiences from this design have also shown there are some disadvantages to using this type of shaper. The process dependence of the triode region transistor's g_{ds} will cause the transconductors' G_m to change from run to run. In order to fine tune the filters and the gain stages, these variations need to be known. This introduces the need to either measure the transconductor's G_m for each process run or to add additional automatic tuning circuitry. While process run measurements may be acceptable for low volume designs, an automatic tuning circuitry would be essential in a large volume design.

A second aspect of the G_m-C based shaper that increases its design complexity, is the necessity of maintaining the signal level within the limits set by the transconductors' bias currents. This becomes especially critical in the gain stage, where a large gain requires a large G_{m1}. Additionally, the signal limitations imposed by keeping the triode region devices in the linear region and the transconductor's output dynamic range limitations can also increase the design complexity.

Because of the additional complexity required in a G_m-C based pulse shaper, it is believed that such a design is best suited for applications where additional control over the shaper parameters offsets the added engineering effort. Specifically, if tunable time constants, controllable bipolar pulse lobe symmetry, or low power consumption are desired, a G_m-C based pulse shaper approach should be considered. Such an approach could be made even more compelling if an automatic tuning circuitry was readily available. For the pulse shaper design presented here, this tuning circuitry should allow the user to select a desired G_m product for the filter biquads to set the low-pass filters' ω_o. An additional function for the tuning circuit try, one that would greatly enhance the potential of a G_m-C pulse shaper, would be the capability of maintaining a constant ω_o while the filter quality factors are adjusted. Finally, it should be noted that the output pulse amplitude may not be entirely independent of the shaper's time constants because the CR stages have fixed τ's, while the biquads have adjustable time constants. The effect of this on the output pulse amplitude should also be considered in later work.

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Appendices

Appendix A

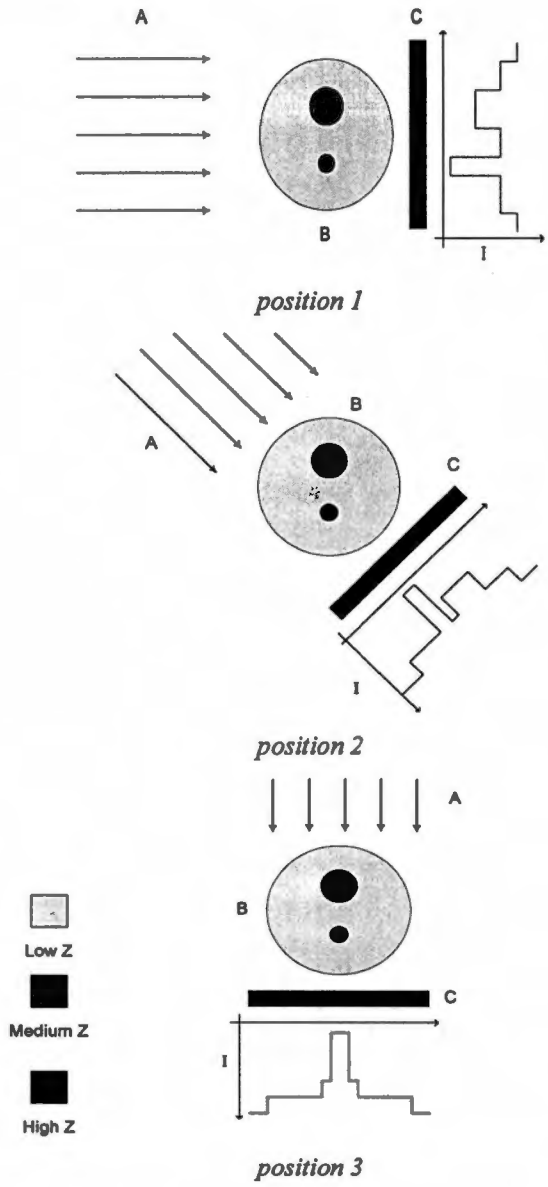


Illustration of *x-ray CT* projection data acquisition as the *x-ray* source (A) and detector (C) and are stepped about the subject (B). In the representative projection data plots the *u* is the axis along the surface of the detector and *v* is the axis along which the *x-rays* are incident.

Figure 1. Acquisition of *X-ray* CT projections.

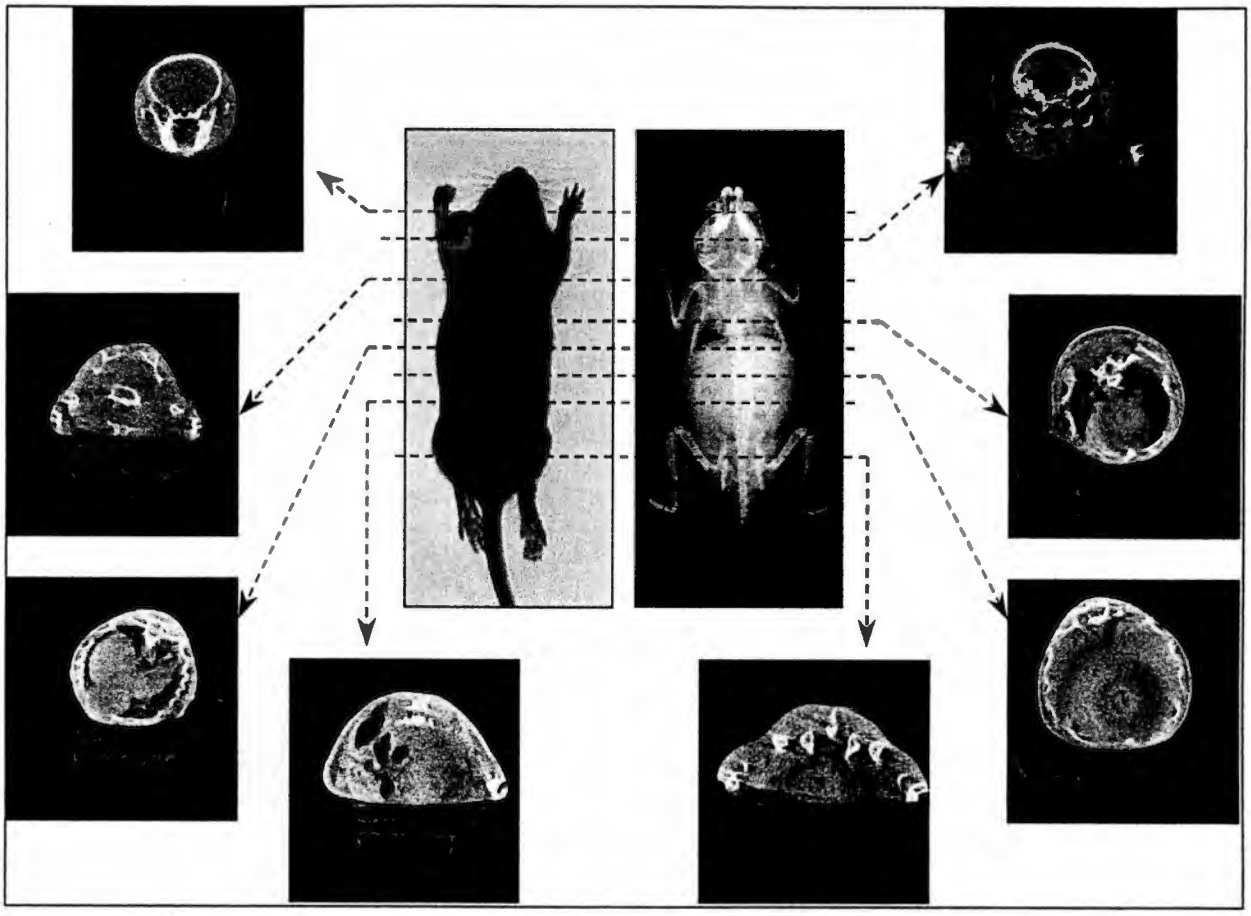
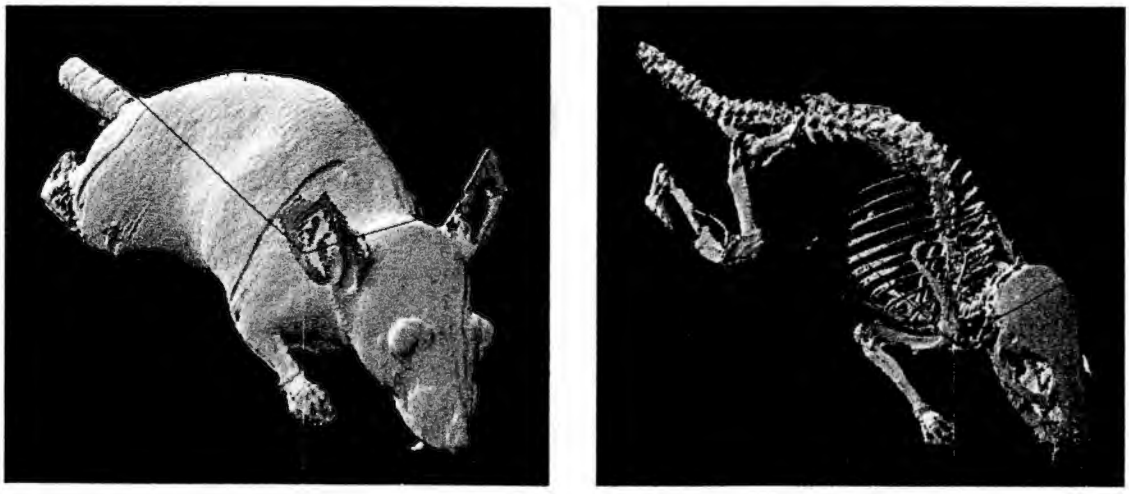


Figure 2. Some example *X-ray* CT images.



(a) Surface Rendering (b) Skeletal Rendering

Figure 3. Some 3-dimensional reconstructions.

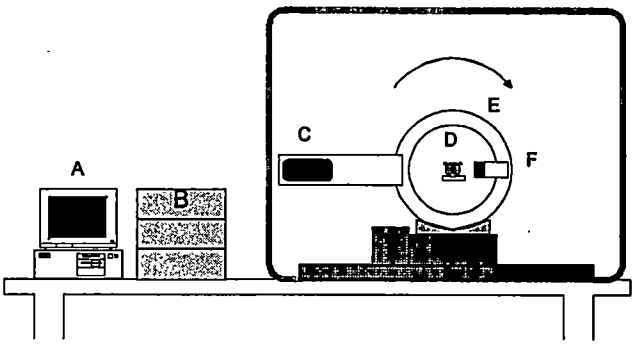


Figure 4. Schematic diagram of MicroCAT system.

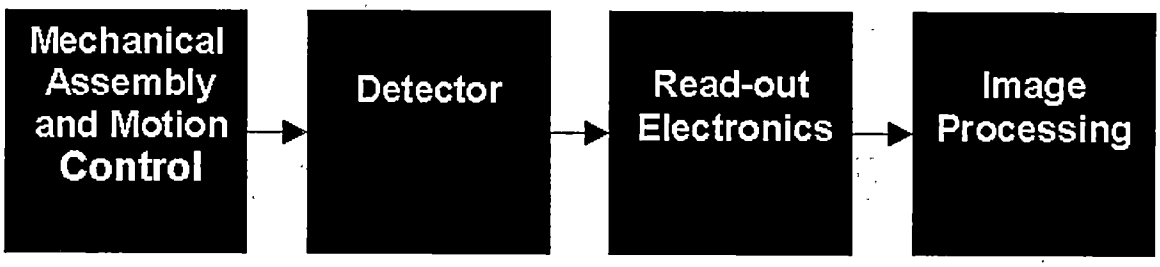


Figure 5. MicroCAT system black box overview.

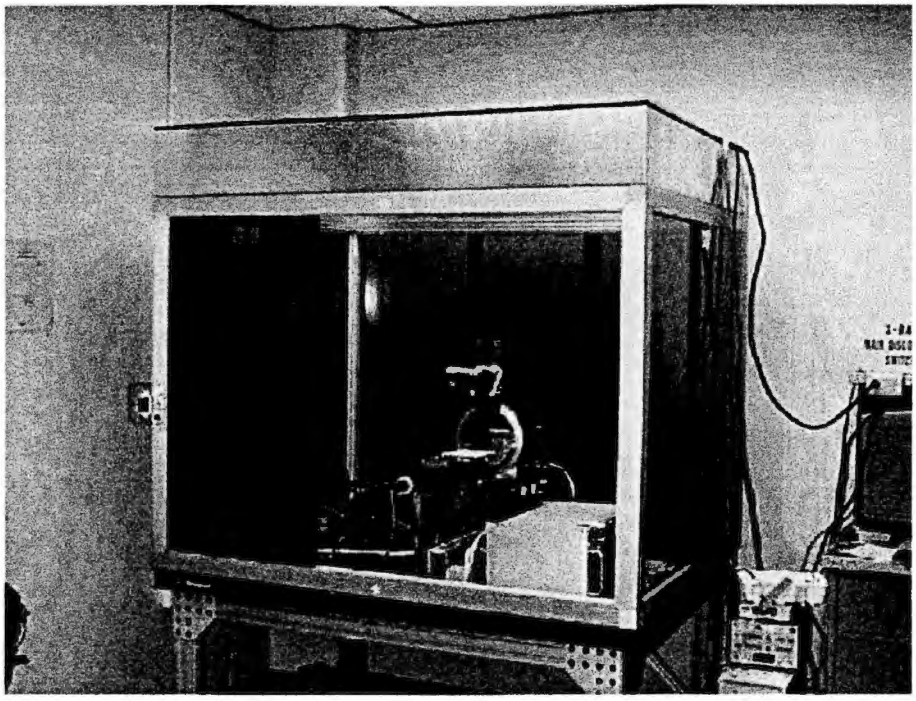


Figure 6. MicroCAT system and enclosure.

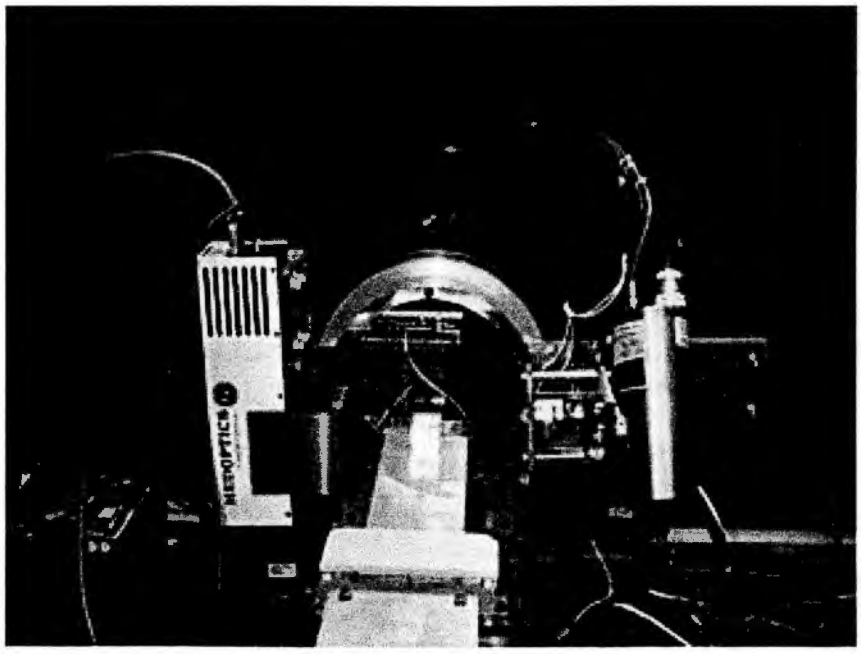


Figure 7. CCD detector, rotating stage, and *X-ray* source.

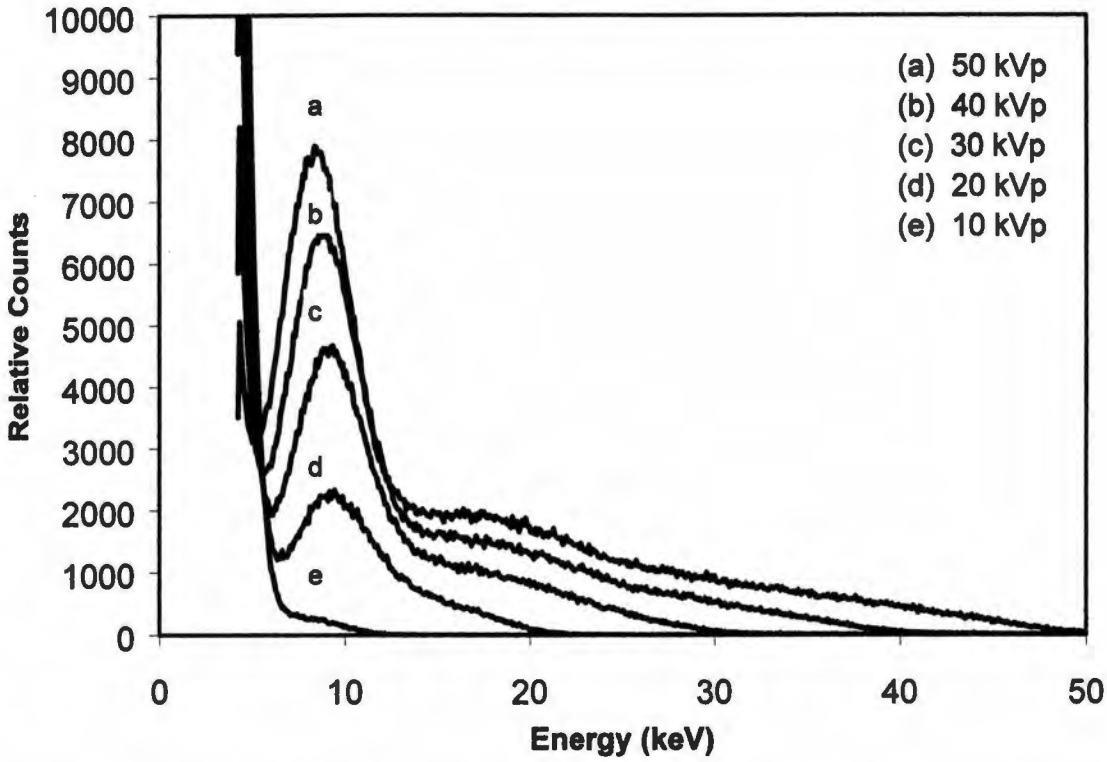


Figure 8. Measured x-ray spectra obtained using the collimated single pixel CZT detector. Source: M. J. Paulus, *et al.*, "A New X-ray Computed Tomography System for Laboratory Mouse Imaging," paper M6-31, presented at the *1998 Medical Imaging Conference*, Toronto, November, 1998.

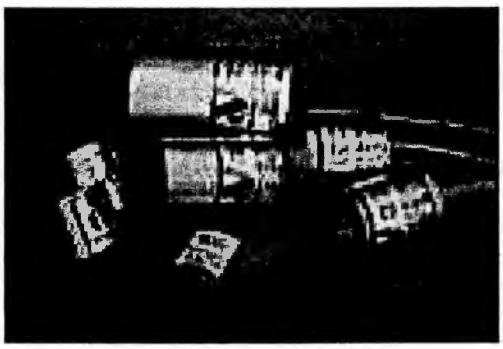


Figure 9. Single pixel CZT detector.

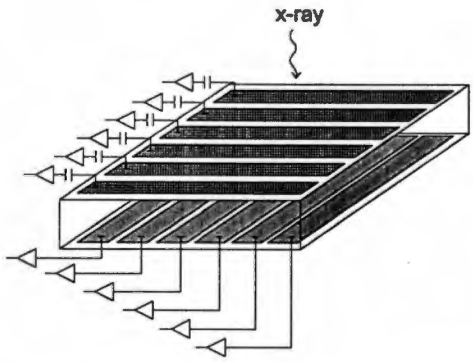


Figure 10. Schematic diagram of a CZT double-sided semiconductor strip detector.

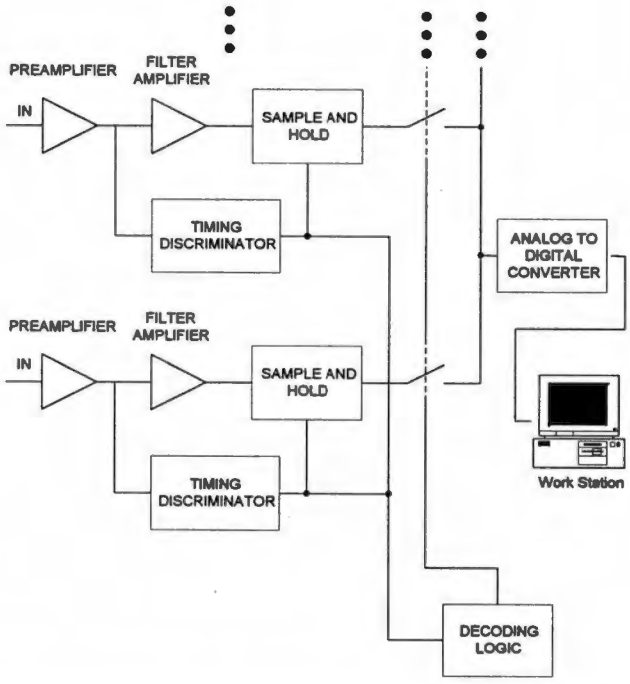


Figure 11. Two channels of proposed application specific integrated circuit.

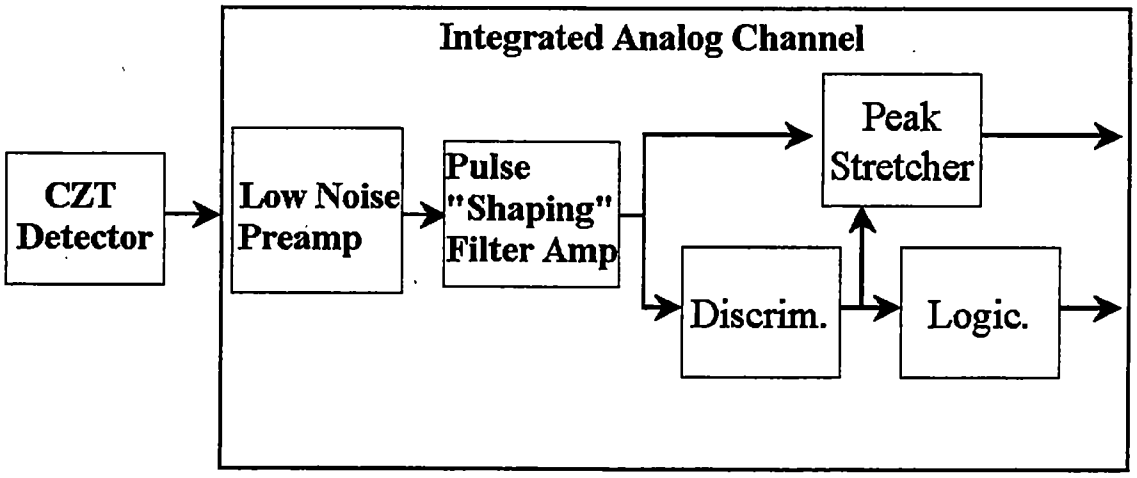


Figure 12. Analog channel and detector block diagram.

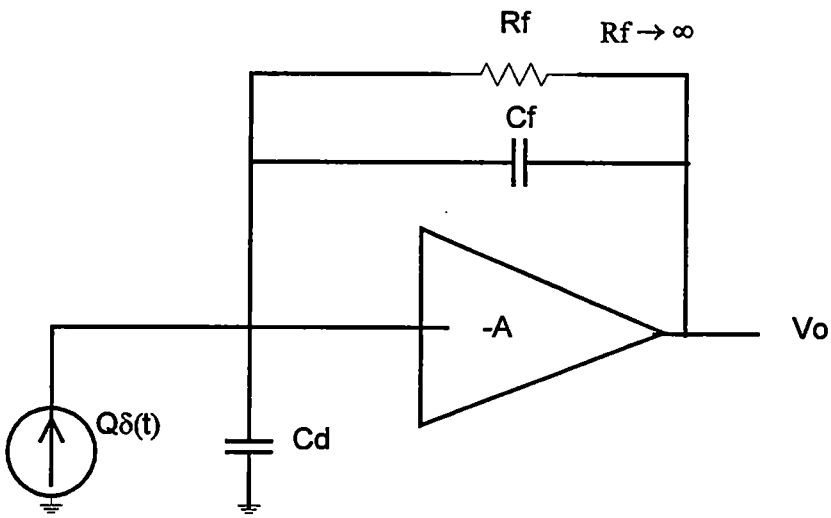


Figure 13. Charge sensitive preamplifier.

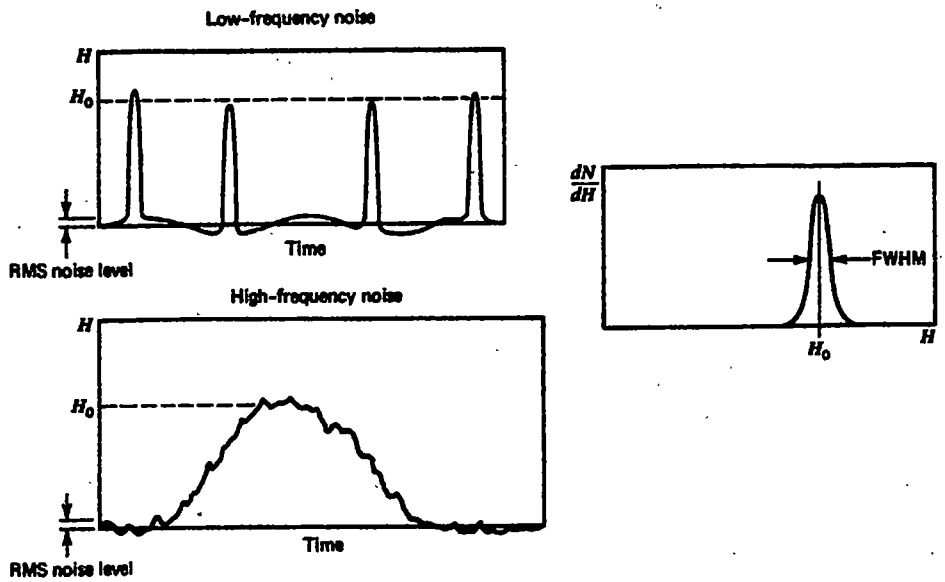


Figure 17-13 Sketches of the effect of low-frequency and high-frequency noise on signal pulses of constant amplitude. The effect is to broaden the peak recorded in the differential pulse height spectrum for these pulses. The FWHM of the peak of Gaussian-distributed noise will be equal to the RMS noise level multiplied by a shape factor of 2.35, provided noise is the only factor in broadening the peak.

Figure 14. Effect of noise on signal pulses. Source: Glenn F. Knoll, (1989) Radiation Detection and Measurement, John Wiley and Sons, Inc. pp. 608.

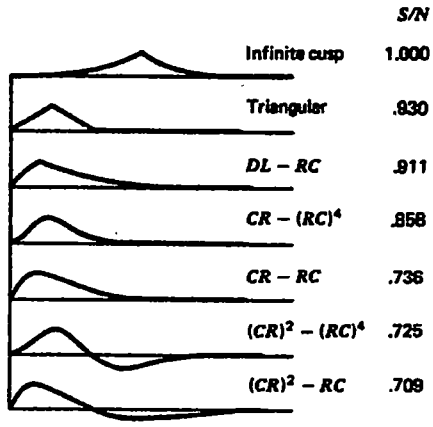


Figure 17-14 Various pulse shapes and their signal-to-noise ratio (S/N) relative to the infinite cusp. Various time constants are chosen to yield minimum noise, and pulse shapes are normalized to constant height. (Reproduced with permission from *Nuclear Electronics*, by P. W. Nicholson. Copyright 1974, by John Wiley & Sons Ltd.)

Figure 15. Pulse shape signal-to-noise ratios. Source: Glenn F. Knoll, (1989) Radiation Detection and Measurement, John Wiley and Sons, Inc. pp. 609.

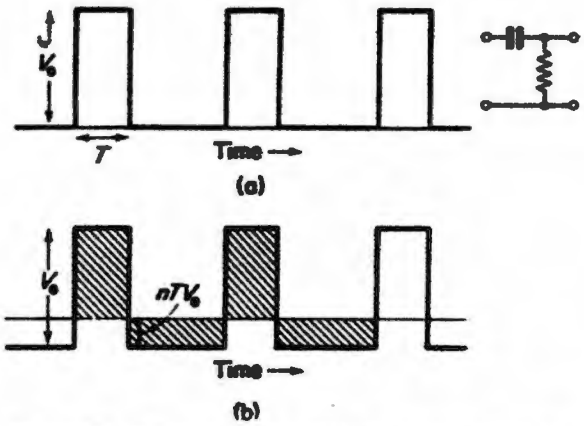


Figure 3.9 Effect of passing unipolar square pulses into a CR high pass filter. n is the rate of the pulses and the result is shown in (b)

Figure 16. Illustration of baseline shift. Source: P. W. Nicholson, (1974) Nuclear Electronics, John Wiley & Sons, Ltd., pp. 96.

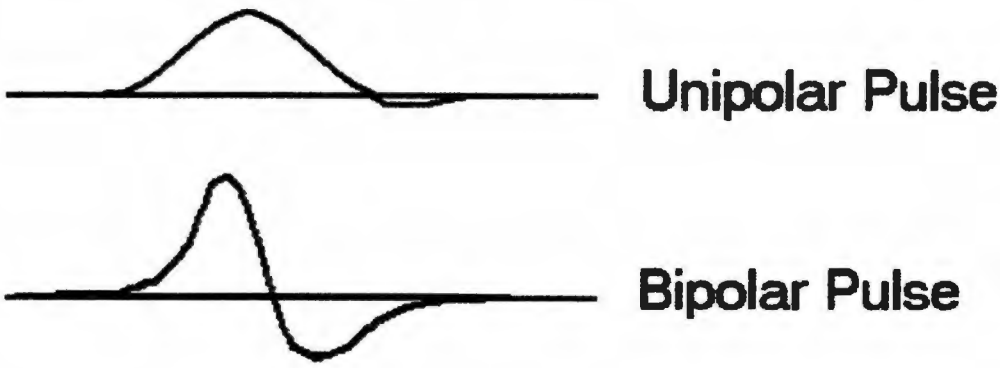


Figure 17. Unipolar and bipolar pulse shapes.

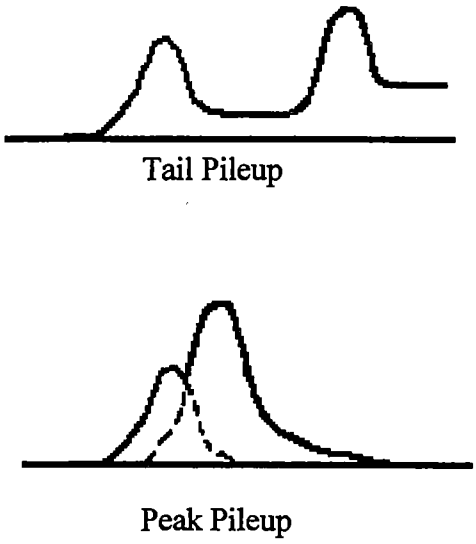


Figure 18. Illustration of pulse pileup.

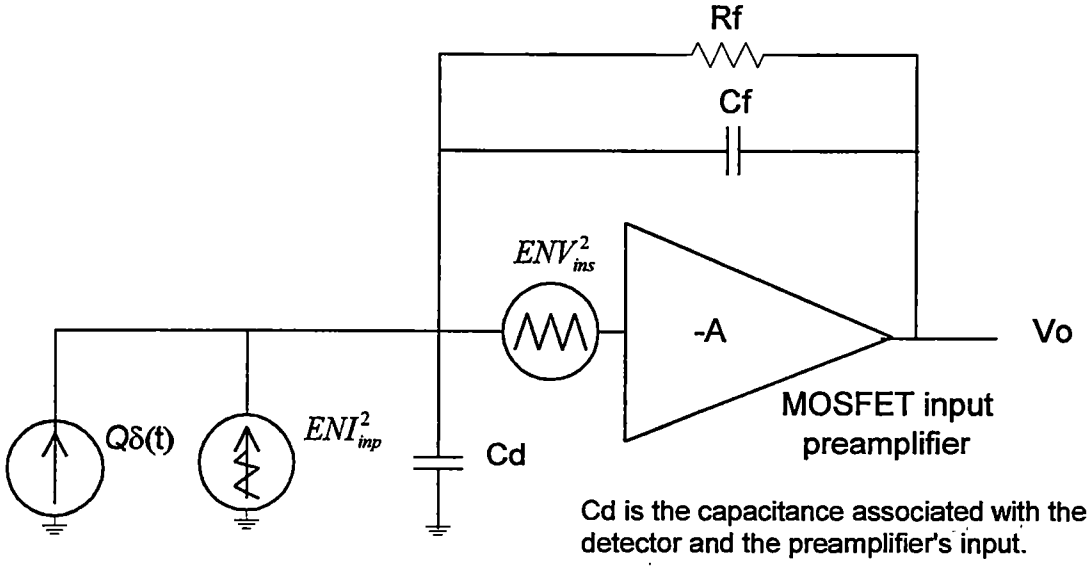


Figure 19. Detector and charge sensitive preamplifier with series and parallel noise sources.

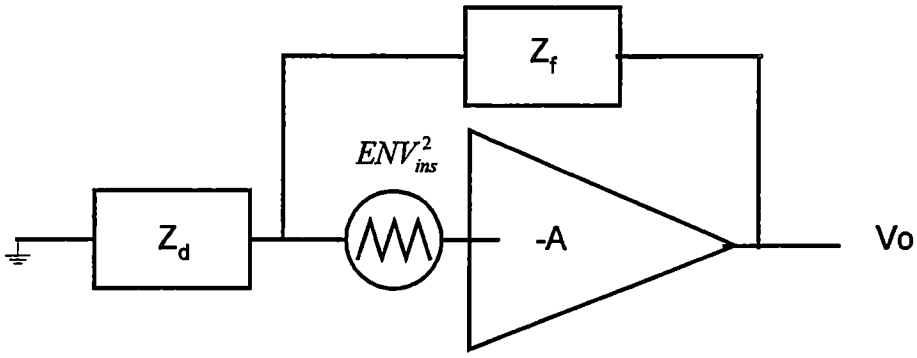


Figure 20. Series noise generator.

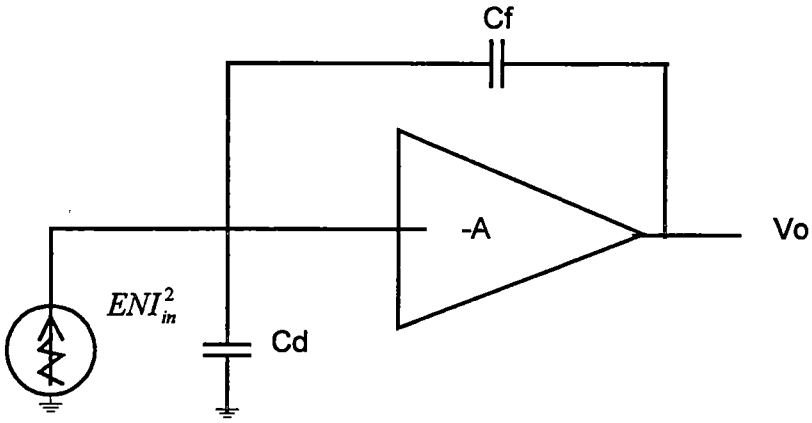


Figure 21. Parallel noise generator.

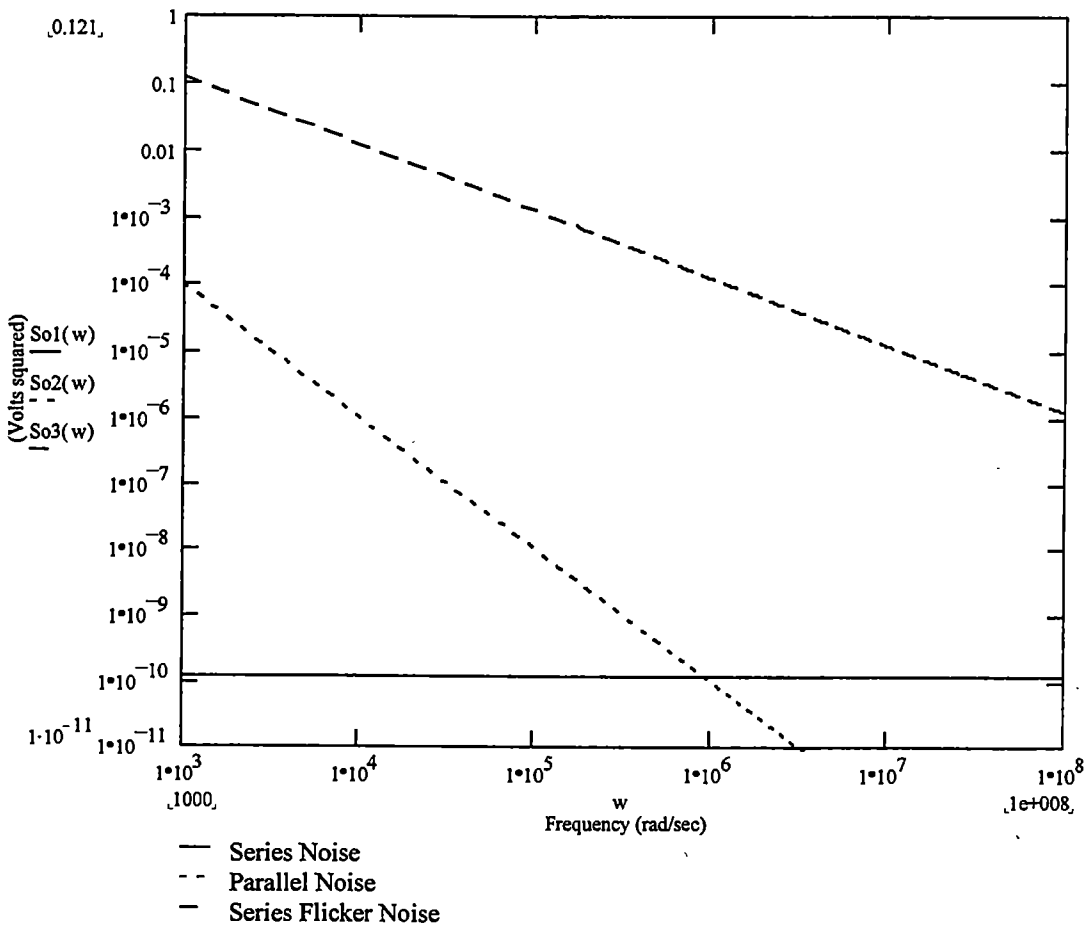


Figure 22. Preamplifier output noise voltage spectral density as a function of frequency.

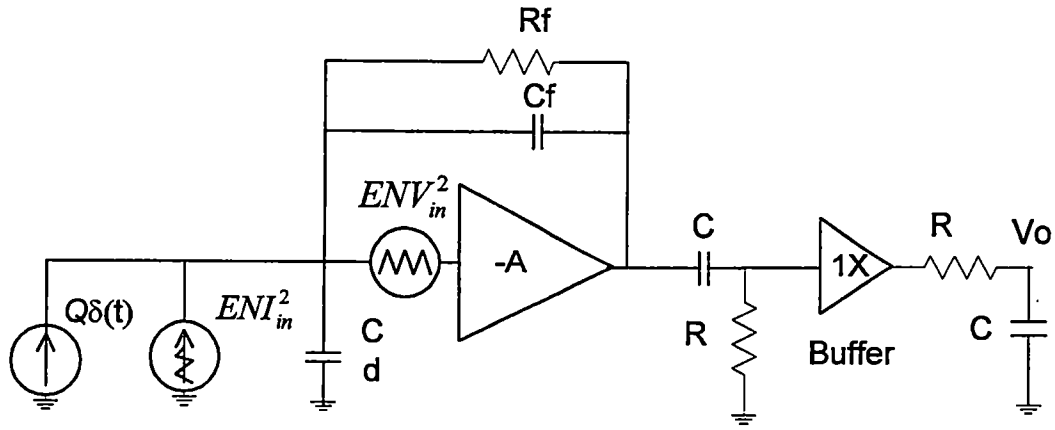


Figure 23. CR-RC pulse shaper with preamplifier, detector and noise sources.

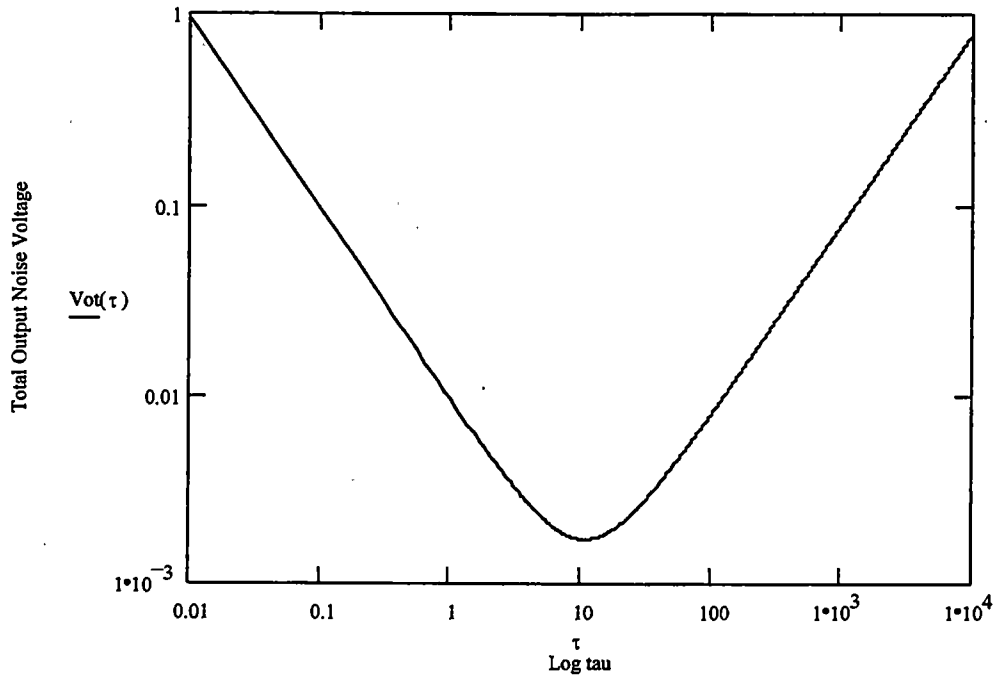


Figure 24. Example of total output noise voltage for a CR-RC shaper vs. tau using example component values.

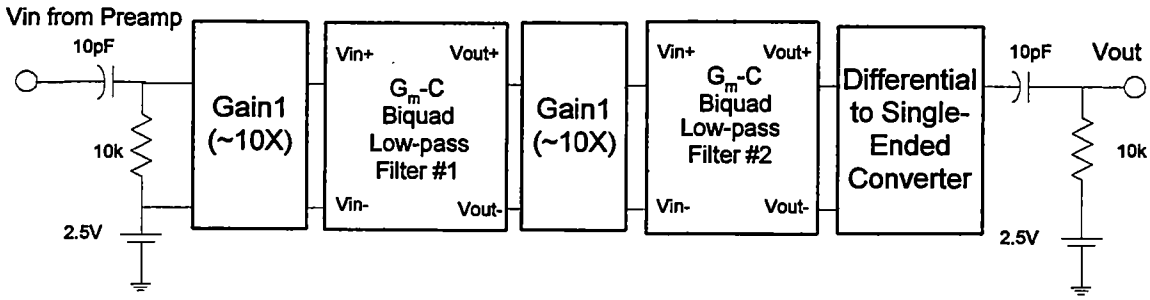


Figure 25. Pulse shaping filter amplifier topology.

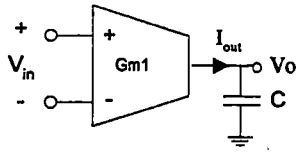


Figure 26. A single-ended G_m-C integrator.

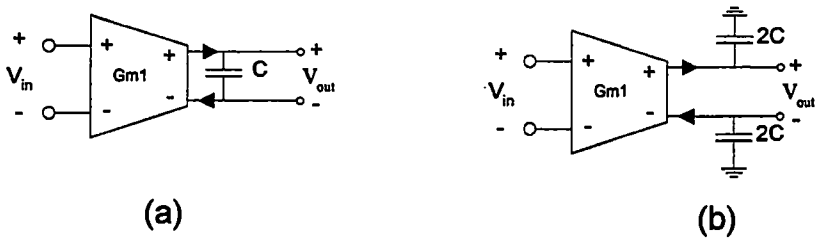


Figure 27. Fully differential integrators. (a) floating capacitor and (b) two grounded capacitors.

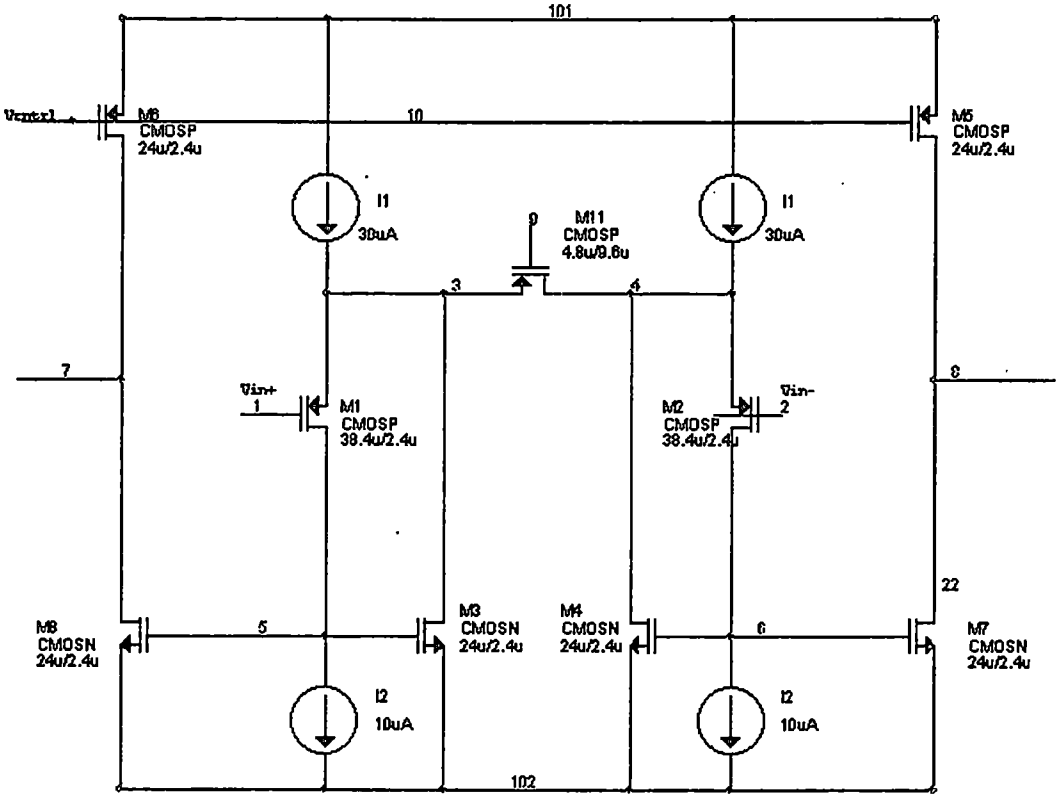


Figure 28. A simplified transconductor based on a triode region transistor.

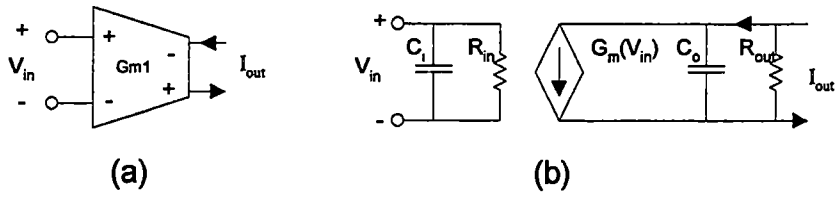


Figure 29. (a) Fully differential transconductor and (b) small signal equivalent circuit.

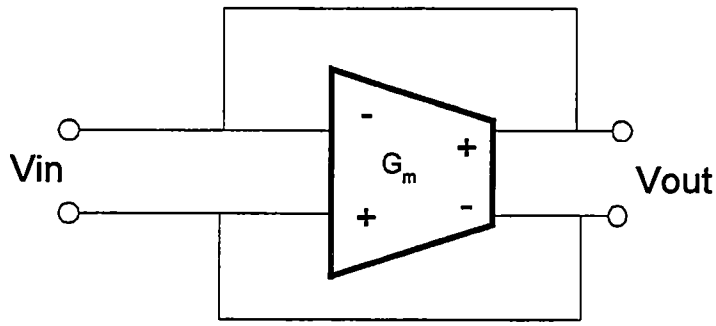
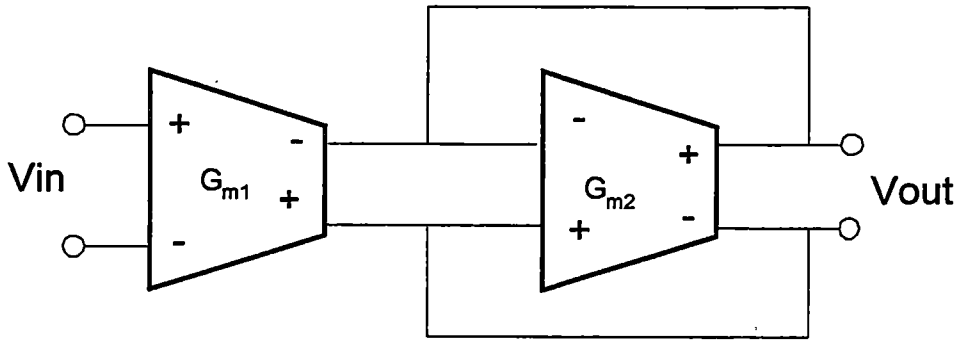


Figure 30. Transconductor connected to simulate a resistor of value $1/G_m$.



Second Transconductor Simulates a Resistor: $$R = \frac{1}{G_{m2}}$$

Voltage Gain: $$\frac{Vout}{Vin} = \frac{G_{m1}}{G_{m2}}$$

Figure 31. Transconductor gain circuit.

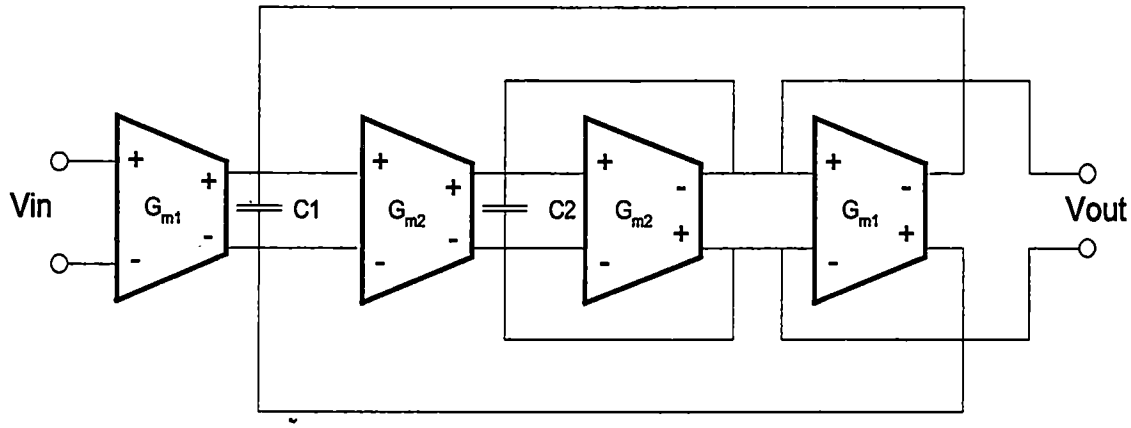


Figure 32. Biquad low-pass filter.

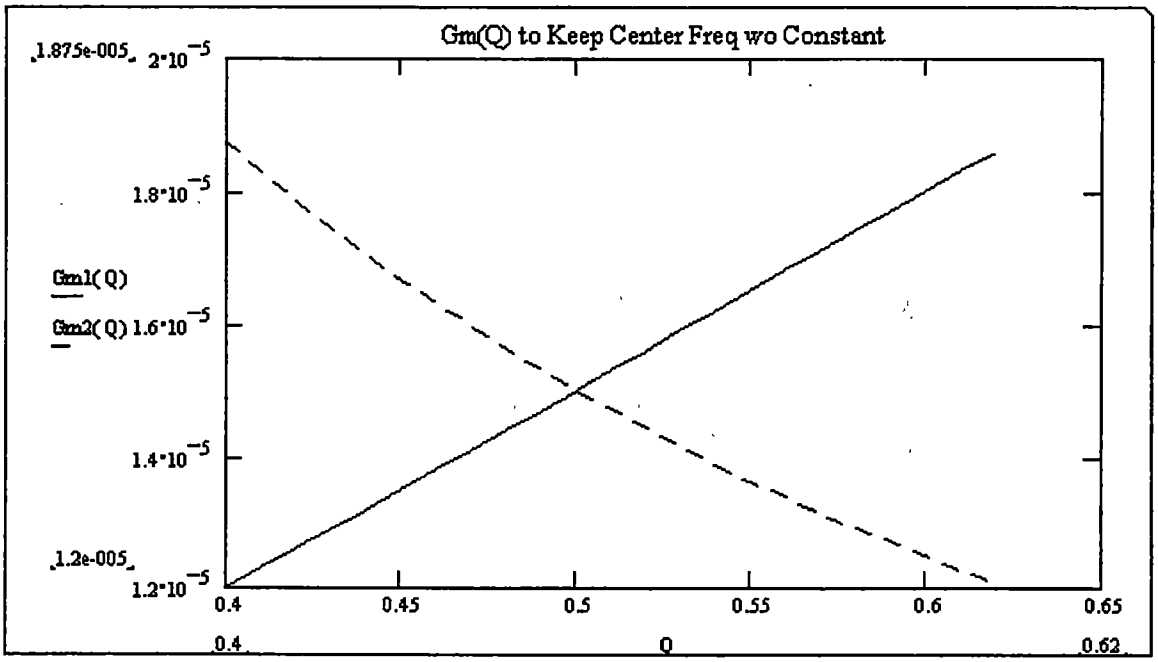


Figure 33. Example illustrating maintaining a constant ω_0 while adjusting Q. $G_{m1} \cdot G_{m2}$ product equals 225E-12.

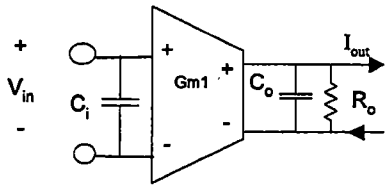
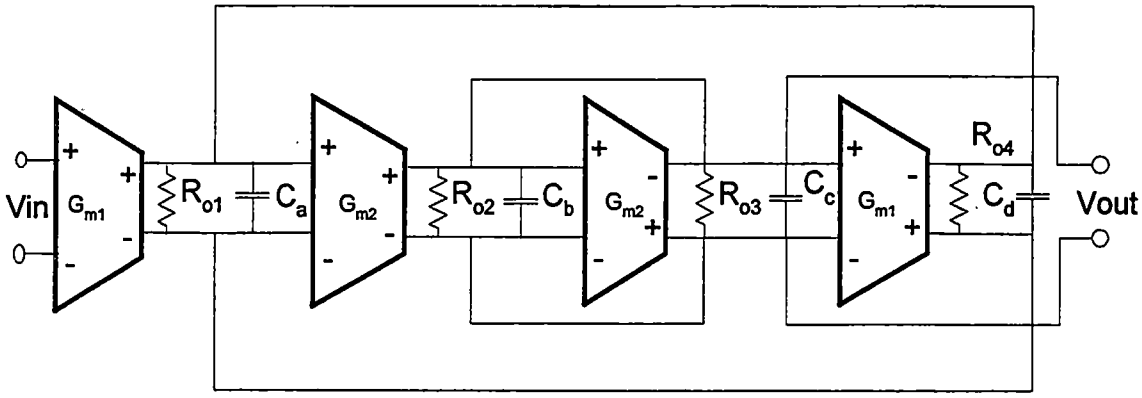
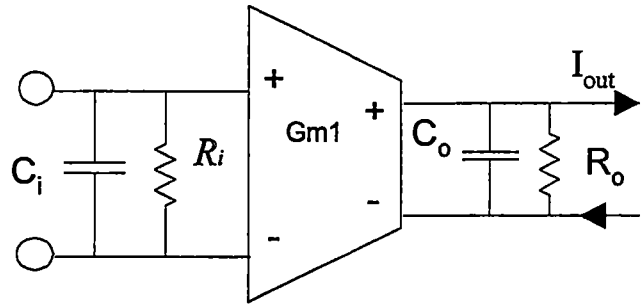


Figure 34. Transconductor with parasitic input and output impedances.

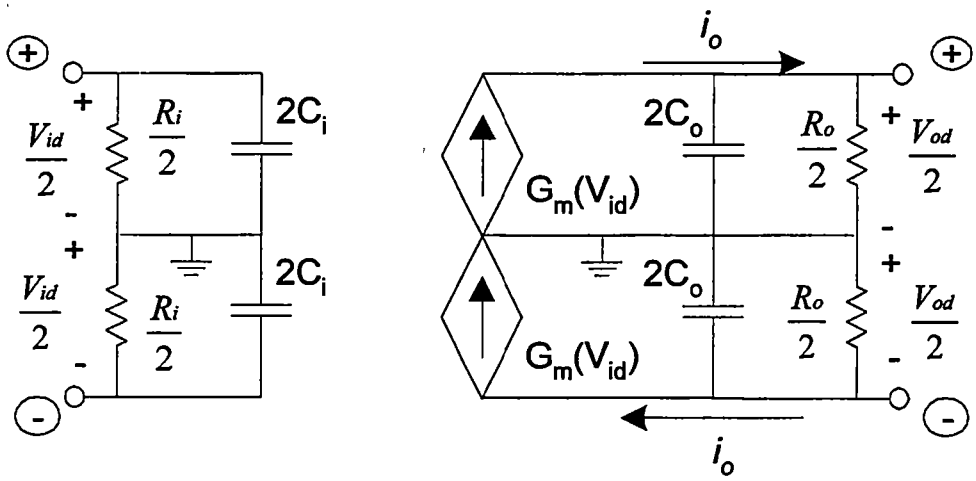


$$C_a = C_1 + C_{o1} + C_{in2} \qquad C_c = C_{o3} + C_{in4}$$
$$C_b = C_2 + C_{o2} + C_{in3} \qquad C_d = C_{o4}$$

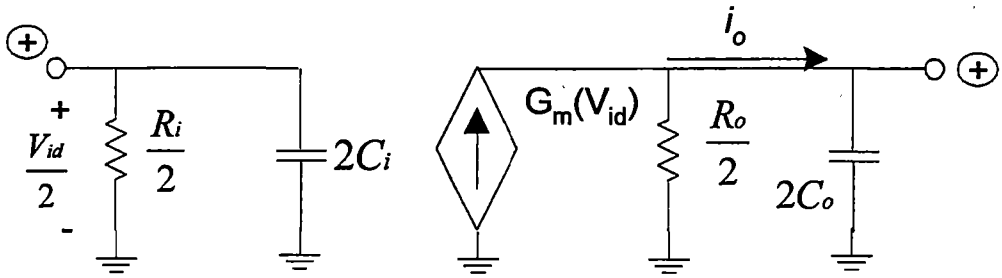
Figure 35. Biquad with parasitics.



Differential transconductor with parasitics

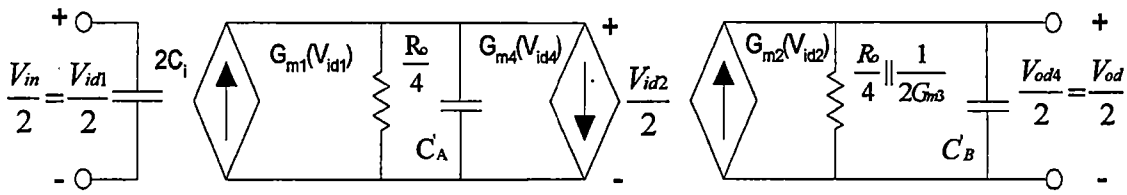


Differential transconductor equivalent circuit with parasitics



Transconductor half-mode circuit

Figure 36. Transconductor half mode circuit with parasitics.



$$C_i = C_{i1} = C_{i2} = C_{i3} = C_{i4} \qquad C_A' = 2C_1 + 4C_o + 2C_i$$

$$R_o = R_{o1} = R_{o2} = R_{o3} = R_{o4} \qquad C_B' = 2C_2 + 4C_o + 4C_i$$

$$C_o = C_{o1} = C_{o2} = C_{o3} = C_{o4}$$

Figure 37. Simplified biquad feedback network with parasitics.

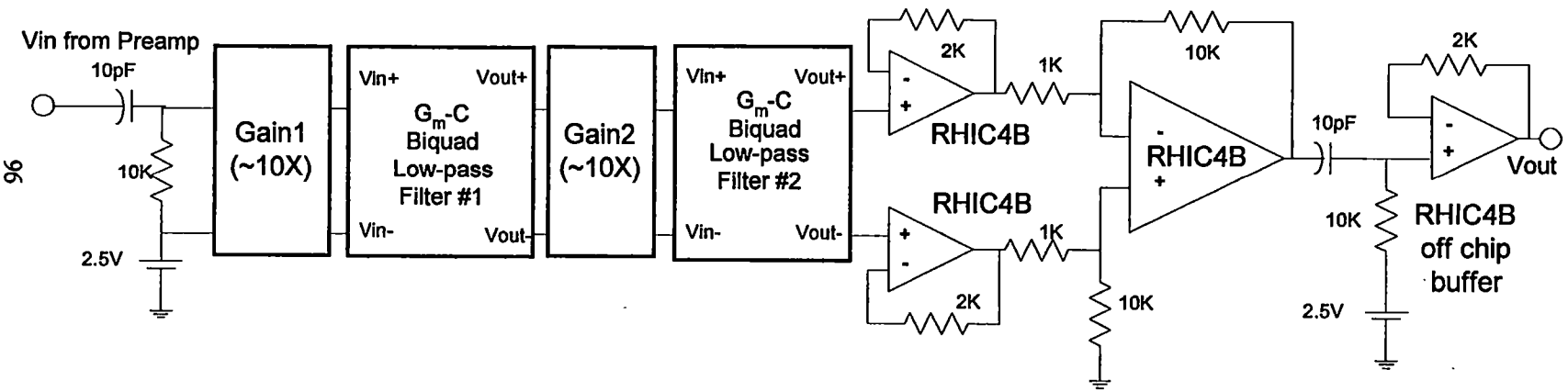


Figure 38. Implemented shaper block diagram.

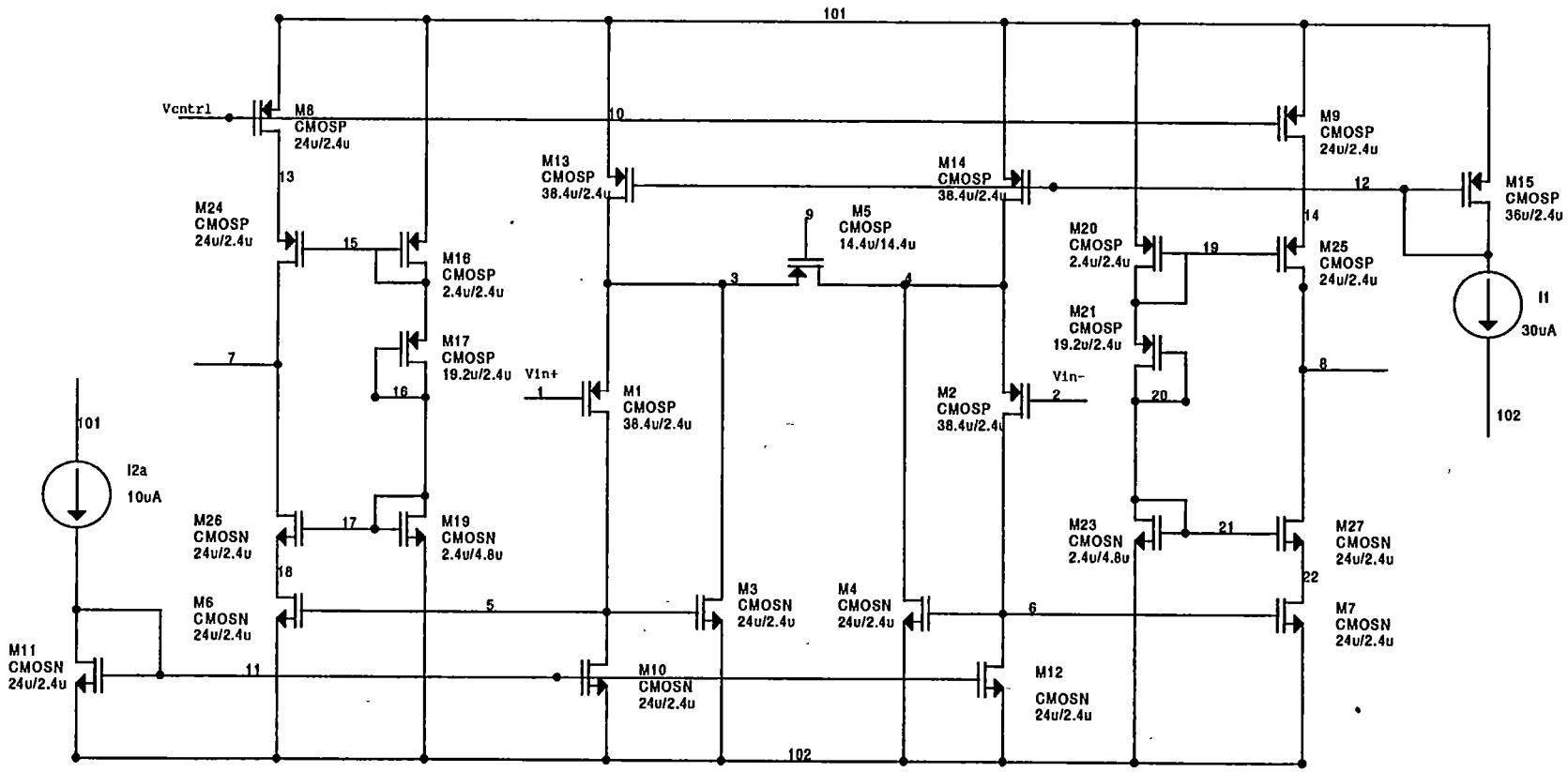


Figure 39. Triode Region transconductor circuit.

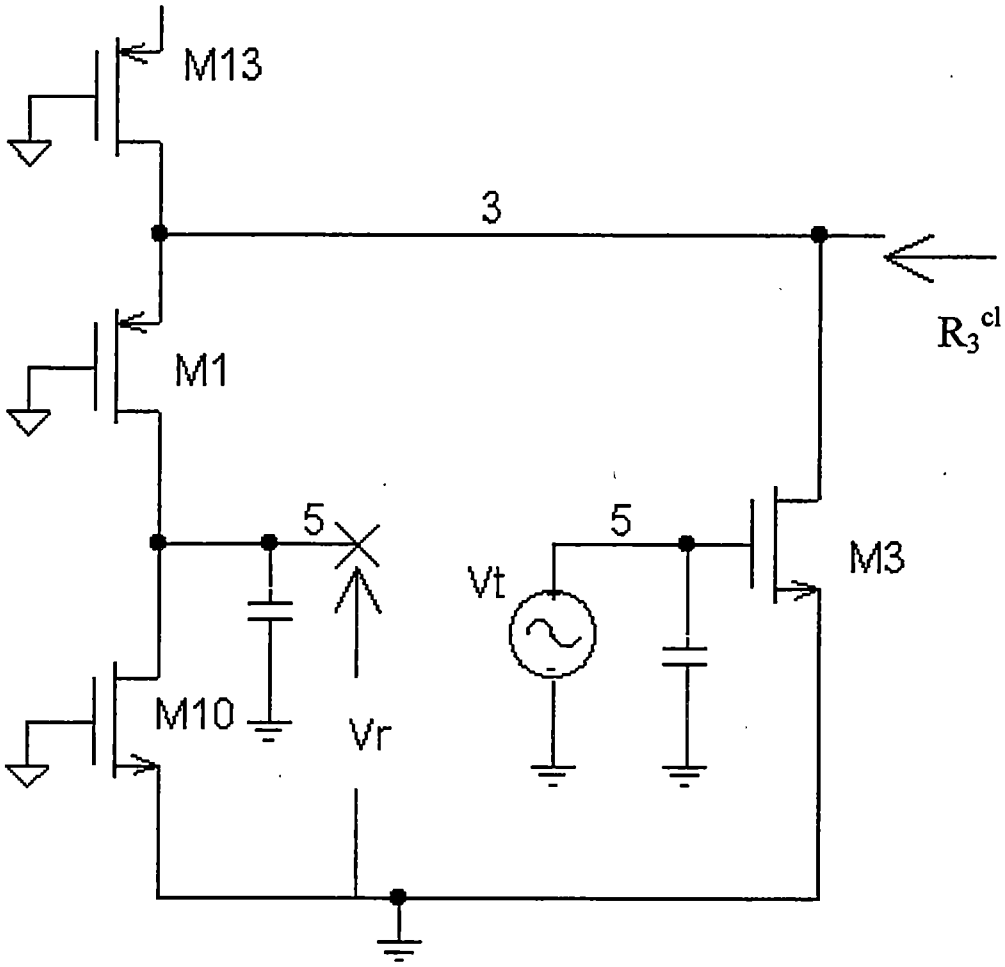


Figure 40. Transconductor local feedback loop transmission calculation.

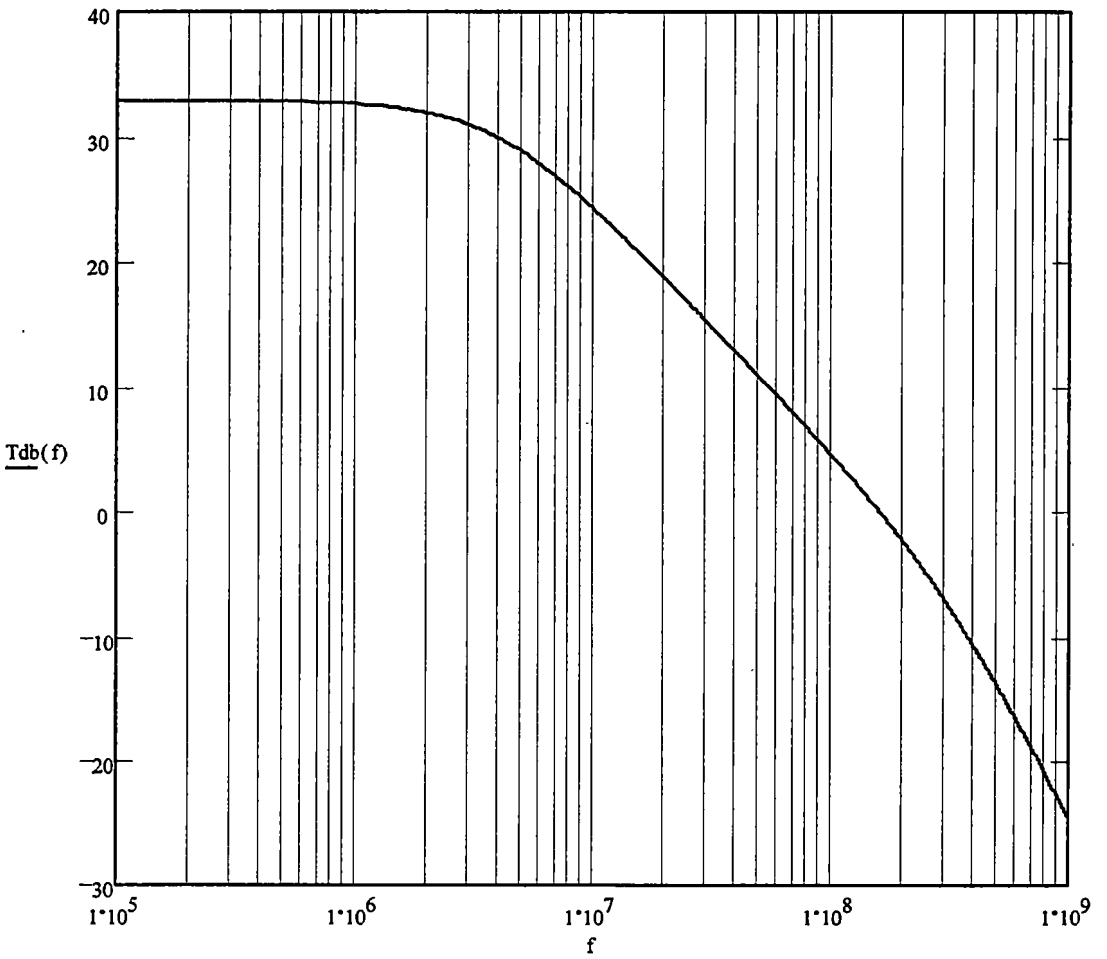


Figure 41. Local feedback loop transmission -|*T(f)*| db (hand calculation).

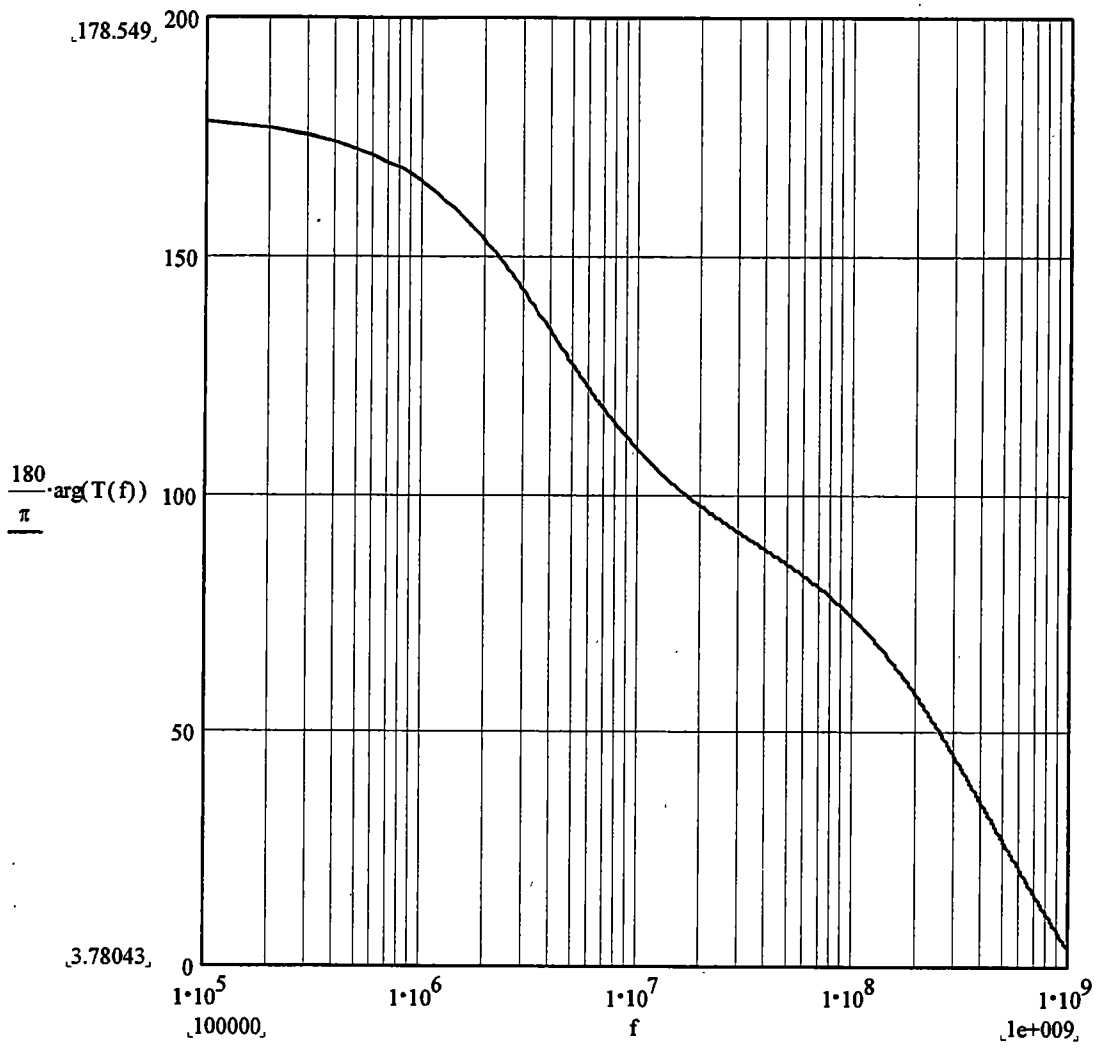


Figure 42. Local feedback loop transmission -*T(f)* phase (hand calculation).

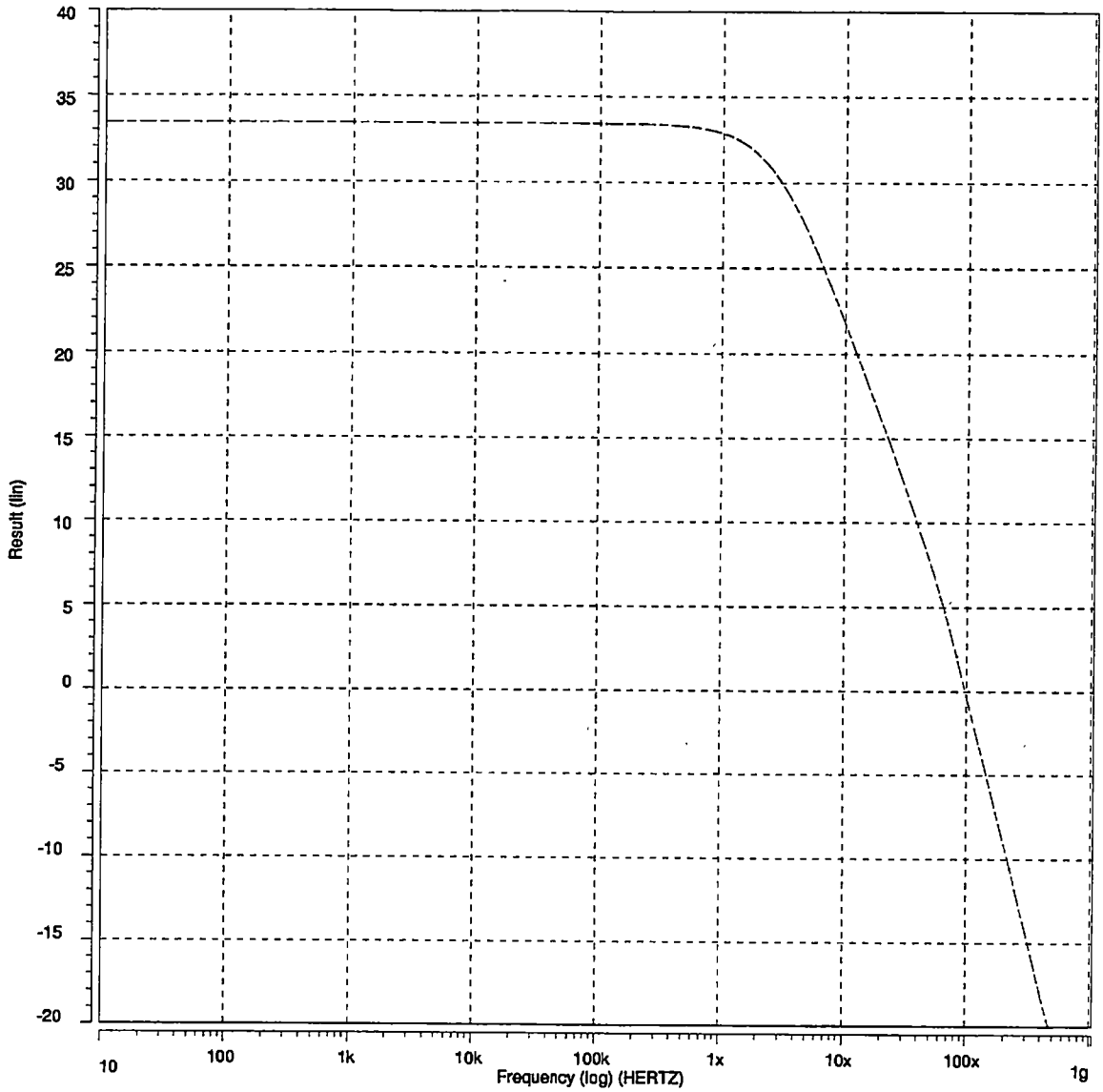


Figure 43. Local feedback loop transmission - $|T(f)|$ dB (SPICE simulation results; V_C=0.5V; N86O process model).

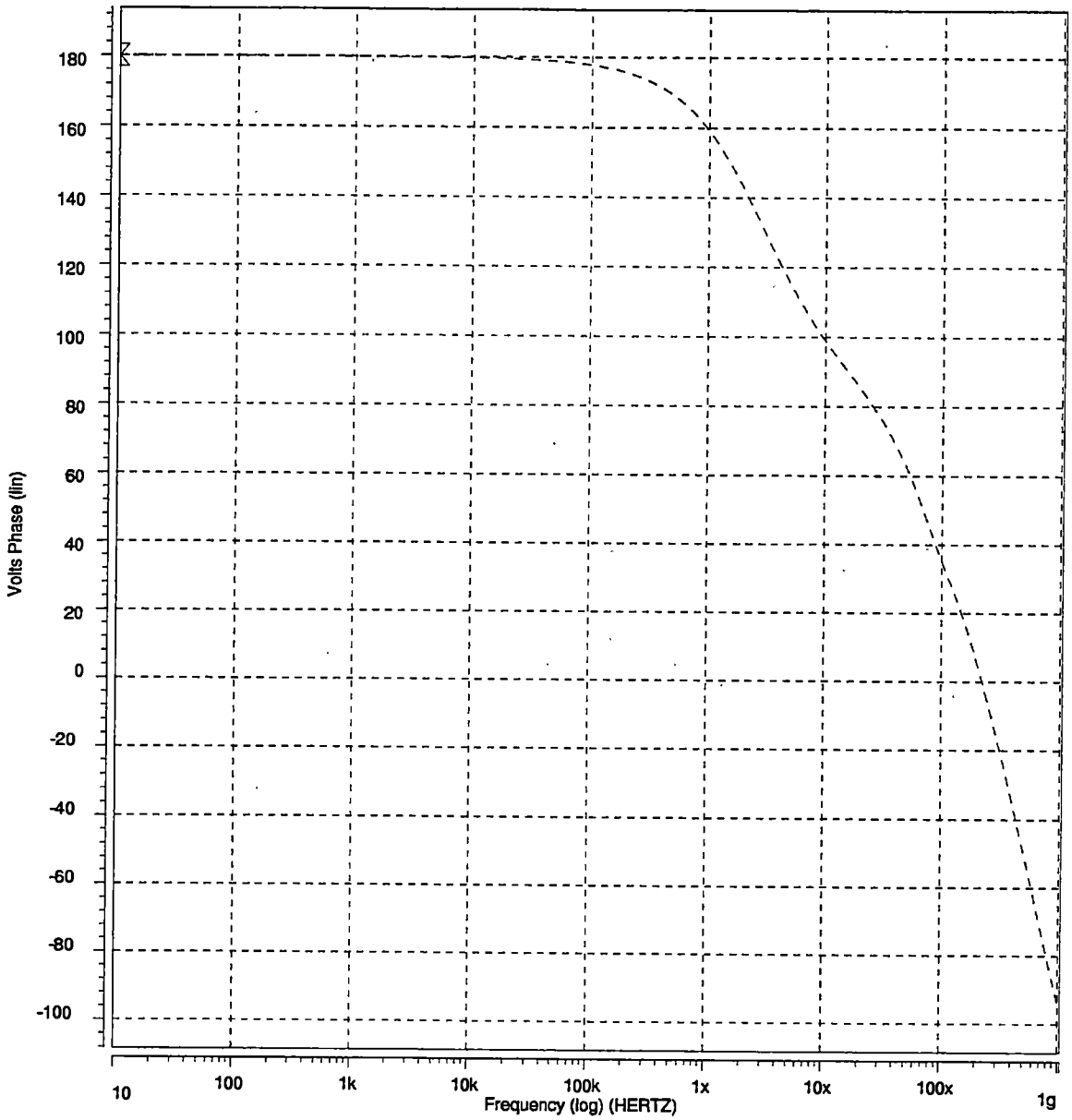


Figure 44. Local feedback loop transmission - *T(f)* phase (SPICE simulation results; V_c=0.5V; N86O process model).

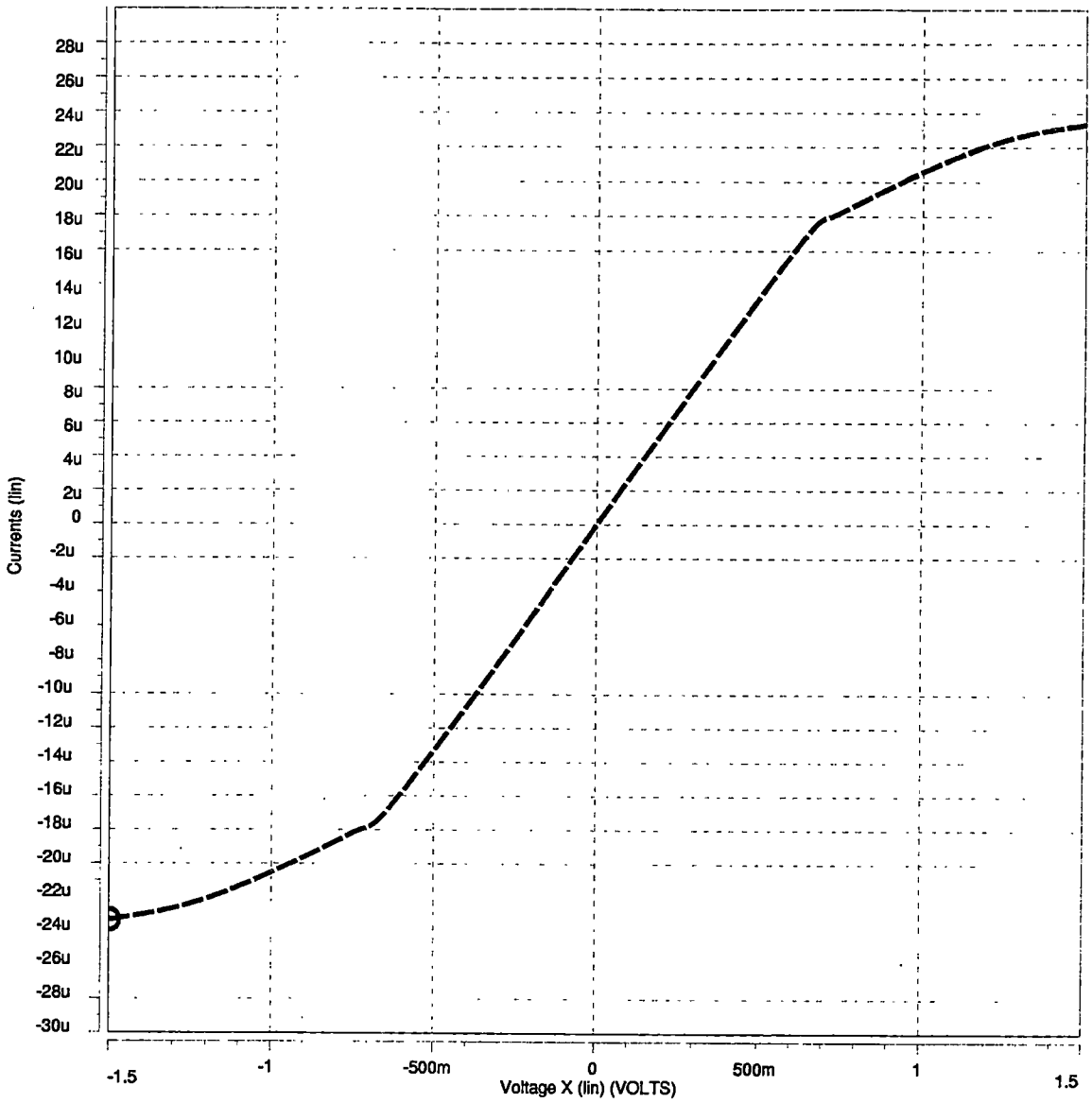


Figure 45. Transconductor $I_{out}(V_{diff})$ for a differential input signal ranging from - 1.5V to +1.5V (V_c=0.5V; N86O process model; Outputs held at 2.5V).

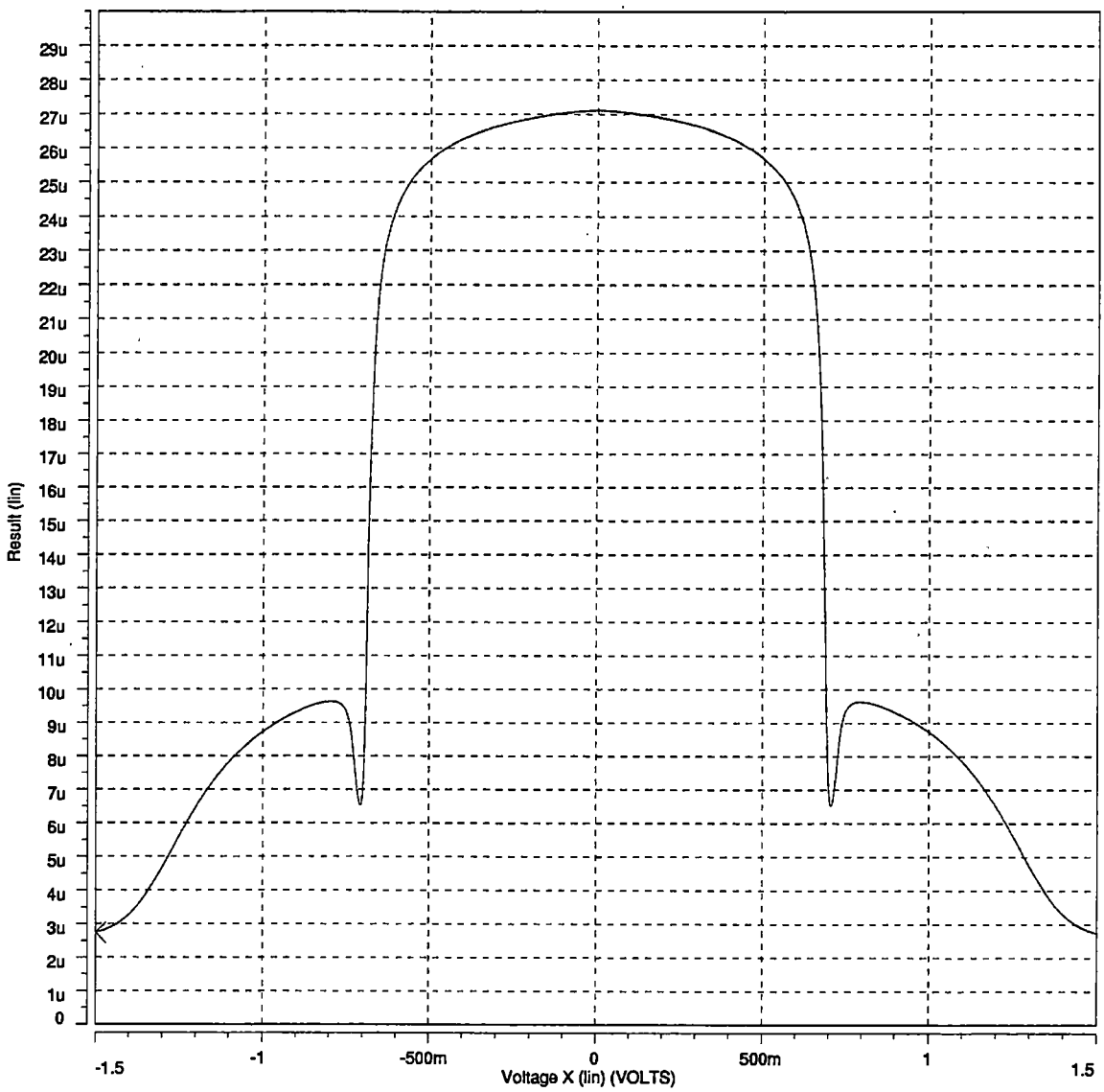


Figure 46. Transconductor $G_m(V_{diff})$ for a differential input signal ranging from - 1.5V to +1.5V (V_c=0.5V; N86O process model; Outputs held at 2.5V).

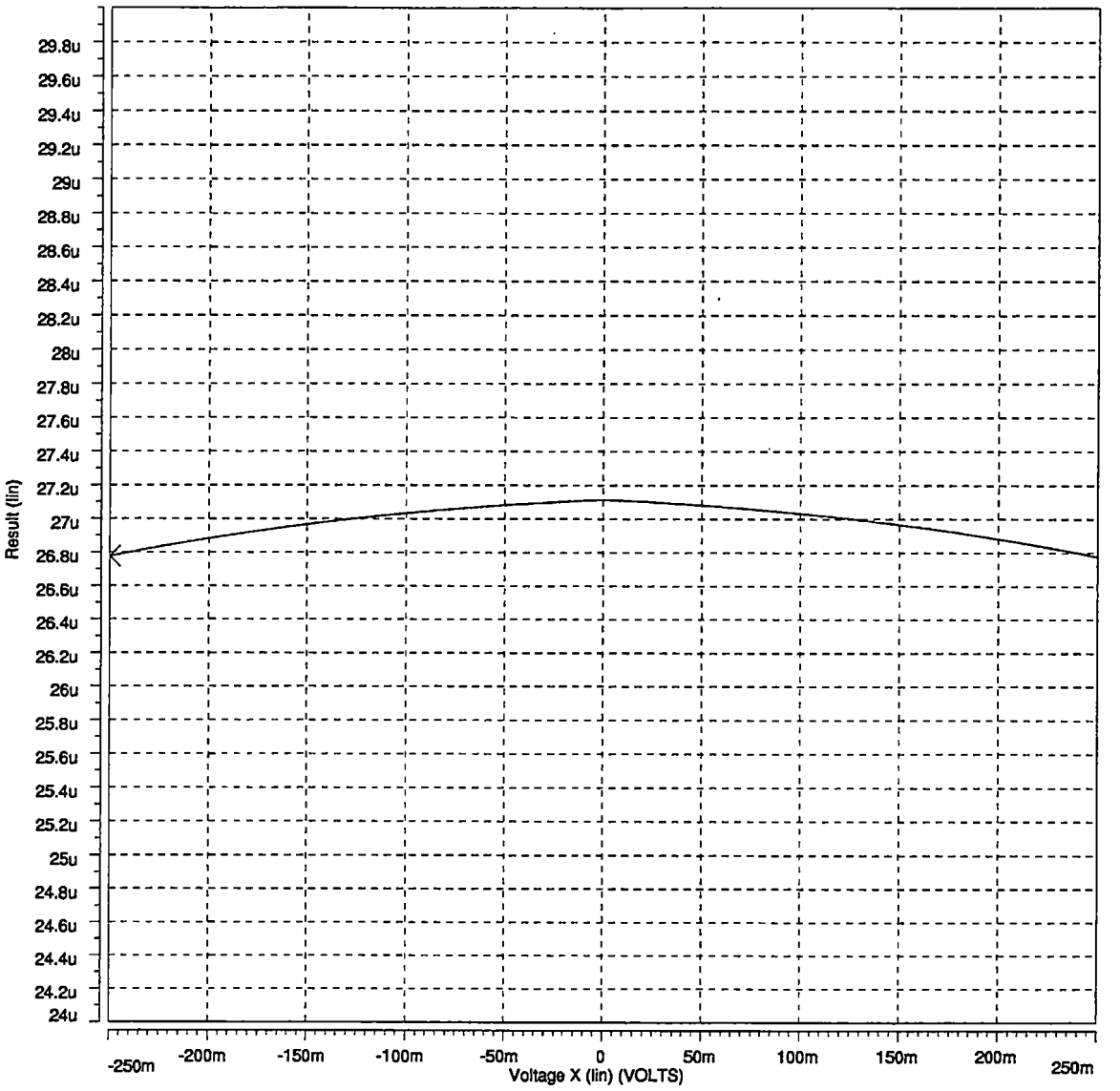


Figure 47. Transconductor $G_m(V_{diff})$ for V_{diff}=± 250mV. ~1.24% Variation in G_m (V_c=0.5V; N86O process model).

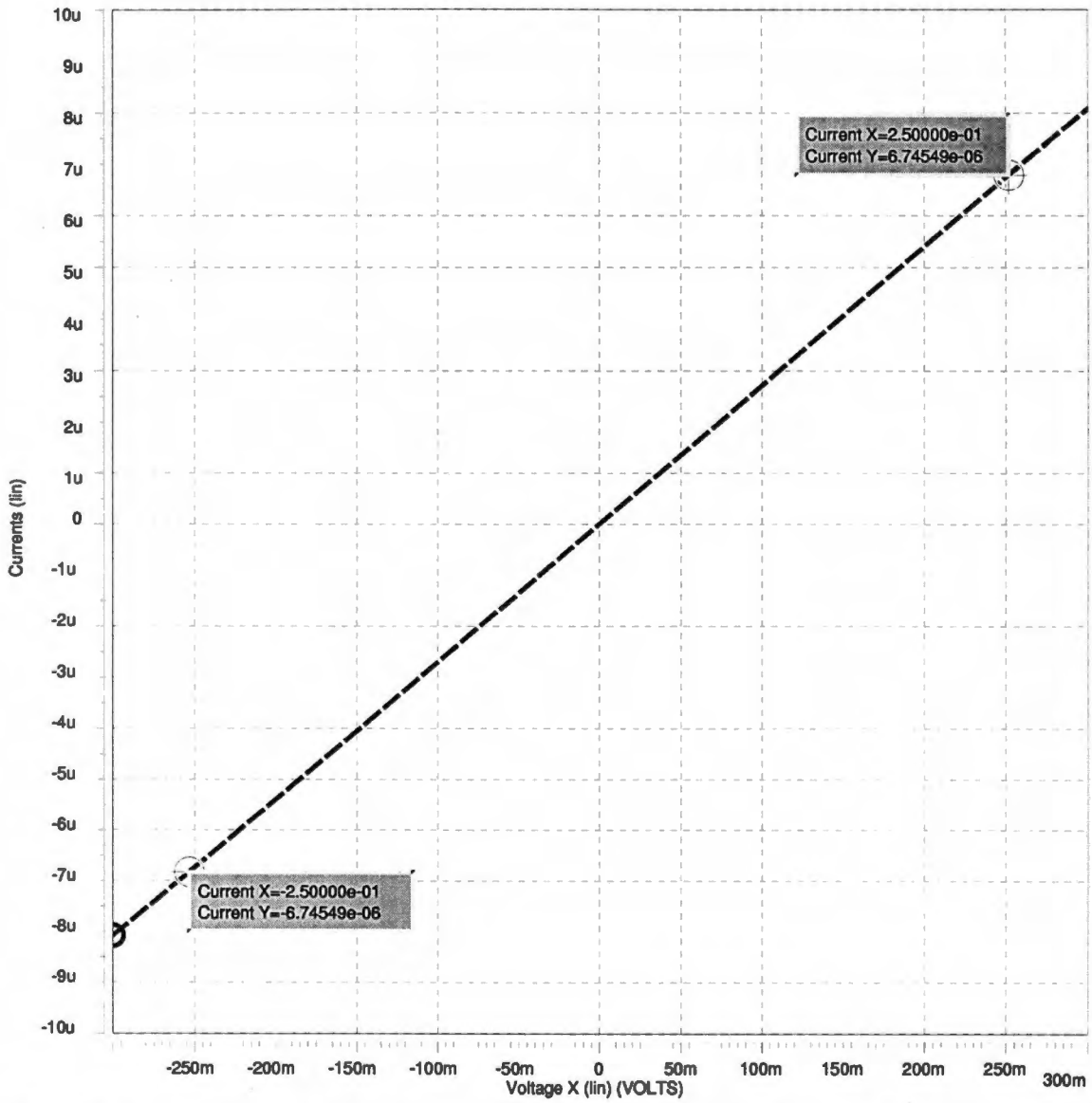


Figure 48. Transconductor $I_{out}(V_{diff})$ for V_{diff}=± 250mV demonstrating nearly perfect linearity (V_c=0.5V; N86O process model). Variation at V_{diff}=± 250mV is ~0.5% from a perfectly linear response.

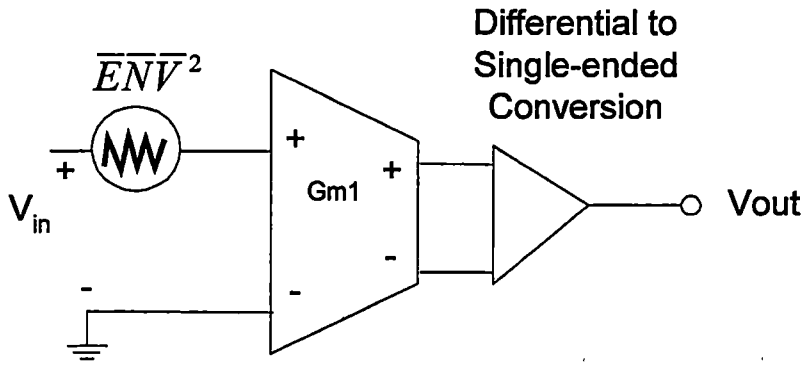


Figure 49. Transconductor model used to calculate the equivalent input noise voltage.

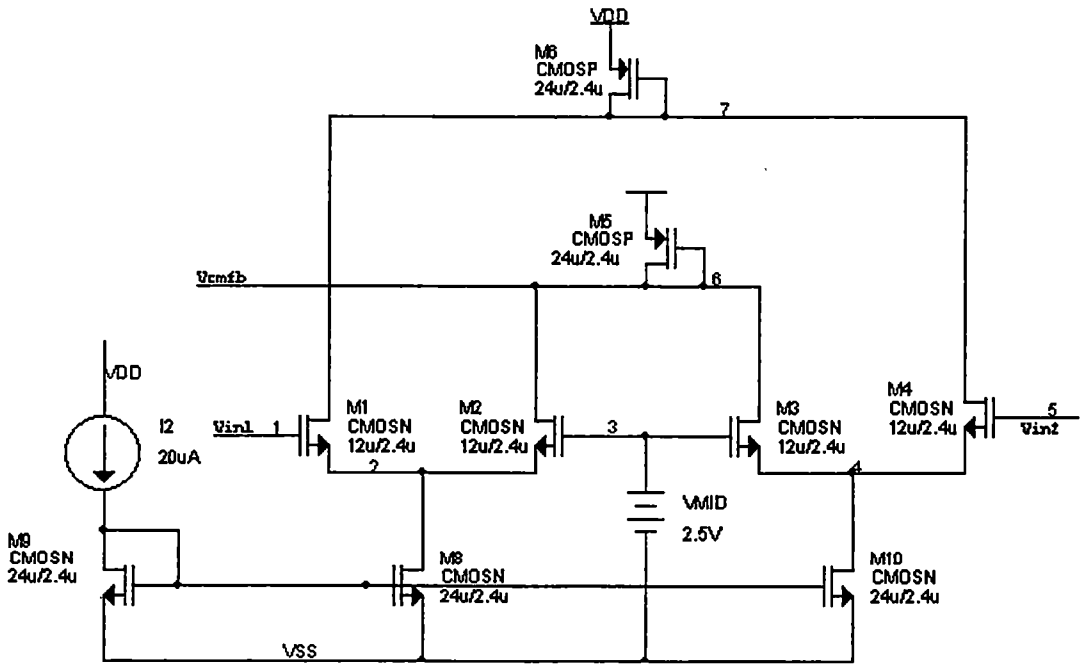


Figure 50. Common mode feedback circuit.

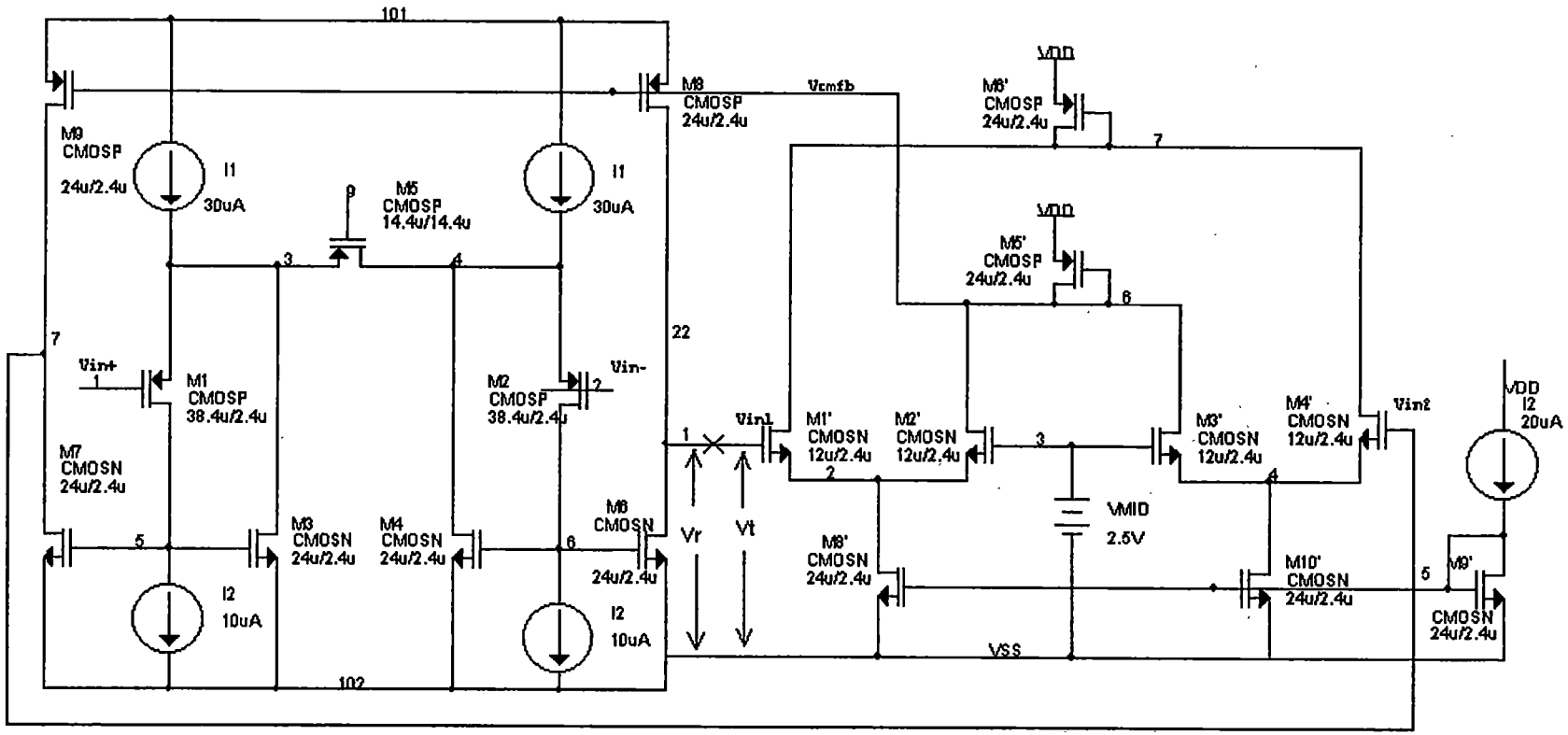


Figure 51. Common mode feedback loop through transconductor. Using simplified transconductor.

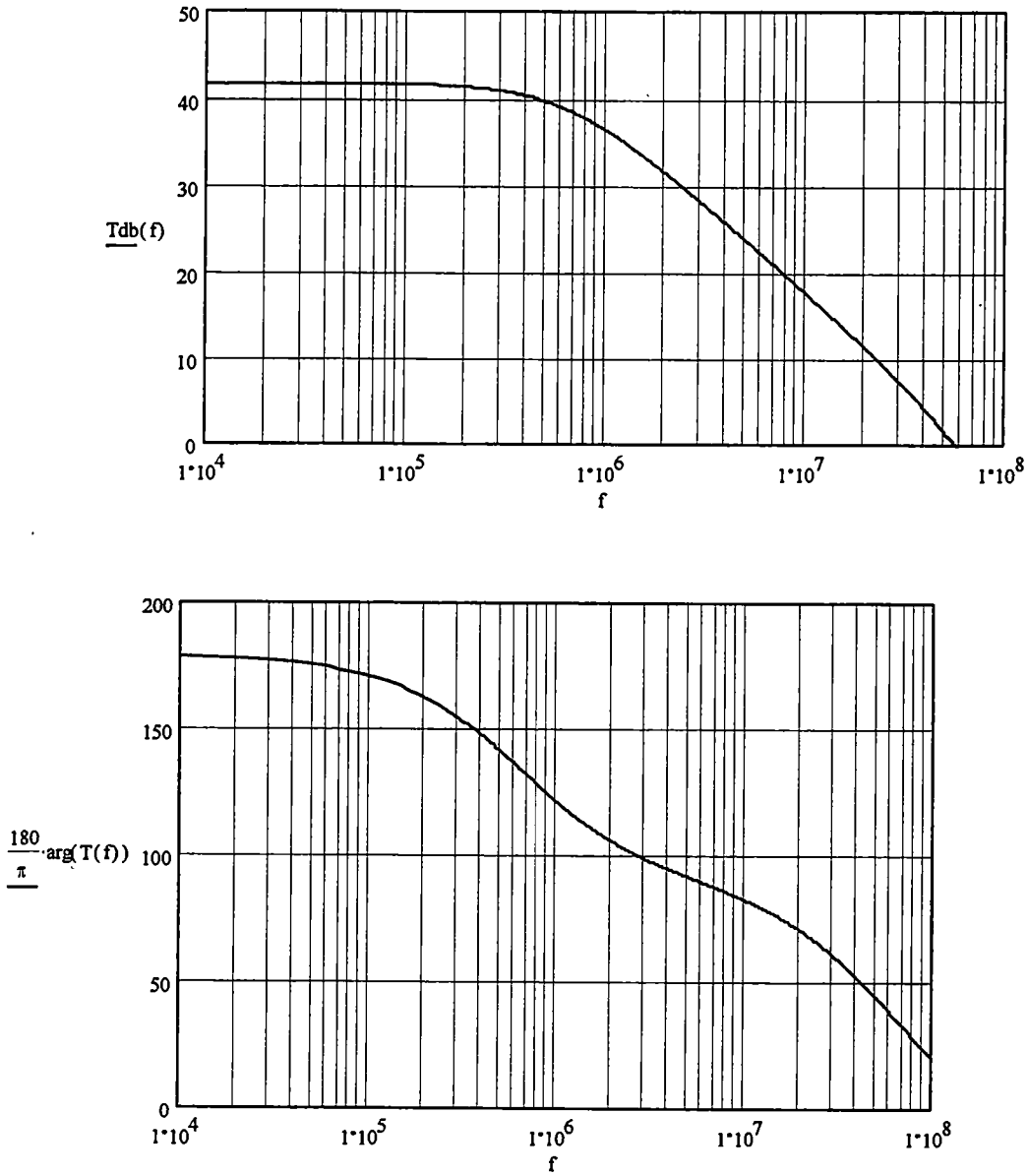


Figure 52. Common mode feedback loop transmission for the gain cell (parasitics from layout ignored). The top graph shows $|T(f)|$ in dB and the bottom graph shows the phase of $T(f)$.

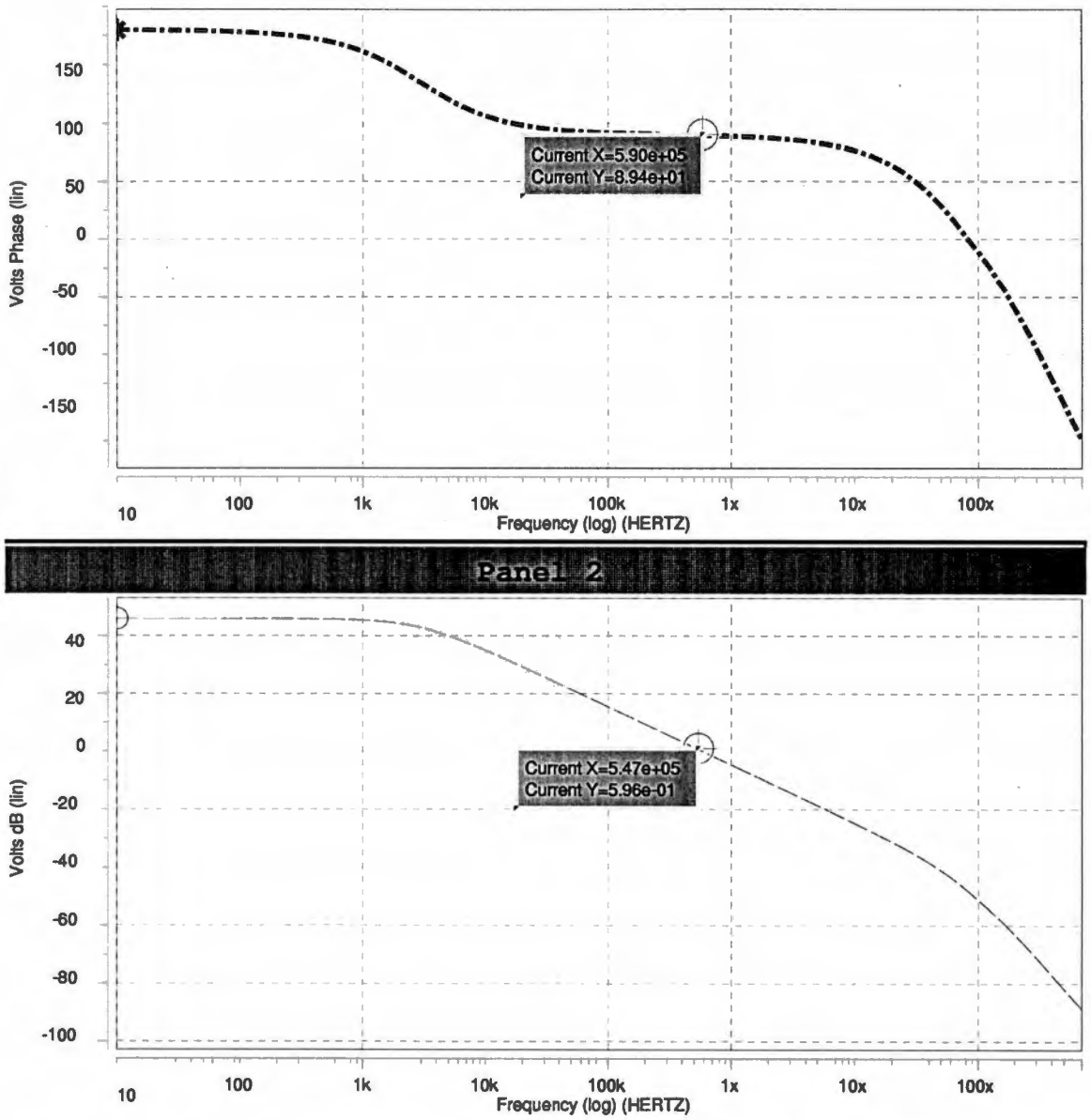


Figure 53. Common mode feedback loop magnitude (dB) and phase for filter capacitor C_f=6.1pF (capacitance to ground $2C_f$=12.2pF). PM=90°.

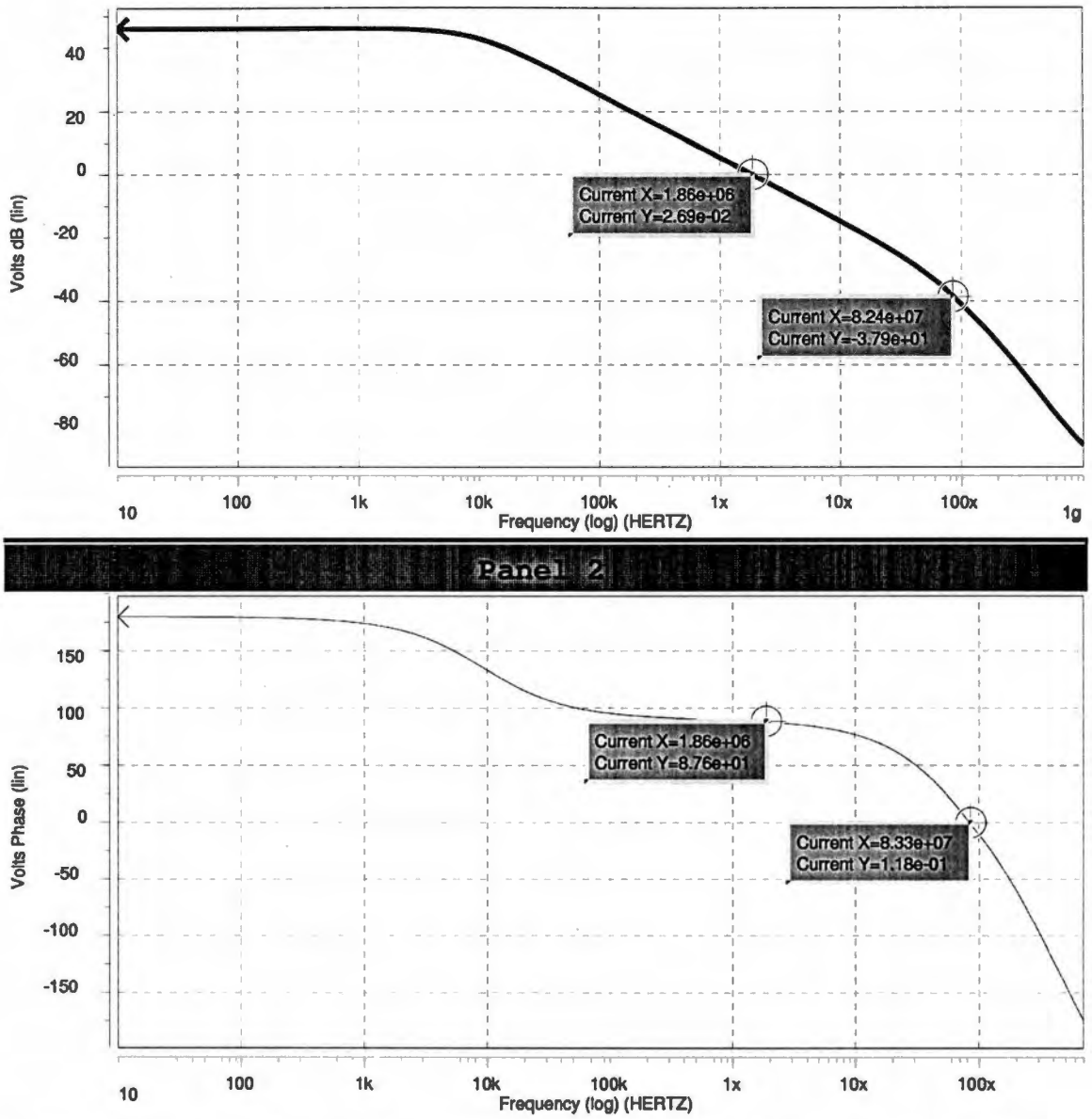


Figure 54. Common mode feedback loop magnitude (dB) and phase for filter capacitor C_2=1.9pF (capacitance to ground $2C_2$=3.8pF). PM=90°.

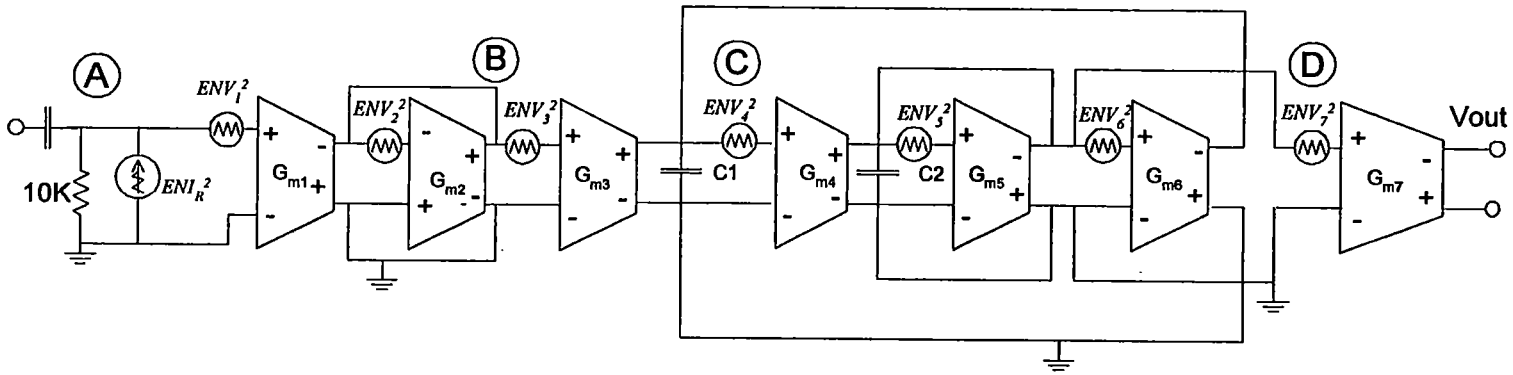


Figure 55.Dominant noise sources in the shaper (first gain and biquad stages and the first transconductor in the second gain stage).

MOSIS PARAMETRIC TEST RESULTS

RUN: N86O VENDOR: AMI

TECHNOLOGY: SCN12 FEATURE SIZE: 1.2 microns

COMMENTS: American Microsystems, Inc. 1.2 micron ABN.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	1.8/1.2			
Vth		0.73	-1.01	Volts
SHORT	10.8/1.2			
Idss		194	-95	uA/um
Vth		0.61	-0.84	Volts
Vpt		10.0	-14.5	Volts
WIDE	30/1.2		-8.2	Volts
Ids0		0.6	-9.4	pA/um
LARGE	10.8/10.8			
Vth		0.65	-0.83	Volts
Vjbkd		17.2	-15.2	Volts
Ijlk		-3.7	-1.4	pA
Gamma		0.62	0.77	V^0.5
Delta length (L_eff = L_drawn-DL)		0.32	0.15	microns
Delta width (W_eff = W_drawn-DW)		1.39	1.48	microns
K' (Uo*Cox/2)		35.0	-11.6	uA/V^2

Figure 56. MOSIS process parameters used in pre-fabrication design (N86O process data).

MOSIS PARAMETRIC TEST RESULTS

RUN: N91A VENDOR: AMI

TECHNOLOGY: SCN12 FEATURE SIZE: 1.2 microns

COMMENTS: American Microsystems, Inc. 1.2 micron ABN.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	1.8/1.2			
Vth		0.72	-1.04	Volts
SHORT	10.8/1.2			
Idss		203	-102	uA/um
Vth		0.65	-0.84	Volts
Vpt		10.0	-14.2	Volts
WIDE	30/1.2		-6.1	Volts
Ids0		0.6	-469.6	pA/um
LARGE	10.8/10.8			
Vth		0.69	-0.84	Volts
Vjbkd		16.9	-15.0	Volts
Ijlk		-32.8	-10.0	pA
Gamma		0.71	0.94	V^0.5
K' (Uo*Cox/2)		34.4	-12.8	uA/V^2

Figure 57. MOSIS process parameters for the protoype shaper run (N91A process data).

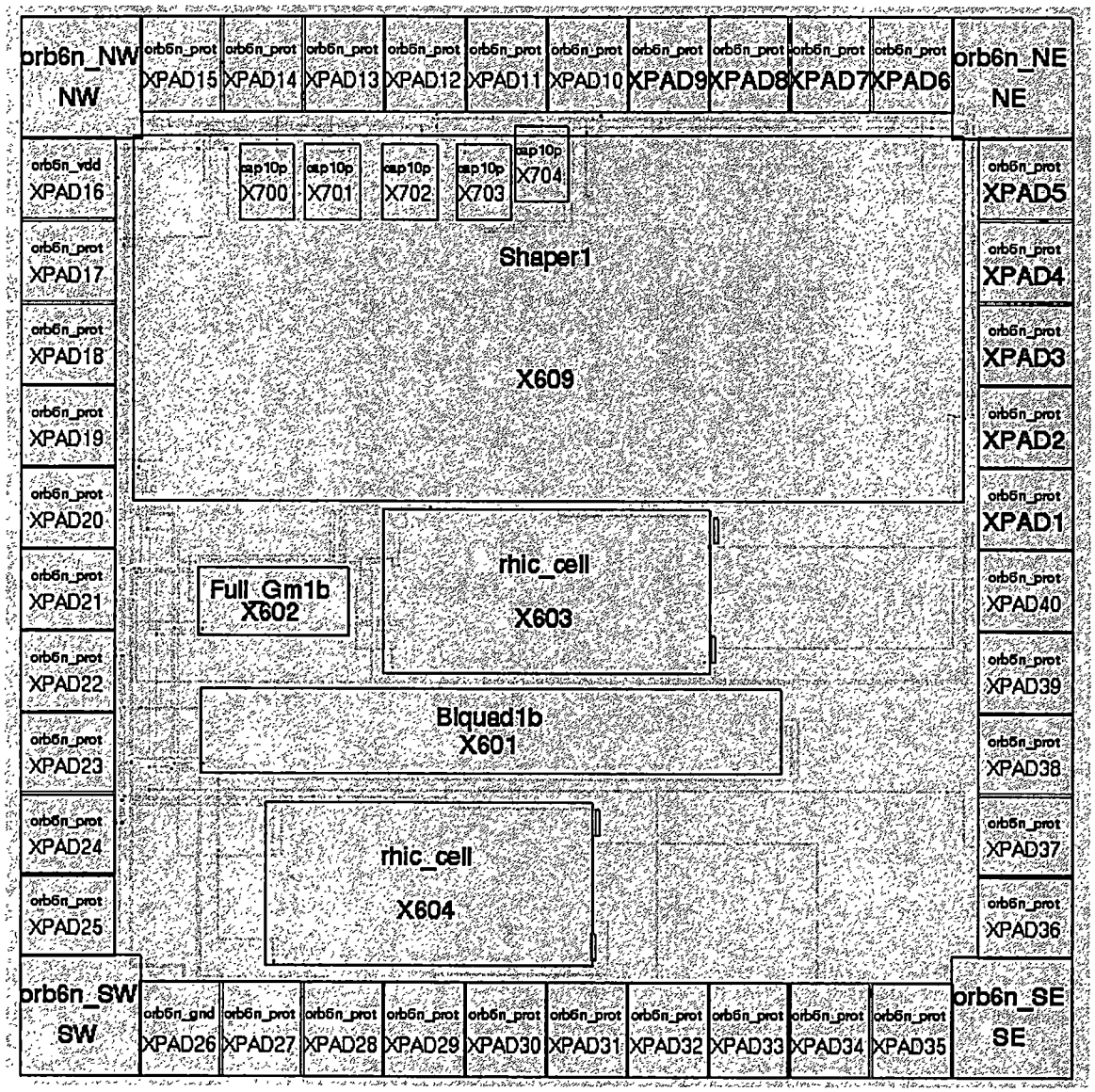


Figure 58. Prototype pulse shaper chip layout, block view.

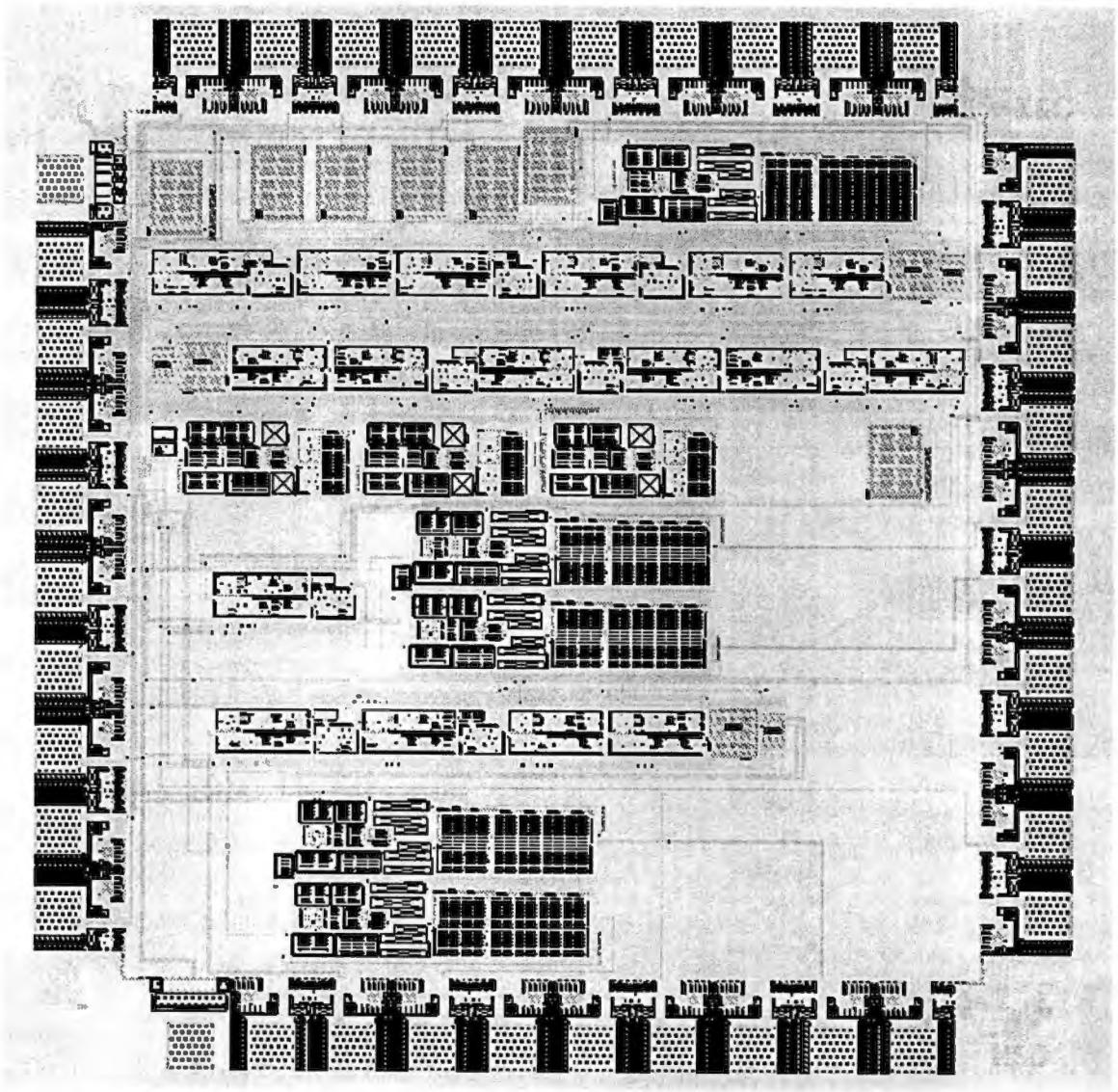


Figure 59. Prototype pulse shaper chip layout, expanded view.

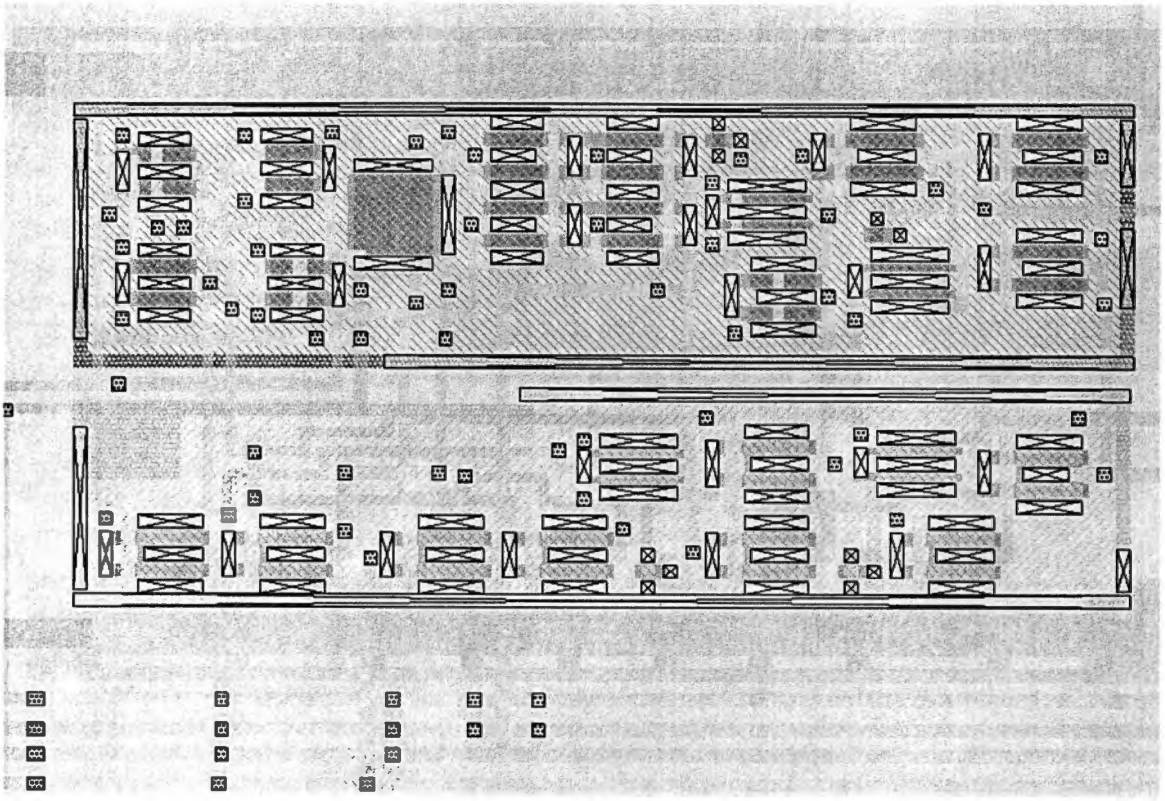


Figure 60. Transconductor circuit layout.

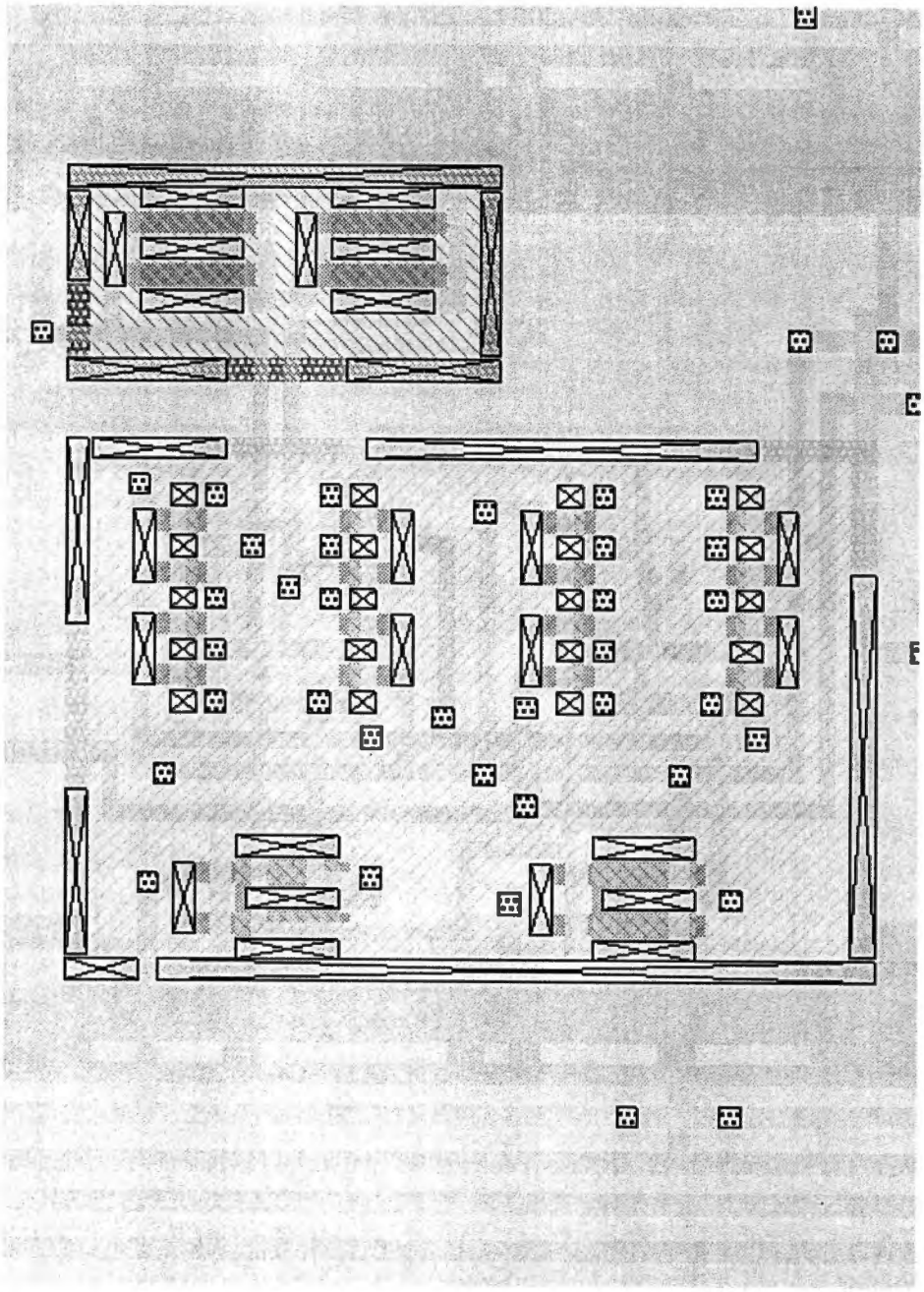


Figure 61. Common mode feedback circuit layout.

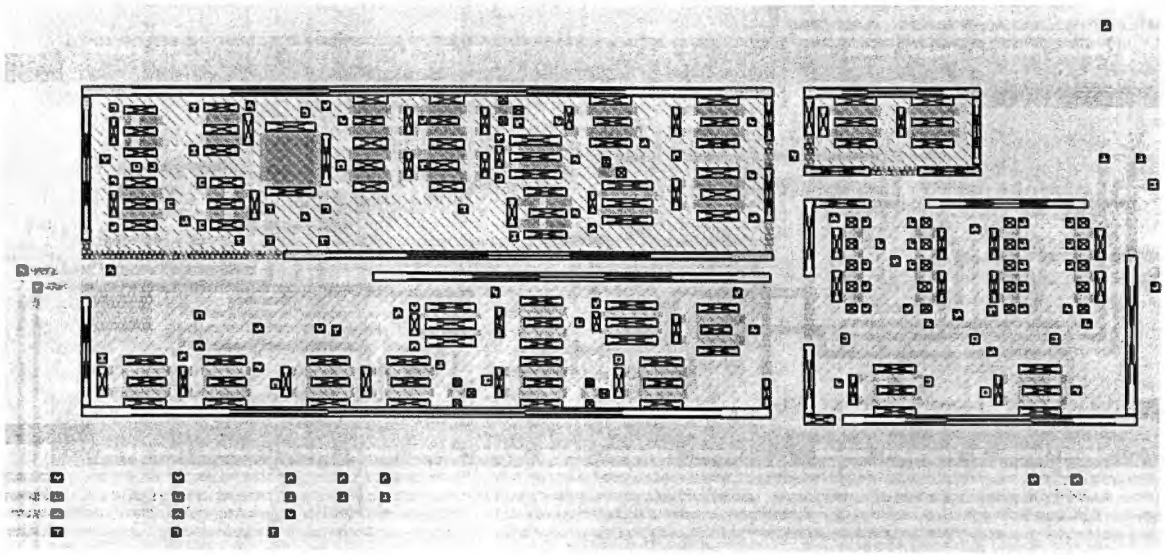


Figure 62. Transconductor and common mode feedback circuit connected in series.

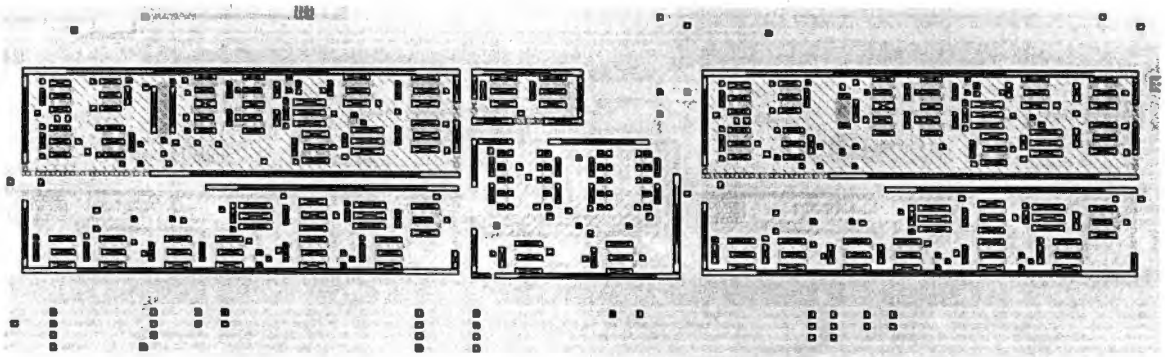


Figure 63. Transconductor based gain cell. Two transconductors and one common mode feedback circuit.

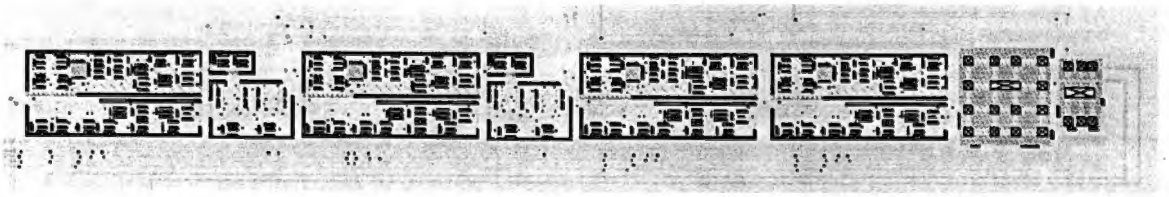


Figure 64. Transconductor based biquad filter.

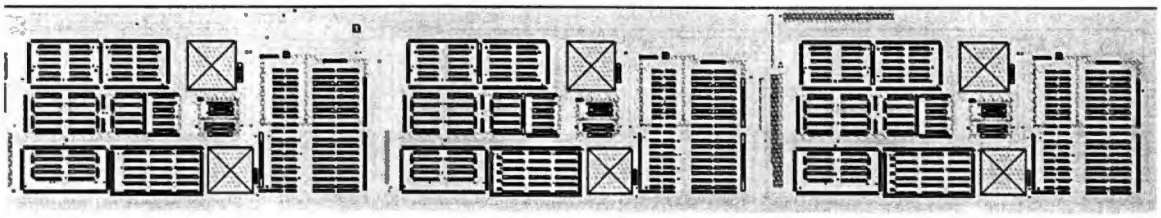


Figure 65. RHIC4B based differential to single-ended conversion.

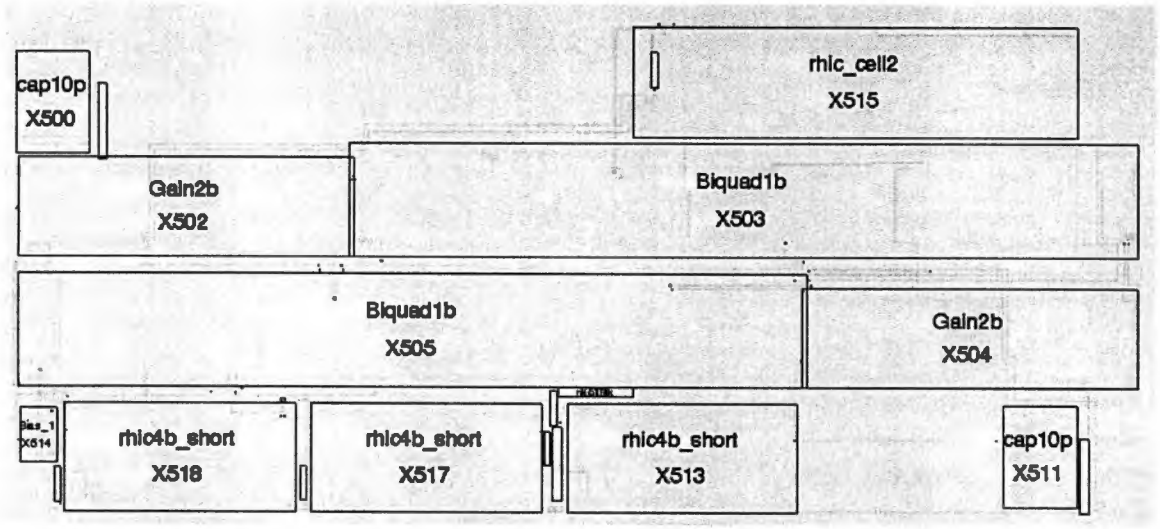


Figure 66. G_m-C based pulse shaping amplifier with RHIC4B off chip driver block diagram.

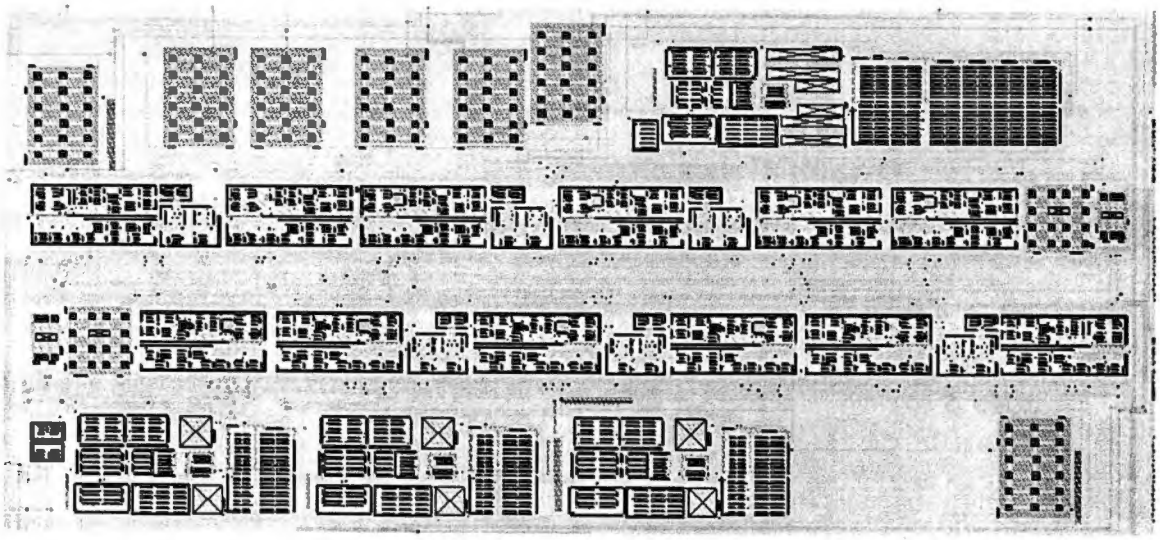


Figure 67. G_m-C based pulse shaping amplifier with RHIC4B off chip driver and bias line filter capacitors.

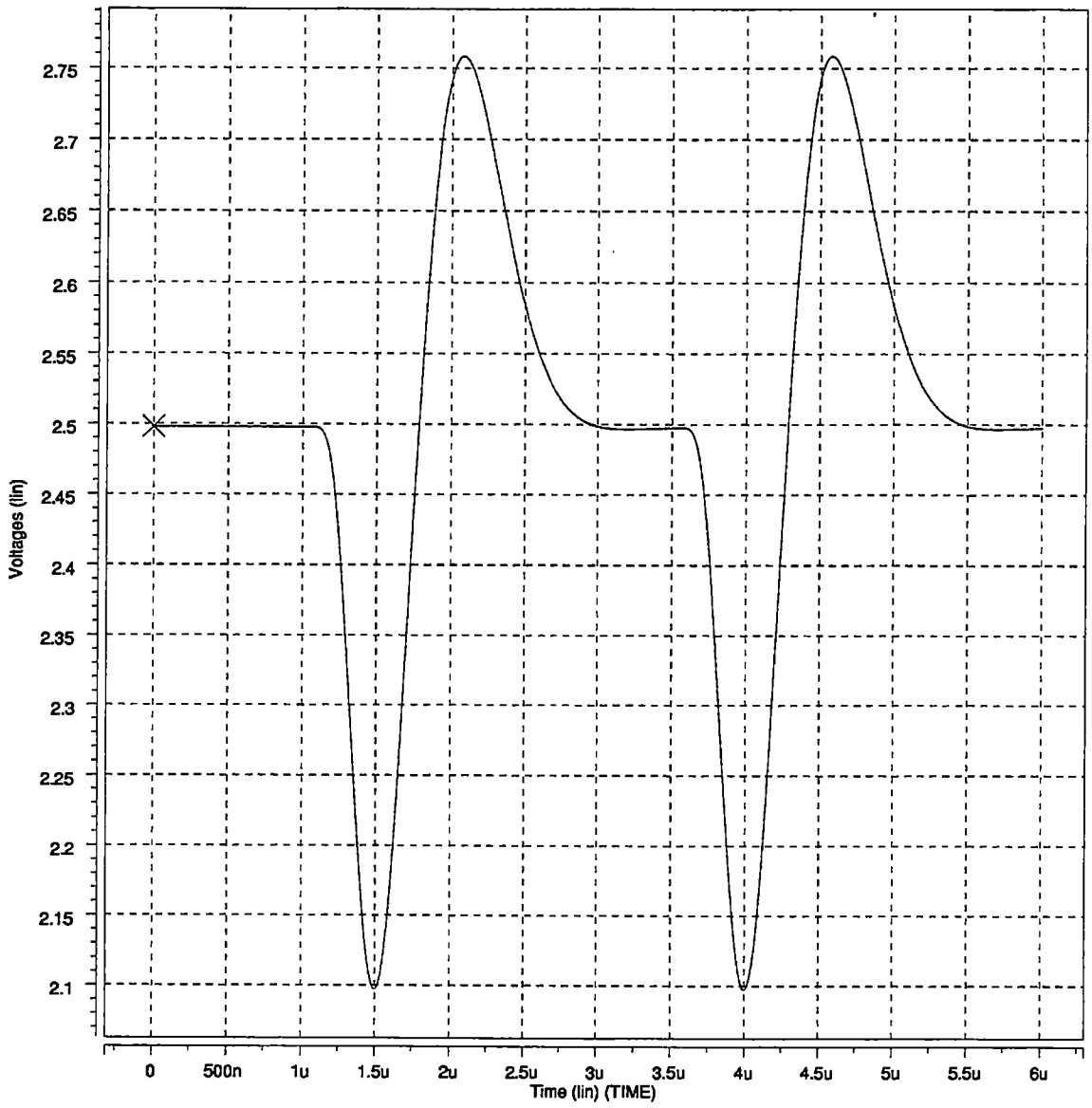


Figure 68. Prototype pulse shaper simulation using AMI N86O BSIM3 v3.1 model.

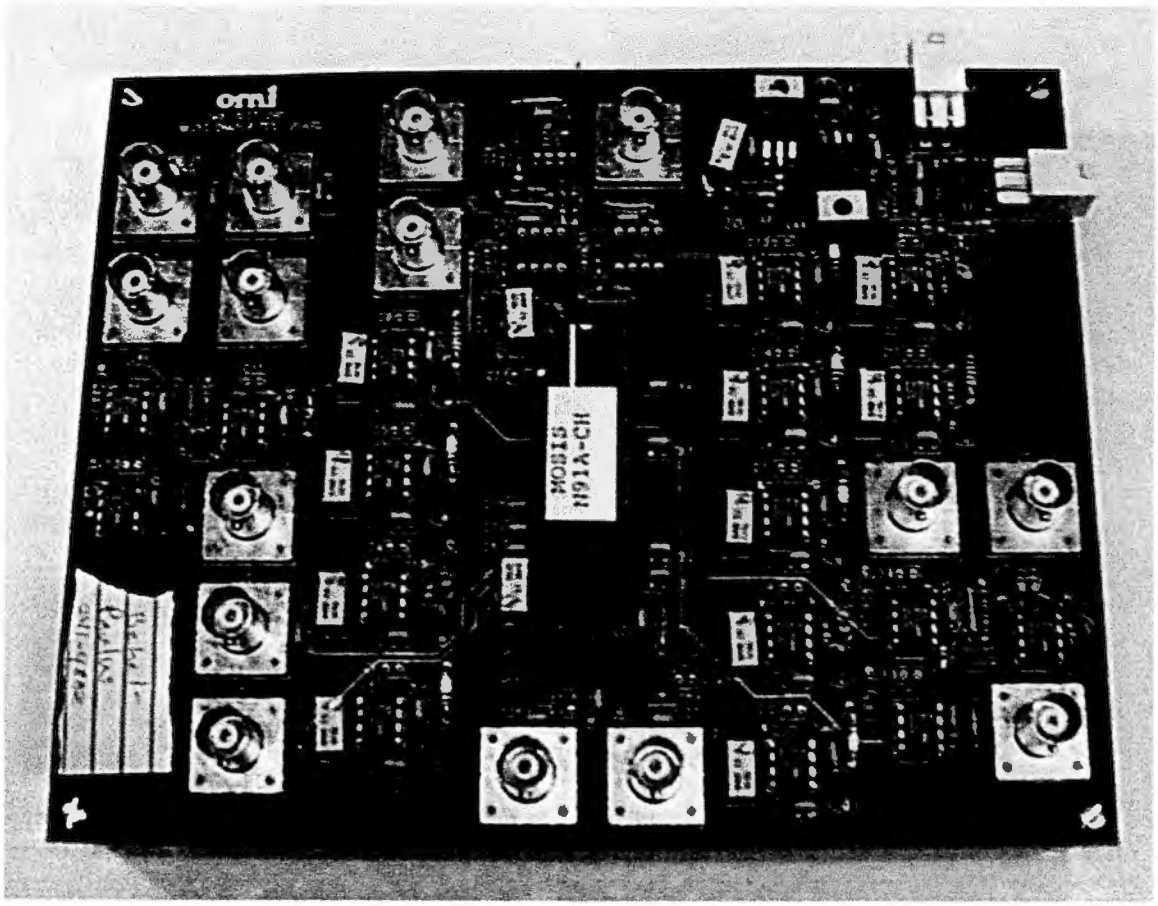


Figure 69. Prototype chip test board.

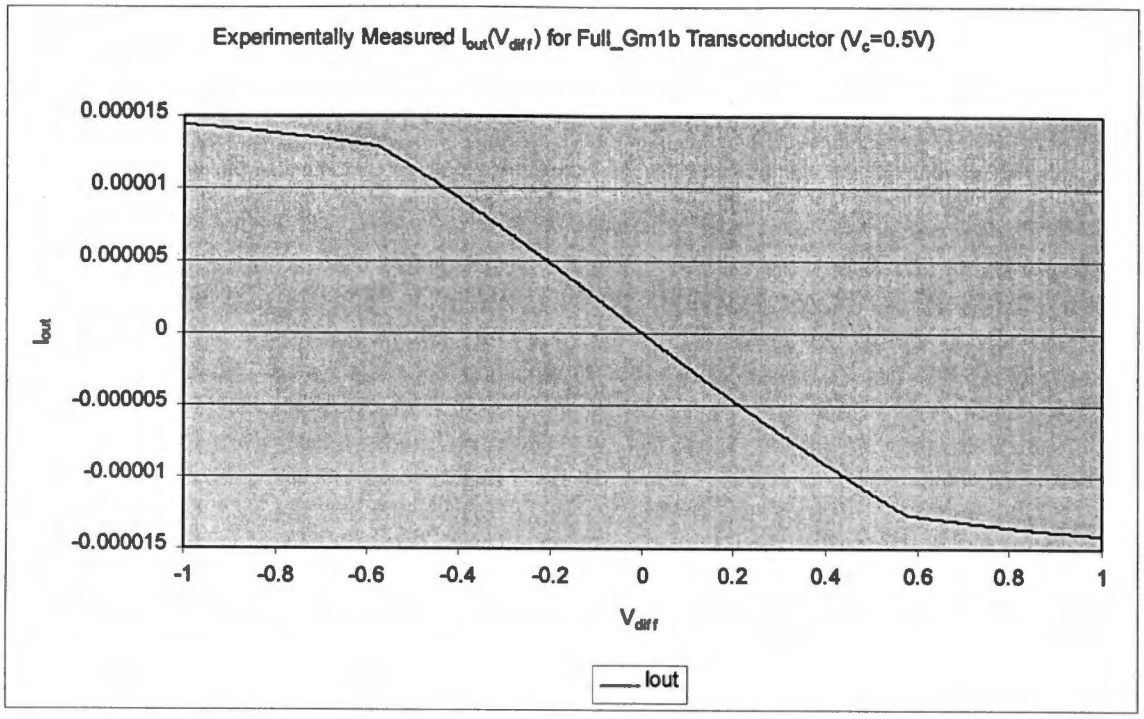


Figure 70. Experimentally measured $I_{out}(V_{diff})$. Full_Gm1b transconductor, V_c=0.5V. Nonlinearity is ~2.7% at V_{diff}=250mV.

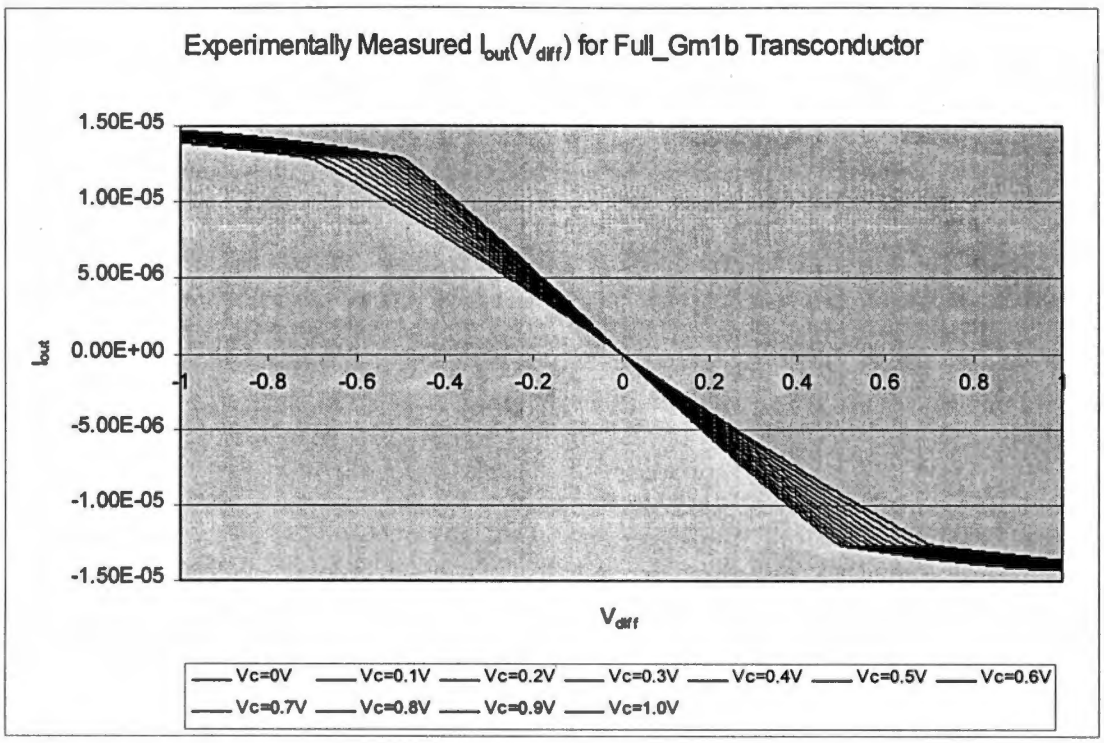


Figure 71. Experimentally measured $I_{out}(V_{diff})$. Full_Gm1b transconductor, V_c=0 to 1V.

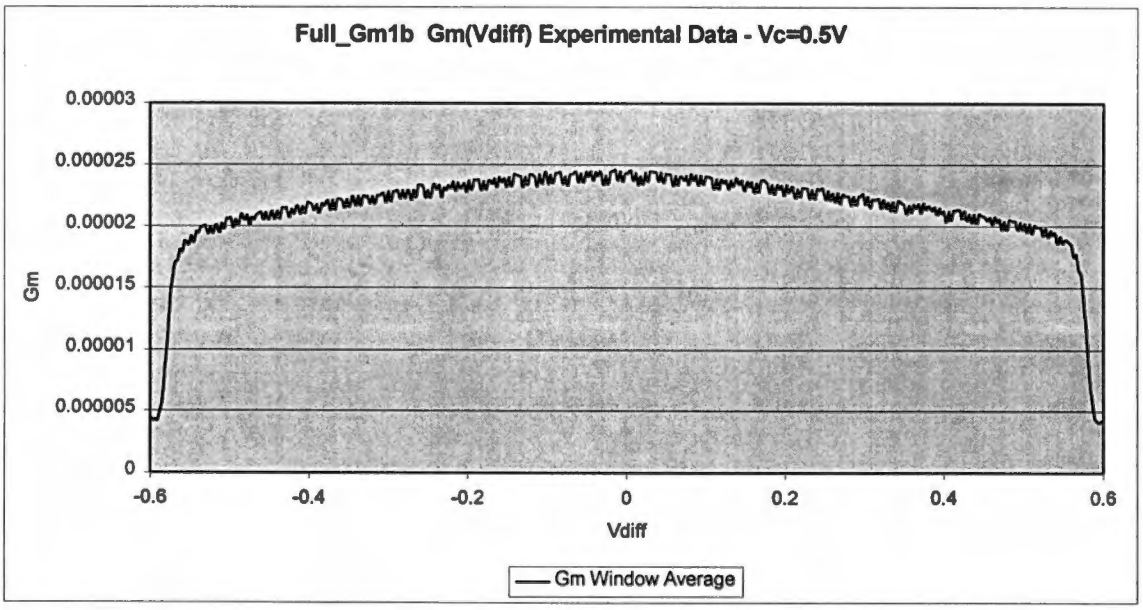


Figure 72. Experimentally measured $G_m(Vd_{iff})$. Full_Gm1b transconductor, V_c=0.5V. G_m variation is ~6.8% at V_{diff}=250mV from G_{m0}.

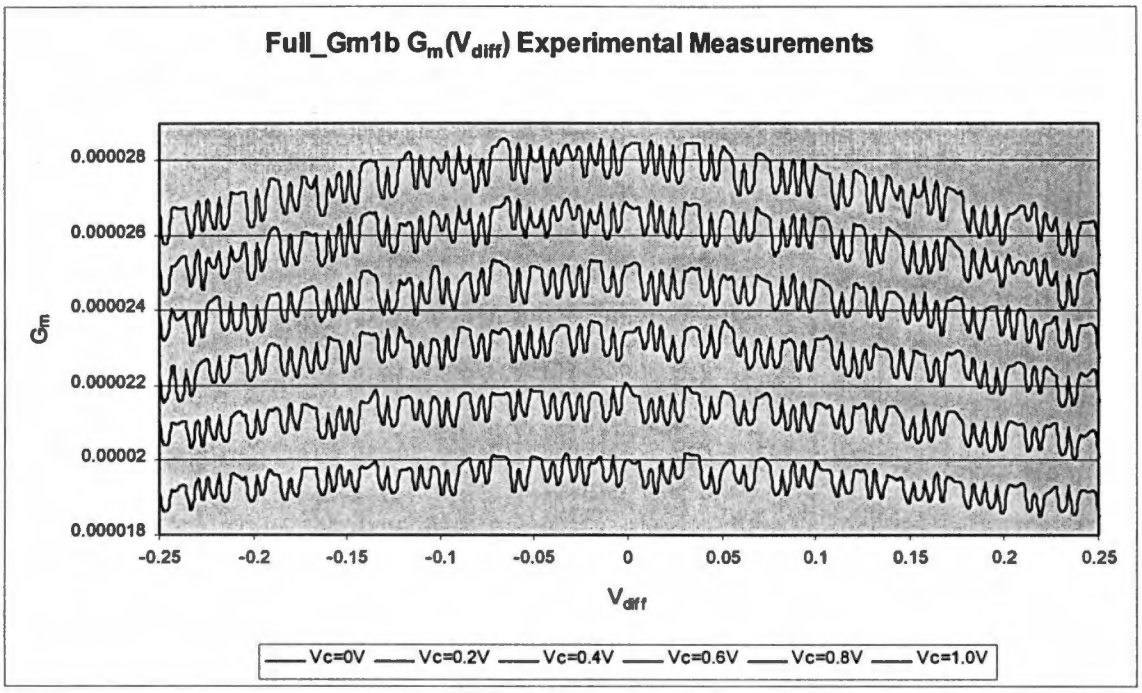


Figure 73. Experimentally measured $G_m(V_{diff})$ for V_c=0 to 1V. Full_Gm1b transconductor.

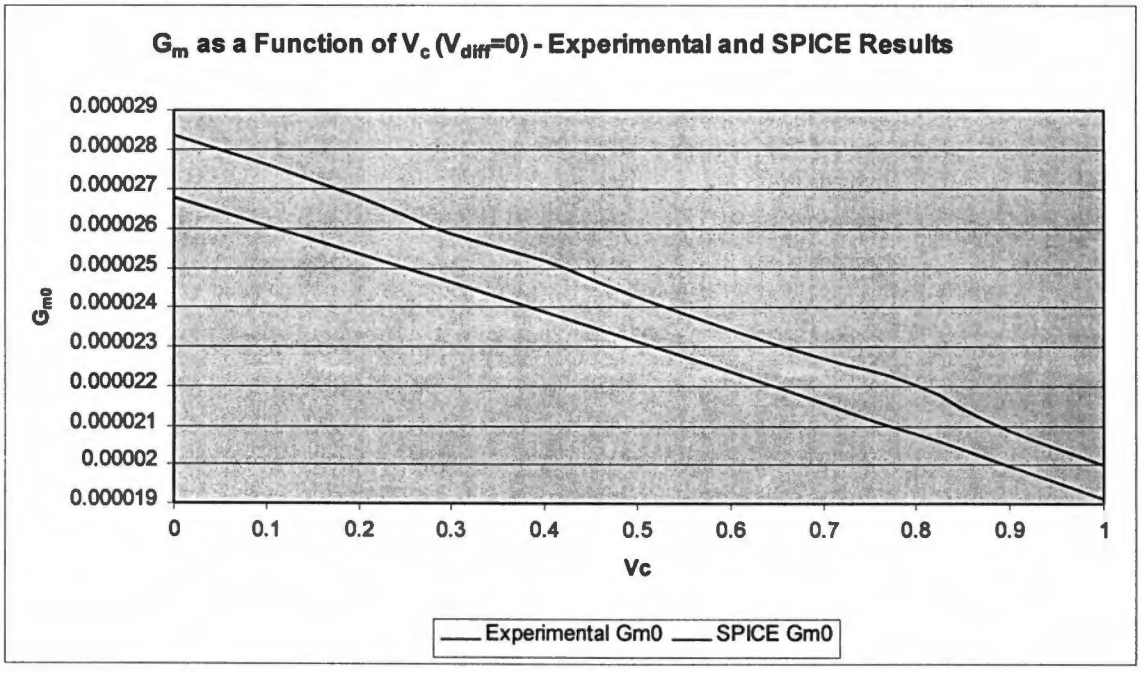


Figure 74. Experimentally measured and simulated G_{m0} as a function of V_c for Full_Gm1b. N91A process model. V_{diff}= 0V.

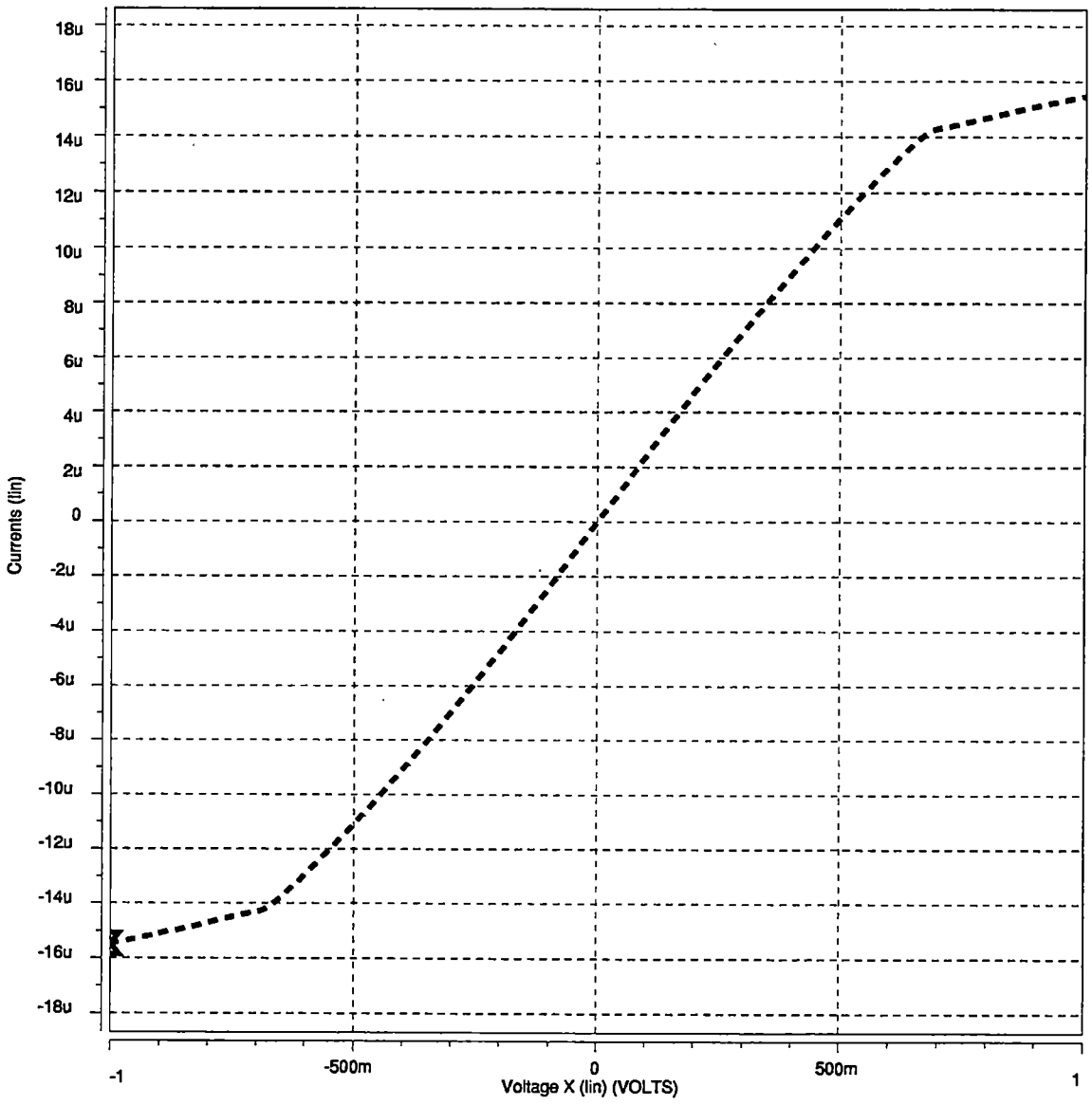


Figure 75. Pre-fabrication simulation results for Full_Gm1b $I_{out}(V_{diff})$ using N86O process data (V_c=0.5V; Outputs held at 2.5V).

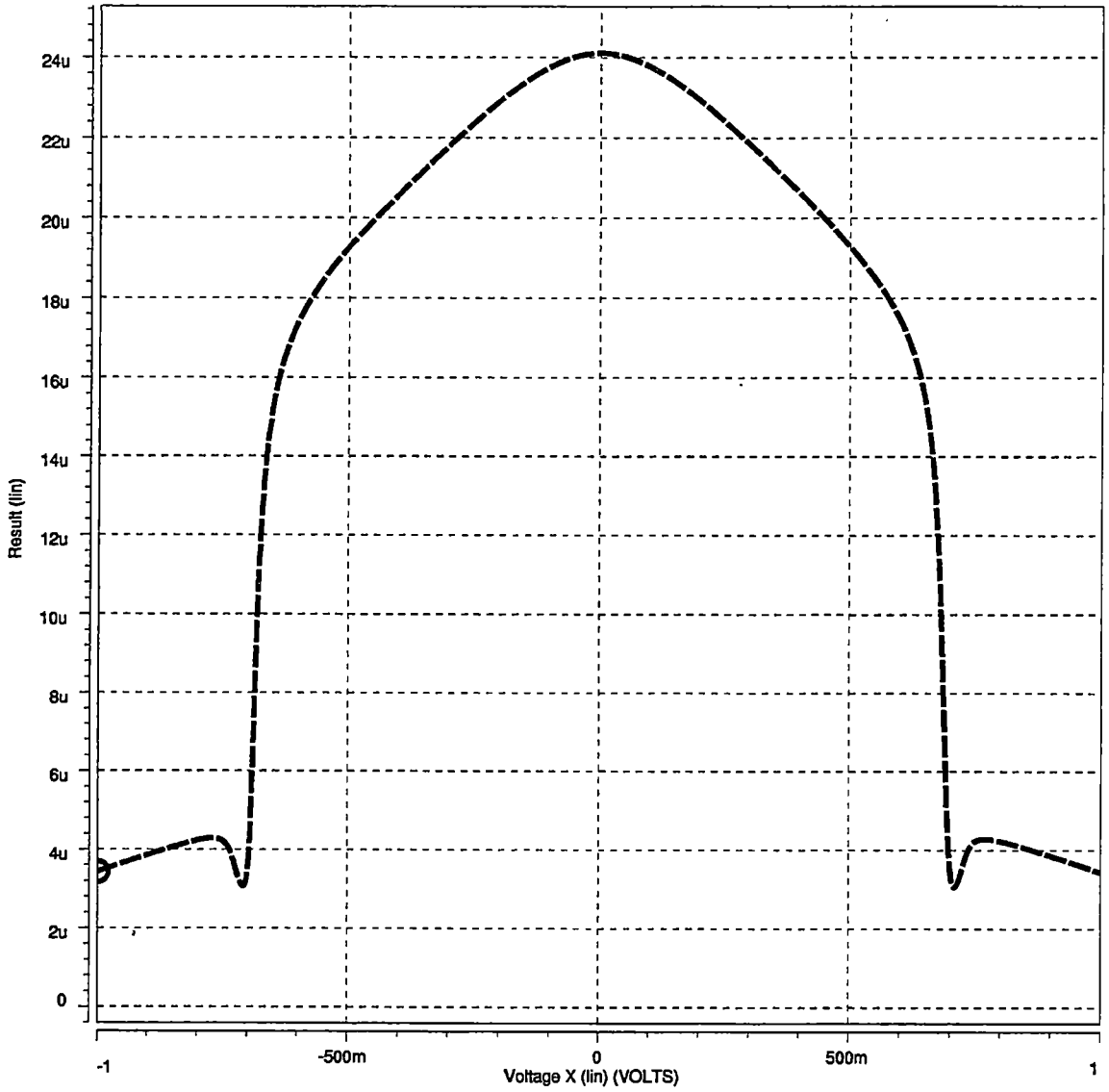


Figure 76. Pre-fabrication simulation results for Full_Gm1b $G_m(V_{diff})$ using N86O process data (V_c=0.5V; Outputs held at 2.5V).

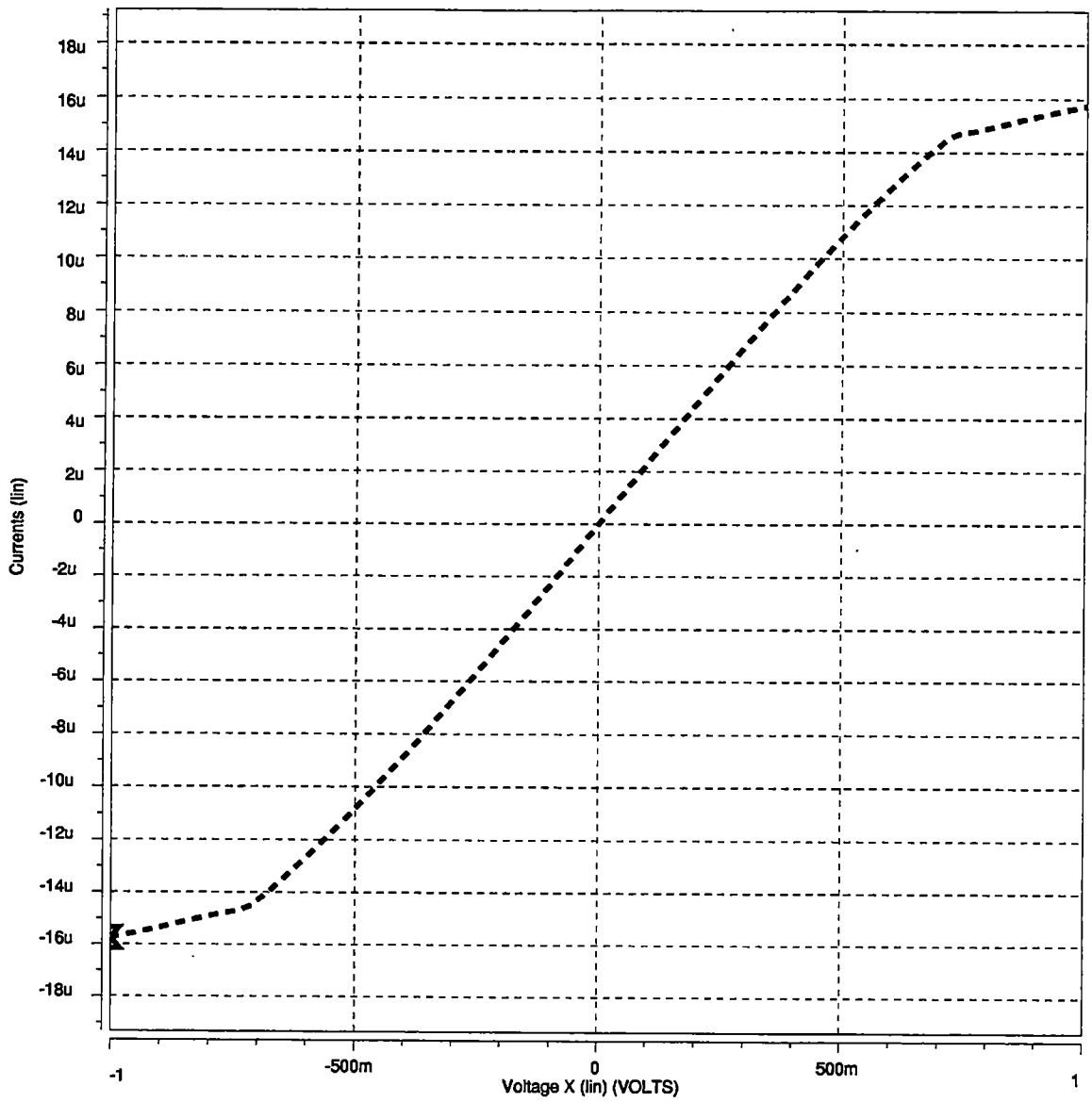


Figure 77. Fabrication run simulation results for Full_Gm1b $I_{out}(V_{diff})$ using N91A process data (V_c=0.5V; Outputs held at 2.5V).

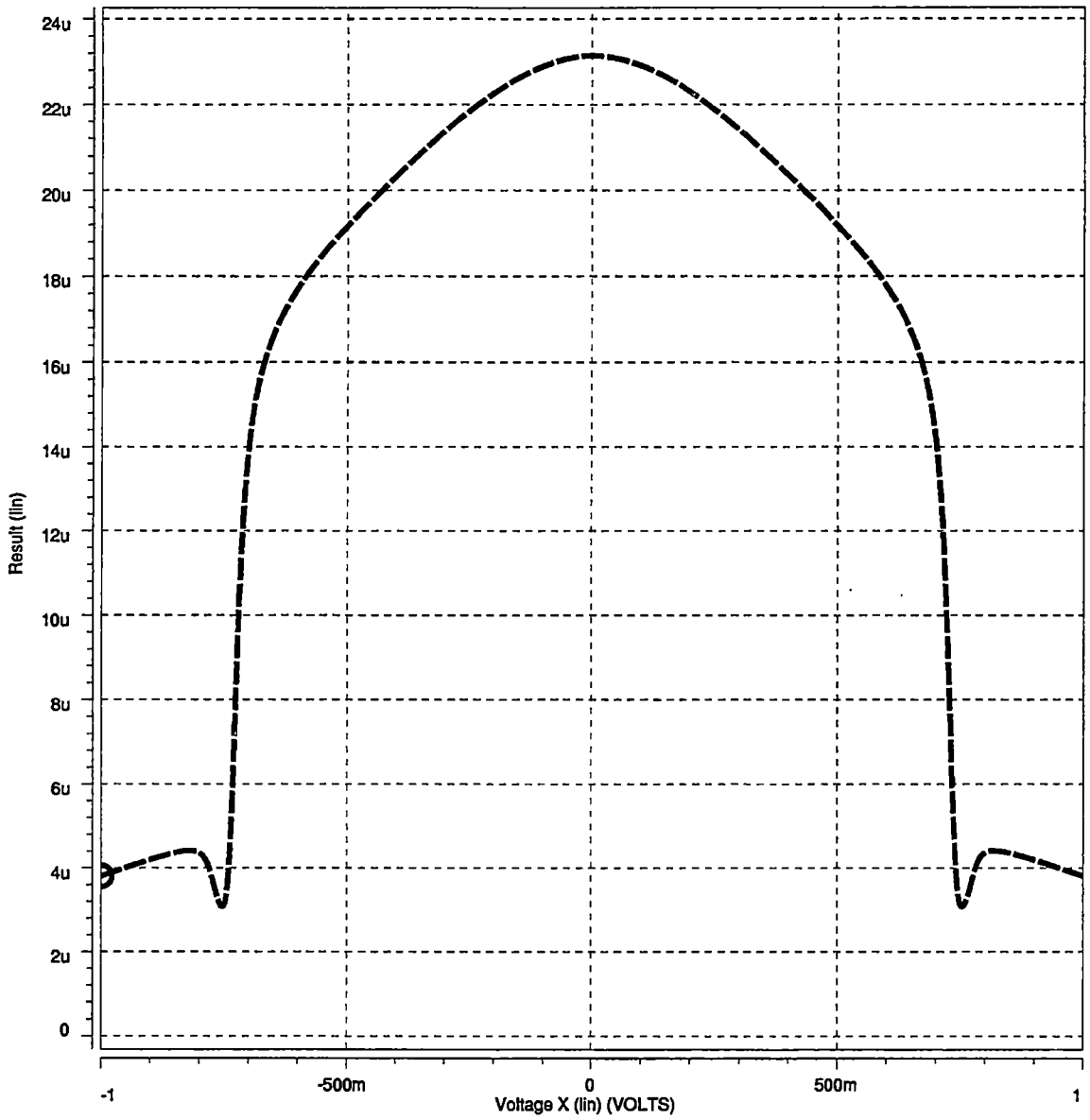


Figure 78. Fabrication run simulation results for Full_Gm1b $G_m(V_{diff})$ using N91A process data (V_c=0.5V; Outputs held at 2.5V).

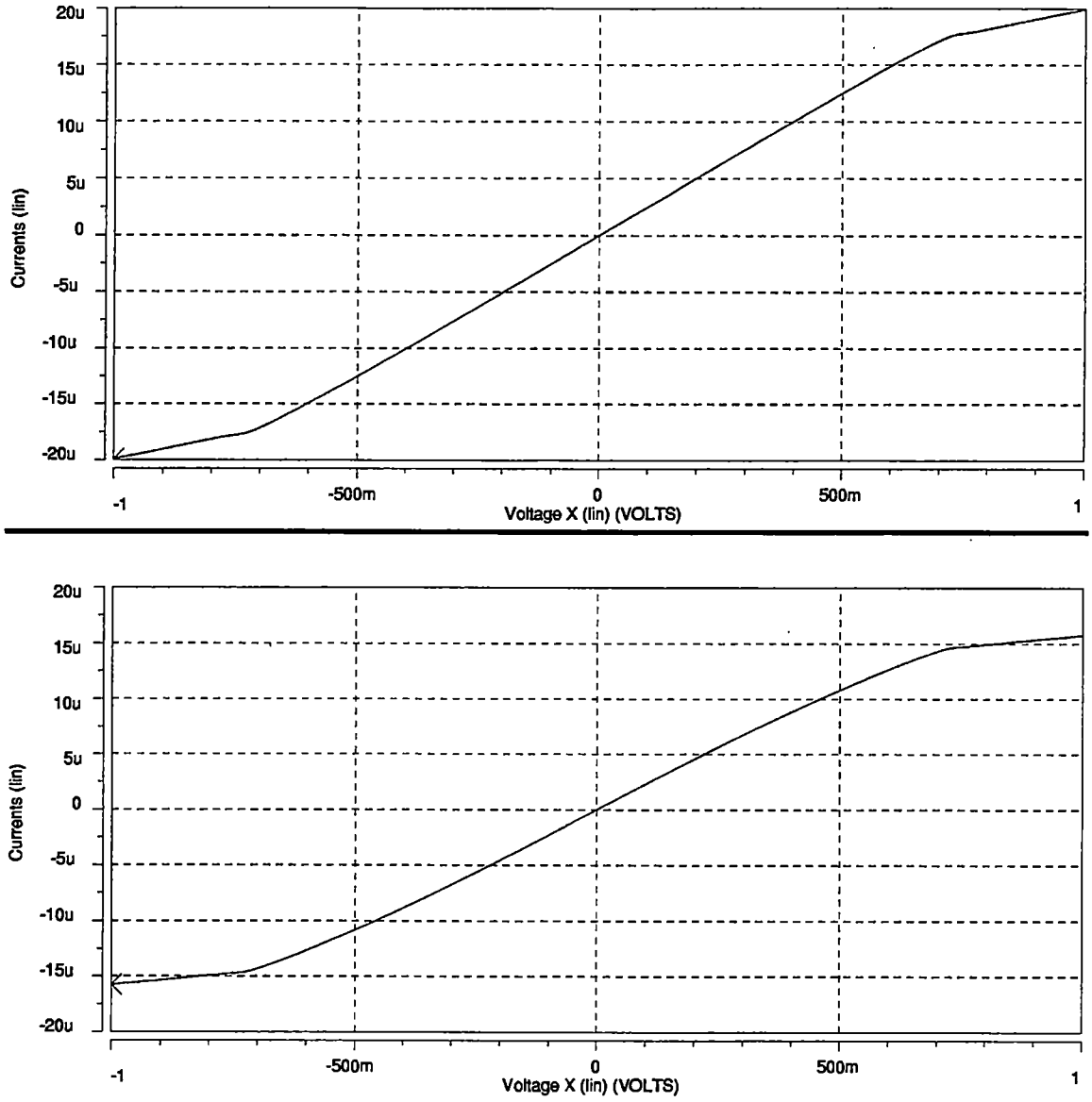


Figure 79. Simulation comparing Full_Gm1b $I_{out}(V_{diff})$ for the fixed output stage transconductor (top) and the fabricated transconductor circuit (bottom). N91A process data used with V_c=0.5V and outputs held at 2.5V.

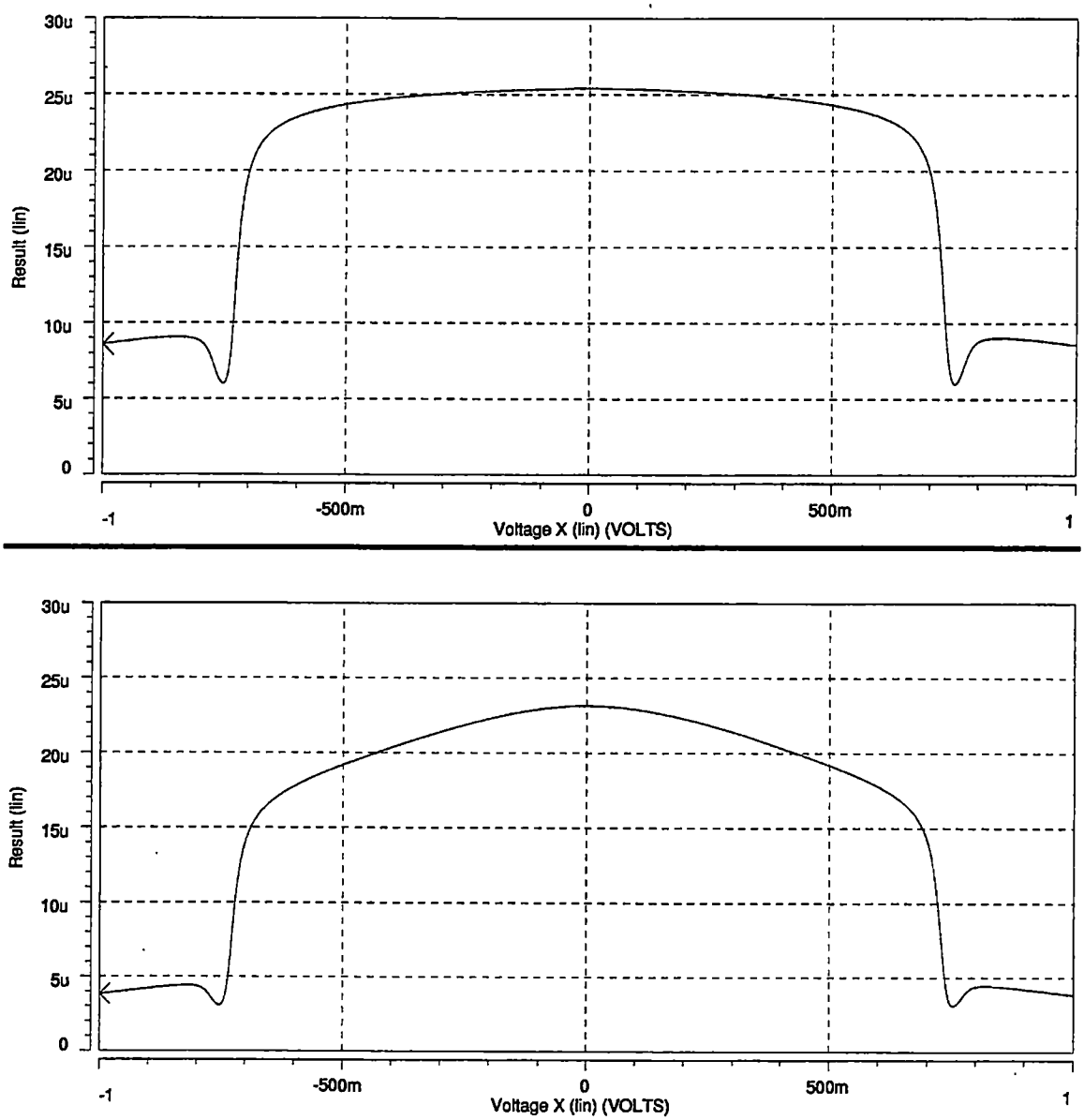


Figure 80. Simulation comparing Full_Gm1b $G_m(V_{diff})$ for the fixed output stage transconductor (top) and the fabricated transconductor circuit (bottom). N91A process data used with V_c=0.5V and outputs held at 2.5V.

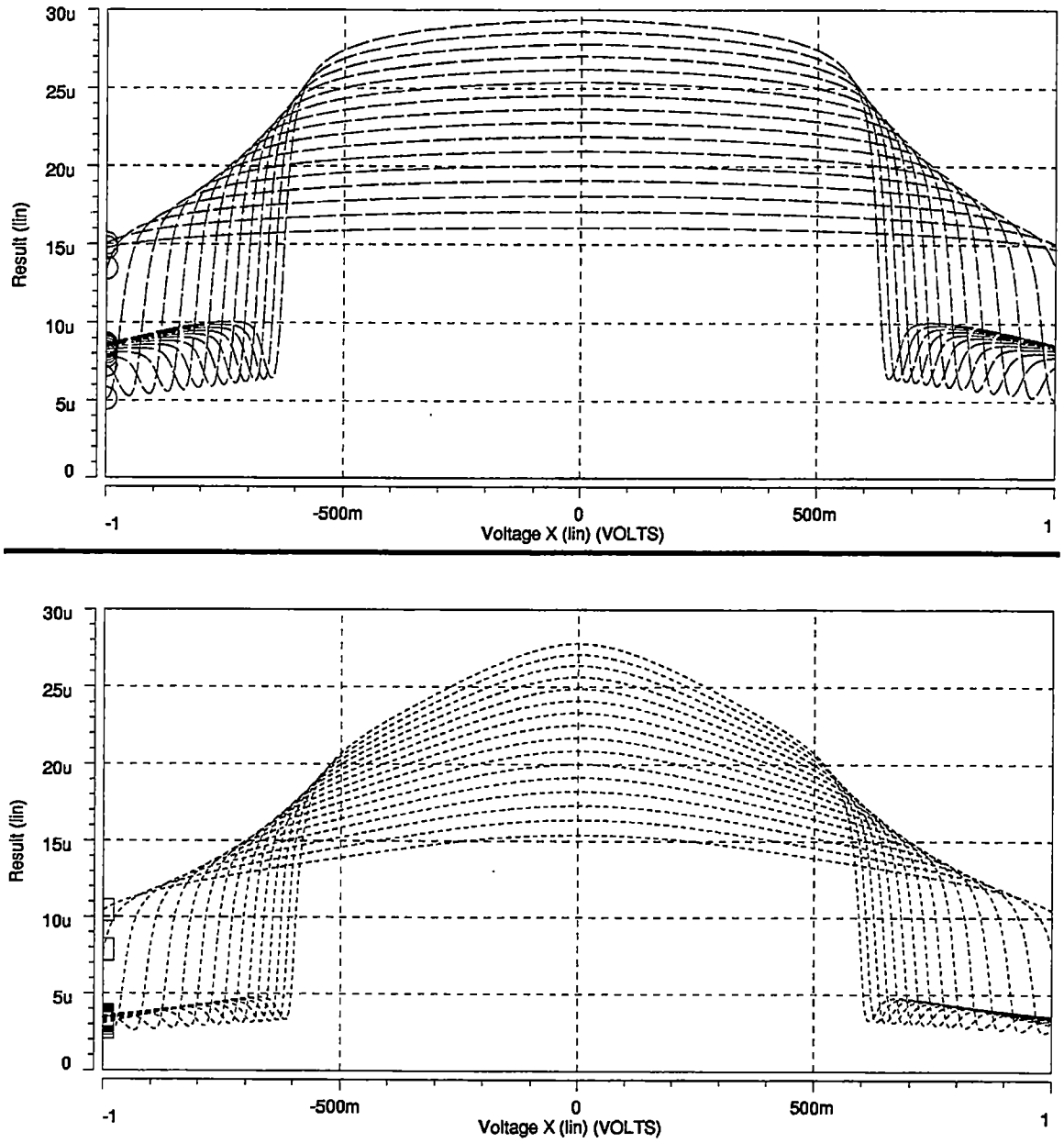


Figure 81. Simulation comparing Full_Gm1b $G_m(V_{diff})$ for the fixed output stage transconductor (top) and the fabricated transconductor circuit (bottom). N91A process data used with V_c sweeped from 0V to 1.5V. Max G_m is when V_c=0V. Outputs held at 2.5V

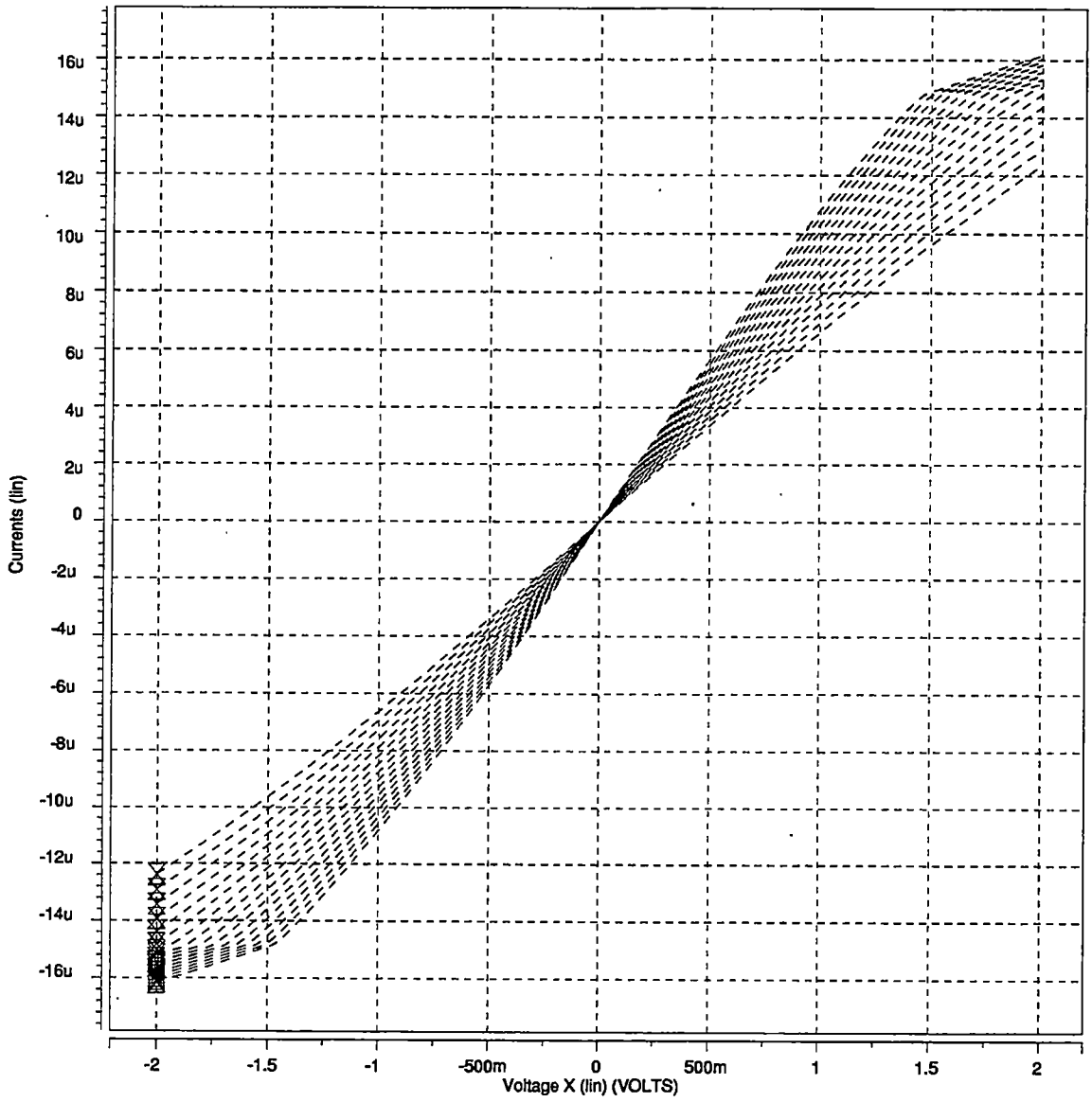


Figure 82. Simulation of $I_{out}(V_{diff})$ for Full_Gm1c transconductor circuit. N91A process data used with V_c sweeped from 0V to 1.5V. Steepest slope corresponds to V_c=0V. Outputs held at 2.5V

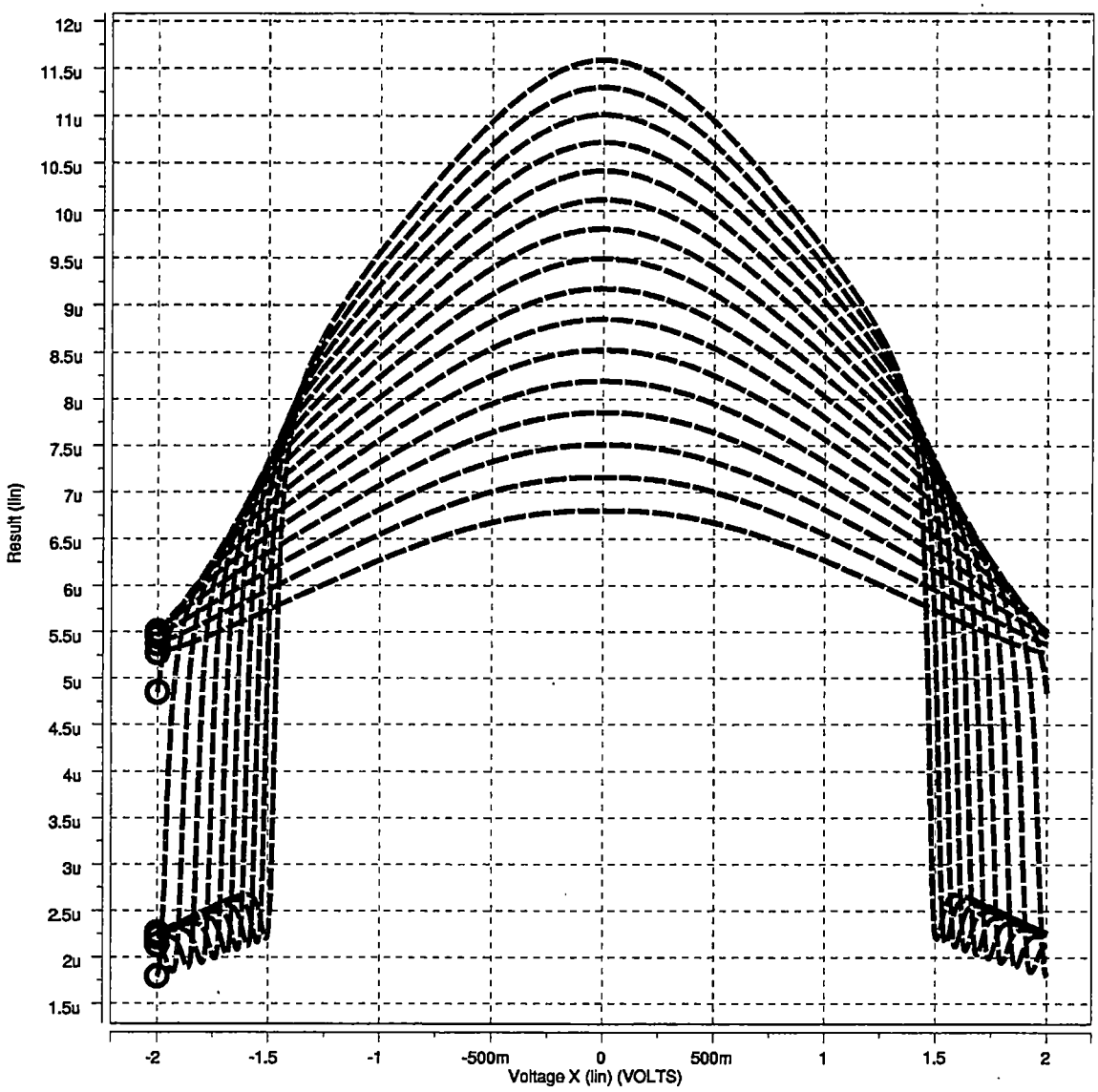


Figure 83. Simulation of $G_m(V_{diff})$ for Full_Gm1c transconductor circuit. N91a process data used with V_c sweeped from 0V to 1.5V. Max G_m is when V_c=0V. Outputs held at 2.5V

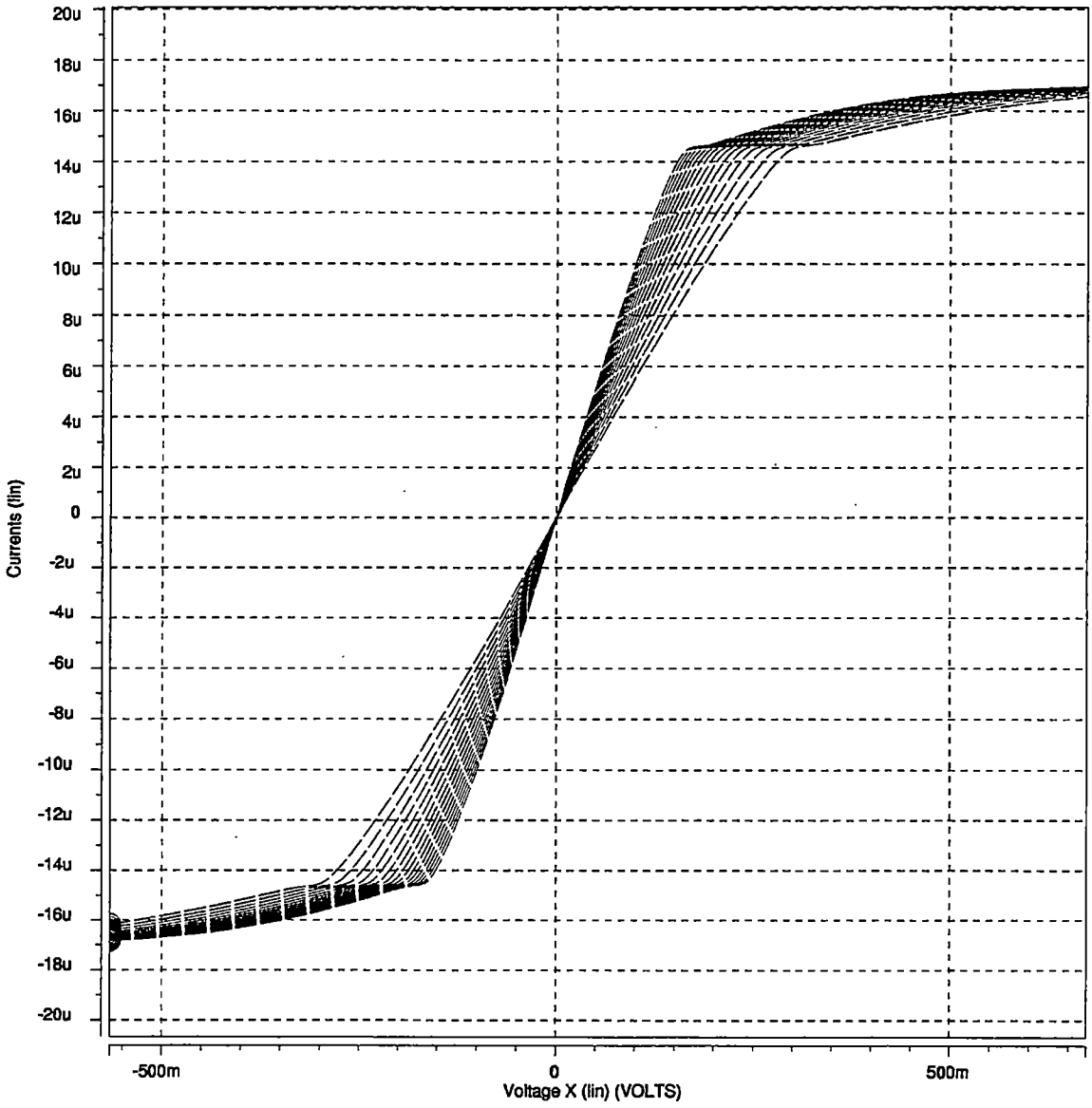


Figure 84. Simulation of $I_{out}(V_{diff})$ for Full_Gm3b transconductor circuit. N91a process data used with V_c sweeped from 0V to 1.5V. Steepest slope corresponds to V_c=0V. Outputs held at 2.5V

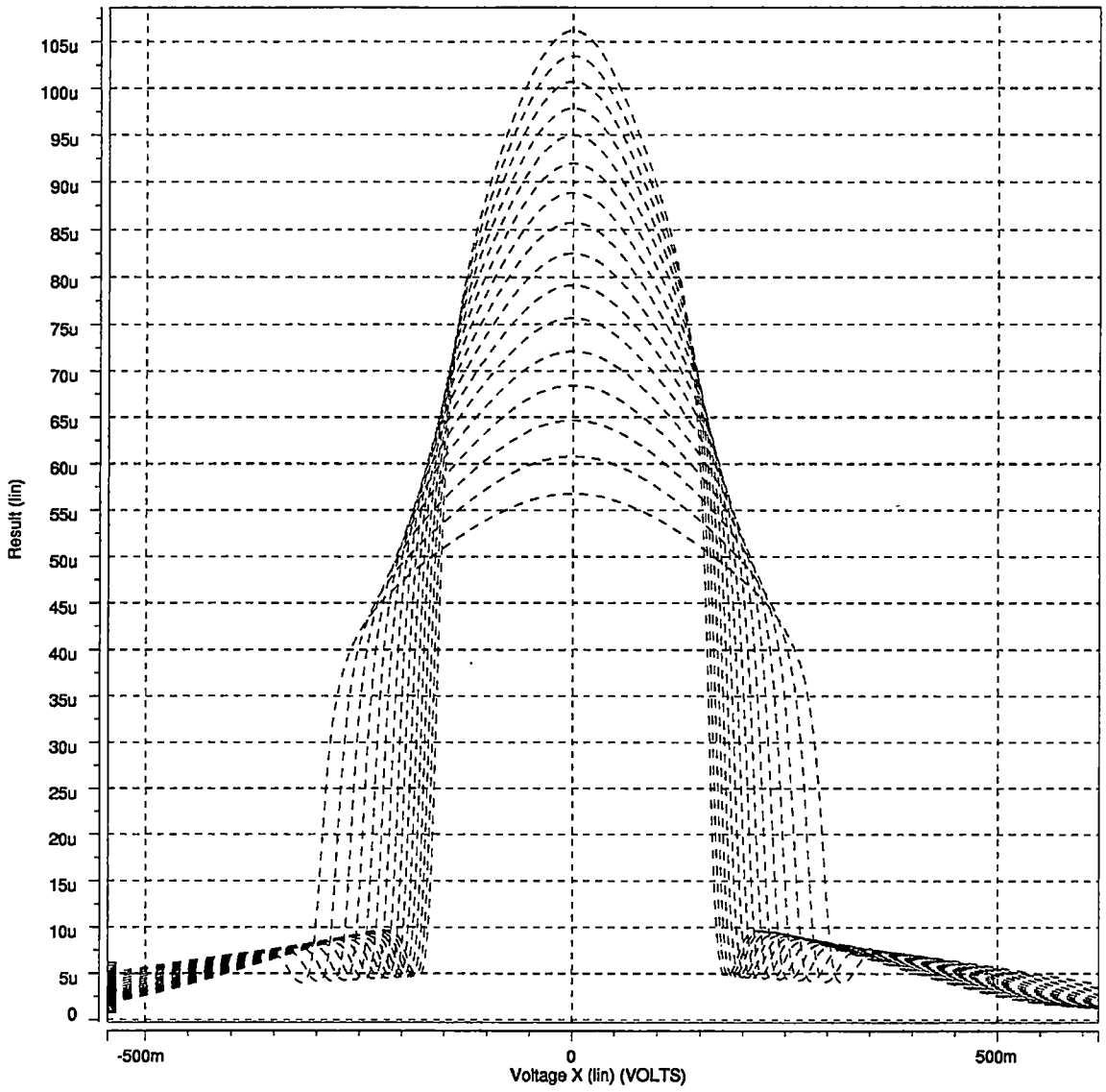


Figure 85. Simulation of $G_m(V_{diff})$ for Full_Gm3b transconductor circuit. N91a process data used with V_c sweeped from 0V to 1.5V. Max G_m is when V_c=0V. Outputs held at 2.5V

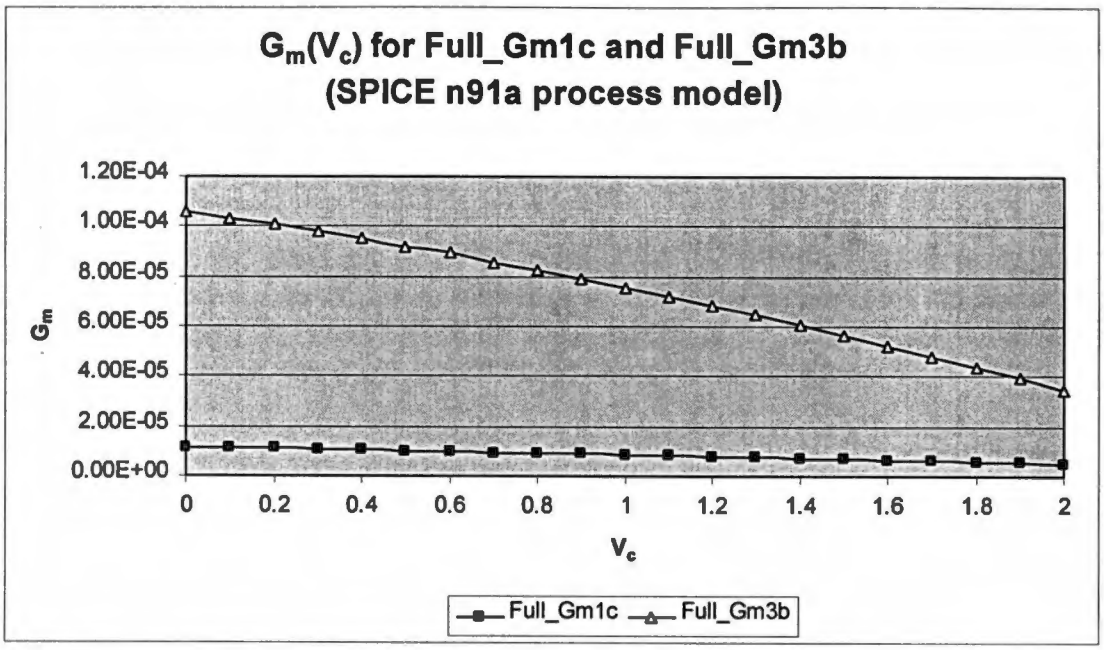


Figure 86. Simulated G_m as a function of V_c for Full_Gm1c and Full_Gm3b ($V_{diff} = 0$).

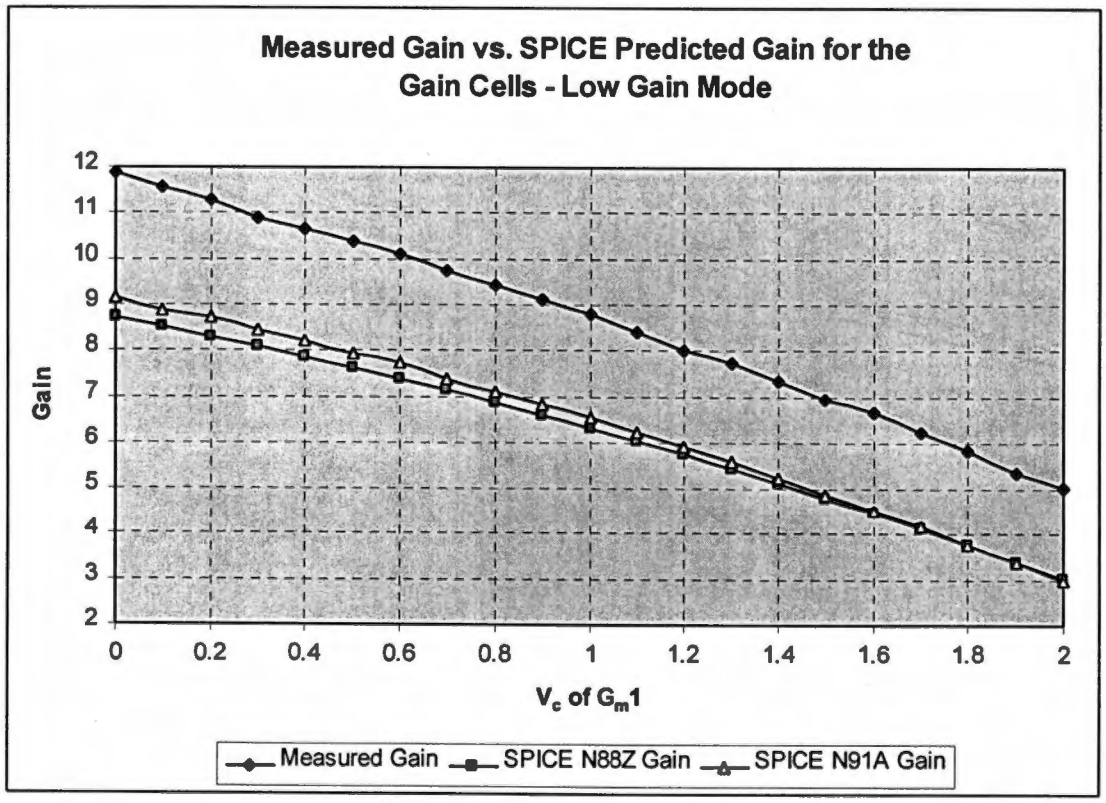


Figure 87. Experimentally measured and predicted gains for the gain cell. Low gain mode. Measured results from N88Z process.

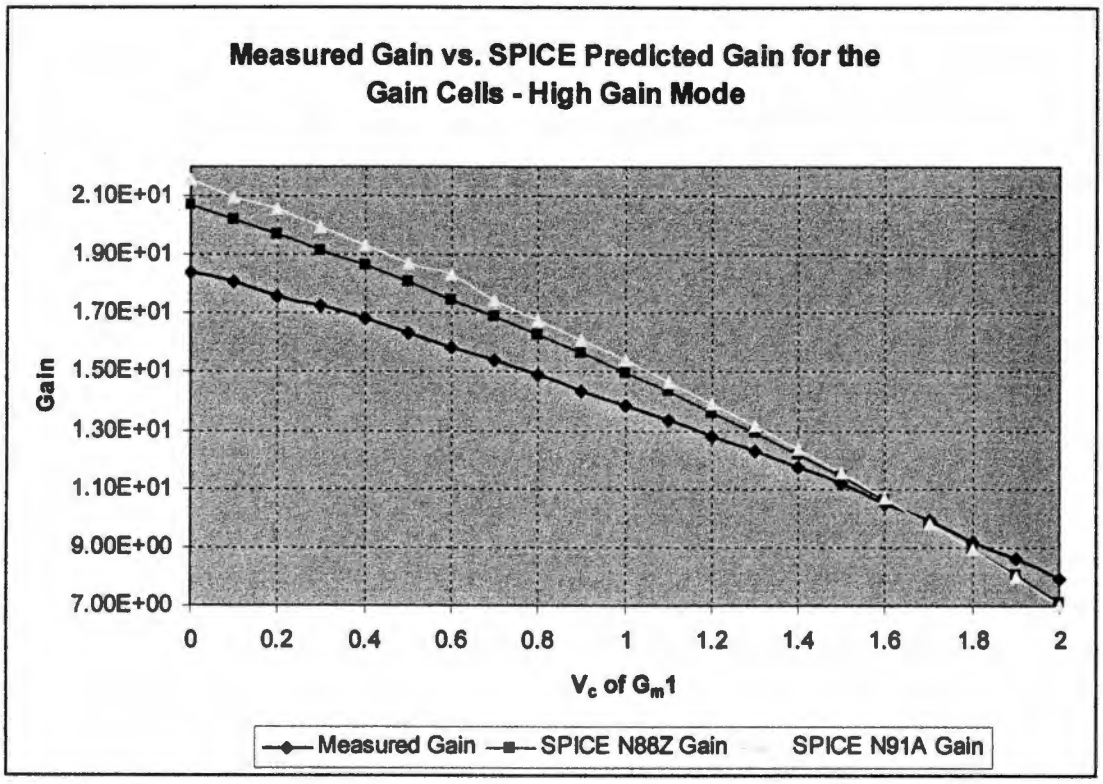


Figure 88. Experimentally measured and predicted gains for the gain cell. High gain mode. Measured results from N88Z process.

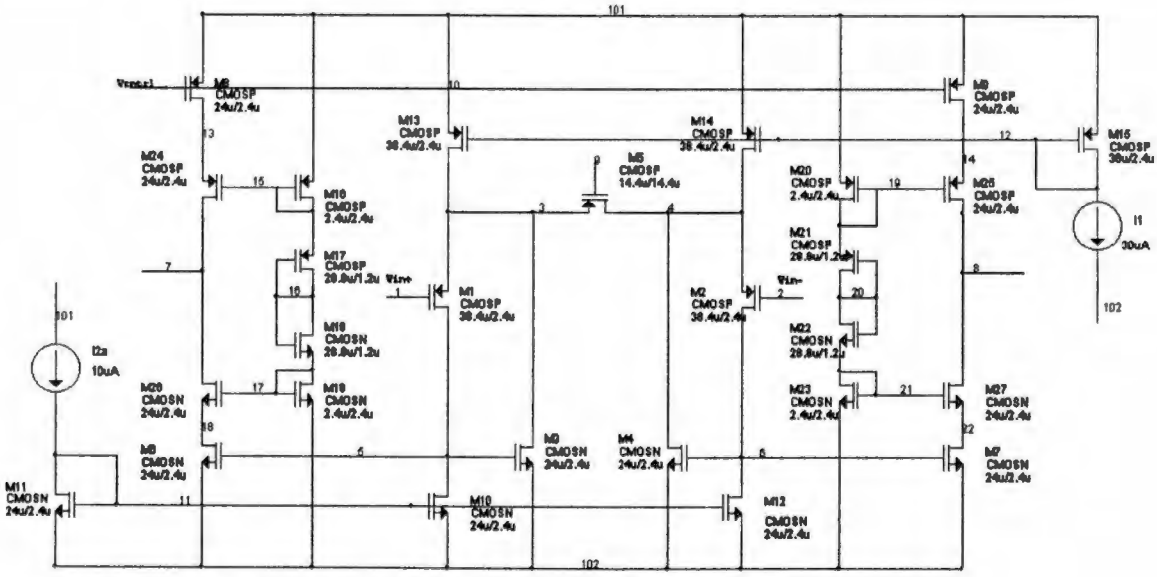


Figure 89. Transconductor circuit fabricated on the prototype chip.

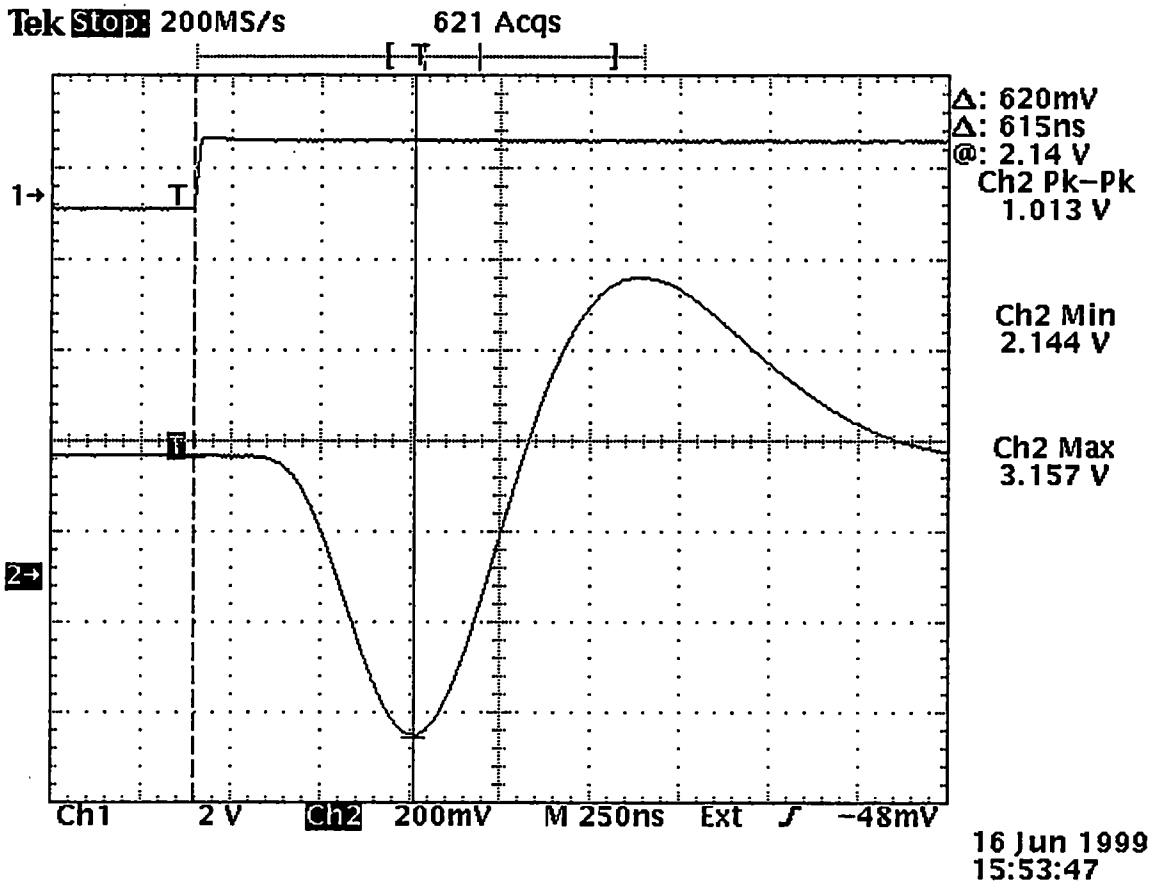


Figure 90. Response of the prototype pulse shaping amplifier to a 16mV input step pulse. Time from the input pulse to the minimum value of the first bipolar pulse lobe.

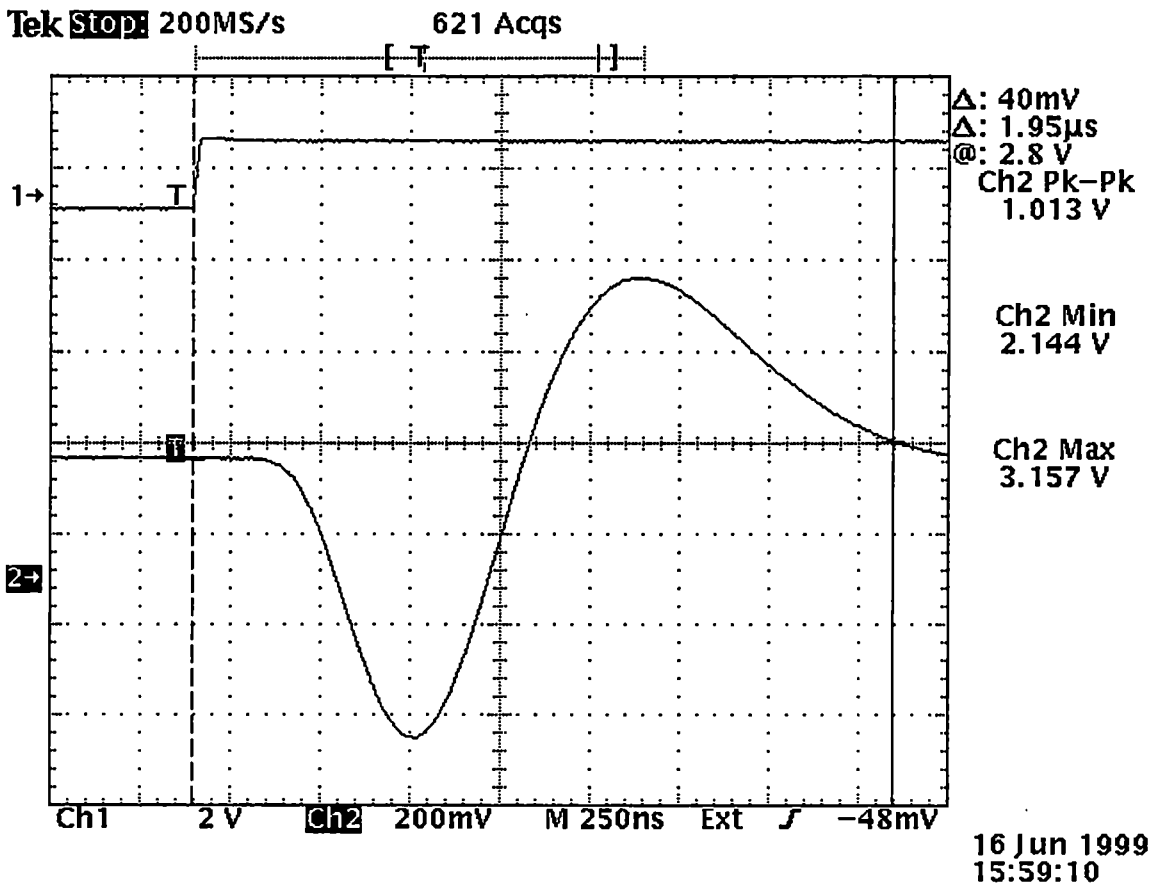


Figure 91. Response of the prototype pulse shaping amplifier to a 16mV input step pulse. Time from the input pulse to 10% of the baseline.

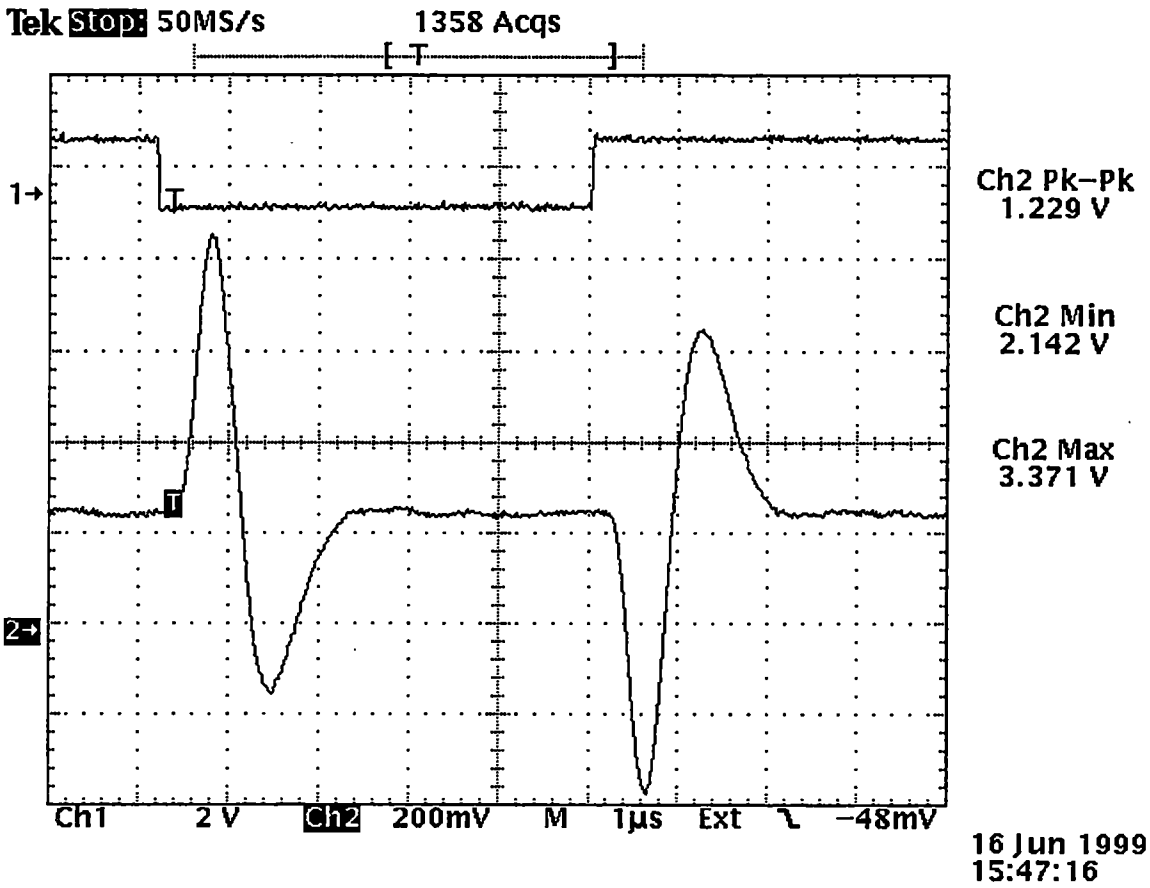


Figure 92. Pulse shaping amplifier response to 16mV input pulse. Both polarity of outputs shown.

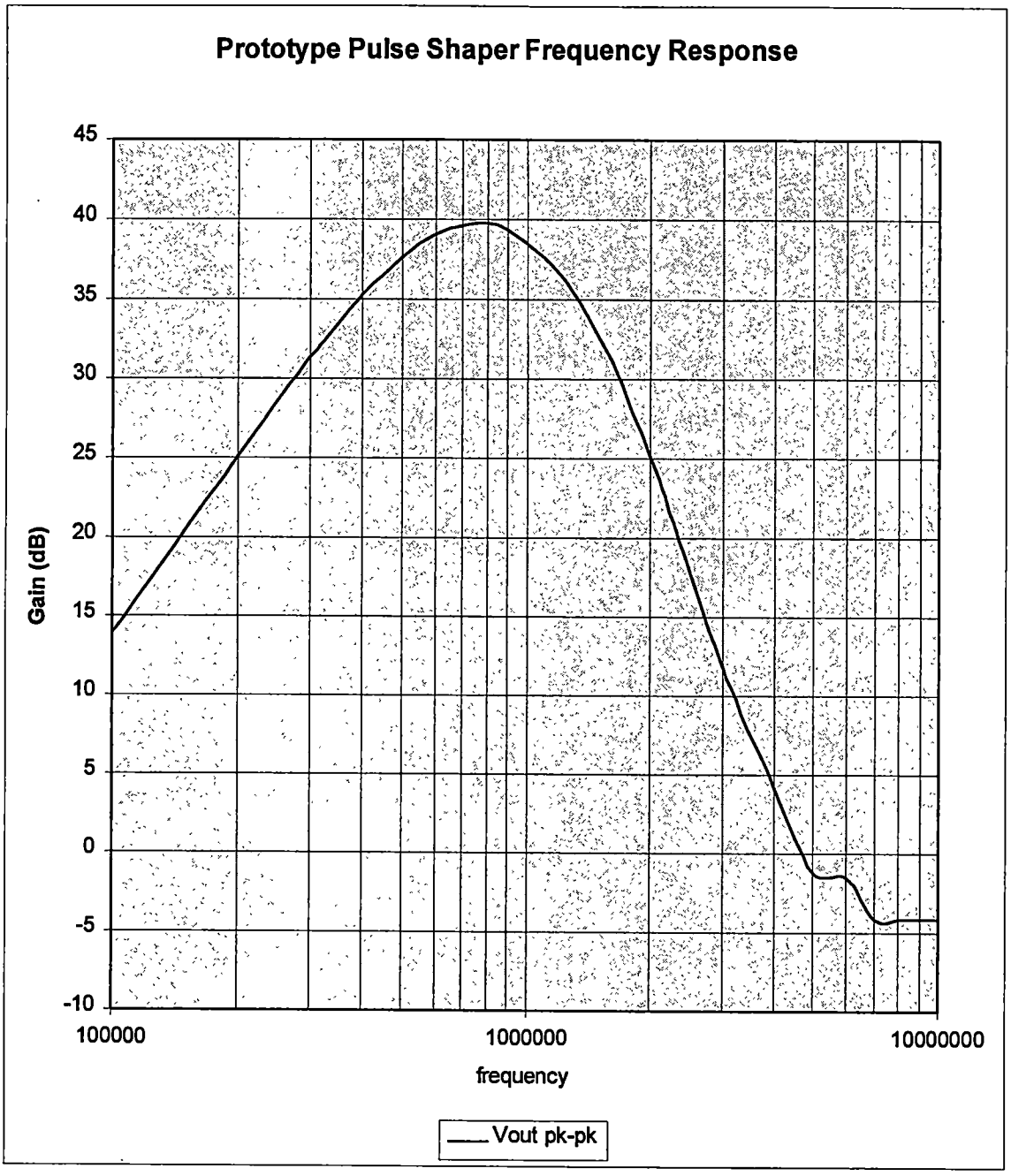


Figure 93. Experimentally measured frequency response of the prototype pulse shaping amplifier.

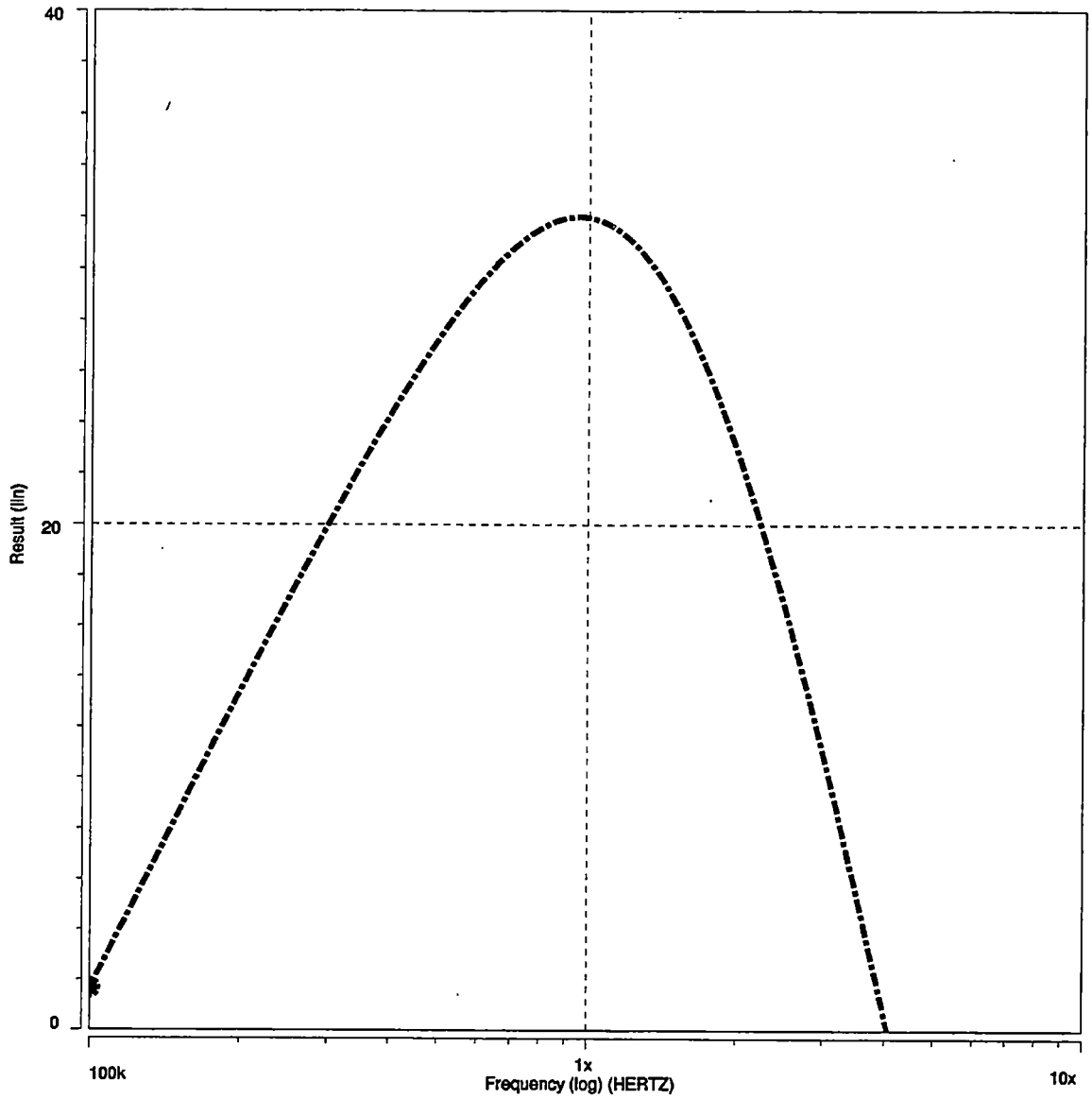


Figure 94. SPICE frequency response of the prototype shaper. Gain in dB versus frequency.

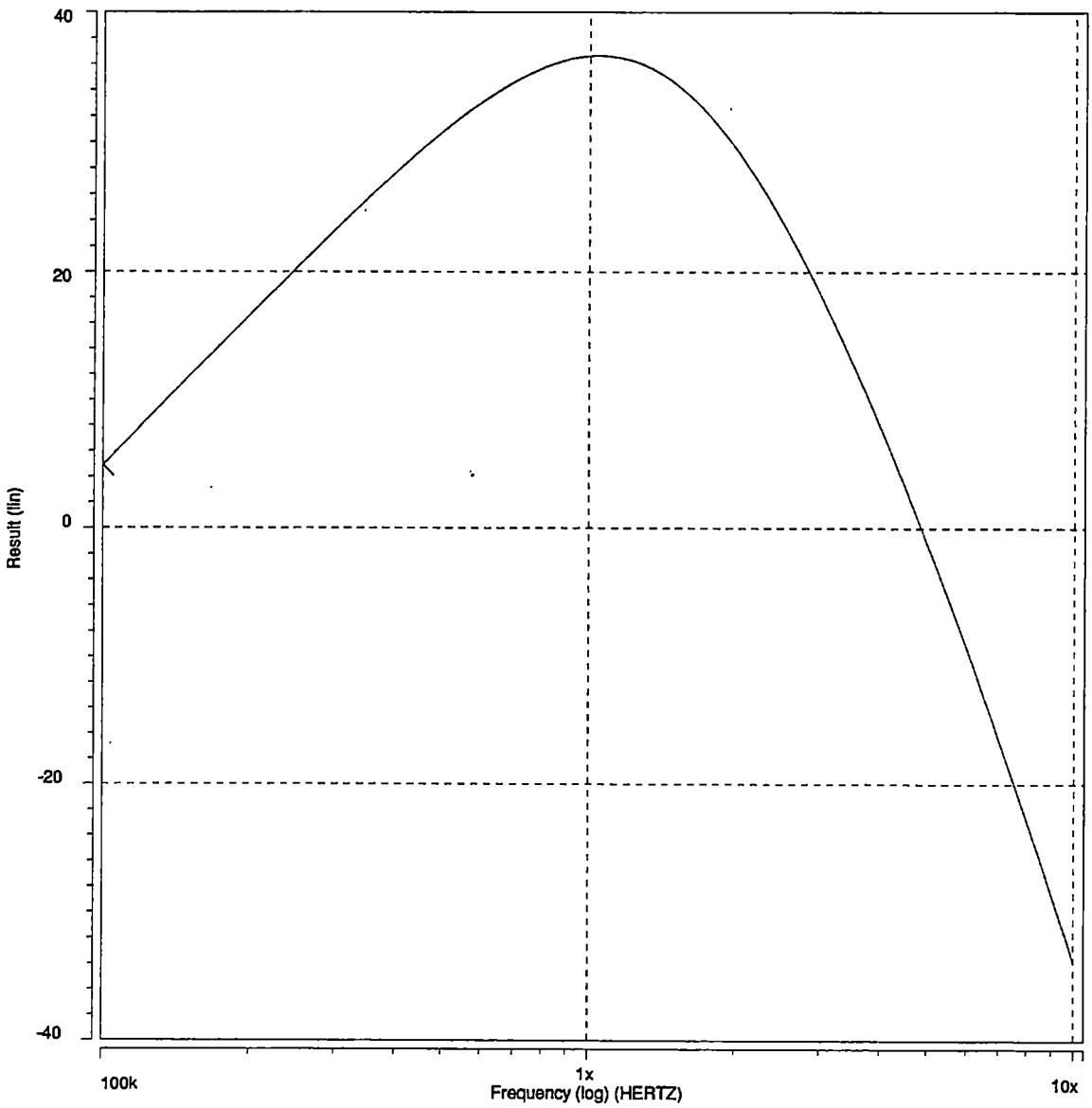


Figure 95. SPICE frequency response of the shaper using the fixed transconductor design from Chapter 3. Gain in dB versus frequency.

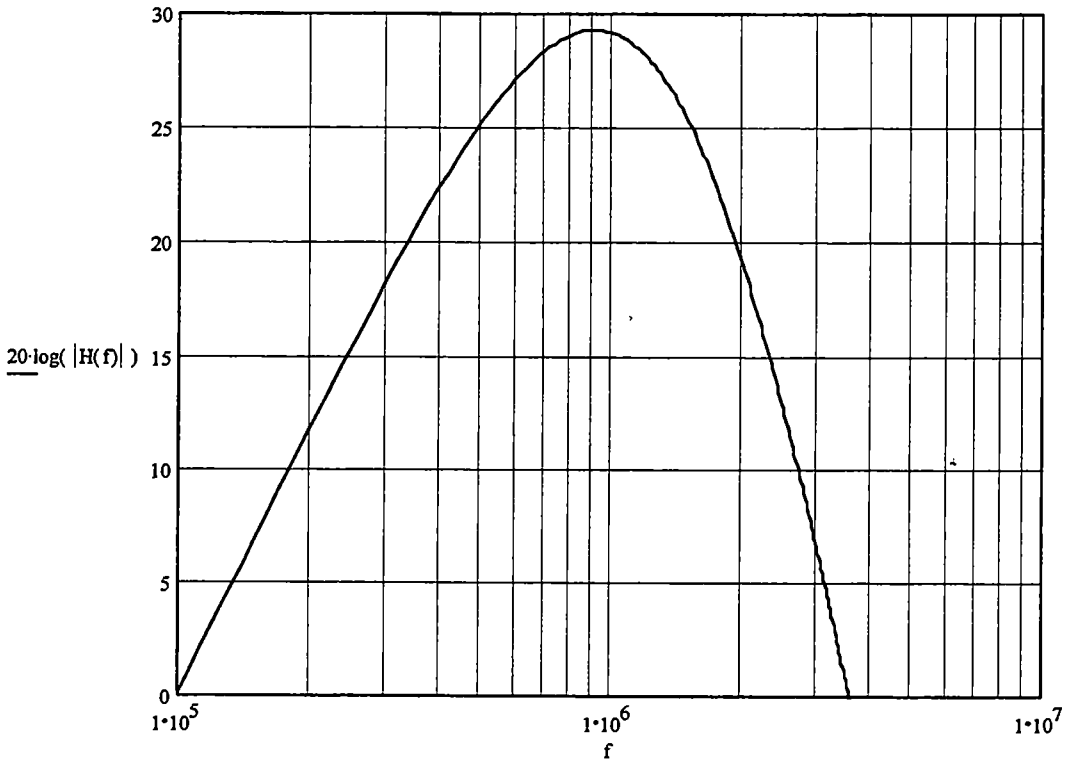


Figure 96. Predicted frequency response of the pulse shaping amplifier including the parasitic poles. Gain in dB versus frequency.

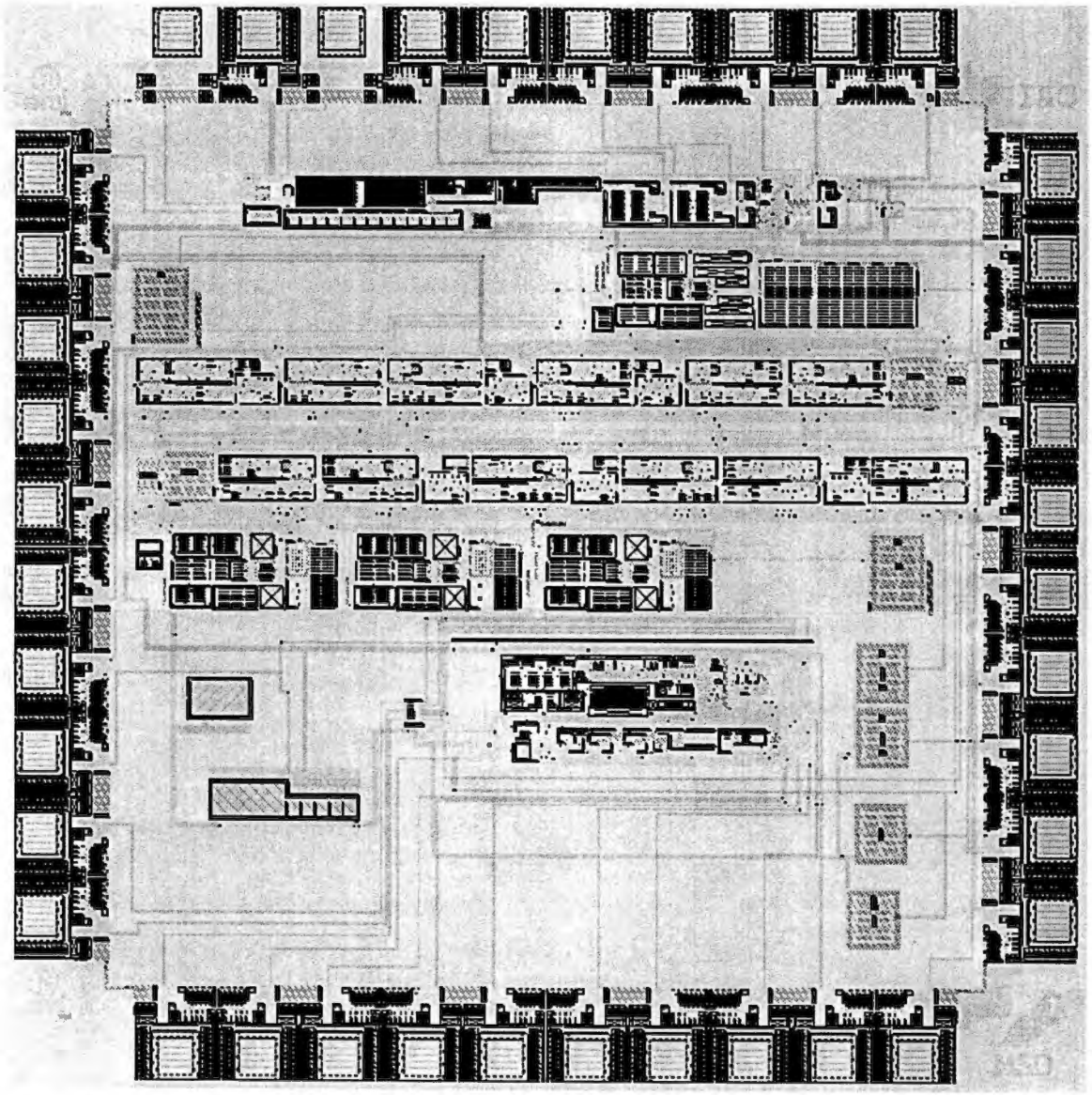


Figure 97. Prototype MicroCAT analog channel chip layout.

Appendix B

Table 1. Analog Channel Design Specifications.

CZT Pixel Detector Charge Collection Time	~1μsec
Preamplifier Rise Time	~13nsec
Experimentally Determined τ_{opt} for ORTEC 571 Shaping Amplifier with a capacitance equal to the CZT pixel detector capacitance.	4-5μsec
G_m-C Based Pulse Shaping Amplifier CR Time Constants	~100nsec
G_m-C Based Pulse Shaping Amplifier Biquad Time Constants	~125nsec
G_m-C Based Pulse Shaping Amplifier SPICE Time-to-Peak	~700 nsec
G_m-C Based Pulse Shaping Amplifier SPICE Complete Pulse Shaping Time (return to baseline)	1.5 μsec

Table 2. Triode region transistor g_{ds} for different process runs and dimensions with *W/L*=1.

W/L=2.4μ/2.4μ	g_{ds} from AMI N77H Process	g_{ds} from AMI N88Z Process	% variation
BSIM3v3 model			
Vgate			
0V	24.5μS	18.32μS	25%
0.5V	20.64μS	15.2μS	26.4%
1.0V	16.46μS	11.8μS	28%
W/L=4.8μ/4.8μ			
BSIM3v3 model			
Vgate			
0V	35.18μS	30.33μS	13.8%
0.5V	30.05μS	25.72μS	14.4%
1.0V	24.44μS	20.57μS	15.8%
W/L=9.6μ/9.6μ			
BSIM3v3 model			
Vgate			
0V	40.55μS	36.92μS	8.95%
0.5V	34.72μS	31.54μS	9.2%
1.0V	28.40μS	25.5μS	10.2%
W/L=14.4μ/14.4μ			
BSIM3v3 model			
Vgate			
0V	42.35μS	39.19μS	7.46%
0.5V	36.32μS	33.55μS	7.63%
1.0V	29.71μS	27.21μS	8.4%

Table 3. Biquad low-pass filter time constants for different values of G_m (C_1=6.1pF, C_2=1.9pF, Q=0.56).

Gm	ω_o	f_{-6db}	τ
30μS	8.8×10^6 rad/s	1.4MHz	113nsec
35μS	10.3×10^6 rad/s	1.64MHz	97.3nsec
40μS	11.7×10^6 rad/s	1.87MHz	85nsec

Table 4. Dominant noise contributions in transconductor.

Transistor	Spectral density at single-ended output and referred to input (V^2/Hz)			
	Output(Hand)	Output(SPICE)	Input(Hand)	Input(SPICE)
M1	$8.77 \cdot 10^{-12} + \frac{105 \cdot 10^{-9}}{f}$	$8.26 \cdot 10^{-12} + \frac{105 \cdot 10^{-9}}{f}$	$140 \cdot 10^{-18} + \frac{1.68 \cdot 10^{-12}}{f}$	$138 \cdot 10^{-18} + \frac{1.75 \cdot 10^{-12}}{f}$
M3	$35.1 \cdot 10^{-12} + \frac{30.9 \cdot 10^{-6}}{f}$	$22.3 \cdot 10^{-12} + \frac{20.5 \cdot 10^{-9}}{f}$	$562 \cdot 10^{-18} + \frac{495 \cdot 10^{-12}}{f}$	$374 \cdot 10^{-18} + \frac{343 \cdot 10^{-12}}{f}$
M13	$31.8 \cdot 10^{-12} + \frac{629 \cdot 10^{-9}}{f}$	$20.2 \cdot 10^{-12} + \frac{418 \cdot 10^{-9}}{f}$	$509 \cdot 10^{-18} + \frac{10.1 \cdot 10^{-12}}{f}$	$337 \cdot 10^{-18} + \frac{6.99 \cdot 10^{-12}}{f}$
M10	$43.8 \cdot 10^{-12} + \frac{25.4 \cdot 10^{-6}}{f}$	$49.2 \cdot 10^{-12} + \frac{30.0 \cdot 10^{-6}}{f}$	$700 \cdot 10^{-18} + \frac{406 \cdot 10^{-12}}{f}$	$822 \cdot 10^{-18} + \frac{502 \cdot 10^{-12}}{f}$
M6	$30.7 \cdot 10^{-12} + \frac{23.2 \cdot 10^{-6}}{f}$	$27.5 \cdot 10^{-12} + \frac{21.9 \cdot 10^{-6}}{f}$	$491 \cdot 10^{-18} + \frac{371 \cdot 10^{-12}}{f}$	$460 \cdot 10^{-18} + \frac{367 \cdot 10^{-12}}{f}$
M8	$19.2 \cdot 10^{-12} + \frac{366 \cdot 10^{-9}}{f}$	$16.0 \cdot 10^{-12} + \frac{319 \cdot 10^{-9}}{f}$	$307 \cdot 10^{-18} + \frac{5.85 \cdot 10^{-12}}{f}$	$267 \cdot 10^{-18} + \frac{5.33 \cdot 10^{-12}}{f}$
M2	$8.77 \cdot 10^{-12} + \frac{105 \cdot 10^{-9}}{f}$	$8.26 \cdot 10^{-12} + \frac{105 \cdot 10^{-9}}{f}$	$140 \cdot 10^{-18} + \frac{1.68 \cdot 10^{-12}}{f}$	$138 \cdot 10^{-18} + \frac{1.75 \cdot 10^{-12}}{f}$
M4	$35.1 \cdot 10^{-12} + \frac{30.9 \cdot 10^{-6}}{f}$	$22.3 \cdot 10^{-12} + \frac{20.5 \cdot 10^{-9}}{f}$	$562 \cdot 10^{-18} + \frac{495 \cdot 10^{-12}}{f}$	$374 \cdot 10^{-18} + \frac{343 \cdot 10^{-12}}{f}$
M14	$31.8 \cdot 10^{-12} + \frac{629 \cdot 10^{-9}}{f}$	$20.2 \cdot 10^{-12} + \frac{418 \cdot 10^{-9}}{f}$	$509 \cdot 10^{-18} + \frac{10.1 \cdot 10^{-12}}{f}$	$337 \cdot 10^{-18} + \frac{6.99 \cdot 10^{-12}}{f}$
M12	$43.8 \cdot 10^{-12} + \frac{25.4 \cdot 10^{-6}}{f}$	$49.2 \cdot 10^{-12} + \frac{30.0 \cdot 10^{-6}}{f}$	$700 \cdot 10^{-18} + \frac{406 \cdot 10^{-12}}{f}$	$822 \cdot 10^{-18} + \frac{502 \cdot 10^{-12}}{f}$
M7	$30.7 \cdot 10^{-12} + \frac{23.2 \cdot 10^{-6}}{f}$	$27.5 \cdot 10^{-12} + \frac{21.9 \cdot 10^{-6}}{f}$	$491 \cdot 10^{-18} + \frac{371 \cdot 10^{-12}}{f}$	$460 \cdot 10^{-18} + \frac{367 \cdot 10^{-12}}{f}$
M9	$19.2 \cdot 10^{-12} + \frac{366 \cdot 10^{-9}}{f}$	$16.0 \cdot 10^{-12} + \frac{319 \cdot 10^{-9}}{f}$	$307 \cdot 10^{-18} + \frac{5.85 \cdot 10^{-12}}{f}$	$267 \cdot 10^{-18} + \frac{5.33 \cdot 10^{-12}}{f}$
M5			$476 \cdot 10^{-18}$ (thermal)	$542 \cdot 10^{-18}$ (thermal)
Total $S_i(f)$ (V^2/Hz)			$5.89 \cdot 10^{-15} + \frac{2.57 \cdot 10^{-9}}{f}$	$5.34 \cdot 10^{-15} + \frac{2.45 \cdot 10^{-9}}{f}$

Table 5. Equivalent noise voltage spectral densities.

Node	Sources of Noise	Equivalent Noise Voltage Spectral Density
A	G_{m1} and the thermal noise of R_1. Note: $f_c \cong 1.59$MHz – the corner frequency of the CR highpass filter.	$S_A(f) = 5.89 \cdot 10^{-15} + \frac{2.57 \cdot 10^{-9}}{f} + \frac{166 \cdot 10^{-18}}{1 + \left(\frac{f}{f_c}\right)^2}$ V^2Hz
B	G_{m2} and G_{m3}	$S_B(f) = 11.78 \cdot 10^{-15} + \frac{5.14 \cdot 10^{-9}}{f}$ V^2Hz
C	G_{m4}	$S_C(f) = 5.89 \cdot 10^{-15} + \frac{2.57 \cdot 10^{-9}}{f}$ V^2Hz
D	G_{m5}, G_{m6}, and G_{m7}	$S_D(f) = 17.67 \cdot 10^{-15} + \frac{7.71 \cdot 10^{-9}}{f}$ V^2Hz

Table 6. Ideal transfer function from noise nodes to the output.

Node	Transfer Function to Output Ignoring Parasitic Poles from Gain Stages and Op Amps
A	$H_A(s) = \frac{(683.9) \cdot \left(\frac{1}{\tau_c}\right)^4 \cdot s}{\left(s + \frac{1}{\tau_c}\right) \cdot \left(s^2 + \frac{s}{Q \cdot \tau_c} + \left(\frac{1}{\tau_c}\right)^2\right)^2}$
B	$H_B(s) = \frac{(82.7) \cdot \left(\frac{1}{\tau_c}\right)^4 \cdot s}{\left(s + \frac{1}{\tau_c}\right) \cdot \left(s^2 + \frac{s}{Q \cdot \tau_c} + \left(\frac{1}{\tau_c}\right)^2\right)^2}$
C	$H_C(s) = \frac{(82.7) \cdot \left(\frac{1}{\tau_c}\right)^3 \cdot s}{\left(s + \frac{1}{\tau_c}\right)^2 \cdot \left(s^2 + \frac{s}{Q \cdot \tau_c} + \left(\frac{1}{\tau_c}\right)^2\right)}$
D	$H_D(s) = \frac{(82.7) \cdot \left(\frac{1}{\tau_c}\right)^2 \cdot s}{\left(s + \frac{1}{\tau_c}\right) \cdot \left(s^2 + \frac{s}{Q \cdot \tau_c} + \left(\frac{1}{\tau_c}\right)^2\right)}$

Table 7. Location of the pulse shaper poles and corresponding time constants.

Source	Pole location (Hz)	Time Constant
CR Stages	1.59MHz	τ_c=100nsec
Biquads	1.27MHz	τ_b=125nsec
Gain 10 Op Amp	1.5MHz	τ_1=106nsec
Gains Stages	13MHz	τ_2=12.2nsec
Unity Gain Op Amps	15MHz	τ_3=10.6nsec

Table 8. Transfer functions from noise nodes to output for Q=0.5. Includes the effect of the parasitic poles from the gain stages and the op amps.

Node	Transfer Function to Output Including Parasitic Poles from Gain Stages and Op Amps
A	$H_A(s) = \dfrac{(683.9)\cdot\left(\frac{1}{\tau_c}\right)^4\cdot\left(\frac{1}{\tau_1}\right)\cdot\left(\frac{1}{\tau_2}\right)^2\cdot\left(\frac{1}{\tau_3}\right)^3\cdot s}{\left(s+\frac{1}{\tau_c}\right)^5\cdot\left(s+\frac{1}{\tau_1}\right)\cdot\left(s+\frac{1}{\tau_2}\right)^2\cdot\left(s+\frac{1}{\tau_3}\right)^3}$
B	$H_B(s) = \dfrac{(82.7)\cdot\left(\frac{1}{\tau_c}\right)^4\cdot\left(\frac{1}{\tau_1}\right)\cdot\left(\frac{1}{\tau_2}\right)\cdot\left(\frac{1}{\tau_3}\right)^3\cdot s}{\left(s+\frac{1}{\tau_c}\right)^5\cdot\left(s+\frac{1}{\tau_1}\right)\cdot\left(s+\frac{1}{\tau_2}\right)\cdot\left(s+\frac{1}{\tau_3}\right)^3}$
C	$H_C(s) = \dfrac{(82.7)\cdot\left(\frac{1}{\tau_c}\right)^3\cdot\left(\frac{1}{\tau_1}\right)\cdot\left(\frac{1}{\tau_2}\right)\cdot\left(\frac{1}{\tau_3}\right)^3\cdot s}{\left(s+\frac{1}{\tau_c}\right)^4\cdot\left(s+\frac{1}{\tau_1}\right)\cdot\left(s+\frac{1}{\tau_2}\right)\cdot\left(s+\frac{1}{\tau_3}\right)^3}$
D	$H_D(s) = \dfrac{(82.7)\cdot\left(\frac{1}{\tau_c}\right)^2\cdot\left(\frac{1}{\tau_1}\right)\cdot\left(\frac{1}{\tau_2}\right)\cdot\left(\frac{1}{\tau_3}\right)^3\cdot s}{\left(s+\frac{1}{\tau_c}\right)^3\cdot\left(s+\frac{1}{\tau_1}\right)\cdot\left(s+\frac{1}{\tau_2}\right)\cdot\left(s+\frac{1}{\tau_3}\right)^3}$

Table 9. Complete shaper transfer function, and the transfer functions from the noise nodes to output. Includes the parasitic poles from the gain stages and the op amps.

Node	Transfer Function to Output Including Parasitic Poles from Gain Stages and Op Amps
Complete Shaper Transfer Function	$H(s)=\dfrac{(683.9)\cdot\left(\frac{1}{\tau_b}\right)^4\cdot\left(\frac{1}{\tau_1}\right)\cdot\left(\frac{1}{\tau_2}\right)^2\cdot\left(\frac{1}{\tau_3}\right)^3\cdot s^2}{\left(s+\frac{1}{\tau_a}\right)^2\cdot\left(s^2+\frac{s}{Q\cdot\tau_b}+\left(\frac{1}{\tau_b}\right)^2\right)^2\cdot\left(s+\frac{1}{\tau_1}\right)\cdot\left(s+\frac{1}{\tau_2}\right)^2\cdot\left(s+\frac{1}{\tau_3}\right)^3}$
A	$H_A(s)=\dfrac{(683.9)\cdot\left(\frac{1}{\tau_b}\right)^4\cdot\left(\frac{1}{\tau_1}\right)\cdot\left(\frac{1}{\tau_2}\right)^2\cdot\left(\frac{1}{\tau_3}\right)^3\cdot s}{\left(s+\frac{1}{\tau_a}\right)\cdot\left(s^2+\frac{s}{Q\cdot\tau_b}+\left(\frac{1}{\tau_b}\right)^2\right)^2\cdot\left(s+\frac{1}{\tau_1}\right)\cdot\left(s+\frac{1}{\tau_2}\right)^2\cdot\left(s+\frac{1}{\tau_3}\right)^3}$
B	$H_B(s)=\dfrac{(82.7)\cdot\left(\frac{1}{\tau_b}\right)^4\cdot\left(\frac{1}{\tau_1}\right)\cdot\left(\frac{1}{\tau_2}\right)\cdot\left(\frac{1}{\tau_3}\right)^3\cdot s}{\left(s+\frac{1}{\tau_a}\right)\cdot\left(s^2+\frac{s}{Q\cdot\tau_b}+\left(\frac{1}{\tau_b}\right)^2\right)^2\cdot\left(s+\frac{1}{\tau_1}\right)\cdot\left(s+\frac{1}{\tau_2}\right)\cdot\left(s+\frac{1}{\tau_3}\right)^3}$
C	$H_C(s)=\dfrac{(82.7)\cdot\left(\frac{1}{\tau_b}\right)^3\cdot\left(\frac{1}{\tau_1}\right)\cdot\left(\frac{1}{\tau_2}\right)\cdot\left(\frac{1}{\tau_3}\right)^3\cdot s}{\left(s+\frac{1}{\tau_a}\right)^2\cdot\left(s^2+\frac{s}{Q\cdot\tau_b}+\left(\frac{1}{\tau_b}\right)^2\right)\cdot\left(s+\frac{1}{\tau_1}\right)\cdot\left(s+\frac{1}{\tau_2}\right)\cdot\left(s+\frac{1}{\tau_3}\right)^3}$
D	$H_D(s)=\dfrac{(82.7)\cdot\left(\frac{1}{\tau_b}\right)^2\cdot\left(\frac{1}{\tau_1}\right)\cdot\left(\frac{1}{\tau_2}\right)\cdot\left(\frac{1}{\tau_3}\right)^3\cdot s}{\left(s+\frac{1}{\tau_a}\right)\cdot\left(s^2+\frac{s}{Q\cdot\tau_b}+\left(\frac{1}{\tau_b}\right)^2\right)\cdot\left(s+\frac{1}{\tau_1}\right)\cdot\left(s+\frac{1}{\tau_2}\right)\cdot\left(s+\frac{1}{\tau_3}\right)^3}$

Table 10. Hand calculated noise voltage at the output. Q=0.56. Noise numerically integrated from 10Hz to 10MHz.

Source Node	Squared Noise Voltage at Output (integrated from 10Hz to 10MHz)
A	2.65830E-4 V^2
B	7.70673E-6 V^2
C	3.4506E-6 V^2
D	2.29092E-5 V^2
mean-squared sum of squares $\overline{v_{ol}^2}$	2.99896E-4 V^2
RMS noise voltage at the output	0.01732 V_{rms}

Table 11. Prototype pulse shaper bias and signal lines.

Vc_1	0.5V	Vcontrol 1 - Controls the Gm of two of the transconductors in each biquad.
Vc_2	0.5V	Vcontrol 2 - Controls the Gm of two of the transconductors in each biquad and Full_Gm.
Vcg1_1	0.5	Vcg1_1 - Gain control Voltage, Gain block #1, voltage 1
Vcg1_2	0.5	Vcg1_2 - Gain control Voltage, Gain block #1, voltage 2
Vcg2_1	0.5	Vcg2_1 - Gain control Voltage, Gain block #2, voltage 1
Vcg2_2	0.5	Vcg2_2 - Gain control Voltage, Gain block #2, voltage 2
I1bias	30uA	I1 bias current
I2bias	10uA	I2 bias current
Icm	20uA	Icm bias current (for common mode feedback circuit)
Ir4b_bias	80uA	RHIC4B bias line
VDD	5V	VDD
VSS	0V	VSS
VMID	2.5V	VMID
Vin_Shaper	N/A	Vin_Shaper
Vout_Shaper	N/A	Shaper Output

Table 12. Prototype Chip Transconductor parameters using MOSIS n91a process models.

	Full_Gm1b	**Full_Gm1c**	**Full_Gm3b**
$(W/L)_5$	14μ/14μ	4.8μ/9.6μ	21.6μ/4.8μ
g_{ds5}	32.8535μS	11.7292μS	156.0924μS
Nominal G_m (V_c=0.5V)	23.1μS	10.2μS	93μS

Table 13. G_m of the transconductor circuits for V_c=0 to 1.5V. N91a process and measured data.

Vc	Measured Full_Gm1b	SPICE Full_Gm1b	SPICE Full_Gm1c	SPICE Full_Gm3b
0	2.8387E-05	2.68E-05	1.16E-05	1.06E-04
0.1	2.7631E-05	2.61E-05	1.13E-05	1.03E-04
0.2	2.6799E-05	2.54E-05	1.10E-05	1.01E-04
0.3	2.5877E-05	2.46E-05	1.07E-05	9.79E-05
0.4	2.5196E-05	2.39E-05	1.04E-05	9.50E-05
0.5	2.4282E-05	2.31E-05	1.01E-05	9.20E-05
0.6	2.3429E-05	2.24E-05	9.81E-06	8.99E-05
0.7	2.2732E-05	2.16E-05	9.50E-06	8.57E-05
0.8	2.2043E-05	2.08E-05	9.18E-06	8.25E-05
0.9	2.0891E-05	2.00E-05	8.86E-06	7.91E-05
1	2.0014E-05	1.91E-05	8.53E-06	7.57E-05
1.1	-	1.83E-05	8.19E-06	7.21E-05
1.2	-	1.74E-05	7.85E-06	6.84E-05
1.3	-	1.65E-05	7.51E-06	6.47E-05
1.4	-	1.56E-05	7.16E-06	6.08E-05
1.5	-	1.46E-05	6.80E-06	5.67E-05
1.6	-	1.37E-05	6.44E-06	5.26E-05
1.7	-	1.27E-05	6.07E-06	4.83E-05
1.8	-	1.17E-05	5.69E-06	4.38E-05
1.9	-	1.06E-05	5.30E-06	3.92E-05
2	-	9.56E-06	4.91E-06	3.45E-05

Table 14. Gain cell modes of operation.

Mode	G_{m1} V_c=0V	G_{m1} V_c=2V
Low Gain: G_{m2} V_c=0V.	9.1 V/V	3 V/V
High Gain: G_{m2} V_c=2V	21.6 V/V	7 V/V

Table 15. Prototype Chip Bias Settings

Signal	Bias Value for Maximum Shaper Output Signal Swing
VMID	2.75V
Vc_1	0.1V
Vc_2	0.1V
Vcg1_1	0V
Vcg1_2	0V
Vcg2_1	2V
Vcg2_2	0V

Table 16. Prototype Pulse Shaping Amplifier Response to an Input Step Pulse.

Input Pulse Amplitude	16mV
Input Pulse 10%-90% Rise Time	~17nsec
Start of input pulse to 1st lobe V_{min} (2.14V)	615nsec
Start of input pulse to zero crossing (2.76V)	920nsec
Start of input pulse to 2nd lobe V_{max} (3.16V)	~1.245μsec
Start of input pulse to 10% of final baseline (2.8V)	~1.95μsec
Start of bipolar pulse to 1st lobe V_{min} (2.14V)	415nsec
Start of bipolar pulse to zero crossing (2.76V)	720nsec
Start of bipolar pulse to 2nd lobe V_{max} (3.16V)	~1.035μsec
Start of bipolar pulse to 10% of final baseline (2.8V)	~1.75μsec

Table 17. Effect of biquad quality factor on pulse symmetry.

Q	ω_o	V_c_1	V_c_2	V_{mid}-V_{low}	VMID-V_{high}	Pulse Lobe Ratios
0.558	8.17Mrad/sec	0	0	776mV	488mV	0.629
0.599	7.60Mrad/sec	0	0.5V	784mV	520mV	0.663
0.658	7.55Mrad/sec	0	1V	800mV	572mV	0.715
0.750	6.08Mrad/sec	0	1.5V	800mV	664mV	0.830

Table 18. Pulse shaping amplifier experimental noise measurements and predictions.

Measurement	Peak Gain at Midband	RMS Noise Voltage at the Shaper's Ouput
Experimental measurement of prototype shaper's noise using HP3400A	39.8dB	7.7mV_{rms}
Experimental measurement of prototype shaper's noise using pulse height analyzer	39.8dB	8.5 mV_{rms}
SPICE simulation of prototype shaper using fabrication run models.	32.0dB	5.2 mV_{rms}
SPICE simulation of shaper using fixed transconductors and experimentally determined bias settings.	36.6dB	7.7mV_{rms}
Hand calculation of the noise using the shaper's transfer function and the estimated gain at the experimentally determined operating points.	29.3dB	6.5mV_{rms}
SPICE simulation of the shaper using the fixed transconductors and nominal bias points (Chapter 3 calculation). V_c of all gain cell transconductors is 0.5V.	43.2dB	16.2 mV_{rms}
Hand calculation of the noise using the shaper's transfer function and the estimated gain at the nominal bias points (Chapter 3 calculation). V_c of all gain cell transconductors at 0.5V	37.7dB	17.64 mV_{rms}

Table 19. Pulse shaper output signal to noise ratio.

Input Signal	Shaper Output Baseline to Peak	Shaper Output Noise (volts RMS)	Shaper Output SNR (dB)
16mV	620mV	7.70mV	38.1 dB
1.6mV	60mV	7.70mV	17.8 dB

Table 20. HSPICE operating point information on the transistors in the transconductor circuit.

Device	I_D	V_{gs}	V_{ds}	V_{bs}	V_{th}	V_{dsat}	g_m	g_{ds}	g_{mb}	C_{gs}	C_{gd}
M_1	-10.05u	-1.20	-2.83	1.30	-967.5m	-247.2m	79.50u	4.25u	12.28u	72.83f	7.92f
M_2	-10.05u	-1.20	-2.83	1.30	-967.5m	-247.2m	79.50u	4.25u	12.28u	72.83f	7.92f
M_3	20.53u	866.2m	3.70	0.00	626.1m	202.6m	144.1u	1.02u	63.86u	38.77f	6.98f
M_4	20.53u	866.2m	3.70	0.00	626.1m	202.6m	144.1u	1.02u	63.86u	38.77f	6.98f
M_5	0.00	-3.20	0.00	1.30	-1.08	-1.96	0.00	34.87u	0.00	110.6f	103.7f
M_6	17.07u	866.2m	554.6m	0.00	627.4m	201.6m	125.2u	1.62u	55.64u	38.84f	7.02f
M_7	17.07u	866.2m	554.6m	0.00	627.4m	201.6m	125.2u	1.62u	55.64u	38.84f	7.02f
M_8	-17.07u	-1.22	-713.2m	0.00	-803.1m	-385.4m	78.38u	4.73u	19.20u	47.24f	5.16f
M_9	-17.07u	-1.22	-713.2m	0.00	-803.1m	-385.4m	78.38u	4.73u	19.20u	47.24f	5.16f
M_{10}	10.05u	799.8m	866.2m	0.00	627.3m	157.3m	95.92u	801.0n	43.04u	38.54f	6.99f
M_{12}	10.05u	799.8m	866.2m	0.00	627.3m	157.3m	95.92u	801.0n	43.04u	38.54f	6.99f
M_{13}	-30.59u	-1.23	-1.30	0.00	-782.6m	-402.7m	130.1u	7.84u	32.10u	74.00f	7.85f
M_{14}	-30.59u	-1.23	-1.30	0.00	-782.6m	-402.7m	130.1u	7.84u	32.10u	74.00f	7.85f
M_{16}	-4.47u	-2.02	-2.02	0.00	-925.3m	-776.6m	7.51u	574.8n	1.87u	2.80f	2.50E-16
M_{17}	-4.47u	-1.36	-1.36	2.02	-1.14	-249.3m	35.61u	1.90u	4.68u	36.36f	3.97f
M_{19}	4.47u	1.62	1.62	0.00	666.7m	561.6m	8.990u	85.29n	3.69u	4.47f	3.56E-16
M_{20}	-4.47u	-2.02	-2.02	0.00	-925.3m	-776.6m	7.51u	574.8n	1.87u	2.80f	2.50E-16
M_{21}	-4.47u	-1.36	-1.36	2.02	-1.14	-249.3m	35.61u	1.90u	4.68u	36.36f	3.97f
M_{23}	4.47u	1.62	1.62	0.00	666.7m	561.6m	8.99u	85.29n	3.69u	4.47f	3.56E-16
M_{24}	-17.07u	-1.31	-1.76	713.2m	-909.5m	-392.6m	79.23u	4.64u	14.69u	46.94f	5.10f
M_{25}	-17.07u	-1.31	-1.76	713.2m	-909.5m	-392.6m	79.23u	4.64u	14.69u	46.94f	5.10f
M_{26}	17.07u	1.06	1.97	-554.6m	844.2m	204.0m	132.8u	1.01u	43.59u	38.42f	6.98f
M_{27}	17.07u	1.06	1.97	-554.6m	844.2m	204.0m	132.8u	1.01u	43.59u	38.42f	6.98f

Vita

Kevin Behel was born on March 31, 1973 in Knoxville, Tennessee. After graduating from Bearden High School in 1991, he continued his education at the University of Tennessee at Knoxville. While an undergraduate, he participated in student co-op programs at CTI PET Systems, Inc., and at Silicon Graphics, Inc. He received his B.S.E.E. in 1997 and his M.S.E.E. in 1999, both from the University of Tennessee at Knoxville.