Incorporation of High-k HfO2 Thin Films in a-IGZO Thin Film Transistor Devices

A Thesis Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Aaron Hamilton Bales

December 2015

Acknowledgements

First, I would like to thank Dr. Philip Rack for providing the idea for this project, guidance along the way, funding, and input on this thesis. In addition, Dr. Joo Hyon Noh has taught me everything I need to know about thin film transistors, including device fabrication, characterization, and applications. These skills he taught me will be invaluable as I continue with my career. Dr. Pushpa Pudasaini has also been a great help in this endeavor, as he has helped with fabrication and testing, as well as providing me with guidance when I needed it. Another huge thank you goes to all of the staff members at the Center for Nanophase Materials Sciences at Oak Ridge National Laboratory, as they trained me on the necessary equipment and provided assistance whenever I needed it. Finally, thanks to Dr. Thomas Meek and Dr. Jason Fowlkes for being a part of my thesis committee and providing valuable input.

Abstract

In this study, HfO_2 [hafnium oxide] thin films are investigated extensively as part of indium gallium zinc oxide (IGZO) thin film transistor (TFT) devices. They are incorporated into the TFTs, both as a gate insulator and a passivation layer. First, the HfO_2 [hafnium oxide] films themselves are investigated through an annealing study and through I-V and C-V measurements. Then, HfO_2 [hafnium oxide] is suggested as a replacement for commonly used SiO_2 [silicon dioxide] gate insulator, as it has a dielectric constant that is 4 – 6 times higher. This higher dielectric constant allows for comparable TFT performance at a lower operation voltage (5 V vs. 20 V). Finally, HfO_2 [hafnium oxide] is applied as a passivation layer in IGZO TFTs, and an annealing study is conducted to determine which processing steps will allow for optimal TFT performance. The HfO_2 [hafnium oxide] passivation layer proves to show a good level of uniformity. Therefore, taking all results into consideration, both HfO_2 [hafnium oxide] gate insulators and passivation layers can be used in conjunction with IGZO TFTs to produce a full electrowetting array, which should prove to be useful in “lab on a chip” studies.

Table of Contents

Chapter 1 Introduction ……1

1.1. Transistors: A Brief History/Types…….....……1

1.1.1. TFT Structures ……..…….2

1.1.2. TFT Operation ……..…….3

1.1.3. TFT Characterization: Output and Transfer Curves ……..……6

1.1.4. Amorphous Oxide Semiconductors: IGZO ……..…….9

1.2. High-κ Dielectrics …….……11

1.2.1. Hafnium (IV) Oxide (HfO_2) and its Performance in IGZO TFTs ……...13

1.2.2. ALD of HfO_2 – Precursors…….……..17

1.2.3. TEMAH Properties from CNMS ALD……18

1.3. Logic Gate Circuits …….18

1.4. Motivation for this Work ……20

Chapter 2 Experimental Procedures……...23

2.1. IGZO TFT Fabrication Overview ……...23

2.1.1. Photolithography……..24

2.1.2. Gate Electrode……..25

2.1.3. Gate Insulator……...25

2.1.4. IGZO Active Layer……..25

2.1.5. Source/Drain Electrodes ……..26

2.1.6. Passivation ……...26

2.1.7. Via Hole ……...27

2.2. Annealing……27

2.3. Electrical Measurements……27

Chapter 3 HfO_2 Film Characterization ……..29

3.1. Overview……29

3.2. Experimental Procedure……..29

3.3. Results and Discussion ……...30

3.3.1. I-V Characterization……30

3.3.2. C-V Characterization ……...32

3.3.3. Ellipsometry……36

Chapter 4 IGZO TFT Performance: HfO_2 G.I. Compared to Previous SiO_2 G.I. Data……37

4.1. Overview……37

4.2. Results and Discussion……37

Chapter 5 HfO_2 Passivation: Annealing Treatments Test ……...……43

5.1. Overview……43

5.2. Results and Discussion……45

Chapter 6 HfO_2 Passivation: Wafer Level Uniformity Test ……51

6.1. Overview……51

6.2. Experimental ……51

6.3. Results and Discussion……53

Chapter 7 Conclusions ……57

List of References ..……58

Vita……....……61

List of Tables

Table 1-1. Properties of various dielectric materials …….12

Table 1-13. Truth tables for logic gate circuit elements…….21

Table 3-1. Calculated κ values at varying frequencies and annealing temperatures …….35

Table 3-2. HfO_2 ellipsometry data …….36

Table 4-1. Specific fabrication process for IGZO TFTs with HfO_2 G.I. ……...38

Table 5-1. Specific fabrication process for HfO_2 PVX……...……...44

Table 6-1. Specific fabrication process for HfO_2 PVX Wafer Level Uniformity…….……54

List of Figures

Figure 1-1. Types of TFT structures ……2

Figure 1-2. Gradual channel approximation schematic ……...4

Figure 1-3. Output and transfer characteristics for an a-Si TFT……..7

Figure 1-4. Saturation region V_{TH} and μ_n extrapolation ……..8

Figure 1-5. Output/transfer characteristics before/after bending in Normura's study...……10

Figure 1-6. IGZO TFT schematic used in Lin and Chou's experiment…….13

Figure 1-7. Transfer characteristics (Lin and Chou)……..14

Figure 1-8. Variation of TFT properties with annealing temperature (Lin and Chou)……..15

Figure 1-9. IGZO TFT schematic from UF group ……16

Figure 1-10. Output and Transfer characteristics (UF group) ……...16

Figure 1-11. Oxford Instruments Auger electron analysis of HfO_2……...19

Figure 1-12. Oxford Instruments RBS analysis of HfO_2 ……...19

Figure 1-13. Logic gate element symbols……...21

Figure 2-1. Schematic of IGZO TFTs with HfO_2 G.I.……...23

Figure 3-1. I-V curves for as-deposited and annealed HfO_2 samples……31

Figure 3-2. Leakage current vs. annealing temperature…….32

Figure 3-3. C-V characteristics ……..33

Figure 3-4. Capacitance vs. annealing temperature ……...34

Figure 4-1. Output and transfer curves for IGZO TFTs with SiO_2 G.I.…….39

Figure 4-2. Transfer characteristics for IGZO TFTs with HfO_2 G.I (low T anneal).…….40

Figure 4-3. Transfer characteristics for IGZO TFTs with HfO_2 G.I (high T anneal).……42

Figure 5-1. Sample 1 transfer characteristics……45

Figure 5-2. Sample 1 transfer characteristics with additional low T annealing……46

Figure 5-3. Sample 2 transfer characteristics before post-PVX annealing……47

Figure 5-4. Sample 2 transfer characteristics……48

Figure 5-5. Sample 2 transfer characteristics with additional low T annealing……50

Figure 6-1. Unit TFT array layout ……52

Figure 6-2. W/L matrix layout……52

Figure 6-3. Row/column transfer characteristics……53

Figure 6-4. Transfer characteristics after 5 and 50 days……55

Figure 6-5. W/L transfer characteristics……56

Chapter 1

Introduction

1.1. Transistors: A Brief History/Types

Starting from the broadest perspective, a transistor is a semiconductor device used to amplify and switch electronic signals. A field effect transistor typically contains three electrodes (electrical leads) consisting of the gate, source, and drain. A voltage can be applied to the gate, which causes an increase in current and the conductivity between source/drain electrodes. The invention of the transistor is credited to Bardeen, Brattain, and Shockley of Bell Laboratories in 1946-1947. The transistor proved to be a good alternative to the vacuum or electron tube, and eventually researchers began using them in integrated circuits. Today, transistors are commonly used in computer memory applications [1].

The invention of the transistor gave way to the creation of different transistor types that were used as field-effect devices. Field-effect devices are those whose properties, specifically conductivity for transistors, change in the presence of an electric field. Types of field-effect transistors include metal-semiconductor field-effect transistors (MESFETs), junction field-effect transistors (JFETs), and metal-oxide-semiconductor field-effect transistors (MOSFETs). Thin film transistors (TFTs), another type of field-effect transistor, have a structure/operation that is very similar to MOSFETs [1,2].

1.1.1. TFT Structures

As previously stated, a common field effect transistor typically consists of three electrodes: a gate, source, and drain. A TFT follows this structure, also employing a gate dielectric/insulator layer and a semiconducting active layer. The difference in MOSFETs and TFTs lies in the fact that MOSFETS use the bulk semiconductor (usually silicon) substrate as an active layer, whereas in TFTs the active layer is a thin film deposited separately. A few examples of TFT semiconducting active layers that have been researched extensively are amorphous silicon (a-Si), polycrystalline silicon (poly-Si), and cadmium selenide (CdSe) [2].

Changing the order of layer deposition changes the TFT structure type [2]. The four common structures of TFTs are shown in Figure 1-1 below.

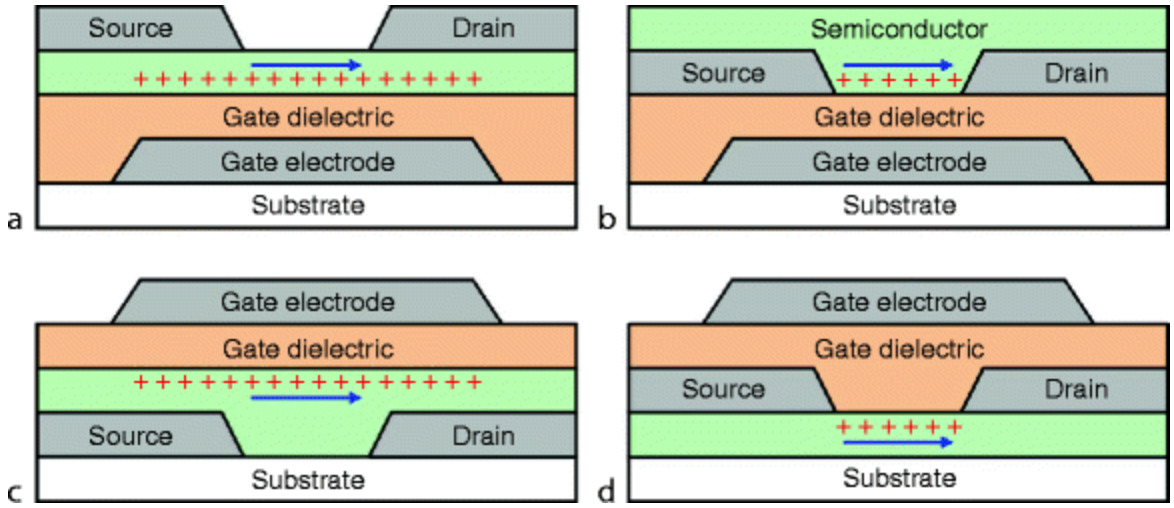

Figure 1-1. Types of TFT structures: (a) inverted-staggered (bottom gate), (b) inverted-coplanar, (c) staggered, and (d) coplanar [3].

The TFT structure type is based upon two factors: the position of the gate itself and the relative position between the gate and source/drain electrodes. An inverted structure means the gate

electrode is deposited directly onto the substrate, thus on the bottom of device. On the other hand, a non-inverted TFT has the gate on the top of the device. Staggered structure means that the gate is on the opposite side of the semiconductor active layer from the source/drain electrodes, whereas in a coplanar structure, all three electrodes are on the same side of the semiconductor. The usage of each structure depends on its intended application. For example, the inverted-staggered TFT structure is commonly used in producing active-matrix liquid crystal displays (LCD) panels [2]. For this work, TFT devices employing the inverted-staggered structure will be synthesized and analyzed.

1.1.2. TFT Operation

TFTs, like standard transistors, operate through a bias being applied to the gate electrode (V_G or V_{GS}), which causes a change in conductivity in the active semiconductor between the source and drain electrodes. Depending on the size of the gate bias in relation to other factors, a TFT can operate in two operational regimes known as the linear and saturation regions [2].

In the linear region, when the gate voltage is much larger than the drain voltage (V_D or V_{DS}), drain current (I_D or I_{DS}) increases linearly with increasing drain voltage. In this linear region, I_D can be calculated as a function of both V_G and V_D, along with other material constants. For the following set of calculations, assume a gradual channel approximation, which means that the whole TFT device will be viewed as a chain of individual smaller 1D devices [2]. Figure 1-2 illustrates how a gradual channel approximation is used to make these calculations. The x-direction is perpendicular and the y-direction is parallel to the channel. The carrier density per unit area depends on distance y, and the channel potential V(y) is a function of V_D. Here, one

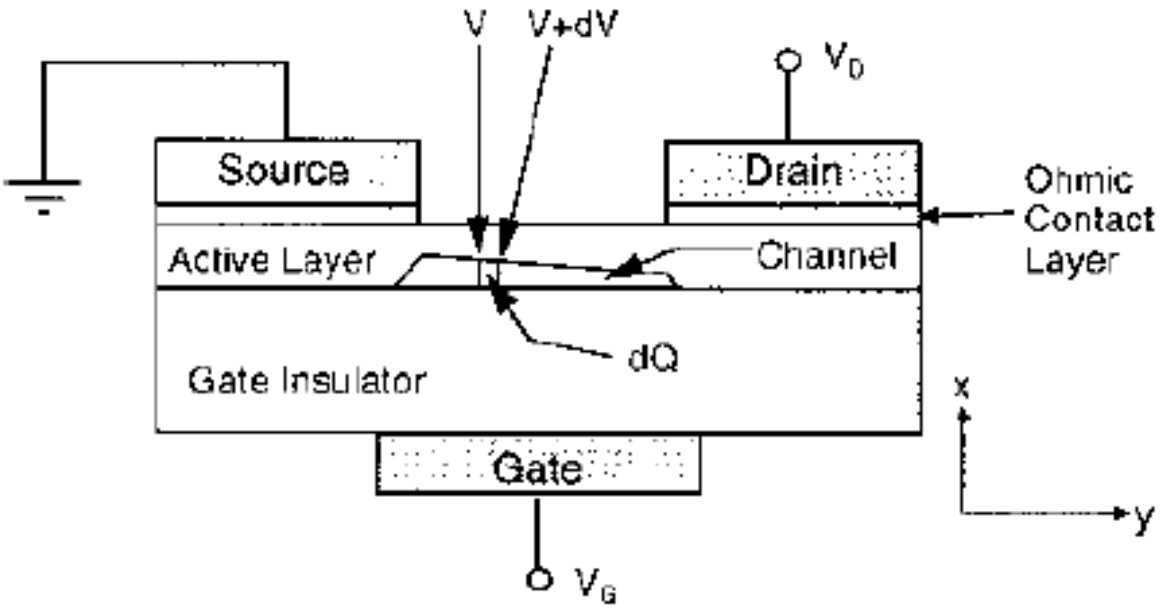

Figure 1-2. A TFT schematic used in gradual channel calculations [2].

material factor that comes into play is the threshold voltage (V_{TH}), which is the V_G value at which the current flow through the device becomes much stronger; in other words, this V_G value causes the formation of a conducting path between the source and drain electrodes [4]. The mobile charge (Q_t) can be calculated with Equation 1.1, if the channel potential V is assumed to be nonzero.

$$Q_t = -C_{GI}(V_G - V_{TH} - V) \qquad \text{Eq. 1.1}$$

C_{GI} represents the capacitance per unit area of the gate insulator. The current induced by majority carriers is given by Equation 1.2.

$$I_D = W\mu_n Q_t E_y \qquad \text{Eq. 1.2}$$

W represents the length of the channel, μ_n is the electron mobility, and E_y is the electric field at distance y. The current density, assuming a diffusion term does not contribute, is given in Equation 1.3.

$$J_n = \frac{I_n}{A} = q\left(\mu_n nE + d_n \frac{dn}{dx}\right) \qquad \text{Eq. 1.3}$$

Considering $E_y = -\frac{dV}{dy}$ and substituting this in to Equations 1.1 and 1.2, followed by integrating from 0 to channel length L (V = 0 to V_D), the gradual channel expression for drain current can be calculated as in Equation 1.4.

$$I_D = C_{GI}\mu_n \frac{W}{L}\left[(V_G - V_{TH})V_D - \frac{1}{2}V_D^2\right] \qquad \text{Eq. 1.4}$$

Finally, considering a TFT operating in the linear regime ($V_D << V_G$), the drain current is calculated in Equation 1.5 [2].

$$I_D = C_{GI}\mu_n \frac{W}{L}(V_G - V_{TH})V_D \qquad \text{Eq. 1.5}$$

As V_D continues to increase, eventually it reaches a point where $V_D = V_G - V_{TH}$. At this point, the electron channel becomes pinched off, and the drain current saturates. The saturation region begins where the drain voltage increases beyond this point (where $V_D > V_G - V_{TH}$). This means that Equations 1.4 and 1.5 for drain current no longer apply, and a new expression must be written to account for this condition (Equation 1.6) [2].

$$I_D = \frac{C_{GI}\mu_n W}{2L}(V_G - V_{TH})^2 \qquad \text{Eq. 1.6}$$

1.1.3. TFT Characterization: Output and Transfer Curves

The main method of measuring TFTs electrical properties is using a probe station. Using the probe station with a semiconductor analyzer, two of the most important TFT characteristics, output and transfer characteristics, can be measured. The output characteristic is found by measuring drain current as a function of drain voltage at different gate voltage steps. On the other hand, the TFT transfer characteristic is found by measuring drain current as a function of gate voltage, using a number of drain voltage steps. Figure 1-3 shows an example of output and transfer curves for an amorphous silicon TFT. The transfer curve is more important in determining the overall quality of the TFT, but the output curve is also significant in showing the linear to saturation region transition. In Figure 1-3 (a), at each gate voltage, it can be seen that up to a certain drain voltage, the drain current increases linearly. Using the same graph, the point at which the drain current saturates (levels off) can be estimated as well. ON current, OFF current, and subthreshold swing are related properties that can be determined using a TFT transfer curve. The OFF current is the current on the transfer curve where the TFT is operating at a very low current (OFF state), whereas the ON current is orders of magnitude higher,

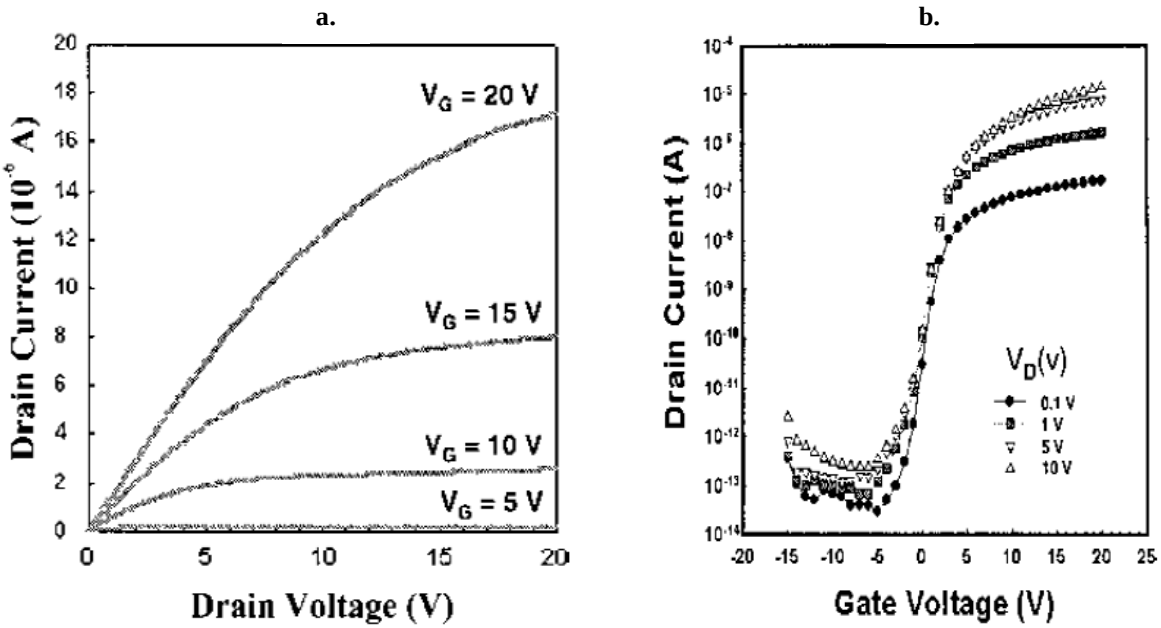

Figure 1-3. (a) Output and (b) transfer characteristics of an a-Si TFT [2].

meaning the TFT is considered to be turned on. The ratio I_{ON}/I_{OFF} is an important factor because it shows how well the TFT works as a switching device and how well a conducting path is formed between the source/drain electrodes and importantly the difference in the on and off states. Subthreshold or gate voltage swing, is the amount of gate voltage that will increase the drain current by a factor of 10. It is measured in units of V/decade, and it is found by finding the maximum slope on the TFT transfer curve [2].

The TFT transfer curve can be manipulated in order to determine other important properties. For instance, if the square root of the drain current is plotted as a function of gate voltage in the saturation region, one can determine the threshold voltage and electron mobility. This type of plot is shown in Figure 1-4.

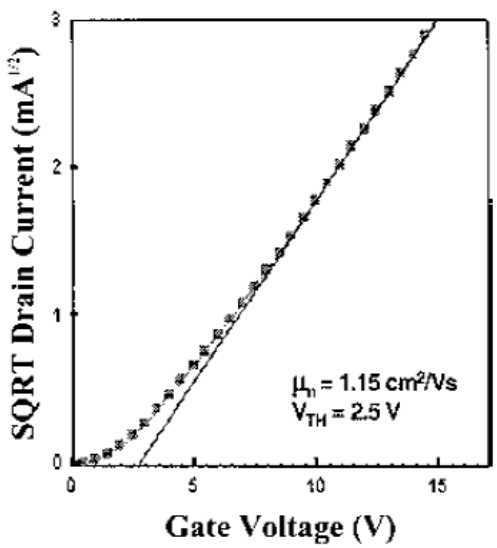

Figure 1-4. Saturation region extrapolation of the threshold voltage and electron mobility. Once the data is fit with a linear function, the slope represents the field-effect mobility, and the x-intercept is the threshold voltage [2].

1.1.4. Amorphous Oxide Semiconductors: IGZO

In recent years, transparent electronics fabricated on flexible substrates have become more prevalent. They can be involved in applications such as paper displays and wearable computers. While hydrogenated amorphous silicon has been studied extensively for use in flexible devices, their performance is not quite good enough for this application. Their field effect mobilities are much too low – on the order of 1 cm^2/V-s. Amorphous oxide semiconductors are one answer to this issue, as they have a significantly larger mobility, which can potentially be larger than10 cm^2/V-s. A study by Kenji Nomura includes fabrication and performance of TFTs made with an indium gallium zinc oxide (IGZO) active layer. These IGZO films were prepared using pulsed laser deposition. To test the usefulness as a flexible substrate, electrical measurements were conducted both before and after bending and as shown in Figure 1-5.

Before bending (a) and (b), the OFF current is on the order of 10^{-7} A, and the I_{ON}/I_{OFF} ratio is around 10^3. In addition, the threshold voltage is around 1.6 V, and the estimated saturation and field effect mobilities were 8.3 cm^2/V-s and 5.6 cm^2/V-s, respectively. After bending, μ_{sat} was around 7 cm^2/V-s, and the I_{ON}/I_{OFF} ratio remained on the order of 10^3. Clearly, bending did not deleteriously affect the TFT characteristics, so transparent amorphous oxide materials such as IGZO are candidate materials for flexible electronics [5]. TFTs that utilize IGZO as the active material will be analyzed extensively in this study.

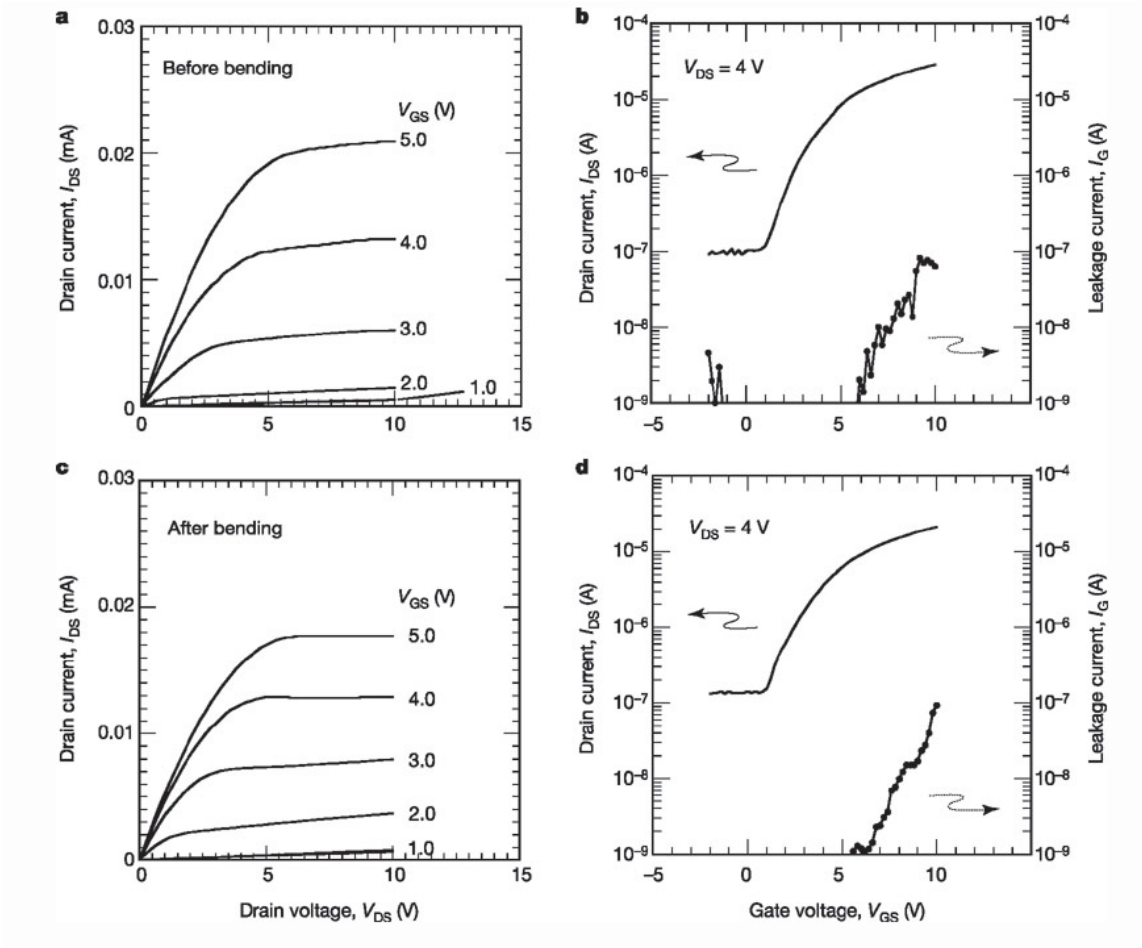

Figure 1-5. (a) Output characteristic before bending, (b) transfer characteristic before bending, (c) output characteristic after bending, and (d) transfer characteristic after bending [5].

1.2. High-κ Dielectrics

SiO_2 has been a commonly used material for the gate dielectric layer in TFTs. The desired thickness of the layer continues to decrease, as a result of Moore's Law, which deals with the fact that the number of transistors on a device has continued to increase throughout the years. While this decreased gate insulator thickness allows the transistor much to operate at higher speeds, once a SiO_2 layer becomes so small, the leakage current becomes too high, as well as increased energy dissipation and heat buildup. In addition, SiO_2 films that small have shown a lack of uniformity. Using a material with a high dielectric constant (κ) as the gate insulator solves some of this leakage current problem, as the same capacitance can be realized with a thicker film [6]. Other advantages to using a high κ material are the fact that these materials will show much less electron tunneling and be able to maintain a higher capacitance at high drive currents than lower-κ materials. In addition, having a high κ enables a TFT to operate at low voltages [7]. Table 1-1 below shows the dielectric constants and other characteristics of numerous insulating materials.

Some of the materials in Table 1-1 exhibit a far superior κ than SiO_2. However, other factors to consider are making sure that the material has the proper band gap offset to be functional with the active material. Considering IGZO as the active material, HfO_2 has not only a superior κ to SiO_2 (25 compared to 3.9), but it also has the proper band gap offset to be effective in IGZO TFTs [7]. In this study, TFTs that use this HfO_2 gate insulator will be characterized and compare to TFTs using a SiO_2 gate insulator.

Table 1-1. Dielectric constant, band gap, and conduction band offset for various dielectric materials [8].

Dielectric	κ	Band gap (eV)	CB offset (eV)
Si	-	1.1	-
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8
Y_2O_3	15	6	2.3
Ta_2O_5	22	4.4	0.35
TiO_2	80	3.5	0
La_2O_3	30	6	2.3
a-$LaAlO_3$	30	5.6	1.8
$SrTiO_3$	2000	3.2	0
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
$HfSiO_4$	11	6.5	1.8

1.2.1. Hafnium(IV) Oxide (HfO_2) and its Performance in IGZO TFTs

Hafnium (IV) Oxide (HfO_2), also known as hafnia, has become a viable candidate for use as the gate dielectric material in IGZO thin film transistors. As previously stated, it has a far larger dielectric constant (~ 6 times larger) than SiO_2. Also, HfO_2 in particular is thermodynamically stable when used in IGZO TFTs [7].

Lin and Chou from National United University conducted an experiment in which they tested temperature effects on IGZO TFTs made with a HfO_2 gate dielectric layer. The TFTs were made using a bottom gate structure as shown in Figure 1-6.

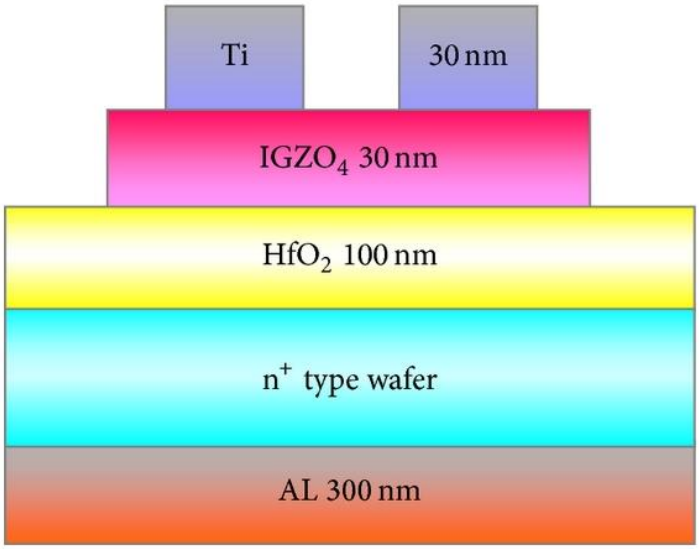

Figure 1-6. A schematic of the IGZO TFTs used in the temperature effects experiment [7].

Following fabrication, the TFTs were subjected to annealing treatments for 30 minutes ranging from 150 °C to 450 °C in 50 °C increments. Finally, the electrical characteristics of these TFTs were measured. The transfer characteristics of the TFTs are shown in Figure 1-7. The results

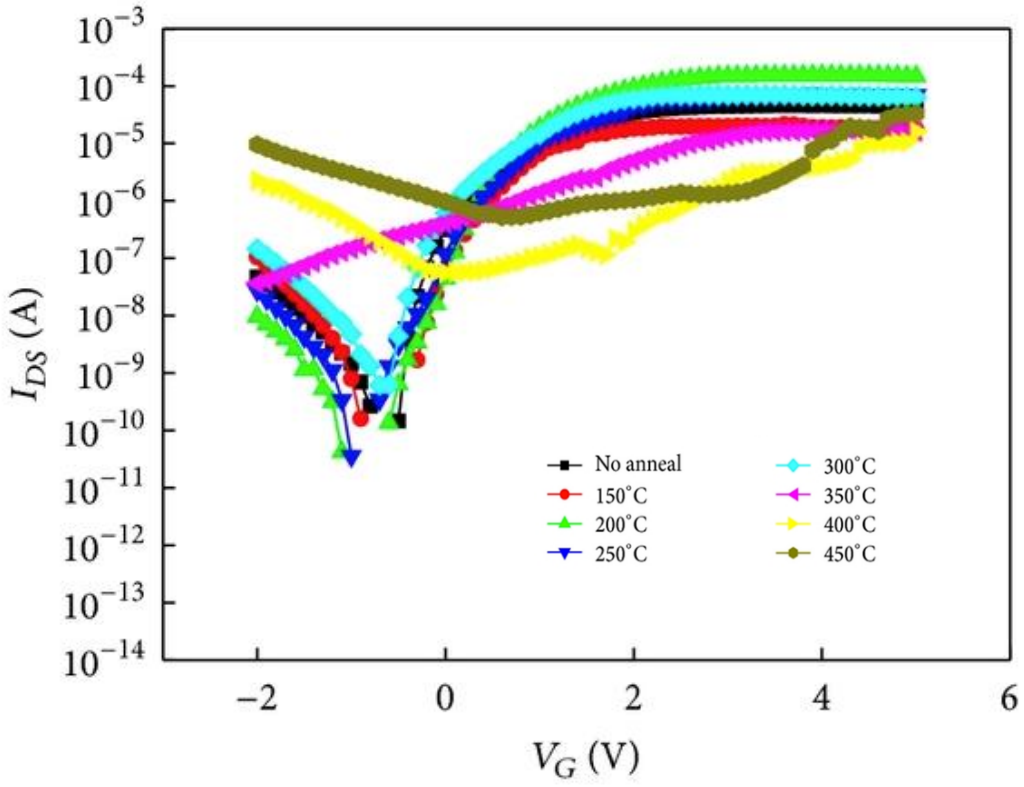

Figure 1-7. Transfer characteristics of IGZO TFTs made with an HfO_2 gate dielectric, annealed at varying temperatures [7].

show that the TFT transfer characteristics improve with 150 and 200 °C anneals. Increasing annealing temperature past 200 °C causes a decline in transfer characteristics up to 350 °C, above which the curves no longer resemble a typical TFT transfer curve. Figure 1-8 shows how important TFT characteristics, such as ON/OFF current ratio and subthreshold swing (SS), change with annealing temperature.

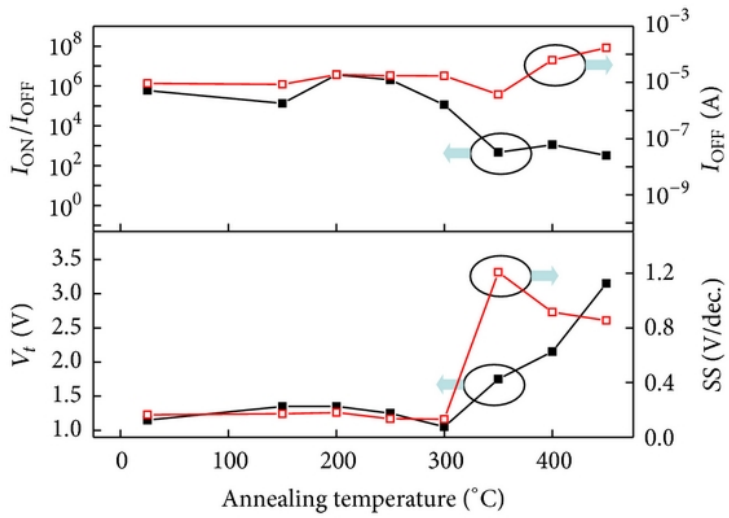

Figure 1-8. Variation of I_{ON}/I_{OFF}, I_{OFF}, threshold voltage (V_t), and SS with annealing temperature [7].

In light of both the transfer curves and the variation in TFT characteristics with annealing temperature, Lin and Chou determined that the optimal annealing temperature for IGZO TFTs made with an HfO_2 gate dielectric is 200 °C. In addition to good electrical characteristics, this method of heat treating the TFTs provides a low thermal budget, making them relatively inexpensive to mass produce [7].

Another study by Wantei Lim and his group at the University of Florida incorporates a sputtered HfO_2 gate dielectric layer into bottom gate IGZO TFTs deposited on glass substrates. Figure 1-9 shows a schematic of their TFTs, and Figure 1-10 shows the output and transfer characteristics.

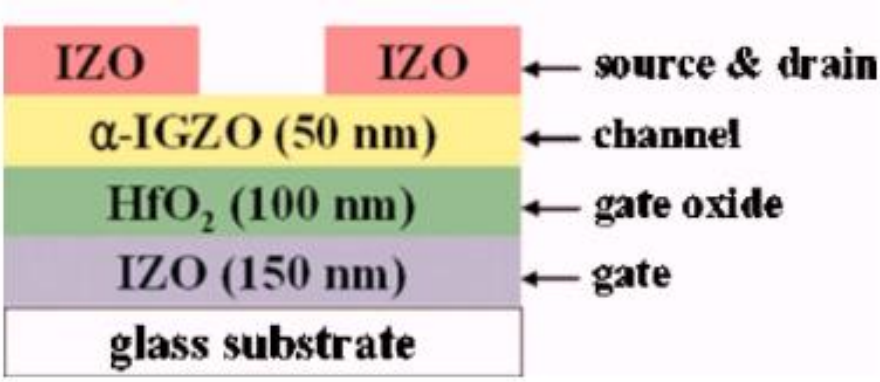

Figure 1-9. A schematic of the IGZO TFTs made by the group at UF. A 6 μm gate length and 100 μm gate width were used [9].

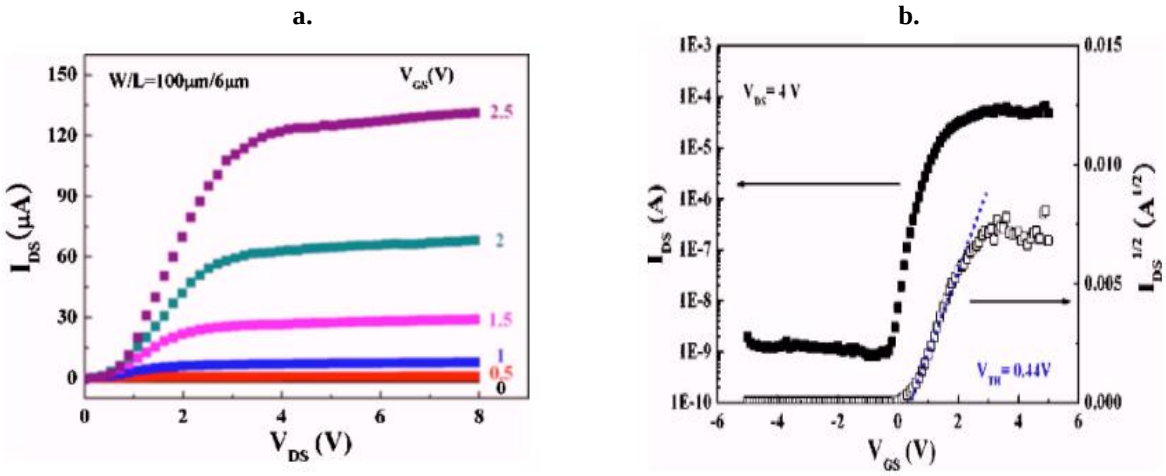

Figure 1-10. (a) Output and (b) transfer curves for the IGZO TFTs with a sputtered HfO_2 gate dielectric [9].

Lim et al reported a saturation mobility of 7.2 cm^2/V-s, a threshold voltage of 0.44 V, I_{ON}/I_{OFF} of around 10^5, and a subthreshold swing of 0.25 V/decade. In addition, they aged the TFTs for 1000 hours at room temperature, yielding promising results. The saturation mobility of the TFTs remained nearly the same after aging. In addition, the threshold voltage changed by as little as 460 mV. These characteristics suggest that these particular TFTs are a viable option for use on organic flexible substrates if the processing temperature is kept low enough [9].

1.2.2. ALD of HfO_2 – Precursors

HfO_2 is commonly deposited using a method known as atomic layer deposition (ALD), which is a form of chemical vapor deposition in which chemicals called precursors react with gases and the surface of the substrate in order for a desired material to be deposited in a self-limiting manner [10]. The precursors and gases used depend on which material is being deposited. For example, there are a few types of precursors that can be used to deposit HfO_2 using ALD. Hafnium amides are a very common type, consisting of amides such as tetrakis (ethylmethylamino)hafnium (TEMAH) and tetrakis (dimethylamino)hafnium. These two precursors require an oxidant to provide an oxygen source, which can be O_2, water vapor (H_2O) or ozone (O_3). Other HfO_2 precursors include hafnium nitrate (HfN_4O_{12}) and hafnium halides, such as hafnium chloride ($HfCl_4$) and hafnium iodide (HfI_4) [11].

1.2.3. TEMAH Properties from CNMS ALD

The TEMAH precursor will be used in our study as it is the precursor used in the ALD tool in the Center for Nanophase Materials Sciences (CNMS) cleanroom (Oxford Instruments). The HfO_2/TEMAH data sheet provided by Oxford Instruments shows a number of characteristics/properties of this particular HfO_2 precursor. The precursor is oxidized via an O_2 plasma and the TEMAH carrier gas, and the purge gas is Ar. HfO_2 deposited with this precursor exhibits a refractive index ranging from 1.95 to 2.05, depending on the plasma exposure time. In addition, the data sheet lists these process benefits to this precursor: true self-limiting ALD behavior, low damage/carbon content from use of remote plasma (as compared to thermal ALD), better stoichiometry (compared to thermal ALD), highly repeatable process, and highly conformal deposition. This low carbon content, which Oxford Instruments claims to be less than 2%, is demonstrated via Auger electron analysis, which is shown in Figure 1-11 below. In addition, Oxford Instruments provides a Rutherford backscattering spectrometry (RBS) analysis showing that their HfO_2 films are stoichiometric. This is shown in Figure 1-12 [12].

1.3. Logic Gate Circuits

TFTs can be used in concert with other circuit elements to form what is known as a logic gate circuit. Logic gate circuits implement Boolean functions, in which the output depends on a combination of inputs. Input and output values in a truth table are represented by 0 and 1, which represent nominal voltages. For example, for a device with a low operation voltage, 0 and 1 could represent 0 V and 5 V, respectively. In this case, the logic gate circuit elements will

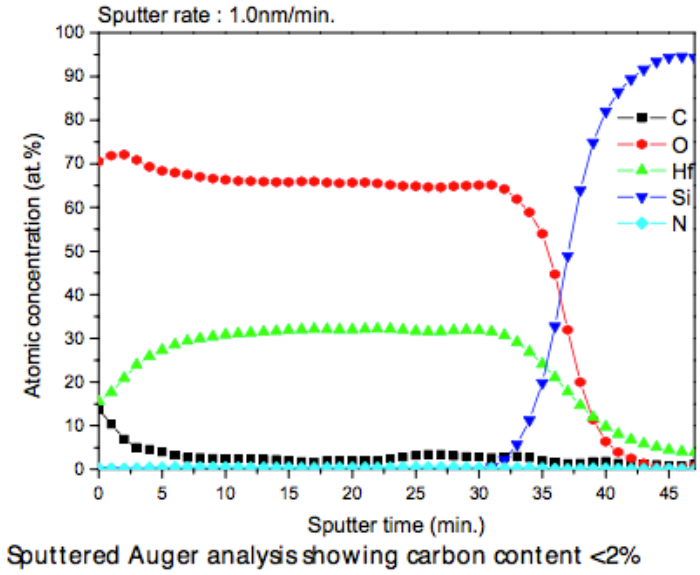

Figure 1-11. Sputtered depth profile Auger electron analysis conducted by Oxford Instruments in order to prove the low carbon content of HfO_2 films deposited with ALD and this TEMAH precursor [12].

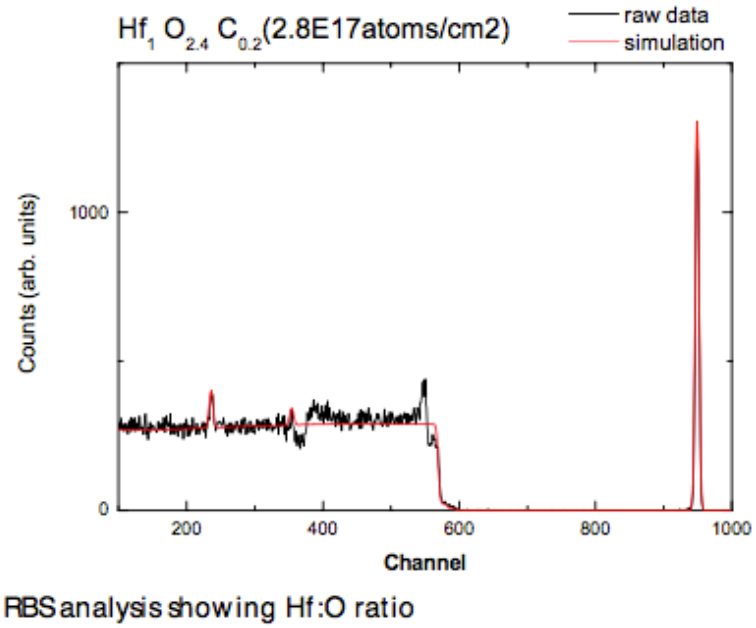

Figure 1-12. RBS analysis conducted by Oxford Instruments in order to prove the proper stoichiometry of their HfO_2 films [12].

employ an HfO_2 gate insulator, so they will operate at low voltage. The truth tables for the circuit elements can be explained by looking at when certain combinations of inputs produce a high output. AND gates exhibit a high output if all of its inputs are also high. In contrast, an OR gate only needs one or more of its inputs to be high for the output to be high. NOT gates, commonly referred to as inverters, essentially invert the input; in other words, the output is high if the input is low (and vice-versa). NAND (NOT-AND) gates consist of an AND gate and an inverter, which means it will operate oppositely to an AND gate. If any input is low, the NAND gate will exhibit a high output. NOR (NOT-OR) gates consist of an OR gate and an inverter, so if any output is high, the output will be low. EXOR (Exclusive-OR) gates are slightly more complicated, as they will only exhibit a high output if either, but not both, of the inputs are high. On the other hand, EXNOR (Exclusive-NOR) gates will exhibit a low output if either, but not both, of its inputs are high [13]. Figure 1-13 show the symbols for logic gate circuit elements, and Table 1-2 shows the truth tables for each of these elements.

1.4. Motivation for This Work

Since TFTs that utilize an HfO_2 gate insulator have become more prevalent in recent years, some of the properties of HfO_2 deposited by ALD will be studied. In addition, it is important to know the optimal processing conditions for IGZO TFT performance, such as O_2 partial pressure during IGZO deposition, HfO_2 film thickness, and annealing time/temperature. Several experiments will be conducted in order to find the optimal process flow for IGZO TFTs that utilize a HfO_2 gate insulator. Since TFT passivation is also an area of interest, HfO_2 will also be applied as a passivation layer for the TFTs, which can also act as an electrowetting

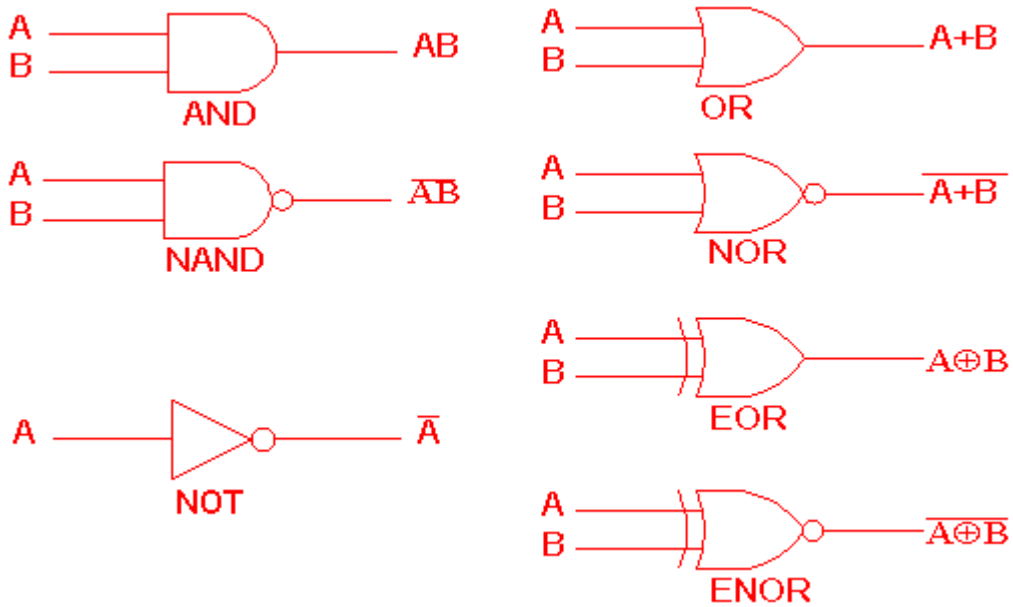

Figure 1-13. Symbols for each type of logic gate element [13].

Table 1-2. Truth tables for each of the logic gate circuit elements [13].

NOT gate	
A	Ā
0	1
1	0

INPUTS		OUTPUTS					
A	B	AND	NAND	OR	NOR	EXOR	EXNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

dielectric film. If HfO_2 passivation is successful and there is a good level of wafer uniformity, HfO_2 passivation may be able to be incorporated into a full electrowetting array. Electrowetting consists of manipulating drops of liquid on a surface electronically by capacitively changing the surface energy of a hydrophobic surface. The area where this will be most applicable is for "lab-on-a-chip" devices, which are necessary due to the ever-decreasing size of electronic devices and a need for high throughput in experiments [14].

Chapter 2

Experimental Procedures

2.1. IGZO TFT Fabrication Overview

The IGZO TFT fabrication process features numerous thin film deposition and patterning steps. The general process for fabrication will be explained below, and specifics for each experiment will be explained in the succeeding chapters. For patterning, a standard photolithography process is utilized. A bottom gate TFT structure will be used exclusively in this work (see Figure 1-1). Fabrication work for these TFTs was conducted in the Center for Nanophase Materials Sciences (CNMS) cleanroom or at the thin films lab at the University of Tennessee, Knoxville. A schematic of the TFTs is shown in Figure 2-1.

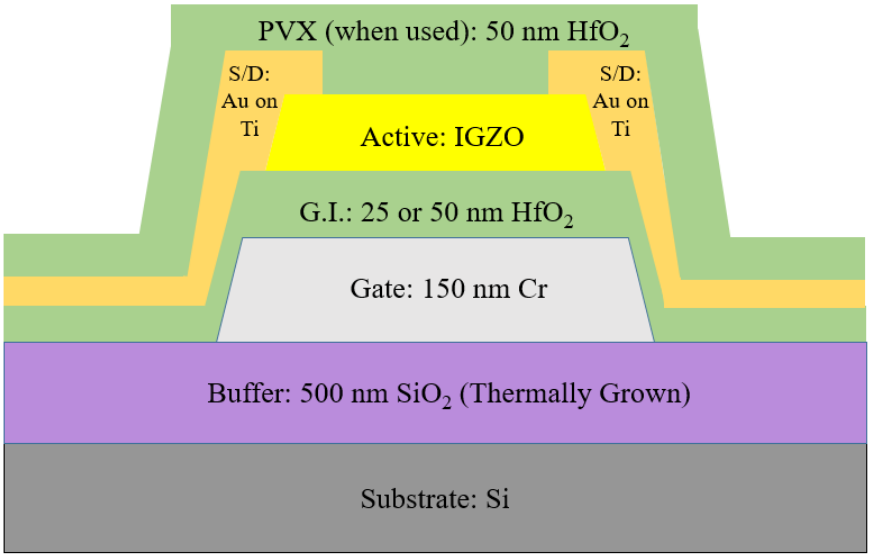

Figure 2-1. Schematic of the IGZO TFTs, which employ an HfO_2 gate insulator and sometimes an HfO_2 passivation layer.

2.1.1. Photolithography

In order to fabricate a proper TFT, patterning must be done in concert with thin film deposition in order to make the desired structure. This can be done using a photolithography process. First, the wafer is coated with first P-20 primer and then SPR995-2.1 (2.1 μm thick) photoresist using a spin coater operating at 3000 rpm for 45 seconds. Then, the wafer is subjected to a pre-exposure bake on a 115 °C hot plate for 1 minute. The wafer is exposed with a Quintel Contact Aligner. Once the proper mask is chosen and loaded into the aligner, the wafer is loaded, the mask features are aligned with the features already on the wafer, and the wafer is exposed to ultraviolet (UV) light for 10-11 seconds. After a post-exposure bake (identical to previous bake), the wafers are developed in CD-26 developer for 1 minute, which causes the exposed pattern to dissolve in the developer solution, creating a positive image of the mask.

The next step depends on whether an etch process or lift-off process is being used. For the etch process, the desired film is already on the wafer and the resist patterned on top, so the next step is to etch away the unwanted areas of the film using either a wet chemical etching or reactive ion etching (RIE) process. For the lift-off process, the next step is to deposit the film that needs to take the form of the pattern. The final step for both etching and lift-off processes is to remove the remaining photoresist using sonicated acetone bath. Once the photoresist is removed, the wafer is rinsed and cleaned, dried, and is ready for the next fabrication step.

2.1.2. Gate Electrode

For IGZO TFT fabrication, the starting substrate is a p-type silicon wafer with a 500 nm layer of thermally grown SiO_2. In each case, chromium was used for the gate electrode layer, and it was deposited using a DC sputtering tool in the CNMS cleanroom. 60 W DC power and 3 mTorr working pressure were used for 16 minutes on each wafer, which deposited a Cr thickness of ~150 nm. During sputtering, 25 standard cubic centimeters per minute (sccm) argon gas was flowing into the chamber. The etching process was used to pattern the gate electrodes. This was done using a Cr etchant (Chromium Etch 1020AC) , and the etching time usually ranged from 2 – 3 minutes.

2.1.3. Gate Insulator

For these IGZO TFTs, HfO_2 was studied as a replacement gate insulator layer for SiO_2. These HfO_2 layers were deposited using an Oxford Instruments ALD tool (see section 1.2.3 for further details). Either a 25 or 50 nm HfO_2 layer was deposited, and either a 150 or 200 °C processing temperature was utilized. In addition, in some cases a H_2 plasma preclean was used, which will be further discussed later as part of the experimental data.

2.1.4. IGZO Active Layer

The active semiconducting layer used in these TFTs was IGZO deposited by radio frequency (RF) magnetron sputtering at the University of Tennessee. 80 W RF power and 5

mTorr working pressure were used consistently throughout these experiments; however, the O_2 partial pressure and sputter time were varied according to the desired IGZO oxygen content and film thickness. The O_2 partial pressures and IGZO sputter times for each experiment will be discussed in detail in the succeeding chapters. The lift-off method was employed in IGZO patterning.

2.1.5. Source/Drain Electrodes

The electron beam evaporator in the CNMS cleanroom was used to deposit the source/drain electrodes. Typically, a titanium/gold layer was deposited; the titanium layer was necessary because otherwise the gold film would not adhere well to the substrate. A 10 nm layer of Ti is first deposited, followed by a Au layer ranging from 60-90 nm in thickness. In the e-beam evaporator, Ti evaporated at currents around 0.1 A, and Au evaporated around 0.25 A. The lift-off method was used in source/drain patterning.

2.1.6. Passivation

In certain experiments, a passivation layer was employed. The objective of passivation is to make a device more stable and less reactive with the environment. The passivation layer was a second layer of ALD HfO_2, which is deposited in the same manner as in the gate insulator deposition step. The passivation layer is a critical layer for one of our TFT applications, which is an active matrix thin film transistor electrowetting array.

2.1.7. Via Hole

In order to be able to do electrical testing on these TFTs, the gate, source, and drain electrodes have to be opened, as they are covered with HfO_2 films from the gate insulator and passivation steps. The photolithography process was used to pattern contact points on the electrodes, and then the HfO_2 was etched away using an Oxford Instruments RIE metal etcher. 50 seconds of etching time in BCl_3 gas was sufficient to etch 50 nm HfO_2; in other words, HfO_2 etched at a rate of ~1 nm/sec, so the etching times were changed according to the total HfO_2 thickness.

2.2. Annealing

Various annealing steps were used, typically using a box furnace but sometimes using a hot plate. The box furnace temperature was set to increase at a rate of 20 °C/min. Various annealing times and temperatures were used according to each experiment. Annealing treatments were done following fabrication most of the time, but in certain experiments a pre-passivation annealing step was investigated as discussed below.

2.3. Electrical Measurements

An Agilent B1500 semiconductor analyzer was used in electrical testing of the IGZO TFTs. The probe station connected to the analyzer was used to probe the three electrodes in order to make electrical measurements. Output and transfer characteristics of the TFTs were

measured using this method. In addition, in the experiment in the following chapter, where the properties of HfO_2 are studied, I-V and C-V measurements are taken instead. Unless otherwise stated, the channel width and length for the measured devices will be 50 μm and 20 μm, respectively.

Chapter 3

HfO_2 Film Characterization

3.1. Overview

Prior to fabricating IGZO TFTs that employ an HfO_2 gate insulator, some of the properties of the ALD-deposited HfO_2 films themselves will be studied. Doing so can shed some light on processing conditions that allow for optimal performance. While processing conditions for IGZO TFTs will be studied extensively in the succeeding chapters, it will be useful to have an idea of what kinds of trends to expect for the HfO_2 films alone.

3.2. Experimental Procedure

First, 50 nm layers HfO_2 were deposited at 150 °C on two moderately doped (10 – 20 Ω-cm) silicon wafers using the ALD tool in the process as described in Section 2.1.3. Following HfO_2 deposition, contacts were made on one of the wafers in order to conduct capacitance-voltage and current-voltage measurements. This was accomplished by first patterning metal contacts (by lift-off) using a TFT source/drain mask, following the steps of the photolithography technique as described in Section 2.1.1. 60 nm Au was deposited onto 10 nm Ti for the S/D contacts. In order to determine the optimal annealing temperature, both the patterned and unpatterned samples were annealed at 200, 300, and 400 °C.

Using the semiconductor analyzer probe station, I-V and C-V measurements were measured using the patterned sample. A 400 μm x 400 μm contact square was probed in

addition to an area of the wafer on which the HfO_2 layer had been scratched off to make contact with the bottom silicon substrate. I-V measurements were measured from -20 – 20 V, where the absolute value of the current is taken to represent the negative current. An HP 4284 LCR meter was connected to the probe station in order to take C-V measurements. The measurements were taken from -10 – 10 V at frequencies of 1, 10, 100, and 1000 kHz.

Ellipsometry measurements were conducted using a Horiba Jobin Yvon Uvisel ellipsometer on the unpatterned sample to determine how annealing temperature affects film thickness and the index of refraction. A 70.2 ° angle of incidence and ~ 632 nm wavelength were used for measurements.

3.3. Results and Discussion

3.3.1. I-V Characterization

The I-V measurements are shown in Figure 3-1. For each of the annealing temperatures below 400 °C, the I-V measurements showed relatively low maximum leakage currents of about 10^{-10} A. The sample annealed at 400 °C showed a substantially larger leakage current of about 2 x 10^{-8} A. The discrepancy between the 400 °C annealed sample and the rest of the samples makes sense because, according to the literature, the crystallization temperature for HfO_2 is around 400 °C [8]. The micro or nanocrystallization in the HfO_2 film is causing a decline in HfO_2 performance, likely via conduction in the grain boundaries, and this fact will be important later when incorporating HfO_2 as a gate insulator for IGZO TFTs.

At low voltages (~5 V), the leakage current does show some improvement. For example, the leakage current reduces by almost an order of magnitude from the as-deposited to the 300 °C

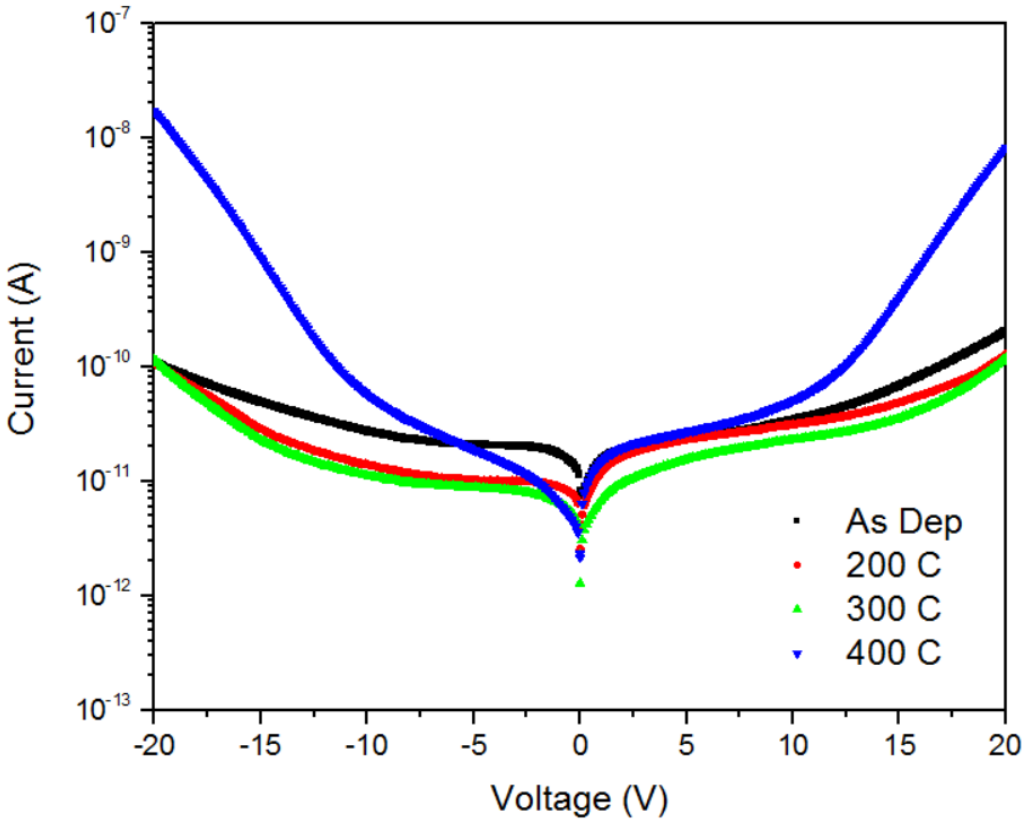

Figure 3-1. I-V curves for the as-deposited and annealed samples in the -20 – 20 V range.

annealed sample. However, at higher voltages (~20 V), there is little variation in leakage current with annealing temperature, again excluding the 400 °C annealed sample. Obviously, a lower voltage yields a lower leakage current. Figure 3-2 below illustrates this fact, along with comparison of the leakage currents for each sample at different voltages.

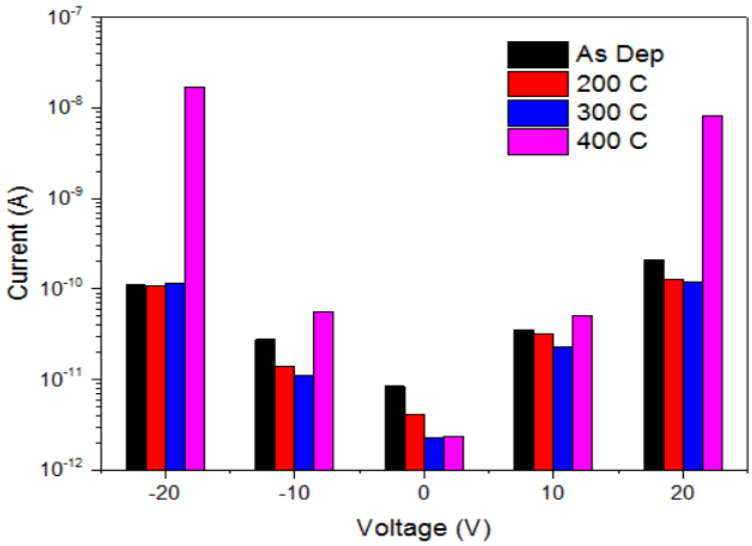

Figure 3-2. Leakage current vs. annealing temperature at -20 to 20 V.

3.3.2. C-V Characterization

While there was some semblance of a relationship between annealing temperature and I-V characteristics, the same cannot be said for the C-V characteristics. Excluding the 400 °C annealed sample, very little change was observed between the capacitance and annealing temperature at all voltages. The C-V curves at the varying frequencies are shown in Figure 3-3. Except for the as- deposited sample, the capacitance steadily increase with frequency until steeply decreasing at 1000 kHz. The reason for this will be explored when calculating the

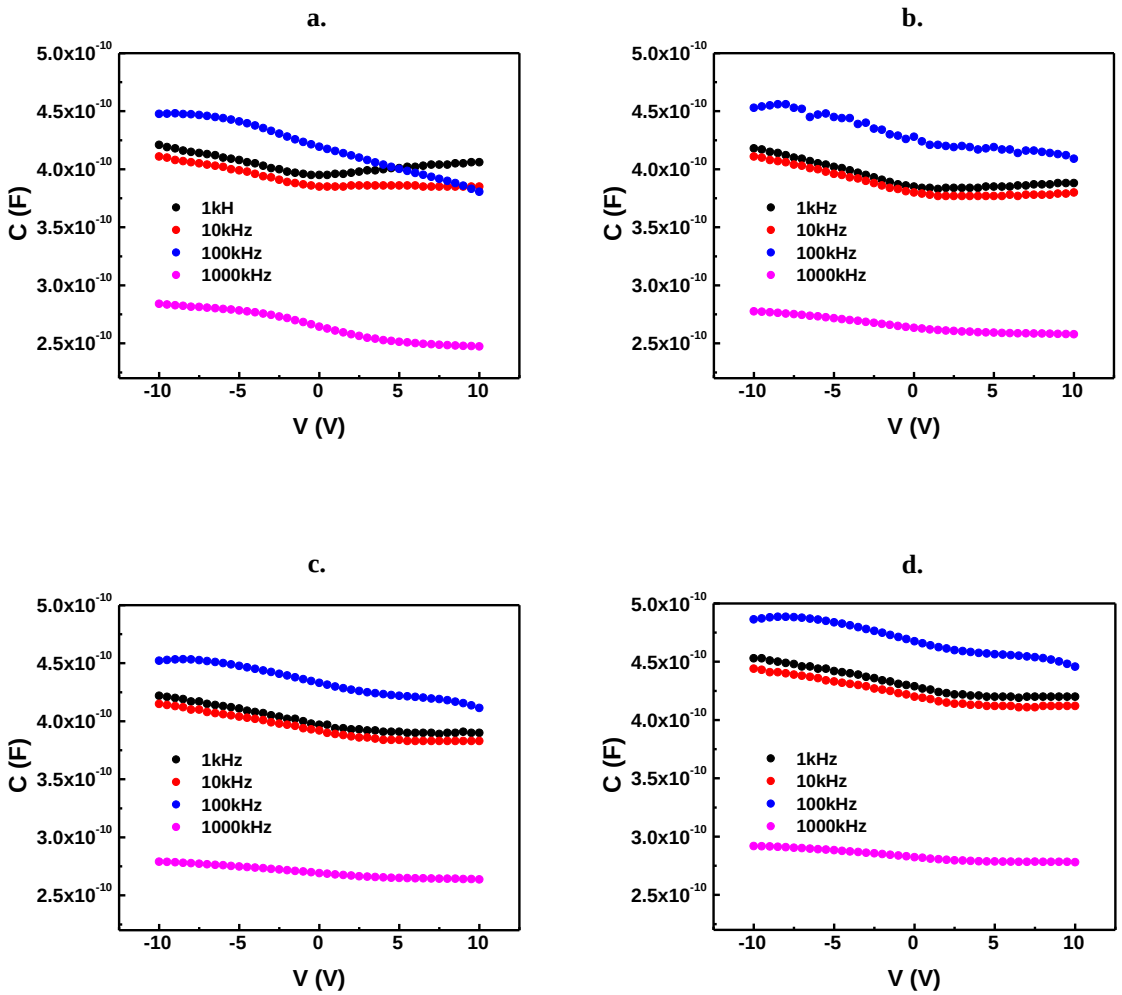

Figure 3-3. C-V curves for (a) as-deposited, (b) 200 °C anneal, (c) 300 °C anneal, and (d) 400 °C anneal.

experimental values of the dielectric constant. Figure 3-4 shows a comparison of the capacitances at varying voltages at 100 and 1000 kHz.

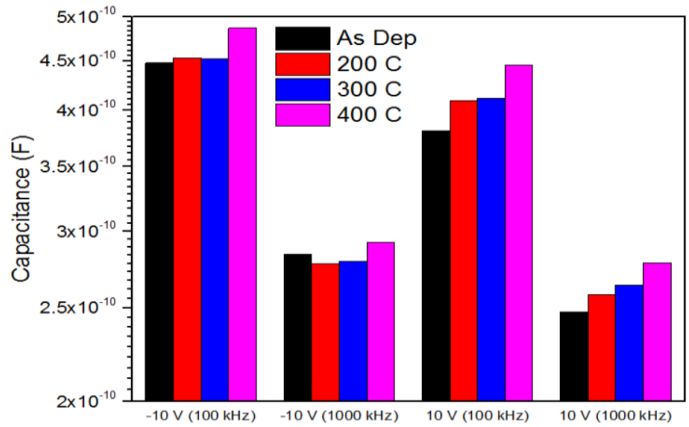

Figure 3-4. Capacitance vs. annealing temperature at 100 kHz and 1000 kHz (-10 and 10 V).

The capacitance measurements can be used to calculate the dielectric constant of HfO_2 at varying frequencies and annealing temperatures. The following expression is used for these calculations.

$$C = \frac{k\epsilon_0 A}{d} \qquad \text{Eq. 3.1}$$

C is capacitance in F, k is the dielectric constant, ε_0 is the vacuum permittivity (8.854 x 10^{-14} F/cm), A is the area of the capacitor in cm^2, and d is the thickness of the film in cm. The thickness of the HfO_2 film is 50 nm (50 x 10^{-9} cm), and the area of the capacitor is 0.0016 cm^2. Therefore, using the maximum measured capacitance from each curve (Fig. 3-3), the dielectric constant can be calculated as a function of frequency and annealing temperatures, as shown in Table 3-1. Excluding the 1000 kHz κ values, the dielectric constants range from around 14.5 to 17, which are reasonable when compared to the literature value of 18 for ALD-grown HfO_2. The drastic decrease in κ for 1000 kHz stems from a change in the modes of polarization present in

Table 3-1. Calculated κ values at varying frequencies and annealing temperatures.

	1 kHz	10 kHz	100 kHz	1000 kHz
As-Deposited	15	14.54	15.88	9.88
200 °C Anneal	15	14.54	15.88	9.7
300 °C Anneal	15	14.54	15.88	9.7
400 °C Anneal	15.88	15.7	16.94	10.05

the material. There are three main modes of polarization, including electronic, ionic, and orientational mechanisms. As the frequency increases, the movement of the charge lags behind the alternating electric field, so one of the polarization mechanisms no longer contributes to the material's net polarization. In this case, upon reaching 1000 kHz, the orientational polarization mechanism drops off, which causes a decrease in the overall polarization and therefore the dielectric constant [15].

3.3.3. Ellipsometry

The measured film thicknesses were fairly close to the expected thickness of 50 nm. Excluding the 300 °C annealed sample, the thickness decreases very slightly with increasing annealing temperature. There is also a slight increase in the index of refraction with an increase in annealing temperature. These results are shown in Table 3-2. The decrease in film thickness from 300 to 400 °C is consistent with the crystallization temperature, as there is also densification of the film.

Table 3-2. Ellipsometry data including HfO_2 film thickness, index of refraction, and chi square (to show goodness of fit to model).

	Thickness (nm)	n	X^2
As- Deposited	51.5	1.919	0.3445
200 °C Anneal	51.1	1.925	0.38
300 °C Anneal	51.2	1.928	0.6011
400 °C Anneal	49.6	1.928	0.576

Chapter 4

IGZO TFT Performance: HfO_2 G.I. Compared to Previous SiO_2 G.I. Data

4.1. Overview

As stated in the introduction, the dielectric constant for HfO_2 is higher relative to that of SiO_2. This higher dielectric constant will yield superior properties, including the ability for the device to operate at a much lower voltage. Previously, IGZO TFTs were studied using an SiO_2 gate insulator. The characteristics for these TFTs will be used as a basis for comparison for ones with an HfO_2 G.I. Table 4-1 below lists the specific steps used in making this set of IGZO TFTs using HfO_2. The previously made TFTs with SiO_2 employ a nearly identical process, with the difference being that the G.I. is 100 nm SiO_2 deposited using plasma-enhanced chemical vapor deposition (PECVD) for 1 minute, 37 seconds at 350 °C; because the G.I. is different, the via hole process is different: SiO_2 is etched using a recipe that utilizes SF_6 gas, in which 100 nm SiO_2 is etched in 1 minute. Assume the SiO_2 sample characteristics were measured as-fabricated (no annealing treatments).

4.2. Results and Discussion

As expressed before, the point of using an HfO_2 gate insulator in lieu of SiO_2 is to lower the operation voltage of the devices. In addition, it will allow for a higher capacitance and lower leakage current. Starting with the previous SiO_2 results, the output and transfer characteristics show good TFT properties in that they show relatively low OFF currents, high ON currents, and

Table 4-1. Steps of the fabrication process for the IGZO TFTs employing an HfO_2 G.I.

Sample	1	2
Substrate	Si	
Buffer	500 nm thermal SiO2	
Gate	150 nm Cr - 60 W, 16 min.	150 nm Cr - 60 W, 16 min.
Gate Patterning	Etching	Etching
G.I.	OPT HfO2 at 150 °C - 50 nm	OPT HfO2 at 150 °C - 25 nm
Active	50 nm IGZO - 80 W, pO2 10%, 36 min.	50 nm IGZO - 80 W, pO2 10%, 36 min.
Active Patterning	Lift-off	Lift-off
S/D	10/60 nm Ti/Au	10/60 nm Ti/Au
S/D Patterning	Lift-off	Lift-off
Via Hole	OPT-HfO2 Etch - 50 sec.	OPT-HfO2 Etch - 50 sec.
Anneal	150, 200, 250, 300 °C for 1 hr.	150, 200, 250, 300 °C for 1 hr.

thus a high ON/OFF current ratio. The output and transfer characteristics for an IGZO TFT utilizing an SiO_2 G.I. are shown in Figure 4-1.

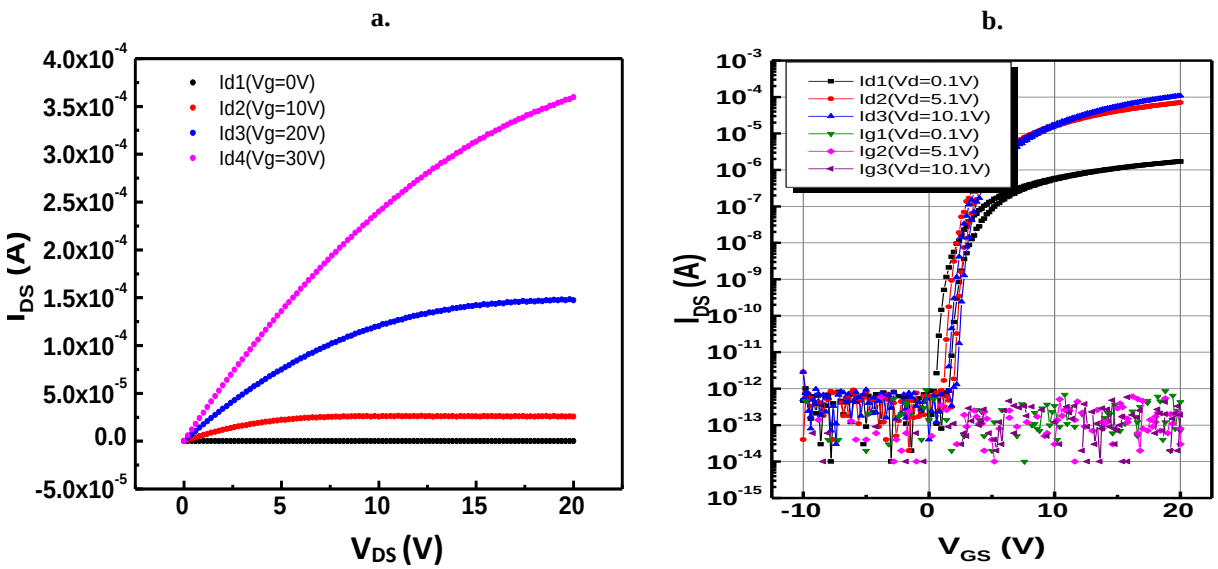

Figure 4-1. (a) Output and (b) Transfer characteristics of previous IGZO TFTs with SiO_2 G.I.

These TFTs show an OFF current of ~ 10^{-12} A, an ON current of ~10^{-4} (at V_{DS} = 10.1 V and V_{GS} = 20 V), and thus an ON/OFF current ratio of ~10^8. The ON current occurs at a gate voltage of 20 V. When considering IGZO TFTs employing an HfO_2 G.I., we expect this voltage to be much lower, and we also expect that the annealing treatment will be the deciding factor in the functionality of these TFTs. Some HfO_2 results are shown in Figure 4-2, in which major differences can be seen when changing the post-fabrication annealing step. While the characteristics improve with increasing annealing temperature, a 200 °C anneal is not sufficient for the superior HfO_2 properties to be realized. However, the low operation voltage becomes effective after annealing at temperatures beyond 200 °C. Such results for both the 25 nm and 50

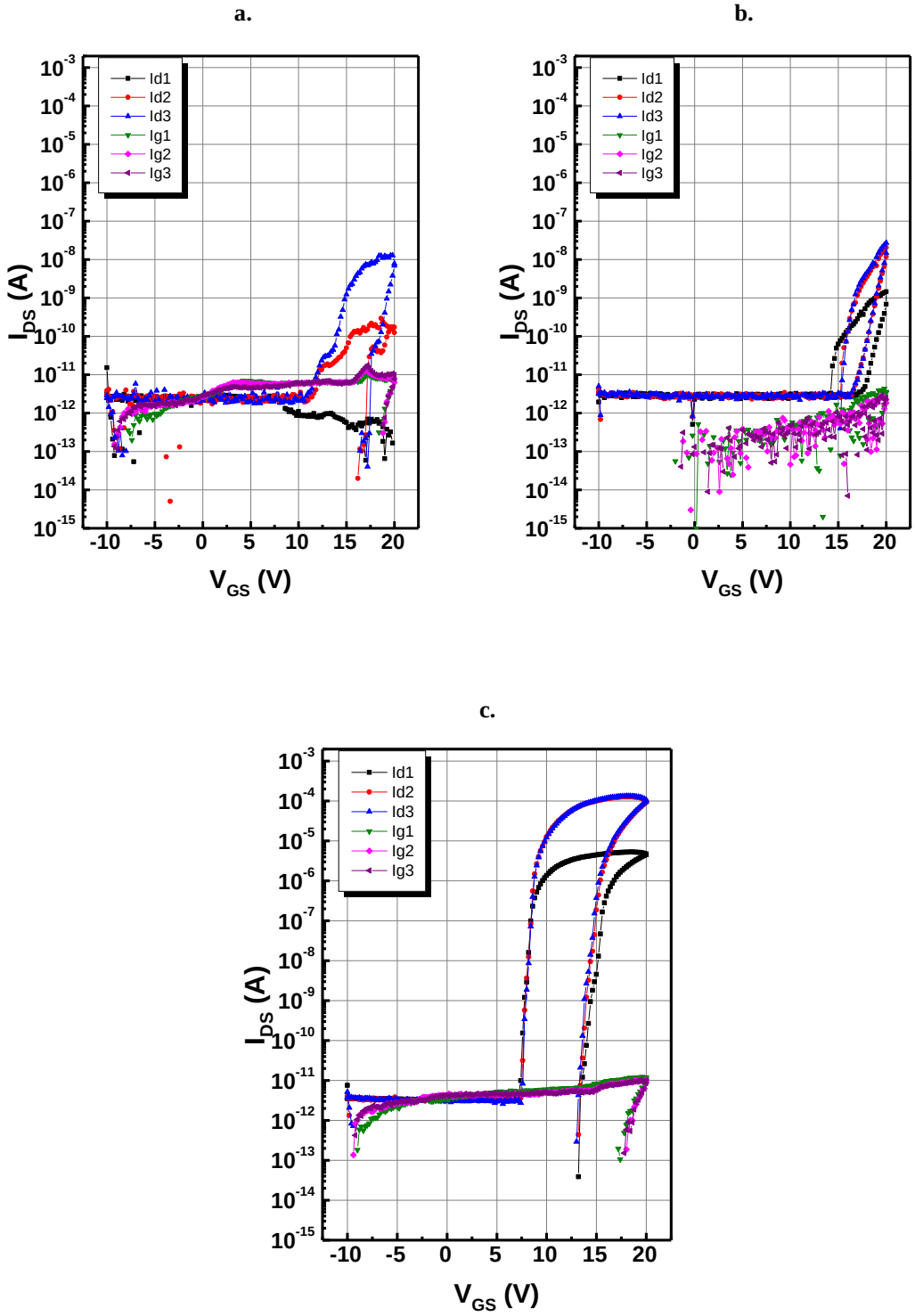

Figure 4-2. Transfer characteristics for (a) as deposited, (b) 150 °C anneal, and (c) 200 °C anneal for the sample with a 50 nm HfO_2 gate insulator.

nm HfO_2 gate insulator samples can be found in Figure 4-3.

While the low voltage operation does become evident after annealing at 250 °C, considerable hysteresis can be seen, which is not desirable in TFT transfer characteristics. The hysteresis is less prevalent in the 25 nm sample relative to the 50 nm sample. However, when a 300 °C annealing temperature is reached, most of the hysteresis is eliminated. For both samples at 300 °C, the OFF current is ~10^{-12} A, the ON current is 10^{-4} A, and thus the ON/OFF current ratio is 10^8, which is the same as the previous SiO_2 gate insulator data. The difference is the much lower operation voltage for HfO_2. The electron mobility, threshold voltage, and subthreshold swing are superior for HfO_2 as well. For HfO_2, μ_n = 19.1 cm^2/V-s, V_{TH} = 1.7 V, and S.S. = 0.07 V/dec. For SiO_2, μ_n = 9.80 cm^2/V-s, V_{TH} = 3.5 V, and S.S. = 0.24 V/dec Figure 4-1 (b) and Figure 4-3 (c) can be used together to compare the performance of SiO_2 and HfO_2 gate insulators. In conclusion, since an HfO_2 gate insulator, with optimal processing conditions, can produce similar properties at a lower voltage than SiO_2, it should also allow electrowetting to be driven at a lower voltage in a full electrowetting array.

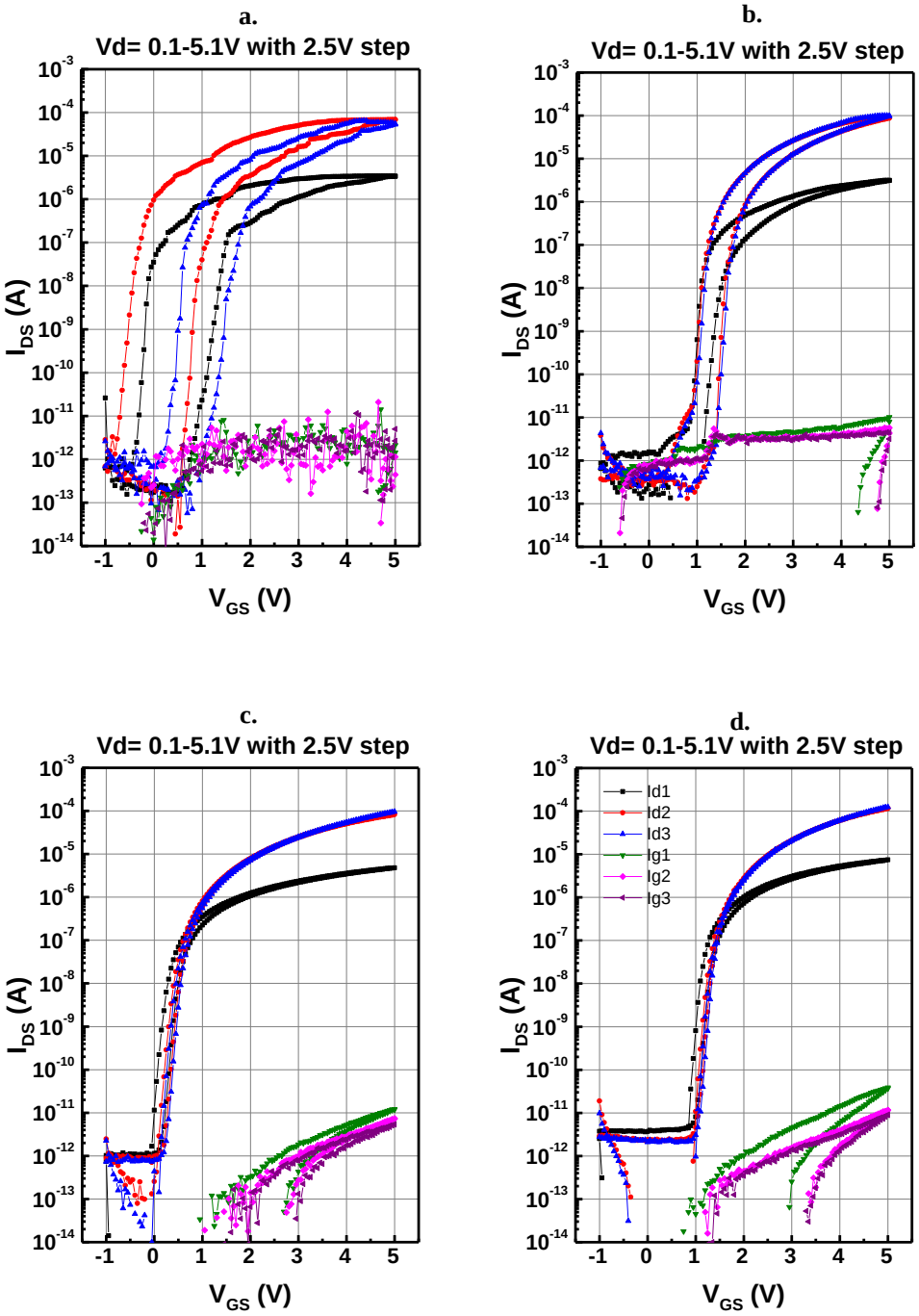

Figure 4-3. Transfer curves for the 50 nm and 25 nm HfO_2 samples annealed at 250 °C ((a) and (b), respectively) and for the 50 nm and 25 nm HfO_2 samples annealed at 300 °C ((c) and (d), respectively).

Chapter 5

HfO_2 Passivation: Annealing Treatments Test

5.1. Overview

As expressed above, passivation has become an area of interest, considering the effects the environment can have on electronic devices. Contaminants are floating around everywhere, and they can compromise the devices. In addition, the surfaces can become subject to oxidation, which will also ruin the devices. In this study, HfO_2 is studied as a passivation layer as part of the process in Chapter 2. A number of annealing treatments are studied to see which produces the best TFT properties. The specifics for this run are shown in Table 5-1 below. The difference between the two samples is that one employs a pre-passivation anneal, whereas the other sample does not. Additional annealing treatments will be used in addition to those in Table 5-1 to attempt to reach good TFT characteristics. According to the literature, IGZO electrical properties are controlled by oxygen vacancies, which are added and removed throughout fabrication (after IGZO deposition) [7]. The concept of adding annealing treatments is valid in this regard because, depending on the time and temperature, annealing can either introduce new oxygen vacancies in IGZO or take them away. This will ultimately determine how good the TFT properties are.

Table 5-1. Specific fabrication steps for HfO_2 PVX.

Sample	1	2
Substrate	Si	
Buffer	500 nm thermal SiO2	
Gate	150 nm Cr - 60 W, 16 min.	150 nm Cr - 60 W, 16 min.
Gate Patterning	Etching	Etching
G.I.	OPT HfO2 at 200 °C - 50 nm	OPT HfO2 at 200 °C - 50 nm
Active	22 nm IGZO - 80 W, pO2 30%, 27 min.	22 nm IGZO - 80 W, pO2 30%, 27 min.
Active Patterning	Lift-off	Lift-off
S/D	10/60 nm Ti/Au	10/60 nm Ti/Au
S/D Patterning	Lift-off	Lift-off
Via Hole (Gate)	OPT-HfO2 Etch - 50 sec.	OPT-HfO2 Etch - 50 sec.
Pre-PVX Anneal	N/A	250 °C for 1 hr.
PVX	OPT HfO2 at 200 °C - 50 nm	OPT HfO2 at 200 °C - 50 nm
Via Hole (All Electrodes)	OPT-HfO2 Etch - 50 sec.	OPT-HfO2 Etch - 50 sec.
Post-PVX Anneal	150, 200, 250, 300 °C for 1 hr.	150, 200, 250, 300 °C for 1 hr.

5.2. Results and Discussion

In each case, the measurements are taken at a drain current of 10.1 V (corresponding to I_D3). Starting with sample 1 without a pre-PVX anneal, the TFT transfer characteristics are not good following PVX deposition. The ON current and subthreshold swing are both very low, and there are many humps in the curves, which could be due to the fact that the IGZO, in that state, is acting too much like an insulator (not enough oxygen vacancies) . The first four annealing treatments do not enhance TFT properties. 150 and 200 °C anneals yield similar TFT characteristics (with a very slight increase in ON current with 200 °C). Annealing at 250 and 300 °C produces metallic behavior (too many oxygen vacancies), meaning the drain current stays high and changes very little with increasing gate voltage. This data is shown in Figure 5-1.

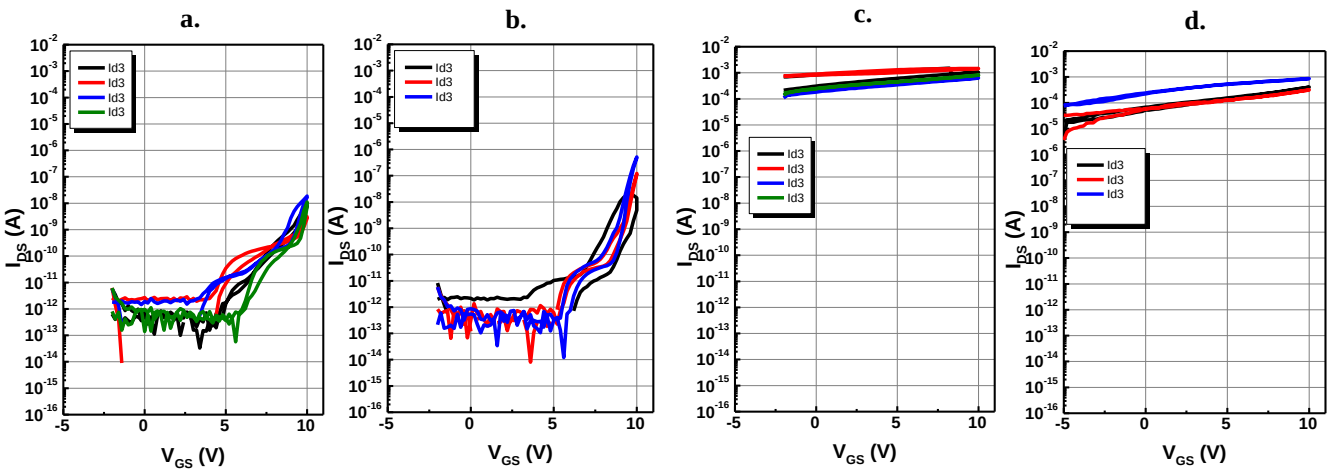

Figure 5-1. Sample 1 transfer characteristics for (a) before post-PVX annealing (after PVX), (b) 200, (c) 250, and (d) 300 °C 1 hour post-PVX anneal.

Additional annealing treatments at 200 °C were added in an attempt to produce good TFT properties. Characteristics of these treatments are shown in Figure 5-2. Annealing for an extra 2 hours at 200 °C for the sample previously annealed at 200 °C for 1 hour produced decent TFT

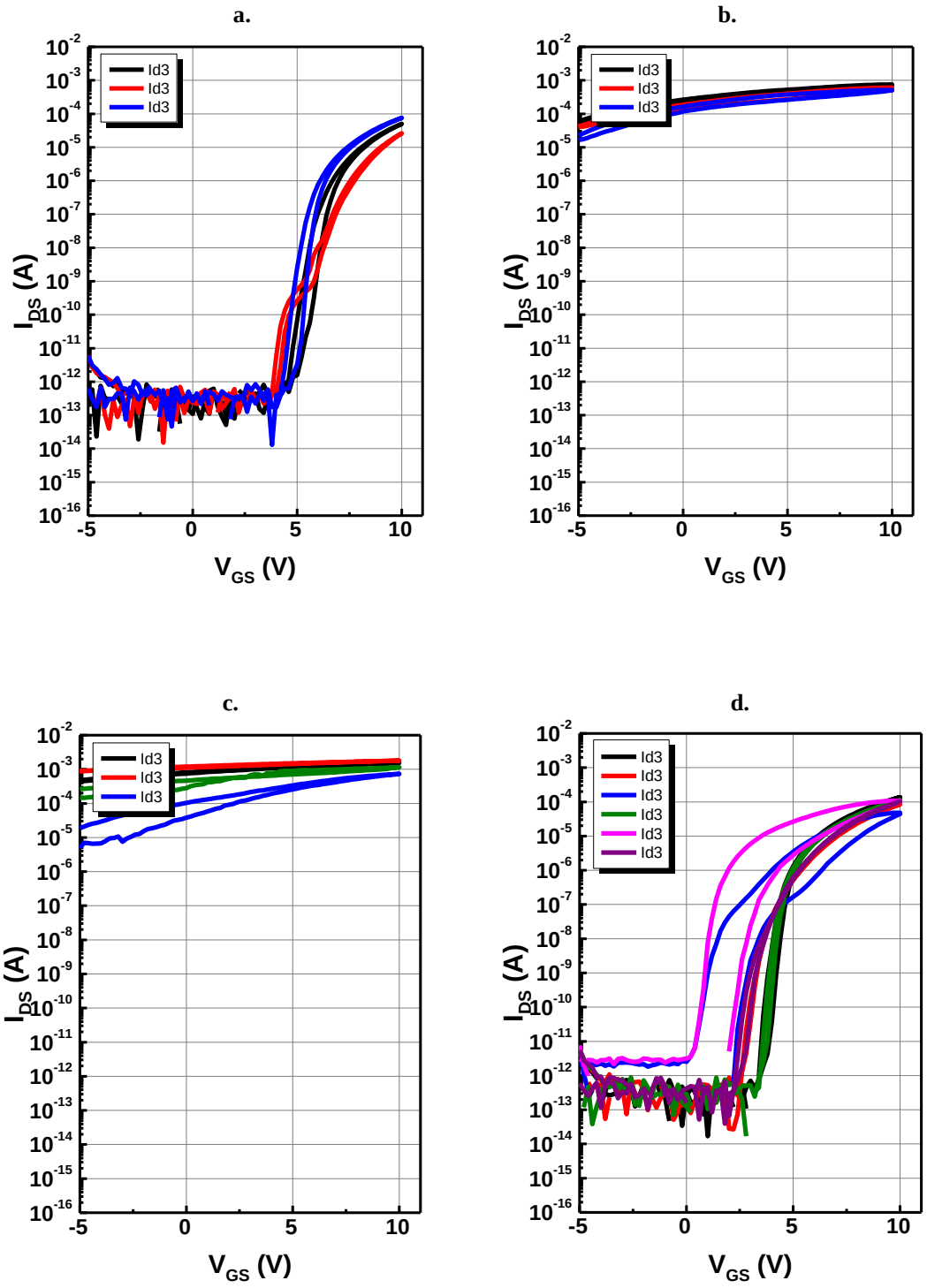

Figure 5-2. Sample 1 transfer characteristics for (a) 200 °C 1 hr. + 200 °C 2 hr. anneal, (b) 250 °C 1 hr. + 200 °C 2 hr. anneal, (c) 300 °C 1 hr. + 200 °C 2 hr. anneal, and (d) 200 °C 1 hr. + 200 °C 4 hr. anneal.

properties, with few humps in the graphs, little hysteresis, and an ON current of ~10^{-4} A at V_G = 10 V and V_D = 10.1 V. However, an extra 2 hours at 200 °C for the 250 and 300 °C samples still produces metallic characteristics. Another 2 hours at 200 °C for the sample with 200 °C post-PVX anneal (for a total of 5 hours at 200 °C) produces significant hysteresis and a lack of uniformity among measurements.

Considering sample 2 (with a pre-PVX annealing step), a major difference can be seen between the transfer characteristics for measurements before and after pre-PVX annealing. Before pre-PVX annealing, the TFTs are not yet turned on, as the ON current is only 10^{-10} A. However, annealing at 250 °C before adding the passivation layer allows the TFTs to reach an ON current of 10^{-5} A (at V_{GS} = 10 V and V_{DS} = 10.1 V), although there is a significant leakage current. After depositing the passivation layer, the TFTs do show significantly less leakage current and a good ON/OFF current ratio (10^8), but the drain current does not increase steeply as it should (high subthreshold swing), and hysteresis becomes a factor. Post-PVX annealing treatments should help eliminate this hysteresis. Figure 5-3 shows a comparison of each of the transfer characteristics for the above described measurements of sample 2.

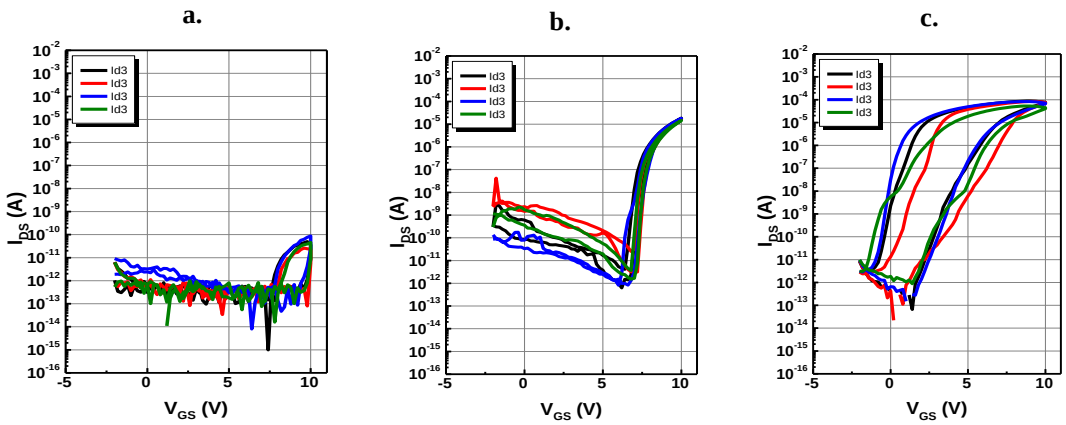

Figure 5-3. Sample 2 transfer characteristics for (a) before pre-PVX annealing, (b) after pre-PVX annealing at 250 °C, and (c) before post-PVX annealing (after PVX).

The same first four post-passivation annealing treatments were applied to sample 2 as in sample 1. A comparison for the first four post-PVX annealing treatments for sample 2 can be seen in Figure 5-4. 150 and 200 °C annealing produces TFT transfer curves with a decent subthreshold swing, but there are humps in some of the curves, possibly due to impurities in the IGZO. The 250 °C annealing treatment produces significant hysteresis, along with a larger variation in threshold voltage in each curve. The 300 °C anneal causes a leftward shift of the curves, and they no longer show good TFT characteristics.

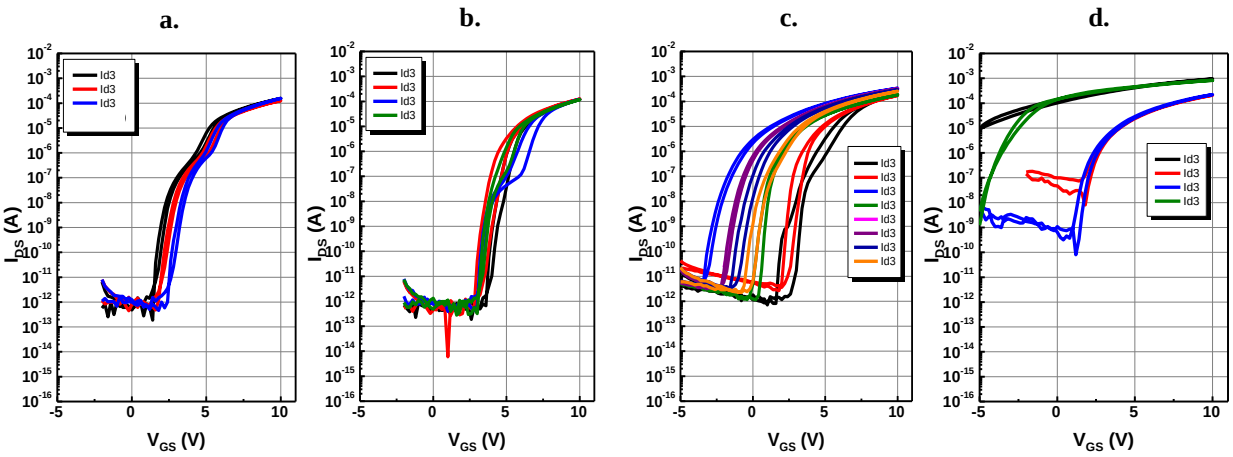

Figure 5-4. Sample 2 transfer characteristics for (a) 150, (b) 200, (c) 250, and (d) 300 °C 1 hour post- PVX anneal.

Similarly to sample 1, additional 200 °C anneals were applied to sample 2, and these produced good TFT transfer characteristics. Based on all of data in this chapter, there are two annealing treatments that produce the best TFT characteristics. One is to apply the pre-PVX anneal at 250 °C for 1 hour, post-PVX anneal at 250 °C for 1 hour, and add an additional 200 °C anneal for 4 hours. The other is to keep the pre-PVX anneal, post-PVX anneal at 300 °C for 1 hour, and add an additional 200 °C anneal for 2 hours. These two treatments yield an ON/OFF current ratio of ~10^7 and a threshold voltage of ~2.5 V. The former case will be used as part of

the HfO_2 PVX wafer level uniformity test in Chapter 7. The data for the additional 200 °C anneals is shown in Figure 5-5 below, where the best TFT characteristics are in (c) and (e). From this study, one can conclude that, first of all, employing a pre-PVX annealing step produces much better results. In addition, there seems to be a critical temperature (above 200 °C) at which annealing adds too many oxygen vacancies, causing the IGZO to be overly conductive. However, further annealing at a lower temperature, 200 °C in this case, allows oxygen to be reintroduced into the IGZO, which causes the TFTs to regain their semiconducting properties.

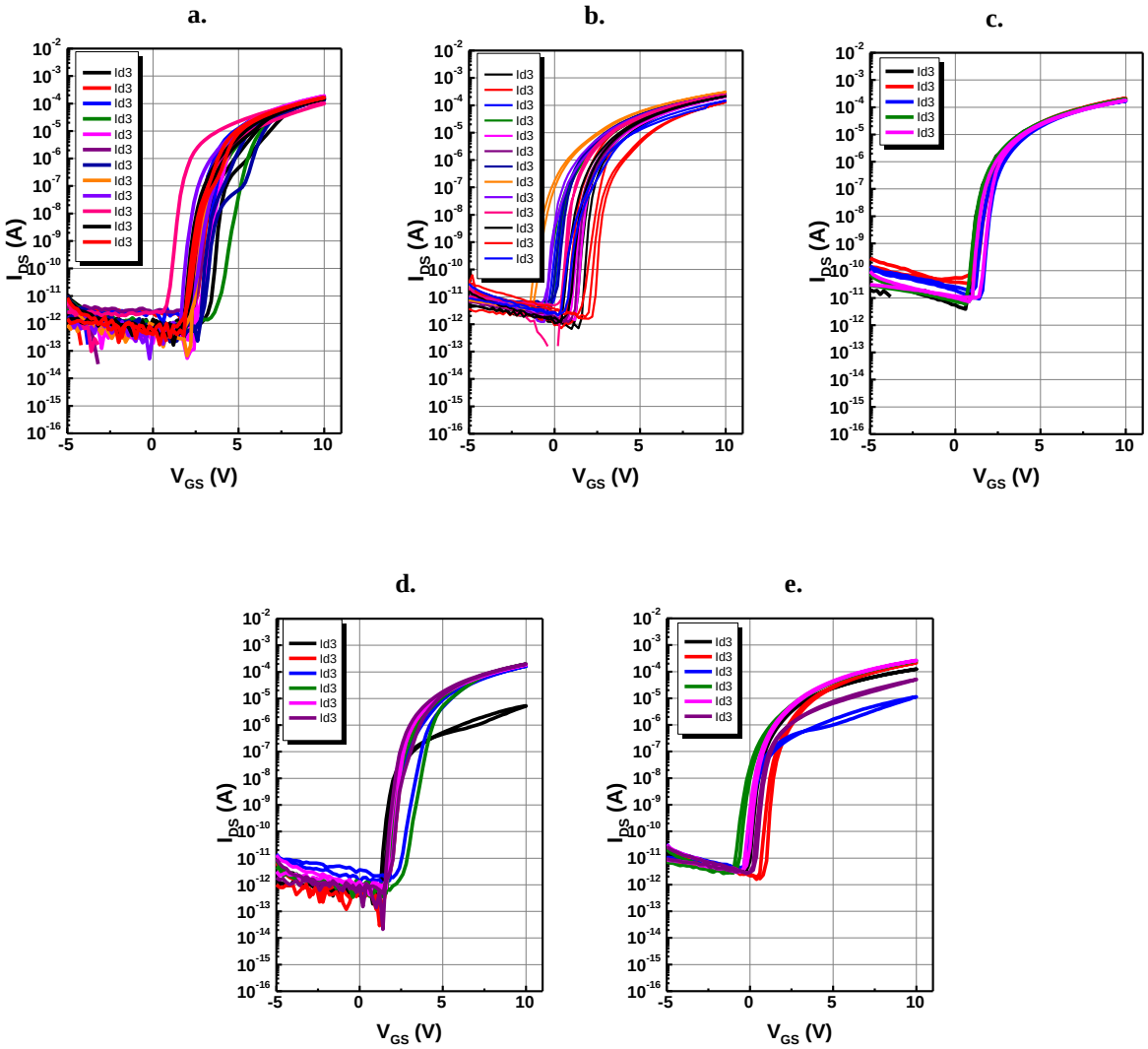

Figure 5-5. Sample 2 transfer characteristics for (a) 200 °C 1 hr. + 200 °C 2 hr. anneal, (b) 250 °C 1 hr. + 200 °C 2 hr. anneal, (c) 300 °C 1 hr. + 200 °C 2 hr. anneal, (d) 200 °C 1 hr. + 200 °C 4 hr. anneal, and (e) 250 °C 1 hr. + 200 °C 4 hr. anneal.

Chapter 6

HfO_2 Passivation – Wafer Level Uniformity Test

6.1. Overview

Uniformity is very important when considering electronic devices. TFTs should show similar characteristics, regardless of where they are measured on the wafer; however, this is not always the case. Problems with deposition steps can lead to a film thickness gradient, which could potentially change the properties. Since an electrowetting device uses a large section of the wafer, uniformity is vital. Non-uniformity will cause an electrowetting device to not function properly. For this reason, before an electrowetting device is fabricated, one must make sure that the specific fabrication steps yield uniformity. In this case, TFT uniformity will be tested across a unit TFT array on a wafer with an HfO_2 passivation layer.

6.2. Experimental

The degree of uniformity for a unit TFT array can be determined by measuring the transfer characteristics at many positions across the wafer. Figure 6-1 shows a layout of the unit TFTs and shows the positions where the properties were measured. These properties were measured a second time five days later to validate passivation success. As part of this experiment, measurements were made for TFT patterns with varying channel widths and lengths. The W/L matrix is shown in Figure 6-2. As expressed in Chapter 2, most TFT characteristics have been measured using TFTs with a channel width of 50 μm and length of 20 μm. This W/L

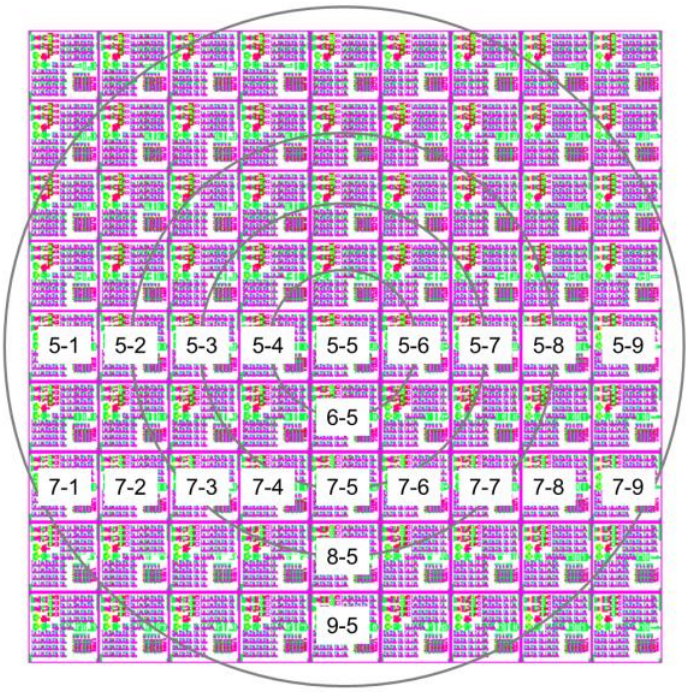

Figure 6-1. Layout of the unit TFT array. The die numbers shown are the ones that will be measured.

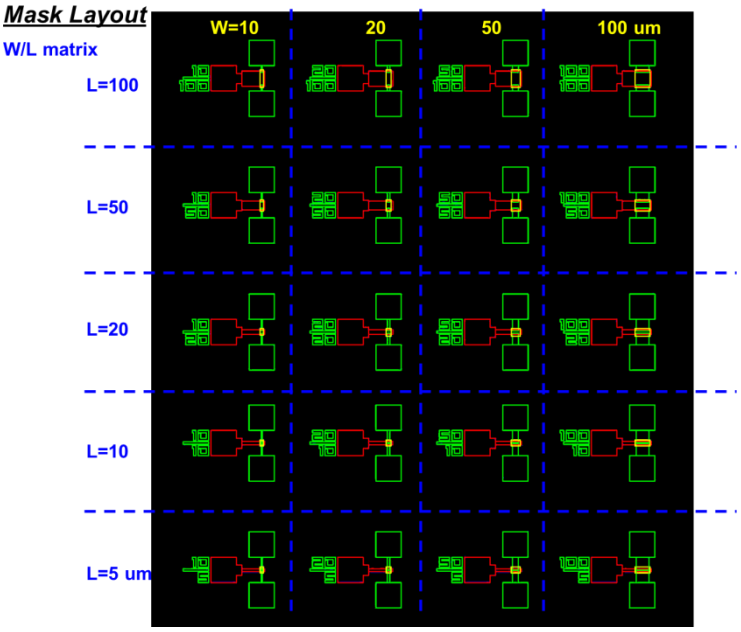

Figure 6-2. TFT layout of the W/L matrix.

Matrix will shed some light on how TFT properties change with channel width and length.

The specific fabrication process for this test is shown in Table 6-1 below. Note that the annealing process used was the optimal one described in Chapter 6. Also, IGZO film thickness is greatly increased due to a mistake in fabrication.

6.3. Results and Discussion

Figure 6-3 shows the general uniformity of the wafer. The characteristics stay fairly constant when moving through row 5 (die 5-1 to 5-9) as both the ON current and OFF current do not change much. The same applies for row 7 (7-1 to 7-9). The curves in column 5 (5-5 to 9-5) do look a bit different at V_G less than 2 V, but the overall TFT characteristics stay about the same. Note that when comparing this run to the results in the annealing treatment test in Chapter 6, the threshold voltage has increased slightly to around 4 – 6 V depending on the die, which comes as a result of the increased IGZO layer.

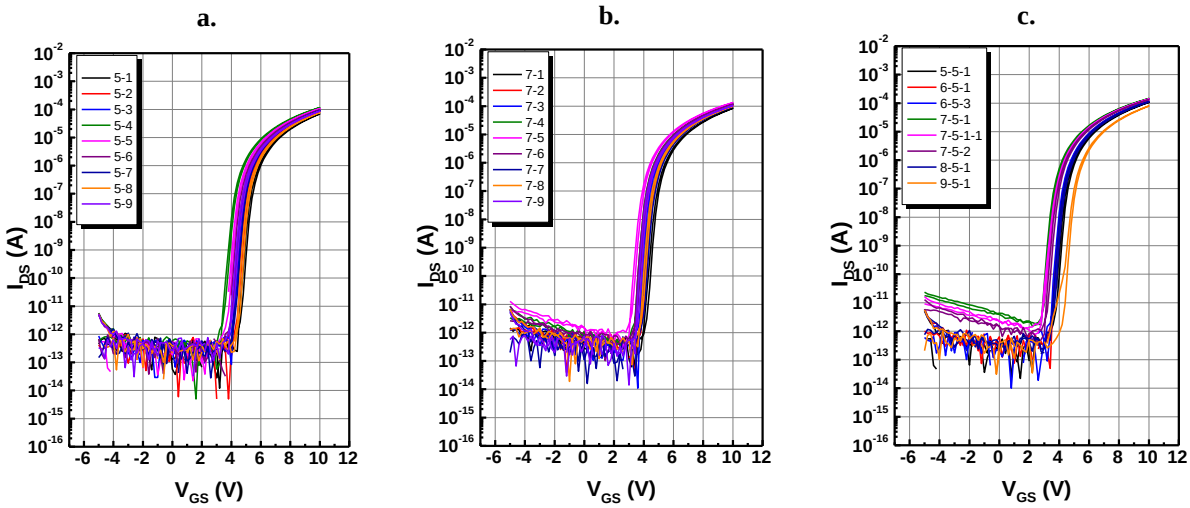

Figure 6-3. Transfer characteristics for (a) row 5, (b) row 7, and (c) column 5.

Table 6-1. Specific fabrication steps for the HfO_2 PVX wafer level uniformity test.

Substrate	Si
Buffer	500 nm thermal SiO2
Gate	150 nm Cr - 60 W, 16 min.
Gate Patterning	Etching
G.I.	OPT HfO2 at 200 °C - 50 nm
Active	86 nm IGZO - 80 W, pO2 30%, 104 min.
Active Patterning	Lift-off
S/D	10/90 nm Ti/Au
S/D Patterning	Lift-off
Via Hole (Gate)	OPT-HfO2 Etch - 50 sec.
Pre-PVX Anneal	250 °C for 1 hr.
PVX	OPT HfO2 at 200 °C - 50 nm
Via Hole (All Electrodes)	OPT-HfO2 Etch - 50 sec.
Post-PVX Anneal	250 °C for 1 hr. + 200 °C for 4 hr.

The TFTs did not degrade after 5 days and 50 days, and the characteristics remained nearly the same. The characteristics before and after waiting 5 and 50 days are shown in Figure 6-4. The

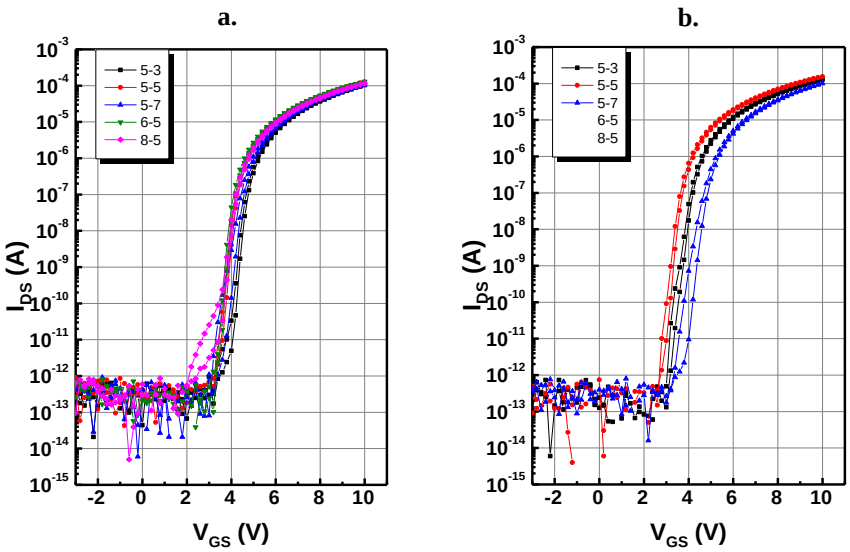

Figure 6-4. Transfer characteristics before and after waiting (a) 5 days and (b) 50 days.

similarities of the before/after 5 days and 50 days curves further validate the success of HfO_2 passivation. The threshold voltages and ON currents are virtually the equal for all cases.

Finally, the W/L study showed a clear trend in regards to threshold voltage. These results are shown in Figure 6-5. Holding width constant, threshold voltage increases with increasing channel length. On the other hand, holding length constant, threshold voltage decreases with increasing channel width.

Considering all of the data, the uniformity should be good enough to produce a full electrowetting array with these processing conditions. HfO_2 has proven to work well as a passivation layer using this particular annealing treatment in conjunction with this fabrication process, but HfO_2 passivation will be studied even more on electrowetting devices outside of this research to determine if there are even better processing conditions to drive electrowetting.

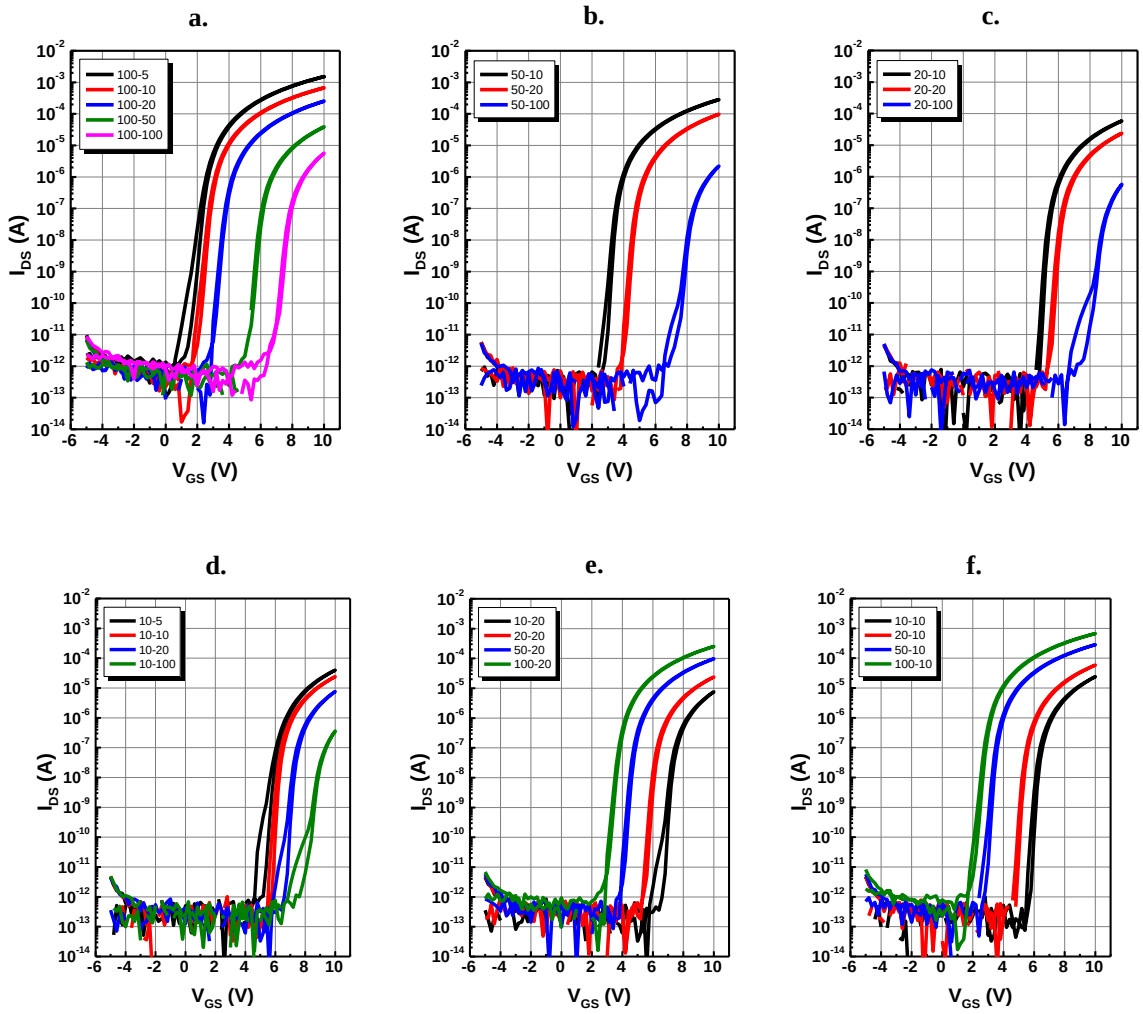

Figure 6-5. Transfer characteristics of constant channel width (a) W = 100 µm, (b) W = 50 µm, (c) W = 20 µm, (d) W = 10 µm and constant length (e) L = 20 µm and (f) L = 10 µm.

Chapter 7

Conclusions

A study of high-κ HfO_2 films at varying annealing temperatures led to the conclusion that since HfO_2 crystallizes between 300 and 400 °C and results in higher leakage currents, 300 °C is the highest annealing/processing temperature that the devices should experience. In addition, analysis of C-V measurements lead to an experimental κ value of 14 – 17, which is reasonable when considering the literature value of 18 for previously measured ALD-grown HfO2. Using an HfO_2 gate insulator in lieu of commonly used SiO_2, it was determined that IGZO TFTs using HfO_2 had properties superior to SiO_2. For instance, HfO_2 allows the TFT to reach an ON current of 10^{-4} A at V_G = 5 V, as opposed to 20 V for SiO_2 (V_D = 5.1 V in both cases). Finally, when HfO_2 was applied as a passivation layer and annealing treatments were studied, it was determined that using a pre-PVX anneal clearly produces better TFT characteristics than not using one. One of the optimal annealing treatments was to anneal before passivation at 250 °C for 1 hour, anneal after passivation at 250 °C for 1 hour, and anneal for an additional 4 hours at 200 °C. This annealing treatment was used for an HfO_2 PVX wafer level uniformity test, and the measurements on varying positions of the wafer showed excellent uniformity.

Considering the success of HfO_2 gate insulators (ability for low operation voltage) and HfO_2 passivation layers (good uniformity) leads to the ultimate conclusion that a full electrowetting array can indeed be made using these processing conditions. Experiments will continue to be done on electrowetting devices incorporating HfO_2, and hopefully this research bears fruit and contributes to the success of “lab on a chip” research.

List of References

1. "Transistor". *Encyclopædia Britannica. Encyclopædia Britannica Online.* Encyclopædia Britannica Inc., 2015.

2. Kagan, Cherie R., and Paul Andry. *Thin-film Transistors*. New York: Marcel Dekker, 2003. Print.

3. Klauk, Hagen. "Organic Thin-film Transistors." *Chemical Society Reviews* 39.7 (2010): 2643. Web.

4. Siebel, Osmar Franca, Marcio Cherem Schneider, and Carlos Galup-Montoro. "MOSFET Threshold Voltage: Definition, Extraction, and Some Applications." *Microelectronics Journal* 43.5 (2012): 329-36. Web.

5. Nomura, Kenji, Hiromichi Ohta, Akihiro Takagi, Toshio Kamiya, Masahiro Hirano, and Hideo Hosono. "Room-temperature Fabrication of Transparent Flexible Thin-film Transistors Using Amorphous Oxide Semiconductors." *Nature* 432.7016 (2004): 488-92. Web.

6. Brezeanu, G., M. Brezeanu, and F. Bernea. "High-K Dielectrics in Nanoμelectronics." Web. <http://www.romnet.net/ro/seminar16martie2010/lucrari_extenso/Modif%20Brezeanu%20lucrare%20finala%20-%202%200.pdf>.

7. Lin, Yu-Hsien, and Jay-Chi Chou. "Temperature Effects on A-IGZO Thin Film Transistors Using HfO2 Gate Dielectric Material." *Journal of Nanomaterials*. Web.

8. Huang, A. P., Z. C. Yang, and Paul K. Chu. "Hafnium-based High-k Gate Dielectrics." *Advances in Solid State Circuit Technologies* (2010). Web.

9. Lim, Wantae, Seonhoo Kim, Yu-Lin Wang, J. W. Lee, D. P. Norton, S. J. Pearton, F. Ren, and I. I. Kravchenko. "High-Performance Indium Gallium Zinc Oxide Transparent Thin-Film

Transistors Fabricated by Radio-Frequency Sputtering." *Journal of The Electrochemical Society:* 155.6 (2008). Web.

10. Johnson, Richard W., Adam Hultqvist, and Stacey F. Bent. "A Brief Review of Atomic Layer Deposition: From Fundamentals to Applications."*Materials Today* 17.5 (2014): 236-46. Web.

11. Kukli, K., M. Ritala, T. Sajavaara, J. Keinonen, and M. Leskelä. "Atomic Layer Deposition of Hafnium Dioxide Films from Hafnium Tetrakis(ethylmethylamide) and Water." *Chemical Vapor Deposition:* 8.5 (2002): 199-204. Web.

12. "HfO_2 remote plasma ALD." FlexAL^{TM}: Systems for remote plasma and thermal ALD. Oxford Instruments Plasma Technology. 2006.

13. Sangosanya, Wale. "Basic Gates and Functions." University of Surrey. Web. <http://www.ee.surrey.ac.uk/Projects/CAL/digital-logic/gatesfunc/index.html>.

14. Mugele, Frieder, and Jean-Christophe Baret. "Electrowetting: From Basics to Applications." *Journal of Physics: Condensed Matter Phys.:* 17.28 (2005). Web.

15. "Dielectric Materials." *Dissemination of IT for the Promotion of Materials Science (DoITPoMS)*. University of Cambridge. Web. <http://www.doitpoms.ac.uk/tlplib/dielectrics/printall.php>.

Vita

Aaron Bales was born on January 11, 1992 in Knoxville, TN to the parents of Lloyd and Julie Bales. He attended Shannondale Elementary School, followed by Gresham Middle School and Central High School, where he graduated in 2010 with highest honors. After graduating, Aaron attended the University of Tennessee, Knoxville to receive a Bachelor of Science degree in Materials Science and Engineering. Along the way, he was a founding member of the Alpha Zeta Chapter of the Beta Upsilon Chi fraternity and was also a member of Fountain City Presbyterian Church's chancel choir. Aaron received his Bachelor of Science in MSE in May 2014, and he graduated Magna Cum Laude. He then accepted a graduate teaching assistantship with Dr. Philip D. Rack at the University of Tennessee, Knoxville where he received his Master of Science degree in Materials Science and Engineering in December 2015.