July 29, 1976

To the Graduate Council:

I am submitting herewith a thesis written by Robert Kent Fisher entitled "A Loose Parts Monitor for Nuclear Reactors." I recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Nuclear Engineering.

Julian E. Mott, Major Professor

We have read this thesis
and recommend its acceptance:

Robert E. Bodenheimer

J. C. Robinson

E. F. Sarqua

Accepted for the Council:

Vice Chancellor
Graduate Studies and Research

A LOOSE PARTS MONITOR FOR NUCLEAR REACTORS

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Robert Kent Fisher

August 1976

1287959

ACKNOWLEDGEMENTS

The author would like to express his thanks to Dr. P. F. Pasqua who made available the funds necessary for the development of the prototype LPM described in this paper. He also expresses his appreciation to Professors J. E. Mott and J. C. Robinson who guided the direction and development of this thesis. James T. Smith deserves a special thanks for the thousands of questions that he was able to answer concerning integrated circuitry. To simply thank Nita Rye for the incredible amount of time and effort that she put into the typing and retyping of this paper hardly seems sufficient, for without her patience and great sense of humor, this thesis would still be a mass of scribbling in a briefcase.

The author must not forget to mention his wife, Patricia. After all, she is the one that had to live with him through this whole project and that must not have been very easy at times.

ABSTRACT

The paper describes the design of a four channel analog/digital system that monitors accoustic emissions received in the form of electronic transients from accelerometers in a nuclear reactor for the purpose of determining their origin and magnitude. Measured are the delay times between the transients produced by the transducers as well as the time that each signal exceeded a floating reference voltage that follows the background noise level. Data is produced in the form of two 8-bit binary words in each channel that can either be interfaced with a PDP-11 minicomputer, including interrupt and reset commands, or decoded and obtained directly via eight 3-digit, 7-segment LED read-outs. The paper also details the calibration and testing procedures, physical construction requirements, and cost considerations.

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CHAPTER I

THE NEED FOR BETTER LOOSE PARTS MONITORING

In the spring of 1974, the Nuclear Engineering Department at The University of Tennessee was asked to perform a neutron noise analysis of the core barrel motion at a major nuclear power generating station. The reactor had been scrammed and there was concern that excessive core barrel motion was responsible for banging sounds observed at several accelerometer locations as the power level, and flow rates, were increased during their attempts to bring the reactor back to its normal operating level. Professors James Robinson and Julian Mott, who developed the noise analysis system at UT, James Smith who kept the computer and all associated electronics working properly, and the author, a first-year graduate student in search of a thesis, packed up the necessary equipment and left for the plant site. The series of events which followed resulted in the development of the system described in this paper.

The impetus for this project began when it became clear that the plant's loose parts monitoring system was far from adequate. It consisted simply of several accelerometers located at various points around the primary reactor loop which were tied to a switch that fed a speaker in the control room. By switching channels, one could listen stethoscopically to the sounds at any of these accelerometer locations. The use of this system alone, however, led to little more than open conjecture as to where these impacts were occurring and

what was causing them. Representatives of the vendor that supplied the reactor were attempting to minimize this guesswork by recording the outputs of each accelerometer using a 14 channel tape recorder. Equipt with a dual-trace storage oscilloscope, and a Polaroid camera, they then attempted to triangulate on the origin of these impacts by measuring the time delays between pulses. This was a slow and tedious procedure since only two pulses could be analyzed at a time, and each of these then needed to be correlated with the next. Their initial conclusions indicated that the impacts were indeed emanating from somewhere in the bottom of the pressure vessel, and that they did not "seem" to always occur at the same point. The lack of precision imposed by this technique still left the question unresolved as to whether the source was a loose core barrel hitting the vessel wall, or whether some actual lost object was being battered about in that lower vessel area.

If the former were the case, then neutron noise measurements would surely bare this out. On the other hand, if these impacts were caused by a lost object, then the problem became one of identification. Knowledge of the energy of these impacts would assist in at least determining the size of the object. As Unit 3 was still under construction, it was the obvious choice for use in obtaining at least a crude calibration for comparison with the accoustical emissions emanating from Unit 2. Various objects attached to a fishing pole of sorts were dropped into, rubbed against, and even battered about Unit 3. These tests were tape recorded and comparisons made. To be honest, however, the comparisons made by the

human ear, with its remarkable pitch and tonal discrimination ability, probably had as much influence on the final analysis as did the physical measurements. The vendor concluded: if it is an object, it's bigger than a golf ball, smaller than a basketball, most likely about the size of a soft ball, and certainly none of the above named objects--not much to go on but something nontheless.

By that time, Drs. Mott and Robinson had collected sufficient data to conclude that the core barrel was secure and probably not the source of the problem. At this point, the vendor and UT personnel pooled their information and dragged out the blueprints. With each explaining his own analysis, raising possibilities while rejecting others, a consensus was finally reached: a bolt retainer cap from one of the recirculation pumps had come loose, travelled down the pipe and through the downcomer. Once in the bottom of the vessel, it simply continued to bang around. The actual disassembly of the reactor proved that this conclusion was correct, and the system was repaired.

Consider, however, the cost of the project in terms of downtime, manpower, equipment usage, transportation, etc. The experience made it clear that existing loose parts monitoring systems alone, as found throughout the nuclear industry--not just at this particular plant--simply do not provide the information necessary to formulate a sound diagnosis in a reasonable length of time even at considerable expense. Neither could that time be shortened, nor the expense diminished with experience, for with each new accoustical emission observed, the same tedious procedure had to be employed in the same inefficient manner. If loose parts monitoring systems were ever to

supply meaningful diagnostic information with the speed and accuracy demanded by the times, considerable upgrading of the speaker-switch system would have to be forthcoming.

CHAPTER II

DECIDING WHAT TO MEASURE

Of all the difficulties encountered in troubleshooting the problem, locating the part and estimating its size were undoubtedly the most frustrating. What was needed was a system that could choose as a datum the signal received at one of the accelerometers and compare it with the relative time that it took for the initial wave to reach two or three others, and at the same time measure the respective pulse magnitudes. Also needed was the incorporation of a data handling system such as a minicomputer as a means to rapidly accumulate and document this information. The realization of these three goals form the foundation of this thesis.

The first of these could be achieved by attaching a triggering circuit to the output of each accelerometer which would control a digital counter. When the sound from an impact reaches the nearest accelerometer, it would inhibit its own counter and start all of the others, thereby establishing the datum. These others in turn would independently stop themselves upon receipt of the sound wave at their respective accelerometers.

In order to exemplify this idea, consider Figure 1. Points A, B, and C are the locations of accelerometers, and X is the point of impact. Since A is closest to X, its counter is not activated while counters B and C are turned on. Counters B and C then stop when the wave reaches them, recording times t_b and t_c respectively.

If the speed of sound in the medium is γ, then γt_b and γt_c define the radii of the circles around B and C. Point X must lie at the center of a circle that goes through point A and touches the circles about B and C at only one point. Noticing that it was assumed that the speed of sound in the medium was known, even this becomes unnecessary if an extra accelerometer and counter are incorporated into the system at some point D. Then, by simply choosing some arbitrary speed of sound (say γ_0), and proceeding as before, a circle of radius $\gamma_0 t_d$ is formed. If the circle about D goes through either two points on the circle about X (meaning γ_0 was too large), or no point (meaning γ_0 was too small), then a new speed of sound, γ_1, is chosen and the procedure repeated until satisfied. Since the system is designed to be tied into a minicomputer, such iterations become quite simple once programmed.

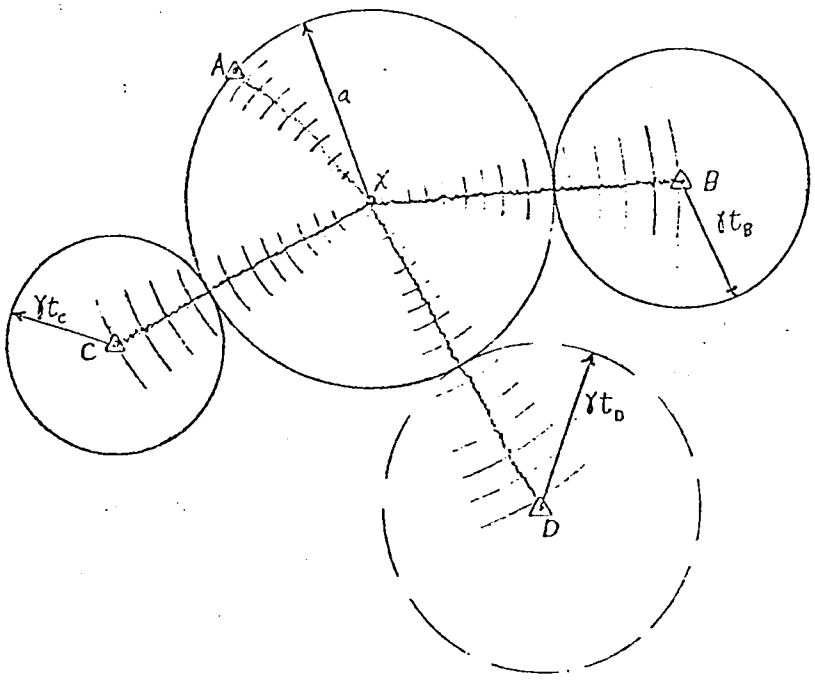


Figure 1. Graphical Solution on an Open Surface.

In practice, the system would probably be calibrated in terms of these time delays by actually impacting the system at various points, whereby the speed of sound to be used in the analysis could be determined. At first glance, this may lead one to conclude that the fourth channel is superfluous, except as a backup check or if one of the others were to malfunction. This is not the case at all. The fourth channel is absolutely necessary. Consider a closed surface with only three accelerometers. No matter how the accelerometers are positioned, there will always be two points (say X and Y) which would represent centers in the circle formed by only three accelerometers. In order to exemplify this point, consider the simple hollow sphere depicted in Figure 2 with accelerometers arbitrarily positioned at points A, B, and C. If the three path lengths $\overline{AX} = \overline{BX} = \overline{CX}$, then $t_A = t_B = t_C = 0$, and X is a center. Similarly, $\overline{AY} = \overline{BY} = \overline{CY}$ implying that Y is also a center. Yet X and Y are two different and distinct points on the surface. The addition of a fourth accelerometer anywhere on the surface resolves this ambiguity with one exception. It cannot be placed on the circle defined by A, B, and C. In using the term "circle" in conjunction with an irregular closed surface, it is meant the locus of points passing through A, B, and C that are accoustically equidistant from some single point within that locus.

One other point to be made is that even the bounding of an open surface requires either four accelerometers or the careful positioning of three. Simply place a hole in the top of the hollow sphere in

Figure 2 and it becomes obvious that if only three are used, either X or Y must lie in the hole.

Having found the point of impact, it is necessary to know something about the source. One indicator of this would be the energy of an impact. This can be determined by measuring the length of time that the pulse observed in an accelerometer is above some reference level if the following parameters are known: the shape of the pulse $f(t,x)$ in terms of its decay rate $\frac{\partial f(t,x)}{\partial t}$, the attenuation in the transmission medium $\frac{\partial f(t,x)}{\partial x}$ along with the location of the impact found via triangulation, and the magnitude of the output of an accelerometer as a function of the energy imparted by an impact at the accelerometer location. Notice that the first parameters are directly related to properties of the material and that the third

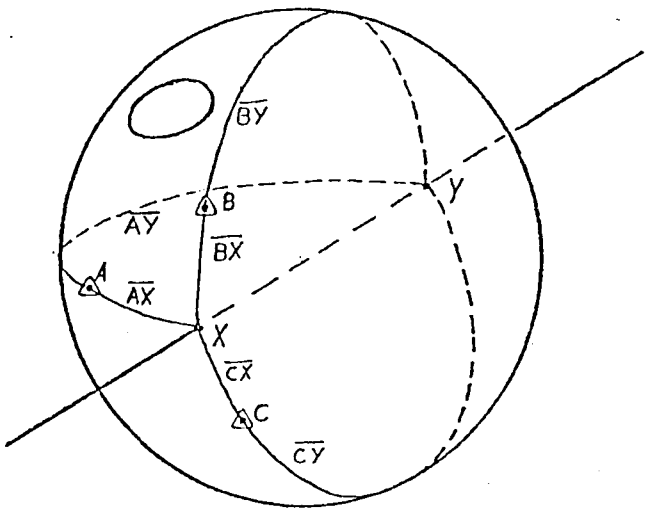


Figure 2. Points of Ambiguity on a Hollow Sphere.

is a property of the accelerometer. All three can be measured. Hence, in principle, the initial impact energy could be determined if one were dealing with an idealized system. This, of course, is not the situation, and the only practical approach is to calibrate the system by actually impacting it and recording the corresponding time that the transient is above some reference level.

Consider now how the time that the pulse is above the reference level could be measured. One way probably used by some investigators is to set a fixed reference voltage level, observe a very narrow bandwidth of input frequencies and record the number of times that the signal exceeds the reference level. This approach has the advantage of being able to provide results which are directly related to some fixed absolute, but has two very serious drawbacks. First, by setting a fixed voltage reference level, the dynamic range is limited to impacts above some minimum energy which in turn is dictated by the noise level of the system being monitored. In a nuclear reactor, that noise level varies widely from one point to another and at various power levels. Hence, the reference voltage must be set above the highest expected noise level, allowing smaller accoustic emissions to go unnoticed even though the background noise may be quite low. Secondly, the observance of only a narrow bandwidth of frequencies is a technological Pandora's Box which is opened by asking the questions: What frequencies should be monitored and why? These are not trivial questions, nor ones to be answered in arbitrary platitudes, such as, it doesn't really matter. It matters greatly and look at a couple of mathematical and physical relations shows why. If the impact constituted a perfect step change in the state of the matter at the point of impact, then it could be

maintained that the response to this in the immediate vicinity of the impact, would be the excitation of all frequencies whose magnitudes could be defined mathematically by the Fourier coefficients for such a change. These would then dampen out until those left represented only the resonant frequencies of the system. The implicit assumption is that an impact does represent a perfect step change in the state of the material, which it is not, unless the collision is a perfectly elastic one. Hence, the elastic properties of both the material being struck, and those of the object which strikes it, define the magnitude of an impulse, since it is the application of a force over some period of time that defines the change in momentum. That is, striking a steel pipe with a hammer excites a different set of frequencies than does hitting it with a piece of wood or a tennis shoe, because the force is distributed over different lengths of time. Hence, the corresponding rate of change in momentum dP/dt is also different. The point of all of this is that if one arbitrarily chooses a small band of frequencies to observe, he may well find himself looking for tennis shoes. In order to avoid such embarrassment, it was decided to leave the frequency window as open as possible and measure the actual time that the pulse was above a floating reference level which follows the background noise level. In doing so, one no longer needs to be concerned about what maximum background noise level can be expected in the reactor, and can focus his attentions on exactly what size signals above background need to be monitored. This is discussed in detail in the following chapters.

CHAPTER III

THE SYSTEM

The basic system, blocked diagrammed in Figure 3, consists of four identical "Channels" and a "Control Board." Each "Channel" contains both analog and digital electronics; the "Control Board" is purely digital logic. All five boards are single-sided finolic, printed-circuit boards which are designed to plug into dual length, DEC backplanes (BPI through BPV). An M-404 crystal controlled digital clock on backplane (BPVII) provides the base frequency for all timing circuits. Data, computer interrupt command, and computer generated reset-command are bussed from backplane VI to a DEC M-1501 Bus Input Data Interface, via four, 6 foot DEC cables no. BC04Z-06. All backplanes are wired so that the required interlocking circuitry is obtained.*

The Analog Electronics

Figure 4 gives the schematic diagram of the analog section of a typical channel. The input is high pass a-c coupled to operational amplifier LM1 which is in a voltage-following configuration. This combination removes the low frequency signals and provides isolation for the rest of the system. The next four amplifiers, LM2, 3, 4, and 5 combine to give the negative absolute value of the system input at the output of amplifier LM5. A negative voltage at resistor R2,

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*See Appendix C and in the Pocket.

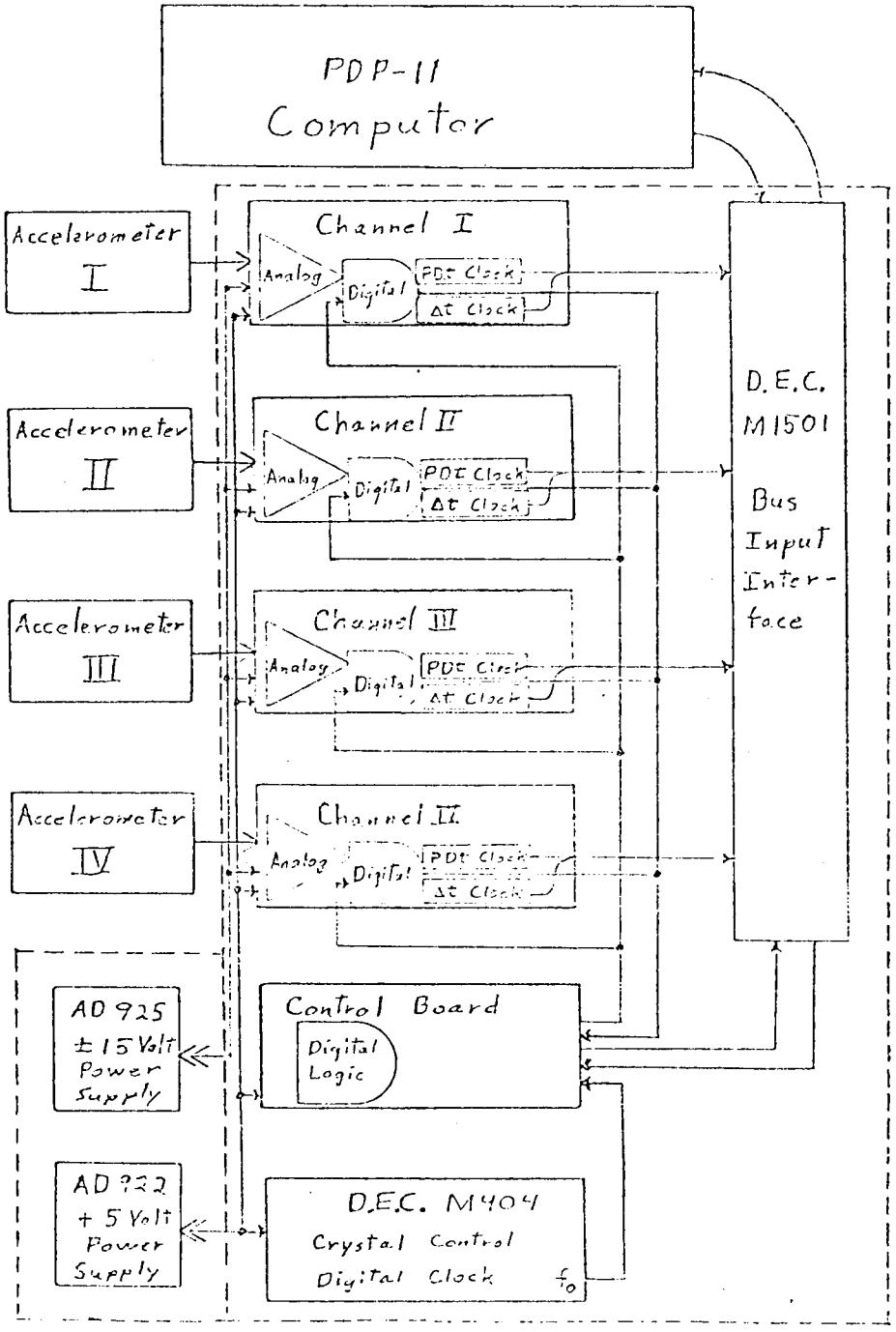


Figure 3. A Block Diagram of the LPM.

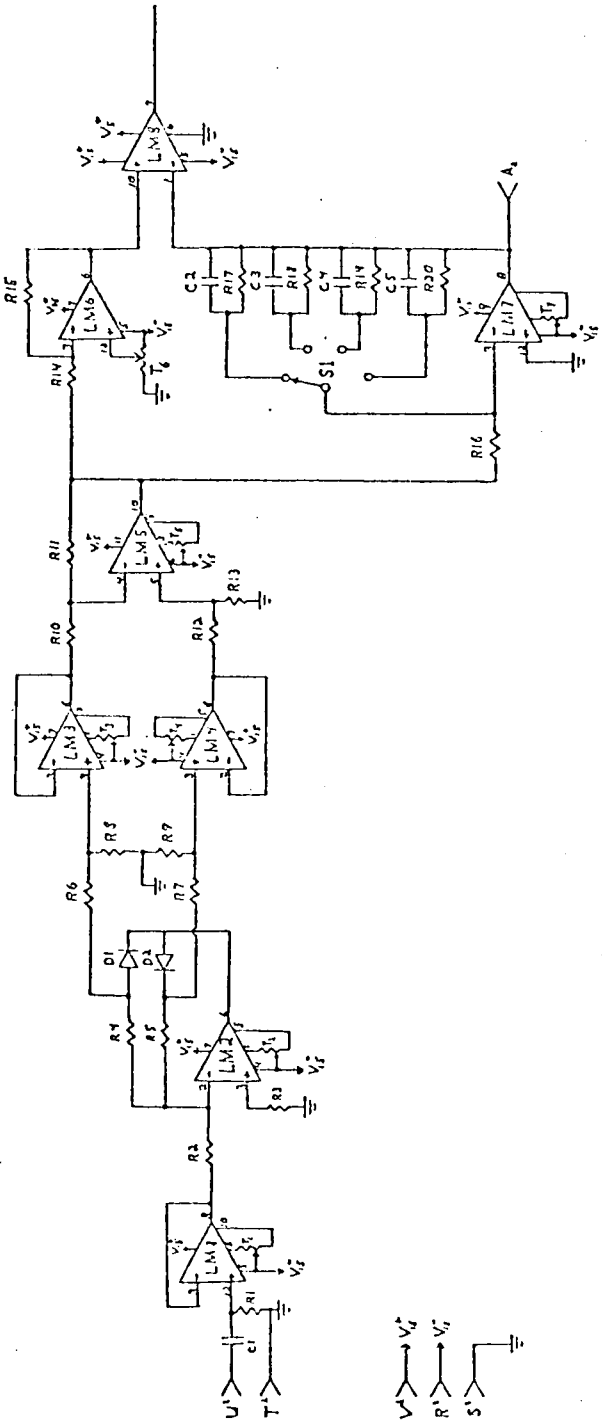


Figure 4. Analog Section of a Typical Channel.

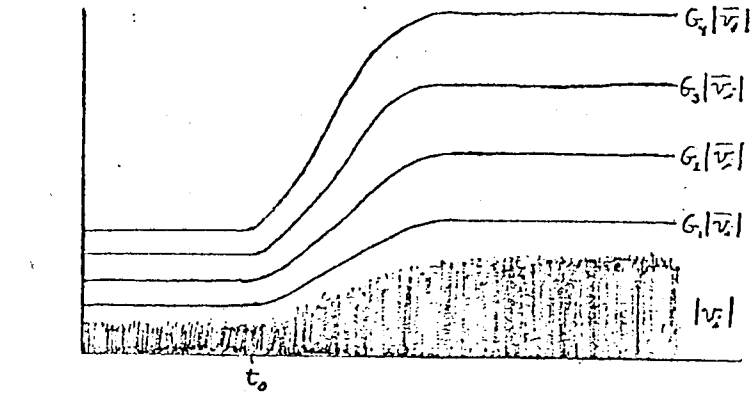
forward biases diode D1 allowing feedback through resistor R4, and reverse biases diode D2. A positive signal at the same point changes the biasing allowing feedback through resistor R5. The values of resistors R4, R5, and R2 are chosen to give a gain of two. The voltage divider formed by resistors R6 and R8 reduce the output voltage at resistor R4 by a factor of two when diode D1 is conducting, and resistors R7 and R9 do the same for resistor R5 when diode D2 is conducted. This multiplying and dividing by the same value is necessary since without resistor R8, amplifier LM3 has no path to ground when diode D1 is reverse biased. The same holds for amplifier LM4. The output of amplifiers LM3 and LM4 are summed via amplifier LM5 operating in the differential mode with unity gain. This circuit gives the true negative absolute value of the incoming signal regardless of its shape.

The next three amplifiers, LM6, 7, and 8 combine to form a transient detector which is the real starting point in the analysis of the signals received. Previous circuitry is primarily signal conditioning for this stage. Amplifier LM6 is an FET-input, op-amp in the inverting configuration. Amplifier LM7 is of the same type having four pre-selected gains with the same RC time constant. Each is obtained by selecting the appropriate position on switch S1. Integrated circuit LM8 is an FET-input voltage comparator which can have only one of two output states: zero or +5.0 VDC.

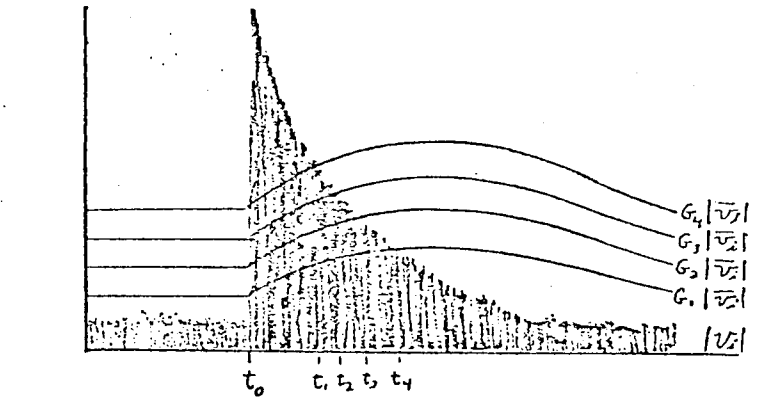
Combined, they work as follows. If the system input at terminal U^2 is $(v_i + V_i)$, where v_i is some time varying signal and V_i is the DC component, then the output of summing amp LM5 becomes

$-|v_i|$. Amplifier LM6 being an inverter with DC offset capabilities via trim-pot T6 has an output ($|v_i|$ + V offset). The output of amp LM7 is $v_{ref} = G_x|\bar{v}_i|$, where G_x is one of the four fixed gains, and $|\bar{v}_i|$ is the "time averaged value" of $|v_i|$ resulting from the 300 msec RC time-constant in the feedback loop. If $|\bar{v}_i|$ is approximated by the relation $|\bar{v}_i| = 0.7071\ |v_i|$, and typical values assigned to G_x are 3.0, 4.3, 5.6, and 7.5, then the resultant values of v_{ref} are $2.1|\bar{v}_i|$, $3.0|\bar{v}_i|$, and $5.3|\bar{v}_i|$ respectively. This is true, however, only if the rate of change of the "time averaged value" of $|v_i|$ is slow with respect to the 300 msec RC time constant. For example, if the value $|v_i|$ were to double in 3.0 sec following a ramp function, then v_{ref} would follow this change rather closely, as illustrated in Figure 5a. If, on the other hand, $|v_i|$ were to take a sudden step in amplitude, Figure 5b, then v_{ref} must necessarily lag behind, following this change only as fast as its time constant will allow.

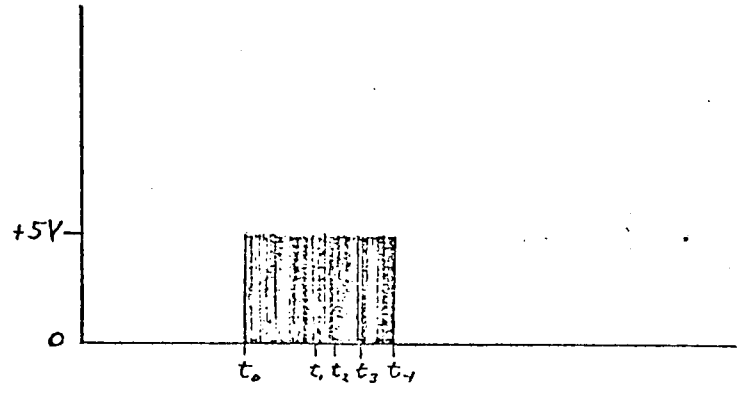
Consider the effect of these two situations on the output of the voltage comparator LM8. In the first case, Figure 5a, ($|v_i|$ + V_{offset}) never exceeds v_{ref}, hence the output of the comparator is always zero. In the second case, the output of the comparator LM8 shown in Figure 5c is zero until time t_o, at which point ($|v_i|$ + V_{offset}) exceeds v_{ref} and the output jumps to +5.0 volts. By making time t_o the datum, then times t_1, t_2, t_3, and t_4 represent the periods that the pulse observed in $|v_i|$ was above v_{ref} for their respective gain settings, G_x.



(a)



(b)



(c)

Figure 5. Effect of Slow and Fast Varying Transients on the Output of Comparitor LM8.

Timing

Before proceeding with an analysis of the digital logic, and timing involved in each of the four typical channels, it is worth discussing the M-404 clock and the associated circuitry used to feed the pulse duration time (PDt) counters BC1 and BC2, and the delay time (Δt) counters, BC3 and BC4. The 50 KHz output of the M-404 crystal clock is tied from BPVIII, terminal N_2 to BPV, terminal D_2 where it is fed directly to the input of binary counter BC7 on the Control Board. Switch S2 feeds all of the Δt counters, while switch S3 feeds the PDt counters. Regardless of what base frequency, f_o, is chosen among those available from the M-404 clock, the binary counter BC7 in conjuction with switches S2 and S3 will provide the following frequencies: f_o, $f_o/2$, $f_o/16$, $f_o/4$, and $f_o/8$ by stepping either switch from the full clockwise position to the full counter-clockwise position. Electronic Data Sheet 1, Appendix A gives the wiring diagram for the M-404 along with the available values for f_o.

The five different frequencies provided by S2 and S3 when combined with the (eleven) available values for f_o not only provide a high degree of versatility, but if used properly can greatly enhance the precision of the measurements. Taking the delay time counters as an example, let the maximum distance between any two accelerometers be d feet, and let the speed of sound in the medium be γ feet/sec. Since the maximum number of bits is 255, the optimum frequency to be used would be $f_o = 255(\gamma/d)$. At that frequency, an impact occurring at one of the two most distance accelerometers would exactly fill the Δt counter attached to the other. The resultant counting error in

such a measurement would be less than 1 part in 128, since the state of the clock is unknown at the points in time when the gate is opened and when it is closed. The reason for taking this approach rather than simply using one or two stock clock frequencies and more data bits is that the cost of handling more bits of data rises non-linearly due to larger interfacing requirements, computer storage space, processing time, etc.

Measuring the Pulse Duration Time, PDt

Now, let us look at how a pulse duration time is measured, and define PDt in terms of what is actually being measured. The output of switch S3 exits BPV at terminal B_2 and enters each of the four channels via their respective backplanes on terminal E_2 shown in Figure 6. There, it is held at NAND gate DM5, pin 13 and prevented from passing by a low voltage on pin 2. Upon incursion of a transient of sufficient magnitude, the output of comparator LM8 pulses high each time that its input is above its floating reference. These pulses are received at the input pins 3 and 4 of the monostable multivibrator or "one-shot" labeled DM1 in Figure 6. Capacitor C6 and resistor R21 determine the pulse width (τ_{pw}) of the outputs on pins 8 and 6 by the following formula,

$$\tau_{pw} = 0.32\ RC\ (1 + \frac{0.7}{R}) \qquad (3.1)$$

where τ_{pw} is in milliseconds, R is in kilo-ohms and C is in micro-farads. In this case, the values have been chosen to give a pulse width (τ_1) of 0.1 micro-second. These pulses are then fed from pin 8 of "one-shot" DM1 to input pins 3 and 4 on DM3 which is another monostable multivibrator having an output pulse width (τ_3) of 1.0

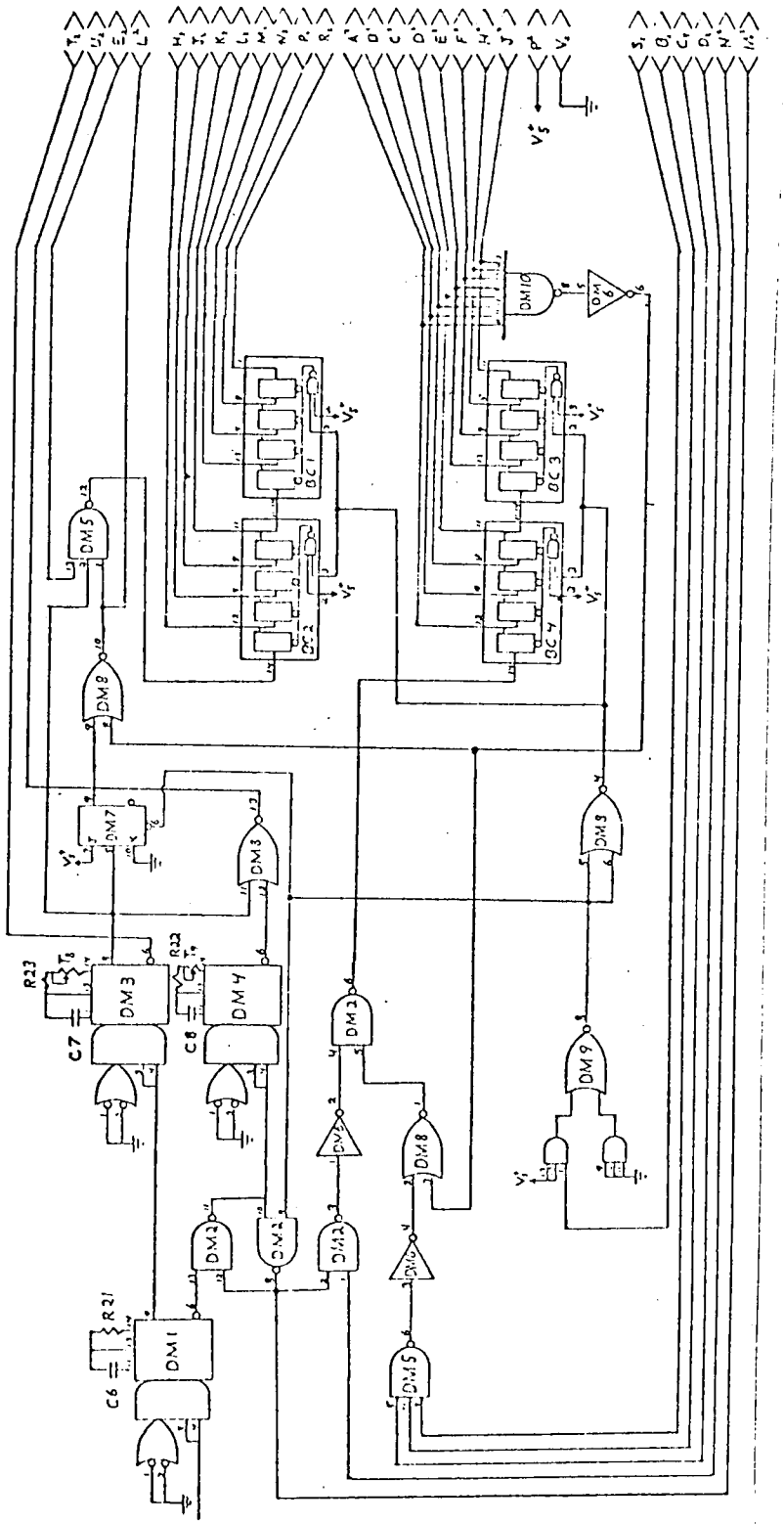


Figure 6. Digital Section of a Typical Channel.

msec as dictated by C7, R23, and T8. One curious property of the "one-shot" is that when pulses are received at intervals shorter than the pulse width, τ_{pw}, the output at pin 8 will remain high. Consequently, as long as the output of the comparator, LM8 is switching at frequencies greater than 1.0 KHz and less than 10 MHz, the output of pin 8 on DM3 stays high. This opens the 3-input NAND-gate DM5 by providing a high input to pin 2 which in conjunction with a high input on pin 1 allows the pulses received at pin 13 to be clocked into the binary counters BC1 and BC2. Once the output of the comparator LM8 stops switching for 1.0 msec, meaning that either the reference level has exceeded its input voltage or that the input frequency at backplane terminal U^2 is less than 0.5 KHz, pin 8 on one-shot DM3 goes low causing pin 9 on J-K flip-flop DM7 to latch high. This, in turn, is inverted at pin 10 on NOR-gate DM8 thereby closing the NAND-gate DM5 by setting its input pin 1 low.

Figure 7 illustrates the various states of the outputs of the circuits used to measure the pulse duration time, PDt, which can now be defined as the length of time that the amplitude of an input transient having a frequency greater than 0.5 KHz and less than 5.0 MHz, is above the reference level, plus 1.0 msec.

Measuring the Delay Time

In order to describe exactly how the delay time Δt is measured, it is necessary to choose one of the channels as being connected to the accelerometer closest to the point of impact. As all of the channels are identical, we shall say that the channel arbitrarily

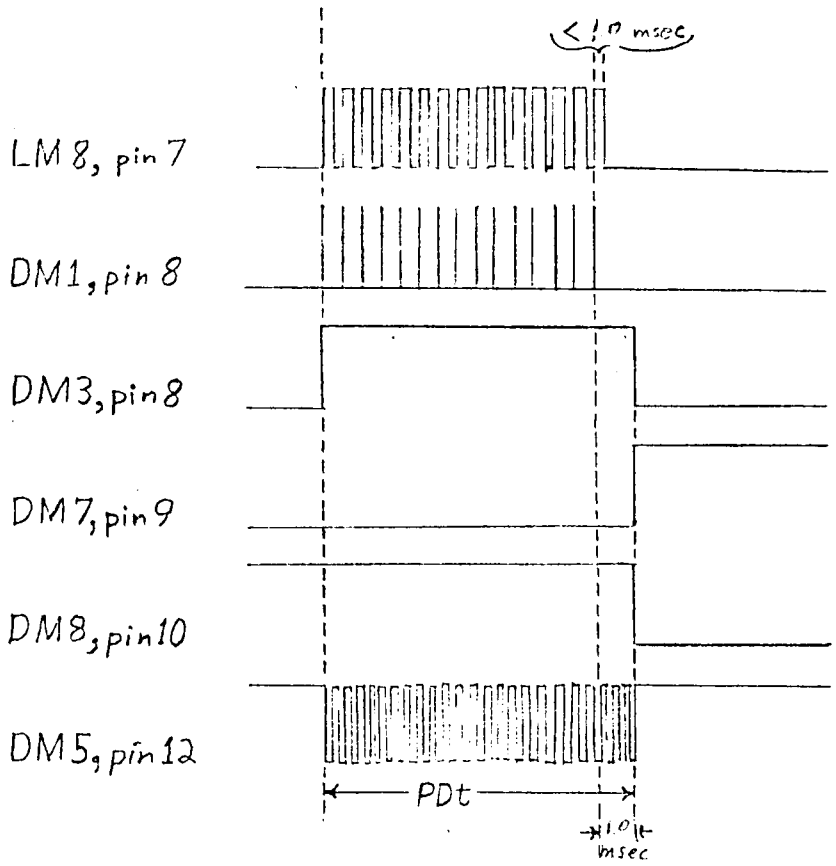


Figure 7. "Pulse Duration Time" Gating Sequence.

labeled "Channel I" on the full schematic in the Pocket starts the sequence of events by detecting the transient before any of the other three.

The first thing to notice is that the output of switch S2, which provides the clock inputs to the Δt counters, enters the respective backplanes on terminals N^2. From there, the clock pulses must pass through NAND-gate DM2, at pin 1, and through one of its sister gates DM2 at pin 4. Prior to the receipt of a transient while all circuits have been reset and waiting, pin 2 on NAND-gate DM2 is high, thereby allowing the clock pulses to pass through that gate to the input of its sister gate at pin 4 where they are held by a low input on pin 5. This low input results from the fact that prior to the receipt of a transient in any of the other three channels, their respect NAND-gates DM2 at pins 8 have a +5 volt potential, which in turn are connected to pins 3, 4, and 5 of NAND-gate DM5 in Channel I via backplane terminals B_2, C_2, and D_2. (Note that since all channels are the same, pins 3, 4, and 5 on NAND-gate DM5 of each of the other three channels must use as their inputs the output of NAND-gates DM2 pins 8 on Channel I and the other two remaining channels.)

Now let a transient in $|v_i|$, as described earlier in the discussion of the PDt measurement, cause the comparator LM8 in Channel I to change output states, i.e., zero volts to +5.0 VDC. The output of one-shot DM1 at pin 6 goes low on the leading edge of the output of the comparator. The two NAND-gates labeled DM2 having outputs on pins 8 and 11 are wired to form a high speed latch, resulting in pin 8

8 latching low when pin 6 of the on-shot DM1 goes low. This low on pin 8 puts a low on pin 2 of DM2 thereby closing that gate and preventing any clock pulses from entering the Δt counter in Channel I. Simultaneously, pins 5 on NAND-gates DM5 in Channels II, III, and IV are set low allowing pulses to be clocked into the Δt counters of each of those remaining channels. Upon receipt of the transient at these channels, each in turn will shut itself off through the same sequence of events that prevented Channel I from starting. Hence, the delay times with respect to Channel I, which becomes the datum, are stored in the binary counters BC3 and BC4 in each channel.

Controls

The control board monitors four points in each of the four channels. Pin 13 on DM8 is the false start indicator; a low output state on pin 8 of NAND-gate DM2 indicates that data has been received; a low state on pin 10 of NOR gate DM8 indicates that both counters have been stopped; a low output on pin 6 of one-shot DM3 indicates a transient in progress. Using the information obtained from these sixteen points logic decisions are made on the control board which determine whether to send a "read data" command to the computer, or to automatically reset itself. In either case, a reset command will be issued, either from the computer or internally, and the control board must recheck the status of the channels before executing the command in order to prevent activation of the system while a transient is in progress.

The false start circuit is active only during the first τ_4 seconds* of a transient and serves the dual function of rejecting transients having a frequency of less than $1/(2\tau_3)$ as well as very short transients having a duration of less than $(\tau_4-\tau_3)$ seconds, which could be extected as a result of electronically induced spikes. Here is how it works, let the comparator LM8 change states at some time causing pin 8 on one-shot DM1 to go high, which in turn causes pin 8 on one-shot DM3 to go high for τ_3 seconds. At the same time, the output pin 6 on one-shot DM1 goes low causing pin 11 of NAND-gate DM2 to latch high thereby triggering a single τ_4 second low pulse at pin 6 of one-shot DM4. Notice that DM3 was triggered before DM4 due to the switching time δ in NAND-gates DM2. Even though δ is on the order of 20 nsec, it is still quite important upon examination of the input and output states on pins 11, 12, and 13 of NOR-gate DM8. Referring to Figure 8 which shows the input/output states of NOR-gate DM8, prior to time t_o, the input at pin 11 is low and the state of pin 12 is high, hence, the output, pin 13, is low. At t_o, the potential on pin 11 goes high, and the state of pin 13 remains unchanged. Then 20 msec later, the state of pin 12 switches low still leaving a low potential on pin 13. In fact, the only way that the output can go high is if the input at pin 11 goes low during the time τ_4. This can occur only under two conditions. Case 1: If the duration of the transient is less than $(\tau_4+\delta-\tau_3)$ then the input at pin 11 will go low before pin 12 switches back high (Figure 8, Case 1).

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*τ_4 is the pulse width of the output of "one-shot" DM4.

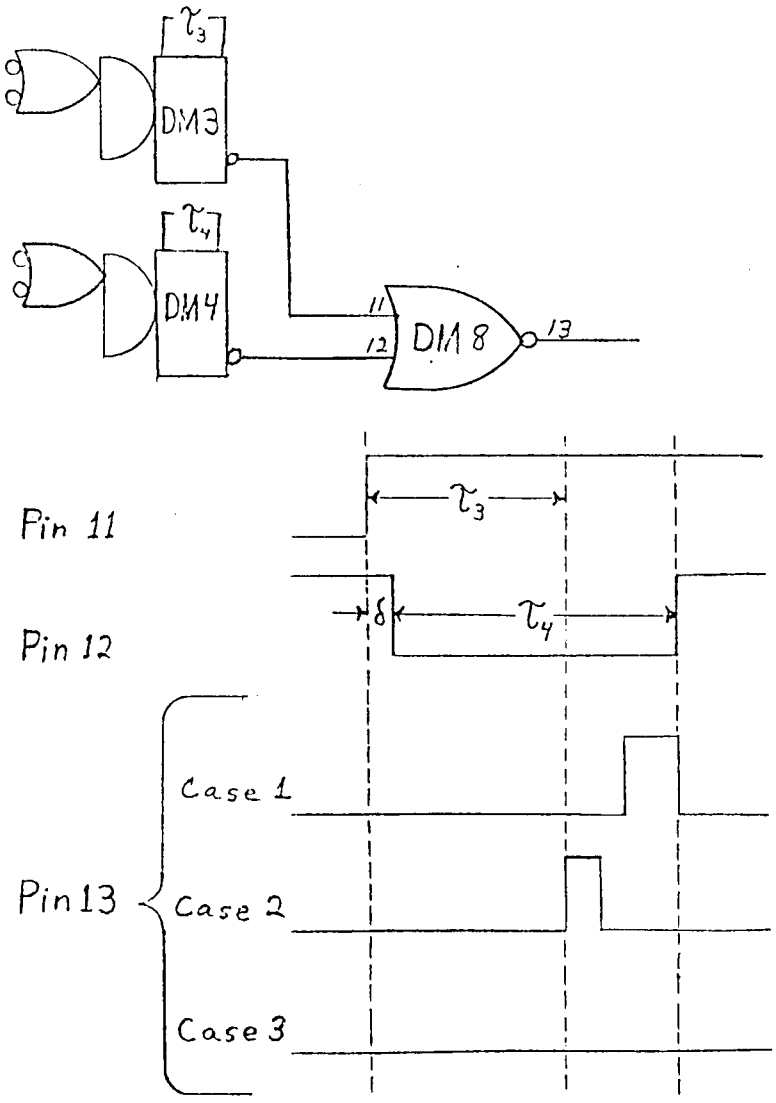


Figure 8. False Start Indicator Circuit and Timing Sequence.

Case 2: If the transient is so slowly varying that the comparator LM8 fails to change states within time τ_3 (Figure 8, Case 2), then one-shot DM3 will not be retriggered in time to prevent its output from switching states causing the voltage on pin 11 on DM8 to pulse low for the period (1/2f) - τ_3, where f is the initial frequency of the transient. If neither condition exists, then the output remains low as shown in Figure 8, Case 3. Typical values chosen for τ_3 and τ_4 are 1.0 and 1.1 msec respectively, which means that transients having a total duration of less than 0.1 msec are rejected, as are those having a duration greater than 0.1 msec, but a frequency of less than 0.5 KHz.

The actual process of declaring a false start occurs in the control board circuitry, Figure 9, AND-OR-Invert-gate (AOI) DM11 monitors the outputs of pin 13 of NOR-gates DM8 on each of the channels. If the outputs of any one of these goes high for as little as 40 nsec, (this is the maximum swtiching time for the J-K flip-flop) the output of AOI-gate DM11 goes low and clocks a pulse into J-K flip-flop DM18 via pin 1. This latches a high output state on pin 12 which is connected directly to the input of AOI gate DM19 at pin 2. This gate is essentially a reset command monitor in that a high state at any of its three available inputs will put a high state on pin 9 of AOI-gate DM22. This gate, in turn, will execute this command only if its input pin 10 is also high as a result of high input states on all of the inputs to NAND-gate DM21 which, not surprisingly, happens to be the "transient in progress" monitor. Its

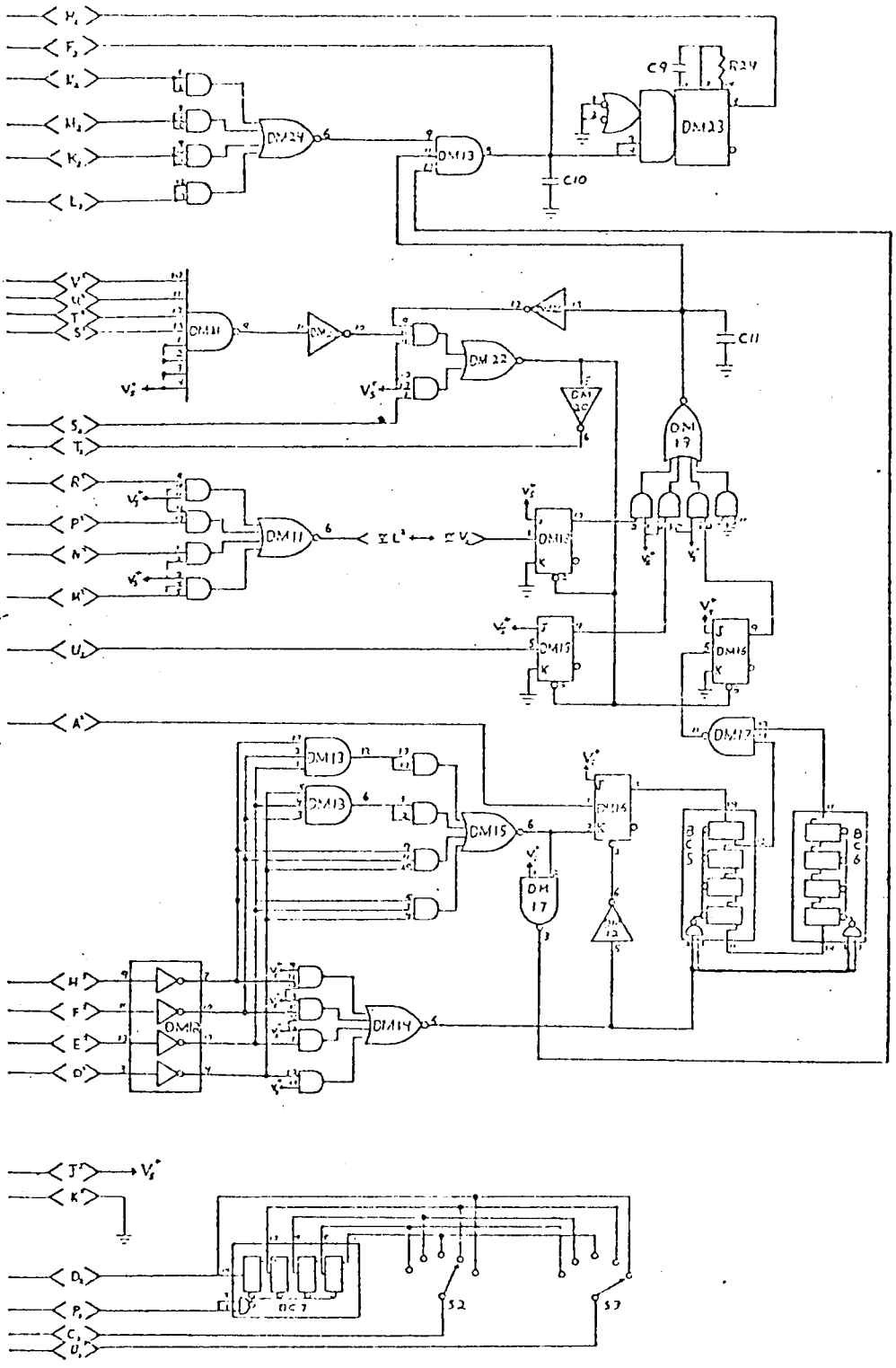


Figure 9. Control Board Schematic.

four inputs are the outputs on pin 6 of one-shots DM3 in each of the four channels. These outputs can be high only if their comparators are not switching states, thereby indicating that a transient of sufficient magnitude to exceed v_{ref} is not in progress.

Barring any false starts, and preceeding as before, assume that an impact occurs near accelerometer I which prevents Δt counter I from starting, thereby establishing the datum, and simultaneously starting all of the other Δt counters. If the clock frequency chosen from swtich S2 is slightly less than the optimum frequency, then none of the Δt counters should register a full count of 255 unless the transient detector in that channel failed to trigger, in which case the output at pin 8 of NAND-gate DM2 would fail to latch low. When this situation occurs in any channel, all of the inputs to NAND-gate DM10 are set high which results in the placement of a high input state on pins 3 and 8 of NOR-gate DM8. This stops both the PDt and the Δt counters. Notice that all bits in the pulse duration counter are low, while all bits in the delay time counter are high. The occurrence of this constitutes a red flag stating clearly that the data contained in this channel is worthless.

The presence of worthless data in more than one channel justifies the issuance of an internal reset command in order to prevent the unnecessary interruption of computer. However, depending upon the positioning of the accelerometers, situations may arise where data in only three channels is sufficient to determine the source and magnitude of an impact. It is also desirable to have the system remain operational in the event of a single channel electronic failure.

Hence, the system is designed to initiate a "read data" command if any three of the four channels trigger within a specified time. This command can then be executed only after all counters have been stopped, which is indicated by a low output state on pin 10 of NOR-gate DM8 in each channel. So, here is how the 3 out of 4 channels triggered criterion works.

When a transient is detected, the output of pin 8 on NAND-gate DM2 latches low. The monitoring of this is done on the control board where each of these outputs is found on the input of one of the four inverts in digital integrated circuit DM12. Prior to the detection of a transient in any channel, all of the outputs of these inverters are low, resulting in high outputs on pin 6 of AOI-gate DM14 and on pin 6 of AOI-gate DM15. The clock output from switch S2, which is also used for clocking the Δt counters, is jumpered on the control board backplane BPV from terminal C_2 to terminal A_2 so that it ends up at the input, pin 1 of J-K flip-flop DM16. When the output of gate DM15 is high, the J-K flip-flop is in its normal counting mode, and would be counting, were it not for the high output of gate DM14 which holds it in the reset mode. Binary counters BC5 and BC6 are similarly held in the reset mode. At time t_0, one of the channels detects a transient causing one of the inverter outputs in DM12 to go high. This changes the output state of DM14 and removes the reset imposed on the binary counters BC5 and BC6, and the J-K flip-flop in DM16 that feeds them. These three modules are wired so that on the 258th pulse received from the clock, pins 12 and 13 on NAND-gate DM17 are both high resulting in a low output state that latches

a reset command into AOI-gate DM19 by setting output, pin 9, of flip-flop DM16 high. If, however, any other two inverter outputs on DM12 also go high prior to the 257th pulse from S2, then the output of DM15 goes low causing the output at pin 12 on flip-flop DM16 to latch high on the next pulse. This stops the counting and prevents the issuance of a reset command while simultaneously issuing a "read data" command by setting the input at pin 10 on AND-gate DM13 high. When all clocks have stopped, the output of AOI-gate DM24 goes high signaling its approval to pin 9 on DM13 to execute the "read data" command, provided there are no reset commands also awaiting execution, in which case pin 11 of DM13 would be low preventing its output from going high. If no reset command exists, one-shot DM23 will signal the computer with a single pulse of width τ_{23}* as dictated by C9 and R24 which is sent via terminal K^1 on BPVI to the M1501 Bus Input Interface on BERG Connector pin Z. Having read the data, the computer must issue a single positive going pulse of at least 40 nsec duration, via the same BERG connector pin X to terminal L^1 on BPVI. From there, it is jumpered to terminal U_2 on BPV and is stored in AOI-gate DM10 by latching the output of pin 9 high on flip-flop DM18. The reset is executed in the same manner described earlier and the system is ready to collect more data.

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*τ_{23} = 0.19 microseconds.

CHAPTER IV

PHYSICAL CONSTRUCTION

The physical layout of a typical channel is shown in Figures 10 and 11. Figure 10 gives the location and designation of each component as viewed from the "top" or component side. Figure 11 shows the printed circuitry also viewed from the component side. The physical layout of the control board and its components is given in Figures 12 and 13 in the same fashion.

Both of these printed circuit boards are single-sided with the printed circuit on the bottom side only. This, however, is not true of all of the boards, and since the DEC backplane is designed to accept both single and double sided boards, this brings up a point of nomenclature. All top side circuit board to backplane connections are designated by a capital letter followed by a superscripted or subscripted 1, e.g., A^1, B^1, A_1, etc. Bottom sided contacts are super- or subscript 2, e.g., A^2, B^2, A_2. A superscript denotes the upper set of 18 connections in Figures 11 and 13; a subscript refers to the lower. Since all boards are keyed and consistent with the nomenclature used by DEC, there should be no ambiguities.

The location of each board on the DEC backplanes is shown in Figure 14 and is viewed looking into the terminals. Channels I through IV are located on backplanes BPI through BPIV, each of which is separated by a sheet of 18 guage galvanized steel to prevent cross-talk

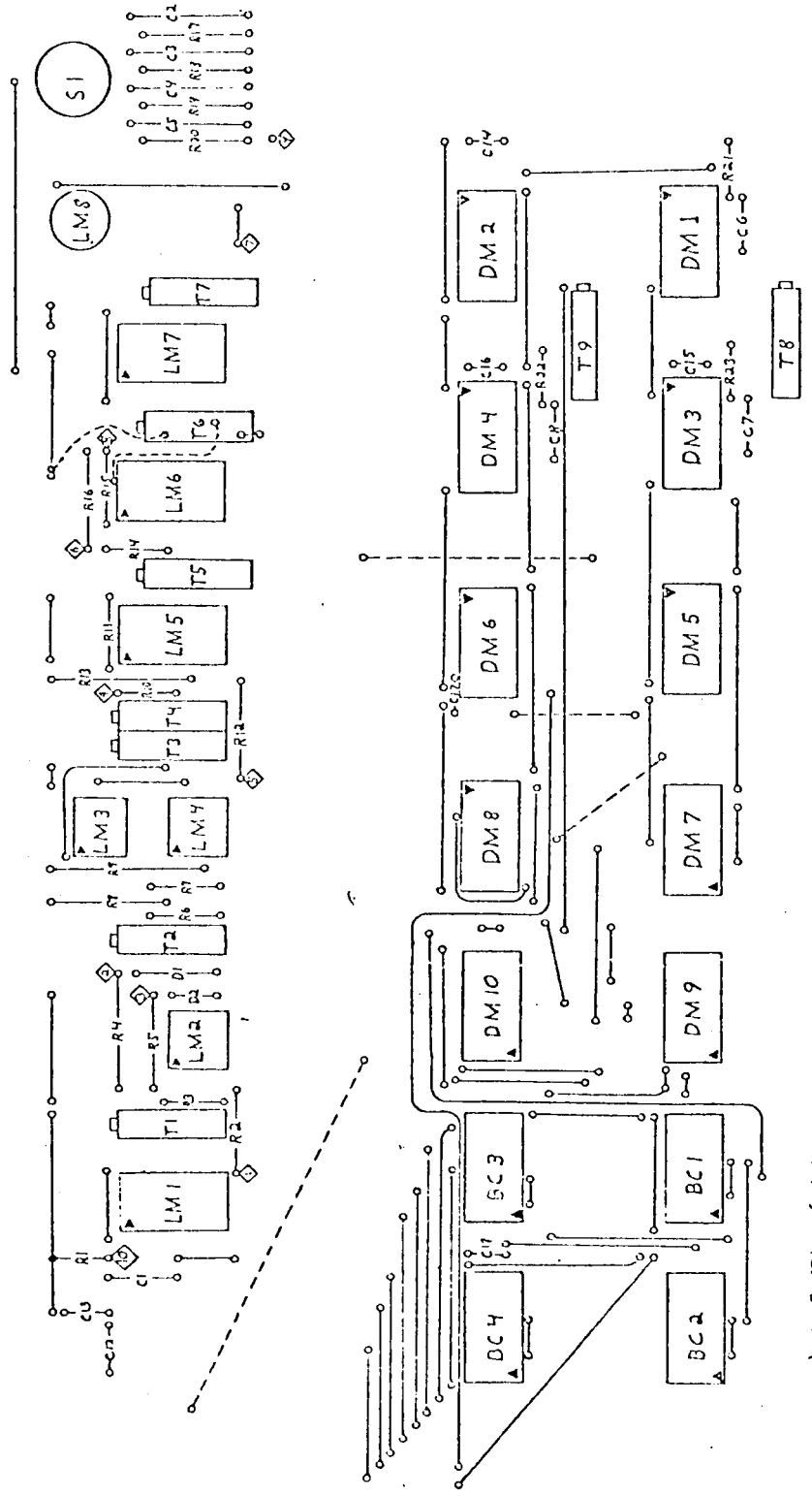


Figure 10. Physical Layout of a Typical Channel.

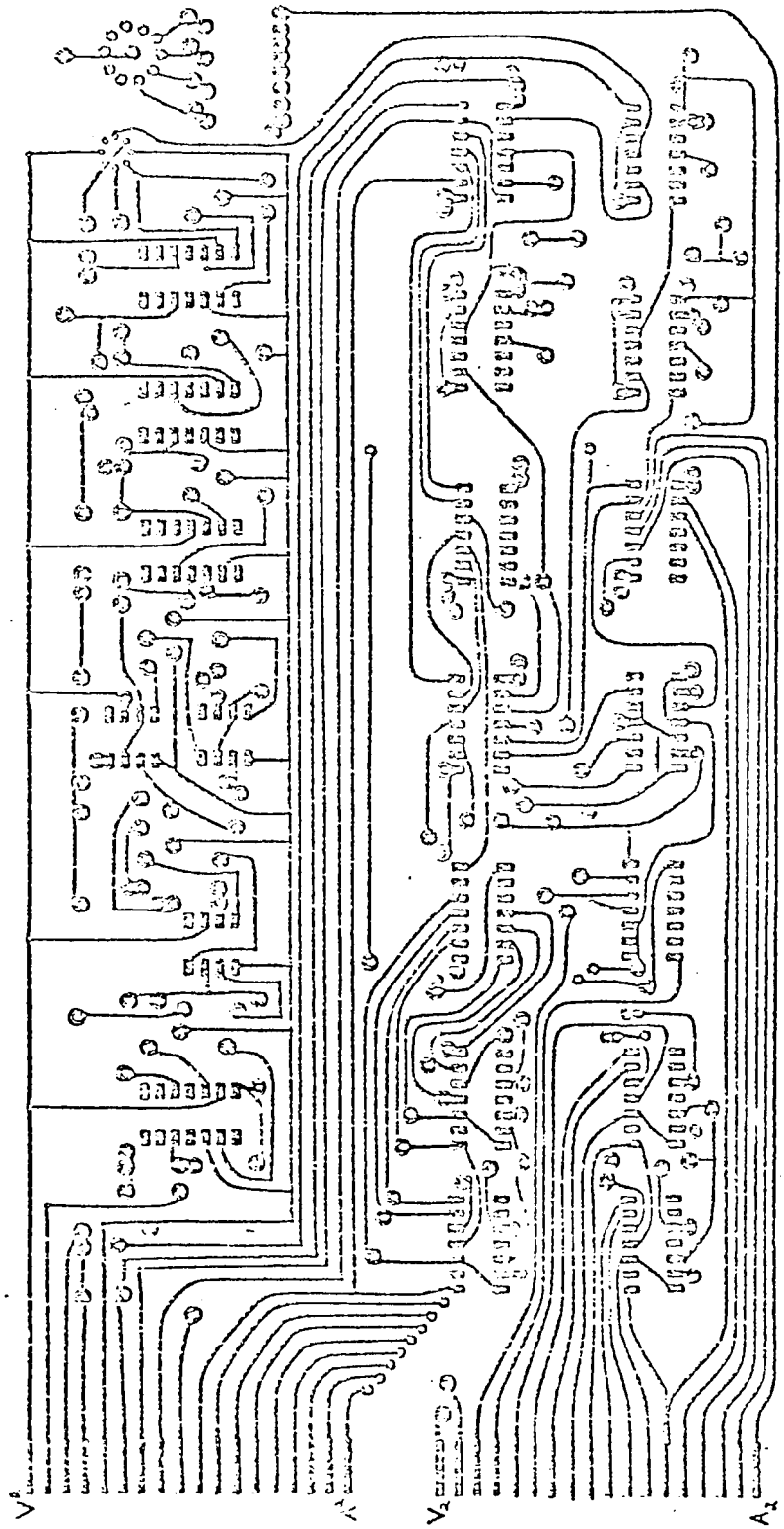


Figure 11. Printed Circuit of a Typical Channel (Top View).

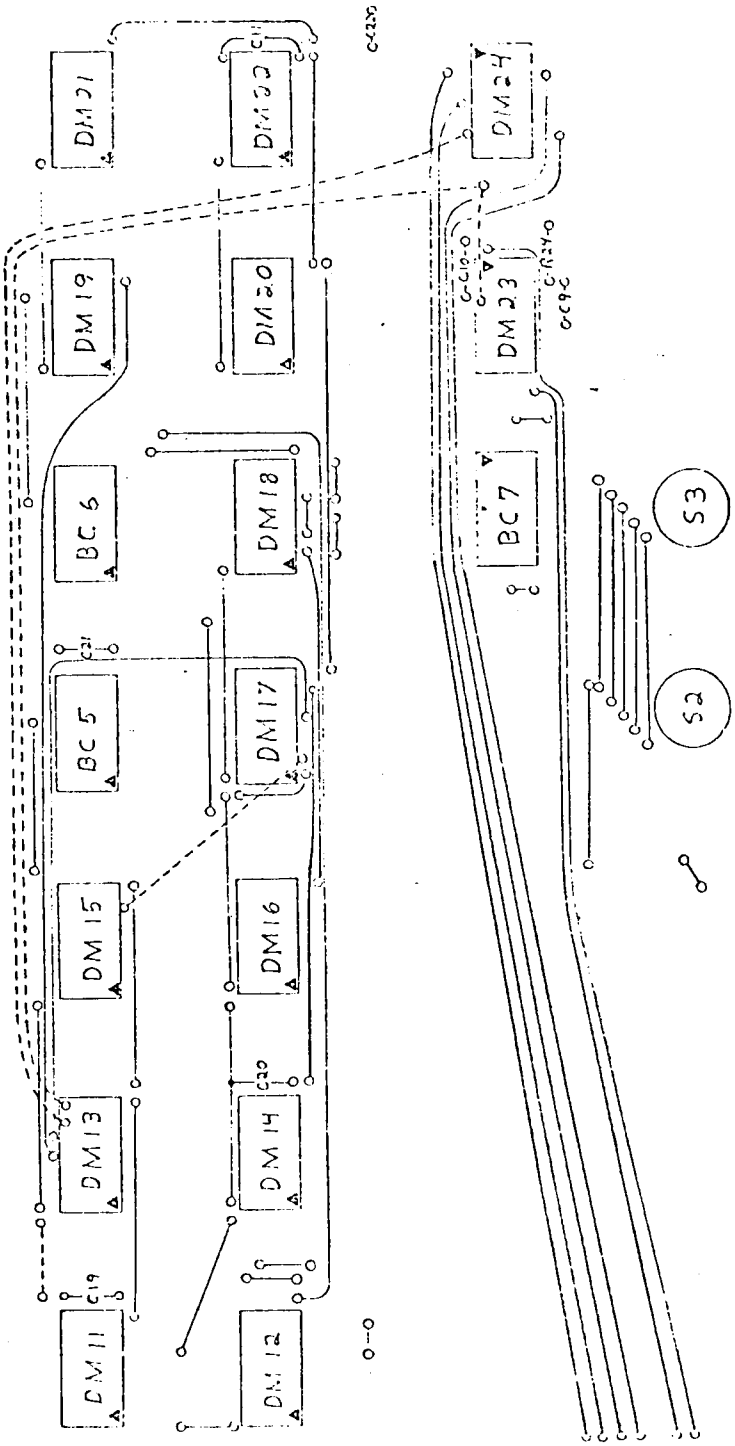


Figure 12. Physical Layout of the Control Board (Top View).

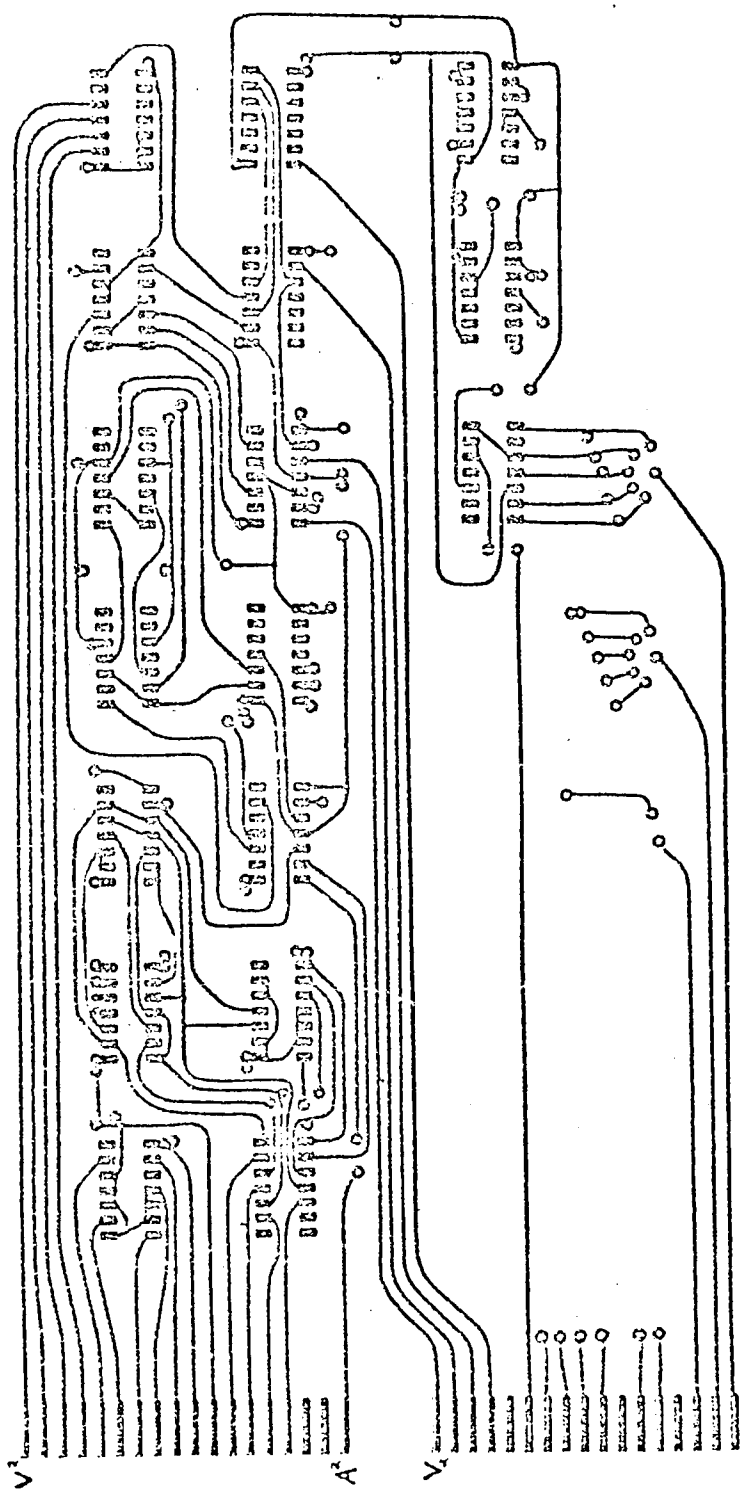


Figure 13. Printed Circuit of the Control Board.

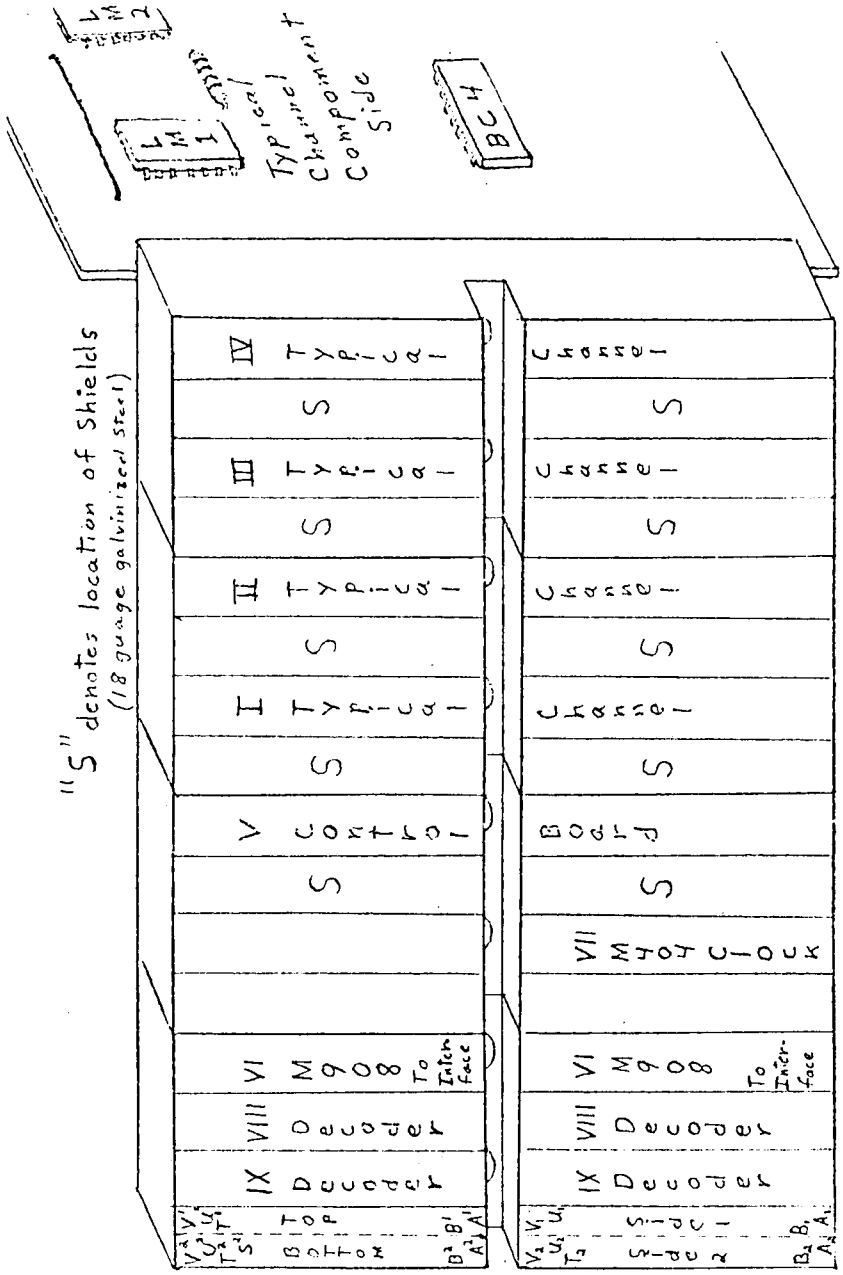


Figure 14. Relative Locations of the Backplanes (Looking into the Terminals).

between channels. Galvanized steel was used simply because it was available at the time. Aluminum, copper, or any other metal would serve the same purpose. The control board is on BPV. The data bus cables are on BPVI. The M-404 clock is on BPVII. The interlocking wiring of these sevel boards is given in terms of their respective pin-to-pin connections in Appendix C. They are also shown on the schematic in the Pocket.

The power supplies used in testing of the prototype described herein would not be used in the actual construction of the system for general usage, since in building the prototype, two Wanlass Electric Company, Model No. Maverick II variable power supplies were used. These are relatively large pieces laboratory test equipment. It is suggested instead that power supplies with specifications comparable to the Analog Devices Models 925 and 922 be used for the ±15 volt and +5 volt power supplies respectively. They are compact, of high quality and relatively low cost. These ratings are given in Appendix A, Data Sheet 3. In wiring in the power supplies, it is important to tie all ground points on the backplane and the power supplies to a single common point rather than "daisy chaining" them in order to avoid ground loops. This point is denoted on the schematic in the Pocket by a circumscribed star drawn near the power supplies. Physically, it should be located as close to them as possible.

CHAPTER V

CALIBRATION AND BENCH TESTING

Tuning the Analog Section

1. Ground all channel input terminals U^2 on BPI through BPIV.
2. Adjust all trim-pots T1 through T9 to about midway on all channels. As these are 20 turn potentiometers, this means 10 turns from either end. Turn switch S1 to the fully counterclockwise position (maximum gain on amplifier LM7), and switch on the +5V and ±15V power supplies.
3. Turn the external reset ON, by placing ±5 VDC on terminal S_2 on backplane BPV.
4. Choose a channel and zero the output of amplifier LM1 using trim-pot T1. This output is at calibration point 1(CP1) on resistor R2 (see Figure 10, page 32).
5. If a dual trace oscilloscope is available, connect one of the scope channels to CP2 and the other to CP3. Place the scope in the "ADD" mode and zero amplifier LM2 using trim-pot T2. The reason for taking this approach is that there will always be a small offset voltage between CP2 and CP3 due to the diode resistance. Refer to Figure 4, page 13, for the schematic of this. If a dual trace scope is not available, adjust T2 until the voltages at CP2 and CP3 are offset equally about zero.
6. Now zero isolation amplifiers LM3 and LM4 using trim-pots T4 and T5, thereby compensating for the diode effect in the previous stage. These outputs are found at CP4 and CP5 respectively.

7. Zero the output of summing amplifier LM5 (output is at CP6) using T5. Do the same for amplifier LM7 using T7 having an output at CP7.
8. There is a small transition region (<20 mv) in the comparator LM8, and if its inputs (the outputs of amplifiers LM6 and LM7) are within that region, the comparator will go into a state of oscillation. For this reason, the dc offset of amplifier LM6 must always be set between -20 milli-volts and -15 volts. This is V_{offset} referred to in Chapter III, page 11, which implies that -20 mv is inherently the minimum fixed discrimination level. Keeping this in mind, attach the oscilloscope to CP8 and adjust trim-pot T6 until the desired offset is obtained. A range of -50 mv to -10 volts is suggested in order to avoid possible drifing into the transition region on the one end, and the non-linear amplifier region on the other.
9. Repeat Steps 4 through 8 for the other three channels.

Tuning the Digital Section

In the preceding section, no special equipment was specified as being absolutely necessary, although it was assumed that at least a voltmeter was available. This section, however, requires the use of at least a single-trace oscilloscope, with a dual-trace scope being preferable, and signal generator having pulsed output capabilities. Proceed as follows.

1. Make sure that Step 3 of the preceding section has been completed and that the external reset is ON, that is +5VDC

on terminal S_2 of BPV. Turn switch S1 fully clockwise for minimum gain on amplifier LM7.

2. Choose any channel and remove the ground connection from the input terminal U^2 on the appropriate backplane. Connect the pulsed output of the signal generator to CP10 at resistor R1 in order to bypass the capacitive coupling at the channel input, and set the generator, to pulse zero to 1.0 volts at 0.5 KHz.
3. Monitor pin 8 of one-shot DM3 (see Figure 6, page 19) and adjust trim-pot T8 until the pulse width is 1.0 msec.
4. Adjust trim-pot T9 until the output of one-shot DM4 at pin 8 has a pulse width of 1.1 msec.
5. Reground the channel input and repeat Steps 1 through 4 for the other three channels.

Bench Testing

In order to test the system under controlled conditions, the circuit in Figure 15 was designed with the help of J. T. Smith of the Nuclear Engineering Department at The University of Tennessee. It consists of seven DM8601 monostable multivibrators, or "one-shots," each having an individual time constant τ. The last four of these, one-shots 1sa through 1sd, each control one of four dual level voltage divider circuits which operate as follows. If the output of the signal generator is v_s, then when any transistor Q_x is conducting the output signal v_x across R_{x3} is given by the following equation.*

*Subscript x is a, b, c, or d depending on the designation of the transistor to which they are connected.

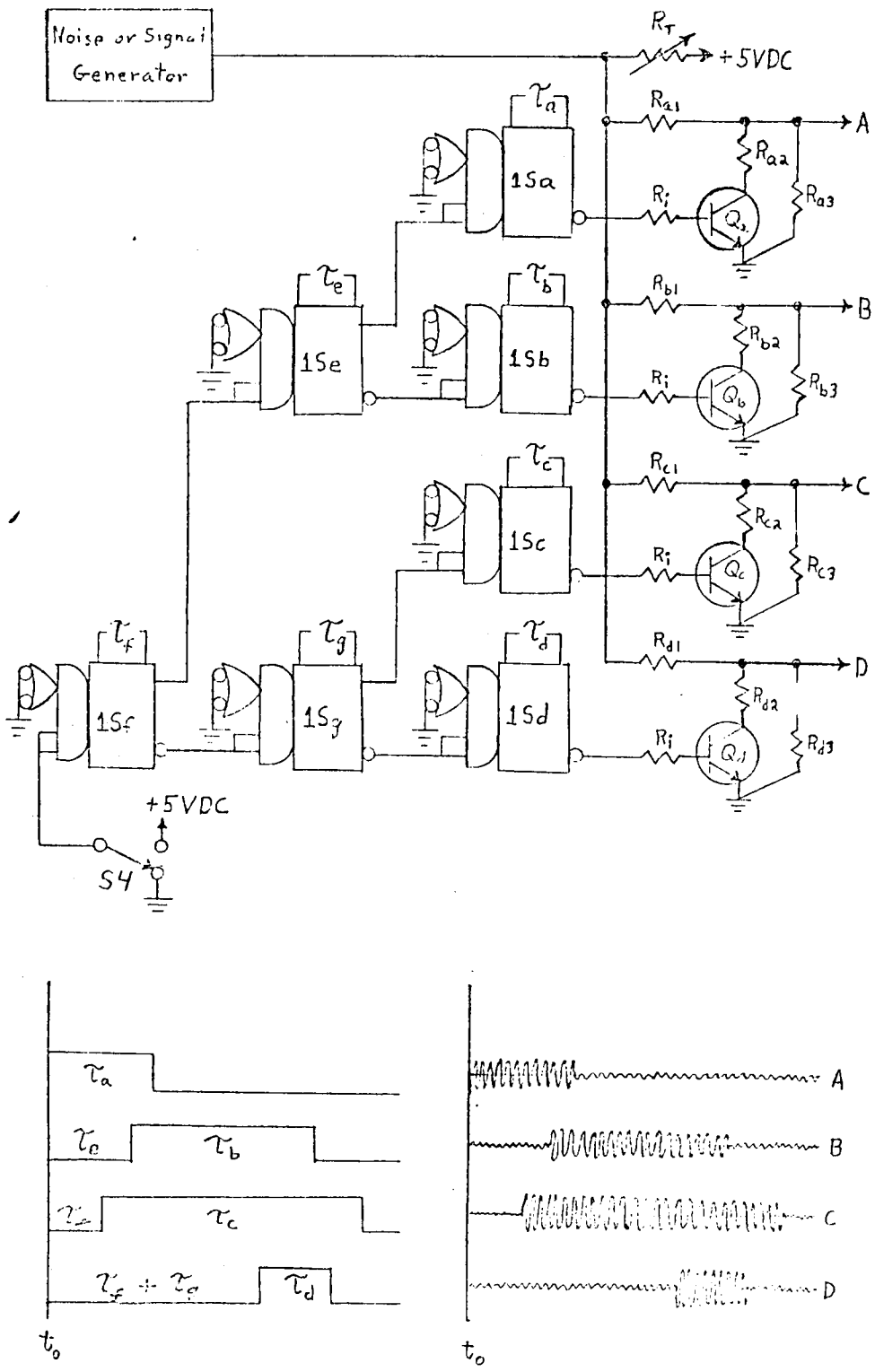


Figure 15. Test Circuit and Associated Output Signals.

$$v_x = \frac{v_s}{1 + \frac{R_{x1}(R_{x2}+R_{x3})}{R_{x2}\,R_{x3}}} \cdot \qquad (5.1)$$

When Q_x is not conducting the signal v_x across R_{x3} is

$$v_x = \frac{v_s}{1 + \frac{R_{x1}}{R_{x3}}} \cdot \qquad (5.2)$$

Now, here is how it works. Prior to some time t_o, switch S4 is grounded and all of the one-shots (1sa through 1sg) are in an "idling mode" meaning that their outputs at pin 6 are all high (+5VDC). Under these conditions, the transistors are conducting so that Equation (5.1) defines the voltage division between the signal generator and outputs at points A, B, C, and D. Now at time t_o, switch S4 is set to the +5VDC position. Immediately, the output states of one-shots 1sf, 1se, and 1sa are reversed causing transistor Q_a to be reverse biased. This removes R_{a2} from the voltage divider circuit causing the output at point A to increase to the level defined by Equation (5.2) for a period of τ_a seconds. After τ_a seconds, the output of one-shot 1sa returns to its original state causing transistor Q_a to conduct again, and the output at point A is returned to its original level. At time $t_o + \tau_e$, the output of one-shot 1se at pin 6 goes high reversing the output of one-shot 1sb. This causes the signal output at point B to increase for τ_b seconds in accordance with the same senerio written for the

output at point A. At $t_o + \tau_f$, the output of one-shot 1sf at pin 6 goes high reversing the output states of one-shots 1sg and 1sc so that the output signal at point C is increased for τ_c seconds. At time $t_o + \tau_f + \tau_g$, one-shot 1sd is triggered and the signal at point D increases for τ_d seconds. Notice the flexibility of this circuit. The duration of the pulses τ_a, τ_b, τ_c, and τ_d are totally independent of each other and can be set by choosing the appropriate resistor and capacitor values in accordance with Equation (3.1). A different delay time may also be chosen for each output by varying the values of τ_e, τ_f, and τ_g. The values of R_{x1} and R_{x3} in Equation (5.2) determine the respective magnitudes of the pulses. And, the choice of resistor R_{x2} in conjunction with resistors R_{x1} and R_{x3} in Equation (5.1) determines the individual background levels.

CHAPTER VI

EXPERIMENTATION

In order to simplify the experimentation with the LPM on physical systems, it was decided to use only two channels. This approach relaxed the troubleshooting requirements and lent itself to a clearer picture of what was actually happening without sacrificing any pertinent information concerning the overall system operation. It did require, however, that the "three out of four channels triggered" criterion be modified to "two out of two channels" needed to execute a read data command. Similarly modified were the "all channels stopped," "transient in progress," and "false start" indicators. This was done by jumpering the following terminals on BPV: N_2 to K_2, M_2 to L_2, V^2 to T^2, U^2 to S^2, R^2 to N^2, P^2 to M^2, H^2 to D^2, F^2 to D^2. A quick glance at the circuit diagram in Appendix D reveals that these changes in no way impair the basic operation of the system.

Until now, the discussion of the operation of the system relied upon the implicit assumption that the input signals would be well defined step changes in amplitude similar to the one illustrated in Figure 5b on page16 or to those produced by the circuit diagrammed in Figure 15 on page 41. One finds, however, that nature refuses to deal in such simplistic terms, and even though the test circuit produces very clear-cut, reproduceable results, the user may easily be fooled by the data obtained in practice unless he is aware of

what is actually being measured. This admonition is not to be taken lightly, for wave propagation in solids is a complex phenomenom with at least three major subdivisions which are directly related to the three elastic moduli. As the purpose of this system is the detection and measurement of waves travelling in steel, and since there are numerous types of steel, the following values[7] shall be used for the purpose of discussion. Young's modulus, M_y: 20.10^{10} nt/m^2, Shear modulus, M_s: 8.10^{10} nt/m^2, Bulk modulus, M_b: 16.10^{10} nt/m^2, density, ρ: 8.10^3 Kg/m^3. From these, the velocity of propagation may be computed by $\gamma_x = (M_x/\rho)^{1/2}$. Hence, one would expect to find three waves having the following velocities

γ_y = 5000 m/sec = 16,400 ft/sec

γ_b = 4470 m/sec = 14,700 ft/sec

γ_s = 3160 m/sec = 10,300 ft/sec.

In order to look at this phenomenom in the laboratory, two Endevco Model 2233E accelerometers were tapped into a 21 ft, 2 in I. D. steel water pipe, and placed 6 inches from each end. The pipe was supported in the center and at each accelerometer location on 1" x 1" x 6" blocks of Neopreme. The accelerometers were tied to the inputs of a dual trace storage oscilloscope, and a third accelerometer, which was used to trigger the scope, was attached to the pipe magnetically 5 ft from one of the end accelerometers which shall be arbitrarily designated Acc I. The LPM was connected to the accelerometer outputs, with the discriminator switch S1 set for minimum gain, the timing frequency set at 50 KHz, and V_{offset} = -50 mv. A 31.5 inch, 0.25 inch diameter rod weighing 7.1 ounces was dropped at various heights through a guide tube also located 5 feet from Acc I. The

rod rebound was about 25 percent so that the energy transfer amounted to about 1 in-lb for every 3 inches of height. Figure 16 shows the relationship between the delay times, Δt, recorded by the LPM versus the height at which the rod was dropped. Figure 17 depicts a typical impact as captured by the storage-scope.

Having measured the difference in distance travelled Δd as being 10 feet, and having found three different delay times (Δt = 0.63, 0.98, 1.20 msec), three different velocities may be calculated γ_1 = 15,900 ft/sec, γ_2 = 10,200 ft/sec, and γ_3 = 8,400 ft/sec. As these were the only three wave velocities observed by the LPM or the oscilloscope, it is reasonable to assume that they respectively represent γ_y, γ_b, and γ_s for this specific pipe. Be this the case, their deviation from the theoretical values only serves to point-up the need for some type of physical on-site calibration. And, one should expect this kind of deviation from the theory, as the elastic moduli relate to changes in both the shape and the volume of the material, and these in turn influence how much of the total energy transferred is imparted to each type of wave. These experiments tend to show that the amplitudes of these waves vary by almost one order or magnitude with γ_s being the largest and γ_y the smallest.

The pulse duration times were also measured in this test and the results are given in Figure 18. The apparent lack of precision in this measurement is due to the total lack of filtering of the input signals. Recall that the pulse duration clocks are stopped when the input signal to the comparator falls below the reference level for 1.0 msec, which corresponds to 0.5 KHz at the system input due to rectification. Since the impact will excite frequencies of less than

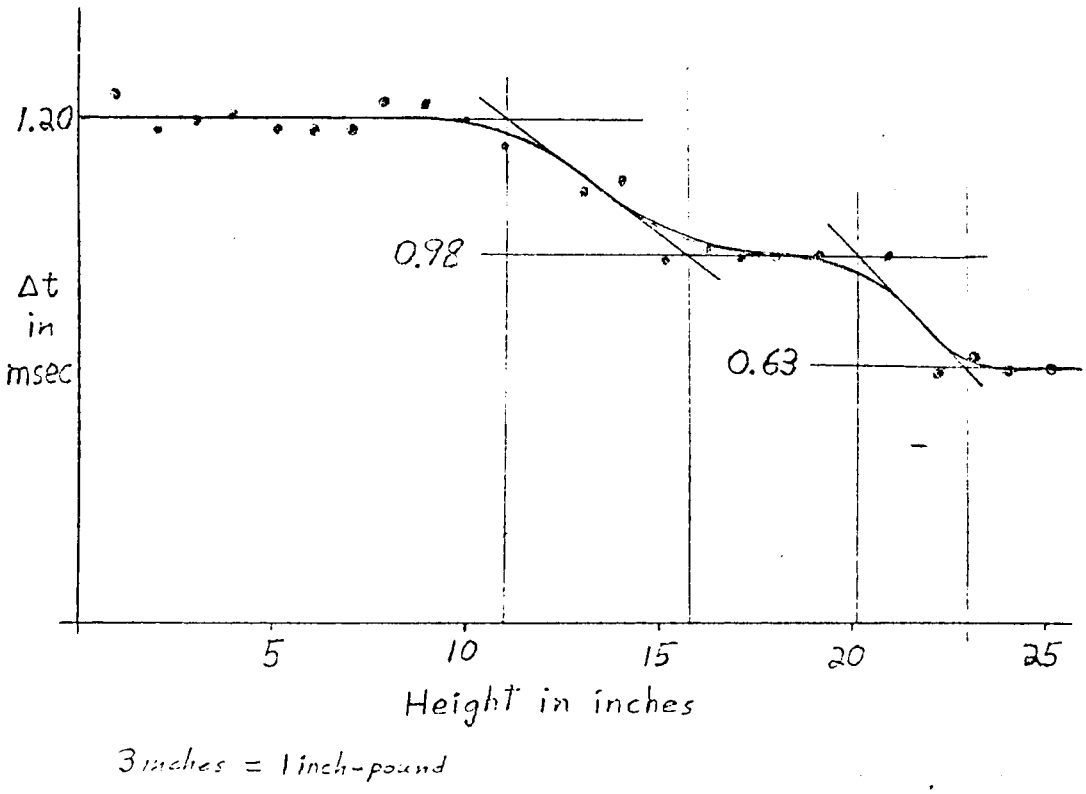


Figure 16. Effect of the Impact Magnitude on the Delay Times.

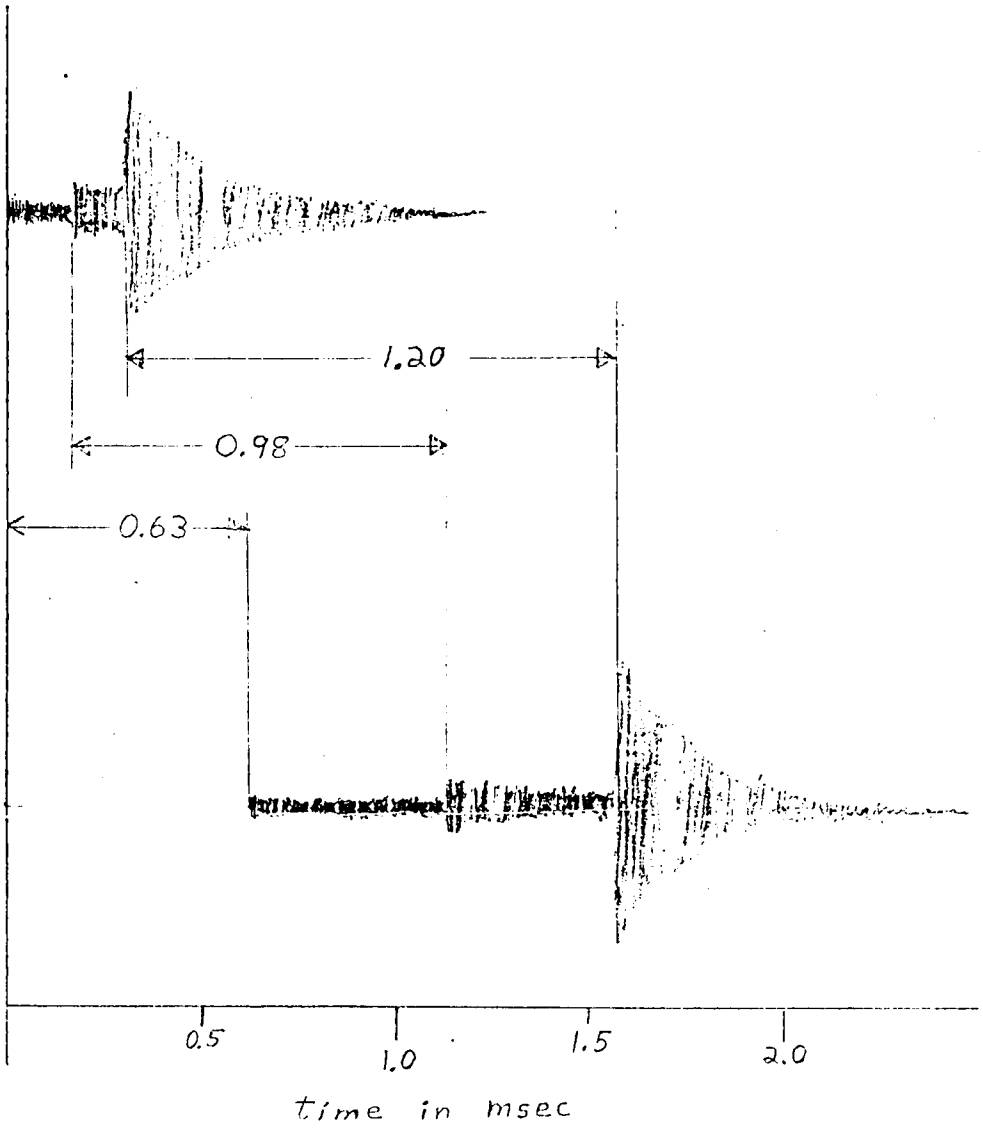


Figure 17. Sound Waves in a Steel Pipe as Viewed on an Oscilloscope.

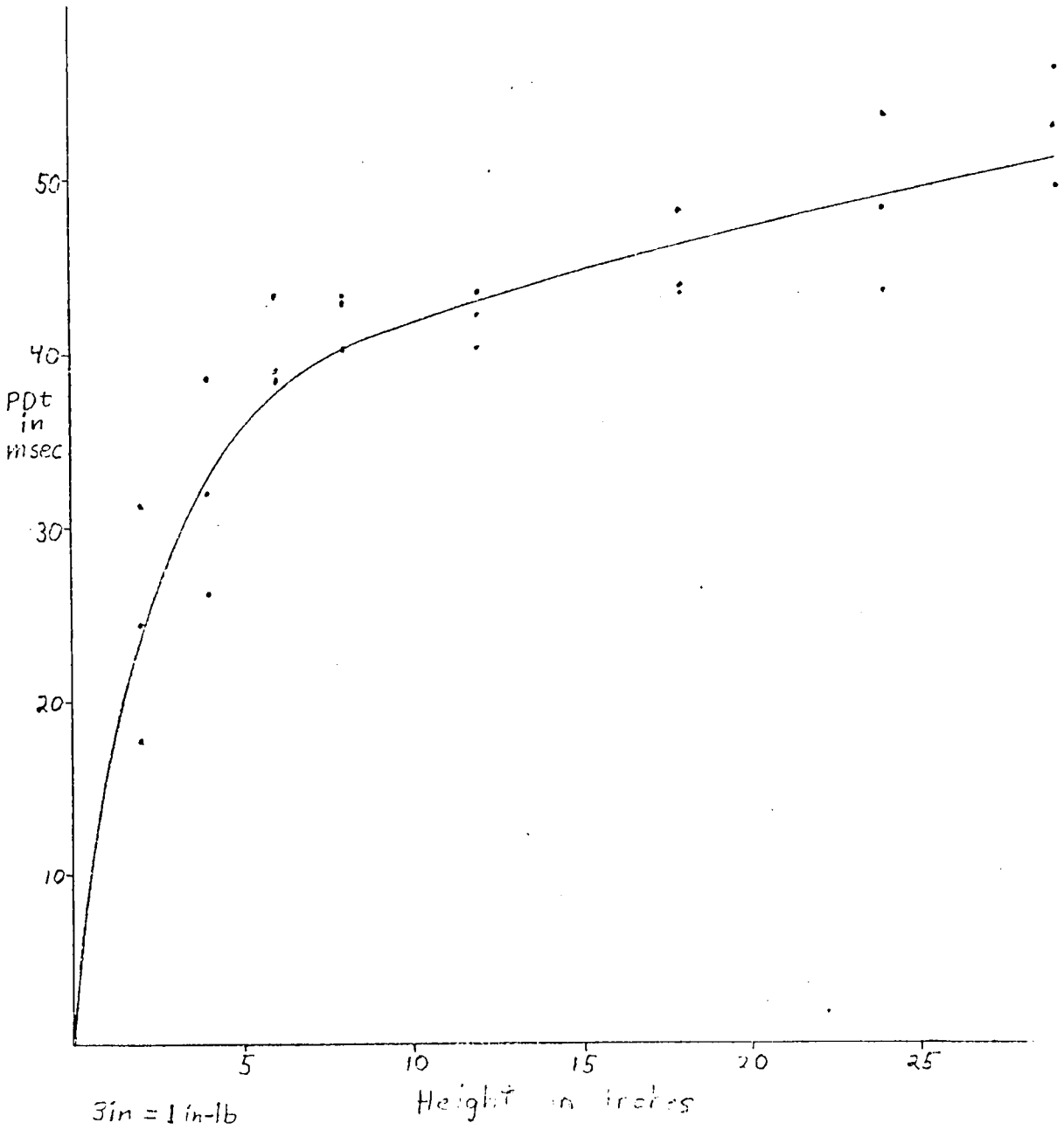


Figure 18. Pulse Duration Time Versus Height.

0.5 KHz, one can never predict when the superpositioning of these will result in a lull of 1.0 msec or more. The user is therefore advised to use some type of high pass filtering if accurate results are to be obtained. The unfiltered results are given here in order to demonstrate the operation of naked system, thereby exposing its weaknesses as well as its strengths. For similar reasons, the discrimination levels have been set at their minima, i.e., lowest gain on LM7 and V_{offset} = -50 mv on LM6.

The next test was to map the length of pipe in terms of the delay times. Immediately, a question arises as to which wave should be measured. More precisely, the question is: Given a set of delay times, how does one know which velocity to use in computing the distance to the point of impact? There are at least two ways. The first method is the iterative one discussed in Chapter II, page 5, where some arbitrary wave velocity γ_0 is chosen and the corresponding "circles" of accoustic equidistance are mapped so as to give the points of intersection. From these, a new velocity, γ_1, is chosen and the procedure repeated until satisfied. The second method is far easier and much more direct. One first looks at the pulse duration time and locates this point on the curve in Figure 18. The energy of the impact found there can now be used in Figure 16 to determine directly which region, and velocity, should be used. Notice that approach is valid even for the two channel system being used in these tests, while there is insufficient information for the former method

For the purpose of illustration, the test pipe was mapped using impacts of 1 in-lbs, meaning that the operative velocity is γ_s, the

largest and slowest of the three. This is chosen because in actual practice, V_{offset} will probably not be set at its minimum, the gain on LM7 may or may not be set at its lowest level, and the system being monitored will most certainly not be quiet. The results of this mapping are given in Figure 19, where Channel I is connected to an accelerometer located 10 feet from the center of the pipe at the position designated +10. Channel II is connected to the other accelerometer located 10 feet from center in the opposite direction at position -10, so that the total span between them is 20 feet.

The three curves given in Figures 16, 18, and 19 only represent the kinds of information that an investigator should have at his disposal when using the monitor. In fact, one would want to have whole families of curves obtained at various discrimination levels, gain settings, and background noise levels, with and without external filtering and other signal conditioners. The permutations are great, but they were meant to be, for the system is designed to be used as an analytical tool, and as such demands a high degree of inherent flexibility.

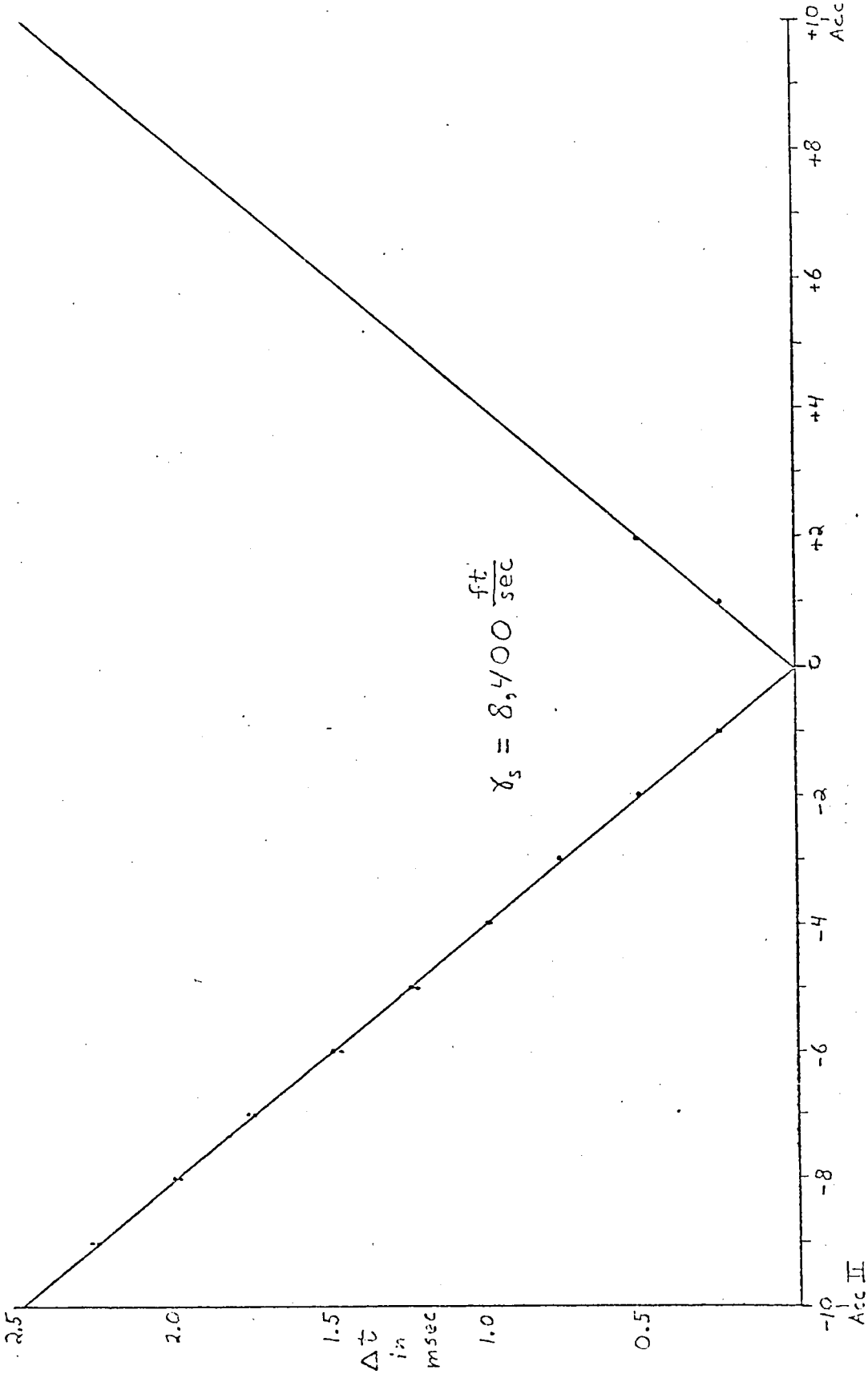


Figure 19. LPM Map of the Test Pipe Δt Versus Position in Feet from Center.

CHAPTER VII

ACCESSORY DECODER

Although the LPM is designed for automatic computer controlled operation, the system would loose much of its commercial and scientific appeal if it relied solely on the availability of a multi-thousand dollar minicomputer. In the interest of relieving this constraint, a low cost 8-bit binary to 7-segment decoder was designed for direct data acquisition. The physical layout of these decoder boards along with the backplane and 7-segment connections is given in Figure 20. The printed circuit is shown in Figure 21.

For manual operation, a reset command is issued by setting terminal S_2 on BPV high (+5V). The status of the system is obtained by connecting an 820 ohm resistor in series with low power LED from terminal F_2 on BPV to ground. A lit lamp tells the operator to read the data and reset the system.

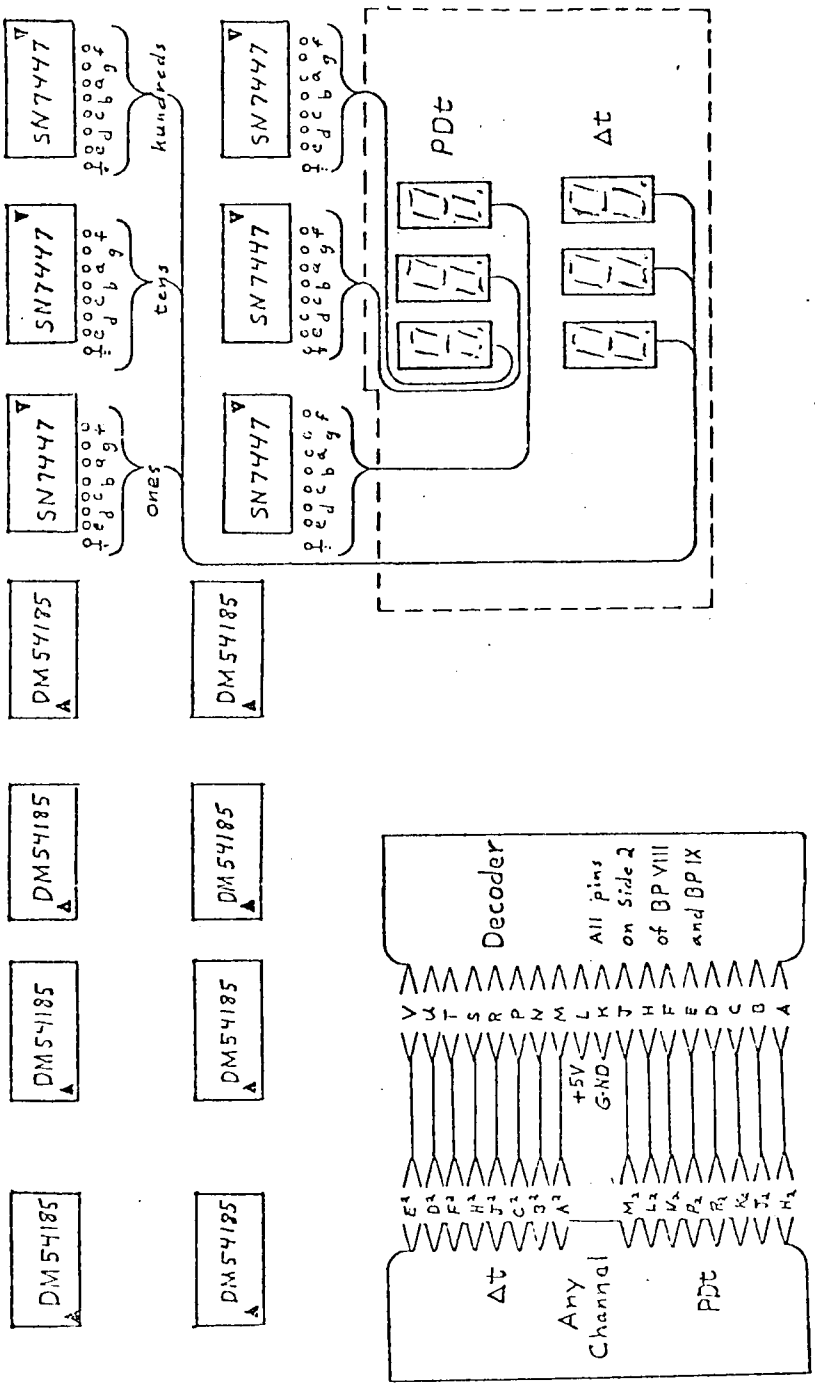
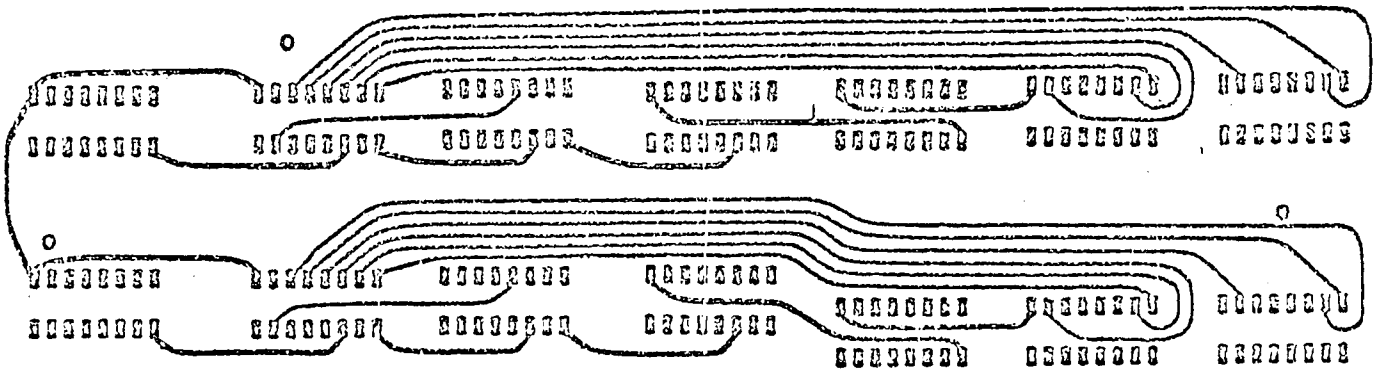
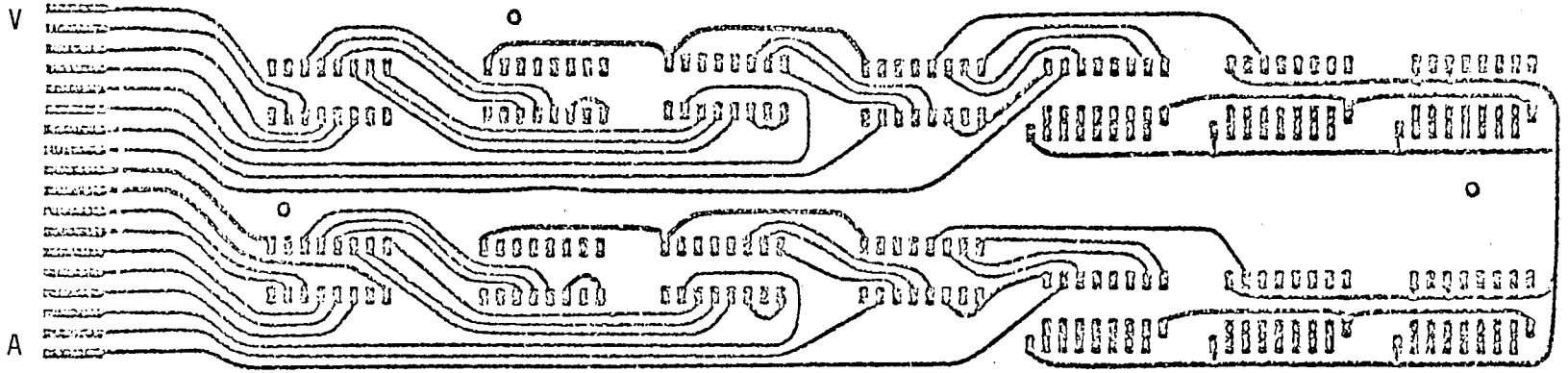


Figure 20. Physical Layout of the Dual 8-bit Decoder.



Top Side Circuitry



Contacts on Side 2

Bottom Side Circuitry

Figure 21. Decoder Printed Circuit as Viewed from the Component Side.

CHAPTER VIII

COST ANALYSIS

A summary of the cost of the components found in Appendix B is given in Table 1. This list, however, can ge misleading because it is only complete in terms of the minimum component requirements. Notably excluded are the packaging and mounting requirements. The major considerations in this respect depend largely on how the system is to be used, and what means of data handling is to be employed. If the data is to be handled by a minicomputer having a 6 inch space available for a 19 inch rack, nothing more than the mounting screws are required, and the decoders become superfluous. If however, all of the data is to be read directly, then the design of the cabinet should be in keeping with the following parameters: metal construction for strength and Gaussian shielding, portability, ease in accessing the switches and controls, minimum disassembly requirements for troubleshooting and part replacement, adequate ventillation for temperature control, clearly visible readouts, and easthetically pleasing overall appearance. Depending on whether ones major emphasis is on the first few points or the last, the design may be as simple as a $20.00 aluminum box, or as elaborate as one's imagination in view of the marketing demands. In the author's opinion, a frugally purchased $150.00 worth of materials should be sufficient.[6] As a third option, both means of data handling may be desirable. The most reasonable approach to this would be to design the enclosure as if the system were totally portable and then allow

TABLE 1

COST SUMMARY OF MATERIALS FOUND IN APPENDIX B

Basic Loose Parts Monitor	
Resistors	16.80
Trim Pots	82.80
Capacitors	25.20
ICS & Diodes	205.85
Switches	32.00
Power Supplies and Clock	308.00
Hardware	90.40
Basic LPM Total	761.05
Computer Interfacing	
Interface, cables, and connectors	280.00
Decoder	
ISc, LEDs, cables and connectors	293.85
Test Circuit	
Circuit components	17.90
Power Supply	41.00
Hardware	16.00
Test Circuit Total	75.00

space for the inclusion of the computer interfacing boards and cables, to which end only a few holes and slots would be necessary. Price it at $50.00 in accordance with previous estimates. The cost of materials, plus 10 percent wastage, may now be estimated for the three types of systems.

1. Computer Data Handling Alone: $1145
2. Direct Data Handling Alone: $1325
3. Both Data Options: $1688.

The labor cost is a large, and widely varying parameter in terms of dollars, so the cost of construction shall be estimated in terms of man hours required on the basis of the author's experience. The drilling of holes, and the placement and soldering of components for the basic system, excluding all data handling equipment, requires 38 man hours. The similar construction of the decoders with LED's, etc. takes 7 man hours. The wiring of the cables for the computer interfacing takes 4 man hours. Cabinet construction gets 1 man hour. Quality control, testing, repairs, retesting and final calibration respectively require 3, 1, 2, 1, and 3 man hours for a total of 10 and 60 percent more for both data handling options. Hence, the labor costs for the above mentioned systems are:

1. Computer Data Handling Alone: 48 man hours
2. Direct Data Handling Alone: 56 man hours
3. Both Data Options: 66 man hours.

In order to get a feel for the magnitude of this, figure that the overhead and labor cost of production alone at a modest $25.00/man hour, then the cost to produce one unit becomes $2345, $2725, $3338

respectively. If the more nebulous costs of marketing, sales, shipping, user product information, warranties, etc. are set equal to the costs of production and a 5 percent profit included, the total cost of the three systems becomes $4925, $5723, and $7010.

The cost of materials for the Test Circuit in Figure 15, page 41, is also listed in Appendix B totalling $75. Adding to this 10 percent wastage and 4 man hours of labor at an overhead cost of $25 per man hour, the production cost becomes $182.50. When doubled as before and a 5 percent profit added, the total cost becomes $383.25. An additional $100 would approximate the total cost for making the circuit flexible by adding breadboarding capabilities bringing the total to $483.25 for the test circuit alone.

CHAPTER IX

WHICH WAY FROM HERE

In all of the previous sections, the system has been discussed in terms of how it is designed; rather than how it should be designed. This system clearly does what it was meant to do, but it could do it more efficiently. One blatant example of electronic over-kill is found in the "three-out-of-four channels must contain data" circuitry on the control board.

The mental logic went like this: if three out of four channels are to contain informative data, then at least three channels must be triggered within the time required for the sound in the medium to traverse the maximum distance between any two accelerometers. The circuitry was designed accordingly. First a counter was needed, so binary counters BC5 and BC6 were added. Then the problem of starting the counter arose, but NOR-gate, DM14 took care of that. Next, the counting had to be stopped if three channels triggered. The quad-3 input AND-OR-Invert circuit formed by DM15 and two AND gates in DM13 coupled with one of the J-K flip-flops in DM16 combined to perform this function. The five inverters in DM12 were necessary in order to get the proper input states to the control circuits. NAND-gate DM17 had to be included in order to provide a pulse that would latch the other J-K flip-flop in DM16. In all 14 individual pieces of digital logic occupying eight integrated circuits were consumed by this bestial circuit alone.

If the logical converse of the original criterion had been expressed, that is, "two out of four channels cannot contain worthless data," the digital result might have been and should have been quite different. It is therefore recommended that the previously described circuitry be replaced by a single Hex-2 input AND-OR Invert-gate (Hex-2AOI). The output of this should be connected to pin 10 on DM13 and pin 5 on DM16. The inputs to it should be the outputs of inverter DM6, pin 6 from each channel. These outputs will form six permutations if taken two at a time which exactly matches the number of 2-input AND gates in the Hex-2AOI. Now the circuit works as follows. When any two Δt counters become full, meaning that the channel did not detect a transient, their 8-input NAND gate outputs go low. These outputs are inverted by inverter DM6 and fed into the Hex-2AOI causing its output to also go low. This constitutes a reset command by latching the output of flip-flop DM16 at pin 5 high, and prevents the issuance of a read data command by setting a low potential on pin 10 of DM13.

Another area of component optimization lies in the analog section where some of the trim-pots could be elminiated such as trim-pots T1, T2, and T5. A question also arises concerning the value of using an FET op-amp to achieve a high input impedence when the input high-pass filter has a 1 Mega-ohm resistor in it going to ground.

The hardware is another area that could use improvement. For example, the control and channel boards are single sided and of

finolic construction. Finolic boards not only have a low cost, they have a short lifetime. The lifetime of glass-epoxy boards justifies their increased cost. Furthermore, by using double sided boards, the labor cost of cutting, stripping, and soldering jumper wires could be greatly reduced and the printed circuit could be designed so that the board width conformed with the standard DEC dimensions for their double width modules (DEC width: 5 3/16 in, LPM width 6 in).

Improvements in these areas and others will undoubtedly be forthcoming in future designs, just as this system is an improvement upon the accelerometer-to-switch-to-speaker system that precipitated the development of this paper. In fact, the time for scrapping much of this loose parts monitor and replacing it with one better may be now.

LIST OF REFERENCES

LIST OF REFERENCES

1. Digital Logic Handbook, 1973, Prepared by the Logic Products Group, Digital Equipment Corporation. .

2. Product Guide to Analog Devices, Analog Devices, Inc., 1975.

3. Linear Integrated Circuits, National Semiconductor Corporation, 1973.

4. Digital Integrated Circuits, National Semiconductor Corporation, 1973.

5. Fairchild Semiconductor Integrated Circuit Data Catalog, Fairchild Semiconductor Division, Fairchild Camera and Instrument Corporation, 1970.

6. Allied Engineering Manual and Purchasing Guide, Allied Electronics Division, Tandy Corporation, 1975.

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APPENDIXES

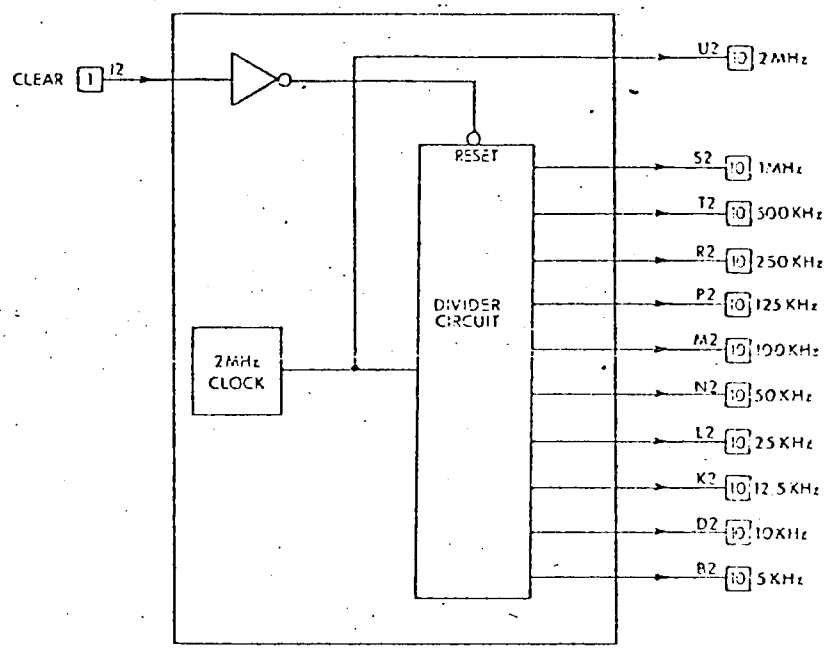
APPENDIX A

ELECTRONIC DATA SHEETS

Data Sheet 1. M-404 Crystal Control Digital Clock.[1]

M404 CRYSTAL CLOCK	TIME RELATED M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	535	A2
GND		C2, T1

The M404 clock contains a 2 MHz crystal oscillator and frequency dividers.

A HIGH on the CLEAR input clears the frequency divider and all outputs go LOW except the 2 MHz output, which is not affected.

SPECIFICATIONS
Accuracy: Maximum error from specified output frequency is 0.01% between 0 degrees C and +55 degrees C.

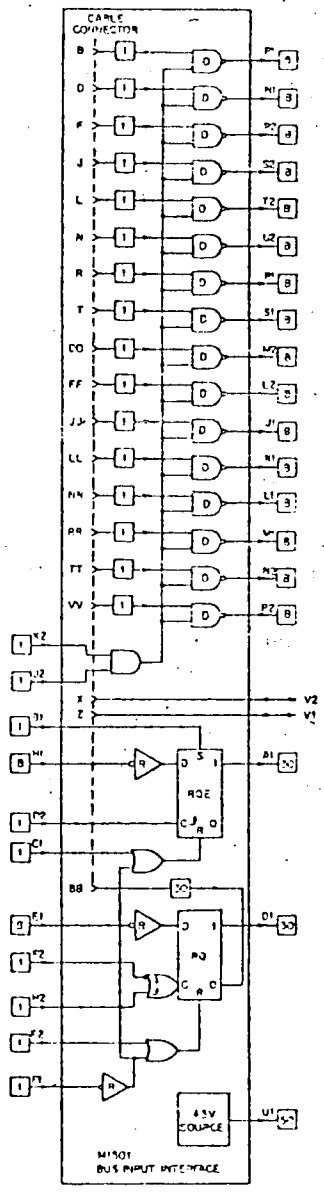
Data Sheet 2. M-1501 Bus Input Interface.[1]

M1501 BUS INPUT INTERFACE	UNIBUS/ OMNIBUS
	M SERIES

Length: Extended
Height: Single
Width: Single

Price:

$50



Volts	Power mA (max.)	Pins
+5	300	A2
GND		C2, T1

The M1501 contains 16 bus drivers for interfacing parallel input data to a bidirectional data bus structure such as the PDP-11 UNIBUS or the PDP-8/e OMNIBUS. The module includes two control flags that can be used for interrupt request and enable. Data inputs from an external device enter a 40-pin flat cable connector mounted on the module itself. All inputs are diode-clamped to ground and +5 volts.

APPLICATIONS

This module is designed for use in bus expansion hardware such as:

BB11 Blank System Unit (PDP-11 UNIBUS)
H9190 Bus Expander (PDP-8/e OMNIBUS)

Expandability: In PDP-11 applications, up to four M1501 modules (64 bits) can be controlled by one M105 Address Selector module, one M7820 Interrupt Control module, and one M1500 Bus Gates module. Similarly, several M1501's can be combined for multiple word input to a PDP-8/e by using an M1510 Bus Device Selector module.

Restrictions: The module is electrically, but not mechanically, compatible with the PDP-8/e OMNIBUS. Do not plug the module directly into the OMNIBUS. OMNIBUS signals may be connected to appropriate module pins by backplane wiring.

FUNCTIONS

Input from Cable: Data is gated from the input connector to the bus when both loading inputs (AK2, AJ2) are HIGH.

Send/Receive Control Signal: Two additional lines are provided from the cable connector (Pins X and Z) to the module to allow communications between the device and the computer.

Flags: A request flag (RE) and a request enable flag (RQE) are included on the M1501. Both flags can be cleared on start-up directly from the GENERAL CLEAR bus line. Both flag clock inputs are transition sensitive. The data input to each flag is buffered by a bus receiver; thus, status data can be entered directly from a bus line if desired. The request enable flag clock input responds to a HIGH going transition. The request flag has an input that is sensitive to a LOW going transition and an input that is sensitive to a HIGH going transition. (Whichever input is not used should be connected to the proper logic level to unassert it.) The user is given the maximum degree of freedom to use the request enable flag as a D flop or as an RS flop because all inputs are accessible.

The output of each flag is fully buffered to protect the flag data as well as to provide high output drive.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
40-Pin Connector Inputs	Bus Data Outputs	50
Flag Clock Inputs	Flag Outputs	75

Data Sheet 3. +5, and ±15 Volt Power Supplies.(2)

900 SERIES: GENERAL PURPOSE POWER SUPPLIES

The 900 series power supplies from Analog Devices have been widely accepted by designers as industry standards for reliability and performance. Useful in industrial and laboratory applications, these companion products to op amps are capable of delivering clean, well regulated power to IC and discrete op amps, digital converter products, and to transducer elements. These modular devices are available in molded plastic, aluminum and thermal-barrier packages. Most modules can be soldered directly into printed circuit boards or can be plugged into an optional mating socket.

Plastic molded cases are used on designs capable of dissipating up to 3 watts. Low thermal resistance aluminum cases are employed on supplies which dissipate between 3-6 watts. Supplies that can provide output power of over 10 watts are packaged in "thermal barrier" housings. The "thermal barrier" design isolates the heat generating components from those that are heat sensitive and allows high power devices, like the 922 and 925, to fit into standard 3.50" x 2.50" profiles.

All designs are line operated. International voltage ratings are offered. Available models feature short circuit protection and current limiting (with over-voltage protection on 903, 905, 922). Current output is ±25mA to ±350mA for dual outputs and 250mA to 2 amps for single outputs. To service its customers, Analog Devices maintains an off-the-shelf stock for immediate delivery. Substantial OEM discounts are available.

SPECIFICATIONS (Typical @ +25°C and 115VAC unless otherwise noted)

	Output Current[2]	Model	Output Error (Max)	Regulation 105 to 125 VAC (Max)	Regulation Load, 0 to 100% (Max)	Temperature Coefficient (/°C)	Ripple & Noise RMS (Max)	Options[4]	Package	Price (1-9)	Price (10-24)
±15V	@ 350mA	925	±1%	0.02%	0.02%	0.015%	0.5mV	E, F, H	H-1	$99	$93
	@ 200mA	920	+300mV -0mV	0.02%	0.02%	0.015% 0.015%	0.5mV	E, F, H	HA-1	$72	$65
	@ 200mA	970	±2%	0.05%	0.05%	0.015%	1mV	E, F, H	J	$79	$72
	@ 100mA	902	+300mV -0mV	0.02%	0.02%	0.015%	0.5mV	E, F, H, I	HA-1	$51	$49
	@ 100mA	902-2	+300mV -0mV	0.02%	0.02%	0.015%	0.5mV	E, F, H, I	HB-1	$51	$49
	@ 100mA	952	±2%	0.05%	0.05%	0.015%	1mV	E, F, H	J	$58	$56
	@ 50mA	904	+200mV -0mV	0.02%	0.02%	0.015%	0.5mV	E, F, H, I	HB-1	$41	$40
	@ 25mA	915	±1%	0.2%	0.2%	0.015%	1mV	E, F, H, I	HB-1	$24	$23
+5V[3]	@ 2000mA	922	±1%	0.02%	0.05%	0.015%	1mV	E, F, H	H-1	$89	$83
	@ 1000mA	905	±1%	0.02%	0.05%	0.015%	1mV	E, F, H	HA-1	$72	$69
	@ 1000mA	955	±2%	0.05%	0.15%	0.015%	2mV	E, F, H	J	$79	$76

Data Sheet 4. AD351J Comparator.[2]

MODEL AD351 J/K/S

Model AD351 is a high performance monolithic comparator which includes additional front end circuitry, usually added externally with other IC designs, to achieve low bias and offset currents with high input impedance. Although its speed is modestly reduced by incorporating these user conveniences, AD351 fulfills the need for a high speed comparator for a wide range of applications including zero-crossing detectors, threshold detectors and window comparators. Typical specifications include 84dB gain, 250nA bias, CMR of 70dB at ±10V and 1 to 7 volt output swing (400ns switch time) with 10kΩ output impedance.

Gain, V/V, min	15,000
Rated Output Voltage Levels, min	+7V @ no load to +1V@2mA
Input Bias Current, max Avg. vs. Temp	250nA 4nA/°C
Input Offset Voltage Initial, 25°C, (adj. to zero), max vs. Temp, max	 ±6mV 20μV/°C
Input Impedance Differential Common Mode	 10MΩ//4pF 10MΩ//4pF
Input Voltage Range Safe Differential Voltage Common Mode Rejection @ ±10V Common Mode Voltage, min	 ±30V 70dB min (5V output) ±10V
Response Time Switching (0 to 5V) Output Delay	 400ns 250ns (2.5V output)
Power Supply Positive Voltage (VDC) Negative Voltage (VDC) Temperature Range	 +(7 to 18)V@2.5mA -18V max@0.5mA 0 to +70°C | 0 to +70°C | -55 to +125°C
Package Outline Case Dimensions	 TO-100

Data Sheet 5. LH0042C Low Cost FET Operational Amplifier.(3)

Operational Amplifiers

LH0022/LH0022C* high performance FET op amp
LH0042/LH0042C low cost FET op amp
LH0052/LH0052C precision FET op amp

general description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 200 microvolts maximum offset and 5 μV/°C offset drift. Input offset current is less than 100 femtoamps at room temperature and 100 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with neglible effect in offset drift or CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the −55°C to +125°C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the −25°C to +85°C temperature range.

features

- Low input offset current—100 femtoamps max. (LH0052)
- Low input offset drift—5μV/°C max (LH0052)
- Low input offset voltage—100 microvolts-typ.
- High open loop gain—100 dB typ.
- Excellent slew rate—3.0 V/μs typ.
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

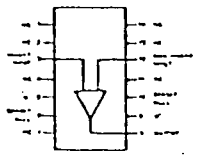
The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

Special electrical parameter selection and custom built circuits are available on special request.

For additional application information and information on other National operational amplifiers, see *Available Linear Applications Literature.*

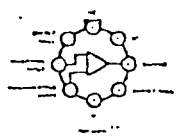
schematic and connection diagrams

Dual-In-Line Package



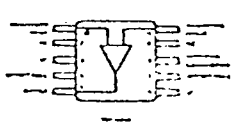
Order Number LH0022D or LH0022CD or LH0042D or LH0042CD or LH0052D or LH0052CD
See Package 1

Metal Can Package

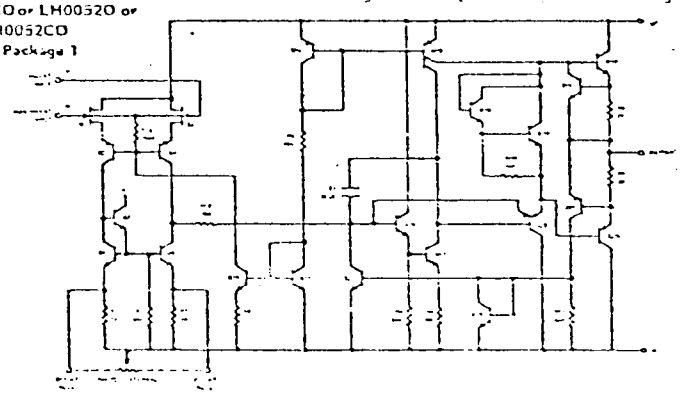


Order Number LH0022H or LH0022CH or LH0042H or LH0042CH or LH0052H or LH0052CH
See Package 11

Flat Package



Order Number LH0022F or LH0022CF or LH0042F or LH0042CF
See Package 3



dc electrical characteristics for LH0042/LH0042C

(T_A = 25°C, V_S = ±15V, unless otherwise specified)

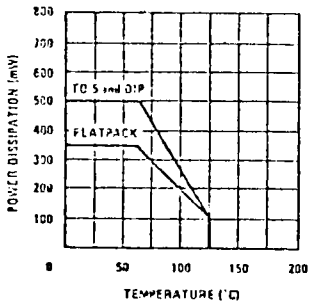
PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0042			LH0042C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\,k\Omega$; $\pm5V \leq V_S \leq 20V$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\,k\Omega$		5			10		µV/°C
Offset Voltage Drift with Time			7			10		µV/week
Input Offset Current			1	5		2	10	pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current			10	25		15	50	pA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$, V_{IN} = ±10V	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$, $\pm5V \leq V_S \leq \pm15V$	70	86		70	80		dB
Large Signal Voltage Gain	R_L = 1 kΩ, V_{OUT} = ±10V	50	150		25	100		V/mV
Output Voltage Swing	R_L = 1 kΩ	±10	±12.5		±10	±12		V
Output Current Swing	V_{OUT} = ±10V	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current			2.5	3.5		2.8	4.0	mA
Power Consumption				105			120	mW

dc electrical characteristics For LH0052/LH0052C (Note 3)

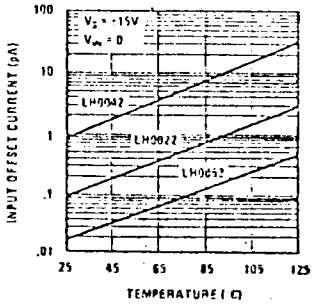
PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0052			LH0052C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\,k\Omega$; V_S = ±15V, T_A = 25°C		0.1	0.5		0.2	1.0	mV
	$R_S \leq 100\,k\Omega$, V_S = ±15V			1.0			1.5	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\,k\Omega$		2	5		5	10	µV/°C
Offset Voltage Drift with Time			2			4		µV/week
Input Offset Current	T_A = 25°C		0.01	0.1		0.02	0.2	pA
				100			100	pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			<0.1			<0.1		pA/week
Input Bias Current	T_A = 25°C		0.5	1.0		1.0	5.0	pA
				500			500	pA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	V_S = ±15V	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$, V_{IN} = ±10V	80	90		76	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$, $\pm5V \leq V_S \leq \pm15V$	80	90		76	90		dB
Large Signal Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10V, V_S = ±15V, T_A = 25°C	100	200		75	160		V/mV
	R_L = 2 kΩ, V_{OUT} = ±10V, V_S = ±15V	50			50			V/mV
Output Voltage Swing	R_L = 1 kΩ, T_A = 25°C V_S = ±15V	±10	±12.5		±10	±12		V
	R_L = 2 kΩ, V_S = ±15V	±10			±10			V
Output Current Swing	V_{OUT} = ±10V, T_A = 25°C	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	V_S = ±15V		3.0	3.5		3.0	3.3	mA
Power Consumption	V_S = ±15V			105			113	mW

typical performance characteristics

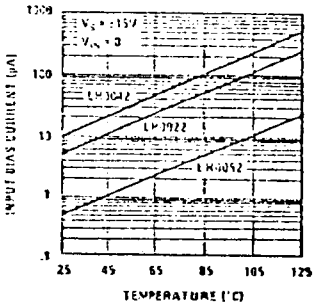
Maximum Power Dissipation



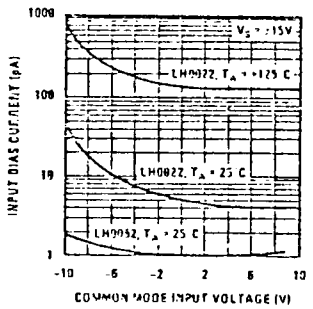
Input Offset Current vs Temperature



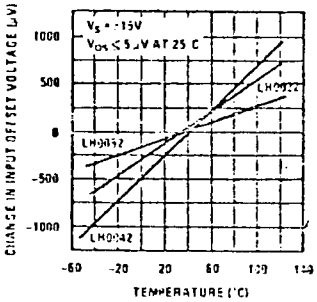
Input Bias Current vs Temperature



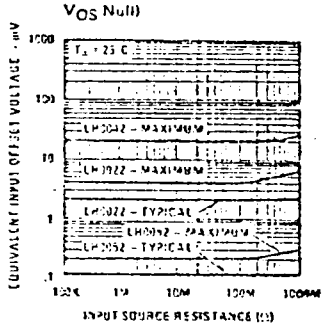
Input Bias Current vs Input Voltage



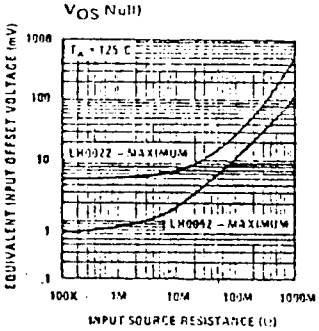
Input Offset Current vs Temperature



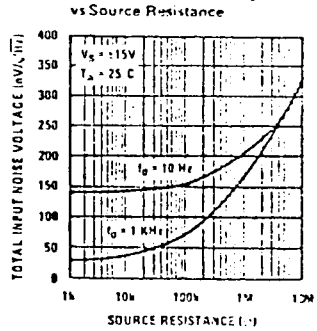
Offset Error (Without V_{OS} Null)



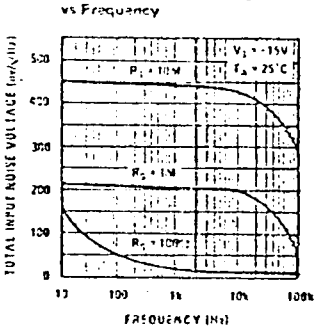
Offset Error (Without V_{OS} Null)



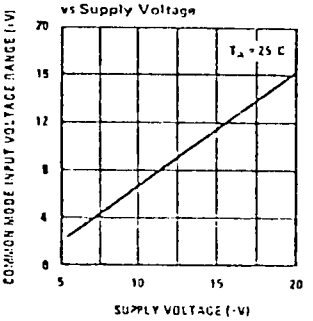
Total Input Noise Voltage* vs Source Resistance



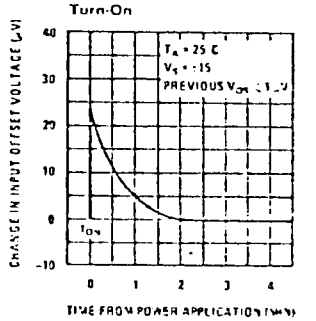
Total Input Noise Voltage* vs Frequency



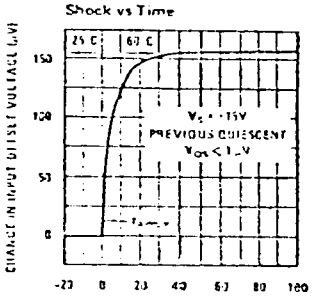
Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On



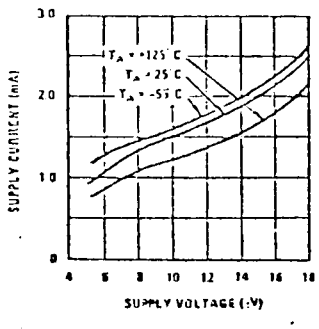
Change in Input Offset Voltage Due to Thermal Shock vs Time



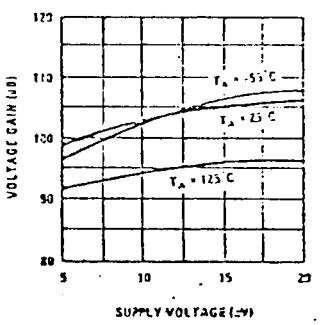
*Noise Voltage Includes Contribution from Source Resistance

typical performance characteristics (con't)

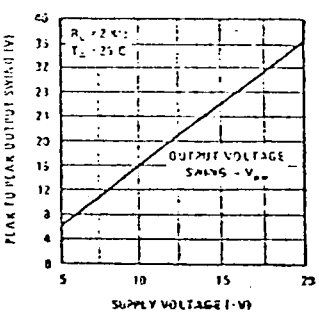
Supply Voltage vs Supply Current



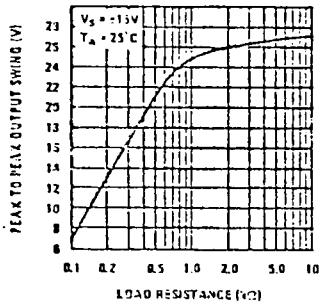
Voltage Gain



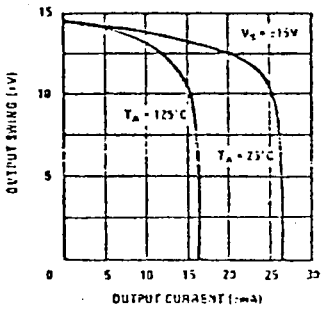
Output Swing vs Supply Voltage



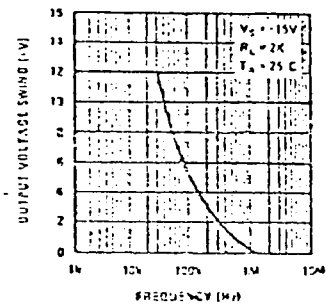
Output Voltage Swing vs Load Resistance



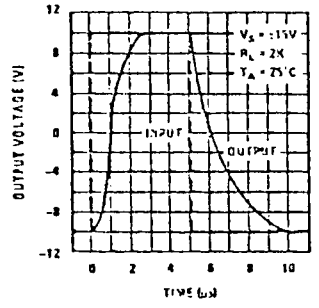
Current Limiting



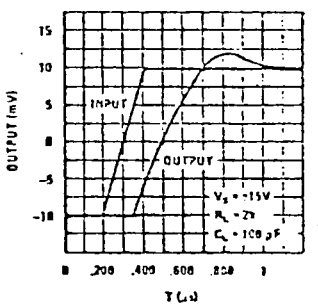
Output Voltage Swing vs Frequency



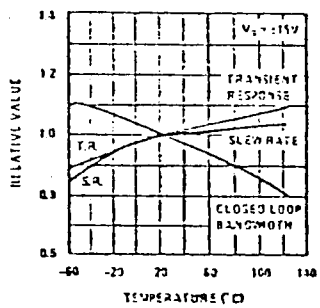
Voltage Follower Large Signal Response



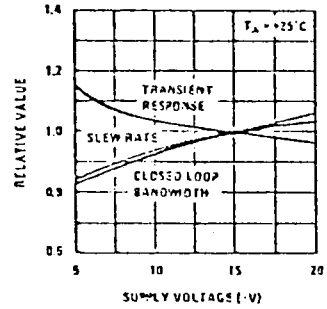
Transient Response



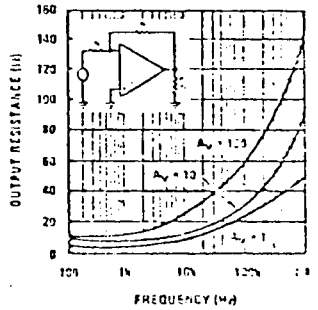
Frequency Characteristics vs Ambient Temperature



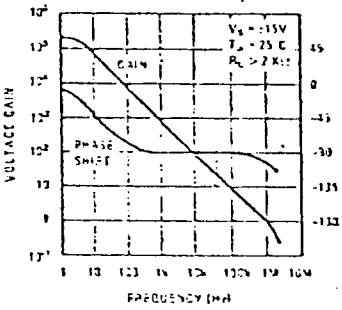
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency



Open Loop Transfer Characteristics vs Frequency



Data Sheet 6. LM741C General Purpose Operational Amplifier.(3)

Operational Amplifiers

LM741/LM741C operational amplifier

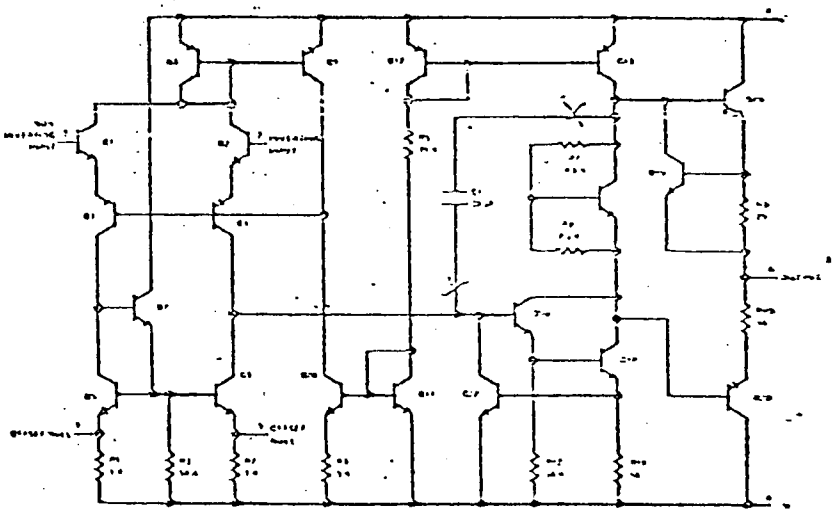
general description

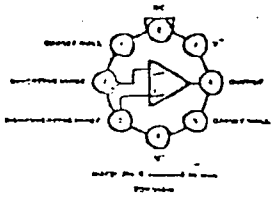
The LM741 and LM741C are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The offset voltage and offset current are guaranteed over the entire common mode range. The amplifiers also offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

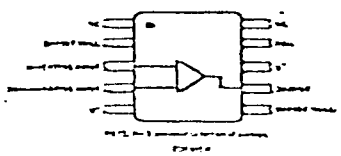
The LM741C is identical to the LM741 except that the LM741C has its performance guaranteed over a 0°C to 70°C temperature range, instead of −55°C to 125°C.

schematic and connection diagrams

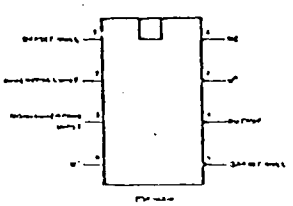




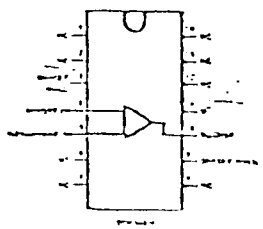
Order Number LM741H or LM741CH
See Package 11



Order Number LM741F
See Package 3



Order Number LM741CN
See Package 20



Order Number
LM741CD or LM741CDX
See Package 1 See Package 12

absolute maximum ratings

Supply Voltage	LM741	±22V
	LM741C	±18V
Power Dissipation (Note 1)		500 mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short Circuit Duration		Indefinite
Operating Temperature Range	LM741	−55°C to 125°C
	LM741C	0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	LM741			LM741C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10k\Omega$		1.0	5.0		1.0	5.0	mV
Input Offset Current	$T_A = 25°C$		30	200		30	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current	$T_A = 25°C$, $V_S = ±15V$		1.7	2.8		1.7	2.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 2k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 2k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = ±15V$, $R_L = 10k\Omega$	±12	±14		±12	±14		V
	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = ±15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	77	96		77	96		dB

Note 1: The maximum junction temperature of the LM741 is 150°C, while that of the LM741C is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to case.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = ±15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM741C, however, all specifications are limited to $0°C \leq T_A \leq 70°C$ and $V_S = ±15V$.

Data Sheet 7. DM8601 Retriggerable Monostable Multivibrator.(4)

Series 9000

DM9601/DM8601 retriggerable monostable multivibrator

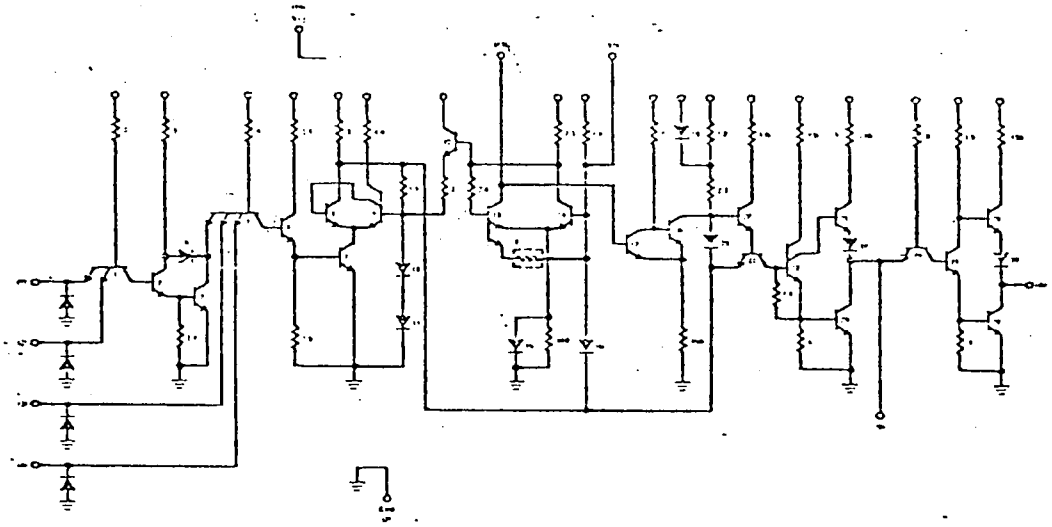
general description

The DM9601/DM8601 is both pin-for-pin and spec-for-spec interchangeable with the 9601 one-shot. Pulse widths range from 50 ns upward depending upon the values of the external R&C used. The retriggerable feature allows for output pulse widths to be extended beyond the normal range attainable with just a resistor and capacitor.

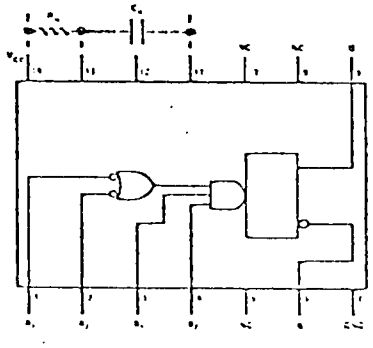
features

- Input Clamping Diodes
- Complementary DC Level Sensitive Inputs
- Flexibility of Operation—Optional Retriggering/Lockout Capability
- DTL/TTL Compatible Logic Levels
- High Speed Operation—Input Repetition Rate > 10 MHz
- Output Pulse Width Range 50 ns to ∞
- Leading or Trailing Edge Triggering
- Complementary Outputs

schematic and connection diagrams



Dual-In-Line and Flat Package



DM8601
absolute maximum ratings

Supply Voltage to Ground	-0.5V to +8.0V
Input Voltage	-0.5V to +5.5V
Voltage Applied to Outputs	-0.5V to +V_{CC}
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +75°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

TABLE II

Symbol	Parameter	Limits							Units	Conditions (Note 1)
		0°C		+25°C			+75°C			
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		V	V_{CC} = 4.75V I_{OH} = -0.95 mA (Note 2)
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC} = 4.75V I_{OL} = 12.8 mA (Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.5		V	V_{CC} = 4.75V
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	V_{CC} = 5.25V (Note 3)
I_R	Input Load Current		-1.6		-1.0	-1.5		-1.6	mA	V_{CC} = 5.25V V_R = 0.45V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25V V_R = 4.5V
I_{SC}	Short Circuit Current			-10		-30			mA	V_{CC} = 5.0V V_{OUT} = 0V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25		25	mA	V_{CC} = 5.25V GND Pins 1 & 2
t_{pHL}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5.0V R_X = 5.0 KΩ
t_{pLH}	Negative Trigger Input to Complement Output				25	40			ns	C_X = 0 C_L = 15 pF
$t_{W(min)}$	Minimum True Output Pulse Width				45	65			ns	
Δt_{out}	Pulse Width Variation			3.08	3.42	3.76			μs	V_{CC} = 5.0V R_X = 10 KΩ, C_X = 1,000 pF
C_{stray}	Maximum Allowable Wiring Capacitance (Pin 13)		50			50		50	pF	Pin 13 to GND
R_X	External Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

Note 1: Unless otherwise specified, R_X = 10 KΩ between Pin 13 and V_{CC} on all tests.

Note 2: Ground Pin 11 for V_{OL} test on Pin 6, V_{OH} test on Pin 8 and I_{SC} test on Pin 8.
Open Pin 11 for V_{OL} test on Pin 8, V_{OH} test on Pin 6 and I_{SC} test on Pin 6.

Note 3: Pulse test to determine V_{IH} and V_{IL} (Min PW = 40 ns).

operating rules

1. An external resistor R_X and an external capacitor C_X are required for operation. The value of R_X can vary between the limits shown on tables I and II. The value of C_X is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width t_{pw} may be calculated as follows:

$$t_{pw} = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_X}\right] \text{ (for } C_X \geq 10^3 \text{ pF)}$$

R_X in KΩ, C_X in pF and t_{pw} in ns

For $C_X < 10^3$ pF, see curve.

3. R_X and C_X must be kept as close as possible to the circuit in order to minimize stray capacitance and noise pickup. If remote trimming is required, R_X may be split up such that at least $R_{X(MIN.)}$ must be as close as possible to the circuit and the remote portion of the trimming resistor $R < R_{X(MAX)} - R_X$
4. Set-up time(t_1) for input trigger pulse >40 ns. (See Figure 1)
   Release time(t_2) for input trigger pulse >40 ns. (See Figure 2)
5. Retrigger pulse width (see Figure 3) is calculated as follows:

$$t_w = t_{pw} + t_{pd} = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_X}\right] + t_{pd}$$

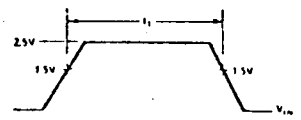


Figure 1

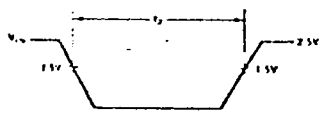


Figure 2

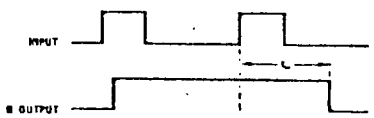


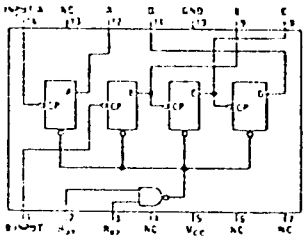
Figure 3

Data Sheet 8. DM7493 4-Bit Binary Counter.(4)

DM5493/DM7493

1. When used as a four-bit binary counter, output A is connected to the B input. In this mode outputs A, B, C, and D provide divisions by 2, 4, 8, and 16 respectively.

2. When the connection is not made between A and B and when an input frequency is applied to the B input, a frequency division of 2, 4 and 8 results on the B, C, and D outputs respectively. In this mode the A flip flop may be used independently except for the common reset input.



DM5493/DM7493

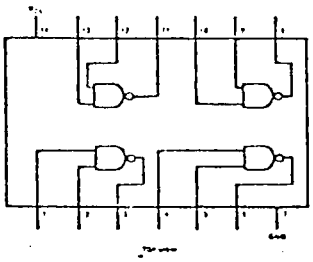
absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
DM5490, DM5492, DM5493	-55°C to +125°C
DM7490, DM7492, DM7493	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

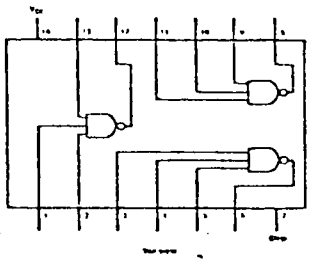
DM5493/DM7493							
Logical "1" Input Current	DM5493	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM7493	V_{CC} = 5.25V				80	μA
$R_{0(1)}$, $R_{0(2)}$							
A, B							
Logical "0" Input Current	DM5493	V_{CC} = 5.5V	V_{IN} = .4V			-1.6	mA
	DM7493	V_{CC} = 5.25V				-3.2	mA
$R_{0(1)}$, $R_{0(2)}$							
A, B							
Supply Current	DM5493	V_{CC} = 5.5V			30	43	mA
	DM7493	V_{CC} = 5.25V					
Maximum Input Frequency		V_{CC} = 5.0V,	T_A = 25°C	20	32		MHz
		F.O. = 10,	C_O = 50 pF				
Propagation Delay Time to a Logical "1" Level From Input to Output	$\frac{A}{B}$	F.O. = 10,	V_{CC} = 5.0V		16	35	ns
	$\frac{C}{D}$	C_{OUT} = 50 pF,	T_A = 25°C		35	60	ns
		All Outputs			50	80	ns
					65	100	ns
Propagation Delay Time to a Logical "0" Level From Input to Output	$\frac{A}{B}$	F.O. = 10,	V_{CC} = 5.0V		19	35	ns
	$\frac{C}{D}$	C_{OUT} = 50 pF,	T_A = 25°C		35	60	ns
		All Outputs			50	80	ns
					64	100	ns
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V					
		T_A = 25°C			8	15	ns

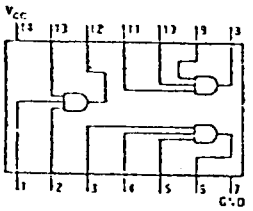
Data Sheet 9. Pin Connections for the Integrated Circuits: DM7400, DM7402, DM7404, DM7410, DM74H11, DM74L51, DM74L54, DM7473, and 9007.(5)

DM5400/DM7400
Dual-In-Line Package



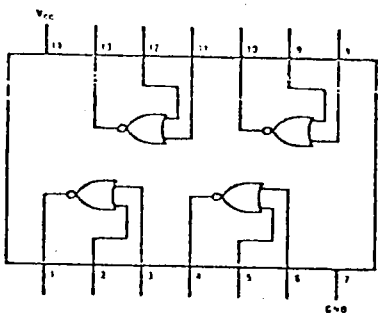
DM5410/DM7410
Dual-In-Line Package



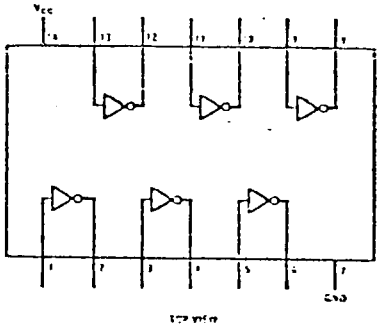


DM54H11/DM74H11
Triple 3-input AND gate

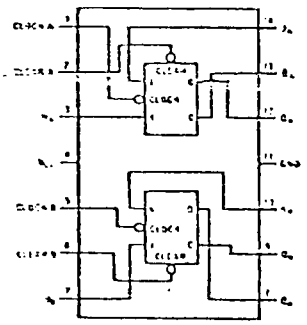
DM5402/DM7402
Dual-In-Line Package



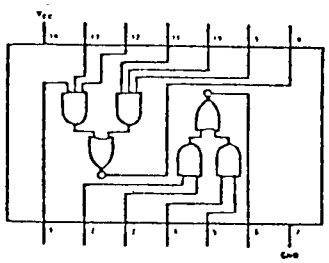
DM5404/DM7404
Dual-In-Line Package



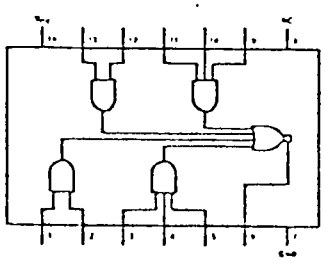
Dual-In-Line and Flat Package



DM5473/DM7473

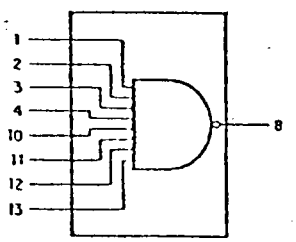


DM54L51/DM74L51



DM54L54/DM74L54

9007



APPENDIX B

PARTS LIST (QUANTITY/UNIT PRICE)

Basic LPM

Resistors, 1/4 Watt, 5%

R1:	1 Meg	(4/.20)	R13:	10K	(4/.20)
R2:	10K	(4/.20)	R14:	1 Meg	(4/.20)
R3:	5.6K	(4/.20)	R15:	1 Meg	(4/.20)
R4:	20K	(4/.20)	R16:	1 Meg	(4/.20)
R5:	20K	(4/.20)	R17:	7.5	(4/.20)
R6:	10K	(4/.20)	R18:	5.6	(4/.20)
R7:	10K	(4/.20)	R19:	4.3 Meg	(4/.20)
R8:	10K	(4/.20)	R20:	3 Meg	(4/.20)
R9:	10K	(4/.20)	R21:	5.6K	(1/.20)
R10:	10K	(4/.20)	R22:	33K	(1/.20)
R11:	10K	(4/.20)	R23:	30K	(1/.20)
R12:	10K	(4/.20)	R24:	10K	(1/.20)

Potentiometers T1 through T9: 10 KΩ, 20 Turns (36/2.30)

Capacitors in uf + 20% unless otherwise specified

C1:	0.1	(4..30)	C7:	0.1	(4/.30)
C2:	0.40 ±10%	(4/.90)	C8:	0.1	(4/.30)
C3:	0.47 ±10%	(4/.90)	C9:	50 pf	(4/.30)
C4:	0.68 ±10%	(4/.90)	C10:	0.1	(1/.30)
C5:	0.10 ±10%	(4/.90)	C11:	0.1	(1/.30)
C6:	50 pf	(4/.30)	C12-22:	0.01 uf	(38/.15)

Integrated Circuits and Diodes

LM1:	LH0042	(4/5.00)	DM10:	Fairchild 9007	(4/.66)
LM2:	LM741CN	(4/.75)	DM11:	DM74L54	(1/.70)
LM3:	LM741CN	(4/.75)	DM12:	DM7404	(1/.70)
LM4:	LM741CN	(4/.75)	DM13:	DM74H11	(1/.90)
LM5:	LM741CN-14	(4/1.60)	DM14:	DM74L54	(1/.70)
LM6:	LH0042	(4/5.00)	DM15:	DM74L54)	(1/.70)
LM7:	LH0042	(4/5.00)	DM16:	DM7473	(1/.88)
LM8:	AD351J	(4/13.45	DM17:	DM7400	(1/.55)
DM1:	DM8601	(4/1.88)	DM18:	DM7473	(1/.88)
DM2:	DM7400	(4/.55)	DM19:	DM74L54	(1/.70)
DM3:	DM8601	(4/.88)	DM20:	DM7404	(1/.70)
DM4:	DM8601	(4/.88)	DM21:	Fairchild 9007	(1/.66)
DM5:	DM7410	(4/.55)	DM22:	DM74L51	(1/.70)
DM6:	DM7404	(4/.60)	DM23, 24:	DM8601	(2/.88)
DM7:	DM7473	(4/.88)	BC1-7:	DM7493	(15/1.60)
DM8:	DM7402	(4/.55)	D1,2:	1N672 (8/1.65)	
DM9:	DM74L51	(4/.70)			

Switches

S1: Spectral 87-21-14 (4/5.00)

S2,3: Spectral 87-21-15 (2/5.00)

Power: Any DPST ON-OFF 115 VAC, 5 Amp Switch (1/2.00)

Power Supplies, Clock

+5VDC: Analog Devices AD922 (1/84.00)

±15VDC: Analog Devices AD925 (1/99.00)

Crystal Control Digital Clock: DEC M-404 (1/120.00)

Hardware

Backplane Connector Block: DEC H803 (4/14.00)

Connector Block Mounting Bar: DEC K941 (1/6.00)

Wire wrapping wire: DEC 934 (150 ft/.05)

Power and Jumper wire: Any 22 guage, solid, insulated (100 ft/.02)

Coaxial Cable: Any RG8/U (4 ft/.60)

Coaxial Cable Jacks: Any BNC (4/1.00)

Printed Circuit Boards: Any 10 in x 7 in single sided, 2 mil, copper (5/2.50)

Computer Interfacing

Bus Input Interface: DEC M1501 (4/50.00)

Ribbon Connector Board: DEC M908 (2/10.00)

Ribbon Cables: DEC BC04Z-06 (4/15.00)

Direct Data Readout

Binary to BCD ICs: DM54185A (32/4.00)

BCD to 7-Segment ICs: SN7447A (24/1.95)

7-Segment LED: HP5082-7730 (24/2.95)

IC to LED Cables: DEC 91-07575 (25 ft/.60)

7-Segment Sockets: Any 10 pin, 0.1 in staggered centers (24/.25)

Read Data Resistor and LED: 820Ω, 1/8 W, 10 percent; (1/2.00)

External Reset Switch SPDT Push Button: Allied 56C5328 (1/3.25)

Printed Circuit Boards: DEC W9720 (4/7.00)

Test Circuit

Ri: 1K, 1/4w, 5% (4/.20)

$R_{\tau u}$ through $R_{\tau g}$: Any 5K to 50K, 1/4w, 5% (7/.20)

R_T: 10K, 20 turn, Trim pot (1/2.30)

All other R: 1K to 100K, 1/4 w, 5% (12/.20)

LSa through $1S_g$: DM8601 (7/.88)

Q_a through Q_b: 2N3904 (4/.40)

Switch: Allied 56C5328 SVDT push button (1/3.25)

PC Board: Any Single Sided 2 mil copper 4" x 5" (1/1.50)

Coaxial Cable: Any RG8lu (2/.60)

Coaxial Connector Jacks: Any BNC (5/1.00)

Aluminum Enclosure: Allied 736-1919, 4" x 5" x 3" (1/3.75)

+5 Volt Power Supply: AD906, 250 ma (1/41.00)

Power Cord: Allied 663-7018, 3 Prong, 125V, 10A (1/1.35)

Jumper wire, solder, etc. (3.29)

APPENDIX C

BACKPLANE WIRING (PIN-TO-PIN CONNECTIONS)

Control Board BPV Connections

|BPV|	|BPV|	|BPI|	|BPII|	|BPIII|	|BPIV|	|BPVI|	|BPVII|
D^2		B_2	B_2	B_2	M^2		
E		C_2	C_2	M^2	D_2		
F		D_2	M^2	C_2	C_2		
H		M^2	D_2	D_2	B_2		
J	(+5V)						
K	(GND)						
M				U_2			
N					U_2		
P			U_2				
R		U_2					
S					T_2		
T				T_2			
U			T_2				
V		T_2					
B		E_2	E_2	E_2	E_2		
C	A^2	N^2	N^2	N^2	N^2		
D							M_2
F	(Manual Read Data)						
H						K^1	
K				L^2			
L					L^2		

|BPV|	|BPV|	|BPI|	|BPII|	|BPIII|	|BPIV|	|BPVI|	|BPVII|
M			L^2					
N		L^2						
S	(Manual Reset)							
T	P_2	S_2	S_2	S_2		S_2		J_2
U							L^1	
V	L^2							

Interface Cable Connector Board Backplane Connections

$BPVI^1$	BPI	$BPVI^2$	BPII	$BPVI_1$	BPIII	$BPVI_2$	BPIV
A^1	R_2	A^2	R_2	A_1	R_2	A_2	R_2
B	P_2	B	P_2	B	P_2	B	P_2
C	N_2	C	N_2	C	N_2	C	N_2
D	M_2	D	M_2	D	N_2	D	M_2
E	L_2	E	L_2	E	L_2	E	L_2
F	K_2	F	K_2	F	K_2	F	K_2
H	J_2	H	J_2	H	J_2	H	J_2
J	H_2	J	H_2	J	H_2	J	H_2
K (to control board)		K (open)		K (open)		K (open)	
L		L (open)		L (open)		L (open)	
M	J^2	M	J^2	M	J^2	M	J^2
N	H^2	N	H^2	N	H^2	N	H^2
P	F^2	P	F^2	P	F^2	P	F^2
R	E^2	R	E^2	R	E^2	R	E^2
S	D^2	S	D^2	S	D^2	S	D^2
T	C^2	T	C^2	T	C^2	T	C^2
U	B^2	U	B^2	U	B^2	U	B^2
V	A^2	V	A^2	V	A^2	V	A^2

Interface Cable Connector Board to M1501 Connections

BPVI Bus to M1501 Interface.

A	VV	Bit 0
B	TT	|
C	RR	Δt
D	NN	Data
E	LL	|
F	JJ	|
H	FF	|
J	DD	Bit 7
K[1]	Z	Reset
L[1]	X	Read Data
M	T	Bit 0
N	R	|
P	N	PDt
R	L	Counter
S	J	|
T	F	|
U	D	|
V	B	Bit 7

Remaining Channel Connections not Wired to Any Other Backplane

BPI, II, III, IV.

U[2]	Channel Input
T[2]	Input Ground
A[2]	Output LM7

V^2 +15 VDC
R^2 -15 VDC } (±15V supply)
S^2 Ground

P^2 +5 VDC

V_2 Ground (5 volt supply).

VITA

Robert Kent Fisher was born on April 4, 1948 in Washington, D.C. and spent his first five years there. Weary of the city, his parents, George L. and Ann G. Fisher moved to Maryland where he attended St. Catherine Laboure Grade School. His secondary school years were spent at Wheaton Public High School where he pursued a vocational program in electronics. Upon completion of this in 1966, the school counselors advised him to get a job; he wasn't considered college material. This advice was ignored and in the fall of 1966, he began attending night classes in Radiation Science at Montgomery College in Takoma Park, Maryland while working full time as a lab technician for W. R. Grace and Company. After two and a half years of this, he found himself bored by his work and decided to further his education. He applied for a USAEC internship in Health Physics at The University of Tennessee, received it, and entered the University in the summer of 1969. He received his Bachelor of Science degree in Health Physics in 1972 and a second B. S. degree in Nuclear Engineering one year later. He then pursued a Master of Science degree in Nuclear Engineering. Upon completion of his thesis, he received his Master's degree in August 1976.