To the Graduate Council:

I am submitting herewith a thesis written by Alex Bolling Shore entitled "A Highly Efficient Amplifier for Driving a Capacitive Load." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

James M. Rochelle

James M. Rochelle, Major Professor

We have read this thesis and recommend its acceptance:

Donald W. Bouldin

L. Vaughn Blalock

Accepted for the Council:

Carl Winkel

Vice Provost and
Dean of The Graduate School

STATEMENT OF PERMISSION TO USE

In presenting this thesis in partial fulfillment of the requirements for a Master's degree at The University of Tennessee, Knoxville, I agree that the Library shall make it available to borrowers under rules of the Library. Brief quotations from this thesis are allowable without special permission, provided that accurate acknowledgment of source is made.

Permission for extensive quotation from or reproduction of this thesis may be granted by my major professor, or in his absence, by the Head of Interlibrary Services when, in the opinion of either, the proposed use of the material is for scholarly purposes. Any copying or use of the material in this thesis for financial gain shall not be allowed without my written permission.

Signature Hall B. Stone

Date November 20, 1986

A HIGHLY EFFICIENT AMPLIFIER FOR DRIVING A CAPACITIVE LOAD

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Alex Bolling Shore

December 1986

DEDICATION

I dedicate this thesis to my parents,

Lawrence Bolling Shore and Faythe Cantrell Shore,

whose love, support, encouragement,

teaching, training, and counsel

entitles them to take credit

for the good fruit

born by their children.

ACKNOWLEDGMENTS

During this most recent year of my academic career, I was fortunate to have been under the supervision of Dr. J. M. Rochelle. I appreciate both his technical and nontechnical guidance, his patient manner, and his encouragement. Developing this amplifier for him has been a genuine pleasure.

Also, I would like to thank Drs. T. V. Blalock and D. W. Bouldin for serving on my thesis committee and for providing advice on academic and professional matters during both the graduate and undergraduate programs. I want to express my appreciation to the project director, Dr. T. M. Moriarty, for generous support, without which it would have been impossible to attain the level of development achieved within such a short time.

ABSTRACT

An amplifier which develops 230 V_{pk} sine waves between 25 and 100 kHz for a 5 nF load was designed, built and tested. The amplifier requires the system controller to configure a set of inductors within the amplifier for the frequency prior to receiving the signal. These inductors resonate with the load capacitance; thereby recycling most of the energy reflected from the load. This yields much greater efficiency than conventional non-resonant amplifiers. The amplifier is capable of initiating and terminating this resonance condition within two cycles thereby permitting accurate reproduction of tone bursts.

TABLE OF CONTENTS

SECTION		PAGE
1.	INTRODUCTION	1
2.	DESIGN PHILOSOPHY	2
3.	DESIGN OF AMPLIFIER AND MAGNETIC COMPONENTS	12
	3.1 The Amplifier's Stages	12
	3.1.1 Selection of the Monolitic Op-amp	12
	3.1.2 Design of the Discrete Gain Stage	14
	3.1.3 Current Gain Block	28
	3.1.3.1 Design of the gate drivers	28
	3.1.3.2 V_{BE} multiplier	37
	3.1.3.3 MOSFET complementary common drain stage	37
	3.2 Magnetic Components	48
	3.2.1 Transformer Design	50
	3.2.2 Design of the Inductors	55
	3.2.2.1 Choosing the inductors' values	55
	3.2.2.2 Designing the inductors	57
	3.2.3 Switch Design	60
4.	EXPERIMENTAL RESULTS	67
5.	CONCLUSIONS	80
	5.1. Suggestions for Further Study	84
REFERENCES		86
APPENDIXES		89
A.	SPICE MODELING RESULTS	90
B.	PROGRAMS USED IN DESIGN OF THE AMPLIFIER	100
C.	SPECIFICATIONS OF THE SWITCHING OF THE INDUCTORS	118
VITA		121

LIST OF FIGURES

FIGURE		PAGE
1.	Series Resonant Configuration	7
2.	Parallel Resonant Configuration	8
3.	Block Diagram of Amplifier System	13
4.	Implementation of the Op-Amp Stage	15
5.	Topology of the Discrete Gain Stage	16
6.	Implementation of the Discrete Gain Stage	25
7.	Topology of the Current Gain Stage	26
8.	Topology of the Resistively Loaded Emitter Follower Driver	29
9.	Emitter-Follower/Current-Sink Driver	31
10.	Implementation of the Gate Driver	32
11.	V_{BE} Multiplier	38
12.	Resistively Loaded Common Drain Amplifier	40
13.	Low Power Complementary Common Drain Amplifier	41
14.	Prototype of Feedback and a Resonant Load	42
15.	Gate Current and Output Voltage of the Prototype of Feedback and a Resonant Load (Figure 14)	44
16.	Implementation of the Current Gain Block	45
17.	Connections of the Resonant Load and the Topology of the Resonant Circuits and Switches Block	49
18.	Equivalent Circuit of the Transformer	51
19.	The Topology of the Double MOSFET Switch	61
20.	The Topology of the Single MOSFET Switch	62
21.	Implementation of the Single MOSFET Switch	63

FIGURE PAGE

22. The Interface Circuit 65

23. Input and Output of the Amplifier System 68

24. Output of the Amplifier System Showing the Rapid Transient Which Occurs at Cut-Off of the Signal 69

25. Input and Output Signals of the Discrete Gain Stage 71

26. Waveform at Junction of Inductor and MOSFET Switch with the Switch "Off" 72

27. Waveform at Junction of Inductor and MOSFET Switch with the Switch "On" 73

28. V_{GS} of MOSFET of One of the Inductor Switches Turning "On" 74

29. V_{GS} of MOSFET of One of the Inductor Switches Turning "Off" 75

30. The Inductor Current, I_L, at Full Power 76

31. The Transformer Current, I_{TRANS}, at Full Power 77

32. The Amplifier Current, I_{AMP}, at Full Power 78

A1. The SPICE Model Diagram of the Output Stage, Feedback Loop and the Resonant Load 94

TABLE OF SYMBOLS

A_e	the effective core area in cm^2.
A_L	the inductance of a specific number of turns on a specific core, for the transformer cores, A_L is for 1000 turns, for the inductor cores, A_L is for 100 turns.
B	the magnetic flux density.
β_x	the current gain of transistor Qx.
C_{GDx}	the gate-drain capacitance of transistor Qx.
C_{GSx}	the gate-source capacitance of transistor Qx.
$C_{jcx}(V)$	the base-collector junction capacitance of transistor Qx under a reverse-bias of V volts.
C_{jex}	the base-emitter junction capacitance of transistor Qx.
E_p	the primary voltage (peak).
E_s	the secondary voltage (peak).
f_c	the frequency where the magnitude of the loop transmission is unity.
f_{Tx}	the gain cut-off frequency for transistor Qx.
gm_x	the transconductance of transistor Qx.
H	the magnetic field strength.
I_{cx}	the collector current in transistor Qx.
I_p	the primary current (rms).
I_{Qx}	the current from a current source containing transistor Qx.
I_s	the secondary current (rms).
l_e	the effective core length in cm.
L_m	the inductance of the primary winding.
n	the ratio of the primary turns to the secondary turns.
N	the number of turns in an inductor winding.

$\|$ used as mathmatical symbol for "in parallel with".

R_c the resistor used to represent the lumped losses in a transformer.

R_{DS} the "on" resistance of a MOSFET measured from the drain to the source.

r_{ex} the dynamic emitter resistance of transistor Qx, approximately equal to the multiplicative inverse of the transconductance.

R_{inx} the input resistance of transistor Qx.

r_{ox} the output resistance of transistor Qx.

R_p the resistance of the primary winding.

R_s the resistance of the secondary winding.

T the loop transmission phasor.

V_{Bx} the voltage at the base terminal of transistor Qx.

V_{BCx} the voltage between the base and collector terminals of transistor Qx.

V_{BEx} the voltage between the base and emitter terminals of transistor Qx.

V_{Cx} the voltage at the collector terminal of transistor Qx.

V_{DSx} the voltage between the drain and source terminals of transistor Qx.

V_e the effective core volume in cm^3, the product of A_e and l_e.

V_{Ex} the voltage at the emitter terminal of transistor Qx.

V_{GSx} the voltage between the drain and source terminals of transistor Qx.

V_T the threshold voltage of an MOSFET transistor.

1. INTRODUCTION

In the field of airborne ultrasonics, one of the more common transducers available is made by the Polaroid Corporation, which uses it on several of their cameras to measure the distance between the lens and the subject. These transducers are sold by Polaroid for use on other ultrasonic equipment. For this project, it was necessary to develop an amplifier which could drive an array of these transducers to their maximum output capability. This maximum output level, which occurs with a drive signal of 200 V_{pk}, had to be maintained over a frequency range from 25 kHz to 100 kHz. This array can be modeled as a parallel RC network consisting of a 450 kΩ resistor and a 450-550 pF capacitor.[1] The primary design goals were prioritized as follows: low distortion, high efficiency, reliability, small size and low weight; these were obtained to varying degrees. Also, since bursts of ultrasound were needed, the ability of the amplifier to rise to full power quickly (within one or two cycles) and then drop back to zero output was important.

These goals were realized with the development of a feedback amplifier which uses power MOSFET's, resonant circuits configured by the system controller, and a voltage step-up output transformer.

2. DESIGN PHILOSOPHY

The development of the design centered around four issues: the use of power MOSFET's for the output devices, the method of achieving the high voltage output, the problem of efficiently driving a capacitive load and the stability of a feedback amplifier driving a capacitive load. Each of these issues will be subsequently discussed.

The current state of the art in power MOSFET technology makes them an attractive alternative to bipolar devices where low saturation voltages are not required and where the frequency of operation is above about 50 kHz.[2,3] Since our frequency band lies in this region and low saturation voltages are not required of the devices, the choice to use power MOSFETs for the output devices was made early. The requirements of low gate drive impedance because of the high gate-source capacitance (often greater than 1000 pF per device) and their susceptibility to destruction by forward biasing the parasitic diode were considered in the selection of the output stage configuration.[4] Advantages to using power MOSFETs are their immunity to secondary breakdown, their resistance to thermal runaway and their low average gate drive current (no DC bias current into the gate).[5]

The high voltage output signal could have been achieved in several ways. Some of the configurations considered were

1) a high-voltage complementary common drain or source (Class AB),
2) a high-voltage driver transistor and current source (Class A),
3) a push-pull configuration using two N-channel devices and a transformer, and

4) a low voltage complementary common drain or source (Class AB) and a voltage step-up transformer.

Initially the required output voltage was 1000 V_{pk-pk}. Therefore, an output stage which used no transformer to step up the output signal level would require devices with breakdown voltages exceeding 1000 V_{pk}. Power MOSFET's with these ratings could not be readily obtained. Another disadvantage to using the transformerless output stage is the power dissipation of a given value of quiesient current is higher since the supply voltages must be greater if no step-up transformer is used. An advantage to using no step-up transformer is that the feedback loop can be connected directly to the junction of the power transistors and the load. Thus differences from the input signal and the voltage across the load can be detected by the feedback and corrected. The use of a transformer between the power transistors and the load introduces AC coupling which rules out a single voltage division feedback network. In order to stabilize the bias points using feedback, a low-frequency DC coupled loop would be required. This second slower feedback loop would only need to be effective up to a few Hertz and would attempt to stablize the bias points against changes in temperature, supply voltage, etc. The main feedback loop could still be a simple resistive voltage divider, but the interaction between the loops would need to be investigated and the benefits of such a system did not seem certain.

The use of a step-up transformer to multiply the voltage from the output of the amplifier to the level required by the load was considered the best approach to take. Even after the output voltage requirement

was reduced to 200 V_{pk}, the advantages of incorporating a step-up transformer outweighed the advantage of simplicity offered by the transformerless design. Some of the advantages of using a step-up transformer are: lower voltage devices are less expensive and more efficient (their internal resistance is lower since less semiconductor is needed to prevent breakdown with a weaker electric field), lower voltage power supplies, lower quiesient power dissipation and the lower voltage devices are available. The transformer must be kept out of the feedback loop to avoid having to add a DC bias loop. Hence, in order to provide a fairly linear output signal, the transformer must be operated within its linear region.

Now that the issue of using a transformer after the output circuit has been decided, what configuration should be used to drive the transformer? The three topologies considered were 1) complementary common source, 2) push-pull common source and 3) complementary common drain. The advantage of the common source configurations is that they are naturally stable even when driving a capacitive load. Since the load is capacitive, this is an important strength. The disadvantage of the common source designs is the complexity of their driver circuit. Both common source circuits require the driver circuit to provide current for the full input capacitance of the power device since gain is required and no reduction of the capacitances by 'bootstrapping' is possible. The complementary circuit requires the driver circuit to develop signals referenced to each of the power supplies. The push-pull circuit requires inversion of the signal for one of the power transistors and a special transformer, both of which are complications.

The complementary common drain circuit has the advantage of simple, low-power driver circuits since the gate-drain capacitance is not multiplied by gain and most of the gate-source capacitance is neglectible because the gain is near unity, and the voltage between the gate and source is nearly constant. The drive signals for the power transistors are identical except for a DC offset; this also simplifies the driver circuitry. The disadvantages to the complementary common drain topology are: 1) the drive signal must be larger in magnitude than the output signal, and 2) capacitive loading may cause oscillation. The first disadvantage is not a great difficulty, but the second one could be. Modeling by SPICE produced inconclusive results, but experimental work with the output stage indicated that the oscillation problem could be solved. See Appendix A for the modeling of the capacitively-loaded common drain amplifier.

If the transformer is well designed, the current due to losses will be a small fraction of the load current. Since the load is capacitive, the current delivered by the power transistors will lead the output voltage by 90°. Essentially, very little energy is actually used by the load. The energy sent to the load by the amplifier is returned to the amplifier where it must be dissipated as heat by the output transistors. This reactive load results in greater power dissipation in the output transistors than driving a resistive load at the same voltage and current would. This energy would have to be supplied by large power supplies and dissipated by large heat sinks and fans. The efficiency of the amplifier could be improved by storing this energy reflected by the

load and returning it to the load on the next cycle. This would reduce the power consumption, weight and size of the amplifier. This was done by selecting four inductors such that the fifteen combinations of the four inductors span the values necessary to resonate with the load capacitance over the frequency range. The system controller knows the frequency of the signal about to be transmitted. It selects the proper combination of inductors prior to applying the signal to the amplifier. By recycling most of the energy reflected from the load, higher efficiency was achieved.

The two configurations possible for the resonant inductors and switches are series and parallel (Figures 1 and 2). The parallel circuit's impedance increases toward infinity as resonance is approached with losses in the wiring and inductor core as well as stray inductance and capacitance limiting the impedance to some finite value. The series circuit's impedance attempts to approach zero reactance at resonance. At resonance, the impedance is real, not reactive; consequently, the amplifier can more efficiently drive the load at resonance.

The maximum available output power into resistive loads is the maximum product of the output voltage times the output current available at that output voltage. Given a maximum output voltage and current rating, there is a minimum large-signal impedance which can be assigned to the output stage. For loads below this minimum impedance, the maximum current is reached before the maximum voltage; and thus, the power delivered to the load is less than the maximum. Similarly, for load impedances above the optimum, the maximum voltage is achieved prior to the

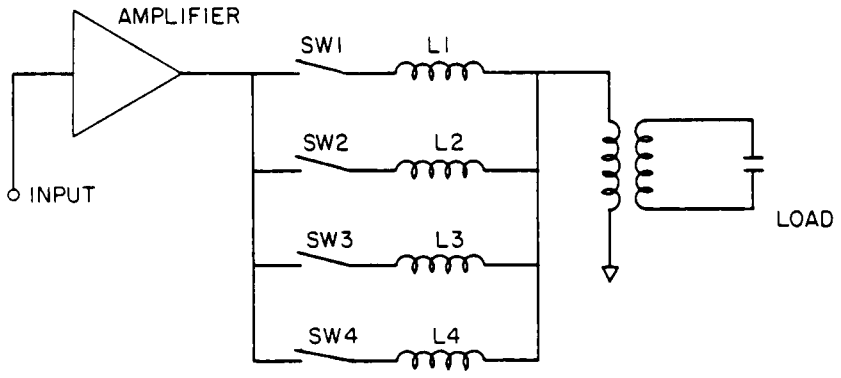


Figure 1. Series resonant configuration.

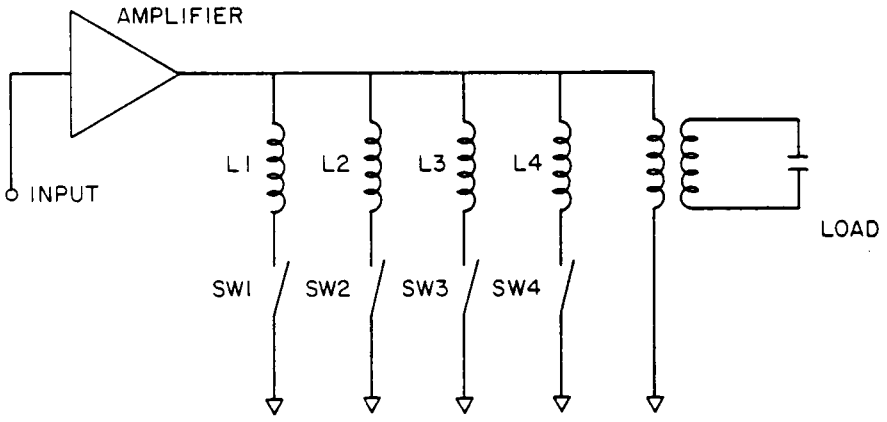


Figure 2. Parallel resonant configuration.

current peaking; consequently, the output power is less than the maximum available. Given an output power level, reducing the voltage across the output devices or the current through them increases the efficiency of the output stage since less power will be lost as heat in the output devices. Essentially, this means that increasing the load impedance, as long as the power level remains constant, tends to improve the efficiency of the output stage. Since the impedance of the parallel configuration peaks as its power consumption wanes, it naturally improves the efficiency of the output stage as it nears resonance. On the other hand, the series configuration's impedance drops as its impedance becomes real; consequently, the voltage across the transistors in the output stage would increase and the transistors would be forced to dissipate more power near resonance.

Furthermore, with the series inductors, the full load current would circulate through the output stage of the amplifier; this would cause much heat and tends to defeat the purpose of having the energy storage. By using the parallel configuration, the large resonant circulating current flows through the inductors and the transformer, not the output transistors. Another disadvantage to the series configuration is that the loop transmission will vary significantly as the frequency approaches the resonant frequency if shunt feedback is used at the amplifier's output. This is because there is voltage division between the output impedance of the output stage and the input impedance of the effective load, the inductors/transformer combination. For the series configuration, as the frequency approaches resonance, the input

impedance of the effective load drops, consequently, so would the magnitude of the loop transmission. This effect would probably require a sophisticated compensation system in the feedback. Based on these observations, the parallel inductor configuration was chosen.

One concern about using the resonant load circuit was the transient response of the resonant tank. SPICE analysis of parallel and series resonant circuits indicated that parallel resonance was advantageous in this aspect as well. The use of a low impedance driver circuit with feedback connected to the junction of the power transistors and the resonant tank allowed good control of the start-up and stopping transients as well as good control of the steady-state output voltage.

Feedback was considered necessary to improve stability, linearity, and simplify the biasing of the amplifier. Considerations in the design of the amplifier and feedback network were stability, step response, adequate loop transmission to reduce distortion, adequate gain to limit input signal to a low level, and the speeds of the various stages in the amplifier. Although the input is always a sine wave, it is amplitude modulated. In the case of a rectangular modulating signal, the output should show no signs of overshoot or ringing; i.e., good step response. Although good step response and stability can be achieved with a variety of configurations; the simplest, and hence the most desirable approach, is to design the amplifier's loop gain to contain a single dominant pole. If an op-amp is used in the amplifier, the dominant pole will be the one in the op-amp. If another stage were to have a pole at a frequency lower than the loop transmission's 0 dB frequency, it would need

to be nullified. This generally means adding a zero in the feedback network to cancel the offending pole. It was desired to keep the feedback network as simple as possible, preferably, a simple voltage divider. If this is to be accomplished, the stages after the op-amp must be designed to be fast enough to allow the op-amp's pole to singularly drive the loop gain to unity.

Good step response in the same sense as above means that the slew rate must be adequate to pass full power signals at the highest frequency in the bandwidth. The stages that must be examined for slew rate are the op-amp and any gain stages. The complementary common drain output stage and the complementary common collector gate drivers (as implemented) are intrinsically very fast.

The gain of the amplifier must be high enough to raise a low level input of 1 V_{pk} or less to the full power output of 200 V_{pk}. Hence, the overall gain through the amplifier and transformer, the amplifier system, should be at least two hundred. For a given open loop gain, the loop transmission decreases if the closed-loop gain is increased. In general, distortion increases as the loop gain decreases. Therefore, the maintainance of sufficient loop gain places a upper limit on the closed loop gain of the amplifier.

3. DESIGN OF AMPLIFIER AND MAGNETIC COMPONENTS

Having discussed the philosophy behind several of the major design decisions, the specifics of the design will be discussed. The basic system must compare the output signal with the input signal, amplify the difference in magnitude and power, store some energy to improve efficiency and transfer the signal to the load (Figure 3). These tasks are most logically discussed as two sections, the amplifier's stages and the magnetic components.

3.1 The Amplifier's Stages

The comparison and voltage gain blocks were accomplished by a monolithic op-amp driving a discrete gain stage. The current amplification was achieved with two gate driver circuits, a V_{BE} multiplier and two power MOSFET's. The energy storage block is constructed of four parallel resonant inductors with a MOSFET switch on each inductor. The transfer of the signal to the load was accomplished with a 1:8 step-up transformer and a short length of coaxial cable. Finally, the feedback network is a simple resistive voltage divider.

3.1.1 Selection of the Monolithic Op-amp

The selection of the monolithic op-amp used was primarily based on two specifications: the gain-bandwidth product and the slew rate. The Motorola MC34081P is a new op-amp which has better performance in these areas than the older 741's and 351's. The gain-bandwidth product is 8 Mhz, and the slew rate is 25 V/μsec. The low frequency pole is given in

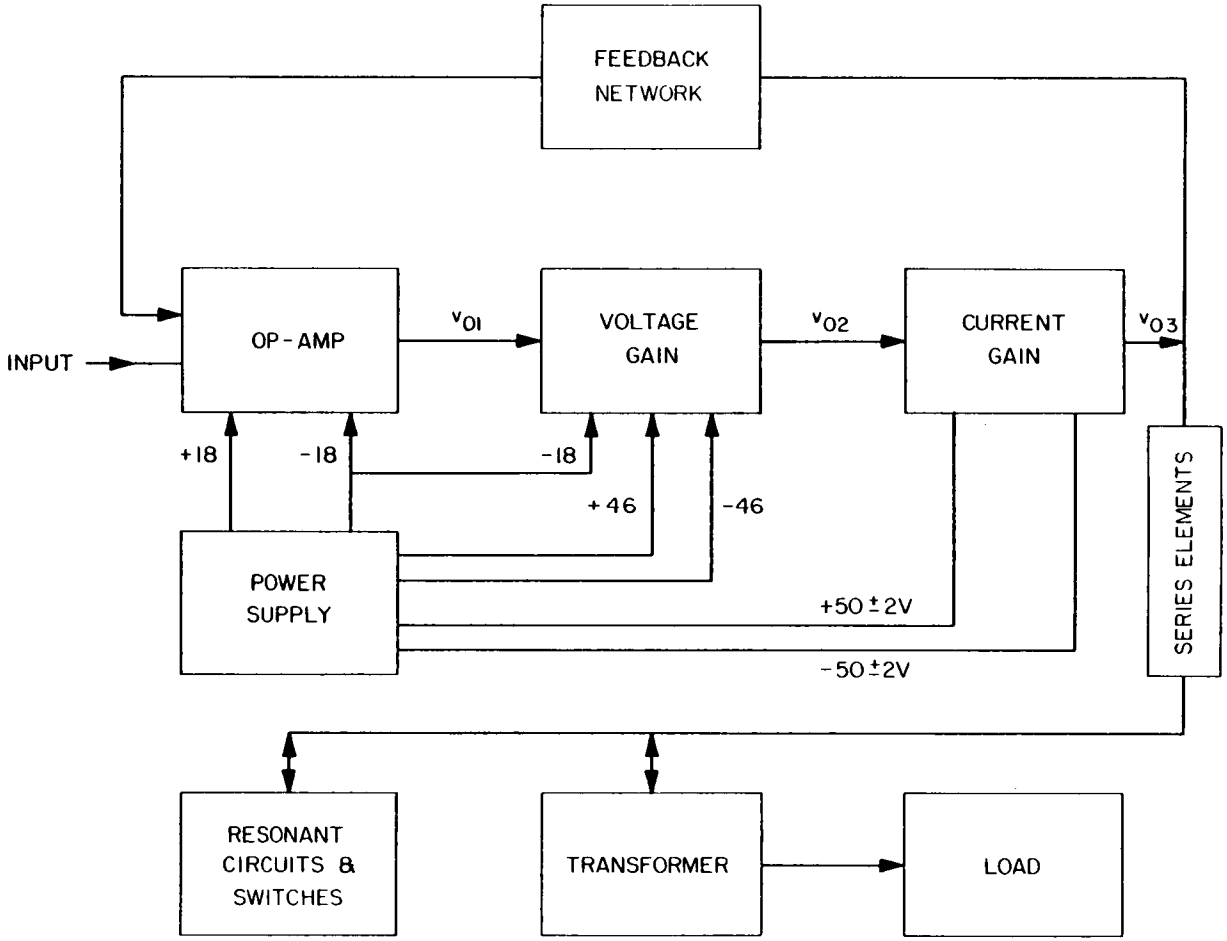


Figure 3. Block diagram of amplifier system.

the data sheet as 100 Hz, and the open loop gain is given to be typically 80,000 V/V.[6] Even though a slower op-amp may have been used, this part was inexpensive and readily available (Figure 4). With the op-amp chosen, the gain stage could be designed.

3.1.2 Design of the Discrete Gain Stage

The gain stage following the op-amp is constructed of four discrete transistors (Figure 5). The input is driven by the op-amp, and the output drives the base of the emitter follower Q5. The equations derived from the analysis of the circuit are given in the first part of this section, and the actual design and implementation is discussed later.

The gain circuit was analysed to produce equations to describe the relationships the components would have on the key performance parameters. These principal performance parameters are the pole and zero frequencies, the magnitude of the forward gain and the slew rate. To develop these equations, certain characteristics of other circuits in the amplifier also had to be described mathematically prior to the section in which they are discussed.

In this configuration, the lowest frequency pole above the passband is at the collector of Q3. This frequency, f_{hi}, is

$$F_{hi} = \frac{1}{(2\pi)(R11 \| R_{in5})(C_{jc3} + C7 + C_{jc4} + C_{in5eff})}, \qquad (1)$$

where:

R_{in5} is the input resistance of Q5,

C_{jc3} is the collector-base capacitance of Q3,

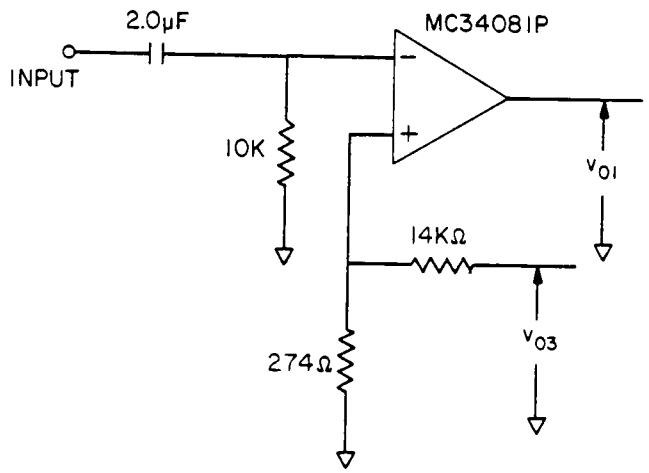


Figure 4. Implementation of the op-amp stage.

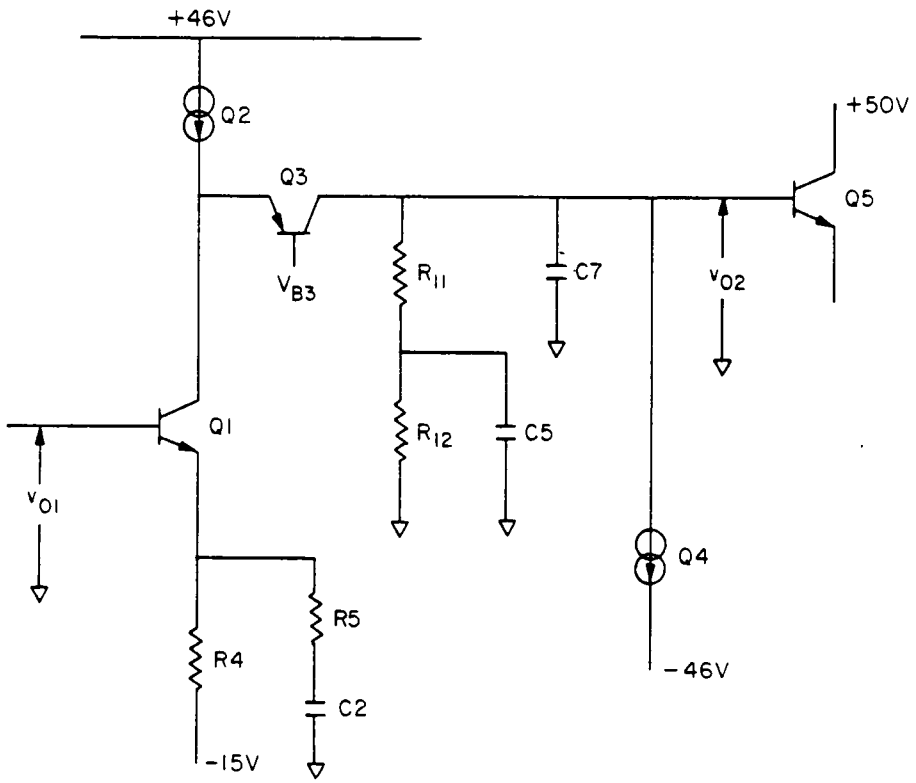


Figure 5. Topology of the discrete gain stage.

C_{jc4} is the collector-base capacitance of Q4, and

C_{in5eff} is the effective capacitance added by Q5.

The zero-voltage bias values for the junction capacitances must be adjusted to reflect the significant reverse bias which these junctions experience. Making use of the parallel plate capacitor analogy, at zero-voltage bias, the junction capacitance primarily due to the charge stored on either side of the depletion region, is at its maximum. For higher voltages, the depletion region widens, the "plates" of charge move away from each other; and hence, the effective junction capacitance is lowered. The values of the capacitances were measured at virtually zero volts reverse bias. The approximation for obtaining the value of the capacitance at higher reverse bias voltages is

$$C_j(V) = \frac{C_j(0)}{(1 + \frac{V}{\phi})^m} , \qquad (2)$$

where:

$C_j(0)$ is the zero bias junction capacitance,

V is the reverse bias in volts,

ϕ is the built-in barrier potential, typically 0.6 V, and

m is the capacitance gradient factor, typically 1/3 to 1/2.[7]

C_{in5eff} is the sum of C_{jc5} (found as for C_{jc3} and C_{jc4}) and the effective emitter-base capacitance, C_{je5eff}. C_{je5eff} can be found by

$$C_{je5eff} = C_{je5}(0)(1 - A_{be5}) , \qquad (3)$$

where A_{be5} is the gain from the base to the emitter of Q5.

The value of R_{in5} is found by first calculating the values of R_{in8}, R_{in9}, R_{in10} and R_{in11}.

$$R_{in8} = R_{in9} \simeq (\beta_{8,9})(r_{e8} + r_{e9} + R17 + R18) \ . \tag{4}$$

$$R_{in10} = R_{in11} \simeq (\beta_{10,11})(r_{e10} + r_{e11} + R23 + R24) \ . \tag{5}$$

Then,

$$R_{in5} \simeq (\beta_5)(r_{e5} + r_{o6} \parallel R_{in8} \parallel R_{in9} \parallel R_{in10} \parallel R_{in11}) \ . \tag{6}$$

Knowing R_{in5}, the mid-band gain of this stage can be found.

$$V_{O2}/V_{O1} = \frac{gm_3(R11 \parallel R_{in5} \parallel r_{o3} \parallel r_{o4})(\frac{1}{gm_3} \parallel r_{o2} \parallel r_{o1})}{\frac{1}{gm_1} + (R4 + R5)} \ , \tag{7}$$

for signals in the band of frequencies between 25 kHz and 100 kHz.

The gain at frequencies below the passband is influenced by the pole of R12 and C5 and the pole and zero of R5 and C2. The gain at frequencies above the midband region is reduced by the poles at f_{hi} and the cutoff frequencies of Q1 and Q2. Thus the gain becomes

$$A(f) = (V_{O2}/V_{O1}) * A_1(f) * A_2(f) * A_3(f) \ , \tag{8}$$

where:

$$A_1(f) = \frac{\frac{1}{gm_1} + (R4 \parallel R5)}{\frac{1}{gm_1} + (R4 \parallel R5)(1 + \frac{R4}{R5})} \ \frac{1 + jf(2\pi C2R5)}{1 + jf(2\pi C2(R4 + R5))} \ ,$$

$$A_2(f) = \frac{R11 + R12}{R11(1 + jf2\pi C5R12)} ,$$

$$A_3(f) = \frac{1}{(1 + j\frac{f}{f_{hi}})(1 + j\frac{f}{f_{T2}})(1 + j\frac{f}{f_{T1}})} .$$

At DC, the gain is increased by the factor 1 + (R12/R11) and reduced by the factor 1 + (R4/R5). Thus, the DC loop gain can be increased over the midband loop gain.

The slew rate of this stage is approximately the available charging current divided by the total node capacitance at the collector of Q3. The total available current is either $I_{Q2} - I_{Q4}$ or I_{Q4}, depending on whether the voltage is slewing positive or negative, respectively.

$$\text{Slew Rate } (+) \simeq (I_{Q2} - I_{Q4})/(C_{jc3} + C_{jc4} + C7 + C_{in5eff}) . \quad (9)$$

$$\text{Slew Rate } (-) \simeq I_{Q4}/(C_{jc3} + C_{jc4} + C7 + C_{in5eff}) . \quad (10)$$

This is greater than the real maximum slewing rate because some of the current is diverted through R11, R12, C5, R_{in5}, r_{o3} and r_{o4}; consequently, it is not available for charging the node capacitance.

During the actual design phase, even more approximate equations were used. The major simplifications were: 1) R_{in5} was assumed infinite, 2) all output impedances of transistors were considered infinite, and 3) the current gain of each transistor was assumed infinite. Thus, the actual gain was slightly less than the design gain.

Choosing the gain and pole frequency was the first step toward implementation of this gain stage. This involves considering the characteristics of the complete feedback loop. In order to allow the loop gain to be driven through unity by a single pole, the f_{hi} of the stage must be beyond the loop transmission's 0 dB crossover frequency, f_c. If the voltage gain block is fairly linear, the loop transmission will not need to be that great in order to achieve low distortion. Subsequently, a loop gain of about 20 at the highest frequency in the passband was chosen as a design goal. The overall gain of the amplifier must be considered in selecting the composite gain of the voltage gain and current gain blocks. Since the combined gain of the amplifier and the transformer can be no lower than 200 and some margin for error should be built-in, the overall input to output gain of the amplifier system was chosen as 300. At the time of the design of the discrete gain stage, the ratio of the step-up transformer was 1:6. Thus, the composite gain of the voltage and current gain blocks was set at 50. In order to have a loop transmission of about 20 at 100 kHz and a gain of 50, the gain of the forward path, A_{fp}, will need to be at least;

$$| \text{ loop transmission } | \simeq \frac{A_{fp}\left(\frac{1}{1 + A_{el}}\right)}{\frac{f}{f_{op\text{-}amp}}} = \frac{A_{fp}\left(\frac{1}{51}\right)}{\frac{f}{100}} , \qquad (11)$$

where:

A_{el} is the desired gain of the electronic amplifier sections,

A_{fp} is the gain of the forward path, and

$f_{op\text{-}amp}$ is the frequency of the dominant pole of the op-amp.

Hence,

$$A_{fp} = 20 * (100 \text{ kHz} / 100 \text{ Hz}) * 51 , \qquad (12)$$

Since the pole of the op-amp is near 100 Hz, the gain of the forward path is at least $1.02 * 10^6$. The gain of the op-amp is about 80,000; so, the voltage gain of this stage must be greater than 12.75. This assumes that the gain of the power stage is unity, which it is close to. Thus, the design goal for the amplifier gain was chosen to be 20. The actual gain will be slightly lower because the full expression for the gain was simplified to a less exact equation for use during the design phase for expediency.

The high frequency pole needs to be beyond f_c. From Eq. 11, f_c can be approximated.

$$\begin{aligned} f_c &= f_{op\text{-}amp} * |T| * A_{op\text{-}amp} * A_{dgs} * A_{cgs} * A_{fb} \\ &= 100 \text{ Hz} * 1 * 80{,}000 * 20 * 0.9 * 1/51 \\ &= 2.8 \text{ MHz} , \end{aligned} \qquad (13)$$

where:

$|T|$ is the magnitude of the loop transmission,

$A_{op\text{-}amp}$ is the small-signal voltage gain of the op-amp,

A_{dgs} is the voltage gain of the discrete gain stage,

A_{cgs} is the voltage gain of the current gain stage, and

A_{fb} is the gain of the feedback network.

Assuming the voltage gain of the current gain block to be 0.9, the loop gain cross-over frequency will be 2.8 MHz. Hence, the first high frequency pole of the voltage gain block was chosen to be beyond 4 MHz.

With a heat sink that will fit into the limited space, the maximum power dissipation of Q1, Q3 and Q4 is about 5 watts. The maximum power dissipation of Q2 is only 1 W. The peak dissipation chosen for Q1, Q3 and Q4 was half their maximum; or 2.5 W. Transistors Q3 and Q4 have the highest dissipation and hence are the limiting devices as far as selecting the value of the current is concerned. The voltage across Q3 and Q4 is about 50 volts, so the maximum average current through either device should be less than 50 mA, to stay below 2.5 watts dissipation.

In order to provide a drive signal to the current gain block of at least 30 V_{pk}, the values for I_{Q2}, I_{Q4} and R11 were chosen to be 60 mA, 35 mA and 1.5 kΩ respectively. With R11 at 1.5 kΩ, only 20 mA is required to develop a 30 V signal. This results in the minimum current flow in Q3 to be I_{Q4} - 20 mA or 10 mA and the maximum current to be 20 mA + 35 mA, or 55 mA. Consequently, the minimum current in Q1 is 5 mA and the maximum current is 50 mA.

The dynamic range of the signal out of the op-amp was kept within ± 5 V. This was done to insure that the open loop gain was close to the small-signal value of 80,000. Consequently, the voltage swing at the base of Q1 needs to be kept small to provide the dynamic range needed for the signal and DC bias adjustments. This constraint keeps R4 and R5 small. To reduce the DC loading of the node at the collector of Q3, R12 was chosen to be 100 kΩ. This causes an increase of the gain as the frequency drops to zero by a factor of 1 + R12/R11 or 67.7. Thus to reduce this to an increase of only 10 or 20, R4 was chosen 5 to 10 times greater than R5. By choosing R4 equal to 470 Ω and R5 equal to 91 Ω, the DC gain is only 11 times greater than the gain at mid-band.

Besides the choice and achievement of the gain of this stage, the design of the dominant pole frequency is probably the most important criteria. Calculation of the first pole frequency above the passband was done with Eqs. 1, 2 and 3. Eq. 2 was used to adjust the values of the collector-base capacitance from their low bias values to their values at the operating conditions.

Q#	$C_{jc}(0)$	Average Reverse Bias, V_{rb}	$C_{jc}(V_{rb})$
3	26 pF	40 V	3.1 pF
4	8.5 pF	40 V	1.0 pF
5	8.5 pF	45 V	0.97 pF

In order to use Eq. 3 to find the effective base-emitter capacitance of Q5, the base-emitter gain must be determined.

$$A_{be5} = R_{Leq} / (r_{e5} + R_{Leq}) . \tag{14}$$

$$R_{Leq} = r_{o6} \parallel R_{in8} \parallel R_{in9} \parallel R_{in10} \parallel R_{in11} . \tag{15}$$

Then A_{be5} can be calculated to be 0.998. Being conservative, a gain of only 0.95 was used to find the effective capacitance. Thus, from Eq. 3, the residual C_{je5eff} was calculated to be 3.0 pF. Finally, C_{in5eff} can be determined from the sum of C_{je5eff} and $C_{jc5}(V_{rb})$, which is 3.97 pF. Calculating f_{hi} from Eq. 1 but ignoring the loading effect of R_{in5}, f_{hi} was found to be 8.3 MHz. This is an approximation which is conservative since the loading of the node by R_{in5} should reduce the impedance of the node, consequently raising the pole frequency. As long as the pole

frequency is higher than 4 Mhz, the amplifier's characteristics should not be seriously degraded.

Referring to Eq. 8, it can be seen that the networks containing capacitors C2 and C5 produce two low frequency poles, f_{1fp1} and f_{1fp2} and one low frequency zero, f_{1fz1}. These capacitors were chosen large enough to keep these low frequency poles and zero at least two decades of frequency below the passband; the values of C2 and C5 are not critical. The function of these capacitors was to separate the DC circuit from the AC circuit, which permitted greater flexibility in design and implementation. The resultant frequencies of the networks containing these capacitors are given in the following table.

Components	Symbol	Frequency
C5, R12	f_{1fp1}	0.8 Hz
C2, R5	f_{1fp2}	795 Hz
C2, (R4 + R5)	f_{1fz1}	129 Hz

The values for several expressions used in the preceding design equations were computed or measured and are given in the following table (Figures 6 and 7).

Expression	Value
I_{C8}, I_{C9}, I_{C10}, I_{C11}	15 mA
β_8, β_9, β_{10}, β_{11}	130
R_{in8}, R_{in9}, R_{in10}, R_{in11}	1.67 kΩ
I_{C5}	35 mA
R_{in5}	71.8 kΩ

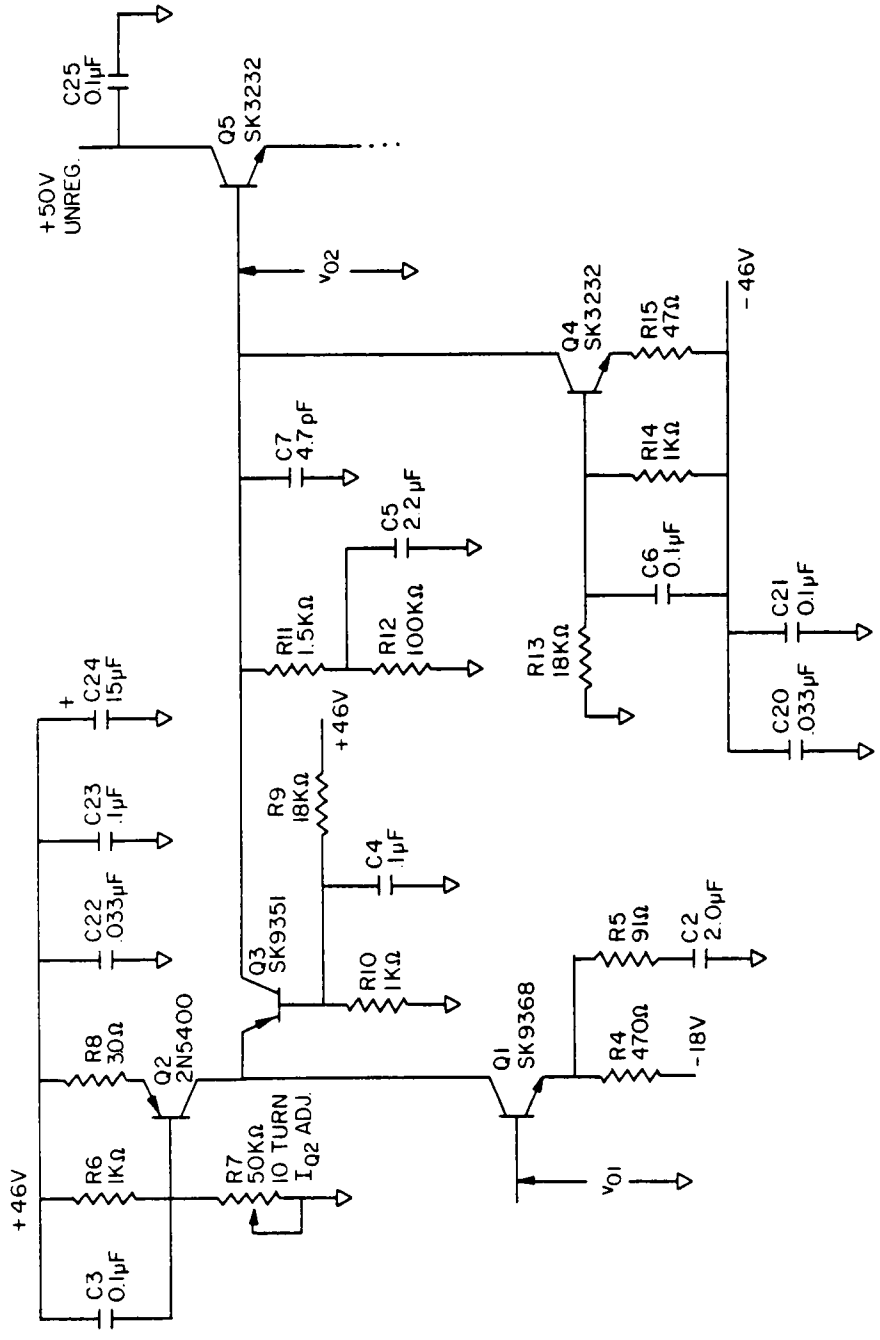


Figure 6. Implementation of the discrete gain stage.

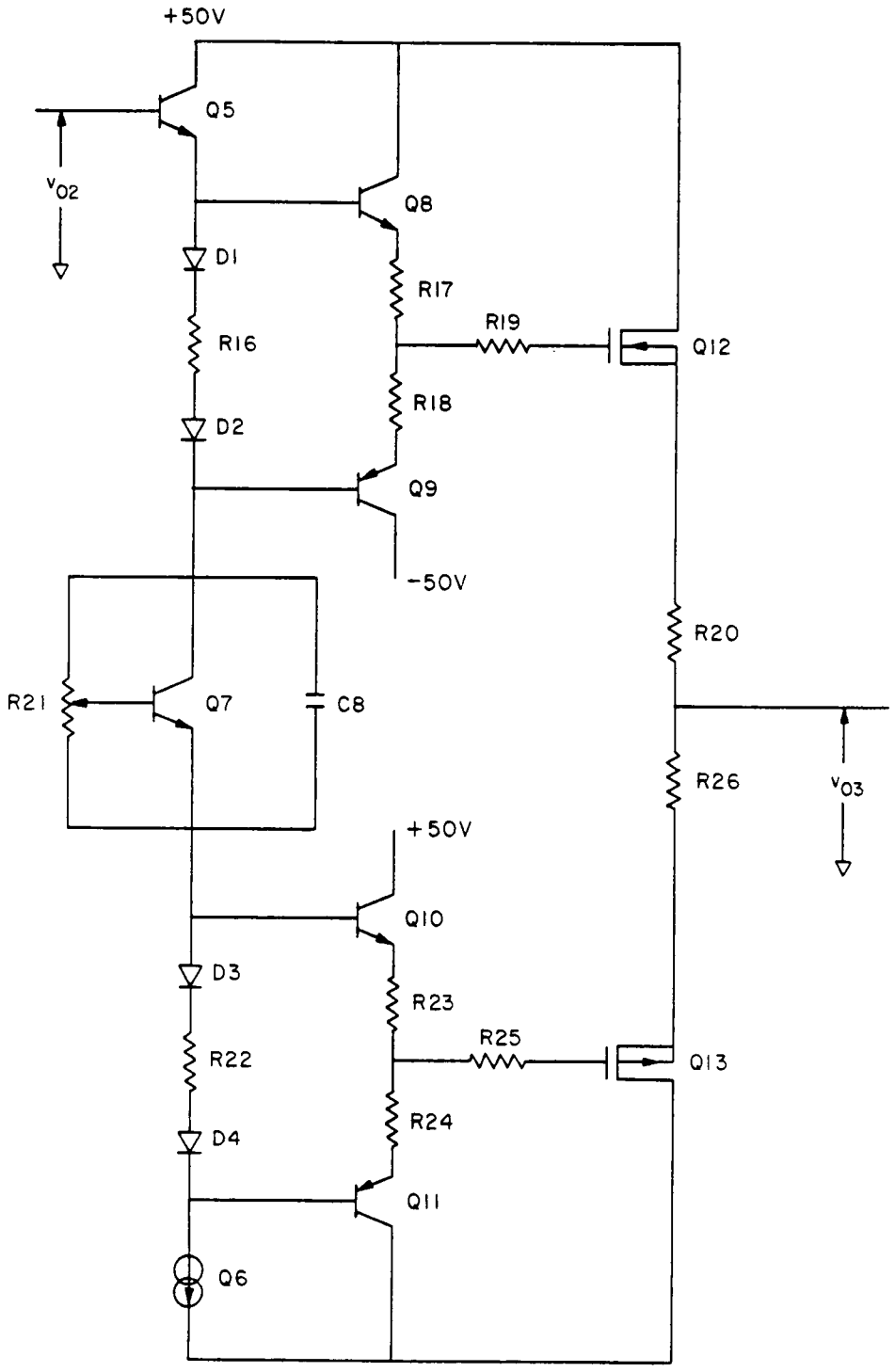


Figure 7. Topology of the current gain stage.

Although the loop transmission calculations and results relate to the entire electronic section of the amplifier system, not just to the discrete gain stage, they were essential to the design of the discrete gain stage. Therefore, the results from the implementation of the following stages have been brought forward to this point so that the discussion of the loop transmission could be completed in this section.

The complete mid-band to high frequency loop transmission is

$$T(f) = \frac{A_{op\text{-}amp} \cdot A_{dgs} \cdot A_{cgs} \cdot A_{fb}}{(1 + j \frac{f}{f_{op\text{-}amp}})(1 + j \frac{f}{f_{dgs}})(1 + j \frac{f}{f_{gd}})^2 (1 + j \frac{f}{f_{CCD}})}, \quad (16)$$

where:

$A_{op\text{-}amp}$ is the mid-band gain of the op-amp, 80,000;

A_{dgs} is the mid-band gain of the discrete gain stage, 17.3;

A_{cgs} is the mid-band gain of the current gain stage, $\approx$ 0.9;

A_{fb} is the gain of the feedback network, 1/51;

$f_{op\text{-}amp}$ is the low frequency pole of the op-amp, 100 Hz;

f_{dgs} is the first pole above mid-band of the discrete gain stage, measured to be about 10 MHz;

f_{gd} is the pole of one of the gate drivers, 60 MHz; and,

f_{CCD} is the pole of the complementary common drain output stage, $\approx$ 436 MHz.

From Eq. 16, the phase margin is 72°, the gain margin is 22.4 dB and the loop transmission at 100 kHz is 24.4 @ 90.7°.

3.1.3 Current Gain Block

The current gain block consists of three main circuits: the gate drivers, the V_{BE} multiplier and the output stage. The design and implementation of each of these circuits is subsequently discussed.

3.1.3.1 Design of the gate drivers

The gate drivers were added to the current gain block to insure that adequate current was available to charge and discharge the gate capacitances. A secondary goal was to reduce the loading on the emitter follower Q5.

In order to supply the charge necessary to rapidly control the current flow in a large power MOSFET, the driver circuit must be able to actively source and sink charge. To maintain a single pole roll-off in the loop gain, the output stage's poles must be well above f_c. The power MOSFET's used have a substantial input capacitance. Consequently, in order to achieve a high frequency stage, the gates must be driven by a low impedance.

One of the configurations considered for the gate driver was the resistively-loaded emitter-follower driver (Figure 8). Considering just one of the outputs of this driver, V_{O1} has a low output impedance during the half cycle when Q1 is supplying current; i.e., the output voltage is increasing. But during the other half cycle, the output impedance is primarily the value of the emitter resistor, R_{E1}. This driver was rejected since the low values required for the emitter resistors, R_{E1} and R_{E2}, also increase the current consumption to an unacceptable level.

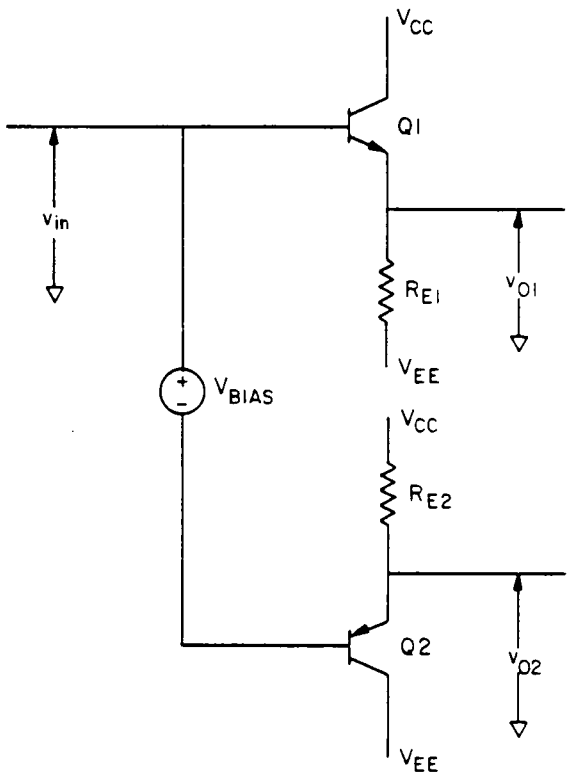


Figure 8. Topology of the resistively loaded emitter follower driver.

Another configuration considered was an emitter-follower and current-sink combination (Figure 9). This configuration has good current sourcing ability, but can only sink charge at the value that the current sink is adjusted to. In breadboarded prototype driver/output combinations, this configuration resulted in poor slew rates for the negative-going portion of the signal. Increasing the current in the current sink would solve the slewing problem but would increase power dissipation and exceed the supply current allocated to the driver circuit.

The gate driver chosen was designed to have a low output impedance, low current consumption and low power dissipation (Figure 10). The complementary common collector configuration has an inherently low output impedance. The emitter resistors, R_{E1} and R_{E2}, serve to prevent thermal runaway as well as increase the input impedance to the gate driver. After the emitter resistor values were finalized, the diode connected transistors and the 1.1 Ω resistors were chosen; they set the quiescent current in the driver transistors to 15 mA.

Choosing the emitter resistors involved three considerations: 1) output impedance, 2) quiescent current and 3) thermal runaway protection. A higher output impedance increases the time required to charge the gate-source capacitance. This reduces the slew rate of the output stage and lowers the pole in the loop transmission associated with the MOSFET gates. From a paper on a linear amplifier which used 680 Ω gate resistors with MOSFET's having half the input capacitance and functioned up to 25 kHz, a scaled value of 100 Ω was chosen an approximate value

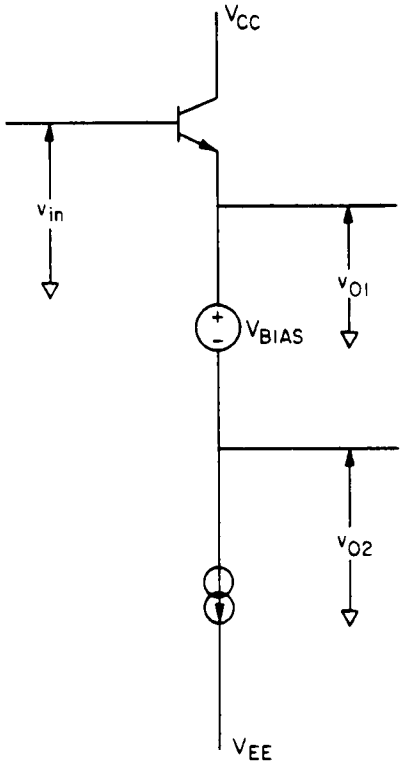


Figure 9. Emitter-follower/current-sink driver.

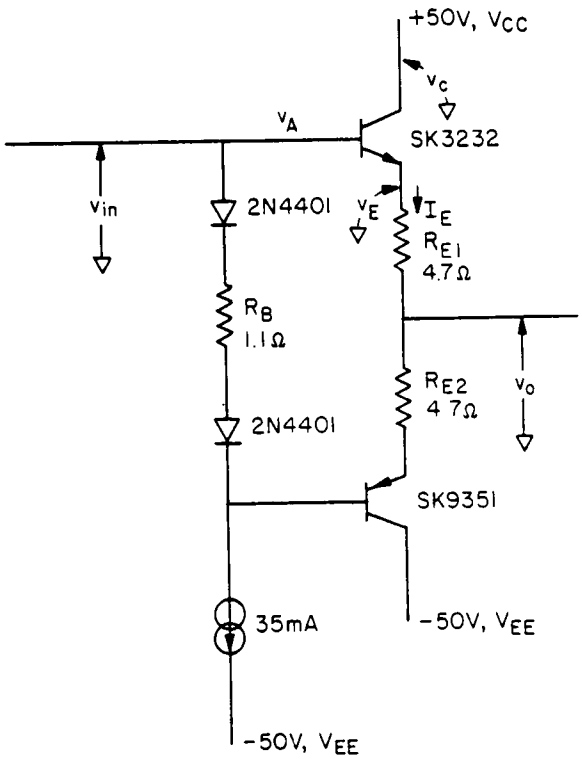


Figure 10. Implementation of the gate driver.

for the gate resistors.[8] In order not to adversely affect the speed of the output stage, this 100 Ω was chosen as the upper limit of the gate impedance. So as to leave freedom for choice of the series gate resistors, the output impedance of the gate drivers was chosen to be less than 10 Ω. Since the node at the input of the gate driver is driven by an emitter follower, its impedance is very low. The output impedance of the gate driver is the sum of the base impedance divided by the current gain and the emitter resistor. The impedance is primarily the value of the emitter resistor since the other component is negligible.

The second criteria for selecting the emitter resistors is the level of the quiescent current. To reduce the loading on the power supplies and reduce the level of heat produced, the quiescent current was chosen to be no more than 50 mA. In order to keep the current gain of the transistors high, the current needed to be above 1-2 mA. Consequently, the quiescent current was chosen to be 15 mA.

The power dissipation with no signal is about 50 V * 0.015 A or 0.75 W, per device. The devices were heatsinked so they can safely handle about 4 Watts. This should easily handle the heat produced when a signal is applied. Indeed, no rise in temperature was detected even at continuous full output power.

The third criteria which impacted the choice of emitter resistors is the thermal stability of the bias point. The bias point of a diode has a negative forward voltage versus temperature coefficient.[9] As the temperature rises in the device during operation, the bias voltage

required to support a given current decreases. Consequently, more current is allowed to pass through the device; this causes more heat which causes further increases in current. If this increase is not checked, the devices will overheat until they are destroyed. This positive thermal feedback effect is known as "thermal runaway". In order to prevent thermal runaway, the emitter resistors must be chosen large enough so that an increase in the current through the resistors increases the voltage across the resistors at least as much as the change in temperature decreased the bias voltage. Simplified, the gain around the loop must be less than unity.

To begin to find the critical value of the emitter resistors, consider the circuit (Figure 10). The power dissipation,

$$P_{diss} = (V_{CC} - V_E - I_E R_E) I_E \ . \tag{17}$$

Let,

$$I_E = I_o + \Delta I \ , \tag{18}$$

where:

I_o = initial quiescent current and

ΔI = positive disturbance in the current due to a change in V_{BE}.

Since

$$V_{BE} = V_A - I_E R_E \ , \tag{19}$$

it follows that the change in V_{BE} due to an increase in the emitter current is

$$\Delta V_{BE} = -\Delta I_E R_E \ . \tag{20}$$

The factor, $\Delta V_{BE}/\Delta Temp$, is defined as $K_{BE} \simeq -2$ mV/C°[10] and relates the change in the bias voltage, ΔV_{BE}, to the change in temperature, $\Delta Temp$. So, the change in V_{BE} due to the increase in temperature is

$$\Delta V_{BE} \simeq \Delta Temp * K_{BE} \ . \tag{21}$$

To prevent thermal runaway, the gain from the input of the thermal system around the loop back to the input, i.e., the thermal loop transmission, must be less than one.

$$\frac{\Delta V_{BE}/\Delta T}{\Delta V_{BE}/\Delta I} < 1 \ . \tag{22}$$

Or, equivalently,

$$\Delta V_{BE}/\Delta I - \Delta V_{BE}/\Delta T < 0 \ . \tag{23}$$

Assuming that ΔV_{CE} is much less than V_{CC} and that the product $I_E R_E$ is also much less than V_{CC},

$$\Delta Temp = \Delta P_{diss} * R_{\emptyset JA} = V_{CC} * \Delta I_E * R_{\emptyset JA} \ , \tag{24}$$

where $R_{\emptyset JA}$ is the junction to ambient thermal resistance. Combining Eq. 21 and Eq. 24,

$$\Delta V_{BE} \text{ due to } \Delta T = V_{CC} * \Delta I_E * K_{BE} * R_{\emptyset JA} \ . \tag{25}$$

Rearranging Eq. 20 gives

$$\Delta V_{BE} \text{ due to } \Delta I = -\Delta I_E R_E \cdot \tag{26}$$

Substituting into Eq. 23,

$$-\Delta I_E R_E - V_{CC} * I_E * K_{BE} * R_{\emptyset JA} < 0 \cdot \tag{27}$$

Since stability is of concern only when ΔI_E is greater than zero, division by ΔI_E is possible, this produces

$$-R_E - V_{CC} * K_{BE} * R_{\emptyset JA} < 0 \cdot \tag{28}$$

Finally, for thermal stabilty,

$$R_E > 0.002 * V_{CC} * R_{\emptyset JA} \cdot \tag{29}$$

Based on a comparison of the size of the heat sinks to ones of known value, $R_{\emptyset JA}$ was estimated to be no greater than 30 C°/W. With $R_{\emptyset JA}$ = 30 C°/W and V_{CC} = 50 V, then R_E must be greater than 3.0 Ω for thermal stability. In light of the low impedance, quiescent current, thermal stability requirements as well as a margin for error, the emitter resistors were chosen to be 4.7 Ω.

After the emitter resistors were chosen, the bias network of two diode-connected transistors and a bias resistor was implemented. Then, the bias resistor, R_B (R16 and R22, Figure 7, p. 26), was adjusted until the quiescent current through the driver transistors was 15 mA.

Another important consideration for the gate drivers is their speed. Since these are emitter follower circuits which have low output impedances and are being driven by a low impedance, the poles at their

input and output terminals will be near f_T of the previous stage and f_T of the driver transistor, respectively. In other words, the pole at the node of Q5 is approximately f_{T5} (Figure 7, p. 26). The poles at the emitters of Q8, Q9, Q10 and Q11 are near the f_T's of the respective transistor. For Q8 and Q10, f_T is typically 80 MHz. For Q9 and Q11, f_T is typically 60 MHz. These frequencies are well above the loop transmission's unity gain frequency; consequently, they are acceptable.

3.1.3.2 V_{BE} multiplier

The sum of the threshold voltages for the power MOSFET's is certain to be between two and ten volts. A DC bias is needed to allow some quiescent current to flow in both MOSFET's; this greatly reduces crossover distortion. A V_{BE} multiplier was designed which easily accomodates this range (Figure 11). It is stable, and is AC bypassed by C8, a 0.1 μF monolithic capacitor.

3.1.3.3 MOSFET complementary common drain stage

The output stage configuration was modeled by SPICE. The simulations indicated that it would work, and highlighted some areas of potential difficulty. The circuits similar to those modeled in SPICE were prototyped in the laboratory to learn more about the areas of difficulty. These areas were high frequency oscillation if the load was too capacitive and possible long transient periods before steady-state was reached. The first problem, oscillation was solved by the use of resistors in series with the gates of the MOSFET's. These resistors are recommended by the manufacturers of power MOSFET's. However, a high

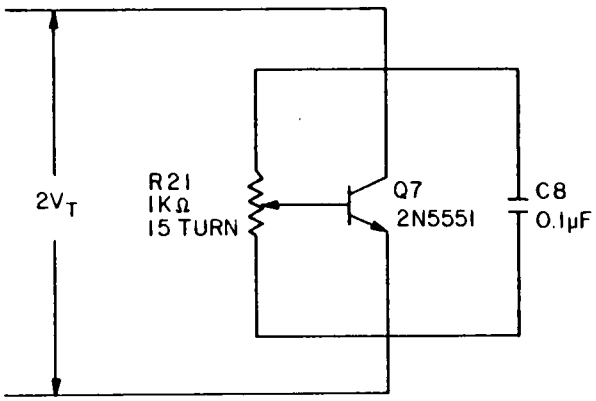


Figure 11. V_{BE} multiplier.

frequency oscillation still appears as a low-level current oscillation, but the output voltage is not affected. The second problem was solved partially by the feedback loop and partially by using large capacitors on the power supply connections of the power transistors. These large capacitors supply the charge surge needed to energize and de-energize the resonant tank.

The development of the output stage began with a simple resistively loaded common drain amplifier (Figure 12). The amplifier oscillated until the 100 Ω gate resistor was added. Next, a complementary common drain circuit was built and tested (Figure 13). This circuit performed well with a resistive load except for a low negative-going slew rate. Increasing the current in the current source improved this problem. Following that experiment, a complementary common drain output stage was built to investigate the combination of a resonant load and feedback (Figure 14). The frequency of resonance of the parallel tank circuit was 51.4 kHz. The particular values for the load capacitance and resonant inductor were determined by multiplying the load capacitance, 5nF, by 30 and then finding a value of inductance to cause resonance near 52 kHz. The load capacitance was multiplied by 30 since a 1:5 step-up transformer multiplies the capacitance of the load by 25, and a 1:6 transformer multiplies it by 36. At this point of development, the transformer ratio had not been finalized. The amplifier performed well for frequencies between 45 kHz and 70 kHz. The amplifier required a 1 μH series inductor, L_s, to prevent oscillation. This oscillation was up beyond 100 kHz in frequency and was a loop stability problem. The

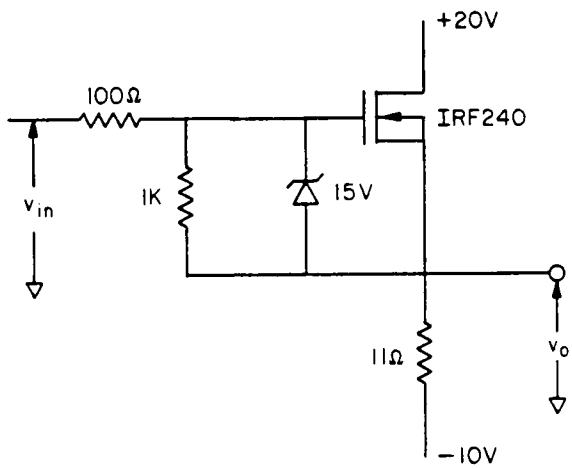


Figure 12. Resistively loaded common drain amplifier.

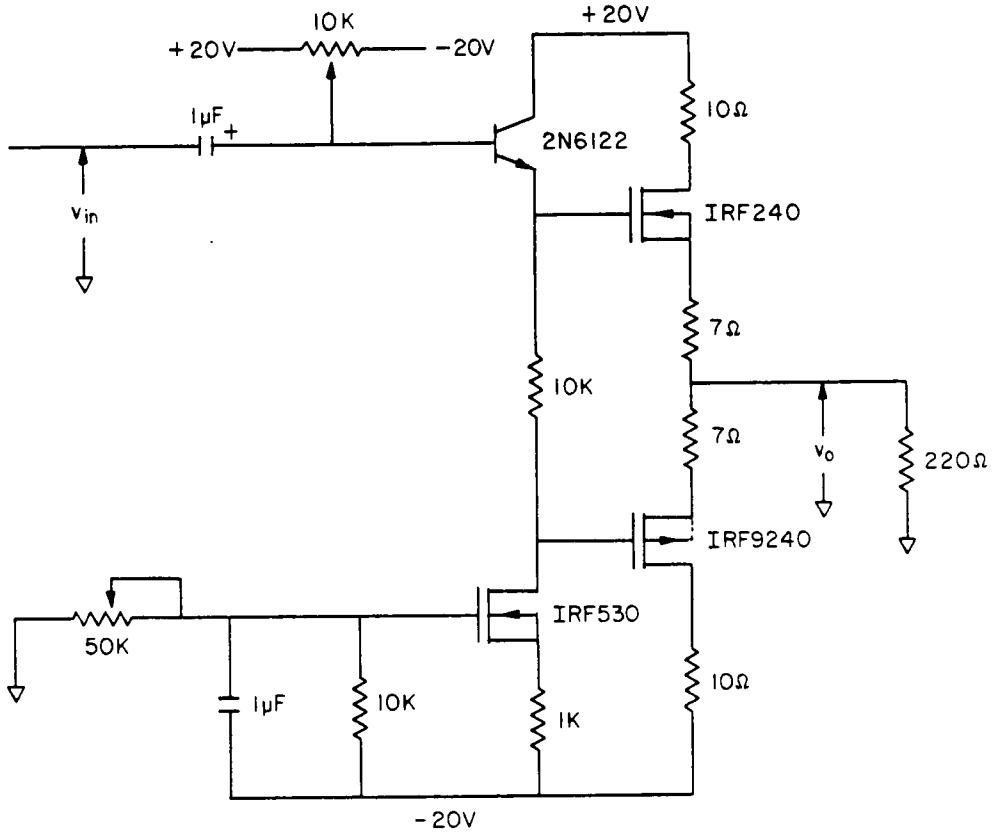


Figure 13. Low power complementary common drain amplifier.

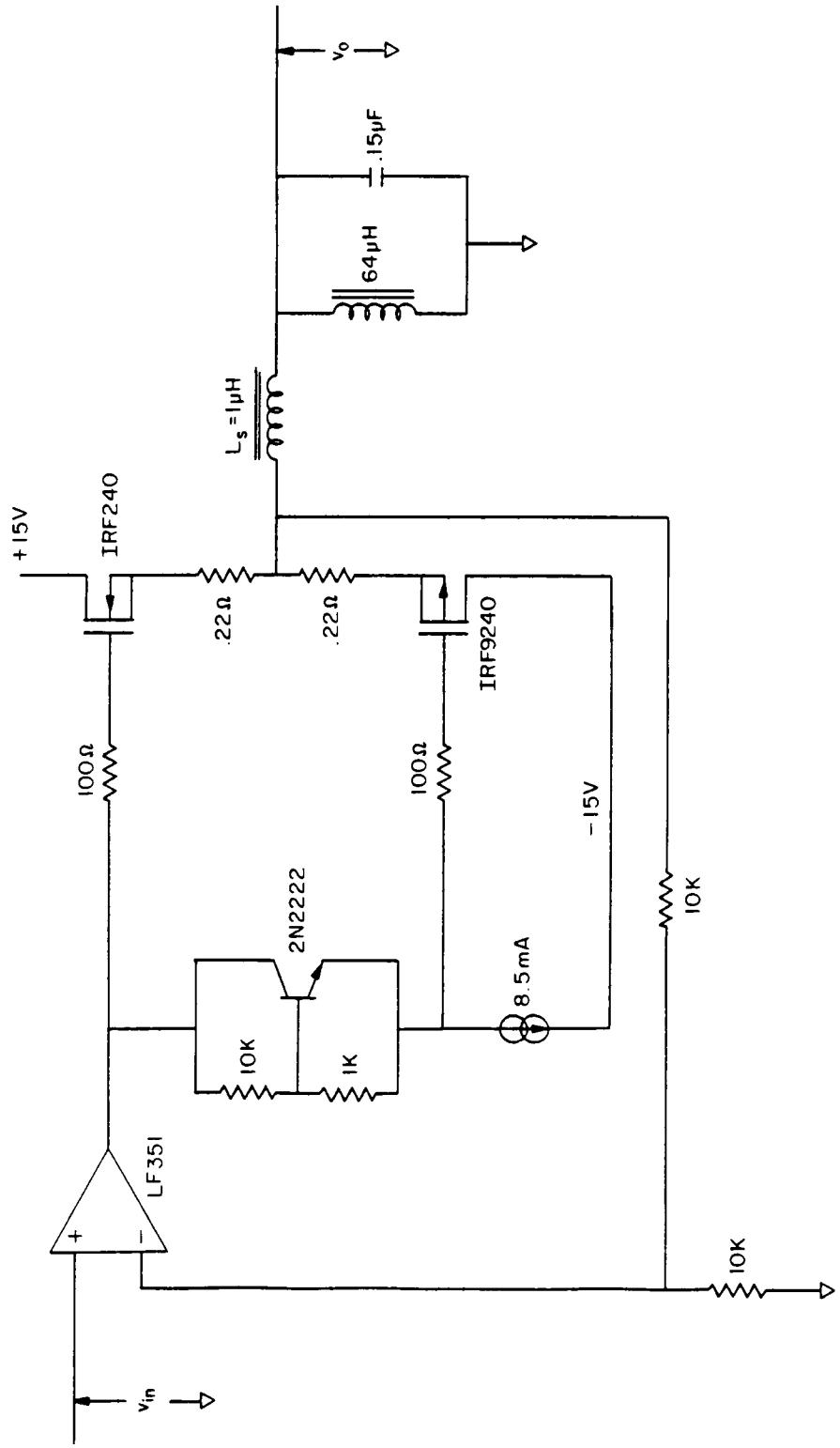


Figure 14. Prototype of feedback and a resonant load.

stability of a high loop transmission feedback system driving a resonant circuit was taken as proof that this configuration would work as long as the amplifier was operated near resonance.

The gate current of one of the power MOSFET's in this circuit was observed on an oscilloscope (Figure 15). A relatively high frequency oscillation was seen. It was not continuous; but instead, it appeared around the zero voltage crossing point of the output signal. The frequency of this oscillation was 22 MHz. This oscillation was a loop stability problem also. After opening the loop and driving the signal to the same output level, the oscillation was not present. The open loop circuit was stable for no load, 50 Ω load, L_s and the tank circuit or just the tank circuit by itself. This stability was tested over the range from 1 kHz to 100 kHz with no oscillation detected on the gates or anywhere else. Consequently, this circuit's topology was chosen for the output stage.

After some experimentation with the currents in the gate drivers and Q6, the output stage was implemented (Figure 16). The gate resistors, R19 and R25, were reduced to 51 Ω and 33 Ω, respectively. These values were about twice the lowest value that reliably prevented oscillation. The source resistors, R20 and R26, were initially picked as a means of limiting each MOSFET's current to about 3.5 amps by placing a gate robbing transistor across each resistor. Above 3.5 amps, the gate robbing transistor would turn on and rob current from its respective gate. This 3.5 amps was the maximum circulating current for a transformer ratio of 1:7. This current limiting was later deemed

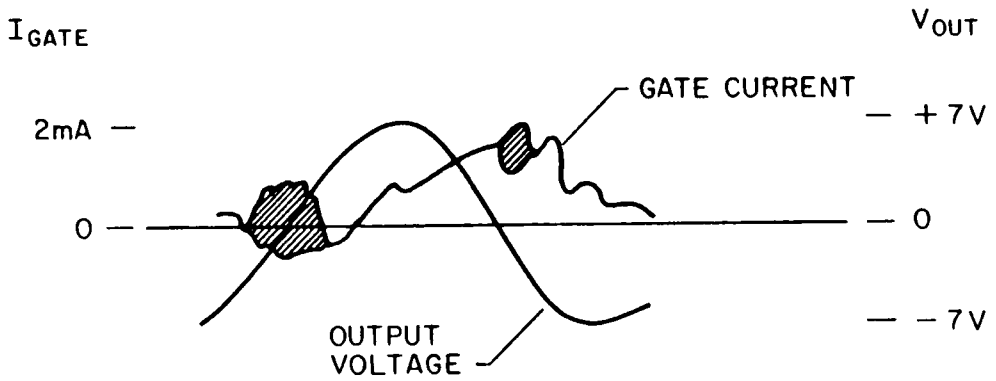


Figure 15. Gate current and output voltage of the prototype of feedback and a resonant load (Figure 14).

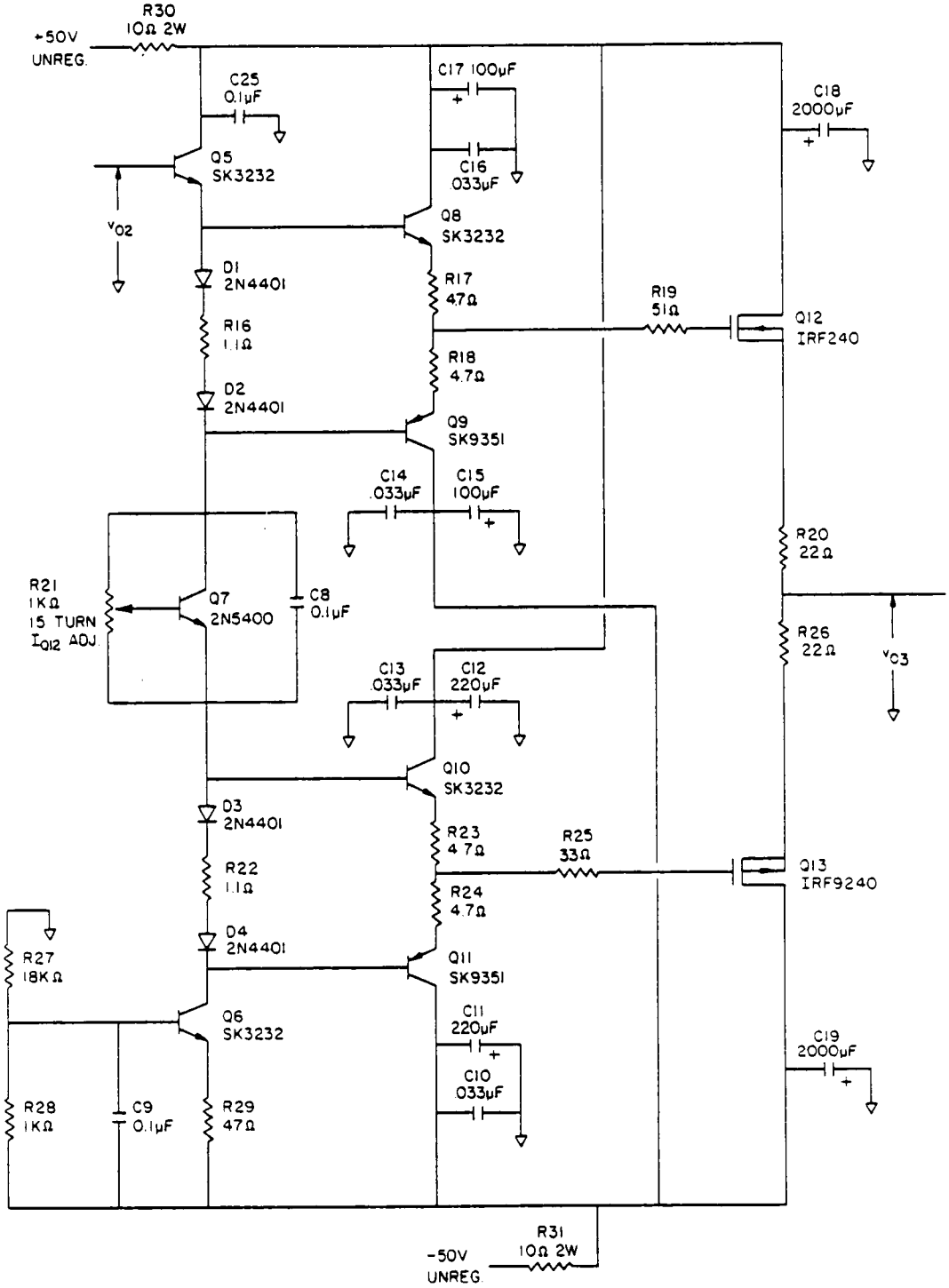


Figure 16. Implementation of the current gain block.

unnecessary. But the source resistors were left in the circuit to provide a convenient facility for measuring the individual source currents. The large power supply filter capacitors, C18 and C19, were added to supply the surge of charge needed to energize and de-energize the output resonant tank at the beginning and end of a tone burst.

The output stage was designed to be cooled by natural convection. The peak power dissipation in the output transistors occurs at the beginning and end of a tone burst. However, this occurs for less than 30 μsec, so it is easily absorbed by the transistors. The condition of operation which results in the highest sustained power dissipation is full power operation at 37.6 kHz in the lowest frequency band. The peak amplifier current, I_{max}, was calculated to be about 690 mA, capacitive (Appendix C). This current was measured to be 740 mA. The power dissipation calculation was done for 1.0 A peak current; since the power supplies can deliver no more than this.

For the 1.0 A reactive current, the power dissipation per MOSFET is

$$P_d(t) = v_{device}(t) * i_{device}(t) , \tag{30}$$

where,

$$v_{device}(t) \simeq V_{CC} - v_{signal}(t) . \tag{31}$$

And,

$$v_{signal}(t) = K * \sin(t) , \tag{32}$$

where the frequency has been normalized and K is the peak amplitude of v_{03} (Figure 16). Ignoring losses in the inductor core and wiring resistance,

$$i_{device}(t) = I_{max} * \cos(t) \ , \tag{33}$$

where I_{max} is the maximum amplifier current required at this frequency. Then,

$$\begin{aligned} P_d(t) &= (V_{CC} - v_{signal}(t)) * I_{max} * \cos(t) \\ &= (48 - 25\sin(t)) * 1.0 * \cos(t) \ . \end{aligned} \tag{34}$$

Integrating the instantaneous power dissipation over the half cycle that the transistor is on, the average power dissipation is

$$\begin{aligned} P_{d\ average} &= 0.5 \left[\int_{-\pi/2}^{\pi/2} 48 \cos(t)\, dt - \int_{-\pi/2}^{\pi/2} 25 \sin(t) \cos(t)\, dt \right] \\ &= 0.5(48(\sin(-\pi/2) - \sin(\pi/2) - 25(0.5)(\sin^2(-\pi/2) \\ &\quad \cdot \sin^2(\pi/2))) \\ &= 0.5(2(48) - 25/2\ ((-1)^2 - (1)^2)) \\ &= 0.5 * 96\ W = 48\ W \ . \end{aligned} \tag{35}$$

This is for continuous output. In general, the duty cycle is less than 10%; consequently, the $P_{d\ average}$ is less than 5 W. The temperature of the transistor's junction, T_j, can be calculated by Eq. 36.

$$T_j = T_a + P_d * (R_{\emptyset JC} + R_{\emptyset CS} + R_{\emptyset SA}), \tag{36}$$

where:

T_a is the ambient temperature, typically 25 C°;

$R_{\emptyset JC}$ is the junction to case thermal resistance, 1.0 C°/W;

$R_{\emptyset CS}$ is the case to sink thermal resistance, ≈ 0.2 C°/W; and,

$R_{\emptyset SA}$ is the sink to ambient thermal resistance, 1.5 C°/W.

So for this worst-case analysis,

$$T_j = 25\ C^\circ + 5\ W * 2.7\ C^\circ/W \simeq 38.5\ C^\circ\ . \qquad (37)$$

This temperature is quite acceptable. Even when operated at full power continuously, the junction temperature does not exceed the maximum specified by the manufacturers.

3.2 Magnetic Components

The amplifier uses magnetic components in the transformer block and in the resonant circuits and switches block. Within the former block is a 1:8 linear step-up transformer; it serves to raise the voltage from the output stage to the level required for the load. The transformer was designed with the help of the first program in Appendix B. The resonant cicuits and switches block contains a set of four carefully chosen inductors and MOSFET switches (Figure 17). By "closing" the switches in different combinations, the inductors are effectively placed in parallel with each other. For a given frequency there is a value of inductance which will resonate with the load capacitance. For a given frequency, choosing the combination of the four inductors which minimizes the current load to the amplifier will result in the best efficiency possible being realized. The values of the four inductors and the frequencies where the combination of inductors is changed were selected by the second program in Appendix B.

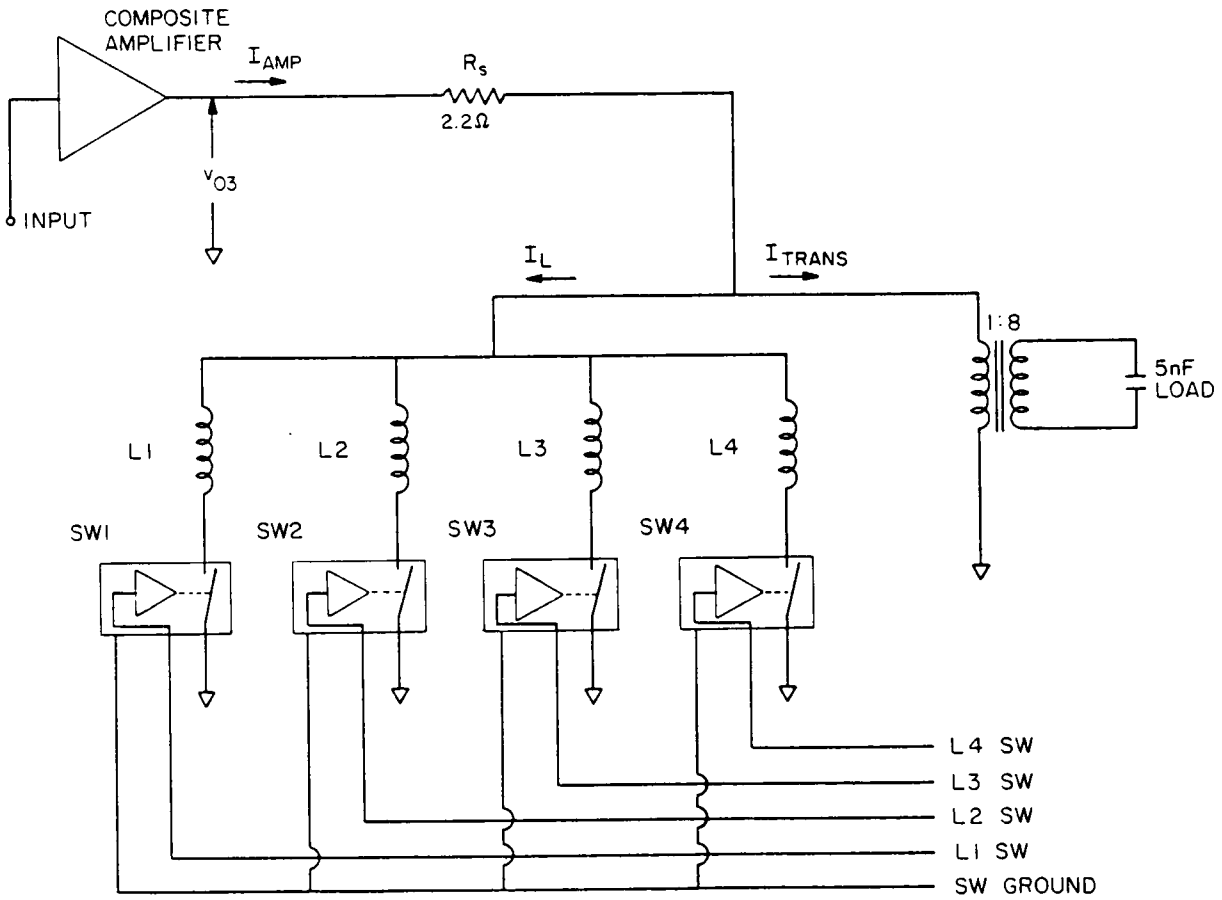


Figure 17. Connections of the resonant load and the topology of the resonant circuits and switches block.

3.2.1 Transformer Design

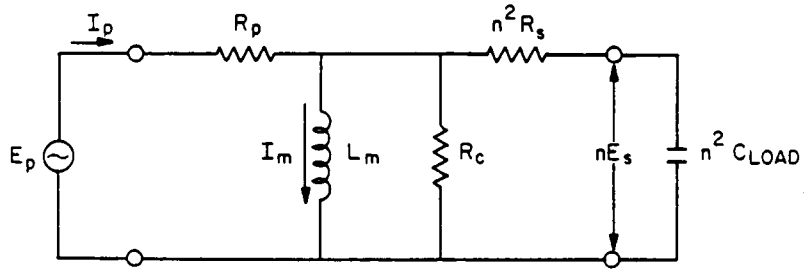
The design of the transformer began by determining the ratio of the primary voltage to the secondary voltage. Eventually, a ratio of 1:8 was settled on. This limited the input voltage to less than 30 V_{pk} for an output voltage of 200 V_{pk}. The available cores for the transformer were three toroid cores from Ferroxcube. They were made of 3C8 material, a medium permeability, high saturation flux density Manganese-Zinc ferrite.[11] The toroid shape was chosen for its self-shielding and low flux leakage properties. This material, 3C8, was chosen over the alternative 3C6A because the transformer must operate as linearly as possible. The flux density versus magnetic field strength curves show the 3C8 material to be linear to a higher flux density that the 3C6A material.

Since the signal level causes the flux density to vary enough to appreciably change the amplitude permeability, μ_a, the transformer is not in low-level operation. So the design procedure used was the one given for power transformers in the Linear Ferrite Magnetic Design Manual.[12]

The first step in the design procedure was to chose M, the ratio of the primary current, I_p, to the magnetizing current, I_m (Figure 18). For efficient use of the core, a high value for M was chosen.

$$M = I_p/I_m = 20 \ . \tag{38}$$

Also, as M is increased, the peak flux density is lowered; this improves the linearity of the transformer.



LEGEND:

R_p	resistance of the primary winding
R_s	resistance of the secondary winding
E_p	primary voltage
E_s	secondary voltage
n	the ratio E_p/E_s
L_m	inductance of the primary winding
I_m	magnetizing current
R_c	lumped resistance to account for core losses

Figure 18. Equivalent circuit of the transformer.

Next, the secondary current, magnetizing current, primary voltage, primary inductance and a design constant related to the power handling capability of the transformer, k_2, must be calculated.

$$I_{s\ rms} = E_{s\ pk} * \sqrt{2} * 2\pi f * C_{load} , \tag{39}$$

$$I_m = I_s/(n*M) , \tag{40}$$

$$E_p = n * E_s , \tag{41}$$

$$L_m = \frac{E_{p(pk)} \cdot \sqrt{2}}{2\pi f I_M} , \tag{42}$$

$$k_2 = \frac{(E_p \cdot \sqrt{2})^2}{L_m \cdot f^2} . \tag{43}$$

The core is chosen by comparing the k_2 value obtained from Eq. 43 to values listed for the cores. After a core is chosen, the values for the effective core area, A_c, and the effective core length, l_e, are used to compute a new design constant, k_1. The design constant k_1 was derived by solving Eq. 44 for N_p and substituting it into Eq. 45 for N_p and solving the resulting expression for B, Eq. 46.

$$B = \frac{E_p \cdot 10^8}{\sqrt{2} \cdot 4.44 \cdot f \cdot N_p \cdot A_e} , \tag{44}$$

$$L_m = 0.4\pi N_p^2 \mu \left[\frac{A_e}{\ell_e}\right] \cdot 10^{-8} , \tag{45}$$

$$B = \frac{2.525 \cdot 10^3 \cdot E_p \sqrt{\mu}}{f \sqrt{2 L_m V_e}} , \tag{46}$$

Then,

$$B = k_1 \sqrt{\mu} , \tag{47}$$

where,

$$k = \frac{2500\ E_p}{f \sqrt{2 L_m V_e}} . \tag{48}$$

Using the graph of μ_a versus B for the 3C8 ferrite material and Eq. 49 the flux density can be chosen so that the permeability is near the value for the material at this flux density.

$$\mu = \frac{\beta^2}{k_1^2} . \tag{49}$$

Once the flux density is known, the number of primary turns can be found by rearranging Eq. 44. Neglecting the resistance of the windings and connecting cable, the number of turns in the secondary winding is just N_p/n.

Since this design procedure only applies directly for single frequency transformers, the implementation of the transformer was calculated at 50 kHz. From Eq. 44, it can be seen that doubling the frequency halves the flux density and vice versa. To provide for as linear

operation as possible, the flux density was kept below 1000 Gauss. The highest flux density occurs when the frequency is 25 kHz. The following equations were used to find I_m and I_p.

$$I_m = \frac{E_p}{2\sqrt{2}\ \pi f L_m} . \tag{50}$$

$$I_p = \frac{I_s}{n} - I_m . \tag{51}$$

The negative sign in Eq. 51 results from I_s being capacitive and I_m being inductive. Eventually, the design was finalized (Table 1).

$$N_p = 11 \text{ turns} .$$
$$N_s = 88 \text{ turns} .$$
$$E_p = 25\ V_{pk} .$$
$$E_s = 200\ V_{pk} .$$
$$n = 1/8 = 0.125 .$$

Table 1. Calculated Values for the 1:8 Step-up Transformer.

	25 kHz	50 kHz	100 kHz	units
$I_{s\ rms}$	0.111	0.222	0.444	A
B	680	340	170	Gauss
$\mu(B(f))^{13}$	3700	3400	3200	
L_m	726	667	628	μH
$I_{m\ rms}$	155	84.4	44.8	mA
$I_{p\ rms}$	0.733	1.69	3.51	A

3.2.2 Design of the Inductors

The purpose of having a set of inductors in parallel with the transformer is to improve efficiency by storing some of the energy reflected from the load and returning it to the load on the next cycle. This is accomplished by choosing the inductor so that it resonates with the effective capacitance of the load at or near the frequency of the signal. Since the frequency spans a range from 25 kHz to 100 kHz one or two inductors will not adequately cover the entire range. Consequently, a set of four inductors, with carefully chosen values are switched in or out of the circuit to generate a set of 15 inductance values. The use of four inductors provides sufficient coverage of the frequency band to limit the current consumption to below 700 mA at the worst case switching frequency. Over most of the band, the current that the power transistors have to supply is less than 300 mA.

3.2.2.1 Choosing the inductors' values

Choosing the inductors, L1, L2, L3 and L4, was done with the help of the second program in Appendix C, 4LPICKERfinal. The lowest and highest resonant frequencies were chosen to be 30 kHz and 95 kHz respectively. This sets the values of the largest inductor, L1, and the value of the parallel combination of all four inductors. Hence, the minimum value of the second largest inductor is,

$$L2min = \frac{3}{\left(\frac{1}{L1 \| L2 \| L3 \| L4} - \frac{1}{L1}\right)} . \qquad (52)$$

By choosing L2 and L3, given L1 and the minimum value L1 ‖ L2 ‖ L3 ‖ L4, the value of L4 can be determined. The program steps through certain combinations of L2 and L3 and takes an error measurement over the frequency range of the amplifier. The lowest error is remembered, and the values for the inductors at the lowest error are printed out.

Optimum Inductor Values

L1	87.9 μH
L2	41.0 μH
L3	33.0 μH
L4	20.8 μH

The optimum frequency to switch to the next inductor combination is the frequency where the magnitude of the amplifier's current, I_{AMP} (Figure 7, p. 26), is the same for the next inductor combination as for the existing inductor combination. These switch frequencies were also computed by the program 4LPICKERfinal and listed along with the control codes in Appendix C. This frequency,

$$Fswitch(m) = \frac{1}{2\pi}\sqrt{\frac{L_{res}(m) + L_{res}(m+1)}{2 \cdot L_{res}(m) \cdot L_{res}(m+1) \cdot \frac{C_{load}}{n^2}}}, \qquad (53)$$

where:

Fswitch is the optimum frequency to switch from inductor combination m to inductor combination m+1,

$L_{res}(m)$ is the inductance of inductor combination m,

$L_{res}(m+1)$ is the inductance of inductor combination m+1,

m is the number of the frequency band of interest (1-15),

n is the ratio of the primary voltage to the secondary voltage of the transformer, and

C_{load} is the capacitance the load represents to the amplifier.

The maximum amplifier current for each switching frequency was calculated by program 4LPICKERMAX4 using Eq. 54 (Appendix C).

$$I_{amplifier}(m,f) = \frac{E_p}{2\pi f}\left(\frac{1}{L_m} - (2\pi f)^2 \frac{C_{load}}{n^2}\right) . \qquad (54)$$

3.2.2.2 Designing the inductors

After the inductors' values were chosen and their maximum current had been calculated, the task of designing the inductors was at hand. The first step was deciding on an appropriate material for use in the cores. After a brief survey of the different materials available, the readily available iron powder cores of Micrometals, Inc. were chosen. Since at different frequencies the flux density will be different, the core's effective permeability will not remain constant. In order to minimize the variation in the inductance with frequency, an ultra-stable medium permeability mix was chosen. This mix is designated 8/90 by Micrometals, Inc.

The next step in the design of the inductor's was to develop an equation to model the rise in the effective permeability due to an increase in the flux density. This equation was found by curve fitting Eq. 55 to the graph for mix 8/90 of percent initial permeability ($\%\mu_o$) versus flux density, B.[14]

$$\%\mu_o = 1 + k = 1 + C_1 \log\beta + C_2(\log\beta)^2 + C_3(\log\beta)^{3/2} , \qquad (55)$$

where:

$c_1 = 0.47867,$

$c_2 = 0.28845,$ and

$c_3 = -0.73591.$

Once the increase in the effective permeability could be related to the flux density, the process for calculating the number of turns could begin. First, an appropriate core was chosen. Due to a limited availability, not all inductors used the same core, even though this would have been desirable. Three inductors, L1, L2 and L3, used the optimum core, T184-8/90. The smallest inductor used a close alternative core, T200-8/90. Next, the effective permeability of the core material was assumed to be the same as the initial permeability; i.e., K in Eq. 55 was taken to be zero. Then the number of turns, N, was found from Eq. 56.

$$N = 100 * \sqrt{\frac{L_{desired}}{A_L(1 + K)}} . \qquad (56)$$

Next, the flux density was calculated using the estimated number of turns N for N_p in Eq. 44. With the flux density, K could be found. By using Eq. 56 again, a new N was found. The process of finding a new N, then the flux density, then a new K, which is used to arrive at the next N was iterated until the number of turns was found within a tolerance of a half turn. Since the highest flux density occurs at the lowest frequency an inductor experiences, this was the frequency used for the flux density calculations.

In order to choose the proper wire size, the peak current of each inductor needed to be determined. This was found using Eq. 57.

$$I_{pk} = E_p/(2\pi fL) \ , \tag{57}$$

where:

I_{pk} is the peak current in amps,

E_p is the peak voltage across the inductor,

f is the operating frequency, and

L is the inductance.

A wire size/current chart[15] was consulted, and a conservative choice of wire size was made.

The final specifications of each inductor are summarized below.

L#	$L_{desired}$	N	B_{ac}(max)	I_{pk}	Wire Size (AWG#)
1	88 μH	34	230	1.80	22
2	41 μH	23	225	2.58	20
3	33 μH	21	200	2.59	20
4	21 μH	16	310	3.21	18

The number of turns on each inductor had to be adjusted slightly when the MOSFET switches were included in the circuit. The effect of the MOSFET switches was to reduce the inductance necessary to cause resonance at the desired frequency. Hence, the number of turns on each inductor (except L4) were removed until the correct resonant frequency was achieved. The final number of turns of each inductor are as follows.

L#	N
1	31
2	21
3	18
4	20

3.2.3 Switch Design

There was a need for a fast, reliable method to switch the inductors in and out of the circuit. The first method for switching considered was a simple reed relay. It could operate within 0.5 millisecond, but the long-term reliability of a mechanical relay was questionable. The second design for the switch considered was a double MOSFET switch[16] (Figure 19). It used the integral body diode to achieve bidirectional AC switching. This design was prototyped, and the V_{in} terminal capacitance (switch "off") was measured and found to be about 700 pF. Another design was brought up during a visit by Dr. Thomas A. Lipo, University of Wisconsin (Figure 20).[17] It was also prototyped and its V_{in} terminal capacitance was measured to be near 165 pF. This capacitance will be in series with the inductor when the inductor is switched out of the circuit. The lower the capacitance the more closely the switch resembles an open circuit. Consequently, the single MOSFET switch circuit was chosen over the double MOSFET switch circuit.

In order to allow the source terminal to float as necessary when the switch is "off", the control voltage was changed to a control current, $I_{control}$, by adding a 1 kΩ resistor (Figure 21). By using a current instead of a voltage control, floating supplies or other means of providing a floating voltage source were avoided.

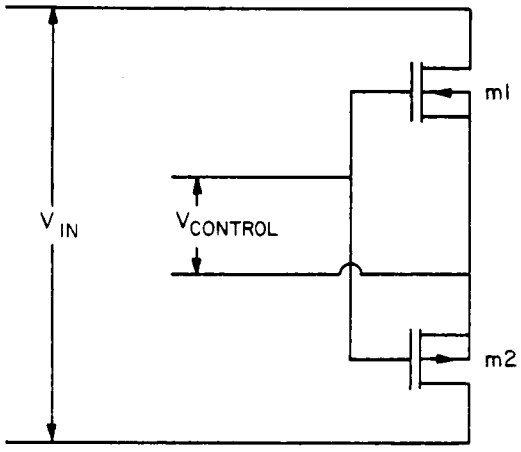


Figure 19. The topology of the double MOSFET switch.

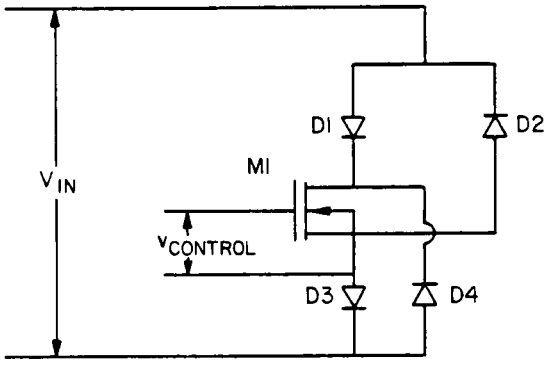


Figure 20. The topology of the single MOSFET switch.

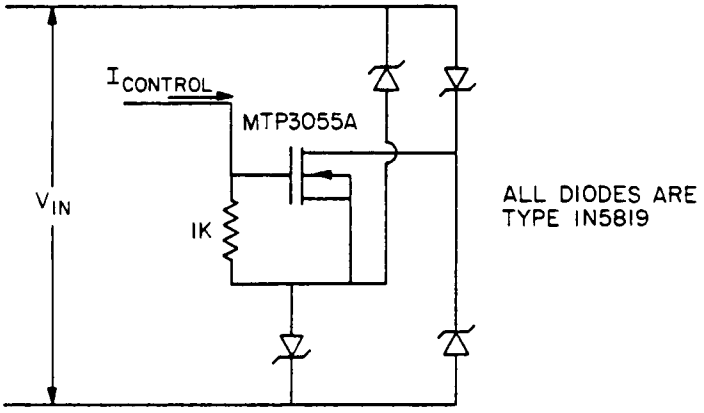


Figure 21. Implementation of the single MOSFET switch.

The 1 kΩ resistor allows a current of 15 mA to fully turn the switch on. This value was chosen because an L.E.D. was to be included in series with the $I_{CONTROL}$ to indicate when the switch is on and between 10 and 15 V are required to fully turn the MOSFET on.[18]

Next the interface circuit was designed (one required for each MOSFET switch) (Figure 22). The interface circuit uses a zener regulated 15 V supply to develop its own 5 V supply (the one 15 V supply is common to all four interface circuits). The 5 V supply is used by the interface circuit to power its opto-isolator and provide pull-up current for the open-collector output of the isolator. When both the open collector output of the opto-isolator and the manually operated switch are open, the pull-up current drives Q2 into saturation. This means that the base of Q1 will be close to 15 V below the 50 V supply. Thus 15 - V_{BE1} will be the voltage across R1. Consequently, $I_{CONTROL}$, the collector current in Q1, will be close to 14.3 mA. This is adequate to produce a large enough voltage across the 1 kΩ gate-source resistor to fully turn "on" the MOSFET (Figure 21).

The voltage at the source of the switching MOSFET will vary during both "on" and "off" conditions. For an input voltage of 25 V_{pk}, the "off" voltage range of the gate will be +0.4 V to -24.6 V. Since the base of Q1 is near 50 V when the switch is "off", the voltage range across the base-collector junction of Q1 is approximately 49.6 V to 74.6 V, which is easily withstood by the 2N3637. When the switch is "on", the current through the MOSFET's source-drain "on" resistance, R_{DS}, develops a relatively appreciable voltage. For a peak switch current of

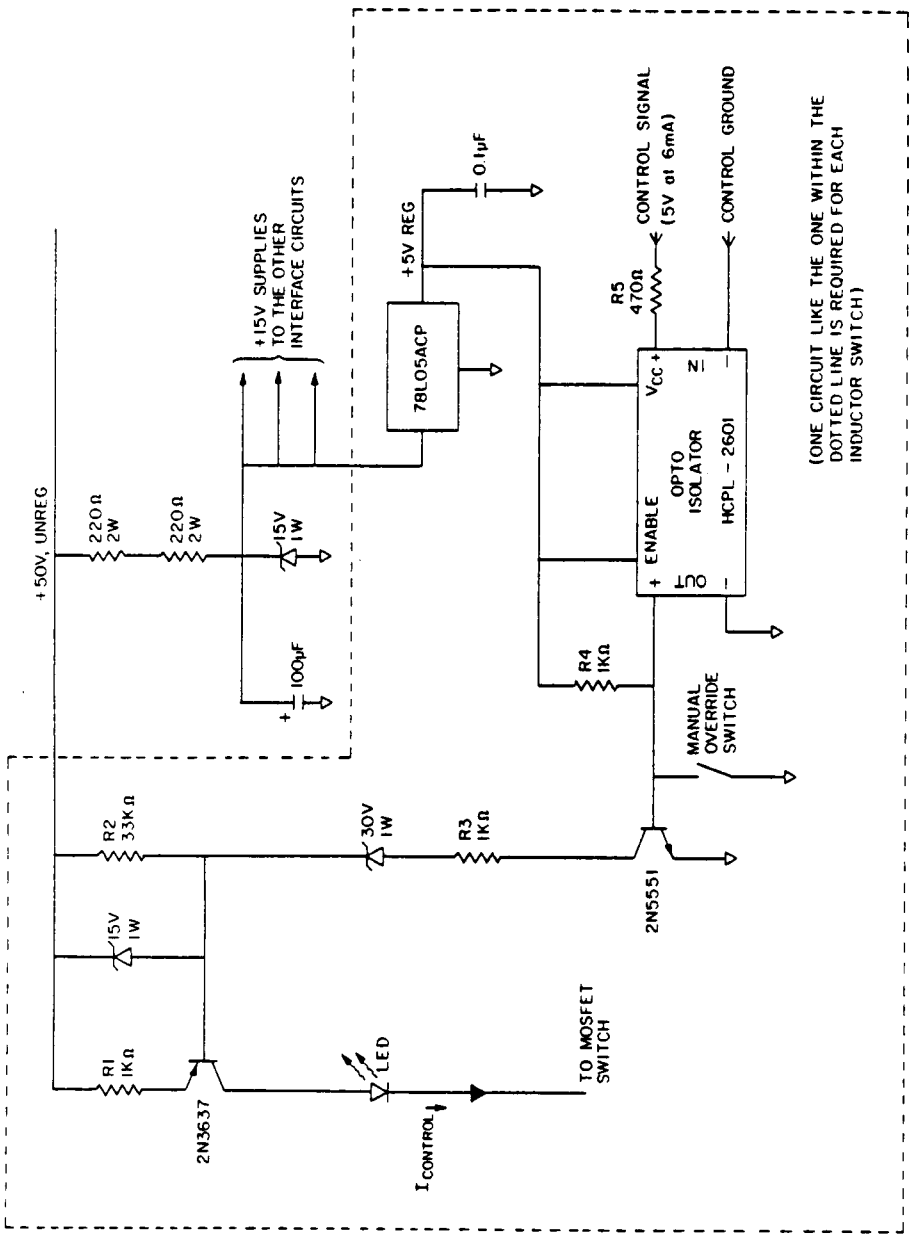


Figure 22. The interface circuit.

2.6 Amps and a maximum R_{DS} of 0.15 Ω, the voltage across the MOSFET will be 0.39 V, roughly equal to the 0.4 V forward drop of the Schottky diodes. Thus, the voltage at the source of the MOSFET will vary from +0.4 V to -0.8 V when the switch in "on". Since the gate is 14.3 V above this value, the gate voltage is between 14.7 V and 13.5 V. Adding 1.6 V for the forward drop of the L.E.D., this puts the voltage of the collector of Q1 between 16.3 and 15.1 V. Thus, the base-collector reverse bias of Q1 of the interface circuit remains between 18.7 and 19.9 V. The power dissipation of Q1 is less than 0.5 mA * 20 V, or 0.3 W, which is well under the power dissipation limit of the 2N3637, which is 1.0 W.

This calculation indicated that the interface circuit would not have problems associated with voltage headroom limitations or power dissipation. True to the theory, the interface circuit/MOSFET switch circuits have worked as they were designed to work. The only difference between the four MOSFET switches is that the switch for inductor L4 has two MOSFET's in parallel for higher current handling capability. The inductor L4 carries the highest current of the four inductors. The paralleling of the MOSFET's results in a lower "on" voltage across the switch and lower power dissipation per device. The temperature rise of each device is roughly the same; hence it was deduced that the current must be dividing virtually evenly between the two MOSFET's.

4. EXPERIMENTAL RESULTS

In this section the characteristics of the prototype amplifier are discussed. Photographs of the input and output signals, as well as some of the more interesting internal signals are also presented. The important external specifications are as follows (Table 2):

Table 2. The Amplifier Specifications

Overall Gain (Amp' and T'former)	400	V/V
Output noise (0 volts input)	< 20	mV_{pk}
Input Impedance	10	kΩ
Output Impedance	5.10	nF
Maximum Output Voltage	230	V_{pk}
Frequency Range	25-100	kHz
Inductor Control Levels	5	mA @ TTL
Power Lockout Control	50	mA @ 5 V

The input and output signals were photographed with the amplifier at full power, 200 V_{pk}, at a mid-band frequency, 50 kHz (Figure 23).

The transient response of the amplifier to tone bursts is important, particularly the cut-off transient. No ringing should be present after the input signal is removed. The amplifier exhibits a rapid response to the cut-off of the signal, and there is no observable ringing (Figure 24). The feedback loop helps de-energize the resonant tank formed by the inductors, the transformer and the capacitive load.

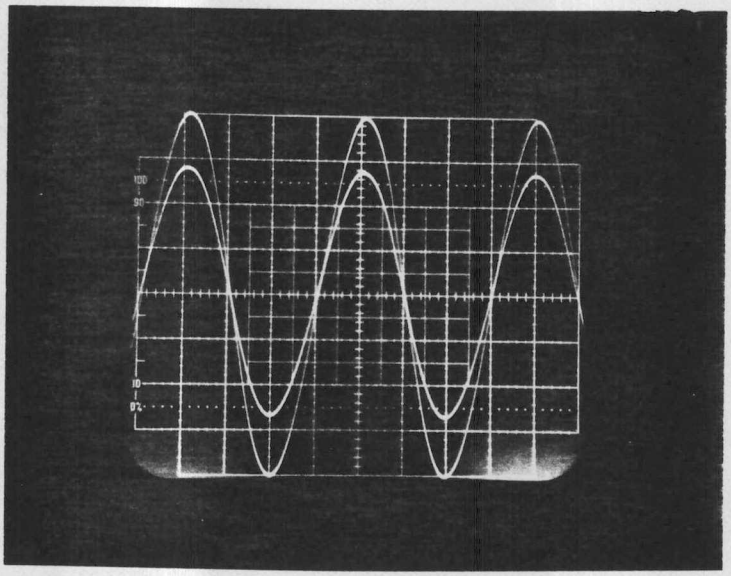


Figure 23. Input and output of the amplifier system. Signal frequency is 50 kHz; horizontal scale is 5 μsec/div. Larger trace is the output signal measured at the load at 50 V/div. Small trace is the input signal at 200 mV/div.

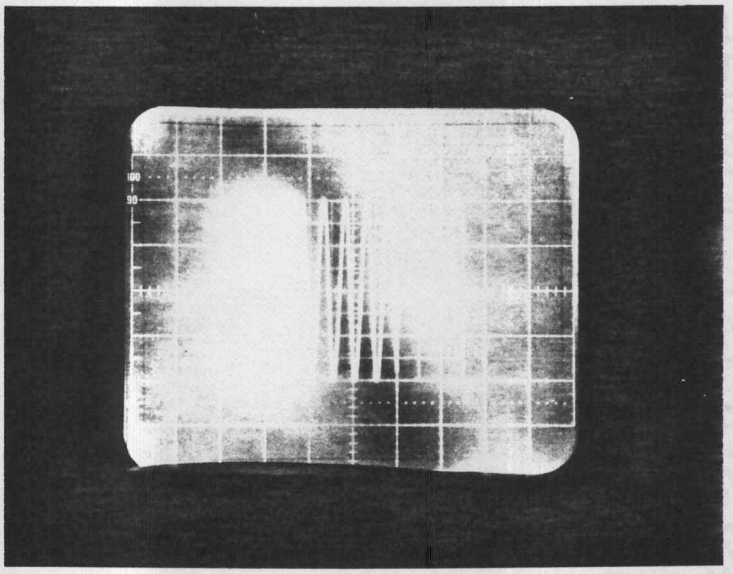


Figure 24. Output of the amplifier system showing the rapid transient which occurs at cut-off of the signal. Signal frequency is 50 kHz; horizontal scale is 5 μsec/div., then 20 μsec/div. Signal is measured at the load; vertical scale is 50 V/div. (Small divisions on both horizontal and vertical scales.)

From the photograph of the input and output signals of the discrete gain stage it can be seen that the actual gain is about -17.3 V/V (Figure 25). The DC offset is about +5 V; this is primarily the sum of the V_{BE}'s of Q5 and Q8 and the V_T of the N-channel MOSFET, Q12.

The MOSFET switches play an important role as the means of quickly and reliably switching the inductor combinations to match the input frequency. An oscillograph was taken of the voltage at the junction of an inductor and a MOSFET switch for the switch "off" and for the switch "on", respectively (Figures 26 and 27). The "off" state voltage does not suggest anything unexpected is occurring. The "on" state voltage trace shows the voltage drops across the Schottky diodes and the internal voltage drop due to R_{DS}. The rounded dome-like part of the waveform is the result of the voltage drop due to R_{DS}. Since the current through the inductor is a sine wave, the voltage across the almost constant R_{DS} is close to a sine wave too.

The next two oscilloscope photographs are of the gate-source voltage of the MOSFET in one of the inductor switches. The turn-on time is about 20 μsec (Figure 28). The turn-off time is about the same, 20 μsec (Figure 29). Considering that these times are within the same order of magnitude as a single period of the signals in the passband, these times were considered acceptable.

The next series of oscilloscope photographs show the currents of an inductor, I_L, the transformer, I_{TRAN}, and of the amplifier, I_{AMP} (Figures 30, 31 and 32). In all these photographs, the large sine wave is the output voltage and is intended to be a reference when observing the

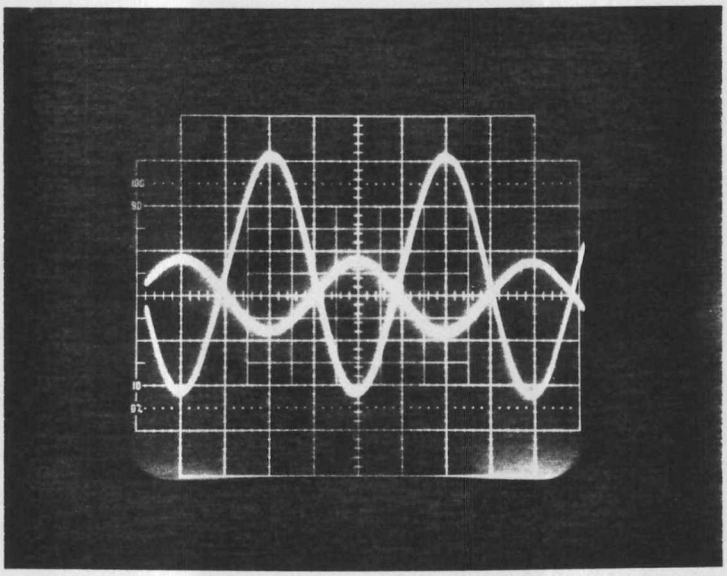


Figure 25. Input and output signals of the discrete gain stage. Signal frequency is 50 kHz; horizontal scale is 5 μsec/div. Larger trace is the output of emitter follower Q5, at 10 V/div. Small trace is the input signal at the base of Q1, v_{01}, at 2 V/div. (AC coupled.)

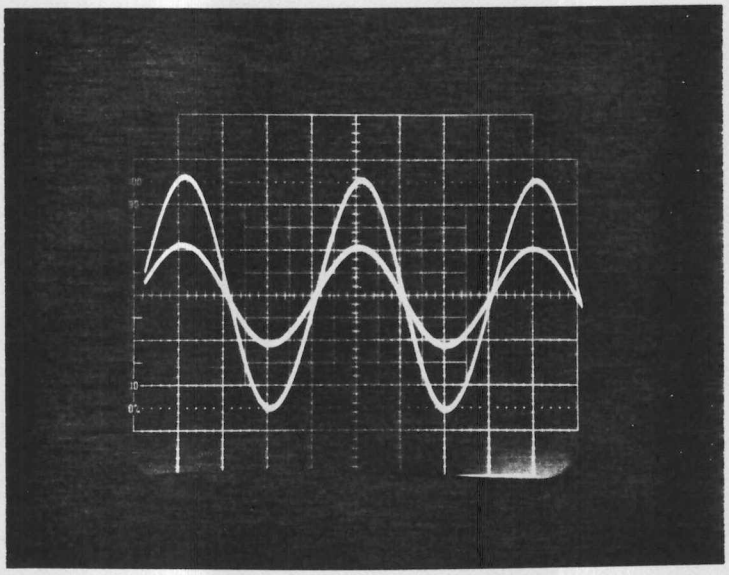


Figure 26. Waveform at junction of inductor and MOSFET switch with the switch "off". The larger trace is the switch waveform at 10 V/div. Signal frequency is 50 kHz; horizontal scale is 5 μsec/div. Small trace is the input signal to the amplifier system at 500 mV/div.

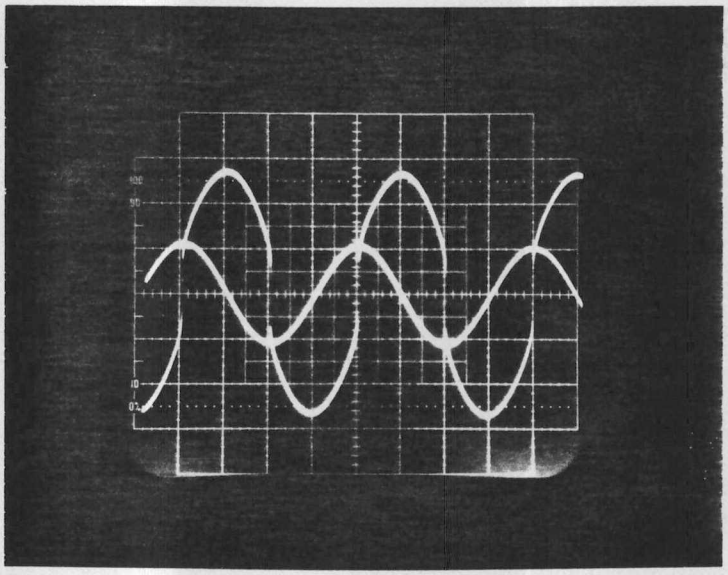


Figure 27. Waveform at junction of inductor and MOSFET switch with the switch "on". The larger trace is the switch waveform at .5 V/div. Signal frequency is 50 kHz; horizontal scale is 5 μsec/div. Small trace is the input signal to the amplifier system at 500 mv/div.

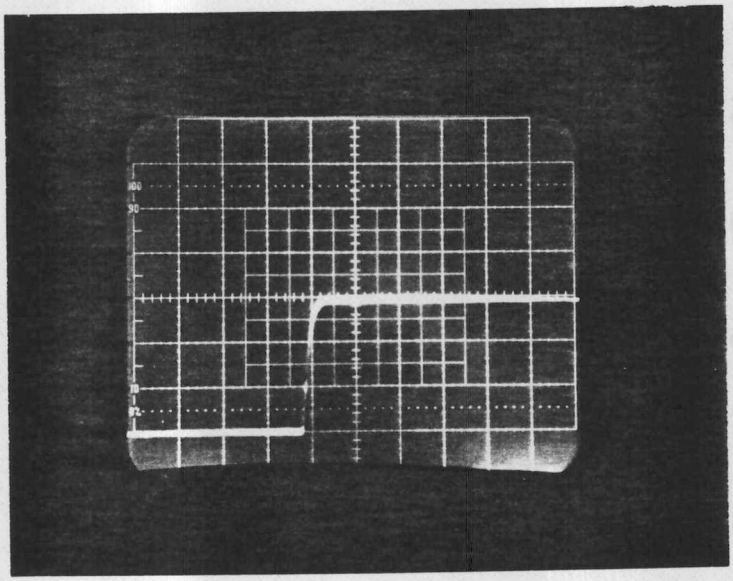


Figure 28. V_{GS} of MOSFET of one of the inductor switches turning "on". Vertical scale is 5 V/div.; horizontal scale is 50 μsec/div.

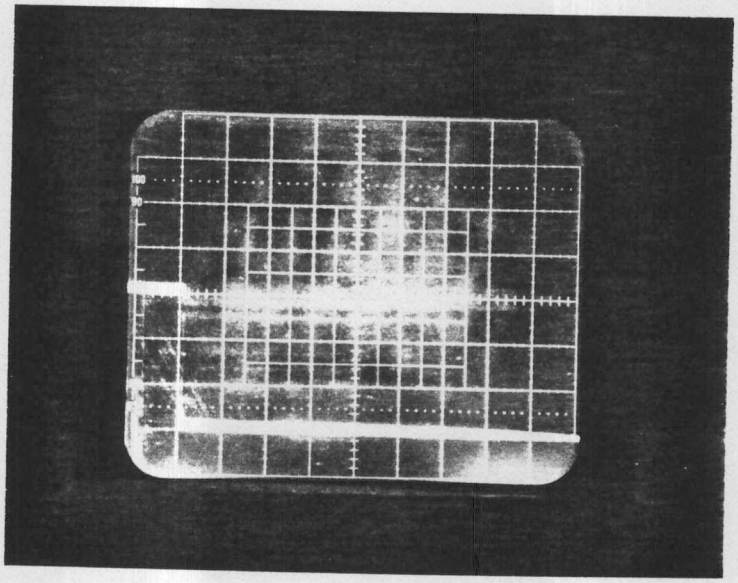


Figure 29. V_{GS} of MOSFET of one of the inductor switches turning "off". Vertical scale is 5 V/div.; horizontal scale is 100 μsec/div.

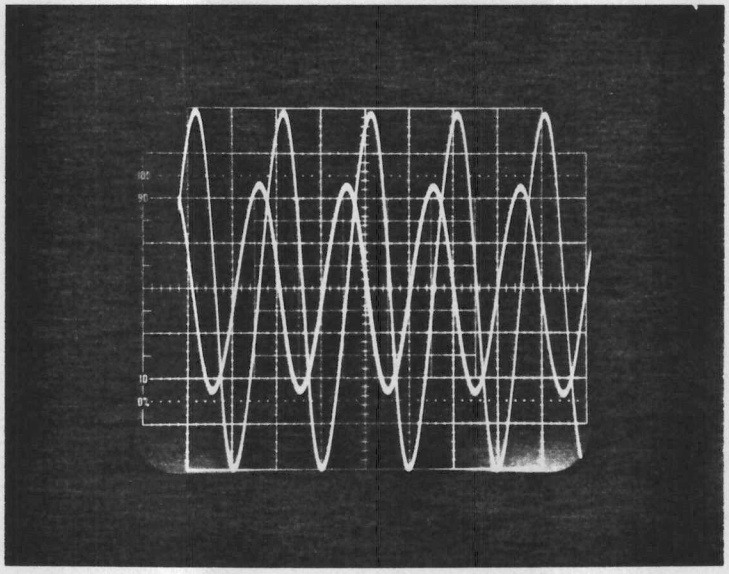


Figure 30. The inductor current, I_L, at full power. Signal frequency is 50 kHz; horizontal scale is 10 μsec/div. Larger trace is the amplifier output measured at the load at 50 V/div. Small trace is the current into the inductor at 1 A/div.

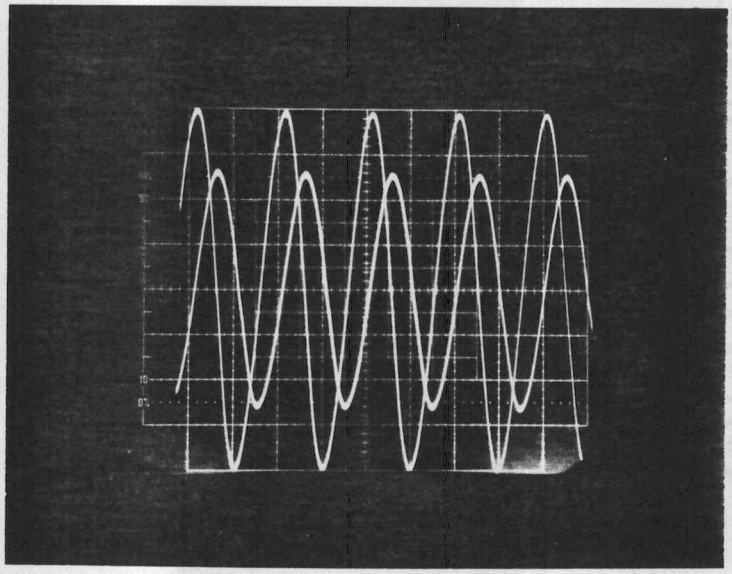


Figure 31. The transformer current, I_{TRANS}, at full power. Signal frequency is 50 kHz; horizontal scale is 10 μsec/div. Larger trace is the amplifier output measured at the load at 50 V/div. Small trace is the current into the transformer at 1 A/div.

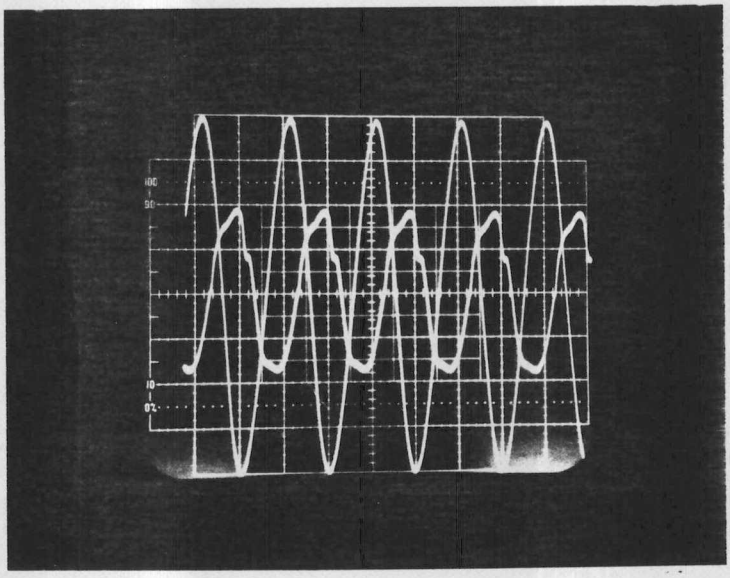


Figure 32. The amplifier current, I_{AMP}, at full power. Signal frequency is 50 kHz; horizontal scale is 10 μsec/div. Larger trace is the amplifier output measured at the load at 50 V/div. Small trace is the current out of the amplifier's output stage at 0.2 A/div.

phases of the various currents. The inductor's current is 90° behind the output voltage.[19] The transformer's current is 90° ahead of the output voltage. The sum of the two currents is the current of the amplifier, I_{AMP}. The amplifier's current does have a low level oscillation imposed upon it. This oscillation is not manifested in the output signal.

5. CONCLUSIONS

In this section, the features of the design, the primary limitation of the design and the related design decisions, of the amplifier system are discussed. Also, the cases where the calculations did not agree with the observed behavior of the circuit are discussed; then, lastly, suggestions for further study are given.

The features of the amplifier system are

1) The output voltage is a low distortion sine wave,

2) The transient response to tone bursts is good,

3) The power consumption is low, and

4) The interface circuit makes the amplifier easy to control.

The output voltage is a sine wave which exhibits no visible distortion. The three factors responsible for this achievement are a low distortion forward path, a moderate loop transmission in the feedback, and a nearly linear transformer. During the design phase, nothing was done to improve the linearity of the current gain stage; and, of course, nothing was done to the monolithic op-amp to improve its linearity. However, the common emitter, Q1, in the discrete gain stage was considered to be a possible source of distortion, and hence, a gain degeneration resistor, R5, was included in the topology of the stage. When measured, the discrete gain stage exhibited only minor distortion, and the current gain stage had no visible distortion.

By keeping the degree of distortion low in the forward path of the amplifier, the desired reduction in distortion can be achieved with a

lower magnitude of loop transmission. This is desirable since a high loop transmission can make the amplifier less stable and may require complicated compensation.

Once the signal has propagated through the amplifier and has suffered only minor distortion, it must still pass through the transformer. Thus, the transformer was designed to operate at a low flux density, in the region where the effective permeability of the material is nearly constant. As designed, the transformer exhibits very little distortion. Consequently the signal arrives at the load with no visible distortion.

Another feature of the amplifier system is its transient response to a tone burst. The amplifier must reach full power on the first cycle of the signal and then drop to zero volts output, with no ringing, when the burst is finished. In order to achieve full power, the resonant tank must be fully energized; hence, the first cycle of a tone burst must fully energize the tank circuit. Similarily, after the last cycle of a tone burst, the amplifier must remove all the energy from the resonant tank. To achieve this, the feedback loop is assisted by large capacitors, C18 and C19, on the power supplies to the output stage. When the feedback senses the error that occurs between the output and input voltages at the beginning of a tone burst, the error signal is amplified around the feedback loop and tries to energize the resonant tank. The capacitors supply the large surge of charge necessary to energize the resonant tank. A similar chain of events occurs at the end of the tone burst when the stored energy in the resonant tank tries to

keep ringing after the input signal has been removed. The feedback amplifies the error and the capacitors, C18 and C19, supply the charge to neutralize the energy in the resonant tank.

Another section of the design of the amplifier that worked exactly as planned was the interface and MOSFET switch circuits. The interface circuit was planned to provide signal and ground isolation from the system controller, provide a floating voltage for controlling the inductor switches, and to allow for manual control of the inductor switches during testing and development. The isolation was achieved with opto-isolators and the manual control was accomplished by a "wire-ANDing" of the DIP switches and the open-collector outputs of the opto-isolators. The floating control voltage was discussed in the section on the switch design.

The basic and primary limitation of the amplifier system is that only frequencies near to each other can be continuously amplified simultaneously. This constraint was not important for the system which utilized the amplifier. If two frequencies are applied to the amplifier simultaneously and they are not in the same frequency band, the current from the selected inductance and the capacitive load will not cancel each other for both frequencies. When the currents do not cancel each other, the amplifier must supply the balance. This reactive current can be quite large, and resistor R_s may not be able to safely carry it. This condition is worse for the frequency bands at either end of the passband. But even for these worst-case bands, if the duty cycle of the signal is low enough, the amplifier can safely handle simultaneous transmission of two signals widely separated in frequency.

There were three areas where the calculations and expectations did not match the results in the laboratory:

1) The first design of the discrete gain stage was to achieve a higher output voltage using smaller transistors,

2) The temperature of the output transistors is lower than predicted by the calculations, and

3) The number of turns on the three larger inductors had to be reduced when the MOSFET switches were added to the circuit, but the number of turns on the smallest inductor had to be increased.

When the discrete gain stage was first designed, small signal transistors (plastic TO-92 package) were used which could not dissipate the heat, even with heat sinking. The problem was that one of the transistors would overheat before the bias point could be adjusted to the desired operating point. After two attempts, which resulted in thermally induced failure of the transistors, the larger transistors (TO-202 metal fin packages) were acquired and a less sensitive design was done. Perhaps metal can TO-92 transistors could have been used successfully, but the TO-202 metal fin packages discharged the heat to the heat sink rapidly enough without being too large. Since time was a precious commodity in this development cycle, no effort was made to try the metal can TO-92 package after the TO-202 transistors were used successfully.

Another discrepancy between the calculations and the actual performance of the hardware is that the temperature of the output transistors is lower than that predicted by the calculations. This can be partially explained since fan-forced cooling air exits the cabinet and

passes over the heat sink, which reduces the thermal resistance of the heat sink.

The third unexpected occurrence was that the number of turns on the smallest inductor had to be increased after the MOSFET switch was included in the circuit. It was expected that the inductance would have to be reduced to achieve resonance after inserting the switch in series with the inductor since the voltage across the inductor would be reduced. To cause the same amount of current to flow through the inductor with a reduced voltage across it, the inductance has to be reduced. The current through the inductor has to be the same magnitude as the current flowing through the capacitor for resonance to occur. Consequently, it was surprising that the number of turns on the smallest inductor, L4, had to be increased, raising the inductance, to achieve resonance at the proper frequency. The only difference between L4 and the other inductors is that it uses a slightly larger diameter core.

5.1 Suggestions for Further Study

The design of the amplifier will have to be modified for further increases in output power capability. The first area to investigate will be the replacement of the monolithic op-amp and discrete gain stage with a high performance op-amp which can drive the emitter follower Q5 directly. The second area to investigate is the cause of the oscillation in the output current of the complementary common drain output stage.

Perhaps it will become necessary to continuously amplify two widely separated frequencies at the same time. If this materializes, then the

use of a single resonant output may not be a viable method of achieving efficiency.

In conclusion, the amplifier did fulfill its requirements. Although not an optimized design with regard to cost, layout, electronic design or maintainablity, the amplifier does drive the transducer array to its highest capacity with much less electronic noise, audible noise, heat, weight or space requirements than a conventional nonresonant amplifier.

This project has been one of the most enjoyable and the most educationally productive the author has ever experienced.

REFERENCES

REFERENCES

1. Dr. T. V. Blalock reported that the resistive component of a single transducer's impedance is 4.5 MΩ.

2. International Rectifier Hexfet Databook, International Rectifier, El Sequndo, California, Third edition, 1985. p. A-12.

3. Power MOSFET Transistor Data, Motorola Semiconductor Products Inc., Phoenix, Arizona, First edition, 1984. p. A-9.

4. International Rectifier Hexfet Databook, International Rectifier, El Sequndo, California, Third edition, 1985. pp. A-58, A-59, A-23, A-25.

5. Power MOSFET Transistor Data, Motorola Semiconductor Products Inc., Phoenix, Arizona, First edition, 1984. p. A-9.

6. Datasheet on MC34080/MC35080 through MC34085/MC35085, Motorola Semiconductor Products Inc., Phoenix, Arizona.

7. Modeling The Bipolar Transistor, Ian Getreu, Tektronix, Inc., Beaverton, Oregon, 1976. p. 30.

8. International Rectifier Hexfet Databook, International Rectifier, El Sequndo, California, Third edition, 1985. pp. A-135.

9. Applied Electronics, J. F. Pierce and T. J. Paulus, Knoxville, TN, 1980. p. 52.

10. Ibid.

11. Linear Ferrite Materials & Components, catalog by Ferroxcube, Saugarities, N.Y., Seventh edition, 1984. p. 1-10.

12. Linear Ferrite Magnetic Design Manual, by Ferroxcube, Saugarities, N.Y.

13. The permeability at the flux density at the given frequency was read from a graph in the Linear Ferrite catalog by Ferroxcube. p. 1-10.

14. Micrometals Iron Powder Cores Catalog 4, Issue D, December 1985, p. 11.

15. Ibid. p. 31.

16. International Rectifier Hexfet Databook, International Rectifier, El Sequndo, California, Third edition, 1985. p. A-67.

17. Design also found in Power Electronics, Richard A. Pearman, Reston Publishing Company, Inc., Reston, Virginia, 1980. p. 72.

18. Power MOSFET Transistor Data, Motorola Semiconductor Products Inc., Phoenix, Arizona, First edition, 1984. p. A-9.

19. There is a phase inversion between the input of the transformer and the output. Hence, the currents appear to be of the wrong phase with respect to the output voltage.

APPENDICES

APPENDIX A

SPICE MODELING RESULTS

Introduction

The modeling of the amplifier centered on modeling the complementary common drain output stage driving a resonant load with feedback connected. First, a model for the power MOSFET's had to be found. The model proposed by Bowers and Nienhaus was used with good success.[1] Next, several simulations of increasing complexity and similarity to the final implementation were done. Simulations of series as well as parallel resonant loads and simulations of above, at and below resonance operation were run. The results of the preliminary survey of various configurations were then confirmed with laboratory work on the more promising designs. In most cases correlation was good; however, occasionally the SPICE analysis would predict an oscillation that was not seen on the bench. After implementation, analysis of the final design was done with results giving good correlation to the experimental results.

Models of the power MOSFET's

The model used by the SPICE-2 program for its MOSFET's was designed to accommodate small-signal devices. By adding certain components to the SPICE-2 MOSFET model, the behavior of a power MOSFET can be fairly accurately modeled.[2] A program was written to perform the calculations for these external components as well as those for the built-in SPICE-2 MOSFET model. The calculations were done for the IRF240 and IRF9240 transistors (Table A1).

Table A1. The Values for the Modified MOSFET Models

Item	IRF240 (N-channel)	IRF9240 (P-channel)	Units
R_L	800	800	kΩ
V_{TO}	3.99	-3.766	V
K_P	23.65	4.225	A/V^2
R_S	0.0584	0.036	Ω
R_D	0.0784	0.276	Ω
C_{GSO}	1115	950	pF
C_{GDO}	160	150	pF
C_{BD}	1734	1147	pF
P_B	1.0	1.0	
I_S	1.0	1.0	fA

Simulation Results

Initially, the DC characteristics of the models for the power MOSFET's were checked. The correlation was excellent. Next, several complementary common drain output stages were simulated with various gate impedances, output loads, and bias schemes. This gave a feel for the operation of the output stage. For the series resonant loads, the results were not encouraging. For the parallel resonant loads, some simulation problems were encountered on the circuits which did not use a feedback loop to keep the output voltage centered around 0 volts. The inductor, being a short circuit at DC, would cause a large current to flow if the output voltage had even a fraction of a volt of DC offset. This problem was also noticed on the laboratory bench.

The final simulation run was of a circuit which contains the output stage, a resonant load operating near resonance and the feedback loop that contains simulated poles where those in the amplifier are expected to be (Figure A1). The SPICE results do agree reasonably well with the laboratory observations. The output voltage is 25.7 V_{pk} for an input of 0.5 V_{pk}. There is no oscillation on the gate current or gate source voltage, and none is observed in the hardware amplifier either. The feedback loop is stable in both SPICE and the hardware unit. The two discrepacies are a oscillation in the hardware unit's amplifier output current, and that the hardware unit's transient time seems to be less than that predicted by SPICE.

First, there is no oscillation in the SPICE's I_{AMP}, IVIO, the current coming out of the amplifier, but there is a small oscillation in the current in the hardware model. It is a mild oscillation and there is no evidence of it in the output voltage; consequently, it has been ignored.

Secondly, comparing the start-up transient of the SPICE model with the photograph of the transient at the end of a tone burst in the hardware unit, it appears that the hardware unit takes one cycle or less to energize or de-energize the resonant tank. The analysis from the SPICE model indicates that about two cycles are required before the resonant circuit is fully energized.

Considering that the actual devices in the hardware model were not measured and their specific parameters given to the simulation program, these slight differences are not surprising. The SPICE analysis did not

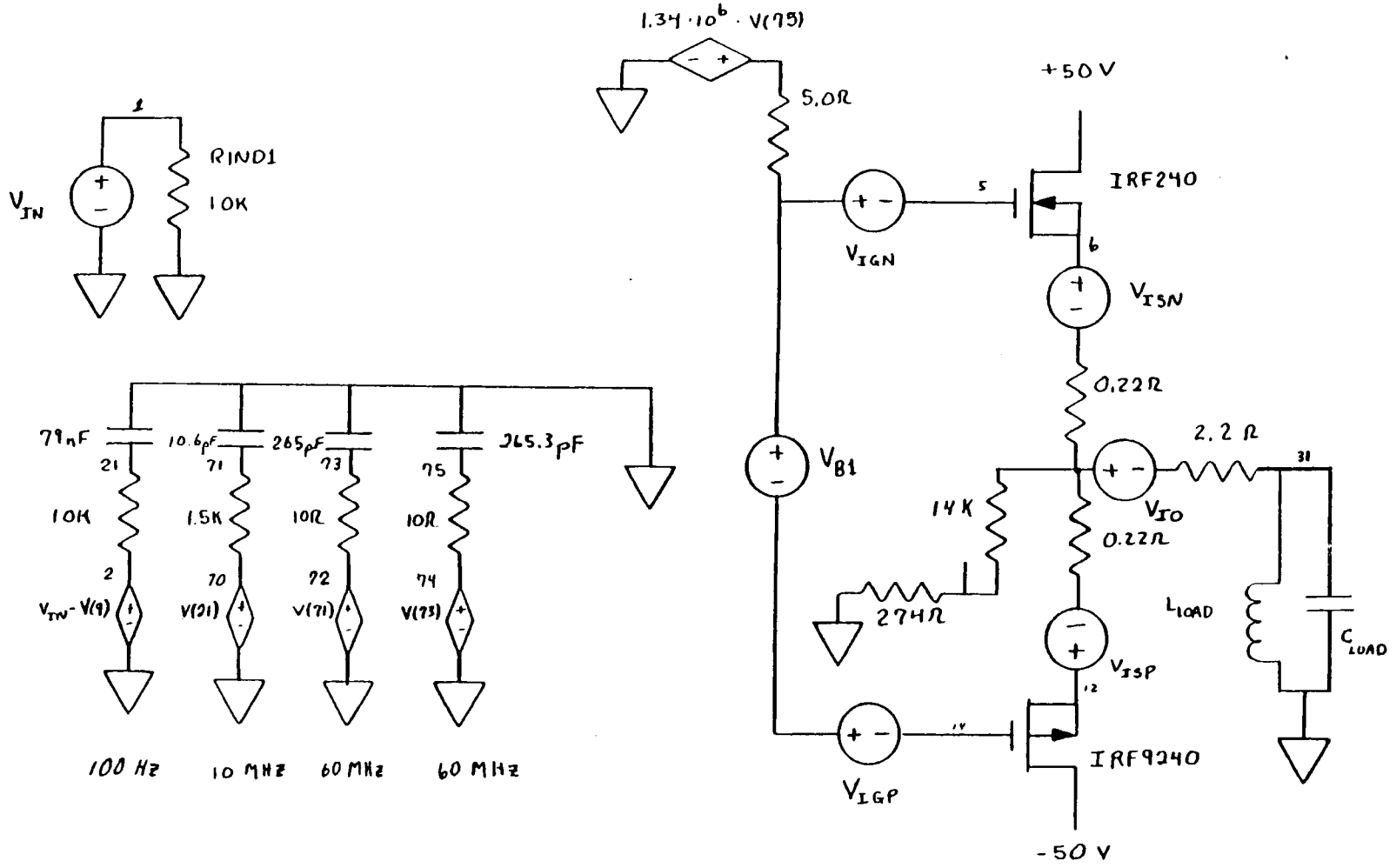


Figure A1. The SPICE model diagram of the output stage, feedback loop, and the resonant load.

indicate that the design was marginal or any other reason to pursue the analysis of the circuit further.

The input listing of the SPICE analysis of the simulation of the feedback loop, the resonant load and the complementary common drain output stage follows.

---

[1] International Rectifier Hexfet Databook, International Rectifier, El Sequndo, California, Third edition, 1985. Pp. A-153 through A-160.

[2] Ibid.

```
********10-29-86******* ALLSPICE (2.11) 07/18/86
*******18:11:26*******

FULL COMPLEMENTARY COMMON DRAIN 1

****      INPUT LISTING                          TEMPERATURE =   27.000 DEG
C

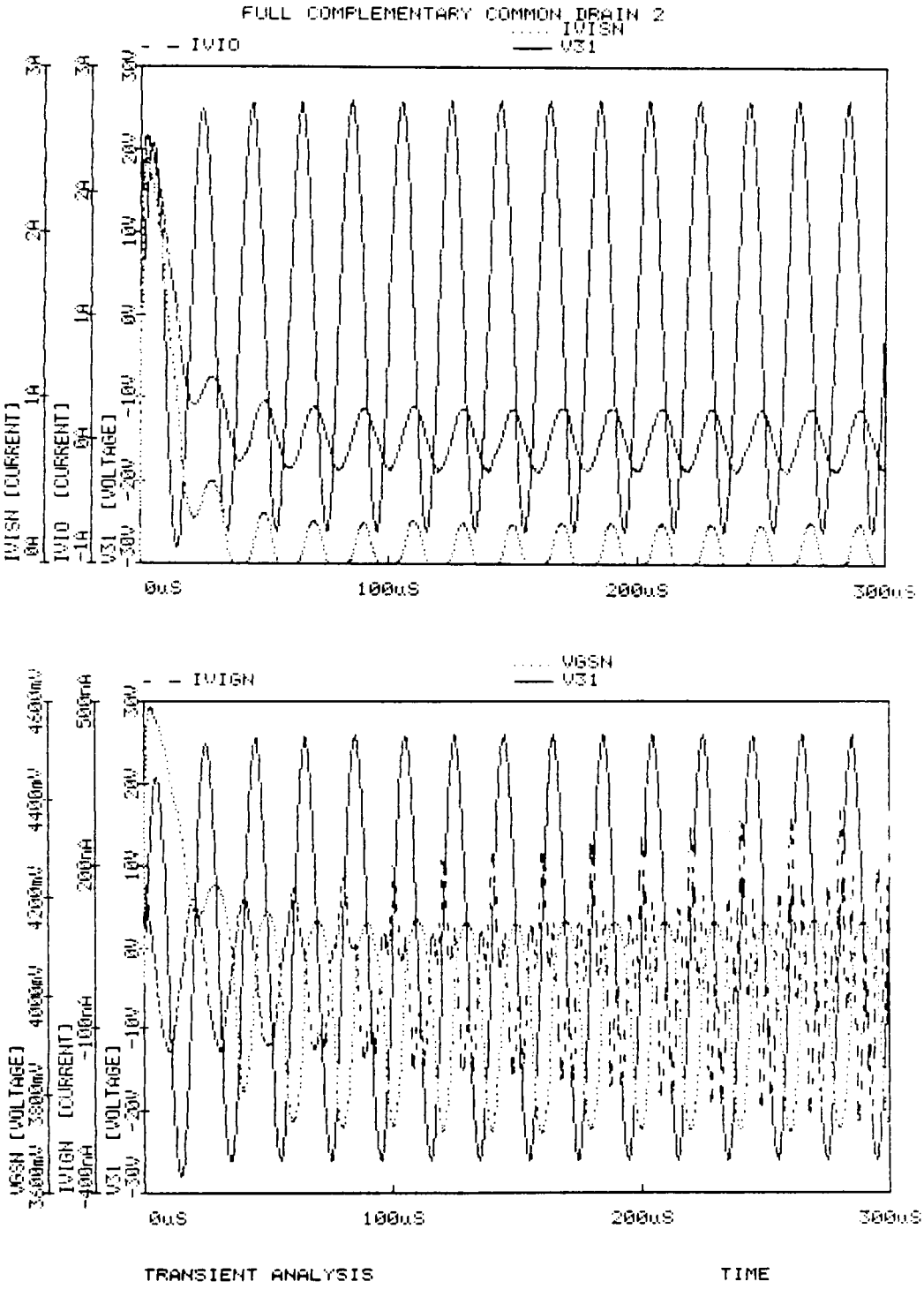
******************************************************************************


 .WIDTH IN=80 OUT=80
 .SUBCKT IRF640 10 20 30
MOS 10 1 30 30 MOSFET
 RG 20 1 51
 RL 10 30 800K
 .MODEL MOSFET NMOS VTO=3.99 KP=23.65 RS=.0584 RD=.0745 CGSO=1115P
 +CGDO=160P CBD=1734P PB=1.0 IS=1.0F
 .ENDS
 .SUBCKT IRF9640 10 20 30
MOS 10 1 30 30 MOSFET
 RG 20 1 33
 RL 10 30 800K
 .MODEL MOSFET PMOS VTO=-3.766 KP=4.225 RS=.036 RD=.276 CGSO=950P
 +CGDO=150P CBD=1147P PB=1.0 IS=1.0F
 .ENDS
 VCC 99 0 50
 VEE 98 0 -50
 X1 99 5 6 IRF640
 X2 98 14 12 IRF9640
 *
 VIN 1 0 SIN(0.0 .50 50000 0.0 0.0)
 RIND1 1 0 10K
 *THE OPAMP COMPARATOR AND POLE
 RINDUMMY 2 21 10K
 CINDUMMY 21 0 79.577E-9
 EOPAMP1  2 0 1 9 1
 *RINDIMMY AND CINDUMMY ESTABLISH THE 100 HZ POLE
 *
 *THE OPAMP GAIN AND OUTPUT: GAIN IS 80,000*16.85
 EOPAMP 3 0 21 0 1.3477E6
 *
 RDRIVEROUT 3 4 5
 *THE GATE DRIVER'S OUTPUT IMPEDANCE IS APPROX. 5 OHMS
 *
 VBIAS1 4 13 7.9
 *THE BIAS BETWEEN THE GATES OF THE MOSFETS
```

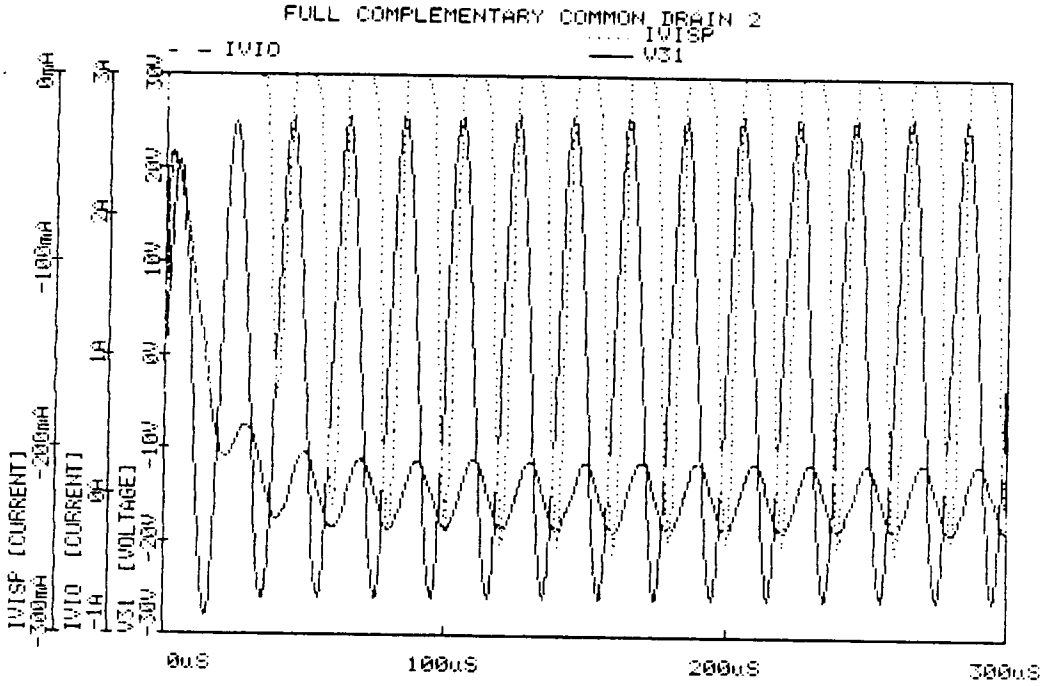
```
*
*THE CURRENT METERS
VIGN 4 5 0
*THE GATE CURRENT FOR THE N-CHANNEL
VIGP 13 14 0
*THE GATE CURRENT FOR THE P-CHANNEL
VISN 6 7 0
*THE SOURCE CURRENT FOR THE N-CHANNEL
VISP 12 11 0
*THE SOURCE CURRENT FOR THE P-CHANNEL
VIO  8 10 0
*THE LOAD CURRENT
*
RSN  7 8 .22
RSP  11 8 .22
*THE SOURCE RESISTORS
*
RF1  8 9 14K
RF2  9 0 274
*THE FEEDBACK RESISTORS
*
RLOAD 10 31 2.2
CLOAD 31 0 320E-9F
LLOAD 31 0 26.1UH
*THE LOAD
.TRAN 1US 500US
*.PRINT TRAN I(VIGN),I(VIGP),I(VISN),I(VISP),I(VIO),V(1),V(3),V(5)
+V(14),V(10),V(9)
.PLOT TRAN V(31),I(VIGN),I(VISN),I(VIO),V(5,6)
.PLOT TRAN V(31),I(VIGP),I(VISP),I(VIO),V(14,12)
.OPTIONS LIMPTS=2000 ITL5=10000
.END
```

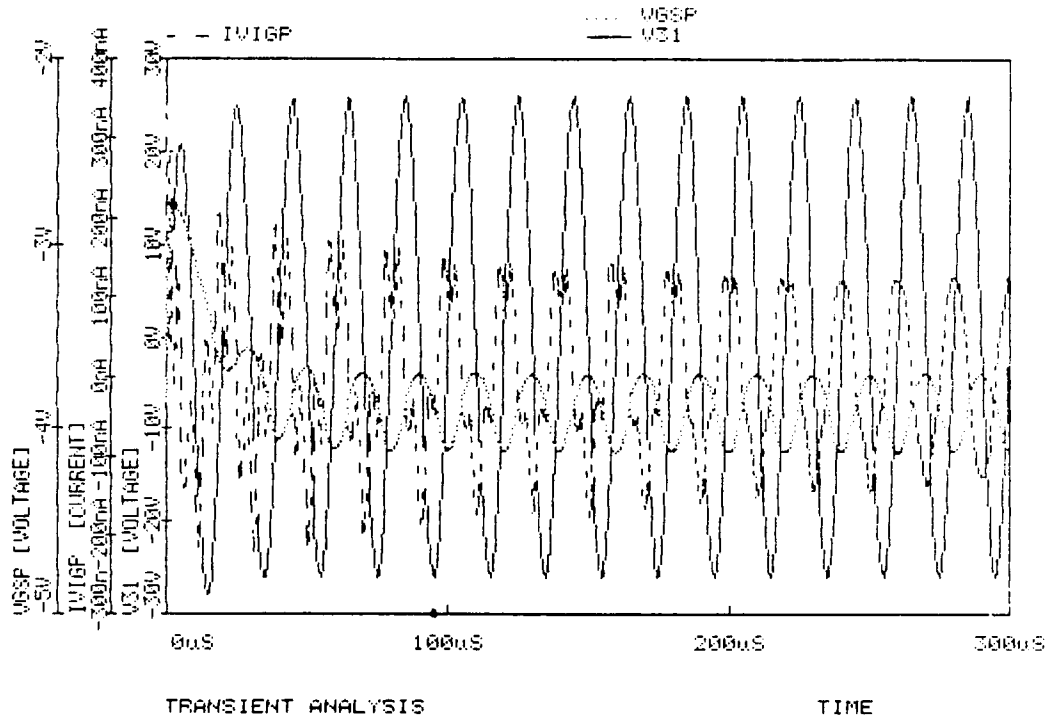
Four plots of the results of this simulation follow:

N-CHANNEL RESULTS:



P-CHANNEL RESULTS:





APPENDIX B

PROGRAMS USED IN DESIGN OF THE AMPLIFIER

TRUEFMR1 a program in True Basic for designing transformers, this version does not contain the high frequency cut-off, or the winding area calculations, which were deemed unnecessary after the first two transformers had been built and tested.

```
REM N is the #pri/#sec
REM Lm, the primary winding's inductance
REM B is the flux density
REM the current that must flow to establish B is Im
REM the primary current Ip = sqrt( secondary current/N squared plus
REM the square of the magnetizing current , Im
REM Ap is the available winding space
REM Ep is the primary voltage, Es is the secondary voltage
REM Is is the secondary current
REM turns/square inch = Np/Ap where Np is the number of primary turns
REM Rp, primary resistance = MLT (Mean Length of Turn) * resistance/length
REM Lt is the leakage inductance
REM Ct is the self-resonating capacitance
REM F2 is the high frequency cut-off
REM F is the operating frequency
REM Cload is the load capacitance
REM M is the ratio of the load component of Ip to the magnetizing current, Im
REM Ae is the effective core area
REM le is the effective core length
REM Ve is the effective core volume
REM Al is the inductance index, in mH per 1000 turns

REM CLS
SET CURSOR 1,1
PRINT"CLOAD ="
PRINT"FREQ ="
PRINT"N = "
PRINT"M = "
PRINT"ES = "
PRINT"IS = "
```

```
PRINT"IM = "
PRINT"EP = "
PRINT"LM = "
PRINT"K2 = "

SET CURSOR 12,1
INPUT PROMPT "enter the core type data, etc.":type$
PRINT " "
SET CURSOR 14,1
PRINT type$

LET Cload = 5E-09
LET F = 100000                    !
LET n=1/8
LET m=20
LET Es = 200                      ! the secondary voltage in Volts peak

REM find Is, Im, Ep, Lm, k2
LET Is = Es*.707*f*2*pi*Cload

LET Im = Is/(n*m)

LET Ep = n* Es

LET Lm = Ep*.707/(2*pi*f*Im)

LET k2 = (Ep*.707)^2/(Lm * f^2)

SET CURSOR 1,7
PRINT Cload
SET CURSOR 2,7
PRINT f
SET CURSOR 3,7
PRINT n
```

```
SET CURSOR 4,7
PRINT m
SET CURSOR 5,7
PRINT Es
SET CURSOR 6,7
PRINT Is
SET CURSOR 7,7
PRINT Im
SET CURSOR 8,7
PRINT Ep
SET CURSOR 9,7
PRINT Lm
SET CURSOR 10,7
PRINT k2

REM ask for the core specific data

DO
   SET CURSOR 12, 1
   INPUT PROMPT" Enter Ae, le for the core selected":Ae,le
   LET Ve = Ae * le
   SET CURSOR 12,1
LOOP UNTIL   Ve <>0
PRINT " "
SET CURSOR 1,20
PRINT"AE ="
SET CURSOR 1,27
PRINT Ae
SET CURSOR 2,20
PRINT "le ="
SET CURSOR 2,27
PRINT le
LET k1 = 2500*Ep*.707/(f*SQR(Lm*Ve))
```

```
SET CURSOR 3,20
PRINT "k1 = "
SET CURSOR 3,27
PRINT k1
DO
   SET CURSOR 4,20
   PRINT"B ="
   SET CURSOR  12,1
   INPUT PROMPT"input B to get μ, else 0.00 to quit":Bnew
   IF bnew<>0 THEN LET b=bnew
   SET CURSOR 4,27
   PRINT b
   LET littlem = (b/k1)^2
   SET CURSOR 5,20
   PRINT"μ="
   SET CURSOR 5,27
   PRINT littlem
LOOP UNTIL  bnew = 0
SET CURSOR 12,1
PRINT" "
SET CURSOR 13,1
PRINT " B should be in the linear region for this material"
SET CURSOR 14,1
PRINT type$

REM find Np, the number of primary turns
LET Np = Ep*.707*1E+08/(4.44*f*B*Ae)
SET CURSOR 6,20
PRINT"NP = "
SET CURSOR 6,27
PRINT Np

LET Ns = Np/n
SET CURSOR 3,40
```

```
PRINT"NS ="
SET CURSOR 3,47
PRINT Ns
END
```

4LPICKERfinal a program in True Basic

```
! Program to find the best inductance values for a 4
! inductor switching resonator.  Freq. range: 25k to 95k
! lowest FRES is set to 30000 Hz, uses iterative search method
!
LET LowestLerror2=2E38              ! initialization

INPUT PROMPT "PRINTER OUTPUT? (Y/N)":PRINTERFLAG$

DIM Lres(15), Fres(15),FSWITCH(15), FRANGE(15), FSTEP(15)
DEF LPERCENT_ERROR(F,LRES)
    LET LIDEAL = 1/(C*(2*PI*F)^2)
    LET LPERCENT_ERROR = ABS((LRES - LIDEAL)/LIDEAL)
END DEF

LET C=64*5E-9
LET L1=1/(C*(2*PI*30000)^2)
PRINT "L1=",L1
LET LMINIMUM = 1/(C*(2*PI*95000)^2)
PRINT "LMINIMUM=",LMINIMUM

! lminimum is the value of l to resonate at 95kHz
! lparallel2 is the inductance required to parallel with L1
! to get the minimum inductance, lminimum

LET LPARALLEL2 = 1/(1/LMINIMUM - 1/L1)
LET L2min = 3 * LPARALLEL2
PRINT "L2min=",L2min


FOR L2 = L2MIN TO L1 STEP 1E-6

    FOR L3 = L2MIN TO L2 STEP 1E-6
        LET IL1=1/L1
```

```
LET IL2=1/L2
LET IL3 = 1/L3
LET IL4=1/LPARALLEL2 - IL2 - IL3
LET L4 = 1/IL4

LET LRES(1) = L1
LET LRES(2) = L2
LET LRES(3) = 1/(IL1 + IL2)
LET LRES(4) = L3
LET LRES(5) = 1/(IL1 + IL3)
LET LRES(6) = 1/(IL2 + IL3)
LET LRES(7) = 1/(IL2 + IL3 + IL1)
LET LRES(8) = L4
LET LRES(9) = 1/(IL1 + IL4)
LET LRES(10) = 1/(IL2 + IL4)
LET LRES(11) = 1/(IL2 + IL4 + IL1)
LET LRES(12) = 1/(IL4 + IL3)
LET LRES(13) = 1/(IL1 + IL3 + IL4)
LET LRES(14) = 1/(IL2 + IL3 + IL4)
LET LRES(15) = 1/(IL1 + IL2 + IL3 + IL4)
!LRES(15) is the smallest; therefore, FRES(15) is the highest



!BUBBLE SORT THE RESULTANT INDUCTANCES
!MAKES SURE THE INDUCTOR AT J IS MORE THAN THE ONE
! AT J+1
FOR I=1 TO 15
    LET SWAPFLAG = 0
    FOR J= 1 TO 14
        IF LRES(J) < LRES(J+1) THEN
           LET TMP = LRES(J)
           LET LRES(J) = LRES(J+1)
           LET LRES(J+1) = TMP
```

```
            LET SWAPFLAG = 1
        END IF
    NEXT J
    IF SWAPFLAG = 0 THEN LET I=16   !IF NO SWAPS, TERMINATE EARLY
NEXT I

FOR I=1 TO 15
    LET FRES(I) = 1/(2*PI*SQR(C*1*LRES(I)))
NEXT I
!LRES(15) is the smallest; therefore, FRES(15) is the highest

!INTEGRATE THE ERROR SQUARED

FOR I = 1 TO 14
     LET FSWITCH(I) = (1/(2*PI))*
                      SQR((LRES(I)+LRES(I+1))/(2*LRES(I)*LRES(I+1)*C))
    !find the best frequency to switch inductors
NEXT I

LET LERROR=0
LET LERROR1=0
LET LERROR2=0
LET LERROR3=0

!INTEGRATE THE FIRST ONE
LET LERROR = 0
FOR F = 25000 TO FSWITCH(1) STEP (FSWITCH(1)-25000)/10
    LET LERROR = LERROR + LPERCENT_ERROR(F,LRES(1))
NEXT F
LET LERROR = LERROR*(FSWITCH(1) - 25000)
LET LERROR1 = LERROR

!INTEGRATE THE MIDDLE ONES
LET LERROR2 = 0
```

```
FOR I=2 TO 14
    LET FRANGE(I) = FSWITCH(I) - FSWITCH(I-1)
    LET LERRORACCUM =0
    FOR F = FSWITCH(I-1) TO FSWITCH(I) STEP FRANGE(I)/10 + .00000001
            LET LERRORACCUM = LERRORACCUM + LPERCENT_ERROR(F,LRES(I))
    NEXT F
    LET LERROR21 = LERRORACCUM*FRANGE(I)
    IF LERROR21 < 0 THEN STOP
    LET LERROR2 = LERROR2 + LERROR21

NEXT I

!INTEGRATE THE LAST ONE
LET LERRORACCUM = 0
FOR F = FSWITCH(14) TO 100000 STEP (100000 - FSWITCH(14))/10
    LET LERRORACCUM = LERRORACCUM + LPERCENT_ERROR(F,LRES(15))
NEXT F
LET LERROR3 = LERRORACCUM*(100000 - FSWITCH(14))
LET LERROR = LERROR1 + LERROR2 + LERROR3

IF LERROR2 < LowestLerror2 THEN
   PRINT "L1 = ";L1,"L2 = ";L2
   PRINT "L3 = ";L3,"L4 = ";L4
   PRINT "LERROR2= ";LERROR2
   LET LowestLerror = LERROR
   LET LowestLerror1 = LERROR1
   LET LowestLerror2 = LERROR2
   LET LowestLerror3 = LERROR3
   LET LowesterrorL1 = L1
   LET LowesterrorL2 = L2
   LET LowesterrorL3 = L3
   LET LowesterrorL4 = L4
END IF
```

```
    NEXT L3
NEXT L2

PRINT "the end; the conditions when Lerror2 was a minimum:"
PRINT "LowestLerror = ";LowestLerror
PRINT "LowestLerror1 = ";LowestLerror1
PRINT "LowestLerror2 = ";LowestLerror2
PRINT "LowestLerror3 = ";LowestLerror3

PRINT "Lowest error L1 = ";LowesterrorL1
PRINT "Lowest error L2 = ";LowesterrorL2
PRINT "Lowest error L3 = ";LowesterrorL3
PRINT "Lowest error L4 = ";LowesterrorL4

IF PRINTERFLAG$ = "Y" OR PRINTERFLAG$ = "y" THEN
   OPEN #1:PRINTER


   LET L1 = LowesterrorL1
   LET L2 = LowesterrorL2
   LET L3 = LowesterrorL3
   LET L4 = LowesterrorL4

   LET IL1=1/L1
   LET IL2=1/L2
   LET IL3=1/L3
   LET IL4=1/L4


   LET LRES(1) = L1
   LET LRES(2) = L2
   LET LRES(3) = 1/(IL1 + IL2)
   LET LRES(4) = L3
   LET LRES(5) = 1/(IL1 + IL3)
```

```
LET LRES(6) = 1/(IL2 + IL3)
LET LRES(7) = 1/(IL2 + IL3 + IL1)
LET LRES(8) = L4
LET LRES(9) = 1/(IL1 + IL4)
LET LRES(10) = 1/(IL2 + IL4)
LET LRES(11) = 1/(IL2 + IL4 + IL1)
LET LRES(12) = 1/(IL4 + IL3)
LET LRES(13) = 1/(IL1 + IL3 + IL4)
LET LRES(14) = 1/(IL2 + IL3 + IL4)
LET LRES(15) = 1/(IL1 + IL2 + IL3 + IL4)
!LRES(15) is the smallest; therefore, FRES(15) is the highest



!BUBBLE SORT THE RESULTANT INDUCTANCES
!MAKES SURE THE INDUCTOR AT J IS MORE THAN THE ONE
! AT J+1
FOR I=1 TO 15
    LET SWAPFLAG = 0
    FOR J= 1 TO 14
        IF LRES(J) < LRES(J+1) THEN
           LET TMP = LRES(J)
           LET LRES(J) = LRES(J+1)
           LET LRES(J+1) = TMP
           LET SWAPFLAG = 1
        END IF
    NEXT J
    IF SWAPFLAG = 0 THEN LET I=16   !IF NO SWAPS, TERMINATE EARLY
NEXT I

FOR I=1 TO 15
    LET FRES(I) = 1/(2*PI*SQR(C*1*LRES(I)))
NEXT I
!LRES(15) is the smallest; therefore, FRES(15) is the highest
```

```
   FOR I = 1 TO 14
       LET FSWITCH(I) = (1/(2*PI))* SQR((LRES(I)+LRES(I+1))/(2*LRES(I)*LRES(I+1)*C))
       !find the best frequency to switch inductors
   NEXT I

   PRINT#1: "the end; the conditions when Lerror2 was a minimum:"
   PRINT#1: " N=8    C=5E-9   FRANGE = 25,000 TO 100,000 "

   PRINT#1: "LowestLerror = ";LowestLerror
   PRINT#1: "LowestLerror1 = ";LowestLerror1
   PRINT#1: "LowestLerror2 = ";LowestLerror2
   PRINT#1: "LowestLerror3 = ";LowestLerror3

   PRINT#1: "Lowest error L1 = ";LowesterrorL1
   PRINT#1: "Lowest error L2 = ";LowesterrorL2
   PRINT#1: "Lowest error L3 = ";LowesterrorL3
   PRINT#1: "Lowest error L4 = ";LowesterrorL4
   PRINT#1: "I","FRES(I)","LRES(I)","FSWITCH(I)"
   FOR I=1 TO 15
       PRINT#1: I,FRES(I), LRES(I),FSWITCH(I)
   NEXT I
END IF
END
```

```
4LPICKERMAX4 a program in True Basic
! Program to calculate the error factors, currents at the switching frequencies
! and various currents for a 4 inductance switching resonator.
! Freq. range: 25k to 95k
! lowest FRES is 30000
!
LET LowestLerror2=2E38            ! initialization


DIM Lres(15), Fres(15),FSWITCH(0:15), FRANGE(15), FSTEP(15)
DEF LPERCENT_ERROR(F,LRES)
    LET LIDEAL = 1/(C*(2*PI*F)^2)
    LET LPERCENT_ERROR = ABS((LRES - LIDEAL)/LIDEAL)
END DEF

LET C=64*5E-9
LET L1=1/(C*(2*PI*30000)^2)
PRINT "L1=",L1
LET LMINIMUM = 1/(C*(2*PI*95000)^2)
PRINT "LMINIMUM=",LMINIMUM

! lminimum is the value of l to resonate at 95kHz
! lparallel2 is the inductance required to parallel with L1
! to get the minimum inductance, lminimum

LET LPARALLEL2 = 1/(1/LMINIMUM - 1/L1)
LET L2min = 3 * LPARALLEL2
PRINT "L2min=",L2min


DO WHILE 1=1


INPUT PROMPT "ENTER L2  microhenries ":L2
```

```
INPUT PROMPT "ENTER L3  microhenries ":L3
let 12 = 12*1e-6
let 13 = 13*1e-6
        LET IL1=1/L1
        LET IL2=1/L2
        LET IL3 = 1/L3
        LET IL4=1/LPARALLEL2 - IL2 - IL3
        LET L4 = 1/IL4

        LET LRES(1) = L1
        LET LRES(2) = L2
        LET LRES(3) = 1/(IL1 + IL2)
        LET LRES(4) = L3
        LET LRES(5) = 1/(IL1 + IL3)
        LET LRES(6) = 1/(IL2 + IL3)
        LET LRES(7) = 1/(IL2 + IL3 + IL1)
        LET LRES(8) = L4
        LET LRES(9) = 1/(IL1 + IL4)
        LET LRES(10) = 1/(IL2 + IL4)
        LET LRES(11) = 1/(IL2 + IL4 + IL1)
        LET LRES(12) = 1/(IL4 + IL3)
        LET LRES(13) = 1/(IL1 + IL3 + IL4)
        LET LRES(14) = 1/(IL2 + IL3 + IL4)
        LET LRES(15) = 1/(IL1 + IL2 + IL3 + IL4)
        !LRES(15) is the smallest; therefore, FRES(15) is the highest



        !BUBBLE SORT THE RESULTANT INDUCTANCES
        !MAKES SURE THE INDUCTOR AT J IS MORE THAN THE ONE
        ! AT J+1
        FOR I=1 TO 15
            LET SWAPFLAG = 0
            FOR J= 1 TO 14
```

```
        IF LRES(J) < LRES(J+1) THEN
           LET TMP = LRES(J)
           LET LRES(J) = LRES(J+1)
           LET LRES(J+1) = TMP
           LET SWAPFLAG = 1
        END IF
    NEXT J
    IF SWAPFLAG = 0 THEN LET I=16   !IF NO SWAPS, TERMINATE EARLY
NEXT I

FOR I=1 TO 15
    LET FRES(I) = 1/(2*PI*SQR(C*1*LRES(I)))
NEXT I
!LRES(15) is the smallest; therefore, FRES(15) is the highest

!INTEGRATE THE ERROR SQUARED

FOR I = 1 TO 14
    LET FSWITCH(I) = (1/(2*PI))*
                     SQR((LRES(I)+LRES(I+1))/(2*LRES(I)*LRES(I+1)*C))
    !find the best frequency to switch inductors
NEXT I

FOR I=1 TO 15
 PRINT I,FRES(I), LRES(I),FSWITCH(I)
NEXT I

LET LERROR=0
LET LERROR1=0
LET LERROR2=0
LET LERROR3=0

!INTEGRATE THE FIRST ONE
LET LERROR = 0
```

```
FOR F = 25000 TO FSWITCH(1) STEP (FSWITCH(1)-25000)/50
    LET LERROR = LERROR + LPERCENT_ERROR(F,LRES(1))
NEXT F
LET LERROR = LERROR*(FSWITCH(1) - 25000)
LET LERROR1 = LERROR

!INTEGRATE THE MIDDLE ONES
LET LERROR2 = 0
FOR I=2 TO 14
    LET FRANGE(I) = FSWITCH(I) - FSWITCH(I-1)
    LET LERRORACCUM =0
    FOR F = FSWITCH(I-1) TO FSWITCH(I) STEP FRANGE(I)/50 + .00000001
        LET LERRORACCUM = LERRORACCUM + LPERCENT_ERROR(F,LRES(I))
    NEXT F
    LET LERROR21 = LERRORACCUM*FRANGE(I)
    IF LERROR21 < 0 THEN STOP
    LET LERROR2 = LERROR2 + LERROR21

NEXT I

!INTEGRATE THE LAST ONE
LET LERRORACCUM = 0
FOR F = FSWITCH(14) TO 100000 STEP (100000 - FSWITCH(14))/50
    LET LERRORACCUM = LERRORACCUM + LPERCENT_ERROR(F,LRES(15))
NEXT F
LET LERROR3 = LERRORACCUM*(100000 - FSWITCH(14))
LET LERROR = LERROR1 + LERROR2 + LERROR3


PRINT "L1 = ";L1,"L2 = ";L2
PRINT "L3 = ";L3,"L4 = ";L4
PRINT "LERROR = ";LERROR
PRINT "LERROR1 = ";LERROR1
PRINT "LERROR2 = ";LERROR2
```

```
      PRINT "LERROR3 = ";LERROR3



    PRINT
INPUT PROMPT "PRINT THE FREQUENCIES? Y/N":PRINTERFLAG$


IF PRINTERFLAG$ = "Y" OR PRINTERFLAG$ = "y" THEN
   OPEN #1:PRINTER

   PRINT#1: "I","LRES(I)","        AMPLIFIER CURRENT  "
   PRINT#1:  " "," "," Low End"," High End"
   let FSWITCH(0)=25000
   let FSWITCH(15)=100000
   FOR I=1 TO 15
       let IampLowFreq = 25*((1/LRES(I)) -
((2*PI*FSWITCH(I-1))^2)*C)/(2*pi*FSWITCH(I-1))
       let IampHighFreq = 25*((1/LRES(I)) -
((2*PI*FSWITCH(I))^2)*C)/(2*pi*FSWITCH(I))
       PRINT#1: I, LRES(I),IampLowFreq,IampHighFreq
   NEXT I
   PRINT#1: "I","FRES(I)","LRES(I)","FSWITCH(I)"
   FOR I=1 TO 15
       PRINT#1: I,FRES(I), LRES(I),FSWITCH(I)
   NEXT I

END IF
LOOP
END
```

APPENDIX C

SPECIFICATIONS OF THE SWITCHING OF THE INDUCTORS

The frequency bands and control codes to be sent to the amplifier.

Band#	Frequency (kHz)		Code			
		inductor:	L4	L3	L2	L1
		plug pin#	9	8	7	6
1	25 - 37.6		1	1	1	0
2	37.6 - 46.5		1	1	0	1
3	46.5 - 51.1		1	0	1	1
4	51.1 - 55.3		1	1	0	0
5	55.3 - 59.5		1	0	1	0
6	59.5 - 63.7		0	1	1	1
7	63.7 - 67.1		1	0	0	1
8	67.1 - 70.4		0	1	1	0
9	70.4 - 74.0		1	0	0	0
10	74.0 - 77.2		0	1	0	1
11	77.2 - 80.1		0	0	1	1
12	80.1 - 82.8		0	1	0	0
13	82.8 - 87.2		0	0	1	0
14	87.2 - 92.6		0	0	0	1
15	92.6 - 100		0	0	0	0

The logic levels for the control lines are CMOS compatible, and need to be driven above 4.5 V for a "1" logic level to be reliably recognized.

The output of 4LPICKERMAX4 is reproduced below:

Band#, m	Theoretical L(m) [μH]	Theoretical $F_{resonant}$(m) [kHz]	Theoretical I_{AMP}(m)	
			Low End	High End [mA]
1	87.9	30.0	553	688
2	41.0	43.9	688	253
3	33.0	49.0	253	212
4	28.0	53.2	212	212
5	24.0	57.4	212	210
6	20.8	61.6	210	210
7	18.3	65.8	210	137
8	16.8	68.5	137	190
9	15.1	72.3	190	169
10	13.8	75.7	169	152
11	12.8	78.7	152	135
12	11.9	81.4	135	142
13	11.1	84.2	142	297
14	9.74	90.1	297	244
15	8.77	95.0	244	490

VITA

Alex Bolling Shore was born in Memphis, Tennessee, on October 8, 1962. He graduated from Bartlett High School in May of 1980. The following September he entered the University of Tennessee's Engineering program at the Knoxville campus. After completing the requirements of a Bachelor of Science degree in Electrical Engineering and the Engineering Co-op program, he was graduated in June of 1985. After working as a Summer Preprofessional at IBM, he began the Master of Science program in September of 1985. He received the Master of Science degree in electrical engineering in December of 1986.