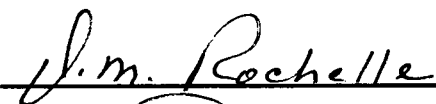
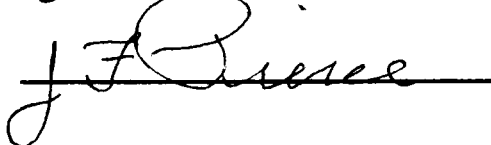


To the Graduate Council:

I am submitting herewith a thesis written by Travis N. Blalock entitled "Development of a Radiation Hardened, 600 Watt, Switchmode Power Converter." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical and Computer Engineering.


Eldredge J. Kennedy, Major Professor

We have read this thesis
and recommend its acceptance:

Accepted for the Council:


Vice Provost
and Dean of the Graduate School

**DEVELOPMENT OF A RADIATION HARDENED
600 WATT SWITCHMODE
POWER CONVERTER**

**A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville**

**Travis N. Blalock
December 1988**

ACKNOWLEDGEMENTS

The author wishes to acknowledge the guidance and collaboration of his thesis advisor, Dr. E. J. Kennedy. Special appreciation is expressed to thesis committee members, Drs. J. F. Pierce and J. M. Rochelle. Dr. T. F. Williams and his assistants of the Chemistry Department, the University of Tennessee, Knoxville, are acknowledged for providing the gamma irradiation facility.

This research was sponsored by the Fuel Recycle Division, Oak Ridge National Laboratory. The work was performed under Subcontract No. 7685 between the Oak Ridge National Laboratory and the Electrical and Computer Engineering Department, the University of Tennessee, Knoxville.

The author is particularly grateful to his wife, Mary T. Blalock, for her continued support and patience. Special appreciation also for, Dr. and Mrs. T. Vaughn Blalock for their years of encouragement and inspiration.

ABSTRACT

The purpose of this investigation was to develop a radiation hardened switching power supply. The power supply will be used in a nuclear fuel reprocessing environment, supplying power to other instrumentation. The supply was required to have three DC voltage outputs, with a total output power capability of 600 watts. Complete isolation of the AC line input and each of the voltage outputs was also required. Each output was to be short-circuit protected and capable of sensing over and under voltage conditions.

The power supply circuit was designed to withstand a total absorbed gamma dose of at least ten megarad. The implications of this requirement were discussed. In addition, the results of specific testing of parts for this application were reviewed along with the radiation hardness of the completed prototype.

In addition to the radiation hardness requirements, frequency and transient response of the various sections were computer simulated and measured. Various circuit topologies for implementation of the switching power supply were discussed in terms of relative advantages and applicability to various applications.

A magnetic amplifier was also discussed and implemented for secondary regulation of two of the output sections. The magnetic amplifier circuit was discussed and computer models for the closed loop response were illustrated.

Complete results for the constructed prototype were presented and discussed. Also included was a complete parts list for the prototype power supply.

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CHAPTER I

THESIS OVERVIEW

Introduction

The development project described in this document resulted from discussions held during a Specialists' Meeting at the Oak Ridge National Laboratory (ORNL) on October 7-9, 1986. The meeting, involving ORNL Fuel Recycle Division (FRD) personnel and French Commissariat a l'Energie Atomique (CEA) personnel, concerned the subject of Environmental Hardening of Remote Maintenance Control System hardware for reactor fuel reprocessing applications. This hardware included remote manipulators, intelligent sensors, communications hardware, and power supplies - all of which had to be designed for operation in a high radiation environment ('hot cell'). The goal of this effort was to produce a system capable of reprocessing nuclear waste which must now be disposed of in the environment in some manner. The meeting was organized under an existing Agreement between the United States Department of Energy (USDOE) and the CEA. The Agreement provided for a cooperative effort between the two countries concerning remote systems technology development, as well as technical exchange [15].

As a result of these discussions, the USDOE-ORNL was commissioned to develop several components of 'hot cell' instrumentation for use in the nuclear fuel recycling application. The USDOE-ORNL let a subcontract to the University of Tennessee, Knoxville, (UTK) Electrical Engineering Department to complete two facets of the commissioned work, the first of which was a general investigation to evaluate the radiation hardness of several commercially available integrated circuits (UTK document number ORNL/SUB-7685,TR-EE/EL/19). The second facet of the subcontract called for the development of a radiation hardened DC power supply for use by the CEA in powering

other 'hot cell' instrumentation in later tests in France. It is this latter development effort which is the topic of this document.

Objectives

The contracted power supply has several demanding specifications and constraints. First, it must be radiation hardened to withstand a total absorbed gamma dose of 10^7 rad with output voltages varying less than $\pm 5\%$. It must also operate in an ambient temperature environment from 10°C to 60°C . In addition, since this supply will be providing power for many other pieces of hardware to be developed later, it must be extremely reliable so that performance of the developing hardware may be evaluated without fear of compromise from the power source.

The power supply operates from a three phase delta wound, 220 VAC, 50 Hz, line input. It has three DC voltage outputs, all of which must have short and open circuit protection. The outputs include +5V @ 25A, and $\pm 15\text{V}$ @ $\pm 15\text{A}$. The complete specifications are summarized in Table 1-1.

Approach

Due to the high power output ($\approx 600\text{W}$) of the proposed DC supply, efficiency is a key issue in the design process. The high ambient temperature specification further increases the importance of power supply efficiency. If the supply efficiency is too low, tremendous self-heating can occur, causing junction temperatures to rise to prohibitive levels.

The traditional approach to power supply design has been linear shunt or series-pass regulator circuits. However, linear regulators are losing ground to switchmode voltage regulation circuits. This is due primarily due to the inefficiency brought about by

Table 1-1. Power supply specifications.

Input:	3 phase delta wound, 50 Hz, 220 VAC $\pm 10\%$ between phases
Protection:	input protection, overvoltage, short-circuit, open-circuit
Status:	A TTL, open-collector signal should be provided to indicate over or under voltage power supply failures.
Volume:	$\leq 7 \text{ dm}^3$ (427 in ³)
Ambient Temperature:	$10^\circ\text{C} \leq T \leq 60^\circ\text{C}$
Radiation Hardening:	Output voltages shall not vary from nominal values by more than $\pm 5\%$ for a total absorbed gamma dose of 10^7 rad, with a maximum dose rate of $3\text{E}4$ rad/h.
Isolation:	All inputs and outputs shall be fully isolated from one another.
+5 VDC output	
Output ripple:	$\leq 100 \text{ mV}$ peak-to-peak
Output current:	$2.5\text{A} < I_{\text{out}} < 25\text{A}$
± 15 VDC output	
Output ripple:	$\leq 150 \text{ mV}$ peak-to-peak
Output current:	$150\text{mA} < I_{\text{out}} < 15\text{A}$

linear regulators' large heat sink requirements and resultant bulky size. This inefficiency is fundamental to the constraint that the power elements must sustain large currents while operating in the linear, V_{CE} or $V_{DS} \geq \approx 1.5$ volts, region of their transfer characteristics. In addition, input transformers for linear supplies operate at line frequencies, ($50 \leq f \leq 120$ Hz), and can be quite large for delivery of even moderate power levels.

In contrast to linear regulators, the power elements in switching regulators operate in saturation or quasi-saturation, and therefore dissipate much less power than their linear supply counterparts. Since the power transformer is typically operating at frequencies at least three orders of magnitude greater than line frequencies, the power transformer is reduced in size by at least three orders of magnitude for a given output power. This increased operating frequency also reduces the size of the output filter elements, (typically simple L-C networks).

Since power elements in switchmode power converters usually operate with lower junction temperatures than similar devices in linear supplies, switching regulators are generally considered to be more reliable than linear regulators. For this reason, and for the increased efficiency provided by the switchmode power converter (SPC) circuit, it was decided to pursue a switching regulator topology over linear topologies for the development project of this thesis.

Overview

As introduced above, this thesis describes the design, modeling, and prototype evaluation of a 600W, radiation hardened, switching power supply. The organization of the thesis is as follows:

Chapter II discusses various SPC topologies and the rationale for the topology chosen for this project. The magnetic amplifier topology used for post regulation of two of the outputs is also introduced.

- Chapter II discusses various SPC topologies and the rationale for the topology chosen for this project. The magnetic amplifier topology used for post regulation of two of the outputs is also introduced.
- Chapter III summarizes basic gamma radiation damage mechanisms and the implications of these mechanisms on circuit component selection.
- Chapter IV covers the design specifics of the various sections of the power supply.
- Chapter V discusses the SPICE models used to simulate and finalize the design of the supply control loops.
- Chapter VI describes the measured performance of the prototype circuit and compares it to the predicted performance.
- Chapter VII covers general conclusions and discusses areas where further work could advance the state of the art in SPC development.
- Appendix includes listings of SPICE programs used for system modeling, and a complete parts list for the prototype circuit.

CHAPTER II

CIRCUIT TOPOLOGY TRADEOFFS

Switching Regulator Introduction

In recent years, as integrated circuit technology has spawned increasingly lightweight and compact designs, the need for similarly elegant power sources has increased. This need, in turn, has fostered the development of switchmode power converter design theory and techniques to the point that switching regulators are being used in applications where linear regulators had been the traditional solution. As outlined in chapter I, the stringent specifications of this application make it quite suitable for off-line switching power supply technology.

The block diagram of the off-line switching power supply is depicted in Figure 2-1. The input line voltage is rectified and filtered, yielding a high voltage DC bus. The high voltage DC is then chopped at a frequency much higher than the input line frequency and transformed to a lower voltage. The transformer output is then rectified and filtered, producing the desired DC output. Output regulation is achieved by modifying the duty cycle of the chopped DC, thereby regulating the energy sent to the transformer. This, in turn, alters the average voltage resulting from the rectification and subsequent low pass filtering at the secondary of the transformer.

For multiple output voltage applications, additional secondary windings are added. Regulation of the additional outputs is usually by magnetic coupling via the ratio of the additional secondary turns to the turns of the sampled secondary section.

In this particular application, the rectified and filtered input line voltage of 220 VAC, three phase, yields a high voltage bus of approximately 300 VDC. In the following discussions and figures, this is the value for the DC voltage referred to as V_{in} .

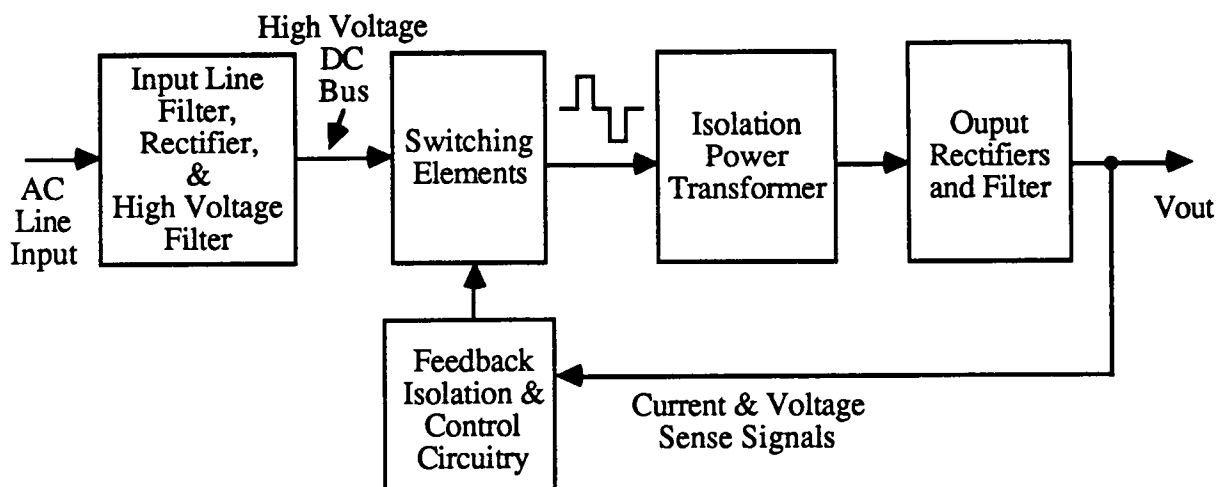


Figure 2-1. Block diagram of the off-line switchmode power converter.

Traditional Topologies

Although the basic approach to off-line switchers is as described above, there are several specific topologies which are used in modern SPC applications. Several of the more practical configurations which can be applied in off-line power supply circuits are outlined in the following sections. The following topology discussions are taken heavily from references [7] and [25]. These switchmode power conversion texts are quite useful and have many other excellent references.

Flyback Converter

Figure 2-2 shows a simplified schematic of a popular SPC topology, the flyback converter. Circuit operation is as follows. Q1 is on for a time, t_{on} , usually less than 50% of the switching frequency period T . During t_{on} , energy is stored in the core of the isolation transformer-choke T1. T1 is referred to as a transformer-choke since it acts both as a transformer and an output choke. When Q1 turns off, the collapsing magnetic field of

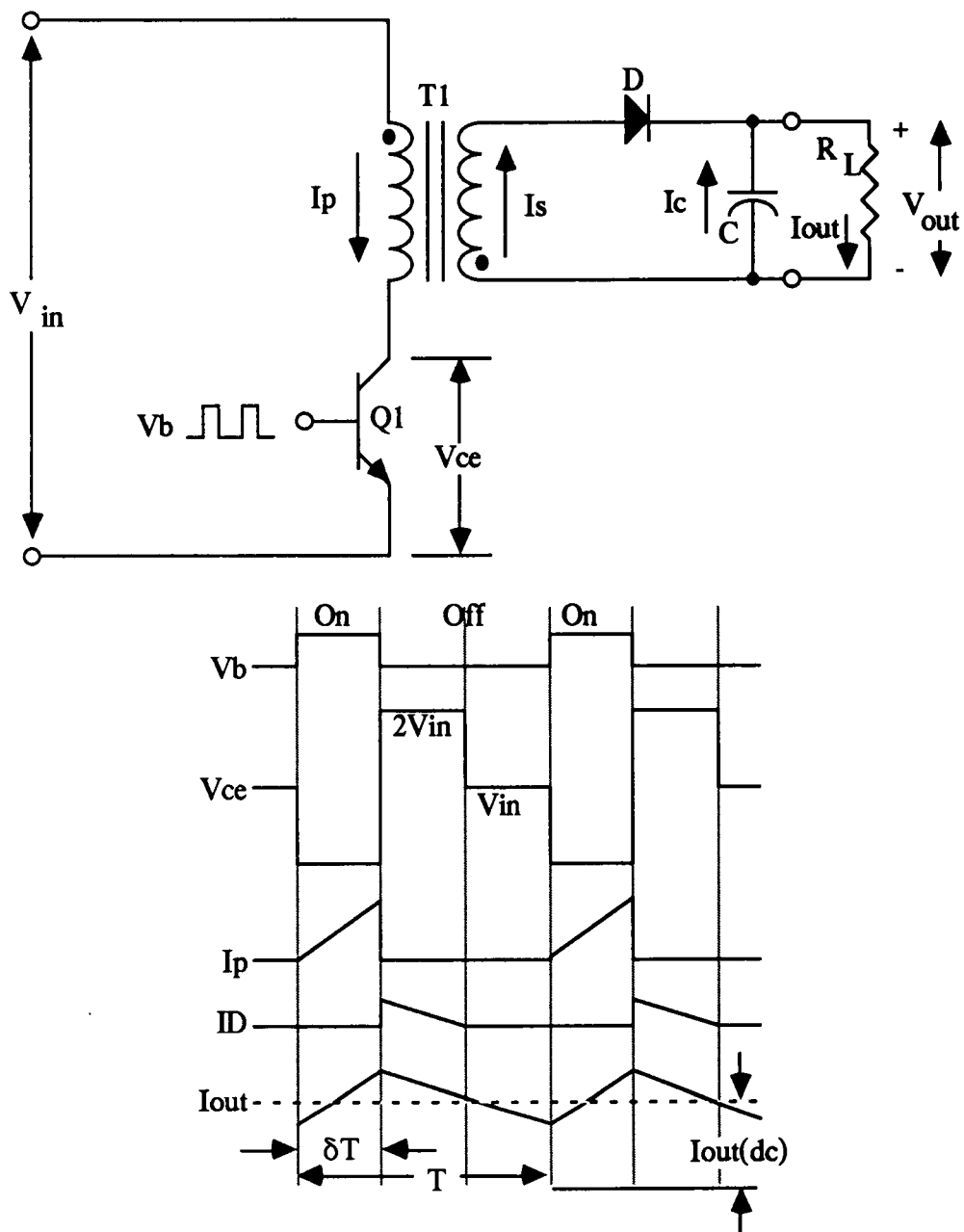


Figure 2-2. Simplified schematic of typical flyback converter with associated waveforms.

T1 causes the transformer windings to reverse polarity, or flyback. This causes the non-dotted terminal of the transformer secondary to become positive--turning on output rectifier diode D and thereby delivering charge to filter capacitor C and current to the load R_L . After a time equal to t_{on} , the transformer has delivered all of its stored energy and D turns off, forcing the output capacitor C to deliver to the load the energy it stored in the form of charge during the flyback pulse. The filter capacitor C delivers all of the load current until the next flyback pulse.

As seen in Figure 2-2, during the flyback portion of the cycle, the reverse voltage impressed across Q1 can be as high as twice V_{in} or higher, depending upon the duty cycle δ . This occurs because the primary winding polarity reverses in the same manner as the secondary when switch Q1 turns off. For safe and reliable operation, a transistor with V_{BCE} of ≥ 800 volts is typically used.

This topology is popular for its simplicity. However, transformer utilization is extremely poor since it only uses half of the B-H curve, forcing transformer core size to increase in order to deliver a given power. Flyback designs are seldom practical above 200 watts [6].

Forward Converter

The forward converter depicted in Figure 2-3 appears very similar to the flyback converter discussed above but actually operates quite differently. Unlike the transformer-choke in the flyback circuit, the forward converter transformer operates as a 'traditional' transformer. This gives rise to the secondary section inductive storage element, L.

Notice also that the primary and secondary windings have the same polarity. This allows energy to be delivered to the output section during the 'ON' time of Q1. When Q1 turns off, T1 polarity reverses, turning D1 on and D2 off. The purpose of D1 is to provide reset current to the power transformer T1 during t_{off} , restoring the flux in T1 to zero and

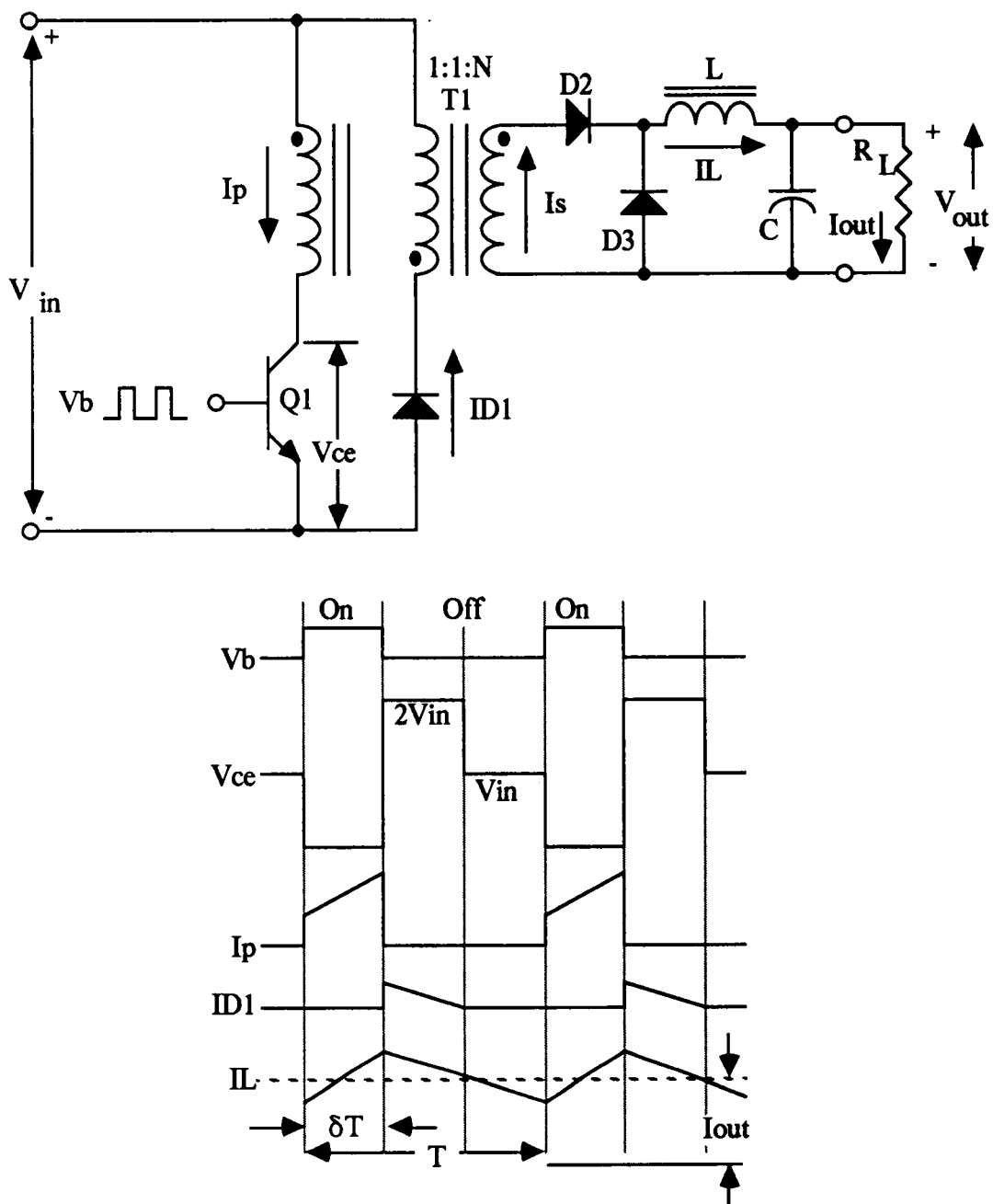


Figure 2-3. Simplified schematic of typical forward converter with associated waveforms.

readying the core for another energy delivery cycle. As diode D2 turns off, output inductor L reverses its polarity due to the collapsing magnetic field in its core. This turns on diode D3, which maintains current flow through L and to the load. Diode D3 is often referred to as a 'catch' or 'flywheel' diode. If L is not large enough, I_L reaches zero before Q1 turns on again, giving rise to a mode of operation known as 'discontinuous conduction mode'. While I_L is zero, output capacitor C must supply all the load current, similar in function to the output capacitor of the flyback topology. Since this condition increases output voltage and current ripple, typical forward converter designs maintain continuous conduction in the output inductor. (This is also true of all topologies discussed in the remainder of this chapter.)

Due to the varying voltages across the output inductor L during the different cycles of the converter, the current through L is of a pulsating nature, as seen in the waveforms accompanying Figure 2-3. Thus, the output filter capacitor C has a pulsating current--similar to that in L--which when summed with the inductor current, gives rise to a nearly constant output current.

Output regulation of the forward converter, as well as the other converter topologies discussed here, is maintained by sampling the output DC voltage, comparing it to a reference voltage, and adjusting the duty cycle of the base drive signal V_b to compensate for any measured error. Duty cycle is increased to increase the output DC level. In this way, the output DC level can be maintained over variations in input line voltage and output load.

There is another form of SPC control known as current mode control. This type of control loop makes use of both output current and output voltage information to generate the appropriate duty cycle variation signals. Since more information is utilized, tighter control of the the output state can be maintained using current mode control. Current mode control was not used in this project since the regulation specifications were not demanding

enough to merit the extra complexity, but references [5,18,27,1,23] are included for the interested reader.

For the forward converter topology in Figure 2-3, the maximum duty cycle, $\delta_{\max}$, is limited to 50% of the switching period T . This is due to the fact that the reset current is actually imposed by a voltage source, V_{in} , which is the same signal imposed during the on time by Q1. In other words, as long as the primary winding and reset winding turns are equal, t_{off} must be $\geq t_{on}$ to fully reset the core, (drive the flux in the core to zero), during each cycle. If the transformer core is not fully reset during each cycle, the net flux still present in the core at the end of each cycle will add to that remaining at the end of the previous cycle. This phenomenon, referred to as 'flux walking,' leads to core saturation. When saturation occurs, the transformer becomes a virtual short circuit and the power switch Q1 catastrophically fails.

Note also that when the core is being reset, the power switch Q1 must sustain a peak collector voltage of twice V_{in} . This is illustrated in the waveforms of Figure 2-3. For a system operating from a rectified 220 VAC input, ≈ 300 VDC, the power switches must have a reverse breakdown voltage of 800 volts or more to ensure reliable operation. This figure allows for possible switching spikes beyond the imposed voltage of $2V_{in}$. Such a large breakdown voltage requirement greatly reduces the number of efficient switching devices available and can be a disadvantage for 220 VAC off-line switching applications.

The power handling capabilities of the forward converter are better than those of the flyback converter. Recall that the flyback transformer-choke delivers power to the secondary when the primary is open-circuited. Similarly, power is delivered to the transformer primary when the secondary is open-circuited. This means that the maximum energy that can be delivered to the load is that which the transformer can store, since the load is never connected when energy is being delivered to the transformer core. The amount that can be stored is basically that energy which the primary magnetizing inductance

can store. On the other hand, the forward converter transformer acts as a conventional transformer - the energy is delivered to the load at the same time that it is delivered to the transformer primary. From basic transformer theory it is known that the flux cancellation due to the simultaneous primary and secondary currents allows the core to deliver far more energy than it is capable of storing in the primary inductance.

Therefore, the forward converter is capable of delivering more power than the flyback converter for a given core size. However, core utilization is still not maximized since the core is only driven in one direction, (only one half of the available B-H curve is used). For applications over 500W, the forward converter is typically abandoned for one in which core utilization is improved.

Push-Pull Converter

Another useful topology is the push-pull configuration in Figure 2-4. Close comparison of the push-pull topology to that of the forward converter reveals that the push-pull can be thought of as two forward converters working 180° out of phase with each other. In place of the reset diode D1 in Figure 2-3, another power switch, Q2 of Figure 2-4, is now found. To take advantage of the additional power switch, the output is now center-tapped, and the output rectifier diodes are configured in a full wave rectification arrangement. Notice that the flywheel diode D3 of the forward topology is no longer present. Assuming diode D1 is on, when the signal on the primary is removed and D1 turns off, the flyback of output inductor L is 'caught' by diode D2. When D2 is delivering power, the diode D1 acts as a 'catch' diode upon D2 turnoff.

Power switches Q1 and Q2 conduct during alternate half cycles. Positive primary current flows into the primary center tap through one side of the primary to whichever transistor is 'on', returning to the negative side of the input source, V_{in} . Transformer reset is inherent to the design since the core is driven in opposite directions along its B-H curve

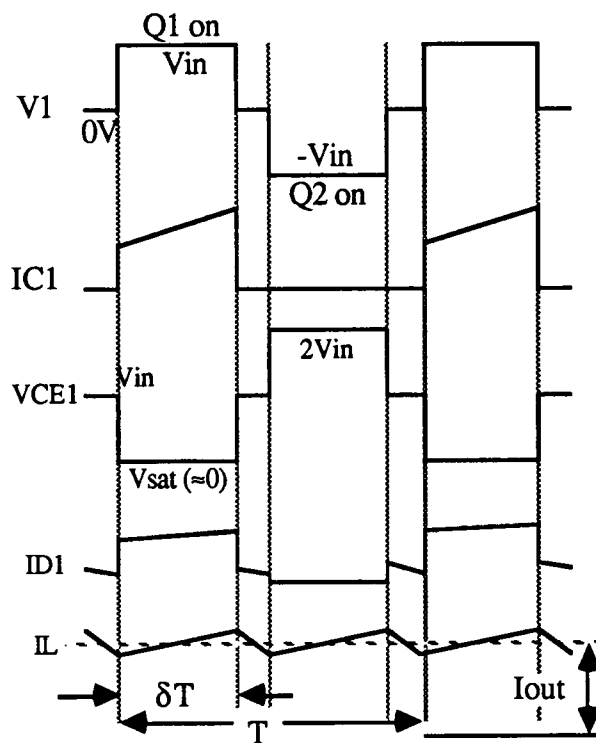
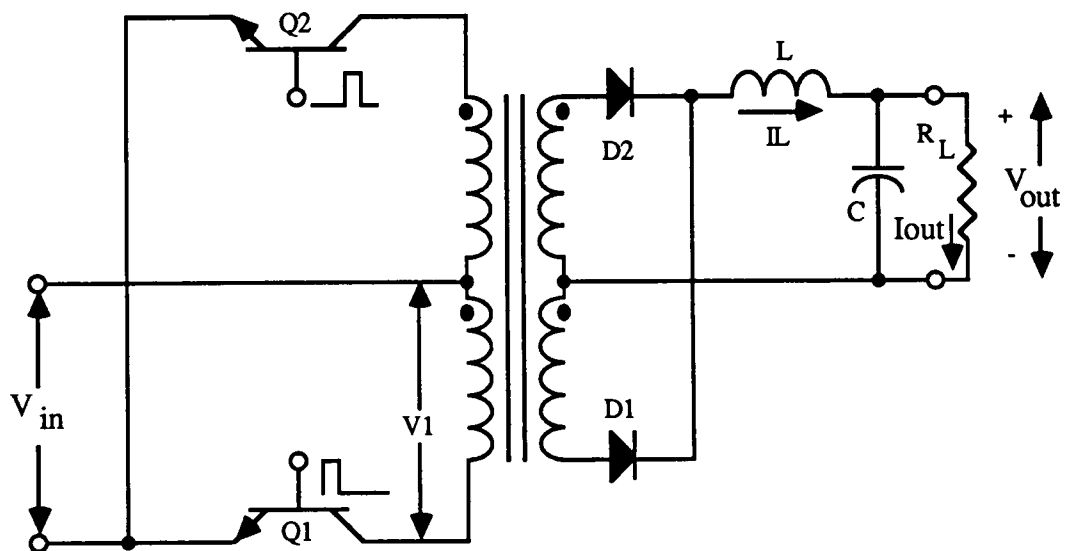


Figure 2-4. Simplified schematic of the push-pull SPC topology and associated waveforms.

during alternate half cycles while delivering power to the load. Because of this, for a given power output the push-pull transformer core must be only half the size of the forward converter transformer, since both halves of the B-H curve are utilized.

Another advantage of the push-pull topology is the full wave rectification at the output. With respect to the frequency with which either of the power transistors are switching, the output section ripple frequency is doubled due to the full wave rectification. This is illustrated in the waveforms of Figure 2-4. Due to this increase in the output ripple frequency, the filter elements, L and C, can be reduced in value, (and usually size), by a factor of two and retain the same ripple rejection as a similar forward converter design.

Unfortunately, the push-pull topology has some serious drawbacks. First, similar to the forward converter, the power switches Q1 and Q2 must sustain a voltage twice the input voltage, or $2V_{in}$. Furthermore, since a center-tapped primary typically has fairly high leakage inductance, there can be substantial switching spikes, further increasing the breakdown voltage requirements on the power drivers.

Another important drawback of the push-pull circuit is a tendency for the core to saturate. In order for the core flux to be reset to zero at the end of each complete switching cycle, Q1 and Q2 must have identical saturation voltages and 'ON' times, t_{on} . This will ensure that identical volt-seconds products are delivered to the core in both directions of the B-H curve. Due to almost certain transistor mismatch, the volt-seconds product delivered to the primary by each switch is not equal, and the transformer tends to 'walk' towards one side of the B-H curve. If this process continues for long, core saturation occurs. The process is regenerative and can result in switch destruction in only a few switching cycles [6].

This problem can be alleviated by increasing the core gap, since this 'flattens' the B-H curve and makes core saturation much more difficult to achieve. However, this increases leakage inductance, thereby increasing switching spikes which could cause

reverse breakdown failures. The other solution to the 'flux-walking' dilemma is to add control circuitry which will detect the volt-sec imbalance and correct it by modifying the pulse widths of the two drivers independently. It should be noted here that this sort of pulse width control is inherent to the current mode control loop mentioned earlier. Of course, this solution increases the complexity of the control circuitry.

As aforementioned, the push-pull has twice the core utilization of the forward converter topology. As a result, many push-pull designs have been implemented with power outputs as high as 1000 watts.

Jensen Converter

To avoid the core saturation problems of the push-pull converter described above, the converter topology shown in Figure 2-5 was developed by J. Jensen in 1957 ([25] - figure 4.12). The topology is essentially the same as the basic push-pull already discussed, with the addition of base drive circuitry. The additional circuitry has two purposes. First, it makes the circuit self-oscillating. Second, it protects the topology from power transformer core saturation.

The self-oscillation of the circuit occurs in the following manner. Assuming Q1 is saturated, the collector of Q2 is at $2V_{in}$ since the center tap of T1 is connected to $+V_{in}$. This, in turn, means that there is a positive voltage on the dotted primary terminal of T2. As a result, the base of Q1 is driven positive, which confirms the original assertion that Q1 is on. Transformer T2 is wound on a saturable core--it is designed to saturate easily. Consequently, after Q1 has been on for a short time, transformer T2 saturates, and its windings become virtual short circuits, removing the positive base drive on transistor Q1. When Q1 turns off, transformer T1 flyback impresses a positive voltage on the non-dotted primary terminal of T2. After a short delay, necessary to bring T2 out of saturation, transistor Q2 turns on. This process repeats as described, and continuous oscillation is

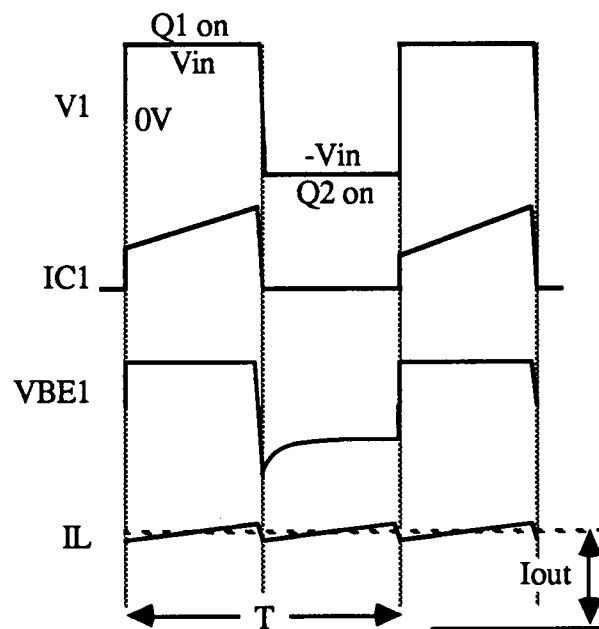
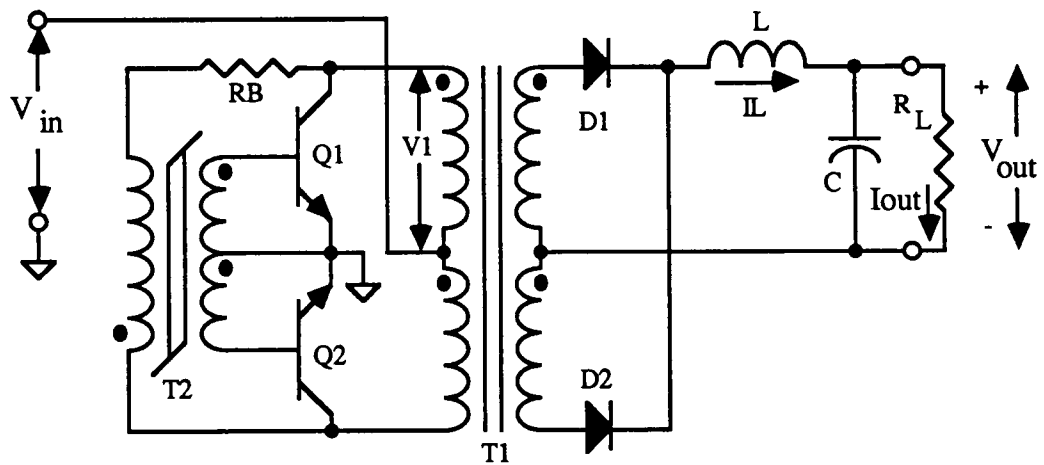


Figure 2-5. Simplified schematic of the Jensen topology SPC and associated waveforms [25].

achieved. The frequency of oscillation is determined by the nominal value of V_{in} , R_B , V_{BE} of the power switches, and by the saturation characteristics of transformer T2.

Power transformer core saturation is avoided by proper design of base drive transformer T2. As previously mentioned, T2 is wound on a saturable core and therefore reaches saturation easily. Since the power switches turn off when T2 saturates, T1 will never saturate if base drive transformer T2 is designed to saturate sooner than T1.

Although this topology offers an elegant solution to the problem of core saturation, it has some drawbacks. One of these is the increased complexity of the magnetics design. A more serious insufficiency of the topology in Figure 2-4 is its lack of provision for accurate regulation of V_{out} . The other circuits discussed here are presented with the assumption that part of the function of the switch control circuitry is to monitor the output voltage and to adjust the duty cycle of the base drive signals to effectively regulate the output voltage. The Jensen converter, as depicted, simply maintains a constant ratio between the input DC and the output DC voltages, this ratio being approximately equal to the turns ratio of transformer T1. If the input voltage is regulated and the load does not vary widely, the output voltage will be fairly well constrained. On the other hand, off-line switchers must be able to regulate their outputs despite input line changes, given that AC power lines can vary as much as $\pm 20\%$. For this to be an effective off-line design, some means of controlling the duty cycle of the power switches must be added.

The most likely addition to the Jensen converter to improve output regulation would be an additional set of turns on T2 coupled with a clipping circuit. The pulse width could be regulated by delaying the turn on of the power switches by clipping the voltage on the extra turns of T2. Another approach is to diode 'OR' a current source at each of the primary terminals of T2. By controlling the current of the added current source, the delay necessary to bring T2 out of saturation could be increased by decreasing the amount of reset current available. This would effectively modulate the duty cycle of the power

switches. Either of these approaches adds complexity to the topology and can negate the basic advantages of the circuit approach.

Half-Bridge Converter

The half bridge converter in Figure 2-6 was developed to overcome the two fundamental problems of the push-pull circuit. These are, of course, the high voltage stress on the power switching elements and the difficulty of avoiding core saturation.

The output section of the half-bridge circuit is the same as that of the push-pull topology. Therefore, it has the same advantages of increased ripple frequency and reduced filter component size as the push-pull.

The salient difference of this topology over the push-pull circuit is the manner in which the power transformer excitation signal originates. First, a 'pseudo ground' is created at a potential halfway between the plus and minus nodes of the input voltage source V_{in} . This is formed by the capacitive divider, comprised of C1 and C2. Resistors R1 and R2 set the DC potential of the 'pseudo ground,' while the capacitors provide a low impedance AC return to the V_{in} voltage rails. One side of the power transformer T1 is connected to this return point. Switches Q1 and Q2 conduct on alternate half cycles and connect the other terminal of the primary to either the positive or negative V_{in} rail. As seen in the waveforms in Figure 2-6, this results in a transformer primary signal of $\pm V_{in}/2$ with respect to the transformer return point. As a result, the maximum voltage stress imposed on the power transistors is $2 \times (V_{in}/2)$, or V_{in} .

It should be noted that the half-bridge transformer primary is not center tapped like the push-pull transformer. This is due to the manner in which this topology generates a bipolar signal across the primary, causing the current flow through both primary terminals to alternate in direction. The push-pull transformer's primary center tap always has

positive current flow. Since the primary current of the half-bridge is a balanced alternating current, it can be capacitively coupled to the power switches. This is a tremendous advantage over other topologies. If the volt-second products of the two switches are not exactly equal, (which is a near certainty due to random component mismatch), instead of impending core saturation, a small DC voltage is developed across the coupling capacitor C3. This DC bias across the coupling capacitor serves to keep the net volt-second product seen by the transformer equal to zero, removing the possibility of core saturation from volt-second imbalance, or 'flux walking'.

Several specifics which should be noted include the relative values of the 'bias' capacitors C1 and C2, (they also act as input rectifier filter elements), and the coupling capacitor C3. When either of the power switches turns on, the coupling capacitor C3 must be charged before energy is passed on to the transformer. This charge must come from the bias capacitors C1 or C2. Consequently, C1 and C2 must be at least two orders of magnitude larger than C3 so that plenty of charge will be available for charging C3 at transistor turn-on. The value of C3 is constrained by two basic equations:

$$f_r = \frac{1}{2\pi\sqrt{L_{leak}C}} , \quad (2-1)$$

where f_r = resonant frequency,
 C = coupling capacitance,
 L_{leak} = transformer leakage inductance,

and,

$$V_C = \frac{I}{C}dt , \quad (2-2)$$

where V_C = capacitor charging voltage,
 I = average primary current,
 C = coupling capacitance, and
 dt = time interval capacitor is charging.

From inspection of the schematic in Figure 2-6, it is found that the coupling capacitor C3 forms a series resonant circuit with the inductance in series with C3. The inductance is the transformer leakage inductance at the primary of T1. The resonant frequency to which this gives rise is expressed in Equation (2-1). The value of the coupling capacitor should be set such that the resonant frequency is well away from the operating frequency of the converter.

Equation (2-2) relates the value of the coupling capacitance to the primary current and the charging voltage across the coupling capacitor. The charging time dt is the power switch 'ON' time. For predictable converter operation, the coupling capacitance C should be set such that the charging voltage is $\leq 10\%$ of $V_{in}/2$.

The diodes D1 and D2 are referred to as commutating diodes. They serve to dump the energy stored in the primary leakage inductance into the V_{in} voltage rails. This reduces the magnitude of turn-off spikes across the power elements.

This new and apparently 'perfect' topology does have some drawbacks, however. Since the excitation signal is half the magnitude ($\pm V_{in}/2$) of the same signal in the push-pull circuit, the current through the power switches must double to deliver the same power to the load. Increased current, though, is typically less of a restriction on power switch selection than high breakdown voltage.

Another drawback to the half-bridge circuit is the need for a floating base drive circuit since both power transistors are not referenced to ground as they are in the push-pull circuit. This adds to the complexity somewhat but can be used to advantage since it simplifies the isolation of the line input from the supply output. The power switches and the high voltage bus are isolated from the rest of the circuit by the power transformer and the base drive transformers.

Core utilization of the half bridge circuit is as good as that of the push-pull circuit. Power handling capability is comparable. Half-bridge designs are useful for applications demanding up to 1000 watts.

Full-Bridge Converter

The full-bridge topology of Figure 2-7 is a simple extension of the half-bridge circuit. In place of the biasing network which provides a return point at a potential equal to $V_{in}/2$, transistors Q3 and Q4 are now found. When Q1 is on, Q3 is also on. Likewise, when Q2 is on, Q4 is also on. As a result, the transformer excitation signal is now twice that of the half-bridge circuit, or $\pm V_{in}$.

Consequently, for comparable power output, the power elements' peak current demands are reduced by a factor of two. Circuit complexity is increased, but power handling capability is also increased. Full-bridge circuits have been used in applications requiring 2000 watts of output power.

In light of the above discussion, it appears that the minimum topology for the 600 watt application under consideration for this contract is the push-pull or the half-bridge circuit. Since the half-bridge offers lower voltage stress on the power elements, simpler transformer design, and inherent input-output isolation advantages, the half-bridge topology is the appropriate choice for this project.

Switchmode Power Converter References

In 1976, R.D. Middlebrook developed small signal models of the aforementioned switchmode power converters operating in continuous conduction mode [19]. Vincent Bello has applied these models to computer simulation of switching regulators [4,2,3]. His results were used in this project for computer modeling of the primary side pulse width modulation control loop. General discussions of switching regulator design techniques and

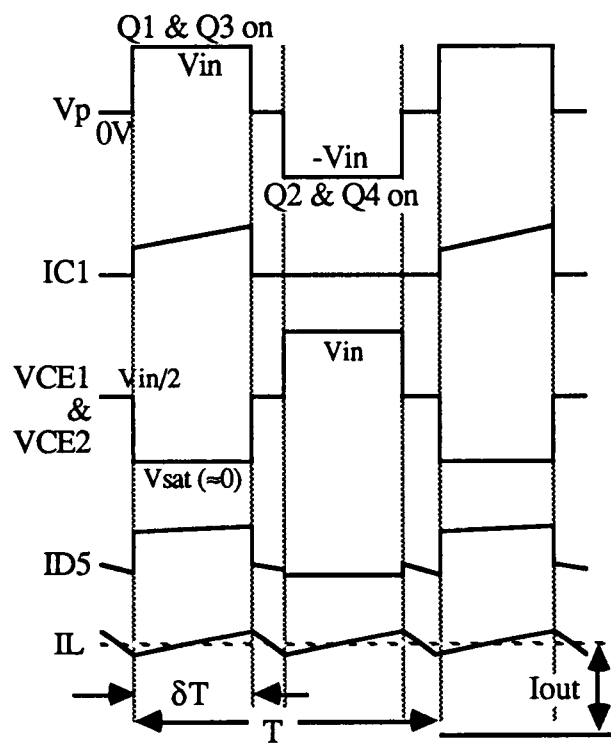
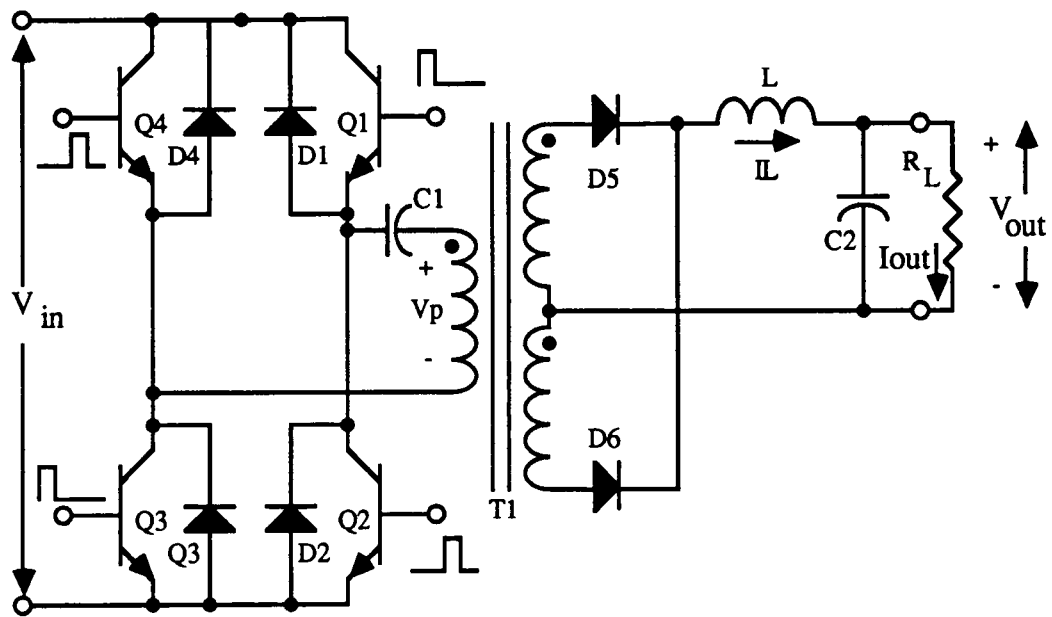


Figure 2-7. Simplified schematic of the full-bridge SPC topology and associated waveforms.

application examples can be found in [7,25,14,10]. Reference [8] discusses various aspects of power supply thermal considerations and includes several useful tables and examples.

Post Regulation

In typical switchmode power converter designs with multiple outputs, only one output is sampled for generation of the feedback signal to maintain regulation. The other outputs are regulated by the turns ratios of the power transformer output secondaries. When the sampled output section delivers the bulk of the total output power, regulation of the unsampled outputs can be maintained within about $\pm 5\%$. However, when power is distributed more evenly between the various outputs, regulation of the unsampled outputs becomes unacceptable due to increased losses in the unsampled output sections.

As specified in chapter I, the SPC designed for this contract has substantial power output on all three sections. As with most SPC designs, one of the outputs is sampled for overall pulse width control feedback. Since the remaining two output sections also deliver substantial power, they must employ some method of post-regulation in order to maintain adequate regulation of their output voltages. Since all of the outputs are isolated, the post regulation circuit can be made identical for the two 15V outputs, thus reducing design time and simplifying construction. For this reason, it was decided the 5V section would be the section regulated via primary side pulse width modulation and the $\pm 15V$ outputs would be regulated via secondary side regulation. Ideally, this post regulation should involve a minimum number of components, be highly reliable, and increase losses only minimally.

Magnetic Amplifier Introduction

An excellent post regulation technique is the magnetic amplifier circuit. Magamp technology was used a great deal in the middle of this century but lost ground as silicon

technology advanced. Now, SPC technology advances and magnetic core material advances have fueled a new interest in the magnetic amplifier circuit.

Figure 2-8 is a typical magamp switching power supply post regulator. This is a typical SPC output rectifier and filter with the addition of M1, D3, and a control block.

At the center of any magamp circuit is the saturable reactor--a magnetic core with an essentially square B-H curve that is easily saturated. The saturable reactor M1, as stated, has a square B-H characteristic curve, meaning it has essentially infinite inductance until the volt-seconds product across it is sufficient to saturate the core. At this point the reactor becomes a virtual short circuit. Utilizing this property of the reactor M1, the circuit holds off the beginning of the pulse arriving at the secondary of the power transformer from the primary side chopping circuit, thereby reducing the duty cycle of the squarewave arriving at the rectifier and filter. This is understood by examining the following two equations developed from magnetics theory [17]. Firstly, the expression for the volt-seconds product of the secondary voltage is:

$$V_1 T = (\text{const.}) N B A_e, \quad (2-1)$$

where

V_1	=	incident voltage,
T	=	time,
A_e	=	magnetic material cross-section area,
B	=	flux density,
N	=	number of turns.

Secondly, the secondary current is

$$I_1 = (\text{const.}) H l_m / N, \quad (2-2)$$

where

H	=	coercive force and
l_m	=	magnetic field path length.

These expressions allow the traditional B-H curve to be redrawn as VT vs. I as in Figure 2-9 [22].

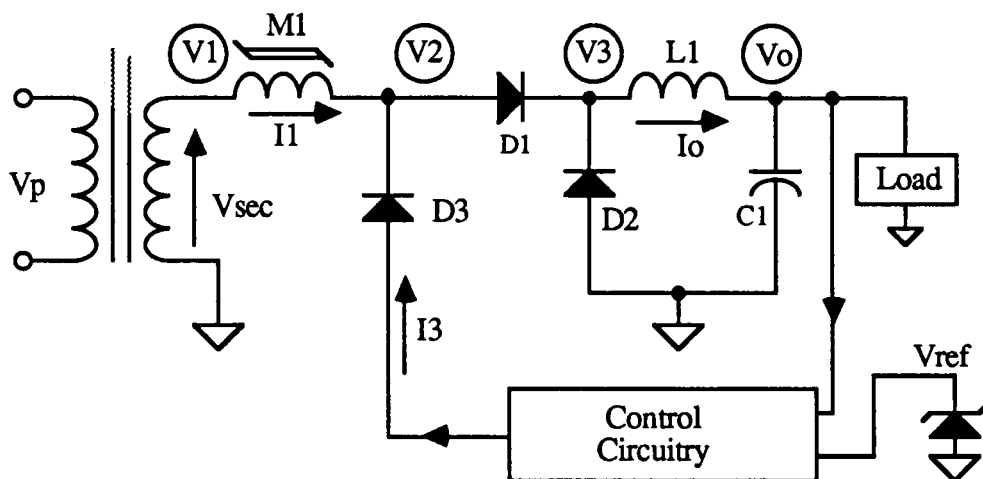


Figure 2-8. Magnetic amplifier regulator simplified schematic.

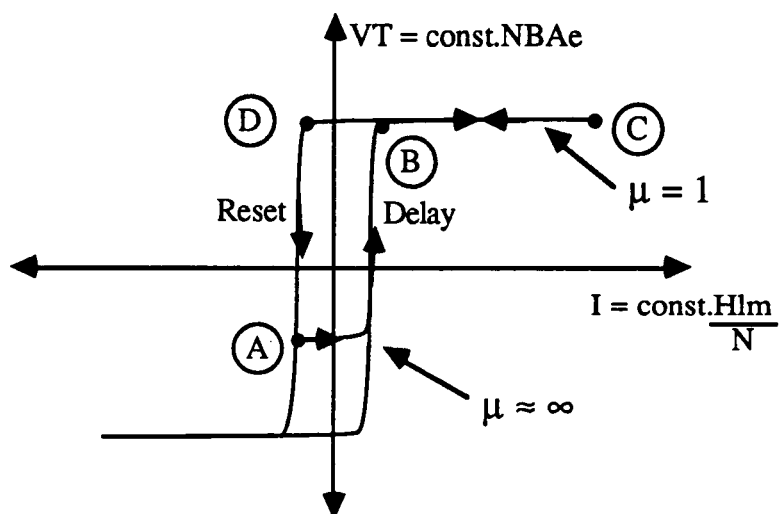


Figure 2-9. Saturable reactor V_T vs. I characteristic curve.

Starting at point |A|, a voltage pulse arrives at the secondary node V1 in Figure 2-8. The resulting voltage across M1 causes the traversing of the B-H loop from point |A| to |B|. The time it takes for this to occur is the amount of the incident pulse that is held off and not passed through to the output rectifier and filter. At |B| the core is saturated and acts much like a short circuit moving on to point |C| with high current and low loss. After the pulse from the primary ends, reset current flows through D3 and causes the B-H curve to be traversed back to point |D| and down to |A|, ready for another pulse. The amount of the incident pulse that is held off is determined by the magnitude of the reset current I_3 . It is this current which determines how low the point |A| reaches on the B-H curve, thereby setting the amount of delay before the core becomes saturated again when a positive pulse arrives at the secondary on the next cycle. The waveforms that result from this process are shown in Figure 2-10.

The control block in Figure 2-8 compares the output voltage V_o , to a reference and generates an error signal to modify the reset current I_3 . If the output voltage is too high, the reset current will be increased in order to increase the amount the core is reset. This, in turn, will increase the amount of time needed for the core to saturate when the next positive pulse arrives at the secondary of T1, effectively reducing the duty cycle of the square wave reaching the rectifier and filter, thereby reducing the output voltage.

The magnetic amplifier approach to SPC post regulation has been demonstrated as highly efficient and extremely reliable [9]. These features, combined with its simplicity made the magnetic amplifier the post regulation circuit of choice for this project.

Magnetic Amplifier References

Small signal models of the magnetic amplifier circuit have been developed by R. D. Middlebrook [17]. These models have been applied to computer simulation with the

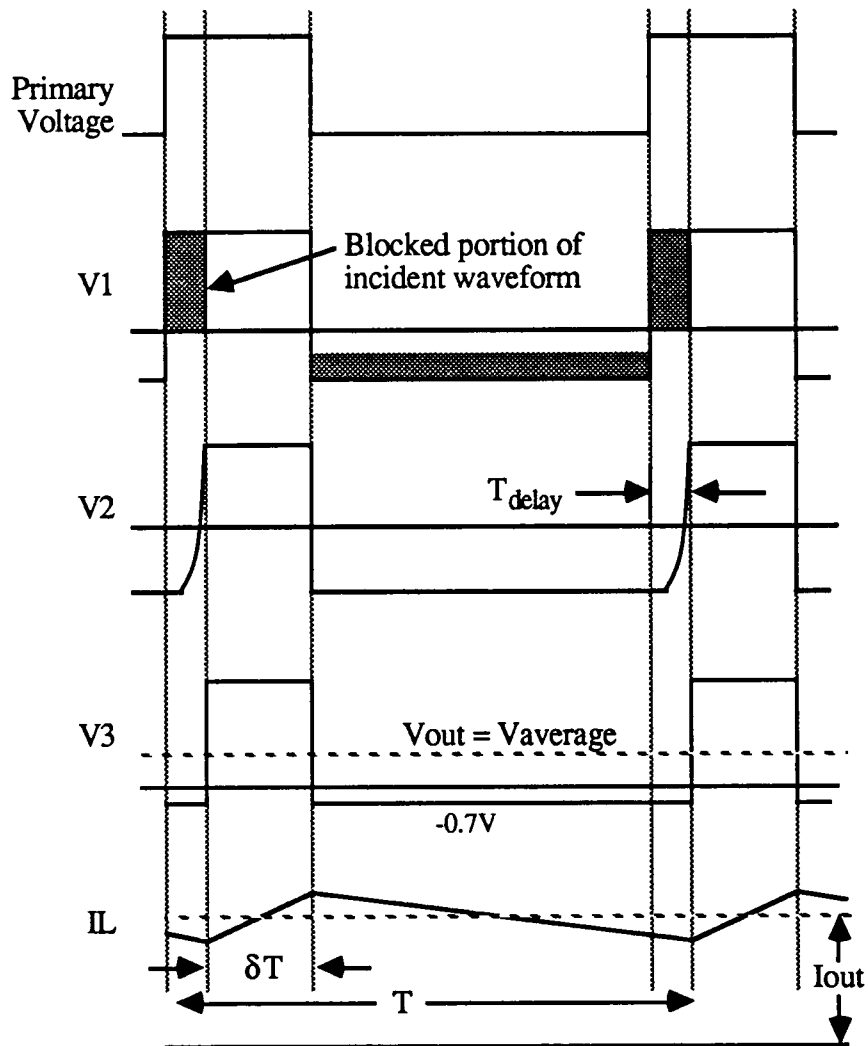


Figure 2-10. Waveforms for magnetic amplifier circuit in Figure 2-8 (not to scale)

SPICE circuit analysis program [28] and were utilized in this project for circuit behavior modeling.

In addition to the references just mentioned, chapter 5 of reference [14] is devoted entirely to the subject of magnetic amplifiers. References [11,13,9] are articles describing the development of specific application circuits utilizing magnetic amplifier technology. All of these sources were utilized in the development of this project.

CHAPTER III

RADIATION HARDENING CONSIDERATIONS

Radiation Effects Overview

As indicated in the specifications in the first chapter, this particular project is concerned only with gamma radiation hardening. Radiation damage in silicon devices can be split into two major categories: displacement damage, and ionization damage.

Ionization damage due to gamma rays occurs through photon interactions. These interactions produce free electrons and positive ions throughout the silicon. Ionization of this type results in two distinct damage mechanisms.

- (i) Photocurrent effects resulting in transient damage.
- (ii) Surface damage at silicon-silicon dioxide interfaces.

Photocurrent Effects

The first of these is a transient form of damage due to photocurrent generation. Excess carriers generated in the depletion region are immediately swept out and form drift currents. Carriers generated within approximately a diffusion length from the junction form diffusion currents. The magnitude of these currents, the primary photocurrents, is directly proportional to the dose rate of the incident radiation.

In the base region of a bipolar transistor, primary photocurrents not shunted by base resistance will give rise to secondary photocurrents due to transistor current gain. The deleterious effects of this phenomenon are only temporary but may cause state changes in sensitive digital applications. With proper design, however, photocurrent effects can be made negligible for most low dose rate applications.

Surface Damage at Si - SiO₂ Interfaces

Ionization damage at silicon, silicon-dioxide interfaces is permanent and is due primarily to positive charge buildup on the SiO₂ side of the interface and to creation of surface states at the interface.

As electron-hole pairs are generated in the surface oxide, the highly mobile electrons are swept out of the oxide by any electric field present. Most of the less mobile holes are also swept out of the oxide, but a few of them are captured by traps present within a few angstroms of the interface [20]. This gives rise to a positive charge buildup on the oxide side of the interface.

As total doses increase, surface (interface) states are generated. These states are located in the forbidden gap that behave like a high-density layer of recombination centers [12]. When electrons occupy these states, and holes are trapped in the overlying oxide, the resulting electric field can cause an inversion at the surface (interface) [12]. This behavior is quite analogous to the channel inversion in MOS devices. The mechanisms involved in the production of these surface states are not clearly understood and are discussed further in several excellent references [12,2,10,11].

Ionization surface damage effects resulting from positive charge buildup and negative interface states are summarized in Table 3-1 below.

Displacement Damage

As its name implies, displacement damage occurs when an atom is displaced from its normal position in a crystal lattice, creating a vacancy and an interstitial defect. Although gamma radiation is far less effective at causing displacements than fast neutrons and heavy ions [12], large total doses of gamma can generate enough displacements to significantly affect device characteristics.

Table 3-1. Summary of the effects of positive charge buildup and negative interface states in different device technologies [26].

Device	Primary property changes
Diodes	Increased junction leakage current Decreased junction breakdown Increased bulk resistance
Bipolar	Decreased current gain Increased junction leakage current Decreased junction breakdown Increased bulk resistance
JFET	Increased junction leakage current Decreased junction breakdown Increased bulk resistance Decreased transconductance Decreased saturation drain current
MOSFET	Negative shift in threshold voltage Increased drain-source 'ON' resistance Decreased transconductance

Displacement damage defects act as acceptors, donors, and recombination centers with energy levels between the valence band and the conduction band in semiconductors [12]. These types of defects can cause a decrease in majority carrier density, a decrease in majority carrier mobility, and a decrease in minority carrier lifetime [12]. In general, displacement damage tends to make the semiconductors more intrinsic [12]. Displacement damage effects on different device technologies are summarized in Table 3-2.

Application Specific Considerations

When a designer does not have the luxury of specifying custom processes, radiation hardened designs must be implemented with commercially available components. This basically means surveying literature for component irradiation test results, and performing irradiation tests, (when facilities are available), to find components that can withstand the necessary dose.

For gamma doses on the order of 10^7 rad, there are a wide variety of components available for electronic applications [20,26,12,29]. There are also a great deal of components which suffer dramatic performance degradation, or complete failure. For example, many SCR's, most MOSFET's, most optoisolators, and several linear application specific integrated circuits suffer unacceptable performance degradation.

In the following sections there are several tables presented with the results of radiation tests performed at the University of Tennessee. These tests were a part of the study mentioned in the first section of chapter I; the other facet of the subcontract through which this thesis project was funded. The complete results of this study are available in reference [29].

Table 3-2. Summary of the effects of displacement damage in different device technologies [26].

Device	Primary property changes
Diodes	Increased junction leakage current Increased junction breakdown voltage Increased bulk resistance Decreased storage time Increased junction dynamic 'ON' resistance Increased junction 'ON' voltage
Bipolar	Decreased current gain Increased junction leakage current Increased junction breakdown voltage Increased bulk resistance Increased turn-on time Decreased storage time Increased saturation voltage Increased junction dynamic 'ON' resistance Increased junction 'ON' voltage
JFET	Increased junction leakage current Increased junction breakdown voltage Increased bulk resistance Decreased transconductance
MOSFET	Increased drain-source 'ON' resistance Decreased transconductance

Power Switches and Rectifiers

As mentioned before, due to surface damage effects, MOSFET devices exhibit a negative threshold voltage shift when irradiated. For example, as discussed in section 4.2.2.7 in reference [12], a typical enhancement mode power MOSFET such as the IRF-150 is converted to a depletion mode device after only 20 to 30 KRad. Obviously, this type of device would be unsuitable for a 10 megarad application.

Consequently, component selection was focused on high power switching bipolars. Several potential candidates were tested, irradiated to 10^7 rd total dose, and retested. The results of these tests are in Table 3-3. As discussed earlier, the power switches must have breakdown voltages of >400 volts for safe and reliable operation. From Table 3-3 it is observed that, of the devices with a suitable breakdown voltage, the 2N6925 has the highest post-irradiation forward current gain. This data coupled with the high power capabilities (300 watts @ 25°C), extremely high power bandwidth ($f_T=10$ MHz @ $V_{CE}=10$ V, $I_C=2.0$ A), and excellent switching characteristics, make the 2N6925 a clear choice for this application.

As will be developed in chapter V, the power rectifiers in the 5V and ± 15 V output sections must sustain $I_F=10 A_{rms}$, $V_R \approx 25$ V and $I_F=4 A_{rms}$, $V_R \approx 75$ V worst case, respectively. Additionally, the output rectifiers must have low switching times in order to minimize losses. Table 3-4 shows radiation test results for several high speed power rectifiers.

The MBR3045PT is a good choice for the 5V volt section due to its high breakdown voltage and very low forward voltage. In addition, the MBR3045PT is packaged in a larger case than the other rectifiers (TO218AC). This allows for better heatsinking, maximizing reliability in the intended high temperature ($T_A=60^\circ\text{C}$)

Table 3-3. Radiation test results for bipolar power transistors.

Type	Mfr.	<u>PreIrradiation</u>			<u>Worst-Case After ≥ 10 MRad</u>		
		BV _{CEO}	BV _{CES}	6A, 2.5V	BV _{CEO}	BV _{CES}	6A, 2.5V
D44VH7	GE	140	200	70	180	200	27
2N6338	MOT	160	350	70	200	340	24
TIP35	MOT	160	430	92	250	440	23
2N5039	MOT	200	360	67	350	330	30
2N6925	GSI	560	720	32	670	760	15
SGSD0032	SGS	540	560	25.6(2A)	750	750	11.5(2A)
MJE13007	SGS	500	600	15(2A)	700	880	10.6(2A)
2N6927	GSI	650	800	26	750	800	10
MJE13090	MOT	600	850	20	600	650	9
D64V55	GE	510	770	23	650	740	6.7
2N6678	RCA	500	920	18	820	980	6
2N6547	MOT	600	1000	12	640	640	4
MJH16010A	MOT	780	1150	13	800	800	3.3
MJ16004	MOT	800	1000	8.6	650	650	2
SGSBVV48A	SGS	600	720	15.7(2A)	950	1100	8.6(2A)
SGSD0042	SGS	540	730	10(2A)	690	1000	3.5(2A)

Table 3-4. Radiation test results for power rectifiers.

Part Number	Mfr.	Description	≥10 MRad Effects
MBR3045PT	MOT	Dual 30A, 45V Schottky	5-10% Increase in V(fwd) at 10A No change in BV(rev)
MBR2535PT	MOT	Dual 25A, 35V Schottky	No change
30CTQ30	IRC	Dual 30A, 30V Schottky	No change
MBR10100	MOT	10A, 100V Schottky	6% increase in V(fwd) at 10A 8% decrease in BV(rev)
MUR3010PT	MOT	Dual 30A, 100V Ultrafast recovery, PN junction	0-10% increase in V(fwd) at 10A No change in BV(rev)
MUR840	MOT	8A, 400V Ultrafast recovery, PN junction	4% increase in V(fwd) at 8A 16% decrease in BV(rev)
MR826	MOT	5A, 600V fast recovery, PN junction	7% increase in V(fwd) at 8A No change in BV(rev)
MUR8100	MOT	8A, 1000V Ultrafast recovery, PN junction	20% increase in V(fwd) at 10A 40% decrease in BV(rev)
MUR105	MOT	1A, 50V Ultrafast recovery	10% decrease in V(fwd) at 1A No change in BV(rev)
MUR150	MOT	1A, 500V Ultrafast recovery	No significant change
1N4933	Diodes, Inc.	1A, 50V Ultrafast recovery	No significant change
1N4936	Diodes, Inc.	1A, 400V fast recovery	No significant change
BR-66	Diodes, Inc.	Bridge Rectifier 6A, 600V	8% increase in V(fwd) at 6A No change in BV(rev)
MB88	Diodes, Inc.	Bridge Rectifier 8A, 600V	No significant change

environment. The MBR10100 was chosen for the $\pm 15\text{V}$ sections since it is one of the only lower voltage, Schottky rectifiers currently available with a sufficiently high reverse breakdown voltage.

The low frequency input line rectifier requirements can be met by either the BR-66 or MB88. The MB88 was the conservative choice due to its higher current capabilities.

Miscellaneous Input Components

Inrush current is limited by the CL-50 from Table 3-5, (radiation test results for several inrush current limiters). The CL-50 is a resistance device that has a negative temperature coefficient (a thermistor). As temperature increases its resistance decreases. In this way turn-on inrush current of the input line rectifier circuit is limited since the current limiter is initially cool and has a sizeable resistance. As current flows through it, resistive heating causes the device to warm up and subsequently decrease resistance until it is effectively a short circuit and has no further effect on circuit operation.

A transient surge suppressor is another miscellaneous part on the input of the supply which had to be tested for radiation hardness. Several classes of these devices are shown in Table 3-6. The ZNR230 is a device known as a MOV, or metal oxide varistor. This is a nonlinear device that has a very interesting and useful property. As voltage across the device increases, its resistance drops dramatically, and can do so at very high speeds. In this manner, the device can effectively shunt short duration events, such as input line high voltage spikes caused by lightning or by line contamination from other devices on the power bus. As indicated in Table 3-6, these devices showed no appreciable damage after 10MRd.

Table 3-5. Radiation test results for inrush current limiters.

Part Number	Manufacturer	Description	≥ 10 MRad Effects
CL - 50	KEYSTONE	NTC, 6.3 Ω to 0.16 Ω	No apparent change
CL - 60	KEYSTONE	NTC, 10 Ω to 0.25 Ω	No apparent change
MCI - 1.0	MIDWEST COMPONENTS	PF, 1A 0.12 Ω to 250 Ω	No apparent change
MCI - 4.0	MIDWEST COMPONENTS	PF, 4A 0.025 Ω to 200 Ω	No apparent change

Table 3-6. Radiation test results for transient surge suppressors.

Part Number	Manufacturer	Description	≥ 10 MRad Effects
1.5KE170	MOTOROLA	120V ZENER	No Change
1.5KE250	MOTOROLA	250V ZENER	No Change
IN5908	MOTOROLA	6.5V ZENER	No Change
IN6276A	MOTOROLA	16V ZENER	No Change
ZNR230	PANASONIC	230V MOV	No Change

Capacitors and Magnetics

In general, capacitors and magnetics are quite insusceptible to gamma radiation for doses up to 10^7 rd [12]. There is some disagreement in the literature as to the exact mechanisms involved in capacitor radiation damage. These discussions are further complicated by the vast number of capacitor technologies available. The primary effects, though, seem to be increased leakage current, increased equivalent series resistance, and decreased capacitance. Ceramic capacitors were used in the small signal circuits. Capacitors in the high power path were polycarbonate and polypropylene, due to their low equivalent series resistance and subsequent high switching current capabilities.

The limiting factor for magnetic devices is the insulating material used. Due to its tendency to become brittle under moderate gamma doses, teflon should be avoided [12]. Polyvinyl-chloride, mylar, polyimide and most insulating varnishes maintain their pliability and usefulness quite well with moderate gamma doses.

Control Components

As discussed in chapter II, regulating the output voltage of a switching power supply requires a control circuit which compares the output voltage to a fixed reference. The result of this comparison is used to generate an appropriate base drive signal for the power switches. The control circuit varies the duty cycle of the base drive circuit as appropriate to maintain the required output voltage.

There are many commercially available single package pulse width modulation (PWM) control circuits which perform all of the above operations. In addition, most of these units also contain the necessary circuitry to implement 'soft-start' features, as well as current limit control. These packages make possible very low component count switchmode power converter implementations.

Previous tests conducted at the University of Tennessee indicate that very few of these controller packages offer much usefulness for total absorbed gamma doses of $\geq 10\text{MRd}$ [20,26]. From previous experience and discussions with the manufacturer concerning processing techniques, it was felt that the best candidate for use in the proposed radiation environment would be a new part from Unitrode Inc., the UCx825 series high speed pulse width modulation control IC. However, as shown in Table 3-7, in both biased and unbiased tests, four out of five parts failed at 80% of the proposed environment. Due to these results, it was decided to design the primary side pulse width modulation control circuit from separate components.

In addition to the PWM type circuits, other types of power supply management components were tested. Two that were used in this design include the SG3543 fault monitor, and the UC3838N magnetic amplifier controller. The SG3543 is used to detect over and under voltage conditions and generates TTL compatible open-collector signals to indicate output error conditions. These signals can be used by powered equipment to take actions appropriate for the indicated error. The magnetic amplifier controller is just as its name implies. It provides all the necessary functions to implement a magnetic amplifier control loop such as the post regulator used in the $\pm 15\text{V}$ output sections of this project.

As mentioned above, the primary side pulse width modulation controller is implemented with separate components due to lack of availability of rad-hard controller units. The PWM contains an oscillator, ramp generator, error amplifier, and comparators. In addition, logic gates and latches are needed for the summing and generation of timing and control signals. The 'LS' family of logic gates is known to be very rad-hard due to its bipolar technology and relatively high bias current levels [20,26,12]. Therefore, all logic functions in this design are implemented with 74LS' TTL integrated circuits.

Table 3-7. Radiation test results for pulse width modulation control circuits.

Part Number	Manufacturer	Description	≥10 MRad Effects
UC2825	UNITRODE	1MHz PWM	Failed starting at 8E+06 Some V(ref) drift Comparators failed
UC3825	UNITRODE	1MHz PWM	Failed starting at 8E+06 Some V(ref)drift Comparators failed
UC3838N	UNITRODE	Mag. Amp. Controller	Degraded V(os)--8mV (w.c.) Reduced A(OL), GB, SR Output current drive decreased by 25% V(ref) shift of +0.6% (w.c.) Still usable at >20 megarad
SG3543	SILICON GENERAL	Fault Monitor	Threshold decrease 2% Increase in fault indication delay 20-50%
SG3548	SILICON GENERAL	Quad Fault Detector	OV threshold increase 15% Failed in UV indication Failed in fault indication delay
UC3836	UNITRODE	Linear Regulator Low Dropout	2% change in V(ref) usable at >10 megarad

The error amplifier and integrating ramp generator are implemented with operational amplifier IC's. Table 3-8 shows results of radiation tests of several commercially available operational amplifiers. The OP42EZ from PMI exhibited excellent radiation hardness. Its acceptable offset voltage, high bandwidth, and high slew rate make it an excellent candidate for many radiation hardened applications. This, coupled with unity-gain stability and low cost were the reasons it was chosen for this project.

Table 3-9 has the results of radiation tests on several comparators from various manufacturers. As mentioned, comparators are necessary to implement some of the functions of the pulse width modulation control circuit. From Table 3-9, it is shown that there are several comparators that would be quite suitable for the application discussed here. Since the CMP05FZ offers the lowest offset, and is packaged in the smaller 8-pin dual inline package, it was chosen for this application.

The ability of a power supply to maintain regulation of its output voltages is of course largely dependent on the stability of the voltage references used in the circuit. In the case of a radiation hardened power supply, many voltage references must be tested to find a reference with a drift that is minimized over the course of the gamma dose absorption. Table 3-10 shows the results of tests performed on several commercially available voltage references. The clear choice is the TL431 from Texas Instruments. It is interesting to note that the 'identical' part from another manufacturer performed much worse after $\geq 10\text{MRd}$. In the area of radiation hardening, it is not unusual to find wide variation in radiation damage effects for parts with the same OEM part number from different manufacturers (or even wide variations in parts with different data codes from the same manufacturer). This is due to the different processing steps and methods a given manufacturer may use to arrive at a part with a given functionality. A rather pleasant coincidence pertaining to the choice of the TL431 as a voltage reference is its low price compared to many of the other references in Table 3-10.

Table 3-8. Radiation test results for operational amplifiers.

Part Number	Mfr.	Description	≥10 MRad Effects
AOP1510	ANADIGICS	150MHz GBW GaAs	Failed
CA3280AE	RCA	Dual, Differential Var. OTA, Bipolar input, High PSRR	4 of 8 failed, Max ΔV_{OS} =1.5mV 70% decrease in GBW 50% decrease in SR
CA3450E	RCA	200MHz GBW 220V/ μ s SR	1 out of 4 failed Max ΔV_{OS} =8.9mV, 27% dec. in SR, 24% dec. in GBW
LT1028	LINEAR TECHNOLOGY	Ultra low noise, Precision Low offset, High OL gain, PSRR, CMRR	Failed
OP42EZ	PMI	Fast, Precision JFET input GBW=10MHz, SR=50V/ μ s	Max ΔV_{OS} =4.2mV 21% decrease in CMRR 31% dec. in SR
OP470	PMI	Quad OP27, Bipolar input, High OL gain High CMRR, PSRR	Max ΔV_{OS} =78.2 μ V 30% decrease in GBW 16% decrease in OL gain
OPA111B	Burr-Brown	Precision, Low noise, JFET input, High OL gain, High CMRR	Max ΔV_{OS} =3.8mV 56% decrease in SR 11% decrease in PSRR
OPA606KP	Burr-Brown	JFET input High A(OL), SR High CMRR	Max ΔV_{OS} =58.8mV 25% decrease in SR 24% decrease in CMRR
RC4227FN	RAYTHEON	Precision, Dual OP27, Very low noise, Bipolar input, Low V_{OS}	Failed
MC34071P	MOTOROLA	Ground sensing, Gen. Purpose, Low-cost Bipolar	Max ΔV_{OS} =40mV, Reduced PSRR, CMRR, A(OL). I_B =5 μ A 50% decrease in SR, Still usable.
MC34081P	MOTOROLA	BIFET, SR=25V/ μ s GB = 8 MHz	Max ΔV_{OS} =33mV, I_B =3nA, Reduced, PSRR, CMRR, A(OL), GBW, SR, Still usable.
OP44	PMI	Fast, JFET input SR=100V/ μ s GBW=20MHz	Max ΔV_{OS} =6mV, I_B =3nA A(OL)>5E5, PSRR>85dB CMRR>100dB, I_{PS} inc. by 15% Excellent output drive

Table 3-9. Radiation test results for comparators.

Part Number	Manufacturer	Description	≥ 10 MRad Effects
CMP01EZ	PRECISION MONOLITHICS, INC. (PMI)	Fast, Precision Bipolar	Max ΔV_{os} = 1.87 mV Max ΔT_{pd} = 70 ns
CMP04FY	PRECISION MONOLITHICS, INC. (PMI)	Quad, Fast, Precision Open-Collector TTL Output Bipolar	Failed
CMP05FZ	PRECISION MONOLITHICS, INC. (PMI)	Fast, Precision Latch Circuit TTL Compatible Output	Max ΔV_{os} = 1.50 mV Max ΔT_{pd} = 26.4 ns
LM361N	NATIONAL SEMICONDUCTOR	Ultra-Fast Differential Input Complementary TTL Output Bipolar	Max ΔV_{os} = 1.94 mV Max ΔT_{pd} = 4 ns
NE521N	SIGNETICS	Ultra-Fast, Dual Differential Input TTL Compatible Output Bipolar	Max ΔV_{os} = 12.02 mV Max ΔT_{pd} = 22.2 ns
NE529N	SIGNETICS	Ultra-Fast Differential Input TTL/ECL Compatible Output Bipolar	Max ΔV_{os} = 1.87 mV Max ΔT_{pd} = 23 ns
SP9685	PLESSEY SEMICONDUCTORS	Ultra-Fast Latch Circuit ECL Compatible Output	Failed

Table 3-10. Radiation test results for voltage references.

Part Number	Mfr.	Description	≥10 Megarad Effects
AD584KH	ANALOG DEVICES	Precision, $\pm 15\text{ppm}/^\circ\text{C}$ $V(\text{out})=10.0\text{V}$ Band-Gap Reference	$\Delta V = -34.78\text{mV}$ (1.215V) $\Delta V(\text{out})=0.2368\text{V}$ to 0.5742V (10V) $\Delta\text{Line Regulation}=10.28\text{mV/V}$ (10V)
AD588AD	ANALOG DEVICES	High Precision Adj. Zener $\pm 1.5\text{ppm}/^\circ\text{C}$ Amplifier Output	$-23.0\text{mV} \leq \Delta V(\text{out}) \leq -1.0\text{mV}$ $\Delta\text{Line Regulation}=2\text{mV/V}$ (10V Output)
1N827A	?	Precision $\pm 10\text{ppm}/^\circ\text{C}$ 6.2V @ 7.5mA	$-2.1\text{mV} \leq \Delta V(\text{ref}) \leq -1.0\text{mV}$
LM199	NATIONAL SEMICONDUCTOR	6.95V MIC, $\pm 0.5\text{ppm}/^\circ\text{C}$ Temp. Controlled Substrate ($\approx 140^\circ\text{C}$)	$\Delta V = -12\text{mV}$
LM336Z	NATIONAL SEMICONDUCTOR	BG= 2.5V , Fixed $\pm\text{ppm}/^\circ\text{C}$	$\Delta V(\text{ref})=25\text{mV}$
LM385-1.2	NATIONAL SEMICONDUCTOR	BG= 1.235V , $\pm 20\text{PPM}/^\circ\text{C}$ Micropower	$V(\text{ref})=2.1\text{V}$ to 2.5V Failed
LM385-2.5	NATIONAL SEMICONDUCTOR	BG= 2.5V , $\pm 20\text{PPM}/^\circ\text{C}$ Micropower	$\Delta V(\text{ref})=0.1\text{V}$ to 0.4V Failed
MZ640	MOTOROLA	Precision $\pm 5\text{ppm}/^\circ\text{C}$ 6.2V @ 7.5mA	$\Delta V(\text{ref})=-26\text{mV}$
REF-01	PRECISION MONOLITHICS (PMI)	10V MIC, $\pm 8.5\text{ppm}/^\circ\text{C}$	$\Delta V = +28$ to $+48\text{mV}$
TL431	MOTOROLA	BG= 2.50V , $\pm 50\text{ppm}/^\circ\text{C}$ Adjustable Zener	$\Delta V(\text{ref})=+65\text{mV}$ $\Delta R(Z)=0.33\Omega$ to 5Ω
TL431	TEXAS INSTRUMENTS	BG= 2.50V , $\pm 50\text{ppm}/^\circ\text{C}$ Adjustable Zener	$\Delta V(\text{ref})=-0.4\text{mV}$ to -0.8mV $\Delta R(Z)=0.22\Omega$ to 0.7Ω

CHAPTER IV

DESIGN SPECIFICS

Circuit Overview

Off-line switchmode power converter (SPC) circuits can be broken into several major blocks to illustrate the circuit functionality from a global perspective. Figure 4-1 is a block diagram of the switchmode power converter designed for this contract. As discussed in chapter II, the basic topology employed in this design is that of the half-bridge converter. A block not mentioned previously is the auxilliary power supply. This block simply consists of a line frequency step-down transformer and subsequent rectifier and filter. The auxilliary power supply delivers bias current to the pulse width modulation control block.

Isolation between the various sections of the SPC should be noted here to clarify subsequent discussion. The $\pm 15\text{V}$ output sections are completely DC isolated from the rest of the circuit since they are each self-contained and are connected to the rest of the SPC only through the power transformer. The pulse width modulation (PWM) block shares a common ground with the 5V output section. However, the only paths between this ground and the line input ground are through the power transformer, the base drive coupling transformers, and the auxiliary power supply transformer. Therefore, these sections are also DC isolated from the rest of the SPC. Note that if the topology used here were that of the push-pull type, (which typically has a DC coupled base drive), the current & voltage feedback signals to the PWM would have to be transformer coupled or optically coupled to maintain proper isolation of the 5V output. This would be a consequence of the DC path that would exist between the line input ground and the PWM ground without these modifications. The additional circuitry in the path of the feedback control signals could compromise regulation accuracy, greatly increase complexity, and therefore reduce the

reliability of the design. Figure 4-2 is a detailed schematic of the SPC represented in block form in Figure 4-1.

Input Line Filter and Rectifier

The first block in Figure 4-1 includes an input radio frequency interference (RFI) filter. As discussed previously, the SPC presents a high frequency pulsating load on the AC line. This can lead to substantial radio frequency interference to other devices on the AC line. This can lead to substantial radio frequency interference to other devices on the AC line and in the vicinity due to electromagnetic radiation. Consequently, the SPC must be separated from the line input by a RFI filter. The filter usually consists of one or two L-C ' π ' sections. Filters such as these are commercially available in potted packages for single and multiple phase applications for varying load current requirements. The input line filter is a three-phase modular unit built by Filter Concepts, Inc. The unit is designed to handle up to 15 amps per phase at a line frequency of 50-60 Hz, quite sufficient for this application.

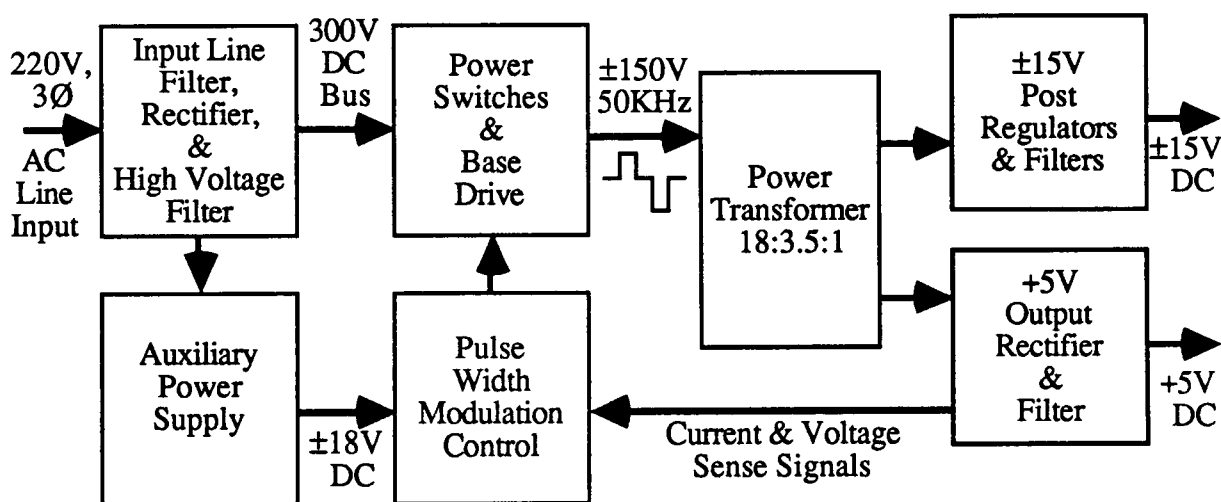


Figure 4-1. Switching power supply block diagram.

Following the line filter is the line rectifier and subsequent capacitive filter for generation of the high voltage DC bus. Referring to Figure 4-2, the rectifier diodes D1-D6 are part of the Diodes, Inc. MB88 bridge rectifier units. RT1 and RT2 are Keystone CL-50 inrush current limiters. They have a room temperature resistance of approximately 6 ohms and reduce to about two tenths of an ohm at operating temperature. C1 and C2 are filter capacitors and provide the high voltage DC bus for chopping. R1 and R2 balance the voltage distribution across C1 and C2 and provide a 'zero' reference for one side of the power transformer, as discussed in chapter II. Assuming a full power efficiency of 80%, the RMS current from the 300V DC bus is $(575W/80\%)/300V$ or $\approx 2.4A$ mps. From circuit theory, the following expression is known:

$$C = \frac{I t}{\Delta V},$$

where

C	=	capacitance across DC bus,
I	=	high voltage load current,
t	=	discharge time (1/ripple frequency), and
ΔV	=	peak to peak ripple voltage.

For a 50Hz, three phase system, the discharge time is approximately 1/300 or 3.3ms. Assuming a ripple voltage of 15V is allowable, C is calculated as 528 μ F. Since C is comprised of C1 and C2 in series, $C1 = C2 = 2 \times C \approx 1000\mu F$. For reliability, C1 and C2 are each comprised of two 470 μ F (standard values) capacitors in parallel. For the prototype circuit, three 470 μ F capacitors were used since the prototype system was evaluated with a single phase power source.

Power Switches and Base Drive

As discussed in chapter II, the half-bridge topology requires a floating base drive circuit since the devices are not referenced to a fixed ground. To satisfy this need for DC

isolation between the control circuit and the power switches, a transformer coupled circuit is employed as illustrated in Figure 4-2. Referring to Figures 4-2 and 4-3, circuit operation is as follows: When a positive pulse is applied to the base of Q3, the dotted terminal of T1 or T2 is pulled to ground by Q3. The other terminal is connected to the positive supply through resistor R10 or R11, the current limiting resistor. This shunts the primary and therefore the secondary, ending the 'ON' period of either Q1 or Q2. To turn Q1 on, the base of Q3 is pulled low. Q3 turns off, allowing the dotted terminal of T1 to 'flyback' positive, generating a positive pulse at the T1 secondary. This turns on Q1, initiating collector current. This current flows through the one turn secondary of T1. Due to transformer action, as positive current begins to flow through the collector winding of base drive transformer T1, a positive drive signal is induced at the base of Q1. This regenerative current maintains the base drive for the remainder of the switching cycle. The cycle is terminated by again saturating Q3, effectively shunting the primary of T1 and stopping the regenerative action of the secondary windings. Capacitors C16 and C17 serve to reduce the ac impedance seen looking into the secondary windings, thus decreasing switching times slightly. The value for resistors R10 and R11 is a compromise. Decreasing their value improves switching speeds of the power switches. Unfortunately, this also increases power dissipation of the drive circuit. The value of 120Ω was experimentally determined to be a good compromise for this application.

The circuit described above is known as a proportional base drive circuit since the turns ratio of the secondary windings forces a constant H_{FE} for the switching transistors. This transformer action of setting the ratio between the collector current and the base drive current varies the available base drive with load requirement--thus the 'proportional base drive' designation. As indicated in chapter II, the 2N6925 transistors from General Semiconductor Inc. were chosen as the power switching elements for the implemented half-bridge circuit. The preirradiation and postirradiation curves for the 2N6925 power

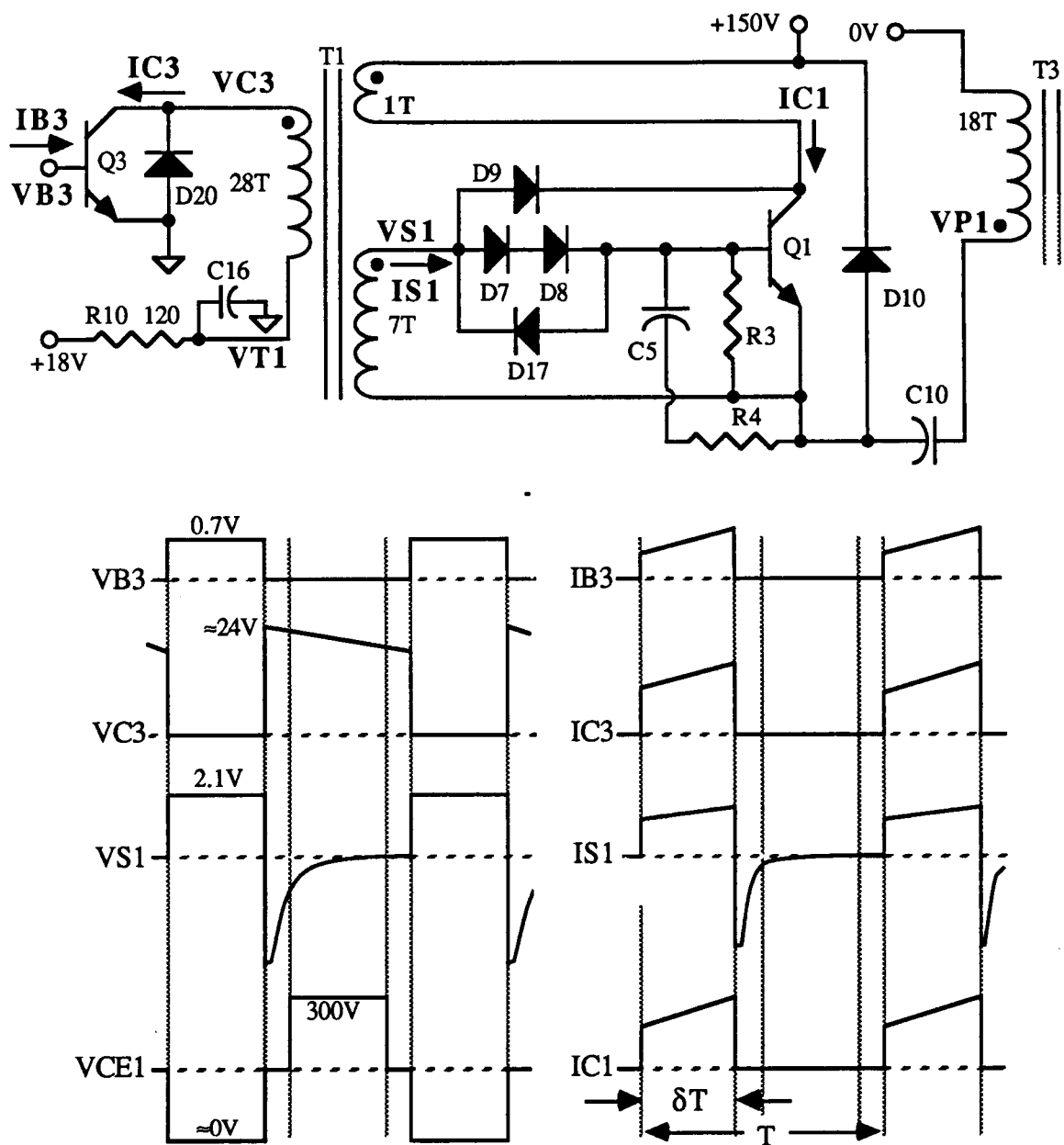


Figure 4-3. Base drive circuit waveforms.

transistor are shown in Figure 4-4. The turns ratio of the secondary windings of the base drive transformer is 7:1, as indicated in Figure 4-2. From the curves in Figure 4-4, it is shown that if the transistor is kept out of deep saturation, (V_{CE} is not allowed to fall below ≈ 0.6 volts), a forward current gain of 7 is obtainable before and after radiation exposure. This is a very important point since H_{FE} is known to decrease with increased radiation dose. If the circuit were designed to operate at a forced H_{FE} that were too high, the collector-emitter voltage would be too high, increasing power dissipation dramatically.

On the secondary of T1 are the base drive components. D7, D8, and D9 make up a Baker clamp to keep Q1 out of deep saturation and improve switching times. From the dotted terminal of T1, there are two diode voltage drops as well as a base-emitter voltage drop to the emitter of Q1. From the same terminal to the collector of Q1 there is only one diode voltage drop. Therefore, when Q1 is on, the minimum V_{CE} is the sum of one diode drop and the base emitter voltage or approximately 1.2 volts. In this manner, the Baker clamp is used to keep a transistor in a switching circuit from entering deep saturation. Shown in Figure 4-5a is the actual collector-emitter voltage, V_{CE} , during the on-time of switch Q1. Due to the transitory nature of the switching action, maximum V_{CE} while Q1 is conducting is approximately 0.7 volts, lower than expected but sufficiently high to keep the power switches out of deep saturation and maintain an H_{FE} of 7. In addition to improving the forward current gain, the Baker clamp also improves turn-off time since the amount of stored base charge is reduced by increasing the ON voltage. Also illustrated in Figure 4-5b are the high voltage switching waveforms for transistor T1.

Diode D17 provides a path for the turn-off base current flow. Often, D17 is replaced by a capacitor to rapidly remove stored base charge out of the power transistor and decrease cut-off time. Due to the exceptional speed of the 2N6925, however, it was experimentally determined that the use of a high speed diode such as D17 optimized the switching time of this particular circuit. It is important to note that although D7, D8, and

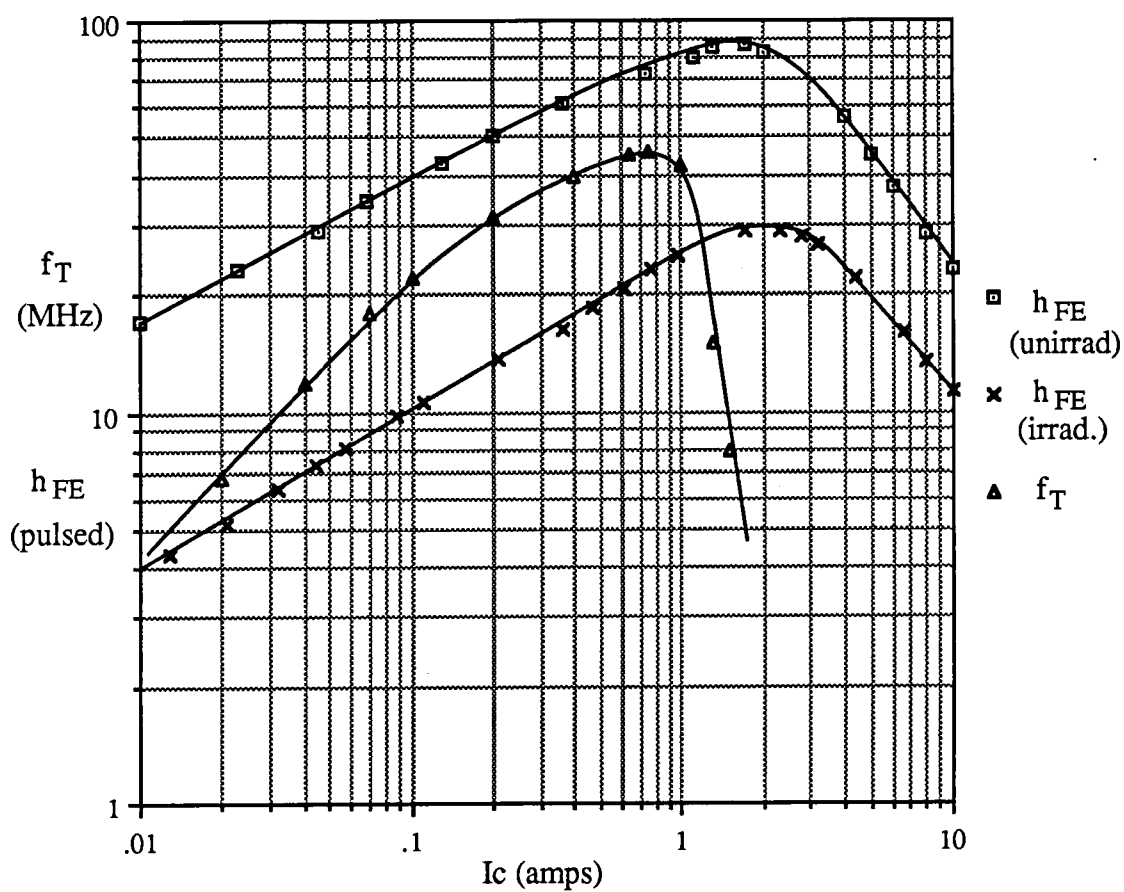
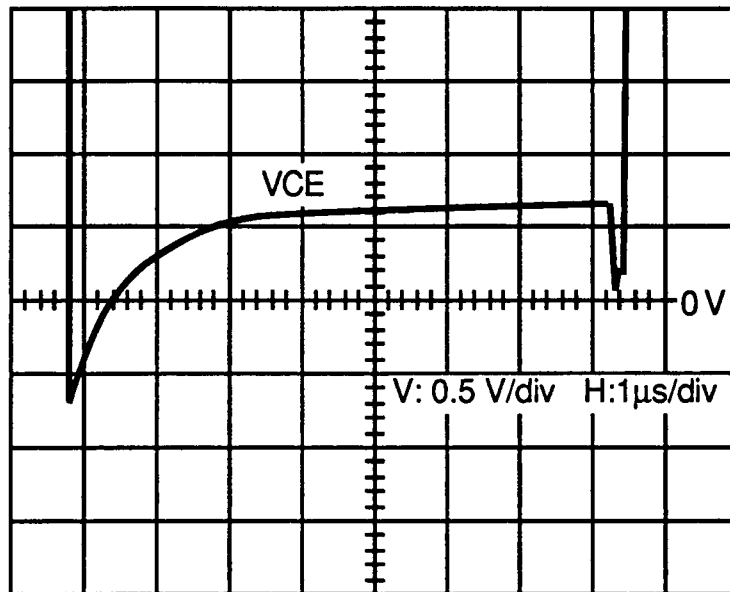
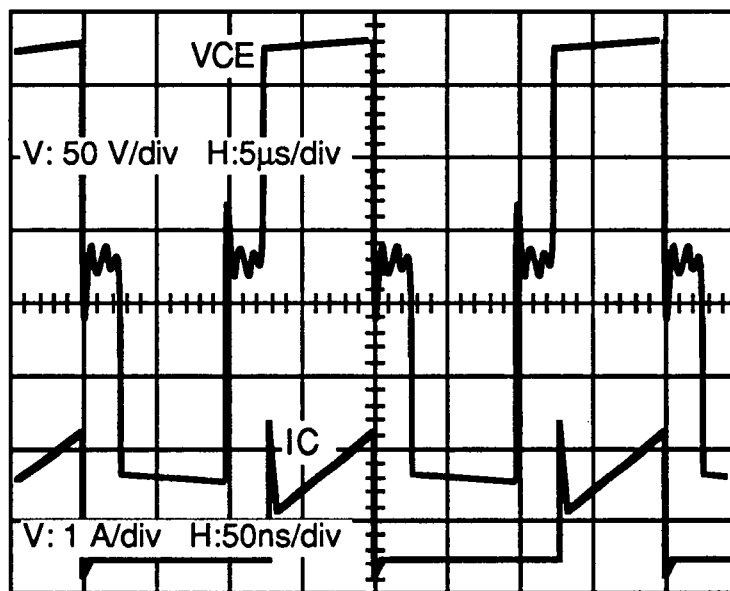


Figure 4-4. Preirradiation and postirradiation characteristics for the 2N6925 ($V_{CE} = 2.5V$)



(a)



(b)

Figure 4-5. Power transistor switching waveforms. (a) - V_{CE} during on-time. (b) - High voltage switching waveforms.

D17 do not need to have large breakdown voltages, D10 and D9 need to have the same BV_{CE} breakdown as that of Q1. D10 absorbs leakage inductance 'kickback' from the power transformer, T3.

Components R3, R4, and C5 provide some impedance by matching and snubbing of high frequency spikes that can cause inadvertent activation of Q1. The values for these components were determined from application notes [24] and experimental results.

Power Transformer

The power transformer was designed according to the Pulse Engineering document of reference [21]. This document is a collection of design equations and tables arrived at after years of experience in magnetics design. Most of the equations have a fundamental basis, but many have coefficients and exponentiation factors that have been arrived at empirically. Therefore, only results of this design process will be presented here.

It is important to point out a possible source of confusion in the SPC design field. Duty cycle is usually expressed in terms of the percentage of one of the power switches 'ON' time versus the total switching cycle period. Consequently, if a $\pm 150V$ bus is chopped and transformed, the energy delivered is actually 150V times twice the duty cycle. The maximum duty cycle, therefore, is 50%.

The following expression holds for the DC input-output relationship:

$$\frac{N_p}{N_s} = \frac{2 V_{in} D}{V_r + V_{out}}, \quad (4-1)$$

where

N_p	=	number of primary turns,
N_s	=	number of turns on one half of the center tapped secondary,
D	=	duty cycle,
V_r	=	output rectifier voltage drop,
V_{out}	=	output voltage, and
V_{in}	=	high voltage DC input.

Assume an average duty cycle of 35%, (a value which allows for efficient operation while leaving enough 'head room' for adequate transient response), an output of 5V, a secondary rectifier loss of approximately 0.7V, and a conservative value of 150V for the input DC. Substituting these values into Equation (4-1) yields a turns ratio of 18.4:1, or approximately 18:1 for S1, the 5V output secondary.

The $\pm 15\text{V}$ magnetic amplifier secondaries are S2 and S3. As described in chapter II, the magamp operates by reducing the incident duty cycle until the filtered output voltage is set at the proper voltage. The transformer turns ratio must be such that the magamp has enough adjustment dynamic range to ensure regulation over varying input line and load conditions. Good results can be obtained by assuming that the magamp must reduce the duty cycle by 25%. Therefore, the magnetic amplifier duty cycle D' is 0.75×0.35 , or 26.25%. Using this value in Equation (4-1) and 15 volts for V_{out} yields a turns ratio of 5:1, or approximately 18:3.5.

To summarize, the S2 and S3 secondaries have 7 turns, center-tapped. S1 has 2 turns center-tapped and the primary has 18 turns.

The 5V secondary, S1, was constructed from two turns of $0.0063" \times 1.08"$ copper foil, yielding a DC resistance of $0.96\text{m}\Omega$. S2 and S3 are each constructed from 7 turns of $0.005" \times 1.08"$ copper foil, with DC resistances of $3.6\text{m}\Omega$ and $4.0\text{m}\Omega$ respectively. The primary consists of two 18 turn parallel windings of #18 copper wire. The two primary layers are at the inside and outside of the transformer build. By paralleling windings in this manner, leakage inductance and resistive losses are minimized. The dimensions and specifics of the mechanical build of the power transformer are in Table 4-1. Constructing this on a Pulse Engineering SW-5 E (window width 0.42") core yields a core fill factor of $0.33/0.42$, or $\approx 79\%$. This is low enough to insure manufacturability.

Table 4-1. Transformer build specifics.

Layer	Description	Layer Dimensions (inches)	
	Coil Form		.040
1/2 of Primary	1 layer #18, 18 turns = .0424 3 layers .005 wrap = .015 (1st half of parallel 18 turn primary)	B _{W1} = .0424 B ₁ =	.0574
S3	7 layers .005 Cu foil (1 turn/layer) = .035 6 layers .005 ins (mylar) = .030 1 layer wrap = .005 (3.5 turns on each side of center tap)	B _{W2} = .065 B ₂ =	.070
S2	7 layers .005 Cu foil (1 turn/layer) = .035 6 layers .005 ins (mylar) = .030 1 layer wrap = .005 (3.5 turns on each side of center tap)	B _{W3} = .065 B ₃ =	.070
S1	2 layers .0063 Cu foil (1 turn/layer) = .0126 1 layer .005 ins (mylar) = .005 3 layers .005 wrap = .015 (1 turn on each side of center tap)	B _{W4} = .0176 B ₄ =	.0326
1/2 of Primary	1 layer #18, 18 turns = .0424 3 layers .005 wrap = .015 (2nd half of parallel 18 turn primary)	B _{W5} = .0424 B ₅ =	.0574
Total Build =			.3324"

From appendix E in the Pulse Engineering design manual [21], the following expression for primary inductance is found:

$$L_p = \frac{1.26 N_p^2 A_e (10^{-8})}{g + \frac{l_e}{\mu_m}}, \quad (4-2)$$

where N_p = number of primary turns,
 A_e = core cross-sectional area,
 l_e = magnetic path length,
 μ_m = core permeability, and
 g = effective gap length.

Filling in the appropriate numbers for the SW-5 core with 0.001" air gaps yields a primary inductance of 1.2 mH. The secondary windings are easily calculated from turns ratios.

Also from reference [21], appendix D, the following expression is found for primary leakage inductance of interleaved windings:

$$L_L = \frac{.85 M_t(ave) N_p^2}{L_w} \left(\sum W + \frac{\sum B_w}{3} \right) 10^{-8}, \quad (4-3)$$

where N_p = number of primary turns,
 $M_t(ave)$ = average mean turn of all windings,
 L_w = length of the winding of interest,
 $\sum W$ = insulation thickness of winding, and
 $\sum B_w$ = sum of the wire build for each winding.

Again, substituting the appropriate values yields a primary leakage inductance of 1.23 μ H.

Four of these transformers were fabricated and tested. One was wound by hand with parts graciously supplied free of charge by Pulse Engineering. The other three were fabricated by Coilcraft, inc. All of the major parameters were measured to extract a measure of the repeatability and accuracy of the design equations. Table 4-2 lists the measured and calculated parameters for these transformers. In this table there are several parameters defined. L_p and L_{leak} are the primary magnetizing inductance and leakage

Table 4-2. Summary of transformer parameter measurements for hand built and contracted power transformers.

Parameter	Calculated Value	Hand Made	% Error	Coilcraft #1	% Error	Coilcraft #2	% Error	Coilcraft #3	% Error
L _p (mH)	1.2	1.05	-12.5	1.14	-5.0	1.16	-3.3	1.06	-11.7
L _{leak} (μH)	1.23	2.06	67.5	2.20	78.9	1.65	34.1	1.65	34.1
L _{s1a} (μH)	3.7	3.30	-10.8	3.78	2.2	3.82	3.2	3.50	-5.4
L _{s1b} (μH)	3.7	3.25	-12.2	3.78	2.2	3.80	2.7	3.55	-4.1
L _{s2a} (μH)	45.4	41.9	-7.7	46.2	1.8	48.2	6.2	43.0	-5.3
L _{s2b} (μH)	45.4	42.3	-6.8	45.8	0.9	46.2	1.8	42.5	-6.4
L _{s3a} (μH)	45.4	41.9	-7.7	46.2	1.8	46.0	1.3	42.4	-6.6
L _{s3b} (μH)	45.4	42.5	-6.4	45.8	0.9	48.0	5.7	43.0	-5.3
R _{pac} (mΩ)	20.0	23.0	15.0	24.0	20.0	23.0	15.0	23.0	15.0

inductance respectively. R_{pac} is the DC resistance of the primary. L_{s1a} and L_{s1b} are the measured magnetizing inductance for each half of the 5V secondary. Similarly, L_{s2a} , L_{s2b} , L_{s3a} , and L_{s3b} are the magnetizing inductances for each half of the $\pm 15V$ secondaries.

Except for the leakage inductance, all measured parameters are very close to the calculated values. The large leakage inductance variations are not unexpected since this parameter is extremely sensitive to the winding process, insulation thickness variations, and the tightness of the windings. The Coilcraft #2 unit was used in the final prototype supply.

Using the Pulse Engineering design process equations, this transformer, when delivering the full power to the load, dissipates approximately 1.6W in copper losses and 3.7W in core losses. Using these numbers and another empirical equation, worst case temperature rise of the transformer is calculated as 30°C above ambient, which is well within the insulation and core material maximum operating temperatures for an ambient temperature of 60°C.

Output Filters

The output filter consists of a series inductor and a parallel capacitor. Consider the basic inductor equation,

$$V_L = L \frac{di}{dt} . \quad (4-4)$$

Approximating the differentials as delta values, Equation (4-4) can be rewritten as:

$$L = \frac{V_{out}(1-D)}{\Delta I_L f_s} , \quad (4-5)$$

where

V_{out}	=	output voltage,
ΔI_L	=	inductor ripple current,
D	=	duty cycle at output section, and
f_s	=	output ripple frequency.

If a ΔI_L equal to 10% of the output DC current is chosen, the inductor value is calculated using $f_s = 100\text{kHz}$ (full wave rectification doubles the ripple frequency), $V_{\text{out}} = 5\text{V}$, $I_{\text{out}} = 10\text{amps}$, and $D = 2 \times 0.35$. These values yield an inductance of $15\mu\text{H}$. Since the inductor value may decrease by as much as 30% at maximum output current, an available value of $26\mu\text{H}$ was chosen.

From circuit theory the following equation is known:

$$\Delta V_{\text{out}} = \frac{1}{C_{\text{out}}} \int_{t_1}^{t_2} i \, dt . \quad (4-6)$$

Integrating over the off-time of each cycle yields:

$$C_{\text{out}} = \frac{\Delta I_L}{8f_s \Delta V_{\text{out}}} , \quad (4-7)$$

where ΔI_L = inductor ripple current,
 f_s = ripple frequency, and
 ΔV_{out} = allowable output ripple voltage.

Using a worst case value of $\Delta I_L = 10\%$ of the 25 amp maximum output current, $\Delta V_{\text{out}} = 100\text{mV}$, and $f_s = 100\text{kHz}$, an output capacitance of $31\mu\text{F}$ is calculated. A $10\mu\text{F}$ and a $20\mu\text{F}$ capacitor were placed in parallel to achieve a value of $30\mu\text{F}$. Two capacitors are placed in parallel to decrease the equivalent series resistance (ESR) of the filter capacitor. The maximum allowable ESR of the output capacitor for a given output voltage ripple is

$$\text{ESR}_{\text{max}} = \frac{\Delta V_{\text{out}}}{\Delta I_L} . \quad (4-8)$$

For a ΔI_L 2.5amps, the ESR of the output filter capacitor must be less than $40\text{m}\Omega$. The capacitors used in this project have an $\text{ESR} < 5\text{m}\Omega$, well within the required value. The magnetic amplifier section filters are designed similarly.

Primary Side Pulse Width Modulation Control

As discussed in chapter III, no pulse width modulation (PWM) control IC's were located that could function reliably up to a total dose of $\geq 10\text{Mrd}$. Therefore, the control circuit is designed from separate components. The schematic for the complete PWM design is shown in Figure 4-6. Waveforms for various nodes of interest in this circuit are illustrated in Figure 4-7. (If not otherwise noted, discussions in this section refer to Figures 4-6, and 4-7.) The control circuit is comprised of both digital and analog circuit components. The circuit modulates the pulse width of the primary side switching signal by comparing an error signal to an oscillating ramp signal on every switching cycle. One of the two power switches (Q_1 or Q_2 in Figure 4-2) is turned on when the ramp is reset to zero. When the ramp voltage exceeds the error signal, the switch is turned off. If the error signal is larger, the on-time is longer.

U3 in Figure 4-6 is constructed from two TTL monostable multivibrators (one-shots) configured as an oscillator. Q2 and VREF2 form a series pass regulator to generate a well regulated +5V supply (V_d) for power to the digital portions of the circuit. U1 is the integrating ramp generator. Q1 resets the integrator ramp when turned on by the blanking pulse from U3a. Each of the two power switches are enabled on alternate cycles by the NAND gates U4a and U4b. U2a divides the 100 kHz asymmetrical signal by two, generating two symmetrical, 50 kHz, square waves, 180° out of phase with one another. These pulses are input to the NAND gates of U4 enabling each power switch on alternate half cycles.

Oscillator and Ramp Generator

One of the first choices to be made in the design of a switching power supply control loop is the operating, or switching frequency. Since many of the losses in the power supply often occur during the power switch transitions, increasing the operating

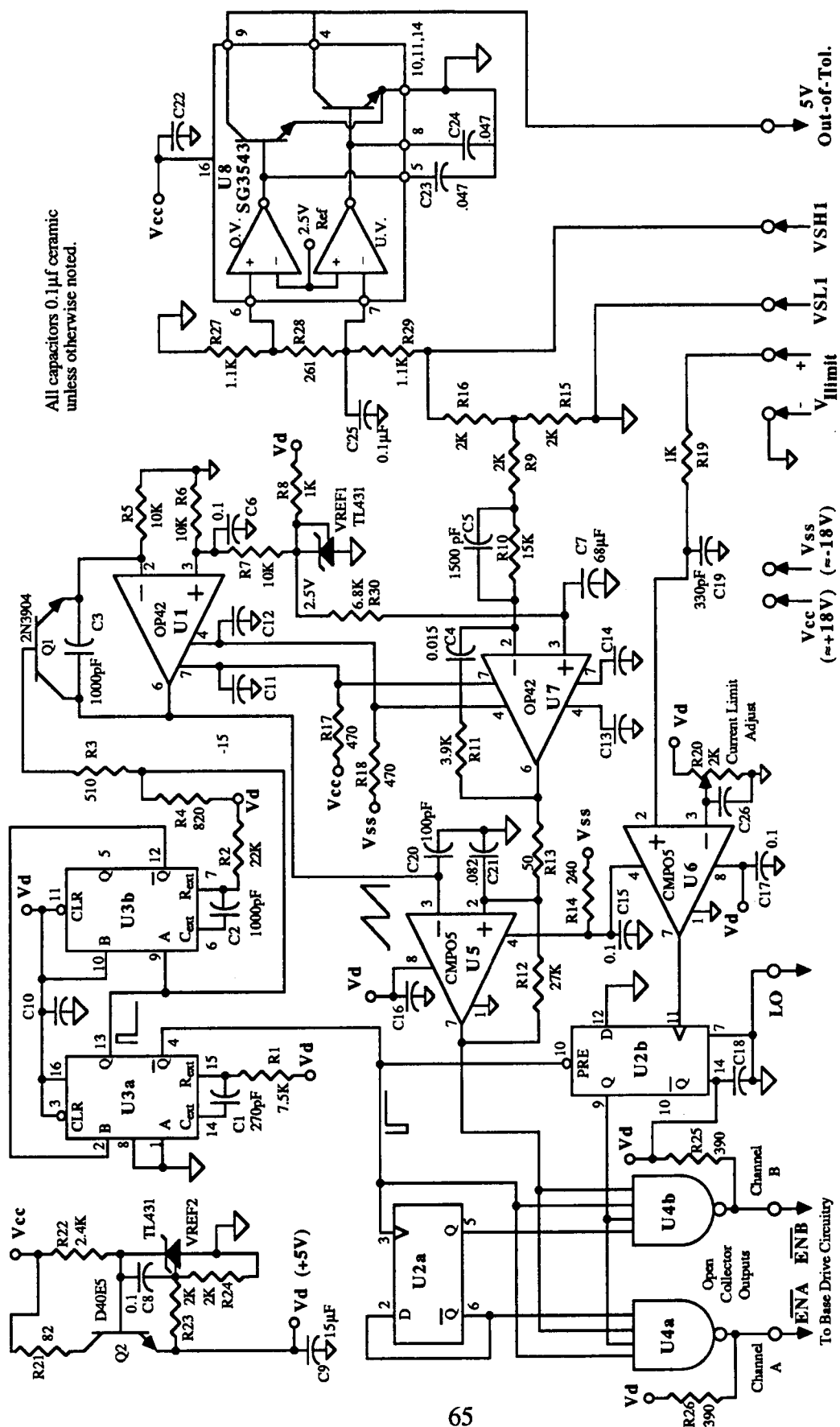


Figure 4-6. Primary Side Pulse Width Modulation Control Circuit.

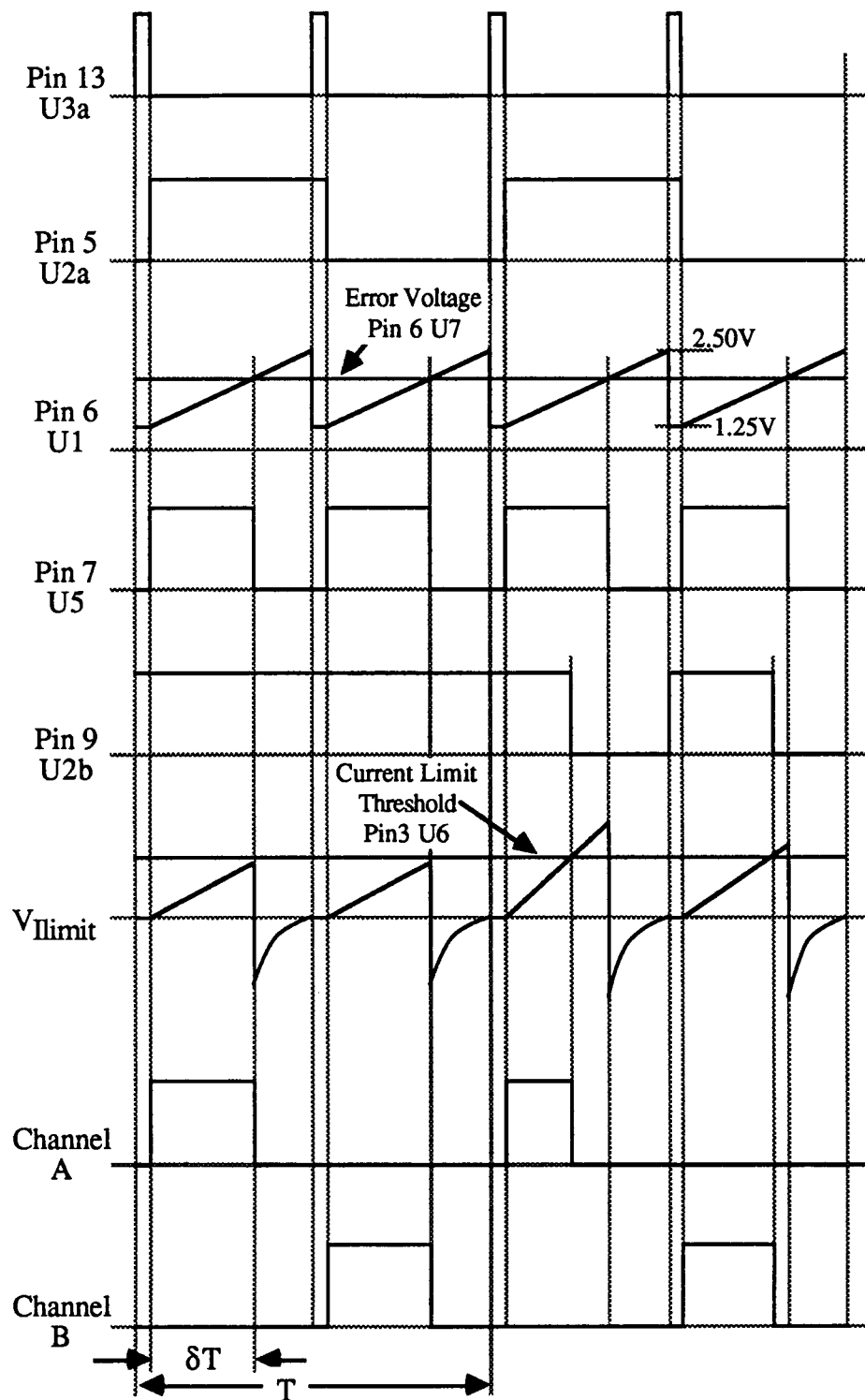


Figure 4-7. Pulse width modulation circuit waveforms.

frequency increases the number of transitions occurring in a given time interval. This indicates an increase in power loss with increasing frequency. On the other hand, increasing operating frequency reduces the size of the power transformer for a given power delivery, as well as the size of the output section filter elements. As in most engineering applications, there is a tradeoff associated with arriving at a particular parameter value. Further, since bipolar transistors rather than MOS transistors are used for power switches, the added time delays compromise the maximum switching frequency that is obtainable; if it were not for the radiation requirements, high-frequency power MOS devices, whose capability extends to operating frequencies > 1 MHz, would have been used. To further complicate matters, two of the secondaries have magnetic amplifier post regulators. These post regulators function by 'holding-off' part of the incident duty cycle. Since there is an inherent time delay associated with the reset and saturation of the saturable cores used to hold off the incident pulse, this would seem to indicate some minimum switching cycle time. Also, to insure short circuit protection, the magamp must be able to hold off an entire switching pulse. The combination of these criteria, coupled with some experimentation with the components in question, indicated that 50 kHz was a suitable compromise choice for the operating frequency of the power supply.

Since the primary side operating frequency is 50KHz, the PWM controller has a 100 kHz digital oscillator from which the 50 kHz primary side switching waveform is derived. The oscillator is composed of TTL one-shots U3a and U3b. At the end of each of the one-shots output pulses, the other one-shot is triggered. In this manner, positive feedback is enabled and continuous oscillation occurs. R1 and C1 set the oscillator blanking time at 750ns. R2 and C2 set the width of the rest of the cycle at 10 μ s, thereby setting the actual oscillating frequency at $1/(10.75\mu\text{s})$ or 93KHz. The blanking pulses at the outputs of U3a reset the integrator U1 and disable both NAND gates U4a and U4b. Disabling these gates terminates the current switching cycle and guarantees an 'OFF' time

between alternate power switch cycles so as to disallow the disastrous possibility of simultaneous conduction of Q_1 and Q_2 (Figure 4-2). The blanking pulse also resets the D-type latch (U2b) used in the current limit circuit.

The ramp generator is composed of the operational amplifier U1, clamping transistor Q1, and the TL431 voltage reference (2.5V). This 2.5V reference signal is divided by two, thereby placing 1.25V on the non-inverting input of U1. This causes a DC current to flow through R5 and the feedback integrating capacitance C3, which produces a positive ramp at the output of U1 due to the charging of C3. This ramp grows until the positive blanking pulse arrives at the base of Q1, thereby discharging C3 and resetting the ramp output. The voltage ramp height, V_m is determined from the following expression:

$$V_m = \frac{V_{ref}}{2} \frac{R_5}{C_3} T. \quad (4-9)$$

With a reference voltage of 2.5V, component values as shown in Figure 4-6, and ramp width T of 10 μ s, an output ramp height of 1.25V is obtained.

Error Amplifier and Comparator

The error amplifier, U7, is an OP-42 PMI unit configured as an integrator with additional compensation zeros and poles introduced by R11, C4, R10, and C5. The ideal 's' domain transfer function is easily found as

$$A(s) = \frac{-(1 + sR_{11}C_4)(1 + sR_{10}C_5)}{(s[R_9 + R_{10}]C_4)(1 + sR_9R_{10}C_5)}, \quad (4-10)$$

with the following frequency domain poles and zeros:

$$\begin{aligned} f_p &= 0, \text{ and } 60 \text{ kHz, and} \\ f_z &= 2.7, \text{ and } 7.1 \text{ kHz.} \end{aligned}$$

The analysis of the complete feedback response is given in chapter V.

The 5V output voltage is sampled by the high and low sense lines VSH1 and VSL1. This voltage is divided by the 1% metal film resistors R16 and R15 and compared to the 2.5V reference by error amplifier U7. The resulting error signal is compared to the ramp signal by comparator U5. The output of U5 is high at the beginning of a switching cycle. When the ramp voltage from U1 exceeds the error signal from U7, the output of U5 goes low, disabling the gates U4a and U4b. In this way, the error amplifier controls the pulse width of the power switches.

R13 and R12 provide some comparator hysteresis to insure clean transitions. The prototype circuit was spuriously triggered by electromagnetic coupling of the high voltage switching signal transitions to the positive input of U5. If the high voltage signal made a positive transition at turn-off, a positive signal was introduced at U5, causing the output of U5 to go positive, turning the power switch on again. When the coupled signal was dissipated, then the comparator went low again, turning the power switch off and restarting the process. Hence, power switch Q2 of Figure 4-2 oscillated on and off at the end of its switching cycle. Capacitors C21 and C20 were added to shunt this high frequency coupling and stop the spurious firing of comparator U5. The hysteresis resistors were also reduced to their present value in order to reduce the impedance at the input to the comparator U5, thereby minimizing the pickup problem discussed above.

Another important detail of this section of the control circuit is the soft-start feature implemented by R30 and C7. When a switching power supply is first powered up, it is important that the duty cycle be increased slowly to minimize transient start up currents and to insure that the systems powered by the supply are not exposed to damaging transient voltage levels. When the line voltage is first applied to the input of the power supply, the large time constant set by C7 and R30 causes the voltage on the noninverting terminal of error amplifier U7 to rise slowly, relative to the voltage levels in the rest of the circuit. This, in turn, causes the control circuit to increase the output voltage slowly since the

control loop forces the output voltage to track the reference voltage on the positive input of U7. Once capacitor C7 is fully charged, the soft-start components have no further impact on the operation of the circuit.

Base Drive Pulse Generation

The D type flip-flop U2a is used to divide the oscillator frequency by two. The two outputs are complimentary, symmetrical, square waves with a frequency of approximately 50 kHz. These signals alternately enable and disable the two power switches. Since the signals are complimentary, the two switches can never be enabled at the same time. The outputs of nand gates U4a and U4b are Schottky, open-collector signals, pulled up to +5V through 390 Ω resistors R25 and R26. These two signals directly drive the bases of Q3 and Q4 in Figure 4-2.

Current Limit

The I_{limit} signal that enters the PWM circuit is the voltage resulting from the bridge rectification of the 5V output return current, sensed by T4 in Figure 4-2 and converted to a voltage by R9. Transformer T4 divides the return current by a factor of 200; thus, the current limit voltage signal equals $I_{\text{return}}(R9/200)$. For a chosen current limit threshold of 28Amps, (this is 3Amps above the maximum current suggested by the 5V output), a 1 volt limit signal is delivered to the PWM circuit. A current-limit threshold adjustment is set by potentiometer R20.

During a switching cycle, the return current ramps up due to L1 in Figure 4-2. If the current ramps beyond the threshold set by R20, the output of comparator U6 goes high and clocks the D flip-flop U2b. This drives pin 9 of U2b low, ending the current switching cycle. In this manner, output current is limited on a pulse-by-pulse basis. U2b is reset by the blanking signal from the oscillator and armed for the next pulse.

Output Fault Detection

Under and over voltage faults are detected by U8, a special-purpose integrated circuit designed specifically for this function. Pins 6 and 7 are compared to an internal 2.5V reference. If pin 6 rises above 2.5V, then pin 9 is pulled low, indicating an output over-voltage fault. Similarly, if pin 7 falls below 2.5V, then pin 4 is pulled low by an internal transistor, indicating an under-voltage fault. The output voltage tolerance 'window' is set by the voltage divider resistor network composed of R27, R28, and R29. For this circuit, the fault setpoints are calculated as $V_o \text{ (high)} = 2.5V(R27+R28+R29)/R27$, and $V_o \text{ (low)} = 2.5V(R27+R28+R29)/(R27+R28)$, or approximately 5.6V and 4.5V (a $\pm 10\%$ out-of-tolerance condition). The two out-of-tolerance signals are wire-ORed to form a single open-collector output fault indication signal.

Auxiliary Power Supply

The auxiliary power supply delivers positive and negative DC voltages to the pulse width modulation control circuit. The power supply is composed of transformer T5, capacitors C3 and C4, and rectifier diodes D26-D29 in Figure 4-2. One phase of the three phase 220V line input is the input to the step-down transformer T5. The center-tapped secondary is full wave rectified and filtered by capacitors C3 and C4, resulting in approximately $\pm 18V$ DC signals. These voltages are supplied to the circuit of Figure 4-6 to supply bias currents for the various components. Before the bias voltages are delivered to the amplifiers and comparators, they are further filtered by the RC networks formed by the resistors R17, R18, R14 and the accompanying bypass capacitors. These resistors also decouple the control components from the switching frequency current pulses induced on the 'raw' voltages, V_{cc} and V_{ss} , by the drive transistors, Q3 and Q4 of Figure 4-2.

A +5V power bus is generated for the digital components by pass transistor Q2, and voltage reference VREF2 in Figure 4-6. The TL431 voltage reference is actually a +2.5V reference and error amplifier in one package. The voltage at the emitter of Q2 is

divided by two with R23 and R24 and sampled by the error amplifier in VREF2. By varying the current through R22, VREF2 sets the base voltage of Q2 such that the emitter voltage of Q2 remains at $(2 \times V_{ref})$ or 5.0V.

Magnetic Amplifier Post Regulators

As introduced in chapter II, the magnetic amplifier circuit is a highly reliable and efficient technique for post regulation of switching power supply output voltages. As discussed, post regulation refers to regulation of an output section on the secondary side of the main power transformer. The magnetic amplifier regulates its output voltage in a manner similar to the conventional switchmode power converters; the duty cycle of a switching voltage signal is adjusted to cause the regulated, filtered output to be maintained at a constant voltage regardless of input voltage changes and output load changes. However, in a conventional SPC, the input is a DC voltage signal which is chopped by the SPC to produce a pulse width modulated square wave. With the magnetic amplifier, the input is a previously produced square wave. The mag-amp reduces the duty cycle of the incident waveform to maintain a desired output voltage. To accomplish this, a saturable reactor is used to 'hold-off' a portion of the incident waveform on each half cycle, as discussed in chapter II. The magnetic amplifier circuit was designed by Dr. E.J. Kennedy, the author's thesis advisor at the University of Tennessee. This circuit is shown in Figure 4-8. The circuit utilizes the Unitrode UC3838 magnetic amplifier controller integrated circuit. This device integrates all of the major mag-amp control functions into one package. Also important is the exceptional radiation hardness of this device (see Figure 3-7).

Saturable Cores

As discussed in chapter II, the saturable reactor is an inductor with an essentially square B-H curve, as illustrated in Figure 4-9. The mag-amp utilizes this property to use

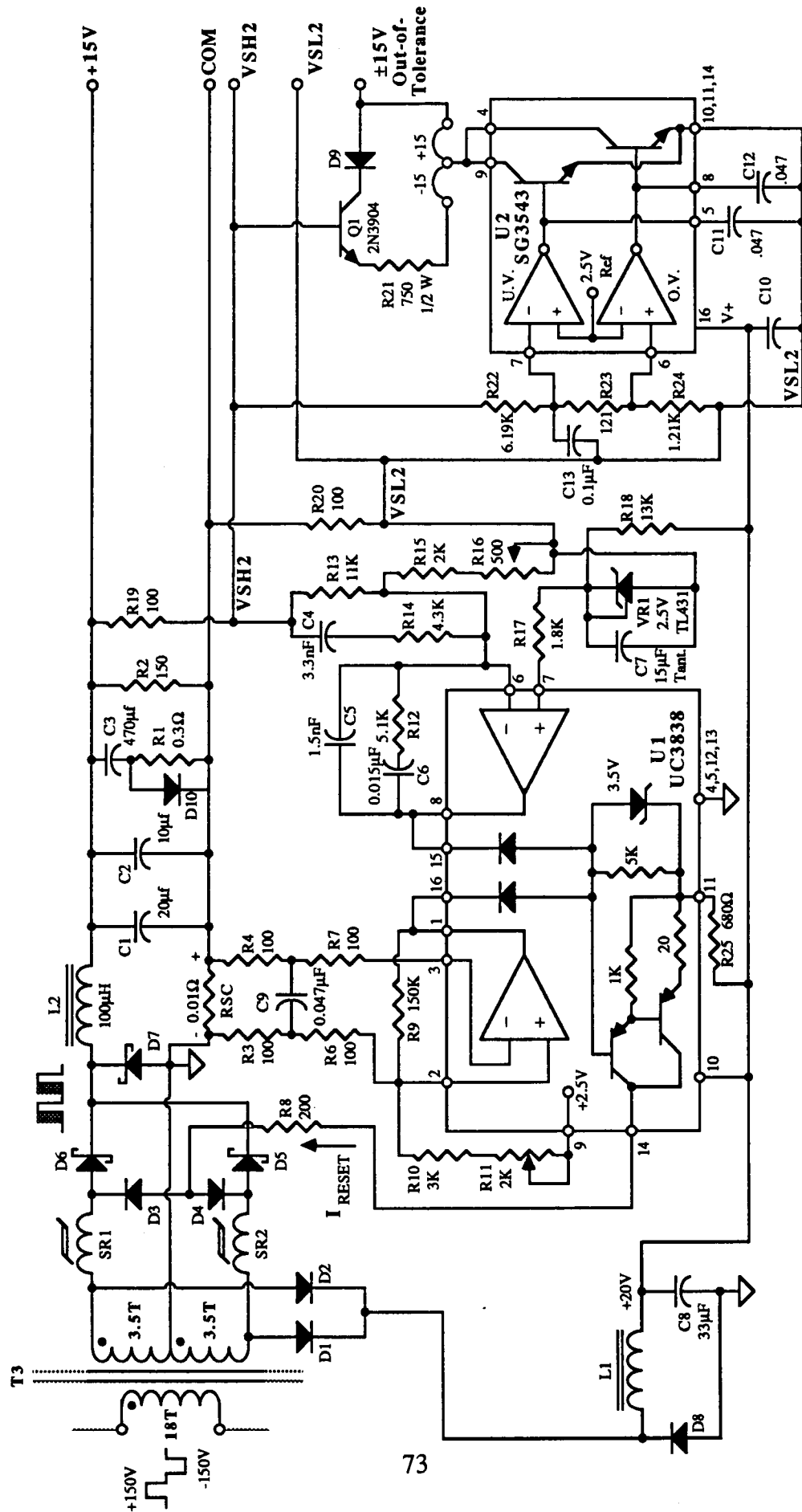


Figure 4-8. Magnetic amplifier controller circuit diagram.

the inductor as a switch. In Figure 4-8, there are two saturable reactors, SR1 and SR2. Since the secondary of T3 is center tapped, the two reactors alternate 'holding-off' a portion of the incident positive pulse on alternate half cycles. When the reactor is on the vertical portion of the B-H curve, ($|A|$ to $|B|$ on Figure 4-9), it acts as an open circuit ($\mu \approx \infty$), and when the volt-seconds product is sufficiently high (point $|B|$ on curve), the reactor becomes a virtual short circuit ($\mu = 1$). When the incident pulse is removed, (point $|C|$), if current is allowed to flow in the reverse direction, the saturable reactor traverses the B-H curve through point $|D|$ and returns to point $|A|$. The distance from $|A|$ to $|B|$ is the number of volt-seconds placed across the reactor before it conducts the incident pulse. Therefore, given an incident pulse magnitude, there is a particular time delay that elapses before the saturable reactor 'switch' closes and allows the remainder of the pulse to reach the rest of the output circuit.

The amount of the incident pulse that is held off is dependent upon how low on the B-H curve the point $|A|$ is located. The location of the reset point can be controlled in two

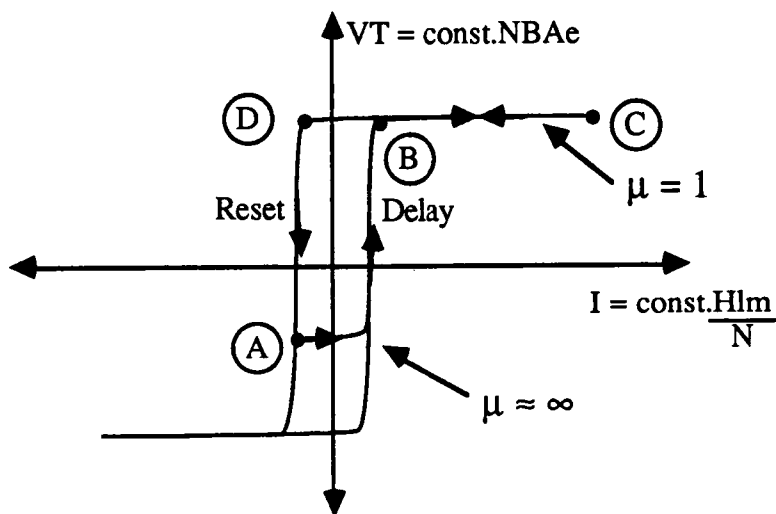


Figure 4-9. Saturable reactor VT vs. I characteristic curve.

ways. Clamping the reverse voltage that develops across the reactor during the reset process limits how far the core can reset. Alternatively, limiting the reset current also sets the location of the point I_A . It is this second approach that is used in the circuit of Figure 4-8.

The output DC voltage is directly proportional to the duty cycle of the pulses that pass through the saturable reactors SR1 and SR2, and is ultimately rectified by D6 and D5. The rectified pulses are filtered by inductor L2 and capacitors C1 and C2, giving rise to the desired DC output voltage. Since the duty cycle is controlled by the reset current, for a particular input voltage and incident duty cycle, it is possible to obtain the output DC voltage as a function of reset current. Figure 4-10 is just such a plot, obtained experimentally in this case for the Magnetics, Inc. 50B10-1E amorphous core. As illustrated in Figure 4-10, the V_{out}/I_{reset} relationship for a particular core can be varied by adjusting the number of windings on the core. To allow for output short circuit conditions, the core must be able to sustain the entire incident volt-seconds product without saturating. From figure 4-10, it is seen that the 40 turn reactor meets this condition. Hence, this is the saturable reactor configuration used in the prototype circuit. A similar amorphous core, (the Toshiba MB21X14X4.5 with 35 turns), was also tested. The Toshiba core exhibited behavior similar to the Magnetics core with slightly lower losses.

Error Amplifier and Reset Current Generation

Referring to Figure 4-8, at the end of a positive conduction cycle through SR1 and D6 into the output filter, the reactor SR1 reverses polarity due to the collapsing magnetic field in its core. Diode D3 'catches' the voltage flyback of SR1 and becomes forward biased, conducting reset current into SR1 through R8. As illustrated in the schematic, U1 contains two PNP transistors connected to form a current source for the reset of the

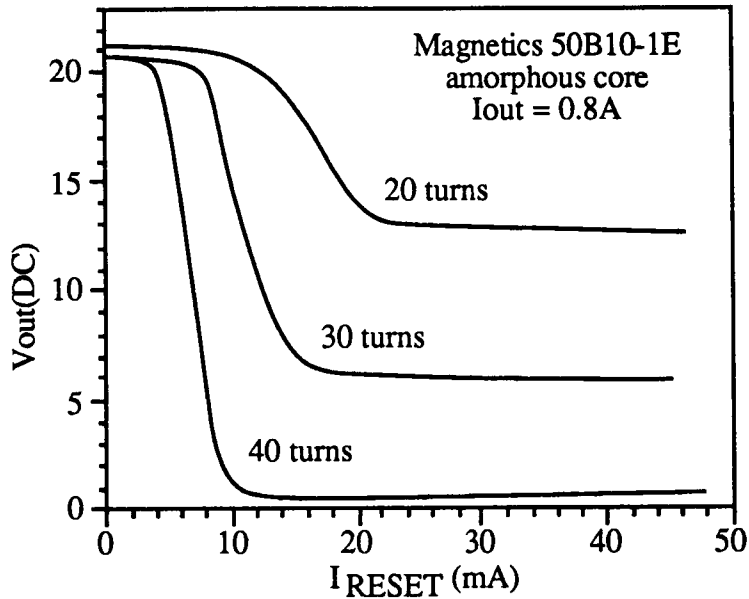


Figure 4-10. Output voltage vs. reset current for various numbers of core windings. $V_{secondary} = 30V$ and duty cycle = 0.36.

saturable reactors. If the DC output voltage is too high, the error amplifier (connected to pins 6,7, and 8 in U1) reduces the voltage on pin 8, increasing the current through the PNP current source. This increase in reset current increases the hold-off time, thereby reducing the duty cycle to the output filter and restoring the output DC voltage to its desired value. If the output voltage is too low, the error amplifier acts to decrease the reset current, thereby increasing the duty cycle and the output DC voltage. The small signal 's' domain transfer function of the error amplifier is found as

$$A(s) = \frac{-(1 + sR_{12}C_6)(1 + s[R_{13} + R_{14}]C_4)}{(s[C_5 + C_6]R_{13})(1 + sR_{12}C_5C_6/[C_5 + C_6])(1 + sR_{14}C_4)}, \quad (4-11)$$

with the following frequency domain poles and zeros:

$$\begin{aligned} f_p &= 0, 11.3, \text{ and } 23 \text{ kHz;} \\ f_z &= 2.0, \text{ and } 3.2 \text{ kHz.} \end{aligned}$$

The complete analysis of the magnetic amplifier closed loop response is given in chapter V.

Current Limit

One of the better features of the magnetic amplifier circuit is its inherent ability to integrate current limit control into the output voltage control loop. If the saturable reactors have been designed to accommodate the entire secondary volt-seconds product without saturating, the output can be current limited by summing a reset current signal into the control loop when an output overcurrent condition is detected. This is accomplished by the comparator (pins 1, 2, and 3) contained in U1. The output current is sampled by RSC in the output current return path. The threshold voltage is set by the voltage divider composed of R10, R11, R6, and R3. The actual setpoint is $2.5V((R3+R6)/(R11+R10+R6+R3))$. When the current through RSC is sufficient to cause a voltage drop greater than the setpoint, the output of the comparator drops to a low voltage, causing the reset current to be set at a maximum. With such a large reset current, the saturable reactors will sustain the entire secondary volt-seconds product and not allow any of the secondary signal to reach the output, effectively disconnecting the load from the power transformer.

Output Fault Detection

Under and over voltage faults are detected by U2, using the same device (the SG3543) as in the 5V control logic of Figure 4-6. Pins 6 and 7 are compared to an internal 2.5V reference. If pin 6 rises above 2.5V, then pin 4 is pulled low, indicating an output over-voltage fault. Similarly, if pin 7 falls below 2.5V, then pin 9 is pulled low by an internal transistor, indicating an under-voltage fault. The output voltage tolerance 'window' is set by the voltage divider resistor network composed of R22, R23, and R24. For this circuit, the fault setpoints are calculated as $V_o(\text{high}) = 2.5V(R24+R23+R23)/R24$, and $V_o(\text{low}) = 2.5V(R24+R23+R23)/(R24+R23)$, or approximately 15.5V and 14.1V (an

$\approx \pm 10\%$ out-of-tolerance condition. The two out of tolerance signals are wire-ORed to form a single open collector output fault indication signal.

Since the identical controller circuit is used for both +15V and -15V outputs, it was necessary to slightly modify the tolerance indication, using transistor Q1, diode D9, and resistor R21. For the +15V controller, pins 9 and 4 of U2 are connected together, so that a fault (UV or OV) on the +15V output will obtain a 'low' output relative to the 'common' terminal. However, for the -15V controller, the normal +15V output of the regulator is at the 'common' potential, while the low side (normally 'common') is now at -15V. Hence, for correct operation of the fault condition, (since now pins 4 and 9 of U2 are relative to -15V), it is necessary to add transistor Q1 and its circuit. Thus, when a fault (OV or UV) indication for the -15V supply produces saturation of the NPN output transistors of U2, then Q1 also saturates, producing a correct 'low' output, relative to the ground potential.

Thermal Considerations

Since the ambient temperature of the intended environment for this power supply may be as high as 60°C, particular attention must be paid to proper heat sinking of power components. Figure 4-11 illustrates the significant heat sink calculations. The prototype power supply was mounted on a 1/4" aluminum plate which was attached to the wall of the environmental chamber during testing. For the thermal calculations it is assumed that the aluminum plate is at the worst-case ambient temperature, 60°C. The power dissipation estimates come from estimates of the integral of the time varying voltages and currents across each of the devices. Most of the estimated 20 watts for the power transistors is dissipated during turn-off since the switches are driving an inductive load. For the power levels and heat sink geometries in Figure 4-11, the junction temperatures for the power switches, 5V rectifiers, and $\pm 15\text{V}$ rectifiers are 91°C, 91°C, and 93°C, respectively. These values are well within the maximum rated junction temperatures for the devices.

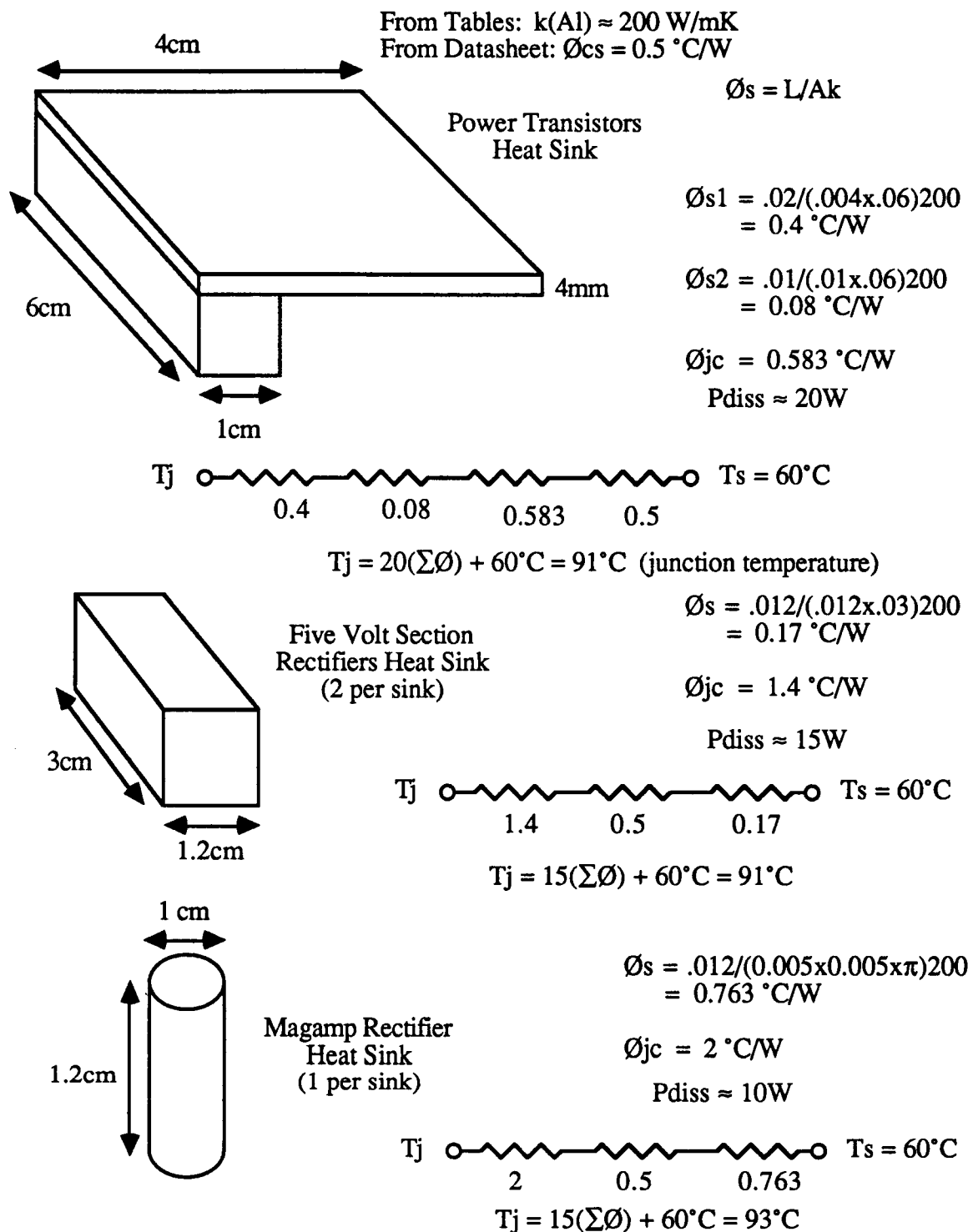


Figure 4-11. Geometries and calculations for power device heat sinks.

CHAPTER V

COMPUTER MODELING

Small Signal Approximations

Switchmode power converters are inherently non-linear systems, due to the manner in which their output signals are derived. Of course, many other electronic systems are non-linear also, but are analysed with linear analysis techniques. Obviously, this must be rationalized with an appropriate set of approximations and constraints on the parameters involved. In the well known case of the bipolar transistor, a small signal approximation is made in which the collector current is assumed to be a linear function of the base-emitter voltage. It is well known, however, that the collector current is actually an exponential function of base-emitter voltage:

$$i_c = I_s e^{\frac{qV_{be}}{kT}}. \quad (5-1)$$

The collector current can be rewritten as the sum of the DC current I_c and a perturbation current, $\hat{i}_c$ (this is often referred to as state variable format).

$$I_c + \hat{i}_c = I_s e^{\frac{qV_{be} + q\hat{v}_{be}}{kT}} = I_c e^{\frac{q\hat{v}_{be}}{kT}}. \quad (5-2)$$

The base emitter voltage, V_{be} , is also rewritten as the sum of a DC part and a perturbation voltage. If the perturbation signals are assumed to be small, the exponential term in Equation (5-2) can be rewritten with a power series expansion as follows:

$$I_c + \hat{i}_c = I_c \left(1 + \frac{q\hat{v}_{be}}{kT} \right). \quad (5-3)$$

Notice that since the perturbation voltage is assumed to be small, the higher order terms are assumed to be negligible. From this expression, one easily arrives at the familiar expression for the small signal transconductance, g_m ,

$$\frac{\hat{i}_c}{\hat{v}_{be}} = g_m = \frac{qI_c}{kT}. \quad (5-4)$$

In the case of switchmode power converters, the process of linearizing a non-linear system is very similar to the process described above. Each of the time varying signals is written in their state variable form. These include the input voltage source, the output current and voltage, and the duty cycle. From equivalent circuit models, the various parameters are combined into equations of state, and for the same reasons as the higher-order series terms above are neglected, nonlinear cross-products of perturbation terms also are neglected. The resulting equations are transformed into the frequency domain. From these equations, an equivalent linear circuit is drawn which can be used for analysis of the frequency response of the non-linear system from which the circuit originated.

Pulse Width Control Loop

The half-bridge converter is a part of a larger class of converters known as buck converters. The process just described was formalized for the buck converter by R. D. Middlebrook and S. Cuk in reference [19] . The equivalent circuit resulting from this process is illustrated in Figure 5-1. The following definitions apply to Figure 5-1:

$$\frac{\hat{v}_c}{V_m} = \hat{d}, \quad (5-5)$$

where

$\hat{v}_c$	=	the small signal control voltage,
V_m	=	the comparator ramp voltage magnitude, and
$\hat{d}$	=	the small signal duty cycle perturbation;

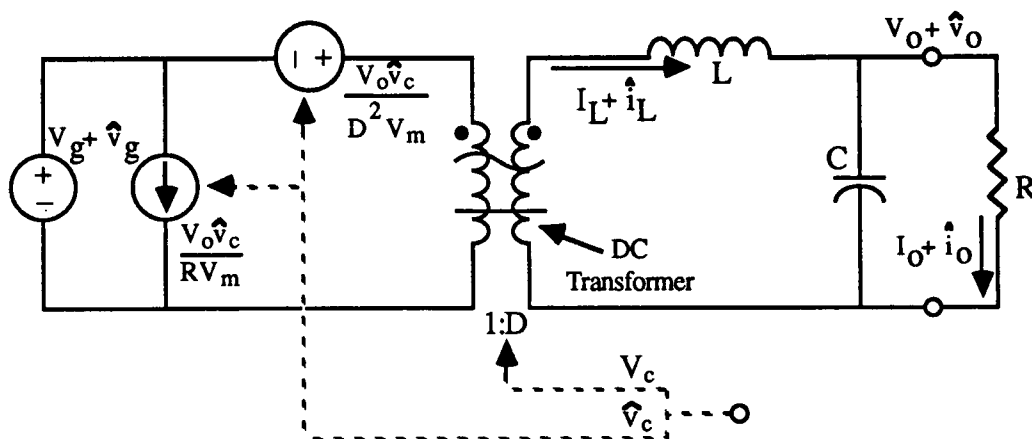


Figure 5-1. Small signal equivalent circuit of the buck converter.

$$D = ND_0, \quad (5-6)$$

where D = apparent duty cycle,
 N = power transformer turns ratio (N_s/N_p), and
 D_0 = nominal (DC) control duty cycle (V_o/V_m).

Now, knowing that the s-domain transfer function from the output to the control signal, $\hat{v}_c$, is $A(s)$ from Equation (4-8), the loop transmission for the +5V output can be written as

$$\begin{aligned} T(s) &= -A(s) \left(\frac{V_{out}}{D^2 V_m} \right) D H_e(s) \\ &= -A(s) \left(\frac{V_{out}}{D V_m} \right) H_e(s) \end{aligned} \quad (5-7)$$

where $H_e(s)$ = output filter transfer function.

Given that r_c and r_l are equal to the equivalent series resistance of the output section filter capacitor and inductor respectively, the following expression is found for $H_e(s)$ (assuming the output load resistance $R_L \gg r_c$ and r_l):

$$H_e(s) = \frac{(1 + sr_c C)}{(1 + sC[r_c + r_l + \frac{L}{R_L C}] + s^2 LC)}, \quad (5-8)$$

where

- C = output filter capacitance,
- L = output filter inductance,
- r_c = output filter capacitance series resistance, and
- r_l = output filter inductor series resistance.

From theory of second-order systems, it is known that the denominator of Equation (5-8) gives rise to a double pole centered about

$$f_p = \frac{1}{2\pi\sqrt{LC}}.$$

Also recall that the coefficient of 's' in the denominator of Equation (5-8) is proportional to the familiar damping factor, ζ . By increasing ζ , the Q of the LC filter is reduced. To avoid excessive peaking and phase shift in the loop transmission, it is necessary to adequately dampen the Q of the output stage. Equation (5-7) shows that by decreasing the output load resistance R_L, the damping is increased. However, at low load conditions it is not desirable to decrease the load resistance unnecessarily, since this will increase the power dissipation. However, the same effect can be accomplished for the AC small signal equivalent circuit by placing a small damping resistance in series with a large AC coupling capacitor across the output terminals, as with R8 and C9 in Figure 4-2 (or, R1 and C3 in Figure 4-8).

Using the values in Figure 4-2, the center frequency for the double pole of Equation (5-8) is 5.7kHz. Recall that the expression for the error amplifier transfer function is

$$A(s) = \frac{-(1 + sR_{11}C_4)(1 + sR_{10}C_5)}{(s[R_9 + R_{10}]C_4)(1 + sR_9R_{10}C_5)}, \quad (5-9)$$

with the following frequency domain poles and zeros:

$$\begin{aligned} f_p &= 0, \text{ and } 60 \text{ kHz;} \\ f_z &= 2.7, \text{ and } 7.1 \text{ kHz.} \end{aligned}$$

The components were chosen to place the two zeros in frequency space so as to cancel the dampened double pole of the output filter. The pole at $s = 0$ is a result of the integrator configuration of the error amplifier and maximizes the accuracy of the output voltage at DC. The 60kHz pole is added to cancel the high frequency zero created by the equivalent series resistance of the output filter capacitor.

SPICE 2 is a circuit analysis computer program written at the University of California at Berkeley and widely used in the electronics industry for design and verification of electronic systems. Vincent Bello used the results of R. D. Middlebrook to generate an equivalent circuit useful for modeling switchmode power converters [2,4] using the SPICE 2 CAD package. The equivalent circuit used to simulate the SPC designed here is illustrated in Figure 5-2. The duty cycle control of the output voltage is modeled with a voltage controlled transformer (dependent sources E1 and G1). To model the open loop gain, the coupling components L_{coup} and C_{coup} are set to very large values. The inductor closes the loop at DC and effectively opens the loop at the frequencies of interest. The capacitor disconnects the AC source from the loop at DC but couples the source into the loop at higher frequencies. In this way the loop remains stable at DC, and can be effectively opened for measurement of open loop gain at the frequencies of interest. In addition to the effects included here, there is a time delay inherent to the sampling nature of the control loop which is a function of the switching frequency. Since the switching frequency is much higher than the crossover frequency of the control loop, the inherent time delay was neglected to reduce the computational time necessary to perform the computer analysis.

Two other parameters of interest are the audio susceptibility and the closed loop transient response. The audio susceptibility is the line input to output transfer function with the feedback loop open. This is modeled with the AC source V_{audio} . With the other AC source, V_{ac} , set to zero, the audio susceptibility is easily calculated. By setting both L_{coup}

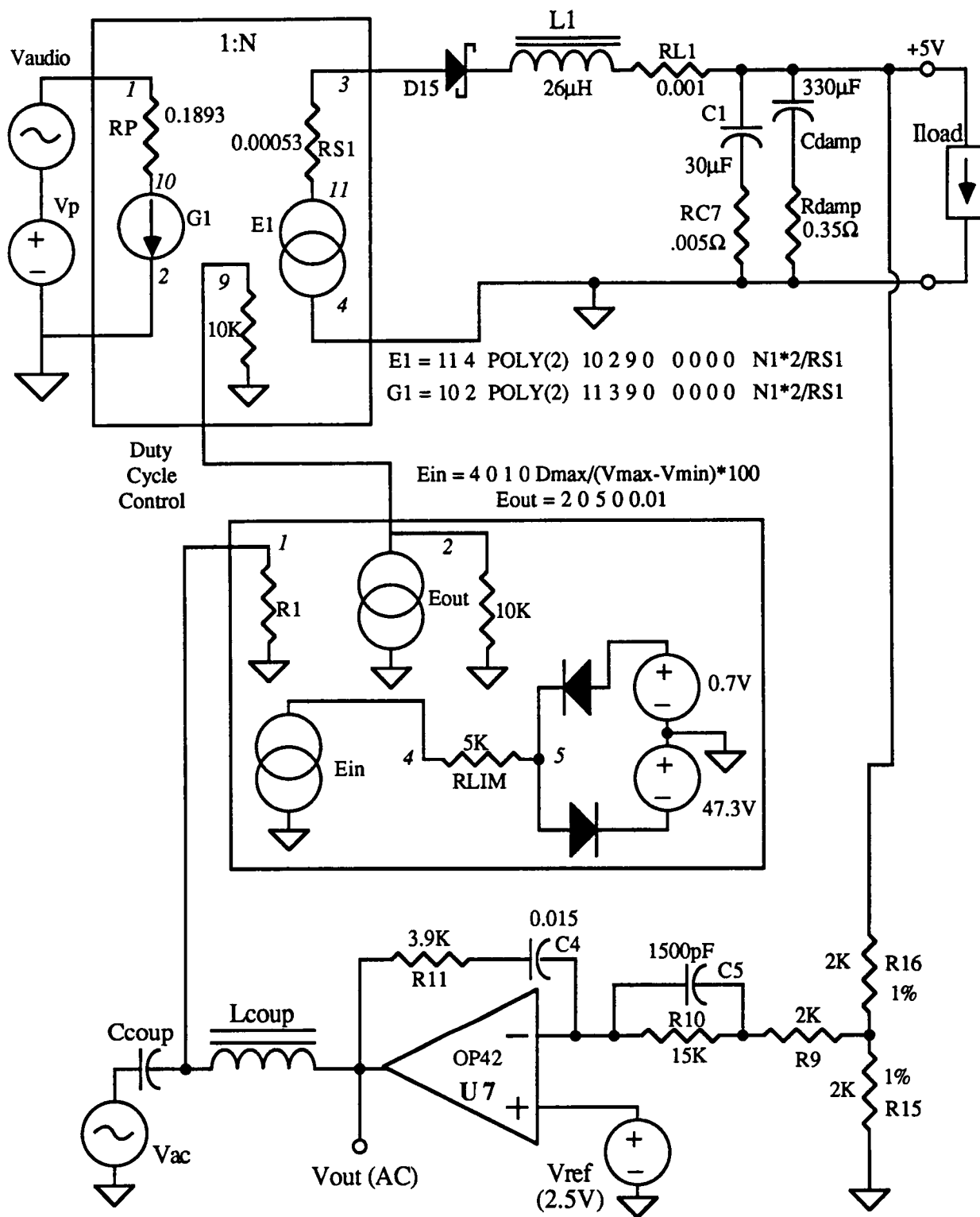


Figure 5-2. Equivalent circuit for computer simulation of half-bridge switching converter.

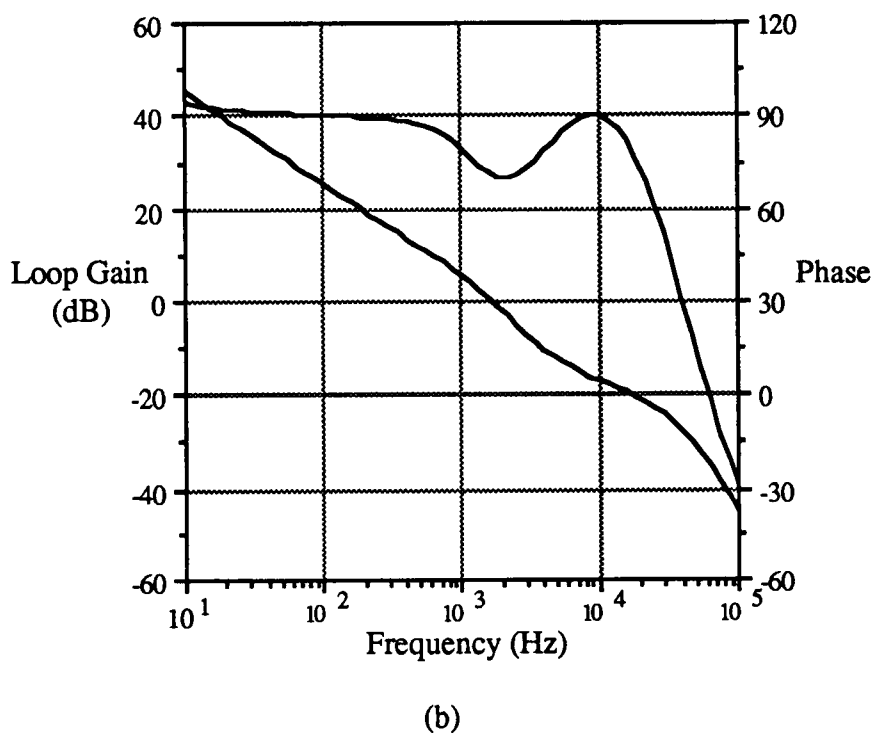
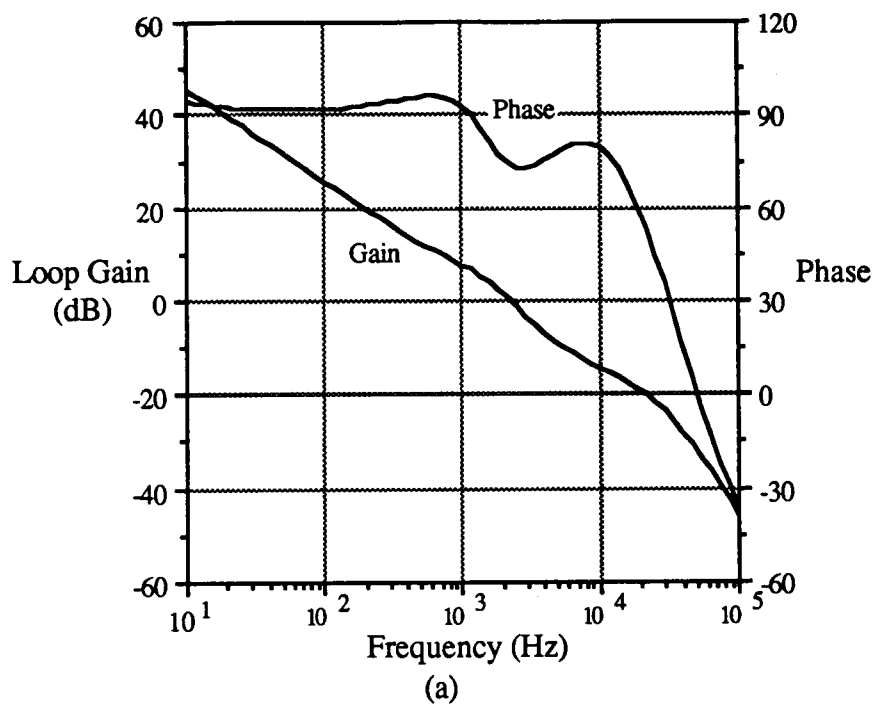


Figure 5-3. Five volt output open loop gain computer simulation results for, (a) - output current of 5 amps, and (b) - output current of 20 amps.

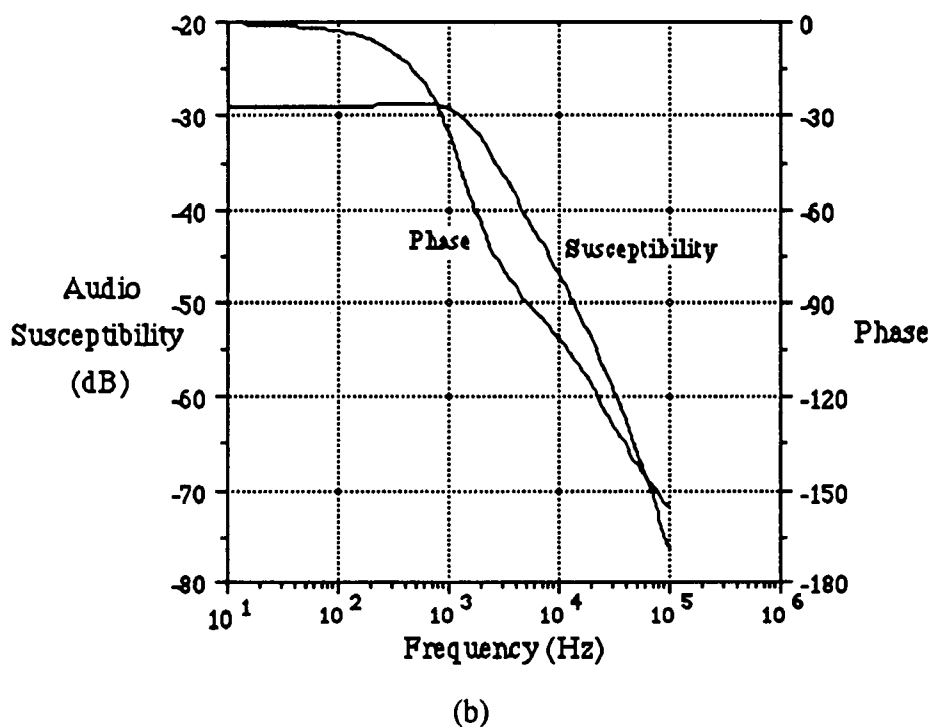
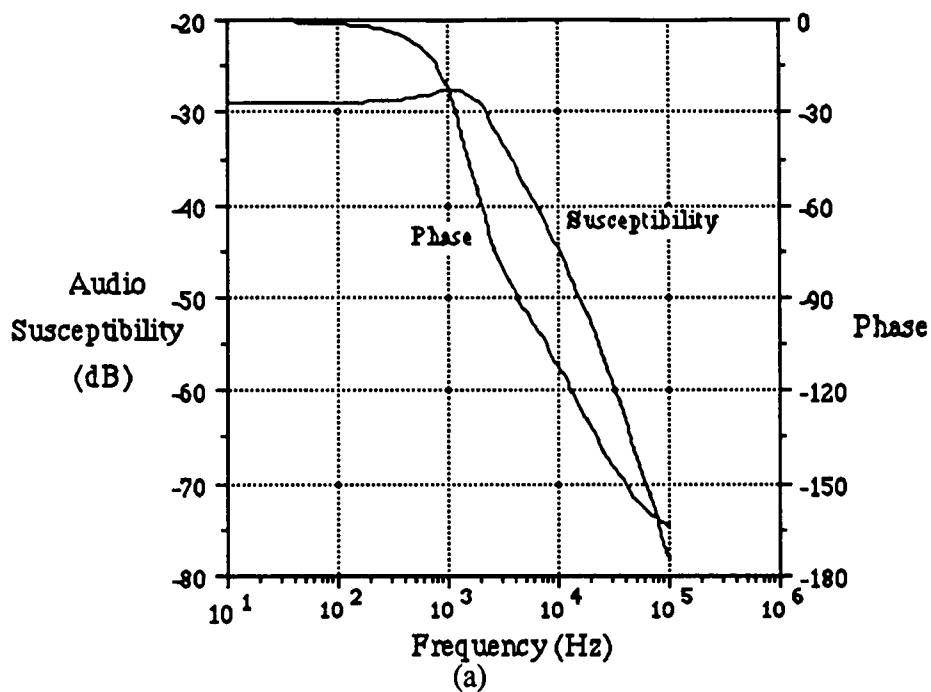


Figure 5-4. Five volt output audio susceptibility computer simulation results for, (a) - output current of 5 amps, and (b) - output current of 20 amps.

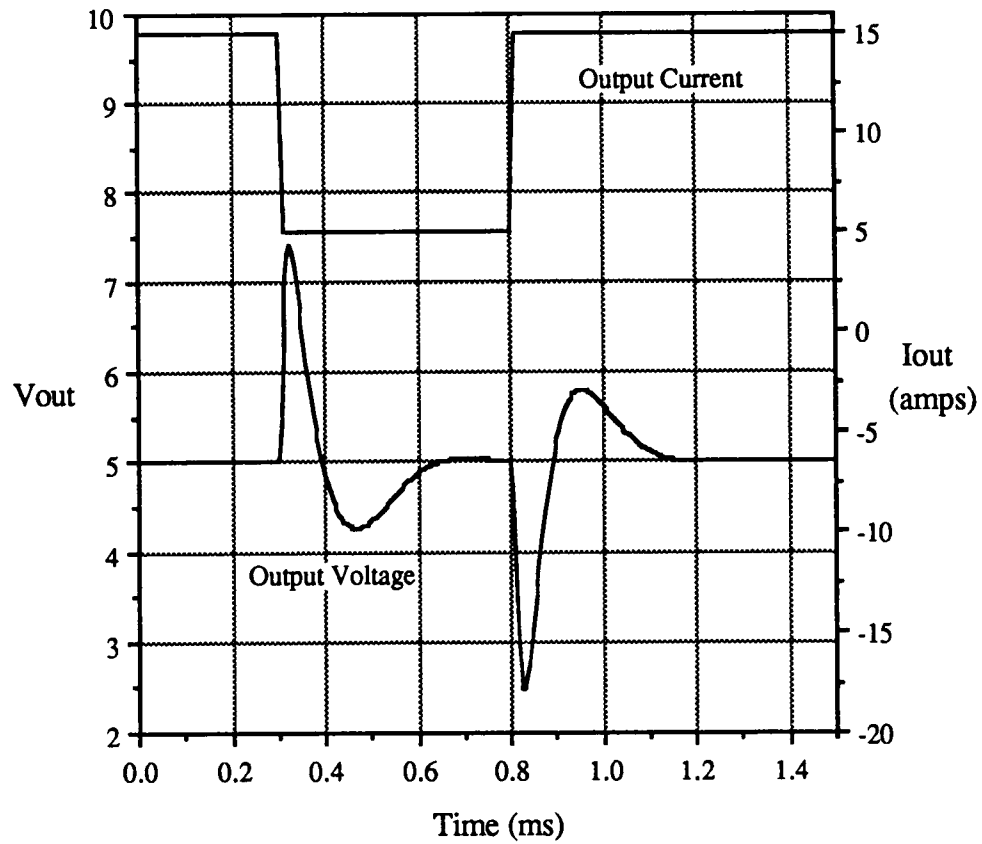


Figure 5-5. Five volt output transient load current response computer simulation. 15 amps to 5 amps.

and Ccoup to extremely low values and applying a transient load current to the output of the circuit, the power supply transient response can also be calculated with SPICE 2. The following pages include the results of simulations of each of these parameters. The source listing for the SPICE 2 input file used here is included in Appendix B.

Magnetic Amplifier

The magnetic amplifier post-regulator circuit used in this project is a nonlinear system similar to that of the pulse width modulation control circuit discussed above. The small signal model for this type of controller was formalized by R. D. Middlebrook in 1973 [17]. The model is a linearization of the non-linear process described in chapters II and IV. Central to the model is the relationship between the reset current to the saturable reactors and the output voltage as illustrated in Figure 4-10. Note that for the 40-turn case, a large portion of the curve very closely approximates a straight line. This indicates a fairly linear relationship between reset current and output voltage, particularly in the vicinity of the 15V output level of interest here. Assuming that the current of the two transistor current source of U1 in Figure 4-8 is a linear function of the error amplifier output voltage, the following expression for the loop transmission can be written:

$$T(s) = -A_{err}(s)A_{cs}A_{sr}H_e(s), \quad (5-10)$$

where

A_{err}	=	error amplifier transfer function,
A_{cs}	=	v/i transfer function of current source,
A_{sr}	=	i/v relationship for the saturable reactors from Figure 4-10, and
$H_e(s)$	=	transfer function of the output LC filter.

The output filter response, $H_e(s)$, is identical in form to that of the +5V control loop discussed previously. The Q of the output filter was dampened with R1 and C3 of Figure 4-8 in the same manner as for the 5V system. The center frequency of the LC double pole is calculated as 2.9kHz. Recall that the error amplifier small signal transfer function is

$$A(s) = \frac{-(1 + sR_{12}C_6)(1 + s[R_{13} + R_{14}]C_4)}{(s[C_5 + C_6]R_{13})(1 + sR_{12}C_5C_6/[C_5 + C_6])(1 + sR_{14}C_4)}, \quad (5-11)$$

with the following frequency domain poles and zeros:

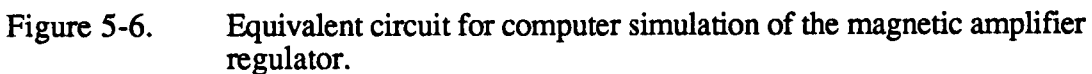
$$\begin{aligned} f_p &= 0, 11.3, \text{ and } 23 \text{ kHz;} \\ f_z &= 2.0, \text{ and } 3.2 \text{ kHz.} \end{aligned}$$

As before, two zeros have been added to cancel the output filter double pole. The additional poles serve to cancel the zero introduced by the output capacitor equivalent series resistance and roll the response off beyond the 0 dB loop crossing frequency. The pole at $s = 0$ maximizes DC accuracy and sets the single pole response from low frequency.

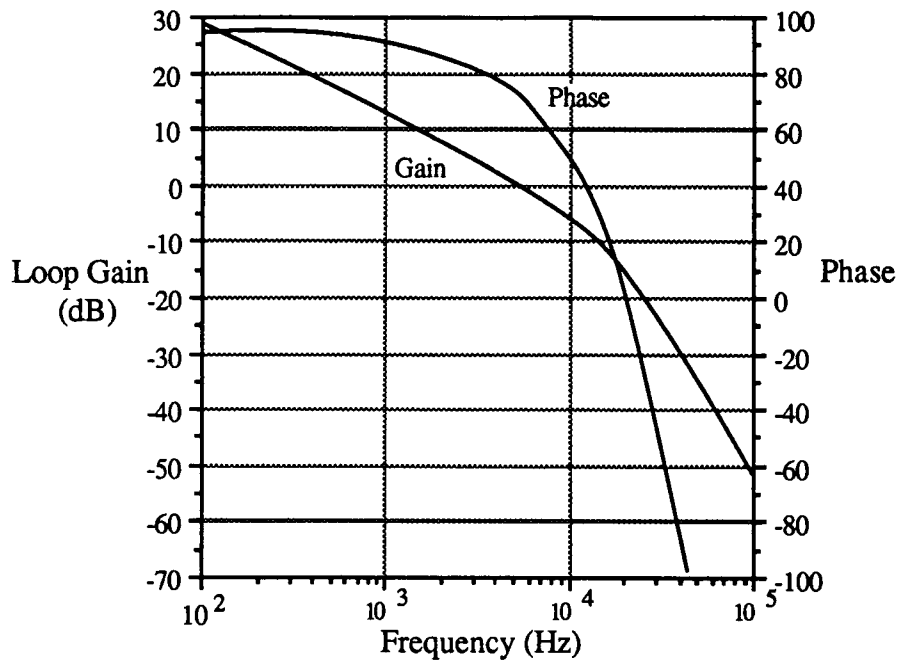
Due to the complexity of the control loop, this circuit was also evaluated with the SPICE 2 computer-aided design package. Reference [28] is an excellent discussion of magnetic amplifier modeling with SPICE 2 and was relied upon heavily in the analysis to follow. Figure 5-6 illustrates a simplified schematic of the equivalent circuit used to simulate the magnetic amplifier. A_{cs} from Equation (5-10) is set by the two transistor current source and has a value of approximately -40 ma/volt. Also from Equation (5-9) is the slope of the V-I characteristic for the saturable reactors found from the slope of the curve in Figure 4-10. For this circuit, the slope has a value of -3100 volts/amp and is controlled by the current controlled voltage source, Vfb.

The time delay is a characteristic of the saturable cores related to the average hold-off time. The value of the delay in this case is $\approx 1.89\mu\text{sec}$. The delay at first was implemented with a transmission delay line element. However, due to the manner in which SPICE 2 handles delay lines, the transient response consumed an unusually high amount of computer time. To reduce computer time, the delay was implemented with a fourth order maximally flat time delay network.

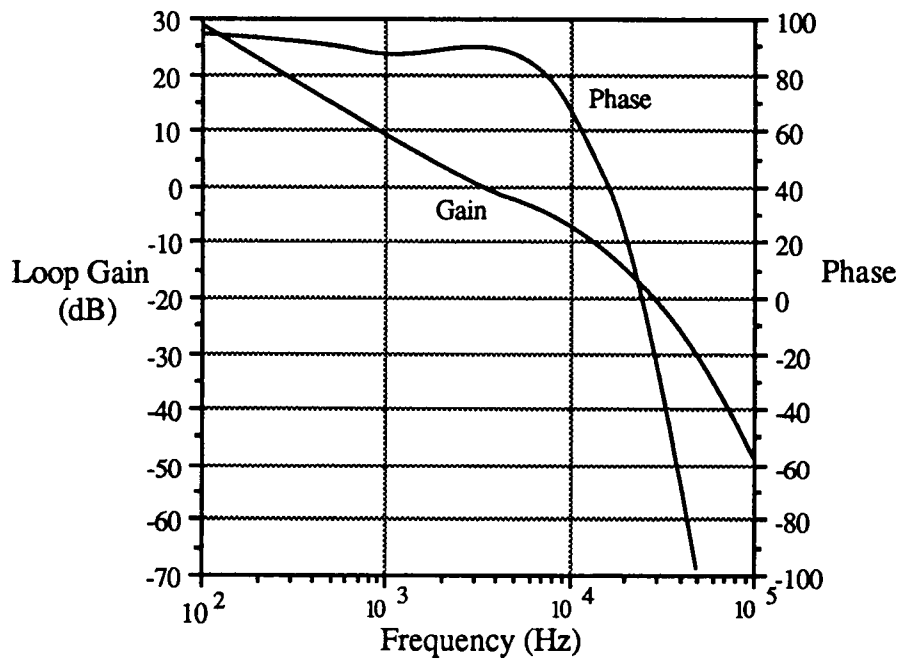
The signal, D, is used to control the dependent voltage source EFB. Notice that this source has the opposite polarity as that of E2. The dependent source E2 is the voltage



present with no reset current. EFB is the amount the output voltage is reduced by the duty cycle hold-off time, as controlled by the reset current. Figures 5-7 and 5-8 indicate the open-loop frequency response simulations and the output transient response respectively. Also verified was the short circuit limiting circuit. The complete simulation listing is included in Appendix B.



(a)



(b)

Figure 5-7. Magnetic amplifier open loop frequency response computer simulation for, (a) - output current of 1 amp, and (b) - output current of 15 amps.

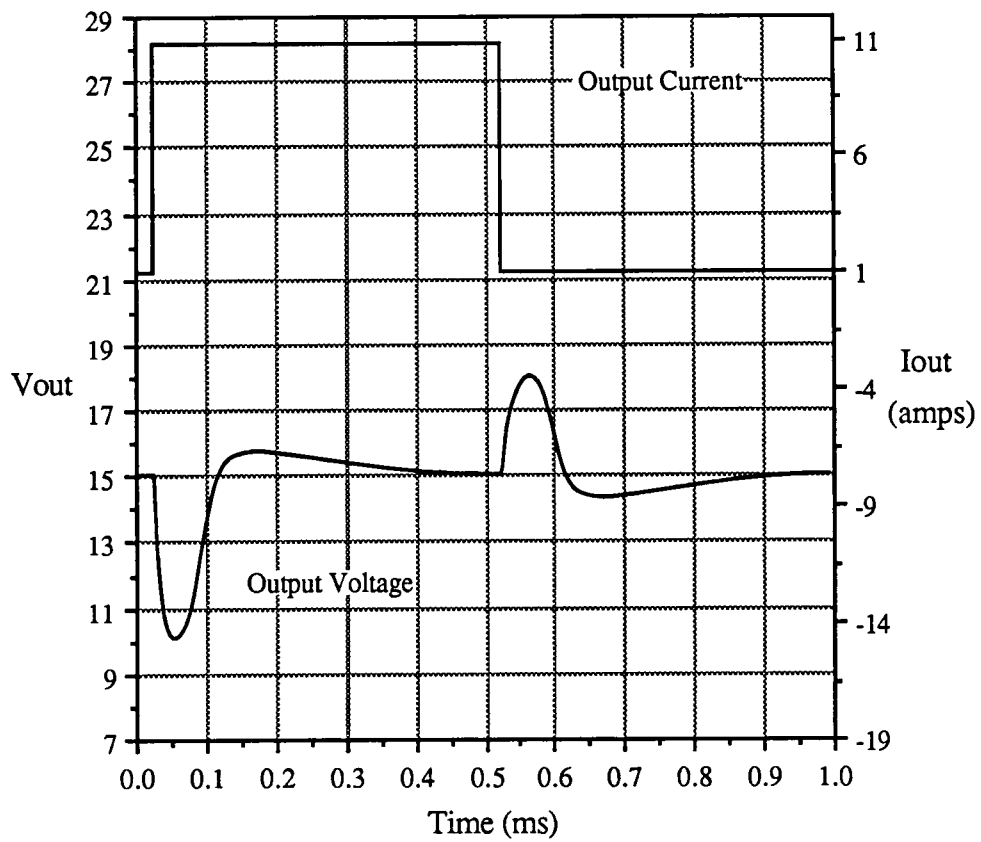


Figure 5-8. Magnetic amplifier transient response computer simulation.

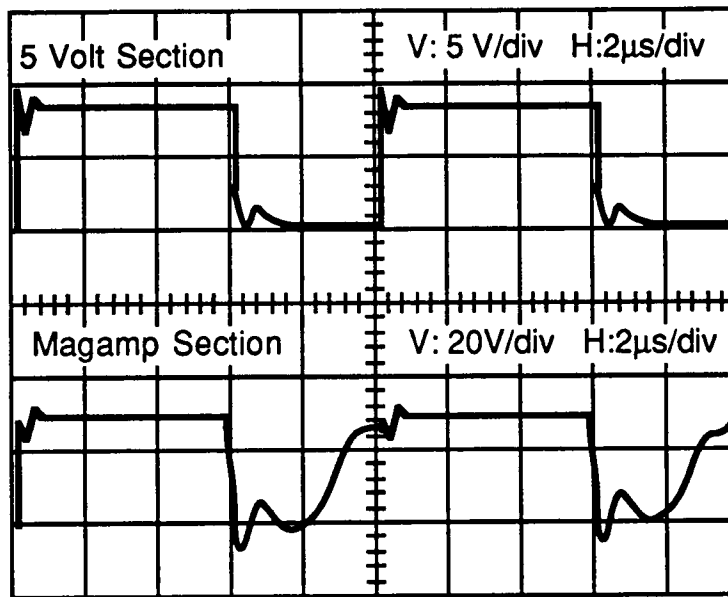
CHAPTER VI

EXPERIMENTAL RESULTS AND CONCLUSIONS

Output Interdependence

The prototype switching power supply was designed and built according to the discussions in the previous two chapters. The circuit exhibited performance very close to predicted values. One anomaly in the performance of the prototype is an interdependence between the various output sections. When the +5V output is delivering low current levels and the magamps deliver moderate to high current, the magamps fall out of regulation. Figure 6-1a shows the voltages at the nodes immediately following the diode rectifiers of the +5V output section and the -15V output section. The magnetic amplifiers are disabled so that there is no saturable reactor reset current in those sections. The +5V section delivers 6 amps to its load. Notice that the duty cycle is approximately 0.3 (referred to the primary). Figure 6-1b shows the voltages at the same nodes with different loads. The magnetic amplifiers are enabled and deliver an average of 7.5 amps. The +5V section still delivers 6 amps. The output voltages of the magamp sections drop to an average of 13V.

The top trace of Figure 6-1b now exhibits an 'extra' pulse of energy at the end of each desired pulse. The duty cycle at the magamp section (D) is now approximately 0.27, while the effective duty cycle (D_{eff}) at the 5V output is ≈ 0.31 . An analysis of this anomaly reveals that the 'extra' pulse is due to stored energy in the saturable reactors of the magnetic amplifier sections. At the end of each conduction cycle, the saturable reactors deliver their stored energy through the power transformer to the primary and the 5V output section. Since the power switches on the primary side are off at this time, all of the stored energy is delivered to the 5V section. Because of this additional energy, the pulse width control loop has to reduce the duty cycle to maintain regulation on the 5V output. To restate, the duty



(a)

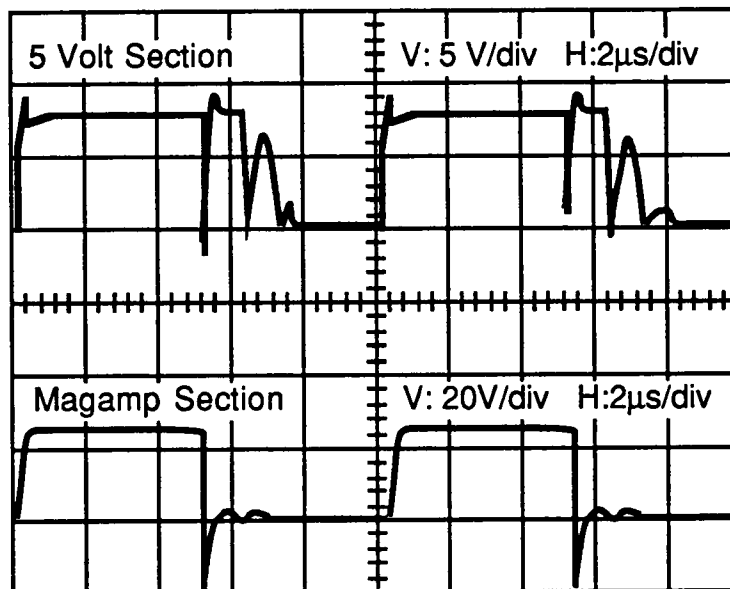


Figure 6-1. Waveforms illustrating output interdependence phenomena. (a) - Post-rectifier waveforms with magnetic amplifiers disabled and 5V output delivering 6 amps. (b) - Same waveforms with magnetic amplifiers delivering 7.5 amps.

cycle seen by the magamps is the duty cycle set by the PWM controller. However, the effective duty cycle at the 5V section is the set duty cycle plus the 'kickback' energy from the saturable reactors. If the 5V load current is increased sufficiently, the magamps remain in regulation since the PWM duty cycle increases to accomodate the additional 5V load. When the 5V load is ≥ 10 amps the ± 15 V sections remain in regulation at all current levels.

Although the anomaly described above results in a very efficient system, it is, however, undesirable due to the regulation limitations. Several approaches for correcting the problem were considered. These included clamping the reverse voltage across the saturable reactors, which resulted in a loss of regulation at low current levels since the reactors could not be sufficiently reset. Also attempted was the placement of an RC-diode snubber across the reactors. Both of these techniques reduced the 'kickback' energy, but interfered with operation of the magnetic amplifier. One of the most promising techniques was using a switching transistor to momentarily shunt the ± 15 V secondaries at the end of each incident pulse to keep the reactor kickback from entering the power transformer. Of course, all of these approaches add to the circuit complexity and decrease efficiency, negating two of the major advantages of the magnetic amplifier. None of the literature surveyed makes any mention of this or any related conditions.

Current Limit

The 5V output current limit of the prototype circuit did not function properly due to saturation of the sense transformer, T4, of Figure 4-2. Diode D30 was not in the original design. It originally was deemed unnecessary since diodes D15 and D16 would catch the flyback of the output filter inductor (this is a common practice in industrial designs). Without D30, the current sense transformer always sees a current equal to the output inductor current. This means that the transformer has to have a larger core to accomodate the higher average current. With D30 inserted, the core only has to sustain current when

D15 or D16 is conducting. Due to time constraints, this was not fully tested but should alleviate the problem of sense transformer core saturation.

Prototype Circuit Measurements

Output Regulation

The output DC levels were tested for accuracy at various output load conditions. These measurements are summarized in Table 6-1. Unless otherwise indicated, the $\pm 15\text{V}$ sections delivered 4.5 amps, and the +5V output delivered 10.0 amps. The $\pm 15\text{V}$ outputs are set with R16 of Figure 4-10. The 5V output is set by two 1% resistors, but could be adjusted by substituting a potentiometer for R15 of Figure 4-6.

Table 6-1. Output regulation accuracy measurements.

+5V output		+15V output		-15V output	
I	V	I	V	I	V
2.5	5.088	0	15.046	0	15.054
7.5	5.085	1.0	15.044	1.0	15.053
15.0	5.082	2.5	15.043	2.5	15.051
20.0	5.080	5.0	15.041	5.0	15.050
25.0	5.077	7.5	15.039	7.5	15.047
		10.0	15.036*	10.0	15.045*
		11.5	15.035*	11.5	15.044*
@ 60° C	+0.31%		-0.15%		-0.14%
Output Ripple	≤ 100mv		≤ 120 mv		≤ 120 mv

*+5V at 15.0 amps

The magnetic amplifier current limit circuit functioned properly and limited the output current at +15.7 and -15.6 amps. This setpoint can be adjusted as high as 18 amps with R11 of Figure 4-10, if desired.

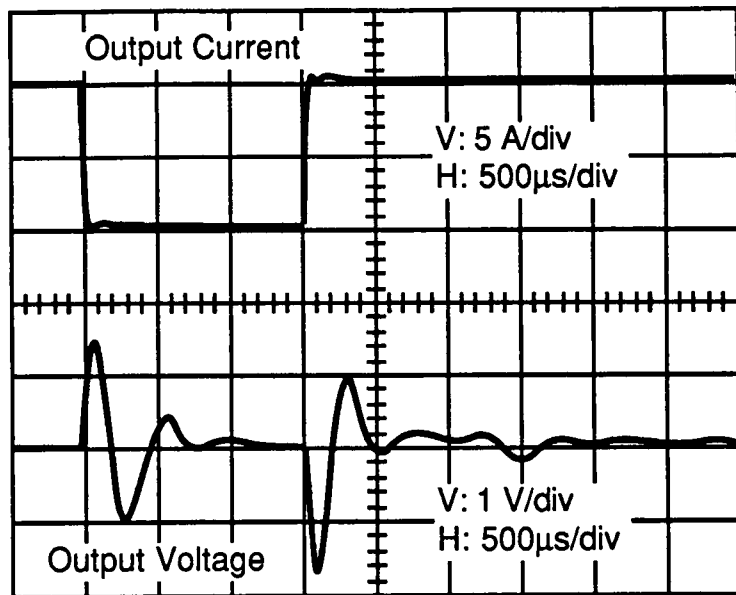
Output Transient Response

Figure 6-2 shows the measured transient response of the prototype circuit at room temperature. The settling time is about twice that predicted by the SPICE 2 models of chapter V. This is not unexpected, primarily due to the assumption of small perturbation signals on which the SPICE 2 models are based. 10 amp load transients certainly induce significant perturbations in the control signals, leading to inaccuracy of the original premise. The models are still useful as a predictor of stability and approximate transient response.

The transient response was also measured at 60° C, and showed no significant differences in settling times. However, at certain load conditions, the circuit exhibited a tendency to oscillate a slight amount. This is related to the interdependency of the outputs discussed previously. When the duty cycle changes, the magamp 'kickback' also changes, leading to an increase in the +5V output. This, in turn, causes the PWM to reduce the duty cycle, leading to another change in the 'kickback' energy. Under certain conditions, this process can lead to an oscillation as the various output sections 'hunt' for the proper output voltage, varying the output levels of the other sections in the process. If the bandwidths of the three output sections were not so similar, the oscillation would probably not occur since the faster of the outputs could always track the other outputs. If the reactor 'kickback' problem is alleviated, this slight oscillation tendency should also be removed.

Power Supply Efficiency

The supply efficiency was measured at various load levels and is illustrated in Figure 6-3. The input power was measured directly across the line input with a moving coil wattmeter. The output power was directly measured with DC voltage and current meters. The efficiency was quite high and showed no degradation after irradiation.



(a)

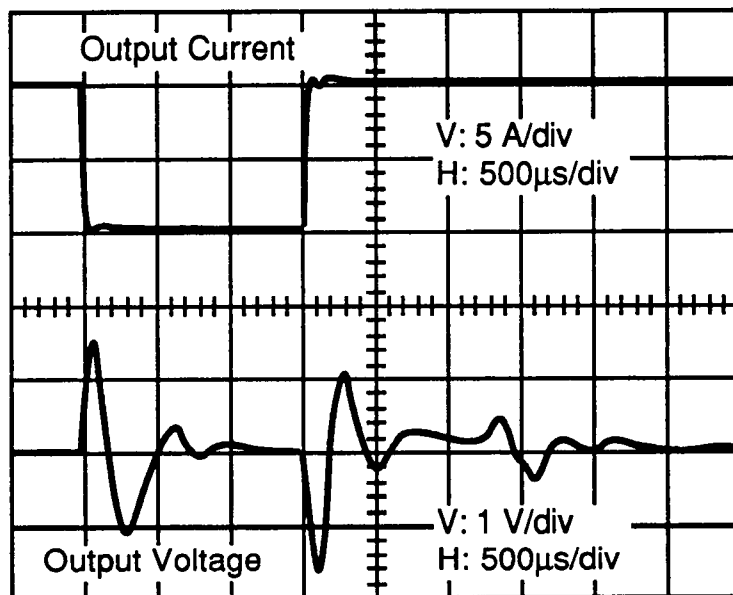


Figure 6-2. Measured transient response for, (a), the 5V output section, and (b), the 15V output sections.

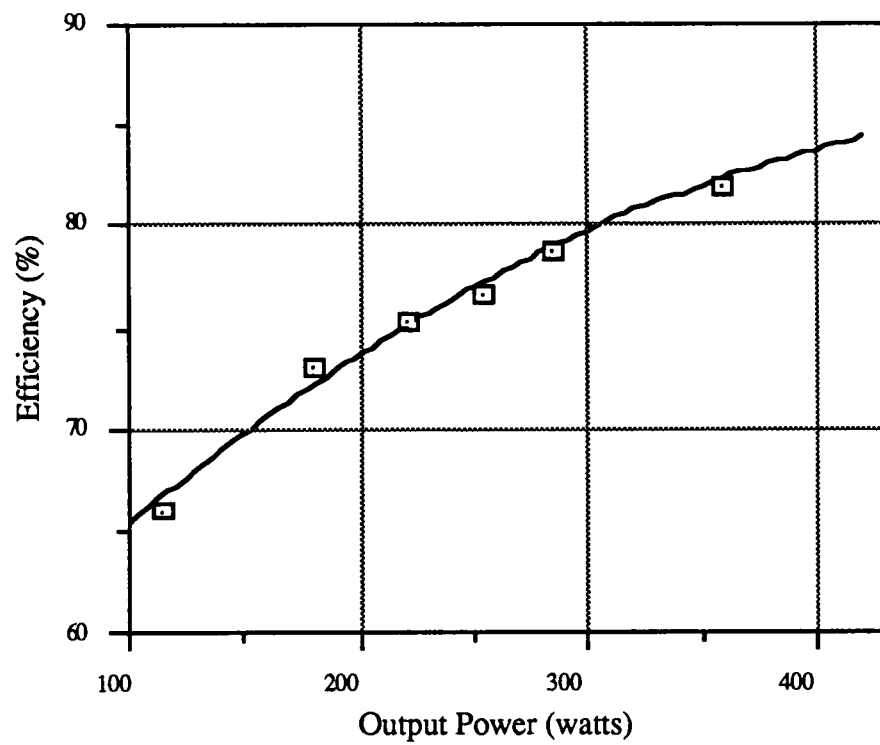


Figure 6-3. Power supply efficiency vs. output power.

Irradiation

The circuit was irradiated in the storage pool of the Oak Ridge National Laboratory High Flux Isotope Experimental Reactor. The irradiation took place over a two week period and exposed the center of the prototype circuit to a total gamma dose of over 12 Mrad. The operating temperature of the circuit was 60°C for the entire irradiation cycle. The supply delivered approximately 300 watts to a static load during the duration of the test. As illustrated in figure 6-4, the +5V output drifted less than 0.7%, and the $\pm 15V$ outputs drifted less than 1.9%. The transient response of the circuit suffered only slight degradation. The primary factor producing the decrease of the $\pm 15V$ outputs was the degradation of the input error amplifier (pins 6-8) for U1 (Figure 4-8). The offset voltage changed from 1mV to 10mV, while the input base currents for the comparator increased from <50nA to $\approx 10\mu A$. These effects resulted in $\approx 0.2V$ decreases in the 15V outputs. For better regulation, one would desire a radiation hardened error amplifier, such as the OP42 device used in the 5V control circuit (Figure 4-6).

Conclusions and Suggestions for Further Study

The power supply was designed, built and tested. With the exception of the 5V current limit and the output section interdependency described previously, the prototype circuit performed as expected. It maintained very accurate regulation during a two week irradiation in an ambient temperature environment of 60°C. The prototype circuit sustained 25% more gamma irradiation than the original requirement of 10 megarad.

There are two particular areas which merit further investigation. The first of these is the output interdependency described in previous sections. This anomaly is primarily a result of having evenly distributed power output across all three output sections. In most applications, one output delivers the bulk of the total power. Because of this, the

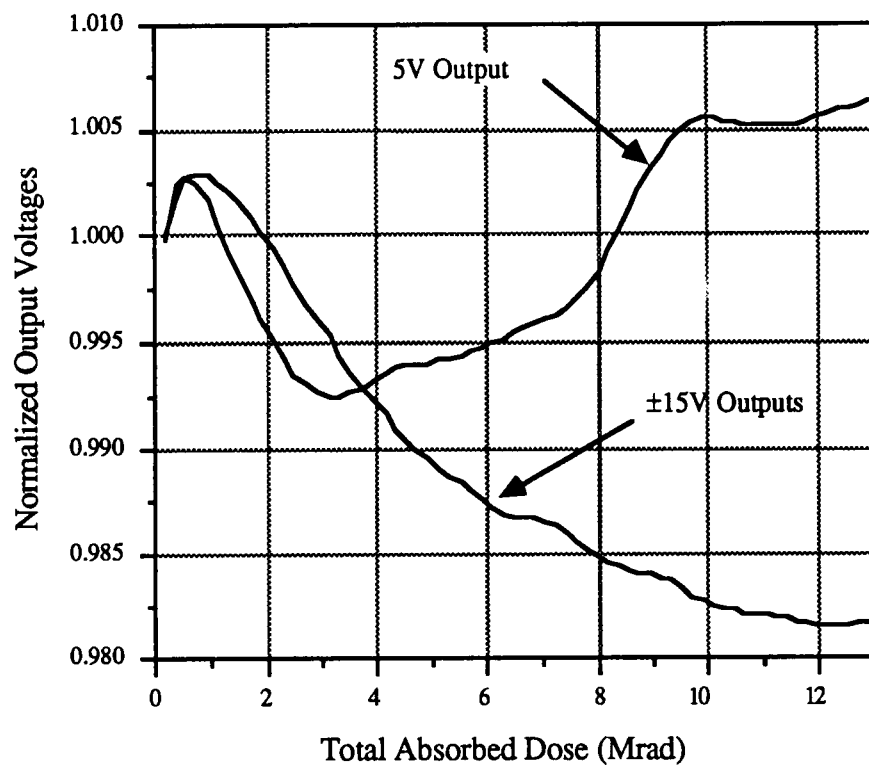


Figure 6-3. Power supply normalized voltage drift vs. absorbed dose.

remaining sections have very little effect on overall regulation. The 'kickback' of energy by saturable reactors in the magamp sections needs to be further investigated and modeled. With an accurate model of the process, it should be possible to design a circuit to circumvent the problem. However, as long as the 5V output current does not fall below the magamp section currents, excellent regulation is maintained.

An area of interest not mentioned previously is the modeling of the proportional base drive circuit. Early in the design process, an attempt was made to model the base drive circuit with the SPICE 2 analysis program. Because there are three mutual inductors in the circuit, there were convergence problems due to the manner in which SPICE 2 handles mutual inductors. Without using mutual inductors, the circuit is difficult to model since the secondary of the base drive transformer is delivering primarily a voltage signal at the start of a cycle, and a current signal (from the collector winding) once the transistor begins to conduct. The shorting of the primary terminals to end a cycle also gives rise to modeling problems. Investigations which resulted in creation of reliable models for this class of circuits would certainly improve the existing design techniques.

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APPENDICES

APPENDIX A

PROTOTYPE CIRCUIT PARTS LIST

Switching Power Supply Main Drawing

<u>Item</u>	<u>Description</u>	<u>Manufacturer</u>
C1, C2	Capacitor; each consisting of three-470 μ F, 250 VDC, hi-reliability, high-temperature (105°C) electrolytic capacitors in parallel. Type LPK 2E471 MHSC	Nichicon, Inc.
C3, C4	Capacitor, electrolytic, 1000 μ F, 25VDC, high temperature (105°C)	Panasonic, Inc.
C5, C6 C16,C17	Capacitor, ceramic, 0.1 μ F, $\pm 10\%$, 50 VDC. Type X7R formulation	USCC, Sprague, or equivalent
C7	Capacitor, metallized polycarbonate, 10 μ F, $\pm 10\%$, 5MC 29 B106 K	Elcon Sales Clifton, NJ
C8	Capacitor, metallized polycarbonate, 20 μ F, $\pm 10\%$, 50 VDC, copper outside shield. Type 5MC29B206K	Elcon Sales
C9	Capacitor, electrolytic, 330 μ F, 10 VDC, high reliability, 105°C, type UPX1A331MPH	Nichicon, Inc
C10	Capacitor, polypropylene, 2 μ F, $\pm 10\%$, 400 VDC. Type EC5MP12J205K	Elcon Sales
C11	Capacitor, ceramic, 820 pF, $\pm 10\%$, 1000 VDC, type X5F formulation	Sprague, Inc.
C12	Capacitor, ceramic, 200 pF, $\pm 10\%$ 50 VDC, type NPO (COG) formulation	Sprague, Inc.
C13, C14, C15	Interference capacitor, 0.1 μ F, $\pm 10\%$, 250 VAC, Type ECQ-EW	Panasonic, Inc.
D1-D6	Diode, rectifier, D1-D4 is a type BR66-ND bridge (6A, 600V). D5, D6 are BR66-ND using two diodes in bridge	Diodes, Inc.

<u>Item</u>	<u>Description</u>	<u>Manufacturer</u>
D7, D8, D11, D12, D17,D18, D21	Diode, rectifier, 1A-50V, ultra-fast recovery. Type MUR105	Motorola, Inc.
D9, D10 D13, D14	Diode, rectifier, 8A-1000V, ultra-fast recovery. Type MUR8100	Motorola, Inc.
D15, D16	Diode, Schottky rectifier, dual, 30A-45V. Type MBR3045PT	Motorola, Inc.
D19, D20 D22-D25 D26-D29	Diode, rectifier, fast recovery, 1A-400V. Type 1N4936	Motorola, Inc.
L1	Inductor, 26 μ H at 30A(max). Type HL-8129	Hurricane Electronics Hurricane, Utah
Line Filter	EMI filter, 3 phase, 220-250 VAC, 50-60 Hz, 15A/phase. Type 3E15DF	Filter Concepts, Inc., Santa Ana, CA
M1, M2, M3	Metal-oxide Varistor (MOV), 230 VAC, 6500A surge, type ZNR20K361	Panasonic, Inc.
Q1, Q2,	Transistor, npn, power, type 2N6925	General Semiconductor Industries
Q3, Q4	Transistor, npn, medium power, type D40E5	National Semiconductor, or General Electric
R1, R2	Resistor, 51 k Ω , $\pm 5\%$, 2W, carbon composition	Allen-Bradley or equivalent
R3, R5	Resistor, 100 Ω , 1/4W, $\pm 5\%$, carbon composition	Allen-Bradley
R4, R6	Resistor, 2.7 Ω , $\pm 5\%$, 1W, carbon composition	Allen-Bradley
R7	Resistor, power, constructed from two-39 Ω , $\pm 5\%$, 10 watt, metal-or carbon-film resistors (non-inductive design)	Sprague, or Caddock
R8	Resistor, 0.33 Ω , $\pm 5\%$, 2W, metal-oxide film	TRW, Inc.
R9	Resistor, 6.8 Ω , $\pm 5\%$, 1W, carbon composition	Allen Bradley

<u>Item</u>	<u>Description</u>	<u>Manufacturer</u>
R10, R11	Resistor, 120 Ω , $\pm 5\%$, 2W carbon composition	Allen Bradley
R12, R13	Resistor, 100 Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R14	Resistor, composed of two-parallel 50 Ω , $\pm 5\%$, 2W, carbon composition	Allen-Bradley
RT1, RT1	Current limiter, thermistor, 7-ohm at 25°C. Type CL-50	Keystone, Inc.
T1, T2	Transformer, base-drive pulse, type PE97003	Pulse Engineering, Inc.
T3	Transformer, power, special construction. Type J8806-A, 9068732	Coilcraft, Inc.
T4	Transformer, current-sense, 1/100 turns ratio. Type HH8141	Hurricane Electronics
T5	Transformer, 115V/230V primary, 28V C.T. secondary, 12 VA. Type DST 5-28	Signal Transformer, Inc.

Primary Side Pulse Width Modulation Control Circuit

C1	Capacitor, ceramic, 270 pF, $\pm 5\%$, 50V, NPO(COG) formulation	USCC, or Sprague
C2, C3	Capacitor, ceramic, 1000 pF, $\pm 5\%$, 50V, NPO(COG) formulation	USCC, or Sprague
C4	Capacitor, ceramic, 0.015 μ F, $\pm 5\%$, 50V, type X7R formulation	USCC, or Sprague
C5	Capacitor, ceramic, 1500 pF, $\pm 5\%$, 50V, type X7R formulation	USCC, or Sprague
C6, C8, C10-C18, C22, C25, C26	Capacitor, ceramic, 0.1 μ F, $\pm 5\%$, 50V, type X7R formulation	USCC, or Sprague
C7	Capacitor, tantalum, 68 μ F, $\pm 10\%$, 6V	Kemet, Inc.
C9	Capacitor, tantalum, 15 μ F, $\pm 10\%$, 25V	Kemet, Inc.

<u>Item</u>	<u>Description</u>	<u>Manufacturer</u>
C19	Capacitor, ceramic, 330 pF, $\pm 5\%$, 50V type NPO(COG) formulation	USCC, or Sprague
C20	Capacitor, ceramic, 100 pF, $\pm 5\%$, 50V type NPO(COG) formulation	USCC, or
C21	Capacitor, ceramic, 0.082 μ F, $\pm 10\%$, 50V. Type X7R formulation	USCC, or Sprague
C23, C24	Capacitor, ceramic, 0.047 μ F, $\pm 10\%$, 50V. Type X7R formulation	USCC, or Sprague
Q1	Transistor, NPN, type 2N3904	Motorola, or National Semiconductor
Q2	Transistor, NPN, medium power, type D40E5	National Semiconductor, or General Electric
R1	Resistor, 7.5 k Ω , $\pm 1\%$, 1/4W, metal-film. Type RN55C	Mepco/Electra
R2	Resistor, 22.1 k Ω , $\pm 1\%$, 1/4W, metal-film. Type RN55C	Mepco/Electra
R3	Resistor, 510 Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R4	Resistor, 820 Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R5, R6, R7	Resistor, 10 k Ω , $\pm 1\%$, 1/4W, metal-film. Type RN55C	Mepco/Electra
R8, R19	Resistor, 1 k Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R9, R15, R16, R23, R24	Resistor, 2 k Ω , $\pm 1\%$, 1/4W, metal-film. Type RN55C	Mepco/Electra
R10	Resistor, 15 k Ω , $\pm 1\%$, 1/4W, metal-film. Type RN55C	Mepco/Electra
R11	Resistor, 392 Ω , $\pm 1\%$, 1/4W, metal-film. Type RN55C	Mepco/Electra
R12	Resistor, 27 k Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley

<u>Item</u>	<u>Description</u>	<u>Manufacturer</u>
R13	Resistor, 51 Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R14	Resistor, 240 Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R17, R18	Resistor, 470, $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R20	Resistor, potentiometer, 2 k Ω , $\pm 10\%$, 15-turn, Cermet, 3/4 watt	Beckman
R21	Resistor, 82 Ω , $\pm 5\%$, 1W, carbon composition	Allen-Bradley
R22	Resistor, 2.4 k Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R25, R26	Resistor, 390 Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R27, R29	Resistor, 1.1 k Ω , $\pm 1\%$, 1/4W, metal-film. Type RN55C	Mepco/Electra
R28	Resistor, 261 Ω , $\pm 1\%$, 1/4W, metal-film. Type RN55C	Mepco/Electra
R30	Resistor, 6.8 k Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
U1, U7	IC, op amp, type OP42EJ	Precision Monolithics
U2	IC, D-type Flip Flop, type 74LS74AN	National Semiconductor
U3	IC, Dual monostable-multivibrator, type 74LS123AN	National Semiconductor
U4	IC, Dual 4-input NAND, open-collector output. Type 74LS22AN	National Semiconductor
U5, U6	IC, comparator, type CMP05FZ	Precision Monolithics
U8	IC, over-and under-voltage comparator, type SG3543N	Silicon General
VREF1, VREF2	IC, precision adjustable Zener, voltage regulator. Type TL431I	Texas Instr. (No substitution)

<u>Item</u>	<u>Description</u>	<u>Manufacturer</u>
-------------	--------------------	---------------------

Magnetic Amplifier Controller, $\pm 15\text{V}$ Output

Item	Description	Manufacturer
C1	Capacitor, metallized polycarbonate, 20 μF , $\pm 10\%$, 50V, copper outside shield. Type 5MC29B206K	Elcon Sales
C2	Capacitor, metallized polycarbonate, 10 μF , $\pm 10\%$, 50V, copper outside shield. Type 5MC29B106K	Elcon Sales
C3	Capacitor, electrolytic, 470 μF , 25VDC, high reliability, 105°C, type UPXIE471MRH	Nichicon
C4	Capacitor, 3300 pF, $\pm 10\%$, ceramic, 50V, type X7R formulation	USCC, or Sprague
C5	Capacitor, 1500 pF, $\pm 5\%$, ceramic, 50V, type NPO(COG) formulation	USCC, or Sprague
C6	Capacitor, 0.015 μF , $\pm 10\%$, 50V, ceramic, type X7R formulation	USCC, or Sprague
C7	Capacitor, 15 μF , $\pm 10\%$, 25V, tantalum	Kemet Inc.
C8	Capacitor, 33 μF , $\pm 10\%$, 35V tantalum	Kemet, Inc.
C9, C11, C12	Capacitor, ceramic, 0.047 μF , $\pm 10\%$, 50V, type X7R formulation	USCC, or Sprague
C10, C13	Capacitor, ceramic, 0.1 μF , $\pm 10\%$, 50V, type X7R formulation	USCC, or Sprague
D1, D2, D3, D4, D8, D9	Diode, small signal, type IN4148	Motorola
D5, D6, D7	Diode, Schottky rectifier, 10A-100V, type MBR10100	Motorola
D10	Diode, rectifier, type MUR105	Motorola
L1	Inductor, 40 turns (#22) on Magnetics type XF-41605-TC toroidal core	Magnetics
L2	Power inductor, 100 μH , 15A max, Type HL-8114	Hurricane Electronics

<u>Item</u>	<u>Description</u>	<u>Manufacturer</u>
Q1	Transistor, npn, type 2N3904	Motorola, or National
R1	Resistor, 0.33 Ω , $\pm 5\%$, 2W, metal film	TRW, Inc.
R2	Resistor, composed of two-parallel 300 Ω , $\pm 5\%$, 2W, carbon composition	Allen-Bradley
R3, R4, R6, R7	Resistor, 100 Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R8	Resistor, 200 Ω , $\pm 5\%$, 1/2W, carbon composition	Allen-Bradley
R9	Resistor, 150 k Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R10	Resistor, 3 k Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R11	Resistor, potentiometer, 2 k Ω , $\pm 10\%$, 16 Turn, 3/4W, cermet, type 66WR2K	Beckman
R12	Resistor, 5.11 k Ω , $\pm 1\%$, 1/4W metal-film. Type RN55C	Mepco/Electra
R13	Resistor, 11 k Ω , $\pm 1\%$, 1/4W metal-film. Type RN55C	Mepco/Electra
R14	Resistor, 4.32 k Ω , $\pm 1\%$, 1/4W metal-film. Type RN55C	Mepco/Electra
R15	Resistor, 2 k Ω , $\pm 1\%$, 1/4W metal-film. Type RN55C	Mepco/Electra
R16	Resistor, potentiometer, 500 $\pm(\pm 10\%)$, 16 turn, cermet. Type 66WR500	Beckman
R17	Resistor, 1.8 k Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R18	Resistor, 13 k Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R19, R20	Resistor, 100 k Ω , $\pm 5\%$, 1/4W, carbon composition	Allen-Bradley
R21	Resistor, 750 Ω , $\pm 5\%$, 1/2W, carbon composition	Allen-Bradley
R22	Resistor, 6.19 k Ω , $\pm 1\%$, 1/4W metal-film. Type RN55C	Mepco/Electra

<u>Item</u>	<u>Description</u>	<u>Manufacturer</u>
R23	Resistor, 121 Ω , $\pm 1\%$, 1/4W metal-film. Type RN55C	Mepco/Electra
R24	Resistor, 1.21 k Ω , $\pm 1\%$, 1/4W metal-film. Type RN55C	Mepco/Electra
R25	Resistor, 680 Ω , $\pm 5\%$, 1W, carbon composition	Allen-Bradley
RSC	Resistor, 0.01 Ω , $\pm 5\%$, 5W metal element film. Type L05	RCL Shallcross Manchester, NH
SR1, SR2	Saturable reactor, 40 turns (#18) on Magnetics 50B10-1E amorphous core; or, (lower loss) 35 Turns (#16) on Toshiba MB21X14X4.5 amorphous core	Magnetics, Inc. or Toshiba
U1	IC, magnetic amplifier controller. Type UC3838N	Unitrode Corp.
U2	IC, over-and under-voltage comparator. Type SG3543N	Silicon General
VR1	IC, precision adjustable Zener, voltage regulator. Type TL431I	Texas Instr. (No substitution)

Miscellaneous

Printed Circuits	1/16" thick, copper-clad, double-sided, 4oz copper epoxy-fiberglass dielectric. FR-4 Nema grade	Precision Laminates Danboro, Mass.
Magnetic Wire	Either polythermaleze coating (200°C), or polyester-imide-nylon (180°C) coating.	MWS Wire Industries
Hookup Wire	PVC insulation, 105°C	Alpha Industries
Power Connectors	Polycarbonate insulation, silver plated copper contacts, 30A and 60A rating. Anderson Powerpole Connectors	Anderson Power Products Boston, MA
Heat Sink insulation for power transistors	Sil-pad 1000	Bergguist Minneapolis, MN

APPENDIX B

SPICE 2 CIRCUIT SIMULATION LISTINGS

Pulse Width Modulation Controller SPICE Model Listing

```
* Switching Power Supply AC Open Loop, Io = 20A
*
* Analysis
*
.AC DEC 15 10 100K
*.PLOT AC VDB(20) VP(20)
.PRINT AC VDB(20) VP(20)
*
* Options
*
.WIDTH OUT=80
.OPTIONS LIMPTS=1000 ITL5=50000
*
VS 2 0 150V
VG 1 2 0
*
* Power Transformer
X1 1 0 3 0 9 0 12 0 23 TFMR
*
* Node 23 is duty cycle control voltage
*
* + 5V output
*
D1 3 4 MBR3045PT
RL1 4 5 0.001
L1 6 5 POLY 26UH 320NH
* Nonlinear inductor 26UH @ 0amps, 18UH @ 25amps
C1 6 7 30UF
RC1 7 0 0.005
CDAMP1 6 8 330UF
RDAMP1 8 0 0.35
*
RLOAD 6 0 0.25
*
* + 15V output
*
RL2 9 0 1K
*
* - 15v output
*
RL3 12 0 1K
* Compensation Amplifier
*
RAIN1 6 13 2K
RAIN2 13 0 2K
*
```

```

RA1 13 14 2K
RA2 14 15 15K
CA2 14 15 1500PF
RA3 15 16 3.9K
CA3 16 17 0.015UF
VCC 18 0 15V
VEE 19 0 -15V
XAMP1 15 24 19 17 18 OP42
VREF 24 0 2.5V
RAL 17 0 20K
* Filter at input to comparator
RO1 17 20 50
CO1 20 0 0.082UF
*
* L for AC Analysis
LCOUP 20 22 10
*
CCOUP 21 22 10
VC 21 0 AC
*
X2 22 23 PWM
*
*
*
*
* PWM SUBCIRCUIT
*
* VIN 0-1.25 VOLTS --- D = 0 - 48% (0 - .48 VOLTS[SEE XFORMER MODEL])
*
* D IS LIMITED BETWEEN 0 AND 48%
*
.SUBCKT PWM 1 2
*
R1 1 3 10K
VOFF 3 0 0V
EGAIN 4 0 1 0 40
*  $D_{max}/(V_{max}-V_{min}) = 0.5/(1.25-0.0)$ 
* X 100 To improve limiting accuracy
RLIM 4 5 5K
DPLIM 5 6 DSIMP
VPLIM 6 0 47.3V
DNLIM 7 5 DSIMP
VNLIM 7 0 0.7V
.MODEL DSIMP D
*
* Output
EBUFA 2 0 5 0 0.01
ROUT 2 0 10K
*
.ENDS PWM
*
*
*
* Three output switching supply transformer model
* for ac and transient analysis of control loop.
*
* Turns ratio = 1:N1*D*2:N2*D*2:N3*D*2

```

```

*
* N1 = 1/18  N2 = 3.5/18  N3 = 3.5/18  D = V(9,0)
*
.SUBCKT TFMR 1 2 3 4 5 6 7 8 9
*
RD 9 0 10K
RP 1 10 0.1893
RS1 11 3 0.00053
RS2 12 5 0.0030
RS3 13 7 0.0032
*
G1 10 2 POLY(2) 11 3 9 0 0 0 0 0 209.64
*      N1*2/RS1=1/18*2/.00053
G2 10 2 POLY(2) 12 5 9 0 0 0 0 0 129.63
*      N2*2/RS2=3.5/18*2/.003
G3 10 2 POLY(2) 13 7 9 0 0 0 0 0 121.53
*      N3*2/RS3=3.5/18*2/.0032
E1 11 4 POLY(2) 10 2 9 0 0 0 0 0 0.1111
*      N1*2=1/18*2
E2 12 6 POLY(2) 10 2 9 0 0 0 0 0 0.3889
*      N2*2=3.5/18*2
E3 13 8 POLY(2) 10 2 9 0 0 0 0 0 0.3889
*      N3*2=3.5/18*2
*
.ENDS TFMR
*
*
.MODEL MBR3045PT D(IS=0.66UA RS=0.01 N=0.9234 TT=1NS CJO=2.7NF VJ=0.5
+ M=0.5 EG=0.69 XTI=2 BV=48 IBV=10MA)
* A dual Schottky diode, with 45V BD, 30A Imax.
*
.SUBCKT OP42      2      3      4      6      7
*      -In  +In  -Vee  Out  +Vcc
*Device Char:  Aol>2E5; CMRR>85db; psrr(+)=110db, (-)>95db; zin=1e12//6pf
* ccm =2pf(ea) ;Zout=50; Vincm=+12.5v,-12v;Ib<200pa;Ios<40pa
* Vos<1mv ;Vout(max)=+12.5v,-12v;Isc=+28ma,-24ma;GB=10Mhz,SR=+55V/us,
*-57V/us;Noise=12nv/rthz(midband) and 150nv/rthz at 2 hz(fb=26 hz, with
1/f
* squared spectra)
* .Total nodes=29.
*
ECMRR 5 3 POLY(2) 1 0 23 0 0 25U 25U
EPSRR 9 5 POLY(2) 7 0 4 0 593.75UV -8.33333U 31.25U
VOS 2 8 1MV
CMI 8 0 2PF
CMN 9 0 2PF
CI 8 9 6PF
IBI 8 0 220PA
IBN 9 0 180PA
RN1 8 11 4.33K
RN2 9 10 4.33K
RN3 11 1 2.94MEG
RN4 10 23 2.94MEG
CN1 11 1 54NF
CN2 10 23 54NF
RI 1 23 1E12

```

```

R1I 8 12 1K
D1I 12 13 D3
VP 7 13 3
R1N 9 21 1K
D1N 21 13 D3
R2N 9 22 1K
D2N 20 22 D3
VN 20 4 3.5
R2I 8 24 1K
D2I 20 24 D3
G1 0 14 23 1 62.89MMHO
R 14 0 3.18MEG
R1 14 15 14.88
D3 14 29 D3
D4 29 14 D3
E1 29 0 15 0 1.0
C 15 0 1NF
E2 16 0 15 0 1.0
R2 16 17 691.3
C1 17 0 10PF
E3 18 0 17 0 1.0
R4 19 18 691.3
C2 19 0 10PF
G2 0 25 19 0 50MMHO
R8 25 0 20
D5 25 26 D5
D6 26 25 D6
E4 26 0 6 0 1.0
R7 25 6 30
D7 6 27 D3
D8 28 6 D3
V3 7 27 3.1
V4 28 4 3.6
IPS 7 4 4.96MA
RPS 7 4 228.6K
.MODEL D3 D(IS=1FA)
.MODEL D5 D(IS=0.22FA)
.MODEL D6 D(IS=20FA)
.ENDS OP42
*
*
.END

```

Magnetic Amplifier Controller SPICE Source Listing

```
MAG AMP OPEN-LOOP FREQ. RESP., USING UNIRRAD. UC3838 PWM --1A Load---
.OPTIONS ABSTOL=1UA VNTOL=1MV CHGTOL=1PC ITL1=500 ITL2=100 LIMPTS=5000
.NODESET V(10)=15.00 V(9)=15.00 V(8)=15.00 V(7)=15.025 V(19)=-.01
V(36)=0.00
+ V(41)=.00 V(37)=0.09 V(38)=0.18 V(43)=19 V(40)=2.501 V(15)=2.502014
+ V(18)=13.92 V(33)=13.97 V(43)=19 V(47)=20 V(20)=15.92 V(21)=-13.31
+ V(22)=-14.35 V(6)=31.144 V(24)=16.12 V(25)=32.24 V(26)=16.12
V(27)=16.12
+ V(31)=16.12 V(1)=29.2 V(2)=29.2 V(3)=29.2 V(4)=29.198 V(5)=28.757
+ V(35)=29.142 V(13)=15.00 V(16)=115.00
*
.AC DEC 10 1 100KHZ
.PRINT AC VDB(10) VP(10) VDB(33) VP(33) VDB(18) VDB(43) VP(43) VDB(19)
*
VIN 1 0 29.2
VG 2 1
LP 3 2 50NH
RP 3 4 2M
*- THE FOLLWING MODELS MBR10100 SCHOTTKY DIODE FOR AC ANALYSIS
RD1 4 35 0.0563
VD1 35 5 0.385
*
F1 5 0 VT3 1
E2 6 19 5 0 1.083
EFB 6 7 27 0 1
RS 7 8 25M
VT3 8 9
LS 9 10 POLY 100UH -2U IC=1
C1 10 11 30UF
R1 11 12 6MOHM
VT4 12 0
CBFC 10 29 470UF
RQ 29 0 0.5
RL 10 0 15
VTX 10 34
DZ2 0 34 D1N6276
RSC 19 0 0.01
RC1 36 0 100
RC2 37 19 100
RC4 41 36 100
RC5 38 37 100
CSC 36 37 0.05UF
RC6 38 40 3.36K
RSCHM 43 38 120K
VT6 42 43
X1 41 38 0 42 30 U3838A
X2 15 45 0 18 30 U3838A
X3 20 21 43 44 0 UC3838CS
LX 10 13 1000
CX 14 13 1000
```

```

VC 14 0 AC
*COMP. CKT. FOR ERROR AMP
R4 13 16 4.3K
C4 16 15 3.3NF
R3 15 0 2.2K
R2 13 15 11K
VREF 39 0 2.5
RREF 40 39 2.5
CCOMP 40 0 0.1UF
RCOMP 45 40 1.8K
R5 17 15 5.1K
C3 18 17 0.018UF
C2 18 15 1.5NF
RB1 33 18 200
CB1 33 0 0.01UF
*
VT2 44 33
VREV 0 28 15
VT1 23 28
D2 22 23 D914
R6 21 22 200
RE1 20 47 750
CQ 20 32 0.015UF
RE2 32 47 200
VT5 30 47
VCC 30 0 20
HC 0 24 VT1 -3100
R7 24 0 1K
* THE FOLLOWING MODELS THE MAG AMP DELAY OF (TYP) 1.89USEC USING A 4th
order
* MAX FLAT TD APPROX. FOR REDUCED CPU TRAN. TIME-see Weinberg--
EC 25 0 24 0 2
R8 25 26 100
DZ1 0 26 DZ1
LD1 26 31 20.866UH
CD1 31 0 6.0121NF
LD2 31 27 96.692UH
CD2 27 0 20.03NF
R9 27 0 100
*
.SUBCKT U3838A      2      3      4      6      7
*                  INV  NON-I  -VEE  OUT   +VCC
* This is the error amp and current-limit amp for the Unitrode UC3838
PWM
* IC chip. The model is a gnd. sensing quad E-F lateral pnp type input
with
* currents chosen for SR=0.3V/Usec, GB=0.8Mhz, PM=65deg.
Aol=1e6,Rout=80, Rin=
* 50Meg. Iout(max) values are +7ma and -4ma, with Vout(max) values of
Vcc-1.2V,
* Vee+0.1V. CMRR=100dB,PSRR>120dB. Vos=1mV. -UNIRRADIATED-Total nodes=16
*
CCM1 3 4 1.5PF
CCM2 2 4 1.5PF
CIN  3 2 1PF
Q1 4 3 1 P1
Q4 4 2 10 P4

```

```

Q2 8 1 5 P2
Q3 9 10 5 P2
CQ1 1 4 1.5PF
CQ2 10 4 1.5PF
R1 8 4 100K
R2 9 4 100K
C2 8 9 0.36PF
I1 7 1 3.25UA
I2 7 5 6.06UA
I3 7 10 2.84UA
GCM 0 11 5 0 1.161NMHO
G1 0 11 8 9 10UMHO
R3 11 0 100K
CFB 11 13 20PF
G3 13 0 11 0 861.42MMHO
RL 13 0 100K
* THE FOLLOWING DIODES ALLOW VOLTAGE LIMITING OF CFB FOR COMPARATOR
APPL.-
D2 13 16 D1
VADD 7 16 1.85
D4 12 13 D1
VX 4 12 -0.75
*
G2 0 14 13 0 1
RO1 14 0 1
RO2 14 6 80
RX 6 0 1MEG
D5 14 15 D5
D6 15 14 D6
E3 15 0 6 0 1
RPS 7 4 80K
IPS 7 4 2.3MA
.MODEL P2 PNP(IS=1FA BF=100 RB=150 TF=16NS TR=200NS XTB=1.5)
.MODEL P4 PNP(IS=1FA BF=40 RB=200 TF=20NS TR=200NS XTB=1.5)
.MODEL P1 PNP(IS=1.0995FA BF=40 RB=200 TF=20NS TR=200NS XTB=1.5)
.MODEL D1 D(IS=1FA)
.MODEL D5 D(IS=2.717PA)
.MODEL D6 D(IS=16.76NA)
.ENDS U3838A
*
.SUBCKT UC3838CS      1      2      3      4      5
*                   VM    COLL. OR1    OR2    SUB.
* This is the current source for resetting the magnetic amplifier PWM
chip.
* Iout max.=100ma. Current transfer= 100ma out for 1.1ma input, or
0.04A/V.
* Supply volts=40V max; VM-Vout=100V max. inputs are two diode OR
function
*
D1 7 3 D1
D2 7 4 D1
DSUB1 5 7 D1
DSUB2 5 6 D1
DZ1 7 1 DZ1
R1 7 1 5K
Q2 2 7 6 QP
R2 6 1 1K

```

Q1 2 6 8 QP AREA=10

R3 8 1 20

DZ2 2 1 DZ2

.MODEL D1 D(IS=1FA RS=30 TT=20NS CJO=3PF VJ=0.7 M=0.3 BV=80)

.MODEL DZ1 D(IS=10FA RS=20 CJO=5PF VJ=0.7 M=0.3 BV=3.5)

.MODEL DZ2 D(IS=10FA RS=20 CJO=3PF BV=100)

.MODEL QP PNP(IS=10FA BF=100 RB=150 TF=15NS TR=300NS VAF=40 IKF=20MA +
CJE=5PF PTF=20 CJC=5PF XTB=1.5)

.ENDS UC3838CS

*

.MODEL D914 D(IS=1.59NA RS=1.2 N=1.68 TT=4NS CJO=1.6PF VJ=0.8 M=0.12
BV=100)

.MODEL DZ1 D(BV=30.9 IBV=1MA)

.MODEL D1N6276 D(IS=30NA RS=0.01 N=1.81 TT=20NS CJO=4500PF VJ=0.85
M=0.375

+ BV=16 IBV=10MA)

* THIS IS A TRANSZORB TYPE TRANSIENT VOLTAGE SUPPRESSOR FOR +15VP.S.
AVAIL.

* FROM MOT., GSI. WILL HANDLE 1500W FOR 1MSEC, WITH 64A PEAK=23.5V(MAX).
.END

VITA

Travis N. Blalock was born in Knoxville, Tennessee on January 20, 1962. He attended elementary and secondary school in Knoxville and was graduated from Farragut High School in 1980. Entering The University of Tennessee at Knoxville in the Fall of 1980, he participated in the Cooperative Engineering Program with work assignments at NASA Langley Research Center.

After graduating from The University of Tennessee in March of 1985 with a Bachelor of Science degree in Electrical Engineering, the author returned to NASA Langley Research Center, and worked for eighteen months in the materials research area. The author then returned to The University of Tennessee to pursue an advanced degree. He is currently pursuing a Doctor of Philosophy degree in microelectronics at Auburn University.

He is married to the former Mary Elizabeth Whitaker of Newport News, Virginia.