A Highly Integrated Gate Driver with 100% Duty Cycle Capability and High Output Current Drive for Wide-Bandgap Power Switches in Extreme Environments

A Dissertation Presented for
The Doctor of Philosophy Degree
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DEDICATION

For my father.

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ABSTRACT

High-temperature integrated circuits fill a need in applications where there are obvious benefits to reduced thermal management or where circuitry is placed away from temperature extremes. Examples of these applications include aerospace, automotive, power generation, and well-logging. This work focuses on the automotive applications, in which the growing demand for hybrid electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEVs), and fuel cell vehicles (FCVs) has increased the need for high-temperature electronics that can operate at the extreme ambient temperatures that exist under the hood, which can be in excess of 150°C. Silicon carbide (SiC) and other wide-bandgap power switches that can function at these temperature extremes are now entering the market. To take full advantage of their potential, high-temperature capable circuits that can also operate in these environments are required.

This work presents a high-temperature, high-voltage, silicon-on-insulator (SOI) based gate driver designed for SiC and other wide-bandgap power switches for DC-DC converters and traction drives in HEVs. This highly integrated gate driver integrated circuit (IC) has been designed to operate at ambient temperatures up to 200ºC, have a high on-chip drive current, require a minimum complement of off-chip components, and be capable of operating at a 100% high-side duty cycle. Successful operation of the gate driver circuit across temperature with minimal or no thermal management will help to achieve higher power-to-weight and power-to-volume ratios for the power electronics modules in HEVs and, therefore, higher efficiency.

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CHAPTER 1

High-Temperature Electronics

Electronic components capable of operating reliably in high-temperature environments can serve a function in a range of applications. Semiconductor-based electronics capable of operating at ambient temperatures above 150°C with reduced or no need for thermal management systems have potential in industries including automotive, aerospace, well-logging, and energy production [1]-[6]. Power electronic modules, which typically contain power semiconductor devices along with relatively low-power control electronics and components, are an integral part of these systems. Wide-bandgap (WBG) power device technologies that are able to operate in these high-temperature environments are maturing and entering the market. Hence, there is a need for associated electronic components that are able to tolerate these temperature extremes. Table 1.1 shows the classifications for extreme temperature electronics [7].

Automotive Applications

The automotive sector is a potentially high volume consumer of high-temperature electronic products, which include an array of under the hood components such as sensors for engine operation, brake systems, exhaust sensing, and power steering [6][8][9]. Additionally, the ongoing development of hybrid electrics vehicles (HEVs) by the automotive industry is a

Table 1.1. Classes of extreme temperature electronics based on temperature tolerance [7].

Electronics Category	Temperature Range
Low-Temperature Electronics	< –55°C
Cryogenic Electronics	< –150°C
High-Temperature Electronics	> 125°C
Wide-Temperature Electronics	< –55°C to > 125°C

potentially large growth area for high-temperature electronics. HEVs are being utilized to increase fuel efficiency amid rising fuel costs and potential shortages and reduce emissions to meet ever-tightening government standards [10]. These improvements over traditional internal combustion engines (ICE) may lead to increasing demand for hybrid electric vehicles.

Current research in the automotive sector on incorporating electronics and electrical systems into automobiles involve three major vehicle technologies, discussed below, that take advantage of the efficiency gained from utilizing electric motor drives. The first technology, HEVs, use either ICEs or diesel engines in conjunction with electric motors to enhance the performance and efficiency (e.g., fuel economy) of the vehicle [10][11]. For clarity, in this document 'engine' will refer to the gas or diesel engine and 'motor' will refer to the electric motor. Series HEVs have a gas or diesel engine that is used to charge the battery pack. In this configuration the electric motor is the sole source of power to the wheels. In parallel HEVs, the electric motor and gas or diesel engine are in parallel, meaning they are both capable of applying power to the drive wheels. However, these parallel HEVs require more complex control systems.

Second, plug-in hybrid electric vehicles (PHEVs) are similar to HEVs and use an ICE in conjunction with a motor to increase efficiency. However, PHEVs have larger battery packs than HEVs and are designed so they can operate solely on the electric motor for short distances [10][11]. PHEVs also have an external charging capability not found in HEVs, so additional efficiency can be gained by recharging the battery from the electrical grid rather than using fuel. For longer distance travel, the engine can be used to power the wheels or recharge the battery pack, depending on the configuration. In these ways, PHEVs maintain the benefits of HEVs while increasing efficiency and providing electric-only capability.

Third, fuel cell vehicles (FCVs) replace the traditional ICE with an electric generator that uses hydrogen as fuel. FCVs afford potential emissions reductions of 55% compared to traditional ICEs and 31.5% compared to standard HEVs [12]. However, although FCVs have higher tank-to-wheel efficiency than ICEs, they have lower tank-to-wheel efficiency than state-of-the-art HEVs [13]. While FCVs may serve as replacements for ICEs in the future, they are not yet ready for commercialization [12][13].

High-Temperature Electronics in the Automotive Industry

The market has seen an increase in demand for HEVs based on recent performance and fuel economy improvements. However, in order to move away from ICEs toward HEVs or PHEVs with higher efficiency, the mechanical and hydraulic systems currently used in these vehicles must be replaced by electromechanical systems [6][9][14]. These systems require power electronic modules, such as those used with DC-DC converters and inverters, underscoring the need to develop reliable, high-performance electronic components.

State-of-the-art HEV technologies utilize two cooling loops, a 105°C cooling loop used by ICEs to cool components under the hood and a 70°C coolant loop. The second coolant loop is used by the power electronics circuitry, which mostly consists of commercially available components rated for temperatures up to only 85°C [15]. In order to reduce the weight and volume requirements associated with power electronics modules, a tactic being considered by the automotive industry is to remove the 70°C coolant loop in favor of the existing 105°C loop or utilize air cooling [8]. However, operation under these extremes is beyond the capabilities of most commercially available electronics, Table 1.2 [5][15]. Achieving this goal will require packaging, passive components, and electronic circuits that are capable of operating reliably at the high ambient temperatures present near the engine without or with minimal thermal management [8]. Removal of the 70°C cooling loop through the introduction of high-temperature capable components can help realize a significant savings in the mass and volume of power electronic modules [15].

Differences in the configuration and placement of electronic components, such as power electronic modules, can cause wide variation in the requisite operating temperatures of the

Table 1.2. Classes of standard commercial electronics based on temperature capability [6].

Component Classification	Temperature Range
Commercial	0°C to 70°C
Industrial	–25°C to 85°C
Military	–55°C to 125°C

components in the engine compartment. Table 1.3 presents a summary of the requirements for high-temperature automotive electronics published by Auburn University, DaimlerChrysler, and Eaton Corporation [4]. The ambient temperature of much of the space in the engine compartment can be in excess of 150°C, and the junction temperatures for power devices can reach at least 25°C above the ambient. Vehicles such as HEVs, with their increased electrical requirements, make use of multiple power electronic modules. These power modules include inverters (e.g., motor inverter) and DC-DC converters (bidirectional converter for high-voltage battery, low-voltage electrical system, etc.) [11][14][16][17]. To satisfy these electrical requirements while improving efficiency and decreasing mass and volume, power electronics are needed that can operate in the extreme ambient temperatures near the engine, which can be in excess of 150°C.

Gate Driver Introduction

Power electronics systems control the flow of current from a source to a load by switching a circuit 'on' and 'off.' This switching is accomplished by the 'on' and 'off' toggling of a power switch which then opens or closes the circuit, allowing or blocking the flow of current. Circuitry is required in order to control the 'on' and 'off' toggling action of the power switch. This circuitry usually takes the form of a gate driver, a common component in power electronics modules. The control signals for the power switch are logic level signals, typically generated by a microcontroller or other logic circuit. These logic-level circuits are characteristically not capable of driving the impedance presented by a power switch, therefore gate drivers are used to

Table 1.3. Automotive temperature ranges [4].

In-Vehicle Location	Temperature Range
In-transmission	150-200°C
On-engine	150-200°C
On Wheel-ABS sensors	150-250°C
Cylinder pressure	200-300°C
Exhaust sensing	ambient 300°C, up to 850°C

convert the logic level signals into control signals with sufficient voltage and current drive to switch the power devices 'on' and 'off.' The functionality of such a system will be dependent on the properties of the power device as well as the capability of the gate driver to successfully and efficiently control the 'on' and 'off' switching.

A representative configuration utilizing a gate driver, a three-phase inverter, is shown in Figure 1.1. This would be a typical system for an electric traction drive in an HEV or other electric vehicle. The three-phase inverter, made up of three phase legs, contains six power switches, Q_1 through Q_6. The 'on' and 'off' switching of these power devices controls the flow of current from the supply to the load. The control signals are generated by a logic device, such as a microcontroller, which does not have the current or voltage drive capability to directly control the operation of the power switches. The gate driver comes into use here, acting as a converter to increase the current and/or voltage levels of the control signal from the microcontroller into a signal that can operate the power switch. Often, the gate driver will serve additional purposes, including protecting the microcontroller from feedback or electromagnetic interference (EMI) from the power system, protecting the power switch or system from faults, and sending signals back to the microcontroller when a fault is detected.

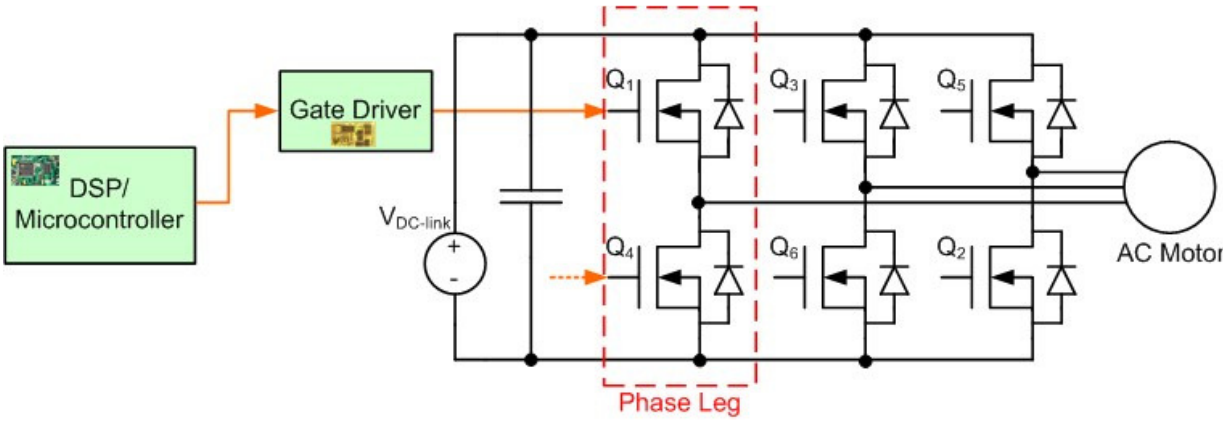


Figure 1.1. Typical gate driver configuration.

Problem Statement

In HEVs and other high-power applications, the high-temperature conditions present a demanding environment for high-temperature capable power electronics. A new generation of power electronics devices that are capable of functioning reliably at higher temperatures than silicon-based devices are maturing. Silicon carbide (SiC) and gallium nitride (GaN) wide-bandgap transistors offer a great deal of promise in these applications. While these power electronics technologies may be capable of operating with reduced cooling mechanisms in harsh environments, electronic components (such as gate drivers) that can operate alongside them are also needed. This will help achieve improved power-to-weight and power-to-volume ratios for power electronics modules and to reduce or remove the need for active and passive cooling systems [8][15].

Therefore, the goal of this research was the development of gate driver electronics capable of operating at ambient temperatures up to 200°C, which will improve the performance and capabilities of existing high-temperature electronic systems. The primary design goals for the high-temperature gate driver presented in this dissertation are shown in Table 1.4.

Table 1.4. Gate driver design goals.

Parameter	Design Goal
Operating frequency	> 20 kHz
Operating temperature range	0°C to 200°C
Supply voltage range	10 V to 30 V
On-chip charge pump to enable 100% duty cycle operation	Enable 100% duty cycle with no off-chip components
Integration	All circuits integrated on-chip with a minimum complement of off-chip components
Current drive	> 2 A at 200°C (increase current drive of previous generation gate driver)

Overview of the Dissertation

This dissertation is organized into 5 chapters. Chapter 1 introduces high-temperature electronics and their role in the automobile industry and established the motivation and goals for this work. Chapter 2 presents a review of integrated gate driver topologies available in the literature and the commercially available high-temperature drivers. Chapter 2 also presents an overview of WBG power devices and silicon-on-insulator (SOI) technology. Chapter 3 introduces the novel charge pump utilized on the gate driver and the methods being implemented to increase the maximum current drive of the circuit. Chapter 3 also presents the integration of the gate driver IC and its various components. Chapter 4 describes the test configurations used and demonstrates the measurement results obtained from the gate driver IC. Chapter 5 summarizes and concludes this work.

A list of acronyms is located in the Appendix, Table A.1.

CHAPTER 2

Power Devices for High-Temperature Applications

The need is growing for semiconductor-based power switches capable of reliable operation at junction temperatures exceeding 150°C and exhibiting high switching frequencies, high power densities, and high blocking voltages [18]. This is particularly true for automotive, well-logging, nuclear, geo-thermal, and aerospace applications. Existing silicon-based devices are incapable of operating at these temperatures and performance levels without utilizing thermal management systems and placing devices in series and in parallel configurations to increase blocking voltages and current ratings, respectively [2][18]. These systems add additional weight, complexity, and volume to the silicon-based power electronic circuits, making their use less desirable.

At temperatures approaching 150°C, silicon (Si) becomes less functional as excessive leakage currents become a major design concern [18]. These 'on' and 'off' state leakage currents cause higher switching currents, leading to increased cross-talk, and can cause latch-up related device failures [2]. One mature process technology that can circumvent some of these issues in integrated circuit applications is the silicon-on-insulator structure, which is described in the following section.

In contrast to silicon, WBG semiconductor materials such as gallium nitride and silicon carbide offer several advantages, including a lower intrinsic carrier concentration, higher electric breakdown field, and higher thermal conductivity [18]-[20]. SiC, arguably the most mature WBG device technology currently available, is the most likely technology to make an immediate impact on replacement of Si devices in high-temperature applications. SiC's bandgap energy of approximately 3.3 eV and electric breakdown field of more than $2x10^6$ V/cm are both appreciably better than bulk silicon. References [2], [18], and [21] have compiled several significant electrical properties of wide-bandgap devices in comparison with Si. These comparisons are shown in Table 2.1.

Table 2.1. Properties of select semiconductors at 300 K [2][18][21].

Property	Si	SiC	GaN	Diamond
Bandgap (eV)	1.12	3.26	3.4	5.5
Relative dielectric constant	11.9	9.2	9.0	5.5
Breakdown field (kV/cm)	250	2200	2000	10000
Thermal conductivity (W/cm·K)	1.5	4.6	3.3	22.0
Electron Saturated Velocity ($\times 10^7$ cm/s)	1.0	2.0	2.2	2.7
Electron Mobility ($cm^2/V{\cdot}s$)	1500	1000	1250	2200
Hole Mobility ($cm^2/V{\cdot}s$)	600	115	850	850

SiC has a lower intrinsic carrier concentration than Si and therefore does not run into uncontrolled conductivity until much higher temperatures [2][18]. Also, due to the lower intrinsic carrier concentration, the p-n junction leakage current in SiC is an order of magnitude lower than Si. Additionally, the electric breakdown field of SiC is much larger than Si. This allows SiC devices to have thinner epitaxial (drift) layers which can support higher breakdown voltages [18]. A smaller drift layer allows a device to have lower drift resistance and therefore reduced conduction losses with a lower per area resistance and a lower forward voltage drop. The reduced drift layer thickness also increases the switching speed of bipolar devices by reducing the minority carrier charge storage. Furthermore, SiC's high thermal conductivity enables higher per area power densities, which facilitates more compact devices [21].

SOI Process Technology

Wide-bandgap semiconductors, as discussed in the previous section, are able to operate at higher temperatures than bulk silicon devices. However, there is no commercial SiC or other WBG semiconductor-based integrated circuit design process. Therefore, for integrated circuit (IC) applications where high-temperature operation is desired, such as in environments with WBG power switches, a substitute for bulk silicon ICs is needed. For integrated circuits with relatively low power needs (up to approximately 300°C), the most mature and commercially available alternative is silicon-on-insulator process technology [22]-[24]. SOI processes are widely available for commercial integrated circuit development.

A cross-section comparing silicon-based metal oxide semiconductor field effect transistors (MOSFETs) on bulk and SOI processes is demonstrated in Figure 2.1. The buried oxide layer, a component of the SOI structure, restricts the leakage paths related to the N-well, as well as the n-channel source and drain p-n junctions. This effectively reduces the leakage current by decreasing the leakage area of the junction by approximately 100 compared to a typical bulk silicon process [22]. Additionally, the threshold voltage variation of SOI-based devices over temperature is lower than in bulk silicon devices [23]. SOI devices also have inherently improved latch-up immunity compared to bulk silicon devices [23]. Factors such as the reduced leakage current, lower device performance variation, and higher latch-up immunity help enable SOI-based devices and circuits capable of successful operation at temperatures up to -300°C. This is well above the approximately 150°C range of conventional bulk silicon-based devices.

Several foundries offer commercial SOI-based semiconductor processes and services with a range of supported devices and supply voltages [25]-[27]. For the design and implementation of the high-temperature gate driver IC presented in this paper, a bipolar-complementary metal oxide semiconductor (CMOS)- double-diffused metal oxide semiconductor (DMOS) (Bipolar-CMOS-DMOS or BCD) on silicon-on-insulator (BCD-on-SOI) process that combines SOI technology with high-voltage compatible devices was chosen. The process utilized for this work is a 0.8 micron, 2-poly, 3-metal process.

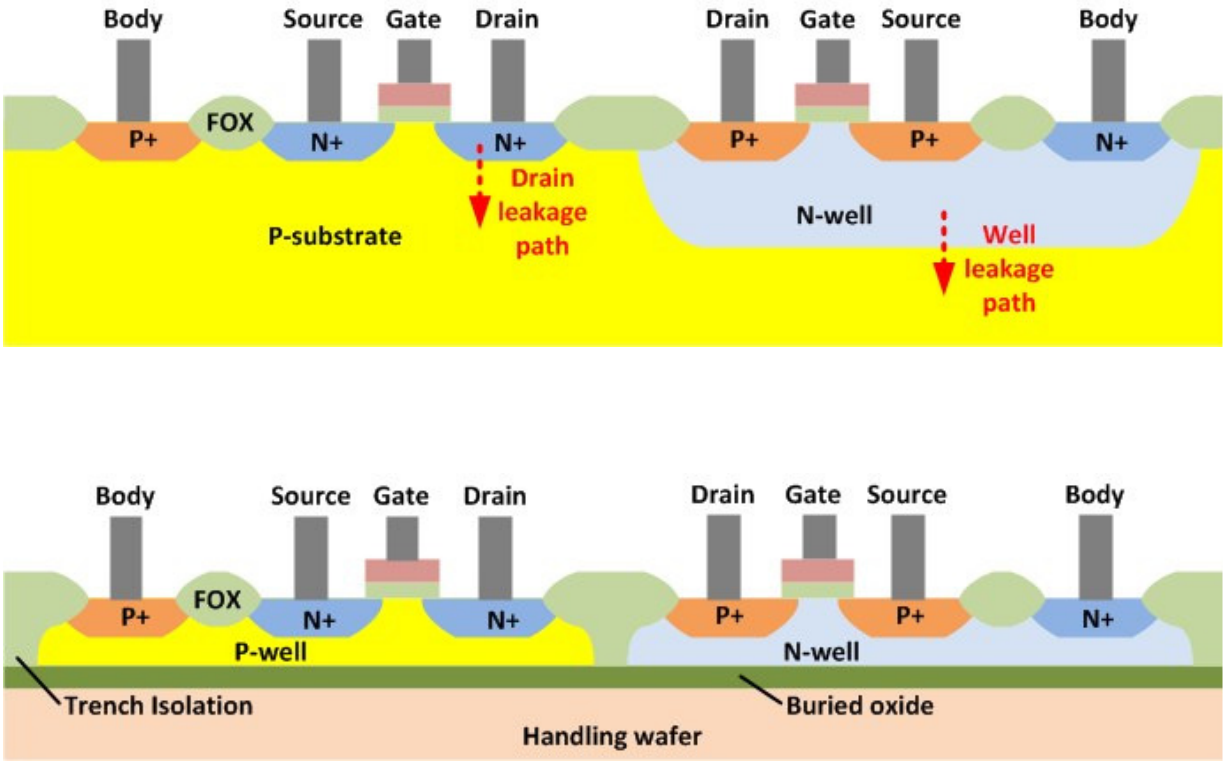


Figure 2.1. Cross-section of bulk-CMOS (top) and SOI (bottom) transistors**.**

Literature Review
High-Temperature Integrated Drivers

Several integrated gate driver topologies have been presented in the literature [28]-[40]. These papers addressed different aspects of integrated gate driver design and operation. Where available, information on drive current, off-chip components, operating frequencies, IC integration and features, and other key characteristics of each driver are reported below. However, of the literature reviewed, only the gate driver reported in [28] demonstrated functionality at temperatures above 150°C. Although Valle-Mayorga et al. reported successful operation at ambient temperatures greater than 200°C, their output drive current without external current boosting stages was limited to 150 mA. No demonstration of this current drive over temperature was provided. Additionally, the authors reported having a transformer based isolation solution, though there was no discussion of how the transformer was implemented, just that it was implemented off-chip and required additional power devices to generate the necessary *dv/dt* to drive the transformer. The design was also not capable of 100% duty cycle operation and required a large off-chip bootstrap capacitor. On-chip features included an under-voltage lock out (UVLO) and over-current protection circuitry. The work was implemented in a 1 µm SOI process.

A gate driver aimed at controlling the switching speed and, therefore, losses of a power device was presented in [29]. Fomani et al. addressed how to control the switching speed by increasing or decreasing the current drive of their gate driver IC, which in turn controls the switching speed of the discrete, off-chip transistors used in the output stage. There was no information given on the current drive of the IC itself but the current driving capability of the discrete output devices was up to 20 A. A bootstrap capacitor was used in this configuration, limiting the lower switching speed, but the maximum reported speed for the system was given as 2 MHz. Off-chip components required by this gate driver included the external output drivers, bootstrap circuitry, and the waveform shaping logic (dead-time controller, level shifter, etc.). The gate driver was fabricated on a TSMC 0.25 µm high-voltage CMOS (HVCMOS) process. No information regarding operation over temperature was presented.

Li et al. demonstrated a half-bridge gate driver with integrated power switches [30]. Philips EZ-HV SOI process with integrated power devices was used for this design. The gate driver achieved a current drive of 350 mA sourcing and 750 mA sinking. The design required an off-chip, 47 nF bootstrap capacitor for the high-side circuitry, which also means it was not capable of DC operation. There was no discussion of operation across temperature or operational frequency.

A monolithic insulated gate bipolar transistor (IGBT) gate driver IC implemented in 50 V, 0.8-µm bulk CMOS process was demonstrated in [31]. The peak output current was given as 100 mA, but there was no discussion of the performance of the design over temperature. Kim et al. listed no operational frequency range for the gate drive IC and mentioned no large off-chip component requirements. The gate driver also included a UVLO and a 5-V regulator.

An integrated gate driver utilizing an isolation transformer and capable of high speed operation was presented in [32]. Nguyen et al. presented a gate driver IC that was essentially a level shifter and inverter-based exponential horn for creating a high current drive that can be used as the input to an isolation transformer. The transformer and demodulation circuitry were located off-chip and the demodulation circuit, not the gate driver, was used to drive the power switch. The output drive of the IC was given as 3 A, with a maximum switching speed of 500 kHz. No information on the circuit's capabilities over temperature was given.

A high-speed gate driver IC for GaN power devices was discussed in [33] and [34]. In these papers, Wang and colleagues proposed an integrated gate driver using a charge pump and two level shifters to drive an inverter-based (push-pull) complementary CMOS output stage. It was designed to drive GaN field effect transistors (FETs) with a power rating of 100 V and 1 A. The maximum operating frequency was 10 MHz and the current drive capability was reported as 50 mA. The design required an off-chip charge pump and two power supplies. The IC was designed in a 0.35 µm 50 V HVCMOS process from Austriamicrosystems (AMS). The temperature performance was not discussed.

An isolated CMOS gate driver for power MOSFETs was presented by Simonot and colleagues in [35] and [36]. This design included transformer based isolation, but no information was given regarding the protection provided by the transformer. Due to its implementation on a standard

CMOS process (AMS 0.35 µm) the metal to substrate isolation may be quite low. The modulation and demodulation circuitry for the transformer was located off-chip, as well as the storage capacitor and charging system for the high-side circuitry. This gate driver was capable of 300 mA output current drive and operated at speeds up to 250 kHz. No information about its operation over temperature was provided.

An IGBT gate driver circuit was demonstrated in [37]. Dalau et al. incorporated several protection features into the gate drive IC, including two-stage turn-off to limit over-voltage when switching 'off' and de-saturation detection circuitry. This IC was implemented using a 1-µm BCD3S process and was designed to drive a 1200-V, 80-A IGBT. The source current and sink current output pins on this IC were not connected on-chip. This allowed for the use of separate off-chip gate resistors for limiting the sourcing and sinking currents, thus enabling the independent adjustment of the 'on' and 'off' switching speed of the driver. The peak transient output current drive of the circuit was 1.2 A sinking and 0.75 A sourcing over a temperature range of –20°C to 125°C.

A novel approach termed 'Drive-by-Microwave' was presented in [38]. Nagai et al. utilized an electromagnetic resonant coupler (EMRC), similar in function to a transformer, to both isolate and power a simple gate driver from a 'drive-by-microwave' frontend that provided the microwave signal to the EMRC. On-chip rectifiers comprised of aluminum gallium nitride (AlGaN)/GaN HFETs were then utilized to drive the GaN device from the received signal. All of the components of the driver (EMRC and HFETs) were on a sapphire substrate. The system was shown to operate with a 10 kHz switching frequency on a 5.8 GHz carrier. No information was provided regarding current drive or temperature capability of the IC but the ERMC was specified to have a breakdown voltage of 9.6 kV.

A CMOS gate driver for IGBTs was presented in [39] and [40]. That IC was developed in a 2.5 µm CMOS with p-channel extended drain MOSFET (ED-pMOSFET) to form high-voltage devices with a V_{DS} breakdown of 36-V. The gate driver was demonstrated driving a 1nF load at 25 kHz with a maximum stated load current capability of 300 mA. No discussion of the temperature capabilities of the circuit was presented.

Table 2.2 and Table 2.3 record several important specifications for the reviewed gate driver ICs. Only [28] was capable of operation above 150°C but with a limited current drive and several off-chip components. The gate driver in [32] was capable of a high 3-A current drive but only at room temperature and with a simple design topology. Two of the reviewed papers had a charge pump, [34] and [36], but they were implemented off-chip.

High-Temperature Non-Integrated Driver

In the literature reviewed, there were several non-integrated gate driver topologies that were developed for wide-bandgap power switches [41]-[48]. However, only [47] and [48] presented a high-temperature non-integrated solution that can operate above 150°C, Table 2.4. The silicon carbide junction gate field effect transistor (JFET) driver presented by Kolar and colleagues in Waffler et al. and Round et al. can operate at up to 200°C ambient temperature. It was capable of driving SiC JFETs at up to 25 $V_{peak\text{-}to\text{-}peak}$ and driving load currents of 5 A to 6 A at temperature. This current drive was accomplished using Honeywell's 1-A SOI MOSFET (HTNFET) discrete transistors. This driver incorporated transformer-based isolation using a high-temperature magnetic core transformer but no other protection features were present.

Table 2.2. Literature reviewed for integrated gate drivers.

	Temperature	Current Drive	Isolation	Process Technology	Frequency	Active or Large Off-chip Components
Valle-Mayorga et al. [28]	Up to 225°C	"Up to" 150 mA without external driver stages	Transformer based isolation mentioned but no discussion of implementation	1 µm SOI CMOS	200 kHz Not capable of DC operation	Output stage (Power transistors), Oscillator 20 nF cap., transformer, 100 nF bootstrap cap.
Fomani et al. [29]	N/A	IC drive capability not stated; 20 A with external output drivers	N/A	TSMC 0.25 µm 12 V HVCMOS	2 MHz Not capable of DC operation	External output drivers, bootstrap circuit
Li et al. [30]	N/A	Sourcing 350 mA Sinking 750 mA	N/A	Philips EZ-HV SOI Technology	1 MHz Not capable of DC operation	47 nF bootstrap cap.
Kim et al. [31]	N/A	100 mA	N/A	0.8 µm (50 V) CMOS	No frequency range stated	Not discussed
Nguyen et al. [32]	N/A	3 A	Transformer based, completely external	Austriamicrosystems. H35B4 0.35 µm 50V HV-CMOS	500 kHz (complementary devices)	Isolation transformer, demodulation circuitry
Wang et al. [33][34]	N/A	50 mA	N/A	Austriamicrosystems. H35B4 0.35 µm 50V HV-CMOS	10 MHz	Charge pump, two power supplies
Simonot et al. [35][36]	N/A	300 mA max. demonstrated	On-chip coreless transformer (~1 kV)	Austriamicrosystems 0.35 µm CMOS	250 kHz	Modulation/demodulation circuitry, storage capacitor (100 nF) and charging system
Dalau et al. [37]	–20°C to 125°C	Sourcing 1.2 A Sinking 0.75 A	N/A	1 µm BCD3S process	No frequency range stated	Off-chip zener diode, capacitors (10 nF, etc.)
Nagai et al. [38]	N/A	Sourcing/sinking current not stated	Electromagnetic resonant coupler (EMRC)	AlGaN/GaN HFETs and EMRC on a sapphire substrate	10 kHz	'Drive-by-Microwave' frontend
Perez et al. [39] **Millan et al. [40]**	N/A	300 mA	N/A	2.5 µm CMOS	25 kHz (complementary devices)	Not discussed

Table 2.3. Literature reviewed for integrated gate drivers, continued.

	Temperature	Voltage	Dimensions	Features (unless otherwise stated, features include input signal processing)
Valle-Mayorga et al. [28]	Up to 225°C	15 V	2 x 3162 x 3162 μm^2 Plus external output drivers and capacitors	UVLO, over-current protection
Fomani et al. [29]	N/A	Not stated (12-V for technology)	1400 x 1200 μm^2	N/A, waveform shaping (dead time, level shifting circuitry all off-chip)
Li et al. [30]	N/A	10 V	Chip micrograph shown, no dimensions given	N/A
Kim et al. [31]	N/A	15 V	Chip micrograph shown, no dimensions given	UVLO, 5-V regulator
Nguyen et al. [32]	N/A	15 V	Chip micrograph shown, no dimensions given	N/A, simple inverter topology
Wang et al. [33][34]	N/A	3.3 V, –7 V	1745 x 1640 μm^2	N/A
Simonot et al. [35][36]	N/A	4 V	2500 x 2500 μm^2	N/A, secondary charge pump capacitors
Dalau et al. [37]	–20°C to 125°C	20 V	Chip micrograph shown, no dimensions given	De-saturation, IGBT two-level turn-off driver
Nagai et al. [38]	N/A	2 V	5000 x 2.5 μm^2	EMRC
Perez et al. [39] **Millan et al. [40]**	N/A	15 V	Chip micrograph shown, no dimensions given.	N/A

Table 2.4. Literature reviewed for non-integrated high-temperature gate drivers.

	Temperature	Current Drive	Output Voltage	Dimensions	Frequency	Features
Round et al.[47] **Waffler et al. [48]**	Up to 200°C	5 A – 6 A (1A SOI MOSFET by Honeywell (HTNFET))	25 V	Estimated to be 44 x 18 mm^2	250 kHz	Transformer-based isolation

Commercially Available Integrated Gate Driver Circuits for High Temperature

CISSOID, a fabless integrated circuit design company located in Belgium, has commercialized several high-temperature integrated circuits developed on an SOI process. Most of these components are rated to operate from junction temperatures of –55°C to 225°C [49]. CISSOID markets their high-temperature gate drivers under their TITAN umbrella of products. Under TITAN they are currently marketing four series of gate driver ICs and systems, including both stand-alone chips and ICs meant to be used in tandem with other products.

CISSOID's first gate driver IC, Pallas (CHT-PALLAS), is a high-temperature capable full-bridge MOSFET driver [50]. Pallas contains two integrated driver channels, a low-side and a high-side, to enable full bridge configurations. This driver circuit's high-side and low-side outputs can operate independently with an output range of up to 10 V on the low-side and 60-V on the high-side. Pallas can source and sink transient currents up to 80 mA and 20 mA on the low-side and high-side channels, respectively, using n-channel output drivers. Pallas also utilizes a charge pump, which requires two 470 nF capacitors and a 200 kHz clock signal.

Their second gate driver product, a half-bridge driver, is marketed as Hyperion (CHT-HYPERION) [51]. Hyperion is designed to drive dual external n-channel MOSFETs. The gate driver has a peak current drive of 1 A and includes a UVLO circuit. It requires an external 100 nF bootstrap capacitor. The datasheet states it can drive 3 nF at frequencies up to 300 kHz.

The next CISSOID product is a dual-chip solution referred to as Themis (CHT-THEMIS) and Atlas (CHT-ATLAS), [52] and [53], respectively. This solution is meant to drive silicon carbide MOSFET and JET devices at up to 2 A per channel. This configuration requires a 22 nF bootstrap capacitor and numerous smaller off-chip passives. Protection circuitry included on Themis includes on-chip regulators, a UVLO, and a de-saturation detection circuit. No frequency constraint information is given.

CISSOID also markets a PCB-based gate driver phase leg design, Hades (EVK-HADES) [54]. Implemented on a polyimide printed circuit board (PCB) substrate, the operational range of this system is up to 175°C ambient temperature. Hades can drive up to 4 A load current with two

driver stages in parallel and can operate at up to 150 kHz. It implements Themis, Atlas, Magma, and other CISSOID and discrete components on a single board.

A summary of the CISSOID gate driver offerings is presented in Table 2.5 and Table 2.6.

Summary

To this author's best knowledge, based on the literature reviewed, there are currently no integrated gate driver solutions capable of operating at temperatures up to 200°C and driving a load current of more than 2 A. Additionally, all of the integrated gate drivers capable of operating at up to 200°C (Valle-Mayorga et al. and some of the CISSOID offerings), required off-chip components, such as large capacitors, that must be high-temperature capable.

Additionally, none of the three gate drivers that employed a charge pump (CISSOID Pallas, Wang et al. driver, and Simonot et al. driver) were fully integrated. The Pallas charge pump required two 470 nF off-chip capacitors and a 200 MHz control signal. The Wang et al. and Simonot et al. drivers used off-chip charge pump circuitry.

Lastly, none of the drivers incorporated the number of protection circuits developed on the integrated gate driver presented in this work. In the literature reviewed, at most two protection circuits were present on an offering (UVLO and de-saturation circuitry). As will be discussed in Chapter 3, the gate driver described here has a much larger complement of integrated circuitry than in the literature presented.

Table 2.5. Commercial high-temperature integrated gate drivers.

	Temperature	Current Drive	Isolation	Technology	Frequency	Active or Large Off-chip Components
CISSOID Pallas	–55°C to 225°C junction	80 mA (low-side channel) 20 mA (high-side channel)	N/A	N/A	Not stated	200 kHz clock for charge pump. Two 470 nF bootstrap capacitors
CISSOID Hyperion	–55°C to 225°C junction	1 A	N/A	N/A	3 nF at up to 500 kHz	100 nF bootstrap capacitor
CISSOID Themis and Atlas	–55°C to 225°C junction	2 A (two channels per chip in parallel can output 4 A)	Possible with additional chip CHT-RHEA	N/A	Not stated	22 nF bootstrap capacitor, multiple smaller capacitors
CISSOID Hades	175°C	2 A (4 A accomplished through parallel drivers)	Transformer based, on-board	Polyimide PCB	150 kHz	Board-level gate driver implementation

Table 2.6. Commercial high-temperature integrated gate drivers, continued.

	Temperature	Voltage	Dimensions	Features (unless otherwise stated, features include input signal processing)
CISSOID Pallas	–55°C to 225°C junction	10 V	N/A	Full-bridge (up to 60 V)
CISSOID Hyperion	–55°C to 225°C junction	5 V	N/A	UVLO
CISSOID Themis and Atlas	–55°C to 225°C junction	5 V to 30 V	N/A	Themis (UVLO, de-saturation, regulators)
CISSOID Hades	175°C	12 V	N/A	Polyimide PCB, isolation (RHEA), Themis features

Brief Overview of Gate Driver Research

The research presented in this dissertation is the continuation of efforts to develop a high-temperature, high-voltage integrated gate driver IC. A brief overview of previous research on the gate driver is given in this section, which includes three "generations" of gate driver design. Figure 2.2 shows a block diagram of the 1st generation, or 1G, gate driver.

This gate driver circuit has six distinct blocks: the output drivers, M_H and M_L, low-side and high-side buffers, bootstrap capacitor based charge pump, low-side to high-side level shifters, the SR latch, and the edge detector. The core functionality of the previous gate driver designs is briefly described here but is covered more thoroughly in [55]-[57]. The low-side logic input drives the low-side buffer, which drives the large output transistor M_L. The high-side logic signal is the input to the edge detector, which generates two narrow pulse trains (SET and RESET), one at the rising edge of the input signal and the other at the falling edge. The level shifter circuits are used to convert the logic-level SET and RESET voltage signals into current signals. These current signals then are converted back into voltage signals referenced to the high-side supply, V_{OP}. The high-side SR latch then uses the high-side referenced SET and RESET voltage waveforms to generate the control signal to drive the high-side buffer, which in turn drives the high-side NMOS switch, M_H.

The 2nd generation (2G) gate driver block diagram is shown in Figure 2.3. New circuitry on the 2G driver included a dead-zone generator, an input stage, and an on-chip voltage regulator. An

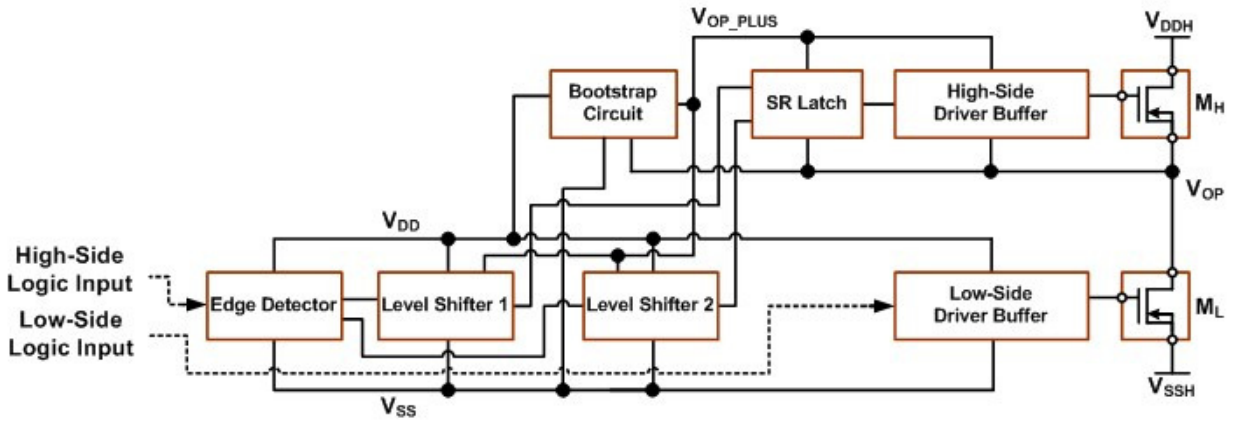


Figure 2.2. Block diagram of the 1G gate driver.

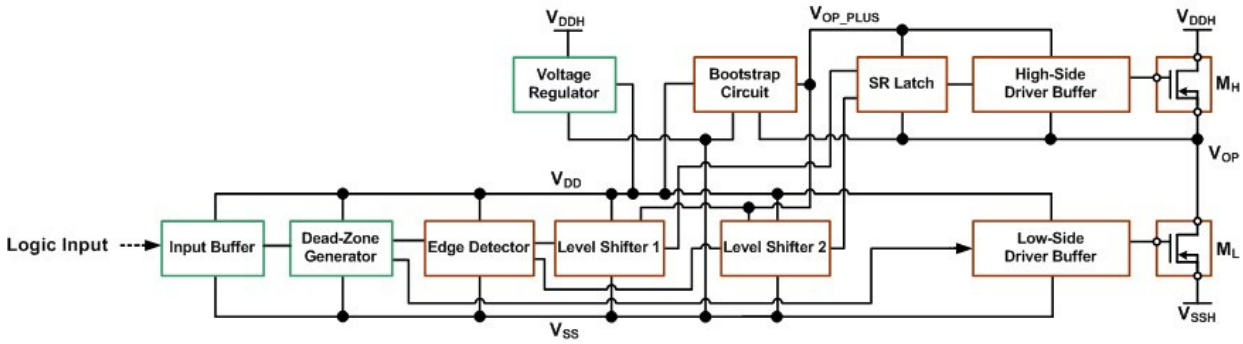


Figure 2.3. Block diagram of the 2G gate driver.

on-chip input buffer circuit was added to provide a cleaner input signal to the edge detector circuit. The dead-time generator creates two non-overlapping waveforms from the logic level input signal. The dead time separating the 'on' state of these two signals ensures the complementary 'on' and 'off' switching of the output stage transistors without shoot-through, or crowbar, current. Since the pulse trains generated by this circuit pass through different circuit paths, an additional pulse shaper circuit is also integrated into the dead-zone generator to further modify the low-side control signal to ensure complementary switching of the M_H and M_L transistors.

Additionally, the 2G gate driver included an on-chip low-dropout (LDO) voltage regulator to generate a 5-V supply rail (V_{DD}) from a 15 V to 30 V high-side supply voltage (V_{DDH}). This circuit utilized a bandgap reference and differential amplifier to generate a reference voltage.

The block diagram for the 3rd generation (3G) gate driver is shown in Figure 2.4. In this revision the input stage was modified to include a Schmitt trigger to create a reliable control signal from the potentially noisy input signal. Protection circuits added to this driver included a temperature sensor, an under-voltage lock out (UVLO) circuit, and a short circuit detection circuit. Feedback signals from the protection circuits are connected to the input stage through a NOR gate that creates a HIGH enable signal. If a feedback signal shows a fault, the enable signal goes LOW, and the output of the gate driver goes 'off', deactivating the power switch.

The dead-time controller circuit block generates two non-overlapping, complementary signals from the buffered input signal. This is done by generating a temperature independent bias current and using it to bias a delay network, which has two programmable delay settings. Two

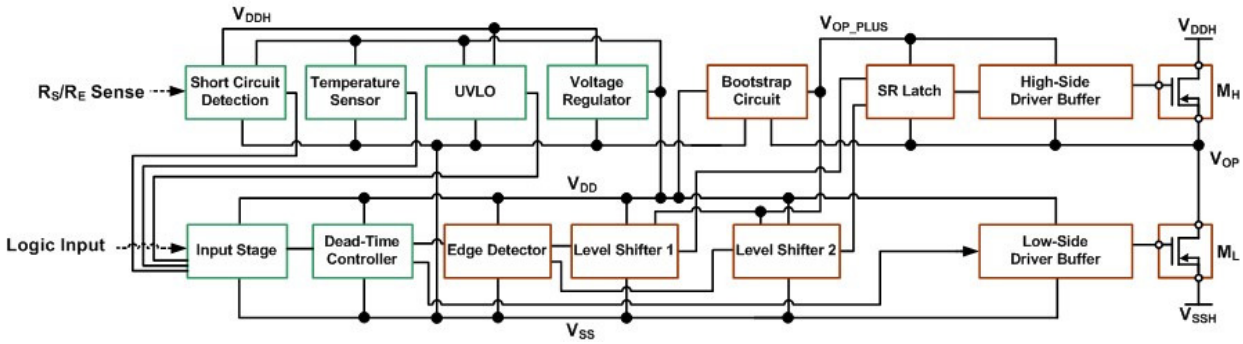


Figure 2.4. Block diagram of the 3G gate driver.

large aspect ratio, high-voltage (45-V) NMOS devices (M_L and M_H) constitute the half-bridge output stage of the gate driver circuit. Complementary switching of these two NMOS devices connects the output terminal of the gate driver to one of the two supply rails (V_{DDH} or V_{SSH}). The rail voltages used are determined according to the type of SiC power switch being driven by the gate driver. This gate driver is designed to operate on V_{DDH} levels between 10 V to 30 V above V_{SSH}.

The large W/L ratios of the two output transistors present a large capacitive load to the control circuitry of the gate driver. Since these output transistors must have fast switching times, multi-stage buffers are employed in this design to mitigate the capacitive loading effects.

CHAPTER 3

4G Gate Driver System Overview

New circuits and modifications instituted for the 4th generation (4G) gate driver IC, Figure 3.1, include the addition of a charge pump, a gate current monitoring circuit, a de-saturation detection circuit, and an enhanced voltage regulator [58]-[62]. The linear voltage regulator on the 3G driver was removed in favor of a LM-723 Zener-based regulator. Nearly all of the remaining gate driver circuits have been updated as well. The output current drive of the gate driver has been increased and the lower than expected current drive was investigated. Also, the level of integration of the gate drive IC has been increased, with all new circuitry incorporated on-chip and fewer required off-chip components.

This section contains a discussion of the 4G gate driver IC's novel circuits and capabilities made over that of the previous work. This includes the design of a novel fully integrated charge pump to enable the operation of the gate driver with a 100% high-side duty cycle. Additionally, the current drive of the IC will be discussed and changes presented to increase the sourcing and sinking current. Finally, the incorporation of the gate driver circuits into a fully integrated device will be presented.

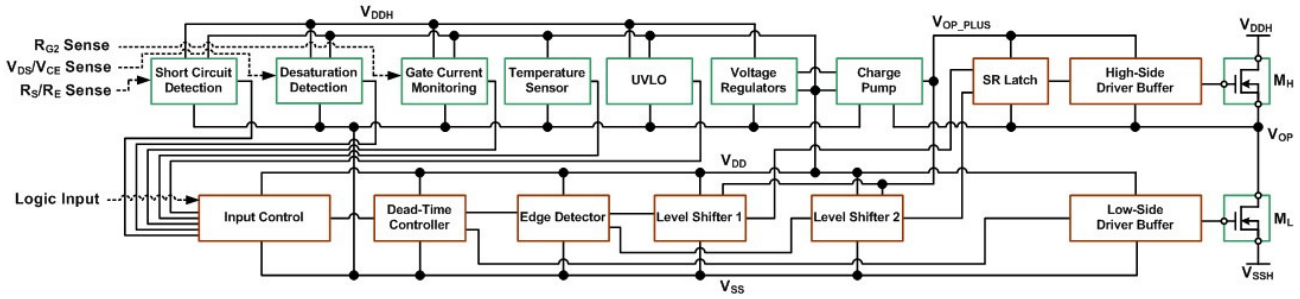


Figure 3.1. 4G (*Corinth*) gate driver block diagram.

Charge Pump

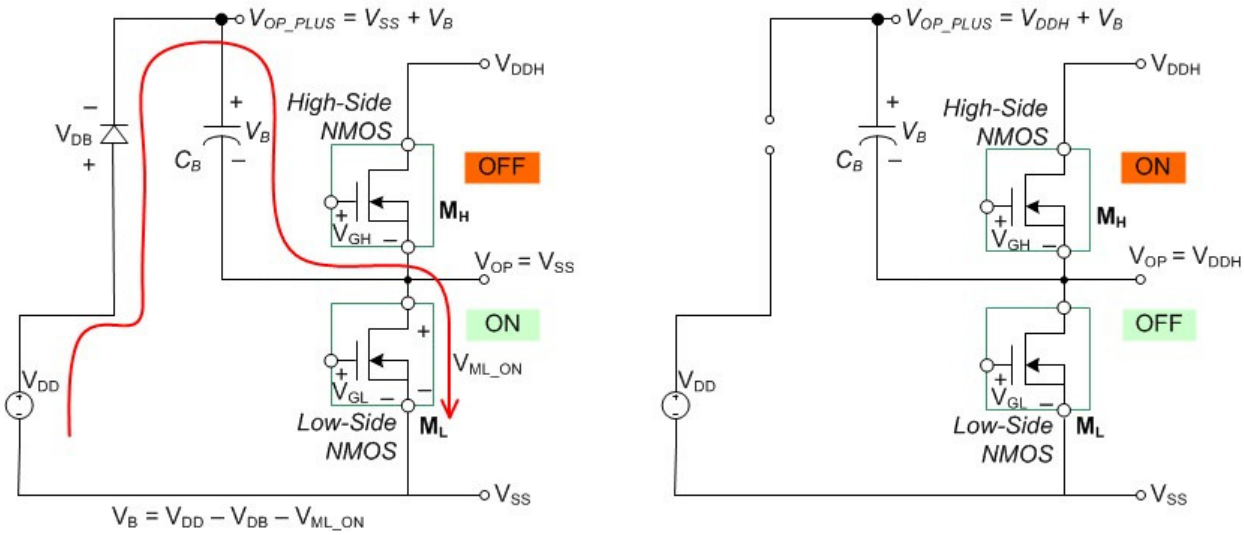
On the 4G gate driver, a fully integrated charge pump is utilized to replace the bootstrap capacitor and diode used in previous iterations of the circuit. The bootstrap circuit was used to provide a 5-V floating supply rail to power the high-side circuitry. A brief study of the bootstrap circuit follows.

Bootstrap Capacitor Based Floating Supply

The bootstrap circuit consists of a bootstrap capacitor, C_B, and diode, D_B, Figure 2.4 and Figure 3.2 [7]. This circuit provides a floating supply voltage (V_{OP_PLUS}) referenced to V_{OP}, which is capable of powering the high-side circuitry of the gate driver when the output of the gate driver is 'on,' or HIGH. Figure 3.2 demonstrates the operation of the bootstrap circuit. When the output of the gate driver is LOW, or 'off,' V_{OP} is at the same potential as V_{SS}. In this configuration M_L is 'on' and M_H is 'off', Figure 3.2 (a). The bootstrap capacitor is charged through diode D_B to voltage V_B, which is given by

$$V_B = V_{DD} - V_{DB} - V_{ML_ON}$$

where V_{DD} is the supply voltage charging C_B, V_{DB} is the voltage drop across diode D_B, and V_{ML_ON} is the 'on'-state voltage across the low-side output driver, M_L. In the second mode of operation, Figure 3.2(b), where M_L is 'off' and the high-side output driver, M_H, is 'on,' V_{OP} increases to V_{DDH}, reverse biasing diode D_B. In this configuration, the bootstrap capacitor functions as a floating supply referenced to V_{OP}. This floating supply is necessary to power the high-side circuitry (level shifters, SR latch, and high-side buffer) in order to drive M_H, which requires a gate control signal above V_{DDH}. The V_{OP} and V_{OP_PLUS} nodes operate as floating supply rails for the high-side circuitry.



(a) (b)

Figure 3.2. Bootstrap circuit operation: (a) charging the bootstrap capacitor and (b) bootstrap capacitor functioning as floating supply [7].

Charge Pump Design

Although the bootstrap circuit functioned, it was limited due to the required cycling of the gate driver's output to recharge the floating supply capacitor, C_B. If the gate driver output remained 'on' for more than roughly 500 µs, C_B would discharge to the point that the output would fail. Due to this constraint, the minimum switching frequency of the gate driver was limited to 1 kHz for reliable operation. The charge pump removes the recharge cycle limitation by providing charge independent of the switching state of the gate driver [63]. This independence is accomplished by continually refreshing the charge on the floating supply capacitor, which provides a floating 5-V rail to the high-side circuitry. The basic schematic for the novel on-chip charge pump is shown in Figure 3.3.

The gate driver is designed to support output voltages up to 30V. To support these supply voltages, the charge pump switches are comprised of 45-V laterally diffused metal oxide semiconductor (LDMOS) devices. This enables the switches to tolerate the high V_{DS} voltages to which they are exposed while switching to and from the high-side and low-side of the circuit.

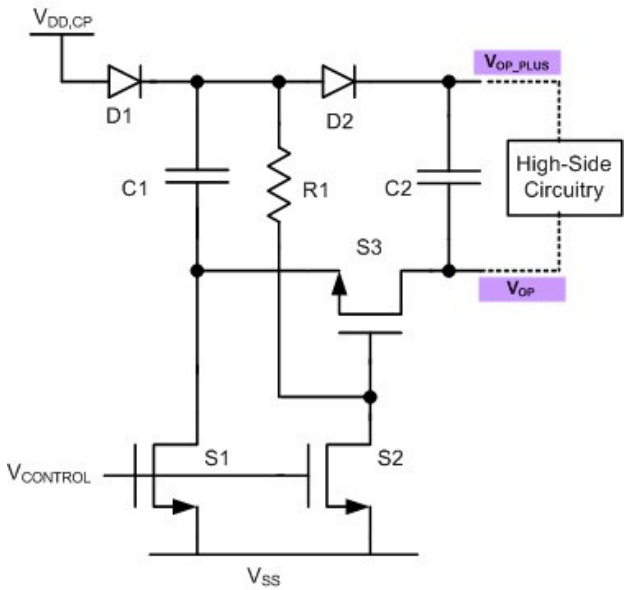


Figure 3.3. Basic charge pump topology.

Similarly, the diodes utilized in this design have a high reverse breakdown, 80 V. The on-chip boost and supply capacitors are accumulation mode metal-oxide-semiconductor capacitors (MOSCAPs). The MOSCAP structure was chosen because it has the highest capacitance per unit area of the capacitors available in the process technology used for this work, which facilitates their on-chip integration. Both capacitors are 1.5 nF, enabling their incorporation on-chip while being capable of storing sufficient charge to power the high-side circuitry during switching transients with this charge pump topology.

The control for the charge pump circuit is provided by a logic signal, $V_{CONTROL}$, which drives switches S1 and S2. The fundamental operation of the charge pump is as follows. When $V_{CONTROL}$ is high, switches S1 and S2 are 'on,' Figure 3.4. Switch S2 pulls the gate of switch S3 LOW, maintaining S3 it in an 'off' state. With S1 'on,' current flows from the supply through diode D1, charging the boost capacitor, C1. The maximum voltage on C1 is given by

$$V_{C1} = V_{DD_CP} - V_{D1} - V_{S1_ON}$$

where V_{DD_CP} is the supply voltage, V_{D1} is the voltage drop across diode D1, and V_{S1_ON} is the 'on'-state voltage drop (V_{DS}) across switch S1.

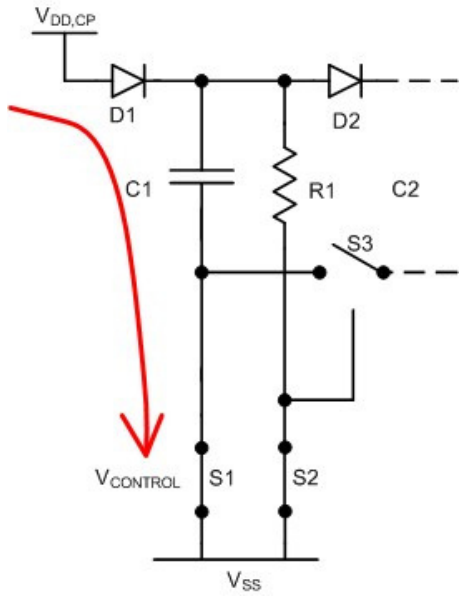


Figure 3.4. Charge pump with switches S1 and S2 closed.

When switches S1 and S2 are then turned 'off,' capacitor C1 begins to charge the gate of switch S3 through resistor R1, Figure 3.5. When enough charge has been placed on the gate of switch S3, it activates. With S3 'on,' capacitor C1 is connected to C2 through S3 and diode D2, and charge is exchanged, Figure 3.6. Diode D1 is reverse biased if the gate driver's output is HIGH, preventing current flow from the floating supply, V_{OP_PLUS}, back to the charge pump supply, V_{DD_CP}. The maximum voltage on capacitor C2, the floating supply, is given by

$$V_{C2} = V_{OP_PLUS} = V_{DD_CP} - V_{D1} - V_{D2} - V_{S1_ON} - V_{S3_ON}$$

where V_{D2} is the voltage drop across diode D2 and V_{S3_ON} is the 'on'-state drop across S3.

When switches S1 and S2 are reactivated, the gate of switch S3 is pulled LOW by switch S2 and turned 'off,' while capacitor C1 is again placed in charging mode, returning the circuit to the state depicted in Figure 3.4. Diode D2 is reverse biased if the gate driver's output is HIGH, preventing current flow from the supply capacitor, C2, back to the boost capacitor, C1, while it is in the charging configuration. With continuous cycling of the logic control signal $V_{CONTROL}$, charge is maintained on capacitor C2 and power is constantly available to the high-side circuitry of the gate driver. This allows for 100% high-side duty cycle operation. This process is also demonstrated in Figure 3.7.

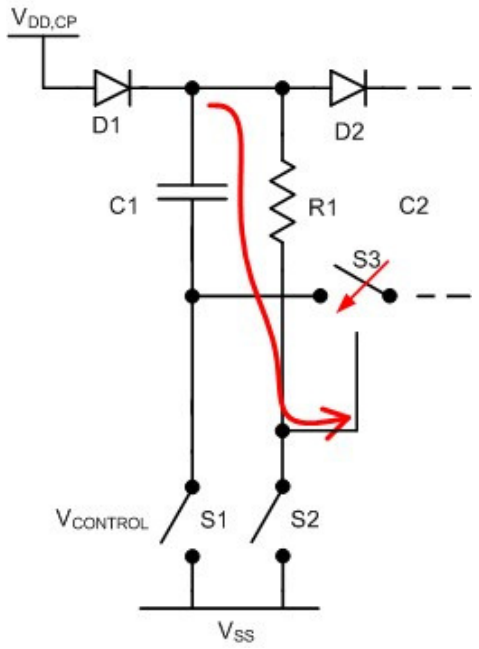


Figure 3.5. Charge pump with switches S1, S2, and S3 open.

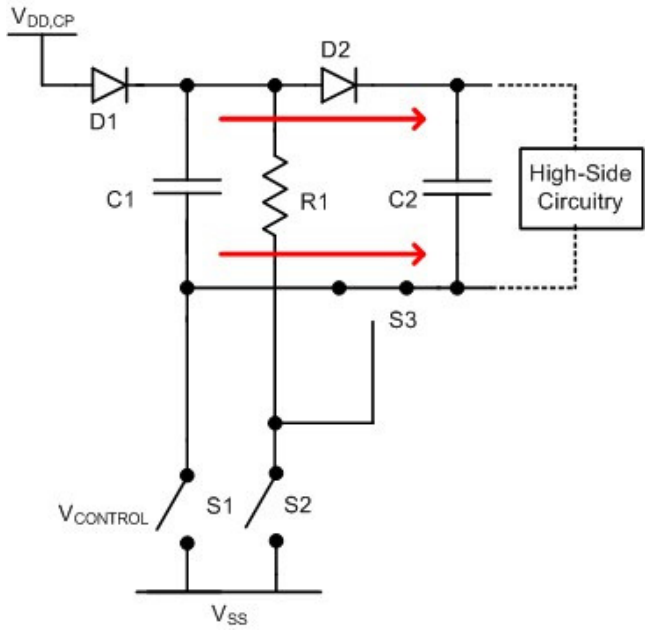


Figure 3.6. Charge pump with switches S1 and S2 open, S3 closed.

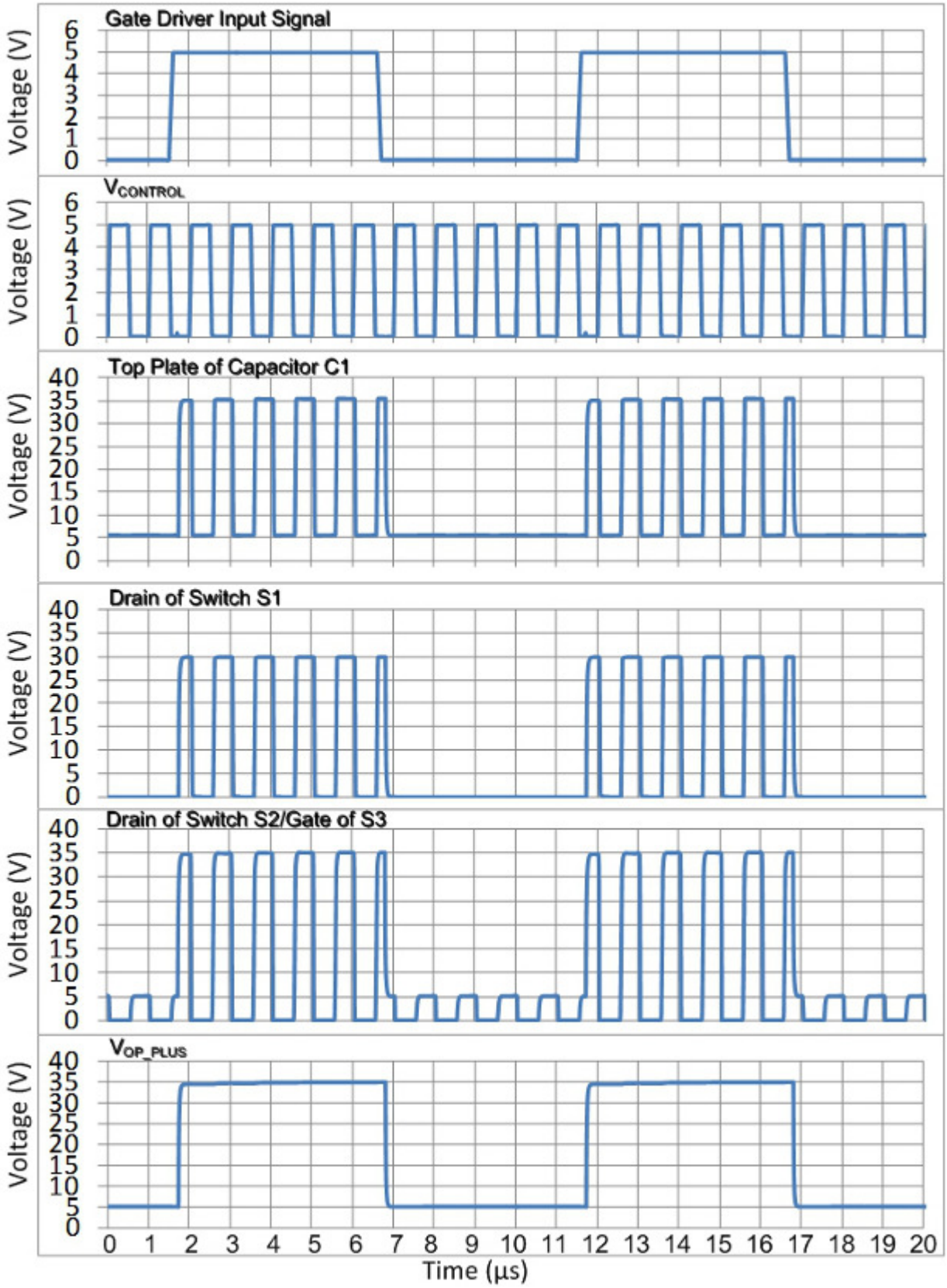


Figure 3.7. Charge pump operation.

Figure 3.7 demonstrates the operation of the charge pump with a 100 kHz input signal to the gate driver. $V_{CONTROL}$ is the 1 MHz control signal for the charge pump circuit. When $V_{CONTROL}$ is HIGH, the top plate of the boost capacitor, C1, stays approximately a diode drop above V_{DD} (charging mode). Also, the bottom plate of C1/drain terminal of S1 is pulled to V_{SS}. When $V_{CONTROL}$ is LOW, the bottom plate of C1/drain terminal of S1 are connected to V_{OP} through S3. This changes the reference node of V_{C1} from V_{SS} to V_{OP}, and the top plate of capacitor C1 is connected to V_{OP_PLUS} through diode D2.

The drain terminal of S2/gate terminal of S3 are pulled up to V_{C1} when $V_{CONTROL}$ is LOW. When $V_{CONTROL}$ is HIGH, this node is held at V_{SS}. With a 30-V V_{DDH}, V_{OP} switches from V_{SS} to 30 V. Therefore, the charge-pump output voltage, V_{OP_PLUS}, swings from approximately 5 V to 35 V to maintain a 5-V floating supply for the high side circuitry.

V_{DD_CP}, the power supply used to charge capacitor C1, is supplied by an on-chip voltage regulator designed to provide a complementary-to-absolute-temperature (CTAT) supply voltage of approximately 6.6 V to 6.1 V across 0°C to 200°C, Figure 3.8. This temperature characteristic offsets the forward voltage drop of diodes D1 and D2 taking into account the associated temperature coefficient, which dominates the voltage drop from V_{DD_CP} to V_{OP_PLUS}. This helps to facilitate the charge pump's generation of a temperature independent floating supply voltage of approximately 5 V, V_{OP_PLUS}.

At lower temperatures, with the increasing diode voltage drop (V_D), measures are needed to prevent excessive voltage from forming across the V_{GS} of switch S3. While switches S1 and S2

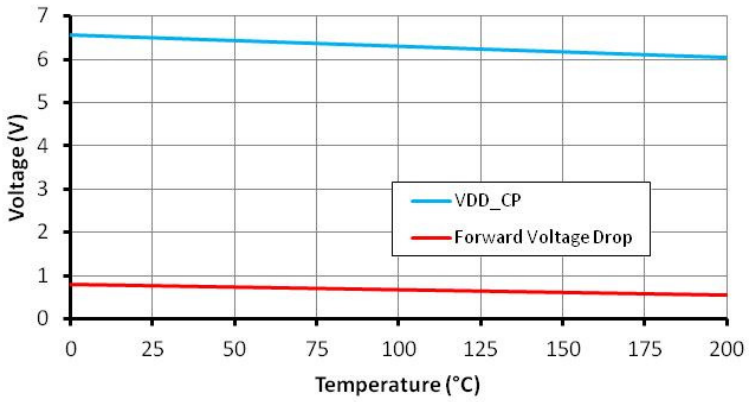


Figure 3.8. V_{DD_CP} and diode voltage drop.

are 'on' the gate and source terminals of S3 are pulled to V_{SS}. However, when S1 and S2 are 'off,' the V_{GS} of S3 approaches V_{DD_CP} minus the voltage drop across diode D1,

$$V_{GS_S3} = V_{C1} = V_{DD_CP} - V_{ON_S1} - V_{D1}.$$

At 25°C V_D is approximately 0.7-V, which will induce a V_{GS} of 5.7 V on switch S3, above the 5.5-V maximum V_{GS} for this process. To prevent this excessive V_{GS}, a clamping circuit, Figure 3.9, is placed across the gate and source of the switch. The current limiting resistor used in this circuit has a temperature coefficient opposite that of the diode's to offset the changes in V_D across temperature and maintain V_{GS} below 5.5 V.

The charge pump's control signal, $V_{CONTROL}$, is generated by a 1 MHz on-chip ring oscillator, Figure 3.10. In this design, the oscillation frequency is dominated by the size of the resistors and capacitors, as the charge/discharge rate of the capacitors determines the propagation delay before each inverter's input crosses its threshold voltage. The resistors R1, R2, and R3 are sized at 200 kΩ and the corresponding capacitors are 1.35 pF. This circuit provides a tolerance of +/– 20% across temperature for the 1 MHz clock, which is well within the operational range of the charge pump.

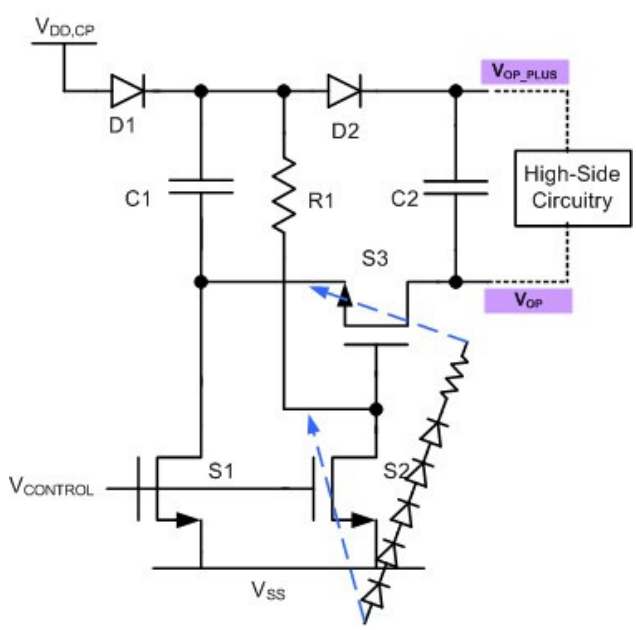


Figure 3.9. Clamping circuit.

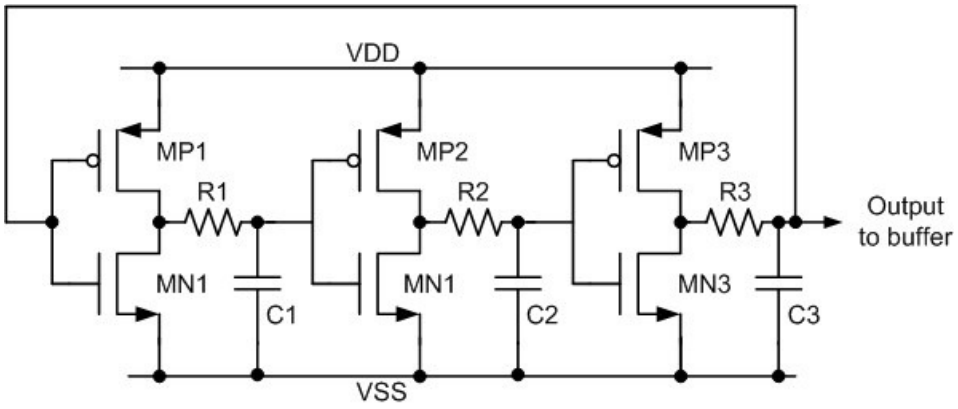


Figure 3.10. Ring oscillator.

Charge Pump Simulations

The following simulations demonstrate the output of the charge pump (V_{OP_PLUS}) providing a floating supply to the full gate driver core high-side circuitry across temperature and at different operating frequencies. For these simulations, a worst-case gate driver supply voltage, V_{DDH}, of 30 V is used. Figure 3.11 demonstrates V_{OP_PLUS} while the gate driving is switching at 10 kHz. The floating supply remains stable at approximately 5 V, providing a 5 V to 35 V supply to the high-side circuitry for LOW and HIGH gate driver outputs. Simulations at 0°C, 100°C, and 200°C are overlaid in the figure and there is no appreciable change over temperature.

Figure 3.12 displays V_{OP_PLUS} for the gate driver switching at 100 kHz. Again, the floating supply rail remains stable across temperature, providing 5 V to the high-side circuitry. Figure 3.13 demonstrates the charge pump providing a stable floating supply when the gate driver output remains high (e.g., a 100% high-side (DC) duty cycle). This is accomplished with a fully integrated charge pump that requires no external control signals or passive components.

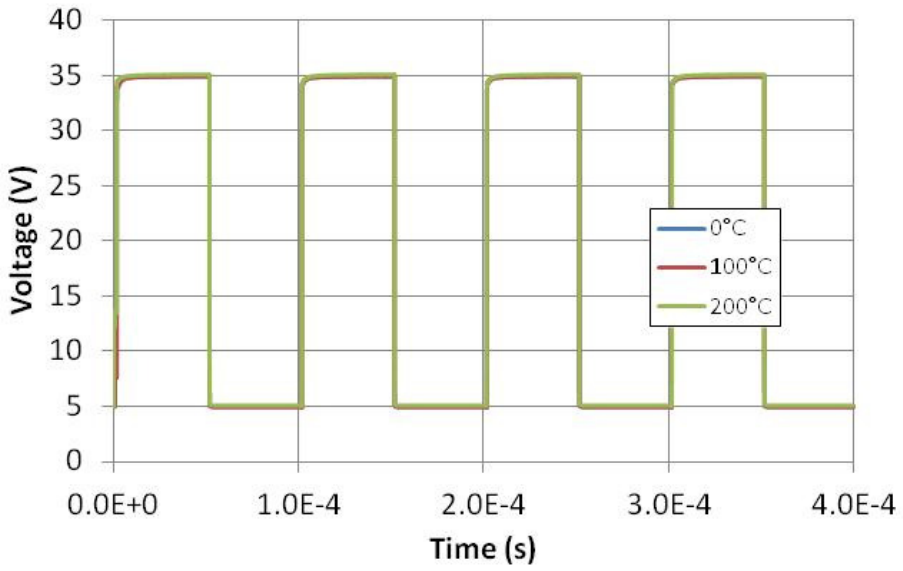


Figure 3.11. V_{OP_PLUS} across temperature with a 10 kHz gate driver input signal and V_{DDH} set to 30 V.

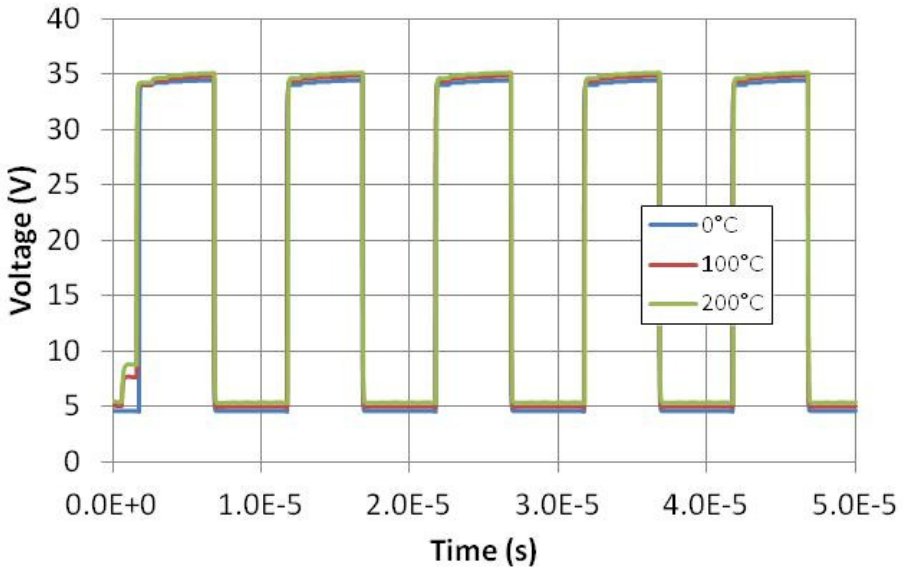


Figure 3.12. V_{OP_PLUS} across temperature with a 100 kHz gate driver input signal and V_{DDH} set to 30 V.

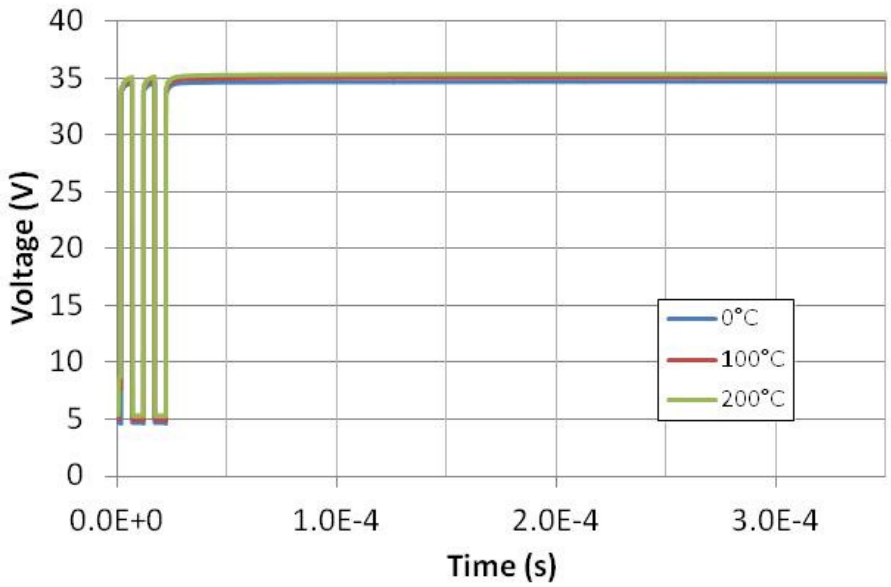


Figure 3.13. V_{OP_PLUS} across temperature with a DC gate driver input signal and V_{DDH} set to 30 V.

High-Voltage Output Stage and Current Drive

The output stage of the gate driver connects to the gate of a wide-bandgap power transistor, Figure 3.14. Through the half-bridge output stage of the gate driver, the gate of the power device is connected to either the V_{DDH} or V_{SSH} supply rails, which are set depending on the drive requirements of the power device (up to 30 $V_{peak\text{-}to\text{-}peak}$). In a CMOS process (such as the process used for this work), there are two common output stage circuit arrangements. In the first configuration, an NMOS transistor is used for the low-side switch and a positive-channel metal oxide semiconductor (PMOS) transistor is used for the high-side switch. This configuration is, in principle, similar to a logic level inverter. The second configuration is an NMOS only stage that uses n-channel devices for both the high- and low-side transistors.

The chief design considerations for this output stage are the drain to source 'on' resistance (R_{DS_ON}), switching speed, and the die area requirements [64]. For a given device size, an NMOS transistors has higher switching speeds and lower R_{DS_ON} when compared to a similarly sized PMOS device. Additionally, a PMOS device would require approximately 2-3 times the

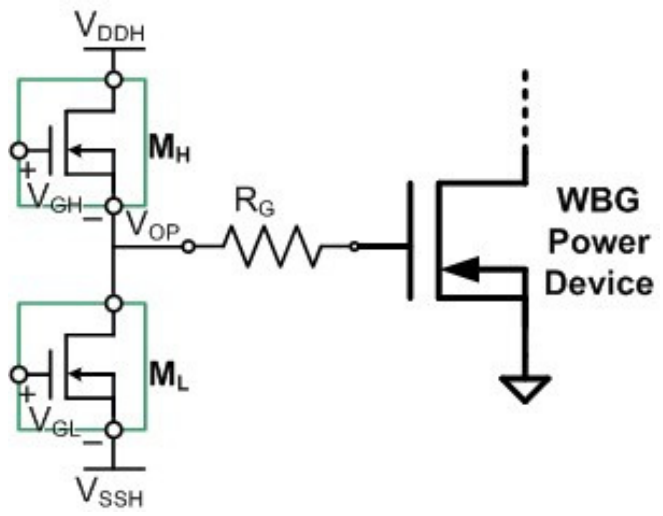


Figure 3.14. High-voltage half-bridge output stage.

die area required by an NMOS device in order to exhibit a comparable drain current, which is due to PMOS devices having a lower electron surface and bulk mobility. Therefore, utilizing PMOS devices would more than double the space required for the output drivers.

The current drive specifications for this gate driver circuit are high for a device with an integrated output stage (> 3 A at 200°C). This necessitates large output drivers and extensive metal routing, which will result in a substantial on-chip footprint. Due to the larger area, lower speed, and higher R_{DS_ON} of a PMOS device, an all-NMOS based half-bridge "totem-pole" topology was chosen for the gate driver IC.

For the 30 $V_{peak\text{-}to\text{-}peak}$ output voltage swing specification of this gate driver, the devices in the output stage must be compatible with these relatively high voltage levels. The BCD-on-SOI process utilized for this work has FET devices available with 45-V V_{DS} ratings, which is sufficiently above the desired output voltage specification. The all-NMOS topology used for the output stage of the gate driver, Figure 3.14, consists of two large arrays of these high-voltage (45-V) n-channel LDMOS transistors. The gate voltage on the lower NMOS device, M_L, is either V_{SSH} ('off') or V_{DD} ('on'). The gate voltage of the top NMOS device, M_H, is either set at V_{SSH}, in which case it is 'off,' or at V_{OP_PLUS}, in which case M_H is 'on.' As discussed previously, the dead-time controller generates two non-overlapping, complementary signals from the

buffered input signal. This ensures that the M_L and M_H are not 'on' at the same time, preventing shoot-through current in the totem-pole output stage.

In the previous gate driver implementation (3G), the output driver stage was designed to provide approximately 3 A drive current to a 10 nF load at 200°C. However, measurement results from the 3G prototype did not demonstrate the desired drive current. Figure 3.15 and Figure 3.16 show the sourcing and sinking current, respectively, of the 3G gate driver across temperature [7].

As the 3G prototype gate driver did not achieve the output current drive predicted by simulations and individual device characteristics, the 4G gate drive is meant to address these limitations. Possible sources of the lower current drive are postulated to be related to (1) self-heating of the output drivers, (2) on-chip resistance and parasitics, and (3) off-chip parasitics. To address the first issue of potential self-heating, the device arrays were altered and heat pipes added to the layout design.

In the 3G output stage design, Figure 3.17, the layout was constructed to be as tightly packed as possible, with the structure of one device overlapping onto the next. For reference, a single LDMOS device, arrays of which make up the output drivers, is shown in Figure 3.18. In the *Corinth* design, the devices are separated and traces on the lowest level metal, metal 1 (M1), were routed between and around the devices and connected to the silicon substrate through

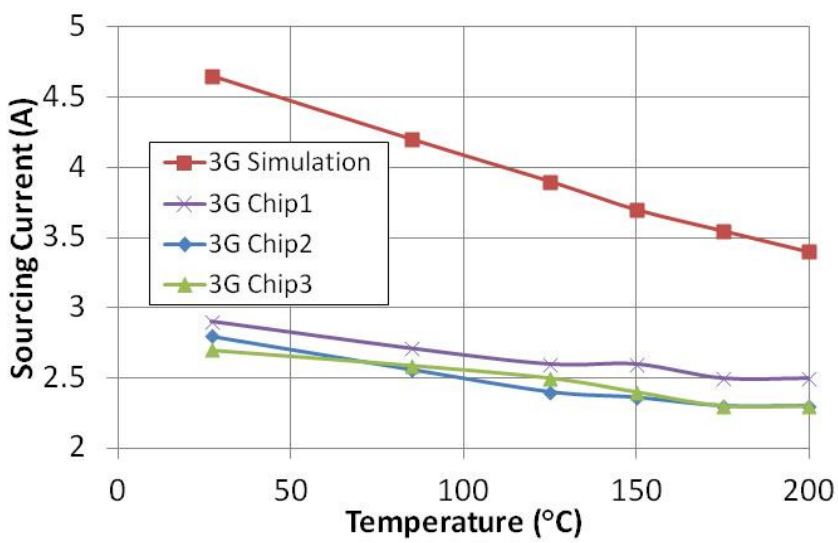


Figure 3.15. 3G sourcing current, simulation vs. measurement.

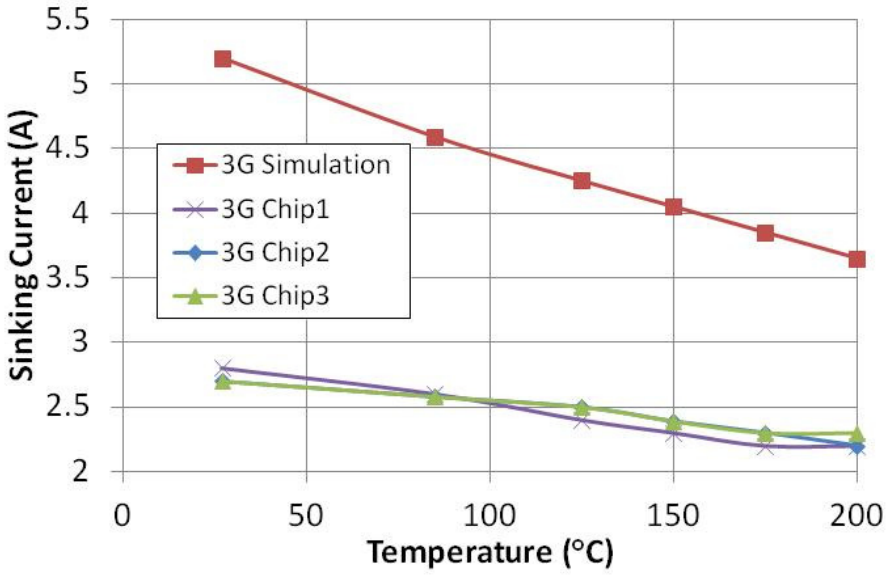
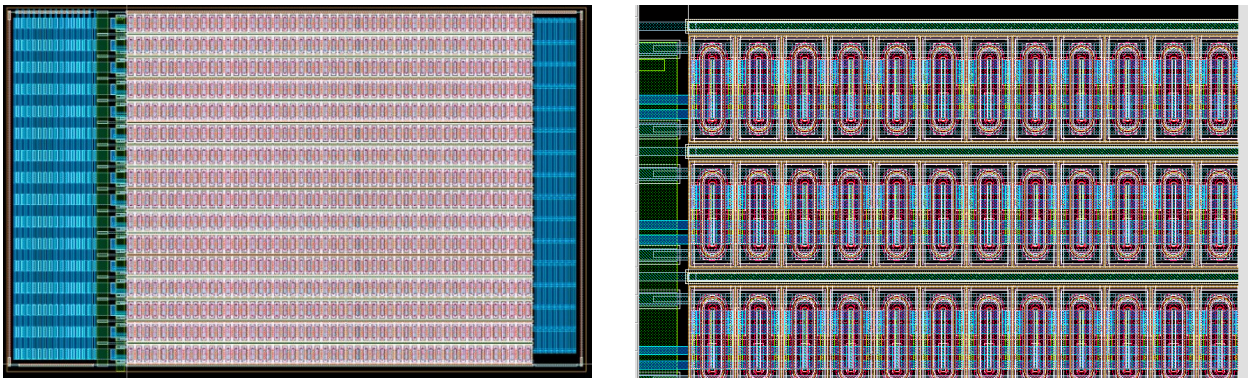


Figure 3.16. 3G sinking current, simulation vs. measurement.



(a) (b)

Figure 3.17. 3G output drivers: (a) output driver array and (b) close-up of parallel devices.

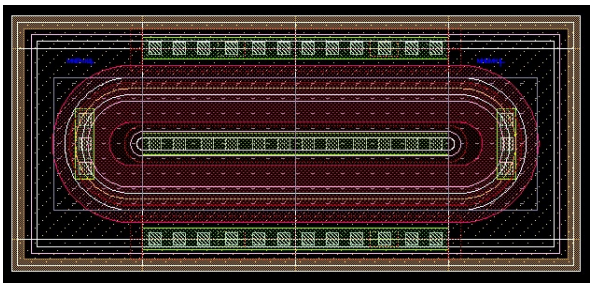


Figure 3.18. 45-V n-type LDMOS device utilized in output drivers.

substrate contacts. These metal 1 'heat pipes' were then connected to a lattice of M1 routing. This lattice is then routed off-chip through a series of parallel bonding pads to pins that can be connected to a board-level ground plane to assist in dissipating any heat collected.

Figure 3.19 shows the 4G output driver layout configuration. The devices are spread apart with M1 'heat pipe' routing (green bands in the layout) encircling each device. This routing is connected to six nearby bonding pads to facilitate routing off-chip.

In order to address the second issue of on-chip resistance and parasitics, two solutions were implemented. The first was to increase the size of the output drive transistors, which brought the equivalent width of each device to 40000 µm, with 1000 devices in each output driver array. This was accomplished within the space allotted and decreased the 'on'-resistance while increasing the current drive of the output stage. Additionally, larger metal traces were used for routing V_{SSH}, V_{DDH}, and V_{OP} off-chip, all on metal 3 (M3). In the SOI process employed for this work, M3 is a thicker routing metal and has lower resistance and higher current density than the other metal layers available. This helped to lower the resistance related to the on-chip routing and reduce the effects of electromigration [65]. Additionally, three bonding pads were utilized for each of the three signals to further reduce resistance. To reduce capacitance, there was only minimal routing of metal beneath the M3 signal routing. A comparison of the 3G and 4G routing are shown in Figure 3.20 and Figure 3.21, respectively.

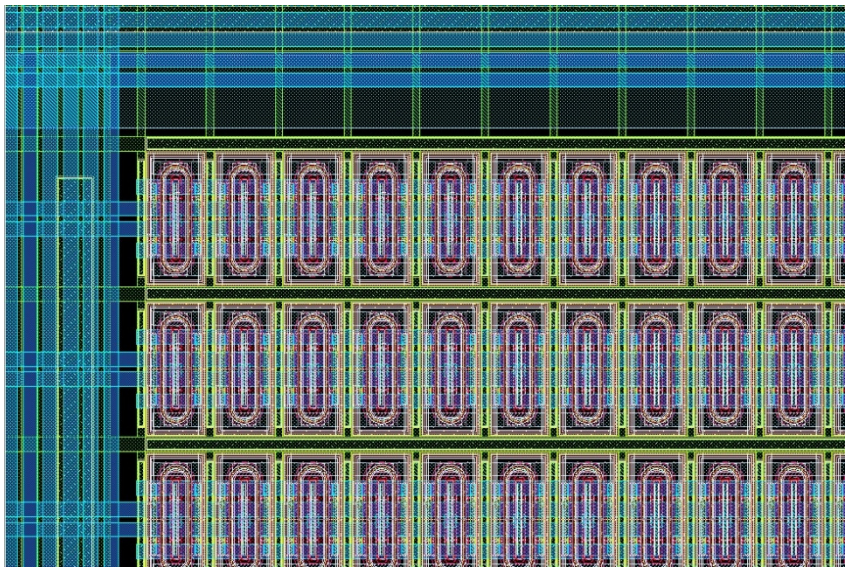


Figure 3.19. 4G output driver device spacing and M1 routing.

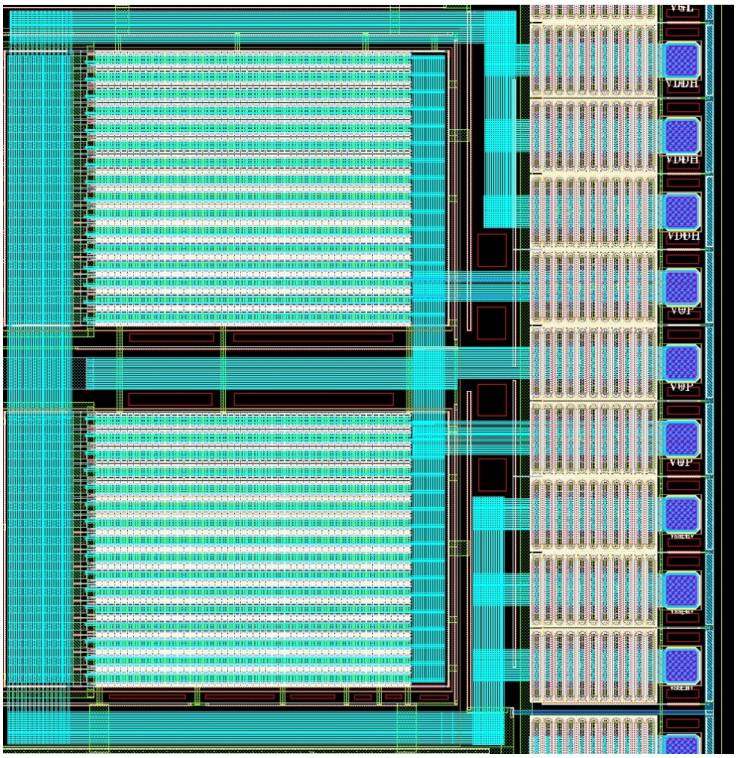


Figure 3.20. 3G output drivers with routing.

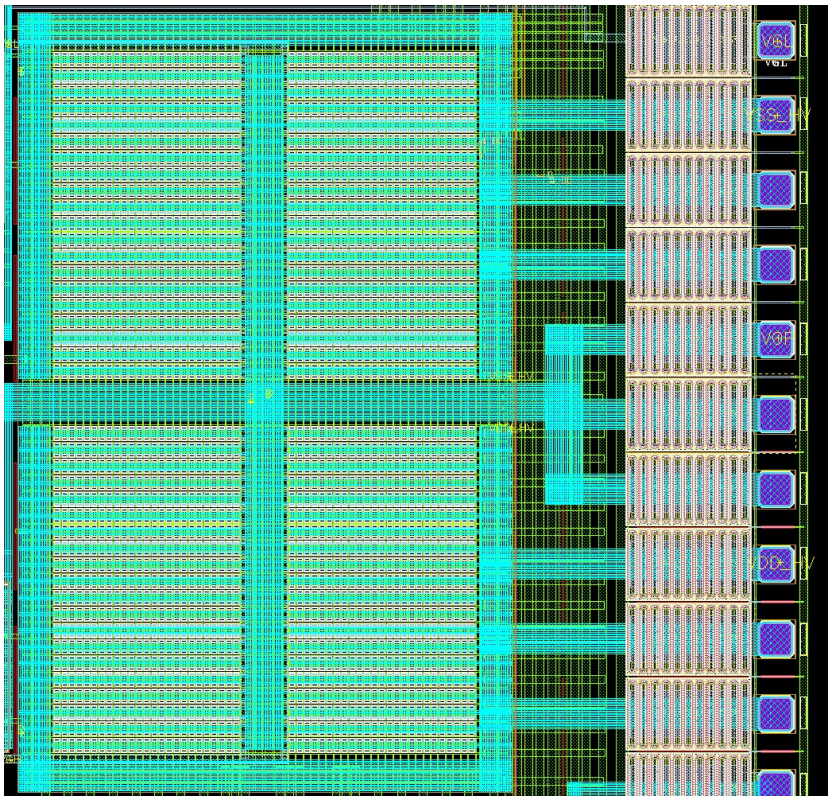


Figure 3.21. 4G output drivers with routing.

To attempt to address the final issue of off-chip parasitics, the 3G test configuration was examined. The 144 pin PGA package used with the 3G gate driver is shown in Figure 3.22. Note the long wire bonds, some up to 15 mm, connecting the gate driver signals to the package. Typical parasitics values for wire bonds are 20 fF/mm capacitance and 1 nH/mm inductance. These parasitics, added to the potential parasitics introduced by the package, represent a potentially substantial source for the reduction in peak output current [66][67].

The 3G test board is shown in Figure 3.23. A major source of parasitics from this board included the PGA socket and the routing and wires to the gate of the power switch. The power switch could not be placed on the printed circuit board (PCB) board due the temperature limitations of its package. Therefore, for temperature testing, the board was placed in a temperature chamber, while the power switch was located outside the temperature chamber, Figure 3.24.

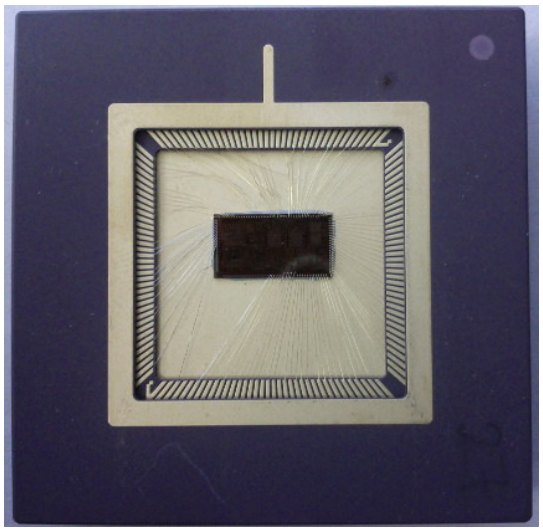


Figure 3.22. 3G packaging [7].

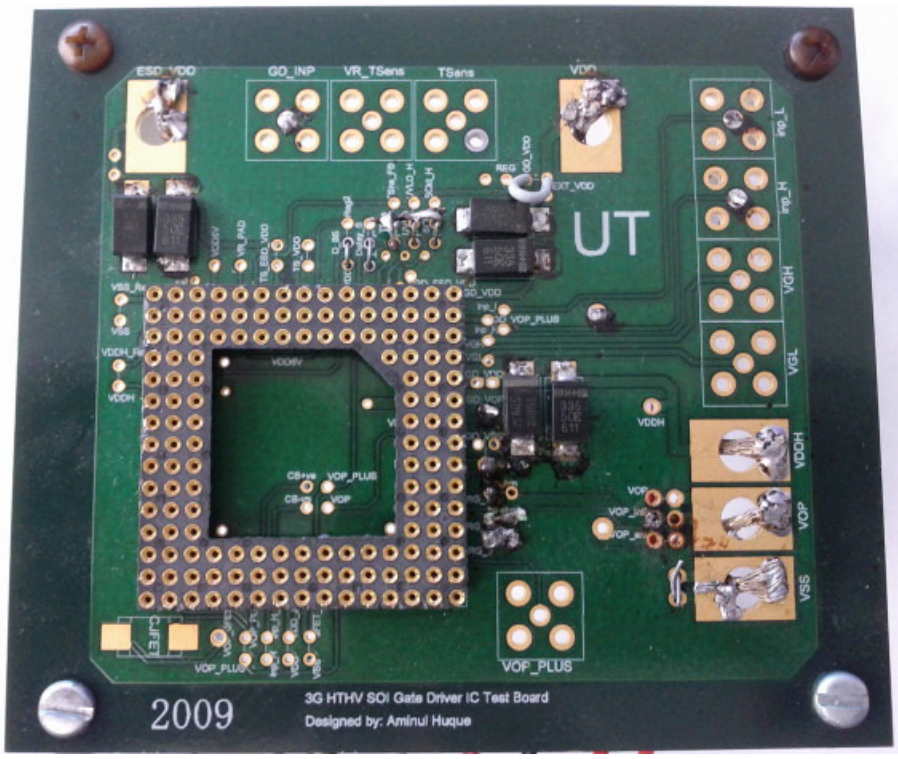


Figure 3.23. 3G test board [7].

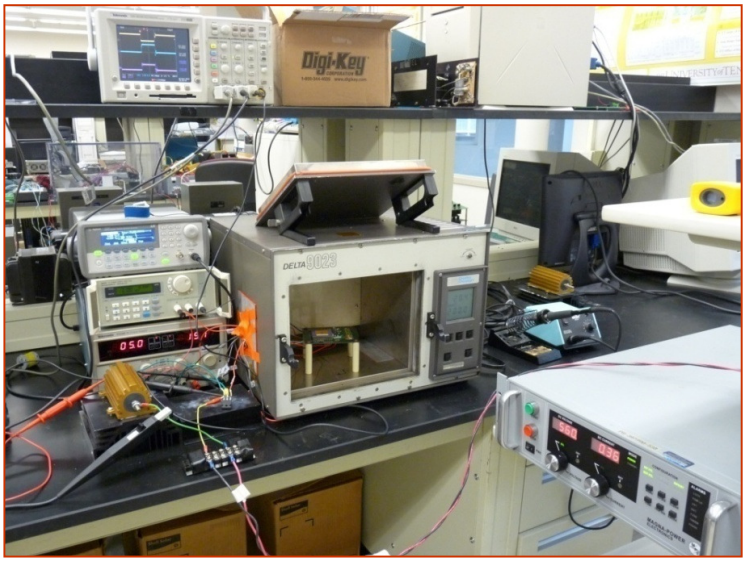


Figure 3.24. 3G measurement setup [7].

Two approaches were used to limit these parasitics. The first approach to overcome these limitations was a tape heater system (also referred to as a foil or film heater), Figure 3.25, which used a tape heater that directly contacted the chip package, heating to temperature only the gate driver die and its package. This scheme can reduce or remove the need for high-temperature (200°C) compatible on-board components and simplify the testing procedure by allowing for shorter wiring between the test board and equipment, test leads, and the power device. The shorter leads and wires lessen off-chip parasitics. The heater and resistance temperature detector (RTD), a temperature sensor, are held in place with an insulating Macor block, a type of machinable ceramic marketed by Corning Inc., which attaches to the board and holds the heater and sensor in place. The overhead for this configuration on the test board was 4 holes to hold the Macor blocks in place and a slot cut in the test board directly under the package for the temperature sensor or tape heater to make contact.

The second approach was a chip-on-board test configuration, for which a mockup is shown in Figure 3.26. Instead of utilizing a die bonded to a package and mating the package to the PCB through a socket, a chip-on-board approach directly bonds the die, in this case a gate driver die, to the PCB test board. This implementation shortens the bond wires, removes the chip package

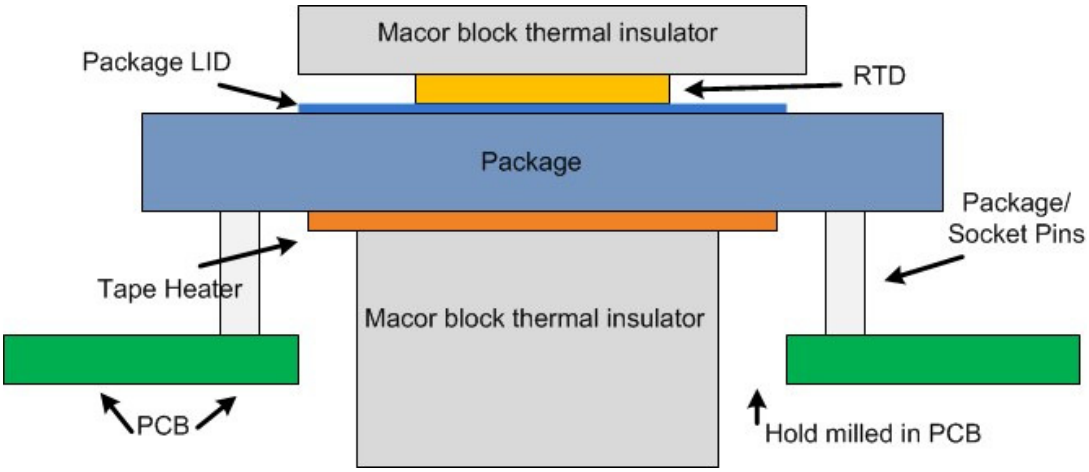


Figure 3.25. Tape heater configuration.

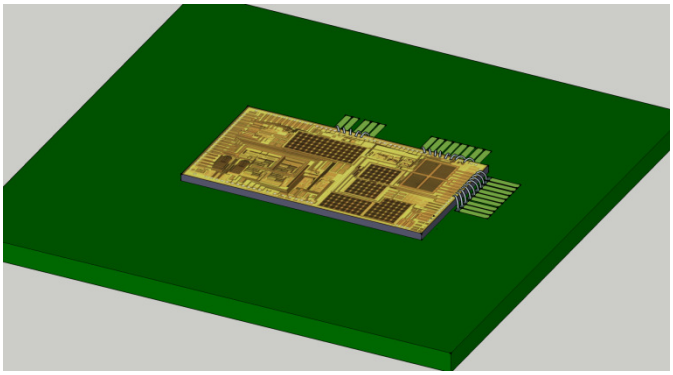


Figure 3.26. Conceptual rendering of chip-on-board with gate driver die.

and socket, and could have a large impact on parasitic reduction. Some key estimated off-chip parasitics are given in Table 3.1.

Figure 3.27 displays 3G vs. 4G output current simulations across temperature. The increase in current across temperature for the 4G driver in these simulations can be attributed to larger output drivers, less-resistive metal traces, and lower on-chip parasitics. Additional increases in the measured current for the 4G gate driver were expected to come from lower off-chip parasitic loading and the improved heat dissipation of the output drivers.

IC Integration

A color coded-block diagram of the 4G gate driver, *Corinth*, is given in Figure 3.28. Components that were left functionally unchanged but received updated layout are shown in brown. Updated or revised circuit blocks are shown in blue. New circuits blocks are indicated in green.

Goals for the integration of the 4G gate driver IC are a minimum number of passive off-chip components and no active off-chip components. The exception to this design rule are sense resistors such as those used in the resistor-sensing short-circuit protection. These passives must be capable of carrying a high current load and are selected by the user for the particular application [69]. As these resistor sizes are not fixed, it would not be feasible or advantageous to incorporate them on-chip.

Table 3.1. Estimated off-chip parasitics [67][68].

Circuit Block	Inductance
Bond wires	7-15 nH per bond wire
Package	16-22 nH
Board routing	10-20 nH
Off-board wiring	100 nH

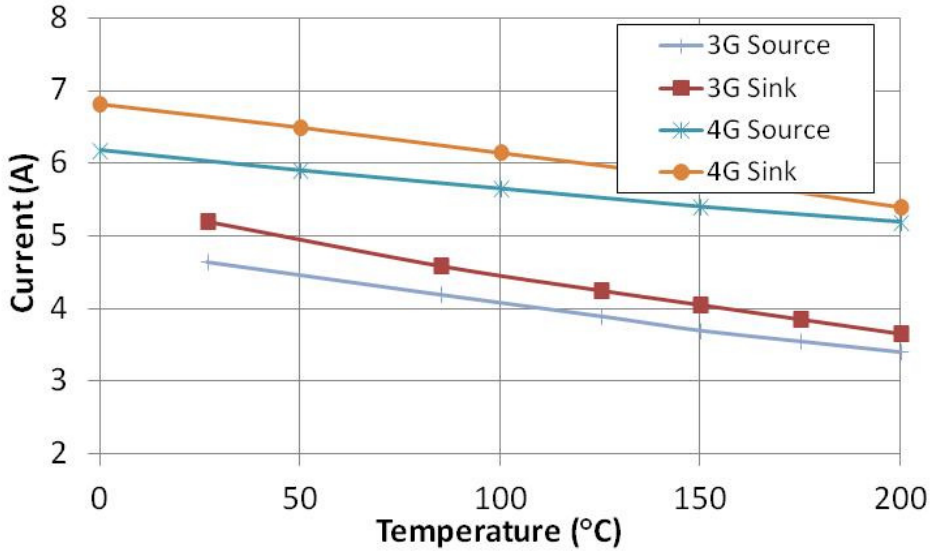


Figure 3.27. 3G vs. 4G sourcing and sinking current simulations (10 nF load).

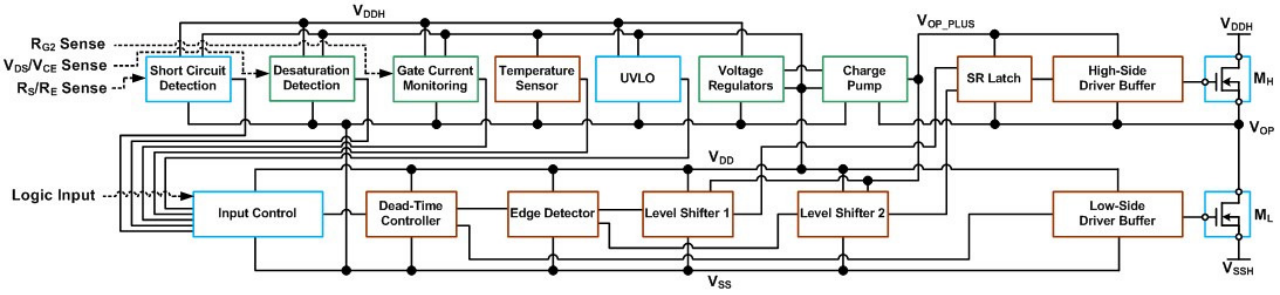


Figure 3.28. Color-coded *Corinth* gate driver block diagram.

The largest passive components on the gate driver IC are the charge pump and voltage regulator capacitors, as seen in Figure 3.29. The two on-chip voltage regulators each require a load capacitor. The 5-V regulator requires a 3.9 nF capacitor and the charge-pump regulator requires a 1 nF capacitor that must be 7-V tolerant. Since the MOSCAP has a maximum top plate to bottom plate voltage rating of 5.5-V it must be constructed by placing two capacitors in series, requiring two 2 nF capacitors.

The charge pump requires two 1.5 nF capacitors, one for the boost capacitor (C1) and the other for the floating supply capacitor (C2), Figure 3.3. These capacitors are constructed of arrays of 50 pF unit capacitors to allow for the best utilization of space, permit for optimal interconnect to the capacitor terminals, and meet the processes design rule check (DRC) rules. An image of the integrated layout with on-chip capacitors is shown in Figure 3.29.

The approximate die area requirements for the components incorporated on the gate drive IC are presented in Table 3.2. As shown in Figure 3.29 and Table 3.2, the largest components of the IC are the output drivers, on-chip capacitors, and protection circuitry blocks.

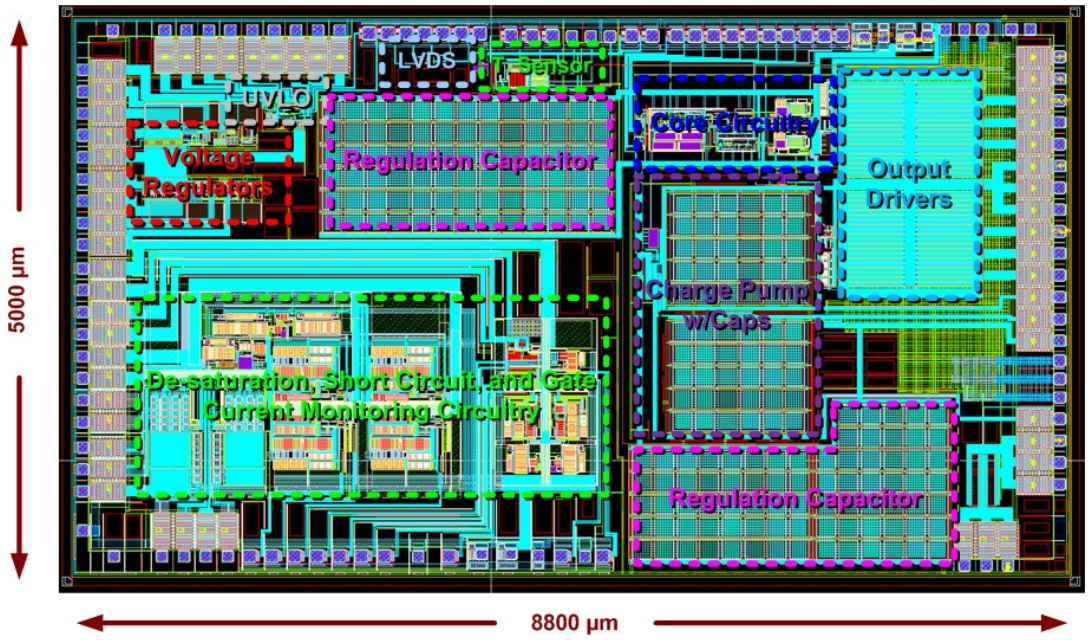


Figure 3.29. *Corinth* gate driver integration.

Table 3.2. Chip area of components.

Circuit Block	Chip Area
Core circuitry	1700 x 600 μm^2
Charge pump	260 x 900 μm^2
Charge pump caps	1200 x 2200 μm^2
Output drivers and routing	1950 x 1250 μm^2
Regulator capacitor 1	2600 x 1230 μm^2
Regulator capacitor 2	2800 x 1200 μm^2
On-chip R_G	550 x 300 μm^2
Temperature sensor	550 x 300 μm^2
Oscillator	140 x 150 μm^2
LVDS	150 x 100 μm^2
Voltage regulators	1150 x 1200 μm^2
UVLO	400 x 200 μm^2
De-saturation, short-circuit, and gate current monitoring circuitry (integrated)	4000 x 2000 μm^2
Padframe	approximately 23200 x 500 μm^2

Free space was minimized on the *Corinth* IC in order to place the maximum number of circuit blocks on the IC while minimizing die size. However, this can lead to complications when the chip's fill requirements are taken into account. Any unused chip area is utilized to meet these process fill requirements, which require a minimum percentage of the chip area to be covered by each level of metal (M1, M2, and M3), diffusion (RX), and trench, among other layers. An example of this fill around a circuit block is shown in Figure 3.30.

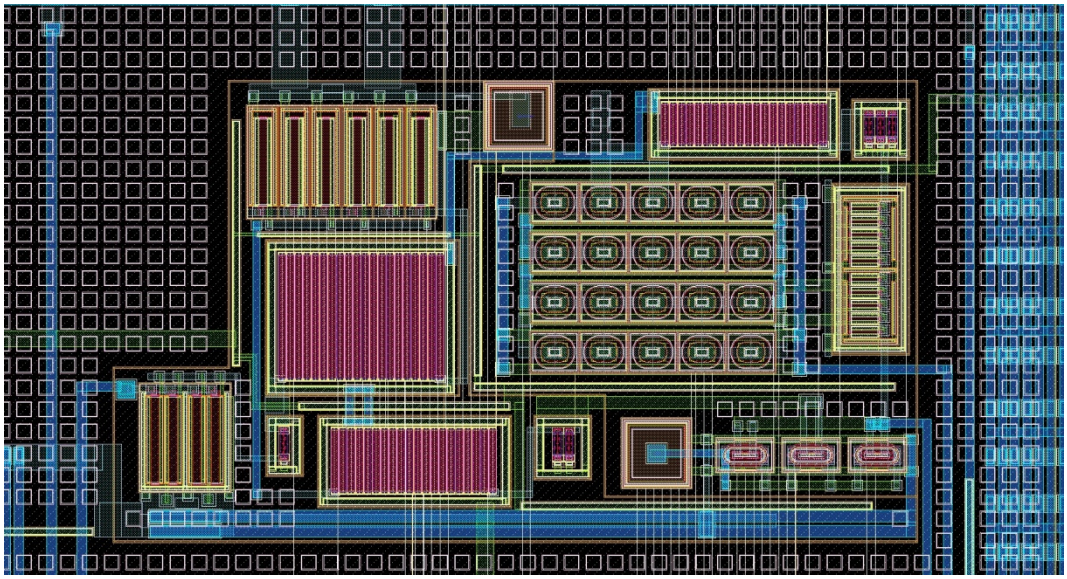


Figure 3.30. *Corinth* fill example.

CHAPTER 4

Fabrication, Gate Driver Die, and Packaging

The high-temperature gate driver integrated circuit presented in this document was fabricated on a Bipolar-CMOS-DMOS (BCD) on silicon-on-insulator (BCD-on-SOI) 0.8-micron, 2-poly, 3-metal process that combines the advantages of high-voltage LDMOS devices with SOI technology. It utilized a 6" SOI wafer and provides approximately 140 9.9 mm x 9.9 mm reticles. Each reticle was identical, containing chip layout and process monitoring (PM) bars. An image of the 4G gate driver wafer is shown in Figure 4.1.

The 4G reticle, Figure 4.2, contained three chips. Chip 1 (*Corinth*) is the primary gate driver chip and is the primary component discussed here, containing the gate driver core, voltage regulators, protection circuitry, and ring oscillator, among other related components. Chip 2 contains test components and circuits including an open-base bipolar junction transistor (BJT) photodetector array, two prototype transformers, modulation and demodulation circuitry, and several oscillators. Chip 3b contains test structures derived from circuits on Chip 1, among them the gate driver output drivers, various components from the charge pump (including capacitors), and a voltage regulator with internal signals accessible.

Post-fabrication, the wafers were diced (sawed) to separate the reticles and, ultimately, to separate and bin (or sort) the individual die (Chip 1, Chip 2, and Chip 3b). The micrograph of a diced *Corinth* (Chip 1) die is shown in Figure 4.3 and an annotated image can be found in the Appendix, Figure A.1. Micrographs of Chip 2 and Chip3b are also located in the Appendix, Figure A.2 and Figure A.3, respectively. After dicing, chips that would be tested were packaged, in this case within 40 or 48 pin DIPs. An image of Chip 1 in a 48-pin DIP is presented in Figure 4.4. Note the bond wires connecting the die to the package which, along with the metal routing within the package and the package socket used to mate the DIP to the test board, add parasitic elements to the test configurations, as discussed in the previous chapter.

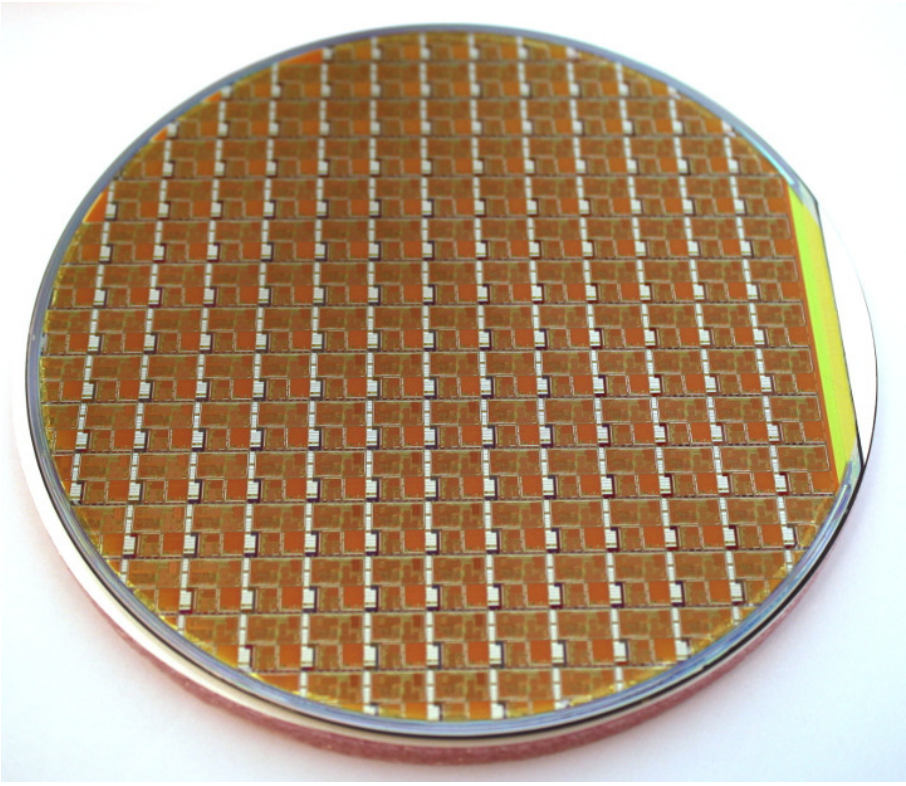


Figure 4.1. 4G 6” wafer image.

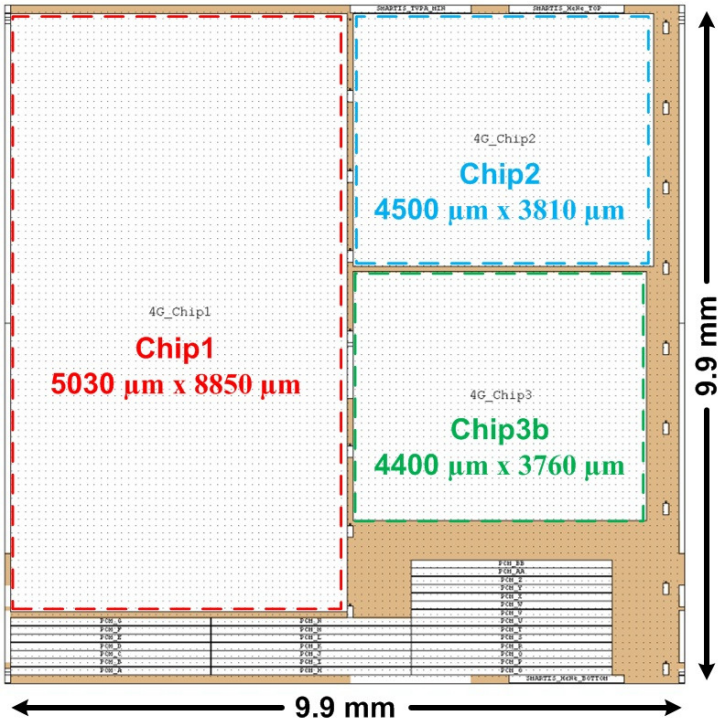


Figure 4.2. Reticle layout.

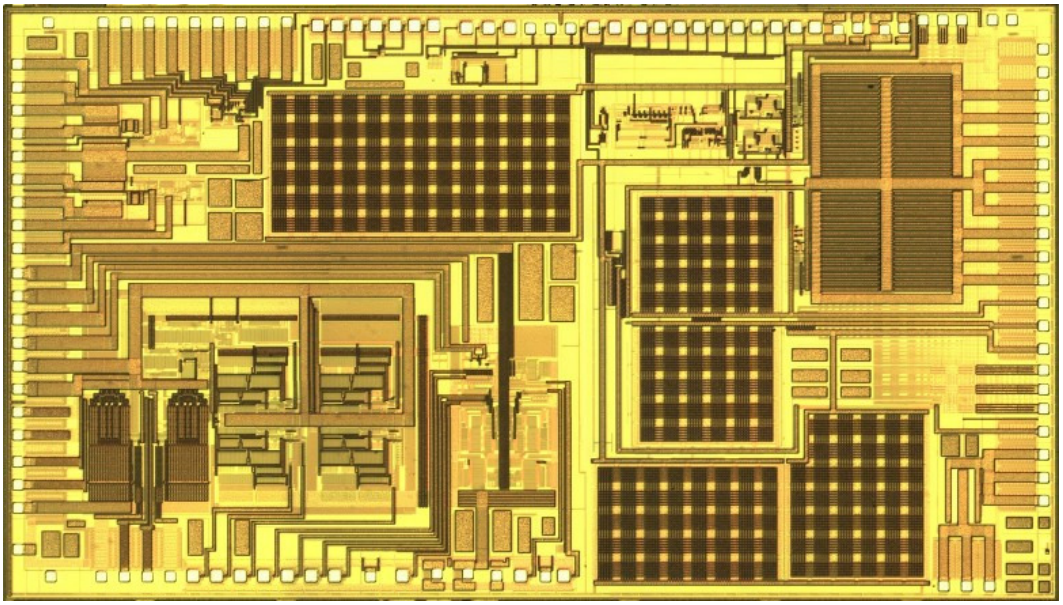


Figure 4.3. *Corinth* (Chip 1) micrograph.

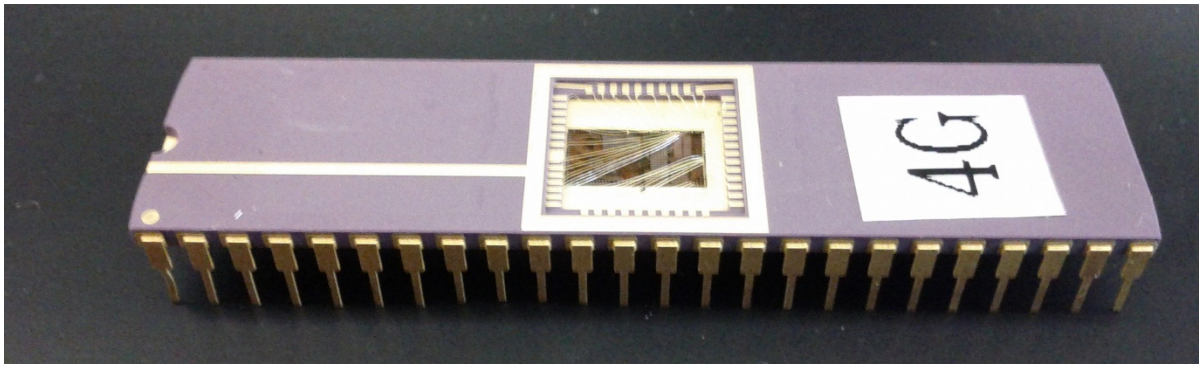


Figure 4.4. *Corinth* in a 48-pin dual inline package.

Test Plan

The test plan for the gate driver included numerous measurements taken of the gate driver integrated circuit and its components under different operating conditions. Characterization of the charge pump that enables 100% high-side duty cycle operation of the driver included measurements of the floating output voltage, V_{OP_PLUS}, across temperature. The charge pump testing also consisted of characterization of the charge pump's supply voltage, V_{DD_CP}. As the values of the on-chip capacitors are important to the functionality of not only the charge pump but the voltage regulators and other circuitry, measurements of capacitor values and their variation across temperature were also documented. Based on the test results, design recommendations for future work are suggested.

Also related to the charge pump is the ring oscillator circuit which provides the clock signal that controls the charge cycling of the circuit. Its oscillation frequency across temperature, nominally 1 MHz, was characterized. The data recorded for the output frequency of the ring oscillator versus temperature was also used to calibrate the tape heater testing configuration. Additionally, characterization of the charge pump operating with different control signal frequencies was also conducted.

The gate driver core testing included characterization of the output current drive and operating frequency across temperature. This also consisted of testing with model capacitive loads and with silicon and silicon carbide power switches, including MOSFETs, JFETs, and BJTs.

Reliability or lifetime testing was also conducted on the gate drive IC. For these tests, the gate driver was heated to 200°C and left operating for at least 336 hours or until catastrophic failure occurred. If the device did not fail during this test, the temperature was increased 25°C and the testing repeated. The tape heater configuration was not usable for reliability testing due to the limited lifetime of the tape heaters. Therefore, the temperature chamber was used. Table 4.1 summarizes the testing described in this section.

Table 4.1. Gate driver test plan.

	Measurement Description	Temperature	Notes
Charge Pump	V_{OP_PLUS} (floating rail) measurements across temperature	25°C to ≥ 200°C	
	Characterization of appropriate V_{DD_CP} across temperature	25°C to ≥ 200°C	V_{DD_CP} offsets the diode voltage drops
	Characterize on-chip capacitor values across temperature	25°C to ≥ 200°C	Charge pump capacitor
	Operating frequency	25°C to ≥ 200°C	
Ring Oscillator	Characterize oscillating frequency of clock generator across temperature	25°C to ≥ 200°C	Nominally 1 MHz
Gate Driver Core	Operating frequency range across temperature	−55°C to ≥ 200°C	
	Output current across temperature	−55°C to ≥ 200°C	
Gate Driver with Power Devices	BJT	25°C to ≥ 200°C	
	MOSFET	25°C to ≥ 200°C	
	JFET	25°C to ≥ 200°C	
Gate Driver Reliability Testing	200°C ambient temperature under load, until failure or > 336 hours	200°C	
	If there was no failure on previous reliability test, increase temperature to 225°C and continue	225°C	

Test Configurations

In order to facilitate testing, several PCBs were designed to connect on-chip circuits, provide access to test signals, and allow for the addition of components, such as loads, to the test configuration. An image of the primary gate driver test board is shown in Figure 4.5. Other test boards were used in the course of the gate driver testing and they will be discussed later in this section.

Two methods were used to take measurements of the gate driver integrated circuit and its components across temperature. One method was to utilize a temperature chamber, or oven, as shown in Figure 4.6. Using this method, the entire PCB, including the gate driver and components, was heated to the desired ambient temperature. The temperature chamber also has the advantage of being capable of cooling the system to below room temperature using liquid nitrogen (LN_2). However, some components, such as load capacitors and power switches, were not able to operate reliably across the temperature extremes experienced in the gate driver testing (−55°C to > 200°C). Additionally, some measurement devices, such as Hall Effect current probes, must be kept outside the chamber and require wiring be brought out to provide an interface. This necessitated long cabling and test leads extending outside the oven, adding complexity and parasitics to the test configuration, as discussed in Chapter 3.

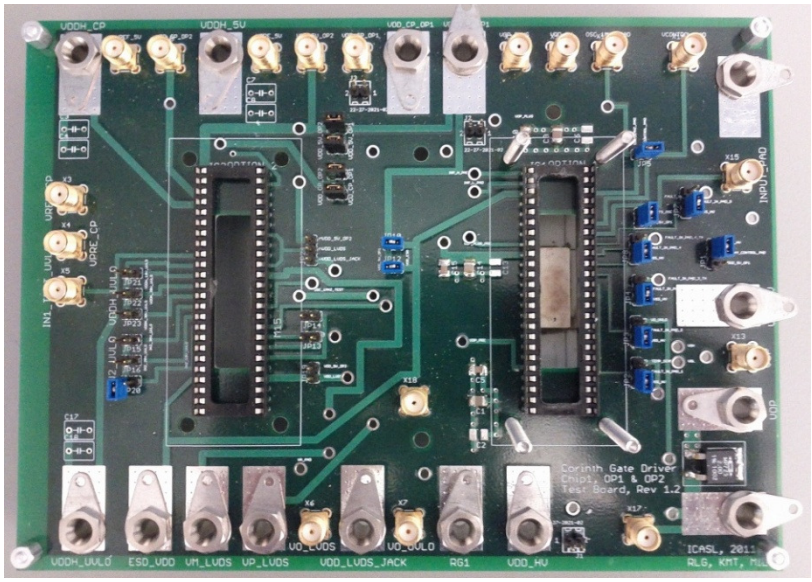


Figure 4.5. 4G *Corinth* printed circuit board ver. 1.2.

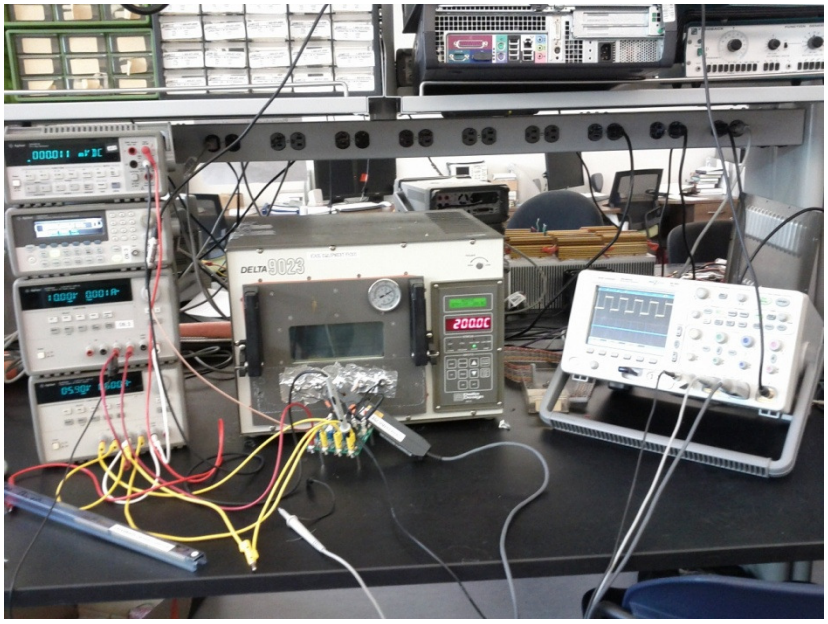


Figure 4.6. Measurement system using temperature chamber.

The second method that was used for temperature measurements was a tape heater system, as described in Figure 3.25. The components for this system are shown in Figure 4.7. In this configuration, a film heater directly contacts the chip package, heating to temperature only the gate driver die and its package. This scheme helps reduce or remove the need for high-temperature (200°C) compatible on-board components and simplifies the testing procedure by allowing for much shorter cabling between the test board and equipment, test leads, and (more importantly) the power device. The shorter leads and wires allow for lower off-chip parasitics. The heater and a temperature sensor, a resistance temperature detector (RTD) were held in place with an insulating Macor block that attached to the board and mechanically held the heating configuration in place. The overhead for this configuration on the test board was 4 holes to hold the Macor blocks in place and a slot cut directly under the chip package for the temperature sensor or tape heater to make contact. However, using the film heater arrangement, temperatures below room temperature (RT, approximately 27°C) were not possible. Figure 4.8 and Figure 4.9 display the heater system installed on a gate driver test board and the tape heater test setup.

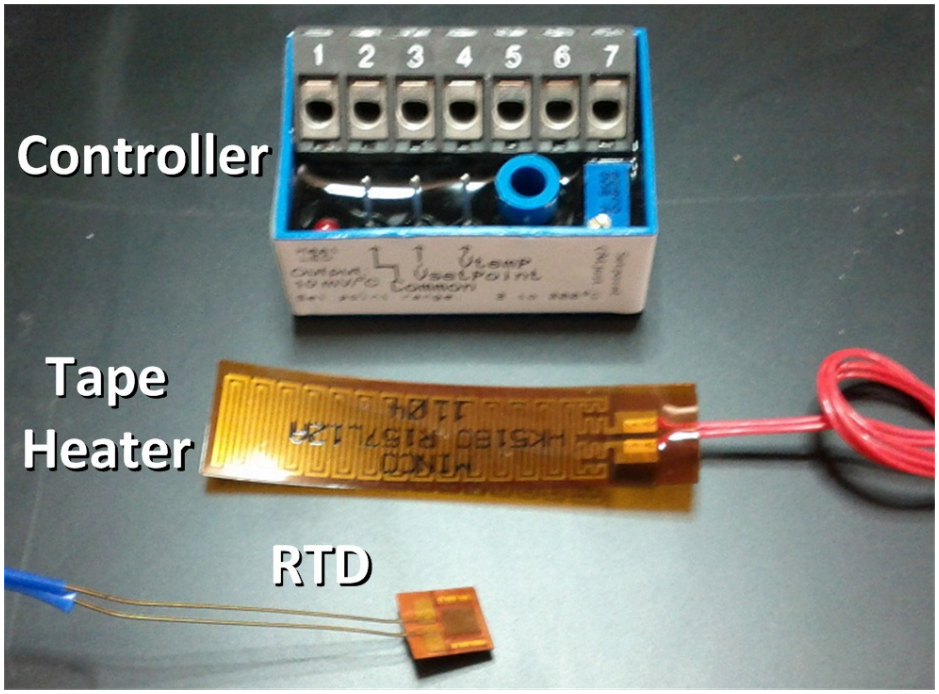


Figure 4.7. Tape heater system with controller and RTD.

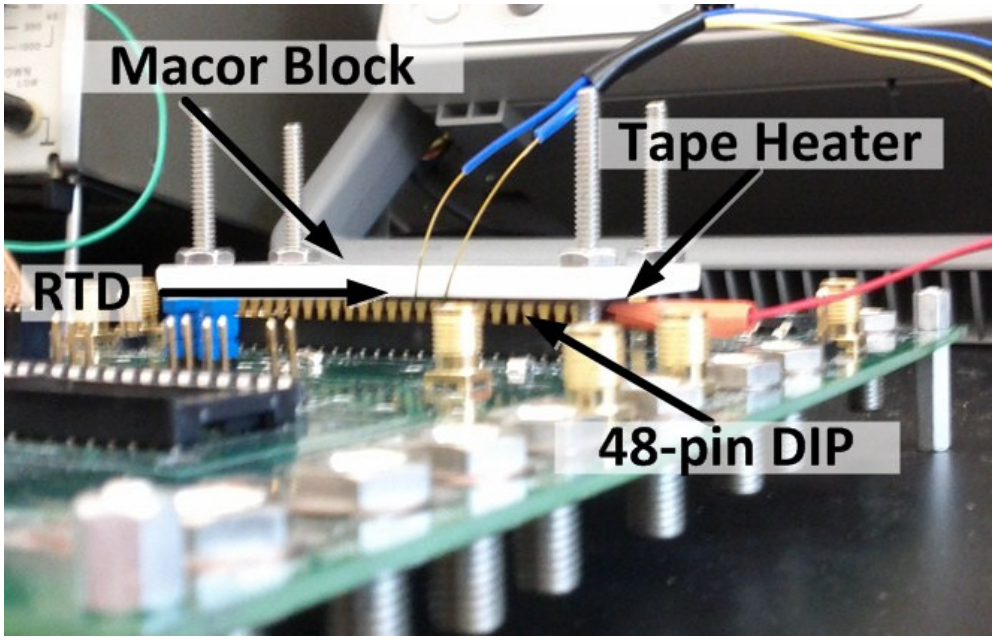


Figure 4.8. Installed tape heater system.

Figure 4.9. Tape heater test setup.

The printed circuit boards used with the tape heater configuration were made of FR-4 epoxy laminate. FR-4 has a maximum glass transition temperature (T_G) of between 125°C and 145°C, which is suitable for the tape heater as the board itself is not directly heated to 200°C [68][70]. Additionally, this test setup used standard solder, with a typical melting point between 180°C and 190°C, as the board itself is not exposed to the high temperatures of the heater.

PCBs for use in the oven at temperatures up to and greater than 200°C must be made with a material that has a higher T_G than FR-4, such as polyimide. Polyimide epoxy materials typically have a T_G above 250°C, and can be as high as 315°C [68][71]. Further, high-temperature solder must be used, with a melting point well above 200°C. Lastly, wire used in the oven (at temperatures over 150°C) that must be insulated, such as wiring going into/out of the oven, must have a high-temperature insulator, such as polytetrafluoroethylene (PTFE). PTFE is capable of surviving extended exposure to temperatures as high as 260°C and has a melting point of 327°C [71].

The last major test configuration utilized was a chip-on-board (COB) system, an image of which is shown in Figure 4.10. As discussed in Chapter 3, instead of utilizing a die bonded to a package and mating the package to the PCB through a socket, a chip-on-board approach directly bonds the die, in this case a gate driver chip, to the PCB under test using bond wires. This implementation shortens the bond wires, removes the chip package and socket, and can therefore have a large impact on the reduction of parasitics. However, the COB approach did have limitations in regard to testing the gate driver. Temperature testing conducted using the chip-on-board configuration was limited to the temperature chamber due to incompatibilities with the tape heater system. Additionally, due to the small board size (2” x 2” for die bonding) there was limited access to on-board test-points and signals. Also, note the small wire loop on the test board. Because the Hall Effect sensor could not be placed in the oven, this loop was brought outside the oven and was required so that the sensor could be used to measure the transient output current of the gate driver.

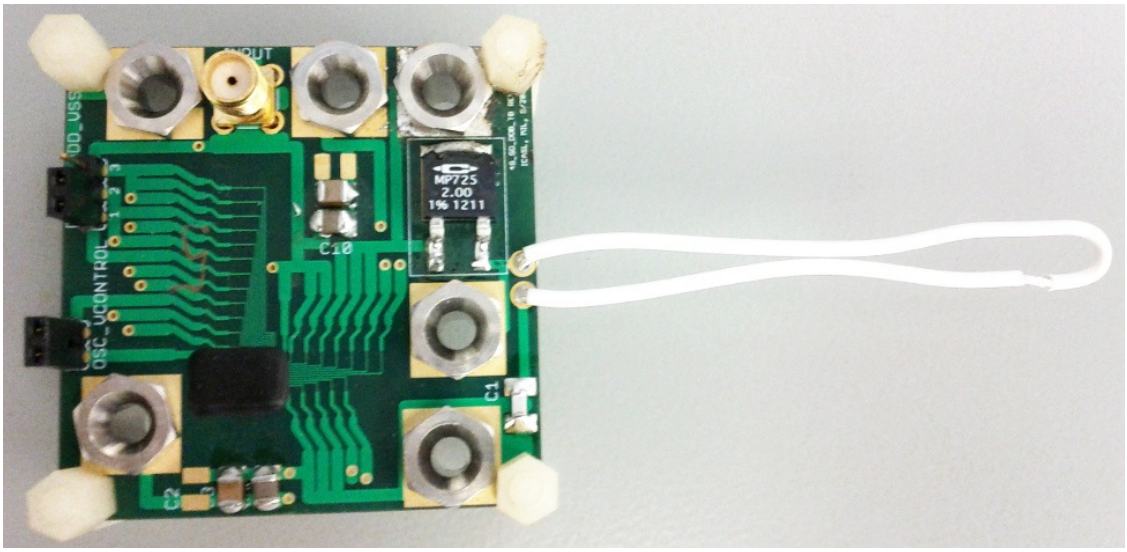


Figure 4.10. Chip-on-board PCB.

Measurement Results

The following sections contain the experimental results obtained for the gate driver IC described in this document. This includes measurements data for the charge pump, ring oscillator, gate driver core, output current drive, power devices being driven by the gate driver, and reliability testing. Where applicable, the configurations used for the test are described.

Ring Oscillator and Tape Heater Calibration

The ring oscillator on *Corinth* is used to control the mode of operation of the charge pump. Ring oscillators are also a useful tool in the characterization of a process across temperature [72]. This is due to the components of the oscillator having a direct and significant measureable impact on the circuit's performance. Additionally, ring oscillators are self-starting and require no external signals, save V_{DD} and V_{SS}, to operate. For these reasons, we also used the ring oscillator to characterize the operation of the tape heater. This was done by first measuring the output frequency of the ring oscillator across temperature using the temperature chamber. These results are given in Figure 4.11.

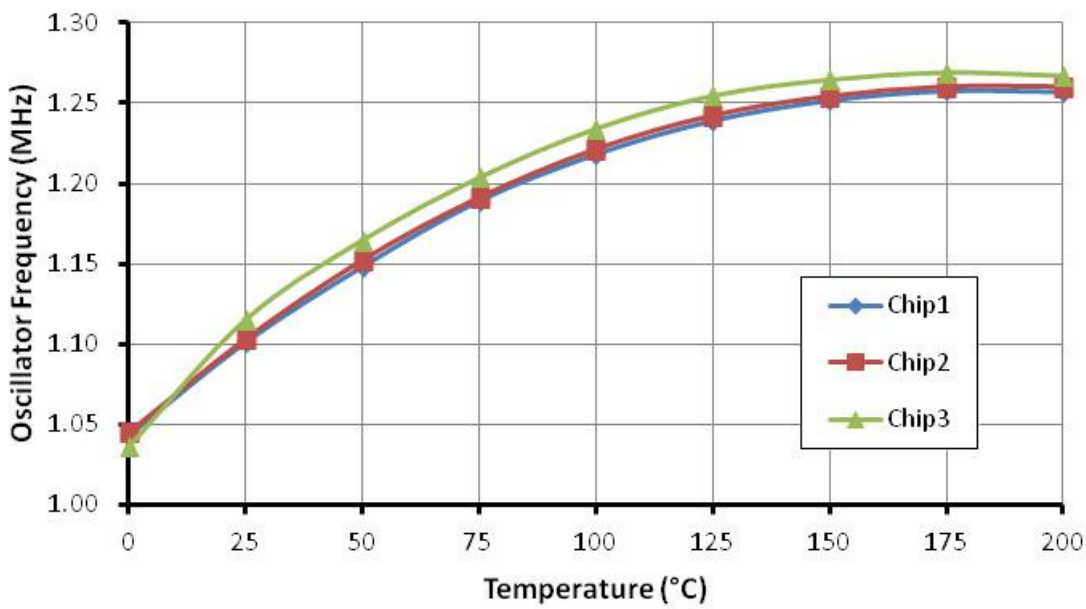


Figure 4.11. Ring oscillator frequency vs. temperature.

The ring oscillator was used to calibrate the tape heater test configuration by comparing the measured oscillation frequencies from the oven at a known temperature, Figure 4.11, to the oscillation frequencies recorded using the tape heater and RTD. Results are shown in Figure 4.12 and Table 4.2. The RTD has a temperature value notably less than the oven for a given oscillation frequency at high temperatures. This was due to the temperature delta between the RTD and gate driver die as the resistance temperature detector was placed on top of the package while the tape heater was located on the bottom of the package.

Charge Pump Capacitors

The charge pump, as described previously, makes use of two large 1.5 nF capacitors for charge transfer and storage to generate the high-side floating supply, V_{OP_PLUS}. These capacitors also share the same unit capacitor (50 pF) with the regulators capacitors, which were arrayed to create the desired capacitor values. Figure 4.13 presents the measured values of sample capacitors across temperature that have an intended nominal value of 1.5 nF. The fact that the capacitor values were lower than expected helps to explain why the ring oscillator was operating faster than simulations predicted, as smaller capacitors would lead to faster oscillation frequencies.

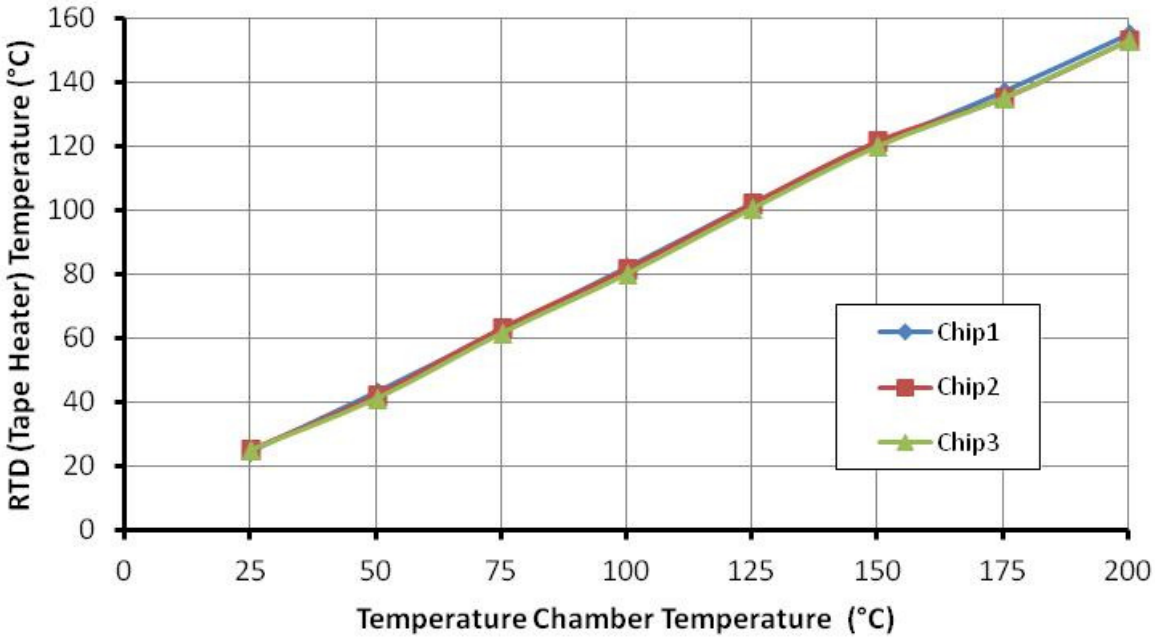


Figure 4.12. Oven temperature vs. tape heater RTD temperature for matched ring oscillator values.

Table 4.2. Oven temperature and RTD temperature for matched ring oscillator values.

Oven Temperature (°C)	RTD (°C)	Delta (°C)
25	25	0
50	42	8
75	62	13
100	81	19
125	102	23
150	121	29
175	136	39
200	154	46

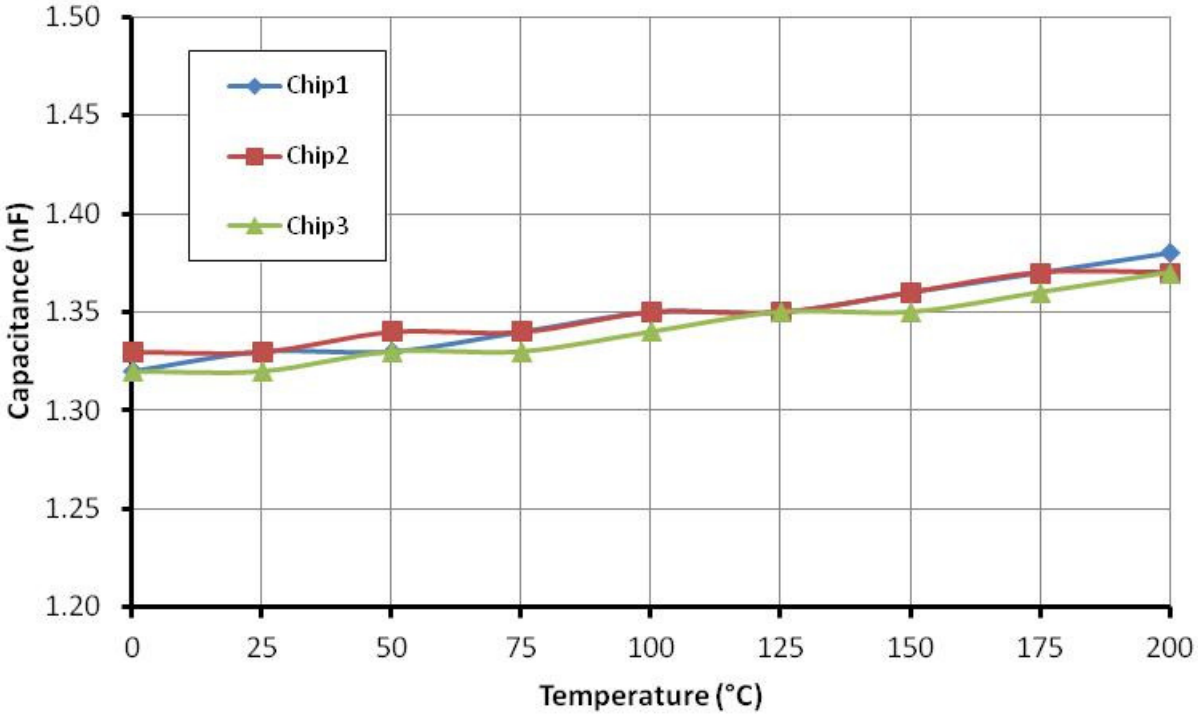


Figure 4.13. Charge pump capacitor value vs. temperature.

Charge Pump

Several measurements were made to characterize the operation of the charge pump circuit while powering the gate driver high-side circuitry. The first measurement was of the floating supply rail generated by the charge pump, V_{OP_PLUS}, designed to be nominally 5 V above the output voltage V_{OP}. Figure 4.14 demonstrates the measured V_{DD_CP} voltage necessary to produce a 5-V V_{OP_PLUS} floating output voltage from the charge pump while under load from the gate driver.

Another measurement made to characterize the performance of the charge pump was to establish the functional switching frequencies, typically supplied by the nominally 1 MHz on-chip ring oscillator. For this measurement the control signal for the charge pump, $V_{CONTROL}$, was swept across frequency. The output voltage, V_{OP_PLUS}, was monitored for changes greater than 10% from its established nominal value at a given temperature. Figure 4.15 and Figure 4.16 show the lower and upper frequency bounds of $V_{CONTROL}$, respectively, to maintain the output voltage of the charge pump within the stated bounds. Additional measured results for the charge pump operating with the core gate driver circuitry are presented in the next section.

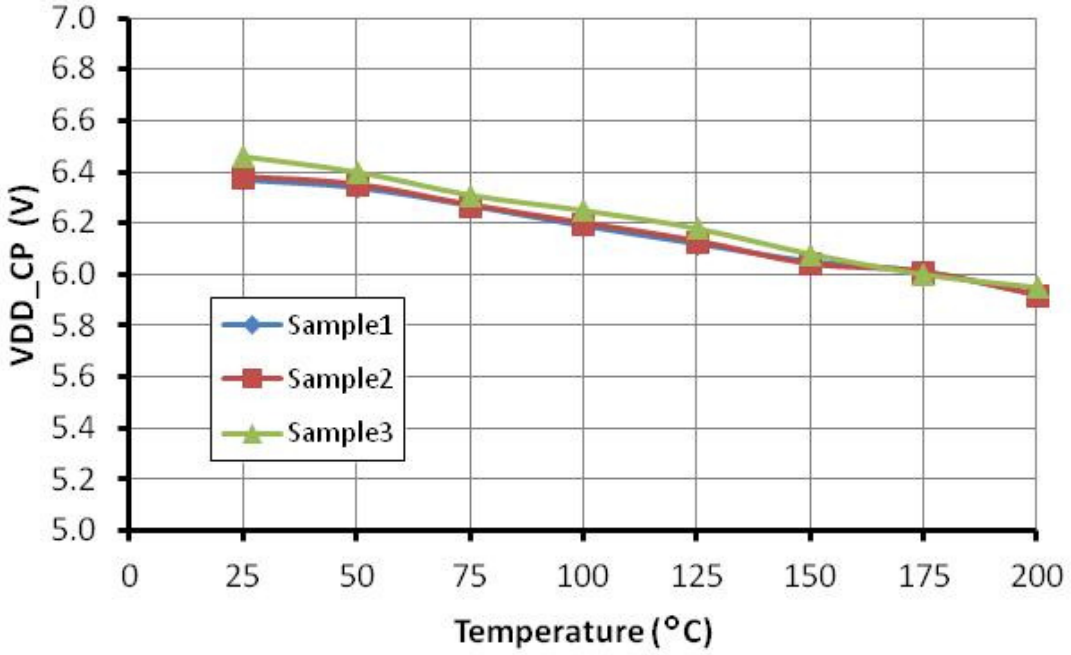


Figure 4.14. Charge pump V_{DD_CP} required for 5-V V_{OP_PLUS}.

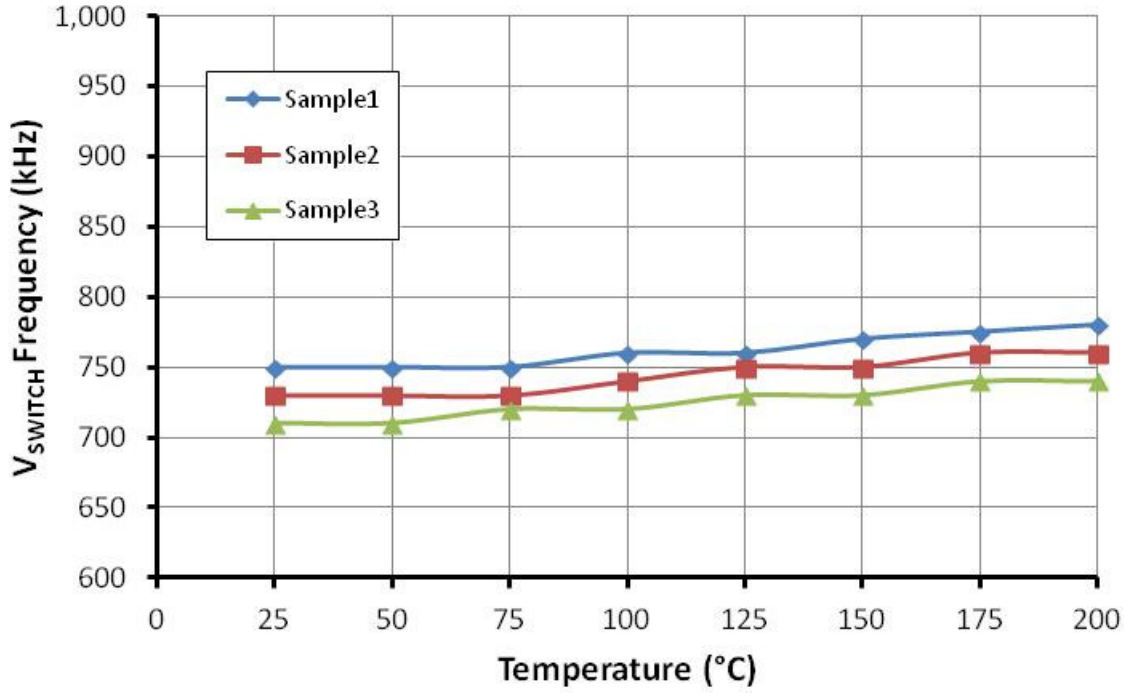


Figure 4.15. Charge pump $V_{CONTROL}$ lower frequency bound.

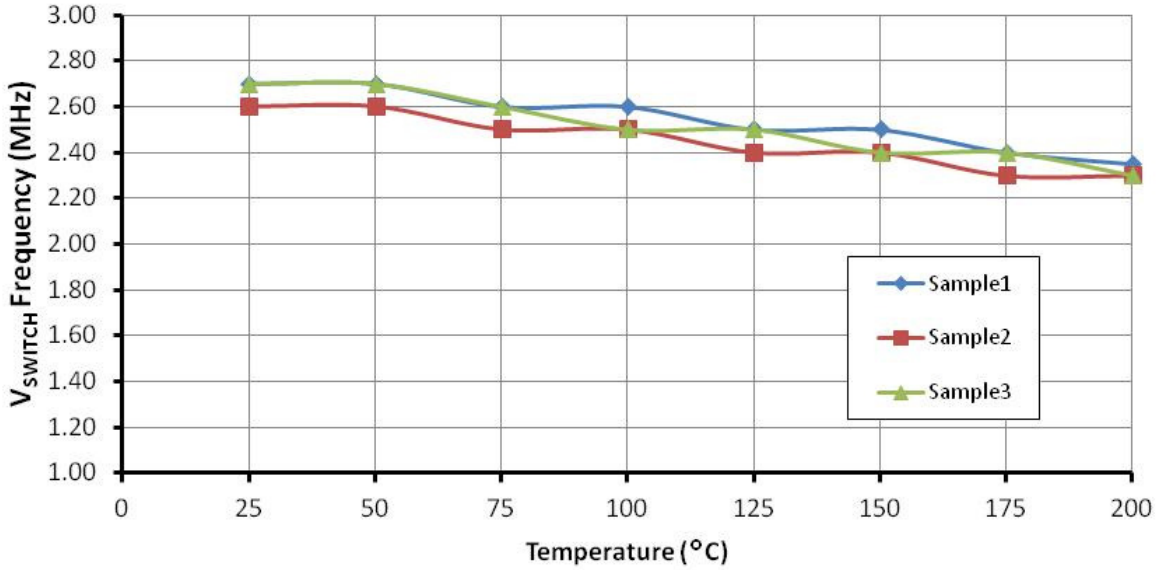


Figure 4.16. Charge pump $V_{CONTROL}$ upper frequency bound.

Gate Driver Core

Measurements were performed to verify and quantify the performance of the core gate driver circuitry. This included maximum sinking and sourcing currents, operational frequency across temperature, and functionality with varying loads (capacitive, SiC MOSFET, BJT, JFET, etc.).

Corinth was designed to drive capacitive loads up to 10 nF. While driving this load, it was important to measure the maximum sinking and sourcing currents generated by the gate driver, as these results help determine the gate drivers suitability for a variety of potential applications. As parasitics have a large impact on the drive current of the IC, the chip-on-board PCB implementation was used for this measurement. The test configuration used for these measurements is shown in Figure 4.17.

Figure 4.18 and Figure 4.19 represent samples of data taken at −55°C and 200°C demonstrating the output current drive of the gate drive IC. The output was connected to the 10 nF load through a 2 Ω gate resistor (R_G) and the gate driver was configured to have an output voltage swing of 30 V. In these measurements, the output current remains above 4-A across temperature. Figure 4.20 and Figure 4.21 display the results for several chip samples across temperature. Figure A.4 and Figure A.5, in the Appendix, demonstrate the output current across temperature using a 1 Ω gate resistor. The sourcing and sinking currents were approximately 4.5-A and 5-A, respectively, at 200°C.

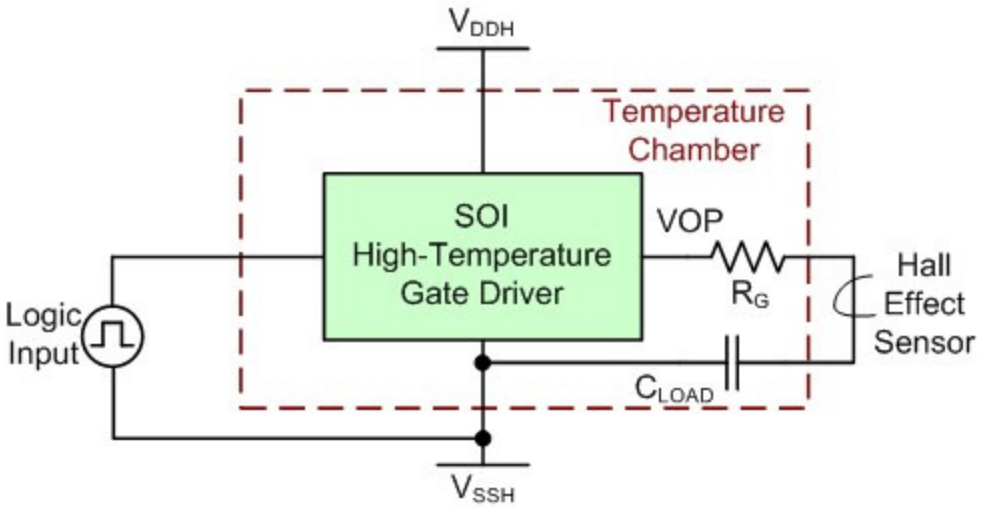


Figure 4.17. Load current test configuration using COB setup.

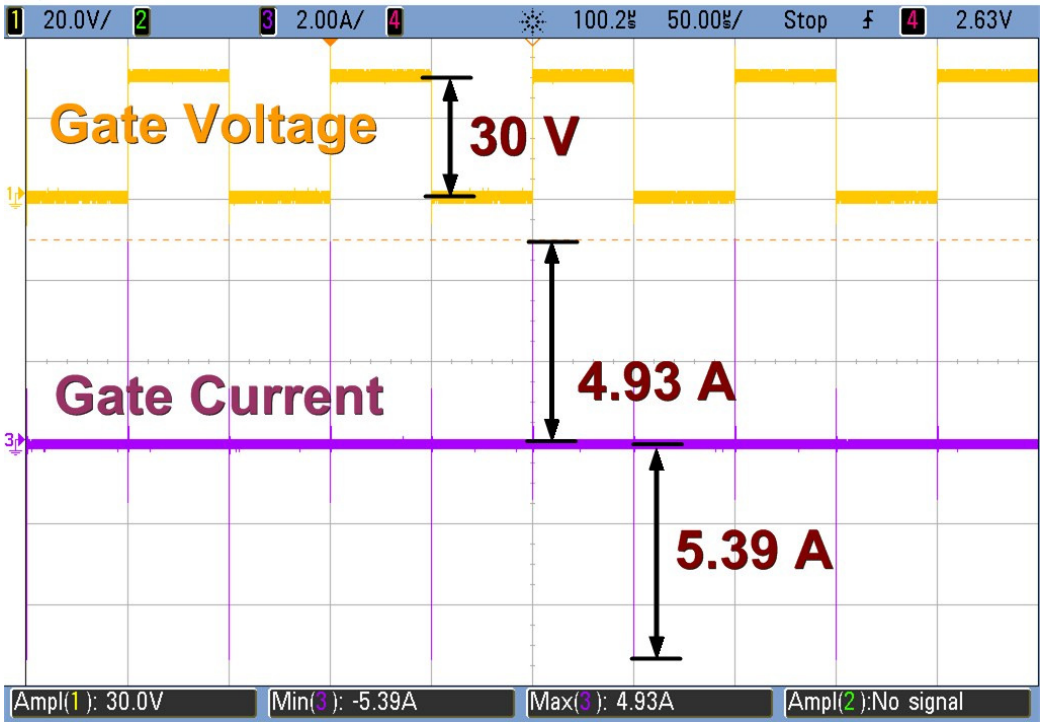


Figure 4.18. Sourcing and sinking currents at −55°C, 30 V output with 2-Ω R_G.

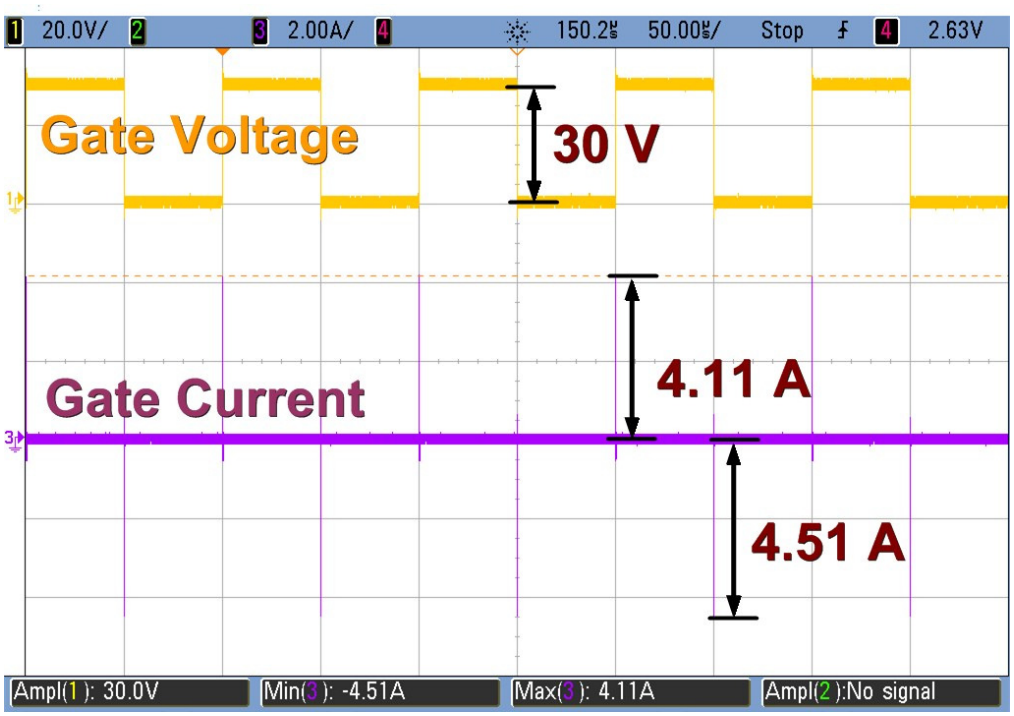


Figure 4.19. Sourcing and sinking currents at 200°C, 30 V output with 2-Ω R_G.

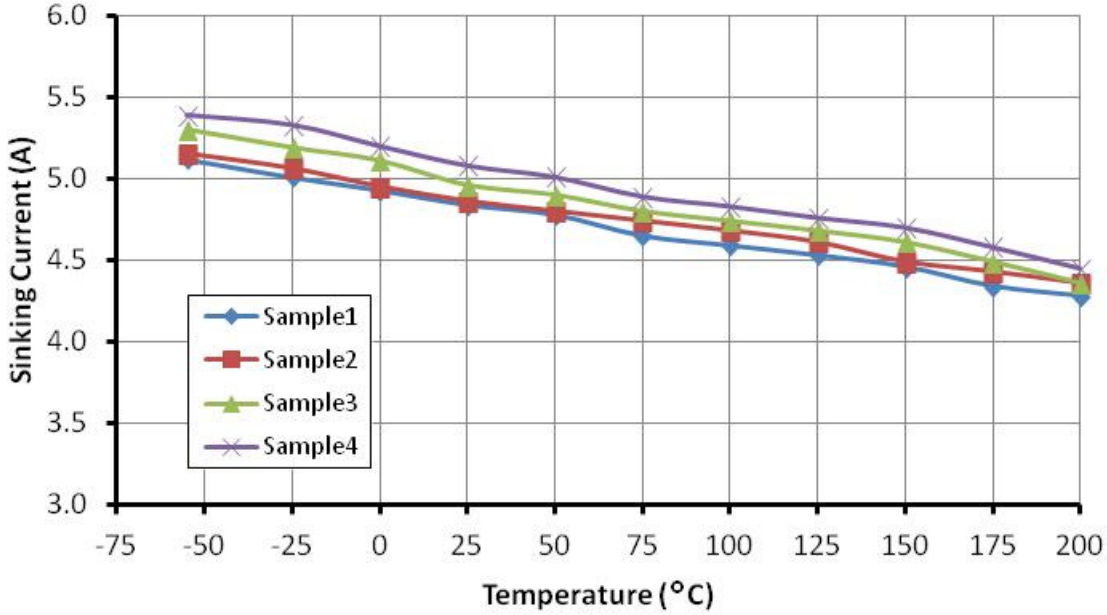


Figure 4.20. **S**inking currents across temperature with. 2-Ω R_G.

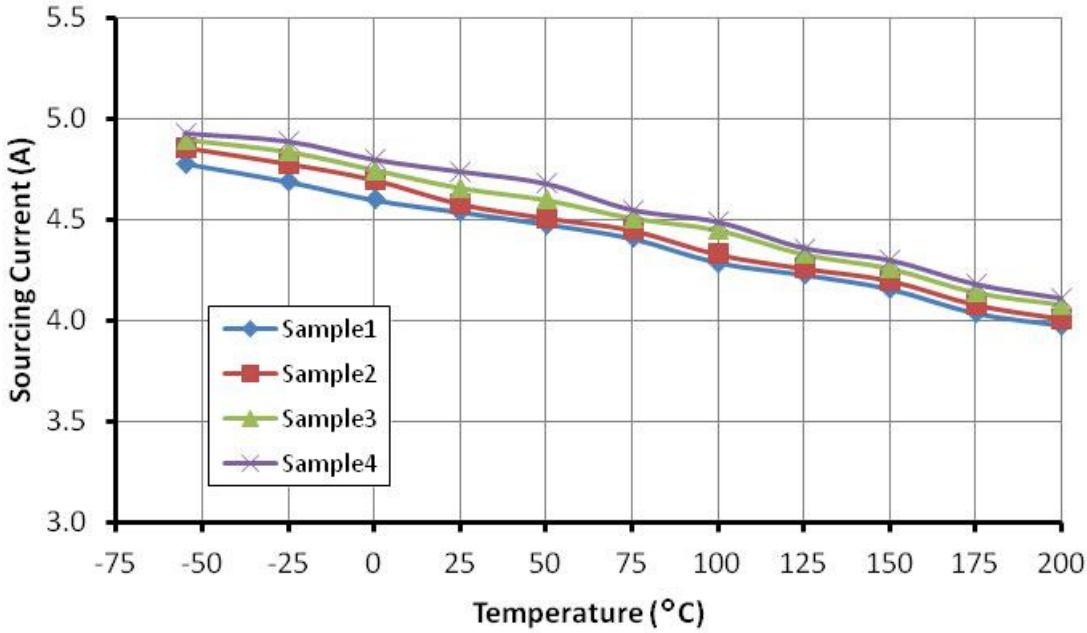


Figure 4.21. Sourcing currents across temperature with 2 Ω-R_G.

Characterization of the maximum operational frequency of the gate driver core across temperature involved sweeping the input signal from DC until there was sufficient signal degradation to render the output signal unusable. This degradation can take the form of phase shifting, amplitude loss, loss of signal, signal noise, etc. This characterization also involved testing of the charge pump circuit, as this test was also dependent on the charge pump being capable of providing sufficient power the high-side devices; V_{DD_CP} was an important element of this test.

The following tests were configured as shown in Figure 4.22. Using the V_{DD_CP} values shown in Table 4.3, which were taken from measurements made of the voltage regulators output, the frequency of the gate driver's input signal was swept from DC to the point that the output signal was sufficiently degraded. The results of this sweep are shown in Figure 4.23. A data point is not given for 200°C operation because the gate driver's output was unstable while operating at this temperature with the V_{DD_CP} value denoted in Table 4.3. If the V_{DD_CP} value at this temperature was lowered to 5.88 V, the operation of the gate driver was stable to approximately 240 kHz. It should be noted this value is similar to that required for a 5-V V_{OP_PLUS} value, Figure 4.14.

Figure 4.24 and Figure 4.25 are representative of the failure mode limiting the upper operational frequency of the gate driver, as shown in Figure 4.23. The figures demonstrate the failure at 200°C using the functional V_{DD_CP} value of 5.88 V. There is obvious loss of signal as the

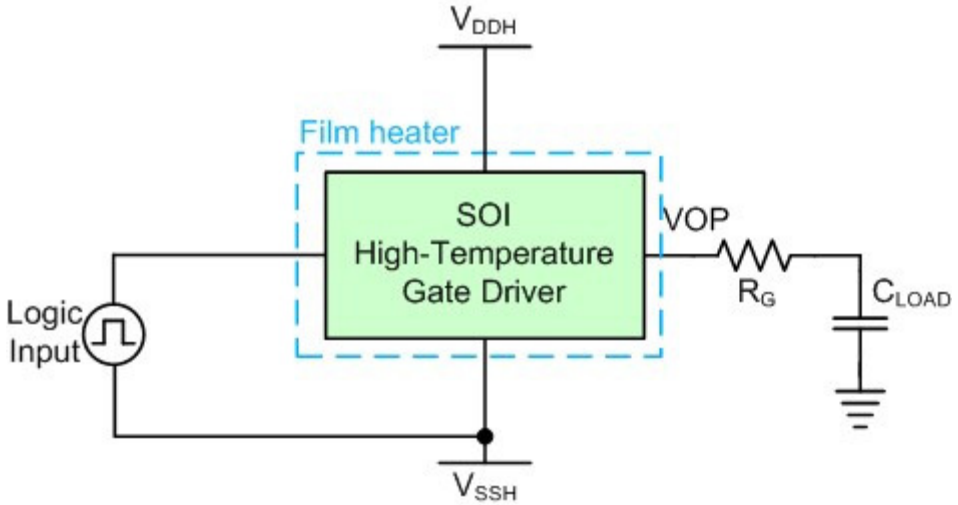


Figure 4.22. Maximum operating frequency test configuration.

Table 4.3. V_{DD_CP} from regulator measurement results.

Oven Temperature (°C)	V_{DD_CP} (V)
25	6.55
50	6.50
75	6.42
100	6.35
125	6.27
150	6.20
175	6.13
200	6.04

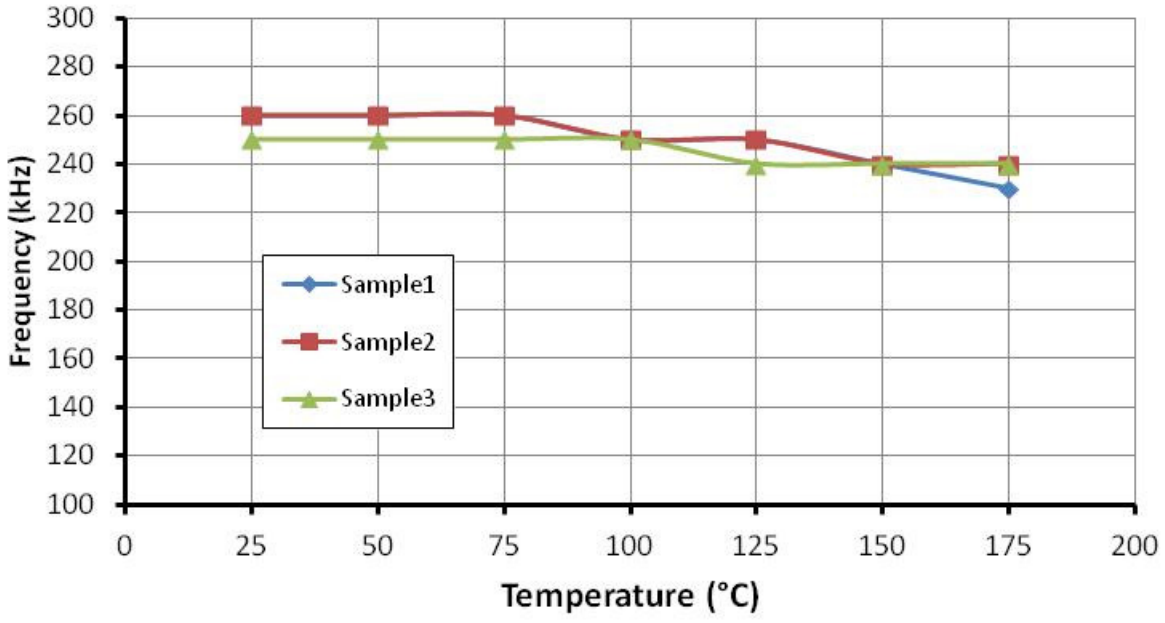


Figure 4.23. Maximum operating frequency with V_{DD_CP} values from Table 4.3.

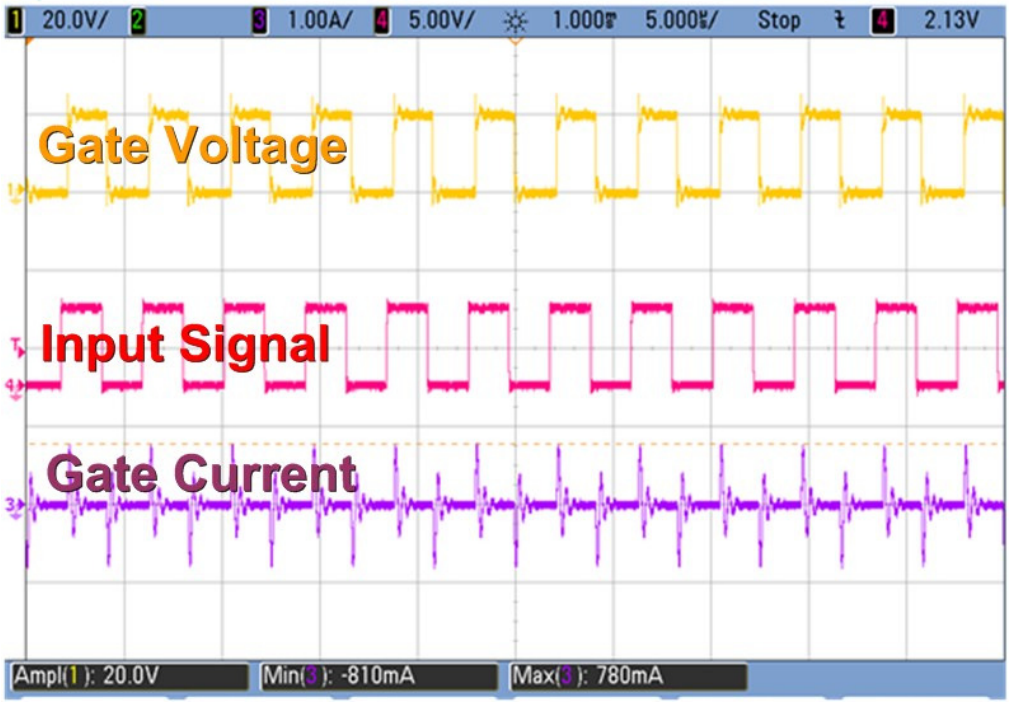


Figure 4.24. Operation of sample 2 at 240 kHz with V_{DD_CP} = 5.88 V (200°C).

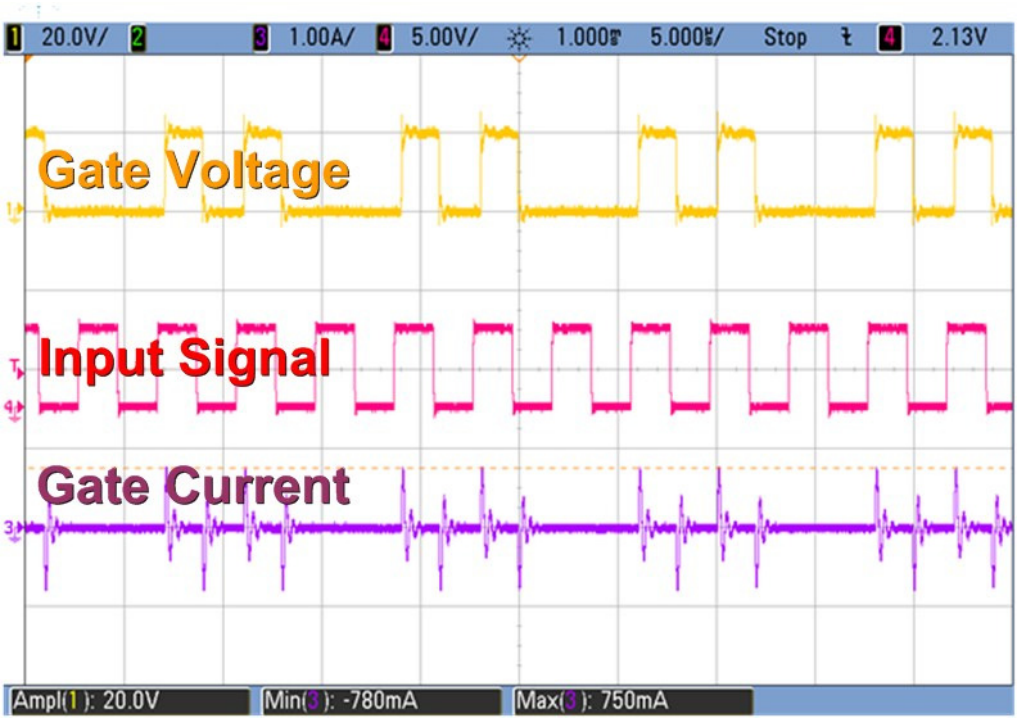


Figure 4.25. Operation of sample 2 at 250 kHz with V_{DD_CP} = 5.88 V (200°C).

frequency is increased. It should be noted that the gate driver was designed to operate up to 100 kHz and exceeds that benchmark in these measurements.

The value of V_{DD_CP} across temperature can be adjusted to enable higher operational frequencies than those presented in Figure 4.23. The values given in Table 4.4 allowed the gate driver to reach another failure mode related to the integrity of the output signal. The frequency range that was attained over temperature with these values is shown in Figure 4.26. As this figure demonstrates, the maximum operational frequency of the gate driver over temperature exceeds 550 kHz. The failure mode in this configuration was signal degradation of the output (V_{OP}) to the point that false triggering could occur.

Figure 4.27 demonstrates the gate driver operating at 200°C and 610 kHz with V_{DD_CP} at 5.48 V. In Figure 4.28, the frequency has been increased to 630 kHz. Note the dip forming near the end of each high-side edge. This signal perturbation increased in magnitude as the frequency was increased and rendered the output signal of the gate driver unsuitable for operation at these frequencies. It is important to note that the gate driver was designed for frequencies up to 100 kHz, and that operation at these frequencies was not a design goal.

Table 4.4. V_{DD_CP} values for higher operational frequencies.

Oven Temperature (°C)	V_{DD_CP} (V)
25	6.37
50	6.34
75	6.25
100	6.10
125	5.95
150	5.80
175	5.65
200	5.48

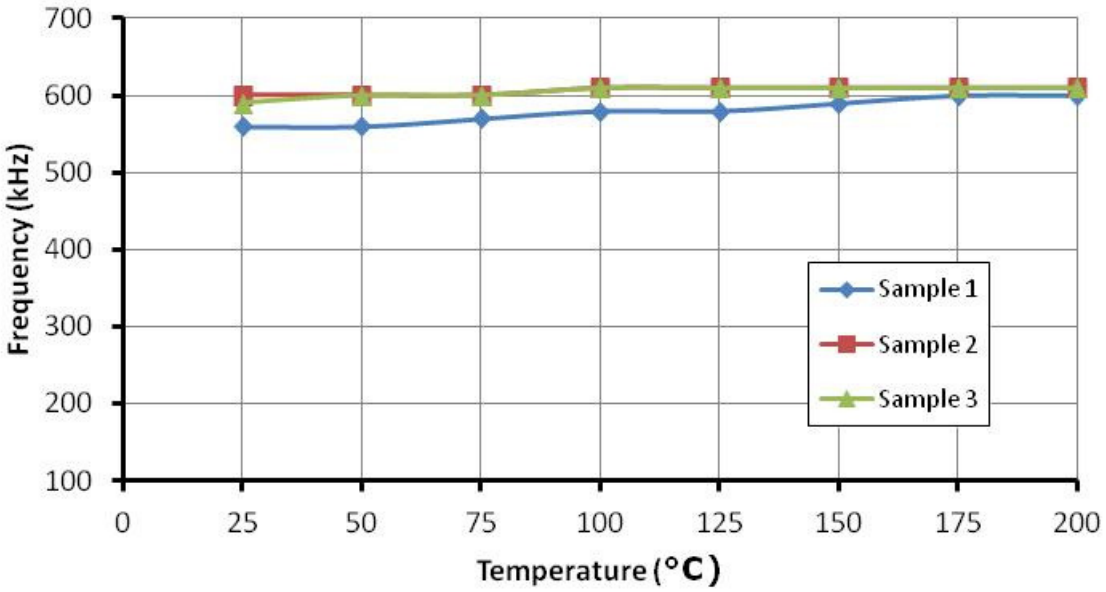


Figure 4.26. Maximum operating frequency with V_{DD_CP} values from Table 4.4.

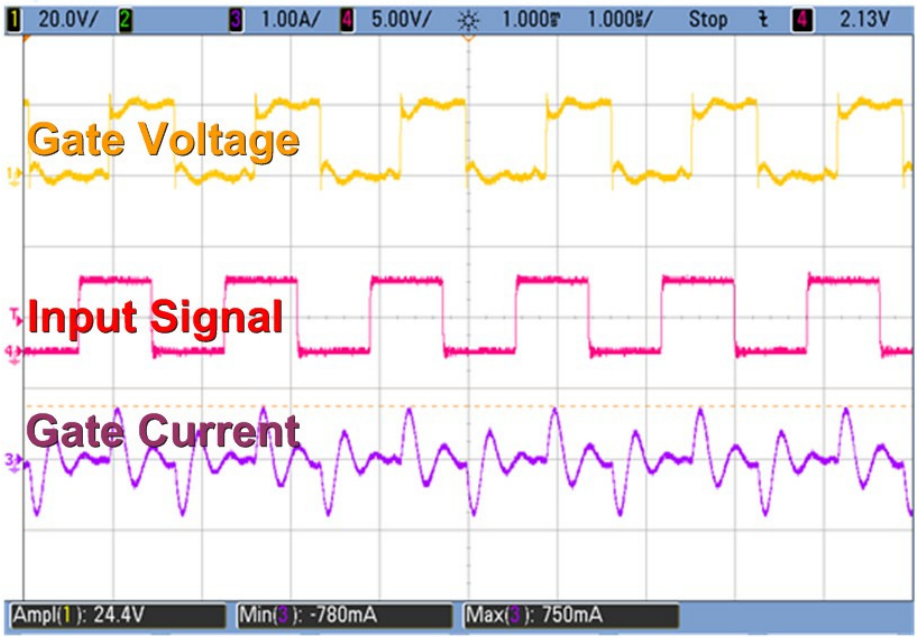


Figure 4.27. Operation of sample 2 at 610 kHz with V_{DD_CP} = 5.48 V.

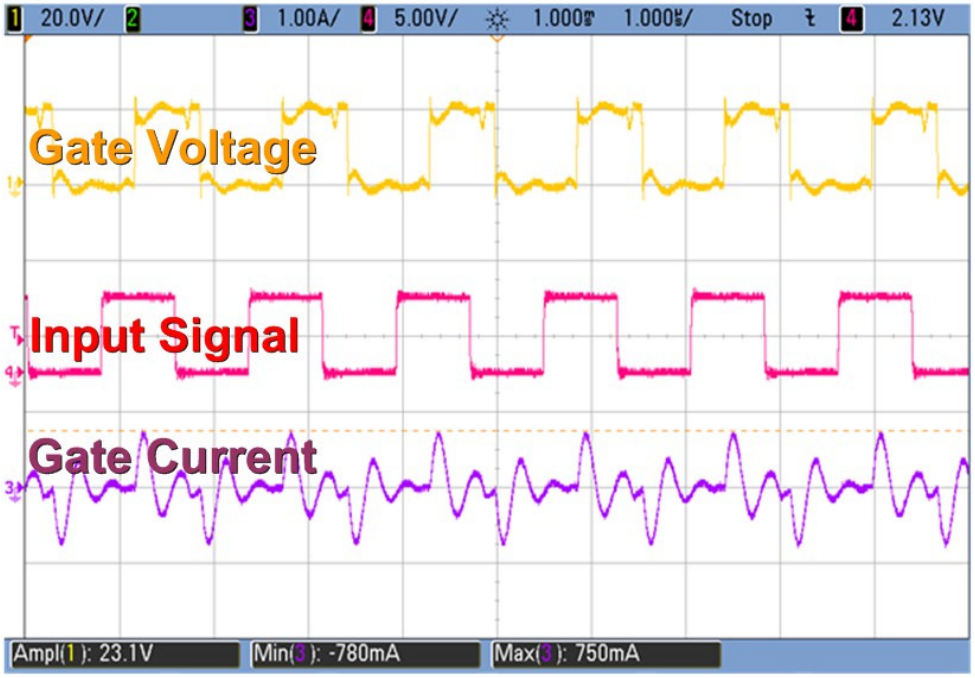


Figure 4.28. Operation of sample 2 at 640 kHz with V_{DD_CP} = 5.48 V.

The charge pump enables the gate driver to operate at a 100% high-side duty cycle by continually refreshing the charge of capacitor C2, which provides the floating supply rail to the high-side circuitry, Figure 3.1. To demonstrate this low frequency operation, the gate driver was tested with a 1-Hz input signal while in the configuration shown in Figure 4.17. Figure 4.29 and Figure 4.30 demonstrate the operation of the gate driver at this frequency for −55°C and 200°C operation. Note that an output current is not shown directly in these figures, as the oscilloscope was unable to resolve the transient current signal while measuring the 1 Hz voltage waveform due to signal resolution limitations.

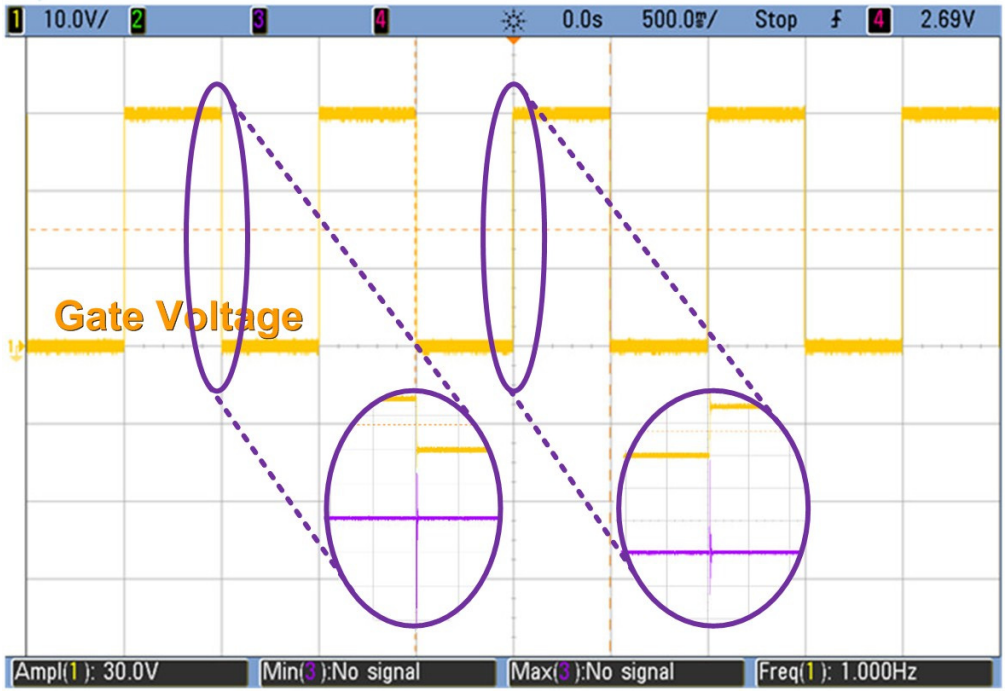


Figure 4.29. 1 Hz gate driver operation at –55°C.

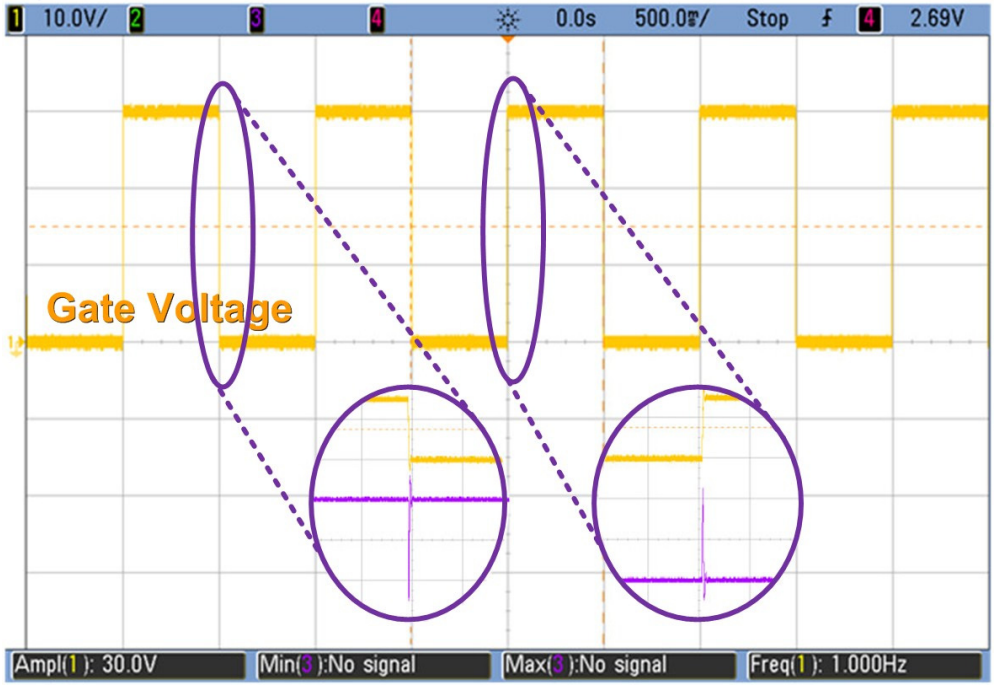


Figure 4.30. 1 Hz gate driver operation at 200°C.

Gate Driver Power Switch Testing

Further testing was carried out on the gate driver by characterizing its operation driving a variety of wide-bandbap power switches. The configuration for these measurements used either the oven or tape heater to temperature cycle the gate driver while leaving the power switch at room temperature, Figure 4.31. This was necessary because the packaging of SiC and other WBG power switches are not typically rated for high-temperature applications. Even though the power switch itself may be capable of operating in an environment up to or exceeding 200°C, the packages and interconnects supplied by the manufactures are not.

One of the devices tested with the gate driver was a 1200 V, 10 A SiC MOSFET manufactured by CREE, model CMF20120D. This device was rated for operation up to 125°C. The n-channel enhancement mode MOSFET was connected to a 600-V DC-link through an 80 Ω load connected to its drain terminal. The gate terminal of the MOSFET was connected to the gate driver through a 2-Ω gate resistor (R_G).

Figure 4.32 and Figure 4.33 show the voltage waveform measured at the gate terminal, the drain current, and the drain voltage of the SiC switch for 25°C and 200°C operation of the gate drive IC. The SiC MOSFET was driven at 10 kHz by a 20-V peak-to-peak gate signal with a 20% duty cycle to limit the power dissipated by the load. The drain current of the power MOSFET was 7.1 A and the drain voltage was 580-V when the switch was active. The V_{GS} rise time and fall time across temperature are given in Table 4.5.

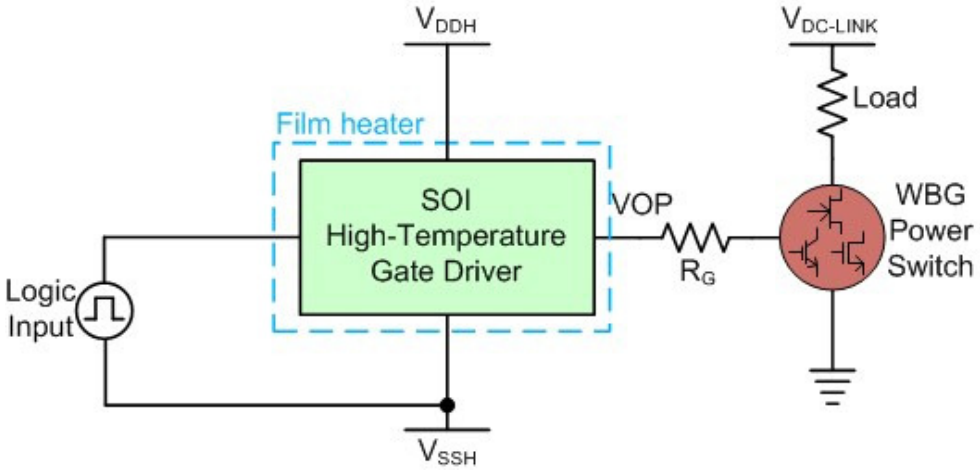


Figure 4.31. Power switch measurement configuration.

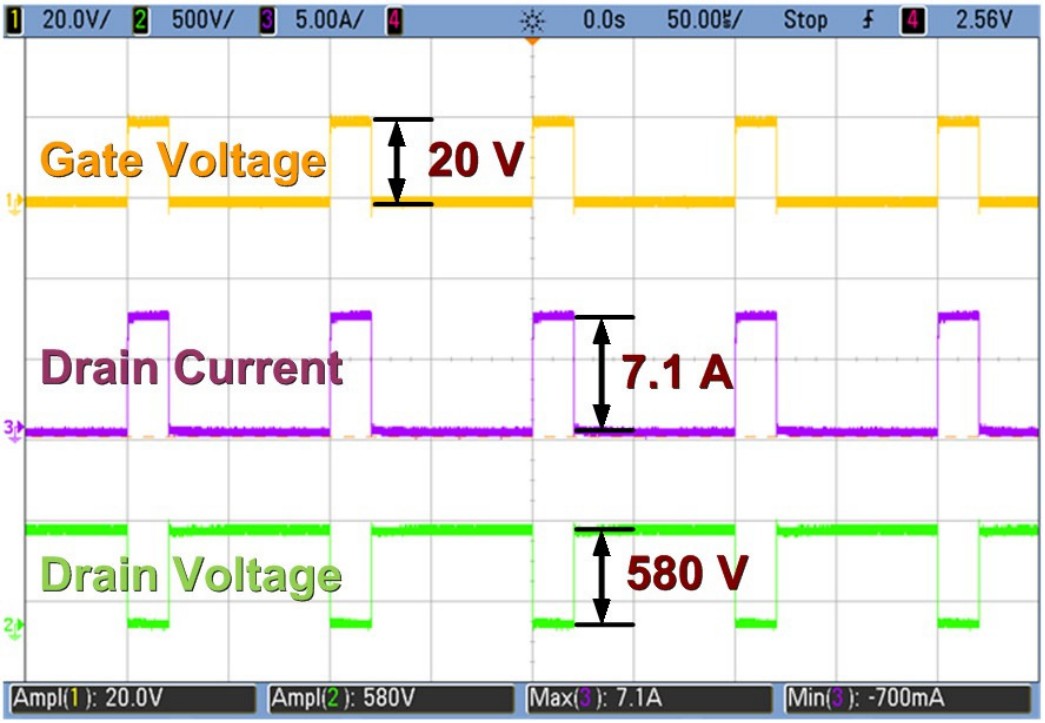


Figure 4.32. SiC MOSFET operating at 10 kHz, 600 V DC-link, 80 Ω load, 25°C.

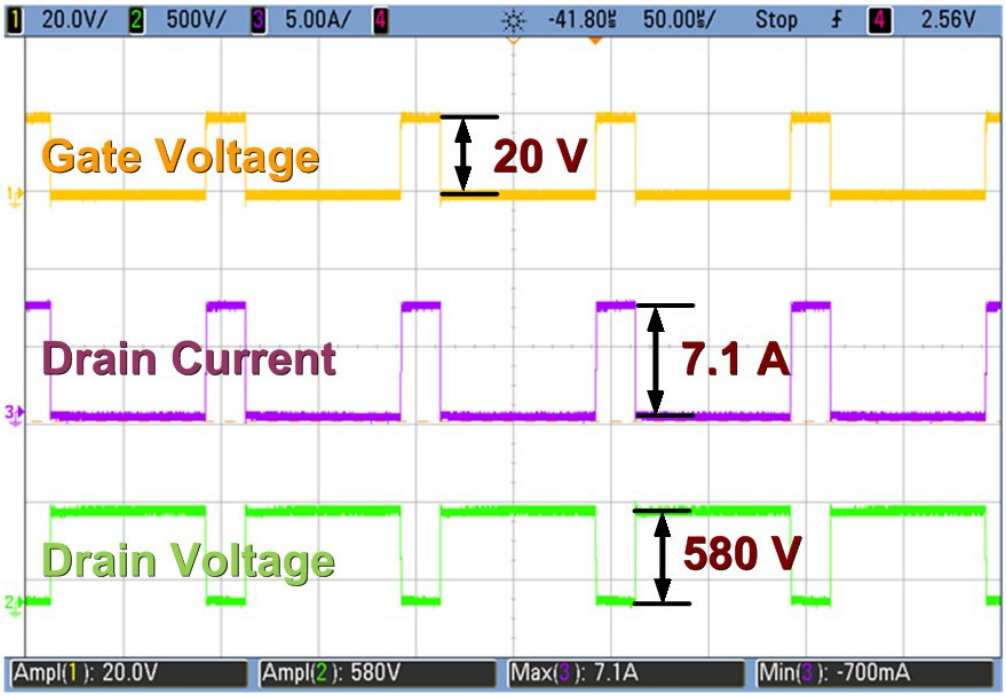


Figure 4.33. SiC MOSFET operating at 10 kHz, 600 V DC-link, 80 Ω load, 200°C.

Table 4.5. SiC MOSFET V_{GS} rise and fall times.

Temperature (°C)	Rise Time (ns)	Fall Time (ns)
25	10	12
125	13	15
200	16	18

Another silicon carbide device tested with the gate driver was a 1200 V, 50 A enhancement-mode JFET module manufactured by Microsemi/SemiSouth, model CMSSJC10A120. This module contained an anti-parallel SiC Schottky freewheeling diode with the JFET device. Using the same configuration shown in Figure 4.31, the JFET module was connected to the 600-V DC-link through an 80-Ω load. The gate terminal was driven by a 10-V (+2.5 V to −7.5 V) signal generated by the gate driver through a 2-Ω gate resistor (R_G).

Figure 4.34 and Figure 4.35 demonstrate the gate voltage, the drain current, and the drain voltage of the SiC switch for 25°C and 200°C operation of the gate drive IC. The configuration was being driven at 10 kHz with a 20% duty cycle to limit the power dissipated by the load. The drain current of the power MOSFET was 7.1 A and the drain voltage was 580-V when the switch was active. The rise time and fall time across temperature are given in Table 4.6.

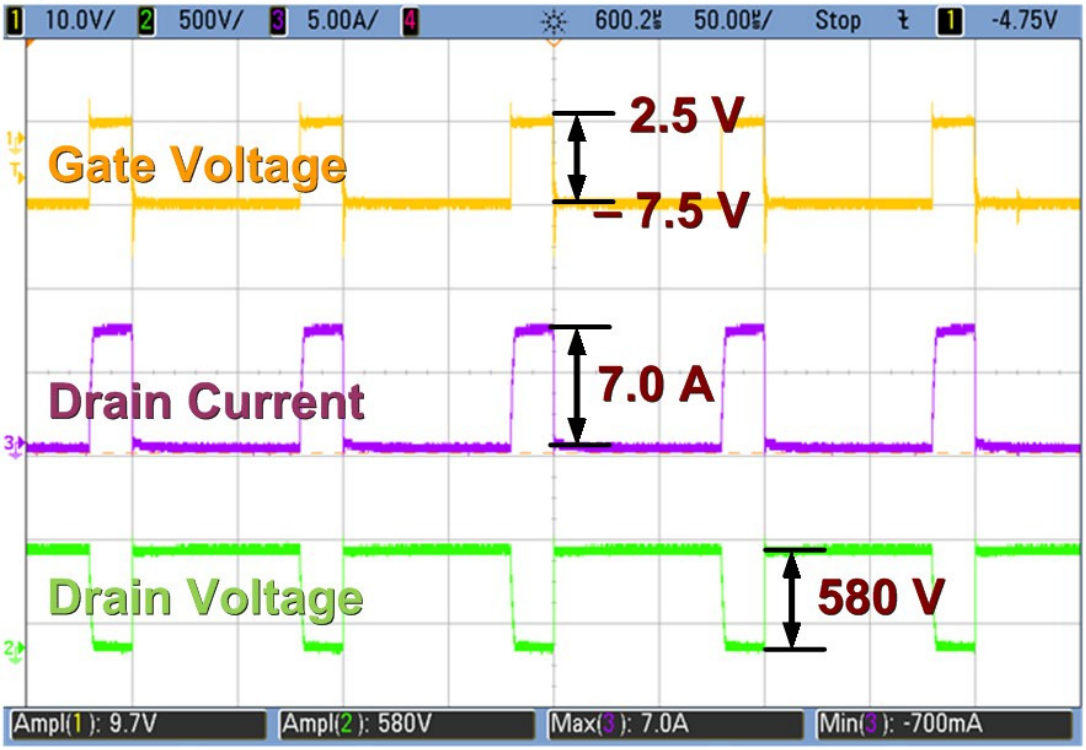


Figure 4.34. SiC JFET operating at 10 kHz, 600 V DC-link, 80 Ω load, 25°C.

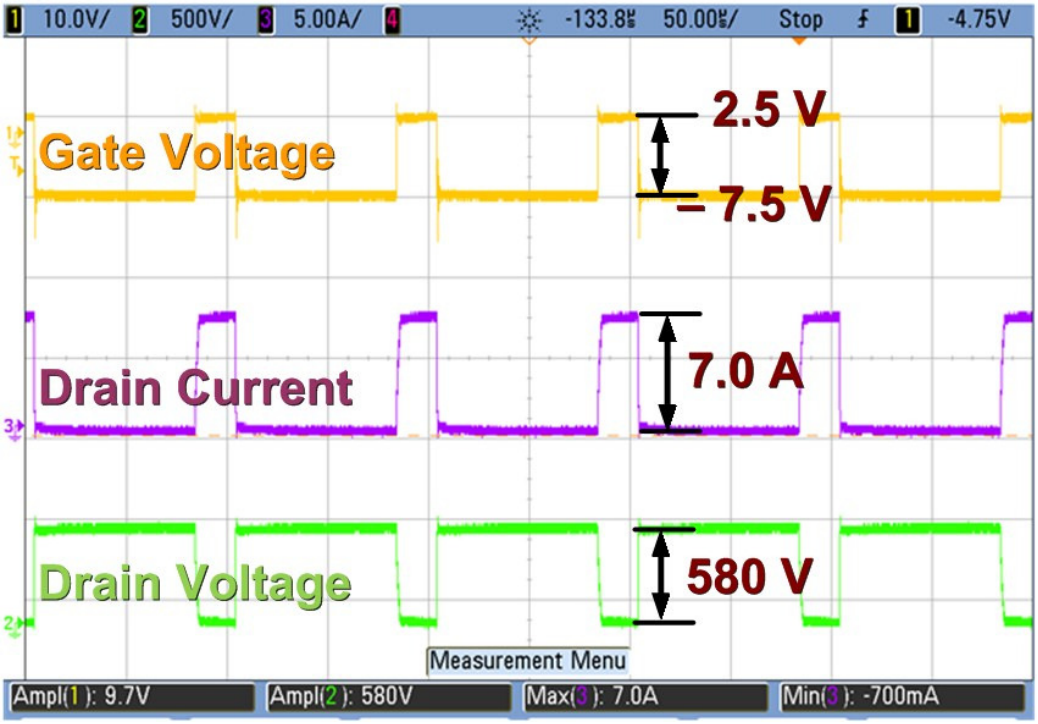


Figure 4.35. SiC JFET operating at 10 kHz, 600 V DC-link, 80 Ω load, 200°C.

Table 4.6. SiC JFET V_{GS} rise and fall times.

Temperature (°C)	Rise Time (ns)	Fall Time (ns)
25	6	13
125	8	16
200	12	20

A silicon carbide super junction transistor (SJT) is a power BJT device that has a relatively high current gain. An SJT tested with the gate driver was a 1200 V, 7 A component manufactured by GeneSiC, model A-GA10JT12. Using the configuration shown in Figure 4.36, the SJT module was connected to the 600-V DC-link through an 80 Ω load. The base terminal was driven by a 15-V signal from the gate driver through a 2 Ω gate resistor (R_{G1}) in series with a 20 nF capacitor (C_{G1}). Additionally, R_{G1} and C_{G1} were in parallel with a 15 Ω R_{G2}. The SJT required a high transient base current to efficiently activate the device and a steady-state current while the device remained 'on.' In this gate network, C_{G1} helped provide the transient current while also providing a low R_G at turn-on [73]. At steady-state, the capacitor becomes an open-circuit element and the 15 Ω R_{G2} limits the DC current supplied by the gate driver.

Figure 4.37 and Figure 4.38 demonstrate the base voltage measured at the device terminal, the base current, and the drain voltage of the SiC switch for 25°C and 200°C operation of the gate drive IC. The configuration was driven at 10 kHz with a 20% duty cycle to limit the power dissipated by the load. The base current of the SJT was 1.72 A and 1.59 A at 25°C and 200°C, respectively, with a steady state value of approximately 300 mA. The drain voltage was 580-V when the switch was active. Figure 4.39 displays the measured drain current of the SJT, which was 7.6 A across temperature. The rise time and fall time across temperature are given in Table 4.7.

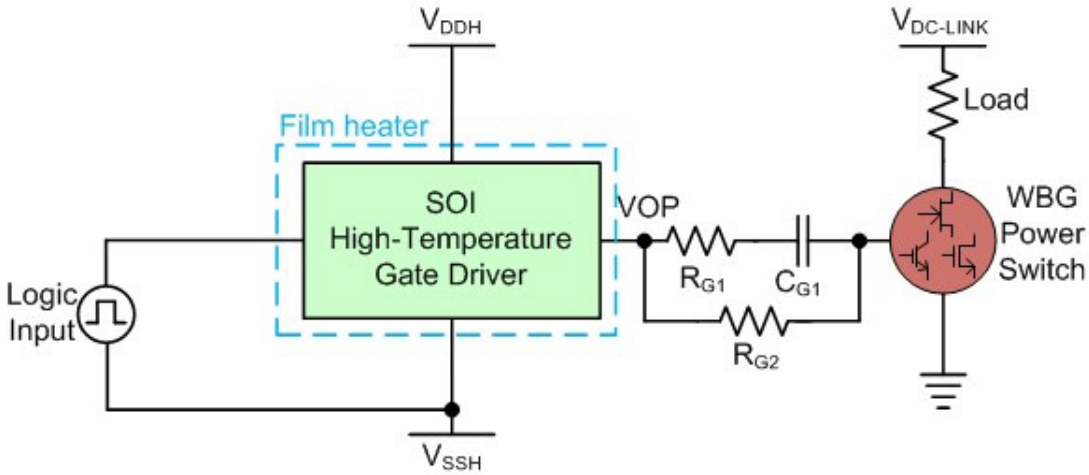


Figure 4.36. Power switch measurement configuration for SJT.

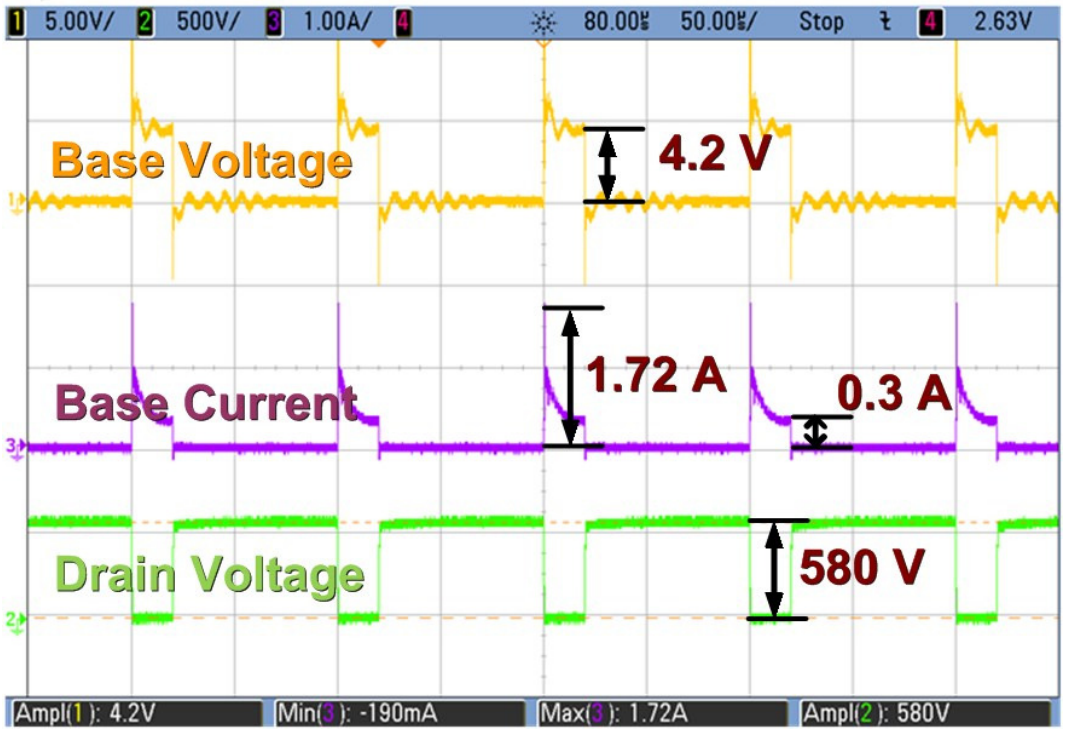


Figure 4.37. SJT operating at 10 kHz, 600 V DC-link, 80 Ω load, 25°C.

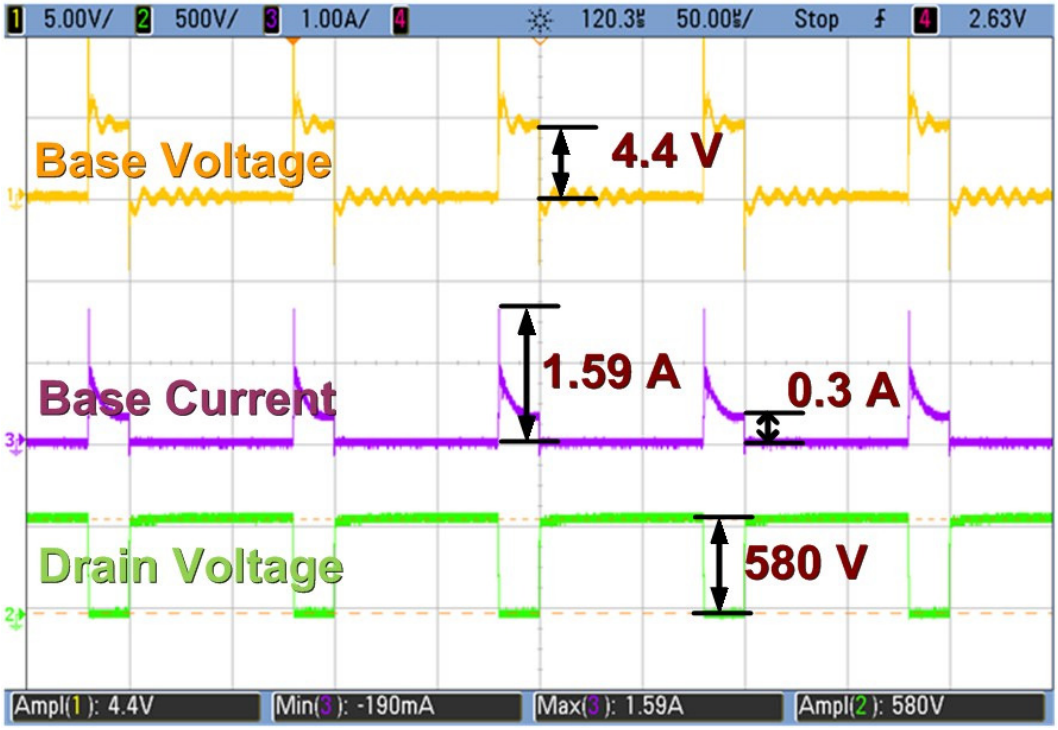


Figure 4.38. SJT operating at 10 kHz, 600 V DC-link, 80 Ω load, 200°C.

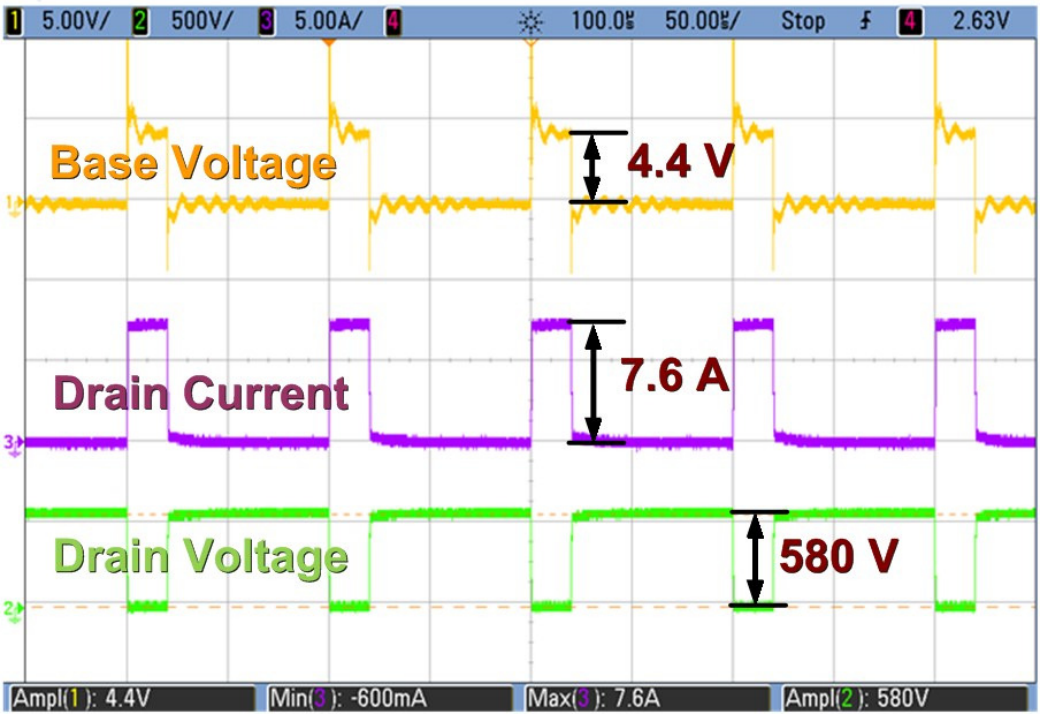


Figure 4.39. SJT operating at 10 kHz, 600V DC-link, 80Ω load, 200°C (displaying drain current).

Table 4.7. SiC SJT V_{BE} rise and fall times.

Temperature (°C)	Rise Time (ns)	Fall Time (ns)
25	6	13
125	8	16
200	11	18

A silicon IGBT with an anti-parallel SiC freewheeling diode was tested with the gate driver. The IGBT was rated for 1200 V and 35 A and was manufactured by GeneSiC, model GA035XCP12-247. The device was configured as shown in Figure 4.31 and connected to the 600-V DC-link through an 80 Ω load. The gate terminal was driven by a 15-V signal from the gate driver through a 2 Ω gate resistor (R_G).

Figure 4.40 and Figure 4.41 show the gate voltage, the drain current, and the drain voltage of the Si IGBT switch for 25°C and 200°C operation of the gate drive IC. The configuration was driven at 10 kHz with a 20% duty cycle to limit the power dissipated by the load. The drain voltage was 580-V when the switch was active and the drain current was approximately 7.7 A. The rise time and fall time across temperature are given in Table 4.8.

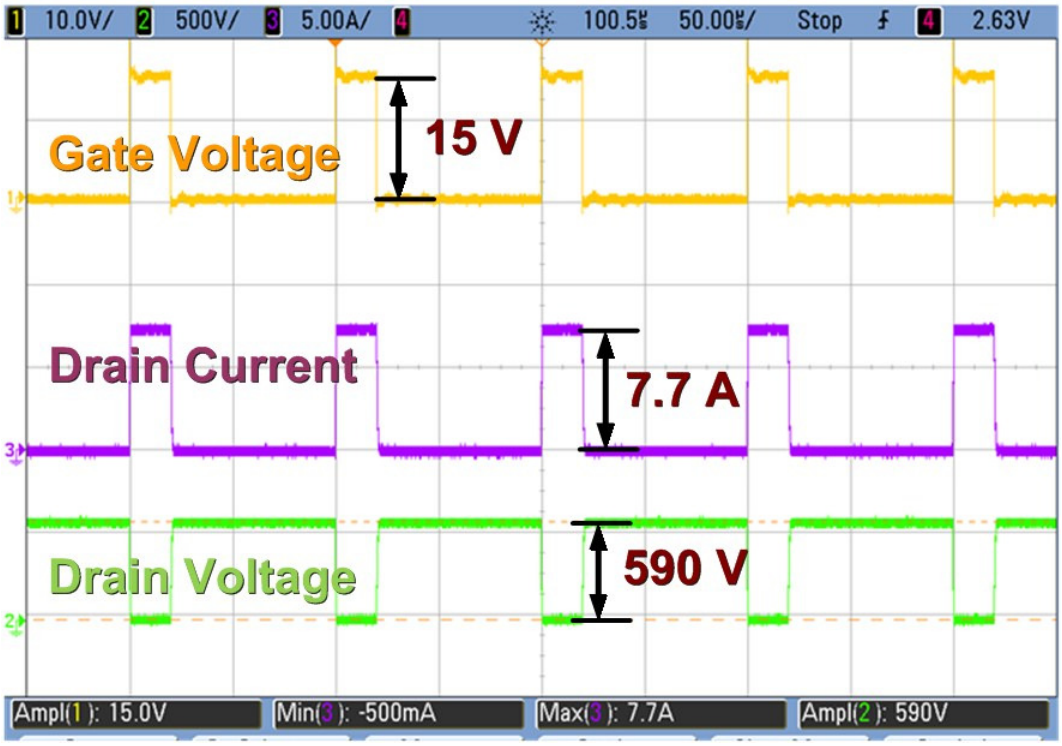


Figure 4.40. IGBT operating at 10 kHz, 600 V DC-link, 80 Ω load, 25°C.

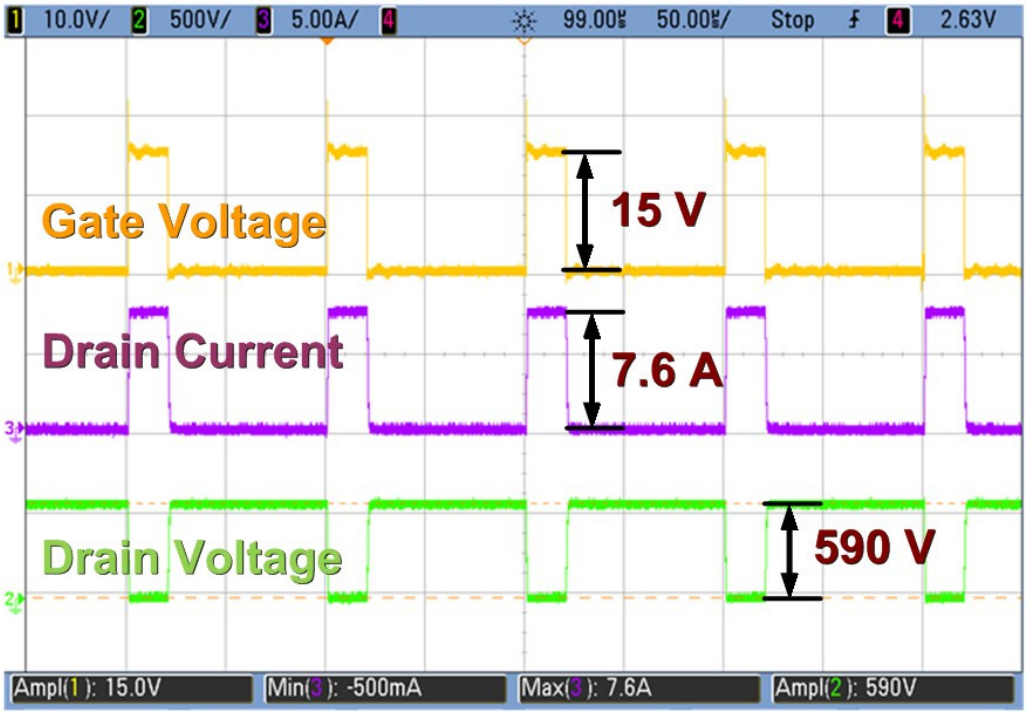


Figure 4.41. IGBT operating at 10 kHz, 600 V DC-link, 80 Ω load, 200°C.

Table 4.8. Si IGBT V_{GS} rise and fall times.

Temperature (°C)	Rise Time (ns)	Fall Time (ns)
25	6	8
125	8	10
200	10	11

Propagation Delay and Dead Time

Measurements were taken in order to characterize the propagation delay from the gate driver's input to the output, V_{OP}. This represents the amount of time required for the gate driver's output to change in correlation to a change in the logic level input control signal. A major factor in the propagation delay is the dead time, described in Chapter 2. The dead-time controller created two non-overlapping waveforms from the logic level input signal. The dead time separating the 'on' state of these two signals ensures the complementary 'on' and 'off' switching of the transistors in the "totem-pole" output stage without shoot-through, or crowbar, current.

The dead-time controller circuit had an input control signal, delay_control, which was tied to either V_{SS} or V_{DD}, to increase or decrease the dead time. Figure 4.42 shows a representative sample of the propagation delay for the rising and falling edges of the gate driver output for both delay_control settings. With delay_control set to V_{SS}, the rising edge propagation delay across temperature varied from 240 ns to 260 ns. The falling edge delay varied from 172 ns to 183 ns. With delay_control set to V_{DD} the rising edge and falling edge delay varied from 315 ns to 330 ns and from 244 ns to 252 ns, respectively.

Measurement results demonstrating the internal delay between the two non-overlapping outputs of the dead-time controller are shown in Figure 4.43. Curves are shown for each delay_control setting for the falling low-side to rising high-side signal delay (L↓ H↑) and the falling high-side to rising low-side signal delay (H↓ L↑). The dead time generated was stable over temperature but varied between the two dead-time controller outputs. The falling low-side to rising high-side dead time was about 40 ns longer than the falling high-side to rising low-side dead time for both delay_control settings.

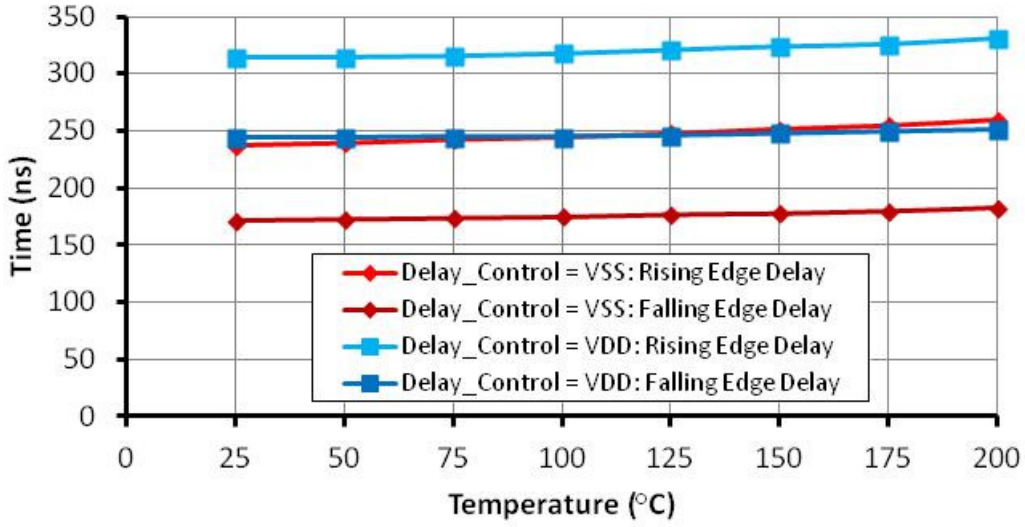


Figure 4.42. Gate driver IC propagation delay vs. temperature.

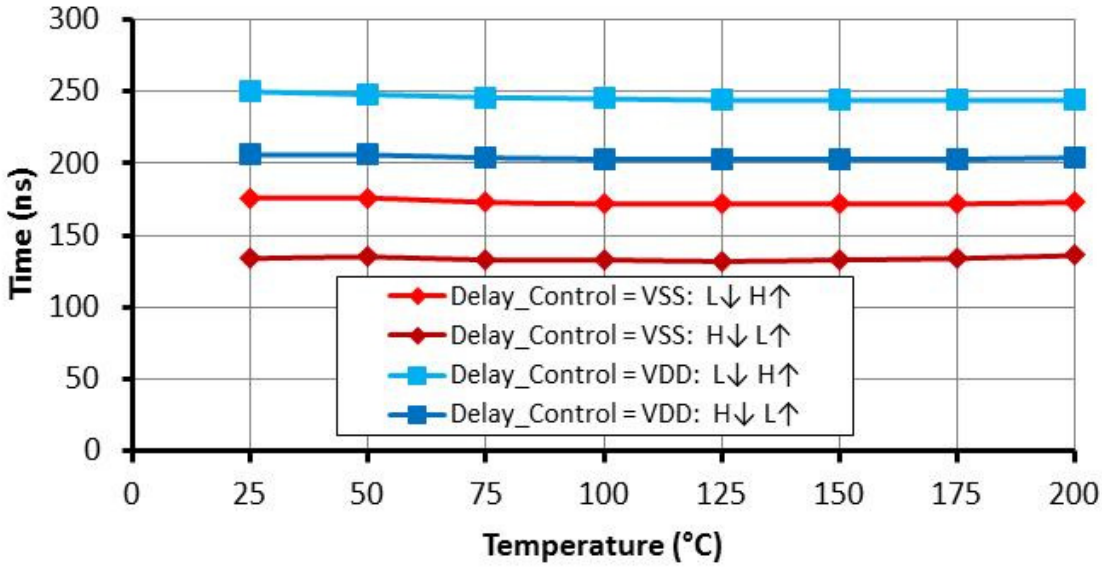


Figure 4.43. Delay time vs. temperature.

Reliability

Reliability testing of the gate driver was conducted to verify the operation of the IC at temperature for extended periods of time. Previous measurements of the gate driver made at high temperatures involved heating the IC until it settled at the target ambient temperature, then taking the desired measurements. For the reliability tests, the gate driver was exposed to the target ambient temperature for more than 336 hours (2 weeks).

In order to minimize possible board and interconnect failures that may cause the test to end prematurely, a PCB was utilized that was less complex than the standard test board (see Figure A.6 in the Appendix). Also, because this test board needed to be placed in the oven (as tape heaters would likely fail over the test's duration) the board was made of high-temperature capable polyimide material, as opposed to FR-4. Additionally, a minimum number of components were placed on the test board to limit potential failures, and jumpers were replaced with wires. The configuration used for the reliability test is shown in Figure 4.44.

Figure 4.45 shows the initial data taken for the 336 hour 200°C test. For this experiment, the input of the gate driver was set at 1 kHz, and V_{DDH} was 20 V. After 336 hours, the gate driver was still functional, as shown in Figure 4.46. The gate voltage and gate current measurements were nearly identical, while the slight (less than 2%) change in gate current can be attributed to degradation of the wiring and interconnect in the oven over the extended test period.

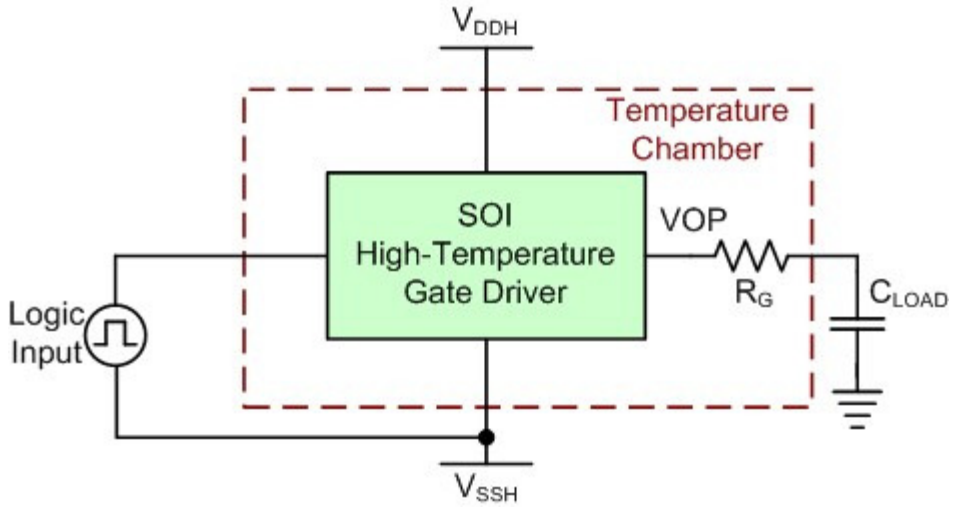


Figure 4.44. Reliability test configuration.

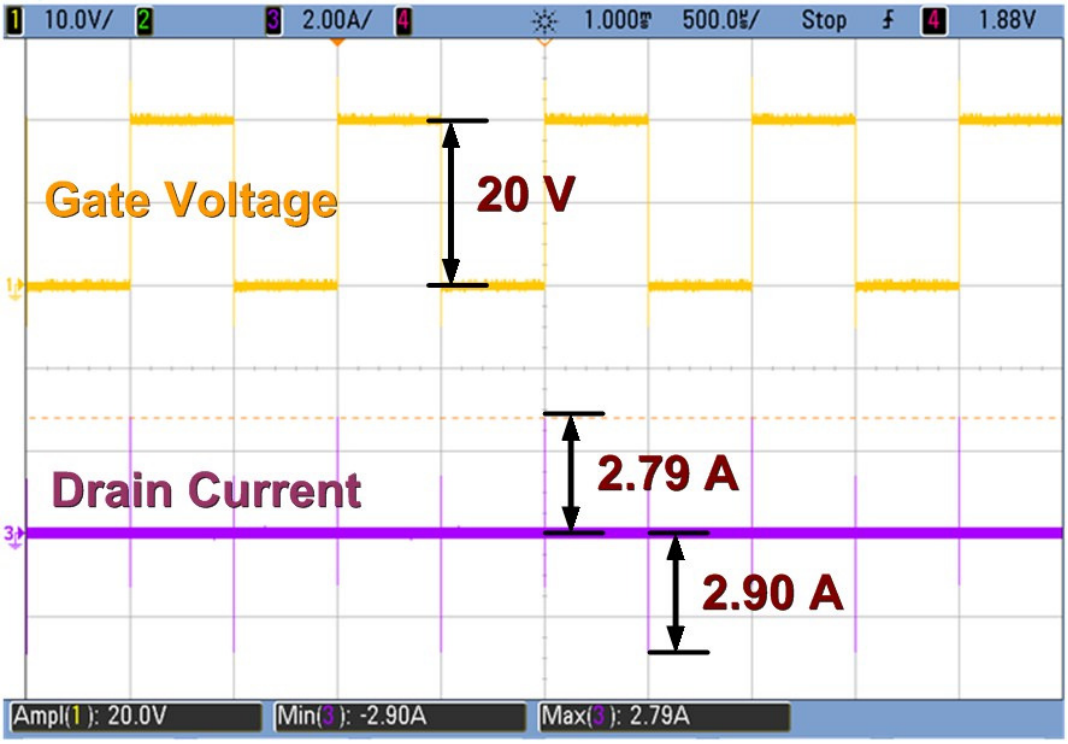


Figure 4.45. 200°C reliability test at start.

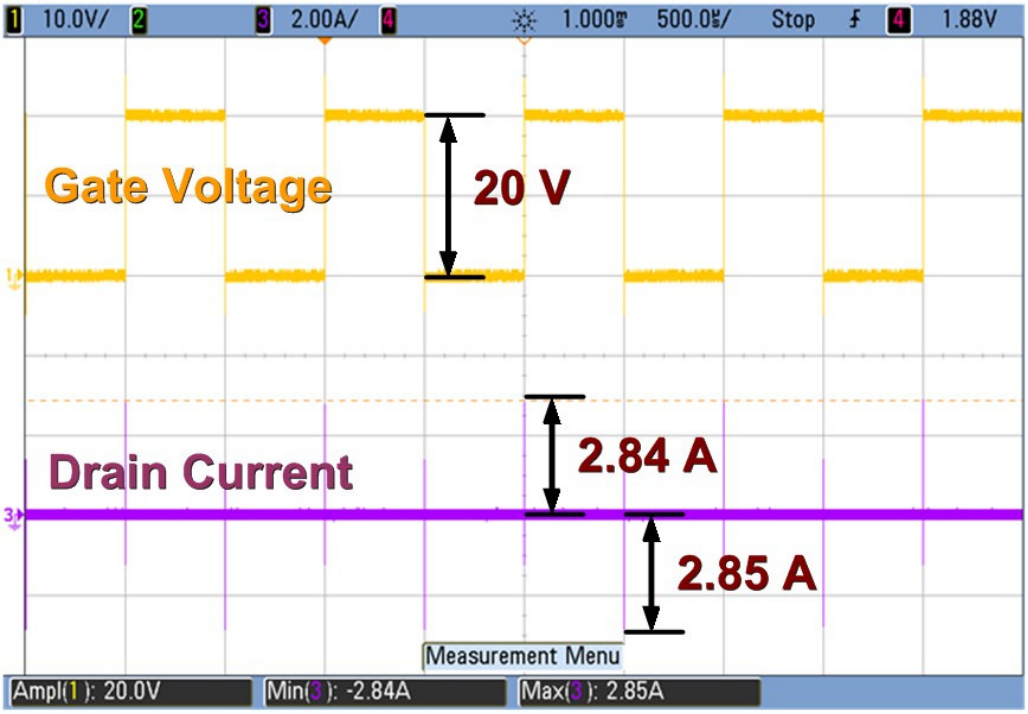


Figure 4.46. 200°C reliability test at 336 hours.

The 225°C reliability test did not succeed on the first attempt. The on-board bypass capacitors supplying transient current and power supply noise tolerance to the gate driver failed within days of being placed in the oven and had to be removed. Also, several solder joints failed and required new test boards to be constructed. Once these problems were overcome, the gate driver was left in the oven at 225°C for more than 400 hours. Results demonstrating the gate driver operating at the start and end of this test are given in Figure 4.47 and Figure 4.48. Again, the small decrease in gate current can be attributed to wiring and interconnect degradation.

Figure A.7 in the Appendix shows the status of the test board after the completion of the extended 400 hour 225°C testing. Note the change in color from green to brown. The board and solder joints also became more brittle over the course of the test, with the gate resistor breaking from the board while it was being removed from the temperature chamber.

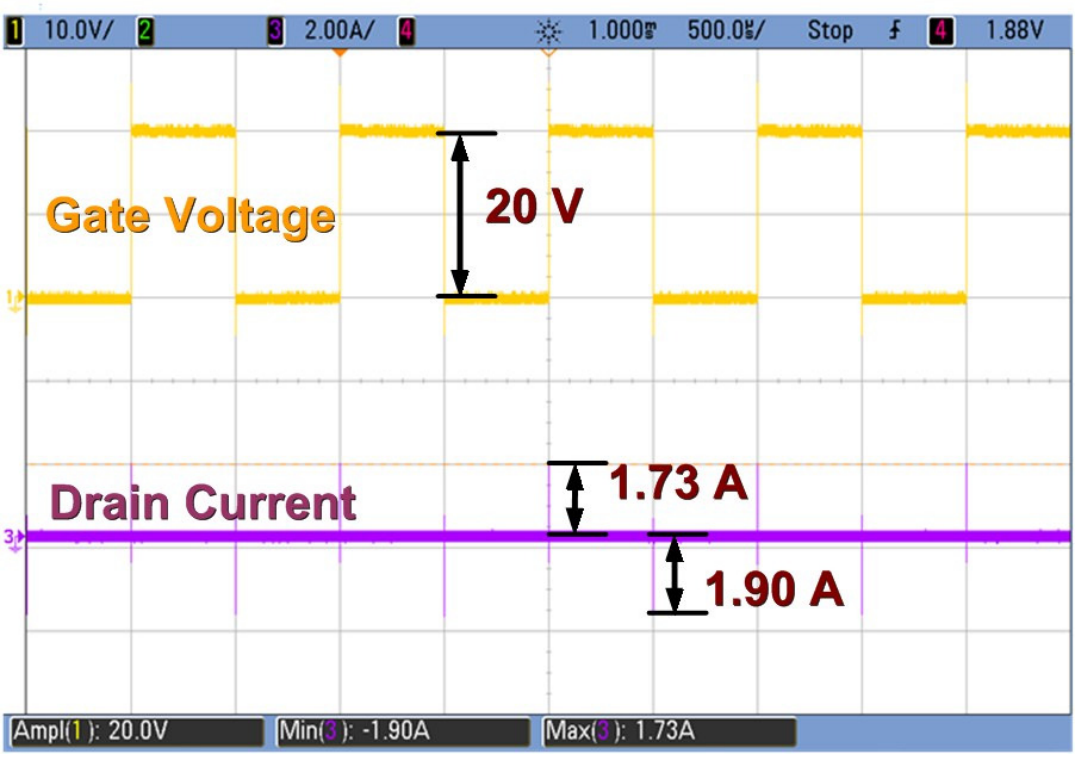


Figure 4.47. 225°C reliability test at start.

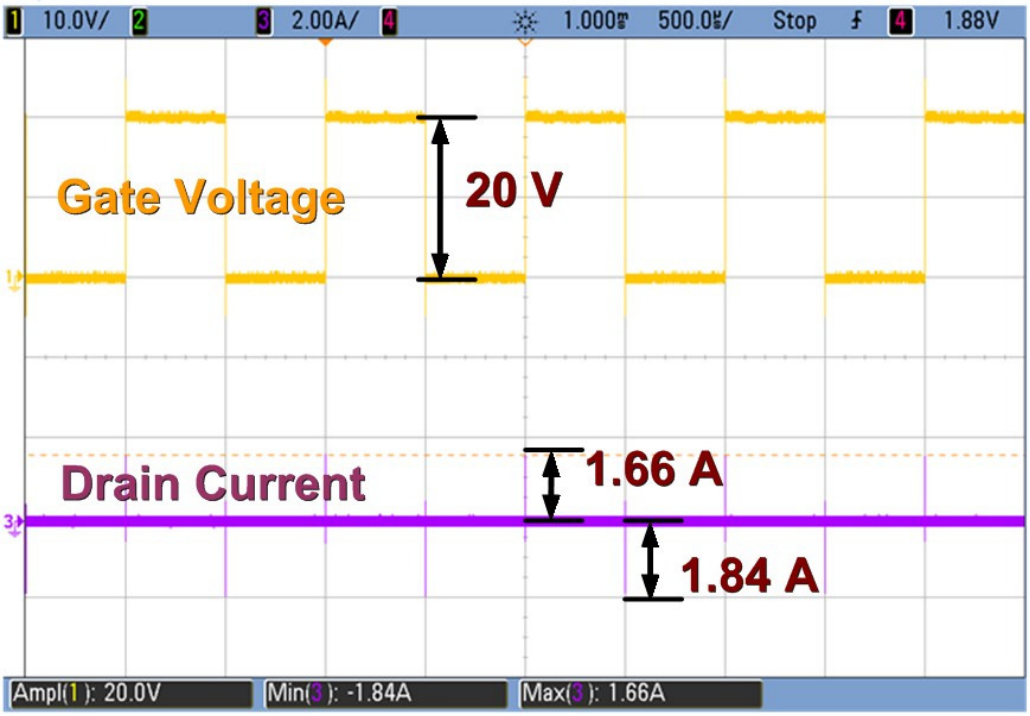


Figure 4.48. 225°C reliability test at 400 hours.

CHAPTER 5

Conclusions

In this paper, the design of a high-temperature, high-voltage, silicon-on-insulator based gate driver was demonstrated and measurement results were presented. The specifications for the gate driver, listed in Table 5.1, meet or exceed the design goals established in Chapter 1. This includes the successful operation of the prototype across a wide temperature range, from −55°C to more than 200°C. Original contributions of the work include:

- Design and implementation of an integrated charge pump enabling 100% high-side duty cycle operation of the gate driver across a wide temperature range. This circuit requires no off-chip control signals or components.
- Demonstration of an output current drive of more than 4 A at 200°C and more than 5 A at −55°C using the on-chip output drivers. Compared to previous work, this was accomplished through the utilization of a larger aspect ratio LDMOS "totem-pole" output stage, reduced on-chip parasitics, and reduced self-heating effects.
- Development of a highly integrated gate driver integrated circuit, requiring a minimum complement of off-chip passive components. This has not been previously presented for a gate driver IC capable of operating across a wide temperature range. A list of the major circuit blocks integrated on the gate driver IC is presented in Table 5.2.

Although this gate driver was designed for automotive applications, it could also be utilized in numerous harsh environment applications in which conventional bulk silicon-based devices cannot deliver an efficient, cost-effective solution. To enable the integration of wide-bandgap power devices into high-temperature power electronic modules, SOI-based integrated circuits capable of operating at ambient temperature above 150°C are needed to interface with control circuitry. The high-temperature, high-voltage gate driver integrated circuit presented in this dissertation can help to facilitate that goal.

Table 5.1. Specifications.

Parameter	*Corinth* Specification
Operating Temperature Range	–55°C to > 200°C
Output Voltage Range	10 V to 30 V ($V_{DDH} - V_{SSH}$)
Current Drive	Sourcing: 5.5 A at –55°C, 4.5 A at 200°C Sinking: 6.0 A at –55°C, 5.0A at 200°C
Operating Frequency Range	Minimum: DC (100% high-side duty cycle) Maximum: > 200 kHz (> 550 kHz measured with adjusted V_{DD_CP})
Integration	Die: 8.8 mm x 5 mm Major circuit blocks integrated on-chip are listed in Table 5.2. Includes regulator and charge pump capacitors.

Future Work

Subsequent iterations of the high-temperature integrated gate driver should incorporate findings from this research to enhance performance. This would include optimizing the supply voltage provided to the charge pump by the on-chip voltage regulator to facilitate a more stable floating high-side supply across temperature. Also, the incorporation of additional circuitry onto the gate drive IC, such as high-temperature galvanic input isolation and crosstalk mitigation, is under investigation. Research is already underway on a project to design an integrated power module that will use technology developed for this gate driver to create a high efficiency smart power module utilizing wide-bandgap power switches.

Table 5.2. Major circuit blocks integrated on *Corinth*.

Major Circuit Blocks	Description
Input Stage	Schmitt trigger buffer and fault shutdown circuitry
Dead-Time Controller	Generates non-overlapping waveforms for output drivers (prevents crowbar current)
Edge Detector	Creates narrow pulses from high-side driver control signal
Level Shifter	Shifts pulses for high-side driver to high-side voltage levels
SR Latch	Recreates control signal for the high-side driver
Output Driver Buffers	Buffers the control signals for the output drivers
M_L & M_H	Low-side and high-side output drivers
Charge Pump	Supplies floating power rail for high-side circuitry
Voltage Regulators	Creates 5-V and charge pump supply voltages for the gate driver from the V_{DDH} supply rail
Temperature Sensor	Detects an over-temperature event
Under Voltage Lock Out (UVLO)	Detects an under-voltage event
Short Circuit Detection	Detects a high-current event on the power switch by monitoring a sense resistor
De-saturation Detection	Detects a de-saturation (high current) event by monitoring the power devices V_{CE} or V_{DS}
Gate Current Monitoring	Detects a high gate current event by monitoring a sense resistor
Low Voltage Differential Signaling (LVDS) Receiver	Generates a single-ended signal from a low-voltage differential signal

LIST OF REFERENCES

[1] S. Lande, "Supply and demand for high temperature electronics," *The Third European Conference on High Temperature Electronics*, pp. 133-135, 1999.

[2] P. L. Dreike, D. M Fleetwood, D. B. King, D. C. Sprauer, and T. E. Zipperian, "An overview of high-temperature electronic device technologies and potential applications," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, vol. 17, no. 4, pp. 594-609, Dec 1994.

[3] F. S. Shoucair, "Potential and problems of high-temperature electronics and CMOS integrated circuits (25 - 250 °C) - an overview," *Microelectronics Journal*, vol. 22, no. 2, pp. 39-54, April 1991.

[4] R. W. Johnson, J. L. Evans, P. Jacobsen, and R. Thompson, "High-temperature automotive electronics," *Proceedings of the International Conference on Advanced Packaging and Systems*, pp. 77-87, March 2002.

[5] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. Thompson, and M. Christopher, "The changing automotive environment: high-temperature electronics," *IEEE Transactions on Electronics Packaging Manufacturing,* vol. 27, no. 3, pp. 164-176, July 2004.

[6] R. Sharp, "The current status of high temperature electronics for automotive use," *IEE Seminar on Automotive Electronic Standards*, pp. 6/1-6/5, June 1999.

[7] M. A. Huque, "A high-temperature, high-voltage SOI gate driver integrated circuit with high drive current for silicon carbide power switches," *Ph.D. Dissertation*, University of Tennessee, 2010.

[8] U.S. Department of Energy, U.S. Drive Partnership, "Electrical and electronics technical team roadmap," Dec 2010.

[9] J. G. Kassakian, "Automotive electrical systems – the power electronics market of the future," *IEEE Applied Power Electronics Conference and Exposition*, pp. 3-9, 2000.

[10] A. Emadi, Y. J. Lee, and K. Rajashekara, "Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 6, pp. 2237-2245, June 2008.

[11] M. Kumari, P. R. Thakura, and D. N. Badodkar, "Role of high power semiconductor devices in hybrid electric vehicles," *India International Conference on Power Electronics*, pp. 1-7, Jan 2011.

[12] H. Moghbelli, A. Niasar, and R. Langari, "New generation of passenger vehicles: FCV or HEV?," *IEEE International Conference on Industrial Technology*, pp. 452-459, Dec 2006.

[13] S. S. Williamson and A. Emadi, "Comparative assessment of hybrid electric and fuel cell vehicles based on comprehensive well-to-wheels efficiency analysis," *IEEE Transactions on Vehicular Technology*, vol. 54, no. 3, pp. 856-862, May 2005.

[14] G. Leen and D. Heffernan, "Expanding automotive electronic systems," *Computer*, vol. 35, no. 1, pp. 88-93, Jan 2002.

[15] K. J. Kelly, T. Abraham, K. Bennion, D. Bharathan, S. Narumanchi, and M. O'Keefe, "Assessment of thermal control technologies for cooling electric vehicle power electronics," *23rd International Electric Vehicle Symposium*, Dec 2007.

[16] M. Ehsani, Y. Gao, and J. Miller, "Hybrid electric vehicles: Architecture and motor drives," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 719-728, April 2007.

[17] M. Marchesoni and C. Vacca, "New DC - DC converter for energy storage system interfacing in fuel cell hybrid electric vehicles," *IEEE Transactions on Power Electronics,* vol. 22, no. 1, pp. 301-308, Jan 2007.

[18] A. Elasser and T. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 969-986, June 2002.

[19] H. Zhang, L. M. Tolbert, and B. Ozpineci, "Impact of SiC devices on hybrid electric and plug-in hybrid electric vehicles," *IEEE Transactions on Industry Applications,* vol. 47, no. 2, pp. 912-921, March 2011.

[20] Z. J. Shen and I. Omura, "Power semiconductor devices for hybrid, electric, and fuel cell vehicles," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 778-789, April 2007.

[21] P. G. Neudeck, "SiC technology," in *The VLSI Handbook*, W. K. Chen, Ed., CRC Press, Boca Raton, Florida, pp. 5.1-5.34, 2007.

[22] P. Neudeck, R. Okojie, and L.-Y. Chen, "High-temperature electronics - a role for wide bandgap semiconductors?," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1065-1076, Jun 2002.

[23] J. Colinge, "SOI for hostile environment applications," *IEEE International SOI Conference,* pp. 1-4, Oct 2004.

[24] S. Cristoloveanu, "Silicon on insulator technology," in *The VLSI Handbook*, W. K. Chen, Ed. CRC Press, Boca Raton, Florida, pp. 4.1-4.15, 2000.

[25] Telefunken Semiconductors GmbH & Co. KG, http://www.telefunkensemi.com

[26] X-FAB Semiconductor Foundries AG, http://www.xfab.com

[27] Honeywell International Inc., http://www.honeywell.com

[28] J. Valle-Mayorga, C. Gutshall, K. Phan, I. Escorcia-Carranza, A. Mantooth, B. Reese, M. Schupbach, and A. Lostetter, "High temperature silicon-on-insulator gate driver for SiC-FET power modules," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, Nov 2012.

[29] A. A. Fomani, Wai Tung Ng, and A. Shorten, "An integrated segmented gate driver with adjustable driving capability," *IEEE Energy Conversion Congress and Exposition*, pp. 2430-2433, Sept 2010.

[30] F. Li, D. Giannopoulos, and I. Wacyk, "A low loss high-frequency half-bridge driver with integrated power devices using EZ-HV SOI technology," *IEEE Applied Power Electronics Conference and Exposition*, pp. 1127–1132, March 2002.

[31] J. M. Park, E. D. Kim, S. C. Kim, N. K. Kim, W. Bahng, G. H. Song, and S. B. Han, "A monolithic IGBT gate driver for intelligent power modules implemented in 0.8 µm high voltage (50 V) CMOS process," *Microelectronics Journal*, vol. 32, no. 5-6, pp. 537-541, 2001.

[32] V. Nguyen, P. O. Jeannin, J. C. Crebier, and J. Schanen, "A new compact, isolated and integrated gate driver using high frequency transformer for interleaved boost converter," *IEEE Energy Conversion Congress and Exposition,* pp. 1889-1896, Sept 2011.

[33] B. Wang, M. Riva, J. Bakos, and A. Monti, "Integrated circuit implementation for a GaN HFETs driver circuit," *IEEE Applied Power Electronics Conference and Exposition*, pp. 901-906, Feb 2008.

[34] B. Wang, M. Riva, J. D. Bakos, and A. Monti, "Integrated circuit implementation for a GaN HFET driver circuit," *IEEE Transactions on Industry Applications*, vol. 46, no. 5, pp. 2056-2067, Sept 2010.

[35] S. Timothé, R. Nicolas, and C. Jean-Christophe, "Design and characterization of an integrated CMOS gate driver for vertical power MOSFETs," *Energy Conversion Congress and Exposition*, pp. 2206-2213, Sept 2010.

[36] S. Timothe, R. Nicolas, C. Jean-Christophe, and A. Jean-Daniel, "Design and characterization of a signal insulation coreless transformer integrated in a CMOS gate driver chip," *International Symposium on Power Semiconductor Devices and ICs*, pp. 360-363, May 2011.

[37] L. Dulau, S. Pontarollo, A. Boimond, J.-F. Garnier, N. Giraudo, and O. Terrasse, "A new gate driver integrated circuit for IGBT devices with advanced protections," *IEEE Transactions on Power Electronics,* vol. 21, no. 1, pp. 38-44, Jan 2006.

[38] S. Nagai, N. Negoro, T. Fukuda, N. Otsuka, H. Sakai, T. Ueda, T. Tanaka, and D. Ueda, "A DC-isolated gate drive IC with drive-by-microwave technology for power switching devices," *Solid-State Circuits Conference Digest of Technical Papers,* pp. 404-406, Feb 2012.

[39] A. Perez, X. Jorda, P. Godignon, M. Vellvehi, J. L. Galvez, and J. Millan, "An IGBT gate driver integrated circuit with full-bridge output stage and short circuit protections," *International Semiconductor Conference*, Sept 2003.

[40] J. Millan, A. Perez-Tomas, and X. Jorda, "A cost-effective high-voltage p-channel MOSFET implemented in a standard twin-tub technology: integrated IGBT gate driver," *IEEE International Symposium on Industrial Electronics*, pp. 479-484, June 2005.

[41] R. Wang, M. Danilovic, D. Boroyevich, Z. Chen, and R. Kaushik, "Transformer-isolated gate drive design for SiC JFET phase-leg module," *Energy Conversion Congress and Exposition,* pp. 1728-1733, Sept 2011.

[42] F. Xu, D. Jiang, J. Wang, F. Wang, L. M. Tolbert, T. J. Han, J. Nagashima, and S. J. Kim, "High temperature packaging of 50 kW three-phase SiC power module," *IEEE 8th International Conference on Power Electronics and ECCE Asia,* pp. 2427-2433, May 2011.

[43] M. L. Heldwein and J. W. Kolar, "A novel SiC J-FET gate drive circuit for sparse matrix converter applications," *IEEE Applied Power Electronics Conference and Exposition*, pp. 116-121, 2004.

[44] I. W. Hofsajer, A. Melkonyan, M. Mantel, S. Round, and J. W. Kolar, "A simple, low cost gate drive method for practical use of SiC JFETs in SMPS," *European Conference on Power Electronics and Applications,* 2005.

[45] K. Mino, S. Herold, and J. W. Kolar, "A gate drive circuit for silicon carbide JFET," *The 29th Annual Conference of the IEEE Industrial Electronics Society*, pp. 1162-1166, Nov 2003.

[46] B. Wrzecionko, S. Kach, D. Bortis, J. Biela, and J. W. Kolar, "Novel AC coupled gate driver for ultra fast switching of normally-off SiC JFETs," *36th Annual Conference on IEEE Industrial Electronics Society*, pp. 605-612, Nov 2010.

[47] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, and P. Friedrichs, "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter*," Industry Applications Conference*, pp. 410-416, Oct 2005.

[48] S. Waffler, S. D. Round, and J. W. Kolar, "High temperature (>200°C) isolated gate drive topologies for Silicon Carbide (SiC) JFET," *Industrial Electronics Conference*, pp. 2867-2872, Nov 2008.

[49] CISSOID S. A., http://www.cissoid.com/

[50] CISSOID S. A., "High-temperature full-bridge driver," CHT-PALLAS datasheet, Rev. 2.3, Nov 2010.

[51] CISSOID S. A., "High temperature half-bridge driver (high side and low side)," CHT-HYPERION datasheet, Rev. 1.1, March 2011

[52] CISSOID S. A., "Power transistor driver controller," CHT-THEMIS datasheet, Rev. 2.1, Oct 2012.

[53] CISSOID S. A., "Dual channel power transistor driver," CHT-ATLAS datasheet, Rev 3.2, Sept 2012.

[54] CISSOID S. A., "High-temperature half-bridge isolated gate-driver dedicated to SiC MOSFETs," EVK-HADES product brief, Rev 1.1, Oct 2011.

[55] M. Huque, R. Vijayaraghavan, M. Zhang, B. Blalock, L. Tolbert, and S. Islam, "An SOI-based high-voltage, high-temperature gate-driver for SiC FET," *IEEE Power Electronics Specialist Conference*, pp. 1491-1495, June 2007.

[56] M. A. Huque, B. J. Blalock, C. Su, R. Vijayaraghavan, S. K. Islam, and L. M. Tolbert, "SOI based integrated circuits for high-temperature applications," *International Conference on High Temperature Electronics*, May 2008.

[57] M. A. Huque, L. M. Tolbert, B. J. Blalock, and S. K. Islam, "A high-temperature, high-voltage SOI gate driver IC with high output current and on-chip low-power temperature sensor," *International Symposium on Microelectronics*, Nov 2009.

[58] R. L. Greenwell, B. M. McCue, L. Zuo, M. A. Huque, L. M. Tolbert, B. J. Blalock, S. K. Islam, "SOI-based integrated circuits for high-temperature power electronics applications," *IEEE Applied Power Electronics Conference and Exposition*, pp. 836-843, March 2011.

[59] R. L. Greenwell, B. M. McCue, L. Zuo, M. A. Huque, B. J. Blalock, L. M. Tolbert, and S. K. Islam, "Universal gate drive IC for harsh environments," *Government Microcircuit Applications & Critical Technology Conference*, pp. 327-330, March 2011.

[60] B. M. McCue, R. L. Greenwell, M. I. Laurence, B. J. Blalock, S. K. Islam, and L. M. Tolbert, "SOI based voltage regulator for high-temperature applications," *IMAPS International Conference on High Temperature Electronics*, pp. 207-213, May 2012.

[61] R. L. Greenwell, B. M. McCue, M. I. Laurence, C. L. Fandrich, B. J. Blalock, L. M. Tolbert, and S. K. Islam, "SOI-based integrated gate driver circuit for high-temperature applications," *IMAPS International Conference on High Temperature Electronics*, pp. 233-244, May 2012.

[62] R. L. Greenwell, B. M. McCue, B. J. Blalock, L. M. Tolbert, and S. K. Islam, "High-temperature SOI-based gate driver IC for WBG power switches," *Accepted to IEEE Applied Power Electronics Conference and Exposition*, March 2013.

[63] S. Park and T. M. Jahns, "A self-boost charge pump topology for a gate drive high-side power supply," *IEEE Transactions on Power Electronics*, vol. 20, no. 2, pp. 300-307, March 2005.

[64] W. T. Ng, O. Trescases, and G. Wei, "Integrated power stages for switched mode power supplies," *International Symposium on Power Electronics*, Nov 2007.

[65] J. R. Baker, *CMOS Circuit Design, Layout, and Simulation, Third Edition*, New York, Wiley-IEEE, 2010.

[66] F. Alimenti, P. Mezzanotte, L. Roselli, and R. Sorrentino, "Modeling and characterization of the bonding-wire interconnection," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 1, pp. 142-150, Jan 2001.

[67] R. K. Ulrich and W. D. Brown, *Advanced Electronic Packaging,* Hoboken, NJ, Wiley, 2006.

[68] M. L. Minges and ASM International Handbook Committee, *Electronic Materials Handbook: Packaging*, ASM International, 1989.

[69] L. Zuo, S. K. Islam, M. A. Huque, C. Su, B. J. Blalock, and L. M. Tolbert, "A universal BCD-on-SOI based high temperature short circuit protection for SiC power switches," *International Conference on High Temperature Electronics*, May 2010.

[70] M. W. Jawitz, *Printed Circuit Board Materials Handbook*, New York, NY, McGraw Hill, 1997.

[71] C. A. Harper and R. M. Sampson, *Electronic Materials & Processes Handbook*, New York, NY, McGraw Hill, 1994.

[72] M. Bhushan, A. Gattiker, M. B. Ketchen, and K. K. Das, "Ring oscillators for CMOS process tuning and variability control," *IEEE Transactions on Semiconductor Manufacturing*, vol. 19, no. 1, pp. 10-18, Feb 2006.

[73] M. Chinthavali, P. Ning, Y. Cui, and L. M. Tolbert, "Investigation on the parallel operation of discrete SiC BJTs and JFETs," *IEEE Applied Power Electronics Conference and Exposition*, pp. 1076-1083, March 2011.

APPENDIX

Table A.1. Table of acronyms.

Acronym	Definition	Acronym	Definition
AlGaN	aluminum gallium nitride	**IGBT**	insulated gate bipolar junction transistor
BCD	bipolar CMOS DMOS	**JFET**	junction gate field effect transistor
BCD-on-SOI	bipolar-CMOS-DMOS on silicon-on-insulator	**LDMOS**	laterally diffused metal oxide semiconductor
BJT	bipolar junction transistor	**LN_2**	liquid nitrogen
CMOS	complementary metal oxide semiconductor	**MOSCAP**	metal oxide semiconductor capacitor
COB	chip-on-board	**MOSFET**	metal oxide semiconductor field effect transistor
DIP	double inline package	**NMOS**	negative-channel metal oxide semiconductor
DMOS	double-diffused metal oxide semiconductor	**PCB**	printed circuit board
DRC	design rule check	**PGA**	pin-grid array
ED-pMOSFET	p-channel extended drain metal-oxide semiconductor field effect transistor	**PHEV**	plug-in hybrid electric vehicle
EMI	electromagnetic interference	**PM or PM bars**	process monitoring bars
EMRC	electromagnetic resonant coupler	**PMOS**	positive-channel metal oxide semiconductor
FCV	fuel cell vehicle	**PTFE**	polytetrafluoroethylene
FET	field effect transistor	**RTD**	resistance temperature detectors
GaN	gallium nitride	**Si**	silicon
HEV	hybrid electric vehicle	**SiC**	silicon carbide
HTNFET	high-temperature n-channel power field effect transistor	**SJT**	super junction transistor
HVCMOS	high-voltage complementary metal oxide semiconductor	**SOI**	silicon-on-insulator
IC	integrated circuit	**UVLO**	under-voltage lock out
ICE	internal combustion engine	**WBG**	wide-bandgap

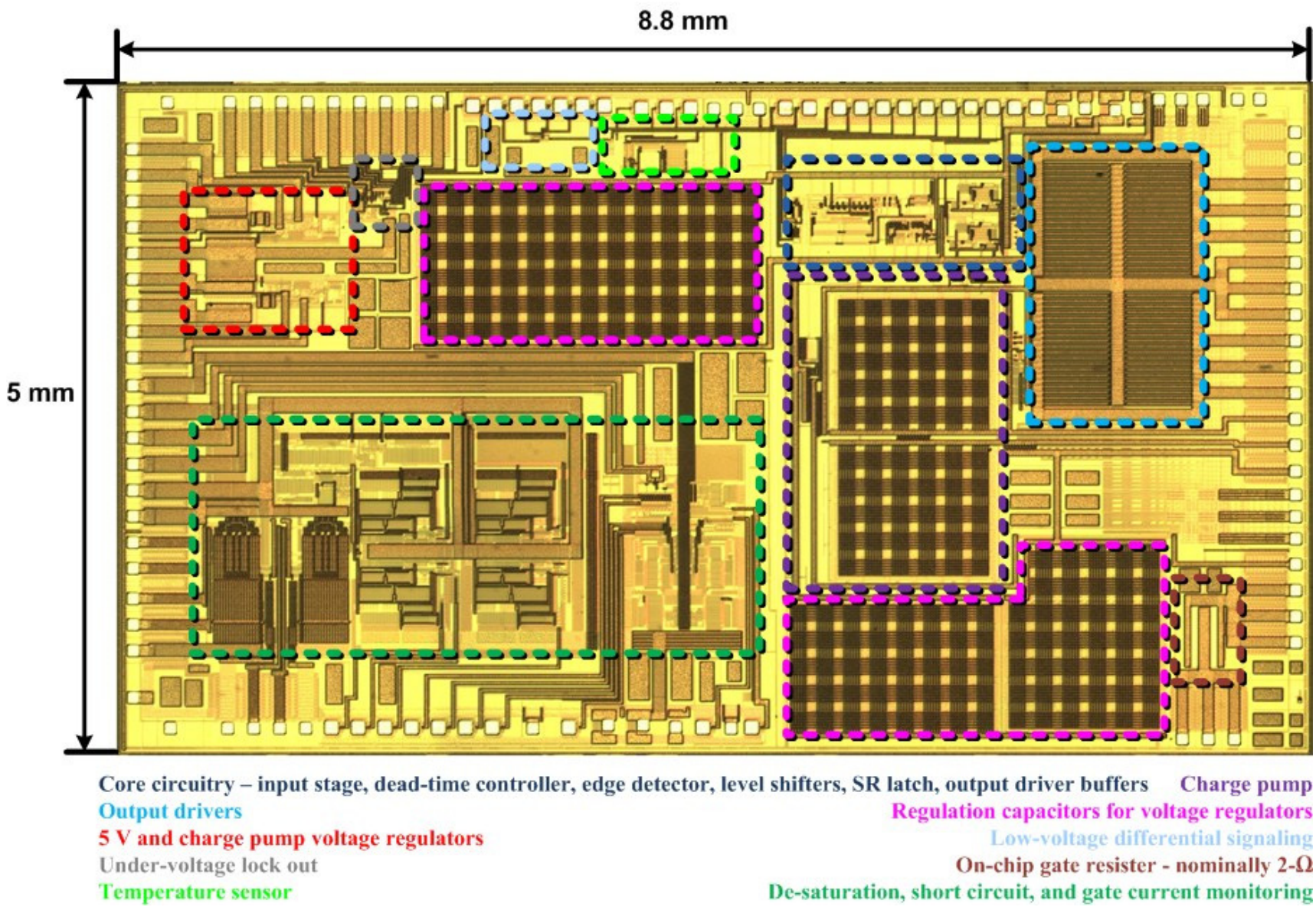


Figure A.1. Annotated *Corinth* micrograph.

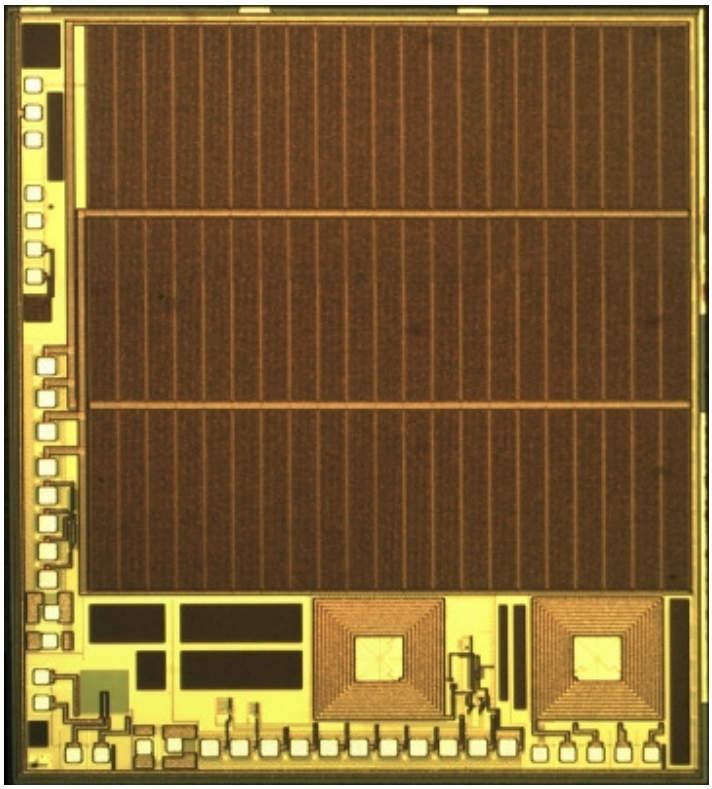


Figure A.2. Chip 2 micrograph.

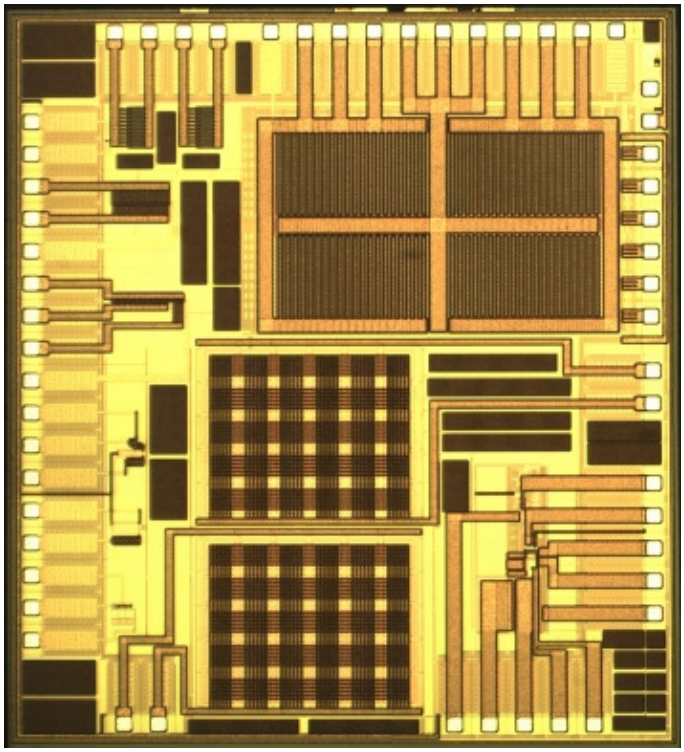


Figure A.3. Chip 3b micrograph.

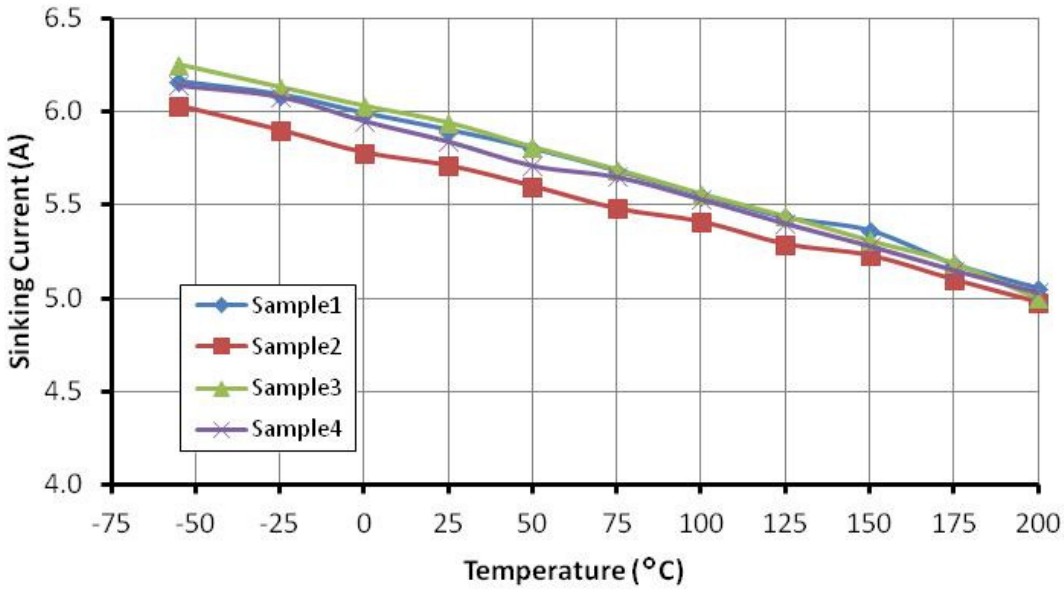


Figure A.4. Sinking currents across temperature with 1-Ω R_G.

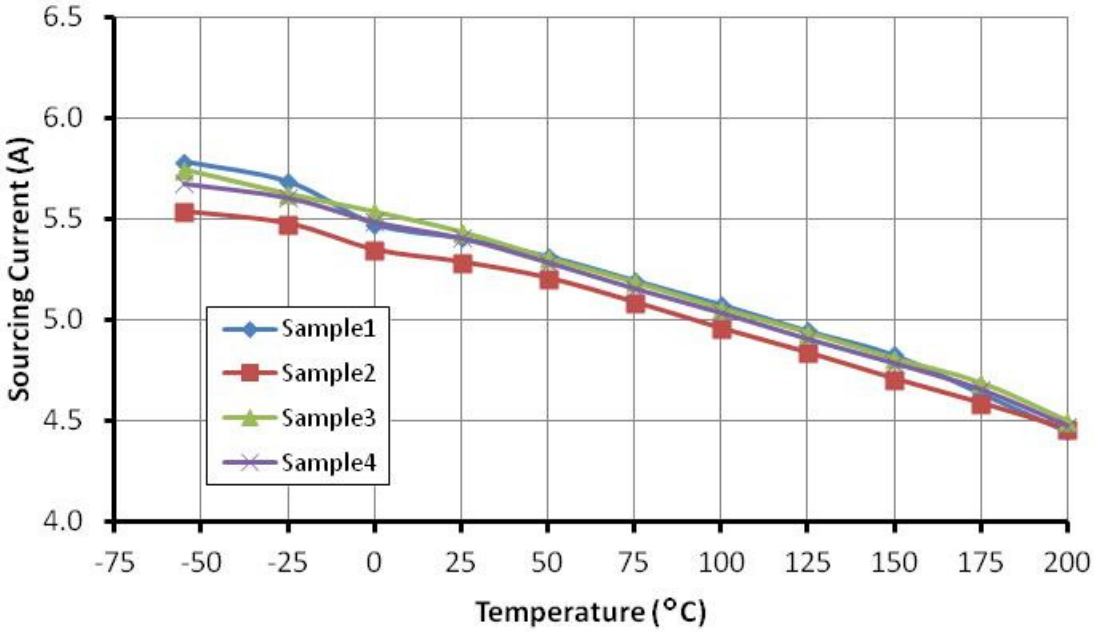


Figure A.5. Sourcing currents across temperature with 1-Ω R_G.

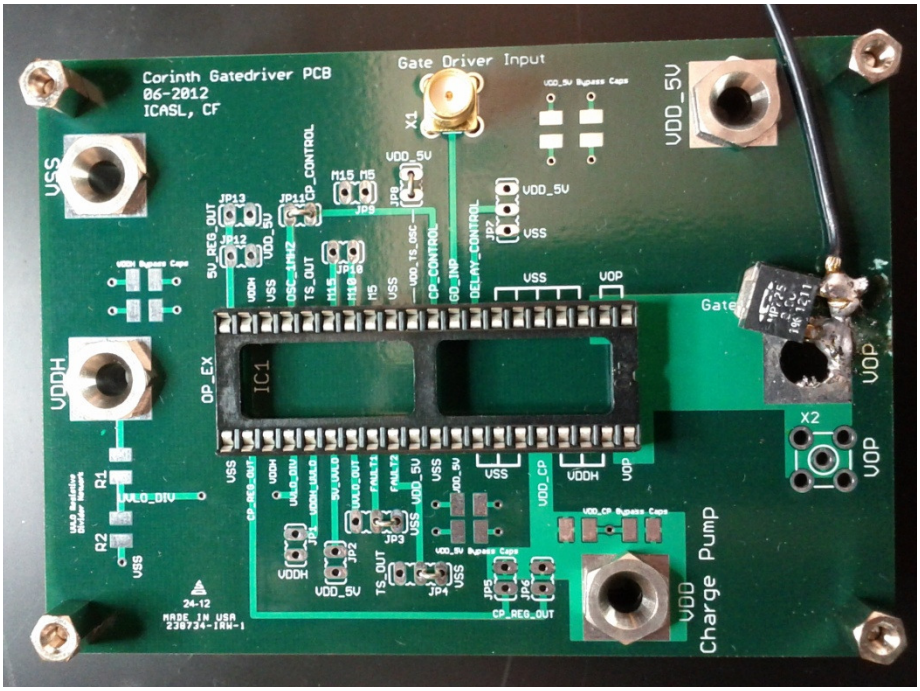


Figure A.6. 225°C reliability test board at test start.

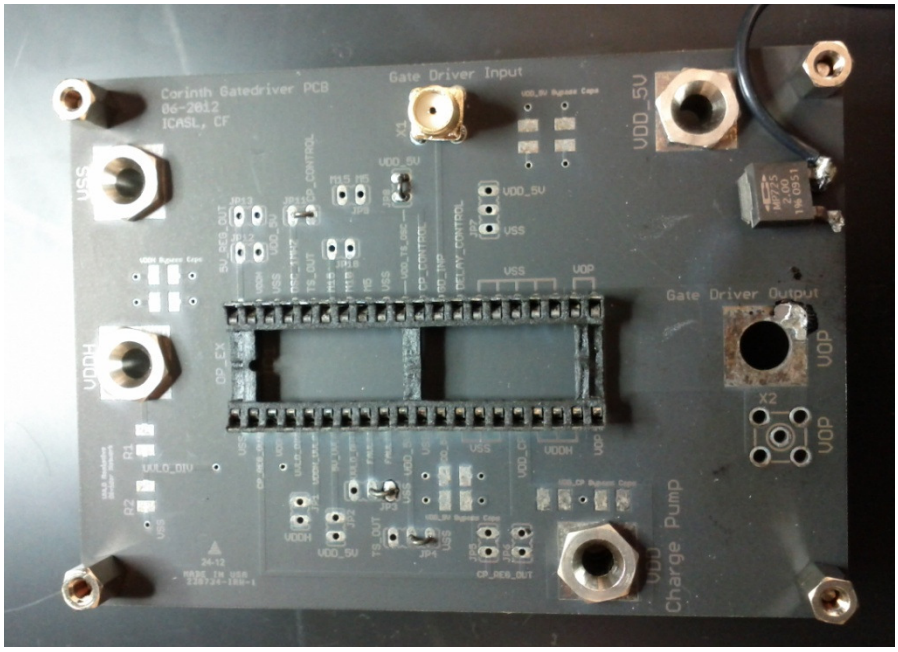


Figure A.7. 225°C reliability test board at 400 hours.

VITA

Robert Lee Greenwell II was born in Garden City, MI, to parents Robert and Linda Greenwell. He attended David Crockett High School in Jonesborough, TN. After graduation, he enrolled at the University of Tennessee, Knoxville where he received his Bachelor of Science in Electrical Engineering in 2003. During his undergraduate career, Robert began working in the Integrated Circuits and Systems Laboratory (ICASL) at UT, where he continued to conduct research throughout his graduate studies. While an undergraduate, Robert also worked as a research assistant at Oak Ridge National Laboratory (ORNL). Robert earned his Master of Science in Electrical Engineering from UT in 2007. His thesis project, *Design of a 5-V Compatible Rail-To-Rail Input/Output Operational Amplifier in 3.3-V SOI CMOS for Wide Temperature Range Operation*, encompassed the design and implementation of a quad-operational amplified (QOA) integrated circuit for the Jet Propulsion Laboratory (JPL). Ninety-four of these QOA chips were used in the motor position encoders on-board the National Aeronautics and Space Administration's (NASA) Mars Science Laboratory (MSL) rover *Curiosity*. Robert earned his Doctor of Philosophy in Electrical Engineering at UT in 2012.

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