A Physics-Based Analytical Compact Model, TCAD Simulation, and Empirical SPICE Models of GaN Devices for Power Applications

A Thesis Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

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December 2018

ACKNOWLEDGEMENTS

I would like to express my appreciation to my advisor, Dr. Syed Kamrul Islam who has been provided the guidance and support necessary for me to develop as an electrical engineer and independence in my research call so that I can call this paper my own. I would also like to thank Dr. Leon M. Tolbert for helping me through the transition into electrical engineering graduate school and providing assistance through research and the wide bandgap program. Additionally, I appreciate the support of DOE for the Wide Bandgap Traineeship fellowship of which I was a part of in this research.

Secondly, thank you to my advisors and mentors at Oak Ridge National Laboratory- Curt Maxey, Yun Liu, and Willem Blokland- that showed me the true potential of the electrical engineering career and gave me the confidence to further pursue my degree. Those experiences and relationships have been invaluable and enriching to my academic and professional life.

Finally, I would like to thank my family and friends particularly my mother for supporting and encouraging my ambitions of being in STEM since I first knew I wanted to be a scientist.

ABSTRACT

The demand for high performance power electronics in consumer electronics, electric vehicle, aerospace, renewable energy is increasing and Si devices are failing to meet the demands of higher voltage, higher current, and high switching frequency efficiency.

Wide bandgap devices, SiC and GaN, offer an alternative solution since they can operate at higher temperatures. GaN in particular is only recently being developed commercially and has a higher mobility, saturation velocity, electric breakdown field, and bandgap. GaN experiences spontaneous and piezoelectric polarization which is exploited in the high electron mobility transistor (HEMT) topology by creating a two dimensional electron gas (2DEG) that forms naturally without the need for doping or voltage bias. This presents a problem for power electronics circuits since power devices should be enhancement-mode or normally-off for control and safety reasons. There are various topologies proposed to convert the device into a normally-off device. One such topology is the Gate Injection Transistor (GIT) whose operational effects has not been sufficiently investigated and much less modeled.

The GIT device is investigated via a TCAD Sentaurus simulation to understand the effects of various parameters unique to the GIT. Based on the TCAD simulation and model, an analytical compact model can be developed for a quick and more intuitive understanding of the GIT behavior. Finally, two commercial GaN devices, one a GIT and the other a HEMT, are empirically modeled in a SPICE simulator.

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CHAPTER 1: INTRODUCTION OF GaN DEVICES IN POWER APPLICATIONS

Why Wide Bandgap Devices?

The increasing need for energy delivery that is both sustainable, environmentally friendly, and practical has demanded innovative devices and technology for power electronic applications. Everything that uses electricity relies on power management which deems power electronics a fundamental industry. Power semiconductor devices are the core of power conversion applications and until recently have been dominated by silicon power MOSFETs [1]. Demands for greater power density, low on resistance, high temperature and high frequency performance are constrained by the use of conventional Si power MOSFETs as the inherent characteristics of the material have reached their limits. Many applications require solid state device operation in extremely harsh conditions which can be met by wide bandgap semiconductor devices [2]. Figure 1.1 shows various industry applications over time that can be improved by the adopting wide bandgap semiconductor technology. Current implementation of wide band gap semiconductor devices is driving improvement due to their amicable characteristics over Si. Figure 1.2 compares material properties of Si, SiC and GaN [3] which shows that GaN has a more favorable electric breakdown field, energy bandgap, saturated electron velocity, and electron mobility [4] compared to

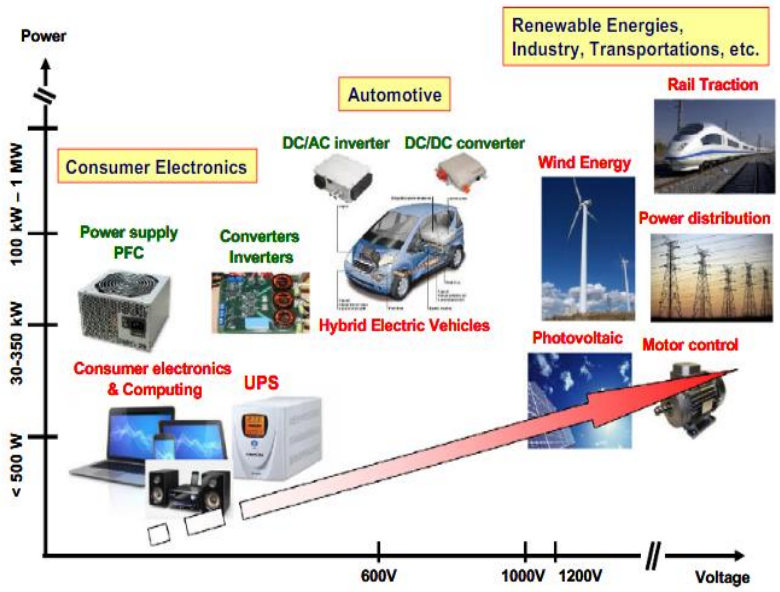

Figure 2.1: Current trends in electronics [1].

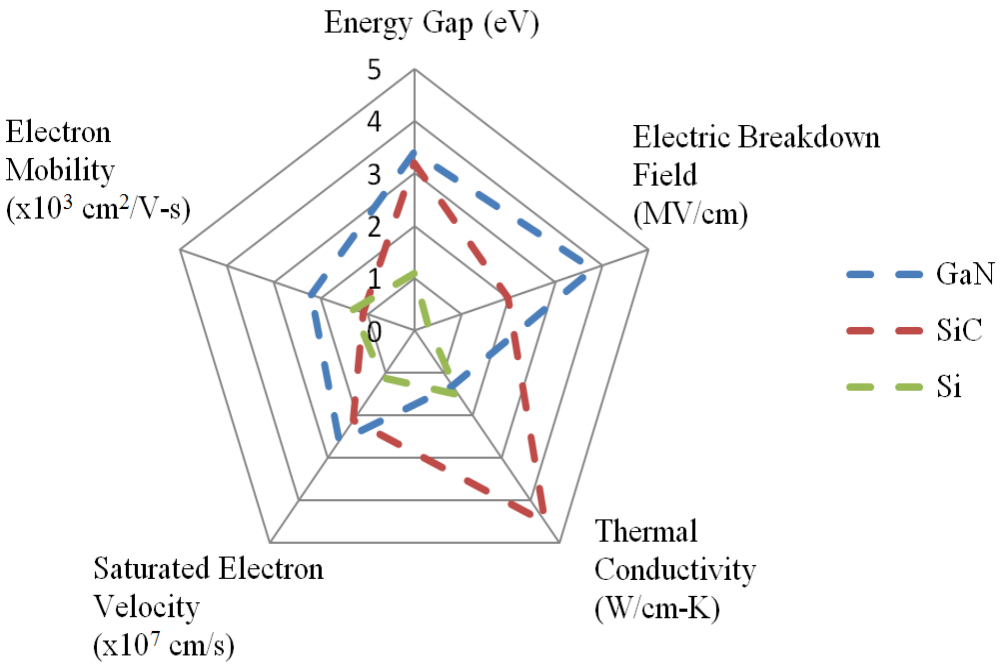

Figure 1.1: Comparison of wide bandgap materials [2]

others. However, GaN fairs poorly in terms of thermal conductivity. The high energy bandgap is useful for applications such as high temperature. Electrical breakdown field is useful to ensure that the device does not fail when exposed to high voltage across the drain and the source terminals when the device requires to be turned off. The high saturated electron velocity allows for a higher velocity of electrons which results in higher current density and high electron mobility is necessary for fast switching applications.

CHAPTER 2: LITERATURE REVIEW

Properties of GaN

GaN is available in two different crystal structures: wurtzite and zinc blende. The wurtzite GaN crystal is commonly used in GaN devices. The lattice structure is shown in Fig. 2.1 [5]. GaN possesses piezoelectric property which allows polarization to occur at the surface of the material when pressure is applied.

Wurtzite is considered more stable than zinc blend due to the iconicity and is commonly used in semiconductor devices. Table 1 shows the properties of wurtzite GaN that make it an appealing material in the use of power electronics [6].

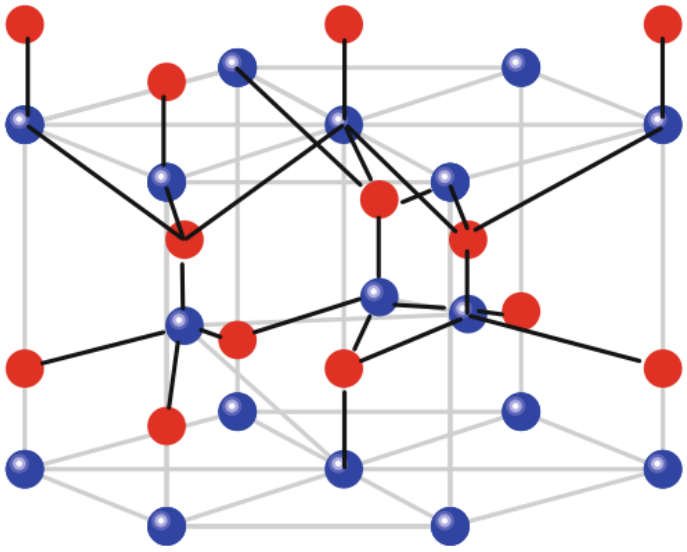

Figure 2.1: Wurtzite GaN structure used in GaN GIT devices [5].

Table 2.1: Properties of Wurtzite GaN [6]

Symbol	Parameter	Quantity
E_g [eV]	Bandgap	3.4
E_{crit} [V/cm]	Breakdown Electric Field	$5x10^6$
μ[cm2/Vs]	Mobility	≤1000
V_{sat}	Saturated electron velocity	$2.6x10^5$
K_C[W/cm°C]	Thermal conductivity	1.3

GaN HEMT Working Principle

Typically, GaN transistors are developed in high electron mobility transistor (HEMT) structure. Figure 2.2 shows the HEMT device structure which is also known as heterostructure FET (HFET) or modulation-doped FET (MODFET). The typical structure of the GaN high electron mobility transistor (HEMT) consists of either Si or SiC substrate lower cost compared to the alternatives. A buffer layer of AlGaN or GaN is grown on top of the substrate which helps mitigate electron punch-through effect [8]. Then a small layer of GaN with an AlGaN barrier layer forms a heterojunction which creates a 2DEG channel. The AlGaN layer has a differing lattice coefficient from the GaN layer proportional to the mole fraction of Al in AlGaN which creates a tensile strain on the GaN layer [9]. GaN is a piezoelectric material and the stresses from the lattice structural differences create

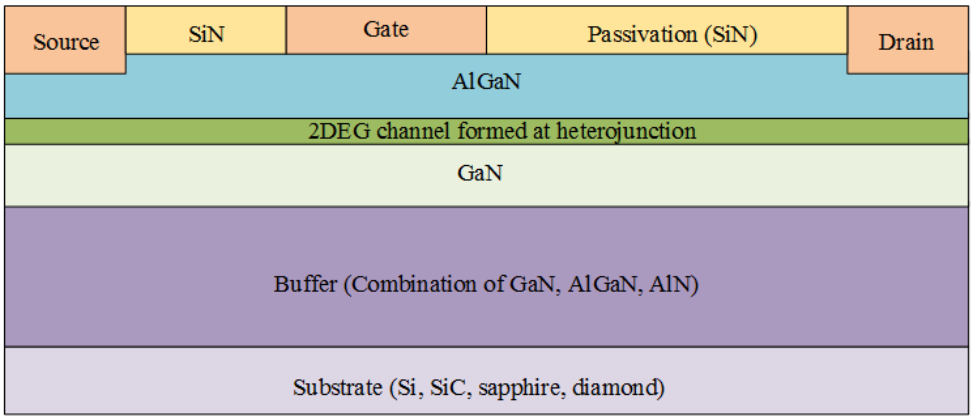

Figure 2.2: Typical structure of a GaN HEMT [7].

a piezoelectric and a spontaneous polarization in the heterojunction [10,11]. Due to the naturally forming channel achieved without dopants, the HEMT structure is capable of achieving high mobility by avoiding scattering due to the dopant atoms. The conduction band of the energy band diagram in depletion-mode HEMTs falls below the Fermi level at the heterojunction between AlGaN and GaN. Unfortunately, the heterojunction structure creates for a depletion mode device which is less than optimal for power device applications [12].

Gate Injection Transistor

There are various proposed models to achieve enhancement mode operation such as the recessed HEMT where the AlGaN layer is reduced in thickness to decrease the 2DEG until there is a positive threshold voltage. This can reduce the current density in the transistor which is less than optimal for power FETs. A promising alternative is the gate injection transistor (GIT) which is

emerging commercially and consequently motivates the interest for a comprehensive understanding of the GaN-GIT.

The HEMT structure is necessary to understand the altered GIT device structure. Figure 2.3 shows the altered structure to the HEMT by the addition of the *p*-doped GaN layer underneath the gate electrode to create the GIT.

The *p*-doped layer raises the conduction band in the channel region above the Fermi level thereby depleting the channel with no bias voltage applied. Like the band diagram for the recessed HEMT, the conduction band is above the Fermi level at zero gate bias transforming the device into an enhancement-mode device. In the case of the recessed HEMT, the thin AlGaN layer corresponds with a smaller drop in the energy band in that region. For the GIT, the conduction band offset between the *p*-GaN and AlGaN raise the conduction band. Further increase of the gate voltage exceeding the threshold voltage results in hole-injection into the channel from the *p*-doped region. This behvior is shown in Figure 2.4. At zero gate bias the channel undeneath the *p*-GaN is depleted. Once the gate voltage is

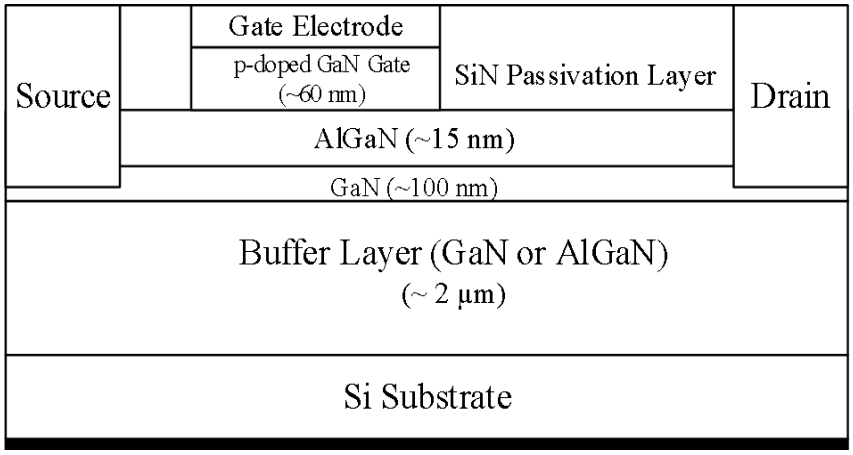

Figure 2.3: Structure of a GaN gate injection transistor (GIT) [13].

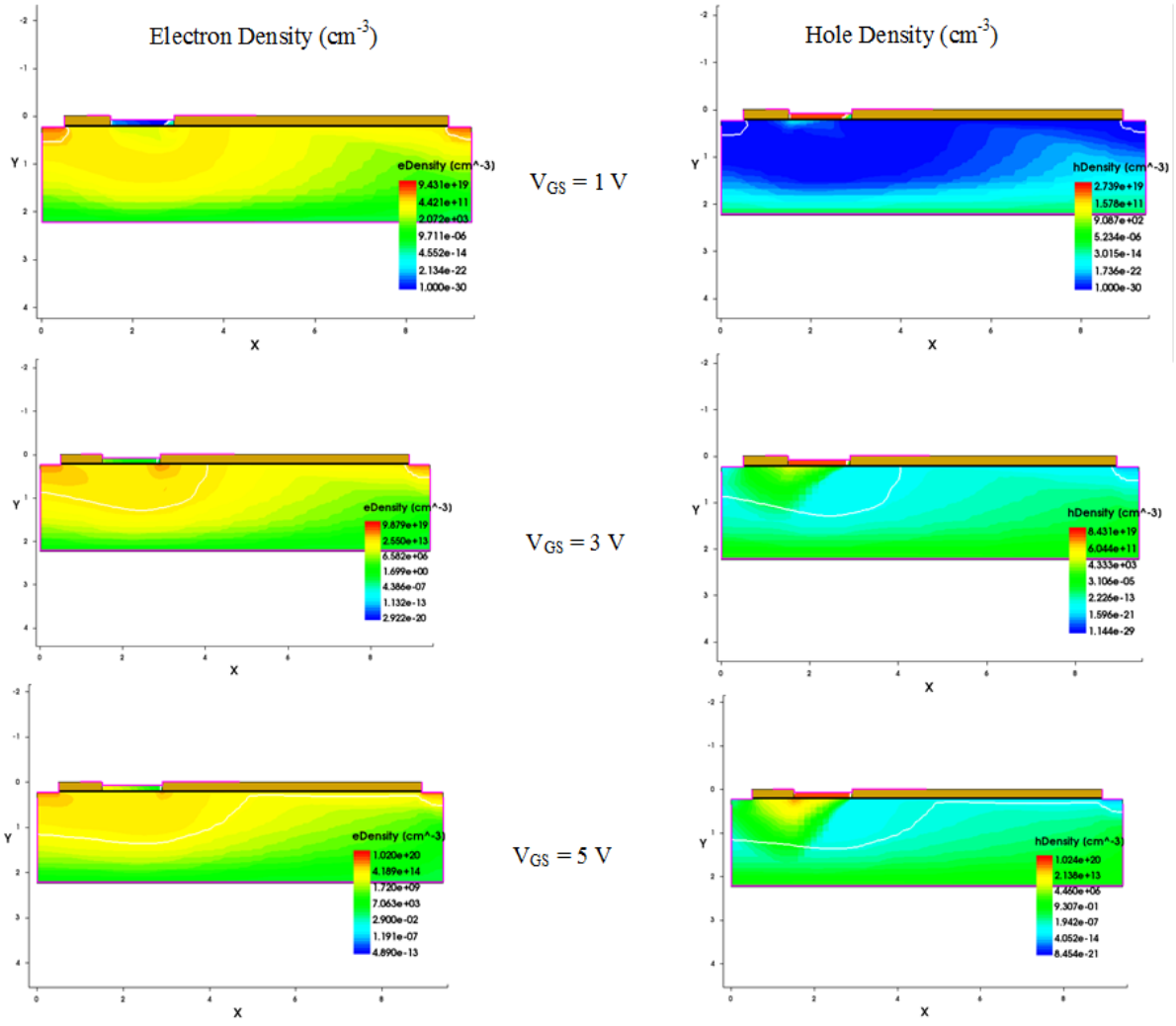

Figure 2.4: Plot of electrons and holes at varying gate-to-source voltage, V_{GS} [13].

increased to 2V the channel begins to form fully including the area under the *p*-GaN layer. With further increase in the gate voltage holes are injected into the channel which stimulated a higher concentration of electrons being attracted into the channel. This conductivity modulation allows for high current density unlike typical recessed HEMTs. The electrons flow due to the drain bias while the holes due to their lower mobility stay close to the gate [13].

The thickness of the barrier layer, the doping of the different layers, and the mole fraction of AlGaN affect the threshold voltage as is shown later. The substrate usually consists of Si or SiC which is superior to GaN in thermal conductivity allowing for a smaller die size by eliminating the need for a heat sink. Although Si is lower in cost than SiC, the latter has a lower thermal expansion coefficient mismatch and lattice mismatch percentage relative to GaN than Si keeping undesired strain to a minimum [14].

Open Issues with GaN Devices

As with any new material and process there is a learning curve for manufacturers to produce reliable GaN material with minimal defects. It is difficult to dope GaN with holes and get it up to a manufacturable volume would require years of effort [15]. However, there have been some strides in GaN device industry pioneered by Transphorms, GaN Systems, Cree, Panasonic, and others to soon follow. SiC has a longer history and thus is more advanced in terms of reliability, known short comings and strengths. Recent defects have shown there are so

called traps formed in random locations in the material where electrons can become trapped and as a result causes the degradation of the device or improper working of the device [16]. The degradations become visible as changes in current or resistances which correlate with the failure of passivation films and electrodes. Particularly at high drain-to-source voltage a phenomenon known as current collapse results in reduction in the drain current. By eliminating the trapping with the use of electric fields to clear electrons trapped in the material current collapse can be mitigated which is the reason the cause or current collapse is attributed to the traps [17]. As manufacturing processes improve this technology may be able to further suppress the current collapse phenomenon.

Another issue with GaN devices arises from the poor conductivity of the material. GaN has a conductivity of about 1.3 as seen from the Table 1. As the current increases through the device the device begins to heat up. Since GaN has poor thermal conductivity it is unable to release the heat fast enough thereby contributing to a decrease in current as the drain-to-source voltage is increased [18]. Methods proposed to address this include using a different substrate for the GaN device such as Si, SiC, AlN, or diamond to dissipate heat more effectively from the device [19]. Of these materials there are various factors to consider such as the lattice mismatch between the buffer layer and substrate and the cost of the material.

Previous Modeling Efforts

TCAD numerical simulation is useful for understanding of the device behavior and provides insight into properties, characterization, and variation of parameters without the cost of having to physically implement controlled experiments for each case one might be interested in. Previous models for TCAD simulation include the works reported in [20, 21]. In [21], a GaN device is modeled and compared to other structures in terms of transfer characteristics. These models provide some insight into the differences for threshold voltage for varying GaN device structures, but does not deeply investigate the GIT structure. The TCAD Sentaurus library provides a sample structure based on a GIT [22]. Since this device discloses the *I-V* characteristics and device structure, dimensions and doping parameters it becomes possible to simulate in a numerical simulator and compare the results with the experimental data. Reference [20] shows good agreement between the experimental results and the numerical model for *I-V* characteristics, but does not investigate further how the dimensions and parameters may affect the device behavior.

There are currently no analytical models for the GIT, but there are existing analytical models for depletion-mode AlGaN/GaN HEMTs and enhancement-mode recessed AlGaN/GaN HEMTs [23-25]. The recessed HEMT is similar to the depletion-mode HEMT except the AlGaN barrier layer has been made thinner to decrease the 2DEG in the channel resulting in a positive threshold voltage. The models proposed for the HEMTs include threshold voltage models based on the

energy band diagram, polarization models, and control charge models using Poisson's equation or quantum well based on Schrodinger's equation. While the more accurate phenomena can be described by using the Schrodinger equation in a quantum well it is impossible to solve analytically since the solution is transcendental and must be solved in conjunction with the Poisson method. Many of these equations yield various parameters which make the expressions less intuitive and more cumbersome for calculation purposes [26]. Despite the models working for HEMTs, the difference in behavior of the GIT due to conductivity modulation raises a challenge for using these conventional methods for the GIT device.

There have been many efforts focused on compact modeling of GaN devices. Particularly for depletion-mode HEMTs, there is a current consideration by the compact model coalition to decide on a universal model that can model high-frequency/high-power and high-speed/high-voltage applications [27]. The current contenders are Angelov model, ASM-HEMT, MVSG and HSP models [28]. The Angelov model is superior in the frequency domain. The ASM-HEMT model is derived from the surface-potential based model. The MVSG model is based on charge current modeling. Finally the HSP model is also a surface-potential based model developed with switching applications.

Despite a number of good models for HEMTs, the GIT may present a challenge by not adhering to the similar behavioral principles as the regular HEMT. These models may not capture the conductivity modulation experienced in GIT.

There have also been attempts at empirically modeling GIT by parameter extraction in reference [29,30]. The extracted parameters are implemented into drift-diffusion model for carrier transport to describe the drain current density.

Contributions in Thesis

The contributions made in this thesis are summarized below:

1. Model of a GIT in Sentaurus TCAD simulator to observe effects of thickness, mole fraction, energy band diagram for the purpose of understanding the device behavior and further advance the modeling efforts using faster methods.
2. Analytical compact model for the threshold voltage for the GIT device.
3. Charge control model with modification for the GIT device that incorporates a scheme for modeling the conductivity modulation phenomenon.
4. Derivation of *I-V* characteristics for GaN GIT.
5. Empirical modeling in SPICE for EPC Recessed HEMT.
6. Empirical modeling in SPICE for GaN GIT.

CHAPTER 3: TCAD SIMULATION

In order to study the effects of device dimensions, doping concentration, mole fraction of Al and Ga in AlGaN material system, etc. on the behavior of the gate injection transistor (GIT) the device was simulated based on an experimental data obtained from testing a commercially available device [30]. The simulation has been performed using TCAD Sentaurus software. The software package has separate tools to focus on the creation of the structure, device physics to be modeled, and the visual plotting of the results. The device tool is used to incorporate physical models such as the carrier transport equation and has included polarization for strain based GaN polarization. Sentaurus visual tool is used for plotting the DC characteristic results. The Sentaurus library provides a sample structure based on *p*-doped GaN layer on top of a HEMT based on [30] experimental data. This serves as a starting point for manipulation of the device to observe the effects of doping, thicknesses, mole fraction of Al in AlGaN, and their corresponding bandgap change for understanding the effects these parameters have on the operation of the device. A table of the default simulation parameters is shown in Table 2. These parameters were used in the TCAD simulation and are the basis for future calculations in the developed model where both the TCAD simulation and the analytical model will be compared. The default simulation results for *I-V* characteristics, transfer characteristics, transconductance, and energy band diagram are shown in Figures 3.1-3.3 [31].

Table 3.1: Default Device Simulation Parameters

Symbol	Parameter	Quantity
φ [eV]	Schottky Barrier Height	0.6
m	Mole fraction	0.2
D [m]	Thickness of AlGaN	15×10^{-9}
ε *[F/m]*	Dielectric constant	$9.3\varepsilon_o$
N_d *[cm^{-3}]*	*n*-AlGaN concentration	1×10^{18}
N_a *[cm^{-3}]*	*p*-GaN concentration	3×10^{17}
L [m]	Length of GIT	15×10^{-6}
Z [m]	Width of GIT	5×10^{-5}
μ [m^2/(Vs)]	Electron Mobility	0.04
E_g [eV]	Bandgap of GaN	3.4
E_{crit} [V/m]	Critical Electric Field	160×10^5

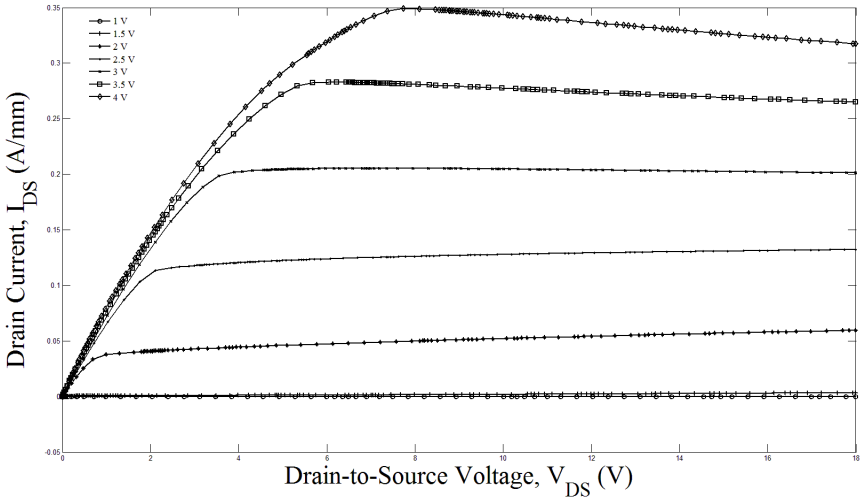

Figure 3.1: Typical *I-V* characteristics of a GaN gate injection transistor.

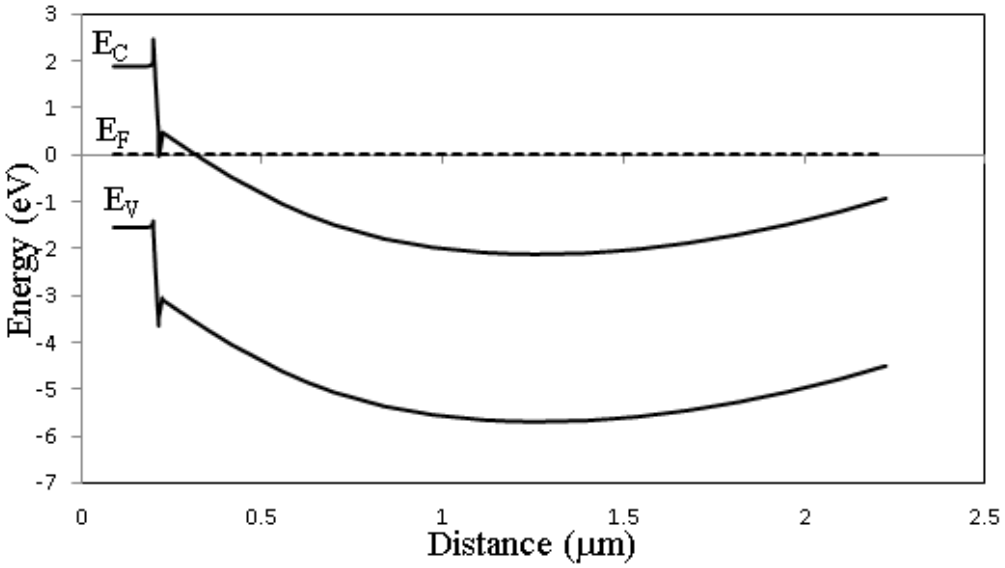

Figure 3.2: Energy band diagram of a GIT where the conduction band in the quantum well is above the Fermi level.

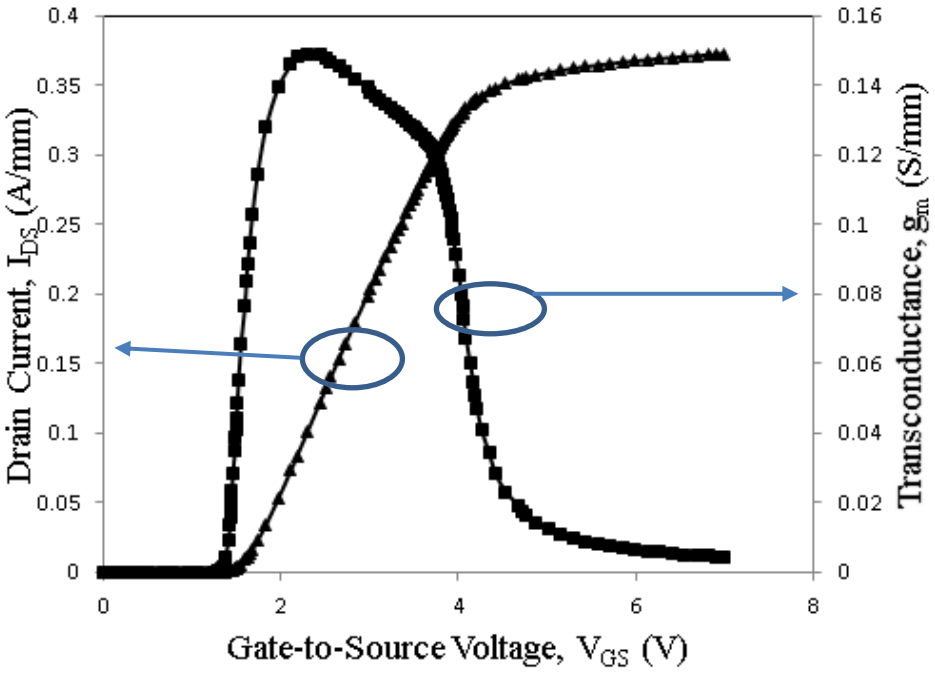

Figure 3.3: Transconductance and drain current response of a GIT.

Effects of p-GaN Cap

The GIT is distinguished from the HEMT by the addition of the *p*-doped GaN layer on top of the AlGaN barrier layer. The thickness and doping of the GaN layer was varied in a TCAD simulation to understand the effect these parameters may have on the operation of the GIT. Figures 3.4 and 3.5 show that the effect of these parameters is negligible with respect to the threshold voltage [31].

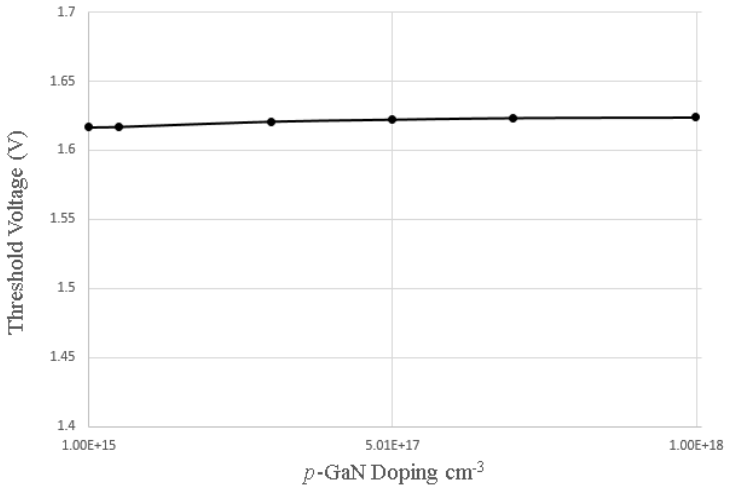

Figure 3.4: Threshold voltage with respect to *p*-doping of GaN.

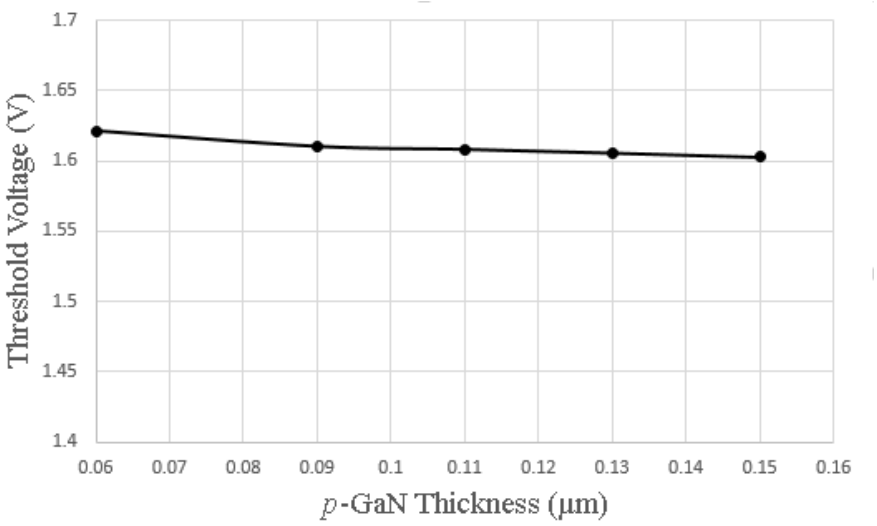

Figure 3.5: Threshold voltage with respect to GaN thickness.

Effects of AlGaN Thickness

In the TCAD simulation the AlGaN barrier layer thickness was varied to study the effect of the thickness. Similar to the recessed GaN HEMT, the thinning of the AlGaN layer reduces the 2DEG in the channel [31]. The 2DEG reduction causes the device to become enhancement mode, but reduces the current density of the device [32]. Figure 3.6 shows the transfer characteristics and the threshold voltage change as the thickness of the barrier layer changes. The energy band diagram in Figure 3.7 shows a lowering of the conduction band as the barrier layer thickness increases until it reaches below the Fermi level indicating a depletion mode device.

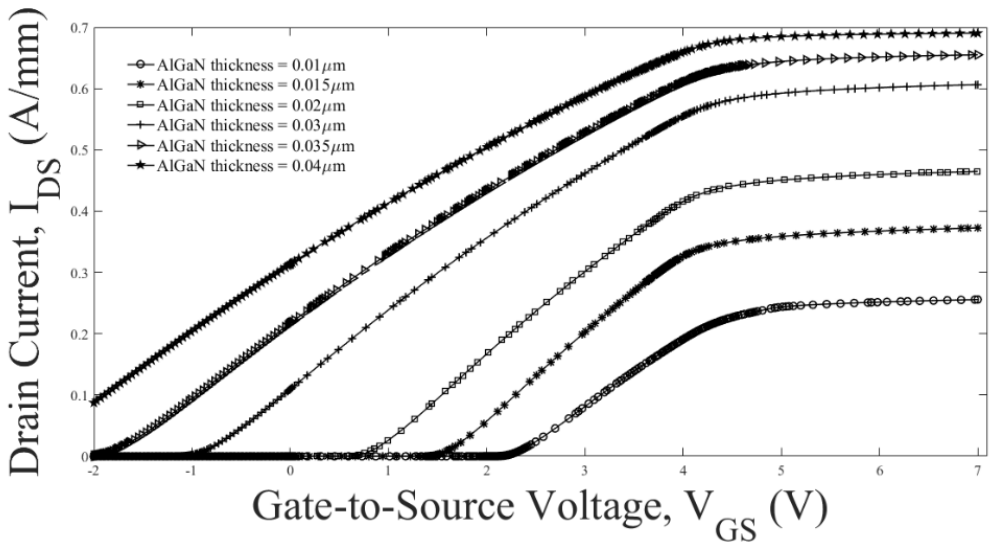

Figure 3.6: Transfer characteristics of a GIT with varying AlGaN layer thickness.

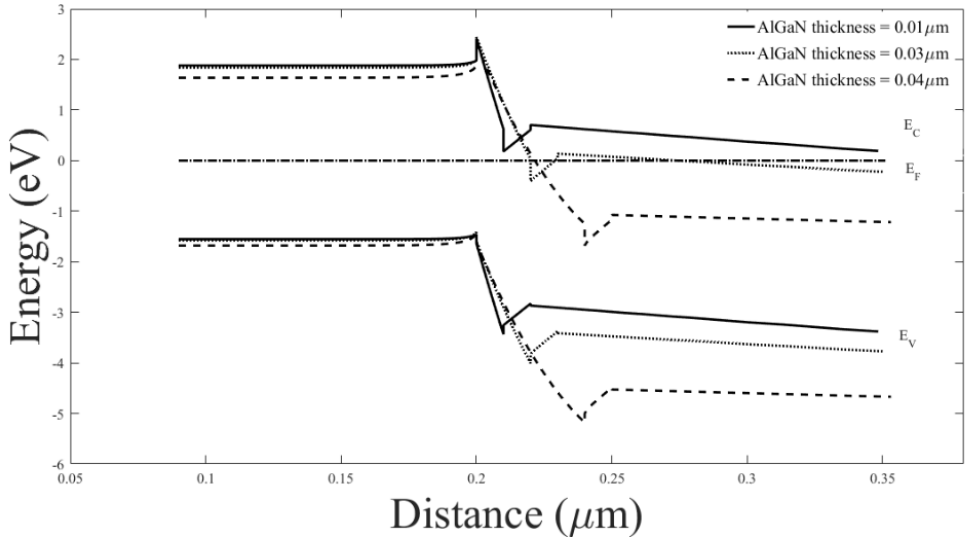

Figure 3.7: Energy band diagram of a GIT for varying AlGaN layer thickness.

Effects of AlGaN doping

The AlGaN *n*-type doping has also been varied in the Sentaurus simulation. The higher the doping concentration the more the extrinsic Fermi level moves closer to the conduction band. As the doping increasing the extrinsic Fermi level rises above the conduction band so the device becomes a depletion mode device. The effect of the doping seems to produce a depletion mode device at high doping around $5x10^{18}$ cm^{-3}. The results are shown in Figure 3.8 and 3.9 [31].

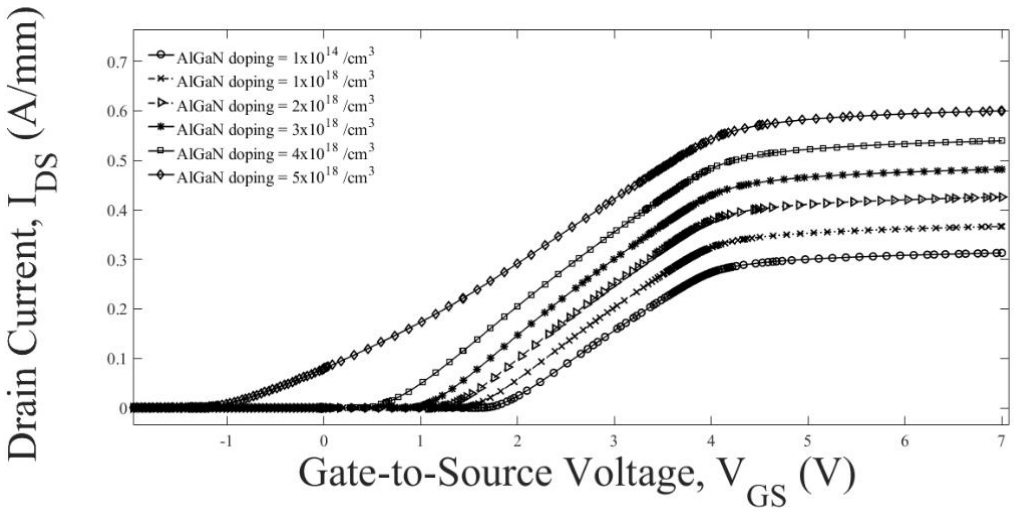

Figure 3.8: Transfer characteristics of a GIT with varying AlGaN doping.

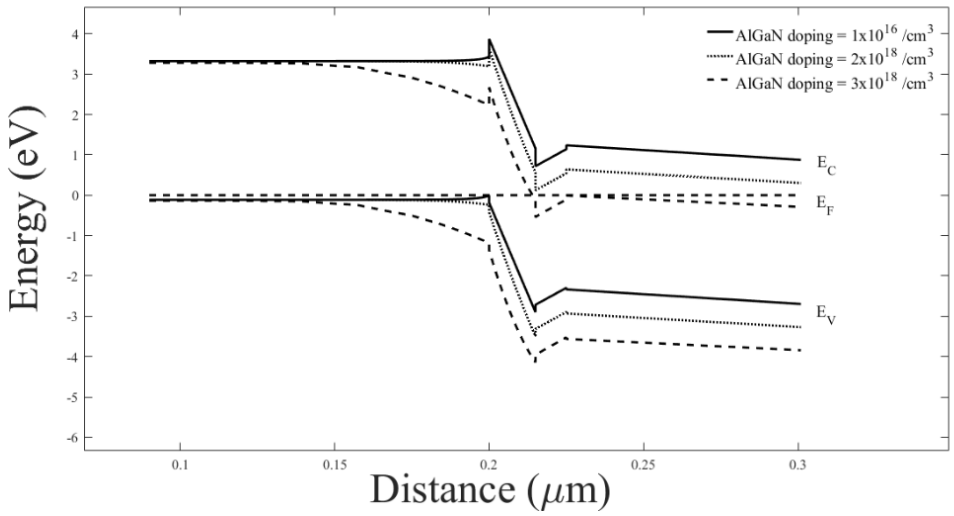

Figure 3.9: Energy band diagram of a GIT for varying AlGaN doping.

Effects AlGaN Mole Fraction

The mole fraction of Al and Ga in AlGaN was varied in the TCAD simulation. Recalling from the literature review chapter, the strain from the differing lattice structures between the AlGaN and the GaN layers provide electrons due to the GaN layer being piezoelectric in nature. The higher the mole fraction of the AlGaN the more the strain and consequently there should be a higher 2DEG concentration. The higher 2DEG would mean the threshold voltage is lower since there are more electrons to deplete. Similarly, since there is a higher number of electrons the current density is much higher for the higher mole fraction for any gate-to-source voltage greater than the threshold voltage of the device. Figure 3.10 and 3.11 show the result of the TCAD simulation for varying mole fraction of AlGaN.

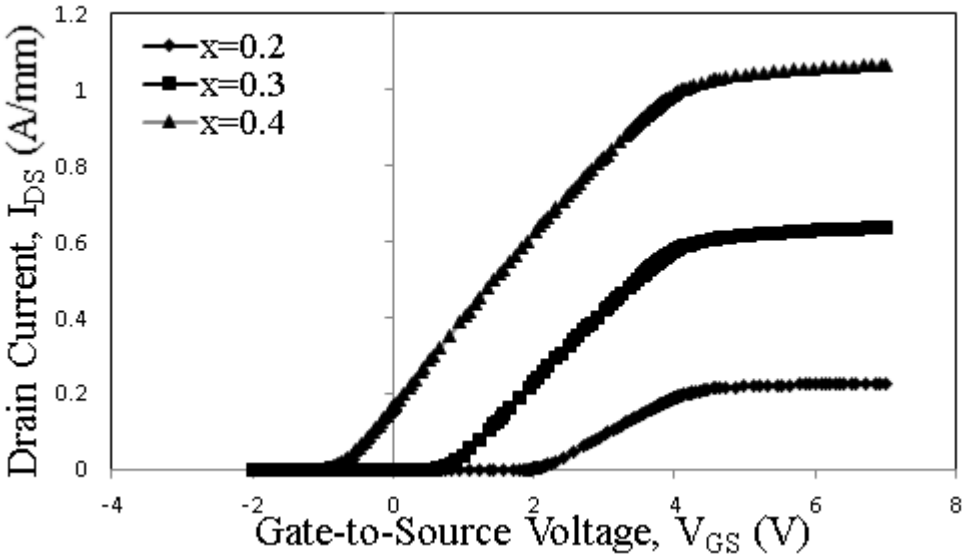

Figure 3.10: Transfer characteristics of a GIT with varying AlGaN mole fraction.

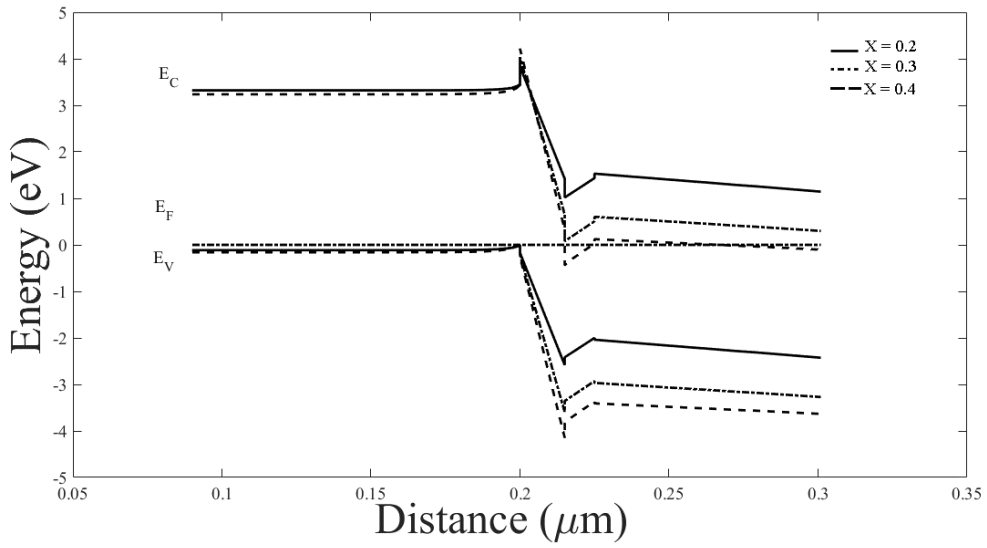

Figure 3.11: Energy band diagram of a GIT with varying AlGaN mole fraction.

CHAPTER 4: COMPACT ANALYTICAL MODEL

In a GaN HEMT, a 2DEG channel is naturally formed at the heterojunction between AlGaN and GaN layers. The similarity of the GIT structure at the heterojunction causes the same behavior, but the conduction band is raised above the Fermi level thereby depleting the channel due to the *p*-doped GaN underneath the gate electrode. For this reason, the existing GaN HEMT model needs to be modified by including the impact of the *p*-doped GaN on the threshold voltage. A new expression for the threshold voltage is derived and the charge control expression is also adjusted to reflect the concentration of electrons in the channel.

Threshold Voltage Model

The expression for the threshold voltage was derived by considering the energy band diagram and defining the threshold voltage as the distance between the conduction band and the Fermi level. When the conduction band is above the Fermi level at zero gate bias, the threshold voltage is positive and so the GIT behaves as an enhancement mode device. Previously reported threshold voltage models for depletion-mode and enhancement-mode devices use the energy band diagram to derive an expression for the threshold voltage [33]. Since the structure of the GIT includes the addition of a *p*-doped GaN layer above the AlGaN layer, the energy band diagram is raised in the *p*-doped region and the change must be accounted for in the model. The proposed energy band diagram is shown in Figure 4.1 [31].

AlGaN has a larger bandgap than GaN which creates the heterojunction conduction band offset as given by ΔE_c. Additionally, materials that are *p*-doped have an extrinsic Fermi level that lies closer to the valence band. As materials are merged, the Fermi levels line up causing the conduction band of the *p*-doped region to rest higher than the undoped GaN buffer and thereby raises the conduction band across the device structure and above the Fermi level. Once the conduction band is above the Fermi level the device is said to be enhancement-mode given that the channel is depleted of electrons. Analyzing the band diagram includes developing expression and definitions for the built-in voltages in the device. The area between the metal and the *p*-doped GaN similarly reflect the structure of a Schottky diode. In the model it is treated as a Schottky diode potential to develop a definition for the first built-in potential, V_{BI1}. Similar to the Schottky diode, the applied voltage will cause V_{BI1} to lower so the energy is expressed as *q*

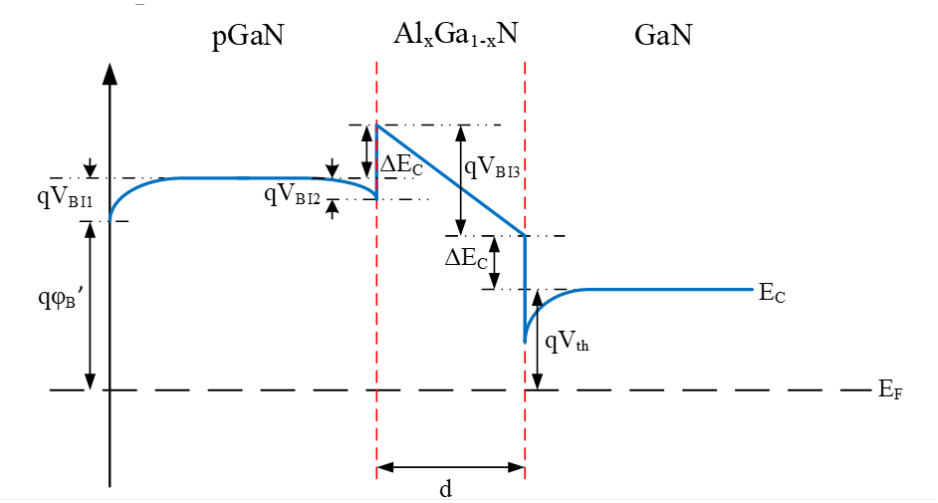

Figure 4.1: Proposed energy band diagram for threshold voltage model.

(V_{BI1}-V_a). For purposes of demonstrating enhancement-mode operation Figure 4.1 is drawn with the assumption the applied gate voltage is $V_a = 0$ V. V_{BI1} is given in by,

$$V_{BI1} = \varphi'_B - \frac{kT}{q} ln\left(\frac{N_v}{N_a}\right) \quad (1)$$

The V_{BI2} voltage is described as a built-in potential for a diode. This diode however takes the form of a *p-n* heterojunction rather than a normal *p-n* homojunction diode. This results in a slightly different expression for the built-in potential. The expression developed is given by [34],

$$qV_{BI2} = \frac{\Delta E_c - \Delta E_v}{2} + kTln\left(\frac{N_d N_a}{n_{i,n} n_{i,p}}\right) + \frac{kT}{2} ln\left(\frac{N_{v,n} N_{c,p}}{N_{c,n} N_{v,p}}\right) \quad (2)$$

Due to the lack of experimental values for specific mole fractions of wurtzite AlGaN, V_{BI2} could not be calculated. However, within normal doping levels, V_{BI2} is negligible and only appears significant for heavy *n*-AlGaN doping as seen from the earlier simulation results. The model calculation excludes V_{BI2}, since moderate level of AlGaN doping is expected.

V_{BI3} is the potential drop across the AlGaN barrier that is previously reported for depletion-mode devices [35] and is given by,

$$V_{BI3} = \frac{qN_D d^2}{2\varepsilon_{AlGaN}} - \frac{\sigma}{\varepsilon_{AlGaN}} d \quad (3)$$

Where d is the thickness of AlGaN, N_D is the doping of AlGaN, and the polarization, σ, is downwards as is typical for GaN/AlGaN and is,

$$\sigma = P_{spont}(AlGaN) - P_{spont}(GaN) + P_{piezo}(AlGaN) \quad (4)$$

Here P_{spont} *(GaN)* is -0.029 and P_{spont}*(AlGaN)* = -0.052*m*-0.029. P_{piezo}*(AlGaN)* is negligible and *m* is the mole fraction of AlGaN [36]. Since the GIT becomes enhancement mode through the *p*-GaN layer by introducing the ΔE_c parameter there is negligible effect on the threshold voltage either in calculation or simulation from the *p*-doping of the GaN since the heterojunction potential well remains undisturbed. Considering the energy band diagram an expression is developed given by [31],

$$V_{th} = \varphi_B' + V_{BI1} - V_{BI3} \tag{5}$$

where, for a *p*-type semiconductor and metal, $\varphi_B' = E_g - \varphi_B$, φ_B is the Schottky barrier height and E_g is the energy bandgap.

Charge Control Model

The charge control model has been previously modeled using Poisson's equation for charge. Ideally a model for heterostructures can be solved with the energy eigen function given by Schrodinger's equation solved in a triangular quantum well. However, an analytical closed form solution is complicated and involves many parameters. It is common to Poisson's equation in the derivation of a charge control model as it is done with the MOSFET as is shown in previous papers [35]. The difficulty arises with realizing that the threshold voltage must remain well defined, but the nature of the GIT behavior seems to cause a discrepancy when using the original Schichman-Hodges model. Recalling the behavior of the GIT, the 2DEG appears to increase as more holes are injected

when the gate voltage is increased. This nonlinear response requires an adjustment in the charge control model. At first glance it appears that the threshold voltage is changing, but it must be well defined. From the threshold voltage model proposed earlier, the value of the threshold voltage is dependent on the applied gate voltage. Once the gate voltage surpass the threshold voltage the conduction band is lowered and the device behaves as a traditional depletion-mode device where the charge present in the channel can now be modeled with a virtual threshold voltage. In order to model the drain current increase due to conductivity modulation the applied voltage and the varying threshold voltage were incorporated into the model along with the proposed virtual threshold parameter.

To derive an analytical model of the DC characteristics of the GIT structure the traditional depletion-mode device model is initially considered without the addition of the *p*-GaN since the charge is present in the channel and is only depleted in the region under the GaN cap as is shown previously in Figure 2.4. This threshold voltage is being referred to as *virtual threshold* voltage, V_{vir}, which is different from the actual GIT threshold voltage given by [36],

$$V_{vir} = \varphi - \Delta E_c - \frac{qN_D d^2}{2\varepsilon_{AlGaN}} - \frac{\sigma}{\varepsilon_{AlGaN}} d \tag{6}$$

With the addition of the proposed GIT threshold voltage $V_{th,}$ which is dependent on the applied voltage at the gate electrode, the conduction band drops as the gate voltage is increased. The charge control model proposed for this case is given by [31],

$$n_s(x) = \frac{\varepsilon}{qd}(V_{GS} - v(x) - V_{vir} + (V_{GS} - V_{th})) \tag{7}$$

where, *v(x)* is the potential with respect to channel, ε is the dielectric constant of AlGaN, *d* is the thickness of the AlGaN layer and V_{GS} is the applied gate-to-source voltage.

The channel current is modeled by considering drift and diffusion to get,

$$I_{DS} = qZn_s(x)u(x) \tag{8}$$

where, *Z* is the gate width and $u(x) = \frac{\mu_o E(x)}{1+\frac{E(x)}{E_{crit}}}$ where, μ_0 is low field mobility simplifying to,

$$I_{DS} = C(V_{GS} - v(x) - V_{vir} + (V_{GS} - V_{th}))\frac{E(x)}{1+KE(x)} \tag{9}$$

and recalling $E(x) = \frac{dV(x)}{dx}$ where, $C = \frac{\varepsilon_{AlGaN}\mu_o}{d}$ and $K = \frac{1}{E_{crit}}$ the following is expression of the drain current is obtained,

$$I_{DS}\left(1 + K\frac{dV(x)}{dx}\right) = C(V_{GS} - v(x) - V_{vir} + (V_{GS} - V_{th}))\left(\frac{dV(x)}{dx}\right) \tag{10}$$

Integrating both sides and ignoring the resistive voltage losses at the source and the drain, and for $V_{GS} > V_{th}$ and $V_{GS} < V_{DSsat}$, for the linear region we get,

$$I_{DSLin} = \frac{C(V_{GS} - v(x) - V_{vir} + (V_{GS} - V_{th}))V_{DS} - 0.5{V_{DS}}^2}{KV_{DS} + L} \tag{11}$$

To derive the saturation current, the channel conductance is zero so that,

$$g_d = \frac{\partial I_D}{\partial V_{DS}} = \frac{C}{(KV_{DS} - L)^2}\{2V_{GS}L - 0.5KV_{DS}^2 - L(V_{th} + V_{vir} + V_{DS})\} \tag{12}$$

When solved for saturation voltage,

$$V_{DSsat} = \left(\frac{\sqrt{4V_{GS}KL - 2KLV_{th} - 2KLV_{vir} + L^2} - L}{K}\right) \tag{13}$$

Such that the drain current in saturation becomes,

$$I_{DSsat} = \frac{C(V_{GS} - v(x) - V_{vir} + (V_{GS} - V_{th}))V_{DS_{sat}} - 0.5{V_{DS_{sat}}}^2}{KV_{DS_{sat}} + L} \quad (14)$$

Self-Heating Effect

GaN devices face various problems one of which is poor thermal conductivity. It is most evident when observing the *I-V* characteristics at high drain-to-source voltages. Due to the high current the device must withstand the heating up of the electrons in the device and the poor conductivity prevents the device from cooling down fast enough. This degrades the device performance which may make the device less appealing for power electronics. There are however, ways to help counter the self-heating effect such as including a silicon or silicon carbide substrate since both of those have a much higher thermal conductivity. Regardless, the device simulated still exhibits drain current degradation due to self-heating. Many self-heating models for AlGaN/GaN type structures are incorporated as empirical models [37-39]. Based on the simulation as well as [40] the gate voltage correlates to an increase in self-heating. The information for lattice temperature versus gate voltage was extracted from the simulated structure based on the default parameters mentioned in Table 2 earlier. The curve was interpolated with a polynomial given by [31],

$$T = -3.089{V_G}^3 + 31.2{V_G}^2 - 54.25V_G + 309 \quad (15)$$

Using the empirically based mobility model from [37] the mobility was calculated for different gate voltages. While the gate voltage contributed significantly to the

degree of self-heating in the device, the degradation of the *I-V* curves occurs at high drain-to-source voltage. For this case, the mobility was assumed to decrease linearly along with the drain-to-source voltage so that the final expression for the drain current was given by [31],

$$I_{DS} = I_{DSlin,sat} - \lambda V_{DS} \tag{16}$$

for both linear and saturation regions of operation.

Comparison of TCAD Simulation and Compact Analytical Model

The default parameters used in the simulation were the same ones used in the calculations for the analytical compact model. Figure 4.2 and 4.3 show the comparison between the two models for varying thickness and doping of the AlGaN barrier layer [31]. While the model is smooth as expected the simulation results tend to follow a general linear trend, but oscillate to some degree. One reason for this could be the scale variability of the simulation parameters is very small and the simulation requires a mesh of the device. The mesh is typically designed with fine density at regions deemed important. While a finer mesh may improve the result, it would increase the simulation time greatly which includes cost. The thickness is varied in both the simulation and the analytical model in the figure where the thicker layer corresponds with a lower threshold voltage level or higher 2DEG for a specific gate voltage.

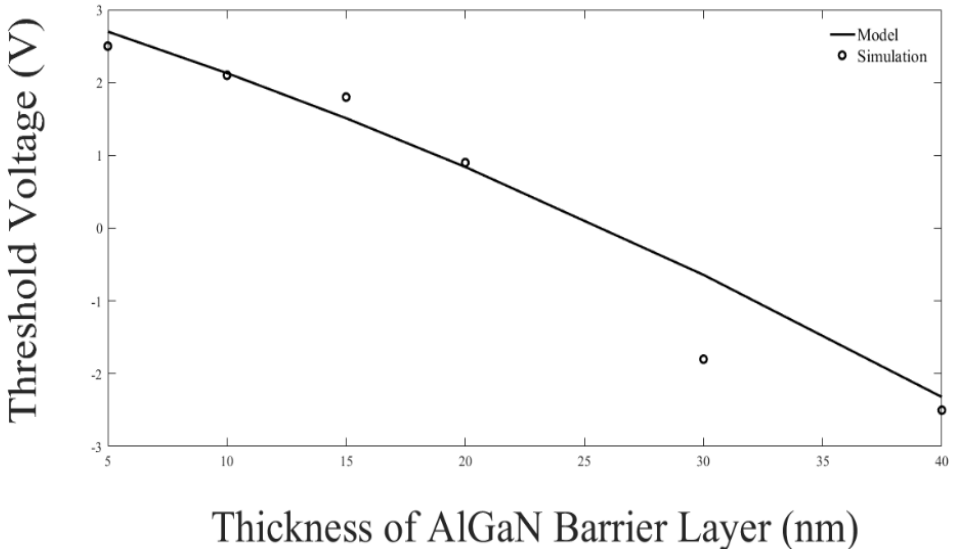

Figure 4.2: Comparison of simulation and model for varying AlGaN thickness.

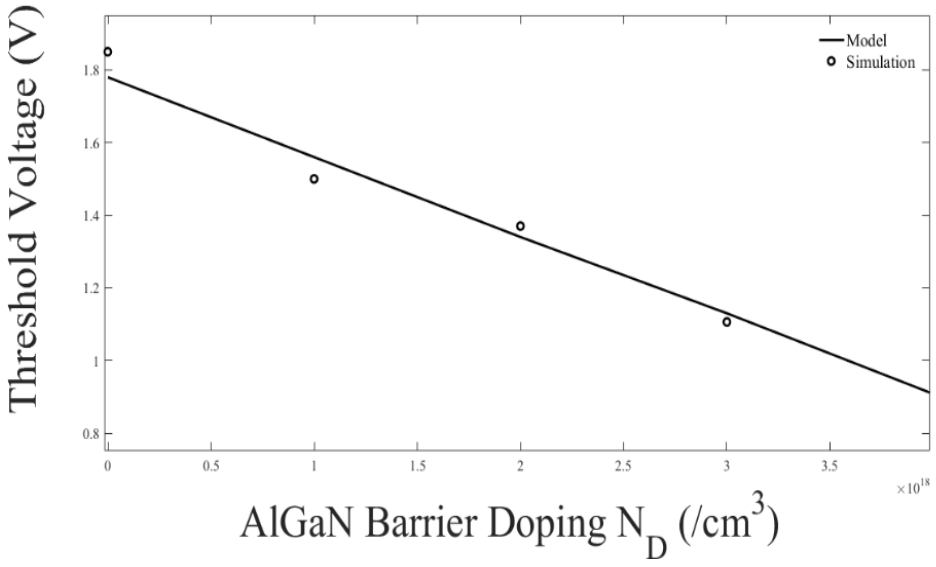

Figure 4.3: Comparison of simulation and model for varying AlGaN doping.

The higher the doping concentration the lower the threshold voltage required to turn the device on. Recalling from the simulation, Figures 3.6 and 3.7 show a significant decrease in the threshold voltage after a high doping is reached. If the doping in the AlGaN reaches high levels it begins to act as a degenerate *n*-type material where the Fermi level begins to penetrate the conduction band. This state represents the typical band diagram representation of a conductor and consequently there are electrons in the channel so the device turns on at zero gate voltage bias since the conduction band offset no longer can compensate for the extrinsic Fermi level position.

The TCAD simulation results and the compact model for threshold voltage as a function of the barrier doping are compared in Figure 4.3 and show a similar trend for both. The drain current for the linear and the saturation regions of operation are derived from the proposed control charge model and are adjusted for self-heating effects following equation (16). The *I*-*V* characteristics obtained from both the TCAD simulation and the compact analytical model with and without the self-heating fitting parameter are compared in Figure 4.4 [31].

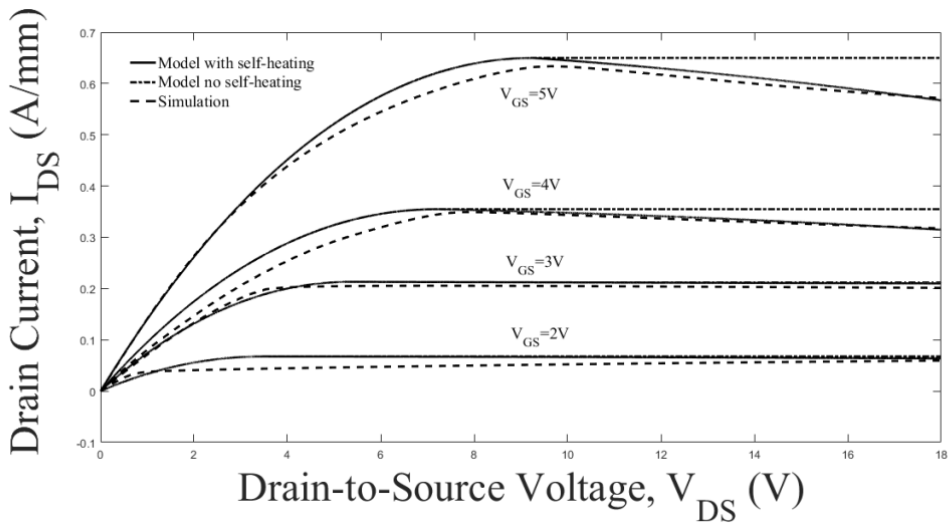

Figure 4.4: *I-V* Comparison of simulation, model with self-Heating, and model with no self-heating.

CHAPTER 5: EMPIRICAL SPICE MODEL IMPLEMENTATION

An equivalent circuit model is developed for a commercial GIT device at room temperature to be carried out in SPICE simulation. The *I-V* and *C-V* characteristics are extracted from the commercial device datasheet and fitted in MATLAB™. The fitted equations are realized as a combination of behavioral circuit components. Finally, the equivalent circuit model is tested in a simple boost configuration typical for power electronics applications to check for convergence and expected results. The Panasonic GIT is modeled using SPICE friendly syntax which includes a smooth transition from linear to saturation regions, reverse conduction, and fast convergence in SPICE simulators.

Development of the Model

The commercial device modeled in this paper is the Panasonic PGA26E07BA device [41]. Based on the datasheet, the *I-V* and *C-V* characteristics were extracted. The extracted data was fitted using Matlab software to easily implement into a simple SPICE simulator with an equivalent circuit model. Figure 5.1 shows the equivalent circuit model used with parasitic effects extracted from the *I-V* and the *C-V* characteristics [42].

The SPICE circuit used for the model from Figure 5.1 uses a voltage-dependent current source, I_{DS}, three voltage-dependent capacitances, and three constant parasitic resistances. The parasitic resistances used were directly from the datasheet.

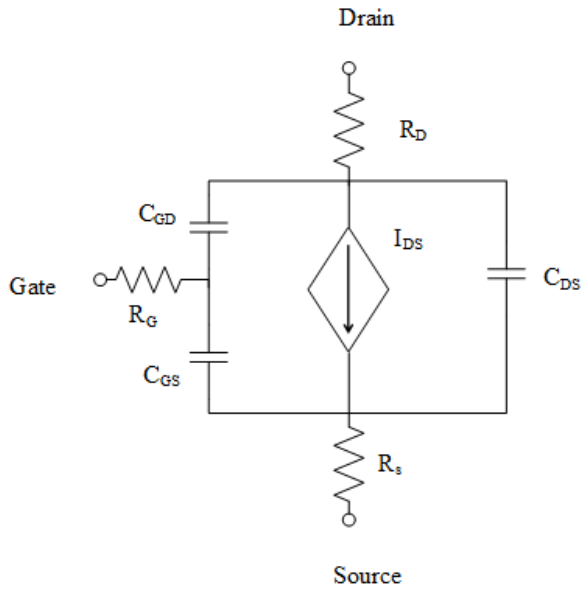

Figure 5.1: Equivalent circuit of a GIT with parasitics.

The voltage-dependent current source is used to model static current-voltage characteristics for both forward and reverse conduction which is seen in GaN devices. The parasitic resistance and capacitances are necessary to provide insight into the behavior of the device switching performance.

The voltage-dependent current source is a bidirectional current source used to mimic the reverse conduction behavior of GaN. The current source is fitted in MATLAB™ and treated as a voltage-dependent switched current source. The parasitic capacitance was included as a drain-to-source voltage-dependent nonlinear capacitance extracted from the datasheet. The sheet includes the capacitance measurements for C_{oss}, C_{rss}, and C_{iss} which are important parameters in the realm of switching power electronics. In order to make this information useful

for the equivalent model (17-19) were used to convert the parameters into C_{gd}, C_{gs}, and C_{ds} for the purpose of forming the equivalent circuit [42].

$$C_{iss} = C_{GD} + C_{GS} \tag{17}$$

$$C_{oss} = C_{DS} + C_{GD} \tag{18}$$

$$C_{rss} = C_{GD} \tag{19}$$

Extraction and Fitting

The *I-V* and the *C-V* curves were extracted and imported into MATLAB™ for a logarithmic fit. While a polynomial fit or compact model may have been used, it is difficult to implement into a SPICE environment with the inclusion of a smooth transition from the linear to saturation region as well as a reverse conduction. Figure 5.2 shows the extracted *I-V* curves with the surface fit in MATLAB™ dependent on V_{GS} and V_{DS} [42]. The 2D fit in Figure 5.3 gives better insight into the discrepancy in the linear region [42]. The saturation region most closely matches the device experimental data which is the region where the device is typically used for switching applications such as DC-DC converters. The fitted equation is given in Figure 5.2.

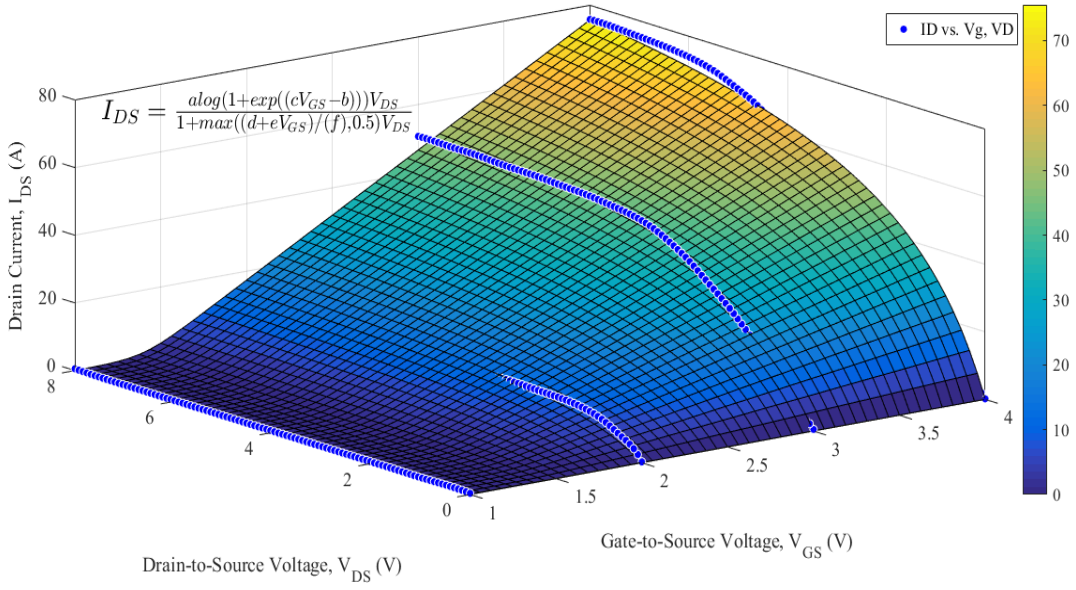

Figure 5.2: 3D Surface fit of the GIT in MATLAB™.

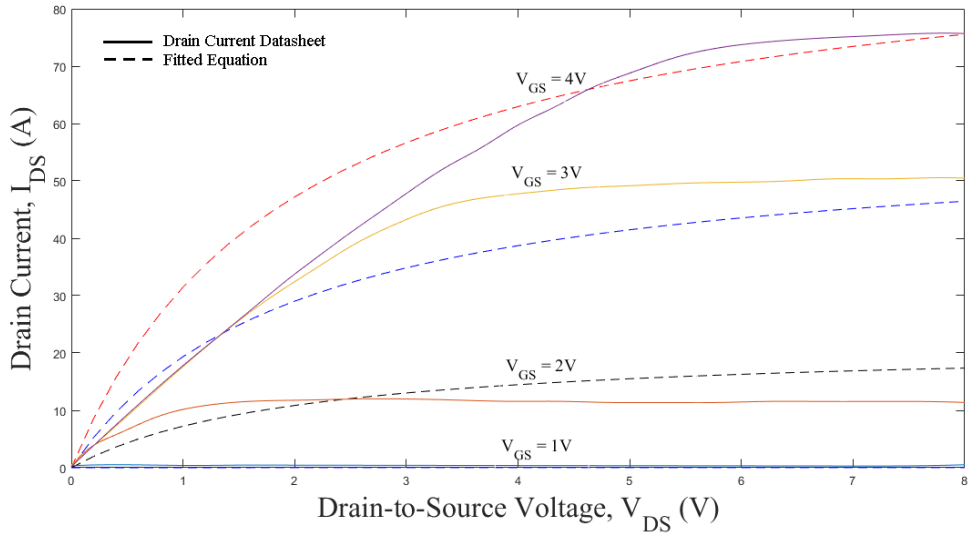

Figure 5.3: 2D fit of the GIT in MATLAB™.

The forward transfer characteristic is shown in Figure 5.4 [42]. While there are better fits available such as a polynomial fit shown in Figure 5.5 there are problems with this model implementation into SPICE [42]. The polynomial fit only performs well within V_{GS} = 0-4V and V_{DS} = 0-8V. The polynomial fit is susceptible to oscillations outside these ranges, there is no reverse conduction implementation with the current source, and there are values of V_{GS} that do not converge to zero at V_{DS} = 0V. These become significant problems for simulation if the conditions are not exactly similar to the ones used for the fitted expression.

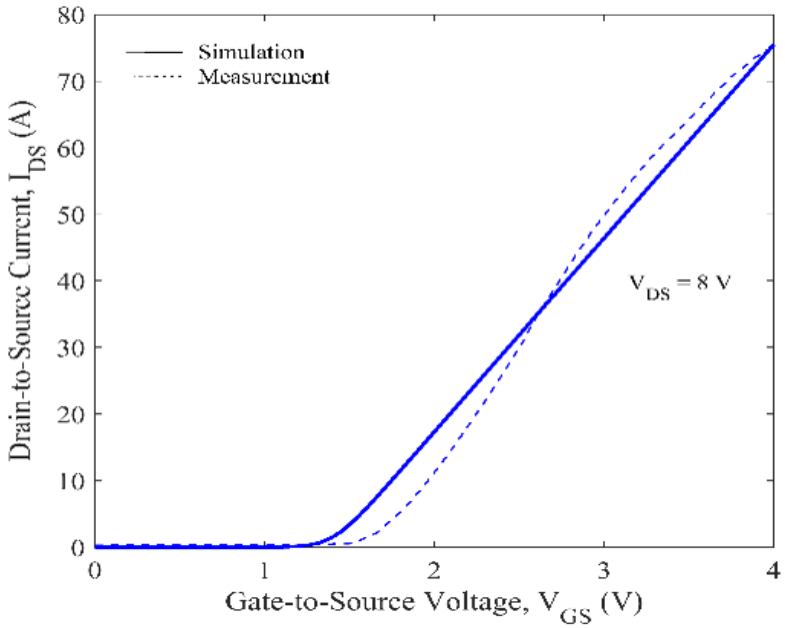

Figure 5.4: Transfer curve at V_{DS} = 8V fit in MATLAB™.

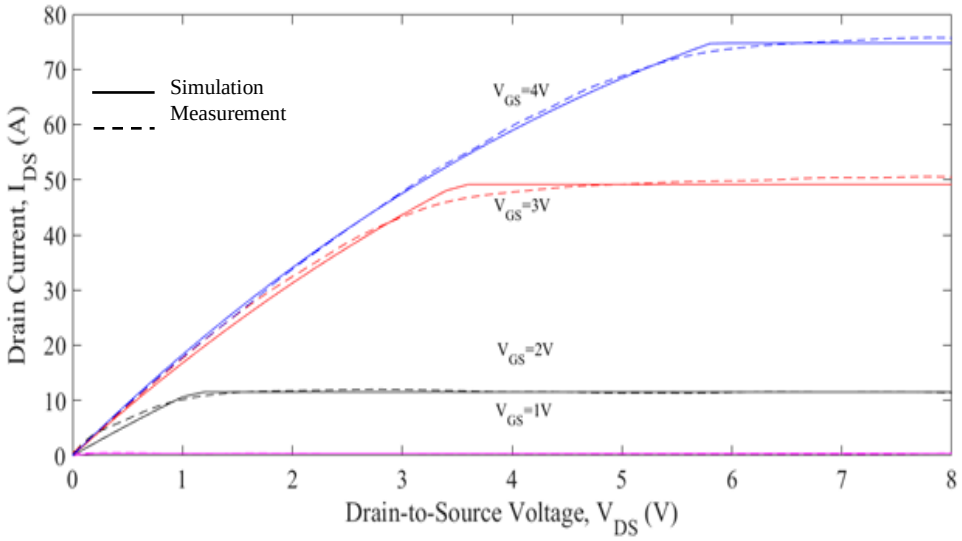

Figure 5.5: Polynomial fit for bidirectional current source

The *C-V* curves were more closely matched and shown in Figures 5.6-5.8 for C_{oss}, C_{rss}, and Ci_{ss}, respectively [42]. C_{oss} shows small signal output capacitance when gate and source terminals are shorted. C_{rss} shows the small signal reverse transfer capacitance and C_{iss} shows the small signal input capacitance when drain and source terminals are shorted. Recalling equations (1-3) the fitted equations for C_{GS}, C_{GD}, and C_{DS} are acquired dependent on V_{DS} The fitted capacitances are given by,

$$C_{oss} = 187e^{-0.0116V_{DS}} + 82.72e^{-0.0004V_{DS}} \quad (20)$$

$$C_{iss} = 145.8e^{-0.2098V_{DS}} + 405.2e^{-4.3x10^{-6}V_{DS}} \quad (21)$$

$$C_{rss} = 110.5e^{-0.241V_{DS}} + 32.54e^{-0.0187V_{DS}} \quad (22)$$

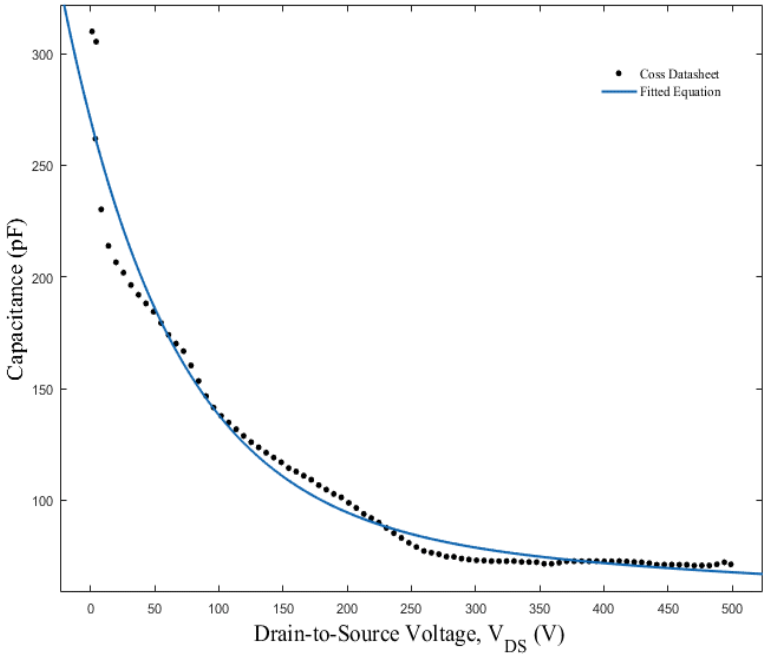

Figure 5.6: Output capacitance curve, C_{oss}, fit in MATLAB™.

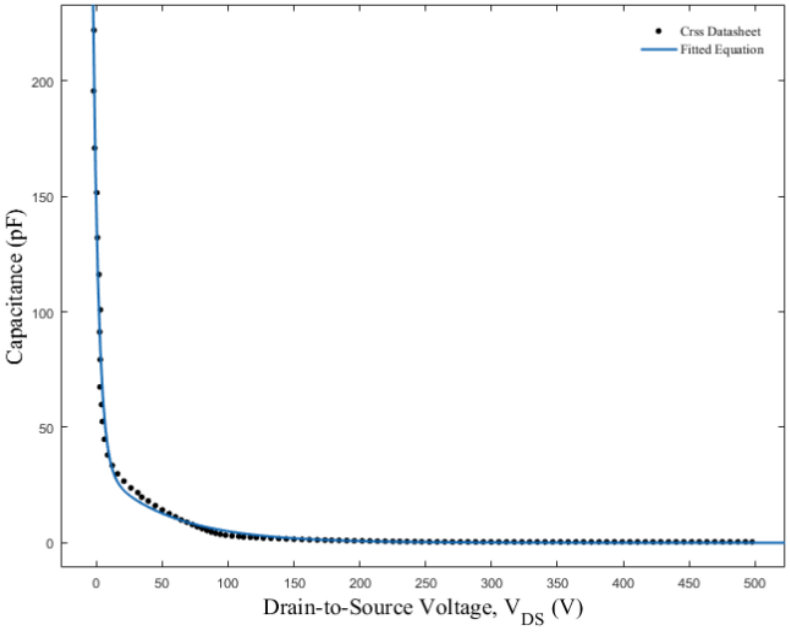

Figure 5.7: Reverse capacitance curve, C_{rss}, fit in MATLAB™.

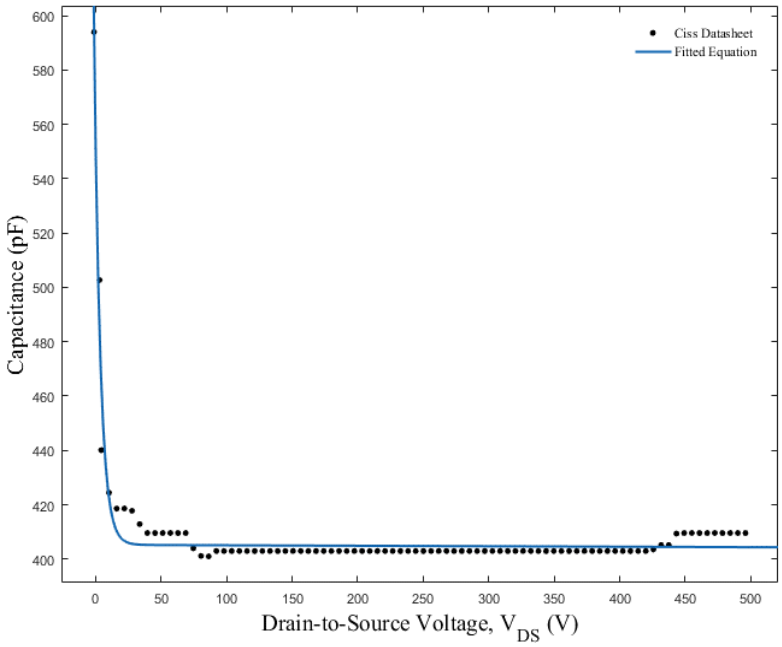

Figure 5.8: Input capacitance curve, C_{iss}, fit in MATLAB™.

SPICE Simulated Parameter Sweep and Boost Converter

Once the equivalent circuit model is implemented as a sub circuit in LTspice (an open source SPICE circuit simulator) it can be used as a part of larger more complex circuits for power applications. To test convergence and the functioning of the model first the device was tested in a simple circuit shown in Figure 5.9. The gate-to-source and the drain-to-source voltages were swept from 1-4 V and 0-8 V, respectively. The results are shown in Figure 5.10 with quick convergence that matches the fitted results [42].

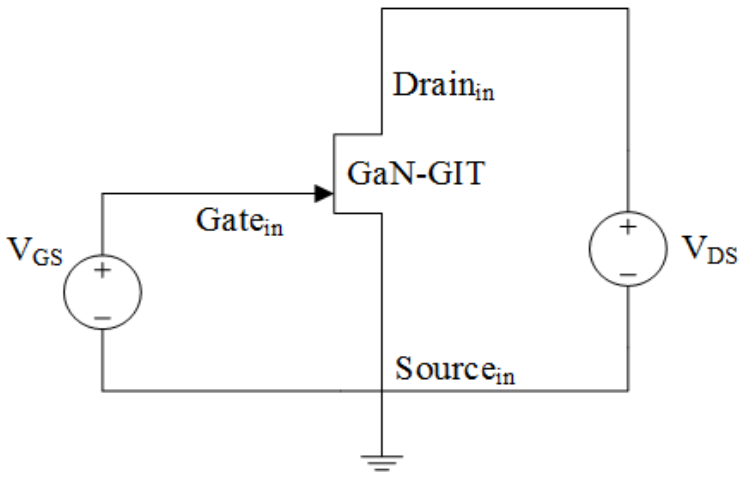

Figure 5.9: Circuit implemented in SPICE for parameter sweep.

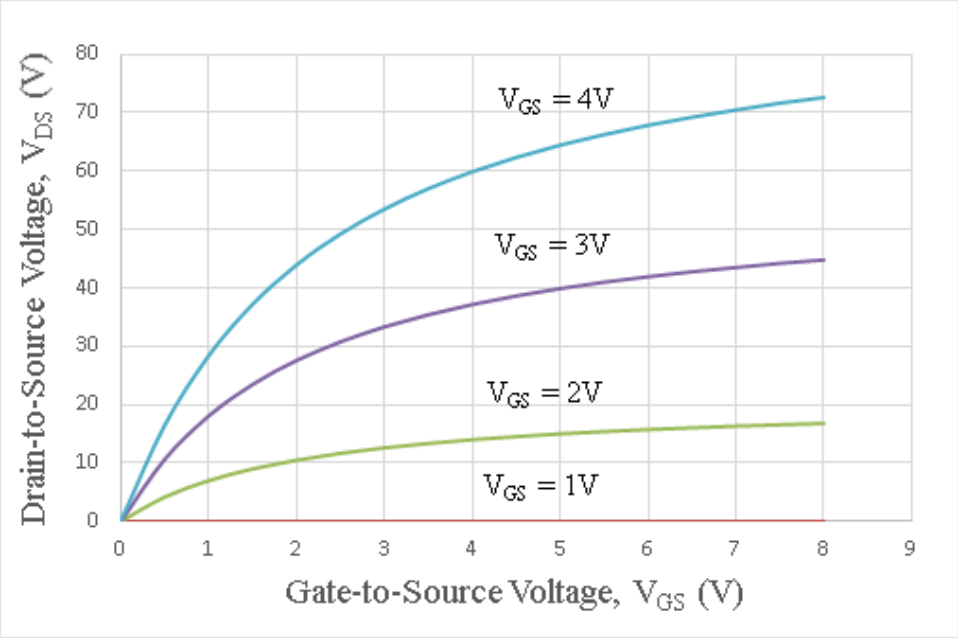

Figure 5.10: Results for parameter sweep in SPICE.

The sub circuit was then implemented into a test simulation of a boost converter in LTspice. Complex models for devices can slow down simulation time or just never converge in large complex circuits with multiple devices switching at high frequency. Fig. 5.11 shows the test circuit for a boost converter with an input of 25 V to 50 V output, switching frequency of 150 kHz, 3 A current ripple and 1 V ripple voltage. The resulting waveforms are shown in Figures 5.12-5.14 [42].

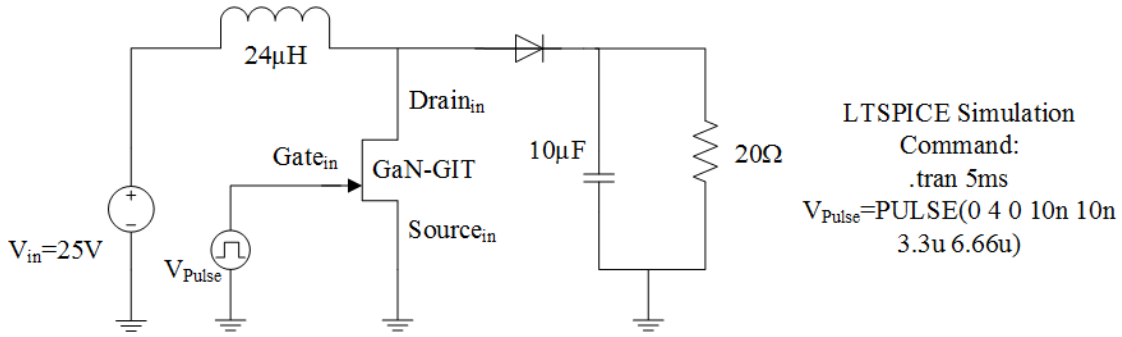

Figure 5.11: Boost converter circuit implementation in SPICE.

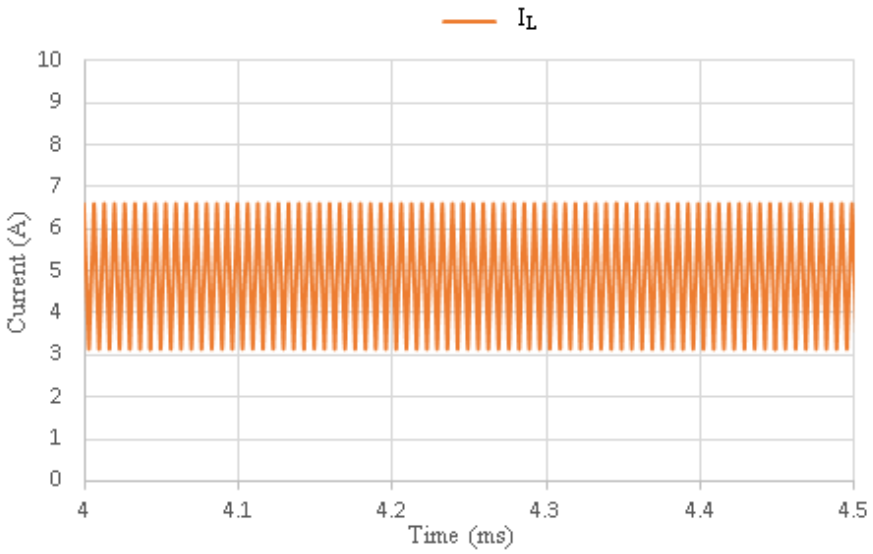

Figure 5.12: LTspice simulation results of inductor current (I_L) for the boost converter topology from Figure 5.11.

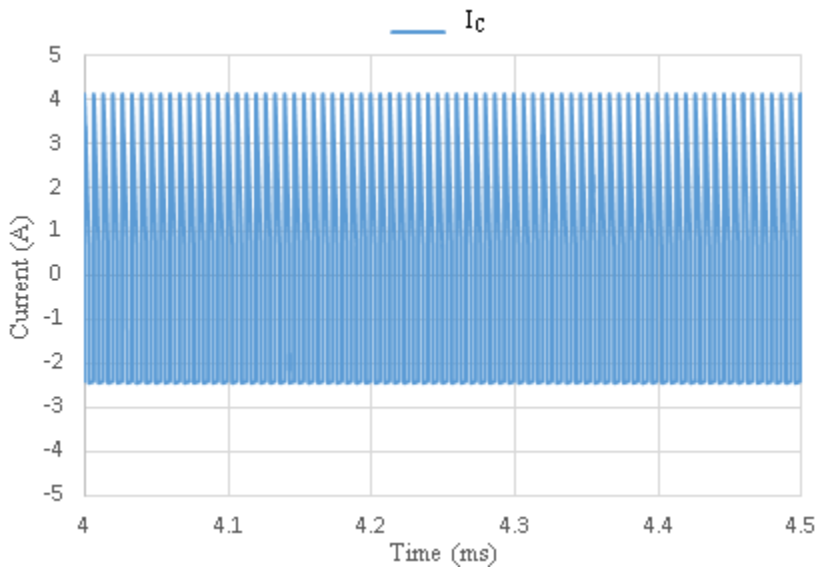

Figure 5.13: LTspice simulation results of capacitor current for boost converter topology shown in Figure 5.11.

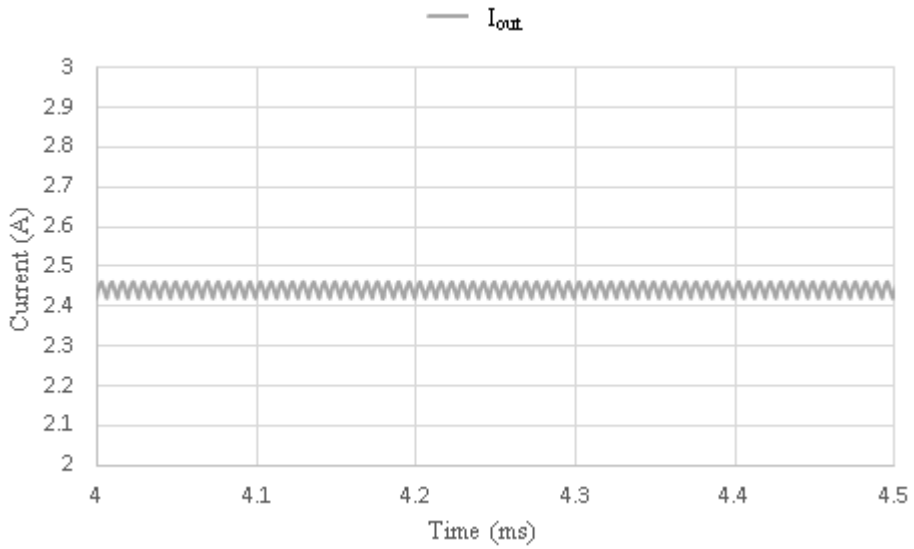

Figure 5.14: LTspice simulation results of output current for boost converter topology shown in Figure 5.11.

This proves the model converges with expected results and can be used as a guide for power electronics simulation. Future improvements for the GIT model include incorporating temperature variance into the model, a more accurate self-heating model, and incorporating into a model such as BSIM.

BSIM Model Parameter Extraction for EPC 2022

The EPC 2022 GaN recessed HEMT device was modeled using the BSIM model typically used for MOSFET devices with a similar process as [43]. The device parameters to be extracted are K_P-transconductance parameter, V_{T0}-threshold voltage, R_S-source parasitic resistance, R_D-drain parasitic resistance, C_{DS0}-gate-to-drain parasitic capacitance, and C_{GS}-gate-to-source parasitic capacitance. The EPC 2022 GaN device was tested for *I-V* and *C-V* static characteristics curves. Parameters that describe the behavior of the device can be extracted from the experimental data and used in a BSIM NMOS SPICE model. In order to extract K_P and V_{T0} the output transfer curve was plotted as shown in Figure 5.15. V_{T0} is the x-intercept and K_P is extracted by the slope information.

In order to extract R_{on}, the I-V output curves were plotted and the information was extracted from the slope shown in Figure 5.16. Since the parasitic resistance is usually expressed as $R_{on} = R_S + R_D$ with respect to V_{GS}, the extracted R_{on} was plotted with respect to $1/ (V_{GS}-V_{TH})$. Linearly interpolating the data and extracting the y-intercept gives a reasonable estimate of the $R_S + R_D$ value as shown in Figure 5.17.

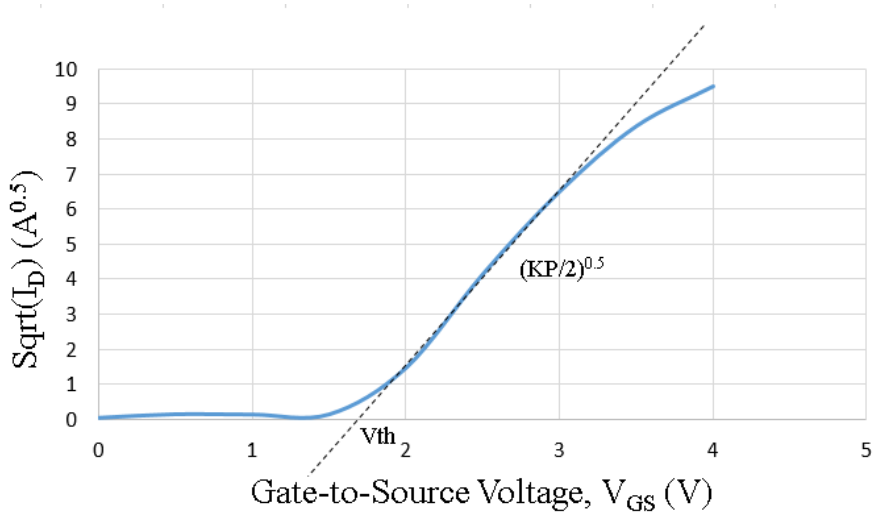

Figure 5.15: Output transfer characteristics used to extract Vth and KP.

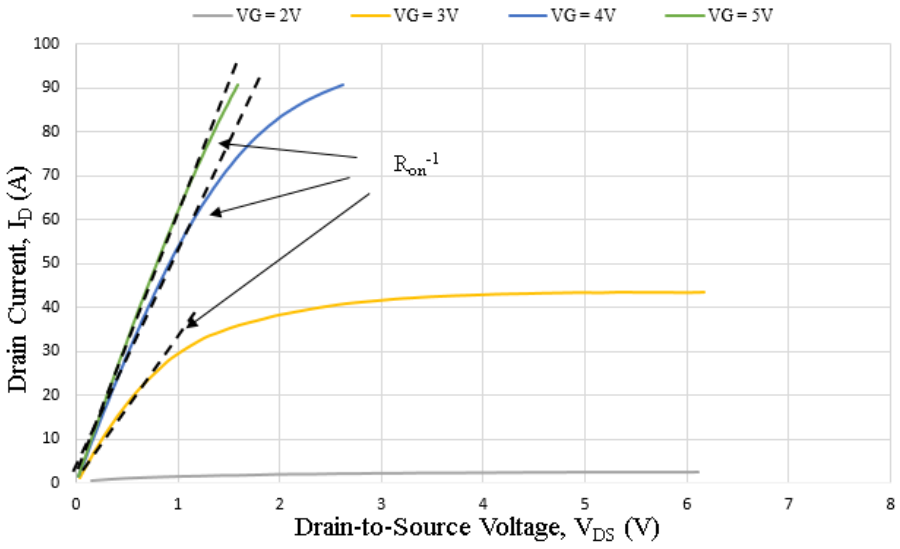

Figure 5.16: R_{on} parameter extraction from *I-V* output curves.

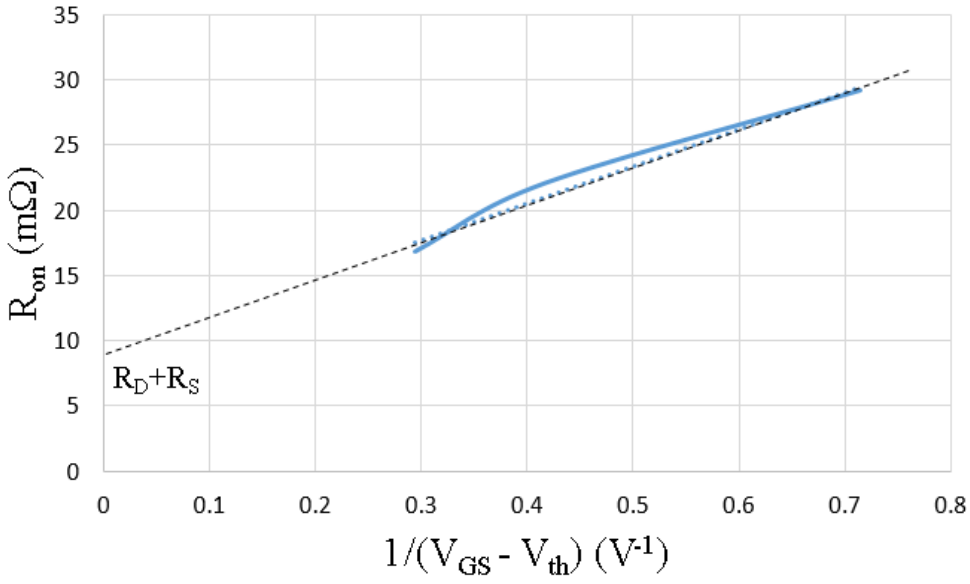

Figure 5.17: R_D +R_S parasitic parameter extraction estimate extracted from R_{on} data.

The parasitic capacitances, C_{DS0} and C_{GS} is extracted from the y-intercept of the capacitance plot with respect to V_{DS} and $V_{GS,}$ respectively. Figures 5.18 and 5.19 show C_{GS} and $C_{DS.}$

Figure 5.20 shows the experimentally extracted static *I-V* curves compared to the BSIM model implemented in LT SPICE with parameters extracted from the experimental data. Table 5.1 shows the values of the extracted parameters.

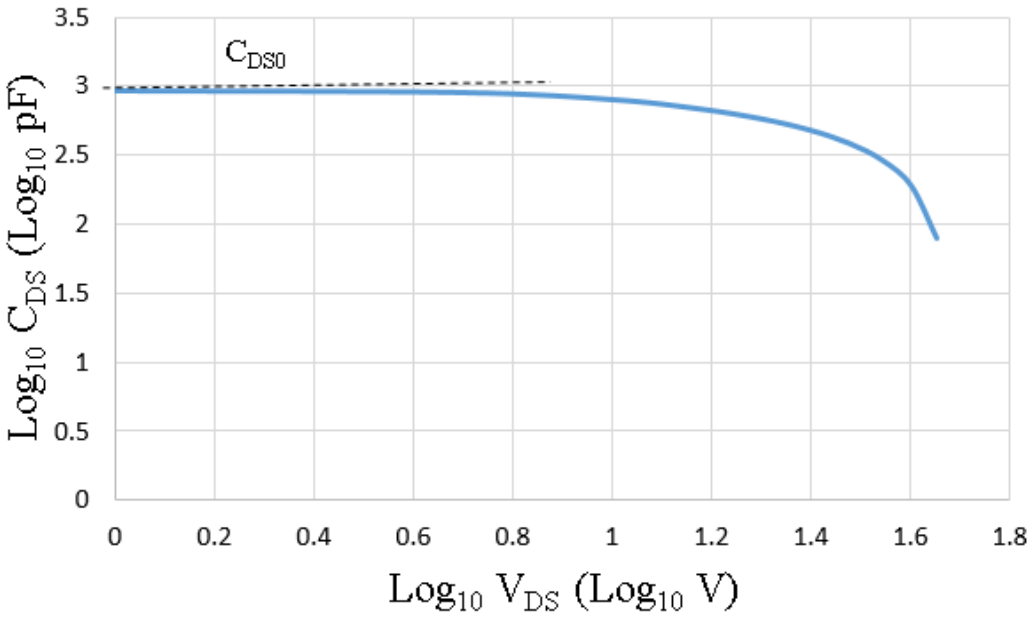

Figure 5.18: Base 10 logarithm C_{DS0} with respect to base 10 logarithm V_{DS}.

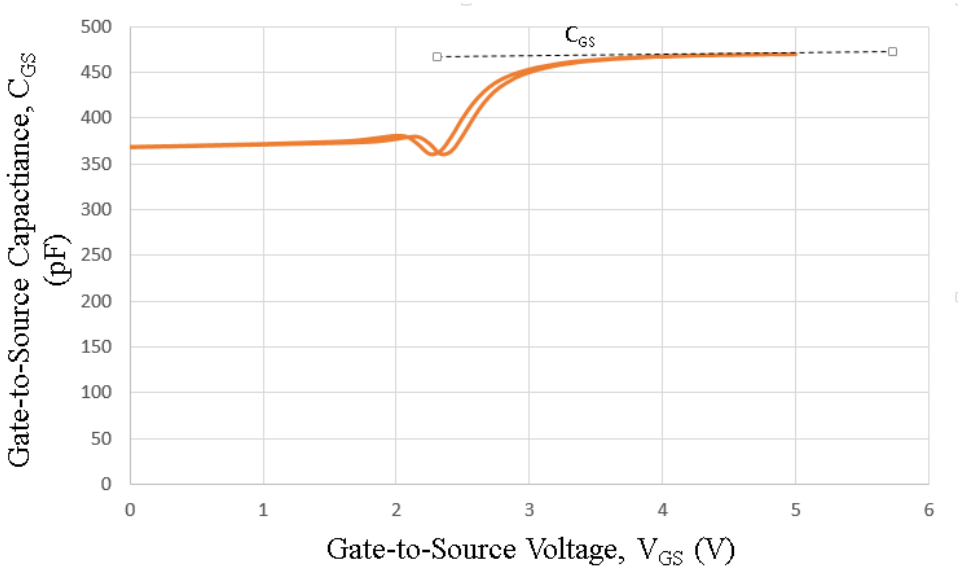

Figure 5.19: C_{GS0} parameter extraction with respect to V_{GS}.

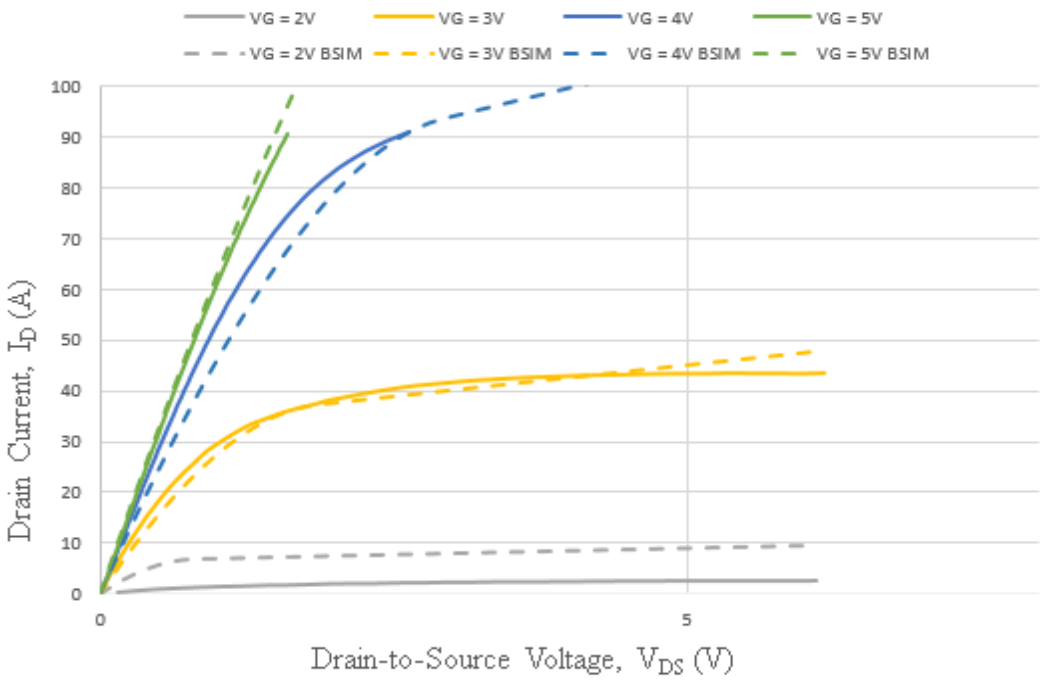

Figure 5.20: BSIM model of EPC 2022 GaN recessed HEMT.

Table 5.1 Extracted Parameters from Experimental I-V and C-V.

Extracted Parameters		
V_{T0}	Threshold Voltage	1.6 V
K_P	Transconductance Parameter	57.2 A/V^2
R_S+R_D	Parasitic Source and Drain Resistances	8.7mΩ
C_{GS0}	Gate-to-Source Parasitic Capactiance	380.2 pF
C_{DS0}	Drain-to-Source Parasitic Capacitances	912.01 pF

A simple equivalent circuit for the GaN GIT and EPC recessed HEMT was developed for SPICE circuit simulators. The HEMT device shows better correlation with the SPICE models because the behavior of the HEMT is more similar than the GIT to the MOSFET than the GIT. The conductivity modulation of the GIT causes a nonlinear response in the *I-V* characteristics that are difficult to model.

The device behavior of both devices was modeled by extracting the drain current from static *I-V* and *C-V* characteristics. The device models capture reverse conduction, a smooth transition from linear to saturation region, and parasitics present at room temperature. Future work for the model includes introducing temperature dependence or considering implementing the model into a GaN HEMT compact model as the Compact Model Coalition (CMC) agrees upon a model for GaN HEMT [44]. The model achieves expected results in DC-DC converter simulation tests with quick convergence due to the compactness of the equivalent circuit.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

A TCAD numerical simulation, an analytical compact model, and an empirical SPICE model were developed for GaN power devices. The TCAD simulation provides insight into band diagram behavior, the effects of mole fraction of Al and GaN, AlGaN thickness, AlGaN doping, and the inclusion of the *p*-GaN layer. An analytical model was based on the simulation results were a model for the threshold voltage was developed using the energy band diagram, a charge control model was developed with accurate modeling for the conductivity modulation, and the derivation of *I-V* characteristics curves. The model provides insight into the device behavior and serves as an original interpretation model for the GIT device. An empirical model produced was developed and fitted based on the Panasonic PGA26E07BA device. It includes the threshold voltage, bi-directional conductance, *I-V* characteristics for ON and OFF state device behavior and the *C-V* characteristics used to describe switching behavior in the device. Another empirical model for the EPC 2022 GaN device was extracted from experimental data and implemented into a BSIM NMOS model in LT SPICE. Future work may include a more analytical and less empirical self-heating model, more robust small-signal analytical model, analytical model for *C-V* characteristics, and parameter extraction and implementation into a universal GaN HEMT compact model after validation of a universal model by the Compact Model Coalition.

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