To the Graduate Council:

I am submitting herewith a thesis written by William F. Jones entitled "A Flexible, Low Cost, High Performance Amplifier Design for Control of an Electron Accelerator Used in an Ultraviolet Photoelectron Spectrometer." I recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

T. V. Blalock

Dr. T. V. Blalock
Major Professor

We have read this thesis and recommend its acceptance:

J. F. Pierce

James C. Hung

Accepted for the Council:

L. Evan Pell

Vice Chancellor
Graduate Studies and Research

A FLEXIBLE, LOW COST, HIGH PERFORMANCE AMPLIFIER DESIGN FOR CONTROL OF AN ELECTRON ACCELERATOR USED IN AN ULTRAVIOLET PHOTOELECTRON SPECTROMETER

A Thesis

Presented for the

Master of Science

Degree

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ABSTRACT

Techniques are developed for the design of an amplifier which must service a portion of an ultraviolet photoelectron spectrometer. The amplifier is required to drive a voltage ramp from a precision (16 bit) digital-to-analog converter onto a metal plate in a vacuum chamber. An additional grounded metal plate, together with the plate driven by the amplifier, forms an electron acceleration chamber. The chamber is intended for use with an electron energy analyzer to perform high resolution ultraviolet photoelectron spectroscopy studies. Electron kinetic energy levels of up to 40.8 eV are processed by the chamber.

Some of the requirements for the amplifier include a 50 volt (-10 to +40.8) output dynamic range, 2.5 ppm/°C maximum gain drift, 100 μV/°C maximum output offset drift, 25 ppm maximum nonlinearity, 1 mV rms maximum broadband output noise, and a minimum gain of 4 V/V. Use of the amplifier as part of a commercially available electronics package, produced in volume, places limitations on the cost and parts count of the amplifier. Ease of manufacture and maintenance must also be considered.

Several different operational amplifier designs for the driver amplifier are discussed. A particular dual op amp design has been built. Test procedures appropriate for the

application are described and test results are included. Relevance of the techniques developed for the dual op amp design is claimed for other applications requiring computer control of precise high voltage signals.

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CHAPTER I

INTRODUCTION

Background of the Thesis

An application for a low cost, low drift, low distortion, high voltage amplifier to be used in driving an electron acceleration chamber has arisen from recent developments in the field of ultraviolet photoelectron spectroscopy (UPS). Design parameters for the amplifier include a 50 volt dynamic range, 2.5 ppm/°C gain drift, 100 microvolt/°C drift at the output, 25 ppm nonlinearity, 1 millivolt rms wideband noise at the output, and a minimum gain of 4 V/V. The acceleration chamber is of a conventional type constructed of two concentric hemispherical metal plates held at different potentials in a vacuum. Electrons traveling radially outward through openings in the plates are accelerated according to the voltage supplied by the amplifier. Both the acceleration chamber and the driver amplifier were required as part of an instrument that allows high resolution UPS studies to be performed.

In UPS, electrons are emitted from a molecular sample that is being exposed to an intense monochromatic ultraviolet light source. Information about the original chemical bond of the sample can be obtained through detailed analysis of the relative kinetic energies of the emitted electrons.

Commercial development of the UPS instrument based upon a "pill box" electron energy analyzer design supplied by Allen (1976)[1] was undertaken by Special Instruments Laboratory, Inc. (Spinlab) of Knoxville, Tennessee. One goal of this project was that a low cost electronics package be constructed which would provide a means for operator and/or computer control over the analyzer. Input to the package was to take the form of panel switches and potentiometers for the operator and a digital interface for the external computer. Output was to be in the form of various adjustable voltage sources suitable for driving the appropriate electrodes in the analyzer. One particular voltage source was to be controlled by a precision digital-to-analog converter (DAC). The driver amplifier under discussion was required to drive the voltage waveform from the DAC onto the second plate of the acceleration chamber. (See Figure I.1.) Performance parameters for the driver amplifier were primarily derived from this development. However, the techniques used in meeting and measuring these parameters should prove useful to those researchers which face similar problems in computer control of precise high voltage signals.

The Acceleration Chamber

In order that the unusual requirements for the driver amplifier may be more clearly understood, a brief discussion

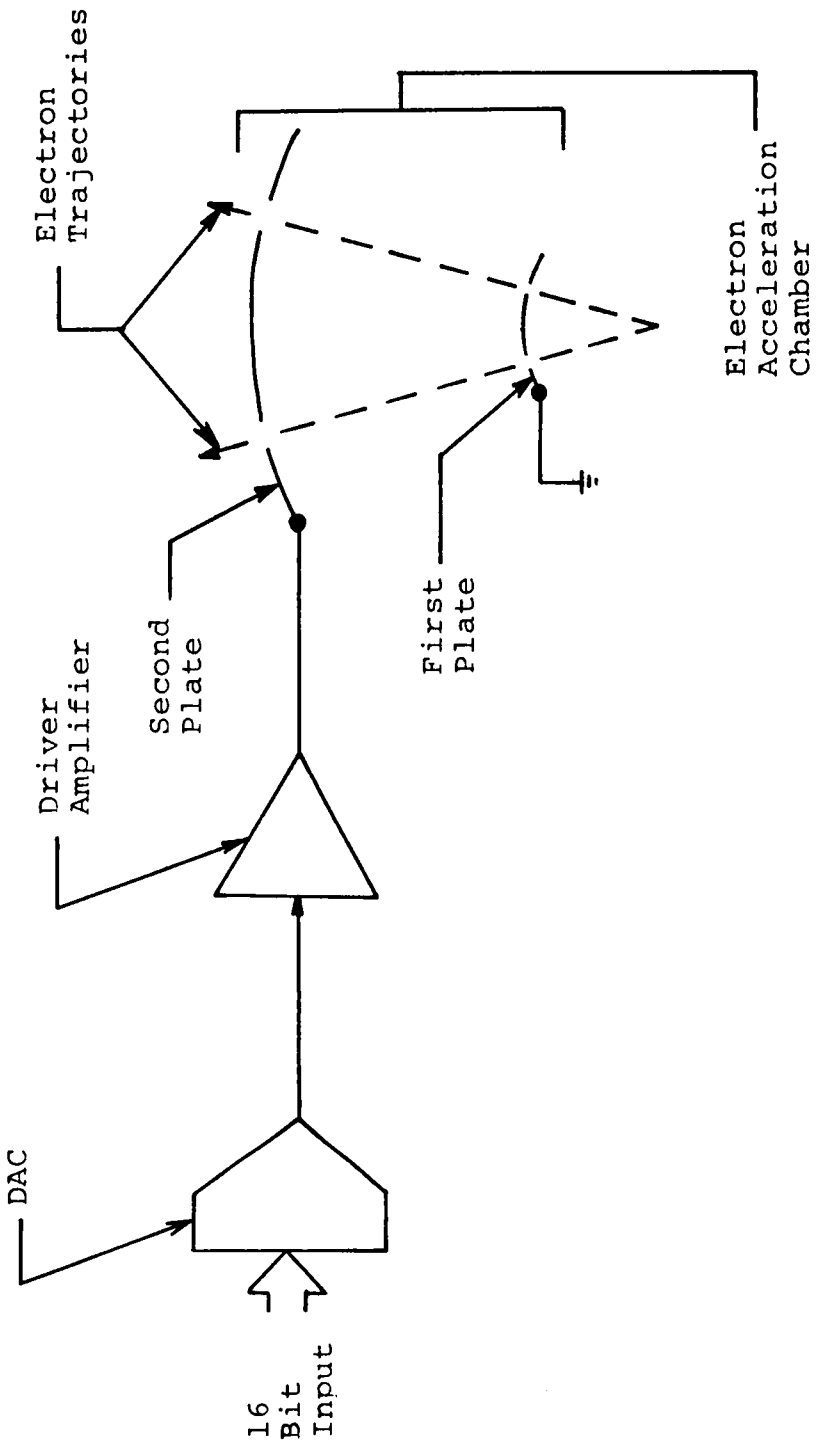

Figure I.1. Driver Amplifier Input and Output.

of the electron acceleration chamber and the manner in which the chamber is utilized is offered. Figure I.2 exhibits a simplified view of the two hemispherical plates and field fringing rings that make up the acceleration chamber. Also shown are the ultraviolet light source and the sample target area. A small portion of the electrons liberated from the molecular sample by the monochromatic light enter the slits in the first acceleration plate. As this first plate is grounded and the second plate is held at a particular voltage, an electrostatic field exists between the two plates. Electrons passing through the aligned slits in the two plates are either accelerated or decelerated according to the voltage applied to the second plate. The electron analyzer is a device that can be tuned to detect those electrons entering with kinetic energy within a specific narrow band. By knowing the kinetic energy of the electrons detected by the analyzer, the kinetic energy shift of the electrons that occurred in the acceleration chamber, and the ionization energy that caused the electron emission in the target area; the binding energy of the electrons when originally bound to the molecule may be determined.

Acceleration chambers similar to the one shown in Figure I.2 have been used elsewhere. One example can be found in the X-ray electron spectrometer apparatus described by Rigden (1972).[2] The justification for use of the chamber

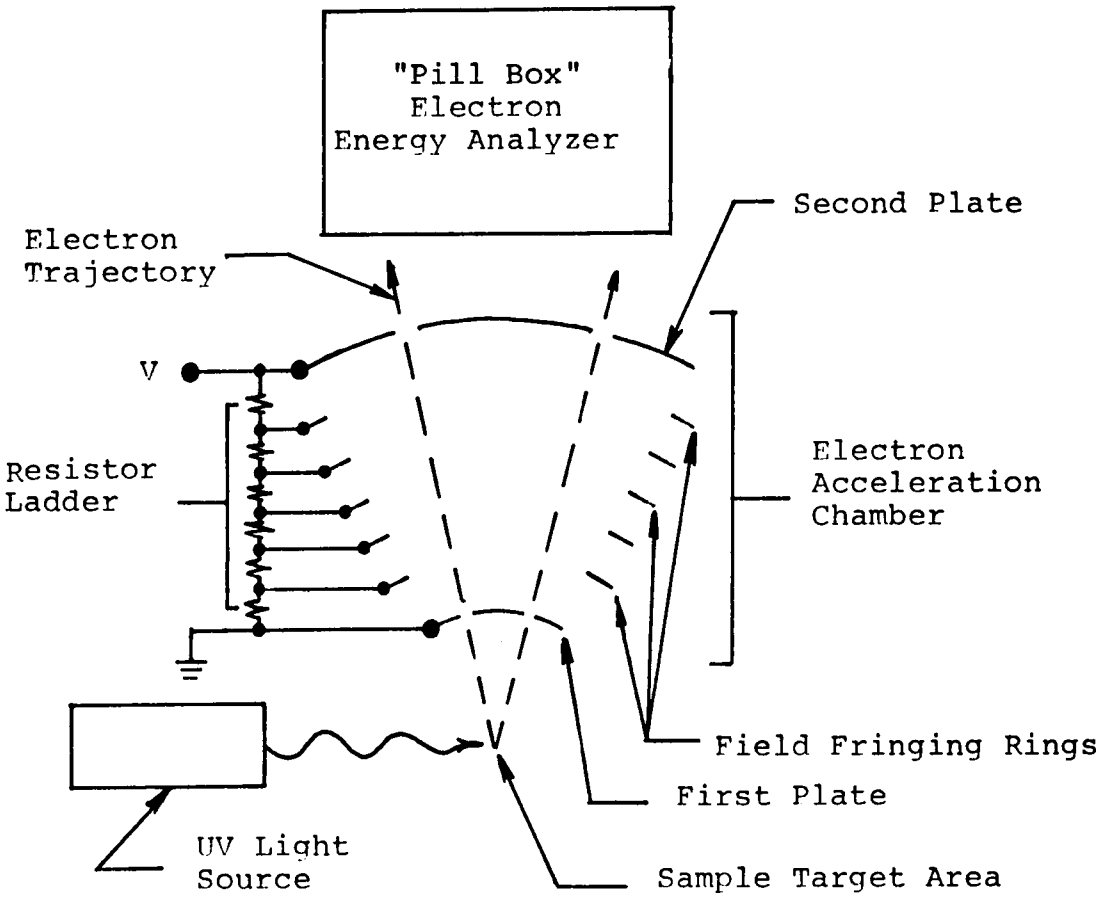

Figure I.2. Cross Sectional View and Schematic of the Acceleration Chamber.

is discussed by Sevier (1972)[3] and by Eland (1974).[4] The principle advantage is that a range of kinetic energies may be analyzed with a constant resolution. Sevier labels this process the "constant energy mode." For this application the "constant energy mode" specifies that the electron energy analyzer be set to detect electrons with a single specific energy (over a narrow band). A range of energies would be analyzed by recording the electron analyzer output (which is in the form of the frequency of an electronic pulse) as the acceleration chamber plate voltage changes. This voltage would take the form of a ramp.

Some quantitative information is desirable. The electron analyzer was designed to detect electrons exhibiting kinetic energies between 0 and 10 electron volts (eV) with a resolution of better than 10 meV. The ultraviolet radiation was to be produced by a He II discharge lamp with the characteristic photoionization energy of 40.8136 eV.[5] (A fully successful He II lamp is still in the design stage.) In order that the 40.8 eV emitted electron range and the 10 eV electron analyzer range might be fully utilized, the acceleration chamber was required to operate over a 50.8 eV range. More specifically, the chamber would have to add kinetic energy by as much as 40.8 eV and subtract kinetic energy by as much as 10 eV. Two extreme examples will illustrate these requirements. With emitted electrons

exhibiting 40.8 eV and the analyzer tuned to detect electrons with near zero kinetic energy, the acceleration chamber would be required to decelerate the passing electrons by 40.8 eV. Also with an emitted electron of near zero kinetic energy and an analyzer tuned to detect electrons with 10 eV, the acceleration chamber would be required to accelerate the passing electrons by 10 eV. These extremes are not usually encountered in practice but do represent the limiting worst case.

The voltage, V, applied to the second acceleration plate relates directly with the kinetic energy shift of the passing electrons. For 1 eV of shift, V must equal 1 volt. For V positive the electrons decelerate. For V negative the electrons accelerate. Because of the +10 to -40.8 eV range required of the chamber, the applied voltage must range from -10 to +40.8 volts. Under typical operating conditions, the analyzer might be tuned to detect 5 eV electrons and the kinetic energy range of interest for the emitted electrons might extend from 2 to 12 eV. The voltage ramp applied to the acceleration plate would then need to extend from -3 to 7 volts.

The resistor ladder shown in Figure I.2 serves to bias the field fringing rings in the conventional manner. Typical impedances from plate to plate will range from 10 k ohms to 10 M ohms, depending upon the construction of the chamber and the electrical noise filtering requirements.

Objective and Scope of the Thesis

The objective of this thesis is to present the design of an amplifier for the described application. The scope of the thesis includes an explanation of the design requirements, a justification of the design choice, the development of several test procedures appropriate for the application, and a presentation of the amplifier evaluation data produced using the developed test procedures.

CHAPTER II

DRIVER AMPLIFIER SPECIFICATIONS AND DESIGN THEORY

The purpose of the amplifier is to apply the signal from a precision DAC to the acceleration chamber plate while introducing minimal distortion and noise. Output from the DAC is to take the form of a voltage ramp. A potentiometer is to be used for zero to unity attenuation of the DAC ramp signal. Buffering of the potentiometer must be provided by a high impedance input to the amplifier. A second input to the amplifier is required to allow for full dc offset control of the voltage ramp appearing at the amplifier output. Coaxial cable is to be used to connect the amplifier output to the second acceleration plate. As the amplifier is to be part of an instrument manufactured in some quantity, the cost and parts count should be kept to a minimum. Ease of service and manufacture are also important considerations.

The simplest form that the driver amplifier can take is the conventional op amp circuit shown in Figure II.1. The input voltage V_1 is the DAC supplied voltage ramp. Potentiometer P_1 provides the ramp attenuation. Voltage V_{P1} is the attenuated ramp signal at the high impedance input to the amplifier. The voltage V_2 is supplied by a low impedance, adjustable voltage source that is very stable

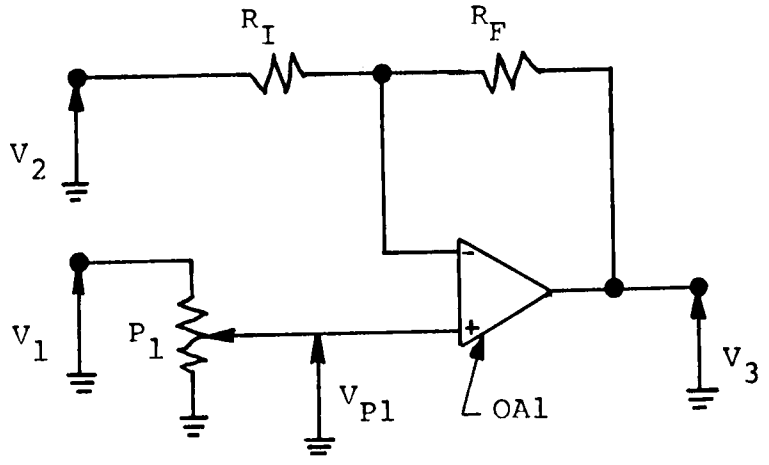

Figure II.1. Single Op Amp Driver Amplifier.

with time and temperature. The output voltage V_3 is the signal sent to the acceleration plate. By the well established op amp equation,

$$V_3 \simeq V_{P1}\left(\frac{R_F + R_I}{R_I}\right) - V_2\left(\frac{R_F}{R_I}\right) , \qquad \text{(II.1)}$$

where R_F and R_I are the feedback resistor values.

Normal operator interaction with the circuit in Figure II.1 occurs after the operator has decided upon the specific range of the electron energy spectrum that is to be scanned. The end points of the V_3 ramp are then determined. By first setting V_2 while V_1 equals zero, then setting P_1 while V_1 is set to full scale; the operator can control the ramp end points. A precision digital voltmeter (DVM) samples V_3 and displays the result, thus aiding the operator in this process. After P_1 and V_2 have been set, the operator initializes the frequency input to a binary counter. The parallel output of the counter controls the digital input to the DAC. In this manner the voltage ramp is produced at the DAC output. Duration of the ramp is determined by the frequency of the signal incrementing the binary counter. When the parallel digital interface is utilized, the binary counter would be bypassed, allowing full computer control over the DAC.

For simpler systems, output from the UPS instrument is generated by an XY plotter with the x-axis driven by the DAC

output. The frequency output from the electron analyzer is sent to a frequency-to-voltage converter and then to the y-axis of the plotter. The resulting plot has electron kinetic energy in eV on the x-axis and electron counts per second (or relative electron population density) on the y-axis. Only one sweep of the electron energy spectrum can be recorded at a time.

In one other application of the instrument, a multichannel analyzer (MCA) is used. The frequency output from the electron analyzer is stored digitally via a binary counter and memory. A different channel (i.e., memory register) in the MCA is accessed at different times during the spectral sweep. Multiple sweeps can be summed arithmetically within the MCA. This process is based on the assumption that the voltage ramp at the acceleration chamber is linear with time. Output from the MCA usually takes the form of a CRT display containing a plot of the stored information.

A more complex and possibly more powerful arrangement for the instrument would involve full computer control over the DAC input. Sampling of the electron analyzer frequency output would also be handled by the computer instead of by (or in addition to) the MCA. Advantages of this approach would include a greater degree of flexibility and the capability for automatic error correction.

Driver Amplifier Specifications

Earlier in this chapter a brief qualitative view of the driver amplifier application was given. Among the topics covered were amplifier input and output characteristics, the type of signal being processed and the economic factors. Characteristics also of interest here that were mentioned in the first chapter include amplifier dynamic range, the resistive load range of the amplifier output, and the resolution of the electron analyzer. All of these characteristics and others relate directly to amplifier operational specifications such as gain, bandwidth, noise, drift, and nonlinearity. In the following paragraphs, a quantitative development of these specifications is attempted.

Minimum Gain

For primarily economic reasons, the voltages V_1 and V_2 in Figure II.1 are to be fed by the output stages of conventional monolithic op amps. Generally monolithic op amps have a usable dynamic range limited to about ±10 volts. The gain of the driver amplifier is partially determined by this limitation. The op amp supplying V_1 can only be expected to be linear up to about 10 volts. For the V_3 ramp to span 40.8 volts while the V_1 ramp extends from zero to +10 volts, a minimum positive gain of 4.08 V/V is established for the driver amplifier. In practice larger gains of from

10 to 20 V/V can prove to be beneficial, particularly by reducing the requirements of the op amps that supply voltages V_1 and V_2.

Noise

As mentioned earlier, the electron analyzer was designed to have a resolution of 10 meV or better. Simply stated, this specification means that the analyzer should be able to distinguish between electrons that differ in kinetic energy by as little as 10 meV. In order that this 10 meV performance level not be degraded, the kinetic energy shift produced by the acceleration chamber was to have an uncertainty of less than 1 meV. Precise control of this shift along with careful control of other system parameters would mean that a more accurate picture of the original chemical bond could be drawn. Resultantly, the allowable uncertainty of the plate voltage was to be less than 1 millivolt (mV). More specifically, the electrical noise exhibited by the voltage at the second acceleration plate was to be less than 1 mV rms over a broad frequency range.

Ramp Linearity

Coverage of the entire 40.8 eV spectrum requires that the voltage ramp at the acceleration chamber cover a 40.8 volt range. (Offset control of the ramp accounts for the other 10 volts of dynamic range.) The 1 mV uncertainty of

the 40.8 volt ramp means that a ramp nonlinearity of 25 ppm is required. (Incidentally, this specification fixes the DAC resolution at 16 bits.)

One limitation to ramp linearity, especially at faster ramp speeds, is the bandwidth of the driver amplifier. A brief mathematical treatment of the relationship between the nonlinearity of a fixed duration ramp signal and amplifier bandwidth is offered in Appendix A. Typical ramp durations extend to as short as 0.05 seconds (primarily useful for computer controlled systems). The results of the Appendix A treatment indicate that the bandwidth necessary for reproduction of a 0.05 second ramp to within 25 ppm is about 127 kHz.

Another limitation to ramp linearity, especially for longer ramp durations, is the offset and gain drift which are functions of time and ambient temperature. Typical ramp durations of up to 50 hours are required when unusually low electron counts per second magnitudes are encountered (for computer, MCA, and XY plotter systems). Because the driver amplifier was to be part of an electronics package offered for sale, the driver amplifier was expected to be used under varied and rather poorly controlled environmental conditions. Ambient temperature variations over a 50 hour period in user's laboratories were assumed to be no worse than about 10°C. Preserving the 1 mV uncertainty under these conditions requires that the offset drift at the output of the driver

amplifier be less than 100 μV/°C and 1 mV/50 h and that the gain drift be less than 2.5 ppm/°C and 25 ppm/ 50 h.

Offset drift for the amplifier in the figure on page 10 is usually specified in terms of input offset voltage and current drift. For a positive forward gain of 5 V/V, the input offset voltage drift value necessary to meet the 100 μV/°C output drift is 20 μV/°C. (This input offset voltage drift specification can be misleading because of the thermal feedback effects discussed a bit later.) In this particular application the effect at the output due to variations in the input current is generally negligible, at least for most FET input and instrumentation grade bipolar op amps.

Low frequency gain drift for the Figure II.1 circuit is largely dependent upon the tracking characteristics of the two feedback resistors (ignoring P_1), especially for large loop gain. To maintain a voltage drift at the output of less than 1 mV over 10°C, R_F and R_I must have a tracking temperature coefficient of less than 2.5 ppm/°C. Also an additional effect must be considered. Temperature changes in R_F and R_I can result from internal ohmic heating as well as from ambient fluctuations. The current flowing in R_F and R_I may be assumed to be equal if op amp input bias currents are small. And, the ratio of the power levels dissipated in R_F and R_I as the amplifier is used may be shown to be equal to the ratio R_F/R_I. Typically the ratio of R_F to R_I will be

in the range of 4 to 20 for this application, and resultantly the power dissipated in R_F will be from 4 to 20 times that of the power dissipated in R_I. Either the resistor power coefficient as defined by Anderson (1978)[6] must be sufficiently low for R_F and R_I, or a good thermal contact between R_F and R_I must be maintained.

Still another limitation to the ramp linearity at low speeds is the thermal feedback effect discussed by Solomon (1974).[7] Variations in the power dissipated by the transistors in the output stage of the op amp caused by the output voltage and current changes can induce a temperature related offset voltage in the input stages. This effect is especially important for op amps with good thermal contact between the output and input stages. For the driver amplifier, 40 volt output levels with 10 k ohm loads mean that fluctuations in the heat generated by the output stage can be large--up to 0.25 watts in a typical case. Consideration must then be given to the degree of the thermal contact between the output and input stages.

Capacitive Loading

Capacitive loading of the driver amplifier in this application will be primarily the result of the coaxial cable connecting the driver to the acceleration plate. Typically less than 20 feet of coax will be used with a rating of

30 pF/ft. The capacitive load presented to the driver amplifier is then expected to be 600 pF or less. The inductive load due to the coaxial cable is generally not a significant problem.

Design Economics

The driver amplifier was to be part of an electronics package that would be manufactured in volumes of 5 to 10 per year and be sold for use both domestically and internationally. The component costs, parts count, cost of assembly and ease of service of the driver amplifier as well as the entire package were important considerations. For these reasons a single, low cost op amp that would satisfy all requirements was very desirable. Descrete designs, although offering the possibility of premium performance, were less desirable because of the increased parts count. Temperature controlling ovens could have been implemented to reduce the operating temperature variations but were to be avoided due to the increased cost and maintenance burden. The following section deals with the limitations encountered in the single op amp approach and discusses some additional alternatives.

Driver Amplifier Design Alternatives

An effort was made to implement a suitable driver amplifier. Information about the available high voltage op amps was collected so that the simple circuit in Figure II.1

(page 10) might be implemented. A portion of this information appears in Table II.1. Wide variations exist in both the price and performance of the 16 op amps appearing in Table II.1. Devices of particular interest include the 1032 with the lowest cost and largest capacitive load rating and the AM301B with the lowest cost for a 20 μV/°C input offset voltage drift rating. The best rated device appeared to be the 171K with the lowest input offset voltage drift of 15 μV/°C.

Because of the cost sensitive nature of the driver amplifier design, a certain amount of research went towards a design that might utilize the least expensive high voltage op amp and, in some manner, boost the performance without seriously increasing the parts count or cost. One avenue for this approach was offered by National Semiconductor (1976).[8] The LM321A precision preamplifier used with the 1032 op amp appeared to be an attractive method for increasing the loop gain and decreasing the input offset voltage drift. Another strategy was suggested by Ott (1973)[9] in which an active drive of the potentiometer trimming inputs of the 1032 would be made by a low cost low voltage op amp. Increased loop gain and decreased drift were also indicated. Still another possibility involved the design of an op amp current source suggested by Widlar (1973).[10] The current source was to drive the summing junction of the 1032 directly

TABLE II.1

OP AMP COMPARISON

Device Number	Manufacturer	Output Voltage	Input Offset Voltage Drift (μV/°C)	D.C. Gain (db)	Max. Cap. Load (pF)	Single Quantity Prices
1032	TELEDYNE PHILBRICK	±115V	50	100	0.01*	$ 59.00
1022	TELEDYNE PHILBRICK	±140V	50	120	0.001*	$ 98.00
3581JM	BURR-BROWN	±70V	25	112	-	$ 74.20
3582JM	BURR-BROWN	±145V	25	118	-	$ 86.00
3583JM	BURR-BROWN	±140V	25	118	-	$ 85.00
171J	ANALOG DEVICES	±140V	50	120	-	$ 88.00
171K	ANALOG DEVICES	±140V	15	120	-	$105.00
AM301A	DATEL	±110V	50	120	500	$ 75.00
AM301B	DATEL	±110V	20	120	500	$ 85.00
AM302A	DATEL	±140V	50	120	500	$ 90.00
AM302B	DATEL	±140V	20	120	500	$120.00
AM303A	DATEL	±140V	50	120	-	$ 90.00
AM303B	DATEL	±140V	20	120	-	$120.00
1810	D.M.C.	±140V	50	120	500	$ 95.00
1811	D.M.C.	±140V	20	120	500	$100.00
ZA136	ZELTEX	±100V	50	100	-	$218.00

*Values are in μF and are not worst case.

Note: All performance values are worst case except where noted.

with implied improvements similar to the earlier designs. A final possibility would have utilized the 1032 as a voltage booster for a conventional high performance monolithic op amp. Advantages of this last approach include those improvements mentioned earlier and a few others.

Design Decisions

A version of the driver amplifier based upon the "voltage booster" approach was the design choice for the driver amplifier. Design flexibility, limited thermal feedback, low cost, and moderate parts count are the principle justifications for this decision. The schematic in Figure II.2 illustrates the amplifier design. Voltages V_1, V_{P1}, V_2 and V_3 are functionally the same as for the Figure II.1, page 10, schematic. The op amp OA1 is the lowest cost, high voltage device listed in Table II.1. Op amp OA2 is a Precision Monolithic OP-07C device with conventional ±15 volt supply lines and 741 compatibility. Low cost carbon resistors R_{BF} and R_{BI} together with OA1 form the voltage booster stage with a positive gain of 5.25 V/V. Resistors R_F and R_I and potentiometer P_1 are also functionally equivalent to those used in Figure II.1 and Equation II.1. R_F and R_I are actually part of a single thin film resistor network (#698-3-R10KF) supplied by Beckman.

One advantage of this driver amplifier design is that the input and output characteristics of the circuit can be

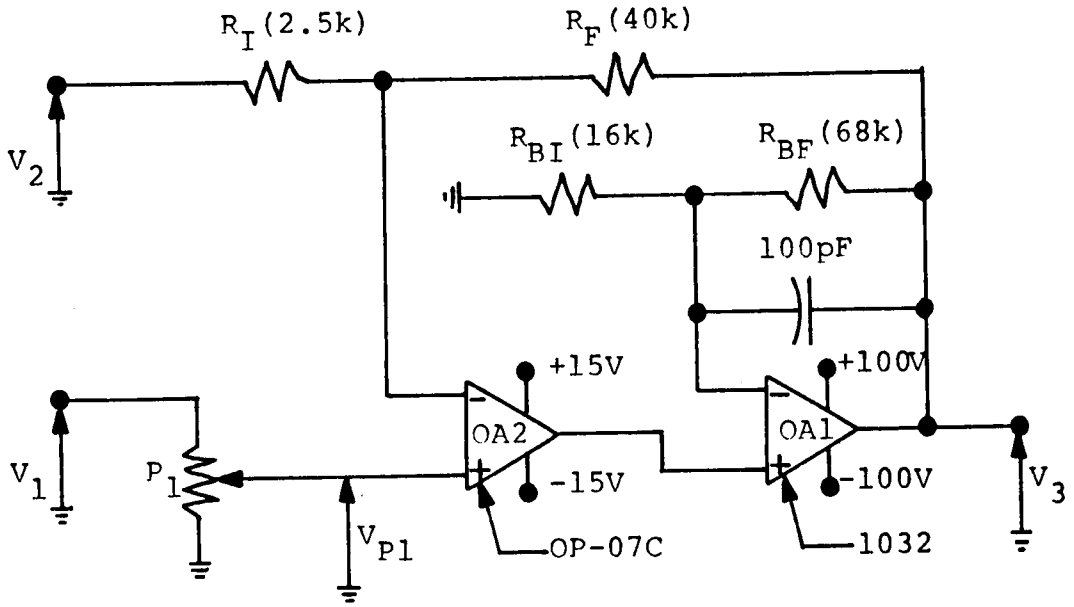

Figure II.2. Dual Op Amp Driver Amplifier.

chosen independently. If the voltage drift requirements change, a new choice for OA2 may be made. If the load requirements change, a new choice for OA1 may be made. This type of flexibility can be beneficial for both commercial and pure research applications where design requirements are typically in a state of flux.

Another advantage of this dual op amp approach lies in the extremely limited thermal feedback path that exists between the output stage of OA1 and the input stage of OA2. The result is that the driver amplifier offset drift at the output will be much less affected by the resistive loading at V_3. Note that the most important thermal feedback path lies within OA2. For this reason the output of OA2 is loaded only by the high impedance positive input to OA1, reducing the thermal effects within OA2 by minimizing power dissipation in the output stage of OA2.

An additional advantage lies in the actual cost of the circuit. There is less than a $10.00 difference between the cost of the circuit in Figure II.1 on page 10 (utilizing a 1032) and the cost of the circuit in Figure II.2. There is more than a $15.00 difference between the 1032 version of the Figure II.1 circuit and a similar circuit utilizing any other op amp from Table II.1. Also, another op amp from Table II.1 with sufficient operating characteristics may be more expensive by $26.00 to $46.00 or more.

The primary disadvantage of the circuit in Figure II.2 is the increase in parts count by four (over the Figure II.1, page 10, circuit) and the associated increase in complexity. Considering the cost savings, the increased parts count does not seem particularly significant. Another disadvantage is the greater attention that must be paid to circuit instability. This topic is discussed in detail in Appendix B.

CHAPTER III

ANALYTICAL AND EXPERIMENTAL RESULTS

The evaluation of the dual op amp driver amplifier will encompass several different test procedures with some appropriate analysis. A linear systems analysis of the amplifier is offered. Various conventional test procedures for noise, gain and offset drift, and thermal feedback effects are also presented along with the test results. In addition, an unusual test for low frequency nonlinearity is discussed. Some appropriate analysis and data from this nonlinearity test are given.

Bandwidth Characteristics

In Appendix B is a linear systems analysis for the dual op amp driver amplifier in Figure II.2. Some of the important amplifier characteristics found in this analysis based upon typical device specifications are shown in Table III.1 along with some of the measured values. The agreement between the two columns in Table III.1 is quite good considering that the Appendix B calculations utilized typical and not actual device parameters. Also the assumption made in Appendix B concerning the negligible effect of poles and zeros above 1 MHz seems to have been justified.

TABLE III.1

CALCULATED AND MEASURED AMPLIFIER GAIN AND BANDWIDTH PARAMETERS

Parameter	Calculated	Measured
DC Loop Transmission	102 db	106 db
Phase Margin	51°	35° to 45°
3 db Bandwidth	150 kHz	170 kHz
DC Closed Loop Gain (Positive)	17 V/V	17 V/V
Peak Gain	23.2 V/V	22.1 V/V
Peak Gain Frequency	73 kHz	80 kHz

Another relevant measurement made during this test phase was of the large signal bandwidth. A 3 volt peak-to-peak sinusoidal input to the amplifier (51 volts at the output) displayed 3 db attenuation at the output at 19 kHz. The effect that this large signal bandwidth will have on the fast ramp linearity is probably small. A 40 volt ramp of 0.05 second duration has a fundamental frequency component at about 20 Hz with about a 13 volt magnitude. The important nonlinearity effects attributable to limited bandwidth relate to the higher frequency components that have a much smaller magnitude. Slew rate is a parameter often associated with the large signal bandwidth. For a 40 volt, 0.05 second ramp the slew rate required is only 0.8 mV/μs.

Appendix A deals with the bandwidth requirements for an amplifier having a single real pole. Appendix B reveals that the dual op amp driver amplifier has two complex poles and a response that is not as flat as that of a single pole amplifier. Additional analysis in Appendix A could easily resolve this dilemma, but for a close approximation the dual op amp driver amplifier can be assumed to have a single pole response. Also, the bandwidth is larger than would be generally required. According to Appendix A the 170 kHz driver amplifier should track a 40.8 volt ramp of 0.05 second duration to within 0.76 millivolts.

Noise

Broadband noise measurements of the driver amplifier were made with a Hewlett-Packard Model 3400A Rms Voltmeter. The meter has a frequency response of 10 Hz to 10 MHz. With V_{P1} and V_2 connection to ground, the noise measured at V_3 was less than 0.3 mV and typically 0.2 mV.

A rough approximation for the expected output noise level under these conditions is in order. The primary noise source is the input noise voltage of the OP-07C. An input wideband noise versus bandwidth plot is provided on the OP-07C data sheet. Noise values are in actuality for a more expensive version of the OP-07C but will be assumed to be appropriate. Also, the plot must be extrapolated for a 170 kHz bandwidth. An input noise voltage of 10 μV rms is indicated. With a forward gain of 17 the expected output noise is 0.17 mV rms.

Agreement between the measured and expected output noise voltages is within a factor of two, with the measured values being higher. A more rigorous treatment of the noise sources within the driver amplifier would include the thermal noise generated by P_1, R_I and R_F and the input noise current of the OP-07C.

Note that the driver amplifier must operate for periods as long as 50 hours and therefore has a low frequency cutoff of 5.6 μHz. Measuring the 1/f noise which dominates the low

frequency spectrum is more difficult and time consuming and was not attempted. However, an estimate for the additional noise that would result from 1/f noise is possible.

In a text by Motchenbacher (1973),[11] the increase in noise resulting from increased amplifier "on" time is discussed. The longer the amplifier "on" time, the lower is the amplifier low frequency cutoff and the higher is the 1/f noise contribution. Noise should increase as the square root of the number of additional decades of bandwidth. In this application the additional bandwidth amounts to 6.25 decades. This added low frequency bandwidth should increase the output noise by a factor of 2.5. Such an increase should not seriously impair the operation of the driver amplifier.

Drift with Temperature

Equipment used for the gain and offset temperature drift test included a Hewlett-Packard 3460B ($5\frac{1}{2}$ digit) Digital Voltmeter (DVM), a hand held forced air heat gun, a 2.5 volt reference, and a bimetal thermometer. V_2 was shorted to ground for the entire test and P_1 was not used. V_{P1} was shorted to ground for the offset measurement and connected to the 2.5 volt reference for the gain measurement. A range of air temperatures of over 30°C was provided by the heat gun. With the gun on maximum, a stream of 55°C to 60°C air could be applied evenly about the driver amplifier. With the gun set to the same fan speed as before but

without the heat source, a stream of 25°C to 30°C air could be applied. Measurements of V_{P1} and V_3 were made by the DVM as the air temperature about the driver amplifier changed. Readings were made of the different air temperatures as the DVM values were recorded. The averaged results from three temperature cyclings are shown in Table III.2. The estimated values for gain and offset drift (developed in the following paragraphs) are also included for comparison.

An expression for output offset drift (V_{3D}) is developed in Appendix C and is

$$V_{3D} = +M_{DC} \frac{R_F R_I}{R_F + R_I} \left(I_{BD} - I_{OFFD}\right) + M_{DC} V_{OFFD} \ . \qquad \text{(III.1)}$$

For the circuit in Figure II.2 (page 22), M_{DC} = 17 V/V, R_I = 2.5 k ohms and R_F = 40 k ohms. The data sheet for the OP-07C lists the worst case values for I_{BD}, I_{OFFD}, and V_{OFFD} to be 50 pA/°C, 50 pA/°C, and 1.8 μV/°C respectively. These values are only guaranteed for 90 percent of the units. To compute a worst case V_{3D}, the sign of the offset parameters must be arbitrarily chosen. I_{BD} and V_{OFFD} will be considered positive quantities and I_{OFFD} negative. Substituting into the drift equation gives

$$V_{3D} = 17 \frac{(2.5k)(40k)}{(2.5k + 40k)} (50pA/°C - (-50pA/°C)) + 17(1.8\mu V/°C) \ , \qquad \text{(III.2a)}$$

$$= 4\mu V/°C + 30.6\mu V/°C \ , \qquad \text{(III.2b)}$$

$$= 34.6\mu V/°C \ . \qquad \text{(III.2c)}$$

TABLE III.2

ESTIMATED AND MEASURED OFFSET AND GAIN DRIFT

Parameter	Estimated	Measured
Output Offset Drift	34.6 μV/°C	50 μV/°C
Gain Drift	± 5 ppm/°C	1.7 ppm/°C

A discrepancy of about 15.4 μV/°C exists between the estimated and measured offset drift. This discrepancy is something of a surprise since the worst case drift values were used in the calculation. An explanation for the error may be found in the elevated test temperatures and the lack of 100 percent device testing by the manufacturer. Still, the magnitude of the output offset drift is sufficiently small to meet the 100 μV/°C limit.

Estimation of the gain drift with temperature depends primarily upon the tracking qualities of R_F and R_I and to a lesser extent upon the loop gain drift. The Beckman thin film network used to implement R_F and R_I has a specified tracking temperature coefficient of ±5 ppm/°C. The schematic in Figure III.1 indicates the manner in which the network was connected to produce R_F and R_I. This circuit was chosen to maximize the thermal contact between R_F and R_I and to maximize the forward gain of the driver amplifier. The increased capacitive coupling between R_F and R_I produced by this circuit seems to have had negligible effect upon the amplifier. The worst case ±5 ppm/°C tracking of R_F and R_I is not sufficiently low to justify the use of the Beckman device in production of the driver amplifier. A thin film network produced by Hycomp (#HC150) has a tracking temperature coefficient listed at ±2 ppm/°C and may be the better choice for this application. Use of the Beckman device in

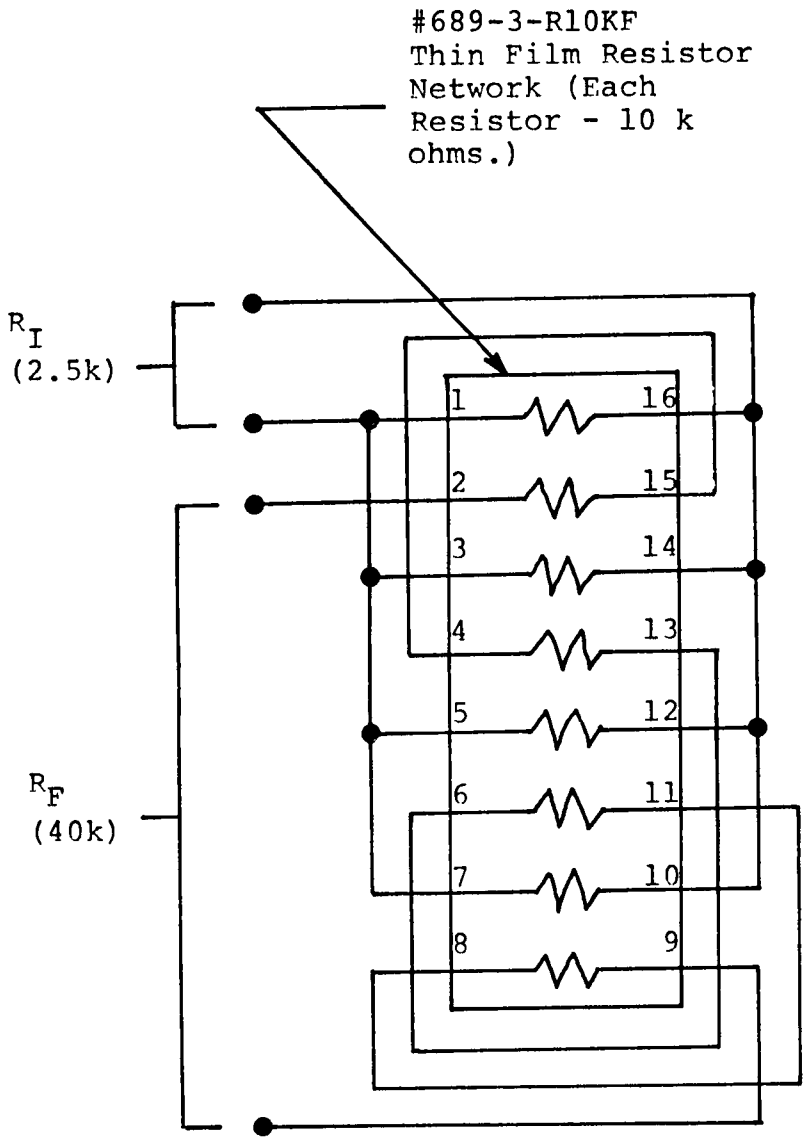

Figure III.1. Resistor Network Schematic.

the test circuit was justified because the network was offered through a distributor as a free sample and seemed to perform sufficiently better than the worst case specifications. In any event a better estimation of gain drift than ±5 ppm/°C will not be attempted here.

Drift with Time

Gain and offset drift with time of the driver amplifier were checked with a fairly simple test procedure. As before, V_2 was grounded and P_1 was not used. A SPDT switch was used to alternately connect V_{P1} to ground and to the 2.5 volt reference. The same $5\frac{1}{2}$ digit DVM was used to monitor V_{P1} and V_3.

Two types of time related measurements were made. One involved letting the amplifier achieve thermal and electrical steady state and recording the DVM readings at fairly regular intervals over several hours and days. Long term tests were made for V_{P1} at ground potential and at 2.5 volts. The other time related measurement involved the thermally affected settling time of the amplifier. This measurement was performed so that the magnitude of the thermal feedback effect could be observed. Settling time to within 25 ppm was measured with the DVM which meant that the minimum settling time that could be resolved was about 0.5 seconds. The step input to the driver amplifier was provided by the

switching of V_{P1}. Amplifier components affected by self-induced thermal transients are primarily R_F, R_I, and the OP-07C. Note that this settling time test is intended to insure that the operator adjusting P_1 will not be hampered by short term fluctuations in the ramp magnitude.

Results of the long term tests were very satisfactory. With V_{P1} set at approximately 2.5008 volts, the DVM readings of V_3 were not observed to vary from 42.522 volts for over 50 hours. Also, the recorded ambient temperature during this 50 hour period varied by over 10°C. (Temperature variations of this magnitude were produced by adjustment of the room heating system.) Long term offset drift measured through a 19 hour period was found to be less than 150 μV.

Results of the thermal settling time test indicate that 25 ppm settling in less than 0.5 seconds can be expected for V_3 stepping both from zero to 40 volts and back. Also, in what is believed to be a typical example, V_3 in stepping from 40 to zero volts settled to within approximately 70 μV of the steady state in less than eight minutes.

Low Frequency Linearity

A simple method for measuring the low frequency linearity of the driver amplifier is illustrated by the schematic in Figure III.2. Originally an attempt was made to measure the voltage that occurred between the differential

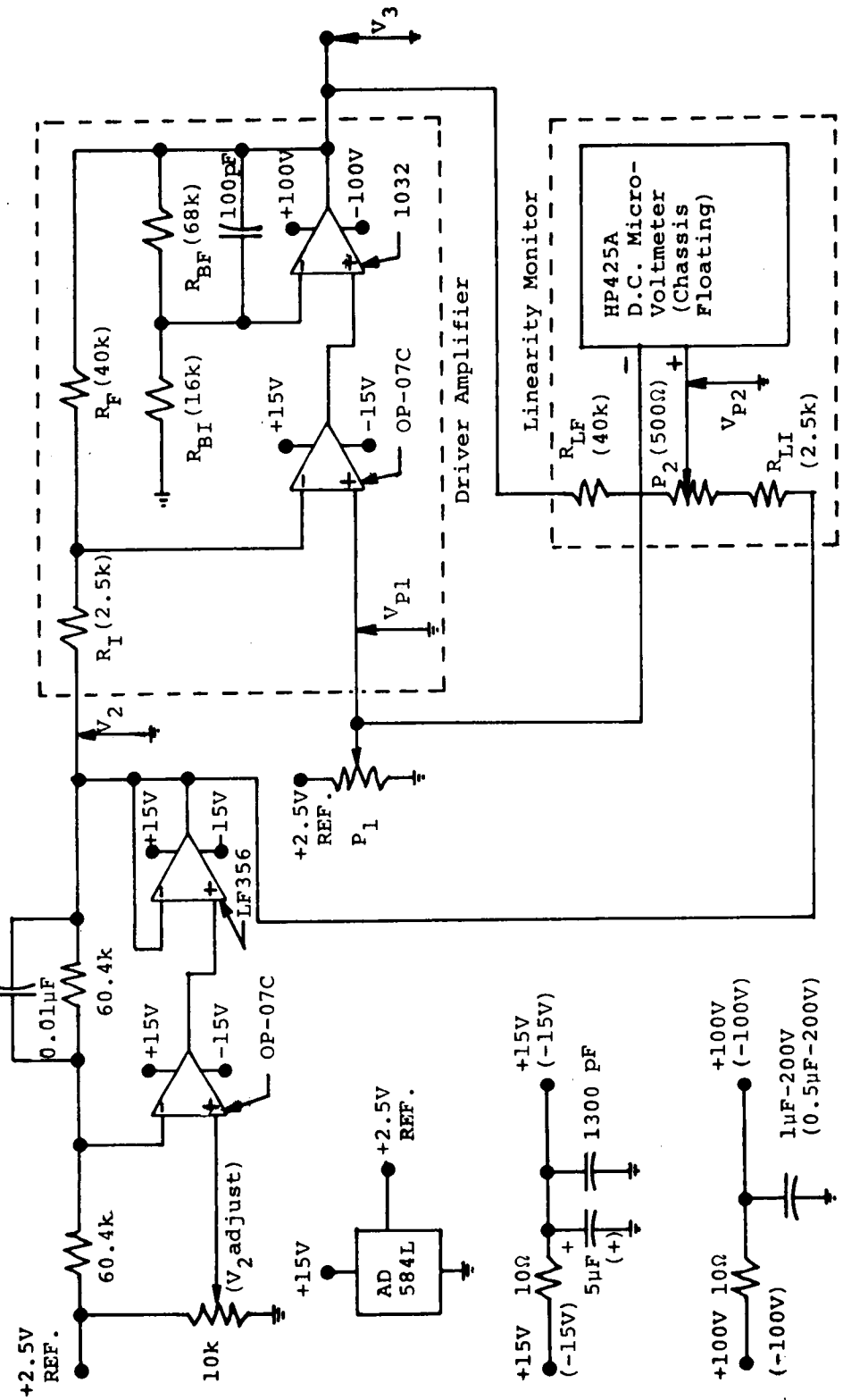

Figure III.2. Linearity Test Schematic.

inputs of the OP-07C. Irregularities present in this differential error voltage would indicate corresponding irregularities in V_3. Ideally the voltage across the differential inputs would be equal to zero; but finite loop gain, nonstable feedback resistors, and the input offset voltage produce a definite error voltage. If, however, the loop gain were sufficiently large, the resistors sufficiently stable, and the input offset voltage constant; then a measure of this error voltage would also be a measure of the circuit nonlinearity.

The magnitude of the voltages that would need to be measured at the OP-07C inputs are on the order of 25 ppm of 2.4 volts or 60 μV. This measurement could be made by a Hewlett-Packard Model 425A, which is a chopper stablized dc voltmeter with 1 μV or better sensitivity and a high degree of noise rejection. However, the capacitive loading of the op amp inputs resulting from the voltmeter lead capacitance caused the circuit to become unstable. This problem was resolved as is shown in Figure III.2.

A thin film resistor pair equivalent to R_F and R_I (namely R_{LF} and R_{LI}) with a trim pot (P_2) connected as shown were used to simulate the driver amplifier summing junction voltage. The potentiometer P_2 was used to overcome slight differences in the ratios R_F/R_I and R_{LF}/R_{LI}. The development in Appendix D indicates that under ideal conditions the

properly adjusted P_2 slider voltage (V_{P2}) will equal the P_1 slider voltage (V_{P1}) less the input offset voltage of the OP-07C. (Input current effects are small and can be ignored.)

Note that the 1 M ohm impedance presented by the HP425A input could provide a positive feedback path and affect the output voltage. However, because the currents flowing through the voltmeter leads are so small; the effects on V_3 can be shown to be negligible. Also note that the voltmeter lead capacitive load is now out of the circuit loop and does not cause circuit instability.

The procedure followed for the linearity test involved adjustment of P_1, V_2, and P_2 while recording the voltmeter readings. Simulation of the voltage ramp that would normally appear at V_{P1} was achieved by connecting V_1 to a 2.5 volt source and adjusting P_1. Readings of the 425A were recorded at several points along the zero to full scale adjustment of P_1. V_2 was set to zero, +0.6 volts, and -1.26 volts during different trials while P_1 was adjusted. Generally the -10 to +40.8 volt dynamic range of V_3 was not exceeded. Ambient temperature variations during the test were less than a few degrees Centigrade.

The magnitude of the voltage as measured by the 425A after P_2 was adjusted was typically 20 μV. This voltage is in keeping with the listed 60 μV typical input offset voltage

of the OP-07C. The variations of this voltage that occurred as P_1 was adjusted from zero to full scale were (during separate trials) as large as 11 μV and as small as 4 μV.

These readings imply an amplifier nonlinearity of less than 5 ppm, but such a conclusion cannot be drawn without more complete information about the power coefficient and tracking characteristics of the thin film resistor networks. The only available indication of the resistor network power coefficient can be found in the earlier thermal transient tests of the amplifier. Because the amplifier settled so quickly to 25 ppm, the resistors R_F and R_I may be assumed to track at least as well as 25 ppm when typical circuit voltage levels are applied. Also, the small magnitude of the implied nonlinearity indicates that the two resistor networks track at least as well as 5 ppm. If a conclusion from this linearity test is to be reached, then the amplifier nonlinearity not due to fluctuations in R_F and R_I is indicated to be less than 5 ppm and the overall nonlinearity is indicated to be less than 25 ppm.

Loading Effects

The capacitive loading limit of the driver amplifier has been found to be over 1000 pF. The required resistive loading limit of 10 k ohms has also been successfully tested. Earlier tests for bandwidth, noise, gain and offset drift,

and nonlinearity were found to be negligibly affected by 1000 pF and 10 k ohm loads.

Additional Notes

Four miscellaneous items pertaining to the driver amplifier should, if discussed, aid the implementing researcher. These are production limitations with the OP-07C, boosting the capacitive load limit, noise induced dc offset, and the design of the sources for V_1 and V_2.

The OP-07C utilized in the design of the driver amplifier proved to be quite sufficient. One contributor to this success was the high open loop gain of the OP-07C (over 700,000 V/V). The open loop gain of the OP-07C directly affects the magnitude of the driver amplifier loop transmission, which in turn can affect the amplifier linearity and gain drift. Worst case open loop gain for the OP-07C is listed at 120,000 V/V. A problem may occur in quantity production of the driver amplifier if an OP-07C with near worst case open loop gain is used. A retest of linearity and gain drift may be in order for a driver amplifier which utilizes an OP-07C with near worst case open loop gain. The results of this retesting will determine whether or not the OP-07C is suitable for use in quantity manufacture of the driver amplifier.

Larger capacitive loads than the 600 pF discussed with the amplifier requirements might possibly be encountered in

slightly different or more stringent applications. The capacitive loading limit of the driver amplifier was measured to be at over 1000 pF. The largest load that was successfully applied was 1450 pF. Larger loads caused oscillations to occur. These oscillations made the amplifier much too noisy to be useful. In an article by Wojslaw (1974),[12] techniques are discussed which can boost the capacitive load limit of the driver amplifier. These techniques are very inexpensive, typically involving two passive components.

Noise induced dc offset effects as described by Duffy (1975)[13] can be important for this application. Most amplifiers respond with a dc shift in the output when a high frequency noise source is applied to the input. The principle high frequency noise source in this application is the digital electronics used to service the DAC. Typical clock frequencies for digital electronics in this instrument range from 1 to 10 MHz. The magnitude of this high frequency noise that reaches the driver amplifier depends in part upon the grounding techniques and the levels of power supply decoupling that are used. Also the degree to which the DAC transmits digital noise to the analog output can be important. Offset measured at the output of the driver amplifier was approximately 0.5 mV when a 1 MHz, 30 mV p-p sinusoidal was applied at V_{P1}. An offset of over 5 mV was measured when a 10 MHz, 30 mV p-p sinusoidal was applied.

A proper design for the voltage source that drives V_2 and the DAC output amplifier that drives V_1 is just as important as the design of the driver amplifier. Bandwidth, linearity and drift must be considered. The drift specifications in particular may present a problem since conventional monolithic op amps are to be used. Thermal feedback, which was discussed earlier, is perhaps more important for monolithic devices than with any other type of amplifier construction. The 2.5 k ohm load presented to the source of V_2, and the P_1 load presented to the V_1 source can induce fairly large heating effects in these sources. One solution to this problem was utilized in the Figure II.2 (page 22) design for the driver amplifier and in the Figure III.2 (page 36) design for the V_2 source. In both cases the heat produced in the output stage is isolated from the input stage by the use of two independent op amps within the loop. In the case of conventional ±15 volt monolithic devices, the cost of adding the extra op amp should be very small. The cost will be certainly smaller than that required for the driver amplifier circuit.

CHAPTER IV

SUMMARY

The application for a flexible, low cost design for a high voltage, low drift amplifier to be used in driving a precision electron accelerator has been described. The specifications for the amplifier were presented and several different means for meeting these specifications were discussed. A particular dual op amp design for the driver amplifier was built. Certain test procedures were developed expressly for the evaluation of the performance of the dual op amp design. Results from these test procedures indicate that the dual op amp design has a 25 ppm nonlinearity over the required -10 volt to +40.8 volt dynamic range, an output offset drift of 50 μV/°C, a gain drift of 1.7 ppm/°C, 0.3 mV rms broadband noise at the output, and a positive forward gain of 17 V/V with 170 kHz of bandwidth.

The most beneficial aspect of this thesis to the general researcher is believed to be the design procedure discussions and not the specific form of the final design. The specific application for this thesis represents a very narrow field of interest; however, readers may have found certain techniques or concepts which are useful for other applications in which precise control of high voltage signals is important.

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APPENDIXES

APPENDIX A

RAMP ERROR AS A FUNCTION OF AMPLIFIER BANDWIDTH

The purpose of this appendix is the development of a simple expression that describes the nonlinearity or transmission error of an amplifier for an ideal ramp input due to the amplifier bandwidth limitations. The development offered is in many ways an expansion upon a discussion of ramp waveforms and low pass filters given by Millman and Taub (1965).[14]

First, the time and complex frequency domain expressions for an ideal ramp of duration t_o and unity magnitude at $t = t_o$ (see Figure A.1) must be produced. By superposition the ideal ramp can be constructed from the three simple waveforms shown in Figure A.2. Summing the three time domain waveform expressions from Figure A.2 will produce the time domain expression for the ideal ramp, r(t).

$$r(t) = \frac{t}{t_o} u(t) - \frac{(t - t_o)}{t_o} u(t - t_o) - u(t - t_o) \qquad (A.1)$$

Taking the Laplace transform of r(t) produces the desired complex frequency domain expression for the ideal ramp, R(s).

$$L[r(t)] = R(s) = \frac{1}{t_o s^2} - \frac{1}{t_o s^2} e^{-t_o s} - \frac{1}{s} e^{-t_o s} \qquad (A.2a)$$

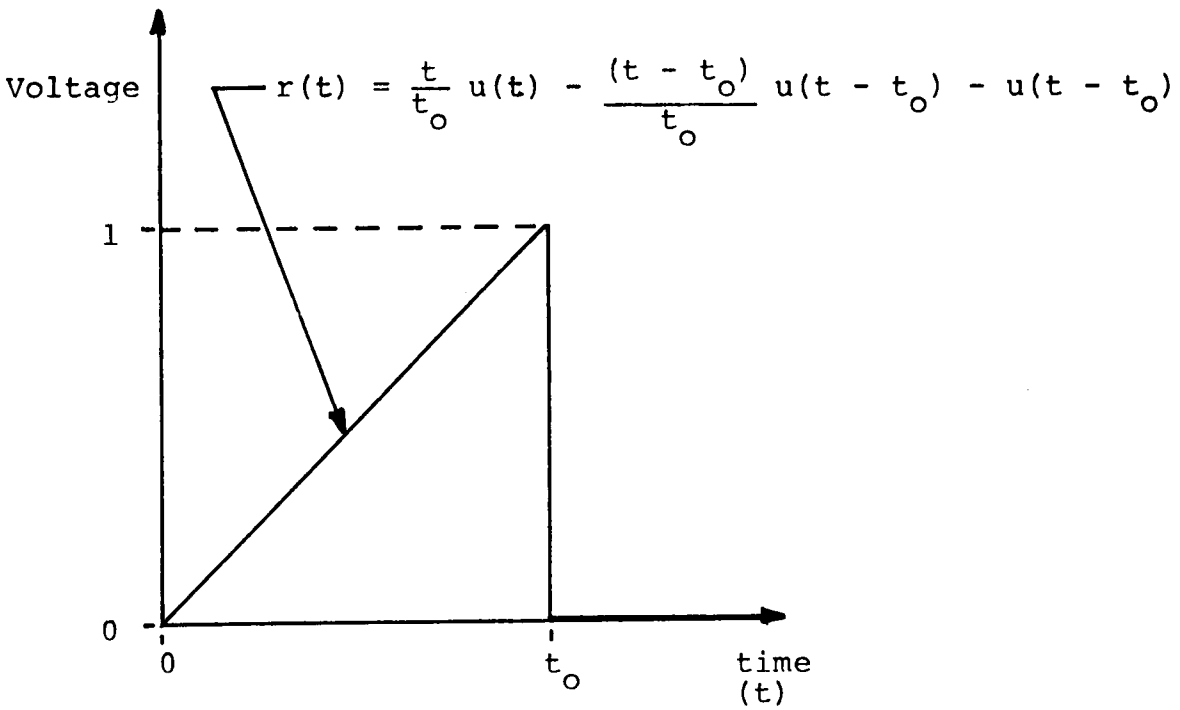


Figure A.1. Ideal Ramp Waveform, **r(t)**.

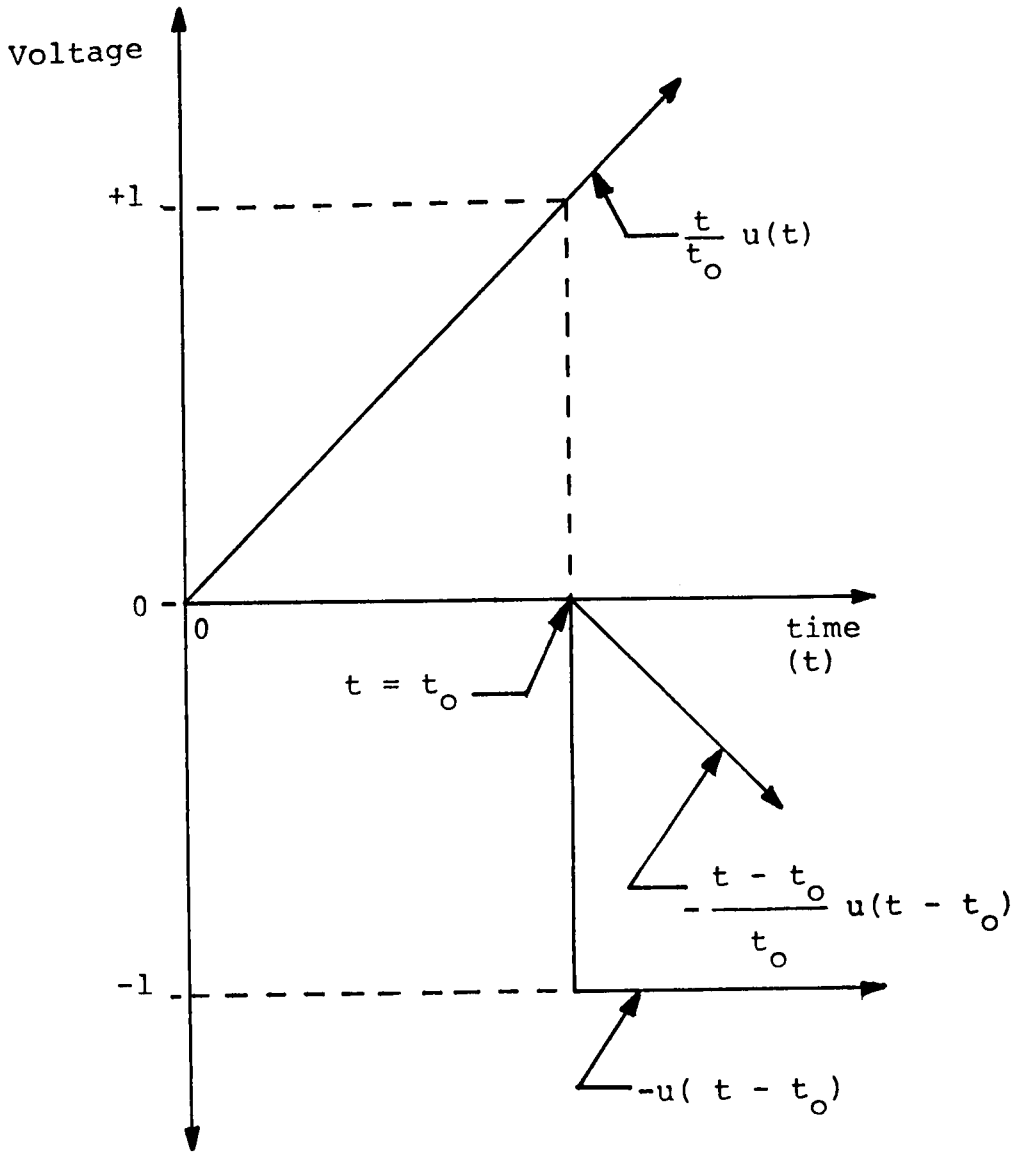


Figure A.2. Ideal Ramp Components.

$$R(s) = \frac{1}{t_o s^2}\left(1 - e^{-t_o s}\right) - \frac{1}{s} e^{-t_o s} \qquad \text{(A.2b)}$$

Second, the transfer function of an ideal amplifier $O(s)/I(s)$ (see Figure A.3) with a gain of A and a single pole at ω_o is required.

$$\frac{O(s)}{I(s)} = \frac{A}{\frac{s}{\omega_o} + 1} \qquad \text{(A.3)}$$

Third, the expression for the amplifier output $O(s)$ that occurs when the ideal ramp is amplified is

$$O(s) = R(s) \cdot \frac{O(s)}{I(s)} = \left[\frac{1}{t_o s^2}\left(1 - e^{-t_o s}\right) - \frac{1}{s} e^{-t_o s}\right] \frac{A}{\frac{s}{\omega_o} + 1} \,. \qquad \text{(A.4a)}$$

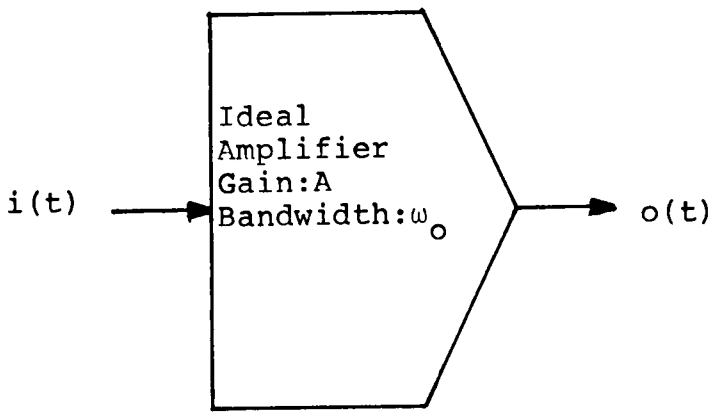
$$O(s) = \frac{A\left(1 - e^{-t_o s}\right)}{t_o s^2\left(\frac{s}{\omega_o} + 1\right)} - \frac{A e^{-t_o s}}{s\left(\frac{s}{\omega_o} + 1\right)} \qquad \text{(A.4b)}$$

By partial fractions,

$$O(s) = \left(\frac{A}{t_o s^2} - \frac{A}{t_o \omega_o s} + \frac{A}{t_o \omega_o^2\left(\frac{s}{\omega_o} + 1\right)}\right)\left(1 - e^{-t_o s}\right)$$

$$+ \left(-\frac{A}{s} + \frac{A}{\omega_o\left(\frac{s}{\omega_o} + 1\right)}\right) e^{-t_o s} \,. \qquad \text{(A.5)}$$

(a) Ideal Single Pole Amplifier.



(b) Transfer Function.

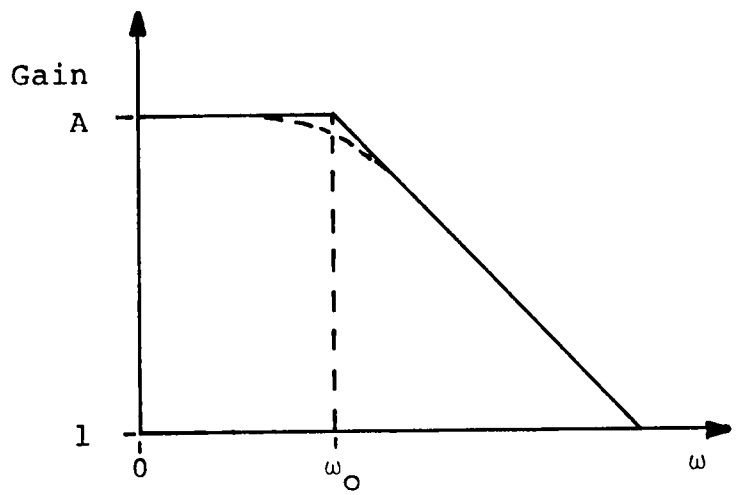


Figure A.3. Ramp Amplifier.

Fourth, the time domain expression for the amplifier output o(t) is produced by taking the inverse Laplace transform of O(s).

$$o(t) = L^{-1}[O(s)] = \left[\frac{A}{t_o}t - \frac{A}{t_o\omega_o}\left(1 - e^{-\omega_o t}\right)\right] u(t)$$

$$+ \left[\frac{A}{t_o}(t - t_o) - \frac{A}{t_o\omega_o}\left(1 - e^{-\omega_o (t - t_o)}\right)\right] u(t - t_o)$$

$$+ \left[-A + Ae^{-\omega_o (t - t_o)}\right] u(t - t_o) \qquad (A.6)$$

A plot of o(t) appears in Figure A.4a.

Fifth, the time domain expression for the ramp error at the output is

$$e(t) = A\, r(t) - o(t) \; . \qquad (A.7)$$

Substituting Equations A.1 and A.6,

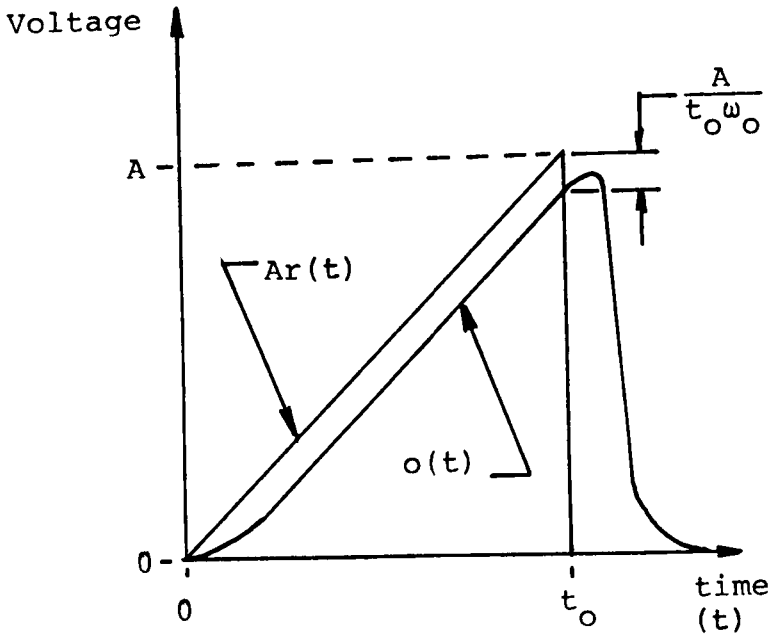
$$e(t) = \left[\frac{t}{t_o} A\, u(t) - \frac{(t - t_o)A}{t_o} u(t - t_o) - Au(t - t_o)\right]$$

$$- \left[\frac{tA}{t_o} - \frac{A}{t_o\omega_o}\left(1 - e^{-\omega_o t}\right)\right] u(t)$$

$$- \left[\frac{(t - t_o)A}{t_o} - \frac{A}{t_o\omega_o}\left(1 - e^{-\omega_o (t - t_o)}\right)\right] u(t - t_o)$$

$$- \left[-A + Ae^{-\omega_o (t - t_o)}\right] u(t - t_o) \; . \qquad (A.8)$$

(a) Plot of o(t) and Ar(t).



(b) Plot of e(t).

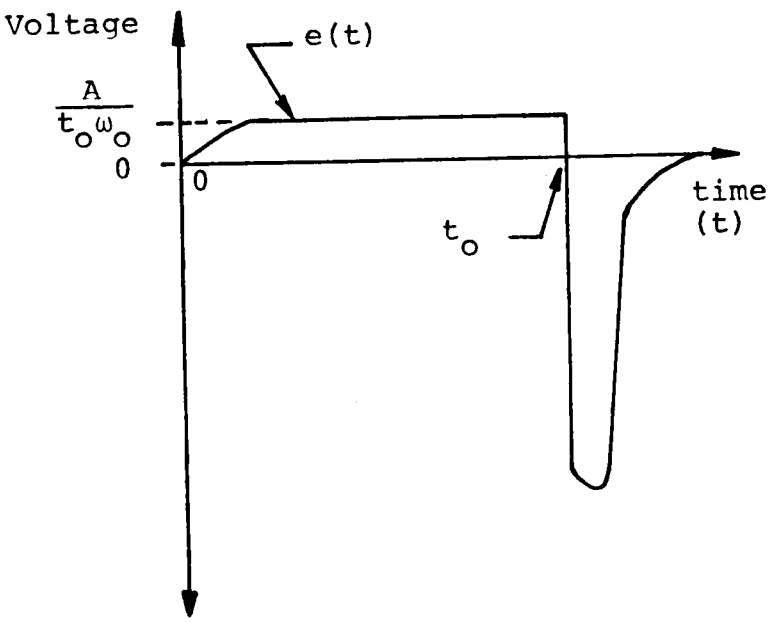


Figure A.4. Voltage Ramp Waveforms.

Simplifying,

$$e(t) = \frac{A}{t_o\omega_o}\left(1 - e^{-\omega_o t}\right)u(t) + \frac{A}{t_o\omega_o}\left(1 - e^{-\omega_o\left(t-t_o\right)}\right)u(t-t_o)$$

$$- Ae^{-\omega_o\left(t - t_o\right)}u\left(t - t_o\right) \quad . \tag{A.9}$$

A plot of e(t) appears in Figure A.4b.

Note that ramp error is of interest only for the duration of the ideal ramp, and e(t) may be reduced for $t < t_o$.

$$e(t) = \frac{A}{t_o\omega_o}\left(1 - e^{-\omega_o t}\right)u(t) \quad , \; t < t_o \tag{A.10}$$

Clearly the maximum error $\left(e_{max}\right)$ occurs at the $t = t_o$ boundary.

$$e_{max} = \frac{A}{t_o\omega_o}\left(1 - e^{-\omega_o t_o}\right) \tag{A.11}$$

A further reduction of e_{max} is possible with the assumption that $t_o\omega_o$ is large.

$$e_{max} = \frac{A}{t_o\omega_o} \tag{A.12}$$

The assumption for Equation A.12 is justified for the application being discussed. Typical worst case values place the product of t_o and ω_o at over 15,000.

The definition for transmission error given by Millman and Taub does not quite apply in this instance since a unity gain between input and output is required. However, if the nonunity gain A is considered; the transmission error definition becomes the difference between the ideal output and the real output divided by the ideal output at $t = t_o$. The transmission error, e_t, in this case is

$$e_t = \frac{A - (A - e_{max})}{A} = \frac{e_{max}}{A} = \frac{1}{t_o \omega_o} \quad . \tag{A.13}$$

Since $\omega_o = 2\pi f_o$, where f_o is the amplifier bandwidth in Hertz,

$$e_t = \frac{1}{2\pi f_o t_o} \quad . \tag{A.14}$$

Note the similarities between this last equation and Equation 2-42 from Millman and Taub. Also note that the transmission error can be considered a form of nonlinearity.

Some examples are in order:

Example #1. Let the ramp magnitude be 40.8 volts and let the ramp duration be 0.05 sec. Also let the required error introduced by the amplifier be less than 0.0025 percent. What would be the minimum allowable amplifier bandwidth?

By Equation A.14, $e_t = \frac{1}{2\pi f_o t_o}$.

$$e_t = \frac{0.0025}{100} \quad , \; t_o = 0.05 \text{ sec.}$$

$$\frac{0.0025}{100} = \frac{1}{2\pi(f_o)(0.05 \text{ sec.})} \quad , \; f_o = \underline{127\text{kHz}} \quad .$$

Example #2. Let the ramp magnitude be 10 volts and let the ramp duration be 0.01 sec. With a bandwidth of 170 kHz, will the ramp error be greater than 1 millivolt?

By Equation A.14, $e_t = \frac{1}{2\pi f_o t_o}$.

$f_o = 170\text{kHz}$, $t_o = 0.01$ sec.

$$e_t = \frac{1}{2\pi(170\text{kHz})(0.01)} = 0.0094\% \quad .$$

The voltage error will be 0.0094 percent of 10 volts or 0.94 mV.

APPENDIX B

STABILITY AND THE TRANSFER FUNCTION OF THE DRIVER AMPLIFIER

The closed loop input-to-output transfer function of the voltage booster stage (see Figure II.2, page 22), M_{BN}, is

$$M_{BN} = \frac{A_B}{1 + A_B F_{BN}} \qquad \text{(see App. C)} \tag{B.1}$$

for,

$$F_{BN} = \left(\frac{R_{BI}}{R_{BI} + R_{BF}}\right) \frac{\left(1 + \frac{jf}{f_1}\right)}{\left(1 + \frac{jf}{f_2}\right)} \quad . \tag{B.2}$$

F_{BN} is the feedback factor for the booster stage, where

$$f_1 = \frac{1}{2\pi R_{BF} C} = 23.4\text{kHz} \tag{B.3}$$

and

$$f_2 = \frac{1}{2\pi\left(R_{BF} \| R_{BI}\right) C} = 123\text{kHz} \quad . \tag{B.4}$$

$$F_{BN} = \left(\frac{16k}{16k+68k}\right) \frac{\left(1 + \frac{jf}{23.4k}\right)}{\left(1 + \frac{jf}{123k}\right)} = 0.19048 \frac{\left(1 + \frac{jf}{23.4k}\right)}{\left(1 + \frac{jf}{123k}\right)} \tag{B.5}$$

and

$$A_B = \frac{150{,}000}{\left(1 + \frac{jf}{7}\right)} \quad . \tag{B.6}$$

A_B is the open loop transfer function of the 1032, where the gain and pole values are estimated from the 1032 data sheet. High frequency poles (above 2MHz) are ignored for simplicity.

$$M_{BN} = \frac{150{,}000}{\left(1 + \frac{jf}{7}\right)\left[1 + \frac{150{,}000}{\left(1+\frac{jf}{7}\right)}\left(\frac{0.19048\left(1 + \frac{jf}{23.4k}\right)}{\left(1 + \frac{jf}{123k}\right)}\right)\right]} \tag{B.7}$$

$$M_{BN} = \frac{150{,}000\left(1 + \frac{jf}{123k}\right)}{(jf)^2\left(\frac{1}{7(123k)}\right) + (jf)\left(\frac{1}{7}+\frac{1}{123k}+\frac{28.571k}{23.4k}\right)+28.571k} \tag{B.8}$$

$$M_{BN} = \frac{150{,}000\left(1 + \frac{jf}{123k}\right)(7)(123k)}{(jf)^2+jf\left(\frac{1}{7}+\frac{1}{123k}+1.221\right)(7)(123k)+(28.571k)(7)(123k)} \tag{B.9}$$

$$M_{BN} = \frac{1.2915 \times 10^{11}\left(1 + \frac{jf}{123k}\right)}{(jf)^2 + jf(1.174289\times10^6) + 2.46 \times 10^{10}} \tag{B.10}$$

Solving for the roots of the quadratic in the denominator of Equation B.10,

$$jf = -\frac{1.1742890\times10^{6}}{2} \pm \frac{\sqrt{(1.1742890\times10^{6})^{2}-(4)(2.46\times10^{10})}}{2} . \quad (B.11)$$

$$jf = -587.1445k \pm \sqrt{\frac{1.2805547\times10^{12}}{2}} \quad (B.12)$$

$$jf = -587.1445k \pm 565.8080k \quad (B.13)$$

$$jf = -21.337k \text{ and } -1.1530M \quad (B.14)$$

Now,

$$M_{BN} = \frac{1.2915\times10^{11}\left(1 + \frac{jf}{123k}\right)}{(jf+21.337k)(jf+1.1530M)} . \quad (B.15)$$

$$M_{BN} = \frac{5.25\left(1 + \frac{jf}{123k}\right)}{\left(1 + \frac{jf}{21.3k}\right)\left(1 + \frac{jf}{1.15M}\right)} \quad (B.16)$$

The high frequency pole at 1.15MHz will also be ignored for simplicity.

$$M_{BN} = \frac{5.25\left(1 + \frac{jf}{123k}\right)}{\left(1 + \frac{jf}{21.3k}\right)} \quad (B.17)$$

Next, the closed loop transfer function for the driver amplifier (noninverting), M_{DN}, is

$$M_{DN} = \frac{A_I M_{BN}}{1 + A_I F_{DN} M_{BN}} \quad , \tag{B.18}$$

where A_I is the open loop transfer function for the input op amp and F_{DN} is the feedback factor for the driver amplifier.

$$A_I = \frac{400k}{\left(1 + \frac{jf}{3}\right)} \quad . \tag{B.19}$$

Gain and pole values are estimated from the OP-07C data sheet. The higher frequency poles (above 2MHz) are again ignored.

$$F_{DN} = \frac{R_I}{R_F + R_I} = \frac{2.5k}{40k + 2.5k} = \frac{1}{17} \tag{B.20}$$

Now,

$$M_{DN} = \frac{\frac{400k}{\left(1+\frac{jf}{3}\right)}}{\frac{\left(1 + \frac{jf}{21.3k}\right)}{5.25\left(1 + \frac{jf}{123k}\right)} + \frac{400k}{\left(1+\frac{jf}{3}\right)}\left(\frac{1}{17}\right)} \quad . \tag{B.21}$$

$$M_{DN} = \frac{400k\left(1 + \frac{jf}{123k}\right)(5.25)}{\left(1 + \frac{jf}{21.3k}\right)\left(1+\frac{jf}{3}\right)+(400k)\left(\frac{1}{17}\right)(5.25)\left(1 + \frac{jf}{123k}\right)} \tag{B.22}$$

$$M_{DN} = \frac{2.10M\left(1+\frac{jf}{123k}\right)}{(jf)^2\left(\frac{1}{63.9k}\right)+jf\left(\frac{1}{3}+\frac{1}{21.3k}+\frac{123.52941k}{123k}\right)+123.5304k} \qquad (B.23)$$

$$M_{DN} = \frac{1.34190\times10^{11}\left(1+\frac{jf}{123k}\right)}{(jf)^2 + jf(85.478k) + (7.89359\times10^{9})} \qquad (B.24)$$

Solving for the roots of the denominator of Equation B.24,

$$jf = -\frac{85.478k}{2} \pm \frac{\sqrt{(85.478k)^2 - 4(7.89359\times10^{9})}}{2} . \qquad (B.25)$$

$$jf = -42.7390k \pm \frac{\sqrt{-2.4267878\times10^{10}}}{2} \qquad (B.26)$$

$$jf = -42.7390k \pm j77.8908k \qquad (B.27)$$

Now,

$$M_{DN} = \frac{1.34190\times10^{11}\left(1+\frac{jf}{123k}\right)}{(jf+42.7390k+j77.8908k)(jf+42.7390k-j77.8908k)} . \qquad (B.28)$$

$$M_{DN} = \frac{17\left(1+\frac{jf}{123k}\right)}{\left(1+\frac{jf}{42.7k+j77.9k}\right)\left(1+\frac{jf}{42.7k-j77.9k}\right)} \qquad (B.29)$$

Equation B.29 represents the frequency domain transfer function of the driver amplifier for V_3/V_{P1}. (See Figure II.2, page 22.) A plot of $|M_{DN}|$ in logarithmic gain (db) versus frequency is shown in Figure B.1.

The driver amplifier stability is determined from an analysis of the loop transmission of the amplifier, $A_I F_{DN} M_{BN}$. Figure B.1 shows a Bode plot of the loop transmission. A graphical determination (aided and verified by a calculator) reveals a phase margin of 51 degrees for the loop transmisson. Stability of the driver amplifier is implied.

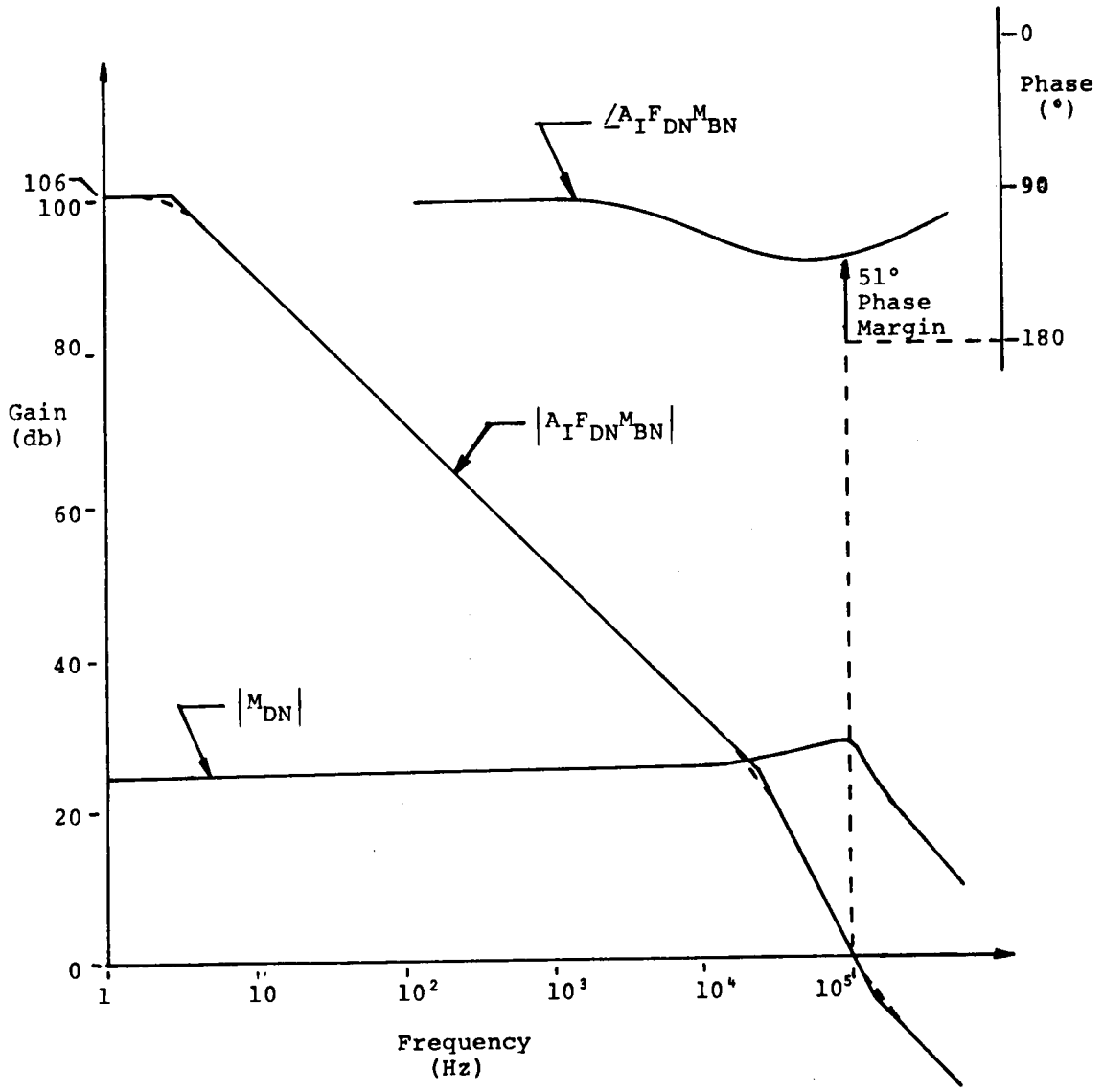


Figure B.1. The Driver Amplifier Bode Plots.

APPENDIX C

OUTPUT OFFSET DRIFT

Drawing from Equations 10.5a and 10.5b along with Equations 10.7a and 10.7b from Barna (1971),[15] an expression for the output offset drift with temperature can be produced for the circuit in Figure II.2 (page 22) of the text.

$$V_{3D} = M_{DC} \frac{R_F R_I}{R_F + R_I} \left(I_{BD} - I_{OFFD} \right) + M_{DC} V_{OFFD} \,, \qquad (C.1)$$

where V_{3D} is the drift with temperature at the driver amplifier output. M_{DC} is the positive forward gain. R_F and R_I are the feedback resistor values. I_{BD} and I_{OFFD} are the input bias current drift and the input offset current drift. V_{OFFD} is the input offset voltage drift.

The equations cited from Barna are not specifically developed for drift with temperature but for the actual magnitude of the offset. In addition, Equation 10.5a in Barna refers to resistors R_S and R_P. For this application, R_S is very close to zero, and R_P is large. Also the open loop gain of the op amp, A_{DC}, is not considered because of the minimal effect that A_{DC} will have upon M_{DC} and the resulting output offset drift calculation.

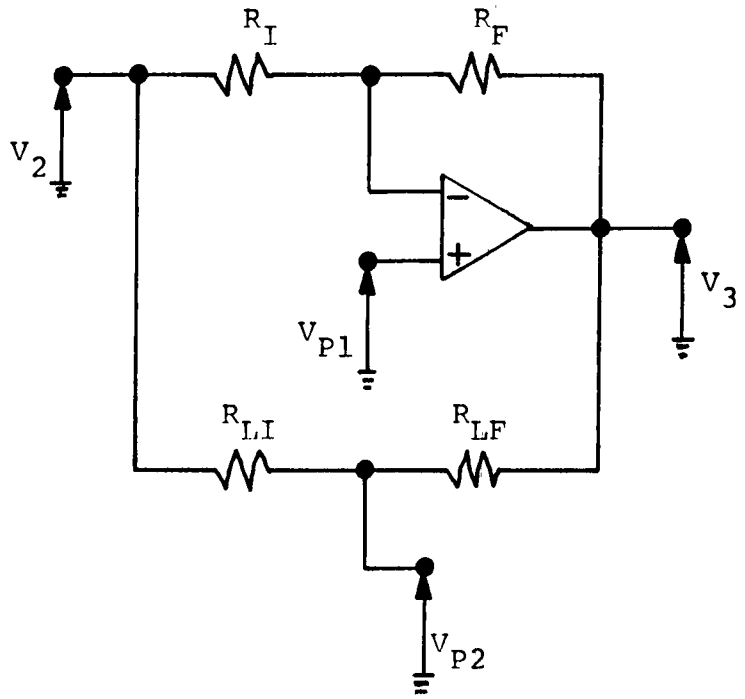


Figure D.1. Simplified Linearity Test Schematic.

and

$$\frac{R_F}{R_I+R_F} = \frac{R_{LF}}{R_{LI}+R_{LF}} \quad . \tag{D.5}$$

By D.4 and D.5, Equation D.2 becomes

$$V_{P2} = \frac{R_I}{R_I+R_F} V_3 + \frac{R_F}{R_I+R_F} V_2 \quad . \tag{D.6}$$

Substituting for V_3 from Equation D.1, Equation D.6 becomes

$$V_{P2} = \frac{R_I}{R_F+R_I}\left(-\frac{R_F}{R_I}V_2+\frac{R_F+R_I}{R_I}V_{P1}+\frac{R_F+R_I}{R_I}V_{OFF}\right) + \frac{R_F}{R_I+R_F}V_2 \quad . \tag{D.7}$$

Simplifying,

$$V_{P2} = -\frac{R_F}{R_F+R_I}V_2 + V_{P1} + V_{OFF} + \frac{R_F}{R_F+R_I}V_2 \quad . \tag{D.8}$$

$$V_{P2} = V_{P1} + V_{OFF} \tag{D.9}$$

VITA

William F. Jones was born in Knoxville, Tennessee on November 29, 1952. He was reared on a farm in the nearby Hardin Valley community while attending elementary and high schools in Knox County. In 1970, he obtained his high school diploma from the Webb School of Knoxville, where he also received that school's Bausch and Lomb Science Award.

Undergraduate work at the University of Tennessee in Knoxville (UTK) began for him as a part time student in the summer of 1969 while he was still a high school junior. Full time undergraduate work began in the fall of 1970 when he enrolled in the college of electrical engineering at UTK. In January of 1972 the author joined the cooperative engineering program and worked six quarters for Western Electric in Winston-Salem, North Carolina. While an undergraduate Mr. Jones joined the Phi Eta Sigma, Phi Kappa Phi, and Eta Kappa Nu academic fraternities. A Bachelor of Science degree with high honors in electrical engineering was awarded in June of 1975.

During the last quarter of his senior year at UTK, Mr. Jones entered the graduate program at UTK. While attending graduate school, he enjoyed full time employment with Special Instruments Laboratory, Inc., also in Knoxville, where he served as a project engineer in instrument design.