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A Programmable Frequency Divider Having a Wide Division Ratio Range, and Close-to-50% Output Duty-Cycle

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Presented for the
Doctor of Philosophy Degree

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Abstract

In Radio Frequency (RF) integrated circuit design field, programmable dividers are getting more and more attentions in recent years. A programmable frequency divider can divide an input frequency by programmable ratios [1]. It is a key component of a frequency synthesizer. It also can be used to generate variable clock-signals for: switched-capacitor filters (SCFs), digital systems with different power-states, as well as multiple clock-signals on the same system-on-a-chip (SOC). These circuits need high performance programmable frequency dividers, operating at high frequencies and having wide division ratio ranges, with binary division ratio controls and 50% output duty-cycle.

Different types of programmable frequency dividers are reviewed and compared. A programmable frequency divider with a wide division ratio range of (8 ~ 524287) has been reported [2]. Because the output duty-cycle of this reported divider is far from 50%, the circuit in [2] has very limited applications. The proposed design solves this problem, without compromising other advantages of the design in [2]. The proposed design is fabricated in a 0.18-μm RF CMOS process. Test results show that the output duty-cycle is 50% when the division ratio is an even number. The duty-cycle is 44.4% when the division ratio is 9. The output duty-cycle becomes closer to 50% when the division ratio is an increasing odd number. For each division ratio, the output duty-cycle remains constant, with different input frequencies from GHz down to kHz ranges, with different

temperatures and power supply voltages. This thesis provides an explanation of the design details and test results.

A Phase Locked-Loop (PLL) based frequency synthesizer can generate different output frequencies. A programmable frequency divider is an important component of this type of PLL. Since bandwidth is expensive, it is preferred to reduce the frequency channel distance of a frequency synthesizer. Using a fractional programmable divider, the frequency channel distance of a PLL can be reduced, without reducing the reference frequency or increasing the settling time of the PLL. A frequency synthesizer with a programmable fractional divider is designed and fabricated. A brief description of the PLL design and test results are presented in this dissertation.

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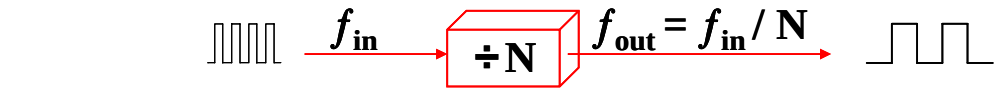
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Chapter 1
Introduction

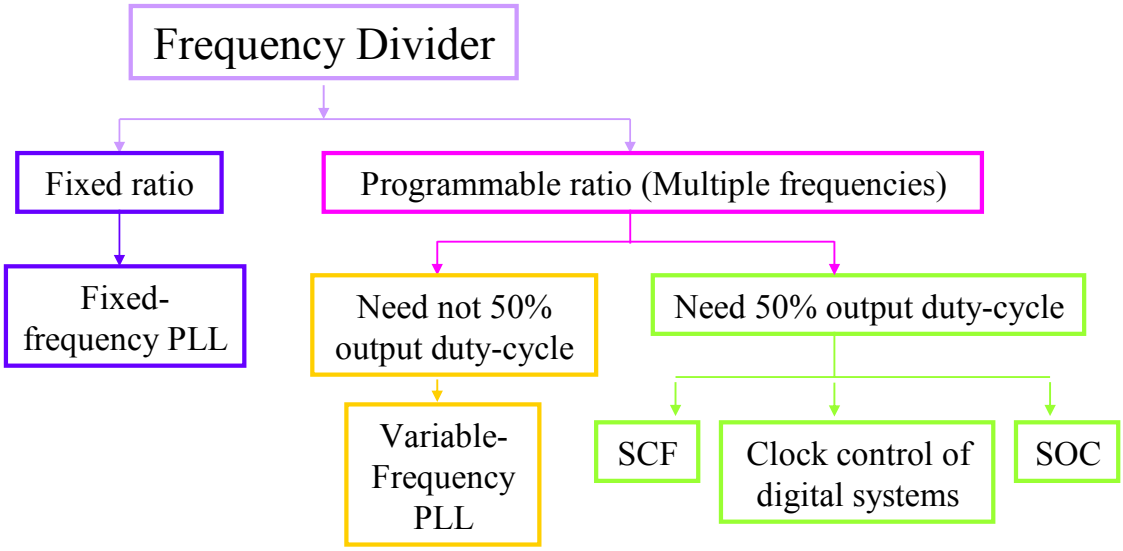
A frequency divider can divide the input frequency f_{in} to a lower frequency $f_{out} = f_{in} / N$ as shown in Figure 1 (a). There are frequency dividers with a single fixed division ratio and programmable division ratios as shown in Figure 1 (b). A fixed ratio divider can be used in a PLL with a fixed output frequency. The division ratio N of a programmable frequency divider can be varied. By changing the division ratio, a programmable frequency divider could generate different output frequencies.

Programmable frequency dividers are getting more and more attention in recent years. A programmable frequency divider is an important component of a frequency synthesizer, or a PLL with variable output frequencies. When used in a frequency synthesizer, normally the output duty-cycle of the programmable frequency divider need not be close to 50%. The reason is that the Phase/Frequency Detector (PFD) in a PLL is mostly single-edge triggered.

Also, a programmable frequency divider can be used to generate variable clock-signals to drive various types of clocked circuits. When used to drive clocked circuits, the output duty-cycle of a programmable frequency divider should be close to 50% for better performance. Clocked circuits include switched-capacitor filters (SCFs), digital systems



(a)



(b)

Figure 1: Fundamentals of frequency dividers: (a) function of a frequency divider, and (b) classification of frequency dividers

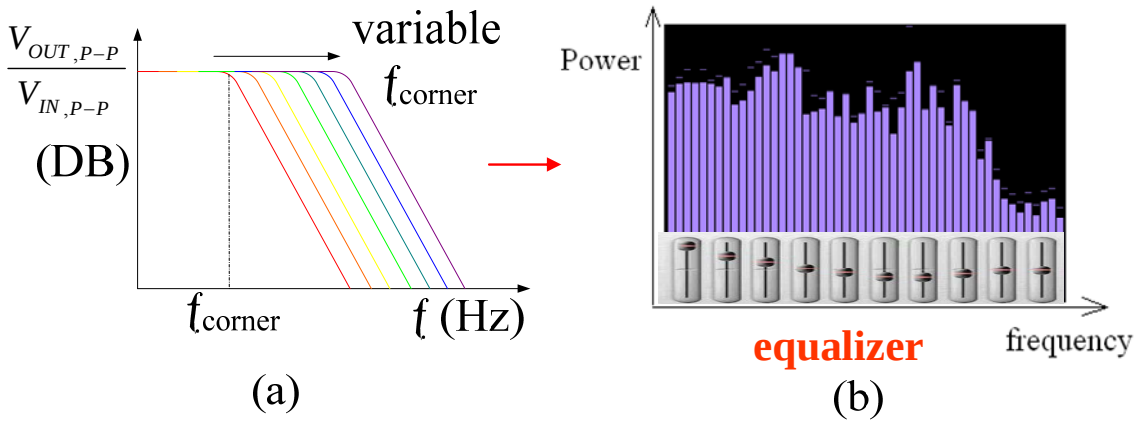


Figure 2: An application of switched-capacitor filters (SCFs): (a) the corner frequency of a SCF could be adjusted by changing the clock frequency, and (b) SCFs could be used in equalizers for audio systems.

with different power-states, as well as multiple clock-signals on the same system-on-a-chip (SOC), and so on.

Figure 2 shows an application of SCFs. Figure 2 (a) shows the transfer function of a low-pass SCF. The corner frequency of the SCF could be varied by changing the clock frequency, which is used to drive the SCF. Also, there are SCFs used as band-pass filters, high-pass filters, and notch (band-reject) filters. The corner frequencies of these SCFs could also be adjusted by changing the clock frequencies. SCFs can be used in audio systems, such as equalizers shown in Figure 2 (b). Equalizers can adjust the output power at different frequency bands. SCFs need clock signals (up to several hundred MHz) with variable frequencies to adjust the corner frequencies. The variable clock signals can be generated using a programmable frequency-divider. The duty-cycle of the clock signal should be as close to 50% as possible for proper operation of the SCFs.

Figure 3 shows an example of the clock and power control of digital systems. Digital systems can use different power states to save power. When the intensity of tasks is lower, low power states could be used. Different power states can use different operating frequencies generated from a programmable frequency divider to adjust the power consumption. Lower operating frequencies can reduce the power consumption. A 50% duty-cycle is important to give equal settling time to circuits when the clock signal is high or low.

Figure 4 shows that the system-on-a-chip (SOC) needs multiple clock signals in a wide frequency range. A PLL followed by several programmable frequency dividers can generate different variable clock signals in a wide frequency range in a SOC. All the digital circuits will have better performance when the duty-cycle of the clock signals is closer to 50%.

These circuits need high performance programmable frequency dividers, operating at high frequencies and having wide division ratio ranges, binary division ratio controls and 50% output duty-cycle. However, before this research work, none of the reported dividers meet all the desirable characteristics. The proposed design is aimed to generate a programmable frequency divider with all the above features.

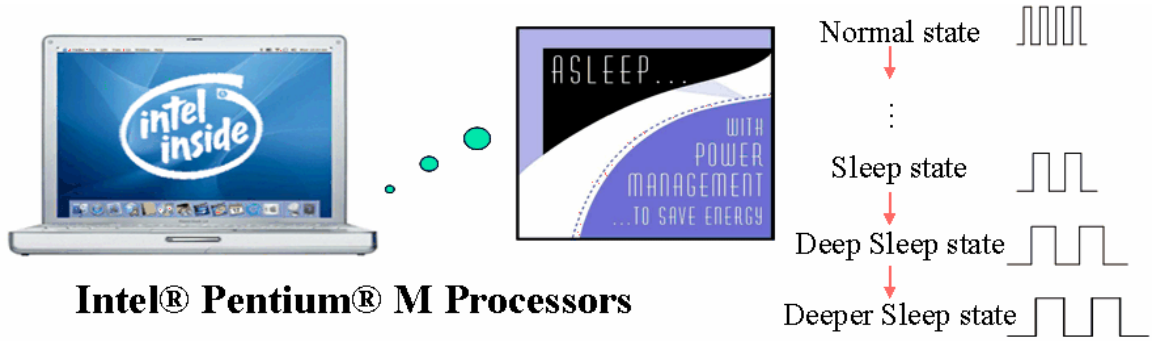
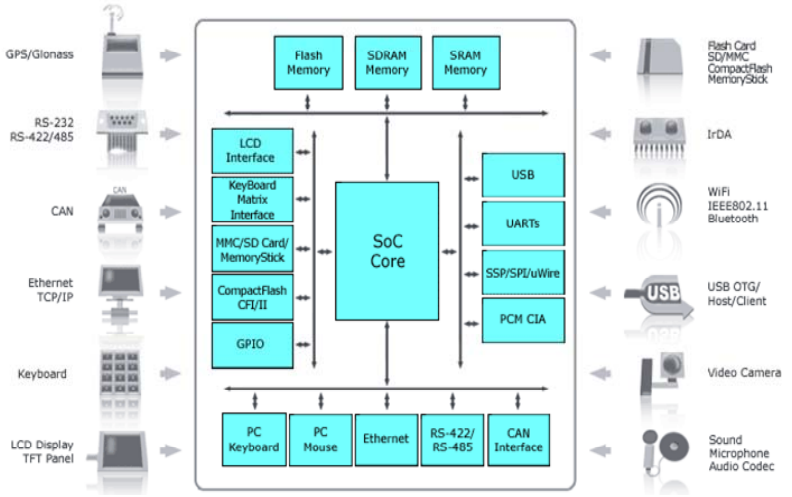


Figure 3: Clock and power control of digital systems.



LCD	**< 1k Hz**
Audio	**20 Hz --- 20 k Hz**
ADC/DAC	**Tens of k Hz --- hundreds of MHz**
Wired network interface (RS-232 / RS485)	**Tens of k Hz --- hundreds of MHz**
USB	**12 MHz, 480MHz**
Memories	**Tens of MHz --- hundreds of MHz**
GPS	**1.1 GHz --- 1.8 GHz**

Figure 4: System-on-a-chip (SOC) needs multiple clock signals in a wide frequency range [3].

Chapter 2
Problem Statements

Various types of circuits need a high performance programmable frequency-divider. Previous designs have some of the following limitations:

- The output duty-cycle is far from 50%,
- Poor capability to drive clocked circuits,
- Requirements of complicated control circuits,
- Operating frequency range is limited,
- Division ratio range is limited.

The proposed work is aimed to create a divider without the above limitations.

2.1 Previous Programmable Divider Designs (Prior Art)

Table 1 lists almost all the high frequency CMOS programmable frequency-dividers that have a wide division ratio range (n_{max} / n_{min} is > 2, where n_{max} is the maximum division ratio, and n_{min} is the minimum division ratio), that have been reported. A few papers that repeated the same type dividers are not listed for simplicity. If n_{max} / n_{min} is ≤ 2, the output frequency range is quite limited. For example, if the highest output frequency is 100 MHz, the lowest output frequency will not be lower than 50 MHz. While if the division ratio range is $2^{min} \sim 2^{max+1} - 1$, and if the highest output frequency is 100 MHz, the lowest output frequency can be in the range of MHz, kHz or even lower. A programmable

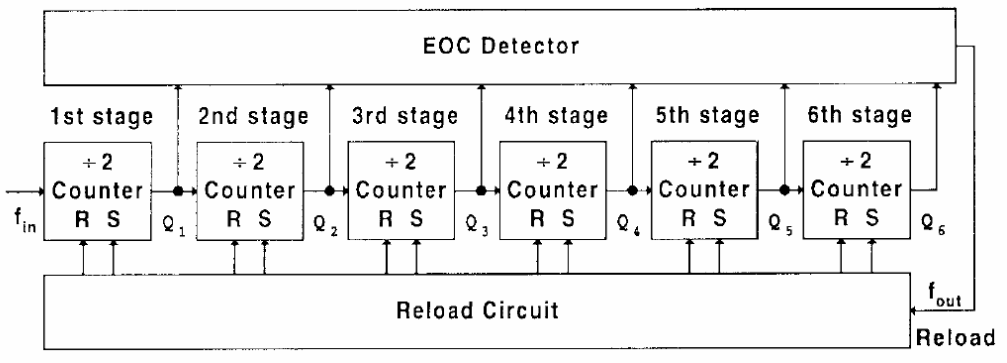
Table 1: Literature review of the published programmable frequency dividers.

	Authors	Publish Year	Division ratio range	Process (μm)	Wide division ratio range	Wide f_{in} range	High operating-frequency	Binary control	Close to 50% output duty-cycle
	Proposed design		2^{min}---2^{max+1} – 1	CMOS 0.18μm	√	√	√	√	√
[2]	C.S.Vaucher *et al.*	2000	2^{min}---2^{max+1} – 1 (8-262143)	CMOS 0.35μm	√	√	√	√	
[4]	X.P. Yu *et al.*	2005	N×P+S	CMOS 0.18μm	√	√	√		√
[5]	S. Khadanga *et al.*	2003	P×R+S (9--65024)	CMOS 0.18μm	√	√			
[6]	D. Guermandi *et al.*	2002	2(P1×4+P2×5) (98-4608)	CMOS 0.35μm	√	√	√		
[7]	T. Ohgishi *et al.*	1978	P×R+S	4μm	√	√			
[8]	Lee Sang-Hoon *et al.*	2002	2 -- 2^M - 1	CMOS 0.6μm	√	√		√	
[9]	Chang Hun-Hsien *et al.*	1998	2 -- 2^M - 1	CMOS 0.8μm	√	√		√	

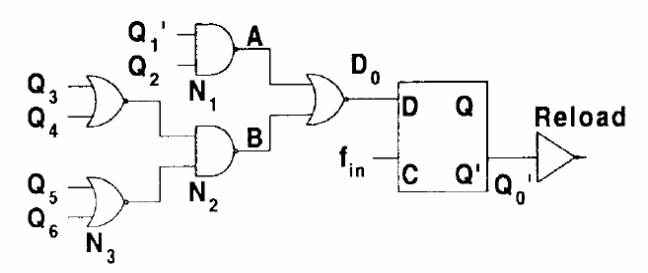
frequency-divider with a wide output frequency range can have much more applications. For example, it can offer clock signals for several digital circuits which need different clock frequencies on the same chip and for switched capacitor circuits which need clock signals with a wide adjustable frequency range.

It can be seen that there are only 3 types of high-frequency CMOS programmable frequency-dividers with a wide division ratio range. The first type is a counter, as shown in references [8] and [9]. A counter has a wide division ratio range from 2 to 2^M-1, where M is the number of "divide-by-2 Counter" stages. The top-level schematic is shown in Figure 5. The operating frequency for this type divider is limited by the accumulated delay time of all the M counter stages. This can be seen from Figure 5 (b), since the logic combination of "$Q_1 \ldots Q_6$", the output signals from all the counter stages, determines the "Reload" signal. The "Reload" signal resets all the counter stages at the same time to start a new counting cycle. Because of the accumulated delay time, it is difficult for the operating frequency of a counter to reach a high value.

The second type programmable-divider is the "P×R+S" divider, as shown in Figure 6. Its operating-speed is comparable with the circuit created by C. S. Vaucher *et al.* [2]. The division ratio control, P×R+S, is not directly in a binary format. In order to be implemented in the actual digital circuits, this second type divider needs extra encoder to transfer the binary control-signals to the P×R+S format. (Reference [2] already has binary control as shown in equation (1)). Binary numbers can be easily implemented in the



(a)



(b)

Figure 5: Schematics of a previously reported programmable counter [9]: (a) the top-level block diagram, and (b) the end-of-count (EOC) detector.

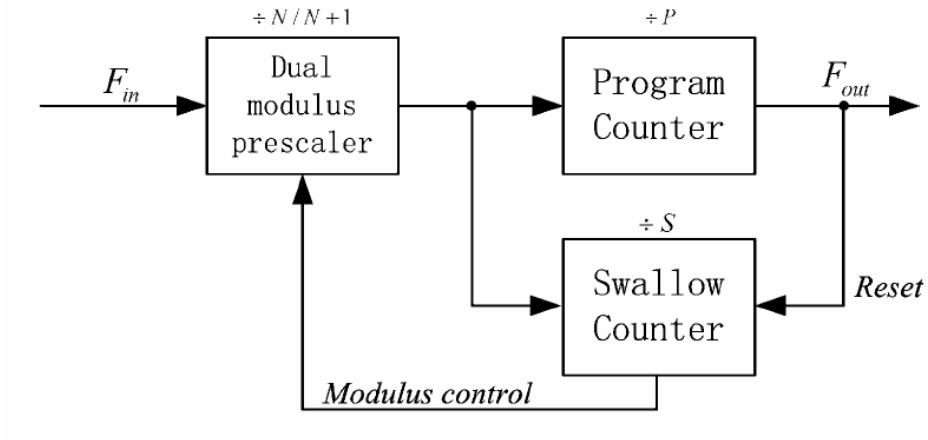


Figure 6: The block diagram of a previously reported programmable divider with division ratios N×P+S [4].

actual circuits, since "LOW" and "HIGH" are used to represent "0" and "1" in digital circuits. C. S. Vaucher *et al.* [2] reported a programmable frequency-divider with a very wide division ratio range, ($2^{min} \sim 2^{max+1}$ -1). The number "min" and "max" can be controlled independently. The schematics of the design [2] are shown in Figure 7. The design is comprised of cascade stages of "2/3 cell". "2/3 cell" is a divider with division ratios of 2 or 3.

The design [2] has several advantages: (1) a wide division ratio range for the circuit in Figure 7 (b), (2) high operating-frequencies, since its operating-frequency is not limited by the delay of all the stages, (3) easy to redesign with different number of stages, since each stage has the similar structure, and (4) the division ratio controls are in a binary format as shown in the following equation. According to [2], the division ratio for the circuit shown in Figure 7 (a) is,

$$division\ \ ratio = P_0 \cdot 2^0 + P_1 \cdot 2^1 + P_2 \cdot 2^2 + \cdots + P_{n-1} \cdot 2^{n-1} + 2^n \qquad (1)$$

where P_0, P_1, …, P_{n-1} are the control bits of the division ratio. Their logic levels are '0' or '1'.

Compared with the other published programmable dividers, the divider [2] has more attractive characteristics. It still has a shortcoming that its output duty-cycle is far from 50%. It is difficult to use the design [2] for various applications, which need a close-to-50% clock duty-cycle. The simulation in Figure 8 demonstrates this problem. In the simulation shown in Figure 8, f_{in} = 5 GHz, and the signal "mod_1" is used as the output

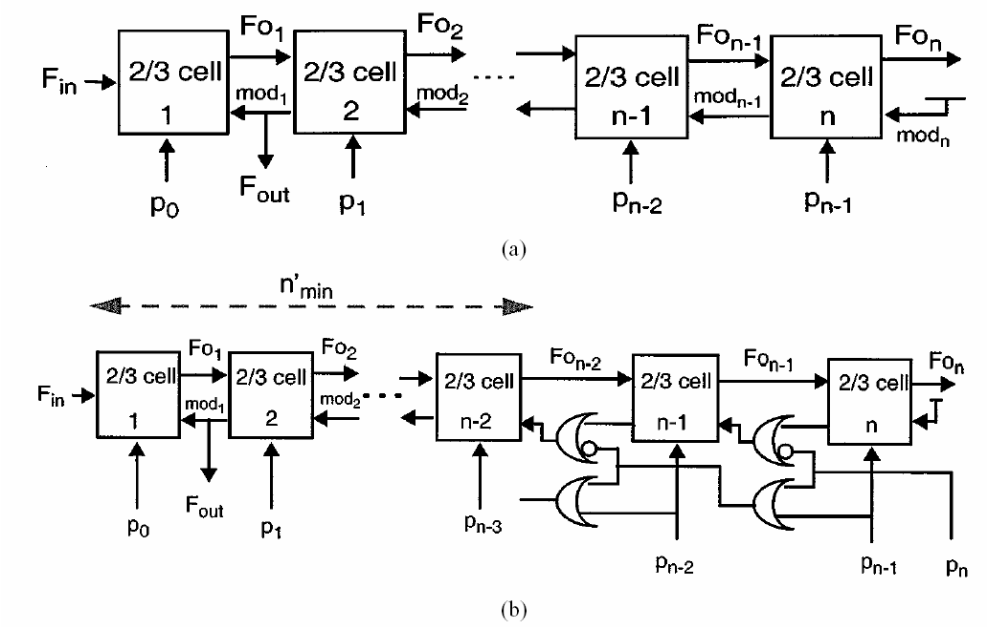


Figure 7: A published programmable frequency divider [2]: (a) the block diagram of the basic architecture ($2^n \le N \le 2^{n+1}-1$), where N is the division ratio, and (b) the circuit diagram with extended division range ($2^{min} \le N \le 2^{max+1}-1$), (in this figure max = n, min = n–2).

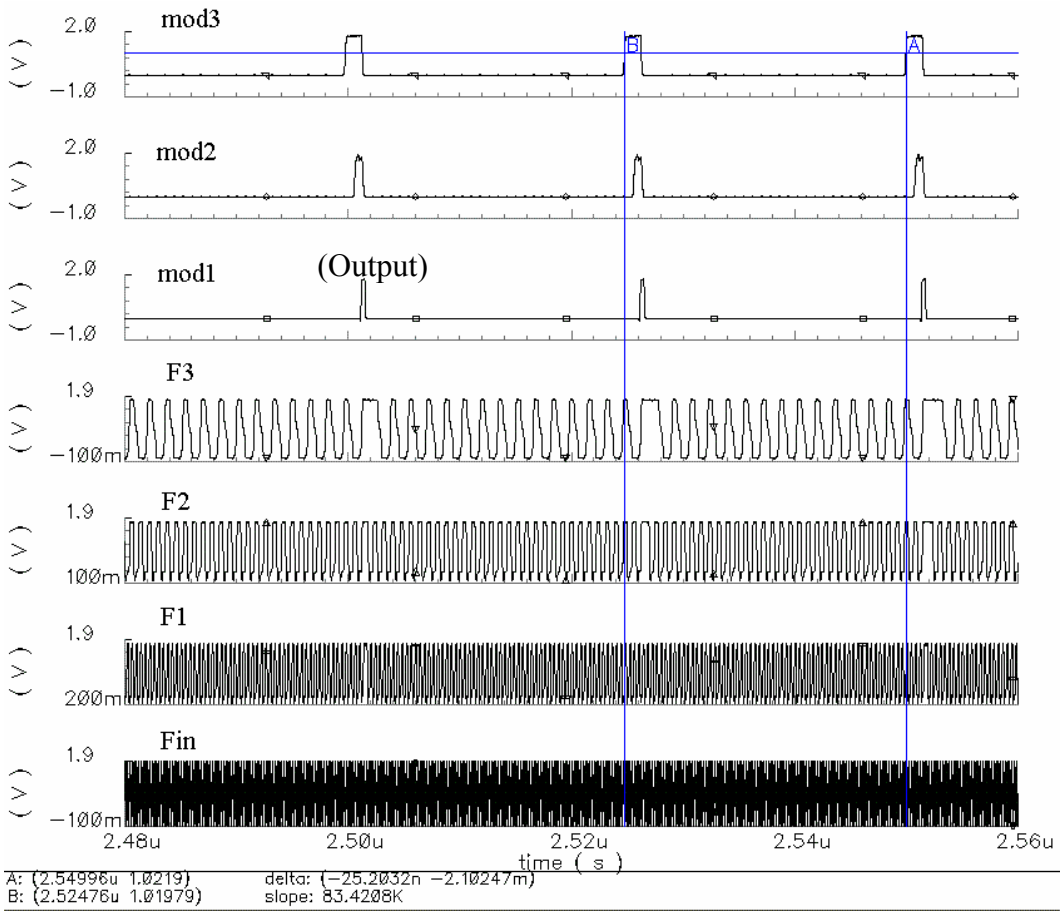


Figure 8: The duty-cycle problem with the published design [2]. The signal "mod_1" is used as the output signal of the divider. In this simulation, f_{in} = 5 GHz.

signal of the divider. The pulse width of "mod_1" is in the nanosecond range. It is difficult to drive load capacitors by using this signal. Even inside a chip, parasitic capacitances also exist, which can become load capacitors.

The capacitors connected to "mod_1" terminal may not be able to be charged to the expected voltage during the narrow pulses. The goal of the proposed design is to solve this problem, while maintaining other advantages of the existing circuit [2].

2.2 Problem Definition

C. S. Vaucher *et al.* designed a programmable frequency divider with high operating frequency and with a wide range of division ratios ($2^{min} \sim 2^{max+1}$-1) [2]. The designer can specify the minimum power value "min" and the maximum power value "max". Thus the output frequency can be changed widely, such as 100MHz to 1MHz, and to 1kHz. The circuit in [2] also can use binary controls to set the division ratios as shown in (1).

Vacucher's divider [2] has a disadvantage that its output pulse width is only 2 or 3 times of the input period. If the input frequency is 2 GHz, the output pulse width is only 1 *n*s or 1.5 *n*s, as shown in Figure 9. The output pulse width does not change if the output frequency is lower. It is difficult to drive large clocked systems by using these narrow pulses, since the divider may not be able to charge the load capacitors to the correct logic level of the clock signal. For example, if the capacitor load is 10 *p*F, and the supply voltage is 2 V, in order to charge the capacitor from 0 V to 2 V in 1 *n*s, the driving

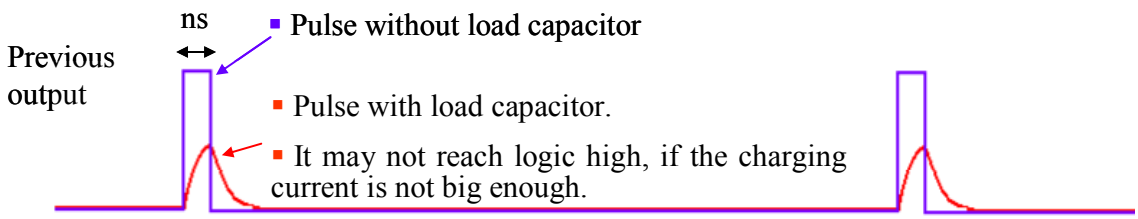


Figure 9: Vaucher's design [2] has low capability to drive other circuits.

current should be,

$$2\,V \times 10\ pF\ /\ 1\,ns = 20\,mA \tag{2}$$

If the driving current is not large enough, the clocked circuits will not read the logic "1" part of the clock signal. If the duty-cycle is close to 50%, with the same output frequency, the output pulse width will be much longer. Having the same current at the output stage, the driving capability of the divider will be greatly increased.

From another point of view, a clock signal with close to 50% duty-cycle can also increase the maximum operating-frequency of clocked circuits. For example, in a master-slave D-Flip-Flop (DFF) as shown in Figure 10, when the "CLK" signal is low, the master circuit is operating; but when "CLK" is high, the slave circuit is operating. As shown in Figure 11 (d), signals in digital circuits require time $t_{required}$ to charge the load capacitors to the desired logic level, and to settle down from the oscillation. A master-slave DFF should have equal settling time when the "clock" signal is high or low. To operate at high frequencies, the duty-cycle of the clock signal should be 50% to give enough time to both the master and the slave circuits to settle down.

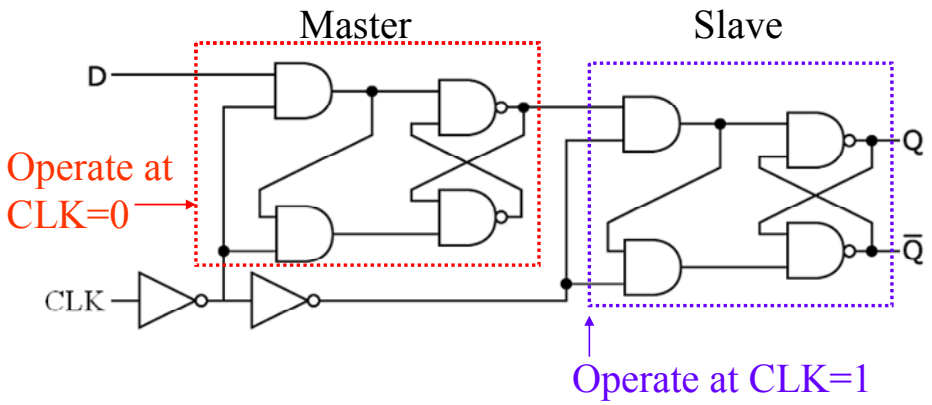


Figure 10: A standard master-slave D-Flip-Flop.

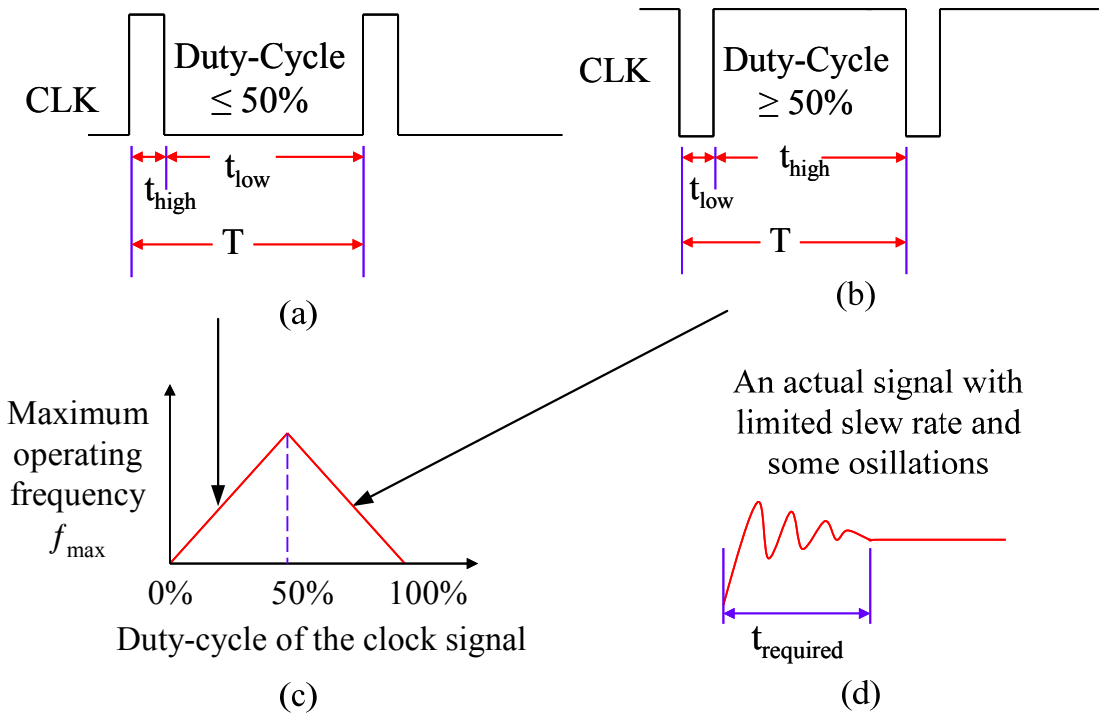


Figure 11: The maximum operating frequency of a master-slave DFF vs. duty-cycle of the clock signal.

The following derivations give a more accurate relationship between the maximum operating frequency of a master-slave DFF and the duty-cycle of the clock signal. The definition of duty-cycle for a periodic signal is,

$$\text{duty - cycle} = \frac{t_{high}}{T} \tag{3}$$

where T is the period, and t_{high} is the time when the signal is logic high. As shown in Figure 11 (a),

$$t_{short} = \text{minimum}\,(\,t_{high}\,,\,t_{low}\,) \tag{4}$$

If duty-cycle $\leq 50\%$, $t_{short} = t_{high}$. From equation (3), the duty-cycle should be,

$$\text{duty} - \text{cycle} = \frac{t_{short}}{T} \tag{5}$$

The following result could be obtained.

$$T = \frac{t_{short}}{\text{duty} - \text{cycle}} \tag{6}$$

If assume $t_{required}$ is the time needed to charge the load capacitors, and to settle the oscillations, the relationship $t_{short} \geq t_{required}$ should exist. Thus,

$$T = \frac{t_{short}}{\text{duty} - \text{cycle}} \geq \frac{t_{required}}{\text{duty} - \text{cycle}} \tag{7}$$

$$f = \frac{1}{T} \leq \frac{\text{duty} - \text{cycle}}{t_{required}} \tag{8}$$

The maximum operating frequency, f_{max}, will be equal to,

$$f_{max} = \frac{\text{duty} - \text{cycle}}{t_{required}} \propto \text{duty} - \text{cycle} \tag{9}$$

The left part of Figure 11 (c) shows the relationship in equation (9).

As shown in Figure 11 (b), if duty-cycle $\geq 50\%$, $t_{short} = t_{low}$. Thus,

$$\text{duty - cycle} = \frac{t_{high}}{T} = \frac{T - t_{low}}{T} = \frac{T - t_{short}}{T} = 1 - \frac{t_{short}}{T} \tag{10}$$

By switching "duty - cycle" and "$\frac{t_{short}}{T}$" in the above equation, the following result can be obtained.

$$1 - \text{"}duty - cycle\text{"} = \frac{t_{short}}{T} \tag{11}$$

$$\text{Thus } T = \frac{t_{short}}{1 - \text{"duty - cycle"}} \geq \frac{t_{required}}{1 - \text{"duty - cycle"}} \tag{12}$$

$$\text{and } f = \frac{1}{T} \leq \frac{1 - \text{"duty - cycle"}}{t_{required}} \tag{13}$$

The maximum operating frequency, f_{max}, will be equal to,

$$f_{max} = \frac{1 - \text{"duty - cycle"}}{t_{required}} \tag{14}$$

The right part of Figure 11 (c) shows the relationship in equation (14).

Figure 11 (c) shows that when the duty-cycle of the clock signal is 50%, the Master-slave DFF can achieve the highest operating frequency. Similarly, clock signals with 50% duty-cycle will also optimize the maximum operating frequency of other clocked circuits.

The output duty-cycle of Vaucher's divider [2] is far from 50%, which can be expressed as,

$$\text{Duty cycle of previous design} = \begin{cases} \frac{2}{n}, \text{ when n is an even number} \\ \frac{3}{n}, \text{ when n is an odd number} \end{cases} \quad (15)$$

where n is the division ratio.

The output duty-cycle of [2] is < 10%, when n is > 20 and n is an even number. For larger values of n, the duty-cycle becomes smaller. For example, if n = 10000, duty-cycle = 0.02%. The small output duty-cycles will degrade the performance of clocked circuits, or digital systems. A thorough review of relevant literatures indicates that no duty-cycle corrector has been reported for the input duty-cycles less than 2% [10] - [17]. The reported duty-cycle correctors could not resolve the duty-cycle problem in [2] when its output duty-cycle is less than 2%.

The proposed design solved the problem of Vaucher's design [2], without degrading its other advantages. The output duty-cycle of the proposed design is very close to 50% (within 44.4% ~ 50%). For each division ratio, the output duty-cycle remains constant, with different input frequencies from GHz down to kHz range, at different temperatures and with different power supply voltages. Test results corroborate the efficacy of the proposed design.

2.3 Original Contributions

The achievement of the dissertation includes:

- The output signal of the proposed work has close to 50% duty-cycle (the duty-cycle error is ≤ 5.6%)
- The step-size of the division ratios is kept to be 1.
- The output duty-cycle remains constant with PVT (Process-Voltage-Temperature) changes and input frequency variations (GHz - kHz).
- A smaller layout area, because of the elimination of large resistors.
- Derivation of the expression for the programmable division ratio.

2.3.1 Close to 50% Output Duty-Cycle

The circuit in [2] has a disadvantage that the output duty-cycle is far off the desired goal of 50%. Its output duty-cycle is: 2/n when n is an even number, or 3/n when n is an odd number, where n is the division ratio. The output waveform and duty-cycle of the circuit [2] is shown in Figure 12 (a). It limits the applications of the programmable divider. The proposed method can make the output duty-cycle of the programmable divider [2] very close to 50% (the duty-cycle error = |50% -"duty-cycle"| ≤ 5.6%), and keep the step of division ratio to be 1. The output waveform and duty-cycle of the proposed design is shown in Figure 12 (b). The output duty-cycle of the proposed design can be expressed as,

$$\text{Duty cycle} = \begin{cases} 50\% & \text{when divided by an even number,} \\ \dfrac{k}{2k+1}, & \text{when divided by an odd number } 2k+1 \end{cases} \tag{16}$$

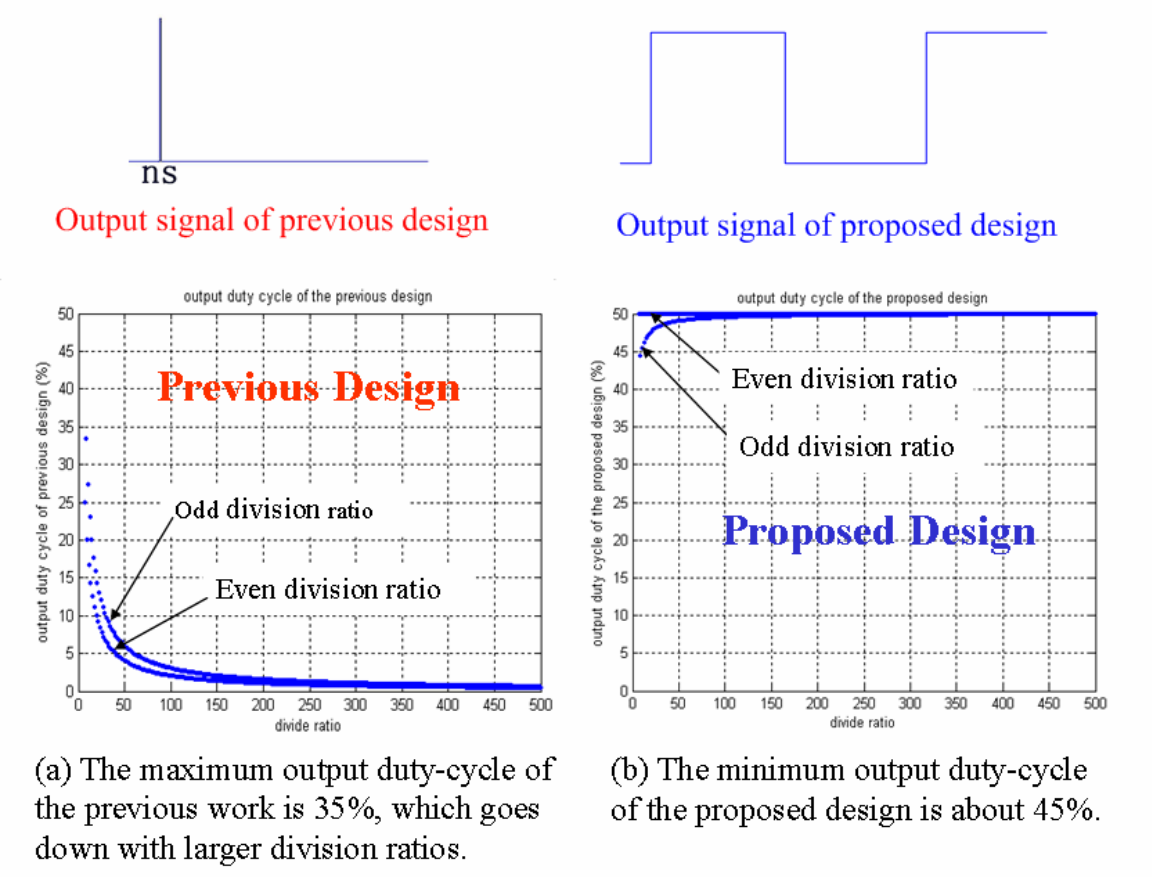


Figure 12: Comparison of the output duty-cycle of: (a) the prior art [2], and (b) the proposed design.

Since k is ≥ 4 (the minimum division ratio of the proposed design is 8), the duty-cycle error is ≤ 5.6%. When the division ratio is > 50, the duty-cycle error is < 1%. A few possible applications of the proposed programmable frequency divider with close to 50% output duty-cycle are described in the following sections.

2.3.1.1 Switched-Capacitor Filters

Switched-capacitor filters (SCFs) are widely used in audio systems, since they have advantages such as high accuracy and that varying the clock frequency can change the corner frequencies of SCFs [18]. Some SCFs need high-frequencies clock signals such as 160MHz [19]. If the proposed wide division-ratio divider follows a PLL output signal to generate the clock frequencies for the SCFs, the corner frequencies of the SCFs can be varied widely from several hundred MHz to arbitrary low frequencies. SCFs need equal and adequate time to settle when the clock signal is high or low. Thus the duty-cycle of the clock signal for a SCF should be as close to 50% as possible. Otherwise, there could be significant problems such as signal distortion, inaccurate filter response and signal attenuation [21].

Figure 13 shows that a switched capacitor can be viewed as an equivalent resistor. A switched capacitor (Figure 13 (b)) needs non-overlapping clock signals Φ_1 and Φ_2 (Figure 13 (c)), which can come from the output of a programmable divider. In Figure 13 (b), $M_1$and M_2 are connected to Φ_1, and M_3 and M_4 are connected to Φ_2. When Φ_1 is high (Figure 13 (d)), a charge $Q = (V_1 - V_2)C$ will flow from node V_1 to V_2. When Φ_2 is high

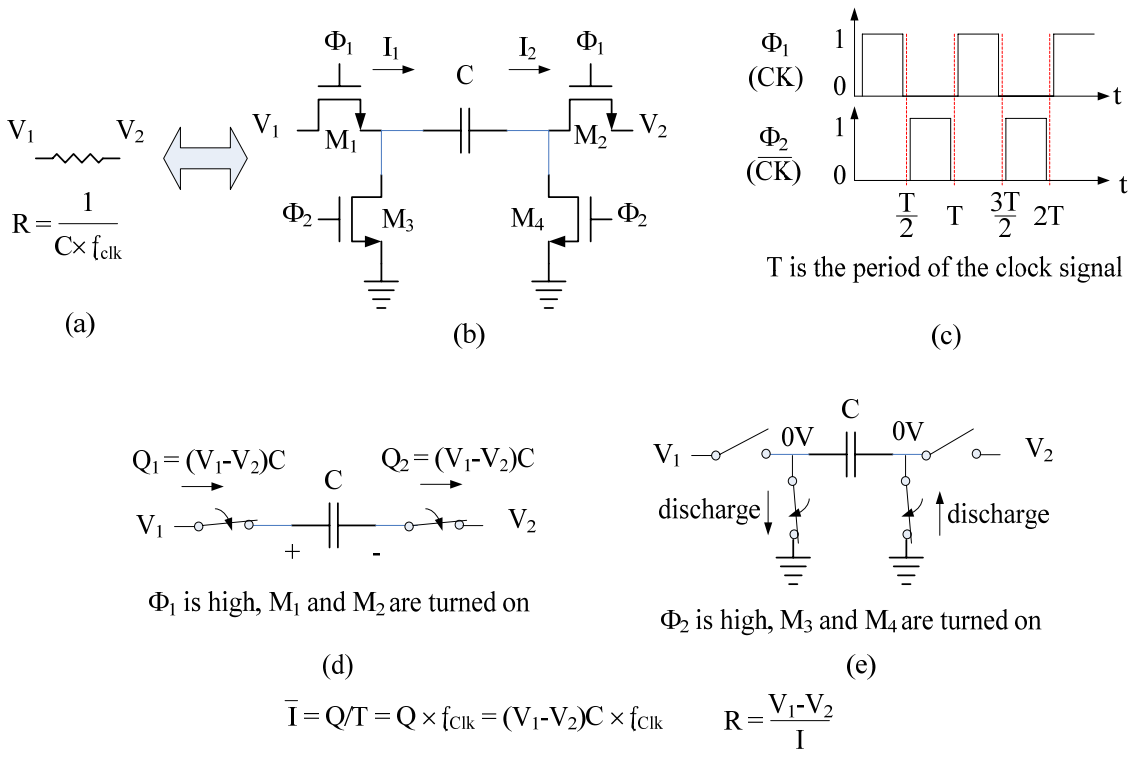


Figure 13: A switched capacitor viewed as a resistor: (a) the equivalent resistor, (b) a switched capacitor, (c) the non-overlapping clock signal for the switched capacitor, (d) when Φ_1 is high, and (e) when Φ_2 is high.

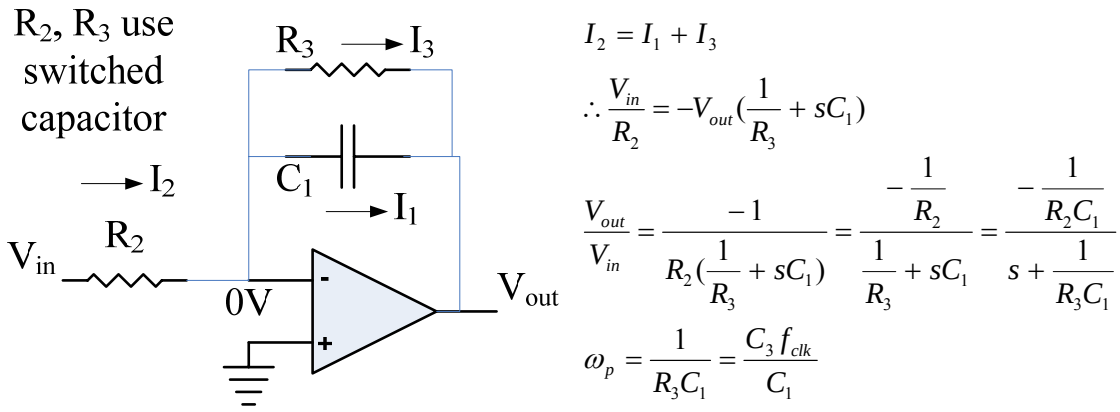


Figure 14: The principle of a switched capacitor filter (low-pass).

(Figure 13 (e)), no charge will flow from node V_1 to V_2, but C will be discharged through M_3 and M_4. During a full clock period, the average current flowing from V_1 to V_2 is,

$$\bar{I} = \frac{Q}{T_{clk}} = Q \cdot f_{clk} = (V_1 - V_2)C \cdot f_{clk} \tag{17}$$

The equivalent resistor will be,

$$R = \frac{V_1 - V_2}{\bar{I}} = \frac{V_1 - V_2}{(V_1 - V_2)C \cdot f_{clk}} = \frac{1}{C \cdot f_{clk}} \tag{18}$$

Figure 14 shows an example of a switched capacitor filter, whose corner frequency can be varied by the clock frequency. R_2 and R_3 are the equivalent resistances of the switch capacitors C_2 and C_3 (not shown) using the schematic in Figure 13 (b). Through the calculation in the right part of Figure 14, it can be shown that the circuit is a low-pass filter. The corner frequency is proportional to f_{clk}, which is the frequency of the clock signal applied to the switched capacitors C_2 and C_3. Thus a programmable frequency divider with a wide division ratio range is very useful for a switched capacitor filter. If

the input frequency of the divider is a fixed value, the output frequency can be changed widely. Using the programmable divider to drive the switched capacitors in Figure 14, the corner frequency of the low-pass filter can be changed widely, such as MHz down to kHz. The following relationship should exist,

$$f_{corner} \propto f_{clk} \propto \frac{1}{division\ ratio} \tag{19}$$

There are other types of switched capacitor filters, such as high-pass, band-pass, 2nd order and higher order filters. Their corner frequencies should also be able to be controlled by the clock frequency.

As mentioned before, clocked circuits prefer clock signals with 50% duty-cycle to be able to operate at higher frequencies. Since switched capacitor filters are clocked circuits, the programmable divider used for them should also have close to 50% output duty-cycle.

2.3.1.2 System-on-a-chip (SOC)

As stated in reference [22], "SOC needs multiple clocks and mostly with 50% duty-cycle in same chip," and "because many subsystems in SOC use both the rising and falling edges of the clock signals, we need to maintain a precise 50% duty-cycle to achieve the best performance for the systems. Also, use of a PLL with arbitrary frequency division (÷N) is a well known method for synthesizing desired frequency." Using a PLL followed by several programmable frequency-dividers with different division ratios can generate clock signals with different frequencies on the same chip, as shown in Figure 15.

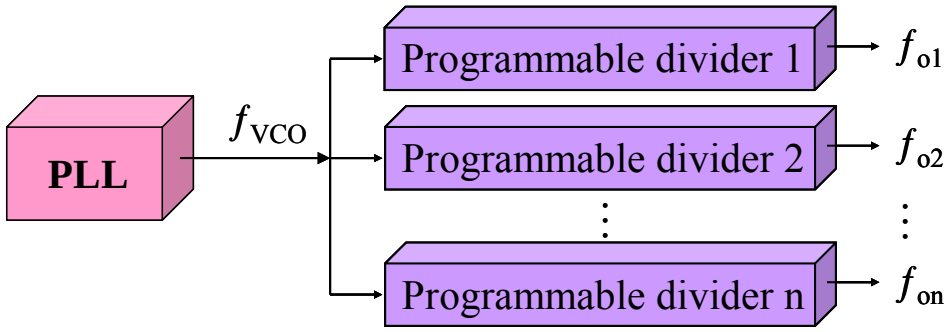


Figure 15: The block diagram showing the development of multi-frequency clock signals for SOCs, which needs multiple clocks and mostly with 50% duty-cycle on the same chip.

The proposed programmable frequency-divider has division ratios in a wide range and close-to-50% output duty-cycle. Thus it could be used to generate multiple clock signals for a SOC.

2.3.1.3 Variable Clock Signals for Different Power States of Digital Systems

Many digital systems have different operating states, such as normal state, snoop state, and sleeping state. The systems enter low power states to reduce power when it is possible. For example, Figure 16 shows the block diagram of the *Clock Control* and *Low Power States* for the *Intel® Pentium® M Processor with 2-MB L2 Cache and 533-MHz Front Side Bus* [23]. This processor has different supply-voltages and clock-frequency options for different states. Page 14 of the datasheet of this Processor [23] explains that "Multiple voltage/frequency operating points provide optimal performance at the lowest power" is a key feature of enhanced Intel speed step technology. Thus a PLL followed by the proposed programmable frequency-divider is a good option to generate different frequencies for different operating states. Since the output duty-cycle of the proposed

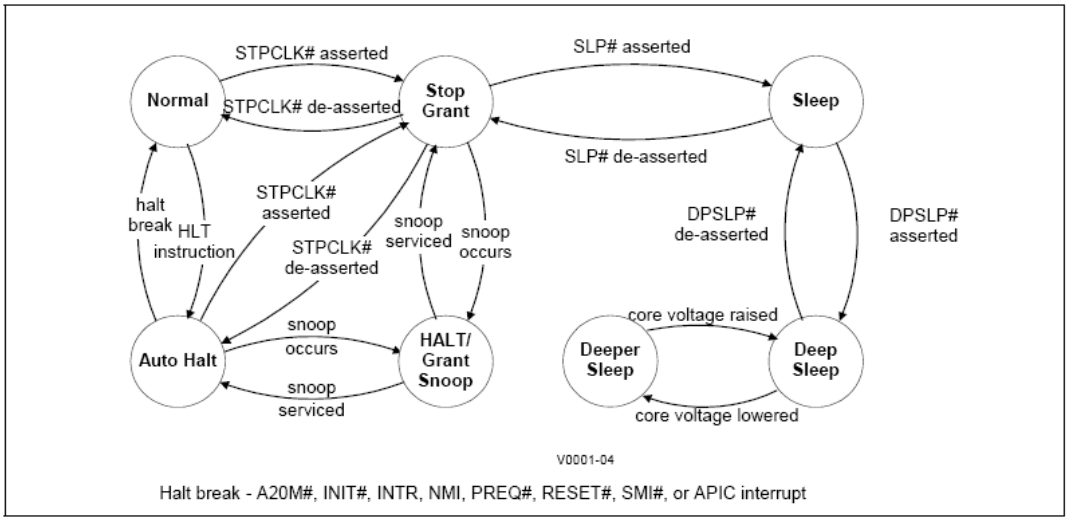


Figure 16: Block diagram of clock control and low power states for Intel® Pentium® M Processor with 2-MB L2 cache and 533-MHz front side bus [23] for wireless laptop computer.

divider is very close to 50%, the performance of the digital systems will be optimized [24] - [26].

There are other published literatures that state 50% duty-cycle is important for double data rate (DDR) circuits. In the abstract of the paper [27], there is the following statement "For those adopting double data rate (DDR) technology systems, the precise system timing plays a crucial role since both rising and falling edges of the system clock signal are used to sample the input data. Due to this requirement, it is necessary to accurately maintain the duty-cycle of the clock signal at 50%." The paper [28] states, "A duty cycle corrector (DCC) is a very important circuit for dual edge triggering systems". The

proposed design is also useful to generate clock signals with close to 50% duty-cycle for DDR circuits.

As explained in all of the above references, 50% duty-cycle of a clock signal is important for various implementations. It is easy to make the output duty-cycle of the programmable frequency-divider to be exactly 50%, by adding a divide-by-2 divider at the output stage. As stated in [29], the division ratio step will be 2 by using this method. This will degrade the output-frequency resolution, since the output-frequency resolution is the smallest variation of the output frequency. While the proposed design can make the output duty-cycle very close to 50%, and maintain the division ratio step to be 1.

2.3.2 Smaller Layout Area

The "2/3 cell" is the basic component of the programmable frequency divider [2] as shown in Figure 7. The schematic of the "2/3 cell" is shown in Figure 17 (a). It includes three "AND-latch" gates and one "D-latch". "AND-latch" is a source coupled logic (SCL) implementation of an AND gate combined with a latch function. The circuit in Figure 17 (b) shows the previous "AND-latch" design. The circuit in Figure 17 (c) shows the proposed "AND-latch" design for the 1st "2/3 cell" stage, and Figure 17 (d) for the 2nd to the end "2/3 cell" stages. Figure 17 (e) shows the proposed "D-latch" circuit used in each "2/3 cell".

The passive resistor loads in the previous "AND-latch" gate in Figure 17 (b) consume much area. In "TABLE I" of [2], for the "2/3 cell" operated at 16 MHz, the load

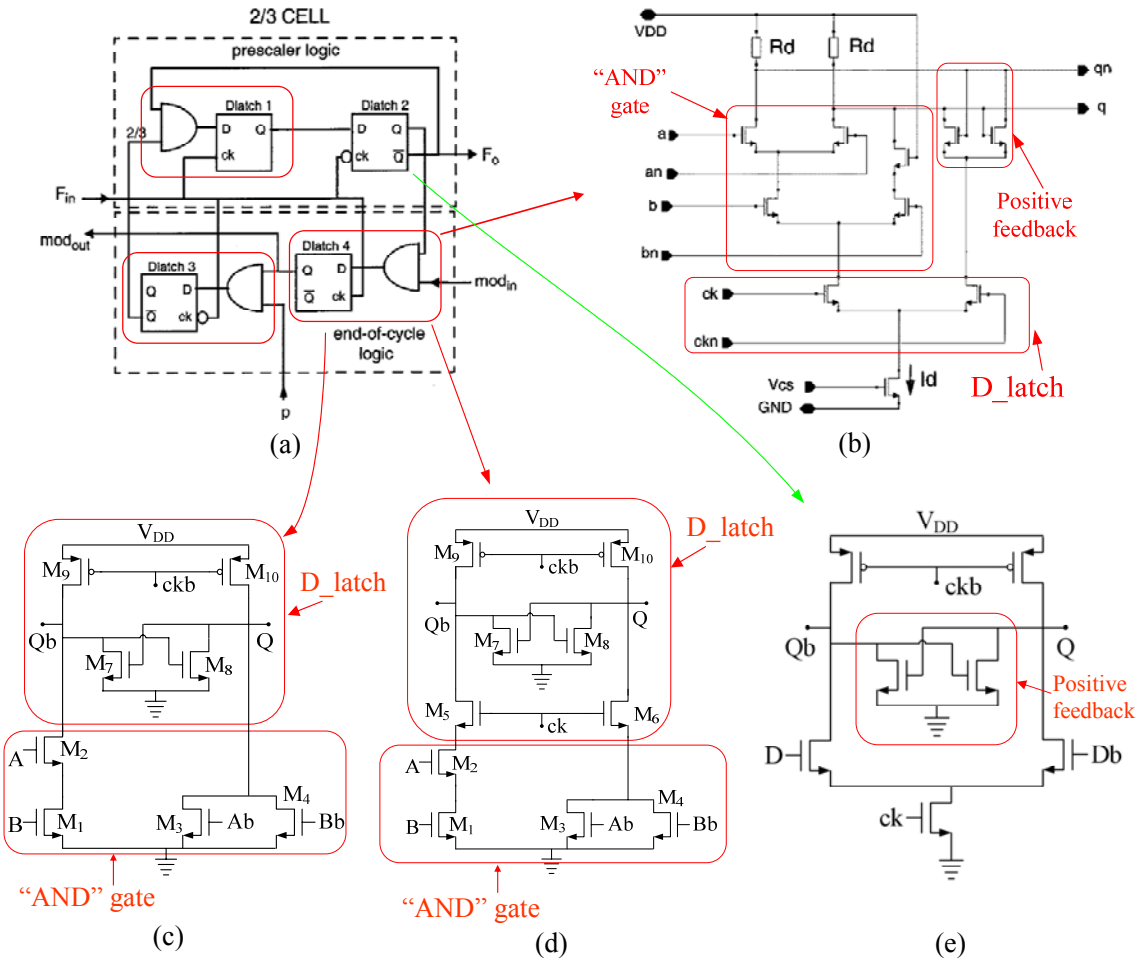


Figure 17: Comparison of the previous design [2] and the proposed design: schematics of: (a) a "2/3 cell", (b) previous "AND-latch", (c) proposed "AND-latch" for the first "2/3 cell" stage, (d) proposed "AND-latch" for the 2nd – the end "2/3 cell" stages, and (e) proposed D-latch in the "2/3 cell".

resistance should be 300 kΩ. In a known 0.18-μm process, the highest sheet resistance is 1006.9 ohm/square using poly resistor. Thus 300kΩ occupies about 300 unit squares. If 1 μm-wide poly is used, 3×2×300 = 1800 μm^2 is needed for each "2/3 cell", since each "AND-latch" gate needs 2 resistances and each "2/3 cell" contains 3 "AND- latch" gates. There are multiple "2/3 cell" in the entire divider. The proposed "AND-latch" gate as shown in Figure 17 (c) and (d) removed the passive resistors. In this way, the proposed design can significantly reduce the layout area.

Chapter 3
Design of the Proposed Programmable Divider

3.1 Design of the "2/3 Cell" Circuit

The "2/3 cell" is a divider with division ratio of 2 or 3. Through derivations, the division ratio of the "2/3 cell" is determined by the following equation.

$$\text{If } \text{mod}_{\text{in}} = 0, \text{mod}_{\text{out}} = 0 \;\&\; f_o = \frac{f_{in}}{2} \tag{20}$$

$$\text{If } \text{mod}_{\text{in}} = 1, \begin{cases} p = 1 \Rightarrow \text{mod}_{\text{out}} = f_o = \dfrac{f_{in}}{3} \\ p = 0 \Rightarrow \text{mod}_{\text{out}} = f_o = \dfrac{f_{in}}{2} \end{cases} \Rightarrow \text{mod}_{\text{out}} = f_o = \frac{f_{in}}{2+p} \tag{21}$$

As shown in Figure 17 (a), the "2/3 cell" includes three "AND-latch" gates and one "D-latch". Figure 17 (e) shows the proposed "D-latch" circuit used in each "2/3 cell". When "ck" is high, if "D" is high and "Db" is low, "Q_b" should be low and "Q" should be high. The "positive feedback" is used to hold the output levels at "Q" and "Q_b" when "ck" is low.

The proposed "AND-latch" designs are shown in Figure 17 (c) and (d). The circuit in Figure 17 (c) is used in the first "2/3 cell", whereas the circuit in Figure 17 (d) is used for the rest stages. In both Figure 17 (c) and (d), the "D-latch" part is used to allow the outputs to change when the clock signal "ck" is high. Transistors M_7 and M_8 in both circuits are used as positive feedback to hold the outputs "Q" and "Q_b". The difference between Figure 17 (c) and (d) is stated as follows. The gates of M_5 and M_6 in Figure 17

(d) are connected to the clock signal "ck". While in Figure 17 (c), M_5 and M_6 are removed, enabling the circuit to yield faster operation.

There are some concerns about the circuits in Figure 17 (c) and (d). The circuit in Figure 17 (c) is combined from the D-latch designs in the references [32]-[34] and an "AND" gate. It can achieve faster operation than the circuit in Figure 17 (d). However at low frequencies, the outputs of the circuit in Figure 17 (c) do not follow the "ck" signal well (shown in Figure 7 of [32], the duty-cycle of the output is not 50%). The reason is that without M_5 and M_6, even when "ck" is low, voltage at Q or Qb can still change. They should change only when "ck" is high. The output signal "mod_{out}" of the first stage need not drive a previous stage, since there is no previous stage. Thus it is appropriate to use the circuit in Figure 17 (c) in the first stage. Simulation and test results also show that using the circuit in Figure 17 (c) in the first stage does not violate the correct operation of the entire divider. On the other hand, since the output signals "mod_{out}" of the 2^{nd} – the end stages need to drive the input signal "mod_{in}" of previous stages, their duty-cycle should be 50% for correct operation. Thus the circuit in Figure 17 (d) is used in "2/3 cell" of the 2^{nd} – the end stages, since its output signals follow the "ck" correctly at lower frequencies. Its output signals can only change when "ck" is high due to the existence of M_5, M_6 and M_9, M_{10}. Therefore, using the circuit in Figure 17 (c) at the first "2/3 cell" and the circuit in Figure 17 (d) at the rest cells can achieve fast and correct operation.

3.2 Division Ratio Expression of Vaucher's Design [2]

3.2.1 Division Ratio Expression for the Basic Architechture [2]

With the time domain analysis of the "2/3 cell", it is found that the period of the output clock signal "f_{out}" is equal to the period of "mod_{out}" signal. It is also found that the time duration when the "mod_{out}" = 1 is always equal to,

$$time(\mathrm{mod}_{out}\ is\ 1) = T_{in} \tag{22}$$

where T_{in} is the period of the input signal "f_{in}" of the "2/3 cell". Equation (22) always exists whether the division ratio control P, and "mod_{in}" of the "2/3 cell" is logic 0 or 1. The time duration when the "mod_{out}" = 0 is equal to,

$$time(\mathrm{mod}_{out}\ is\ 0) = (1 + P \cdot \mathrm{mod}_{in}) \cdot T_{in} \tag{23}$$

It is related to the logic level of the division ratio control P, and the modulus control "mod_{in}".

The induction method will be used to verify the division ratio (shown in equation (1)) for the basic circuit in Figure 7 (a). Equation (1) is rewritten as follows,

$$division\ \ ratio = P_0 \cdot 2^0 + P_1 \cdot 2^1 + P_2 \cdot 2^2 + \cdots + P_{n-1} \cdot 2^{n-1} + 2^n \tag{24}$$

The following verification includes three sections for the induction method. In the three sections, the number of the "2/3 cell" stages will be (I) 1, (II) 2, and (III) n.

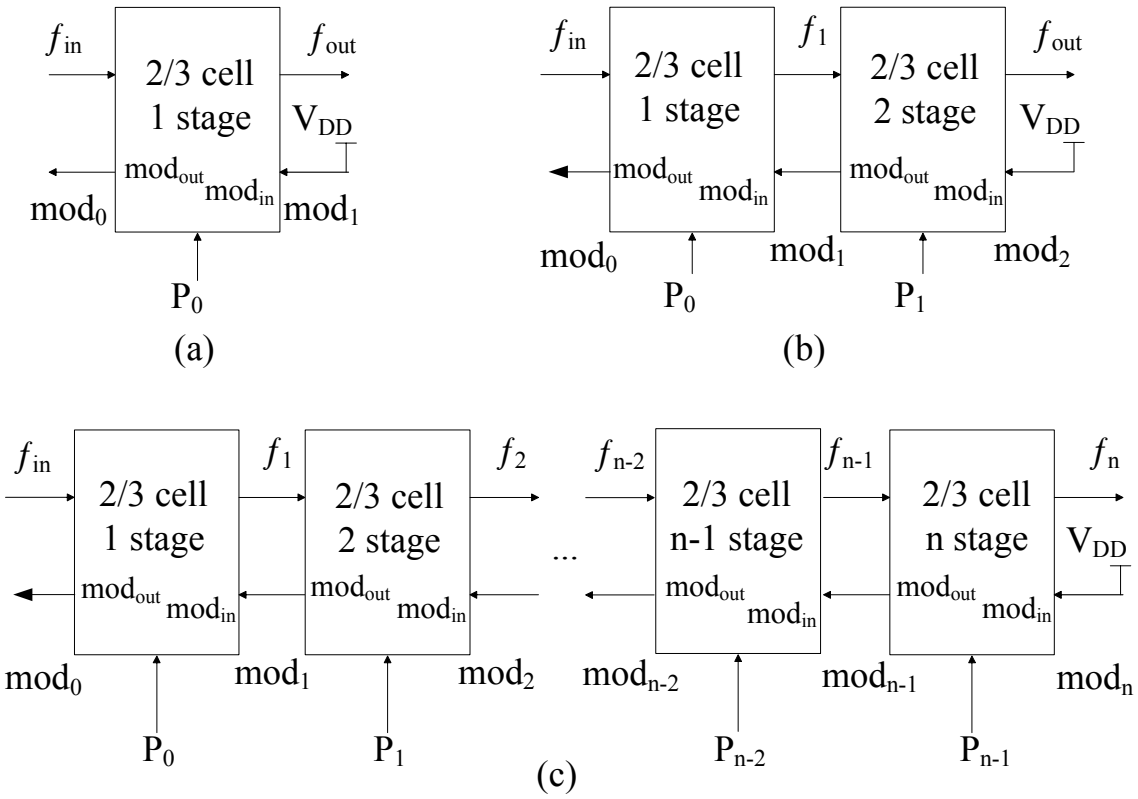


Figure 18: Schematics of the basic architecture of Vaucher's programmable divider **[2]**, with the following number of the "2/3 cell" stages: (a) 1, (b) 2, and (c) n.

(I) Figure 18 (a) shows the circuit when there is only one "2/3 cell" in the entire divider. The division ratio control P for the 1st "2/3 cell" is "P_0". According to equation (21), the division ratio will be,

$$division\ ratio = 2 + P_0 = 2^0 \cdot P_0 + 2^1 \tag{25}$$

Equation (25) is compatible with equation (24), with n = 1.

(II) Figure 18 (b) shows the circuit when there are two "2/3 cell" stages in the entire divider.

(Case 1) According to equation (22), the time duration when "mod_1" is "1" will be,

$$time(\mathrm{mod}_1\ is\ 1) = T_{in2} = T(f_1) \tag{26}$$

where T_{in2} is the period of the input signal of the 2nd "2/3 cell", which is also the period of the output signal f_{out} of the 1st "2/3 cell", $T(f_1)$. Since the "mod_{in}" signal of the 1st "2/3 cell" "$mod_1 = 1$", according to equation (21), the division ratio of the 1st "2/3 cell" will be $2 + P_0$. The division ratio control P for the 1st "2/3 cell" is "P_0". The period of the output signal f_{out} of the 1st "2/3 cell", $T(f_1)$ will be,

$$T(f_1) = (2 + P_0) \cdot T_{in} \tag{27}$$

where T_{in} is the period of the input signal of the entire divider.

By inserting equation (27) into equation (26), the following result could be obtained,

$$time(\mathrm{mod}_1\ is\ 1) = (2 + P_0) \cdot T_{in} \tag{28}$$

(Case 2) The division ratio control P for the 2nd "2/3 cell" is "P_1". According to equation (23), the time duration when $\mathrm{mod}_1 = 0$ will be,

$$time(\mathrm{mod}_1\ is\ 0) = (1 + P_1 \cdot \mathrm{mod}_{in2}) \cdot T_{in2} \tag{29}$$

Since "mod_{in2}", the "mod_{in}" signal of the 2nd "2/3 cell" is connected to V_{DD}, "mod_{in2}" = 1. Thus equation (29) can be written as,

$$time(\mathrm{mod}_1\ is\ 0) = (1 + P_1) \cdot T_{in2} = (1 + P_1) \cdot T(f_1) \tag{30}$$

Since $\mathrm{mod}_1 = 0$, according to equation (20), the division ratio of the 1st "2/3 cell" will be 2. The period of the output signal f_{out} of the 1st "2/3 cell", $T(f_1)$ will be,

$$T(f_1) = 2 \cdot T_{in} \tag{31}$$

By inserting equation (31) into equation (30), the following result could be obtained.

$$time(\mathrm{mod}_1\ is\ 0) = 2 \cdot (1 + P_1) \cdot T_{in} = (2 + 2 \cdot P_1) \cdot T_{in} \tag{32}$$

For the 2nd (the end) "2/3 cell", the period of the output clock signal "f_{out}" is equal to the period of the "mod_1" signal. The period of the "mod_1" signal will be the sum of the time duration when "mod_1" is 1 and the time duration when "mod_1" is 0. Thus the output period of the entire divider will be,

$$T_{out} = time(\mathrm{mod}_1\ is\ 1) + time(\mathrm{mod}_1\ is\ 0) \tag{33}$$

By inserting equation (28) and (32) into equation (33), the output period can be obtained as follows.

$$T_{out} = (2 + P_0) \cdot T_{in} + (2 + 2 \cdot P_1) \cdot T_{in} \tag{34}$$

$$T_{out} = (P_0 + 2 \cdot P_1 + 4) \cdot T_{in} = (2^0 \cdot P_0 + 2^1 \cdot P_1 + 2^2) \cdot T_{in} \tag{35}$$

Thus the division ratio of the entire divider will be,

$$division\ ratio = \frac{T_{out}}{T_{in}} = 2^0 \cdot P_0 + 2^1 \cdot P_1 + 2^2 \tag{36}$$

Equation (36) is compatible with equation (24), with n = 2.

(III) Suppose the division ratio for a divider with n-1 stages of the "2/3 cell" is equal to the following expression,

$$division\ ratio\ (n-1\ stages) = 2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^1 \cdot P_{n-2} + 2^{n-1} \tag{37}$$

If another stage is added after the existing n-1 stages, the new divider will have n stages.

(Case 1) According to equation (22), the time duration when "mod_{n-1}" is 1 will be,

$$time(\text{mod}_{n-1}\ is\ 1) = T_{in,n} = T(f_{n-1}) \tag{38}$$

where $T_{in,n}$ is the period of the input signal of the n^{th} "2/3 cell", which is also the period of the output signal f_{out} of the $(n-1)^{th}$ "2/3 cell", $T(f_{n-1})$. According to equation (37), the period of the output signal f_{out} of the $(n-1)^{th}$ "2/3 cell", $T(f_{n-1})$ will be,

$$T(f_{n-1}) = (2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^1 \cdot P_{n-2} + 2^{n-1}) \cdot T_{in} \tag{39}$$

By inserting equation (39) into equation (38), the following result could be obtained,

$$time(\text{mod}_{n-1}\ is\ 1) = (2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^1 \cdot P_{n-2} + 2^{n-1}) \cdot T_{in} \tag{40}$$

(Case 2) According to equation (23), the time duration when $\text{mod}_1 = 0$ will be,

$$time(\text{mod}_{n-1}\ is\ 0) = (1 + P_{n-1}) \cdot T_{in,n} = (1 + P_{n-1}) \cdot T(f_{n-1}) \tag{41}$$

According to equation (20), if "mod_{in}" = 0, "mod_{out}" = 0. Since "mod_{n-1}" = 0, all of the "mod_{out}" signals of the previous stages will be 0. Thus,

$$\text{mod}_{n-2}, \text{mod}_{n-3}, ..., \text{mod}_1, \text{mod}_0 = 0 \tag{42}$$

Thus the division ratio of the 1^{st} – the $(n-1)^{th}$ "2/3 cell" will all be equal to 2. The period of the output signal f_{out} of the $(n-1)^{th}$ "2/3 cell", $T(f_{n-1})$ will be,

$$T(f_{n-1}) = 2^{n-1} \cdot T_{in} \tag{43}$$

By inserting equation (43) into equation (41), the following result could be obtained,

$$time(\text{mod}_{n-1}\ is\ 0) = 2^{n-1} \cdot (1 + P_{n-1}) \cdot T_{in} = (2^{n-1} + 2^{n-1} \cdot P_{n-1}) \cdot T_{in} \tag{44}$$

For the n^{th} (the end) "2/3 cell", the period of the output clock signal is equal to the period of the "mod_{n-1}" signal. The period of the "mod_{n-1}" signal will be the sum of the time duration when "mod_{n-1}" is 1 and the time duration when "mod_{n-1}" is 0. Thus the output period of the entire divider will be,

$$T_{out} = time(\text{mod}_{n-1}\ is\ 1) + time(\text{mod}_{n-1}\ is\ 0) \tag{45}$$

By inserting equation (40) and (44) into equation (45), the output period can be obtained as follows.

$$T_{out} = (2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^1 \cdot P_{n-2} + 2^{n-1}) \cdot T_{in} + (2^{n-1} + 2^{n-1} \cdot P_{n-1}) \cdot T_{in} \tag{46}$$

$$T_{out} = (2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^1 \cdot P_{n-2} + 2^{n-1} \cdot P_{n-1} + 2^n) \cdot T_{in} \tag{47}$$

Thus the division ratio of the entire n stage divider will be,

$$division\ ratio\ (n\ stage) = \frac{T_{out}}{T_{in}} = 2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^1 \cdot P_{n-2} + 2^{n-1} \cdot P_{n-1} + 2^n \tag{48}$$

It is the same as equation (24). Thus the above derivations should prove the division ratio expression of the basic architecture of Vaucher's programmable divider [2].

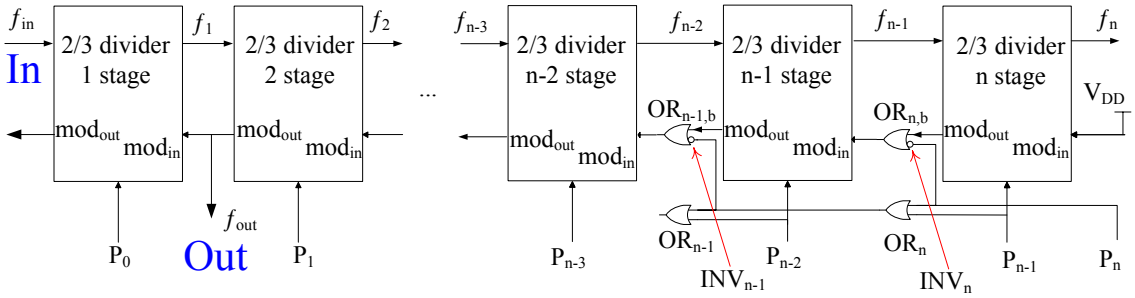


Figure 19: Vaucher's design with extended division range ($2^{min} \le N \le 2^{max+1}$-1) [2].

3.2.2 Division Ratio Expression for Vaucher's Design with Extended Division Range [2]

Vaucher's design with extended division range ($2^{min} \le N \le 2^{max+1}$-1) [2], or Figure 7 (b) gives designers more division ratio options and flexibilities to use the divider in different applications. Figure 7 (b) is redrawn in Figure 19. The following derivation will explain the procedure to obtain the division ratio expression for the divider shown in Figure 19.

Compared with the basic architecture as shown in Figure 18 (b), the following differences exists: (1) several "OR" and "INV" gates are added, (2) the output signal of the entire divider is changed to the "mod_{out}" signal of the 2nd stage "2/3 divider", instead of using the "f_{out}" of the nth "2/3 divider". The small circuit at the input of "$OR_{n,b}$" and "$OR_{n-1,b}$" represents inverters.

For the example shown in Figure 19, min = n-2, max = n. The following derivation will explain the division ratio for three cases: (I) "P_n =1", (II) "P_n P_{n-1} = 0 1" (III) "P_n P_{n-1} = 0 0".

(I) "P_n P_{n-1} P_{n-2} …P_1 P_0 = 1 x x … x x ". "P_n" is equal to logic 1, the output of "INV_n" will be 0. Since "P_n" is equal to logic 1, the output of the "OR_n" will be 1. Thus the output of "INV_{n-1}" will be 0. Since the outputs of "INV_n" and "INV_{n-1}" are both 0, they will not affect the outputs of "$OR_{n,b}$" and "$OR_{n-1,b}$". The "mod_{in}" signal of the $(n-1)^{th}$ stage will be equal to the "mod_{out}" of the n^{th} stage. It seems like that the "mod_{in}" signal of the $(n-1)^{th}$ stage is connected to the "mod_{out}" of the n^{th} stage directly. For the same reason, it should seem like that the "mod_{in}" signal of the $(n-2)^{th}$ stage is connected to the "mod_{out}" of the $(n-1)^{th}$ stage directly. The division ratio of the entire divider will be the same as the basic architecture as shown in Figure 18 (b) with n "2/3 cell" stages. Thus the division ratio will be the same as shown in equation (48), which can be rewritten as follows.

$$division\ ratio\ (P_n\ is\ 1) = 2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^{n-2} \cdot P_{n-2} + 2^{n-1} \cdot P_{n-1} + 2^n \cdot P_n \qquad (49)$$

If all of "P_{n-1}", …, "P_1" and "P_0" are logic 1, the division ratio of the divider will be the maximum value, which is 2^{n+1}-1, or 2^{max+1}-1 (max = n).

(II) "P_n P_{n-1} P_{n-2} …P_1 P_0 = 0 1 x … x x ". "P_n" is equal to logic 0, the outputs of "INV_n" will be 1. The output of "$OR_{n,b}$" will always be 1. Thus the "mod_{in}" signal of the $(n-1)^{th}$ stage "2/3 cell" will always be 1. Since "P_{n-1}" is equal to logic 1, the output of "OR_n" will be 1. The "mod_{in}" signal of the $(n-2)^{th}$ stage will be equal to the "mod_{out}" of the $(n-1)^{th}$ stage. The division ratio of the entire divider will be the same as the basic architecture as shown in Figure 18 (b) with (n-1) "2/3 cell" stages. The division ratio when "P_n P_{n-1} P_{n-2} …P_1 P_0 = 0 1 x … x x " can be written as follows.

$$division\ ratio\ ("P_n\ P_{n-1}"\ is\ "01") = 2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^{n-2} \cdot P_{n-2} + 2^{n-1} \qquad (50)$$

Equation (50) can be rewritten as the following one.

$$division\ ratio\ (P_n\ P_{n-1}\ is\ "01") = 2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^{n-2} \cdot P_{n-2} + 2^{n-1} \cdot P_{n-1} + 2^n \cdot P_n \quad (51)$$

If equation (49) and equation (51) are combined, the following result could be obtained. If any of P_{min+1}, P_{min+2}, …, P_{max-1}, P_{max} = 1, or division ratio is $\geq 2^{min+1}$, (min = n-2, max = n), the division ratio will be,

$$division\ ratio = 2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^{n-2} \cdot P_{n-2} + 2^{n-1} \cdot P_{n-1} + 2^n \cdot P_n \quad (52)$$

(III) "P_n P_{n-1} P_{n-2} …P_1 P_0 = 0 0 x … x x ". Both "P_n" and "P_{n-1}" are equal to logic 0, the output of "OR_n" will be 0. The outputs of "INV_{n-1}" will be 1. The output of "$OR_{n-1,b}$" will always be 1. Thus the "mod_{in}" signal of the $(n-2)^{th}$ stage "2/3 cell" will always be 1. The output of "OR_{n-1}" is not connected to anywhere. The division ratio of the entire divider will be the same as the basic architecture as shown in Figure 18 (b) with (n-2) "2/3 cell" stages. "P_{n-2}" has no effect in the division ratio. The corresponding division ratio could be written as follows.

If all of P_{min+1}, P_{min+2}, …, P_{max-1}, P_{max} = 0, or division ratio is $< 2^{min+1}$, (min = n-2, max = n), the division ratio will be,

$$division\ ratio = 2^0 \cdot P_0 + 2^1 \cdot P_1 + ... + 2^{n-3} \cdot P_{n-3} + 2^{n-2} \quad (53)$$

If all of "P_{n-3}", …, "P_1" and "P_0" are logic 0, the division ratio of the divider will be the minimum value, which is 2^{n-2}, or 2^{min} (min = n-2).

For other "min" and "max" values, the division ratios can be obtained in a similar way. Thus the division ratio of Vaucher's divider [2] shown in Figure 19 is obtained.

(a) If all of P_{min+1}, P_{min+2}, …, P_{max-1}, P_{max} = 0, or division ratio is < 2^{min+1},

$$\begin{aligned} division\ ratio &= P_0 \cdot 2^0 + P_1 \cdot 2^1 + \cdots + P_{\min-1} \cdot 2^{\min-1} + 2^{\min} \\ &= \sum_{i=0}^{\min-1} P_i \cdot 2^i + 2^{\min}; \end{aligned} \tag{54}$$

(b) Other wise, if any of P_{min+1}, P_{min+2}, …, P_{max-1}, P_{max} = 1, or division ratio is ≥ 2^{min+1},

$$\begin{aligned} &division\ ratio \\ &= P_0 \cdot 2^0 + P_1 \cdot 2^1 + \cdots + P_{\min-1} \cdot 2^{\min-1} + P_{\min} \cdot 2^{\min} + \cdots + P_{\max-1} \cdot 2^{\max-1} + P_{\max} \cdot 2^{\max} \\ &= \sum_{i=0}^{\max} P_i \cdot 2^i \end{aligned} \tag{55}$$

Both equation (54) and (55) are in binary format. The special case is that when the division ratio is < 2^{min+1}, the control signal P_{min} has no effect.

When the division ratio is < 2^{min+1}, P_{min} is set to logic "1", and then equation (54) can be rewritten as,

$$division\ ratio = P_0 \cdot 2^0 + P_1 \cdot 2^1 + \cdots + P_{\min-1} \cdot 2^{\min-1} + P_{\min} \cdot 2^{\min} \tag{56}$$

Equation (56) is compatible with equation (55). Thus equation (57) alone can be used to express the division ratio for all cases, with the following condition:

When the division ratio is $< 2^{min+1}$, P_{min} is set to logic "1", then,

$$\begin{aligned} &division\ \ ratio \\ &= P_0 \cdot 2^0 + P_1 \cdot 2^1 + \cdots + P_{\min -1} \cdot 2^{\min -1} + P_{\min} \cdot 2^{\min} + \cdots + P_{\max -1} \cdot 2^{\max -1} + P_{\max} \cdot 2^{\max} \end{aligned} \quad (57)$$

For the circuit shown in Figure 19, min = n-2, and max = n.

If the division ratio is $< 2^{n-1}$, P_{n-2} is set to logic "1". The division ratio for Figure 19 will be,

$$division\ ratio = P_0 + P_1 \cdot 2^1 + P_2 \cdot 2^2 + \cdots + P_{n-1} \cdot 2^{n-1} + P_n \cdot 2^n \quad (58)$$

Equation (54) and (55) are quite complicated. For compactness, the following calculations will use equation (58).

3.3 The Proposed "Solution 1" with 50% Duty-Cycle

The output pulse width of Vaucher's divider [2] is very narrow. Thus it has poor capability to drive other circuits. The circuit shown in Figure 20 can generate output signals with very close to 50% duty-cycle, while retaining the same division ratios as 2^{min} to 2^{max+1}-1.

In order to achieve 50% duty-cycle, a divide-by-2 divider, "Div2", is added at the output of "Div_n_vaucher" (shown in bottom-left part of Figure 19). An "AND" gate and an "n bit half adder" are also included in the feedback loop as shown in Figure 20. Figure 21 shows the schematics of a 1-bit half adder and a 1-bit full adder. The "n bit half adder" includes n stages of "1-bit half adder" connected in series. The first stage is the least

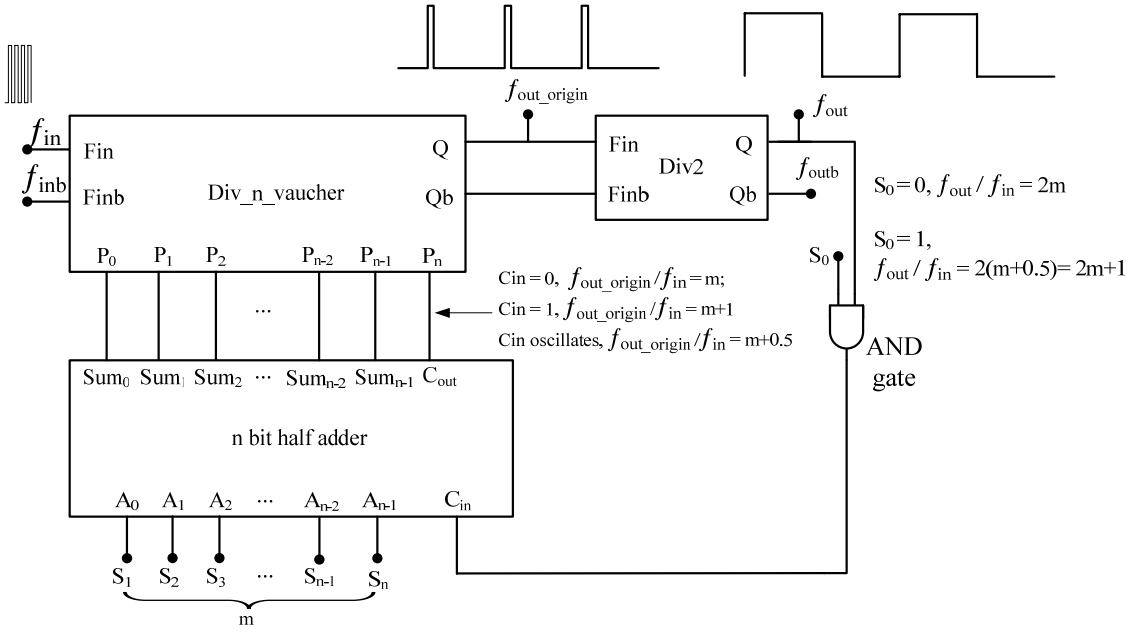


Figure 20: Schematic of the proposed "Solution 1" to generate output signal with 50% duty-cycle.

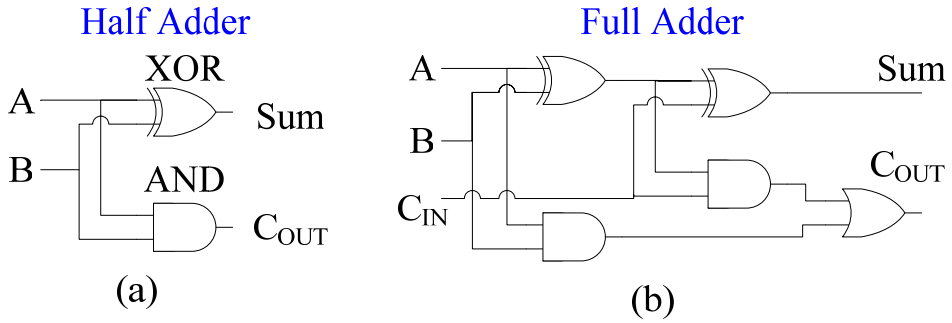


Figure 21: Schematics of: (a) a 1-bit half adder, and (b) a 1-bit full adder.

significant bit (LSB). The "B" input of each "1-bit half adder" (shown in Figure 21 (a)) should be conntected to the "C_{out}" of the previous stage. The "B" input of the first "1-bit half adder" is used as "Cin" of the "n bit half adder" in Figure 20.

In Figure 20, the original output signal is "f_{out_origin}" (top-middle part), whose duty cycle is far-off 50%. The duty cycle of the proposed output, "f_{out}" (top-right part), is very close to 50%. This is because "f_{out}" is the output of "Div2", and the period of "f_{out_origin}" changes very little. S_0, S_1, …, S_n are the division ratio controls of the proposed divider. "S_0" is the LSB (Least Significant Bit). "f_{out}" and "S_0" are the inputs of the "AND" gate.The output of the "AND" gate is fed to the C_{in} input of the "n bit half-adder". The outputs of the adder are used as the division ratio controls for "Div_n_vaucher".

The binary combination of (S_1, S_2, …, S_n) is represented as "*m*", thus,

$$m = S_1 + S_2 \cdot 2^1 + S_3 \cdot 2^2 + \cdots + S_{n-1} \cdot 2^{n-2} + S_n \cdot 2^{n-1} \tag{59}$$

For the "Div_n_vaucher" in Figure 19, $P_{min} = P_{n-2}$, and $P_{max} = P_n$ as stated before.

P_{n-2} or S_{n-1} is set to logic "1" when the division ratio of "Div_n_vaucher" is $< 2^{n-1}$ (or the proposed division ratio is $< 2^n$). Thus equation (58) can be used to represent the division ratio of "Div_n_vaucher".

If "S_0" is 0, the binary combination of the adder outputs will be equal to "m". The ratio of "f_{in} / f_{out_origin}" will also be equal to "m". After "Div2", the ratio of "f_{in} / f_{out}" will be equal to,

$$2 \times m = 0 + S_1 \cdot 2^1 + S_2 \cdot 2^2 + S_3 \cdot 2^3 + \cdots + S_{n-1} \cdot 2^{n-1} + S_n \cdot 2^n \quad (60)$$

If "S_0" is "1", the signal at input "C_{in}" of the adder will oscillate between "0" and "1", with a close to 50% duty-cycle. The binary outputs of the adder (or the division ratio of "Div_n_vaucher") will have an average value of 0.5 + m. Thus the average ratio of "f_{in} / f_{out}" will be equal to,

$$2 \times (0.5 + m) = 1 + S_1 \cdot 2^1 + S_2 \cdot 2^2 + S_3 \cdot 2^3 + \cdots + S_{n-1} \cdot 2^{n-1} + S_n \cdot 2^n \quad (61)$$

If equations (60) and (61) are combined, the division ratio can be written as follows,

$$proposed\ \ division\ \ ratio = S_0 + S_1 \cdot 2^1 + S_2 \cdot 2^2 + S_3 \cdot 2^3 + \cdots + S_{n-1} \cdot 2^{n-1} + S_n \cdot 2^n \quad (62)$$

The proposed division ratio expressed in equation (62) is the same as the original one in equation (58) (except for that "P" is changed to "S").

The output duty-cycle of the proposed design can be calculated as follows. When "S_0" is 0, the division ratio is an even number as shown in equation (60). Since the adder outputs or the division ratio of "Div_n_vaucher" do not change, neither f_{out_origin} nor the period T_{out_origin} changes. After "Dvi2", the duty-cycle of f_{out} will be exactly 50%. When "S_0" is 1, the division ratio is an odd number as shown in equation (61). Since the adder outputs or the division ratio of "Div_n_vaucher" changes between m and m+1, T_{out_origin} changes between $m \times T_{in}$ and (m+1) $\times T_{in}$, where T_{in} is the period of the input signal. The "on" and "off" time of the proposed output signal f_{out} will be $m \times T_{in}$ and (m+1) $\times T_{in}$. Thus when the division ratio is an odd number, the duty-cycle of the proposed output is m / (2m+1), where 2m+1 is the division ratio. These results are compatible with equation (16).

According to the above analysis, the proposed circuit in Figure 20 generates an output signal with close to 50% duty-cycle, also keeps the step size of the division ratio to be 1 (by changing the LSB control bit "S_0").

3.4 Proposed "Solution 2" with 50% Duty-Cycle

The above scheme, "Solution 1", does not work for the isolated division ratios of 2^r-1 (such as 15, 31, 63, 127), where "r" is a natural number. The proposed "Solution 2" scheme shown in Figure 22 solved this problem. Figure 22 (a) shows the top level circuit of Solution 2. Figure 22 (b) shows the revised "2/3 cell" for "Solution 2". Figure 22 (c) shows the circuit to judge the "0/1" edge of the control digits.

It is also important to keep the uniformity of the division ratio expression as shown in equation (57). The same method could be used as in the proposed "Solution 1". It is also the requirement stated just above equation (57). When the division ratio is $< 2^{min+1}$, "P_{min}" should be set to logic "1".

As shown in Figure 22 (a), if a "2/3 cell" is connected to the first nonzero control-digit in the MSB (most significant bit) part, this "2/3 cell" is "on edge". For the particular example shown at the bottom of Figure 22 (a), P_{n-2} is the first nonzero control-digit counting down from the MSB part. Thus the $(n-1)^{th}$ "2/3 cell" stage, which is connected

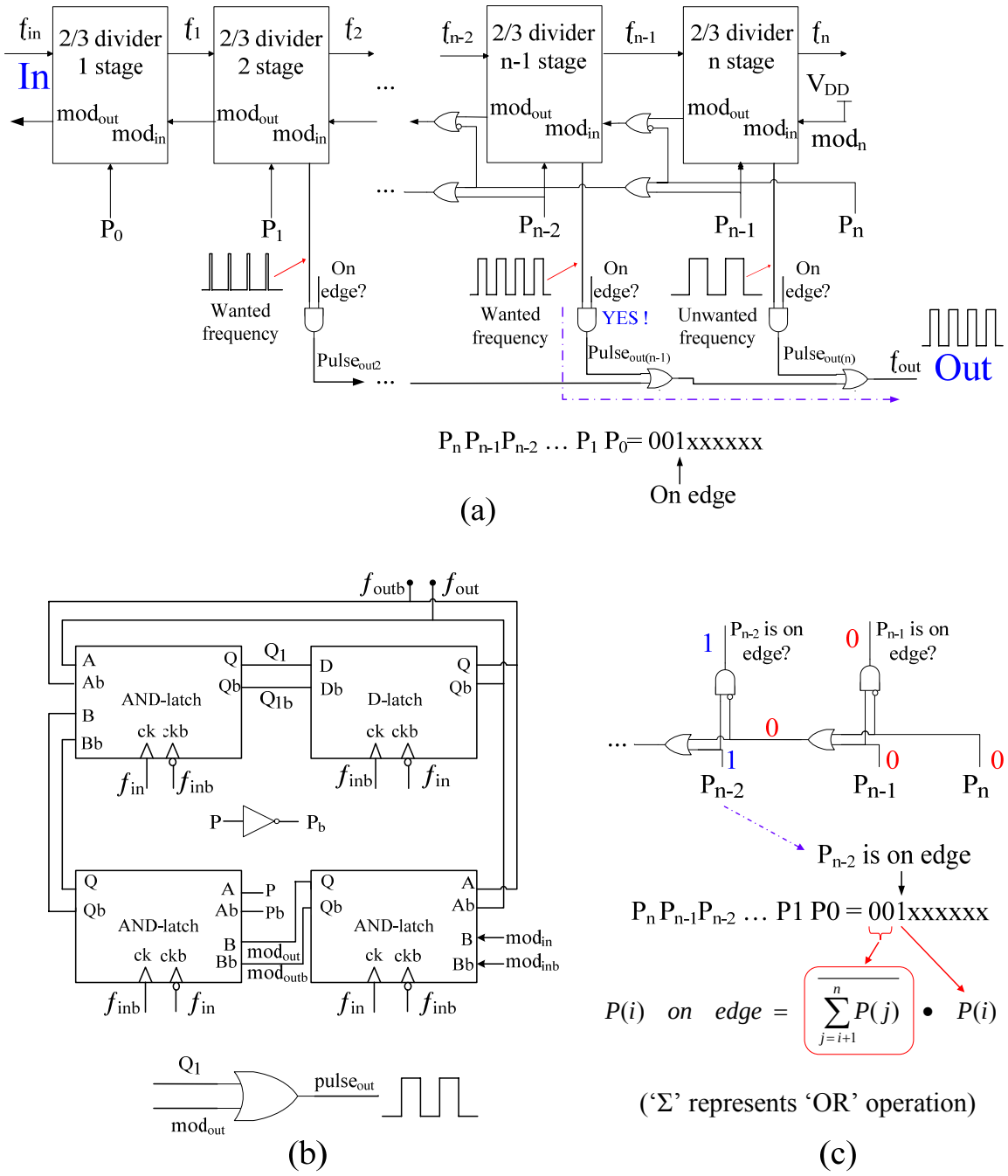


Figure 22: Schematics of the proposed “Solution 2” for the division ratios of “2^r - 1” with 50% output duty-cycle: (a) top level scheme, (b) circuit to generate “$pulse_{out}$” in each “2/3 cell”, and (c) the “on edge” judgment circuit.

with P_{n-2} signal, is "on edge". The "$pulse_{out}$" signals from the on-edge "2/3 cell" and the previous cells have the desired output frequency, which is "f_{in} / (the expected division ratio)". The "$pulse_{out}$" signals from the latter "2/3 cell" have unwanted frequencies, which are different from "f_{in} / (the expected division ratio)". Among the "$pulse_{out}$" signals from the on-edge "2/3 cell" and the previous cells, the signal from the on-edge cell has a duty-cycle closest to 50%. Thus the "$pulse_{out}$" signal from this on-edge cell will be used as the output for the entire divider.

Figure 22 (b) shows the revised "2/3 cell". It is drawn in a differential mode, for example both "D" and "Db" are drawn in the "D-latch". Actually, the only difference between the revised "2/3 cell" and the one shown in Figure 17 (a) is that an "OR" gate is added in the revised one to generate the "$pulse_{out}$" signal. The signals "Q_1" and "mod_{out}" are the inputs of the "OR" gate. When the division ratio is a "2^r - 1" number, the "$pulse_{out}$" signal of the "on-edge" "2/3 cell" has a duty-cycle of $\frac{k}{2k+1}$, where $2k + 1 = 2^r - 1$ or the division ratio. Since the division ratio "2^r - 1" is an odd number, this duty-cycle is compatible with the expression shown in equation (16).

Figure 22 (c) shows the circuit to judge the "0/1" edge of the control digits, or the first nonzero control-digit in the MSB part. In the figure, the expressions have the following meaning,

$$\sum_{j=i+1}^{n} P(j) = (P_{j+1}) \; OR \; (P_{j+2}) \; OR \; ... \; OR \; (P_{n-1}) \; OR \; (P_n) \tag{63}$$

$$\overline{\sum_{j=i+1}^{n} P(j)} = NOT\ (\ \sum_{j=i+1}^{n} P(j)\ ) \tag{64}$$

As the example shown in Figure 22 (c), if "$P_nP_{n-1}P_{n-2} = 001$", P_{n-2} will be the first nonzero control-digit counting down from the MSB part. If "OR" operations are applied to all the MSB digits before P_{n-2}, the result will be 0. The inversion of this result 0 is 1. If "AND" operation is applied to the inversion signal "1" and P_{n-2}, the result will be 1. Only when P_{n-2} is "on-edge", the result will be 1. The results for other control digits will all be 0. By implementing the combination of "OR", "AND" and "inverter" logic gates, the "P_{n-2} is on edge?" signal will be high. Thus the circuit shown in Figure 22 (c) can judge the on-edge cell automatically.

The proposed "Solution 2" shown in Figure 22 can solve the problem of the proposed "Solution 1". When the division ratio is "2^r-1" number, the output duty-cycle of "Solution 2" is $\frac{k}{2k+1}$, where $2k + 1$ is the division ratio.

3.5 Combination of the Proposed Solution 1 and 2 with 50% Duty-Cycle

To obtain close-to-50% output duty-cycle for each division ratio, the proposed "Solution 1" and "Solution 2" are combined together, as shown in Figure 23. With the circuit shown in Figure 24, the proposed divider will automatically judge if the division ratio has

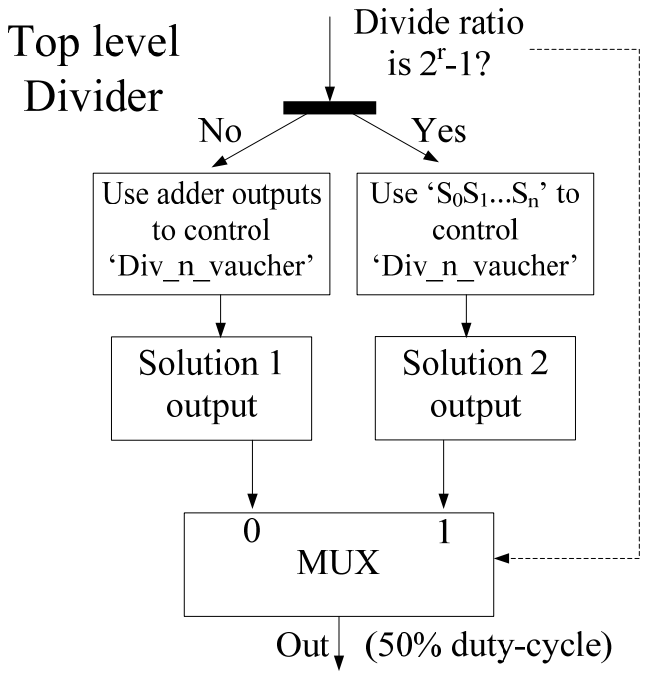


Figure 23: Combination of "Solution 1" and "Solution 2" in the proposed design.

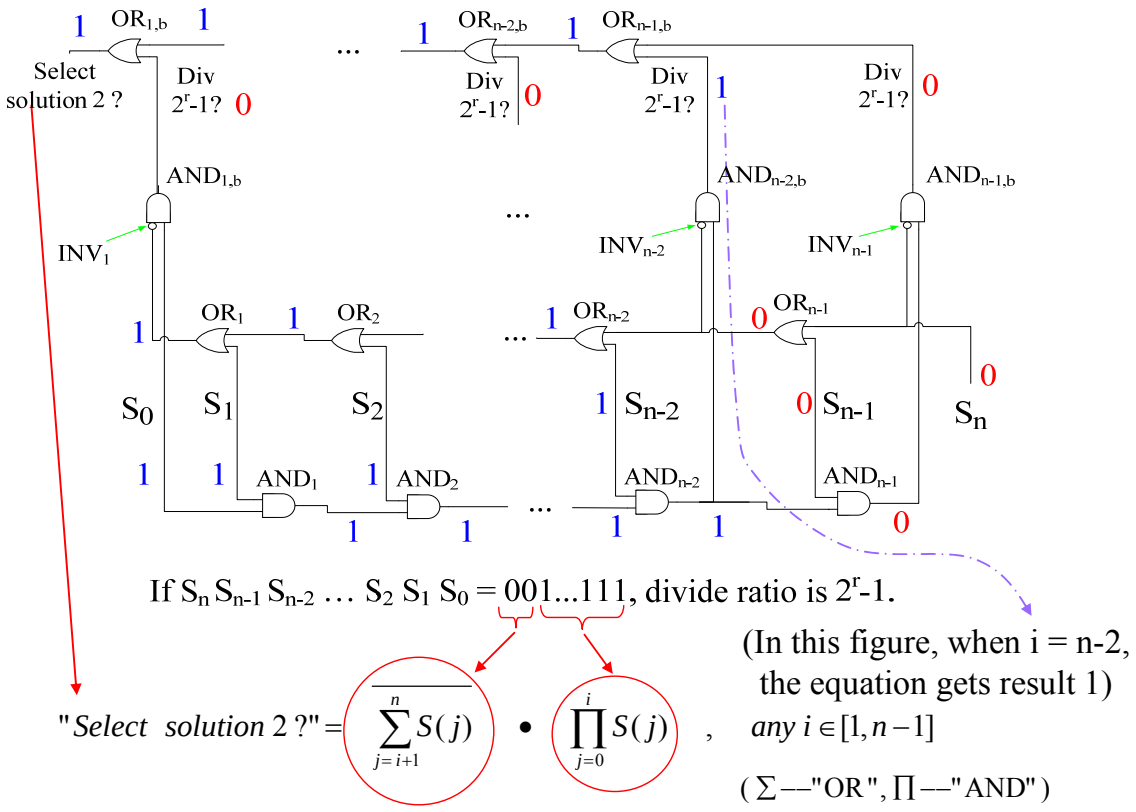


Figure 24: Division ratio judgment circuit.

the "$2^r - 1$" format. If the division ratio is not a "$2^r - 1$" number, the control digits "$S_0S_1\ldots S_n$" will be assigned to the adder inputs and the AND gate input as shown in Figure 20. Thus the adder outputs will be used to control the division ratio of "Div_n_vaucher". "Div2" output shown in Figure 20 is used as the final output. Otherwise, if the division ratio is a "$2^r - 1$" number, the control digits "$S_0S_1\ldots S_n$" are assigned directly to the controls "$P_0P_1\ldots P_n$" of "Div_n_Vaucher"(the circuit shown in Figure 22 (a)). The output shown in Figure 22 (a) is used as the final output. In order to keep the uniformity of the division ratio expression, when the division ratio is $< 2^{min+1}$, S_{min} should be set to logic "1" similarly to equation (57). Here "$S_0S_1\ldots S_n$" are the division ratio controls of the top level design.

Figure 24 shows the circuit to judge if the division ratio is a "$2^r - 1$" number. Some expressions at the bottom of the Figure 24 have the following meaning,

$$\sum_{j=i+1}^{n} S(j) = (S_{j+1})\ OR\ (S_{j+2})\ OR \ldots OR\ (S_{n-1})\ OR\ (S_n) \tag{65}$$

$$\prod_{j=0}^{i} S(j) = (S_0)\ AND\ (S_1)\ AND \ldots AND\ (S_{i-1})\ AND\ (S_i) \tag{66}$$

If a number has the "2^r - 1" format, it should be able to be expressed in binary format as "0…01...111". Number i_{edge} is used to represent the index of the first nonzero digit counting down from the MSB (left) part. For the example shown in Figure 24, if $S_n\ S_{n-1}S_{n-2}\ \ldots\ S_2\ S_1\ S_0 = 001...111$, the division ratio is a "$2^r - 1$" number, and r = n-1. The first nonzero MSB control digit is S_{n-2}, so i_{edge} = n-2. The MSB digits "S_n" and "S_{n-1}", the

digits left to S_{n-2}, are all 0. If the logic "OR" operations are applied to all of the MSB digits "S_n" and "S_{n-1}",

$$A = \sum_{j=i+1}^{n} S(j) = 0 \Rightarrow \overline{A} = 1, \text{ here } i = \text{n-2}. \tag{67}$$

If the logic "AND" operations are applied to all of the LSB digits (including digit S_{n-2}), "S_{n-2} ", …, "S_2", "S_1", "S_0", the following result will be obtained.

$$B = \prod_{j=0}^{i} S(j) = 1, \text{ where } i = \text{n-2}. \tag{68}$$

$$\text{Thus } \overline{\sum_{j=i+1}^{n} S(j)} \bullet \prod_{j=0}^{i} S(j) = \overline{A} \bullet B = 1, \text{ where } i = \text{n-2}. \tag{69}$$

In the middle part of Figure 24, the gates "AND_1", "AND_2", …, "AND_{n-1}" are used to realize the logic "AND" operations $B = \prod_{j=0}^{i} S(j)$ in the circuit. The gates "OR_1", "OR_2", …, "OR_{n-1}" are used to realize the logic "OR" operations $A = \sum_{j=i+1}^{n} S(j)$. At the upper part of Figure 24, the small circles "o" at the inputs of "$AND_{1,b}$", …, "$AND_{n-2,b}$", "$AND_{n-1,b}$" are inverters. They are applied to A to realize the logic "NOT" operation to obtain $\overline{A}$. An "AND" gate is used to apply the logic "AND" operation to $\overline{A}$ and B , to obtain $\overline{A} \cdot B$. Thus each signal "Div 2^r-1?" represents the result of $\overline{A} \cdot B = \overline{\sum_{j=i+1}^{n} S(j)} \bullet \prod_{j=0}^{i} S(j)$ for the corresponding *i*. For the above example, since $S_n\, S_{n-1}\, S_{n-2} \ldots S_2\, S_1\, S_0 = 001...111$,

$$\overline{\sum_{j=i+1}^{n} S(j)} \bullet \prod_{j=0}^{i} S(j) = 1 \text{ for } i = \text{n-2}. \tag{70}$$

Thus the signal "Div 2^r-1?" above "$AND_{n-2,b}$" is "1", where n-2 is i_{edge}. If $\overline{\sum_{j=i+1}^{n} S(j)} \bullet \prod_{j=0}^{i} S(j) = 1$ for any particular index $i \in [1, n-1]$, the division ratio "$S_n\ S_{n-1}\ S_{n-2}\ \ldots\ S_2\ S_1\ S_0$" should be a "$2^r - 1$" number. This particular index i will be i_{edge}, the index of the first nonzero control digit counting down from the MSB part. At the top part of Figure 24, gates "$OR_{1,b}$", …, "$OR_{n-2,b}$", "$OR_{n-1,b}$" are above the "Div 2^r-1?" signals. If any "Div 2^r-1?" signal is "1", with the logic "OR" operations, the output signal "Select solution 2?" will be "1". Thus if the division ratio "$S_n\ S_{n-1}S_{n-2}\ \ldots\ S_2\ S_1\ S_0$" is a "$2^r$-1" number, for any natural number "$r \in [1, n-1]$", the circuit will select Solution 2.

Figure 25 shows a more detailed top-level schematic of the proposed design. The "division ratio judgment circuit" used in Figure 25 at the left-bottom corner has been shown in Figure 24. If the division ratio is a "$2^r - 1$" number, the "division ratio judgment circuit" in Figure 25 will give an output "1". In this case, "Solution 2" will be used. The "n+1 bit MUX" circuit in the middle of Figure 25 will be used to select signals to assign the "$P_0P_1\ldots P_n$" controls of "Div_n_vaucher". If "Solution 2" is used, "$S_0S_1\ldots S_n$" will be selected and assigned to "$P_0P_1\ldots P_n$" of "Div_n_vaucher". If the division ratio is not a "$2^r - 1$" number, "Solution 1" will be used. The division ratio control digits "$S_0S_1\ldots S_n$" will be assigned to the inputs of the adder and the "AND" gate. The "n+1 bit MUX" circuit will select adder outputs and assign them to the "$P_0P_1\ldots P_n$" controls of "Div_n_vaucher". The "Div_n_vaucher" for the combined proposed divider is the entire circuit of "Solution 2" as shown in Figure 22 (a). The "MUX" circuit at the top of Figure 25 gives the final output by selecting "Solution 1 output" or "Solution 2 output".

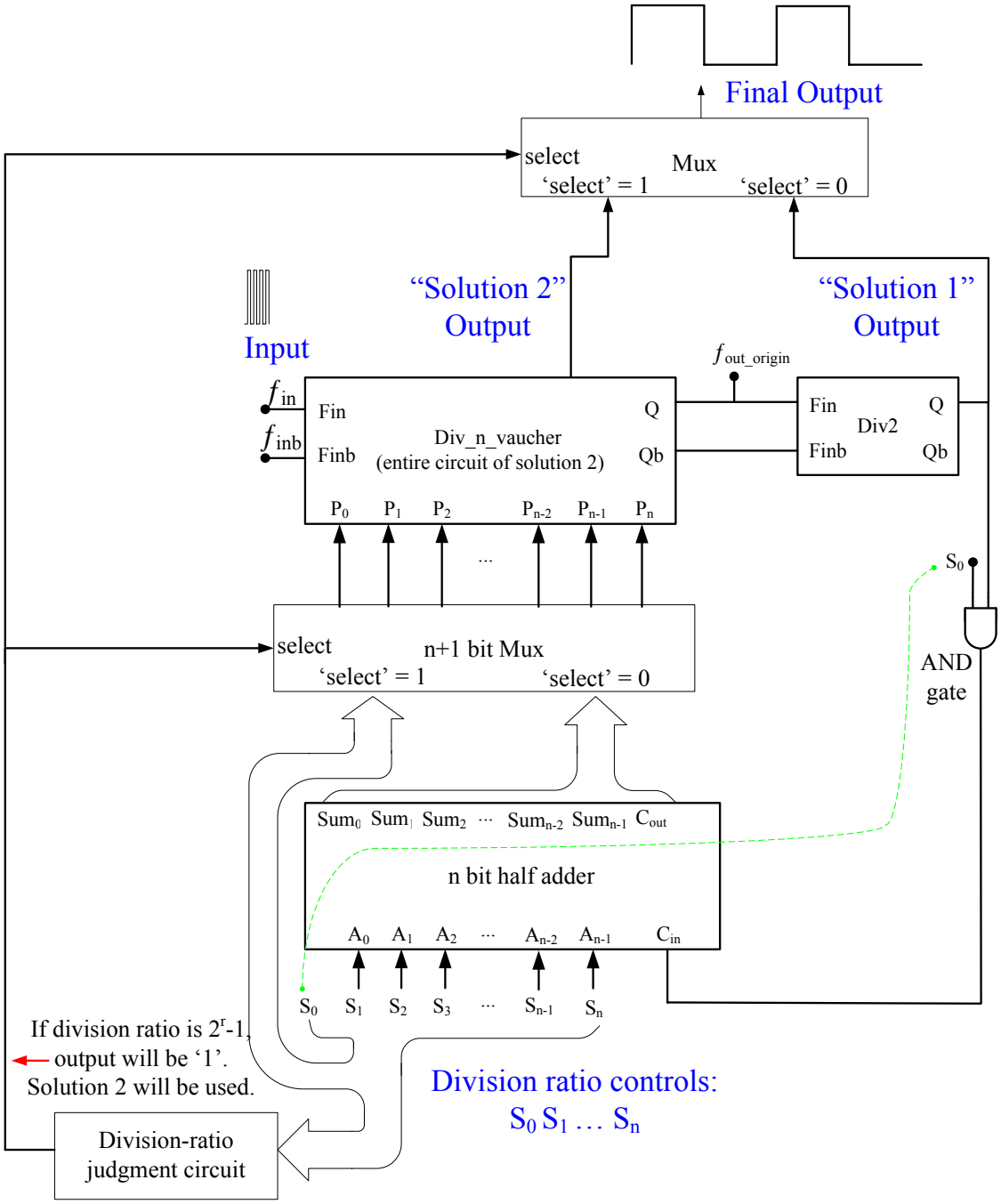


Figure 25: A more detailed schematic of the top-level proposed design.

Since all the additional circuits in the proposed design (for duty-cycle correction) operate at relatively low frequencies, they only adds less than 10% power consumption penalty to the original divider.

3.6 Simulations of the Proposed Divider

Simulations were performed for the proposed-design. They verify that the proposed programmable divider realized the division ratios shown in equation (62) and has the output duty-cycle very close to 50% as shown in equation (16). Table 2 shows the pre-layout simulation results for the comparison of *Process-Voltage-Temperature* (PVT) performance of the proposed design. When the temperature is lower or V_{DD} is higher, or with a faster process corner, the maximum operating-frequency is higher. For each division ratio, the output duty-cycle of the proposed design remains constant with various PVT, with various input frequencies, and with different chips.

3.7 Phase Noise Analysis of the Proposed Divider

A few references [35]-[36] state the noise analysis of frequency dividers. References [35] carried out the noise analysis for dividers using CMOS transistors, which is similar to the proposed divider.

Accorder to [35], for a synchronized frequency divider, the output phase noise is the accumulation of the phase noise in each “2/3 cell” stage. In each “2/3 cell” stage, the

Table 2: Performance of the proposed divider for various process-voltage-temperature

(a) The maximum operating-frequency vs. V_{DD} and Temperature, process = tt

	V_{DD} = 1.6 V	V_{DD} = 1.8 V	V_{DD} = 2 V
Temp = - 40ºC	**5.8 GHz**	**6.7 GHz**	**7.5 GHz**
Temp = 0ºC	**5.3 GHz**	**6.1 GHz**	**6.8 GHz**
Temp = 27ºC	**5.1 GHz**	**5.8 GHz**	**6.4 GHz**
Temp = 50ºC	**4.9 GHz**	**5.5 GHz**	**6.2 GHz**
Temp = 85ºC	**4.6 GHz**	**5.2 GHz**	**5.8 GHz**

(b) The maximum operating-frequency vs. process corner (0.18-µm) V_{DD}=1.8V, temperature = 27ºC

Process	f_{in}
ff	**7.4 GHz**
tt	**5.8 GHz**
ss	**4.6 GHz**

phase noise is caused by both the thermal noise and flicker noise caused by certain transistors.

The entire thermal noise can be written as the following equation, as shown in equation (10) of [35],

$$L_w = 8\pi^2 \cdot (1 + \frac{\gamma}{\alpha} + \frac{\gamma_T g_{mT} R_L}{2\alpha_T}) \cdot \frac{kTC_L}{I_B^2} \cdot f_{out} \tag{71}$$

where $\gamma \cong 1$, and $\alpha \cong 0.6$ for the input differential pair. $\gamma_T \cong 2/3$, and $\alpha_T \cong 1$ for the long-channel MOS transistor to generate the tail current. g_{mT} is the transistor transconductance, which generates the tail current. R_L is the equivalent resistance of the PMOS transistors. The PMOS transistors will operate in linear region, when their gates are connected to V_{SS}, and their drain voltages are at $V_{DD}/2$. R_L can be expressed as the following equation [37], when a PMOS transistor is operating in the linear region,

$$R_L = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{thp}|)} \tag{72}$$

k is the Boltzmann constant, which is 1.38×10^{-23} J/K. T is the absolute temperature. C_L is the load capacitor for each "2/3 cell" stage. I_B is the current flowing in each transistor is the input differential pair, when $V_{out} = \overline{V_{out}}$. f_{out} is the output frequency of the "2/3 cell" stage.

The flicker noise of the input differential NMOS pair will affect the output phase noise. The flicker noise at the offset frequency *f* can be written as the following equation, as shown in equation (13) of [35],

$$L_F(f) = 2\pi^2 f_{out}{}^2 \cdot (\frac{C_L}{I_B})^2 \cdot \frac{2K_f}{f} \quad (73)$$

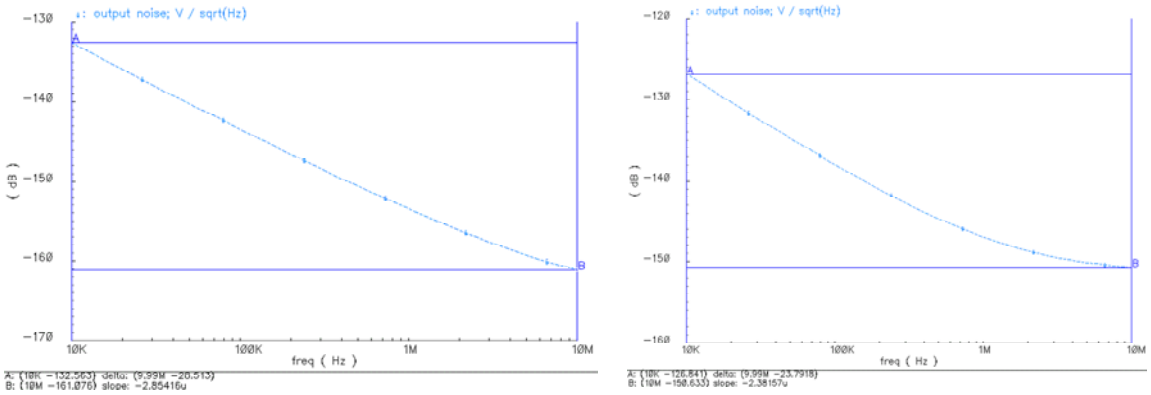
where f_{out} is the output frequency of the "2/3 cell" stage. C_L is the load capacitor for each "2/3 cell" stage. I_B is the current flowing in each transistor of the input differential pair, when $V_{out} = \overline{V_{out}}$. f is the offset frequency, the frequency difference from f_{out}. K_f is expressed in the following equation [37],

$$K_f = \frac{K}{C_{ox}WL} \quad (74)$$

In equation (74), K has a value about 10^{-25} $V^2 \cdot F$. C_{ox} is the oxide capacitance per unit area. W and L are the width and length of the corresponding transistor.

The phase noise of each "2/3 cell" stage should be the sum of equation (71) and (73). The phase noise of the entire divider should be the sum of the phase noise of each "2/3 cell" stage and the output buffers.

Some phase noise simulations are carried out for the proposed "2/3 cell" as shown in Figure 26. Figure 26 (a) is for the 1st stage, with the simulation conditions that f_{in} = 2.4 GHz, and division ratio = 3. Figure 26 (b) is for the latter "2/3 cell", with f_{in} = 100 MHz, and division ratio = 3. At 10 kHz offset from the output frequency, the phase noise of the 1st stage "2/3 cell" is -132.563 dB. At 10 kHz offset from the output frequency, the phase noise of the slow "2/3 cell" is -126.841 dB. It can be seen that the phase noise of the slow "2/3 cell" is higher than the 1st stage "2/3 cell".



A (10 kHz, -132.563 dB)
B (10 MHz, -161.076 dB)

(a)

A (10 kHz, -126.841 dB)
B (10 MHz, -150.633 dB)

(b)

Figure 26: Phase noise simulation of the proposed "2/3 cell": (a) 1st stage, f_{in} = 2.4 GHz, division ratio = 3, (b) the slow "2/3 cell", f_{in} = 100 MHz, division ratio = 3.

3.8 Three Copies of the Proposed Programmable Divider

The chip includes three copies of the proposed divider to test the divider with both high and low input frequencies. The input signal (f_{in}) of the first copy will be connected to a high frequency signal generator (Agilent E8257D PSG Analog Signal Generator) to test GHz range signals. The high-frequency input signals will be amplified by several buffer cells shown in Figure 27 (a). In Figure 27 (a), C_1 and C_2 high pass the input signals and apply the signals to the differential pair M_2 and M_3. M_6, M_7 and M_8, M_9 are used to generate input biasing voltage for the differential pair. The optimum biasing voltage and C_1, C_2 values are obtained through simulation to achieve the largest amplification, when several buffer cells are connected in series. The buffer cells can only amplify high frequency signals (higher than about 500 MHz). The signal generator can only generate

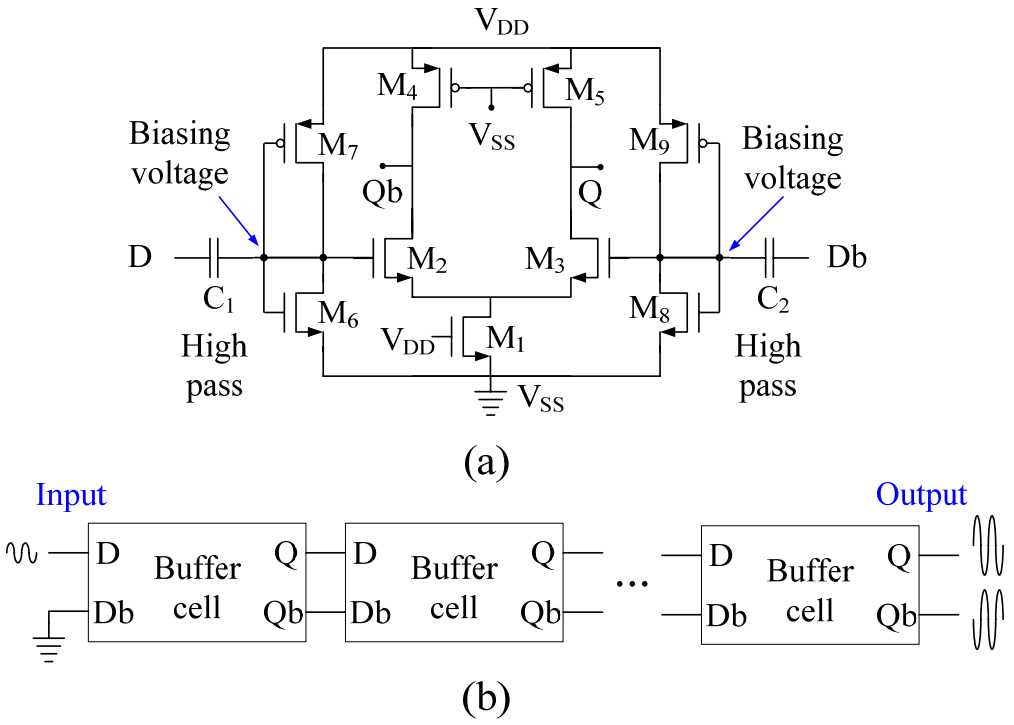


Figure 27: Schematic of the high frequency buffer: (a) one differential cell, (b) several cells to convert a single-ended signal to differential output signals.

single-ended signals, but the proposed divider needs differential inputs. As shown in Figure 27 (b), several cascade buffers with one input connected to 0V can convert the single-ended input signal to differential output signals.

The input signal (f_{in}) of the second copy is coming from an on-chip ring-VCO. This input signal will also be amplified by several high-frequency buffer stages. The input signal (f_{in}) of the third copy will be connected to a low frequency signal generator (Tektronix AFG3102 Dual Channel Arbitrary/Function Generator), which generates 50MHz - kHz range signals. Several inverters are used to generate differential signals from the third input signals, which is a single-ended signal.

Chapter 4
Measurements of the Proposed Programmable Divider

4.1 Photographs of the Fabricated Chip and the Test Board

The chip was fabricated using a 0.18-μm RF CMOS process. Figure 28 shows the photograph of the fabricated chip. The chip includes three copies of the proposed divider to test the divider with both high and low input frequencies. Each copy consumes an area of about 0.1 mm^2. A RF (radio frequency) PCB (printed circuit board) is designed to test the proposed divider and a fractional PLL including the proposed divider. The PLL occupies and area of about 0.8 mm^2 and it will be discussed in more details later.

Figure 29 shows the photograph of the PCB, which is a 4-layer board. Compared with a 2-layer PCB design, a 4-layer board has the following advantages. With the same total thickness of all the layers, the distance between two nearby layers will be greatly reduced. With a smaller distance between two layers, the 50 Ω transmission line drawn on the board will have much smaller width. This is very helpful to layout the PCB compactly.

4.2 Test Results of the Proposed Divider

The proposed programmable frequency-divider is tested using an oscilloscope to check the output duty-cycle for both high frequency and low frequency input signals. Close-to-50% output signals are obtained.

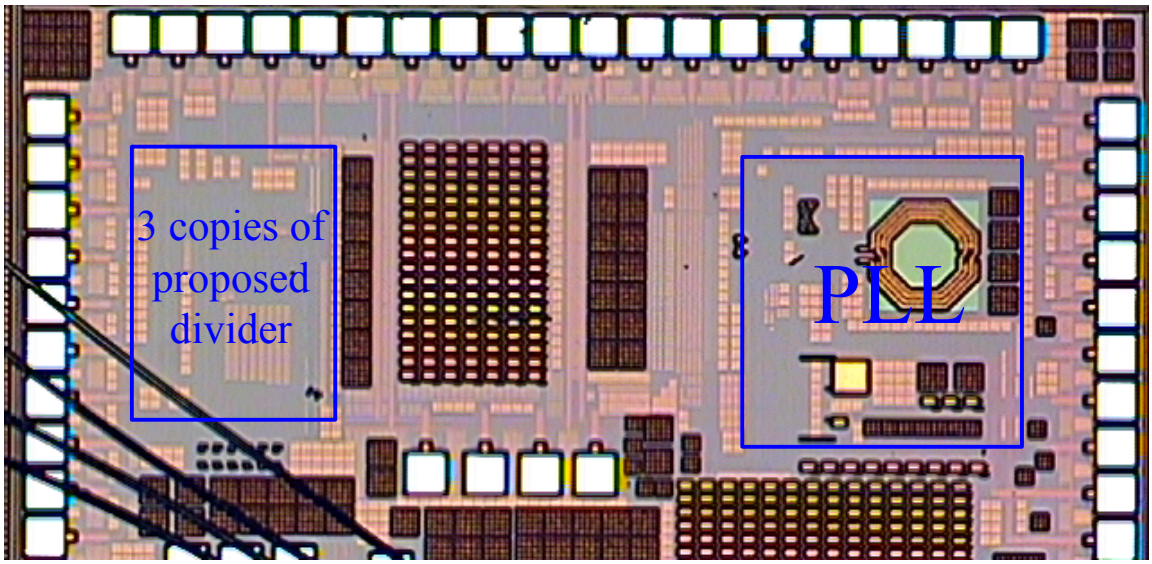


Figure 28: Photograph of the proposed programmable divider after fabrication.

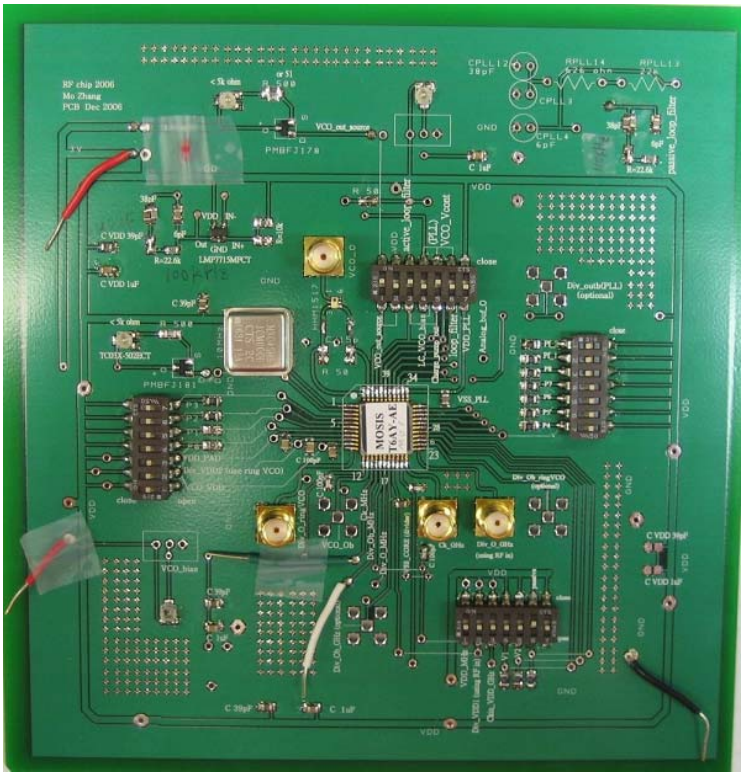
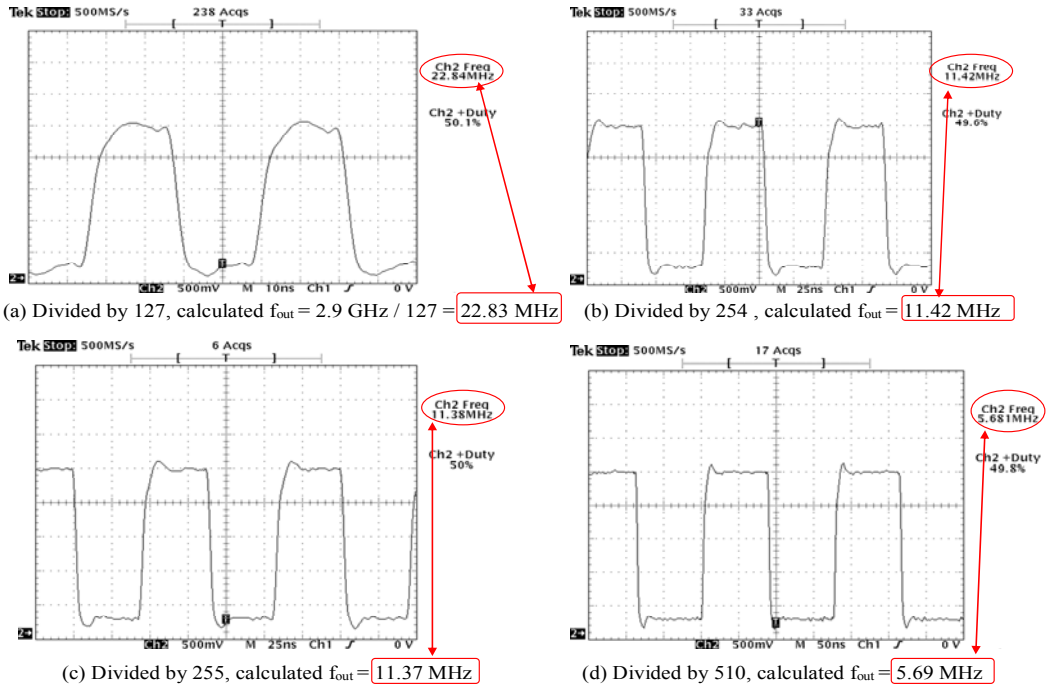


Figure 29: PCB test board for the proposed programmable frequency divider.

Figure 30 shows the transient test results of the proposed design with a 2.9 GHz input signal with different division ratios. A Tektronix TDS 340A digital real-time oscilloscope with 100MHz BW is used for the measurements. The division ratios include "2r – 1" numbers ((a) 127 (c) 255), and other numbers ((b) 254 (d) 510). For simplicity, transient measurements with other division ratios are not shown here. Since the bandwidth of the oscilloscope is limited, it is hard to view the waveform for small division ratios. In Figure 30 it can be seen that for each division ratio, the output duty-cycle is very close to 50%. Figure 31 shows the output spectra for more division ratios (a) 8 (b) 15 (c) 62 (d) 240. An Agilent E4407B spectra analyzer is used for the spectra measurements.

Figure 32 shows the transient test results of the proposed design with a 500 MHz input signal and with different division ratios. The division ratios include "2^r – 1" numbers ((a) 15), and other numbers ((b) 16 (c) 251 (d) 509). Figure 33 shows the transient test results of the proposed design with a 10 MHz input signal with different division ratios (a) 8 (b) 29 (c) 59 (d) 123. Figure 34 shows the transient test results of the proposed design with a 1 kHz input signal with different division ratios (a) 11 (b) 15 (c) 31 (d) 67. The output duty-cycle in each figure is close to 50% as expected. Table 3 - Table 10 shows the comparison of calculated and measured results of the proposed divider, when the input frequencies are 2.9GHz, 500MHz, 50MHz, 10MHz, 1MHz, 100kHz, 10 kHz and 1kHz. The comparisons are about the output frequency and the output duty-cycle. The calculation of the output duty-cycle is based on equation (16). Since the bandwidth of the oscilloscope (Tektronix TDS 340A) is limited (about 100 MHz), when the output



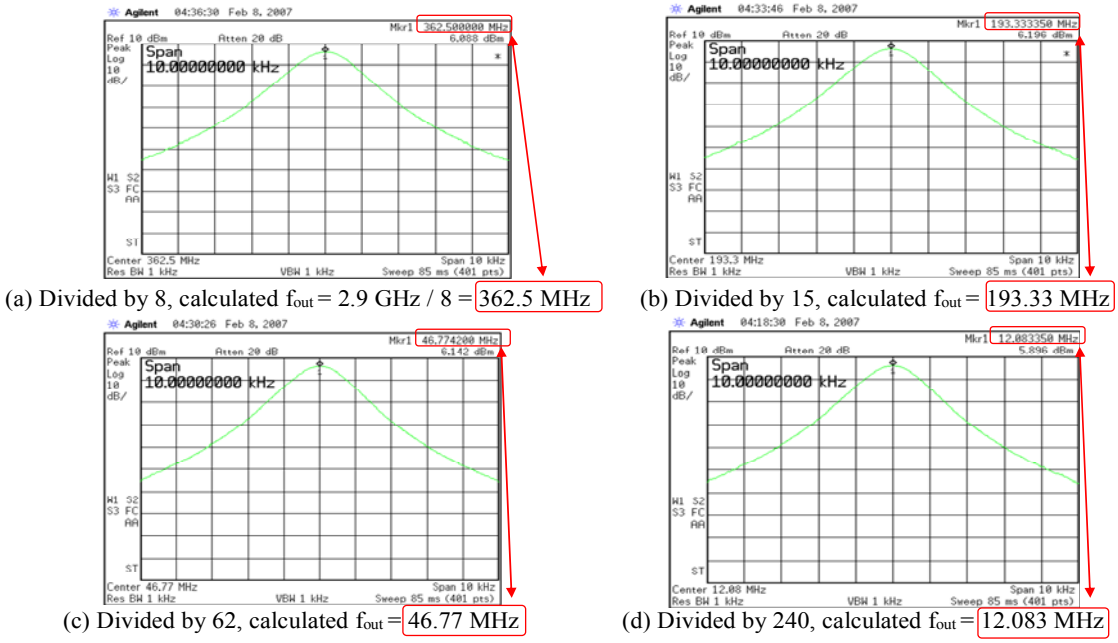
(a) Divided by 127, calculated f_{out} = 2.9 GHz / 127 = 22.83 MHz

(b) Divided by 254 , calculated f_{out} = 11.42 MHz

(c) Divided by 255, calculated f_{out} = 11.37 MHz

(d) Divided by 510, calculated f_{out} = 5.69 MHz

Figure 30: Transient test results of the proposed design with a 2.9GHz input signal with division ratios: (a) 127, (b) 254, (c) 255, and (d) 510.



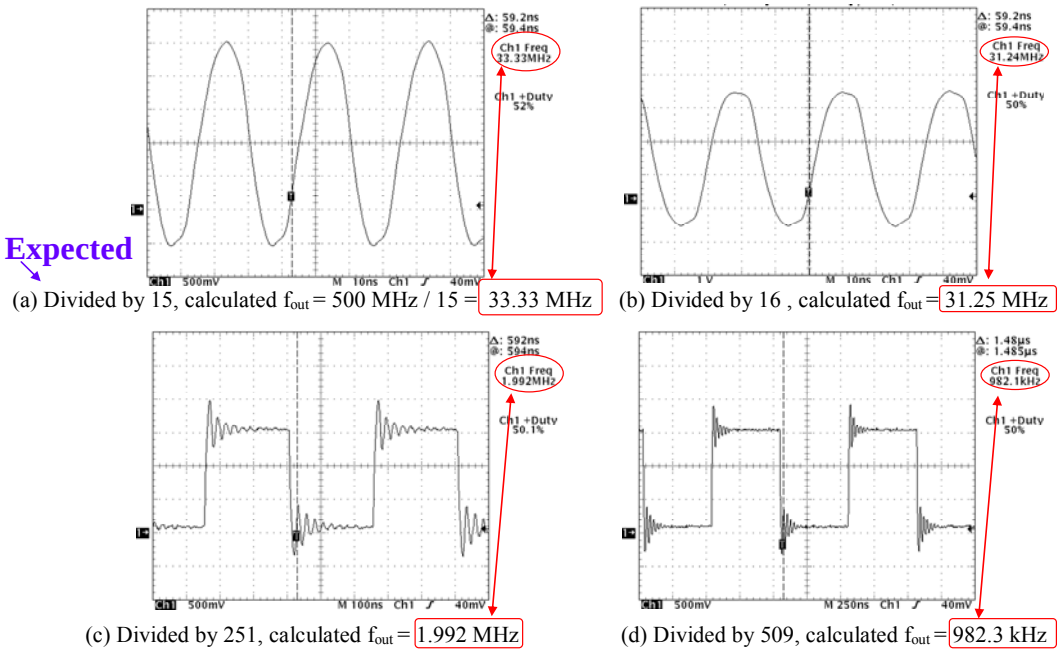
(a) Divided by 8, calculated f_{out} = 2.9 GHz / 8 = 362.5 MHz

(b) Divided by 15, calculated f_{out} = 193.33 MHz

(c) Divided by 62, calculated f_{out} = 46.77 MHz

(d) Divided by 240, calculated f_{out} = 12.083 MHz

Figure 31: Output spectra of the proposed design with a 2.9GHz input signal with division ratios: (a) 8, (b) 15, (c) 62, and (d) 240.



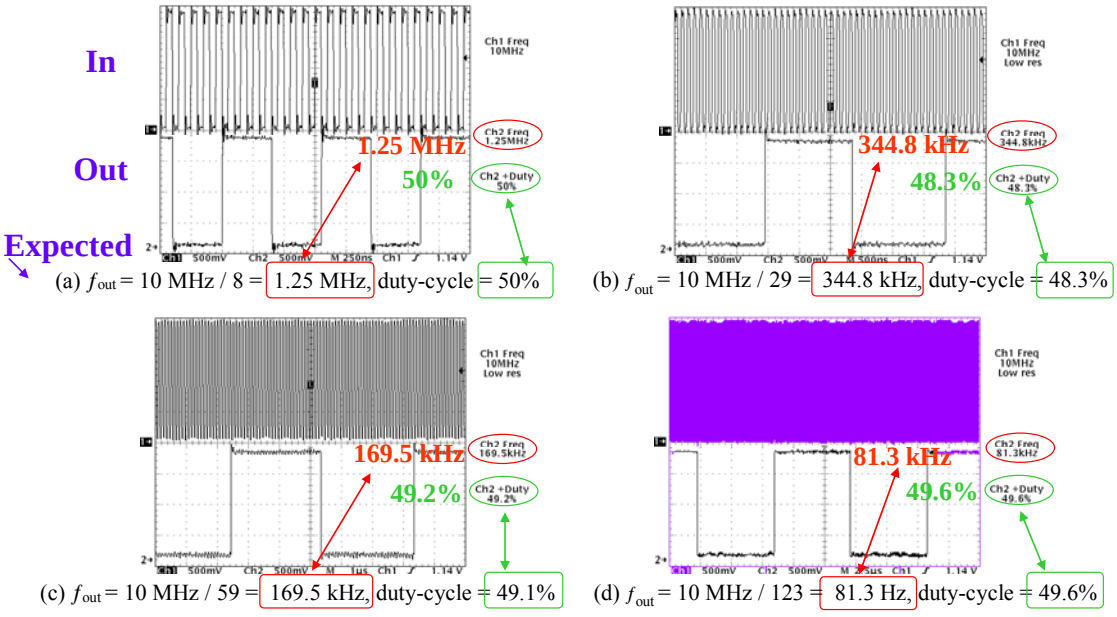
(a) Divided by 15, calculated f_{out} = 500 MHz / 15 = 33.33 MHz

(b) Divided by 16 , calculated f_{out} = 31.25 MHz

(c) Divided by 251, calculated f_{out} = 1.992 MHz

(d) Divided by 509, calculated f_{out} = 982.3 kHz

Figure 32: Transient test results of the proposed design with a 500 MHz input signal with division ratios: (a) 15, (b) 16, (c) 251, and (d) 509.



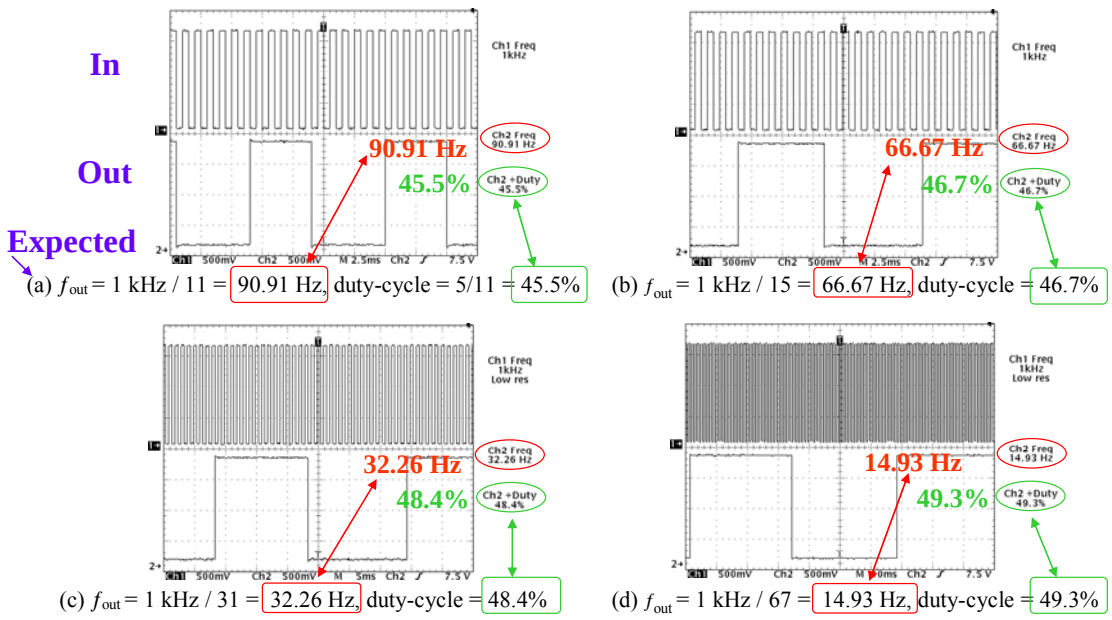
(a) f_{out} = 10 MHz / 8 = 1.25 MHz, duty-cycle = 50%

(b) f_{out} = 10 MHz / 29 = 344.8 kHz, duty-cycle = 48.3%

(c) f_{out} = 10 MHz / 59 = 169.5 kHz, duty-cycle = 49.1%

(d) f_{out} = 10 MHz / 123 = 81.3 Hz, duty-cycle = 49.6%

Figure 33: Transient test results of the proposed design with a 10 MHz input signal with division ratios: (a) 8, (b) 29, (c) 59, and (d) 123.



(a) f_{out} = 1 kHz / 11 = 90.91 Hz, duty-cycle = 5/11 = 45.5%

(b) f_{out} = 1 kHz / 15 = 66.67 Hz, duty-cycle = 46.7%

(c) f_{out} = 1 kHz / 31 = 32.26 Hz, duty-cycle = 48.4%

(d) f_{out} = 1 kHz / 67 = 14.93 Hz, duty-cycle = 49.3%

Figure 34: Transient test results of the proposed design with a 1 kHz input signal with division ratios: (a) 11, (b) 15, (c) 31, and (d) 67.

Table 3: Comparison of the calculated and the measured results of the proposed divider for the input frequency of 2.9 GHz.

Division ratio	Calculated f_{out} (MHz)	Measured f_{out} (MHz)	Calculated output duty-cycle	Measured output duty-cycle
127	22.83	22.81	49.6%	49.8%
240	12.08	12.08	50.0%	49.5%
252	11.51	11.51	50.0%	49.5%
253	11.46	11.46	49.8%	49.7%
254	11.42	11.42	50.0%	49.6%
255	11.37	11.38	49.8%	50.0%
510	5.686	5.681	50.0%	49.8%

Table 4: Comparison of the calculated and the measured results of the proposed divider for the input frequency of 500 MHz.

Division ratio	Calculated f_{out} (MHz)	Measured f_{out} (MHz)	Calculated output duty-cycle	Measured output duty-cycle
15	33.33	33.33	46.7%	48.0%
16	31.25	31.24	50.0%	50.0%
17	29.41	29.42	47.1%	49.3%
31	16.13	16.13	48.4%	46.9%
61	8.197	8.196	49.2%	50.0%
63	7.937	7.936	49.2%	49.4%
125	4	4	49.6%	49.8%
251	1.992	1.992	49.8%	49.9%
509	0.9823	0.9821	49.9%	50.0%
510	0.9804	0.9804	50.0%	49.9%

Table 5: Comparison of the calculated and the measured results of the proposed divider for the input frequency of 50 MHz.

Division ratio	Calculated f_{out} (MHz)	Measured f_{out} (MHz)	Calculated output duty-cycle	Measured output duty-cycle
8	6.25	6.251	50.0%	49.9%
9	5.556	5.555	44.4%	44.1%
11	4.545	4.544	45.5%	45.3%
15	3.333	3.333	46.7%	46.7%
31	1.613	1.613	48.4%	48.3%
61	0.8197	0.8197	49.2%	49.2%
125	0.4	0.4	49.6%	49.6%
127	0.3937	0.3937	49.6%	49.6%
251	0.1992	0.1992	49.8%	49.8%
255	0.1961	0.1961	49.8%	49.8%
509	0.09823	0.09824	49.9%	49.9%

Table 6: Comparison of the calculated and the measured results of the proposed divider for the input frequency of 10 MHz.

Division ratio	Calculated f_{out} (kHz)	Measured f_{out} (kHz)	Calculated output duty-cycle	Measured output duty-cycle
8	1250	1250	50.0%	50.0%
9	1111.1	1111.1	44.4%	44.4%
13	769.2	769/2	46.1%	46.2%
15	666.7	666.7	46.6%	46.6%
29	344.8	344.8	48.3%	48.3%
31	322.6	322.6	48.3%	48.3%
45	222.2	222.2	48.9%	48.9%
59	169.5	169.5	49.1%	49.2%
111	90.09	90.09	49.5%	49.5%
123	81.3	81.3	49.6%	49.6%

Table 7: Comparison of the calculated and the measured results of the proposed divider for the input frequency of 1 MHz.

Division ratio	Calculated f_{out} (kHz)	Measured f_{out} (kHz)	Calculated output duty-cycle	Measured output duty-cycle
9	111.1	111.1	44.4%	44.4%
15	66.67	66.67	46.7%	46.7%
17	58.82	58.82	47.1%	47.1%
25	40	40	48.0%	48.0%
31	32.26	32.26	48.4%	48.4%
33	30.3	30.3	48.5%	48.5%
41	24.39	24.39	48.8%	48.8%
60	16.67	16.67	50.0%	50.0%
63	15.87	15.87	49.2%	49.2%
71	14.08	14.08	49.3%	49.3%

Table 8: Comparison of the calculated and the measured results of the proposed divider for the input frequency of 100 kHz.

Division ratio	Calculated f_{out} (kHz)	Measured f_{out} (kHz)	Calculated output duty-cycle	Measured output duty-cycle
9	11.11	11.11	44.4%	44.4%
12	8.333	8.333	50.0%	50.0%
15	6.667	6.667	46.7%	46.7%
21	4.762	4.762	47.6%	47.6%
27	3.704	3.704	48.1%	48.1%
31	3.226	3.226	48.4%	48.4%
47	2.128	2.128	48.9%	48.9%
57	1.754	1.754	49.1%	49.1%
63	1.587	1.587	49.2%	49.2%
125	0.8	0.8	49.6%	49.6%

Table 9: Comparison of the calculated and the measured results of the proposed divider for the input frequency of 10 kHz.

Division ratio	Calculated f_{out} (Hz)	Measured f_{out} (Hz)	Calculated output duty-cycle	Measured output duty-cycle
10	1000	1000	50.0%	50.0%
15	666.7	666.7	46.7%	46.7%
17	588.2	588.2	47.1%	47.1%
19	526.3	526.3	47.4%	47.4%
24	416.7	416.7	50.0%	50.0%
25	400	400	48.0%	48.0%
33	303	303	48.5%	48.5%
55	181.8	181.8	49.1%	49.1%
65	153.8	153.8	49.2%	49.2%
127	78.74	78.74	49.6%	49.6%

Table 10: Comparison of the calculated and the measured results of the proposed divider for the input frequency of 1 kHz.

Division ratio	Calculated f_{out} (Hz)	Measured f_{out} (Hz)	Calculated output duty-cycle	Measured output duty-cycle
11	90.91	90.91	45.5%	45.5%
15	66.67	66.67	46.7%	46.7%
20	50	50	50.0%	50.0%
31	32.26	32.26	48.4%	48.4%
35	28.57	28.57	48.6%	48.6%
39	25.64	25.64	49.7%	48.7%
63	15.87	15.87	49.2%	49.2%
67	14.93	14.93	49.3%	49.3%
81	12.35	12.35	49.4%	49.4%
121	8.264	8.264	49.6%	49.6%

frequency is in the tens of MHz range, the frequency and the output duty-cycle test results are not very accurate. When the output frequency is lower, such as in kHz or Hz range, the measured results are almost the same as the calculated results.

A number of testing involving temperature, power supply voltage, input signal power and phase noise are also carried out. Figure 35 shows the maximum operating (input) frequency vs. temperature for two chips. For the test related to temperature, the on-chip ring VCO is used as the input source, and with a power supply voltage of 1.8V. When the temperature increases, the maximum (highest) operating frequency will be decreased. Figure 36 shows the relationship between the highest operating-frequency and the power-supply voltage V_{DD} for two chips. If the V_{DD} increases, the programmable frequency-divider can operate at higher frequencies. Figure 37 shows the lowest necessary input power vs. the operating frequencies for two chips. When the operating frequency is lower, the divider will be able to operate correctly with smaller power of the input signal.

Figure 38 shows the phase noise measurement of the proposed. Figure 38 (a) shows the input phase noise of the divider. The input signal is a 2.4 GHz signal generated by a signal generator. Figure 38 (b) shows the output phase noise of the proposed divider with the 2.4 GHz input signal generated by the signal generator, and with a division ratio of 240. If Figure 38(a) and (b) are compared, it can be seen that the two phase noise figure has almost the same results. Thus the proposed divider almost adds no phase noise to the circuit.

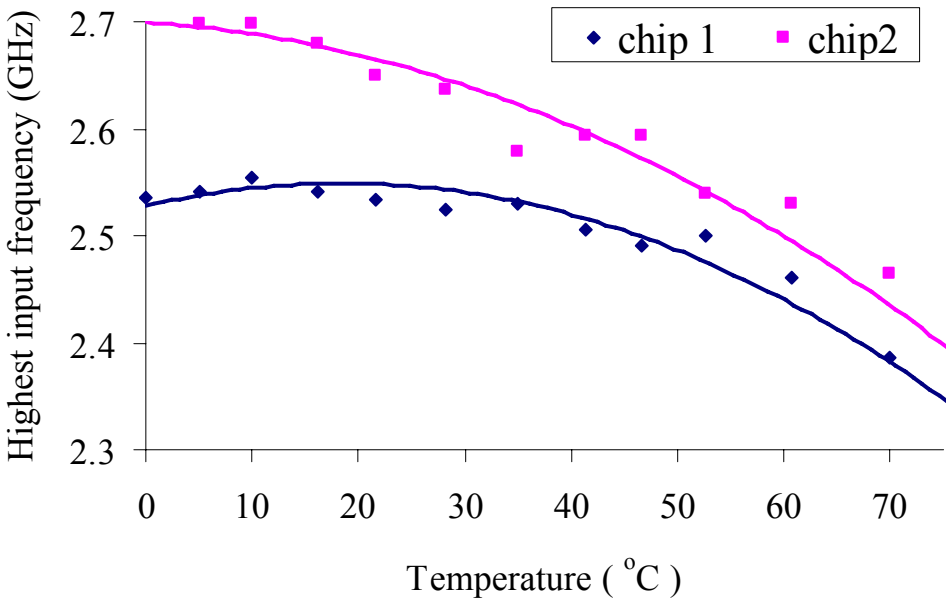


Figure 35: Maximum operating (input) frequency vs. temperature.

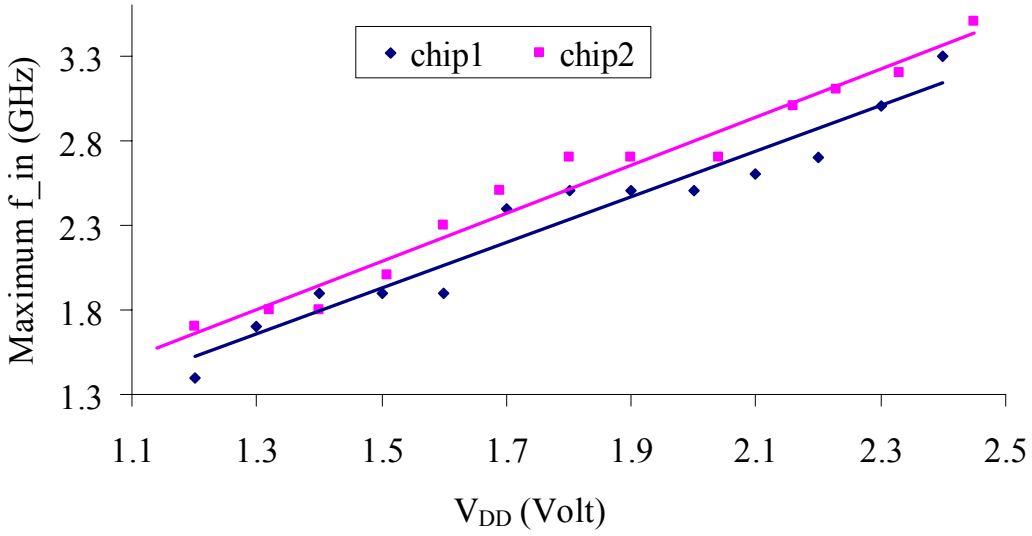


Figure 36: The highest operating (input) frequency vs. V_{DD} for two chips. The dots are the experimental results. The lines are the best-fitting lines.

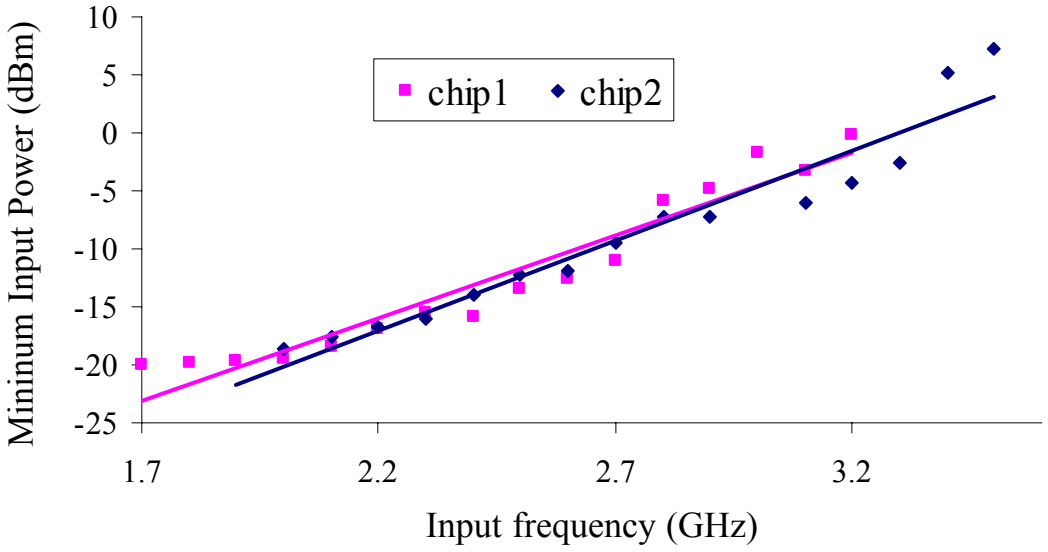
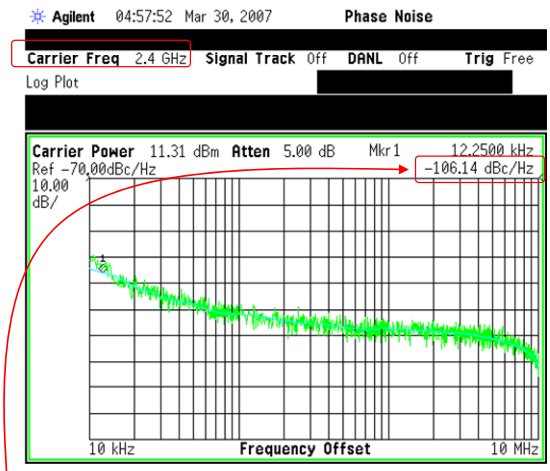
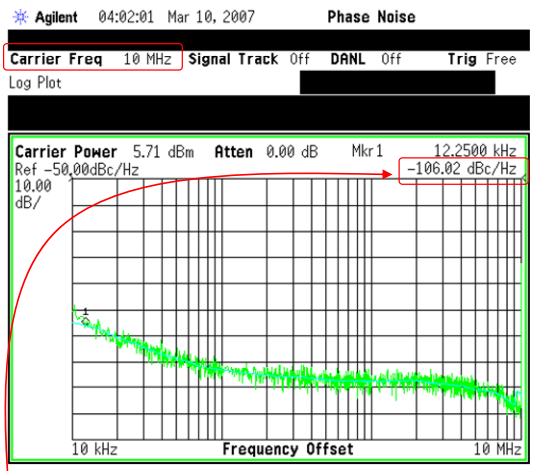


Figure 37: The lowest necessary input power vs. operating frequencies. The dots are the experimental results. The lines are the best-fitting lines.



(a) Input phase noise
2.4 GHz from the signal generator
-106 dBc/Hz @ 12.25 kHz offset frequency



(b) Output phase noise
2.4GHz / 240 = 10 MHz
-106 dBc/Hz @ 12.25 kHz offset frequency

Figure 38: The phase noise of the proposed divider: (a) input phase noise of the 2.4 GHz signal generated by the signal generator, and (b) output phase noise of the divider, 2.4 GHz / 240 = 10 MHz.

Figure 39 shows the eye diagram measurement [38] of the proposed divider. An Agilent 54624A Oscilloscope is used for the measurement. The on-chip ring VCO is used as the input of the proposed divider, whose output frequency is set to 2.04 GHz. The division ratio of the divider is set to 127. Figure 39 (a) shows that the zero-crossing jitter of edge 1 = 5.6 ns, and ISI (inter-symbol interference) = 266 mV. Figure 39 (b) shows that zero-crossing jitter of edge 2 = 6 ns, and noise margin = 797 mV.

Tests are carried out to check if the proposed divider could change the corner frequency of a SCF. A low pass switched-capacitor filter, MAX7413, is used for the test. The clock signal of the SCF is generated by the proposed divider. The on-chip ring VCO is used as the input of the proposed divider. The output frequency of the VCO is set to about 398 MHz. Figure 40 and Figure 41 show some transient test results of the SCF when the division ratio of the proposed divider is set to 255 and 510 respectively. Channel 1 shows the input signal, and channel 2 shows the output signal. Since the SCF is a low pass filter, when the input frequency is higher, the peak-peak amplitude of the output signal is smaller. For each input frequency, $V_{out,\ p\text{-}p}$ / $V_{in,\ p\text{-}p}$ is calculated to evaluate the transfer function of the SCF in frequency domain. Figure 42 shows the measurements of the transfer functions of the SCF. The blue dots in Figure 42 show the test results when the division ratio of the proposed divider is 255. In this case, the output frequency of the divider or the clock frequency of the SCF will be 1.56 MHz. The corner frequency of the SCF (-3DB frequency of the low pass filter) is about 23 kHz. The pink dots in Figure 42 show the test results when the division ratio is doubled, or 510. In this case, the clock frequency of the SCF is reduced to 780 kHz. The -3DB frequency of the SCF is about

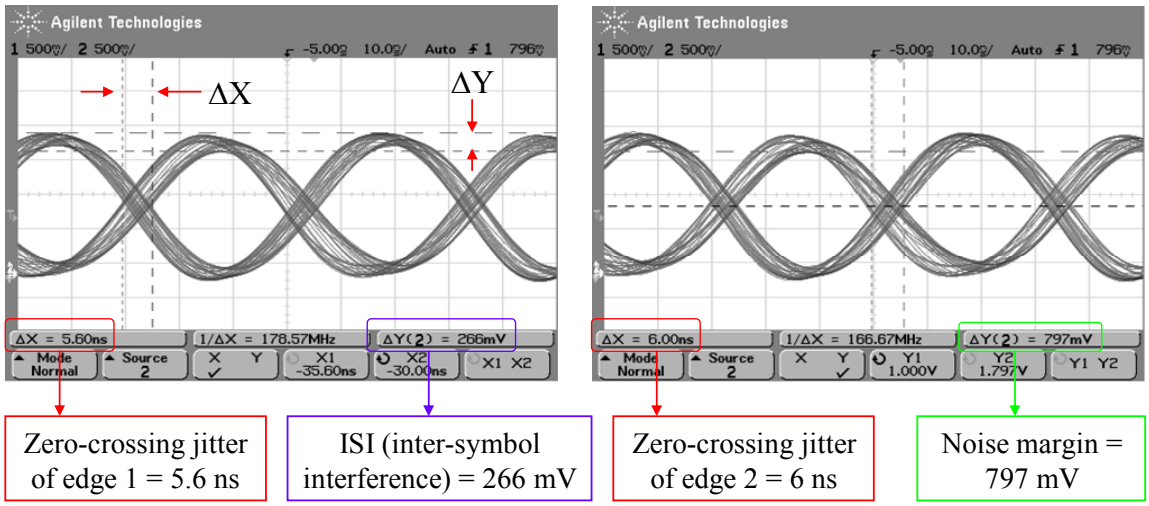
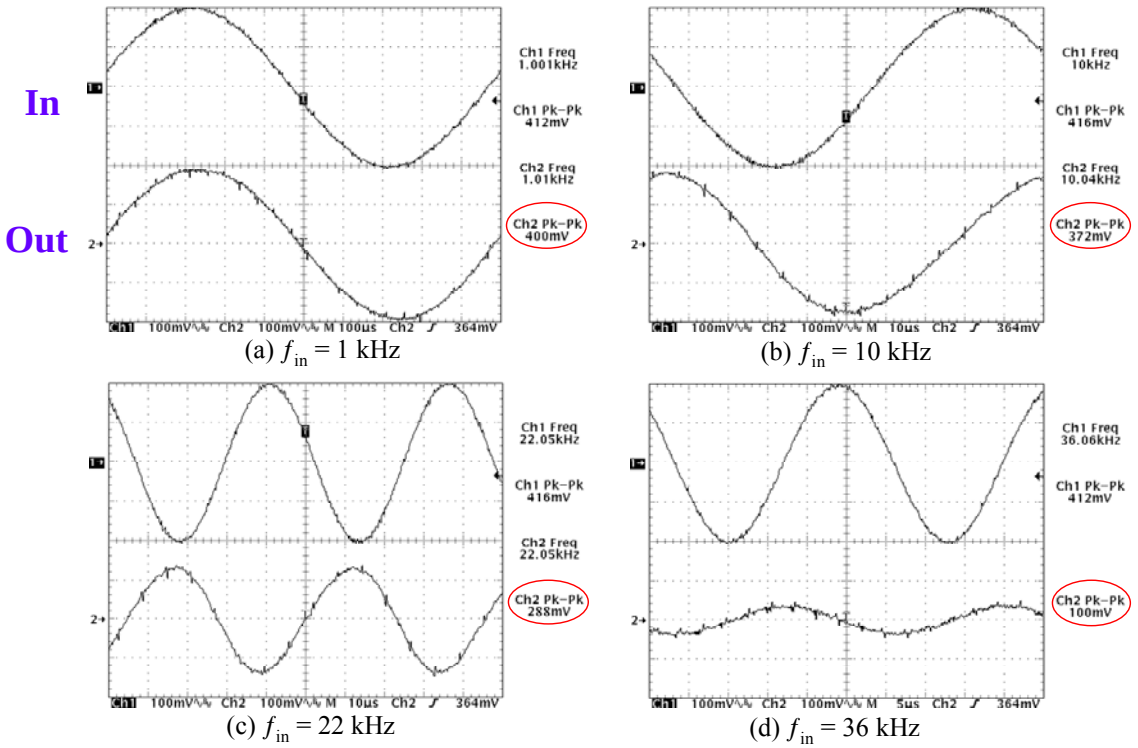


Figure 39: The eye diagram measurement of the proposed divider: (a) zero-crossing jitter of edge 1 = 5.6 ns, and ISI = 266 mV (b) zero-crossing jitter of edge 2 = 6 ns, and noise margin = 797 mV.



(a) f_{in} = 1 kHz (b) f_{in} = 10 kHz

(c) f_{in} = 22 kHz (d) f_{in} = 36 kHz

Figure 40: Measurements of the proposed divider (division ratio is 255) used as the clock signal for a SCF (MAX7413). The input frequencies of the filter are: (a) 1 kHz, (b) 10 kHz, (c) 22 kHz, and (d) 36 kHz.

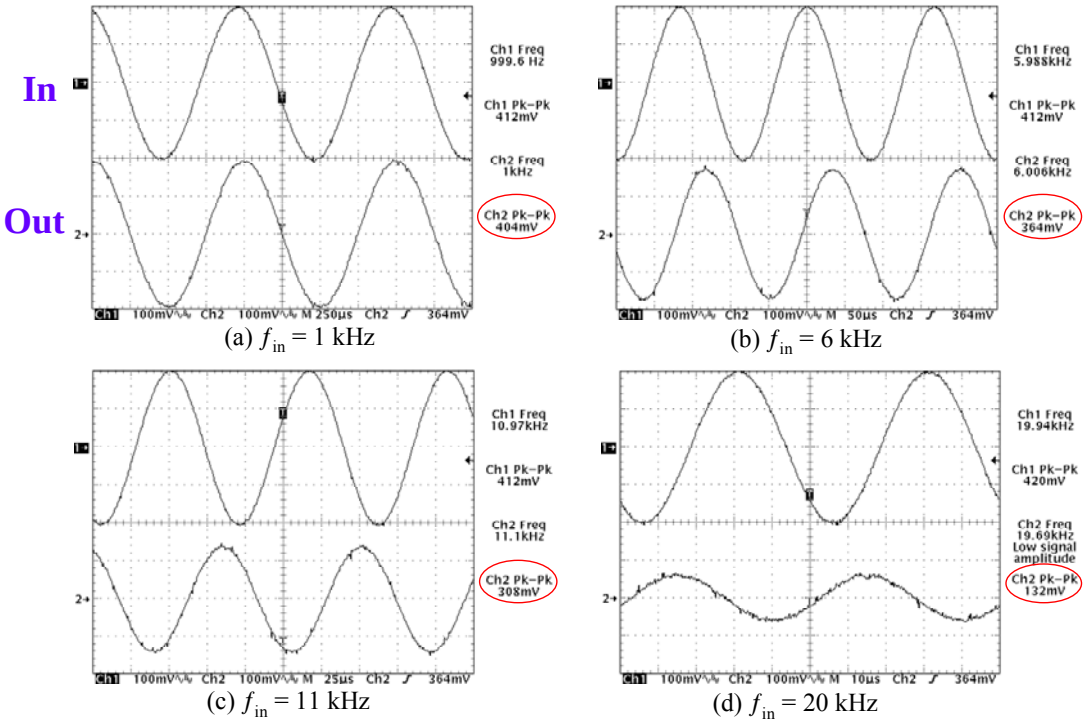


Figure 41: Measurements of the proposed divider (division ratio is 510) used as the clock signal for a SCF (MAX7413). The input frequencies of the filter are: (a) 1 kHz, (b) 6 kHz, (c) 11 kHz, and (d) 20 kHz.

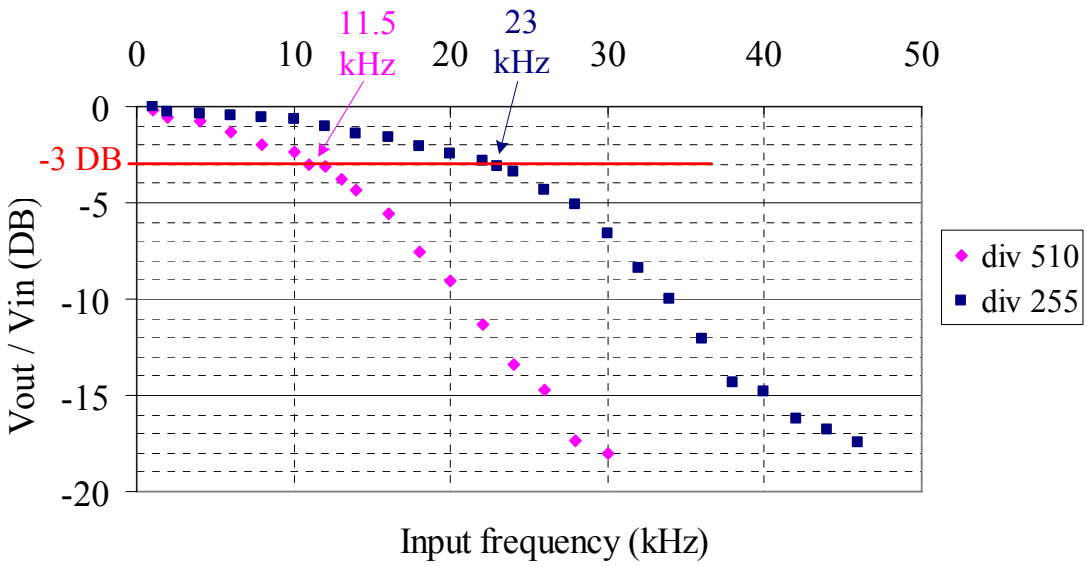


Figure 42: Measurements of the proposed divider with a SCF.

11.5 kHz. From the test results, the following equation could be obtained,

$$\frac{23\text{kHz}}{11.5\text{kHz}} = \frac{1.56\text{MHz}}{780\text{kHz}} = \frac{510}{255} \tag{75}$$

Equation (75) verifies the relationship shown in equation (19). Thus the corner frequency of the SCF is proportional to f_{clk}, which is reversely proportional to the division ratio of the divider.

In general, the test results of the fabricated circuit verify the effectiveness of the proposed programmable divider. It can generate very close-to-50% output duty-cycle, and with a wide division ratio range for a very wide frequency range (GHz down to kHz). The phase noise caused by the proposed divider is also very small.

Chapter 5
A Fractional Programmable PLL

5.1 Introduction of the Programmable PLL

PLL (Phase Locked Loop) is widely used in telecommunications and computers. It can generate high frequency signals with small phase errors for radio receivers, mobile telephones, GPS systems and computer CPUs. A programmable PLL can generate a range of frequencies from a fixed oscillator. It is more useful since there are more output frequency options.

Figure 43 [39]-[40] shows the block diagram of a typical programmable PLL. A programmable PLL includes the following building block: "Reference Frequency", "PFD (Phase/Frequency Detector) & Charge Pump", "Loop Filter", "VCO (Voltage-Controlled Oscillator)", and "Programmable Frequency Divider".

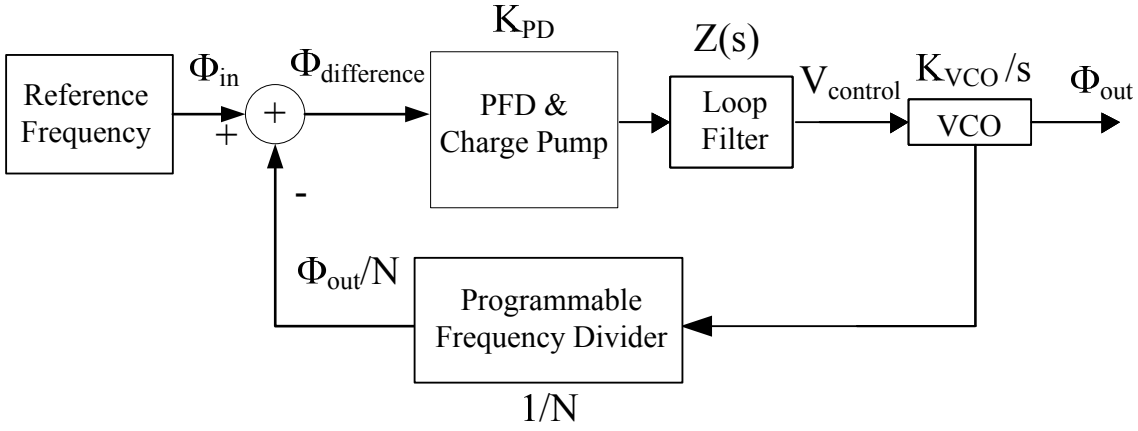


Figure 43: The block diagram of a programmable PLL.

In the following statements, all of the phase Φ is the change compared to the initial Φ_0 value. Normally the reference frequency comes from a high quality crystal oscillator. The programmable divider divides the VCO output phase (Φ_{out}) by N. The "PFD & Charge Pump" will detect $\Phi_{difference}$, the difference between Φ_{in} and "Φ_{out} / N". It will generate an output current $K_{PD} \times \Phi_{difference}$. The current will charge or discharge the loop filter and generate a $V_{control}$, which is equal to $K_{PD} \times \Phi_{difference} \times Z(s)$. Z(s) is the equivalent impedance of the loop filter. The output phase (Φ_{out}) of the VCO is $V_{control} \times K_{VCO} / s$. In reality,

$$\phi(t) = 2\pi \int f\,dt = 2\pi f \cdot t \tag{76}$$

Figure 44 shows a detailed schematic of a programmable PLL. It includes a second order loop filter. The following equations could be obtained.

The impedance of the Loop Filter Z(s) is,

$$Z(s) = \frac{(R_1 + \frac{1}{sC_1}) \cdot \frac{1}{sC_2}}{R_1 + \frac{1}{sC_1} + \frac{1}{sC_2}} = \frac{R_p C_P s + 1}{s(C_p + C_2 + sC_p C_2 R_P)} \tag{77}$$

The open loop gain is,

$$H(s)_{open} = \frac{I_P}{2\pi} \cdot \frac{R_1 C_1 s + 1}{s(C_1 + C_2 + sC_1 C_2 R_1)} \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N} \tag{78}$$

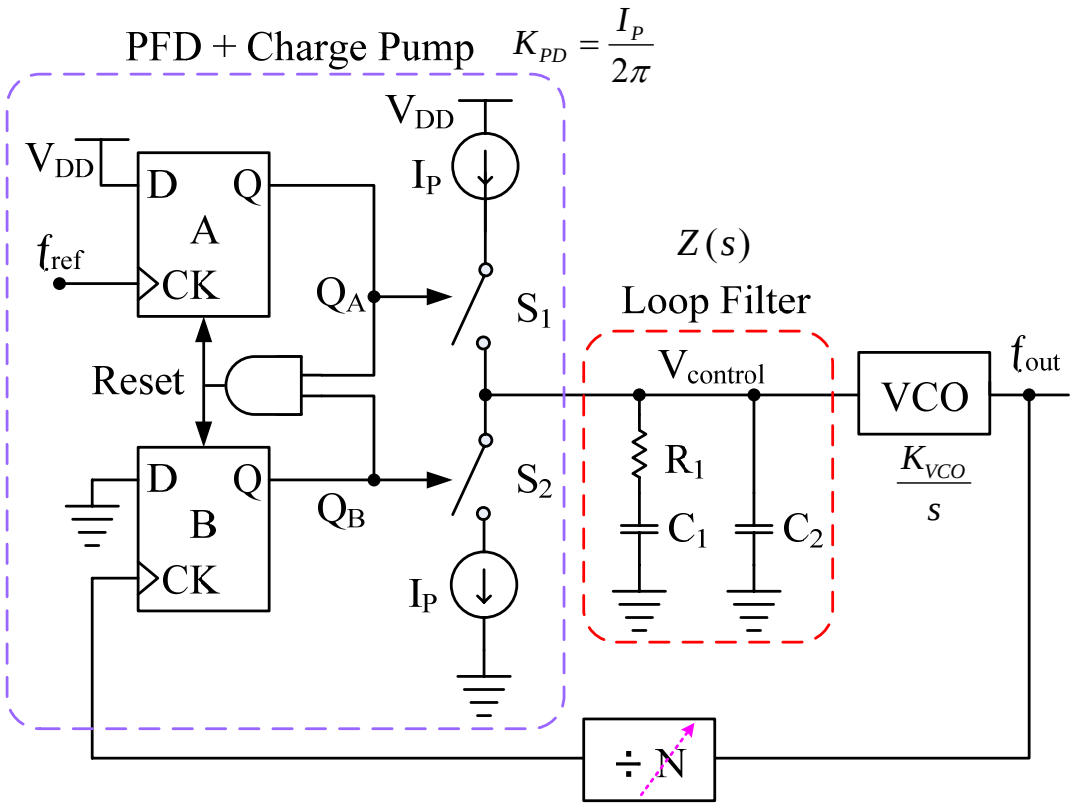
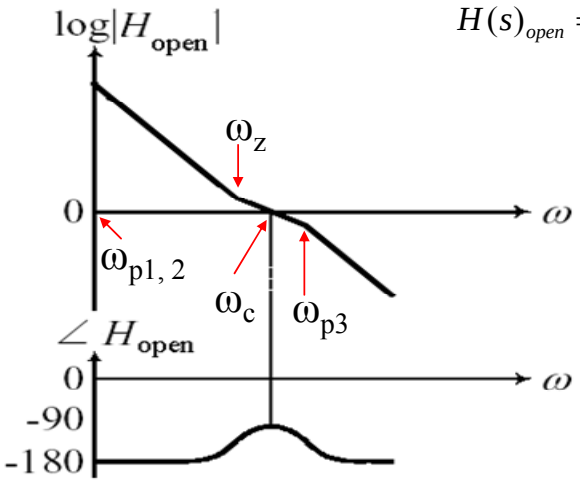


Figure 44: More detailed schematic of a programmable PLL.



$$H(s)_{open} = \frac{I_P}{2\pi} \cdot \frac{R_1 C_1 s + 1}{s(C_1 + C_2 + sC_1 C_2 R_1)} \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N}$$

$$\omega_{p1} = \omega_{p2} = 0$$

$$\omega_z = \frac{1}{R_1 C_1}$$

$$\omega_{p3} = \frac{C_1 + C_2}{C_1 C_2 R_1} = \frac{1}{\frac{C_1 C_2}{C_1 + C_2} R_1} = \frac{1}{C_{1,2series} R_1}$$

$$\omega_c \; is \; the \; |s| \; value, when \; |H(s)_{open}| = 1$$

Figure 45: The bode plot of a programmable PLL.

$$H(s)_{open} = A \cdot \frac{s - \omega_z}{(s - \omega_{p1})(s - \omega_{p2})(s - \omega_{p3})} \tag{79}$$

Figure 45 shows the Bode plot of the open loop gain of a programmable PLL, based on equation (78) and (79). If the two equations are compared, it can be seen that there are: two LHP (left half plane) poles (ω_{p1} and ω_{p2}) at 0Hz; one LHP zero ω_z at $-1/(R_1 C_1)$; and a third LHP pole ω_{p3} at $-1/(R_1 C_{1,2series})$, where $C_{1,2series}$ is the equivalent capacitance of C_1 and C_2 connected in series. Since,

$$C_{1,2series} = \frac{C_1 C_2}{C_1 + C_2} = C_1 \cdot \frac{C_2}{C_1 + C_2} < C_1 \tag{80}$$

ω_{p3} is larger than ω_z. The LHP zero will make $s - \omega_z = s + |\omega_z|$, which will increase the phase angle of $H(s)_{open}$ with larger frequency around frequency ω_z. Thus it can improve

the phase margin of $H(s)_{open}$ because of the ripple of the $\angle H_{open}$ curve shown in Figure 45. When the peak of the ripple happens at the crossover frequency ω_c, the best phase margin can be obtained. With a better phase margin, the negative feedback system will be more stable.

Based on Figure 43 and Figure 44, the closed loop transfer function of the programmable PLL could be obtained as follows,

$$H_{closed}(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_{PD} \cdot Z(s) \cdot \frac{K_{VCO}}{s}}{1 + \frac{1}{N} \cdot K_{PD} \cdot Z(s) \cdot \frac{K_{VCO}}{s}} \tag{81}$$

By inserting the result of equation (77) into equation (81), the following result will be obtained,

$$H_{closed}(s) = \frac{K_{PD} \cdot \frac{R_1 C_1 s + 1}{s(C_1 + C_2 + sC_1 C_2 R_1)} \cdot \frac{K_{VCO}}{s}}{1 + \frac{1}{N} \cdot K_{PD} \cdot \frac{R_1 C_1 s + 1}{s(C_1 + C_2 + sC_1 C_2 R_1)} \cdot \frac{K_{VCO}}{s}} \tag{82}$$

By multiplying s^2 to both the numerator and the denominator of equation (82), the following result could be obtained,

$$H_{closed}(s) = \frac{K_{PD} \cdot \frac{R_1 C_1 s + 1}{(C_1 + C_2 + sC_1 C_2 R_1)} \cdot K_{VCO}}{s^2 + \frac{1}{N} \cdot K_{PD} \cdot \frac{R_1 C_1 s + 1}{(C_1 + C_2 + sC_1 C_2 R_1)} \cdot K_{VCO}} \tag{83}$$

In equation (83), when $s = j2\pi f = 0$, $H_{closed}(s)$ will be N. This means that at DC or steady state, the output phase $\Phi_{out} = N \times \Phi_{in}$. According to equation (76), $\Phi \propto f$, so $f_{out} = N \times f_{in}$.

5.2 A Fractional Programmable PLL

A frequency divider is an important component in a PLL. If the division ratio is N, and the input reference frequency of a PLL is f_{in}, the output frequency f_o will be $N \cdot f_{in}$. In the case of a PLL using a programmable divider, the frequency channel-distance of f_o will be $\Delta N \cdot f_{in}$, where ΔN is the increasing step of the division ratios. Obviously, the smaller the value of ΔN, the smaller is the channel distance. With a smaller channel distance and limited entire bandwidth, there could be more channels. It is not always a good idea to reduce f_{in}, because it will make a PFD to wait longer to compare the reference frequency with the signal out of the frequency divider. In that case, a longer settling time will be induced to the PLL. If a fractional programmable divider is used, ΔN will be reduced. Without decreasing f_{in}, smaller channel distance still could be obtained. Since f_{in} is not reduced, the settling time of the PLL will not be longer.

Another advantage of fractional division ratios is stated bellow. The loop bandwidth of a PLL should be set to lower than 1/10 of the reference frequency. At higher offset frequencies, the VCO phase noise will be smaller. Since the VCO phase noise will be high-passed to the output of the PLL, the VCO phase noise will be suppressed more with a wider loop bandwidth or a higher reference frequency. Thus with the same frequency resolution or output frequency channel distance, a fractional divider can use a higher reference frequency, which can have a wider loop bandwidth and lower phase noise from the VCO [30] [31].

5.2.1 A Fractional Programmable Frequency Divider

Figure 46 shows the schematic of the proposed fractional programmable PLL. The difference between this PLL and the one shown in Figure 43 is that a Delta-Sigma (ΔΣ) modulator is added to control the division ratio of the integer divider. The output signal of the ΔΣ modulator is changing between "0" and "1". For the ΔΣ modulator, if the fractional number at the input is ".f", the time percentage when the output is "1" should also be ".f". The average value of the output of the ΔΣ modulator will be ".f". Thus the LSB division ratio control P_0 will have an average value of ".f". If use "m" to represent the binary combination of the MSB controls "$P_1P_2\ldots P_n$", the entire division ratio will be "m.f". A fractional programmable division ratio is obtained and the output frequency f_o will be "m.f × f_{in}".

Figure 47 shows the schematic and the equivalent model of a first order ΔΣ modulator. It is an accumulator as shown at the left part of Figure 47, which includes a multi-bit adder and several DFFs.

If $\omega T << 1$, and T is the clock period for the accumulator,

$$z^{-1} = e^{-sT} = e^{-j\omega T} = \cos(\omega T) - j\sin(\omega T) \approx 1 - j\omega T = 1 - sT \tag{84}$$

$$\therefore 1 - z^{-1} = 1 - (1 - sT) = sT \tag{85}$$

From the equations shown in Figure 47 and equations (84) and (85), the following results could be obtained,

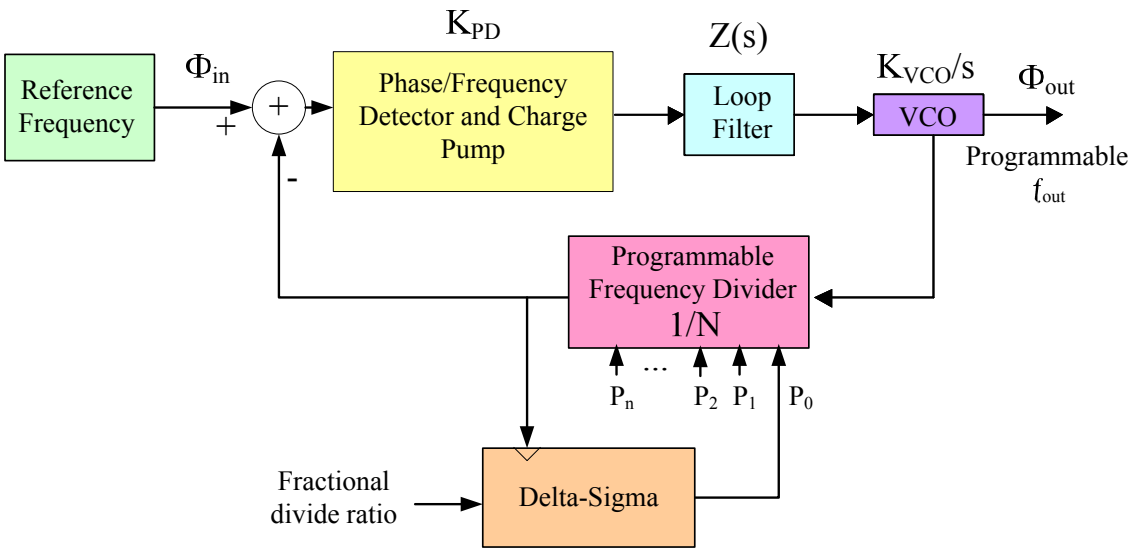
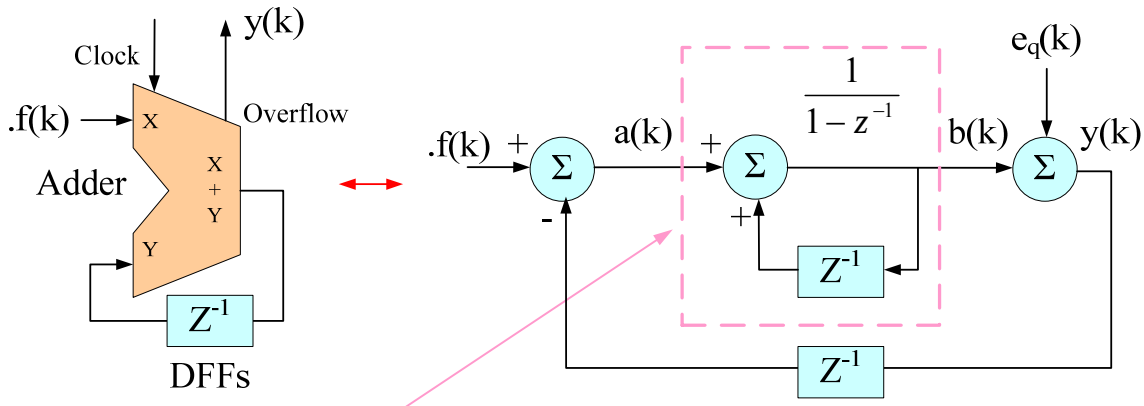


Figure 46: Schematic of the proposed fractional programmable PLL.



$$A + B \cdot z^{-1} = B$$

$$A = B - B \cdot z^{-1}$$

$$B = A \cdot \frac{1}{1 - z^{-1}}$$

$$(F - Y \cdot z^{-1}) \frac{1}{1 - z^{-1}} + E = Y$$

$$F - Y \cdot z^{-1} + E \cdot (1 - z^{-1}) = Y \cdot (1 - z^{-1})$$

$$F + E \cdot (1 - z^{-1}) = Y$$

$$Y = F + E \cdot (1 - z^{-1})$$

Figure 47: Schematic and the equivalent model of a first order ΔΣ modulator.

$$Y = F + E \cdot (1 - z^{-1}) \approx F + E \cdot sT = F + E \cdot j2\pi f \tag{86}$$

According to the result in equation (86), the output Y of the accumulator will high pass the quantization error E. It means that when the frequency f is higher, the output Y will contain larger component coming from the quantization error E. Thus the phase noise of Y will be higher at higher frequency f.

Figure 48 shows the proposed fractional programmable divider with more details. An accumulator or a ΔΣ modulator is inserted between the "f_{out_origin}" and the "C_{in}" input of the adder. The inputs of the accumulator are part of the division ratio controls. "S_0" is the LSB integer ratio control, while "Sf_1" and "Sf_2" are the MSB and LSB binary controls of the fractional division ratio. The input clock signal of the accumulator is connected to the original (Figure 7 (b)) integer divider output.

When the division ratio is $< 2^{min+1}$, S_{min} is set to logic '1'. Thus the division ratio of the fractional divider will be,

$$\begin{aligned} &division\ \ ratio \\ &= Sf_2 \cdot 2^{-2} + Sf_1 \cdot 2^{-1} + S_0 + S_1 \cdot 2^1 + S_2 \cdot 2^2 + S_3 \cdot 2^3 + \cdots + S_{n-1} \cdot 2^{n-1} + S_n \cdot 2^n \end{aligned} \tag{87}$$

5.2.2 The LC VCO

Figure 49 shows the LC VCO used in the proposed PLL, which is similar to the circuit used in [41]. Figure 49 (a) shows the top level schematic, (b) shows the equivalent circuit of the LC tank, and (c) shows the equivalent one-side circuit. The advantage of this circuit is the low power consumption and not too large output swing.

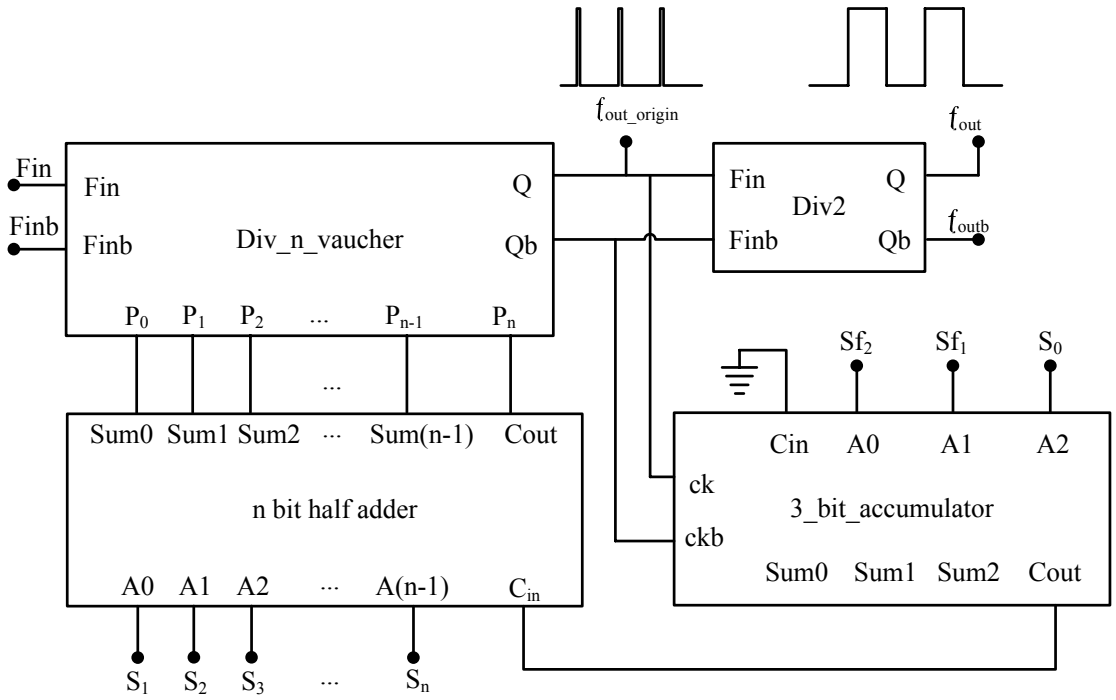


Figure 48: Schematic of the proposed fractional programmable frequency divider with more details.

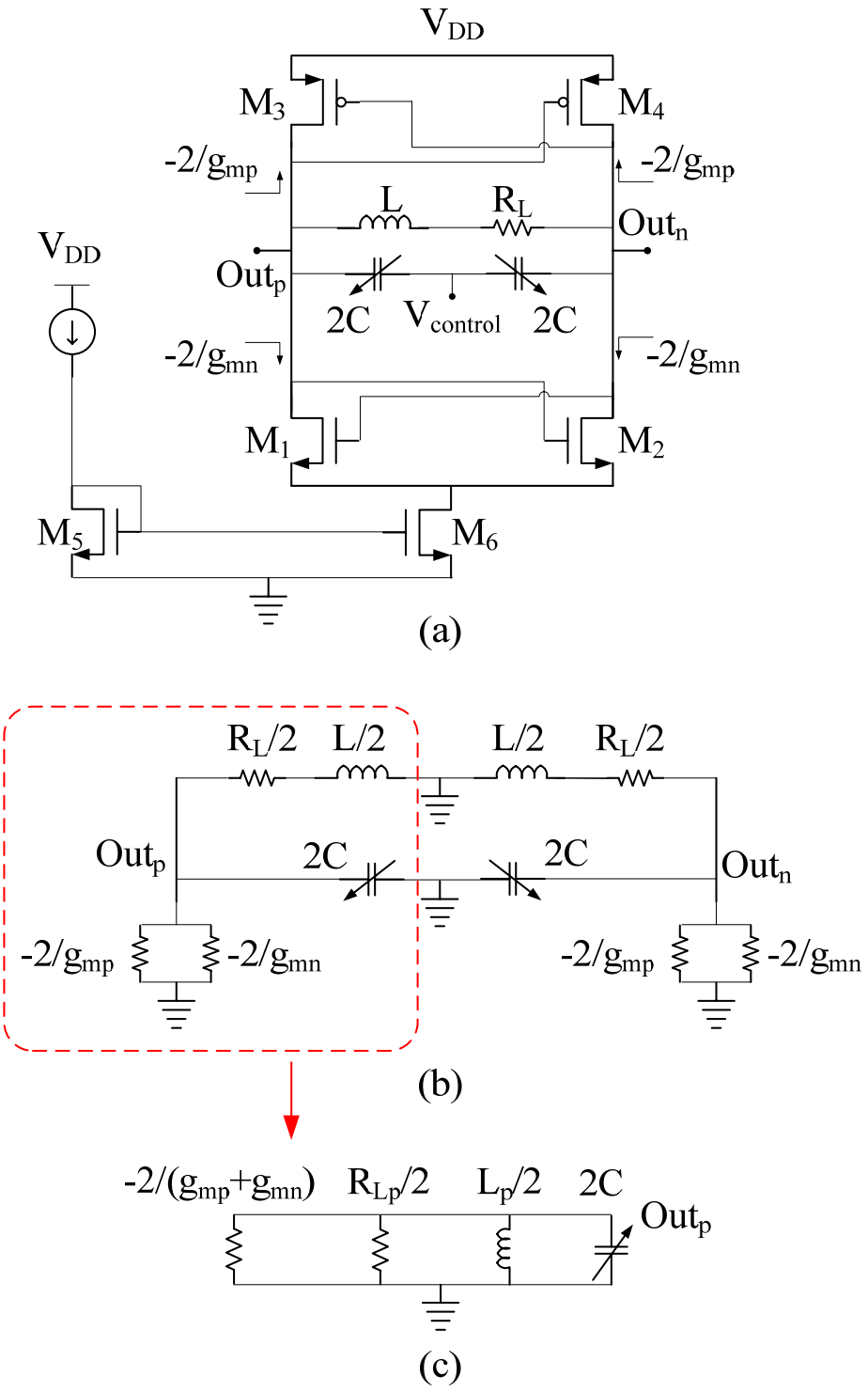


Figure 49: Schematic of the LC VCO used in the PLL: (a) the top level schematic, (b) the equivalent circuit of the LC tank, and (c) the equivalent one-side circuit.

In Figure 49 (a), both PMOS and NMOS cross-coupled pairs exist. They can reduce the power consumption, and limit the output swing to avoid destroying any device in the circuit. "R_L" is the series resistance of the inductor. The output impedance at the drain of each cross-coupled MOS is $-2/g_m$ [39]. The VCO control voltage $V_{control}$ and the voltage at the middle point of the inductor should be constant at the steady state. Thus they are AC ground. By splitting the inductor into two equal parts, Figure 49 (b) could be obtained. The left and right parts of Figure 49 (b) have symmetric structures. Forsimplicity, Figure 49 (c) only shows the left side of Figure 49 (b). In Figure 49 (c), according to [40],

$$R_{LP} = R_L(Q^2+1), \text{ and } L_P = L\frac{Q^2+1}{Q^2} \approx L \tag{88}$$

To keep the LC tank oscillate, the parallel impedance of $-2 / (g_{mp} + g_{mn})$ and R_{LP} should be infinite, so the current flowing into them will be 0 with limited voltage cross them. In that case, "$-2 / (g_{mp} + g_{mn})$ and R_{LP}" could be viewed as open circuit and be excluded from the LC tank. Thus the LC tank could maintain the oscillation like an ideal one. The following relationship should exist,

$$\frac{-\frac{2}{g_{mp}+g_{mn}}\cdot R_{LP}}{-\frac{2}{g_{mp}+g_{mn}}+R_{LP}} = \infty \quad \Rightarrow \quad -\frac{2}{g_{mp}+g_{mn}}+R_{LP}=0, \tag{89}$$

$$\therefore R_{LP} = \frac{2}{g_{mp}+g_{mn}} \tag{90}$$

$$\therefore g_{mp} + g_{mn} = \frac{2}{R_{LP}} \tag{91}$$

Since $g_m = \sqrt{2\beta I}$, sufficient large current "I" has to be given in the circuit for sufficient large $g_{mp} + g_{mn}$. Here g_{mp} and g_{mn} use the same dc current. There are other types of LC VCOs [37], which only have one pair of cross-coupled MOS, such as only one pair of cross-coupled NMOS. After the derivation similar to the above, the following relationship will be obtained,

$$g_{mn} = 2 / R_{LP} \tag{92}$$

Only one item g_{mn} appears on the left part of the equation. Thus for the same value of R_{LP}, more current is needed to obtain larger g_{mn}, when compared with equation (91).

Another advantage of the VCO shown in Figure 49 (a) is that the output voltage will not be higher than V_{DD}. While for some other types of LC VCO [37], the output may be higher than V_{DD}, which may destroy some transistors connected to the VCO outputs. In Figure 49 (a), when "Out_p" is high, "Out_n" should be low. Thus M_4 is off and M_3 is on. When "Out_p" is increased closed to V_{DD}, M_3 enters the linear region. The drain current of M_3 will be reduced. When "Out_p" is increased to V_{DD}, the drain current of M_3 will be 0. Thus the highest voltage of "Out_p" will be V_{DD}. Similarly, the highest voltage of "Out_n" will also be V_{DD}. Using this VCO, the circuit can operate properly for a long time.

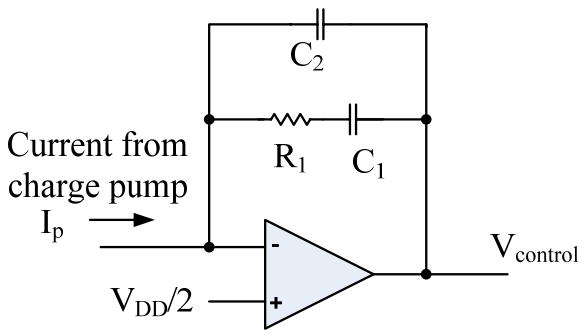


Figure 50: Schematic of the active loop filter.

5.2.3 The Loop Filter

Figure 50 shows the schematic of the active loop filter used in the proposed PLL. An off-chip amplifier is used in the proposed active loop filter. The advantage of this circuit is that the voltage at the inverting input of the amplifier will be biased at $V_{DD}/2$. Thus the voltage of the charge pump output will also be biased at $V_{DD}/2$.

The charge pump is shown in Figure 44. The current sources are MOS transistors in current mirrors. If the charge pump output is much lower than $V_{DD}/2$, and the switch connected to the NMOS current source is closed. The drain of the NMOS transistor used as the current source will also be much lower than $V_{DD}/2$. Since the V_{DS} may be less than $V_{GS} - V_{thN}$, the NMOS transistor may be driven into linear region. Thus the current generated from the NMOS current source will be smaller than the ideal value. At the same time, if the switch connected to the PMOS transistor used as the current source is closed, the drain of the PMOS transistor will be much lower than $V_{DD}/2$. Since the V_{SD} will be larger than $V_{SG} - |V_{thP}|$, the PMOS transistor will be in the saturation region. Its current will be the same as the ideal value. Thus there is a mismatch between the NMOS

and PMOS current sources. If the charge pump output is much higher than $V_{DD}/2$, the mismatch also exists. The current mismatch will induce jitters at the output signal of the PLL [37].

With the same combination of R_1, C_1 and C_2, their equivalent impedance Z(s) in Figure 50 will be the same as the Z(s) shown in equation (77). Since $V_{DD}/2$ is a constant value, the inverting input of the amplifier could be viewed as AC ground. Thus from Figure 50, the following result could be obtained,

$$V_{control} = - I_p \times Z(s) \tag{93}$$

For the passive loop filter shown in Figure 44,

$$V_{control} = I_p \times Z(s) \tag{94}$$

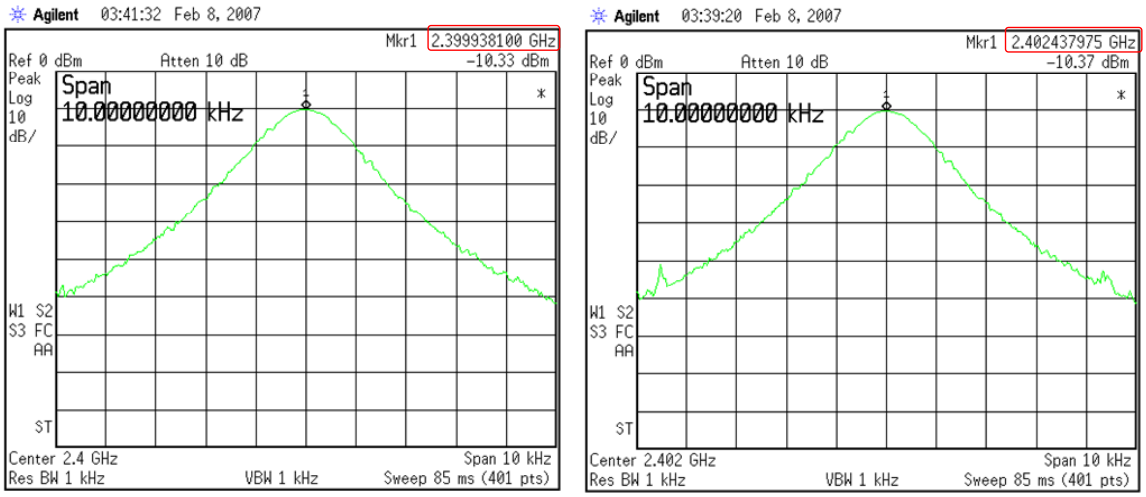
With the comparison of equations (93) and (94), the active loop filter has similar effects in the circuit as the passive loop filter. The only difference between them is that the polarities in equations (93) and (94) are different.

5.2.4 Test Results

The fractional programmable PLL is fabricated in the same chip using a standard 0.18-μm CMOS process. The right part of Figure 28 shows the photograph of the proposed PLL after fabrication.

Figure 51 shows the output spectra of the proposed PLL, where the divider in the PLL has division ratios of (a) 240 (b) 240.25. Figure 52 shows the phase-noise measurements

of the proposed PLL, where the divider in the PLL has division ratios of (a) 240 (b) 240.25 (c) 240.5 (d) 176.25. Both the output spectra and the phase-noise plot show the PLL output power densities at different frequencies. The phase-noise plot has a log-scale frequency unit, which is the difference from the output spectra. A 2nd order active loop filter is used in the PLL. The loop bandwidth of the PLL is set to about 100 kHz. The experimental results show about −82 dBc/Hz in-band phase noise at 10 kHz-offset frequency and −135 dBc/Hz out-of-band phase noise at 100 MHz-offset frequency. The jitter at the reference frequency (10 MHz) is about -67dBc/Hz compared with the PLL (or VCO) output power at the carrier frequency.



(a) (b)

Figure 51: Output spectra of the proposed fractional programmable PLL. The divider in the PLL has division ratios of: (a) 240, and (b) 240.25.

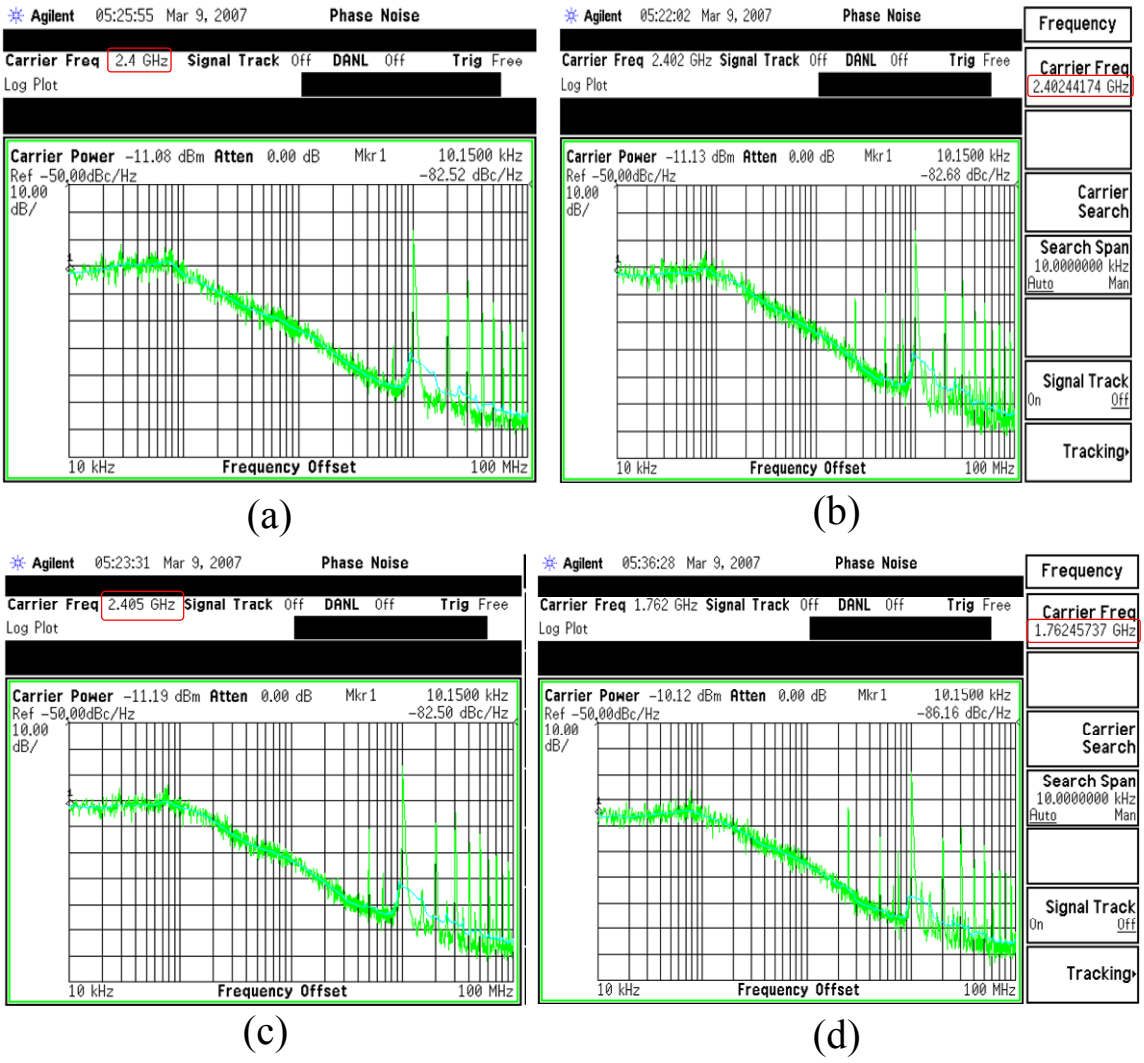


Figure 52: Phase-noise test results of the proposed fractional programmable PLL. The divider in the PLL has division ratios of: (a) 240, (b) 240.25, (c) 240.5, and (d) 176.25.

The fractional programmable PLL has an approximate frequency range of 1.7 - 2.5 GHz, and a frequency resolution of 2.5 MHz. With a 1.8 volt power supply, the power consumption is about 20 mW. The PLL can operate at 2.4 GHz with a power consumption of only 10 mW with a 1.46 V power supply voltage.

Chapter 6
Conclusions and Future Work

A highly efficient programmable frequency-divider with a wide division ratio range and close-to-50% output duty-cycle has been presented. The circuits are designed and fabricated using a 0.18-μm RF CMOS process. The test results verify the effectiveness of the proposed design. The output duty-cycle does not change with the input frequency (3.5 GHz down to 1 kHz), with temperature, with the voltage supply, or with different chips. When the power supply is 1.8 V, the power consumption of the programmable frequency-divider is about 15 mW.

A fractional programmable PLL is also presented. Test results show that the proposed PLL has a frequency resolution of 2.5 MHz, and a minimum power consumption of 10 mW when operating at 2.4 GHz.

In the future, a fractional PLL with a multi-bit and higher order $\Delta\sum$ modulator can be implemented for finer frequency resolution and lower phase noise. A charge pump [42] shown in Figure 53 can be implemented in the PLL. It can reduce jitters of the PLL at the reference frequency.

The charge pump shown in Figure 44 has a charge-sharing problem, which is stated in section 15.3.1 of [37]. This problem occurs when the PFD compares the reference

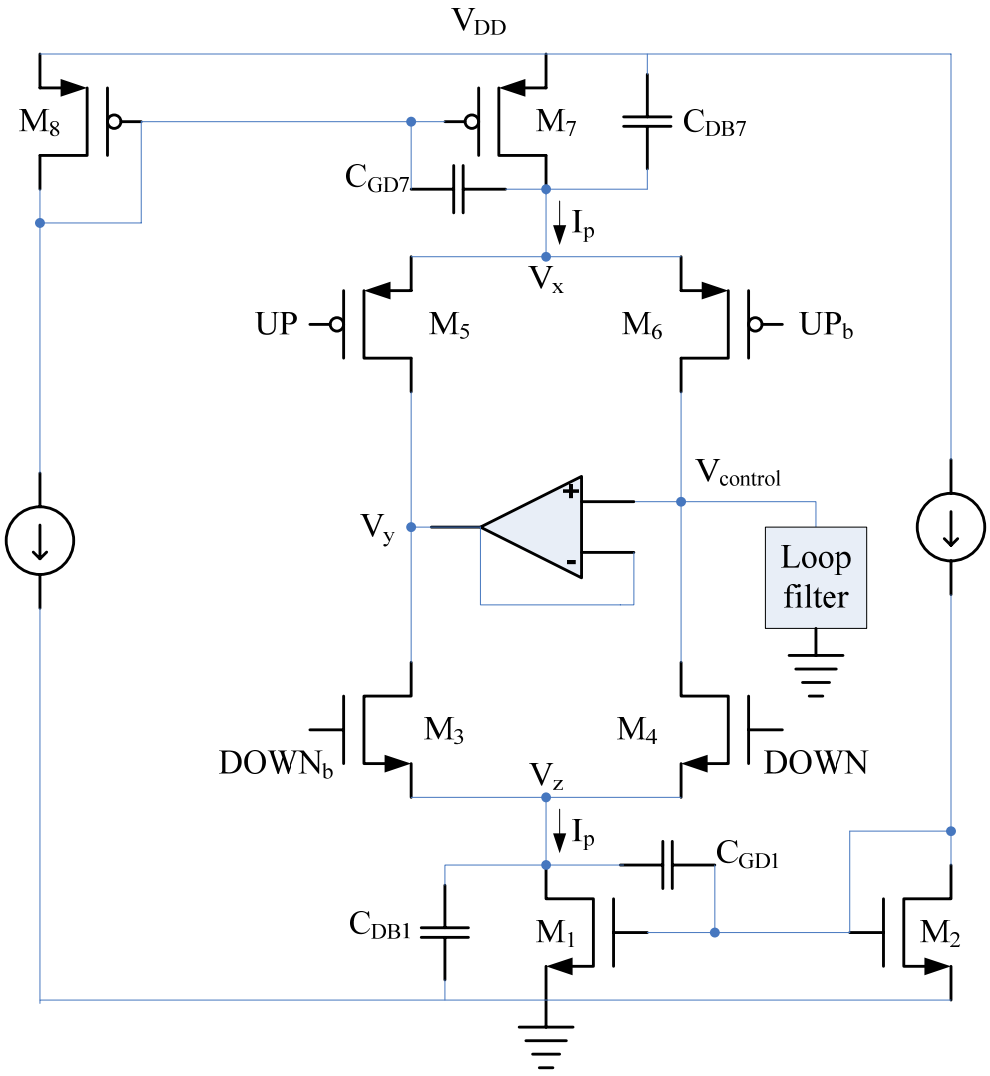


Figure 53: A charge pump that can reduce jitters at the reference frequency.

frequency and the divider output. Thus PLL output jitters will appear at the reference frequency. The advantage of the charge pump shown in Figure 53 is stated as follows. M_5 and M_6 have the same size. M_3 and M_4 have the same size. When UP is high, M_6 is on and M_5 is off. When UP changes from high to low, M_6 turns off and M_5 turns on. V_y follows $V_{control}$ and is equal to $V_{control}$. When UP changes from low back to high, M_6 turns on and M_5 turns off. Since M_5 and M_6 have the same size, and V_y is equal to $V_{control}$, neither I_{d7} nor V_x (V_{D7}) will change. Thus the charges on C_{DB7} and C_{GD7} will not change. Since I_{D8} and V_{SG7} are constant, V_{G7} is ac ground. There is no current flowing into C_{DB7} and C_{GD7}. Thus the current flowing into the loop filter will be exactly I_p. For DOWN part, when DOWN changes from low to high, V_z (V_{D1}) and the charges on C_{DB1} and C_{GD1} also do not change. Thus the current flowing out of the loop filter will be exactly I_p. No (or very little) current or charging disturbance occurs. Thus the PLL output jitters at the reference frequency will be reduced.

Programmable frequency divider is an important component in the integrated high-speed circuit. Any improvements of it will benefit in RF and digital design area. A programmable PLL is also a very interesting and challenging work. Efforts to improve each block in it will enhance the performance of the PLL, which may result more applications.

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