Design and Implementation of an ISFET Sensor with Integration of an on-Chip Processor

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Abstract

Portable sensors are used in many applications. Among them, pH sensors are suitable for quantifying and identifying various analytes in real-time and doing so non-invasively. The analytes may have environmental impact such as in water quality monitoring. The analytes may also have biological impact such as monitoring cell culture or remote patient health assessment. CMOS based sensors are compact and enable low power consumption suitable for these portable applications.

This work reports on the development of a portable CMOS based pH sensor. The contributions of this dissertation are as follows. First, a differential pH sensor, with two different sized electrodes that mitigates the need for time consuming and expensive post processing, was developed. The sensor was fabricated in a 0.5 μm CMOS technology and operated on 2 V supply with a power consumption and sensitivity of 12 μW and 42 mV/pH. Second, a voltage-clamped topology further lowered the required power supply and integrated a quasi-digital duty cycle based output signal that was proportional to the measured pH. The sensor was fabricated in a 0.18 μm CMOS technology and has a sensitivity of 40 mV/pH and area of 0.0036 mm^2. The duty cycle was further digitized, using a counter, in a 0.5 μm CMOS technology. The sensors occupied 0.205 mm^2 and consumed 206 μW. Finally, a portable pH sensing system was developed using a microcontroller to enable flexible post fabrication signal processing. The primary version was realized with an off-chip microprocessor. Further design miniaturization is explored through integration of both an on-chip MIPS and on-chip ARM microprocessor.

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Chapter 1

Introduction

Medical device design is a critical first step in creating new instruments for various medical applications. This includes new tools used at medical care facilities, implantable, wearable, and portable devices that can deliver medicines, monitor vital signs in real-time, and more. The design step is important in determining the functionality of the final product. Generally, a medical device's design can be broken into three categories: **mechanical, electrical, and software**. Though each of these is not always required, most modern, complex medical devices include all three categories. Mechanical design considerations may include device strength, ability to withstand stress, and product lifetime. Biomechanical materials will also need to be considered for medical devices, particularly for those that come into contact with patients.

Electrical engineering can apply to medical device designs across a wide array of needs. One key area is electrical sensors, both for direct patient monitoring or monitoring the device performance itself. Electrical components may also be required to power a mechanical movement, such as in a pump intended to deliver drugs. In some instruments, like a defibrillator, the primary function is to deliver an electrical current. Communication between other devices and networks is also a very common need. Electrical engineering design is required to achieve each of these things while ensuring the reliable performance of components.

Software is the final design category of medical device design. As these tools and instruments become increasingly complex, it is increasingly common for them to have their

operating system to control the device. This can range from device management and simple data collection to running complicated algorithms intended to make critical decisions within the device. The software design may also be limited by mechanical and electrical engineering design's physical characteristics.

Among the medical devices and sensors, biosensors convert the biological responses into a signal used for further process. The first biosensor was invented in 1956. It was invented by Leland C. Clark Jr., in oxygen detection systems. He paved the way for other sensors to be invented such as the glucose sensor in 1962, urea sensor in 1969, and the first commercial biosensor by Yellow Spring in 1975. Till now, there is huge progress and growth with novel biosensors [1]. Nowadays, the biosensors can play a vital role in electrical cell impedance measurements [2].

The main use of biosensors is in electrochemical measurements. It is used for the detection of chemical substances. The sensitive material in contact with the biosensors can be cells, enzymes, antibodies, and nucleic acids. A biosensor consists of a bio-recognition module, bio-transducer module, and some electronic systems. The electronic systems are subdivided into a signal amplifier, signal processor, and display. In order to make the devices small, CMOS-based sensors can be used. The bio-receptor, which is a recognition component, can use bio-molecules from organisms or receptors. These molecules interact with the system, and the bio-transducer measures the interaction. The result is seen as a measurable signal proportional to the target analyte amount in the sample. The primary goal of designing a biosensor is to detect the targets quickly, accurately, and easily. The structure of this biosensor can be divided into the categories which are depicted in Fig. 1.1 [1, 3, 4],

- The bio-receptors are some bio-selective materials that interact with the analytes, such as the enzymes, the cells, and the antibodies.

- The transducers have the same characteristics as the electrodes, pH electrodes, field-effect transistors, and some nano-particles. Since the signal of the biosensors is pretty small, an amplification stage is needed. A data processing system and a display unit for illustrating the results are necessary.

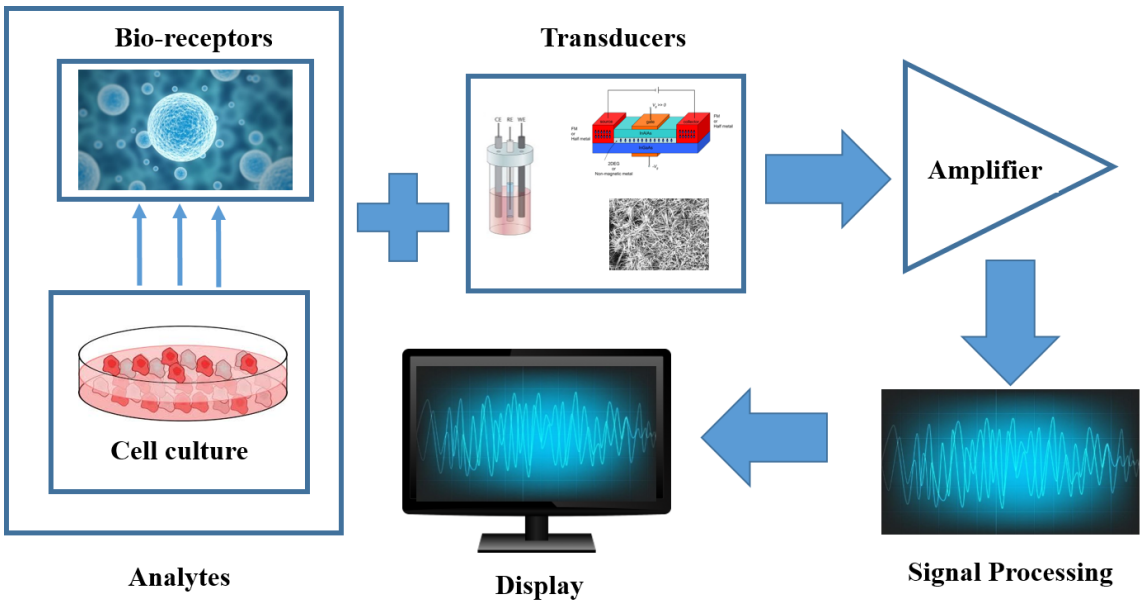

Figure 1.1: Biosensor setup (adapted from [1], [3], [4]).

Today miniaturization and wireless connectivity have seen the bulkiest devices shrink to once impossible sizes, allowing for the portability of complex and life-changing technologies. Although we all enjoy our smartphones, mp3 players, and other entertainment and communications devices, medical device portability can be genuinely life-changing and sometimes life-saving. Specially during COVID 19 pandemic and the high need for portable medical devices, the patients can stay home or travel using portable medical devices. At the same time, they can connect with their doctors remotely. With the records of the data, the doctors can treat the patients and give them good advice (Fig. 1.2) [5].

Generally, portable medical devices can be divided into different categories. They are available to be used in respiratory applications, blood glucose meters, blood pressure monitors, and ultrasound devices (Fig. 1.3) [6, 7, 8, 9].

1.1 Research Goals

This dissertation makes a number of scientific contributions. First, a differential voltage-clamped pH sensor is developed. The novelty of this design is in using different sizes of the sensing electrode gate areas without using CMOS post-processing for a more cost-efficient design. Second, a portable system is developed with an end goal of being able to display a pH measurement readout on a display (LCD). The portable pH sensor is implemented using an ADC and microcontroller to measure and read the analog voltage output of an ISFET based sensor circuit. Since this design needs to be used in biomedical applications, the size is reduced to have all of the blocks on a single chip. A quasi-digital circuit is used to convert the signal to a digital signal, and an on-chip processor is also used to further reduce the size and power. The system overview is shown in Fig 1.4. Having sensors integrated with an on-chip processor decreases power while the device is in use. The advantage of this design is that the power consumption and the size are pretty small compared to using the off-chip processors. The design, implementation, and simulation of the portable pH sensor are shown in this dissertation.

Figure 1.2: Usage of portable medical devices [5].

(a) **(b)** **(c)** **(d)**

Figure 1.3: Portable medical devices (a) Respiratory products [6]. (b) Blood glucose meters [7]. (c) Blood pressure monitors [8]. (d) Ultrasound devices [9].

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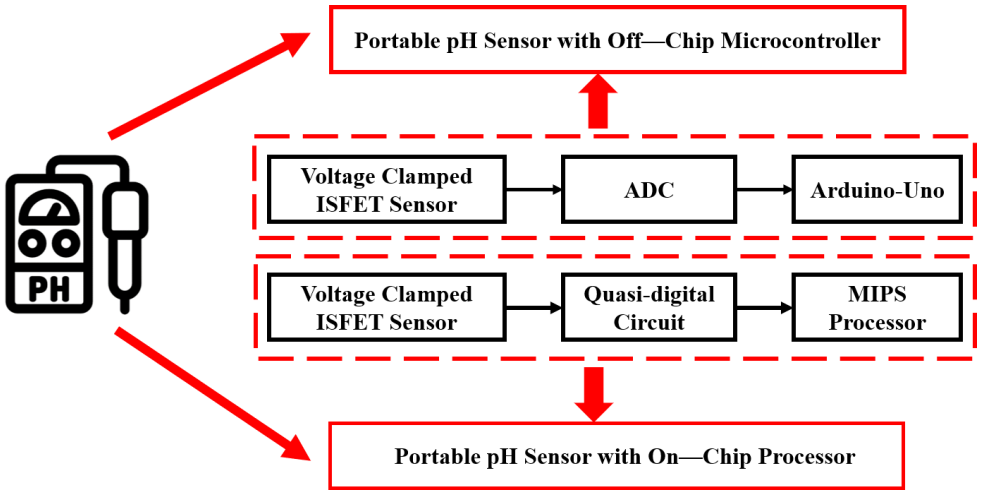

Figure 1.4: Proposed design showing a portable ISFET pH sensor along with an on-chip and off-chip processor.

1.2 Dissertation Overview

The rest of this dissertation is organized as follows. Chapter 2 presents the literature reviews over ISFET pH sensors, analog to digital converters, and microprocessors. After a literature review, the proposed system design of a differential ISFET pH sensor along with the simulation, electrical experiments, and sensor calibration experimental verification with standard pH buffer solutions are described in chapter 3. Chapter 4 depicts the single-ended ISFET pH sensors. This chapter includes all of the simulation, electrical experiments, and experimental verification with standard pH buffer solutions. A pH-impedance system for lab-on-a-chip based sensing is described in chapter 5. In chapter 6, an architecture that incorporates a MIPS based processor and ARM based processor are explored. A comparison between the two architectures is outlined. The synthesized on-chip designs of these processors with their simulations and post-layout simulations are included in this chapter. The proposed integration is verified by integrating the pH sensor with digitized output with the processor implemented in an FPGA platform along in the chapter concluding sections. Finally, in chapter 7, the conclusion is discussed, and possible future paths are outlined.

Chapter 2

Literature Review

Portions of this section are published in,

"ISFET Digital Readout Circuit with an on-Chip MIPS Processor," IEEE Sensors, Rotterdam, Netherlands, Oct 2020.

"A Portable CMOS Based pH Sensor," IEEE International Midwest Symposium on Circuits and Systems, Springfield, MA, USA, pp. 525-528, Aug 2020.

"CMOS Based Whole Cell Impedance Sensing: Challenges and Future Outlook," Biosensors and Bioelectronics, Vol. 143, 111600, Oct 2019.

"A Low-Power Voltage-Clamped CMOS pH to Frequency Sensor," IEEE International Symposium on Circuits and Systems, Sapporo, Japan, pp. 1-5, May 2019.

"A Differential Low-Power Voltage-Clamped ISFET Topology for Biomedical Applications," IEEE Dallas Circuits and Systems Conference, Dallas, TX, USA, pp. 1-4, Nov 2018.

2.1 pH Sensors

Electrochemical sensors are characterized via transduction. This is the reason for a chemical reaction between the analytes and the receptors. This reaction is called Redox. In a simpler words, Redox is an exchange of the electrons at the surface. For electrochemical measurements, three sets of electrodes are used. They are the Working Electrode (WE), Reference Electrode (RE), and Counter Electrode (CE). For measuring the current flow in

the WE, the potential on it must be constant. Consequently, RE is used to keep the potential constant. CE is used to measure the current, which is related to the Redox Reaction. The illustration of these electrodes with its equivalent circuit is shown in Fig. 2.1 [1].

For electrochemical measurements, different kinds of pH sensors can be used. These pH sensors are divided into potentiometric glass pH sensors, metal-metal oxide pH sensors, ISFET pH sensors, and fiber optic pH sensors. The potentiometric glass pH sensors work based on the potential difference between a glass electrode and a reference electrode. A glass membrane that is pH sensitive is used in its structure. The tube has a silver (Ag) and silver chloride (AgCl) reference electrode. This structure combines the electrical and chemical [1]. The structure is depicted in Fig. 2.2.

Optical methods for measuring the pH is in the category of fiber optic based pH sensors. It consists of an optical fiber. A photodetector, such as a photodiode or a photomultiplier, is used in this structure. Two kinds of sensing can be used in this technique, direct and indirect. In the case of direct sensing, the tip of the fiber is in contact with the solution. In the case of indirect sensing, the indicator's color is monitored to measure the pH [10].

Although glass electrodes are widely used, small and more flexible materials are needed for the structure in some cases. In metal-metal oxide pH sensors, metals such as Sn, Fe, Ir, Ag, Cu, and Zn are used and are coated by an oxide. In the ISFET pH sensor, traditional FET with some changes is compatible with ion concentration measurements. The ISFET structure is similar to Metal Oxide Semiconductor Field Effect Transistor (MOSFET) where the gate is floating. The reference electrode replaces the metal gate. Ion sensitive material such as SiO^2 is placed on top of it. Positive hydrogen ions are the reason for separating the charges on the other side of the transistor's dielectric in the channel region. By increasing the number of hydrogen ions near the dielectric, the device's IV characterstic is changed. In ISFET, this is modeled as a threshold voltage change [11, 12].

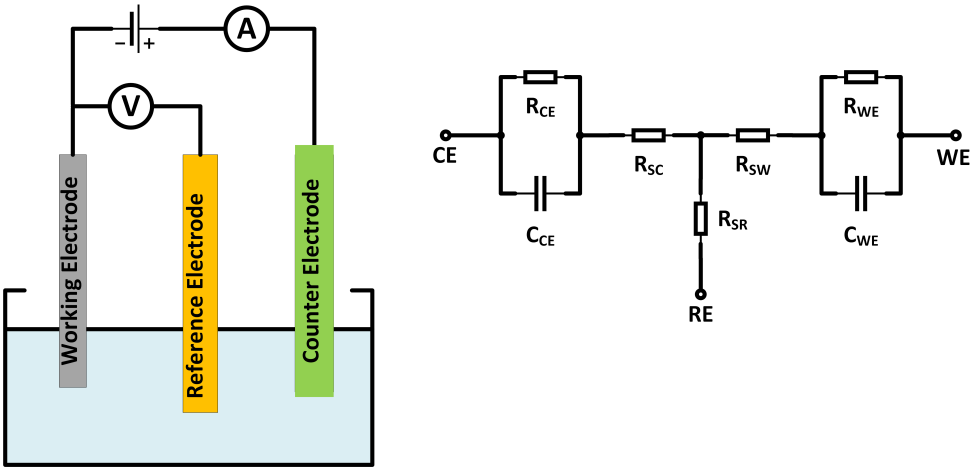

Figure 2.1: Three electrodes electrochemical cell.

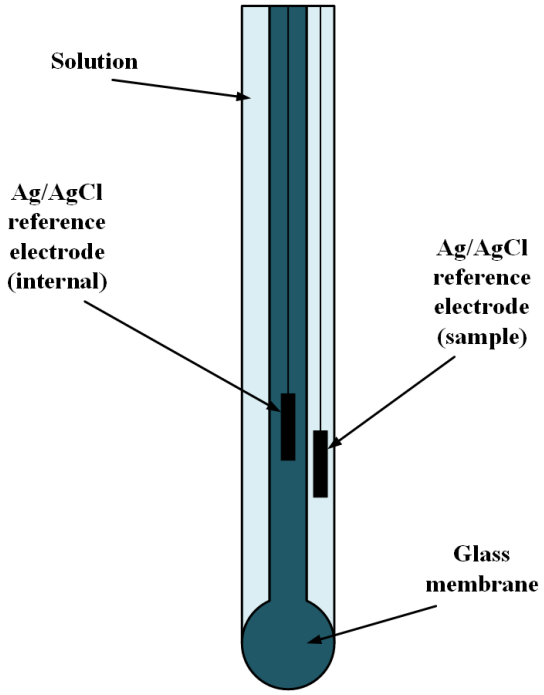

Figure 2.2: Glassy pH sensor.

Using the integrated CMOS pH sensor is valuable since it minimizes the space between the sensors and the electronic. In that case, the noise sources can not be coupled to the integrated system easily. The ion-sensitive field-effect transistor (ISFET), developed originally in the 1970s [11], has largely paved the way for this research area. While other pH sensing devices such as the ion-sensitive electrodes (ISE) exist and are used today, the ISFET is far smaller, cheaper, and more robust than it's ISE counterpart. This combination makes the ISFET ideal to achieve small, portable, and even implantable pH sensing devices. In the past, ISFET devices were developed and used; they required large and complex circuitry to perform the measurement readout function. They also required special, modified processes to fabricate [13, 14, 15]. These things are counter-intuitive to the goal of achieving a complete system-on-chip (SoC) design utilizing ISFETs. To fully realize this, the ISFET and its readout circuits need to be compatible with the standard, commercial CMOS process without any extra steps, allowing for easy fabrication, small size, and cheap cost.

A large focus of the research is done in this area. It is shown that an ISFET can be produced in a standard CMOS process without any post-processing by using an extended gate structure [16], however, the devices exhibited large, varied threshold voltages associated with different device geometries. The extended gate approach used the standard top passivation material of the CMOS process, typically silicon nitride or silicon oxynitride stacked on top of silicon dioxide, to serve as the pH sensing layer [16, 17, 18]. The polysilicon gate of a normal MOSFET is extended to this passivation layer using the normal metals in the CMOS process to create vias. Using an extended gate such as this, an ISFET can be fabricated entirely in the standard CMOS process. In turn, all existing CMOS circuit cells and resources can also be used to implement completely integrated ISFET sensor circuits. The cross-section of an ISFET pH sensor is depicted in Fig. 2.3 [19]. As has already been touched on, CMOS implementation for the ISFET does not come without challenges. These challenges come from non-idealities in both the physics of the ISFET itself and fabrication in the CMOS process. These include problems like trapped charge, drift, capacitive attenuation, temperature effect, and noise corruption [20, 21, 22]. Each of these issues is still being researched to provide possible solutions. For example, it is shown that UV radiation can be used to control threshold voltage and reduce it to a more acceptable level [17] and that a

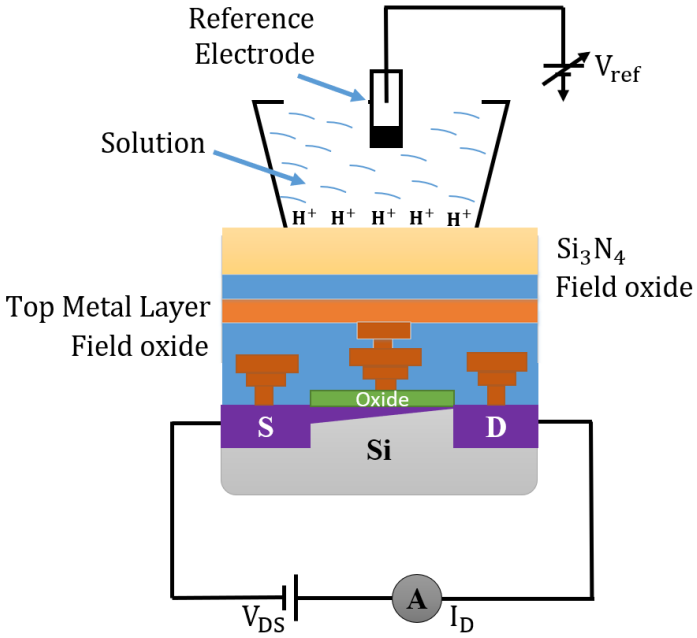

Figure 2.3: Cross-section of an ISFET [19].

bridge-type floating source circuit can be implemented to provide temperature compensation and greater stability [23, 24, 25].

Nonetheless, these are all problems that need to be addressed to achieve the desired reliability and scalability with ISFET CMOS integration. Another important innovation came from the work of Shepherd and Toumazou, which showed that an ISFET could be utilized as a transistor with chemical input through operation in the weak inversion region [18, 26, 27]. Very importantly, weak inversion allows for a current in the order of nanoamps, meaning the device can be operated at very low power in the order of nanowatts. With some external manipulation, the ISFET in weak inversion yields a linear proportionality function between the output current and the ion concentration. Furthermore, the current-mode output can be paired with trans-linear circuits to perform real-time analysis such as multiplication and division [26]. The contribution operation of an ISFET in weak inversion is an important step towards the complete chemical VLSI and SoC integration designs.

2.1.1 ISFET Behavioral Macro-Model

An ISFET device is described as a MOSFET transistor for which the gate has been separated by an insulating layer that is chemically sensitive and tied to a reference electrode. When there is ion interaction from the interface of a solution with the sensing insulating layer, the $I_D - V_{GS}$ characteristics of the device are affected. When a voltage is applied to the reference electrode, it is capacitively coupled with the insulator, and the channel current is controlled by the pH-depending charge of the ions present at the interface. The result is that the threshold voltage (V_{th}) is modulated by the pH of the solution applied at the insulator interface. The consequence of a charge build-up at the electrolyte insulator interface is an equal and opposite charge, spreading over the double layer, leading to the Helmholtz plane, known as the charge distribution of attracted to the insulator surface sites. The charge following distribution by Boltzmann is described as the Gouy-Chapman layer, which is the diffusion (Fig. 2.4) [28].

The characteristics of the ISFET can be derived using site-binding theory, which considers the ion at the insulating surface, alongside the Gouy–Chapman–Stern double layer model, which considers the capacitive double layer formed by the Helmholtz plane and the

Gouy–Chapman layer [29]. From this derivation, the modulation of the threshold voltage can be described as a combination of the typical MOS threshold voltage with additional chemical terms (eq. (2.1)),

$$V_{th_{ISFET}} = V_{th_{MOSFET}} + \gamma + \alpha S_N pH \tag{2.1}$$

where γ is a constant chemical term, S_N is Nernstian sensitivity (typically 59 mV/pH), and α is a number from 0 to 1 describing the deviation from Nernstian sensitivity due to the capacitive double layer [18]. The chemical terms in eq. (2.1) are often combined as a final simplification,

$$V_{Chem} = \gamma + \alpha S_N pH \tag{2.2}$$

A simplified macro-model, shown in Fig. 2.5 [19], can also be derived using the theory and effects previously discussed to model the ISFET [18, 20]. From this model, the following equation (2.3) can be observed,

$$V_{G'} = V_G - V_{Chem} \tag{2.3}$$

Using this macro-model and the relationship in eq. (2.1), the device cannot be shown to operate in the same regions as a MOSFET. For strong inversion, this equates to the typical saturation region equation for a MOSFET,

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{G'S} - V_{th})^2 \tag{2.4}$$

where μ, C_{ox}, W, and L are device parameters, $V_{G'S}$ is the chemically dependent potential determined by eq. (2.3), and V_{th} is the device threshold voltage. Strong inversion was initially the only operation mode considered by researchers for the ISFET until the weak inversion region of the ISFET was introduced.

For the weak inversion operation mode shown by Georgiou and Toumazou [18], the channel current is dominated by diffusion of carriers, as opposed to drift, due to the operating condition of $V_{GS} < V_{th}$. The result is that the operation characteristic (assuming that $V_{DS} > 4U_t$) is described by an exponential relationship,

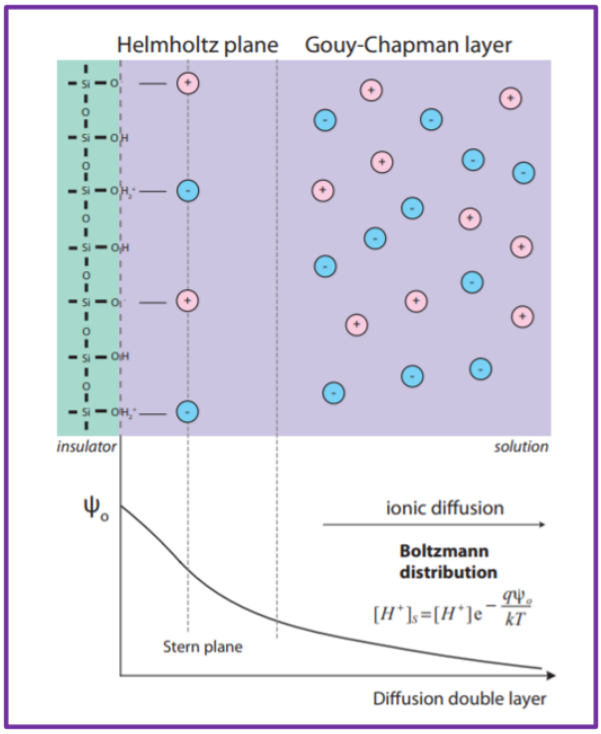

Figure 2.4: Formation of the Helmholtz plane and the Gouy-Chapman layer on an ISFET due to the charge distribution [28].

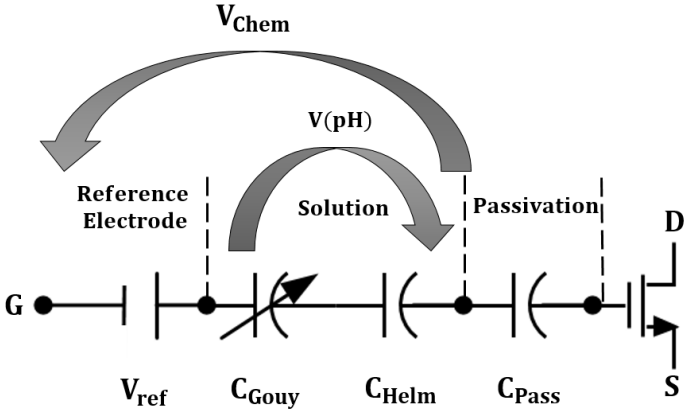

Figure 2.5: ISFET macro-model. C_{Gouy} is the Gouy-Chapman layer capacitance, C_{Helm} is the Helmholtz layer capacitance, and C_{Pass} is the passivation layer capacitance [19].

$$I_D = I_0 \times exp\frac{V_{GS} - \gamma - \alpha S_N pH}{nU_t} \tag{2.5}$$

where I_0 is the characteristic current, V_{GS} is the gate-to-source potential, V_{DS} is the drain-to-source potential, n is the sub-threshold slope factor, and U_t is the thermal voltage. Operation in this region provides benefits such as low-power operation and high intrinsic voltage gain [18].

2.1.2 ISFET Readout Circuits

In the world of sensors, the sensing device itself is nearly meaningless without a proper way to interpret and manipulate the information being sensed. For a sensor, accuracy is key, and as such, a great amount of emphasis is placed on the various signal processing steps of a sensor system. Characteristics such as detection limits, resolution, and dynamic range determine the quality of a sensor. They are directly correlated to how the sensing device is interfaced with the analyte to retrieve the measured information. A readout circuit serves as the intermediary between the sensing device (here an ISFET) and any signal processing performed. For an ISFET, the readout circuit serves to establish a quiescent operating point. It is possible to track its floating gate, which in turn correlates to tracking the chemical signal input. This is achieved due to the sensing membrane potential being directly modulated by the ionic concentration (pH) of the chemical input to the ISFET. By tracking the floating gate, an ISFET readout circuit can produce an analog voltage or current output that is a direct function of ionic concentration. With this relationship established, other means of signal processing can easily be achieved to further process the signal.

When considering the readout circuit design for an ISFET-based sensor, the desired application becomes a critical factor in determining the readout circuit's overall design direction. This includes considerations of chip area, power, accuracy, number of sensors, robustness, temperature, and cost. Any of these things, amongst others, limit the options as to what a feasible readout circuit could be for any given application. It is important to go into readout design, considering the advantages and disadvantages of any given approach to achieve an optimum readout for the required application. For example, many readout

configurations fail to address the random DC offset at the floating gate, so readouts such as piecewise-linear approximating (PLA) are used in [30], in an attempt to address it as well as temperature independence and linearity. Of all the readout circuits proposed for ISFET pH sensing, there are essentially five groups depicted in the following. Each type can come in many flavors, which may vary in complexity, advantages, and disadvantages. The five generalized groups include [20, 31],

- **Single-Ended Readout:** An output current or voltage relates the floating gate potential only through a buffer.
- **Differential Readout:** Common-mode signals are rejected through differentiation from a reference FET.
- **Programmable Gate Readout:** A control capacitor is added to the ISFET's floating gate to act as a programmable gate capable of tuning and canceling DC offset.
- **Trans-linear Readout:** The ISFET is biased in weak inversion to provide an output current that is not temperature sensitive through analog computation.
- **Averaging Array Readout:** An array of ISFETs, each paired with one of the above readout types, takes the overall set's average output signal.

Single-Ended Readout

A single-ended ISFET readout can be as simple as a source-follower buffer or can be more complex by using feedback. It can be divided into a few categories detailed in the following sections.

Drain-Source Follower: Constant V_D, V_{Ref}, and I_D. V_S varies with pH.

The ISFET terminals are kept constant, and the drain current is kept constant through biasing and feedback. This allows for any changes at the floating gate to be tracked by the source and drain terminals of the ISFET. Also, it provides linearity at the expense of chip area and sensitivity to mismatched current sources. No further signal processing is performed, and the signal may clip with sufficient DC offset. Fig. 2.6a shows this structure

[20]. Most of these structures use feedback via operational transconductance amplifiers, resulting in a higher number of transistors and power consumption. Based on the results, they are not suitable for implantable and biomedical applications [32].

Feedback to Gate: Constant V_D, V_S, and I_D. V_{Ref} varies with pH.

The ISFET terminals and current are kept constant through feedback by adjusting the reference electrode. This can potentially remove DC offset if the reference electrode range is sufficient and also serves to remove the effect of the decoupling capacitor (Fig. 2.6b) [33].

Voltage Clamped: Constant V_D, V_{Ref}, and V_S. I_D varies with pH.

The voltage at the ISFET terminals is kept constant, and the current becomes a function of the change in potential at the floating gate. However, the linearity of this configuration is limited by the supply rails and the cascode-regulating transistor's saturation operation. The ISFET can be biased in either strong or weak inversion to achieve either a linear or exponential relationship, respectively (Fig. 2.6c). This technique reduces OTAs by providing an interface with a constant and stable bias to the ISFET. Subsequently, fewer transistors are required, and the power will be decreased [34, 35].

Differential Readout

Differential readout uses a reference FET (REFET) to tackle noise and signal drift issues through common-mode rejection. The REFET experiences a similar condition to the ISFET, except for responding to an occurring chemical reaction. A REFET can be implemented by either making an ISFET with an insensitive membrane or copying the ISFET exactly and isolating it while exposed to a solution such that no reaction occurs. A standard differential pair can be used with one input as an ISFET and the other as a REFET. This results in reducing both electrical and chemical noise (Fig. 2.7) [36, 37, 38, 39].

Programmable Gate Readout

This technique addresses the DC offset issue by introducing a control capacitor C_{CG} to the ISFET floating gate, resulting in a programmable gate ISFET (PG-ISFET). The trapped

charge in the passivation layer (creating the DC offset) of the ISFET can be canceled out by tuning the control capacitor. It should also be noted that, if the drift trend is clear, it also could be similarly canceled by the control capacitor. Up to this point, however, drift appears to be mostly random and unpredictable. Based on this concept, several readout circuits were introduced to take advantage of it, such as auto offset removal and direct capacitive feedback circuits. Auto offset removal uses two control capacitors in which one is used for offset evaluation, and the other is used for sensing, and the feedback is used to switch between two modes. Direct capacitive feedback resets the floating gate and, through the use of feedback and the control capacitor, tracks the changes. A programmable gate adds flexibility and another degree of freedom to the system but comes at the expense of increased area and decreased scalability (Fig. 2.8) [40].

Trans-linear Readout

Trans-linear readout is based on the trans-linear circuit's principal, allowing current-mode signal processing from the chemical input signal by operating the ISFET device in weak inversion. The temperature effect on pH sensitivity is then eliminated due to the similar intrinsic FET temperature dependency within the weak inversion operation region. Using this concept, several circuits were proposed to take advantage of it, such as the H-cell and chemical Gilbert cell. The H-cell serves to produce an output current, which becomes an exponential function of the pH. The chemical Gilbert cell uses a differential measurement between the output currents of two ISFETs with a tunable gain input. The output current is proportional to the gain in pH and is controlled by the bias current.

Alongside eliminating the temperature dependency, the translinear readout is advantageous for low-power readout due to the weak inversion operation. Scaling, however, is an issue.

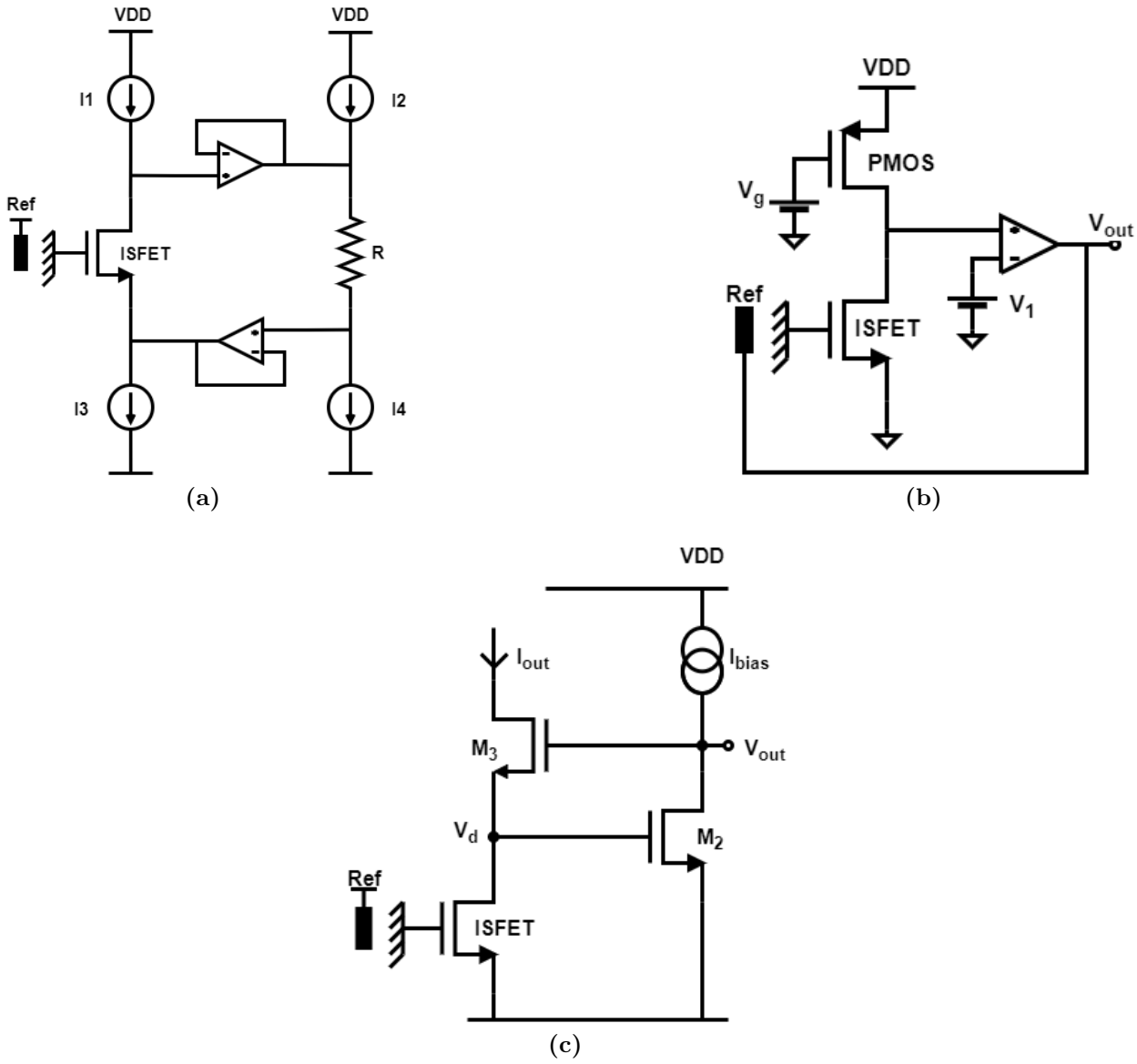

Figure 2.6: Single-ended readouts topologies for ISFET: (a) **Topology:** Constant V_D, V_{Ref}, and I_D. V_S varies with pH [20]. (b) **Topology:** Constant V_D, V_S, and I_D. V_{Ref} varies with pH [33]. (c) **Topology:** Constant V_D, V_{Ref}, and V_S. I_D varies with pH [34].

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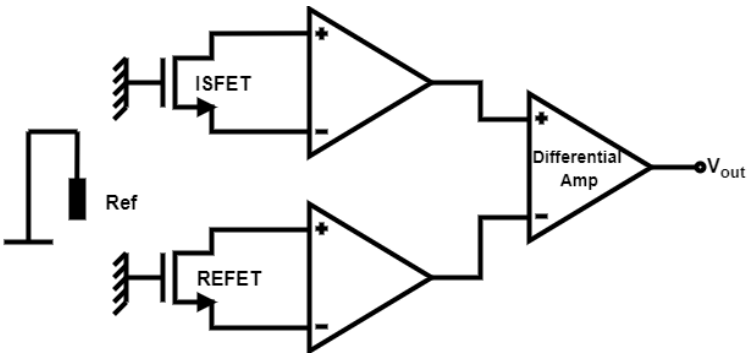
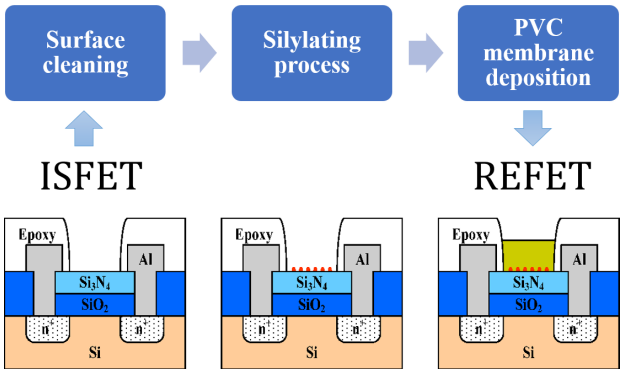


(a)



(b)

Figure 2.7: Differential readout: (a) Differential readout circuit [36]. (b) Cross-section of the differential readout circuit [37].

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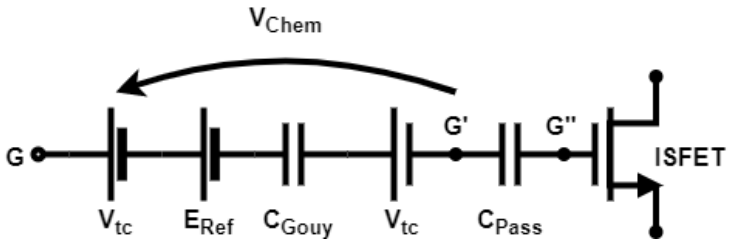


Figure 2.8: Programmable gate readout [40].

DC offset, biasing, and calibration becomes increasingly complex to handle as scale increases (Fig. 2.9) [41].

Averaging Array Readout

Averaging array readout uses multiple ISFET devices, each utilizing one of the readouts mentioned earlier types, and sums the resulting outputs. An averaged result can be generated through instrumentation. Averaging arrays come at a cost. It is also possible that DC offset can bias an ISFET outside of the desired operation region, possibly resulting in the signal being further attenuated, rather than improved, by the averaging. In [42], the averaging array technique was used to make the pixels within the same array carry sensitivity to all parts. It resulted in multi-ion sensing.

ISFET Applications

ISFETs have different applications and can be divided into two big categories such as *in vivo* (eg. cancer detection, and intracellular-extracellular activities), and *ex vivo* (eg. urine tests, saliva tests, and cell counts and viability) (Fig. 2.10) [43]. There are also categories, such as ENFET and BIOFET that represent the ISFET function under a specific condition. In general, ENFETs are enzyme-modified ISFETs which measure analyte concentration, like glucose. At the same time, BIOFETs are bio-organic-semiconductor field-effect transistors, which are helpful to measure the concentration of proteins or DNA [44]. The very first ISFETs were designed for *in vivo* applications such as "heart pace maker". The first commercial application of the ISFET was a catheter for *in vivo* measurements of the blood pH [43]. Based on the dipstick device, Bergveld and his team fabricated an enzyme sensor with ureas for *ex vivo* applications. They also invented an ISFET pH sensor to be used on muscles and the nerves [45]. One of the most important applications of ISFET is DNA sequencing. In the extension process, base pairs are integrated with a chemical reaction that releases H^+. This results in a pH change of the reaction solution [46]. Another application is using ISFET that are integrated with microfluidics to monitor sodium ions (Na^+) concentration in sweat [47]. These applications are illustrated in Fig 2.11 [45].

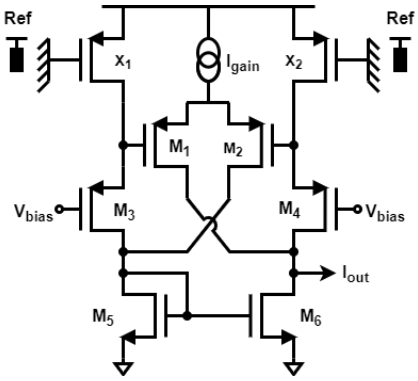


Figure 2.9: Trans-linear readout (Gilbert cell) [41].

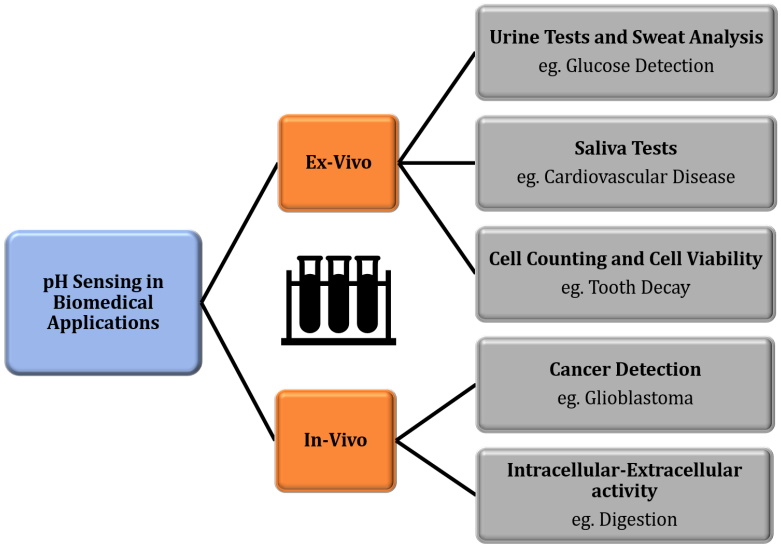
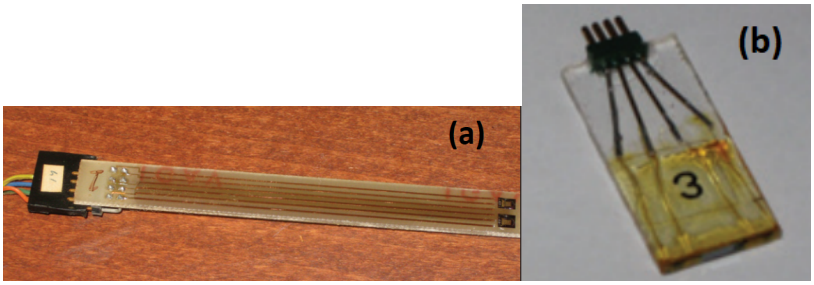


Figure 2.10: pH applications in two different groups: *in vivo*, and *ex vivo*.



(a) **(b)**

Figure 2.11: ISFET applications to be used with, (a) urea and (b) muscles and nerve [45].

2.2 Analog to Digital Converters

To interface between an analog front-end and the processor, an analog to digital conversion step is required. Several approaches convert the signal of the sensor into parameters such as phase, frequency, and magnitude. In these methods, the transistors and the amplifiers are used for converting the signal to voltage, and the analog to digital converters (ADCs), quasi-digital circuits, or voltage-controlled oscillators (VCOs) are utilized for digitizing the corresponding voltage [48, 49, 50, 51]. Quasi digital circuits present some advantages, such as dynamic range for size, compared to ADCs or VCO based solutions [51].

Amongst the Nyquist ADC group and the oversampling ADCs, there are a variety of different ADC architectures with differing performances in speed and resolution depending on the intended application. These can be further split into two groups, high-resolution ADCs and high-speed ADCs.

High-Resolution ADCs

When selecting an ADC architecture, the target application is typically used to select the optimal architecture based on the required performance, including resolution and speed. For high-resolution ADCs, the pipeline architecture is traditionally used. More recently, successive approximation registers (SAR) and pipelined SAR architectures have been used as high-resolution ADCs in place of the traditional pipeline. This comes from increases in process technology, allowing for increases in logic speeds in circuits.

The pipeline ADC consists of several notches, where each notch is made up of a sub-ADC, a residue amplifier, and a digital-to-analog converter (DAC). Fig. 2.12 shows a block timing diagram of the pipeline ADC architecture. Circuit operation is divided into sampling and amplification phases. In the amplification phase, the residue signal from the first stage is transferred to the second stage, as shown in the figure. Typically, the residue amplifier is an op-amp with large power consumption. As such, it isn't easy to reduce the power required by the pipeline architecture [52].

The SAR ADC includes a DAC, a sampler, a SAR controller, and a comparator. Compared to the pipeline architecture, the SAR ADC has lower power consumption since

an op-amp is not required. Fig. 2.12 depicts the block timing diagram of the SAR ADC architecture. The circuit operation of a SAR ADC consists of sampling and successive approximation (SA) phases. The input signal is sampled, then the DAC estimates the sampled signal using a binary search algorithm. The period of SA operation is proportional to the number of bits. Therefore, the sampling speed in high-resolution conversion is much slower than the pipeline ADC [52]. A hybrid pipeline SAR ADC has also been developed for higher speed operation. The pipeline SAR architecture consists of a residue amplifier and MSB/LSB SAR ADCs. It has a faster sampling speed than SAR ADCs due to a reduced SA period. The resolution of the first pipeline stage is also increased by SAR, resulting in fewer stages required and lower overall power consumption over the traditional pipeline ADC [53].

High-Speed ADCs

In high-speed ADCs, the Flash ADC is used for ultra-wide-band receivers, though it is primarily used at low resolutions due to increased power consumption at higher resolutions. More recently, the time-interleaved (TI) ADC has been used in wide-band receivers to solve the trade-off between resolution and power consumption. TI ADCs suffer from performance degradation due to channel-to-channel mismatch.

The Flash ADC incorporates comparators and track and hold circuits (T/H). The number of comparators used is $2^k - 1$, where k is the number of bits used in the ADC. Fig. 2.13 illustrates the block timing diagram of the Flash ADC. The amplifier in the T/H block is typically power-hungry. The comparators utilize a large amount of power due to an exponential increase in the comparators' number with an increase in resolution. As such, the Flash ADC is typically used at lower resolutions to achieve lower power. The TI ADC consists of several sub-ADCs, each of which is directly connected to the input signal. In each block, the sampling period is shifted to $1/f_s$ where f_s is the sampling period of the TI ADC. An effective sampling frequency is realized at $f_s = Nf_{sub}$, where N is the number of sub-ADCs and f_{sub} is the sampling frequency. Fig. 2.13 displays the block timing diagram for the TI architecture.

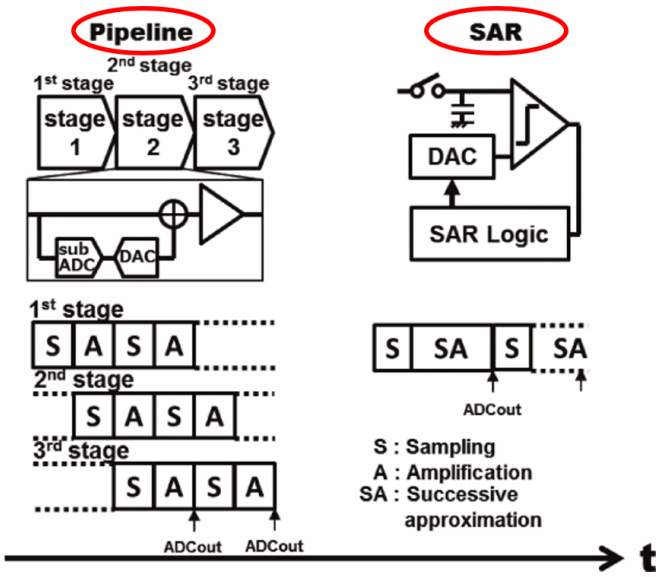


Figure 2.12: Block diagram and timing diagram for high-resolution ADCs [52].

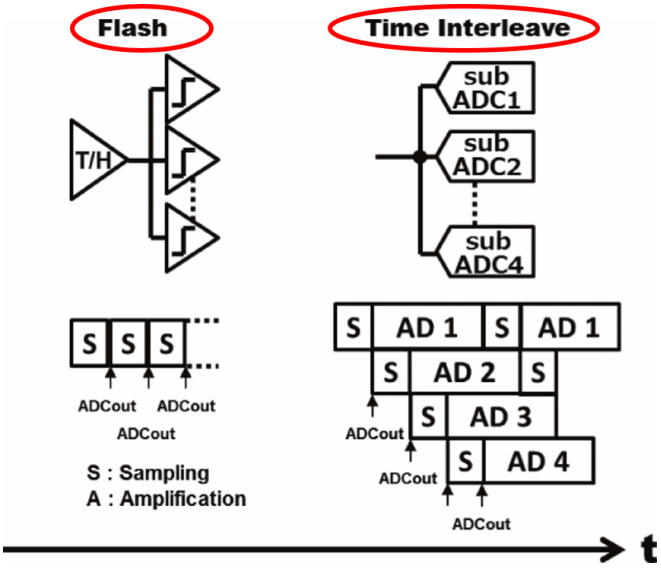


Figure 2.13: Block diagram and timing diagram for high-speed ADCs [52].

Compared to the Flash ADC, the TI architecture can achieve higher resolution due to the relaxation of each sub-block sampling frequency. However, the TI ADC suffers from channel-to-channel mismatch due to offset and gain mismatch. Calibration methods exist for this mismatch in both the digital and analog domains, but that comes with drawbacks of large circuit blocks [54] and increased noise [55].

Voltage Controlled Oscillator (VCO)

A voltage-controlled oscillator (VCO) is an oscillator with a signal whose output may vary over a wide range, controlled by the input DC voltage. It is an oscillator whose output frequency is directly associated with the voltage at its input. The circuit design for a VCO is shown in Fig. 2.14 [56]. The cross-coupled transistors (M1 and M2) are utilized as a compensation for the LC tank's loss, containing L1 and C_{var}. The other cross-coupled transistors (M3 and M4), and C_{rec} are used to rectify a dc voltage, V_{bias}, which is utilized to bias the bodies of M1 and M2 through bias resistor, R. The output oscillation frequency is shown as f_o.

Ring VCOs, are the other topology of VCO with smaller silicon area, larger tuning range, better linearity corresponding to the supply voltage, and easier implementation. The Ring VCO is depicted in Fig. 2.15. It is a regular inverter-based single-ended RO in which their output is connected to a common center node via similar inductors. This framework is symmetric regarding the three phases of the R_O, meaning that the dc current can't run through the center node and the inductors. This design act as an open circuit at multiples of $3f_0$. The frequency of an inverter-based R_O is [57],

$$f_{ring} = \frac{1}{2n\tau} \tag{2.6}$$

where τ is the delay in an inverter, and n is the total number of inverters.

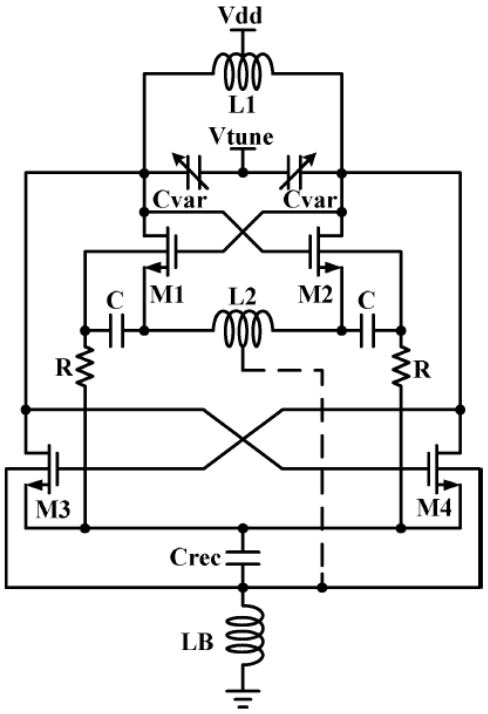


Figure 2.14: Illustration of voltage-controlled-oscillator [56].

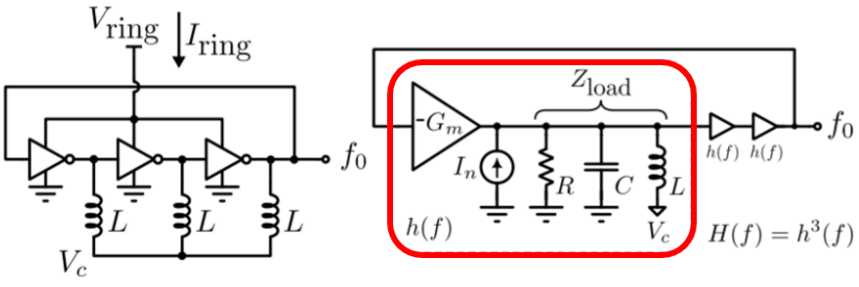


Figure 2.15: Ring VCO with an inductive load and a linear model [57].

Voltage to Frequency Converter

In [58], a frequency proportional to the measured impedance was obtained. A current was periodically sinked and sourced via the impedance. The reference voltage was utilized for switching between charging and discharging mode. In phase one, the current charged the impedance, and the voltage level reached an amount set by the high reference voltage. In the next phase, the voltage decreased due to the current discharging the capacitor. This continued until the voltage reached a minimum set by the low reference voltage. The loop continues, and this creates a periodic signal proportional to the impedance.

Fig. 2.16 depicts the topology of an impedance to frequency converter [58]. When V_{out} is high, ϕ_1 is active, and ϕ_2 is low. Subsequently, I_0 is injected through the electrode. This circuit has some extra switches like ϕ_2 to prevent a short circuit between supply and ground.

The time intervals that take the capacitor to charge and discharge ultimate the output frequency. The electrode potential increases as ϕ_2 close, and I_0 is sourced to it. The voltage of the capacitor is continuously being compared to V_{refH}. Once the voltage meets the high voltage, ϕ_2, opens, and I_0 is sinked, decreasing the capacitor's voltage. To calculate the period of a single charge-discharge cycle, the following equation can be used [58],

$$T = 2\frac{C_e}{I_0}(\Delta V - 2R_e I_0) = 2C_e(\frac{\Delta V}{I_0} - 2R_e) \tag{2.7}$$

where R_e is the resistance and C_e is the cell's capacitance.

Another topology is the temperature to frequency conversion technique, which is shown in Fig. 2.17. The resultant temperature is frequency-modulated where the PTAT signal is converted to temperature through a scaling transistor and current mirror, and then finally charges a capacitor [59].

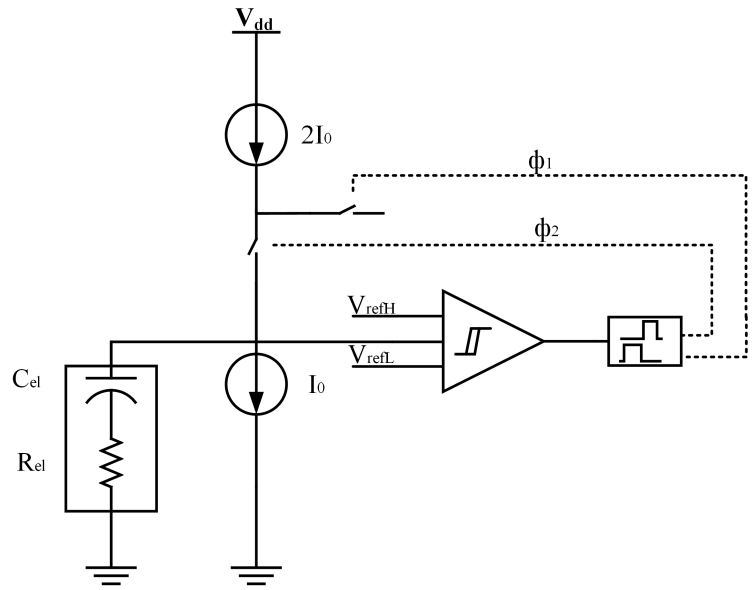


Figure 2.16: Illustration of impedance-to-frequency topology [58].

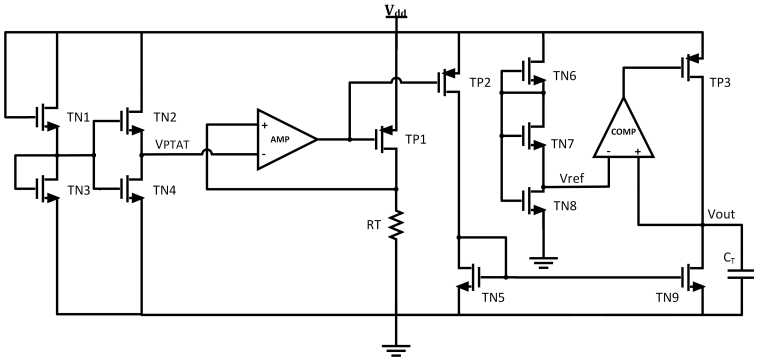


Figure 2.17: Illustration of temperature-to-frequency topology [59].

2.3 Microprocessors

A digital system will need a processor, which will act as a brain in a human body. A microprocessor is an electronic device that plays as a role of CPU to provide the computational in the system. Generally speaking, a microprocessor has built-in arithmetic and logical units, control command sets, instruction processing circuitry, and a memory class. The main function of the microcontroller is to perform calculations, which helps in working a computer.

The microcontrollers are characterized with respect to **bus-width**, **memory structure**, and **instruction set**. The bits in the microcontroller can be divided into 8-bit, 16-bit, and 32-bit. Considering the 8-bit, the ALU performs the arithmetic and logical commands when the internal bus is 8-bit. In contrast to 8-bit, the 16-bit microcontroller performs greater and faster operation than 8-bit. As an example, 8-bit microcontrollers can only use 8 bits, resulting in a final range of 0x00-0xFF (0-255) for each cycle, while 16-bit microcontrollers with its 16-bit data width have a range of 0x0000-0xFFFF (0-65535) [60]. As reported, the memory classifications can be divided as follows,

• **Embedded Memory Microcontroller**: In this category, the system has a microcontroller with all the functional blocks on the same chip.

• **External Memory Microcontroller**: In this category, the system has a microcontroller unit which all the functional blocks are not implemented on the same chip [60].

The microcontrollers are divided into two groups regarding the instruction sets; Reduced Instruction Set Computer (including ARM and MIPS), and Complex Instruction Set Computer (including Intel Pentium and AMD threadripper) [61].

• **CISC**: CISC is a Complex Instruction Set Computer. It permits the user to utilize one instruction in place of numerous less complex instructions. CISC allows users to have a single instruction to access memory. One of the complex tasks which CISC is able to perform, is string searching. Also, they are able to utilize a number of different instruction formats with varying lengths.

• **RISC**: The RISC is a Reduced Instruction Set Computer. It permits each instruction to function on any register or utilize any addressing mode, and synchronous get to the

program and information. Generally speaking, RISC frameworks abbreviate execution time by a reduction in the clock cycles per instruction. In contrast, CISC frameworks abbreviate this time by a reduction in the number of instructions per program. The RISC gives distant better execution performance than CISC [60].

MIPS (Microprocessor without Interlocked Pipeline Stages) is among the most used topologies of RISC processors. In 1984, Stanford University introduced a corporation to industrialize research into MIPS architecture, with various companies soon following suit. Since this time, the MIPS architecture has found its way into CISCO Routers, digital TV, cable modems, and many more household appliances, as a result of its designer-friendly composition [62]. Instruction set architecture is called as ISA in MIPS. Among embedded systems in the industry, MIPS is known as the lowest power consumption system. It was estimated that every third of all RISK chips would be manufactured on a MIPS-based structure because of its good performance. MIPS processor has three main elements; 1. Data path, 2. Controller, and 3. ALU control [63].

One of the elements is **data path**. For an 8-bit MIPS processor, an 8-bit wide data path should be used. The data path is divided into eight symmetric bitslices. In each bitslice, an ALU and a register are used. Since the control signals need to move across the bitslices, a zipper is used to buffer and drive the control signals into the data path.

Another element is the **controller**. It receives several instructions and decodes them to make appropriate control signals. This results in a flow of data in the processor. The controller consists of a controller-pla and aludec. They are built from standard cell libraries such as NANDs, NORs, and inverters [63]. Its duty is to decode the fetched instructions from memory and send the control signals to the data path.

ALU control is the third element. ALU is available at each bitslice. There is one ALU per bitslice. The ALU controller receives ALUOp to send the control signals to the ALU. This results in carrying out the operation. The hierarchical block diagram of the MIPS and its components are shown in Fig. 2.18 [64].

The MIPS instruction sets can be divided into several categories, such as Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Memory Access (MEM), and Write Back (WB).

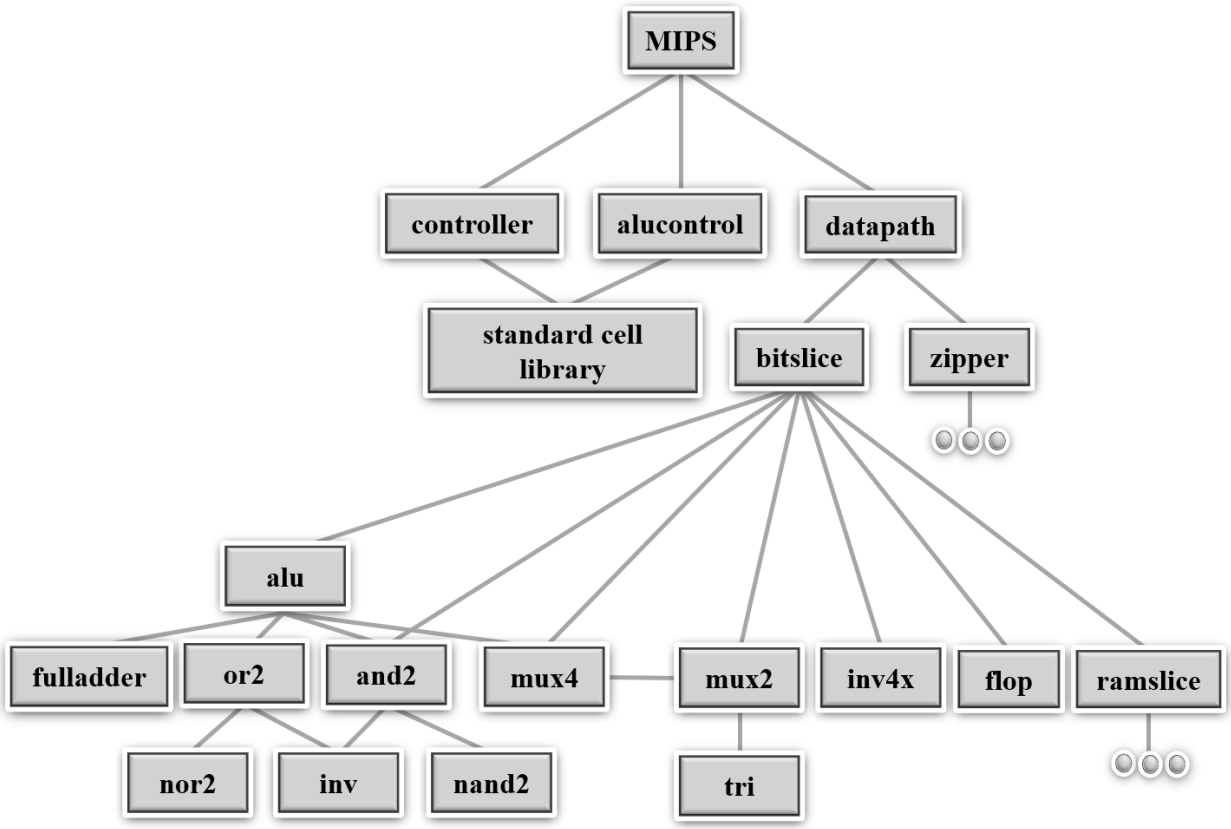


Figure 2.18: MIPS hierarchical design.

These instruction sets use a six-bit operation code to define the action which must be performed by a processor. These actions can be categorized into add, subtract, or load information from memory.

2.3.1 Theory and Designs

In a computer, a high-level programming language gets translated into assembly language with a compiler's help. The next step is to convert the assembly language into a machine language, a binary representation of the instructions.

This is done by formatting the instruction in a specific way to be correctly interpreted, which is called the instruction format. In MIPS, the instruction format has a fixed length of 32 bits. The 32 bits are divided into segments, called fields, which communicates specific information. The fields are divided differently depending on the type of instruction. There are three types of instruction encodings, I-type (for immediate), R-type (for register), and J-type (for jump).

For all instructions, the first 6 bits are the opcode, which distinguishes the type of instruction. For J-type instructions, the remaining bits are used for the target address. For I-type and R-type instructions, the next 5 bits denote the first register, and the 5 bits after that denote the second register. The remaining bits for the I-type instructions denote the address/immediate. The remaining bits for the R-type instructions are separated as follows, 5 bits describe the destination register, 5 bits describe the shift amount, and the last 6 bits describe the function code. The function code describes the specific variant of the instruction.

I-type instructions are responsible for load and store operations that move data between the registers and memory, called data transfer instructions. These instructions are the only instructions that have access to memory; all of the other operations are performed within the registers. Registers are built-in memory locations within the CPU, while memory is located outside of the CPU. Memory is a large, one-dimensional array where the index is called the address. In the 8-bit version of MIPS, there are eight general-purpose registers. Although memory stores a larger amount of data than registers, the CPU can operate on registers faster. I-type instructions also add immediate instructions, where one operand of

the instruction is an immediate or a 16-bit constant. Because constants frequently occur in computer programs, this instruction allows for a much faster operation than loading a constant memory. The constant zero plays such an important role in the MIPS instruction set that register $zero is hardwired to be the constant zero. Other I-type instructions include conditional branches; branch if equal and branch if not equal. In conditional branches, two values are compared, and the transfer of control to a new address in the program depends on the outcome of the comparison [64]. These two instructions are responsible for decision making on a computer.

R-type instructions are used for arithmetic operations. All arithmetic operations are performed within the registers. Some examples of arithmetic operations include add, subtract, bit shift left, bit shift right, logical AND, OR, NOT, or set less than (to see if a variable is less than another variable).

J-type instructions are used to jump to a specified address. These instructions are unconditional branches, meaning the processor always follows that branch. To implement a switch statement in a program, MIPS uses a jump address table or jump table. A jump table is a table of addresses corresponding to labels in code that a program can index into and then jump to an alternative instruction sequence. A procedure is a stored subroutine that performs a task with the provided parameters and returns to the point of origin with a result. The jump-and-link instruction is a J-type instruction specifically used for procedures; it jumps to an address while simultaneously saving the next instruction's address in register $ra (register 31). This address is called the return address and allows a procedure to return to the proper address. MIPS also has a jump register instruction which jumps to the address specified in $ra.

As described before, MIPS instruction encodings contain a field for addresses or immediate. In immediate addressing, this field contains a constant. However, MIPS uses different addressing modes, or multiple forms of addressing, to account for 32-bit immediate operands or 32-bit addresses that cannot fit within this field. Register addressing uses a register to hold the operand. Base or displacement addresses load an operand from memory whose address is the sum of a register and a constant instruction. PC-relative addressing uses the sum of the program counter (which holds the current instruction) and a constant

in the instruction to form the branch address. Lastly, pseudo-direct addressing forms the jump address by using the 26 bits of the instruction concatenated with the upper bits of the PC [64]. A high-level view of how MIPS works can be seen in Fig. 2.19 [64]. To implement the instructions, first, the PC is sent to the memory location to fetch the instruction, and the instruction is read from the registers. The arithmetic-logical unit (ALU) is then used for all instructions except jump. The ALU is used for address calculations (load and store instructions), operation execution (arithmetic), and comparisons (branch). The ALU result is written to a register if it is an arithmetic-logical instruction, used as an address if it is a load or store instruction (and written into the register file), or used to determine the next instruction address for branch instructions. This describes the datapath of the architecture. The control unit decides how to set the control lines based on the instruction. In other words, it controls the datapath. In Fig. 2.19, the datapath is in black, and the control path is in orange. By splitting up different instructions into separate stages of the architecture, a quasi-parallel processing structure evolves to accelerate the simultaneous handling of multiple tasks. While the specifics may vary between processors, MIPS generally includes a stage for instruction fetch, instruction decode, execution, memory, and write back. By pipelining these five stages, the processor can simultaneously handle five instructions in a single clock cycle. For example, given instructions A and B, the processor could compute in the same clock cycle the instruction decode for A and B's execution. After completing one step, the process is forwarded to the next stage, and the pattern propagates through [65].

ARM Cortex M0 is a high performance and energy-efficient ARM processor. It is designed to be cost-sensitive and power-constrained solutions for a vast range of devices. The Cortex M0 processor is the smallest among all of the cores in ARM. If the license fee is a matter, open-source processors such as MIPS can be considered. Although ARM is currently the most popular RISC ISA, it is very similar to MIPS. They have a similar core of instruction sets. The main difference is that MIPS has more general-purpose registers, while ARM has more address modes [64]. Having more addressing modes allows for more flexible access to memory but increases complexity and power. On the other hand, MIPS is attractive for its ultra-low power consumption (the architecture is also open-sourced and

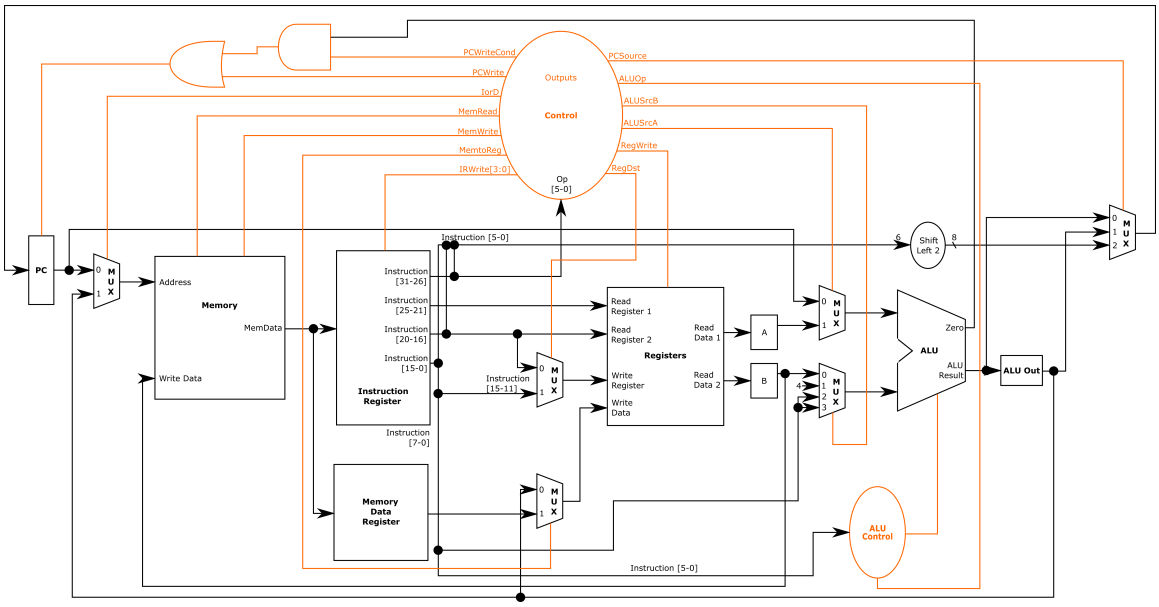


Figure 2.19: 8-bit MIPS block diagram.

well documented). Due to its relatively simple design, it is a good base MCU design for an ASIC. The main differences between MIPS and ARM are [66],

1. **Power vs. Performance:** Generally speaking, simple instructions consumes less power. Those processors are designed for high-performance applications like servers, while RISC processors are used in mobile applications, and they are simpler. Their performance compromised for better power efficiency. Every day in the news, we can see an improvement over these processors. For example, ARM added more complexity to its instructions to get better performance, and Intel changed its opcodes into micro-ops, which are the same as ARM to get better power. Among all, MIPS uses the simplest ISA, and its application is with embedded designs where the low power consumption is needed.

2. **Security and Virtualization:** ARM and Intel have some additional option called TrustZone and vPro. Their application is for hardware security. ARM and Intel have support for virtualization and memory management, and the main difference is the implementation. Generally speaking, deploying fewer instructions and addressing modes will result in less complexity in the instruction decoder, the addressing logic, and the execution unit. Therefore, the system will be clocked faster because of less work in each clock period. Processors have much faster speed than the memories. For example, a processor clocked at 100 MHz would like to get to the memory in 100 ns. But at some point, the memory combined with the processor needs a time of 60 ns for access. So, the processor has a gap, waiting during each memory access, which results in wasting execution cycles. To overcome this problem and reduce the number of accessing to the main memory, adding instruction and data cache to the processors might be helpful. A cache is a kind of high-speed RAM where data and their specific addresses are stored. The cache will be read at the first stage, every time the processor tries to read the main memory data. This is because of saving time. When the address is not found in the cache, it takes the full access time to store the data. According to the results, the cache is ten times faster than the main memory.

SiFive standard cores are the foremost silicon-deployed RISC-V arrangements within the world. From low-power microcontrollers to multi-core application processors, this IP has better security and the most straightforward way to RISC-V. SiFive standard cores are customizable and can be tuned to meet the exact needs of the SiFive center originator.

Generally, it consists of three cores; E cores, S cores, and U cores. E cores are 32-bit embedded cores with MCU, edge computing, AI, and IoT. S cores are 64-bit embedded cores with storage, AR/VR, and machine learning. U cores are 64-bit application processors with the application of Linux, data center, and network base-band [67]. For MCU's application, E series can be used, comprising the 32-bit E76 and E76-MC, and provides hard real-time capabilities.

For open-source example, in [68], an ultra-low voltage (ULV) microcontroller is presented based on MSP430 architecture. They employed several methods to overcome design challenges specific to ULV operation. They used a dual Vdd, multi-threshold voltage partitioning in the LP/GP process mix to enable each system block's operation close to its minimum-energy point under the 25-MHz timing constraint [68]. An all-digital adaptive voltage scaling system (AVS) is employed to reduce speed due to PVT variations. A multi-threshold voltage clock tree and a standard-cell library with upsized gate lengths are used to ensure robust operation.

Roy implemented a 16-bit MSP430 architecture in a custom 90 nm xLP FDSOI process. This custom process technology was optimized for near and subthreshold operation by providing transistors with reduced threshold voltage variation and lower subthreshold leakage. The result was an MSP430 implementation that consumes less energy [69]. Besides that, Bhadra and his team implemented an asynchronous MSP430 microprocessor that offered over $\times 10$ reduction in power consumption compared to the synchronous design. They achieved this by using asynchronous finite state machines (AFSMs) and relative timing technology [70].

2.4 Conclusion

Considering the literature, ISFET, as a potentiometric pH sensor, is reviewed. The mechanism of ISFET's operation with integration in CMOS technology is discussed, and several readout circuits and different applications are considered. In the second part, several readout circuits for converting an analog signal to digital are illustrated. In agreement with the references, the quasi digital technique is prioritized due to the simplicity, low

power, and small area. In microcontrollers, power consumption and accuracy are of great interest. Different kinds of microcontrollers with their advantages and disadvantages are discussed. The RISC version would be preferable among all those microprocessors because of the simplicity and less power consumption.

Chapter 3

Differential pH Sensor

Portions of this section are published in,

"A Portable CMOS Based pH Sensor," IEEE International Midwest Symposium on Circuits and Systems, Springfield, MA, USA, pp. 525-528, Aug 2020.

"A Differential Low-Power Voltage-Clamped ISFET Topology for Biomedical Applications," IEEE Dallas Circuits and Systems Conference, Dallas, TX, pp. 1-4, Nov 2018.

3.1 Single ISFET

To verify the I-V characteristics and determine parameters of an ISFET, a chip with ISFET transistors of varying sizes was fabricated. Figures 3.1, and 3.2 shows the experimental setup. A micropipette was utilized for applying different solutions directly to the chip area. For this experiment, three different buffer solutions, pH=4.0, pH=7.0, and pH=10.0, were used. Gold wire was used as the reference electrode when in contact with the solution. For electrical testing measurements, the Keithley semiconductor characterization system was utilized. In this experiment, V_{DS} was set to 1 V. The sensing area of the fabricated transistor is $10\mu m \times 10\mu m$. By applying the solutions on the area, the passivation layer capacitance per unit area was calculated as 0.00287 $\frac{fF}{\mu m^2}$. This is in line with the estimated capacitance per unit area of 0.00226 $\frac{fF}{\mu m^2}$, which was extracted from a combination of using theoretical equations and I-V characteristics of fabricated ISFETs (Fig. 3.3).

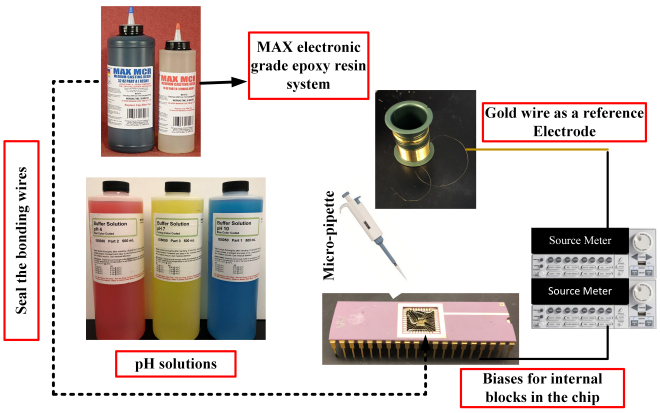
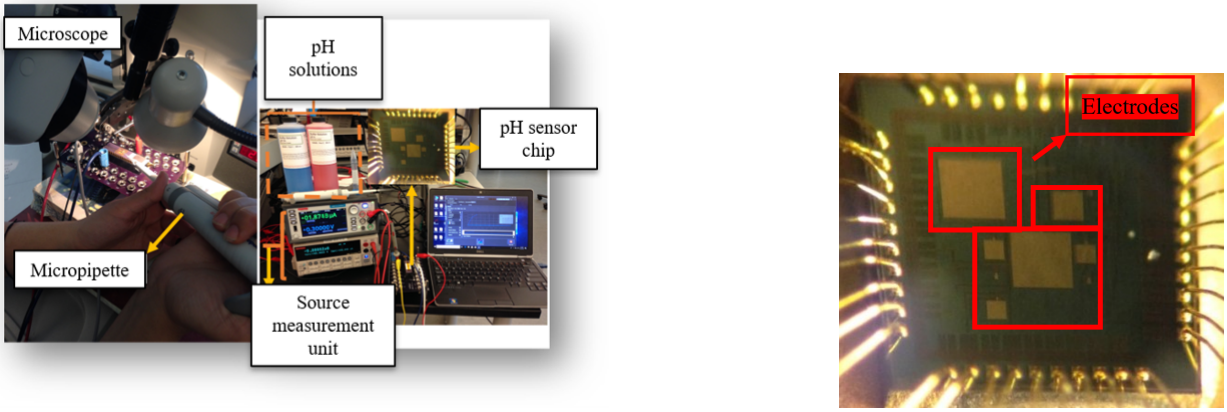


Figure 3.1: The chip is in a cavity in the ceramic package. Bond-wires are sealed using epoxy.



(a) **(b)**

Figure 3.2: (a) Experimental testing for representing I-V characteristics of an ISFET. (b) Fabricated chip in 0.5 μm CMOS technology.

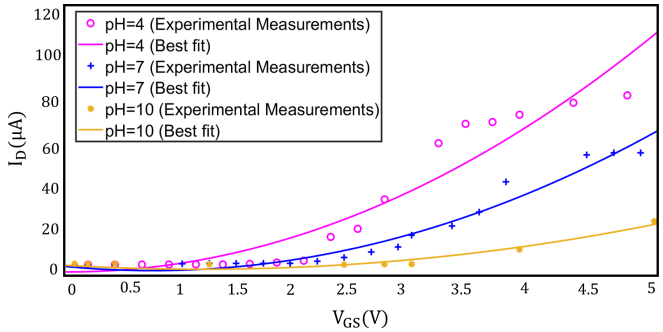


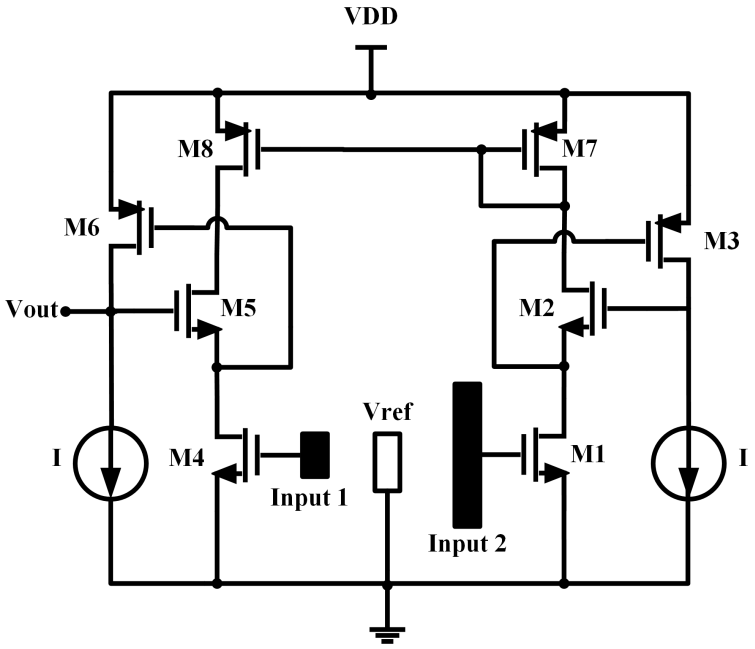
Figure 3.3: I-V characteristics for a fabricated CMOS ISFET.

As shown, the I-V characteristic of an ISFET is the same as a MOSFET, and this is proof that ISFETs characteristics are the same as MOSFETS.

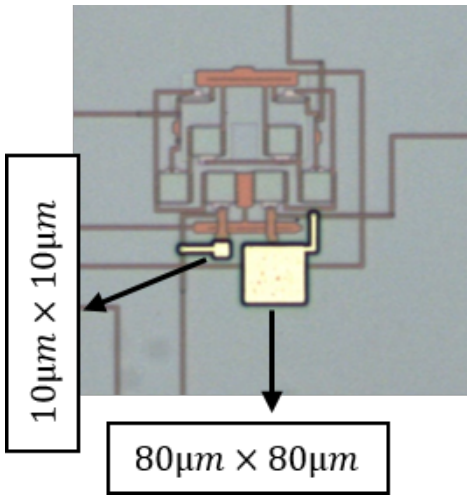
3.2 A Differential Voltage-Clamped ISFET Topology

A differential voltage-clamped pH sensor with different electrode gate areas is shown in this part. One of the parameters which affect the sensitivity is the size of the top metal layer in ISFET. Numerous executions require specialized processing and steps to fabricate the ion-sensitive layers and electrodes. An ISFET can be made native to the CMOS process without a need for post-processing, essentially utilizing the top metal connection to the gate and making a floating gate terminal. This truth can be utilized to eliminate the requirement for expensive and/or time-consuming post-processing method [71, 72].

Two techniques, voltage clamping, and two different sensing gate areas were utilized in this circuit. Differential readout can eliminate common-mode noise improving the accuracy. The design can measure pH either as current or voltage. By applying a fixed voltage to the V_{ref} and making the source of the ISFET grounded, the drain voltage of the ISFET is fixed and clamped at a constant potential. The drain current of the ISFET corresponds to the ion changes in the solutions near the top metal connected to the gate of transistors M1 and M4. The proposed circuit design is shown in Fig. 3.4a. Electrodes with two different sizes (10 μm$\times$10 μm and 80 μm$\times$80 μm) were used. This is shown in Fig. 3.4b. Two sets of the transistor pairs, ((M2 and M3) and (M5 and M6)) perform the voltage clamping. M3 is biased utilizing a constant current source, which is implemented by current mirrors. The drain voltage of the ISFET is fixed. Therefore the pH changes will cause changes in the drain current of the ISFET. Since this circuit was designed for biomedical applications, the MOSFETs were selected to work in the sub-threshold region. This helps the circuit to operate with lower power. The output voltage and current are as follows,



(a)



(b)

Figure 3.4: (a) Proposed differential voltage-clamped ISFET pH sensor. (b) Photomicrograph of the fabricated chip in 0.5 μm CMOS technology.

$$V_{out} = -2.3\alpha U_t pH \tag{3.1}$$

$$I_{out} = I_{D0} \times \frac{W}{L} \times exp\frac{V_{GS}}{nU_t} \times (1 - exp\frac{-V_{DS}}{nU_t}) \tag{3.2}$$

Where V_{GS} and I_{D0} are,

$$V_{GS} = \frac{C_{pass}}{C_{pass} + C_{eox}} \times (V_{Ref} - (\gamma + 2.303\alpha U_t pH)) - V_s \tag{3.3}$$

$$I_{D0} = \mu_n C_{ox}(n-1)U_t^2 \times exp\frac{-V_{thISFET}}{nU_t} \tag{3.4}$$

This design is intended to be used in biological applications (such as real-time cell culture monitoring). In these applications, the temperature is ordinarily kept decently steady, and circuit varieties are not a noteworthy concern due to temperature changes. In this design, α = 95 and γ=-324 mV. The bias current is 0.5 nA, which is above the transistors' noise level in the current mirror, and the supply voltage is 0.9 V. M4, M6, M7, and M8 have the aspect ratio of 10/10. M2 and M5 have an aspect ratio of 1.5/10.

3.2.1 Simulation and Experimental Results

According to the results, the proposed differential ISFET pH sensor has low noise, low power, and high sensitivity without extensive CMOS post-processing. The sensor was designed in 0.5 μm standard CMOS technology. Figure 3.5 shows the transient response of the output voltages for pH 1-14 in simulation and experimental. The pH and the corresponding voltages are shown in Table 3.1. The sensitivity is a function of the electrode gate areas $(dV_{out}/dpH) \propto A$ (A is the sensing gate areas). With an increase in pH, the output voltage decreases. Because the ISFETS moving their region of operation as their input voltage changes, there is some non-linearity in the plots. With transistors' operation in subthreshold regions, the sensor consumes a power of 2.3 nW with 0.9 V of the supply voltage. The area of this chip is estimated as 0.0093 mm^2. The sensitivity of this circuit is about -49 mV/pH, which is shown in Fig. 3.5c. The comparison between this design and the state of arts is shown in Table. 3.2.

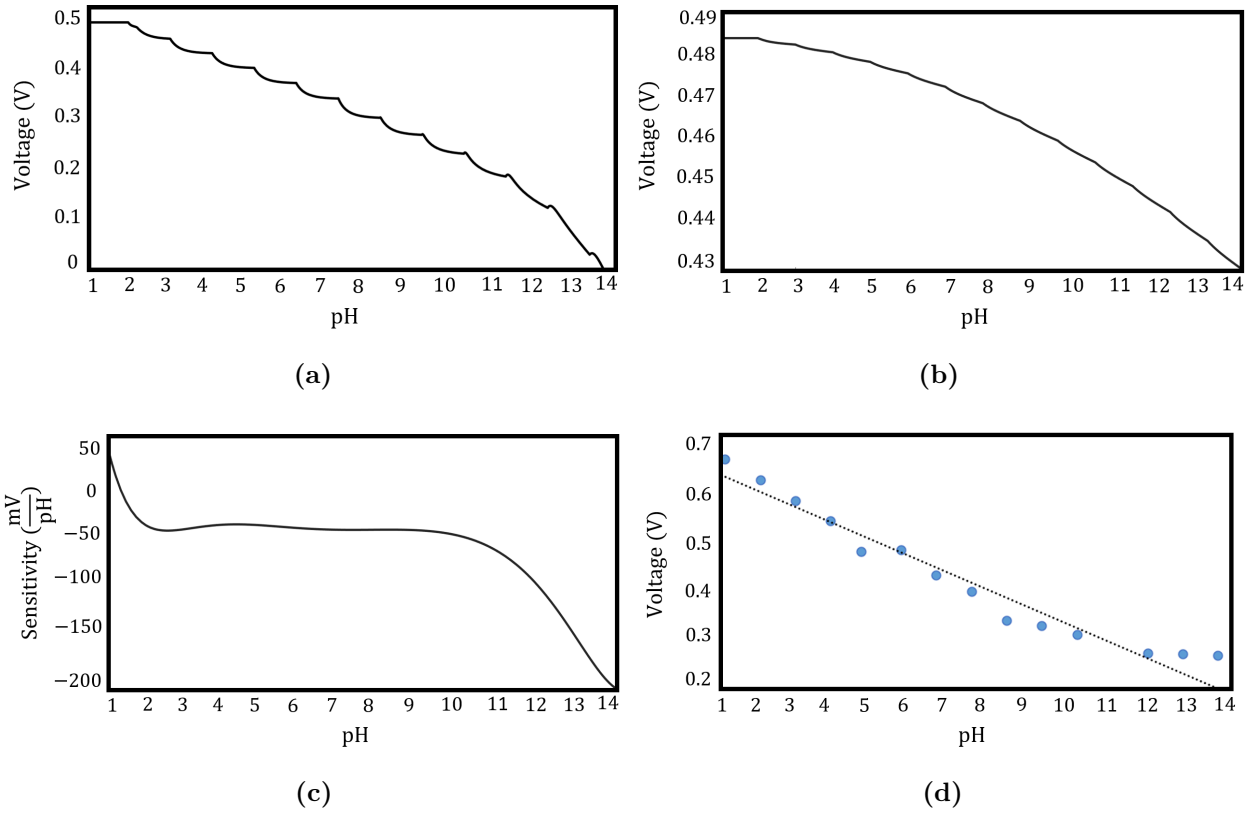


Figure 3.5: Simulation and experimental results for the proposed differential ISFET sensor (a) V_{out1}. (b) V_{out2}. (c) Differential ISFET Sensitivity. (d) Experimental results for differential output voltage.

Table 3.1: Voltage and corresponding pH for differential output.

pH	Input voltage (mV)	pH	Input voltage (mV)
1	110	8	510
2	160	9	570
3	210	10	630
4	270	11	690
5	330	12	750
6	390	13	810
7	450	14	870

Table 3.2: Comparison with state of the art.

	[17]	[25]	[35]	[39]	[71]	[73]	This Work
Year	2004	2015	2017	2020	2016	2018	2018
Technology (nm)	600	180	350	180	180	350	500
ISFET Topology	Differential	Dual-mode pixel	Voltage clamped	Differential	Differential	Translinear	Voltage clamped
pH Range	6 pH units	1-14	4-10	5.5-10.5	1-14	6.6-8.6	1-14
ISFET Sensitivity (mV/pH)	43	26.2	-44.5	25.7	50	-	-49
Power	2.1 mW	105.6 mW	2.5 nW @ pH=7	0.72 nW	31.3 μW	16.6 μW	2.3 nW
System Area (mm^2)	18.22	12.5	-	0.85	0.0064	3.74	0.0093

3.2.2 Portable Differential Voltage-Clamped ISFET Sensor

An analog signal can be digitized and then processed by a microcontroller for a complete readout system. The full system needs an analog front-end (AFE), analog to digital converter (ADC), and a digital back-end. The bio-signal is sensed and detected by the AFE. For further analysis, the signal is digitized by ADC and processed for further applications such as wireless transmission. The digitized signal can be transmitted to a central radio station where the transmitter and receiver are employed to propagate and intercept the radio waves.

This section presents the design and experimental measurements of a portable pH measurement system based on a differential voltage-clamp topology. Fig. 3.6 depicts the system overview. Recently Karolcik and his team implemented a portable system with display [74]. Also, Cacho and his team demonstrated a portable ISFET platform for point of care (PoC) diagnosis [75]. They used a custom cartridge and a Raspberry Pi to interface with the system. This benefited their system for configuration and biasing. According to the proposed design in the previous section, the front-end differential circuit eliminated the need for expensive post-processing of a reference ISFET by utilizing two ISFETs with different top metal electrodes. The voltage clamping circuit is made of transistors (M2-M3) and (M5-M6). M3 and M6 were biased with a constant current source, implemented in practice by a resistor and current mirror. Therefore, the drain voltage of the ISFET is fixed, and the drain current (I_{out}) of the ISFET corresponds to the ion changes in the solutions near the top metal electrodes (transistors M1 and M4). Transistors M1, M2, M4, M5, M7, and M8 have an aspect ratio of $10\mu m/10\mu m$, and transistors M3 and M6 have an aspect ratio of $1.5\mu m/10\mu m$.

The output of the front-end sensor is connected to an Analog Devices instrumentation amplifier (AMP03). An op-amp (TLC272), which functions as a buffer and trims the offset voltage, transfers the output voltage to the ADC (ADC0801) with a 1 kΩ resistor. For utilizing a microcontroller to convert the output voltage to a pH and display it on an LCD, an Arduino Uno with a 5 V supply was used. R1 and R2 were implemented as off-chip resistors. RG, R3, and R4 are all 1 kΩ resistors. The design was implemented on the PCB board, which is shown in Fig. 3.7.

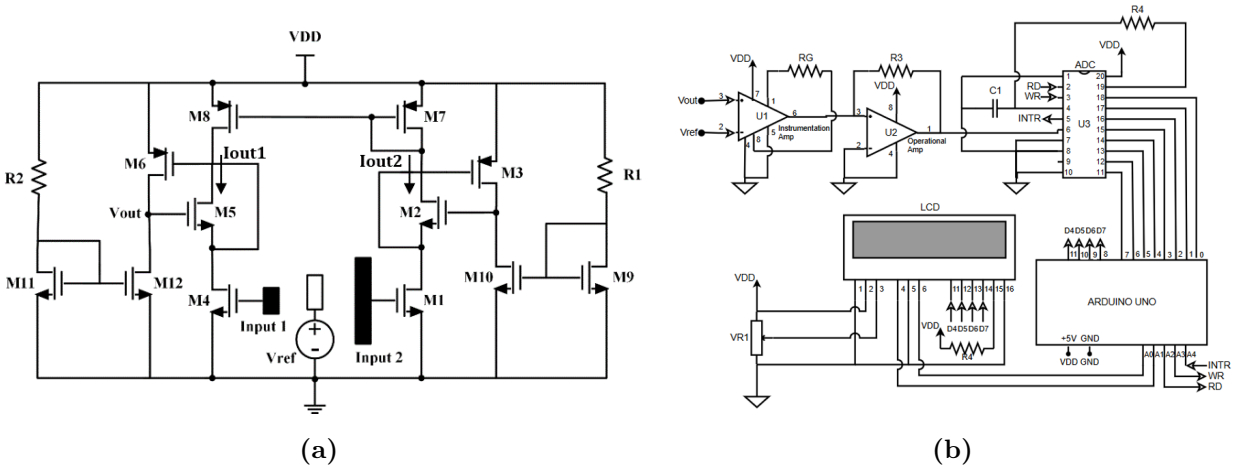


Figure 3.6: (a) The front-end relies on two different top metal electrode sizes and a differential voltage-clamp topology. (b) The output is amplified, buffered, digitized, and displayed.

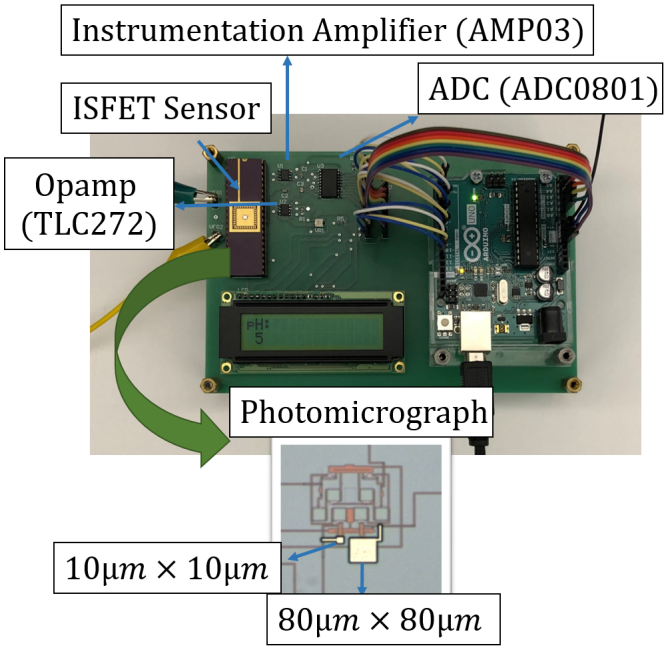


Figure 3.7: Picture of the full portable pH sensing system.

The current in transistors M_1 and M_7 are,

$$I_{out2} = \frac{1}{2}K_{n_1}(Input2 - V_{TN})^2 \tag{3.5}$$

$$I_{out2} = \frac{1}{2}K_{p_7}(V_{GS_7} - V_{TP})^2 \tag{3.6}$$

Equating the currents gives,

$$(V_{GS_7} - V_{TP})^2 = \frac{K_{n_1}}{K_{p_7}} \times (Input2 - V_{TN})^2 \tag{3.7}$$

The currents in M_4, M_5, and M_8 are,

$$I_{out1} = \frac{1}{2}K_{n_4}(Input1 - V_{TN})^2(1 + \lambda_4 V_{G_6}) \tag{3.8}$$

$$I_{out1} = \frac{1}{2}K_{n_5}(V_{out} - V_{G_6} - V_{TN})^2(1 + \lambda_5(V_{D_8} - V_{G_6})) \tag{3.9}$$

$$I_{out1} = \frac{1}{2}K_{p_8}(V_{GS_8} - V_{TP})^2(1 + \lambda_8(V_{D_5} - V_{DD})) \tag{3.10}$$

The gate of M_6 which is the drain voltage of M_4 is,

$$V_{G6} = \frac{2I_{out1}}{\lambda_4 K_{n_4}(Input1 - V_{TN})^2} - \frac{1}{\lambda_4} \tag{3.11}$$

Since $V_{GS7} = V_{GS8}$, the output voltage is,

$$V_{out} = \sqrt{\frac{K_{n1}(Input2 - V_{TN})^2(1+\lambda_8(V_{D_8} - V_{DD}))}{K_{n_5}(1+\lambda_5(V_{D_8} - \frac{2I_{out1}}{\lambda_4 K_{n_4}(Input1 - V_{TN})^2} + \frac{\lambda_5}{\lambda_4}))}} + V_{TN} + \frac{2I_{out1}}{\lambda_4 K_{n_4}(Input1 - V_{TN})^2} - \frac{1}{\lambda_4} \tag{3.12}$$

where K_n and K_p are the transconductor parameters, $V_{TN/TP}$ is the threshold voltage, λ is the channel length modulation parameter, V_{GS} is the gate to source voltage, and V_D is the drain voltage. Input1 and Input2 are functions of the electrode area and the pH (i.e. V_{FG} from equation (3.13)).

$$V_{FG} = \frac{C'_{pass} \times A}{C'_{pass} \times A + C_{eox}} \times (V_{Ref} - V_{Chem}) \tag{3.13}$$

where C'_{pass} is the passivation layer capacitance per unit area, A is the area of the top metal, C_{eox} is the oxide capacitance, and V_{ref} is an externally supplied reference voltage.

3.2.3 Simulation and Experimental Results

The simulation and experimental results of a portable pH sensor established by differential voltage clamping are presented. The ISFET sensor consumes a power of 12 μW with a sensitivity of 42 mV/pH and 80 μW with a sensitivity of 71 mV/pH for two supply voltages of 2 V and 5 V, respectively. The simulation and experimental results are in agreement with each other. The USB powered sensor has a power of 100 mW with an area of $10cm \times 16cm$. The entire setup costs less than $20, which is inexpensive. By implementing the processor and the front-end sensor on the same chip, the price can be further reduced (to less than $1/chip) suitable for environmental and biomedical applications.

The pH sensor front-end was fabricated in 0.5 μm CMOS technology. A Keithley source meter was used to sweep the input voltages for testing three different chips. The differential structure was electrically characterized from 0 to 2 V, the entire power supply range. For initial measurements, Input2 was kept constant at 1.5 V, while Input1 was swept from 0 to 2 V. Then, Input2 was swept from 0 to 2 V, and Input1 was kept constant. This experiment indicates that one of the electrodes has been made insensitive to pH. Simulation and experimental measurements are shown in Figs. 3.8 and 3.9.

The design utilized two different sizes of electrodes. To consider the effects of the two electrodes at the same time, the inputs were swept simultaneously with different voltages. The supply voltage was 2 V and V_{ref} was 0.9 V. Input1 was swept from 431.3-1110.55 mV, and Input2 was swept from 449.3-1157.31 mV to cover the pH 1 to 14 range (Fig. 3.10). The values of the voltages and the corresponding pH are shown in Table 3.3. This experiment also used VDD=5 V and V_{ref} of 0.9 V (Fig. 3.11).

The output voltage from this chip was sent to the instrumentation amplifier, ADC, and finally, the microcontroller to be depicted on an LCD. This portable PCB board has the total area of $10\,cm \times 16\,cm$ with the fabricated ISFET of 0.0093 mm^2. Instead of using the laptop's USB connector, we can use a 6 VDC battery (A544, Alkaline, Button, 140 mAh) with a 4.5 hours lifetime. Stanford Research Systems model (SR785) two-channel dynamic signal analyzer was used for the noise measurement showing an average of 27 nV/$\sqrt{Hz}$ in the 10 Hz to 100 kHz frequency range.

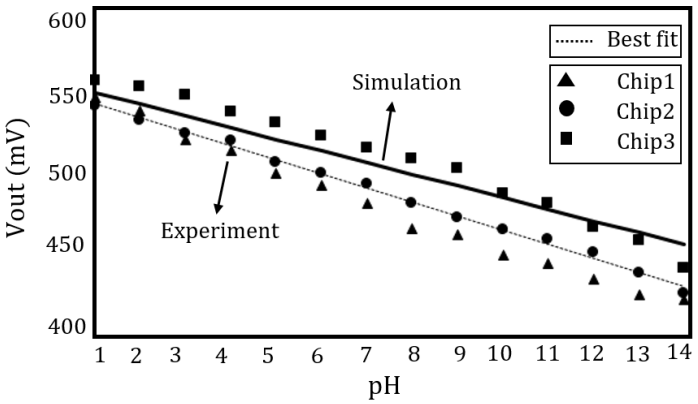


Figure 3.8: Sensor front-end for varying V_{FG_1}. VDD=2 V, Vref=0.9 V, V_{FG_2} = 1.5 V.

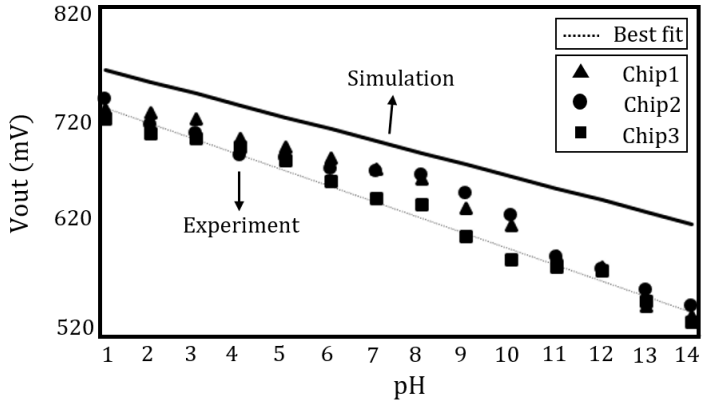


Figure 3.9: Sensor front-end for varying V_{FG_2}. VDD=2 V, Vref=0.9 V, V_{FG_1} = 1.5 V.

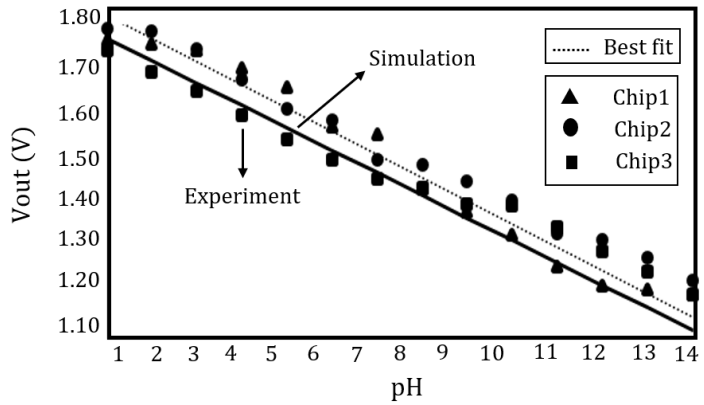


Figure 3.10: Simulation results versus experimental results for Vdiff of two different sizes of gate electrodes ($10\mu m \times 10\mu m$ and $80\mu m \times 80\mu m$) in three different chips (VDD=2 V, Vref=0.9 V).

Table 3.3: Voltage and corresponding pH.

pH	Input1 (mV)	Input2 (mV)	pH	Input1 (mV)	Input2 (mV)
1	1110.55	1157.31	8	744.8	776.16
2	1058.3	1102.86	9	692.55	721.71
3	1006.05	1048.41	10	640.3	667.26
4	953.8	993.96	11	588.05	612.81
5	901.55	939.96	12	535.8	558.36
6	849.3	885.06	13	483.55	503.91
7	797.05	830.61	14	431.3	449.46

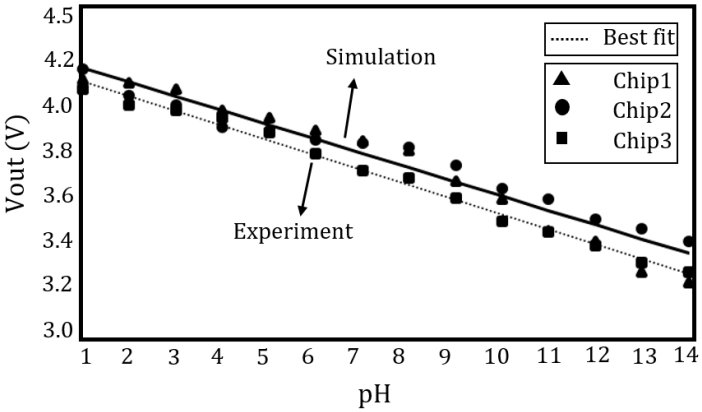


Figure 3.11: Simulation results versus experimental results for Vdiff of two different size of gate electrodes ($10\mu m \times 10\mu m$ and $80\mu m \times 80\mu m$) in three different chips (VDD=5 V, Vref=0.9 V).

Finally, the comparison between this design and state of the art is shown in Table 3.4. This design is a prototype of a portable pH sensor utilizing a voltage-clamp technique combined with different gate electrodes sizes. The proposed design is cost-effective due to the elimination of the post-processing method. The front-end sensor was fabricated in a 0.5 μm CMOS process. The power consumption is 12 μW with a supply voltage of 2 V and 80 μW with a supply voltage of 5 V. The sensitivity for the supply voltages as mentioned earlier is 42 mV/pH and 71 mV/pH, respectively. The designed chip is 0.0093 mm^2, which is more area efficient in comparison to others. With the pH ranges of 1-14, this design is suitable for a wide range of applications.

3.2.4 Experimental Verification with Standard pH Buffer Solutions

Since the fabricated IC was packaged, we first sealed it to protect it against the solutions. Epoxy resin (epoxy experts, max epoxy systems) was used for this process. Next, experimental verification with three buffer solutions (pH=4, pH=7, and pH=10), were performed. The pH buffer calibration kit was purchased from Innovative Science. Before starting the actual test, we verified the pH solutions using the Fisherbrand accumet AB15 pH meter. The measured values are shown in Fig. 3.12. The result of applying pH solutions on the chip is shown in Fig. 3.13. With VDD=2 V, the average voltage for pH 4 is 0.914, for pH 7 is 0.894, and for pH 10 is 0.816. Also, with VDD=5 V, the average voltage for pH 4 is 3.86, for pH 7 is 3.67, and for pH 10 is 3.3.

Table 3.4: Comparison with state of the art.

	[24]	[25]	[31]	[42]	[72]	[73]	[74]	This Work
Year	2006	2015	2019	2020	2017	2018	2019	2020
Technology (nm)	350	180	180	180	130	350	350	500
Topology	CVCC	Dual-mode pixel	Differential	Averaging pixel	Differential	Current mode	Current mode	Differential voltage-clamped
pH Range	2-12	1-14	4-10	-	1-14	6.6-8.6	1-14	1-14
Sensitivity	51.7 (mV/pH)	26.2 (mV/pH)	11.78 (%/pH)	166.5 (mV/pH)	35 (mV/pH)	-	1.03 (μA/pH)	42 (mV/pH) @Vdd=2V 71 (mV/pH) @Vdd=5V
Front-End Power	50 μW	-	61 μW	36 nW	1.2 μW	16.6 μW	-	12 μW @Vdd=2V 80 μW @Vdd=5V
Front-End Current	100 μA	-	1 μA	-	1 μA	10 nA	200 μA	6.4 μA @Vdd=2V 16.2 μA @Vdd=5V
System Power	-	105.6 mW	-	2.9 μW	-	-	660 μW	100 mW
Area (mm^2)	0.85	12.5	4	1.17	0.0128	3.74	1.06	0.0093+1.6
Complete System	No	Yes	Yes	Yes	No	No	Yes	Yes

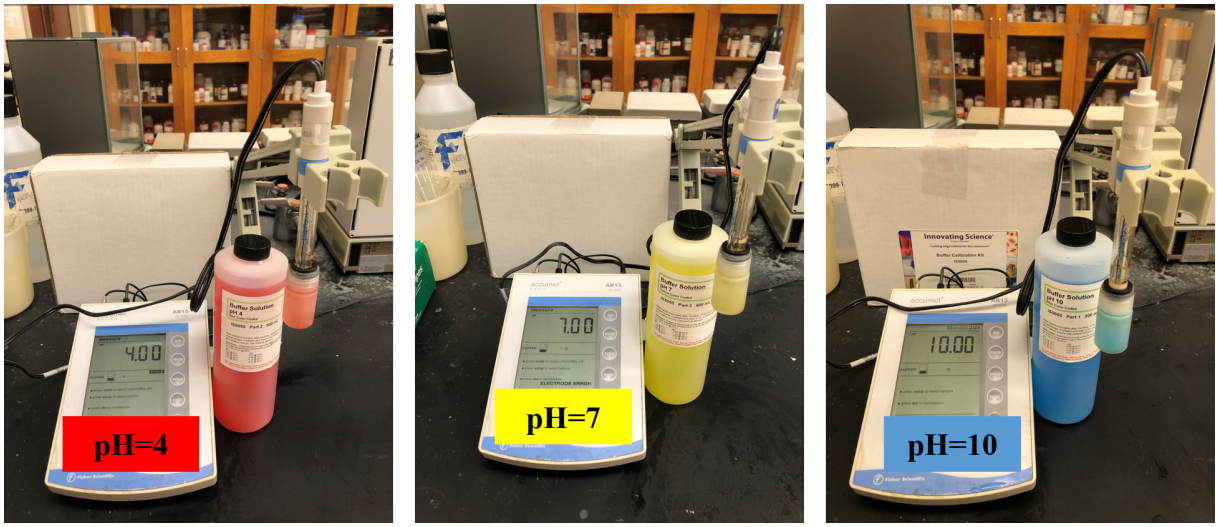


Figure 3.12: Commercial pH meter to verify the pH of the buffer solutions.

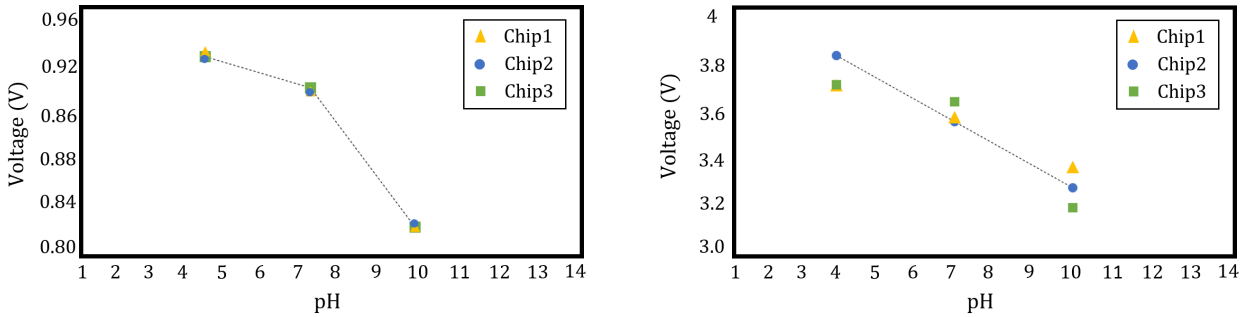


Figure 3.13: Experimental verification with standard pH buffer solutions on differential voltage-clamped circuit design, tested on three different chips with two supply voltages, (a) VDD=2 V. (b) VDD=5 V.

Chapter 4

Low Power Single Ended pH Sensor

Portions of this section are published in,

"ISFET Digital Readout Circuit with an on-Chip MIPS Processor," IEEE Sensors, Rotterdam, Netherlands, Oct 2020.

"A Low-Power Voltage-Clamped CMOS pH to Frequency Sensor," IEEE International Symposium on Circuits and Systems, Sapporo, Japan, pp. 1-5, May 2019.

4.1 A Low-Power Voltage-Clamped CMOS pH to Frequency Sensor

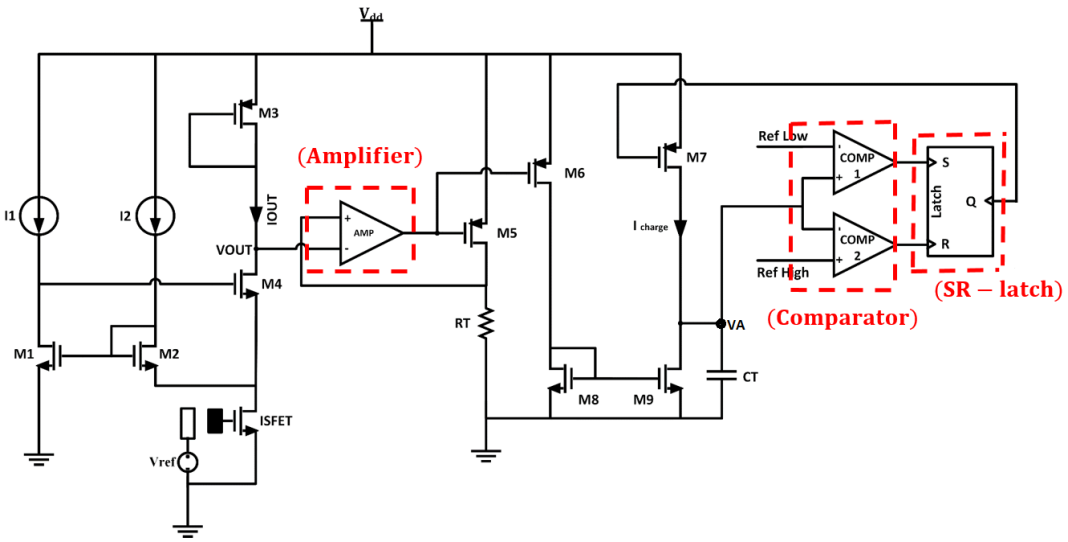
As discussed in the previous section, we want a digital signal for further processing, calibration, and illustrating on an LCD. There are various methods to convert the sensor information to some characteristics such as phase, frequency, and magnitude. After extracting output voltage from the sensor, it will get digitized utilizing techniques such as the implementation of voltage-controlled oscillators (VCOs), quasi digital techniques, and analog to digital converters (ADCs) [51]. Based on the literature, in comparison to ADCs and VCO based solutions, quasi digital circuits have some advantages such as dynamic range for size. A quasi digital output design combines the benefit of analog devices (low power, less complexity) and digital devices to generate a pulse, frequency/time.

A pH to frequency converter based on a voltage-clamped ISFET topology combined with a quasi-digital frequency technique is depicted in this section. The single-ended voltage-clamped structure was implemented in a standard 0.18 μm CMOS technology. The proposed single-ended pH to frequency converter is depicted in Fig. 4.1. It consists of different segments, such as a voltage-clamped ISFET pH to voltage conversion circuit, a differential low-power amplifier, a voltage comparator, and an SR-latch. In Fig. 4.1 (a), voltage clamping is performed by the transistor pairs of M1 and M4. A constant current source was used for biasing M1. M1 and M4 fix the drain voltage of the ISFET. Subsequently, any changes in ion concentrations change the ISFET's current. Compared to other voltage-clamped circuit designs, this structure has minimum power consumption and lower power supply, which helps overload protection. The minimum power supply is as follows,

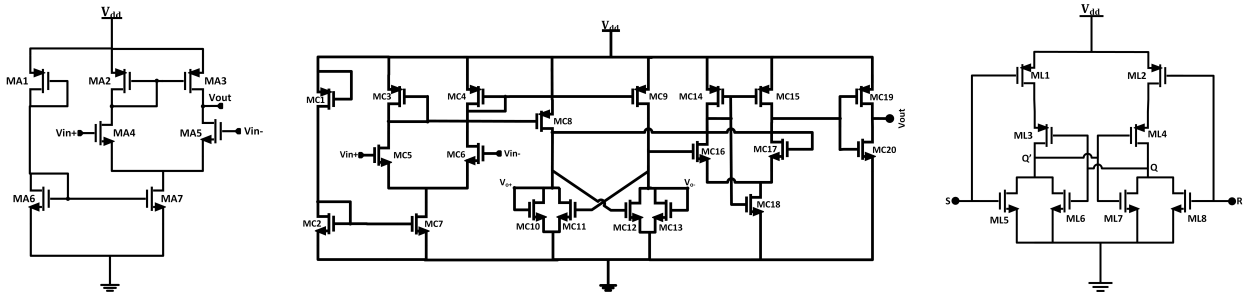
$$V_{DD} = V_{DS_3} + V_{DS_4} + V_{DS_{ISFET}} \tag{4.1}$$

If you compare this equation with the other voltage-clamped circuits, you can see one V_{GS} is mitigated from the equation, which results in having a lower power supply. The topology of [49] follows the frequency conversion circuit structure.

SR-latch is used to turn M7 on and off to make charging and discharging the capacitor (C_T). The output voltage from the entire design is converted to current for this purpose. The oscillation in the circuit is continued by charging and discharging the capacitor. It is performed by M6, M7, differential amplifier, and the resistor (R_T). A comparison window is performed by the comparators to convert the voltage level of the capacitor to frequency. The capacitor is discharged at the first stage, so the voltage which is sourced to the comparators is lower than the references and results in the low output voltage of SR-latch. When M7 is supplied with the low voltage, it turns on and charges the capacitor consequently. In the system, the pH applied on the electrode surface will make a change to the current. So the charging rate of capacitance relates to the pH level. At the next level, when the voltage gets to the upper reference voltage, (C_T) will be discharged. With the comparators' performance, the current mirror, which is formed by M6, M7, M8, and M9, will convert the analog input to digital output. The photomicrograph of the pH to frequency sensor is shown in Fig. 4.2.



(a) Complete proposed readout circuit for pH to frequency design.



(b) Amplifier **(c)** Voltage comparator **(d)** SR-latch

Figure 4.1: (a) Complete proposed readout circuit for pH to frequency design that includes, (b) Low-power amplifier, (c) Voltage comparator, and (d) an SR-latch circuit.

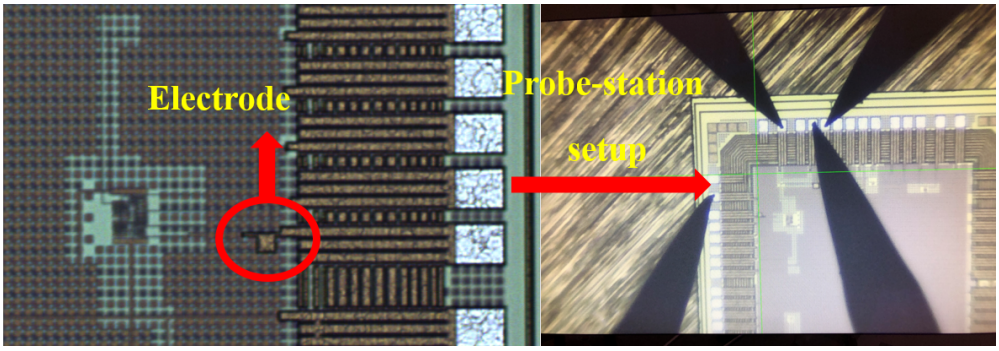


Figure 4.2: Photomicrograph of the chip designed in 0.18 μm CMOS technology.

The topmost metal layer (Metal 6) in 0.18 μm CMOS technology formed the sensing electrode.

4.1.1 Simulation and Experimental Results

The proposed circuit design was fabricated in 0.18 μm CMOS technology. Based on [20], $\alpha = 0.95$ and $\gamma = -324mV$ were used in this design. The reference voltage is 0.9 V. The transistors' dimensions are as follows, M1, M2, M3, M4, and ISFET have an aspect ratio of $1\mu m$/180nm, $3\mu m$/180nm, $1\mu m$/180nm, $3\mu m$/180nm, and 220nm/180nm, respectively. Also, the current supplied by the current mirrors were implemented with diode-connected transistors with the W/L of $3\mu m$/180nm. The transient response of the front-end ISFET with three different electrode sizes is shown in Fig. 4.3. As demonstrated, with varying the pH from 1-14, the output voltage is variable from 165-930 mV. The power consumption of the block is 15.38 μW. The sensitivity is shown in Fig. 4.4. The sensitivity for the ISFET with the smaller size of the electrode ($10\mu m \times 10\mu m$) is 27 mV/pH, for ($80\mu m \times 80\mu m$) is 40 mV/pH, and the larger size of the electrode ($200\mu m \times 200\mu m$) is 110 mV/pH. The output voltage is then conveyed into the amplifier and the resistor. The amplifier is a low-power amplifier with a power consumption of 54.52 nW.

The transistor's aspect ratio (in the amplifier) MA1, MA2-MA3, MA4-MA5, MA6, and MA7 are 700nm/$7\mu m$, 700nm/$14\mu m$, $60\mu m$/180nm, 400nm/$7\mu m$, and 220nm/$7\mu m$ respectively. R_T and C_T are 500 kΩ and 167 fF. For the comparators, the transistors' size is as follows: MC1-MC2, MC5-MC6, MC10-MC13, MC16-MC17, and MC20 have the aspect ratio of $1\mu m$/500nm. MC3-4, MC7, and MC14-15 have an aspect ratio of $2.5\mu m$/500nm. MC8-9 and MC19 have an aspect ratio of $1.5\mu m$/500nm. For DC characterization in voltage comparator, the positive input was swept from 0-1 V, while the negative input was stepped from 0-1 V within 100 mV increments. AV of the comparator can be extracted out of the derivative of DC characterization. The measured AV was about 600. The output of the comparators goes into the input of the SR-latch. The size of the transistors that are being used in SR-latch are as follows, ML1-ML4 transistors have an aspect ratio of 280nm/$7\mu m$ and transistors ML5-ML8 have an aspect ratio of 800nm/$7\mu m$. Fig. 4.5 illustrates the

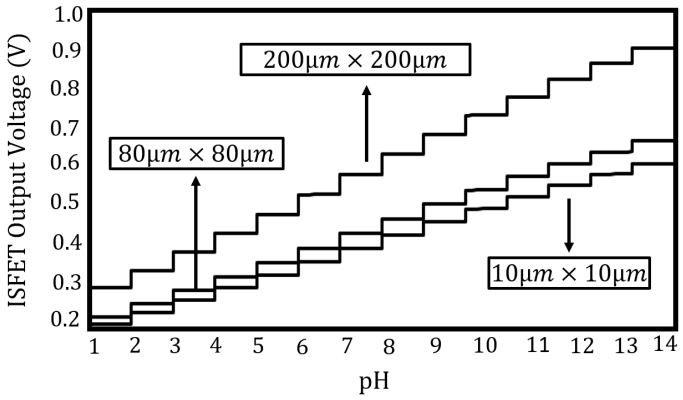


Figure 4.3: Transient response of ISFET output voltage for three different gate electrodes ($10\mu m \times 10\mu m$, $80\mu m \times 80\mu m$, and $200\mu m \times 200\mu m$).

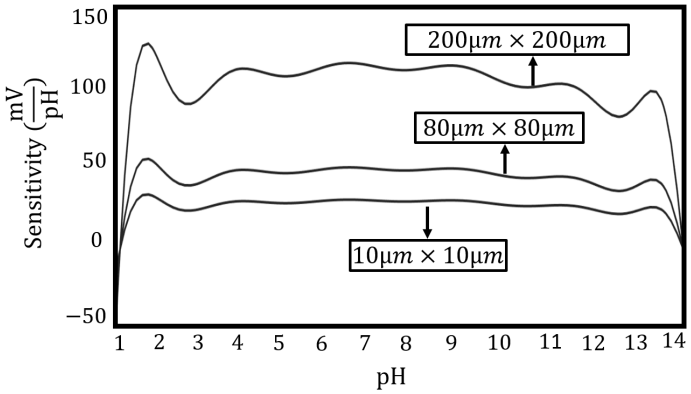


Figure 4.4: ISFET sensitivity for three different sizes of gate electrodes ($10\mu m \times 10\mu m$, $80\mu m \times 80\mu m$, and $200\mu m \times 200\mu m$).

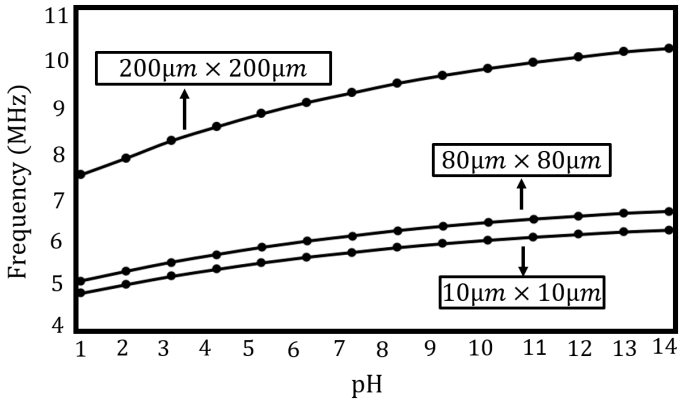


Figure 4.5: Frequency as a function of pH for three different sizes of gate electrodes ($10\mu m \times 10\mu m$, $80\mu m \times 80\mu m$, and $200\mu m \times 200\mu m$).

relation between the pH and frequency of the whole circuit design. The frequency is variable between 4.90-6.70 MHz for $10\mu m \times 10\mu m$ and $80\mu m \times 80\mu m$. The frequency for $200\mu m \times 200\mu m$ electrode is variable between 7.5-10.2 MHz.

One of the parameters which might affect the linearity of the circuit is a mismatch. To see the fabricated device's variation, Monte-Carlo was performed on the circuit at each pH level from 1-14. 100 runs up to 1000 were performed. The results are illustrated in Figs. 4.6 and 4.7. The mean frequency is as follows; for pH 4 is 5.82 MHz, pH 7 is 5.98 MHz, and pH 10 is 6.14 MHz. Also, the mean standard deviation for pH 7 is 308 kHz, and the maximum standard deviation and the minimum standard deviation is 346 kHz and 285 kHz, respectively.

For experimental measurements, the probe station with the model of "Cascade PMC200 from Form-Factor" was used. According to Table 4.1, the input voltage was changed, and the output voltage was recorded. The experimental testing of the front-end is depicted in Fig. 4.8. Also, the frequency tested on three different chips is variable between 220-570 kHz. It is depicted in Fig. 4.9. The graph in Fig. 4.10 describes the dependence of the pH, floating gate voltage, and the frequency.

4.1.2 Experimental Verification with Standard pH Buffer Solutions

This chip was tested under actual pH as well. After sealing, experimental verification with standard pH buffer solutions (pH=4, pH=7, and pH=10), were performed. The results are illustrated in Fig. 4.11, 4.12, and 4.13. Outputs were distorted and not fully digital, however frequency content can still be extracted. The frequency for pH=4, pH=7, and pH=10 are 25 kHz, 40 kHz, and 55 kHz, respectively. These plots were derived from the output of the oscilloscope. Finally, the comparison between this design and other recent sensors is illustrated in Table. 4.2. Based on the comparison, this design can be utilized in biomedical applications.

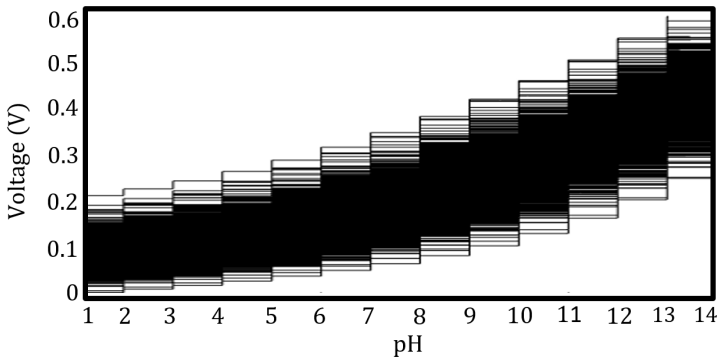


Figure 4.6: 1000 runs Monte-Carlo simulation performed on ISFET output voltage.

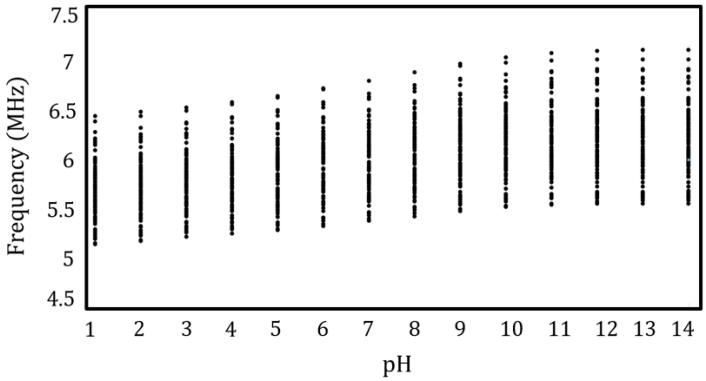


Figure 4.7: 1000 runs Monte-Carlo simulation performed on pH to frequency output.

Table 4.1: Voltage and corresponding pH (pH to frequency).

pH	Input1 (mV)	Input2 (mV)	pH	Input1 (mV)	Input2 (mV)
1	630	676	8	490	522
2	610	654	9	473	502
3	588	632	10	454	481
4	570	610	11	436	460
5	552	588	12	410	433
6	528	561	13	390	410
7	509	541	14	370	388

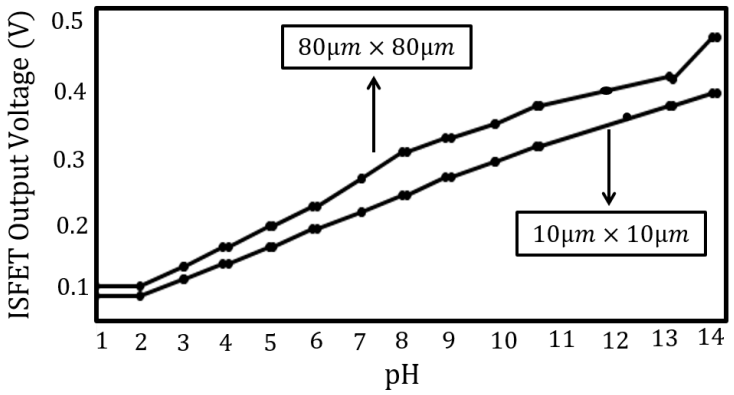


Figure 4.8: ISFET output voltage (experimental).

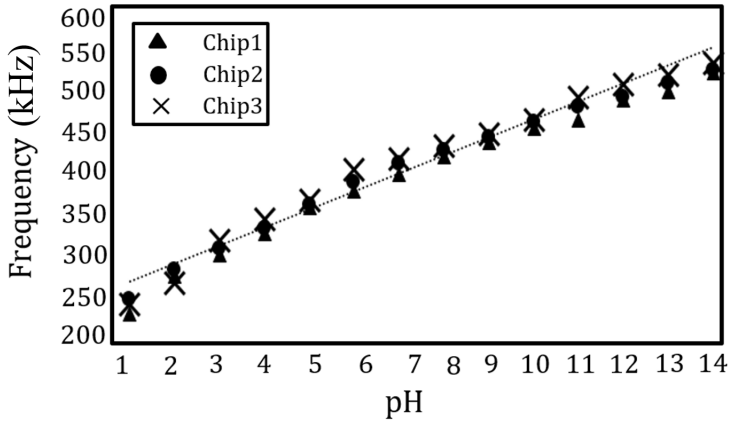


Figure 4.9: Frequency as a function of pH (experimental testing) for three different chips.

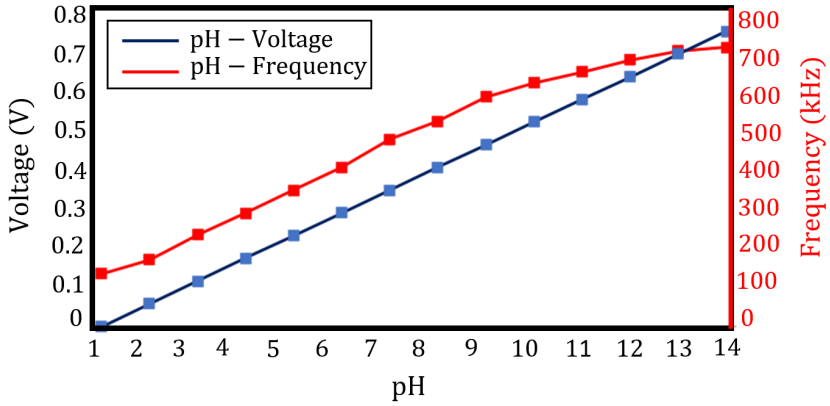


Figure 4.10: The pH-voltage-frequency pattern in fabricated IC design.

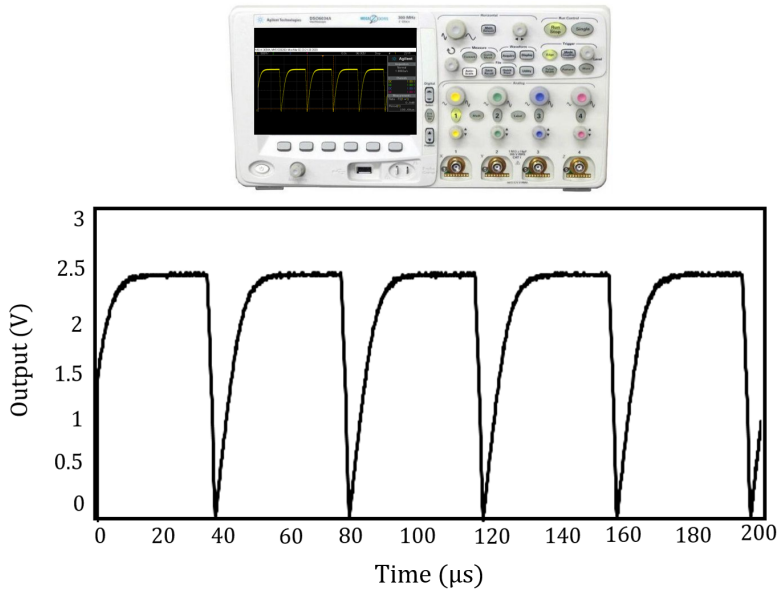


Figure 4.11: Experimental frequency verification with standard pH buffer solutions (pH=4). The results were derived from C_T. Frequency is 25 kHz.

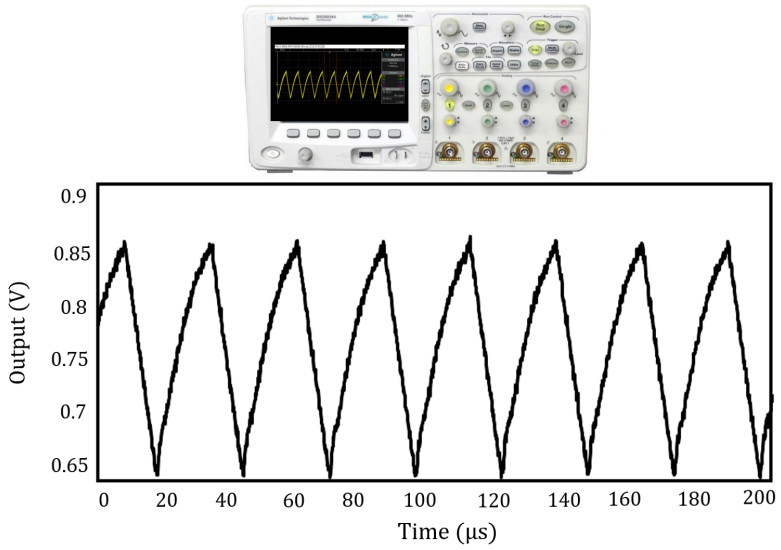


Figure 4.12: Experimental frequency verification with standard pH buffer solutions (pH=7). The results were derived from C_T. Frequency is 40 kHz.

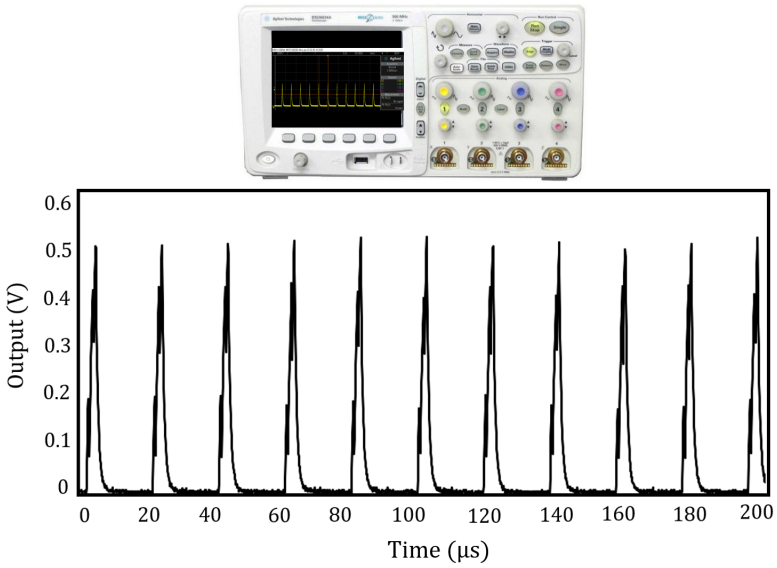


Figure 4.13: Experimental frequency verification with standard pH buffer solutions (pH=10). The results were derived from C_T. Frequency is 55 kHz.

Table 4.2: Comparison with state of the art.

	[23]	[39]	[42]	[48]	[49]	[51]	[73]	This Work
Year	2013	2020	2020	2006	2011	2009	2018	2019
Technology (nm)	350	180	180	250	180	350	350	180
ISFET Topology	Differential	Differential	Averaging	-	-	-	Translinear	Voltage clamped
pH Range	1-14	5.5-10.5	-	-	-	-	6.6-8.6	1-14
Sensitivity	50 (mV/pH)	25.7 (mV/pH)	166.5 (mV/pH)	520 (kHz/V)	500 (kHz/V)	1 (MHz/V)	-	40 (mV/pH) 6.92 (MHz/V) 138 (kHz/pH)
Output Frequency	-	-	-	110-416 kHz	0-501 kHz 510-993 kHz	1.2-2.2 MHz	-	4.90-6.70 MHz
Total System Power	231.5 μW	0.72 nW	2.9 μW	-	60 μW	1.03 mW	16.6 μW	40.20 μW
Area (mm^2)	-	0.85	1.17	0.340	-	-	3.74	0.0036

4.1.3 Portable pH to Frequency ISFET Sensor

To make a portable pH to frequency sensor, PCB design was fabricated. Instead of using the off-chip ADC part (for converting an analog signal to digital), an on-chip quasi-digital technique was used. The output voltage from the chip was sent to an Arduino-Uno to be displayed on an LCD. The portable board is depicted in Fig. 4.14. It has a total area of 4.9 inch $\times$ 4.5 inch, with the fabricated ISFET of 0.0036 mm^2. The pH and its corresponding frequency are shown on an LCD.

4.2 Integration of ISFET Digital Readout with Counter

Previously, the pH to frequency converter was designed with utilizing a quasi-digital circuit. Since the pH in a solution is almost unchanged in the event of no chemical disruption, the counter is needed to produce a bit-stream of data, the average of which is the scaled version of the carrier frequency in a given period. The other way to analyze the relationship between pH and quasi-digital performance is to test bitstream's DC quality. The bitstream's DC value could be estimated by counting the number of ones in the quasi-digital output in a specific period. The design is most likely the same as the one proposed in Fig. 4.1, (using a single-ended voltage-clamped with the combination of the quasi-digital circuit).

The output of the SR-latch is fed to the counter (Fig. 4.15), which is a sequential digital logic that uses an input called x in the diagram and a CLK to store the data. The counter is depicted in Fig. 4.16. The block consists of J-K flip-flops, And gates, Nand gates, 3-Input-And gates, and 3-Input-Nand gates. This counter is a synchronous counter with an external clock signal. The external clock signal connects every J-K flip-flops within the counter in the chain, so all of the flip-flops are clocked simultaneously. J and K of the second flip-flop are connected to the first flip-flop's output, but the J and K of the other flip-flops are driven from additional AND gates. These blocks are supplied from the input and output of the former stage. The benefit of using a synchronous counter is that there is no propagation delay since all of the counter stages are triggered in parallel simultaneously. The proposed circuit design was fabricated in 0.5 μm CMOS technology. The photomicrograph of the proposed design is depicted in Fig. 4.17.

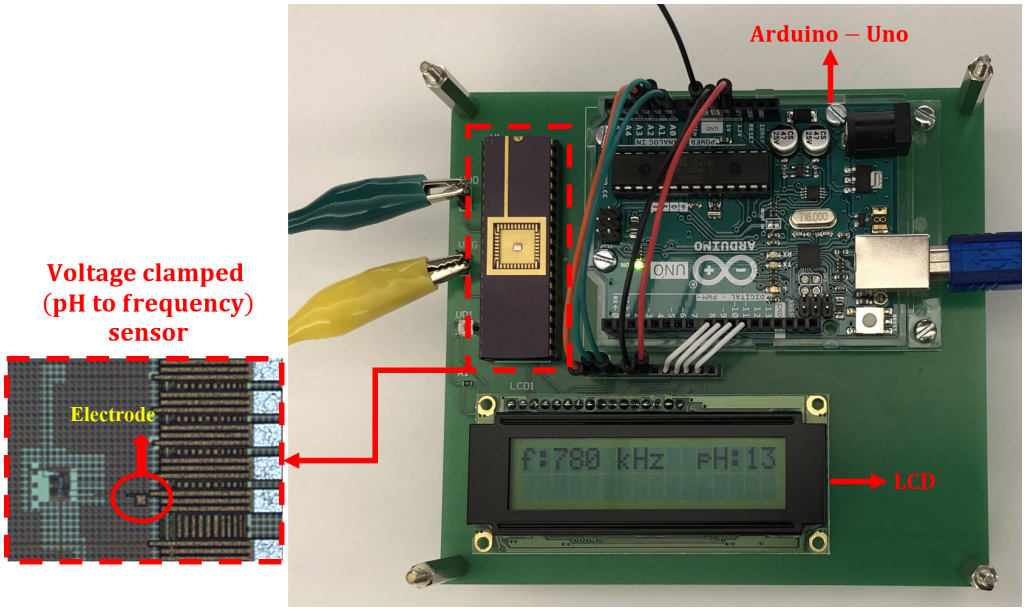


Figure 4.14: PCB of the full portable single-ended ISFET pH to frequency sensor.

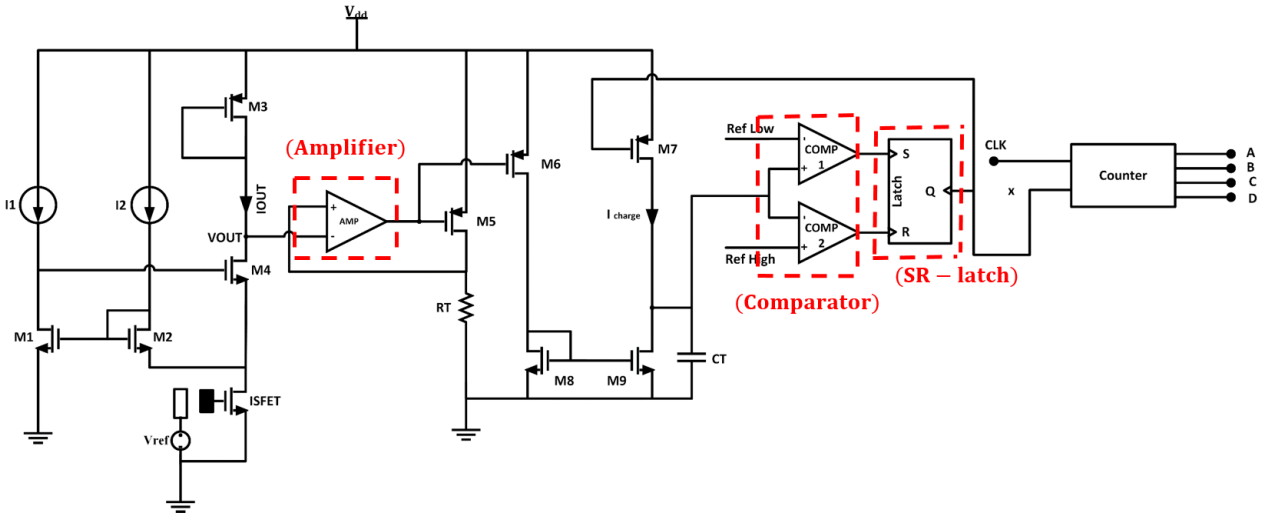


Figure 4.15: Integration of the quasi-digital ISFET readout circuit with the counter for generating bit-stream of data.

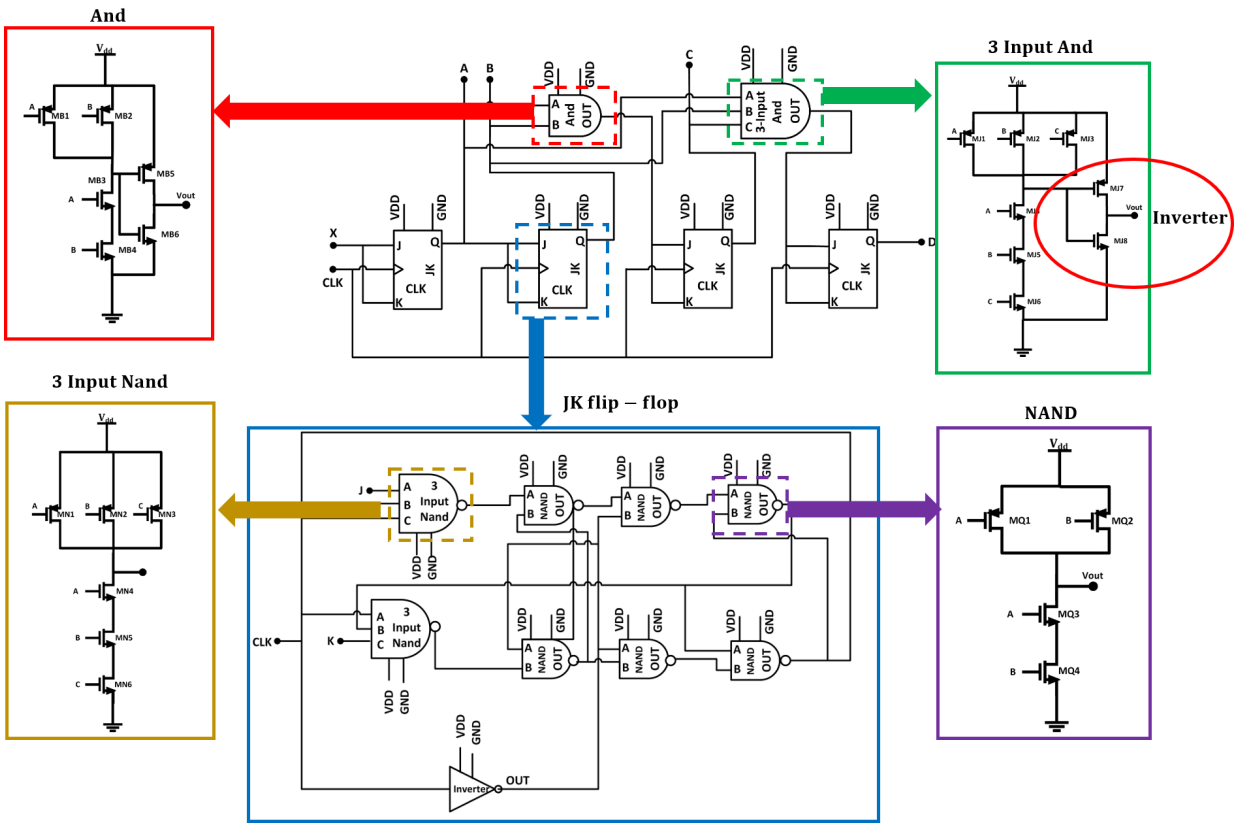


Figure 4.16: Counter circuit design which includes J-K flip-flops (Nand gates and 3-Input Nand gates), And gate, and 3 Input And gates.

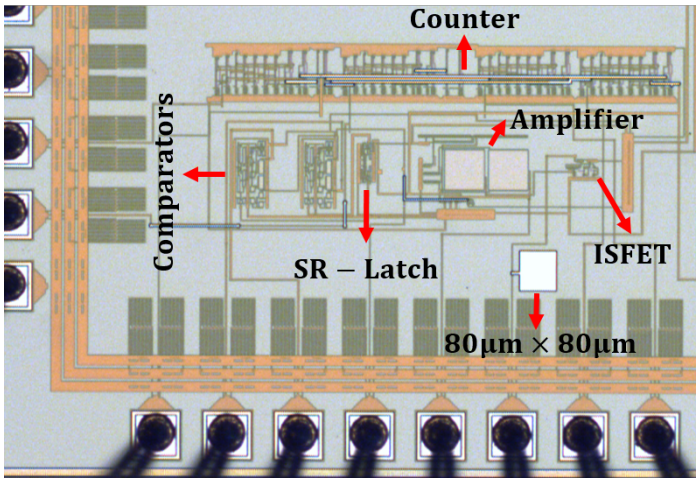


Figure 4.17: Photomicrograph of the fabricated chip (integration of the quasi-digital ISFET with the counter).

4.2.1 Simulation and Experimenal Results

The proposed circuit design was fabricated in 0.5 μm CMOS technology. The transistors' dimensions are as follows, M1, M2, M3, M4, and ISFET have an aspect ratio of 1.5 /0.6, 3/0.6, 6/0.6, 15/0.6, and 10/1.5, respectively. Also, the current supplied by the current mirrors were implemented with diode-connected transistors with W/L of 3/0.6. V_{ref} of the design is 0.9 V. The transient response of the front-end ISFET is shown in Fig. 4.18. As demonstrated, with varying the pH from 1-14, the output voltage is variable from 0.75-1.03 V. The power consumption of the front-end is 315 nW. The sensitivity is 50 mV/pH, which is shown in Fig. 4.19. The output voltage is then conveyed into the amplifier and the resistor. The amplifier is a low-power amplifier with a power consumption of 56 μW. The aspect ratio of the transistors MA1, MA2-MA3, MA4-MA5, and MA6-MA7 are 10/1.5, 24/0.6, 60/60, and 80/0.6, respectively. R_T and C_T are 500 kΩ and 300 pF. For the comparators, the size of the transistors are as follows, MC1-MC4 and MC7, MC5-MC6, MC8-MC13 and MC19-MC20, MC14-MC17, and MC18 have the aspect ratio of 6/7, 20/7, 3/7, 3/24, and 3/4, respectively.

The output of the comparators goes into the input of the SR-latch. ML1-ML4 transistors have an aspect ratio of 3/7, and transistors ML5-ML8 have an aspect ratio of 1.5/7. Finally, the output of the SR-latch is connected to the input of the counter. Fig. 4.20 illustrates the relation between the pH and frequency of the whole circuit design. The frequency is variable between 21.70-27.90 kHz. The linearity is within pH 1 to pH 10. The delay, rise time, and fall time for 1pF-5pF capacitors are shown in Table 4.3. According to Table 4.3, the rise time, fall time, and the delay linearly varies with the capacitive loading. The rise time and fall time were measured for 10 MHz frequency. These numbers prove the counter's linearity and show that the fall time is higher compared to the rise time. This is due to the presence of NMOS transistors in the circuit. So the load capacitors discharge via NMOS transistors to get to the ground potential.

Stanford Research Systems model (SR785) two-channel dynamic signal analyzer was used for the noise measurement showing an average of 75 nV/$\sqrt{Hz}$ in the 10 Hz to 100 kHz frequency range.

As it is clear in the schematics, there are different blocks of Nands in the design which have NMOS transistors in series. Having transistors in series result in a greater resistance of the transistors, higher RC delay, and, consequently, higher fall time. Also, in Nand gates, PMOS transistors are parallel, which expedites in charging the load capacitors and results in lower rise time.

The transient response of the counter is shown in Fig. 4.21. The figure shows the output response of the counter with a 10 MHz input clock. By falling the clock edges, the transitions of the Q output will start. The first flip-flop toggles on every edged triggered pulse. While at a specific and given clock pulse, the second flip-flop will trigger. The third flip-flop toggles if the two outputs of the first two flip-flops (A and B) are high. D will also toggle if all the three outputs (A, B, C) are high. By counting the number of pulses (D output) which resides in SR-latch output, we can estimate the bit-stream from each signal (Fig. 4.21). The electrical experiment, along with the counter, is shown in Fig. 4.22. Note that these particular experiments were performed over shorter and longer times.

Finally, the comparison between this design and state of the art is shown in Table. 4.4. As shown, this design has a good sensitivity (50 (mV/pH)) as well as a small size area (0.205 mm^2) in the range of pH 1-10.

4.2.2 Experimental Verification with Standard pH Buffer Solutions

After sealing the ICs, experimental verification with standard pH buffer solutions (pH=4, pH=7, and pH=10), were carried out. The pH buffer calibration kit was purchased from Innovative Science. With using pH=4, the experimental results from four flip-flops are shown in Fig. 4.23, with pH=7, the results are shown in Fig. 4.24, and with pH=10, the results are shown in Fig. 4.25. Based on the results, the sensor is responsive to different ion concentrations. With an increase in pH, there is an increase in the generated outputs from each of the flip-flops. After 5 μs, by applying pH=4, the counter counted 0100, with pH=7, it counted 1110, and with pH=10, it counted 1111.

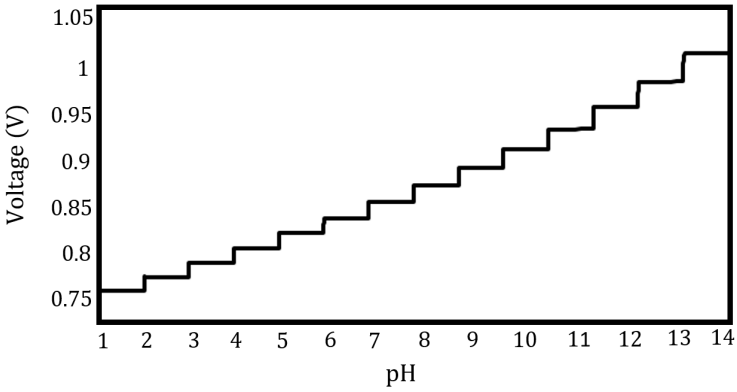


Figure 4.18: Transient response for ISFET output voltage.

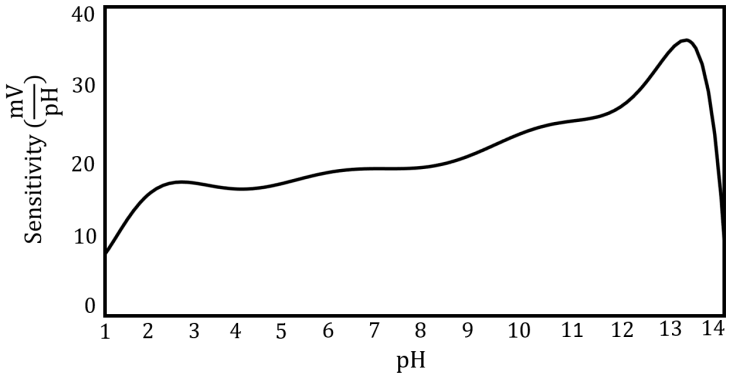


Figure 4.19: ISFET sensitivity.

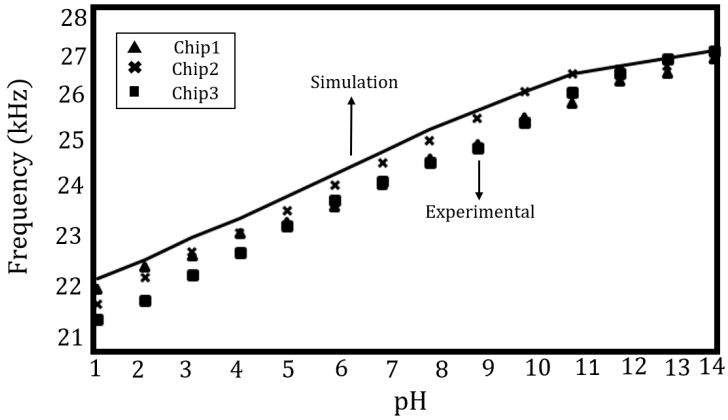


Figure 4.20: Frequency as a function of pH.

Table 4.3: Delay, rise time, and fall time for 1-5 pF output capacitors.

Capacitor (pF)	1	2	3	4	5
Delay (ns)	2	3.37	4.25	6.11	7.47
Rise time (ns)	2.72	5.06	7.41	9.10	10.7
Fall time (ns)	8.68	16.9	25.2	33.4	40.0

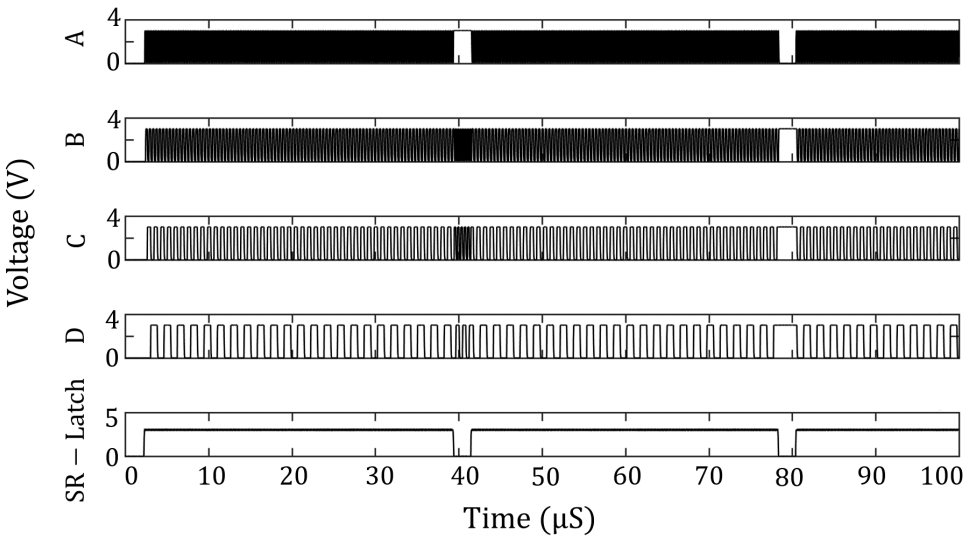
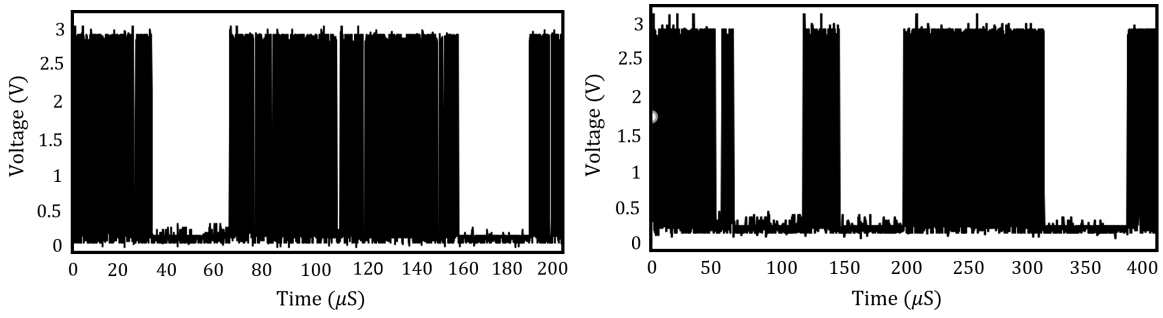


Figure 4.21: Transient response of the counter.



(a) **(b)**

Figure 4.22: Counter experimental results. (a) Experimental results over 200 μs. (b) Experimental results over 400 μs.

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Table 4.4: Comparison with state of the art.

	[31]	[38]	[39]	[42]	[73]	[76]	This Work
Year	2019	2019	2020	2020	2018	2019	2020
Technology	180 (nm)	180 (nm)	180 (nm)	180 (nm)	350 (nm)	180 (nm)	500 (nm)
ISFET Topology	Differential	Differential	Differential	Averaging pixel	Translinear	Voltage clamped	Voltage clamped
pH Range	4-10	5.5-9	5.5-10.5	-	6.6-8.6	1-14	1-10
Sensitivity	11.78 (%/pH)	9.7 (mV/pH)	25.7 (mV/pH)	166.5 (mV/pH)	-	40 (mV/pH)	50 (mV/pH) 440 (Hz/pH)
Total System Power	61 (μW)	176 (nW)	0.72 (nW)	2.9 (μW)	16.6 (μW)	40.20 (μW)	206 (μW)+ 36 (mW)
Area (mm^2)	4	13.94 (mm^3)	0.85	1.17	3.74	0.0036	0.205+0.0338
Modules	ISFET+ Linear OTA+ Switches +XOR +Sawtooth OSC	Differential CVCC using ISFET +REFET +FSM	Differential readout using ISFET +REFET +SAR ADC Current bias generator+ Interface	ISFET+ ADC+DAC+ Switches+ SRAM	Translinear ISFET+ I_{Ref} mirror+ +Switches	ISFET+VFC with window comparators +SR-latch	ISFET+ VFC with window comparators +SR-latch +Counter 8-bit MIPS

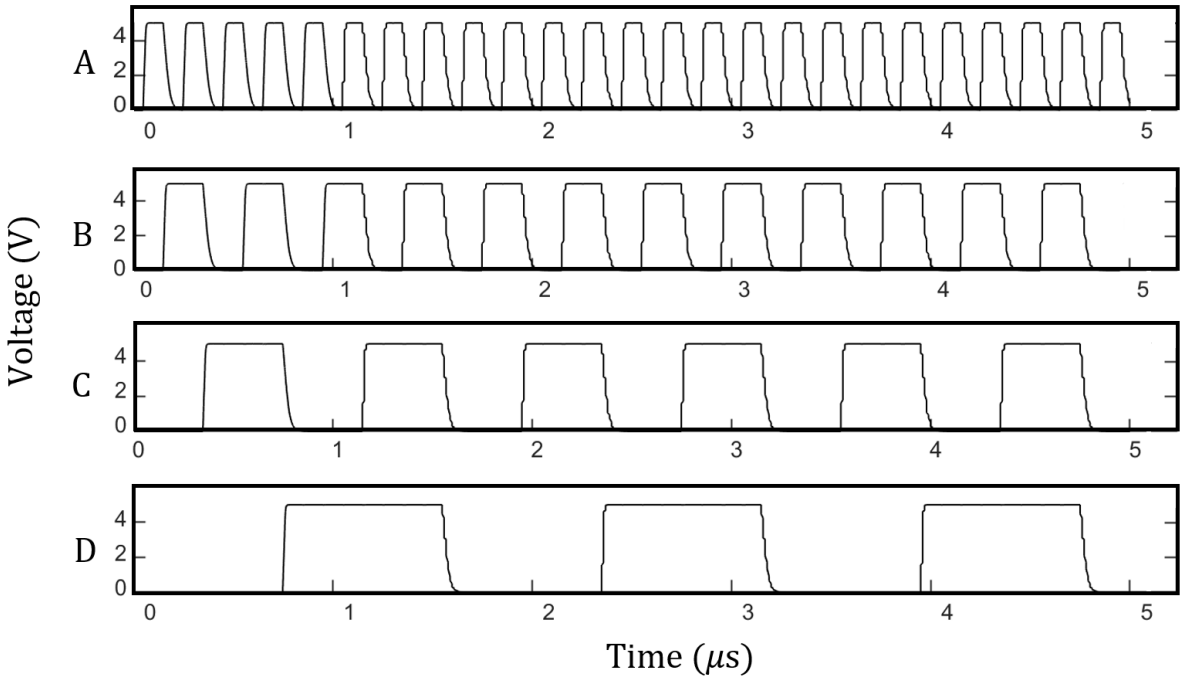


Figure 4.23: Counter experimental results using pH=4 solution. After 5 μs, the counter counted up to 0100.

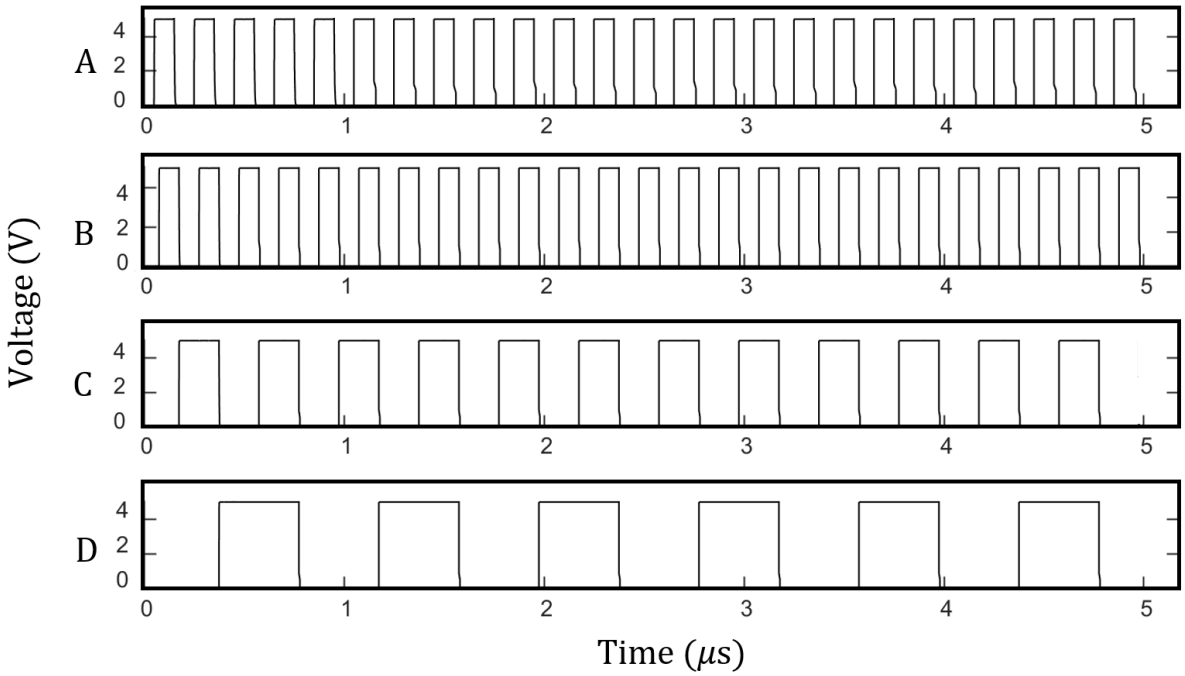


Figure 4.24: Counter experimental results using pH=7 solution. After 5 μs, the counter counted up to 1110.

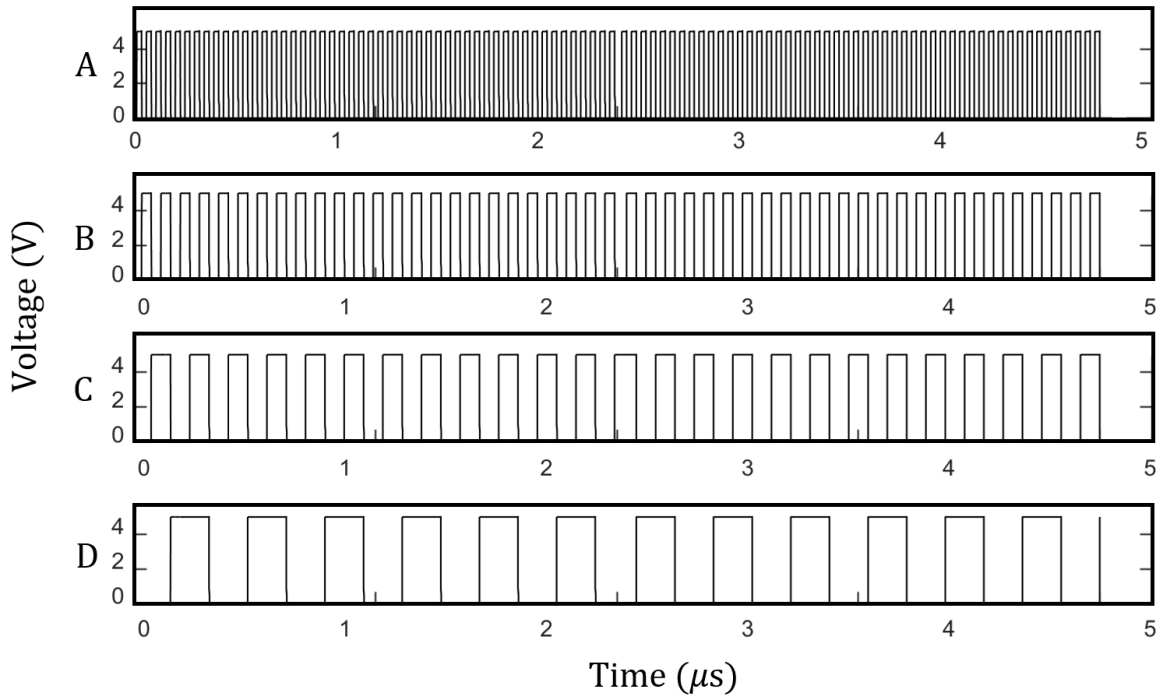


Figure 4.25: Counter experimental results using pH=10 solution. After 5 μs, the counter counted up to 1111.

4.3 Effects of Temperature on pH

Generally speaking, the temperature has a remarkable effect on pH measurement. With an increase in the temperature, there is an increase in molecular vibrations, making the water ionize and create additional hydrogen ions. There are two types of temperature compensation [77],

Automatic Temperature Compensation (ATC): This method is commonly built into updated pH meters for accurate results and is a compensation technique for fluctuating milli-volts output from the electrode. The pH and temperature are measured simultaneously. When a sample is tested, the pH and temperature probe should be inserted in the solution and stirred to have a stable reading.

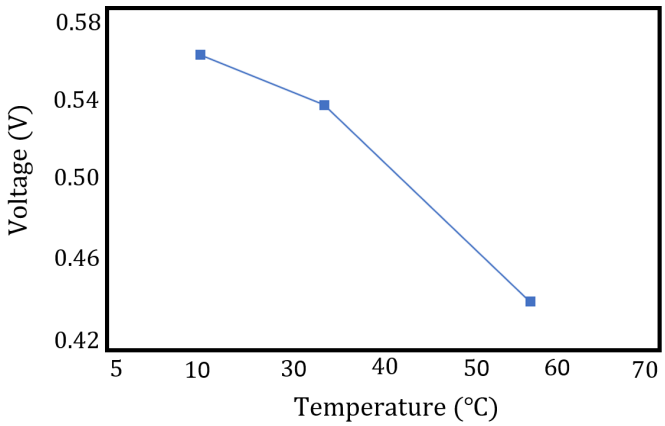
Solution Temperature Compensation (STC): This is a compensation technique to convert the pH at a measurement temperature to the pH at a reference temperature. In this method, the pH values taken at the same temperature and using the same solution temperature compensation can be compared to each other. As mentioned, the variations in temperature can cause an effect on solution viscosity and ion mobility. Temperature affects electrode sensitivity and membrane resistance. Besides that, it affects the result of the solutions which are applied to the electrodes.

To verify the effects of the temperature on pH solution, an experiment was performed. The chip was asserted in the temperature chamber, and the voltage corresponded to pH solutions were varied. The temperature chamber model is Sun Electronics Systems Temperature Chamber (-73 to 315 ^oC). The result is illustrated in Fig. 4.26. The temperature was varied over $5-70^oC$ with the pH of 4, 7, and 10. Also, this figure shows the variation dependence of pH on temperature ranging from -2.8 to -1.94, and to -1.16 mV/^oC for pH 4, 7, and 10 respectively.

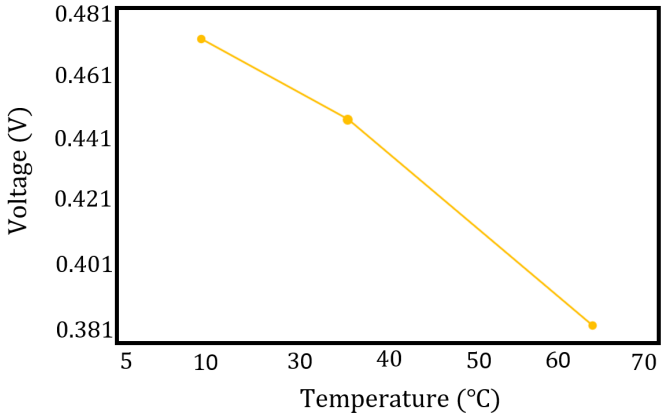
4.4 Conclusion

In this chapter, the state of the art for the single-ended quasi-digital ISFET pH sensors were considered. The ISFET pH sensors enable low-power consumption and low area for portable

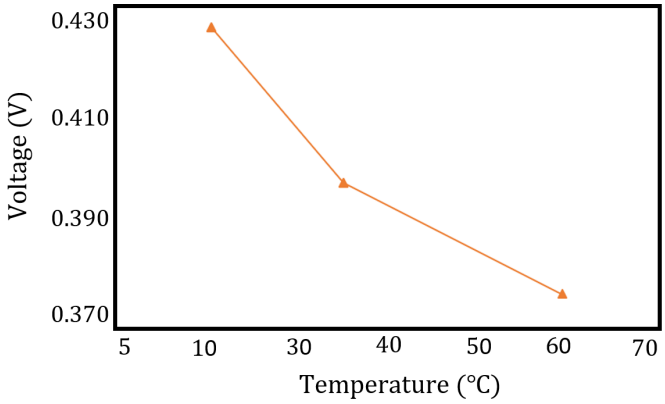
and miniaturized applications. A quasi-digital circuit was used to combine the voltage-clamped technique to reduce the size and eliminate ADC's use. The counter was used for generating the bitstream of data. The simulation and experimental results of the proposed ISFET pH sensors were presented. The pH to frequency ISFET sensor was implemented in the 0.18 μm CMOS process. The total system power consumption is 40.20 μW, with an area of 0.0036 mm^2. The sensitivity for this design is reported as 40 mV/pH. The PCB board was designed to make it portable. The board area is 11 $cm \times 11$ cm. For generating the bit-stream data, the counter was considered as a part of the design. The design with a counter as a readout circuit consumes 206 μW of power with a frequency of 21.70 to 27.90 kHz. The area is 0.205 mm^2.



(a)



(b)



(c)

Figure 4.26: Effects of the temperature on voltage-clamped ISFET pH sensor. (a) pH=4, (b) pH=7, and (c) pH=10.

Chapter 5

A pH-Impedance System for Lab-on-a-Chip Based Sensing

Portions of this section are published in,

"An Integrated pH-Impedance System for Lab-on-Chip Continuous Cell Based Sensing," Ready for submission, 2020.

"CMOS Based Whole Cell Impedance Sensing: Challenges and Future Outlook," Biosensors and Bioelectronics, Vol. 143, 111600, Oct 2019.

"A Low-Power Voltage-Clamped CMOS pH to Frequency Sensor," IEEE International Symposium on Circuits and Systems, Sapporo, Japan, pp. 1-5, May 2019.

5.1 Integrated System

Electric cell-substrate impedance sensing (ECIS) (Applied BioPhysics, Inc.) is a non-invasive technique to do an experimental testing measurement in real-time [78]. It is an approach for studying and diagnosing living cells in in-*vitro* and in-*vivo* environments. The interaction between the cells and the substrate is measured through ECIS. They are usually attached via the gold-film electrodes placed on the surface of the culture dish. These electrodes help the system measure the cell monolayer's ability to prevent a non-invasive AC signal. Fig. 5.1 shows this method. A voltage source creates an electric field between two electrodes. The presence and physical area of the cells between these two electrodes determine the measured

electric field. This comes about in a change of the measured current. On the other hand, a current source can be connected and the voltage measured. The two electrodes of the framework are known as the working electrode (WE) and the counter electrode (CE) [2].

Fig. 5.2 (Applied BioPhysics Inc.) shows the cultureware device. The 8W10E is an eight well culture dish with an identical circular electrode in each well, each of those has 10 smaller identical circular uninsulated openings to allow for current flow.

When the current flows via the culture medium, the impedance starts to increase, and it indicates an increase in the number of the attached cells on the electrodes. The impedance results from the electrodes' insulation by the cell membranes and through the junctions formed via neighboring cells and the distance the cells are from the substrate. In one of our proposed voltage-clamped ISFET pH sensors designs [76], which was fabricated in 0.18 μm CMOS technology, the pH sensor was integrated with an impedance sensor to be applicable for biological applications.

One of the applications which we considered with the proposed design is dielectric spectroscopy (DS). DS is a non-invasive method, which is also called impedance spectroscopy and is a technique for measuring the dielectric properties as a function of frequency. Real-time biological cell measurements can be crucial for many applications such as cancer research, drug screening, pathology, and monitoring neural cells. Electrical impedance and pH are two of the most crucial characteristics of the cells. pH measurements give valuable information regarding metabolic rates, the passage of fluids, or differentiating different cells. Also, extracellular pH plays a vital fact in cell functions. The medium's pH plays an important role in determining the cell growth and metabolism of protein synthesis. Also, the medium's acidity indicates an aggressive tumor phenotype [79]. Measuring the cell's reaction is beneficial for continuous tracking of metabolic changes in drug discovery. Impedance measurements give useful information regarding impedance tomography for lung function monitoring, breast, and skin cancer detection.

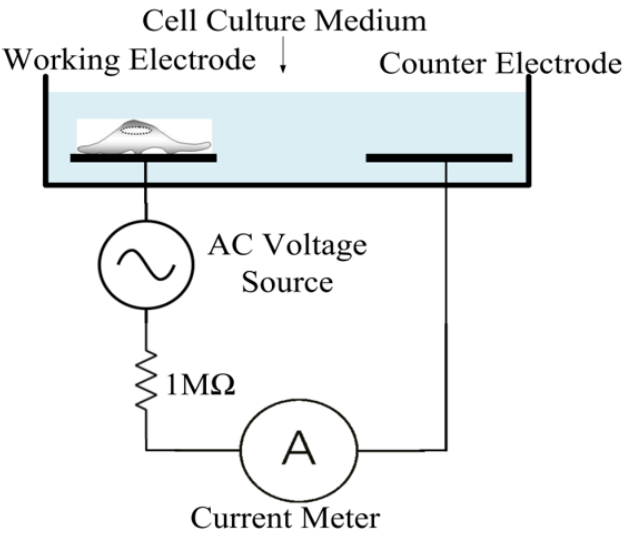


Figure 5.1: Measurement system design for ECIS application [2].

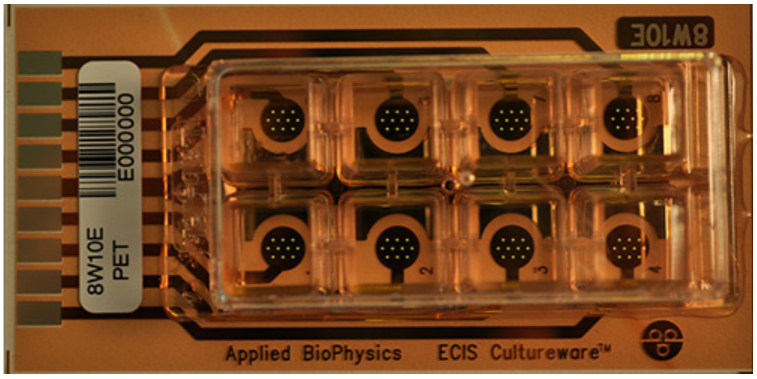


Figure 5.2: Electric Cell-substrate Impedance Sensing (ECIS) cultureware. There are ten circular 250 μm diameter active electrodes in each of the 8 wells connected parallel to a standard gold pad. The gold electrodes are attached on the PET (Polyethylene terephthalate) substrate, and there is an insulating material on top of the electrodes.

Implementation in CMOS facilitates portable/implantable sensors. As shown in Fig. 5.3, the output is a frequency proportional to pH and impedance. The impedance frequency module uses a current-mode comparator and an SR-latch. pH to frequency module uses native ISFET with a differential amplifier, comparator, and an SR-latch. The photomicrographs of the proposed chips are shown in Fig. 5.4.

5.2 Simulation and Experimental Results

The impedance to frequency sensor is a two-phase sensor that has independent circuits for resistance and capacitance measurements. The resistance measurement circuit consists of a current comparator and an SR-latch and the capacitance measurement circuit consists of the two voltage comparators, XOR, and an SR-latch.

A small AC signal was used to excite the sample. In the resistance measurement, this AC voltage changed to current by going through the sample via one of the current comparators; the other input is a DC reference. When the resistance is larger/smaller, the alternating current signal's amplitude is smaller/larger. The alternating current from the sample, which is compared to the DC giving an output pulse-width proportional to the amplitude of the alternating AC signal and subsequently proportional to the sample's resistance.

In the capacitance measurement, two comparators are used. One comparator is connected to the sample. The AC excitation signal going through the sample delivers a delayed signal to this comparator; comparing this delayed AC signal to a DC value, a delayed pulse is shown in the output. The other comparator is connected to the AC excitation signal and is then compared to a DC signal, giving us a pulse in phase with the alternating AC signal. The delayed pulse and the in-phase pulse with the AC signal are fed into the XOR as it's two inputs to capture the delay between these two pulses in terms of the pulse-width. The delay captures are proportional to the capacitance of the sample.

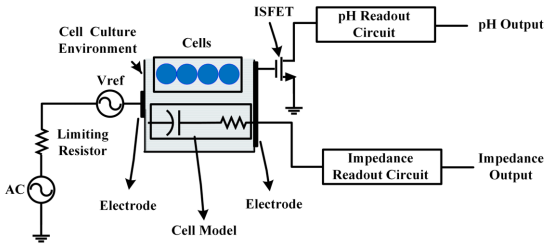
As seen above, the resistance and capacitance are translated to pulse-width; however, the pulse-width is not a convenient form of data to transfer or process by the next analog/digital blocks. SR-latch is used as a higher frequency modulator to convert pulse-width to frequency. In this design, a higher rate input pulse was assigned to the reset pin of the SR-latch. Until

the output of the comparator is high, this input produces pulses in higher frequency. As soon as dropping the current comparator's output to low, the output of the SR-latch keeps its status in a low mode. The simulation and experimental results for the ISFET pH sensor was shown in chapter 4, sections 4.1.1 and 4.1.2. With using a cultureware as an off-chip electrode (exactly the same as shown in 5.3 (a), the pH-voltage-impedance plot is shown in Fig. 5.5. The measurements were done using three wells as an electrode. Based on the results, with pH 4, the average pulse-width is 287.16 μs, with deionized water, the average pulse-width is 150.53 μs, with pH 7, the average pulse-width is 146.73 μs, and with pH 10, the average pulse-width is 111.2 μs. The average voltage for pH 4, deionized water, pH 7, and pH 10 is 98.33 mV, 111.6 mV, 165 mV, and 248.33 mV, respectively. Also, the pH-voltage-capacitance plot is shown in Fig. 5.6. With using pH 4, deionized water, 7, and 10, the pulse-width is 282.16 μs, 299 μs, 301 μs, and 320 μs, respectively.

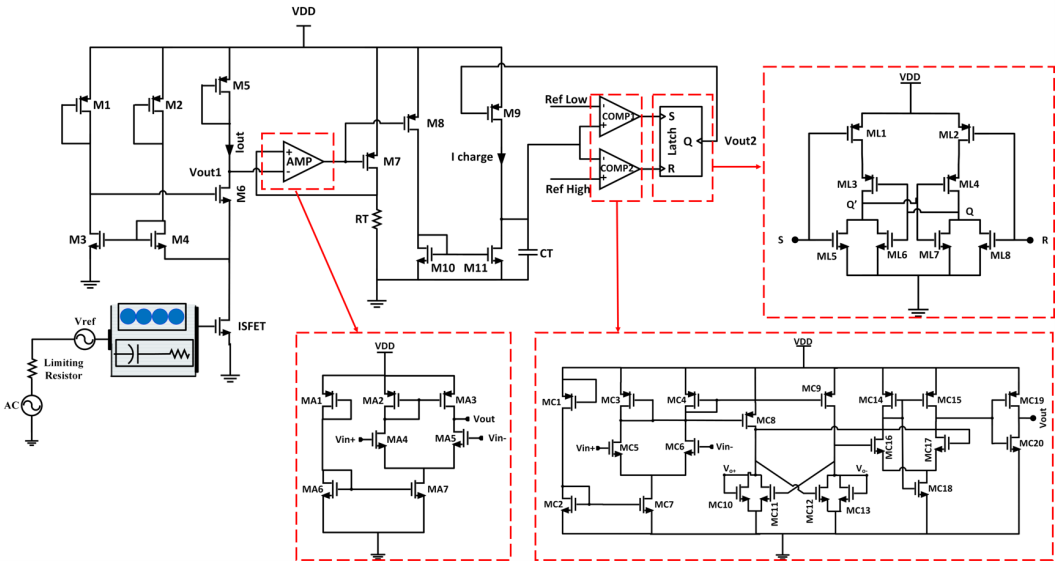
For the impedance sensor, the input signal, a sinusoidal voltage source with a 0.5 V amplitude and frequency of 100 kHz, were used for simulation. A 50 kΩ input resistor was implemented at the alternating voltage reference output to limit the current flowing through the cell to μA levels. The output of the current comparator is shown in Fig. 5.7. The current comparator's output for 1 kΩ, 50 kΩ, and in case of a dead cell (simulated by a pico-farad range capacitance corresponding to detached cell from the surface) shows that the bandwidth difference concerning impedance is visible and distinguishable.

For the experimental measurements, a sinusoidal voltage source with a 0.5 V amplitude, and four sets of frequencies (<1 kHz, 1 kHz, 10 kHz, and 100 kHz) were used to simulate the whole impedance circuit, using 10 Ω-1 MΩ resistance, which is shown in Fig. 5.8. Based on the results, with using less than 1 kHz frequency as an input signal, the pulse-width is about 1430 μs, with 1 kHz frequency, the pulse-width is variable between 0-1000 μs. Using 10 kHz frequency as an input signal, the pulse-width is variable between 0-100 μs, and finally, with 100 kHz frequency as an input signal, the pulse-width is variable between 0-10 μs.

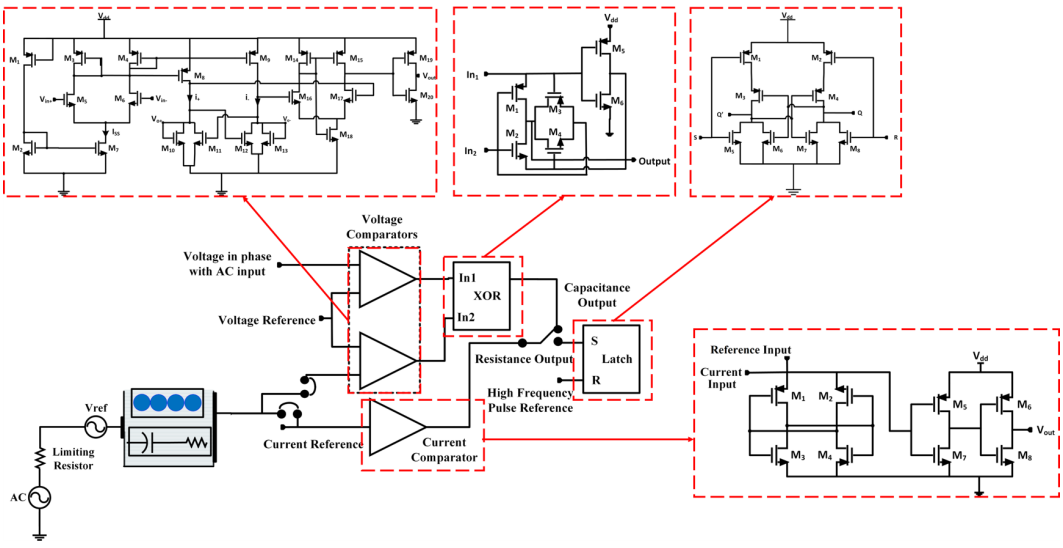
For capacitance testing, an AC signal was sourced to a reference resistance and an impedance. Due to the phase changes during the signal flow, a voltage comparator was used to make a constant voltage crossing. In the next step, an XOR was used to convert the phase to the duty cycle.



(a)



(b)



(c)

Figure 5.3: (a) Integrated pH-Impedance sensor, (b) ISFET pH sensor design. (c) Impedance sensor design.

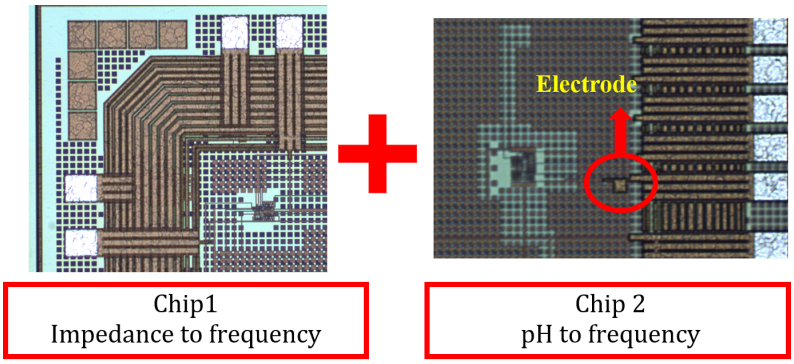


Figure 5.4: Photomicrograph of the two chips, impedance to frequency sensor, and pH to frequency sensor fabricated in 180 nm CMOS technology.

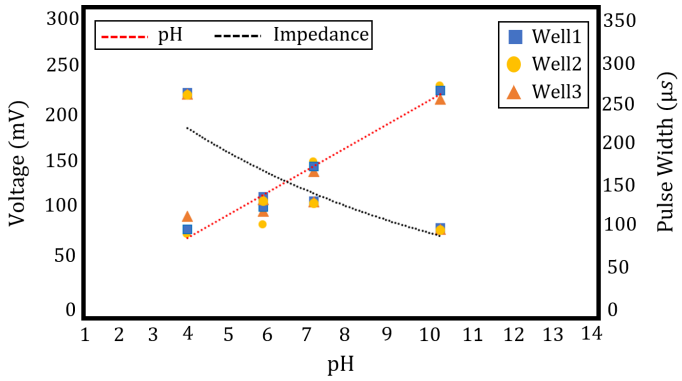


Figure 5.5: pH-voltage-impedance plot using a cultureware as an electrode.

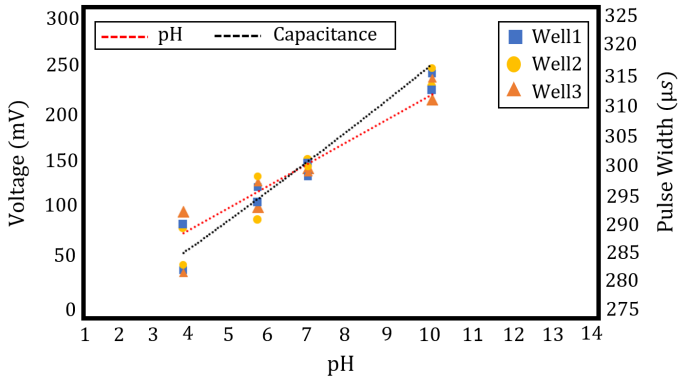


Figure 5.6: pH-voltage-capacitance plot using a cultureware as an electrode.

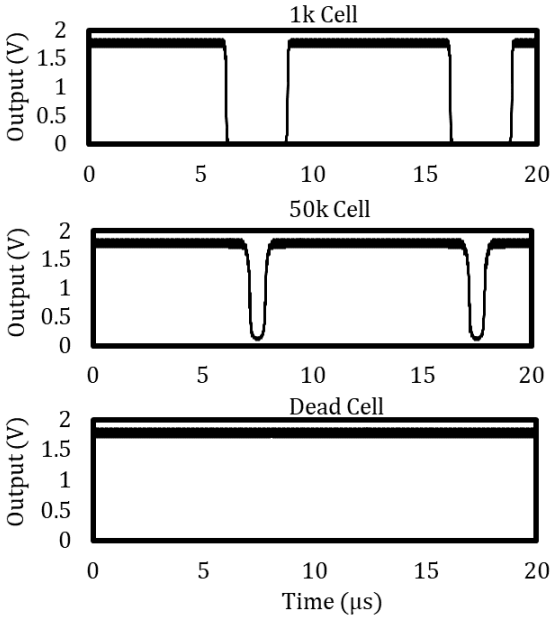


Figure 5.7: Simulation results for the current comparator with the cells in three different states, 1 kΩ, 50 kΩ, and a dead cell (Simulated by a pico-farad range capacitance corresponding to detached cell from the surface).

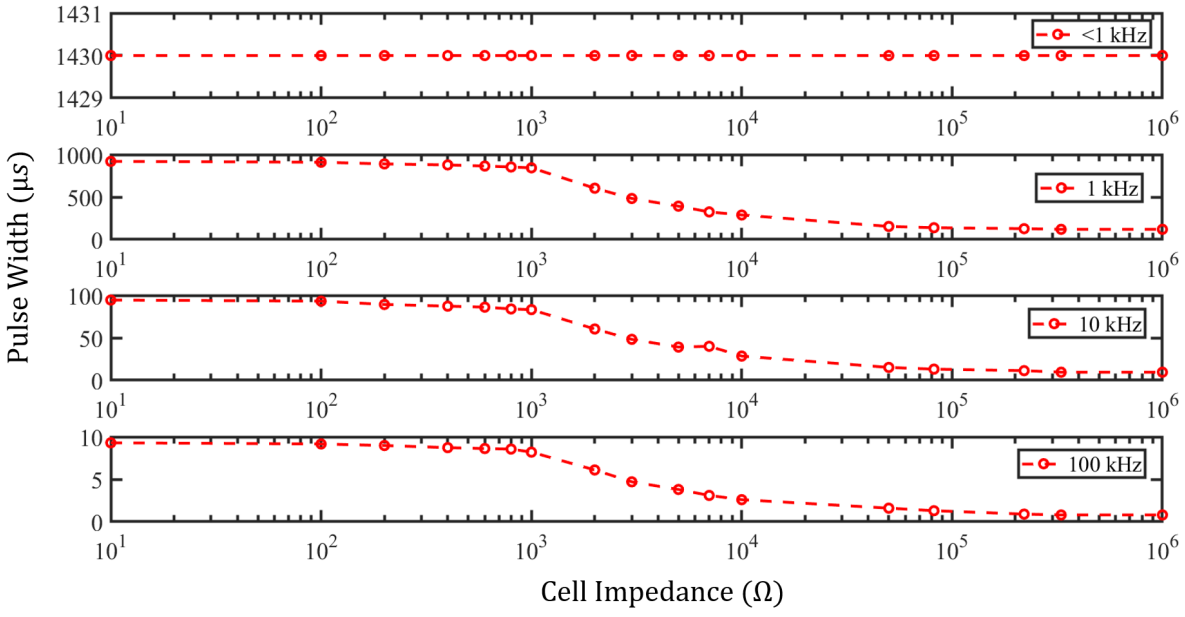


Figure 5.8: Experimental resistance output pulse-width for four sets of input frequency (<1-1-10-100 kHz) using 10 Ω to 1 MΩ resistance.

To see the system's linearity, the output frequency was measured for 40 nF to 2200 nF input capacitances. Fig. 5.9 shows the results measured in the frequency range of 500 Hz to 1 kHz. Based on the results, the pulse-width is variable between 0-160 μs.

The final PCB board along with the measured pH, impedance, and capacitance are shown on an LCD screen, which is depicted in Fig. 5.10. Finally, the comparison between this design and the state of the art is shown in Table. 5.1. This design is the portable pH/impedance to frequency sensor which can be used for cell culture monitoring. With varying the pH from 1-14, the frequency is variable between 4.90-6.70 MHz, while with varying the impedance from 0-120 kΩ, the frequency is variable between 7.1-10.5 MHz.

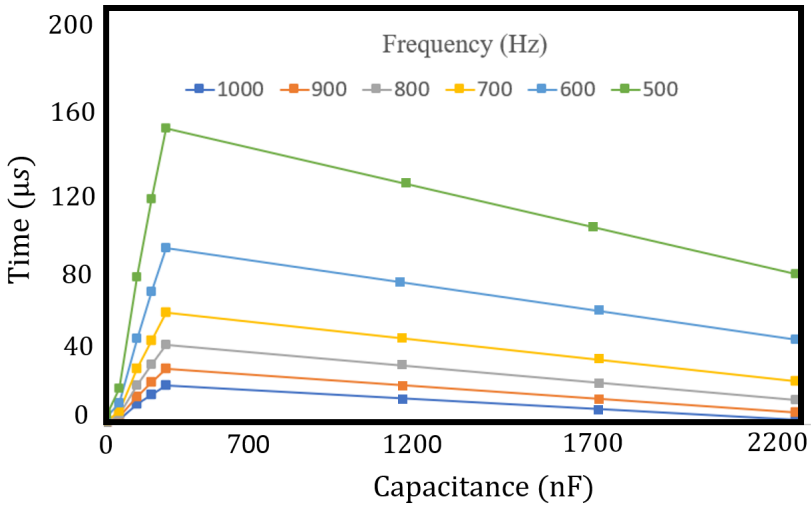


Figure 5.9: Experimental capacitance output frequency for different sets of capacitors.

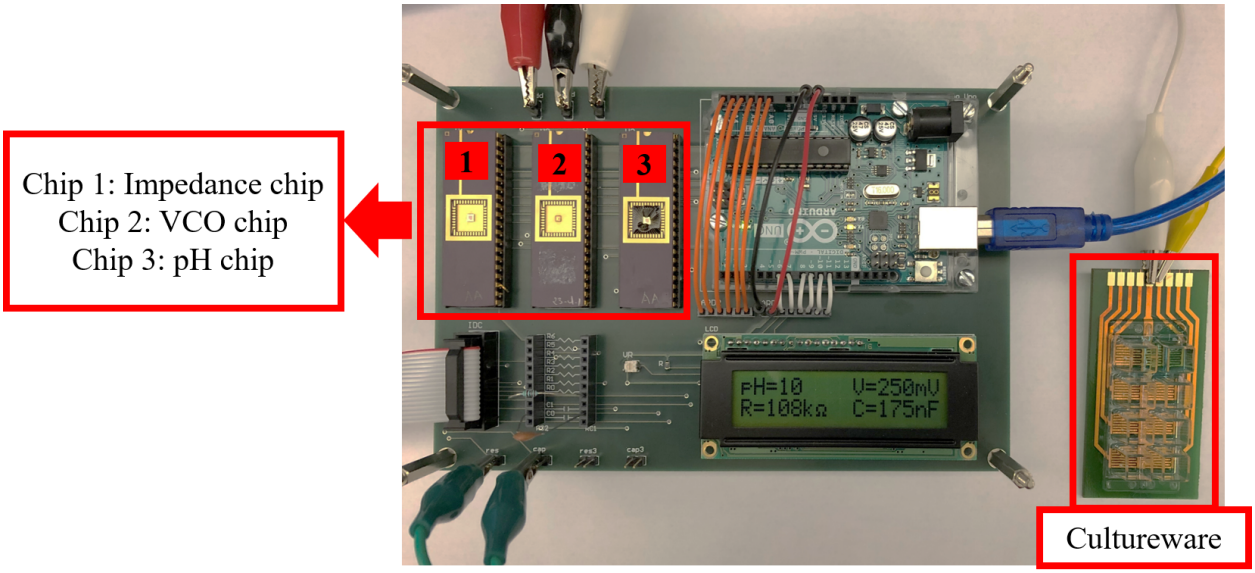


Figure 5.10: PCB design for pH-impedance integrated system.

Table 5.1: Comparison with state of the art.

Reference	Technology (μm)	Sensitivity	Area (mm^2)	Power (μW)	Range (pH, Impedance or Voltage)	Output Frequency	Application
[48] (2006)	0.25	520 kHz/V	0.340	-	0-0.9 V	110-416 kHz	Voltage to frequency
[49] (2011)	0.18	500 kHz/V	-	60	0-1 V	0-501 kHz 510-993 kHz	Voltage to frequency
[50] (2018)	0.18	199.9 (Hz/($\mu\Omega$ /Ω)	0.45	112.5	1.35-1.65 V	85-165 kHz	Voltage to frequency
[51] (2009)	0.35	1 (MHz/V)	-	1030	1.0-2.0 V	1.2-2.2 MHz	Voltage to frequency
[58] (2011)	0.35	-	2	330 nW	10-40 kΩ	6-22 kHz	Impedance to frequency
[80] (2012)	-	-556 Hz/pH	1.2 (cm^3)	-	0-12 (pH) 0-40 (MΩ) (Impedance)	0-20 kHz	pH-Impedance Implantable Wireless
[81] (2019)	0.13	348.8 kHz/V	0.227	78	0-10 mV	0.033-3.48 MHz	Voltage to frequency
[82] (2020)	0.18	287 Hz/pH	0.00042	33 pW	9.15 pH	10 mHz-8 Hz	pH to frequency
[83] (2009)	0.5	-	0.045	5.2	-	0.01-10 kHz	Impedance to frequency
[84] (2015)	0.18		2.7	87	1-12 MΩ	0.7-400 Hz	Impedance to frequency
[85] (2019)	0.13	-	14	-	50 kΩ- 1.2 MΩ	0.2 Hz-22.5 kHz	Impedance to frequency
[86] (2012)	0.13	-	0.01	207	-	1-200 kHz	Impedance to frequency
This work	0.18	138 kHz/pH 40 (mV/pH)	0.006	56	370-630 mV 1-14 (pH) 0-108 kΩ (Impedance)	4.90-6.70 MHz (pH) 7.1-10.5 MHz (Impedance)	pH+ Impedance to frequency

Chapter 6

Integration of the pH Sensors with an on-Chip Processor

Portions of this section is published in,

"ISFET Digital Readout Circuit with an on-Chip MIPS Processor," IEEE Sensors, Rotterdam, Netherlands, Oct 2020.

6.1 MIPS Processor

6.1.1 Design

In the early 1990s, the MIPS processor started licensing their designs to third-party vendors. Compared to the CISC processors, MIPS was successful because of the core's simplicity, which allowed it to be used in several small and cheap applications. This subset of the design employs 8-bit and 32-bit MIPS instruction, and general-purpose registers are named \$0–\$7. In an 8-bit processor, Register \$0 is hardwired to contain 0. The instructions are ADD, SUB, AND, OR, SLT, ADDI, BEQ, J, LB, and SB. The main MIPS code can be written in Assembly language; however, MIPS hardware needs to read the program as 8-bit. Machine language will translate the Assembly code into a high-level language such as C. The

main trade-offs (size, power, speed) in designing MIPS is the selection for the MIPS micro-architecture. The micro-architecture decides how the processor executes the instruction set. The main micro-architectures can be divided into the following groups [87];

Single cycle micro-architecture: It executes each instruction in one clock cycle. This micro-architecture has the best control, but since it executes each instruction in one clock cycle, the processor's speed is chosen by the slowest instruction. It also has a big area since it requires additional hardware.

Multi-cycle micro-architecture: Unlike the single clock, this method uses many clocks to execute each instruction. This permits quick instructions to require few clock cycles while the slow ones require longer clock cycles. Also, it is area efficient in comparison to the previous method.

Pipelined micro-architecture: This architecture employs a single cycle method while adding a pipeline to the execution. Therefore it needs some additional logic to cope with conditions among different cycles and pipelines.

As claimed by [88], utilizing on-chip elements vs. off-chip one resulted in power savings of 28% to 36%, an energy savings of 13% to 35%, and also fast execution time in the range of 1% to 29%. In this design, a pipelined micro-architecture was used. The block diagram is shown in Fig. 6.1 with the inputs, which are summarized in Table 6.1. For ignoring the hold-time problems, this specific MIPS used a two-phase clocking system (ph1 and ph2). Reset input arranges the PC to 0 and initializes the FSM to the beginning state. The leftover portion of the signals is utilized for an 8-bit memory interface. The processor sends an 8-bit address ADR and optionally asserts MemWrite. There will be two cycles in there; on a read cycle, the memory returns a data on the MemData, and on a write cycle, the memory gets inputs from WriteData.

Fig. 6.2 shows the layout of the 8-bit MIPS processor both in Encounter and Cadence. Generally, the physical design starts with a floor-plan. After synthesizing the Verilog code in Synopsys, the floor-plan will take place. The floor-plan gauges the zone of major units within the chip with considering the dimensions and characterizing their relative arrangements. The floor-plan is fundamental to determine whether a proposed design will fit within the chip area budgeted and assess wiring lengths and wiring congestion.

Table 6.1: Top-level inputs and outputs (8-bit MIPS processor).

Inputs	Outputs
ph1	MemWrite
ph2	Adr [7:0]
reset	WriteData [7:0]
MemData [7:0]	

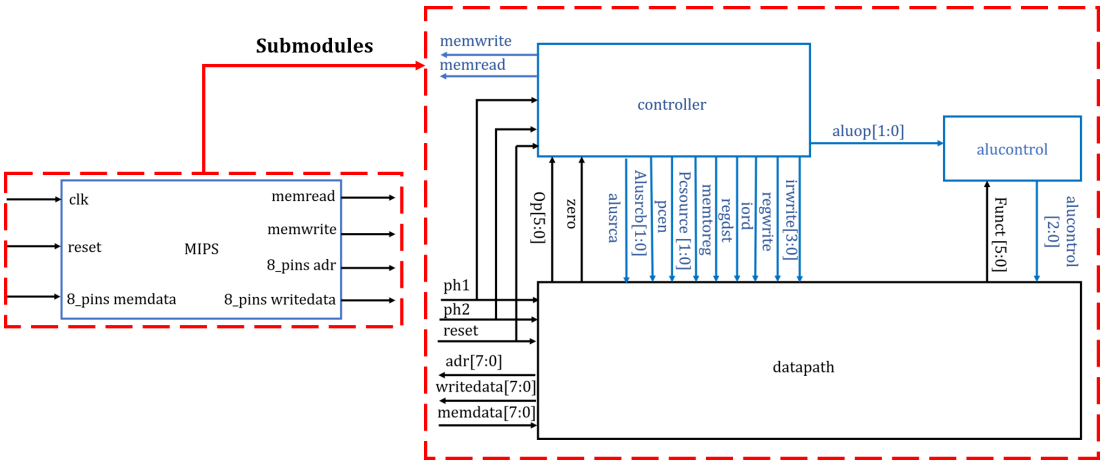
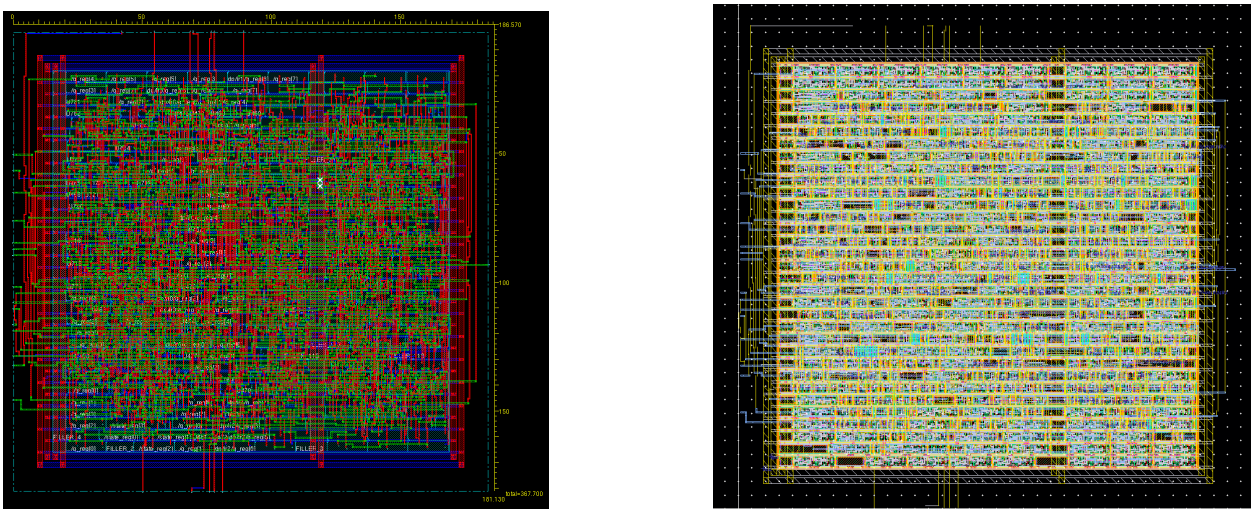


Figure 6.1: Top-level 8-bit MIPS processor along with the subsystems using 1-poly 3-metal 180 nm CMOS process.



(a) **(b)**

Figure 6.2: 8-bit MIPS layout using standard 1-poly 3-metal 180 nm CMOS process in (a) Encounter, (b) Cadence Virtuoso.

We used the standard cells from standard 1-poly 3-metal 180 nm CMOS process to synthesize the Verilog code and to import it in Encounter. In this design, the supply rails have a width of 8 λ to carry more currents and were separated 90 λ center-to-center (λ is determined based on the process selection parameters). Supply powers were used by metal 1, which runs horizontally. Inputs and outputs were drawn in metal 2 in a vertical axis. For inserting the NMOS and PMOS transistors, the NMOS transistors were placed in the bottom 40 λ while the PMOS transistors were placed in the top 50 λ. After floor-planning and when the layers were ready in the design, placing and routing the wires took place. We exported this file and then imported it in Cadence, with standard 1-poly 3-metal 180 nm CMOS process. The final size is 0.0338 mm^2.

The Verilog code for an 8-bit MIPS processor was customized in a way to have the ability to store and process more data (32-bit). The same procedures from synthesizing, floor-planning, placing and routing, and exporting in cadence were performed on the 32-bit code. Fig. 6.3 shows the synthesized 32-bit MIPS block diagram with its sub-modules. The final layout for 32-bit MIPS in Encounter is shown in Fig. 6.4. The amoeba plot is shown to observe the result of cells and hard blocks placement. The area is 1.83 mm^2. Since the 32-bit processor has more sub-modules, the area is larger than the 8-bit processor.

6.1.2 Simulation Results

Vivado was used for simulation. Generally speaking, MIPS consists of several inputs and outputs. The inputs can be divided into the clock, reset, and Memdata and the outputs can be divided as MemWrite, Adr, and writeData. A clock signal is used for avoiding hold-time problems. Reset signals initialize the PC to 0 and the FSM to the start state. For interfacing, the memory with the processor, MemData [7:0], is used. For the processing in MIPS, the processor sends an 8-bit address and sets it on MemWrite. During the read cycle, the data asserts MemData. The simulation results are shown in Fig. 6.5. Based on the results, the data flow in the circuit. It indicates that the registers function properly for further process. Simulation results for the 32-bit MIPS processor are depicted in Fig. 6.6.

6.2 ARM Processor - Cortex M0

6.2.1 Design

The Cortex-M0 has an exceptionally small silicon area enabling developers to achieve 32-bit performance. This processor was designed to enable developers to create cost-sensitive and power-constrained solutions for a vast numbers of the applications. It is available for a low cost with Arm DesignStart. It consists of several parts like power management controllers unit, input/output controllers, and system controllers. After purchasing the Verilog codes from ARM, we synthesized the codes in "Synopsys Design Compiler", which resulted in creating the transistor level netlist. The top-level block diagram, with its sub-modules, is shown in Fig. 6.7. Also, this block has memory modules (Flash and SRAM) integrated with it. Table. 6.2 explains the input and output pins. The sub-modules of the ARM processor are listed as following,

- **Pin-mux**: pin multiplexer and tristate buffers for the I/O port.
- **System**: microcontroller system-level design.
- **Clkctrl**: clock and reset control.
- **PMU**: power management unit.
- **Rst-ctrl**: clock and reset control.
- **Bootloader**: debugging the system.
- **RAM**: RAM of the system.
- **ROM**: ROM of the system.

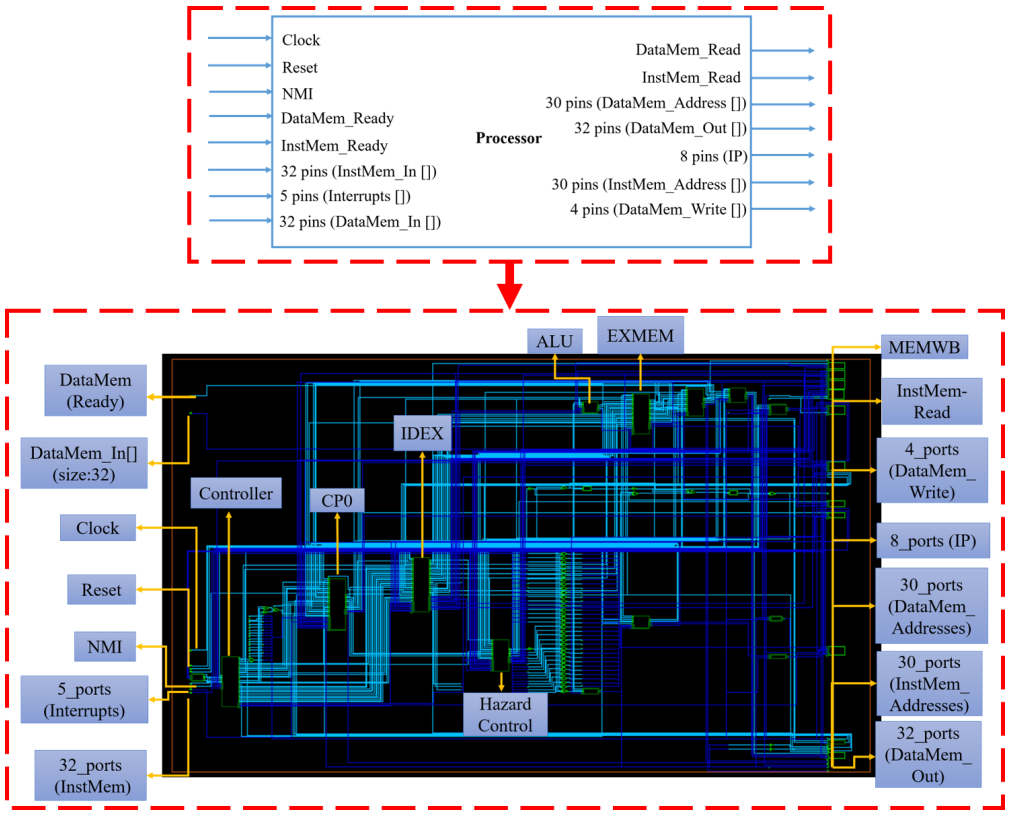
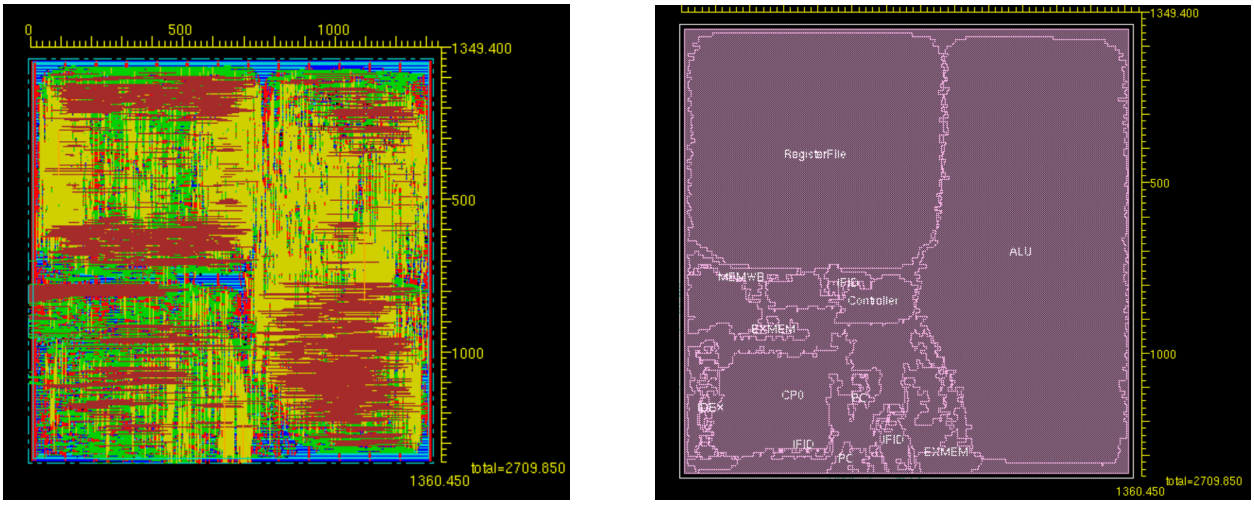


Figure 6.3: Top-level 32-bit MIPS processor along with the subsystems using 2-poly 6-metal 180 nm CMOS process.



(a) **(b)**

Figure 6.4: 32-bit MIPS layout using 2-poly 6-metal 180 nm CMOS process standard cells in Encounter, (a) Layout. (b) Amoeba placement.

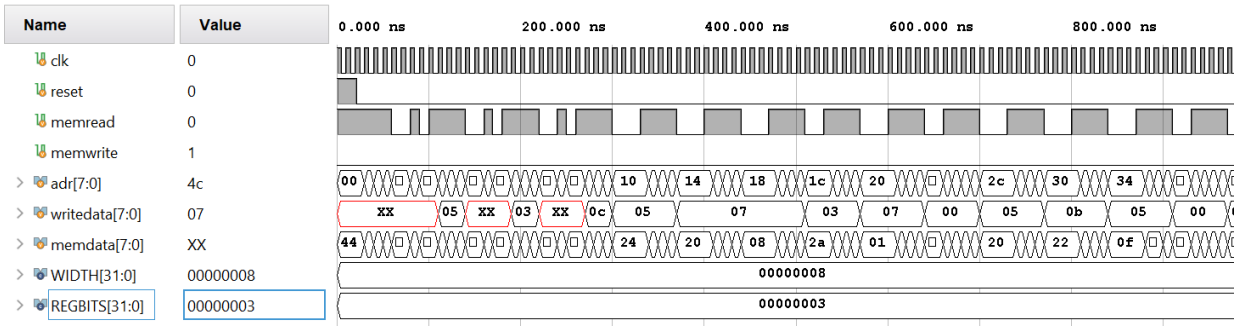


Figure 6.5: Verilog simulation results in Vivado for 8-bit MIPS processor.

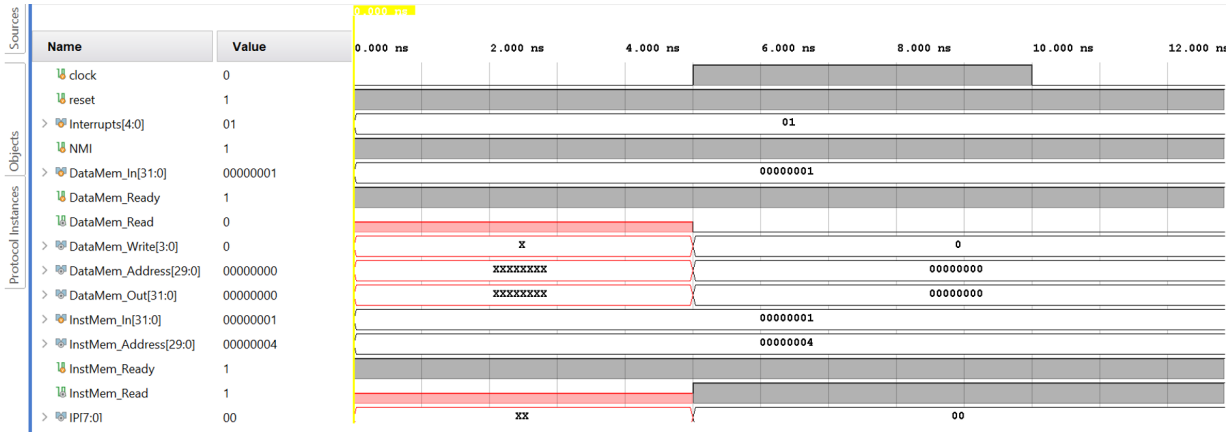


Figure 6.6: Verilog simulation results in Vivado for 32-bit MIPS processor.

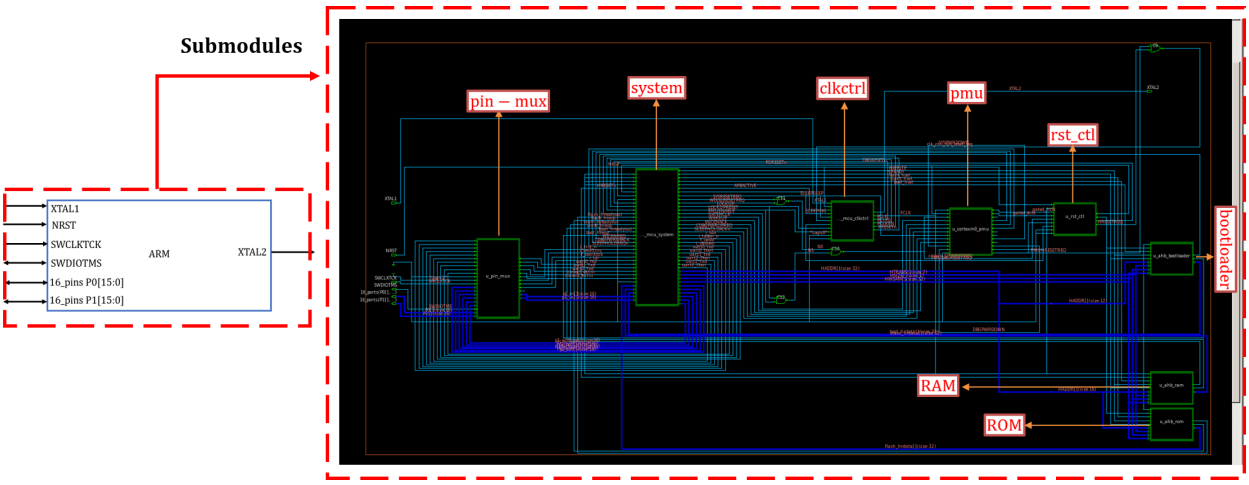


Figure 6.7: Top-level 32-bit ARM processor along with the subsystems using 1-poly 3-metal 180 nm CMOS process.

Table 6.2: Top-level inputs and outputs (32-bit ARM processor).

Signal	Direction	Description
XTAL1	Input	Crystal oscillator
XTAL2	Output	Crystal oscillator feedback
NRST	Input	Reset, active LOW
P0[0:15]	I/O	GPIO
P1[0:15]	I/O	GPIO
SWCLKTCK	Input	Debug signal
SWDIOTMS	I/O	Debug signal

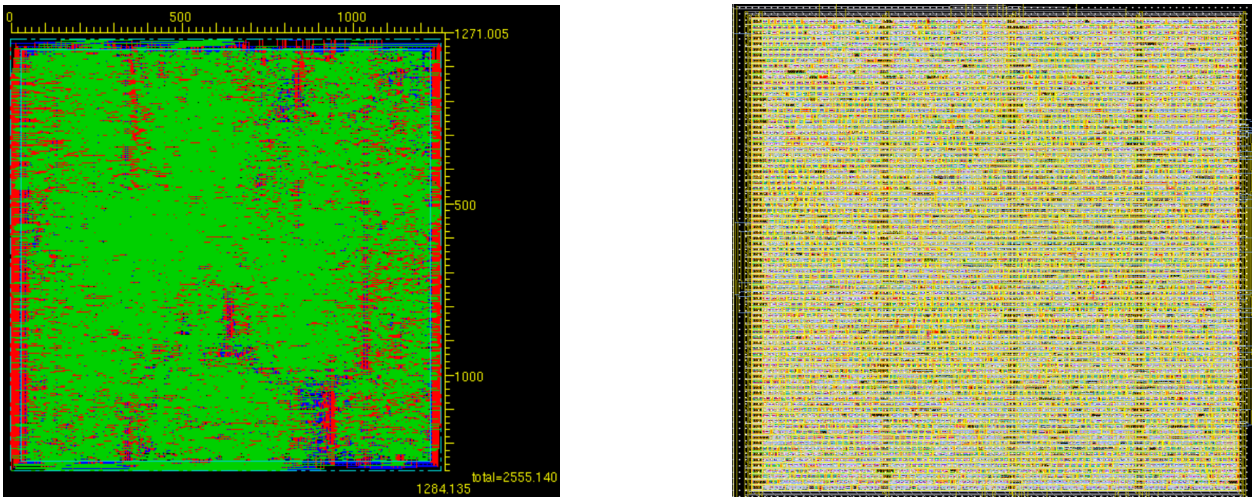
After synthesizing the Verilog code, the netlist was imported into Encounter to generate the layout. By importing the netlist in the Encounter, floor-planning, and placing and routing, the layout was generated. The final layout in encounter and cadence is shown in Fig. 6.8. The final size is 1.7 mm^2. In Encounter, the size was opted on no DRC errors.

This processor was integrated with an analog front-end to be used as a smart ASIC digital gas sensor. The analog front-end was designed by the University of Maryland. The final ASIC consists of several components; the analog front-end (AFE), which includes the offset cancellation and amplification of the bridge sensor outputs, the successive approximation ADC, the clock generator, the LED driver, the sensor supply voltage regulator, the pad frame, the digital control logic, and other miscellaneous circuits including on-chip bias generators and buffers. The fabricated chip is shown in Fig. 6.9.

6.2.2 Simulation Results

Vivado was used for simulation. Generally speaking, ARM consists of several inputs and outputs. The inputs can be divided into XTAL1, NRST, and SWCLKTCK, and the outputs can be divided as XTAL2. Other pins can be considered either as an input or an output. A clock signal is used for avoiding hold-time problems. Reset signals initialize the PC to 0 and the FSM to the start state. For interfacing, the memory with the processor, p0 [15:0], is used.

To check the processor before fabrication, post-layout simulations of the processors (MIPS and ARM) were performed in cadence. The results are shown in Fig. 6.10. By applying an external clock and inserting an input as data, the data flows to the processor and demonstrates it as an output. V_{in} was set to 0-5 V, and the clock was set to 1 MHz. The input is shown over a time, passing through the processor. The simulations from both MIPS and ARM are an indication that they are functioning properly. These processors are integrated with other front-ends to do calibration and processing.



(a) (b)

Figure 6.8: 32-bit ARM layout using standard 1-poly 3-metal 180 nm CMOS process in (a) Encounter. (b) Cadence.

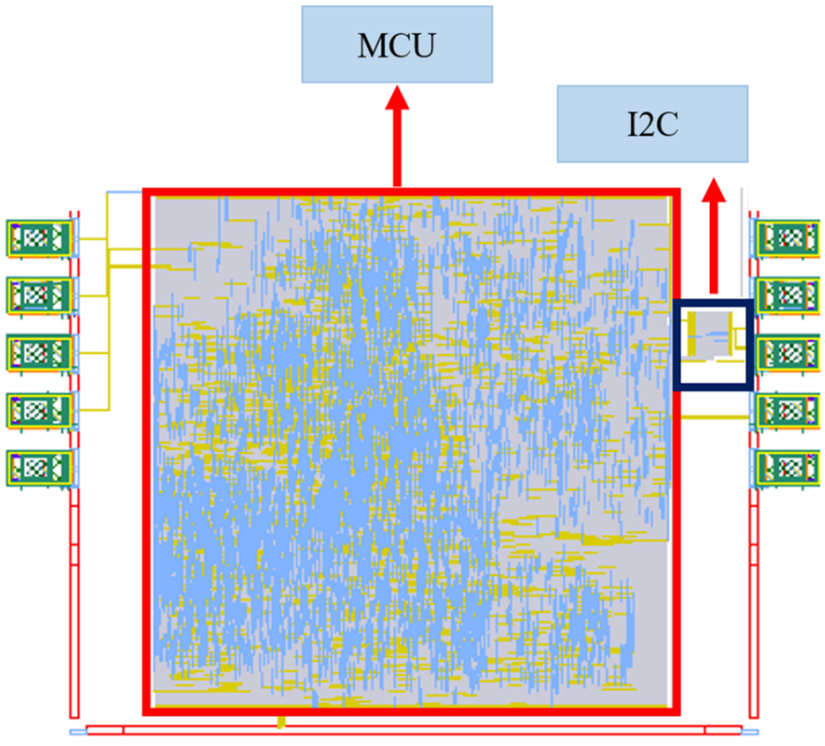
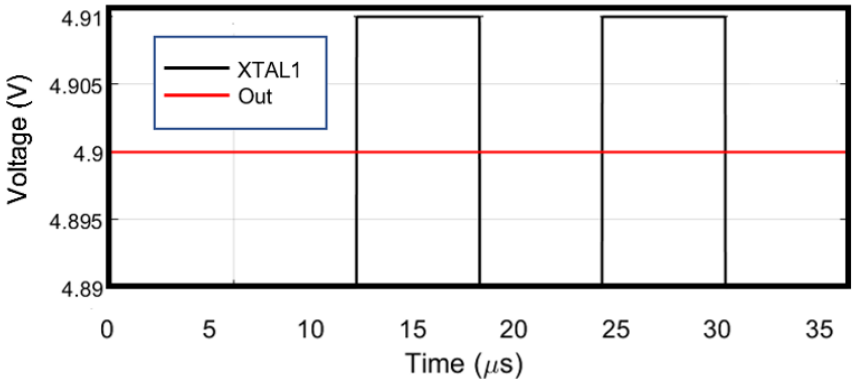
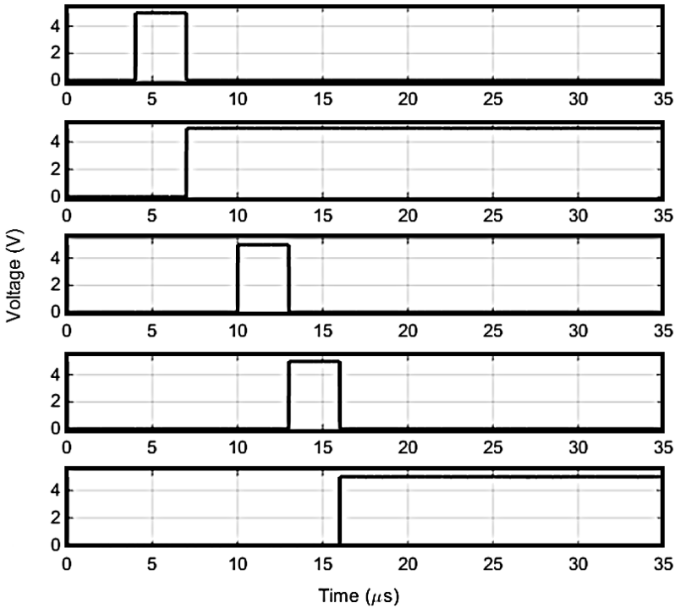


Figure 6.9: MCU-I2C connection in cadence using standard 1-poly 3-metal 180 nm CMOS process.



(a)



(b)

Figure 6.10: Post-layout simulations of the processor (a) ARM processor, (b) MIPS processor.

Generally, the I2C module is used for transferring the signal from MCU to the outside world. This module's schematic is shown in Fig. 6.11, which consists of the Byte controller and several blocks of the registers. GitHub open source website was used for downloading the I2C Verilog code [89]. The simulation is shown in Fig. 6.12. MCU and I2C makes a connection in a way that at the end of the first byte, it is time for the MCU to acknowledge the access, or not. After receiving and decoding the address byte in MCU, the MCU outputs acknowledge on the SDA line. To do this, it will pull the SDA signal low, and release it after the acknowledge is complete. The acknowledge line is the combination of low and high signals. After the acknowledges, MCU will then begin transmitting each byte of data. After first iteration, the data waits a specified sampling interval, activates the PWM, waits a ramp-up duration, then takes a measurement of each of inputs, flags MCU to read, then goes to a wait mode until the next sampling interval.

6.3 Comparison between MIPS and ARM Processors

Two designs (MIPS and ARM) are shown in Table. 6.3. The MIPS processor has a smaller power consumption than the ARM processor. While the ARM processor performs faster due to its higher clock speed, clocks are chosen to have no timing violations in the system design. This also helps the system to have positive slack during the operation. The main reason for choosing this size of memory is based on the results which were derived from Arduino-Uno. The Arduino that integrated with the customized portable PCB board has an ATMEGA328p processor, with 32 kB Flash and 2 kB SRAM.

6.4 Integration of the pH Sensor with on-Chip Processor

Previously Arduino was used with the ISFET [19], but the system design was improved using an on-chip processor to save power and size, making the design more efficient. The system diagram is shown in Fig. 6.13. The front-end is a voltage-clamped ISFET with a combination of the quasi-digital circuit and a counter. The output from this design is

connected to an 8-bit MIPS processor. As detailed previously in chapter III, the fabricated front-end pH sensor was designed in 0.5 μm CMOS technology. The final layout is shown in Fig. 6.14. In summary, the power consumption of the front-end ISFET is 315 nW, and the sensitivity is 50 mV/pH. The power consumption of the ISFET sensor integrated with the quasi-digital technique and counter is 206 μW. The counter and the SR-latch's transient responses are shown in Fig. 6.15 (a). For the experimental measurements, a Keithley source meter was used to sweep the input voltages from 450 to 1158 mV, calculated based on the pH values 1-14. The supply voltage set to 3 V. By varying the input voltages, the data's bitstream were generated. The number of the generated bitstream is 23 pulses for the input of 901.55 mV.

An on-chip 8-bit MIPS processor was used for processing the generated bitstream of data and doing the calibration. One goal is to store the bitstream data in memory displayed on an LCD for portable applications. The processor will also convert the voltage to a pH value based on an initial calibration experiment. When data enters the processor, it passes through multiple pipelined stages. Calibration is performed after compiling and uploading the instruction code onto the fabricated processor. Reset signals initialize the processor to 0 and the FSM to the start state. If the reset is logic 1, the MIPS processor is in an idle mode. If the reset is low, then the data from the pH sensor is transferred to the registers. When the pH sensor output is valid on the processor input, the Arithmetic Logic Unit (ALU) will perform the pre-loaded instructions, like calibration on the sensor. Notably, Memdata receives the results upon the execution of those specific instructions for loading and storing. Finally, in the writing stage, the executed data will be displayed on an LCD. Simulations results using Vivado is shown in Fig. 6.15 (b).

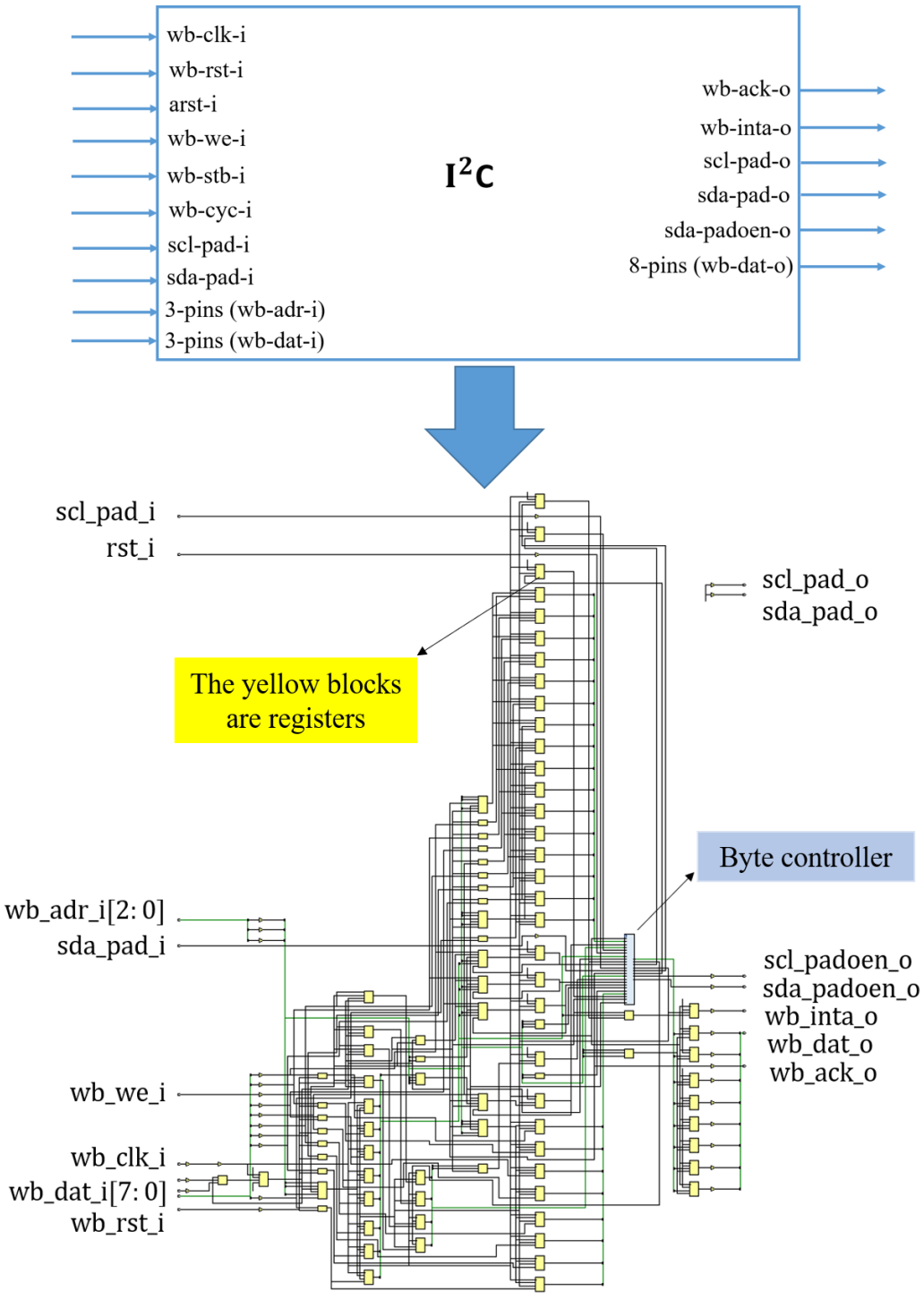
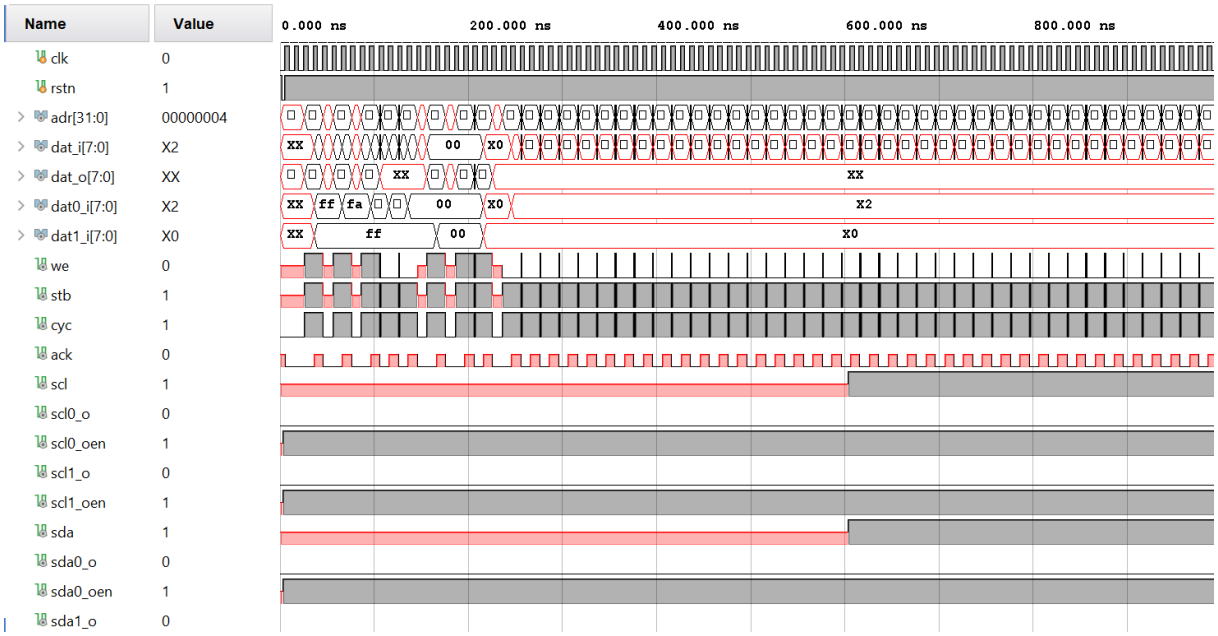
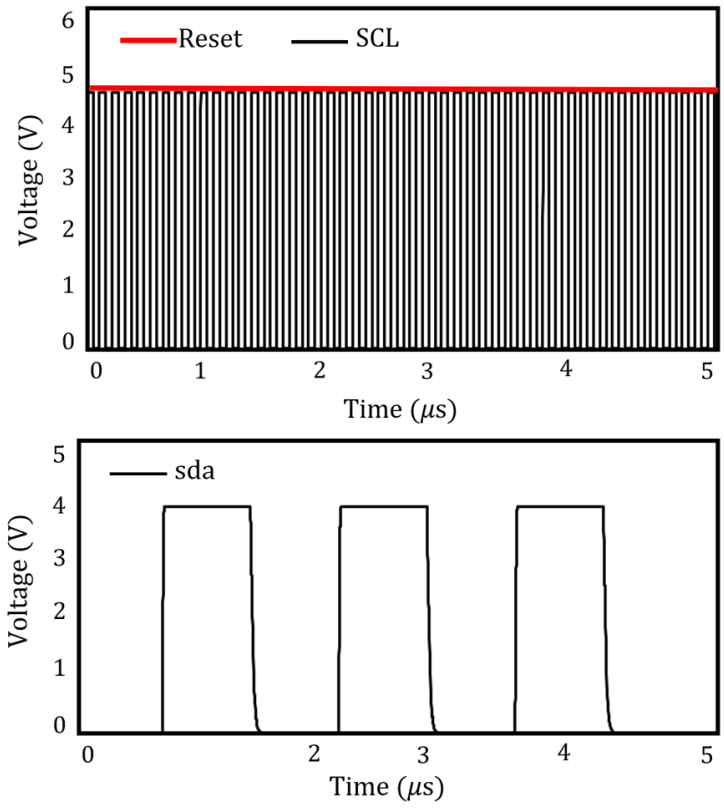


Figure 6.11: Block diagram of the I2C along with the schematic view.



(a)



(b)

Figure 6.12: Simulation and post-layout simulations for I2C module in (a) Vivado, and (b) Cadence (Data is asserted on the sda line and the output is shown).

Table 6.3: Comparison between MIPS and ARM specifications.

Core	32-bit ARM Cortex-M0	8-bit MIPS	32-bit MIPS
Data Bus Width	32 (bit)	8 (bit)	32 (bit)
Number of I/Os	30	16	34
Layout Size	1.7 (mm^2)	0.0338 (mm^2)	1.8 (mm^2)
Power	81 (mW)	36 (mW)	66 (mW)
Clock	50 (ns)	1 (μs)	100 (ns)
Speed	20 (MHz)	1 (MHz)	10 (MHz)
RAM	4 (kB)	-	4 (kB)
ROM	32 (kB)	-	32 (kB)

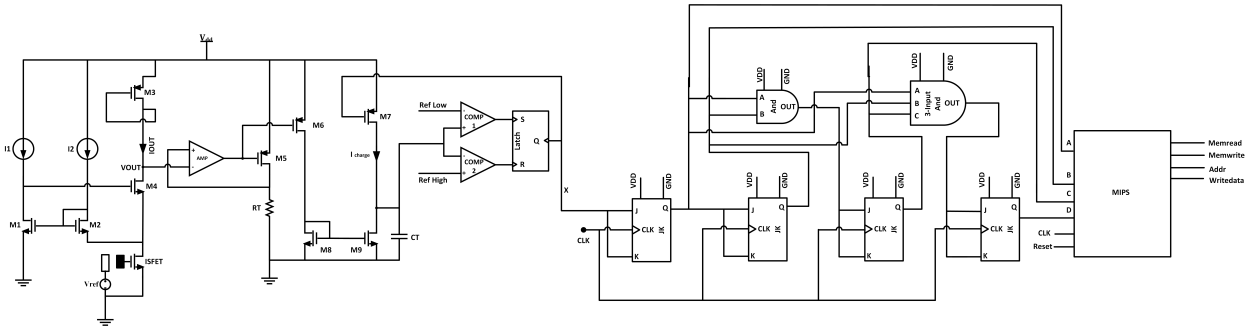


Figure 6.13: Implementation of the pH sensor with a MIPS processor. The front-end consists of the voltage-clamped pH sensor, quasi-digital technique, and a counter.

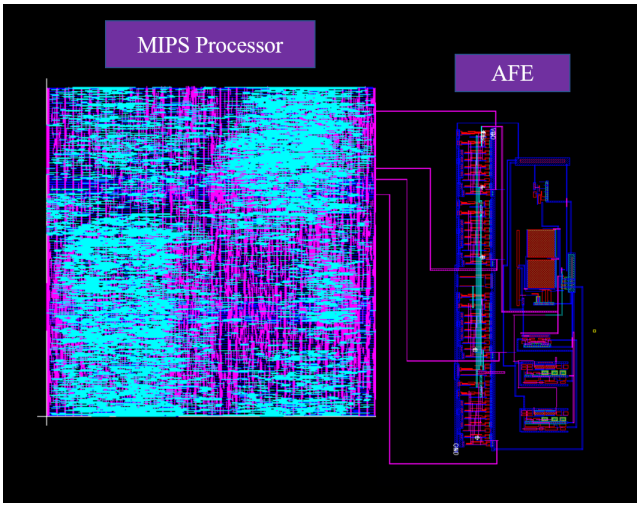


Figure 6.14: Layout of the integrated pH sensor with 8-bit MIPS processor.

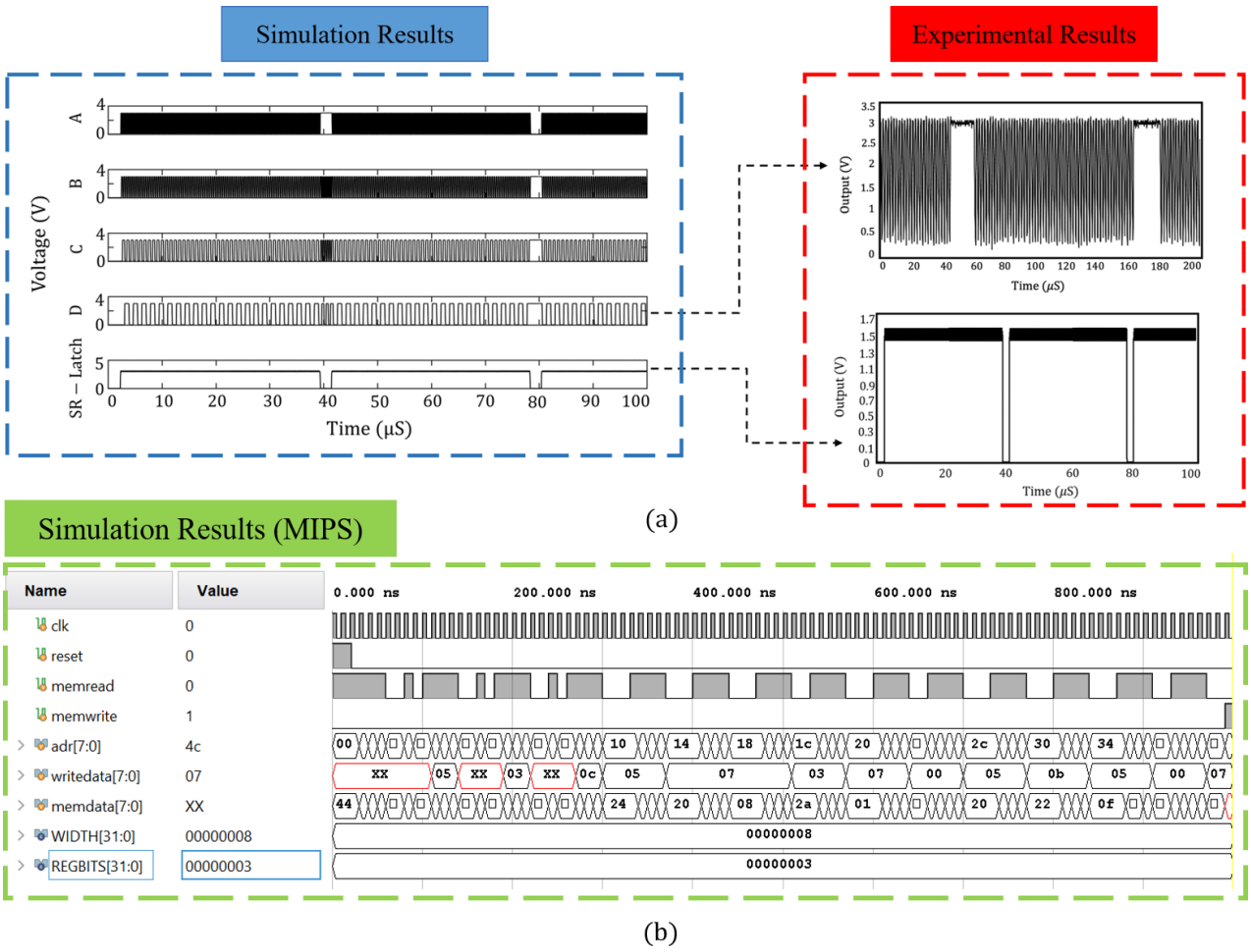


Figure 6.15: (a) Simulation and experimental results for analog front-end. (b) Timing diagram derived from synthesis and simulation 8-bit MIPS processor in Vivado.

6.4.1 Implementation of the ISFET pH Sensor and the Processor in FPGA Platform

FPGA has some advantages like having a low cost and being re-programmed in the field for error correction. Using the HDL code allows the FPGA to be applicable to be used by different applications. We used the FPGA in our design to prototype the MIPS processor with the ISFET pH sensor. Generally speaking, FPGAs are reliable platforms in the design of embedded systems. The FPGA that we used was NEXYS 4 DDR, which features Xilinx Artix-7 XC7A100T-ICSG324C FPGA. The Artix-7 FPGA has more capacity, higher performance, and more resources than the initial designs. It can be used in different fields like introductory circuits to some powerful embedded processors. Implementation was done within the following procedure,

First, the Verilog code downloaded from the MIPS open-source website was synthesized and implemented in Vivado. After that, the bitstream was generated to be able to be compiled on the FPGA. After compilation, the FPGA board was connected to the ISFET pH sensor, which was integrated with the counter. The test setup is shown in Fig. 6.16.

6.5 Calibration

Each time solution is applied to the chip area, the chip's initial pH scale reading will begin with a unique and different amount based on Nernest equation. To compensate this uncertainty in calculating the pH scale, calibrating the chip design is very important.

The calibration was performed by applying pH 7 on the chip and recording the output voltage. Those measured value was used for calculating the actual pH. The data from the analog front-end entered the digital pins of the microcontroller. The next stage corresponds to the sensor's initial calibration to the pH level of 7, and it recorded the respective voltage determined by the equations (6.1 and 6.2).

$$V_{FG} = \frac{C'_{pass} \times A}{C'_{pass} \times A + C_{eox}} \times (V_{Ref} - V_{Chem}) \tag{6.1}$$

$$V_{out} = \sqrt{\frac{K_{n1}(Input2-V_{TN})^2(1+\lambda_8(V_{D_8}-V_{DD}))}{K_{n_5}(1+\lambda_5(V_{D_8}-\frac{2I_{out1}}{\lambda_4 K_{n_4}(Input1-V_{TN})^2}+\frac{\lambda_5}{\lambda_4}))}} + V_{TN} + \frac{2I_{out1}}{\lambda_4 K_{n_4}(Input1-V_{TN})^2} - \frac{1}{\lambda_4} \tag{6.2}$$

Then it determined the program for interfacing with LCD. It used the transfer output serial data from the microcontroller to the Wi-Fi module for communication with the outside world. Fig. 6.17 is the calibration setup along with the flow-chart for the proposed system that shows the operation sequence of the program. The calibration was performed on the differential voltage-clamped pH sensor along with the PCB board and the Arduino Uno. The result is shown in Fig. 6.18. Based on the results, the calibration improves the non-linearity in the sensor. This non-linearity is because of the ISFETS moving their region of operation when the input voltage changes.

6.6 Conclusion

MIPS (Microprocessor without Interlocked Pipeline Stages) is among the most used RISC (Reduced Instruction Set Computer) processors. The MIPS architecture has found its way into CISCO Routers, digital TV, cable modems, and many more household appliances due to its designer-friendly composition. With a synthesized in programmable hardware from software descriptions written in HDL in MIPS, a soft-core processor provides flexibility, reduced cost, and longevity of utility to a wide array of applications. The digital system can be directly integrated with the pH ISFET sensor on the same chip. The pH sensor is then integrated with a processor. In the previous chapters and the first design, the implementation was implemented using discrete parts like Arduino and ADC blocks. Using an on-chip processors, the system has great advantages over more common digital methods, including lower power and lower size.

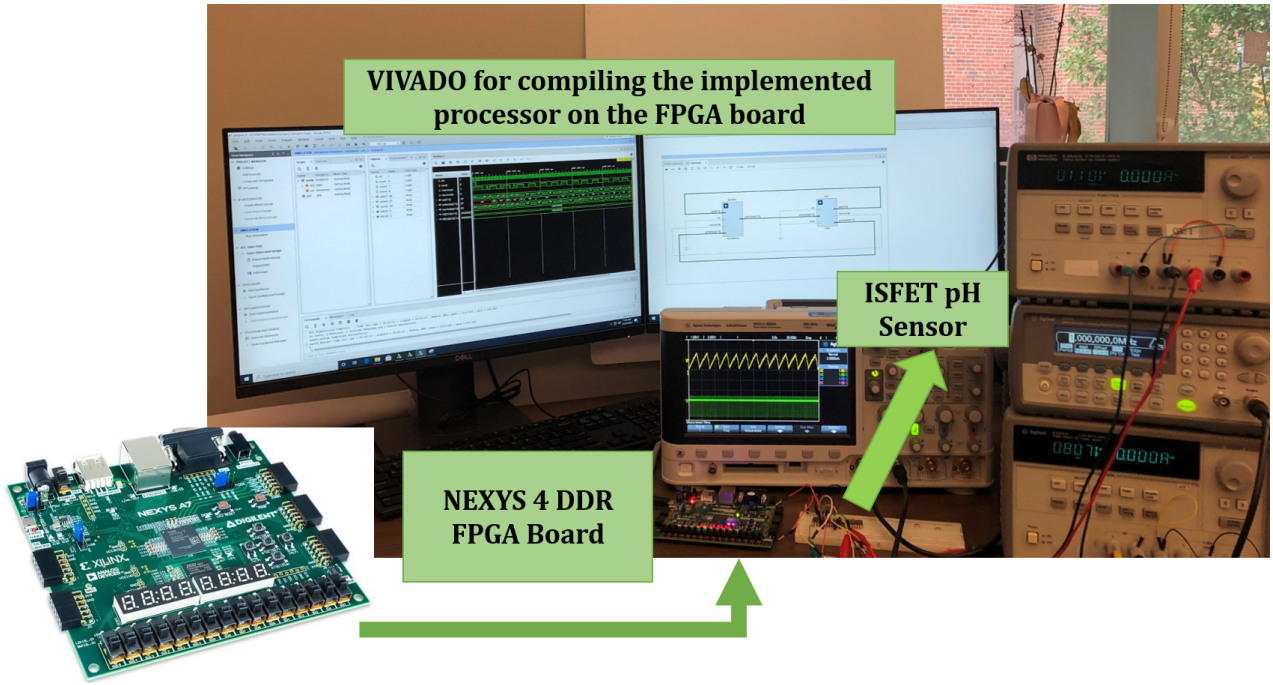


Figure 6.16: Implementation of the ISFET pH sensor along with the MIPS processor, using FPGA platform.

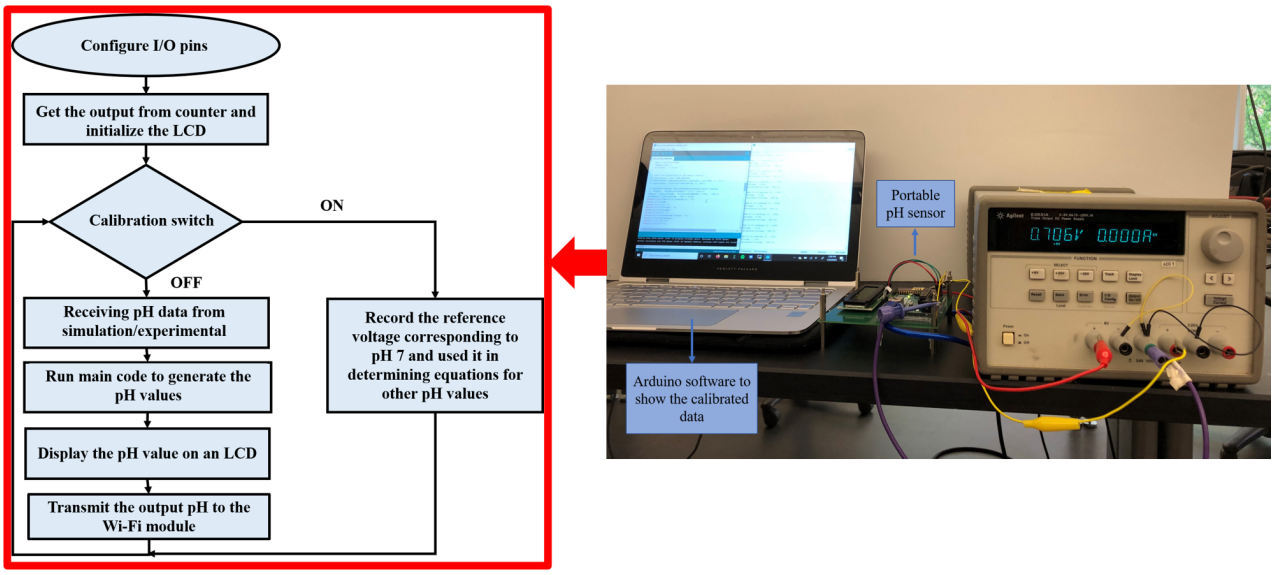


Figure 6.17: Calibration setup along with the flow-chart.

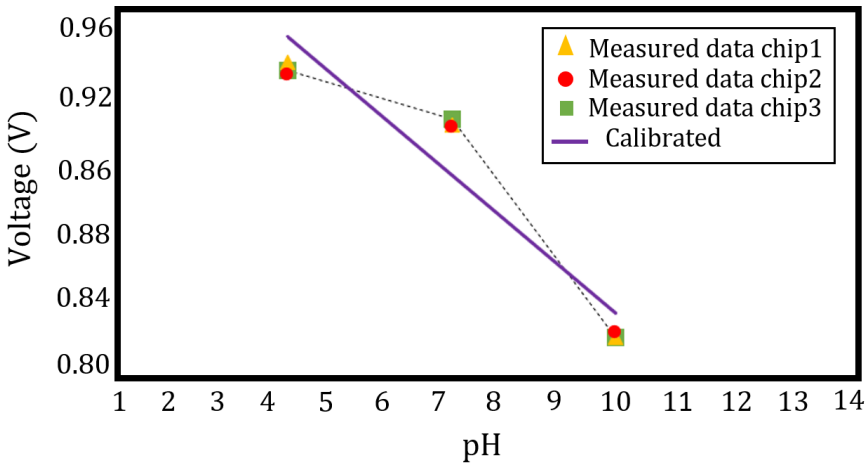


Figure 6.18: Results based on the calibration.

Chapter 7

Conclusion

From the beginning of 2020, we faced a pandemic surpass the world. The Covid-19 widespread has produced expanded mindfulness of the noteworthy points of interest and conceivable outcomes of using portable medical devices at home. These portable medical devices are categorized based on the product (fitness and wellness, medical monitoring and imaging, and medical therapeutics) and based on applications (cardiology, gastrointestinal, gynecology, neurology, and orthopedics). According to the research, at a Compound Annual Growth Rate (CAGR) of 10.68 %, the number is anticipated to rise from USD 29,886.56 Million to USD 54,947.05 Million from 2019 to 2025 [90]. So this shows an on-going research over the portable medical devices.

7.1 Original Contribution

In this work,

- The differential voltage-clamped ISFET was designed, which used two electrodes with different size areas, eliminating the need for post-processing and making the design cost-efficient.
- A portable pH sensor was presented. Several readout circuits were shown which step further than the state-of-art design by providing low-power and low-area designs with frequency output.

- To digitize the design, the pH sensor used sub-threshold CMOS technology and window voltage comparators to translate the pH to voltage and frequency. A counter was added to the design for generating the bitstream of data.

- Integrating an on-chip processor with sensors was then presented that took the initial step towards having a smart digital pH sensor. This on-chip processor saves the area and power budget. The on-chip processor block was implemented using low-power MIPS and ARM Verilog codes. This is the first implementation of sensors with an on-chip processor on the same chip. The power consumption of the integrated on-chip processor is pretty much lower than off-chip processors like Arduino. Also, the size is smaller than the discrete version (implementing on the PCB board). This decrease in power and size is an indication that this method is a promising method to implement on-chip processors in portable and wearable devices in the age of quantum computing.

7.2 Possible Future Paths

There are a number of future possible paths for this research.

1. More sensors (for example, temperature, impedance, and humidity sensor) can be integrated with the existing sensor to have a complete standalone sensing system. For example a combined pH, temperature, and impedance sensor, arrayed as the base of a smart culture dish can monitor biological cells in real time. A wearable/portable pH, impedance, temperature, and optical sensor for pulse oximetery could be helpful in giving early warnings and mitigating respiratory distress.

2. To reduce chip area and power, Machine Learning techniques can be incorporated into the chip.

3. Since most portable devices need to be connected to the smart cell phones, a wireless transmitter capable of sending the signal out of the processor to the mobile applications can be considered as another future path.

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Appendices

A Layouts of the Proposed Circuits in Cadence

In this appendix, the layouts of the proposed designs are illustrated.

1. Differential Voltage-Clamped pH Sensor:

The layout of the differential voltage-clamped ISFET pH sensor, along with two electrodes, was implemented in 0.5 μm CMOS technology and is shown in Fig. 1. The supply voltage was set as 2 V. Pins 1-3, 30, and 32 were used for this specific design. Table. 1 shows the pins' numbers and the pins' names related to the schematic and the pad frame.

2. A Low-Power Voltage-Clamped pH to Frequency Sensor:

The pH to frequency sensor's layout was implemented in 0.18 μm CMOS technology and is shown in Fig. 2. It consists of several blocks like a voltage-clamped ISFET pH sensor, an amplifier, SR-latch, and two comparators. The power supply for all blocks in this design was set as 1.8 V. The reference voltage in ISFET was about 0.9 V. Two bias voltages for the voltage window comparators were used, 700 mV and 850 mV. The system's speed is determined by the voltage window comparator since there is a loop with charging and discharging the capacitor. The whole pad frame is shown in Fig. 3. Pins 22-27 and 32-33 were used for this design. Table. 2 shows the pins' numbers and the pins' names related to the schematic and the pad frame.

3. Integration of ISFET pH Sensor with Counter:

The layout of the integrated voltage-clamped ISFET pH to frequency sensor along with counter was implemented in 0.5 μm CMOS technology and is shown in Fig. 4. V_{ref} of the design was 0.9 V. The ISFET output voltage was variable from 0.75-1.03 V, which was acting as an input for the second part. The whole chip design, along with separate sub-modules, is shown in Fig. 5. Pins 16-22, 24, 30, and 32 were used for this specific design. Table. 3 shows the pins' numbers and the pins' names related to the schematic and the pad frame.

4. Pad frame of the Integrated ARM Processor with a Gas Sensor:

The pad frame of an ASIC design, which was designed in 1-poly 3-metal 180 nm CMOS process, is shown in Fig. 6. Pins 2 and 26-29 were used for this specific design. Table. 4 shows the pins' numbers and the pins' names related to the schematic and the pad frame.

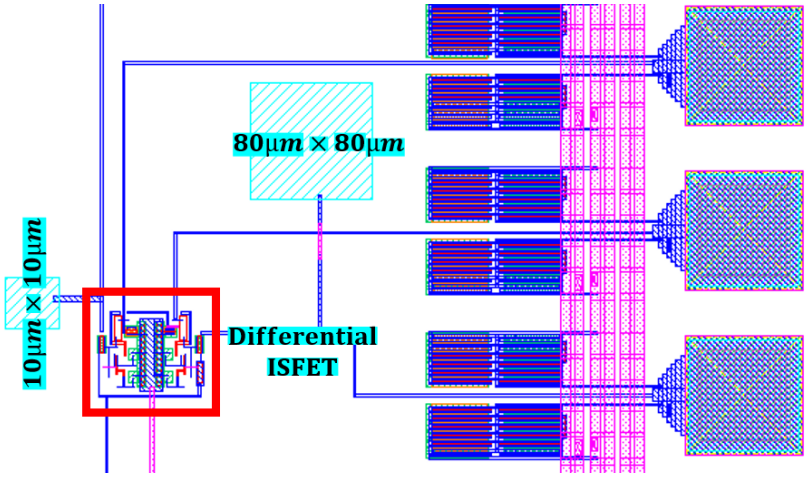

Figure 1: The layout of the differential voltage-clamped pH sensor fabricated in 0.5 μm CMOS technology.

Table 1: Pin names and numbers (Matched with Fig. 3.4a in chapter 3, section 3.2.)

Numbers	Names
1	V_{FG} (ISFET2)
2	V_{Out}
4	V_{FG} (ISFET1)
30	GND
32	Vdd

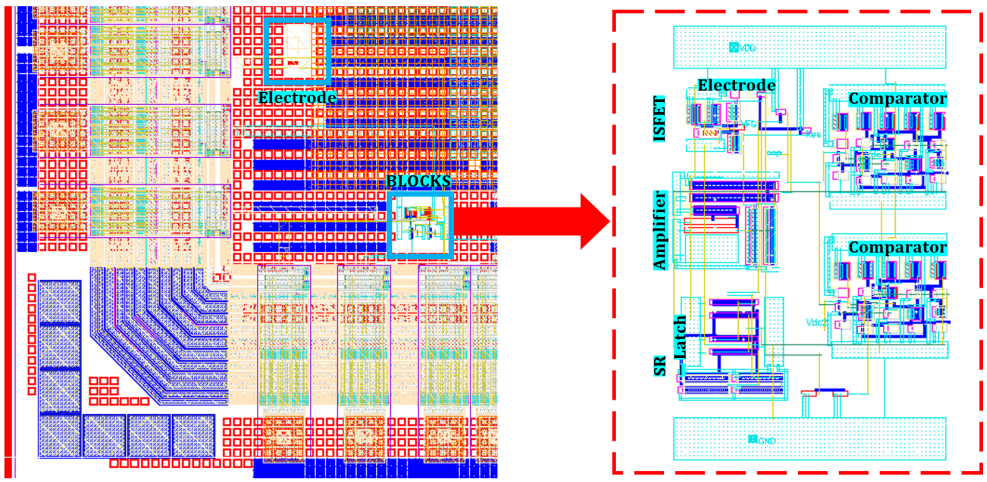

Figure 2: Layout of the pH to frequency sensor fabricated in 0.18 μm CMOS technology.

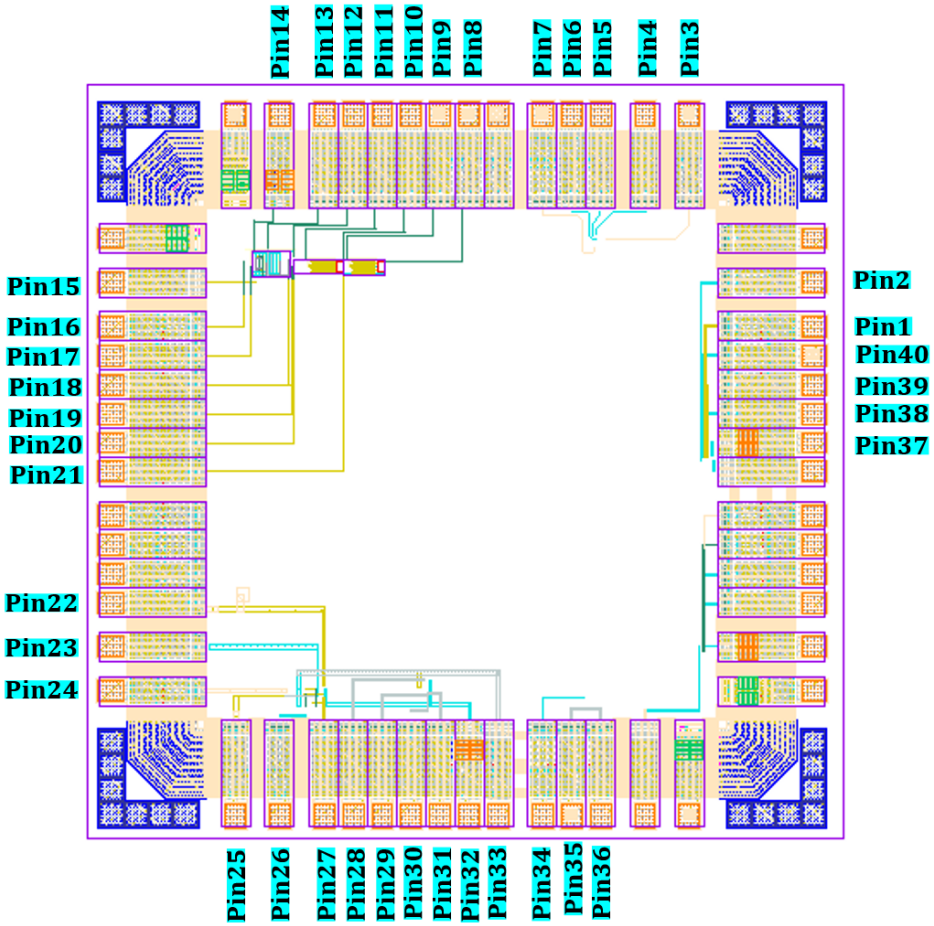

Figure 3: The whole pad frame for the pH to frequency sensor fabricated in 0.18 μm CMOS technology.

Table 2: Pin names and numbers (Matched with Fig. 4.1a in chapter 4, section 4.1.)

Numbers	Names	Numbers	Names
22	V_{FG} (ISFET)	26	SR-latch Output
23	Capacitor (C_T)	27	Resistor (R_T)
24	Ref-High (comparator)	32	Vdd
25	Ref-Low (comparator)	33	GND

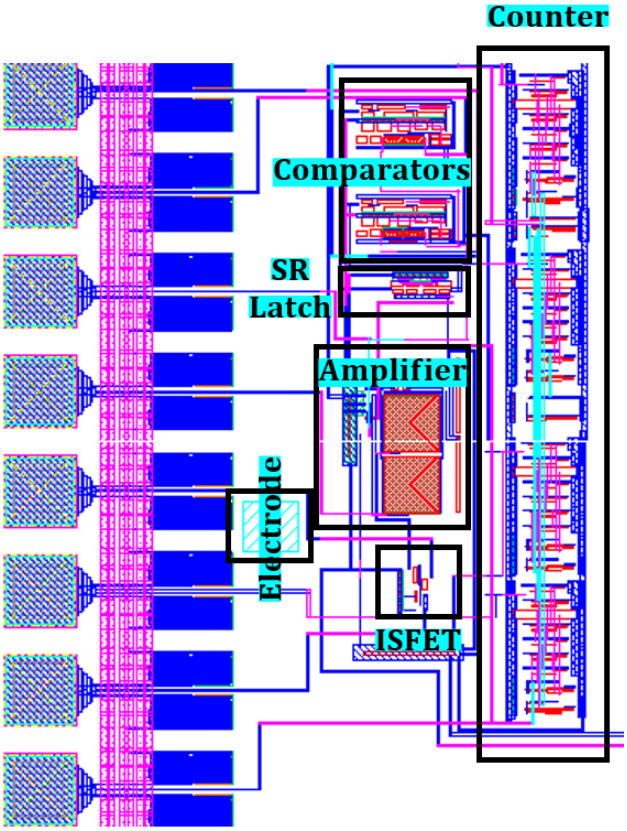

Figure 4: The ISFET pH sensor's layout integrated with counter fabricated in 0.5 μm CMOS technology.

Table 3: Pin names and numbers (Matched with Fig. 4.15 in chapter 4, section 4.2.)

Numbers	Names	Numbers	Names
16	CLK	21	V_{FG} (ISFET)
17	Ref-High (comparator)	22	A/B/C/D (counter)
18	Ref-Low (comparator)	24	Q (SR-latch Output)
19	Capacitor (C_T)	30	GND
20	Resistor (R_T)	32	Vdd

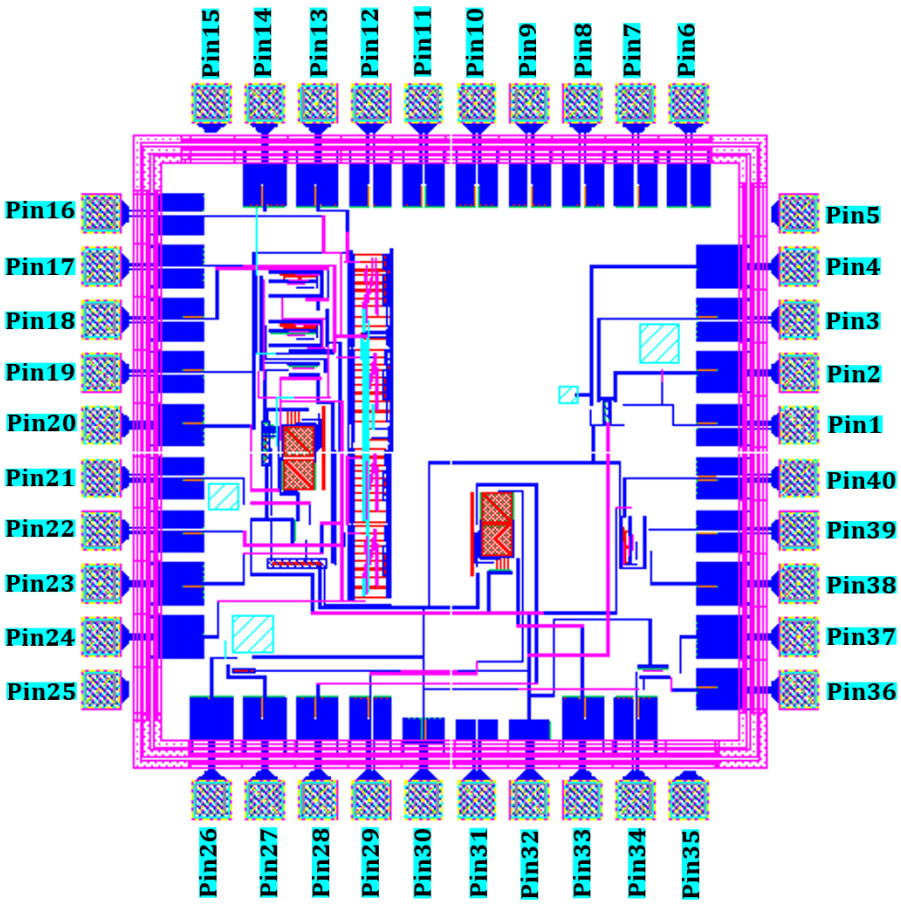

Figure 5: The whole pad frame layout consists of the ISFET pH sensor integrated with counter and sub-modules fabricated in 0.5 μm CMOS technology.

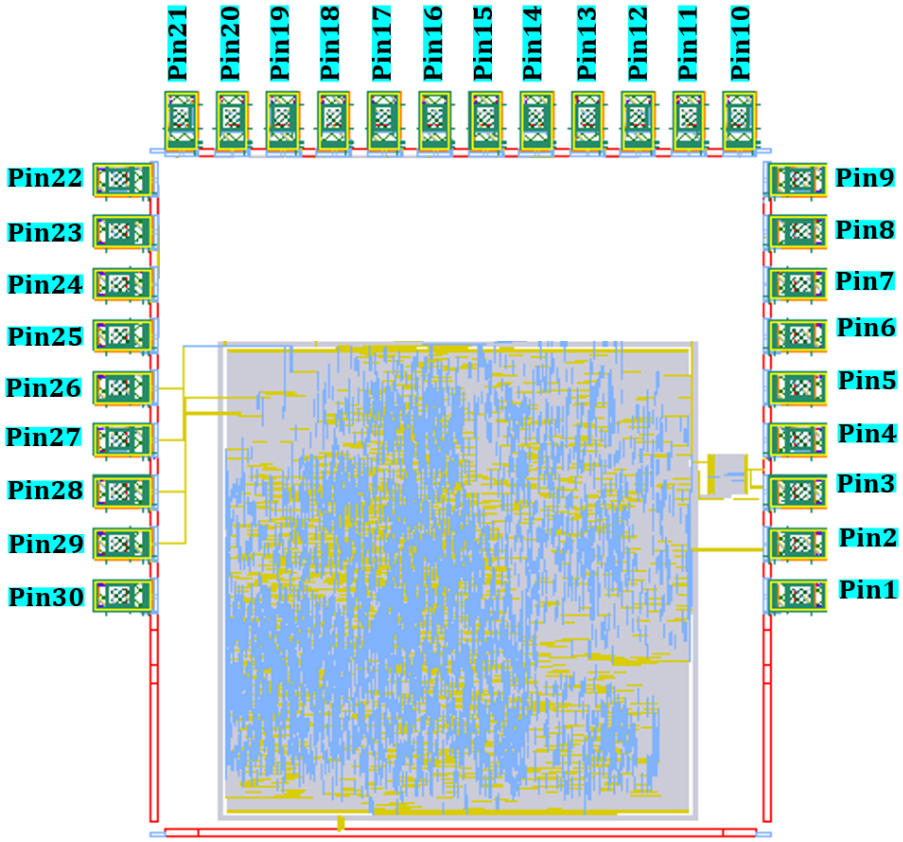

Figure 6: An ASIC pad frame's layout consists of ARM processor and an I2C module in 1-poly 3-metal 180 nm CMOS process.

Table 4: Pin names and numbers (Matched with Fig. 6.7 in chapter 6, section 6.2.1.)

Numbers	Names
2	XTAL1
26	XTAL2
27	NRST
28	SWIDO
29	SWCLK

B PCB Designs (Schematics and Layouts)

Based on the previous works, a readout PCB board was designed to readout pH from an ISFET-based differential circuit. This chip measured pH as a function of voltage in a differential structure mode, so the system's goal was to convert the output voltage to the associated pH value. The PCB board took that output voltage, performed signal processing, and digitized the result. A microcontroller could then convert that measured voltage to the associated pH value and display it on an LCD. With all of the pin-outs checked and the proper connections known, the system was connected and built at a schematic level in the Altium Design software. This schematic is shown in Fig. 7. The footprints are shown as a layout of this board in Fig. 8.

Another PCB board was designed for the pH to frequency sensor. The schematic level and final layout of the PCB are shown in Fig. 9, and Fig. 10, respectively.

The third PCB board was designed for the integrated pH-impedance sensing system. The schematic level and final layout of the PCB are shown in Fig. 11, and Fig. 12, respectively.

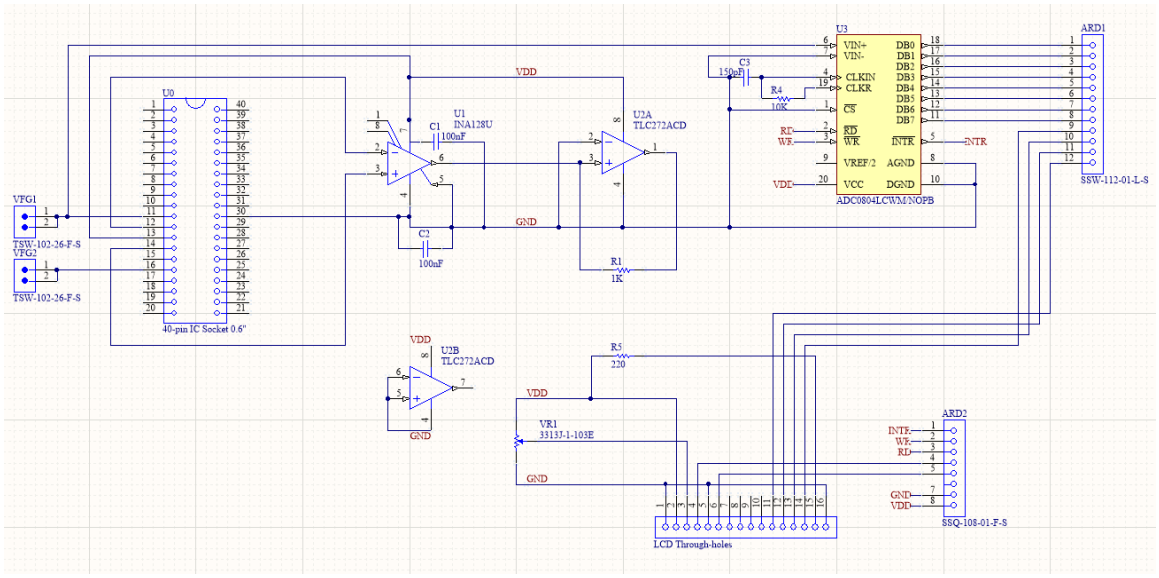

Figure 7: Schematic of the PCB board designed for the portable differential voltage-clamped ISFET pH sensor.

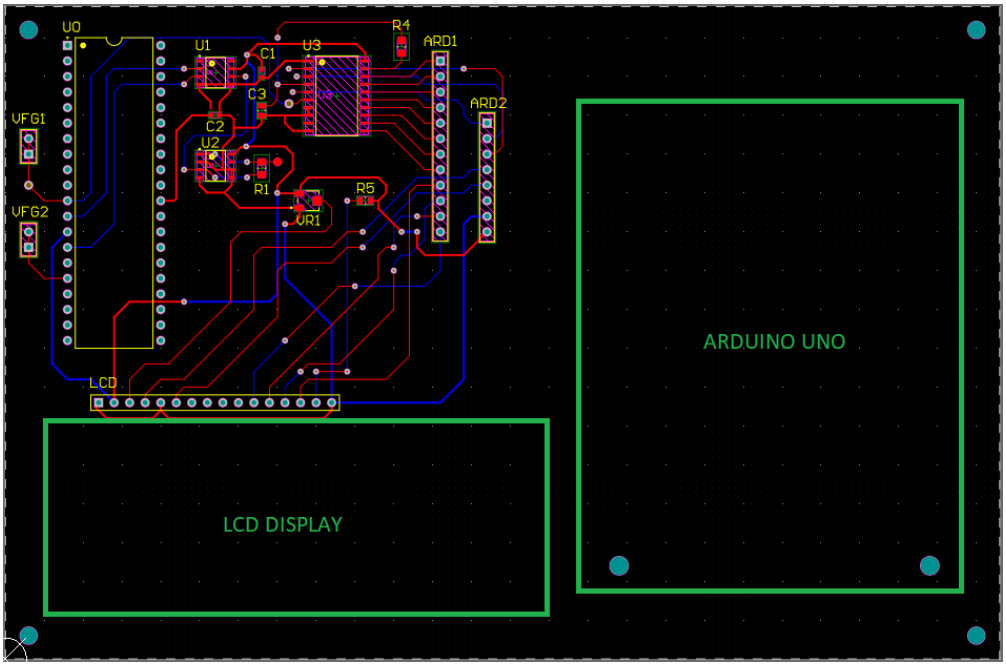

Figure 8: The layout of the PCB board designed for the portable differential voltage-clamped ISFET pH sensor.

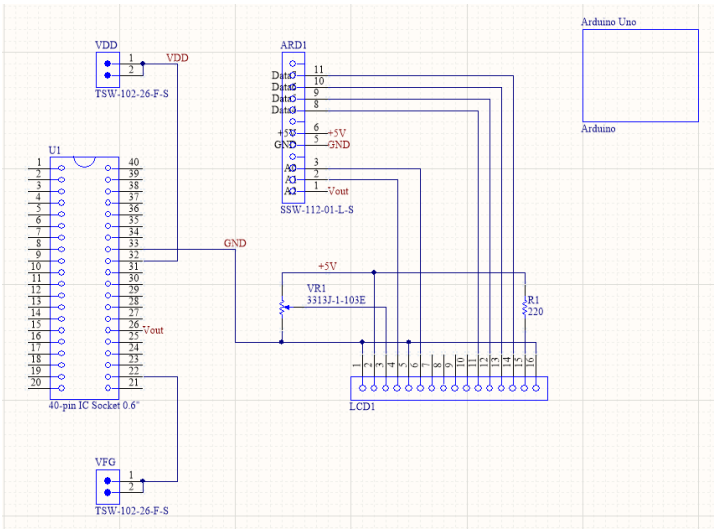

Figure 9: Schematic of the PCB board designed for the portable pH to frequency ISFET pH sensor.

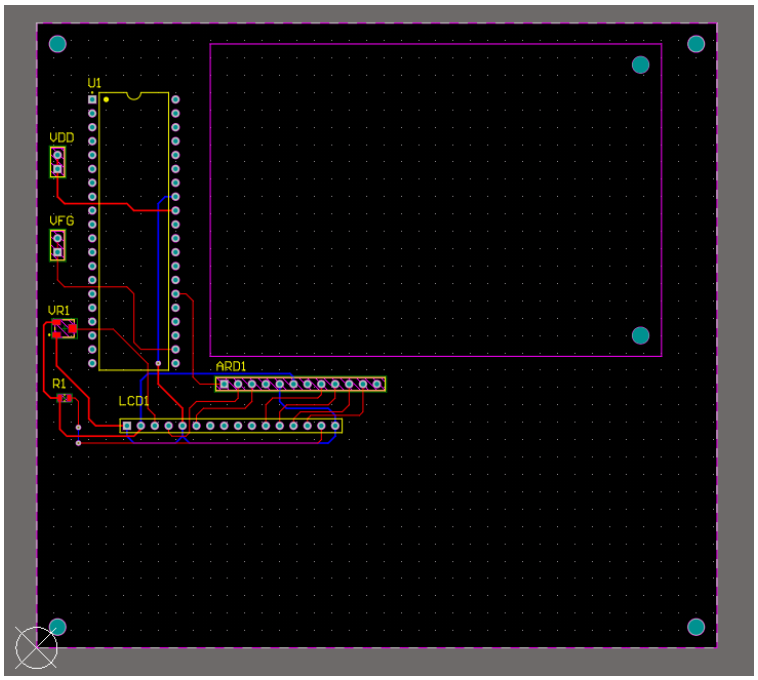

Figure 10: The layout of the PCB board designed for the portable pH to frequency ISFET pH sensor.

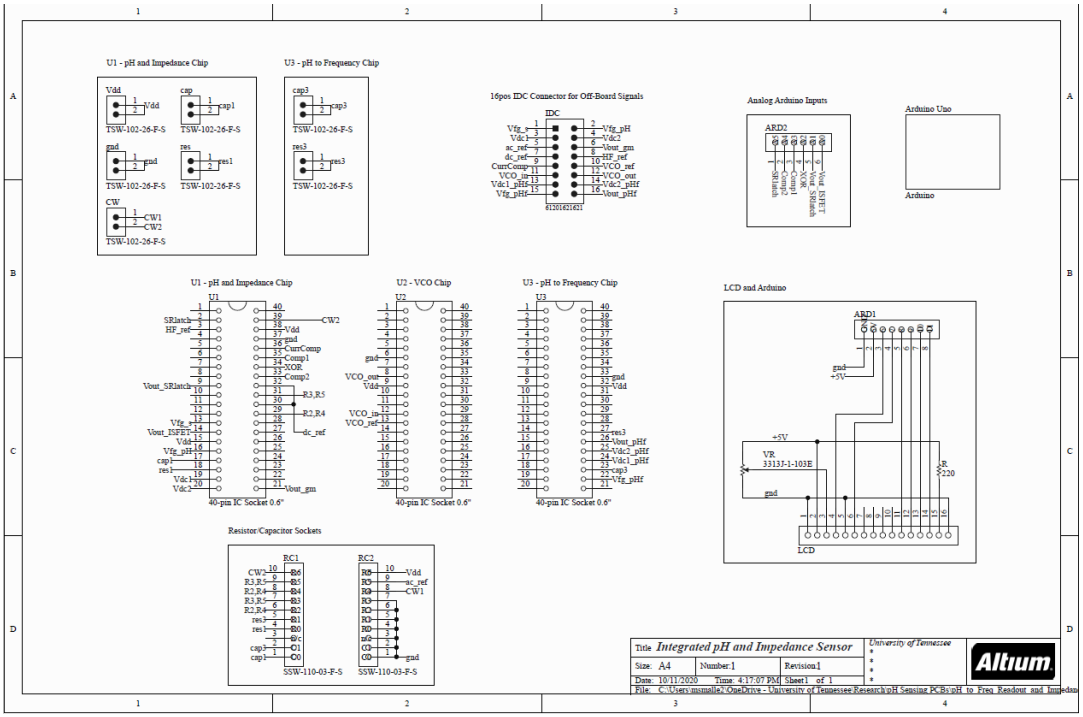

Figure 11: Schematic of the PCB board designed for the portable integrated pH-impedance sensing system.

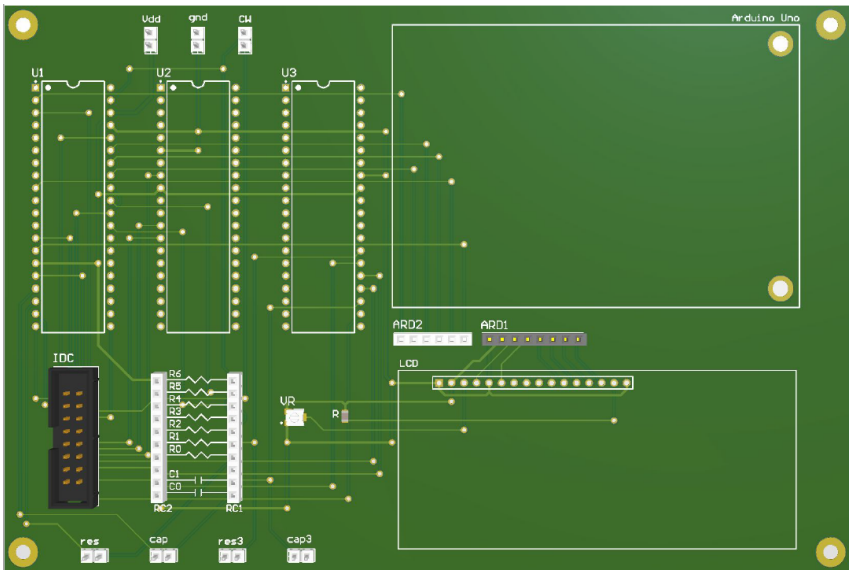

Figure 12: The layout of the PCB board designed for the portable integrated pH-impedance sensing system.

C Calibration Code

Portions of this code adapted from [91], The code which we used for the calibration is as follows,

```
#include <LiquidCrystal.h>
#include <math.h>
const int rs = A1, en = A0, d4 = 11, d5 = 10, d6 = 9, d7 = 8;
LiquidCrystal lcd(rs,en,d4,d5,d6,d7);
// register select pin, enable pin, D4 pin, D5 pin, D6 pin, D7 pin
int pinsIn[] = {0,1,2,3,4,5,6,7};   // array to receive 8 bit digital
input from LSB to MSB
void setup() {
lcd.begin(16,2);
// set up the LCD's number of columns and rows
//lcd.print("Voltage:");
//lcd.setCursor(0,1);
lcd.print("pH:");
//lcd.setCursor(7,1);
//lcd.print("f:");
for(int i = 0; i < 8; i++)     // set ADC input pins 0-7 as inputs
{
  pinMode(pinsIn[i], INPUT);
}
pinMode(A2, OUTPUT);
// pin A2 ouputs to RD pin of ADC
to send conversion to output of ADC
digitalWrite(A2, HIGH);
// pulse high to low to activate RD
```

```
pinMode(A3, OUTPUT);
// pin A3 ouputs to WR pin of ADC to start conversion
digitalWrite(A3, LOW);     // pulse low to high to activate WR
pinMode(A4, INPUT);
// pin A4 reads INTR pin status of ADC to determine when conversion
is complete
}
void loop() {
digitalWrite(A3, HIGH);              // send high pulse to WR pin of ADC
while(digitalRead(A4) != LOW){
// while conversion is happening do nothing
  //do nothing
}
if(digitalRead(A4) == LOW){
// when INTR to A4 goes low send low pulse to RD pin of ADC
to read conversion
digitalWrite(A2, LOW);
  int adc = parallelToByte();
  // read digital value from ADC conversion
  float voltage = adc*4.94/255.0;
  // calculate voltage for 8-bit digital value with 5V reference
  (calibrated to measured reference value)
  float rounder = round((0.63-voltage)/0.05+1);
  int pH = rounder;

  lcd.setCursor(0,1);
  if (pH < 10) {
    lcd.print("    ");
    lcd.setCursor(1,1);
    lcd.print(pH);
```

```
    }
  else {
    lcd.print(pH);
    }

  digitalWrite(A2, HIGH);    // return pin RD of ADC to HIGH value
  digitalWrite(A3, LOW);     // return pin WR of ADC to LOW value
  delay(100);                // delay 0.1 sec
  }
}

/*
* parallelToByte() - converts a binary value on 8 digital inputs to
an integer.
*/
int parallelToByte() {
  int ret = 0;  // Initialize the variable to return
  int bitValue[] = {1,2,4,8,16,32,64,128};
  // bit position decimal equivalents
  for(int i = 0; i < 8; i++)  // cycle through all the pins {
    if(digitalRead(pinsIn[i]) == HIGH)
    // because all the bits are pre-loaded with zeros, only need to do
    something when we need to flip a bit high
    {
      ret = ret + bitValue[i];
      // adding the bit position decimal equivalent flips that
      bit position
    }}
  return ret;}
```

Vita

Shaghayegh Aslanzadeh received her B.Sc. degree in Electrical Engineering from Shahid Rajaee Teacher Training University, Tehran, Iran, in 2013 and her M.Sc. degree in Electrical Engineering from Shahid Rajaee Teacher Training University, Tehran, Iran, in 2015. She is currently pursuing her Ph.D. degree in Electrical Engineering in the Department of Electrical Engineering and Computer Science at the University of Tennessee, Knoxville. Her research interests include analog and mixed-signal integrated circuit designs, VLSI designs, low-power, and low-noise lab-on-chip designs, bio-implantable and biomedical devices, microelectronics, and semiconductor devices.