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I am submitting herewith a thesis written by Jason Michael Vann entitled "Design of Low-Level Current Sources for Addressable Electron Emitter Array." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

James M. Rochelle, Major Professor

We have read this thesis
and recommend its acceptance:

Accepted for the Council:

Associate Vice Chancellor and
Dean of The Graduate School

# Design of Low-Level Current Sources for Addressable Electron Emitter Array

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Jason Michael Vann
August, 1998

## Dedication

I would like to dedicate this thesis

to my wife,

*Julie*

for her enduring love and support, for which
I am eternally grateful,

and

to my parents,

*Mr. Stanley Vann*

and

*Mrs. Sandra Vann*

whose love I have never doubted and
whose sacrifices have provided me with
unlimited educational opportunities.

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# Abstract

The development of a Massively Parallel Electron Beam Lithography system has led to the design of addressable 100pA current sources. BSIM Level 13 model parameters were extracted for the HP 0.5μm CMOS process, for characterization of weakly inverted, small geometry devices implemented in the current source design. A 5 x 5 array of 100pA current sources was also constructed for a feasibility and lifetime study of Amorphous Diamond electron emitters. The current sources were fabricated in the ORBIT 1.2μm CMOS process and attained a measured output impedance of 80GΩ.

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# Abbreviations

| | |
|---|---|
| AD | Amorphous Diamond |
| BSIM | Berkeley Short Channel Insulated Gate Field Effect Transistor |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DIBL | Drain-Induced Barrier Lowering |
| EB | Electron Beam |
| EKV | Enz-Krummenacher-Vittoz |
| HP | Hewlett-Packard |
| IC | Integrated Circuit |
| I-V | Current-Voltage |
| MOSFET | Metal-Oxide Semiconductor Field Effect Transistor |
| MPEBL | Massively Parallel Electron Beam Lithography |
| NA | Numerical Aperture |
| ORNL | Oak Ridge National Laboratory |
| Si | Silicon |
| UT | University of Tennessee |
| UV | Ultra-Violet |

# Chapter 1

# Lithographic Systems

## 1.1 Introduction to Lithographic Systems

Lithography is the process in which a pattern is transferred to a resist covered wafer. After the resist is cured by exposure to a particular radiation, a positive or negative etch sequence is implemented. The windows created by etching allow the subsequent ion-implantation and diffusions necessary to create semiconductor devices. The increasing density of integrated circuits (ICs), as predicted by Moore's Law [1], will soon become limited by current optical lithographic techniques. While optical lithography has been the workhorse of the IC industry since its inception, feature size limitations of optical lithography have led to the need for other technologies. Competing lithographic techniques, such as Deep Ultra-Violet (UV), X-ray, and Electron Beam (EB), allow the small feature sizes required to maintain the pace of Moore's Law. However, these techniques present tremendous technological difficulties.

## 1.2 Optical, Deep UV, and X-ray Lithographic Techniques

### 1.2.1 Optical Lithography

Optical lithography utilizes UV (200nm - 400nm wavelengths) light to transfer a pattern onto a photoresist covered wafer. Three types of exposure methods are used with optical lithographic techniques: (1)contact printing; (2) proximity (shadow) printing; and (3) projection printing. The contact printing method requires the mask to be brought into direct contact with the wafer, thus requiring a 1:1 mask to image ratio. Proximity printing, on the other hand, places a small gap, 10μm to 50μm, between the photomask and the wafer, again requiring a 1:1 mask to image ratio. Although contact printing provides higher resolution than shadow printing, particles of dust may become imbedded in the mask, due to the mask to wafer contact, resulting in defects in following wafer exposures. Therefore, the contact printing method can be very costly. Since shadow printing requires the mask to be placed very close to the wafer to minimize diffraction effects, wafer surface defects or dust particles lodged between the mask and wafer can result in severe mask damage [2,3].

To overcome the possibility of mask damage with either the shadow printing or contact printing method, a projection printing technique is used in optical

lithography. The mask image, typically 5 to 10 times larger than the wafer image, is focused by a lens onto the wafer. The projection system has several advantages over a 1:1 imaging system. The increased photomask size reduces the complexity of mask generation, minimizes the number of defects in the mask, reduces effects of dust particles on the mask, and results in easier alignment of the different mask layers [4].

Figure 1.1 shows a simplified optical lithographic imaging system. The resolution, or minimum feature size, of the imaging system is given by

$$l_m \cong \frac{\lambda}{NA}, \qquad (1.1)$$

where NA is the numerical aperture of the lens and $\lambda$ is the wavelength of the UV light. NA can then be defined by

$$NA = \bar{n}\sin\theta, \qquad (1.2)$$

where $\bar{n}$ is index of refraction in the image medium and $\theta$ is the angle of incidence on the image plane. Equations (1.1) and (1.2) show that the minimum feature size can be decreased by either reducing the wavelength of the UV light or increasing the NA. The depth of focus, $\Delta z$, however, is given by

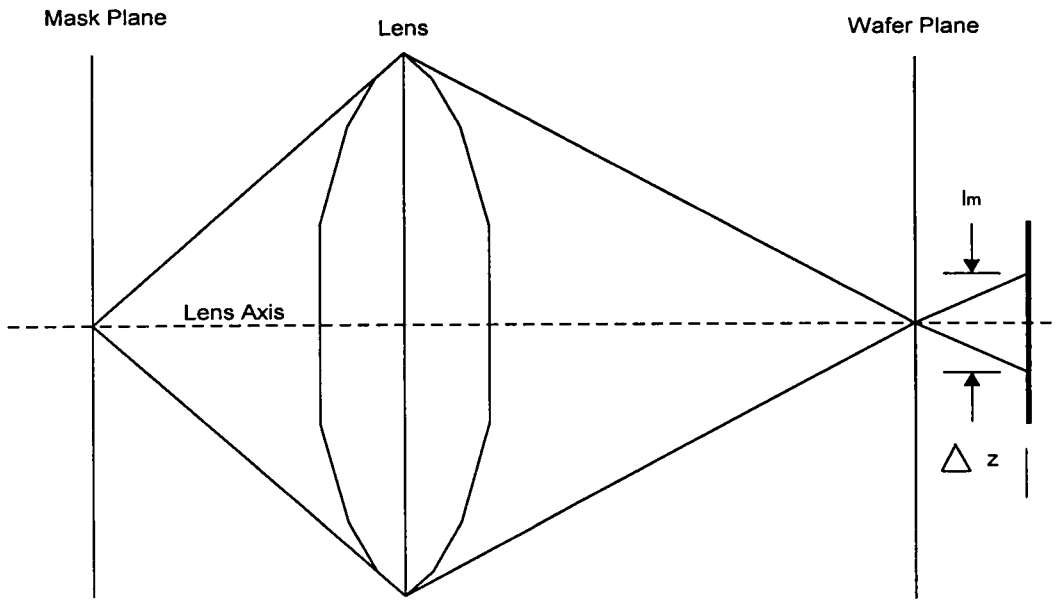



**Figure 1.1** Simplified Optical Lithography imaging system [5].

$$\Delta z \approx \frac{\bar{n}\lambda}{2*NA^2}. \qquad (1.3)$$

Since the depth of focus is more dependent upon NA than $\lambda$, $\Delta z$ will decrease more with increasing NA than with decreasing $\lambda$. This dependence on NA shows that minimization of feature size is primarily accomplished by decreasing the wavelength of the UV light, which results in light diffraction and other wavelength limitations [6].

Optical lithography has been the leading technology for many years, however, the push for deep sub-micron feature sizes cannot continue to be supported through optical techniques. Decreasing feature sizes are limited by diffraction effects and the ability of the lens to focus the shorter wavelengths onto the wafer. Current estimates predict that optical lithography is not viable for feature sizes smaller than 100nm.

### 1.2.2 Deep UV Lithography

Overcoming the diffraction limitations of optical lithography requires the implementation of shorter wavelengths, such as Deep UV (<200nm). Deep UV is much like optical lithography but uses shorter wavelengths and does not utilize projection printing techniques, resulting in a

1:1 mask to wafer image ratio. This results in more complex mask generation, increases in the number of wafer defects, and also increased difficulty in mask alignment. While Deep UV is still limited by diffraction effects, the capability to achieve smaller line widths has made Deep UV an appropriate transitional technology from optical lithography.

### 1.2.3 X-ray Lithography

Another technology that has been used to achieve smaller device sizes, while maintaining a relatively high IC throughput, is X-ray lithography. X-rays have wavelengths on the order of 0.4nm to 50nm, eliminating the diffraction effects observed in UV lithography processes. X-ray lithography uses a shadow printing method with a 1:1 mask ratio, however, X-ray sources have a finite size whereas UV light can be generated to cover an entire wafer. The limited size of the source and the finite gap between the mask and wafer lead to the penumbral blur effect and a lateral magnification error [7].

The penumbral blur effect results in a loss of resolution and a blurring of edges on the wafer. The lateral magnification error gives a laterally shifted image on the wafer where amount of shift is proportional to the radial position of the image on the wafer. The lateral magnification error can be minimized with compensation

techniques in the mask generation process. Although X-ray lithography can achieve sub-micron feature sizes, complex mask fabrication and penumbral blur will continue to be a limiting factor. In addition, the cost of X-ray sources may be prohibitive.

## 1.3 Electron Beam Lithography

### 1.3.1 Single Electron Beam Lithography

Single Electron Beam (EB) lithography can achieve higher resolution than the previously mentioned technologies. EB lithography uses an electron beam to write the image directly to the resist by using beam deflection techniques. Although EB lithography is currently not widely used in IC fabrication, it is a rather mature technology and has been primarily implemented to define masks utilized by other lithography techniques.

Although EB lithography has the distinct advantage of producing very high resolutions while eliminating masks and the resulting mask alignment errors, the throughput is very low compared to other techniques. A given EB system can pattern a 4" wafer with 0.5μm feature sizes in about an hour, whereas, an optical lithographic system could pattern approximately 70 to 90 similar wafers per hour [8]. Because of the sequential nature of the EB pattern write process, the wafer throughput is proportional to $1/l_m^2$, where $l_m$ is

the minimum feature size [9]. Other than low wafer throughput, EB lithography also suffers from short electron emitter lifetimes. Short emitter lifetimes result in increased cost per wafer and a further decrease in throughput due to emitter replacement time.

### 1.3.2 Multiple Electron Beam Lithography

Advancement of throughput for EB lithographic systems has led to the development of multiple electron beam lithography. The addition of multiple electron emitters has improved the throughput of EB systems but still trails the throughput of the other lithographic techniques. Multiple EB lithography may consist of up to 200 parallel emitters. Further throughput improvement in Multiple EB lithography is limited by the size of individual electron emitters.

### 1.3.3 Massively Parallel Electron Beam Lithography

The need has arisen for Massively Parallel EB lithography (MPEBL) to maintain the high throughput necessary of a commercially viable lithographic system while obtaining the sub-micron feature sizes necessary for increasing chip density. A MPEBL system would consist of millions of electron emitters simultaneously writing patterns to a wafer. Figure 1.2 gives a simplified diagram of a MPEBL system with major sub-systems. With large arrays

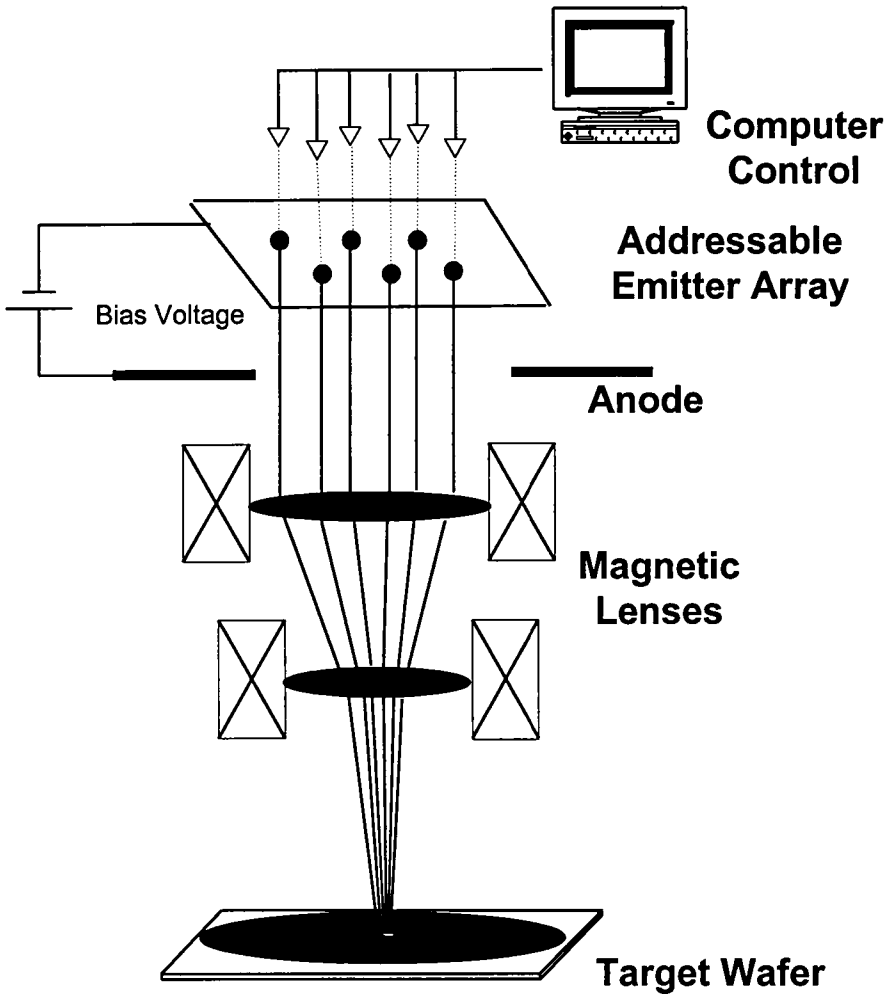



**Figure 1.2** MPEBL system diagram, consisting of computer controlled emitter array, magnetic focusing lens, and target wafer.

of emitters an entire chip with sub-micron line widths could potentially be written in less than a second.

The implementation of massively parallel emitters requires the development of an addressable electron emitter array. The electron emitter array would be addressable through a large shift register, where the output of each register would activate its respective emitter and regulate its respective emission characteristics, as shown in Figure 1.3.

Regulation of the separate emitters is critical for maintaining a uniform pattern transfer to the wafer. Differing emission characteristics from the electron emitters would result in nonuniform etch rates of the electron resist. Mismatched etch rates may result in wafer defects and poor circuit performance.

Advancement of current lithographic will require an improvement in EB lithography, particularly in increased IC chip density. For MPEBL to become an economically viable lithographic process improved emitter lifetime and increased wafer throughput is essential.

## 1.4 Scope of Thesis

This work will describe a proposed MPEBL system and its various subsystems. A prototype 5 X 5 array of electron emitters was constructed for a feasibility and emitter lifetime study for this MPEBL system. The addressable

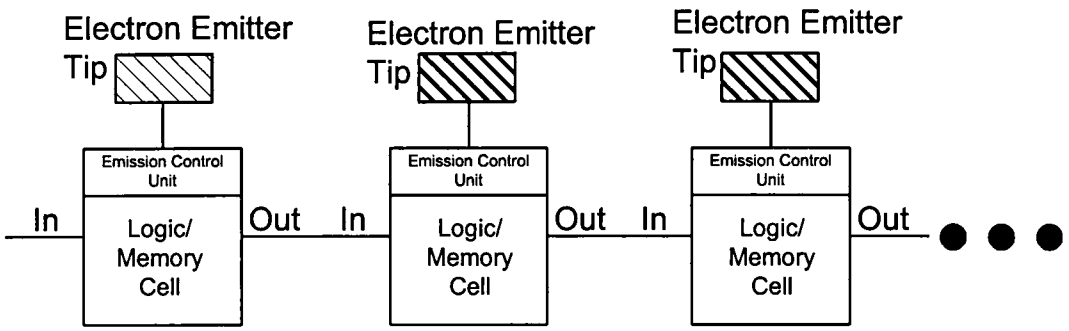



**Figure 1.3** Addressable electron emitter array comprised of large shift register with emission control, memory cells, and electron emitters.

emitter control systems were designed, modeled, and tested for implementation in the system.

The principal focus of this thesis is the design, simulation, fabrication, and testing of the electron emitter control circuitry. The design of the individual control cells primarily focused on emission regulation, emitter addressability, and adjustability of the test system. The 5 X 5 array of addressable control circuits was fabricated using the ORBIT 1.2μm CMOS process. Also, models were developed for the Hewlett-Packard (HP) 0.5μm CMOS process from measured devices. The 0.5μm models were developed for characterization of future current control circuit designs fabricated in the 0.5μm process.

Chapter 2 will be an explanation of electron emitters and different types of electron emission. Thermonic emission, photo emission, and field emission will be presented along with a discussion of Spindt tip and Amorphous Diamond (AD) emitters. Chapter 2 will end with a brief introduction to the current regulation systems of a MPEBL system.

Since the emitter control circuits operate at very low current, Chapter 3 will follow with a discussion of the subthreshold operation of MOSFETs. This chapter will explain the operation of MOSFETs in deep weak inversion and short channel effects. Since future implementations of the

emitter control circuits will use even smaller devices, device models will be determined for simulation of emitter control circuits fabricated in a 0.5μm CMOS process.

Chapter 4 will address the design and simulation of the emitter control circuits, followed by a discussion of the testing and evaluation of the control circuits in Chapter 5. Chapter 5 will conclude with a comparison of the calculated, simulated, and measured results taken from the emitter current regulation circuits. This work will be concluded in Chapter 6 with final comments on the presented topic.

# Chapter 2

# Electron Emitters

## 2.1 Types of Electron Emission

### 2.1.1 Thermonic Emission

Thermonic emission occurs when some electrons obtain enough thermal energy to escape the material's surface. The minimum kinetic energy necessary for an electron to escape the material's surface is the work function, $\phi$. The maximum current density, J, of a thermonic electron beam leaving a material is described by the Richardson-Dushman equation,

$$J = B_0 * T^2 * e^{(-\phi/kT)} \ A/m^2 \ , \qquad (2.1)$$

where $B_0$ is $4\pi q m_e k^2/h^3$, $q$ is the charge of an electron, $m_e$ is the effective mass of an electron, k is Boltzman's constant, and h is Plank's constant. Because of the high temperatures involved in the thermonic emission of electrons, the lifetime of these emitters is typically short.

### 2.1.2 Photo Emission

Electron emission can also be stimulated by optical illumination. Emission of an electron requires that the work function of the material be less than the energy of the incident light. Low work function materials are needed to obtain emission from the normal wavelengths available from inexpensive optical sources. To achieve a reasonable electron current density intense light sources (e.g. lasers) are required [10].

### 2.1.3 Field Emission

Field emission is accomplished by placing an adequately high electric field normal to the surface of a material to overcome its work function. For small electric fields, a material's work function is effectively decreased, thus allowing the Richard-Dushman equation to determine the current density leaving the material. However, large fields result in a tunneling process called field emission. Since the tunneling phenomena is essentially temperature independent, low temperature electron emission can be achieved through field emission techniques [11]. The Fowler-Nordheim equation describes the current of field emitters by

$$I = \frac{aq^3 \alpha E^2}{8\pi h\phi} e^{-\frac{8\pi\phi\sqrt{2m_e\phi}}{3heq\beta E}} \text{ A}, \qquad (2.2)$$

where E (V/m) is the applied electric field, $\phi$ is the work function of the material, a is the emission area, and $m_e$ is the mass of an electron [12]. The $\alpha$ and $\beta$ terms are related to the geometry of the emitter and model the field enhancement of the emitter configuration. The current density of a field emitter can therefore be increased dramatically by the geometric shape of the material.

## 2.2 Spindt Tip Electron Emitters

Spindt tips use localized field enhancement to obtain low-field and low-temperature electron emission. Spindt tip emitters are sharply pointed cathodes with a Molybdenum, Tungsten, or Silicon coated tip [13]. A typical Spindt emitter setup is shown in the Figure 2.1. When a bias voltage is placed between the cathode and anode, electrons will emit from the Spindt tip through the anode opening. The electron beam would then be accelerated and guided by a beam deflection and focusing system.

Although the sharp points allow low-field emission, they are difficult to fabricate, have a small emitter area, and have a short lifespan. Because of the small tip area large current densities can exist in the tip for small

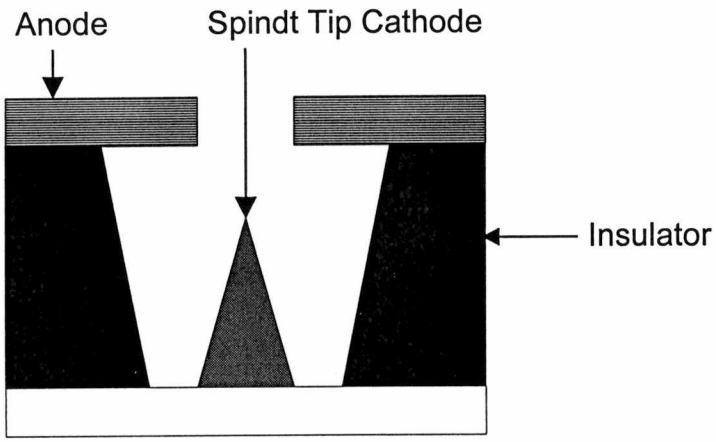



**Figure 2.1** Spindt tip field emitter configuration.

emission levels. A large current density causes damage to the tip through erosion and self-heating resulting in a shortened emitter lifetime [14].

## 2.3 Amorphous Diamond Electron Emitters

Current research has led to the development of Amorphous Diamond (AD) electron emitters. Amorphous Diamond has a "negative electron affinity" from the <111> face, thus allowing very low field emission [15]. The electron affinity of a material is the amount of energy required to move an electron from the bottom of the conduction band to the vacuum level (i.e. out of the material). Amorphous Diamond also has high thermal conductivity, extreme hardness, and good chemical stability which makes it an attractive material for the current application. However, the actual emission mechanism is not well understood, yet [16].

The much lower electric field required by an AD emitter in contrast to the Spindt tip emitters, allows the use of flat emitting surfaces. The flat emitting surface extends the life of the emitter by decreasing the current density required for a given current level. Potential ease in fabrication is another significant advantage AD holds over Spindt tip emitters. The long emitter lifetime and ease of fabrication have led to research in implementing AD emitters in the realization of a MPEBL system.

## 2.4 Amorphous Diamond Emission Control

In any practical MPEBL system each AD emitter requires a control circuit to maintain precise emission and write properties, as mentioned in Chapter 1. Nonuniform emission properties can result in poorly defined features and non-functional circuits. The exponential nature of field emitters (equation 2.2) can lead to significant differences in emission levels because of process variations and electric field differences between emitters. Therefore we propose to use current sources, instead of voltage sources, to control the AD electron emitters. A current source would limit emission variations between emitters to current level matching of the current sources and the finite output impedance of the current sources.

Due to the massive number of electron beams utilized with MPEBL, the current levels of each emitter must be kept extremely low to minimize space charge effects [17]. In this proposed system each emitter will operate at a current level of 100pA. These low current levels require an extremely high current source output impedance to maintain good emission regulation. For example, if the pixel-to-pixel variation in operational voltage is 1V, an output impedance of 1000GΩ is required to regulate a 100pA current source to 1%.

# Chapter 3

# Subthreshold Modeling of MOSFETs

## 3.1 Subthreshold Operation

The extremely low electron beam current of 100pA per source dictates that the current control devices operate in deep weak inversion. The use of minimum geometry devices within the control cell electronics is also required to achieve the massive array of control cells in a chip of reasonable size. Therefore, a thorough understanding of MOSFET small geometry effects and weak inversion operation is central to this work.

### 3.1.1 Subthreshold Drain Current Equations

Unlike the strong inversion case, the weak inversion drain current of a MOSFET is not dominated by drift current but rather by a diffusion current. The MOSFET in weak inversion operates much like a bipolar transistor. A voltage placed on the gate of the MOSFET lowers the barrier potential between the source and the bulk, creating an excess of minority carriers in the channel at the source

junction. Conversely, the excess minority carrier concentration at the drain junction is essentially zero, resulting in a diffusion current, $I_D$, from the source to drain. In examining the concentration gradient across the channel of a MOSFET it can be shown that [18]

$$I_D = k'e^{\left(\frac{V_{GS}-V_T}{nV_t}\right)}\left(1-e^{\frac{-V_{DS}}{V_t}}\right), \qquad (3.1)$$

where $V_T$ = threshold voltage,

$V_t$ = kT/q = thermal voltage,

k' = exponential prefactor,

n = exponential slope factor.

Figures 3.1 and 3.2 show the terminology and conventions used in equation (3.1). The exponential slope factor, n, is defined by [21]

$$n \equiv 1 + \frac{C_{depl}}{C_{OX}} \qquad (3.2)$$

where $C_{depl}$ is the depletion layer capacitance and $C_{OX}$ is the gate oxide capacitance. Lastly, the $\left(1-e^{\frac{-V_{DS}}{V_t}}\right)$ term is applicable only in the linear region and can therefore be neglected for a MOSFET operating in saturation.

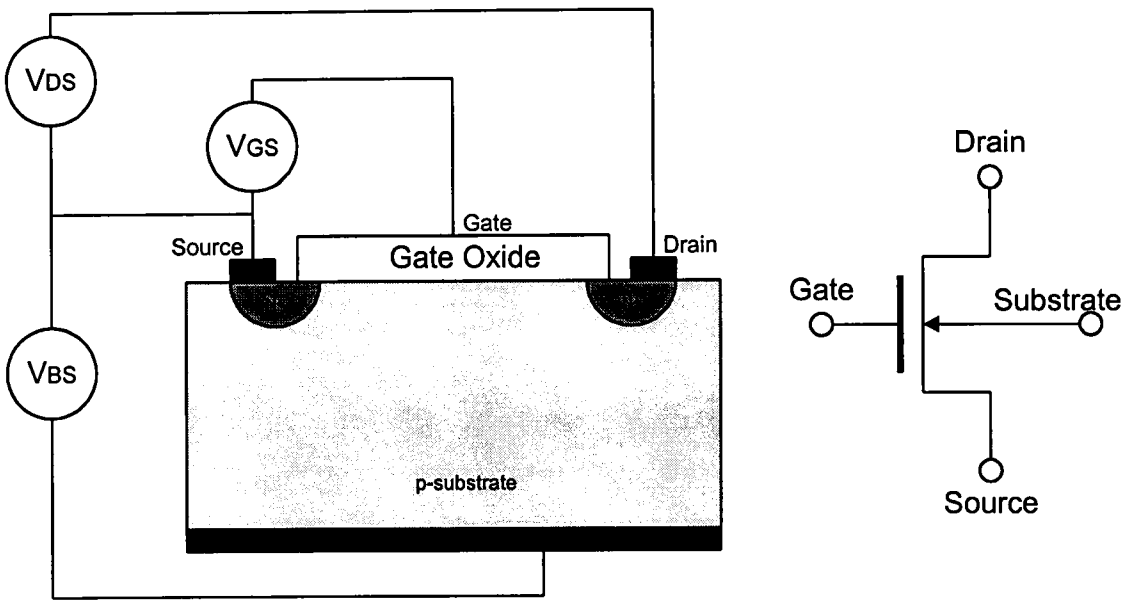



**Figure 3.1** N-channel MOSFET cross-section, accompanied with MOSFET terminal connections [19].

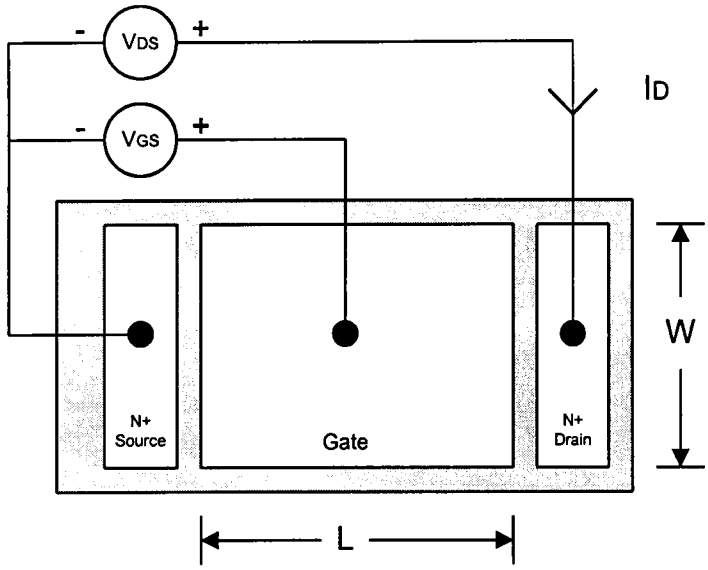



**Figure 3.2** Top view of n-channel MOSFET with drawn gate length and width [20].

### 3.1.2 Short Channel Effects

The gate length, L, and gate width, W, from Figure 3.2 are the drawn gate dimensions for a MOSFET. However, the effective channel length of a MOSFET is given by [22]

$$L_{eff} = L_{drawn} - L_d - L_s - X_d - X_s, \qquad (3.3)$$

where $L_d$ = lateral diffusion length for the drain,

$L_s$ = lateral diffusion length for the source,

$X_d$ = drain depletion layer width,

$X_s$ = source depletion layer width.

The effective channel length can be considerably decreased when the depletion layer widths and lateral diffusion lengths become comparable to the drawn gate length, giving rise to short channel effects.

Two short channel effects of particular interest are a lower threshold voltage due to decreased gate length and a lower threshold voltage due to drain bias. In a short channel device a larger percentage of charge in the channel region has electric field lines terminated by the source and drain depletion region charge. Therefore, a smaller charge on the gate is required to invert the channel, hence the lower threshold voltage [23].

For long channel devices the channel region is assumed to be uniform with little interaction between the drain and

gate field lines. However, for short channel devices the drain bias interacts with the gate bias by effectively lowering the barrier potential between the source and bulk regions. This phenomena is known as the Drain Induced Barrier Lowering (DIBL) effect [24]. A lowering of the barrier potential effectively lowers the threshold voltage of the device. Considering only the effects of drain bias on the threshold voltage, the output impedance, $R_{out}$, of a weakly inverted device in saturation can be approximated by allowing

$$V_T = \alpha - \beta V_{DS}, \tag{3.4}$$

where $\alpha$ and $\beta$ are the parameters of a particular process. Then, equation 3.1 becomes

$$I_D = k' e^{\frac{V_{GS} - \alpha + \beta V_{DS}}{nV_t}}, \tag{3.5}$$

and

$$R_{out} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} \propto \frac{nV_t}{\beta} e^{\frac{\alpha - \beta V_{DS}}{nV_t}}. \tag{3.6}$$

Equation (3.6) shows that the DIBL contribution to the output impedance of a MOSFET in weak inversion is not constant and is exponentially related to the drain voltage.

## 3.2 MOSFET Subthreshold Modeling

Simulation of the electron emitter current control circuitry requires that model parameters be determined for the subthreshold operation of minimum geometry MOSFETs. Due to the extremely high output impedance required of the current sources, the model must account for short channel effects, primarily DIBL. Adjustment of model parameters for differing device geometries is also necessary for characterization of a control circuit containing devices of various sizes. In this work, the commercial simulator HSPICE is utilized for simulation of the current control circuitry.

### 3.2.1 Level 1 and 2 Models

The Level 1 model is primarily concerned with characterization of large geometry, thick gate oxide devices. The Level 1 model uses the basic "square-law" device equations for the strong inversion region while defining subthreshold current as zero. This model does not

account for small geometry effects that are critical in this work.

The Level 2 model attempts to address inadequacies in the Level 1 model but results in a mathematically complex scheme. Although the Level 2 model does address some short channel effects and allows subthreshold conduction, parameter extraction and adjustment is difficult due to a limited parameter set. Since the calculations for the Level 2 model are greatly involved, the model also presents problems with convergence and computation time [25].

### 3.2.2 Level 3 Model

The Level 3 model addresses the problems of the Level 2 model with a somewhat more empirical approach. The Level 3 model does allow subthreshold conduction and certain small geometry effects, such as DIBL. The Level 3 model is also very simple and is therefore much more computationally efficient than the Level 2 model.

Although the Level 3 model has less problems with convergence and provides more accurate calculations, the model was primarily created for device sizes greater than 1μm and was not intended to address sub-micron phenomena. Lastly, the subthreshold model has a small parameter set making parameter extraction very difficult.

## 3.3 BSIM Level 13 MOSFET Modeling

The BSIM model takes a more empirical approach to MOSFET characterization than the Level 1, 2, or 3 models. The BSIM model does not utilize complex mathematics to describe MOSFET operation but uses an extensive set of empirical parameters. The large parameter set implemented within the BSIM model results in a simplified equation set and allows for easier model extraction. The BSIM model also characterizes subthreshold conduction and many short channel effects. Because of the ease in parameter extraction and short channel modeling capabilities, the BSIM model has been selected for this application.

The EKV model, a new model candidate, has been shown to give extremely good modeling results of MOSFET subthreshold and small geometry operation. However, use of the EKV model has been discarded since it is not yet implemented in commercial SPICE simulators [26].

### 3.3.1 BSIM Subthreshold Current Modeling

The subthreshold drain current, $I_{sub}$, of a MOSFET is described in the BSIM Level 13 model by [27]

$$I_{sub} = \frac{I_{lim} * I_{exp}}{I_{lim} + I_{exp}} . \qquad (3.7)$$

$I_{lim}$ is a limiting current implemented to improve convergence and smooth the transition from the weak inversion to the strong inversion region, and is given by [28]

$$I_{lim} = 4.5\mu C_{ox}\frac{W_{eff}}{L_{eff}}V_t^2, \qquad (3.8)$$

where $C_{ox}$ is the gate oxide capacitance and $\mu$ is the channel mobility. For deep subthreshold operation, where $I_{sub} \approx I_{exp}$, $I_{exp}$ is defined by [29]

$$I_{exp} = \mu C_{ox}\frac{W_{eff}}{L_{eff}}V_t^2 e^{1.8} e^{\frac{V_{GS}-V_T}{x_n * V_t}}\left(1-e^{-\frac{V_{DS}}{V_t}}\right), \qquad (3.9)$$

where $x_n$ is the weak inversion gate drive coefficient and the $\left(1-e^{\frac{-V_{DS}}{V_t}}\right)$ term is negligible in the saturation region. The exponential slope is set by the $x_n$ term which is defined by [30]

$$x_n = N_{0eff} - N_{Beff} * V_{BS} + N_{Deff} * V_{DS}, \qquad (3.10)$$

where $N_{0eff}$ is the effective gate drive coefficient, $N_{Beff}$ is the effective substrate bias adjustment of gate drive

coefficient, and $N_{Deff}$ is the effective drain bias adjustment of gate drive coefficient.

### 3.3.2 BSIM Length and Width Dependency Modeling

To account for small geometry effects the BSIM model allows each parameter to have length and width dependencies. An effective parameter value is calculated from a base parameter value and its corresponding length and width dependencies by [31]

$$X_{eff} = X_0 + LX*(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}}) + WX*(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}}), \quad (3.11)$$

where $X_0$ is the base parameter value, LX is the parameter's length dependency, and WX is the parameter's width dependency. The $LREF_{eff}$ and $WREF_{eff}$ parameters are the channel length and width references, respectively. The channel reference terms are included to make the model more manageable when different models are extracted for different device sizes, referred to as binning [32]. Although a particular BSIM parameter set can support devices over a wider range of geometries than other models, binning may still be required for designs with widely varying device geometries.

### 3.3.3 BSIM Output Impedance Modeling

The DIBL short channel effect is modeled in BSIM with the Linear Drain Voltage Threshold Coefficient ($ETA_0$) parameter. The $ETA_0$ parameter is factored into the threshold voltage calculation by the following [33]:

$$V_T = V_{FBeff} + \phi + \gamma\sqrt{\phi + V_{SB}} - \text{xeta} * V_{DS}\,, \qquad (3.12)$$

where $V_{FBeff}$ is the effective flatband voltage, $\phi$ is 2 times the Fermi potential, $\gamma$ is the body effect parameter, and xeta is directly proportional to the $ETA_0$ parameter. The xeta term is related to the effective value of $ETA_0$ by

$$\text{xeta} = ETA_{0eff} - X2E_{eff} * V_{BS} + X3E_{eff} * (V_{DS} - VDDM)\,, \qquad (3.13)$$

where $X2E_{eff}$ is the substrate bias correction to $ETA_0$, the $X3E_{eff}$ is the high drain field correction to $ETA_0$, and VDDM is the critical voltage for high drain field mobility reduction. Once the DIBL effect has been accounted for, the output impedance of a device can be calculated by combining equations (3.6), (3.9), and (3.12). Assuming operation in the saturation region and that the threshold voltage dependence on drain voltage determines the output impedance, $R_{out}$ is found to be

$$R_{out} \cong \frac{L_{eff} * xn}{\mu C_{ox} W_{eff} V_t e^{1.8} * xeta} e^{\frac{-xeta * V_{DS}}{xn * V_t}} e^{\frac{V_{T0} - V_{GS}}{xn * V_t}} , \qquad (3.14)$$

where

$$V_{T0} = V_{FBeff} + \phi + \gamma\sqrt{\phi + V_{BS}} . \qquad (3.15)$$

Therefore, as $W \to \infty$, $\mu \to \infty$, xeta$\to\infty$, and $V_{DS} \to \infty$ the output impedance approaches zero and as $L \to \infty$, $R_{out}$ approaches infinity.

## 3.4 BSIM Model Parameter Extraction

Simulation of the electron emitter current control circuitry requires a BSIM model parameter set for the MOSFET devices. The current design was implemented in the ORBIT 1.2μm process, for which a complete BSIM Level 13 parameter set is available. However, development of BSIM parameters for the HP 0.5μm CMOS process was required for simulation of future current control electronic designs. Because a limited parameter set was available for the HP 0.5μm devices, only certain parameters were extracted for device characterization.

Because the current control circuitry was primarily for emission studies of AD and did not involve high frequency

measurements, only DC model parameters were required. Also, substrate voltage dependencies were not modeled for several reasons, including a reduction in modeling time, a reduced parameter set, and the limited output impedance dependence on substrate bias. Only the length dependence of the devices was determined because the output impedance is primarily limited by short channel effects. While narrow channel effects were not critical to the application presented in this work, narrow channel devices were also not available for testing.

### 3.4.1 Model Parameters

Modeling of the DC parameters requires that device simulations be fit to the measured drain current versus gate voltage, $I_D$ vs. $V_{GS}$, and drain current versus drain voltage, $I_D$ vs. $V_{DS}$, curves. Curve fitting to the exponential subthreshold current, from the $I_D$ vs. $V_{GS}$ curves, requires the determination of the exponential slope and the exponential coefficient. From equation (3.9) it can be seen that the $C_{OX}$, $\mu$, $V_T$, and $x_n$ values are available for adjusting the exponential slope and coefficient to fit measured data of a particular device geometry.

Because the $C_{OX}$ parameter is a device constant determined by the oxide thickness and does not have geometric dependencies, the $C_{OX}$ parameter would not be

sufficient for curve fitting. The $\mu$ value is an interpolation between several different terms and is difficult to directly relate to a particular parameter. The zero bias mobility, MUZ, parameter is the most directly related parameter to the channel mobility, however the MUZ parameter also has no length and width dependencies. Therefore, the $\mu$ would not be a sufficient term for curve fitting. Therefore the $I_D$ vs. $V_{GS}$ curves were modeled through the $V_T$ and xn terms. Since equation (3.8) can be written in the form

$$I_D \propto e^{\frac{-V_T}{xn*V_t}} * e^{\frac{V_{GS}}{xn*V_t}}, \qquad (3.16)$$

The xn term would adjust the exponential slope while the threshold voltage would model the exponential coefficient.

Because the body effect and high drain field effects are neglected and the output impedance is limited by the DIBL effect, equations (3.10), (3.12), and (3.13) can be simplified to

$$xn = N_{0eff}, \qquad (3.15)$$

$$V_T = V_{FBeff} + \phi + \gamma\sqrt{\phi} - xeta * V_{DS}, \qquad (3.16)$$

$$xeta \approx ETA_{0eff}, \qquad (3.17)$$

respectively. Therefore, the $N_0$ parameter would model the exponential slope of the subthreshold current and the $ETA_0$ parameter would model the output impedance. Because the Fermi potential is a device constant and is not directly proportional to the threshold voltage, the flat-band voltage, $V_{FB}$, would be used to model the threshold voltage.

The length dependencies of these parameters were determined to account for short channel effects. For long channel devices, with little length dependence, the $N_{0eff}$, $V_{FBeff}$, and $ETA_{0eff}$ parameters are approximately equal to their respective base parameters. The length dependency parameters for the three base parameters, $N_0$, $V_{FB}$, and $ETA_0$, are the $LN_0$, $LV_{FB}$, and the $LETA_0$ parameters, respectively. Table 3.1 shows the final parameter set required for device characterization and their default values provided for the HP 0.5μm process.

### 3.4.2 Device Measurement and Parameter Extraction

The method for determining the six model parameters involved several key elements. First, long channel devices were used to determine the base parameters, then short channel devices were used to obtain the length dependencies of each parameter. Secondly, the same W/L ratio for the short channel and long channel devices were used so that the only difference in current levels between devices would be adjustable by the length dependency parameter set. Lastly,

**Table 3.1** BSIM Level 13 parameters, with default values for HP 0.5μm CMOS process, required for modeling of subthreshold current, output impedance, and short channel effects.

| Parameter | N-channel device | P-channel device |
|---|---|---|
| N0 | 1.00 | 1.00 |
| LN0 | 0.00E+00 | 0.00E+00 |
| VFB | -6.68E-01 | -6.60E-02 |
| LVFB | -9.88E-03 | -1.78E-02 |
| ETA0 | 6.14E-05 | 7.91E-03 |
| LETA0 | 1.80E-02 | 1.92E-02 |

large width devices were used to improve device matching and minimize narrow channel effects.

Device measurements were taken on both n- and p-type transistors with a Hewlett Packard 4156A Precision Semiconductor Parameter Analyzer utilizing a Hewlett Packard 16442A Test Fixture. Figure 3.3 shows the test setup for the device curve measurements of the n-channel devices, while Figure 3.4 shows the test setup for the p-channel devices.

Measurements were taken on devices with a W/L ratio of 40. Table 3.2 shows the devices measured for their $I_D$ vs. $V_{GS}$ and $I_D$ vs. $V_{DS}$ characteristics. The $I_D$ vs. $V_{DS}$ curves were taken at approximately 100pA for better modeling of the current application.

### 3.4.3 Parameter Determination for HP 0.5μm Process

The extraction of the model parameters specified in Table 3.1 involved the following process:

1) Set the length dependencies of the required base parameters ($N_0$, $V_{FB}$, $ETA_0$) to zero.

2) Utilizing the measured $I_D$ vs. $V_{GS}$ curves for the 200μm/5μm device, adjust the $N_0$ parameter to match the

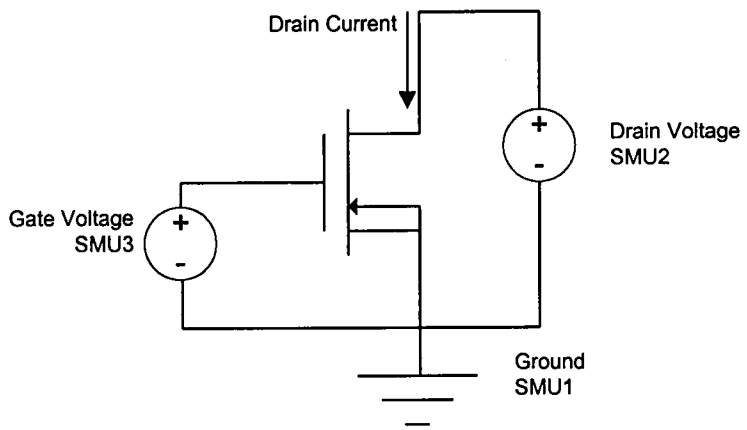



**Figure 3.3** N-channel MOSFET test setup on HP parameter analyzer.

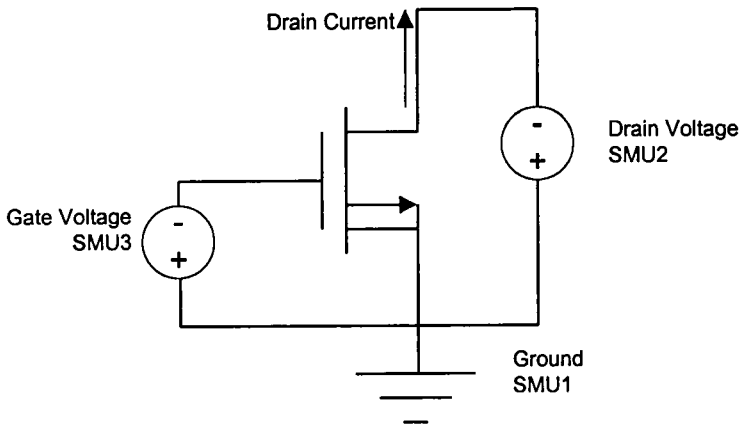



**Figure 3.4** P-channel MOSFET test setup on HP parameter analyzer.

**Table 3.2** Device sizes tested for their DC characteristics.

| | N-channel size | P-channel size |
|---|---|---|
| **Long channel device** | 200um/5um | 200um/5um |
| **Short channel device** | 20um/0.5um | 20um/0.5um |

exponential slope of the simulated curves to the measured curves.

3) Next, simultaneously adjust the $V_{FB}$ and the $ETA_0$ parameters to match the simulated $I_D$ vs. $V_{DS}$ curve to the measured curve of the 200μm/5μm device.

The base parameter set has now been determined with the long channel devices. The length dependencies of these parameters were next determined with the measured curves obtained for the short channel devices by:

4) Using the $I_D$ vs. $V_{GS}$ curve for the 20μm/0.5μm device, adjust the $LN_0$ parameter to model the shift in the exponential slope for the short channel device.

5) Finally, using the measured $I_D$ vs. $V_{DS}$ curve for the 20μm/0.5μm device, adjust the $LV_{FB}$ and $LETA_0$ parameters to simulate the shift in the current levels and the change in output impedance of the short channel device.

This procedure was implemented to determine the BSIM model parameters for both n- and p-channel devices. The final extracted parameter set is shown in Table 3.3. Figures 3.5-

**Table 3.3** Extracted BSIM Level 13 parameter values for n- and p-type devices in the HP 0.5µm process.

| Parameter | N-channel | P-channel |
|---|---|---|
| N0 | 1.52 | 1.31 |
| LN0 | -8.00E-02 | 4.90E-02 |
| VFB | -8.56E-01 | -1.13E-01 |
| LVFB | -1.30E-03 | 2.40E-02 |
| ETA0 | 1.00E-05 | 2.41E-03 |
| LETA0 | 3.90E-03 | 2.60E-01 |

3.10 show the simulated and measured device curves for each device.

The short channel effects are more significant in the p-channel devices, particularly the DIBL effect. Figure 3.10 shows a large exponential increase in drain current with respect to drain bias, which is typical for DIBL. Differences in the p-channel and n-channel devices that could explain the large variation in short channel dependencies include differences in effective channel lengths, substrate doping levels, and threshold voltages.

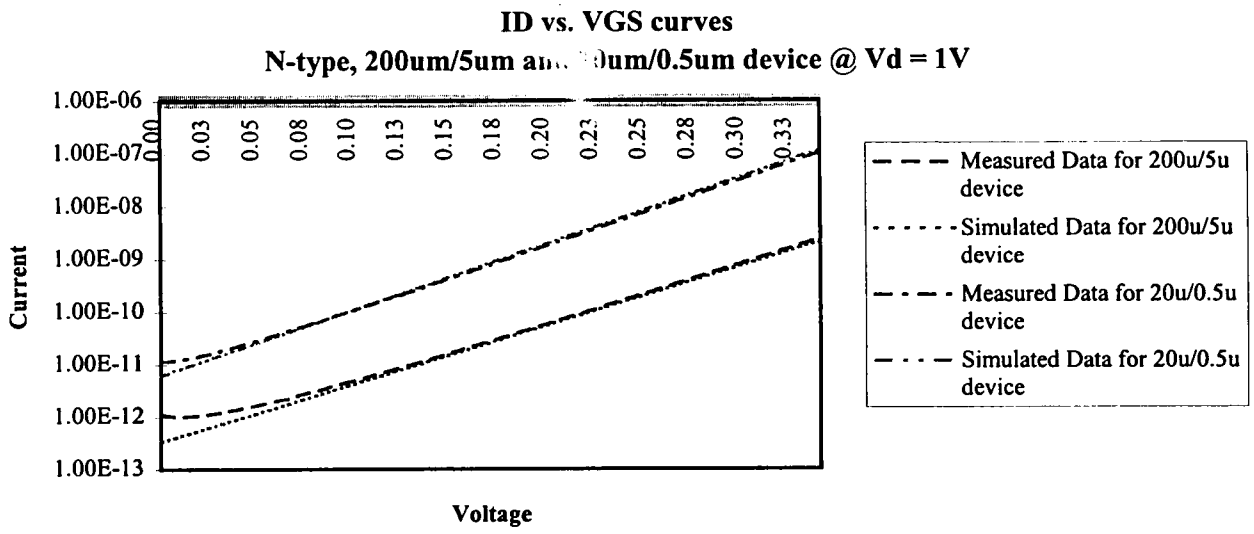





**Figure 3.5** Drain current versus gate voltage curves for an n-type long and short channel devices. Simulated and measured device curves are shown.

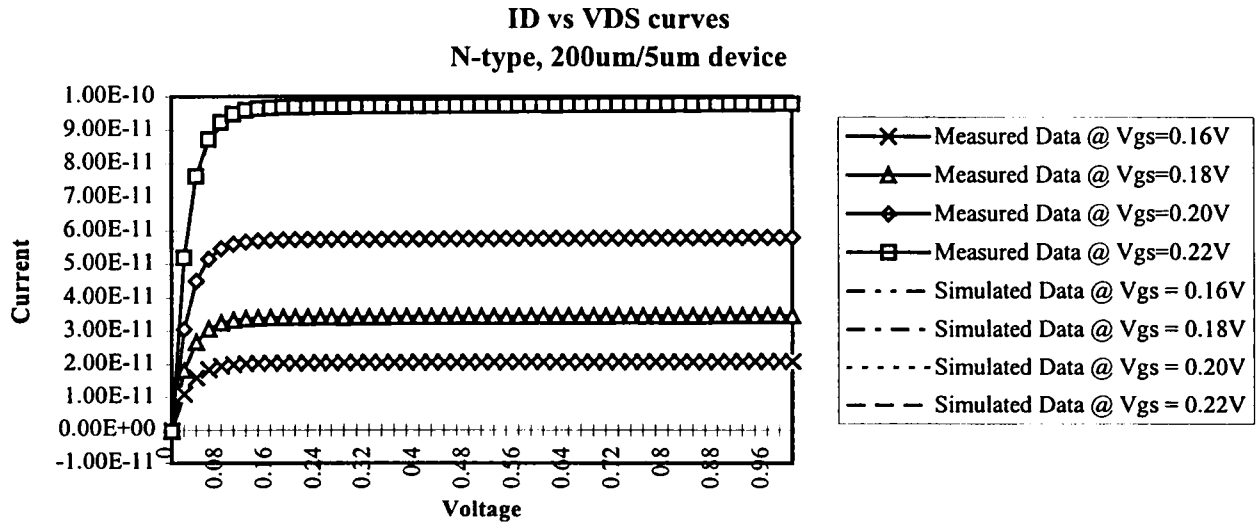



**Figure 3.6** Drain current versus drain voltage curves for an n-type long channel device. Simulated and measured device curves are shown.

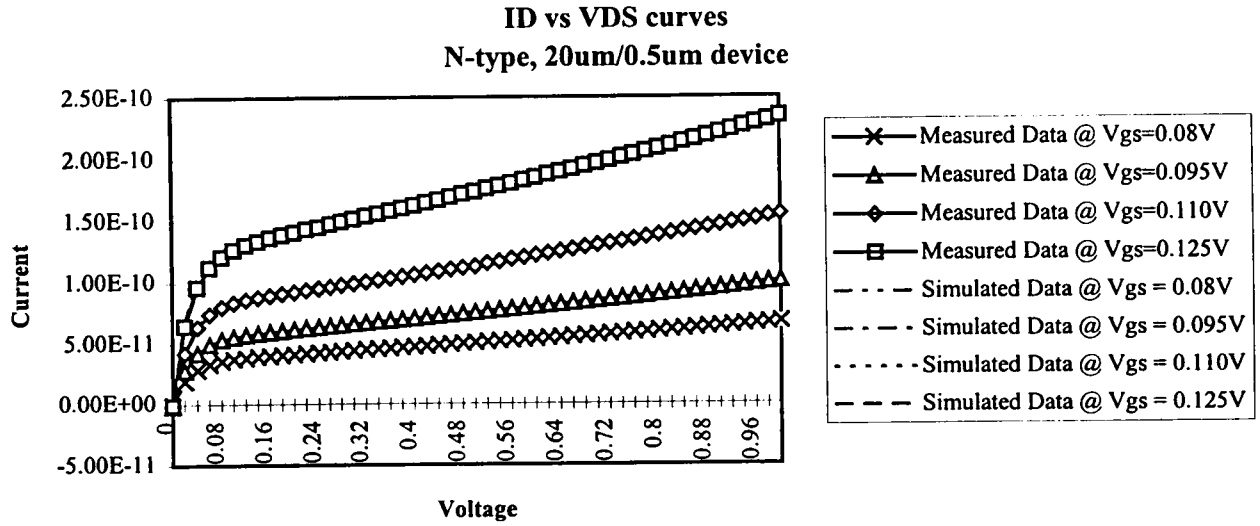





**Figure 3.7** Drain current versus drain voltage curves for an n-type short channel device. Simulated and measured device curves are shown.

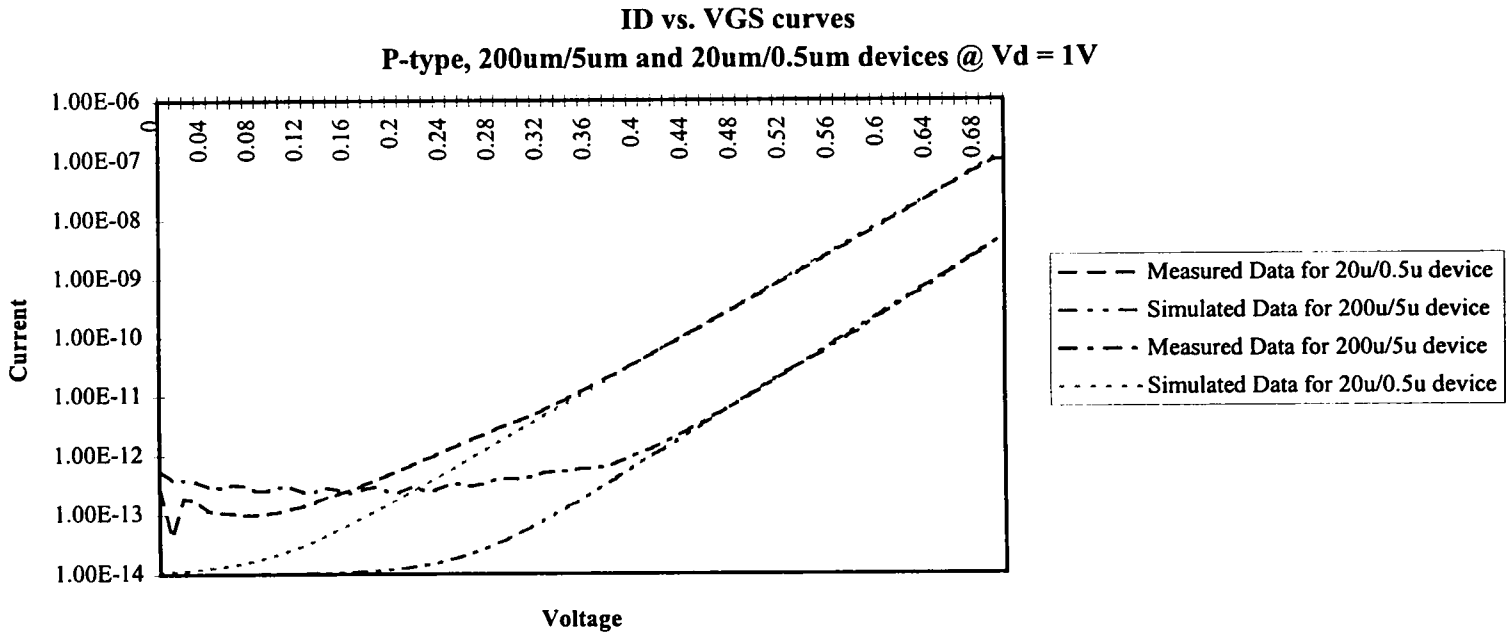



**Figure 3.8** Drain current versus gate voltage curves for a p-type long and short channel device. Simulated and measured device curves are shown.

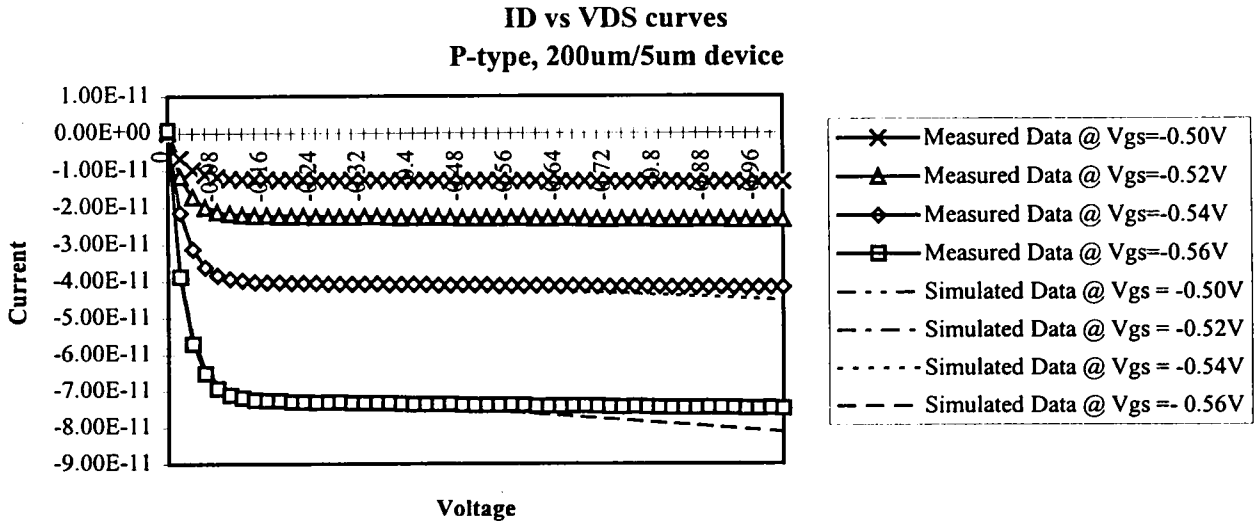





**Figure 3.9** Drain current versus drain voltage curves for a p-type long channel device. Simulated and measured device curves are shown.

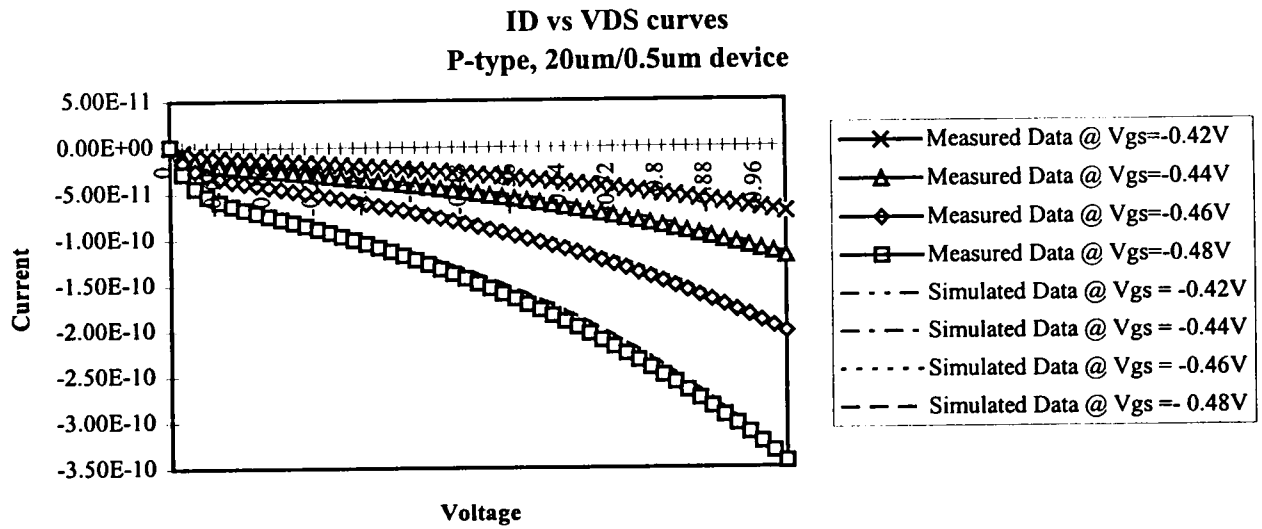



**Figure 3.10** Drain current versus drain voltage curves for a p-type short channel device. Simulated and measured device curves are shown.

# Chapter 4

# Electron Emitter Current Source Development

## 4.1 Circuit Description

### 4.1.1 Addressable Current Source

The addressable current sources for the prototype 5 x 5 electron emitter array were designed to maximize output impedance while utilizing reasonable resistance values and allowing easy adjustment of current levels. The schematic of an individual current source is shown in Figure 4.1. The design indicates the on-chip and board level components, along with their corresponding connections.

$V_{dd}$ is the power supply voltage and was regulated to 5.0V. The $V_{bias2}$ input biases the gates of MOSFETs M1 and M4, which operate as cascode devices to increase the current source output impedance. The TO_AD pin is the output of the current source and connects to the AD electron emitters. The $V_{catch}$ connection was implemented to maintain transistors M4 and M3 in saturation even if the AD was not emitting.

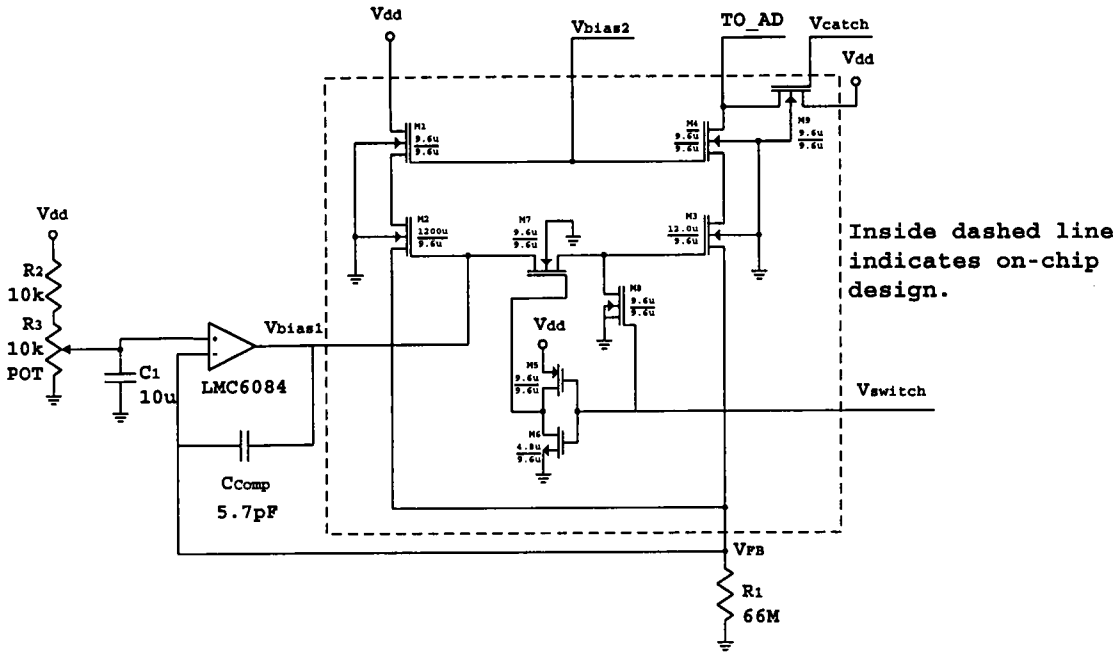



**Figure 4.1** Current source schematic with on-chip and board level circuitry designated.

The $V_{switch}$ input was utilized to activate individual current sources. The $V_{bias1}$ and $V_{FB}$ nodes connect the op-amp output and negative input terminal, respectively, to the on-chip circuitry.

The setting of the 100pA current level was accomplished with reasonable resistance values through current mirroring techniques. Resistors R2 and R3 set a DC level that establishes a current level through R1. The majority of the current flowing across R1 will be supplied by M2, because of the size differential between M2 and M3. Since M2 is 100 times larger than M3, a current level of 10nA through M2 will produce an approximate current level of 100pA through M3. Therefore, setting the potentiometer, R3, to 0.66V will produce a current source output of 100pA.

### 4.1.2 Current Source Activation Circuit

Each current source was activated through a digital control circuit connected to the $V_{switch}$ terminal. The digital control circuitry allowed the manual or programmable activation of the individual current sources. Figure 4.2 shows the digital control circuit for an individual source control line.

In manual mode the $V_{switch}$ digital control lines may be connected to +5V or ground. However, if the $V_{switch}$ control line is connected to the programming input, the source would be operated by the output of a shift register cell. An

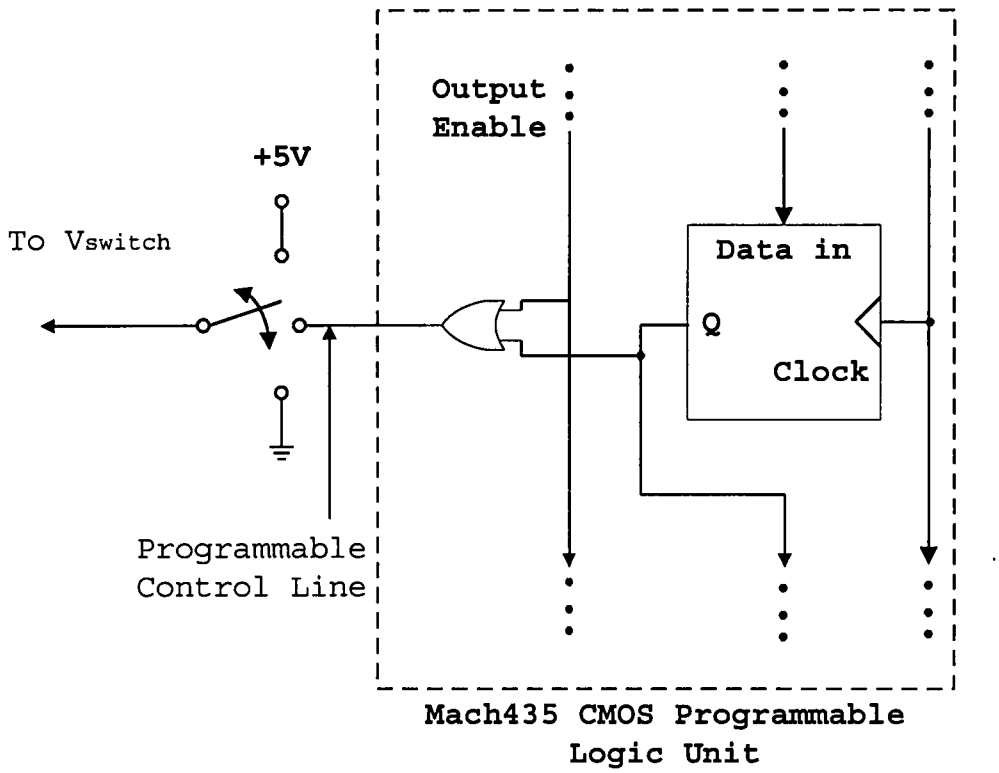



**Figure 4.2** Control cell for an individual current source.

output enable is integrated into the shift register design to allow simultaneous activation of all current sources. The current sources are activated by an active low input, therefore the output enable was implemented with an OR gate. Twenty-five programmable control cells were integrated into a 25 bit shift register design, utilizing a MACH435 CMOS programmable logic unit.

### 4.1.3 Design Considerations

There were several issues to contend with in the design of the individual current cells including adjustment of the current levels, voltage compliance, stability of the feedback loop, leakage current of the op-amps, and noise filtering. The output current was set by the potentiometer, R3, and could be adjusted from approximately 100pA to 380pA. Because the AD emitter test devices are biased from external power supplies, voltage compliance was not critical to the current application, however voltage compliance may be important in future current source designs. The $V_{dd}$ was regulated to limit current level dependence on power supply. The regulator and R3 were heavily filtered to limit the amount of noise entering the system. Lastly, the op-amp was selected to have a FET input to limit the amount of input bias current.

## 4.2 Current Source Design Analysis

### 4.2.1 Output Impedance Calculations

The output impedance of the current cell was maximized through several design techniques. The output of the current source utilized a cascode configuration with long channel devices to increase output impedance. Also, the extremely low current level of the source resulted in a large output impedance, due to the inverse relationship between output impedance and drain current. Lastly, the implementation of feedback to stabilize current levels and bias points further increased the output impedance of the current source.

The small signal circuit for a current source cell is shown in Figure 4.3. The current cell small DC signal output impedance is given by

$$R_{out} = r_{o4} + r_{o3}(1 + r_{o4}G_{m4}) + \frac{R_1(1 + A_o r_{o3}G_{m3})(1 + r_{o4}G_{m4})(r_{o2} + r_{o1} + r_{o1}r_{o2}G_{m1})}{R_1(1 + A_o r_{o2}G_{m2})(1 + r_{o1}G_{m1}) + r_{o2} + r_{o1} + r_{o1}r_{o2}G_{m1}}, \quad (4.1)$$

where, $r_{o1}, r_{o2}, r_{o3}, r_{o4},$ = output impedance of M1, M2, M3, M4,

$G_{m1}, G_{m2}, G_{m3}, G_{m4},$ = effective transconductance of M1, M2, M3, M4,

$A_o$ = open loop gain of LMC6084 op-amp,

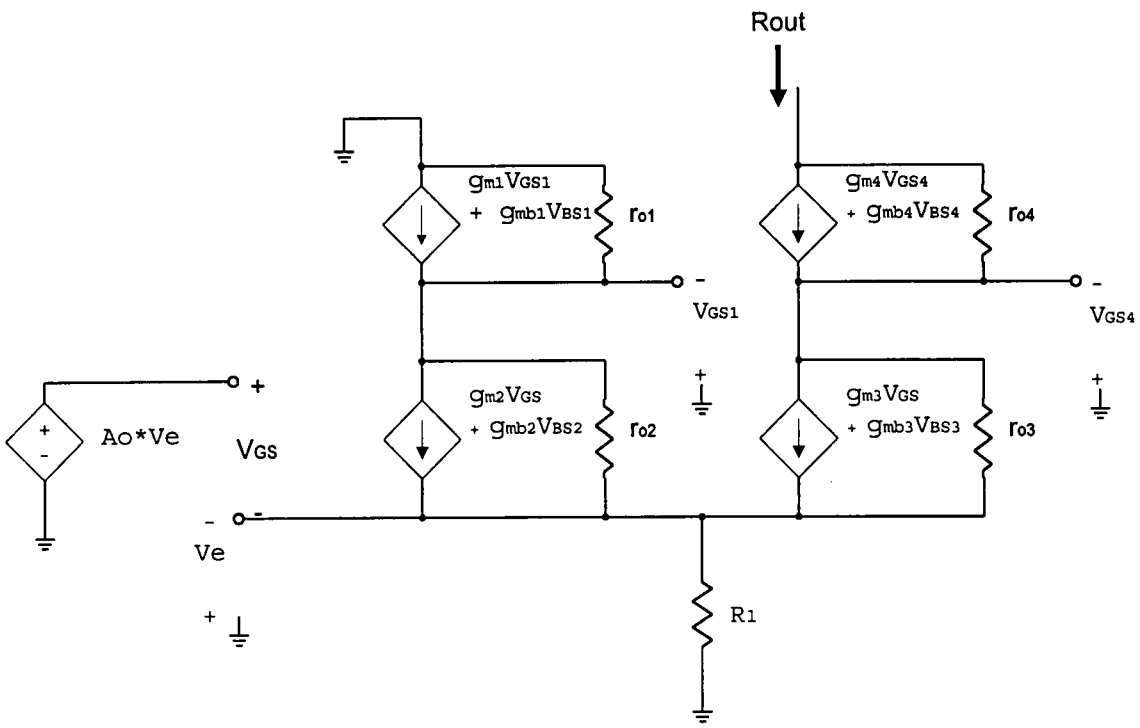



**Figure 4.3** Small signal equivalent circuit for an individual current source.

while assuming $A_o >> 1$. Also assuming that $r_o G_m >> 1$, the output impedance derivation could be simplified to

$$R_{out} \approx r_{o4} + r_{o3} r_{o4} G_{m4} + \frac{G_{m3} r_{o3} G_{m4} r_{o4}}{G_{m2}} . \qquad (4.2)$$

From equations (4.1) and (4.2), the output impedance was not significantly related to the gain of the feedback amplifier, $A_0$, due to the dual feedback paths, through M2 and M3. Also, the output impedance does not strongly depend on M1 and is primarily related to the small signal parameters of M4, M3, and M2.

The effective transconductance of devices, M1 and M4, was calculated by adding the body-source transconductance, $g_{mb}$, to the gate-source transconductance, $g_m$. For simplification, the effective transconductance of devices, M2 and M3, was calculated in the same manner. The small signal parameters for each device were determined through HSPICE simulations utilizing the BSIM Level 13 models provided for the ORBIT 1.2μm CMOS process. After biasing each device size within HSPICE to the current levels specified in the design, the gate-source, drain-source, and body-source transconductance parameters were then extracted for the small signal model. The open loop gain, $A_0$, of the LMC6084 op-amp was determined from the model provided by

National Semiconductor [34]. The small signal parameters obtained from the HSPICE bias point simulations are given in Table 4.1. The output impedance was then calculated using equations (4.1) and (4.2), returning a closed loop output impedance of 9.72 x $10^{12}\Omega$ and 9.68 x $10^{12}\Omega$, respectively.

### 4.2.2 Loop Stability Analysis

The use of feedback to stabilize bias points and regulate current levels requires an analysis of the loop stability. Because MOSFETs M2 and M3 are biased with extremely low currents, their transconductances were extremely low, resulting in a high source input impedance. The high impedance of the source node introduces a low frequency pole in the loop transmission.

The poles and zeroes for the op-amp were determined from the op-amp model provided through National Semiconductor. The loop transmission of the uncompensated feedback circuit is determined by breaking the loop at the negative input terminal of the op-amp and is given by

$$T(f) = \frac{1.2 * 10^6 (1 + j\frac{f}{3.3MHz})}{(1 + j\frac{f}{1.634Hz})(1 + j\frac{f}{10.4kHz})(1 + j\frac{f}{1.1MHz})(1 + j\frac{f}{4.98MHz})(1 + j\frac{f}{28.6MHz})}, \quad (4.4)$$

**Table 4.1** Small signal model parameters obtained from bias point simulations with HSPICE utilizing the BSIM Level 13 model parameters. The open loop gain, $A_o$, of the LMC6084 operational amplifier is also given.

| | | | |
|---|---|---|---|
| | | | |
| **MOSFET** | **gm (A/V)** | **gmb (A/V)** | **ro (Ohms)** |
| M1 | 2.25E-07 | 8.07E-08 | 9.11E+08 |
| M2 | 2.49E-07 | 1.05E-07 | 2.94E+08 |
| M3 | 2.56E-09 | 1.10E-09 | 2.87E+10 |
| M4 | 2.30E-09 | 7.86E-10 | 1.08E+11 |
| | | | |
| **Ao=** | 1.30E+06 | | |

where the zero at 3.3MHz and the poles at 1.634Hz, 1.1MHz, 4.98MHz, and 28.6MHz were introduced by the op-amp. The pole at 10.4kHz was located at the sources of M2 and M3. The frequency response of the uncompensated current cell is shown in Figure 4.4 by the magnitude and phase plots. The figure showed that the phase of the loop transmission crosses -180° before the magnitude plot reaches unity, resulting in an unstable feedback loop.

To compensate for the midband pole introduced by the large FET source impedance, a zero was added in the loop transmission. A capacitor was placed between the output and negative input of the op-amp, as shown if Figure 4.5. By setting capacitor $C_{Comp}$ equal to the negative terminal node capacitance of 5.7pF, the loop transmission was then given by

$$T(f) = \frac{1.2 * 10^6 (1 + j\frac{f}{3.3MHz})(1 + j\frac{f}{10.4kHz})}{(1 + j\frac{f}{1.634Hz})(1 + j\frac{f}{5.2kHz})(1 + j\frac{f}{1.1MHz})(1 + j\frac{f}{4.98MHz})(1 + j\frac{f}{28.6MHz})}, \quad (4.5)$$

The magnitude and phase plots for the compensated loop transmission are shown in Figures 4.6, resulting in a stable feedback loop with a phase margin of 69° and a gain margin of approximately 40db.

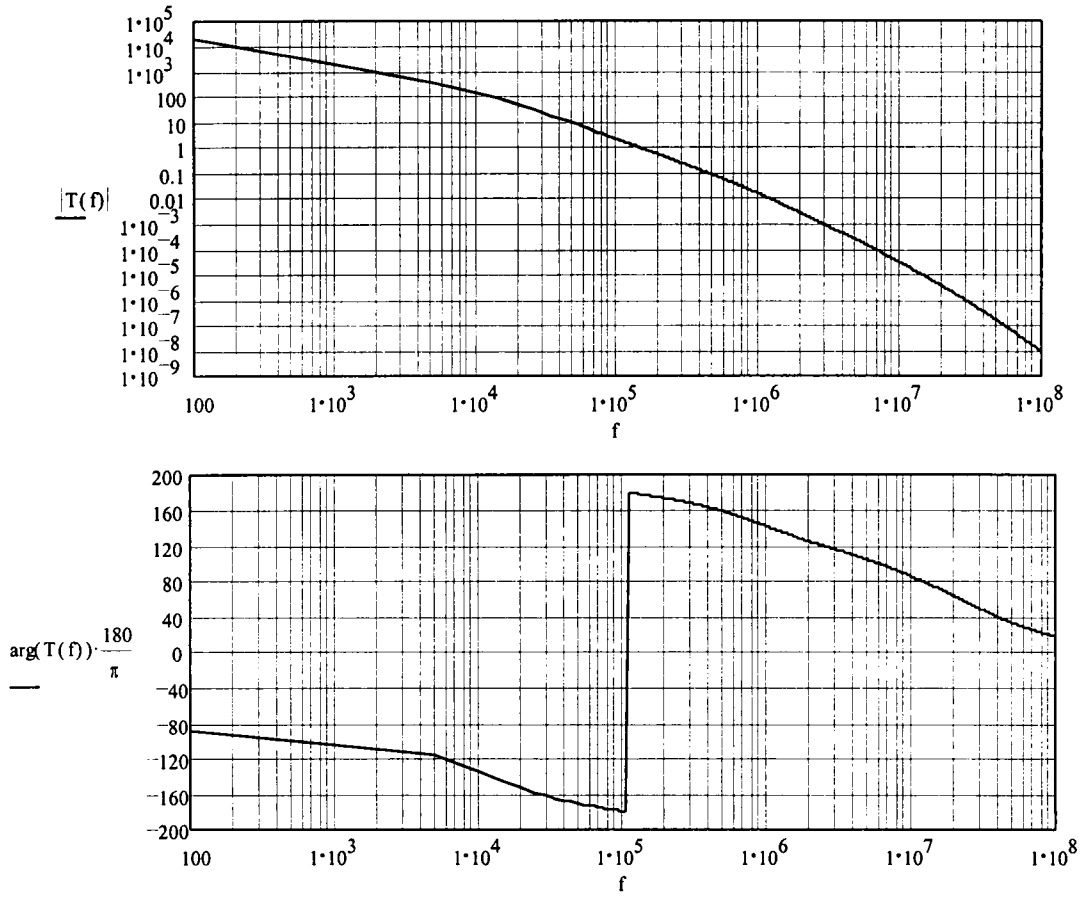



**Figure 4.4** Phase and magnitude plots for the uncompensated current cell loop transmission.

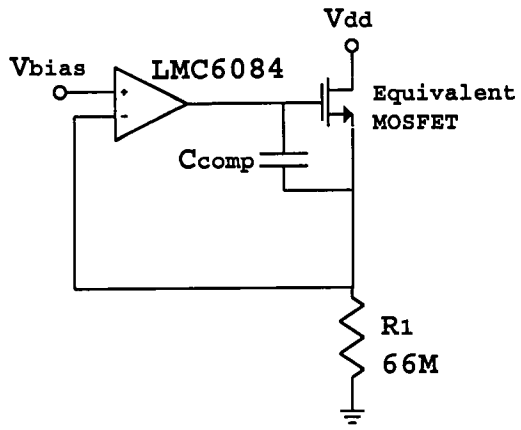



**Figure 4.5** Equivalent circuit for the loop transmission showing compensation used to stabilize the loop.

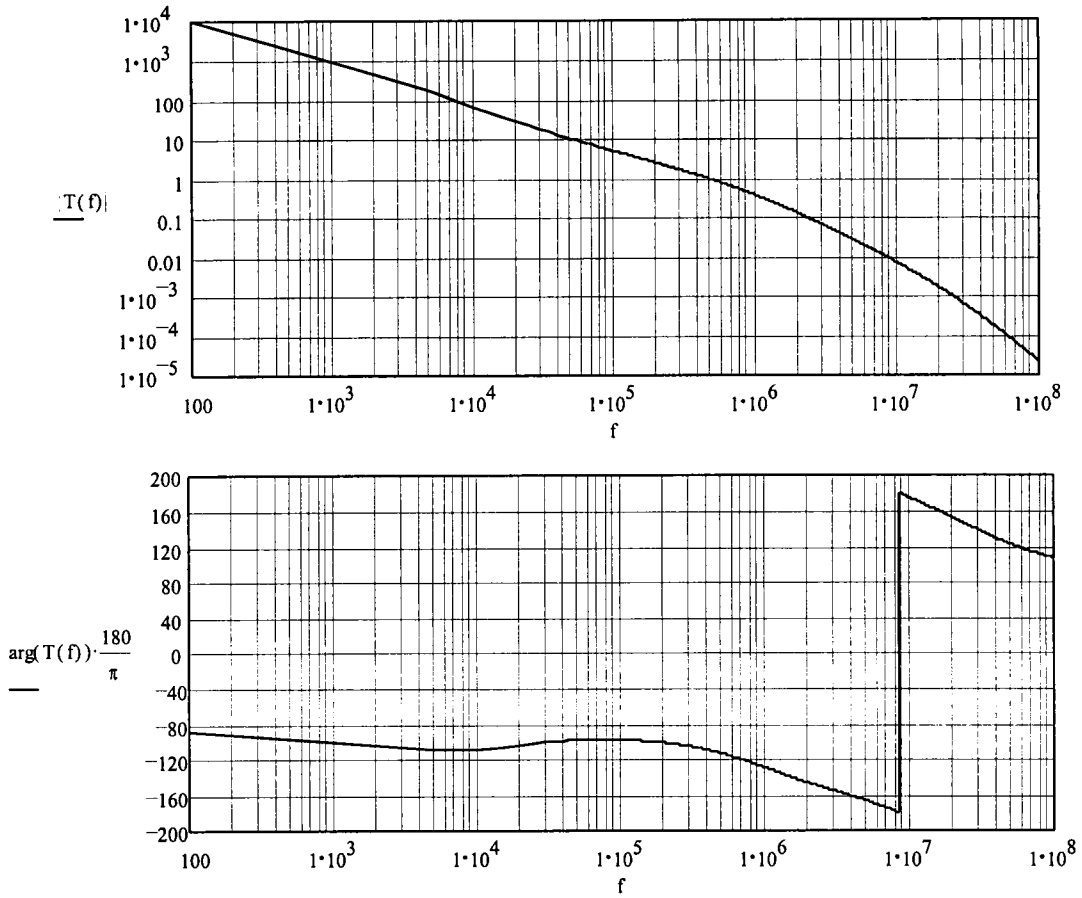



**Figure 4.6** Phase and magnitude plots for the compensated current cell loop transmission.

## 4.3 Circuit Layout

The circuit was designed in the ORBIT 1.2μm CMOS process utilizing the MAGIC layout tools. The layout primarily focused on current source matching and addressability. The design was implemented with eight current sources per chip, while permitting a wide range of adjustability per current source.

### 4.3.1 Current Source Matching

Current matching between different current sources is primarily limited by the current mirroring between M2 and M3. For a given reference current through R1 in each current source, the output current depends on how well M2 and M3 are matched. To improved matching, M3 was interdigitated with M2 to limit process variations and thermal effects between M2 and M3. For further improvement, M2 was constructed by paralleling a large number of M3 size transistors. Constructing the M2 device as a multiple of M3 devices minimized size mismatch effects. Figure 4.7 shows the layout of an individual current cell with the individual devices labeled.

As shown in Figure 4.7, M3 was divided into four parallel transistors, one for each quadrant of M2, with a size of 3.0μm/9.6μm for each device. Since M2 was required to have 100 times the current level of M3, M2 was

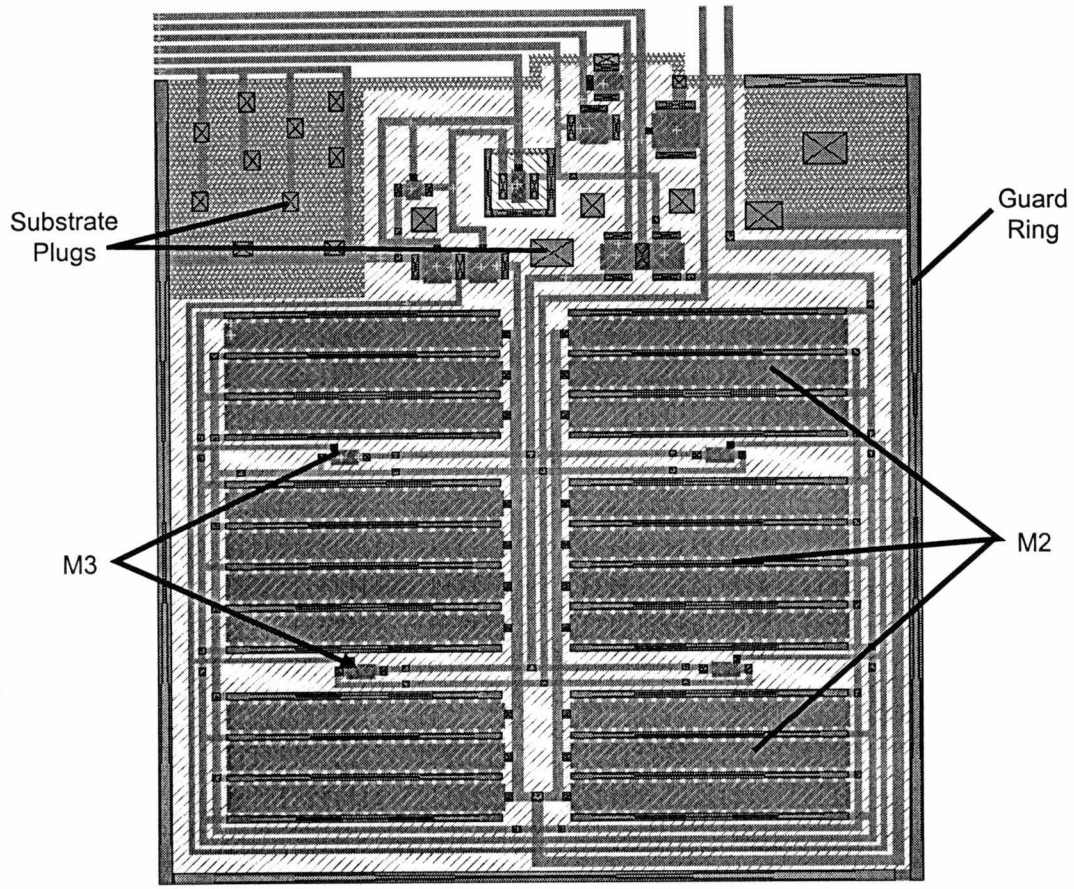



**Figure 4.7** Current source cell with guard ring and substrate plugs.

constructed with a multiplicity vector of 400 with a size of 3.0μm/9.6μm. The four transistors comprising M3 were then interdigitaded within four regions of the M2 transistor to limit the effects of process variations running horizontally, vertically, and diagonally across the wafer.

### 4.3.2 Source Addressability

Individual current sources were addressed by a digital control line through $V_{switch}$, which controlled the gate bias of M3. A digital high would short circuit M8 to ground while M7 would become an open circuit, therefore deactivating M3 and the current source. A digital low, however, would connect the gates of M3 to M2, thus biasing M3 and M2 to the same $V_{GS}$ and activating the current source.

### 4.3.3 Individual Source Adjustment

To maximize the number of current sources per chip certain controls were shared between current cells. Each source shared their $V_{bias2}$ and $V_{catch}$ pins. The $V_{bias2}$ pin biased the gates of the M1 and M4 transistors, while the $V_{catch}$ pin was utilized to maintain current source bias despite load conditions. The sharing of the $V_{bias2}$ and $V_{catch}$ pins do not considerably degrade the output impedance of the current sources, while also having little effect on the current matching between sources.

## 4.4 Circuit Extraction and Simulation

The current cells were extracted and simulated within HSPICE utilizing BSIM Level 13 models provided for the ORBIT 1.2μm process. The values provided for the $N_0$, $ETA_0$, and $V_{FB}$ parameters and with their respective length dependencies are shown in Table 4.2, with the complete BSIM parameter set shown in Appendix 1. The model for the LMC6084 operational amplifier was also obtained for simulation of the entire circuit. The complete SPICE source file, including the LMC6084 model, is given in Appendix 2.

Extraction of the circuit required that the transistors be extracted with multiplicity vectors. Figure 4.8 shows the ratio of drain current between M2 and M3 with and without using the multiplicity vector in the size calculation. Due to the length and width dependencies of each device, the current levels are considerably different if same size transistors are used in the current mirror.

The circuit was simulated to determine output impedance and loop stability. The output impedance was found to be $10.8 \times 10^{12}\Omega$. Lastly, the feedback loop was found to be stable with a phase margin of 60°, as shown in Figure 4.9.

**Table 4.2** BSIM Level 13 parameter values for the ORBIT 1.2μm process.

| Parameter | N-channel | P-channel |
|---|---|---|
| N0 | 1.65 | 1.32 |
| LN0 | 2.51E-02 | 1.43E-01 |
| VFB | -6.71E-01 | -2.19E-01 |
| LVFB | 1.31E-02 | 6.90E-02 |
| ETA0 | -6.68E-05 | -9.40E-03 |
| LETA0 | 1.08E-02 | 4.10E-02 |

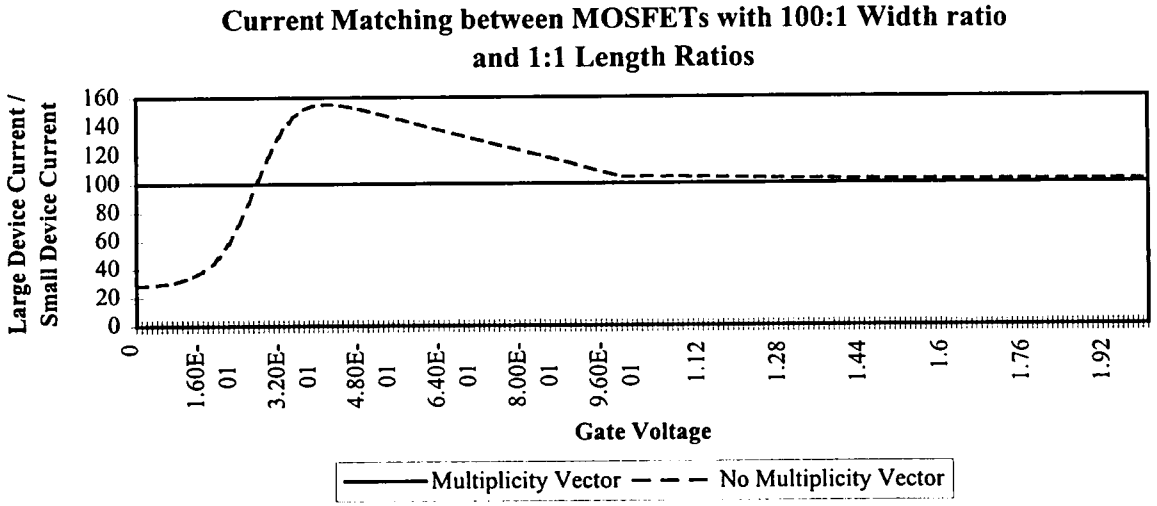





**Figure 4.8** Drain current matching between large and small geometry devices with a W/L ratio of 100, utilizing multiplicity vectors in the circuit extraction.

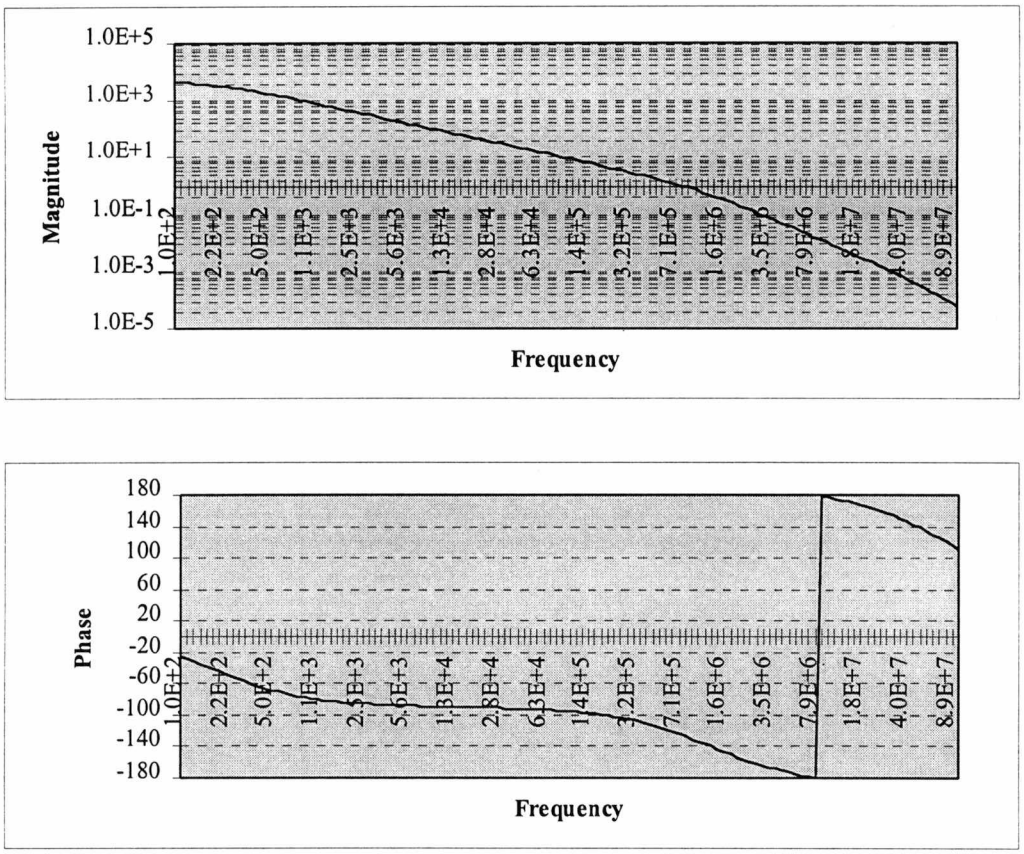



**Figure 4.9** Simulated phase and magnitude plots for compensated current source.

# Chapter 5

# Experimental Testing and Results

## 5.1 Current Source Operation

### 5.1.1 Board Layout and Construction

The final board layout, including the addressable current sources and the digital control board, is shown in Figure 5.1. The digital control board contains the programmable logic and manual control array for the current sources, while the current source board includes the current source chips and other board level components. The three arrays on the digital control board are the manual/programmable switches used to activate individual current sources. The connection for the AD chip was placed on the back side of the current source board to conserve space.

The chip layout is shown in Figure 5.2 and took an area of 2.20mm x 2.20mm. The large block structure in the center of the chip layout, Figure 5.2, is a $V_{dd}$ to ground bypass capacitor. Several other bypass capacitors were placed along the $V_{bias2}$ and $V_{catch}$ bias lines to prevent noise from

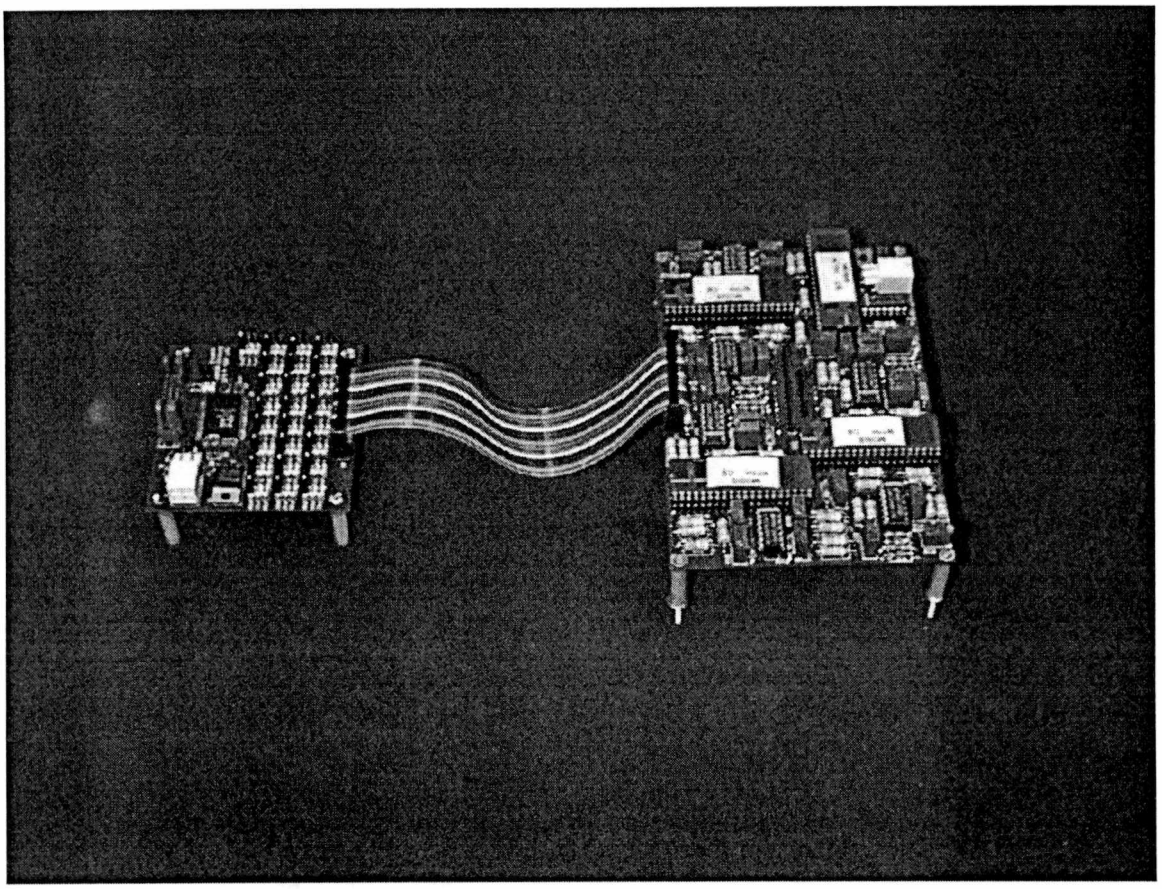


**Figure 5.1** Picture of the Digital Control Board (left) and Current Source Board (right).

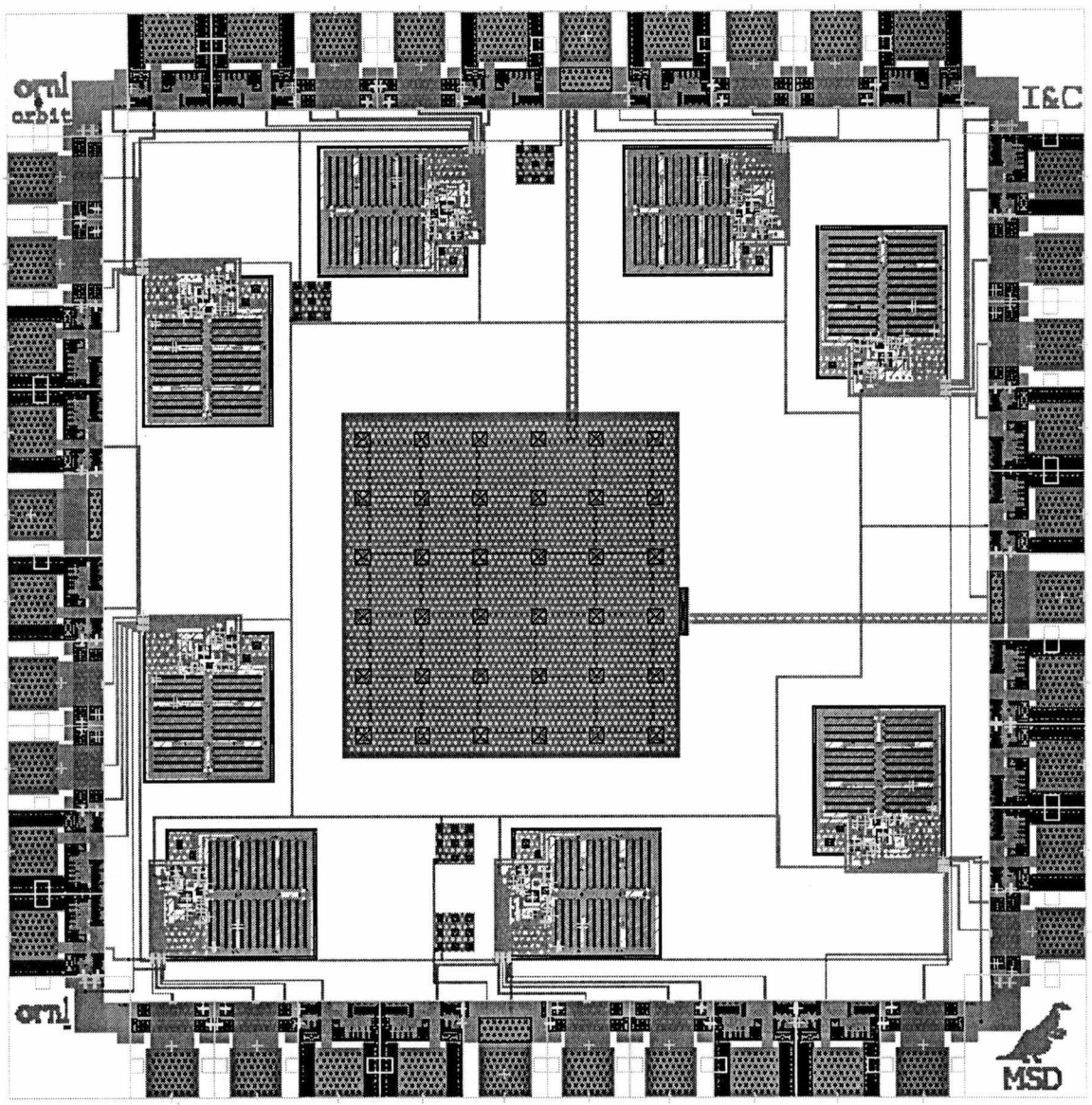



**Figure 5.2** Layout of Amorphous Diamond current source chip.

entering the signal path. The eight rectangular structures in Figure 5.2 are the individual current sources, with each having a 266µm x 341µm area.

### 5.1.2 General Circuit Operation

The circuit was biased and tested for power consumption, feedback operation, and loop stability under differing load conditions. The entire design, including the programmable logic chip, drew approximately 200mA, while sinking only 20mA without the programmable logic. The feedback was operational and stable at a current source setting of 100pA.

## 5.2 100pA Current Source Impedance Measurements

### 5.2.1 Test Setup

Each current source was biased to 100pA, through adjustment of R3, and manually activated on the digital control board before testing. The current sources were tested by sweeping the output with a voltage source. The voltage sweeps were implemented with a Hewlett Packard 4156A Precision Semiconductor Parameter Analyzer utilizing a Hewlett Packard 16442A Test Fixture.

### 5.2.2 Current Source Measurement Results

The current sources were first tested for output impedance dependence on $V_{bias2}$. Each source was swept from 2.0V to 3.0V with $V_{bias2}$ settings of 1.5V, 2.0V, and 2.5V. Each of the five current source chips had their individual current sources measured for their current-voltage curves. The output of each current source was averaged for each $V_{bias2}$ setting resulting in the curves shown in Figure 5.3. The output impedance for the current cells was found to be 81.0GΩ, 78.4GΩ, and 59.3GΩ for $V_{bias2}$ equal to 1.5V, 2.0V, and 2.5V respectively.

The large difference of 10.8TΩ to 78.4GΩ between the simulated and measured output impedance could possibly be attributed to several factors including a finite pad impedance, reverse biased junctions, and faulty device models. At sub-10pA current levels, pad and reverse biased junction leakage become significant, while models of these effects may not be accurate. Measurements were not able to attribute the limiting factor in the output impedance to a particular mechanism. Further investigation is needed to determine the reason for the large discrepancy between the simulations and measurements, while also providing model or layout improvements that could alleviate this problem.

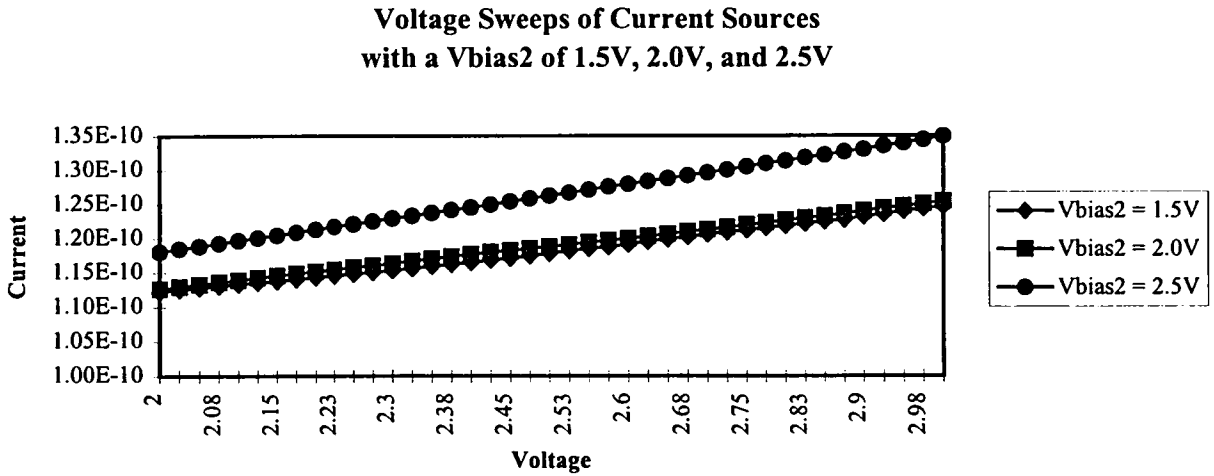





**Figure 5.3** Voltage sweeps of current sources for Vbias2 settings of 1.5, 2.0, and 2.5V.

## 5.3 100nA Current Source Impedance Measurements

The 100pA current level was selected to minimize the space charge effects associated with millions of parallel electron beams. However, the current application was developed for the individual testing of twenty-five electron emitters per chip. To simplify measurements, the current source requirements were relaxed to 100nA per source. The increased current level is easier to measure with current probes and also allows an improved lifetime study of the emitters, due to the increased current densities.

To increase the current level to 100nA per source, R1 was replaced with a 70kΩ resistor. Potentiometer, R3, was then adjusted to set a voltage of 0.70V across R1, resulting in a current of approximately 10μA through M2. The 10μA through M2 would therefore establish a 100nA current through M3. The current sources were able to regulate the 100nA current level to less than 0.5% with a one volt change on the output, resulting in an output impedance greater the 2.0GΩ.

## 5.4 Amorphous Diamond Measurements

### 5.4.1 Design of AD Emitters

The array of Amorphous Diamond emitters were initially designed with all of the emitters connected in parallel.

Figure 5.4 gives the general construction of an individual AD emitter, showing that each emitter is connected directly to a p Silicon substrate while sharing the same anode. The emitters were evenly spaced in a 5 X 5 array, as shown in Figure 5.5, with an individual emitter opening shown in Figure 5.6.

### 5.4.2 Test Results

The AD emitters were connected to the current sources for stability tests. Since the emitters were assembled in parallel, the current sources had to be connected in parallel, therefore the total current for the entire chip was 2.50μA. The AD chip substrate was connected to the parallel current sources while the AD anode was connected to a 5.0V source measurement unit. The current was measured to be approximately 2.5μA and was stable through several hours of operation. The AD emitters are currently under test for their I-V characteristics.

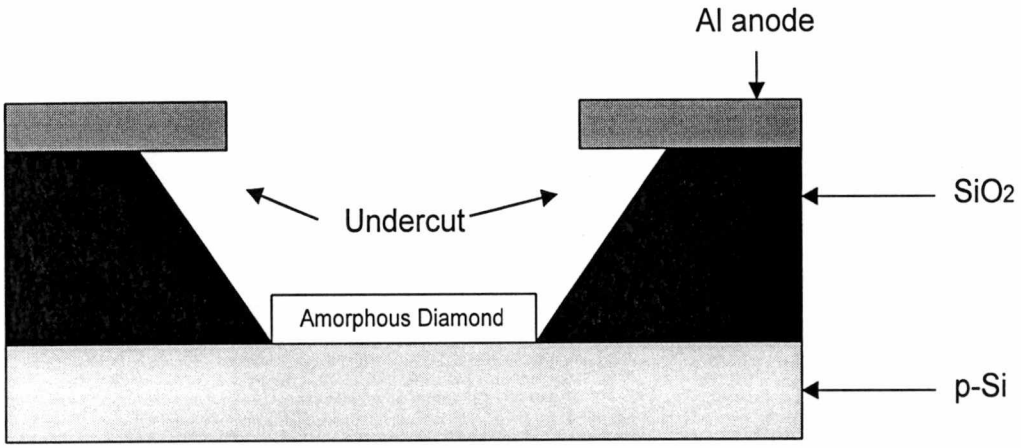



**Figure 5.4** Construction of AD emitter.

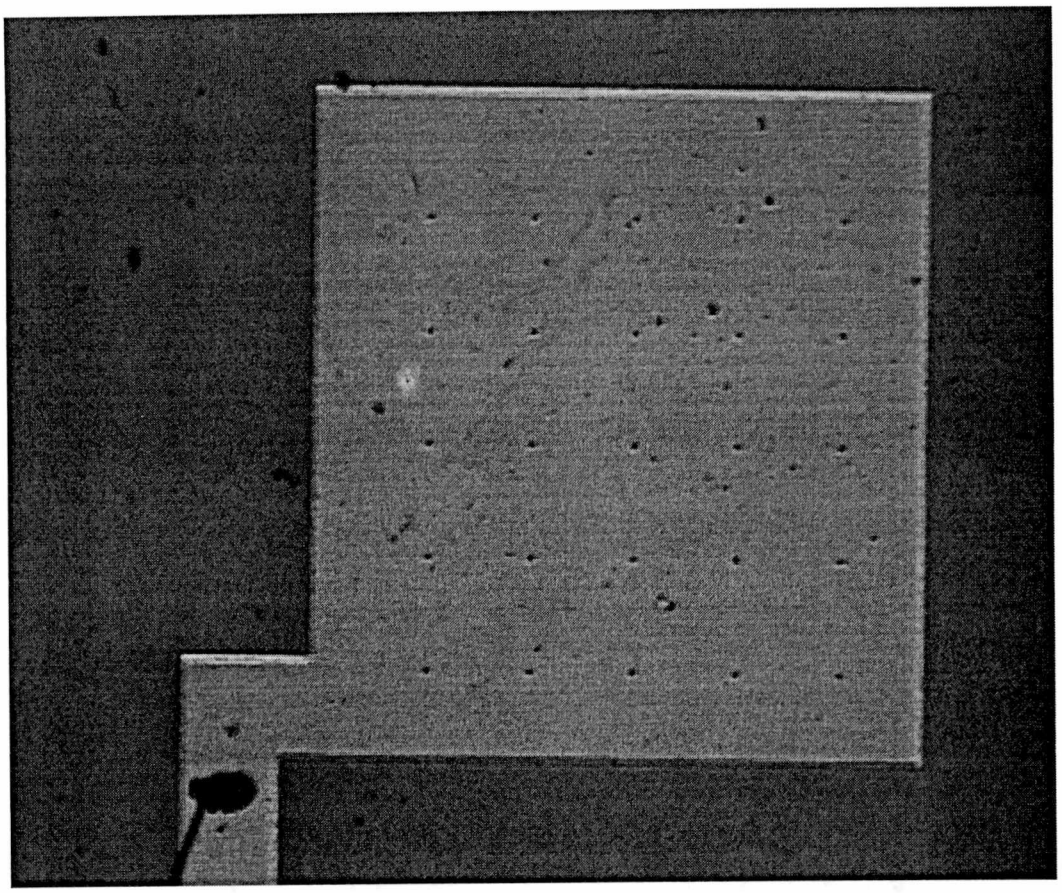


**Figure 5.5** Picture of 5 X 5 AD emitter array.

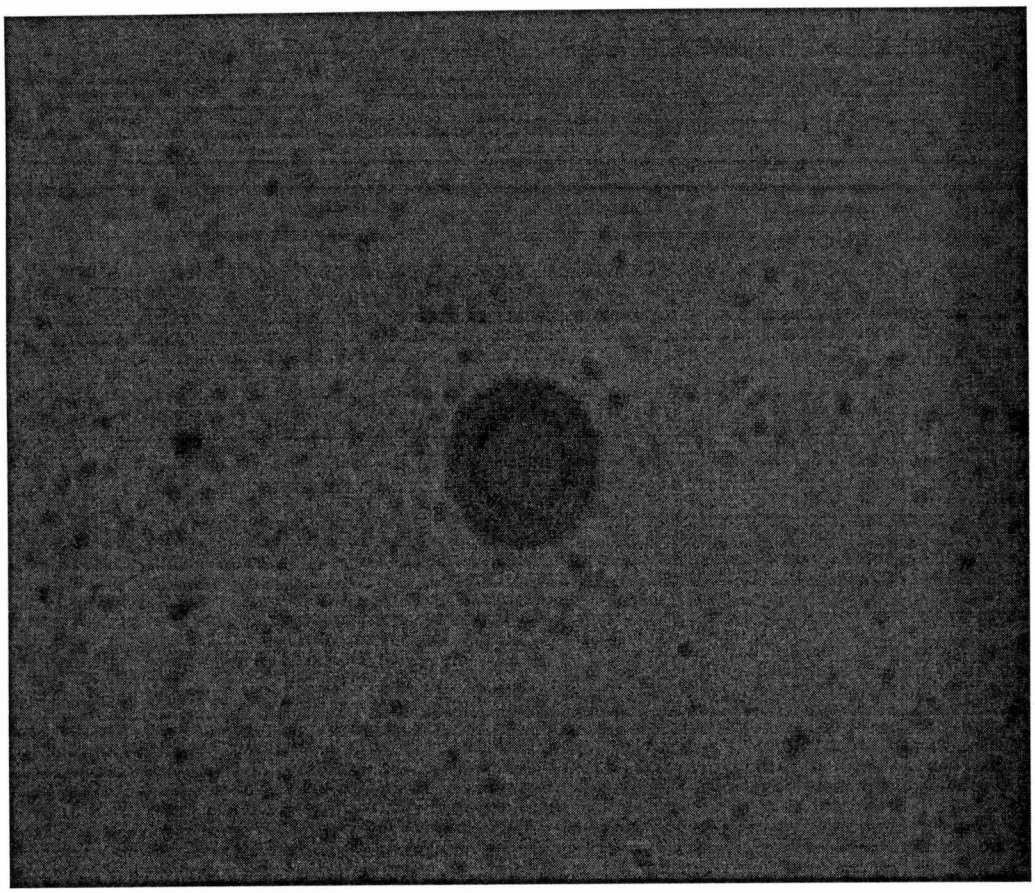


**Figure 5.6** View of anode opening showing an AD emitter.

# Chapter 6

# Conclusions and Future Work

## 6.1 Conclusions

The pressure to continue the exponential increase in IC chip density, as predicted by Moore's Law, is motivating research that will lead to a Massively Parallel Electron Beam Lithography (MPEBL) system. AD is proposed as the electron emitter of the MPEBL system because of its low-temperature, low-field emission properties and its possible ease in fabrication. The strict emission regulation and source addressability properties of the MPEBL system require the development of addressable array of current sources for regulation of electron emission.

In the final system implementation each current source will be required to operate at 100pA or lower to avoid space charge effects. This low current level, combined with tight emission regulation, will require that the current sources have an extremely high output impedance. Also, minimization of device geometries is essential for maximizing the number of current sources per chip. Therefore, a thorough understanding of device operation in weak inversion and

small geometry effects is critical to the design and implementation of an addressable array of current sources.

In this work, models were developed for the HP 0.5μm CMOS process for simulation of future current source designs. A BSIM level 13 parameter set was updated to model device operation in weak inversion, particularly output impedance and short channel effects. A process for extraction of BSIM level 13 parameters was developed utilizing curve fitting to measured device curves.

Twenty-five 100pA current sources were designed, simulated, and fabricated for testing prototype AD electron emitters. The current sources were implemented in the ORBIT 1.2μm CMOS process and were designed to maximize output impedance while allowing easy adjustment and activation of individual sources. The output impedance of the current sources was calculated to be approximately 10TΩ through simulations and hand calculations. However, the measured output impedance of 80GΩ was probably due to inadvertent leakage paths, where further research is needed to determine the exact mechanism.

The current sources were constructed and exhibited a measured output impedance of about 80GΩ. The feedback loop was stable with a simulated phase margin of 60°. For the prototype electron emitters, the current sources were

operated at a current level of 100nA, where the measured output impedance was greater than 2.0GΩ.

Finally, the AD emitters were connected to the current sources for stability testing and lifetime studies. The current sources and electron emitters were stable over several hours of testing. Currently, the AD emitters are being tested for their I-V characteristics

## 6.2 Future Work

Additional work is needed to explain the discrepancy between the simulated and measured output impedance of the current sources. Further development of device models, primarily for sub-0.5μm processes, will be required for implementation of a massive array of current sources. Maximization of the number of current sources per chip will require the implementation of minimum geometry devices, furthering the need for a greater understanding of short channel as well as narrow width effects. A massively parallel addressable field emitter array will eventually need to be designed, simulated, and fabricated for an MPEBL system. Finally, further documentation and understanding of AD emission properties and lifetime is required before final system implementation.

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# Appendices

# Appendix 1

# Appendix 1

```
**********************************************************
*
* Model Definitions for HSPICE
*
**********************************************************

.model CMOSP Pmos(LEVEL=13 capop=4 TOXM=22.5m
+ VDDM=6,LD=0.1U, WD=0.43U NSUB=1E16 PB=0.7298 MJ=0.4022
+ CJ=451U PJW=0.863 MJSW=0.3646 CJSW=445.4P JS=610N JSW=0.2N
+ FC=0.5 CGSO=108P CGDO=108P CGBO=625P TREF=25 xpart=1
+ RSH=370)
+ af=0.5 kf=4.2e-31 nlev=1 acm=3 hdif=1.5u
+ muz=300
+ vfb=-0.2192     lvfb=0.069      WVFB=0.1241
+ phi0=0.7692     LPHI=0.0598     WPHI=0
+ MUS=247.7       LMUS=31.66      WMUS=-21.15
+ u00=0.1468      LU0=0.2623      WU0=-0.0585
+ k1=0.4806       LK1=2.167m      WK1=0.0336
+ k2=0.01617      LK2=0.0551      WK2=-1.282m
+ ETA0=-9.4m      Leta=0.0408     WETA=0
+ U1=0.2659       LU1=-0.138      WU1=0
+ X2E=-0.792m     LX2E=-1.545m    WX2E=-0.9233m
+ X3E=1.183m      LX3E=-2.16m     WX3E=-4.061m
+ X2MZ=8.366      LX2MZ=13.83     WX2MZ=1.822
+ X2MS=14.81      LX2MS=1.524     WX2MS=0.801
+ X3MS=1.0        LX3MS=0         WX3MS=-0.0526
+ x2u0=-0.2914m   LX2U0=0.0691    WX2U0=0.5875m
+ X2U1=-0.1138m   LX2U1=3.39m     WX2U1=0
+ X3U1=0.02579    LX3U1=-0.01815  WX3U1=0
+ N0=1.317        LN0=0.143       WN0=0
+ NB=63.24m       LNB=-97.29m     WNB=-0.4176
+ ND0=0           LND=0           WND=0

.model CMOSN Nmos(LEVEL=13 capop=4 TOXm=22.5E-3 VDDM=7
+ LD=0.1u WD=0.104u NSUB=1E16 PB=0.749 MJ=0.4158 CJ=554.2U
+ PJW=0.9958 MJSW=0.4017 CJSW=371.9P JS=0.25U JSW=75P FC=0.5
+ CGSO=310P CGDO=310P CGBO=340P  TREF=25 XPART=1 RSH=350)
+ af=.5 kf=2.3e-29 nlev=1 acm=3 hdif=1.5u
+ MUZ=650
+ VFB=-0.6708  LVFB=13.14m     WVFB=-0.1
+ PHI=0.7665   LPHI=28.62m    WPHI=0
+ MUS=559.9    LMUS=44.18      WMUS=-20
+ U00=99.48m   LU0=0.2747      WU0=-0.0506
+ K1=1.172     LK1=-33.63m     WK1=0.2099
+ K2=62.18m    LK2=40.96m      WK2=0.020
+ ETA0=-66.8u  LETA=10.76m     WETA=0.0158
+ U1=0.06      LU1=0           WU1=0
+ X2E=-0.8775m LX2E=-4.17m     WX2E=-1.246m
+ X3E=0.957m   LX3E=-1.76m     WX3E=-4.8m
```

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+ X2MS=-0.8378 LX2MS=22.12      WX2MS=3
+ X3MS=-0.3     LX3MS=0          WX3MS=0
+ X2U0=-7.547m LX2U0=33.22m     WX2U0=6.912m
+ X2U1=0.017m  LX2U1=-0.5m      WX2U1=0
+ X3U1=0.26     LX3U1=0          WX3U1=0
+ N0=1.649      LN0=0.0251       WN0=-0.544
+ NB=74.1m      LNB=19.93m       WNB=-0.501
+ ND0=0          LND=0            WND=0
**********************************************************
```

# Appendix 2

# Appendix 2

```
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* File Location        /msd6/vannjm/magic/cell
*************************************************************

.OPTION converge=1 LIST NODE POST GMINDC=.1f GMIN=.1f
.ic v(2)=0.66 v(3)=1.6603 v(6)=1.2931 v(11)=1.1519

.op
.dc Vdlc 3 4 .01
.ac dec 20 1 1000000000

Vdd 10 0 5
Vdlc 9 0 dc 3.5 ac .001
Vbias 5 0 3
Vbias1 50 0 .66

Rbias 2 0 66000000
Ccomp 3 2 5.7pF

Vpos 100 0 8
Vneg 101 0 -8
XOP 50 2 100 101 3 LMC6084

M1 10 5 11 0 CMOSN W=9.60U L=9.60U GEO=0
M2 11 3 2 0 CMOSN M=400 W=3.00U L=9.60U GEO=0
M7 3 8 4 0 CMOSN W=9.60U L=9.60U GEO=0
M8 4 7 0 0 CMOSN W=9.60U L=9.60U GEO=0
M3 6 3 2 0 CMOSN M=4 W=3.00U L=9.60U GEO=0
M4 9 5 6 0 CMOSN W=9.60U L=9.60U GEO=0
M9 10 12 9 0 CMOSN W=9.60U L=9.60U GEO=0
M5 8 7 0 0 CMOSN W=4.80U L=4.80U GEO=0
M6 8 7 10 10 CMOSP W=9.60U L=4.80U GEO=0
C1 0 5 1.0F
C2 0 2 1.0F
C3 4 2 1.0F
C4 6 2 1.0F
C5 0 12 1.0F
C6 0 7 1.0F
C7 0 3 1.0F
C8 4 11 1.0F
C9 3 6 2.0F
C10 0 9 1.0F
C11 3 2 2.0F
C12 11 2 4.0F
C13 0 10 1.0F
C14 3 0 901.0F
C15 5 0 81.0F
C16 7 0 88.0F
```

```
C17 12 0 55.0F
C18 10 0 67.0F
C19 11 0 220.0F
C20 2 0 378.0F
C21 9 0 64.0F
C22 4 0 234.0F
C23 6 0 103.0F
C24 8 0 28.0F

*** Node Listing for subckt:  current_cell
** N0                          ==  IdealGND
** N2                  [U=2]    ==  Vfb
** N3                  [U=2]    ==  Vbias1
** N4                  [U=3]    ==  N4
** N5                  [U=2]    ==  Vbias2
** N6                  [U=2]    ==  N6
** N7                  [U=3]    ==  Vswitch
** N8                  [U=3]    ==  N8
** N9                  [U=2]    ==  To_DLC
** N10                 [U=4]    ==  Vdd
** N11                 [U=2]    ==  N11
** N12                 [U=1]    ==  Vcatch

* Connections:      Non-inverting input
*                   |   Inverting input
*                   |   |   Positive power supply
*                   |   |   |   Negative power supply
*                   |   |   |   |   Output
*                   |   |   |   |   |
*                   |   |   |   |   |
.SUBCKT LMC6084A 1   2  99  50  28
* CAUTION:  SET .OPTIONS GMIN=1E-16 TO CORRECTLY MODEL INPUT
BIAS CURRENT.
*
* Features:
* Operates from single supply
* Rail-to-rail output swing
* Low offset voltage (max) =          350uV
* Ultra low input current =            10fA
* Slew rate =                        1.5V/uS
* Gain-bandwidth product =            1.3MHz
* Supply current =                    450uA/Amplifier
*
* NOTE: - Model is for single device only and simulated
*         supply current is 1/4 of total device current.
*       - Noise is not modeled.
*       - Asymmetrical gain is not modeled.
*
CI1 1  50 2P
CI2 2  50 2P
* 1.634 Hz pole capacitor
C3  98 9  9.715N
```

```
* 1.1 MHz pole capacitor
C4  6  5  13.95P
* 4.98 MHz pole capacitor
C5  98 15 31.9F
* Drain-substrate capacitor
C6  50 4  3P
* 28.6 MHz pole capacitor
C7  98 11 5.62F
DP1 1  99 DA
DP2 50 1  DX
DP3 2  99 DB
DP4 50 2  DX
D1  9  8  DX
D2  10 9  DX
D3  18 20 DX
D4  21 18 DX
D5  26 24 DX
D6  25 27 DX
D7  22 99 DX
D8  50 22 DX
D9  0  14 DX
D10 12 0  DX
EH  97 98 99    49 1.0
EN  0  96 0     50 1.0
* Input offset voltage -
EOS 7  1  POLY(1) 16 49 350U 1
EP  97 0  99    0  1.0
E1  97 19 99    18 1.0
* Sourcing load +Vs current
F1  99 0  VA2   1
* Sinking load -Vs current
F2  0  50 VA3   1
F3  13 0  VA1   1
G1  98 9  5     6  0.1
G2  98 11 9     49 1U
G3  98 15 11    49 1U
* DC CMRR
G4  98 16 POLY(2) 1 49 2 49 0 1.26E-8 1.26E-8
G5  98 18 15    49 1U
I1  99 4  33.46U
I2  99 50 366.5U
* Load dependent pole
L1  22 28 80.4U
* CMR lead inductor
L2  16 17 73.1M
* 3.30 MHz lead inductor
L3  98 3  48.2M
M1  5  2  4     99 MX
M2  6  7  4     99 MX
R3  5  50 5.18K
R4  6  50 5.18K
R5  98 9  1E7
```

```
R8   99 49 50K
R9   49 50 50K
R10 18 3  1E6
R12 98 11 1E6
R13 98 17 1K
* -Rout
R16 23 24 70.7
* +Rout
R17 23 25 80.3
* +Isc slope control
R18 20 29 64K
* -Isc slope control
R19 21 30 130K
R21 98 15 1E6
R22 22 28 636
VA1 19 23 0V
VA2 14 13 0V
VA3 13 12 0V
V2   97 8  0.713V
V3   10 96 0.710V
V4   29 22 1.170V
V5   22 30 0.63V
V6   26 22 0.63V
V7   22 27 0.63V
.MODEL  DA D     (IS=2.5E-14)
.MODEL  DB D     (IS=2.0E-14)
.MODEL  DX D     (IS=1.0E-14)
.MODEL  MX PMOS (VTO=-2.456 KP=7.0547E-4)
.ENDS

.end
```

# Vita

# Vita

Jason Michael Vann was born in Oak Ridge, Tennessee on February 12, 1975. He attended Roane County public schools where he graduated with honors from Oliver Springs High School in May, 1993. After graduation, Michael entered the University of Tennessee, Knoxville in August, 1993 with the assistance of the Herbert S. Walters' scholarship and a National Merit Special Scholarship. While an undergraduate, he was involved with several organizations including Tau Beta Pi, IEEE, and the Robot Car Competition Team. He began work as a intern with the Monolithic Systems Development Group in the Instrumentation and Controls Division of Oak Ridge National Laboratories (ORNL) in May, 1996. After graduating Summa Cum Laude with a Bachelor of Science Degree in Electrical Engineering in August, 1997, he continued his work at ORNL as a graduate student in the joint UT-ORNL graduate program in Mixed Signal-VLSI design. He graduated with a Master of Science degree with a major in Electrical Engineering in August, 1998. In addition, Michael also enjoys reading, politics, all types of sports, and spending time with his wife.