To the Graduate Council:

I am submitting herewith a thesis written by David M. Binkley entitled "A Low Noise 45-75 MHz Phase-Locked Loop Frequency Synthesizer For A High Performance Communications Receiver." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

T. Vaughn Blalock

T. Vaughn Blalock, Major Professor

We have read this thesis
and recommend its acceptance:

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Accepted for the Council:

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The Graduate School

A LOW NOISE 45-75 MHz PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER FOR A HIGH PERFORMANCE COMMUNICATIONS RECEIVER

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

David M. Binkley

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DEDICATION

This thesis is dedicated in memory of Oneda Binkley, the mother of my father.

ACKNOWLEDGMENTS

There are so many people who helped me with this work that it is difficult to begin acknowledging them. I begin by thanking Technology for Energy Corporation, my employer, for supporting me in writing this thesis. Also, I want to thank Mike Farmer, Jim Hornkohl, and others with whom I worked with several years ago at Spectron Development Laboratories for the opportunity to design frequency synthesizers.

I would like to thank several well known low noise signal source designers for numerous helpful discussions. Included in this group are Dieter Scherer of Hewlett Packard, Ulrich Rohde of Rohde and Schwarz, and Michael Driscoll of Westinghouse. I also want to thank Hugo Viffian of Hewlett Packard who directed me to Dieter Scherer.

I certainly have to thank Neill Fry who is responsible for getting me interested in communications receivers. Many of the designs in this thesis were first reviewed by Neill during our regular Sunday morning conversations across Tennessee by ham radio.

It is with great sadness that I acknowledge the encouragement and assistance of a great scientist and friend, Bill Managan, who passed away in the final days that I was preparing this thesis. Bill's incredible knowledge of science and zeal for learning were truly remarkable. I am grateful he took such an interest in this thesis.

Finally, I thank George Presley who did the printed circuit board layouts for the synthesizer as a ham radio project for us. And, I want to thank the members of my thesis committee, most notably Dr. Blalock, my major professor, for their guidance and patience while I was working on this thesis.

ABSTRACT

Many modern high performance communications receivers utilize phase-locked loop frequency-synthesized signal sources for driving their mixers to provide excellent tuning accuracy and stability. Phase noise in these synthesizers must be low as it degrades receiver performance due to reciprocal mixing noise. A low noise phase-locked loop frequency synthesizer is described for a 0.1-30 MHz communications receiver. The synthesizer covers 45-75 MHz with 1 kHz channels and features a phase noise of -145 dBc at 20 kHz from the carrier. The excellent noise performance is obtained by using a switched inductor design for the voltage controlled oscillator.

Phase noise theory and measurement is discussed, and a phase noise test set that was used to evaluate the synthesizer noise performance is described. Phase-locked loop theory is discussed with particular emphasis on noise performance. Practical design considerations are also presented. Additionally, oscillator noise theory and design is discussed with particular emphasis on maximizing in-circuit resonator Q and minimizing circuit noise. Phase modulation noise due to active device nonlinearities and low frequency circuit noise is also discussed.

Extensive analysis is provided for the synthesizer, including several computer programs using both the FORTRAN language and the SPICE circuit analysis program. Suggestions are offered for improving the synthesizer design along with suggestions for further research in low noise signal source design.

PREFACE

Low phase noise radio frequency (RF) signal sources are fascinating and challenging electronic circuits to design and build. The design of these circuits involves low noise design techniques at RF frequencies as well as at low frequencies. This forces the designer to be well versed in both low noise RF design and low noise low frequency design. In addition, he must operate somewhat intuitively as circuit nonlinearities greatly complicate the design process by making complete design equations elusive, if not impossible to derive. Further, no design equation will give the designer the circuit topology, which is probably the most important design consideration for low noise signal sources.

It is hoped that this thesis will provide a thorough design discussion for those interested in low noise signal source design and provide useful analysis concepts for all electronic designers. Although the synthesizer described in this thesis is not unique (others similar to it have been built), it is a state-of-the-art unit featuring very low phase noise. The rather extensive analysis of the synthesizer should serve as a starting point for many low noise signal source designs.

Hopefully, the greatest value of this thesis is the fact that it combines in one place many topics of low noise signal source theory and design. These topics include subtleties such as phase modulation noise caused by active device nonlinearities and circuit noise. Finally, the computer programs that are presented will hopefully save the designer many hours of tedious calculations.

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LIST OF ABBREVIATIONS AND SYMBOLS

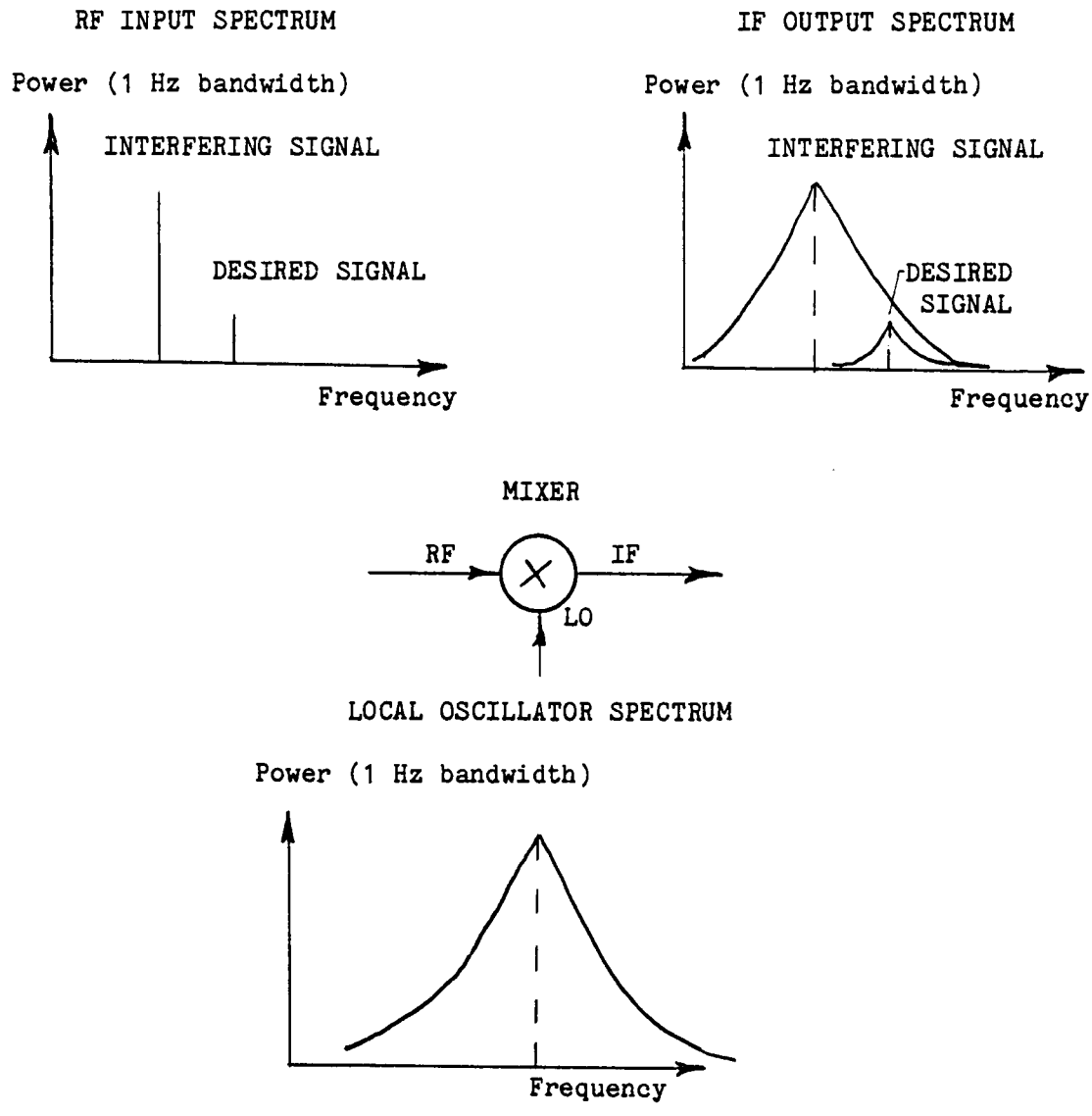
ac	Alternating current
AGC	Automatic gain control
AM	Amplitude modulation
BCD	Binarily coded decimal
CMOS	Complementary symmetry metal oxide semiconductor
DAC	Digital-to-analog converter
dB	Decibel
dBc	Decibels refered to the carrier as measured in 1 Hz band
dBm	Decibels referenced to 1 mW
dc	Direct current
DIP	Dual-in-line
EPROM	Erasable, programmable read-only memory
ECL	Emitter coupled logic
FFT	Fast Fourier transform
f_m	Modulation frequency
FM	Frequency modulation
HF	High frequency
IF	Intermediate frequency
IIL	Integrated injection logic
JFET	Junction field effect transistor
K_ϕ	Phase detector gain
K_V	Voltage controlled oscillator gain
$L(f_m)$	Single sideband phase noise (in dBc)
LC	Inductor-capacitor
LO	Local oscillator
LRC	Inductor-resistor-capacitor
LSTTL	Low power Schottky transistor-transistor logic
MOS	Metal oxide semiconductor
N	Phase-locked loop frequency divider ratio
pk	Peak
PLL	Phase-locked loop
PM	Phase modulation
Q	Quality factor
rad	Radian
RF	Radio frequency
rms	Root-mean-square
s	Complex frequency variable
SPICE	Simulation program with integrated circuit emphasis
$S_\phi(f_m)$	Phase noise spectral density ($rads^2/Hz$)
$S_f(f_m)$	Frequency noise spectral density (Hz^2/Hz)
$S_y(f_m)$	Fractional frequency noise spectral density (/Hz)
SSB	Single sideband
TTL	Transistor-transistor logic
UHF	Ultra high frequency
VCO	Voltage controlled oscillator
VHF	Very high frequency
1/f	Denotes low frequency noise characteristic

1. INTRODUCTION

Application Of Low Phase Noise Signal Sources

Phase noise describes the random phase fluctuations in an oscillator from the ideal signal phase. Low phase noise signal sources are required in many RF and microwave systems. For instance, phase shift or frequency shift keyed systems used to transmit digital data over RF and microwave carriers require signal sources with low phase noise. Phase noise or phase jitter can obscure the signal modulation, raising the bit error rate in these systems.[1] Doppler radar systems, which measure extremely small frequency shifts caused by a moving target, also require low phase noise signal sources.[2] Probably the greatest use of low phase noise signal sources is for local oscillators in superheterodyne receivers. Local oscillator phase noise must be low to minimize the effects of reciprocal mixing noise.

Reciprocal mixing noise degrades receiver sensitivity and selectivity. This occurs because incoming signals are mixed with the local oscillator carrier signal, and unfortunately, with its phase noise induced sidebands. The mixer output contains the desired frequency converted input signals except that these signals now have noise sidebands similar to those of the local oscillator. When receiving a signal close in frequency to a larger interfering signal, the noise sidebands of the larger signal may completely obscure the desired signal at the mixer output.[3] This effect is shown in Figure 1.1.



Note that the noisy local oscillator spectrum is transferred to the IF output. The noise sidebands of the interfering signal completely obscure the desired signal at the mixer IF output.

Figure 1.1. Effects of Reciprocal Mixing Noise in a Receiver.

Reciprocal mixing noise effects can be characterized in two ways. First, an imperfect local oscillator spectrum (a widened spectrum due to phase noise) degrades receiver selectivity. Receiver selectivity is often controlled by oscillator phase noise instead of by the intermediate frequency (IF) amplifier. If this is the case, the IF filter requirements can be relaxed as local oscillator phase noise effectively widens the IF filter.[4,5]

The second way of characterizing reciprocal mixing noise is to evaluate the noise floor or noise figure of a receiver when strong out-of-band signals are present at its input. Consider, for example, a receiver with a noise figure of 10 dB, a local oscillator single sideband (SSB) phase noise of -120 dBc at 100 kHz from the carrier (this specification will be discussed in Section 2) with a -20 dBm input 100 kHz away from the passband frequency. The effective noise floor of the receiver will be raised by the interfering -20 dBm signal.[1]

The receiver front-end noise floor in a 1 Hz bandwidth is

$$P_n = -174 \text{ dBm/Hz} + 10 \text{ dB} = -164 \text{ dBm/Hz}, \tag{1.1}$$

where -174 dBm/Hz is the thermal resistance noise power in a 1 Hz bandwidth at room temperature. The noise floor (in a 1 Hz bandwidth) due to reciprocal mixing noise is

$$P_{rm} = -120 \text{ dBc} - 20 \text{ dBm} = -140 \text{ dBm/Hz}. \tag{1.2}$$

Thus, the overall noise floor of the receiver is dominated by reciprocal mixing noise and is approximately -140 dBm/Hz or 24 dB higher than

the noise contribution of the receiver front-end. In summary, the receiver noise floor increases by 24 dB when a -20 dBm interfering signal is present 100 kHz from the passband. If the local oscillator SSB phase noise were -160 dBc at 100 kHz from the carrier, the receiver's noise floor contribution due to reciprocal mixing noise would be only -180 dBm/Hz. This is negligible compared to the front-end noise, meaning the receiver noise floor would not increase when the -20 dBm interfering signal was present.

It should be clear that high performance, high dynamic range receivers require low phase noise local oscillators as these receivers nearly always have strong interfering signals present at their inputs. In the following discussion, phase noise requirements are presented for the 45-75 MHz frequency synthesizer that was designed for a high performance receiver local oscillator.

Design Requirements For The Frequency Synthesizer

The frequency synthesizer discussed is to be used as the first local oscillator in a 0.1-30 MHz high performance communications receiver. The receiver's first IF is at 45 MHz, making the required tuning range of the synthesizer 45.1-75 MHz. Channel steps of 1 kHz are satisfactory for the synthesizer since finer receiver tuning will be accomplished using the second local oscillator. The second local oscillator will be a narrow range frequency synthesizer with 10 Hz channel spacings and will use a voltage controlled crystal oscillator. Only the 45-75 MHz first local oscillator synthesizer is discussed.

A PLL type of synthesizer was chosen because of its simplicity, low cost, and low spurious outputs compared to direct crystal synthesizers that mix different frequencies to synthesize output frequencies. A hybrid frequency synthesizer approach using both direct crystal synthesis and PLL synthesis would be superior, as it features fast switching speeds and low phase noise. This is because direct crystal synthesizers switch very rapidly, even if they have very narrow channel spacings. However, their high spurious output levels require that they be followed by a PLL synthesizer, which inherently has low spurious output levels. The PLL synthesizer may be wideband since the fine frequency channel spacing is generated in the crystal synthesizer. The result is low phase noise and high microphonic noise rejection, as the wideband PLL minimizes both internally and externally generated phase noise perturbations. The hybrid system also switches rapidly.

Several commercial synthesizers use both crystal synthesis and PLL synthesis, with probably the most outstanding example being the Hewlett Packard HP-8662A Synthesized Signal Generator.[6] Unfortunately, such a system is far too expensive to use in a communications receiver for the short-wave listener or ham radio operator.

Phase noise is the most important design parameter of the 45-75 MHz synthesizer because of reciprocal mixing noise. Phase noise requirements were derived by researching state-of-the-art frequency synthesizers for communications receivers. Rohde discusses a synthesizer for receiver local oscillators that has SSB phase noise of -90-100 dBc at 1 kHz from the carrier and -140 dBc at 20 kHz from the

carrier.[7] In his recently published synthesizer book (8, p. 353), he presents a 41-71 MHz synthesizer design with a SSB phase noise of better than -125 dBc at 25 kHz from the carrier. The Racal Company provides yet another example. The synthesized local oscillator in the Racal RA1772 receiver, an excellent high frequency communications receiver, has SSB phase noise of -135 dBc at 20 kHz from the carrier.[5]

A tabular presentation of the design specifications for the 45-75 MHz synthesizer presented in this thesis is given in Table 1.1. A range is given for the phase noise specification covering good to exceptional performance.

Table 1.1. Design Specifications for the 45-75 MHz Synthesizer.

Parameter	Specification
Frequency range	45-75 MHz
Channel spacing	1 kHz
Lock time	0.2 seconds max.
Power requirements	+24 V, -24 V, +5 V less than 2 W max.
Output level	+10 dBm into 50 ohms
Frequency programming	BCD coding, 5 V CMOS levels
Phase noise	
at 1 kHz	-90-100 dBc
at 20 kHz	-125-140 dBc
ultimate floor	-150-160 dBc
Reference frequency sidebands	first sidebands over 80 dB down other sidebands over 100 dB down
Spurious outputs	over 100 dB down
Cost	below $150.00

Organization Of Thesis

This thesis contains general theory and analysis as well as analysis of the 45-75 MHz synthesizer. Section 2 contains a description of phase noise and methods of quantifying and measuring it. Section 3 contains descriptions and a general analysis of phase-locked loops with special emphasis on the second-order system. Also included is a noise analysis including low noise design strategies. The section concludes with a brief discussion of PLL circuit elements.

Section 4 contains oscillator noise theory and low noise design approaches. Both crystal and LC oscillators are discussed with design emphasis on maximizing in-circuit resonator Q and minimizing circuit noise. The effects of both low frequency and RF device noise are covered. Section 5 contains a presentation of the voltage controlled oscillator in the 45-75 MHz synthesizer. Attention is directed primarily to its noise performance, and a computer program is presented to analyze its switched inductor tank circuit.

Section 6 contains a presentation of the 45-75 MHz synthesizer design, analysis, and experimental measurements. The loop amplifier/filter, loop frequency divider, and reference frequency oscillator are discussed in detail, and computer programs are presented that greatly simplify the analysis. Actual synthesizer performance is compared to the design specifications. Section 7 contains suggestions for improving the synthesizer and suggestions for further theoretical and experimental work in low noise signal source design.

Finally, the appendixes contain computer program listings for programs used in the synthesizer analysis, as well as a description of

the phase noise test set that was used to measure the synthesizer phase noise.

2. PHASE NOISE THEORY AND MEASUREMENT

Description Of Phase Noise

Long-term frequency or phase instability refers to frequency or phase instability measured over a long period of time, typically greater than several seconds. Crystal oscillator aging and other slow frequency drifts in oscillators are examples of long-term phase instability. Long-term phase instability does not contribute to reciprocal mixing noise; instead it causes a receiver to drift slowly off frequency with time.

Short-term phase (or frequency) instability refers to phase (or frequency) instability measured over a short period of time, typically less than one second. Short-term instability will be discussed in this thesis as it is responsible for reciprocal mixing noise in receivers.

Consider the output signal of an oscillator. Mathematically the output voltage can be represented as

$$V_{out}(t) = V_0[1 + e(t)]\cos[\, 2\pi f_0 t + \emptyset(t)\,]. \quad [9,10,11] \qquad (2.1)$$

The function e(t) describes amplitude fluctuations with time. Fortunately, amplitude limiting inherent in oscillators causes amplitude fluctuation effects to be negligible. Further, since most mixers are operated in a saturated mode, amplitude fluctuations are even further reduced in local oscillator applications.[9]

The term $2\pi f_0$ refers to linearly increasing phase with time, f_0 being the carrier frequency in Hz. The term $\emptyset(t)$ represents phase

fluctuation with time. If $\phi(t) = 0$, the oscillator signal would have no phase noise and would have an infinitely narrow power spectrum. In reality, $\phi(t)$ is a zero mean noise signal that causes the oscillator signal to have a finite width power spectrum. Both the noiseless and noisy signals are shown in Figure 2.1 along with their corresponding power spectra.

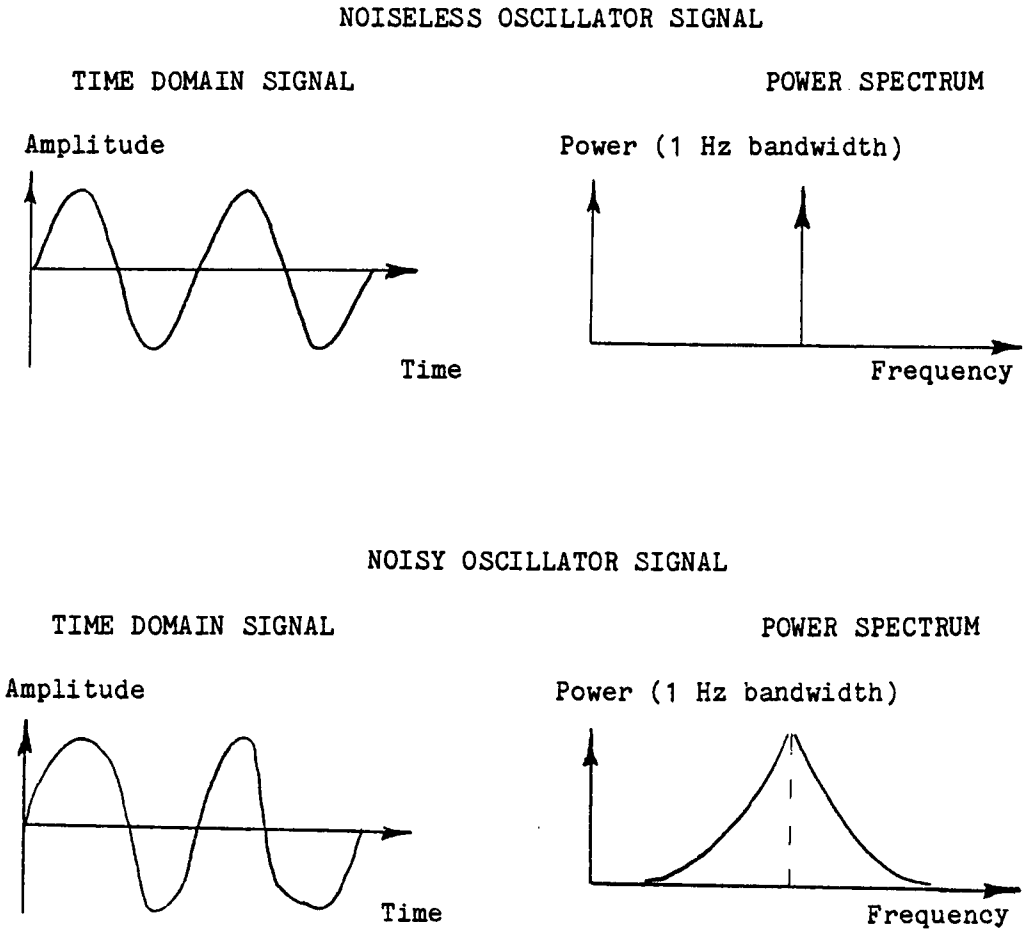


Figure 2.1. Noiseless and Noisy Oscillator Signals.

Quantization Of Phase Noise

Signal Power Spectrum

The phase noise of a signal may be characterized by the signal's power spectrum. This is the type of spectrum displayed on a spectrum analyzer where oscillator power in a fixed bandwidth (often normalized to 1 Hz) is plotted as a function of frequency. It is very difficult to measure low phase noise with a spectrum analyzer since most practical spectrum analyzers have local oscillators that are much noisier than the signal under test. For this reason, power spectrum specifications are rarely used. However, the SSB phase noise specification is very similar to the power spectrum and is widely used. This specification will be discussed later.

Phase Noise Spectral Density

Recall from Equation 2.1 that phase noise is denoted by $\phi(t)$. Since $\phi(t)$ is a noise signal, it may be represented by a spectral density just as a noise voltage or current. Phase noise spectral density is designated by $S_{\phi}(f_m)$ and has units of radians^2/Hz.[9,10,11] It is the mean square phase noise measured in a 1 Hz bandwidth at the frequency f_m. The frequency f_m is called the Fourier frequency, offset frequency, modulation frequency, baseband frequency, or sideband frequency.[6] All of these are identical, but for consistency, modulation frequency (denoted f_m) will be used in this thesis.

Phase noise spectral density is easily directly measured, but is usually converted to SSB phase noise as will be described later. However, phase noise spectral density is directly useful when

analyzing phase modulated systems. It is also usually calculated in oscillator analysis directly and again later converted to SSB phase noise.

Frequency Noise Spectral Density

Phase and frequency modulation are intimately related as frequency is the time derivative of phase. Similarly, frequency noise is related to phase noise in an oscillator. Frequency noise describes the random frequency shifts of an oscillator as a function of time. It is represented by the spectral density function $S_f(f_m)$ and has units of Hz^2/Hz.[9,10,11] $S_f(f_m)$ is the mean square frequency shift from the carrier measured in a 1 Hz bandwidth at the frequency f_m.

Frequency noise spectral density can be related to phase noise spectral density. This relationship is valuable because phase noise spectral density is generally a more practical phase noise specification. Again, an oscillator's output voltage can be represented by

$$V_{out} = V_0 \cos[\, 2\pi f_0 t + \phi(t) \,], \qquad (2.2)$$

where f_0 is the carrier frequency in Hz, V_0 is the peak signal amplitude, and $\phi(t)$ is the phase noise. The instantaneous frequency is

$$f(t) = (1/2\pi)\, d/dt\, [\, 2\pi f_0 t + \phi(t) \,]$$

$$= f_0 + (1/2\pi)\, d/dt\, [\, \phi(t) \,] \quad (Hz). \qquad (2.3)$$

Defining the frequency deviation from the carrier as $f_f(t)$ gives

$$f_f(t) = f(t) - f_0$$

$$= (1/2\pi)d/dt\ [\ \phi(t)\ ] \quad \text{(Hz)}. \tag{2.4}$$

Taking the Laplace transform of both sides of the equation gives

$$F_f(s) = (s/2\pi)\phi(s). \tag{2.5}$$

Finally, squaring both sides gives

$$F_f^2(s) = (s/2\pi)^2\phi^2(s), \tag{2.6}$$

from which the spectral densities are derived:

$$S_f(f_m) = (2\pi f_m/2\pi)^2 S_\phi(f_m)$$

$$= f_m^2 S_\phi(f_m) \quad \text{(Hz}^2\text{/Hz)}.^{10} \tag{2.7}$$

From this relationship, it is clear that a flat phase noise spectrum is equivalent to a frequency noise spectrum that increases at 6 dB/octave. Frequency noise spectral density can be a very misleading specification because it varies directly with the oscillator carrier frequency, making a higher frequency oscillator appear much noisier than a lower frequency one. For this reason, the National Bureau of Standards proposed a fractional frequency noise density, which is simply a normalized frequency noise density. It is denoted by $S_y(f_m)$ and is related to frequency and phase noise spectral densities by

$$S_y(f_m) = (1/f_0)^2 S_f(f_m) = (f_m/f_0)^2 S_\phi(f_m) \quad \text{(1/Hz)}.^{10} \tag{2.8}$$

Fractional frequency noise spectral density is independent of carrier

frequency, allowing comparison of different oscillators. It has units of mean square fractional frequency deviation measured in a 1 Hz bandwidth.

Single Sideband Phase Noise

Probably the most widely used phase noise specification is SSB phase noise. SSB phase noise is denoted by $L(f_m)$ and has units of dBc (decibels from the carrier).[9,10,11] It is the ratio of signal power in a 1 Hz bandwidth at a frequency f_m away from either side of the carrier frequency to the total signal or carrier power. $L(f_m)$ describes the signal spectrum on only one side of the carrier, as the spectrum on the other side is a mirror image. This is shown pictorially in Figure 2.2 along with the definition of $L(f_m)$. It must be remembered that $L(f_m)$ can only be used to describe signals with a power spectrum that is symmetrical about the carrier frequency. This requirement is met if the signal has negligible amplitude modulation noise, which, as described earlier, is a generally valid assumption for oscillators.

SSB phase noise may be related to phase noise spectral density through frequency modulation (FM) theory. This is useful since phase noise spectral density is often measured directly and then converted to SSB phase noise.

Consider a frequency modulated signal with an instantaneous frequency

$$f(t) = f_0 + f_p \cos 2\pi f_m t, \tag{2.9}$$

where f_0 is the carrier frequency, f_p is the peak deviation from the

carrier, and f_m is the modulation frequency.[6] The total signal phase is

$$\Phi(t) = 2\pi \int_0^t f(t)dt$$

$$= 2\pi \int_0^t [\, f_0 + f_p \cos 2\pi f_m t \,]dt$$

$$= 2\pi f_0 t + (f_p/f_m)\sin 2\pi f_m t. \qquad (2.10)$$

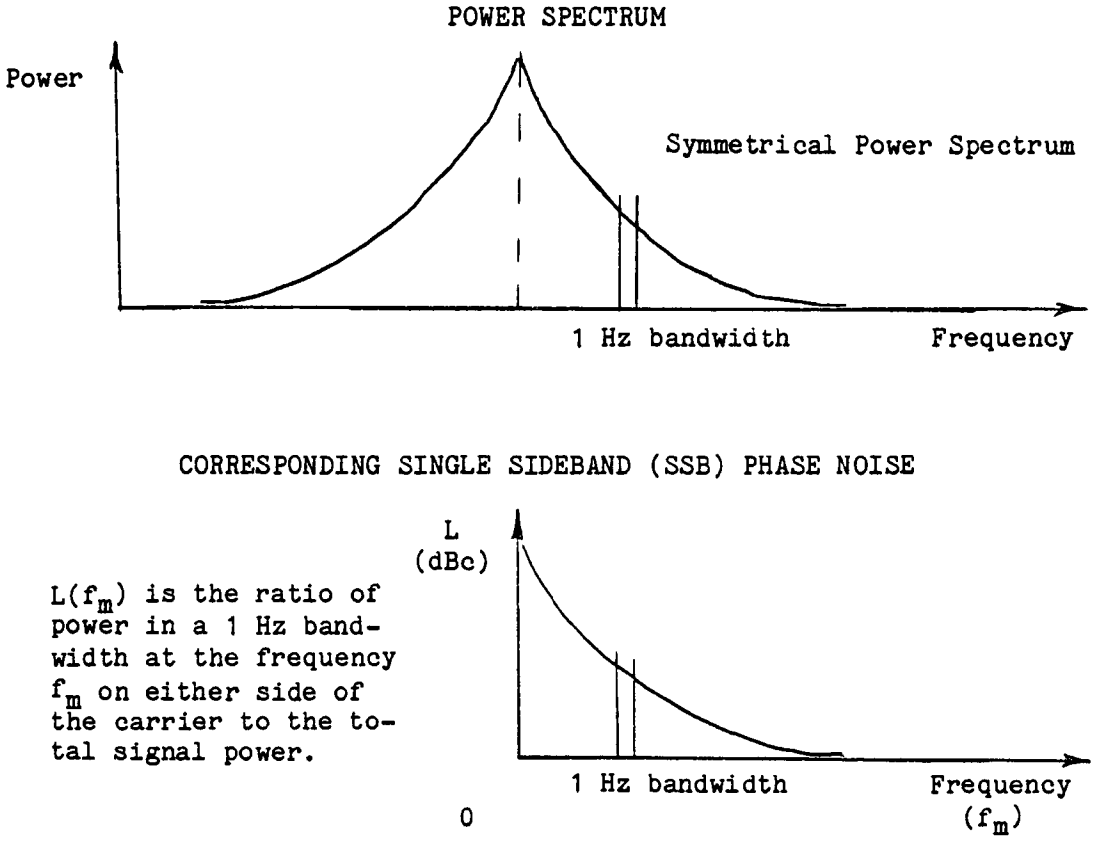


Figure 2.2. Definition of SSB Phase Noise.

The oscillator signal is then

$$V_{out}(t) = V_0 \cos[\, \Phi(t) \,]$$

$$= V_0 \cos[\, 2\pi f_0 t + (f_p/f_m)\sin 2\pi f_m t \,], \qquad (2.11)$$

where f_p/f_m is the FM modulation index as well as the peak phase deviation. This signal may be rewritten to illustrate its spectrum using trigonometric expansions, and is given by

$$\begin{aligned} V_{out}(t) = \; & V_0 J_0(\emptyset_p)\cos 2\pi f_0 t \\ & + V_0 J_1(\emptyset_p)[\, \cos 2\pi(f_0+f_m)t - \cos 2\pi(f_0-f_m)t \,] \\ & + V_0 J_2(\emptyset_p)[\, \cos 2\pi(f_0+2f_m)t + \cos 2\pi(f_0-2f_m)t \,] \\ & + V_0 J_3(\emptyset_p)[\, \cos 2\pi(f_0+3f_m)t - \cos 2\pi(f_0-3f_m)t \,] \\ & + \cdots\cdots\cdots , \end{aligned} \qquad (2.12)$$

where $\emptyset_p = f_p/f_m$, which is the peak phase deviation or modulation factor, and J_0, J_1 etc. are Bessel functions of the first kind. A derivation of this expression is given by Krauss (12, pp. 263-265).

If $\emptyset_p$ is much less than one, then $J_0(\emptyset_p) = 1$, $J_1(\emptyset_p) = 0.5\emptyset_p$, and all the Bessel functions of order greater than one are equal to zero. Under this assumption, the ratio of the first (and only) FM sidebands to the carrier is

$$V_{ssb}/V_0 = J_1(\emptyset_p)/J_0(\emptyset_p)$$

$$= (1/2)\emptyset_p. \qquad (2.13)$$

Squaring both sides of the equation gives the SSB to carrier power ratio, which is

$$(V_{ssb}/V_0)^2 = (1/4)\phi_p^2. \tag{2.14}$$

Converting ϕ_p to rms units gives

$$\phi_p = \sqrt{2}\phi_{rms}, \tag{2.15}$$

which gives

$$(V_{ssb}/V_0)^2 = (1/2)\phi_{rms}^2. \tag{2.16}$$

This conversion is necessary because spectral densities must be denoted in mean square units. Finally, the corresponding spectral density functions are

$$L(f_m) = (1/2)S_\phi(f_m).^6 \tag{2.17}$$

The spectral densities may also be expressed in logarithmic (dB) form, giving

$$L(f_m) = S_\phi(f_m) - 3\ \text{dB}$$

$$\text{(dBc)} \qquad \text{(dB rel to 1 rad}^2\text{/Hz)}. \tag{2.18}$$

The relationship between SSB phase noise and phase noise spectral density is simply a scale factor, as shown above. The assumption of $\phi_p << 1$ is extremely important because of the Bessel function approximations that were made. In practice, the peak phase deviation is much less than one radian, making the assumption a valid one.

Summary of Phase Noise Relationships

The relationships between SSB phase noise, phase noise spectral density, and frequency noise spectral density are listed below:

$$L(f_m) = (1/2)S_\phi(f_m) = (1/2)(1/f_m)^2 S_f(f_m). \qquad (2.19)$$

The slope of $S_\phi(f_m)$, and likewise $L(f_m)$, is used to characterize phase noise power law mechanisms. Different names are given to phase noise to describe the slope of $S_\phi(f_m)$ or $L(f_m)$. These are listed below:[11]

- White phase noise where $S_\phi(f_m)$ is flat with frequency.
- Flicker phase noise where $S_\phi(f_m)$ goes down as $1/f_m$ (10 dB/decade).
- White FM noise where $S_\phi(f_m)$ goes down as $1/f_m^2$ (20 dB/decade).
- Flicker FM noise where $S_\phi(f_m)$ goes down as $1/f_m^3$ (30 dB/decade).
- Random walk FM noise where $S_\phi(f_m)$ goes down as $1/f_m^4$ (40 dB/decade).

The slope of $S_\phi(f_m)$ is described by the above defined names, the exponent or power of the frequency dependence, or by the slope in dB/decade. These descriptions are frequently used interchangeably in the literature.

Measurement Of Phase Noise

Signal Power Spectrum Measurements

A signal's power spectrum is displayed, as mentioned, on a spectrum analyzer where power in a fixed bandwidth (usually normalized to 1 Hz) is measured at various frequencies. However, since many state-of-the-art signal sources have an ultimate phase noise floor of -160 dBc or more, the spectrum analyzer must have a dynamic range of

160 dB or more. For this reason, direct power spectrum measurement is rarely used for phase noise measurements. Spectrum analyzers are, however, very useful for checking for spurious outputs that occur well away from the carrier.

Frequency Noise Measurements

Another method of measuring phase noise is to measure signal frequency fluctuations and use the mathematical relationships between frequency noise spectral density, phase noise spectral density, and SSB phase noise. Frequency fluctuations are measured using a frequency discriminator which produces a voltage that is linearly proportional to instantaneous signal frequency. Cavity, crystal, and delay line discriminators are commonly used for this purpose.[6] A block diagram of a frequency noise spectral density test set is shown in Figure 2.3. Note that the discriminator output goes to a low frequency spectrum analyzer to measure the spectral density.

Frequency noise measurements may be improved by heterodyning a low noise oscillator with the test oscillator. This results in a lower frequency signal that has greater FM noise modulation. Unfortunately, because frequency noise increases by 6 dB/octave with increasing frequency for flat phase noise, a frequency discrimination system is not very sensitive at modulation frequencies above 1 kHz.[13] A measurement system noise floor of -115 dBc at 1 kHz from the carrier has been reported.[6]

Phase Noise Measurements by Comparing Two Oscillators

A reference oscillator of low phase noise may be compared to an

oscillator under test using a phase detector. To do this, the two signals must track each other in long-term phase quadrature. Under this condition, the phase detector output is a noise voltage signal that represents the phase fluctuations between the two oscillators. Because of normal oscillator drifts with temperature and time, some method of forcing the reference oscillator to track the signal under test is required. This is done by using a "loose" phase-locked loop.

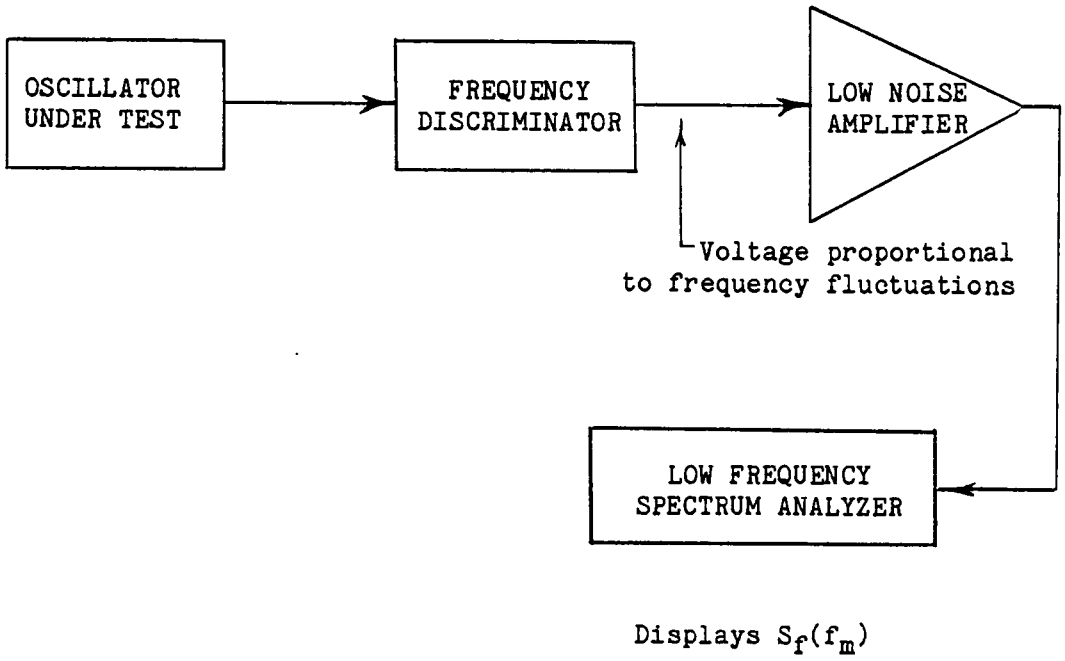


Figure 2.3. Frequency Noise Test Set Using a Discriminator.

"Loose" implies that the loop's bandwidth is low, typically 1-10 Hz, so that phase noise at frequencies above this is not tracked by the reference oscillator and thus cancelled out at the phase detector output. A block diagram of this type of phase noise measurement system is shown in Figure 2.4.

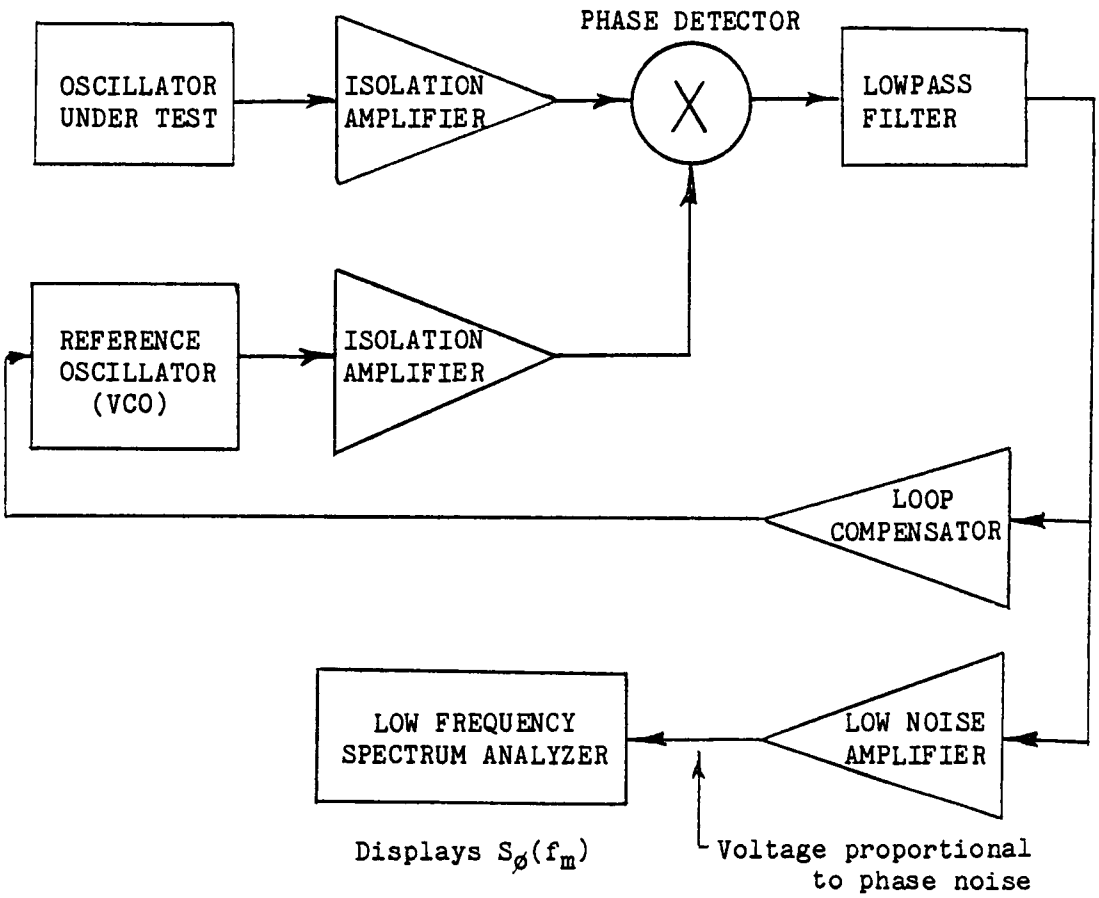


Figure 2.4. Phase Noise Test Set Using Two Oscillators and a Phase Detector.

Since the output of the phase detector is directly proportional to the phase difference between the reference oscillator and signal under test, a direct measurement of phase noise is made. However, there are a number of very critical practical considerations. For example, the reference phase noise must be known and subtracted from the measurement.[14] Also, a high gain phase detector is required to achieve a low phase noise floor.[15,16] Further, the reference oscillator must be isolated from the oscillator under test, or these oscillators will tend to injection lock to each other, resulting in overly optimistic (and erroneous) phase noise measurements.[15,16]

The two oscillator phase noise measuring system using a phase detector is optimum except when measurements very close to the carrier (low f_m) are required. Phase noise measurements of -166 dBc at 1 kHz and a phase noise floor of -180 dBc have been reported in the literature.[6,15]

The phase noise test set used for evaluating the 45-75 MHz synthesizer is this type of circuit. It is described in detail in Appendix D and has an ultimate phase noise floor of -165 dBc.

Time Domain Measurements

So far, the discussion of phase noise quantification and measurement has involved frequency domain techniques. Phase noise, however, may be measured in the time domain. Generally, time domain measurements are used for close-in phase noise measurements. Time domain measurements are made using period counters which measure the slightly differing periods of successive cycles. A parameter known as the Allan variance is usually calculated and other phase noise

specifications are then calculated from it.[6] Time domain measurements may be improved by heterodyning a reference oscillator with the oscillator under test to create a lower frequency signal with larger period variations. Of course, the reference oscillator should have equal or lower phase noise than the oscillator under test to prevent introducing serious error.

Time domain measurements are not used in this thesis for characterizing the phase noise of the 45-75 MHz synthesizer. The reader is referred to References 9,17,18, and 19 for a thorough discussion of time domain measurement theory, measurement circuits, and mathematical relationships to phase noise spectral density and SSB phase noise.

Effects Of Frequency Multiplication And Division On Phase Noise

The phase noise of a signal is altered if the signal is frequency multiplied or divided. Since frequency multiplication and division are frequently used in communications systems, the effects of a noiseless frequency multiplier or divider on the phase noise of a signal are important. The effects of noise within the frequency multiplier or divider must be considered separately.

Consider once again the output signal of an oscillator, which can be represented as

$$V_{out} = V_0 \cos[\, 2\pi f_0 t + \emptyset(t)\,]. \qquad (2.20)$$

This signal can be represented as

$$V_{out} = V_0 \cos K[\, 2\pi f_0 t + \emptyset(t)\,] \qquad (2.21)$$

after passing through a noiseless frequency multiplier or divider with a multiplication factor of K. Rewriting this expression gives

$$V_{out} = V_0 \cos[\, 2\pi K f_0 t + K\emptyset(t)\,], \qquad (2.22)$$

where it can be seen that both the carrier frequency and phase noise are multiplied by the factor K. Thus, frequency multiplication increases phase noise by the amount of the multiplication, and frequency division improves phase noise by the amount of the division. Frequently, a signal source will be designed by dividing down a higher frequency oscillator to improve phase noise.

3. PHASE-LOCKED LOOP THEORY AND DESIGN

Description Of Phase-Locked Loops

A phase-locked loop is a feedback circuit that generates an output frequency that is synchronized to its input frequency. A PLL is like other feedback circuits except that its input and output signals are phase instead of voltage or current.[20]

A PLL consists of a phase detector to compare input phase against feedback phase, a loop amplifier/filter to control the frequency response and stability of the loop, a voltage controlled oscillator (VCO) to generate the output signal, and a loop frequency divider in the feedback path. A block diagram of the simple single loop PLL is shown in Figure 3.1.

In a PLL, feedback forces a finite phase difference to appear between the inputs of the phase detector. From the block diagram of Figure 3.1, this means that the input frequency (f_{in}) and the feedback frequency (f_{fbk}) must be equal. Since the feedback frequency is equal to f_{out}/N, where N is the loop frequency divider ratio, the output frequency must equal the input frequency multiplied by N. Mathematically stated,

$$f_{out} = Nf_{in}. \tag{3.1}$$

A PLL accomplishes phase-locking because the phase detector outputs an error voltage proportional to the phase difference between the input and feedback signals. This error voltage steers the VCO frequency so that phase-locking or frequency synchronization occurs.

PLLs have two main applications: frequency synthesis and frequency tracking.[20] For frequency synthesis, the input frequency is fixed and called the reference frequency. The PLL generates one or more output frequencies by varying the loop divider ratio, N. For frequency tracking, the loop divider ratio is fixed, and the input signal varies in frequency. The tracking loop tracks the input frequency and produces a voltage that is proportional to the input frequency at the VCO input. The PLL frequency demodulator is an example of a tracking loop. Only synthesis type loops are considered in this thesis, but the analysis of both loop types is identical.

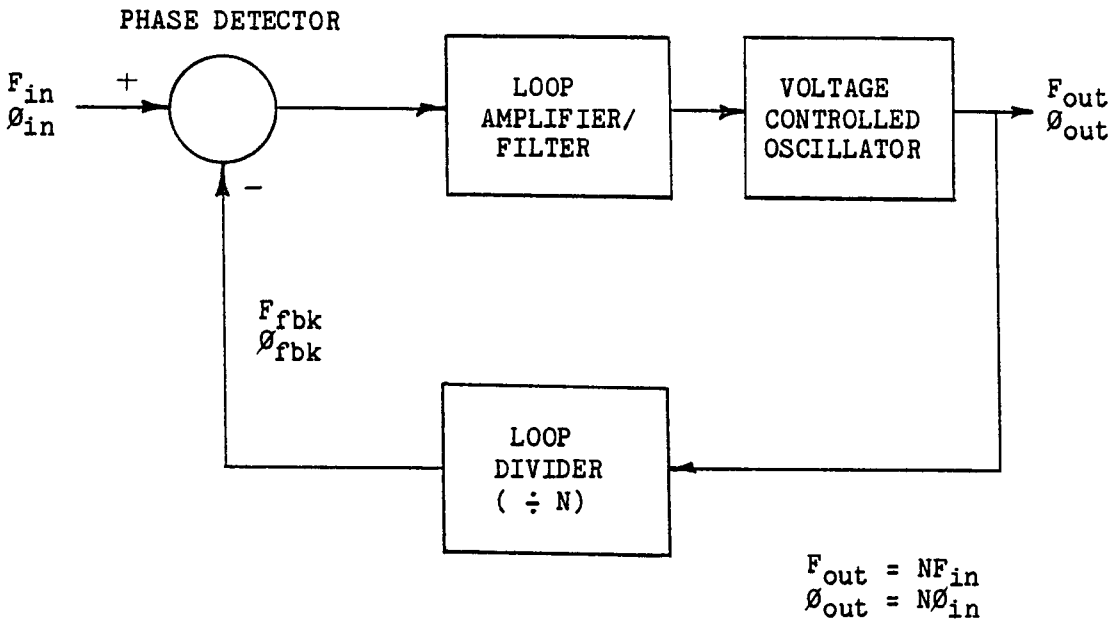


Figure 3.1. Single Loop Phase-Locked Loop.

Stability, Frequency, And Transient Response

Analysis Model

Since PLLs are feedback circuits, they can potentially become unstable. A block diagram for PLL Laplace transform analysis is shown in Figure 3.2.

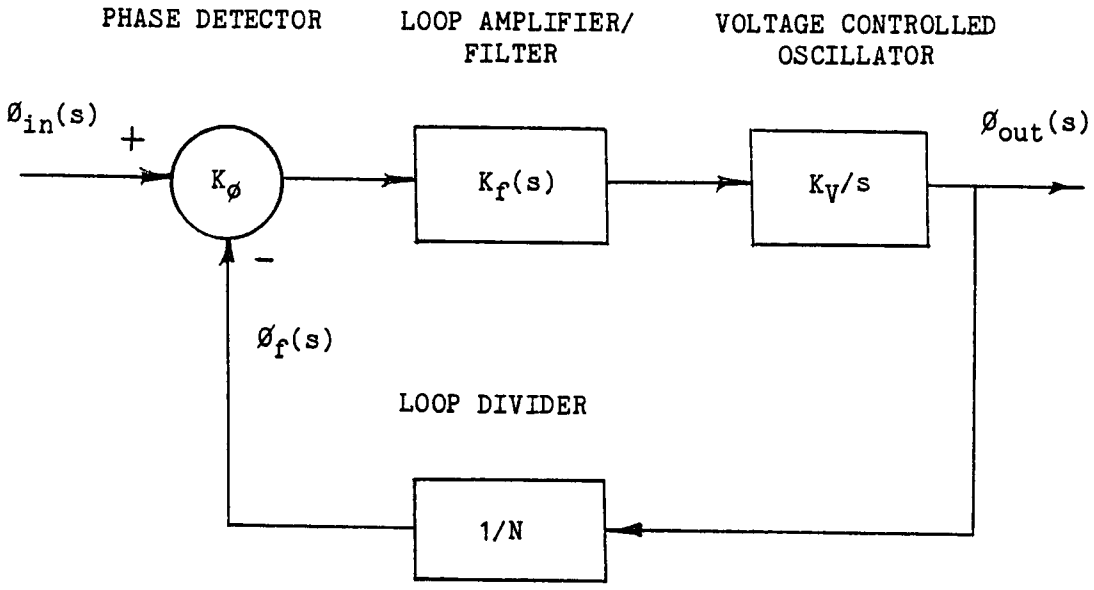


Figure 3.2. Model for Phase-Locked Loop Laplace Transform Analysis.

The PLL parameters, as shown in Figure 3.2, are defined below:

- K_{ϕ} is the phase detector gain and has units of volts/radian.
- $K_f(s)$ is the amplifier/filter transfer gain.
- K_V is the VCO gain and has units of radians/volt sec.
- N is the loop divider ratio and has units of radian/radian.

Note that the VCO is a pure phase integrator because a steady dc input results in a constant output frequency or constant linearly increasing phase. Additionally note that the loop divider transfer function (1/N) is a simplification because in reality the loop divider has a finite delay time associated with it. The actual transfer function is $e^{-ts}(1/N)$. This effect is negligible if the delay is significantly less than the loop input signal period.[21] PLL analysis including the loop divider delay is presented by Fadrhons in Reference 22.

General Feedback Analysis

Using the previously described model, PLL loop gain is given by

$$T = -K_{\phi}K_f(s)K_V/(sN), \tag{3.2}$$

and the feedback factor B, is given by

$$B = \phi_f/\phi_{out} = 1/N. \tag{3.3}$$

From feedback theory, the closed loop gain is

$$A_{cl} = \phi_{out}/\phi_{in} = (1/B)[\ -T/(1-T)\ ]. \tag{3.4}$$

Substituting the expression for T into this equation gives

$$A_{cl} = \phi_{out}/\phi_{in} = N\,[\,K_\phi K_f(s)K_V/(sN)\,]\,/\,[\,1 + K_\phi K_f(s)K_V/(sN)\,]. \quad (3.5)$$

The phase error appearing between the phase detector inputs is important in finding the output error of the PLL. Phase error is given by

$$\phi_{error}/\phi_{in} = (\phi_{in}-\phi_f)/\phi_{in} = 1/(1-T) = 1/[1 + K_\phi K_f(s)K_V/(sN)]. \quad (3.6)$$

The PLL output phase error is then

$$\phi_{out\ error} = -N\phi_{error} = -N\phi_{in}\,[\,1/(\,1 + K_\phi K_f(s)K_V/(sN)\,)\,]. \quad (3.7)$$

These equations serve as a basis for PLL analysis and are valid for a system of any order. Later, the second-order PLL will be discussed.

Loop Stability and Compensation

Before progressing on, it is necessary to study the stability of the PLL. At first glance, it would appear that PLLs are inherently stable if the loop amplifier/filter has no frequency dependency. The loop gain would then have a constant 90 degree phase lag due to the integrating behavior of the VCO. However, practical considerations force the loop amplifier/filter to be a lowpass filter to minimize reference frequency ripple coming out of the phase detector. This ripple will modulate the VCO, causing severe frequency or phase jitter.

A lag-lead type compensation network is often used for the loop amplifier/filter. This network provides both lowpass filtering and loop compensation. The lag-lead network is particularly useful

because it allows the designer independent selection of loop bandwidth and damping. This is done by strategically positioning the pole and zero frequency locations of the compensator.

Bode techniques as well as root locus techniques illustrate how the lag-lead compensator is used in a PLL. Figure 3.3 shows both Bode and root locus plots of the lag-lead compensated PLL. Note that a PLL with this type of compensator is a second-order system. Actual PLLs are not second-order systems since there are always extra poles in the loop gain. If these poles are located much higher in frequency than the loop gain unity gain crossover frequency, second-order analysis is sufficient. More realistic stability analysis can be done using third- or fifth-order equations as described by Rohde (8, pp. 31-42), or by tabulating loop gain and phase and looking at the gain and phase margins.

In the following discussion, analysis for the lag-lead compensated PLL will be presented. Included in the analysis will be details for the selection of component values in the compensator.

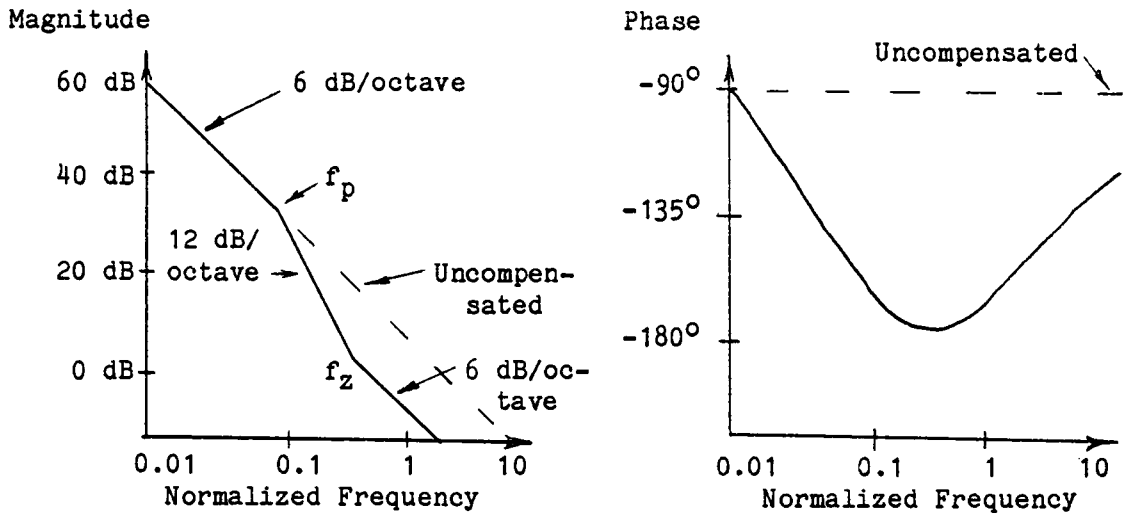
The Second-Order Phase-Locked Loop

If the loop amplifier/filter is a lag-lead network, the PLL becomes a second-order system provided there are no additional poles in the loop gain. The schematics and accompanying equations for both passive and active lag-lead networks are shown in Figure 3.4.

Closed loop response. Substituting the lag-lead network transfer functions into the closed loop gain equation, Equation 3.5, gives

$$A_{cl} = \phi_{out}/\phi_{in} = N[\ G(st_2+1)/t_1\ ]\ /\ [\ s^2 + s(1+Gt_2)/t_1 + G/t_1\ ] \quad (3.8)$$

BODE PLOT OF LOOP GAIN (T)



ROOT LOCUS PLOT OF LOOP GAIN (T)

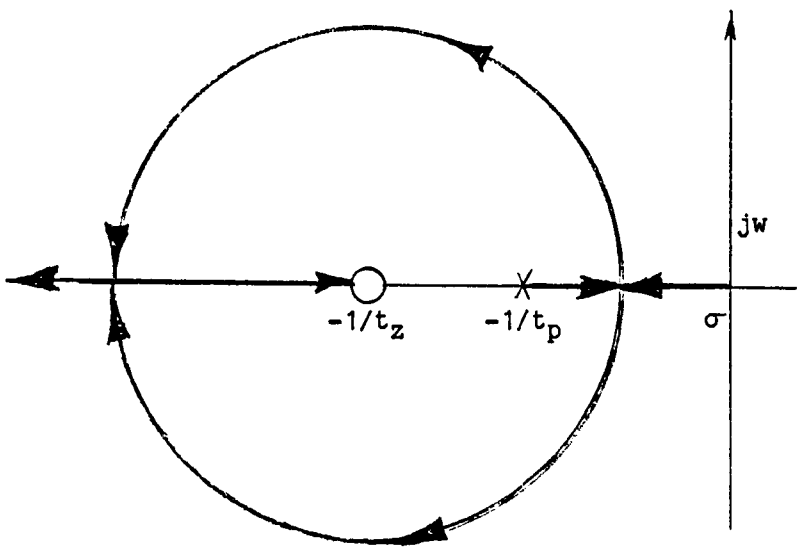
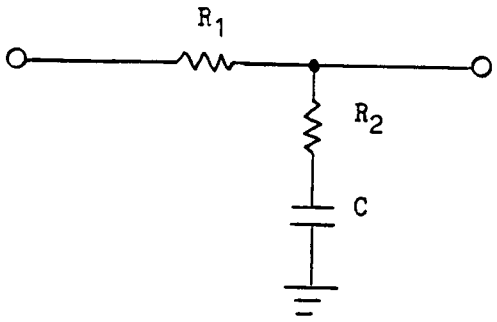


Figure 3.3. Bode and Root Locus Plots for the Lag-Lead Compensated Phase-Locked Loop.

PASSIVE LAG-LEAD NETWORK

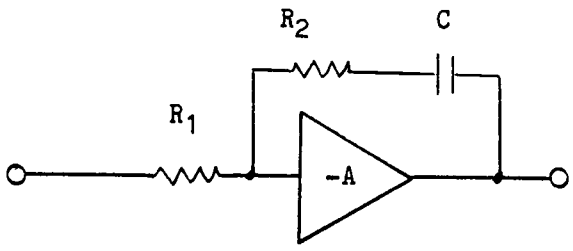


$$K_f(s) = (st_2 + 1)/(st_1 + 1)$$

$$t_1 = (R_1 + R_2)C$$

$$t_2 = R_2C$$

ACTIVE LAG-LEAD NETWORK



A large

$$K_f(s) = (st_2 + 1)/st_1$$

$$t_1 = R_1C$$

$$t_2 = R_2C$$

Figure 3.4. Passive and Active Lag-Lead Networks.

for the passive filter, and

$$A_{cl} = \phi_{out}/\phi_{in} = N[\ G(st_2+1)/t_1\ ]\ /\ [\ s^2 + sGt_2/t_1 + G/t_1\ ] \qquad (3.9)$$

for the active filter, where the dc loop gain is

$$G = K_\phi K_V/N. \qquad (3.10)$$

The closed loop gain equations may be rewritten as

$$A_{cl} = \phi_{out}/\phi_{in} = N[\ s(2\zeta w_n - w_n^2/G) + w_n^2]\ /\ [s^2 + 2\zeta w_n s + w_n^2] \qquad (3.11)$$

for the passive filter, and

$$A_{cl} = \phi_{out}/\phi_{in} = N[\ 2\zeta w_n s + w_n^2]\ /\ [s^2 + 2\zeta w_n s + w_n^2] \qquad (3.12)$$

for the active filter, where w_n is the loop natural frequency in radians/second and ζ is the loop damping factor. W_n and ζ are found by inspection to be

$$w_n \text{ (passive filter)} = \sqrt{G/t_1}, \qquad (3.13)$$

$$\zeta \text{ (passive filter)} = (1/2)w_n[t_2 + 1/G], \qquad (3.14)$$

$$w_n \text{ (active filter)} = \sqrt{G/t_1}, \qquad (3.15)$$

$$\zeta \text{ (active filter)} = (1/2)w_n t_2. \qquad (3.16)$$

The closed loop gain equations for the loop with the passive filter become equal to those of the active loop if $1/G \ll t_2$. If this condition is met, the loop is called a high gain second-order system. To simplify the analysis and because most PLLs can be approximated by

high gain second-order systems, the remaining analysis will focus on the high gain second-order system.

Note that the dc loop gain G has dimensions of sec^{-1} or an inverse time constant. Although the dc loop gain is a constant with frequency, it is a function of VCO gain, phase detector gain, and the loop divider ratio. The loop divider ratio is not fixed for frequency synthesizers with multiple output frequencies. In addition, the VCO often has a nonlinear output frequency to input voltage characteristic. Practical methods of dealing with these problems and the resulting varying dc loop gain will be discussed later.

The closed loop frequency response consists of a second-order lowpass response summed with a second-order bandpass response as can be seen from the equations. Since typical loop damping (ζ) values vary from 0.5-2, the bandpass response does not cause significant peaking. It does, however, dominate the response for frequencies above the loop natural frequency (w_n), causing a 6 dB/octave ultimate roll-off with increasing frequency. A plot of the closed loop frequency response for different damping values is shown in Figure 3.5.

Loop-error response. The loop-error response is also of interest since it illustrates how internal noise perturbations are treated by the loop. The loop-error response is

$$\phi_{error}/\phi_{in} = 1/(1-T) = s^2 /[\, s^2 + 2\zeta w_n s + w_n^2 \,], \qquad (3.17)$$

which is a second-order highpass response. A plot of the error frequency response for different damping values is shown in Figure 3.6.

Transient response. The transient response of a PLL is very important for understanding the behavior of the loop for step changes in the input frequency, changes in N (the loop divider ratio), and all transient perturbations. Loop transient response may be found for a step input frequency change by recognizing that $\Delta w/s^2$ is the Laplace transform of the input phase for a step change in frequency. Multiplying this driving function by the closed loop gain response allows

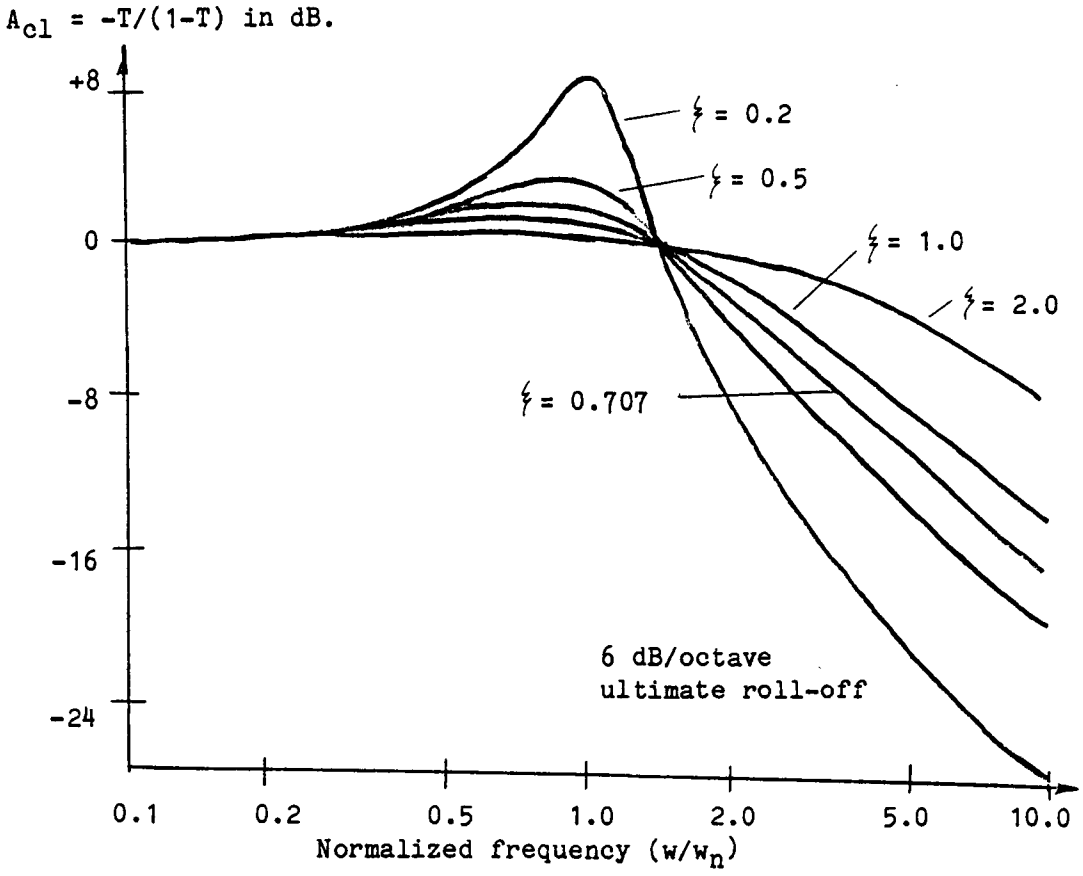


Figure 3.5. Closed Loop Frequency Response for a High Gain Second-Order Phase-Locked Loop.

the output phase response to be found. Then the output phase response is differentiated with respect to time to find the output frequency transient response (23, pp. 46-47). If the VCO has a fairly linear voltage-to-frequency characteristic, as is usually the case, the input voltage of the VCO will follow a loop transient just as the output frequency does. One method of measuring ζ is in fact by watching the

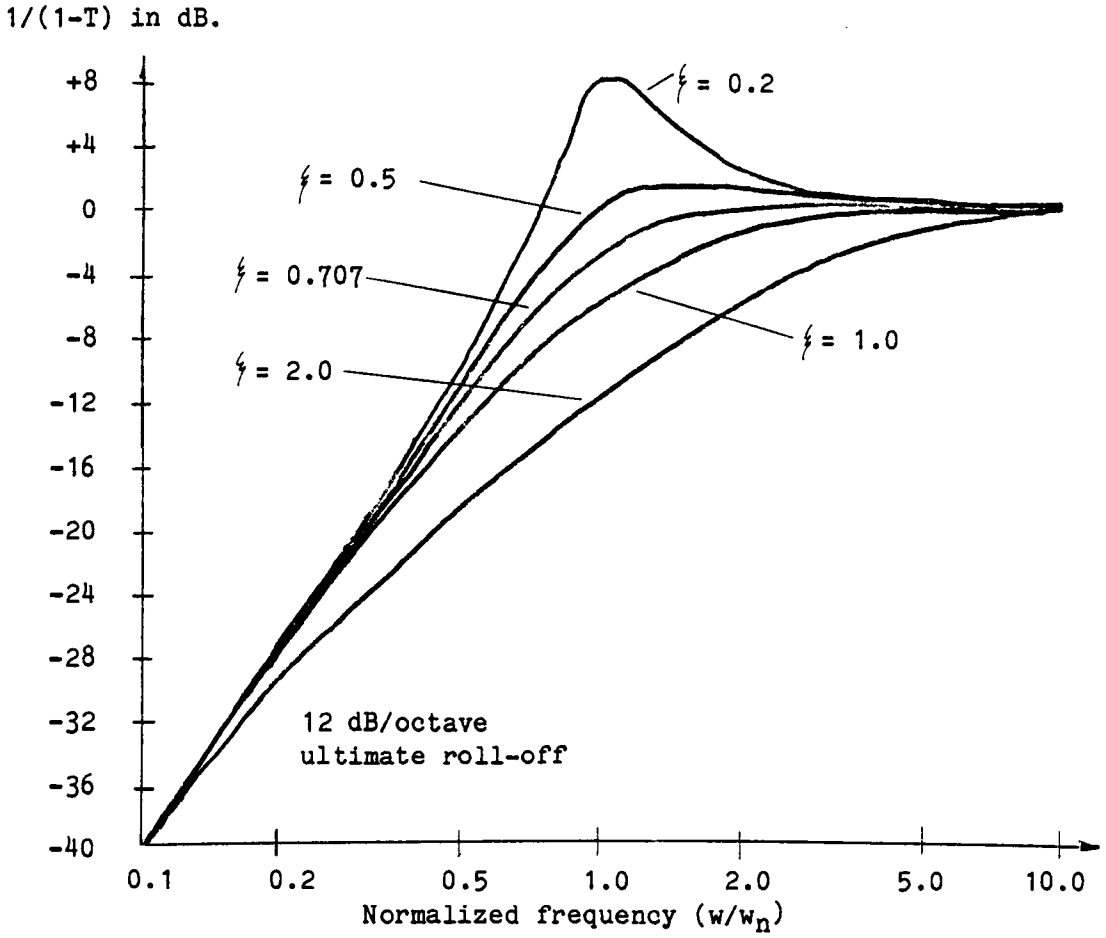


Figure 3.6. Loop-Error Frequency Response for a High Gain Second-Order Phase-Locked Loop.

VCO input voltage during a loop transient. The transient response for a second-order loop is shown in Figure 3.7.

Lock-up time is that time, as measured by the transient response, that is required for the loop to adjust to a transient. In synthesis loops, lock-up time is the time required for the loop to correctly synthesize a new output frequency when N is changed. Lock-up time can be seen from the transient response shown in Figure 3.7.

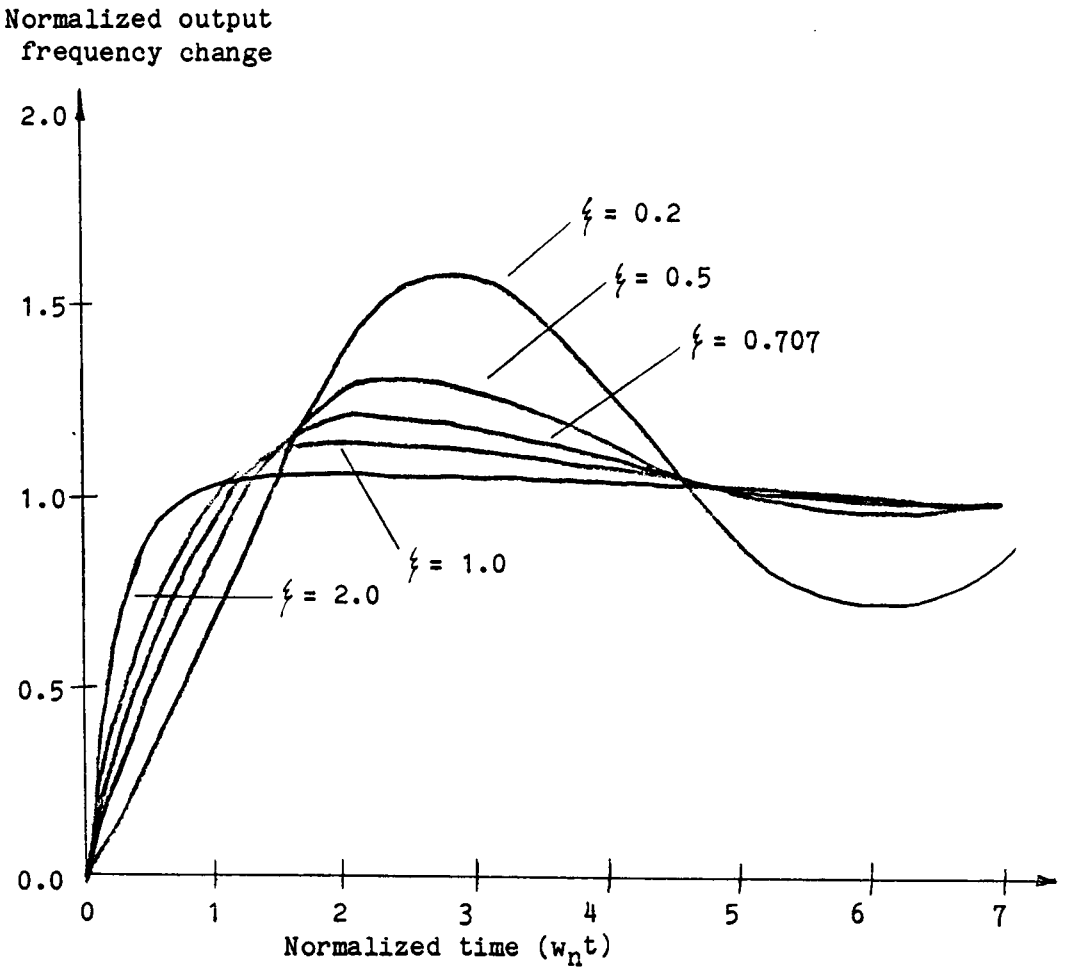


Figure 3.7. Transient Response for a High Gain Second-Order Phase-Locked Loop.

Lock-up time is inversely proportional to w_n, which means that a wideband loop locks more rapidly than a narrow bandwidth loop. There are, unfortunately, practical considerations which limit the loop bandwidth to a value well under the loop input frequency or reference frequency.

Noise Analysis Of Phase-Locked Loops

Noise Model

Phase noise in the output of a PLL is caused by noise at the reference input and by internal noise contributions of the various PLL stages. Depending upon where noise is introduced into the system, feedback will affect it differently. A noise model that will be used for PLL noise analysis is shown in Figure 3.8.[6]

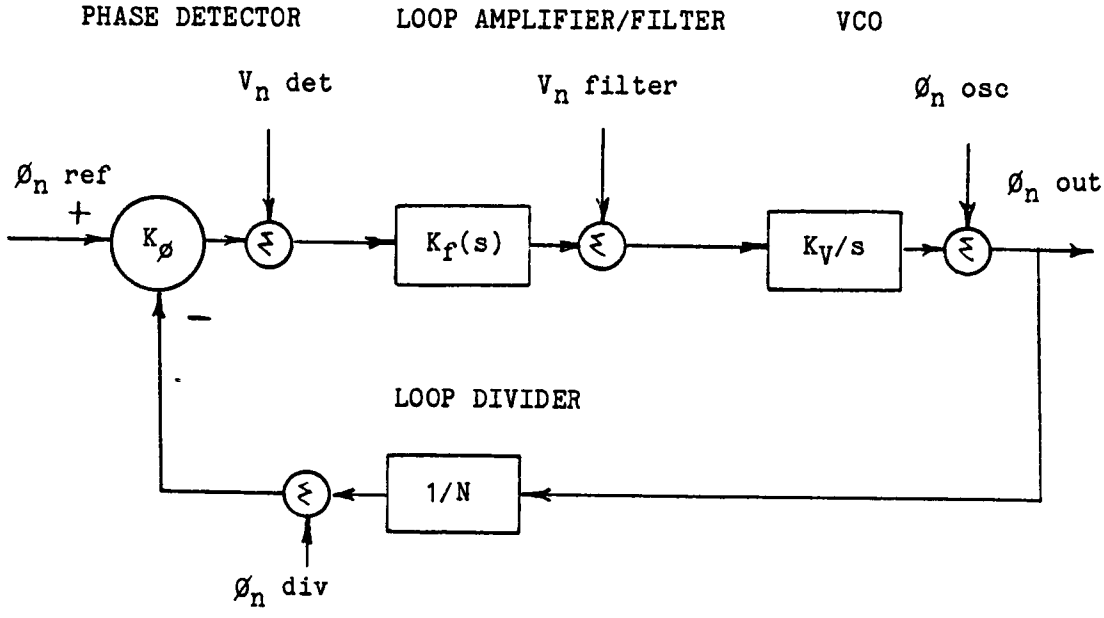


Figure 3.8. Phase-Locked Loop Noise Model.

The model noise parameters are defined below:

- $\cdot\phi_n$ ref — Reference or input phase noise
- $\cdot V_n$ det — Phase detector output noise voltage
- $\cdot V_n$ filter — Loop amplifier/filter output noise voltage
- $\cdot\phi_n$ osc — VCO output phase noise
- $\cdot\phi_n$ div — Loop divider output phase noise
- $\cdot\phi_n$ out — Phase-locked loop output phase noise

Noise Analysis

The PLL output phase noise contribution from each noise source must be evaluated and summed to find the total PLL output noise. Reference phase noise and divider phase noise appear as inputs to the PLL and are acted upon by the closed loop gain. Their contribution to output phase noise is given by

$$\phi_n \text{ out}/\phi_n \text{ ref} = \phi_n \text{ out}/\phi_n \text{ div} = N[\ -T/(1-T)\ ]. \qquad (3.18)$$

Similarly, phase detector output noise voltage is acted upon by the closed loop gain, after it is converted to equivalent phase noise at the phase detector input. This contribution to PLL output phase noise is given by

$$\phi_n \text{ out}/V_n \text{ det} = (1/K_\phi)N[\ -T/(1-T)\ ]. \qquad (3.19)$$

VCO noise is acted upon by the loop-error response, and its noise contribution is given by

$$\phi_n \text{ out}/\phi_n \text{ osc} = 1/(1-T). \qquad (3.20)$$

Finally, the amplifier/filter noise voltage is also acted upon by the loop-error response, after it is converted to equivalent phase noise at the VCO output. The PLL output phase noise contribution is given by

$$\phi_n \text{ out}/V_n \text{ filter} = (K_V/2\pi f_m)[\ 1/(1-T)\ ]. \qquad (3.21)$$

All of the PLL noise sources are uncorrelated as each stage is independent. Thus, the total output phase noise may be calculated by squaring the individual noise contributions of each stage and then summing them. This gives

$$\phi_n^2 \text{ out} = [\phi_n^2 \text{ ref} + \phi_n^2 \text{ div} + (V_n^2 \text{ det})(1/K_\phi^2)][N(-T/(1-T))]^2$$

$$+ [\phi_n^2 \text{ osc} + (V_n^2 \text{ filter})(K_V/(2\pi f_m))^2][1/(1-T)]^2. \qquad (3.22)$$

The output phase noise in this expression has units of radians squared and is the mean square phase noise if all noise sources are specified in mean square units. If spectral densities are used for the noise terms, output phase noise is in the familiar form of phase noise spectral density, $S_\phi(f_m)$. Since the noise terms and their corresponding transfer functions are functions of frequency, phase noise should be evaluated at several frequencies to arrive at the output phase noise spectral density.

Low Noise Design Considerations

The preceding noise analysis can be used to develop low noise design strategies. The analysis shows that all noise sources should have minimum noise (obviously), and that the phase detector gain (K_ϕ)

should be maximized and the VCO gain (K_V) should be minimized.[6] Maximizing the phase detector gain also raises the loop gain (T), which is usually desirable, but minimizing the VCO gain lowers the loop gain, which is usually not desirable as this lowers the loop bandwidth.

Since reference, divider, and phase detector noise are acted upon by the closed loop gain, these are significant noise sources at frequencies below the loop bandwidth. However, at frequencies well above the loop bandwidth they become insignificant. In contrast, VCO and amplifier/filter noise are acted on by the loop-error response. These noise sources are "cleaned up" by the loop at frequencies below the loop bandwidth, but contribute directly to the output noise at frequencies above the loop bandwidth. In summary, reference, divider, and phase detector noise are dominant at frequencies well below the loop bandwidth, whereas VCO and amplifier/filter noise are dominant at frequencies well above the loop bandwidth.[6]

It should be apparent that there is an optimum PLL loop bandwidth for minimum output noise at which frequency the reference, divider, and phase detector noise contributions just equal the VCO and amplifier/filter noise contributions. This optimum loop bandwidth is found by plotting the PLL output noise due to the reference, divider, and phase detector assuming infinite loop gain, or ideal closed loop gain ($-T/(1-T) = 1$). Then the output noise contribution of the VCO and amplifier/filter is plotted on the same graph, assuming that the loop gain is zero, giving maximum error response ($1/(1-T) = 1$). The frequency where these two noise plots intersect is the optimum loop bandwidth for noise performance. For a loop with this loop bandwidth,

the output phase noise is given approximately by the lesser of the two noise plots.[24] In addition to selecting loop bandwidth, some noise optimization is possible by selecting loop damping.[25]

It is unfortunate that loop bandwidth is limited usually to 20% of the reference frequency and cannot exceed the reference frequency. Thus, the optimum loop bandwidth for noise may not be attainable in a synthesizer with narrow channel spacing, or correspondingly, a low reference frequency. Similarly, low dc loop gain may impose additional limits on the loop bandwidth, causing it to be below the optimum value. In wideband loops, fast lock-up time requirements may require a higher loop bandwidth than the optimum bandwidth for noise.

Spurious Noise Outputs

It is important to realize that spurious noise outputs in a PLL are not caused by random noise. The use of terminology such as "60 Hz noise or reference frequency noise" is misleading since these outputs are usually caused by power supply ripple and phase detector reference frequency feedthrough, respectively. Spurious outputs can be very difficult to predict and eliminate as they are often caused by poor shielding and poor grounding techniques.

In multiple loop PLLs where mixers are often used to generate sum or difference frequencies, spurious outputs are to be expected due to unwanted mixer products. Single loop PLLs are essentially free of these spurious outputs, which are often several MHz away from the carrier.

Phase-Locked Loop Circuit Elements

Reference Frequency Oscillators

The reference frequency oscillator should have excellent long-term frequency stability and low phase noise. Reference oscillators are almost always crystal oscillators. However, atomic clocks are sometimes used as references for low phase noise crystal oscillators. The resulting system has excellent long-term stability (from the atomic clock), and excellent short-term stability (from the crystal oscillator).[26]

Since many PLL frequency synthesizers require low reference frequencies because of narrow channel spacings, digital frequency dividers are often used in conjunction with a low noise crystal oscillator. Low phase noise crystal oscillator design will be discussed later in this thesis.

Phase Detectors

The phase detector senses the loop input phase and feedback phase difference and provides an error voltage proportional to this difference. There are basically two types of phase detectors. One type has an output that is a continuous sine or square wave with a varying dc level proportional to phase difference. A mixer or multiplier is an example of this type of phase detector. Since the strong ac signal in the output of this detector will modulate the VCO, causing severe reference frequency sidebands, this type of phase detector is rarely used for PLL frequency synthesizers. It is, however, sometimes used for single frequency synthesizers where the

reference frequency is very high and may be easily filtered out of the phase detector output.[20]

The second type of phase detector does not produce the continuous sine or square wave output. Instead, its output contains a dc level with only minimal reference frequency feedthrough. The output of this phase detector may be filtered much easier in the amplifier/filter stage of the loop to prevent VCO modulation.[20]

Most of these types of phase detectors are actually phase/frequency detectors because they respond to frequency error as well as phase error. That is, if the inputs are at different frequencies, the phase/frequency detector will output a full scale voltage to allow for correction. Phase/frequency detectors are almost always used in PLL synthesizers as they ensure reliable phase-locking.

The digital tri-state phase/frequency detector is commonly used for PLL synthesizers. It produces an output pulse equal to its positive supply voltage for the time duration the feedback phase lags the reference phase or continuously if the feedback frequency is less than the reference frequency. Similarly, it produces an output equal to its negative supply voltage for the time duration the feedback phase leads the reference phase or continuously if the feedback frequency is greater than the reference frequency. Finally, if the feedback phase and reference phases are equal, the output goes to the tri-state or open circuit state. The capacitors in the loop amplifier/filter hold the dc voltage that results in phase-locking. The output of this phase/frequency detector is very clean because it only comes into play when there is phase error. Most of the time the

VCO control voltage is being generated by charge storage in a capacitor that has very little noise.

The RCA CD4046 CMOS PLL integrated circuit contains a tri-state phase/frequency detector and is probably the best commercially available integrated circuit phase detector. There are some interesting subtleties with this and other similar types of detectors. Most importantly, when the phase error is zero, gain drops significantly as the detector is essentially out of the circuit (8, p. 224). This causes the loop feedback parameters to change. Rohde (8, pp. 225-229) presents several circuits that deal with this problem, the simplest being placing a 1 M ohm resistor between the detector output and ground. This causes the output to produce narrow pulses to overcome the current leakage in the resistor. However, this obviously degrades the reference frequency suppression since there is a continuous ac component in the phase detector output.

Loop Amplifier/Filters

The loop amplifier/filter provides lowpass filtering for phase detector reference frequency feedthrough and other noise. It also provides compensation for the loop. The loop amplifier/filter is designed just as any other voltage sensitive stage. Since active elements are often used, their noise contributions must be considered.

The most common loop amplifier/filter is the lag-lead network followed with additional lowpass filtering or notch filtering for improved reference frequency suppression. Low noise operational amplifiers or discrete amplifiers may be used, and careful attention

must be paid to device noise, power supply rejection, and circuit shielding.

If the loop divider ratio changes over a significant range, say over 2:1, it may be desirable, or even necessary, to change the loop amplifier/filter response to maintain an adequately stable loop. A multiplying CMOS DAC may be used to change the loop amplifier/filter response digitally to track changes in the loop divider ratio.[27] Since microprocessors are so widely used, it may be convenient to program the loop amplifier/filter digitally based upon the selected output frequency range of a synthesizer.

Voltage Controlled Oscillators

VCO phase noise performance is extremely important as it dominates the PLL phase noise performance at frequencies above the loop bandwidth unless the amplifier/filter noise is excessive. The VCO must have a well buffered output with good reverse isolation so that nonlinear loading effects do not perturb it, causing increased output phase noise. Low noise oscillator design is discussed exclusively in Sections 4 and 5 of this thesis.

Loop Frequency Dividers

There are many implementations of digital frequency dividers. Most use programmable moduli or division ratios if they are used in a multiple output frequency synthesizer.

Programmable dividers are available in CMOS, TTL, IIL, MOS, and ECL technologies. They are usually presettable down counters that automatically set and count down to zero and then set again, producing

a single pulse out for every group of N pulses, where N is the division ratio. Since the counters have to reach the terminal count (usually zero), know that they have reached it, and preset to N within one input clock cycle (unless a look-ahead scheme is used), they are usually limited in frequency. CMOS and MOS programmable dividers are typically limited to 1 MHz, except for the new high speed CMOS dividers which have speeds comparable to low power Schottky TTL. TTL programmable dividers are usually limited to around 10-30 MHz depending upon the family.

To overcome these limitations, some form of frequency prescaling or division ahead of the programmable dividers is often necessary. Fixed modulus prescalers are undesirable as they limit the overall division ratio resolution of the divider network. This in turn forces the reference frequency of the loop to be lowered by the amount of the prescaling. This is bad since the highest possible loop reference frequency is usually desired as it allows for a wider loop bandwidth.

Variable modulus prescalers overcome this problem by permitting division ratio resolution down to the single digit, while still lowering the frequency feeding the next stages. Consider, for example, a ÷10/11 variable modulus prescaler in a programmable divider circuit. To divide by 649, the variable modulus prescaler divides by 11 nine times and then divides by 10 for the remaining of the 55 counts. The resulting overall division ratio is then (9x11) + (55x10), which is 649. Other variable moduli or division ratios may be used, such as ÷100/101. A ÷100/101 variable modulus programmable divider is described later for the 45-75 MHz synthesizer.

The topic of programmable dividers is extensive and well covered in the literature. The reader is referred to Rohde's book[8] and the Plessey digital data book[28] for additional discussion and practical circuits.

4. LOW NOISE OSCILLATOR THEORY AND DESIGN

Causes Of Oscillator Noise

An oscillator has two basic circuit elements: a resonator or frequency determining element, and a sustaining amplifier to maintain a gain of one around the loop. Finite Q in the resonator and noise in the sustaining amplifier give rise to oscillator noise.

From the Barkhausen criterion, an oscillator operates at a frequency where the phase shift around the loop is zero and the gain around the loop is one (8, pp. 143-144). When an oscillator is first powered, the loop gain exceeds one, and internal noise builds until the oscillator levels at its designed output level. At this point, the loop gain is maintained at precisely unity by some form of limiting or automatic gain control (AGC).

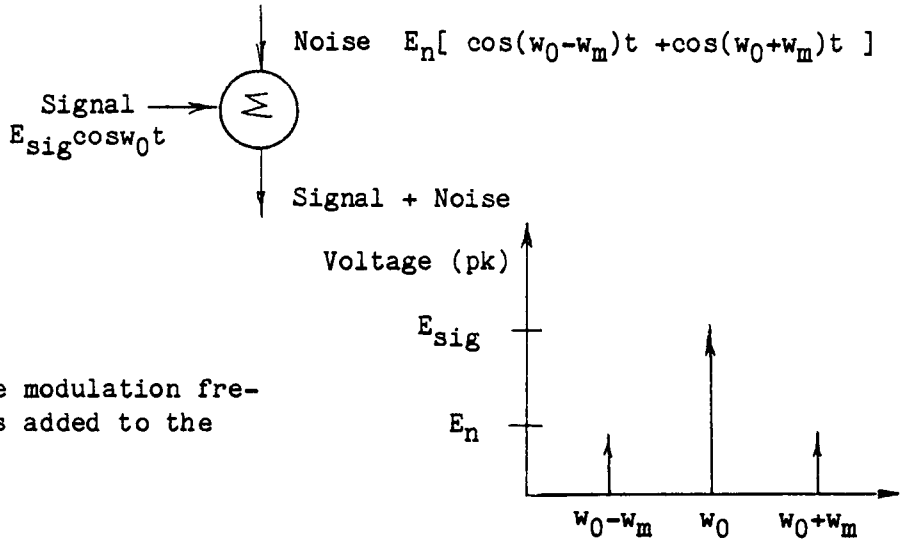
The mechanism for oscillator phase noise is actually quite simple. The resonator, which is usually a single pole bandpass filter, has a phase transfer characteristic that is a function of frequency. At resonance, the phase shift through the filter is zero, and it approaches positive (usually $+90^{o}$) and negative (usually -90^{o}) limits for frequencies below and above resonance. If the sustaining amplifier introduces a phase error in the oscillator signal, the oscillator output will have to change to the frequency where the resonator phase shift just cancels the sustaining amplifier phase error. This is required to maintain a phase shift around the loop of zero. Thus, the oscillator output frequency wanders around correcting for phase perturbations that the sustaining amplifier introduces (8, pp. 153-154).

As discussed previously, oscillator frequency fluctuations can be directly related to phase fluctuations.

It should be clear that if the sustaining amplifier is noiseless, the oscillator will be noiseless as frequency shifts are not required because there are no phase perturbations that require correction. Additionally, if the resonator Q is infinite, the oscillator is also noiseless because sustaining amplifier phase perturbations will be corrected by infinitesimal shifts in the oscillator frequency. The goals of low noise oscillator design are then to minimize sustaining amplifier phase noise and to maximize the resonator Q. It is important to realize that it is the loaded Q of the resonator that is important in an oscillator. The oscillator circuit will always degrade resonator Q by some degree, and resonator Q can be degraded by more than one-half in a poorly designed oscillator circuit. To understand how the sustaining amplifier introduces phase noise into an oscillator, it is necessary to understand additive noise.

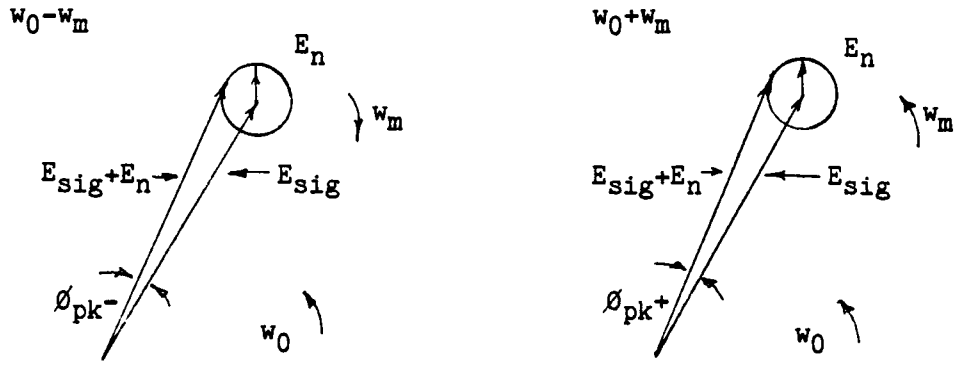
Additive Noise

Additive noise describes linear summing of noise and should not be confused with noise that is generated by signal mixing (multiplication) or other nonlinear processes. Consider white noise that is added to a signal that has no phase noise. The mechanism of additive noise is shown in Figure 4.1, where sinusoidal noise sources are shown at a frequency f_m from each side of the carrier. The phasor diagrams in Figure 4.1 show how the added noise results in a phase perturbation at the frequencies $f_0 - f_m$ and $f_0 + f_m$ in the signal spectrum, where f_0



Noise at the modulation frequency w_m is added to the signal.

PHASOR DIAGRAMS



The peak phase deviation for each phasor is E_n/E_{sig} if $E_n/E_{sig} << 1$. Since noise at the frequencies w_0-w_m and w_0+w_m is uncorrelated, the phase deviations add power-wise. Thus $\phi_{pk} = \sqrt{2}\phi_{pk-} = \sqrt{2}\phi_{pk+}$.

So $\phi_{rms} = (1/\sqrt{2})\sqrt{2}E_n/E_{sig}$, and $\phi_{rms}^2 = (E_n/E_{sig})^2$, resulting in $S_\phi = (E_n/E_{sig})^2$.

Figure 4.1. Illustration of Additive Phase Noise.

Source: Scherer, D.,"Design Principles and Test Methods for Low Phase RF and Microwave Sources," Hewlett-Packard RF and Microwave Symposium and Exhibit, October 1978.

is the carrier frequency. The frequencies of the phase perturbations correspond to a phase noise frequency of f_m. The resultant phase noise spectral density as derived in the figure is

$$S_\phi(f_m) = (E_n/E_{sig})^2 = P_n/P_{sig}, \qquad (4.1)$$

where E_n is the noise voltage in a 1 Hz bandwidth, and E_{sig} is the total signal voltage. If evaluating in terms of power, P_n is the noise power in a 1 Hz bandwidth, and P_{sig} is the total signal power.

Note that it has been assumed that the additive noise is white noise. This is a good assumption because phase noise at the modulation frequency f_m is caused by noise at the frequencies f_0-f_m and f_0+f_m. Since the carrier frequency f_0 is usually much greater than the modulation frequency f_m of interest, the added noise of interest is contained in a small band of frequencies near the carrier. Over this narrow frequency band, the added noise usually has a constant spectral density.

Note that the phase noise due to additive noise is given simply by the noise to signal ratio. Thus, it is desirable to maximize the signal and to minimize noise. Consider the following additive noise example. A signal of +10 dBm is passed through an amplifier with a +12 dB noise figure. The phase noise spectral density due to additive noise is

$$\begin{aligned} S_\phi(f_m) &= (-174 \text{ dBm/Hz} + 12 \text{ dB}) - (+10 \text{ dBm}) \\ &= \underset{\text{(noise)}}{-162 \text{ dBm/Hz}} \quad - \underset{\text{(signal)}}{(+10 \text{ dBm})} \\ &= -172 \text{ dB rel to } 1 \text{ rad}^2/\text{Hz}. \end{aligned} \qquad (4.2)$$

Here the ratio of noise to signal power was calculated in logarithmic or dB form by subtracting the signal power from the noise power. SSB phase noise is just as easily found and is simply half the phase noise spectral density $S_{\phi}(f_m)$. In the previous example, SSB phase noise is found by simply subtracting 3 dB from the answer. The units would then be, of course, dBc.

Leeson's Oscillator Model

In 1966, Leeson published a heuristic model for oscillator phase noise.[29] It was presented without formal proof, but the phase noise transfer function portion of the model has since been proven by Sauvage.[30] Leeson's model is widely referenced in the literature and allows a designer to estimate the noise performance of an oscillator.

Consider the oscillator block diagram in Figure 4.2. The diagram shows the oscillator sustaining amplifier and a single pole bandpass resonator. Through modulation theory, it can be shown that a phase modulated signal passing through a bandpass filter has the same phase modulation as if the phase modulating signal were passed directly through an equivalent lowpass filter. This analogy is described in Reference 31. From this theory, Leeson's model was derived. The phase modulation equivalent oscillator model is shown in Figure 4.3.

Note that Leeson's model describes the phase noise in an oscillator, where ϕ_{pert} is the added phase noise or phase perturbation at the sustaining amplifier, and ϕ_{out} is the oscillator output phase noise. The phase modulation equivalent filter for the single pole resonator is a single pole lowpass filter with a corner frequency of $f_0/2Q_L$,

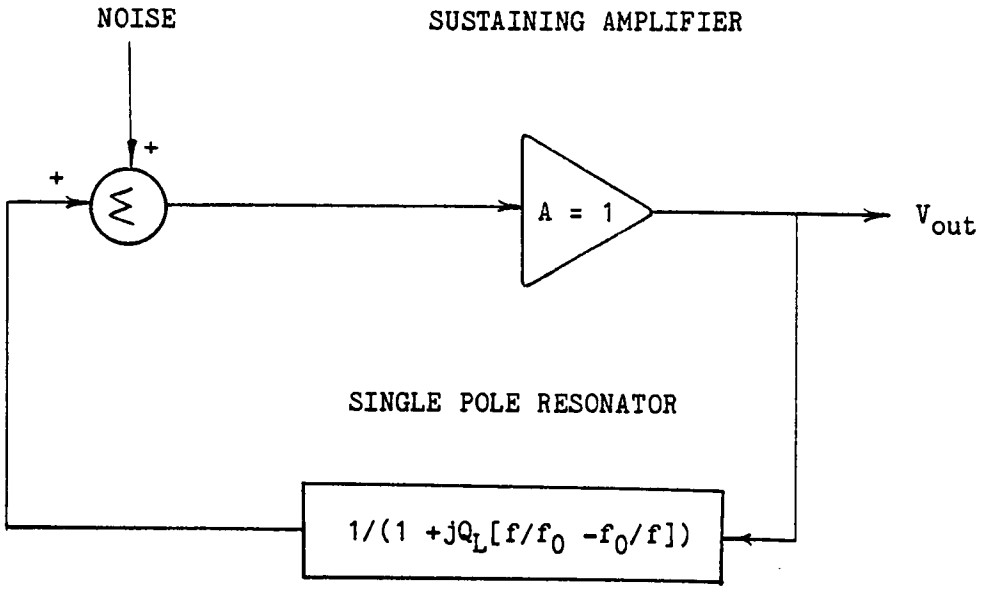


Figure 4.2. Oscillator Block Diagram.

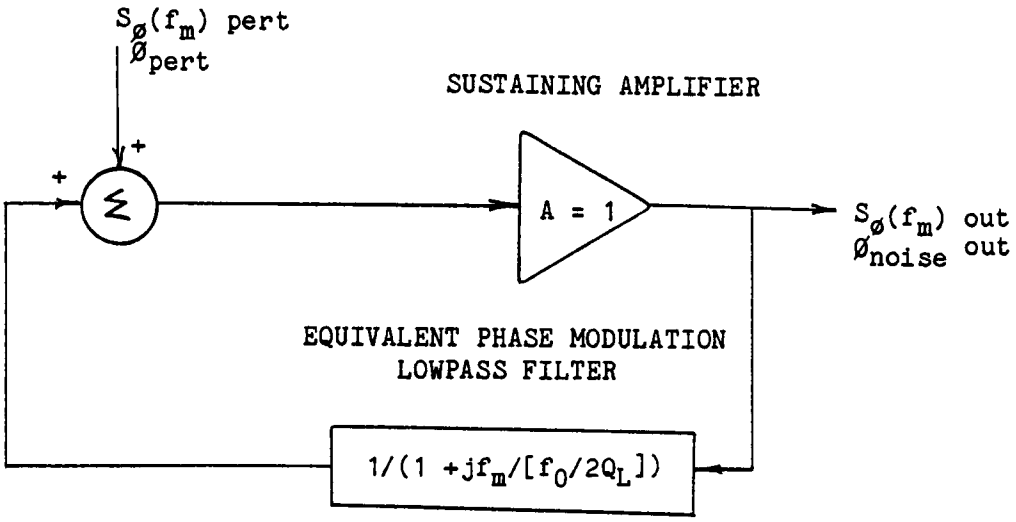


Figure 4.3. Oscillator Phase Modulation Equivalent Model.

where f_0 is the center frequency of the resonator and Q_L is the loaded quality factor of the resonator. Thus, the oscillator feedback element (the resonator) allows phase modulation to pass unattenuated at modulation frequencies below $f_0/2Q_L$ and attenuates phase modulation at frequencies above this by 6 dB/octave. This is analogous to signal phase modulation passing unattenuated through a bandpass resonator at modulation frequencies, f_m, less than half the resonator's 3 dB bandwidth. At modulation frequencies above half the resonator's 3 dB bandwidth, signal phase modulation is attenuated by 6 dB/octave.[6]

Applying feedback theory to Leeson's model results in an expression for the oscillator output phase noise. The sustaining amplifier phase perturbation is acted upon by the loop error response (1/(1-T)), where T is the oscillator loop gain. This gives

$$\begin{aligned} \phi_{out} &= \phi_{pert}\,[\ 1/(1-T)\ ] \\ &= \phi_{pert}\ \frac{1}{1 - 1/[\ 1 + jf_m/(f_0/2Q_L)\ ]} \\ &= \phi_{pert}\,[\ 1 - jf_0/(2Q_L f_m)\ ], \end{aligned} \tag{4.3}$$

where the corner frequency of the equivalent lowpass filter, as previously described, is one-half of the resonator's bandwidth, $f_0/2Q_L$. Note that the loop gain, T, of a feedback amplifier is positive.

The oscillator output phase noise may be expressed in terms of spectral density, which gives

$$S_\phi\ out(f_m) = S_\phi\ pert(f_m)[1 + f_m^{-2}(f_0/2Q_L)^2]. \tag{4.4}$$

This was obtained by squaring the left side of Equation 4.3 and multiplying the right side of the equation by its complex conjugate. Then the spectral densities were substituted for the mean square phase noise terms.

The phase perturbation spectral density is constant with frequency for white additive noise. In reality, the phase noise perturbation increases at low frequencies. This is due to additional noise which is not additive noise. The additional low frequency noise is caused mainly by the effects of 1/f device noise and the resulting modulation of device transconductance and input and output impedances.[6] The 1/f device noise is thus up-converted into the RF oscillator spectrum because of device nonlinearities causing an increase in phase noise close to the carrier. Thus, Leeson described the phase perturbation spectral density by

$$S_{\phi}\ \text{pert}(f_m) = (E_n/E_{sig})^2[1 + f_c/f_m], \qquad (4.5)$$

where E_n is the noise voltage in a 1 Hz bandwidth at the sustaining amplifier input, E_{sig} is the signal voltage at the sustaining amplifier input, and f_c is the low frequency phase noise corner frequency.[29] Note that the expression "$(E_n/E_{sig})^2$" describes additive noise and that the expression "$1 + f_c/f_m$" describes the excess low frequency phase noise. The latter expression is somewhat arbitrary, but Leeson and others have presented experimental data that give the expression credibility.[29]

Leeson recommends using a higher noise level for E_n than the actual noise level.[29] This is because broadband white noise causes a

higher level of white noise to appear in the oscillator sustaining amplifier because of noise intermodulation products. White noise far away from the carrier gets up-converted and down-converted into the frequency region near the carrier, resulting in a higher white noise floor in the oscillator sustaining amplifier and a higher oscillator output phase noise.

Substituting the phase perturbation spectral density (Equation 4.5) into Equation 4.4 gives

$$S_{\phi}\ out(f_m) = (E_n/E_{sig})^2[1 + f_c/f_m][1 + f_m^{-2}(f_0/2Q_L)^2], \qquad (4.6)$$

which is Leeson's complete expression for oscillator phase noise.[29] Again, f_0 is the resonator center frequency or oscillator carrier frequency, Q_L is the loaded resonator quality factor, E_n is the noise voltage in a 1 Hz bandwidth at the sustaining amplifier input, E_{sig} is the signal voltage at the sustaining amplifier input, and f_c is the low frequency noise corner frequency.

Leeson's expression for oscillator phase noise may be expressed in terms of SSB phase noise. This gives

$$L(f_m) = (1/2)S_{\phi}(f_m) = (1/2)(E_n/E_{sig})^2[1+f_c/f_m][1+f_m^{-2}(f_0/2Q_L)^2], \quad (4.7)$$

where it is assumed that the total peak phase noise is much less than one radian.

This expression may be plotted for two distinct cases. If the resonator half bandwidth ($f_0/2Q_L$) exceeds the low frequency phase noise corner frequency (f_c), the oscillator is called a low Q oscillator.[6] Most LC oscillators are low Q oscillators. If the resonator

half bandwidth is less than the phase noise corner frequency, the oscillator is called a high Q oscillator.[6] Most crystal oscillators are high Q oscillators. The SSB phase noise of both oscillator types is shown in Figure 4.4.

Note from the figure the different phase noise slopes. Within the resonator half bandwidth, phase noise increases at 20 dB/decade with decreasing frequency. At frequencies below the low frequency phase noise corner frequency, phase noise increases by an additional 10 dB/decade with decreasing frequency. The ultimate phase noise floor is reached at frequencies above the greater of the resonator half bandwidth or the low frequency phase noise corner.

Minimizing Sustaining Amplifier Noise

Signal-to-Noise Ratio Effects at RF Frequencies

From Leeson's model, it is clear that additive noise at the sustaining amplifier is a primary contributor to oscillator noise. Additive noise is caused mostly by RF noise in the active devices, so obviously low RF noise devices should be used. Further, since additive phase noise varies inversely with the signal-to-noise ratio, the sustaining amplifier input signal should be maximized. There are, unfortunately, practical limits governing the signal level in an oscillator. The active devices should not be overdriven to where they saturate, become improperly biased, or reach breakdown. Any of these occurrences will usually result in a severe degradation of resonator Q by loading the resonator.

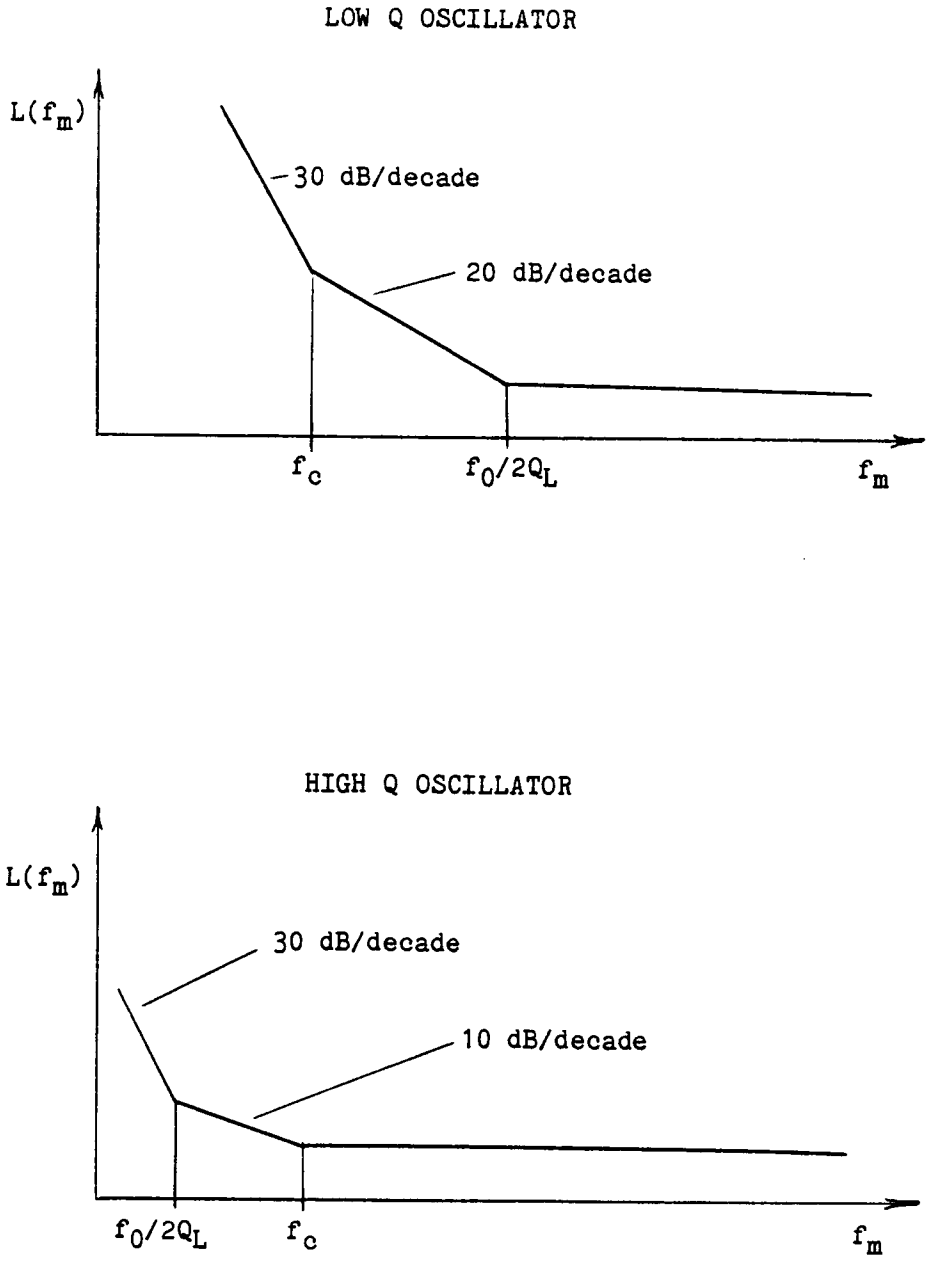


Figure 4.4. Phase Noise of Low Q and High Q Oscillators.

The choice between bipolar transistors and junction field-effect transistors (JFETs) is not obvious as the decision must be based on resonator loading effects, impedance levels, and device noise. JFETs are generally well suited for LC oscillators because they present a high impedance load to a parallel LC tank circuit. Further, they can be driven by the high impedance of an LC parallel tank circuit because of their low noise currents.

Bipolar transistors are generally well suited for overtone crystal oscillators where the crystal is coupled to the emitter of the transistor. The low emitter resistance of the bipolar transistor assures the introduction of minimum series resistance into the crystal circuit, thus maximizing its loaded Q. In addition to selecting an active device with minimum RF noise, low frequency 1/f noise must also be minimized along with device intermodulation distortion.

Low Frequency Device Noise Modulation Effects

Mechanisms of low frequency device noise modulation. Low frequency device noise cannot add directly to the RF oscillator signal, as signal addition generates no new frequency components. Unfortunately, low frequency device noise modulates the device transconductance and input and output impedances, causing both AM and PM modulation. The low frequency noise is thus effectively up-converted into the RF signal spectrum.

Generally, amplitude modulation caused by low frequency noise does not directly pose a problem, as limiting within the oscillator suppresses AM noise. However, AM-to-PM conversion within the active

devices causes amplitude modulation to be converted to phase modulation, resulting in phase noise. Circuit limiting, of course, does nothing to reduce phase modulation.

AM-to-PM conversion is caused in part by nonlinear device input and output impedances. The impedance levels in fact are a function of the signal level causing circuit phase fluctuations that are a result of fluctuating signal levels caused by AM noise.[32] The initial AM noise is generated mostly by low frequency or 1/f noise device transconductance modulation.

Bipolar transistors are especially susceptible to AM and PM noise modulation. This is because their transconductance and input and output impedances are strong functions of bias level, which fluctuates due to low frequency device noise. Bipolar transistor AM and PM modulation may be analyzed or measured by finding the magnitude and phase of device transconductance as a function of bias current. Transconductance should be evaluated at the RF frequency of interest.

Once the magnitude and phase of device transconductance are found as a function of bias current, the expressions may be differentiated with respect to bias current. The change in transconductance magnitude with bias current gives the AM gain for low frequency noise, and the change in transconductance phase with bias current gives the PM gain for low frequency noise. This calculation is illustrated by Healey using the hybrid-pi transistor model.[33]

Bipolar transistor input and output impedance and transconductance dependency on emitter current are easily seen from the hybrid-pi model. If the current gain, B, and gain bandwidth product, f_T, are

assumed to be constant with emitter current, additional inaccuracy above the basic hybrid-pi model will result in the calculations of AM and PM gain in the device. This is because both B and f_T are functions of emitter current, and to a lesser extent, base-collector voltage. The computer analysis program SPICE (Simulation Program with Integrated Circuit Emphasis) is recommended for analyzing device bias-level AM and PM gain. The SPICE program uses the Gummel-Poon bipolar transistor model, which is a charge-controlled model that includes many of the subtle transistor parameter shifts with bias and signal levels.

JFETs exhibit much less transconductance and input and output impedance modulation with bias current compared to bipolar transistors. This is because their transconductance is not as strong a function of bias current and their input and output impedances remain much more constant with varying bias current. This is the reason JFETs exhibit superior intermodulation performance over bipolar transistors. In short, JFETs are more linear devices and are less susceptible to low frequency AM and PM noise modulation.

The mechanism of phase modulation has been thought to be primarily a second-order intermodulation effect where low frequency noise modulation of the fundamental frequency results in most of the phase modulation.[34] Second-order intermodulation is evaluated by finding transconductance phase modulation at the oscillator fundamental frequency. However, recent analysis has shown that in some oscillators, particularly VHF oscillators, the phase modulation is actually a third-order intermodulation effect. Here the oscillator fundamental

and second harmonic are AM modulated by differing amounts. Since the second harmonic is out of phase with the fundamental, this causes considerable phase modulation. The fundamental and second harmonic are out of phase because device phase shift is greater for the second harmonic. This third-order intermodulation mechanism has been analyzed using the SPICE circuit analysis program.[34] This intermodulation mechanism is probably not present in oscillator stages that are tuned because signal harmonics are heavily rejected.

Circuit parameter changes or modulations that are caused by the oscillator fundamental signal should not be confused with circuit parameter modulations caused by low frequency noise. Circuit parameter modulation caused by the oscillator fundamental frequency causes the generation of harmonics only, and this is simply harmonic distortion. Harmonic distortion, in itself, is generally not a problem in oscillators, and if it were, the harmonics could be easily filtered out.

Further discussion of low frequency device modulation mechanisms is beyond the scope of this thesis as low frequency or 1/f noise is an entire subject of its own, and the mechanisms of phase modulation due to device nonlinearities is another entire subject area. The remaining focus will be on optimum circuit designs that minimize the effects of 1/f noise and on the selection of low 1/f noise devices. The reader is referred to Reference 35 for further discussions of theoretical 1/f noise effects in oscillators and to Reference 36 for discussions of 1/f noise in solid state devices.

Circuit design for low 1/f noise effects. Low frequency noise modulation effects may be minimized by using low frequency circuit degeneration to minimize low frequency noise modulation of device bias, and by using RF circuit degeneration to help stabilize device transconductance and input and output impedances and thus reduce the PM modulation gain of the active device.[37] The reduction of PM modulation gain is a result of making the active device more linear and lowering its intermodulation distortion. This not only reduces low frequency noise modulation, but also reduces broadband noise intermodulation, which raises the effective additive noise in the oscillator.

Consider the circuit of Figure 4.5 for an example of 1/f noise circuit degeneration. The oscillator of Figure 4.5 is an LC oscillator with a JFET differential limiter for the sustaining amplifier. Low frequency JFET device noise voltage is heavily degenerated by the current source bias and by the high reactance of the source coupling capacitor.[38] Thus, low frequency device noise does not significantly modulate the device bias currents, resulting in less AM and PM modulation in the active devices. At RF frequencies, the coupling capacitor reactance is low, allowing the oscillator signal to be coupled between the JFET sources. There is no RF degeneration in this circuit except for self-degeneration in the JFET source impedances. Additional RF circuit degeneration is not needed because of the low PM modulation gain of JFETs.

As discussed, bipolar transistors are particularly nonlinear devices and have high PM modulation gains for bias current modulation.

The PM modulation gain may be significantly reduced by using RF circuit degeneration, particularly in the emitter circuit. Healey provides data of PM modulation gain versus bias current for typical bipolar transistors at 30 MHz.[33] A device with a bias current of 5 mA, f_T of 1000 MHz, $r_{bb'}$ of 50 ohms, and a B of 100 has a transconductance PM modulation gain ($d\emptyset/dI_{emitter}$) of approximately 0.045 radians/mA. The same device with a 50 ohm external emitter resistor has a transconductance PM modulation gain of 0.01 radians/mA.[33] It is clear that even moderate emitter degeneration results in a substantial reduction of PM modulation gain. Boychuk also presents data of

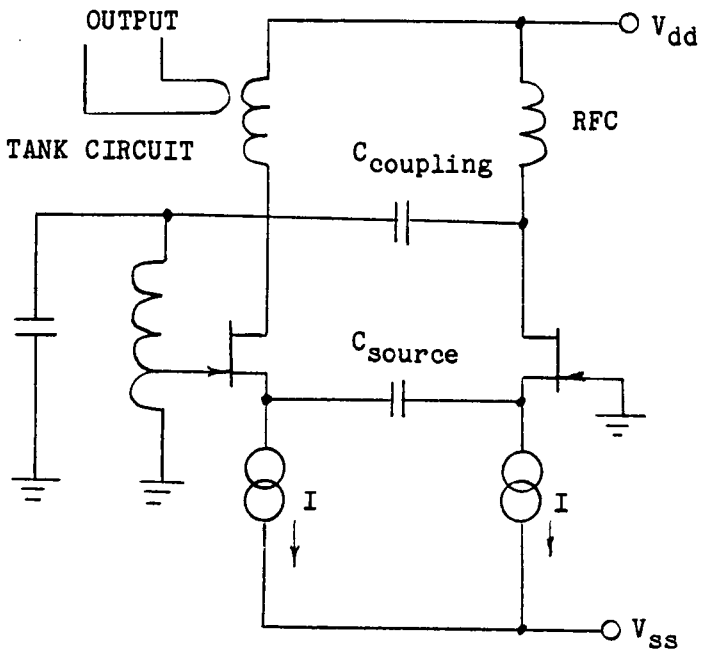


Figure 4.5. Example of Low Frequency Noise Circuit Degeneration.

bipolar transistor transconductance (and input and output impedance) modulation with emitter current for varying degress of emitter degeneration.[39]

Unfortunately, resistive emitter degeneration adds thermal noise to the circuit so the emitter resistance cannot be made arbitrarily large. The author has considered using a sustaining amplifier stage that uses lossless feedback to accomplish device linearization without the addition of noise caused by resistive feedback. Lossless feedback was developed by Norton and uses transformer feedback.[40] This will be discussed later as a suggestion for future work.

Walls gives an empirical expression of close-in phase noise for a common emitter bipolar transistor amplifier operated without emitter degeneration.[41] The expression describes 1/f noise PM device modulation and is given by

$$S_{\phi}(f_m) = 10^{-11} \text{ rad}^2/f_m.^{40} \qquad (4.8)$$

Thus, $S_{\phi}(1 \text{ Hz})$ is empirically -110 dB (relative to 1 rad^2/Hz) and falls at 10 dB/decade until the white additive noise floor is reached. Emitter degeneration can improve this by 30-40 dB.[37] In fact, a 2N3904 isolation amplifier with a 27 ohm emitter resistance is reported to have a close-in phase noise 30 dB below this empirical (non-emitter degenerated) value.[41]

Fortunately, it is very convenient to couple the crystal of a series resonant overtone crystal oscillator circuit to the emitter of a bipolar transistor. This not only maximizes the loaded Q of the crystal because of the low drive impedance seen from the emitter, but

also provides emitter degeneration. The crystal impedance provides emitter degeneration, especially at frequencies off of resonance where the impedance becomes quite large.

Rohde suggests that a series resistor placed between the bipolar transistor collector and the collector tuned circuit used in an overtone crystal oscillator further reduces low frequency noise modulation.[32] Rohde references a report which mathematically demonstrates the reduction of AM-to-PM conversion and the corresponding low frequency modulation.[32]

Low 1/f noise device selection. JFETs generally have the lowest 1/f noise corner frequency of active devices. The corner frequency typically varies from 10 Hz to 10 kHz. Additionally, their low noise currents make them extremely attractive if their input signal source is not low impedance. Further, their improved linearity over bipolar transistors makes them less susceptible to low frequency PM noise modulation. The J308,J309,J310 family and the 2N5397 are good JFETs for low noise oscillators. The J308,J309,J310 family are good for VHF service, and the 2N5397 is good for UHF service. MOSFETS should be avoided as they have very high 1/f noise.

Bipolar transistors may be used effectively in low noise oscillators if they are driven from low impedance sources to shunt the effects of base current noise. Large junction devices generally exhibit less 1/f noise than small junction devices. Thus, a small-signal low noise RF transistor may not be an optimum device for low noise oscillator service because of 1/f noise (23, p. 106).

The 2N5943 transistor, which is a moderately large geometry device, is reported to have low 1/f noise.[38,41] The author has seen a 20 dB noise improvement at 1 kHz from the carrier using the 2N5943 in place of an MRF-901 in a 45 MHz crystal oscillator circuit. The 2N2857 is commonly used in low noise oscillators into the UHF range and has been in use for some time.

High current gain transistors have lower 1/f noise as they have lower surface recombination velocities.[33] However, high B transistors usually have large base-spreading resistances that introduce higher levels of additive white noise into an oscillator circuit. The BC-109C is a high B transistor with low 1/f noise, but it has higher broadband or white noise than the 2N2857 because of its higher base-spreading resistance.[33]

PNP transistors are reported to have lower 1/f noise than NPN transistors.[36] PNP devices are not, however, used as frequently as NPN devices. The 2N4260 is a good PNP transistor for service up into the UHF range.

The optimum bipolar transistor is a medium-to-large geometry device with high B, low base-spreading resistance, and of course a satisfactory gain-bandwidth product. It is important to realize that 1/f noise is very process dependent. It may well be necessary to individually select devices for critical low noise oscillator applications.

Passive devices also exhibit 1/f noise. Silver mica capacitors are reported to have high 1/f noise.[36,37] Similarly, electrolytic and ceramic capacitors are also reported to have high 1/f noise as well as

carbon composition resistors.[36] Reversed biased varactor diodes also exhibit 1/f noise.[42] Finally, hot carrier diodes have low 1/f noise, which makes them desirable limiting elements.[36]

Power Supply Noise Effects

As in low noise low frequency amplifiers, power supply noise can significantly degrade the noise performance of an oscillator. Additive noise effects are not a problem as supply bypassing assures negligible noise at the RF frequencies. However, the low frequency noise of power supplies can cause device transconductance and input and output impedance modulation to occur. Power supply modulation effects are similar to 1/f device noise modulation effects.

Power supply noise effects can be minimized by designing for maximum power supply rejection. The circuit of Figure 4.5 has excellent power supply rejection for the negative supply voltage. This is because of the current source bias. It is interesting to note that this circuit was designed for low 1/f device noise effects, but has excellent power supply rejection as well. Note that the parallel LC tank circuit is capacitively coupled to one of the JFET drains, and this drain is biased through an RF choke to the positive supply voltage. Noise on the positive supply will modulate the drain-gate capacitance of the JFET, causing reactance modulation of the oscillator tank circuit or resonator.

It is recommended that power supply phase noise contributions be measured experimentally to determine if indeed device noise is controlling noise performance. Of course, every effort should be made to

minimize low frequency supply noise using low noise series pass regulator circuits and filtering.

Maximizing In-Circuit Resonator Q

Resonator Choices

The quartz crystal is the highest Q resonator known to man. When operated in the series resonant overtone mode, crystal Q can exceed 1 million. The Quarzkeramik Company makes exceptionally high Q crystals (8, p. 200). Also, the Bliley Company makes high Q crystals. Most crystals for low noise oscillators are AT cuts, but BT and SC cuts are also used.[32,34,43]

Q values up to 3 million are possible for 5th overtone AT cut 5 MHz crystals.[44] Groslambert reports a 5 MHz 5th overtone AT cut crystal with a loaded Q of 1.5 million in an oscillator circuit.[45] Driscoll reports an interesting scheme for actively multiplying the Q of a crystal.[46] This is done using a negative resistance generator in series with the crystal to lower the effective series resistance of the crystal. A 30 MHz crystal with a Q of 2.9×10^5 was Q-multiplied to an effective Q of 1×10^6.[46] Similarly, an 80 MHz crystal was Q-multiplied to an effective Q of 5×10^5. Of equal significance to the process of multiplying crystal Q is the fact that the negative resistance generator used by Driscoll has a phase noise comparable to that of nonregenerative stages.[46] This opens up possibilites for some very low noise crystal oscillator designs.

Transmission lines, helical resonators, and cavities are also high Q resonators, and Q values over 1000 are easy to obtain.

Although not as limited in tuning range as crystals, the tuning range of these resonators is small.

Where wide tuning ranges are required, the LC resonator is usually required. Unfortunately, Q values over 500 are rarely obtained in a circuit. Most LC resonators are parallel circuits, thus Q is maximized by increasing the capacitance to inductance ratio until coil losses become severe. Maximizing the parallel capacitance also minimizes capacitance modulation effects caused by devices coupled to the tank circuit.[6] This effect is caused by low frequency device capacitance modulation and the resultant phase modulation due to varying capacitance in the tank circuit.

The author has considered using a Q-multiplied parallel LC tank circuit in an LC oscillator, which was a suggestion offered by the late Bill Managan. Unfortunately, time did not allow for the design and evaluation of this circuit before the completion of this thesis. It is hoped that a circuit of this type will be as successful as Driscoll's crystal Q-multiplying circuit.[46] This will be suggested later as a topic for future study.

Oscillator Limiting

As previously discussed, some form of controlling oscillator loop gain at unity is required. This is done in many oscillators by letting the active devices cut off or saturate. It is crucial in low noise oscillators that the limiting mechanism does not significantly degrade the loaded Q of the resonator.

Most LC oscillators use a parallel tank circuit for the resonator. It is imperative that oscillator circuitry does not

resistively load the tank circuit, degrading its loaded Q. Devices that saturate or are driven into breakdown will degrade the loaded Q of the parallel tank circuit by shunting resistance across it.

Self-limiting oscillator circuits are commonly used and are usually quite simple. Self-limiting occurs when the input level of a device builds up to the point where the device cuts off for a portion of the signal cycle. As the device becomes cutoff for a larger portion of the cycle, the average transconductance drops. Self-limiting occurs at the signal level that degrades device transconductance to where the overall oscillator loop gain is unity.

If a self-limited stage is used to drive a crystal in a series-mode oscillator circuit, the series impedance driving the crystal will be high during device cutoff. Thus, the average driving impedance of the crystal will be much higher compared to the driving impedance of a class A stage where the device is on for the entire signal cycle. This, of course, will degrade the loaded Q of the crystal.

Driscoll reported a comparison between two 47 MHz crystal oscillators, where one was self-limiting in the crystal driver stage, and the other used a class A crystal driver stage and a separate limiting stage.[43] The single stage self-limiting oscillator has a reported loaded Q of 24,000, whereas the two-stage oscillator with the class A crystal driver has a reported loaded Q of 120,000.[43] Obviously, the oscillator with the higher loaded Q will have lower close-in phase noise. However, self-limiting designs often have lower ultimate noise floors because they typically operate with larger signal levels. The

drive of a class A stage must usually be limited to prevent device cutoff.

The differential limiter is an excellent oscillator limiting element. It provides essentially a fixed square-wave current output for a wide range of input voltages. Because it maintains high input and output impedances during limiting, it is an extremely desirable limiting element. Further, the differential limiter may be driven by large signals, permitting a maximum signal-to-noise ratio for minimum additive noise.

Hot carrier or Schottky diodes may also be used for limiting. These may be placed at a circuit point that is buffered from the resonator to limit signal levels. They may also be placed across a tap that is near ground on a parallel tank circuit. This will load the tank circuit some, but it is possible to load it only slightly.

AGC is sometimes used in oscillators to control loop gain. Here the signal level is rectified and used to control loop gain at unity for a fixed signal level. The use of AGC for oscillator limiting does not appear as popular as other forms of oscillator limiting.

In summary, limiting generally should not occur in the resonator but in a separate isolated stage. This assures maximum in-circuit resonator Q.[6,32] Although a separate limiting stage has been recommended, good oscillator performance has been observed in some oscillators where this was not done. For example, series resonant crystal oscillators that have emitter-coupled bipolar transistor crystal drivers have been operated with the driver cut off for a portion of the signal cycle. Phase noise degradation is not as severe as

expected because of device reactance during cutoff, which acts to maintain coupling to the crystal.[47,48] A pure reactance in series with a resonator will not degrade the Q of the resonator. This may help to explain the surprising performance of some seemingly sloppy oscillator circuits.

Buffer Amplifier Noise Effects

Usually, a buffer amplifier is used to buffer the oscillator output signal from the internal oscillator circuitry. This prevents changing load conditions from introducing phase noise. The buffer amplifier also raises the signal level to the level needed for subsequent circuitry.

The buffer amplifier introduces phase noise of its own. Phase noise is introduced by additive noise and low frequency device and power supply modulation effects. The buffer amplifier should be designed with the same considerations as the oscillator sustaining amplifier to minimize phase noise.

Voltage Controlled Oscillator Considerations

If the resonator resonant frequency is varied by a dc control voltage, an oscillator becomes a VCO. If the tuning range is extremely narrow (below 1 kHz), a crystal may be pulled with a varactor diode. If the tuning range is moderately wide (less than a 10% range), a transmission line resonator may be pulled with a varactor diode. The transmission line resonator may be tuned over a wider range by using switched capacitors at one or both ends. Finally, for

wide tuning ranges, an LC resonant circuit may be tuned using a varactor diode.

Voltage Controlled Oscillator Gain Effects on Phase Noise

It is unfortunate that all VCOs are FM modulators. Any noise on the dc control voltage will result in output frequency fluctuation or phase noise. If the VCO output frequency to input voltage characteristic or gain is high, this effect can become quite severe.

Consider two VCOs with different gains that are fed by the thermal noise voltage of a 1 k ohm resistor. The first oscillator has a gain of 100 kHz/volt, and the second has a gain of 10 MHz/volt. VCO frequency fluctuation noise due to input noise is calculated as

$$S_f(f_m) = [E_n(f_m)K_V]^2, \tag{4.9}$$

where E_n is the input rms noise voltage in a 1 Hz bandwidth and K_V is the VCO gain. From frequency fluctuation noise, the phase noise is found to be

$$S_\phi(f_m) = (1/f_m^2)S_f(f_m) = (1/f_m^2)[E_n(f_m)K_V]^2. \tag{4.10}$$

A plot of the resulting output phase noise for both the low gain and high gain VCO is shown in Figure 4.6. Note that the VCO with the higher gain has much greater output phase noise due to the input noise voltage than the lower gain VCO.

The varactor control voltage can be heavily lowpass filtered to reduce noise. This filtering must not cause significant phase shift within a PLL as loop stability will suffer. However, even if the control voltage is totally filtered into a pure dc voltage, varactors

have an internal thermal noise voltage caused by their bulk resistance that will cause VCO phase noise.

Voltage Controlled Oscillator Frequency Presteering

Minimizing VCO gain usually requires coarse frequency steering of the oscillator tank circuit. This may be done by switching varying amounts of either capacitance or inductance into the circuit. A varactor diode then provides the fine tuning. The switching of capacitance or inductance into the tank circuit may be done using

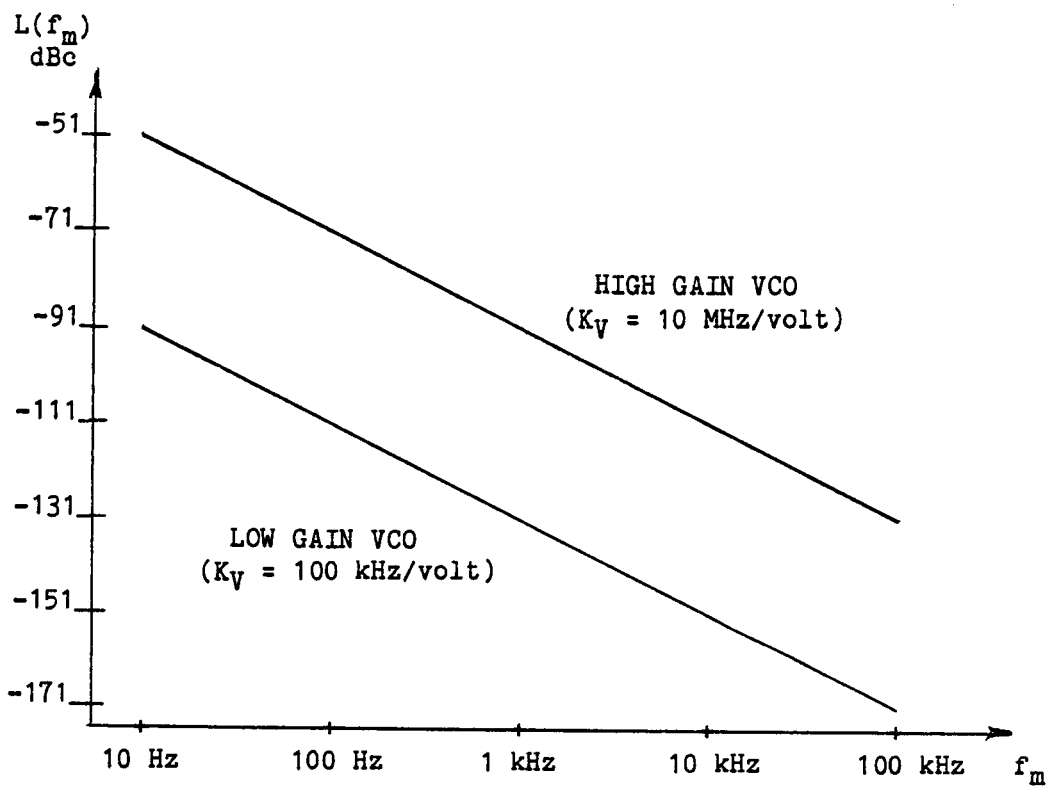


Figure 4.6. Phase Noise of a Low Gain and High Gain VCO Due to Control Voltage Noise Caused by a 1 k Ohm Resistor.

mechanical relays or solid state devices. PIN diodes are commonly used as a solid state RF switch. Unfortunately, they have a series resistance when turned on and an off-capacitance in series with a resistance when turned off, which results in a degradation of tank circuit Q. Further, PIN diodes have a small varactor diode characteristic when reversed biased off that makes the tank circuit susceptible to PIN diode bias voltage noise.

Additional Circuit Considerations

In addition to the VCO gain noise problem, VCOs present additional circuit problems. The varactor diode should not become forward biased or reach breakdown by excessive signal levels. Thus, oscillator signal levels may have to be reduced when using a varactor. Additionally, varactors have much poorer Qs than fixed capacitors. The effect of varactor Q is minimized in low gain VCOs because the varactor has a more limited effect on the resonator. Gallium arsenide varactors have superior Qs over silicon varactors, but they are much more expensive.

Low Noise Oscillator Examples

Because of the extremely high Q of quartz crystals, crystal oscillators exhibit superb phase noise performance. Three crystal oscillators in the 100 MHz range will be compared, each having a considerably different design from the others. Since the next section of this thesis is devoted to an LC VCO that is used in the 45-75 MHz frequency synthesizer, no examples of LC oscillators will be given.

The first oscillator was designed by Rohde and uses a bipolar transistor sustaining amplifier and a bipolar transistor differential limiter.[32] An abbreviated schematic of this oscillator is shown in Figure 4.7.

The sustaining amplifier is a cascode amplifier with current bias. The current bias results in significant degeneration of low frequency noise because of the high low frequency impedance at the emitter of transistor Q1. The parallel tuned circuit tunes the oscillator to the correct overtone of the crystal, which is generally required in overtone oscillators. The 470 ohm resistor in series with the collector of Q2 minimizes AM-to-PM conversion and the resulting up-conversion of low frequency device noise. This was discussed earlier, and Rohde references a computer analysis that verifies this effect.[32] Transistors Q3,Q4 and Q5,Q6 form two differential limiters. One limiter is used in the oscillator feedback loop for levelling, and the other is used as an output buffer amplifier.

This oscillator has a measured SSB phase noise of -112 dBc at 10 Hz, -142 dBc at 100 Hz, and -160 dBc at 1 kHz. The ultimate noise floor is reached at close to 1 kHz and is -160 dBc. This oscillator has the best close-in phase noise performance of the oscillators.

The second oscillator uses a bridged-tee self-limiting configuration with a bipolar transistor cascode sustaining amplifier and was designed by Healey.[34] An abbreviated schematic of this oscillator is shown in Figure 4.8. The cascode arrangement of Q1 and Q2 helps prevent the base-collector capacitance of Q1 from degrading the crystal Q. As the circuit is self-limiting, the transistors are turned

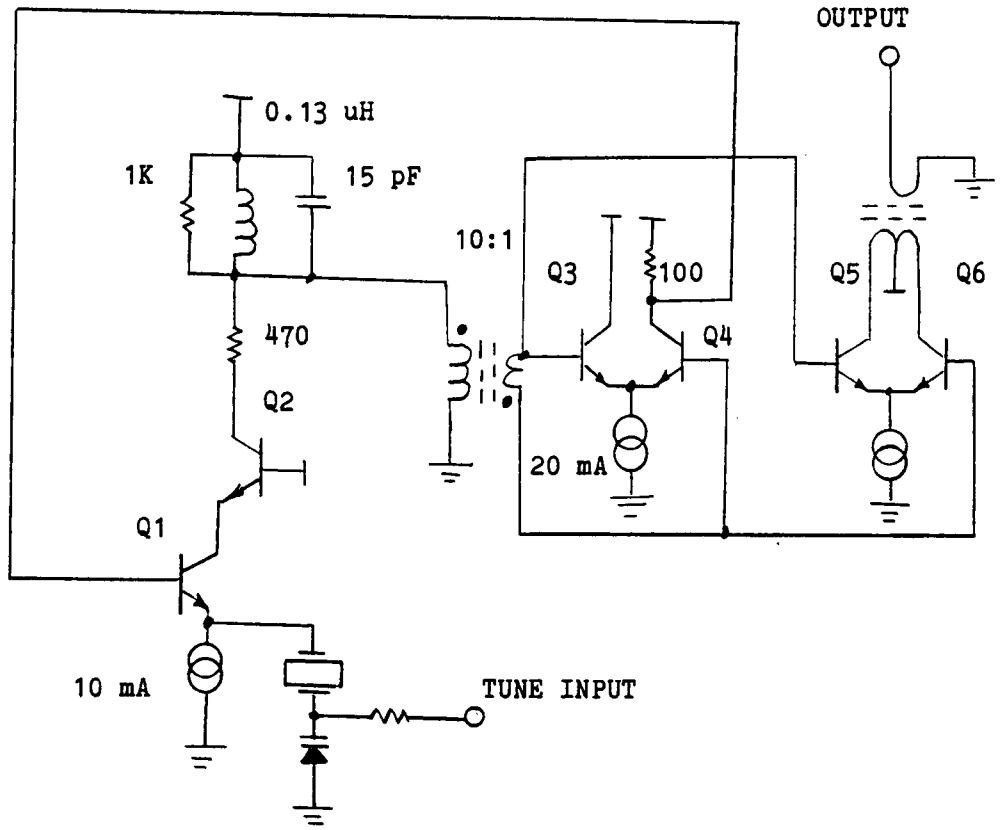


Figure 4.7. Abbreviated Schematic of Rohde's 100 MHz Crystal Oscillator.

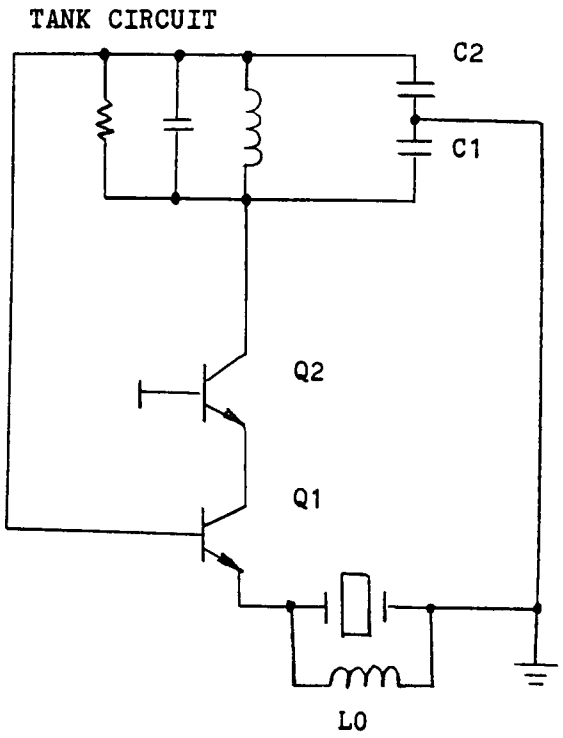


Figure 4.8. Abbreviated Schematic of Healey's 100 MHz Crystal Oscillator.

off for a portion of the signal cycle. Although this degrades crystal Q, the oscillator still has respectable close-in performance.

The phase noise of this oscillator is -132 dBc at 100 Hz, -157 dBc at 1 kHz, and -168 dBc at 10 kHz. The ultimate noise floor is reached at slightly above 10 kHz and is -170 dBc. This oscillator does not have as good a close-in performance as the first oscillator, probably because of degraded crystal Q caused by limiting in the crystal driving stage. It does, however, have a superior ultimate noise floor, due probably to larger oscillator signal levels. Details of output signal coupling were not given in Healey's paper.[34] Link coupling to the tank circuit inductor is probably used with subsequent buffering.

The third oscillator uses all JFETs and was designed by Neubig.[49] An abbreviated schematic of this oscillator is shown in Figure 4.9. The sustaining amplifier is a JFET cascode with a pi-network connected between output and input. The 180° phase shift of the sustaining amplifier combined with the 180° phase shift of the pi-network results in positive feedback. Limiting is provided by Schottky diodes at the pi-network. Output buffering is provided by a grounded gate JFET.

The measured SSB phase noise of this oscillator is -114 dBc at 100 Hz, -140 dBc at 1 kHz, and -147 dBc at 10 kHz. The ultimate noise floor is reached at slightly above 2 kHz and is -147 dBc. This oscillator does not have as low a phase noise as the other two oscillators. This is probably due to degraded crystal Q caused by high JFET source resistance as compared to low bipolar transistor emitter resistance. Additionally, oscillator signal levels are probably

lower, resulting in lower signal-to-noise ratios. This can usually be found to be true in an oscillator with a higher ultimate noise floor.

The topology of this oscillator is very similar to that of Healey's oscillator except for the use of diode limiting. Healey reports another crystal oscillator with the same basic topology, including diode limiting.[50] This oscillator operates at 90 MHz and uses bipolar transistors.

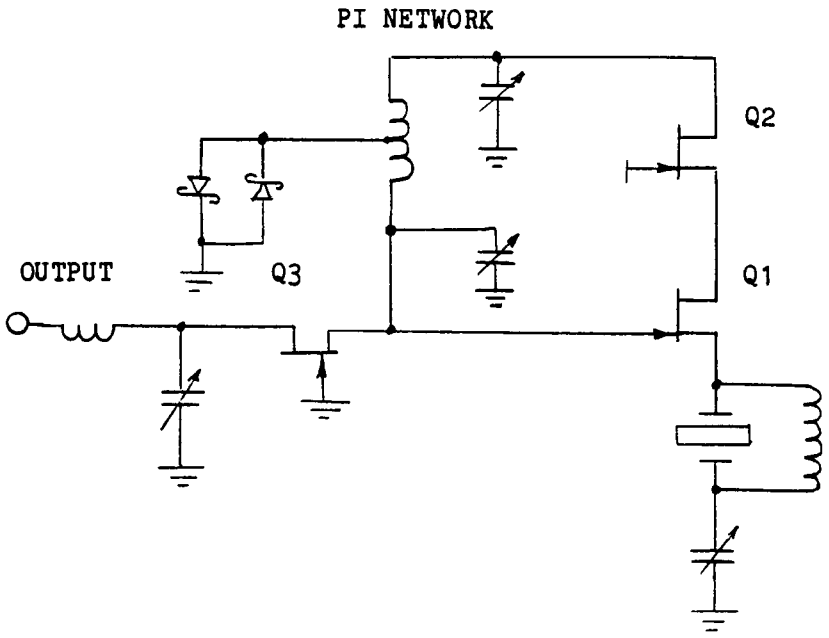


Figure 4.9. Abbreviated Schematic of Neubig's 96 MHz Crystal Oscillator.

5. VOLTAGE CONTROLLED OSCILLATOR IN THE 45-75 MHz SYNTHESIZER

Design Goals

VCO noise requirements can be taken directly from the synthesizer design specifications in Table 1.1 since phase noise above 1 kHz is controlled by the VCO. Phase noise above 1 kHz is controlled by the VCO because the PLL loop bandwidth is well under 1 kHz since loop bandwidth must be less than the reference frequency of 1 kHz. In fact, the selected loop bandwidth is only 10 Hz because of the low dc loop gain. PLL noise performance was not specified at frequencies below 1 kHz because close-in phase noise is not critical in HF communication receiver local oscillator applications.

To accomplish the low noise performance, it is necessary to minimize the gain of the VCO for reasons described in the previous section. A switched inductor design was chosen that limits VCO gain to 100-200 kHz/volt. The inductors will be switched in a binarily coded fashion under control of a ROM that will select the proper inductors based upon the selected frequency of the synthesizer. Fine tuning will be provided by a varactor diode.

The VCO will have two outputs: one output will be the main RF output to the outside world; the other will drive the synthesizer's programmable divider. Both outputs will be well buffered from the oscillator circuitry and from each other. Of course, the VCO will be thoroughly shielded and use careful power supply filtering and bypassing techniques.

Circuit Description

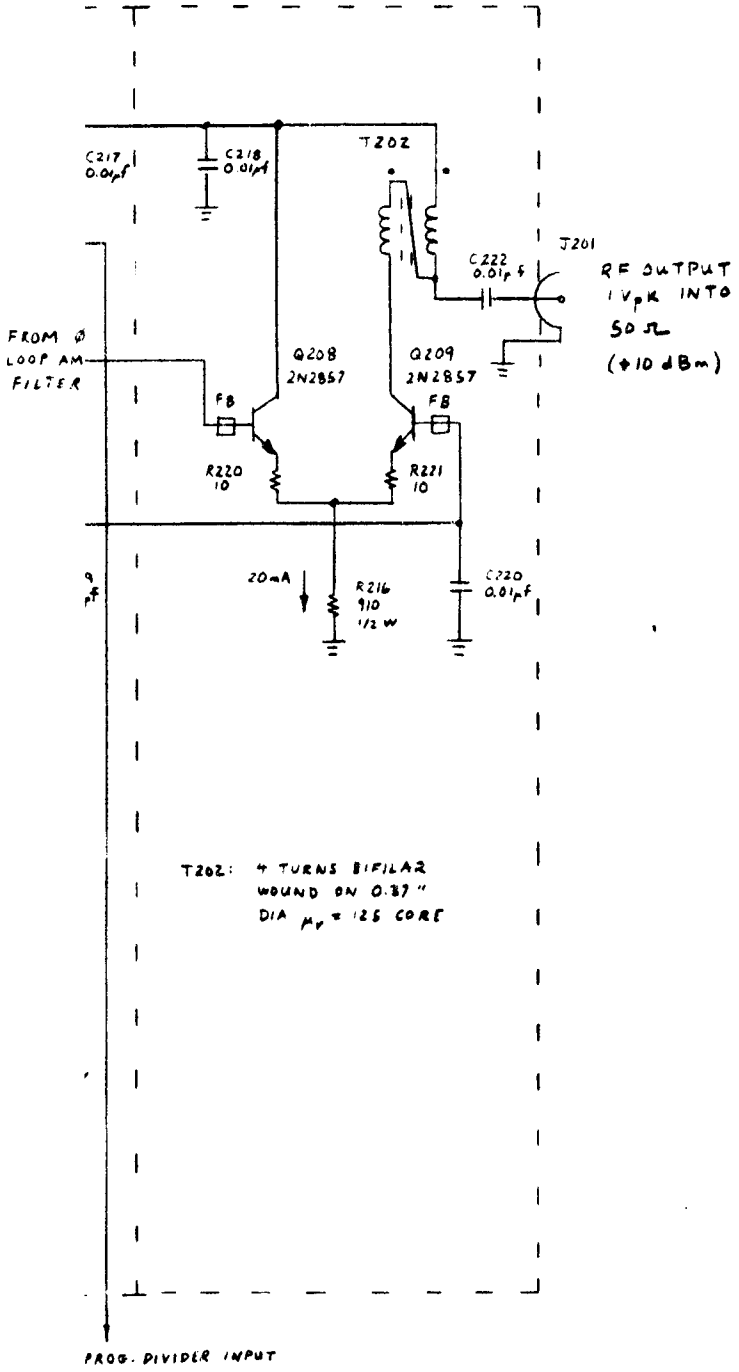
A schematic diagram of the VCO is shown in Figure 5.1. The circuit consists of a JFET differential limiter for the sustaining amplifier, a switched inductor parallel LC tank circuit with varactor diode fine tuning, and two bipolar transistor differential limiters for output signal buffering.

Sustaining Amplifier

The JFET differential limiter consists of JFETs Q201 and Q202. The gate of Q201 is connected to a tap on the fixed tank inductor, L201. The selection of this tap sets the differential limiter RF input voltage. The drain of Q202 is returned to a higher tap on L201 and provides positive feedback to the tank circuit. This tap allows a tank circuit RF voltage that can exceed the power supply limited RF voltage at the drain of Q202.

The JFET differential limiter is current biased by resistors R208 and R209. The high impedance of these resistors provides a high degree of 1/f noise degeneration in the JFETs, minimizing 1/f noise (as well as white noise) modulation of JFET source current. Additionally, the low-valued source coupling capacitor, C212, provides 1/f noise degeneration in the JFETs by preventing low frequency coupling between the JFET sources.

Although fixed JFET source bias resistors have less noise current than bipolar transistor current sources, they place demanding low noise requirements on the negative power supply line. This is because noise variations in the negative supply modulate the bias currents of


C217
0.01μf
C218
0.01μf
T202
J201
C222
0.01μf
RF OUTPUT
1 Vpk INTO
50 Ω
(+10 dBm)
FROM Ø
LOOP AM
FILTER
Q208
2N2857
Q209
2N2857
FB
FB
R220
10
R221
10
20mA
R216
910
1/2 W
C220
0.01μf
T202: 4 TURNS BIFILAR
WOUND ON 0.37"
DIA μr = 125 CORE
PROG. DIVIDER INPUT

the JFETS (Q201 and Q202). Resistor R224 and capacitor C230 form a power supply lowpass filter to help reduce negative power supply noise.

Bipolar transistor current sources were initially designed into the circuit to provide a high degree of power supply rejection. However, they did not appear to improve the noise performance and were believed to have parasitic oscillations at frequencies well above the oscillator frequency. The parasitic oscillations were probably caused by excessive layout conductor length. Bipolar transistor current sources will be utilized in the second generation synthesizer.

The J309 JFET was chosen for Q201 and Q202 as it has good VHF performance, low RF noise, and low 1/f noise. Other similar JFETs, such as the 2N5397, would work well in the circuit. In fact, the HP 8662A synthesized signal generator uses 2N5397 JFETs in a similar circuit for a 320-640 MHz VCO.[6]

Tank Circuit

The tank circuit capacitors consist of C201, C208, and the varactor diode D201. Tank circuit inductors consist of the fixed inductor, L201, and the six PIN diode switched inductors L202-L207. As mentioned, the inductors are binarily weighted and switched in a binary coded fashion under control of a ROM. This ROM is located in the synthesizer programmable divider circuit.

The VCO is preset to within approximately 1 MHz of the desired frequency by the switched inductors. The varactor diodes then provide the fine tuning, which limits the gain of the VCO to between 100-200 kHz. This is sufficiently low for low noise performance.

As discussed, the JFET differential limiter is coupled to the tank circuit by taps on L201. The tap close to ground couples the input of the limiter to the tank circuit, and the higher tap couples the output of the limiter to the tank circuit. In addition to controlling the input and output RF signal levels at the limiter, coupling into the tank circuit by these taps helps buffer the tank circuit from the input and output impedances of the limiter. This is because of the impedance transformation provided by the taps, which results in a higher impedance appearing across the tank circuit.

Buffer Amplifiers

The sustaining amplifier output is taken from the drain of Q201 across resistor R219 and is coupled to the inputs of the bipolar transistor differential limiters by transformer T201. This low impedance voltage signal is used to drive the differential limiters. The programmable divider limiter consists of transistors Q206 and Q207, and the output limiter consists of transistors Q208 and Q209. The outputs of both limiters are taken from the collectors of grounded base transistors to provide isolation from their outputs to the sustaining amplifier. Additionally, the sustaining amplifier output is isolated from the tank circuit by the JFET Q201.

The 2N2857 bipolar transistor was selected for the differential limiter buffer amplifier transistors. This RF device features good noise performance and is optimized for operation in the 10 mA collector current range.

The bipolar transistor differential limiters are operated from a single power supply line and are current-biased by resistors R215 and

R216. Base bias voltage is derived from the resistive divider consisting of R217 and R218 and is heavily bypassed to ground by capacitors C228, C219, and C220. This helps prevent power supply noise modulation of the limiter bias currents by maintaining an essentially constant base bias voltage. Device bias current noise caused by circuit noise and power supply noise has been minimized in both the sustaining amplifier and the buffer amplifiers because it results in phase modulation caused by device nonlinearities. This, of course, raises the phase noise levels, especially at low modulation frequencies because of high levels of 1/f noise and low frequency power supply noise. The phase modulation gain of the differential limiters is reduced by linearizing them with emitter resistors R211, R212, R220, and R221.

Transformer T202 is used to multiply the output current of Q209 and provides a higher output level in output buffer. The output is a square wave of 2 Vpp into 50 ohms. The output of the programmable divider buffer is a square wave of approximately 0.7 Vpp, which is sufficient for driving the programmable divider ECL input stage. Transformers T201 and T202 are wound on ferrite toroids with a relative permeability of approximately 125. T202 is a transmission line type transformer.

Oscillator Circuit Analysis

Tank Circuit

Circuit model and analysis. The tank circuit may be modelled at frequencies near resonance as a parallel circuit consisting of an

inductor, a capacitor, and a resistance. The effective parallel inductance and capacitance set the resonant frequency. The effective parallel resistance divided by the reactance of either the inductance or capacitance sets the loaded Q of the circuit. Further, tank circuit impedance at resonance is equal to the effective tank resistance.

Each element of the tank circuit may be modelled as a series LRC circuit, and series-to-parallel transformations can be used to arrive at the effective parallel tank resistance, inductance, and capacitance. Since PIN diode switching provides coarse tuning in 64 steps, 64 tank circuit calculations are required, each at a different resonant frequency with different circuit elements switched into the circuit. Additionally, since the PIN diodes must be modelled with finite on-resistance as well as finite off-capacitance, it should be clear that the tank circuit calculations are extremely tedious. For this reason, a FORTRAN computer program was written to analyze the tank circuit.

The tank circuit model used in the computer program is shown in Figure 5.2. Note that all inductors are modelled as an inductance in series with a resistance as a result of finite inductor Q. Inductor Q at 50 MHz is used as a program input, and operating Q is calculated by the program based on the assumption that inductor Q increases as the square root of frequency with increasing frequency. Inductor Q increases slightly with increasing frequency because the inductive reactance increases linearly with frequency and the series resistance only increases as the square root of frequency. The resistance of a conductor increases as the square root of frequency because of the skin

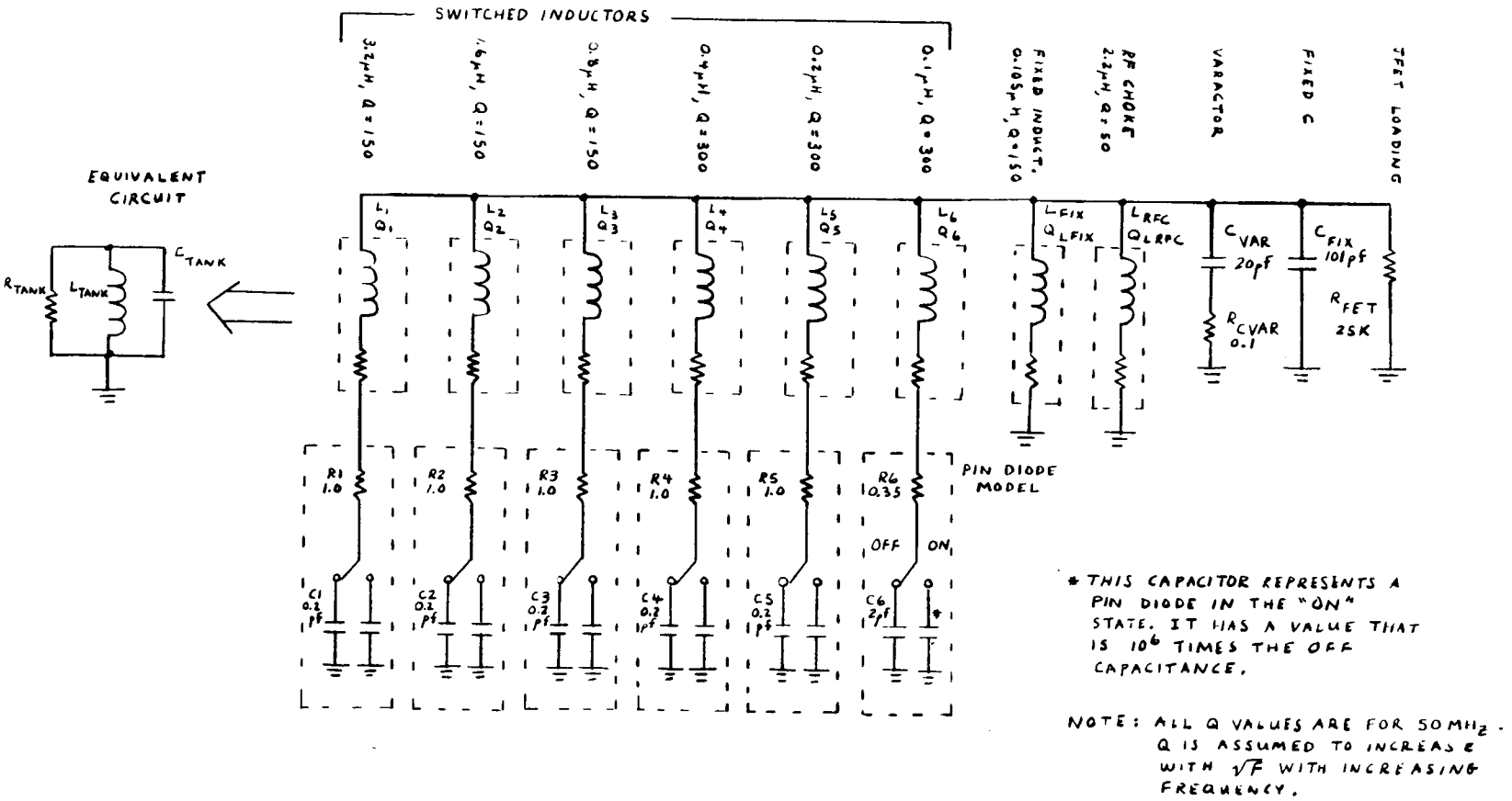


Figure 5.2. Tank Circuit Model Used in the Tank Circuit Analysis Program.

effect. However, inductor Q only increases with frequency until the effects of winding shunt capacitance become significant. Once the operating Q of the inductor is found, the inductor series resistance is calculated in the program as

$$R_{series} = X/Q. \qquad (5.1)$$

The varactor diode is modelled as a fixed capacitor in series with a fixed resistor. Its capacitance is not varied in the program, and it will have a negligible effect on the tank circuit since its capacitance is much less than the capacitance of the fixed capacitor. The fixed capacitor is modelled as a perfect capacitor as its Q is much greater than the inductor Qs.

The PIN diodes are modelled with a fixed resistance (the on-resistance) in series with either off-capacitance or a large on-capacitance approximating a short circuit. A large series on-capacitance was used in place of a short circuit for programming simplicity.

The PIN diode model is very important because in the on-state the PIN diode will effectively degrade the Q of the inductor it is switching because of its series resistance. In the off-state, the PIN diode off-capacitance will add capacitance to the circuit affecting the tank circuit tuning. Additionally, the PIN diode off-capacitance can series resonate with the inductor that it is switching, causing severe circuit loading since a series resonant circuit looks like a low impedance at resonance.

The fixed shunt resistance (RFET) in the tank circuit model represents the parallel combination of the transformed sustaining amplifier input and output resistances. The input and output resistances are transformed because of the tapped connections on L201.

The computer program runs through an algorithm for each of the 64 PIN diode settings. Each series circuit is analyzed, and if the series circuit is inductive, an effective parallel inductance is added to the tank circuit. If the series circuit is capacitive (the case if the PIN diode is off), an effective parallel capacitance is added to the tank circuit. In both cases, an effective parallel resistance is added to the tank circuit.

The series-to-parallel transformations are listed below:

$$\cdot L_{parallel} = [\ (Q_{series}^2 + 1)\ /Q_{series}^2\ ]L_{series}, \qquad (5.2)$$

where $L_{series} = X_{series}/w$ if the series circuit reactance is inductive.

$$\cdot C_{parallel} = [\ Q_{series}^2\ /(Q_{series}^2 + 1)\ ]C_{series}, \qquad (5.3)$$

where $C_{series} = 1/wX_{series}$ if the series circuit reactance is capacitive.

$$\cdot R_{parallel} = [\ 1 + Q_{series}^2\ ]R_{series}, \qquad (5.4)$$

which applies whether the series circuit reactance is inductive or capacitive.

X_{series} is the total reactance of the series circuit, R_{series} is the total resistance of the series circuit, Q_{series} is the Q of the

series circuit, and w is the frequency in radians/second. Note that

$$Q_{series} = X_{series}/R_{series}. \qquad (5.5)$$

Since the series-to-parallel transformations are functions of frequency, the program uses an iterative solution with a starting frequency of 50 MHz. After the first iteration is completed and the total parallel L, R, and C values are calculated, the resonant frequency of the tank circuit is calculated. The resonant frequency is calculated as

$$f_0 = 1 \,/\, (2\pi\sqrt{L_{parallel}C_{parallel}}). \qquad (5.6)$$

The calculated resonant frequency is used in the next iteration instead of 50 MHz for calculating all the frequency sensitive parameters. Three iterations are used, and convergence is assured by printing out the resonant frequency of the last two iterations.

A printout of the computer program results is provided in Figure 5.3 for the VCO tank circuit. This printout is very valuable because it illustrates how the ROM must be programmed to coarse tune the VCO where the printout parameter "N" is the decimal equivalent of the binary code for the PIN diode switching. The printout also gives the effective parallel resistance and tank circuit loaded Q that will be used in signal level calculations, oscillator starting gain calculations, and oscillator noise calculations. A source listing for the program is provided in Appendix A.

PIN diode selection. The perfect PIN diode would have zero on-resistance, infinite off-impedance (including zero capacitance), and

L= 3.20E-06 1.60E-06 8.00E-07 4.00E-07 2.00E-07 1.00E-07 1.05E-07 2.20E-06
C= 2.00E-13 2.00E-13 2.00E-13 2.00E-13 2.00E-13 2.00E-12 2.00E-11 1.01E-10
R= 1.00E+00 1.00E+00 1.00E+00 1.00E+00 1.00E+00 3.50E-01 1.00E-01 2.50E+04
Q= 1.50E+02 1.50E+02 1.50E+02 3.00E+02 3.00E+02 3.00E+02 1.50E+02 5.00E+01

N	LAST F	F	L TOTAL	C TOTAL	R TOTAL	Q
0	4.506428E+07	4.506428E+07	1.002235E-07	1.244532E-10	3.208032E+03	1.130465E+02
1	4.580307E+07	4.580307E+07	9.717986E-08	1.242438E-10	3.181302E+03	1.137507E+02
2	4.649198E+07	4.649198E+07	9.431569E-08	1.242511E-10	3.129779E+03	1.135983E+02
3	4.721210E+07	4.721210E+07	9.161550E-08	1.240408E-10	3.107088E+03	1.143277E+02
4	4.784142E+07	4.784142E+07	8.906570E-08	1.242572E-10	2.979289E+03	1.112803E+02
5	4.854384E+07	4.854384E+07	8.665391E-08	1.240463E-10	2.962985E+03	1.121056E+02
6	4.919512E+07	4.919512E+07	8.436930E-08	1.240543E-10	2.926120E+03	1.122033E+02
7	4.988202E+07	4.988202E+07	8.220205E-08	1.238425E-10	2.911950E+03	1.130257E+02
8	5.043280E+07	5.043280E+07	8.014265E-08	1.242654E-10	2.770766E+03	1.091046E+02
9	5.110409E+07	5.110409E+07	7.818461E-08	1.240531E-10	2.763038E+03	1.100601E+02
10	5.172278E+07	5.172278E+07	7.631996E-08	1.240619E-10	2.737879E+03	1.103861E+02
11	5.238096E+07	5.238096E+07	7.454217E-08	1.238487E-10	2.730997E+03	1.113181E+02
12	5.294049E+07	5.294049E+07	7.284537E-08	1.240687E-10	2.653610E+03	1.095134E+02
13	5.358587E+07	5.358587E+07	7.122406E-08	1.238548E-10	2.648868E+03	1.104596E+02
14	5.417682E+07	5.417682E+07	6.967335E-08	1.238644E-10	2.628839E+03	1.108419E+02
15	5.481099E+07	5.481099E+07	6.818872E-08	1.236495E-10	2.624584E+03	1.117636E+02
16	5.525048E+07	5.525048E+07	6.676778E-08	1.242800E-10	2.006157E+03	8.655297E+01
17	5.587230E+07	5.587230E+07	6.540315E-08	1.240648E-10	2.014500E+03	8.773891E+01
18	5.643800E+07	5.643800E+07	6.409319E-08	1.240752E-10	2.013108E+03	8.857346E+01
19	5.705013E+07	5.705013E+07	6.283466E-08	1.238590E-10	2.020877E+03	8.972307E+01
20	5.755552E+07	5.755552E+07	6.162465E-08	1.240828E-10	1.992351E+03	8.940145E+01
21	5.815792E+07	5.815792E+07	6.046033E-08	1.238660E-10	1.999915E+03	9.052161E+01
22	5.870209E+07	5.870209E+07	5.933919E-08	1.238772E-10	1.998335E+03	9.130473E+01
23	5.929603E+07	5.929603E+07	5.825887E-08	1.236593E-10	2.005431E+03	9.239323E+01
24	5.972915E+07	5.972915E+07	5.721690E-08	1.240918E-10	1.968968E+03	9.169549E+01
25	6.031386E+07	6.031386E+07	5.621182E-08	1.238735E-10	1.976361E+03	9.277728E+01
26	6.083831E+07	6.083831E+07	5.524145E-08	1.238856E-10	1.975114E+03	9.353410E+01
27	6.141558E+07	6.141558E+07	5.430401E-08	1.236663E-10	1.982088E+03	9.458727E+01
28	6.187754E+07	6.187754E+07	5.339789E-08	1.238939E-10	1.957751E+03	9.430189E+01
29	6.244715E+07	6.244715E+07	5.252148E-08	1.236739E-10	1.964562E+03	9.533147E+01
30	6.295423E+07	6.295423E+07	5.167337E-08	1.236869E-10	1.963139E+03	9.604606E+01
31	6.351726E+07	6.351726E+07	5.085223E-08	1.234658E-10	1.969601E+03	9.705025E+01

Figure 5.3. Printout of the Tank Circuit Analysis Program Results.

N	LAST F	F	L TOTAL	C TOTAL	R TOTAL	Q
32	6.428579E+07	6.428579E+07	5.005806E-08	1.224436E-10	2.019843E+03	9.989614E+01
33	6.484574E+07	6.484574E+07	4.928703E-08	1.222207E-10	2.025944E+03	1.008866E+02
34	6.533971E+07	6.533971E+07	4.853941E-08	1.222338E-10	2.023683E+03	1.015526E+02
35	6.589381E+07	6.589381E+07	4.781413E-08	1.220098E-10	2.029498E+03	1.025198E+02
36	6.632148E+07	6.632148E+07	4.711022E-08	1.222410E-10	2.005833E+03	1.021752E+02
37	6.686938E+07	6.686938E+07	4.642672E-08	1.220162E-10	2.011568E+03	1.031240E+02
38	6.734886E+07	6.734886E+07	4.576276E-08	1.220302E-10	2.009270E+03	1.037566E+02
39	6.789158E+07	6.789158E+07	4.511754E-08	1.218044E-10	2.014766E+03	1.046847E+02
40	6.824484E+07	6.824484E+07	4.449011E-08	1.222467E-10	1.988216E+03	1.042198E+02
41	6.878132E+07	6.878132E+07	4.388004E-08	1.220204E-10	1.993906E+03	1.051447E+02
42	6.924704E+07	6.924704E+07	4.328647E-08	1.220353E-10	1.991825E+03	1.057592E+02
43	6.977890E+07	6.977890E+07	4.270873E-08	1.218079E-10	1.997296E+03	1.066650E+02
44	7.017522E+07	7.017522E+07	4.214624E-08	1.220432E-10	1.976259E+03	1.063460E+02
45	7.070198E+07	7.070198E+07	4.159836E-08	1.218151E-10	1.981663E+03	1.072364E+02
46	7.115539E+07	7.115539E+07	4.106454E-08	1.218309E-10	1.979533E+03	1.078222E+02
47	7.167799E+07	7.167799E+07	4.054424E-08	1.216016E-10	1.984751E+03	1.086954E+02
48	7.193755E+07	7.193755E+07	4.003736E-08	1.222541E-10	1.749845E+03	9.669382E+01
49	7.245429E+07	7.245429E+07	3.954261E-08	1.220244E-10	1.756789E+03	9.759112E+01
50	7.289552E+07	7.289552E+07	3.905993E-08	1.220414E-10	1.757447E+03	9.823582E+01
51	7.340854E+07	7.340854E+07	3.858890E-08	1.218105E-10	1.764176E+03	9.911815E+01
52	7.377728E+07	7.377728E+07	3.812911E-08	1.220501E-10	1.750664E+03	9.904749E+01
53	7.428605E+07	7.428605E+07	3.768013E-08	1.218185E-10	1.757245E+03	9.991545E+01
54	7.471664E+07	7.471664E+07	3.724161E-08	1.218364E-10	1.757632E+03	1.005315E+02
55	7.522207E+07	7.522207E+07	3.681317E-08	1.216036E-10	1.764029E+03	1.013858E+02
56	7.551306E+07	7.551306E+07	3.639440E-08	1.220566E-10	1.749516E+03	1.013168E+02
57	7.601396E+07	7.601396E+07	3.598513E-08	1.218233E-10	1.755906E+03	1.021657E+02
58	7.643422E+07	7.643422E+07	3.558496E-08	1.218423E-10	1.756164E+03	1.027616E+02
59	7.693212E+07	7.693212E+07	3.519359E-08	1.216078E-10	1.762389E+03	1.035978E+02
60	7.727649E+07	7.727649E+07	3.481075E-08	1.218518E-10	1.749470E+03	1.035061E+02
61	7.777081E+07	7.777081E+07	3.443614E-08	1.216165E-10	1.755580E+03	1.043301E+02
62	7.818172E+07	7.818172E+07	3.406950E-08	1.216365E-10	1.755618E+03	1.049009E+02
63	7.867334E+07	7.867334E+07	3.371060E-08	1.214000E-10	1.761584E+03	1.057133E+02

Figure 5.3. (Continued)

no large signal limitations. PIN diodes that optimize any one of these parameters are available. For example, low on-resistance PIN diodes will usually have a high off-capacitance. Conversely, low off-capacitance PIN diodes will usually have a high series resistance. Finally, an otherwise desirable PIN diode may perform poorly under large RF signal conditions.

The RF signal being controlled by a PIN diode must not severely modulate the stored charge in the intrinsic region of the diode. The negative going RF half-cycle will pull charge out of the intrinsic region. If the charge is completely removed, the diode becomes an open circuit.

The intrinsic region charge is stored by the dc bias current and the finite lifetime of the carriers. To prevent the RF signal from completely removing the stored charge, the following condition must be met:

$$I_F t > I_{RF}(pk)/(\pi f), \tag{5.7}$$

where I_F is the dc bias current, t is the carrier lifetime, I_{RF} is the peak RF signal current, and f is the frequency in Hz (51, pp. 80-81). Restated as a design equation,

$$I_F > I_{RF}(pk)/(\pi f t). \tag{5.8}$$

Listed in Table 5.1 are several useful PIN diodes for RF switching with specified on-resistance, off-capacitance, minority carrier lifetime, and the required bias current for the stated

Table 5.1. Common Switching PIN Diode Parameters.

Parameter	Motorola MPN-3401	HP 5082-3002	HP 5082-3188
On-resistance (max)	0.7 ohms	1.0 ohms	0.6 ohms
Off-capacitance (max)	1.0 pF	0.2 pF	1.0 pF
Stated bias current	10 mA	100 mA	10 mA
Minority carrier lifetime (min)	40 ns (meas by author)	100 ns	40 ns (typ)
Peak RF current at 50 MHz for depleting stored charge	62.8 mA (meas by author)	1.57 A	62.8 mA

Sources: Motorola Inc., Motorola RF Data Manaual. Phoenix, Arizona, 1981.

Hewlett-Packard, Diode and Transistor Designer's Catalog 1982-1983. Palo Alto, California, 1982.

on-resistance. Also included in the table is the maximum 50 MHz RF signal that can be switched for the stated bias current.

PIN diode D202 switches the greatest amount of RF current in the VCO because it switches the lowest valued inductor. It is turned on for frequencies above approximately 60 MHz and must handle about 300 mA of peak RF current. Two Motorola MPN-3401 PIN diodes in parallel are used for D201. These diodes are operated at 100 mA, which assures adequate large signal handling capability. The fact that they are operated at such a high current also assures that the 100 mA of bias current will divide evenly between the two diodes. A 0.35 ohm on-resistance and a 2 pF off-capacitance were used to model D202 in the tank circuit analysis program.

The HP 5082-3002 PIN diode was selected for the remaining PIN diodes in the VCO. Although they are relatively expensive, especially compared to the Motorola MPN-3401, they proved to be a good choice. The Motorola MPN-3401 diode off-capacitance will almost series resonate with the larger inductors. For this reason, the low off-capacitance HP diodes are required. These diodes are biased at 100 mA, which assures minimum on-resistance and adequate large signal handling capabilities. A 1 ohm on-resistance and a 0.2 pF off-capacitance were used to model the HP 5082-3002 PIN diodes in the tank circuit analysis program.

Varactor diode selection. The varactor diode must pull the VCO frequency approximately 1 MHz at the worst case operating frequency of 45 MHz. This can be seen from the tank circuit analysis printout of

Figure 5.3 as a requirement to tune the VCO between coarse frequency settings.

The required varactor capacitance change is found by approximating the resonant frequency versus tank capacitance function as a linear function, which is realistic over the small frequency span of 1 MHz. Thus, the required varactor capacitance change is

$$\Delta C = \Delta f / (\delta f / \delta C), \tag{5.9}$$

where

$$\delta f / \delta C = \delta / \delta C \left[1 / (2\pi\sqrt{LC}) \right]$$

$$= -C^{-3/2} / (4\pi\sqrt{L}). \tag{5.10}$$

Substituting Equation 5.10 into Equation 5.9 gives the design equation,

$$\Delta C = -\Delta f \left[4\pi\sqrt{L}\, C^{3/2} \right]. \tag{5.11}$$

L and C are the total parallel tank inductance and capacitance, respectively. Δf is the frequency change in Hz caused by a ΔC capacitance change in farads.

Evaluating this expression for the worst case condition (the condition requiring the largest ΔC) of 45 MHz gives

$$\Delta C = 1 \text{ MHz} \left[4\pi\sqrt{0.1 \text{ uH}} \cdot (125\text{pF})^{3/2} \right]$$

$$= 5.6 \text{ pF}. \tag{5.12}$$

Two Motorola MV-109 varactors in parallel will provide a capacitance

of 20 pF at 13 V and 14 pF at 20 V, which is satisfactory (52, p. 19:33). This tuning voltage range was chosen because 12 V or more is needed to prevent varactor diode forward bias, and the loop amplifier/filter stage is limited to about 21 V maximum output.

Operating the varactor diodes at these large bias voltages has both advantages and disadvantages. The disadvantage is the capacitance change per volt becomes smaller at higher bias voltages. The advantage is that varactor Q increases at higher bias voltages. This is because the bulk resistance remains essentially constant, while the capacitance decreases at higher bias voltages.

The Motorola MV-109 varactor has a Q of approximately 2200 at 50 MHz at a reverse bias of 12 V (52 p. 19:34). A value of 20 pF (13 V reverse bias) and a series resistance of 0.1 ohms are used to model the two paralleled varactors in the tank circuit analysis program. The series resistance selected actually implies a Q at 50 MHz of less than 2200.

The VCO gain is approximately the 1 MHz tuning range divided by the 7 V tuning voltage range, or about 150 kHz/volt. This is within the desired 100-200 kHz/volt range. The VCO gain will be higher for higher frequencies because the tank circuit inductance decreases with increasing coarse frequency selections, while the tank circuit capacitance remains constant. Additionally, the VCO gain will be higher at the minimum control voltage because the varactor capacitance versus voltage curves are steeper at lower bias voltages.

Inductor selection. Inductor values were selected after several trial and error runs of the tank circuit analysis program. It was

necessary, of course, to include the PIN diode parameters as PIN diode series resistance limits how much the tank circuit C/L ratio can be maximized. This is because PIN diode series resistance causes a decrease in effective inductor Q as the inductor value is lowered. A total tank circuit capacitance of 125 pF was obtainable without significant PIN diode Q degradation in the switched inductors. This is believed to be high for a 45-75 MHz oscillator, which is desirable as it assures a low impedance tank circuit that is not as strongly affected by resistive and capacitive loading introduced by the sustaining amplifier.

L201, L202, and L203 are the lowest valued inductors and dominate the Q and parallel resistance (at resonance) of the tank circuit. These are single-layer air-wound coils using silver plated wire. A length-to-diameter ratio of 0.8 and a turns spacing greater than twice the conductor diameter were used. Additionally, these inductors were also placed as far from metal objects as possible to minimize eddy current losses. All of these inductor construction practices are discussed at length in Terman's classic Radio Engineer's Handbook (54, pp. 74-90). The intent, of course, is to maximize inductor Q.

It was necessary to place a 0.15 ohm fixed resistance in series with L201 to make its Q comparable to the effective Q of the switched inductors. If this is not done, the tank circuit resistance at resonance becomes too large at 45 MHz when no inductors are switched into the circuit. This will cause a tank circuit signal level that is too large. L201 was modelled with a Q of 150 to consider the effects of this fixed resistance.

L204 is single-layer, air-wound, and has a length-to-diameter ratio that is somewhat above the approximately optimum ratio of one-half as mentioned by Terman (54, p. 74). Finally, L205-L207 are wound on powdered iron toroidal cores as their Q is not very important because of their high inductance value and limited effect on the tank circuit. The Q of the air-wound inductors is estimated at 300, and the Q of the toroidal inductors is estimated at 150. These values were used in the tank circuit analysis program for the inductors except for L201. As mentioned, the Q of L201 was degenerated to about 150 by a 0.15 ohm fixed series resistance.

Oscillator Starting Gain

In order to assure oscillation, it is necessary that the oscillator loop gain is greater than unity during oscillator startup. Once the oscillator signal has risen to the designed level, limiting within the oscillator sustaining amplifier will control the loop gain at precisely unity. During startup, the sustaining amplifier functions as a linear small signal amplifier, so small signal analysis is sufficient for determining oscillator starting gain.

To evaluate the oscillator starting gain, the voltage gain between the gate of Q201 and the n_1 or gate tap of L201 is determined. The gain between the gate voltage of Q201 and the total tank circuit voltage is given by

$$V_{tank}/V_{gate} = g_m/2 \left[n_2/n_{total} \right] R_{tank}, \qquad (5.13)$$

where g_m is the operating transconductance of Q201 and Q202, n_2 is the number of turns in L201 from ground to the drain tap, n_{total} is the

total number of turns in L201, and R_{tank} is the tank circuit equivalent parallel resistance. Note that the ratio of n_2 to n_{total} describes the current gain from the drain tap of L201 to the top of L201.

The gain between the gate of Q201 back around to the gate tap of L201 (the tap loaded with the input impedance of Q201) is the oscillator loop gain and is given by

$$G = V_{tank}/V_{gate} \left[n_1/n_{total} \right]$$

$$= g_m/2 \left[n_1 n_2/n_{total}^2 \right] R_{tank}. \qquad (5.14)$$

All terms of the expression were previously described, except n_1 which is the number of turns in L201 from ground to the gate tap. The assumption has been made that the operating transconductances of Q201 and Q202 are equal.

The minimum transconductance of Q201 and Q202 at 8 mA of drain current is given by

$$g_m(8\ mA) = \sqrt{8\ mA/10\ mA} \cdot g_m(10\ mA), \qquad (5.15)$$

where $g_m(10\ mA)$ is the minimum transconductance at a drain current of 10 mA. From the Siliconix JFET data book, $g_m(10\ mA)$ is guaranteed to be at least 10 m℧ for the J309 JFET.[55] Evaluating Equation 5.15 gives

$$g_m(8\ mA) = \sqrt{8\ mA/10\ mA} \cdot 10\ m℧$$

$$= 8.94\ m℧. \qquad (5.16)$$

Substituting the transconductance value and the other parameters into Equation 5.14 gives the starting gain,

$$G = g_m/2 \left[n_1 n_2 / n_{total}^2 \right] R_{tank}$$

$$= 8.94\ m\mho/2 \left[(1.75)(3.25)/(4)^2 \right] 1700\ \text{ohms}$$

$$= 2.7. \qquad (5.17)$$

The value for R_{tank} was taken from the minimum value of R_{tank} in the tank circuit analysis results of Figure 5.3. Note that the oscillator loop gain is greater than unity, indicating that oscillation will start. Interestingly enough, the gate tap on L201 had to be increased from its initial 0.5 turns to sustain oscillation during testing. This problem was quickly solved by evaluating the oscillator starting gain and raising the gate tap.

Oscillator Signal Levels

It is important to evaluate signal levels within the oscillator to ensure proper circuit operation and to estimate oscillator phase noise. Note that measured signal levels are given on the VCO schematic of Figure 5.1 for the 45-75 MHz frequency range.

If the sustaining amplifier (Q201 and Q202) operates as a perfect limiter, a square wave of current is fed from the drain of Q202 into the tank circuit. Only the fundamental frequency component of this square wave is important as the high Q tank circuit will reject the harmonic components. The ratio of the peak sinusoidal fundamental component to the peak square wave amplitude is $4/\pi$, which is found by evaluating the Fourier series of a square wave.

The total tank circuit voltage is

$$V_{tank(pk)} = n_2/n_{total}\ (4/\pi)\ I_{pk}\ R_{tank}, \qquad (5.18)$$

where n_2 is the number of turns in L201 from ground to the drain tap, n_{total} is the total number of turns in L201, I_{pk} is the peak amplitude of the current square wave at the drain of Q202, and R_{tank} is the total tank circuit parallel resistance. The factor $4/\pi$ describes the ratio of the limiter fundamental frequency amplitude to the total square wave amplitude as previously described. The total tank circuit voltage is important as it controls the PIN diode RF currents and the varactor diode RF voltage.

It was observed that the total tank circuit voltage was less than the calculated value. The measured tank voltage was 10 Vpk at 45 MHz, dropping to 5 Vpk at 75 MHz, compared to calculated values of almost twice these levels. This error is probably due to imperfect limiting action in Q201 and Q202, calculations of tank circuit resistance that are high, and measurement error. The sustaining amplifier signal levels were also measured to be approximately one-half of the calculated values, which is expected since they are developed by taps on L201.

The voltage at the drain of Q202 is given by

$$V_{drain(pk)} = V_{tank(pk)}\ n_2/n_{total}$$

$$= [\ n_2/n_{total}\ ]^2\ (4/\pi)\ I_{pk}\ R_{tank}. \qquad (5.19)$$

The RF voltage at the drain of Q202 must be less than approximately 12 Vpk to prevent saturation of Q202. Note the voltage at the drain

of Q202 goes equally above and below the supply voltage (15 V) because of the RF choke, L208.

The voltage at the gate of Q201 is given by

$$V_{gate(pk)} = V_{tank(pk)}\ n_1/n_{total}$$

$$= n_1 n_2/n_{total}^2\ (4/\pi)\ I_{pk}\ R_{tank}, \qquad (5.20)$$

where n_1 is the number of turns from ground to the gate tap in L201. The RF gate voltage is important as it controls the RF signal-to-noise ratio and correspondingly the phase noise of the sustaining amplifier. Further, the gate voltage must not be so large as to cause device breakdown or saturation.

Finally, the input voltage of the output limiters is given by

$$V_{limiter(pk)} = 0.5\ I_{pk}\ R219, \qquad (5.21)$$

where the factor 0.5 describes the turns ratio of T201. I_{pk}, again, is the peak value of the current square wave at the drain of Q202. This expression assumes that the input impedance of the output limiters is much greater than R219/4, the driving or source impedance. The limiter input voltage is important to evaluate limiter phase noise contributions.

The peak value of the current square wave at the drain of Q202 (I_{pk}) is equal to one-half of the total current supplying the Q201 and Q202 differential limiter. Since each device is operated at 8 mA, the total current is 16 mA, which makes I_{pk} equal to 8 mA pk. Perfect limiting has been assumed.

Oscillator Noise Analysis

In this section, phase noise is approximated using Leeson's model for the oscillator stage.[29] Then noise calculations are presented for the output buffer amplifier phase noise contribution. Finally, the phase noise of both the oscillator section and output buffer amplifier is combined to find the total oscillator phase noise. Phase noise will be calculated at 45 MHz. Phase noise at 75 MHz will be slightly higher because of lower signal levels and the higher carrier frequency.

The effects of device nonlinearity and the resulting phase modulation caused by circuit noise is considered by using the phase perturbation spectrum presented in Leeson's model.[29] This noise spectrum increases at low frequencies because of 1/f noise device phase modulation and has a higher white noise level than implied by pure linear additive noise because of broadband noise phase modulation.

Oscillator Stage

The oscillator stage consists of the sustaining amplifier (Q201 and Q202) and the tank circuit. The output of this stage is the voltage signal appearing across R219. Output phase noise spectral density from Leeson's model is

$$L(f_m) = 1/2\ (E_n/E_{sig})^2\ [\ 1 + f_c/f_m\ ][\ 1 + f_m^{-2}(f_0/2Q_L)^2\ ], \qquad (5.22)$$

which was presented earlier in Equation 4.7.

E_n is the effective input RF noise at the gate of Q201 and must include the effects of both Q201 and Q202. Initially, JFET noise was calculated from van der Ziel's JFET noise model.[56] However, the gate current noise due to gate-source capacitive coupling to the channel was found to be unrealistically high. The model is apparently not accurate at 45 MHz.

Noise figure data from the Siliconix JFET data book was used to find the equivalent input noise of each JFET.[55] A noise figure of 4 dB for a source resistance of approximately 100 ohms and a drain current of 8 mA was taken from the data book.[55] This implies an equivalent noise voltage of approximately 1.6 $nV/\sqrt{Hz}$ for each JFET. Since the noise of each JFET is uncorrelated, the effective input noise at the gate of Q201 is approximately 2.3 $nV/\sqrt{Hz}$, which is the square root of the sum of the squared noise voltages of both JFETs. An equivalent noise voltage of 3 $nV/\sqrt{Hz}$ was chosen because the actual input source impedance is closer to 500 ohms than 100 ohms, as can be calculated by the impedance transformation of the tank circuit parallel resistance as seen from the gate of Q201. The higher source impedance results in a larger noise voltage component due to gate current noise.

It is necessary to use a value of E_n greater than the actual value because of broadband noise modulation effects as discussed by Leeson.[29] A value for E_n of 4 $nV/\sqrt{Hz}$ was chosen and is felt to be reasonable. The low frequency phase noise corner frequency, f_c, is perhaps the hardest parameter to estimate for use in Leeson's

oscillator model. A value of 1 kHz was chosen to represent the 1/f noise in both of the JFETs.

A loaded Q of 100 was chosen to use in Leeson's model. This is representative of the tank circuit Q as tabulated in Figure 5.3. Since the measured oscillator signal levels were lower than the calculated signal levels, the measured level of RF gate voltage at Q201 will be used for the value of E_{sig} in Leeson's model. At 45 MHz this level is 3 Vrms, and it drops to approximately 1.5 Vrms at 75 MHz.

The oscillator phase noise (excluding the buffer amplifier noise) at an operating frequency of 45 MHz is

$$L(f_m) = 1/2\ (E_n/E_{sig})^2\ [\ 1 + f_c/f_m\ ]\ [\ 1 + f_m^{-2}(f_0/2Q_L)^2\ ]$$

$$= 1/2\ ((4\ nV/\sqrt{Hz})/3\ V)^2[\ 1 + 1\ kHz/f_m\ ][\ 1 + f_m^{-2}(45\ MHz/(2 \cdot 100))^2]. \quad (5.23)$$

This expression will be plotted later along with the phase noise contribution of the output buffer amplifier.

Output Buffer Stage

Since programmable divider phase noise is not significant at frequencies well above the PLL loop bandwidth, the phase noise of the programmable divider output buffer will not be analyzed. Again, as mentioned earlier, PLL phase noise at frequencies above 1 kHz will be almost totally dominated by VCO phase noise. It is then important to evaluate the effects of the main VCO output buffer amplifier phase noise.

Output buffer phase noise analysis is much simpler than the phase noise analysis of the oscillator stage of the VCO. This is because there is no frequency selective feedback involved in the buffer amplifier. The phase noise contribution of the output buffer is caused by additive noise and by phase modulation of the signal due to device nonlinearities and device bias fluctuations. The phase modulation effect can be considered just as the phase perturbation signal is modelled in Leeson's model.[29] The phase noise introduced in a signal passing through the output buffer can be given by

$$L(f_m) = 1/2\ (E_n/E_{sig})^2\ [\ 1 + f_c/f_m\ ], \qquad (5.24)$$

where, as in Leeson's model, E_n is the equivalent input noise voltage, E_{sig} is the input signal level, and f_c is the low frequency phase noise corner frequency. This expression describes the increase in close-in phase noise caused by 1/f device noise and the resulting phase modulation it causes as a result of device nonlinearities. Again, as in Leeson's model, E_n should be taken somewhat higher than the actual noise value because of the increase in the noise level caused by broadband noise mixing into the frequencies of interest (frequencies near the carrier). Further, a higher value of E_n can be used to accommodate phase modulation caused by device bias noise at frequencies above the low frequency corner, f_c. Exactly how much to increase E_n from its actual value depends on both the magnitude of circuit noise (particularly at low frequencies) and the intermodulation performance or linearity of the active devices.

From the Motorola RF data book, the noise figure of the 2N2857 transistors (Q208 and Q209) is estimated to be approximately 4 dB at a collector current of 10 mA with a source impedance of approximately 100 ohms (52, pp. 17:4). The source impedance of Q208 is approximately 100 ohms, and the source impedance of Q209 is 0 ohms. The noise figure data implies an equivalent noise voltage of approximately 1.6 $nV/\sqrt{Hz}$ per device. Since the noise in Q208 and Q209 is uncorrelated, the effective input noise is then increased by the square root of two, making it 2.3 $nV/\sqrt{Hz}$. The thermal noise contributions of R220 and R221, which are 10 ohm resistors, do not significantly change the equivalent input noise. A value of 3 $nV/\sqrt{Hz}$ was chosen for E_n and allows for noise intermodulation effects.

The output buffer input signal level from Equation 5.21 is approximately 1 Vrms. This was also the measured value of the signal. Finally, a value of f_c of 10 kHz was chosen to represent the 1/f noise corner in the 2N2857 bipolar transistors.

The output buffer phase noise is then given by

$$L(f_m) = 1/2\ (E_n/E_{sig})^2\ [\ 1 + f_c/f_m\ ]$$

$$= 1/2\ (3\ nV/\sqrt{Hz})/1\ V)^2\ [\ 1 + 10\ kHz/f_m\ ]. \qquad (5.25)$$

It will be seen in the next discussion that the output buffer phase noise is negligible compared to the oscillator stage noise.

Total Predicted Voltage Controlled Oscillator Phase Noise

The total VCO phase noise is calculated by adding the oscillator stage phase noise and the buffer amplifier phase noise, assuming no

correlation between them. Since phase noise is given in mean square or power units, Equations 5.23 and 5.25 may be added directly together to evaluate the uncorrelated summing of the oscillator and buffer stage noises. It must be remembered that the effects of varactor diode noise are not included in this analysis. Varactor diode noise voltage introduces phase noise as described in Equation 4.9. This effect has been omitted as the bulk resistance of the MV-109 varactor is quite low and the VCO gain is also low.

The total predicted oscillator phase noise is plotted in Figure 5.4 along with the oscillator stage noise component and the output buffer noise component. Note that the output buffer contributes very little to the total output phase noise. Phase noise is given in units of dBc, which is found by taking $10\log_{10}$ of Equations 5.23, 5.25, and their sum. Phase noise is only given for an operating frequency of 45 MHz for clarity. Phase noise at 75 MHz is approximately 6 dB higher because the oscillator stage input voltage drops to about one-half of its 45 MHz value. This approximation is not exact because the effects of the higher carrier frequency are not included. The loaded Q of the synthesizer is very nearly constant at 100 for all operating frequencies, so this term in Leeson's noise model does not change.

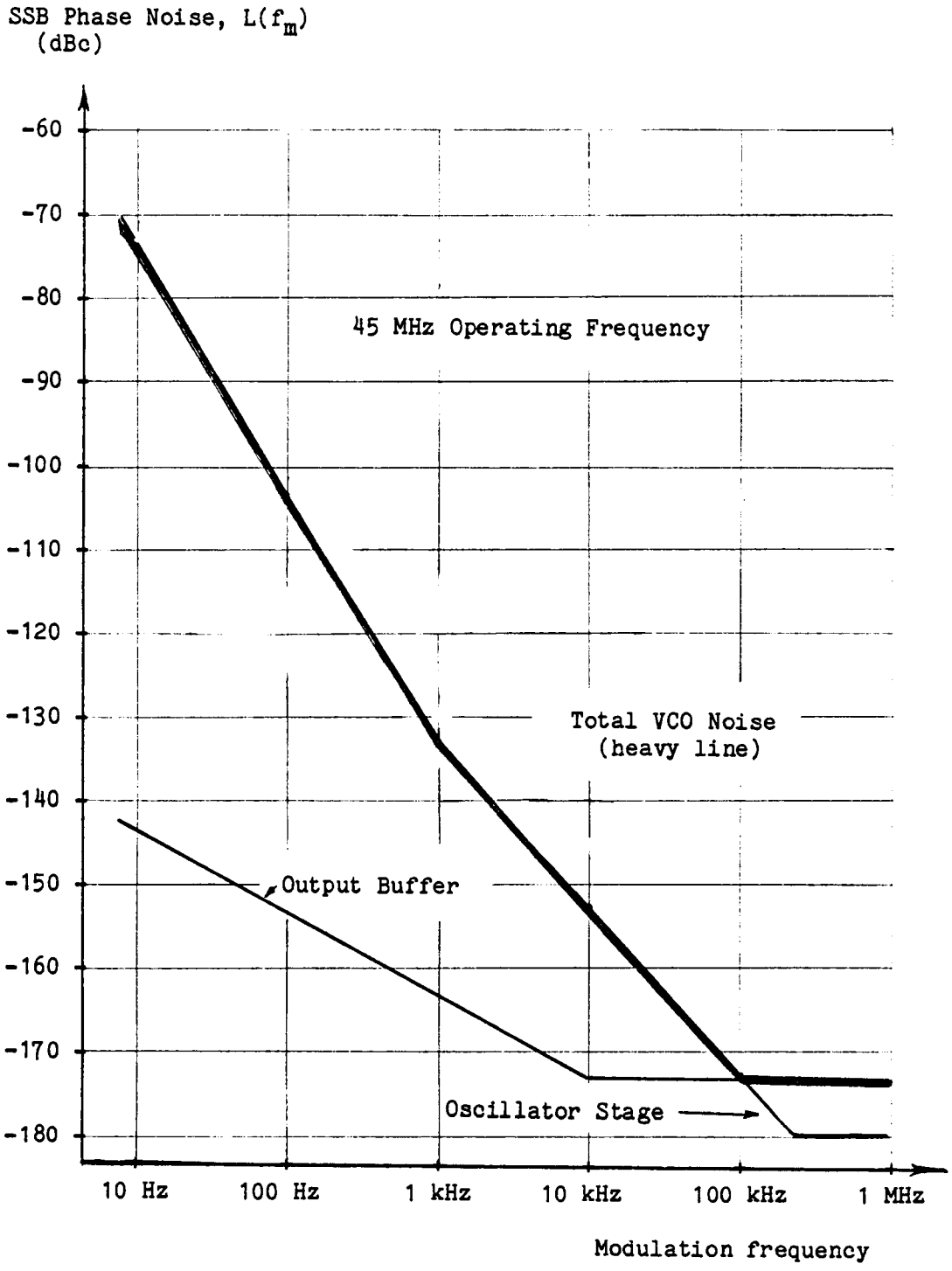


Figure 5.4. Predicted Voltage Controlled Oscillator Phase Noise.

6. THE COMPLETE 45-75 MHz SYNTHESIZER

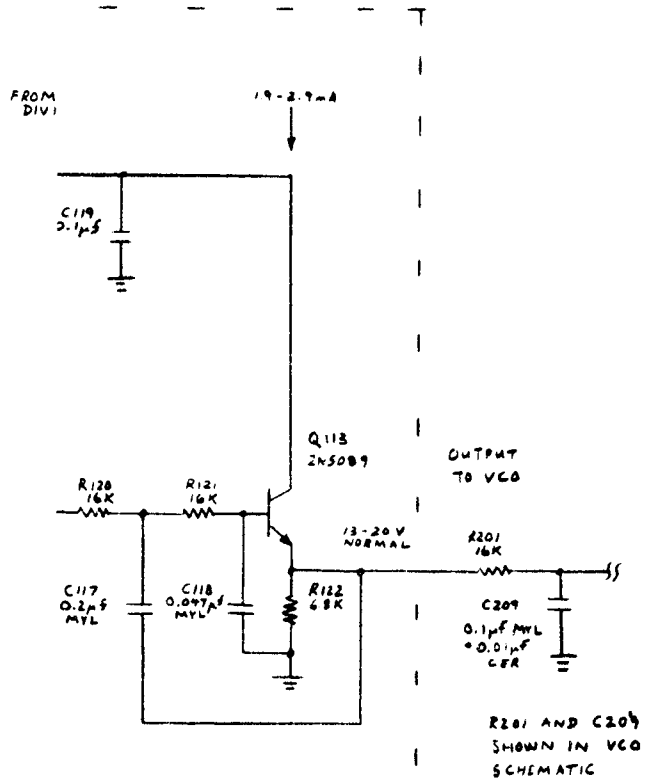
Phase Detector And Loop Amplifier/Filter

Circuit Description

A schematic diagram of the phase detector and loop amplifier/filter for the synthesizer is shown in Figure 6.1. The circuit consists of an integrated circuit-type phase detector, a discrete loop amplifier and lag-lead filter, and a three pole lowpass filter for rejection of reference frequency phase detector ripple and circuit noise.

The reference frequency and feedback frequency inputs are translated to ±7.5 V logic levels to drive the CD4046 type phase detector (U101), which is operated from ±7.5 V bias levels. The logic translation circuits, Q101-Q106, are designed to produce pulses with a fast positive-going risetime because the phase detector compares phase at the positive-going transition of its inputs. The phase detector is operated at ±7.5 V bias levels because its output voltage operates at a voltage equal to the input voltage of the lag-lead filter stage, which is close to ground. Since the phase detector outputs positive (+7.5 V) and negative (-7.5 V) pulses to correct for either leading or lagging phase errors, the phase detector has equal gain for both leading and lagging phase errors.

The phase detector (U101) is a CD4046 type integrated circuit detector which was described earlier in Section 3 in the "Phase Detectors" discussion. The output of this phase detector goes to a high impedance or off-state when no phase correction is required. This greatly reduces the phase detector reference frequency ripple. Phase


FROM DIV 1
1.9 - 2.9 mA
C119 0.1μF
Q113 2N5089
OUTPUT TO VCO
R120 16K
R121 16K
13 - 20 V NORMAL
R201 16K
C117 0.2μF MYL
C118 0.0997μF MYL
R122 4.8K
C209 0.1μF MYL + 0.01μF CER
R201 AND C209 SHOWN IN VCO SCHEMATIC

detector ripple causes reference frequency sidebands in the VCO output spectrum. Phase-lock detection is provided by JFET Q107. The drain of Q107 is saturated to ground during phase-locked conditions, and is cutoff when phase-locking is lost. This stage is used to control an LED, which glows under normal or phase-locked conditions.

The active lag-lead filter consists of transistors, Q108-Q112. The active lag-lead filter is designed for a positive output of 8-21 V to operate the tuning varactor in the VCO. The input stage features a low input bias current because the input device (Q108) is a JFET. It is important that leakage current be minimized at the phase detector output because leakage current must be compensated for by output pulses, which will raise the VCO reference frequency sidebands.

The active lag-lead filter stage has a very high open loop gain because of the high dominant pole impedance at the collector of Q109. Feedback elements R114, R119, and C112 provide the lag-lead response. Capacitor C113 introduces an additional real pole for lowpass filtering of phase detector ripple.

The three pole lowpass filter consists of transistor Q113 in a two pole active lowpass filter configuration followed by a single pole passive lowpass filter. Resistor R201 and capacitor C209 form the passive single pole lowpass filter that immediately precedes the VCO. This passive filter minimizes noise at the varactor because it provides a continuous roll-off of circuit noise. Active filters usually have fixed noise floors set by active device noise.

Circuit Analysis

The phase detector gain is 7.5 V/cycle since a phase error results in a 7.5 V pulse (either positive or negative, depending upon whether the phase is leading or lagging) equal in duration to the time of the phase overlap. Under phase-locked conditions, the positive edges of the phase detector input signals are in phase. The phase detector gain will be used later in PLL compensation calculations.

The transfer function of the lag-lead filter is

$$K_{lag\text{-}lead} = [\ (1 + st_2)/st_1\ ]\ \ [\ 1/(1 + st_{L1})\ ], \qquad (6.1)$$

assuming an infinite open loop gain. The time constant t_1 is given by

$$t_1 = (R114)\ (C112); \qquad (6.2)$$

the time constant t_2 is given by

$$t_2 = R119\ [\ C112 + C113\ ]; \qquad (6.3)$$

and the lowpass time constant t_{L1} is given by

$$t_{L1} = (R119)\ (C113). \qquad (6.4)$$

The time constants t_1 and t_2 describe the active lag-lead filter that was described earlier in Figure 3.4. The time constant t_{L1} describes the added single pole lowpass response that helps to filter out reference frequency sidebands.

The three pole lowpass filter is composed of a second-order lowpass filter followed by a single pole lowpass filter. The transfer

function of the three pole lowpass filter is

$$K_{3\ pole\ lpass} = [\ w_L^2/(\ s^2 + 2\zeta w_L s + w_L^2\ ]\ [\ 1/(\ 1 + st_{L2})\ ], \quad (6.5)$$

where w_L is the 3 dB frequency (in radians/second) of the second-order lowpass filter, ζ is the damping of the second-order lowpass filter, and t_{L2} is the time constant of the single pole lowpass filter. A three pole Butterworth response is obtained by setting the damping of the second-order lowpass at 0.5, and by setting the 3 dB frequencies of both the second-order lowpass and the single pole lowpass equal to the desired 3 dB frequency of the three pole filter (57 p. 12:1).

The 3 dB frequency of the second-order lowpass filter is

$$f_{3\ dB} = 1/(2\pi RC), \text{ where} \quad (6.6)$$

$$R = R120 = R121, \text{ and} \quad (6.7)$$

$$C = C117/\zeta = \zeta C118, \quad (6.8)$$

where ζ is the damping factor of the second-order lowpass filter (58 p. 123). The3 dB frequency of the single pole lowpass filter is

$$f_{3\ dB} = 1/(2\pi R201 \cdot C209) = 1/(2\pi t_{L2}). \quad (6.9)$$

Loop Compensation Design

The values of t_1, t_2, t_{L1}, and the 3 dB frequency of the three pole lowpass filter must be properly selected to ensure stability of the synthesizer. To select these values, it is necessary to

calculate the dc loop gain, G. The dc loop gain is given by

$$G = K_{\phi}K_V/N, \tag{6.10}$$

which is the product of the phase detector gain and the VCO gain divided by the loop divider ratio. Evaluating the dc loop gain at the geometric mean of 45 MHz and 75 MHz, which is 58 MHz, for an average VCO gain of 150 kHz/volt gives

$$\begin{aligned} G &= K_{\phi}K_V/N \\ &= (7.5 \text{ V/cycle }) (150 \text{ kHz/volt }) / (58000) \\ &= 19.4 \text{ sec}^{-1}. \end{aligned} \tag{6.11}$$

The time constants t_1 and t_2 are found for the second-order PLL with an active lag-lead filter by rearranging Equations 3.15 and 3.16 of Section 3, which describe PLL natural frequency and damping. The time constant t_1 is given by

$$t_1 = G/w_n^2, \tag{6.12}$$

and the time constant t_2 is given by

$$t_2 = 2\zeta/w_n. \tag{6.13}$$

The PLL natural frequency is w_n, and the PLL damping is ζ.

A PLL natural frequency of 10 Hz (62.8 radians/sec) and a PLL damping factor of 0.707 were chosen for the synthesizer. A low value of natural frequency was chosen because of the low dc loop gain and because of the need to provide a very high attenuation of the 1 kHz

reference frequency phase detector ripple, which will cause reference frequency sidebands in the VCO output spectrum.

The values selected for t_1 and t_2 in the synthesizer are

$$t_1 = G/w_n^2$$

$$= 19.4/(62.8)^2 \quad = 4.9 \text{ ms, and} \tag{6.14}$$

$$t_2 = 2\zeta/w_n$$

$$= 2(0.707)/(62.8) \quad = 22.5 \text{ ms.} \tag{6.15}$$

The 3 dB frequency of the single pole lowpass filter in the lag-lead stage was set at 200 Hz and the 3 dB frequency of the three pole lowpass filter was set at 100 Hz. The 3 dB frequencies of these filters were set at a minimum of 10 times greater than the loop natural frequency. The selection of the lowpass corner frequencies involves a compromise between loop stability and reference frequency sideband suppression. For the synthesizer to closely approximate a second-order PLL, the 3 dB frequencies of the lowpass filters need to be set much higher than the loop natural frequency. For maximum lowpass filtering of the reference frequency, the 3 dB frequencies should be set at as low a frequency as possible. Since the synthesizer is a sixth-order system, a computer program will be presented later to evaluate the frequency and phase response.

Noise Analysis

Phase detector noise will be considered later in the "Synthesizer Phase Noise Analysis" discussion of this section and is not a

significant contributor to synthesizer phase noise above 1 kHz. Since noise appearing across the varactor modulates the VCO causing phase noise, noise analysis of the loop amplifier/filter must be considered in calculating the total synthesizer phase noise. This noise could be a potentially significant contributor to synthesizer noise since it is not reduced by the loop at frequencies above the loop bandwidth.

Noise analysis of the loop amplifier/filter is extremely complex since the loop amplifier/filter contains five poles and one zero (the lead network zero). For this reason, SPICE computer analysis was used to evaluate the noise voltage appearing across C209 which also appears across the varactor diode.

Noise is evaluated assuming an infinite phase detector output impedance which models the phase detector under phase-locked conditions. To establish dc biasing, a current source is connected across R123, and a 1000 M ohm resistor is paralleled across C112. The current source is modelled as a noiseless source, and the 1000 M ohm resistor does not affect the circuit noise for frequencies above 1 Hz as it is shunted by C112. These additions to the loop amplifier/filter circuit model set the output voltage at approximately 18 V, which is within the normal circuit operating range.

The SPICE program is written to analyze the circuit from R123 to the voltage appearing across C209. All components are labelled in the SPICE program source listing as they are in the schematic. All transistors have an assumed 1/f noise corner of 1 kHz. The SPICE source listing is contained in Appendix B, and a tabular listing of the loop amplifier/filter output noise in $V/\sqrt{Hz}$ is provided in Figure 6.2.

FREQ (Hz)	ONOISE ($V/\sqrt{Hz}$)
1.000D+01	3.815D-07
1.259D+01	3.425D-07
1.585D+01	3.082D-07
1.995D+01	2.784D-07
2.512D+01	2.526D-07
3.162D+01	2.306D-07
3.981D+01	2.123D-07
5.012D+01	1.971D-07
6.310D+01	1.834D-07
7.943D+01	1.658D-07
1.000D+02	1.335D-07
1.259D+02	8.846D-08
1.585D+02	5.119D-08
1.995D+02	2.873D-08
2.512D+02	1.649D-08
3.162D+02	9.876D-09
3.981D+02	6.237D-09
5.012D+02	4.167D-09
6.310D+02	2.933D-09
7.943D+02	2.153D-09
1.000D+03	1.628D-09
1.259D+03	1.255D-09
1.585D+03	9.790D-10
1.995D+03	7.694D-10
2.512D+03	6.073D-10
3.162D+03	4.805D-10
3.981D+03	3.808D-10
5.012D+03	3.020D-10
6.310D+03	2.397D-10
7.943D+03	1.903D-10
1.000D+04	1.511D-10
1.259D+04	1.200D-10
1.585D+04	9.530D-11
1.995D+04	7.570D-11
2.512D+04	6.012D-11
3.162D+04	4.776D-11
3.981D+04	3.793D-11
5.012D+04	3.013D-11
6.310D+04	2.393D-11
7.943D+04	1.901D-11
1.000D+05	1.510D-11

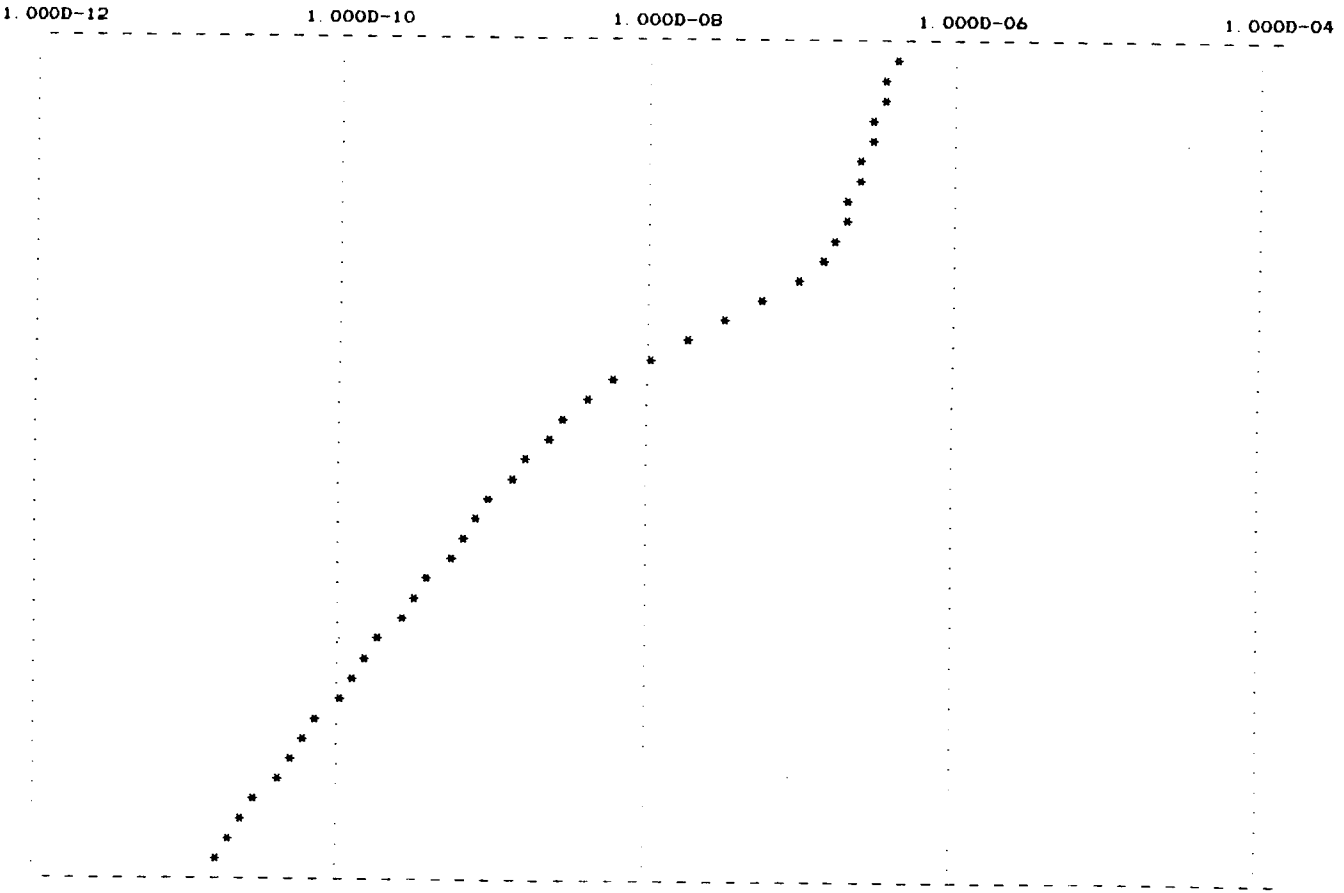


Figure 6.2. Loop Amplifier/Filter Output Noise for the Synthesizer from SPICE analysis.

Programmable Divider And Voltage Controlled Oscillator Presteering ROM

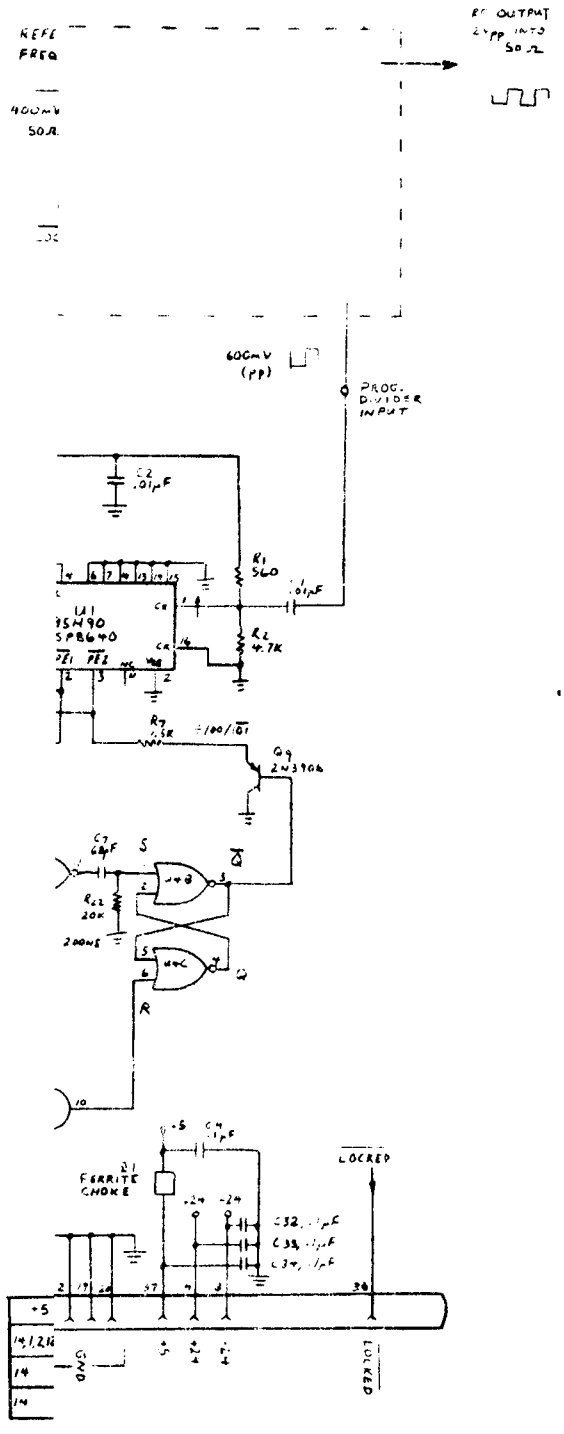
Circuit Description

The programmable divider and the VCO presteering ROM are located on a separate printed circuit board from the VCO, phase detector, and loop amplifier/filter. This is to accommodate shielding of the critical analog circuitry of the VCO, phase detector, and loop amplifier/filter from the programmable divider and the outside world. A schematic of the programmable divider and VCO presteering ROM is shown in Figure 6.3.

The programmable divider uses a two modulus variable modulus prescaler with division ratios of 100 and 101. A modulus control programmable divider controls the 1 kHz and 10 kHz frequency settings of the synthesizer. Another or main programmable divider controls the 100 kHz, 1 MHz, and 10 MHz frequency settings of the synthesizer.

The variable modulus prescaler divides the input signal by 101 for the number of counts set in the modulus control divider or counter. When the count in the modulus control counter reaches zero, the set-reset flip-flop made up of U4(B) and U4(C) changes the state of the prescaler modulus control line, causing the prescaler to now divide by 100. The operation of variable modulus prescalers in programmable dividers is discussed in more detail in Section 3 in the "Loop Frequency Dividers" discussion.

The variable modulus prescaler is made up of integrated circuits U1 and U2 along with transistors Q1 and Q2, and the NAND gate U3(A). Integrated circuit U1 is an ECL device and integrated circuits U2 and


REFERENCE FREQ
400mV
50Ω
RF OUTPUT
2 V p-p INTO 50Ω
600mV (p-p)
PROG. DIVIDER INPUT
C2 .01μF
R1 560
.01μF
U1
MC4390
SP8640
R2 4.7K
R7 1.5K ÷100/÷101
Q9 2N3906
C7 68pF
S
Q
R
R22 20K
200nS
10
+5
C4 .1μF
FERRITE CHOKE
LOCKED
+24
-24
C32, .1μF
C33, .1μF
C34, .1μF
÷5
÷4
÷4
LOCKED

U3 are LSTTL devices. All other integrated circuits in the programmable divider are CD4000 series CMOS devices since they are operated at a factor of 100 or 101 lower in frequency than the 45-75 MHz operating frequency because of the prescaler.

Integrated circuits U5 and U6 are programmable dividers operated in the BCD countdown mode. They are cascaded together and act as the modulus control programmable divider or counter. Integrated circuits U7-U10 are also programmable dividers operated in the BCD countdown mode. These dividers are cascaded together to form the main programmable divider.

A look-ahead scheme is used to determine the terminal count of the main programmable divider and to reload both the modulus control divider and the main divider. This scheme is used because there is not enough time to decode the terminal count (zero) and then reload the programmable divider before the next clock cycle. One clock cycle after the main divider reaches a count of zero, a zero logic level is clocked into the D flip-flop U12(A), which loads both programmable dividers with the parallel BCD frequency or division ratio data. Also the set-reset modulus control flip-flop is set for division by 101. The load pulse lasts until immediately after the next clock cycle, where a logic level of one gets clocked into the D flip-flop because the main divider no longer has a count of zero in it, having been preset with nonzero data. Both the modulus control and main divider will begin counting down on the next clock cycle because the load line is no longer asserted.

The look-ahead scheme causes two clock cycles to be lost in the programmable dividers; this is the price paid for having enough time to operate the slow CD4000 series CMOS programmable devices. It is thus necessary to subtract 200 (decimal) from the inputted division ratio. This is because the prescaler always divides by 100 at the end of a division cycle since it can only divide by 101 for up to 99 counts (the maximum count in the modulus control divider), which would be completed earlier in the division cycle. The extra two counts lost by the main divider are then equal to 200 lost counts in the overall programmable divider. The subtraction of 200 is not a problem since the synthesizer frequency setting will have to be altered by the addition of the IF frequency and by small offsets for proper single-sideband reception in the communications receiver.

The input frequency set lines for the programmable divider are BCD coded 5 V CMOS logic levels. These lines are all bypassed to ground by 0.001 uF capacitors to prevent conducted RF from leaving the programmable divider. The three most significant decade (10 MHz, 1 MHz and 100 kHz) inputs are sampled by U(11), the VCO presteering ROM. This ROM is an EPROM integrated circuit and generates a truth table based on the frequency setting of the synthesizer to select the proper inductors in the VCO. Since the EPROM cannot switch the 100 mA of current needed to operate the PIN diodes in the VCO, transistors Q3-Q8 are required to provide the needed current.

ROM Truth Table

The ROM truth table was generated from the tank circuit analysis results of Figure 5.3. The truth table controls the selection of the

VCO inductors to ensure that the VCO will be properly tuned so that fine tuning by the varactor tuning diode will result in phase-locking of the synthesizer. Table 6.1 contains a listing of the ROM truth table.

Reference Frequency Oscillator

The reference frequency oscillator for the synthesizer consists of a 5 MHz series resonant crystal oscillator followed by a digital frequency divider with a division ratio of 5000. The output of the reference frequency oscillator is a 1 kHz logic signal that can drive a 50 ohm load. A schematic of the reference oscillator is shown in Figure 6.4.

Transistor Q1 is a Class A crystal oscillator sustaining amplifier with emitter coupling to the crystal. This stage maximizes the loaded Q of the crystal because its low emitter impedance drives the crystal. Transistors Q2 and Q3 form a differential limiter. The signal at the collector of Q2 is coupled to the input of the sustaining amplifier (Q1) to provide positive feedback in the oscillator. The collector of Q3 is the buffered oscillator output, which is TTL compatible and feeds the frequency dividers.

The crystal oscillator is similar to Rohde's 100 MHz crystal oscillator which was discussed in Section 4 in the "Low Noise Oscillator Examples" discussion. The reference oscillator, however, uses only one differential limiter and does not use the cascode configuration in the sustaining amplifier.

Table 6.1. ROM Truth Table for the Synthesizer.

INPUT		OUTPUT						
Frequency (MHz)	Address (hex)	Q5 (L202	Q4	Q3	Q2	Q1	Q0 L207)	Data (hex)
45.0-45.7	448-455	1	1	1	1	1	1	3F
45.8-46.4	456-462	1	1	1	1	1	0	3E
46.5-47.2	463-470	1	1	1	1	0	1	3D
47.3-47.8	471-476	1	1	1	1	0	0	3C
47.9-48.5	477-483	1	1	1	0	1	1	3B
48.6-49.2	484-490	1	1	1	0	1	0	3A
49.3-49.9	491-497	1	1	1	0	0	1	39
50.0-50.5	498-503	1	1	1	0	0	0	38
50.6-51.1	504-509	1	1	0	1	1	1	37
51.2-51.8	510-516	1	1	0	1	1	0	36
51.9-52.4	517-522	1	1	0	1	0	1	35
52.5-53.0	523-528	1	1	0	1	0	0	34
53.1-53.7	529-535	1	1	0	0	1	1	33
53.8-54.3	536-541	1	1	0	0	1	0	32
54.4-54.9	542-547	1	1	0	0	0	1	31
55.0-55.3	548-551	1	1	0	0	0	0	30
55.4-55.9	552-557	1	0	1	1	1	1	2F
56.0-56.5	558-563	1	0	1	1	1	0	2E
56.6-57.1	564-569	1	0	1	1	0	1	2D
57.2-57.7	570-575	1	0	1	1	0	0	2C
57.8-58.3	576-581	1	0	1	0	1	1	2B
58.4-58.8	582-586	1	0	1	0	1	0	2A
58.9-59.4	587-592	1	0	1	0	0	1	29
59.5-59.9	593-597	1	0	1	0	0	0	28
60.0-60.5	598-603	1	0	0	1	1	1	27
60.6-61.0	604-608	1	0	0	1	1	0	26
61.1-61.6	609-614	1	0	0	1	0	1	25
61.7-62.1	615-619	1	0	0	1	0	0	24
62.2-62.6	620-624	1	0	0	0	1	1	23
62.7-63.1	625-629	1	0	0	0	1	0	22
63.2-63.7	630-635	1	0	0	0	0	1	21
63.8-64.3	636-641	1	0	0	0	0	0	20

Table 6.1. (Continued)

INPUT		OUTPUT						
Frequency (MHz)	Address (hex)	Q5 (L202	Q4	Q3	Q2	Q1	Q0 L207)	Data (hex)
64.4-64.8	642-646	0	1	1	1	1	1	1F
64.9-65.3	647-651	0	1	1	1	1	0	1E
65.4-65.9	652-657	0	1	1	1	0	1	1D
66.0-66.3	658-661	0	1	1	1	0	0	1C
66.4-66.9	662-667	0	1	1	0	1	1	1B
67.0-67.4	668-672	0	1	1	0	1	0	1A
67.5-67.9	673-677	0	1	1	0	0	1	19
68.0-68.4	678-682	0	1	1	0	0	0	18
68.5-68.9	683-687	0	1	0	1	1	1	17
69.0-69.3	688-691	0	1	0	1	1	0	16
69.4-69.9	692-697	0	1	0	1	0	1	15
70.0-70.3	698-701	0	1	0	1	0	0	14
70.4-70.8	702-706	0	1	0	0	1	1	13
70.9-71.3	707-711	0	1	0	0	1	0	12
71.4-71.7	712-715	0	1	0	0	0	1	11
71.8-72.0	716-718	0	1	0	0	0	0	10
72.1-72.5	719-723	0	0	1	1	1	1	0F
72.6-72.9	724-727	0	0	1	1	1	0	0E
73.0-73.5	728-733	0	0	1	1	0	1	0D
73.6-73.9	734-737	0	0	1	1	0	0	0C
74.0-74.4	738-742	0	0	1	0	1	1	0B
74.5-74.8	743-746	0	0	1	0	1	0	0A
74.9-75.0	747-748	0	0	1	0	0	1	09

Note: An output of "0" denotes the inductor is switched into the circuit. All undefined memory locations are stored with hex FF, which corresponds to the 45 MHz frequency setting.

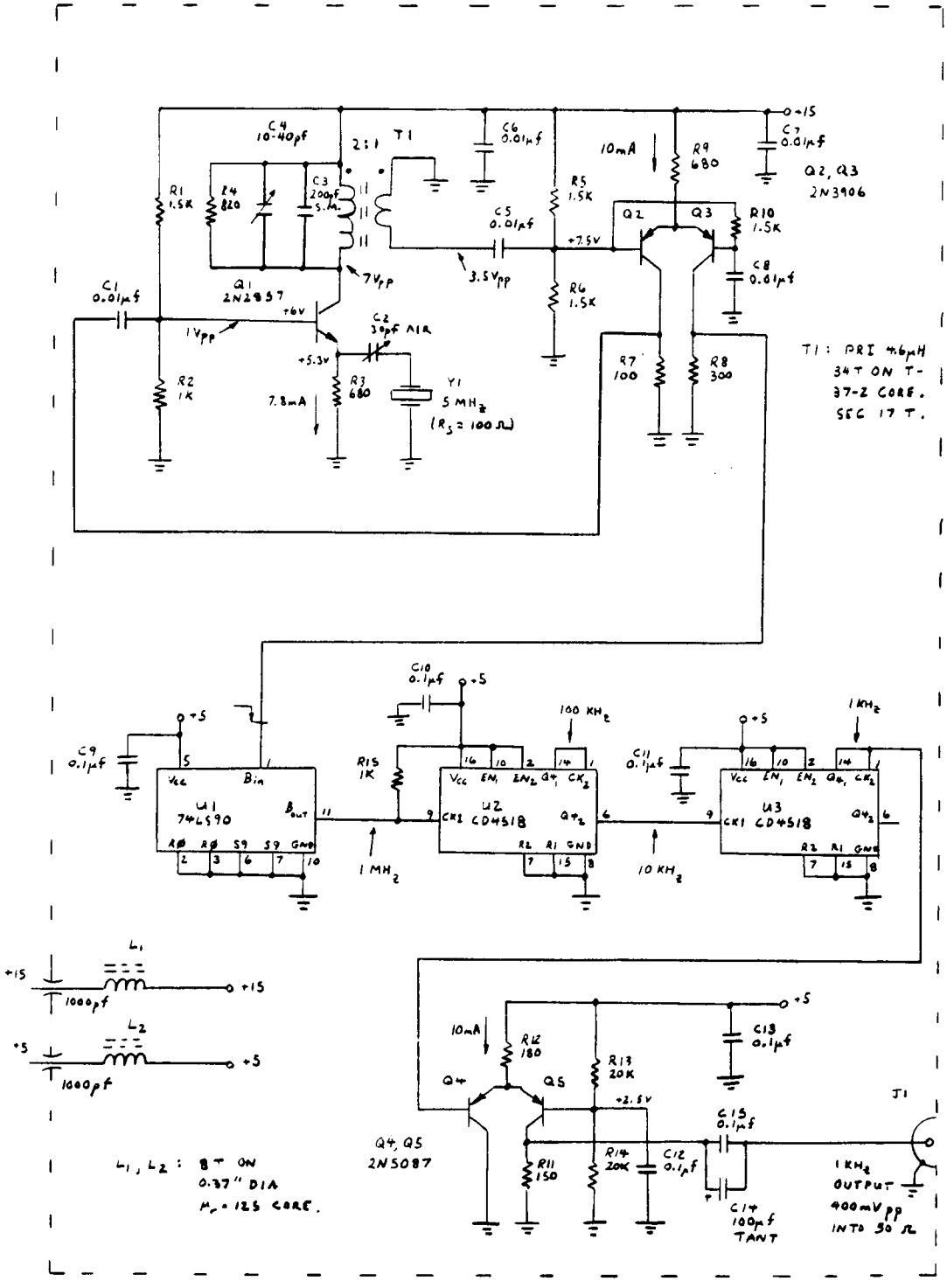


Figure 6.4. Schematic Diagram of the Reference Frequency Oscillator Used in the Synthesizer.

Integrated circuits U1-U3 are fixed frequency dividers that divide the 5 MHz oscillator signal down to 1 kHz. Integrated circuit U1 is an LSTTL device, and U2 and U3 are CMOS devices. Transistors Q4 and Q5 form a differential limiter that is used for output buffering of the reference frequency oscillator output.

A detailed analysis of the reference oscillator is not provided because it is a negligible contributor to synthesizer phase noise at frequencies above 1 kHz. Signal levels, bias levels, and other notes are included on the schematic of Figure 6.4 and provide a brief analysis of the circuitry. An estimation of phase noise for the reference oscillator is plotted in Figure 6.5.

Phase noise was estimated using Leeson's model for the 5 MHz crystal oscillator with a sustaining amplifier input noise of 1.5 nV/$\sqrt{\text{Hz}}$, a low frequency phase noise corner frequency of 10 kHz, a sustaining amplifier input signal level of 0.35 Vrms, and a loaded crystal Q of 50,000. Buffer amplifier phase noise was assumed to be negligible. The phase noise of the 5 MHz crystal oscillator was then reduced by the division ratio of 5,000 or 74 dB to normalize it to 1 kHz. Finally, an estimated divider phase noise of -160 dBc, increasing at 10 dB/decade at frequencies below 1 kHz, was added. This value was taken to be between the phase noise floor of TTL and ECL dividers, which is given by Scherer.[6] Data on CMOS dividers was not found in the literature.

It is interesting to note that divider noise almost totally dominates the reference oscillator noise. The estimated reference phase noise will be used later in calculating total synthesizer phase noise

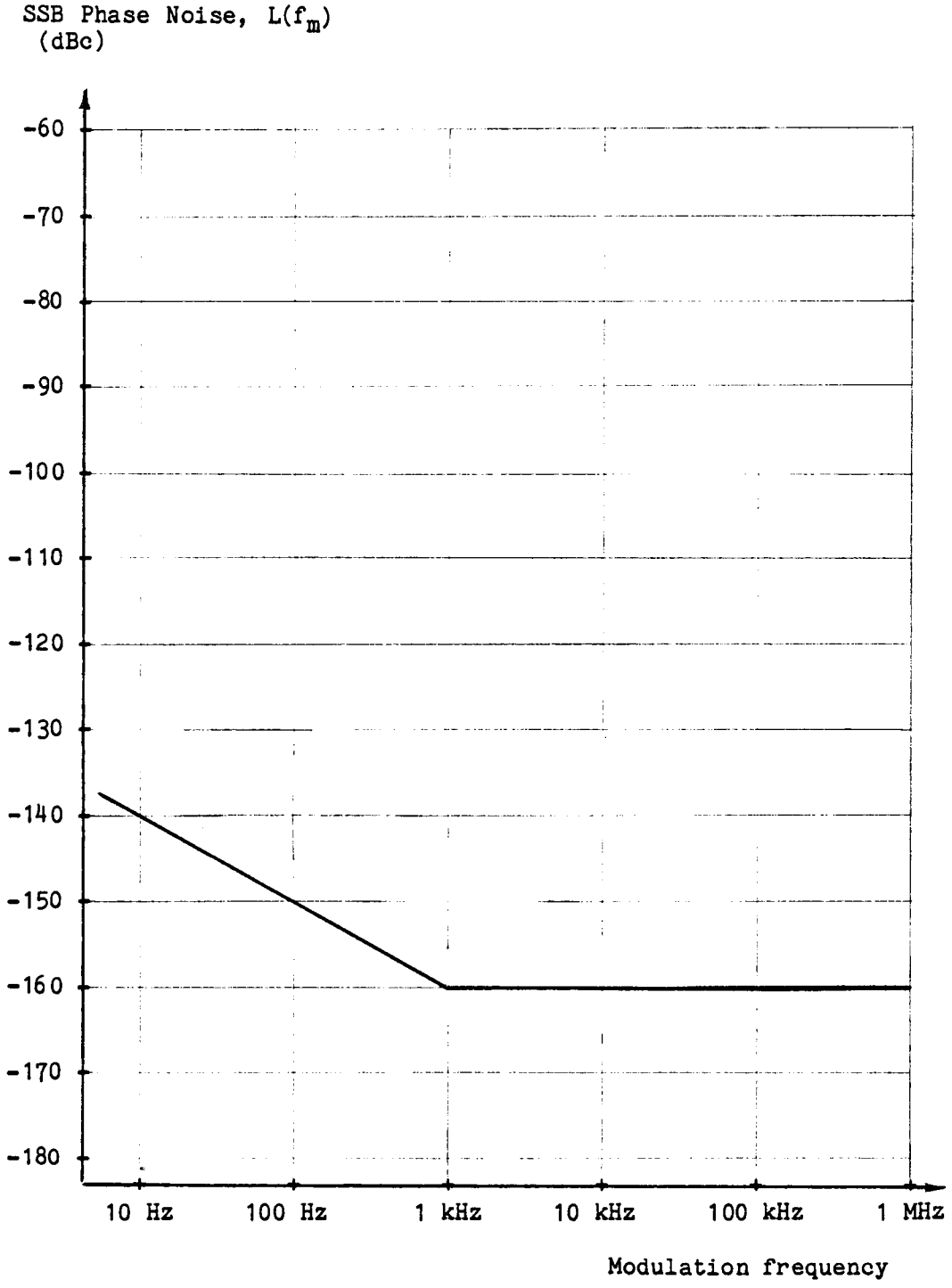


Figure 6.5. Estimated Phase Noise of the 1 kHz Reference Oscillator Used in the Synthesizer.

to verify that reference oscillator phase noise is indeed negligible at frequencies above 1 kHz.

Synthesizer Frequency And Phase Response

The loop gain of the synthesizer, from Equation 3.2 in Section 3, is given by

$$T = K_{\phi}K_{V}K_{f}(s)/(sN)$$

$$= \left[\frac{K_{\phi}K_{V}}{sN}\right] \left[\frac{1 + st_2}{st_1}\right] \left[\frac{1}{1 + st_{L1}}\right] \left[s^2 \frac{w_L^2}{+2\zeta w_L s + w_L^2}\right] \left[\frac{1}{1 + st_{L2}}\right], \quad (6.16)$$

(lag-lead with lowpass) (three pole lowpass)

where all terms of the equation have been previously described. Since the synthesizer is a sixth-order system, computer analysis of frequency and phase response is a practical necessity.

A FORTRAN computer program was written that tabulates loop gain and phase as functions of frequency. The program also tabulates the loop amplifier/filter gain as this is important to determine the rejection of phase detector reference frequency ripple. Finally, the program tabulates the synthesizer closed loop gain factor (-T/(1-T)) and the PLL error response (1/(1-T)).

The program computes the different transfer functions at various frequencies, using complex arithmetic which FORTRAN very conveniently supports. The program was run for the synthesizer parameters and a listing of the results is contained in Figure 6.6. A source listing of the program is contained in Appendix C.

KO (VOLTS/CYCLE)	KV (HZ/VOLT)	NDIV
7.50E 0	1.50E 5	5.80E 4

T1 (SEC)	T2 (SEC)	FC0 (HZ)
4.90E -3	2.25E -2	2.00E 2

FC2ND (HZ)	ZETA	FC1 (HZ)
1.00E 2	5.00E -1	1.00E 2

DC LOOP GAIN (1/SEC)
1.94E 1

FREQUENCY	AMP/FILTER KF		LOOP GAIN T		PLL GAIN T/(1+T)	PLL ERROR 1/(1+T)
(HZ)	MAG (dB)	PHASE (DEG)	MAG (dB)	PHASE (DEG)	MAG (dB)	MAG (dB)
1.00	30.32	-83.39	40.11	-173.39	.09	-40.02
1.12	29.36	-82.61	38.16	-172.61	.11	-38.05
1.26	28.36	-81.70	36.14	-171.70	.14	-36.01
1.41	27.42	-80.75	34.22	-170.75	.17	-34.06
1.59	26.42	-79.61	32.18	-169.61	.21	-31.97
1.78	25.49	-78.43	30.27	-168.43	.26	-30.01
2.00	24.55	-77.08	28.32	-167.08	.33	-27.98
2.24	23.64	-75.64	26.43	-165.64	.41	-26.02
2.51	22.75	-74.06	24.55	-164.06	.51	-24.04
2.82	21.87	-72.30	22.65	-162.30	.63	-22.02
3.16	21.03	-70.45	20.83	-160.45	.77	-20.05
3.55	20.20	-68.44	18.99	-158.44	.95	-18.04
3.98	19.43	-66.34	17.22	-156.34	1.15	-16.07
4.47	18.68	-64.11	15.47	-154.11	1.40	-14.07
5.01	18.00	-61.87	13.79	-151.87	1.67	-12.13
5.62	17.36	-59.59	12.16	-149.59	1.97	-10.19
6.31	16.77	-57.31	10.56	-147.31	2.30	-8.26
7.08	16.24	-55.12	9.03	-145.12	2.64	-6.39
7.94	15.77	-53.08	7.56	-143.08	2.96	-4.61
8.91	15.35	-51.22	6.15	-141.22	3.24	-2.91
10.00	14.99	-49.61	4.78	-139.61	3.43	-1.35
11.20	14.68	-48.34	3.49	-138.34	3.49	-.00
12.60	14.41	-47.39	2.20	-137.39	3.37	1.18
14.10	14.19	-46.89	1.00	-136.89	3.07	2.07
15.90	14.00	-46.83	-.24	-136.83	2.54	2.78
17.80	13.84	-47.27	-1.38	-137.27	1.86	3.24
20.00	13.71	-48.27	-2.52	-138.27	1.01	3.53
22.40	13.60	-49.81	-3.62	-139.81	.08	3.69
25.10	13.50	-51.98	-4.70	-141.98	-.95	3.75
28.20	13.42	-54.89	-5.80	-144.89	-2.07	3.73
31.60	13.34	-58.48	-6.86	-148.48	-3.22	3.64
35.50	13.27	-62.99	-7.95	-152.99	-4.45	3.50
39.80	13.19	-68.35	-9.02	-158.35	-5.71	3.31
44.70	13.10	-74.86	-10.11	-164.86	-7.06	3.06
50.10	12.99	-82.49	-11.21	-172.49	-8.46	2.75
56.20	12.84	-91.61	-12.36	178.39	-9.97	2.39
63.10	12.62	-102.51	-13.59	167.49	-11.62	1.97
70.80	12.25	-115.34	-14.95	154.66	-13.46	1.49
79.40	11.67	-130.23	-16.54	139.77	-15.54	1.00
89.10	10.72	-147.23	-18.49	122.77	-17.96	.53
100.00	9.28	-165.61	-20.93	104.39	-20.77	.16
112.00	7.34	176.10	-23.85	86.10	-23.91	-.06
126.00	4.81	158.01	-27.41	68.01	-27.55	-.14
141.00	2.02	142.27	-31.17	52.27	-31.32	-.15
159.00	-1.22	127.27	-35.46	37.27	-35.58	-.12
178.00	-4.45	114.76	-39.66	24.76	-39.75	-.08

Figure 6.6. Frequency and Phase Response of the Synthesizer.

FREQUENCY	AMP/FILTER KF		LOOP GAIN T		PLL GAIN T/(1+T)	PLL ERROR 1/(1+T)
	MAG	PHASE	MAG	PHASE	MAG	MAG
(HZ)	(dB)	(DEG)	(dB)	(DEG)	(dB)	(dB)
200.00	-7.89	103.23	-44.12	13.23	-44.18	-.05
224.00	-11.34	93.15	-48.55	3.15	-48.58	-.03
251.00	-14.86	84.00	-53.06	-6.00	-53.08	-.02
282.00	-18.54	75.51	-57.75	-14.49	-57.76	-.01
316.00	-22.18	67.98	-62.38	-22.02	-62.39	-.01
355.00	-25.96	61.00	-67.17	-29.00	-67.17	-.00
398.00	-29.71	54.78	-71.91	-35.22	-71.92	-.00
447.00	-33.56	49.06	-76.77	-40.94	-76.77	-.00
501.00	-37.37	43.98	-81.57	-46.02	-81.57	-.00
562.00	-41.24	39.37	-86.44	-50.63	-86.44	-.00
631.00	-45.16	35.18	-91.37	-54.82	-91.37	-.00
708.00	-49.08	31.44	-96.29	-58.56	-96.29	-.00
794.00	-52.99	28.10	-101.20	-61.90	-101.20	-.00
891.00	-56.94	25.08	-106.15	-64.92	-106.15	-.00
1000.00	-60.91	22.38	-111.12	-67.62	-111.12	-.00
1120.00	-64.81	20.01	-116.01	-69.99	-116.01	-.00
1260.00	-68.88	17.80	-121.09	-72.20	-121.09	-.00
1410.00	-72.76	15.92	-125.96	-74.08	-125.96	-.00
1590.00	-76.92	14.13	-131.16	-75.87	-131.16	-.00
1780.00	-80.83	12.62	-136.05	-77.38	-136.05	.00
2000.00	-84.87	11.24	-141.09	-78.76	-141.09	.00
2240.00	-88.79	10.04	-146.01	-79.96	-146.01	.00
2510.00	-92.74	8.96	-150.94	-81.04	-150.94	.00
2820.00	-96.78	7.98	-156.00	-82.02	-156.00	.00
3160.00	-100.73	7.12	-160.93	-82.88	-160.93	.00
3550.00	-104.77	6.34	-165.99	-83.66	-165.99	.00
3980.00	-108.74	5.65	-170.95	-84.35	-170.95	.00
4470.00	-112.77	5.03	-175.99	-84.97	-175.99	.00
5010.00	-116.73	4.49	-180.94	-85.51	-180.94	.00
5620.00	-120.72	4.01	-185.93	-85.99	-185.93	.00
6310.00	-124.75	3.57	-190.96	-86.43	-190.96	.00
7080.00	-128.75	3.18	-195.96	-86.82	-195.96	.00
7940.00	-132.73	2.84	-200.93	-87.16	-200.93	.00
8910.00	-136.73	2.53	-205.94	-87.47	-205.94	.00
10000.00	-140.74	2.25	-210.95	-87.75	-210.95	.00
11200.00	-144.68	2.01	-215.87	-87.99	-215.87	.00
12600.00	-148.77	1.79	-220.99	-88.21	-220.99	.00
14100.00	-152.68	1.60	-225.87	-88.40	-225.87	.00
15900.00	-156.85	1.42	-231.09	-88.58	-231.09	.00
17800.00	-160.77	1.26	-235.99	-88.74	-235.99	.00
20000.00	-164.82	1.13	-241.05	-88.87	-241.05	.00
22400.00	-168.76	1.01	-245.97	-88.99	-245.97	.00
25100.00	-172.71	.90	-250.92	-89.10	-250.92	.00
28200.00	-176.76	.80	-255.97	-89.20	-255.97	.00
31600.00	-180.71	.71	-260.92	-89.29	-260.92	.00
35500.00	-184.76	.63	-265.97	-89.37	-265.97	.00
39800.00	-188.73	.57	-270.94	-89.43	-270.94	.00
44699.99	-192.76	.50	-275.98	-89.50	-275.98	.00
50100.01	-196.73	.45	-280.93	-89.55	-280.93	.00
56200.00	-200.72	.40	-285.92	-89.60	-285.92	.00
63100.00	-204.74	.36	-290.95	-89.64	-290.95	.00
70800.01	-208.74	.32	-295.95	-89.68	-295.95	.00
79400.01	-212.73	.28	-300.93	-89.72	-300.93	.00
89100.00	-216.73	.25	-305.94	-89.75	-305.94	.00

Figure 6.6. (Continued)

Note that the phase margin is approximately 43°, and the gain peaking is approximately 3.5 dB, indicating stable operation. Also note the large loop amplifier/filter attenuation at the reference frequency (1 kHz) and at its harmonic frequencies. This attenuation will greatly reduce reference frequency sidebands. Note that relative to synthesizer phase noise performance, the error response is unity for frequencies above 10 Hz, which indicates that VCO phase noise above this frequency will not be cleaned up by the synthesizer. Also note that the closed loop gain factor drops rapidly at frequencies above 20 Hz, which indicates that the reference oscillator, loop divider, and phase detector noise will be attenuated at frequencies above this.

Synthesizer Phase Noise Analysis

The calculation of PLL output phase noise was discussed earlier in Section 3 in the "Noise Analysis Of Phase-Locked Loops" discussion. A PLL noise model was presented in Figure 3.8, and an equation for total PLL output phase noise was presented in Equation 3.22. The following analysis will be based upon this earlier discussion. Note that synthesizer output phase noise is the uncorrelated sum of the reference frequency oscillator, phase detector, loop frequency divider, loop amplifier/filter, and VCO noise contributions.

Noise Components Affected by the Closed Loop Gain

The reference frequency, phase detector, and loop frequency divider noise contributions are all acted upon by the PLL closed loop

gain. From Equation 3.22, the synthesizer output phase noise due to these noise components is

$$\phi_n^2 \text{ out} = [\phi_n^2 \text{ ref} + \phi_n^2 \text{ div} + (V_n^2 \text{ det})(1/K_\phi^2)][N\ (-T/(1-T))]^2. \quad (6.17)$$

These noise components decrease very rapidly at frequencies above the loop bandwidth because the synthesizer is a sixth-order system.

The 1 kHz reference oscillator phase noise must be increased by N^2 as can be seen in Equation 6.17. For a synthesizer operating frequency of 45 MHz, this corresponds to an increase of $45{,}000^2$ or 93 dB. Additionally, the reference phase noise must be scaled by the closed loop gain factor (-T/(1-T)), which is tabulated in Figure 6.6. The reference oscillator phase noise contribution is evaluated by adding 93 dB to the reference oscillator phase noise in Figure 6.5, and then adding the "PLL GAIN", which is given in dB in Figure 6.6.

The phase detector and loop divider will be assumed to be noiseless since their noise contribution, like the reference oscillator noise contribution, is acted upon by the closed loop gain factor of the PLL, which is very low at frequencies above 1 kHz. The assumption of no phase detector and loop divider noise will be justified later by comparing total synthesizer phase noise to the reference frequency phase noise contribution.

Noise Components Affected by the Loop-Error Response

The VCO phase noise is acted upon by the loop-error response, which, unlike the closed loop response, does not decrease at frequencies above the loop bandwidth. In fact the error response approaches a value of unity for frequencies above the loop bandwidth.

It should be apparent that VCO phase noise contributions are very important at frequencies above 1 kHz.

Loop amplifier/filter noise modulates the VCO, causing additional phase noise in the output of the VCO. Loop amplifier/filter noise, as seen in the VCO output, is also acted upon by the loop-error response. Loop amplifier/filter noise could be a potentially significant contributor to synthesizer output phase noise.

The phase noise contributions of the VCO and loop amplifier/filter as given in Equation 3.22 are

$$\phi_n^2 \text{ out} = [\ \phi_n^2 \text{ osc} + (V_n^2 \text{ filter})(K_V/2\pi f_m)^2\ ][\ 1/(1-T)\ ]^2. \qquad (6.18)$$

The noise contribution of the VCO is plotted in Figure 6.7 and was evaluated by multiplying the predicted VCO phase noise of Figure 5.4 by the loop-error response taken from the tabulation in Figure 6.6. The noise contribution of the loop amplifier/filter is also plotted in Figure 6.7 and was evaluated using Equation 6.18. The loop amplifier/filter noise was taken from Figure 6.2, the VCO gain was taken to be 150 kHz/volt, and the loop-error response was taken from the tabulation in Figure 6.6.

Total Predicted Synthesizer Noise

The total predicted synthesizer noise is presented in Figure 6.7 along with the reference frequency oscillator contribution, VCO noise contribution, and the loop amplifier/filter contribution. Note that the reference frequency oscillator contribution is indeed negligible at frequencies above 1 kHz. The assumption of no phase detector and loop divider noise is valid because it can be seen from Figure 6.7

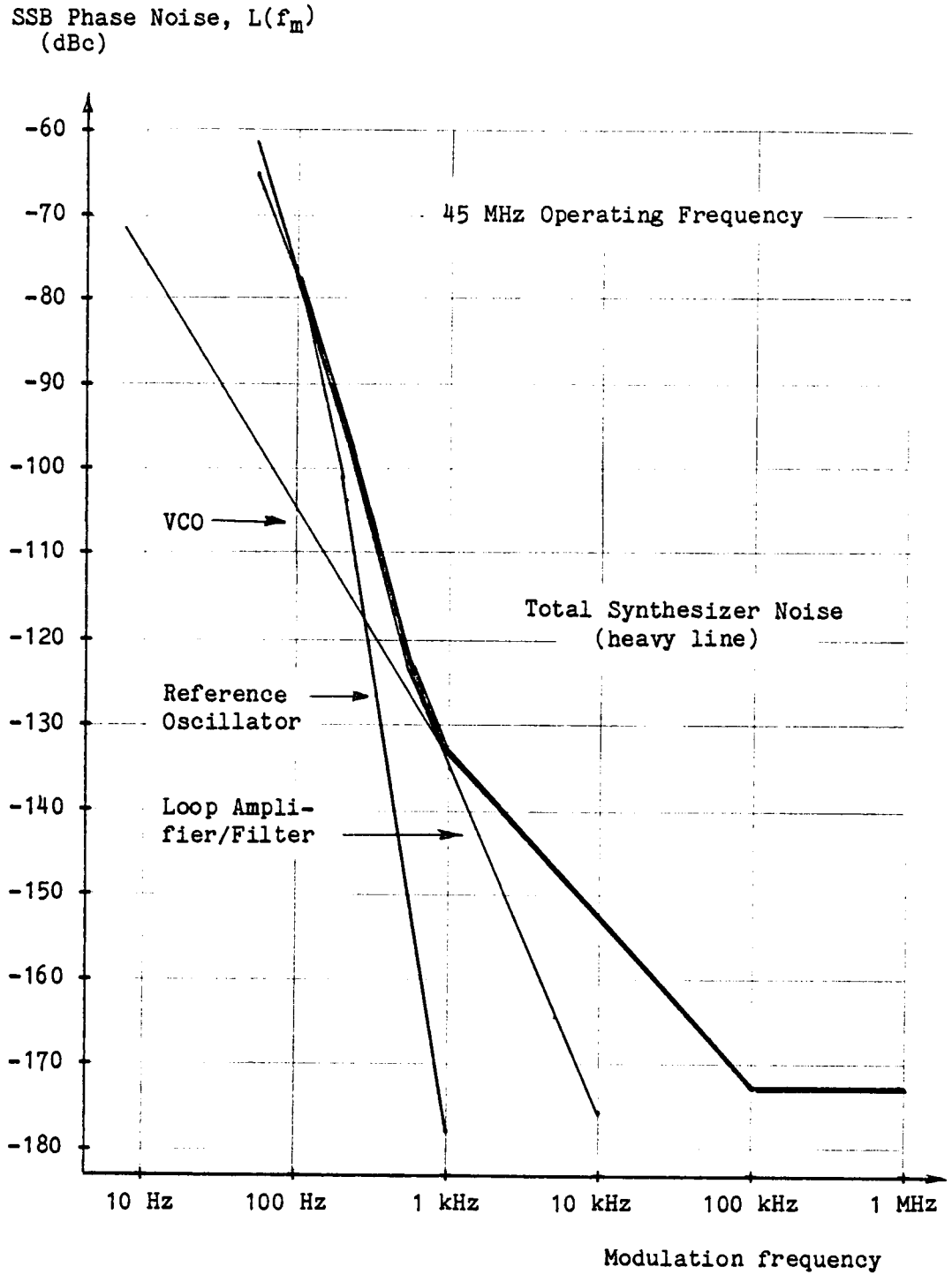


Figure 6.7. Predicted Phase Noise of the Synthesizer.

that these noise sources would have to be much greater than the reference oscillator noise to have an impact on the synthesizer noise. These noise components (phase detector noise, loop divider noise, and reference frequency noise) are acted upon by the closed loop gain, which rolls off very rapidly at frequencies above the loop bandwidth because the synthesizer is a sixth-order system. The high-order system is a requirement both for low phase noise and for low reference frequency sidebands.

The assumption of no phase detector and loop frequency divider noise is only valid because of the narrow bandwidth of the loop and the high loop order. These assumptions are certainly not valid for all synthesizer designs or applications. It is always necessary to evaluate the closed loop gain factor and to estimate noise contributions to determine if these are potentially troublesome noise sources.

Clearly, the VCO dominates the synthesizer phase noise at frequencies above 1 kHz which is why the major design emphasis was placed on its noise performance. The loop amplifier/filter noise contribution is not totally negligible and would almost certainly have become significant if the VCO gain were higher or if the loop amplifier/filter stage did not incorporate passive filtering immediately ahead of the varactor diode to minimize noise.

The predicted synthesizer noise exceeds the synthesizer design requirements of Table 1.1 and represents state-of-the-art performance. The actual synthesizer noise performance will be compared with the predicted noise performance and the noise design requirements later.

Synthesizer Reference Sideband Levels

Reference frequency ripple components in the phase detector output give rise to reference frequency sidebands in the synthesizer output spectrum. These sidebands are equally spaced on both sides of the carrier with a separation equal to the reference frequency. Reference frequency sideband levels may be calculated by determining the reference frequency (and reference frequency harmonic) contents appearing in the VCO tuning voltage.

As mentioned earlier in Section 3 in the "Phase Detectors" discussion, it is necessary to provide a current leakage path at the output of the CD4046 phase detector to keep its gain from dropping very low during phase-locked conditions. A significant loss of loop gain will result in instability in a lag-lead compensated PLL. As a result of this leakage path, reference frequency output pulses are always present in the output of the CD4046 phase detector. The height of these pulses is approximately 7.5 V, and they are of sufficient duration to overcome the leakage current.

The current provided by these pulses must equal the phase detector output leakage current. Mathematically stated,

$$(t/T)\cdot(V_0/R114) = I_L, \tag{6.19}$$

where t/T is the duty cycle of the output pulses, V_0 is the pulse amplitude, R114 is the series resistance from the phase detector output to the virtual ground of the active lag-lead filter, and I_L is the leakage current. Refer to the phase detector and loop amplifier/filter schematic of Figure 6.1 for the location of R114.

The leakage current (I_L) is approximately 68 nA, which is found by dividing the phase detector output bias voltage by R123, the resistor responsible for the leakage current. Solving Equation 6.19 for the pulse duty cycle gives

$$t/T = I_L\ (R114/V_0) = 68\ nA\ (\ 47\ k\ ohm/\ 7.5\ V) = 4.3 \times 10^{-4}. \quad (6.20)$$

The harmonic contents of a periodic pulse train can be found from Fourier series analysis. These components are given by

$$V_{rms}(n) = [\ \sqrt{2}\ V_0/(n\pi)\ ]\ \sin(n\pi t/T), \quad (6.21)$$

where n defines the harmonic, t/T is the pulse duty cycle, and V_0 is the pulse amplitude. Note if the duty cycle is much less than unity, the reference pulse train has harmonics of equal magnitude extending way up the frequency spectrum. In effect, this is equivalent to a periodic impulse signal.

The reference sideband levels are calculated by multiplying each phase detector reference frequency component by the gain of the loop amplifier/filter, $K_f(s)$. This evaluates the signal levels appearing directly at the VCO varactor. Sideband levels are then evaluated from

$$L_{sidebands}(nf_{ref}) = 1/2\ [\ V(nf_{ref})\ K_V/(nf_{ref})\ ]^2, \quad (6.22)$$

where L describes the ratio of the sideband to the carrier, n defines the reference frequency harmonic, f_{ref} is the reference frequency, $V(nf_{ref})$ is the reference signal component at the varactor, and K_V is the VCO gain. This equation is derived from Equation 4.8 in the

"Voltage Controlled Oscillator Gain Effects on Phase Noise" discussion of Section 4.

The calculations of reference frequency sidebands are presented in Table 6.2. A phase detector output voltage of 7.5 V, a phase detector output duty cycle of 4.3×10^{-4}, and a VCO gain of 150 kHz were used to make the calculations. The loop amplifier/filter attenuation was taken from the tabulated values in Figure 6.6. Note that all sidebands beyond the first sidebands are over 95 dB down. This sideband performance was only obtainable by using extensive lowpass filtering ahead of the VCO varactor and by minimizing the VCO gain. Equal sideband performance could also be attained by using a more elaborate phase detector and less lowpass filtering. This will be discussed later as a design improvement.

Table 6.2. Predicted Synthesizer Reference Sideband Levels.

Sideband frequency (Hz)	Phase detector signal component (V_{rms})	Component at VCO varactor (V_{rms})	Sideband-to-carrier ratio (dB)
1 kHz	4.6 mV	4.2 uV	- 67 dB
2 kHz	4.6 mV	0.27 uV	- 97 dB
3 kHz	4.6 mV	58.0 nV	-114 dB
4 kHz	4.6 mV	16.3 nV	-127 dB
5 kHz	4.6 mV	7.3 nV	-136 dB
6 kHz	4.6 mV	3.7 nV	-144 dB
7 kHz	4.6 mV	1.7 nV	-152 dB
8 kHz	4.6 mV	1.0 nV	-158 dB
10 kHz	4.6 mV	0.43 nV	-167 dB

Actual Synthesizer Performance

Several problems were encountered during the testing of the synthesizer. The most difficult problem was caused by the switched reactance tank circuit. Specifically, the inductor L207 was series resonating with the off-capacitance of PIN diode D207 when it was switched out of the circuit. This caused the tank circuit impedance to be very low at frequencies approaching 75 MHz. As a result, the VCO would not oscillate at the higher frequencies.

Since the tank circuit analysis program results and the oscillator starting gain calculations indicated that the PIN diode off-capacitance should not be a problem, it was determined that circuit board capacitance across the PIN diodes must be the culprit. Removing PIN diodes D205-D207 from the circuit board and placing them directly in series with the inductors solved the problem. The VCO now oscillated reliably at all frequencies. Only 0.7 pF of capacitance is required for series resonance with L207 at 75 MHz. The circuit board capacitance was adding a significant amount of capacitance to the 0.2 pF off-capacitance of the PIN diodes.

The VCO operating frequency deviated slightly from the tank circuit analysis results at frequencies over 60 MHz. This is probably a result of inaccurate tank circuit alignment or even coupling between the inductors. It was, however, not a serious problem, but will require a slight modification in the VCO presteering ROM truth table. Synthesizer testing was done without the VCO presteering ROM by connecting +5 V as required to the PIN diode bias resistors. The VCO

presteering ROM will be programmed later for the second generation synthesizer.

As mentioned earlier, the tank circuit RF voltages measured about one-half of the calculated values. This is probably due to tank circuit inaccuracies (such as errors in the estimated Q of the inductors), imperfect limiting in the sustaining amplifier, and measurement error. As a result of this, the bias current of Q201 and Q202 was raised to 8 mA from an initial value of 5 mA to achieve larger signal levels. It is believed that the improved circuit layout of the second generation synthesizer will eliminate the tank circuit deviations from the calculated analysis.

The synthesizer was completely stable at all operating frequencies. Its transient response was evaluated by observing the VCO varactor control voltage during step changes in the loop divider ratio. The loop risetime was approximately 20 ms, and the overshoot was approximately 20%. This is in good agreement with the synthesizer design natural frequency of 10 Hz and a damping of 0.707. The agreement is especially good considering the synthesizer is a sixth-order system because of the extensive lowpass filtering.

The programmable divider was tested separately initially and was found to operate up to 93 MHz. Its power consumption was 5 V at 125 mA, excluding the VCO presteering ROM. Two BCD coded thumbwheel switches were used to select the 10 MHz and 1 MHz frequency settings of the programmable divider. Small DIP switches were used for the other frequency settings.

It was necessary, as suggested by Rohde, to provide a leakage path at the output of the CD4046 phase detector. As mentioned earlier, this is required to prevent the phase detector gain from dropping very low under phase-locked conditions. A small, but unacceptable, loop oscillation was present if the leakage path provided by R123 (located at the phase detector output) was omitted. A value for R123 of 22 M ohm, which gives 68 nA of leakage, was determined to stop the oscillation. This worked well with different CD4046 phase detectors made by both RCA and Motorola.

It was noticed that the synthesizer phase noise increased occasionally for no apparent reason and that it was affected by bringing objects near the circuitry. Ferrite beads were placed on the gates of Q201 and Q202 and solved the apparent high frequency parasitic oscillation. It is believed that the circuit runs in the layout are too long, causing the problem.

The phase noise performance of the synthesizer is quite good and far exceeds the design specifications of Table 1.1. Synthesizer phase noise at 45 MHz is presented in Figure 6.8 and was measured using the phase noise test set described in Appendix D. Note that the noise floor of the test set is presented along with the measured phase noise of the synthesizer in the figure.

The measured synthesizer phase noise is approximately 10 dB higher than the predicted value in Figure 6.7. The higher actual phase noise is not surprising since the predicted phase noise is extremely low. Phase noise analysis by Leeson's model is perhaps not accurate for very large signals (3 Vrms) appearing at the sustaining

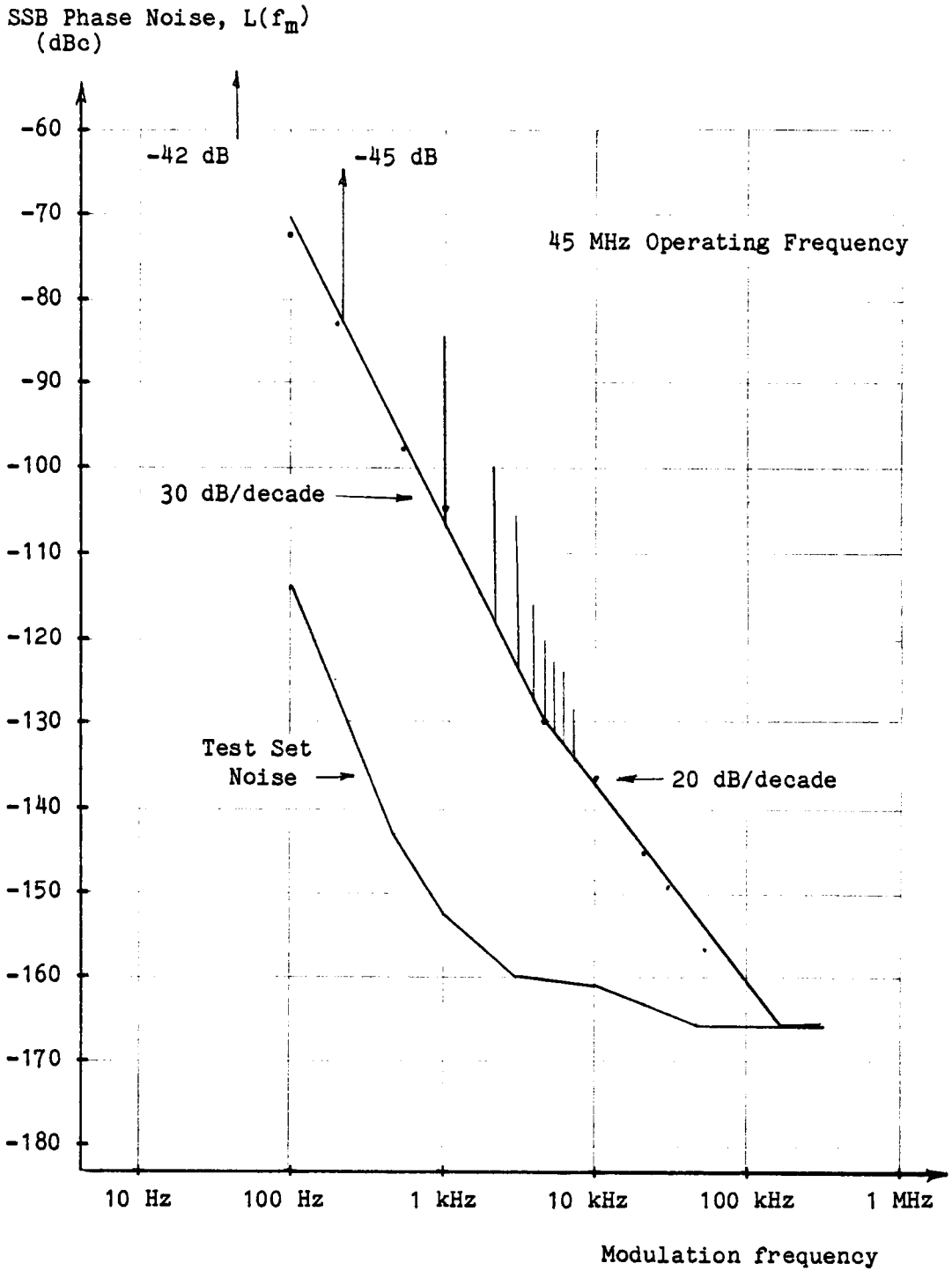


Figure 6.8. Actual Phase Noise of the Synthesizer.

amplifier input. It is interesting to note that the very low synthesizer phase noise floor could not be measured by the test set, which has a noise floor of -165 dBc.

Note that the measured synthesizer phase noise decreases at 30 dB/decade for frequencies below 5 kHz and decreases at 20 dB/decade for frequencies above 5 kHz. These phase noise slopes are in agreement with Leeson's model. The measured low frequency phase noise corner is approximately 5 kHz, which is higher than the assumed value of 1 kHz.

Synthesizer phase noise was also measured at 62 MHz, and was approximately 3 dB lower than the phase noise at 45 MHz. The lower phase noise at 62 MHz was not expected because of the higher carrier frequency and lower oscillator signal levels. Synthesizer phase noise performance at 45 MHz may have been degraded over performance at 62 MHz because of the excessively high sustaining amplifier input voltage (3 Vrms) at 45 MHz. The sustaining amplifier input voltage is lower (2 Vrms) at 62 MHz.

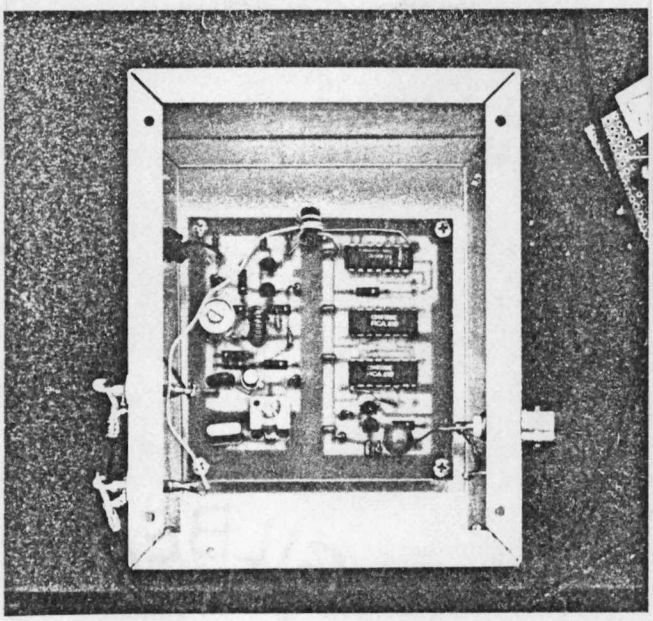
The reference sidebands near the carrier are lower than predicted in Table 6.2 and exceed the design requirements of Table 1.1. Note the presence of 60 Hz related power supply sidebands. These sidebands are always present in a synthesizer that is operated from ac power. With the improved shielding and power supply filtering planned, these sidebands should be lower in the second generation synthesizer.

It was necessary to evaluate synthesizer phase noise in an acoustically quiet location because of microphonics. Microphonics do not appear to be a problem above several kHz as most vibration frequencies

are below this. Probably the majority of microphonic effects are caused by vibration in the tank circuit inductors and capacitors, which results in a tank circuit frequency shift. Microphonics at frequencies above the loop bandwidth are not minimized by phase feedback within the synthesizer. For this reason, wideband PLLs are desirable for microphonic rejection.

A photograph of the synthesizer is shown in Figure 6.9. Note that the programmable divider circuit board is located outside of the aluminum shield box that houses the VCO, phase detector, and loop amplifier/filter. Also note the shielding between the circuits within the shield box. Finally, note that the reference frequency oscillator is housed in its own separate enclosure. Shielding will be even more extensive in the second generation synthesizer.

REFERENCE OSCILLATOR



MAIN SYNTHESIZER

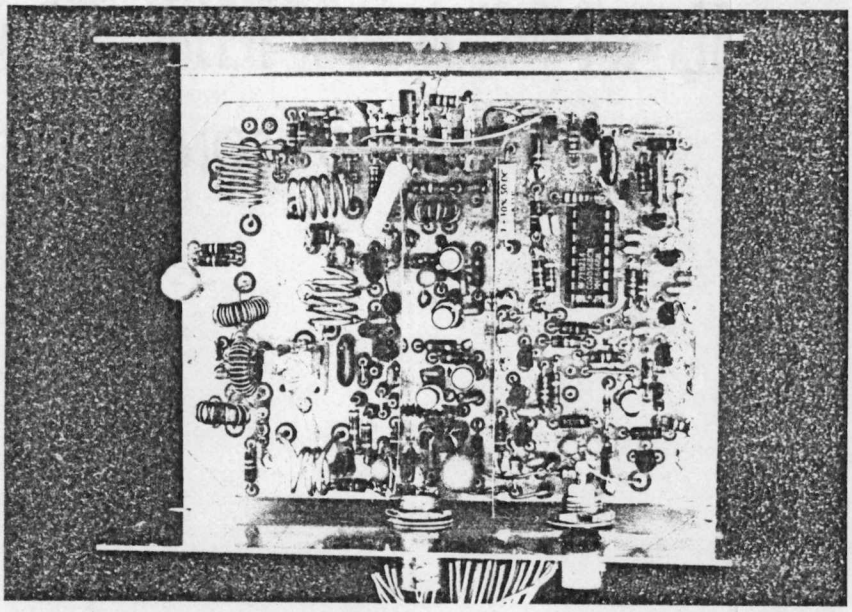


Figure 6.9. Photograph of the Synthesizer.

7. CONCLUSIONS

Suggested Improvements For The Synthesizer

A second generation synthesizer is planned and will be slightly different from the synthesizer presented in this thesis. The discrete loop amplifier/filter circuitry will be replaced with an operational amplifier. The noise performance of most operational amplifiers is sufficient for this circuit because of the extensive lowpass filtering. The discrete transistor two pole lowpass filter will not be changed as it offers good performance and circuit simplicity. The phase detector may be replaced with a more sophisticated design. Unfortunately, an improvement over the CD4046 phase detector is obtained only with a rather massive amount of circuitry. The phase detector logic circuits will be operated off a single supply voltage to eliminate the rather complex logic translation circuits and the $\pm$ 7.5 V bias levels.

The second generation synthesizer will be better shielded than the first generation unit. The phase detector circuitry will be mounted on its own circuit board and so will the loop amplifier/filter and the VCO. This will allow for very good shielding for these stages by mounting them in independent shield boxes. These boxes will be fabricated out of 0.032 inch printed circuit board copper-clad stock. An additional benefit will be the ability to try different circuitry easily by replacing the affected circuit module.

The circuit layout of the VCO will contain very short circuit lengths in the second generation synthesizer. Additionally, the

switched inductors will be better separated. It will still be necessary to mount some of the PIN diodes off the circuit board because of stray capacitance. To simplify the tank circuit, five switched inductors instead of six will be tried. It will then be necessary to use a higher capacitance change varactor diode system. Finally, transistor current sources will again be tried for biasing the sustaining amplifier. They should work well with the tighter circuit layout.

The programmable divider circuit will not be changed in the second generation synthesizer. A more modern design using the new high speed CMOS devices could be used, but would not improve the performance of the synthesizer. The phase detector, loop amplifier/filter, and VCO circuits are much simpler from a standpoint of the number of connections. Their new layouts will be small and challenging to design, but will not require much time to design. A new layout of the programmable divider (and VCO presteering ROM) could easily take a week to design.

The second generation synthesizer will be easier to build and could even be mass-produced. The use of toroidal inductors wound from the same powdered iron mix could be used to replace the air-wound inductors. This would make inductor alignment unnecessary in production. Minimum inductor alignment is a requirement to fabricate the synthesizer inexpensively. Finally, the second generation synthesizer will offer better performance and reliability. In particular, reference sidebands and power supply sidebands should be lower because of better shielding techniques.

Suggestions For Future Work In Low Noise Signal Source Design

Future work in low noise signal source design falls into two categories: innovative circuit ideas and improved analytical methods. As mentioned earlier, the use of lossless feedback (nonresistive transformer feedback) should be tried to make a linear low noise sustaining amplifier. Extensive amounts of feedback could be used to linearize the amplifier without degrading its noise performance. A more linear sustaining amplifier would have a lower phase modulation gain for bias supply and device noise. The result would be lower phase perturbations, especially at low frequencies.

A second circuit idea is to try an active Q multiplier in the parallel LC tank circuit of an oscillator. This suggestion came from the late Bill Managan and certainly warrants exploration since Driscoll's Q-multiplied crystal resonator circuit was successful.[46] Driscoll's circuit was discussed earlier in Section 4 in the "Resonator Choices" discussion. It is apparent from Leeson's oscillator model that an improvement in resonator Q is always welcomed in low noise signal source design. Of course, it is necessary that the noise introduced by a Q multiplier does not defeat its application. Conceivably, both Q multiplication and lossless feedback could be tried in an oscillator. The phase noise performance would have to be worth the effort a circuit of this complexity would require to build.

There is much work to be done in the area of analytical methods for low noise signal source design. Computer analysis using programs such as the SPICE program provides an idea of the noise phase

modulation in active devices that is caused by device nonlinearity. Perhaps through the use of nonlinear mathematics, a new improved oscillator model could be developed (if it does not already exist). The value of a model that is more complex than Leeson's model is questionable unless it can suggest additional low noise design strategies. Nonetheless, it would be desirable to model oscillator noise accurately, even if extensive device data were required for the model.

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LIST OF REFERENCES

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APPENDIXES

APPENDIX A

SOURCE LISTING FOR THE OSCILLATOR TANK CIRCUIT ANALYSIS PROGRAM

```
C       TANK CIRCUIT ANALYSIS FOR VOLTAGE CONTROLLED SWITCHED REACTANCE
C                       OSCILLATOR
C
C  DESCRIPTION
C
C       THIS PROGRAM EVALUATES THE EQUIVALENT PARALLEL L,C,R,Q, AND RES-
C       ONANT FREQUENCY OF A TANK CIRCUIT.
C
C       SIX INDUCTORS ARE SWITCHED BY BEING IN SERIES WITH CAPACITORS THAT ARE
C       SWITCHED FROM C TO 1,000,000C (REPRESENTING ESSENTIALLY A SHORT CIR-
C       CUIT) TO SIMULATE PIN DIODE SWITCHING OF THE ELEMENTS.  THE SWITCHING
C       IS IN A BINARY CODED FASHION REPRESENTED BY DECIMAL INTEGERS 0-63.
C
C       TWO FIXED INDUCTORS AND TWO FIXED CAPACITORS ARE INCLUDED IN THE CIR-
C       CUIT ALONG WITH A FIXED RESISTOR.
C
C
C
C
C
C  VARIABLE NAMES
C
C       N, INTEGER 0-63 REPRESENTING BINARY CODED PIN DIODE SWITCHING
C       K, REGISTER FOR N
C       J, SERIES CIRCUIT INDEX
C       M, ITERATION INDEX (3 ITERATIONS ARE PERFORMED FOR SOLUTION)
C       M1, REGISTER WITH VALUE M+1
C
C       L(J), A 6 ELEMENT DATA INPUT ARRAY OF INDUCTANCE VALUES
C       QL(J), A 6 ELEMENT DATA INPUT ARRAY OF Q (AT 50 MHZ) VALUES FOR L(J)
C       C(J), A 6 ELEMENT DATA INPUT ARRAY OF CAPACITANCE VALUES
C       R(J), A 6 ELEMENT DATA INPUT ARRAY OF RESISTANCE VALUES
C       A(J), A 6 ELEMENT ARRAY INDICATING PIN DIODE SWITCHING.
C               A(J)=1.0E6 PIN DIODE ON; A(J)=1.0 PIN DIODE OFF
C       LFIX, A FIXED INDUCTOR VALUE
C       QLFIX, Q (AT 50 MHZ)  OF LFIX
C       LRFC, INDUCTANCE OF AN RF CHOKE
C       QLRFC, Q OF LRFC
C       CVAR, TUNING DIODE CAPACITANCE
C       RCVAR, SERIES RESISTANCE OF CVAR
C       CFIX, CAPACITANCE OF A FIXED CAPACITOR
C       RFET, RESISTANCE OF A FIXED RESISTOR
C
C       QCVAR, Q OF CVAR
C       QLFX, Q AT FREQUENCY F(M) OF LFIX
C
C
C       X, TOTAL REACTANCE OF SERIES CIRCUIT BEING EVALUATED
C       RSER, TOTAL R OF SERIES CIRCUIT BEING EVALUATED
C       Q, Q OF SERIES CIRCUIT BEING EVALUATED
C               X AND Q ARE POSITIVE IF CIRCUIT IS 'INDUCTIVE, NEGATIVE
C               IF CIRCUIT IS CAPACITVE
C
C
C       BL, TOTAL RECIPRICOL INDUCTANCE OF TANK CIRCUIT
C       G, TOTAL CONDUCTANCE OF TANK CIRCUIT
C       CTOT, TOTAL CAPACITANCE OF TANK CIRCUIT
C       RTOT, TOTAL RESISTANCE OF TANK CIRCUIT
C       LTOT, TOTAL INDUCTANCE OF TANK CIRCUIT
C       QTOT, TOTAL Q OF TANK CIRCUIT
```

```
C       F(M), RESONANT FREQUENCY (HZ) OF TANK CIRCUIT USED DURING ITERATIONS
C       F(M+1 OR M1), RESONANT FREQUENCY (HZ) OF TANK CIRCUIT CALCULATED
C               AFTER THE Mth ITERATION
C       W, RESONANT FREQUENCY OF TANK CIRCUIT IN RADIANS/SEC
C
C
C  SPECIFICATION STATEMENTS
C
        INTEGER*2 N,K,J,M,M1
        REAL*4 L(6),C(6),R(6),A(6),QL(6),X,Q,BL,G,CTOT,LTOT,QTOT,RTOT,
        1       F(4),W,LFIX,LRFC,CVAR,RCVAR,CFIX,RFET,QLFIX,QLRFC,RSER
        1       ,QCVAR,QLFX
C
C       DATA INPUT STATEMENTS
C
C
        DATA L/3.2E-6,1.6E-6,0.8E-6,0.4E-6,0.2E-6,0.1E-6/
        DATA QL/150.,150.,150.,300.,300.,300./
        DATA R/1.0,1.0,1.0,1.0,1.0,0.35/
        DATA C/0.2E-12,0.2E-12,0.2E-12,0.2E-12,0.2E-12,2.0E-12/
        DATA LFIX,QLFIX,LRFC,QLRFC,CVAR,RCVAR,CFIX,RFET/0.105E-6
        1       ,150.,2.2E-6,50.0,20.0E-12,0.1,101.4E-12,25.0E3/
C
C
C  PRINTING OUT COMPONENT VALUES
C
C
        WRITE (1,90) L(1),L(2),L(3),L(4),L(5),L(6),LFIX,LRFC
        WRITE (5,90) L(1),L(2),L(3),L(4),L(5),L(6),LFIX,LRFC
        WRITE (1,91) C(1),C(2),C(3),C(4),C(5),C(6),CVAR,CFIX
        WRITE (5,91) C(1),C(2),C(3),C(4),C(5),C(6),CVAR,CFIX
        WRITE (1,92) R(1),R(2),R(3),R(4),R(5),R(6),RCVAR,RFET
        WRITE (5,92) R(1),R(2),R(3),R(4),R(5),R(6),RCVAR,RFET
        WRITE (1,93) QL(1),QL(2),QL(3),QL(4),QL(5),QL(6),QLFIX,QLRFC
        WRITE (5,93) QL(1),QL(2),QL(3),QL(4),QL(5),QL(6),QLFIX,QLRFC
90      FORMAT (3X,'L= ',8(1PE9.2))
91      FORMAT (3X,'C= ',8(1PE9.2))
92      FORMAT (3X,'R= ',8(1PE9.2))
93      FORMAT (3X,'Q= ',8(1PE9.2))
C
C
C  LABELING COLUMN HEADINGS
C
C
        WRITE (1,95)
        WRITE (5,95)
95      FORMAT (1X,' ')
        WRITE (1,95)
        WRITE (5,95)
C
C
        WRITE (1,100)
        WRITE (5,100)
100     FORMAT(1X,'N',T18,'LAST F',T36,'F',T54,'L TOTAL',T72,'C TOTAL',
        1       T90,'R TOTAL',T108,'Q')
C
        WRITE (1,95)
        WRITE (5,95)
C
C
C  MAIN LOOP FOR CALCULATING ALL SETTINGS , N
C
        DO 40 N=0,63
```

```
C
C       COMPUTING ARRAY A TO REPRESENT PIN DIODE SETTINGS
C
        K=N
        DO 10 J=1,6
                IF (ISHFT(K,16-J).LT.0) THEN
                A(J)=1.0E6
                ELSE
                A(J)=1.0
                END IF
10      CONTINUE
C
C
C       SETTING INITIAL RESONANT FREQUENCY FOR FIRST ITERATION
C
        F(1)=5.0E7
C
C       ITERATION LOOP FOR CALCULATIONS
C
        DO 30 M=1,3
                BL=0.0
                CTOT=0.0
                G=0.0
                W=2.0*3.1415927*F(M)
C
C               CALCULATING SERIES CIRCUITS 1-6 SUCCESSIVELY
C
                DO 20 J=1,6
                        X=W*L(J)-1.0/(W*C(J)*A(J))
                        RSER=R(J)+W*L(J)/(QL(J)*SQRT(F(M)/50.E6))
                        G=X/RSER
                        IF (X .LT. 0.0) THEN
                        CTOT=-1.0*(G**2/(G**2+1.0))/(W*X) +CTOT
C
C                       THE CIRCUIT IS CAPACITIVE AND ADDS TO CTOT
C
                        ELSE
                        BL=(G**2/(G**2+1.0))*W/X +BL
C
C                       THE CIRCUIT IS INDUCTIVE AND ADDS TO BL
C
                        END IF
C
                        G=1.0/((RSER)*(1.0+G**2)) +G
20              CONTINUE
C
C
C               CALCULATING THE EFFECTS OF THE UNSWITCHED ELEMENTS
C
                QCVAR=1.0/(RCVAR*W*CVAR)
                QLFX=QLFIX*SQRT(F(M)/50.0E6)
C
                CTOT=CTOT+CFIX+CVAR*QCVAR**2/(1.0+QCVAR**2)
                BL=BL+(QLFX**2/(QLFX**2+1.0))/LFIX
     1                  +(QLRFC**2/(QLRFC**2+1.0))/LRFC
                G=G+1.0/(QLFX*W*LFIX)+1.0/(QLRFC*W*LRFC)+
     1                  1.0/(RCVAR*(QCVAR**2+1.0))+1.0/RFET
C
C
C
C
C               CALCULATING THE RESONANT FREQUENCY FOR THE NEXT ITERATION
C                       OF CALCULATIONS
```

```
C
                M1=M+1
                F(M1)=1.0/(2.0*3.1415927*SQRT(CTOT/BL))
C
C
30      CONTINUE
C
C       SOLVING FOR THE FINAL RESULTS
C
        RTOT=1.0/G
        LTOT=1.0/BL
C
        GTOT=1.0/(2.0*3.1415927*F(M1)*LTOT*G)
C
C       WRITING OUTPUT
C
C
        WRITE(1,110) N,F(M),F(M1),LTOT,CTOT,RTOT,GTOT
        WRITE(5,110) N,F(M),F(M1),LTOT,CTOT,RTOT,GTOT
110     FORMAT(3X,I3,6(1PE18.6) )
C
C
C       CONTINUE ON TO NEXT SETTING OF N
C
40      CONTINUE
        STOP
        END
```

APPENDIX B

SPICE PROGRAM SOURCE LISTING FOR THE LOOP AMPLIFIER/FILTER NOISE ANALYSIS

```
LOOP AMPLIFIER/FILTER NOISE ANALYSIS FOR THE 45-75 MHZ SYNTHESIZER  AMPFLT.SPI
*
*********************************************************************
*       ANALYSIS PURPOSE
*********************************************************************
*
*
* THIS ANALYSIS DETERMINES THE OUTPUT NOISE OF THE LOOP AMPLIFIER/FILTER
* FOR THE 45-75 MHZ SYNTHESIZER.  THE CIRCUIT IS ANALYZED ASSUMING AN
* INFINATE DRIVING IMPEDANCE FROM THE PHASE DETECTOR, WHICH IS INDICATIVE
* OF PHASE LOCKED CONDITIONS.
*
* AN INPUT BIAS CURRENT SOURCE, IBIAS, IS CONNECTED TO THE INPUT OF THE CIRCUIT
* TO ESTABLISH DC BIASING.  A RESISTOR, RBIAS, OF 1000 MEG OHMS IS PARALLELED
* ACROSS C112 TO PROVIDE A DC FEEDBACK PATH SO THAT PROPER DC BIASING CAN
* OCCUR.  THESE ELEMENTS DO NOT AFFECT THE CIRCUIT NOISE, AND ARE USED TO SET
* THE OUTPUT VOLTAGE OF THE CIRCUIT AT APPROXIMATELY 18 VDC.
*
* ALL TRANSISTORS HAVE AN ASSUMED 1/F NOISE CORNER FREQUENCY OF 1 KHZ
*
* OUTPUT NOISE VOLTAGE HAS UNITS OF V/ROOT HZ.
*
*********************************************************************
*
*       POWER SUPPLY VOLTAGE
*
VCC 1 0 24V
*
*       INPUT BIAS CURRENT SOURCE
*
IBIAS 2 0 82NA
*
*********************************************************************
*       LAG/LEAD CIRCUITRY
*********************************************************************
*
R123 2 0 22MEG
R114 2 3 47K
J108 4 3 0 J309
D109 0 6 D1N5228
D108 6 5 D1N5228
C110 5 0 1UF
Q109 7 5 4 Q2N3904
C111 7 0 100PF
R115 5 8 16K
Q110 7 8 9 Q2N3906
R116 9 1 120
D106 1 10 D1N914
D107 10 8 D1N914
Q111 1 7 11 Q2N3904
R117 11 0 16K
Q112 1 11 12 Q2N3904
R118 12 0 5.1K
C112 12 13 0.1UF
R119 3 13 220K
C113 3 13 2000PF
*
*       PARALLELING RBIAS ACROSS C112 TO ESTABLISH DC BIASING
*
RBIAS 12 13 1000MEG
*
*********************************************************************
* 3 POLE LOWPASS FILTER CIRCUITRY
```

```
*******************************************************************************
*
R120 12 14 16K
R121 14 15 16K
Q113 1 15 16 Q2N5089
R122 16 0 6.81K
C117 14 16 0.2UF
C118 15 0 0.047UF
R201 16 17 16K
C209 17 0 0 11UF
*
*******************************************************************************
* DEVICE MODELS
*******************************************************************************
*
*       NOTE: ALL TRANSISTORS HAVE AN ASSUMED 1/F NOISE CORNER OF 1 KHZ.
*
*       JFET MODEL
*
.MODEL J309 NJF VTO=-2.5V BETA=3.2M  LAMBDA=0.05 RD=20 RS=20 CGS=10PF CGD=5PF
+ AF=1 KF=0.015F
*
*       BIPOLAR TRANSISTOR MODELS
*
.MODEL Q2N3904 NPN IS=2FA BF=200 IKF=100MA ISE=1PA NE=2 VAF=100V RB=200
+ RBM=100 IRB=100MA RC=2.5 RE=0.3 CJE=4.5PF CJC=3.5PF TF=0.5NS XTF=1.1
+ VTF=1V ITF=100MA KF=0.32F
*
.MODEL Q2N3906 PNP IS=2FA BF=200 IKF=100MA ISE=1PA NE=2 VAF=100V RB=200
+ RBM=100 IRB=100MA RC=2.5 RE=0.3 CJE=4.5PF CJC=3.5PF TF=0.5NS XTF=1.1
+ VTF=1V ITF=100MA KF=0.32F
*
.MODEL Q2N5089 NPN IS=20FA BF=750 IKF=12MA ISE=1PA NE=2 VAF=92V RB=800
+ RBM=500 IRB=12MA RC=63 RE=0.33 CJE=6PF CJC=4PF TF=0.22NS XTF=1.1
+ VTF=1V ITF=12MA KF=0.32F
*
*       DIODE MODELS
*
.MODEL D1N914 D IS=10FA RS=0.3 CJO=2PF
*
.MODEL D1N5228 D BV=4.3V IBV=20MA
*
*
*******************************************************************************
* ANALYSIS COMMANDS
*******************************************************************************
*
.NODESET V(3)=-1.5V
.AC DEC 10 10 100KHZ
.NOISE V(17) IBIAS 10
.PLOT NOISE ONOISE
.END
```

APPENDIX C

SOURCE LISTING FOR THE SYNTHESIZER FREQUENCY AND PHASE RESPONSE PROGRAM

```
C       PLLRES.FOR
C       11/24/83
C
C       THIS PROGRAM COMPUTES PLL AMPLIFIER/FILTER RESPONSE,
C       PLL LOOP GAIN RESPONSE, PLL CLOSED LOOP RESPONSE, AND
C       PLL ERROR RESPONSE.
C
C               LOOP AMPLIFIER/FILTER DETAILS
C
C  [ACTIVE LAG-LEAD +SINGLE POLE LPASS]        [3RD ORDER LPASS]
C       Made up of lag-lead active filter    Made up of 2nd order
C       with added real pole                 lowpass with single
C                                            pole lpass at varactor
C
C               INPUT VARIABLES
C
C       KD      PHASE DETECTOR GAIN (VOLTS/CYCLE)
C       KV      VCO GAIN (HZ/VOLT)
C       NDIV    DIVIDER RATIO
C
C       T1      LAG-LEAD FILTER ZERO TIMECONSTANT
C       T2      LAG-LEAD FILTER POLE TIMECONSTANT
C       FC0     -3DB FREQ OF SINGLE POLE LPASS ADDED TO LAG-LEAD
C
C       FC2ND   -3DB FREQ OF 2ND ORDER LOWPASS
C       ZETA    DAMPING OF 2ND ORDER LOWPASS
C       FC1     -3DB FREQ OF SINGLE POLE LPASS ADDED TO 2ND ORDER LP
C
C       NPTS    NUMBER OF FREQUENCY POINTS USED IN CALCULATIONS
C       SCALE(20)       AN ARRAY OF LOG COMPRESSED VALUES FOR FREQS
C
C               CALCULATED VARIABLES
C
C       S       COMPLEX FREQUENCY VARIABLE
C       FREQ(NPTS)      ARRAY OF FREQUENCY VALUES
C
C       KFMAG(NPTS)     ARRAY OF LOOP FILTER MAGNITUDES VS FREQ
C       KFPHA(NPTS)     ARRAY OF LOOP FILTER PHASES VS FREQ
C
C       TMAG(NPTS)      ARRAY OF LOOP GAIN MAGNITUDES VS FREQ
C       TPHA(NPTS)      ARRAY OF LOOP GAIN PHASES VS FREQ
C
C       ACLMAG(NPTS)    ARRAY OF CLOSED LOOP GAIN VS FREQ
C
C       ERRMAG(NPTS)    ARRAY OF LOOP ERROR MAGNITUDE VS FREQ
C
C       KF      COMPLEX VARIABLE FOR LOOP AMP/FILTER
C       T       COMPLEX VARIABLE FOR LOOP GAIN
C       ACL     COMPLEX VARIABLE FOR CLOSED LOOP GAIN
C       ERROR   COMPLEX VARIABLE FOR LOOP ERROR GAIN
C
C       TL0     TIMECONSTANT ASSOCIATED WITH THE SINGLE POLE LPASS
C                       ADDED TO THE LAG-LEAD FILTER
C       TL1     TIMECONSTANT ASSOCIATED WITH THE SINGLE POLE LPASS
C                       ADDED TO THE 2ND ORDER LPASS FILTER
```

```
C       WC2ND   FC2ND EXPRESSED IN RADS/SEC
C       WC2ND2  WC2ND SQUARED
C       WCZET2  2.0*ZETA*WC2ND2
C
C       G       DC LOOP GAIN
C
C
C
C
C
C               VARIABLE DEFINITIONS
C
        REAL K0,KV,SCALE(20),FREQ(100),KFMAG(100),KFPHA(100),
       1        TMAG(100),TPHA(100),ACLMAG(100),ERRMAG(100),NDIV
C
        COMPLEX KF,T,ACL,ERROR,S
C
C       THE FOLLOWING DECLARATION IS REQUIRED IN SS FORTRAN ONLY
        COMPLEX CMPLX
C
C               INITIALIZING VARIABLES
C
        DATA SCALE /1.00,1.12,1.26,1.41,1.59,1.78,2.00,2.24,2.51,
       1        2.82,3.16,3.55,3.98,4.47,5.01,5.62,6.31,7.08,7.94,
       1        8.91/
C
        NPTS = 100
C
C               INPUTTING VARIABLES FROM THE KEYBOARD
C
        WRITE (1,10)
10      FORMAT (1X, 'ENTER K0,KV IN FLOAT PT OR SCI NOTATION : '$
        READ (1,20) K0,KV
20      FORMAT (2G0.0)
C
        WRITE (1,30)
30      FORMAT (1X, 'ENTER NDIV IN FLOAT PT FORM : '$
        READ (1,40) NDIV
40      FORMAT (G0.0)
C
        WRITE (1,50)
50      FORMAT (1X, 'ENTER T1,T2,FC0 IN FL PT OR SCI NOT : '$
        READ (1,60) T1,T2,FC0
60      FORMAT (3G0.0)
C
        WRITE (1,70)
70      FORMAT (1X, 'ENTER FC2ND,ZETA,FC1 IN FL PT OR SCI NOT : '$
        READ (1,80) FC2ND,ZETA,FC1
80      FORMAT (3G0.0)
C
C               COMPUTING DC LOOP GAIN
C
        G = K0*KV/NDIV
C
C               PRINTING OUT THE INPUT PARAMETERS AND G
```

```
      WRITE (1,1)
1     FORMAT (1X, ' ')
      WRITE (1,100)
100   FORMAT (1X, 'K0 (VOLTS/CYCLE)  KV (HZ/VOLT)   NDIV')
      WRITE (1,110) K0,KV,NDIV
110   FORMAT (5X,1P3E12.3)
      WRITE (1,1)
      WRITE (1,120)
120   FORMAT (1X, '       T1 (SEC)    T2 (SEC)     FC0 (HZ)')
      WRITE (1,130) T1,T2,FC0
130   FORMAT (5X,1P3E12.3)
      WRITE (1,1)
      WRITE (1,140)
140   FORMAT (1X, '       FC2ND (HZ)   ZETA        FC1 (HZ)')
      WRITE (1,150) FC2ND,ZETA,FC1
150   FORMAT (5X,1P3E12.3)
      WRITE (1,1)
      WRITE (1,160)
160   FORMAT (1X, 'DC LOOP GAIN (1/SEC)' )
      WRITE (1,170) G
170   FORMAT (5X,1PE12.3)
      WRITE (1,1)
C
C
C               COMPUTING THE FREQUENCY ARRAY
C
      INDEX = 0
C
C     LOOP FOR EACH DECADE OF FREQUENCY
C
      DO 1000 N = 1,5
C
C               LOOP FOR EACH MANTISSA FREQUENCY VALUE
C
               DO 1010 M = 1,20
               INCREMENT INDEX
               FREQ(INDEX) = SCALE(M)*10.0**(N-1)
1010           CONTINUE
1000  CONTINUE
C
C
C               CONVERTING INPUT VALUES TO OTHER FORMS
C
      TL0 = 1.0/(6.28319*FC0)
      TL1 = 1.0/(6.28319*FC1)
      WC2ND = 6.28319*FC2ND
      WC2ND2 = WC2ND**2
      WCZET2 = WC2ND*ZETA*2.0
C
C -------------------------------------------------------------------
C               LOOP FOR EACH FREQUENCY VALUE
C -------------------------------------------------------------------
C
      DO 2000 N = 1,NPTS
C
```

```
        S = CMPLX (0.0, 6.28319*FREQ(N) )
C
C ---------------------------------------------------------------
C       COMPUTING THE LOOP FILTER RESPONSE
C ---------------------------------------------------------------
C
        KF = ((S*T2 +1.0)/(S*T1)) * (1.0/((1.0 +TL0*S)*(1.0 +TL1*S)))
        1       * WC2ND2/( S*S + WCZET2*S + WC2ND2 )
C
        KFMAG(N) = 20.0*ALOG10( CABS(KF))
        KFPHA(N) = 57.2958*ATAN2( AIMAG(KF), REAL(KF) )
C
C
C ---------------------------------------------------------------
C       COMPUTING THE LOOP GAIN
C ---------------------------------------------------------------
C
        T = KF*G/S
C
        TMAG(N) = 20.0*ALOG10( CABS(T))
        TPHA(N) = 57.2958*ATAN2( AIMAG(T), REAL(T) )
C
C
C ---------------------------------------------------------------
C       COMPUTING THE CLOSED LOOP GAIN
C ---------------------------------------------------------------
C
        ACLMAG(N) = 20.0*ALOG10( CABS(T/(T+1.0)) )
C
C
C ---------------------------------------------------------------
C       COMPUTING THE ERROR RESPONSE
C ---------------------------------------------------------------
C
        ERRMAG(N) = 20.0*ALOG10( CABS(1.0/(1.0+T)) )
C
C
C ---------------------------------------------------------------
C       GOING TO NEXT FREQ VALUE AND REPEATING CALCULATIONS
C ---------------------------------------------------------------
C
2000    CONTINUE
C
C
C
C ---------------------------------------------------------------
C       PRINTING OUT COMPUTED DATA
C ---------------------------------------------------------------
C
C
        WRITE (1,1)
C
C               LABELLING THE COLUMN HEADINGS
C
        WRITE (1,3010)
```

```
3010    FORMAT (5X,'FREQUENCY',7X,'AMP/FILTER',10X,'LOOP GAIN',7X,
        1        'PLL GAIN',2X,'PLL ERROR')
        WRITE (1,3020)
3020    FORMAT (25X,'KF',18X,'T',12X,'T/(1+T)',3X,'1/(1+T)')
        WRITE (1,3030)
3030    FORMAT (22X,'MAG   PHASE',7X,'MAG    PHASE',7X,'MAG',
        1        8X,'MAG')
        WRITE (1,3040)
3040    FORMAT (7X,'(HZ)',10X,'(dB)   (DEG)',7X,'(dB)    (DEG)',7X,
        1        '(dB)',7X,'(dB)')
        WRITE (1,1)
C
C
C       PRINTING OUT THE VALUES
C
        DO 4000 N = 1,NPTS
C
        WRITE (1,4010) FREQ(N),KFMAG(N),KFPHA(N),TMAG(N),TPHA(N),
        1       ACLMAG(N),ERRMAG(N)
4010    FORMAT (1X,F10.2,3X,6F10.2)
C
4000    CONTINUE
        STOP
        END
```

APPENDIX D

PHASE NOISE TEST SET USED TO MEASURE THE SYNTHESIZER PHASE NOISE

Theory Of Operation

A block diagram of the phase noise test set is shown in Figure D.1, which includes signal levels and descriptive information. Note that the phase of a low noise reference oscillator is compared to the phase of the oscillator under test by a phase detector. If the phase noise of the reference oscillator is much less than the phase noise of the oscillator under test, then the phase detector output voltage is an accurate signature of the time-varying phase noise in the oscillator under test.

It is necessary that the phase detector be operated under phase quadrature conditions for linear phase comparison and minimun sensitivity to AM noise in the oscillator signals. Since it is virtually impossible manually to tune the reference oscillator to track the oscillator under test, a phase-locked loop is used. This phase-locked loop is designed to hold long-term phase quadrature between the two oscillators while not tracking the short-term phase variations in the oscillator under test. Phase noise at frequencies above the loop bandwidth of the phase-locked loop appears directly in the phase detector output as the loop cannot track it. Stated differently, the phase noise of the oscillator under test is acted upon by the loop-error response, which approaches a value of unity for frequencies above the loop bandwidth.

Since it is so important to assure that the loop bandwidth is significantly less than the minimum desired measured phase noise frequency, the loop features four settings of loop bandwidth, 1 Hz, 10 Hz, 100 Hz, and 1 kHz. The lower frequency settings are used for

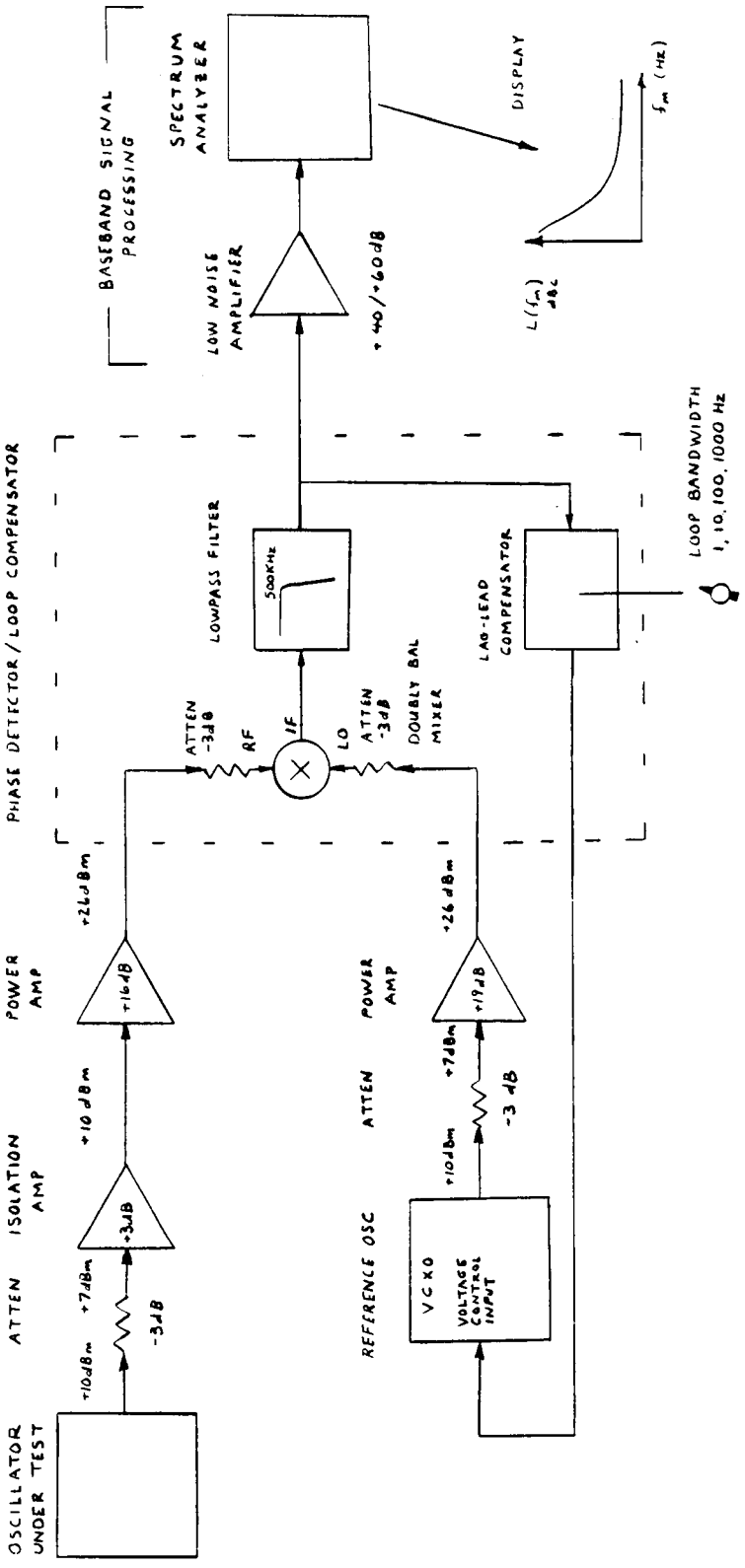

Figure D.1. Block Diagram of the Phase Noise Test Set.

measuring phase noise close to the carrier. The higher frequency settings are very convenient for measuring phase noise at high phase noise frequencies because they allow the loop to reject the very large low frequency noise components that would otherwise limit the dynamic range of the measurements.

As discussed earlier in Section 2 in the "Measurement of Phase Noise" discussion, there are several critical design considerations in this type of phase noise test set. First, since the test set actually compares phase between the oscillators, the reference oscillator phase noise must be either much lower than the oscillator under test or it must be subtracted from the measurement.[14] Second, injection locking between the oscillator under test and the reference oscillator must be prevented as this causes the oscillators to track each other's phase noise, particularly at low frequencies.[15,16] Finally, the phase detector must be a high level detector to achieve a low noise floor and the low noise amplifier must have good low noise performance.[15]

The test set noise floor may be determined by comparing two identical oscillators. If it is assumed that these oscillators have equal phase noise, the test set phase noise floor is 3 dB below the measured noise floor obtained by comparing the two oscillators. The 3 dB correction takes into account the uncorrelated summing of the oscillator phase noises. It is important to determine the phase noise floor of the test set to be assured that it is less than the oscillator under test.

Circuit Description

The reference oscillator is a low noise voltage controlled crystal oscillator, using the crystal in the series resonant overtone mode. A schematic diagram of this oscillator is shown in Figure D.2. Note the similarity between its design and the design of the reference oscillator for the synthesizer that was discussed in Section 6 in the "Reference Frequency Oscillator Discussion." With the varactor tuning, the gain of the test set reference oscillator is approximately 300 Hz/volt. Two of these oscillators were constructed so they could be compared against each other to determine the test set noise floor.

The phase detector and loop compensation circuitry contains a high level doubly balanced mixer for the phase detector and an active lag-lead filter to provide loop compensation. A schematic of this circuitry is shown in Figure D.3.

The doubly balanced mixer IF output is connected to a lowpass filter to reject the very strong sum frequency image. Note that at this image frequency the mixer IF output is terminated into 50 ohms. This is important to maintain isolation between the RF and LO ports of the mixer and to assure proper mixer operation. The lowpass filter is similar to the filter described by Fischer for a phase noise measuring circuit.[15] Note that the filter presents a much higher impedance than 50 ohms at low frequencies (below 1 MHz), which unloads the mixer and increases its phase detection gain. The measured gain of the phase detection circuitry is 1.7 V/rad, which was measured by unlocking the test set and measuring the peak sinusoidal difference frequency signal at the mixer IF output. The peak value of the difference frequency

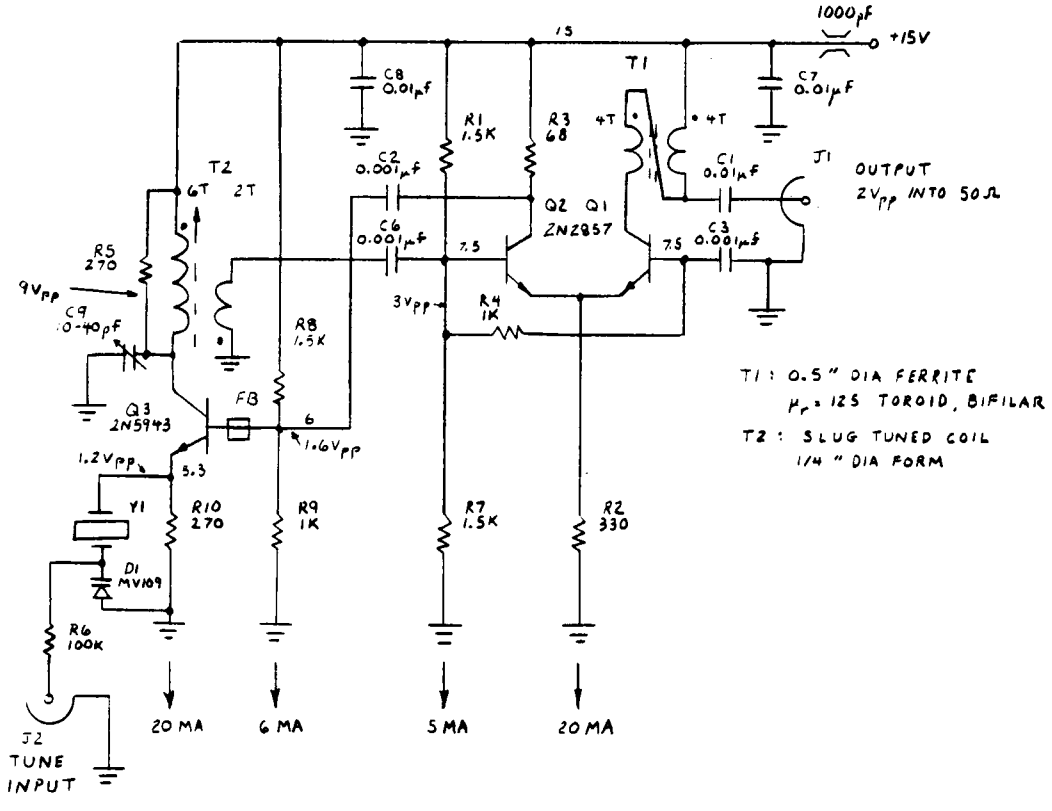

Figure D.2. Schematic Diagram of the Reference Oscillator for the Phase Noise Test Set.

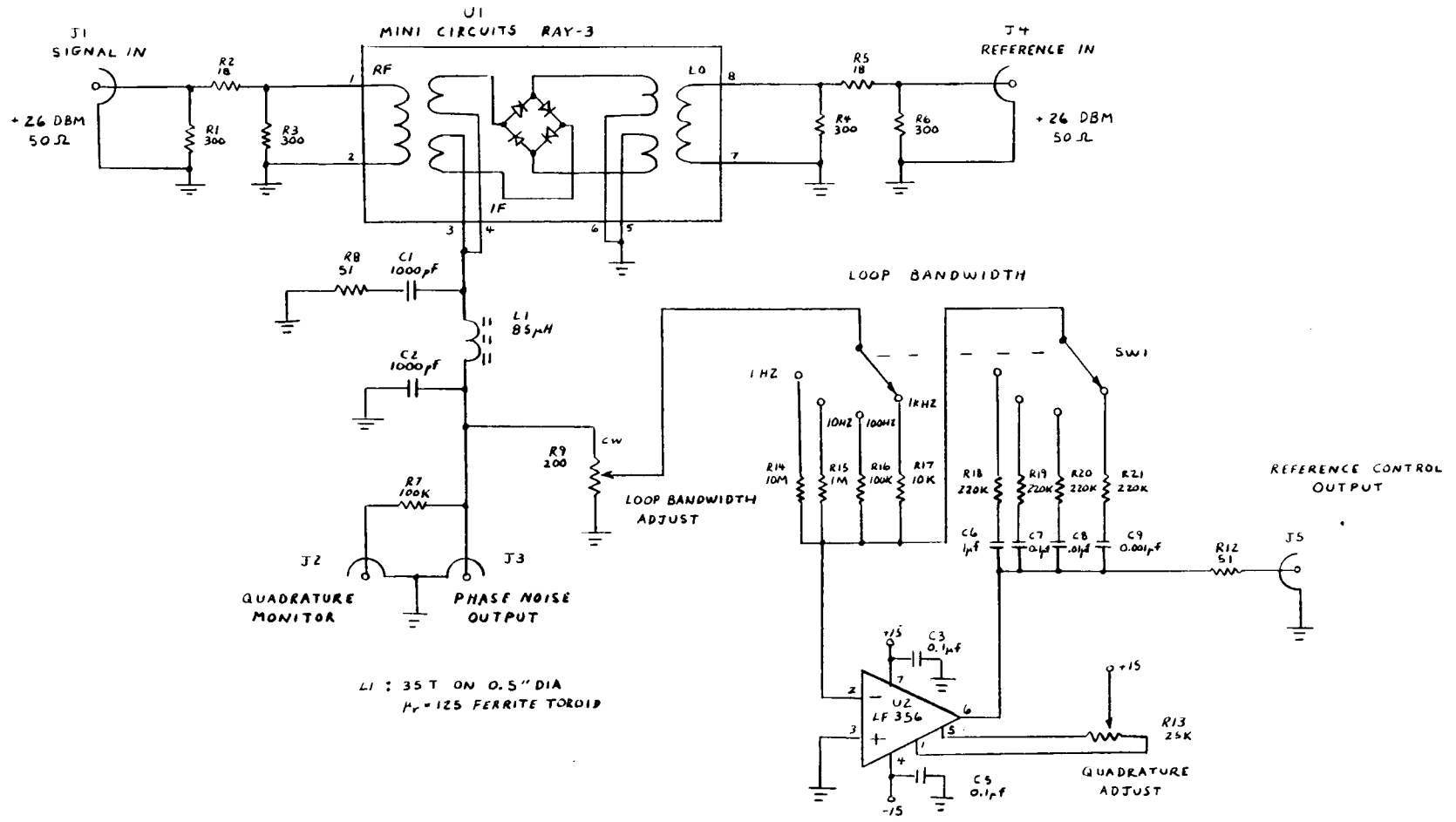

Figure D.3. Schematic Diagram of the Phase Detector and Loop Compensator for the Phase Noise Test Set.

signal is equal to the phase detector gain if the detector is operating as a linear detector.[6] For greater precision, a known phase modulation should be measured to determine phase detector gain.

The loop compensation circuitry consists of an active lag-lead network. The extremely high dc gain of this network assures that the two oscillators remain in long-term phase quadrature. During phase quadrature the phase detector output is at a dc level of 0 V, excepting phase offset errors in the detector.

As mentioned, the loop bandwidth is variable to optimize the dynamic range of phase noise measurements in different frequency ranges. This is accomplished by the switch-selectable lag-lead parameters.

The power amplifier is a broadband single stage RF amplifier using base-collector feedback. Its gain and signal levels are shown in the test set block diagram of Figure D.1. It uses the 2N5109 transistor, which is a low noise medium power RF device. Noise performance of the amplifiers used in the test set is somewhat important because of additive phase noise. However, the large signal levels present in the test set would assure a good signal-to-noise ratio even if the amplifiers were not particulary low noise circuits. A schematic diagram of the power amplifier is shown in Figure D.4.

A schematic diagram of the isolation amplifier is shown in Figure D.5. It has a measured isolation of over 60 dB at 50 MHz. The estimated isolation between the oscillator under test and the reference oscillator is over 100 dB. This is sufficient, especially since phase noise very close to the carrier is not being measured in the

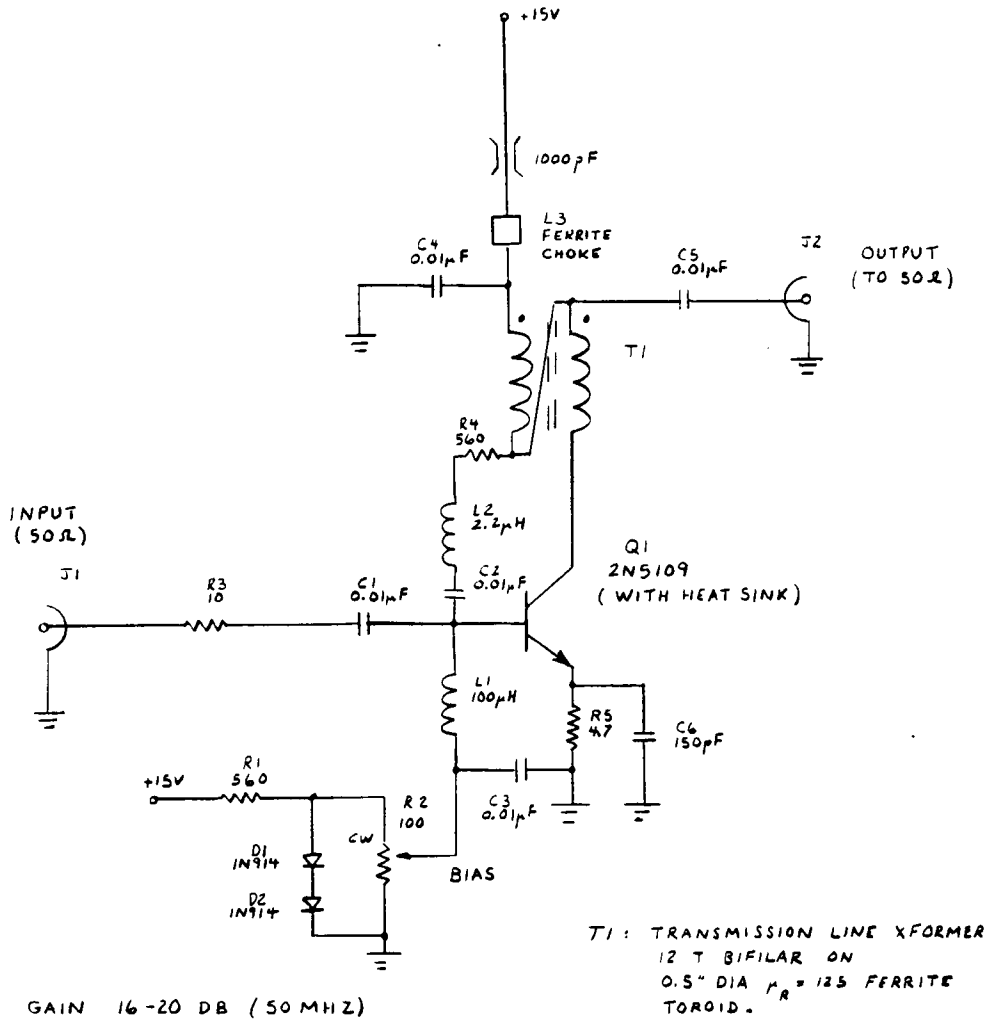

Figure D.4. Schematic Diagram of the Power Amplifier for the Phase Noise Test Set.

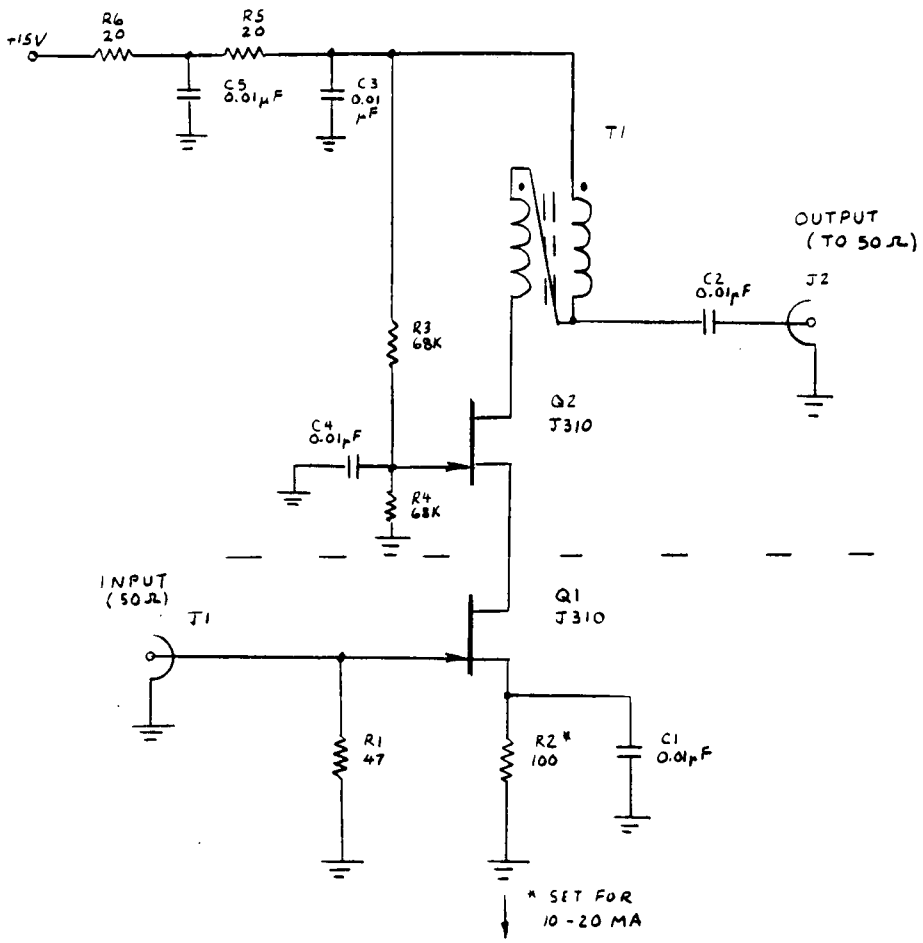

Figure D.5. Schematic Diagram of the Isolation Amplifier for the Phase Noise Test Set.

test set. It is interesting to note that without the isolation amplifier the two oscillators would synchronize with each other if brought close enough together in frequency.

The low noise amplifier has a selectable gain of either 40 dB or 60 dB and a noise floor of approximately 1 $nV/\sqrt{Hz}$. Its bandwidth is approximately 10 Hz to 2 MHz (20 MHz if operated at a gain of 40 dB). It was designed by the author and features a JFET input stage for minimum current noise. No schematic diagram is provided for it in this thesis.

The attenuators are pi-network resistive attenuators designed for 50 ohm source and load impedances. They are used to set signal levels in the test set. The attenuators located adjacent to the doubly balanced mixer (the phase detector) serve an additional function of providing source impedances for the mixer that are close to 50 ohms.

For phase noise measurements below 50 kHz from the carrier, a digitally based FFT analyzer was used. Like most FFT analyzers it supports data display of reference units based on a user-entered reference level. A reference level was used that is equal to the product of the phase detector gain, the low noise amplifier gain, and the square root of two (this compensates for the 3 dB difference between SSB phase noise and phase noise spectral density). The FFT analyzer then reads SSB phase noise directly when used in the noise mode where the spectrum measurements are normalized to a 1 Hz bandwidth.

Phase noise measurements at frequencies above 50 kHz from the carrier were taken using an analog spectrum analyzer. The analyzer

was used in the averaging mode, so no correction for peak detection was required. The measurements were normalized to a 1 Hz bandwidth by correcting for the analyzer noise bandwidth.

A photograph of the phase noise test set is shown in Figure D.6. Note the shielded construction of each stage. In particular, note that the stages are individually constructed for maximum shielding. This also allows the test set to be reconfigured by rearranging the different stages. All signal connections between the stages are made by means of 50 ohm coaxial cable with BNC type connectors.

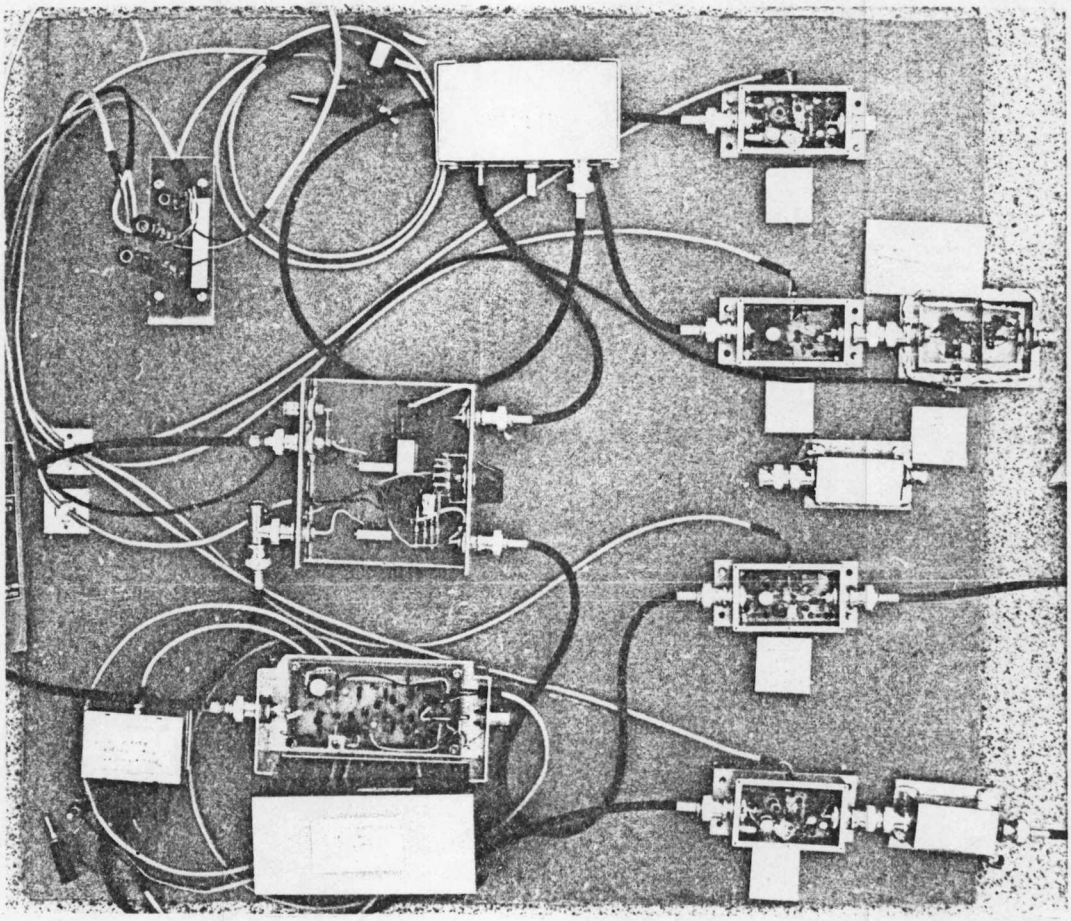

Figure D.6. Photograph of the Phase Noise Test Set.

VITA

David Martin Binkley was born in Knoxville, Tennessee on July 19, 1955. He graduated from Bearden High School in Knoxville and then attended the University of Tennesse in Knoxville, receiving a Bachelor of Science Degree in Electrical Engineering.

He worked at several companies while in the COOP engineering program at the University of Tennessee and obtained experience in the design of RF PLL synthesizers and superheterodyne receivers. Since graduating from the University of Tennessee, he has been employed at Technology for Energy Corporation in Knoxville. There he specializes in analog electronic instrumentation design.

Mr. Binkley is a professional jazz pianist who, at the time of this thesis publication, performs regularly at the Regas Restaurant in Knoxville. His hobbies include amateur radio (call sign WB4TQM), photography, jazz composition and arranging, and running. Most recently, after typing this thesis, he has become a somewhat experienced word processing operator.