New Application for Indium Gallium Zinc Oxide thin film transistors: A fully integrated Active Matrix Electrowetting Microfluidic Platform

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Dedicated to Hyunju Cha, Christina S. Noh, Eric H. Noh,

and my parents and parents in law

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Abstract

The characterization and fabrication of active matrix thin film transistors (TFTs) has been studied for applying an addressable microfluidic electrowetting channel device. Amorphous Indium Gallium Zinc Oxide (a-IGZO) is used for electronic switching device to control the microfluidic device because of its high mobility, transparency, and easy to fabrication. The purpose of this dissertation is to optimize each IGZO TFT process including the optimization of a-IGZO properties to achieve robust device for application. To drive the IGZO TFTs, the channel resistance of IGZO layer and contact resistance between IGZO layer and source/drain (S/D) electrode are discussed in this dissertation. In addition, the generalization of IGZO sputter condition is investigated by calculation of IGZO and Oxygen (O_2) incorporation rate at different oxygen partial pressure and different sputter targets. To develop the robust IGZO TFTs, the different passivation layers deposited by Radio Frequency (RF) magnetron sputter are investigated by comparing the electrical characteristics of TFTs. The effects Plasma Enhanced Chemical Vapor Deposition (PECVD) of Silicon Dioxide (SiO_2) passivation layers on IGZO TFTs is studied the role of hydrogen and oxygen with analyzed and compared the concentration by the Secondary Ion Mass Spectroscopy (SIMS).

In addition, the preliminary electrowetting tests are performed for electrowetting phenomena, the liquid droplet actuation, the comparison between conventional electrowetting and Laplace barrier electrowetting, and the different size electrode effect for high functional properties. The active matrix addressing method are introduced and investigated for driving the electrowetting microfluidic channel device by Pspice simulation. Finally, the high resolution electrowetting

microfluidic device (16x16 matrix) is demonstrated by driving liquid droplet and channel moving using active matrix addressing method and fully integrated IGZO TFTs.

Table of Contents

1 Introduction

1.1 Motivation of this work ……..……...…..……1

1.2 Thin film Transistors (TFT) …..……..……..……2

1.2.1 Historical background ……..……4

1.2.2 Basic TFTs operation ……...…4

1.2.3 TFTs structure ……..……..……..7

1.2.4 Electrical characterization of TFTs …….....10

1.2.4.1 Threshold voltage (V_{th}) and turn on voltage (V_{ON}) ……..…….……10

1.2.4.2 Field effective mobility (μ_{FE}) ……..…….13

1.2.4.3 Subthreshold gate swing slope and current on/off ratio ……14

1.2.5 Metal oxide semiconductor TFTs ……..……..…….....16

1.2.5.1 Overview of transparent electronics and amorphous oxide semiconductors (AOSs) …….……..16

1.2.5.2 Electronic structure and carrier transport model of amorphous oxide semiconductors ……..……..……18

1.3 Electrowetting and microfluidic channel in Lab on a chip device ……..24

1.3.1 Overview of Electrowetting Phenomena …….……..24

1.3.2 Electrowetting on dielectric (EWOD) in a lab on a chip ……...……28

2 Device fabrication and characterization

2.1 Fabrication of IGZO TFTs ……..31

2.1.1 Gate electrode ……...…….33

2.1.2 Gate insulator ….……36

2.1.3 Semiconductor ……...39

2.1.4 Source and drain electrode ……..……..39

2.1.5 Passivation layer ……44

2.1.6 Post annealing for TFTs activation ……..…..44

2.2 Fabrication of the lab on a chip system which is fully integrated on the IGZO TFTs array ……..47

3 Basic characteristics and generalization of IGZO layer

3.1 Channel resistance and contact resistance ……...49

3.1.1 Introduction ……...49

3.1.2 Experiments ……...……49

3.1.3 Results and discussion ……...51

3.1.4 Conclusion ……...……..60

3.2 Generalization the rf sputter condition of IGZO layer ……61

3.2.1 Introduction ……...61

3.2.2 Experiments ……...63

3.2.3 Results and discussion …….……..63

3.2.4 Conclusion ……72

4 Characterization of Passivation layer

4.1 Introduction ……73

4.2 Characterization of IGZO TFTs with different passivation layer ……...…77

4.3 Characterization of PECVD SiO_2 passivation layer ……...…84

4.4 Conclusion ……..……..99

5 Preliminary Electrowetting Basic Test

5.1 Introduction ……..……...…100

5.2 Electrowetting phenomena experiment ……100

5.3 Droplet actuation in simple electrode structure ……..……..109

5.4 Conventional electrowetting microchannel & Laplace barriers electrowetting ……....113

5.5 Split the different size electrodes ……..120

5.6 Conclusion ……125

6 Active matrix driving for electrofluidic device using IGZO TFTs

6.1 Introduction ……...……126

6.2 Experiments ……...……127

6.3 Results and Discussions ……..……..126

6.4 Conclusion ……131

7 Full integration TFTs and Electrowetting device

7.1 Introduction ……...……145

7.2 Experiments ……...……147

7.3 Results and discussions ……154

7.4 Conclusion ……167

8 Conclusions ……168

*** List of References** ……170

*** Appendix A:** Run sheet for IGZO TFTs processing ……185

*** Appendix B:** Run sheet for Full integrated electrowetting device using IGZO TFTs ……188

***Vita**……194

LIST OF TABLES

Table 1-1. Comparison of characteristics which has different kinds of semiconductor layers in thin film transistor …….…….3

Table 2-1. Resistivity of different metals at 20-25℃, and temperature coefficient resistance …35

Table 2-2. Work function of different metals ……...…43

Table 3-1. Summary of electrical characteristics of a-IGZO TFT with different TFT size (W/L) at V_{DS}= 10.1V ……...56

Table 3-2. The sputter parameters of IGZO deposition with same oxygen and IGZO flux ….…67

Table 3-3. TFT characteristics of the same Φ_{O_2} and Φ_{IGZO} which have different oxygen partial pressure and deposition rate …….68

Table 3-4. TFT characteristics of the same Φ_{O_2} and Φ_{IGZO} with different sputter targets ….....71

Table 4-1. The sputter deposition conditions of different passivation layer Al_2O_3, SiO_2, Hf_2O_3, and Y_2O_3 ……..…….81

Table 4-2. TFT characteristics of different passivation layers, Al_2O_3, SiO_2, Hf_2O_3, and Y_2O_3 ...83

Table 4-3. Summarization refractive indexes (n) collected at 600nm wavelength and film densities of passivation PECVD SiO_2 layer of a-IGZO TFTs. ……...……..…93

Table 7-1. Transfer characteristics of TEG 8TFTs and Main array 6TFTs ……..……..163

LIST OF FIGURES

Figure 1-1. (a) The basic structure of TFT and corresponding energy bond diagrams as viewed through the gate for several biasing conditions: (b) equilibrium, V_{GS}=0 [V], (c) V_{GS} <0 [V], and (d) V_{GS} > 0 [V] 6

Figure 1-2. Cross section of the various TFT structure as S/D electrodes: (a) normal staggered TFT structure (b) inverted staggered TFT structure ……...……8

Figure 1-3. Cross section of the various TFT structure as gate electrodes: (a) Bottom gate TFT structure (b) Top gate TFT structure ……..……9

Figure 1-4. Schematic diagram for definition of V_{th}, V_{ON}: (a) Output conductance gate to source voltage ($g_D - V_{GS}$) characteristic illustration threshold voltage estimation (b) Log (I_D-V_{GS}) transfer characteristics showing the turn on voltage, V_{ON}, and the threshold voltage, V_{th} for the same device ……...12

Figure 1-5. Schematic diagrams for definition of subthreshold slope and drain current ratio $\mathbf{I_D^{ON-OFF}}$ ……...15

Figure 1-6. Besides transparency. Amorphous AOS TFTs have additional useful characteristics to compete with existing technologies ……17

Figure 1-7. Schematic electronic structures of silicon and ionic oxide semiconductors. (a–c) Bandgap formation mechanisms in (a) covalent and (b, c) ionic semiconductors. Closed and open circles denote occupied and unoccupied states, respectively. ……..20

Figure 1-8. Schematic orbital drawings for the carrier transport paths in crystalline and amorphous semiconductors. (a) Covalent semiconductors with sp^3 orbitals (b) metal oxide semiconductors with s-orbital overlap of metal cation …….……..21

Figure 1-9. Carrier transport in a-IGZO (a) Relationship between Hall mobility and carrier density for c-IGZO and a-IGZO (b) Illustration of percolation conduction model showing examples of (i) a shorter path and (ii) a longer winding path ……...….22

Figure 1-10. Subgap density of states in a-IGZO obtained by the C–V method. Data for a-Si:H are shown for comparison. ……...23

Figure 1-11. Different degrees of wetting: On the left there is high wetting and the contact angle is small. On the right side little wetting and there is a high contact angle. …….…..26

Figure 1-12. Liquid droplet on an insulated surface with and without applied voltage: Applying the voltage creates the wetting on the surface. …….27

Figure 1-13. Schematic diagram of a typical lab on a chip device: EWOD consist of metal electrode, insulator layer (dielectric), and hydrophobic layer on top and bottom plates. Pigment droplet which is filled with oil lay on between top and bottom electrodes. ..29

Figure 1-14. Envisioned digital microfluidic circuit and the four fundamental droplet operations necessary ……..30

Figure 2-1. The schematic structure of IGZO TFTs (a) Schematic structure of IGZO TFTs with process sequence (b) Layout design of IGZO TFTs (c) Process flow chart of IGZO TFTs …….32

Figure 2-2. SEM images of TFTs represent the step coverage of gate insulator on Cr gate electrode ……...35

Figure 2-3. I-V characteristics, J-V characteristics, J-E characteristics, and capacitance of different gate insulator layers (Al_2O_3, SiO_2, SiN_x, TiO_2, and ATO) ……37

Figure 2-4. Transfer hysteresis curves of different gate dielectric layers ……38

Figure 2-5. Schematic diagram the S/D contact resistance between S/D and IGZO layer, and channel resistance of IGZO layer ……41

Figure 2.6 Band diagram the match-up between S/D metal and semiconductor layer (a) metal and n-type semiconductor before contact (b) metal and n-type semiconductor after contact (c) metal and n-type semiconductor contact with reverse bias (d) metal and n-type semiconductor with forward bias ……42

Figure 2-7. Micro oven temp history during the post annealing in air atmosphere …….….45

Figure 2-8. SEM images of IGZO TFTs, (a) Overview of IGZO TFT, (b) Channel area, and (c) Cross sectional SEM images of IGZO TFTs ……....46

Figure 2-9. The whole layout of electrowetting device, (a) 5×2 electrodes device, (b) Electrode shape, and (c) Cross section view ……48

Figure 3-1. Schematic diagram for TLM pattern and TFT structure: (a) Transmission line method (TLM) Pattern, (b) Structure of IGZO TFTs ……..……..50

Figure 3-2. The schematic drawing the physical origin of the resistance components ……54

Figure 3-3. The transfer curve characteristics as different length TLM pattern TFTs, all TFTs have 200um width. (a) Log(I_{DS}) - V_{GS} (b) $(I_{DS})^{1/2}$ - V_{GS} ……..……..55

Figure 3-4. The total TFT ON resistance (R_T) versus channel length (L) for several levels of V_{GS} ……...……57

Figure 3-5. The Contact resistance (R_S + R_D) and the channel resistance (R_{ch}× L) as a function of V_{GS} …….....58

Figure 3-6. Extracting the intrinsic field-effect mobility and threshold voltage by plotting $1/r_{ch}$ versus V_{GS} ……...……59

Figure 3-7. Molecules incorporation of IGZO and O_2 with oxygen partial pressure in growing IGZO film during sputtering ……62

Figure 3-8. Deposition rate of IGZO layer with different oxygen partial pressure and different rf power ……66

Figure 3-9. The power conditions corresponded the deposition rate which has the same oxygen and IGZO flux ……..67

Figure 3.10. The transfer curves of the same Φ_{O_2} and Φ_{IGZO} which have different oxygen partial pressure and deposition rate: (a) pO_2 = 20%, (b) pO_2 = 30%, (c) pO_2 = 40%, and (d) merge the transfer curves of three TFTs at V_{DS}=10.1[V] ……...….69

Figure 3-11. The transfer and output curves of the same Φ_{O_2} and Φ_{IGZO} of different sputter targets (a) Sputter target A (b) Sputter target B ……..…….70

Figure 4-1. (a) Schematic showing the electric field induced adsorption of oxygen molecules from the ambient atmosphere (b) Schematic showing the electric field induced desorption of water molecules into the ambient atmosphere ……..……..75

Figure 4-2. (a) Schematic showing the electric field induced desorption of water molecules into the ambient atmosphere (b) Transfer curve change before passivation layer and after passivation layer …….……..76

Figure 4-3. (a) Schematic structure of different passivation layer samples (b) Transfer curves of IGZO TFTs before passivation layer ……79

Figure 4-4. Hysteresis curves with oxygen gas flow with 4 kinds of metal sputter targets for the rf reaction sputtering ……...…….80

Figure 4-5. Transfer curves with different passivation layers, Al_2O_3, SiO_2, Hf_2O_3, and Y_2O_3 82

Figure 4-6. (a) Transfer characteristics of a-IGZO TFTs without passivation layer. [annealed at 350℃ N_2 1hr, TFT W/L=50/20 um, V_{DS} = 0.1, 5.1, 10.1 V], (b) Bottom gate structure of un-passivated TFTs ……..87

Figure 4-7. (a) Transfer characteristics of a-IGZO TFTs with different temperature PECVD SiO_2 passivation layers after N_2 350℃ 1hr. (b) Transfer characteristics of a-IGZO TFTs with different temperature PECVD SiO_2 passivation layers after air 350℃ 1hr. [TFT size W/L=50/20um, V_{DS}=10.1V ……..…….89

Figure 4-8. Schematic summary of the interaction mechanism between PECVD passivation layer and IGZO active layer before and after annealing step in the IGZO TFTs. Solid arrows represent as-dep passivation, dash- arrows represent after post annealing. …….92

Figure 4-9. TOF-SIMS depth profiles of different SiO_2 films deposited by PECVD (a) as-deposited samples at PECVD 150C and 350C, (b) hydrogen concentration of different SiO_2 films in different annealing atmosphere (c) oxygen intensity of different SiO_2 film in different annealing atmosphere ……...…….96

Figure 4-10. Compare the concentration of hydrogen and oxygen with initial and after passivation or post annealing (a) hydrogen concentration, (b) oxygen intensity, (c) total carrier change ratio ($\Delta n_{tc,\ total\ carrier\ change}$), and (d) compare total carrier change and I_{DS} [A] at V_{GS} = 0V in different passivation and post annealing samples .98

Figure 5-1. Three interfacial surface tension (a) with un-biased, (b) with biased ……..…103

Figure 5-2. The schematic basic electrowetting test system (a) Direct connect with Power supply, (b) MOSFET (IRF840), (c) In_2O_3 TFT ……..104

Figure 5-3. (a) The circuit diagram of electrowetting device, (b)-(c) The RC delay at 200MΩ and 2kΩ of electrowetting device in Pspice simulation ……...….105

Figure 5-4. The experiment set up for electrowetting test using In_2O_3 TFT ……..107

Figure 5-5. The In_2O_3 TFT characteristics and the electrowetting phenomena test 1) TFT-off state (V_g = -12V) with V_d = 0V, 2) TFT-off state (V_g=-12V) with V_d=40V and 3) TFT-On state (V_g=0V) with V_d=40V ……108

Figure 5-6. Schematic cross-section of electrowetting droplet actuation (a) zero bias, (b) voltage applied ……111

Figure 5-7. 5X1 electrodes with Parylene-C/Fluoropel coating sample from University of Cincinnati. The droplet actuation voltage is 90~110V. ……..……112

Figure 5-8. (a) Schematic cross section of Laplace barrier electrowetting device (b) SEM image of vertical Laplace barrier on top plate (c) Conventional Electrowetting not to maintain the shape without applied bias (d) Laplace barrier electrowetting holding the shape without applied bias (e) Illustration of arrayed Laplace barrier ……114

Figure 5-9. Mask layout of 2×5 electrowetting device, and sample picture ……..116

Figure 5-10. The actuation of droplet without post (conventional electrowetting) and with post (Laplace barrier electrowetting) ……116

Figure 5-11. The moving time of droplet with applied voltage and the moving speed of droplet with applied voltage (a) Conventional electrowetting (without post), (b) Laplace barrier electrowetting (with post) ……...…118

Figure 5-12. The moving time and speed between 2nd electrode to 3rd electrode, relation of threshold voltage with post and without post samples ……...119

Figure 5-13. Droplet configuration for splitting. (a) Top view, (b) Cross-sectional view B-B'. (c) Cross-sectional view A-A'. (d) The relation splitting factors with menisci, contact angle, gap height in splitting ……..122

Figure 5-14. Mask layout design of different electrode size (1mm, 500um, 250um, 100um) ...123

Figure 5-15. Different size two droplets motion and the process of splitting in different size electrodes ……124

Figure 6-1. (a) Picture of 5 x 5 IGZO TFTs array. (b) Cross-sectional view of IGZO TFT. (c) Schematic diagram of TFTs array driving system. (d) Illustration of interconnection between TFTs array and electrofluidic device. (e) Cross-sectional view of electrofluidic device. …….130

Figure 6-2. (a) Individual TFTs transfer characteristics. TFT output voltage V_E as a function of (b) V_G and (c) V_S. ……..132

Figure 6-3. (a) Electrowetting transfer velocity as a function of V_S. (b) Square root of the electrowetting transfer velocity plot as a function of V_E. ……..…134

Figure 6-4. Simultaneous and individual control of two droplets by active matrix addressing method using IGZO TFT array ……..136

Figure 6-5. Electrofluidic functionalities using AM driven electrofluidic device for Lab-on-chip application. Continuous channel formation (a) on one row and (b) across rows (c) One droplet control on the adjacent row when continuous channel was formed on one row. ……..…138

Figure 6-6. (a) Schematic diagrams of wave form measurement. Gate, source, and electrowetting voltage waveforms as a function of external storage capacitor with gate pulse width of 100 msec; (b) only electrofluidic device, (c) electrofluidic device + 10 nF external storage capacitor, and (d) electrofluidic device + 100 nF external storage capacitor.

Voltage waveforms for the electrofluidic device + 10 nF external storage capacitor with gate pulse frequency of (e) 10 Hz and (f) 120 Hz (50% duty ratio). ……142

Figure 7-1. Prospective schematic diagram of electrofluidic device integrated on the TFTs array. ……...……..146

Figure 7-2. Mask designs, the cross section structure, and sample picture of 5x5 full integrated TFTs electrowetting device ……....148

Figure 7-3. Mask design and sample picture of high resolution 16x16 full integrated TFTs electrowetting device ……..149

Figure 7-4. Process flows of full integration TFTs electrowetting device ……152

Figure 7-5. Sample preparation and assembly full integration device ……....153

Figure 7-6. The degradation of TFT characteristics after electrowetting dielectric PECVD 350℃ SiO_2 process ……...…156

Figure 7-7. The transfer curves of 5×5 full integrated TFTs electrowetting device during the each process step: 1) after electrowetting electrode, 2) after electrowetting dielectric deposition, 3) after the final post annealing, and 4) before electrowetting test (hydrophobic layer coating and curing) ……157

Figure 7-8. Fabrication issues of full integration TFTs electrowetting device ……..159

Figure 7-9. TFT characteristics change of finally optimized the fabrication process ……...….160

Figure 7-10. Transfer curves of different position in 16×16 high resolution electrowetting device ……162

Figure 7-11. Driving the 5×5 full integration TFTs electrowetting device (a) Final sample picture, (b) Final TFT characteristics, and (c) Driving the droplet actuation ……..165

Figure 7-12. Driving the 16×16 full integration TFTs electrowetting device (a) individual droplet moving, (b) Horizontal channel moving ……...……..166

Chapter 1

Introduction

1.1 Motivation of this work

A lab on a chip (LOC) is a device that integrates one or several laboratory functions on a single chip of only millimeters to a few square centimeters in size. To control the small amount liquid in LOC devices many researchers have studied the electrowetting (EW) and electrowetting-on-dielectric (EWOD) principles applied to microfluidic devices [1]. Over the past decade there has been growing the interest in the development of experimental ways for controlling small amounts of liquid, reducing the driving voltage, realizing multi-functional liquid movement, and achieving high resolution LOC devices for bio-applications [1-6]. LOCs may provide many advantages to standard alternative procedures. There is low fluid volume consumption of liquid, faster response of the system, multi-functional droplets using small amount volume, and low fabrication cost. Although they have many advantages for LOC device, they have limitations of high resolution device for driving multi-functional droplet moving and real LOC device because of the number of control lines from high numbers of electrodes. To solve this limitation, we will apply to active matrix driving which has widely has been used in the flat panel display industry and integrated Indium Gallium Zinc Oxide TFTs (Thin Film Transistors) for high resolution LOC device. In this dissertation, we have focused on the optimization of thin film materials processing methods and electrical characterization of IGZO TFTs, the method of applying the active matrix driving for high resolution electrowetting LOC device, and demonstration of high resolution multi-functional microfluidic and electro wetting LOC device with fully integrated IGZO TFTs.

1.2 Thin Film Transistor (TFT)

Thin film transistors (TFTs) are a special kind of field effect transistor made by depositing thin films of a semiconductor active layer as well as dielectric layer and metallic contacts over a supporting substrate. TFTs have been used as electronic switching elements to control electronic devices such as displays, semiconductors, flash memories, and so on. Currently, many researchers have studied many kinds of semiconducting layers for thin film transistor such as Si-based TFTs [7-11], metal oxide semiconductors [12-14], organic materials [15-17], and polymers [18-20]. Table 1-1 shows the comparison of TFTs characteristic made by different kinds of semiconductor layers. Conventionally, the main applications for TFTs has been flat panel display such as liquid crystal displays (LCDs) and active matrix organic light emitting displays (AMOLEDs) which are used in amorphous Si (a-Si) semiconductor layer or poly silicon (poly-Si) semiconductor layers. Recently, in commercial flat panel display industry, many demands about large size, high resolution, and low power consumption for displays necessitate new semiconductor layers instead of a-Si and poly-Si. The a-Si semiconductor layers have low field effective mobility (below than 1 ㎠/Vs) and poly-Si also has a difficulty for large sized fabrication for their high temperature process and laser crystallization process. Therefore, they have a solution for metal oxide semiconductor layer instead of a-Si and poly-Si, because of their high field mobility, transparency, good uniformity, and easy fabrication at room temperature. In this dissertation we focus on the metal oxide semiconductor using a-IGZO semiconductor layer to control our electrowetting based microfluidic device.

Table 2-1. Comparison of characteristics which has different kinds of semiconductor layers in thin film transistor

	Metal Oxide (a-IGZO)	a-Si	poly-Si	Polymer Organic
Field Effect Mobility (㎠/Vs)	10~50	0.5~1	30~300	Up to 0.1
Process Temperature (℃)	<350℃	~350℃	>450℃	<150℃
Transparency (%)	>80	<20	<20	>80
Uniformity	Good	Good	Fair	Medium
Reliability	Low → High	Low	Medium/High	Low
Fabrication Difficulty	Easy	Easy	Difficult	Easy
(# of Mask layer)	5	5	(7~10)	(4~5)

1.2.1 Historical background of TFTs

Thin film transistors (TFTs) have been used as a capacitor and electronic computer in the past 60 years. The basic operation concept is similar those of the metal oxide semiconductor field-effect transistors (MOSFETs). The first operation concept of TFTs was suggested by Lilienfeld [21], Brody [22], and Heil [23].They introduced the MOSFET and established the concept of 3-terminal operation (gate, source and drain) using field driven by a capacitor. After that, the thin film transistor was demonstrated by P. K Weimer (1962) who used a top gate staggered structure with a microcrystalline cadmium sulfide (CdS) active layer [24]. Since Weimer's work, TFTs based on a wide variety of semiconductor materials including organic and polymer, and amorphous and polycrystalline materials have been developed. Nowadays, the most dominant TFT technology is based on hydrogenated amorphous silicon (a-Si:H) which was proposed by LeComber as an electronic switching device in 1979 [11]. Using amorphous silicon, lower leakage current can be achieved to apply the low current applications such as liquid crystal flat panel displays [10,25], and solar cell panels [26,27]. In addition, poly-Si based TFTs based on many kinds of crystallization methods to increase field effect mobility and improve stability of TFT characteristic such as solid phase crystallization (SPC), metal induced crystallization (MIC), and sequential lateral crystallization (SLS), and so on [7-9,28,29]. More recently, for large size, transparent and flexible flat panel display applications, metal oxide semiconductors were introduced by Hosono's group in 1994 [13].

1.2.2 Basic TFT operation

Figure 1-1 shows the basic structure of n-type semiconductor TFT and energy band diagrams with the gate bias [30]. In Figure 1-1(b), the device is in equilibrium state with 0V gate bias.

Figure 1-1(c) shows an energy band diagram with the negative bias on the gate. This applied negative bias repels the mobile electrons from channel region at the interface between semiconductor and dielectric layer. The absence of mobile electrons in channel region creates a depletion layer in the semiconductor layer. The depletion layer reduces the conductance of the semiconductor layer, and inhibits current between the source and drain. In Figure 1-1(d), when a positive voltage is applied at the gate electrode, the mobile electrons are attracted in the channel region, and results in the "accumulation mode" in the TFT device. The channel layer accumulates mobile electrons and has low resistance and high conductivity. Devices with positive gate bias results in a high current path between the source and drain electrodes. This describes the simple operation of TFT devices which are referred to as the on-state and off-state of the electronic switching device.

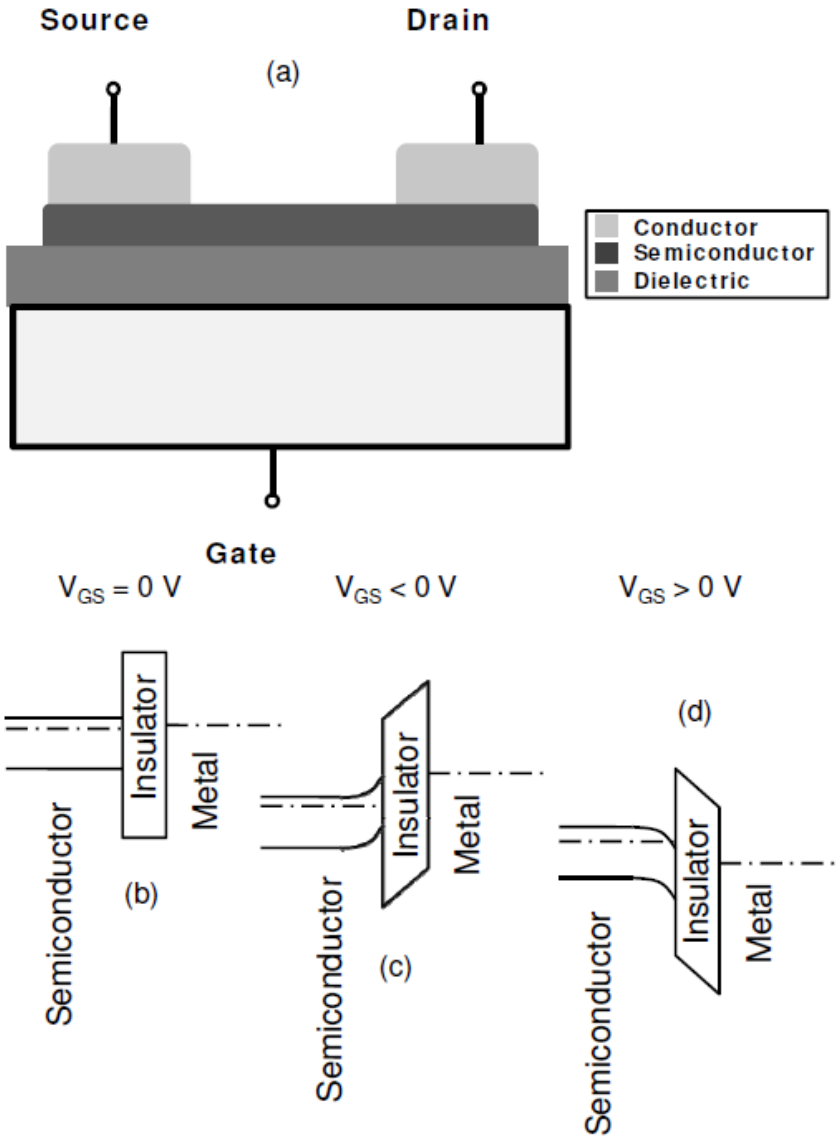


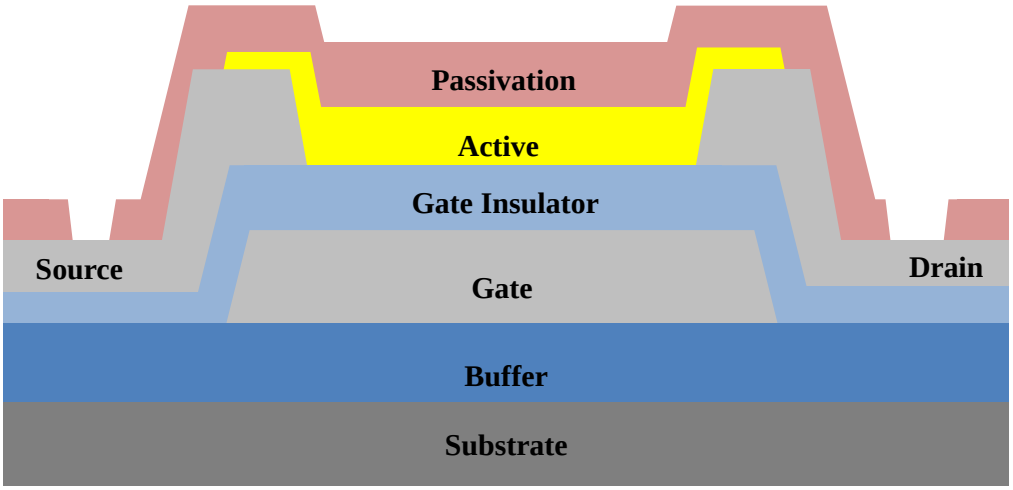
Figure 1-7. (a) The basic structure of TFT and corresponding energy bond diagrams as viewed through the gate for several biasing conditions: (b) equilibrium, V_{GS}=0 [V], (c) V_{GS} <0 [V], and (d) V_{GS} > 0 [V]

C. R. Kagan et al. "Thin-film transistors"[30]

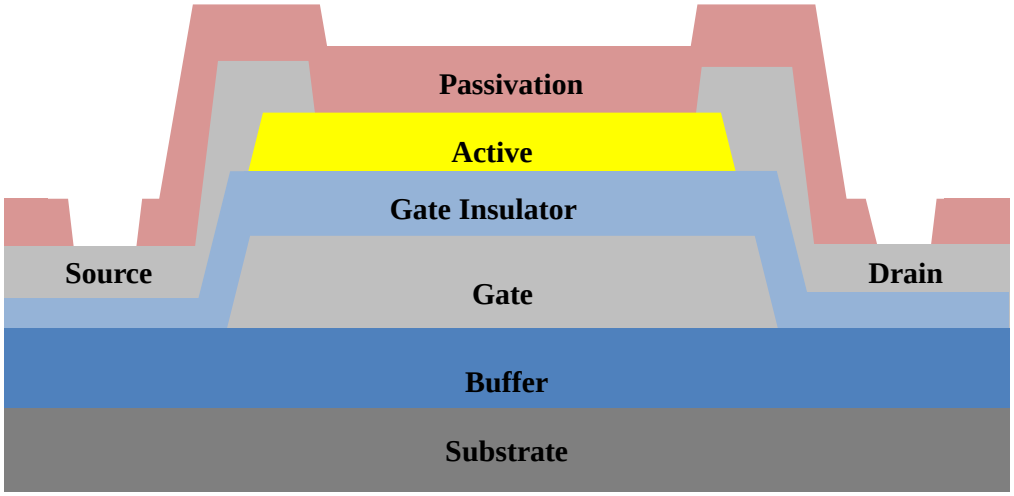
1.2.3 TFT structure

There are two types of classification method for TFT structures. One is inverted or normal staggered structure of TFTs which is classified by formation of source drain electrodes (S/D). The other is top gate and bottom gate structure which changes the sequence of formation of gate electrodes. Figure 1-2 and 1-3 represent the structure of TFTs depends on S/D and gate electrodes. In Figure 1-2(a), this structure is normal staggered structure of TFTs which is proposed earlier than the inverted structure as shown Figure 1-2(b). This structure has difficulty in making ohmic contact layers between the semiconductor layer and S/D electrodes (normally in case of a-Si, n^+ a-Si layer is used for the ohmic contact). Furthermore, degradation of the electrical characteristics of TFTs can occur due to exposure to atmosphere and etch damage on interface between gate dielectric and a-Si layer during S/D patterning process. To enhance the TFT characteristics, this inverted TFT structure is widely used in a-Si and metal oxide semiconductor TFTs. This structure has advantage in formation n^+ a-Si layer for ohmic contact and inhibition from degradation of TFT characteristics during S/D formation. However this structure is very sensitive to back channel effects and damage of semiconductor layer. Figure 1-3 shows the bottom gate structure and top gate structure depending on the gate location. In Figure 1-3(a), bottom gate structure is normally used in a-Si based TFTs and metal oxide semiconductors. As already mentioned, this structure has advantage of ohmic contact and minimal degradation of TFT characteristics. However, in case of poly-Si based TFTs the bottom gate structure has limitation of gate electrode material due to high temperature process (~600℃) for crystallization of a-Si. Therefore poly-Si based TFTs normally use the top gate structure as shown Figure 1-3(b). Recently, many researchers have studied and changed the basic TFT's

structure to enhance the electric characteristics of TFT and improve its stability and reliability of biased stress, temperature stress, and time dependence.

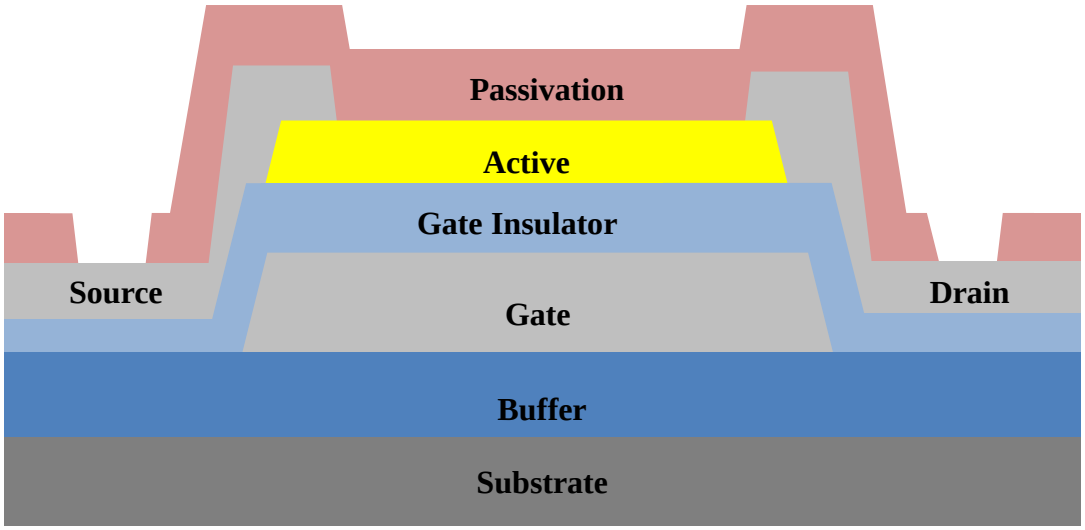


(a) Normal staggered TFT structure

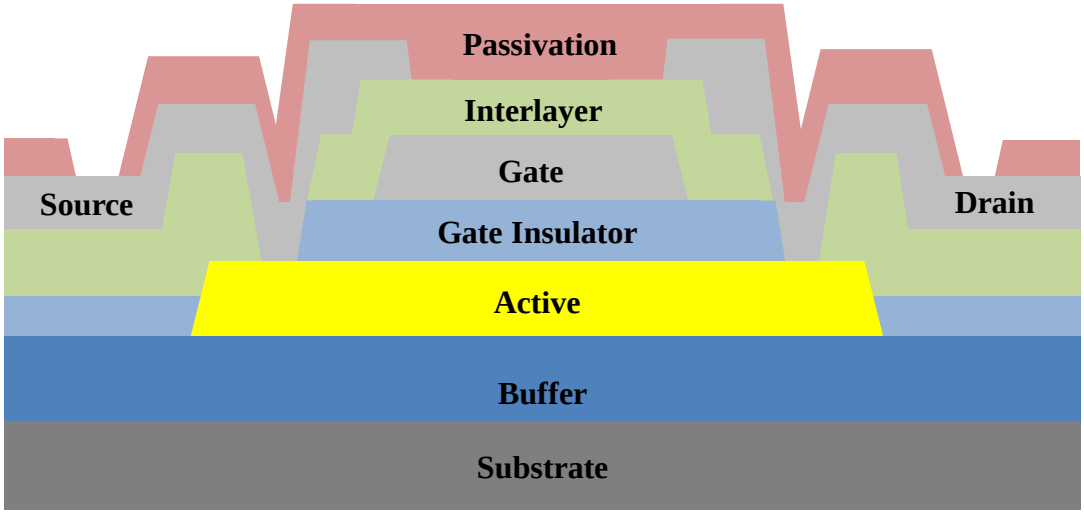


(b) Inverted staggered TFT structure

Figure 1-8. Cross section of the various TFT structure as S/D electrodes: (a) normal staggered TFT structure (b) inverted staggered TFT structure



(a) Bottom gate TFT structure



(b) Top gate TFT structure

Figure 1-9. Cross section of the various TFT structure as gate electrodes: (a) Bottom gate TFT structure (b) Top gate TFT structure

1.2.4 Electrical characterization method of TFT

This section discusses several important TFT figures-of-merit, threshold voltage (V_{th}), field effective channel mobility (μ_{FE}), subthreshold gate swing (S.S), and on/off current ratio ($(I_D^{ON-OFF}$).

1.2.4.1 Threshold voltage (V_{th}) and turn on voltage (V_{ON})

Threshold voltage, V_{th}, is an important TFT parameter indicative of the onset of drain current [31,32]. However, it is not possible to uniquely define V_{th}, which sometimes leads to ambiguous or misleading conclusion. Therefore, an alternative figure of merit for the onset of drain current, the turn on voltage (V_{ON}), is introduced at the end of this section. V_{th} can be estimated graphically by plotting the TFT output conductance, g_D, as a function of the gate-source voltage, V_{GS}. The drain current (I_d) is given by

$$I_D = \mu C_I \frac{W}{L} \left[V_{DS} \left(V_{GS} - V_{th} \right) - \frac{V_{DS}^2}{2} \right], \tag{1.1}$$

where W is the width of the TFT, L is the length between source and drain, μ is the mobility in the semiconductor layer, C_I is the capacitance density of the gate insulator, V_{DS} is the drain-source voltage, and V_{GS} is the gate-source voltage. Estimating g_D as the derivative of I_D with respect to V_{DS} leads to

$$g_D = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS}=constant} = \mu C_I \frac{W}{L} (V_{GS} - V_{th} - V_{DS}). \tag{1.2}$$

Figure 1-4(a) shows the schematic diagram for definition of V_{th}. G_D-V_{GS} plot should be an extrapolation of the linear portion of this curve to the V_{GS} axis is equal to V_{th} + V_{DS}. An alternative procedure for assessing the initiation of current flow in a TFT is to employ a

log I_D $-V_{GS}$ curve and to define a turn on voltage, V_{ON}, as the voltage which I_D begins to increase with V_{GS}. Figure 1-4(b) shows a log I_D $-V_{GS}$ plot which represents the difference between V_{th} and V_{ON}. The other way to extract V_{th} in the transfer curve of TFTs will be extracted by extrapolating in the saturation region on the $I_{DS}^{1/2} - V_{GS}$ characteristic plot as shown in Figure 1-4(a). In this dissertation we will use the second method to extract the V_{th} using $I_{DS}^{1/2} - V_{GS}$ graph.

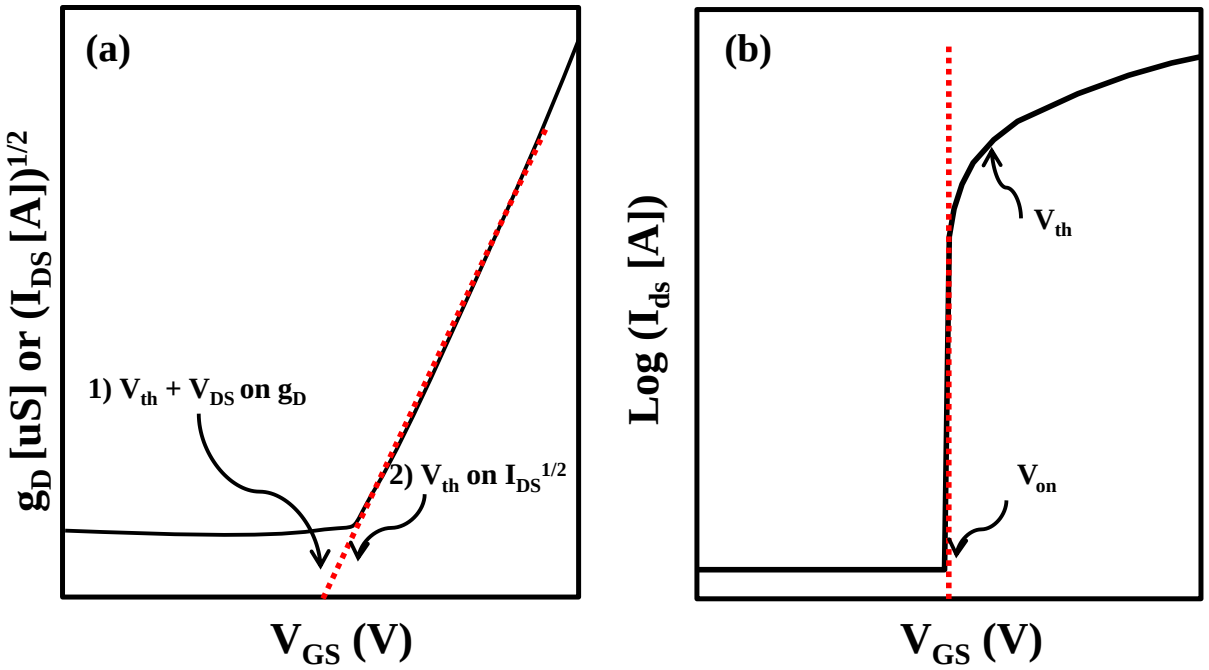


Figure 1-10. Schematic diagram for definition of V_{th}, V_{ON}: (a) Output conductance gate to source voltage (g_D – V_{GS}) characteristic illustration threshold voltage estimation or extract V_{th} from $I_{DS}^{1/2}$ graph, (b) Log(I_D-V_{GS}) transfer characteristics showing the turn on voltage, V_{ON}, and the threshold voltage, V_{th} for the same device

1.2.4.2 Field effective mobility (μ_{FE})

There are three methods to extract the field effect mobility of semiconductor layers[31,33]. The mobility is a measure of the mobile carrier transport in the semiconductor related to the current drive of the TFT. Average mobility (μ_{AVG}) is an estimate of the mobility of all carriers induced into the semiconductor by an applied gate bias, V_{GS}. Average mobility is calculated using

$$\mu_{AVG}\ V_{GS} = \frac{LG_D^{LIN}(V_{GS})}{WC_l(V_{GS}-V_{ON})}, \tag{1.3}$$

where W and L are the width and length of the TFT, C_l is the gate insulator capacitance, and G_D^{LIN} is the output conductance as a function of applied gate bias calculated in the linear region. The output conductance is evaluated at small values of V_{DS} and is calculated as

$$G_D^{LIN}\ V_{GS} = \frac{I_D\ V_{GS}}{V_{DS}}_{V_{DS}\to 0}, \tag{1.4}$$

Incremental mobility is the mobility of charges incrementally added to the semiconductor by a corresponding incremental change in V_{GS}. Incremental mobility is calculated as

$$\mu_{INC}\ V_{GS} = \frac{LG_D^{LIN'}\ V_{GS}}{WC_l}_{V_{DS}\to 0}, \tag{1.5}$$

where $G_D^{LIN'}\ V_{GS}$ is the change in output conductance due to a corresponding change to V_{GS}.

$$G_D^{LIN'}\ V_{GS} = \frac{\partial G_D^{LIN}}{\partial V_{GS}}_{V_{DS}\to 0}, \tag{1.6}$$

A third mobility, saturation mobility, is extracted from a $I_D - V_{GS}$ plot, measured with the device held in saturation. Saturation mobility is calculated as

$$\mu_{SAT} = \frac{2Lm^2}{WC_i}_{V_{DS} \gg V_{GS}-V_{ON}}, \quad (1.7)$$

where m is the slope of a plot of $\overline{I_{D,SAT}}$ of $I_D - V_{GS}$ plot. This slope is calculated as

$$m = \frac{\partial \overline{I_{D,SAT}}}{\partial V_{GS}}, \quad (1.8)$$

In this study, we will extract the field effect mobility from the saturation region because this region is relatively insensitive to the magnitude of the source-drain resistance (contact resistance), and independent of V_{DS}, unlike linear region.

1.2.4.3 Subthreshold gate swing slope and current on/off ratio

The subthreshold swing (S.S) and the current on/off ration are estimated using a log plot of the transfer characteristics taken at high V_{DS} (i.e. $V_{DS} > V_{DSAT} = V_{GS} - V_{ON}$) as shown Figure 1-5. S.S is the maximum slope in the transfer curve,

$$S.S = \left(\frac{\partial \log_{10} I_D}{\partial V_{GS}}\right)^{1}_{max}, \quad (1.9)$$

S.S is very useful values of how efficiency the device turns on and is typically less than 1V/decade. Current on/off ratio (I_D^{ON-OFF}) is a parameter for switching application and device performance. Current on/off ration is calculated as

$$I_D^{ON-OFF} = \frac{I_D^{ON}}{I_D^{OFF}}, \quad (1.10)$$

The value of I_D^{ON-OFF} is usually ~$10^{8\sim9}$.

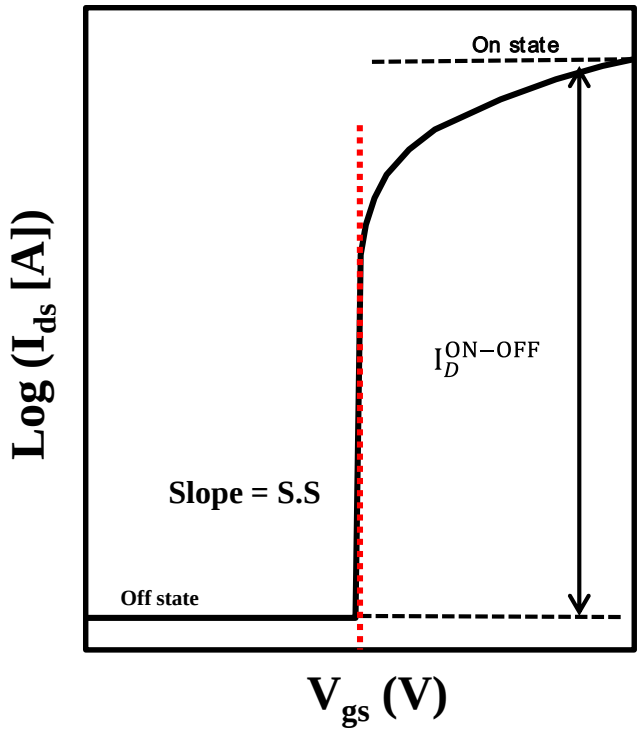


Figure 1-11. Schematic diagrams for definition of subthreshold slope and drain current ratio $\mathbf{I_D^{ON-OFF}}$.

1.2.5 Metal oxide semiconductor based TFTs

1.2.5.1 Overview of transparent electronics and amorphous oxide semiconductors (AOSs)

The phenomenon of a material being optically transparent and electrically conductive was first observed in 1907 with a cadmium oxide film [34]. However, it was not until the 1940s that transparent conducting oxides (TCOs), specifically tin oxide (SnO_2), found widespread use as electric defrosters for airplane windscreens. After that, the birth of transparent electronics using $CuAlO_2$ can be dated to the first port of a highly conductive p-type TCOs [35]. TCOs have been used for their optical properties as infrared reflecting coatings in a variety of markets including energy conserving low emissivity widows, glasses, and oven windows [36,37]. Using both its optical and electrical properties, TCOs have been an enabling technology for flat panel liquid crystal displays, touch panel displays, and the front electrodes of solar cells [36-38]. In 2003, transparent electronics development took off with the contemporaneous report of a ZnO TFT or TTFT by three groups [33,39,40]. Transparent oxide semiconductors that are attracting the most interest can be broadly divided two categories; polycrystalline oxide semiconductor (POS) such as ZnO, and amorphous oxide semiconductors (AOS) including InZnO, InSnO, ZnSnO, InZnSnO, and InGaZnO (a-IGZO) [41-44]. There materials have large Bandgap and wide controllability of carrier concentration, which can make them useful for transparent thin film transistor (TFTs) applications. In the case of POS TFTs, they have high field effect mobilities comparable to low temperature poly-silicon (LTPS) TFTs, but the polycrystalline structure have limitations for uniformity which affects the grain boundaries that can deteriorate the reproducibility. On the other hand, AOS TFTs have good uniformity and reasonably high field effect mobilities ($\sim 10 \mathrm{cm}^2/Vs$) even though deposited at room temperature because of their

amorphous structure. From the advantages of AOS TFTs there are lots of new applications such as transparent displays using large band gap materials, flexible display using plastic or stainless substrate, large sized high resolution display in flat panel display industry. Recently, Samsung and LG electronics demonstrated a 55" FHD AMOLED display in 2013 CES conference, flexible displays, and transparent displays using amorphous Indium Gallium Zinc Oxide (IGZO) TFTs. Figure 1-6 summarized the advantages and possible application of using AOS TFTs.

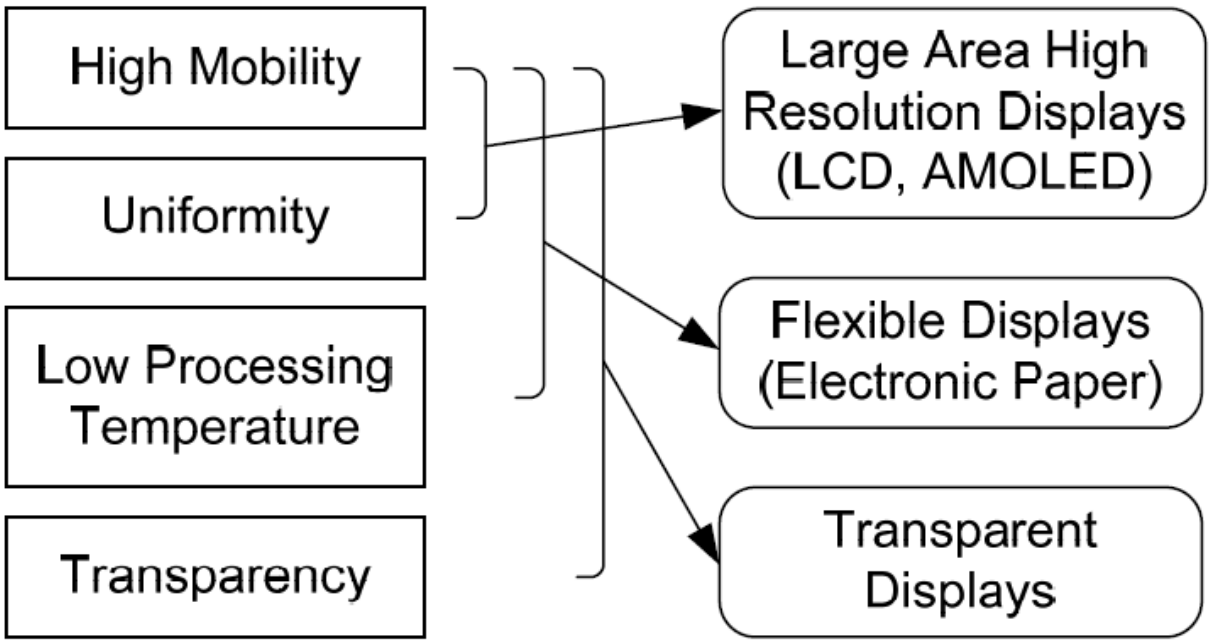


Figure 1-12. Besides transparency. Amorphous AOS TFTs have additional useful characteristics to compete with existing technologies

Wager et al, "Transparent electronics" (2008) [45]

1.2.5.2 Electronic structure and carrier transport model of amorphous oxide semiconductors

The conduction mechanism in amorphous oxide semiconductors (AOSs) is very different from that in conventional Si-based semiconductors. Usually, amorphous silicon has poor carrier transport properties ($\sim 1 \mathrm{cm}^2/Vs$) relative to single crystalline silicon materials ($\sim 500 \mathrm{cm}^2/Vs$). This is related to the structure and conduction mechanism between amorphous and single crystal materials. Si has a strong covalent bond, and the conduction band minimum (CBM) and valence band maximum (VBM) are made of anti-bonding ($\mathrm{sp}^3\ \sigma^*$) and bonding ($\mathrm{sp}^3\ \sigma$) states of Si hybridized orbitals, and its band gap is formed by the energy splitting of the $\sigma - \sigma^*$ level shown by Figure 1-7(a) [46]. The mobility of a-Si:H (hydrogenated amorphous silicon) is limited to ($\sim 1 \mathrm{cm}^2/Vs$), as carrier transport is controlled by hopping between localized tail-states and band conduction is not achieved [13]. Therefore, this hopping mechanism is strongly related to the local range order or structure, such as the strained and disordered chemical bonds from rather deep and high density of localized states below conduction band minimum (CBM) and above valence band maximum (VCM), causing the carrier trapping process. On the other hands, the amorphous oxide semiconductors have strong ionicity and charge transfer occurs from heavy metal ion to oxygen atoms shown by Figure 1-7(b). When heavy metal ions and oxygen ions comes close, charge transfer occurs due to largely different electron affinity and ionization potential (Figure 1-7(c)). In addition, the Madelung potential which comes from the difference between cations and anions by virtue of their opposing charges stabilizes the ionized states during the ionic bonding process. As a result, in Figure 1-7(c), the Madelung potential induces the energy splitting and the conduction band minimum (CBM) is occupied the 2p orbital of oxygen and the valence band maximum un-occupied by ns orbital of cations. The CBMs with large spatial sized s-orbital of heavy cations overlaps with the neighboring metal s orbital, and

makes the conduction path for carriers which are not influenced largely by disordered local structure. This is the reason why the metal oxide semiconductors have high mobility ($\sim 10 \mathrm{cm}^2/Vs$) even though there are amorphous structure. Figure 1-8 shows the schematic drawing of the structure Si-based and metal oxide semiconductors structure. Figure 1-8(a) is the Si semiconductor layer which has the hopping mechanism to transfer the electron carriers. In single crystal structure, there is a transfer path with hopping mechanism because of the long range order in crystal structure using sp^3 hybridization orbitals, and have large amount of electron field mobility. However, the amorphous structure doesn't have any long range order in this structure, and electron carriers cannot move fast in this structure because of the barrier with random structure. In metal oxide semiconductor, large sized s-orbital of metal ion have an overlapping between an adjacent atoms, and there provide the current path of electron carrier. Even though there have amorphous structure in metal oxide layer, s-orbital is easy to overlap as shown Figure 1-8(b). Figure 1-9(a) demonstrates the relation between the hall mobility and carrier density in a-IGZO and c-IGZO. The hall mobility increases with carrier density, and this trend is opposite to that observed in simple crystalline semiconductors having ionized impurity scattering in highly doped semiconductor due to the percolation model [46]. The basic concept of percolation model is that there are different electron conduction path as shown Figure 1-9(b). Amorphous semiconductors have a potential fluctuation above the mobility edge and the distribution of potential barriers exists in the conduction band. These different paths cause the different conductance for the electron transmission over the potential barrier. In other words, the carrier density creates the degenerated conduction for a-IGZO and c-IGZO. Figure 1-10 shows the trap density in a-IGZO and a-Si:H. The density of states of a-IGZO near conduction band are lower than a-Si:H [47]. The low defect density in the a-IGZO layer is the reason why a-IGZO has good

subthreshold slope in the transfer curve. This is therefore possible to apply the low voltage driven TFTs for having low power consumption.

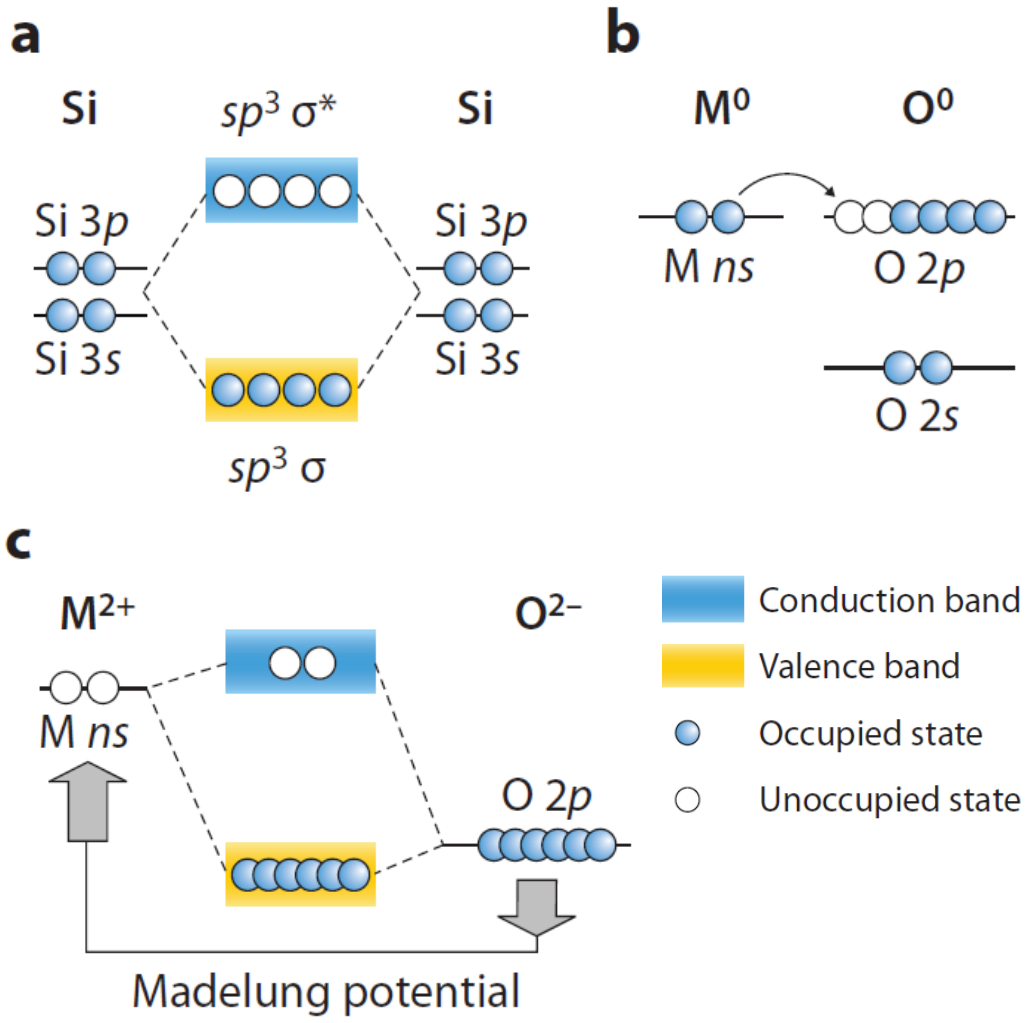


Figure 1-7. Schematic electronic structures of silicon and ionic oxide semiconductors. (a–c) Bandgap formation mechanisms in (a) covalent and (b, c) ionic semiconductors. Closed and open circles denote occupied and unoccupied states, respectively.

Kamiya et al, NPG Asia Mater, Vol. 2, Pages 15-22(2010) [46]

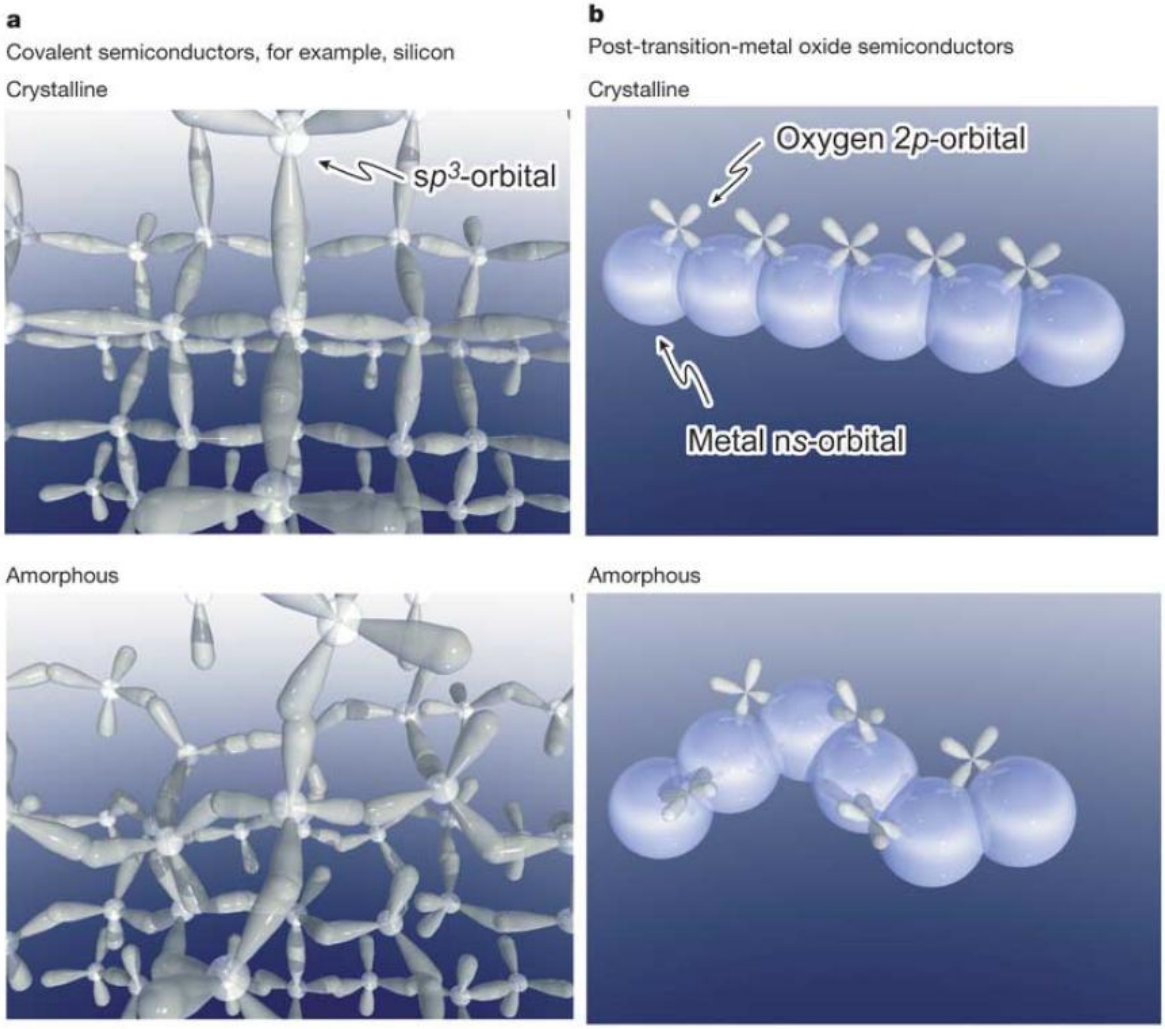


Figure 1-8. Schematic orbital drawings for the carrier transport paths in crystalline and amorphous semiconductors. (a) Covalent semiconductors with sp^3 orbitals (b) metal oxide semiconductors with s-orbital overlap of metal cation

Nomura et al, Nature, Vol. 432, Issue 7016, pages 488-492 [13]

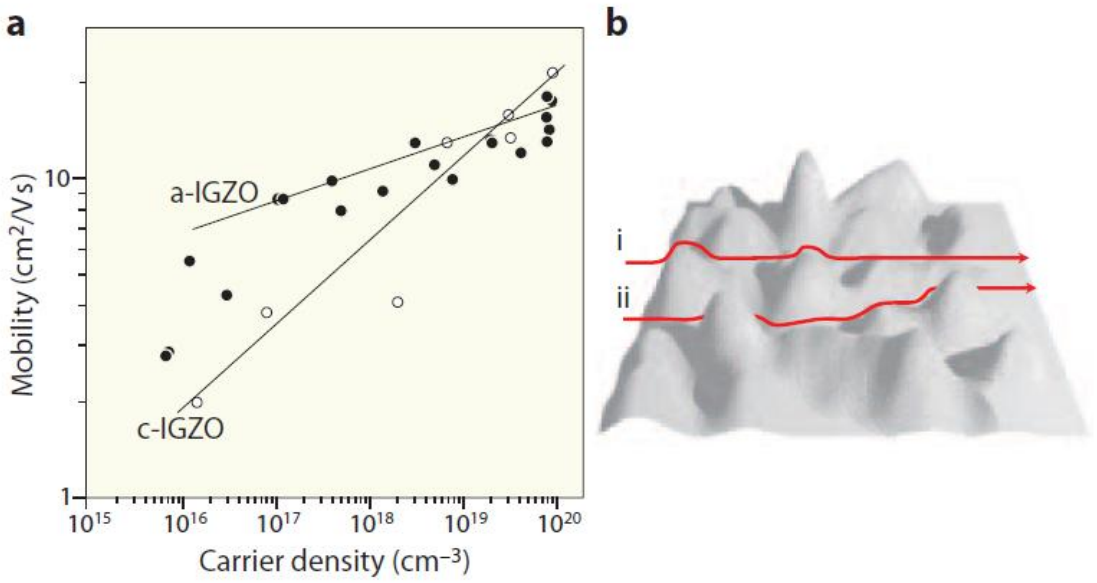


Figure 1-9. Carrier transport in a-IGZO (a) Relationship between Hall mobility and carrier density for c-IGZO and a-IGZO (b) Illustration of percolation conduction model showing examples of (i) a shorter path and (ii) a longer winding path

Kamiya et al, Science and Technology of Advanced Materials, vol. 11, Issue 4 (2010) [48]

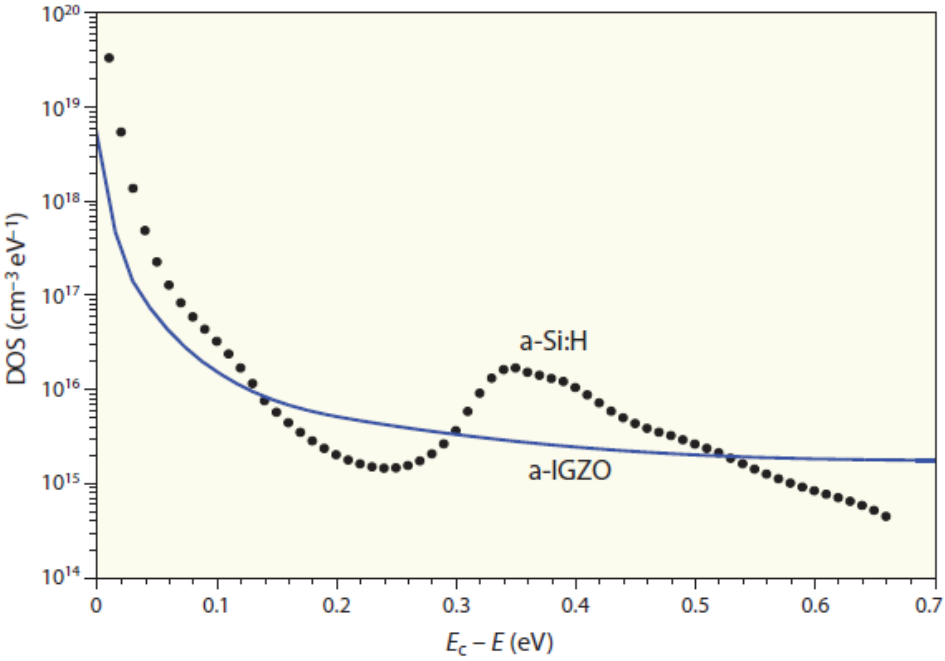


Figure 1-10. Subgap density of states in a-IGZO obtained by the C–V method. Data for a-Si:H are shown for comparison.

Kamiya et al, NPG Asia Mater, Vol. 2, Pages 15-22(2010) [46]

1.3 Electrowetting and microfluidic channel in lab on a chip device

1.3.1 Overview of electrowetting phenomena

Some decades after Young's discoveries, in 1805, a French physicist named Gabriel Lippmann investigated effects of electrocapillarity using mercury, and after that Froumkin studied how surface charge changed the shape of water droplet in 1936 [49]. The term of electrowetting was introduced in 1981 to describe an effect proposed for designing a new type of display [50]. Surface tension at the interface of two materials depends on their mutual properties. The below equation is Young's equation in which the contact angle θ, the angle created between the outer surface of the liquid and the surface on which it lies, depends on three surface tensions.

$$\gamma_{\mathrm{LG}}\, cos\theta = \gamma_{SG} - \gamma_{SL}, \tag{1.11}$$

The surface tension between the liquid and the air is γ_{SL}, between the surface and the air is γ_{SG}, and between the liquid and the air is γ_{LG}. Figure 1-11 schematically represents the relative forces operative to obtain Young's equation. In electrowetting, one is generically dealing with droplets of partially wetting liquids on planar solid substrates. Based on Lippmann's work, a term due to electro polarization was added the Young's equation.

$$\gamma_{\mathrm{LG}}\, cos\theta = \gamma_{SG} - \gamma_{SL} + 1/2CV^2, \tag{1.12}$$

In this Young-Lippmann equation, *V* is the electric voltage and *C* is the electric capacitance per unit area in the region of contact between the metal electrode and the drop. Therefore, the electric charges in the liquid are free to move, and the operation voltage is concentrated in different locations in droplet. The operation force on the charges within the liquid causes the

contact region between drop and the metal electrode to widen, or flatten out the droplet. Figure 1-12 represents the electrowetting properties which changes the wetting angle of droplet when a voltage is applied between the liquid droplet and biased substrate. A few years ago, Bruno Berge added the insulation layer between liquid and metal electrode to overcome to electrochemical reactions during operation [51]. It is possible to control without electrical conduction between the water droplet and the metal. This method is called EWOD "Electro Wetting On Dielectric". This was a significant technical breakthrough because the electrowetting created was stable for a long period of time.

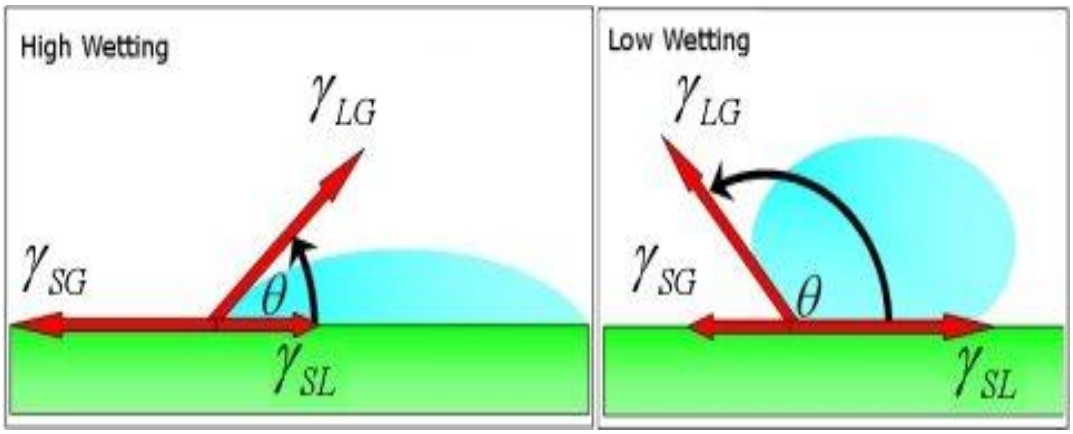


Figure 1-11. Different degrees of wetting: On the left there is high wetting and the contact angle is small. On the right side little wetting and there is a high contact angle.

Romi et al, Physicaplus, Issue 9 (2007) [52]

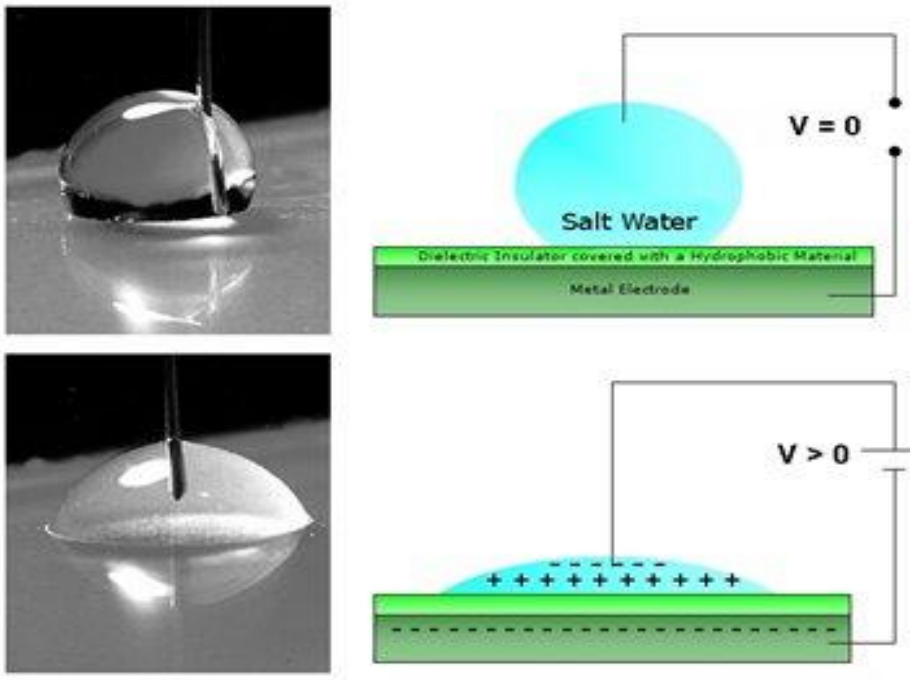


Figure 1-12. Liquid droplet on an insulated surface with and without applied voltage: Applying the voltage creates the wetting on the surface.

Romi et al, Physicaplus, Issue 9 (2007) [52]

1.3.2 Electrowetting on dielectric (EWOD) in a lab on a chip

Lab on a chip applications of electrowetting were mainly promoted by the laboratories of Richard Fair at Duke University [6] and Kim at UCLA [5] with several other groups joining later. Figure 1-13 shows the basic schematic EWOD structure consisting of a hydrophobic layer, insulator and metal electrodes. The principal of EWOD is to provide a substrate with electrode arrays allowing for moving droplets along an arbitrary path with a programmable activation sequence of the electrodes. Several operations can be performed including splitting, merging, mixing and forming microfluidic channel [3]. The actuation of a liquid droplet depends on the applied voltage of electrodes and capacitance of dielectric layer, and hydrophobic layer. Currently, many researchers have reported the various aspects of EWOD. The limitation of high voltage of EWOD driving can be overcome by thinning the dielectric layer on an EWOD to lower voltage driving of electrowetting, improve the wettability of liquid, and hydrophobic layer [1,3,4,6]. As this effort of electrowetting technology, the improvement of droplets moving speed on EWOD can be adopted for multi-functional moving and micro-channel devices. Figure 1-14 shows four fundamental droplet manipulation mechanisms in a digital microfluidic circuit [5]. With this kind of liquid handling technique a general electrowetting LOC device can be controlled by pressure control as well as electrowetting techniques.

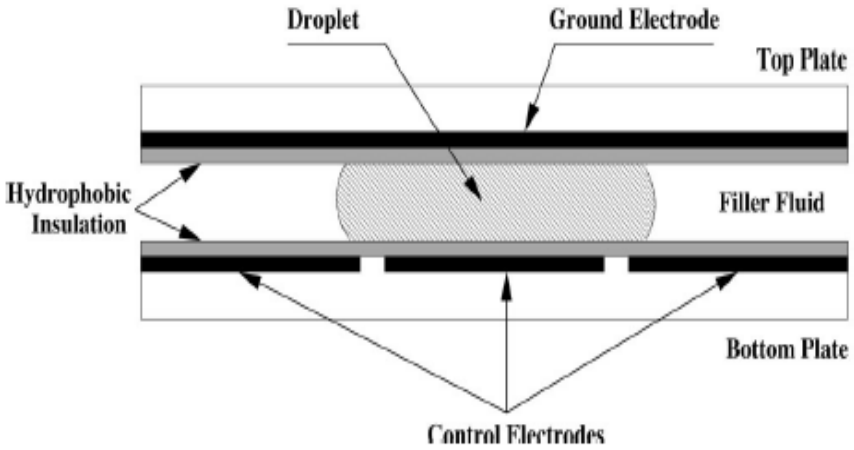


Figure 1-13. Schematic diagram of a typical lab on a chip device: EWOD consist of metal electrode, insulator layer (dielectric), and hydrophobic layer on top and bottom plates. Pigment droplet which is filled with oil lay on between top and bottom electrodes.

Cho et al, Journal of Microelectromechanical Systems, vol.12, issue1, p70-80 (2003) [3]

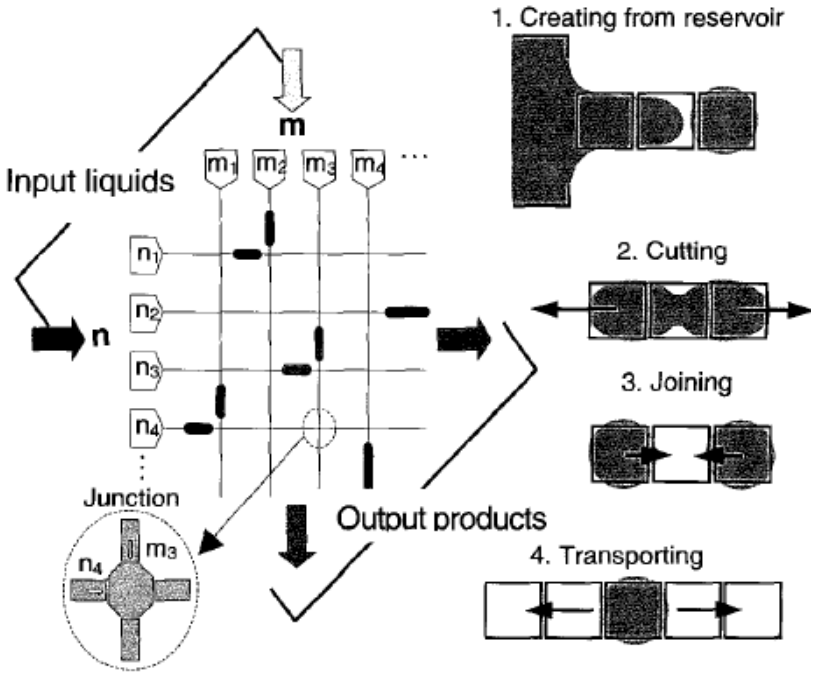


Figure 1-14. Envisioned digital microfluidic circuit and the four fundamental droplet operations necessary

Cho et al, Journal of Microelectromechanical Systems, vol.12, issue1, p70-80 (2003) [3]

Chapter 2

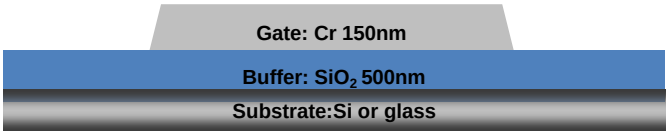
Device Fabrication and characterization

2.1 Fabrication of IGZO TFTs

In this study, we are focused on the inverted staggered bottom gate structure which is normally used in a-IGZO TFT structure. This structure has the below advantages: 1) protects the interface between gate dielectric and semiconductor layer without any exposure of external atmosphere 2) improve the contact resistance between IGZO layer and source drain electrodes 3) reduce the number of masks for IGZO TFTs. Figure 2-1 shows the schematic the inverted staggered bottom gate structure of IGZO TFTs with passivation layer, mask design of IGZO TFTs, and process flow of IGZO TFTs. We normally use 4 masks for IGZO TFTs. To test IGZO TFTs we have different sizes of TFTs, test elements group (TEG pattern) in our layout design. In this section we explain the fabrication methods and conditions of each step for TFTs and electrowetting devices.

(a) Schematic structure of IGZO TFTs

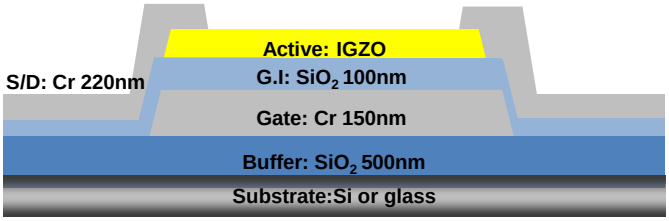
Mask 1: Gate



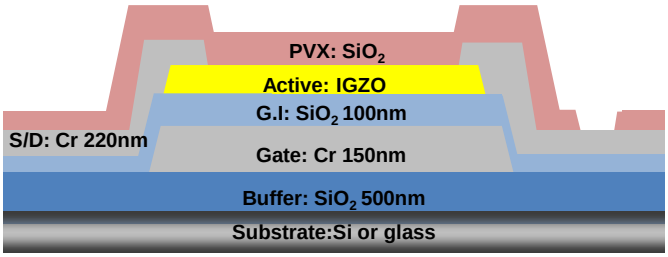
Mask 2: Active IGZO



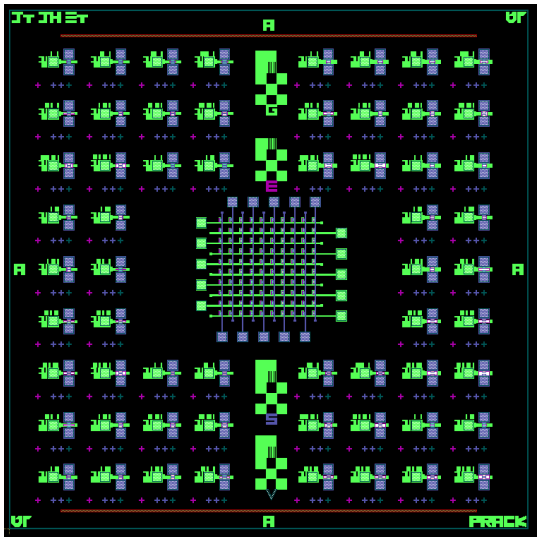
Mask 3: Source and Drain



Mask 4: VIA hole



(b) Layout design of IGZO TFTs



(c) Process flow of IGZO TFTs

1. Substrate: Si wafer or glass
2. Buffer: SiO_2 500nm by PECVD
3. Gate: Cr 120nm by sputter
4. Gate insulator: SiO_2 100nm by PECVD
5. Active: IGZO 50nm by sputter
6. S/D: Cr 150nm by sputter
7. PVX: SiO_2 200nm by PECVD
8. VIA hole: RIE Dry Etch
9. Post anneal: 350℃ 1hr air

Figure 2-1. The schematic structure of IGZO TFTs (a) Schematic structure of IGZO TFTs with process sequence (b) Layout design of IGZO TFTs (c) Process flow chart of IGZO TFTs

2.1.1 Gate electrode

The selection of metal electrode material for gate electrode must consider several factors. First of all, a low resistivity gate is essential for high speed operation and low power consumption because of RC delay for TFT operation. Low resistivity gate electrodes reduce the charging time to the gate dielectric layer and affect the inducing time in semiconductor layer. The resistance of metal line must be sufficiently low from the following equation,

$$\mathrm{R} = \rho\frac{L}{A} = \rho\frac{L}{Wd} = \frac{\rho}{d}\frac{L}{W} = R_s\frac{L}{W}, \tag{2.1}$$

Where ρ resistivity of metal electrode, *L* and *W* are the length and the width of metal line, the *d* is the thickness of metal thin film, and R_s is the sheet resistance. Table 2.1 shows the electrical properties of different metals [53]. In this study, chromium (Cr) was used for gate electrode because it has reasonably low resistivity, as well as high selectivity during fluorine based plasma etching (SF_6) during VIA hole etch process. In addition, chromium has a good thermal stability compared to aluminum and copper electrodes. Usually, the chromium gate layer deposited by rf magnetron sputter with DC substrate bias of 5W(125~126V) at 5mTorr working pressure using Ar gas which has the electrical properties of chromium layer in Figure 2.2 [54]. In our condition, chromium has $1.85\mathrm{X}10^{-5} ohm \cdot cm$ and deposition rate of Cr is $3.0\mathrm{nm/min}$. The chromium layer is lithographically pattered using wet chemical etchant including Ceric Ammonium Nitrate and Acetic Acid diluted by water (22% $Ce(NH_4)_2(NO_3)_6$ + 9% CH_3COOH +69% H_2O). The wet etch mechanism is the below process.

$$\mathrm{HClO_4} \rightarrow H^+ + ClO_4^-, \tag{2.2}$$

$$\mathrm{NH_4} \cdot 2\mathrm{Ce}\ \mathrm{NO_3}_{\ 6} \rightarrow 2NH_4^+ + Ce_4^+ + 6NO_3^-, \tag{2.3}$$

$$\mathrm{Cr} + 6\mathrm{Ce}_4^+ + 4H_2O \rightarrow CrO_4^{2-} + 6Ce_3 + 8H^+, \quad (2.4)$$

The etch rate is $\sim 66.7\mathrm{nm/min}$ at a room temperature without agitation, and for 150nm chromium requires $150\sim160\mathrm{sec}$ which includes a 20% over etch time. The wet etch process is an isotropic etch which creates sidewalls with a typically shallow edge ($\sim 45^{\circ}$). This is ideal for good step coverage for the next thin dielectric SiO_2 layer. Figure 2-2 represents the SEM image of chromium gate and SiO_2 gate dielectric layer which has good step coverage.

Table 2-1. Resistivity of different metals at 20-25℃, and temperature coefficient resistance

Metal	Resistivity at 20-25℃ (μΩ-㎝)	Temperature Coefficient Resistance (10^{-3} ℃)
Ag	1.59	4.100
Al	2.65	4.290
Au	2.35	4.000
Cr	12.90	3.000
Cu	1.67	6.800
Ir	5.30	3.925
Mo	5.20	-
Nb	12.50	-
Pt	10.60	3.927
Ta	12.45	3.830
Ti	42.00	-
W	5.65	-

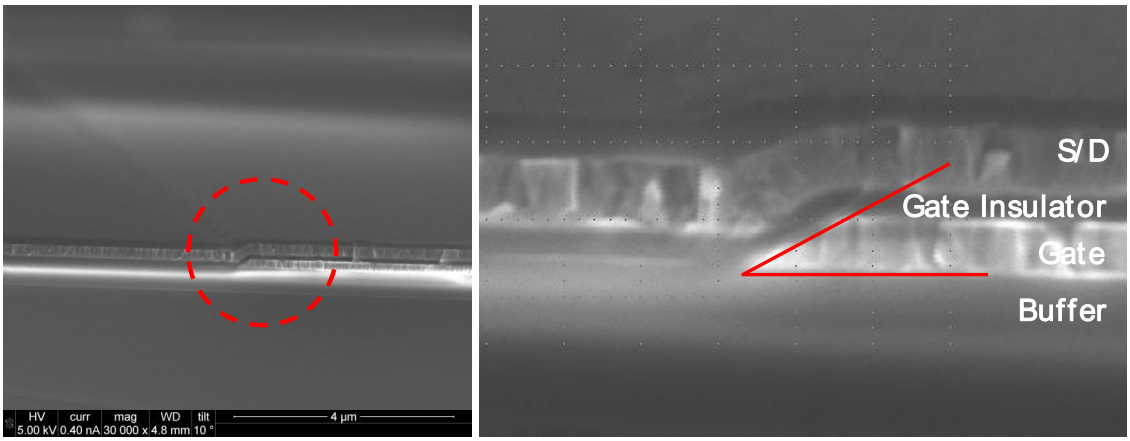


Figure 2-2. SEM images of TFTs represent the step coverage of gate insulator on Cr gate electrode

2.1.2 Gate insulator

Silicon dioxide (SiO_2) has been widely used as a gate dielectric layer of thin film transistor devices. In metal oxide semiconductors the gate dielectric requires a high electrical resistance to minimize gate leakage current at the overlapped area of S/D, and high compatibility to semiconductor layer such as interface properties and interface reactions. Many researchers have studied the optimized gate insulator layer using different gate dielectric layers such as SiO_2, SiN_x, Al_2O_3, ATO ($Al_2O_3TiO_2$) [55-59]. In this study, SiO_2 (100nm) gate dielectric material is deposited by plasma enhanced chemical vapor deposition (PECVD). The standard deposition condition of PECVD SiO_2 film is 20W RF power, 1000mTorr pressure, 5% SiH_4-Ar/N_2O (85/157sccm) gas flow, and 350℃ temperature. The deposition rate is 68.9nm/min. Figure 2-3 shows the leakage current of different gate dielectric layers and the capacitance of dielectric layers. SiO_2 and SiN_x are deposited by PECVD, and the other layers are deposited by rf sputter. All thicknesses of dielectric layers are 200nm and the electrode area is 3.24×10^{-6} ㎠. In case of

SiO_2 layer the current density (J) has below 10^{-8}A leakage current up to 15MV/cm and the capacitance of SiO_2 layer is about 8.0pF in this sample (Figure 2-3(d) represents only Al_2O_3, SiO_2, SiN_x dielectric. In case of TiO_2 and aluminum-titanium oxide (ATO) dielectric we cannot measure the capacitance because of the high leakage current.). This is a good dielectric property of IGZO TFT, and also have good hysteresis characteristic in transfer curve of IGZO TFT. Figure 2-4 shows the hysteresis of transfer curve of IGZO TFTs with SiO_2 and SiN_x gate insulator. As we can see the transfer curves of SiO_2 and SiN_x, hysteresis of SiO_2 dielectric layer is smaller than that of SiN_x (less than 1V of SiO_2, ~5V of SiN_x), and V_{th} represents ~10V of SiO_2 and ~20V of SiN_x. Based on these results, we choose the SiO_2 gate dielectric layer for our full integrated TFT - electrowetting devices.

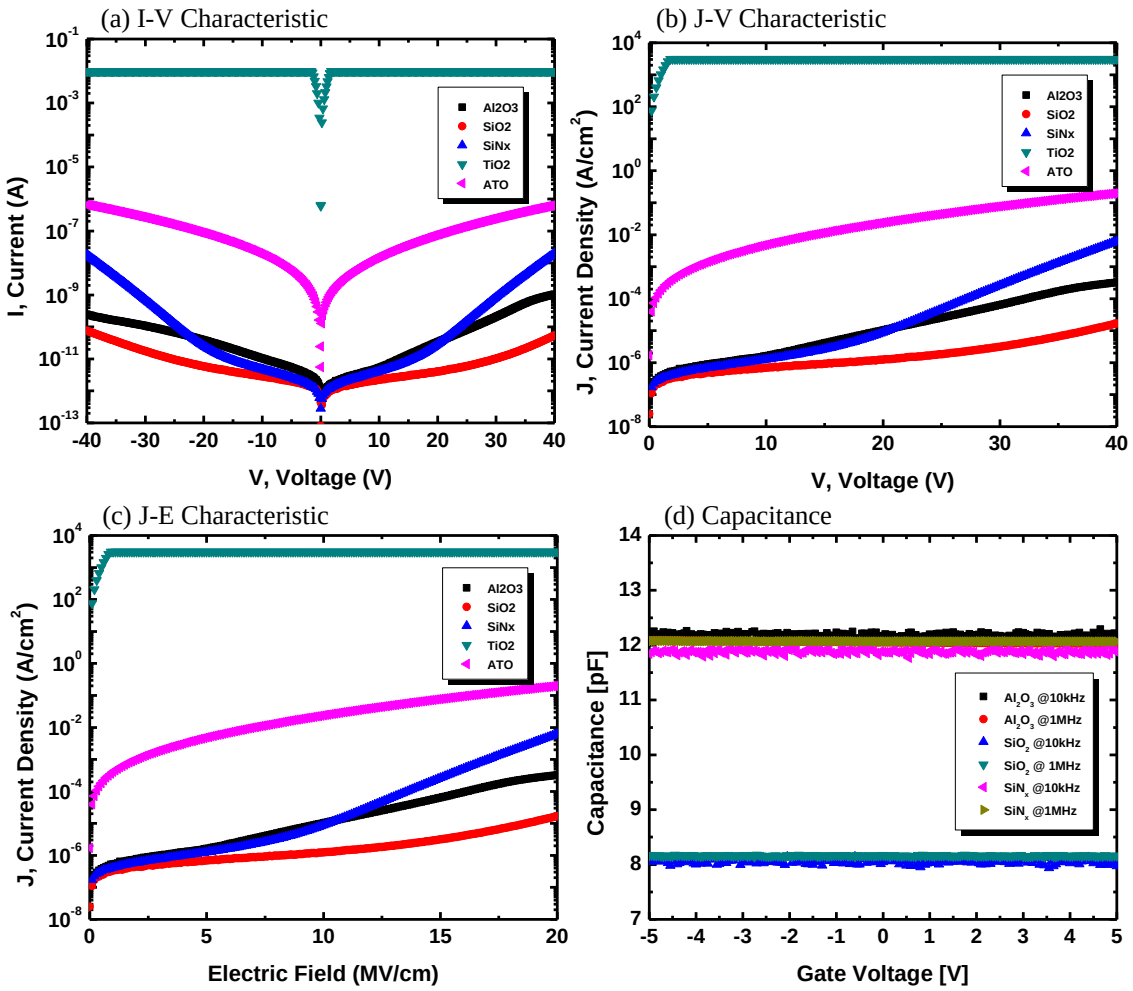


Figure 2-3. I-V characteristics, J-V characteristics, J-E characteristics, and capacitance of different gate insulator layers (Al_2O_3, SiO_2, SiN_x, TiO_2, and ATO)

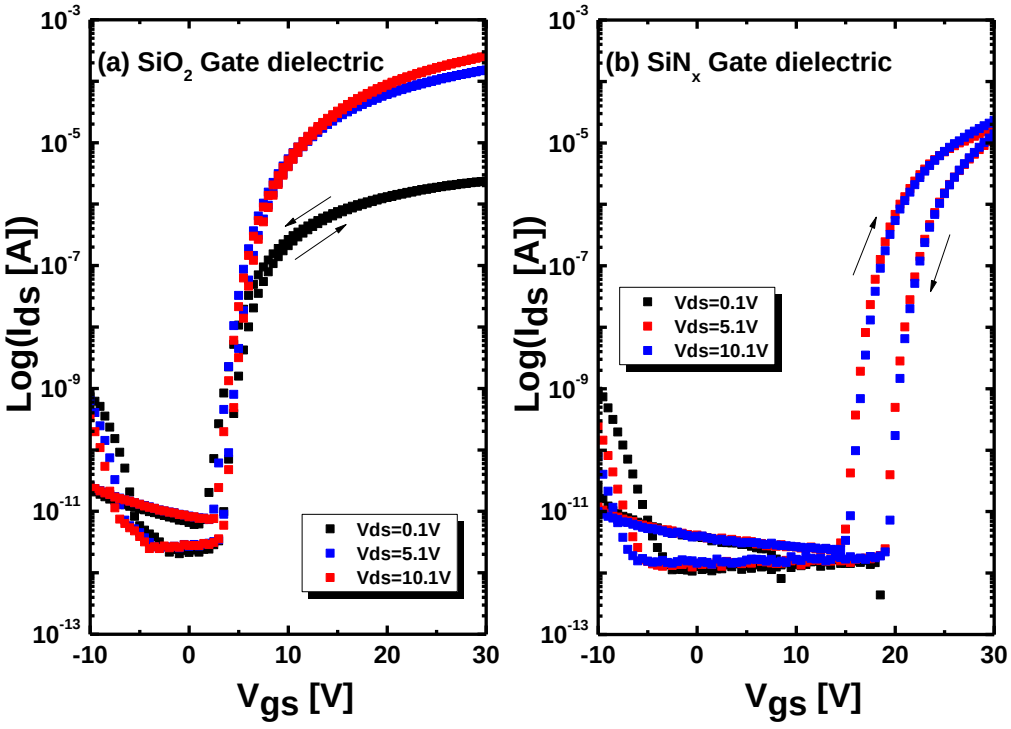


Figure 2-4. Transfer hysteresis curves of different gate dielectric layers

2.1.3 Semiconductor layer

As already mentioned the chapter 1, a-IGZO ($In_2O_3Ga_2O_3ZnO$=1:1:1 mol%) is used as the semiconductor layer in our device, and normally a-IGZO is very sensitive to the deposition condition because the oxygen vacancy concentration controls the carrier concentration. During rf magnetron reactive sputtering with Ar and O_2 mixture gas, the total carrier concentration is determined by the oxygen partial pressure. In this study, we already optimized the deposition condition which is rf power 97W, pO_2 40%, and working pressure 5mTorr. In this condition the deposition rate of IGZO film has 1.18nm/min. The a-IGZO was patterned by a wet etch process using the 0.01% diluted buffer oxide etchant solution (based on HF). The a-IGZO 50nm was completely etched after ~30sec including 20% over etch time; the etch rate is around 120nm/min. In this study, we include the basic characteristics of the IGZO layer and the effects of the sputter deposition conditions in the next chapter 3.

2.1.4 Source and Drain electrode

Chromium was mainly used for the source and drain electrode in our study. In the TFT device, the total turn-on resistance (R_{total}) of the thin film transistor (TFT) is expressed as

$$\mathrm{R_{total}} = R_S + R_{CH} + R_D, \tag{2.5}$$

where R_S is the resistance associated with the source contact, R_D is the resistance associated with the drain contact, and R_{CH} is the channel resistance of semiconductor layer. Figure 2-5 shows the schematic diagram the turn-on resistance of TFTs. There are many factors to select the source drain electrode of a-IGZO semiconductor and many researchers have reported the contact issues for different materials of source drain electrodes [60-67]. First of all, the work function of the

metal is key factor that controls the so-called Schottky barrier height and contact resistance of the metal on semiconductor which is related flat band and threshold voltages of the metal oxide semiconductor device. The occurrence of the Schottky barrier between the metal and semiconductor arises due to the requirement that the Fermi levels in the two materials match up. Such a barrier to charge transfer between the metal and the semiconductor is the result of the unequal work functions of these materials. We can predict the contact and behavior between the metal and semiconductor by comparing the work functions. Table 2-2 lists the selected values of the work function of the metals of interest [53]. Figure 2-6 shows the schematic band diagram which creates the bend bending between the semiconductor layer and metal electrodes [68]. The work function of a-IGZO films have a reported value from 4.3eV~5.01eV [69]. In this study, chromium (Cr) or Ti/Au metal layers are used as source/drain electrodes in our TFTs because of its relative low resistivity, ohmic contact between IGZO and S/D electrode, and high etch selectivity between IGZO and Cr electrode during S/D wet etch. The Cr source/drain electrode is deposited 200nm thick by rf magnetron sputter with substrate bias 5V to decrease resistivity and film stress (as already reported chapter 2 gate electrode section), and patterned by wet etching using Cr etchant, which has selectivity of Cr/a-IGZO=13 [70].

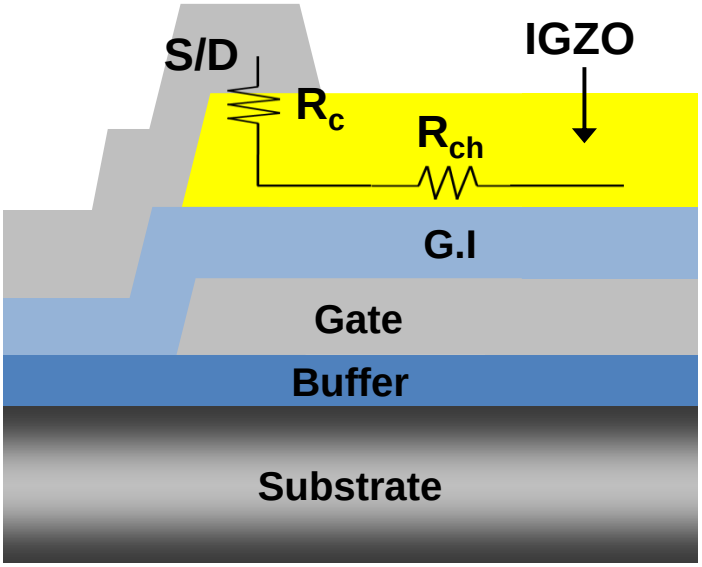


Figure 2-5. Schematic diagram the S/D contact resistance between S/D and IGZO layer, and channel resistance of IGZO layer

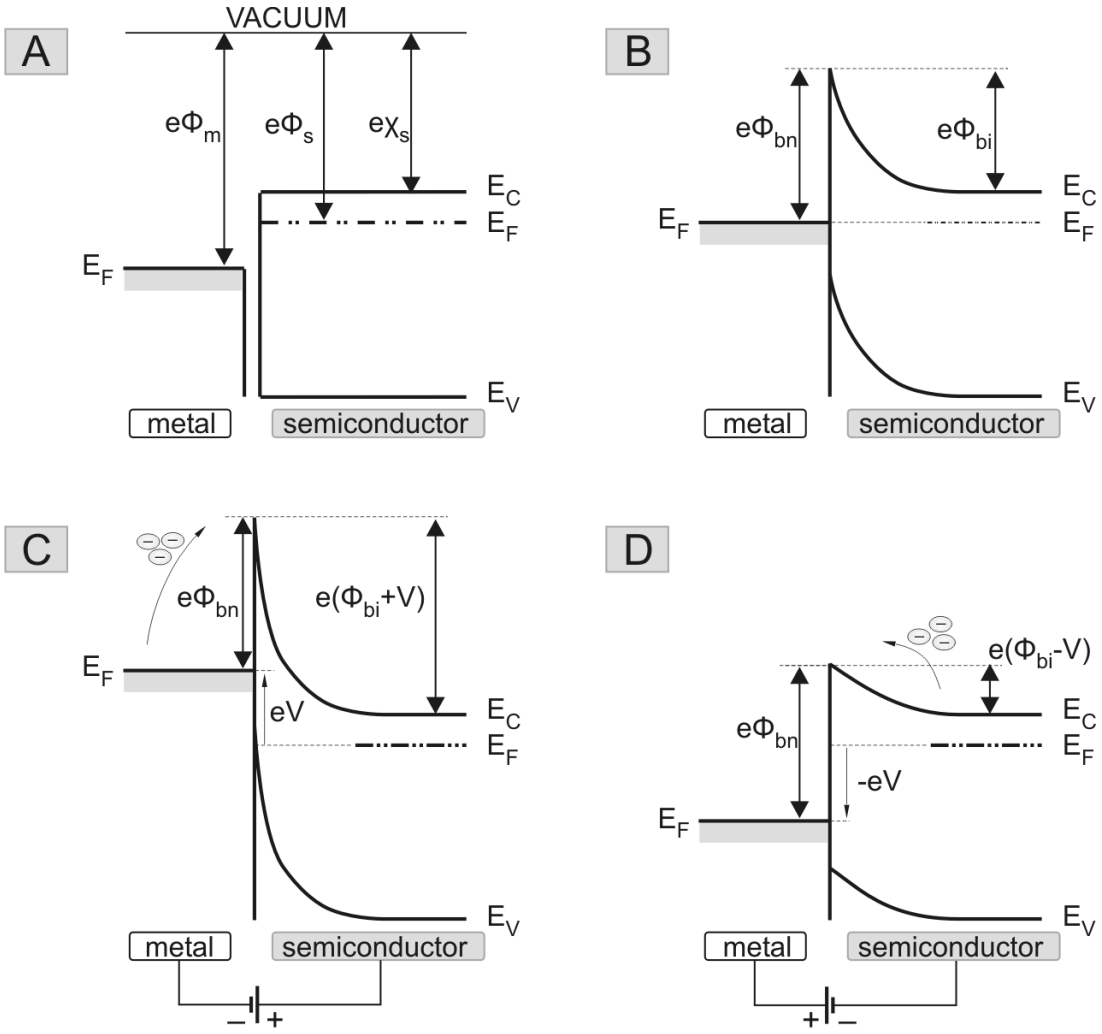


Figure 2.6 Band diagram the match-up between S/D metal and semiconductor layer (a) metal and n-type semiconductor before contact (b) metal and n-type semiconductor after contact (c) metal and n-type semiconductor contact with reverse bias (d) metal and n-type semiconductor with forward bias

D.A. Neamen et al, "Semiconductor Physics and Devices" [68]

Table 2-2. Work function of different metals

Metal	Work Function Φ_m (eV)
Ag	4.73
Al	4.08
Au	4.82
Cr	4.60
Cu	-
Co	4.40
Mo	4.20
Nb	4.01
Pt	5.34
Ta	4.19
Ti	~4
W	4.52

2.1.5 Passivation layer

A passivation layer in a TFT commonly has been used to protect the device from subsequent post processing and the external environment. In case of AOSs, the passivation layer affects the electrical characteristics of TFTs and the stability because of the sensitive back-channel effects of semiconductor layer. This topic will be studied in detail in chapter 4. We deposit the different passivation materials (such as SiO_2, SiN_x, Hf_2O_3, Al_2O_3, and Y_2O_3) using different deposition methods. We optimize the material of passivation layer and deposition method, and we investigate the mechanism why and how the passivation layer affects the electronic characteristics of a-IGZO TFTs. Currently our standard process of passivation layer consists of a 200nm SiO_2 which is deposited by 200℃ PECVD process. After photolithographic patterning, in order to contact the gate and S/D electrodes we etch the VIA hole process using RIE dry etch using SF_6 + Ar gas chemistry.

2.1.6 Post annealing for TFTs activation

The a-IGZO TFTs are typically thermally activated by furnace annealing in an N_2 or air ambient to recover the electronic characteristics of TFTs during the process steps. The post annealing effect on the a-IGZO TFT have been reported based on different atmosphere, temperature and time [71-73]. In this study we takes the post annealing in N_2 or air atmosphere of 350℃ 1hr. The temperature ramping rate is ~ 10℃/min in tube furnace or ~15℃/min in box furnace and cool down to room temperature. Figure 2-7 represents a standard temperature profile during the post annealing. In chapter 4, we investigate the effect of different atmospheres during the post annealing process. Currently, the whole process of IGZO TFTs is mentioned the above.

Figure 2-8 represents the SEM image of our TFT samples including the cross sectional SEM images.

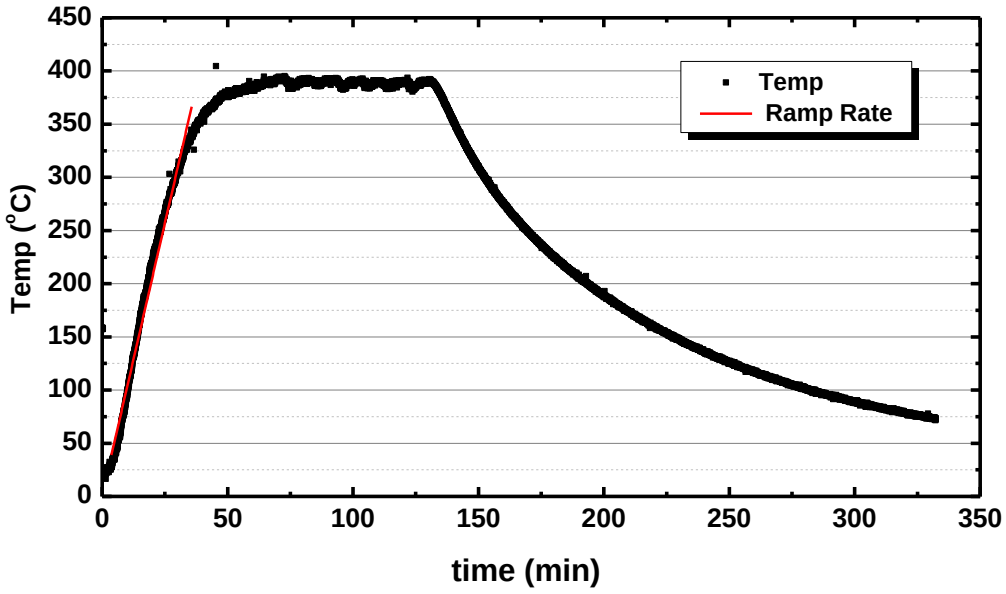
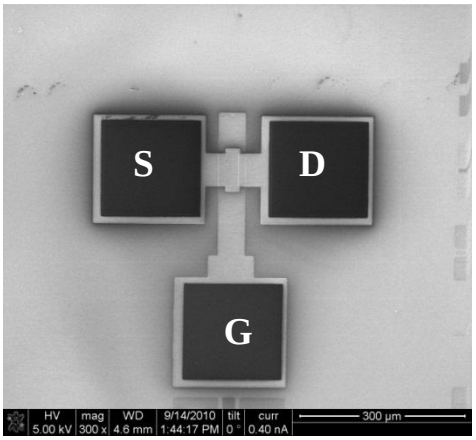
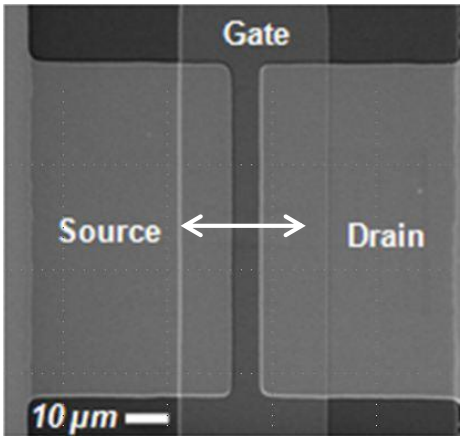


Figure 2-7. Micro oven temp history during the post annealing in air atmosphere

(a) IGZO TFTs



(b) Channel area



(c) Cross sectional SEM images of IGZO TFTs

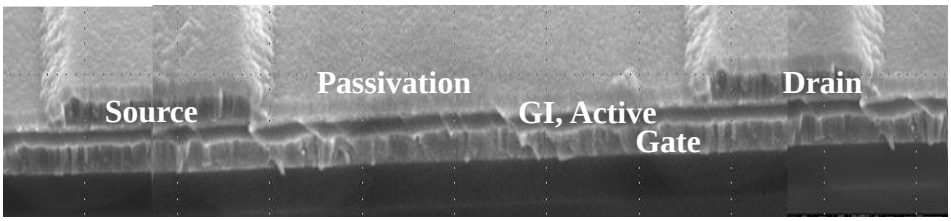


Figure 2-8. SEM images of IGZO TFTs, (a) Overview of IGZO TFT, (b) Channel area, and (c) Cross sectional SEM images of IGZO TFTs

2.2 Fabrication of the lab on a chip system which is fully integrated on the IGZO TFTs array

In this section, we introduce the design of electrodes for electrowetting on dielectric device (EWOD) and the fabrication of the EWOD device. As mentioned the chapter 1, the electrowetting device consists of a bottom and top plate. Bottom plates are fabricate on a glass substrate, with the electrowetting electrode of Al or Cr layer using rf sputter or e-beam evaporation and is connected to the applied voltage for droplet actuation. The electrowetting dielectric is normally a 200nm thick SiO_2 layer deposited by PECVD. After that, we coat the hydrophobic layer (Fluoropel 0.5um) with a dip coater, and cure this layer at 190℃ 30min on a hot plate. The top plate consists of a 100nm ITO layer ($In_2O_3SnO_2$, 10wt % SnO_2) which is connected to ground. A thin hydrophobic layer coating (Fluoropel 0.5um) is also deposited onto the ITO layer to make it hydrophobic. The deposition condition of ITO layer is pO_2 3.8%, working pressure 5mtorr, rf power 150W, and deposition rate is about 6.06nm/min. An aqueous solution is mixed with a pigment (a 10 wt % red pigment with 0.01 wt% of sodium lauryl sulfate was dispersed in the fluid) and insulating silicone oil (Dow Corning OS-30 oil) is infiltrated into the gap between the plates. Figure 2-9 shows the layout and cross section schematic drawing of electrowetting device.

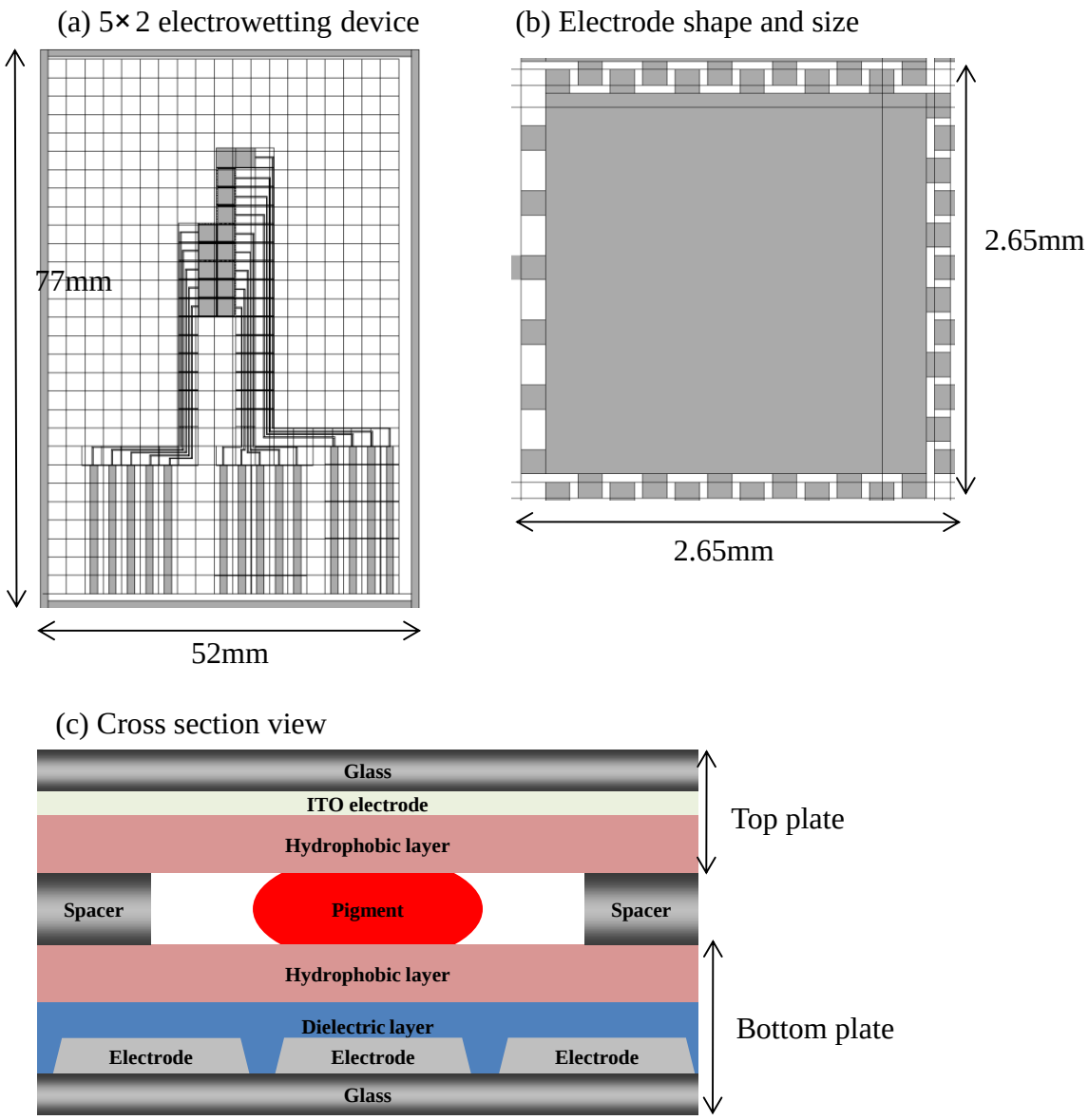


Figure 2-9. The whole layout of electrowetting device, (a) 5×2 electrodes device, (b) Electrode shape, and (c) Cross section view

Chapter 3

Basic characteristics and generalization of IGZO layer

3.1 Channel resistance and contact resistance

3.1.1 Introduction

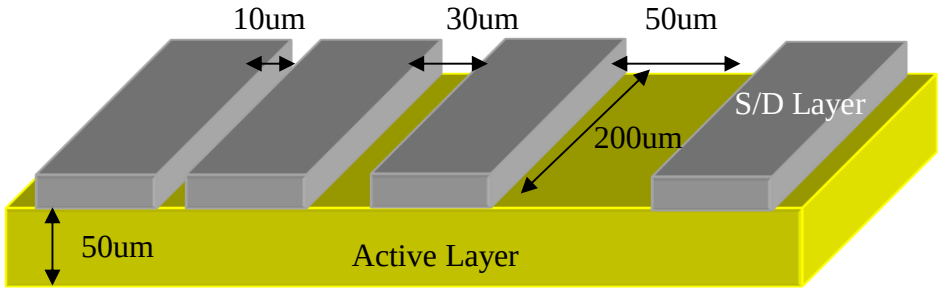
In this chapter we investigate the basic characteristics of amorphous indium gallium zinc oxide layer as used by semiconductor layer in our TFTs. In previous works, we reported the electrical resistivity of IGZO layer with oxygen partial pressure, optical properties compared with free carrier concentration, surface roughness, and basic structural studies of IGZO layers with annealing temperature dependence. Based on previous studies, we developed the optimized condition of IGZO semiconductor layer using rf magnetron sputter. In this study we investigate the channel resistivity and contact resistance of IGZO TFTs between S/D and IGZO layer when TFT is in the ON state. In addition, we investigate which resistance component of TFT channel layer is dominant for driving our IGZO TFTs.

3.1.2 Experiments

Figure 3.1 shows the schematic drawing of transmission line method (TLM) pattern and structure of IGZO TFTs. For the TFT fabrication we use the common gate with heavy doped p-type Si wafer, and then 100nm SiO_2 100nm grown by LPCVD as the gate insulator layer. The a-IGZO active layer (50nm) is deposited with pO_2 = 40% at fixed total gas flow rate (25sccm) and rf power 97W during sputtering. The source/drain electrodes are Ti/Au (10nm/100nm) evaporated by e-beam evaporation, and patterned by lift-off process. Finally, the post annealing was 350℃1hr at N_2 atmosphere. After annealing process we measured the TFT electrical

characteristics in TLM pattern with different size electrodes, and I-V characteristics between different size patterns to extract the channel resistivity and contact resistance.

(a) TLM pattern structure



(b) TFT sample structure

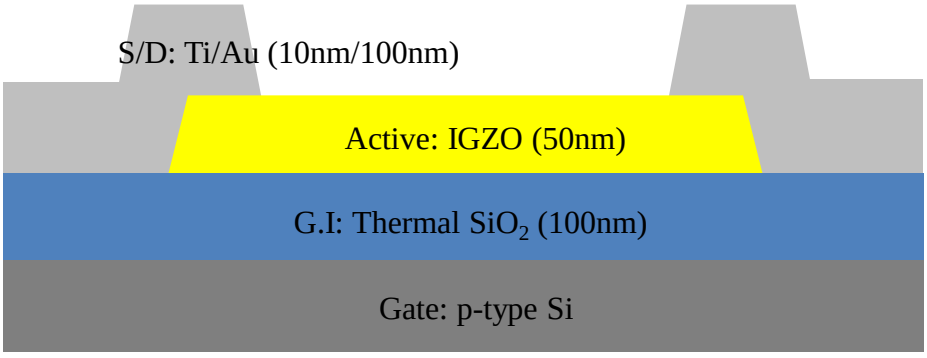


Figure 3-1. Schematic diagram for TLM pattern and TFT structure: (a) Transmission line method (TLM) Pattern, (b) Structure of IGZO TFTs

3.1.3 Results and discussion

The electric characteristic of IGZO TFTs is the extraction of the total TFT ON resistance (R_T) and the source/drain (S/D) contact resistance using transmission line analysis method (TLM) [74]. In Figure 3-2, the term "channel length (L)" is defined as the physical distance between the source and drain electrodes. However, the actual current in the channel cannot be addressed in an edge of S/D contacts. The real current path needs to extend a distance under the S/D electrodes which is usually recognized as channel length bias (ΔL). The total TFT ON resistance (R_T) can be described by

$$R_T = \frac{V_{DS}}{I_D} = R_S + R_D + r_{ch} \cdot L, \tag{3.1}$$

where r_{ch} is the TFT channel resistance per unit length, R_S and R_D are contact resistance of source electrode and drain electrode. From the general MOSFET equation, the drain current represents by

$$\mathrm{I_D} = \frac{W}{L} \cdot C_{OX} \cdot \mu \cdot (V_{GS} - V_{th}) \cdot V_{DS}, \tag{3.2}$$

where W and L are the channel width and length, respectively, and C_{OX} is the gate insulator capacitance per unit area. From (3.1) and (3.2) equations, we can express the TFT ON resistance R_T as a function of the apparent field-effect mobility (μ) and threshold voltage (V_{th}).

$$R_T = \frac{V_{DS}}{I_D} = \frac{L}{W \cdot C_{OX} \cdot \mu \cdot (V_{GS} - V_{th})}, \tag{3.3}$$

We can express the TFT channel resistance per unit length (r_{ch}) as a function of the intrinsic mobility (μ_{in}) and threshold voltage ($V_{th,\,in}$) from the ideal TFT equation.

$$r_{ch} = \frac{1}{W \cdot C_{OX} \cdot \mu_{in} \cdot (V_{GS} - V_{th,in})}, \quad (3.4)$$

In this equation, we can attain the intrinsic TFT parameters μ_{in}, $V_{th,\,in}$ are representative of the electrical characteristics of the conduction channel without the influence of the source/drain contact resistance. We apply the TLM pattern to our a-IGZO TFTs by analyzing a series of TFTs with the same channel width (200*um*) but different channel lengths (10, 30, 50*um*). The output curves and transfer curves for these TFTs are shown in Figure 3-3, and the TFT parameters are summarized in Table 3-1. The threshold voltage (V_{th}), subthreshold slope (*S.S*), and off-current value (I_{off}) are similar for the 3TFTs in TLM pattern.

At first, we plot R_T as a function of the TFT channel length for different V_{GS}, as shown in Figure 3-4. From this graph we can attain the total contact resistance of source and drain ($R_S + R_D$) and r_{ch} using the linear fitting ($R_L - L$) plot. Y interception and slope for different V_{GS} biases represent the ($R_S + R_D$) and the r_{ch}, respectively. The extracted source/drain contact resistance ($R_S + R_D$) and channel resistance ($r_{ch} \times L$) are both V_{GS} dependent as shown in Figure 3-5. ($R_S + R_D$) is 2.59kΩ at V_{GS}=20V and increase up to 22.05kΩ at V_{GS}=10V, and is more than one order of magnitude of smaller than the TFT channel resistance, depending on the channel length.

The intrinsic TFT parameters can then be obtained by plotting ($1/r_{ch} - V_{GS}$). The TFT channel resistances per unit length (r_{ch}) and contact resistance ($R_S + R_D$) are extracted from the slope and Y intercept of the plots for different V_{GS}, respectively. ΔL and R_0 can be extracted from the common cross point of all ($R_T - L$) curves shown in Figure 3-4. Using equation (3.4), $V_{th,\,in}$ and μ_{in} can be extracted by the X interception and the slope of ($1/r_{ch} - V_{GS}$) graph. The data shown in Figure 3-6 yield $V_{th,\,in}$ = 8.63V and μ_{in}= 6.22 ㎠/V-s. It can be observed from Table 3-2 that the

TFT apparent field effect mobility is slightly smaller than its intrinsic value. This effect is more severe for 10um channel length devices, since the channel resistance is smaller than that of 30um or 50um TFTs, and therefore more comparable to the source/drain contact resistance. In addition, 10um channel length device have more experiment errors during the S/D lift-off process.

The effect of the source/drain contact resistance can also be represented as an increase of the apparent channel,

$$R_T = R_S + R_D + \frac{L}{W \cdot C_{OX} \cdot \mu_{in} \cdot (V_{GS} - V_{th,in})} = 2 \cdot R_0 + \frac{L + 2\Delta L}{W \cdot C_{OX} \cdot \mu_{in} \cdot (V_{GS} - V_{th,in})}, \quad (3.5)$$

where R_0 represents the limit of R_S/R_D for a very high V_{GS}, and ΔL is associated with the effective channel length. Both ΔL and R_0 are originally independent of V_{GS}. The value of ΔL and R_0 are extracted from the ($R_T - L$) curves, which coordinate is ($-2\Delta L$, $2R_0$) as shown Figure 3-4. We obtained ΔL from 0.9um ~ 1.45um where the deviation of ΔL is affected by the experiment error of the S/D layer patterning. However, this is the effective channel length is longer than the real channel length, and $R_0 \sim 0\Omega$ which means a negligible source/drain contact resistance at very high V_{GS} voltage. In addition, we can suggests that a good ohmic contact between the source/drain (Ti/Au) and a-IGZO active layer.

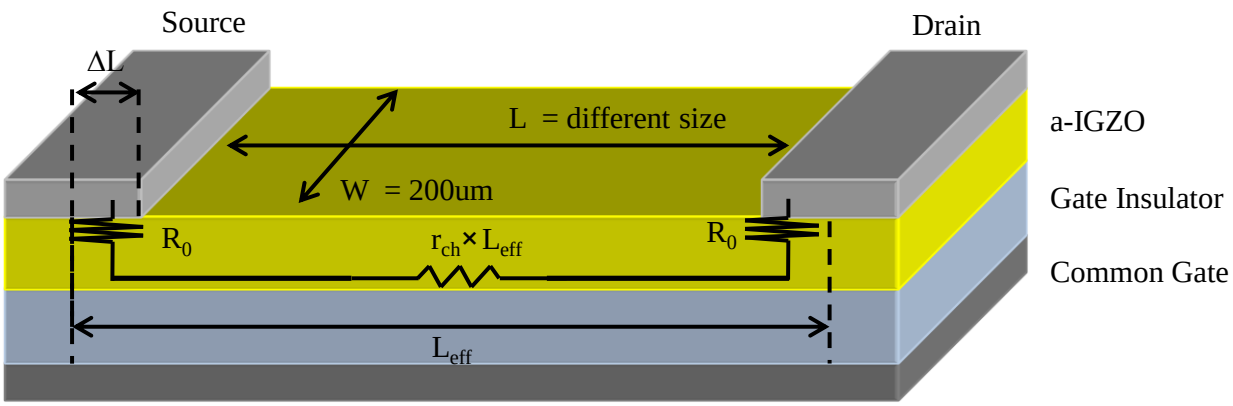


Figure 3-2. The schematic drawing the physical origin of the resistance components

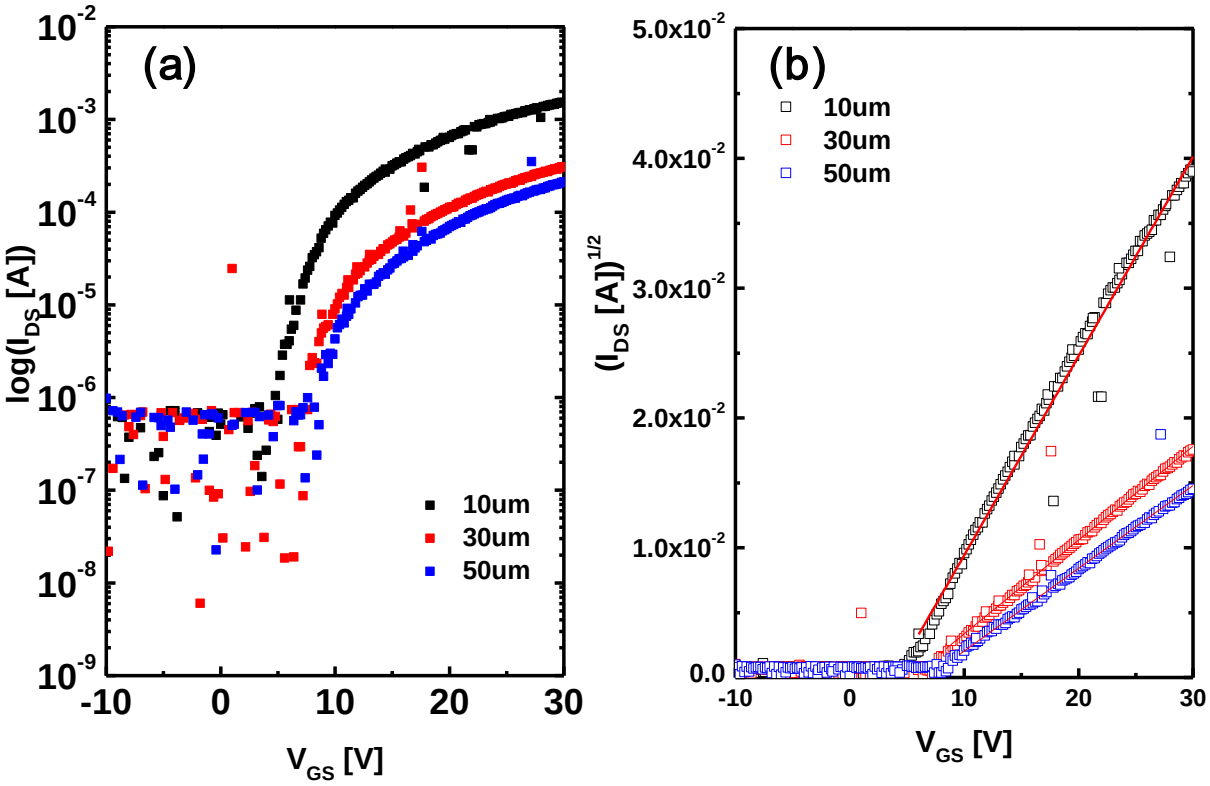


Figure 3-3. The transfer curve characteristics as different length TLM pattern TFTs, all TFTs have 200um width. (a) Log(I_{DS}) - V_{GS} (b) $(I_{DS})^{1/2}$ - V_{GS}

Table 3-1. Summary of electrical characteristics of a-IGZO TFT with different TFT size (W/L) at V_{DS}= 10.1V

TFT size (W/L) [um]	200/10	200/30	200/50
Vth [V]	3.85	5.33	6.82
S.S [V/dec]	1.69	2.13	2.41
Mobility [㎠/V·sec]	3.13	2.06	2.68
I_{on} [A]	1.4×10^{-4}	3.12×10^{-4}	2.06×10^{-4}
I_{off} [A]	1.34×10^{-7}	1.71×10^{-7}	7.21×10^{-7}

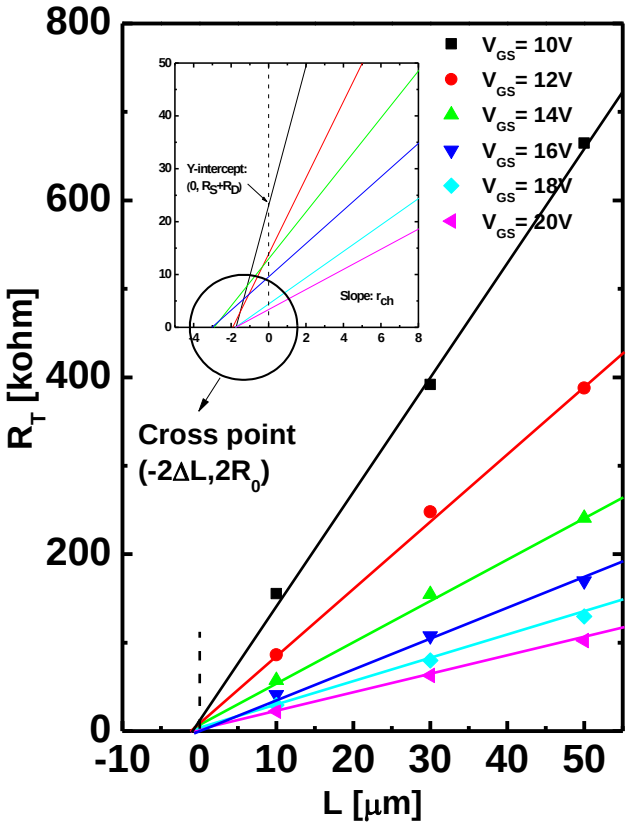


Figure 3-4. The total TFT ON resistance (R_T) versus channel length (L) for several levels of V_{GS}

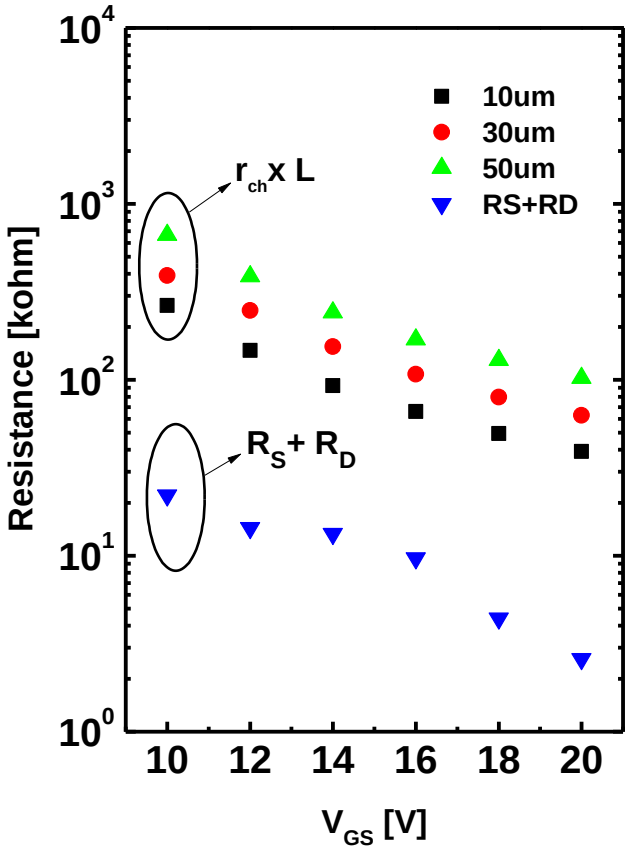


Figure 3-5. The Contact resistance (R_S + R_D) and the channel resistance (R_{ch}× L) as a function of V_{GS}

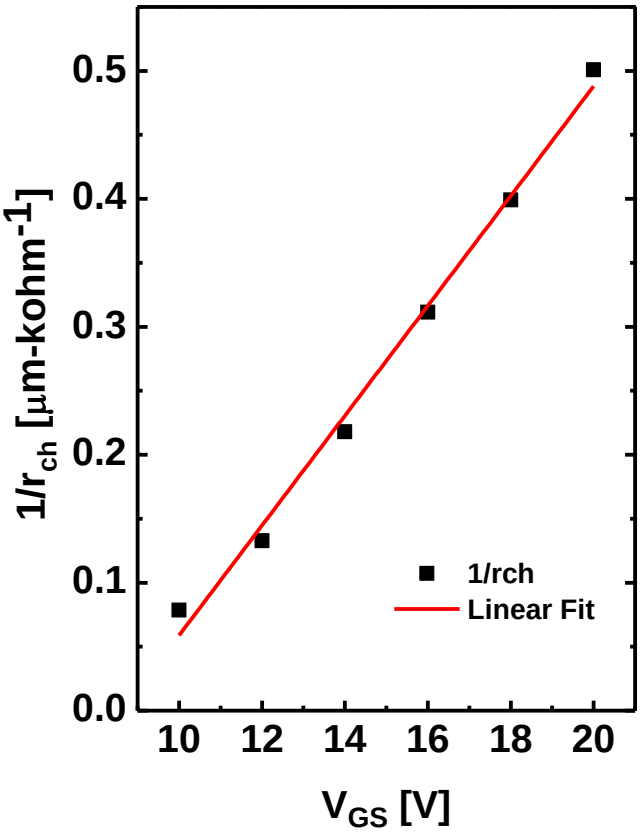


Figure 3-6. Extracting the intrinsic field-effect mobility and threshold voltage by plotting $1/r_{ch}$ versus V_{GS}

3.1.4 Conclusion

We fabricated the inverted staggered a-IGZO TFTs on Si wafer substrate using common gate. The devices demonstrated good electrical properties such as field effect mobility, threshold voltage, subthreshold slope, and on-off current ratio. The channel resistance of a-IGZO is much larger than the source/drain contact resistance between source/drain and a-IGZO active layer. In real driving voltage of high V_{GS} the contact resistance can be ignored the electrical properties of IGZO TFTs. The source/drain contact resistance examined by the TML method suggests that an Ohmic contact exists between source/drain (Ti/Au) and a-IGZO active layer.

3.2 Generalization the rf sputter condition of IGZO layer

3.2.1 Introduction

In this section, we investigate how to generalize the electronic characteristics of IGZO semiconductor layer. We already reported the quantitative calculation method for oxygen incorporation rate in IGZO rf magnetron sputtered film in our previous work [75]. This study demonstrates the generalization of the method and confirm at the previous work using IGZO TFT devices. Figure 3-7 represents the molecular incorporation rate of both IGZO and O_2. In the region where the effective oxygen incorporation rate is equal to the deposition rate with IGZO, the IGZO TFT has the best performance as electronic device. To confirm and generalize this result using the quantitative calculation method we fabricate the TFT samples which have different deposition rate and oxygen partial pressure with the same incorporation flux ratio of IGZO and O_2. In addition, we extend the generalization of different sputter targets which have same the composition.

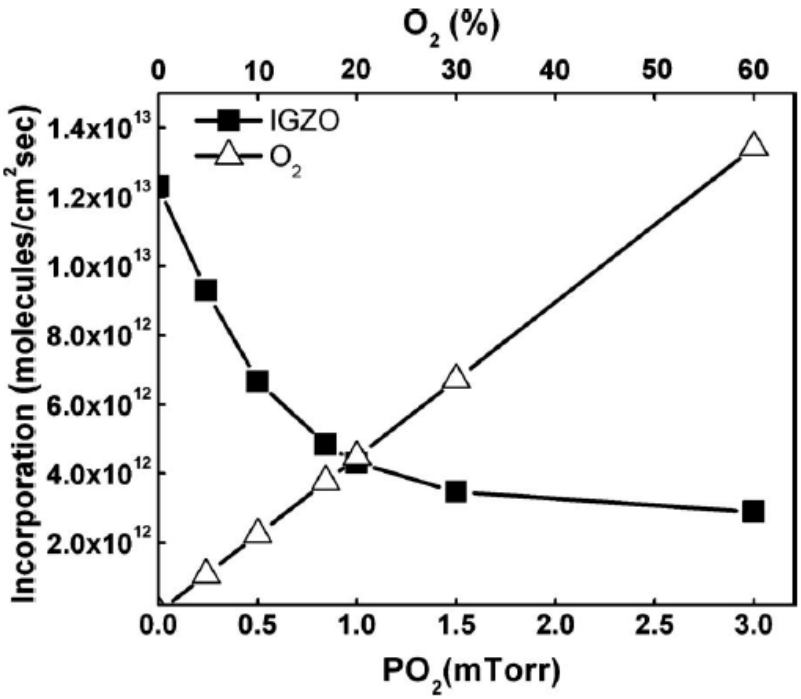


Figure 3-7. Molecules incorporation of IGZO and O_2 with oxygen partial pressure in growing IGZO film during sputtering

Kwon et al. / Journal of the Electrochemical Society, 158 (3) H289-H293 (2011)

3.2.2 Experiments

Before the fabrication of IGZO TFTs we investigate the same molecular incorporation rate between IGZO and different oxygen partial pressure. We prepare the samples to measure the deposition rate as a function of rf power with different oxygen partial pressure. We fix three sputter conditions with same oxygen and IGZO flux during IGZO sputtering in pO_2 = 20%, 30%, and 40%. TFT fabrication processes are same to chapter 3.1 using p-type Si wafer as the common gate. IGZO layers are deposited with three different conditions which is calculated and extracted from the below results. We measure the electrical characteristics of these TFTs, and compare the result. In addition, we prepare the two IGZO sputter targets which has same composition (In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol%), and we measure the deposition rate with same method to attain the sputter conditions with the same oxygen and IGZO flux during IGZO sputtering. The TFTs electrical characteristics are measured and compared between. The TFT size that was evaluated is W/L = 50um/20um.

3.2.3 Results and discussion

Figure 3-8 shows the deposition rate as a function of power and different oxygen partial pressure (pO_2 20%, 30%, and 40%). From this graph, we attained the relation between rf power and deposition rate of IGZO sputtering in each oxygen partial pressure where linear fits are used to interpolate or extrapolate the data.

The incorporation rate of O_2 is calculated by,

$$\Phi_{O_2} = \frac{P_{O_2}}{2\pi M_{O_2} kT}^{2} \ (molecules \times cm^{-2} \times \sec^{-1}), \quad (3.6)$$

where M_{O_2} is the molecular weight of O_2 (32g/mol), k is the Boltzmann constant, and T is the absolute temperature during sputtering (assumed at 298 K). The incorporation rates of O_2 at pO_2

20%, 30%, and 40% are 3.19×10^{17}, 4.78×10^{17}, and 6.38×10^{17} ($molecules \times cm^{-2} \times \sec^{-1}$). In our previous work, when the molecular incorporation rate of O_2 and IGZO (Φ_{O_2} $\Phi_{IGZO} \approx 1$) is the same, the electrical characteristics and resistivity of IGZO layer have good TFT performance. To attain the deposition rate of IGZO with oxygen partial pressure according the relation of Φ_{O_2} $\Phi_{IGZO} \approx 1$ we calculate the deposition rate with the below equation,

$$\Phi_{O_2} \approx \Phi_{IGZO} = g_{IGZO} \cdot \frac{\rho_{IGZO} \cdot N_A}{M_{IGZO}} \ (molecules \times cm^{-2} \times \sec^{-1}), \quad (3.7)$$

$$g_{IGZO} = \Phi_{O_2} \cdot \frac{M_{IGZO}}{\rho_{IGZO} \cdot N_A}, \quad (3.8)$$

where g_{IGZO} and ρ_{IGZO} are the deposition rate of IGZO (nm/min) and the density of a-IGZO (~5.9 g/㎤), respectively. N_A is Avogadro constant and M_{IGZO} is the molecular weight of IGZO (546.5 g/mol). Figure 3-9 represents the rf power value with the same oxygen and IGZO flux calculated by equation 3.8. All linear fit line on Figure 3-8 have the same oxygen and IGZO flux during IGZO sputtering. We choose the three values of different partial oxygen pressure at pO_2=20%, 30%, 40%, and the sputtering conditions for these oxygen partial pressure are shown the Table 3-2.

Figure 3-10 demonstrates three transfer curves of IGZO TFTs with different oxygen partial pressure and deposition rate. The three TFTs have the same flux of IGZO and O_2, and same electrical characteristics as shown Figure 3-10(d). Table 3-3 represents the electrical characteristics of TFTs with different oxygen partial pressure and same Φ_{O_2} and Φ_{IGZO}. The threshold voltages of these TFTs have 4.25V~6.1V which is only small deviation, less than 2V, and the field effect mobilities of TFTs have 7.21~7.54 ㎠/Vsec. In addition, other parameters such as I_D^{ON-OFF} and S.S (the subthreshold slope) have the value of ~10^9 and 0.31~0.40 V/dec.

Even though they have different rf power (deposition rate) and oxygen partial pressure during the IGZO sputter deposition, the electrical characteristics of TFTs with the same Φ_{O_2} and Φ_{IGZO} have exactly same properties.

To confirm the above result which IGZO semiconductor layers deposited the same condition with Φ_{O_2} $\Phi_{IGZO} \approx 1$ have the same electrical properties of TFTs, we test two different sputter targets of IGZO with same composition (In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol%). Using the new target, we calculated the Φ_{O_2} Φ_{IGZO} ratio and determine the same deposition rate for the Φ_{O_2} $\Phi_{IGZO} \approx 1$ condition. Target A has the pO_2 20%, rf power 60W and deposition rate is 0.612nm/min and Target B has the pO_2 20%, rf power 50W for the same deposition rate (0.612nm/min). Both sputtering conditions have the same oxygen partial pressure and deposition rate, thus we attain the same flux of IGZO and O_2 between two kinds of IGZO sputter targets. Figure 3-11 shows the transfer curves and output curves of IGZO TFTs with two different IGZO sputter targets. The electrical characteristics of TFTs deposited by two IGZO targets are represented in Table 3-4. The threshold voltages of two TFTs are 5.68V and 5.72V, and the mobilities are 8.65 ㎠/Vsec and 8.69 ㎠/Vsec. Thus we demonstrate that this is a very robust way of optimizing the appropriate sputtering conditions for IGZO thin film transistors.

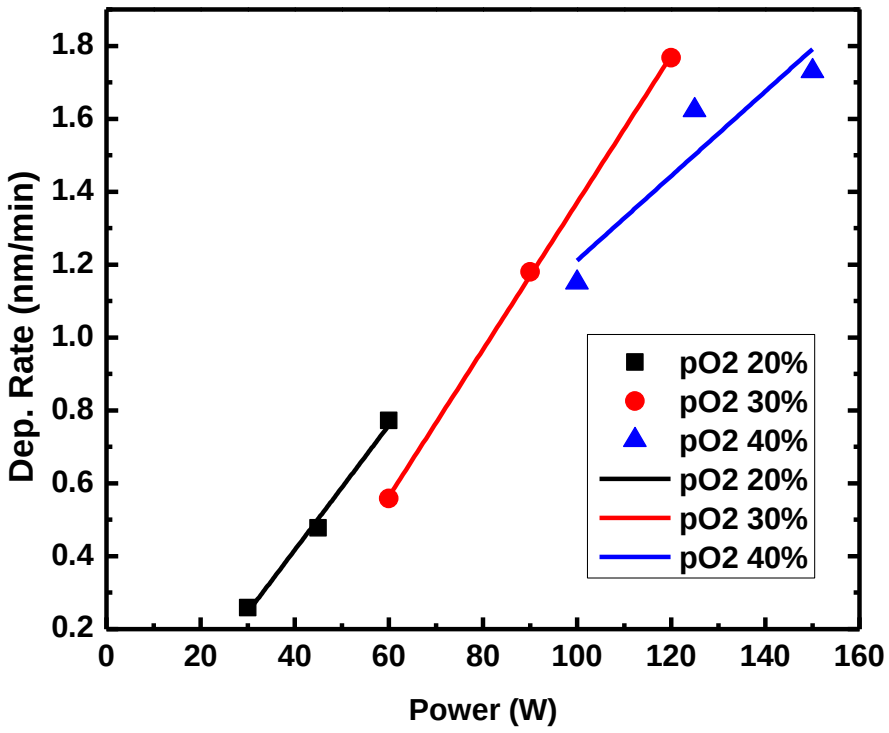


Figure 3-8. Deposition rate of IGZO layer with different oxygen partial pressure and different rf power

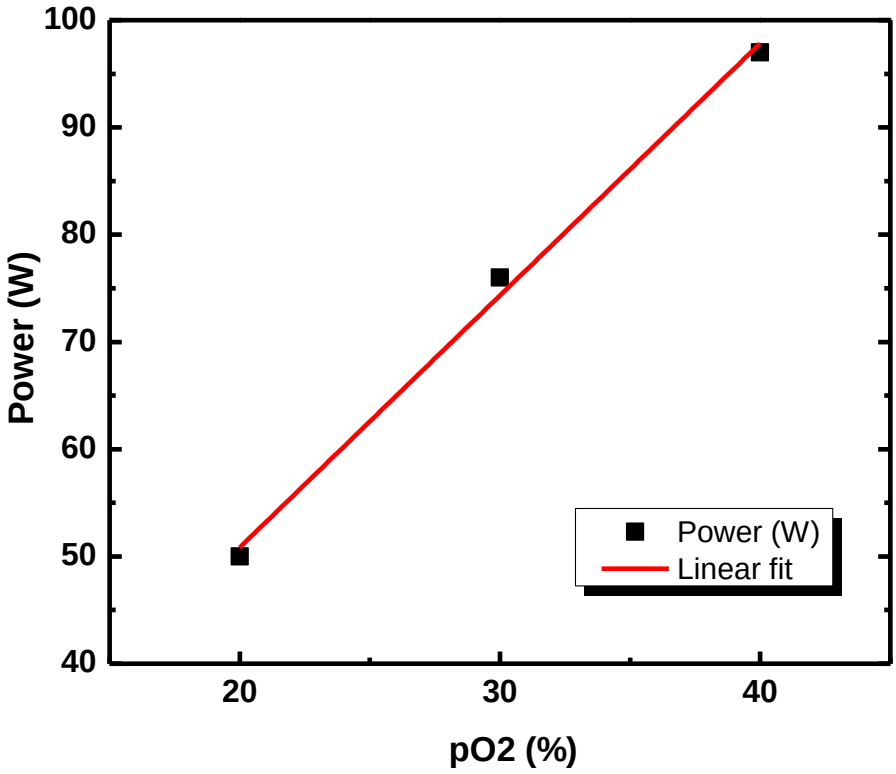


Figure 3-9. The power conditions corresponded the deposition rate which has the same oxygen and IGZO flux

Table 3-2. The sputter parameters of IGZO deposition with same oxygen and IGZO flux

Sputter deposition condition	RF power (W)	Working Pressure (mtorr)	Dep. Rate (nm/min)	Dep. Time (min sec)
pO_2 20%	50	5	0.59	84'45"
pO_2 30%	76	5	0.88	56'49"
pO_2 40%	97	5	1.18	42'37"

Table 3-3. TFT characteristics of the same Φ_{O_2} and Φ_{IGZO} which have different oxygen partial pressure and deposition rate

TFTs with pO_2 (%)	pO_2=20%	pO_2=30%	pO_2=40%
Vth [V]	6.10	4.25	4.34
S.S [V/dec]	0.40	0.31	0.31
Mobility [㎠/V·sec]	7.54	7.21	7.37
I_{on} [A]	1.8×10^{-4}	2.2×10^{-4}	1.9×10^{-4}
I_{off} [A]	2.0×10^{-13}	1.4×10^{-13}	2.1×10^{-13}

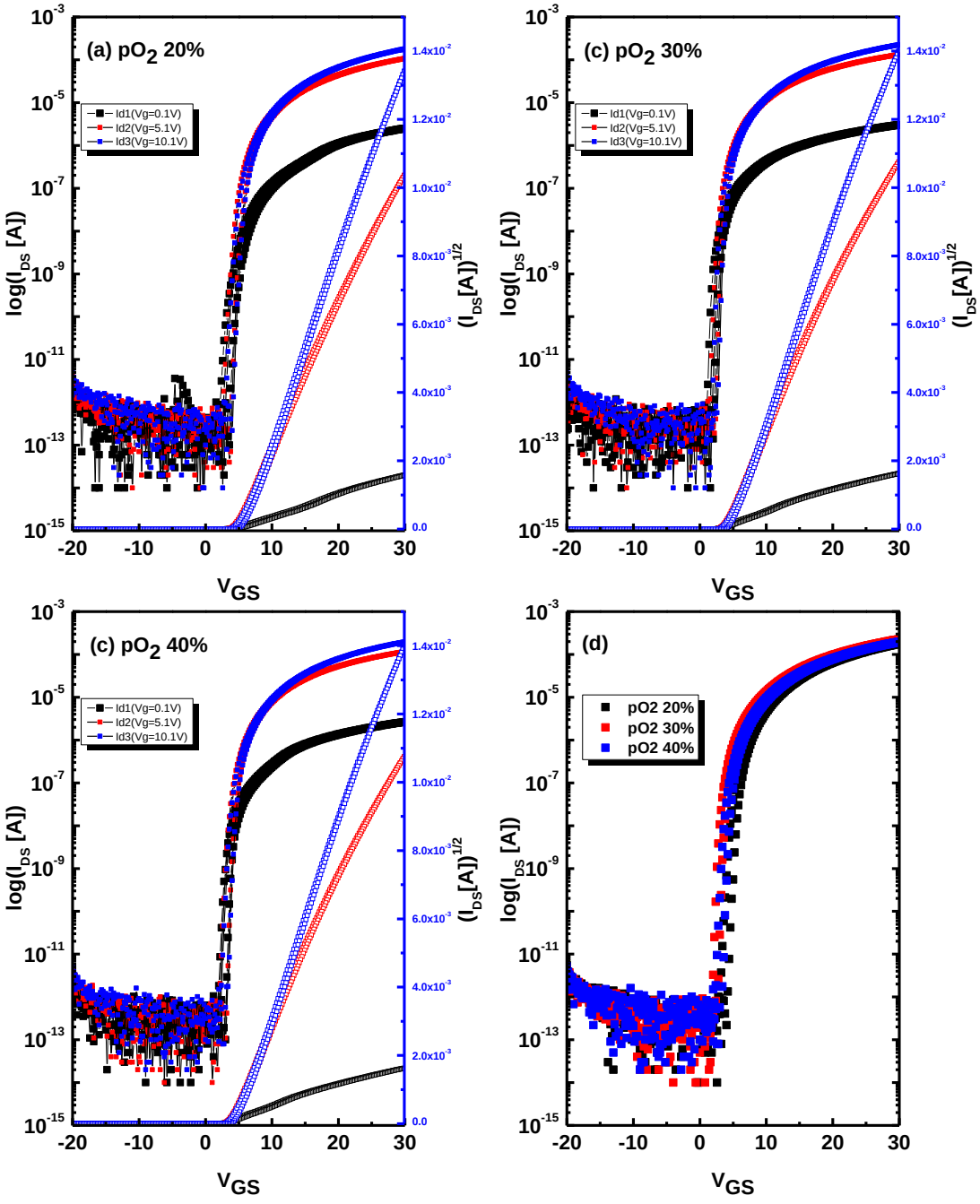


Figure 3.10. The transfer curves of the same Φ_{O_2} and Φ_{IGZO} which have different oxygen partial pressure and deposition rate: (a) pO_2 = 20%, (b) pO_2 = 30%, (c) pO_2 = 40%, and (d) merge the transfer curves of three TFTs at V_{DS}=10.1[V]

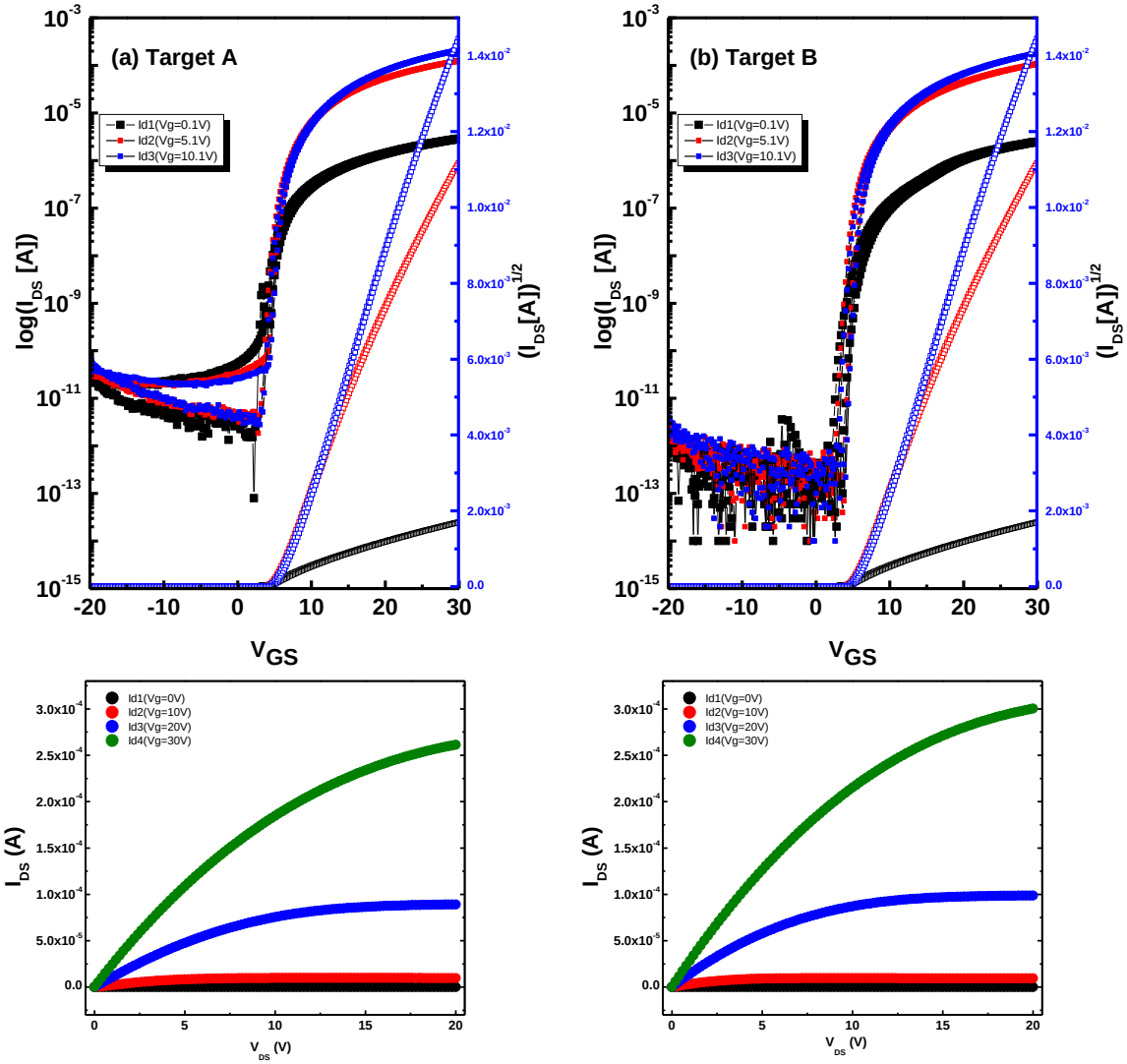


Figure 3-11. The transfer and output curves of the same Φ_{O_2} and Φ_{IGZO} of different sputter targets (a) Sputter target A (b) Sputter target B

Table 3-4. TFT characteristics of the same Φ_{O_2} and Φ_{IGZO} with different sputter targets

TFTs with different Sputter Target	Target A	Target B
Vth [V]	5.68	5.72
S.S [V/dec]	0.48	0.43
Mobility [㎠/V·sec]	8.65	8.69
I_{on} [A]	2.0×10^{-4}	1.7×10^{-4}
I_{off} [A]	9.4×10^{-12}	2.0×10^{-13}

3.2.4 Conclusion

In summary, we investigated the optimization and generalization of IGZO sputter deposition conditions by using the quantitative calculation method. We confirmed that the electrical characteristics of TFTs with same incorporation flux of IGZO and O_2 have similar TFT properties. Even though they have very different sputtering process conditions, they have the same IGZO TFT characteristics if we prescribe the same oxygen and IGZO incorporation flux during the IGZO deposition process. In addition, we expanded the generalization work with different IGZO targets. Therefore, if we calculate and extract the flux of IGZO layer during sputtering, we can find the optimized deposition condition from this work. In addition, as we controlled the deposition rate of IGZO and oxygen partial pressure of IGZO, we can increase the productivity of IGZO using the new condition for increasing deposition rate with a comparable increase in the oxygen incorporation rate. Thus we confirm the generalization of the rf sputter process of the IGZO layer and can be contributed to the many applications using IGZO TFTs.

*Acknowledgment

The quantitative calculation of oxygen incorporation in sputter IGZO films and the impact on transistor properties has been published previously in the Journal of The Electrochemical Society by Seyeoul Kwon, Joo Hyon Noh, Jiyong Noh, and Philip D. Rack [75]. In this section we confirmed the quantitative calculation method to apply the TFT devices with different conditions, and we expand the generalized works for different IGZO Targets. Of the work presented in this chapter Joo Hyon Noh and Seyeoul Kwon helped to the fabrication TFTs and measurement TFTs characteristics. Philip Rack provided direction, funding of the research, discussion and motivation.

Chapter 4

Characterization of Passivation layer

4.1 Introduction

The passivation layer (PVX layer) is typically used to protect devices from the additional post processing to and external ambient atmosphere. However, currently, amorphous oxide semiconductors have two big issues. One is the passivation issue and the other is stability of AOSs. A passivation layer in the TFT commonly is used to protect device from following process and to inhibit the external environmental effects.[76-79] The passivation layer suppresses the interaction between the active backchannel and ambient played a critical role in determining the V_{th} instability [80]. For devices without passivation layers on the back-channel of IGZO TFT the adsorbed oxygen and water (H_2O) can capture an electron from the conduction band and the resulting oxygen species can exist in various forms such as O^{2-}, O^- as described by the following chemical reaction, $O_2\ \ gas\ + e^- = 2O^-\ \ solid$. The capturing of an electron decreases carrier concentration on back-channel of IGZO TFTs and inhibits V_{th} negative shift on TFTs. Figure 4-1 shows the schematic diagram of oxygen and water adsorption in back channel of IGZO layer which is the origin of threshold voltage instability in IGZO TFT without passivation. Figure 4-2(a) represents $I_{D,\ SURFACE}$ is due to mobile carriers at the channel layer-passivation layer interface [79]. The effect of $I_{D,\ SURFACE}$ reflects the V_{th} negative shift in the transfer curve because of the additional carriers charge. Figure 4-2(b), illustrates how the electrical characteristics of TFT is degraded due to passivation layer. Many researchers have studied the mechanism of passivation layer to solve these issues of IGZO TFTs using N_2O surface treatment before passivation deposition, O_2 partial pressure control to inhibit O_2

desorption on back channel, and investigating a variety passivation materials and deposition method techniques [75,81-84]. In this chapter, we investigate the characteristics of TFTs with different passivation materials and deposition methods. And then, we will optimize the characterization of PECVD SiO_2 passivation and study the mechanism of hydrogen and oxygen concentration changes during PECVD SiO_2 passivation layer.

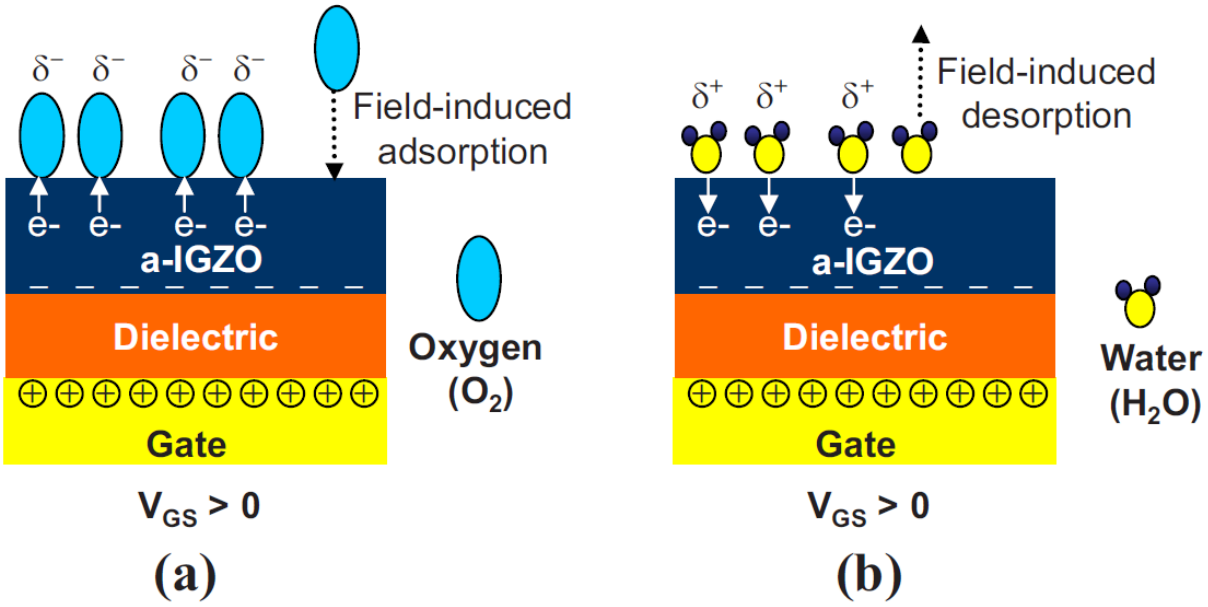


Figure 4-1. (a) Schematic showing the electric field induced adsorption of oxygen molecules from the ambient atmosphere (b) Schematic showing the electric field induced desorption of water molecules into the ambient atmosphere

Jeong et al, Applied Physics Letters, Vol. 93, Issue 12 (2008) [80]

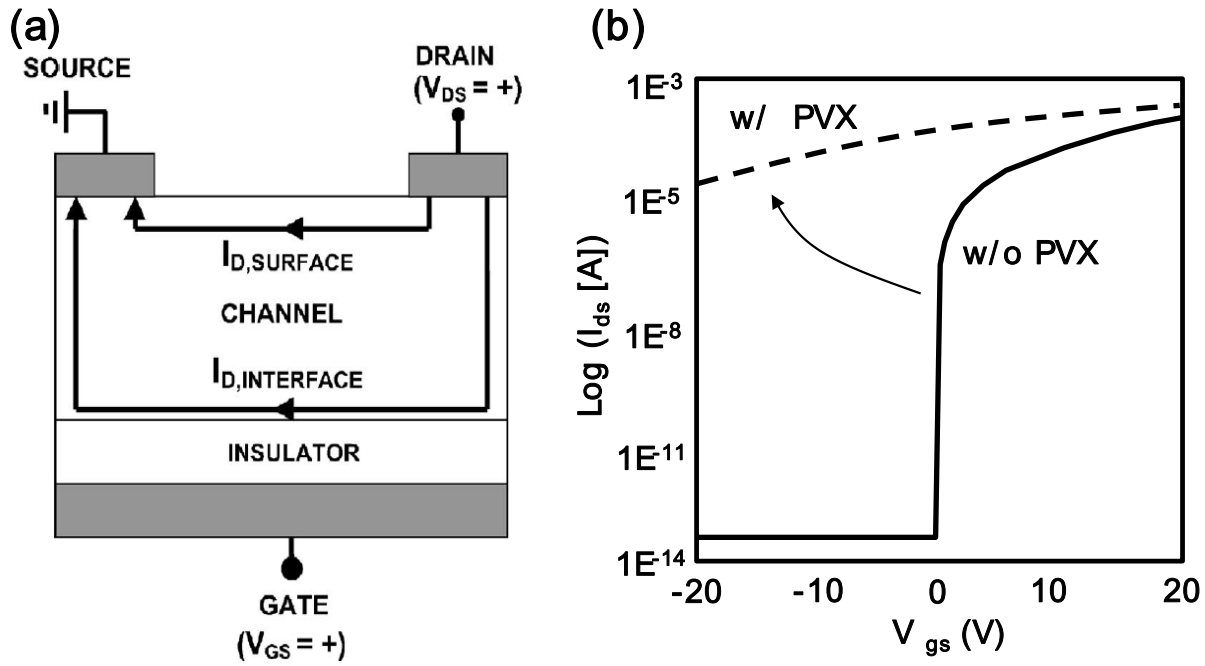


Figure 4-2. (a) Schematic showing the electric field induced desorption of water molecules into the ambient atmosphere (b) Transfer curve change before passivation layer and after passivation layer

Hong et al, AVS, Vol. 23, Issue 6, Pages L25-27 (2005) [79]

4.2 Characterization of IGZO TFTs with different passivation layer

Currently, many researchers have studied the different materials for passivation layers which are deposited by rf sputter, PECVD, and ALD (atomic layer deposition). There are many results of passivation layers in IGZO TFTs. Even though the ALD Al_2O_3 layer has a good electrical characteristic as passivation layer, this cannot apply the large sized display industry because of the size limitation of ALD system. Therefore we need to develop the sputter or PECVD passivation deposition methods, and proper materials for the passivation layer. We fabricate the common bottom gate structure IGZO TFTs, and then investigate the passivation layer properties for different materials (Al_2O_3, SiO_2, Hf_2O_3, and Y_2O_3). We prepared the low resistivity Si-wafer using the common gate, and the silicon dioxide 100nm as gate insulator grown by LPCVD. The 50nm IGZO layer is deposited by rf sputter with pO_2 40%, power 97W, and working pressure 5mTorr, and patterned by lithography process. Ti/Au (10/100nm) S/D electrodes are deposited by e-beam evaporation, and patterned by lift-off process. Figure 4-3(a) shows the cross-section structure of the samples, and Figure 4-3(b) represents the transfer curve of an un-passivated sample. All passivation layers are deposited by rf magnetron sputter using different metal sputter targets (Al, Si, Hf, and Y). For the insulator layer (oxide layer) we deposit via reactive sputtering using an $Ar + O_2$ mixture gas. Before the deposition of passivation layer, we check the hysteresis curves with oxygen amount (sccm) of each metal target and optimize the deposition condition of these passivation layers, and we use the deposition condition as shown the dash line on Figure 4-4. Table 4-1 represents the sputter condition of different passivation layers. The transfer characteristics of four kinds of passivation layers deposited by rf sputtering are shown in Figure 4-5. Al_2O_3 and Hf_2O_3 passivation layer have a good electrical property except the back-channel

effects because of ion damage during the sputter deposition. However, SiO_2 and Y_2O_3 degrade the TFT characteristics because of the passivation layer.

Table 4-2 represents the specific electrical TFT characteristics of different passivation layers. We can explain the effect on the different passivation layers and electrical property in this experiment. Even though good characteristics for Al_2O_3 and Hf_2O_3 passivation layers are observed, there are fabrication issues during the rf reactive sputtering process. Namely, nanoparticles can contaminate the devices issues, TFT size dependent characteristics, back channel current, and device. However, we find it possible to deposit passivation layers on IGZO TFTs because the low temperature process, reduced hydrogen effect, and oxygen recovery during the post annealing as will be demonstrated.

(a) Cross section structure of PVX test samples

(b) Transfer curve before PVX deposition

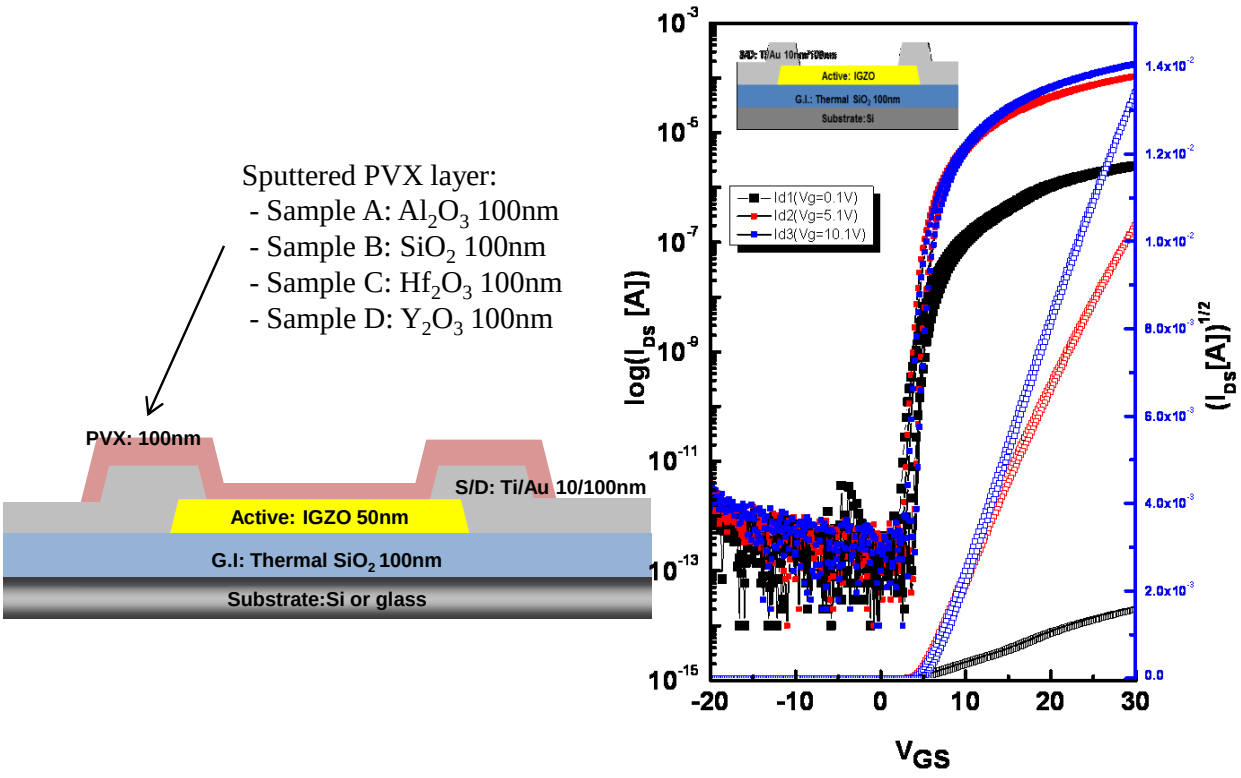


Figure 4-3. (a) Schematic structure of different passivation layer samples (b) Transfer curves of IGZO TFTs before passivation layer

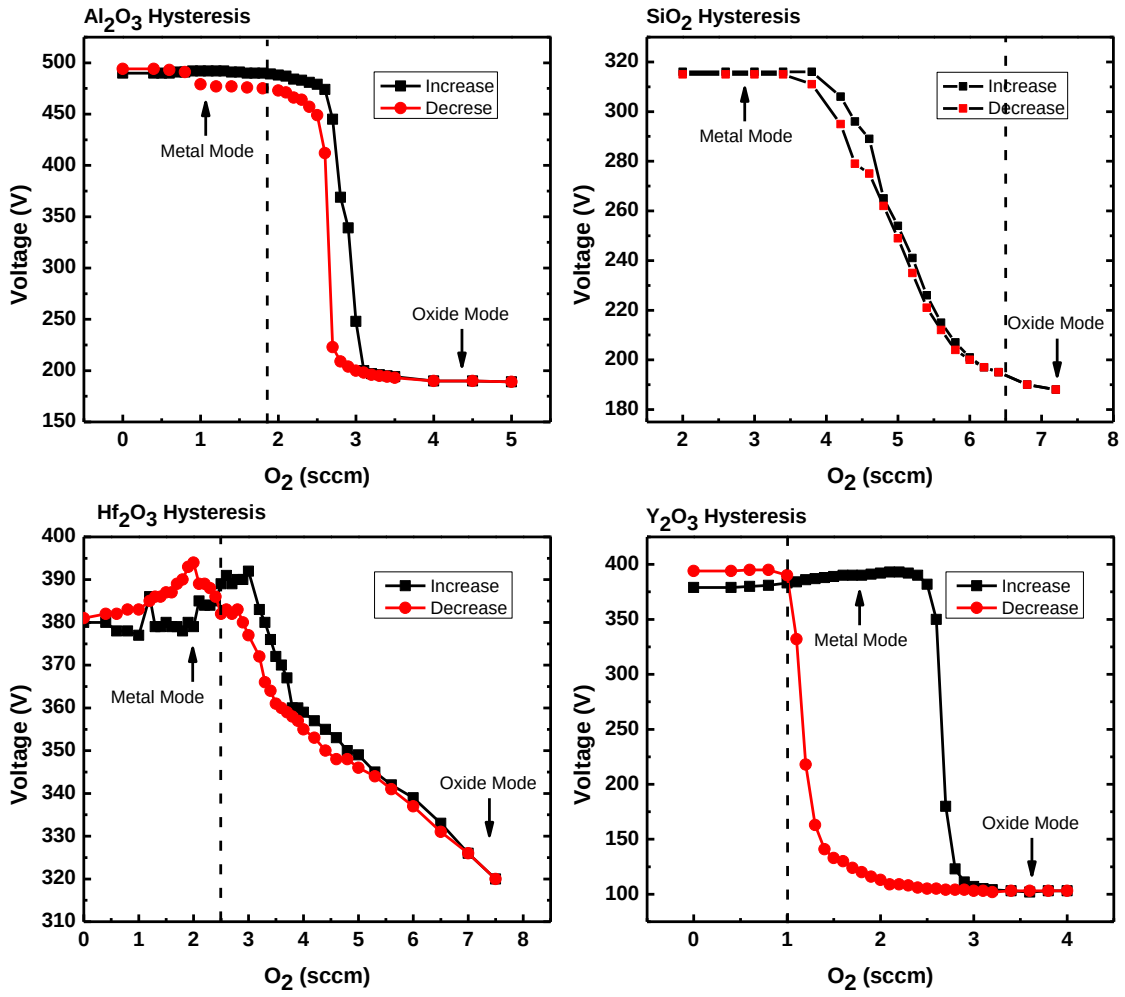


Figure 4-4. Hysteresis curves with oxygen gas flow with 4 kinds of metal sputter targets for the rf reaction sputtering

Table 4-1. The sputter deposition conditions of different passivation layer Al_2O_3, SiO_2, Hf_2O_3, and Y_2O_3

Passivation layers	RF power (W)	Ar/O_2 (sccm)	pO_2 (%)	Working Pressure (mTorr)	Time (min)	Sputter Mode
Sample A: Al_2O_3 (100nm)	150	25/1.8	6.71	5	28'38"	Metal
Sample B: SiO_2 (100nm)	200	18.5/6.5	26	5	86'12"	Oxide
Sample C: Hf_2O_3 (100nm)	200	25/2.5	9.09	5	7'48"	Metal
Sample D: Y_2O_3 (100nm)	200	25/1.0	3.85	5	9'03"	Metal

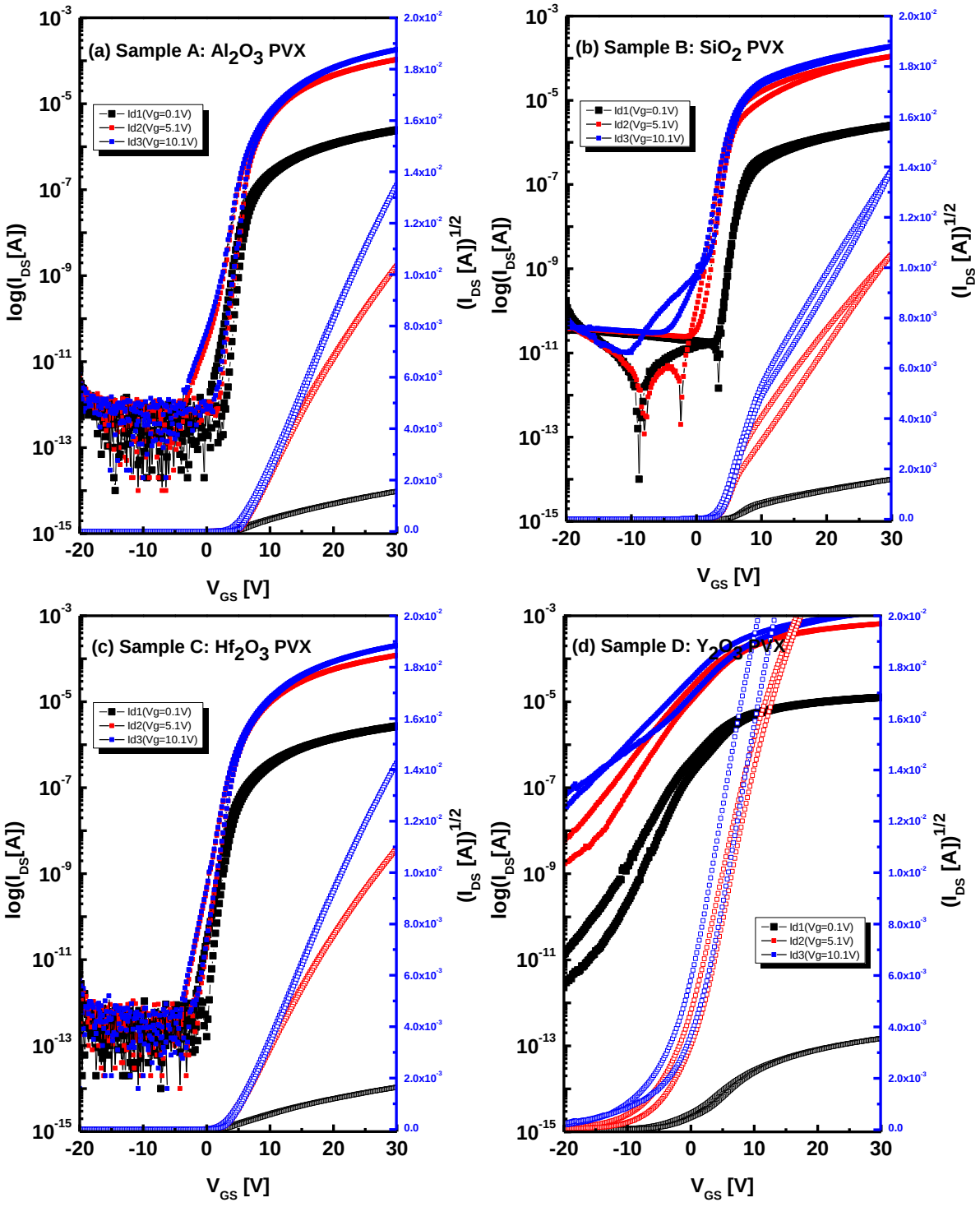


Figure 4-5. Transfer curves with different passivation layers, Al_2O_3, SiO_2, Hf_2O_3, and Y_2O_3

Table 4-2. TFT characteristics of different passivation layers, Al_2O_3, SiO_2, Hf_2O_3, and Y_2O_3

TFTs Characteristics different passivation layer	Al_2O_3	SiO_2	Hf_2O_3	Y_2O_3
Vth [V]	5.14	5.14	3.37	-8.06
S.S [V/dec]	1.81	3.39	1.39	6.52
Mobility [㎠/V·sec]	7.09	7.09	6.99	22.79
I_{on} [A]	1.8×10^{-4}	1.9×10^{-4}	2.0×10^{-4}	1.2×10^{-3}
I_{off} [A]	2.0×10^{-14}	1.0×10^{-11}	2.6×10^{-13}	1.0×10^{-6}

4.3 Characterization of PECVD SiO_2 passivation layer

From the chapter 4.1 experiment, we can attain the possibility of passivation layer if we reduce: the process temperature, sputter ion damage, and reducing the hydrogen effects. Subsequently, we investigated plasma enhanced chemical vapor deposition (PECVD) of silicon dioxide passivation layers and the In_2O_3-Ga_2O_3-ZnO (IGZO) thin film transistors are compared after N_2 and air atmosphere annealing. Thin film transistors (TFTs) using amorphous oxide semiconductors (AOSs) have attracted significant attention for large sized flat panel displays such as active matrix organic light emitting diode.[12,85] Recently we have also demonstrated active matrix lab on a chip devices using IGZO because of their high mobility, transparency and low temperature process.[86] However, a common problem encountered by IGZO TFTs is the instability of the threshold voltage (V_{th}) and reliability of TFTs characteristics after PECVD[79] and sputtered passivation layers.[75,87] In this respect, the stability and reliability of the passivation layer of AOSs are of critical importance to the realization of practical applications. The main issue is back-channel conduction in passivated AOSs; the passivation layer inhibits oxygen adsorption on the back-channel during passivation layer growth and the activated hydrogen in PECVD SiO_2 acts as a donor level and reduces the oxygen which creates a conductive semiconductor layer.[80] As is already known, low temperature PECVD SiO_2 contains high a concentration of Si-O-H as compared to that of high temperature SiO_2.[88] In addition to the different concentration of Si-O-H in the SiO_2 layer, the PECVD growth temperature also affects film properties such as stress, density and the amount of hydrogen in the film.[89] While hydrogenation of the IGZO during PECVD growth is one of main factors that affect the TFT characteristics, it is also important to understand possible hydrogenation or dehydrogenation during the final activation annealing step. To this end, it is necessary to

realize that the thermal decomposition process of Si-O-H in SiO_2 layers starts at ~ 220^{o}C.[90,91] Therefore, carrier concentration in the IGZO layer and the subsequent electrical properties of TFTs from Si-O-H decomposition in the passivation layer and diffusion of external gas ambient during post annealing process should be controlled to optimize the IGZO device properties.[65,75,92] In this study, we report the changes of hydrogen and oxygen concentration of IGZO TFTs after passivation using SiO_2 films with various hydrogen concentrations deposited by different PECVD temperatures and different post anneal atmospheres.

Figure 4-6 shows the transfer curve and structure of the bottom gate IGZO TFTs most commonly studied and reported in the literature. Before the passivation layer is deposited, the TFTs have good transfer curves having V_{th}~8.2V and subthreshold slopes are ~0.66 V/decade. The devices were fabricated on silicon wafers coated with a 500nm silicon dioxide insulating layer. A 100nm thick Cr gate electrode was deposited by RF sputter at room temperature and patterned via contact lithography and etched with a standard Cr wet chemical etchant including Ceric Ammonium Nitrate and Acetic Acid diluted by water (22% $Ce(NH_4)_2(NO_3)_6$ + 9% CH_3COOH +69% H_2O). A 100nm thick silicon dioxide gate insulator layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350℃. On top of the gate insulator, the IGZO (In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol %) active layer was RF sputter deposited at room temperature. The rf power applied to the 50mm diameter target was 97W and the working pressure was 5mTorr with the pO_2 = 40% of an Ar and O_2 gas mixture. In addition, the IGZO layer was patterned via optical lithography and etched with a 1000:1 diluted HF solution. After IGZO patterning, Ti/Au Source-Drain (S/D) electrodes were electron beam evaporated and defined via a lift-off process. Subsequent to S/D deposition, SiO_2 passivation layers were

PECVD deposited at different temperatures from 150℃ to 350℃. The common PECVD conditions were 5% SiH_4/Ar 85sccm, N_2O 157sccm, working pressure 1000mTorr, and rf power 20W. Finally, we annealed the samples in either N_2 or air ambient at 350℃ for 1hr in a furnace.

The electrical properties of the TFTs were measured using an Agilent 4156A semiconductor parameter analyzer. The refractive index of all SiO_2 passivation layers are measured by VASE Rotating Analyzer Ellipsometers (RAE) from 250nm to 1000nm wavelength. Hydrogen and oxygen concentration of both as-dep. and annealed samples for each condition were determined by Secondary Ion Mass Spectrometry.

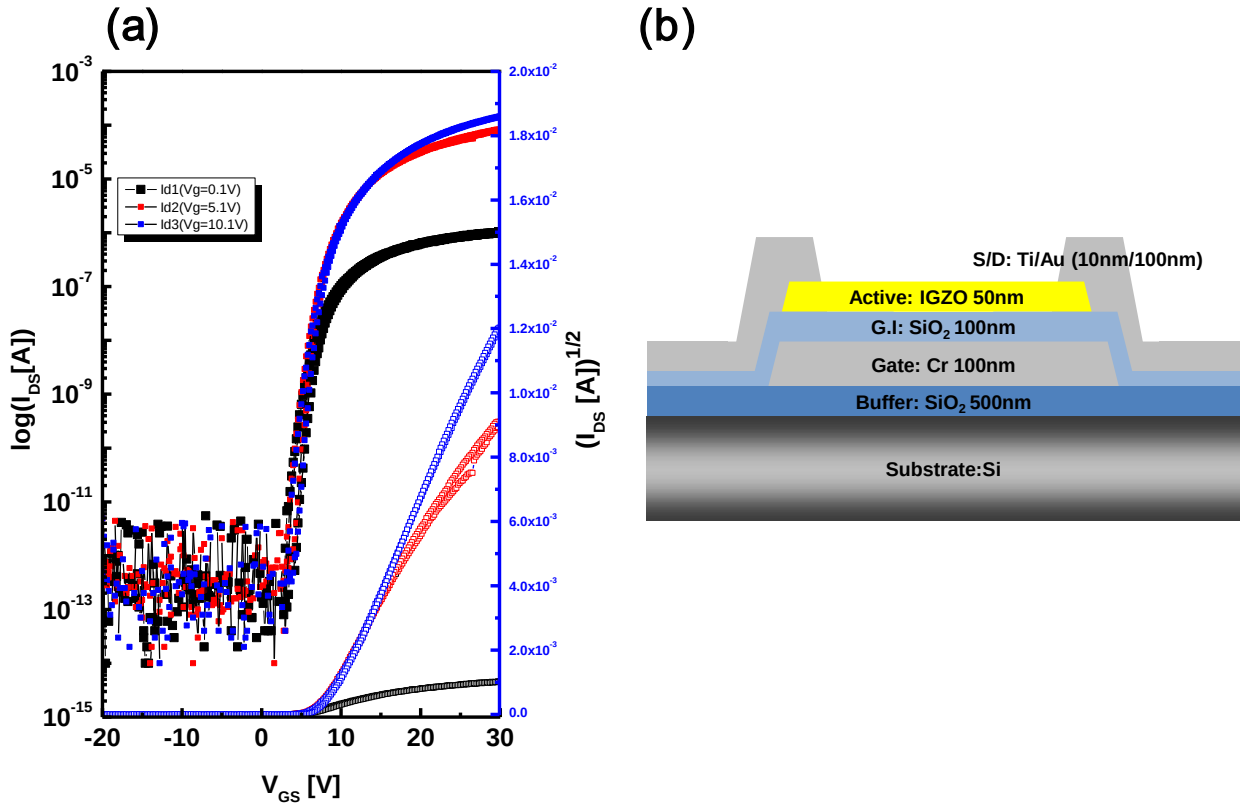


Figure 4-6. (a) Transfer characteristics of a-IGZO TFTs without passivation layer. [annealed at 350℃ N_2 1hr, TFT W/L=50/20 um, V_{DS} = 0.1, 5.1, 10.1 V], (b) Bottom gate structure of un-passivated TFTs

Figure 4-7(a) and (b) shows the transfer characteristics of the N_2 2(a) and air 2(b) annealed devices for SiO_2 passivation layers deposited at different PECVD temperature. The two different annealing atmospheres have different trends in the TFTs characteristics. For the N_2 anneal, the passivation layers deposited up to 250℃ have semiconducting properties. However, the devices with passivation layers grown above 250℃ deposition have high conductivity over the entire gate voltage range tested. On the other hand, all devices annealed in air atmosphere have good electrical characteristics with V_{th} ranges 10V~15V and $I_{on/off}$ $\sim 10^{7\sim 8}$. The N_2 annealing effects can be understood by the back channel effect as already alluded to, namely; the passivation layer prohibits oxygen and H_2O adsorption on the back channel.[93] In addition, the passivation layers contain large concentration of hydrogen from the PECVD passivation process and this has an effect on the channel layer (IGZO layer). Hydrogen in the IGZO acts as a donor and increases the concentration of carriers. However in the case of air atmosphere annealing, the devices deposited at different PECVD SiO_2 temperatures have a different tendency. In this case, the external oxygen is incorporated in the channel layer during the annealing process, and the TFT's carrier concentrations is appropriate and thus has comparatively good transistor characteristics after the passivation and anneal process.

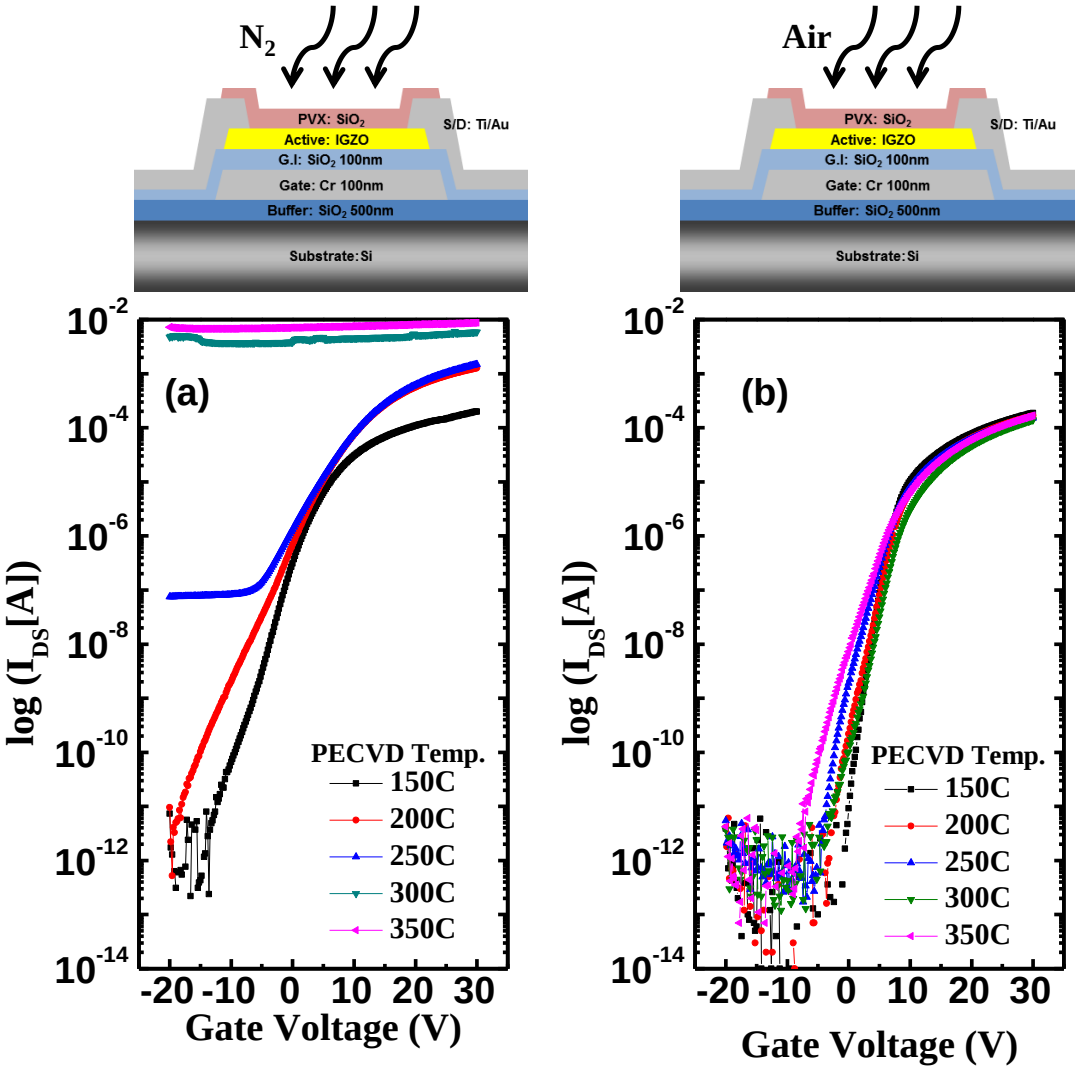


Figure 4-7. (a) Transfer characteristics of a-IGZO TFTs with different temperature PECVD SiO_2 passivation layers after N_2 350℃ 1hr. (b) Transfer characteristics of a-IGZO TFTs with different temperature PECVD SiO_2 passivation layers after air 350℃ 1hr. [TFT size W/L=50/20um, V_{DS}=10.1V

Figure 4-8 shows the schematic diagram to explain the origin of hydrogen and oxygen effects after passivation layer and different atmospheres annealing. We studied two mechanisms to explain cumulative effect of the passivation layer and anneal. One contribution is the internal interaction such as hydrogenation and oxygen absorption during PECVD passivation deposition and the other is external interaction such as dehydrogenation and oxygen absorption through the passivation layer during the post annealing step. The amount of hydrogenation and oxygen adsorption were affected by the PECVD passivation growth temperature. The SiO_2 films deposited at low temperature contain more Si-O-H (Silanol) and water and are less dense than films deposited and grown at high temperatures. The role of the PECVD SiO_2 passivation layer may change the concentration of hydrogen and oxygen in the IGZO active layer.

After growth and during the annealing step, hydrogen in the as-deposited PECVD SiO_2 passivation can diffuse into the IGZO layer. Specifically, during the passivation deposition and annealing step Si-O-H is converted to Si-O and Si-O-Si with by-products such as H_2O, H^+, O^{2-} .[88,89,94] These by-products result from decomposition of Si-O-H in the PECVD SiO_2 layer, which can subsequently affect the total channel layer carrier concentration induced by hydrogen and oxygen.

Based on the annealing results, SiO_2 passivation layers (grown at 150C~350C via PECVD) are apparently sufficiently permeable during the 350℃ annealing step, and the permeation of ambient external gas (O_2 or N_2) is related to film density. Table 4-3 reveals the refractive index

measured by ellipsometry and film density extracted by the Lorentz-Lorenz equation from the refractive index. The Lorentz-Lorenz equation is expressed as

$$\Pi = \frac{1}{3} N_A \alpha = \frac{n^2-1}{n^2+2} \frac{M}{\rho}, \quad (4.1)$$

where Π is the molar poralization of SiO_2 (7.4797cm^3/mol), M is the molecular mass of SiO_2 and (60.08g/mol).[95] As demonstrated and as expected, the film density of SiO_2 passivation layers increased as deposition temperature increased. This suggests that the high temperature deposited SiO_2 layer is denser than that of low temperature, and therefore less permeable to the ambient (O_2, N_2) during the annealing step.

In real devices, two mechanisms as mentioned above work concurrently to control the TFTs characteristics. In case N_2 annealing, the total carrier densities of IGZO channel layer increase the amount of diffused H_2 or H^+ during passivation deposition and oxygen out-diffusion during post annealing. The oxygen out-diffusion is related to the passivation film density where lower out-diffusion occurs at higher passivation growth temperatures. On the other hand, for the air annealed samples, total carrier densities of IGZO channel layer compensates the amount of diffused in H_2 or H^+ during passivation and amount of absorbed external O_2 gas during the annealing process. As PECVD temperature increased, the film density of SiO_2 passivation layer varied from 2.28 g/㎤ at 150℃ passivation to 2.32 g/㎤ at 350℃.

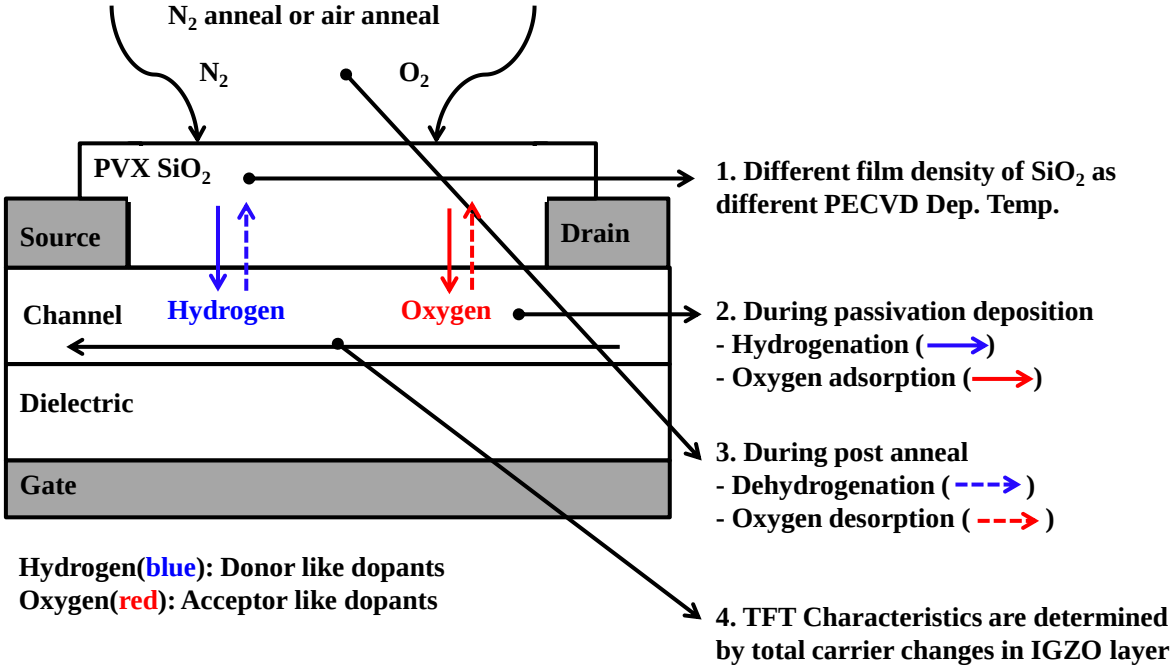


Figure 4-8. Schematic summary of the interaction mechanism between PECVD passivation layer and IGZO active layer before and after annealing step in the IGZO TFTs. Solid arrows represent as-dep passivation, dash- arrows represent after post annealing.

Table 4-3. Summarization refractive indexes (n) collected at 600nm wavelength and film densities of passivation PECVD SiO_2 layer of a-IGZO TFTs.

Passivation PECVD Temp (℃)	As-Deposition	
	n	ρ (g/cm^3)[a]
150	1.48165	2.28852
200	1.48594	2.30592
250	1.49014	2.32288
300	1.49094	2.3261
350	1.49092	2.32599

[a] ρ is extracted by Lorentz-Lorenz equation, $\Pi = \frac{1}{3} N_A \alpha = \frac{n^2-1}{n^2+2} \frac{M}{\rho}$, substituting the following values; M (molecular mass of SiO_2) = 60.08g/mol, Π (molar polarization of SiO_2=7.4797cm^3/mol)

Figure 4-9 shows the depth profile of the hydrogen concentration and oxygen intensity (arbitrary units) using Secondary Ion Mass Spectroscopy (SIMS). We investigate the change in the hydrogen concentration and the changes in the intensities of oxygen, silicon, zinc, and gallium before and after N_2 and Air annealing. Indium was omitted in our SIMS analysis as we were focused on the accuracy of the hydrogen concentration (low mass elements). Figure 4-9(a) illustrates the concentrations of the above elements for as deposited SiO_2 passivation layers grown at 150℃ and 350℃. Figure 4-9(b) and (c) show the concentration changes of hydrogen and the intensity changes of oxygen before and after N_2 and air annealing. After PECVD SiO_2 deposition, the concentration of hydrogen increases from $1.99x10^{21}$ atom/cm^3 in the initial IGZO film to $2.5x10^{21}$ atom/ cm^3. On the other hand, the intensity of oxygen strongly depends on the PECVD deposition temperature and ranges from $1.805X10^{-1}$ in initial oxygen value to $4.0X10^{-1}$ and in case of 150℃ SiO_2 layer and 2.0 $X10^{-1}$ in 350℃ SiO_2 layer. After post N_2 and air annealing, hydrogen and oxygen diffuse out from the IGZO layer and yields different hydrogen concentrations and oxygen content. Because hydrogen and oxygen vacancies are both donor levels in IGZO, The total carrier concentration contributed to IGZO TFTs characteristics was estimated by

$$n_{total} = n_{initial} + \Delta n_{Hydrogen} - 2\Delta n_{Oxygen} \ , \tag{4.2}$$

$$n_{total} = n_{initial} + \Delta n_{tc,\ total\ carrier\ change} \ , \ \Delta n_{tc} = \Delta n_{Hydrogen} - 2 \times \Delta n_{Oxygen} \ , \tag{4.3}$$

$$\Delta n_{tc,\ total\ carrier\ change} = \frac{\Delta n_{hydrogen}}{n_{hydrogen,initial}} - 2 \times \frac{\Delta n_{oxygen}}{n_{oxygen,initial}} \ , \tag{4.4}$$

Where: n_{total} is the total carrier concentration of the channel layer; $\Delta n_{Hydrogen}$ is the hydrogen concentration change; and $2 \times \Delta n_{Oxygen}$ is the oxygen concentration change. In equation (4.4), we can normalize the change of concentration divided by the initial values to extract the change of relative hydrogen and oxygen concentrations from SIMS concentration data.

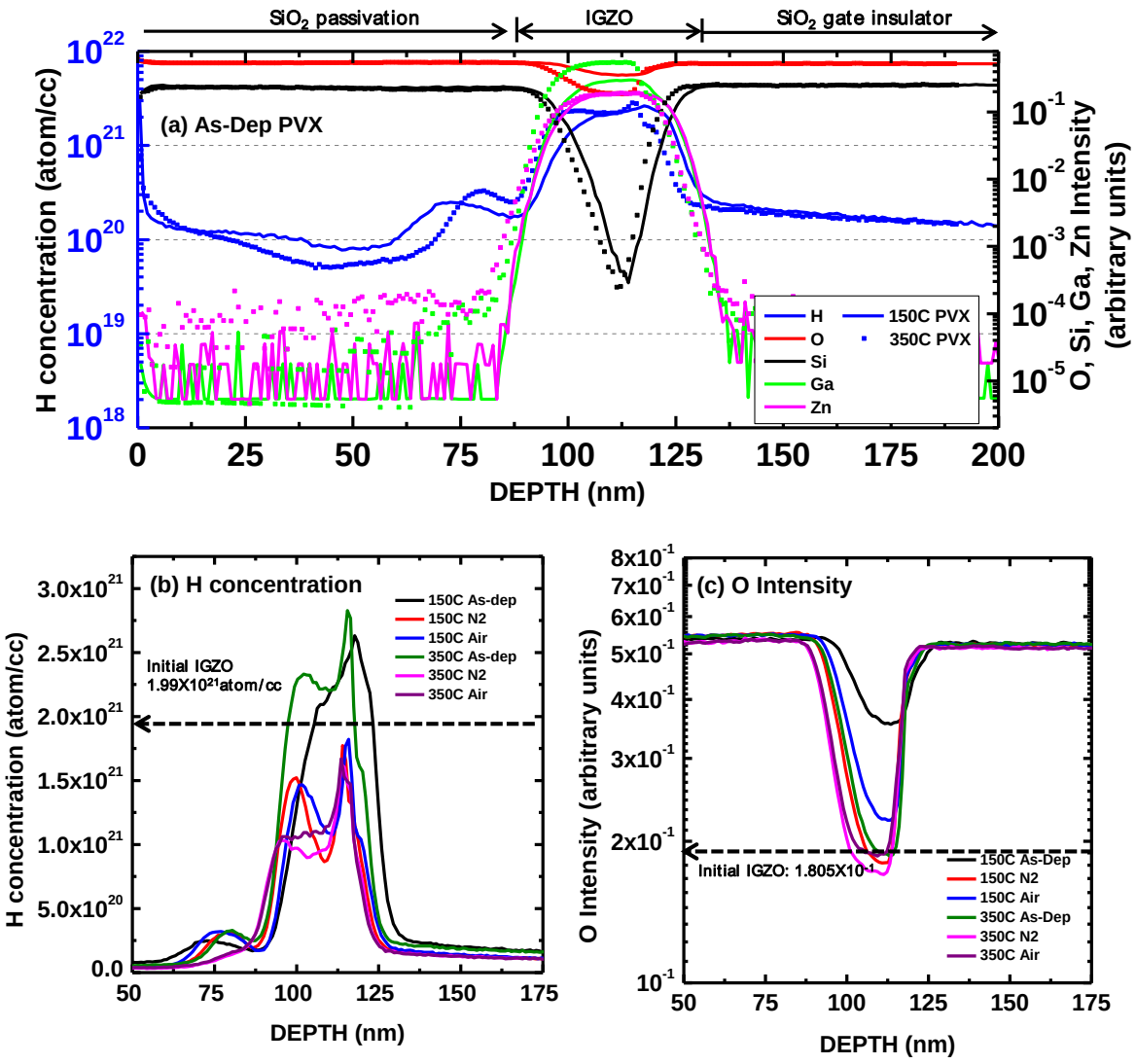


Figure 4-9. TOF-SIMS depth profiles of different SiO_2 films deposited by PECVD (a) as-deposited samples at PECVD 150C and 350C, (b) hydrogen concentration of different SiO_2 films in different annealing atmosphere (c) oxygen intensity of different SiO_2 film in different annealing atmosphere

To illustrate the correlations, Figure 4-10(a) show the initial hydrogen concentration, hydrogen concentration after passivation or post annealing process and normalized concentration change ratio of hydrogen, $n_{H,ini}$, $n_{H,after}$ (left axis) and $\Delta n_H/n_{H,ini}$ (right axis). As the same method, the oxygen intensity represents $n_{O,ini}$, $n_{O,after}$ (left axis) and $\Delta n_O/n_{O,ini}$ (right axis) in the show Figure 4-10(b). In Figure 4-10(c), the normalized concentrations of hydrogen and oxygen ($\Delta n_H/n_{H,ini}$ and ($\Delta n_O/n_{O,ini}$) are compared on the left axis, and we can attain the total carrier change ratio ($\Delta n_{t.c}$) on our IGZO TFTs with different passivation condition and post annealing atmosphere from equation 4-4. Figure 4-10(d) represents the correlation of the I_{DS} at V_g=0V of IGZO TFTs and the total carrier change parameter $\Delta n_{t.c}$. The value of $\Delta n_{t.c}$ is strongly related with TFTs characteristics whether the TFTs had appropriate switching behavior or not. In case of working TFT samples, Δn_{tc}values are from -1.0 to -0.7 and I_{DS} values at V_{GS}=0V are from 10^{-10} to 10^{-5}[A]. However, the device having Δn_{tc}< -1.0 and > -0.7 have un-activated (low I_{DS}) properties in the whole gate bias region, conversely, and were effectively metallic or shorted devices with I_{DS} > 10^{-3}[A] depends on the hydrogen and oxygen concentration changes.

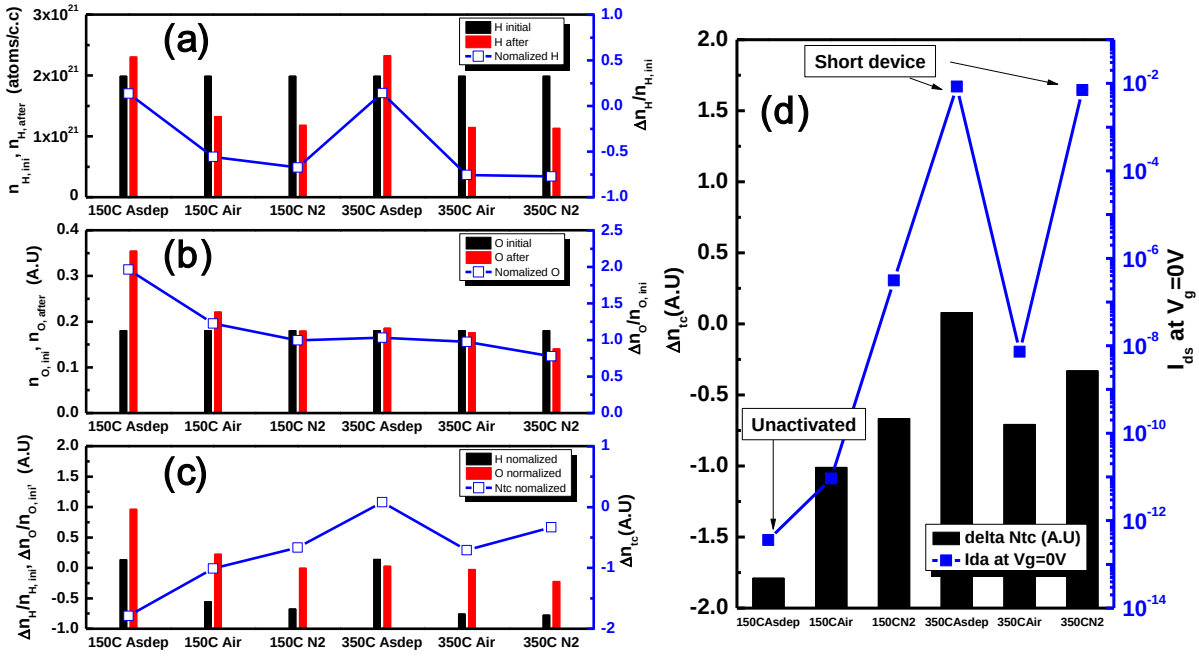


Figure 4-10. Compare the concentration of hydrogen and oxygen with initial and after passivation or post annealing (a) hydrogen concentration, (b) oxygen intensity, (c) total carrier change ratio ($\Delta n_{tc,\ total\ carrier\ change}$), and (d) compare total carrier change and I_{DS} [A] at V_{GS} = 0V in different passivation and post annealing samples

4.4 Conclusion

In summary, we investigate the change of electrical characteristics with the different passivation layers and different deposition method of passivation layer. Al_2O_3 and Hf_2O_3 passivation layer deposited rf magnet sputter have a good electrical properties. However, we need good uniformity on the whole wafer area, and fabrication issues during sputter deposition for high resolution full integrated TFTs electrowetting devices. From this passivation layer test we find the possibility of passivation layer of IGZO TFTs because the low temperature process, reduce the hydrogen effect, and oxygen recovery during the post annealing. In the PECVD SiO_2 passivation test, the investigations on the effects of hydrogen and oxygen concentration revealed that the carrier concentration of IGZO channel layer was changed with passivation layer and external oxygen during post annealing. To attain the good characteristics TFTs after SiO_2 passivation layer we should control total carrier concentration which is affected by density of passivation layer, passivation temperature, and post annealing atmosphere. Therefore, we would provide a feasible mechanism of PECVD passivated IGZO TFTs and realize lots of applications of IGZO TFTs. In addition, these mechanisms of passivation layer would be expected to descript the reliability and stability issues of IGZO TFTs.

Chapter 5

Preliminary Electrowetting Basic Test

5.1 Introduction

In this chapter we study the basic electrowetting tests which overviews wetting phenomena with and without biased voltage, electrowetting droplet actuation of simple electrode structures, compares conventional and Laplace barrier EWOD device in which a post array is patterned on the top plate to hold the droplets in the off-state, and splitting on different size electrodes on our EWOD device. This preliminary test will provide basic concepts to drive electrofluidic devices of our fully integrated TFT electrofluidic device.

5.2 Electrowetting phenomena experiment

The planar substrate is usually a hydrophobic (Fluoropel) surface with dielectric layer and an electrode buried underneath. In the absence of external electric fields, the liquid droplet has a large contact angle called the Young's angle (θ_Y). θ_Y is a characteristic of the conductive liquid, air ambient and the hydrophobic (Fluoropel) surface. In figure 5-1(a), there are three interfacial surface tension vectors (γ_{WO}, γ_{OF}, γ_{WF}) at the triple phase contact that determines θ_Y, where γ_{WO} is the water/oil interfacial surface tension, γ_{OF} is the Fluoropel/oil interfacial surface tension, and γ_{WF} is the water/Fluoropel interfacial surface tension. These surface tension vectors are related to θ_Y by

$$\gamma_{WO}\cos\theta_Y + \gamma_{WF} = \gamma_{OF}, \tag{5.1}$$

Subsequent to an applied voltage, the Young's angle (θ_Y) can be electromechanically reduced

to a new contact angle projection (θ_V) as shown in Figure 5-1(b) [96]. The applied voltage causes the liquid to conduct charges to the liquid-dielectric interface establishing strong non-uniform electric fields between the charges in the liquid phase and the dielectric underneath near the triple phase contact. From the non-uniform electric fields the electromechanical force on the liquid is reduced the contact angle projection (θ_V) of the liquid. This electromechanical force per unit length (F_{em}) acts in direction to γ_{OF} and is added to the three interfacial surface tension vectors as:

$$\gamma_{OF} - \gamma_{WO} \cos\theta_v = F_{em} + \gamma_{WF} \cdot F_{em} = \frac{\varepsilon\varepsilon_0}{2d} \cdot V^2, \tag{5.2}$$

The net effect of all the interfacial surface tension forces and the electromechanical force on θ_V can be expressed by the electrowetting equation

$$\cos\theta_v = \cos\theta_Y + \frac{\varepsilon\varepsilon_0}{2d\gamma_{WO}} \cdot V^2, \tag{5.3}$$

where V is the applied voltage, ε is the relative electric permittivity of the hydrophobic dielectric, ε_0 is the permittivity of free space and d is the thickness of the dielectric.

Figure 5-2 represents the schematic diagram for the basic electrowetting tests: a) directly connected power supply on the sample, b) connect to a MOSFET on the sample, and c) connect the In_2O_3 TFT on the sample. The bottom plate sample prepared 0.1um ITO electrode, Paylene-C 1μm or Paylene-F 0.3μm coated with 0.05μm Fluoropel as the hydrophobic layer. Firstly, the directly connected sample has the contact angle changed when we applied the voltage of 85~110V for Parylene-C 1um and 40~50V for Parylene-F 0.3um layer. This is a reversible process, the droplet exhibits are reduced contact angle on the dielectric and hydrophobic layers

when we applied the voltage, and when the applied voltage removed, the droplet changes back to the original state as shown Figure 5-2 pictures. With the MOSFET connected, the resistance and capacitance of electrowetting device are ~200MΩ and ~100pF. This RC time is very important factor to drive the active addressing methods to hold the signal during the off-state signal. In this case, we simulated the simple structure with PSPICE simulators. The R_{on} at V_g 12V, V_d=40V and R_{off} of MOSFET are ~0.7Ω and 2.222MΩ, respectively. Figure 5-3 represents the simple circuit structure and the change of the RC time with resistance of electrowetting device. At the R=200MΩ, C=100pF of electrowetting device when we make 2.5msec of gate on pulse and 2.5msec of duration time at V_d=40V and V_g=12V, the RC time is around 0.5msec. In addition, when we decrease R=2kΩ of electrowetting device, RC time decreased 0.1msec. The RC delay is decreased with the resistance of electrowetting resistance. Resistance and capacitance of electrowetting device depend on the dielectric layer, hydrophobic layer, and electrode pad size.

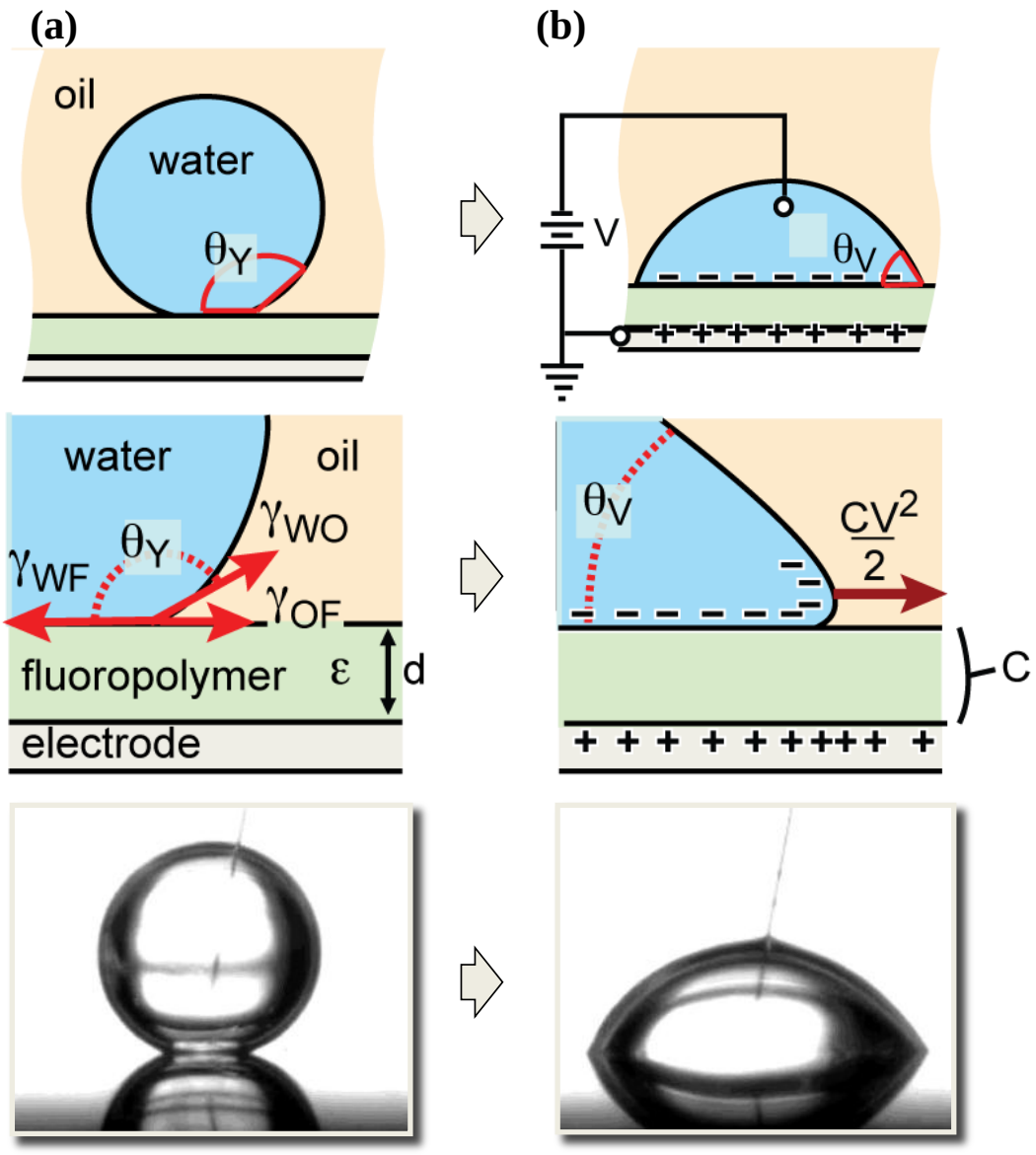


Figure 5-1. Three interfacial surface tension (a) with un-biased, (b) with biased

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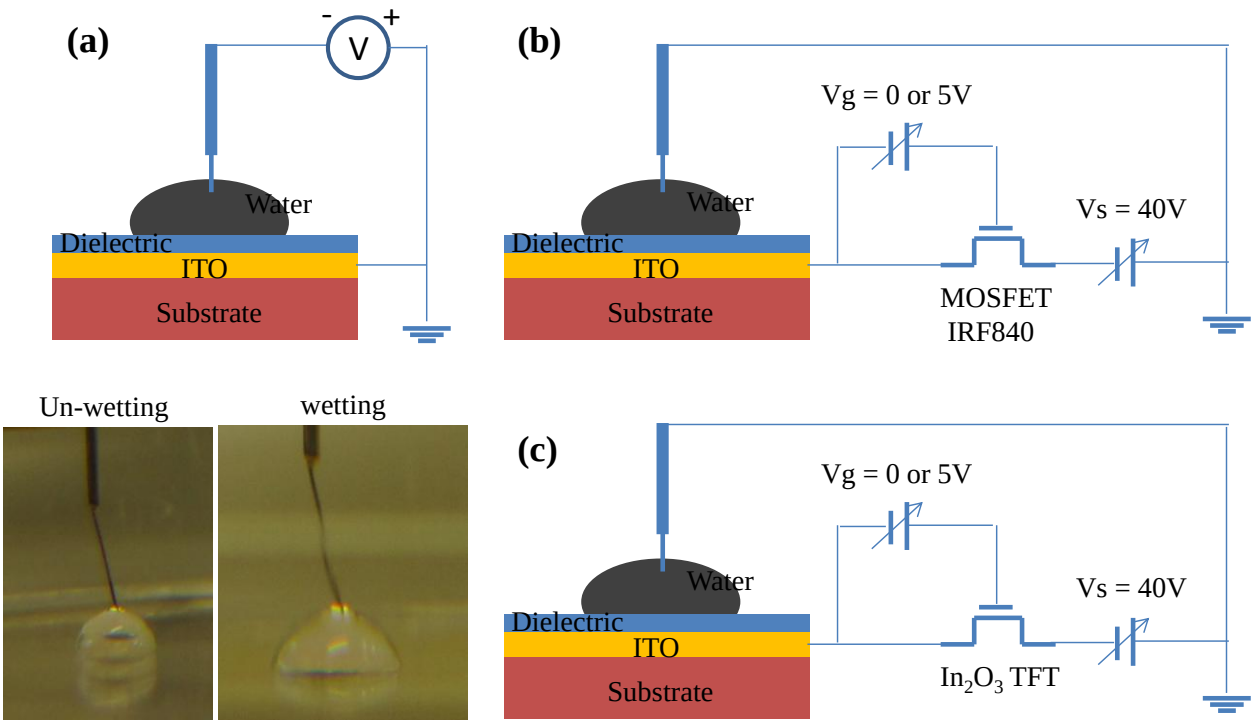
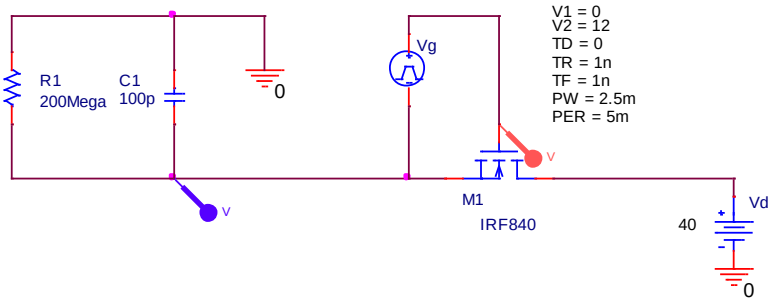
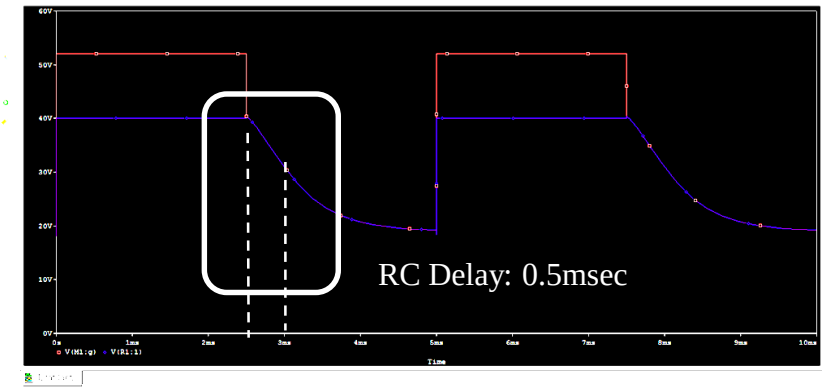


Figure 5-2. The schematic basic electrowetting test system (a) Direct connect with Power supply, (b) MOSFET (IRF840), (c) In_2O_3 TFT

(a) Simple circuit diagram of electrowetting device



(b) RC delay time at R=200MΩ, C=100pF of electrowetting device with 2.5msec pulse signal on Vg



(c) RC delay time at R=2kΩ, C=100pF of electrowetting device with 2.5msec pulse signal on Vg

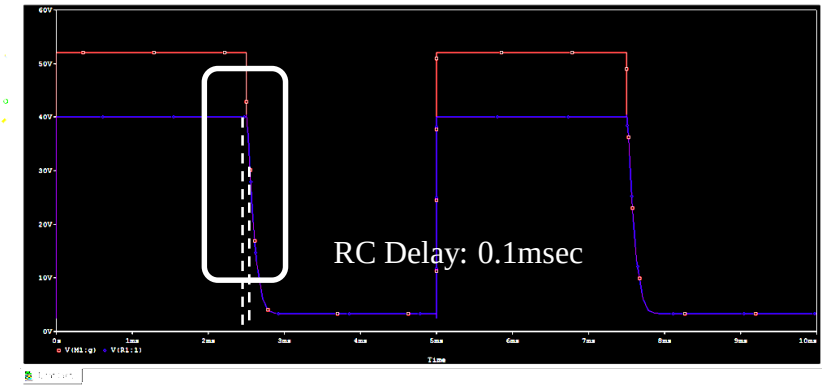


Figure 5-3. (a) The circuit diagram of electrowetting device, (b)-(c) The RC delay at 200MΩ and 2kΩ of electrowetting device in Pspice simulation

For the connection of the In_2O_3 TFT of this simple electrowetting device, In_2O_3 TFTs were fabricated on the common gate of a p-type Si, and gate insulator thermal SiO_2 100nm grown by LPCVD, and Ti/Au (10nm/100nm) S/D electrodes evaporated by e-beam evaporation. This In_2O_3 TFT has -10V off-state and 0V in on-state, and the drain current of each state are 10^{-12} A and 10^{-5} A as shown Figure 5-5. As the TFT is turned on and off state, the wetting angle projection (θ_V) is reduced according the applied voltage. In this experiment, we apply 40V to the drain electrode to change the wetting angle of the liquid. Figure 5-4 demonstrates electrowetting device and the simple circuit diagram with In_2O_3 TFTs as the switching devices which is connected source and gate in the probe station. The liquid is wetting on the V_d=40V and V_g=0V (on-state), and return to the original dewetting state V_d=0V or V_g=-12V. In this experiment In_2O_3 TFT works well as switching device in our electrowetting device. For additional understanding of electrowetting device and active matrix addressing we have studied the RC time relation of electrofluidic device, the frequency of V_G, and duty ratio for driving electrowetting device. We will investigate this relation on chapter 6 in this dissertation.

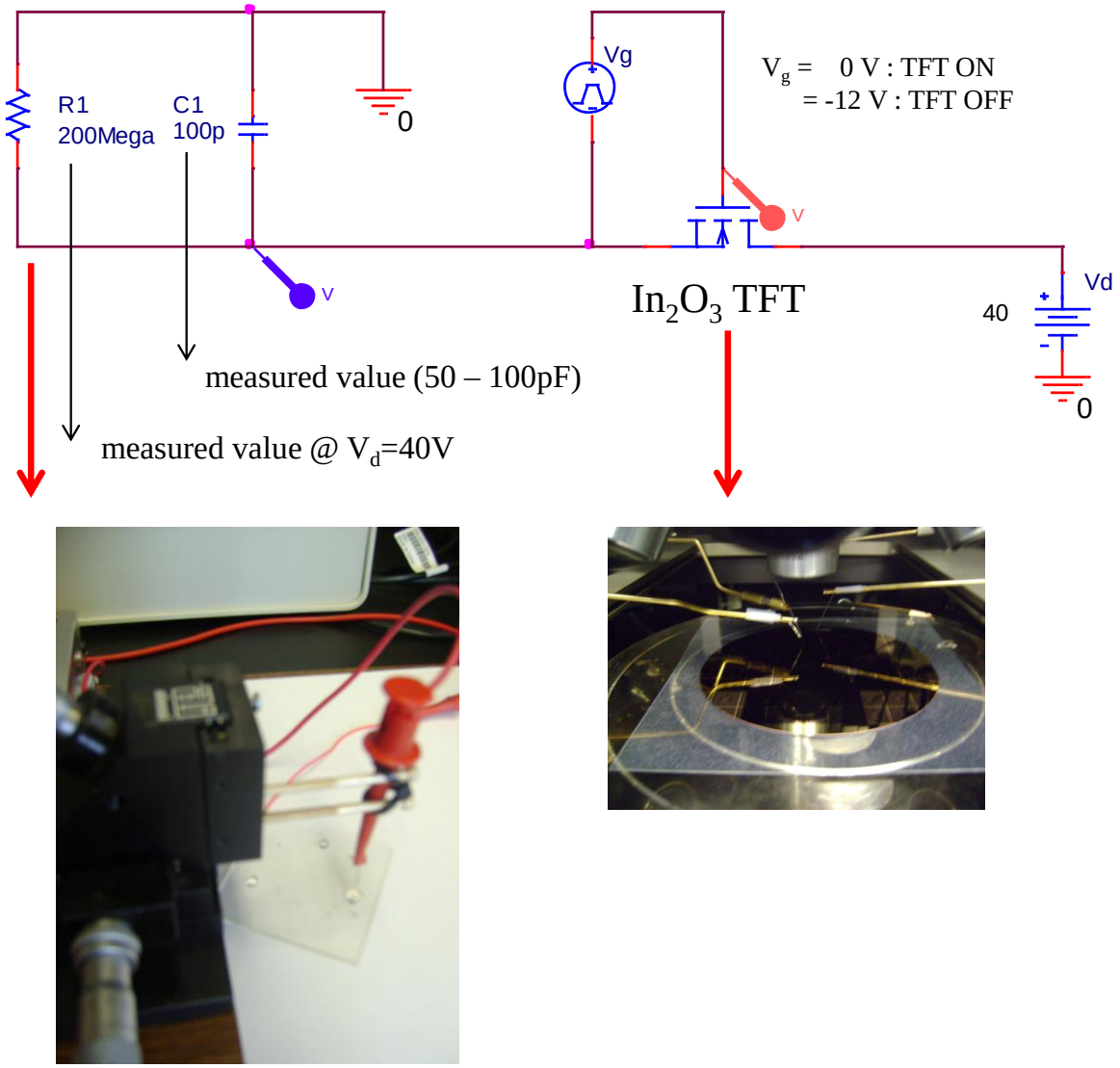


Figure 5-4. The experiment set up for electrowetting test using In_2O_3 TFT

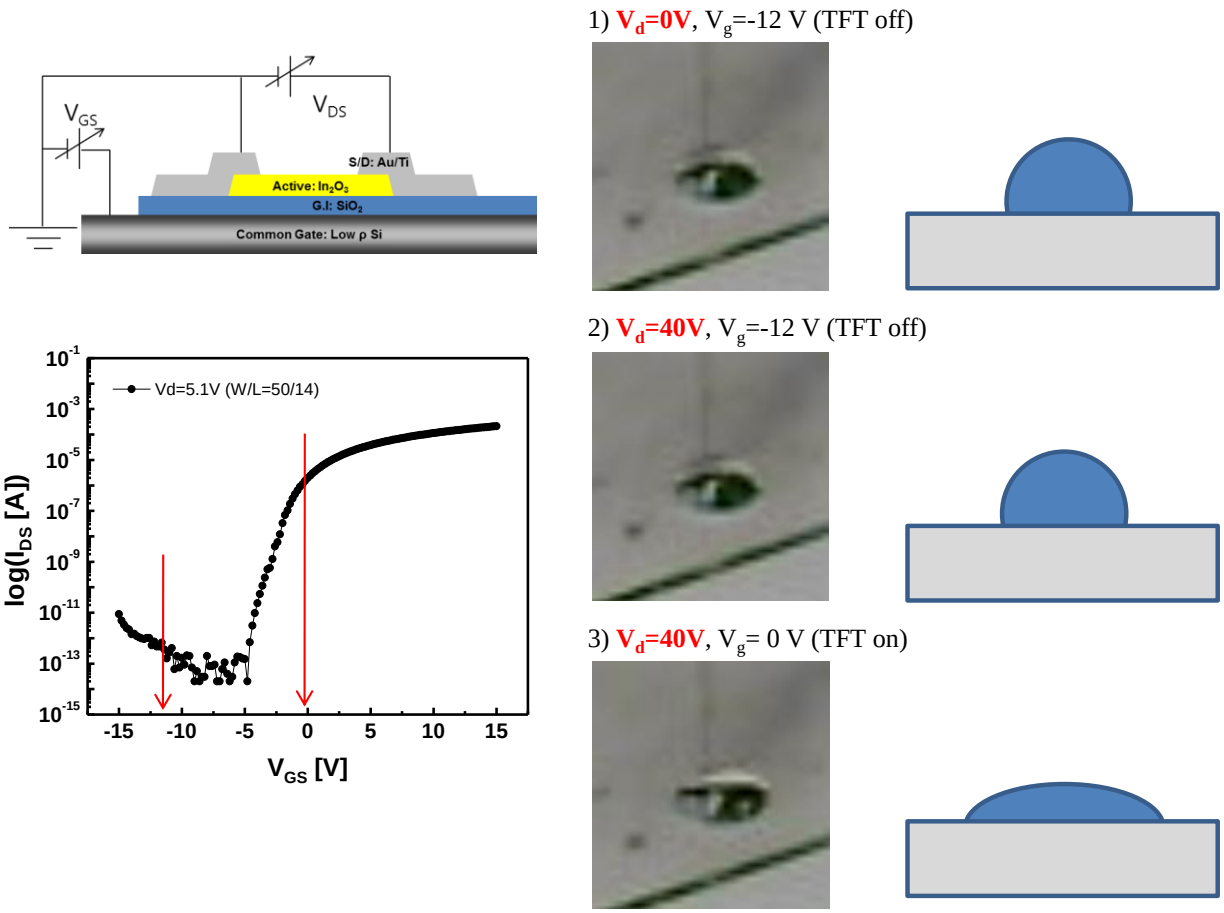


Figure 5-5. The In_2O_3 TFT characteristics and the electrowetting phenomena test 1) TFT-off state (V_g = -12V) with V_d = 0V, 2) TFT-off state (V_g=-12V) with V_d=40V and 3) TFT-On state (V_g=0V) with V_d=40V

5.3 Droplet actuation in simple electrode structure

The principle of electrowetting based droplet actuation is descripted in Figure 5-6. Application of an electric field on the bottom side of the droplet creates an imbalance of net pressure which drives bulk flow of the droplet. The top plate contains a single continuous ground electrode while the bottom plate contains two independently addressable control electrodes. The electrode size and droplet volume are designed such that when a droplet is centered upon an electrode it slightly overlaps all adjacent electrodes as well. The top electrode is coated with a thin Fluoropel polymer layer to make it hydrophobic. The bottom electrode is coated with a two layer dielectric stack for electrowetting control (SiO_2 dielectric & Fluoropel polymer). Without bias state, Figure 5-6(a), the droplet stays at Young's contact angle (θ_Y), and is balanced by Young-Laplace pressures at the front and back side water/oil interfaces:

$$P_f = P_b = \gamma_{WO} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2}\right), \tag{5.4}$$

where P_f and P_b are front and back Young-Laplace pressures respectively, γ_{WO} is water/oil interfacial surface tension, and R_1 and R_2 are the principle radii of curvature of the water/oil interface. A typical liquid channel has a channel height h<<droplet diameter d. Therefore, Young-Laplace pressure in this channel is dominated by only a single radius of curvature R. With oil ambient, the Young's contact angle θ_Y is >160^o, and R can be further approximated as being only due to the channel height (R~h/2). P_f and P_b can then be simplified to:

$$P_f = P_b \approx \frac{2\gamma_{WO}}{h}, \tag{5.5}$$

To actuate the droplet movement, a voltage is applied to the front electrode while the back electrode and top electrode are both connected the ground state. The bottom contact angle at the front water/oil interface is then reduced to θ_V because of the electrowetting effect. Therefore, the radius of curvature R is increased $R \approx \frac{h}{2\frac{\epsilon\epsilon_0}{2d\gamma_{WO}}\cdot V^2}$, where $\frac{\epsilon\epsilon_0}{d\gamma_{WO}}$ is the hydrophobic dielectric capacitance per unit area, and the applied voltage is indicated by V. A net pressure imbalance is created by this radius of curvature increase. The front pressure P_f is reduced to $\frac{2\gamma_{WO}}{h} - \frac{\varepsilon\varepsilon_0}{2dh}\cdot V^2$. The net pressure acting on the droplet can be approximated as

$$\Delta P = P_b - P_f \approx \frac{\varepsilon\varepsilon_0}{2dh}\cdot V^2, \tag{5.6}$$

This net pressure imbalance ΔP is the driving force for movement the liquid droplet. When the electric field is removed, the bottom contact angle will return to Young's angle θ_Y and the net pressure ΔP will be balanced to zero. Therefore, the droplet will be static again.

Figure 5.7 shows the 5 electrodes with Parylene-C/Fluoropel coating sample from University of Cincinnati. This sample consists of100nm Al electrodes on a glass substrate and covered with Parylene-C 1μm / Fluoropel 0.05μm. When we apply the 90V~110V on the each electrode, the droplet starts to actuate and move to other 5 electrodes of the device. In this experiment we encounter the problem for driving the droplets such as high driving voltage due to thick dielectric layer (1um Parylene C) and not suitable hydrophobic layer (Fluoropel), and contact problems between electrodes. Despite these problems, we succeeded to demonstrate the actuation of droplets through the all 5 electrodes in our device.

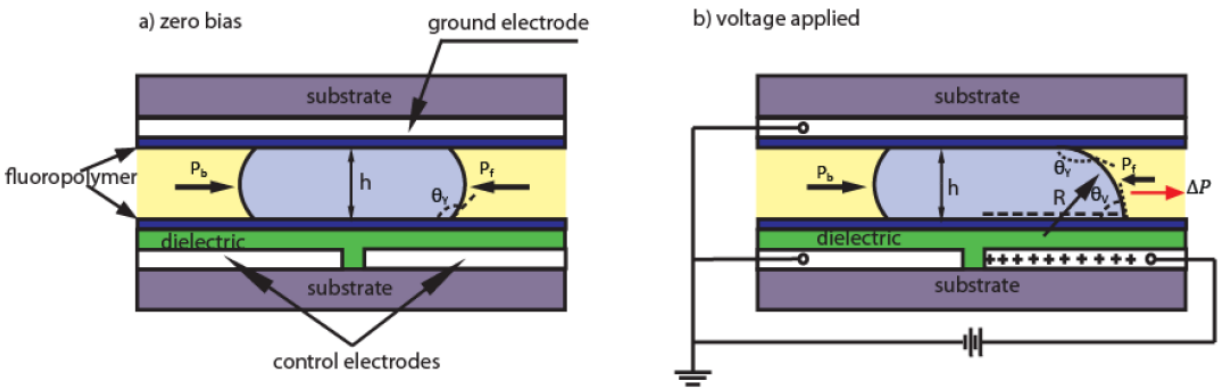
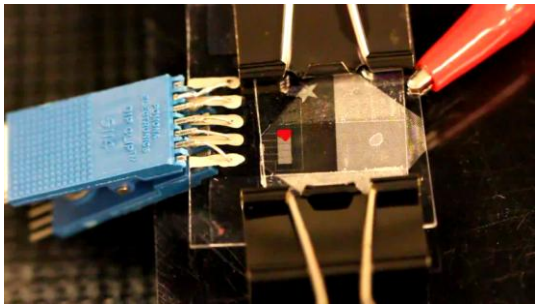


Figure 5-6. Schematic cross-section of electrowetting droplet actuation (a) zero bias, (b) voltage applied

(a) Sample assembly



(b) Sample information

- Electrode: Al 100nm
- Dielectric layer: Parylene-C 1um
- Hydrophobic layer: Fluoropel 0.05um
- Pigment: 10wt% red pigment with 0.01% of sodium lauryl sulfate
- Oil: Dow Corning OS-30
- Gap Height: 120um

(c) Actuation sequence of droplets

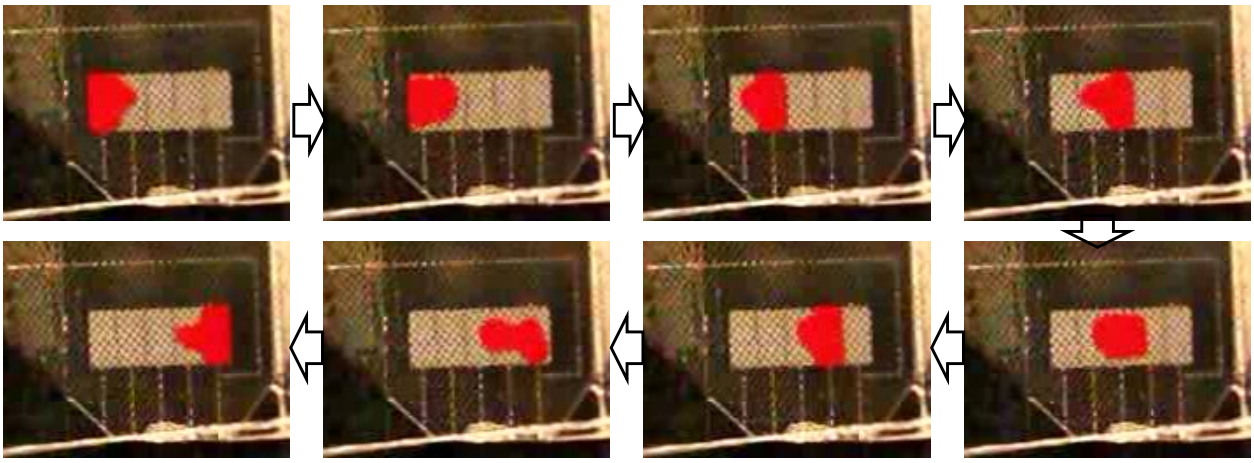


Figure 5-7. 5X1 electrodes with Parylene-C/Fluoropel coating sample from University of Cincinnati. The droplet actuation voltage is 90~110V.

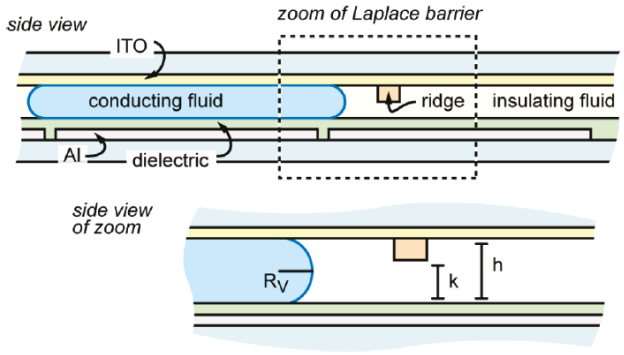
5.4 Conventional electrowetting microchannel & Laplace barriers electrowetting

In this section, we investigate the functionality of electrowetting devices with conventional planar top-plates and so-called Laplace barrier devices. Laplace barriers can be easily adapted to any conventional electrowetting microchannel device but enhance device function by virtually confining the fluid [97]. We apply the type of Laplace barrier which relies on the influence of Laplace pressure in the vertical plane. Figure 5-8 shows the schematic cross section structure, SEM image and effects on the electrowetting difference when we turn off the applied voltage. When we apply the voltage on the electrode, there are no difference between conventional electrowetting and Laplace barrier electrowetting. However, when we turn off the applied voltage, Laplace barrier electrowetting maintains the electrode shape by the Laplace barrier pressure. When we applied voltages on the electrode (at the limit of stability), the pressure acting on the conducting fluid can be expressed as

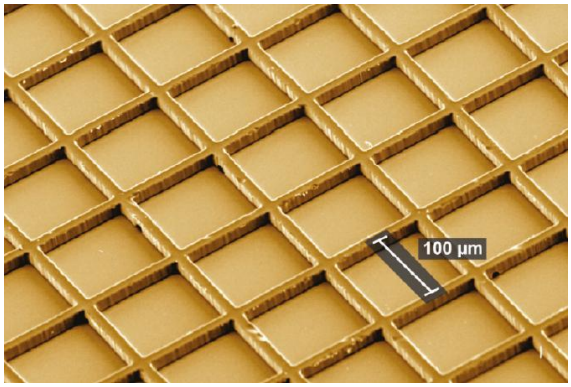
$$\Delta p \cong \gamma_{ci}(2\ \ h-1\ \ k), \tag{5.7}$$

where Δp is Laplace pressure, $\gamma_{ci}$is the surface tension between conducting liquid and insulator, *h* is the gap height, and k is the barrier height of Laplace post.

(a) Cross-section structure



(b) SEM image of vertical Laplace barriers



(c) Conventional Electrowetting



(d) Laplace barrier electrowetting



(e) Illustration of arrayed Laplace barrier

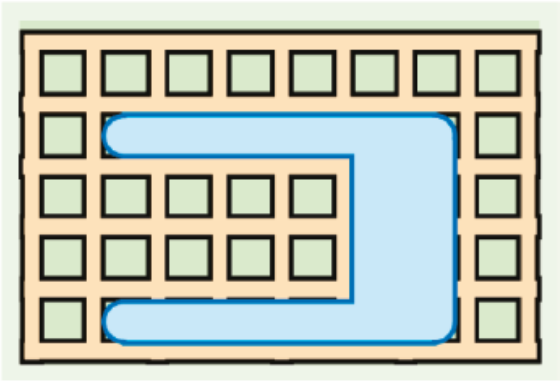


Figure 5-8. (a) Schematic cross section of Laplace barrier electrowetting device (b) SEM image of vertical Laplace barrier on top plate (c) Conventional Electrowetting not to maintain the shape without applied bias (d) Laplace barrier electrowetting holding the shape without applied bias (e) Illustration of arrayed Laplace barrier

Kreit et al, Langmuir, 26, 23, 18550~18556 (2010)

Figure 5-9 shows the mask layout of 2×5 electrowetting sample and picture of our sample. Each of the electrodes has a 2.54mmx2.54mm size separated 50μm with neighbor electrode. In the region of electrode separation the overlapping area between the electrodes is 150μm. The electrodes again were 100nm Al deposited by e-beam evaporation, and the dielectric layer is 200nm SiO_2 deposited by PECVD. After the SiO2 coating, a hydrophobic layer was dip-coated to 0.05μm thick, and finally, we anneal the sample at 195℃ 30min on the hot plate. In this study, we can measure the droplet moving time using video analysis method (1frame = 1/30sec) with post and without post sample on the top plate. Figure 5-10 represents the actuation of droplet with post and without post sample, and the electrode pitch size is 2.54mm. To reduce the experiment error depend on the device status like hydrophobic, surface contamination of external atmosphere, and degradation the dielectric properties of driving time, we investigate the each electrodes for moving, and choose the 3 electrodes for the best moving performance nearby each other.

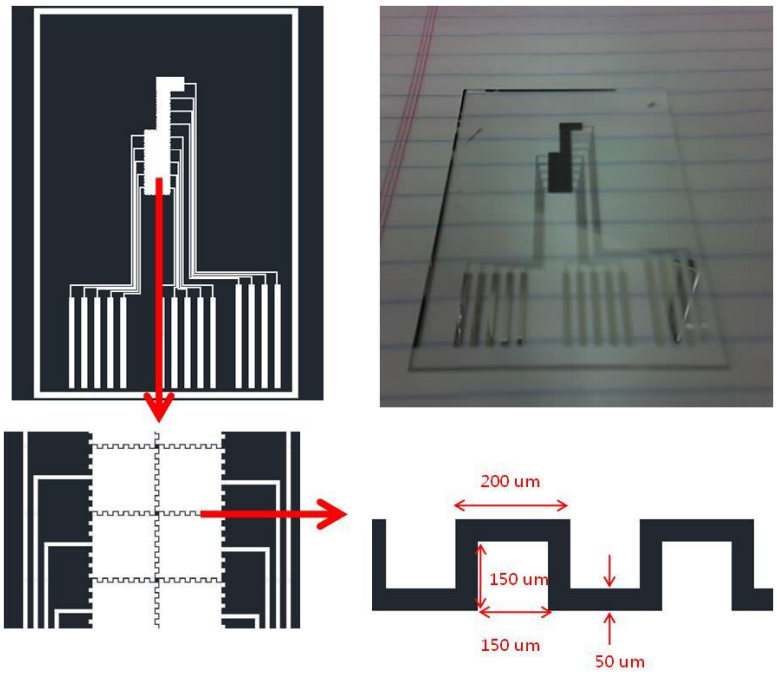


Figure 5-9. Mask layout of 2×5 electrowetting device, and sample picture

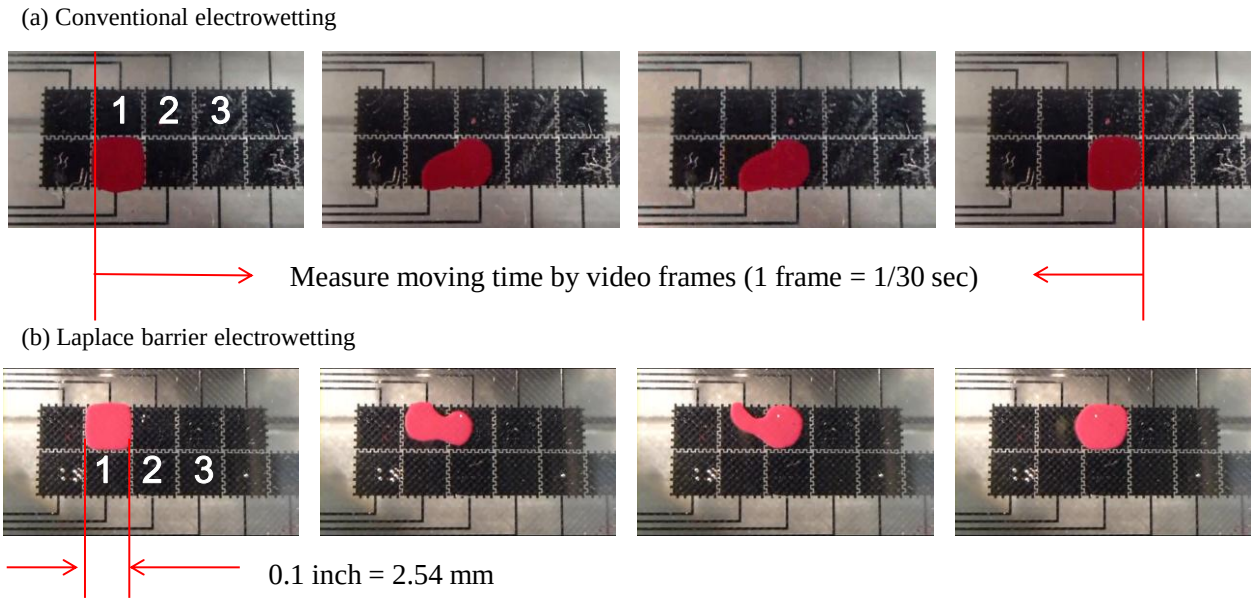


Figure 5-10. The actuation of droplet without post (conventional electrowetting) and with post (Laplace barrier electrowetting)

Figure 5-11 represents the moving time of the droplet with an applied voltage with conventional and Laplace barrier electrowetting samples. We categorize the number of electrode to reduce the other effects such as defect on the surface, state of hydrophobic layer, and difference of gap height which is very sensitive the droplet moving speeds. In case of conventional electrowetting device, the actuation of droplet is working on 20V. However, the Laplace barrier electrowetting device works at slightly higher voltage -- 26~27V. The threshold voltage difference for actuation of droplet is due to surface tension and Laplace barrier of the post array. Both of the samples reduce the duration time with increasing the applied voltage. We can calculate the moving speed which is based on the electrode pitch size divided duration time (mm/sec). The sample without post have from 0.6mm/sec at 20V to 8.5mm/sec at 50V, also the sample with post have from 0.5mm/sec at 26V to 6mm/sec at 50V. The number of graph (for example 1-2) represents the moving direction of liquid droplet from electrode 1 to electrode 2. Figure 5-12 shows the comparison between the conventional electrowetting device and Laplace barrier electrowetting device which has the post on the top plate. Figure 5-12(a) and (b) show the moving time and speed of droplet (from 2^{nd} electrode to 3^{rd} electrode) as function of the applied voltage. In the case of the conventional device the moving speed is slightly faster than that of the Laplace barrier device at the same applied voltage due to the difference of threshold voltage to actuate the liquid droplet. Hereby, the threshold voltages of the conventional and Laplace barrier devices are extracted ~18V and ~26V on both devices, respectively. The difference of threshold voltage is around 8V to actuate the liquid droplet. Figure 5-12(c) and (d) demonstrate the moving time and speed versus the subtraction from applied voltage to threshold voltage.

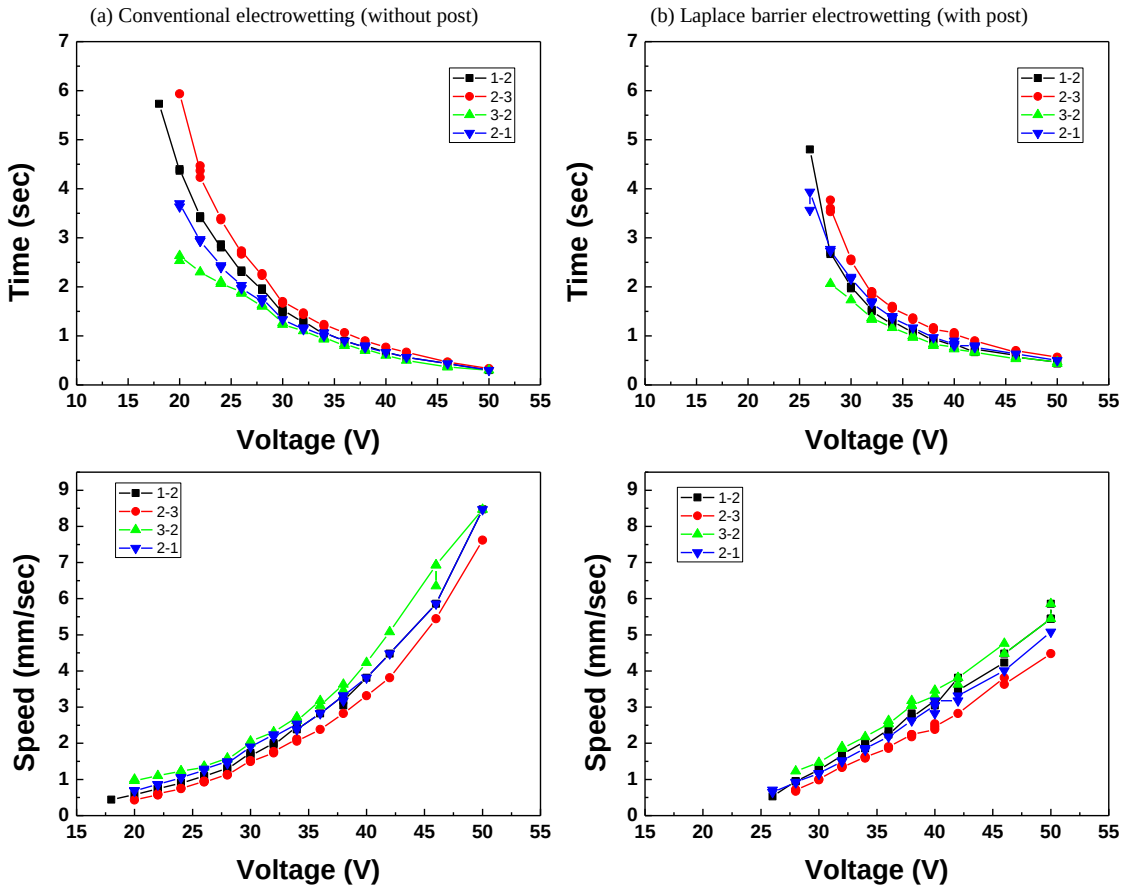


Figure 5-11. The moving time of droplet with applied voltage and the moving speed of droplet with applied voltage (a) Conventional electrowetting (without post), (b) Laplace barrier electrowetting (with post)

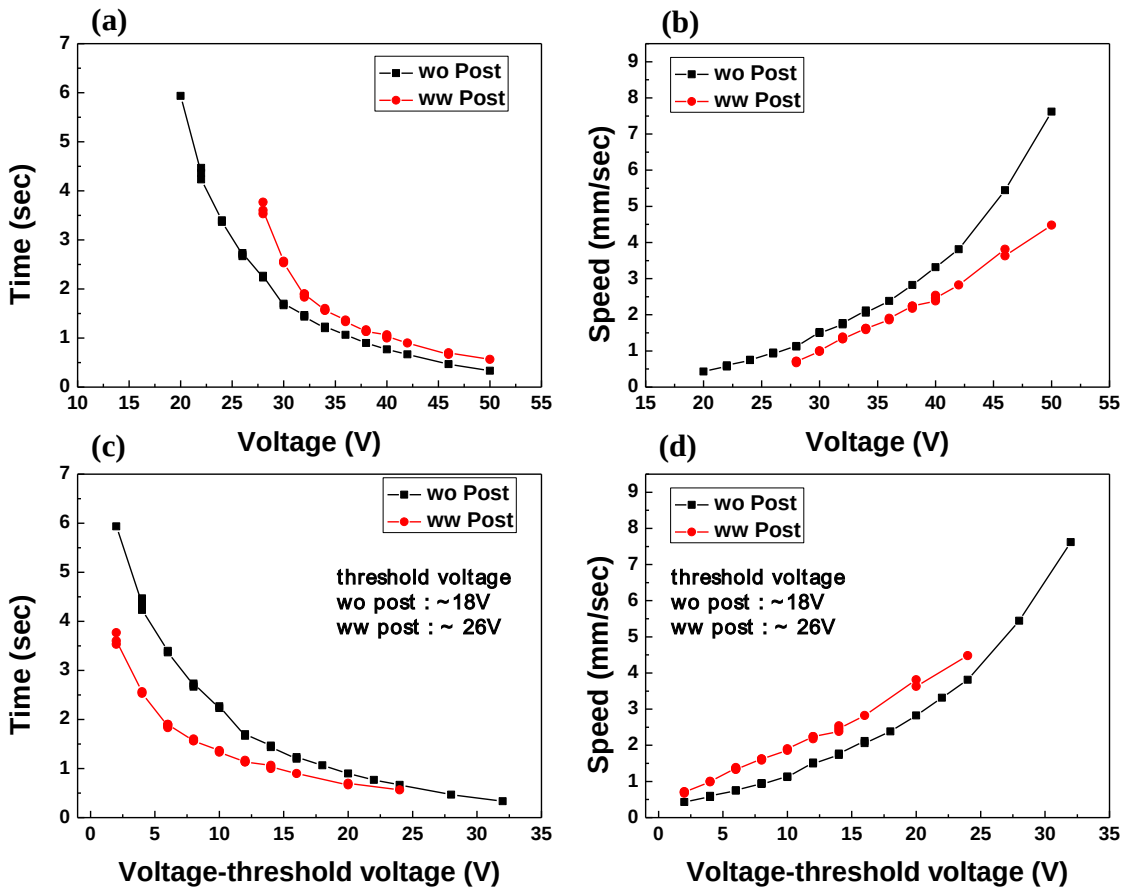


Figure 5-12. The moving time and speed between 2nd electrode to 3rd electrode, relation of threshold voltage with post and without post samples

5.5 Split the different size electrodes

In this section, we check the possibility of splitting the droplets between the different size electrodes. In the LOC device, this split properties is important functionality to extract the small amount of droplet from a reservoir system having large amount of liquid. The liquid droplet transporting mechanisms have already reported by Cho et al, in university of California, Los Angeles [3]. To split the liquid droplet, the droplet is elongated in the longitudinal direction by making the two ends wetting and keeping the middle nonwetting. Figure 5-13 shows the schematic diagram of droplet splitting mechanism and relation between the contact angle and gap height of electrowetting device. The main factors of droplet splitting are shown as:

$$\frac{R_2}{R_1} = 1 - \left(\frac{R_2}{d}\right) \cdot \frac{\epsilon_0 \epsilon V_d^2}{2\gamma_{WO} t}, \tag{5.8}$$

where R_1 and R_2 are the radius of droplet when the cutting is initiated by necking in the middle of the droplet and the radius of droplet at the end of region. d is the gap height on this channel, and V_d is the applied voltage. $\frac{\epsilon_0 \epsilon}{t}$ is the dielectric constant and thickness of dielectric layer. In other words, the function of the splitting the droplet is affected by the amount of liquid and electrode size related the droplet radius, applied voltage, surface tension between water and oil, and gap height. Figure 5-13(d) represents the splitting condition where R_1 is negative (necking is created), the system have $d/R_2 < 0.22$ condition which corresponds $d < 154\mu m$ for 1.4mm × 1.4mm electrodes. In our experiments we can make different size electrodes (1mm, 500μm, 250μm, and 100μm) to control the droplets. Figure 5-14 shows the mask layout of our different sized electrowetting device. We deposit the Al electrode (100nm) using e-beam evaporation on glass substrate, and patterned by lift-off process. The dielectric layer was 200nm SiO_2 deposited

by PECVD. The hydrophobic layer (Fluoropel) was dip-coated to ~with 0.05μm, and final annealing take 350℃ 1hr in air atmosphere. Also the top plate is used by ITO (100nm) coated glass and hydrophobic layer coating (same as bottom plate condition). To maintain the gap height between bottom and top plate we can use the microslide having 120um thickness. Figure 5-15 represents the actuation moving of two different sized droplets (1mm and 500μm), we can attain the moving speed of two droplets by changing the signal speed of applied voltage. In 20V applied voltage, two droplets initiate the actuation of movement from 100msec scanning signal. When we decrease the time of scanning signal down to 50msec, the droplet of 1mm size cannot arrive at the next electrode to complete the movement. However, the 500μm droplet is easy to arrive and follow the 50msec scanning signal. We investigate the moving speed between two size droplets, and both two droplets have ~10mm/sec moving speed in this sample. There is no difference of moving speed of electrode size. Figure 5.15(b) represents the process of splitting in different sized electrode. At first, we turn on the electrodes 3^{rd}, 4^{th} row electrodes from the bottom electrodes to elongate the droplet. After that, we turn-off the 2^{nd} row electrode, the necking is initiated on droplet. Finally, we turn-on the 5^{th} raw electrode and turn-off 3^{rd} raw electrode, the splitting of droplet is completed. However, we cannot successfully split droplets with electrodes smaller in size than the 500μm electrodes because of the gap height dependence of splitting. In small electrodes, we need the small gap height to split the liquid droplet as already mentioned before.

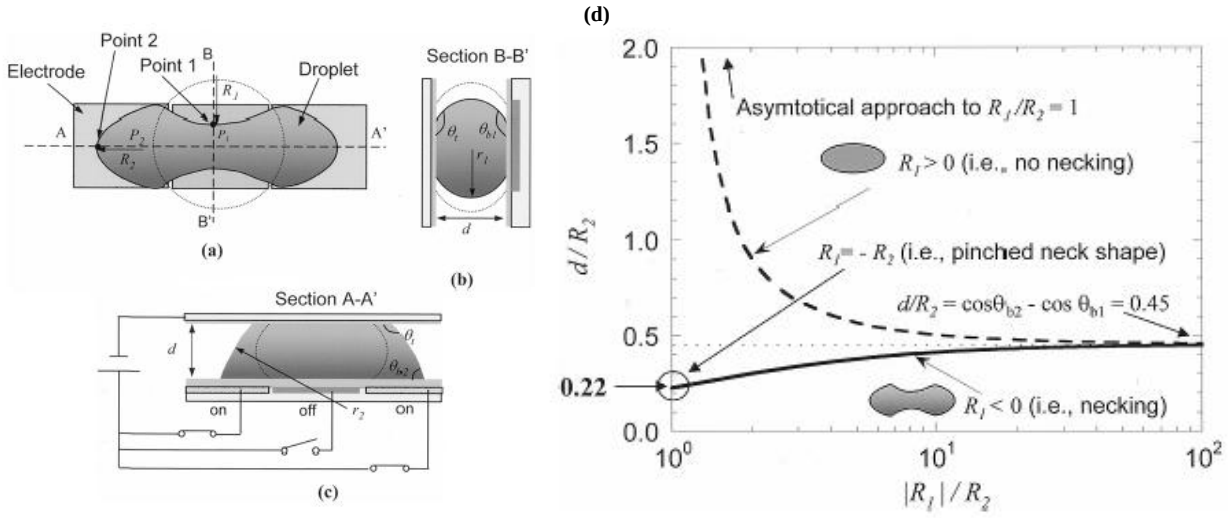


Figure 5-13. Droplet configuration for splitting. (a) Top view, (b) Cross-sectional view B-B'. (c) Cross-sectional view A-A'. (d) The relation splitting factors with menisci, contact angle, gap height in splitting

Cho et al, Journal of Microelectromechanical system, vol 12, no 1, (2003)

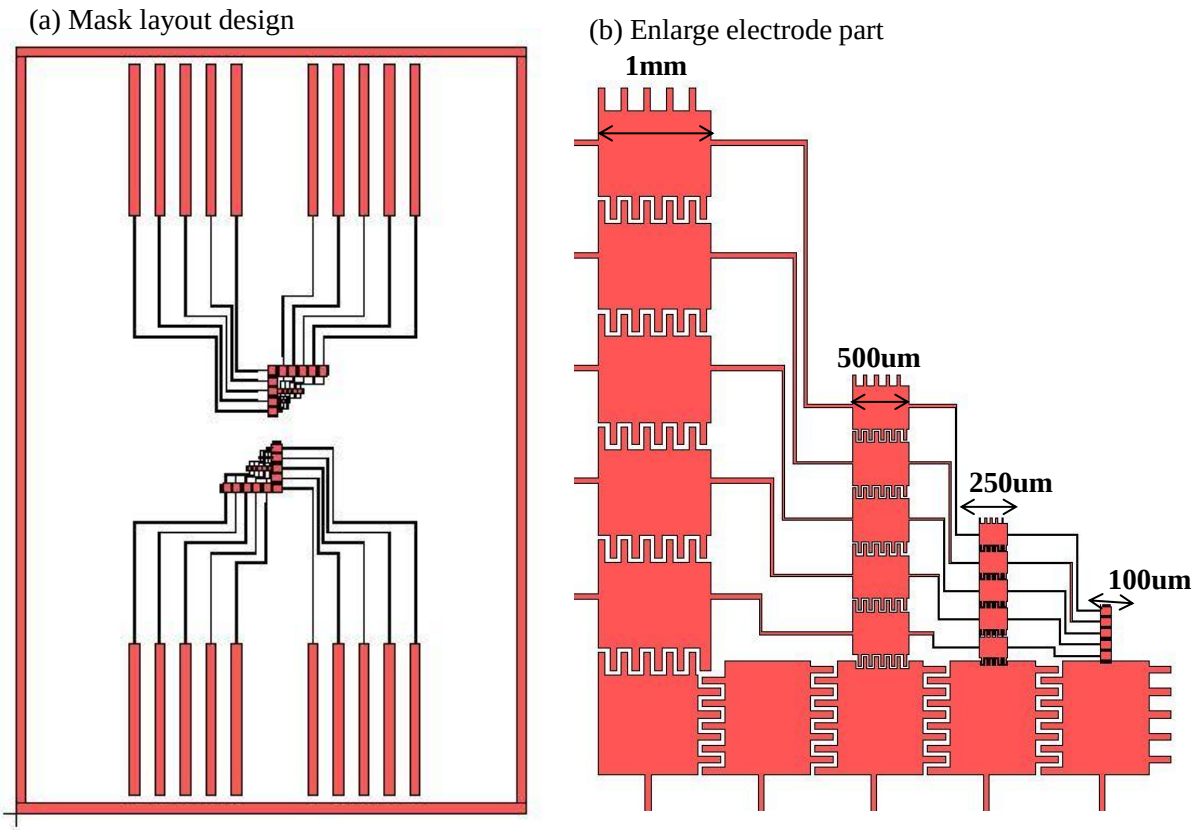
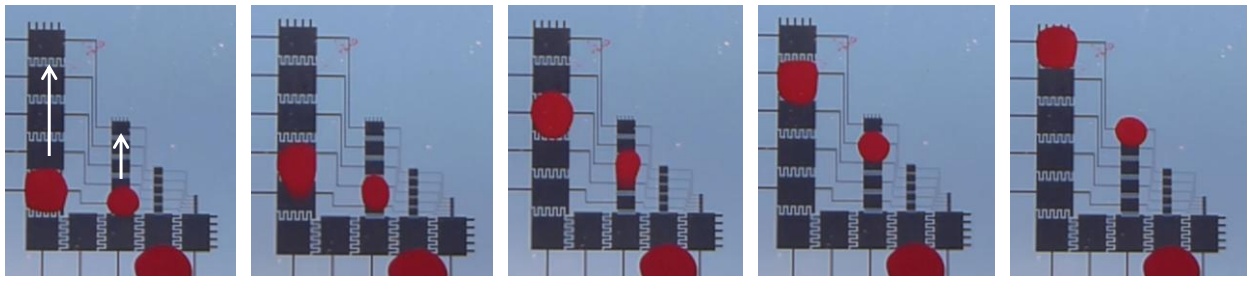


Figure 5-14. Mask layout design of different electrode size (1mm, 500um, 250um, 100um)

(a) The actuation of two droplets in 1mm electrodes and 500um electrodes



(b) The process of splitting in different size electrodes (from 1mm to 500um)

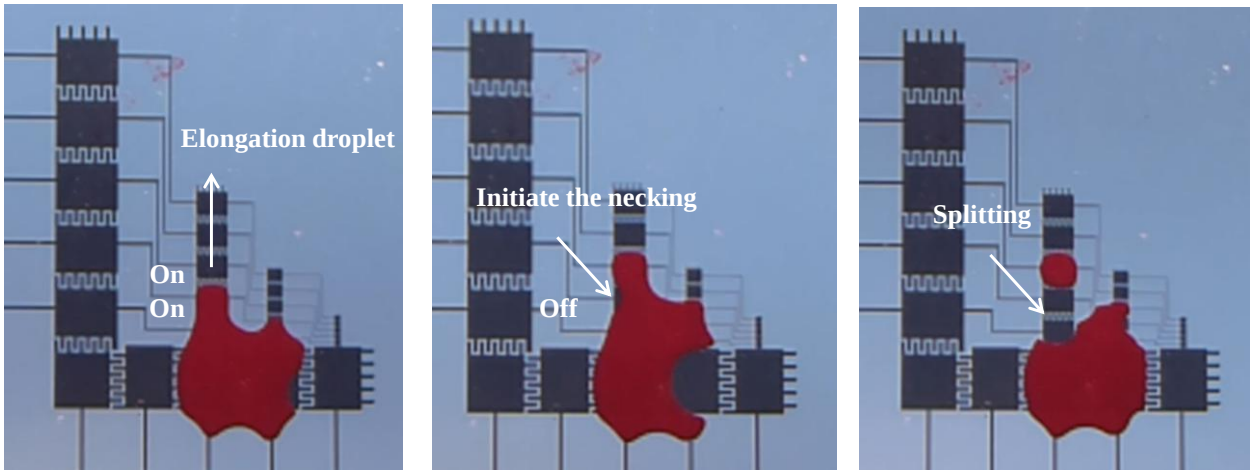


Figure 5-15. Different size two droplets motion and the process of splitting in different size electrodes

5.6 Conclusion

In this chapter, we have studied the basic electrowetting test which demonstrates electrowetting phenomena such as, liquid droplet actuation test, comparison of conventional and Laplace barrier devices, and splitting mechanisms of liquid droplets in different sized electrodes. In electrowetting phenomena test, we demonstrates the change of wetting angle with applied voltage and performance of In_2O_3 TFT as switching device in electrowetting device. In addition we have studied the droplet actuation which is performed in 5x1 electrode electrowetting devices.

The comparison between conventional electrowetting device and Laplace barrier device is implemented by measuring the moving time and speed of liquid droplet. Finally, we tested the splitting the liquid droplet in the different size of electrode device. This basic electrowetting tests are based on the actuation and functional moving of liquid droplet in our full integrated TFT electrowetting device.

*Acknowledgement

The work presented in this chapter has been collaborated with Jason Heikenfeld's group and Ian Papautsky in University of Cincinnati. The some parts of electrowetting device and top plates for Laplace barrier device was fabricated by Jason Heikenfeld's group. Joo Hyon Noh helped to the device fabrication and Pspice simulation of this chapter, and Philip Rack provided direction, funding of the research, discussion and motivation.

Chapter 6

Active matrix driving for electrofluidic device using IGZO TFTs

6.1 Introduction

Many researchers have studied the development of highly integrated and automated lab-on-a-chip systems for chemical and biological applications [98,99]. Lab-on-a-chip systems offer many potential advantages including efficiency of time and materials, the automation of test, and the portability lab. To realize many of these advantages of lab-on-a-chip, there are two kinds of lab on chip systems. One is the continuous microfluidics micro channels which provide pressure driven flow, and the other is electrowetting device using electrokinetic and surface tension of liquid droplets [2,100-102]. In this dissertation we will focus on the electrowetting device to control the small liquid droplet and microfluidic channel. Electrical addressability of lab-on-chip devices currently requires external switching devices for each individual electrode for droplet transport, merging, and splitting [99]. Thus for complex arrays, many switching devices and interconnections are needed and scale directly with the number of elements (increased size or resolution). Therefore fabrication processes and cost can be complicated and expensive as the number of input-output connections becomes unwieldy. This problem can be overcome if an active matrix (AM) addressing method is integrated with electrowetting or dielectrophoresis control (m + n interconnections for the m x n elements array), as is used in liquid crystal display technologies [103]. For AM addressing, thin-film transistors (TFTs) are used as switching devices, where conventional active matrix flat panel displays typically employ hydrogenated amorphous or polycrystalline silicon as the semiconducting active layer. However, Si-based thin-film transistors (TFTs) are not transparent to visible light and have low mobility of < 1 $cm^2/V{\cdot}s$,

[48] thus making it challenging to implement optical imaging or spectroscopy, and to use high capacitance electrowetting control or high frequency dielectrophoresis control. Recently, transparent amorphous oxide semiconductors (AOSs) have been intensely studied for thin-film transistor arrays for AM display applications because of their high mobility of 1 -15 $cm^2/V{\cdot}s$ allowing logic inverters and ring oscillators with operations at frequencies as high as 2.1 MHz and low-temperature processing of room temperature – 350 °C allowing use of low-cost and large-area glass and polymer substrates. [13,48,75,104,105] Such high mobility can allow the electrofluidic platform to perform dielectrophoresis driving as well as electrowetting driving.

6.2 Experiments

In this dissertation, we demonstrate the addressability of electrofluidic devices with amorphous indium gallium zinc oxide (a-IGZO) thin film transistor arrays. Before the full integrated TFT electrowetting device, we represent the external connection between IGZO TFTs and electrofluidic device as an intermediate demonstration, a TFT array was coupled to electrofluidic devices using the interconnection scheme, as shown in Figure 6-1. Several important electrofluidic functionalities are demonstrated using a 2 x 5 electrode array connected to a 2 x 5 IGZO TFT array.

The 5 x 5 TFTs array using an inverted staggered structure was fabricated using a-IGZO film as the semiconductor n-type active layer. A chromium (Cr) gate metal (150 nm) was sputter deposited onto a 500 nm SiO_2 coated silicon wafer and subsequently lithographically patterned and wet chemically etched with a standard Cr wet etch solution ($9\%(NH_4)_2Ce(NO_3)_6$ + $6\%(HClO_4)$ + H_2O). A SiO_2 gate dielectric (100 nm) layer was deposited via plasma enhanced chemical deposition (PECVD). The a-IGZO active layer (50 nm) was deposited by rf-magnetron

sputtering using 2 inch diameter target (In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol %) at room temperature. The rf sputtering power was 60 W and the sputtering pressure was 5 mtorr with a 20:5 mixing ratio of argon and oxygen, respectively, at a fixed total flow rate of 25 sccm. The a-IGZO active area was photolithographically patterned and etched using diluted 0.1% buffered oxide etchant. Ti/Au (10/80 nm) source and drain electrodes were deposited by e-beam evaporation and patterned by a lift-off method. The TFT semiconductor channel width (W) and length (L) were 50 and 20 μm, respectively. Finally, the samples were annealed at 350°C in nitrogen ambient for 1 hr. Figure 6-2 (a) and (b) show a picture of fabricated 5 X 5 IGZO TFT array and cross-sectional view schematic. Figure 6-2 (c) shows schematic diagram of electrical driving system developed for active matrix addressing of the IGZO 5 X 5 TFTs array. A pulse generating program was developed using LabView software. This program controlled the data acquisition (DAQ) card to send control signals to solid state relays (Vishay Semiconductors LH1512BB). During operation, 2 external power supplies (Keithley Model 2400 Sourcemeter) and 10 relays were used. Relays were inserted between power supplies and gate and source electrodes, as shown in Fig. 6-2 (c). During the testing the relays used 5 V signals generated by the DAQ card, and higher voltages were then applied to IGZO TFTs array platform. Electrical connections between the TFT array and the electrofluidic pixels were made using a customized test clip with spring load pins. For the active matrix testing and characterization, an unpassivated TFT array was used and the interconnection scheme is illustrated in Fig. 6-2 (d).

Electrofluidic devices consisted of a 2 x 5 array of interdigitated electrodes with a pitch of 2.54 mm. The bottom glass plate was coated with a 100 nm-thick Al layer by e-beam evaporation and patterned using the lift-off process. Subsequently, a 200 nm-thick SiO_2 dielectric layer was deposited by plasma enhanced chemical deposition (PECVD). The

electrofluidic top plate consisted of the indium-tin oxide (ITO) coated glass. The bottom and top plates were then dip-coated in Cytonix Fluoropel 1601 V solution with a 2.5 mm/s pulling speed and baked for 30 min at 140 °C to form a hydrophobic fluoropolymer film of~50 nm thickness and a low ~16 mN/m surface energy. The Fluoropel is so thin and porous, that the ITO electrode on the top plate is effectively electrically conductive with any fluid in the channel. A glass spacer was used to create the requisite gap of 160 μm between the top and bottom plate. Before clamping, an aqueous conducting fluid of ~ 1 μl was dosed on the Al electrode. For visualization, a 10 wt % red pigment with 0.01 wt% of sodium lauryl sulfate was dispersed in the fluid. The top and bottom plates were then clamped, and insulating silicone oil (Dow Corning OS-30 oil) was infiltrated into the gap between the plates. The interfacial surface tension between the conducting pigment dispersion and insulating oil was $\gamma_{ci} \approx 56$ mN/m. Figure 6-2 (e) shows cross-sectional schematic of the completed electrofluidic device.

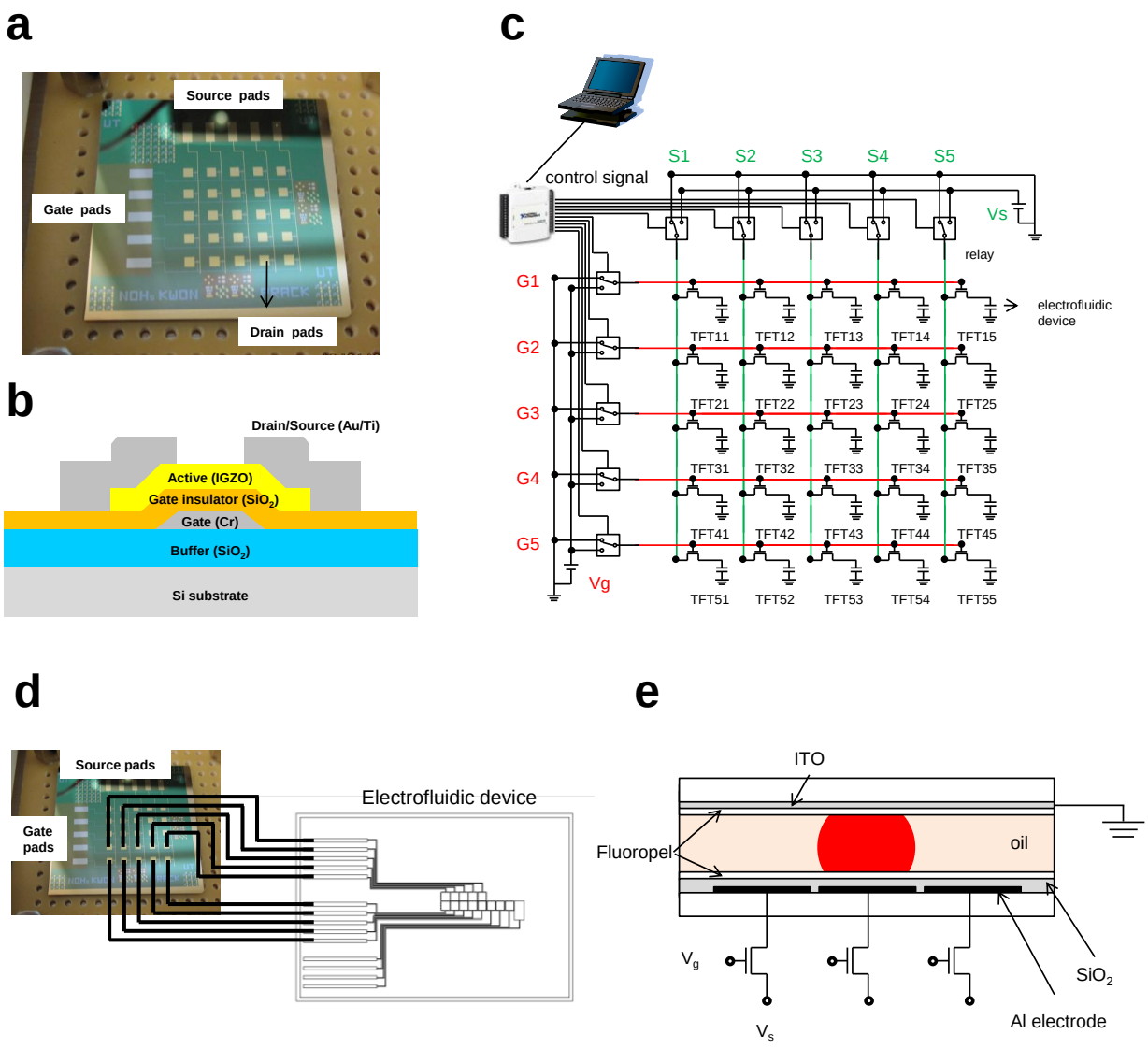


Figure 6-1. (a) Picture of 5 x 5 IGZO TFTs array. (b) Cross-sectional view of IGZO TFT. (c) Schematic diagram of TFTs array driving system. (d) Illustration of interconnection between TFTs array and electrofluidic device. (e) Cross-sectional view of electrofluidic device.

6.3 Results and Discussions

Figure 6-2 (a) shows the transfer characteristics at V_{DS}=30V of 15 IGZO TFTs (rows 1 - 3). The IGZO TFTs demonstrate good electrical performance and uniformity. The saturation field effect mobility μ_{FE} and threshold voltage V_{th} are 6.3 ± 0.18 cm^2/V-s and V_{th} of 6.6 ± 0.49 V, respectively. The off-currents at V_{GS} = 0 V were ~ 10^{-9} A, corresponding to ~ 30 GΩ off-state resistance.

In order to determine the real driving voltage of the electrofluidic device when the TFT was connected to the electrofluidic device, the source voltage was applied to source electrode of TFT, and then the voltage at the drain electrode, which is the real driving voltage of electrofluidic device (V_E), was measured as a function of V_G and V_S. Figure 6-2(b) shows V_E as a function of V_G when the V_S was maintained at 20 V for the 3 TFTs (TFT 11, TFT 21, and TFT 31). When V_G was 0, V_E was also 0, which means the entire V_S was dropped across TFT. As V_G was increased and the TFT channel resistance decreased, V_E increased and the voltage drop across the TFT ($V_S - V_E$) decreased. Figure 6-2(c) shows the driving voltage V_E as a function of V_S.

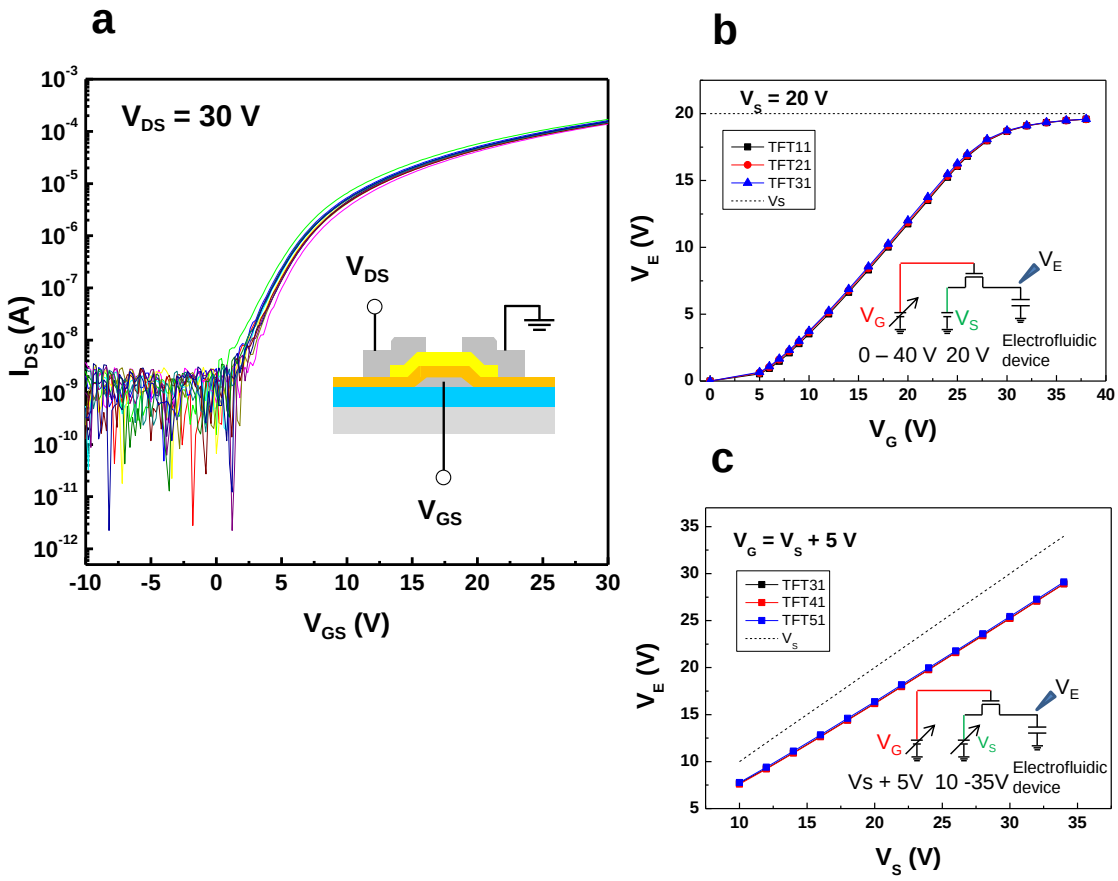


Figure 6-2. (a) Individual TFTs transfer characteristics. TFT output voltage V_E as a function of (b) V_G and (c) V_S.

To evaluate the capability of the TFTs to drive electrowetting without compromise in droplet transport speed, droplet transport velocities were compared for both relay and TFT driven electrofluidic devices. In the case of the relay driven electrofluidic devices, each electrode was connected directly to the relay. As the relay has very low on-state resistance (10 Ω), the voltage drop across relay is virtually 0 V. In the case of the TFT driven electrofluidic device, each electrode of the electrofluidic device was connected to a drain electrode of a TFT. Constant source voltage was applied on the source electrodes of all TFTs and the gate voltage of each TFT was modulated to drive electrowetting. The droplet transport velocity was calculated from the moving time of the droplet leading edge across the electrode pitch of 2.54 mm by image analysis. According to the electrode position, there were deviations of droplet transport velocity because droplet transport is sensitive to the surface condition and gap height. As shown in Figure 6-3(a), the droplet transport velocity for the TFT driven electrofluidic device was slightly slower than for the relay driven electrofluidic device at the same applied voltage because of the slight voltage drop across the TFT, in agreement with the data of Figure 6-2. When the supplied voltage is replaced with the real driving voltage (V_E) for the TFT using Figure 6-3(c) data, as expected, there is no difference in the droplet transport velocity between the relay and TFT driven electrofluidic device. Figure 6-3(b) shows the velocity$^{1/2}$ vs. voltage plot (where V_E was used for the TFT driven electrofluidic device using the relationship of V_S and V_E from Fig. 6-2(c)). The linear relationship between the square root of droplet velocity and voltage was obtained which is consistent to what has been reported previously[106]. The linear fit line is shown as the blue dashed line.

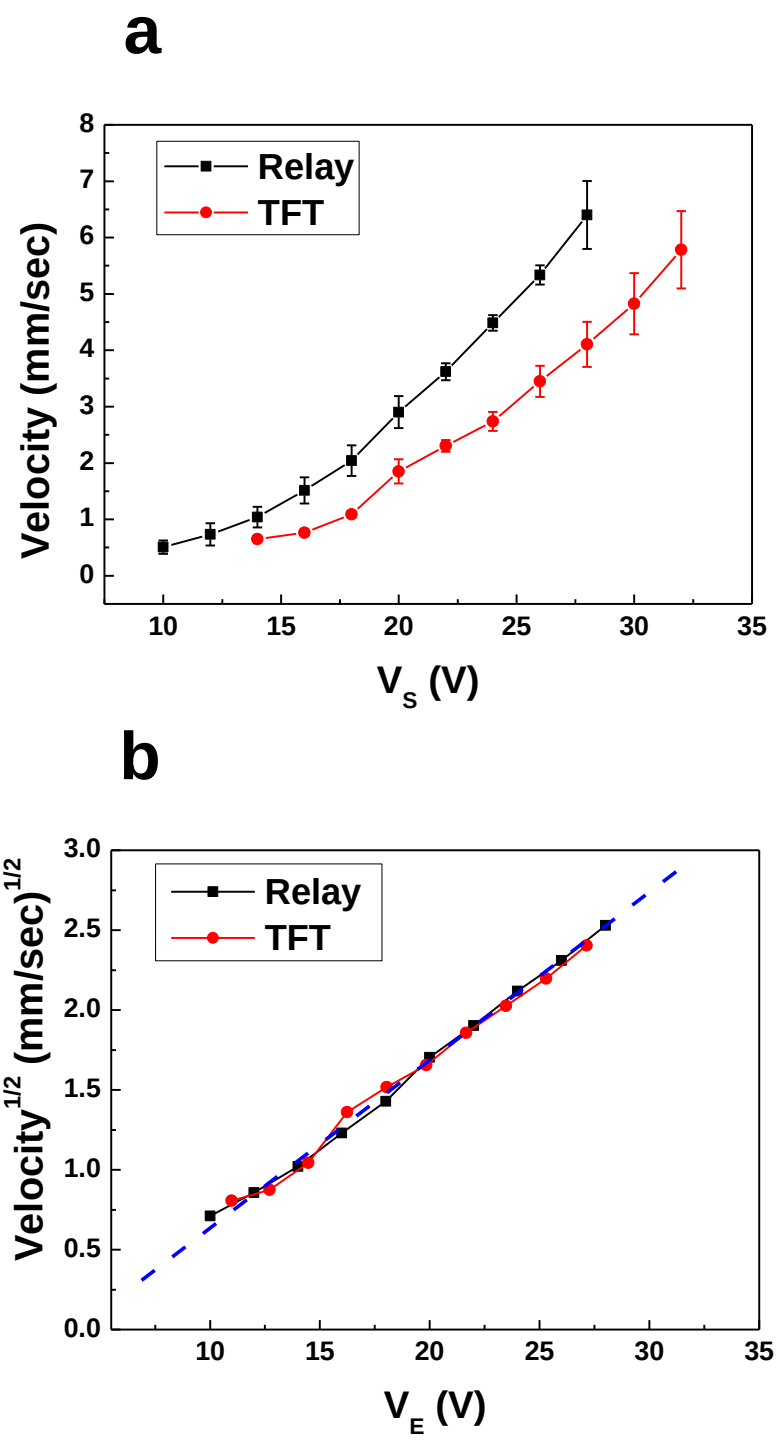


Figure 6-3. (a) Electrowetting transfer velocity as a function of V_S. (b) Square root of the electrowetting transfer velocity plot as a function of V_E.

Beyond the TFT actuated electrofluidic transport, active matrix (AM) electrowetting control was also explored. To show unique AM driven electrowetting, two individual droplets were simultaneously controlled using a 2 (gate rows) x 5 (source columns) electrofluidic electrode array (Figure 6-4). Gate pulses with 50 msec pulses width and 40 V amplitudes were sequentially applied to the two gate rows. Initially, two droplets were positioned at (G1, S4) and (G2, S2) with a combination of gate and source pulses, as indicated as ① in Figure 6-4. Source pulses had 50 msec pulse widths and 35 V amplitudes. To simultaneously move the droplets upward and downward, the source pulses were changed, as indicated as ②. Interestingly, droplets could not entirely move to the next electrodes during one 50 msec pulse sequence because droplet transport speed was ~ 6 mm/sec at a source voltage = 35 V. Therefore, these pulse combinations had to be maintained for certain time (denoted as t_{moving}) to completely move the droplet from pixel to pixel, as indicated as ③. For the current system, t_{moving} was ~ 3 sec (or ~ 30 pulses). Using similar combination of gate and source pulses further droplet motions were demonstrated, as indicated as ④ - ⑧. As demonstrated in Figure 6-4, the simultaneous and individual droplet control for 10 (2 x 5) electrodes was achieved using only 7 bias lines (2 gate and 5 source bias lines), which is obvious merit of AM driving method. If electrofluidic device is scaled up with m x n elements for complex electrofluidic arrays, only m + n bias lines are needed.

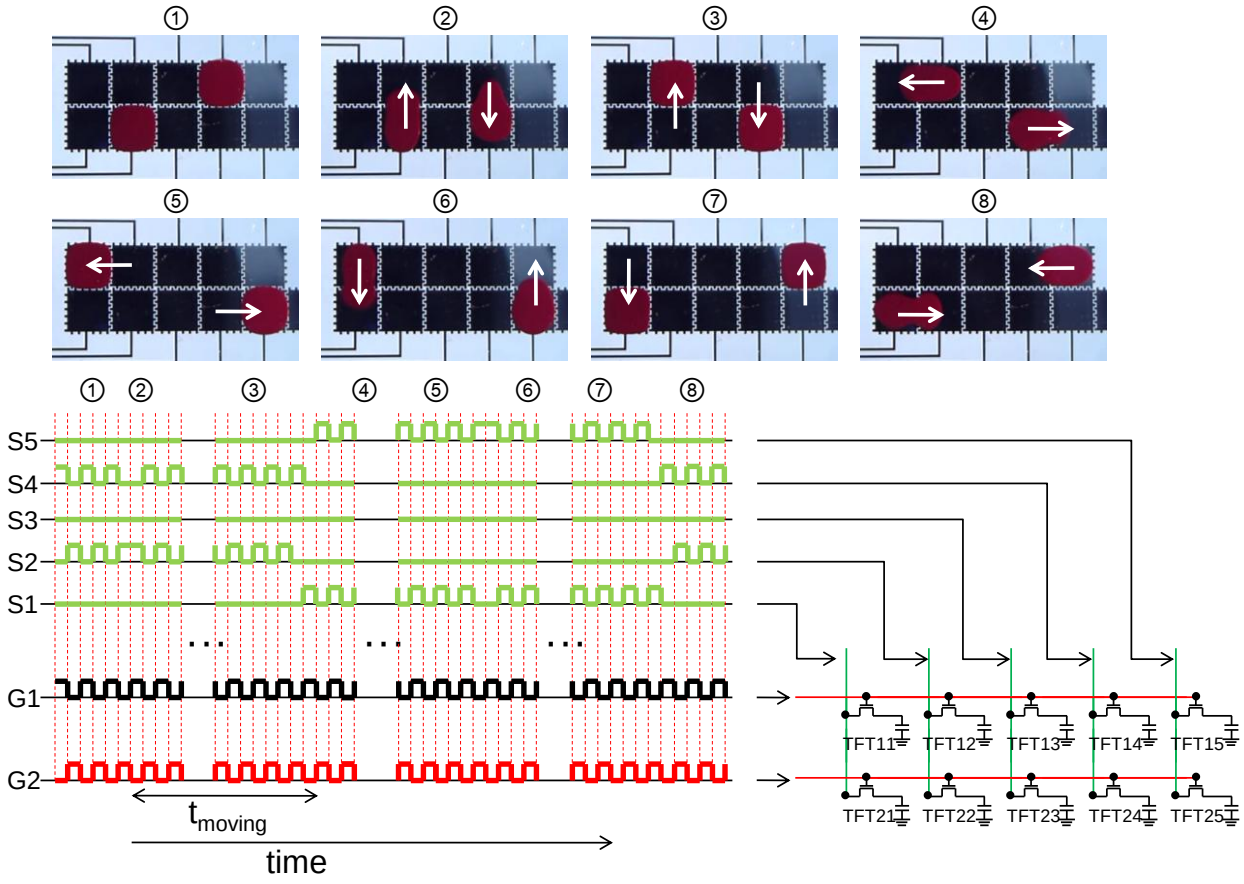


Figure 6-4. Simultaneous and individual control of two droplets by active matrix addressing method using IGZO TFT array

Figure 6-5 shows additional functionalities obtained using AM driven electrofluidic devices that are important for Lab-on-chip microfluidic applications. Continuous channel formation is demonstrated in Figure 6-5(a). The continuous channel could be formed evenly across individual rows. Two dimensional “L” and “T” shape channel formations are also demonstrated in Figure 6-5(b). However, this two dimensional channel cannot be maintained if the voltage is turned off. “L” or “T” shapes change to circular shapes due to surface tension. However, if the top plate is replaced with post arrays or a so-called “Laplace barrier” structure [97], off-state stability is possible and the channel shape can be maintained even when the voltage is turned off. Additionally, channel merging and splitting are demonstrated in Figure 6-5(c). The number on the top left side of figure indicates merging and splitting sequence.

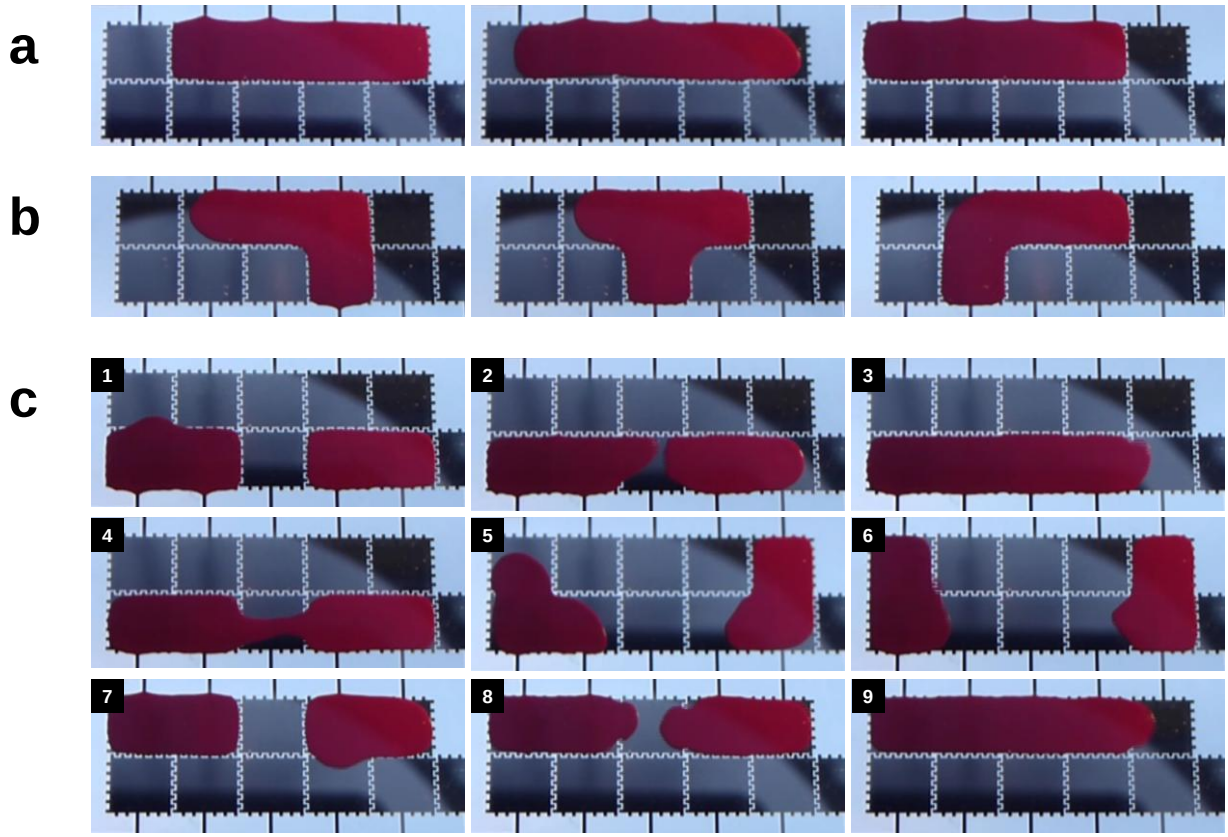


Figure 6-5. Electrofluidic functionalities using AM driven electrofluidic device for Lab-on-chip application. Continuous channel formation (a) on one row and (b) across rows (c) One droplet control on the adjacent row when continuous channel was formed on one row.

Several additional observations for AM driven electrowetting droplet movement are worthy of discussion. Interestingly, droplet vibration was observed during AM driving. In order to understand this vibration, we measured wave forms during gate and source pulsing using an oscilloscope, as illustrated in Figure 6-6(a). Figure 6-6(b) shows the wave forms of the gate, source and electrowetting voltage. The gate pulse frequency was 5 Hz and duty cycle was 50 %. The source pulse width was set equal to the gate pulse width. The gate and source pulse amplitudes were 35 and 30 V, respectively. When the gate and source pulses were applied, ~ 5 V was dropped across the TFT and a V_E of ~ 25 V was induced at the electrofluidic device. For the AM driving, V_E should be maintained during the subsequent gate pulse off period. However, the measured V_E showed a rapid decrease, reducing the electrowetting effect, which causes the droplet vibration during pulsing. At the end of gate pulse off period (indicated with arrows in Figure 6-6), V_E was 0 V. The voltage decrease is related to RC charging-discharging in the series circuit of the resistance and capacitance of the apparently leaky SiO_2 dielectric layer. The voltage discharging is expressed as

$$V_E = V_{E,max} \cdot \exp\left(-\frac{t}{\tau}\right), \tag{6.1}$$

where V_E is the voltage across the electrofluidic device, $V_{E,max}$ is the initial voltage, t is the elapsed time, and τ is the RC time constant of the circuit. The leakage current through one electrode of the electrofluidic electrodes with a liquid droplet was individually measured and was determined to be in the range of 10 – 100 MΩ (denoted as R_E). The capacitance of one electrofluidic electrode (denoted as C_E) was calculated to be ~ 750 pF based on the dielectric constant and thickness of SiO_2 (3.9, 200nm) and Fluoropel (2.0, 50nm) layers and the area of the electrode (0.0645 cm^2). Using the RC time constant of 7.5 msec (10 MΩ x 750 pF), the

calculated voltage across the electrofluidic device is 1.74 V after 20 msec, which is in good agreement with the measured value of ~ 2.5 V. In order to slow down the discharging time, external storage capacitors were additionally connected to electrofluidic device. Figure 6-6(c) and (d) show the waveforms with the 10 and 100 nF external storage capacitors, respectively. At the end of gate pulse off period, V_E was 11.8 and 20.2 V, corresponding to 47.4 and 84.2 % of $V_{E\,max}$, respectively.

Two ways to keep V_E high during the gate pulse off period is to increase the electrofluidic device capacitance or the driving frequency. Figure 6-6(e) shows the waveform with 10 nF external storage capacitor for the gate pulse frequency of 10 Hz and duty ratio of 50 %, respectively, and the source pulse width was again set equal to the gate pulse width (50 msec). At the end of the gate pulse off period, V_E was 15.7 V, which is higher relative to the 11.8 V of the 5 Hz pulse frequency. With the current geometry and 10 nF external storage capacitor, using a typical drive frequency of 120 Hz (4 msec pulse width and 50 % duty cycle) the voltage decreased only to 87.8 % of $V_{E\,max}$, as shown in Figure 6-6(f). 60-120 Hz is a key frequency target as it is the commonly utilized frame rate for the hardware and software that controls pixels in AM liquid crystal displays.

The most obvious way to decrease the discharging time and obtain a high RC time constant is to increase resistance of dielectric. The RC time constant can be expressed as

$$R \cdot C = \rho \cdot \frac{t}{A} \cdot \varepsilon_0 \varepsilon_r \frac{A}{t} = \rho \varepsilon_0 \varepsilon_r, \tag{6.2}$$

where ρ is resistivity, ε_0 is vacuum permittivity, ε_r is relative dielectric constant, *A* is area, and *t* is thickness of dielectric layer. Because resistivity and relative dielectric constant are intrinsic

material parameters, the RC time constant is fixed regardless pattern size when a single layer dielectric material is chosen. Thus, instead of single layer dielectrics, multilayer dielectrics, which consist for instance of polymer layers with low leakage current [107] and inorganic layers with higher dielectric constant, can be used to optimize the resistance and capacitance for optimal AM driving without significant loss of total capacitance[104].

Conversely, charging of the capacitor also slows as capacitance was increased and gate pulse width was decreased. The charging time is expressed as

$$t_{charging} = C_{tot} \cdot \frac{V_E}{I_{on}}, \tag{6.3}$$

where, C_{tot} is total capacitance, and I_{on} is on-state current of the TFT. Thus charging time can be reduced by increasing on-current of TFT: 1) increase field effect mobility of TFT, 2) increase voltage of gate (V_G), and 3) change the TFTs geometry (increase width or decrease length of TFT).

From the above consideration of the electrofluidic/TFT properties, the necessary dielectric properties can be extracted for a scaled-up electrofluidic device with any number of gate rows, m. When the gate pulse width is chosen t_G, the time of the gate off period is expressed as $t_G \cdot (m-1)$. If a 10 % voltage drop is tolerable to maintain an on-state and ensure smooth droplet movement, the gate off period time should be shorter than ~ 0.105 times the RC time constant ($t_G \cdot (m-1) < 0.105\tau$). Consequently, the dielectric material should be tailored to satisfy necessary RC time constant. If the dielectric material itself cannot satisfy necessary RC time constant, an additional storage capacitor can be implemented in the TFT array platform as is commonly used for AM LCD displays.

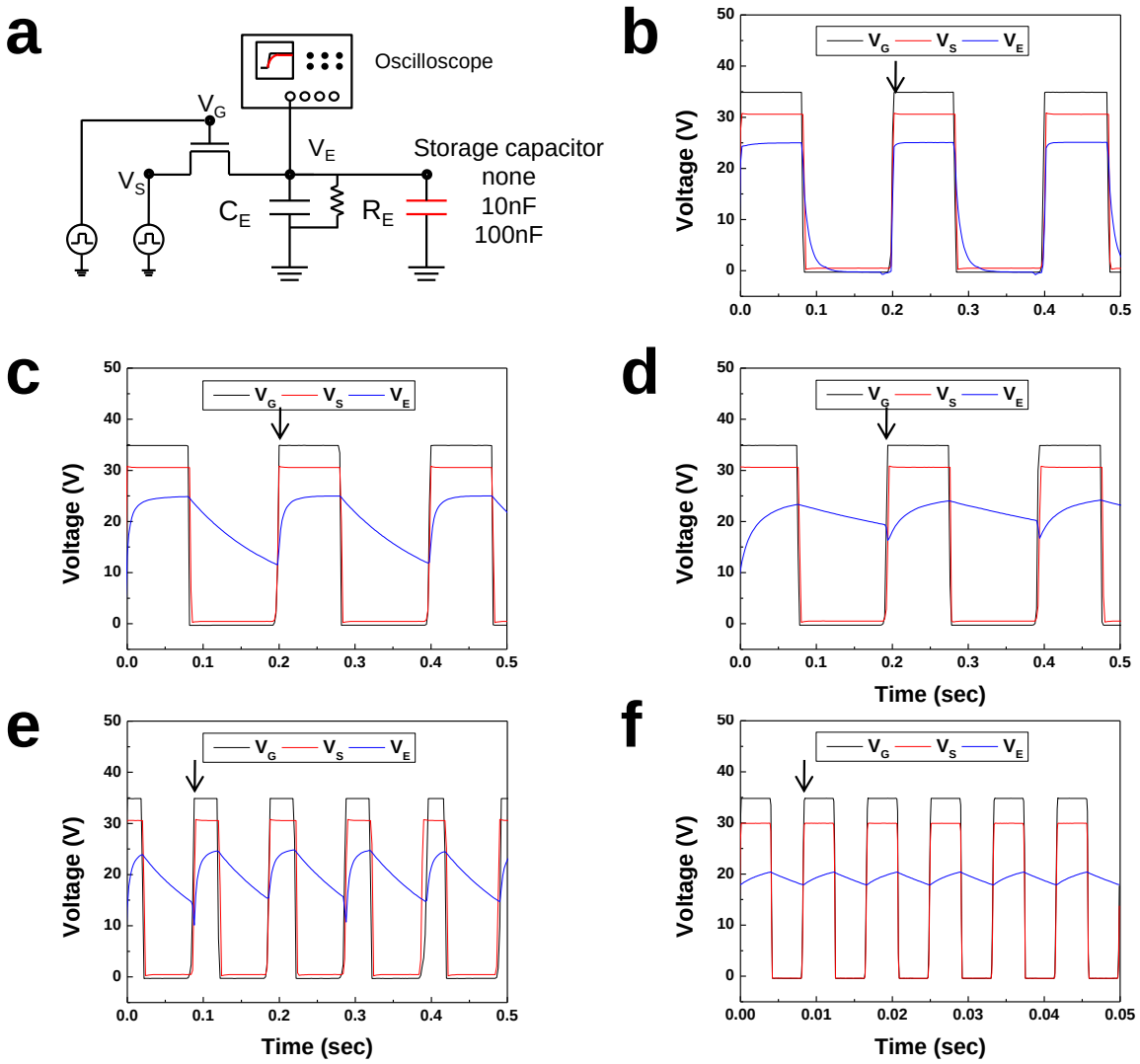


Figure 6-6. (a) Schematic diagrams of wave form measurement. Gate, source, and electrowetting voltage waveforms as a function of external storage capacitor with gate pulse width of 100 msec; (b) only electrofluidic device, (c) electrofluidic device + 10 nF external storage capacitor, and (d) electrofluidic device + 100 nF external storage capacitor. Voltage waveforms for the electrofluidic device + 10 nF external storage capacitor with gate pulse frequency of (e) 10 Hz and (f) 120 Hz (50% duty ratio).

Additionally, the TFTs must be optimized for both ON and OFF state resistance to satisfy an active matrix drive scheme. Firstly, the ON state resistance of the TFT must be small enough, which can be achieved by increasing the gate voltage and/or by increasing the TFT semiconductor active channel width as mentioned above, such that the TFT can fully charge the electrofluidic voltage (capacitor) during the gate row write time. This suggests that the $R_{(TFT-ON)}C_E$ time constant should be less than ~ 20% of the designed write time. Secondly, once a voltage is written to the electrofluidic device capacitor, the voltage has to be maintained during the entire frame (until the next voltage is written in the next frame). This requires that the time constant for the OFF state TFT resistance and electrofluidic device capacitance ($R_{(TFT-OFF)}C_E$) be much longer than the frame write time. This further requires that the R_E be similarly large such that it also satisfies an R_EC_E time constant much than the frame rate. To achieve for instance a typical VGA (640 columns x 480 rows) and assuming R_E is 1 GΩ, and C_E is 750 pF, and a 120 Hz frame rate (frame time = 8.3 ms, write time = 17.4 s); the requisite ON and OFF state resistances for the TFTs are ~ 4.6 kΩ and ~ 1 GΩ respectively. This combination should be achievable by using multi-layer electrofluidic dielectrics (R_E > 1 GΩ) and increasing either or a combination of the gate voltage, the TFT mobility, and/or channel width.

6.4 Conclusions

In summary, we have demonstrated a programmable electrofluidic platform driven by an active matrix addressing method using amorphous oxide thin film transistors. Because the active matrix addressing method minimizes the number of control lines necessary (m + n lines for the m x n elements array), the active matrix addressing method integrated with the electrofluidic platform can be a significant breakthrough for complex electrofluidic arrays (increased size or resolution) with enhanced function, agility and programmability.

*Acknowledgement

Active matrix driving for electrowetting device using a-IGZO TFTs has been published previously in the Lab on a Chip by Joo Hyon Noh, myself, Eric Kreit, Jason Heikenfeld, and Philip D. Rack [86]. Of the work presented in this chapter Joo Hyon Noh helped to perform the fabrication and electrowetting test, all fabrication processes were performed in Center for Nanophase Materials Science of Oakridge national Laboratory by me and Joo Hyon Noh. Philip Rack provided direction, funding of the research, discussion and motivation of this work.

Chapter 7

Full integration TFTs and Electrowetting devices

7.1 Introduction

In this chapter, we introduce the full integrated active matrix driving electrofluidic device. The fully integrated TFTs-electrofluidic device has the thin film transistor array underneath the electrofluidic device to control the electronic switching of the electrofluidic electrode. Figure 7-1 shows a prospective schematic diagram of electrofluidic device integrated on the TFT array. To realize the electrofluidic device integrated with the TFT array we need to develop the robust IGZO TFTs with passivation layer which is already discussed in chapter 4 in this dissertation, and the electrofluidic device process after TFT passivation layer. In this section, we describe the specific process flow and driving method of the fully integrated electrowetting device, and then we study the current issues of the fabrication process. We will investigate the change and optimization of the electric TFT characteristics after passivation layer. Finally we demonstrate the actuation of droplets and channels using a 5×5 matrix and 16×16 matrix fully integrated electrowetting device using active matrix addressing methods.

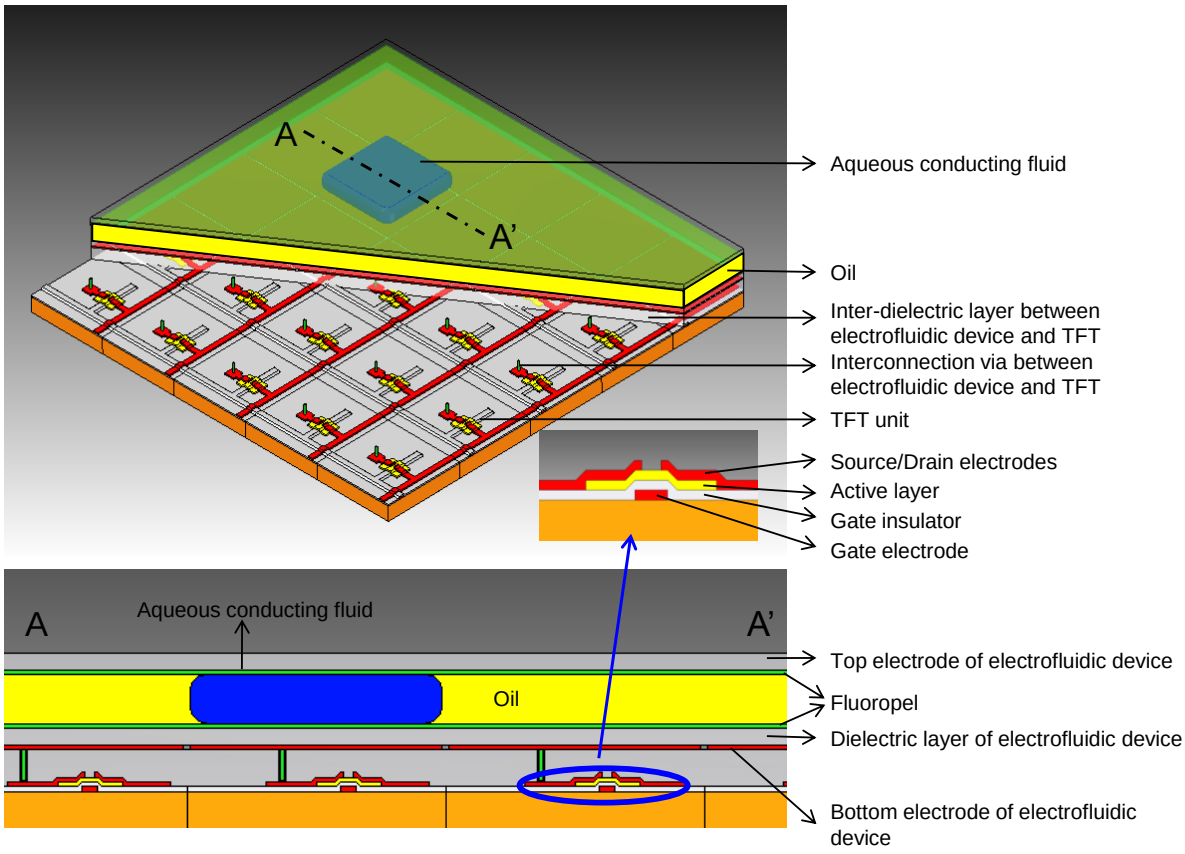


Figure 7-1. Prospective schematic diagram of electrofluidic device integrated on the TFTs array.

7.2 Experiments

Initially, we demonstrate a 5×5 matrix electrowetting devices consisting of 25 electrodes. Figure 7-2 shows the mask layout, cross-section structure and real sample picture of 5×5 matrix electrowetting device. We can fabricate 4 samples on each 4” wafer or glass substrate, and each sample has 25 IGZO TFTs with a W/L is 50/20um underneath electrowetting device and 25electrodes for on the top of TFTs. Secondly, we enlarge the scope of our electrowetting device with high resolution devices. Figure 7-3 represents the mask layout and sample picture of a 16×16 matrix electrowetting device which has total 256 electrodes.

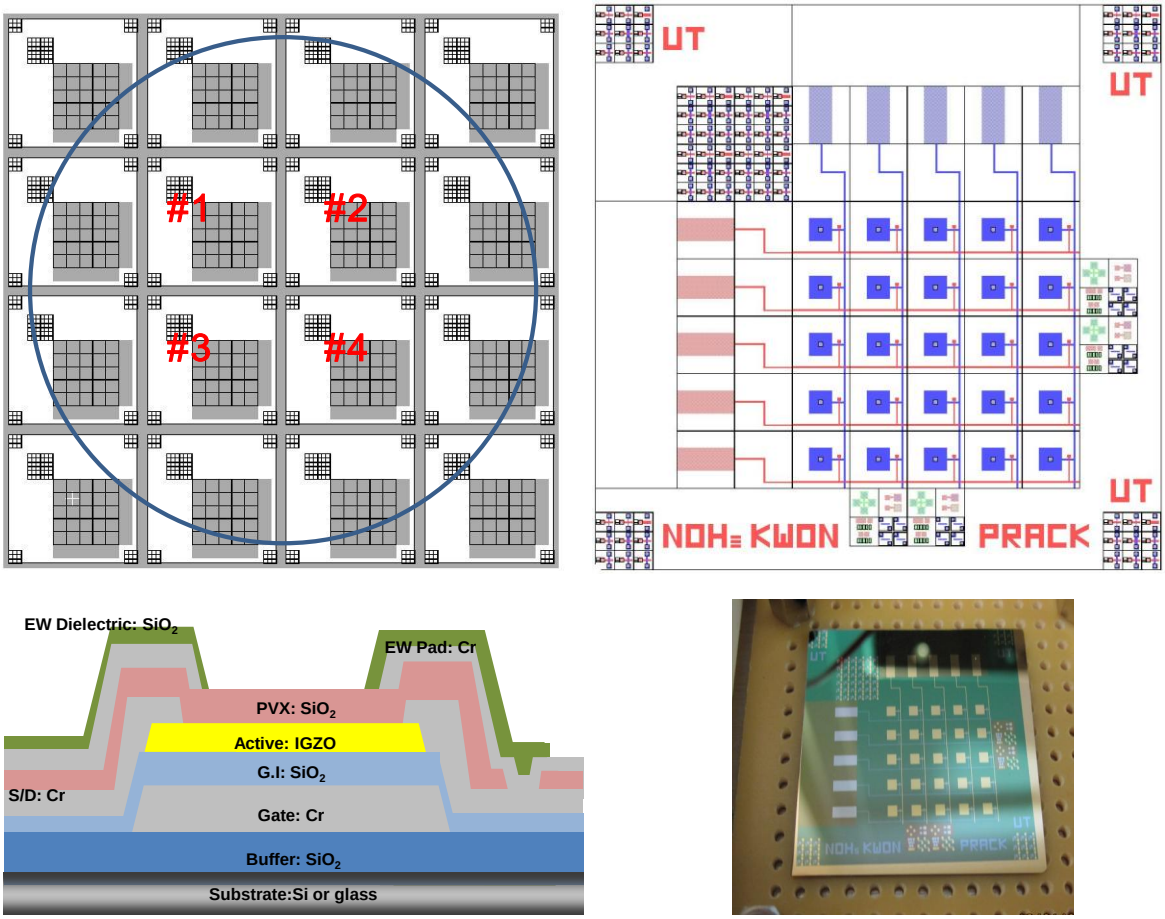
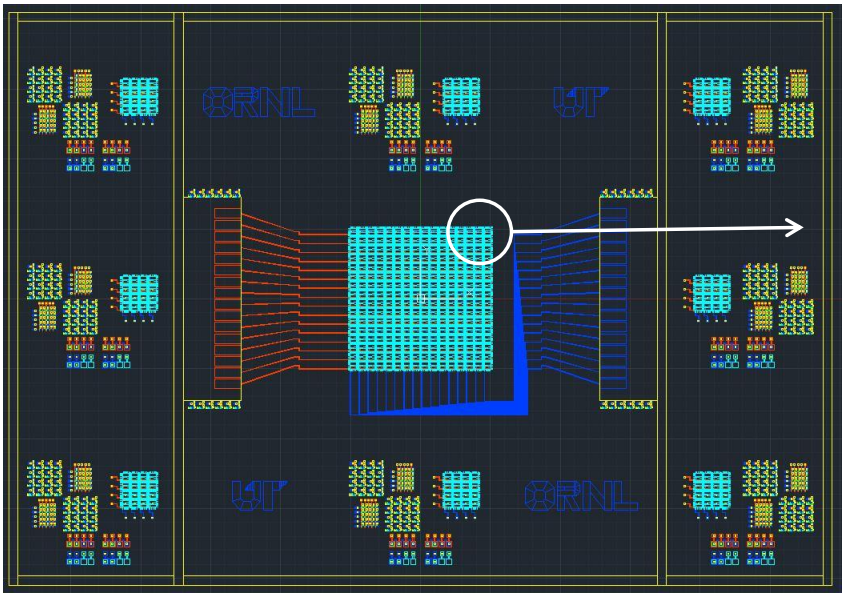
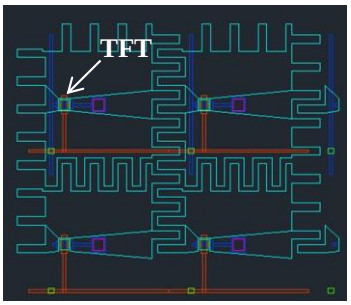


Figure 7-2. Mask designs, the cross section structure, and sample picture of 5x5 full integrated TFTs electrowetting device

(a) The mask design layout of 16 × 16 fully integrated electrowetting platform



(b) Shape of electrowetting electrodes



(c) Sample picture

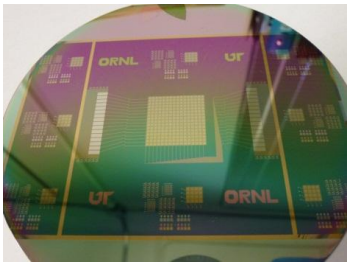


Figure 7-3. Mask design and sample picture of high resolution 16x16 full integrated TFTs electrowetting device

The preparation of fully integrated electrowetting device has lots of complicated process steps. Figure 7-4 shows the all process steps for fully integrated electrowetting device including the top plate of the sealed electrowetting device. We normally use 6 or 7 masks for this device (an additional 1 mask is used in passivation oxygen recess step to recovery IGZO TFTs on the final step because of instability and sensitivity of IGZO active layer). A 5 x 5 TFT array using an inverted staggered structure was fabricated using a-IGZO film as the semiconductor n-channel active layer. A chromium (Cr) gate metal (150 nm) was sputter deposited onto a 500 nm SiO_2 coated silicon wafer and subsequently lithographically patterned and wet chemically etched with a standard Cr wet etch solution (9%$(NH_4)_2Ce(NO_3)_6$ + 6%($HClO_4$) + H_2O). A SiO_2 gate dielectric (100 nm) layer was deposited via plasma enhanced chemical vapor deposition (PECVD). The a-IGZO active layer (50 nm) was deposited by rf-magnetron sputtering using 2 inch diameter target (In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol %) at room temperature. The rf sputtering power was 97 W and the sputtering pressure was 5 mtorr with a 15:10 mixing ratio of argon and oxygen, respectively, at a fixed total flow rate of 25 sccm. The a-IGZO active area was photolithographically patterned and etched using diluted 0.1% buffered oxide etchant. Ti/Au (80/10 nm) or Cr source and drain electrodes were deposited by e-beam evaporation patterned by a lift-off method or by rf magnetron sputter using the same condition as with the gate electrode. The TFT semiconductor channel width (W) and length (L) were 50 and 20 μm, respectively. The SiO_2 (400nm) passivation layer is also deposited by lower temperature plasma enhanced chemical vapor deposition process (200℃). Then the VIA hole, which is connected between the electrofluidic device and thin film transistor, is etched with an RIE dry etcher using SF6+Ar mixture gas. The Ti/Au(10nm/80nm) or Cr electrodes for electrofluidic device are deposited by evaporation or rf magnetron sputter and patterned by lift-off process or photolithographically wet

etch process, respectively. The electrowetting dielectric of the electrofluidic device is an SiO_2 (~200nm) deposited by PECVD. The 2nd VIA hole process, which connects the external signal line on gate and source electrodes of the TFT to control the device, is etched by an RIE dry etch similar to the 1st VIA hole process. Finally we anneal the sample for IGZO TFT activation at 350℃ for 1hr in air atmosphere. Subsequently, we fabricate the top plate using ITO (100nm) electrodes on the 3"×1" glass slide by rf magnetron sputtering.

Before the driving of electrowetting device, the bottom device, which is the fully integrated TFT electrofluidic device, and top plates, which is the ITO coated top plate, are dip-coated in Cytonix Fluoropel 1601 V solution with a 2.5 mm/s pulling speed and baked for 30 min at 140 °C to form a hydrophobic fluoropolymer film of~50 nm thickness. A glass spacer was used to create the requisite gap of ~160 μm between the top and bottom plate. Before clamping, an aqueous conducting fluid of ~ 1 μl is dosed on the bottom TFT sample. For visualization, a 10 wt % red pigment with 0.01 wt% of sodium lauryl sulfate was dispersed in the fluid. The top and bottom plates were then clamped, and insulating silicone oil (Dow Corning OS-30 oil) is infiltrated into the gap between the plates.

Figure 7-5 shows installation and assembly of the fully integrated TFT electrofluidic device and the electrical driving system developed for active matrix addressing of the IGZO 16 × 16 TFTs array. For the high resolution array, the microprocessor and user interface for controlling signal which were developed by Dan Grissom from the University of California at Riverside. The full integrated TFTs electrofluidic samples which were prepared to assembly bottom and top plate are connected to the microprocessor by using the external lines the gate electrodes (16 lines)

and source electrodes (16 lines). Two external power supplies are also connected to the microprocessor to control gate signal and source signal. A user interface was developed based on JAVA programming for easy controlling the pulse signals. All pulse signals between gate and source are simultaneously represented on an LED light board to conveniently monitor the pulse signals.

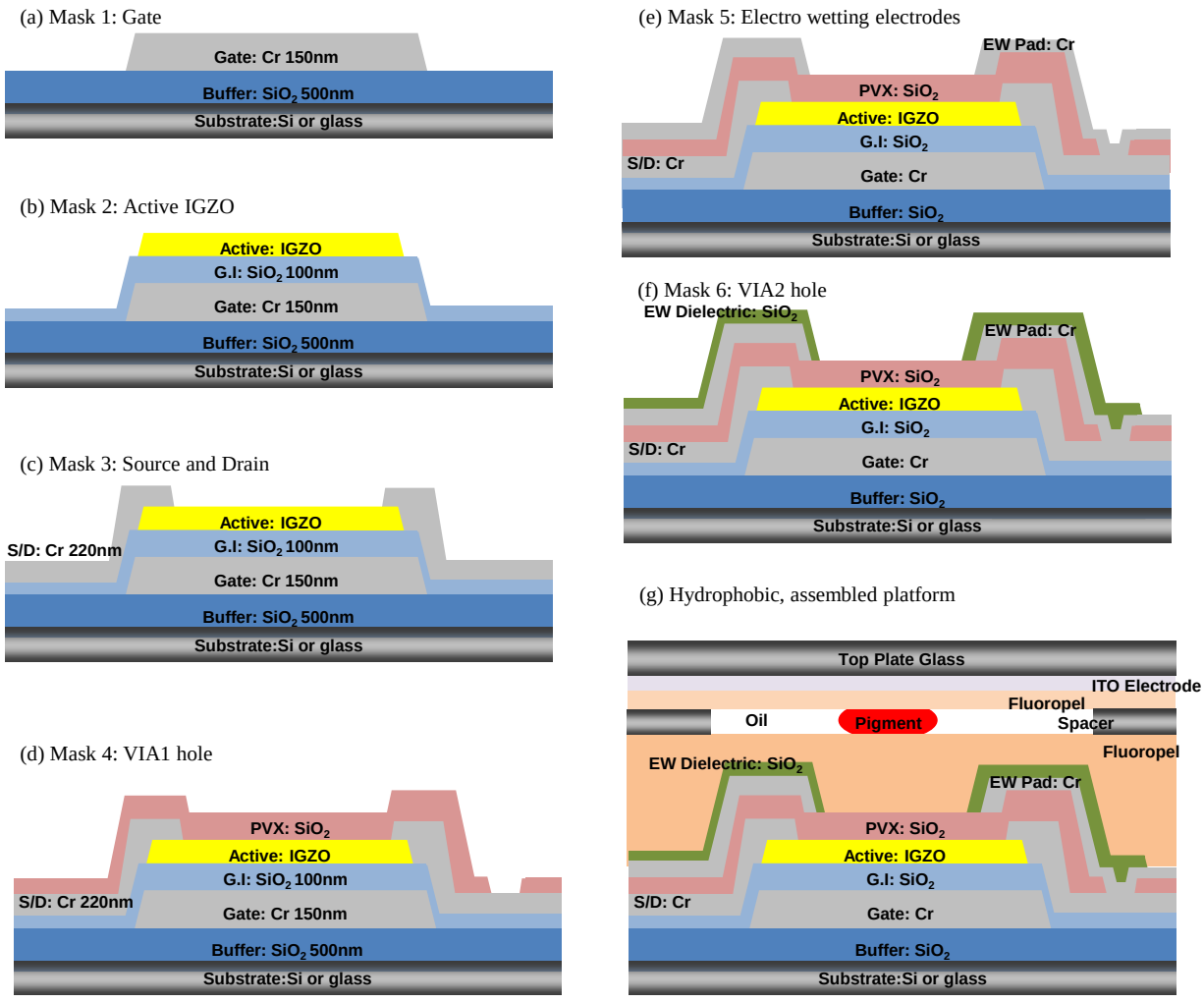


Figure 7-4. Process flows of full integration TFTs electrowetting device

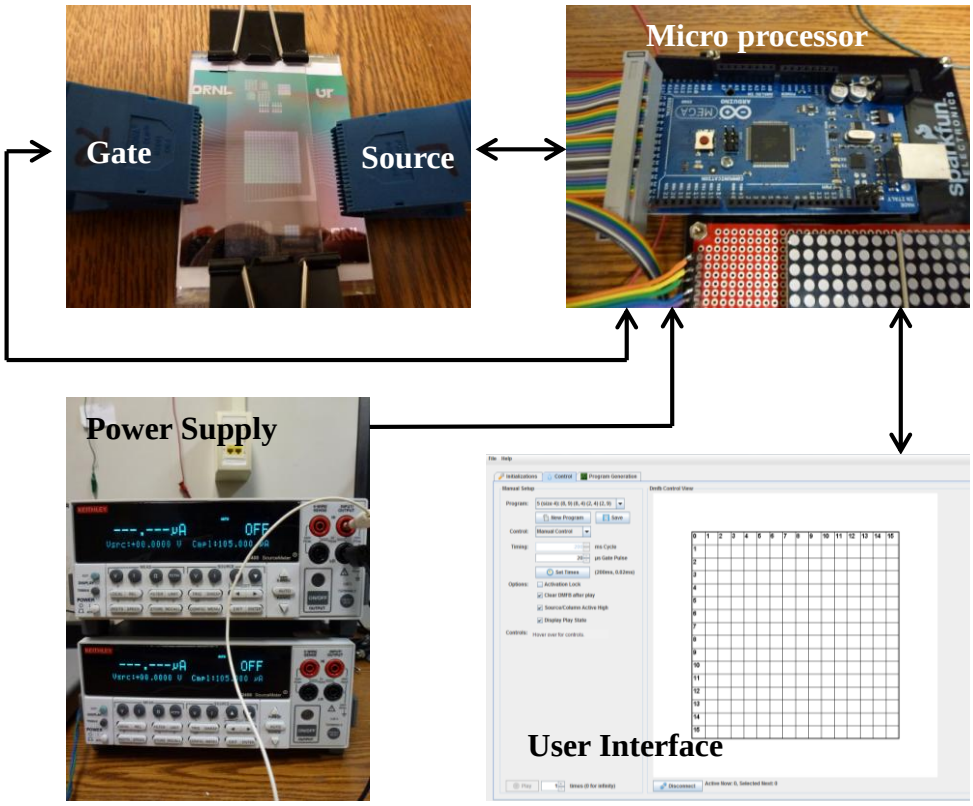


Figure 7-5. Sample preparation and assembly full integration device

7.3 Results and discussions

In chapter 4 we investigated the electrical characteristics of IGZO TFTs with passivation layers. Even though we had a good result of PECVD SiO_2 passivation layer, there are another problem during the post electrofluidic device process on top of the IGZO TFTs. The electrical characteristics of IGZO TFTs are degraded with post-processing progression because of the vacuum processes of the electrowetting electrode deposition and electrowetting dielectric process include high temperature process up to 350℃. Figure 7-6 represents the degradation of TFT characteristics before and after electrofluidic device process. To confirm this degradation required that the TFT electrical properties be evaluated step-by-step and subsequently optimize all the processes for full integration of the TFTs-electrofluidic device. The main process attributed to the TFT degradation was anticipated to be the oxygen reaction in IGZO semiconductor layer as described by the following chemical reaction with Kröger vink notation of formation of oxygen vacancies,

$$2O^- \text{ in IGZO solid } \rightarrow O_2 \ \ gas \ \uparrow + e^-, \tag{7.1}$$

$$\text{null} \rightarrow \frac{1}{2}O_2 + V_O^{2+} + e^-, \tag{7.2}$$

where V_O^{2+} is the oxygen vacancy sites which have 2+ charge in IGZO layer. Therefore, additional an 350℃ PECVD process creates additional oxygen vacancies and carriers in the IGZO layers, which effectively shorts the channel of the TFT. To solve this problem we changed our mask layout to remove the metal electrode on top of active channel region, so slight re-oxidation during the final annealing step could be facilitated. After all processes are finished, we

anneal the full integration devices at 350℃ for 1hr in air atmosphere to recover the TFT characteristics. Figure 7-7 represents the changes of TFT characteristics step-by-step and after the passivation process. After the passivation step without activation annealing, the electrowetting electrode deposition by e-beam or sputtering is the IGZO TFTs are slightly activated. After the electrowetting dielectric SiO_2 (200nm) deposition by PECVD the number of carriers increase in the IGZO layer as mentioned already and the characteristics of the IGZO TFT is degraded. These exhibit only high current (over 10^{-2} [A] over all operation gate voltage ($-10 < V_{GS} < 30V$)), thus this device cannot be used as electronic switching device. However, after 350℃ 1hr air atmosphere anneal, this TFT recovers to the original TFT characteristics, and exhibits a stable off-state.

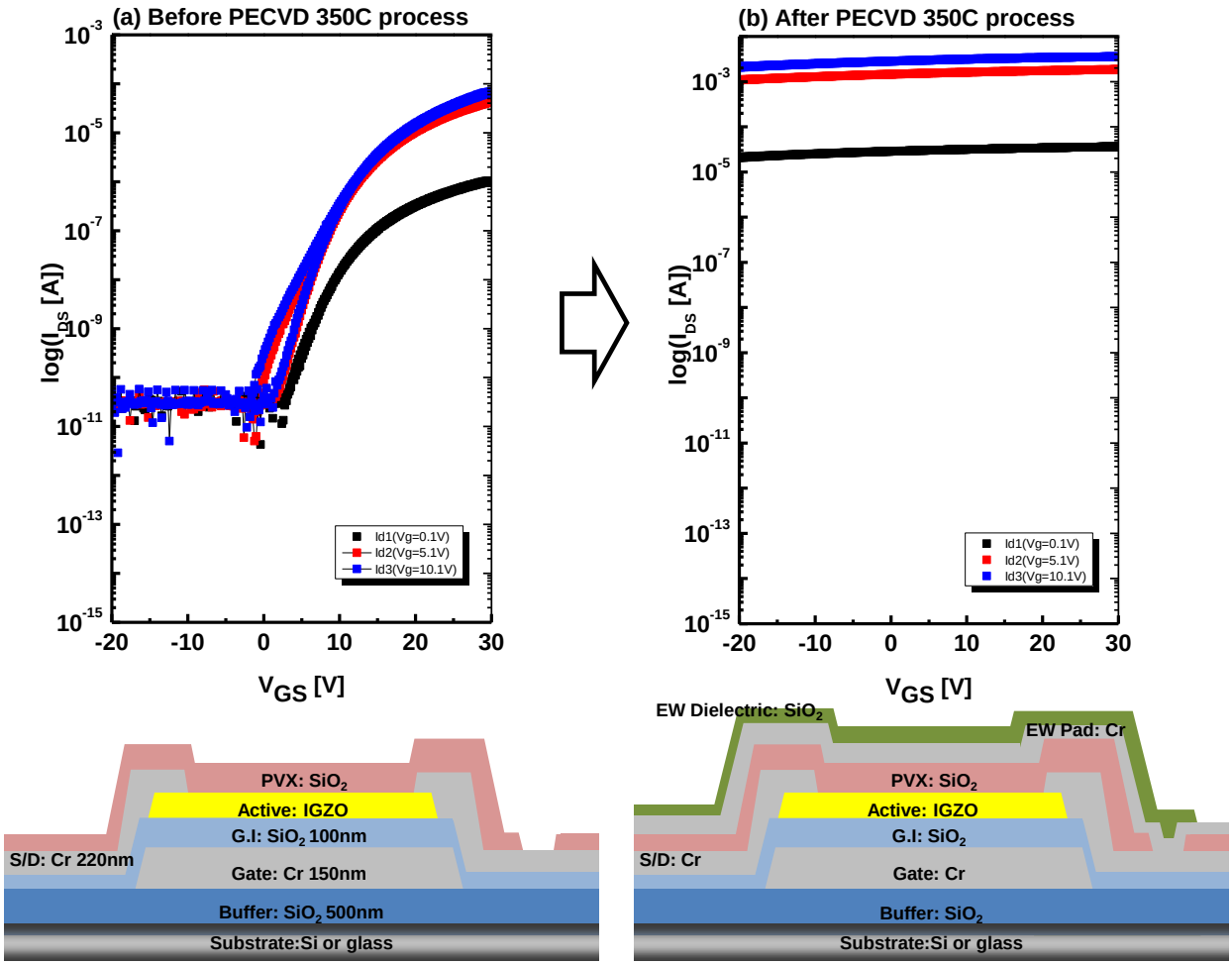


Figure 7-6. The degradation of TFT characteristics after electrowetting dielectric PECVD 350℃ SiO_2 process

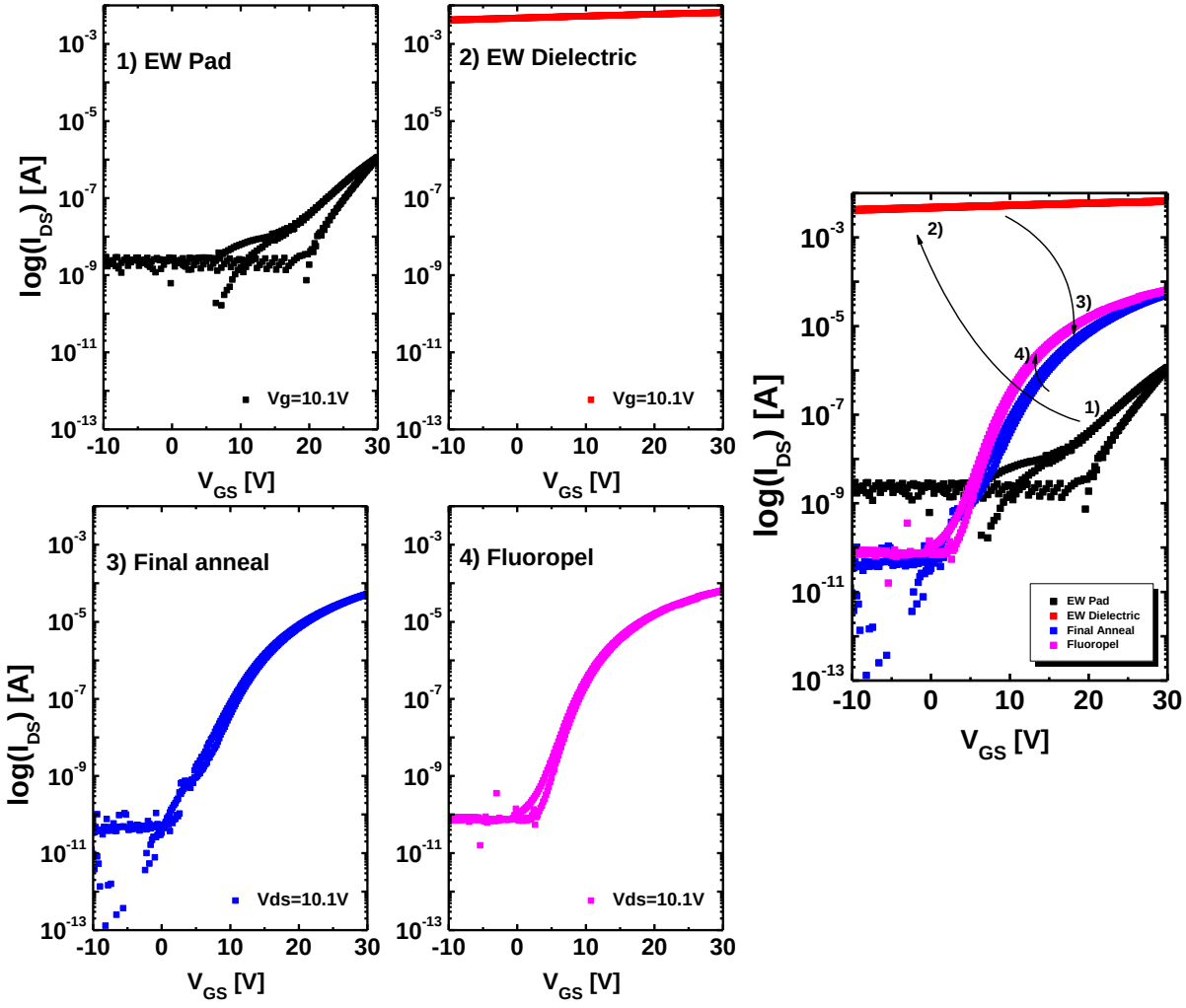


Figure 7-7. The transfer curves of 5×5 full integrated TFTs electrowetting device during the each process step: 1) after electrowetting electrode, 2) after electrowetting dielectric deposition, 3) after the final post annealing, and 4) before electrowetting test (hydrophobic layer coating and curing)

The additional fabrication issues of full integrated IGZO TFT electrofluidic device includes the peel off the metal electrode after annealing process and bubble like defects in the active (IGZO region) during the annealing process. Figure 7-8 demonstrates these two type issues after annealing process. We cannot clearly define these issues; however one reason for the electrode film peel-off is due to the stress accumulation of additional deposited film, and bubble like defect in active layer could result from vaporization of water or hydrogen during high temperature annealing process. Consequently, we adopt the additional annealing steps to reduce the film stress and remove the water or hydrogen vaporization in the process steps of electrowetting electrode deposition and after active wet-etching process. We finalize the all fabrication process step as shown in Appendix Ⅰand Ⅱ.

Figure 7-9 shows the change of electrical characteristics of IGZO TFTs after adopting the new process sequence to solve the above fabrication issues. We applied the active annealing after IGZO wet etch process to remove the adsorbed water on IGZO surface, and we applied a 2^{nd} annealing after the electrowetting electrode deposition to reduce the film stress. Finally, after all fabrication process completed, we applied the final post annealing. All annealing step is 350℃ 1hr in air atmosphere.

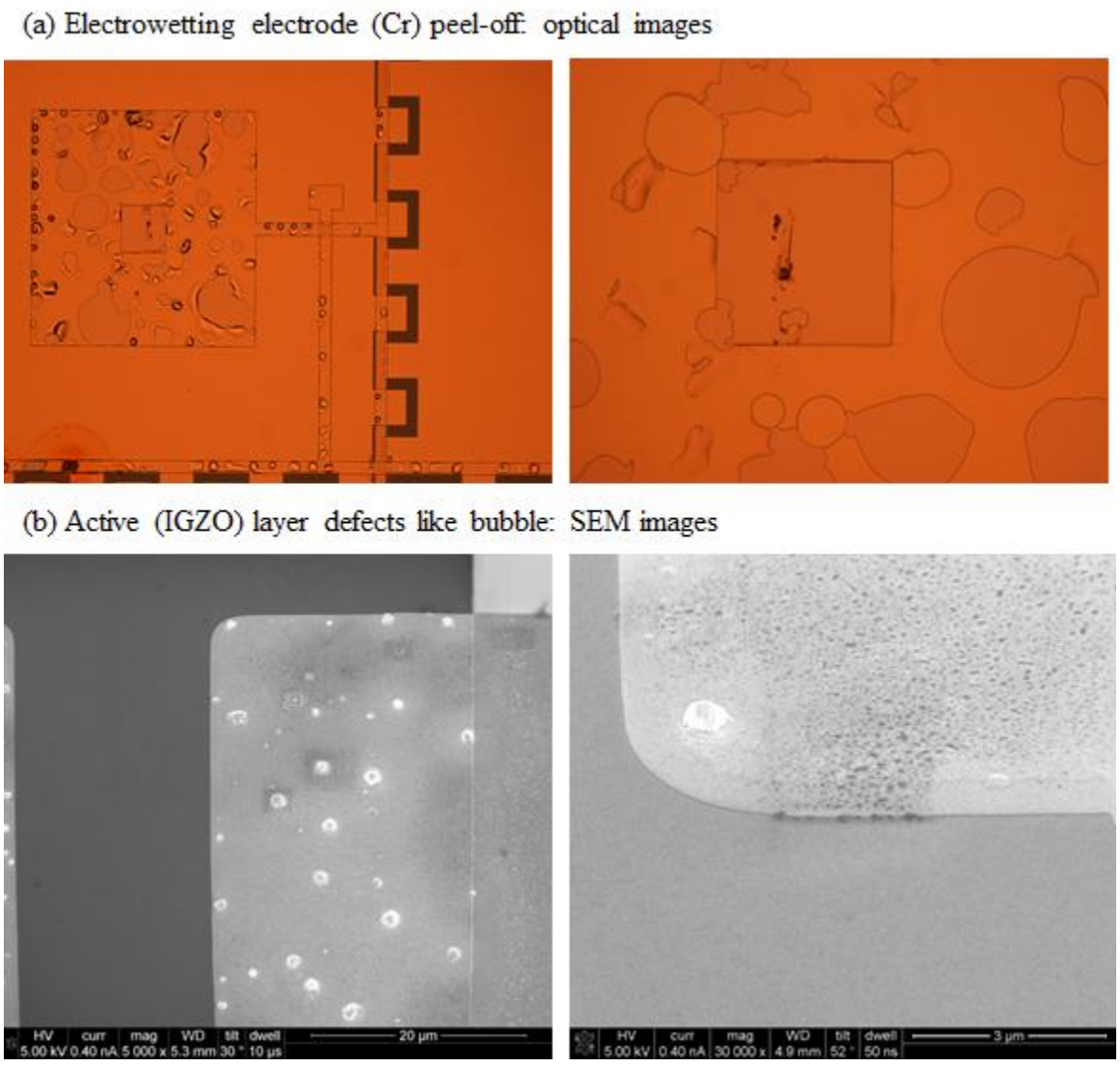


Figure 7-8. Fabrication issues of full integration TFTs electrowetting device

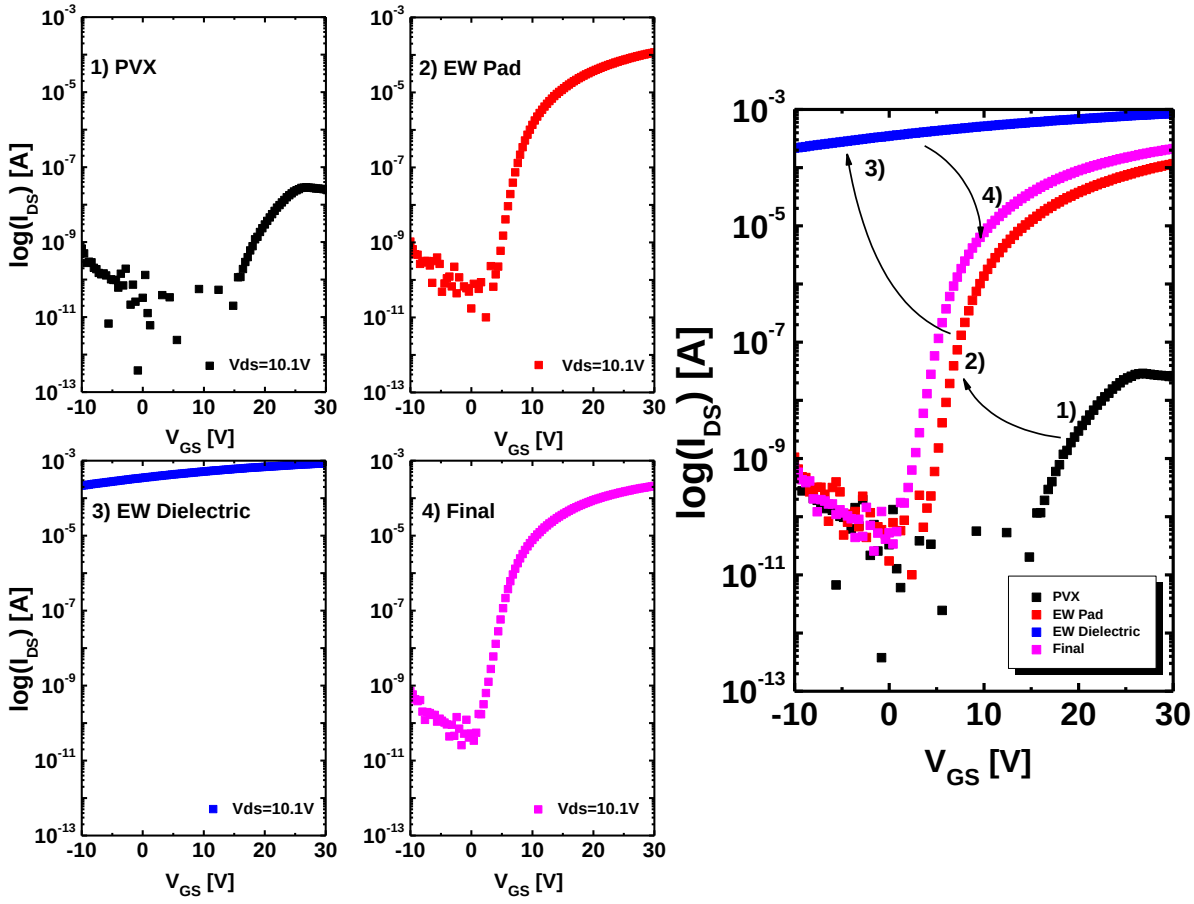


Figure 7-9. TFT characteristics change of finally optimized the fabrication process

The Figure 7-10 represents the uniformity of TFT transfer curves in our full integration TFT-electrofluidic array. The left side represents the different positions of the entire wafer (top, bottom, left, and right side) and right side shows the main array matrix TFTs (1×1, 1×2, 1×3 and so on). Table 7-1 shows the parameters and deviation of TFT characteristics as shown Figure 7-10. All TFTs have a small deviation in the TFT characteristics and good uniformity of the whole wafer area. Threshold voltage of these TFTs have 10.3~12.5V for the 8 TFTs on test elements group (TEG) and 9.8~12.0V for 6 TFTs in the main array. The subthreshold voltage swing (S.S) was 1.60~1.68 for the 8 TFTs on test element group (TEG) and 1.40~1.71 for the 6 TFTs on the main array. The subthreshold voltage swing is larger than before the passivation TFT characteristics. Additional processing after passivation layer affects the TFT characteristics. In the case of the field effect mobility the devices have 6.65~6.76 ㎠/Vs for the 8 TFTs on TEG pattern and 5.29~6.85 for the 6 TFTs in the main array.

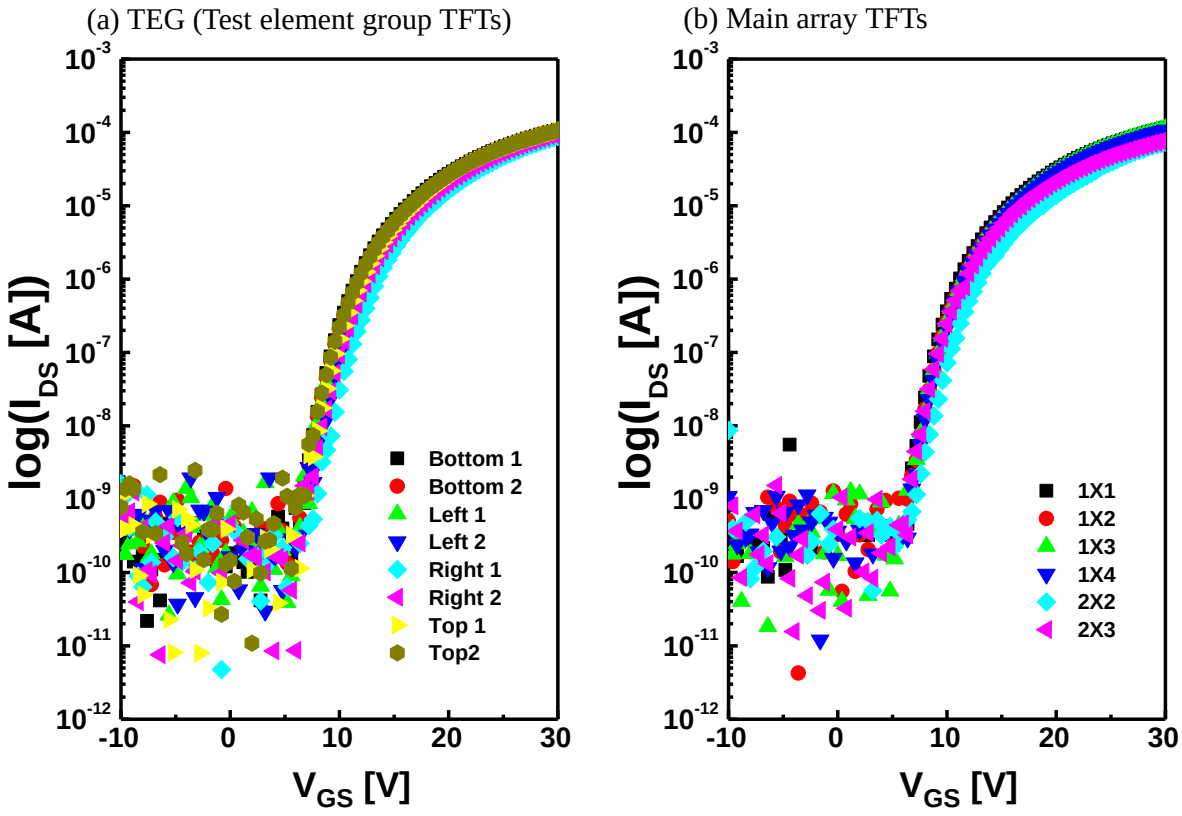


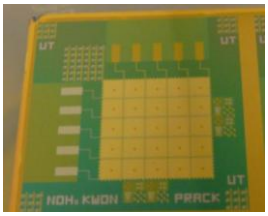
Figure 7-10. Transfer curves of different position in 16×16 high resolution electrowetting device

Table 7-1. Transfer characteristics of TEG 8TFTs and Main array 6TFTs

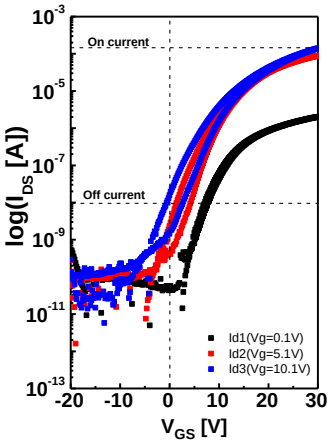
TFTs Characteristics	TEG 8 TFTs (W/L=50/20um)	Main Array 6 TFTs (W/L=50/20um)
Vth [V]	10.3~12.5	9.8~12.0
S.S [V/dec]	1.60~1.68	1.40~1.71
Mobility [㎠/V·sec]	6.65~6.76	5.29~6.85
I_{on} [A]	~1.0×10^{-4}	~1.1×10^{-4}
I_{off} [A]	~4.0×10^{-10}	~2.0×10^{-10}

At first we demonstrated the 5×5 full integration IGZO TFTs electrofluidic device. In this test we had successful droplet actuation with full integration TFT-electrofluidic device for only 1/4 of the 25 electrodes due to surface condition, external particles, and other fabrication issues. This sample had the TFT characteristics as shown Figure 7-11(b) which has ~2.0 10^{-4} [A] at V_{GS}=30V (TFT on state) and ~10^{-8} [A] at V_{GS}=0V (TFT off state). Figure 7-11(c) demonstrates the driving the droplet actuation of 5×5 full integration IGZO TFTs in electrofluidic device. Furthermore, after we optimize the whole process and solve the fabrication issues, we successfully fabricated a 16×16 high resolution full integration IGZO TFTs - electrofluidic platform. Figure 7-12 demonstrates the individual moving and horizontal channel moving using this electrofluidic platform.

(a) Final sample



(b) Final characteristics



(c) Driving the droplet actuation

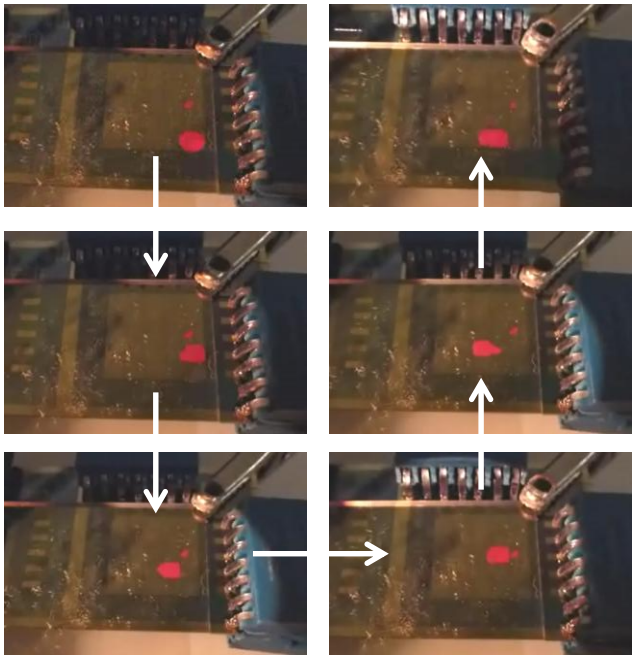
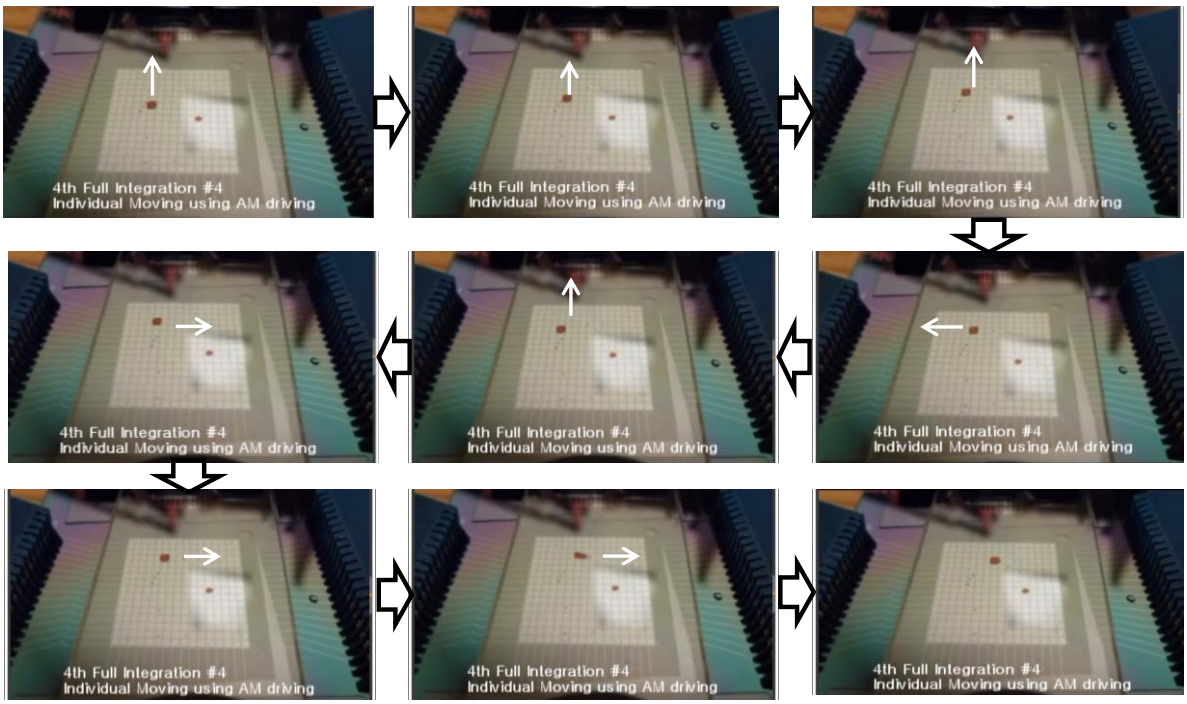


Figure 7-11. Driving the 5×5 full integration TFTs electrowetting device (a) Final sample picture, (b) Final TFT characteristics, and (c) Driving the droplet actuation

(a) Individual droplet moving in 16× 16 devices



(b) Horizontal signal scanning of droplet actuation

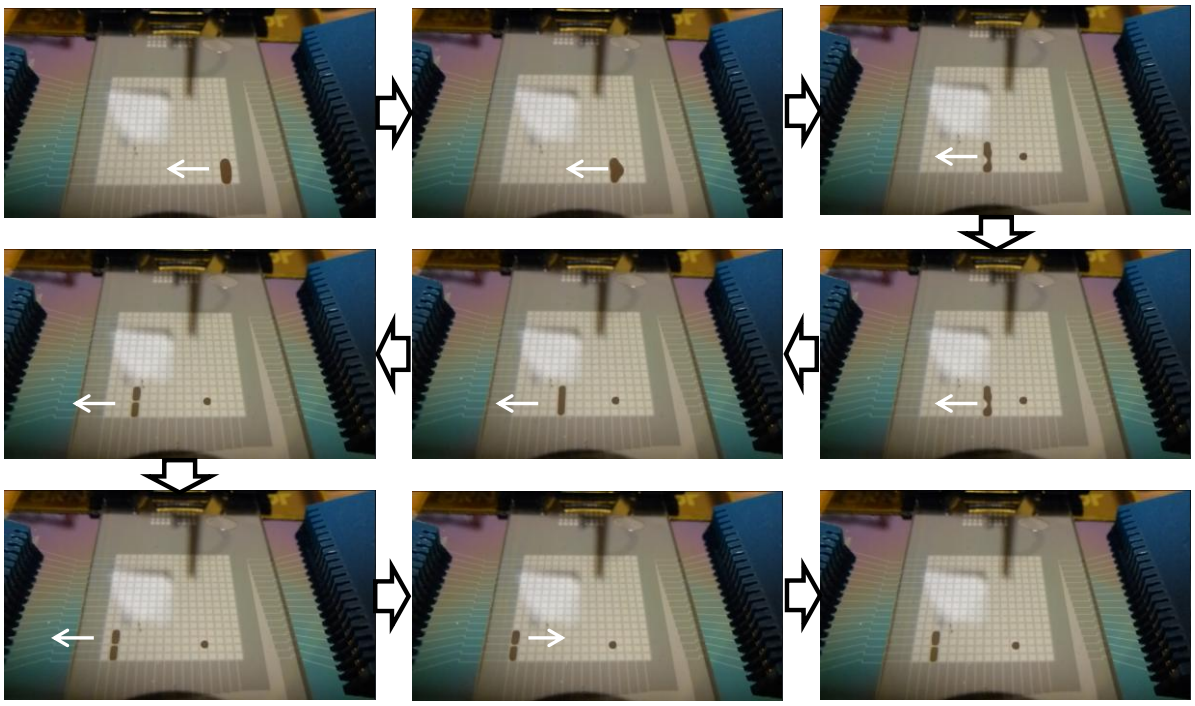


Figure 7-12. Driving the 16×16 full integration TFTs electrowetting device (a) individual droplet moving, (b) Horizontal channel moving

7.4 Conclusion

In summary, we optimized the entire process for full integration of IGZO TFTs with electrofluidic electrodes. After passivation layer we encountered the degradation of the TFT characteristics during the post passivation process, and fabrication issues such as peel-off film during high temperature process and bubble like explosion of the film on top of semiconductor layer. We adopted and optimized the our whole process to recover our TFT characterization using oxygen recess process on IGZO layer, additional annealing steps to release the film stress and remove the defects. Finally, we successfully demonstrated good TFT characteristics enough to control droplets and microfluidic channels. Finally, we demonstrated a high resolution 16×16 electrode microfluidic device with integrated IGZO TFTs.

*Acknowledgement

In this work, Dan Grissom in University of California at riverside helped to make microprocessor and user interface program to drive high resolution electrofluidic device. Joo Hyon Noh also helped to fabricate and test the electrowetting device. Philip Rack provided direction, funding of this research, discussion and motivation.

Chapter 8

Conclusions

In this dissertation the characterization of IGZO thin film transistors and fabrication of fully integrated IGZO TFTs for high resolution electrofluidic device were studied. We had success addressing the high resolution electrofluidic device for an addressable microfluidic electrowetting channel device with great promise for a real high-functional microfluidic device for applications in bio-synthesis, bio threat detection, and medical diagnostics using lab on a chip systems.

The channel resistance and contact resistance between a-IGZO layer and source/drain electrode was performed to characterize the a-IGZO TFTs. We confirmed the Ohmic contact between Ti/Au electrode and IGZO semiconductor layer. To apply as electronic switching device we confirmed that the channel resistance is higher than the contact resistance of the TFT on state. To generalize of a-IGZO deposition condition using rf magnetron sputter we investigated different sputtering conditions with the same IGZO and O_2 incorporation flux. We confirmed the same electrical characteristic of these TFTs. In addition, we verified the generalization of IGZO sputter condition using different sputter targets and compared the electrical properties of the resulting IGZO TFTs.

The characterization of different materials and processes for the passivation layer was studied in detail. We discovered several low temperature processes all which require and post annealing in air atmosphere. In case of PECVD SiO_2 we investigated the mechanism and roles of hydrogen and oxygen concentration using secondary ion mass spectroscopy, ellipsometry, and electrical

analysis. From this analysis we optimized the passivation layer and post annealing process of IGZO TFTs.

To develop the high functional electrofluidic device we performed the basic preliminary tests such as electrowetting phenomena, droplet actuation, and various electrowetting mechanisms (merge, splitting, and channel formation). The comparison of conventional and Laplace barrier electrowetting devices was performed by comparing the moving time, moving speed, and threshold voltage.

To reduce the control lines for high resolution lab on a chip device we studied the active matrix addressing method commonly used in flat panel displays. We investigated and simulated the pulse signal, capacitance, and resistance of electrofluidic device. For the effective addressing methods we performed the intermediate test connecting the IGZO TFTs and electrofluidic device. We demonstrated the functional droplet movement by active matrix addressing method connected IGZO TFTs.

Finally, we successfully demonstrated a high resolution (16×16) fully integrated IGZO TFTs electrofluidic device. We fabricated and optimized the whole process for microfluidic devices platform in this dissertation.

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Appendix Ⅰ: IGZO TFTs Run Sheet

Layer	Process	Equipment	Condition: Base Condition	Time
Initial Cleaning	Initial Cleaning	Spin Cleaner	DI wafer	-
Buffer	Buffer	PECVD (Oxford)	Recipe: Silicon Dioxide SiH_4/N_2O (85/157) Pressure 1000 mTorr Temp: 350C, 500nm	7' 15"
	Post Cleaning	Spin Cleaner	DI Water	-
Gate (Mask 1)	Cleaning		Nitrogen Gun	
	Gate Layer	Sputter	Cr: 150nm 200W, Bias 5W(126V), 5mTorr, Ar:25sccm	40'
	Cleaning		DI water	
	Gate Litho	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 4000rpm, 45sec PreBake: 115℃, 60sec Exposure: 10sec PostBake: 115℃, 60sec Develop: CD-26A, 60sec	-
	Gate Etch	Wet Etch	Cr-14S	3'30"
	Strip	Acetone/DI water		more than 10'
	Inspection	Optic Microscopy	All Main Array Check-up	-
	Post Cleaning		DI water	-
Gate Insulator	Gate Insulator	PECVD (Oxford)	Recipe: Silicon Dioxide SiH_4/N_2O (85/157) Pressure 1000 mTorr Temp: 350C, 500nm	1'27"
	Post Cleaning	Spin Cleaner	DI water	-
Active (Mask 2)	Cleaning		Nitrogen Gun	-
	Active layer (IGZO:50nm)	Sputter (Gun: #3)	IGZO 50nm pO2 40%, 5mTorr, Ar/O2=15/10, Power: 97W	42'22"
	Cleaning		DI water	-
	Active Litho	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 4000rpm, 45sec PreBake: 115℃, 60sec Exposure: 10sec PostBake: 115℃, 60sec Develop: CD-26A, 60sec	-
	Active Wet Etch	Wet Etch	BOE 10:1, Dilluted 100:1 (Total 1000:1)	30"
	Active Strip	Acetone/DI water	Ultrasonic	more than 10'
	Inspection	Optic Microscopy	All Main Array Check-up	-
S/D (Mask 3)	Cleaning		Nitrogen Gun	-
	S/D Layer	Sputter	Cr: 200nm 200W, Bias 5W(126V), 5mTorr, Ar:25sccm	50'
	Cleaning		DI water	
	S/D Litho	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 4000rpm, 45sec PreBake: 115℃, 60sec Exposure: 10sec PostBake: 115℃, 60sec Develop: CD-26A, 60sec	-
	S/D Etch	Wet Etch	Cr-14S	4'10"
	S/D Strip	Acetone & IPE	Ultrasonic	more than 10'
	Inspection	Optic Microscopy	All Main Array Check-up	-
PVX	Cleaning		DI water	-
	PVX Layer (PECVD SiO2)	PECVD (Oxford)	Recipe: OPT Silicon Dioxide Low Rate Temp: 200C, 400nm	6'47"
	Post Cleaning	Spin cleaner	DI water	-
	Inspection	Optic Microscopy	All Main Array Check-up	-

(Continued)

VIA (Mask 4)	Cleaning		DI water	-
	VIA	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 3000rpm, 45sec PreBake: 115℃, 60sec Exposure: 7sec PostBake: 115℃, 60sec Develop: CD-26A, 60sec	-
	VIA Hole Etch	Oxford RIE (Metal Chamber)	OPT SiNx ICP (SF6) Etch Rate: 26.23A/sec for 480nm (20% Over Etch)	3'03"
	VIA Strip	Acetone & IPE	Ultrasonic	more than 10'
	Ashing	Microwave	Recipe: Descum 2'30"	2'30"
	Inspection	Optic Microscopy	All Main Array Check-up	
Post ANL	Annealing	High Temp Micro Oven	400C 1hr	1hr
	Inspection	Optic Microscopy	All Main Array Check-up	
TFT Measure	TFT-IV	Probe station		-

Appendix Ⅱ: Full integration IGZO TFTs Electrowetting Device

Layer	Process	Equipment	Condition: Base Condition	Time
Initial Cleaning	Initial Cleaning	Spin Cleaner	DI wafer	-
Buffer	Buffer	PECVD (Oxford)	Recipe: Silicon Dioxide SiH_4/N_2O (85/157) Pressure 1000 mTorr Temp: 350C, 500nm	7' 15"
	Post Cleaning	Spin Cleaner	DI Water	-
Gate (Mask 1)	Cleaning		Nitrogen Gun	
	Gate Layer	Sputter	Cr: 150nm 200W, Bias 5W(126V), 5mTorr, Ar:25sccm	40'
	Cleaning		DI water	
	Gate Litho	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 4000rpm, 45sec PreBake: 115℃, 60sec Exposure: 10sec PostBake: 115℃, 60sec Develop: CD-26A, 60sec	-
	Gate Etch	Wet Etch	Cr-14S	3'30"
	Strip	Acetone/DI water		more than 10'
	Inspection	Optic Microscopy	All Main Array Check-up	-
	Post Cleaning		DI water	-
Gate Insulator	Gate Insulator	PECVD (Oxford)	Recipe: Silicon Dioxide SiH_4/N_2O (85/157) Pressure 1000 mTorr Temp: 350C, 500nm	1'27"
	Post Cleaning	Spin Cleaner	DI water	-
Active (Mask 2)	Cleaning		Nitrogen Gun	-
	Active layer (IGZO:50nm)	Sputter (Gun: #3)	IGZO 50nm pO2 40%, 5mTorr, Ar/O2=15/10, Power: 97W	42'22"
	Cleaning		DI water	-
	Active Litho	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 4000rpm, 45sec PreBake: 115℃, 60sec Exposure: 10sec PostBake: 115℃, 60sec Develop: CD-26A, 60sec	-
	Active Wet Etch	Wet Etch	BOE 10:1, Dilluted 100:1 (Total 1000:1)	30"
	Active Strip	Acetone/DI water	Ultrasonic	more than 10'
	Inspection	Optic Microscopy	All Main Array Check-up	-
Active ANL	Annealing	High Temp Micro Oven	400C 1hr	1hr
	Inspection	Optic Microscopy	All Main Array Check-up	
S/D (Mask 3)	Cleaning		Nitrogen Gun	-
	S/D Layer	Sputter	Cr: 200nm 200W, Bias 5W(126V), 5mTorr, Ar:25sccm	50'
	Cleaning		DI water	
	S/D Litho	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 4000rpm, 45sec PreBake: 115℃, 60sec Exposure: 10sec PostBake: 115℃, 60sec Develop: CD-26A, 60sec	-
	S/D Etch	Wet Etch	Cr-14S	4'10"
	S/D Strip	Acetone & IPE	Ultrasonic	more than 10'
	Inspection	Optic Microscopy	All Main Array Check-up	-
PVX	Cleaning		DI water	-
	PVX Layer (PECVD SiO2)	PECVD (Oxford)	Recipe: OPT Silicon Dioxide Low Rate Temp: 200C, 400nm	6'47"
	Post Cleaning	Spin cleaner	DI water	-
	Inspection	Optic Microscopy	All Main Array Check-up	-

(Continued)

VIA #1 (Mask 4)	Cleaning		DI water	-
	VIA	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 3000rpm, 45sec PreBake: 115℃, 60sec Exposure: 7sec PostBake: 115℃, 60sec Develop: CD-26A, 60sec	-
	VIA Hole Etch	Oxford RIE (Metal Chamber)	OPT SiNx ICP (SF6) Etch Rate: 26.23A/sec for 480nm (20% Over Etch)	3'03"
	VIA Strip	Acetone & IPE	Ultrasonic	more than 10'
	Ashing	Microwave	Recipe: Descum 2'30"	2'30"
	Inspection	Optic Microscopy	All Main Array Check-up	-
PVX ANL	Annealing	High Temp Micro Oven	400C 1hr	1hr
	Inspection	Optic Microscopy	All Main Array Check-up	-
EW Electrode (Mask 5)	Cleaning		Nitrogen Gun	
	EW Pad Layer	Sputter	Cr: 200nm 200W, Bias 5W(126V), 5mTorr, Ar:25sccm	50'
	Cleaning		DI water	-
	EW Pad Litho	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 4000rpm, 45sec PreBake: 115℃, 60sec Exposure: 7sec PostBake: 115℃, 60sec Develop: CD-26A, 60sec	-
	EW Pad Etch	Wet Etch	Cr-14S	4'10"
	EW Pad Strip	Acetone & IPE	Ultrasonic	more than 10'
	Post Cleaning		DI water	-
	Inspection	Optic Microscopy	All Main Array Check-up	-
EW Dielectric	EW Dielectric Layer (PECVD SiO2)	PECVD (Oxford)	Recipe: Silicon Dioxide SiH_4/N_2O (85/157) Pressure 1000 mTorr Temp: 350C, 500nm	4'21"
	Post Cleaning		DI water	-
	Inspection	Optic Microscopy	All Main Array Check-up	-
VIA #2 (Mask 6)	EW Hole	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 3000rpm, 45sec PreBake: 115℃, 90sec Exposure: 9sec PostBake: 115℃, 90sec Develop: CD-26A, 180sec	-
	VIA Hole Etch	Oxford RIE (Metal Chamber)	OPT SiNx ICP (SF6) Etch Rate: 26.23A/sec for 400nm (20% Over Etch)	**2'32"**
	EW Hole Strip	Acetone & IPE	Ultrasonic	more than 10'
	Inspection	Optic Microscopy	All Main Array Check-up	-
VIA #3 (Oxtgen recess) (Mask 7)	Cleaning		DI water	-
	VIA	Spinner Aligner (pressure mode)	PPR(w/ Primer) SPR3.0 Coating: 3000rpm, 45sec PreBake: 115℃, 60sec Exposure: 7sec PostBake: 115℃, 60sec Develop: CD-26A, 60sec	-
	VIA Hole Etch	Oxford RIE (Metal Chamber)	OPT SiNx ICP (SF6) Etch Rate: 26.23A/sec for 300nm (No Over Etch)	**1'55"**
	VIA Strip	Acetone & IPE	Ultrasonic	more than 10'
	Inspection	Optic Microscopy	All Main Array Check-up	-
Post ANL	Annealing	High Temp Micro Oven	400C 1hr	1hr
	Inspection	Optic Microscopy	All Main Array Check-up	-
TFT Measure	TFT-IV	Probe station		-
Fluoropel Coating	N2 Cleaning	N2 gun		-
	Fluoropel Coating	Dip coater		-
	Fluoropel Annealing	High Temp Micro Oven	150C Setting (Real 130C)	20'

VITA

Jiyong Noh received the B.S degree in ceramic engineering from Hanyang University, Seoul, South Korea, in 2002. He received the M.S degree in materials science engineering from Columbia University, New York, NY, USA, in 2006. From 2006 to 2009, he worked at AMOLED (Active Matrix Organic Lighting Emitting Diode) R&D center in Samsung Mobile Display, Gi-hueng, Kyunggi-do, South Korea, where he worked as thin film process engineer and research engineer for developing AMOLED display applied metal oxide semiconductor, low resistivity metallization, and transparent conductive films for high efficiency. He received the Ph.D degree in material science and engineering in 2013, Knoxville, TN, USA. His research interests include the characterization and fabrication of active matrix IGZO thin film transistors and an addressable microfluidic electrowetting channel device for application.