Reducing The Levelized Cost of Energy of Residential PV Inverters Through Dynamic Hardware Allocation

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I would like to dedicate this to my late father Sabi Tchayaou Gorowè

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Abstract

Renewable energy, such as wind and solar are becoming an integral part of world energy production. Photovoltaic (PV) systems are projected to constitute a large portion of the energy generation portfolio. Achieving a low-cost residential PV system will enable the wide adoption of solar energy throughout the USA. Although innovation in several areas is required to achieve this goal of a low-cost residential PV system, inverter reliability innovation is one key area that is essential. Present string inverters' lifetime is less than 15 years. Increasing their lifetime to 50 years will reduce the cost of operation and maintenance, increase energy yield, and drive down the levelized cost of energy (LCOE) for residential PV systems. Present-day solutions for increasing the inverter reliability focus on topologies that use the more-reliable film capacitors instead of electrolytic. However, following the elimination of electrolytic capacitors, further improvement of inverter lifetime requires consideration of the overall system architecture including power devices.

In this dissertation, a new topological and control scheme that allows dynamic hardware allocation (DHA) has been developed to address this challenge. In the proposed architecture, a common set of modules consisting of a pool of identical hardware resources dynamically shifts operation between active power filtering (APF) and line frequency inverter operation. Each module is used either as a buck type APF (with embedded energy storage) or a ZVS inverter phase leg, in each case controlled through a low-frequency current reference.

The benefit of this approach is multifold. First, inverter lifetime and reliability are increased because the pooled hardware resources are re-assigned in the event of a single failure of any element. Second, the modular nature of the system facilitates the use of high-reliability components, and allows for simple repair or maintenance through the replacement

of individual modules instead of requiring a complete inverter replacement. Third, the cycle-by-cycle operation of the DHA allows the use of a smaller total semiconductor area in the power stage compared to a traditional system.

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Chapter 1

Introduction

The system installation cost of solar photovoltaic (PV) in the United States has fallen by more than 60% in the last decade and is expected to further decrease in the future [1]. The cost reduction coupled with financial incentives in the form of tax credits has contributed to increasing the adoption of solar power in the U.S. This trend is expected to continue in the next decade as illustrated in Fig. 1.1. PV systems are classified into three categories: residential, commercial and utility-scale [2]. Residential PV systems' size range from 1 to 10 kW, while systems with power levels between 10 kW and 2 MW are considered commercial systems. Any system with a power level greater than 2 MW is considered a utility scale. According to the recent U.S. Solar Market Insight report published in [3], the total installed DC solar capacity in the U.S including residential, commercial, and utility is expected to quadruple, from approximately 100 GW in 2020 to more than 400 GW, in the next decade. Despite this optimistic prediction in the growth of solar, there is an opportunity for further cost reduction, and growth especially in the residential PV market.

Residential solar sales have exceeded all expectations in 2020 due to financial product innovation, increased interest in home improvements, and customers in areas prone to extreme weather events attempting to diversify their energy supply. As shown in Fig. 1.2, there was 3.2 GW of new PV capacity installed in 2020, up 11% from the previous year. This trend is expected to continue with a steady annual growth of 9% to 12%, surpassing 7 GW of installed capacity in 2030. As a result, the share of homes with solar will increase from

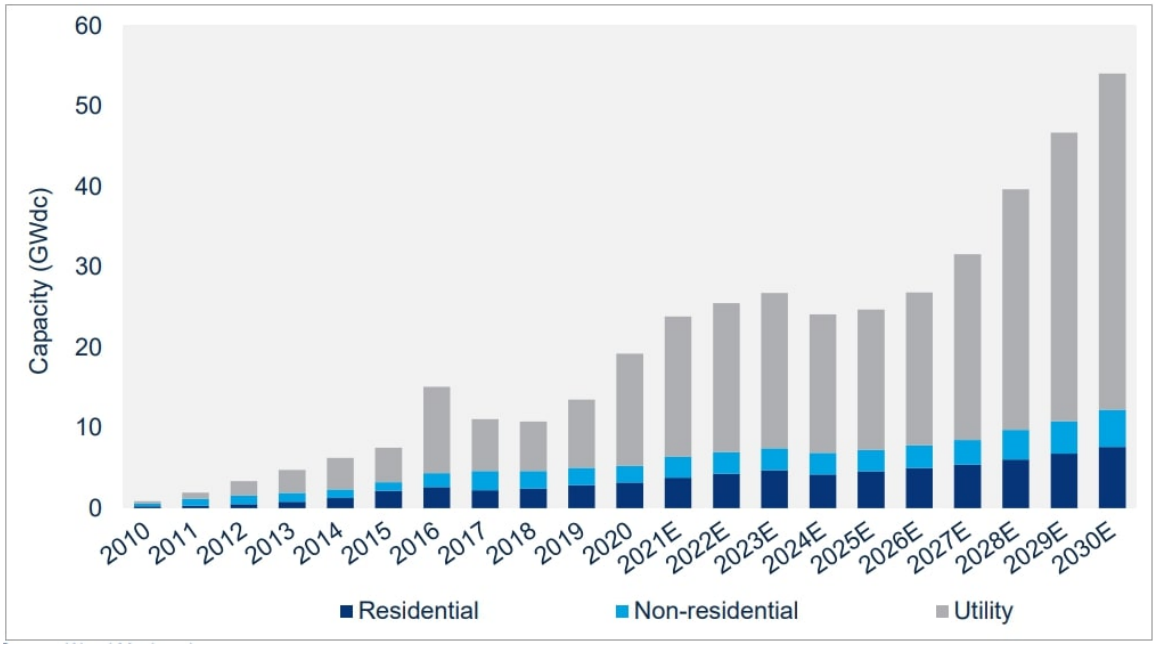


Figure 1.1: U.S. PV installations and forecast 2010-2030E [3].

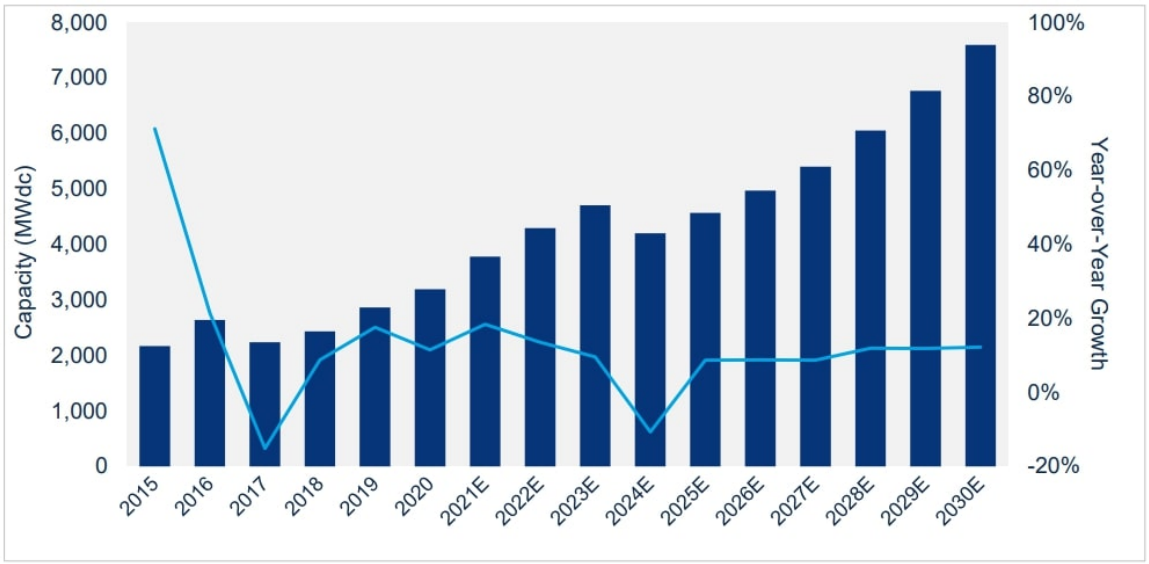


Figure 1.2: U.S. Residential PV installations and forecast 2015-2030 E [3].

4% in 2020 to 13.4% by 2030 [3]. However, these estimates only represent a small fraction of the full residential PV technical potential in the U.S.

Fig. 1.3 illustrates the predicted annual average technical potential for residential rooftop PV in the U.S. The National Renewable Energy Laboratory (NREL) estimates that installing PV at the time of roof replacement and as part of a new home construction process provides a significant opportunity for cost savings and market growth. With an estimate of 3.3 million homes per year to be built or require roof replacement between 2017 and 2030, the residential PV technical potential is roughly 30 GW per year [4]. This is a significant market opportunity for residential PV that can contribute to the U.S. goal of reaching carbon neutrality by 2050. Achieving such an objective presents both technical and business challenges. As previously mentioned, business innovation has fueled most of the solar growth while technical innovation including power electronics has lagged. Current residential inverters are unreliable and have received few technical improvements since their invention. Their limited lifetime represents one key contributor to the high cost of solar power systems [5]. Thus, designing a highly reliable inverter is essential to reduce the lifetime cost of the solar system and enable its wide adoption.

Increasing inverter reliability has become a priority not only for the industry but for DOE as well. To catapult the innovation in this sector, the DOE solar energy technologies office (SETO) in their recent funding opportunity announcement for the fiscal year 2021 for photovoltaics and concentrating solar-thermal power funding program seeks to invest in projects that will increase the PV system useful life to 50 years while lowering the cost of energy. SETO is the branch of the DOE that drives innovation in the area of renewable energy including photovoltaic by investing in early-stage research and development. According to information released by the DOE, the project should aim to improve overall PV system components hardware including inverters through increased durability [6]. In addition, with the early success of the SETO Sunshot initiative to reduce the cost of residential, commercial, and utility-scale PV by 75% by 2020, the DOE has set even more aggressive targets to be achieved by 2030 [4].

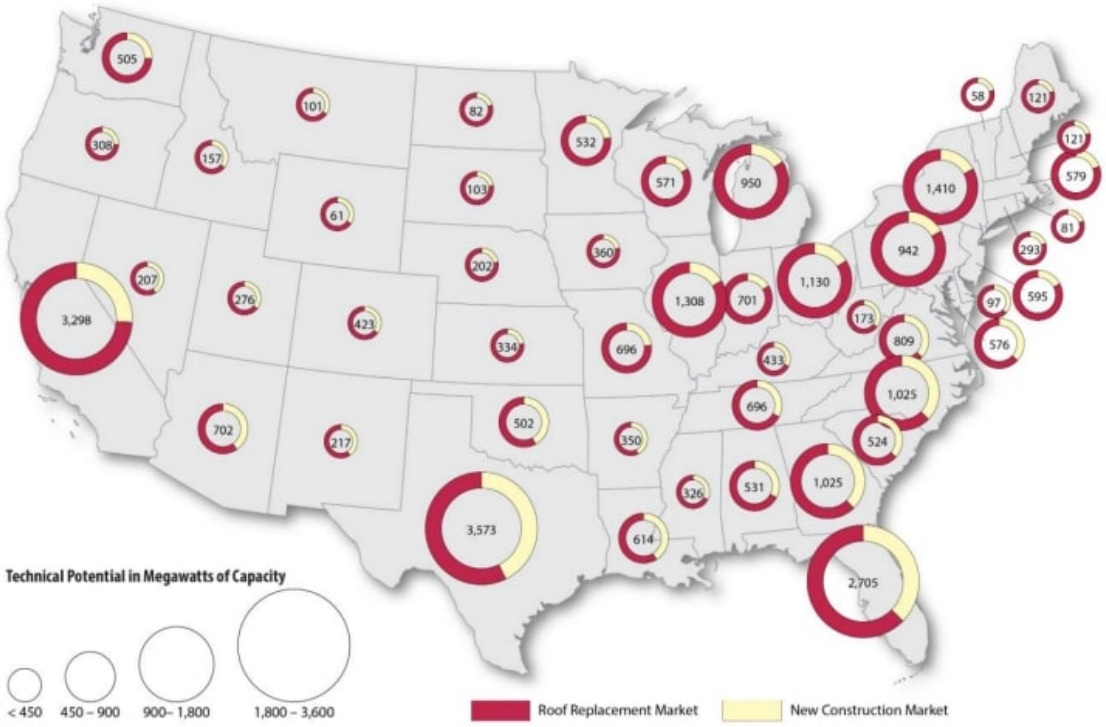


Figure 1.3: Annual average technical potential for residential rooftop PV at time of roof replacement and new construction projected between 2017 and 2030 [4].

1.1 Levelized Cost of Energy for Photovoltaic System

Generally expressed in a dollars-per-kilowatt hour ($/kWh) or dollars-per-megawatt hour ($/MWh), the Levelized cost of energy (LCOE) is the present value assessment of a PV system's total lifetime costs and the lifetime energy yield from a power generation system. The energy yield is affected by the overall system efficiency while the cost is affected by initial investments, and the ongoing operation and maintenance cost of the system [7]. Thus, any factor that leads to lower the total lifecycle costs or greater energy output over the chosen analysis period contributes to lower LCOE. It is the yardstick that is often used to evaluate and compare the impacts of new technology [8]. It is used as the metric to assess the impact of a particular technology in comparison to others. The DOE uses LCOE as a benchmark to achieve certain technology targets. For instance, according to DOE, from 2010 to 2017, LCOE for residential PV declined from 52 ¢/kWh to 15 ¢/kWh and expect the cost reduction for PV to continue through a host of innovative approaches in different sectors such as technology, business, and finance [4]. Through its SunShot 2030 initiative described in [9], DOE has laid out a pathway to reduce the average unsubsidized LCOE of utility-scale PV to 3 ¢/kWh, 4 ¢/kWh for commercial and 5 ¢/kWh for residential rooftop PV by 2030 which is illustrated in Fig. 1.4. Achieving these goals is expected to enable greater levels of PV deployment, more than double the projected amount of electricity demand met by solar and make the solar electricity market competitive with fuel-based electricity without subsidies.

From the inverter technology standpoint, two angles can contribute to lowering the LCOE. First, improvement in efficiency can help increase the lifetime energy supplied to the load. Second, increases in inverter reliability contribute to reducing the lifetime operation and maintenance cost of the system. The survey of the literature presented in Chapter 3 shows that most of the inverter design trend so far has been toward higher efficiency and power density. On the other hand, the design for high reliability has been lagging behind that of efficiency and has generally been focused on replacing the electrolytic capacitor with the more reliable film capacitor through the use of the active power filter technique. Although efficiency improvement contributes to lowering the LCOE, its incremental impact on LCOE

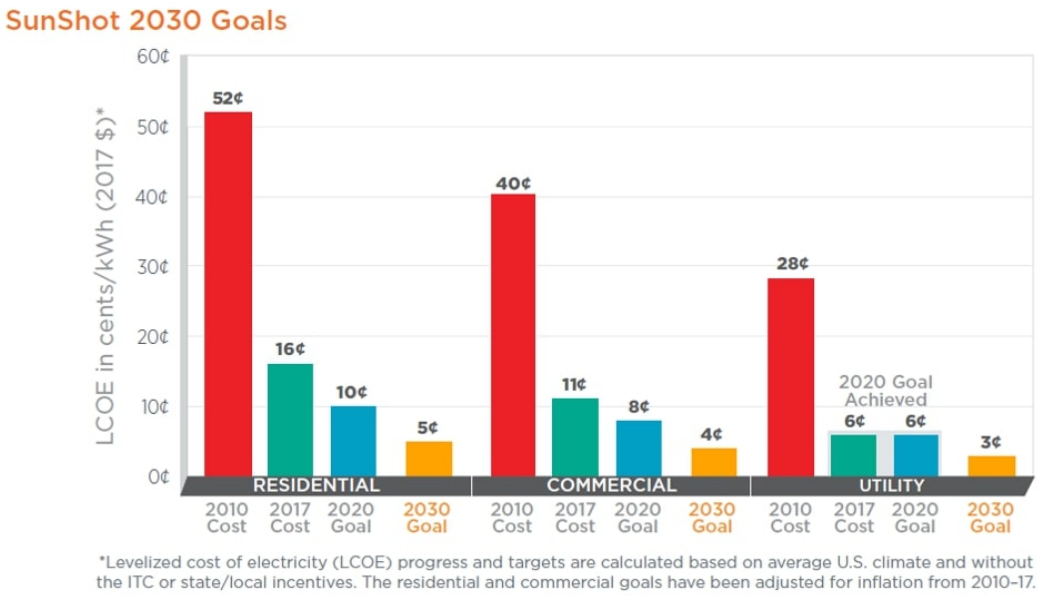


Figure 1.4: LCOE values and Sunshot PV goals for residential, commercial and utility-scale [9].

is minimal for residential PV systems. According to [10], its impact is significant for utility-scale systems. Thus, efficiency improvement alone is not enough to meet the SETO LCOE target for the next decade.

1.2 PV Inverter Configuration

Power inverters are the essential electronics that convert direct current (DC) from solar panels into alternating current (AC) that powers electrical loads in homes or flows to the utility distribution grid. They are the workhorse of PV systems. They are generally classified into four categories depending on their configuration.

First, a central inverter configuration, illustrated in Fig. 1.5(a), has the output of a PV array consisting of paralleled string connection of PV panels all connected to one inverter. It processes all the power that is fed to the grid and uses a centralized maximum power point tracking (MPPT) control. This type of inverter structure is simple, highly efficient, and cost-effective, but suffers from energy losses due to module mismatch and the centralized MPPT. It also has limited reliability given that the entire system depends on one inverter. Despite these drawbacks, it is still the configuration of choice for commercial and utility-scale PV applications [12, 13]. Second, a modular version of the central inverter, denoted as a string inverter is shown in Fig. 1.5(b). It consists of series-connected solar panels tied in a string individually connected to an inverter. The PV string can be connected in a parallel connection of different inverters in the case of a multi-string configuration. This setup is cost-effective but results in the reduced power production of the string if any individual panel is shaded. Next, AC module inverters, also denoted microinverters, are depicted in Fig. 1.5(c). It is made up of small inverters at the panel level, where the power is processed locally and connected to the grid directly. This configuration allows each panel to operate at its optimal power point, which is better optimized than in the case of String inverters. Also, the modular nature of this configuration allows for easy modification of the system and the shading of any panel does not affect the power processed by the other panels. On the other hand, microinverters have a high cost per kW when compared with other inverters. Lastly, DC-module inverters, shown in Fig. 1.5(d), combine the characteristics of microinverters and

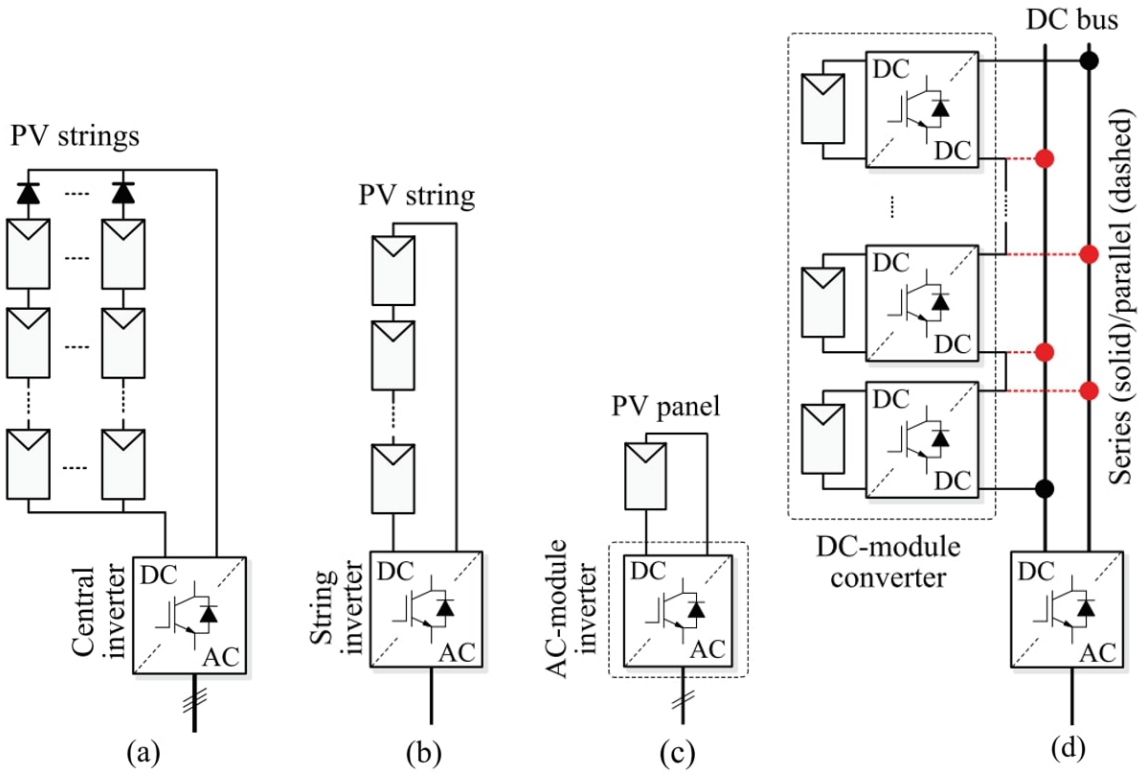


Figure 1.5: PV inverter configurations: (a) Central inverter, (b) String inverter, (c) AC-module inverter, (d) DC-module string inverter [11].

a string inverter. It uses DC optimizers, which is a DC-DC stage at the panel level, for power point tracking and a single-string inverter for AC conversion. It has all the advantages of microinverters with slightly lower cost and better efficiency [11].

Both microinverters and DC power optimizers are module-level power electronics (MPLE) and have become the dominant inverter configuration of choice in the U.S. for residential PV applications. As depicted in Fig. 1.6, MPLEs accounted for 86% of the U.S. residential market share in 2018 [1]. This wide adoption of MLPEs has also been driven by changes to the National Electric Code (NEC) in 2017 requiring a rapid shutdown at the module level for rooftop PV systems. They provide an optimized design solution at the module level that makes them more reliable and safe when compared with other inverters.

1.3 Challenge and Motivation

A common design goal for any power electronic converter is to maximize efficiency, power density, and reliability at a minimal cost. With the recent advancements in power semiconductor technology such as Gallium Nitride (GaN) and Silicon Carbide (SiC), the general trend over the years for PV inverters has been towards increasing efficiency and power density. For instance, the state-of-the-art inverters today have been able to reach a peak power efficiency of 99% and achieve a power density of 243 W/in^3 [14, 15, 16]. Despite these achievements, PV inverters are still one of the most fragile elements in a PV system, contributing to many downtimes [17, 11, 18]. According to maintenance data from 144 operational PV systems recorded by Sandia National Laboratory (SNL) and reported in [5], inverters contributed to the greatest amount of faults and failures events as shown in Fig. 1.7. They made up about 70% of all events within all of their surveyed PV system portfolio of 144 systems with a total capacity of 780 MW$_{DC}$.

A PV inverter failure can significantly affect the instantaneous energy production, thereby negatively affecting the O&M costs and the lifetime energy yield of the system [19]. Today, the commercially available PV modules are typically offered with a 25-year performance warranty and constitute the most reliable component of a PV system [20]. Thus, it has become a priority for the PV industry to improve the reliability of PV inverters to at least

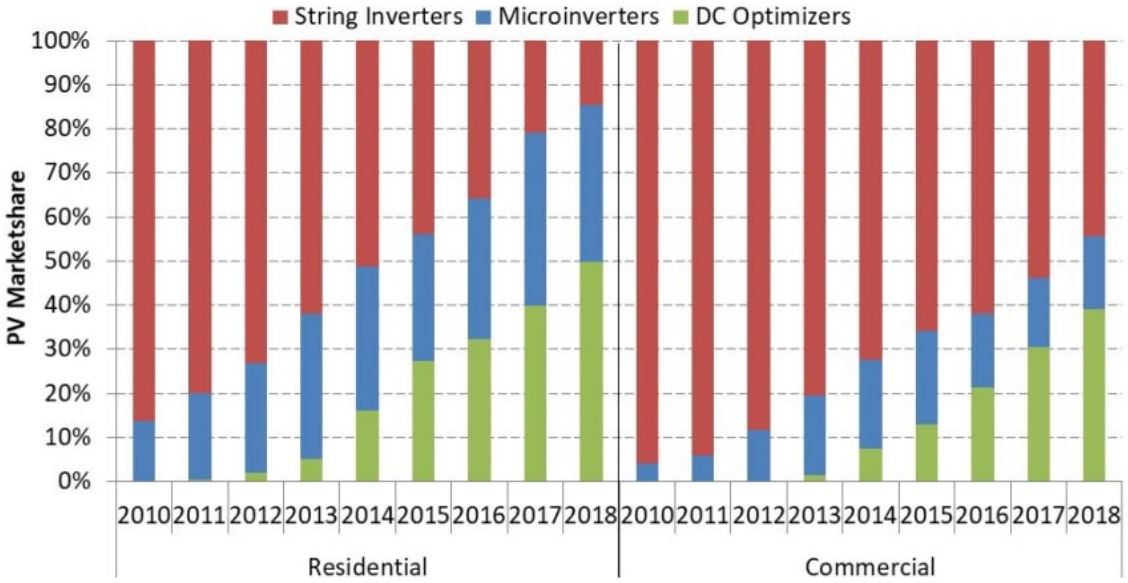


Figure 1.6: U.S. residential and commercial inverter market from 2010 to 2018 [1].

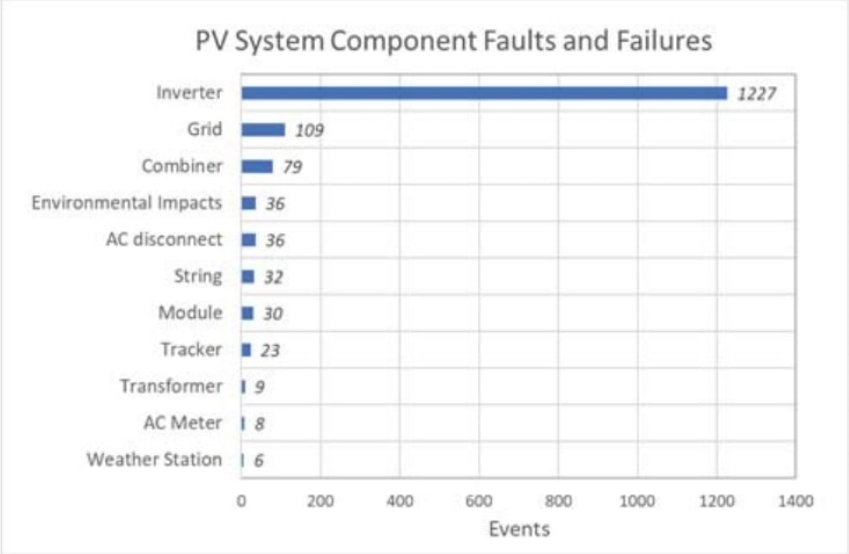


Figure 1.7: Summary of number of fault and failures across a portfolio of 144 PV Systems [5].

match the lifetime of PV modules [21]. With the projected growth of residential solar power for the next decade, there is an urgent need to design highly reliable PV converters to further enable the growth of residential solar power in the U.S. This will enable the U.S. to capture a significant part of its market potential of roughly 30 GW per year while achieving the DOE 2030 Sunshot targets of 5 ¢/kWh LCOE for residential PV [4].

Many innovations have to take place to reach the DOE 2030 LCOE targets, but Fig. 1.8 shows one potential route, which relies on significant improvements in module price reduction, efficiency increase, system reliability, O&M costs, hardware, and labor costs, and financing rates [9]. Although progress in one individual metric is not sufficient to reach the DOE SunShot goals, an early model of a 5.6 kW residential system developed by NREL shows that an inverter-related improvement such as doubling the inverter lifetime from 15 years to 30 years would lower LCOE by 1.7 ¢/kWh. Reliability improvements will decrease O&M cost from \$20 to \$7/kW$_{DC}$ contributing to 10% lower LCOE [10, 4]. Furthermore, according to reliability and repair analysis performed in [5], improving the lifetime of the PV inverter so that it does not need to be fully replaced during the lifetime of the system has a larger impact than efficiency on reducing LCOE. Achieving the high reliability of PV inverters to match that of PV modules is essential to lower the cost of renewable energy, suggesting a growing need for further research to improve the inverter's lifetime.

According to [21], the reliability approaches that the next generation of PV inverters should adopt include modular and redundant topologies, new energy buffering techniques, and high-temperature semiconductor devices. In addition, design for reliability has to be integrated into the design phase of the inverter in addition to efficiency and power density metrics [11, 22, 23, 24].

The work in this dissertation focuses on increasing the reliability/lifetime of grid-connected single-phase string inverters for residential PV applications. Using the design for reliability approach and a design optimization technique, a new inverter architecture control, and operation are developed. The new inverter provides a paradigm shift in the way PV inverters work and can be extended to other applications.

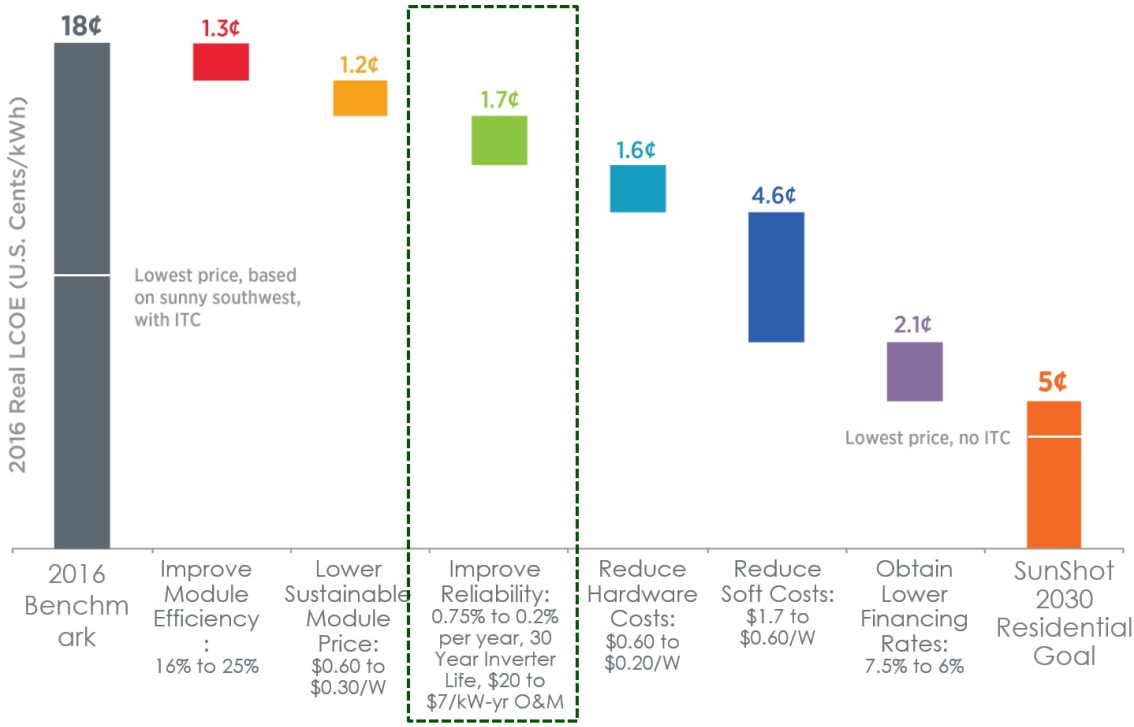


Figure 1.8: Progress toward an LCOE target of 5 cents per kW for 5.6 kW residential systems [9].

Chapter 2

Overview of Single-Phase Transformerless PV Inverters

PV inverters use either line-frequency or high-frequency transformers to provide galvanic isolation between the DC and AC side. However, line frequency transformers are large, bulky, and heavy, making the overall volume of the system large. On the other hand, the high-frequency transformers are smaller in size, but require several power stages, reducing the system efficiency and increasing the complexity. Thus, transformerless inverter topologies have been developed to offer the advantages of high efficiency, high power density, and low-cost [25]. However, the lack of galvanic isolation in transformerless inverters introduces a common mode leakage current that flows through the parasitic capacitor between the PV array and ground when a variable common-mode voltage is generated. The CM ground current causes an increase in current harmonics, high losses, and safety issues [26, 27, 28]. Thus, the choice of topology and type of modulation influences the size of the output filter components and EMI filter requirements, greatly impacting the overall converter efficiency, power density, and safety. This chapter discusses some of the classic transformerless single-phase inverters including the H-bridge, H5 of SMA, H6, HERIC of Sunways, and neutral-point-clamped inverters. The inverter power stage is classified into two groups based on the common full-bridge topology and the number of active switches in the circuit. Next, various power pulsating buffer (PPB) techniques are reviewed and categorized as passive or active depending on the type of technology used.

2.1 Leakage Current Generation in Transformerless Voltage Source Inverters

The common-mode leakage current is one of the major issues in transformerless voltage source inverters (VSI) and can cause personal safety problems, increase system losses, affect the grid-connected current quality, and increase the conducted and radiated EMI [25]. In the structure depicted in Fig. 2.1, the PV panels are directly connected to the grid providing a direct path for the leakage ground current (I_{G-PV}) to flow through the parasitic capacitance (C_{G-PV}) formed between the surface of the PV and the grounded frame [12]. When a person touches the surface of the PV array, the ground current can flow through the human body, causing personal injuries if it exceeds a certain level. Thus, electrical codes and standards require a rapid shutdown of the system within a given time for any sudden leakage current that goes above a certain threshold. For instance, according to the German VDE 0126-1-1 electrical code, a leakage current over 300 mA must trigger a breaker within 0.3 sec [29].

In addition to the suppression of the leakage current, the grid-connected PV inverters should satisfy other electrical specifications such as total harmonic distortion (THD), second harmonic power buffering, and keeping the conducted and radiated EMI within the FCC class B standards. A brief summary on different grid codes and standards for grid-connected PV systems is illustrated in Fig. 2.2 [30]. For instance, in most of the surveyed countries, the THD has to be kept below 5%. The second harmonic ripple power from the AC side results in undesirable low-frequency ripple on the DC-link voltage and current. The undesirable ripple causes system performance degradation, reducing the maximum peak power tracking (MPPT) efficiency of the PV panels [31]. Also, for many applications, inverters must meet FCC Part 15B standards for both conducted and radiated emissions. Different modulation strategies of the inverter power stage would yield different common-mode (CM) and differential-mode (DM) voltage waveforms, leading to different EMI filter requirements [32]. The CM ground current causes an increase in current harmonics, high losses and safety issues [26, 27, 28]. Thus, the choice of topology and type of modulation would yield small or large output filter components and EMI filter requirements, impacting the overall converter efficiency and power density.

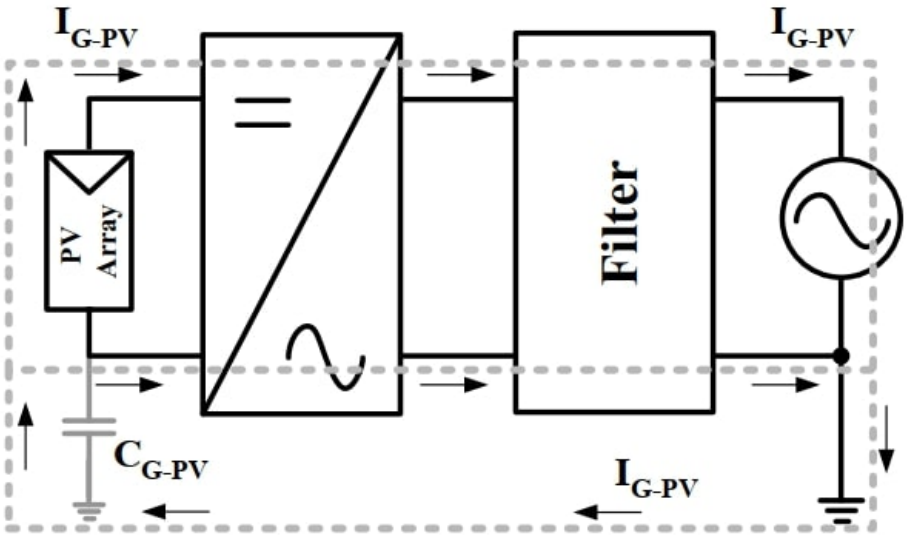


Figure 2.1: Transformerless PV system showing the parasitic capacitance between the PV and the grounded frame of the array and the path of the alternating ground leakage current [12].

Standard No.	Publication Origin	THD	DC Current Injected	Grid Frequency (f_g) Range (Hz)	Power Factor
IEEE 1547 [17]	USA (IEEE)	Less than 5%	<0.5% of rated output current	57 ~ 60.5	0.9 to 0.97
IEEE 929-2000 [20]	USA (IEEE)	Less than 5%	<0.5% of rated output current	59.3 ~ 60.5	> 0.85
IEC 61727 [28]	Swiss (IEC)	Less than 5%	< 1% of rated output current	49 ~ 51	> 0.90
AS4777 [52]-[54]	Australia	Less than 5%	0.5% of rated output current per phase	48 ~ 52	0.8 to 0.95
EN 61000-3-2 [22]	England	Less than 5%	< 0.22A corresponding to a 50 W half-wave rectifier	47.5 ~ 50.2	NA
EREC G83 [21]	England	Less than 5%	0.25 % of AC current rating per phase	49 ~ 51	0.95
VDE 4105 [18]	Germany	Less than 5%	< 1 A; max. trip time 0.2 s	47.5 ~ 51.5	0.89 to 0.95
BDEW [23]	Germany	Less than 5%	NA	47.5 ~ 51.5 (-5% ~ +3%)	0.95
GB/T 19964-2012 [24]	China	Less than 5%	< 1% of rated output current	48-50.5	0.95
JEAC 9701-2012 [25]	Japan	Less than 5%	NA	47.5 ~ 51.5 (Eastern Japan) 57 ~ 61.8 (Western Japan)	0.9 to 0.95

Figure 2.2: Grid connected PV system standards and grid codes [30].

2.2 Full-Bridge Based Inverters

Although there are many topologies used to implement a single-phase inverter, the traditional full-bridge architecture depicted in Fig. 2.3 forms the basic building block of many transformerless single-phase inverter designs. It is simple to implement and allows for different modulation schemes to generate a sinusoidal voltage at the output. There are several modulation techniques used to drive the inverter; two common ones are unipolar and bipolar modulation. In the case of bipolar modulation, both phases are switched at high frequency. Switches S_1 and S_4 are switched together at high switching frequency, and complimentary to S_2 and S_3. As shown in Fig 2.4b, the bipolar modulation inherently results in a constant CM voltage V_{CM} and has almost a nonexistent high-frequency CM noise. Furthermore, this switching scheme yields a large ripple across the output filter inductor and low efficiency due to increased switching loss. In the case of unipolar modulation, there are several methods of achieving this type of modulation. The two most common ones are switching S_1 and S_3 at high frequency, while the remaining switches (S_2, S_4) on the other phase leg operate at the line frequency. Another way to achieve the same thing is to switch both legs at the same high frequency with a 180° phase shift in between them. This switching method has the advantage of low switching loss; however, it has a significant distortion of the output current at the zero crossing as well as significant CM noise [33, 34]. The unipolar modulation yields a pulsating common-mode voltage V_{CM} as depicted in Fig 2.4a, contributing to an increased CM noise and leakage current.

The main advantage of the full-bridge inverter is its simplicity and depending on the type of modulation used, it would result in minimal ground leakage current. The unipolar switched inverter has the advantage of low switching loss; however, it has a significant distortion of the output current at the zero crossing as well as significant CM noise. In contrast, the bipolar switched inverter has an almost non-existent high-frequency CM noise and zero crossing output current distortion, but it has the disadvantage of low efficiency due to increased switching loss. To take advantage of the high efficiency of the unipolar switched transformerless inverters while mitigating the issue of leakage currents, switched topologies such as the H5, H6, and HERIC have been introduced.

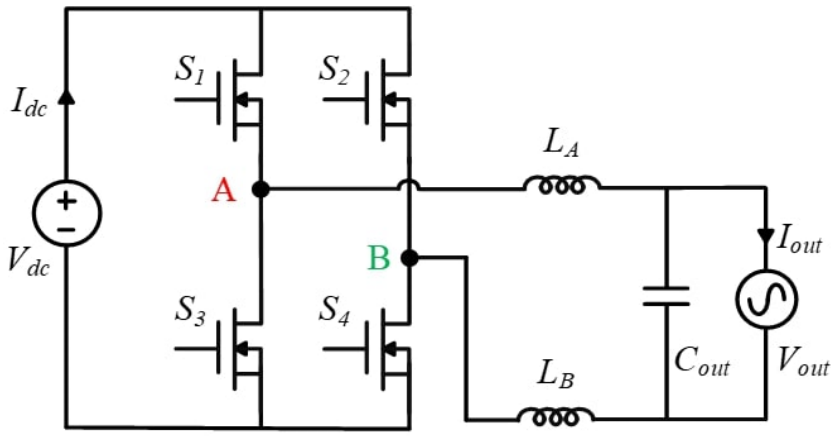
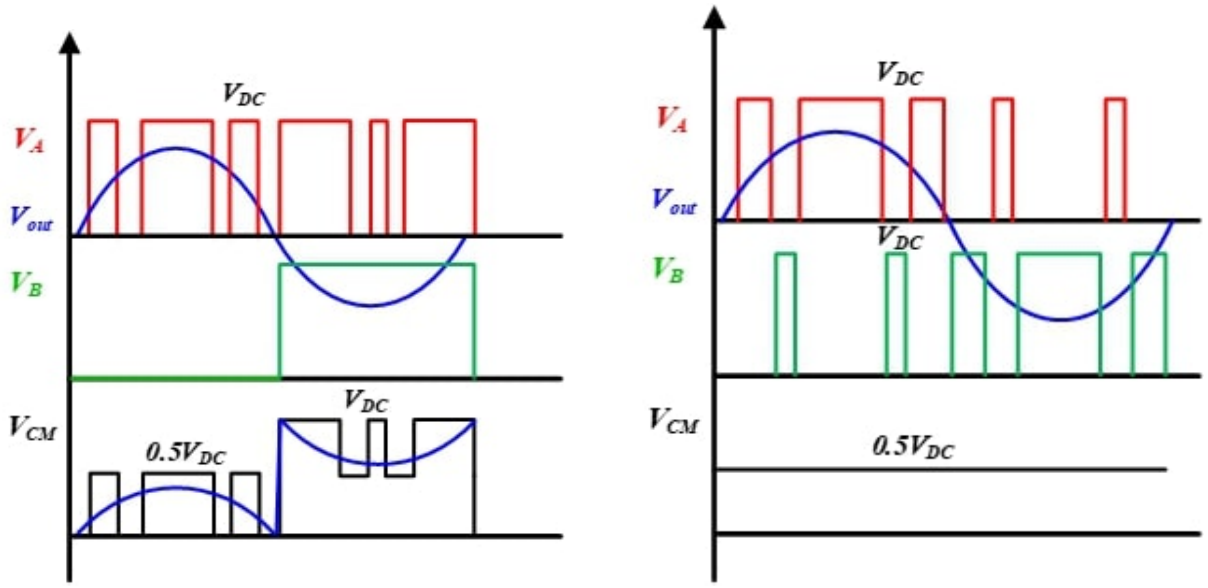


Figure 2.3: Full bridge inverter topology.



(a) Unipolar modulation waveform **(b)** Bipolar modulation waveform

Figure 2.4: Switch node and common mode voltage waveform.

2.2.1 H5-Inverters

From the full-bridge topology shown in Fig. 2.3, an active switch S_5 is introduced between the positive DC terminal and the H-bridge module acting as a decoupling network. The resulting topology shown in Fig. 2.5 is known as the H5-Inverter and has been widely used in residential single-phase PV applications [35]. The DC decoupling network provides a disconnection from the AC side during the zero-voltage operation, which minimizes or eliminates leakage current that flows through the parasitic capacitance of the PV ground. To generate the zero-voltage level, the upper switches, S_1 and S_3, conduct while the blocking switch, S_5, and the lower switches S_2 and S_4, are turned OFF. Thus, the PV panel is disconnected from the AC side during the zero-voltage level operation. The minimal number of components in the H5 inverter and its inherent ability to minimize ground leakage current has made it a prevalent choice for high-power density design. However, it has high conduction losses due to the fact that the current must flow through three switches in series during the active phase. In addition, this configuration is prone to shoot-through issues similar to traditional full-bridge PWM inverters because the three active switches are series-connected to the DC bus [36].

2.2.2 H6-Inverters

These are a category of inverters with two additional switches on the DC side of the H-bridge or the AC side between the full-bridge module and the filter inductors. Fig. 2.6 shows the basic H6 topology. In this topology, there are two possible decoupling modes between the PV and the AC grid side during the zero-voltage level operation: S_1, S_3 ON or S_2, S_4 ON. Although the redundant switching pattern enhances the modulation flexibility, the basic H-6 inverter has high conduction losses because there are now four switches that are ON during the energy transfer phase from the PV to the grid [29].

To address the high conduction loss issue, many improved versions of the basic DC side decoupled H6-inverter have been proposed to address the high conduction loss issue. Fig. 2.7 shows an example of a family of improved H6-inverters. The operation of those two topologies is similar. The three switches S_5, S_1, S_4 conduct during the positive half cycle and only two switches conduct during the entire negative half cycle: S_2, S_6 or S_2, S_4 depending on the

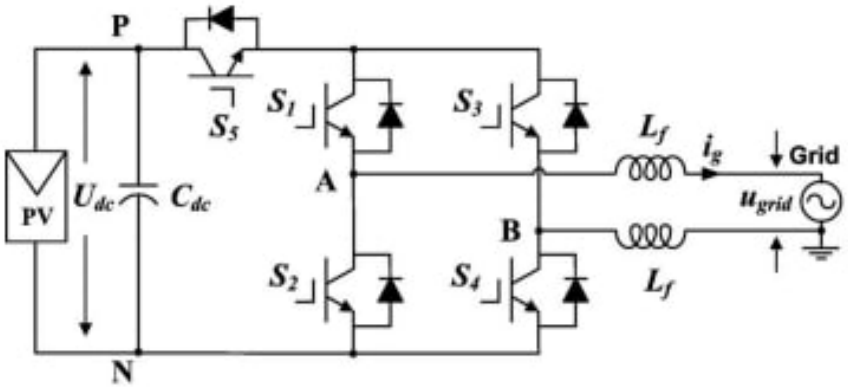


Figure 2.5: H5-Inverter topology [35].

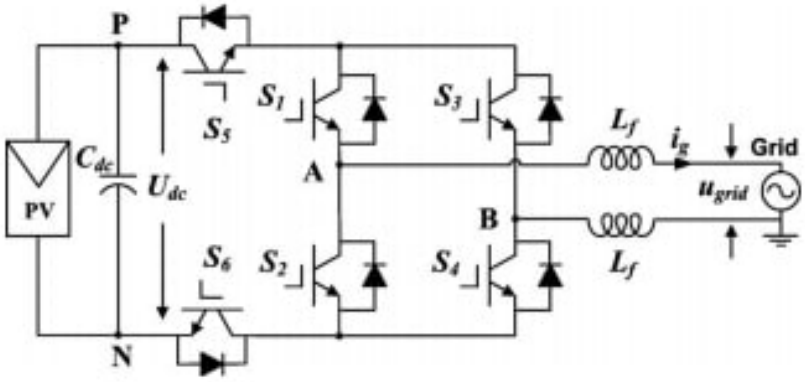
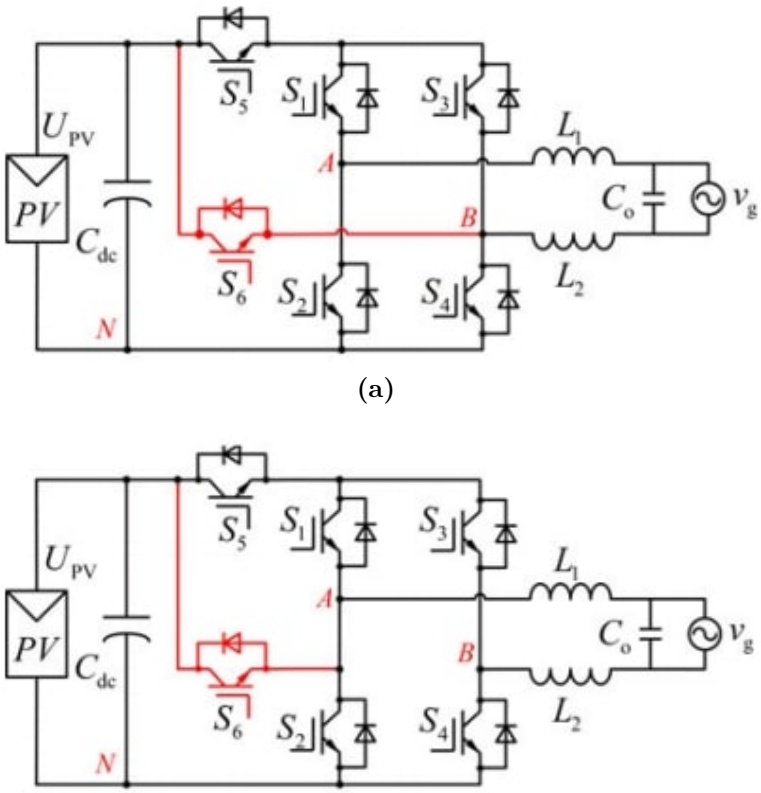


Figure 2.6: H6-Inverter topology [29].



(a)

(b)

Figure 2.7: A family of proposed H6-type inverter topologies [37].

topology. Given that only two switches conduct during the entire negative line frequency half cycle, the improved H6 inverter has lower conduction losses in comparison to the H5 architecture. In addition, the common mode of both proposed topologies is half of the DC link voltage, resulting in a low leakage current, and conduction losses [37].

2.2.3 HERIC-Inverters

Another category of six-switch type transformerless inverter is adding a set of bidirectional switches between the switch node terminal A and B of the full-bridge module acting as a decoupling network. Topologies that use this method consisted mainly of the Highly Efficient Reliable Inverter Concept (HERIC) set of inverters. Fig. 2.8 shows the HERIC inverter developed and patented by SUNWAYS [38]. During the positive half-line cycle, switches S_1 and S_4 are ON, while switches S_2 and S_3 are OFF. In contrast, during the negative half-line cycle, switches S_2 and S_3 are ON, while switches S_1 and S_4 are OFF. During the freewheeling stage, the inductor current flows through S_6, D_6 or S_5, D_5. Other HERIC topologies made use of two switches in series as shown in Fig. 2.9a or a rectifier bridge in parallel with a switch in Fig. 2.9b. To break away from the patent barrier posed by the original design, many innovative HERIC based inverters have been proposed in the literature [37, 39, 40, 41, 42]. Overall, they offer the same advantage of minimal common-mode noise similar to the DC-based H5 and H6 inverters.

In summary, the H5, H6, and HERIC based inverters generate minimal ground current but resulted in high conduction losses. Also, the increased number of active switches makes the implementation of these topologies costly and complex.

2.3 Non Full-Bridge Based Inverters

2.3.1 Dual Parallel Buck Inverter

The dual parallel buck inverter is depicted in Fig. 2.10. Buck A is used during the positive half cycle, switch S_4 is ON while S_1 is operated at high frequency to generate the positive half cycle voltage. During the remaining half cycle, buck A is turned off, while buck B is used

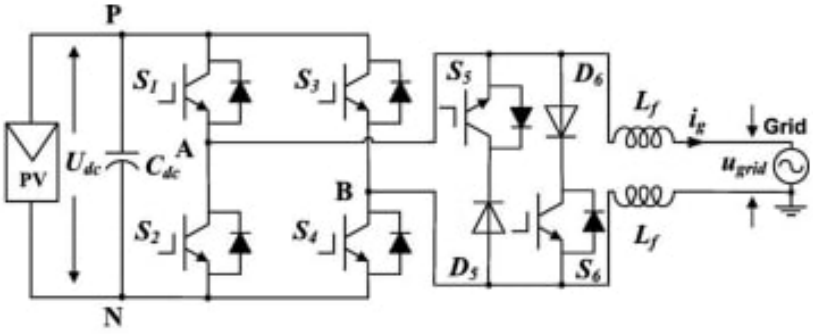


Figure 2.8: AC-based HERIC inverter [38].

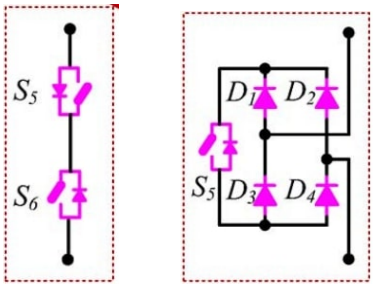


Figure 2.9: AC-based HERIC inverter switch configuration. (a) Switches in series. (b) Rectifier bridge in parallel with a switch [29].

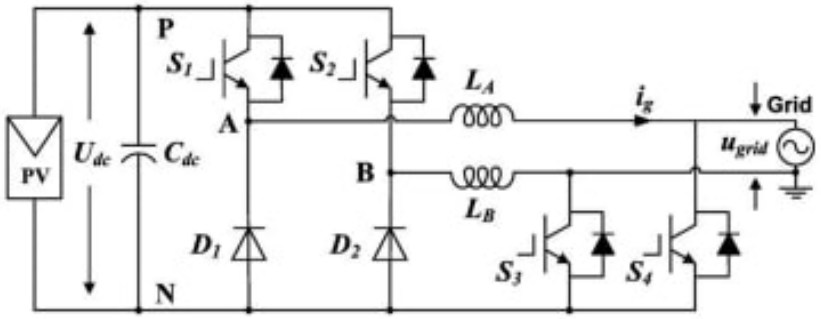


Figure 2.10: Dual parallel buck converter [36].

to generate the negative voltage by switching S_4 ON and modulating S_2 at high frequency. In contrast with the previously discussed H5 and H6 topologies, this inverter eliminates the issue of high conduction losses because only two switches are conducting during the power transfer phase of the inverter [36]. But, both inductors L_A and L_B are required and are operated alternately which negatively affected the cost and power density of the inverter [29].

2.3.2 Karschny Inverters

The basic Karschny inverter also known as a flying-inductor topology is illustrated in Fig. 2.11 and was first introduced in [43] to eliminate the leakage current. The negative terminal of the PV array is directly connected to the neutral point of the AC output voltage, eliminating any CM voltage oscillation. This inverter architecture can operate as a buck and boost stage with switches S_3 and S_4 setting the output polarity [44]. During the positive half cycle, switch S_4 is turned ON while switches S_1 and S_5 are modulated complementary at high frequency to achieve buck operation. The remaining switches S_2 and S_3 are turned off during this period. In contrast, during the negative half cycle, switches S_2, S_3 are now turned ON while S_4 is OFF. Next, S_1 and S_5 are switched alternatively at high frequency to achieve a boost mode. Although the Karschny inverter has a minimal leakage current, it has a large conduction loss since a large number of power devices (at least three) are in the conduction path at any given time [29].

2.3.3 Neutral Point Clamp Inverters

Neutral point clamped (NPC) inverters are derived from a half-bridge inverter architecture with the main advantage being an excellent leakage current performance [42]. In NPC inverters, the AC output voltage neutral line is connected to the middle point of the dc-link. This fixes the voltage of the PV array to the grounded neutral as illustrated in the example topology of a three-level NPC inverter in Fig. 2.12. The resulting constant CM voltage helps to eliminate the leakage current, making NPC converters attractive for transformerless PV

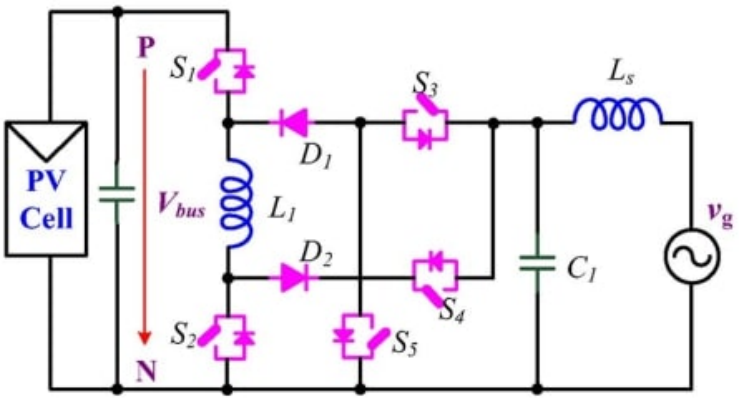


Figure 2.11: Karschny transformerless inverter [29].

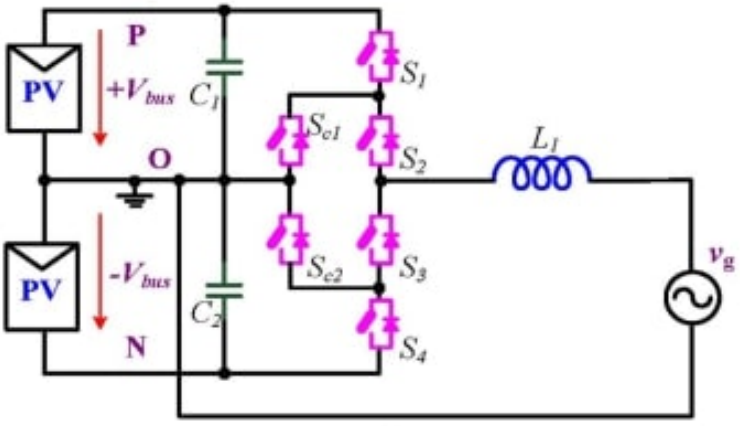


Figure 2.12: Three-level NPC inverter [29].

system applications. However, one of the main drawbacks of this type of inverter for single-phase inverter application is the high DC link voltage, which is twice the grid peak voltage. Depending on the system, this could reach voltages higher than the allowable maximum system voltage, requiring the need for a boost converter stage at the inverter input, which could decrease the overall efficiency of the system [12].

2.3.4 Multi-level Inverters

There are four common types of multilevel inverters: diode clamped, cascaded H-bridge, flying capacitor, and switched capacitor [45]. They generate a sinusoidal voltage from several levels of voltages, usually obtained from a capacitor voltage source. For instance, Fig. 2.13 illustrates the topology of a conventional five-level flying capacitor multi-level (FCML) inverter. For an n level converter, the FCML can be modulated with phase-shifted pulse width modulation (PSPWM) of $360/(n-1)$ degrees to generate a rectified sinusoidal output that is flipped by the full-bridge unfolder every half-line cycle to generate a true sine-wave output. In addition, the voltage on each switch is $V_{dc}/(n-1)$ and the effective switching frequency seen by the filtering inductor is $(n-1)$ times higher than the switching frequency of the devices. This allows for the use of lower voltage rated devices, a reduction of the output inductor filter size and a low current ripple on the inductor. With an increased demand in PV inverter power handling capacity in recent years, multi-level inverters with a neutral point clamped configuration are applied to more and more PV systems [46]. They combine both the advantages of multi-level inverters with the excellent leakage current performance of neutral point clamped topologies. Despite those advantages, research in [47] and [13] have shown that multilevel inverters significantly increase the component count and control complexity. Their high number of converter levels requires many storage capacitors, isolated gate drivers, and supplies, making it complex and expensive. Furthermore, the capacitor voltage imbalance is a major drawback of these types of inverters. Imbalanced capacitors increase the voltage across switches and could lead to device failure if the voltage exceeds their ratings, requiring additional controls and sensors to prevent.

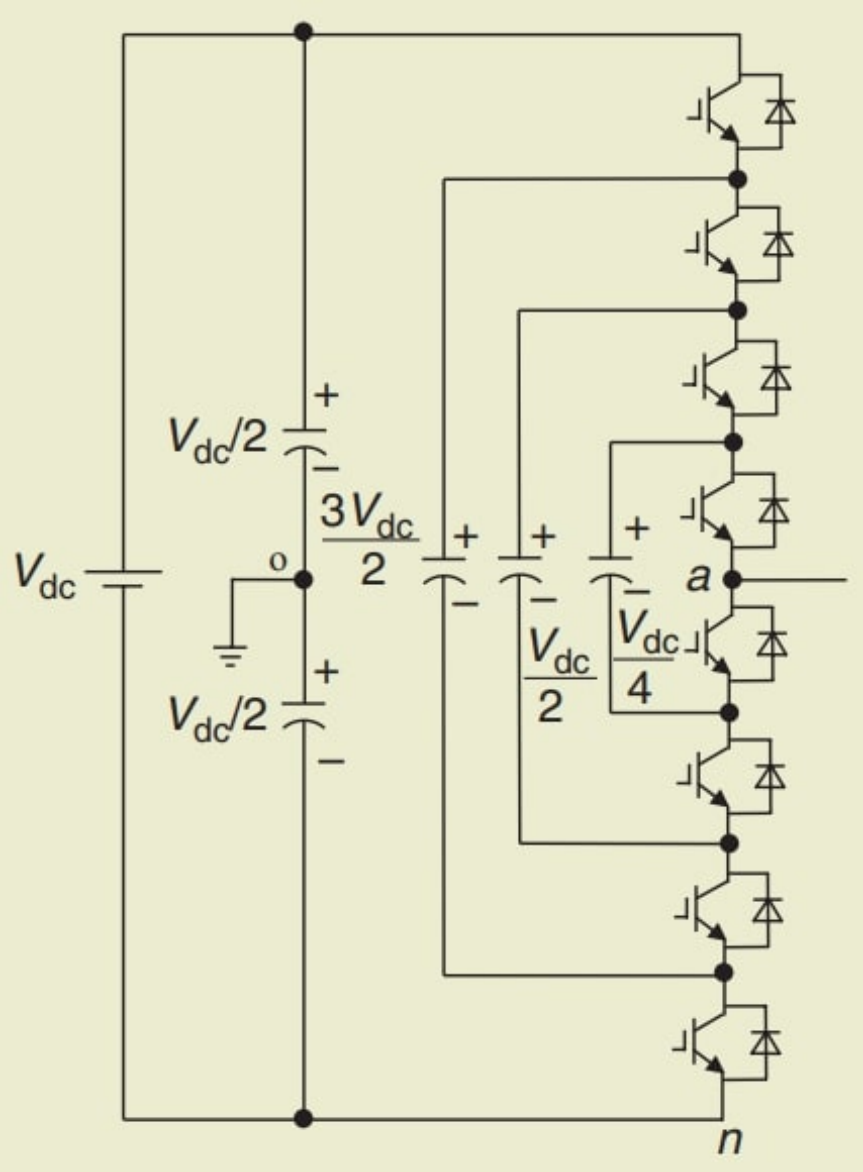


Figure 2.13: A conventional five-level flying capacitor multi-level (FCML) inverter [46].

2.4 Power Decoupling Methods

Fig. 2.14 shows the power flow in a single-phase power conversion system for a PV application. The DC side has a constant power $P_{dc} = P_o = V_{dc}I_{dc}$, while the output has a time varying power flow $P_{ac}(t) = V_{ac}(t)I_{ac}(t)$. Assuming a unity power factor, with $V_{ac}(t) = V_o \sin(\omega t)$ and $I_{ac}(t) = I_o \sin(\omega t)$, the resulting output power is given by

$$P_{ac}(t) = V_{ac}(t) \cdot I_{ac}(t) = \frac{V_o I_o}{2} - \frac{V_o I_o}{2} \cos(2\omega t) \tag{2.1}$$

The double line frequency time-varying power difference between the DC input and AC output power has to be compensated by the converter to satisfy the energy conversion and performance requirements of the system. The second-order ripple power on the DC link causes the DC voltage and current to pulsate at twice the line frequency resulting in a system degradation and loss in efficiency [48]. To address this issue, the conventional way has been passive decoupling, which uses a large electrolytic capacitor on the DC link while the other approach is using active power filtering (APF) techniques. These methods consist of using power electronics circuits and a control algorithm to buffer the power between the DC input and AC output.

2.4.1 Passive Power Filter

The passive decoupling technique has been the dominant solution and consists of using a large capacitor or an inductor or a combination of both as demonstrated in Fig. 2.15(a). Generally, due to their high energy density and low cost, capacitive energy storage is preferred over inductive options. However, the voltage and current ripple requirements in PV applications are such that it results in a huge bulky electrolytic capacitor on the DC link. These are assumed to be one of the life-limiting components in power converters for PV application [49]. To take advantage of the benefits of capacitive power decoupling while addressing their reliability issues, many active capacitive dc-link solutions have been proposed.

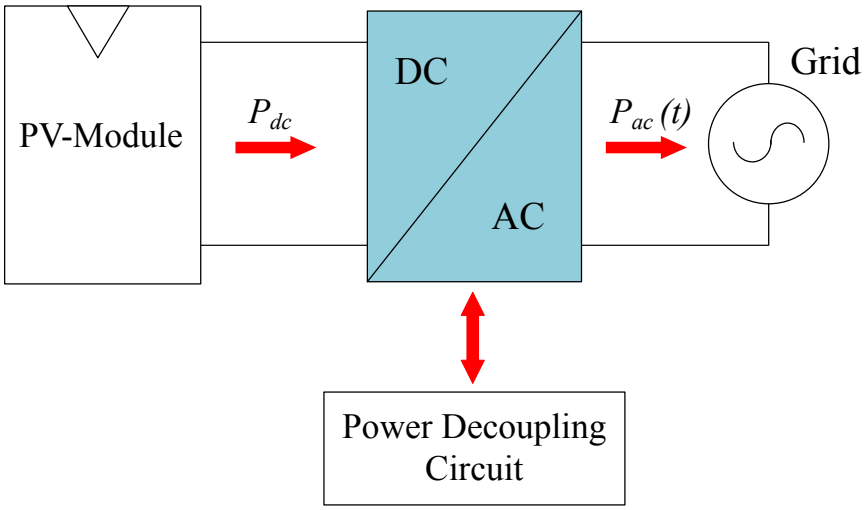


Figure 2.14: High level power filtering schematic.

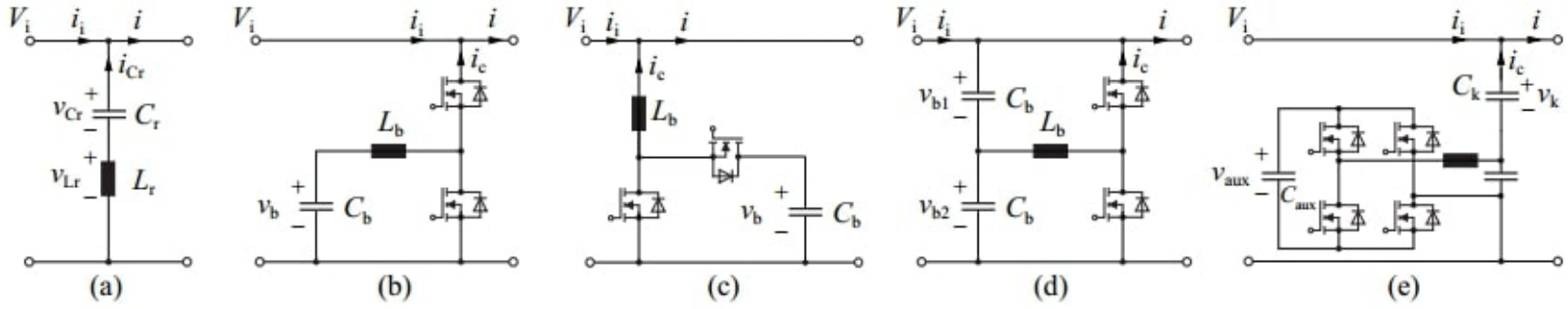


Figure 2.15: Overview of common PPB topologies connected in parallel to the dc bus of a single-phase inverter or rectifier. (a) notch filter (b) buck (c) boost (d) flying capacitor (e) stacked capacitor approach [50].

2.4.2 Active Power Filter

Active decoupling techniques consist of using control algorithms and power electronics circuit topologies to divert the ripple power from the DC link to a storage element that allows larger fluctuation of the voltage or current [51, 52]. For instance, by controlling the voltage ripple on the storage elements to be larger than that of the DC bus, the overall size of the power decoupling can be minimized by using smaller capacitors. These types of filtering can be implemented on the DC side or the AC side of the inverter. They can also operate independently or integrated as part of the inverter power stage in the case of switch multiplexing decoupling topologies [52].

First, regarding the DC side power filtering, the fundamental idea is to introduce a high or low-impedance element either in series or parallel to the inverter power stage. By controlling the impedance of this element, current can be shunt through it (low impedance) in the case of a parallel connection or blocked from flowing (high impedance) to the DC side in the case of a series connection. To achieve this purpose, many DC-DC topologies have been proposed in a series or parallel configuration with the DC bus. These topologies are operated independently and require a sophisticated control system to successfully compensate for the fluctuating power. Moreover, it is important to note that the reduction in capacitance value depending on the choice of topology, allows the use of film or ceramic capacitors which are more reliable than their electrolytic counterpart.

An example implementation of DC-based APF topologies such as buck, boost, flying capacitor, full-bridge stacked capacitor are all shown in Fig. 2.15. A review in [50] between the DC-based APF topologies depicted in Fig. 2.15 with the goal of achieving a high-power density showed that the buck type APF (Fig. 2.15(b)) had the lowest requirement on the buffer capacitor, resulting in the converter with the highest power density. The boost converter depicted in Fig. 2.15(c) has the same working principle as the buck type and could be modulated the same way. However, the decoupling capacitor must be regulated to a voltage level higher than the DC bus, making it undesirable for high-voltage applications. Next, the flying capacitor type APF in Fig. 2.15(d), has the advantage of having the buffer capacitors filter the high voltage DC bus while also handling the power buffering. But, it also

requires in total four times more capacitance when compared with the buck-type topology making it unappealing for high power density oriented design. Lastly, the full-bridge stack capacitor topology in Fig. 2.15(e) consists of a full bridge buffer converter connected in series with a main energy storage capacitor. One key advantage of this architecture is that the full-bridge converter only processes part of the output power as the series capacitor provides the bulk of the power buffering. Because of the low voltage stress in the full-bridge converter, a small-size inductor, low voltage, and high-speed devices can be used [53]. The full-bridge architecture can also be used in a series connection as depicted in Fig. 2.16.

It is often controlled as an AC voltage source in series with the DC voltage source. The voltage source is controlled in such a way to generate a 180° phase shifted voltage ripple with the same amplitude as the 120 Hz voltage ripple across the DC link capacitor. As a result, the ripple in the input voltage and current is near zero. One of the main drawbacks of this approach is that while the DC link voltage is smooth, a low-frequency voltage ripple still exists at the input of the inverter which could impede the operation of the inverter if the output voltage goes above the input voltage.

Second, AC-based APF filters are mostly dependent on decoupling topologies that use energy storage passives located at the AC side and provide decoupling through an additional phase leg or active control schemes. They are also referred to as switched-multiplexing decoupling topologies, where the basic decoupling cell partially or fully shares power semiconductor devices with the inverter stage [52].

Waveform control is one of the commonly used techniques in the literature and can be implemented with a buck, boost, or buck-boost differential inverter topology. Fig. 2.17 shows an example of a differential buck-type inverter using waveform control to filter. Its basic operation consists of individually controlling the output voltages of the DC-DC converters of the differential inverter such that the pulsating power is transferred towards the output decoupling capacitors while their differential voltage still maintains a pure sinusoidal output voltage [54]. One of the main advantages of using waveform control is that it does not require additional components; it does not change the basic operation of the inverter structure, which makes it appealing for a high-power density design. According to [54], in waveform control topologies, the differential inverter can contain a DC offset component due to time delays

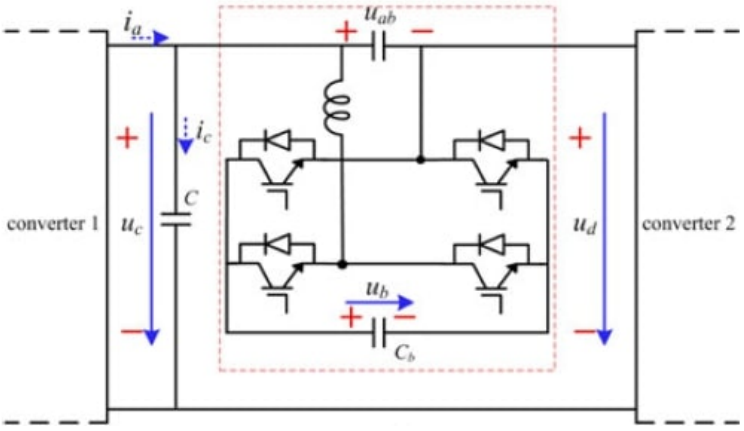


Figure 2.16: Series active ripple filter topology [52].

and practical imperfections in the control, which should be prevented in grid-tied inverter applications.

Next, from the basic structure shown in Fig. 2.17, many other topologies have been proposed in the literature where an additional phase leg is added to provide power decoupling [55]. Fig. 2.18a shows an example of a buck-type AC-based APF with an additional phase leg. This topology results in a large peak current, almost twice the load current, flowing in the U, V phase legs because the Z phase current flows through them [55]. To address the high conduction loss associated with this topology, the inverter in Fig. 2.18b has been proposed. It can successfully compensate the ripple power if the capacitor current or voltage is controlled to follow a pure sinusoidal waveform with the same frequency as the AC source [51]. The middle phase leg is shared by the original converter and the decoupling cell. As a result, the shared bridge arm has to undertake the task of inversion and power buffering, which presents some control complexity.

In summary, AC-based active power filters offer the main advantage of integrating power buffering into the inverter operation with an additional phase leg or without any extra components. However, it has the disadvantage of coupling the inverter power stage with the APF stage. On the other hand, a DC-based active power filter is operated independently of the inverter stage and offers the flexibility of using different circuit topologies and configurations. Overall, both approaches enable the use of more reliable capacitor alternatives such as ceramic and film. However, the use of better and more reliable capacitors does not subsequently lead to an approved system from a reliability standpoint. The additional components introduced in the circuit may affect the overall system-level reliability, efficiency, and power density. As a result, consideration has to be given to the choice of inverter topology and modulation scheme coupled with design for reliability techniques.

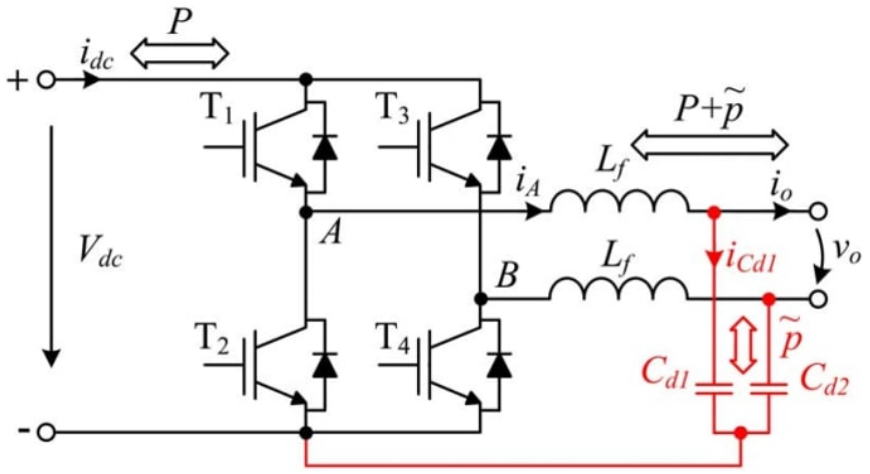
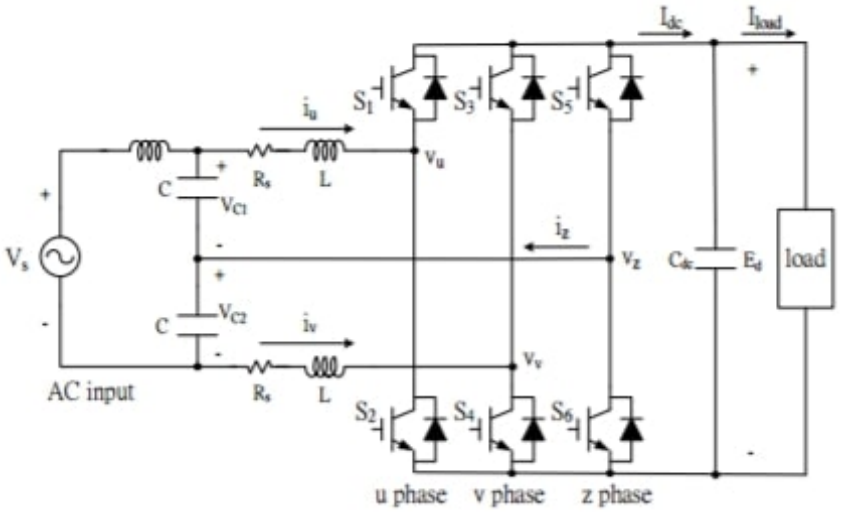
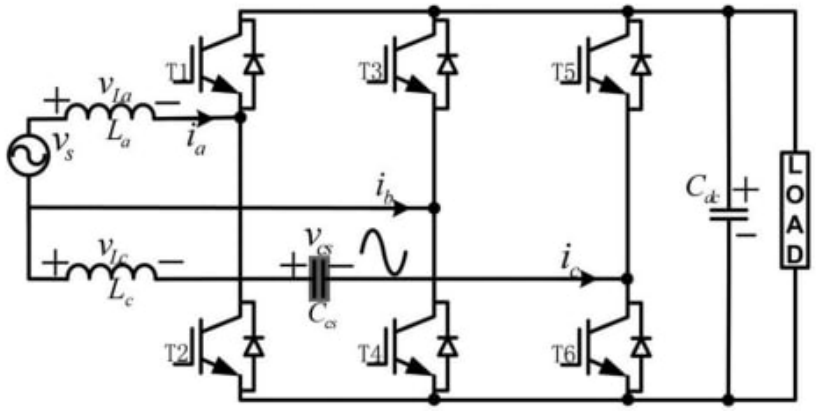


Figure 2.17: Buck-type differential inverter with decoupling circuit [56].



(a)



(b)

Figure 2.18: The power decoupling circuit diagram with (a) ac side capacitor [55] (b) ac side series inductor and capacitor [51].

Chapter 3

Survey of Single-Phase PV Inverters and Design for Reliability Techniques

The survey of single-phase transformerless inverter topologies in this chapter focuses on the latest academic and industrial techniques used to improve their efficiency, power density and reliability. Designing for high efficiency, power density and reliability while minimizing cost are desired design targets in any power converter. However, achieving these objectives while meeting design constraints such as operation temperature, EMI, CM voltage, and leakage current is a challenge for engineers. Oftentimes, this leads to Pareto front optimization to determine the optimal operating point based on the desired outcome. Depending on the application, some objectives weigh more than others. In PV applications, where efficiency and cost are very sensitive, the design with high efficiency and minimal initial cost has been the standard. This has led to innovations that produced inverters reaching 99% efficiency using a minimal number of components [16]. But, with the growing demand for solar power in the world, highly reliable inverters are essential in driving down the lifetime cost of the system and further accelerating adoption. The reliability of PV inverters has been a limiting factor in PV systems, leading to significant downtimes [11, 5, 57]. Regardless of the topology, it has been established that electrolytic capacitors are the most unreliable component in inverter [58, 59, 60, 61]. Thus, to increase reliability, there has been a push toward inverter design methods that eliminate the use of electrolytic capacitors for ripple power filtering. Such topologies use active power filtering in order to reduce the size of the capacitance,

allowing the use of ceramic or film capacitors. Such design also offers a power density and efficiency benefit that has been demonstrated in the Google littlebox challenge (LBC), with inverters reaching a power density of 243 W/in^3. Thus, the inverter topologies surveyed in this chapter have been classified into design methods that lead to high efficiency, power density and reliability.

3.1 High Efficiency Inverters

The main design objectives for transformerless PV inverters are towards high efficiency and minimal ground leakage current [62]. Traditionally, commercial inverters have had an efficiency of around 96%. In recent years, the introduction of new innovative topologies coupled with advancements in control techniques and semiconductor power devices have all contributed to inverter architectures that could achieve well over 99% efficiency. The following review looks at the latest inverter architecture with high efficiency. These topologies include the dual buck, a modified HERIC, a ZVS assisted architecture and a flying capacitor inverter.

3.1.1 Dual Parallel Buck Inverter Concept

The topology depicted in Fig 3.1 is derived from the classic dual parallel buck inverter. One of the main differences in this topology is that the positive terminal of the PV array is connected to the phase output during the positive half cycle and the neutral point during the negative half cycle. Looking at its modes of operation, during the positive half cycle, T_2 is switched at high frequency, while T_3 is turned ON. In contrast, during the negative half cycle, T_1 is operated at high frequency, while T_4 is turned ON. When switch T_1 or T_2 is deactivated, diode D_1 or D_2 respectively provides the current freewheeling path, while the energy from the PV array is stored in the dc-link capacitors. In addition, the leakage current is greatly minimized in this topology. The negative terminal of the PV array is directly connected to the neutral point and the phase output respectively during the positive and negative half-cycles resulting in a constant CM voltage. The experimental result showed that the measured peak efficiency of the circuit reached 99%, while the European

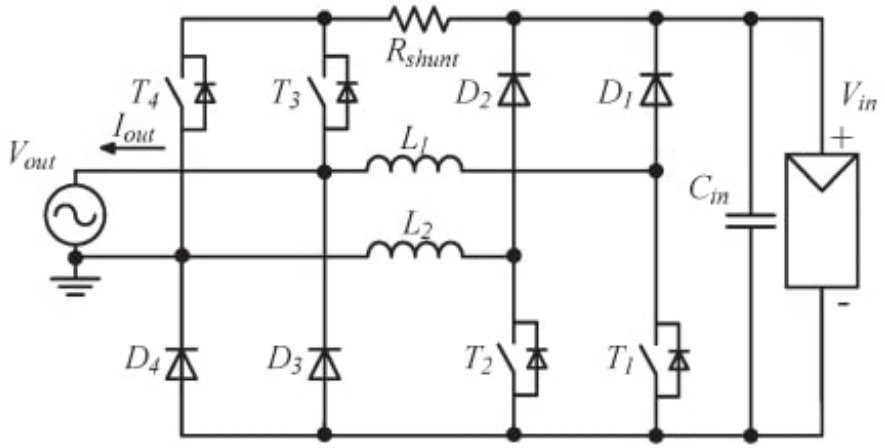


Figure 3.1: Proposed high efficiency single-phase transformerless inverter topology [44].

efficiency value was approximately 98.8% for an input voltage of 375 V and rated peak power of 4.5 kW [44]. CoolMOS power devices were used for all the switches ($T_1 - T_4$) implementation and silicon carbide Schottky diodes for all the diodes ($D_1 - D_4$). This helped to further minimize the converter switching losses due to the lack of reverse recovery effects in the silicon carbide Schottky diodes. A large (1.7 mF) DC-link electrolytic capacitor in parallel with a small (20 µF) metalized polypropylene film capacitor was used for the power buffering. Although this architecture was able to achieve remarkable efficiency, it was limited to only unity power factor operation and cannot process reactive power, as the current freewheeling is separated from the dc-link capacitance. In addition, both inductors L_1 and L_2 are required and are operated alternately, which negatively affects the cost and power density of the inverter. In regards to the overall reliability of this converter, the DC link electrolytic capacitor still represents the biggest liability in this design.

3.1.2 Virginia Tech Modified HERIC Inverter

Fig 3.2 shows another proposed topology in the literature that has achieved a high efficiency. This architecture is a combination of the dual parallel buck and HERIC inverter with an AC side pair of switches. It is composed of six switches ($S_1 - S_6$) and six diodes ($D_1 - D_6$) with two split ac-coupled inductors L_1 and L_2 that operate separately during the positive and negative half-cycles. The converter has four modes of operation within one grid cycle. First, during the positive half cycle, S_1 and S_3 are switched at high frequency while S_5 is turned ON. S_5 and D_5 are operated next to provide the freewheeling stage during the positive period. Third, in the negative half cycle, S_2 and S_4 are switched at high frequency, and S_6 is turned ON. Finally, S_6 and D_6 provide the freewheeling stage during the negative half cycle. The rest of the diodes ($D_1 - D_4$) are used for voltage clamping for the active switches. During the freewheeling phase, the grid is decoupled from the PV array helping to minimize the CM leakage current. The converter is also free from reverse recovery issues, given its split structure architecture, allowing the use of super junction MOSFETs. This enabled the converter to operate and reach super high efficiency over a wide output power range with a peak at light load. A 5 kW experimental prototype using super junction MOSFETs as the

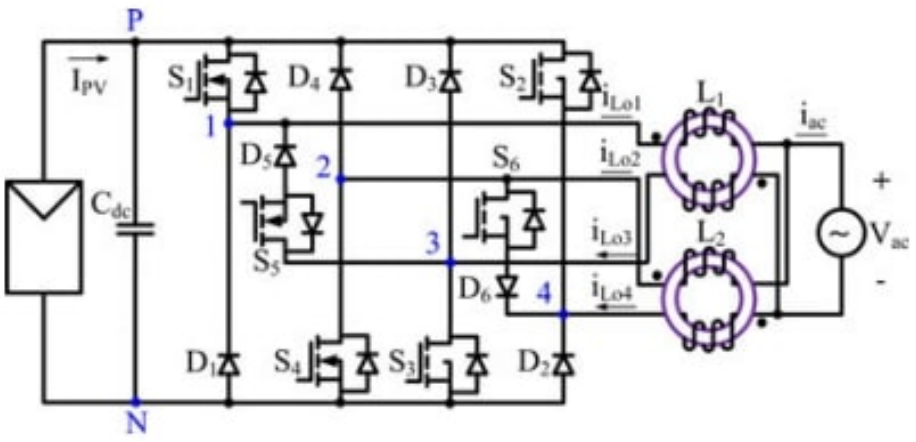


Figure 3.2: High efficiency and reliability PV transformless inverter topology [36].

main switches yielded a peak efficiency of 99.3% and CEC efficiency of 99.0% while operating at 20 kHz switching frequency [36].

In addition to the high efficiency, one of the main advantages of this structure is that the shoot-through issue that is encountered in traditional full-bridge inverters is eliminated through the use of split ac-coupled inductors. It greatly improves the converter robustness. For the power decoupling, an electrolytic capacitor solution is employed. Overall this converter has achieved super-high efficiency, a low CM leakage current, and improved converter-level robustness. However, the increased number of component counts adds to the cost and without any redundancy, that increases the probability of failure of the inverter.

3.1.3 Coupled-Magnetic Based Soft-Switching Inverter

Fig 3.3 shows the topology of a soft-switching inverter using auxiliary resonant circuits. These auxiliary circuits are composed of switches (Q_{X1}−Q_4), diodes (D_{X1}−D_{X8}) and coupled inductors ($L_{r1} - L_{r4}$) which all have been designed to assist the main switches ($Q_1 - Q_4$) to achieve zero-voltage switching. A detailed analysis of the different modes of operation of this inverter is given in [62]. The converter has eight switching intervals including the resonance period during the dead time when the auxiliary switches are operated. In addition, the proposed converter has reactive power capabilities

A 5 kW experimental prototype converter achieved a 99.26% peak efficiency and 99.13% CEC efficiency without a cooling fan. The main switches were implemented using MOSFETs and IGBTs for the auxiliary devices [62]. The MOSFET conduction loss and the output filter inductor loss, including both the core and conduction loss, were the dominant forms of loss in the power stage. Despite its high efficiency, the auxiliary circuit in this architecture added a large number of extra components and not only increased the cost of the circuit but hindered the reliability of the system.

3.1.4 Siwakoti Flying Capacitor Based Inverters

The flying inverter topology developed in [16] and [63] has demonstrated high efficiency with reactive power capabilities while maintaining an almost zero common-mode leakage current

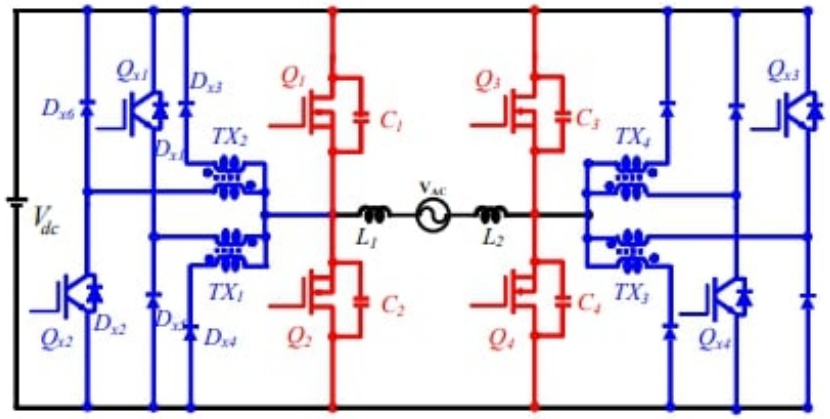


Figure 3.3: Coupled-Magnetic based proposed soft-switching inverter [62].

and low THD. The initially proposed architecture is illustrated in Fig 3.4. The inverter is modulated using unipolar SPWM modulation. During the positive cycle, switch S_1 is turned ON while S_3 is operated at high frequency. The flying capacitor C_{FC} is charged during this cycle by having S_1 and D ON during the entire period. Next, for the negative cycle, S_3 is OFF, and S_4 is switched ON while S_2 is switched at high frequency and C_{FC} supplies the voltage to the load. The diode is turned ON automatically when S_2 turns OFF. For the zero voltage state, switches S_1 and S_4 are turned ON [63].

This inverter has been realized using SiC MOSFETs devices and achieved a 99.2% peak efficiency at 1 kW full load. An improved second version (Type II) of this topology is depicted in Fig 3.5 where switch S_1 is moved to connect directly to C_{FC}. Similar to the initial architecture, its operational fundamentals are the same with the exception that in this topology, only one switch S_3 carries the load current during the positive half cycle instead of S_1, S_3. As a result, S_3 now has voltage stress twice the DC link voltage. However, this helped to reduce the conduction loss in the circuit. The experimental prototype of this inverter realized a maximum efficiency of 99.25% at full load.

Both inverter architectures achieve high efficiency with near-zero leakage current and are implemented using a minimal number of semiconductor devices: four switches and a diode. Its low component count makes it an ideal solution for low-cost PV inverter solutions. However, from a reliability perspective, the use of electrolytic decoupling for power buffering still constitutes a reliability issue for the lifetime of the inverter. In addition, as stated previously, any component failure will result in the converter seizing operation and having to be fixed or replaced. Table 3.1 summarises and gives a comparison of the major high-efficiency single-phase transformerless PV inverters.

Despite the ultra-high efficiency achievement of all these inverter topologies, reliability remains an issue. This is understandable given that the main objective for these inverter designs was high efficiency. High power density and reliability were not the main targets. However, with the latest push and the growing demand for more reliable inverter solutions, design for reliability techniques are integrated into the inverter design phase to evaluate the converter's lifetime performance.

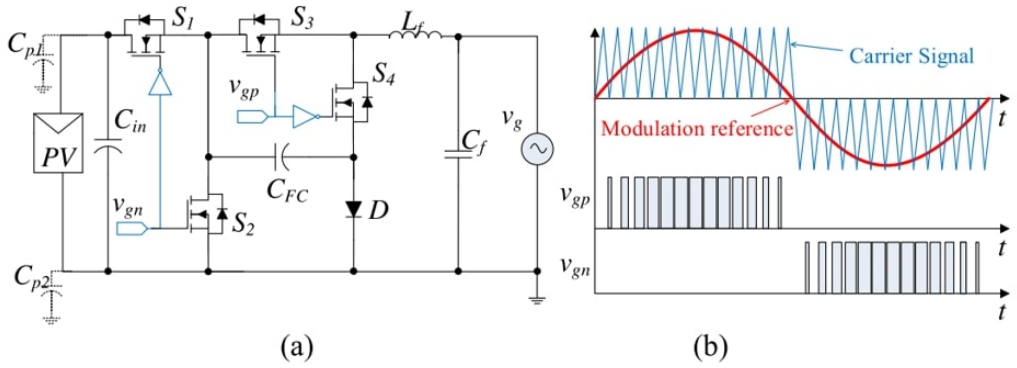


Figure 3.4: Type-I flying capacitor transformerless grid-connected single phase inverter topology with two switches in series during positive cycle [63].

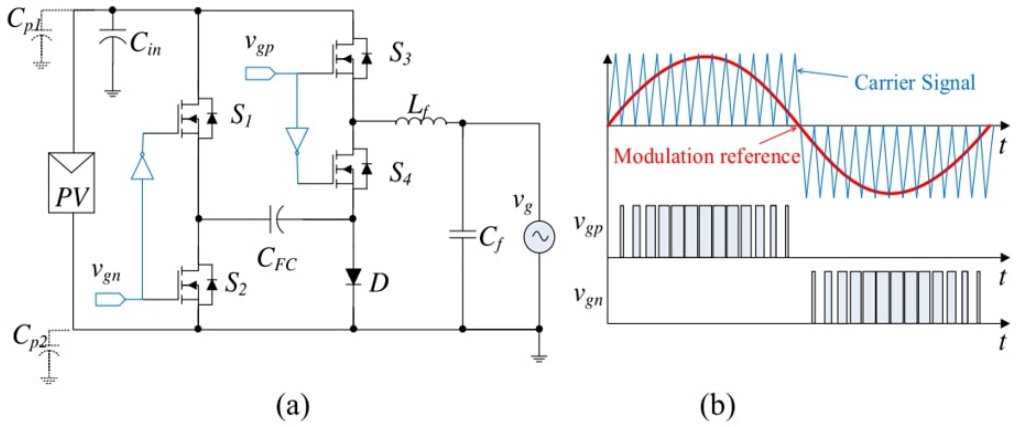


Figure 3.5: Type-II flying capacitor transformerless grid-connected single phase inverter topology with a single switch in series during the positive cycle [16].

Table 3.1: Comparative Summary of High-Efficiency Topologies

Topologies	Dual Parallel Buck (I)	VT HERIC (II)	CM-Soft switched (III)	Siwokati (IV)
Reference	[44]	[36]	[62]	[16]
Input Voltage	376 - 537 V	380 V	400 V	400 V
Output Voltage	230 Vrms	240 Vrms	240 Vrms	230 Vrms
Switching frequency	16 kHz	20 kHz		50 kHz
Line frequency	50 Hz	60 Hz	60 Hz	50 Hz
Output power	4.5 kW	5 kW	5 kW	1 kW
Devices	CoolMOS	MOSFET	MOSFET	SiC
Efficiency	Peak: 99% CEC: 98.8%	Peak: 99.3% CEC: 99.0%	Peak: 99.26% CEC: 99.13%	Peak: 99.25% CEC: NA
Power Buffering	Passive	Passive	Passive	Passive

3.2 High Power Density Inverters

High power density and high-efficiency converters are two important design targets in power electronics for many modern applications such as electric vehicles and renewable energy. In this section, converter design with high power density is the main design objective surveyed. Recent trends have put an emphasis on reducing the size of inverters for residential and commercial grid-tied applications. A smaller and lighter inverter can reduce the size of the overall system and the associated cost of installation and maintenance [15, 53, 64]. In 2014, Google and IEEE brought the world's attention to developing ultra-high power density inverters by hosting a little box challenge (LBC), which consisted of designing a 2 kW inverter that would reach a power density of at least 50 W/in^3 [15]. Through the LBC, there were innovations in the power stage, power decoupling, thermal management, and EMI filter design that came from various teams. Wide bandgap devices have also played an important role in enabling some of the breakthroughs that have been achieved in this challenge. The use of GaN and SiC allowed for high-frequency operation while minimizing switching losses. Out of the 18 finalists that were selected, the Belgium team CE+T Power was awarded first place. Their converter is an interleaved full-bridge TCM inverter with a Buck-type APF. It achieved a power density of 143 W/in^3 and is similar in design to the ETH inverter which achieved a power density of 134 W/in^3. Most of the teams used either a Full-bridge topology or a derivative of the full-bridge. But, an innovative 7-level flying capacitor architecture with a full bridge series-stacked APF presented by the University of Illinois at Urbana-Champaign (UIUC) achieved a remarkable power density of 216 W/in^3. A recent update by ETH presented in [14] has demonstrated a new inverter architecture that yielded a power density of 243 W/in^3 similar to UIUC. This review looks at the technical approach including power stage and power decoupling design from both UIUC and ETH teams.

3.2.1 ETH Inverter

The first version 1.0 of the ETH little box (LB) inverter topology is an interleaved full-bridge inverter with four-phase legs, each consisting of 2 phase legs in parallel. The schematic

is shown in Fig 3.6. The inverter is soft-switched using triangular current mode (TCM) modulation with a variable switching frequency in the range of 200 kHz-1 MHz. This TCM modulated interleaved inverter required complicated electronic circuitry for zero current detection which added to the complexity of the system but did result in higher power density and higher efficiency. The converter realized a power density of 134 W/in^3 and a nominal efficiency of 96.4% and was ranked among the top 10 out of 100+ contestants [65]. The hardware prototype is depicted in Fig 3.7.

In their next revision, part B LB 2.0, an iteration of the previously described inverter, the ETH team came up with a subsequent inverter design that reached a power density of 243 W/in^3 and a nominal efficiency of 97.4% [14]. Fig 3.8 shows the architecture for the proposed inverter system. It is a DC to rectified AC buck stage followed with H-bridge unfolder. The high-frequency DC-DC Buck stage circuit is used to generate the current source and an unfolder circuit switching at the line frequency, 60 Hz, is connected in series with the DC-DC stage. In contrast to LB 1.0, the Buck power stage is operated at a 140 kHz constant frequency PWM and hard-switching around the peak of the AC output current. The hardware prototype is shown in Fig 3.9. Paralleled 600 V/70 mΩ CoolGaN power semiconductor technology from Infineon are employed for the implementation of the inverter Buck stage while 650 V/25 mΩ enhancement-mode GaN transistors from GaNSystems (GS66516T) are used for the full-bridge unfolder stage.

Both ETH inverter LB 1.0 and 2.0, used a synchronous buck converter for their second-harmonic power buffering. A realized prototype in [50] tested in combination with a 2 kW inverter stage achieved an overall volume of 4.7 in^3 and a peak efficiency of 98.7% efficiency at rated power. The use of APF lowered the requirement on the buffer capacitor allowing for the use of ceramic capacitors, which can be operated with much larger current ripples than electrolytic capacitors. However, a large number of ceramic capacitors had to be soldered together to meet the energy storage and capacitance requirement in the range of 100 to 200 µF. For instance, in the LB 1.0 hardware prototype depicted in Fig 3.7, 120 x 2 µF CeraLink capacitors from EPCOS/TDK have been used and 200 x 2 µF in the LB 2.0 hardware implementation shown in Fig 3.9.

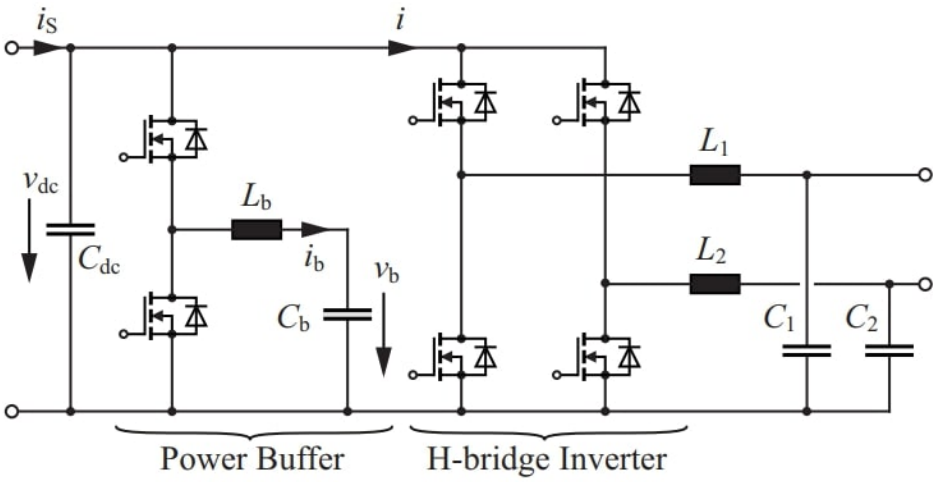


Figure 3.6: H-bridge inverter with DC-link referenced output filter and buck-type parallel current injector (PCI) active power buffer (Little Box 1.0) [14].

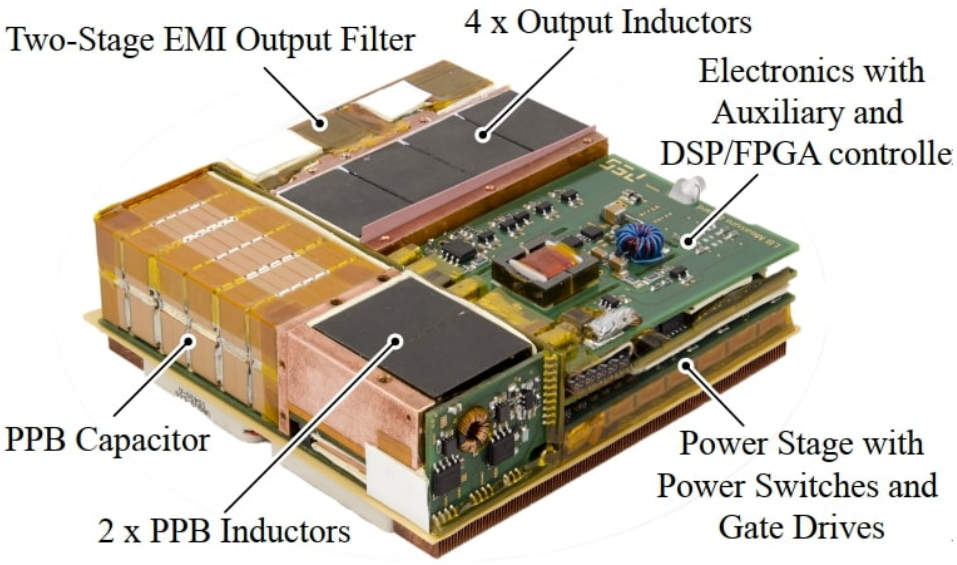


Figure 3.7: Photograph of the realized LB 2.0 hardware [14].

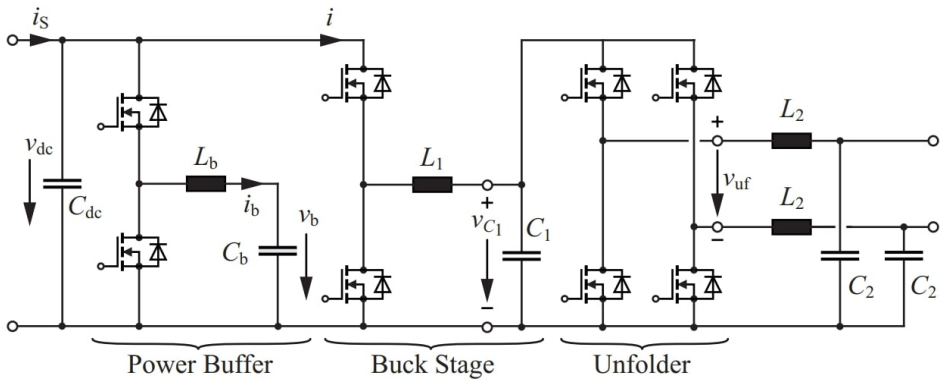


Figure 3.8: $DC/|AC|$ buck-stage and $|AC|/AC$ H-bridge unfolder inverter with PCI active power buffer (Little Box 2.0) [14].

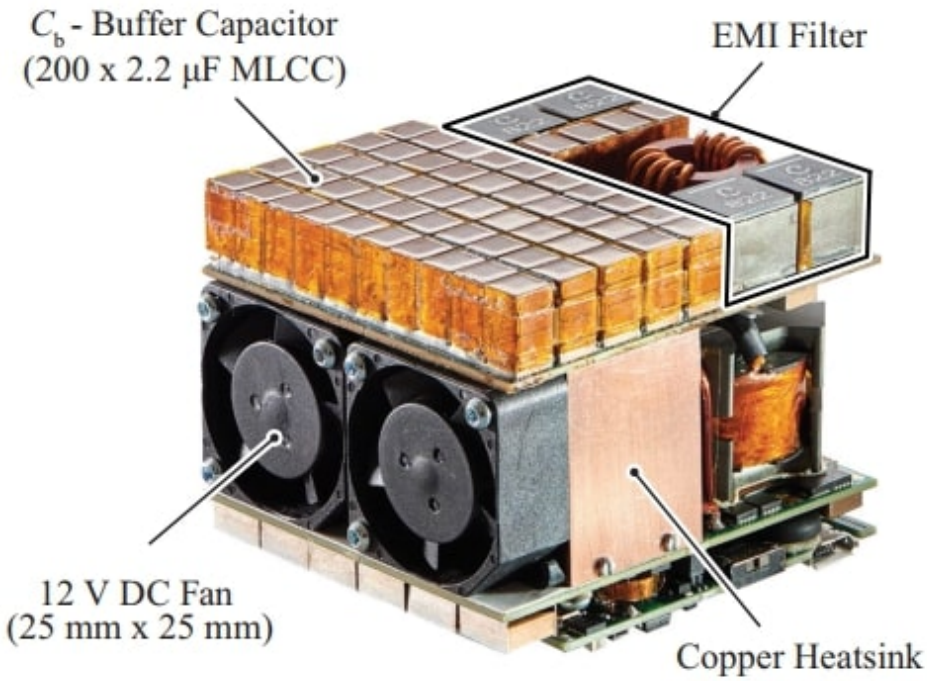


Figure 3.9: Photograph of the realized LB 1.0 hardware [14].

3.2.2 UIUC 7 level Flying Capacitor Inverter

Fig 3.10 shows a schematic drawing of the power stage of the UIUC 7−level FCMI converter followed by the full-bridge unfolder. The FCMI is modulated with a phase-shifted pulse width modulation (PSPWM) of $360/(N-1)$ degrees to generate a rectified sinusoidal output that is flipped by the full-bridge unfolder every half-line cycle to generate a true sinewave output. This inherently leads to an overall lower THD [53]. Their converter uses 150 V GaN devices that switch at 120 kHz, bringing the effective frequency seen by the filter inductor to 720 kHz. The inherent high effective switching frequency and low voltage ripple at the switched node help to reduce the output inductor filter size and to relax the attenuation requirement for the EMI filter design in comparison to the conventional full-bridge inverter. These beneficial properties result in a reduction in the EMI filter size and an improvement in the overall inverter power density. According to the UIUC team, their EMC filters constitute only 3% of the total inverter volume and less than 10% of the area. Their design achieves a power density of 216 W/in^3 and a peak efficiency of 97.6 % [53]. The experimental hardware is depicted in Fig 3.11.

For their power buffering stage, the UIUC team used a series stacked full-bridge architecture shown in Fig 3.12. In this architecture, a full bridge is connected in series with a main energy storage capacitor C_1, which is operated with a large voltage ripple. One key advantage of this architecture is that the full-bridge converter only processes part of the output power as the series capacitor C_1 provides the bulk of the power buffering. Because of the low voltage stress in the full-bridge converter, a small size inductor, low voltage, and high-speed devices are used [53]. It has been shown experimentally in [66] and [67] that their APF architecture alone achieved an impressive 99.6% peak efficiency and a power density of 611 W/in^3. Similar to the Buck type APF used in the ETH design, a large number of ceramic capacitors are soldered together to get the value of C_1 and C_2. As illustrated in the hardware implementation of their active energy buffer shown in Fig 3.13, the bulk of the volume has been taken by the ceramic capacitors. According to [53], 239 x 2.2 µFceramic capacitors from TDK were used for C_1 and 126 x 15 µF for C_2. Not only does this chain

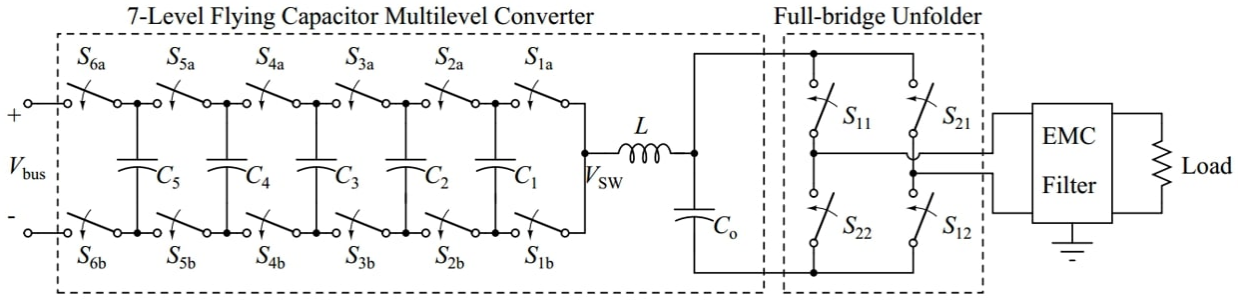


Figure 3.10: Schematic drawing of the 7-level flying-capacitor multilevel inverter. [53].

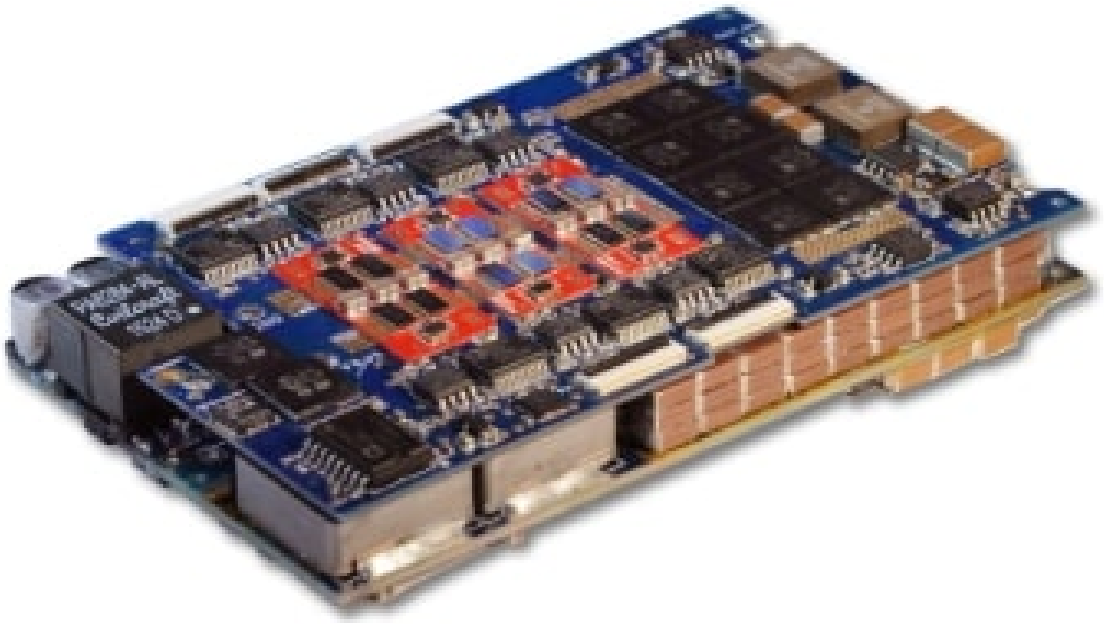


Figure 3.11: Photograph of the FCML inverter board and energy buffer fit together [53].

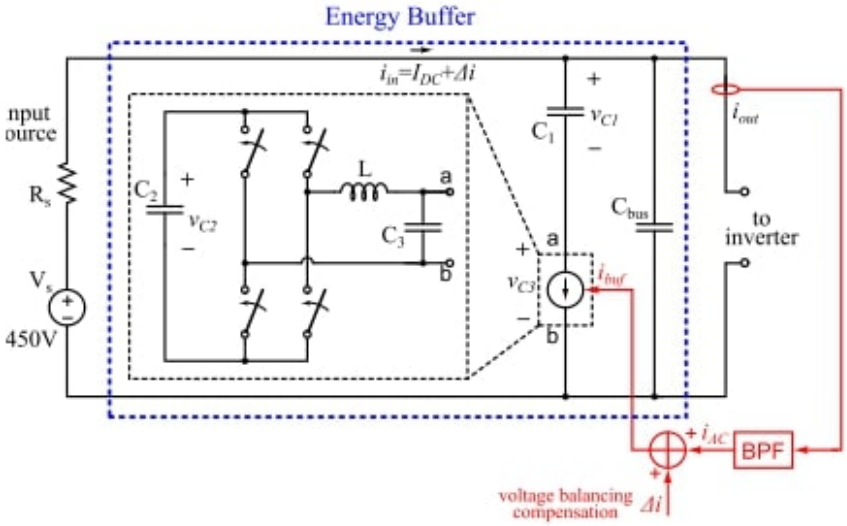


Figure 3.12: Active energy buffer with high level control flow diagram [53].

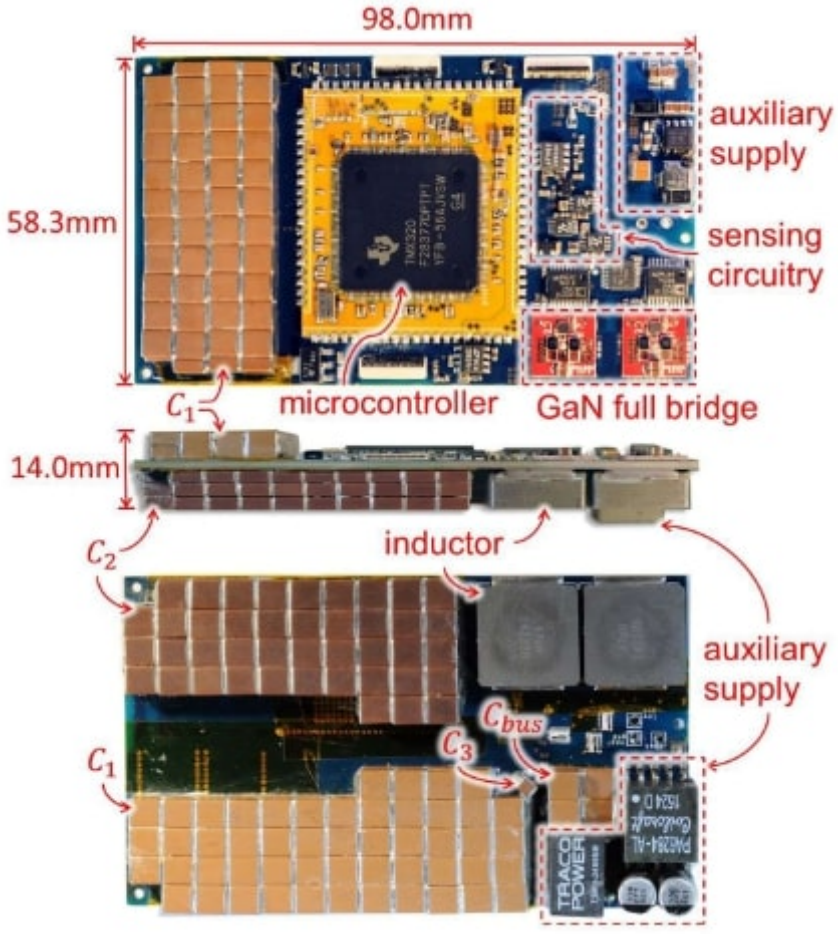


Figure 3.13: Annotated photographs of the active energy buffer board[53].

of ceramic capacitors increase the volume of the overall converter, but more importantly, it hinders the overall reliability of the system.

Table 3.2, summarizes the state-of-the-art inverter topologies surveyed in this chapter. Regardless of the architecture, the electrolytic capacitors have been replaced by massively paralleled ceramic capacitor banks in these research prototypes. This substitution, along with the power stage and controls to implement an active power filter, resulting in a significant reduction in volume by eliminating bulky and failure-prone electrolytic capacitors. This approach was meritorious in the LBC, where power density was the main design goal as opposed to high reliability and long lifetime. However, in designing for commercial systems, the massively paralleled capacitor banks lose all merit. Though ceramic capacitors exhibit, individually, over 10x MTTF compared to electrolytic capacitors, their massively paralleled ($>$ 200 in parallel) implementation reduces reliability; a failure of only one of these capacitors will short the entire bank. This failure is increasingly likely with thermal cycling due to the rigid mechanical structure of the capacitor banks. 120x2 µF CeraLink capacitors from EPCOS/TDK have been used and 200x2 µF

3.3 Reliability of PV Inverter

It has been established that electrolytic capacitors are the most unreliable component in inverter [58, 59, 60, 61]. Thus, to increase reliability, there has been a push toward inverter design methods that eliminate the use of electrolytic capacitors for ripple power filtering. Such topologies use active power filtering in order to reduce the size of the capacitance allowing the use of reliable film capacitors. Some of the latest inverter topologies that use film capacitors are demonstrated in [68, 69]. Despite these improvements, the lifetime evaluation of these proposed designs is not calculated to quantify their reliability performance. Eliminating electrolytic capacitors is not everything. According to an investigation of several single-phase PV inverter topologies in [70], most inverter failures occur during the switching stage and temperature is the most dominant cause of failure. Thus, the switching devices are as important as the capacitors. As a result, some of the

Table 3.2: Comparative Summary of High Power Density Topologies

Topologies	Interleaved FB Inverter (I)	Buck Unfolder (II)	7-Level FMCL (III)
Reference	[65]	[14]	[65]
Input Voltage	450 V	450 V	450 V
Output Voltage	240 V	240 V	240 V
Switching Frequency	200 kHz - 1 MHz	140 kHz	Switch: 120 kHz Effective: 720 kHz
Line Frequency	60 Hz	60 Hz	60 Hz
Output Power	2 kW	2 kW	2 kW
Power Density	134 W/in^3	243 W/in^3	216 W/in^3
Efficiency	Peak: 96.4% CEC: 95.07%	Peak: 97.4% CEC: 96.12%	Peak: 97.4% CEC: 97.0%
Switches	GaN-GIT (600 V/70 mΩ)	GaN-GIT (600 V/70 mΩ)	EPC (150 V/ mΩ)
Power Buffering	Buck APF	Buck APF	Series Stacked H-Bridge
APF Capacitors	120x2.2 µF	200x2.2 µF	C_1: 239x2.2 µF C_2: 126x15 µF

proposed solutions in [11, 71, 23] have focused on reliability-oriented design techniques which is discussed in detail in Section 3.5 instead of simply eliminating the electrolytic capacitor.

3.3.1 APF Based inverter using Film Capacitors

The APF can be implemented on the AC side with the use of an additional half-bridge phase leg as illustrated in the proposed inverter topology shown in Fig 3.14 [72]. This novel APF-based 2 kW inverter uses three half bridges where the extra phase is used for power buffering, allowing for the full utilization of the filtering capacitor. Through this decoupling approach, an 80µF/450 V film capacitor from TDK (B32778G4756K) is used to meet the energy requirement for the 2 kW inverter. The converter hardware implementation is shown in Fig 3.15 using GaN System (GS66508P 650V/30A) power devices; it achieves a 98% efficiency and a power density of 55.8 W/in^3.

Fig 3.16 illustrates the example of a recently proposed T-type common ground transformer-less single phase inverter with integrated power decoupling [69]. This topology is a combination of a bi-directional boost stage, an asymmetric half-bridge inverter stage followed by a bidirectional T-branch. It uses the dynamic dc-link active power decoupling technique detailed in [69], which allows a large voltage swing on the DC-link. Thus, reducing the decoupling capacitor C_{link} requirement and allowing an all-film capacitor implementation.

A 1 kW experimental prototype using SiC MOSFETs from CREE (CREE C2M0040120D) for all the switches is shown in Fig 3.17. The system capacitance requirement for 1 kW power buffering is reduced to 55 µF at 500 V peak DC-link voltage. Furthermore, the converter operates at 200 V DC input and 120 V/60 Hz AC output with a peak efficiency of 98.22 % and a CEC efficiency of 98.03% at a 50 kHz switching frequency. The overall converter volume including the heat sink is 83.26in^3 (10.93 inch x 5.52 inch x 1.38 inch) yielding a power density of 12 W/in^3.

Although the use of an all-film capacitor in the proposed topology configuration can increase the lifetime of the inverter in comparison to traditional inverters employing an electrolytic capacitor, the extra devices and the series configuration of this topology still constitute a reliability risk. A failure of any of the power devices or capacitors will cause the entire system to fail.

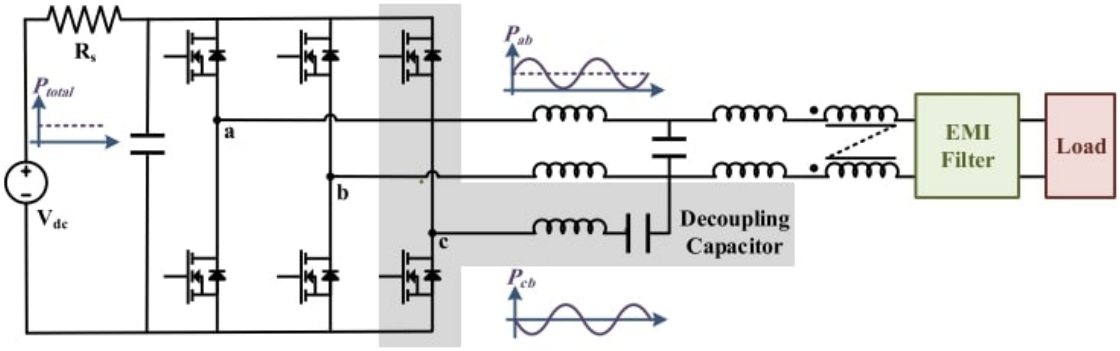


Figure 3.14: Full-bridge inverter with an integrated half-bridge AC side power decoupling [72].

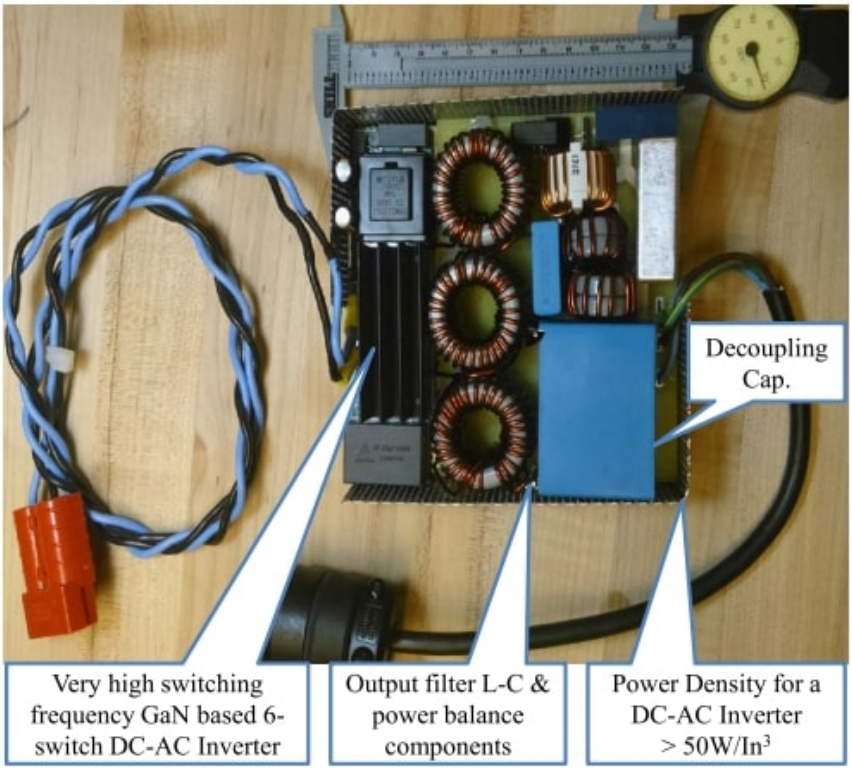


Figure 3.15: 2 kW experimental prototype of the proposed inverter with an AC side APF implementation using a film capacitor [72].

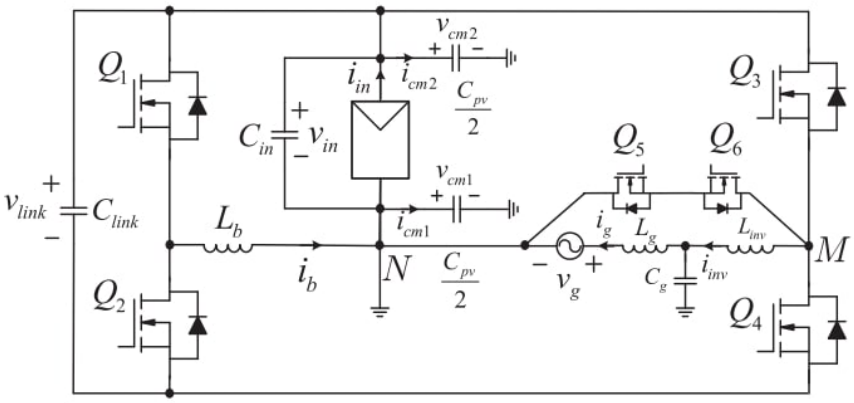


Figure 3.16: T-type common ground voltage swing inverter [69].

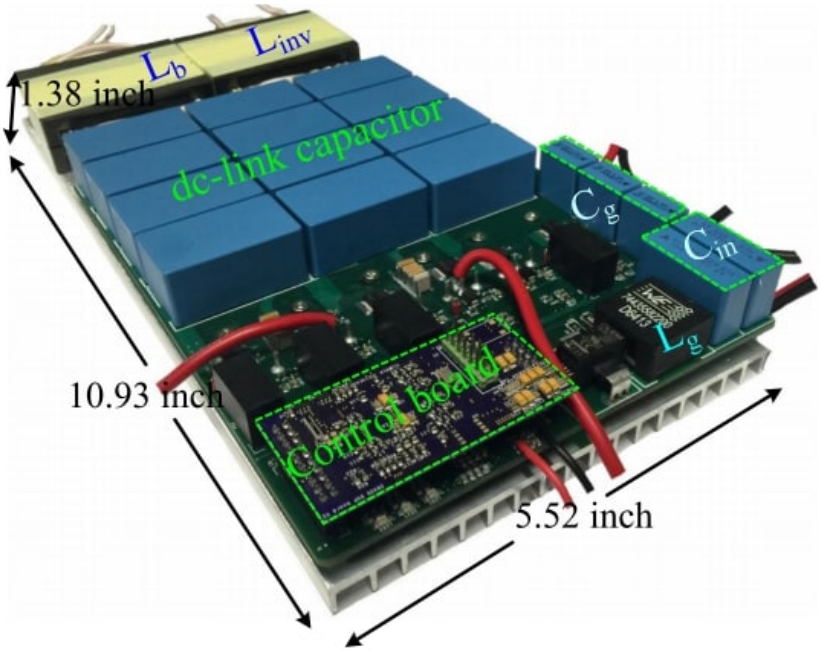


Figure 3.17: 1 kW experimental prototype of T-type common ground voltage swing inverter [69].

3.3.2 Multi-Port Dual Inverter Technique

A multiport inverter concept that eliminates the requirement of a power buffering capacitor without the use of an active power decoupling technique has been proposed in [73]. This is a dual output inverter module, where the outputs of the inverter are controlled in phase quadrature with ideally balanced loads. In other words, the first module (H-bridge 1) is controlled to support the stand-alone residential load while the other module (H-bridge 2) supplies power to the grid. This ensures that the double-line frequency power is eliminated, ideally not requiring any decoupling capacitors. However, due to nonidealities or the presence of any unbalance in the system, a very small film capacitor is used on the DC link. Furthermore, the proposed inverter concept is modular and can be paralleled and stacked together to meet higher power requirements. Fig 3.18 depicts the circuit schematic of the multiport dual-inverter where each module has been realized using a traditional full-bridge topology. The H-bridge modules are operated using any of the conventional PWM modulations such as bipolar or unipolar.

The concept has been validated in simulation and an experimental testbed using a controller hardware-in-the-loop (CHIL) for a 2 kW system (1 kW for each of the modules). The hardware for their proposed inverter architecture has been modeled in the OPAL-RT OP5600 based on a real-time simulation platform [73]. Thus, it is challenging to evaluate the true performance of this inverter. Certainly, the proposed multi-port dual inverter architecture helped to eliminate the requirement for large decoupling capacitors; however, its configuration and the way it operates means that only half of the power generated by the PV is supplied to the grid while the other half is supplied to some load. This solution is not practical and can only be applied in specific applications where the power injected to the load is equivalent to that of the grid.

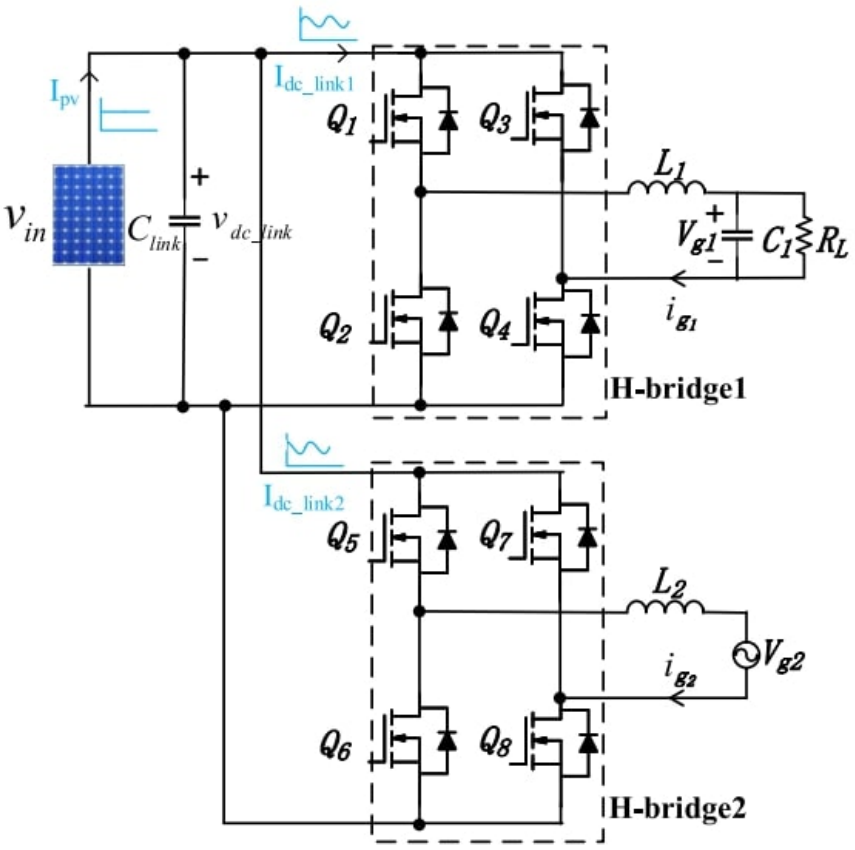


Figure 3.18: Circuit schematic of the proposed multiport dual-inverter [73].

3.4 Commercial grid Connected Transformerless PV Inverter Topologies

There are many players in the residential string PV inverter market worldwide including Fimer (Previously known as ABB), Fronius, SMA, SolarEdge, Sungrow. As of the writing of this dissertation, most of the residential string inverters on the market today, except for SolarEgde, use some type of transformerless inverter architecture with electrolytic DC link capacitors for power decoupling. Fig 3.19 shows a hardware example of a commercial string inverter from SMA. As can be noted, electrolytic capacitors are used for power decoupling. Although the technology associated with central inverters has been improving over the years, they are still considered one of the most unreliable components in a solar PV system. The inverter warranties currently offered on the market vary from 5 to 15 years, in contrast to micro-inverters which have much longer warranties ranging from 15 to 25 years [57]. This is due mainly to their small power processing and the use of film capacitors.

A survey of the state of the art commercial centralized inverters shows that one of the leading products on the market at the time of the writing of this dissertation is the high-definition wave inverter from SolarEdge technology. Their inverter uses a modified five-level flying capacitor circuit with an active power filter. Fig 3.20 shows the inverter schematic and Fig 3.21 shows the complete system hardware which has a CEC efficiency of 99.0% and is rated for 7.6 kW [74]. The multilevel inverter topology allows for the use of small voltage rating devices, reduction in device losses, high switching frequency operation, and reduction of the cooling system.

Conventional five-level flying capacitor circuits require a large number of capacitors resulting in an increased cost and reduced reliability. In contrast, SolarEdge topology uses an active capacitor circuit with an interphase balancing block, which reduces the size and cost of input bus and flying capacitors. Although the new inverter configuration introduces a large number of additional switches in the circuit, they are operated at low voltage and high frequency helping to increase efficiency and reduce the size and cost of passive components. In comparison to conventional inverters on the market, SolarEdge HD-wave inverter has smaller magnetics and fewer cooling components. In addition, the use of active power filtering

Figure 3.19: SMA transformerless single-phase inverter [75].

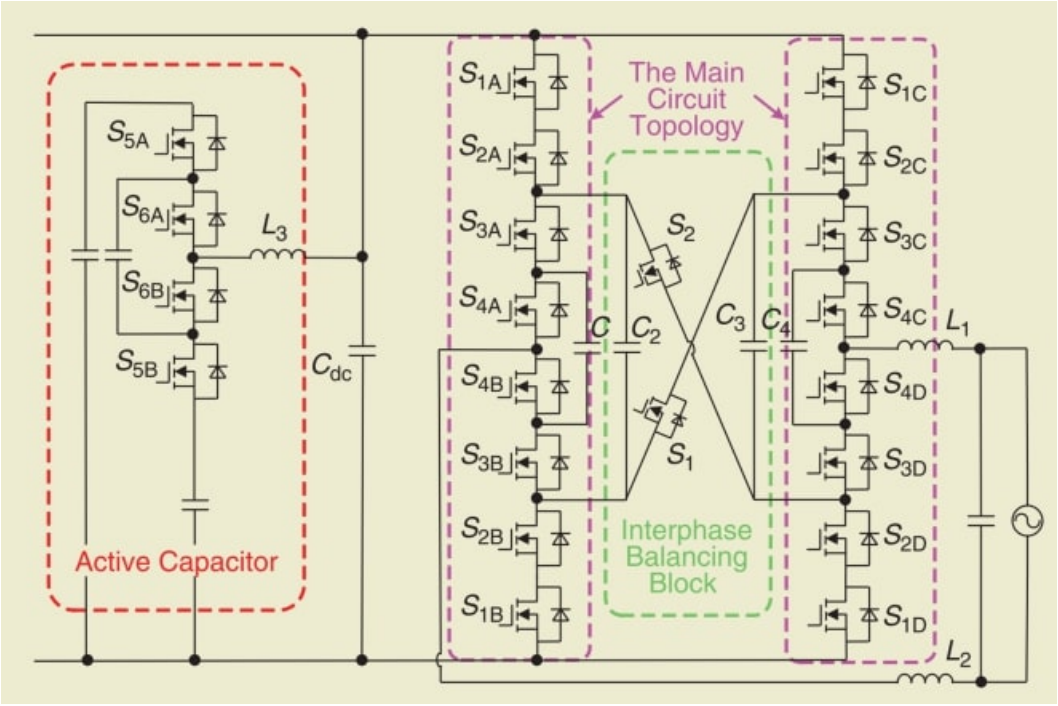


Figure 3.20: Five-level flying-capacitor topology of SolarEdge [46].

Figure 3.21: 7.6 kW SolarEdge HD Wave inverter [74].

enables the use of thin-film capacitors instead of electrolytic, thus improving the reliability of the system [46].

3.5 Design for Reliability of PV Inverters

The reliability of power converters depends heavily on the performance of each component in the converter. For instance, factors such as ambient/operating temperature, design defect, power level, moisture, and material wear out cause component-level failures leading to overall system-level failure. According to field data, components such as power devices, capacitors, gate drivers, and fans are generally responsible for failures in PV inverters [76]. However, the power semiconductor devices and capacitors have been reported in [77, 78, 60] and [79] as the main lifetime limiting components of the system. Among all the components in a PV inverter, power semiconductor and soldering failure contributed 21% of all failures while capacitors contributed approximately 30% of the failures [80, 81, 61, 79]. Thus, the reliability analysis of power devices and DC link capacitors is essential to accurately predict the lifetime of the PV inverter in particular and that of the lifetime cost of energy of the overall PV system in general. Over the years, the common method for reliability assessments of electronics components has used the Military Handbook 217 (MIL-HDBK-217) to compute the Mean Time Between Failure (MTBF) or Mean Time to Failure (MTTF) [82]. The technique employed in this handbook assumes a constant failure rate and uses a static approach where the reliability models of components are already determined. This reliability modeling technique is outdated for new technologies, vague on the failure mechanism, data type, and does not consider different operating conditions. For instance, solar irradiance and ambient temperature are two factors considered as mission profiles of the system that affect the power production and lifetime of PV inverters [78]. To address this shortcoming, the physics of failure-based reliability models have been developed taking into account different modes of failures in power electronics. These new models take into account components' physical structure, internal material characteristics and operational conditions such as temperature [11]. In addition, integrating reliability analysis as part of the design phase is important. For instance, the design for reliability (DfR) technique using Monte Carlo approach proposed

in [23] is used to estimate the reliability of PV inverters. This approach has been widely employed in [83, 78, 11]. Fig. 3.22 shows an example flow diagram of this technique. First, the dynamic parameters such as junction temperature ($T_{j,m}$) and temperature swing (ΔT_j) for a given mission profile are translated into an equivalent static value to be used in a Monte Carlo simulation of individual components with n samples. From the obtained lifetime estimation, a Weibull lifetime distribution is deduced. Next, the reliability or the percentile lifetime (B_x) of each component is evaluated through the cumulative density function (CDF). Finally, the total converter level reliability is calculated based on its component configuration (series, parallel, or both). Thus, to accurately model the reliability of the PV inverter, it is essential to first model the lifetime of the PV inverter's critical components such as the DC-link capacitor and power devices (i.e. MOSFET and GaN). These have been established to be the major life-limiting components and failure modes of the PV inverter [78].

3.5.1 Lifetime Model of DC Link Capacitors

Lifetime models are essential to accurately predict the lifetime and quantify the performance of different capacitor technologies. Three types of capacitors are widely used for dc-link application: Aluminum Electrolytic Capacitors (Al-Caps), Metallized Polypropylene Film Capacitors (MPPF-Caps), and Multi-Layer Ceramic Capacitors (MLC-Caps). The underlying technology of each capacitor is unique and presents advantages and limitations. For example, Al-Caps have the highest energy density and lowest cost per joule but exhibit high wear-out issues due to electrolyte evaporation, high ESR, and low ripple current rating. In contrast, MLC-Caps are expensive and mechanically unstable. They are prone to insulation degradation and flex cracking. On the other hand, they have a smaller size, wider frequency range, and can operate at a much higher temperature. Lastly, the MPPF-Caps exhibit a large volume and moderate upper operating temperature in comparison to both Al-Caps and MLC-Caps. They are highly susceptible to corrosion due to moisture and dielectric loss. Nonetheless, they have a well-balanced performance in terms of cost, ESR, capacitance, ripple current, and reliability [84].

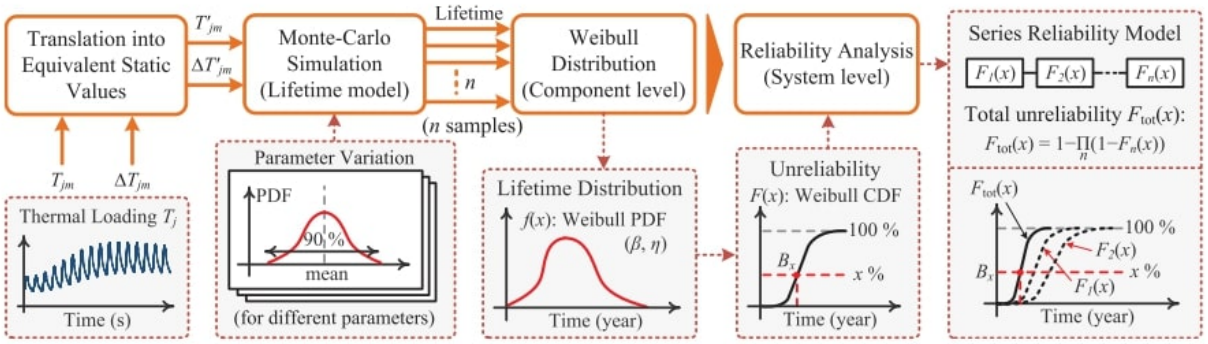


Figure 3.22: Flow diagram of the Monte Carlo-based reliability assessment of PV inverters with the reliability block diagram [83]

In modeling the lifetime of capacitors, operating temperature and voltage rating are the two major stress factors that are considered. A widely used lifetime model of capacitors taking those factors into account is

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times \exp\left[\left(\frac{E_a}{K_B}\right) \times \left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \tag{3.1}$$

where L, V, and T are the lifetime, voltage, and temperature in Kelvin under the use condition while L_0, V_0, and T_0 are the same parameters under testing condition respectively. E_a is the activation energy, K_B is Boltzmann's constant (8.62×10^{-5}eV/K) and n is the voltage stress exponent [85]. Next, a simplified model derived from 3.1 is often used for electrolytic and film capacitors,

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times 2^{\frac{T_0 - T}{10}} \tag{3.2}$$

where E_a=0.94 eV and T_0 is represented by 398 K. In addition, a more generic model has been proposed to provide physical explanations of the lifetime model variants from different capacitor manufacturers. In this model,

$$L = L_0 \times \exp\left[a_1 \left(V_0 - V\right)\right] \times \exp\left[\frac{E_{a0} - a_0\xi}{K_B T} - \frac{E_{a0} - a_0\xi_0}{K_B T_0}\right] \tag{3.3}$$

ξ and ξ_0 depicts the voltage and/or temperature stress variables under operation and test condition respectively. Constants a_0 and a_1 illustrate the voltage and temperature dependency of E_a while E_{a0} is the activation energy under test [85].

The lifetime models of dc-link capacitors are hugely affected by operating voltage and temperature including both ambient and operational.

3.5.2 Lifetime Model of Silicon Power Devices

Silicon power semiconductor devices have been in use for so many years that there is a wealth of operational and test data to accurately model their lifetime. Their failure mechanisms and related causing factors have been studied extensively and are well understood. Thermo-mechanical stress, including temperature cycles, bond wire lift-off, and base plate solder

failure has been determined to be the main cause of failure in silicon power devices such as IGBTs [86, 87, 88]. Several empirical lifetime models based on this failure mechanism have been developed over the years and are expressed as a number of cycles to failure (N_f). Despite different variations and techniques for lifetime models of power devices, there are three major models based on the Coffin-Manson model

$$N_f = A \cdot (\Delta T)^{-n} \tag{3.4}$$

where a and n are parameters that depends on the module design, and (ΔT) represent the temperature swing [89]. In addition, all three models indicate that the number of failures in a power module mainly depends on the junction temperature variation ΔT_j, and the mean junction temperature $T_{j,m}$. Thus, the LESIT model established in [90] is a modified Coffin-Manson model with an Arrhenius term considering the effect of junction temperature stress. The LESIT model is

$$N_f = A \cdot (\Delta T_j)^{-n} \cdot \exp\left(\frac{E_a}{k_B \cdot T_{j,m}}\right) \tag{3.5}$$

with $\Delta T_j = T_{j,max} - T_{j,min}$ and $T_{j,m} = (T_{j,max} + T_{j,min})/2$. K_B is Boltzmann's constant, while the activation energy E_a, a and n are model parameters. Next, Bayerer's Model, also known as the CIPS2008 model, similarly describes the temperature impact based on the basic Coffin-Manson term,

$$N_f = A \cdot (\Delta T_j)^{\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{j,max}}\right) \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \tag{3.6}$$

however this model considers additional factors such as device heating time (t_{on}), the absolute maximum junction temperature ($T_{j,max}$), the current per bond wire stitch (I), the bond wire diameter (D), and the device blocking voltage (V) [86]. The third lifetime model introduced in [87] by SEMIKRON

$$N_f = A \cdot (\Delta T_j)^{\alpha} \cdot ar^{\beta_1 \cdot \Delta T_j + \beta_0} \cdot \left(\frac{C + t_{on}^{\gamma}}{C + 1}\right) \cdot \exp\left(\frac{E_a}{k_B \cdot T_{j,m}}\right) \cdot f_{diode} \tag{3.7}$$

considers power cycling test results with Semikron SKiM power modules featuring standard Silicon IGBTs and diodes. This new model not only includes the thermomechanical stress of bond wires, it considers the impact of cycle period (t_{on}), bond wire aspect ratio ar, and the diode. A, α, β_0, β_1, γ and C are model parameters that can be obtained by curve fitting using simulation or experimental data [91].

The LESIT, CIPS2008, and SEMIKRON models are all solely derived from empirical data for silicon devices and have demonstrated good lifetime estimations [89]. With the recent push for the wide adoption of SiC and GaN power devices, these same models have been used to estimate their lifetime often leading to erroneous estimation. Thus, new lifetime models based solely on wide bandgap power modules are essential to accelerate their worldwide acceptance.

3.5.3 Lifetime Model of GaN Power Devices

Gallium Nitride (GaN) power devices are an emerging technology that has enabled the design of high-efficiency and high-frequency converters due to their exceptional material properties [92]. For instance, their high breakdown field and high mobility allow for the design of power devices with lower ON resistance. In addition, their saturation velocity and lower capacitance enable faster switching transients resulting in lower switching losses in comparison to Silicon devices with comparable voltage and current [93, 94, 95, 96, 97]. Current reliability testing of these devices are based on the JEDEC (Joint Electron Device Engineering Council) and AEC (Automotive Electronics Council) standards established for Silicon MOSFETs and IGBT devices. Given their different material properties, GaN devices may not respond the same way as Silicon devices given the same test conditions. In addition, all GaN devices currently available on the market do not use the same technology, thus, different reliability qualification standards may be required. To address this challenge, the working group within the JEDEC JC-70 committee has been making progress towards defining a set of tests, conditions, and pass/fail criteria to evaluate the reliability of GaN devices for a given mission profile [98]. One of the major challenges for GaN power transistors is to achieve normally-off operation, which is required for the safe operation of the system [99]. A GaN-HEMT is inherently a depletion mode (d-mode) normally-ON device which is undesirable for voltage source

converters because of the potential for shoot-through during start-up or loss of control power [100]. The basic depletion-mode transistor is shown in Fig. 3.23. A two-dimensional electron gas (2DEG) is created by the piezoelectric polarization at the heterojunction between GaN and AlGaN taking advantage of the inherent high sheet carrier density caused by the built-in polarization electric field. The source and drain electrode pierce through the AlGaN layer to form an ohmic contact with the 2DEG pool creating a short circuit between the drain and the source. To turn the device off, a negative voltage must be applied to the gate depleting the electrons in the 2DEG out of the device. In power electronics applications, this type of GaN device poses a challenge. At the startup of the converter, a negative bias must first be applied to avoid a short circuit.

To remedy these shortcomings of the depletion-mode (d-mode) type GaN, enhancement mode (e-mode) GaN has been developed. They are normally off and would not conduct current until a positive bias voltage is applied to the gate. Most GaN devices available on the market today are enhancement mode (e-mode) lateral devices that use processes such as recessed gate, implanted gate, p-GaN gate, and cascade hybrid to achieve normally-off operation [101]. Panasonic and Infineon's Gate Injection Transistor (GIT) GaN technology consists of a p-type AlGaN gate structure. As depicted in Fig. 3.24, a p-type AlGaN is placed over an AlGaN/GaN heterojunction to realize a normally-off operation. The p-AlGaN lifts the gate to the source threshold voltage and depletes the channel electrons under the gate. When the device is ON, $V_{gs} > V_{th}$, the injection of holes from the gate generates an equal number of electrons through conductivity modulation, resulting in high drain current and low on-resistance [99].

On the other hand, GaN Systems devices use an insulated gate structure technology but have not published information on their technology and how it operates. Lastly, Transphorm devices use a cascode structure which is a combination of a depletion mode GaN HFET with a low-voltage e-mode Silicon MOSFET as shown in Fig. 3.25. The two dies are connected in the same package such that the output drain to source voltage of the MOSFET sets the gate to source voltage of the GaN. Note that the blocking voltage is distributed between the two devices while off, and they conduct the same channel current while on [100].

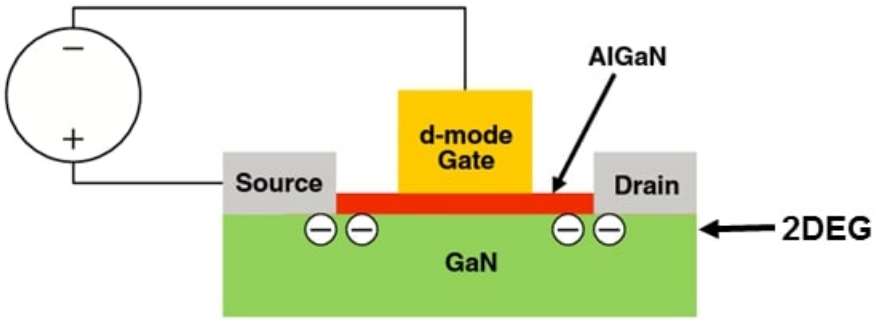


Figure 3.23: Depletion mode (d-mode) HEMT. By applying a negative voltage to the gate of the device, the electrons in the 2DEG are depleted out of the device [101].

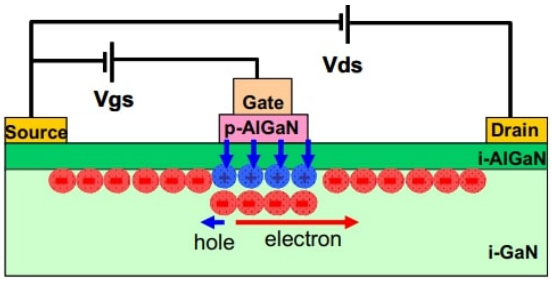


Figure 3.24: Cross section of a GaN-GIT showing a p-type AlGaN gate structure [99].

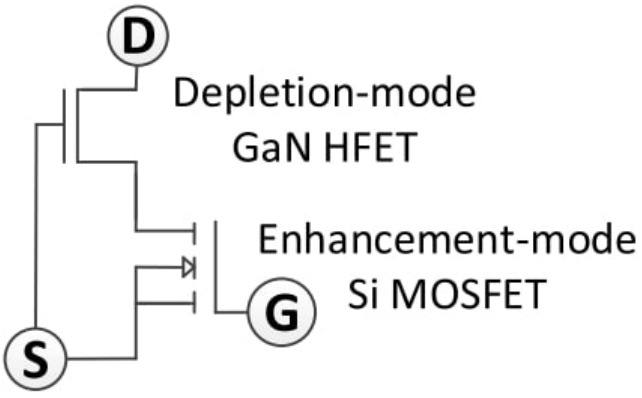


Figure 3.25: Normally-OFF GaN cascode device structure [100].

Current collapse at high drain voltage has been another main challenge of e-mode GaN transistors. This phenomenon is characterized by a dynamic ON-resistance that is proportional to the blocking voltage. It occurs because electrons get trapped when a high drain voltage is applied and may not dissipate immediately when the device switches on. The trapped electrons repel carriers in the channel layer, further reducing the number of carriers, thus increasing the ON-resistance of the channel [102]. Some GaN device manufacturers such as Panasonic have been able to mitigate the current collapse issue by introducing holes into the GaN device that instantaneously releases the trapped electrons. In 2015, Panasonic introduced a current-collapse free Hybrid Drain-embedded GIT (HD-GIT) GaN that operates up to 850 V. In the cross-section of the HD-GIT shown in Fig. 3.26, an additional p-GaN region has been introduced near the drain electrode and is electrically connected [102]. The recessed gate is used to thicken the AlGaN layer to avoid carrier depletion under the p-type region. Experimental measurements have shown the operation of the GIT without any current collapse up to 650 V.

Given the underlying differences in the technology based on the company, the outlined failure mechanisms may not be the same and differ from one device to the other. To generalized the lifetime assessment of GaN power devices, two types of tests are used to report the application relevant reliability results of GaN devices [103]. The first test is the Accelerated Lifetime Testing (ALT); it uses failure distribution plots to obtain wear-out models and calculate the device switching lifetime. The second, dynamic high-temperature operation life (D-HTOL) involves running the devices in an actual application circuit to validate the robustness, interactions with other components, and operating mode experienced during the product operation. Both testing methods are complementary to each other to ensure accurate lifetime models and reliable operation in an application. However, the lack of practical field reliability testing data to back up the accelerated lifetime model has been a major challenge in accurately evaluating the lifetime of GaN devices.

According to reliability analysis in [103], temperature, voltage, and current are the three stress factors that are essential in evaluating the switching lifetime of GaN FETs. However, based on the switching lifetime evaluation for hybrid-drain-embedded Gate Injected Transistor (HD-GIT) in [104] developed by Panasonic Corporation, the long time switching

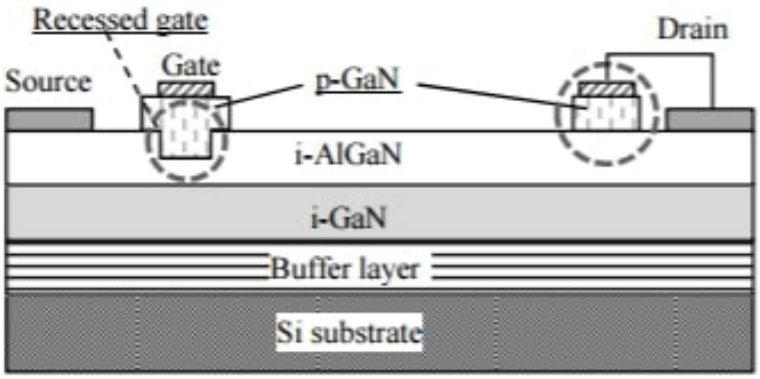


Figure 3.26: Cross section of a Hybrid-Drain-embeded GIT (HD-GIT) showing a p-GaN at the drain and a recessed-gate structure [102].

lifetime of their device depends strongly on the peak drain current and voltage. They have found that there is a weak correlation between temperature and the switching lifetime. The HD-GIT switching lifetime (τ) is calculated as

$$\tau(V_{DD}, I_{DP}) = A \cdot \exp\left[-\left(\beta_v \cdot V_{DD} + \beta_c \cdot I_{DP}\right)\right] \tag{3.8}$$

where A is a constant factor approximately equal to 1e5, β_v is the voltage acceleration factor and β_c is the current accelerated factor. The acceleration factor test of the voltage V_{DD} and current I_{DP} on the lifetime yielded that $\beta_v = 0.039$ and $\beta_c = 0.47$. Continuous tests to characterize the lifetime dependence on temperature yielded small activation energy of 0.1 eV, meaning that the lifetime of the device is weakly dependent on the temperature. As a result, thermal stress is not a major factor in the lifetime of GaN-GIT power transistors.

Building upon the work presented in [104] showing that the wear out from switching stress accumulates until failure, a generalized approach to estimate the switching lifetime of a GaN FET is introduced in [103]. First, for a given voltage and current applied to the device, the switching stress is

$$\Delta stress = V_{DS} \cdot AF(V) \cdot I_D \cdot AF(I) \cdot \Delta t \tag{3.9}$$

where V_{DS} and I_D are the instantaneous drain voltage and current respectively. $AF(V)$ and $AF(I)$ are the corresponding voltage and current acceleration factors. Next, the switching stress rate S_{sw} representing the transition stress with applied temperature, duty cycle, and switching frequency acceleration factors is

$$S_{sw} = [C \cdot \sigma_{Tr} \cdot AF(T) \cdot AF(D)] \cdot AF(f_{sw}) \tag{3.10}$$

C is a constant for normalization of units of hour and kHz, σ_{Tr} is the stress per switching transition and is determined by summing all the switching stress. $AF(T)$, $AF(D)$, and $AF(fsw)$ are the respective temperature, duty cycle, and switching frequency acceleration factors. Note that the term in square brackets is the switching stress applied to the device per hour when switching at 1 kHz. The time to failure (TTF) is given by

$$TTF = 1/S_{sw} \tag{3.11}$$

The switching lifetime model of GaN is calculated using the accelerated lifetime test requiring the acceleration factors (AF) to be determined first. However, not all device manufacturers have published the AF analysis data for their devices making the lifetime evaluation of GaN FETs under practical application challenging.

3.5.4 Component Level Reliability Assessment

The reliability of a component denoted as $R(x)$ is defined as the ability of a system or component to operate without a failure under stated conditions for a specified amount of time [105]. It also represents the percentage of a group of the sample or the probability that a sample can properly function for a given time t. The dual of reliability is unreliability, $F(x)$, and is expressed as the percentage failure of a group of a sample or the probability of failure during a given time x. Both $R(x)$ and $F(x)$ are expressed as

$$R(x) = 1 - F(x) = 1 - \int_0^x f(x)dx \tag{3.12}$$

where $f(x)$ is the Weibull probability density function

$$f(x) = \frac{\beta}{\eta^\beta} x^{\beta-1} \exp\left[-\left(\frac{x}{\eta}\right)^\beta\right]. \tag{3.13}$$

β is the shape parameter and η is the scale parameter, which can be obtained through curve fitting. As demonstrated in Eq. 3.12, the unreliability function, $F(x)$ can be defined by the cumulative distribution function (CDF)

$$F(x) = \int_0^x f(x)dx = \int_0^x \frac{\beta}{\eta^\beta} x^{\beta-1} \exp\left[-\left(\frac{x}{\eta}\right)^\beta\right] dx \tag{3.14}$$

Another reliability metric widely used in literature is the Mean Time Between Failure (MTBF) or Mean Time to Failure (MTTF). They are calculated as

$$MTBF = 1/\lambda \tag{3.15}$$

where λ is the component rate of failure, meaning the number of failures per unit of time that can be expected to occur for the product [106]. Eq. 3.15 assumes that λ is constant throughout the component lifetime, which is not the case for most power electronics components. In actuality, the failure rate generally follows the bathtub curve shown in Fig. 3.27 [105]. The curve has three intervals, given by the fitting parameter β.

The early stage where $\beta < 1$ is dominated by early failure due to infant mortality. The second interval where $\beta = 1$ exhibits a constant failure rate and is dominated by random failure i.e. overvoltage, overcurrent, overheating, or human error. Lastly, in the third stage, wear-out failure becomes dominant causing an increase in the failure rate with $\beta > 1$. This is mainly due to the end-of-life component degradation over time [23].

Assuming a constant failure rate ($\beta = 1$) is expected to occur throughout the lifetime of the component, as modeled in the MTTF, an exponential distribution can model the probability density function as

$$f(x) = \lambda \exp(-\lambda x) \tag{3.16}$$

Thus, the reliability is

$$R(x) = \exp(-\lambda x) \tag{3.17}$$

This model is a simplistic reliability metric that does not account for the time-dependent wear-out failures over time, which can lead sometimes to erroneous results. It represents the time of operation when 63% of the components have failed and the reliability is 37%. However, in many power electronics applications, a 90% reliability or above is preferred. Due to its limitation in properly evaluating the reliability performance of a component/system, the lifetime distribution function is often used. Given the reliability $R(x)$ or unreliability curve $F(x)$, the percentage lifetime denoted by $B_(x)$ has been widely demonstrated to be a better metric to quantify the reliability of the component/system. It represents the useful lifetime of a population of items, meaning a time by which a certain percentage of the population would have failed [85]. For instance, Fig. 3.28 shows the failure probability

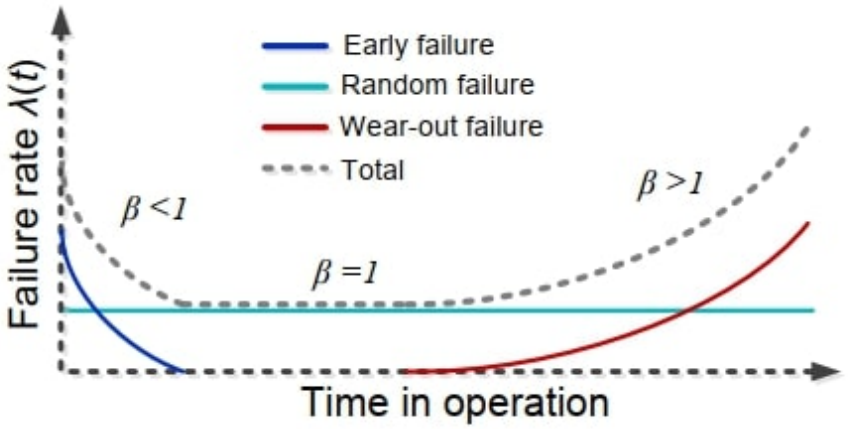


Figure 3.27: Bathtub curve or component failure rate curve [23].

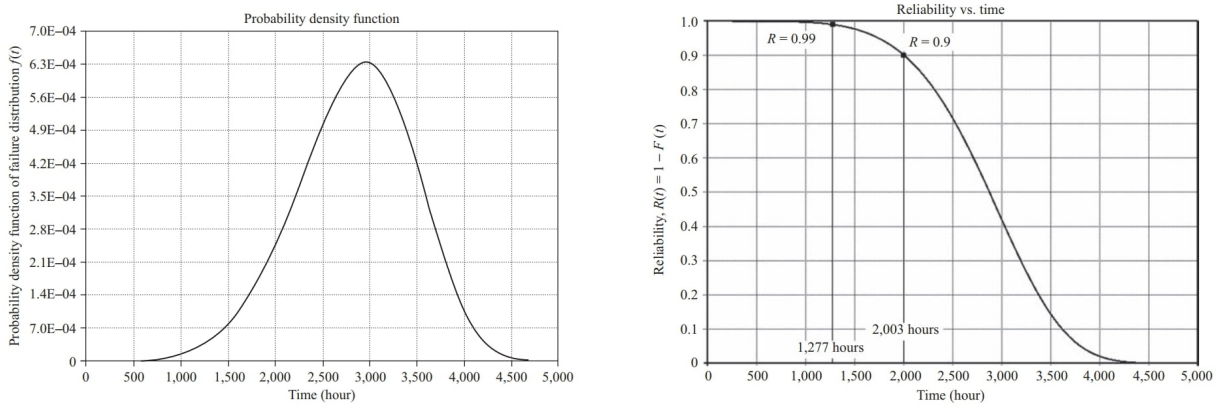


Figure 3.28: (a) failure distribution function and (b) reliability function $R(x)$ example for a group of capacitors [85].

distribution function (PDF) for a group of capacitors and their subsequent reliability function $R(x)$. The B_{10} lifetime, the time of operation where 10% of the capacitors have failed is 2003 hours. This corresponds also to 90% reliability. Furthermore, the MTTF, which is equivalent to a percentile lifetime of 63% (B_{63}) is 2700 hours.

Furthermore, there are several uncertainties and parameter variations in the lifetime estimation of components; as a result, Monte Carlo analysis is often used to model these variations [78, 83, 11]. The Monte Carlo technique introduces a variation in the component stress factor such as the mean junction temperature $T_{j,m}$, and temperature swing ΔT_j; the result is then simulated with a large number of samples. From the obtained set of lifetime estimation results, a Weibull distribution can be used as previously outlined to obtain the CDF or unreliability function. This method has been demonstrated in [83] to accurately estimate the lifetime of power devices and DC link capacitors for a given mission profile and variation in the lifetime model parameters.

3.5.5 Converter Level Reliability Assessment

The reliability analysis so far has focused on estimating the lifetime and reliability of a single component or a system with a single item. However, power converters have several components often arranged in a series, parallel configuration, or a combination of both. There are well-established analytical models that are used to calculate the simple series or parallel system arrangement. However, numerical simulation methods such as Monte Carlos simulations have also been recommended to compute the reliability of more complicated topologies [85]. This is often the case for a complicated system consisting of series and parallel arrangements of components.

3.6 Summary

High efficiency and power density have dominated the latest technological innovation trend in single-phase transformerless inverter design. However, string inverter reliability has lagged. Inverters are among the most vulnerable components in a PV system [24]. Their reliability performance has a significant impact on the levelized cost of energy (LCOE). High failure

rate contributes to a short system lifetime and an increase in operation and maintenance cost [22]. To address this challenge, most of the literature assumes that increasing the inverter reliability is a matter of eliminating the DC bus electrolytic capacitors by using active power filtering schemes which allows the use of more-reliable film capacitors. It is assumed that these capacitors provide higher reliability regardless of the circuit topology [70]. Though film capacitors certainly are more reliable than electrolytic capacitors, using them in a circuit does not automatically guarantee that the system will be more reliable. The addition of active switches and other components may change the reliability of the overall system [49]. Power devices also constitute one of the critical components in a converter and their reliability should be taken into account in the inverter power stage design to optimize for high reliability and efficiency. According to [21], the design for reliability should be adopted for the next generation of PV inverters with modular and redundant topologies in addition to new energy buffering techniques, and new semiconductor devices such as silicon carbide (SiC) and gallium nitride (GaN). It is essential to integrate reliability analysis using design for reliability (DfR) techniques in the inverter design stage to inform design choices and evaluate the lifetime performance for a given inverter architecture. To evaluate the merit of inverter topologies in comparison to other architectures, the LCOE is a good benchmark that helps to quantify the overall performance of the system. It encompasses the three important PV inverter design parameters: cost, efficiency, and reliability. It also provides a quantitative way to better design and evaluate the system performance.

Chapter 4

Dynamic Hardware Allocation

With recent advancements in power semiconductor technology, such as Gallium Nitride (GaN) and Silicon Carbide (SiC) transistors, power converters for PV applications have been able to reach a peak power efficiency of 99% and achieve a power density of 243 W/in^3 [14, 15, 16]. Despite these achievements, the reliability of PV inverters has been a limiting factor in PV systems, leading to significant downtimes [11]. PV converter topologies are depicted conceptually in Fig. 4.1. Traditional PV converter topologies are implemented using single-purpose power stages and passives as shown in Fig. 4.1a with bulky electrolytic capacitors used to decouple the double-line-frequency power. However, the inverter reliability and lifetime evaluation are impacted by the DC-link capacitor and power devices [78]. When used, electrolytic capacitors are the dominant component limiting the lifetime of the inverter. Longer lifetimes are obtained when power filtering is accomplished without the use of bulk electrolytic capacitors [107]. To address reliability challenges, a common approach is to use some type of active power filter (APF), as depicted in Fig. 4.1b, to reduce the required capacitance thus allowing the use of more reliable film or ceramic capacitors. Following the elimination of bulk electrolytic capacitors, further improvement of inverter lifetime requires consideration of the overall system architecture including power devices.

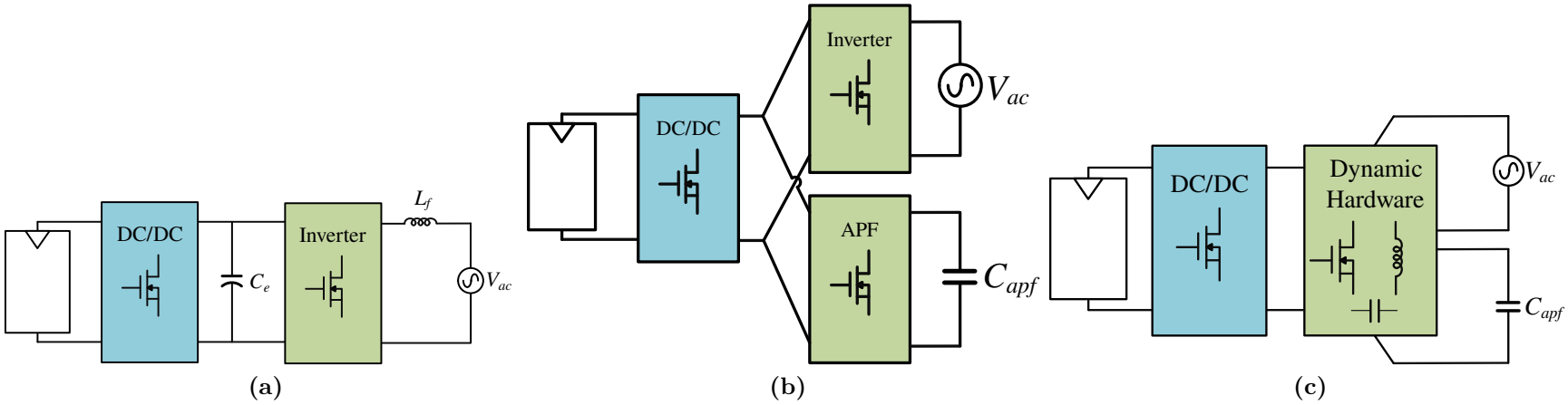


Figure 4.1: Conceptual PV converter topologies (a) traditional electrolytic-decoupled string inverter; (b) generalized diagram of APF-based system; (c) dynamic hardware-based (DHA) system.

To address these shortcomings of PV inverters, a new topological and control scheme using the concept of dynamic hardware allocation (DHA) is introduced and illustrated in Fig. 4.1c. In the proposed converter implementation, a common set of hardware resources shift operation between different conversion functions dynamically in time. Note that this is not a static, integrated topology that has dedicated pathways for each; instead, the system consists of a pool of identical modules that can be dispatched to perform a specified function, principally active power filtering (APF: double-line-frequency decoupling) and line frequency inverter operation. In addition, available modules can be reassigned in the event of a single failure of any element.

The benefit of this approach is multifold. First, the inverter lifetime and reliability are increased substantially because the pooled hardware resources can be re-assigned in the event of a single failure of any element. In the traditional architecture shown in Fig. 4.1(a-b), any semiconductor element is often a single point of failure (SPOF). If an inverter transistor fails, the system can no longer supply power to the grid. In the DHA scheme, if a transistor that is currently performing dc-ac inversion fails, the failure can be isolated and hardware resources are re-routed from alternate functions to replace it. Second, the modular nature of the system facilitates the use of high-reliability components, and allows for simple repair or maintenance through the replacement of individual modules instead of requiring a complete inverter replacement.

4.1 Basic Concept of Operation

The basic proposed single-phase BCM inverter architecture using the DHA scheme is shown in Fig. 4.2. This implementation consists of three high-frequency (HF) phases/modules and a single line-frequency (LF) return phase. A schematic of a single HF module is depicted in Fig. 4.3. Each of these modules is a zero-voltage switching half-bridge employing a dual-current programmed mode (DCPM) control [108, 109] with a low-frequency reference V_{ref} to achieve boundary current mode (BCM) switching [110]. The pair of switches S_{inv} and S_{apf} control the hardware allocation, allowing the module to function as an inverter, shunt APF,

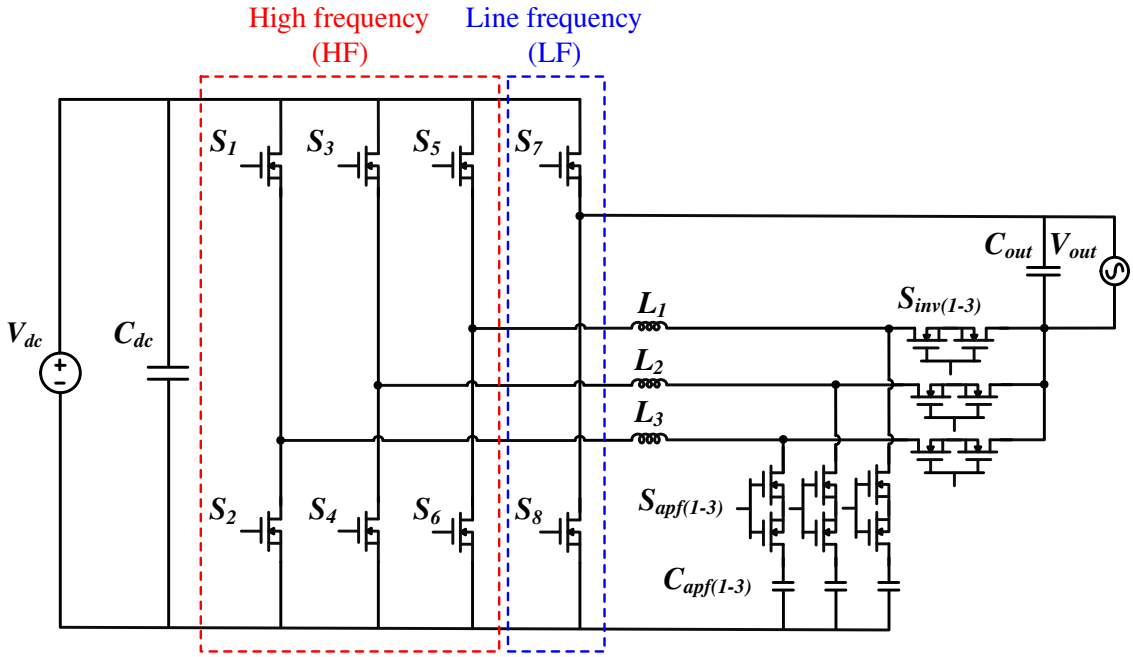


Figure 4.2: Proposed DHA inverter topology.

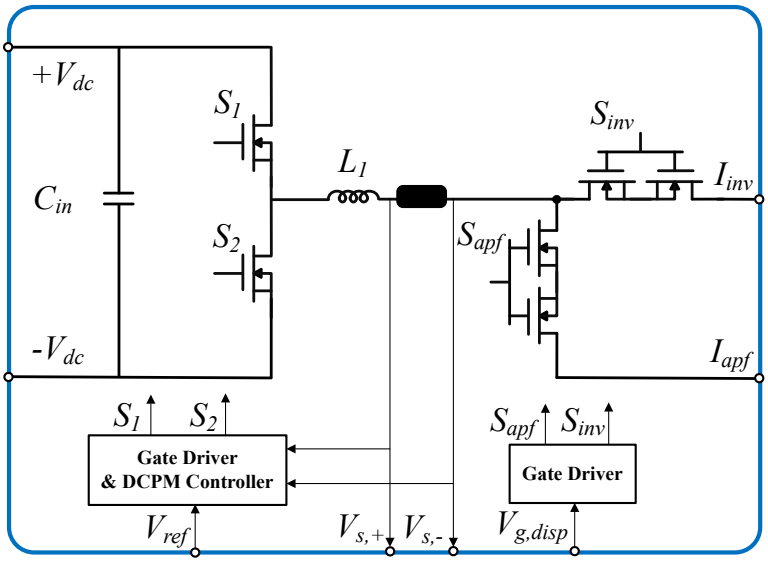


Figure 4.3: DHA inverter high-frequency module schematic.

or idle. The design and implementation of the high-frequency DCPM controller to achieve BCM modulation are discussed in Chapters 5 and 6.

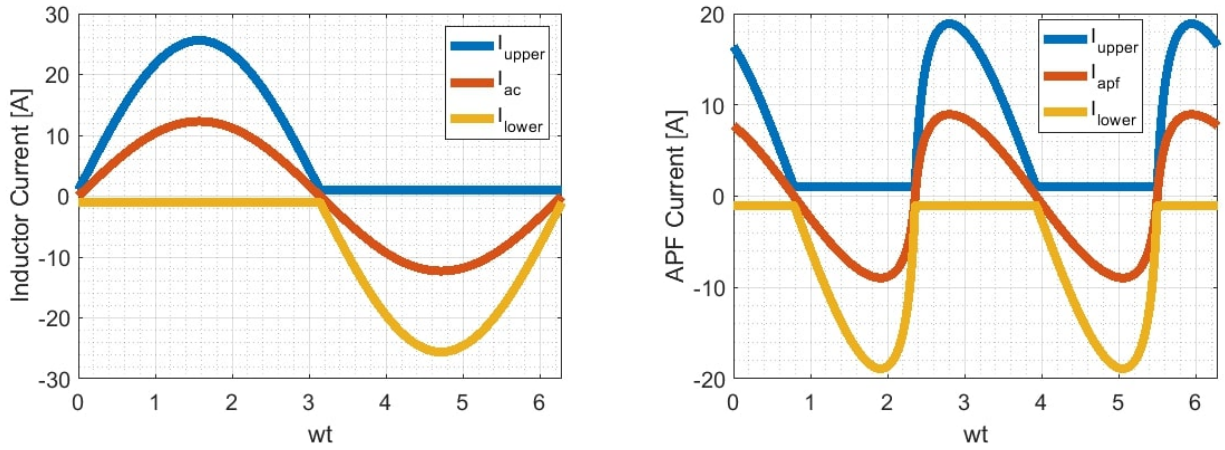
The DHA approach exhibits the same potential advantages of a traditional soft-switching multiphase converter: current sharing among modules, phase shedding, and ripple cancellation. In addition, the DHA is able to dynamically dispatch each high-frequency module to either do APF or inverter operation. In an example case, the DHA may use the majority of the modules for inverter operation during the peak output current, and the majority for APF operation during the output current zero-crossing to reduce peak current stresses. When the dispatching scheme is optimized, DHA has the potential to improve both the efficiency and lifetime of a Non-DHA implementation with the same hardware. The power loss and reliability model are derived next and used to evaluate the reliability performance of the DHA inverter with BCM operation.

4.2 Power Loss Model

To analyze the impact of the switching scheme on the overall DHA converter and reliability, the module-level power loss for the half-bridge module is derived. Based on the applied switching technique, both the inductor and device losses are the main contributor to the power loss. Fig. 4.4 shows the inverter current (I_{ac}) and APF current (I_{apf}) for a 2 kW system using BCM modulation. In this switching technique, the expected maximum inverter and APF current I_{upper} can reach well over twice the peak output current. The ZVS current is set by (I_{lower}). Other forms of losses such as shunt resistor and APF equivalent resistance capacitor do not vary significantly with different switching techniques. First, a basic loss model computes the DC-DC power loss at each operating point, then averages it over the line cycle for the entire module loss.

4.2.1 Switching Loss Analysis

The switching frequency in the unipolar switched BCM inverter varies along the line cycle and is at its maximum near the zero crossings. The resulting frequency can reach values in the MHz range, so it is important to limit the frequency to a range that guarantees noise



(a) **(b)**

Figure 4.4: Estimated peak and average inductor current for (a) Inverter and (b) APF operation at 2 kW.

immunity and a good performance of the control [108, 109]. Thus, a minimum ON/OFF time of 200 ns and a maximum switching frequency of 800 kHz are selected, based on the DCPM controller design in Chapter 5. These limits constrain the selection of inductance and the reverse conduction current required to achieve ZVS. For an inductance of 20 µH, Fig. 4.5 shows the relationship between the ZVS current and the switching frequency for a given average inductor current. For instance, for an average inductor current above 3.5 A, the reverse conduction current can be set to a minimum of 1.1 A to achieve ZVS while keeping the switching frequency to below 800 kHz. Near the output current zero-crossing, where the current is at its minimum, the minimum ZVS current needs to be extended to 3 A to limit the switching frequency.

The power stage switches are implemented using GaN devices. The device losses primarily consist of the conduction and switching losses (P_{cond}, P_{sw}). The former depends on the current flow through the devices, while the latter is mainly due to the energy loss during the turn-off of the GaN devices and the reverse conduction of the devices during the deadtime. Using BCM modulation, ZVS is achieved throughout the line cycle; however, it is not without any switching losses. The loss analysis for a single module consisting of a half-bridge and the allocation switches, includes device switching loss P_{sw} and conduction loss P_{cond} for every switching period and averaged over the line cycle as

$$P_{dev,loss}(t) = \frac{2}{T_s}\int_0^{T_s/2}(P_{sw} + P_{cond})dt. \tag{4.1}$$

The half-bridge soft-switching loss P_{sw} is comprised of both device turn off loss, P_{toff} and the reverse conduction loss, P_{rc}

$$P_{toff} = E_{off,zvs} \cdot f_s$$
$$P_{rc} = V_F \cdot I_{peak} \cdot dt_{rc}$$

Unlike hard switching transitions, where the energy E_{oss} stored in the the active device output capacitor is lost in the device during its turn-on transition, in soft switching transitions, the stored energy is recovered and not lost. However, this energy transfer is

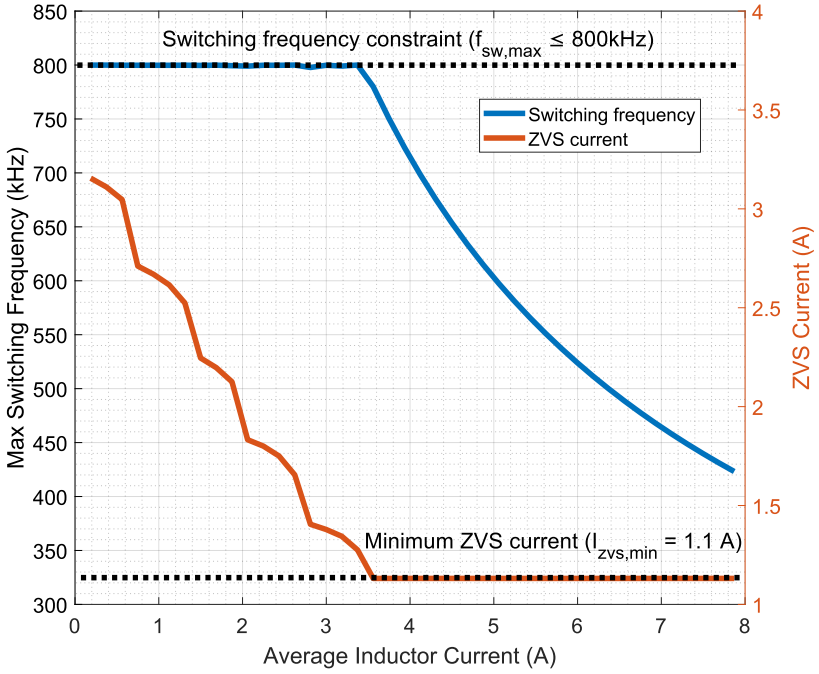


Figure 4.5: Relationship between the ZVS current I_{zvs} and maximum switching frequency for a given average output current I_{out}.

not without loss. The voltage and current may still overlap during the turn-off transient causing a small energy loss $E_{off,zvs}$. In [111] it has been demonstrated that this energy can be approximated by subtracting the device output capacitance energy E_{oss} from the hard switching energy during turn off

$$E_{off,zvs} = E_{off} - E_{oss}. \tag{4.2}$$

The reverse conduction loss P_{rc} is a function of the switch reverse conduction forward voltage drop V_F, the peak inductor current I_{peak} and the period dt_{rc} during which the device is conducting. GaN devices usually exhibit a significant voltage drop. Thus, SiC-diodes with much lower voltage drop are placed in an anti-parallel position to the GaN device to keep the voltage drop low [112]. In addition, the deadtime could dynamically be adjusted in such a way to minimize the soft-switching transition period such that the reverse conduction time is minimized

Next, included in the conduction loss (P_{cond}) is all the device's conduction loss due to its ON-resistance $R_{ds(ON)}$ and that of the shunt resistance (R_{shunt}) used for the current sensing for the DCPM control. Given the RMS current flowing through the switch, the conduction loss is given by

$$P_{rds(ON)} = I_{rms}^2 \cdot R_{ds(ON)} \tag{4.3}$$

and

$$P_{shunt} = I_{rms}^2 \cdot R_{shunt}. \tag{4.4}$$

4.2.2 Magnetic Loss

Given the modular nature of the system, low-profile PCB trace winding planar magnetics are employed in this converter implementation. The magnetic loss during half a line cycle consists of both winding loss P_{cu} and core loss P_{fe}

$$P_{mag,loss}(t) = \frac{2}{T_s}\int_0^{T_s/2}(P_{fe} + P_{cu})dt. \tag{4.5}$$

The former results from non-ideal current conduction in the copper wires and can be calculated as a combination of the RMS current (I_{rms}) flowing through the winding and the resistance of the winding itself both at DC and AC

$$P_{cu} = I_{rms}^2 \cdot (R_{L,DC} + R_{L,AC}). \tag{4.6}$$

The DC resistance $R_{L,DC}$ is straightforward and can be approximated given the core geometry and the number of turns. On the other hand, the AC resistance $R_{L,AC}$ is much more challenging to estimate and is caused by eddy currents present in the conductor. These result from fringing, proximity, and skin effects and are much more prevalent at high-frequency [113]. Various design and modeling techniques developed in [114, 115, 116, 117] and [118] can be used in combination with finite-element analysis tools to estimate these effects. In a multi-layer winding, where the copper thickness h is less than the skin depth of the conductor δ, the proximity effect is often the dominant form of loss and increases rapidly with frequency. The ratio of AC to DC resistance can be approximated as

$$\frac{R_{ac}}{R_{dc}} = 1 + \frac{(\pi N_s)^2 \cdot h^6}{192 \cdot \delta^4 \cdot b^2} \tag{4.7}$$

where N_s is the number of turns per section, and b is the breadth of the winding as shown in Fig. 4.6 [119]. After surveying available planar cores for high-power, high-frequency applications, the EI38 planar core geometry with the high-frequency core material 3F36 from Ferroxcube is used to implement the inductor. The core parameters are summarized in Table 4.1.

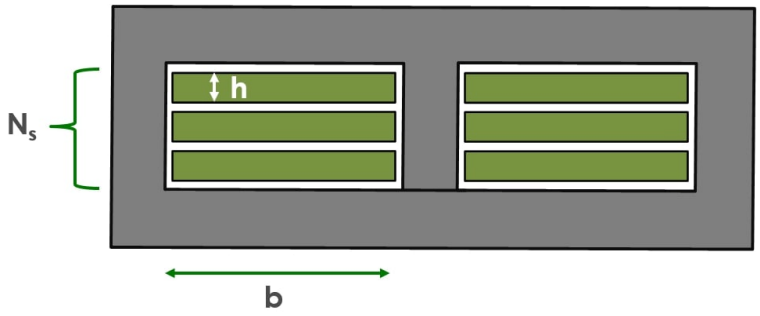


Figure 4.6: Example 2D drawing showing important dimensions for an inductor design. h is copper thickness, N_s is the number of turns and b is the copper width.

Table 4.1: Inductor Core Parameters

Core Type	Material	A_c (cm^2)	MLT (cm)	l_m (cm)	Vol (cm^3)
EI38	3F36	1.94	6.6	4.37	8.46

The core loss density, in Watts per cubic centimeter of core material is modeled using the general Steinmetz equation [120] for every switching period and averaged over the line cycle,

$$P_{fe} = \frac{2A_c \cdot l_m}{\pi} \int_0^{\pi} (K \cdot f_s(\theta)^{\alpha} \cdot \Delta B(\theta)^{\beta}) d\theta \tag{4.8}$$

where A_c represents the core cross-sectional area and l_m is the mean magnetic path length. The core material parameters K, α, and β are provided by the core manufacturer.

4.2.3 Phase Allocation

With the module-level power loss model developed, the device and magnetic loss model are used to determine the allocation that would yield the lowest converter loss for a given number of phases. In this analysis with a total of 3 HF modules ($n = 3$), a simple search algorithm loops through the total number of modules and computes the losses for each possible allocation, at each point in the line cycle.

Fig. 4.7a shows the analytical waveform of the powers, currents and voltages in an inverter and APF operation with its subsequent phase allocation during the positive half cycle. This plot is based on a unity power factor for a 2 kW average power system, an output voltage of 240 V_{rms} at 60 Hz and an APF capacitor value of 100 µF which is enough to meet the energy and capacitance requirements to buffer the second-harmonic ripple power on the DC side [121]. Starting at $\omega t = 0$, there are 2 modules locked into APF operation ($n_{apf} = 2$) while one module is allocated for the inverter ($n_{inv} = 1$). At $\omega t = \omega t_1$, the allocation switches to 2 phases in inverter mode ($n_{inv} = 2$) while only one phase is in APF mode ($n_{apf} = 1$) throughout the peak inductor current. At $\omega t = \omega t_2$, when APF is transitioning to peak APF current, the allocation switches back to $n_{apf} = 2$ and $n_{inv} = 1$. All waveforms are identical in the negative half-cycle. In the case of Non-DHA scheme shown in Fig. 4.7b, the multiphase inverter consists of 4 HF modules ($n = 4$) with two phases locked in inverter mode ($n_{inv} = 2$) while the remaining two phases perform APF operation ($n_{apf} = 2$). The allocation is static and does not change throughout the line cycle.

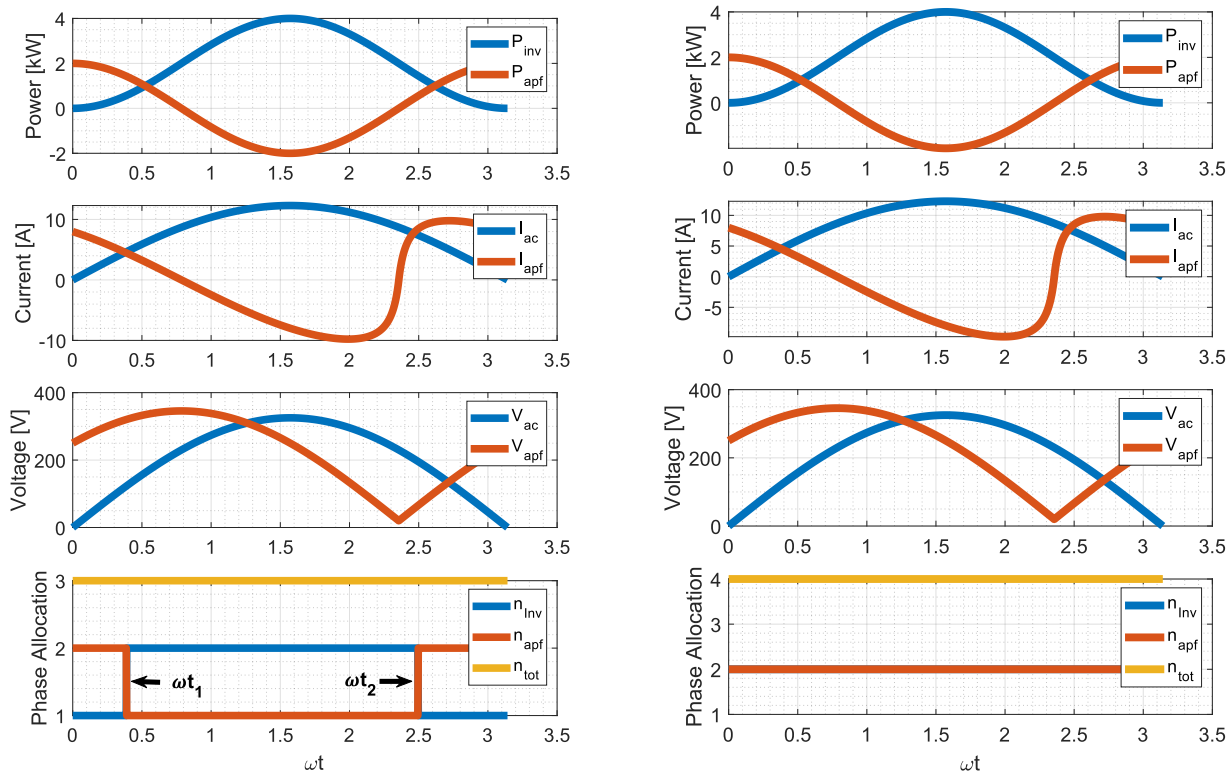


Figure 4.7: Analytical waveform showing inverter and APF power (P_{inv}, P_{apf}), average output AC current and APF current (I_{ac}, I_{apf}), average output AC voltage and APF capacitor voltage (V_{ac}, V_{apf}) and phase allocation (n_{inv}, n_{apf}) for 2 kW (a) 3 module DHA system and (b) 4 module Non-DHA system.

4.3 Design for Reliability

The current state-of-the-art design for reliability (DfR) technique proposed in [23] is used to predict the lifetime, failure rate, and design robustness of individual components in order to design the inverter. This method takes full consideration of the operating condition, commonly denoted as mission profile, which is important in the lifetime calculation. For PV systems, the ambient temperature and solar irradiance of the location are the two important parameters in establishing the operating condition of the inverter. Fig. 4.8 shows both parameters for a PV system installed in Phoenix, AZ, which is used as the base location for the analysis. Furthermore, statistical analysis coupled with components lifetime models are used to predict the reliability of the system. The proposed multiphase inverter with DHA uses 3 high-frequency modules ($n = 3$) for both inverter and APF operation, while the non-DHA uses a set of 2 high-frequency modules for each operation ($n = 4$). The converter design parameters for a 2 kW PV system are given in Table 4.2. Table 4.3 provides the list of the components employed in this analysis.

4.3.1 Monte Carlos-Based Lifetime Evaluation and Mission Profile

In order to determine the inverter level reliability, the lifetime of individual components is first evaluated using Monte Carlo simulation, where the stress factors of each component are varied. The ambient temperature T_a and solar irradiance from the mission profile, are the factors that have a large influence on the lifetime of components. The ambient temperature shown in Fig. 4.8, can reach a maximum of 47 °C in the summer. In the case of power devices for instance, it directly affects the device junction temperature T_j and temperature swings ΔT_j. Given that the operating condition is dynamic and changing throughout the year, it makes it even more challenging to apply parameter distribution to T_j and ΔT_j in the Monte-Carlo simulation. As a result, equivalent static values are used and have been shown in [83] to yield the same results as using dynamic variables.

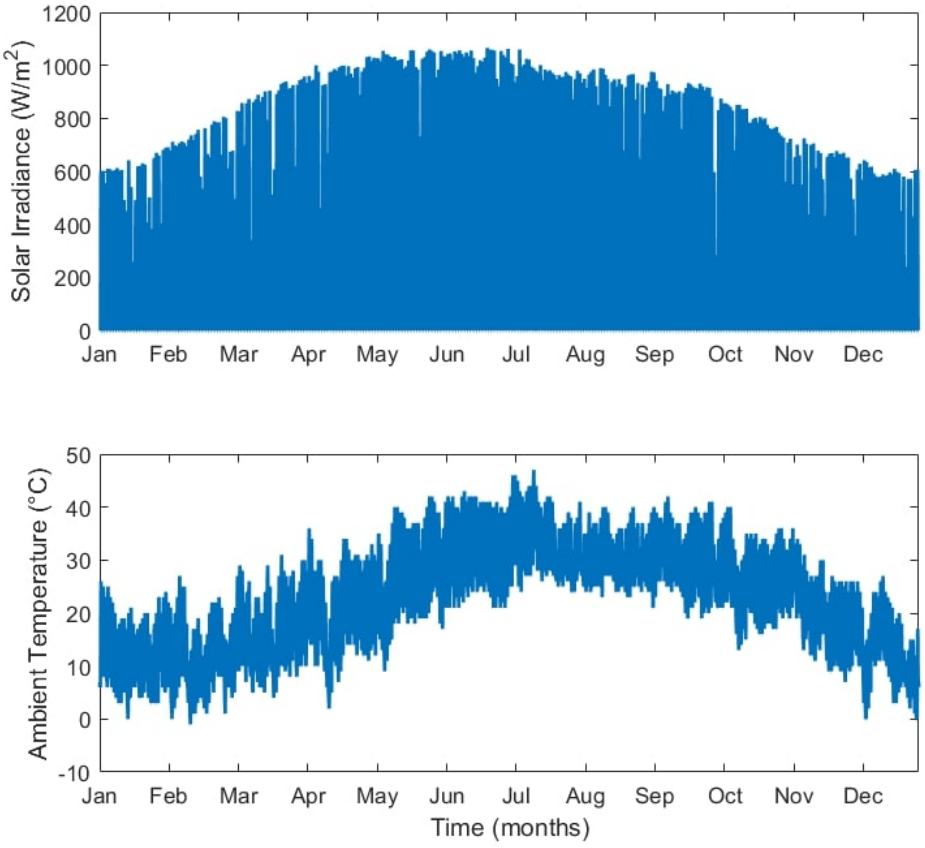


Figure 4.8: Yearly mission profiles including solar irradiance and ambient temperature in Phoenix, AZ [122].

Table 4.2: Converter Design Parameters

Parameter	Label	Value
PV rated power	P_{dc}	2 kW
DC-link voltage	V_{dc}	400 V
AC output voltage	V_{ac}	240 V_{rms}
Switching frequency	f_{sw}	$\leq$ 800 kHz
Grid frequency	f_{line}	60 Hz
Module inductor	L_i	20 µH
APF capacitor	C_{apf}	100 µF

Table 4.3: Summary of Components Used in the Analysis

Parameter	Type	Value
GaN	GaN-GIT	600V/70mΩ (PGA26E07BA)
MOSFET	CoolMOS	650V/33mΩ (IPT65R033G7)
Capacitor	MPPF	650 V/110 µF (C4AQCEW6110A3AJ)

4.3.2 Film Capacitors

First, the two stress factors that have a huge influence on capacitor reliability are operating temperature and voltage. From a PV inverter reliability standpoint, Metallized Polypropylene Film Capacitors (MPPF-Caps) have a well-balanced performance in comparison to both ceramic and electrolytic capacitors. For a 2 kW system using active power filter technique, a 100 µF capacitor is calculated to satisfy the inverter energy requirement. Thus a 650 V/110 µF (C4AQCEW6110A3AJ) film capacitor from KEMET corporation is selected. Fig. 4.9 shows the manufacturer's lifetime testing data illustrating the relationship between the voltage and temperature on the lifetime expectancy of the capacitor.

As expected, the lifetime of the capacitor rapidly degrades as its hot spot temperature increases. However, the capacitor is expected to operate up to 100,000 hrs for hot spot temperatures below 70 °C. The following equation is used to calculate the expected capacitor hot spot temperature

$$T_{HS} = T_{amb} + \Delta T \tag{4.9}$$

and

$$\Delta T = ESR \times I_{rms}^2 \times R_{th(th-a)} \tag{4.10}$$

where I_{rms} is the expected RMS current through the capacitor. $R_{th(ht-a)}$ is the hot spot to ambient thermal resistance. Given the mission profile in Phoenix, AZ where the ambient temperature can reach up to 47 °C in the summer, the capacitor temperature swing must be kept below 23 °C ($\leq$ 23 °C). Fig. 4.10 shows the estimated capacitor hot spot temperature based on mission profile in Phoenix, AZ for a 2 kW rated unipolar BCM module. The maximum operating temperature is expected to be below 60 °C.

Next, the lifetime model of the MPPF-Cap is given by

$$L_c = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times 2^{\frac{T_0 - T}{10}} \tag{4.11}$$

where V_0, L_0 and T_0 are the rated voltage, lifetime and temperature respectively under manufacturer testing conditions. V is the voltage and T is the temperature at operating

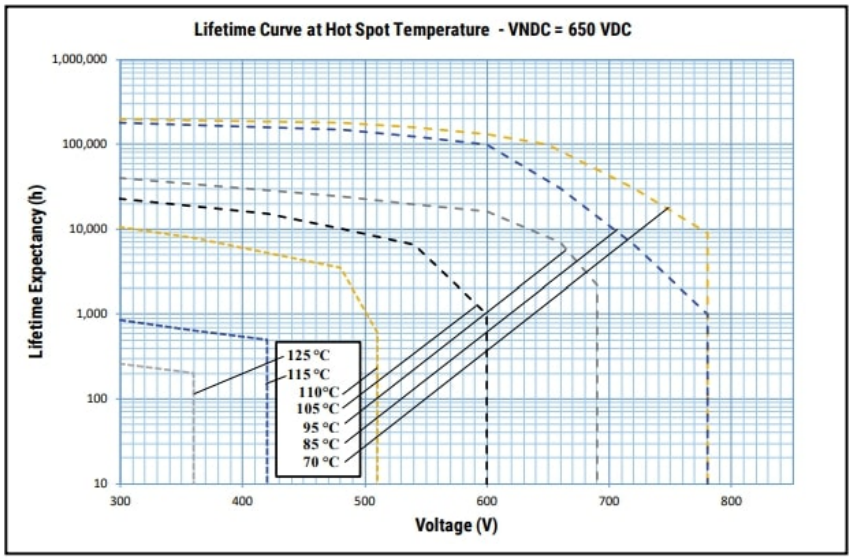


Figure 4.9: Lifetime Curve at Hot Spot Temperature at nominal VDC=650 V [123].

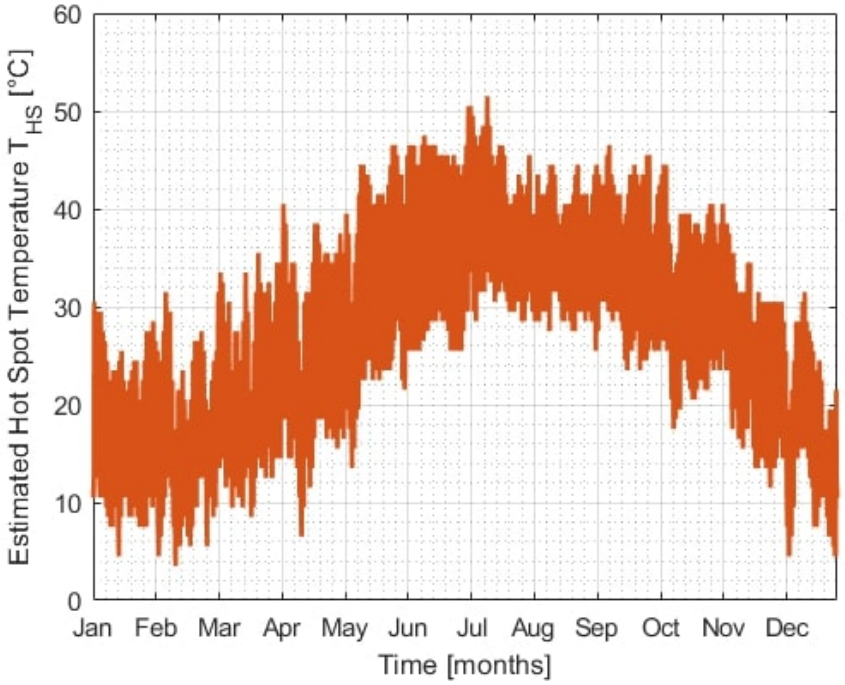


Figure 4.10: Estimated capacitor hot spot temperature T_{HS} based on mission profile in Phoenix, AZ.

condition. n is the voltage stress exponent and can be around 7 to 9.4 for MPPF Caps [84]. Table 4.4 summarizes the capacitor parameters used in this model.

In order to apply the Monte Carlo simulation, the maximum expected operating temperature is used as a static operating temperature derived based on the mission profile and the thermal model. Fig. 4.11 shows the result from the Monte Carlo simulation with 10,000 samples with variations of the operating voltage V_{dc} and temperature T. The subsequent Weibull distribution is given by the PDF. From these results, 100% of the capacitors will survive well past a 50-year lifetime.

4.3.3 Silicon Power Devices

For silicon power MOSFETS, junction temperature T_j and temperature swings ΔT_j are the two major stress factors that affect their reliability. The SEMIKRON model

$$N_f = A \cdot (\Delta T_j)^{\alpha} \cdot ar^{\beta_1 \cdot \Delta T_j + \beta_0} \cdot \left(\frac{C + t_{on}^{\gamma}}{C + 1}\right) \cdot \exp\left(\frac{E_a}{k_B \cdot T_{j,m}}\right) \cdot f_{diode} \tag{4.12}$$

introduced in [87] is used to estimate the number of cycles to failure (N_f) of the Silicon power MOSFET. $T_{j,m}$ is the absolute mean junction temperature, ΔT_j is the junction temperature swing, and t_{on} is the cycle period. The lifetime consumption (LC) of the device is calculated using Miner's rule

$$LC = \sum_i n_i/(N_f)_i \tag{4.13}$$

where n_i is the number of cycles per year. The device reaches end of life when LC is unity [124]. $T_{j,m}$ and ΔT_j are the equivalent static values derived based on the mission profile and the thermal model as

$$T_{j,m} = P_{loss} \cdot \left[R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}\right] + T_{a,m} \tag{4.14}$$

where P_{loss} is the device total expected power loss at 2 kW, which is mostly conduction loss. R_{th} is the thermal impedance from junction to case $(j-c)$, case to heatsink $(c-h)$ and heatsink to ambient $(h-a)$. Based on the Phoenix, AZ mission profile, the maximum expected ambient temperature $T_{a,max}$ is approximately 47 °C in the summer and a low of

Table 4.4: Parameters of the Film Capacitor Lifetime Model

Parameter	Label	Value
Rated Lifetime	L_0	100,000 hours
Rated Voltage	V_0	650 V
Rated Temperature	T_0	70 °C
Operating Voltage	V_{dc}	400 V
Max. Operating Temperature	T	60 °C

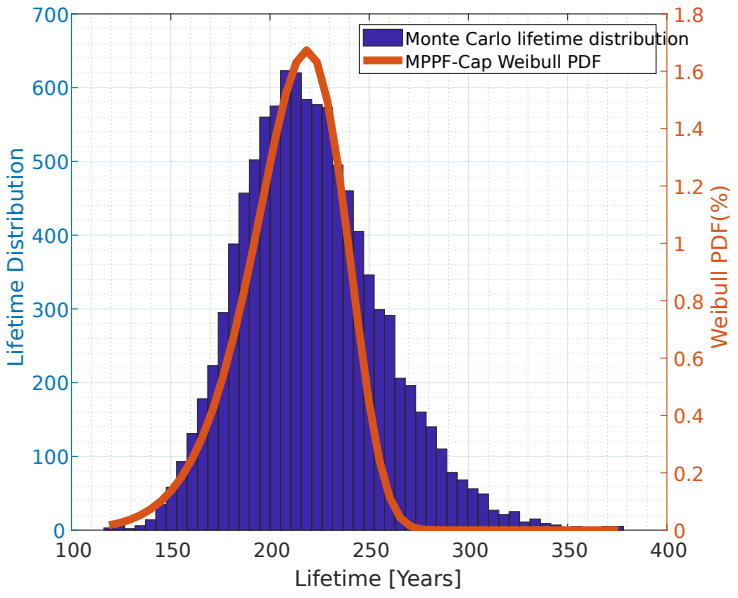


Figure 4.11: Lifetime distribution of MPPF-Cap using Monte Carlo simulation with 10,000 samples and Weibull PDF function .

-1 °C in the winter. However, the average ambient temperature is 22 °C. Table. 4.5 shows default model parameters used in the model and the values for the remaining parameters for the thermal model is depicted in Table. 4.6.

Fig. 4.12 shows an example of mean junction temperatures $T_{j,m}$ and cycle amplitudes ΔT_j of the CoolMOS device for 2 kW PV inverter in Arizona. From this result, a static mean junction temperature and amplitude cycle can be derived to estimate the lifetime of the device. Table 4.7 gives a summary of the static parameters used in the model. The result from the Monte Carlo simulation with 10,000 samples with variations in $T_{j,m}$ and ΔT_j is shown in Fig. 4.13 with the Weibull distribution. It shows that 100% of the MOSFET devices will survive well past 50 years in this inverter configuration.

4.3.4 GaN-GIT Power Devices

With the recent push for the wide adoption of SiC and GaN power devices, lifetime models for Silicon power devices have been used to estimate their reliability, often leading to erroneous estimation [89]. Having lifetime models based solely on wide bandgap power modules is essential to accelerate their worldwide acceptance. According to reliability analysis in [103], temperature, voltage, and current are the three stress factors that are essential in evaluating the switching lifetime of GaN FET. However, based on the switching lifetime evaluation for Hybrid Drain-embedded Gate Injection Transistor (HD-GIT) in [104] developed by Panasonic Corporation, the switching lifetime of their device depends strongly on the peak drain current I_{DP} and voltage V_{DD}. The HD-GIT switching lifetime (τ) is

$$\tau(V_{DD}, I_{DP}) = A \cdot \exp\left[-\left(\beta_v \cdot V_{DD} + \beta_c \cdot I_{DP}\right)\right] \tag{4.15}$$

where β_v is the voltage acceleration factor and β_c is the current accelerated factor. The acceleration factor test of the voltage V_{DD} and current I_{DP} on the lifetime yields $\beta_v = 0.039$ and $\beta_c = 0.47$. A is a constant factor approximately equal to $1e15$. During every switching action, V_{DD} and I_{DP} reduce the switching lifetime of the device by

$$\Delta\tau(V_{DD}, I_{DP}) = \frac{1}{\tau(V_{DD}, I_{DP}) \cdot f_{sw}} \tag{4.16}$$

Table 4.5: Parameters for MOSFET Lifetime Model [78]

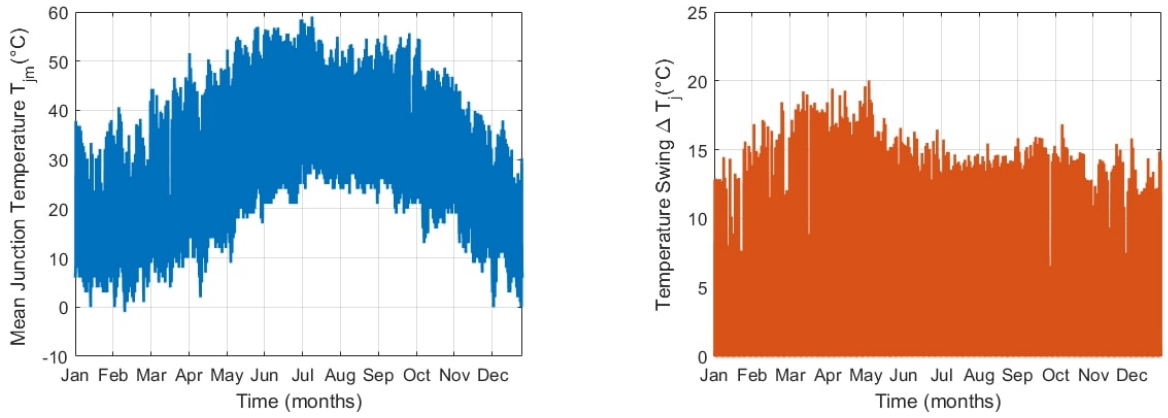
Parameter	Value	Experimental Condition
A	3.4368×10^{14}	
α	-4.923	$64\ \text{K} \leq \Delta T_j \leq 113\ \text{K}$
β_1	-9.012×10^{-3}	
β_0	1.942	$0.19 \leq ar \leq 0.42$
C	1.434	
γ	-1.208	$0.07\ s \leq t_{on} \leq 63\ s$
f_{diode}	0.6204	
E_a	0.06606 eV	$32.5°C \leq T_j \leq 122°C$
k_B	8.6173324×10^{-5} eV/K	

Table 4.6: Parameters of the MOSFET Thermal Model

Parameter	Label	Value
Expected RMS Current for 2 kW	(I_{rms})	18 A
Junction to Case thermal resistance	$(R_{th(j-c)})$	0.32 °C/W
Case to heatsink thermal resistance	$(R_{th(c-h)})$	0.4 °C/W
Heatsink to ambient thermal resistance	$(R_{th(h-a)})$	0.82 °C/W

Table 4.7: Static Parameters used for MOSFET Lifetime Model

Parameter	Label	Value
Mean ambient temperature	$T_{a,m}$	22 °C
Mean Junction temperature	$T_{j,m}$	32.92 °C
Temperature swing	ΔT_j	4 °C
Cycle period	t_{on}	0.083 s
Yearly cycles	n_i	1.89x10^9



(a) **(b)**

Figure 4.12: Expected (a) mean junction temperature $T_{j,m}$ and (b) cycle amplitude ΔT_j of the CoolMOS device under a mission profile in Phoenix, AZ .

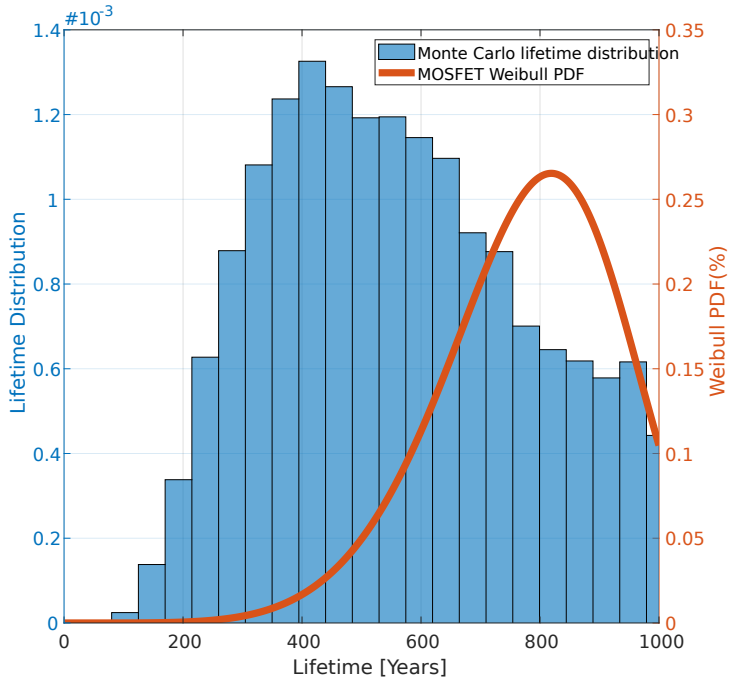


Figure 4.13: Lifetime distribution of MOSFET using Monte Carlo simulation with 10,000 samples and Weibull PDF function .

where f_{sw} is the switching frequency. Similar to the Silicon power device lifetime model, the GaN-GIT device reaches the end of its life when its switching stress $\Delta\tau$ accumulates to unity [104].

The Monte Carlo analysis for the GIT-GAN lifetime model uses 10,000 samples with variations in the stress factor V_{DD} and I_{DP}. The obtained results of the Monte Carlo simulation including the Weibull distribution are shown in Fig. 4.14. The GaN-GIT Weibull PDF shows that half of the GaN devices will fail within 30 years.

4.3.5 Component-Level Reliability

The unreliability evaluation result for each component in both DHA and Non-DHA modules is shown in Fig. 4.15. Their B_{10} lifetime percentage, which is defined as the lifetime when 10% of the population have failed, is summarized in Table 4.8. In both cases, the GaN-GIT device is the most unreliable component in the system. However, in the case of the DHA technique, there is less peak current stress on the GaN-GIT allowing for a higher lifetime in contrast to Non-DHA. The lifetimes of the MPPF-Cap in both schemes are nearly equal. Lastly, the MOSFET devices in the DHA module have such a significant lifetime of 600 years that it would not have much impact on the overall converter reliability at this power level. Its high reliability in this design is mainly due to the minimal junction temperature swings.

4.3.6 Converter-Level Reliability

From the unreliability function $F(x)$ of individual components, the unreliability of a single module is calculated before evaluating the lifetime of the entire system. Each DHA module is a half-bridge topology consisting of six power switches ($S_1, S_2, S_{apf}, S_{inv}$), an inductor ($L_1$) and a capacitor ($C_{apf}$). The Non-DHA module is the same with the exception of the switches S_{apf} and S_{inv}. All the components in the module are in a series configuration given that a failure of any one of them will cause the entire module to fail. Thus, the unreliability of a DHA single module $F_{mod,\mathrm{dha}}(x)$ is given by

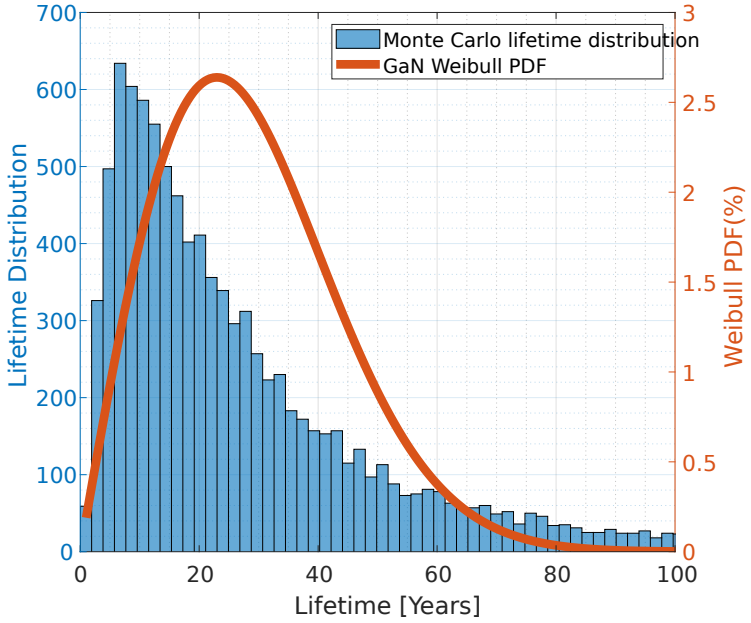


Figure 4.14: Lifetime distribution of GaN using Monte Carlo simulation with 10,000 samples and Weibull PDF function .

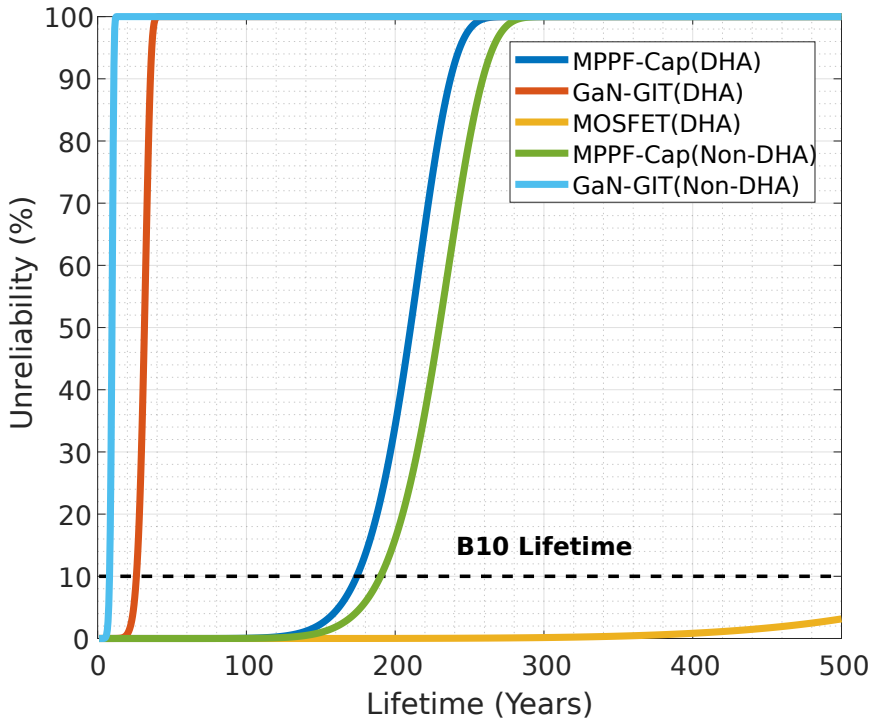


Figure 4.15: Unreliability function showing B_{10} lifetime of MPPF-Capacitor, MOSFET and GaN-GIT devices for both DHA and Non-DHA.

Table 4.8: Summary of B_{10} Lifetime Evaluation Results of Components for DHA and Non-DHA module

Components	DHA B_{10} Lifetime (Year)	Non-DHA B_{10} Lifetime (Year)
GaN-GIT	25	8
MPPF-Cap	172	190
MOSFET	600	-

$$F_{mod,\text{dha}}(x) = 1 - \Big[(1 - F_{gan}(x))^2 \cdot (1 - F_{dsph}(x))^4 \cdot (1 - F_{cap}(x))\Big] \tag{4.17}$$

where $F_{gan}(x)$ is the unreliability of the GaN-GIT power switches (S_1, S_2), $F_{dsph}(x)$ is the unreliability of the dispatch power switches (S_{apf}, S_{inv}) and $F_{cap}(x)$ is the unreliability of the APF capacitor. In the case of Non-DHA, its single module unreliability function $F_{mod,\text{nondha}}(x)$ is

$$F_{mod,\text{nondha}}(x) = 1 - \Big[(1 - F_{gan}(x))^2 \cdot (1 - F_{cap}(x))\Big] \tag{4.18}$$

The reliability models for single modules are used to generate the lifetime for the system. In this design, the failure of a single module due to internal component failure will not cause the entire system to cease operation. However, a minimum of two phases ($n = 2$) have to be operational in the case of DHA, with one phase dedicated to inverter operation while the other performs active power filtering. In the case of Non-DHA, one of each phase has to be operational at any given time. Thus, both DHA and Non-DHA power stage reliability is a parallel configuration system with identical element reliability $R_{HF}(x)$ that can be calculated using the simplest case of k out of n hot redundancy given by

$$R_{HF}(x) = \sum_{i=k}^{n} \binom{n}{i} R_{mod}(x)^i (1 - R_{mod}(x))^{n-1} \tag{4.19}$$

and

$$R_{mod}(x) = 1 - F_{mod}(x) \tag{4.20}$$

where k out of n available items are required for the system to properly operate [85]. In addition, there is a half-bridge module operating at line frequency (LF) used as the return phase leg. The LF module consists solely of two MOSFET power devices and can cause the entire system to fail if either of the devices fails. However, the probability of failure of a single MOSFET device is so low that it does not constitute a significant impact on the overall reliability of the system. The unreliability of the LF module is

$$F_{LF}(x) = (1 - F_{mos}(x))^2 \tag{4.21}$$

The total system unreliability function is

$$F_{sys}(x) = 1 - [R_{HF}(x) \cdot (1 - F_{LF}(x))] \,. \tag{4.22}$$

Fig. 4.16 shows the total estimated unreliability waveform of both the multiphase inverter architecture using DHA with 3 modules and Non-DHA with 4 and 6 modules. The obtained B_{10} lifetime and peak efficiency of both schemes are given in Table 4.9. Although both architectures achieve comparable efficiency performance, the DHA inverter yields a B_{10} lifetime of 26 years, which is more than three times that of the lifetime of a multiphase Non-DHA approach. To achieve comparable lifetime results to the DHA inverter, a Non-DHA system will require 6 modules with 3 phases each doing inverter and APF. When using the DHA technique, the reliability performance of the GaN-based inverter is greatly improved with fewer number of phases in comparison to the traditional multiphase approach.

4.4 Experimental Prototype

A low power and voltage experimental prototype of the proposed DHA inverter has been implemented to demonstrate the feasibility of the DHA concept. The prototype consists of 3 high-frequency modules ($n = 3$) with a single low-frequency return phase. The components and parameters used to implement each module is provided in Table 4.10. A picture of the hardware is given in Fig. 4.17. Each module is operated using BCM modulation with unipolar switching. The power stage of the high-frequency module uses 600V/70mΩ GaN-GIT devices from Panasonic while 650V/33mΩ CoolMOS devices from Infineon are used for the DHA switches (S_{apf}, S_{inv}). A XILINX Spartan 6 FPGA is used for digital logic and control. The experimental switching frequency ranges from 150 kHz to 800 kHz.

Fig. 4.18 and Fig. 4.19 show the operation of the inverter using DHA for 1.5 A RMS output current and 30 V RMS output voltage. The inductor current for all three modules ($I_{L1} - I_{L3}$) and AC output voltage V_{out} can be seen in Fig. 4.18. In this test, module 1 is

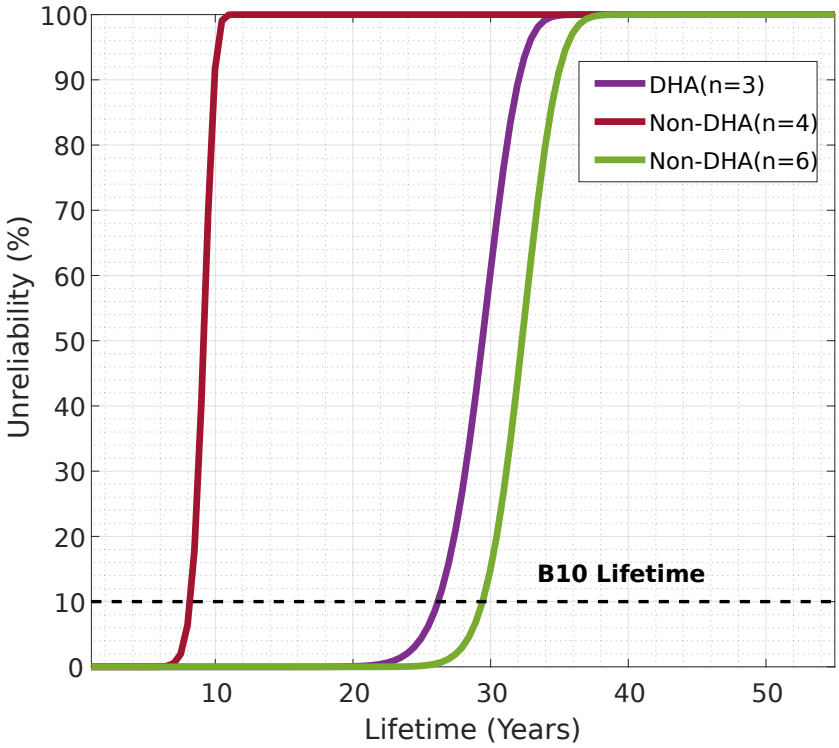


Figure 4.16: Unreliability function showing B_{10} lifetime of proposed 3 modules DHA (n=3), 4 modules non-DHA (n=4), and 6 modules non-DHA showing (n=6).

Table 4.9: Summary of B_{10} Lifetime Evaluation Results of DHA and Non-DHA

Parameter	Units	DHA	Non-DHA	Non-DHA
Allocation Type		Dynamic	Static	Static
Number of Modules (n)		3	4	6
B_{10} Lifetime (B_{10})	Years	26	8	29
Peak Efficiency (η)	%	96.10	96.48	96.51

Table 4.10: Components and Parameters of prototype

Parameter	Value
Input voltage V_{dc}	80 V
Output voltage V_{out}	30 V/60 Hz
GaN Device	600V/70mΩ-GaN-GIT
MOSFET Device	650V/33mΩ-CoolMOS
MPPF APF Capacitor	3x30 µF (MKP1847630354Y5)
Inductor L_1, L_2, L_3	20 µH
Shunt Resistor R_{shunt}	20 mΩ
Inductor Core Geometry	Planar EI38
Inductor Core Material	Ferroxcube 3F36
Switching Frequency	120 kHz - 750 kHz

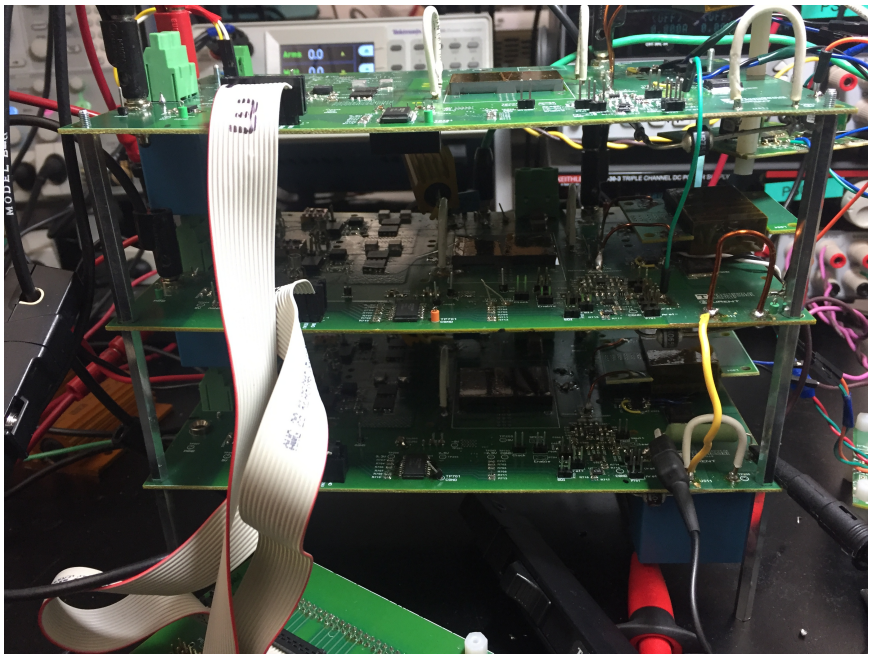


Figure 4.17: DHA experimental prototype board.

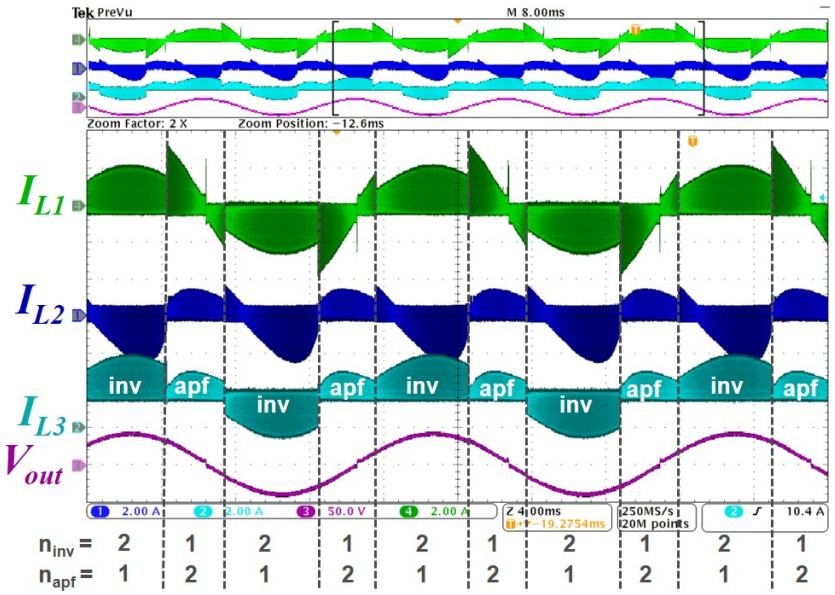


Figure 4.18: Prototype experimental waveform of DHA inverter showing module 1, 2 and 3 inductor current ($I_{L1} - I_{L3}$), and AC output voltage V_{out}.

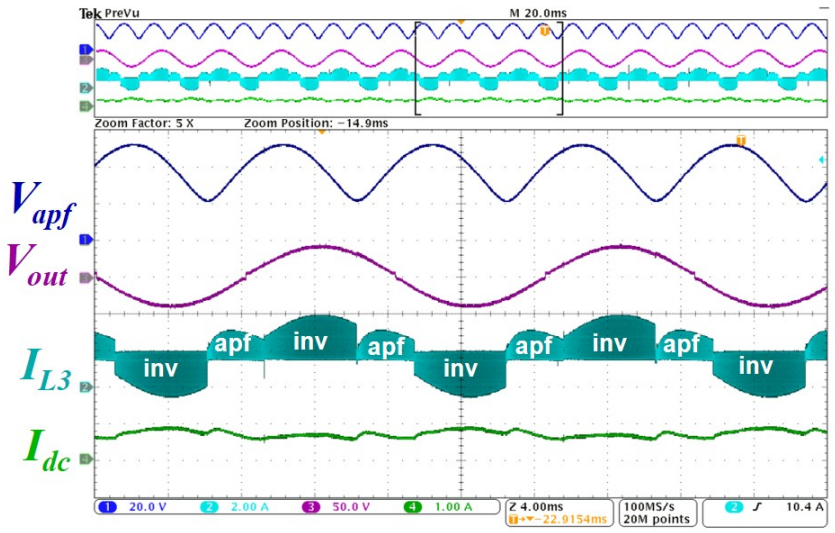


Figure 4.19: Prototype experimental waveform of DHA inverter showing APF capacitor voltage V_{apf}, AC output voltage V_{out}, module 3 inductor current I_{L3} and DC-link current I_{dc}.

allocated for inverter operation, module 2 for APF, and module 3 switches operation between inverter and APF operation. The figure also illustrates the number of modules allocated for each operation (n_{inv} and n_{apf}) during the entire line cycle. The peak inverter and APF current are well-regulated to 4 A and 2.5 A respectively. Fig. 4.19 gives the measured APF capacitor voltage V_{apf} and the DC-link current I_{dc}. It can be seen that the APF successfully filters the second harmonic ripple power, and the DC-link current does not exhibit much fluctuation.

4.5 Summary

The design for reliability analysis of a GaN-based single-phase inverter using DHA has been carried out and compared with a multiphase inverter with the static allocation (Non-DHA). The GaN device was determined to be the limiting component in the system. However, with the DHA inverter approach, the system achieves a much longer lifetime of approximately 26 years, outperforming the lifetime of a multiphase Non-DHA system with comparable efficiency metrics. In addition, this reliability assessment shows that it is essential to integrate design for reliability analysis during the converter design stage instead of designing for just high efficiency. A low voltage and current experimental prototype has been built and tested to validate the feasibility of the DHA concept.

Chapter 5

High Frequency Dual Current Program Mode Control

The advancements in wide bandgap (WBG) power devices such as gallium nitride (GaN) and silicon carbide (SiC) transistors have introduced new opportunities and challenges in high-frequency power electronics. Their device properties allow converters to operate at high switching frequency with minimal switching losses in comparison to silicon devices [125]. Despite their advantageous characteristics, operating any converters at high switching frequency results in increased switching losses and more severe electromagnetic interference (EMI) [126, 65]. As a result, control-based modulation techniques such as Boundary Current Mode (BCM) modulation are used in inverters and rectifiers to achieve zero voltage switching (ZVS) and overcome the increased switching losses at high-frequency [65, 127, 128, 129, 130, 131, 132]. To implement BCM modulation, a model-based control or direct inductor current control using, e.g., dual current programmed mode (DCPM) control is used. One traditional implementation of the DCPM is shown in Fig. 5.1 where a current-sensing resistor, differential amplifier, comparators, flipflop, and a DSP are used.

The analog and digital circuitry regulate the inductor current within a line-frequency envelope set by a controller through inductor current references [133]. Although the differential amplifier in the loop contains a low-pass filter characteristic that attenuates the high-frequency noise, the current control network is still prone to anomalous switching actions when subject to high dv/dt switching, as will be present in a GaN-based implementation

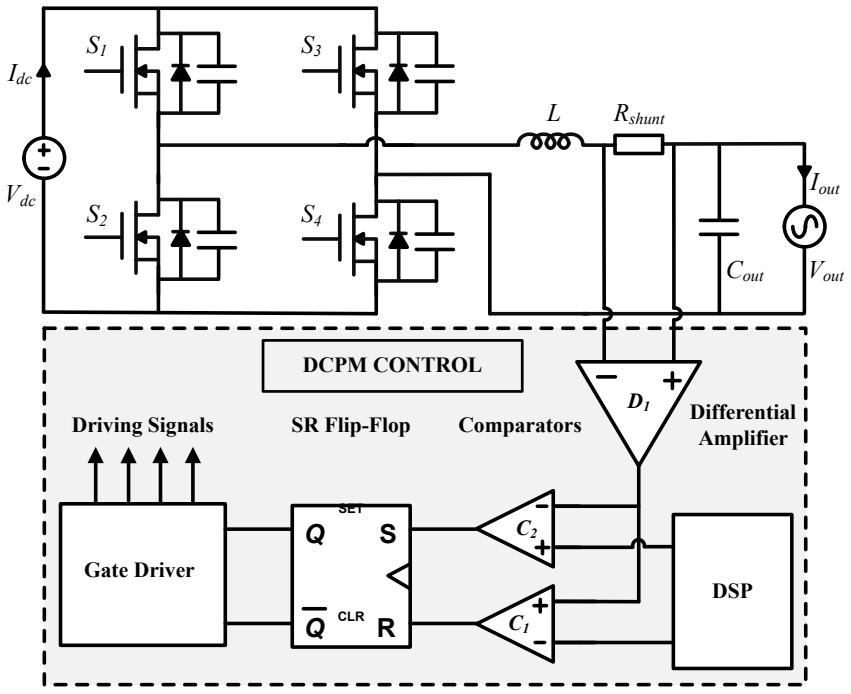


Figure 5.1: Full bridge inverter topology with traditional DCPM control.

[134]. In [135], several control techniques have been proposed to mitigate this issue; however, these control schemes are complicated for practical implementation. In addition to noise issues, propagation delays inherently introduced by components in the current loop cause the inductor current to overshoot its reference point. This results in extra unnecessary peak inductor current and changes of the switching frequency [136]. To overcome both the issue of noise and propagation delay in BCM, a simple and low-cost solution is proposed in this dissertation. The description of the proposed current mode control circuit, the characterization of propagation delay, and current compensation implementation followed by experimental results are outlined next.

5.1 Noise Mitigation in High-Frequency Dual Current Programmed Mode Control

The traditional DCPM implementation is illustrated in Fig. 5.2. It relies on instantaneous comparison between the sensed inductor current V_{sens} and two low-frequency references, $V_{ref,+}$ and $V_{ref,-}$. While this allows wide-bandwidth, cycle-by-cycle current regulation, it also results in high susceptibility to noise. Any oscillation in the sensed inductor current at or near the switching time will result in anomalous level transitions at the outputs of comparators C_1 and C_2 as depicted in Fig. 5.3. Due to parasitics in the sensing circuitry and nonidealities of the analog elements, such oscillations are observed following power stage switching. In addition, the fast dv/dt and di/dt switching transitions of GaN transistors, coupled with the presence of parasitic inductance and capacitance in the circuit, introduce noise into the DCPM control loop at high frequency.

5.1.1 Principle of Operation

In order to mitigate the impact of switching noise, a modified DCPM using blanking times following each switching action has been introduced in [108]. Fig. 5.4 diagrams show an improved DCPM control loop that uses a combination of Oneshots and AND gates to create a controllable blanking time following each switching action to reject ensuing noise. Fig. 5.4

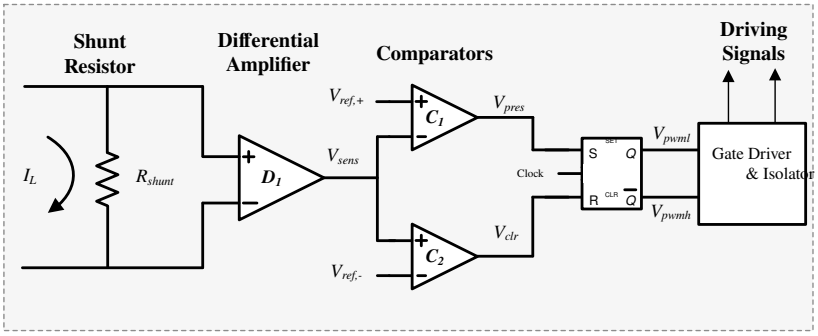


Figure 5.2: Traditional dual current programmed mode control loop network.

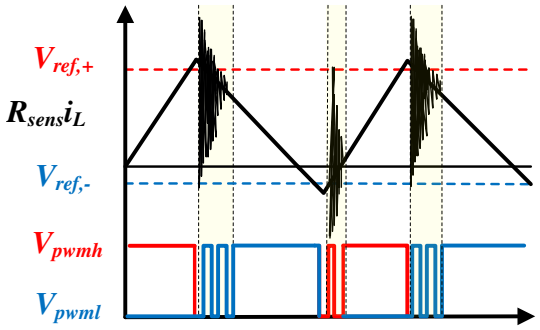


Figure 5.3: Waveform demonstrating the anomalous transition.

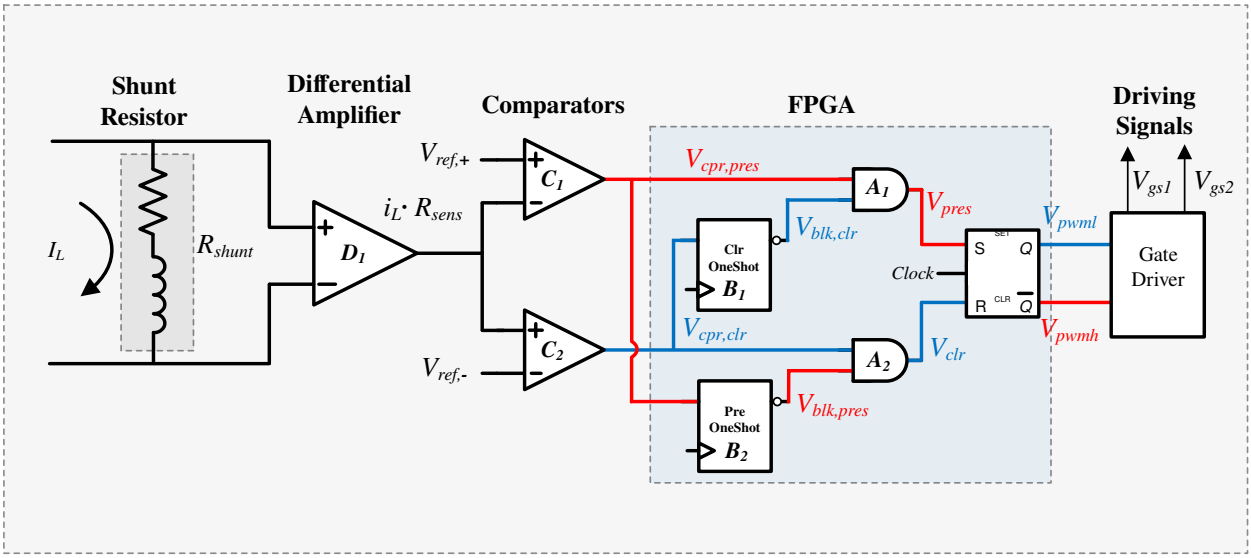


Figure 5.4: Proposed dual current programmed mode control loop network.

shows the diagram of the proposed improved DCPM control loop with additional switching noise immunity. One-shots B_1 and B_2 and AND gates A_1 and A_2 have been added to the traditional design of Fig. 5.2. These elements are used to create a controllable blanking time T_{blk} following each switching action to reject ensuing noise. The blanking time can be set such that T_{blk}, during which switching is prevented, is below the minimum required T_{on} or T_{off} during operation.

Ideal operation waveforms of the circuit in a half-bridge are outlined in Fig. 5.5. For simplicity, the synchronization of the waveforms with the clock has been omitted. The effective transimpedance of the current sensing resistor and amplifier is

$$R_{sens} = \frac{V_{sens}}{i_L} = R_{shunt} \cdot H \tag{5.1}$$

where H is the voltage gain of D_1. Relative to the BCM reference in Fig. 6.1, the current limits $i_{ref,\pm} \cdot R_{sens} = V_{ref,\pm}$. During the turn-on transition of S_2, the following events happen in sequence. Prior to the beginning of the transition, both one-shot B_1 and B_2 outputs are high. First, the sensed inductor current V_{sens} reaches the high reference $V_{ref,+}$; then, the comparator C_1 is triggered, causing its output $V_{cpr,pres}$ to change state from low to high. Second, the logic change of the comparator triggers two simultaneous events: (1) the output of the AND gate A_1 goes high tracking $V_{cpr,pres}$ and (2) the output of B_2 one-shot, $V_{blk,pres}$ is driven low. The output of B_2 remains low for the duration of T_{blk}, during which A_2 prevents high-frequency switching noise from resetting the latch and causing an undesirable turn-off of S_2. Third, after T_{blk}, the output of B_2 goes back to high, and the next switching action is ready to occur. In the next switching action, S_1 turns on, S_2 turns off and the entire process is repeated. For proper operation of the logic circuit, T_{blk} should be set based on the highest expected switching frequency and should not exceed the lowest allowed switching interval, $T_{blk} \leq \min(T_{on}, T_{off})$. Though this implementation significantly improves switching noise immunity, it still requires that any parasitic ringing which couples into the sensing circuitry following a switching action is damped out prior to T_{blk}. If not achieved inherently, this constraint can be met by reducing sensing and power stage parasitics, adding additional

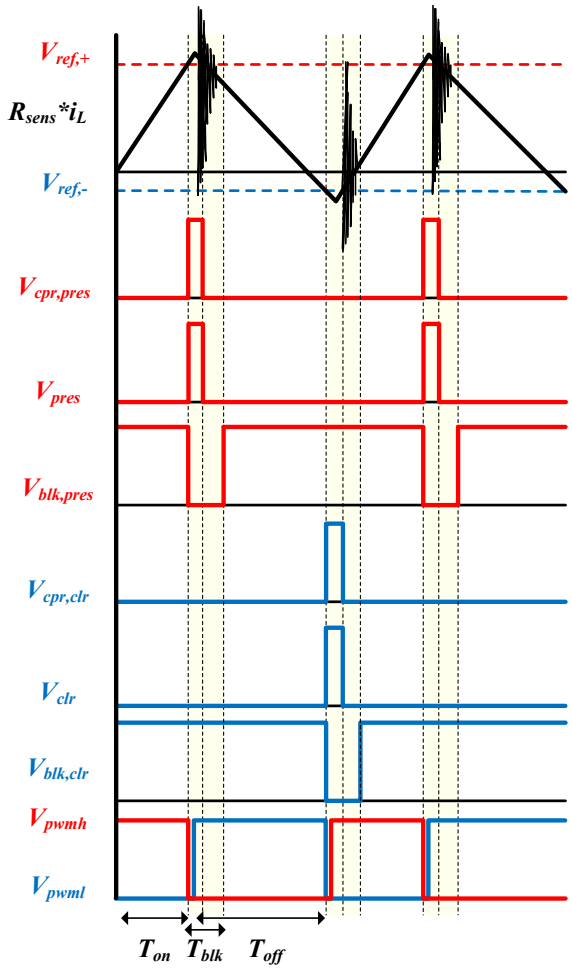


Figure 5.5: Ideal waveform of proposed current control loop.

filtering, or increasing T_{blk}. The latter may require reducing the power stage maximum switching frequency.

5.1.2 Experimental Results

In order to validate the proposed solutions, a 500 W prototype experimental half bridge is constructed with the proposed DCPM control implementation of Fig. 5.4. Details of the converter power stage are given in Table 5.1, and components used in the control circuitry are given in Table 5.2. A photograph of the experimental prototype is shown in Fig. 5.6. The power stage is implemented using a GaN-GIT power device from Panasonic Corporation and the digital logic circuitry of the DCPM loop and the reference generation and compensation are implemented in a XILINX Spartan 6 FPGA.

The converter is operated in BCM operation as illustrated resulting in a varying switching frequency ranging from 300 kHz to 800 kHz. The upper and lower boundaries of the inductor current are set using an FPGA to generate the subsequent voltage references. Fig. 5.7a shows the inductor current I_L, the sensed inductor current $V_{sens} = R_{sens} \cdot i_L$, and gate drive signals V_{pwmh}, V_{pwml} when using the traditional current mode control and the proposed current mode control with noise immunity. With the traditional approach, the effect of the noise during the inductor zero-current crossing is seen on the gate drive signals causing the active switch S_1 to exhibit anomalous switching actions. In Fig. 5.7b, the undesirable switching of S_1 is eliminated by using the proposed current loop with a blanking time of 290 ns. Both gate drive signals show no uncontrolled switching actions while operating at 800 kHz maximum switching frequency and 3.5 A peak inductor current.

An improved simple and low-cost noise immunity model to address noise challenges prevalent in BCM control has been proposed. A combination of one-shot and AND gates are used to implement a blanking time that prevents the noise during the inductor zero current transition to interfere with the operation of the active switch.

Table 5.1: Experimental Prototype Converter Design

Parameter	Value
S_1, S_2	Panasonic GaN-GIT
L	26 µH
R_{shunt}	20 mΩ
Inductor Core Geometry	Toroid
Inductor Core Material	Mix No. 2 (Micrometal)
V_{dc}	400 V
P_{out}	500 W
f_{max}	800 kHz

Table 5.2: Experimental Prototype Control Circuit Components

Component	Part No.
Gate Driver	UCC21520
OpAmp	THS4509
Comparator	LTC6752-4
FPGA	XILINX Spartan 6

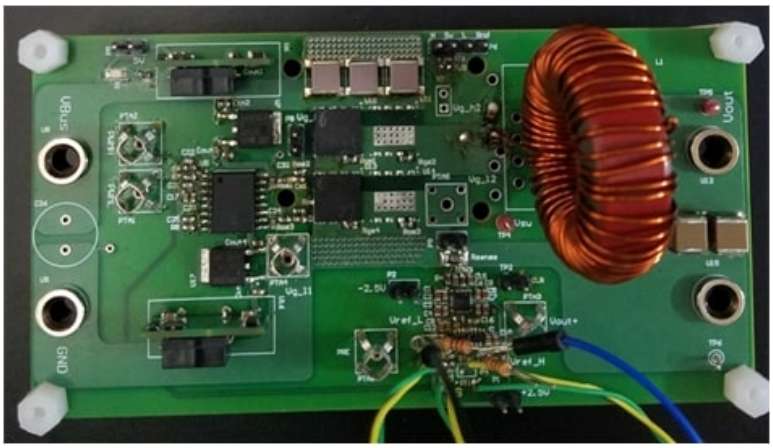
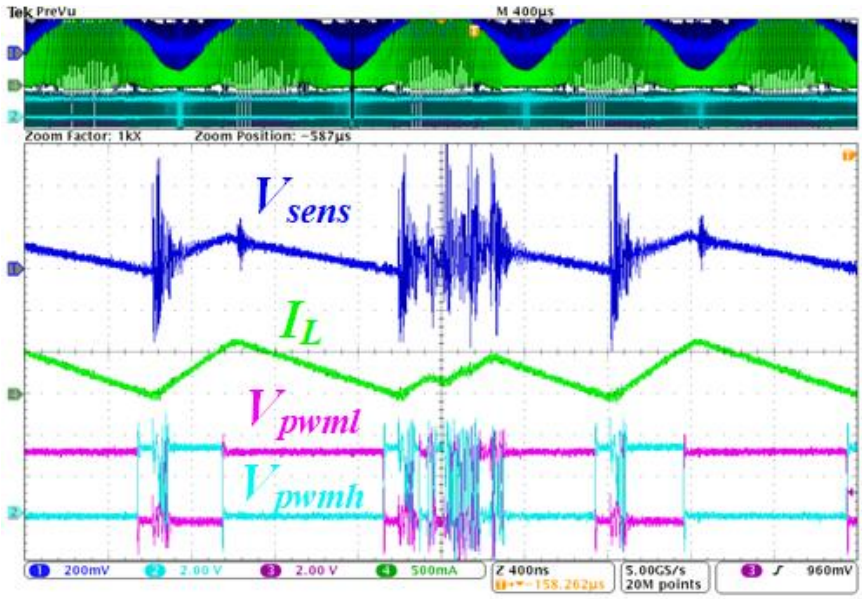
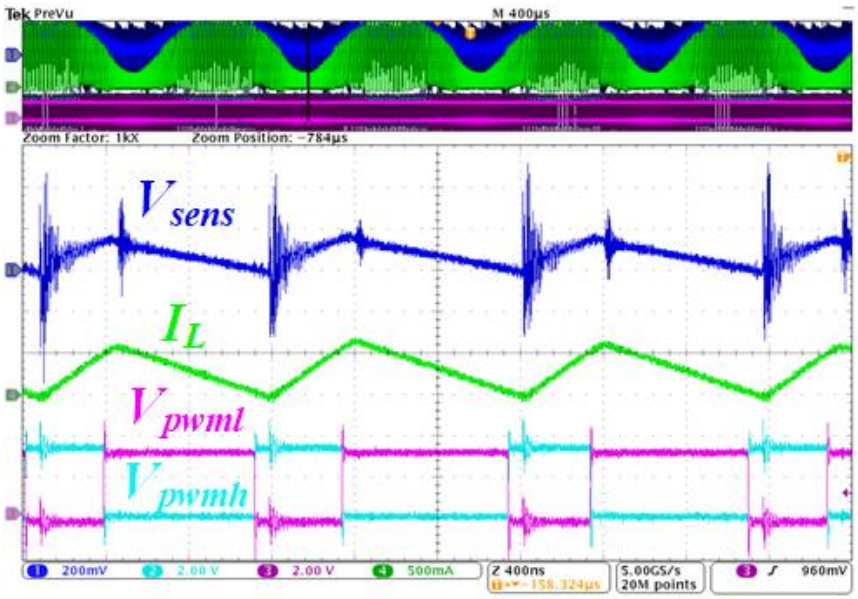


Figure 5.6: Experimental prototype board.



(a)



(b)

Figure 5.7: Experimental result using (a) Traditional DCPM without blanking time and (b) proposed DCPM with blanking time.

5.2 Delay Mitigation in High-Frequency Dual Current Programmed Mode Control

The improved DCPM control significantly enhances switching noise immunity at high frequency; however, the added components introduced in the control network contribute additional propagation delay in the control. The introduced delay in the current control circuit presents challenges in BCM modulation. The current controller cannot immediately react when the current crosses the high and low references. This can cause the inductor current to overshoot past its reference point and quickly increase when its current slope is large, changing the switching frequency [65]. This delay can be compensated using a model-based offset to the current references which varies with operating point [136, 137], but this approach requires additional controller complexity comparable to indirect control methods such as [128]. To address the issue of propagation delay without an increase in controller complexity, a design approach for a resistive current sensing circuit is proposed. In the approach, the opposing distortions caused by sensing delay and parasitic inductance are tuned such that the two effects are equal, nullifying their impact on current regulation. The modeling, design and implementation of the proposed delay mitigation technique are outlined next.

5.2.1 Modeling and Design of Delay Compensation

In the proposed DCPM control implementation of Fig 5.4, the inductor upper and lower limits $(i_{L,+}, i_{L,-})$ are set respectively by the positive and negative comparator reference voltages $(V_{ref,+}, V_{ref,-})$. Assuming an ideal sensing resistor ($L_{par} = 0$) and zero delays between the shunt resistor current and the resulting switching action, the relationship between the inductor current and voltage reference at the switching instant for the inductor positive reference is

$$i_{L,+} = \frac{V_{ref,+}}{R_{shunt} \cdot H} \tag{5.2}$$

where H is the voltage gain of the differential amplifier D_1. In any practical implementation of DCPM control, both the parasitic inductance L_{par} and the time delay of the sensing circuit will take non non-zero value. In general, both quantities are parasitic and component selection and layout should take care to minimize their impact. However, particularly in high switching frequency designs and in designs where small R_{shunt} is employed to minimize power loss, the inductance and delay may present significant distortion of current regulation.

Fig. 5.8 shows the effect of propagation delay on the inductor current during its positive slope. The propagation delay consists of the time delay of the comparator, logic gates, isolator and gate driver. At point 1 in Fig. 5.8, the inductor current reaches its ideal reference, and therefore $V_{sens}(t) = V_{ref,+}$ and the sensing circuit begins to initiate a switching action that will result in S_1 turn-off and S_3 turn-on. However, because of the propagation delay in the control loop, the switching action is delayed by t_{delay}. As the signal propagates during this delay, the inductor current overshoots by

$$\Delta i_{L,+} = \frac{\Delta V_{ref,+}}{R_{shunt} \cdot H} = t_{delay} \left(\frac{di_L}{dt} \right) \tag{5.3}$$

As a result of the delay, the actual switching transition occurs at point 2. At high switching frequency, and at operating points where the inductor current slope di_L/dt is high, even modest time delays may cause the inductor current to overshoot by several amps. In [136], a constant offset has been used in the reference signal to compensate for the extra inductor current, but the dynamic variation of di_L/dt in BCM operation results in a compensation magnitude that varies with the operating point.

When considering the effect of propagation delay, actual inductor current at the switching time becomes

$$i_{L,+} = \frac{V_{ref,+}}{R_{shunt} \cdot H} + t_{delay} \left(\frac{di_L}{dt} \right) \tag{5.4}$$

where the first term is the ideal value, as in (5.2) and the second term is the inductor current error resulting from t_{delay}.

In contrast to the impact of sensing delay, Fig. 5.9 shows the effect of parasitic inductance on the inductor current during its positive slope. In a real implementation, the sense resistor will exhibit some parasitic inductance, L_{par}, which causes a small distortion of the sensed

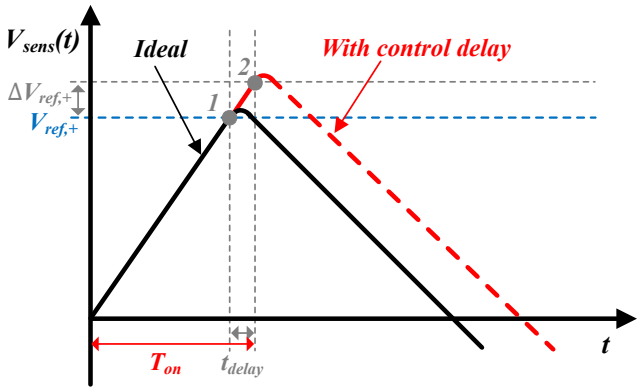


Figure 5.8: Ideal waveform of sensed inductor current V_{sens} showing the effect of propagation delay during ON time T_{on}.

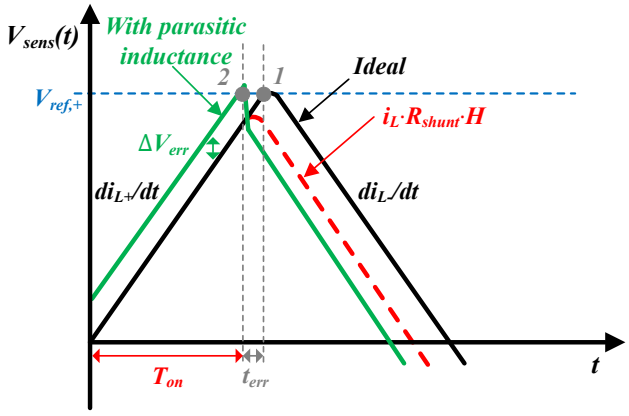


Figure 5.9: Ideal waveform of sensed inductor current V_{sens} showing the effect of parasitic inductance during ON time T_{on}.

voltage. The package of a typical SMD shunt resistor and the connection of the sensed wires or PCB traces determine the parasitic inductance [138]. Point 1 in Fig. 5.9 is the ideal peak reference point that should initiate S_1 turn-off and S_3 turn-on transition. Because the inductor current slope is nearly constant during T_{on}, the presence of L_{par} introduces a fixed offset voltage

$$\Delta V_{err} = L_{par}\left(\frac{di_L}{dt}\right)H \tag{5.5}$$

In contrast to the effect of propagation delay, the parasitic inductance results in $V_{sens}(t)$ reaching its positive reference ($V_{ref,+}$) early. The switching transition now occurs at point 2, reducing the total on-time by t_{err}. As a result, the actual inductor current at the switching time, considering the impact of L_{par}, is

$$i_{L,+} = \frac{V_{ref,+}}{R_{shunt}\cdot H} - \frac{L_{par}}{R_{shunt}}\left(\frac{di_L}{dt}\right) \tag{5.6}$$

The inductor current falls short of its reference and becomes distorted.

From (5.4) the propagation delay t_{delay} causes an overshoot of the inductor current, while the parasitic inductance L_{par} causes a lower inductor current as shown in (5.6). Thus, when considering both the effect of propagation delay and parasitic inductance, the resulting inductor current is

$$i_{L,+} = \frac{V_{ref,+}}{R_{shunt}\cdot H} + \left(t_{delay} - \frac{L_{par}}{R_{shunt}}\right)\left(\frac{di_L}{dt}\right) \tag{5.7}$$

and the average output current when using bipolar switching is

$$\frac{i_{L,+} + i_{L,-}}{2} = \frac{V_{ref,+} + V_{ref,-}}{2R_{shunt}\cdot H} - \frac{2V_{out}}{L}\left(t_{delay} - \frac{L_{par}}{R_{shunt}}\right) \tag{5.8}$$

The effect of parasitic inductance of the shunt resistor counteracts the effect of time delay in the control loop. Thus, by designing the shunt resistance R_{shunt}, the propagation delay t_{delay} and the parasitic inductance L_{par} to satisfy

$$R_{shunt}\cdot t_{delay} \approx L_{par} \tag{5.9}$$

the dependence on the operating point is nullified and the inductor current returns to the ideal expression in (5.2). As a result, current control is nearly ideal and is independent of the varying di_L/dt present in BCM modulation. To achieve this goal, careful design consideration needs to be given to the choice of R_{shunt}, t_{delay} and L_{par}.

5.2.2 Implementation of Delay Compensation

The underlying implementation principle of this proposed delay compensation technique is that the sensing circuit is designed such that the compensation condition given by $(t_{delay} - L_{par}/R_{shunt}) \approx 0$. In the ideal case, this is accomplished by making both t_{delay} and L_{par} zero.

Practically, for a given converter implementation, t_{delay} can be increased through digital control delay, but cannot be decreased below $t_{delay,min}$, the base delay contributed by the components in the control loop and gate driver. Conversely, increasing t_{delay} will reduce the maximum achievable switching frequency

$$f_{s,max} < \frac{1}{2t_{delay}} \tag{5.10}$$

and lower values of $f_{s,max}$ will occur at duty cycles other than 50%.

Similarly, L_{par} may be altered by the selection of the sensing resistor form factor and through modifying the sensing connections, but is practically bounded by the package inductance of the resistor component on the low end. On the high end, too large of an L_{par} will increase the minimum achievable inductor current ripple; due to the offset in (5.5), considering both switching actions, regulation can only be maintained if

$$V_{ref,+} - V_{ref,-} > L_{par} H \left(\frac{di_L{}^+}{dt} - \frac{di_L{}^-}{dt} \right) \tag{5.11}$$

Additionally, large L_{par} may cause additional ringing and distortion.

The value selected for R_{sens}, the product of R_{shunt} and the amplifier voltage gain H is constrained by limits on conduction loss on the high-end. The minimum value for R_{sens} is dictated by limitations on signal integrity, including amplifier offset voltage and SNR.

Thus, as in traditional design, every effort should be made to minimize t_{delay} and L_{par} in the initial design. Then, based on the results achieved, minor modifications to R_{shunt}, t_{delay} and/or L_{par} are made to satisfy (5.9).

First case: $R_{shunt} \cdot t_{delay,min} < L_{par}$

In this situation, given the choice of R_{shunt} and the measured minimum delay $t_{delay,min}$ in the control, the measured parasitic inductance L_{par} is still larger than the product of the other two parameters. Thus, the compensation condition is $(t_{delay} - L_{par}/R_{shunt}) < 0$. From (5.8), this condition increases the RMS output current in bipolar switching BCM modulation. To meet the design target, additional digital delay can be programmed into the control; the shunt resistor can be increased, or the parasitic inductance can be reduced. The use of a shunt resistor for current sensing exhibits an i^2R type power loss. As a result, increasing the shunt resistance value would lead to increased conduction losses negatively impacting efficiency. The input/output voltage rating of the differential amplifier also constrains the shunt resistance. Thus, it is preferable to reduce the parasitic inductance L_{par} or program additional delay t_{delay} in this case. The parasitic inductance can be reduced by placing multiple, higher-value shunt resistors with the same package in parallel. In the case where the parasitic inductance cannot be reduced, additional delay can be digitally programmed into the control offsetting the effect of parasitic inductance. Although the propagation delay would increase in this scenario, it does not result in an overshoot of the inductor current and an altering of the on-time t_{on} because the effect of the extra delay is canceled out by the parasitic inductance. Although both options would satisfy the design objective, the former would yield a net positive effect by further reducing the parasitic inductance in the control loop while also keeping the converter loss the same.

Second case: $R_{shunt} \cdot t_{delay,min} > L_{par,max}$

This case is often given by the minimal expected delay $t_{delay,min}$ being too high resulting in a compensation condition greater than zero $(t_{delay} - L_{par}/R_{shunt}) > 0$. Besides causing an increase in the peak and RMS inductor current, it also leads to a drop in the output current as illustrated in (5.8) when using bipolar switching in BCM modulation. To mitigate this

issue, R_{shunt} and L_{par} are manipulated instead since the delay cannot be further decreased. The shunt resistance can be decreased or the parasitic inductance can be increased to meet the design target. Increasing the parasitic inductance can be achieved by having multiple small-valued shunt resistances in series or slightly altering the connection of the sensing wires to the shunt resistance (i.e. moving away from a Kelvin connection). Tuning the parasitic inductance to cancel the effect of propagation delay affects the noise immunity of the control. A large L_{par} decreases the measurement bandwidth, which is undesirable for high-frequency operation. In addition, it may exacerbate the ringing following every switching action when subject to high dv/dt and di/dt. The use of the improved DCPM controller previously outlined in Fig. 5.4 is essential to the operation of this control and addresses this issue by adjusting the blanking time following each switching action to reject ensuing noise [108]. Despite these design efforts, a minimal L_{par} is always desirable to minimize ringing in the control.

In each case, the approach to compensation has additional implications on converter losses, noise immunity, or minimum achievable on time. Propagation delays and parasitic inductance are both parameters that negatively affect the controller operation at high frequency. Therefore, circuit design best practices should still be followed to keep both to a minimum while the choice of shunt resistance should satisfy design power and efficiency requirements.

5.2.3 Experimental Results

Fig. 5.10 shows an experimental prototype of the full bridge inverter using the improved DCPM controller with the proposed propagation delay mitigation technique successfully implemented and tested up to a maximum switching frequency of 750 KHz. The main design parameters are listed in Table 5.3. The power stage has been implemented using GaN-GIT devices from Panasonic Corporation and a XILINX Spartan 6 FPGA for the digital logic and control. The major components used in the power stage are summarized in Table 5.4.

To demonstrate the operation of the proposed delay compensation technique, a fixed upper and lower reference are used for DC-DC operation. The measured total propagation delay of the network including the gate driver is approximately 63 ns over the range

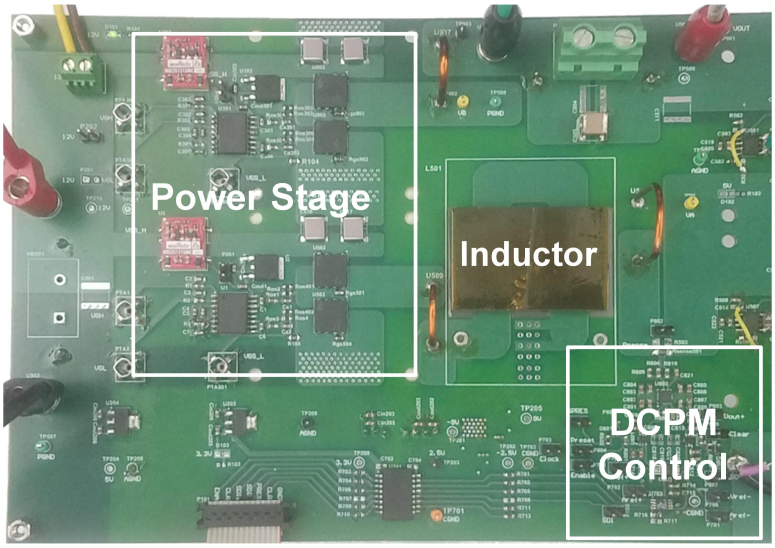


Figure 5.10: Experimental prototype board.

Table 5.3: Parameters of prototype

Parameter	Value
Input voltage V_{dc}	250V
Output voltage V_{out}	120V/60Hz
Device	Panasonic GaN-GIT
Inductor L_1, L_2	20 µH
Shunt Resistor R_{shunt}	20 mΩ
Inductor Core Geometry	Planar EI38
Inductor Core Material	Ferroxcube 3F4
Switching Frequency	120 kHz - 750 kHz

Table 5.4: Components of the experimental prototype

Component	Part No.
Gate Driver	UCC21520
Differential Op-Amp	THS4509
Comparator	LTC6752-4
Op-Amp	LMV722
DAC	LTC2602
Digital Isolator	ADuM262N
FPGA	XILINX Spartan 6

of measured di_L/dt. The parasitic inductance of the shunt resistor is estimated using experimental results illustrated in Fig. 5.11 showing the measured inductor current I_L, the sensed inductor current V_{sens}, and the switch node voltage V_{sw}. During T_{on} and T_{off}, the parasitic inductance of the shunt resistor results in a voltage offset ΔV_e. The estimated parasitic inductance L_{par} is approximately 1.2 nH in the prototype converter.

The effect of propagation delay and parasitic inductance are shown experimentally in Fig. 5.12. In this design, the control circuit includes a digital isolator which accounts for up to 13 ns of delay. The logic network and comparator add a total of 23 ns of delay and the gate driver accounts for 27 ns of delay. When only considering the effect of propagation delay, the compensation voltage $\Delta V_{ref,+}$ needs to be decreased with di_L/dt. On the other hand, when considering only the effect of parasitic inductance, resulting compensation voltage needs to be increased to meet the desired target. When both effects are considered as in (5.7), $\Delta V_{ref,+}$ is nearly zero and does not vary much with increased inductor slope.

Fig. 5.13 shows the experimental, analytical and ideal results of the inductor current compensation using the proposed delay mitigation technique with a fixed reference. With a minimum measured propagation delay of 63 ns, a 20 mΩ shunt resistor with a parasitic inductance of 1.20 nH is used to satisfy (5.9). As expected, the measured inductor current is regulated to the reference and is nearly independent of di_L/dt. Similar results are observed for the inductor negative reference.

Once the model has been validated using a set of fixed references, and the parameter values have been determined, the converter is operated in BCM mode. The upper and lower reference voltages ($V_{ref,+}, V_{ref,-}$) are implemented digitally in the FPGA and converted to an analog signal using a DAC. The negative reference is generated using an inverting op-amp, which contributes a constant offset voltage. This offset is canceled out by adjusting the programmed reference value ($V_{ref,-}$). The generated reference voltage using the delay mitigation technique for a peak inductor current of 5 A and a fixed reversed ZVS current of 1.50 A is shown in Fig. 5.14. To ensure ZVS through the entire line cycle, a fixed deadtime of 100 ns has been used. ZVS is achieved throughout all operating points, and the inverter switching frequency varies from 120 kHz to 750 kHz.

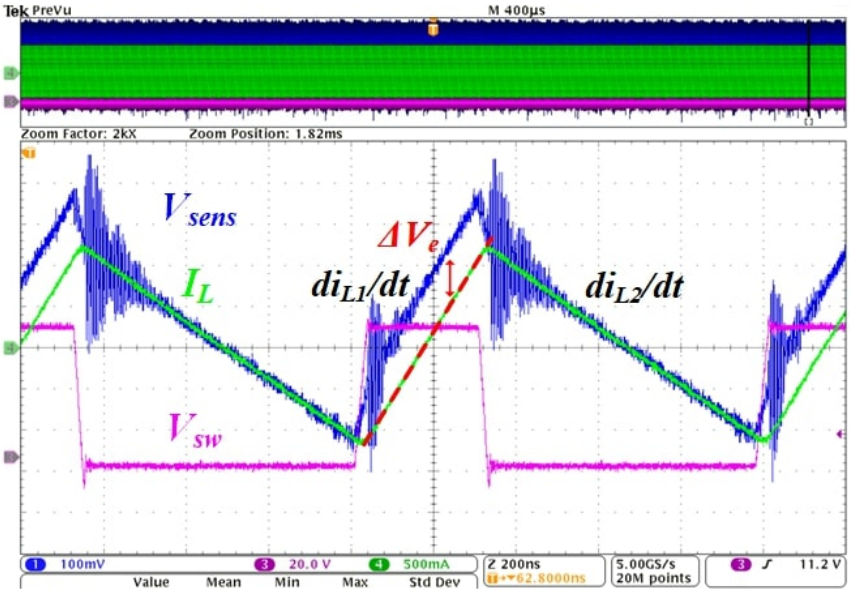


Figure 5.11: Experimental result showing the effect of parasitic inductance on the sensed inductor current.

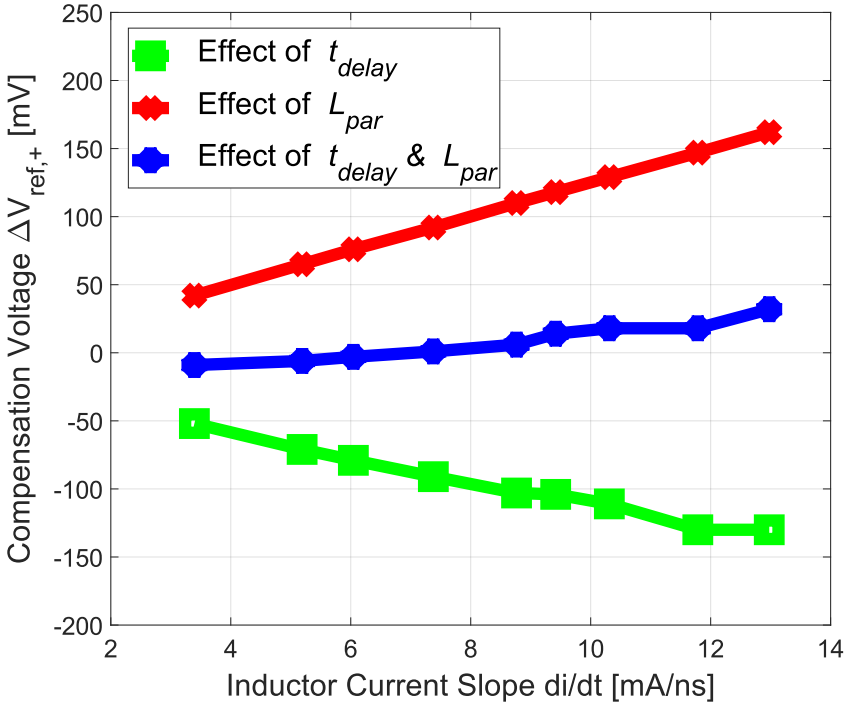


Figure 5.12: Estimated compensation reference voltage $\Delta V_{ref,+}$ showing the effect of propagation delay t_{delay} and parasitic inductance L_{par}.

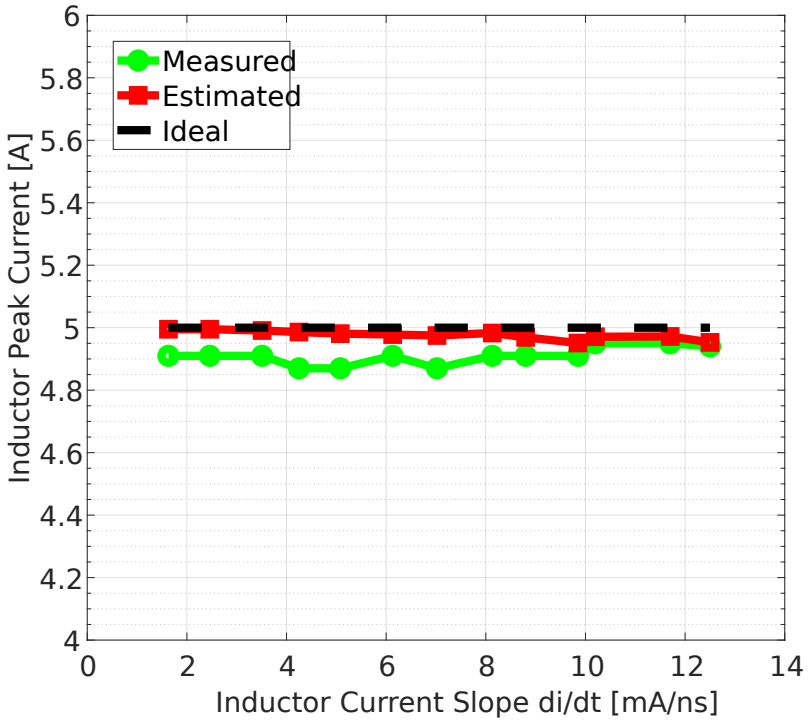


Figure 5.13: Experimental and analytical positive peak inductor current $i_{L,+}$ waveforms using the proposed delay mitigation technique.

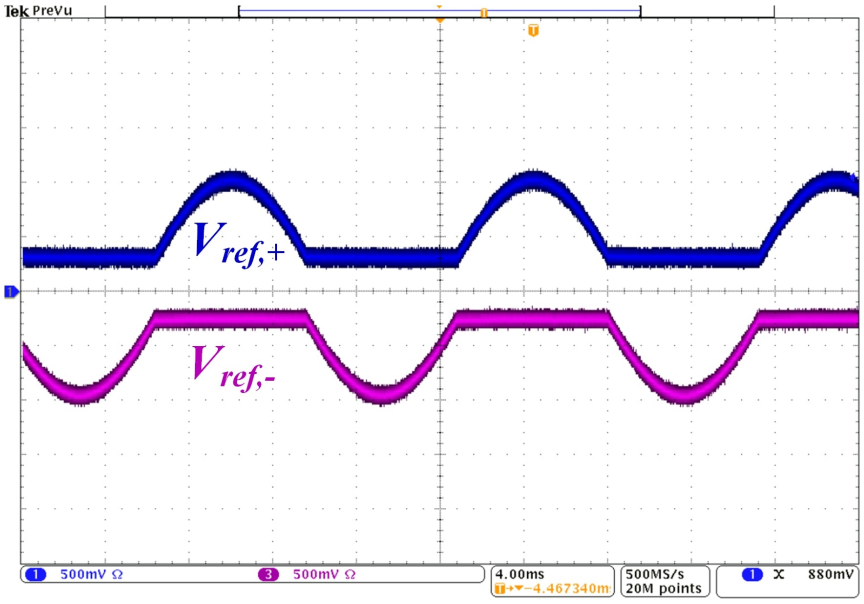


Figure 5.14: Inductor positive reference $V_{ref,+}$ and negative reference $V_{ref,-}$ voltage waveforms.

First, using the previously derived parameters (R_{shunt}= 20mΩ, t_{delay} = 63ns, and L_{par} = 1.2nH), Fig. 5.15 illustrates the corresponding inductor current (I_L), and compensated output current (I_{out}) of the BCM ZVS full bridge inverter using the improved DCPM control with the proposed delay mitigation technique. The obtained RMS inductor current is 1.98 A and does not deviate from its desired reference with a measured RMS output current of 1.15 A and a total harmonic distortion (THD) of 0.85%.

Second, for the same reference inductor current and minimum expected propagation delay of 63 ns, when using a R_{shunt} of 12 mΩ for instance, the effect of parasitic inductance L_{par} is dominant. The compensation condition is less than zero, meaning that the product of propagation delay and the shunt resistance is unmatched with the parasitic inductance. As shown in Fig. 5.16, the output current (I_{out}) is slightly distorted and higher than expected with a measured THD of 1.4%. In the third example demonstrated in Fig. 5.17, when using a higher shunt resistance of 30 mΩ with the expected propagation delay of t_{delay} = 73 ns, the compensation condition is greater than zero. Thus, the effect of propagation delay is dominant in this case. Although this does not affect the output current THD, it results in an increase of the RMS inductor current by 10% and a drop in regulation of the RMS output current to 1.10 A.

The obtained experimental results using the proposed delay mitigation technique for all three scenarios are summarized in Table 5.5. In the case where the compensation condition is less than zero when R_{shunt} =12 mΩ, the parasitic inductance is reduced in half by placing two higher value shunt resistors 30 mΩ and 20 mΩ with the same package in parallel. With the minimum expected propagation delay of 63 ns, and the parasitic inductance now 0.6 nH, current compensation is achieved. The measured compensated output current has a THD of 0.85% and an RMS current of 1.12 A. The output current THD is improved by 39% and the RMS current is regulated within the design target.

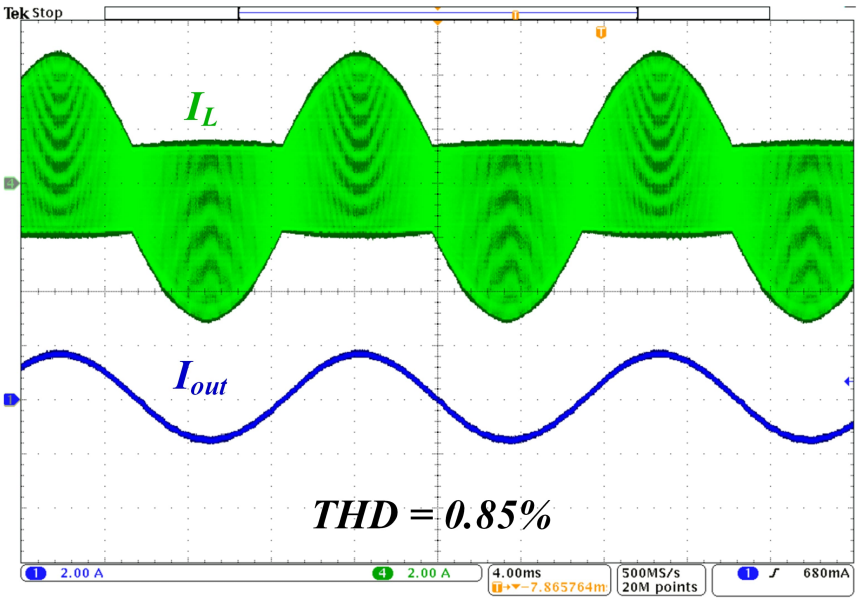


Figure 5.15: Inductor current I_L and output current I_{out} waveforms of BCM inverter with compensation condition of zero $(t_{delay} - L_{par}/R_{shunt}) \approx 0$, $R_{shunt} = 20\ m\Omega$, $t_{delay} = 63\ ns$ and $L_{par} \approx 1.2\ nH$.

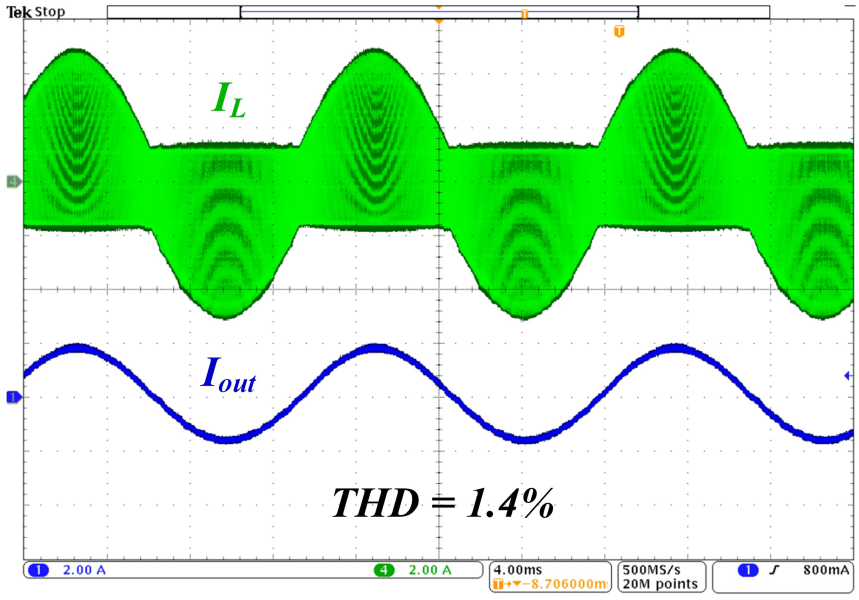


Figure 5.16: Inductor current I_L and output current I_{out} waveforms of BCM inverter with compensation condition less than zero $(t_{delay} - L_{par}/R_{shunt}) < 0$, $R_{shunt} = 12\ m\Omega$, $t_{delay} = 63\ ns$ and $L_{par} \approx 1.2\ nH$.

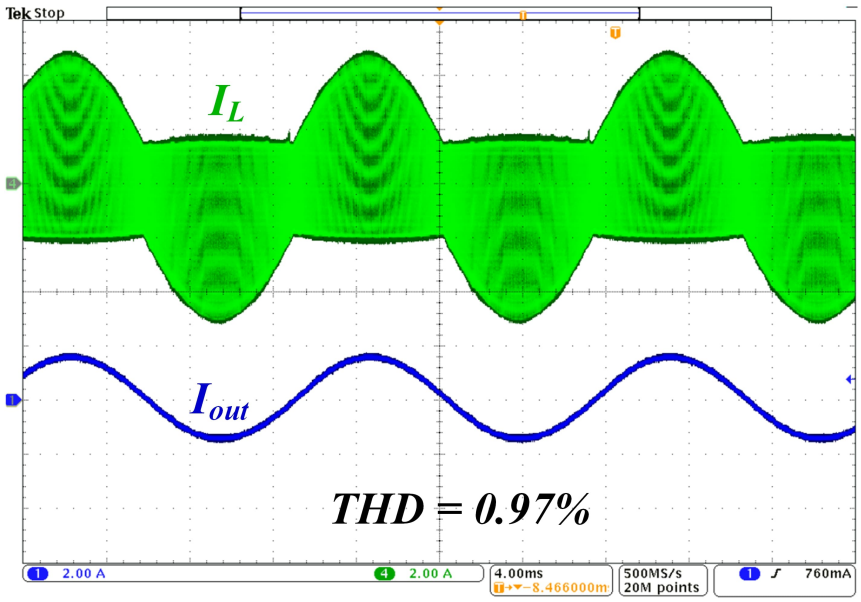


Figure 5.17: Inductor current I_L and output current I_{out} waveforms of BCM inverter with compensation condition greater than zero $(t_{delay} - L_{par}/R_{shunt}) > 0$, $R_{shunt} = 30\ m\Omega$, $t_{delay} = 73\ ns$ and $L_{par} \approx 1.2\ nH$.

Table 5.5: Summary of Experimental results

Shunt Resistance R_{shunt} (mΩ)	Propagation Delay t_{delay} (ns)	Parasitic Inductance L_{par} (nH)	Compensation Condition $t_{delay} - (L_{par}/R_{shunt})$	THD (%)	Inductor Current $I_{L,rms}$ (A)	Output Current $I_{out,rms}$ (A)
20*	63	1.2	≈ 0	0.85	1.98	1.15
12	63	1.2	< 0	1.4	2.0	1.23
$(30\|\|20)*$	63	0.6	≈ 0	0.85	2.0	1.12
30	73	1.2	> 0	0.97	2.1	1.10
$(15+15)*$	73	2.4	≈ 0	0.99	1.97	1.15

* Compensated using the proposed delay mitigation technique.

In the third case when R_{shunt}=30 mΩ, the compensation condition is greater than zero; thus, the parasitic inductance is doubled by placing two 15 mΩ shunt resistors with the same package in series and also digitally programming an additional delay of 10 ns to meet the design compensation condition of approximately zero. The increased parasitic inductance from 1.2 nH to 2.4 nH in this instance helps to mitigate the effect of propagation delay. The extra peak inductor current is eliminated and the measured RMS inductor current is reduced to 1.97 A. The output current has a THD of 0.99% and an RMS current of 1.15 A as expected.

Fig. 5.18 shows the experimental waveform of the compensated output current for all three design scenarios using the proposed delay mitigation technique. By sizing R_{shunt}, t_{delay}, and L_{par} to satisfy the compensation condition of zero, the effect of propagation delay and parasitic inductance cancel each other out. This yields a better control performance, lower RMS inductor current, and no AC output current degradation.

5.3 Summary

An improved simple and low-cost noise immunity and current compensation model to address noise and propagation delay challenges prevalent in boundary current mode control has been proposed. A combination of one-shot and AND gates are used to implement a blanking time that prevents the noise during the inductor zero current transition to interfere with the operation of the active switch. The proposed solution has been successfully demonstrated in an experimental GaN-based half-bridge inverter prototype that operates at a maximum frequency of 800 kHz and 3.5 A inductor peak current. The propagation delay of the proposed current control network has been characterized, and a current compensation method that takes advantage of the parasitic inductance in the shunt resistor to estimate the compensation error has been proposed.

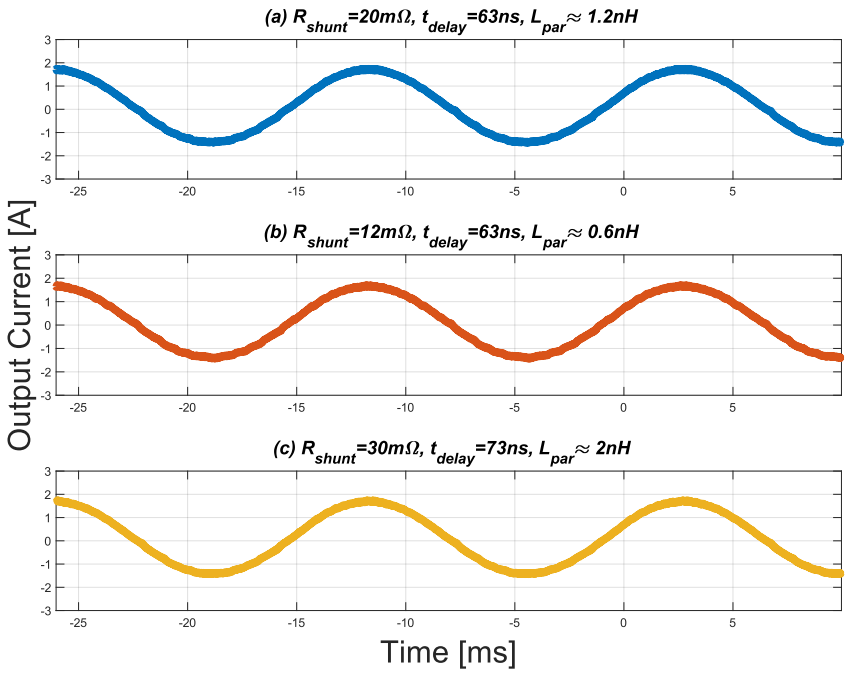


Figure 5.18: Output current I_{out} using delay mitigation technique with (a) matched compensation condition using $R_{shunt} = 20\ m\Omega, t_{delay} = 63\ ns$, and $L_{par} = 1.2\ nH$ (b) reduced L_{par} to 0.6 nH to match compensation condition when $R_{shunt} = 12\ m\Omega$, and $t_{delay} = 63\ ns$, (c) increased L_{par} to 2 nH and t_{delay} to 73 ns to match compensation condition when $R_{shunt} = 30\ m\Omega$.

Chapter 6

Design and Implementation of a Bipolar-Unipolar Switched Boundary Current Mode Control Single-Phase Inverter

High power density and high-efficiency converters are two important design targets in power electronics for many modern applications such as electric vehicles and renewable energy. Recent trends have put an emphasis on reducing the size of inverters and rectifiers for residential and commercial grid-tied applications. A smaller and lighter inverter can reduce the size of the overall system and the associated cost of installation and maintenance [15, 53, 64]. To achieve this goal, a common single-phase full-bridge inverter operating at a high switching frequency is often used. However, the high switching frequency results in high power loss and more severe electromagnetic interference (EMI) limiting the maximum switching frequency in practice [53, 126]. To overcome these challenges, soft switching techniques such as boundary current mode (BCM) control is used in inverters to realize zero voltage switching (ZVS) operation and minimize switching losses [65, 133, 130, 131].

6.1 Boundary Current Mode Modulation

BCM modulation without the use of auxiliary components is a low-cost soft switching approach in order to achieve high efficiency and high power density [139, 140, 131, 141, 142, 128, 143]. The basic operation principle of the BCM inverter is illustrated in [140] and [131]. To achieve ZVS operation with minimal current stresses, the inductor current is controlled in a full bridge topology to follow the envelope wave shape shown in Fig. 6.1. BCM modulation exhibits cycle-by-cycle inductor current polarity inversion, facilitating operation with zero-voltage switching of all semiconductor devices. This feature can be used to increase the switching frequency in order to reduce the size of passive components, to increase efficiency by greatly reducing switching losses, or a combination of the two [128, 133, 65, 132, 129, 144].

BCM modulation can be achieved using either unipolar or bipolar switching schemes. Regardless of switching operation, efficiency, CM noise and output current distortion are all important factors governing the design of the inverter [145]. The presence of common mode (CM) noise and leakage current can cause safety issues, increase system loss, and induce electromagnetic interference (EMI) [39, 25, 29]. Both unipolar and bipolar switched BCM inverters for off-grid applications have been explored in detail in the context of low-frequency output current distortion, efficiency, leakage current and common mode voltage. The unipolar switched inverter has the advantage of low switching loss; however, it has a significant distortion of the output current at the zero crossing as well as significant CM noise [145, 34]. Although the bipolar switched inverter has almost non-existent high-frequency CM noise and zero-crossing output current distortion, it has the disadvantage of low efficiency due to increased switching loss [145]. Taking advantage of the benefits of both switching schemes, while also mitigating their respective challenges, a combination of both unipolar and bipolar switched BCM inverters can be used to help improve efficiency, eliminate current distortion and minimize leakage current. The proposed technique eliminates the low-frequency output current at the zero crossing while improving efficiency by 2% in comparison to a standard bipolar switched BCM inverter.

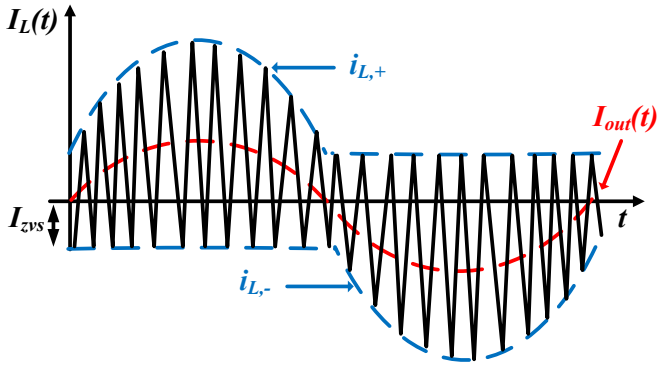


Figure 6.1: BCM modulation inductor current waveform with fixed reverse ZVS current I_{zvs}.

6.1.1 BCM with Unipolar Switching

The traditional full bridge topology often used in a unipolar switched BCM control inverter is shown in Fig. 6.2. This topology uses an asymmetrical inductor configuration, consisting of one inductor on the high switching frequency phase leg A.

The phase leg A devices, S_1 and S_3, operate at high switching frequency while the phase leg B switches, S_2 and S_4, operate at line-cycle frequency. During the positive half line cycle, S_4 is on and S_2 is off and vice-versa during the negative half period. During the output current zero crossing, all switches are turned off. For a given positive and negative peak inductor current $I_{L,+}$ and $I_{L,-}$, the ON/OFF time with reference to the active switch are

$$t_{on} = \frac{L \cdot (I_{L,+} - I_{L,-})}{V_{dc} - V_{out}} \tag{6.1}$$

$$t_{off} = \frac{L \cdot (I_{L,+} - I_{L,-})}{V_{out}} \tag{6.2}$$

which result in a switching frequency which varies over the line cycle as

$$f_s = \frac{V_{out} \cdot (V_{dc} - V_{out})}{V_{dc} \cdot L \cdot (I_{L,+} - I_{L,-})} \tag{6.3}$$

For the following analysis, the average value of the dc-link voltage V_{dc} is assumed to be 250 V, the RMS output voltage V_{out} is 120 V, and the line frequency is 60 Hz. In addition, the analysis assumes a fixed reverse ZVS current I_{zvs}. Fig. 6.3 shows how the ON time, t_{on} and switching frequency f_s vary for two inductance, 10 μH and 30 μH during the positive half-cycle. For instance, for an inductance L_A of 10 μH, the minimum ON time and switching frequency converge to zero at the zero crossing. When the switching frequency is at its peak value of 880 kHz, t_{on} is approximately 370 ns. Unipolar switching can only demagnetize the inductor current at a rate of $-V_{out}/L$. In a standalone system when the output voltage V_{out} approaches zero, the switching frequency converges to zero causing a distortion of the current and a potential loss of regulation [146]. This undesirable issue requires the implementation of additional control to ensure BCM waveforms and output regulation are maintained or minimally distorted during the output voltage zero crossing.

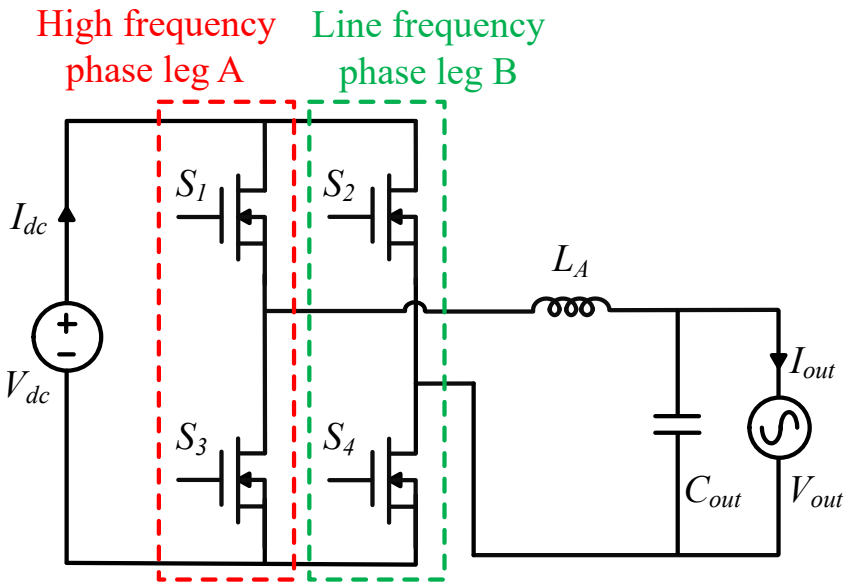


Figure 6.2: Full bridge inverter topology for unipolar switched BCM inverter.

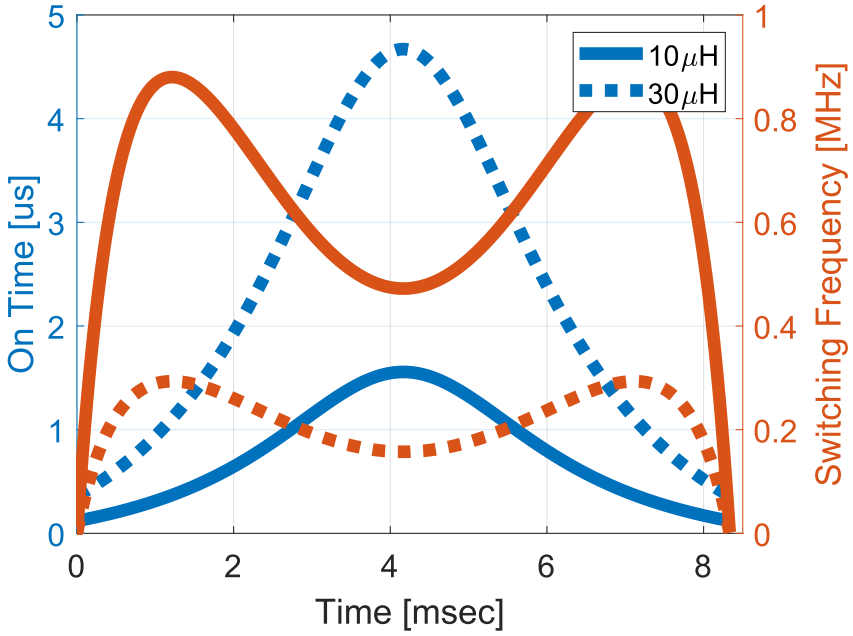


Figure 6.3: On time t_{on} and switching frequency f_s for 10 μH and 30 μH inductor in a unipolar switched BCM inverter during the positive half line cycle.

Fig. 6.4 illustrates an experimental waveform of the output current distortion at the zero crossing. In addition, this switching scheme yields a pulsating CM voltage at the output of the inverter, thus contributing to CM noise and leakage currents [44]. Topologies such as the H5, H6, and HERIC alleviate issues with leakage currents in unipolar switched transformerless inverters through the use of additional switches; however, the bipolar switched BCM full bridge does not exhibit the same leakage current issues when using balanced output impedance [44].

6.1.2 BCM with Bipolar Switching

To overcome the zero crossing regulation and leakage current issues present with a unipolar switched BCM inverter, a bipolar switching technique is often used. The topology for the bipolar switched BCM full bridge inverter with a symmetrical inductor configuration is shown in Fig. 6.5.

The inductance is split between both phase legs to balance impedance and minimize common-mode effects. The total equivalent inductance is $L_{eq} = L_A + L_B$. In contrast to a unipolar switched BCM inverter, both phase legs A and B are switched at high frequency. Switches S_1 and S_4 are switched in unison at high switching frequency and complementary to S_2 and S_3. The turn ON/OFF time of the active switches are

$$t_{on} = \frac{L \cdot (I_{L,+} - I_{L,-})}{V_{dc} - V_{out}} \tag{6.4}$$

$$t_{off} = \frac{L \cdot (I_{L,+} - I_{L,-})}{V_{dc} + V_{out}} \tag{6.5}$$

and the switching frequency is

$$f_s = \frac{V_{dc}^2 - V_{out}^2}{2V_{dc} \cdot L \cdot (I_{L,+} - I_{L,-})} \tag{6.6}$$

As illustrated in Fig. 6.6, the frequency does not drop to zero at the output current zero crossing. Because the zero-state is not employed in bipolar modulation (i.e. the differential output is always V_{dc}), inductor demagnetization occurs in finite time as long as $|V_{out}| < V_{dc}$.

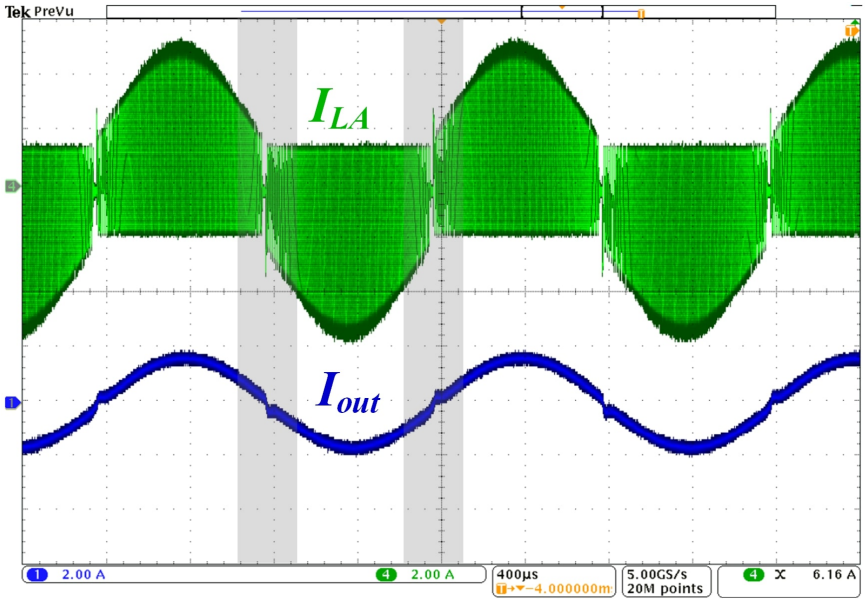


Figure 6.4: Experimental inductor current I_{LA} and output current I_{out} waveform of unipolar switched BCM inverter showing output current distortion at the zero crossing.

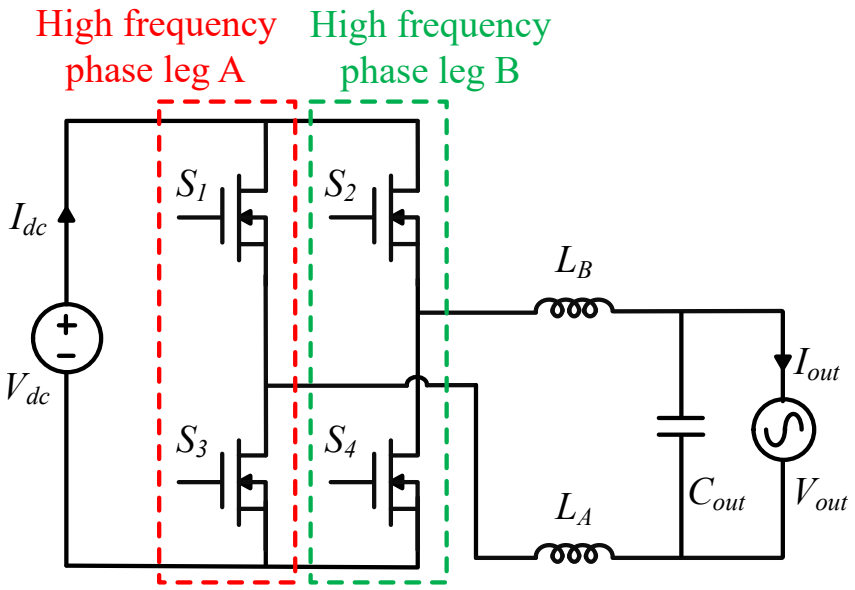


Figure 6.5: Full bridge inverter topology for bipolar switched BCM inverter.

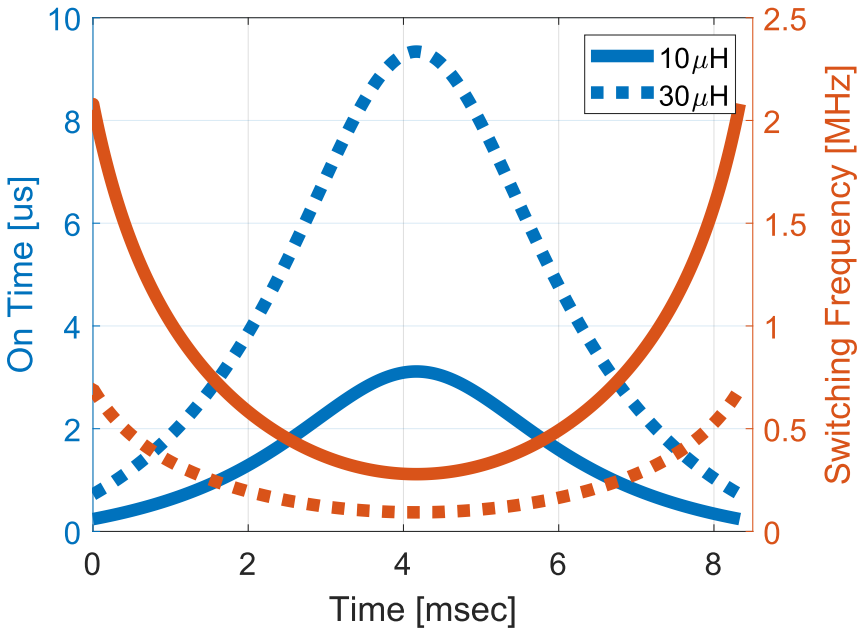


Figure 6.6: On time t_{on} and switching frequency f_s for 10 μH ($L_{eq} = 20$ μH) and 30 μH ($L_{eq} = 60$ μH) inductor in a bipolar switched BCM inverter during the positive half line cycle.

Therefore, the current distortion observed in the unipolar switching case does not occur in the bipolar case. For an inductance L_A and L_B of 10 μH as in the unipolar switching case, the resulting equivalent inductance L_{eq} is 20 μH. Despite doubling the equivalent inductance in this case, the minimum ON time is around 240 ns while the maximum switching frequency is approximately 2.1 MHz. The resulting maximum switching frequency in this case more than double that of the unipolar, resulting in increased switching loss when both modulations achieve ZVS. The common mode voltage in this switching scheme has no high-frequency variation; thus, the CM noise and leakage current are nearly eliminated [44, 29].

Although the bipolar switched BCM inverter helps mitigate current distortion at the zero crossing and minimize leakage current, it results in lower efficiency due to the high switching loss [145]. In addition, the additional inductor in this architecture makes this design costly.

6.2 Bipolar-unipolar switched BCM inverter

Fig. 6.7 shows the proposed BCM inductor waveform using a combination of bipolar and unipolar switching technique. The modulation technique consists of using unipolar switching (U) during the high current sections of the line cycle and bipolar switching (B) at the zero crossing. Using bipolar modulation near the zero-crossing eliminates issues related to zero-crossing distortion inherent to unipolar modulation, while unipolar switching at high currents reduces switching losses. The transition between unipolar and bipolar modulation occurs when the unipolar switching ON time falls below a specified minimum $t_{on,min}$.

Because BCM modulation achieves ZVS for all switching actions, remaining switching loss mechanisms are dominated by turn-off loss and deadtime reverse conduction, both of which increase significantly at high currents and are proportional to switching frequency. Thus, confining bipolar operation to the low-current portion of the line cycle will minimize the resulting impact on switching losses.

As previously noted, in the unipolar switched topology, there is only one high switching frequency phase leg with an asymmetrical inductor configuration. On the other hand, during bipolar switching, both phase legs are operated at high switching frequency with equal inductance on both phases A and B. Given two sets of inductor configuration in a full bridge

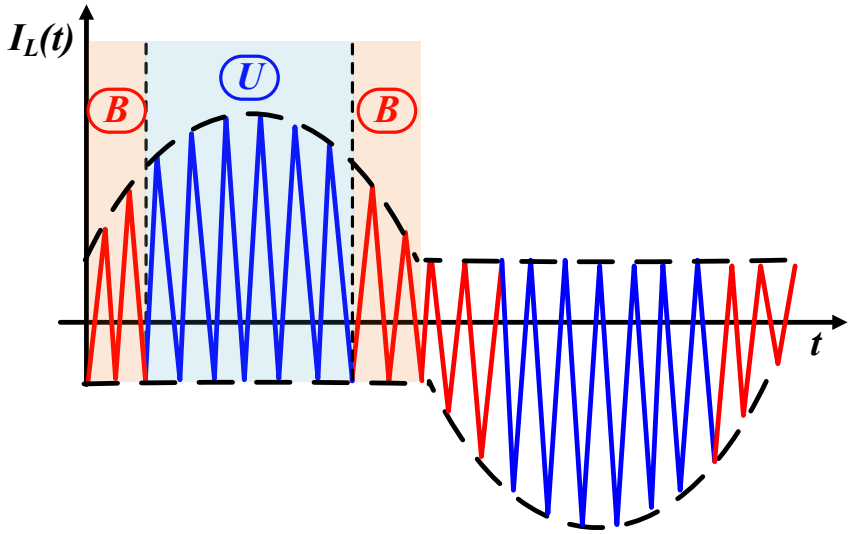


Figure 6.7: Proposed bipolar-unipolar switched BCM modulation waveform with fixed reverse ZVS current I_{zvs}.

topology depending on the switching method, the implementation of the bipolar-unipolar switching technique on either the single-inductor topology in Fig. 6.2 or the split-inductor topology of Fig. 6.5 will result in oscillations in the opposite mode.

6.2.1 Hardware Architecture

When the bipolar-unipolar switching technique is implemented using the full bridge topology with the asymmetrical inductor configuration illustrated in Fig. 6.2, it introduces a high-frequency common mode voltage during the bipolar switching mode [29]. Phase leg B, previously switched at line frequency during unipolar operation, is now switching at high frequency during bipolar operation near the zero crossing. This operation, with only a single inductor, allows the high-frequency voltage at the switch node V_B to directly connect to one terminal of the output, resulting in significant common mode variation and excitation of any parasitic grounding capacitance at the switching frequency. This issue is mitigated by using a symmetrical inductor configuration with an inductor on each phase leg as in bipolar switched BCM full bridge topology in Fig. 6.5.

Although the symmetrical inductor configuration addresses the high-frequency common mode issue, it now introduces a resonance between the phase B inductor L_B and the parasitic grounding capacitance of the output during unipolar switching operation.

To overcome these challenges, an additional phase leg C is introduced as illustrated in Fig. 6.8. Phase A and B are operated at high switching frequency during bipolar switching while phase C is operated at line frequency during unipolar switching. This hardware solution mitigates the high frequency CM voltage issue during bipolar switching and the resonance problem during unipolar switching. However, the additional phase leg increases the component count and changes the equivalent inductance during each switching mode. During bipolar switching, the equivalent inductance $L_{eq} = L_A + L_B$; during unipolar switching the equivalent inductance is half as large, $L_{eq} = L_A$. The resulting switching frequency and ON time for two sets of inductances are shown in Fig. 6.9. The frequency is at its maximum at the zero crossing when using bipolar switching and does not converge to zero. Everywhere else, the frequency distribution is given by the unipolar switching.

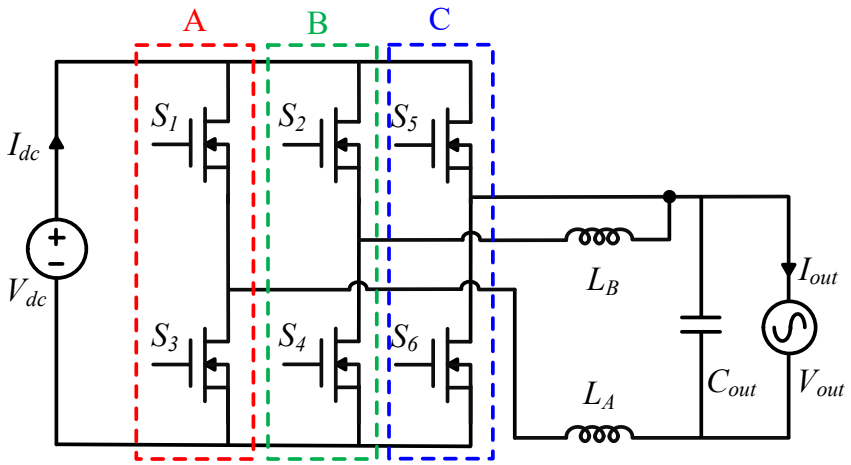


Figure 6.8: Full bridge inverter topology for proposed bipolar-unipolar switched BCM inverter.

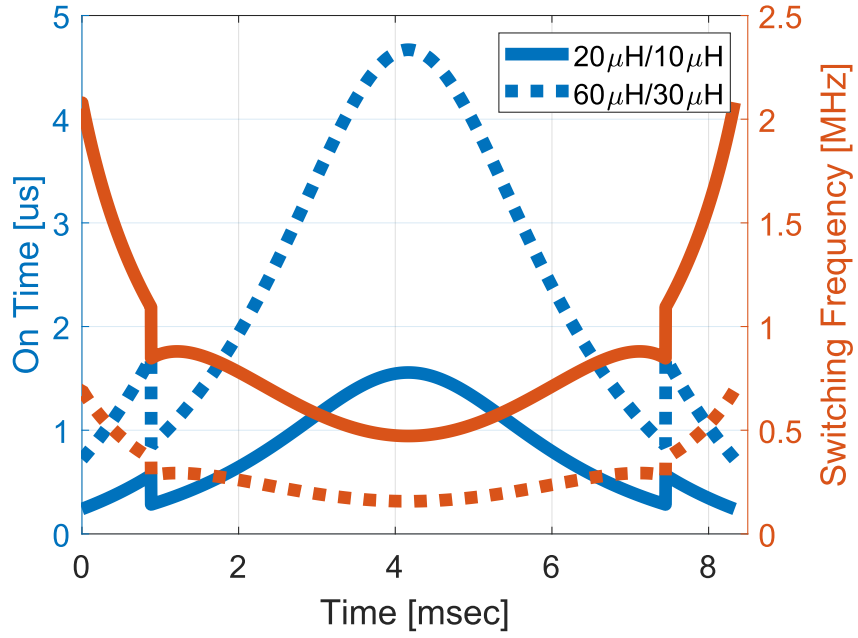


Figure 6.9: On time t_{on} and switching frequency f_s for an equivalent inductance of 20 $\mu H/10$ μH and 60 $\mu H/30$ μH in a bipolar-unipolar switched BCM inverter during the positive half line cycle.

6.2.2 Tradeoff Between Standard Bipolar and Bipolar-Unipolar Switching Technique

When compared with a standard bipolar-switched BCM inverter, first, the switching frequency during the unipolar switching phase in the proposed approach is slightly higher. As illustrated in Fig. 6.10, for an equivalent inductance L_{eq} of 20 μH the switching frequency of the proposed switching scheme is larger during the unipolar phase. The increased switching frequency during the unipolar switching phase is due to the half reduction of the inductance. This slight increase in frequency has a minimal effect on the device switching loss because during the unipolar operation, only two devices are switched at high frequency rather than the four in bipolar, resulting in reduced switching losses.

Second, the hardware implementation of the proposed switching technique introduces additional control complexity and requires careful consideration of current commutation during the transition between the switching phases. If not timed correctly, this may introduce some distortion of the output current, causing an increase in THD. In comparison to a bipolar-switched BCM inverter, the proposed bipolar-unipolar switching technique is a tradeoff between efficiency and THD.

6.3 Converter Loss Model

To analyze the impact of the switching scheme on the converter efficiency, the devices and inductor losses are estimated and the efficiency between the standard bipolar switched BCM inverter is compared with the bipolar-unipolar switching model. Based on the applied BCM switching technique, both the inductor core and winding loss with the device switching and conduction loss are the main contributor to the power loss. Other forms of loss do not vary significantly with different switching techniques.

6.3.1 Switching Frequency

In this design, the switching frequency range is limited by the minimum ON time during the bipolar switching phase at light loads. For noise immunity and good control performance,

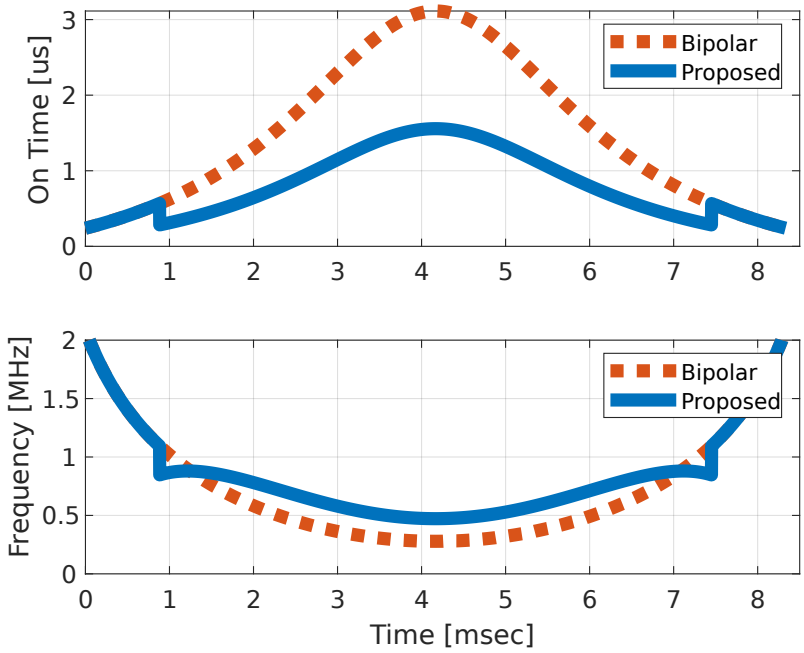


Figure 6.10: On time t_{on} and switching frequency f_s for an equivalent inductance of 20 μH in a standard bipolar and 20 μH/10 μH in a proposed bipolar-unipolar switched BCM inverter during the positive half line cycle.

a minimum ON/OFF time of 200 ns and a maximum switching frequency of 1 MHz are selected. These limits constrain the selection of inductance and ZVS current value.

Fig. 6.11 shows the frequency distribution during the positive half-cycle for different inductance combinations during bipolar/unipolar switching. The 40 μH/20 μH inductance combination is within design specification and has been selected. Although larger inductance values above the 40 μH/ 20 μH combination also satisfy the design constraint, they have not been considered because they require either more volume or exhibit more core loss.

6.3.2 Converter Switching and Magnetic Loss

An analytical loss model of the inverter, including the inductor, device and shunt resistor is developed. Based on the applied switching technique, both the inductor core loss and device switching and conduction loss are the main contributors to the power loss. Other forms of loss do not vary significantly with different switching techniques. After surveying available planar cores for high frequency, high power applications, an EI38 planar core made from 3F4 ferrite material from Ferroxcube is used to implement the two 20 μH inductors. Based on the planar inductor design outlined in [147, 148] and the loss model, a 4-turn, 2 oz profiled copper trace winding is used to achieve a 20 μH inductance. The inductor Q3D model and implementation is shown in Fig. 6.12.

The AC resistance of the winding is estimated using a finite element analysis tool and measured experimentally with an impedance analyzer. Fig. 6.13 compares the measured and analytical AC resistance for the selected core material for the EI38 core. As expected, the AC resistance for both materials is dominant at high frequency leading to the increase in ESR as the frequency increases. However, this effect is more acute for the 3F36 than 3F4 material, resulting in a significant difference at higher frequencies. The model matches well with the measurement at frequencies up to 800 kHz.

The core loss P_{fe} is estimated using the Steinmetz Equation for every switching period and averaged over the line cycle as shown in the following equation:

$$P_{fe} = \frac{2A_c \cdot l_m}{\pi} \int_0^{\pi} (K \cdot f_s(\theta)^{\alpha} \cdot \Delta B(\theta)^{\beta}) d\theta \tag{6.7}$$

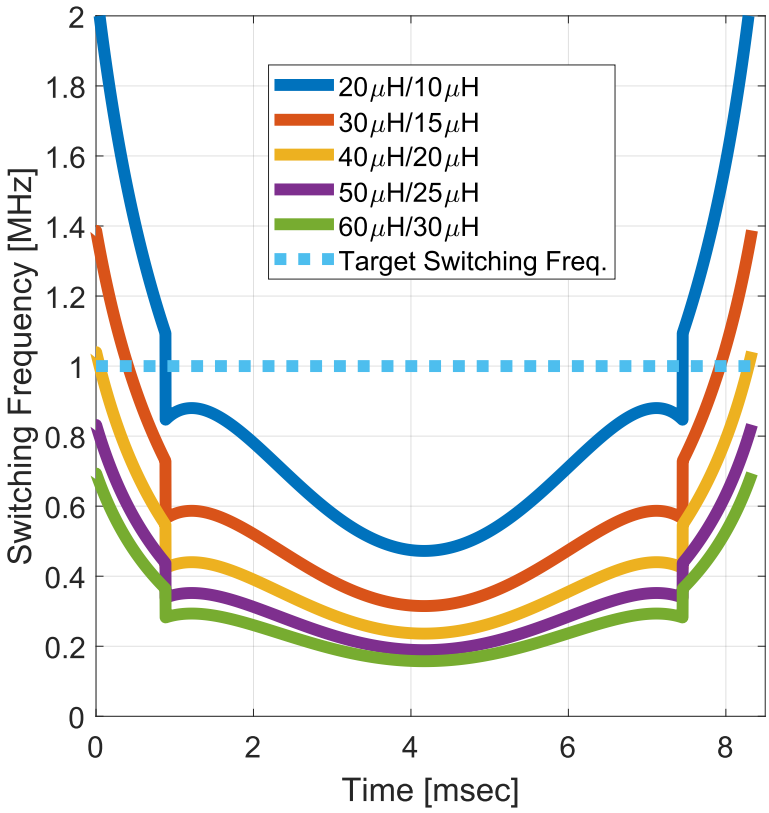


Figure 6.11: Switching frequency f_s for a varied set of inductances $2L_A/L_A$ in a proposed bipolar-unipolar switched BCM inverter during the positive half line cycle.

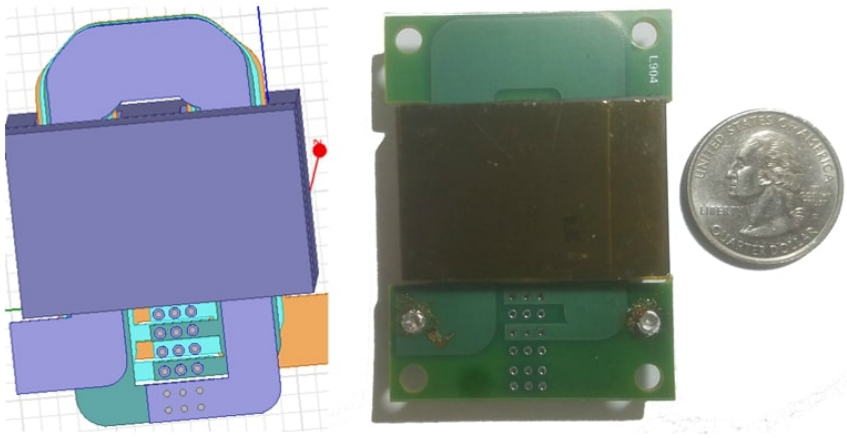


Figure 6.12: Q3D model and designed of 20 μH planar inductor using EI38 planar core and 3F4 ferrite material.

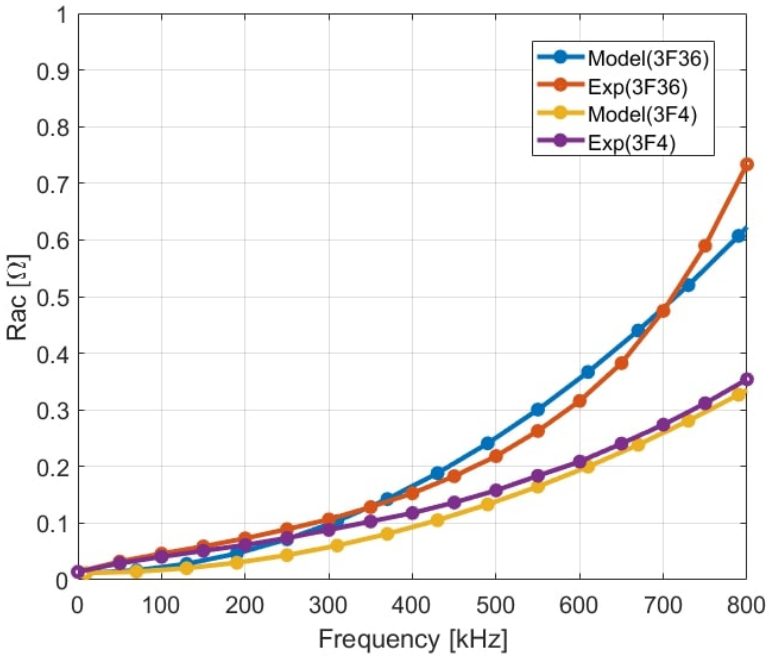


Figure 6.13: Analytical vs experimental result of the AC resistance.

A_c represents the core cross-sectional area and l_m is the magnetic path length. The core material parameters K, α and β are provided by the core manufacturer.

Using BCM modulation, ZVS is achieved throughout the line cycle; the switching losses are primarily turn-off losses. All the switches are implemented using GaN-GIT devices from Panasonic Corporation. Thus, the turn-off loss is estimated using the model developed in [112] for ZVS GaN GIT devices operating in low and high-frequency bridge leg applications. It is important to note that deadtime optimization is not part of this work and the loss analysis does not include reverse conduction losses at the different operating points. As illustrated in Fig. 6.14, the bipolar-unipolar switching technique yields a higher efficiency when compared with the standard bipolar-switched BCM inverter.

6.4 Experimental Results

An experimental prototype of the bipolar-unipolar switched BCM inverter is constructed and shown in Fig. 6.15. The additional phase leg with the second inductor is populated on a second identical board and connected in parallel. The main design parameters are listed in Table 6.1. To ensure ZVS through the entire line cycle, a fixed dead time of 100 ns and a fixed reverse ZVS current of 1.5 A is used. The inverter switching frequency varies from 120 kHz to 750 kHz, maintaining ZVS at all operating points over the line cycle. The inductor positive and negative current limits $I_{L,+}$ and $I_{L,-}$, are set using voltage references and regulated using the improved dual current programmed mode (DCPM) controller circuit. Waveforms of the converter under BCM modulation with a combination of both bipolar and unipolar switching are shown in Fig. 6.16 for an output current RMS of 1.15 A.

To provide a comparison for the proposed switching scheme, a standard bipolar switched BCM modulation is implemented on the same prototype board. The obtained inductor current and output current waveform for both switching approaches are nearly identical and is shown in Fig. 6.17. At 200 W, the measured efficiency for the bipolar-unipolar switching is 93.9% and the output current THD is 1.15%. In contrast, for the fully bipolar switching, the measured efficiency at the same power level is 91.8%, and the THD is 0.85%.

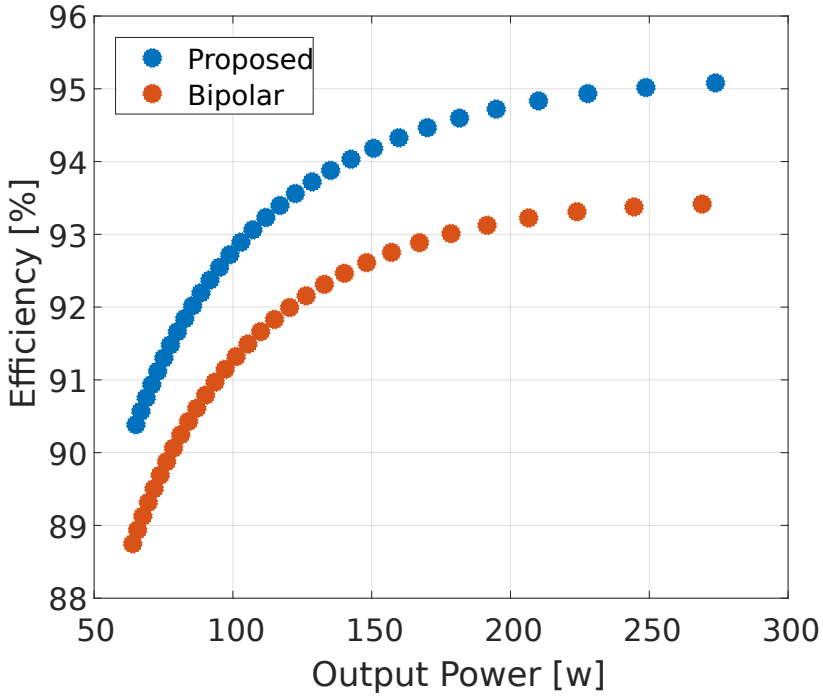


Figure 6.14: Analytical efficiency comparison between the standard bipolar switched and proposed bipolar-unipolar switched BCM inverter.

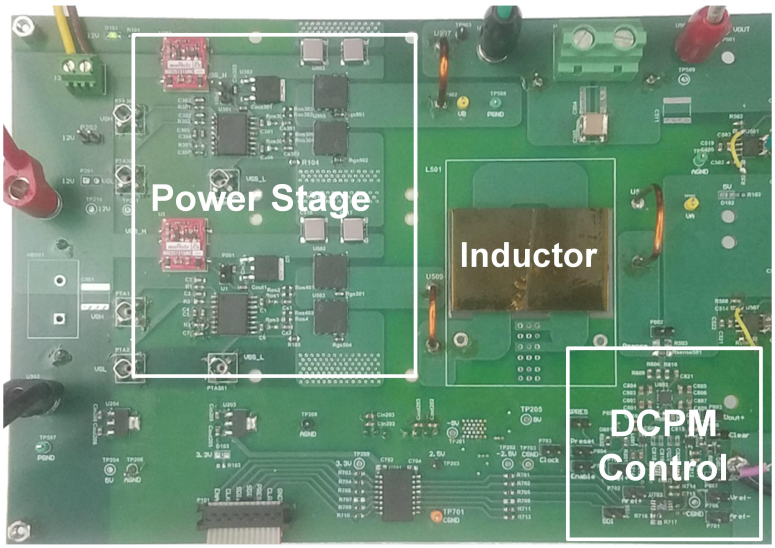


Figure 6.15: Experimental prototype board.

Table 6.1: Parameters of prototype

Parameter	Value
Input voltage V_{dc}	250 V
Output voltage V_{out}	120 V/60 Hz
Device	Panasonic GaN-GIT
Inductor L_A, L_B	20 μH
Shunt Resistor R_{shunt}	20 mΩ
Inductor Core Geometry	Planar EI38
Inductor Core Material	Ferroxcube 3F4
Switching Frequency	120 kHz - 750 kHz

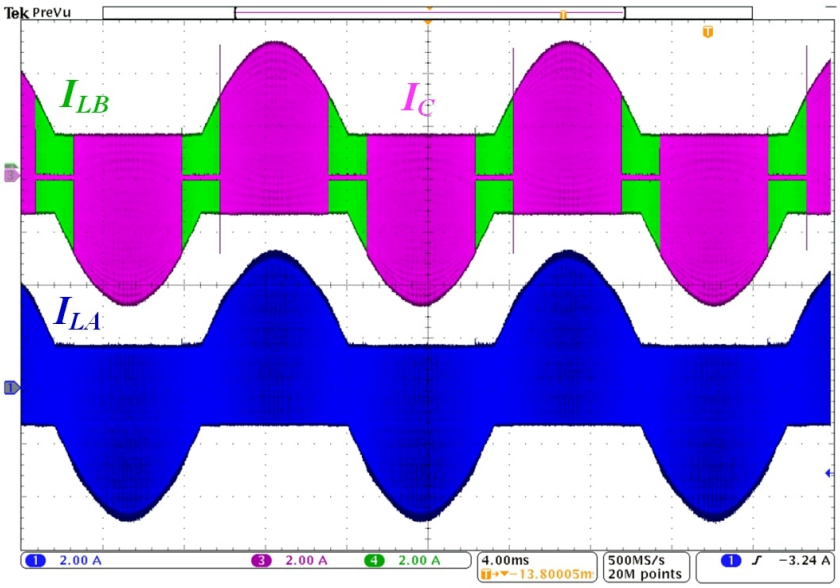
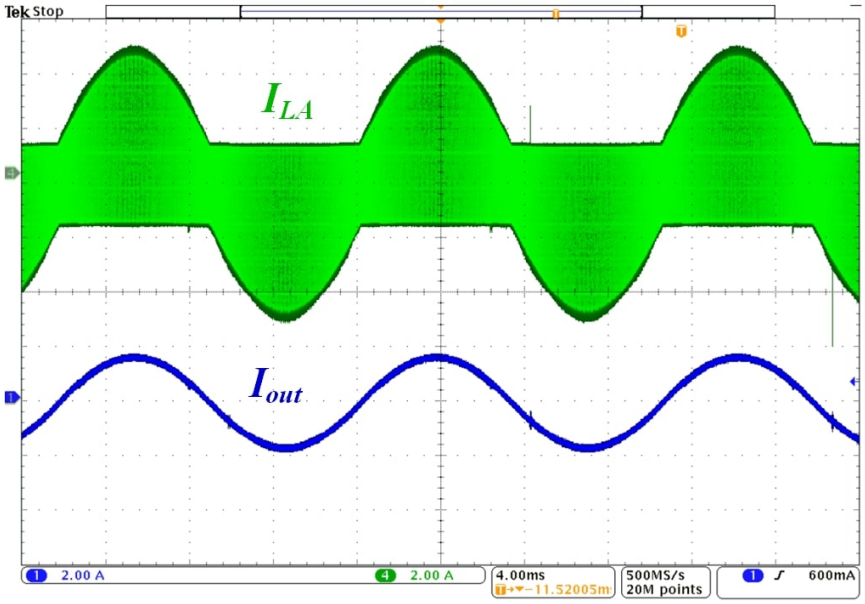
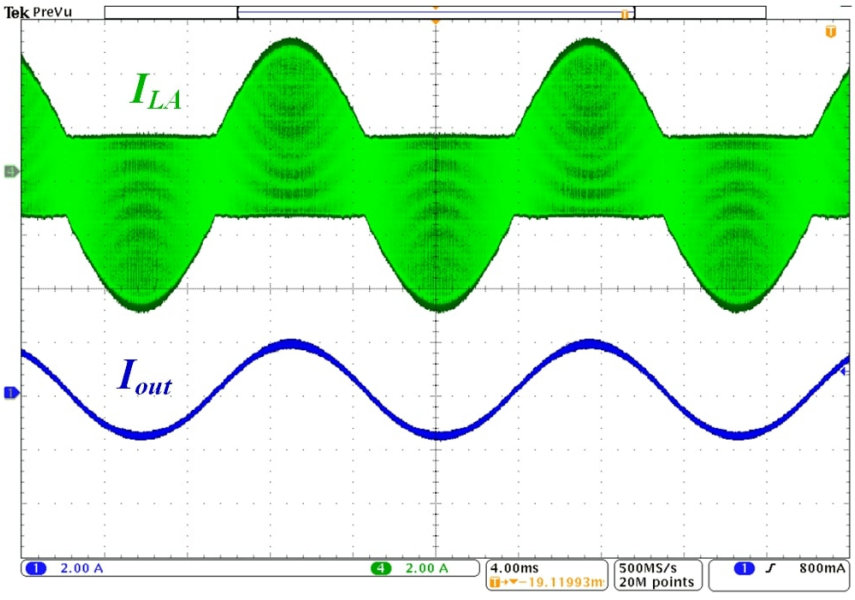


Figure 6.16: Experimental phase leg A inductor current I_{LA}, phase leg B inductor current I_{LB}, and phase leg C current I_C waveform using the proposed bipolar-unipolar switched BCM inverter for $I_{out,rms} = 1.15$ A.



(a)



(b)

Figure 6.17: Experimental phase leg A inductor current I_{LA} and output current I_{out} waveform using (a) proposed bipolar-unipolar switching and (b) standard bipolar switching for $I_{out,rms} = 1.15$ A.

The proposed bipolar-unipolar switched BCM inverter yielded a 2% improvement in efficiency and a slight increase in output current THD in comparison to the standard bipolar-switched BCM inverter.

6.5 Summary

Both unipolar and bipolar switching techniques have been analyzed individually in the context of efficiency, output current distortion, CM noise, and leakage current. Unipolar switched BCM inverter yields higher efficiency but causes a distortion of the output current at the zero-crossing. On the other hand, bipolar switched BCM inverter has the advantage of minimal leakage current and addresses inductor current regulation and distortion issues. However, it results in lower efficiency. Thus, a ZVS BCM control inverter combining both bipolar and unipolar switching has been proposed in this dissertation. This technique takes advantage of the high-efficiency operation of the unipolar switching with the better inductor current regulation of the bipolar switching at zero-crossing. To mitigate the high-frequency CM noise and resonance issue, a full bridge inverter with a dedicated phase leg for each switching phase has been introduced. Although the proposed switching scheme increased control complexity, and the output current THD, it yielded an improved efficiency of approximately 2% at 200 W when compared with a standard bipolar switched BCM inverter.

Chapter 7

LCOE Driven Design Optimization of DHA Inverter

To design an efficient, robust, and reliable inverter with a minimal lifetime cost, an LCOE-driven design optimization of the DHA is presented in this chapter. The derived loss and reliability model are used to evaluate and optimize the inverter architecture design based on efficiency, reliability and cost. The system-level performance of the DHA inverter is evaluated and compared with traditional multiphase inverter without DHA and a full-bridge architecture. Table 7.1 shows the inverter design parameters and target CEC efficiency and B_{10} lifetime.

7.1 Model Development for LCOE Analysis

Power loss or efficiency are oftentimes the criteria of choice for comparing different topologies across the board, but it only captures one aspect of the design. It leaves out important metrics such as reliability and the lifetime cost of the system. To bridge this gap in evaluating a given set of technologies in PV application, the Levelized cost of energy (LCOE) is a fair metric to evaluate the performance of new systems [149]. It captures total system efficiency, reliability, and costs including hardware, operation, and maintenance. The LCOE function

$$\mathrm{LCOE}(x) = \frac{C_{\mathrm{life}}(x)}{E_{\mathrm{life}}(x)} \tag{7.1}$$

Table 7.1: Design Parameters and Target of single-phase PV inverter

Parameter	Label	Value
Rated Power	(P_{dc})	2 kW
DC-link Voltage	(V_{dc})	400 V
AC Output Voltage	(V_{ac})	240 V_{rms}
Switching Frequency	(f_{sw})	$\leq$ 800 kHz
Grid Frequency	(f_{line})	60 Hz
Target CEC Efficiency	(η)	$\geq$ 97 %
Target Lifetime	(B_{10})	$\geq$ 50 years

where $C_{\text{life}}(x)$ is the present value of the inverter total cost during its operational lifetime, and $E_{\text{life}}(x)$ is the total energy supplied to the electric grid by the inverter during its lifetime [71]. Those two parameters are essential to the LCOE calculation. The System Advisory Model (SAM) developed by the National Renewable Energy Laboratory (NREL) is used to compute the LCOE of a PV system [122]. It can be used to simulate real residential PV installation scenarios and comparisons. It is also the principal tool used in calculating the LCOE in the DOE SunShot benchmark [150]. It provides a set of financial assumptions and energy output data from a given region in addition to the inverter performance parameters. Fig. 7.1 shows the details of a sample LCOE calculation for a 10 kW PV system installed in Phoenix, AZ using a generic inverter with 96% efficiency.

The output energy data for that location is shown in Fig. 7.1b and the obtained real LCOE 7.82 ¢/kWh is depicted in Fig. 7.1a. The model assumes a 25-year system lifetime. To assess the performance of the PV inverter and its impact on the LCOE, the lifetime cost and energy production model are used in conjunction with the set of parameters in the SAM model to calculate the LCOE for a given inverter topology.

7.1.1 Cost Model

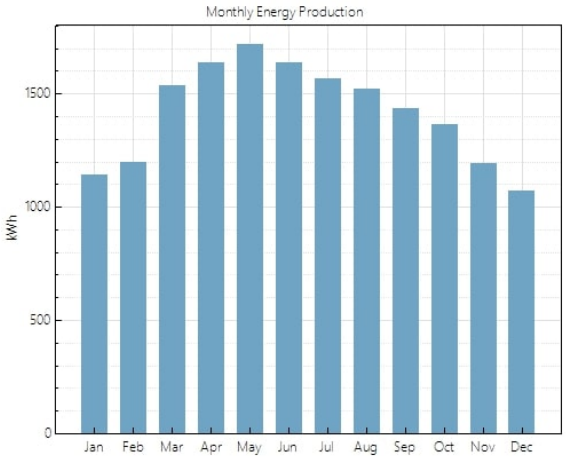
The present value of a PV inverter total lifetime cost C_{life} consists of its initial fixed manufacturing cost C_o and its maintenance and operational cost $C_M(x)$, $C_{\text{life}}(x) = C_o + C_M(x)$. The former is fixed and straightforward to calculate while the latter depends on the reliability characteristics of the inverter. For this analysis, the initial upfront cost of the inverter based on the individual price of components in the inverter is assumed to be the manufacturing cost of the inverter. The cost of a single high-frequency module is estimated and scaled based on the number of modules needed for a given architecture. Thus the initial cost is

$$C_o = \sum_{i=1}^{m} i \cdot C_{mod} \tag{7.2}$$

with m being the total number of modules in a given architecture. C_{mod} is the average cost of a single module comprising of the cost of associated power devices, capacitors, inductor,

Metric	Value
Annual energy (year 1)	17,009 kWh
Capacity factor (year 1)	19.4%
Energy yield (year 1)	1,701 kWh/kW
Levelized COE (nominal)	10.46 ¢/kWh
Levelized COE (real)	7.82 ¢/kWh
Electricity bill without system (year 1)	$2,158
Electricity bill with system (year 1)	$299
Net savings with system (year 1)	$1,859
Net present value	$6,697
Simple payback period	12.8 years
Discounted payback period	NaN
Net capital cost	$26,633
Equity	$0
Debt	$26,633

(a)



(b)

Figure 7.1: Example of a 10 kW PV system installed in Phoenix, AZ showing (a)LCOE analysis and (b) monthly energy output.

printed circuit board (PCB), and any additional part such as control units, etc. Note that the line frequency module does not include the cost of the inductor. Next the present value of the maintenance and operational cost of the inverter $C_M(x)$ is characterized by the reliability of the inverter. According to [71], $C_M(x)$ is computed by estimating the future expenses for repairing the PV inverter to the corresponding present value as

$$C_M(x) = \sum_{i=1}^{n} F_i(x) \cdot C_r \cdot \frac{(1+g)^i}{(1+d)^i} \tag{7.3}$$

where n is the total operational years of the PV inverter, $F_i(x)$ is the average number of failures that the inverter would encounter in a given year of operation i and is characterized by the inverter unreliability function $F(x)$. C_r is the present value cost of repairing the inverter, g and d are the expected annual inflation rate and the annual discount rate respectively.

7.1.2 Energy Production Model

The modified lifetime energy production of the system originally presented in [71] is

$$E_{\text{life}}(x) = \sum_{y=1}^{n} \sum_{t=1}^{8760} P_{pv}(t,y) \cdot \eta(t,y) \cdot \Delta t \cdot N_{mod}(t,y) \cdot (1-\delta)^{y-1} \tag{7.4}$$

where t is the time of operation within a year ($1 \leq t \leq 8760$), y is the operational lifetime of the system in years ($1 \leq h \leq n$), and Δt represent the hourly simulation time step. For a given hour of the year in operation, P_{pv} is the output power generated by the PV, η is the inverter efficiency, and N_{mod} is the total number of operational modules within the inverter during that period. δ denotes the degradation factor of the PV module and can be approximated at 0.8%/year [151]. It's important to note that the PV panel degradation not only decreases the annual energy production of the system, it also shortens the lifetime of the PV inverter [83].

The probability that a given module within an inverter will operate successfully at time t and beyond is given by the unreliability function $F(t)$ of each module and that of the system.

Furthermore, the efficiency of the inverter

$$\eta(t,y) = \frac{P_{pv}(t,y) - P_{loss}(t,y)}{P_{pv}(t,y)} \tag{7.5}$$

characterizes the performance of the converter at any given time. P_{loss} represents the total inverter power loss and is equal to the sum of all the components' losses including devices and passives. P_{pv} is the DC output power of the PV without panel degradation. The output filter is not part of this design and has not been considered in this analysis.

7.2 Optimization Framework

To design an efficient and reliable inverter with a minimal lifetime cost, an LCOE-driven design optimization of the DHA is presented. The converter loss, reliability, and cost model are derived and used to evaluate the optimal inverter architecture design consisting of the number of modules and allocation that would yield a minimum LCOE for a system lifetime of 50 years based on a mission profile in Phoenix, AZ. A flowchart of the proposed LCOE design optimization is illustrated in Fig. 7.2. For a given topology architecture, the objective function

$$\min\left(LCOE(x) = \frac{C_{\text{life}}(x)}{E_{\text{life}}(x)}\right) \tag{7.6}$$

is evaluated using the genetic algorithm (ga) function from the MATLAB optimization toolbox in order to determine the design parameters and architecture configuration provided the loss, reliability and cost model that would yield a minimum LCOE within a total system lifetime of 50 years. For multiphase inverter architecture, there are two levels of optimization. First, for a given number of modules, the device and magnetic loss model are used to determine the allocation that would yield the lowest loss in the power stage. Next, a top-level optimization using a genetic algorithm is used to determine the optimal architecture with the highest reliability and lowest cost. The optimal values of the design parameters are thus evaluated for both DHA and non-DHA architecture (i.e. multiphase and Full-bridge) allowing for a fair performance comparison between the two designs.

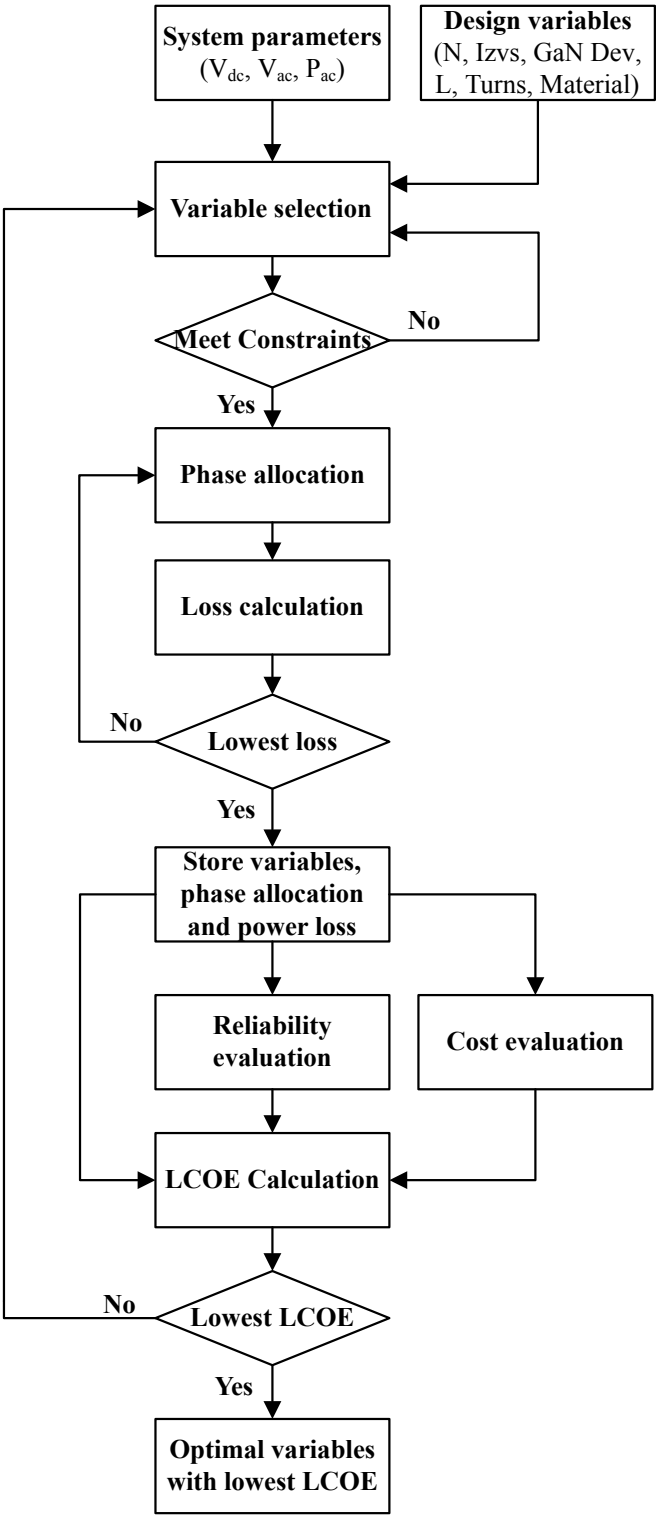


Figure 7.2: Flowchart of the LCOE optimization.

7.3 Power Stage Design

The power stage design target is to come up with an optimal DHA architecture configuration by selecting the optimal inductance value, inductor number of turns, device type and configuration (i.e. single or parallel), phase configuration (i.e. single or multi-phase) that would yield the lowest loss and high reliability. This initial optimization considers power loss and design for reliability technique to maximize the lifetime of the system. The efficiency optimization procedure is given by the power loss cost function

$$\min \{P_{loss}(t)\} \tag{7.7}$$

subject to design specifications and constraints. The specification includes the system full power, the RMS grid voltage, the PV panel DC voltage. The design constraints are given by the number of modules, inductance, inductor number of turns, device type and configuration. The input design variables is summarized in Table 7.2.

7.3.1 Device Selection

Fig. 7.3 shows a schematic configuration of the DHA inverter comprising of n high frequency (HF) modules and a single line-cycle frequency (LF) return phase. The same optimization procedure is used to select the optimal device for the non-DHA multiphase inverter shown in Fig. 7.4 and the traditional full-bridge inverter architecture shown in Fig. 7.5. The device selection is based on minimizing the Levelized cost of energy (LCOE) for a given architecture selection. The half-bridge configuration shown in Fig. 7.6a is the building block of full-bridge based inverter architecture. Its basic power stage configuration consists of two power switches and an inductor. The power switches can be implemented using a single device (Fig. 7.6a), parallel devices (Fig. 7.6b) or using a multi-phase approach as demonstrated in Fig. 7.6c. Any of these configurations outlined in Fig. 7.6 can be used to implement the high-frequency phase leg for inverter and APF operation or the line frequency current return phase leg. With the different possible module configurations, an optimization process is used to determine the inverter architecture and device selection that would yield the highest efficiency and reliability at a minimal cost.

Table 7.2: Optimization Variable Constraints

Parameter	Value
Number of modules	$3 \leq n \leq 10$
HF module device type	GaN
HF device configuration	Single (1x)
LF module device type	MOSFET
LF device configuration	Single (1x) $\leq x \leq$(2x)Parallel
ZVS Current	0.5 A $\leq I_{ZVS} \leq$ 4 A
Inductance	10 µH $\leq L \leq$ 100 µH
Inductor number of turns	3 $\leq$ Turns $\leq$ 10
Core Geometry	Planar EI38
Core Material	3F4, 3F36

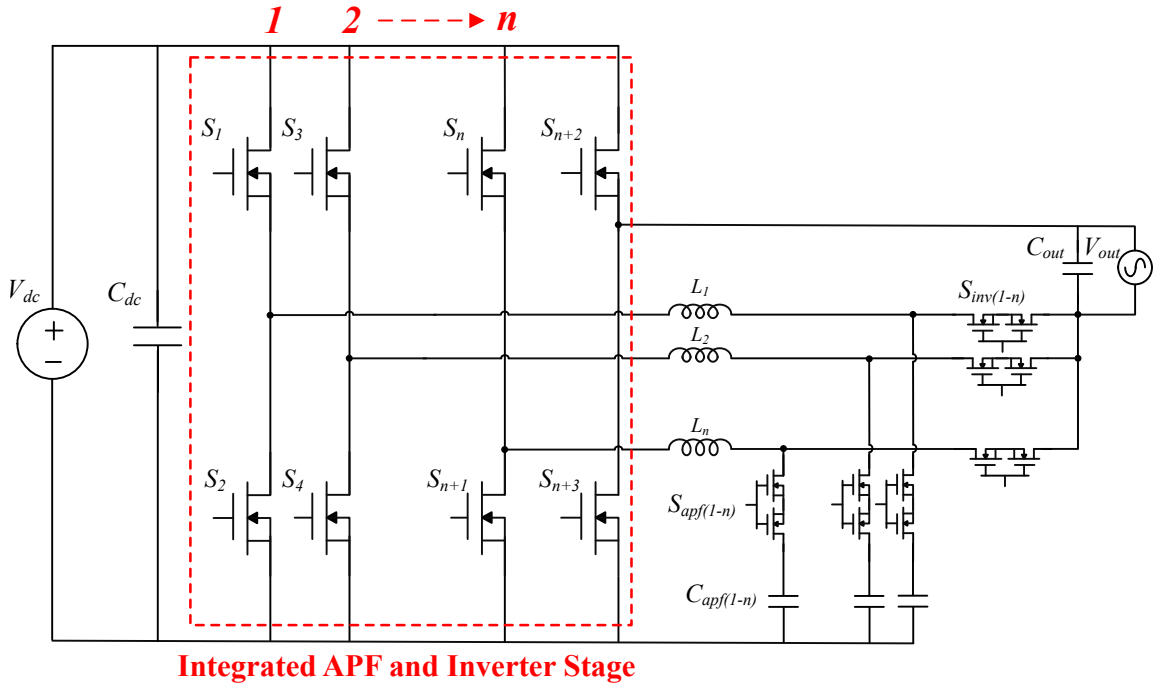


Figure 7.3: DHA Inverter Topology.

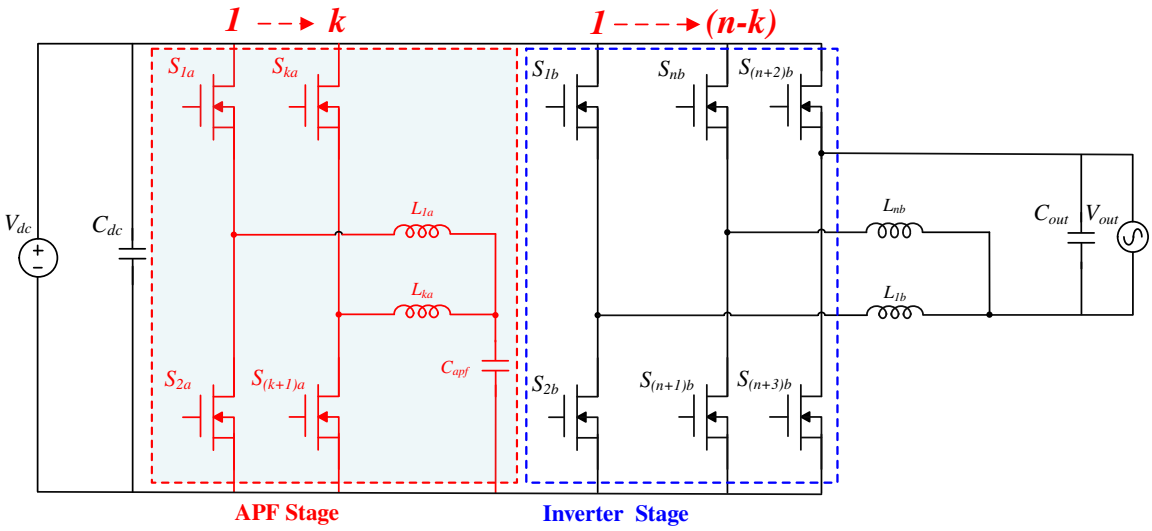


Figure 7.4: Multi phase non-DHA inverter architecture with n HF modules.

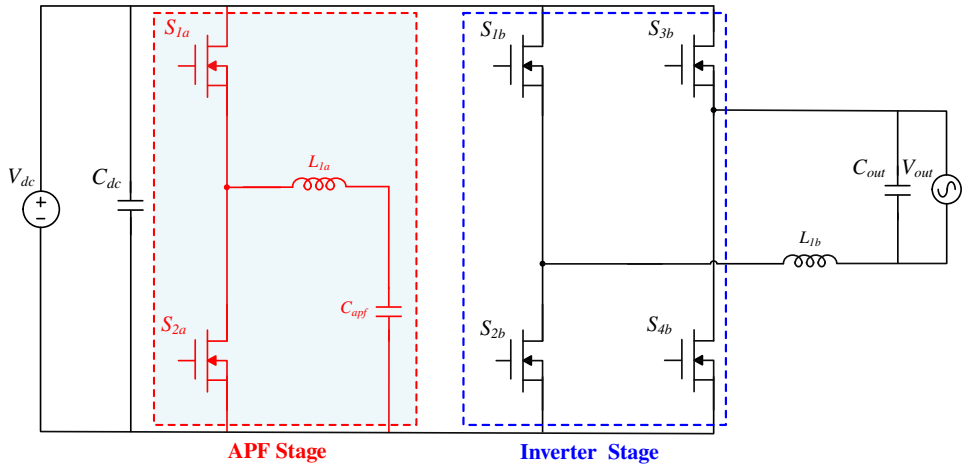


Figure 7.5: Traditional Full-bridge inverter topology with Active Power Filter (APF).

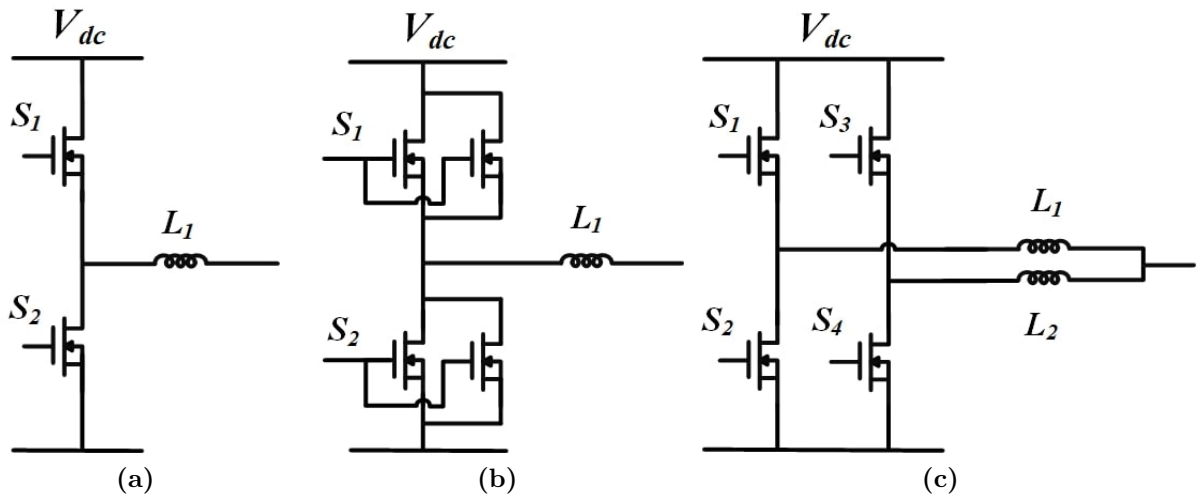


Figure 7.6: Module configuration consisting of (a) single device (b) parallel devices and (c) multiphase.

The selection of devices and their configuration such as single or parallel significantly affect the system architecture. Because of the high-frequency operation of the converter, only 600 V and above GaN devices are considered for the high-frequency module switches for all three topologies. Table 7.3 summarizes the GaN device parameters, used in this optimization. These devices are also based on availability at the writing of this dissertation. Silicon MOSFET power devices are used for the remaining power devices including the inverter-APF switches ($S_{inv(1-n)}, S_{apf(1-n)}$) in the case of DHA and the line frequency module switches. The switching loss at line frequency is negligible, thus only available Si devices with lower ON resistance currently available on the market is considered for this optimization. Table 7.4 shows the parameters for the 600 V Infineon Si MOSFET (IPT60R022S7) with a $R_{on} = 22\ \Omega$ used in this design.

7.3.2 Switching Frequency

The choice of inductance directly affects the switching frequency of the converter. Fig. 7.7 shows the relationship between the switching frequency for different inductor values in the unipolar switched BCM inverter. The switching frequency varies along the line cycle and is at its maximum near the zero crossings. The resulting frequency can reach values in the MHz range during light load operation as shown in Fig. 7.7a, so it is important to limit the frequency to a range that guarantees noise immunity and good performance of the dual current programmed mode controller [108, 109]. Thus, for this design a minimum ON/OFF time of 200 ns and a maximum switching frequency of 800 kHz are selected, based on the hardware design in [110]. These limits constrain the selection of inductance and the reverse conduction current required to achieve ZVS.

7.3.3 Inductor Design

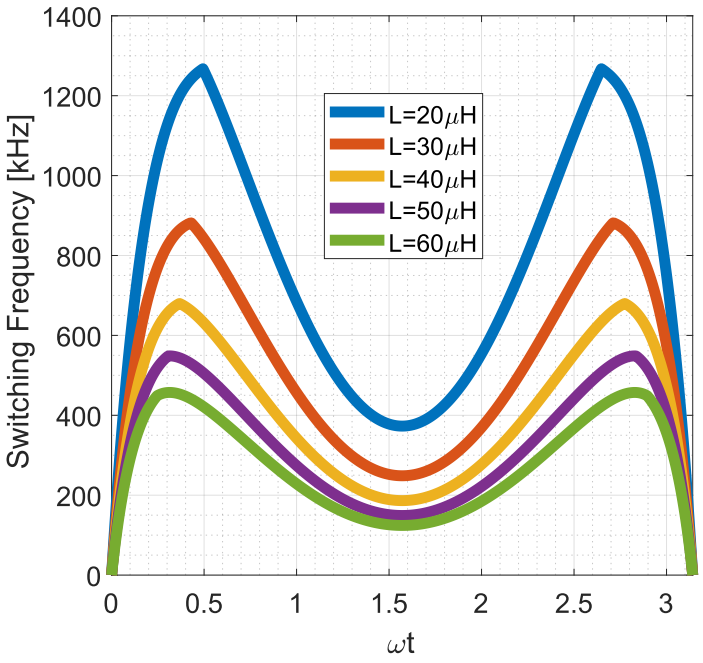
The main objective of the inductor design is to select the optimal inductance value, number of turns and core type that would yield the lowest converter loss and high reliability. The derived magnetic loss model previously presented in Chapter 4 is used in this optimization algorithm. The core geometry is constrained to EI38 and Ferroxcube high-frequency 3F4 and

Table 7.3: Commercial GaN Device Parameters

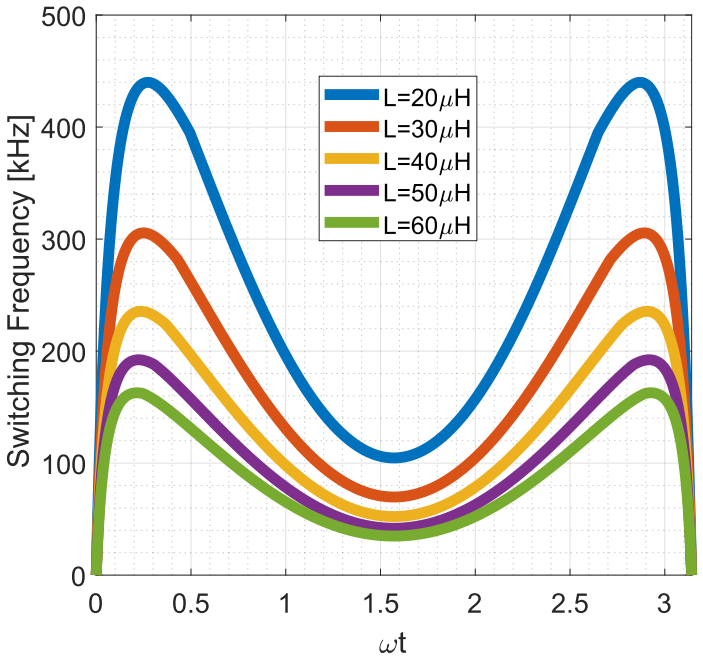
GaN Device Characteristics						
Manufacturer	Part Number	Voltage (V)	Current (A)	$R_{ds,on}$ (mΩ)	C_{oss} (nF)	Q_g (nC)
GaN System	GS-065-004	650	4	570	7	0.8
GaN System	GS-065-008	650	8	285	14	1.5
GaN System	GS-065-011	650	11	190	20	2
GaN System	GS66504B	650	15	130	31	3.3
GaN System	GS66506T	650	22.5	90	49	4.5
GaN System	GS66508T	650	30	63	65	6.1
GaN System	GS66516T	650	60	32	126	14.2
Infineon	IGT60R190D1	600	12.5	190	28	3.2
Infineon	IGLD60R070D1	600	15	70	72	5.8
Infineon	IGT60R070D1	600	31	70	72	5.8

Table 7.4: Commercial MOSFET Device Parameters

MOSFET Device Characteristics						
Manufacturer	Part Number	Voltage (V)	Current (C)	$R_{ds,on}$ (mΩ)	C_{oss} (nF)	Q_g (nC)
Infineon	IPT60R022S7	600	23	22	89	150



(a)



(b)

Figure 7.7: Switching frequency f_s for a varied set of inductances in a unipolar switched BCM inverter during the positive half-line cycle for (a) 500 W output power and (b) 2 kW output power.

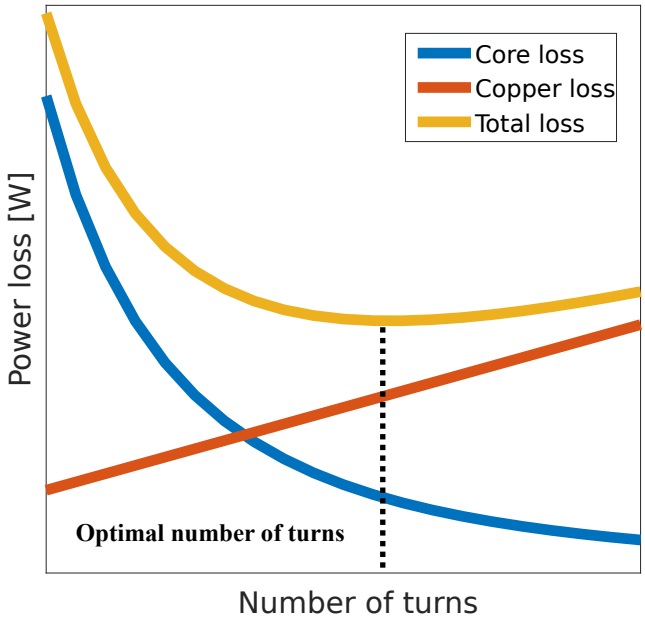


Figure 7.8: Inductor design showing the relationship between core and copper loss versus number of turns.

3F36 core materials. Fig. 7.8 shows the relationship between the copper and core loss of the inductor for a given number of turns. As shown in the figure, the core loss decreases with an increased number of turns, while in contrast, the winding loss increases. The optimal number of turns is determined by the point where the total inductor loss including both core and copper loss is minimal. This process guarantees the optimal inductor design for a selected inductance, core geometry material and type.

7.3.4 Phase Allocation

As previously described, each module is a soft switched half bridge using DCPM control and doing APF or inverter depending on the power requirements. The DHA phase allocation optimization is characterized by the phase distribution that would yield the lowest converter loss for a given number of phases. For n number of modules, a search algorithm loops through the total number of phases and computes the losses for each possible allocation, at each point in the line cycle. In the case of non-DHA, the optimization determines the number of phases allocated for inverter mode (n_{inv}) while the remaining phases perform APF operation (n_{apf}). The allocation is static and does not change throughout the line cycle.

For a basic operation of the converter, a minimum of two phases ($n = 2$) have to be operational at all times, one phase dedicated to the line frequency inverter operation while the other performs active power filtering. The minimum number of modules for the DHA and non-DHA to operate properly represents the traditional full-bridge configuration as shown in Fig. 7.5. Regardless of the topology, there is a half-bridge module operating at line cycle frequency (LF) used as the return phase leg. Since all the phases are identical and can shift operations, module shedding can be implemented as well.

7.4 LCOE Optimization Evaluation

To compute the LCOE optimization, the PV system cost parameters are first characterized. Table 7.5 summarizes the cost parameters such as annual inflation rate g, discount rate d used in the LCOE calculation. This cost is based on the current market rate of components provided by the manufacturer and data from the NREL SAM model. The current PV cost

per capacity is estimated using the Q1 2020 U.S Solar PV and energy storage cost benchmark reported in [1].

The cost of parts C_{parts} here is an estimate of the cost of the inductor, auxiliary components and manufacturing cost per module. It does not include the cost of power switches (i.e. GaNFET, MOSFET) and APF capacitors which are based on the market rate for bulk components pricing provided by electronic sales websites such as Digikey or Mouser. Fig. 7.9 shows the current market cost data and model of GaN-Systems 650 V devices vs on-resistance. As expected, the cost of the device is proportional to its on-resistance. Although this cost model will vary with the different device manufacturers, the trend will relatively be the same. The Si-MOSFET device has been limited to the best in class Infineon CoolMOS 600V/22mΩ (IPT60R022S7) device given its superior on-resistance performance in the 600 V Si-MOSFET category. Its cost estimate is straightforward and given by the present bulk market price of $8.00.

From this, the cost of individual DHA or multi-phase non-DHA module C_{mod} can be calculated. Furthermore, the analysis does not account for repairs; instead, it assumes a present value of the financial opportunity cost of maintenance C_m of 100.00 \$/kW$_{dc}$ related to module failure. The yearly PV module degradation coefficient δ is 0.8% [151].

With the cost parameters defined, the genetic algorithm (ga) function available in the MATLAB global optimization toolbox is used in combination with the phase allocation algorithm in order to compute the combination of device type, inductance, number of turns, material, ZVS current and configuration yielding the lowest LCOE with a minimum 50 years B_{10} lifetime and a peak efficiency of 97%. The obtained optimal design variables for all three inverter architecture is summarized in Table 7.6

For the specific components and financial characteristics considered in this analysis, the output LCOE for both DHA and non-DHA is shown in Fig. 7.10a. The optimal number of modules when using DHA is when $n = 4$, which yields an LCOE of 2.44 ¢/KWh. On the other hand, the non-DHA design yielded an LCOE of 3.11 ¢/KWh using an optimal number of 7 modules. Increasing the number of phases past 4 in the case of the DHA, and 7 in the case of non-DHA as the power level is held constant (2 kW) yields overall system lifetimes

Table 7.5: Cost Parameters of The Inverter

Parameter	Label	Value
Cost of parts per module	(C_{parts})	\$ 95.00
Film Cap. Cost per unit Capacitance	(C_{cap})	9 ¢/ µF
PV Cost per Capacity	(C_{pv})	2.46 \$/W_{dc}
Cost of Maintenance	(C_m)	100.00 \$/kW_{dc}
Inflation Rate	(g)	5%
Discount Rate	(d)	3%

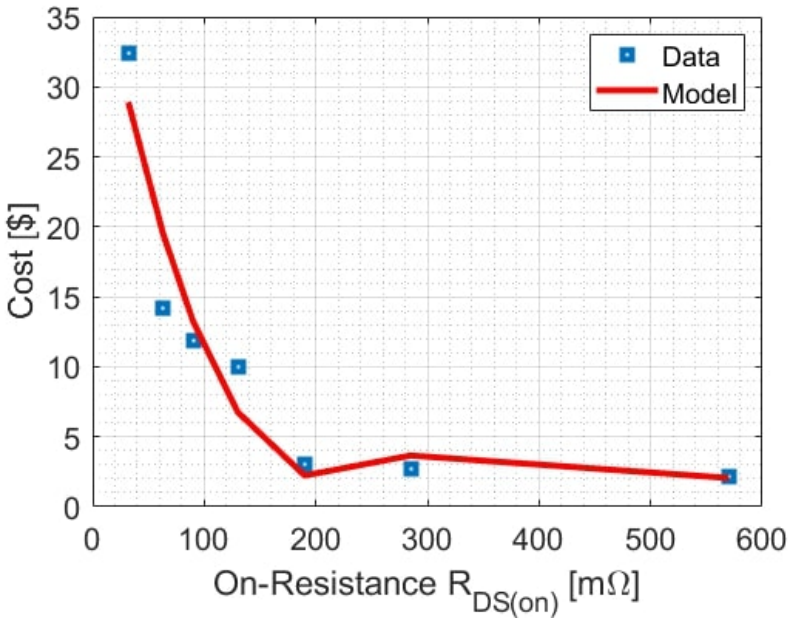
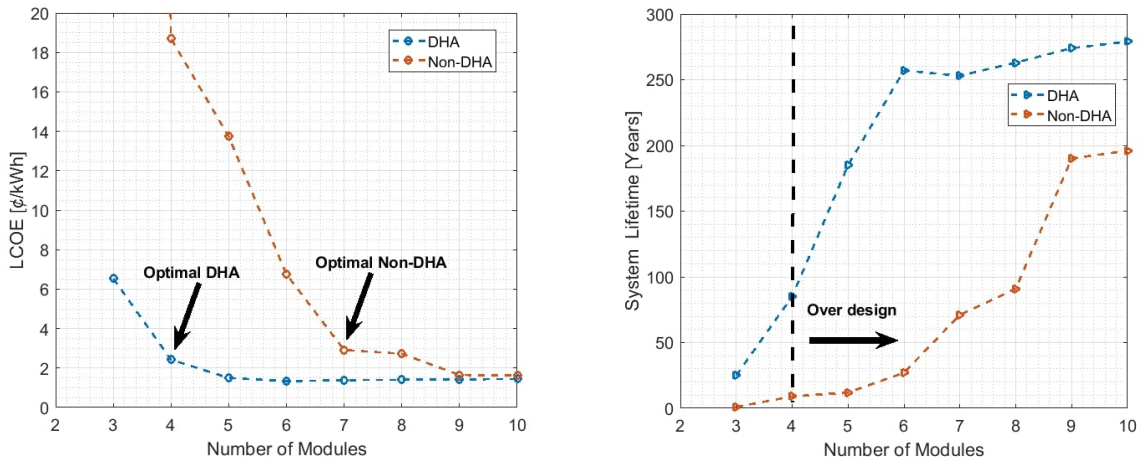


Figure 7.9: GaN cost model for 650V GaN System GaN devices.

Table 7.6: Optimal Design Variables For Inverter Based on LCOE

Parameter	DHA	Non-DHA	Full-Bridge
Number of module (n)	4	7	2
Allocation type	Dynamic	Static	Static
HF device type	GS66508T	GS66508T	GS66506T
HF device configuration	Single(1x)	Single(1x)	Parallel(2x)
LF device type	IPT60R022S7	IPT60R022S7	IPT60R022S7
LF device configuration	Parallel(2x)	Parallel(2x)	Parallel(2x)
Inductance (μH)	64	64	12
Number of turns	8	8	4
Core Geometry	EI38	EI38	EI38
Core Material	3F36	3F36	3F36
ZVS Current (A)	0.5	0.5	2.5
LCOE (¢/KWh)	2.44	3.11	21



(a) **(b)**

Figure 7.10: Analytical (a) LCOE and (b) Lifetime of the system as the number of modules vary.

that are well beyond the target design of 50 years as illustrated in Fig. 7.10b resulting in a diminishing return on the LCOE.

7.4.1 Reliability

The B_{10} lifetime evaluation for all three converters is provided in Table 7.7. The DHA design with 4 modules yielded the lowest LCOE of 2.44 ¢/KWh with the highest B_{10} lifetime of 77 years. The optimal non-DHA requires 7 modules to reach an LCOE of 3.51 ¢/kWh with 66 years lifetime. The FB architecture has the highest LCOE of 21 ¢/kWh due to its short lifetime of 8.5 years. Fig. 7.11 shows the unreliability waveform of all three inverter architectures with their B_{10} lifetime. The lifetime performance of the GaN-Based inverter is significantly improved when using DHA in comparison to non-DHA static allocation and in the case of the APF-based FB architecture. Although the FB design uses a more reliable film capacitor, its lifetime performance is similar to that of full-bridge architecture using an electrolytic capacitor because of the GaN device.

7.4.2 Efficiency

The efficiency results are summarized in Table 7.8, and Fig. 7.12 shows the efficiency sweep comparison between all three designs. The optimal design for both the DHA and non-DHA inverter architecture yields approximately the same CEC efficiency of 97%. Their power stage uses GS66508T, 650V/63mΩ from GaN-Systems. The lower efficiency of the DHA in comparison to the non-DHA is due to the additional conduction losses introduced by the extra switches in the circuit. The optimal FB topology uses 2 phases with paralleled GaN-devices (GS66506T, 650V/90mΩ). Although the FB architecture yields the lowest efficiency in comparison to the other two topologies; it has the smallest cost and complexity among all three designs. This shows why the FB has been the topology of choice for single-phase string PV inverters. It is simple and less expensive to implement. However, it is not the most reliable and cost-effective when considering system lifetime cost.

Table 7.7: Lifetime Evaluation Results

Parameter	Label	DHA	Non-DHA	FB
Allocation Type		Dynamic	Static	Static
Number of modules	(n)	4	7	2
B_{10} Lifetime	(Years)	77	66	8.5

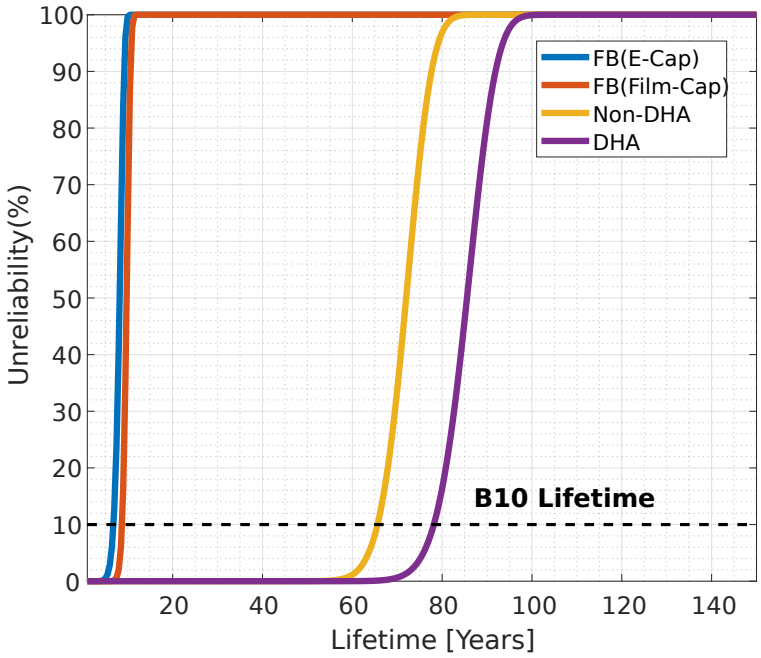


Figure 7.11: Unreliability function of proposed DHA with 4-modules ($n = 4$), non-DHA with 7-modules ($n = 7$) and a traditional 2 modules ($n = 2$) Full-bridge inverter architecture with an Electrolytic and Film Cap showing B_{10} lifetime.

Table 7.8: Efficiency Results

Parameter	Label	DHA	Non-DHA	FB
Allocation Type		Dynamic	Static	Static
Number of modules	(n)	4	7	2
CEC Efficiency η	(%)	97.63	97.73	97.03

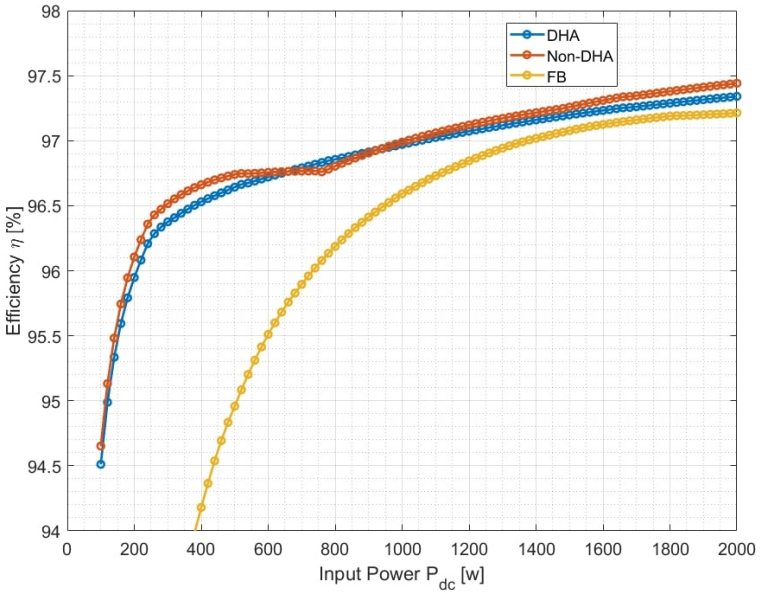


Figure 7.12: Analytical efficiency comparison between the optimal design of DHA, non-DHA and traditional Full-Bridge inverter.

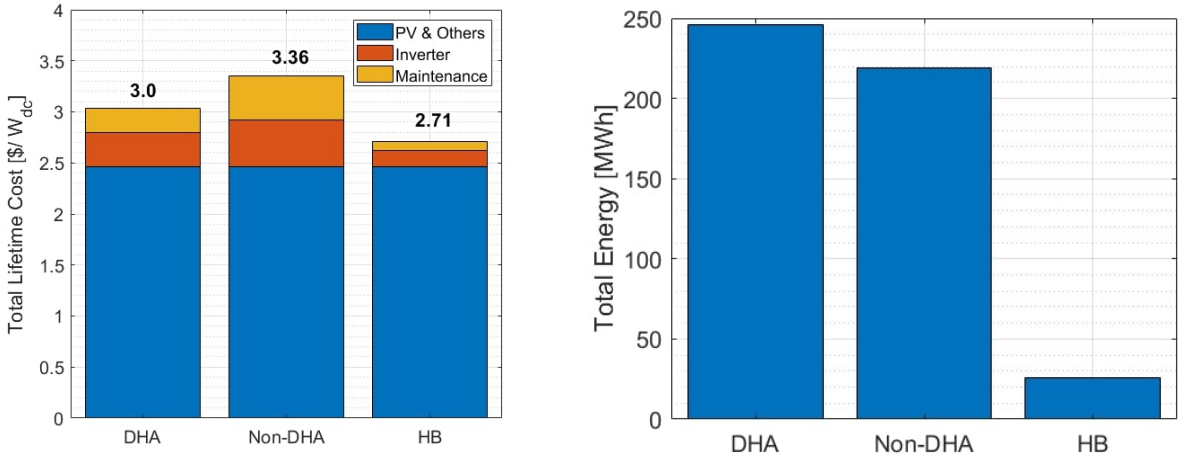
7.4.3 Cost and Energy Production

The initial cost of the inverters is given in Table 7.9. As expected, the non-DHA design with 7 modules ($n = 7$) has the highest inverter initial cost of 0.46 \$/W$_{dc}$ amongst all three designs. The full-bridge architecture has the lowest cost among all three designs, but the highest LCOE. Multiphase design whether doing DHA or non-DHA helps to lower the current stress on the GaN power device inherently helping to increase the overall lifetime and efficiency of the system. On the other hand, it does contribute to an increase in the initial cost of the system as illustrated in Fig. 7.13a. The initial cost of the inverter using DHA is around 0.34 \$/W_{dc}, but its extended lifetime contributes to longer system operation in the field resulting in more energy yield depicted in Fig. 7.13b. That explains why the traditional full-bridge has a higher LCOE of 21¢/KWh despite its lowest initial cost of 0.16 \$/W_{dc} amongst all three inverters. The lifetime energy yield of the system is constrained by the limited lifetime of the inverter.

In the case of the DHA inverter design, Fig. 7.14a shows the yearly energy output and number of modules over the lifetime of the system. For over 50 years of the system operation, 100% of the components will operate with no expected failure, degradation is the main contributor to energy decline in the system. After the 70th year, the probability of failure of the DHA starts to slightly increase causing an additional decrease in the energy output with every associated module failure in the system. The output PV energy processed is proportional to the number of operational HF modules in the DHA inverter. For instance, in the 4-module DHA architecture, if one module fails, 75% of the energy is still processed through the remaining phases. Only 25% of the energy output is lost in this case in contrast with a traditional system where a single module failure will result in a complete loss of energy output. The DHA reaches the end of its life when there are fewer than 2 modules that are operational. Although there are no repairs in this model, Fig. 7.14b shows the maintenance cost associated with running the system and a module failure. This cost is distributed throughout the lifetime of the inverter and reaches its maximum when the inverter is at the end of its operation.

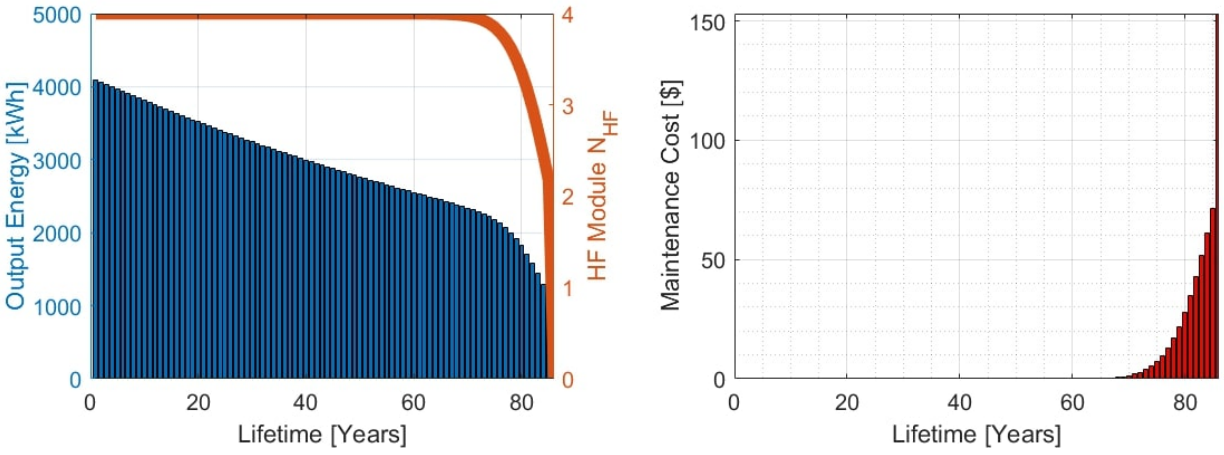
Table 7.9: Initial Cost Results

Parameter	Label	DHA	Non-DHA	FB
Allocation Type		Dynamic	Static	Static
Number of modules	(n)	4	7	2
Initial Cost	$(\$/W_{dc})$	0.34	0.46	0.16



(a) **(b)**

Figure 7.13: Analytical total lifetime (a) Cost and (b) Energy output of proposed DHA with 4 modules, non-DHA with 7 modules and a traditional 2 modules full-bridge inverter architecture.



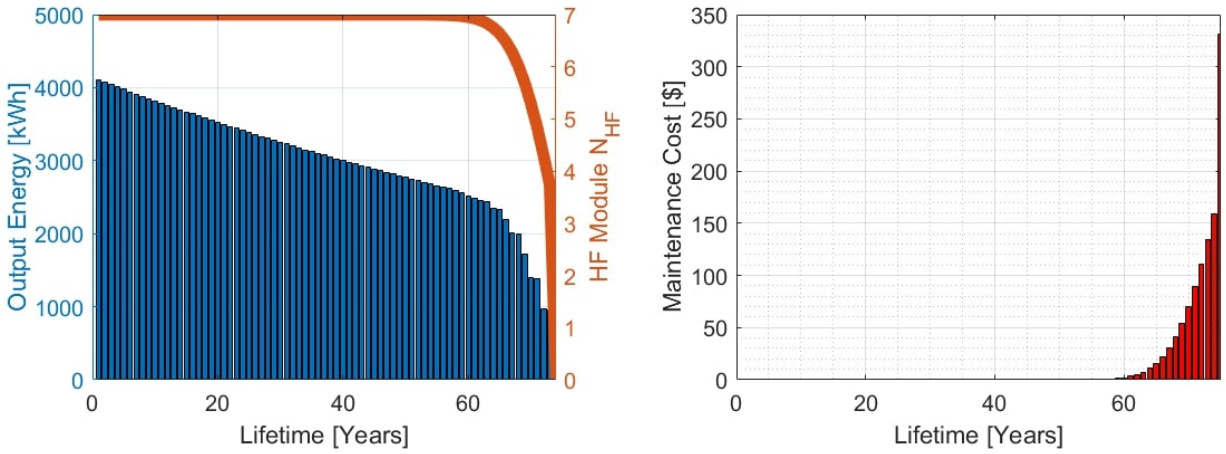
(a) **(b)**

Figure 7.14: Analytical lifetime (a) Energy output and (b) Cost distribution of PV system in the case of DHA inverter using dynamic allocation.

The yearly energy output and cost for a non-DHA inverter with static allocation are illustrated in Fig. 7.15. Similar to the DHA case, the early non-DHA energy output is characterized by panel degradation for the first 60 years followed by significant energy decrease due to module failure. In contrast to the DHA, whenever there is a failure, the energy loss is derated by the ratio of the number of modules doing inverter or APF depending on which module failed. For example, when considering a 4-module multiphase system with 2 modules each allocated for inverter and apf, whenever there is a single module failure, the energy output is derated by 50%. That's 25% more than what is expected in the case of the DHA system. In this case, the inverter reaches the end of its life when all the modules allocated for each operation have failed. In addition, the yearly maintenance cost distribution is shown in Fig. 7.15b. The difference in both cost outputs for a given year is due to the difference in their unreliability function.

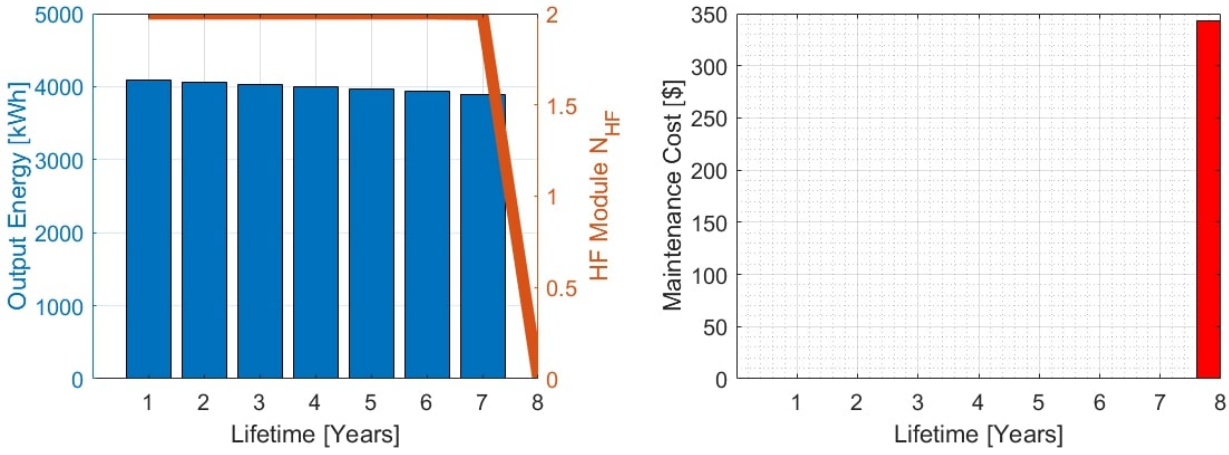
In the case of a full-Bridge architecture, the yearly energy and cost output is depicted in Fig. 7.16. From the unreliability function of the h-bridge topology, the inverter reaches the end of its lifetime when one of the modules fails. At that point, the output energy of the system is zero. The associated maintenance cost of the system illustrated in Fig. 7.16b is minimal in comparison to the other design. This is due to the short lifetime of this system and the fact that repair scenarios are not part of this design. The single maintenance cost shown in the $8th$ year, is the opportunity cost associated with the total system failure.

In this analysis, the power level has been assumed constant at 2 kW and the DHA inverter architecture using 4 modules yielded the overall best performance. In addition, the modular nature of the DHA architecture facilitates the scaling of the system depending on the PV system size while achieving the same performance. From this analysis, it can also be deduced that 500 W is the optimal power level for a single module. As a result, a DHA architecture with 4 modules is used for a 2 kW system. The linear relationship between the power level and the number of phases suggests that the PV system and inverter power can be scaled up with the number of modules while maintaining the same level of performance. As presented in Fig. 7.17, as the number of modules and power increases up to 5 kW, the expected LCOE only varies within 3% up to 12 modules. At 6 kW, the LCOE increases substantially due to the drop in reliability of the MOSFET devices. This is illustrated in the unreliability plot of



(a) (b)

Figure 7.15: Analytical lifetime (a) Energy output and (b) Cost distribution of PV system in the case of non-DHA inverter using static allocation.



(a) (b)

Figure 7.16: Analytical lifetime (a) Energy output and (b) Cost distribution of PV system in the case of the Full-bridge inverter.

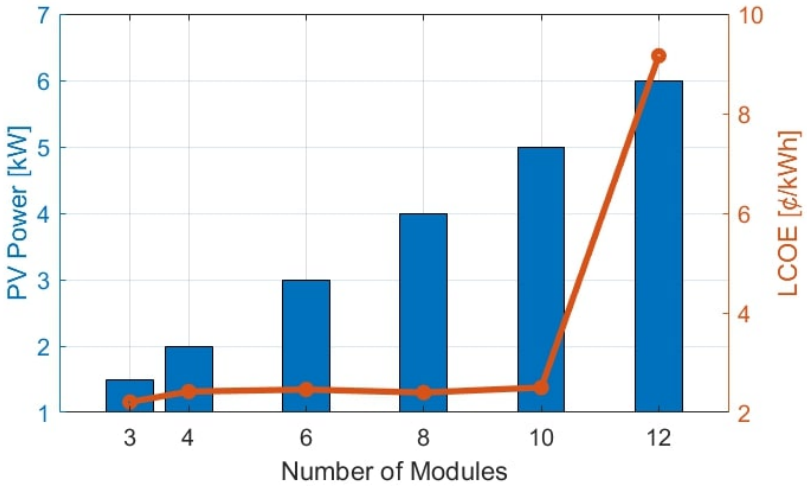


Figure 7.17: Graph showing how the number of modules scale with the rated system with the corresponding LCOE.

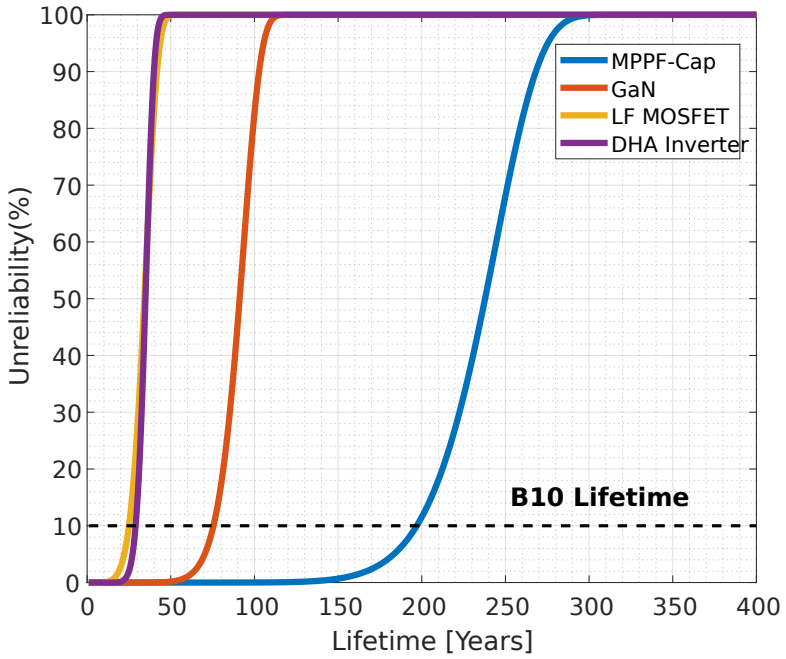


Figure 7.18: Component-level unreliability function showing B_{10} lifetime of MPPF-Capacitor, GaN, MOSFET components and converter-level unreliability of DHA inverter with 12 modules for a 6 kW PV system.

the components and converter level of 12 modules DHA shown in Fig. 7.18. At a 6 kW power level, the MOSFET device used in the line frequency module is the least reliable component in the system, hindering the reliability of the entire inverter.

7.5 Summary

In this chapter, the design analysis, optimization and implementation of the GaN-based single-phase inverter using DHA has been carried out and compared with a multiphase inverter with static allocation (non-DHA) and the traditional full-bridge inverter architecture. When considering only the efficiency performance metric, the DHA performance is comparable to that of non-DHA and the Full-bridge inverter. The DHA could achieve better efficiency performance with improvements to the way the inverter and APF switches are implemented in this design. However, when designing for high reliability and efficiency, the DHA can achieve a lifetime of well over 50 years outperforming the lifetime of the other two designs. This significantly increases the lifetime energy yield of the PV systems while reducing maintenance costs. As a result, the DHA inverter would yield the lowest LCOE over a 50-year lifetime of the PV system making it a cost-effective option. In addition, its modular structure makes it simple to scale up with an increased PV power rating.

Chapter 8

DHA Control Design and Implementation

In the previous chapter, the optimal design of the DHA inverter with dynamic allocation and how it compares with the traditional multi-phase non-DHA and the full-bridge inverter with static allocation has been carried out using the LCOE-driven design optimization. In this chapter, the presented optimization is used to derive a hardware prototype of the DHA inverter that is built and tested to validate its efficiency, steady state and dynamic model. The same hardware is then used to implement the non-DHA inverter and show how its performance compares with the DHA inverter operation. The system-level controller design and implementation of the DHA inverter is also presented in this chapter. The module-level control regulates the inductor current and has been previously illustrated in Chapter 5.

8.1 Hardware Prototype Design

To validate the DHA power loss model, steady state and dynamic operation, the LCOE-driven design optimization developed in Chapter 7 is used to derive the optimal DHA hardware prototype with a set of new constraints due to hardware limitations and components market availability. The silicon MOSFET device has been changed to the 700V/33mΩ CoolMOS (IPT65R033G7) device from Infineon and the line-frequency module device configuration has also been limited to a single device configuration instead of a

parallel configuration. Furthermore, the inductor design is changed to the ETD44 core type, the Ferroxcube high-frequency 3F4 and 3F3 material, and Litz wire for the winding. To guarantee full ZVS operation at all times and a safe operation of the hardware, a 1.5 A ZVS current is used. The obtained DHA prototype design variables including the inductor design using the aforementioned set of constraints are summarized in Table 8.1.

To validate the steady state and dynamic performance of the DHA inverter and how it compares to the non-DHA operation, the DHA inverter prototype hardware with 4 modules is used for both operations. The analytical lifetime, efficiency and LCOE have been computed for both DHA and non-DHA inverters using the same hardware prototype design and the results are summarized in Table 8.2. As expected, the DHA has the lowest LCOE with an expected lifetime of 41 years and an efficiency of 97.10% in comparison to the non-DHA which yields an expected lifetime of 8 years and an efficiency of 96.92%. Next, the hardware prototype of the DHA module is built and tested starting with the control implementation.

8.2 Control Implementation

The schematic of the optimal DHA inverter with the overall control strategy is shown in Fig. 8.1. The system level controller regulates both the magnitude of the inverter ac output voltage (v_{ac}) and the dc-link input current ripple (I_{dc}). The controller also dispatches the modules during the line cycle based on the phase allocation algorithm.

8.2.1 Output AC Voltage-Loop Controller Design

This controller is designed to regulate the peak ac output voltage. First, the ac voltage is sensed and converted into the dq frame through Park transformation. Then a phase locked loop (PLL) is used to derive the phase angle θ and the voltage magnitude V_m. To design the compensator for the voltage loop control, the transfer function of the system is derived. Each module of the BCM inverter is modeled. Thus, during each switching cycle, the average inductor current and capacitor voltage are

Table 8.1: Optimal Design Variables For Inverter Based on LCOE

Parameter	Label	DHA
Number of module	(n)	4
Allocation type		Dynamic
HF device type		GS66508T GaN Systems
LF device type		IPT65R033G7 CoolMOS Infineon
ZVS Current	(A)	1.5
Inductance	(μH)	63
Number of turns		29
Core Geometry		ETD44
Core Material		3F3
Litz Wire		650/44
LCOE	(¢/KWh)	4.36

Table 8.2: Analytical Lifetime, Efficiency and LCOE Evaluation

Parameter	Label	DHA	Non-DHA
Allocation Type		Dynamic	Static
Number of modules	(n)	4	4
System Lifetime	(Years)	41	8
Efficiency η	(%)	97.10	96.92
LCOE	(¢/KWh)	4.36	19.25

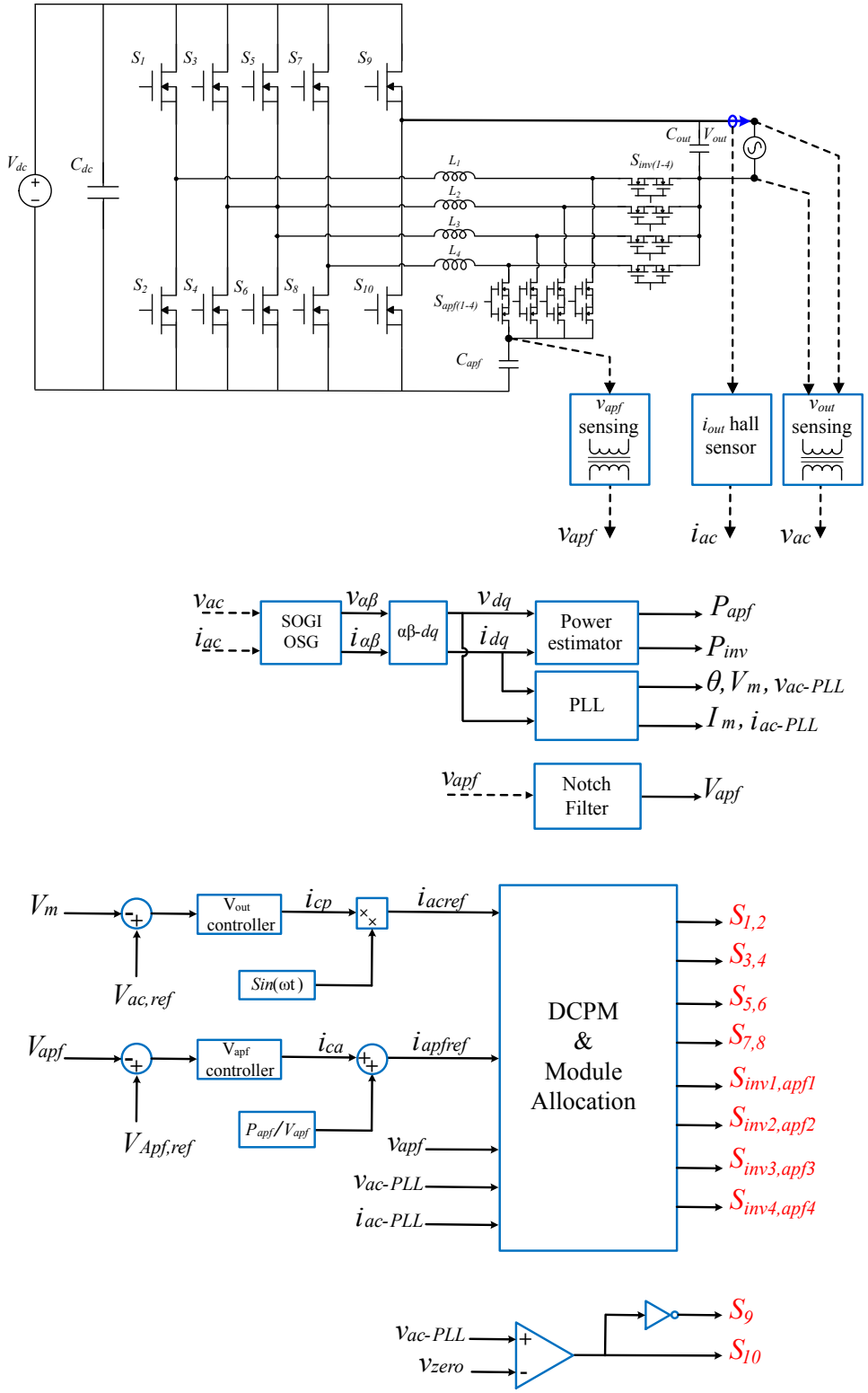


Figure 8.1: Control strategy for the optimal DHA inverter with four modules.

$$\begin{cases} L\frac{di_L}{dt} = d \cdot (v_{dc} - v_{out}) - d' \cdot v_{out} \\ C_{out}\frac{dv_{out}}{dt} = (i_L - v_{out}) \end{cases} \tag{8.1}$$

The average inductor current is simplified as half of the peak inductor current and inserted in 8.1 resulting in

$$\left\langle i_L \right\rangle = \frac{1}{2} i_{L,pk} \tag{8.2}$$

perturbation and linearization of 8.1 yields the small signal model

$$\begin{cases} \frac{1}{2}L\frac{d\hat{i}_{L,pk}}{dt} = D\hat{v}_{dc} - \hat{v}_{out} + \hat{d}V_{dc} \\ C_{out}\frac{d\hat{v}_{out}}{dt} = \frac{1}{2}\hat{i}_{L,pk} - \frac{\hat{v}_{out}}{R} \end{cases} \tag{8.3}$$

which is equivalent in the s domain as

$$\begin{cases} \frac{1}{2}sL\hat{i}_{L,pk} = D\hat{v}_{dc} - \hat{v}_{out} + \hat{d}V_{dc} \\ sC_{out}\hat{v}_{out} = \frac{1}{2}\hat{i}_{L,pk} - \frac{\hat{v}_{out}}{R} \end{cases} \tag{8.4}$$

rearranging and solving 8.4 for the output voltage as a function of the peak inductor current yields

$$\hat{v}_{out} = \frac{1}{2}\frac{R}{(1 + RC_{out}s)}\hat{i}_{L,pk} \tag{8.5}$$

The controlled inductor current to output transfer function $G_{vi,ac}$ for the half-bridge BCM modulated converter is

$$G_{vi,ac}(s) = \frac{\hat{v}_{out}}{\hat{i}_{Lpk}} = \frac{R}{2} \cdot \frac{1}{1 + RC_{out}s} \tag{8.6}$$

With the converter transfer function derived, the compensator for the output voltage control loop is designed to have a high gain at DC and a minimum phase margin of 80°. A PI compensator $G_{c1}(s)$ is used to achieve this goal. Fig. 8.2 shows the bode plot of the compensated loop gain $T_s(s)$ of the system. The obtained results yield a phase margin of

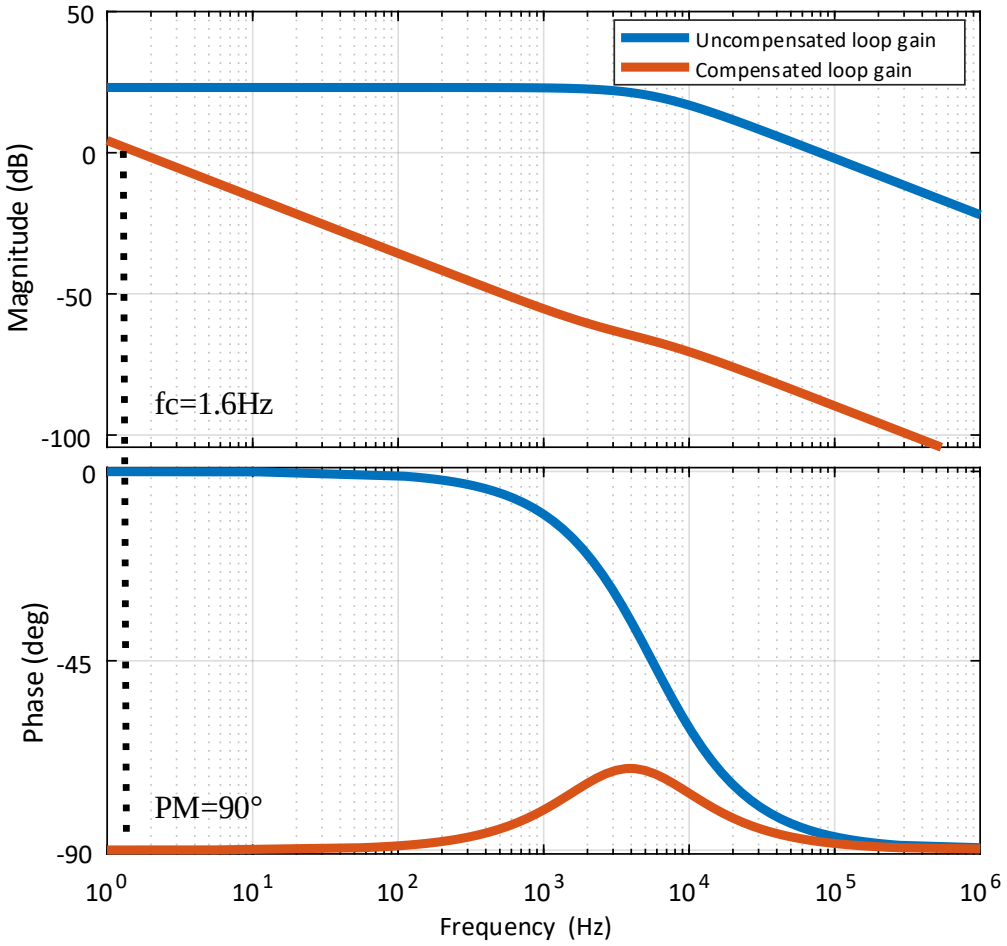


Figure 8.2: Bode diagram of the output voltage control loop.

90° with a bandwidth of 1.6 Hz. This control has been designed to have low bandwidth to avoid the impact of the double-line frequency ripple controller.

8.2.2 Double-line Frequency Ripple Current Filter Design

The objective of this controller is to regulate the 120 Hz component of the input dc-link current to zero while also controlling the average component of the APF capacitor voltage to 200 V. To accomplish this objective, a model-based controller is used. First, the derived voltage and current obtained in the *dq* frame are used to estimate the inverter power

$$P_{ac}(t) = P_{avg} + P_{apf}(t) = \frac{I_m V_m}{2} cos(\varphi) + \frac{I_m V_m}{2} cos(2\omega t + \varphi) \tag{8.7}$$

which consists of the average power component P_{avg} and the second harmonic component that corresponds to the APF power

$$P_{apf}(t) = \frac{I_m V_m}{2} cos(2\omega t + \varphi) \tag{8.8}$$

From 8.8, the second harmonic ripple current $I_{apf}(t)$ can be calculated in real-time by dividing the APF power $P_{apf}(t)$ with the sensed capacitor voltage $V_{apf}(t)$. The calculated APF current reference is given by

$$I_{apf}(t) = \frac{I_m V_m}{2V_{apf}(t)} cos(2\omega t + \varphi) \tag{8.9}$$

Next, the average model of the buck-type APF is used to derive the current-to-voltage transfer function in order to regulate the average component of the APF voltage. The transfer function from the controlled current to the APF voltage is

$$G_{vi,apf}(s) = \frac{\hat{v}_{apf}}{\hat{i}_L} = \frac{1}{C_{apf} s} \tag{8.10}$$

Similar to the output voltage controller design, a PI compensator $G_{c2}(s)$ is used to design the APF voltage control loop to have a high gain at dc and a minimum phase margin of 80°. The control loop also includes a 120 Hz digital notch filter that is used to filter out the second harmonic component of the sensed APF voltage. The resulting voltage is compared with the

average reference voltage $V_{apf,ref}$. The obtained magnitude and phase of the compensated loop gain are shown in Fig. 8.3. The design has a crossover frequency of 6 Hz and a phase margin of 88°.

8.3 Simulation Verification

8.3.1 Output Voltage and APF Voltage-Loop Controller

The average model of the BCM switched inverter with closed-loop control has been implemented and simulated in MATLAB Simulink to validate the performance of the ac output voltage and APF voltage controller. The K_p and K_i parameters of the PI controller for both control loops are summarized in Table 8.3. The obtained simulation waveforms including the output voltage (v_{out}), current (i_{out}), APF voltage (v_{apf}), and input dc-link current (I_{dc}) at full load are illustrated in Fig. 8.4. The output voltage is well regulated at 240 V_{rms} while the dc component of the APF voltage is regulated to approximately 200 V. The resulting second-harmonic ripple current on the input dc-link is approximately 500 mA which is 20% of the average dc link current.

8.3.2 Phase Allocation

The DHA phase allocation is derived based on the LCOE optimization algorithm previously discussed in Chapter 7 and then programmed into the DSP. The real-time calculation of the output and APF power is used to derive the corresponding module allocation. The LCOE-optimized phase allocations at different load conditions are depicted in Fig. 8.5. At 350 W load, as demonstrated in Fig. 8.5a there are only 2 modules that are operational, with module 1 allocated for inverter operation and module 2 for APF at all times. Modules 3 and 4 are OFF. It is important to note that module shedding is not shown in this analysis, but any of the 4 modules can be allocated in hardware at any time for both inverter or APF operations. The modules are also turned ON in ascending order depending on the load condition, starting from module 1 up to module 4. In the second scenario illustrated in

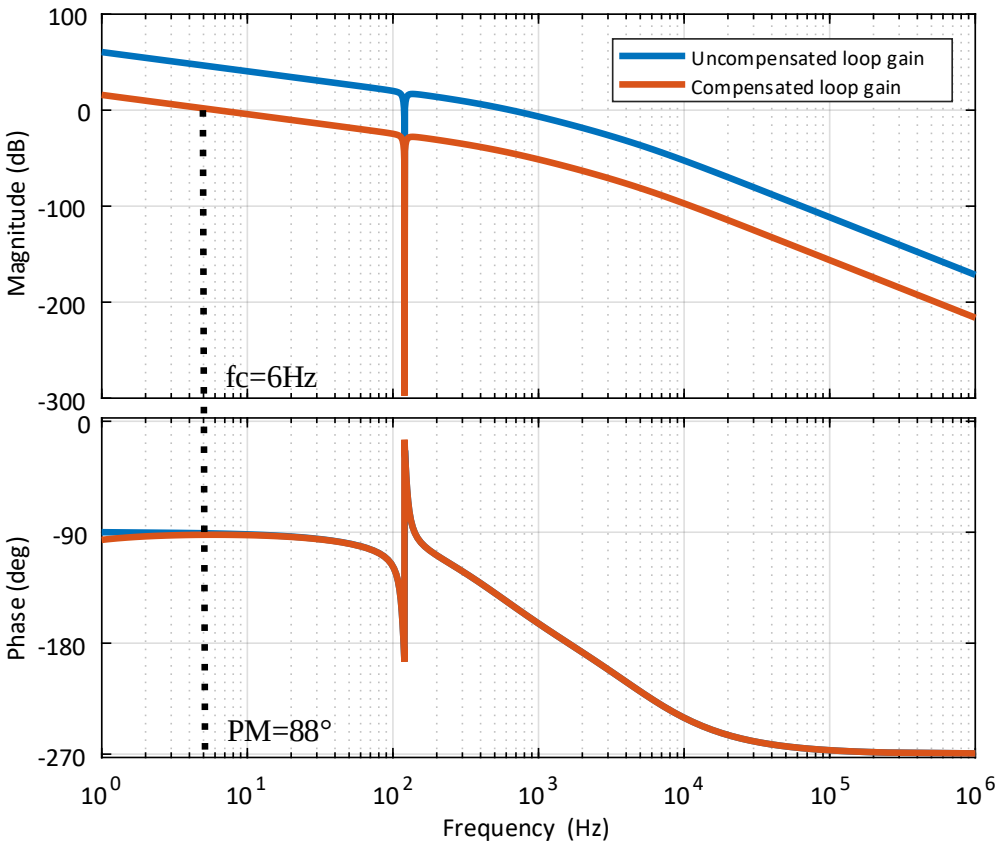


Figure 8.3: Bode diagram of the APF voltage control loop with a notch filter at 120 Hz.

Table 8.3: Controller Parameters

Parameter	Output Voltage	APF Voltage
K_p	$4.131e^{-5}$	$3.508e^{-3}$
K_i	0.7235	$2.393e^{-3}$

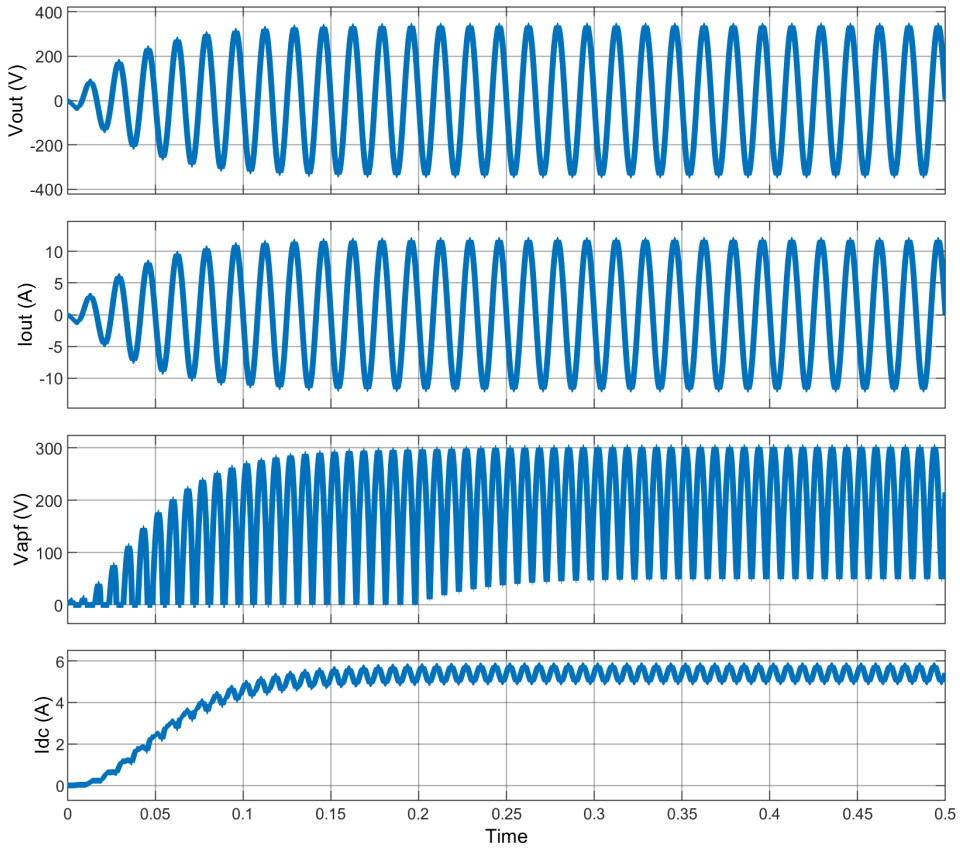
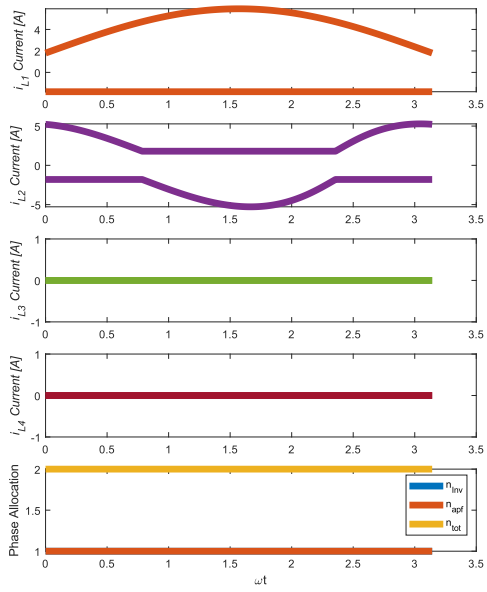
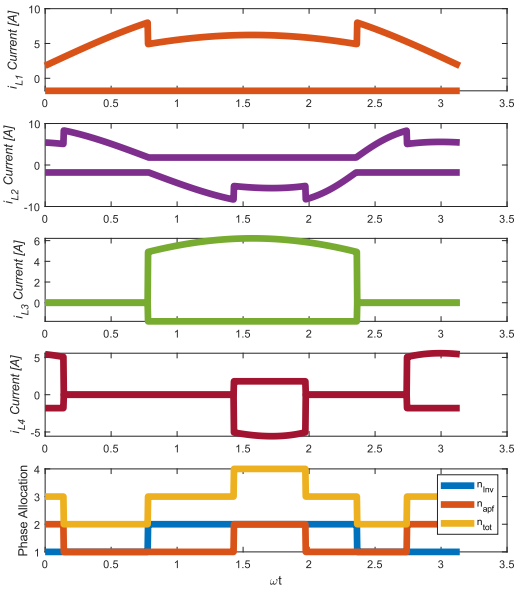


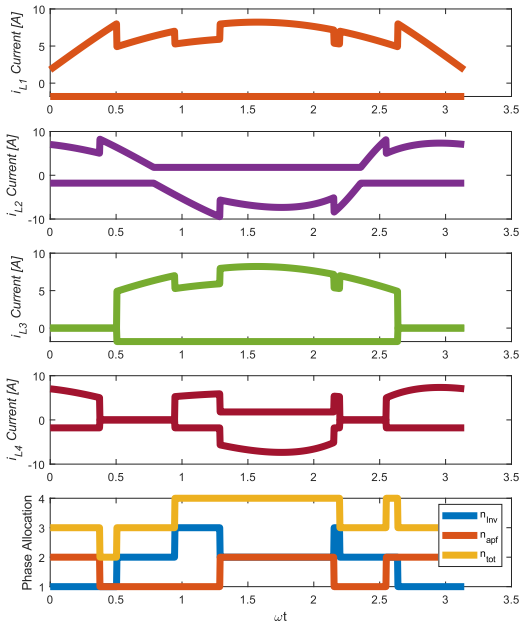
Figure 8.4: Simulation waveform of the closed loop control of DHA showing the regulated output voltage (v_{out}), output current (i_{out}), regulated APF voltage (v_{apf}) and input dc-link current (I_{dc}) at 2 kW full power.



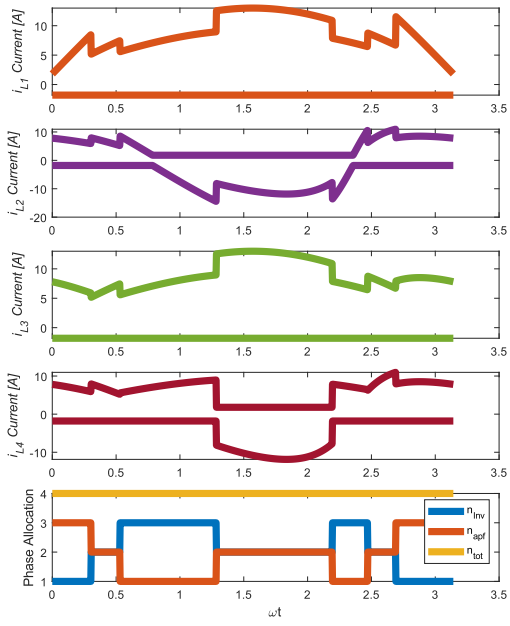
(a)



(b)



(c)



(d)

Figure 8.5: Expected phase allocation and inductor current envelope waveforms $i_{L1}, i_{L2}, i_{L3}, i_{L4}$ for all four modules at (a)350 W, (b)650 W, (c)1 kW and (d)2 kW operation point.

Fig. 8.5b, as the power increases to 650 W, the previous allocation is maintained; however, the 4th module now comes online to assist module 2 with APF operation during its expected peak current. All four modules are operational, with modules 3 and 4 turning ON and OFF at various times during the line cycle. In the third example depicted in Fig. 8.5c, the allocation becomes more intricate at 1 kW. There are a maximum of 3 modules allocated for inverter operation and 2 modules for APF operation at various times during the line cycle. Module 4 switches between inverter and APF operation. Finally, the allocation and inductor current at 2 kW operation is illustrated in Fig. 8.5d. All 4 modules are projected to be used in the allocation and ON at all times. In this case, module 1 is allocated for inverter and module 2 is allocated for APF. Modules 3 and 4 change between inverter and APF operation modes.

8.4 Hardware Prototype

An experimental prototype of the optimal DHA inverter with four modules has been built and tested up to 1 kW. Fig. 8.6 shows the hardware prototype, and Table 8.4 summarizes the components and parameters used in this implementation. The same hardware is used to test the performance of both the DHA and the non-DHA multi-phase inverter operation. The hardware consists of five daughterboards: four high-frequency modules ($n = 4$) and one low-frequency module for the current return phase. All the modules are connected to the main motherboard which has the APF capacitors, dc-link capacitor, power supply and all the sensing circuits. The power stage of the high-frequency module is illustrated in Fig. 8.7. Some 650V/63mΩ GS66508T devices from GaN-Systems are used to implement the power stage in addition to 700V/33mΩ CoolMOS devices from Infineon for the inverter and APF switches (S_{apf}, S_{inv}). The inductor is implemented using an ETD44 core and is mounted on the back of the high-frequency daughterboard as depicted in Fig. 8.7b. A 6 mΩ shunt resistor is used for sensing the inductor current on the high-frequency power module and the sensed inductor current is sent to the dual current programmed mode (DCPM) controller board through the SMA connector. A fixed ZVS current of 1.5 A has been chosen to ensure full ZVS and safe operation during the entire line cycle. The module power stage and DCPM controller board are depicted in Fig. 8.8. All the modules are connected to the motherboard

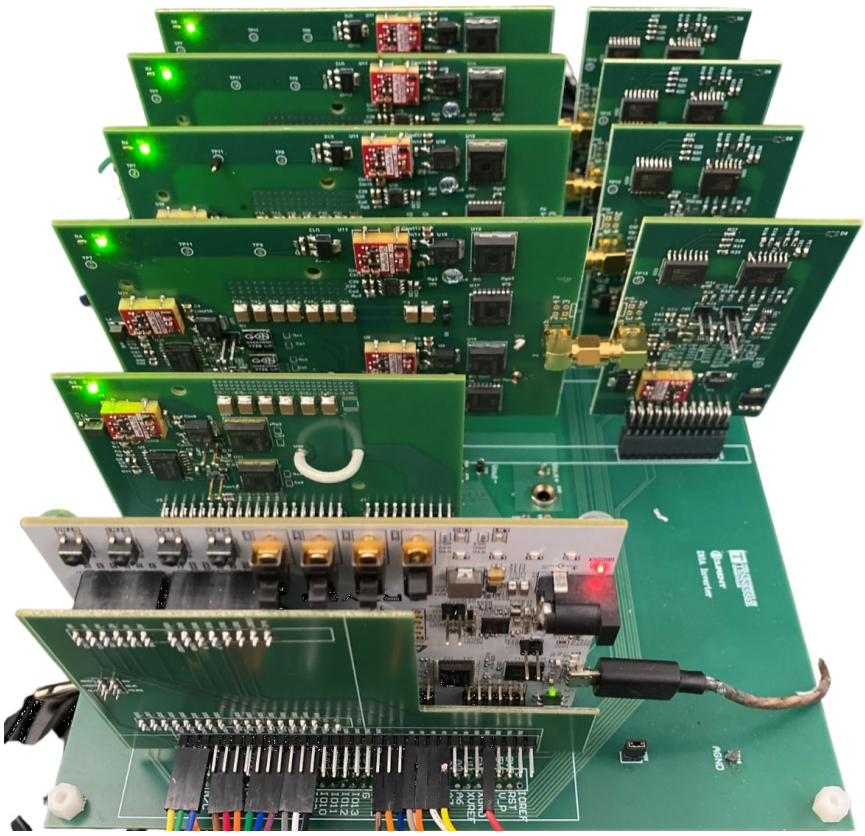
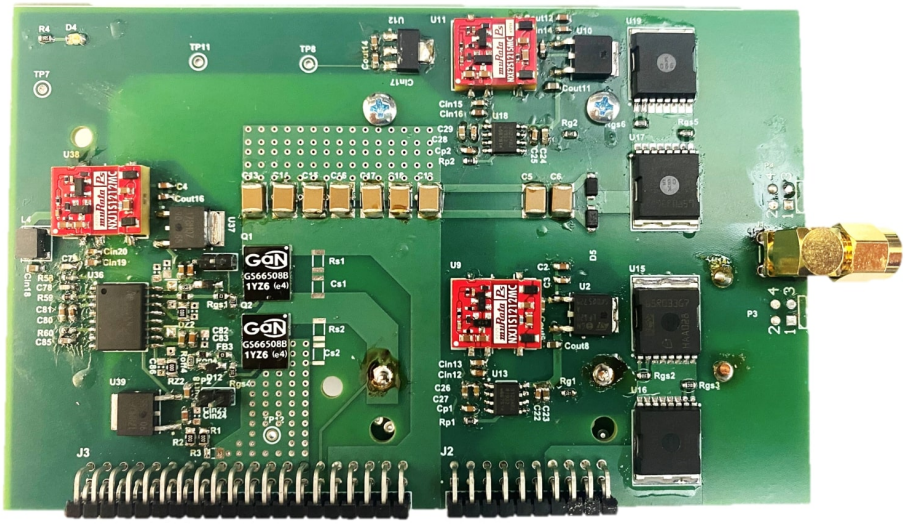


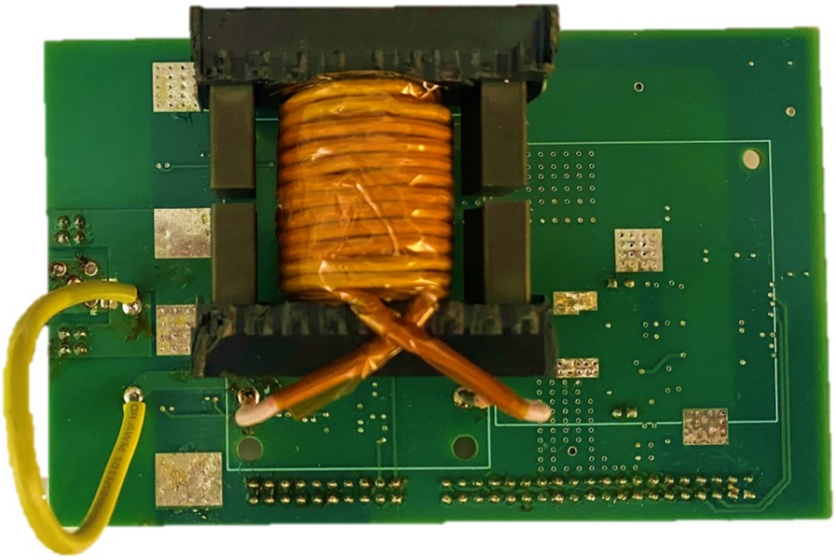
Figure 8.6: Optimal DHA inverter hardware prototype with 4 modules.

Table 8.4: Components and Parameters of prototype

Parameter	Value
Input voltage V_{dc}	400 V
Output voltage V_{out}	240 V/60 Hz
GaN Device	650V/63mΩ-GS66508T GaN Systems
MOSFET Device	700 V/33mΩ-IPT65R033G7 Infineon
APF Capacitor	5 x 30 μF, 700 V (MKP1847630354Y5)
Dc-link Capacitor	16 μF, 700 V (B32796E3166K)
Shunt Resistor R_{shunt}	6 mΩ
ZVS Current I_{zvs}	1.5 A
Inductance L_1, L_2, L_3, L_4	60 μH
Core Geometry	ETD44
Core Material	Ferroxcube 3F3
Wire	650/44 Litz
Switching Frequency	120 kHz - 500 kHz



(a)



(b)

Figure 8.7: DHA daughterboard depicting the power stage (a) front and (b) back with the planar inductor of the high-frequency module.

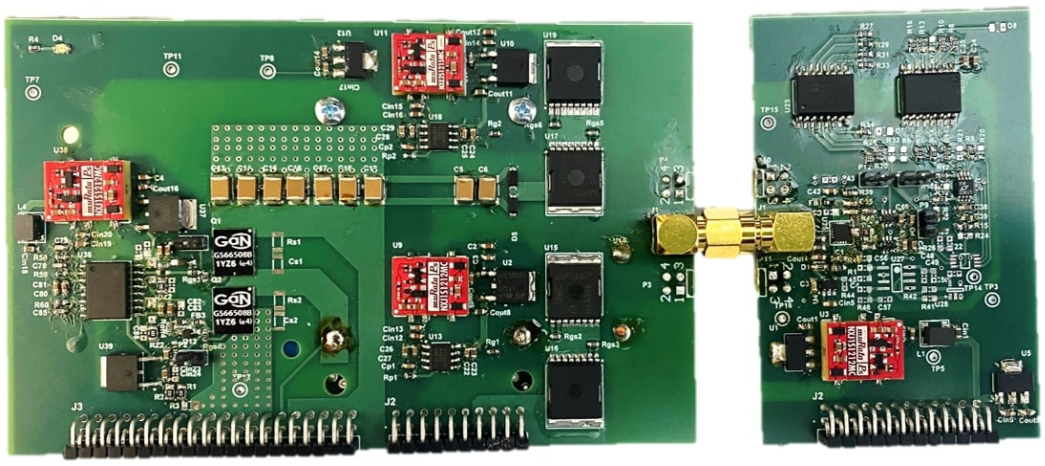


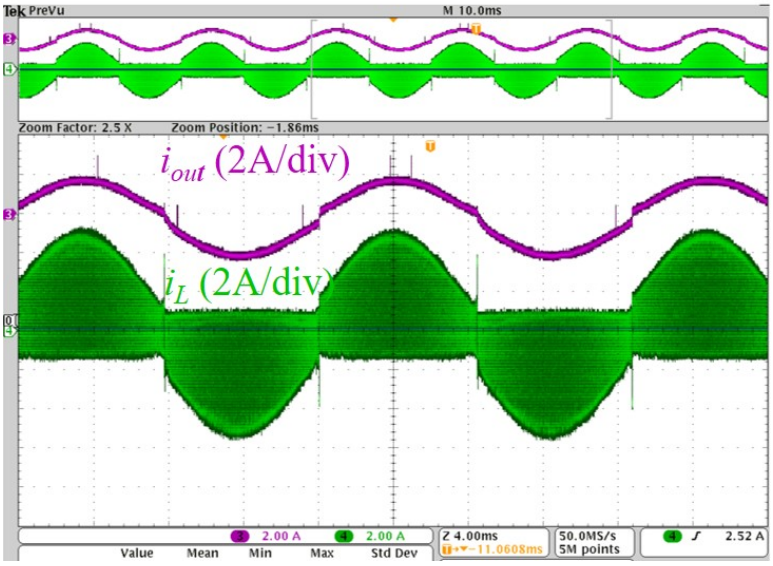
Figure 8.8: DHA module hardware prototype depicting both the power stage and the dual current programmed mode (DCPM) controller board connected through an SMA connector.

which has all the sensing circuitry including the input dc-link current, voltage, APF voltage, output current and voltage sensors. A Texas Instruments TMS320F28379D DSP launchpad is used to sample all the sensed signals at a rate of 50 kHz and to implement the system level controller including output voltage, APF voltage, input current regulation and phase allocation. The Arty S7-50 development board using Spartan 7 FPGA from XILINX is used to implement the local level module current control and the generation of the current references needed for the DCPM control. The converter efficiency, voltage and current THD are measured using the Tektronix PA1000 power analyzer.

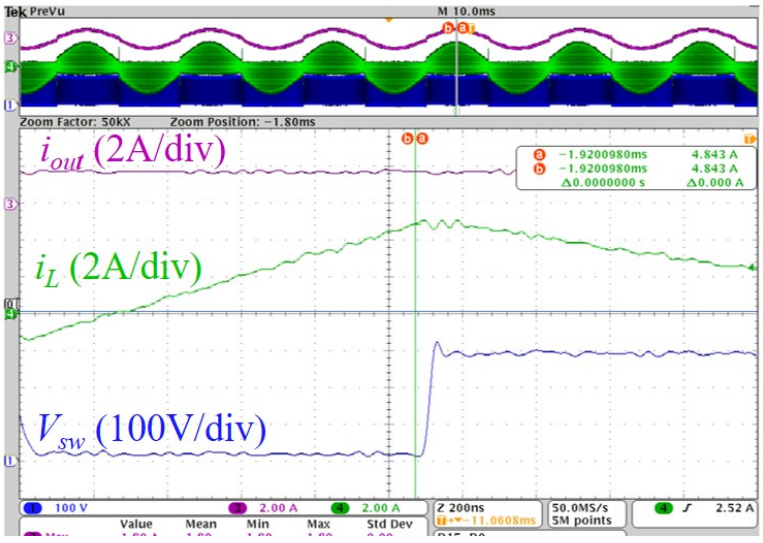
8.5 Experimental Verification

8.5.1 Propagation Delay Compensation

The choice of the shunt resistor (R_{shunt}) is integral to the performance of the dual current programmed mode controller (DCPM). In this design, the shunt resistor has been selected such that the effect of its parasitic inductance counteracts that of the time delay in the DCPM control loop. The measured propagation delay from the current control loop is approximately 100 ns, and the parasitic inductance of the shunt is about 1.2 nH. Thus, using design techniques discussed in Chapter 5, a shunt resistance of 6 mΩ is selected in this implementation through a parallel combination of two 12 mΩ sensing resistors. This setup reduces the parasitic inductance by half and together with the low sensing resistor value cancels out the effect of the propagation delay. Fig. 8.9a shows an example waveform of the inductor current (i_L) and output current (i_{out}) with the proposed compensation technique. For instance, during the positive half cycle, the inductor current is well regulated to a peak value of 5 A as depicted in the zoomed-in Fig. 8.9a. In contrast, when a 20 mΩ shunt resistor is used without compensation, there is an overshoot of the inductor current past its reference point by 500 mA resulting in a distortion of the output current. This is demonstrated in the results shown in Fig. 8.10a and in the zoomed-in waveform in Fig. 8.10b.

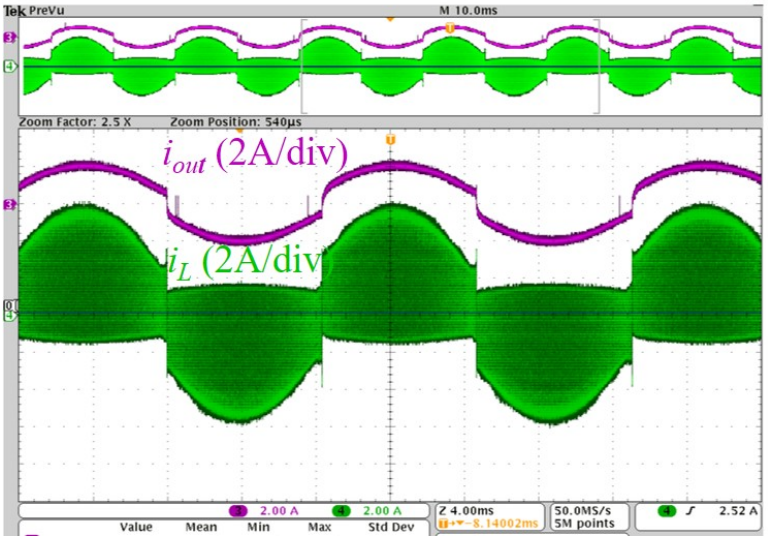


(a)

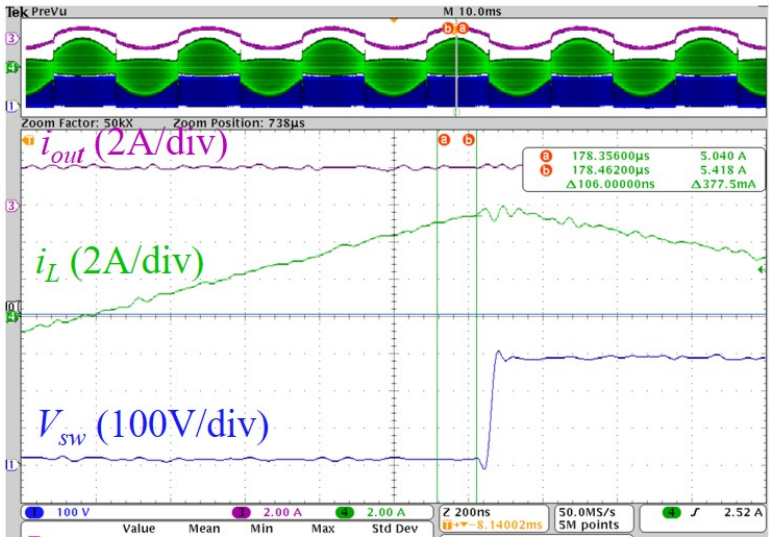


(b)

Figure 8.9: Experimental results showing the effect of propagation delay compensation using a 6 mΩ shunt resistor through a combination of two 12 mΩ in parallel. The waveform depicts (a) output current i_{out}, inductor current i_L and (b) output current i_{out}, inductor current i_L and switch node V_{sw}.



(a)



(b)

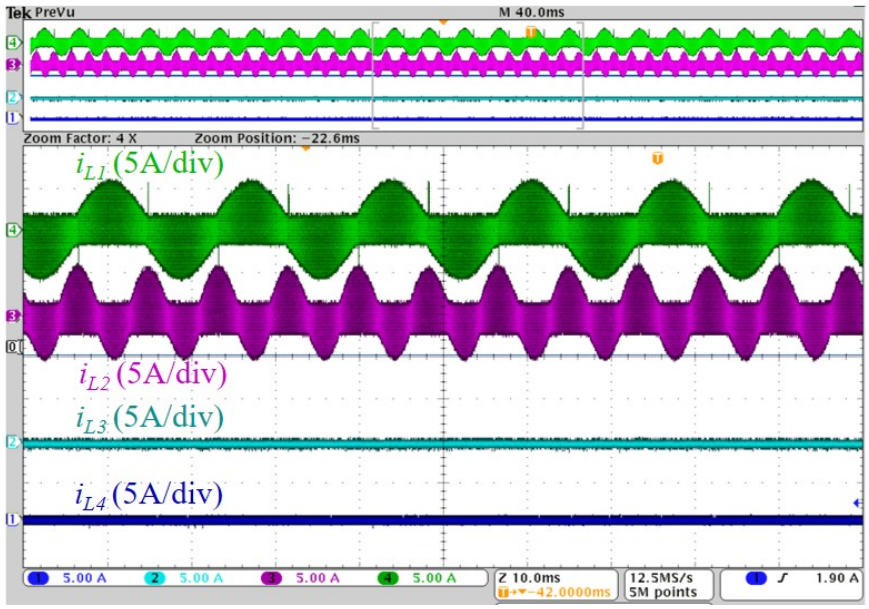
Figure 8.10: Experimental results showing the effect of propagation delay without compensation using a 20 mΩ shunt resistor. The waveform depicts (a) output current i_{out}, inductor current i_L and (b) output current i_{out}, inductor current i_L and switch node V_{sw}.

8.5.2 Steady-State Operation

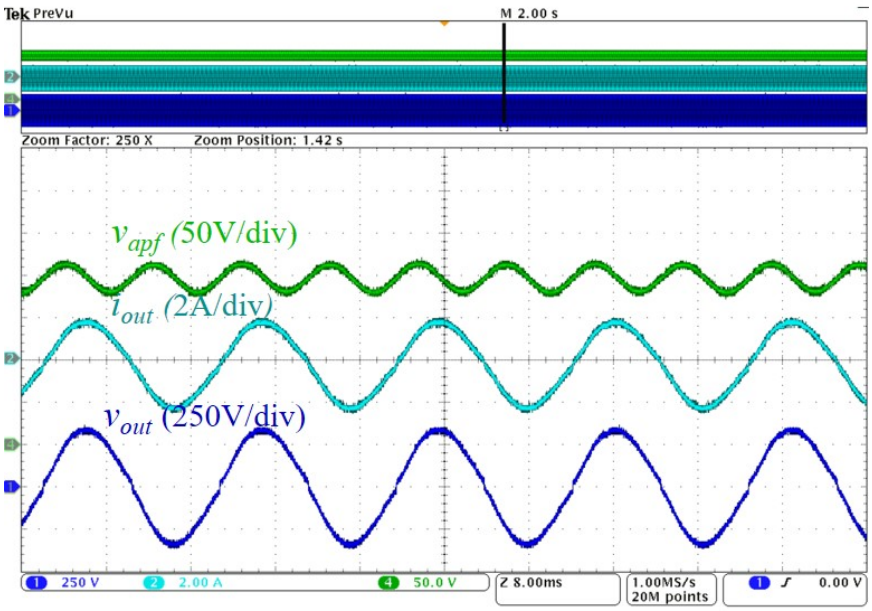
The steady-state operation of the DHA inverter is first demonstrated in Fig. 8.11 with the experimental waveform of the inductor current of each module, ac output voltage (v_{out}), APF voltage (v_{apf}) and input current (I_{dc}) at 350 W light load operation. At this power level, both the DHA and Non-DHA have the same allocation with one module doing inverter and the other doing APF during the entire line cycle. The remaining 2 modules are OFF. The RMS output voltage is well regulated at 240 V_{rms} while the dc component of the APF voltage is regulated at 200 V. In addition, Fig. 8.12 presents a detailed experimental waveform of the inductor currents of module 1 and module 2 and their corresponding switch node voltages V_{sw1} and V_{sw2}. The inductor currents are well regulated in BCM modulation, and full-range ZVS is achieved. The measured switching frequency varies approximately between 120 kHz and 500 kHz at its maximum.

Fig. 8.13 shows the experimental waveform of the DHA and Non-DHA inverter at 550 W. When doing DHA as illustrated in Fig. 8.13a, there are a maximum of three modules used with module 1 allocated for inverter, module 2 allocated for APF while module 3 is turning ON and OFF to assist with inverter operation according to the phase allocation. At the beginning of the line cycle, only module 1 is doing inverter before transitioning to module 1 and module 3 around the peak inductor current. In the case of non-DHA operation at 550 W, the inductor current waveforms for all four modules are shown in Fig. 8.13b. The allocation is static, and there are two modules ON during the entire line cycle, with module 1 doing inverter while module 2 is doing APF at all times.

Second, Fig. 8.14 shows the steady-state operational waveforms at 700 W. For the DHA operation in Fig. 8.14a, all four modules are used. Modules 1, 2 and 3 operation is similar to the previous allocation with the addition of module 4 turning ON and OFF to assist with APF operation. At the beginning of the positive line cycle, only module 1 is doing inverter before transitioning to module 1 and module 3. Similarly, the APF starts OFF with a single module (module 2) before transitioning to 2 modules (module 2 and module 4) during the negative peak APF inductor current. On the other hand, for the Non-DHA case depicted in

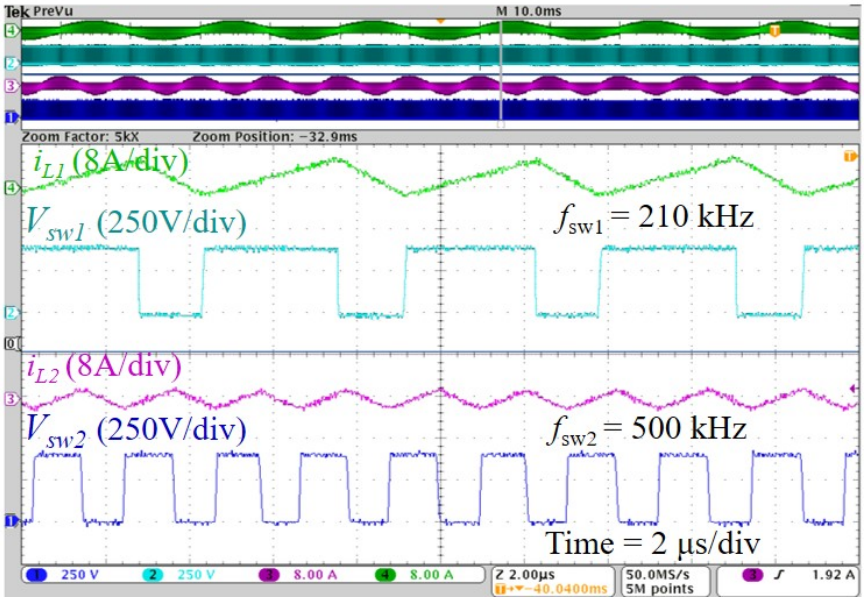


(a)

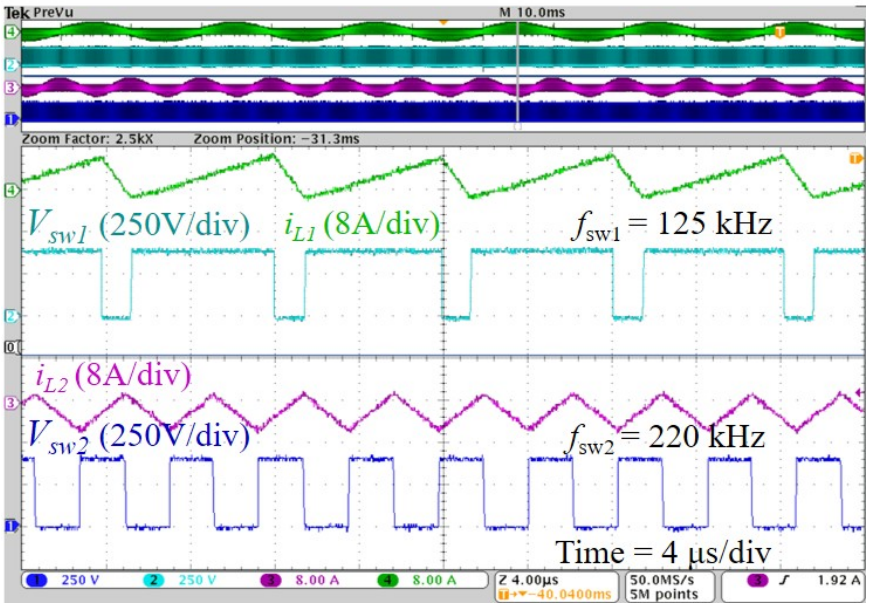


(b)

Figure 8.11: Experimental waveforms of DHA inverter showing (a) inductor current $I_{L1}, I_{L2}, I_{L3}, I_{L4}$ and (b) APF capacitor voltage V_{apf}, ac output current i_{out} and voltage V_{out}.

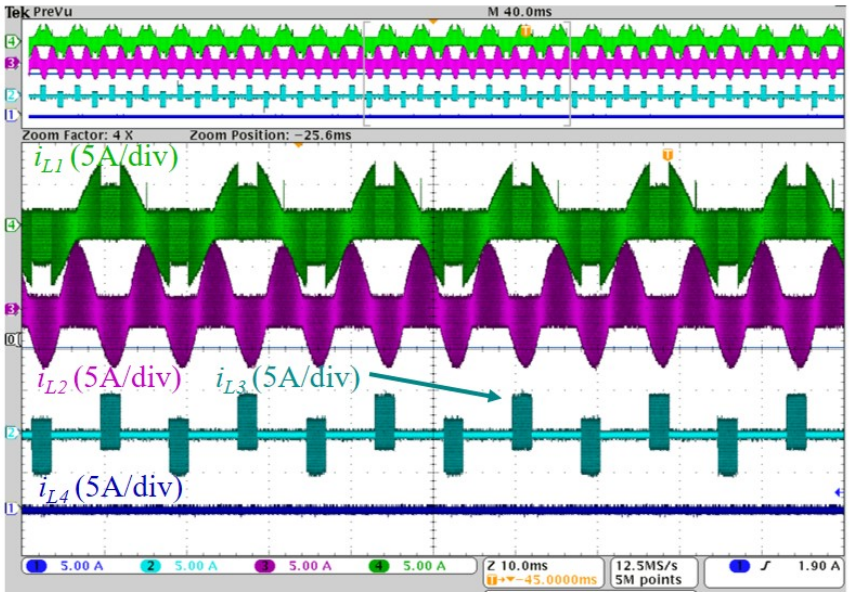


(a)

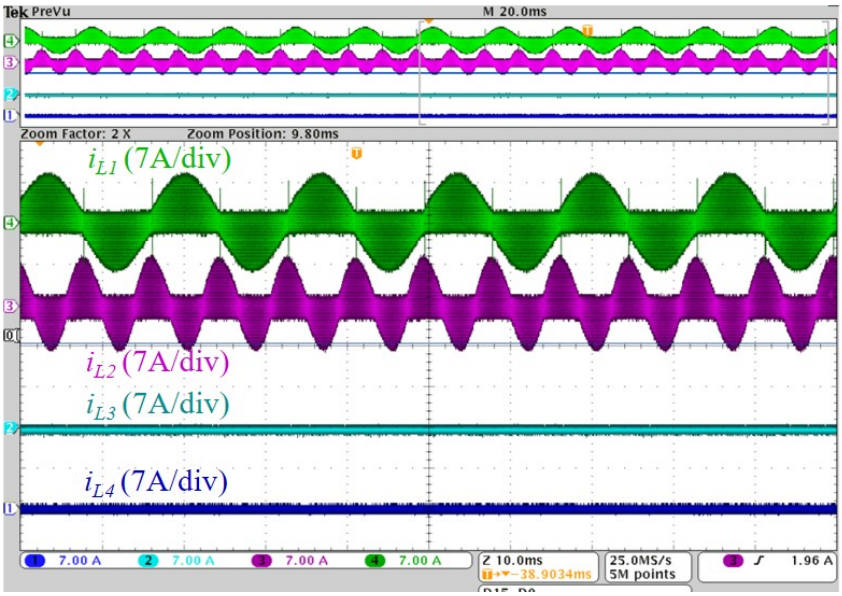


(b)

Figure 8.12: Experimental waveform showing module 1 and module 2 inductor current I_{L1}, I_{L2} and switch node voltage V_{sw1}, V_{sw2} (a) near the APF inductor current zero crossing and (b) peak inverter and APF inductor current.

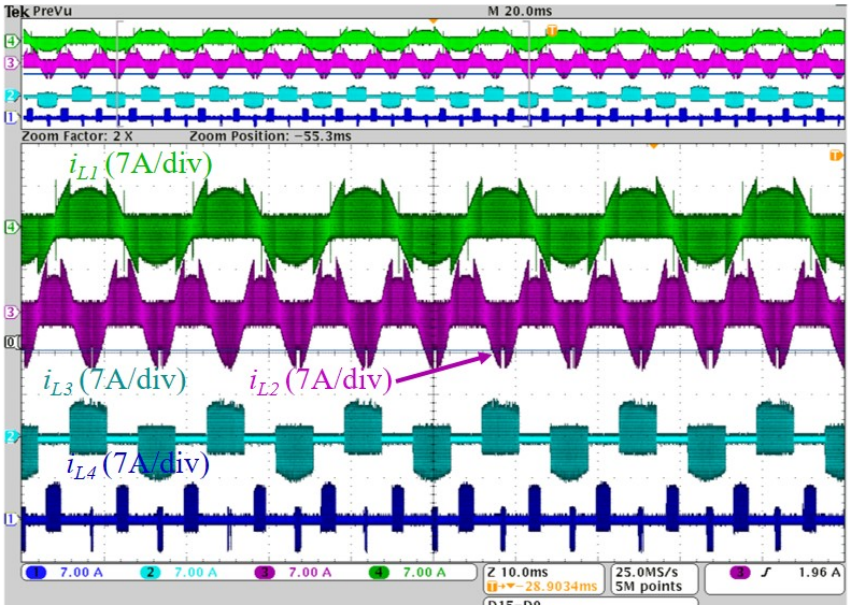


(a)

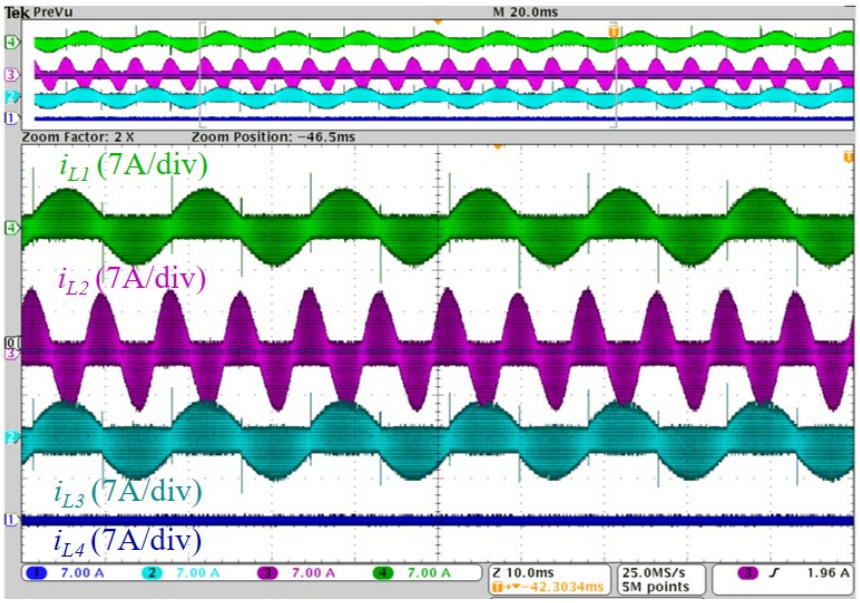


(b)

Figure 8.13: Experimental waveforms showing inductor current for (a) DHA and (b) Non-DHA at 550 W.



(a)



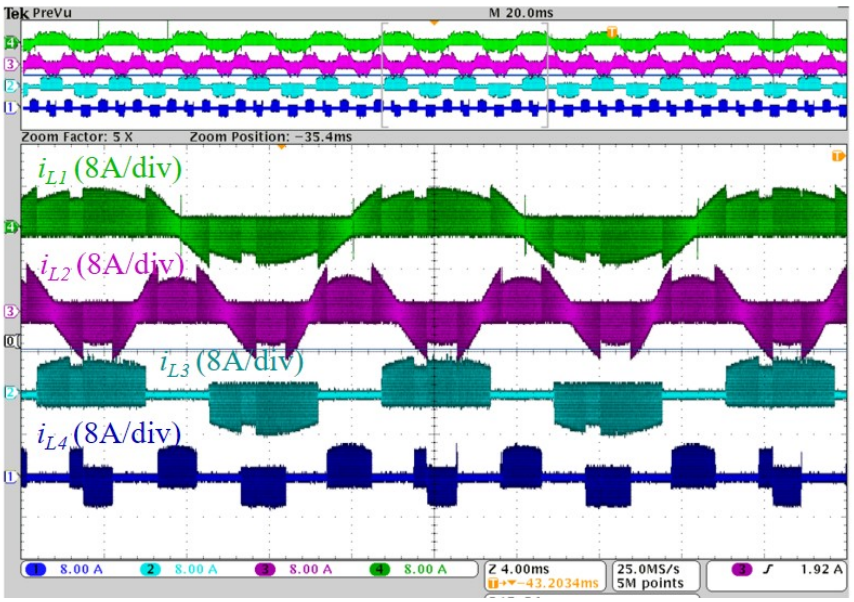
(b)

Figure 8.14: Experimental waveforms showing inductor current for (a) DHA and (b) Non-DHA at 700 W.

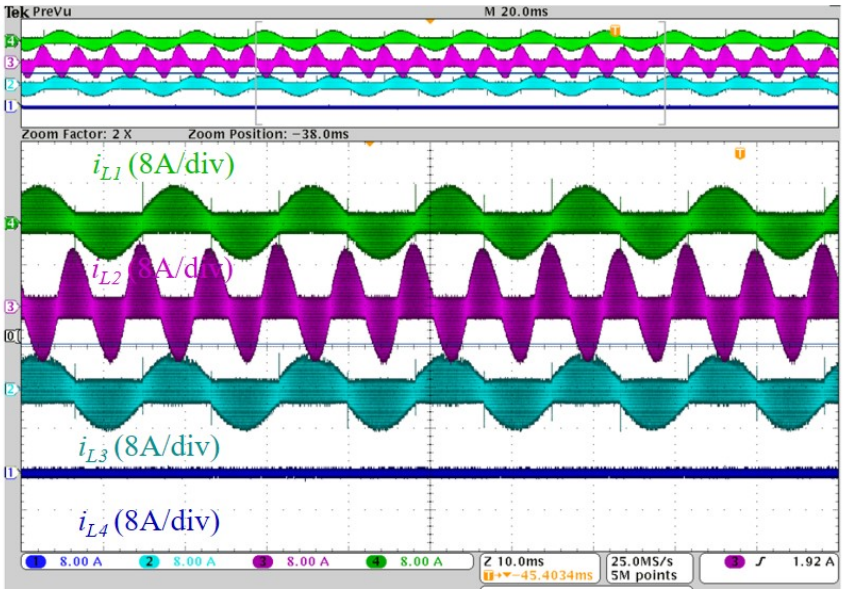
Fig. 8.14b, there are three modules that are ON while the remaining module is off. Module 1 and module 3 are doing inverter and module 2 is doing APF.

Third, Fig. 8.15 demonstrates the inverter operation at 850 W. The allocation for Non-DHA operation at this power level is illustrated in Fig. 8.15b and is exactly the same as the previous allocation at 700 W. In contrast, for the DHA operation shown in Fig. 8.15a, there are now a maximum of three modules (module 1, module 3, module 4) allocated for inverter function and two modules (module 2, module 4) allocated for APF. At the beginning of the line cycle, only module 1 is doing inverter before transitioning to module 1 and module 3 followed by module 4. Similar to the previous allocation, the APF starts off with only one module (module 2) before transitioning to module 2 and module 4 during the negative peak APF inductor current. Module 4 in this set-up alternates between both inverter and APF operation. This is illustrated in its inductor current (iL_4) shown in Fig. 8.15a.

Lastly, Fig. 8.16 depicts the experimental allocation at 1 kW full load operation. The module allocation for the DHA is similar to that at 850 W with a minor difference. At the beginning of the line cycle as depicted in Fig. 8.16a, two modules (module 1, module 2) are allocated for inverter and APF operation. Next, the allocation transition to two modules (module 1, module 3) and three modules (module 1, module 3 and module 4) doing inverter. From three modules, the allocation goes to two modules (module 1, module 3) when the module 4 transitions from inverter to APF operation. After assisting with APF operation, module 4 transitions back to inverter operation before turning off. In the case of non-DHA, as presented in Fig. 8.16b, all four modules are operating with 2 modules (module 1, module 3) doing inverter while the remaining modules (module 2, module 4) are doing APF. This is a static allocation and does not vary over the line cycle. Fig. 8.17 shows a comparison between the analytical and experimental inductor current allocation at 1 kW. The calculated inductor current illustrated in Fig. 8.17a is in accordance with the measured inductor current allocation shown in Fig. 8.17b.

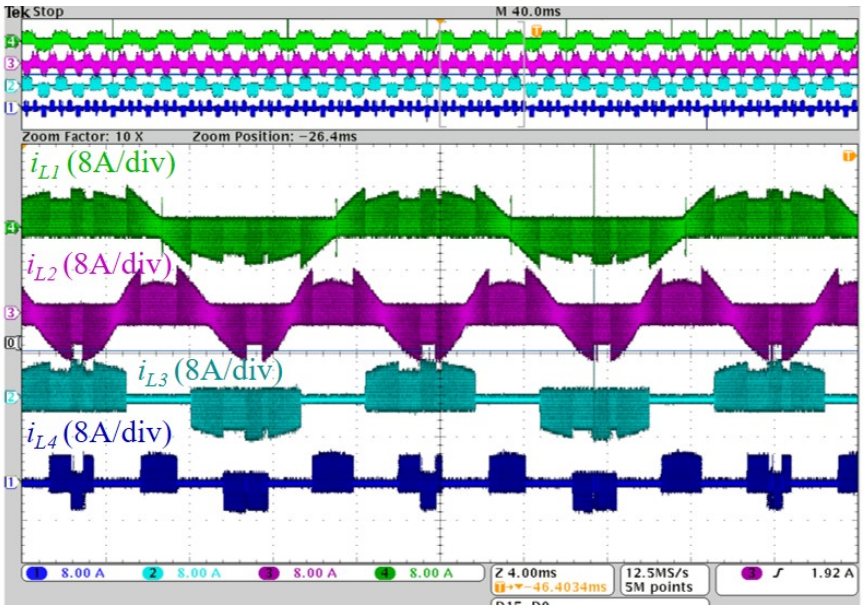


(a)

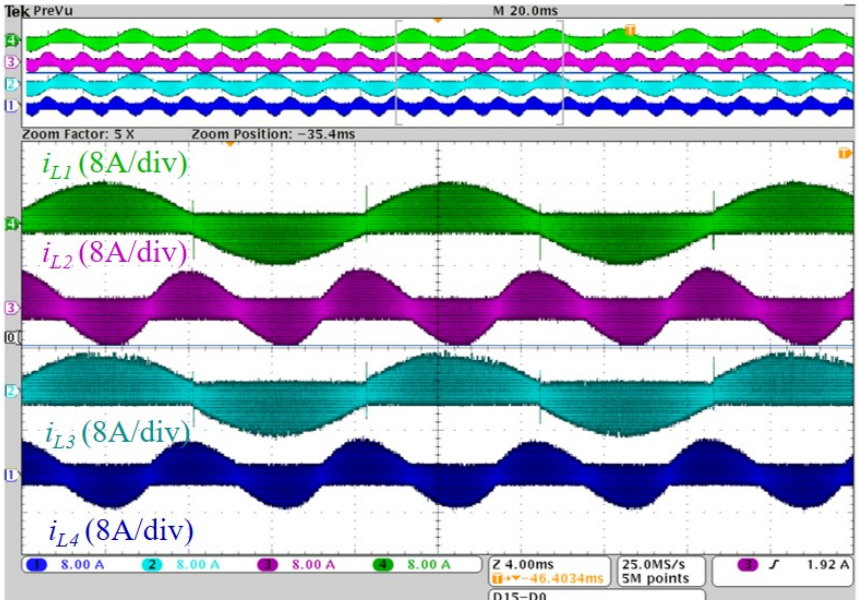


(b)

Figure 8.15: Experimental waveforms showing inductor current for (a) DHA and (b) Non-DHA at 850 W.

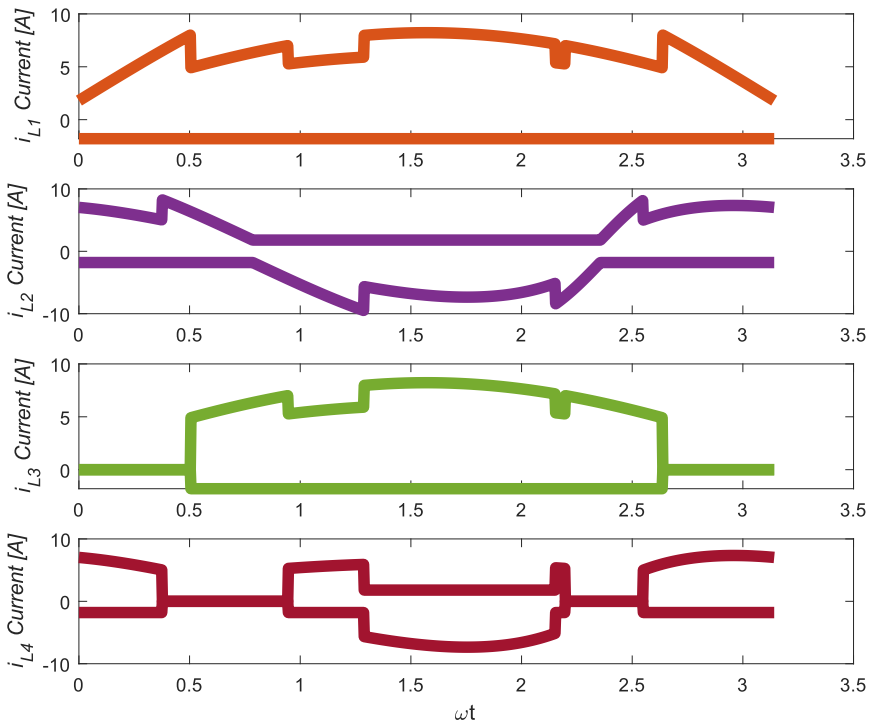


(a)

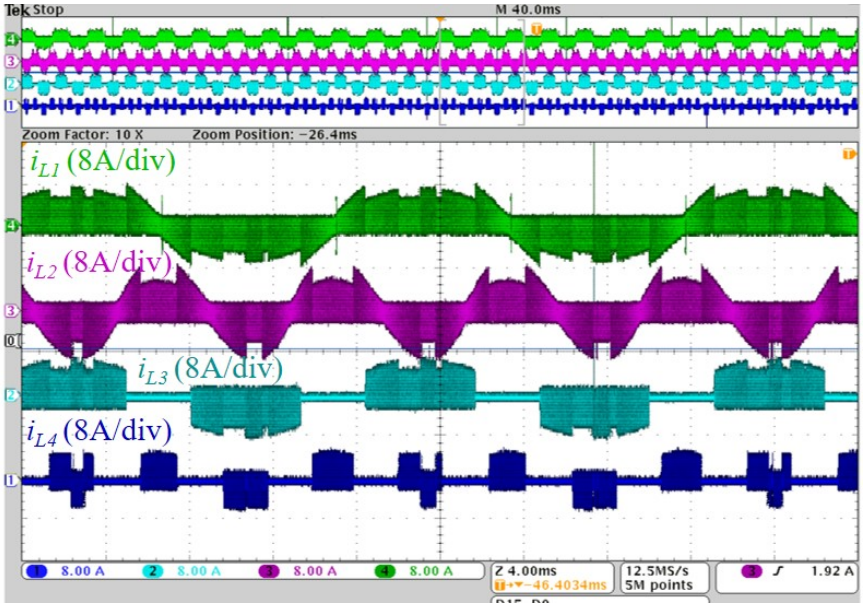


(b)

Figure 8.16: Experimental waveforms showing inductor current for (a) DHA and (b) Non-DHA at 1 kW.



(a)



(b)

Figure 8.17: Analytical and experimental inductor current allocation waveform comparison of DHA at 1 kW.

8.5.3 Active Power Filtering Operation

The operation of the energy buffer using active power filtering is demonstrated in Fig. 8.18. A total capacitance of 150 μF using a set of 5 x 30 μF capacitors in parallel is used as the buffer capacitor in this implementation. It can be seen in the waveform that the power buffer successfully compensates the 120 Hz ripple current on the dc-link. The APF capacitor voltage v_{apf} is well regulated with an average value of 200 V without any distortion. The measured input peak-to-peak current ripple ($2\Delta i_{dc}$) at full load is approximately 1 A, which is 20% of the average input current. To further illustrate the successful operation of the APF, the input dc-link current without power buffering has been tested. Due to the expected high ripple current on the dc-link, the test is performed at 650 W load. The recorded results are shown in Fig. 8.19. The measured ripple current ($2\Delta i_{dc}$) is approximately 3.90 A, which is well above 100% of the average current.

8.5.4 Efficiency Performance

Fig. 8.20 depicts the measured efficiency comparison between the DHA and non-DHA for varying load conditions. The DHA yields a better efficiency than the non-DHA. The measured DHA peak efficiency is 97.03% while that of the non-DHA is 96.76%. At light load, both DHA and non-DHA have the same efficiency given that they both start with the same number of module allocations, module 1 for inverter and module 2 for APF or (1, 1) allocation. The remaining modules, module 3 and 4 are both off. As the load increases, the DHA allocation is dynamic and changes as previously explained. However, in the case of the Non-DHA operation, the allocation is static and goes from 1 module doing inverter and 1 module doing APF (1, 1) to 2 modules doing inverter and 1 module doing APF (2, 1). This allocation helps to maintain high efficiency as power increases all the way to 850 W, when the fourth module comes online. At 1 kW load, all four modules are ON with a (2, 2) allocation. There are two modules doing inverter while the remaining half are doing APF. Fig. 8.21 and Fig. 8.22 show the measured and analytical efficiency comparison for the DHA and Non-DHA inverter. The measured efficiency data for both inverter operations are in accordance with the predicted efficiency. The predicted loss breakdown at full load

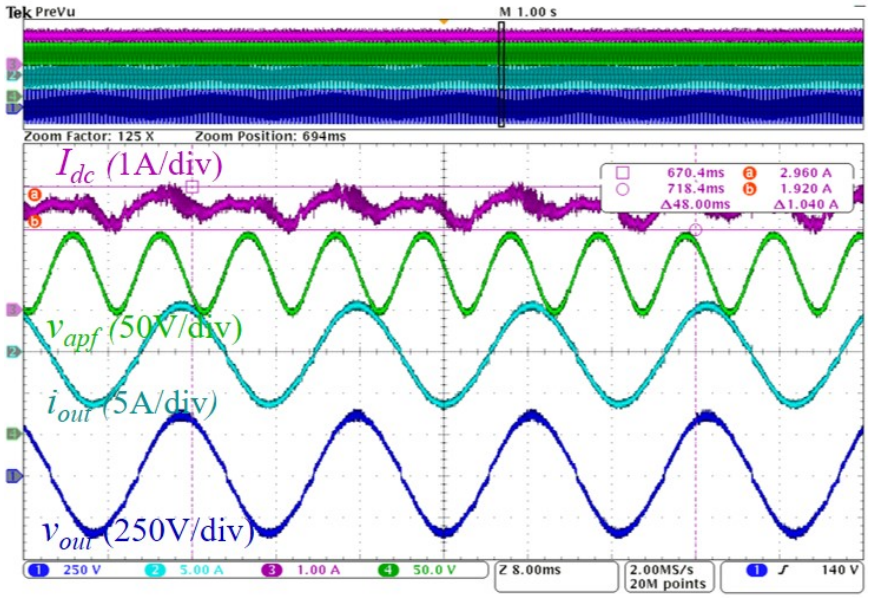


Figure 8.18: Experimental results demonstrating active power filter operation. Waveforms shown include input dc-link current I_{dc}, APF capacitor voltage v_{apf}, ac output current i_{out} and voltage v_{out} at 1 kW.

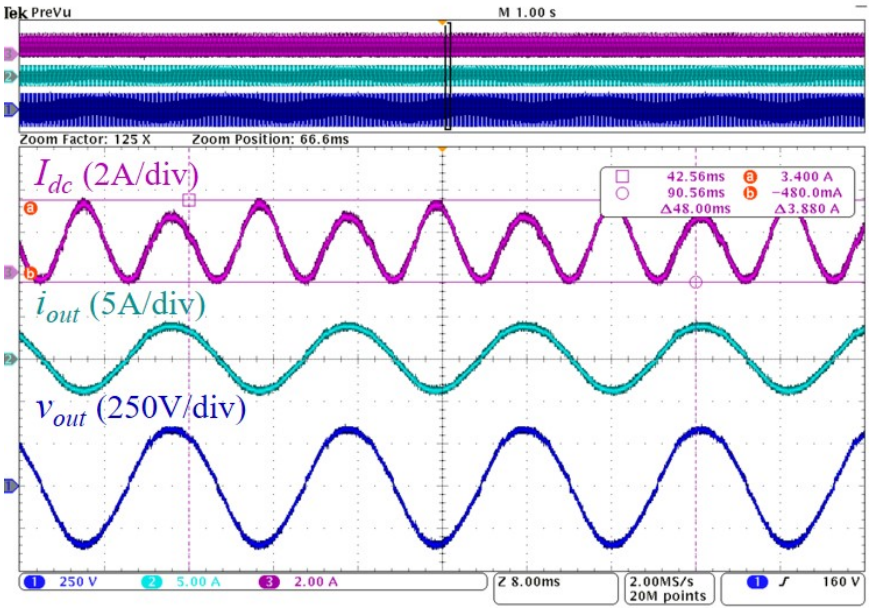


Figure 8.19: Experimental results without power buffering. Waveforms shown include input dc-link current I_{dc}, ac output current i_{out} and voltage v_{out} at 650W due to the high input ripple current on the dc-link.

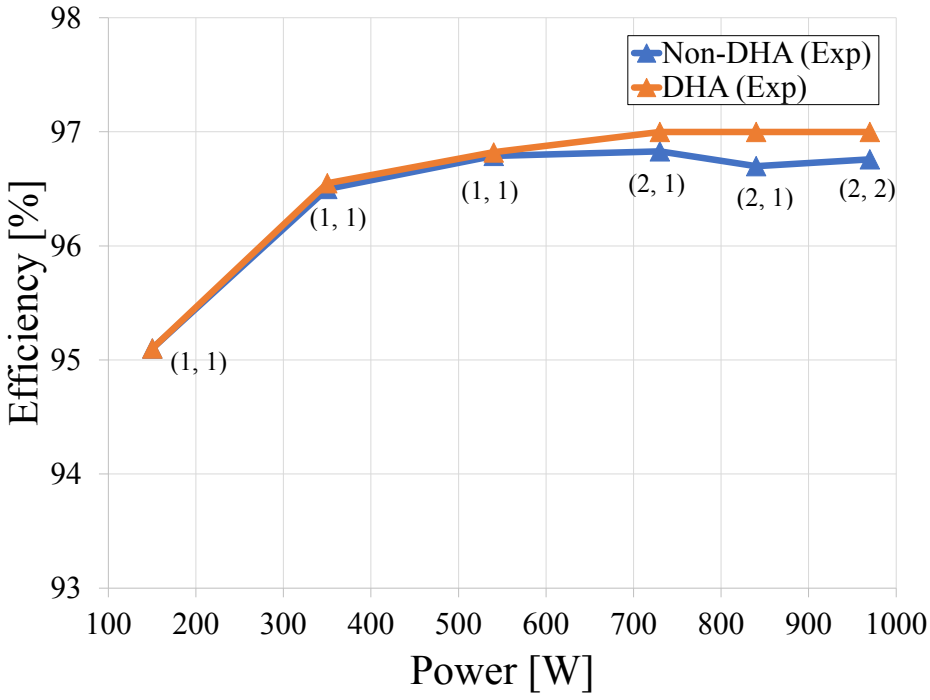


Figure 8.20: Experimental efficiency comparison of the DHA and nonDHA inverter operation for various load conditions.

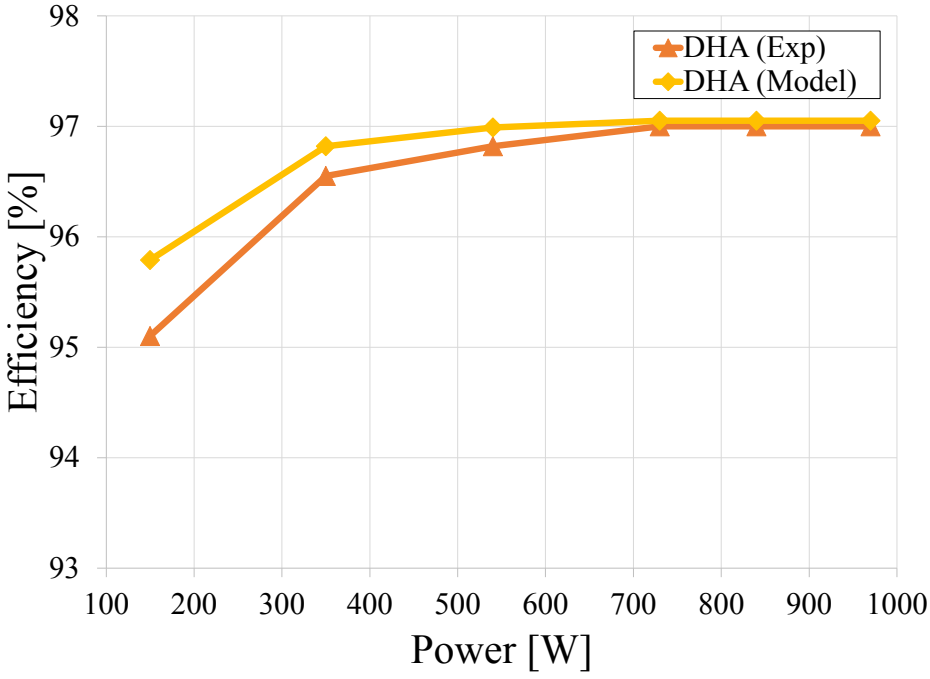


Figure 8.21: Analytical and experimental efficiency comparison of the DHA inverter operation for various load conditions.

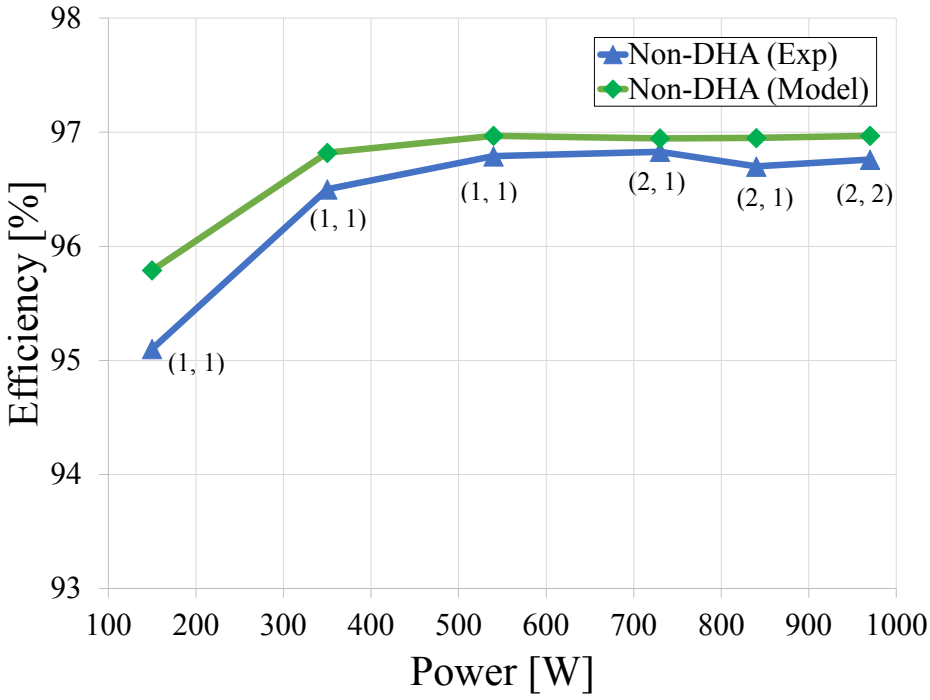


Figure 8.22: Analytical and experimental efficiency comparison of the Non-DHA inverter operation for various load conditions.

for both DHA and non-DHA operation is depicted in Fig. 8.23. The primary losses include inductor winding and core loss, device switching and conduction, and shunt resistor. The non-DHA operation does result in a slightly higher conduction loss than the DHA given the inverter and APF dispatch switch (S_{apf}, S_{inv}) present in this hardware. In an ideal hardware implementation of the non-DHA inverter, the inverter and APF dispatch switches would be non-existent, which will help lower its power loss in comparison to the DHA.

Fig. 8.24 demonstrates the thermal performance of the DHA inverter. Its cooling system consists of a fan and does not use a heatsink. The maximum steady state operating temperature of all the components in the converter including switching devices and indicators is kept below 45°C at 1 kW full load. As previously noted, the modules are turned ON in ascending order starting from module 1 and 2 up to module 4 at heavy load operation. Module 1 and 2 are kept ON at all time for inverter and APF operation while modules 3 and 4 are turned ON and OFF at various times during the line cycle as power increases. This implementation contribute to a higher power loss on module 1 and uneven heat distribution across the modules. To mitigate this effect, module shedding can be implemented in the DHA control. By shedding modules as needed, the DHA is able to distribute the heat generated more evenly across all four modules. This will help improve the overall converter efficiency.

8.5.5 THD Performance

Fig. 8.25 shows the experimental waveform of the APF capacitor voltage v_{apf}, ac output current i_{out} and voltage V_{out} for the DHA and non-DHA operation at 850 W load. Fig. 8.26 shows the measured current THD (iTHD) comparison between the DHA and non-DHA inverter operation. They both have a comparable current THD performance $< 5\%$ at high power. This result shows that the DHA inverter does not result in increased distortion of the current waveform despite the extra switching action introduced by the phase allocation.

8.6 Dynamic Operation

The dynamic response of the DHA is demonstrated in Fig. 8.27 with a load step change from 400 W to 700 W. Following a load change as illustrated by the compensator voltage v_{comp} it

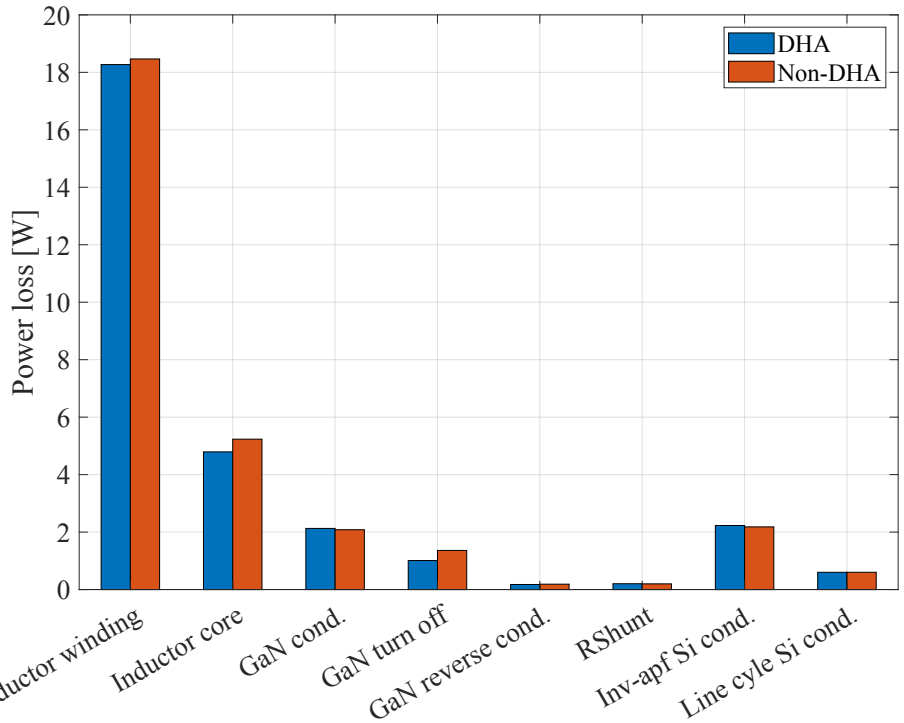


Figure 8.23: Estimated power loss breakdown comparison of the DHA and non-DHA inverter operation at 1 kW.

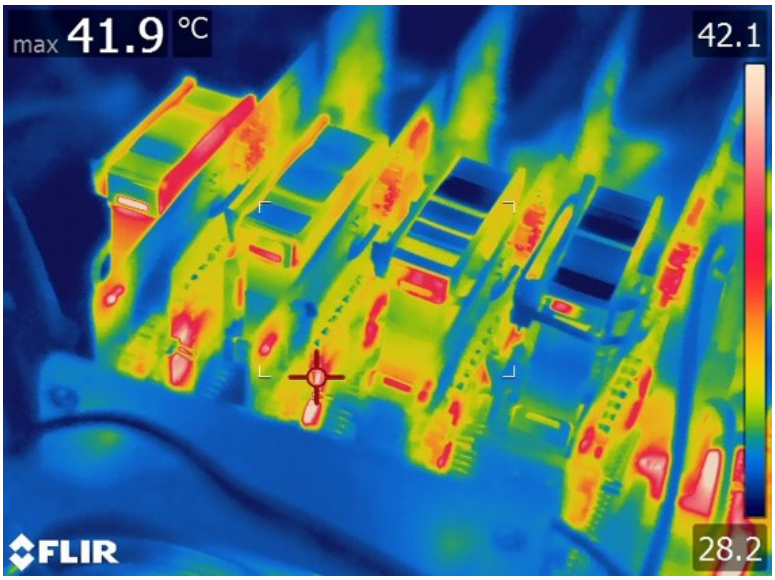
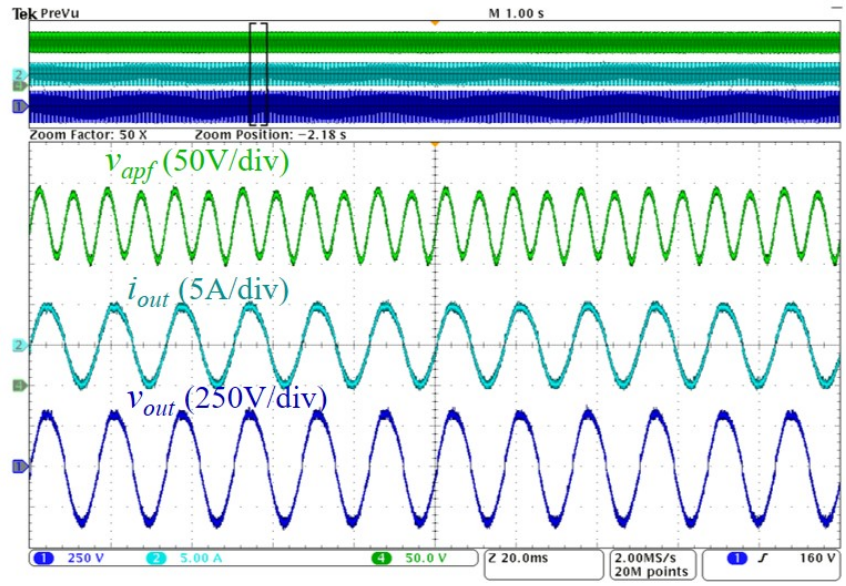
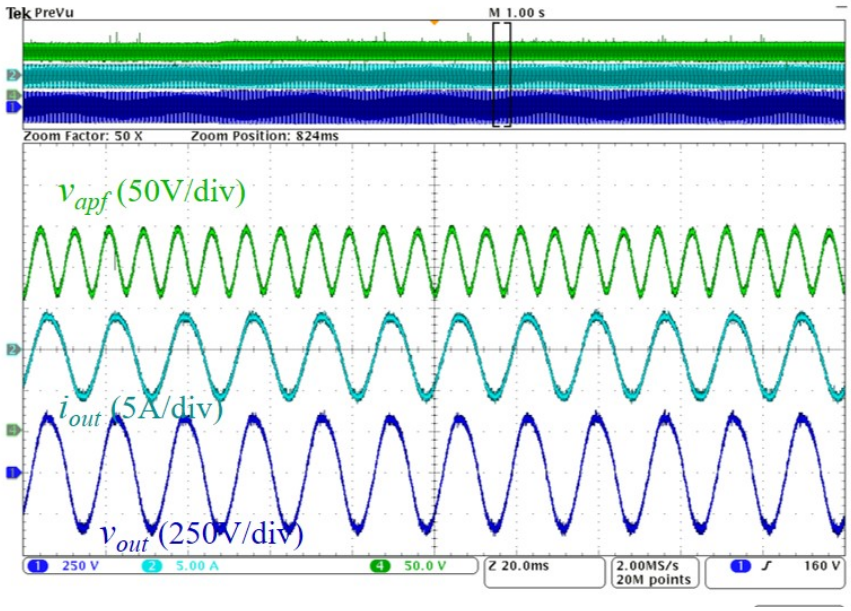


Figure 8.24: Thermal image of the DHA inverter operating at 1 kW full power.



(a)



(b)

Figure 8.25: Experimental waveform showing the APF capacitor voltage v_{apf}, ac output voltage v_{out} for (a) DHA and (b) Non-DHA at 850 W.

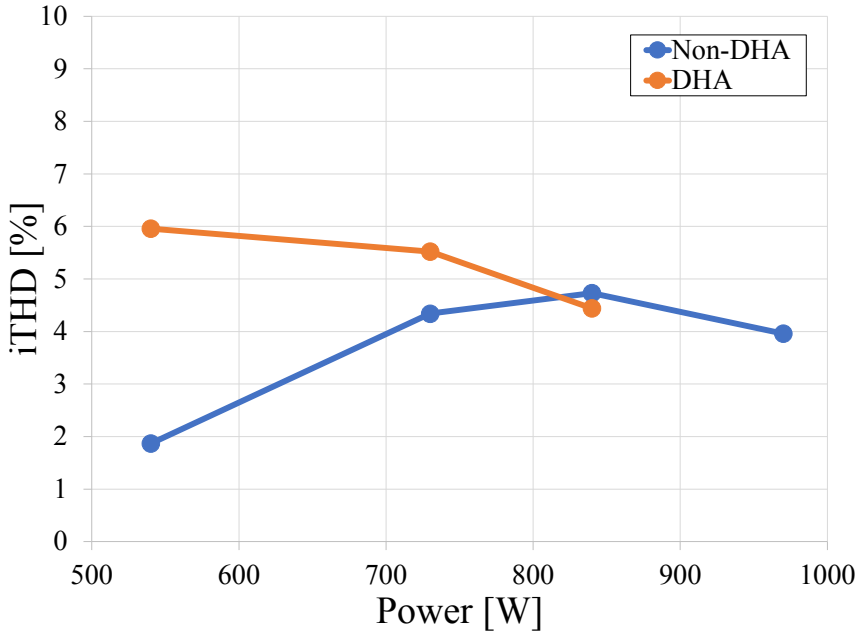


Figure 8.26: Measured iTHD comparison of DHA and Non-DHA for various load condition.

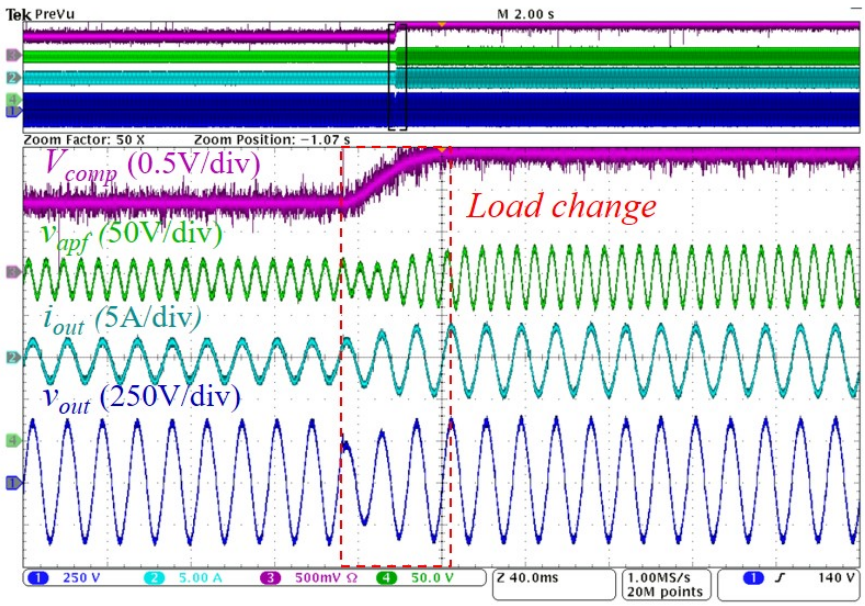


Figure 8.27: Experimental waveform of DHA showing the compensator voltage v_{comp}, APF voltage v_{apf}, output current i_{out} and voltage v_{out} during a load step transients from 400 W to 700 W.

can be seen that the magnitude of the output voltage v_{out} and the average APF voltage v_{apf} are well regulated. The dc component of the APF voltage is well regulated to 200 V and is not impacted by the load change. The measured response time is within 50 ms or three line cycles after the load change.

Fig. 8.28 shows the predicted transient response from the average model with a load step. Similar to the obtained experimental results, the modeled transient response takes about 3 line cycles which is in accordance with the experiment. This agreement between the experiment and model demonstrates the accuracy of the control loop design and simulation.

8.7 Summary

In this chapter, a hardware prototype of the DHA inverter has been designed, built and tested to validate the DHA model and how it compares with the traditional non-DHA approach. The controller design and modeling analysis of the DHA inverter has also been carried out and validated through simulation and experimental prototypes. A closed loop controlled hardware prototype of the optimal DHA with 4 modules has been built and tested up to 1.0 kW.

The small signal model of the converter has been derived and the average model has been built and simulated in Simulink Matlab to verify the control design. The control has been successfully implemented experimentally and allowed for a stable dynamic response with an autonomous phase allocation of the inverter. The phase allocation exhibits a smooth transition of the inductor current between modules. It effectively regulates the magnitude of the ac output voltage and filters the second harmonic current on the dc-link. Both, the steady state and dynamic model of the DHA inverter have been validated with the experimental results, demonstrating the accuracy of the design and modeling process.

In addition, the DHA inverter achieves a peak efficiency of 97% efficiency and a current THD of less than 5%. Its estimated LCOE is 4.36 ¢/KWh. In contrast, the multi-phase non-DHA inverter using the same hardware has a peak efficiency of 96.76%, a current THD of 4% and an estimated LCOE of 19.25 ¢/KWh. The DHA yields the lowest expected LCOE,

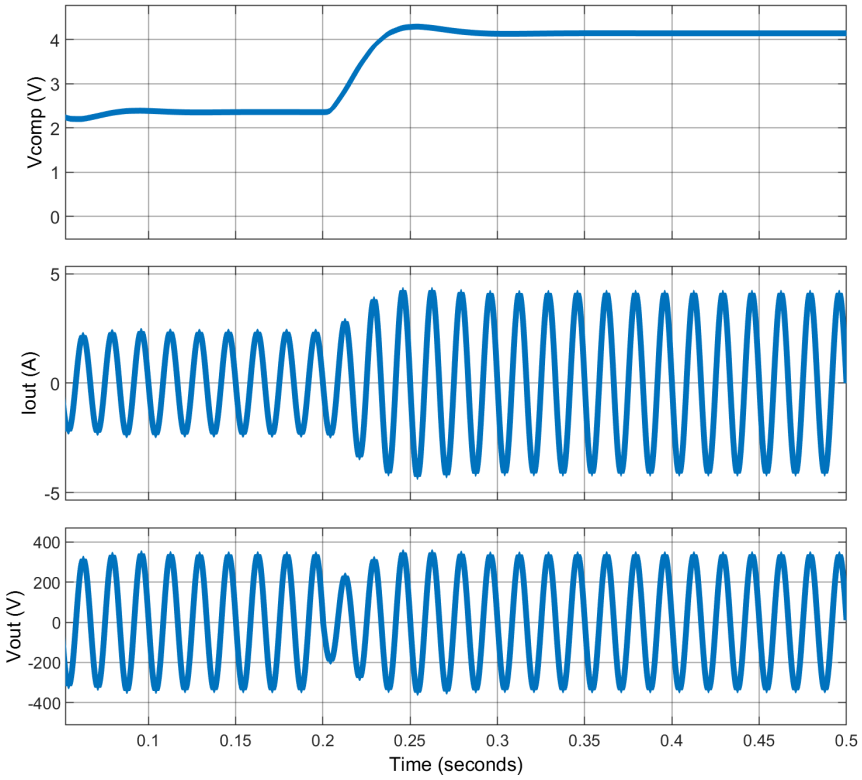


Figure 8.28: Model waveform of DHA transient response showing the compensator voltage v_{comp}, output current i_{out} and output voltage v_{out} during a load step transients from 400 W to 700 W.

the highest efficiency, and an equivalent current THD performance when compared with the multi-phase non-DHA inverter operation with the same hardware.

Chapter 9

Conclusions and Future Work

9.1 Summary of Work

In this dissertation, a new topological and control scheme that allows dynamic hardware allocation (DHA) has been introduced to increase the reliability of single-phase GaN-based PV inverters. The proposed method achieves a lifetime of well over 50 years contributing to lowering the Levelized cost of energy (LCOE) of PV systems. To achieve this goal, technical innovations addressing control challenges for GaN-based operation at high frequency have been proposed.

First, a dual current program mode (DCPM) controller has been developed to address noise and propagation delay challenges prevalent in boundary current mode control. In addition, a hybrid control technique combining both bipolar and unipolar switching techniques has been implemented and demonstrated in order to mitigate the zero-crossing issues prevalent in unipolar-switched BCM inverters.

Second, a mission profile-based design for reliability (DfR) analysis has been used to evaluate the reliability performance of the DHA inverter in comparison to the traditional multiphase approach without DHA. The analysis showed that the lifetime of the inverter could be significantly improved with DHA and illustrated how essential it is to integrate design for reliability evaluation during the converter design stage instead of designing for just high efficiency.

Third, an LCOE-driven design optimization has been carried out to derive optimal designs for both DHA and Non-DHA inverters. The proposed DHA inverter yields the lowest LCOE over a 50-year PV system lifetime, making it a cost-effective option. Then, a low voltage and current experimental hardware of the inverter using DHA has been successfully built and tested to validate the feasibility of the DHA concept.

Finally, a 1 kW prototype using 4 modules has been built and tested to demonstrate the operation of the DHA inverter. It achieves a peak efficiency of 97.0% and has a better efficiency performance when compared with the traditional multiphase non-DHA architecture with a similar number of modules. The proposed current compensation technique has also been applied to the DHA implementation, yielding a low current THD of $< 5\%$.

9.2 Contributions

The contributions of this dissertation are summarized as follows:

1. A dual current programmed mode (DCPM) controller has been introduced to address noise and propagation delay challenges in GaN-based high-frequency boundary current mode (BCM) modulated inverters. The improved DCPM controller enhances switching noise immunity and compensates for propagation delays at high frequency.

2. An inverter control scheme combining both the advantages of bipolar and unipolar switching has been developed to address zero-crossing issues prevalent in unipolar-switched BCM inverters. The proposed technique eliminates the low-frequency output current distortion at the inverter output current zero crossings while improving efficiency.

3. A new topological and control scheme using dynamic hardware allocation (DHA) has been introduced. The proposed control technique and hardware increase the reliability and lifetime of GaN-based PV inverters.

4. A LCOE-driven design optimization technique of GaN based single phase inverter using dynamic hardware allocation has been proposed to select the optimal number of modules in the DHA.

5. A control strategy for GaN based single phase inverters using dynamic hardware allocation has been proposed and developed.

9.3 Future Work

9.3.1 Active Power Filter Control Using Proportional Resonant Compensator

The block diagram for the APF control loop is illustrated in Fig. 9.1. This control loop is designed to set the 120 Hz component of the input dc-link current to zero while regulating the DC component of the APF voltage to 200 V. To improve the power buffing performance of the DHA inverter, a proportional resonant (PR) controller technique could be used. Instead of a model-based approach where the APF reference current is calculated from the power equation, a PR controller is tuned to the second and fourth harmonics present in the input current. The input dc-link current is then regulated to cancel out the 120 Hz ripple current and its harmonics by setting it to zero. The transfer function for the PR is given by

$$PR(s) = K_p + K_i \cdot \frac{s}{s^2 + w_2^2} + K_i \cdot \frac{s}{s^2 + w_4^2} \tag{9.1}$$

and that of the controlled current to input dc-link current is

$$G_{vi,apf}(s) = \frac{\hat{v}_{apf}}{\hat{i}_L} = \frac{1}{C_{apf}s} \tag{9.2}$$

Similar to the model-based implementation, a PI compensator $G_c(s)$ is used to regulate the average APF voltage to 200 V.

The average model of the BCM switched inverter has been designed and simulated in PLECS to validate the proposed APF controller using a PR compensator. A schematic of the model is shown in Fig. 9.2. The obtained simulation waveforms including the AC power (P_{ac}), output voltage (v_{out}), current (i_{out}), regulated APF voltage (v_{apf}) and input dc-link current (I_{dc}) are illustrated in Fig. 9.3. The performance of the APF is improved. The

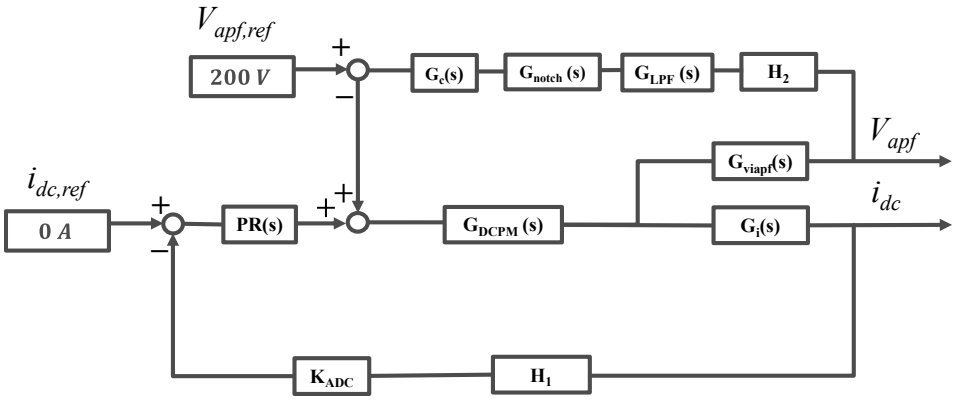


Figure 9.1: APF voltage and input dc-link control loop.

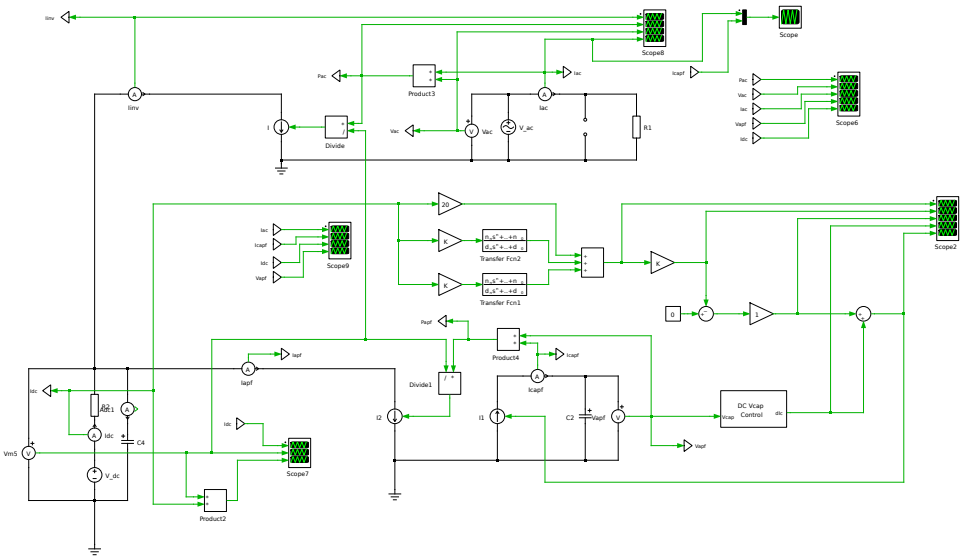


Figure 9.2: Inverter average model schematic in PLECS.

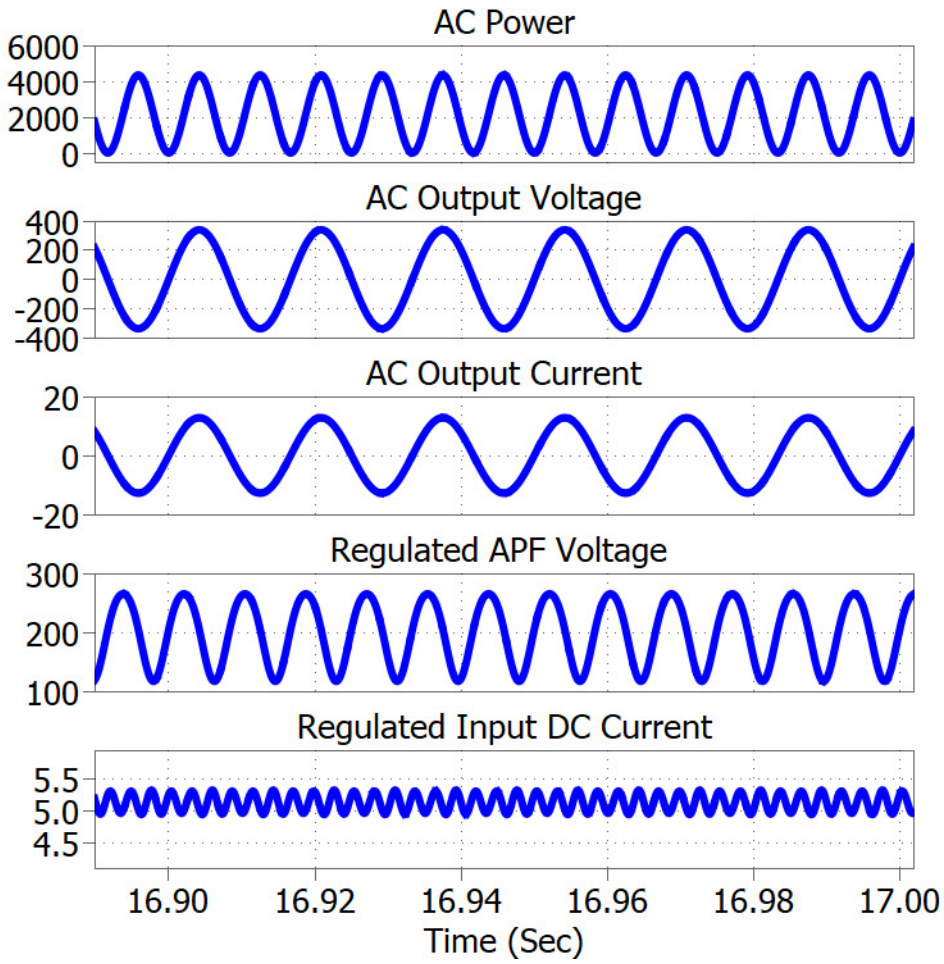


Figure 9.3: Inverter simulation waveforms with derived APF closed loop control. Signals from top to bottom include inverter AC power (P_{ac}), output voltage (V_{ac}), current (I_{ac}), regulated APF voltage (V_{apf}) and input dc-link current (I_{dc}).

second-harmonic ripple current on the input dc-link is limited to within 3% while the DC component of the APF voltage is regulated to approximately 200 V.

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Vita

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