

# **Characterization Methodology, Modeling, and Converter Design for 600 V Enhancement-Mode GaN FETs**

A Dissertation Presented for the  
Doctor of Philosophy  
Degree  
The University of Tennessee, Knoxville

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May 2018

## Acknowledgments

I would like to acknowledge the support and collaboration of my many peers and mentors at the University of Tennessee, Knoxville. Dr. Fred Wang provided many years of guidance and education as my advisor. Drs. Leon Tolbert, Daniel Costinett, Benjamin Blalock, Syed K. Islam, Burak Ozpineci, and Lee Riedinger have also been valuable faculty advisors during my graduate career. The feedback and advice offered during group meetings and individual discussions have made this work possible.

The collaboration with other students at the University of Tennessee has been equally important. I have been guided and challenged by these peers as we all work together to learn and earn our degrees. I would especially like to thank Yalong Li, Zheyu Zhang, Ben Guo, Weimin Zhang, Cameron Riley, Bo Liu, Ren Ren, Rémi Perrin, Zhiqiang Wang, Chongwen Zhao, Yutian Cui, Zhuxian Xu, Jing Xue, Jacob Dyer, Craig Timms, Paige Williford, Jianliang Chen, Zhe Yang, and Fei Yang for working closely with me on my research over the past five years.

Outside of UTK, I would also like to thank Joonas Puukko, Sandeep Bala, and Jing Xu from ABB; Eric Persson, Tim McDonald, and Deepak Veerreddy from Infineon; Adam Barkley from Wolfspeed; Christina Dimarino, Xiucheng Huang, Bin Lu, and Zhengyang Liu from CPES at Virginia Tech; He Li from The Ohio State University; Dr. Raghav Khanna from The University of Toledo; and Dr. Andrew Lemmon from The University of Alabama.

At my alma mater, Virginia Tech, Dr. Jason Lai and Dr. Allen Mackenzie were both major influences in my early academic career, advising me on undergraduate research and professional direction.

I would also like to acknowledge the financial support and use of facilities sponsored by the Engineering Research Center Program of the National Science Foundation and Department of Energy, the CURENT Industry Partnership Program, the Bredesen Center for Interdisciplinary

Research and Graduate Education, and the UTK Department of Electrical Engineering and Computer Science.

I appreciate the support of my friends and family throughout my academic career. In particular, I would like to thank my fiancée Carissa for her patience and understanding when the days got long and the weekends disappeared.

## **Abstract**

Gallium Nitride (GaN) power devices are an emerging technology that have only become available commercially in the past few years. This new technology enables the design of converters at higher frequencies and efficiencies than those achievable with conventional Si devices. This dissertation reviews the unique characteristics, commercial status, and design challenges that surround GaN FETs, in order to provide sufficient background to potential GaN-based converter designers.

Methodology for experimentally characterizing a GaN FET was also presented, including static characterization with a curve tracer and impedance analyzer, as well as dynamic characterization in a double pulse test setup. This methodology was supplemented by additional tests to determine losses caused by Miller-induced cross talk, and the tradeoff between these losses and overlap losses was studied for one example device.

Based on analysis of characterization results, a simplified model was developed to describe the overall switching behavior and some unique features of the device. The impact of the Miller effect during the turn-on transient was studied, as well as the dynamic performance of GaN at elevated temperature.

Furthermore, solutions were proposed for several key design challenges in GaN-based converters. First, a driver-integrated overcurrent and short-circuit protection scheme was developed, based on the relationship between gate voltage and drain current in GaN gate injection transistors. Second, the limitations on maximum utilization of current and voltage in a GaN FET were studied, particularly the voltage overshoots following turn-on and turn-off switching transients, and the effective cooling of GaN FETs in higher power operation. A thermal design was developed for heat extraction from bottom-cooled surface-mount devices. These solutions were verified in a GaN-based full-bridge single-phase inverter.



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## Chapter 1

### Introduction

#### 1.1 *Design tradeoffs in power semiconductor devices*

The field of power electronics provides opportunities for a wide range of applications, from increased portability in small consumer electronics to increased efficiency in high voltage dc transmission lines. The magnitude of these improvements is often limited by the components and design tools available, such as power semiconductor devices, high-performance passives, topologies, and control schemes. The power semiconductor device is the core component in switch-mode power conversion, so improvements in this technology can benefit the field as a whole.

Figure 1.1 shows a typical example of a silicon (Si) power device, a vertical doubly-diffused power MOSFET (DMOS). When the gate is forward biased, an inversion layer is formed across the p-doped body region, creating a low-impedance path between drain and source terminals. This on-resistance produces undesirable conduction loss, but it can be reduced by enlarging the die area, reducing the drift region height, or increasing the doping density of the device design. However, there are tradeoffs in each of these parameters that affect the performance of the device in a switch-mode converter. A larger die area increases the input and output capacitance of the device, which causes higher switching loss. A narrower drift region or higher doping density reduces the effective depletion region that acts to block voltage when the gate is biased in an off state, as shown in Figure 1.2. This narrower depletion region may reduce the device's maximum blocking voltage capability, as determined by the electric breakdown field of Si. Choosing an appropriately rated device is critical to designing an efficient converter, balancing the tradeoff between voltage-blocking capability, switching loss, and conduction loss. New wide bandgap semiconductors have properties that are superior to Si and shift the balance of this tradeoff for the benefit of the converter design.

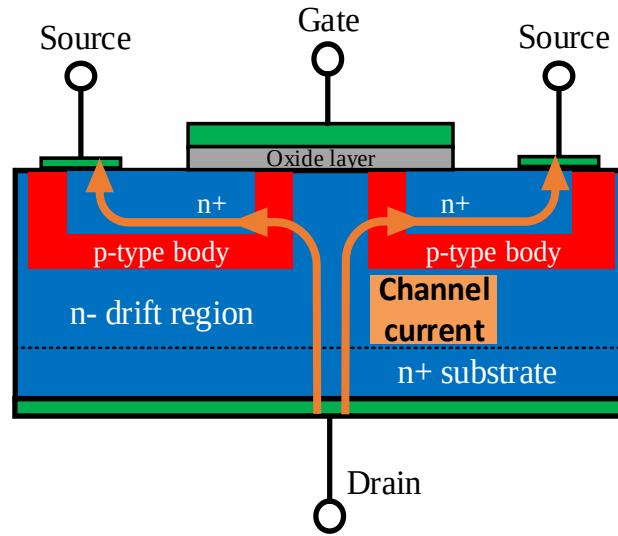


Figure 1.1. Simplified drawing of a vertical doubly-diffused (DMOS) power MOSFET in on-state [1].

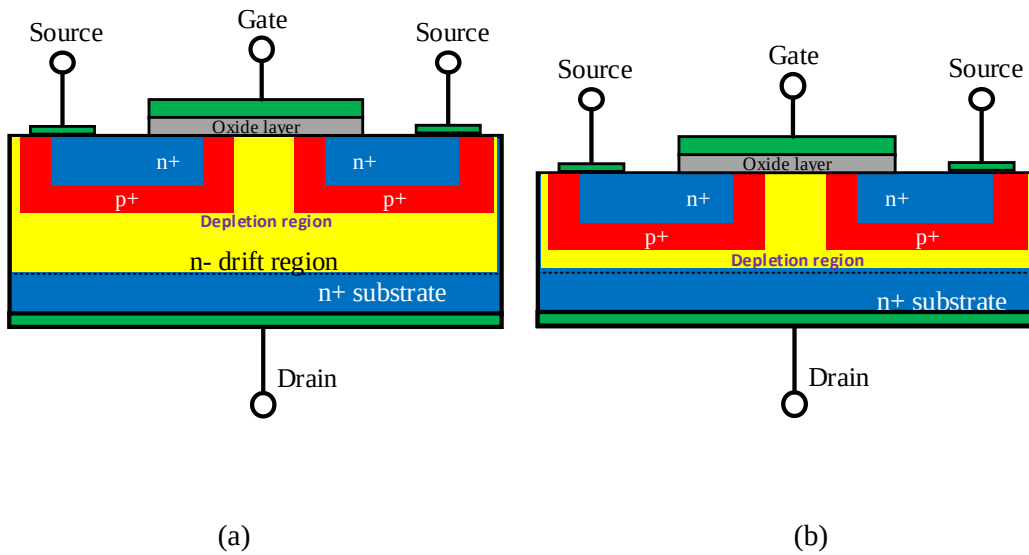


Figure 1.2. Simplified drawing of a vertical doubly-diffused (DMOS) power MOSFET in off-state, comparing (a) a device with higher voltage-blocking capability, and (b) a device with a lower voltage-blocking capability.

## 1.2 *Wide bandgap semiconductors*

Wide bandgap (WBG) devices are an enabling technology for high-frequency, high-efficiency power electronics. WBG semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) provide advantages over conventional Si power devices, as shown in Figure 1.3 and Table 1.1. The higher breakdown field of a WBG semiconductor allows for devices to be optimized with thinner drift regions to achieve a given voltage rating, resulting in power devices with lower specific on-resistance. This allows a smaller die size to achieve a desired on-resistance and current capability, and therefore lower input and output capacitances. Higher saturation velocity and lower junction capacitances enable faster switching transients. In total, the material properties of WBG semiconductors result in a device with lower conduction and switching losses than a Si device with comparable voltage and current capabilities [2-5].

SiC excels in high temperature applications, due to the thermal conductivity and overall device performance at elevated temperatures. However, the material characteristics of GaN make it a superior semiconductor for high-efficiency, high-frequency converters. The higher breakdown field enables a similarly rated GaN power device to typically outperform Si and SiC in terms of on-resistance, switching speed, or both, depending on the design of the device. Other WBG semiconductors such as GaAs, diamond, and AlN have also been heavily researched for power applications, but SiC and GaN have shown the most promise for near-term commercialization [2-5].

Figure 1.4 shows a timeline for the development of power semiconductor devices. In the 1950's, the thyristor was the only option for solid-state power electronics in the hundreds of volts. As the technology further developed, newer devices such as the JFET, power MOSFET, and IGBT were introduced with greatly improved performance and higher voltage and current ratings. Now, in the 21<sup>st</sup> century, wide bandgap semiconductors are the latest in the trend toward higher-

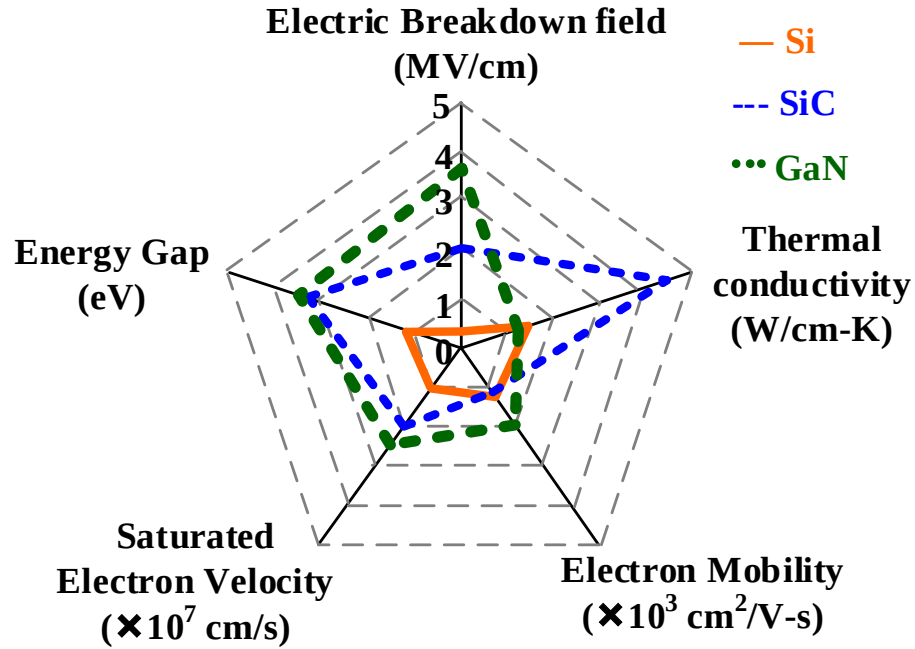


Figure 1.3 Comparison of Si, SiC, and GaN for power semiconductor applications [4],[5].

Table 1.1. Properties of wide bandgap semiconductors [4],[5].

| Property                                                                | Si   | GaAs | 6H-SiC                              | 4H-SiC                                | GaN                                    | Diamond | AlN  |
|-------------------------------------------------------------------------|------|------|-------------------------------------|---------------------------------------|----------------------------------------|---------|------|
| Bandgap, $E_g$ (eV)                                                     | 1.12 | 1.42 | 3.00                                | 3.26                                  | 3.44                                   | 5.45    | 6.20 |
| Electric breakdown field, $E_c$ (MV/cm)                                 | 0.3  | 0.4  | 2.5                                 | 2.0                                   | 3.8                                    | 10.0    | 12.0 |
| Electron mobility, $\mu_n$ ( $\text{cm}^2/\text{V-s}$ )                 | 1500 | 8500 | 420 <sup>a</sup><br>84 <sup>c</sup> | 950 <sup>a</sup><br>1190 <sup>c</sup> | 1000 <sup>a</sup><br>2000 <sup>2</sup> | 3800    | 300  |
| Saturated electron drift velocity, $v_s$ ( $\times 10^7 \text{ cm/s}$ ) | 1.0  | 1.2  | 2.0                                 | 2.0                                   | 2.5                                    | 2.7     | 1.7  |
| Dielectric constant, $\epsilon_r$                                       | 11.8 | 13.1 | 9.7                                 | 10.0                                  | 9.5                                    | 5.5     | 8.5  |
| Thermal conductivity, $\lambda$ (W/cm-K)                                | 1.5  | 0.46 | 4.9                                 | 4.9                                   | 1.3                                    | 22      | 2.85 |

<sup>a</sup> Mobility along a-axis

<sup>c</sup> Mobility along c-axis

<sup>2</sup> Mobility of 2DEG

performance power electronics.

Commercialization of wide bandgap power devices began with the development of SiC diodes and JFETs. More recently, the 1200 V SiC MOSFETs and Schottky diodes have entered the market to compete with the 1200 V Si IGBT and Si diodes. SiC devices are available at lower voltages as well, including 600-900 V, but most of the SiC devices available today are rated at 1200 V. SiC MOSFETs are vertically diffused, with structures similar to the Si power MOSFET, including planar and trench MOSFETs. However, the doping, drift region width, and die size are very different [6],[7].

At the 600 V level, the Si Super Junction MOSFET has been the dominant technology for several years. This device structure uses deep p-doped wells beneath the body regions to produce devices capable of blocking over 600 V, while maintaining a thin effective drift region to reduce the on-resistance and die size. However, there are some undesirable drawbacks, such as a highly nonlinear output capacitance. The lateral GaN heterojunction field effect transistor (HFET), also called the high electron mobility transistor (HEMT), has recently presented another option for 600 V power devices.

The GaN HFET has been available at the 600 V level for only a few years, but EPC entered the market in 2009 with the first commercial GaN HFET rated at low voltage [8]. Today, at least ten companies have commercial or near-commercial GaN power devices, and this number continues to climb. The technology of GaN power devices is a primary thrust of this dissertation, and more details will be covered in Chapter 3.

Lateral GaN devices have reached ratings up to 650 V and 90 A, while SiC MOSFETs occupy more of the high voltage and high power market segment. GaN and SiC together occupy a large area for both current and voltage, and WBG semiconductors can thereby enable efficient power electronics at power levels infeasible for conventional Si.

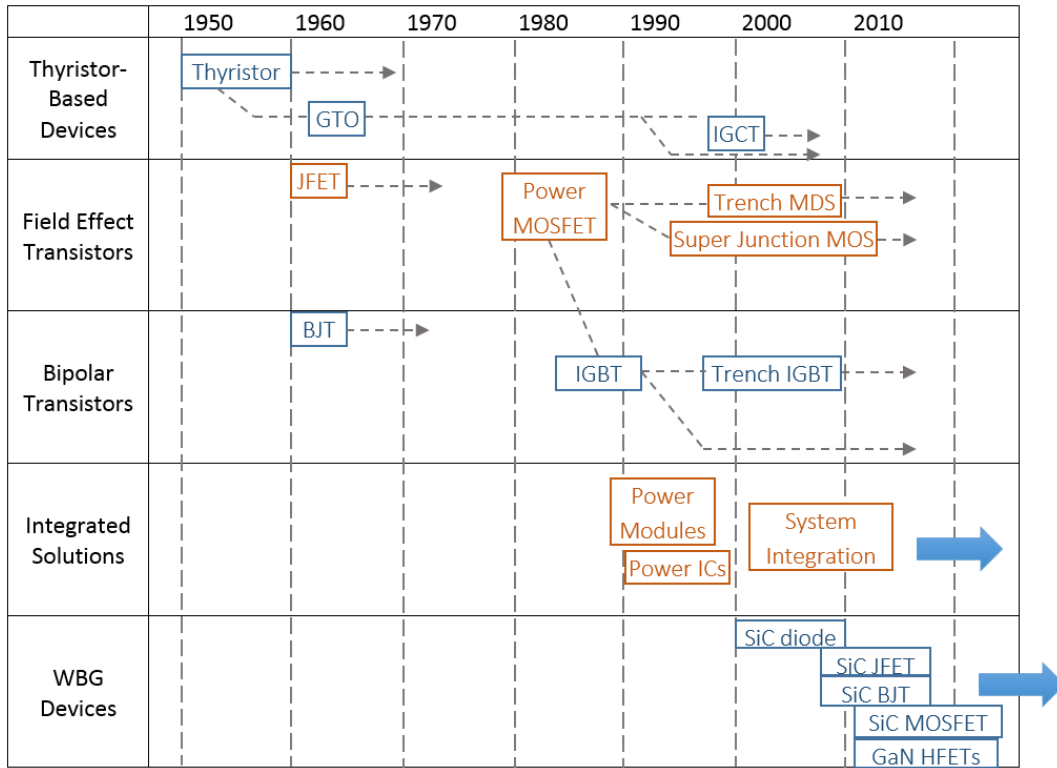


Figure 1.4. Timeline of the development of power semiconductor devices [9].

### 1.3 Benefits and challenges of WBG-based converters

As previously mentioned, the material properties of WBG semiconductors produce device-level benefits that can propagate into converter-level improvements. However, these benefits also carry new challenges with them, as shown Figure 1.5. The smaller die size makes it more difficult to extract heat from the packaged device, which in turn may require a more advanced thermal design. The faster turn-on and turn-off transients have benefits for switching loss, but the high voltage and current slew rates demand more attention to the board layout and gate driver design to prevent spurious switching events in parasitic circuit elements. These high slew rates and circuit parasitics also cause more severe voltage overshoots, which can reduce the effective voltage rating of the device [10-18]. The high current slew rate presents a particular challenge, because it requires a higher speed for overcurrent protection circuits, in addition to the potentially lower short-circuit

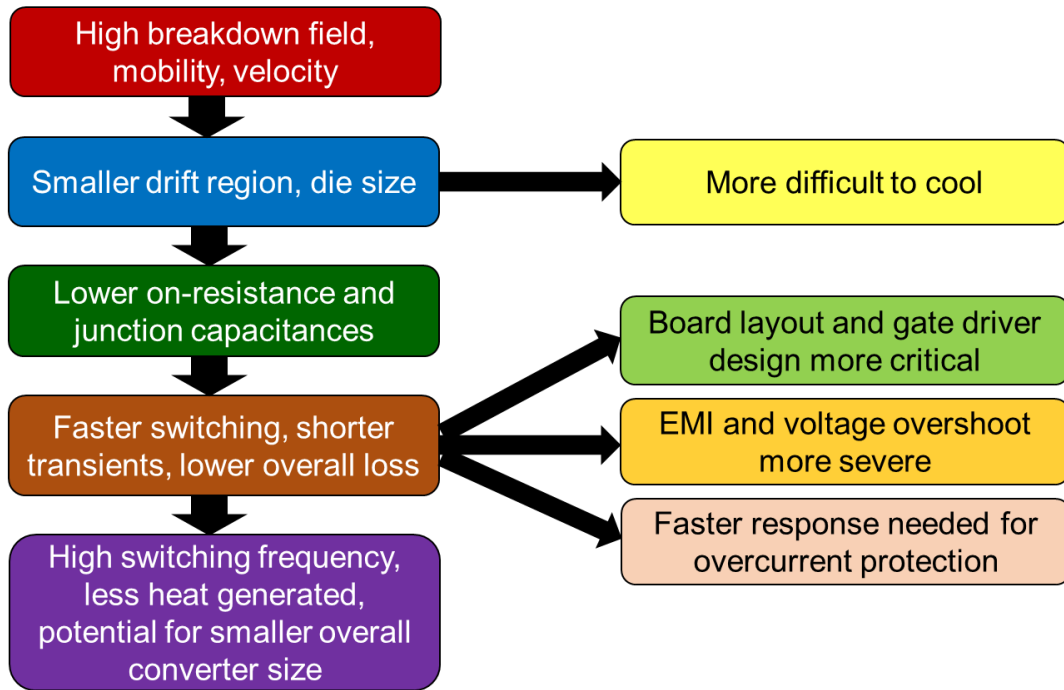


Figure 1.5. Benefits and challenges for WBG-based converters.

withstand capability of WBG devices due to their smaller die size [19-21].

#### 1.4 Motivations and objectives

The primary motivation for this work is to provide the tools necessary for implementing a GaN-based converter design, including a fundamental understanding of the device behavior, characterization of the static and dynamic performance of a GaN device, models describing the key impact factors in GaN switching behavior, and converter-level design considerations for maximum utilization of the device.

The first step is to provide a thorough user-oriented review of GaN power devices for an audience of power designers. Rather than discussing only device physics or converter design principles, this dissertation aims to bridge the gap between the two, providing the background necessary for a power electronics engineer to begin a project in GaN-based converter design. Because the availability of commercial GaN devices is rapidly changing, this review will cover



technology that is currently available and also recent developments that are targeted for near-term commercialization. Therefore, the material presented may be used to understand the uniqueness of commercial GaN devices available now, as well as provide the tools to identify and understand newer GaN technology as it continues to develop.

Once the underlying technology is explained, the methodology for experimentally capturing the characteristics of a specific GaN power device will be presented. Using the characterization results, a simplified model will be developed for the enhancement-mode GaN HFET, including equations governing the general switching behavior during turn-on and turn-off transients, as well as some unique properties of this device. Although this simplified model is not intended for simulation, the equations can be used to better understand and interpret experimental results. The model is aimed at understanding and explaining some of the trends and properties that were discovered during the characterization process, and are not explained by the conventional model of a MOSFET.

Finally, some of the key design challenges in a GaN-based converter design will be discussed, and solutions will be proposed for each. The first is a fast overcurrent protection scheme to protect GaN FETs from damage during short-circuit fault conditions. Second, the limitations on reducing voltage and current margins will be analyzed. Analysis and experimental characterizations of transient overshoot voltage will be presented to achieve this aim, and a thermal design will be proposed for bottom-cooled surface-mount GaN power devices. Identifying and overcoming these converter-level design challenges can be seen as an example of the preceding work's implementation, as it relied heavily on the characterization methodology and models presented here. Neither the protection scheme nor the margin reduction could have been achieved in this manner without detailed and accurate device characteristics.

### 1.5 *Organization of dissertation*

This dissertation is organized as follows. Chapter 2 reviews prior literature related to the key contributions of this work. Chapter 3 reviews GaN power devices, including the basic structure and properties of vertical and lateral devices, as well as the commercial status and design challenges associated with GaN power devices. Chapter 4 discusses the methodology for GaN device characterization, including both static and dynamic testing. Chapter 5 describes a methodology for characterizing the additional loss due to cross-talk in a GaN phase leg, and provides the results of a comprehensive study using a commercially available enhancement-mode GaN FET. Chapter 6 then continues that analysis and develops a simplified model for an enhancement-mode GaN FET, including the general switching behavior, interactions due to the Miller effect, and the impact of elevated temperature on the turn-on transient and loss. Chapter 7 proposes a new overcurrent and short-circuit protection scheme for GaN gate injection transistors. Chapter 8 describes the design process and key considerations for a GaN-based full-bridge single-phase inverter, which harnesses many of the preceding methodologies to reduce the current and voltage margins of the device. Finally, Chapter 9 summarizes the contributions presented and plans for future work.

## Chapter 2

### Literature Review

#### 2.1 *Reviewing a power device*

The review of GaN power devices is a major goal of this paper, so it is helpful to first consider the elements of a typical review paper for power devices. Device reviews were popular in the 1980's and 1990's to update the power electronics community on the state of the art [22-28]. These papers particularly include summaries of power MOSFETs and IGBTs, as well as other types such as SCRs, BJTs, IGCTs, GTOs, and MCTs. More recently, similar reviews such as [29] discussed the new Super Junction devices available from several manufacturers. These reviews vary widely in both scope and perspective. In some, specific focus is given to the physical structures and fabrication steps of the devices, with an intended audience of device physicists and manufacturers. Another type of review is on the other end of the spectrum, covering power electronics at a very high level. These reviews describe the latest device types as black boxes, without much depth into the internal structure of each, then summarize the applications of these devices in various converter topologies based on their properties.

Some application notes such as [30],[31] follow a different review format, because they serve another specific purpose. These also serve as reviews, each for one device from a particular manufacturer, and they may cover the full spectrum from the material properties to application recommendations. For example, [31] provides a thorough introduction to Infineon's CoolMOS C7 Super Junction MOSFET, including the fabrication structure and recent improvements of that particular device, properties of the device at a black-box level, and design concerns in a CoolMOS-based converter.

Since the advent of wide bandgap power electronics, device reviews have seen a second wave of popularity, covering materials such as SiC, GaN, and perhaps to a lesser extent diamond

and GaAs. These fit into a similar spectrum to the reviews mentioned earlier, from material properties to device applications [2],[4],[5],[32-34].

Even more specifically, there have been a number of reviews focusing on GaN power devices, which informs Chapter 3 of this dissertation. Some of these cover a range of GaN technologies for specific applications, such as electric vehicles [35],[36]. Others focus on one particular GaN technology by a single manufacturer [37-39]. Lastly, some GaN reviews describe the benefits and concerns of GaN devices in a particular circuit topology, such as resonant LLC or totem-pole PFC [40-42]. However, none of these reviews provide all of the necessary tools for a power designer's first GaN-based converter, so several of them must be read to cover the different aspects.

From surveying these previous review papers on GaN and other power devices, it is clear that a user-focused review of GaN HFETs should discuss the following topics:

- The material properties of GaN, as compared with the Si and SiC, and the advantages of these materials for power devices.
- The structures, behavior, and fabrication challenges of vertical devices, as well as a survey of commercial vertical GaN manufacturers.
- The structures and behavior of lateral devices, including a survey of the distinct device types used by commercial lateral GaN manufacturers, and the unique properties of lateral GaN such as diode-like reverse conduction behavior, dynamic  $R_{ds-on}$ , and breakdown mechanisms.
- Gate driver considerations for GaN power devices, such as the voltage and current capabilities, common mode transient immunity, and cross-talk mitigation.
- Converter-level considerations for GaN power devices, such as the reliability of the devices, thermal design, device packaging, PCB layout, large-scale device availability, and the overall switching behavior of the GaN devices as compared with conventional Si power devices.

## 2.2 *Characterization of wide bandgap power devices*

Characterization and modeling of power devices is often an integral component of graduate theses, such as in [10],[17],[43-48]. Often this characterization is performed for the purpose of developing or improving a model, or for optimizing the design of a particular converter topology. However, methodology for characterization of Si and SiC devices has been well-covered in these prior works. In particular, [47] details the test setup and measurements for a double pulse test, then [17] provides a thorough update of this methodology for SiC devices, and [46] performs a similar update for cascode GaN devices. Outside of theses, several works have provided methodology for characterization and modeling of GaN devices in particular [49-57].

Static characterization techniques are covered far less in existing literature, although references such as [30] have given thorough background on the characteristics of power MOSFETs and the significance of the different curves provided in typical device datasheets. Additionally, manufacturers of static characterization equipment such as [58] have detailed the operation of their equipment for general applications and some key tests that are particularly useful for WBG devices.

From these references, the following tests are applicable for characterization of enhancement-mode GaN devices at the 600 V level:

- 1) Pulse-based static measurements with a curve tracer
  - a) Output characteristic ( $I_d$ - $V_{ds}$ ) with fixed  $V_{gs}$
  - b) Transfer characteristic ( $I_d$ - $V_{gs}$ ) with fixed  $V_{ds}$
  - c) Leakage current ( $I_{d,off}$ - $V_{ds}$ ) with fixed  $V_{gs}$
  - d) Consideration of elevated junction temperature ( $T_j$ )
- 2) Capacitance measurements with an impedance analyzer
  - a) Output capacitance ( $C_{oss}$ ) vs.  $V_{ds}$
  - b) Input capacitance ( $C_{iss}$ ) vs.  $V_{ds}$

- c) Reverse transfer capacitance ( $C_{rss}$ ) vs.  $V_{ds}$
- 3) Dynamic characterization with a Double Pulse Test (DPT) circuit, as shown in Figure 2.1.
  - a) Measurement of  $v_{ds}$  and  $v_{gs}$  with passive voltage probes
  - b) Measurement of  $i_d$  with a coaxial current shunt
  - c) Calculation of switching energy loss during hard turn-on and hard turn-off transients ( $E_{on}$  and  $E_{off}$ ), at various operating points of  $V_{dc}$ ,  $I_L$ , and  $T_j$
  - d) Calculation of peak voltage overshoots and transient interval durations

Particularly in the case of DPT setup and measurement, several key issues were identified in prior literature that will affect the accuracy of characterization results:

- 1) Choosing voltage measurement probes and the current measurement shunt with sufficient bandwidth to measure the switching transient
- 2) Minimizing ground-lead inductance of voltage measurement probes with tip adapters
- 3) Reduction of common-mode ringing using chokes on all dc power supplies and measurement channels

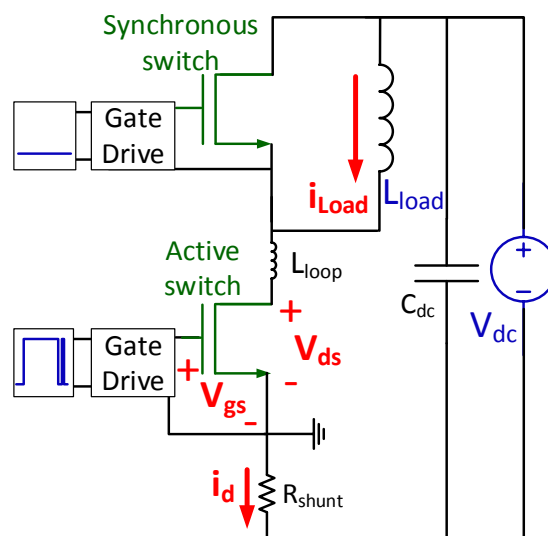


Figure 2.1. Double Pulse Test (DPT) circuit used for dynamic characterization.

#### 4) Proper I-V alignment through deskew of the current measurement channel

### 2.3 *Miller-induced cross-talk in a phase leg*

Cross-talk is a term sometimes used to describe the mechanism causing a false turn-on in the synchronous switch of a phase leg, during the turn-on transient of its complementary switch. More generally, it also involves the interactions between these two switches during a hard turn-off as well, although the more common concern is the turn-on case. This spurious turn-on of the synchronous switch channel occurs when the complementary switch's channel is also partially on, allowing a shoot-through current to flow from the dc supply into both devices of the phase leg, causing extra losses and even potentially a short-circuit fault condition (which may destroy one or both devices). This topic has been well covered in literature, including explanation of the physical mechanism, analytical models, considerations for device selection, and gate driving techniques to avoid the phenomenon [12],[13],[16],[18],[59-63].

Figure 2.2 from [18] shows an explanation of the cross-talk false turn-on phenomenon. When the low-side (active) switch turns on in a phase leg, its voltage must fall from  $V_{dc}$  to near 0 V. Simultaneously, the high-side (synchronous) switch voltage must increase from near 0 V to  $V_{dc}$ . This requires a charging current to flow through the drain-source capacitance ( $C_{ds}$ ) of the synchronous switch, and also through the Miller capacitance  $C_{gd}$ . The  $C_{ds}$  charging current is typically much larger than that of the Miller capacitance, due to the relative sizes of these junction capacitances. However, the Miller capacitance current must flow from the drain to gate, which means that it must also have a path to flow from the gate to source for a complete circuit. Some of this current may be available from the gate driver, which is connected at the gate and source, but the gate driver current is somewhat limited by

$$i_{drv} \approx \frac{v_{gs} - V_{drv-}}{R_{g,ext} + R_{g,int} + R_{pd}} \quad (2.1)$$

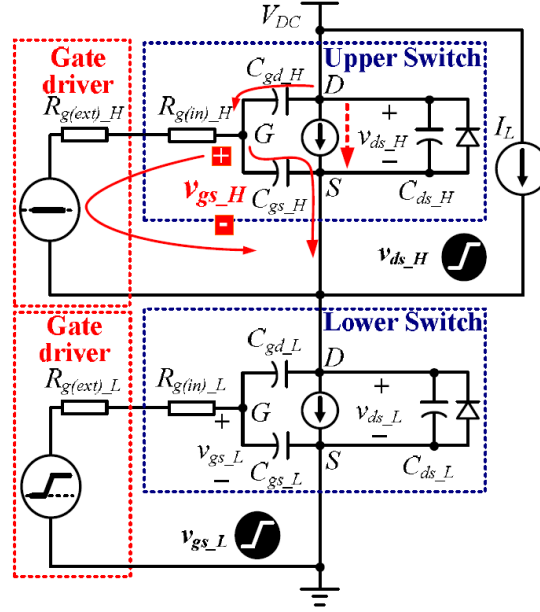


Figure 2.2. Mechanism causing false turn-on in the synchronous switch of a phase leg [18].

where  $V_{drv-}$  is the voltage supplied to the driver,  $v_{gs}$  is the instantaneous voltage on the gate,  $R_{g,ext}$  is the gate resistance of the driving circuit,  $R_{g,int}$  is the internal gate resistance inside the device package, and  $R_{pd}$  is the pull-down/sink resistance of the gate driver IC. At this time,  $v_{gs}$  should be equal to  $V_{drv-}$ , and this current should be zero.

Any additional charging current in  $C_{gd}$  will then flow through the gate capacitance  $C_{gs}$ . This will cause an increase in the gate voltage of the synchronous switch, according to

$$\frac{dv_{gs}}{dt} = \frac{i_{gd} - i_{drv}}{C_{gs}}. \quad (2.2)$$

As this causes a positive shift in the synchronous switch  $v_{gs}$ , some of the current may begin to flow through the driving loop according to (2.1). When the gate voltage is positively shifted above the threshold voltage, the synchronous switch channel begins to turn on, allowing a shoot-through current to flow from drain to source as indicated in Figure 2.2 [18].

The most straightforward method to prevent false turn-on is to choose devices with junction capacitances that are sized in such a way that the  $C_{gd}$  charging current can never charge  $C_{gs}$  beyond



the threshold voltage, according to

$$\frac{Q_{gd}}{Q_{gs,th}} < 1 . \quad (2.3)$$

where  $Q_{gd}$  is the Miller charge of the device at the dc voltage of the phase leg, and  $Q_{gs,th}$  is the gate charge required to bring  $v_{gs}$  to the threshold voltage. These values can be extrapolated from the device's gate charge characteristic, or calculated from the capacitance characteristic curves.

According to [16],[62], selecting devices that meet this criterion will prevent cross-talk from causing a false turn-on of the synchronous switch. However, it is more difficult to meet this criterion with newer WBG devices, where the gate capacitance is substantially lower than conventional Si MOSFETs. The cross-talk phenomenon can also be mitigated by providing a more negative off-state driving voltage, so that a positive shift in  $v_{gs}$  may still not bring it above the threshold voltage. Another technique involves using a high gate resistance for the active switch turn-on path, and a lower gate resistance for the synchronous switch turn-off path, so that the turn-on speed (and  $dv_{ds}/dt$ ) can be reduced, while also providing a low impedance gate loop for the synchronous switch Miller capacitance to charge. A third, more recently proposed technique, requires an active or multi-level gate driver to improve the driver's ability to provide sufficient current to the Miller capacitance without a positive gate voltage shift [60],[61],[63-65].

Despite these numerous techniques for cross-talk mitigation, the fast switching of WBG-based phase legs makes it difficult to completely eliminate the concern. In [13], an analytical model for predicting and explaining the extent of cross-talk is proposed, based on the capacitance curves of the device. An experimental methodology was proposed in [62] for evaluating the additional losses in a continuously operated buck converter, by applying a more negative off-state driving voltage on the synchronous switch and observing the change in overall converter loss.

## 2.4 Analytical models of transient device behavior

One of the most fundamental equations used in explaining the transient behavior in a phase leg is given by

$$\frac{dv_{ds}}{dt} = -\frac{V_{drv}-V_{Miller}}{R_g C_{gd}} \quad (2.4)$$

where  $V_{Miller}$  is the Miller voltage of the device [66]. This model, shown in Figure 2.3, rests on the assumption that the gate voltage does not change during the turn-on voltage fall time or turn-off voltage rise time, a phenomenon known as the “Miller Plateau.”

A contrary equation was proposed in [67], giving

$$\frac{dv_{ds}}{dt} = \frac{-g_{fs}(V_{drv}-V_{th})+I_L}{C_{ds}+(1+g_{fs}R_g)C_{gd}} \quad (2.5)$$

This model, shown in Figure 2.4, is still based on the Miller Plateau assumption, although it includes some allowances for variation of  $v_{gs}$  during the  $dv_{ds}/dt$  transient.

However, neither model considers the impact of  $C_{gs}$  or the output capacitance of the synchronous switch. These assumptions become increasingly unrealistic as the switching speed increases and the duration of the transient shrinks, particularly in WBG devices.

Other models have been developed extensively for Si, SiC, and GaN power devices, although these are typically intended for estimation of loss or simulation, and they are often physics-based or derived from experimental curve-fitting [37],[48],[49],[52],[57],[68-84]. These models provide great insight into the behavior of the devices studied in each paper, although they do not improve upon the relationships of (2.4) and (2.5) or provide an intuitive explanation of the  $dv_{ds}/dt$  transient behavior in a fast-switching power device.

## 2.5 Capacitive gate driver circuits for GaN GITs

The gate injection transistor (GIT) was originally developed by Panasonic and published in [85]. Despite the inherent depletion-mode nature of the GaN heterojunction structure, the GIT

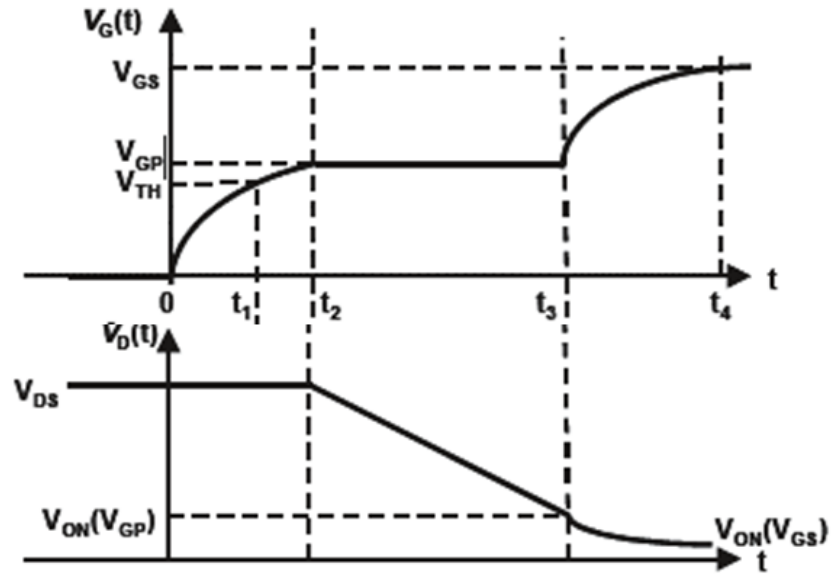


Figure 2.3. Turn-on transient model of  $v_{gs}$  and  $v_{ds}$  described by (2.4) [66].

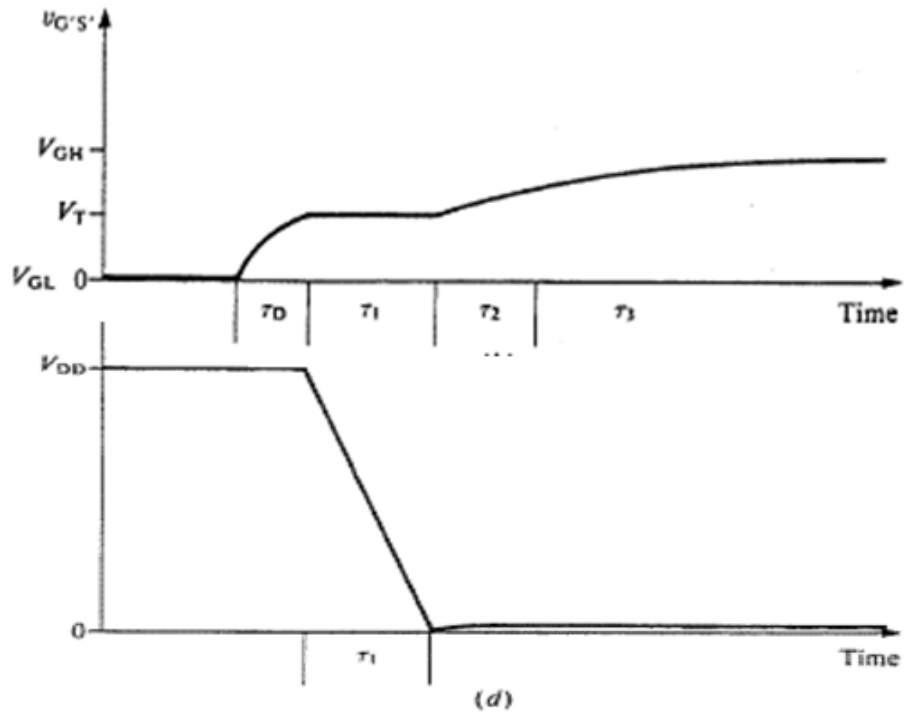


Figure 2.4. Turn-on transient model of  $v_{gs}$  and  $v_{ds}$  described by (2.5) [67].

behaves as an enhancement-mode FET due to the embedded diode created by a p-doped GaN layer beneath the gate. This junction between the p-GaN and AlGaIn must be forward biased in order to restore the 2-dimensional electron gas (2DEG) that was depleted by the junction's depletion region, and thereby complete the device channel. Therefore, the channel will remain in the cutoff region until a positive voltage is applied to the gate above the diode's forward voltage, and then a current will flow into the gate for the duration that the device is in an on-state. The internal gate voltage of the device is also clamped near to this forward voltage ( $\sim 3.5$  V), similar to the voltage clamping of a conventional diode.

This steady-state gate current and clamped gate voltage present a challenge for gate driver design. In order to turn the device on quickly and avoid heavy overlap losses, a higher gate voltage is desirable. Therefore, Panasonic developed a unique gate driving circuit that provides a short burst of dynamic gate voltage and current, followed by a low current-controlled gate voltage [86]. The first version of this circuit used discrete components as shown in Figure 2.5, producing the gate voltage and current characteristics shown in Figure 2.6.

The initial  $C_{gs}$ -charging current can peak as high as  $VCC/R_{g,on}$ , assuming that  $R_{g,on}$  is several orders of magnitude lower than  $R_{ig}$ . The duration and shape of this initial pulse depends on the time constant  $R_{g,on}C_s$ . As  $C_s$  becomes charged, the current through  $R_{g,on}$  falls to zero, and the remaining current is  $(VCC-V_{gs})/R_{ig}$ . This current is typically in the range of 10-50 mA. The parameters  $VCC$ ,  $R_{g,on}$ ,  $C_s$ , and  $R_{ig}$  can be tuned to produce the desired driving voltage shape. A separate path is provided for the turn-off gate resistance, which does not have a series capacitance, since no steady-state current is needed in the cutoff region [86].

More recently, Panasonic has commercially released an integrated version of this driving scheme, with a functional block diagram as shown in Figure 2.7 [87]. This IC featuring a built-in negative off-state voltage regulator, active Miller clamping, and an adjustable constant-current

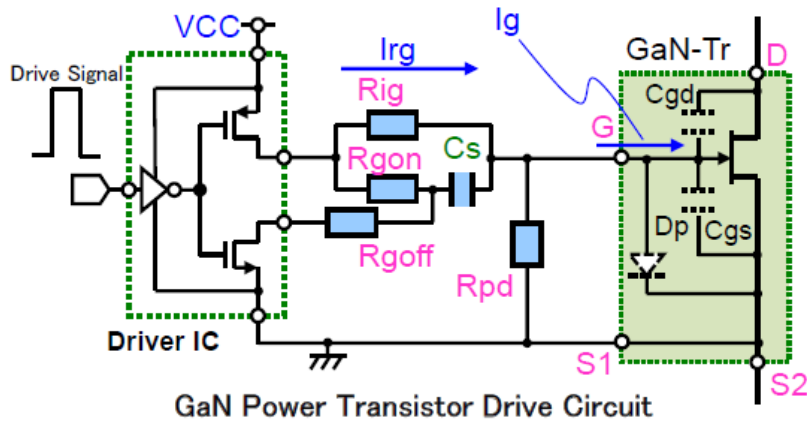


Figure 2.5. Recommended GIT gate drive circuit from Panasonic application note [86].

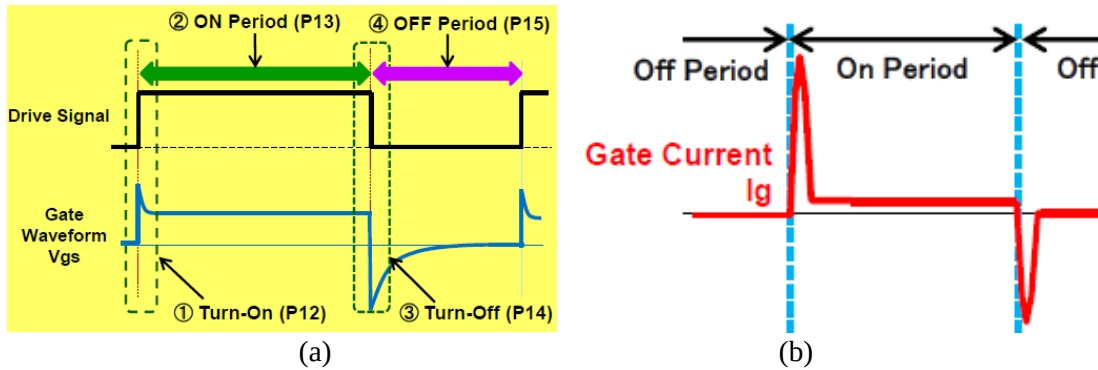


Figure 2.6. Expected gate voltage and current waveforms, when using recommended GIT gate drive circuit from Panasonic application note.

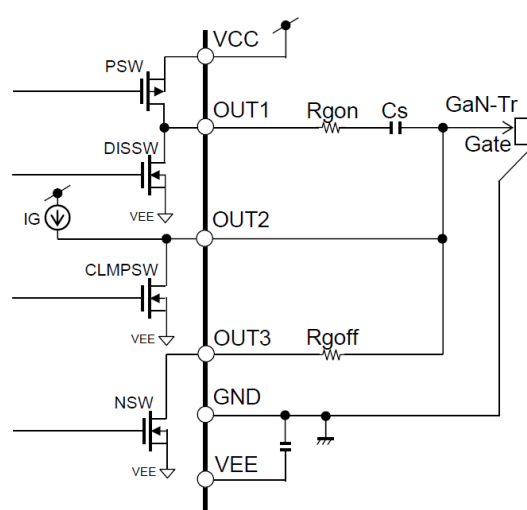


Figure 2.7. Functional block diagram of Panasonic x-GaN gate driver IC [87].

source for the steady-state turn-on output. However, the initial burst of dynamic  $C_{gs}$ -charging current is still accomplished with a series RC turn-on path.

## 2.6 *Overcurrent and short-circuit protection for GaN power devices*

The requirement of fast overcurrent and short-circuit protection for WBG devices has been shown to be much stricter than conventional Si devices. This can be explained by the much smaller die size, resulting in reduced thermal capacitance, and the potential for a more rapid spike in junction temperature [19],[21]. Recent literature has shown that a healthy GaN FET can be destroyed by a short circuit pulse as brief as 400-600 ns at 400 V [88-96], and in some cases even 200 ns [97-99]. This short-circuit capability increases significantly with lower bus voltages, but degradation may occur with any sustained short circuit condition.

Perhaps the most common overcurrent protection scheme is desaturation protection, shown in Figure 2.8 [21]. Desaturation protection requires sensing of the drain-source voltage, and triggers the gate driver to turn off when this voltage indicates that the device has entered the saturation region. This scheme is limited for several reasons: 1) a diode must be used to protect the sensing circuit from the much higher drain-source voltage when the device is in an off-state, which reduces the response time and adds capacitive loading to the output capacitance of the device; 2) the overcurrent threshold is set by the saturation current at the gate driver voltage and cannot be selected independently; 3) the threshold is also a strong function of junction temperature, so a much higher overcurrent threshold must be chosen for room temperature in order to guarantee protection at higher temperature. Desaturation overcurrent protection has been shown to function well for GaN in [100-102] with a total response time of  $\sim 200$  ns, but the desaturation detection circuit adds capacitive loading to the drain of the GaN device, increasing both the response time and the switching loss. In [101], a desaturation scheme was demonstrated for 600 V GaN devices, although with the modification that the  $v_{ds}$  threshold was chosen in the ohmic region. This allows for a lower

overcurrent protection threshold, but it also slows down the response time, since the slew rate of  $v_{ds}$  in the ohmic region is much lower than it is in saturation. The desaturation protection proposed in [102] used an overcurrent threshold of only 3 A, and [100] was designed for a 200 V rated GaN FET, so neither is directly applicable to a higher-rated 600 V GaN FET operating in the tens of amps range.

However, desaturation is not the only short-circuit or overcurrent protection scheme proposed for power devices. Another protection scheme was demonstrated for IGBTs and proposed for SiC MOSFETs in [21],[103]. This scheme, shown in Figure 2.9, is based on the voltage between the power source and Kelvin source terminals of the device. The voltage across the parasitic inductance between them represents  $L_s di_d/dt$ , so it is passed through an analog integrator so that  $i_d$  can then be sensed by a comparator for fault detection. This scheme relies on a large parasitic inductance existing between the source and Kelvin source terminals. With near-chipscale GaN FETs, the inductance may not be sufficient to implement this scheme. This issue was resolved in [104] by intentionally inserting a PCB-embedded inductor at the source terminal, but this work was

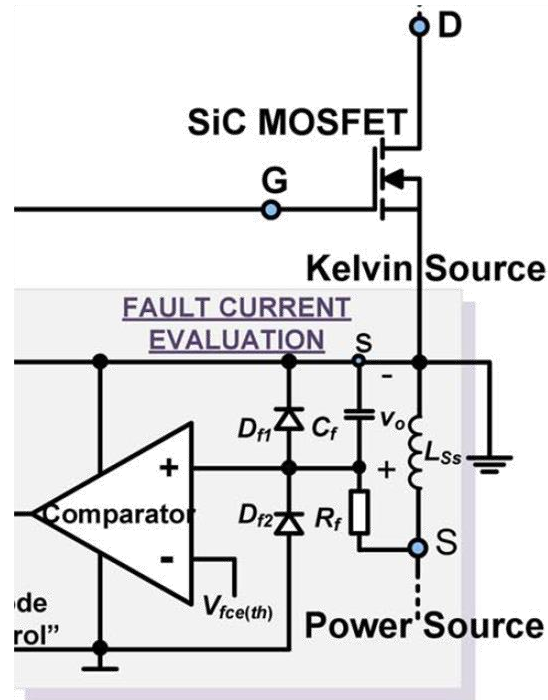


Figure 2.9. Schematic of a  $di/dt$  integration overcurrent protection scheme [21].

intended for double-pulse test characterization rather than continued operation of the converter.

An overcurrent detection and protection scheme for GaN FETs was proposed in [105], using an monolithically embedded shunt resistance to measure current at the die level, as shown in Figure 2.10. This solution obviously requires the fabrication of custom semiconductor dies, which may be costly. Similar solutions have been used in the past with discrete shunt resistors, although this scheme is difficult to implement due to extra losses, isolation concerns, and noise immunity [19].

Figure 2.11 shows an overcurrent protection scheme proposed for IGBTs, which relies on the unique gate charge characteristic that occurs in a short-circuit condition as opposed to a typical turn-on transient [106]. However, this requires dynamic measurement of gate current, and this scheme has not yet been verified in GaN FETs.



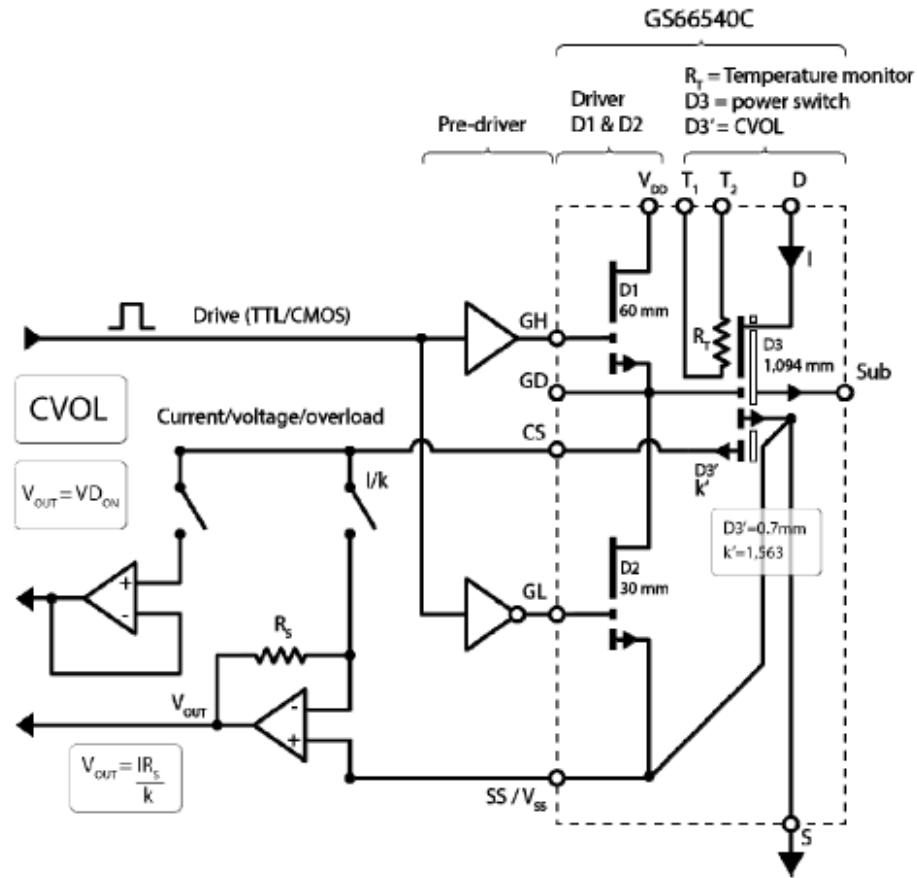


Figure 2.10. Schematic of a monolithical shunt based overcurrent protection scheme [105].

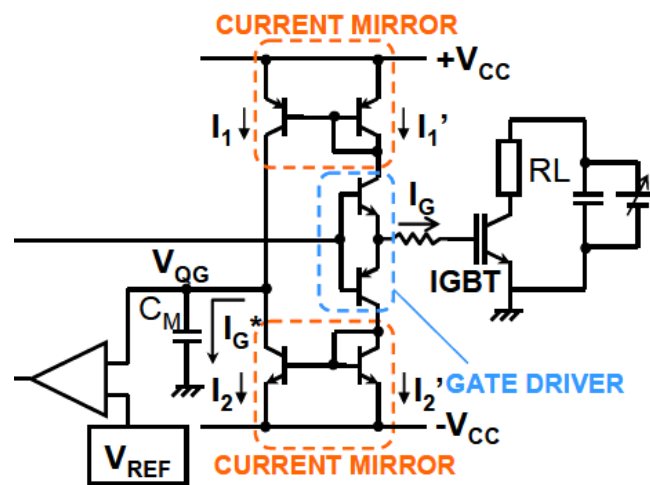


Figure 2.11. Schematic of gate charge based overcurrent protection scheme [106].

## 2.7 Thermal design for bottom-cooled power devices

The recommended thermal design for bottom-cooled devices is based on thermal vias, which are densely packed PCB vias intended to pull the heat out of the thermal pad of the device [107],[108]. Thermal vias allow a heatsink to be connected to the bottom side of the PCB, with an electrically insulating thermal interface material between the two. Copper planes in a multi-layer PCB can improve this design, as shown in Figure 2.12, by acting as heat spreaders to expand the effective heatsink connection below. An application note from GaN Systems [68] showed that with the design in this figure, the thermal resistance could be between 3.12 and 11.54 °C/W, depending on the density of vias, number of layers, and PCB thickness. The best case is the highest via density, thinnest PCB, and most copper layers. The Infineon application note [69] showed a lower thermal resistance of 1.2 °C/W for PCB thermal vias, although this could be attributed to the larger thermal pad on the ThinPak 8x8 package used in the example.

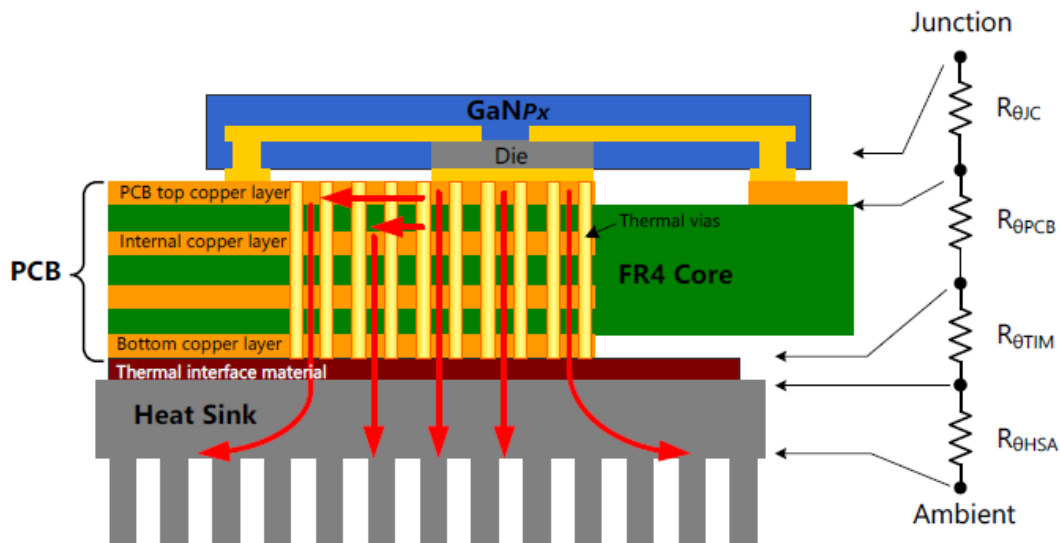


Figure 2.12. Bottom-side cooling design using thermal PCB vias [107].

Another approach, demonstrated by [109], replaces the thermal vias with a copper PCB inlay, or “heat slug,” to significantly reduce the thermal resistance between the device package and the heatsink. Figure 2.13 shows a diagram of this thermal design. In this case, the thermal resistance is much lower at 0.56 °C/W in total for two devices, including the thermal interface material. This demonstration used an extruded aluminum heatsink with a custom-machined rectangular projection on the top to provide a thermal standoff between the PCB and heatsink, which was necessary to prevent an accidental short-circuit and allow for utilization of the bottom side of the PCB.

A third approach can be found in literature about thermal design at the packaging level, using direct bond copper (DBC) to share electrical conduction and thermal conduction in a single copper area [110],[111]. This is more challenging to implement with already packaged devices, particularly with bottom-side cooling. Figure 2.14 shows an example of a DBC cooling scheme in a module, where the electrical connections are positioned on the top side of the chip, and the thermal connection is on bottom side. The ceramic DBC substrate is coated in copper on both sides, so this can also be used for the drain and source electrical connections with a custom-designed DBC board. However, it may be less practical to include the gate driver circuit in DBC, as it does not allow for convenient multi-layer design as in a PCB, and the gate loop must be very dense to limit parasitic inductance.

In addition to the thermal vias or heat slug, the thermal resistance of the device from junction to case ( $R_{\theta jc}$ ) must be considered, as well as the heatsink to ambient ( $R_{\theta sa}$ ). Both of these values vary with the structure and material properties, as well as with operating conditions. The junction-to-case thermal resistance of packaged devices has been shown to increase significantly as a function of temperature or power, including GaN devices as well as Si and other semiconductors [112-114]. This relationship can be explained by the thermal conductivity of the constituent materials that physically connect the junction to the case, including GaN, Si, and

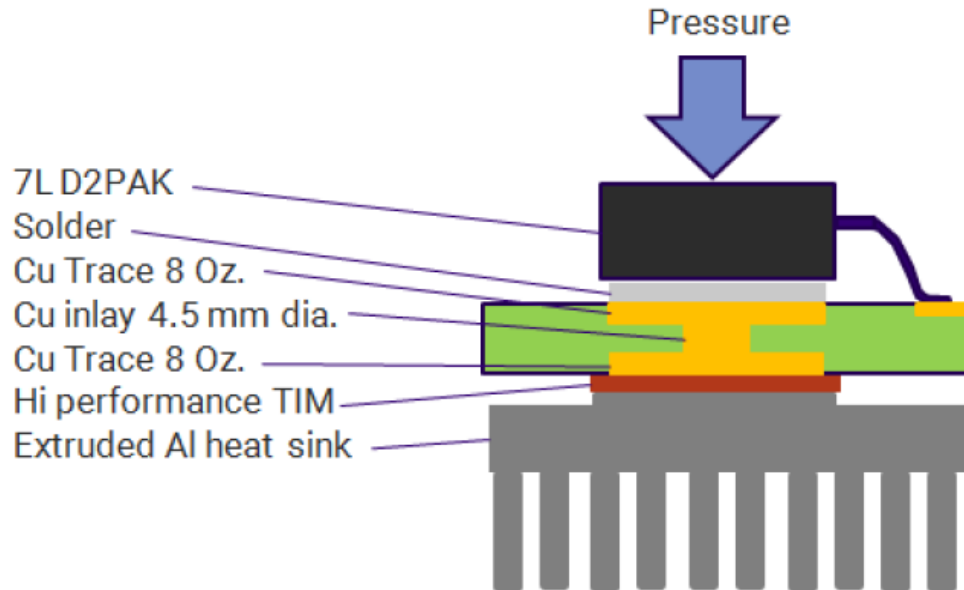


Figure 2.13. Bottom-side cooling design using copper PCB inlay [109].

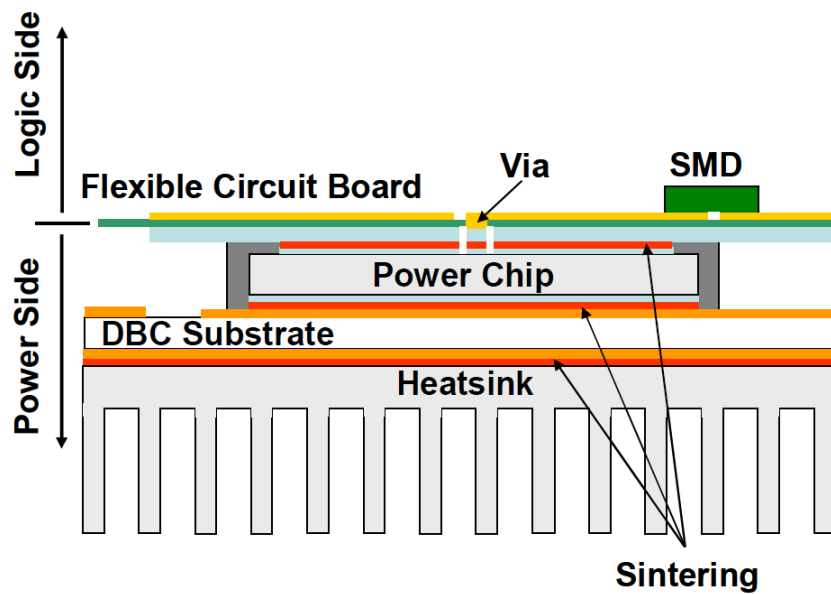


Figure 2.14. Example cooling design using direct bonded copper (SKiN) [111].

intermediate layers [115-118]. The thermal conductivities of both Si and GaN have been shown to decrease significantly in the range of 25 to 150 °C [119-121]. This variable thermal resistance over junction temperature is not typically reported in device datasheets, but it can be evaluated using the methodologies presented in [122],[123]. The thermal resistances in the entire thermal equivalent circuit can be calculated as a function of power by measuring the junction, case, heatsink, and ambient temperatures. Most of these temperatures can be directly measured with sensors, although the junction temperature must be calculated by measuring one of several temperature-sensitive electrical parameters (TSEPs) such as on-resistance, threshold voltage, or transconductance [124-127]. For GaN FETs in particular, recent work has shown that junction temperature can be accurately calculated based on the measured gate voltage at a known gate current [128],[129].

The thermal resistance of the heatsink also varies strongly with power, although in this case the thermal resistance decreases with higher power dissipation. In fact,  $R_{\theta,sa}$  has been explained previously as a function of the temperature rise  $\Delta T_{sa}$ , which is the difference between the heatsink temperature (at the point of contact with the device/interface) and the ambient temperature [130]. Other important factors include the baseplate dimensions (length, width, thickness), fin geometry (height, length, thickness, spacing), and air flow. The thermal resistance as a function of temperature rise will depend on these factors, because a higher temperature rise will impact the heat spreading and utilization of the entire heatsink. In the particular case of natural convection cooling, the fin geometry and overall heatsink orientation also determines the air flow generated by heat dissipation. Convection-cooled heatsinks must be oriented vertically to achieve the optimum thermal resistance, so that air movement from natural convection will draw heat along the entire length of the fins [131-136].

Finally, the heatsink must be attached to the device case in some fashion. In the case of bottom-cooled devices, this includes the thermal vias or heat slug as previously described, as well

as an additional layer of thermal interface material (TIM) that acts as an electrical insulator and a thermally conductive gap-filler. The thermal resistance of TIM varies with material properties, but it is generally lower with larger area, lower thickness, and higher compression [137],[138].

## Chapter 3

### Review of GaN Power Devices and GaN-Based Converter Design Challenges

#### 3.1 *Introduction*

Before designing power electronics with GaN power devices, it is useful to understand their characteristics and the challenges that typically accompany such a project. Several review and survey papers have been published on the relative characteristics of WBG devices, including the benefits and design challenges associated with each [5],[33],[139],[140]. Other reviews, such as [35],[37],[141-143], have provided useful background on GaN power devices and GaN-based converter design. Some of these reviews focus on one particular GaN technology or research direction, rather than covering the full range of commercial devices available today. In addition, the significant developments in the past few years require an update to these prior works. Therefore, this review aims to cover the aspects of GaN power devices that are relevant to the converter designer, as the landscape of commercially available devices continues to change. This includes explanation of device physics properties to an audience who may not have device physics backgrounds, as well as exploring converter design elements that are not commonly required for Si-based power electronics.

#### 3.2 *Vertical GaN devices*

Vertical GaN devices, using structures similar to their Si and SiC counterparts, can take greatest advantage of the superior GaN material properties. However, the lack of availability of high-quality, low-cost GaN wafers has limited these prospects. This section will review the recent progress in the commercialization of vertical GaN devices.

### 3.2.1 Vertical GaN device structures

Avogy and HRL have publicly disclosed efforts to develop and commercialize vertical devices through the Strategies for Wide Bandgap, Inexpensive Transistors for Controlling High-Efficiency Systems (SWITCHES) program, funded by ARPA-E [144].

The first vertical structures published by Avogy were diodes, including the Schottky diodes and p-n diodes shown in Figure 3.2. Schottky diodes have been developed with blocking voltage up to 600 V, as well as p-n diodes up to 1700 V [145]. P-n junction diodes were fabricated with relatively large die areas, up to 16 mm<sup>2</sup>, able to block 700 V and handle pulsed currents up to 400 A [146].

Avogy also developed a vertical GaN FET with 1.5 kV blocking capability and 2.3 A saturation current. The device, shown in Figure 3.2, is a combination of the conventional JFET structure and the heterojunction AlGaIn/GaN structure used in lateral devices. With a threshold voltage of 0.5 V, this device is enhancement-mode and therefore normally-off [147].

More recently, HRL published their successful fabrication of a vertical GaN-on-GaN MOSFET, with ratings of 600 V and 2 A [148]. This device structure is shown in Figure 3.3. The bare die was fully characterized in [149], including its static characteristics up to the device ratings, as well its switching performance when paired with a complementary SiC Schottky diode. Development of vertical GaN MOSFETs has been published recently by others in [150-152]. The key challenge for vertical GaN MOSFETs is achieving high voltage and current capability simultaneously due to the relative immaturity of GaN fabrication technology, although [152] was able to achieve a blocking voltage of 1605 V with over 25 A verified current capability.



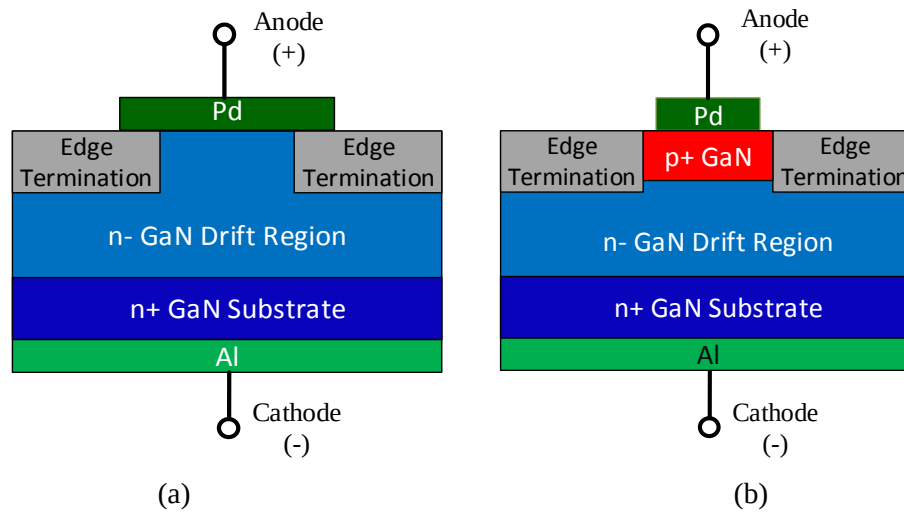


Figure 3.1. Vertical GaN-on-GaN diodes, including (a) Schottky and (b) p-n junctions [145].

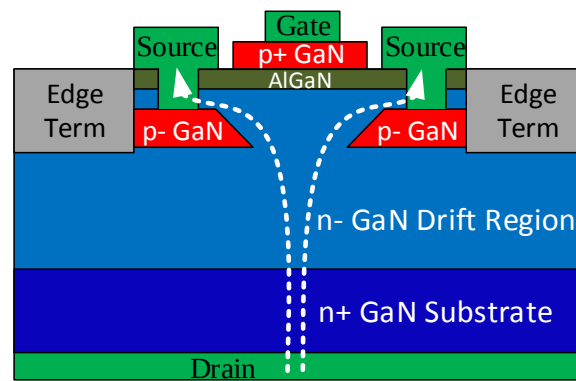


Figure 3.2. Vertical GaN-on-GaN normally-off JFET [147].

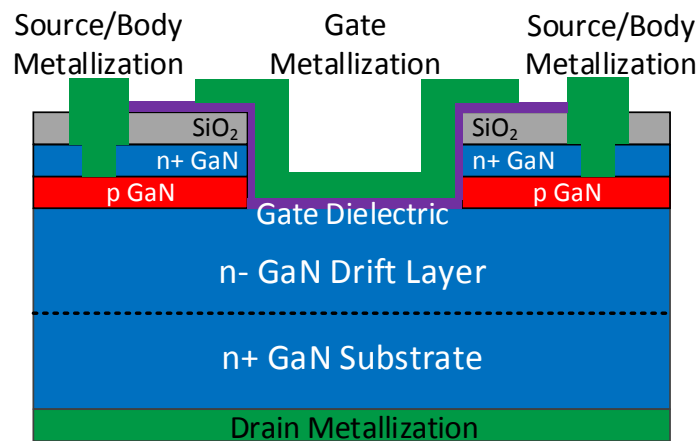


Figure 3.3. Vertical GaN-on-GaN trench MOSFET [148].

### 3.2.2 *GaN wafer fabrication*

Although wafer fabrication itself is not relevant in the converter design process, affordable GaN wafers are an important step toward commercialization of vertical GaN devices. These wafers form the substrate of a GaN-on-GaN device, on which the drift region is epitaxially deposited. As opposed to the melt-growth method used to produce Si wafers, GaN wafers are typically produced using hybrid vapor-phase epitaxy (HVPE) or chemical vapor deposition (CVD) on a foreign material such as sapphire. The foreign material is then removed, leaving only the GaN layer of the wafer. This process is sometimes referred to as “pseudo-bulk” wafer fabrication, and presents many challenges due to the lattice mismatch between GaN and the foreign material [153].

Other technologies are currently being researched to fabricate true bulk GaN wafers, without the need for foreign substrates. The three most promising technologies are high nitrogen pressure solution growth (HNPSG), low pressure solution growth with sodium flux (Na-flux), and ammonothermal growth. HNPSG and Na-flux methods have been used to produce GaN on foreign substrates with several inches in diameter, and more limited success in producing true bulk GaN. Ammonothermal growth has been the most successful in production of bulk GaN, with over two inches in diameter fabricated in boule form. Each of these methods has its own challenges, as shown in Table 3.1.

Figure 3.4 shows the relative cost and growth rates of GaN wafers from vapor and ammonothermal methods based on current predictions, as compared to Si wafers produced with seeded melt-growth and SiC wafers produced with seeded sublimation. The ammonothermal method has the potential to drastically reduce the cost of GaN wafer fabrication at the production scale, but the current cost for small-scale ammonothermal GaN growth cannot compete with more established hybrid vapor phase epitaxy [153].

Table 3.1. Comparison of GaN wafer fabrication methods [153].

| Fabrication Method | Approximate Growth Rates |        | Largest Crystal Size |          | Defect Density   | Challenges                                                          |
|--------------------|--------------------------|--------|----------------------|----------|------------------|---------------------------------------------------------------------|
|                    | $\mu\text{m/hr}$         | mm/day | On Substrate         | Boule    | $\text{cm}^{-2}$ |                                                                     |
| HVPE               | 100                      | 2.4    | > 6 inch             | --       | 105-106          | Stresses, wafer curvature, growth front breakdown, growth direction |
| HNPSG              | 3                        | 0.07   | 2 inch               | Few mm   | 101-102          | Scaling, growth rates, purity                                       |
| Na-Flux            | 30                       | 0.7    | 4 inch               | Few mm   | 102-105          | Scaling, sustained growth rates                                     |
| Ammonothermal      | 4                        | 0.1    | --                   | > 2 inch | 104              | Growth rates, purity                                                |

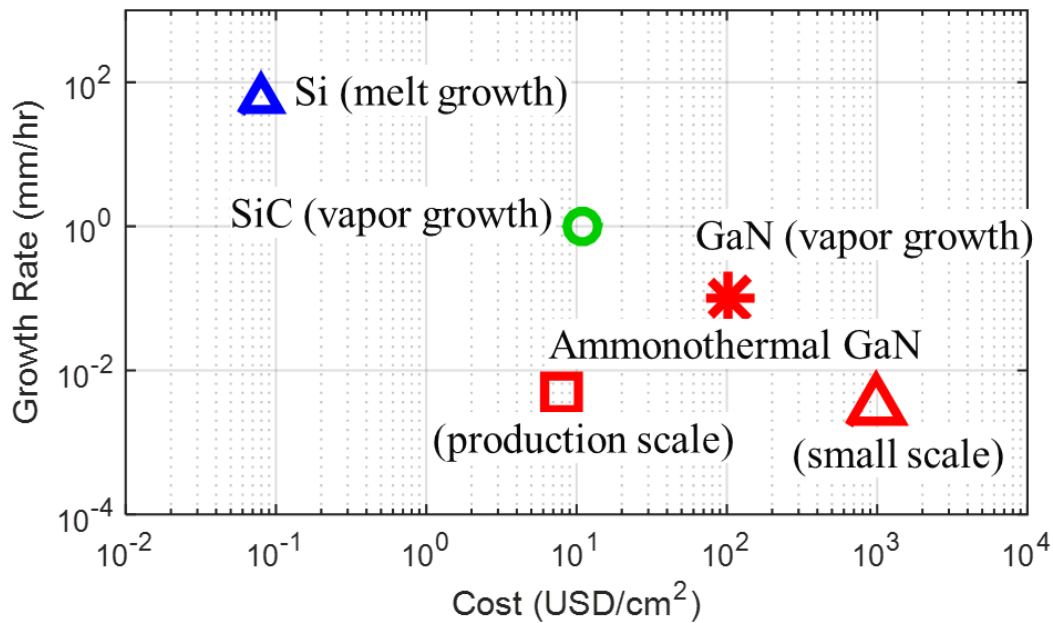


Figure 3.4. Cost and growth rate comparison of wafers with different growth techniques [153].

Vertical GaN devices require doping of the GaN material, which is achieved with impurities in Group IV (Si, C) for n-type GaN and Group II (Mg) for p-type GaN. These impurities create hole or electrons at the Ga site in the GaN crystal lattice [154],[155].

### 3.3 The lateral GaN HFET

Because vertical GaN devices have not yet been produced on a commercial level, most of the GaN devices available today are lateral heterojunction field-effect transistors (HFETs), also known as high electron mobility transistors (HEMTs). These devices are typically rated at 600-650 V. Because of the lateral heterojunction structure, these devices are fundamentally different from MOSFETs and have unique characteristics.

#### 3.3.1 Basic device structure

Figure 3.5 shows the basic structure of the GaN HFET. The principle feature of this structure is the AlGaIn/GaN heterojunction. At the interface between these two layers, a layer of high-mobility electrons called “two-dimensional electron gas” (2DEG) forms as a result of the crystal polarity, and is also augmented by piezoelectric crystal strain due to the lattice mismatch between AlGaIn and GaN. The 2DEG forms a native channel between the source and drain of the device.

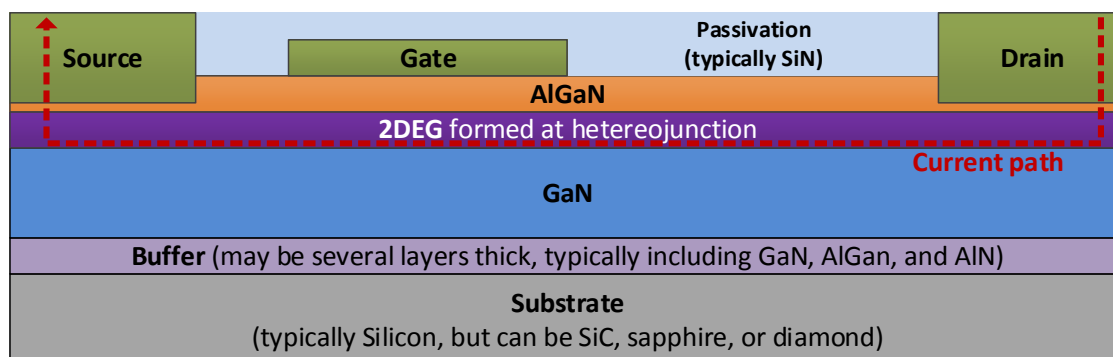


Figure 3.5. Basic structure of depletion-mode lateral GaN HFET (not drawn to scale) [141].

The substrate is typically Si, but other materials such as SiC, sapphire, and diamond can be used. In order to deposit the GaN layer on the substrate, a buffer layer must first be deposited that provides strain relief between the GaN and the foreign material. This buffer often includes several thin layers of GaN, AlGaIn, and AlN [141].

Because of the native 2DEG channel, the HFET is inherently a depletion-mode (normally-on) device. This is not desirable for voltage-source converters, because of the potential for shoot-through during startup or loss of control power. Several methods have therefore been used to fabricate normally-off GaN HFETs [141].

### 3.3.2 Cascode HFETs

A normally-off GaN device can be made with a depletion-mode HFET, using the cascode structure shown in Figure 3.6. A cascode device requires co-packaging of the depletion-mode HFET with a low-voltage enhancement-mode MOSFET. The two dies are connected in such a way that the output (drain-source) voltage of the MOSFET determines the input (gate-source) voltage of the HFET. Both devices share the same channel current while on, and the blocking voltage is distributed between them while off.

The two dies are connected inside the package with wire bonds or in a planar architecture.

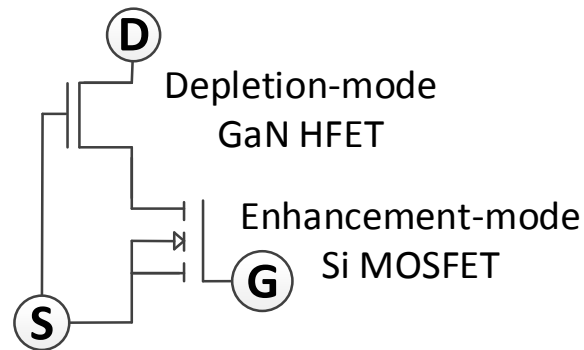


Figure 3.6. Device structure for the normally-off GaN cascode.

The switching performance of the cascode device relies heavily on the parasitic inductances in the package, especially between the two dies, and also on how well the junction capacitances of the two are matched. If the inductances are too high, or the capacitances are not matched well, the switching losses can increase significantly.

Table 3.2 shows the commercial status of cascode GaN devices. Transphorm is the only vendor currently selling cascodes on a large scale, although International Rectifier and MicroGaN have produced engineering samples. All three are rated at 600 V and use GaN-on-Si HFETs. MicroGaN has also produced a version of their cascode that acts as a diode rather than a FET [38],[156-161].

RFMD was selling engineering samples of their 650 V GaN-on-SiC device in 2014, but has since discontinued this product line. The use of a SiC substrate allowed for improved performance over GaN-on-Si cascodes, but this is not as common as GaN-on-Si due to the higher cost of SiC wafers.

### 3.3.3 *Enable switch*

Texas Instruments and VisIC were also included in Table 3.2, but it is important to note that they do not use the cascode circuit described in Figure 3.6. However, these devices utilize a similar concept, where a depletion-mode GaN HFET is connected in series with a lower voltage Si MOSFET inside the package to create a normally-off device. The key difference between these devices and a conventional cascode is that the low-voltage MOSFET is used here as an “enable switch” that is only turned off when the gate driver experiences a loss of power. The typical concern with depletion-mode transistors in power electronics is the potential for shoot-through during the system startup or accidental loss of control power. The “enable switch” GaN FET used by TI and VisIC avoid this risk by utilizing a cascode-like structure, although only the depletion-mode GaN is switched during normal operation. In this way, the full capabilities of a depletion-mode GaN

Table 3.2. Commercial cascode and enable-switch GaN FETs

| Manufacturer                 | Voltage Rating (V) | Current Rating (A) | $R_{ds-on}$ (m $\Omega$ ) | $Q_g$ (nC) | Package     | Availability    |
|------------------------------|--------------------|--------------------|---------------------------|------------|-------------|-----------------|
| Transphorm [156]             | 600-650            | 9-26               | 72-290                    | 6-14       | PQFN/TO-220 | Online ordering |
|                              |                    | 35-50              | 35-49                     | 28         | TO-247      |                 |
|                              |                    | 70                 | 34                        | 28         | HB Module   |                 |
| International Rectifier [38] | 600                | 10                 | 125                       | --         | PQFN        | Discontinued    |
| MicroGaN [158]               | 600                | --                 | 320                       | --         | TO-263      | Samples         |
| RFMD/Qorvo [159],[160]       | 650                | 25                 | 85                        | 16.2       | PQFN        | Discontinued    |
|                              |                    | 30                 | 45                        | 15.7       | TO-247      |                 |
| Fujitsu [161]                | 500                | --                 | 100                       | 14         | TO-220      | Unknown         |
| Texas Instruments [162]      | 600                | 12                 | 70                        | N/A        | PQFN        | Online ordering |
| VisiC [163],[164]            | 650                | 14-80              | 18-150                    | 9-35       | PQFN        | Samples         |
|                              | 1200               | 50                 | 40                        | N/A        | Module      |                 |

FET can be harnessed, but it performs as a normally-off switch at a system level.

VisiC offers devices that can be driven by a conventional MOSFET gate driver, and both companies offer modules with an integrated gate driver or buffer inside the device package. VisiC offers a 1200 V option, although this is actually two dies in series with a shared gate driver. [162-164].

### 3.3.4 Enhancement-mode HFETs

Although the 2DEG makes the lateral HFET natively depletion-mode, the gate can be modified to shift the threshold voltage positively and thereby make an enhancement-mode device. Several companies have produced e-mode GaN devices, and Table 3.3 lists a selection of these as well as their commercial availability at this time.

Most of these companies have published papers that show their device structure, and explain how their devices achieve a positive threshold voltage. Figure 3.8 shows some of these published techniques, which are used to deplete the 2DEG carriers beneath the gate when no voltage is applied. A positive voltage above the threshold is then required to enhance this depleted 2DEG beneath the gate and complete the channel.

Table 3.3. Commercial enhancement-mode GaN FETs

| Manufacturer             | Voltage Rating (V) | Current Rating (A) | $R_{ds-on}$ (m $\Omega$ ) | $Q_g$ (nC) | Package                | Availability        |
|--------------------------|--------------------|--------------------|---------------------------|------------|------------------------|---------------------|
| EPC [165]                | 15-80              | 1-90               | 1.5-480                   | 0.1-19     | Near-chipscale (LGA)   | Online ordering     |
|                          | 100-150            | 1.7-90             | 3.2-550                   | 0.1-13.2   |                        |                     |
|                          | 200                | 5-48               | 10-100                    | 1-8.8      |                        |                     |
| GaN Systems [166]        | 650                | 7.5-60             | 25-200                    | 1.5-12.1   | Near-chipscale (GaNpx) | Online ordering     |
|                          | 100                | 45-90              | 7-15                      | 6.2-12     |                        |                     |
| Panasonic [39],[167-169] | 600                | 15                 | 65                        | 11         | TO-220                 | Samples             |
|                          |                    | 13-26              | 56-140                    | 12-32      | DFN                    | Online ordering     |
| Infineon                 | 600                | 31                 | 55                        | 6          | TOLL/DSO               | Samples             |
| HRL [170],[171]          | 1200               | 10                 | 500                       | --         | --                     | Licensed to Navitas |
|                          | 600                | 10                 | 350                       | --         | --                     |                     |
| Navitas [172-175]        | 600                | --                 | --                        | --         | --                     | Samples             |
| Exagan [176]             | 600                | 100                | --                        | --         | --                     | Unknown             |
|                          | 1200               | 100                | --                        | --         | --                     |                     |
| Powdec [177]             | 1200               | 16                 | --                        | --         | --                     | Unknown             |

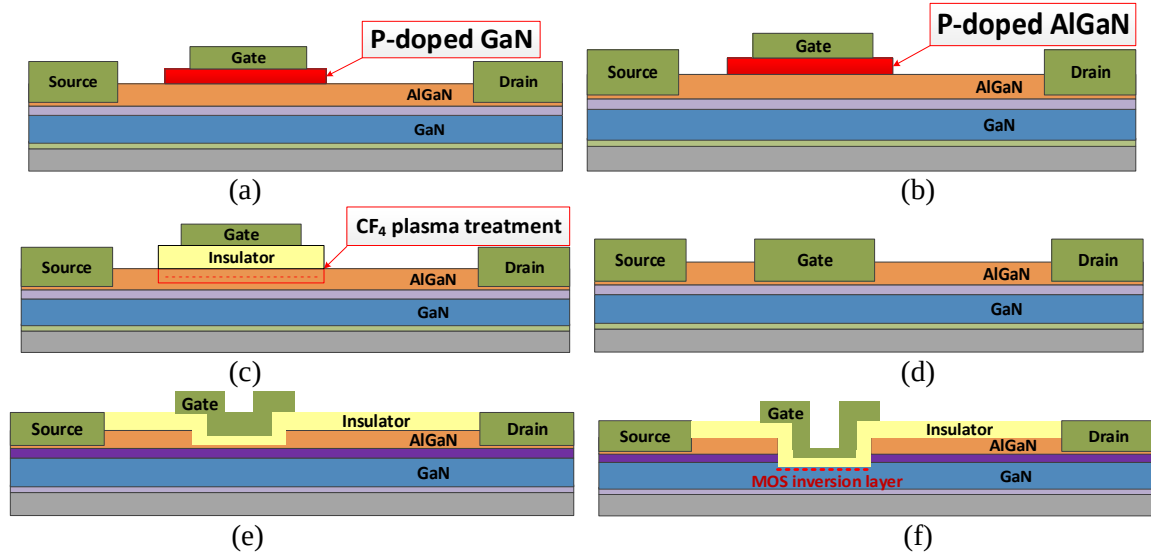


Figure 3.7. Gate modification techniques for enhancement-mode GaN HFETs, (a) P-doped GaN, (b) P-doped AlGaN, (c) Plasma treatment, (d) Recessed gate, (e) Insulated recessed gate, (f) Hybrid MIS-HFET [35],[37],[163],[167],[170],[171],[176-178].



EPC uses a p-doped layer of GaN beneath the gate as shown in Figure 3.7 (a), which creates a diode-like characteristic on the gate that shifts the threshold up by the magnitude of the diode voltage drop [37]. Panasonic and Infineon also use a p-doped layer of GaN in their latest x-GaN Gate Injection Transistors (GITs), although an earlier version of the GIT used p-doped AlGaIn rather than GaN as shown in Figure 3.7 (b) [39],[167],[168],[179]. One key difference between these two methods is the forward voltage drop on the gate before steady-state gate current begins to flow, which may be due to the etching depth beneath the p-doped GaN layer. The EPC diode knee occurs at  $\sim 5$  V, whereas the GIT's diode knee occurs at  $\sim 3$  V. The EPC device is typically driven with 4.5-5 V, just below the knee when diode current begins to increase. The GIT is typically driven above the knee where several mA of steady-state current flows into the gate. This intentional injection of minority carriers enhances the conductivity of the 2DEG and reduces on-resistance, but it also increases the complexity of gate drive design [39],[165],[167],[168].

HRL first used plasma treatment to deposit fluorine ions beneath the gate as shown in Figure 3.7 (c), effectively depleting the 2DEG until it is re-enhanced by a positive gate voltage [170]. However, HRL's later devices use a recessed gate as shown in Figure 3.7 (e) [171]. This technique involves etching away the AlGaIn beneath the gate to a precise depth, then replacing it with an insulating material. HRL chose AlN as the gate insulating layer. In 2015, HRL licensed its lateral GaN technology to Navitas Semiconductor [180].

Recessed gates are used by several other manufacturers as well, including Exagan and NEC, usually in conjunction with other modifications to further increase the threshold voltage [176],[181]. Sanken has developed devices using a non-insulated recessed gate as shown in Figure 3.7 (d) [182],[183].

Figure 3.7 (f) depicts another option for enhancement-mode devices, a hybrid MIS-HFET. This structure requires etching past the AlGaIn layer, and permanently removing the 2DEG beneath

the gate. The 2DEG remains on the drain-side and source-side of the channel, but the two sides must be connected by a MISFET inversion layer beneath the gate in order to turn on the device [35]. Powdec has published an enhancement-mode structure that is similar to a cascode, but the lower-voltage MOSFET is fabricated on the top surface of the GaN device next to the HFET gate [177].

### 3.3.5 *Reverse conduction behavior*

A MOSFET's body diode provides a path for reverse conduction through the p-n doping of the body and drift regions. The GaN HFET does not have a body region or doping in the drift region, so there is no body diode. However, there are reverse conduction mechanisms in both cascode and e-mode GaN devices.

In a cascode device, the body diode of the low-voltage Si MOSFET will turn on when the cascode is reverse biased. The Si body diode will then turn on the channel of the GaN HFET. In this way, the cascode approximates the behavior of a body diode. The reverse recovery charge of the low-voltage MOSFET is much less than that of a power MOSFET, so the additional switching losses due to reverse recovery are relatively low.

An enhancement-mode HFET has no body diode at all, but it demonstrates a mechanism that has been called “self-commutated reverse conduction” (SCRC) or “diode-like behavior” (DLB). The key to this mechanism is the symmetry of the device. The channel will turn on when the gate-source voltage  $V_{gs}$  exceeds its threshold,  $V_{gs,th}$ , and it will similarly turn on when the gate-drain voltage  $V_{gd}$  exceeds its own threshold voltage,  $V_{gd,th}$ . If the output of the device is reverse biased, the gate-drain voltage will be

$$V_{gd} = V_{gs} - V_{ds} . \quad (3.1)$$

When the gate-drain voltage exceeds the threshold voltage  $V_{gd,th}$ , which is typically close to the specified  $V_{gs,th}$ , the e-mode device channel will turn on and allow reverse current to flow. The voltage drop in DLB mode will then be

$$V_{sd} = V_{gd,th} - V_{gs} + I_d R_{sd,rev} \quad (3.2)$$

where  $R_{sd,rev}$  is the effective channel resistance in DLB.  $R_{sd,rev}$  is typically higher than  $R_{ds,on}$  and similarly varies with  $T_j$ ,  $V_{gs}$ , and  $I_d$ . When  $V_{gs} < V_{gs,th}$ , reverse current forces the device into saturation, but only just past the knee between ohmic and saturation regions. A more negative  $V_{gs}$  drives the device even further into saturation, and  $R_{sd,rev}$  becomes more dominated by the reverse transconductance rather than the ohmic on-resistance. Therefore, applying a negative off-state driving voltage is often undesirable for e-mode GaN devices, because the DLB voltage drop and resistance will increase. Figure 3.8 shows a typical characteristic for e-mode device, including DLB with 0 V and -2 V applied to  $V_{gs}$  [141].

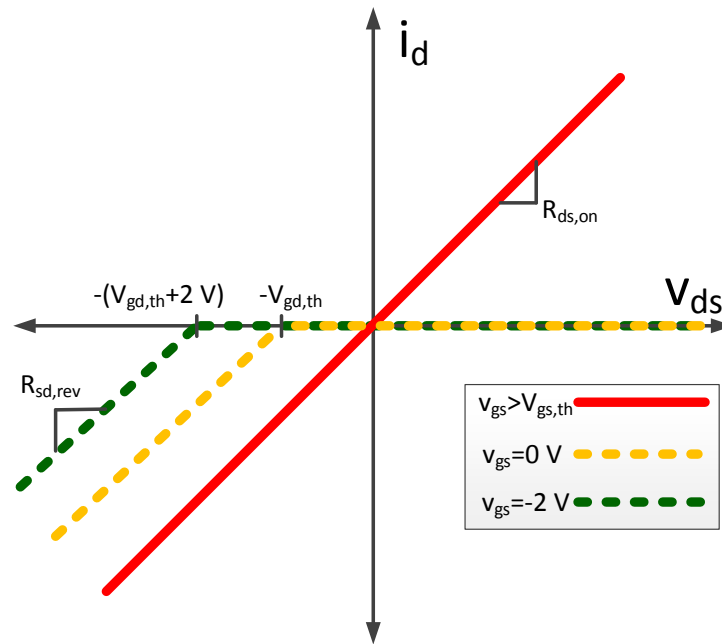


Figure 3.8. Reverse conduction characteristic of an e-mode GaN HFET.

Compared to the voltage drop on a MOSFET body diode, the total DLB  $V_{sd}$  is often quite high (3-5 V). E-mode GaN conduction losses may become excessive during long dead times. However, this “diode-like behavior” does not actually contain a diode, so there are no reverse recovery losses during switching. The lack of reverse recovery also reduces the dead time required to ensure ZVS switching, which is especially useful in soft switching applications [40].

Another option for either cascode or e-mode devices is to pair the HFET with an antiparallel Schottky diode, as is common with IGBTs. This will increase the output capacitance of the device, and therefore increase switching loss, but it may be a practical solution for some applications. In such a case, it is beneficial to package the diode with the HFET to minimize parasitics and reduce overall size [184]. The relative merits of adding an antiparallel diode or utilizing the DLB mechanism were compared in [185],[186]

### 3.3.6 Dynamic $R_{ds-on}$

Current collapse has been a widely reported phenomenon for lateral GaN devices, causing a temporary increase in on-resistance that is proportional to blocking voltage. This dynamic  $R_{ds,on}$  occurs primarily through two mechanisms, demonstrated in Figure 3.9. The first is trapping of surface charges near the drain-edge of the gate terminal when the device is in its off-state. The lateral structure causes the gate-drain electric field to be strongest near the gate edge, and impurities in the surface passivation and interface trap these charges temporarily. During the following on-state, these trapped charges act as a “virtual gate,” weakening the 2DEG until they are released. The second mechanism is the injection of “hot electrons” into even deeper traps within the device, particularly in traps caused by carbon doping in the buffer layer. These trapped charges also weaken the 2DEG and increase  $R_{ds,on}$ , and may cause long-term degradation to the device. Both of these effects are proportional to blocking voltage, and the hot electron effect has also been shown to increase with higher switching energy loss [187-189].

Measurement and characterization of dynamic  $R_{ds,on}$  is challenging, because it requires accurate measurement of  $V_{ds}$  in the 0.1-V scale immediately after falling from several hundreds of volts. This can be accomplished by clamping the measurement node at a low voltage during the off-state, using a diode-based or active clamping circuit, then unclamping the measurement node voltage after turn-on. However, this clamping action causes ringing in the measurement that may require several hundred nanoseconds to dampen. Because dynamic  $R_{ds,on}$  is a very time-dependent phenomenon, it is important to capture this measurement as early as possible. A comprehensive study of dynamic  $R_{ds,on}$  over several operating conditions was performed in [190] using this clamping technique. Temperature, load current, and bus voltage are all significant factors. Also, switching frequency and duty cycle have a major effect on the overall increase in dynamic  $R_{ds,on}$  during a switching period. Therefore, additional conduction losses due to this phenomenon could be easily misdiagnosed as switching loss.

GaN device manufacturers have made much progress in mitigating current collapse, primarily through the use of field plates. Each manufacturer may use a different structure and combination of field plates. Source and gate field plates help to redistribute the gate-drain electric field away from the gate edge. An example of basic field-plate structure is shown in Figure 3.10. The Si substrate can also act as a bottom field plate if it is connected to the source, which has been demonstrated to significantly improve the dynamic  $R_{ds,on}$  [191],[192]. Some manufacturers internally connect the substrate and source of their GaN HFETs, while others choose to electrically isolate the Si substrate to prevent current from flowing through it. If a separate thermal pad is provided in the device package, the manufacturer may recommend that the substrate be externally source-connected to help mitigate current collapse [193],[194]. The recent HD-GIT developed by Panasonic uniquely adds a second p-doped drain contact next to the ohmic drain to counteract dynamic  $R_{ds,on}$  [179].

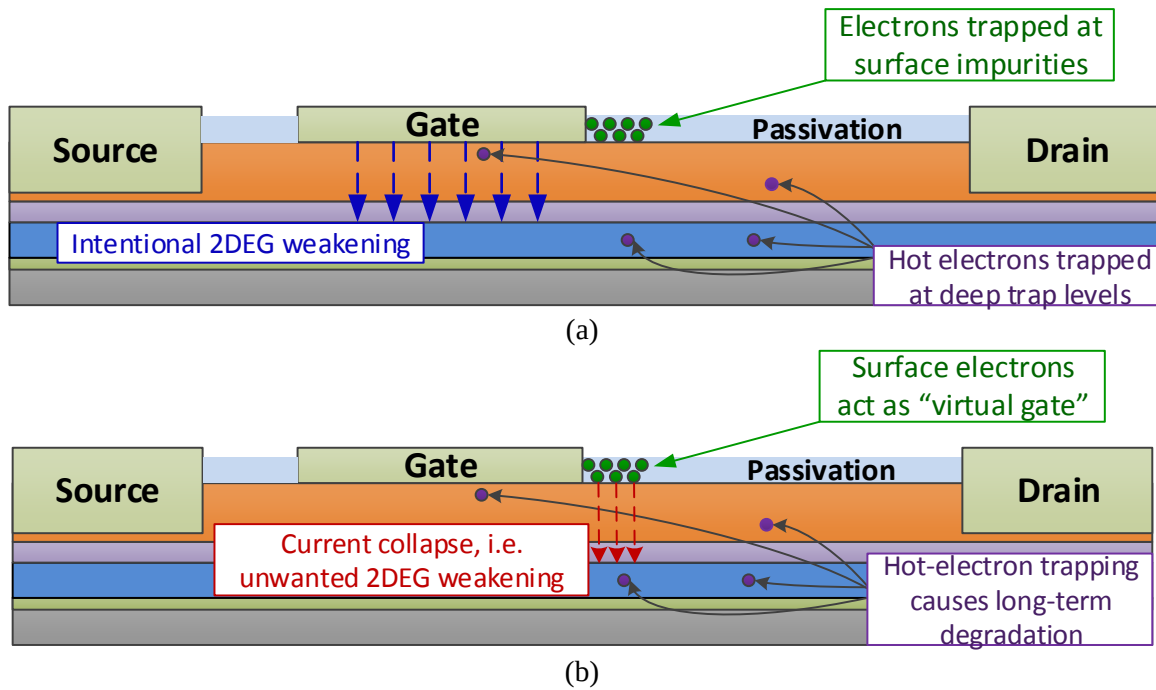


Figure 3.9. Mechanisms causing dynamic  $R_{ds,on}$  in lateral GaN HFETs: (a) Trapping of charges when blocking voltage in off-state, (b) Consequences of trapped charges during following on-state.

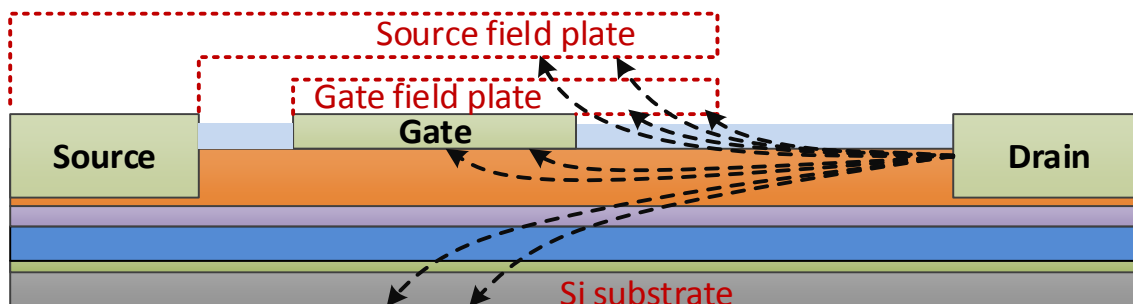


Figure 3.10. Field plates reshaping the gate-drain electric field to mitigate current collapse.

### 3.3.7 Breakdown mechanisms

Design of voltage-source converters often rely on the MOSFET's ability to survive a limited exposure to voltages over the device rating, according to the specified avalanche energy rating. However, lateral GaN HFETs do not have the potential for avalanche breakdown, because they do not rely on a p-n junction for voltage blocking. Vertical GaN MOSFETs may have avalanche capabilities, but lateral HFETs experience catastrophic dielectric breakdown when exposed to sufficient overvoltage [195]. This breakdown is destructive and non-recoverable. For this reason, GaN devices are typically rated much lower than the actual breakdown voltage. The dielectric may be designed to survive twice the rated voltage to prevent lateral breakdown along surface states. While source-connecting the substrate is beneficial for current collapse mitigation, this also provides a vertical path for leakage current to flow, which is a second breakdown mechanism for some devices. [196-202]

The gate in lateral HFETs is also susceptible to rupture. This failure mechanism may present as a gradual increase in steady-state current until the gate dielectric or Schottky junction completely breaks down [203]. Steady-state gate current is expected during normal operation for e-mode HFET with a p-doped layer beneath the gate. However, this has also been observed for insulated gate devices when exposed to excessive voltage and elevated temperatures, even when both of these conditions are within the ratings of the device [204]. For this reason, it is useful to periodically check the health of devices under test by measuring steady-state gate current, with a simple test setup using a dc power supply and current meter.

## 3.4 Reliability qualification

Power transistors such as MOSFETs and IGBTs are typically tested according to published JEDEC standards, and thereby qualified for particular reliability specifications. Testing for Si MOSFETS generally includes high-temperature reverse bias (HTRB), high temperature gate bias

(HTGB), high temperature storage (HTS), temperature cycling (TC), high temperature high humidity reverse bias (H3TRB), unbiased autoclave (AC), moisture sensitivity level (MSL), and electrostatic discharge (ESD) testing. Reliability data based on these tests have been published for EPC and Transphorm devices [205-207].

However, because these JEDEC standards were written for Si MOSFETs, different reliability qualification standards may be required for GaN HFETs. One of the main challenges for new devices is the accelerated lifetime testing. Conventional Si devices are tested for accelerated lifetime based on well-established models and years of experience. GaN devices may not respond the same way in the same test conditions, and there have not been as many years with practical field reliability experience to back up the accelerated lifetime models [208]. A path to developing new standards specifically designed for GaN devices has been proposed by [209-211]. The unique breakdown mechanisms discussed in the previous section must be addressed, and the qualification process will likely be different for lateral and vertical GaN power devices. JEDEC has recently formed a committee to set these new qualification standards [212].

### 3.5 *Operating temperature and thermal design*

GaN devices exhibit a positive temperature coefficient for  $R_{ds,on}$ , similar to that of Si. Figure 3.11 shows the trend of  $R_{ds,on}$  over temperature for several commercial GaN HFETs. These trends are derived variously from data sheets and published characterizations. The threshold voltage of most GaN devices is relatively stable over temperature. According to [213] and Chapter 6 of this dissertation, e-mode devices exhibit increasing switching loss with higher temperature due to the decreasing transconductance. This was shown experimentally in [52],[168],[204],[213]. Panasonic has the best reported performance at higher temperature of these devices listed.

Thermal design for some GaN devices can be challenging, depending on the package type. Surface-mount devices with bottom-side cooling typically connect to a heatsink through the board,



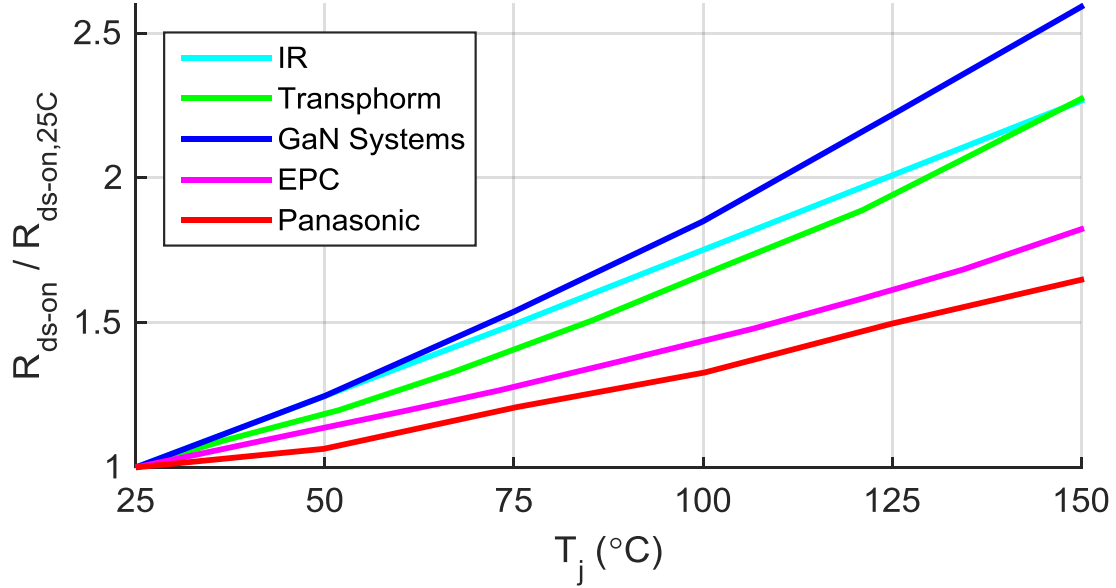


Figure 3.11. Normalized on-resistance of commercial GaN HFETs [38],[156],[165],[168],[204].

using thermal vias [107]. Top-cooled devices are also available from some vendors, and others use TO-220 packages that make thermal design easier. As compared with SiC, thermal design is especially critical for GaN-based converter design, because of the potential thermal runaway from both conduction loss and switching loss.

### 3.6 Switching behavior

GaN devices switch much faster than Si devices with similar voltage and current ratings. The input capacitance  $C_{iss}$  and gate charge  $Q_g$  are lower for GaN HFETs than Si MOSFETs. The output capacitance  $C_{oss}$  is also lower for GaN due to the smaller die size, as mentioned previously. The output capacitance of a Super Junction MOSFET could be the same as a similarly-rated GaN HFET at high voltage, but the Super Junction  $C_{oss}$  increases several orders of magnitude at low voltage. GaN switching speed can exceed 200 V/ns, and the turn-on and turn-off delay times can be under 10 ns at 400 V [204].

In hard-switched converters, the two significant sources of switching energy losses are the energy related to stored charge in the output capacitors ( $C_{oss}$  loss) and the loss from conduction of

the load current through a saturated device channel (overlap loss). In [214], it was shown that two selected e-mode devices experienced lower  $C_{oss}$ -related loss than a selected cascode with similar ratings, but higher overlap loss during turn-off. This study concluded that the cascode was better for soft switching and the two e-modes were more suitable for hard switching. However, such a comparison is very difficult to make in a universal sense, because of differences in die size and current ratings.

The switching behavior for a given device depends on the gate driver IC, converter topology, and board layout. Switching losses and speeds are difficult to approximate from device datasheets. The approximate capabilities of a given device can be determined experimentally with a double pulse test (DPT). Performing a DPT for WBG devices is a challenge in itself [54], but DPT results for many commercial GaN devices have been published [52],[57],[168],[204],[214],[215]. Although these characterizations are still not accurate when applied to a different converter, they may provide enough information for device selection and thermal design.

### 3.7 *Device packaging and PCB layout*

Fast switching transients magnify the impact of parasitic inductances in device packaging and printed circuit board (PCB) traces, because the voltage drop across any stray inductance is equal to

$$v_{stray} = L_{stray} \frac{di}{dt} . \quad (3.3)$$

Package parasitics such as  $L_d$ ,  $L_s$ , and  $L_g$  worsen the ringing that occurs during and after the switching transient, which limits the switching speed and may cause damage to the device. The common-source inductance  $L_{cs}$  couples the high  $di/dt$  from the power loop into the lower-voltage gate loop. The voltage drop across  $L_{cs}$  reduces the applied gate voltage during turn-on and increases it during turn-off, thereby slowing down both switching transients and worsening the switching

loss. It is crucial that common-source inductance be minimized, in the package as well as board layout. Some devices provide a Kelvin source connection, a separate connection to the source metallization that is only used by the gate loop, decoupling it more effectively from power loop transient effects [14],[18],[215],[216].

Overall parasitics can be reduced by combining the high-side and low-side devices in a single module, with decoupling capacitors and optimized internal connections [217]. Integrating the gate driver into the module provides additional benefits, as demonstrated in [218],[219]. TI's LMG5200 was the first commercially available GaN intelligent power module (IPM), built with EPC devices and rated at 80 V. TI also make a driver-integrated module with its own enable-switch 600 V GaN device and a gate driver combined in a surface-mount package [220],[221]

Lateral GaN devices offer the unique opportunity to monolithically integrate high-side and low-side devices on the same die and nearly eliminate package parasitics. This has been accomplished at 12 V by EPC and Panasonic, although isolation of the two devices on a shared die is more difficult to accomplish at higher voltage [222],[223]. Furthermore, a GaN-based gate driver can be monolithically integrated on the same die as the HFET for ultra-fast switching capabilities. Navitas has demonstrated success with monolithic integration of an e-mode GaN FET and gate driver, including a single device and a phase leg version [172],[174],[224].

### 3.8 *Commercial device availability*

As with any new technology, the relatively low availability of GaN power devices poses a barrier to widespread adoption [33]. Therefore, several of the leading GaN manufacturers have established industry partnerships and taken steps to increase availability of their devices. Transphorm has established agreements with both Fujitsu and ON Semiconductor, to mass produce and co-brand their cascode devices [225],[226]. Panasonic has a licensing agreement with Infineon to establish dual sourcing of the GIT [227]. GaN Systems has recently ramped up its production

ten times at their foundry, TSMC [228]. With these recent steps toward mass production, availability of GaN power devices may no longer be a barrier to industrial adoption.

### 3.9 *Gate driver considerations*

Beyond understanding the internal device structure, it is important that the power electronics engineer understand how it will impact converter design. Because of the faster switching and unique characteristics of HFETs, common design practices for Si-based converters may not take full advantage of GaN. In fact, simply replacing a Si MOSFET with a GaN HFET will likely cause the converter to stop functioning, and may even destroy the GaN device itself. This section will cover the critical differences between Si and GaN devices, and important considerations for GaN-based converter design.

#### 3.9.1 *Gate voltage and current*

Gate driver design for cascode devices is similar to driving conventional Si MOSFETs, because the input of a GaN cascode is a rugged Si MOSFET gate. However, e-mode GaN HFETs have more specific gate driver requirements. The threshold voltage of an e-mode HFET is typically 1-2 V, and the recommended driving voltage is typically around 5 V. This only allows a few volts of ringing before spurious switching events occur, during both turn-on and turn-off transients. Gate rupture is also a known issue with e-mode GaN devices. Even a small gate voltage overshoot may destroy the device.

Relatively few gate driver ICs on the market are designed specifically for the requirements of GaN devices. The LM5113 from TI is a dual driver designed for GaN that can drive both high-side and low-side devices, and can isolate the high-side driver up to 100 V. However, this driver is not suitable for higher-voltage applications. The LM5114 can drive any single GaN device, but it does not provide signal isolation [229].

Typically, gate driver ICs are chosen based on the specified current capability, but this number is not an accurate description of the IC's suitability for driving GaN, because of the relatively short switching time of the GaN device. Instead, the resistances and rise/fall times of the pull-up/source and pull-down/sink transistors can be used for the comparison. The rise and fall time should be lower than the turn-on and turn-off delay times of the GaN device, or as close to them as possible, to avoid limitations on the switching speed during the crucial overlap times [230]. The source and sink on-resistances effectively add series gate resistance for the turn-on and turn-off paths, so they should be considered when choosing external gate resistors.

The Panasonic GIT is somewhat unique in its steady-state gate current requirement. Although the device is voltage-driven, full enhancement of the channel requires a small steady-state gate current in the mA range. The diode characteristic of the gate limits the input voltage below 5 V, but a higher driving voltage is desirable during the turn-on transient to enable faster switching. This can be accomplished with an RC-type gate driving circuit, or a multi-stage driver as demonstrated in [231]. Panasonic has recently released a commercial driver IC for its device that includes this feature [232].

### 3.9.2 *Common mode transient immunity*

Silicon Labs also makes a series of isolated gate driver ICs that are optimized for GaN devices, compatible with driving voltages from 3 to 30 V and bus voltages in the kV range. These devices use digital isolators based on RF modulation as opposed to optical isolators, providing superior common-mode transient immunity (CMTI). Insufficient CMTI may allow spurious switching events when the  $dv/dt$  exceeds the CMTI specification [233]. While several isolated drivers have specified typical CMTI of 50-100 kV/ $\mu$ s, this characteristic varies due to process variation and temperature. The actual CMTI could be as low as the specified minimum, which may be much lower than the typical value. Available isolation methods have been reviewed for several

GaN-based converters [234],[235], and it is generally concluded that these RF-based digital isolators tolerate higher  $dv/dt$  than alternatives such as optocouplers or capacitive isolators. The newer Si827x family has a specified minimum CMTI of 200 kV/ $\mu$ s, much higher than any other available isolated gate driver [236]. Of course, even with a sufficient CMTI-rated gate driver IC, the PCB layout must be designed very carefully to prevent common-mode interference through stray impedances. To further improve CMTI, other techniques may be implemented in the gate drive circuit, such as a common-mode choke or differential connection of the digital signal inputs [237],[238].

### 3.9.3 Cross-talk

Another source of spurious switching events is interference between high-side and low-side devices due to the Miller effect. This may cause cross-talk, also known as cross-conduction or Miller turn-on, a phenomenon in which one device is inadvertently turned on when the complementary device in the same phase leg is intentionally turned on, due to the  $dv/dt$  on its Miller capacitance. This cross-talk allows a shoot-through current to flow from the dc bus across the saturated channels of both devices, incurring additional switching losses. In a phase leg configuration, cross-talk losses may be especially noticeable during light load operation, when the overlap losses are nearly zero and the turn-on switching speed is highest [60].

Figure 3.12 shows the cross-talk mechanism for this device, including the parasitic impedances of the device, PCB, and gate driver IC. As current flows through the Miller capacitance  $C_{gd}$  to displace its charge, the same current will be split between the gate capacitance ( $i_{gs}$ ) and the gate loop ( $i_{gss}$ ). If  $i_{gs}$  deposits sufficient gate charge to raise  $v_{gs,int}$  above its threshold during active device turn-on, the synchronous device will also turn on and cause shoot-through losses. Similarly, during active device turn-off, the synchronous device displacement current induces a negative voltage on  $v_{gs,int}$ , which increases conduction losses during dead time when the device is operated

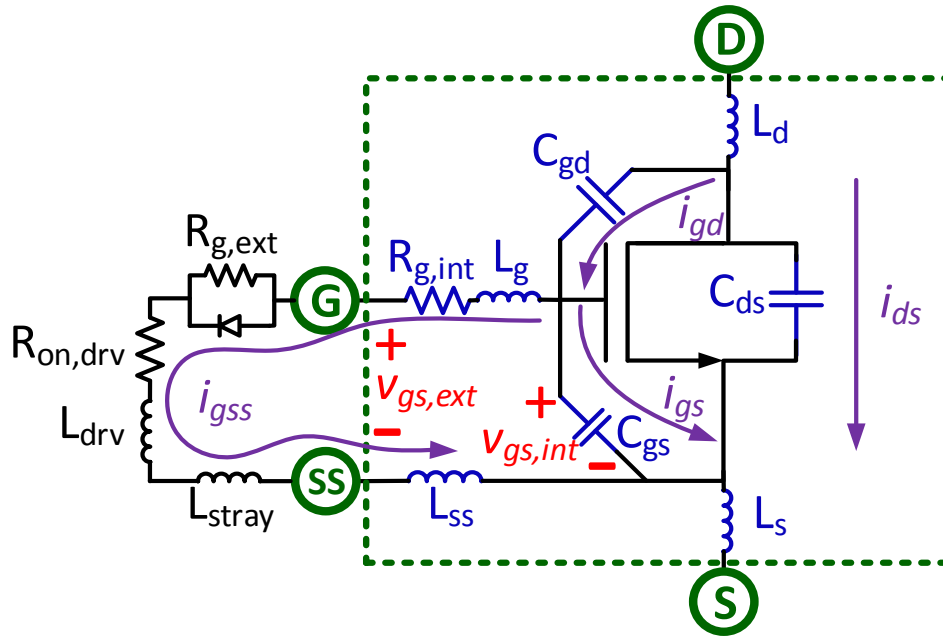


Figure 3.12. Mechanism causing cross-talk in the synchronous device of a phase leg.

in DLB mode.

Kelvin-source connections are often used in WBG devices to reduce common-source inductance. This is overall beneficial to gate voltage oscillation, but the Kelvin terminal also creates a much higher gate loop inductance than in the power loop. This gate loop inductance resonates with the capacitances  $C_{gs}$  and  $C_{gd}$  during switching, causing oscillation as well as a mismatch between the true internal gate voltage and the measured external gate voltage. It is difficult to characterize the cross-talk mechanism for WBG devices by directly viewing the external gate-source voltage because of this mismatch.

Cross-talk can be prevented by slowing down the turn-on transient (e.g. with a higher turn-on gate resistance) but this will also increase the overlap losses. The tradeoff between overlap and cross-talk loss will be different for every converter, based on the device, driver, switching speed, and operating conditions. However, there are several techniques to minimize cross-conduction effects. One common method to prevent cross-talk for SiC devices is to use a negative voltage

supply for the off-state. However, this is non-ideal for enhancement-mode GaN devices, because it increases the reverse conduction losses during dead time. Another method to mitigate cross-talk is adding an external capacitor in parallel with the internal device  $C_{gs}$ , slowing the switching transients to limit  $dv_{ds}/dt$  while also providing a low-impedance path for the  $C_{gd}$  displacement current. However, this is also not desirable due to increased overlap and driving losses.

The simplest cross-talk mitigation method for GaN may be to use 0  $\Omega$  gate resistance for the turn-off path and a higher resistance for the turn-on path, however this will also increase overlap losses somewhat. Some drivers provide separate paths for gate current during turn-on and turn-off. If the driver does not provide separate paths, a Schottky diode can be added in parallel with the gate resistor [11],[239]. The most effective solution for cross-talk mitigation may be an active gate driver as demonstrated in [60] for SiC.

### 3.10 Summary

The basic structures and characteristics of GaN power devices have been reviewed, including both vertical and lateral devices. The commercial status and specifications of normally-off GaN power devices were summarized. Currently, three manufacturers produce enhancement-mode GaN HFETs for open online ordering, as well as one cascode. Several lateral device manufacturers are providing samples of their e-mode and cascode devices, and vertical device samples may also be available soon. As the availability and performance of commercial GaN devices continues to improve, GaN-based converter design skills will need to keep pace with these device developments. Here, GaN-based converter design considerations were reviewed, including switching characterization, packaging, board layout, gate driver design, reverse conduction mechanisms, dynamic  $R_{ds,on}$ , and thermal design. The breakdown mechanisms and reliability concerns were also discussed, as well as the qualification process to characterize the reliability of



commercial GaN devices. This review provided an introduction to GaN-based power devices, in order to help readers effectively use GaN to design high-frequency and high-efficiency converters.

Because this review discussed vertical GaN as well as cascode and e-mode lateral GaN, it presents the opportunity to compare these technologies in terms of performance and commercial readiness. In terms of maturity, cascode devices have been produced commercially for longer than most other GaN devices at the 600 V level, and have been shown to be capable of very high-speed and low-loss switching. However, the fewer internal components and interconnections of enhancement-mode HFETs may enable higher reliability as the technology continues to mature. Recently available vertical GaN devices are the youngest of these, and very little is known of their performance relative to their laterally-structured cousins, but the material properties of GaN indicate that they should be able to achieve superior performance to SiC MOSFETs when the challenges of wafer and vertical device fabrication are overcome. At the moment, there is no clear winner between these three categories of GaN power devices, and each product may find its own niche at a particular range of voltage, current, and switching frequency.

## Chapter 4

### **Methodology for Static and Dynamic Characterization of an Enhancement-Mode GaN FET**

#### *4.1 Introduction*

As mentioned in the previous chapter, normally-off power GaN devices are currently produced as one of two fundamental types: cascode and enhancement-mode. Cascode GaN devices are a convenient way to produce a normally-off device, but they have reliability and switching performance limitations. Alternatively, an enhancement-mode GaN device can be directly fabricated with several different gate structures. The HFET is a fundamentally different device from Si or SiC MOSFETs, and e-mode modification techniques make each HFET unique from each other as well [141]. Before selecting the best GaN FET for a given application, it is necessary to know the characteristics of the devices available. This includes static characteristics such as on-resistance, maximum current, gate leakage, drain-source leakage, and junction capacitances. Additionally, dynamic characteristics such as switching energy, transient times, slew rates, and overshoot voltages are important parameters. These must be characterized across a range of operating conditions in order to effectively design a converter, especially if the device is relatively new and a full datasheet has not yet been published.

The detailed methodology for characterizing the static and switching performance of power devices, particularly Si and SiC, have been presented by previous works [44],[47],[54],[240]. However, some of these procedures and test setups must be revised for GaN devices, and the analysis of the results is different due to the fundamentally different device structure. This chapter will describe the techniques used to characterize enhancement-mode GaN FETs, as well as the challenges associated with these methods. For demonstration purposes, two devices will be

considered as example devices under test (DUTs), both rated at 600 V and 30 A: GS66508P from GaN Systems and a gate injection transistor (GIT) from Infineon.

## 4.2 *Static characterization*

The static characteristics of a GaN device describe its behavior in steady-state, such as its on-resistance, maximum current capability, and breakdown voltage. Some of the static characteristics are also helpful in interpreting later dynamic test results.

### 4.2.1 *Pulsed I-V testing*

The primary equipment used for static characterization is a power device curve tracer. In order to test static behavior over a range of operating conditions without overheating the device, a curve tracer provides a pulse of output voltage to the device, while also controlling the gate voltage. One example of a curve tracer, model 371b from Tektronix, provides a fixed pulse period and duty cycle, and also takes its measurement at a fixed point during the pulse [241]. The newer Keysight B1505a curve tracer allows more control over these pulse parameters. In fact, the exact duration and timing of the voltage pulses applied to the input and output can both be controlled [242]. The goal of this pulsing is to allow both the gate and drain voltages to reach steady-state, then take a measurement after any transient behavior is over. GaN devices have a much smaller die size than a comparable Si device, so the pulses must be relatively short and spaced further apart to prevent self-heating during and between pulses.

The effect of this pulse timing can be seen most clearly in the device's saturation region, where the power loss during a long pulse results in considerable self-heating, and the measurement may show erratic or false trends during repeated testing. Figure 4.1 and Figure 4.2 shows an example of this phenomenon with Infineon's GIT, tested with the Keysight B1505a curve tracer. Figure 4.1 shows the oscilloscope view of one pulse in the saturation region, and Figure 4.2 shows the output characteristic with different measurement delay times across the sweep of output voltage.

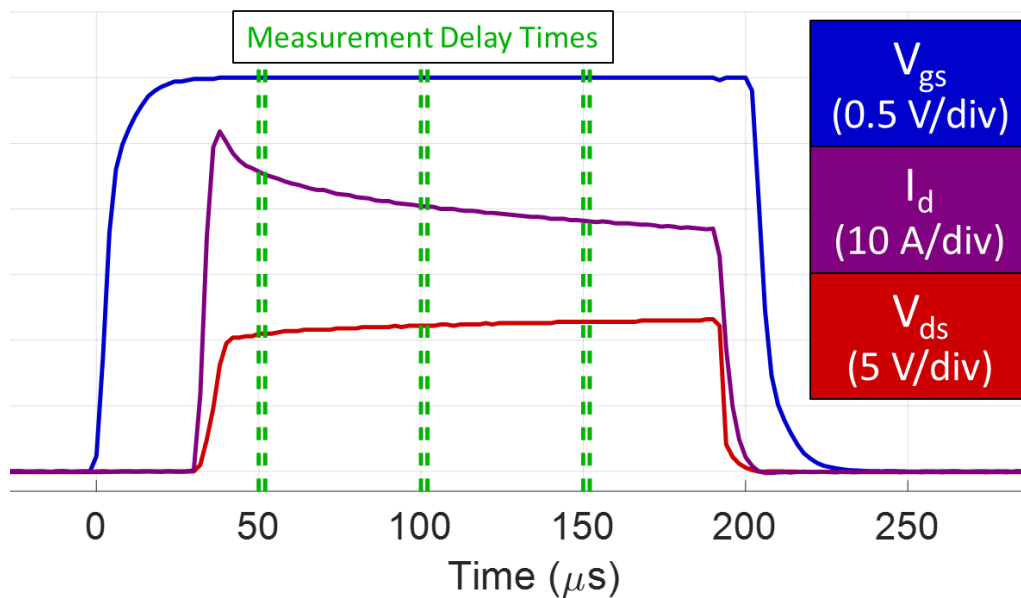


Figure 4.1. Oscilloscope view of I-V pulses from a Keysight B1505a curve tracer, testing an Infineon GIT in the saturation region.

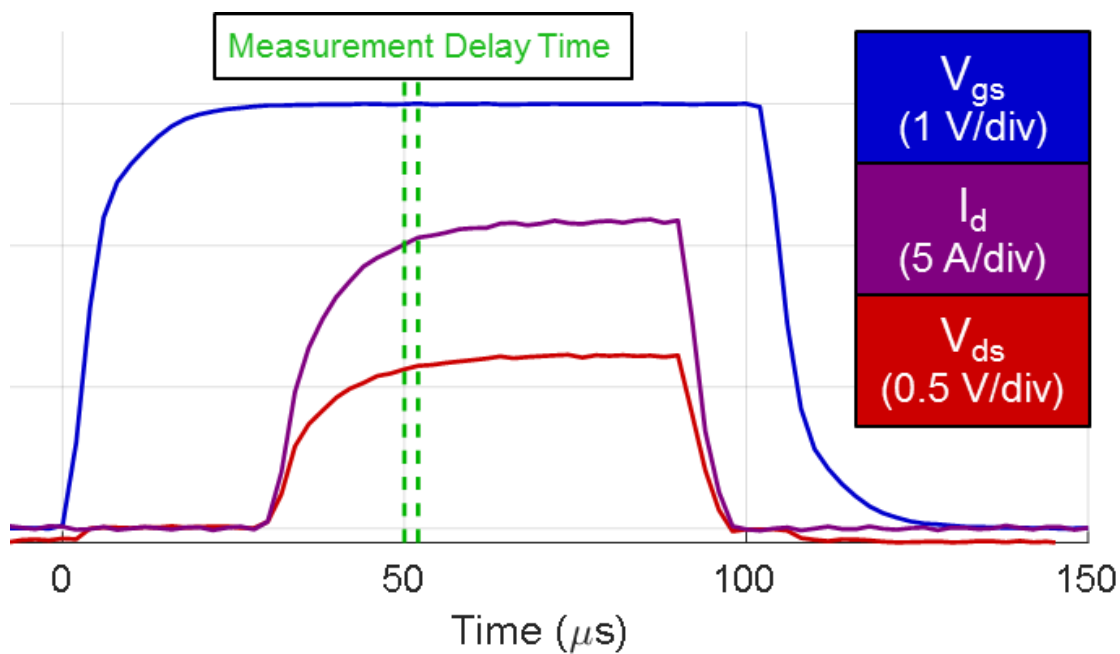


Figure 4.2. Oscilloscope view of I-V pulses from a Keysight B1505a curve tracer, testing an Infineon GIT in the ohmic region.

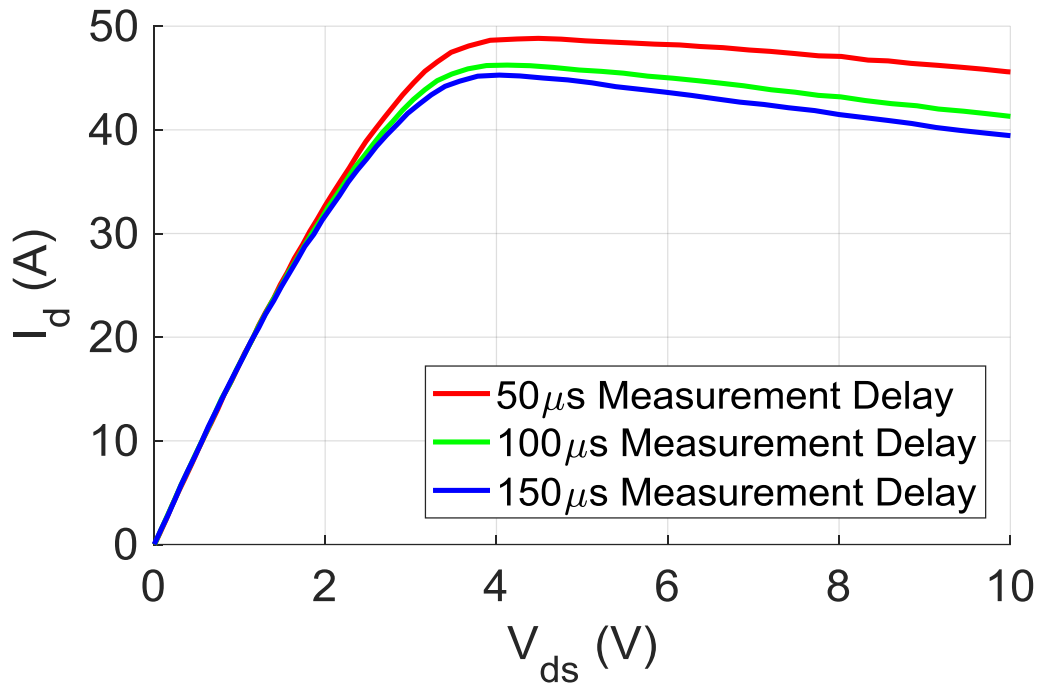


Figure 4.3. Resulting output characteristic curves from a Keysight B1505a curve tracer, testing an Infineon GIT in the ohmic and saturation regions with various measurement delay times.

Due to the self-heating during each pulse, taking the static measurement later in the pulse results in a higher junction temperature at higher voltage, and therefore a more negative slope of output current with respect to voltage. Decreasing the period between pulses may also result in a similarly negative trend due to accumulated self-heating across the sweep. Therefore, the pulse timing and measurement delay should be chosen appropriately for each device, based on a careful analysis of the curve tracer pulse waveforms.

The accuracy of a curve tracer is improved with four-wire Kelvin measurement. One pair of wires is used to force a voltage across the drain and source terminals, while measuring the current produced through the device, and a second pair of wires senses the voltage across the terminals. If the sense wires are connected very close to the device terminals, stray resistances from the test fixture and wires do not affect the measurement accuracy. However, a voltage drop will still occur between the curve tracer's force terminals and the device, so the applied drain voltage will not be

exactly equal to the measured drain voltage. While this series resistance does not affect the accuracy of the measurements, it may require a higher force voltage to reach the same measured voltage for a higher output current.

#### 4.2.2 *Output characteristic*

Once the pulse parameters are established, the remaining question is what boundaries to choose for the sweeps of gate voltage, drain voltage, and drain current. GaN FETs require special treatment in this area for two reasons. The first is gate voltage. The threshold for GaN FETs is typically 1-2 V, much lower than comparable Si devices. Additionally, some devices such as the GIT have a diode-like characteristic on the gate, limiting the pulsed gate voltage to the knee voltage of that gate diode. Other GaN devices with insulated gates may be easy to rupture with repeated pulses above the steady-state gate voltage rating. It is therefore safest to only test the devices up to this steady-state rating, even though the curve tracer testing is pulse-based. This reduces the risk that the device is degrading or breaking down as testing progresses. A series resistor is often placed between the curve tracer and gate to reduce oscillations, so the applied gate voltage may need to be adjusted by the voltage drop across this resistor to achieve the desired gate voltage.

The test conditions and sweep boundaries must be chosen based on the expected behavior of the device under test (DUT). For a GaN FET, this should include both positive and negative gate voltages, a range of temperatures, and output I-V points that include both ohmic and saturation regions. Figure 4.4 shows an example output characteristic in both forward and reverse directions for an Infineon GaN GIT, captured using a Keysight B1505a curve tracer. Figure 4.5 shows a similar characteristic for a GaN Systems GS66508P, captured using a Tektronix 371b curve tracer.

One of the key characteristics for a power device is  $R_{ds,on}$  as a function of gate voltage, output current, and junction temperature. This can be calculated from the output characteristic, and is usually given at one particular output current, although it may vary as a function of current as

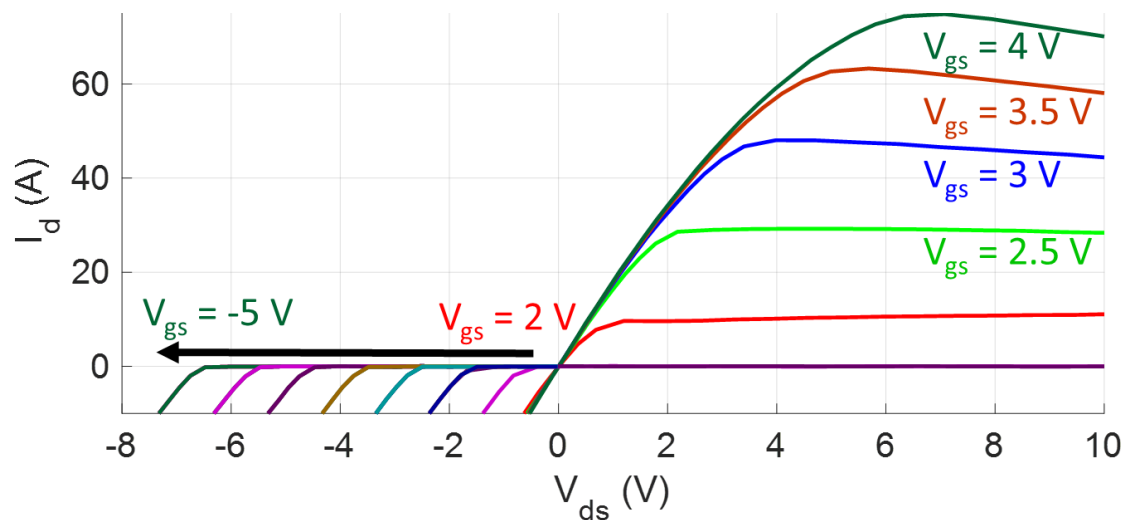


Figure 4.4. Output characteristic of Infineon GIT at  $T_j = 25\text{ }^{\circ}\text{C}$ .

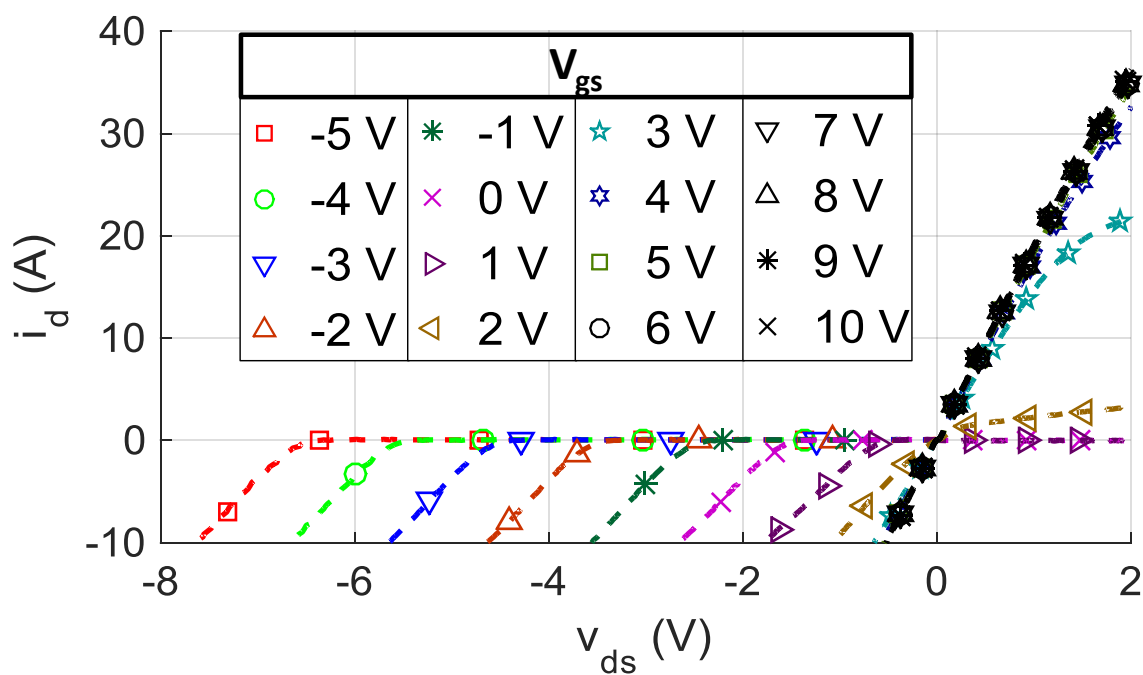


Figure 4.5. Output characteristic of GaN Systems GS66508P at  $T_j = 25\text{ }^{\circ}\text{C}$ .

well. Figure 4.6 shows the calculated  $R_{ds-on}$  for GaN Systems GS66508P with a load current of  $\pm 10$  A. As expected, the forward-conduction and reverse-conduction on-resistances are equivalent, and they both dropped with higher gate voltage. However, the reduction in on-resistance is not very significant above 5 V. Similarly, Figure 4.7 shows the on-resistance of the Infineon GIT measured with 10 A load current, over increasing gate voltage, and it does not drop significantly above 3 V.

Output characteristics are typically measured with junction temperatures up to 150 °C, using a hot plate or oven to heat the device case. The benefits and drawbacks of these techniques will be discussed later in this chapter. As the junction temperature increases, on-resistance increases, often by a factor of 2 or more. Figure 4.8 shows the relative increase in on-resistance over temperature for the two devices tested, normalized to 25 °C.

The on-resistance also has a relationship with drain current, because higher current brings the drain-source voltage closer to the point of saturation. The results in Figure 4.6 are based on the

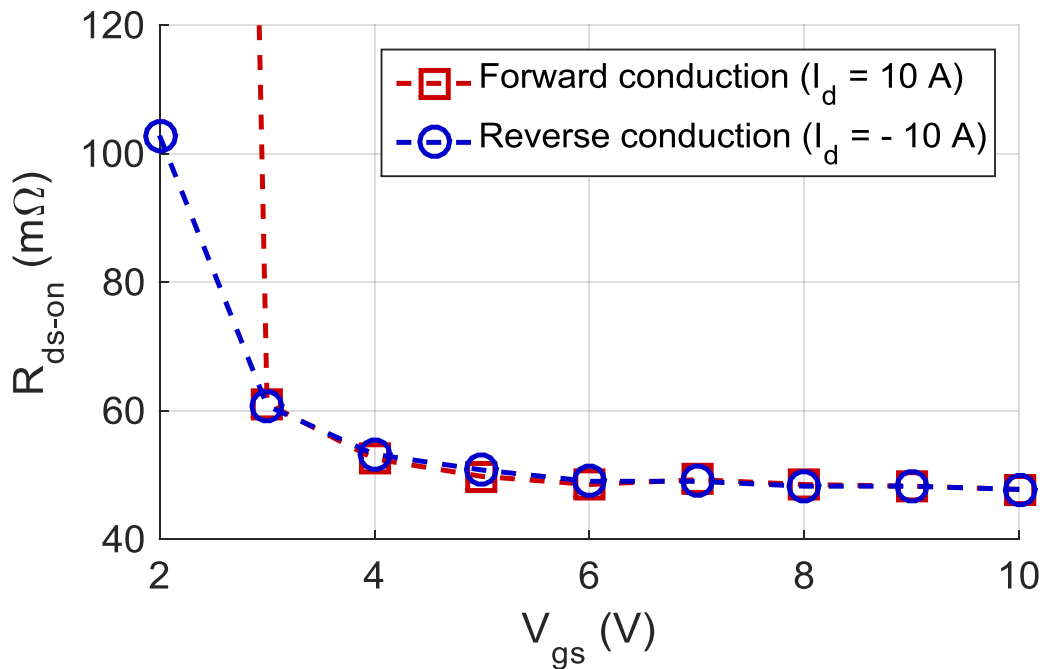


Figure 4.6. On-resistance of GaN Systems GS66508P at  $T_j = 25$  °C, over increasing gate voltage.



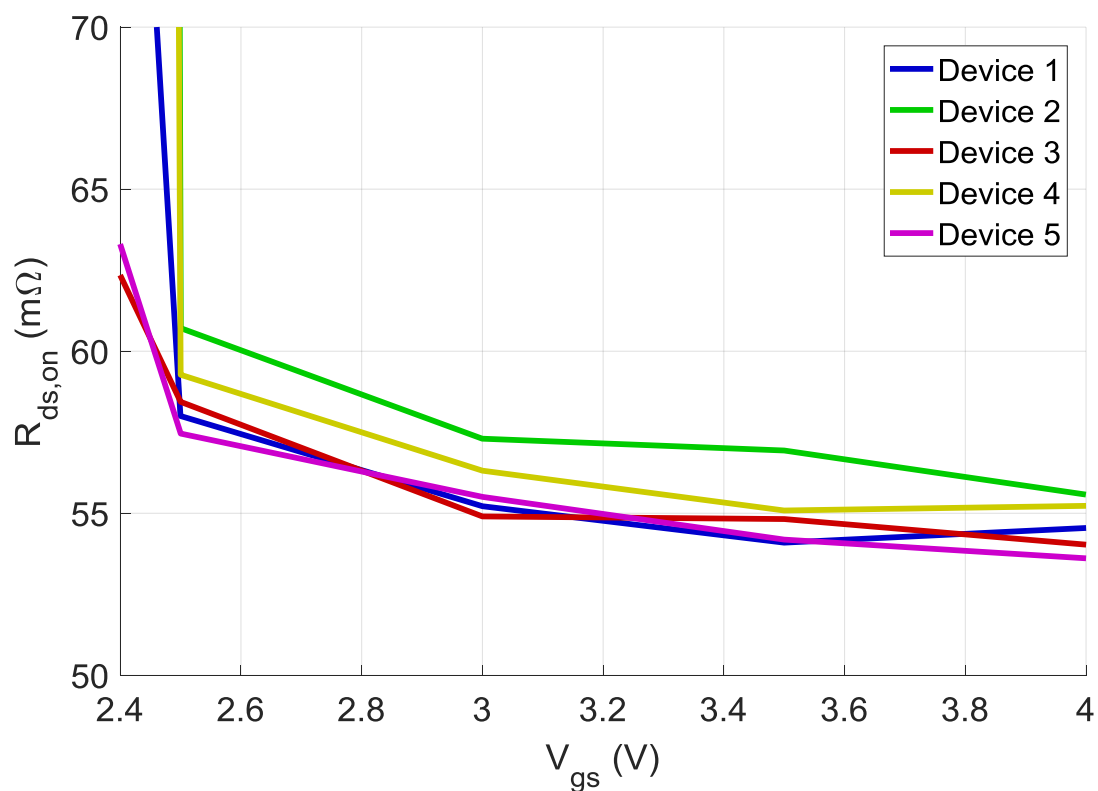


Figure 4.7. On-resistance of Infineon GIT at  $T_j = 25\text{ }^{\circ}\text{C}$ , over increasing gate voltage.

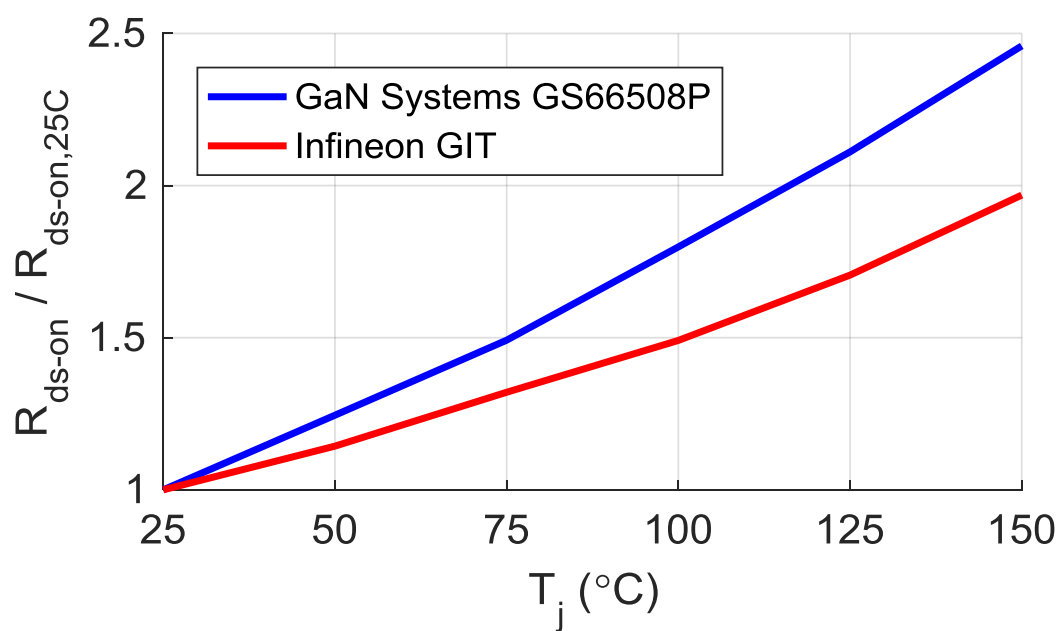


Figure 4.8. On-resistance for a sample device of GaN Systems GS66508P and Infineon GIT, over increasing junction temperature.

output characteristics at 10 A, because there is no noticeable change from 0 A to 10 A. However, at the full rated current of 30 A, there is an increase of up to 10% in the ohmic region. Figure 4.9 and Figure 4.10 show this relationship at 25 °C and 125 °C, respectively. In the higher temperature case, the channel enters the saturation region at a lower drain current than it does at room temperature, so there appears to be a stronger relationship with drain current. However, with a gate voltage of 6 V or higher, an increase of only 5-10% occurs over the entire current rating.

A unique property of GaN FETs is the reverse conduction mechanism, often described as “self-commutated reverse conduction” (SCRC) or “diode-like behavior” (DLB). Unlike a Si device with a true body diode, the GaN channel actually becomes enhanced when a reverse voltage is applied between drain and source. The threshold of this turn-on, and the subsequent forward voltage drop in DLB, is proportional to the applied gate-source voltage. The slope of the I-V curve in DLB mode,  $R_{sd,rev}$ , is typically higher than the on-resistance  $R_{ds,on}$ , but it is similarly dependent on junction temperature. The shape of a DLB reverse output curve can be approximately described by (2.5).

When  $V_{gs} < V_{gs,th}$ , reverse conduction forces the device into saturation, but only just past the knee between ohmic and saturation regions. A more negative  $V_{gs}$  drives the device even further into saturation, and  $R_{sd,on}$  becomes more dominated by the reverse transconductance rather than the typical ohmic on-resistance. Figure 4.11 shows  $R_{sd,rev}$  at 10 A, over a range of  $V_{gs}$  and  $T_j$ . In addition to higher resistance, a more negative  $V_{gs}$  also increases the DLB forward voltage drop, so this is generally an undesirable mode of operation.

### 4.2.3 Transfer characteristic

Whereas an output characteristic includes both ohmic and saturation region behavior, a transfer characteristic focuses on the relationship between gate voltage and output current in the

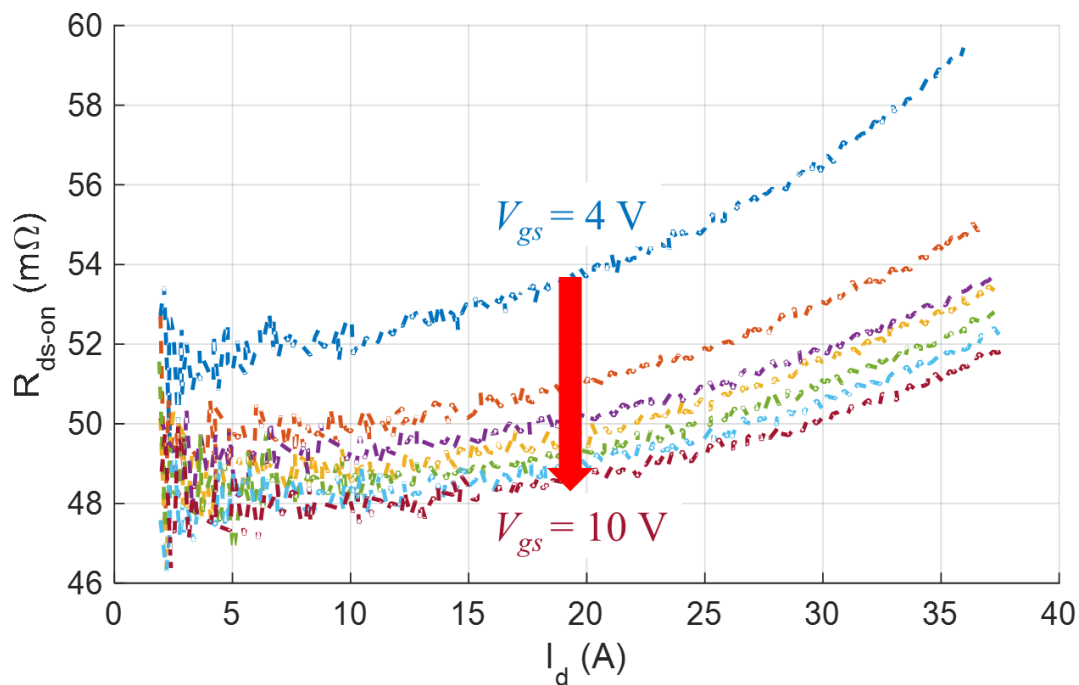


Figure 4.9. On-resistance vs. drain current for GaN Systems GS66508P at  $T_j = 25^\circ\text{C}$ .

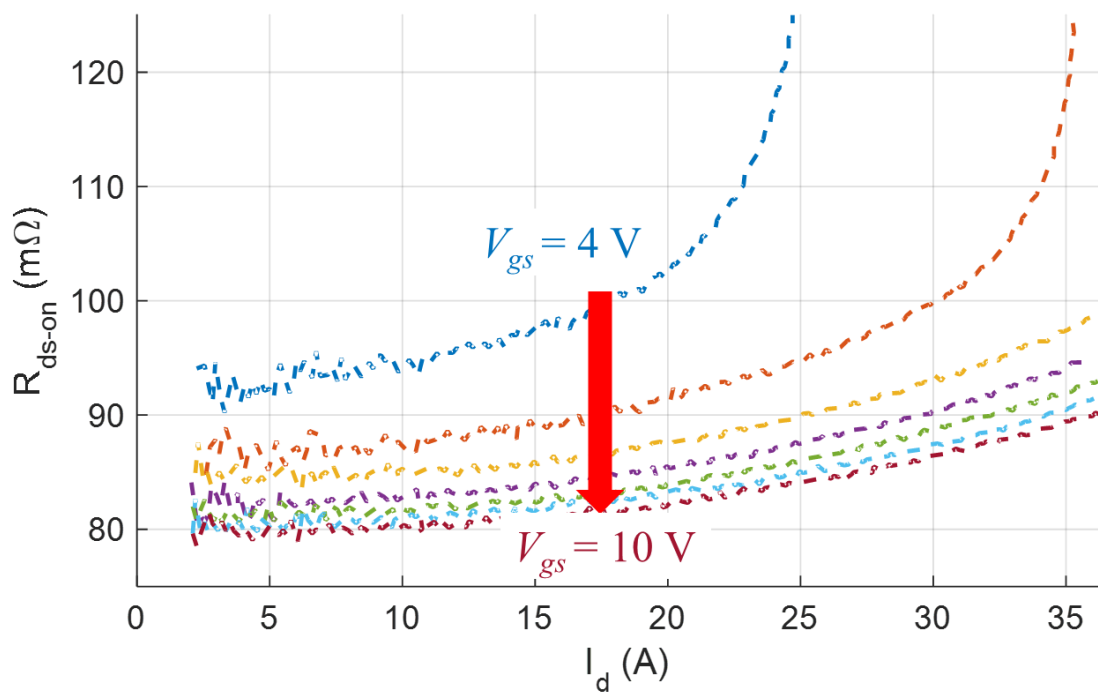


Figure 4.10. On-resistance vs. drain current for GaN Systems GS66508P at  $T_j = 125^\circ\text{C}$ .

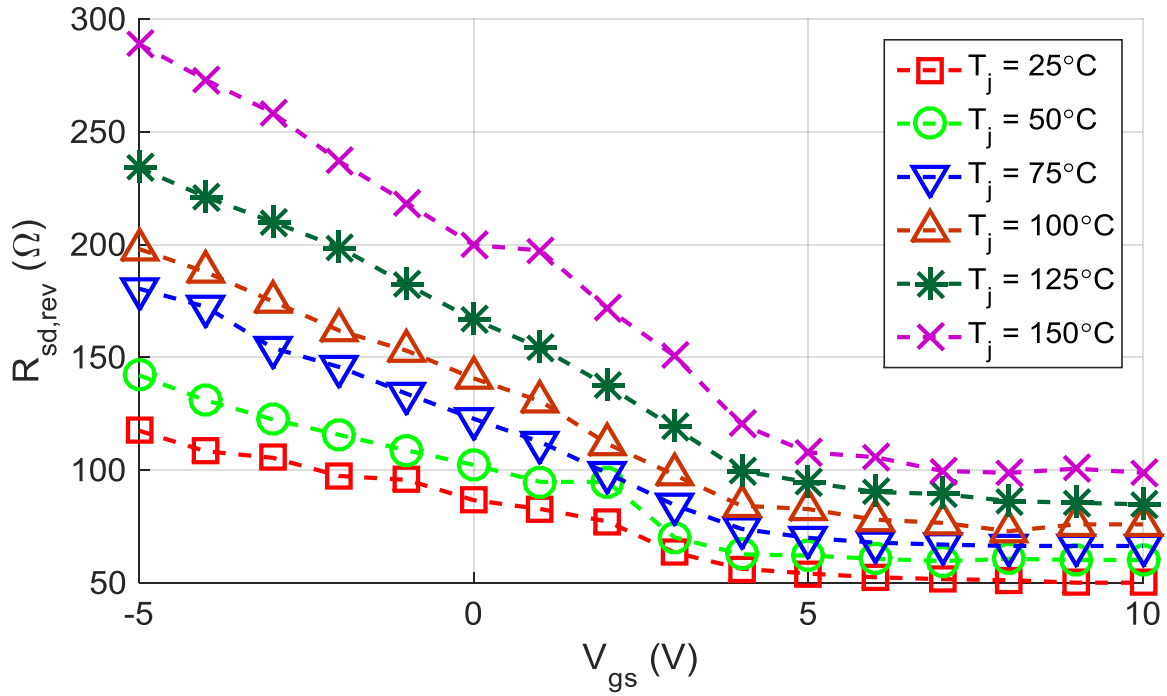


Figure 4.11. Reverse conduction on-resistance  $R_{sd,rev}$  of GaN Systems GS66508P at 10 A.

saturation region. The slope of this curve is the forward transconductance,  $g_{fs}$ . For a given transfer characteristic, the drain voltage must be held constant at a point that will keep the device in the saturation region, based on

$$V_{ds} > V_{gs,max} + V_{th} . \quad (4.1)$$

Figure 4.12 shows an example transfer characteristic of a GS66508P, and Figure 4.13 shows an example transfer characteristic for an Infineon GIT. Plotting several transfer curves at different temperatures helps in identifying the maximum achievable drain current for given operating conditions, and determining the gate voltage at which a fixed drain current occurs can be considered the device's threshold voltage.

#### 4.2.4 Gate leakage current

The gate current test is not as common for conventional Si devices as the others presented here, but it is very important for GaN FETs. Enhancement-mode lateral GaN FETs can be divided

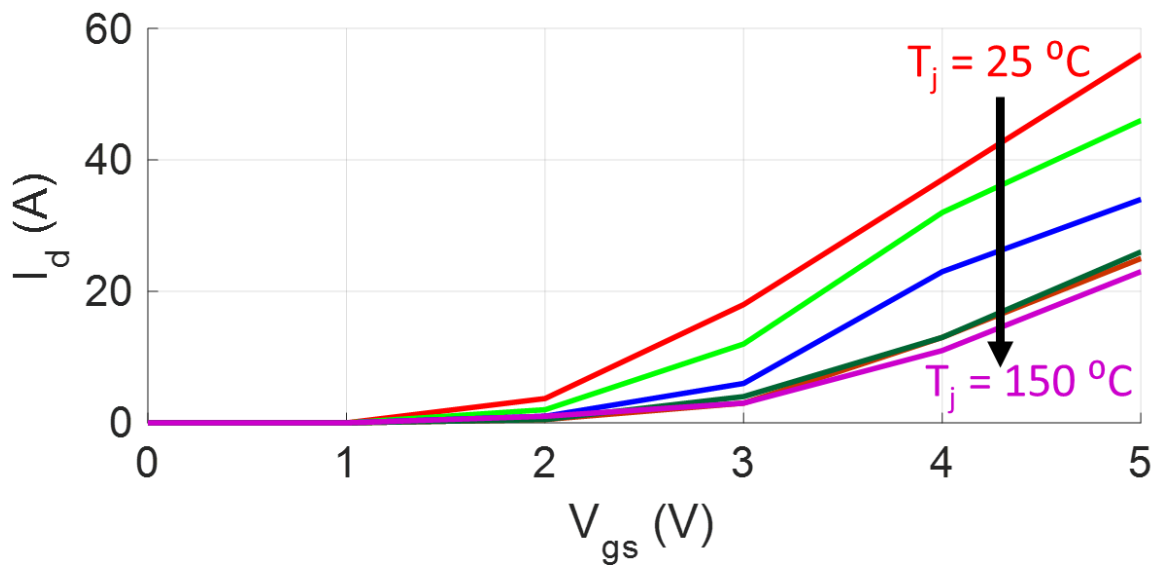


Figure 4.12. Transfer characteristic for GaN Systems GS66508P, collected using Tektronix 371b, with  $V_{ds} = 7\text{ V}$ .

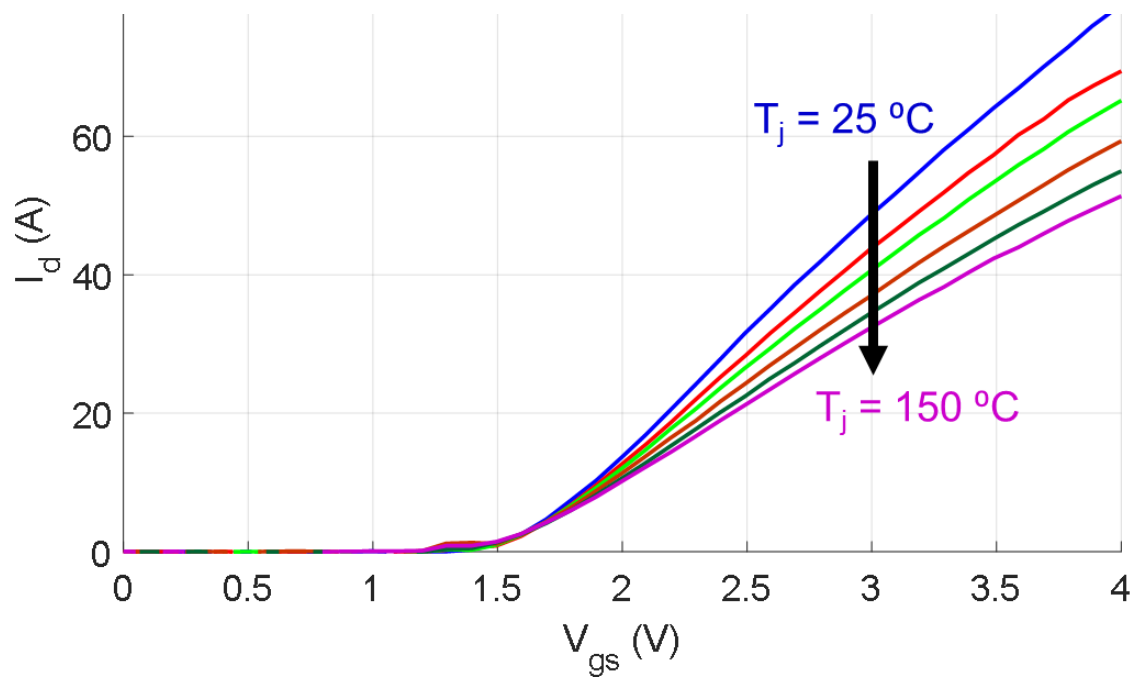


Figure 4.13. Transfer characteristic for Infineon GIT, collected using Keysight B1505a, with  $V_{ds} = 8\text{ V}$ .

into two groups: those with insulated gates, and those with non-insulated diode-like gates. For insulated gates, such as the GaN Systems GS66508P, the leakage current may be non-negligible and highly dependent on both gate voltage and junction temperature. Because the current flows through the gate insulator, this may lead to device breakdown, and characterization is helpful in determining a safe and reliable gate driving scheme [204],[243]. For diode-like gates, such as the Infineon or Panasonic GIT, this gate current is not actually leakage. However, the driving voltage must be carefully selected to ensure that the proper current flows through the gate to keep its diode forward-biased without exceeding the rating of the device.

In either case, the gate current characteristic is critical for effective driver design. Gate current can be measured automatically by some curve tracers, but it can also be measured manually during output characteristic sweeps, by measuring the voltage on a shunt resistor that is inserted in series with the gate driving loop. Figure 4.14 and Figure 4.15 show example gate current characteristics for two GaN devices, one with an insulated gate and one with a diode-like gate. It is also noteworthy that for the GIT, this current is strongly dependent on the applied  $V_{ds}$  during the test, in addition to gate voltage and junction temperature.

#### 4.2.5 *Drain-source leakage current*

Lateral GaN devices do not inherently have any avalanche breakdown capability, so breakdown voltage testing can result in catastrophic dielectric breakdown and destruction of the device. However, the expected breakdown voltage can be characterized by carefully measuring the drain-source leakage current above the voltage rating. This leakage is also related to the applied gate voltage, although this correlation can be positive or negative. Figure 4.16 and Figure 4.17 show the leakage current curves for GaN Systems GS66508P and the Infineon GIT, respectively. As shown, the GIT's leakage current increases with a more negative gate voltage, and the GS66508P's leakage current decreases somewhat with more negative gate voltage.

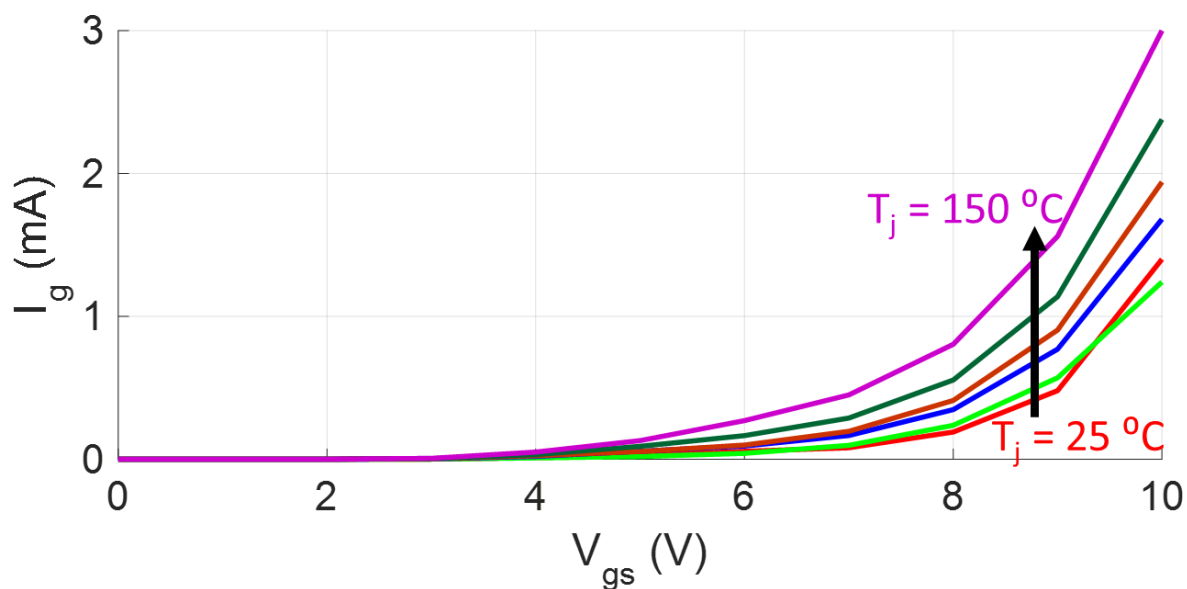


Figure 4.14. Gate current characteristic for GaN Systems GS66508P, collected using a shunt resistor in series with the gate.

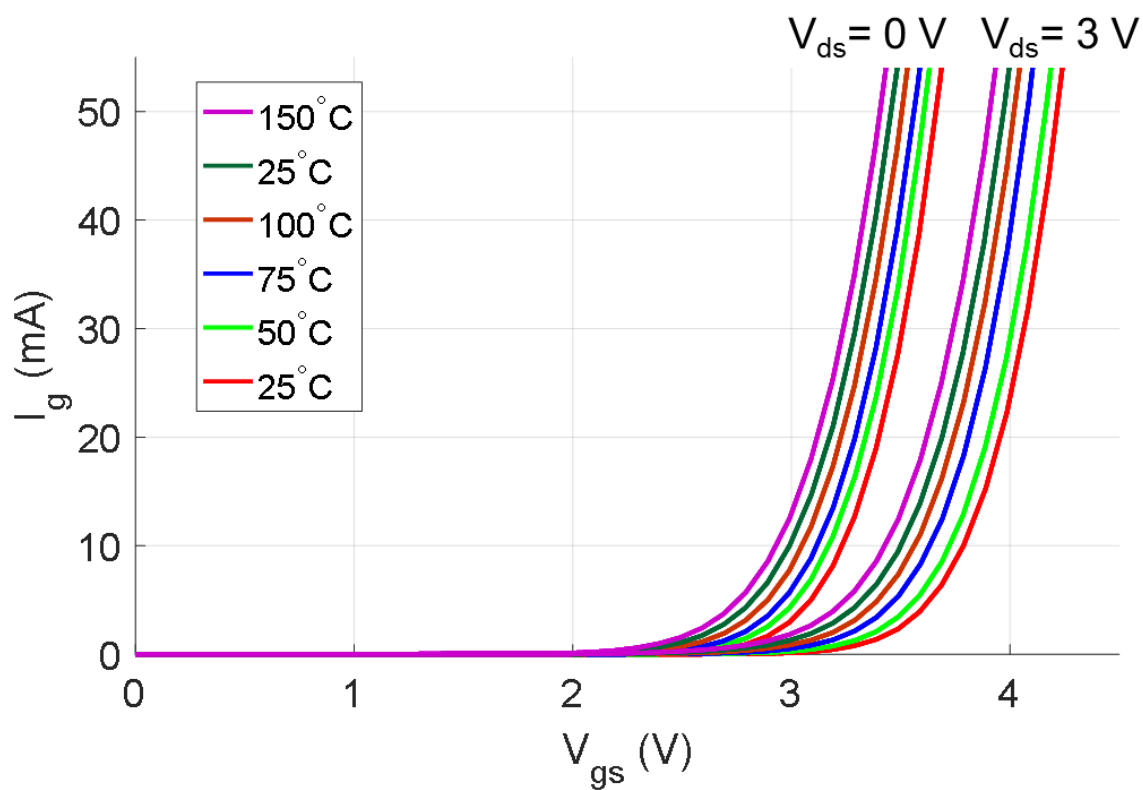


Figure 4.15. Gate current characteristic for Infineon GIT, collected using Keysight B1505.

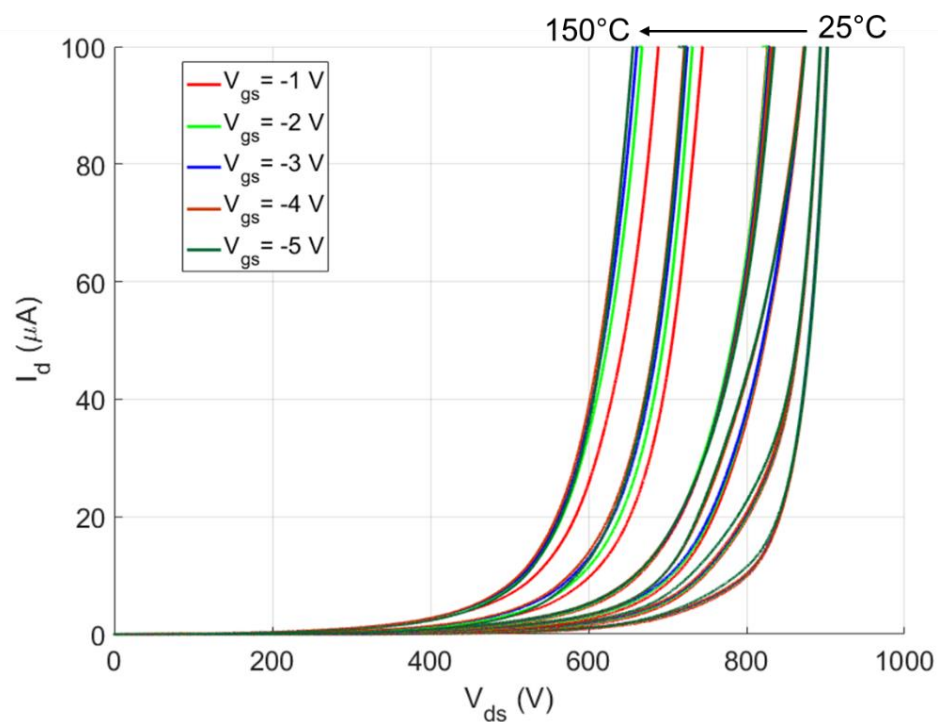


Figure 4.16. Drain-source leakage current characteristic for Infineon GIT, collected using Keysight B1505a[244],[245].

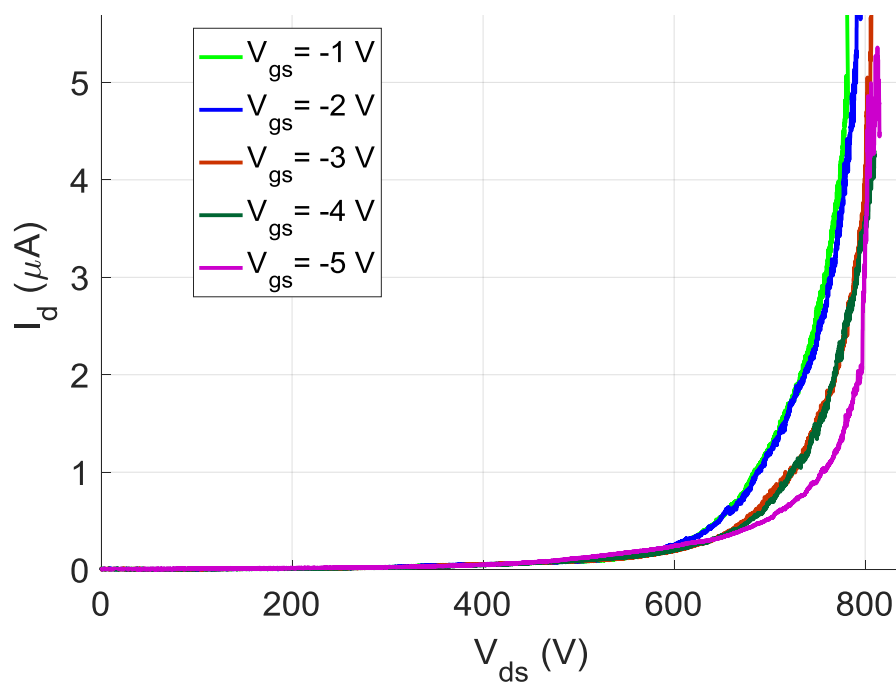


Figure 4.17. Drain-source leakage current characteristic for GaN Systems GS66508P at 25 °C, collected using Keysight B1505a.



#### 4.2.6 Junction capacitance measurement

The capacitance across the output terminals of the device is a nonlinear function of the voltage across those terminals, as the depletion region width changes. Rather than reporting the terminal capacitances  $C_{ds}$ ,  $C_{gd}$ , and  $C_{gs}$ , it is conventional to report the output capacitance  $C_{oss}$ , the input capacitance  $C_{iss}$ , and reverse transfer capacitance  $C_{rss}$ , defined as

$$C_{oss} = C_{ds} + C_{gd} \quad (4.2)$$

$$C_{iss} = C_{gs} + C_{gd} \quad (4.3)$$

$$C_{rss} = C_{gd} . \quad (4.4)$$

These capacitances can be characterized with a precision impedance analyzer, and this is also a feature of some curve tracers. However, the measurement equipment must be precisely calibrated for the impedance of the test fixture. This includes all cables and test leads, as well as the PCB in cases of a surface-mount device. The exact position of the test leads affects the fixture impedance, not only the impedance of the leads themselves. A custom fixture adapter must therefore be designed for devices, with rigidly oriented connections such as in the example shown in Figure 4.18 for a surface-mount GaN GIT. This adapter cannot be connected to the measurement equipment with flexible cables, but instead is mounted with rigid banana connectors so that the equipment can be calibrated with an open-circuit and short-circuit variant of the board.

Figure 4.18 shows an example capacitance characteristic of an Infineon GIT. The output capacitance characteristic is particularly useful for analysis of switching transients and loss, as explained later in this chapter. It is worth noting that the input capacitance does not typically change much as a function of drain voltage, but the  $C_{gs}$  component is a stronger function of gate voltage. As a result, it is useful to characterize this behavior as well. Figure 4.20 shows an example  $C_{gs}$ - $V_{gs}$  characteristic for the same Infineon GIT, obtained using the Keysight B1505a. It is clear from the figure that the  $C_{iss}$ - $V_{ds}$  curve is not a complete picture of the actual input capacitance, since

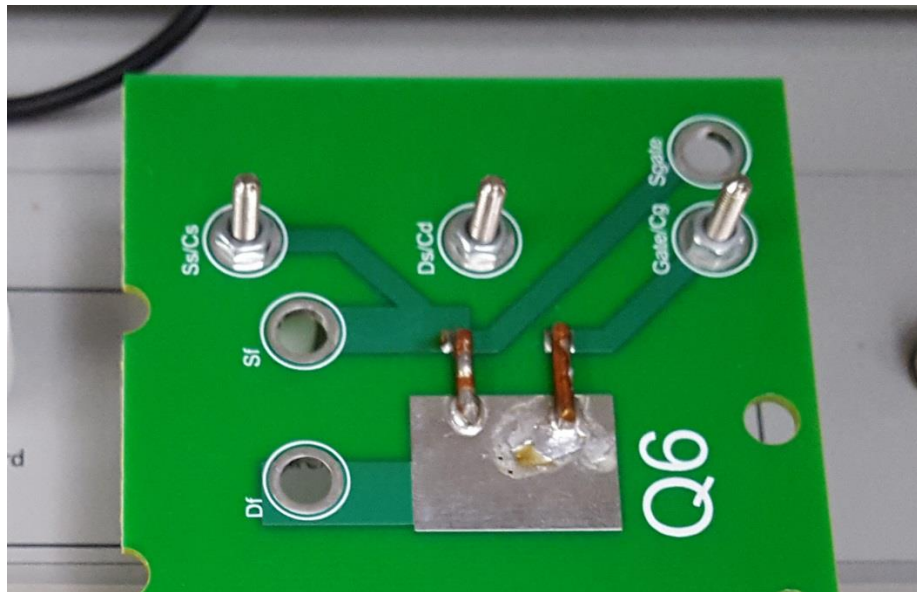


Figure 4.18. Capacitance test fixture adapter for a surface-mount device, configured for the short-circuit calibration.

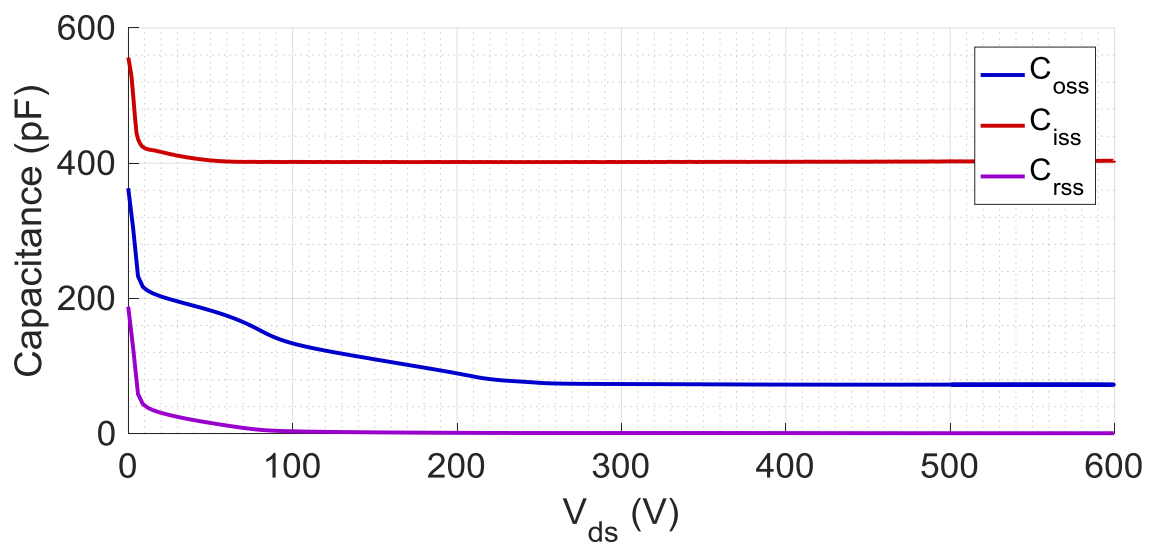


Figure 4.19. Capacitance characteristic for Infineon GIT, collected using Keysight B1505a.

$C_{gs}$  increases threefold as it approaches the threshold voltage.

Another special consideration for some GaN device is the connection of the thermal pad with the source terminal. The thermal pad is connected internally to the Si substrate of the device, and this pad must be connected to the source to reduce the effects of dynamic on-resistance. Some devices (such as the Infineon GIT) connect the thermal pad and source within its own package, where others (such as GaN Systems GS66508P) require that the two device terminals be connected externally on the PCB. Therefore, it would be easy to mistakenly measure the output capacitance from the drain to source with the thermal pad (and therefore substrate) electrically floating. However, this can neglect a significant amount of output capacitance, as shown in Figure 4.21.

#### 4.2.7 *Junction temperature control*

Control and monitoring of a device's junction temperature is an important part of the static characterization test setup. There are three common methods to control junction temperature. The first is placing the device in an oven or thermal chamber. With proper air circulation inside the chamber and enough time, this is the most accurate method. The biggest challenge for this option is the effect of the elevated temperature on the surrounding area of the device. If it is already mounted on a board for testing, all auxiliary components must be rated for that temperature. If it is connected to the curve tracer with alligator clips and cables, then those must also be capable of withstanding that temperature.

The second method is mounting the case of the device on a hot plate. This technique poses less risk to the surrounding components and connections, but may introduce error by allowing a temperature difference between the hot plate and the device junction. Measurement of the case temperature may not be an accurate representation of the junction temperature, since most of the case's encapsulant is exposed to ambient temperature. Figure 4.22 shows the test setups for these two common methods, and Figure 4.23 shows the error in measurement caused by the unknown

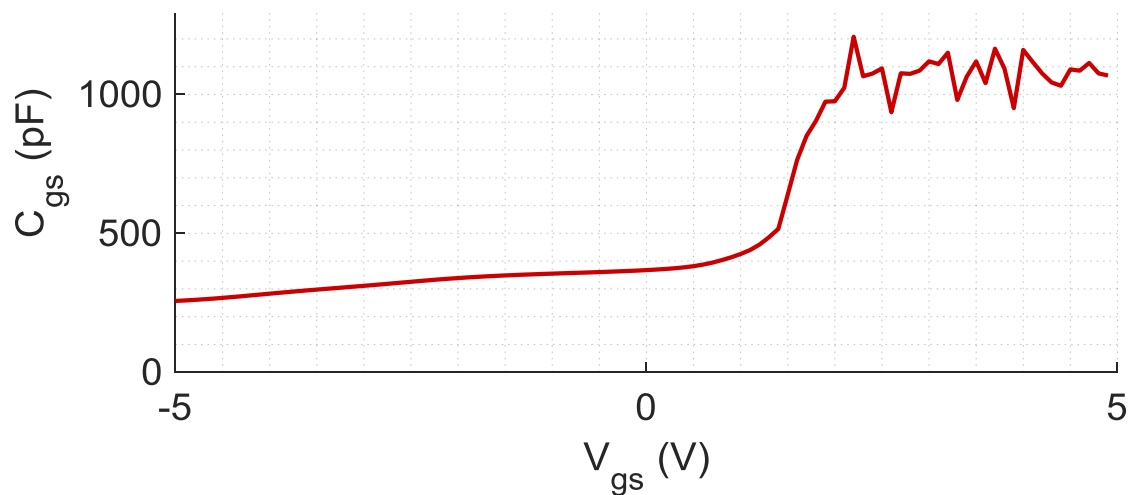


Figure 4.20.  $C_{gs}$ - $V_{gs}$  characteristic for Infineon GIT, collected using Keysight B1505a.

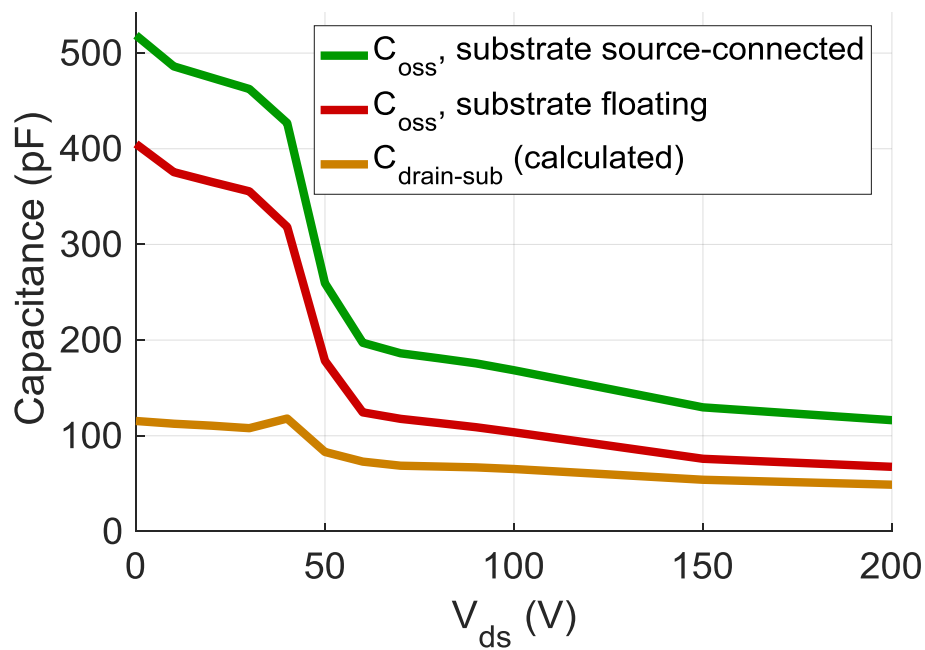


Figure 4.21.  $C_{oss}$  characteristic for GaN Systems GS66508P with and without the substrate connected to the source, collected using an impedance analyzer.

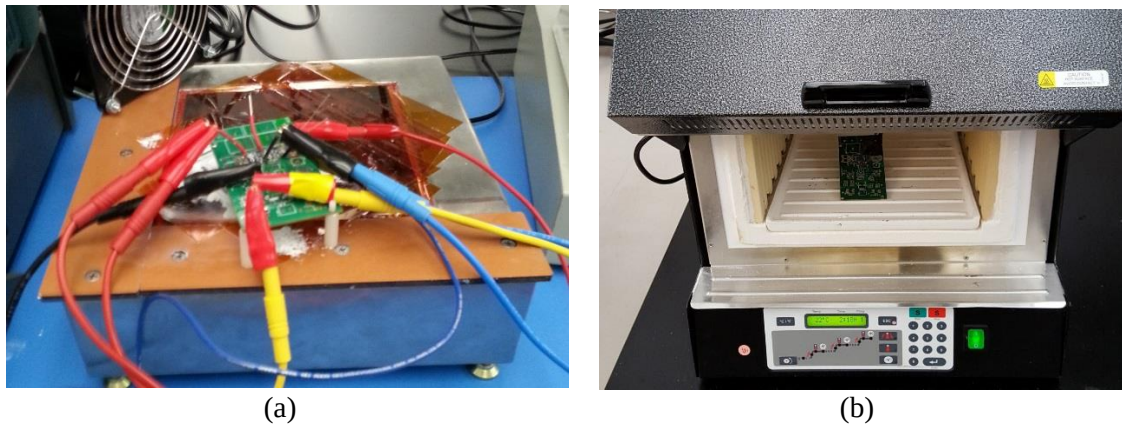


Figure 4.22. Two techniques of junction temperature control: (a) hot plate and (b) oven.

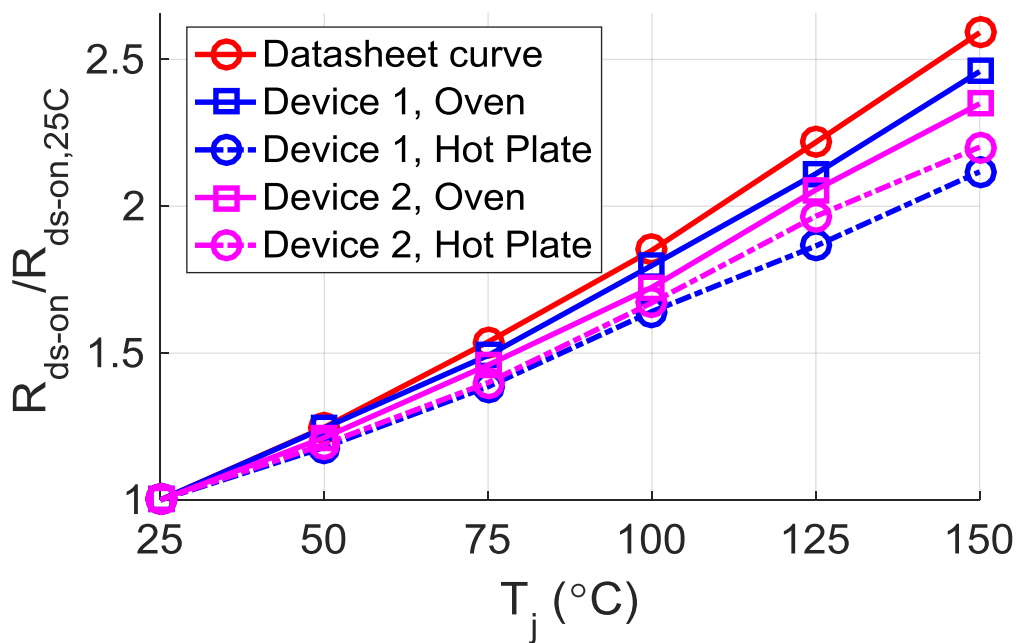


Figure 4.23. Error in on-resistance measurement for GaN Systems GS66508P with hot plate setup vs. oven.

temperature drop from the hot plate, as compared to the results when testing the same two devices in an oven.

A combination of the oven and hot plate methods may be most effective. The oven gives the most accurate results, but is not suitable for dynamic testing. However, once the on-resistance of a particular device is captured from testing in an oven, this curve can be used to precisely calibrate a hot plate test setup, so that the hot plate temperature setting is known for any desired junction temperature. This calibrated hot plate setup can then be used later to test the dynamic performance over temperature.

### 4.3 *Dynamic characterization*

The dynamic behavior of a GaN device is the most difficult aspect to characterize, because of the extremely fast switching and short duration of the transient. The conventional method for dynamic characterization is the double pulse test (DPT).

#### 4.3.1 *DPT setup*

The DPT is not unique to GaN FET characterization, but the very high  $dv/dt$  and  $di/dt$  and the nanosecond-scale transients impose stricter requirements than conventional Si MOSFETs. Figure 2.1 shows the circuit for a DPT, including the measured variables, control signals, and output capacitances. The low-side device behaves as the active device in this case, while the high-side device acts as a synchronous device in DLB mode. The high-side device can be replaced with a diode instead of another GaN FET, but the switching results for that case will no longer accurately represent the true switching losses in a phase leg converter. The DPT must mimic the intended application circuit as closely as possible in order for the resulting loss estimation to be accurate.

Two logical pulses are sent to the gate driver of the low-side device. The first pulse acts to establish the desired load current, and the end of the first pulse can therefore be used to study a turn-off transient at that current and voltage point. The beginning of the second pulse can then be

used to study the turn-on transient at that same current and voltage. The gate voltage, drain voltage, and drain current of the low-side/active device are typically measured in a DPT, partly because the active device's source terminal is a stable voltage for the ground reference of the oscilloscope.

Figure 4.24 shows an example bench setup for a DPT. The board itself is situated on a hot plate to control junction temperature, while the input dc capacitors and output load inductor are positioned in safer, room temperature locations. Voltage and current measurement probes are connected to an oscilloscope, and temperature measurement is also indicated for precise control of device case temperature. The logical pulses are provided here by a programmable function generator, although a DSP or FPGA can also be used to generate these pulses. Although not pictured here, short-circuit protection is strongly recommended during a DPT, such as with a solid-state

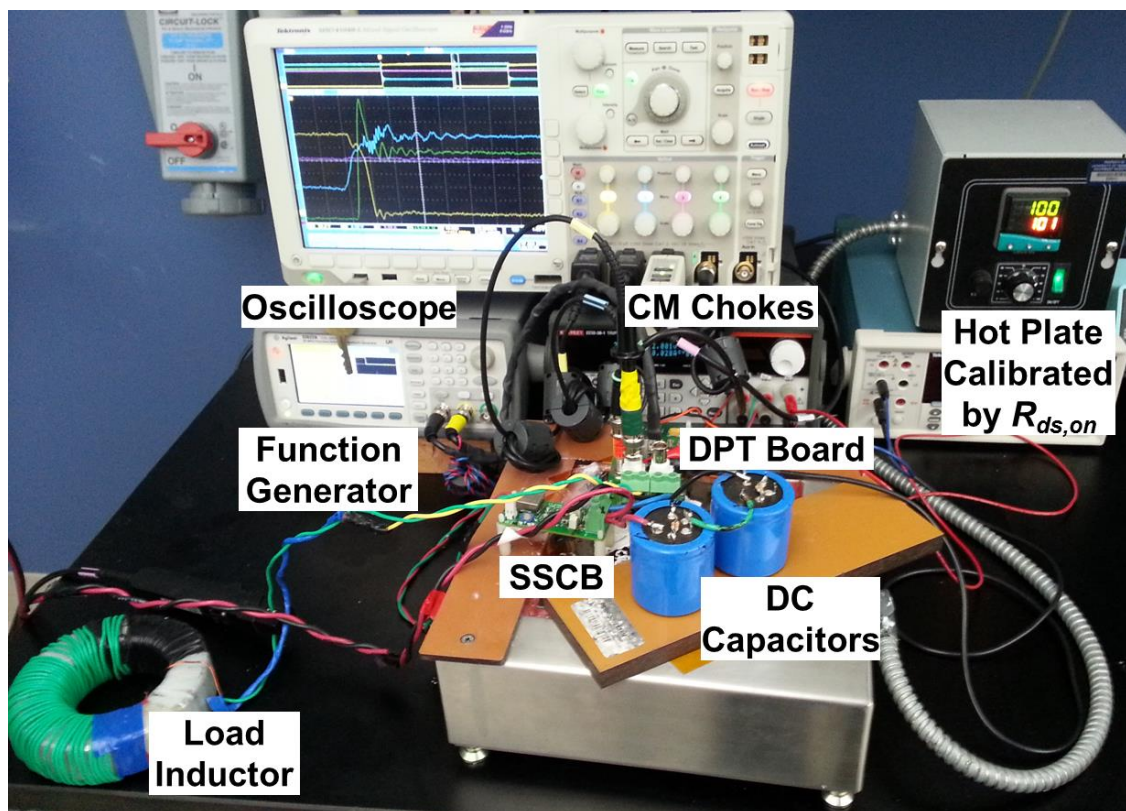


Figure 4.24. Double pulse test bench setup.

circuit breaker based on desaturation protection as described in [21], which can be positioned between the DPT board and dc bus capacitors to protect the devices under test from accidental damage.

#### 4.3.2 DPT board design

There are a few noteworthy distinctions for the GaN DPT board, or for any phase leg topology with fast-switching devices. First, the decoupling capacitance must be sufficiently high, and located very close to the devices to minimize the power loop inductance. Second, the gate resistances should be asymmetric, meaning a separate resistor path for the pull-up driver output (turn-on) and pull-down driver output (turn-off). This can be accomplished directly with some drivers, or a parallel diode may be added for a low-impedance pull-down resistance. Asymmetric gate resistance is helpful in controlling the turn-on and turn-off speeds independently, and also for mitigating cross-talk [239].

Lastly, the board must be designed to avoid false switching events due to noise in the signal path. The signal isolator or isolated driver IC must be rated for common-mode transient immunity (CMTI) at least as high as the expected  $dv/dt$  of the device [243]. The PCB layout must also be designed to separate the signal loop from gate and power loops. The layout must be fairly dense to minimize parasitic inductances from long traces [14]. Even with these measures, it is helpful to add a small capacitor directly to the input of the gate driver and signal isolator to filter noise.

Dynamic characterization is often used to precisely calculate the turn-on and turn-off switching energy losses,  $E_{on}$  and  $E_{off}$ , or various other features of switching waveforms. This usually involves designing the DPT board for the fastest achievable turn-on and turn-off speeds, without violating any device constraints. The key constraint may be the peak dynamic gate voltage or drain voltage, or it may simply be the maximum rated driving voltage with  $0\ \Omega$  external gate resistance. The switching speed limiting constraint may be different for each device under test, but it often



requires careful consideration of PCB power loop and gate loop layout, gate driver IC and signal isolator selection, and circuit parameters (driving voltage, resistances, decoupling capacitances).

#### 4.3.3 Voltage and current measurements

The challenges associated with dynamic measurement with GaN and fast-switching devices has been well-covered in other papers such as [53],[54]. The key takeaway is that both the probes and oscilloscope must be suitable for measurement at the desired voltage and bandwidth. The required bandwidth can be estimated based on the highest equivalent frequency of the measured waveform, given by

$$f_{eq} = \frac{0.45}{\min(t_r, t_f)}, \quad (4.5)$$

where  $t_r$  and  $t_f$  are the rise-time and fall-time of the measured waveform (current or voltage), respectively. This 0.45 factor is sometimes given as 0.35, depending on the model used for the measurement circuit. It is worth noting that the actual slew rate ( $dv/dt$  or  $di/dt$ ) is not a factor in this equation. Therefore, a 1-ns transient contains the same frequency components at any voltage. The desired bandwidth for GaN transient measurements is on the order of 1 GHz, since that should capture sub-nanosecond transients [246]. An example measurement setup might therefore be a Tektronix TPP1000 probe for measurements up to 300 V with 1 GHz bandwidth, or a TPP0850 probe for measurements up to 1000 V with 800 MHz bandwidth.

In addition to bandwidth, the oscilloscope must be capable of capturing high-resolution waveforms in both the horizontal and vertical scales. This means that the sample rate must be high enough to capture several samples during a nanosecond-scale transient. For example, the Tektronix DPO-4000 series oscilloscope allows up to 5 GHz sampling, and the DPO-5000 series allows up to 10 GHz sampling. Both of these oscilloscopes are compatible with the aforementioned probes. There are other suitable equipment setups available from other manufacturers, but this measurement setup was used to produce the data presented later in this section.

As described in [54], probe tip adapters and common-mode chokes should be used to minimize ground loop noise for capturing clean and accurate voltage waveforms. The root cause of this ground-loop noise is the shared common of all channels in the oscilloscope, connected to different grounding points on the board, which adds an inductance that can resonate with parasitic capacitances in the test setup. The ground of each probe should be connected to the board very close to the tip to minimize the loop, using an adapter such as 131-5031-00 for the TPP1000 probe or 013-0291-02 for the TPP0850 probe. Clip-on ferrite cores such as ZCAT3035-1330 from TDK can be used to easily add common-mode inductance to any probe cable and filter out ground loop current.

Drain current is particularly challenging for high-bandwidth measurement. Rogowski coils may provide a suitable bandwidth for some cases, but since most GaN devices are surface-mount components, it is challenging to find a wire or trace for the coil to clamp around. Coaxial current shunts, also called current viewing resistors, are the most common measurement device for this reason. Although a shunt may add several nH to the power loop inductance, the bandwidth of the measurement is in the GHz range. The GHz-bandwidth is accomplished with a four-terminal Kelvin connection: two terminals for the oscilloscope connection, and two separate terminals for the actual drain current to flow through the shunt resistance [47].

In terms of vertical scaling, an 8-bit oscilloscope provides a vertical resolution of  $\frac{V_{max}}{256}$  (e.g., 2 V resolution for a 500 V scale). Eight bits may be sufficient, as long as the vertical scale is adjusted precisely to optimize for each waveform. This is particularly important for accurate drain current measurement in turn-off, since the peak current for a turn-on transient may be several times higher than the peak current for the turn-off waveform in the same DPT. Re-scaling and re-pulsing with optimized vertical scaling for the turn-on and turn-off transient waveforms separately can resolve this issue easily.

#### 4.3.4 Deskew procedures for V-I alignment

For accurate calculation of the switching losses, it is vital that the deskew be set correctly for the current and voltage channels to eliminate V-I misalignment. Using the  $v_{ds}$  channel as a reference, the deskew setting of the  $i_d$  channel can be tuned so that the two signals are time-aligned. While there are many V-I alignment methods, two techniques that do not require any special test setup or fixture will be detailed here. The first is alignment of the initial turn-on voltage drop during the current rise-time with the time derivative of the current signal, according to

$$v_{ds} = (V_{dc} + V_{dlb}) - i_d R_{shunt} - L_{loop} \frac{di_d}{dt} \quad (4.6)$$

where  $L_{loop}$  is the total parasitic inductance of the power loop,  $R_{shunt}$  is the resistance of the current measurement shunt, and  $V_{dlb}$  is the forward voltage drop across the synchronous switch when in diode-like behavior (DLB) mode.

This technique can be performed graphically in the oscilloscope or in post-processing software such as MATLAB. The derivative function in the oscilloscope may induce some unspecified skew, so the derivative can be more accurately calculated in post-processing as

$$\frac{di_d}{dt}(t) = \frac{i_d(t + \Delta t) - i_d(t - \Delta t)}{2\Delta t} \quad (4.7)$$

where  $\Delta t$  is an increment of the sampling period. The ease of graphical alignment is limited by the amount of noise in the current measurement, which is amplified by derivation and may overpower the signal itself. Over-filtering of the signal may add skew, so  $\Delta t$  should be chosen as the lowest increment of sampling periods that provides a sufficiently clean  $di_d/dt$  waveform. An added benefit of this technique is that it requires adjusting  $L_{loop}$  until the magnitudes on either side of (4.6) match, which gives an indication of the total power loop inductance [204].

Figure 4.25 shows a flow chart describing it, and Figure 4.26 shows a step-by-step example of implementing this technique. In (a), an initial guess is made for  $L_{loop}$ , and only one sampling

period is used for  $\Delta t$ . The bounds of the current rise time are indicated with dashed lines for reference. It is difficult to estimate the correct  $L_{loop}$  in (a) due to the noise in the  $di_d/dt$  calculation, so the first step is to increase  $\Delta t$  to three sampling periods as shown in (b). Now, the estimated  $L_{loop}$  can be increased until the amplitude of the two plots match well as shown in (c). It is apparent at this point that the  $di_d/dt$  waveform is offset to the right, which can be correct by shifting the  $i_d$  waveform to the left. Shifting  $i_d$  by 1 ns as shown in (d) causes the waveform based on  $i_d$  to be offset to the left. Therefore, the properly deskewed waveforms are given in (e), where  $i_d$  is shifted earlier in time by 0.5 ns, as compared with the initial deskew setting of the current measurement. The oscilloscope's deskew setting for this channel can then be updated by adding or subtracting the necessary time shift, and the measured data will remain properly deskewed for any further tests.

The second method for V-I alignment relies heavily on the static characterization. According to [213],[247], the experimentally measured turn-on loss at 0 A can be calculated from the  $C_{oss}$  curve of the high-side device, according to

$$E_{on,0A} = \int_0^{V_{dc}} C_{oss}(v) \times (V_{dc} - v) dv . \quad (4.8)$$

At light load, the turn-on loss is very fast and sensitive to V-I misalignment, so this can be matched against several 0 A loss measurements to determine a proper current deskew setting. The beginning of the first pulse of a DPT is a 0 A turn-on, so this can be used to measure that loss directly. Several dc bus voltage points can be measured for further confidence, since the results of (4.8) are voltage-dependent. However, the error induced by stray capacitance in the PCB, other components, and measurement probes can limit the effectiveness of this method. If the  $di_d/dt$  deskew technique is first used to deskew the measurement setup, (4.8) can be used to back-calculate the amount of stray capacitance.

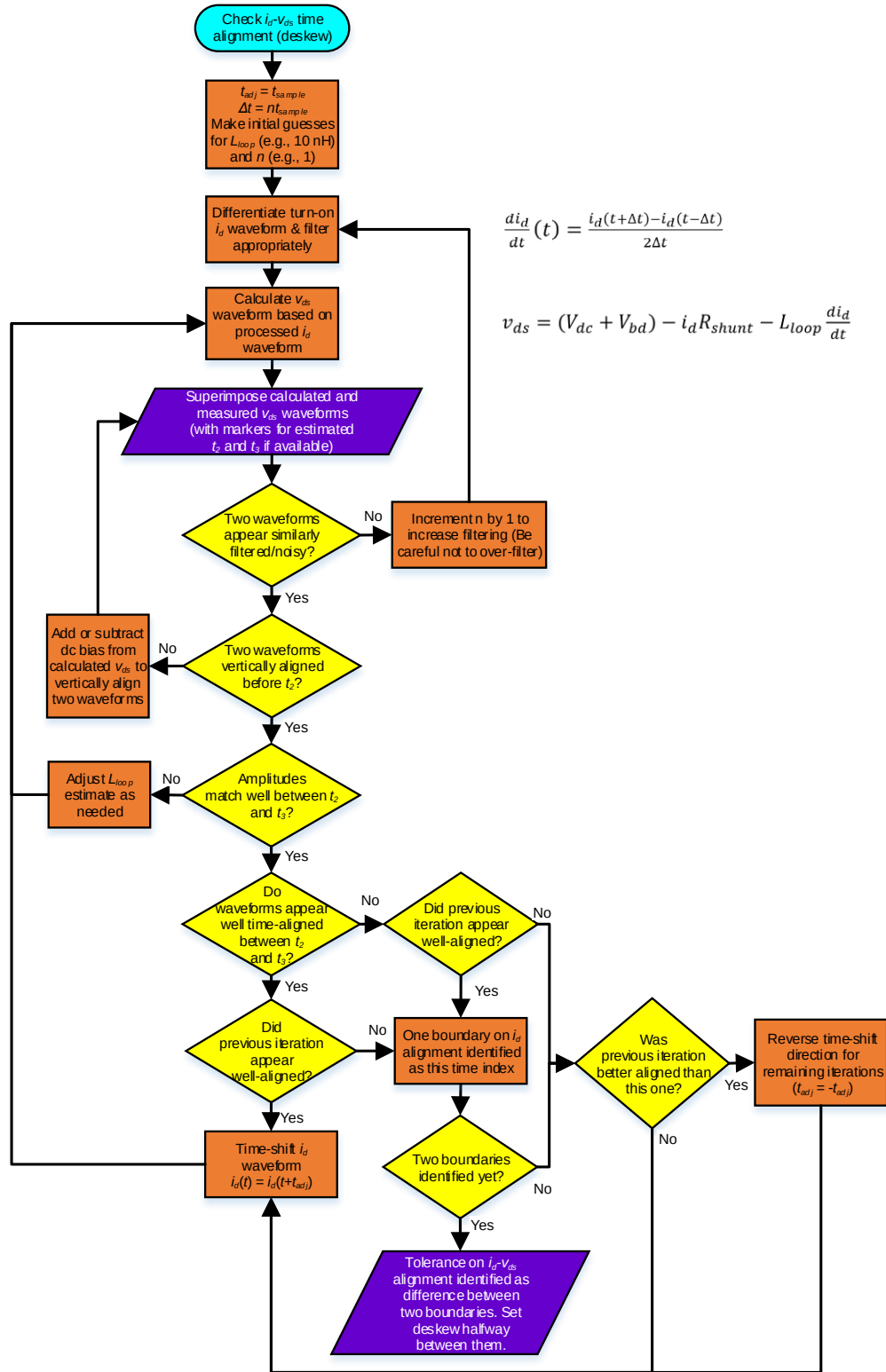


Figure 4.25. Flow chart describing the procedure for computational V-I deskew adjustment.

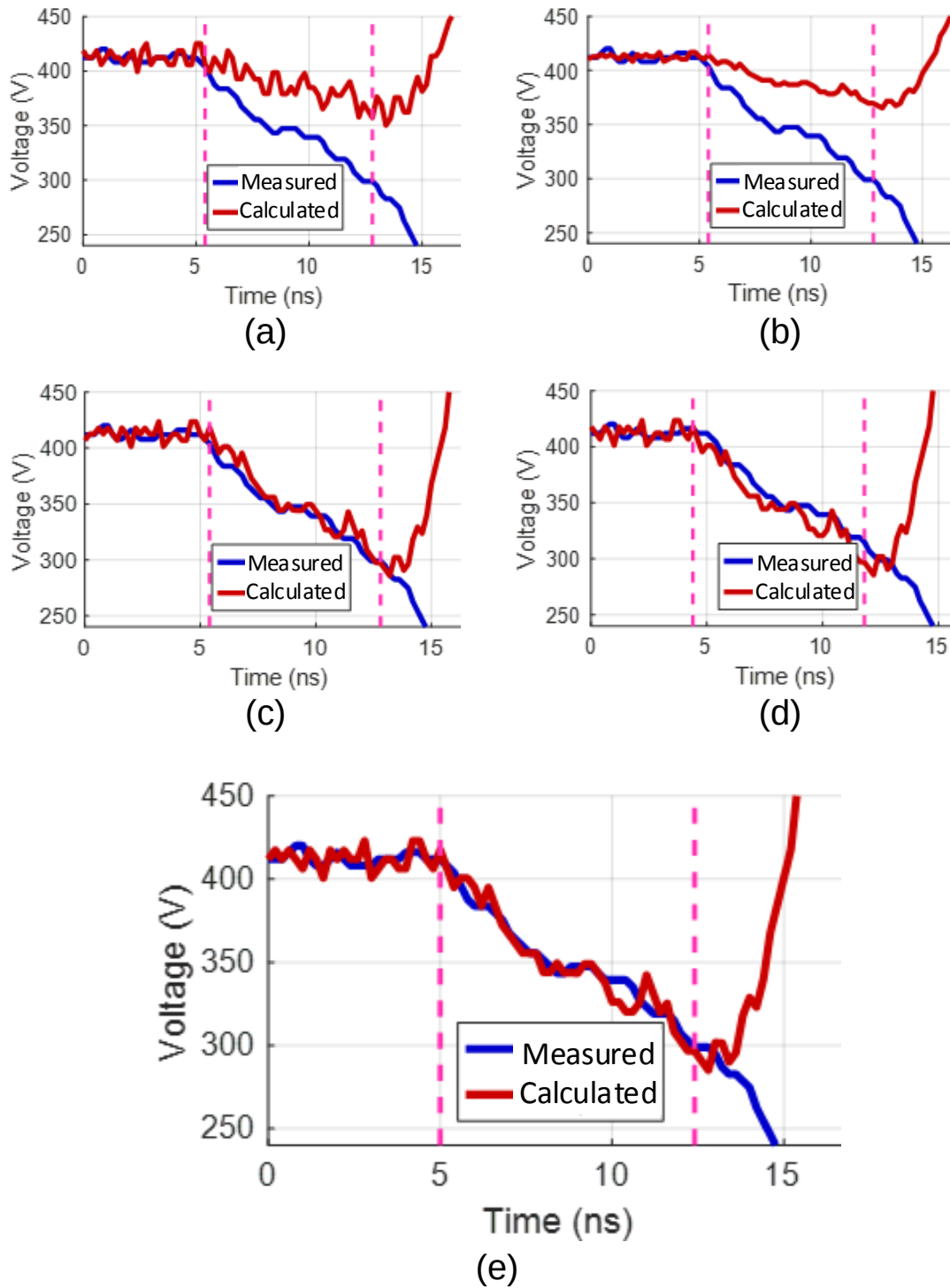


Figure 4.26. Step-by-step procedure for computational I-V alignment of DPT data shown through example waveforms, using example GaN FET DPT data. (a) Filter frequency too low; (b)  $L_{loop}$  amplitude too low; (c)  $i_d$  skewed to the right; (d)  $i_d$  skewed to the left; (e) Final selected deskew setting.

#### 4.3.5 Post-processing of data

Once turn-on and turn-off waveforms have been captured and the current and voltage waveforms are aligned, further analysis can be performed in post-processing as described by the flow chart in Figure 4.27. The first step in post-processing is to identify the turn-on and turn-off transients intervals from each waveform data set, as well as the timing subintervals within each transient. Figure 4.28 shows a flow chart for this procedure, and an implementation using MATLAB code can be found in Appendix A. Figure 4.29 and Figure 4.30 show examples of turn-on and turn-off waveforms for the GS66508P and Infineon GIT, respectively, with the timing variables labeled in each.

The turn-on delay time  $t_{d,on}$  is defined to begin when gate voltage changes from the off-state driving voltage (e.g. 0 V), detected based on the slope of the  $v_{gs}$  waveform. The current rise time  $t_{cr}$  starts when the slope of the  $i_d$  waveform becomes positive, and ends when the drain current reaches the load current. This marks the beginning of the voltage fall time  $t_{vf}$ , which ends at the zero crossing of  $v_{ds}$ .

The turn-off delay time  $t_{d,off}$  is defined to begin when gate voltage changes from the on-state driving voltage (e.g. 7 V), detected based on the slope of the  $v_{gs}$  waveform. The start of the current fall time  $t_{cf}$  can similarly be detected based on a negative slope in the drain current waveform, and the end of  $t_{cf}$  is detected based on the zero crossing of the drain current. However, devices with non-negligible package inductance may experience several  $i_d$  zero crossings before the end of the transient. Since the end of the current fall time is also marked by the peak overshoot of  $v_{ds}$ , the correct zero crossing should be the first time that  $i_d$  crosses 0 A with a negative slope that occurs after  $v_{ds}$  exceeds  $V_{dc}$ . With a fast gate voltage transient such as this, the voltage rise transition is the same as the current fall transition, so  $t_{cf}$  and  $t_{vr}$  are equivalent.

Once accurately triggered transient subintervals have been determined, the switching

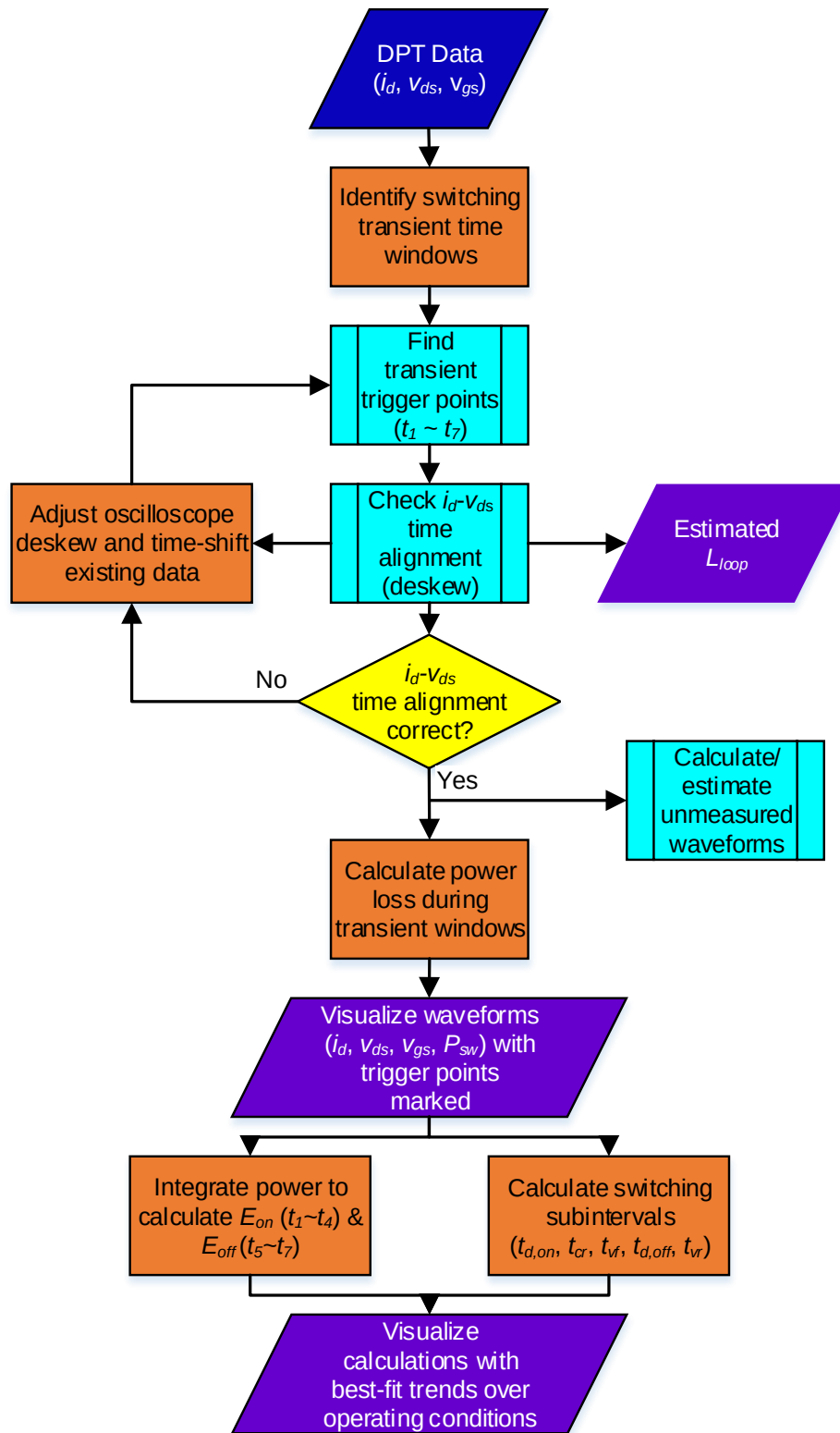


Figure 4.27. Flow chart describing the overall procedures for data processing of DPT measurements.



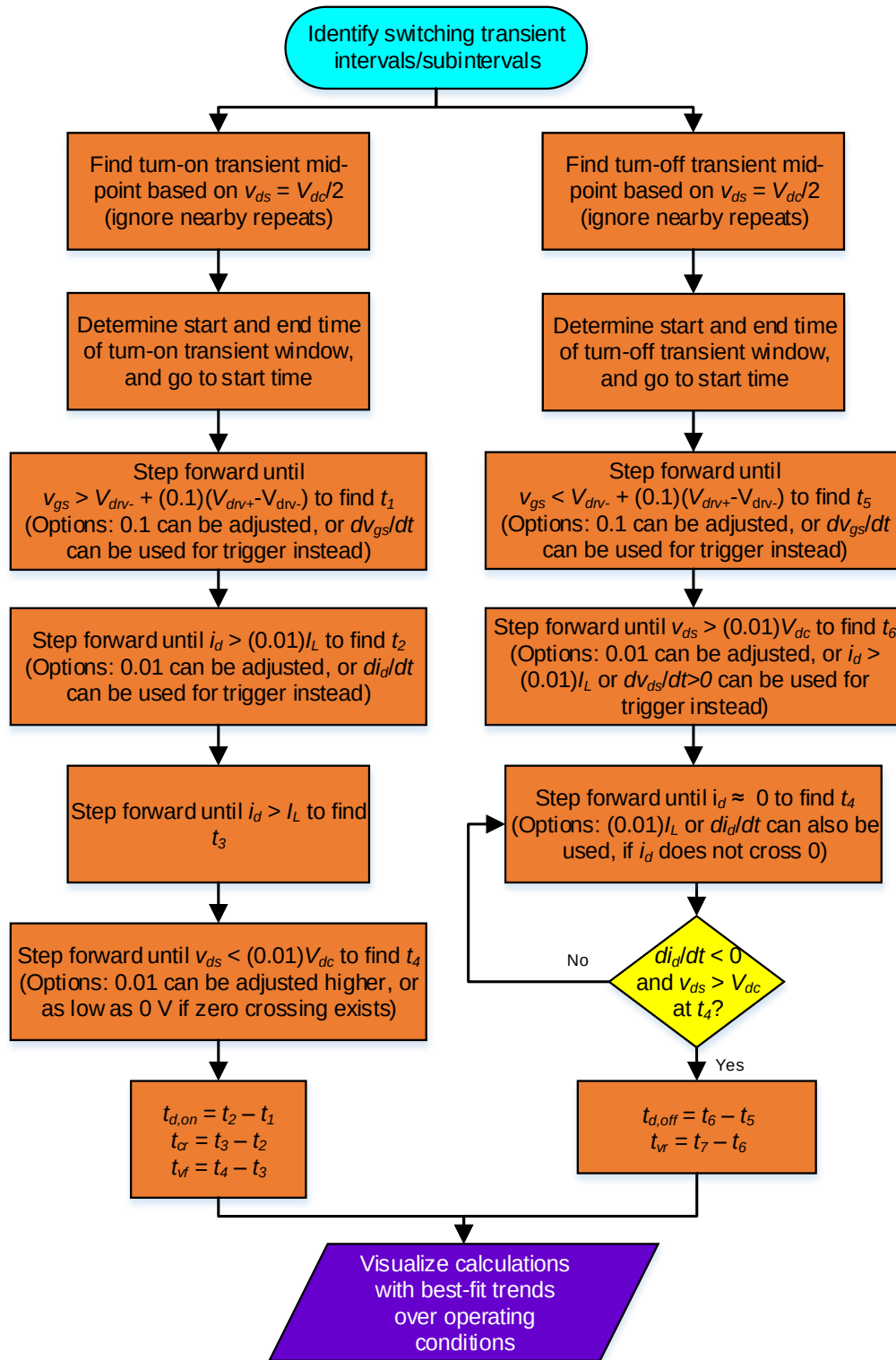


Figure 4.28. Flow chart describing the procedures for finding switching transient interval trigger points.

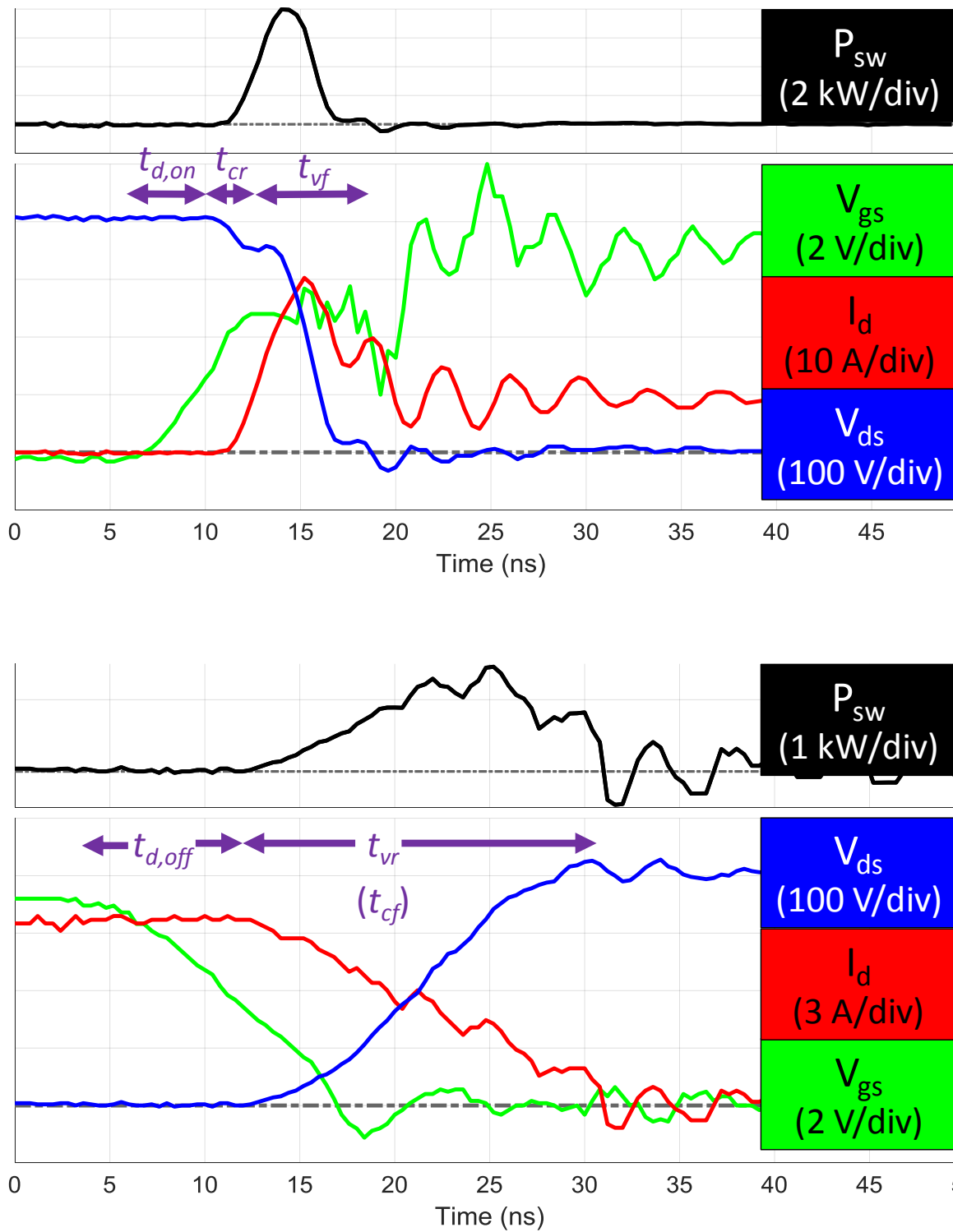


Figure 4.29. Turn-on and turn-off transient waveforms for the GaN Systems GS66508P, captured with 400 V dc bus and 10 A load current.

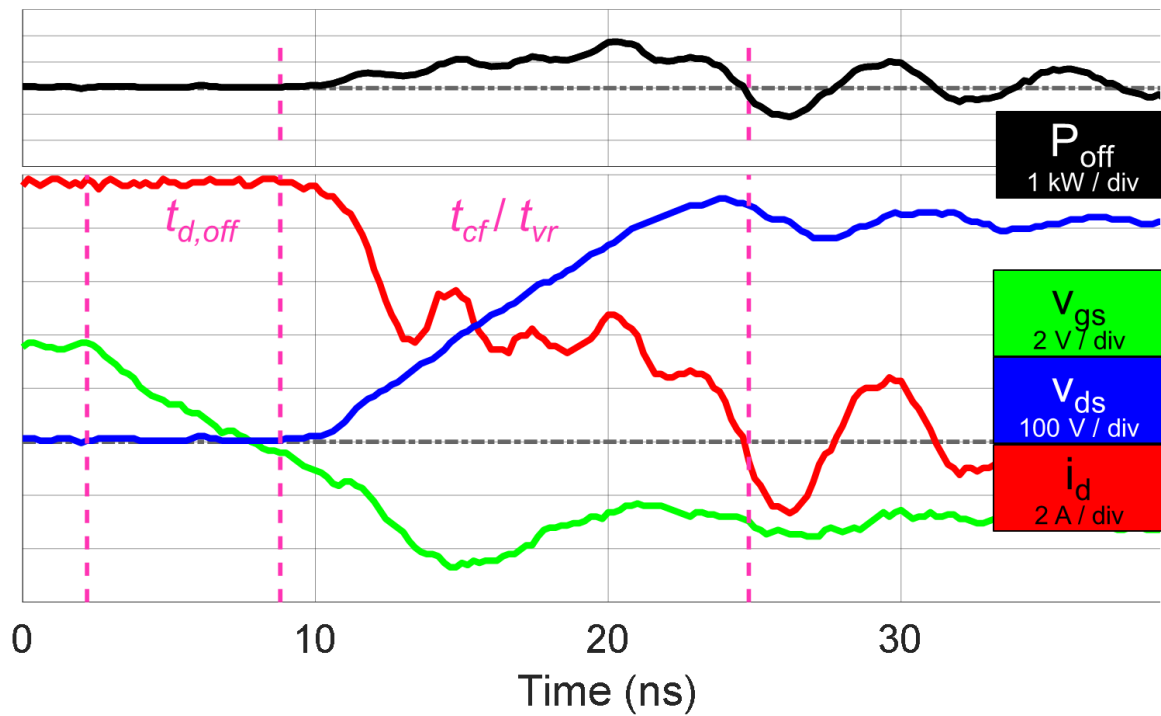
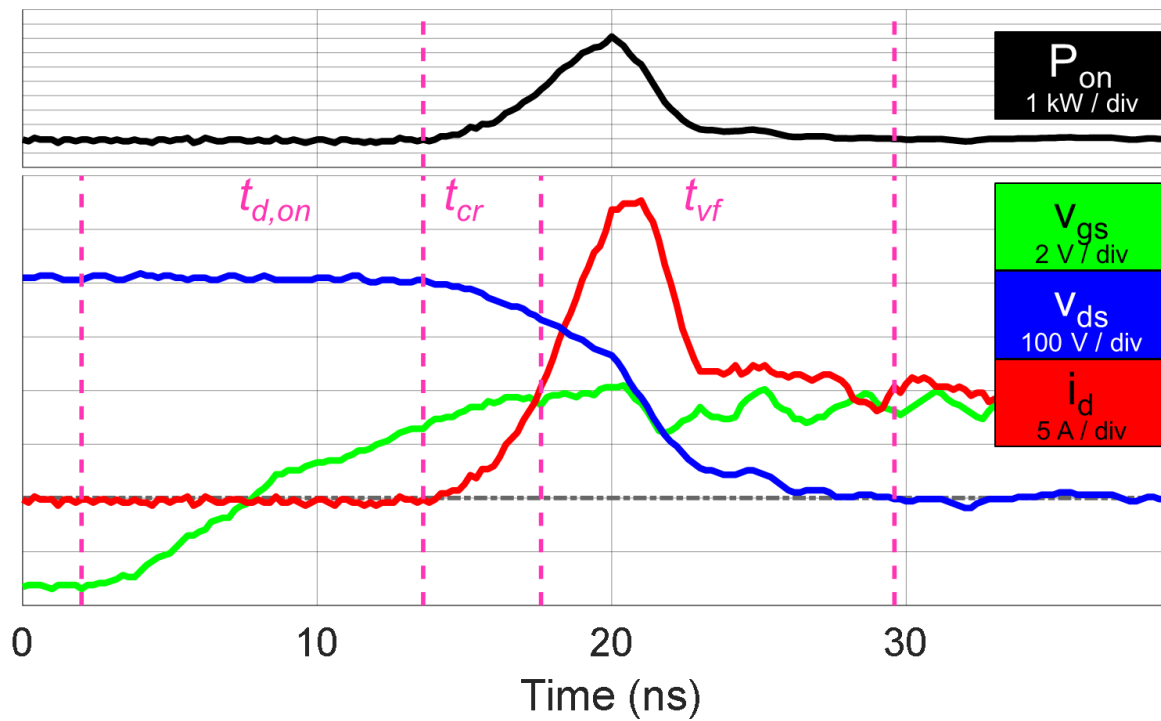


Figure 4.30. Turn-on and turn-off transient waveforms for the Infineon GIT, captured with 400 V dc bus and 10 A load current

energy losses can be calculated. The  $C_{oss}$ -related energy given by (4.8) is only a part of the turn-on switching loss. During the current rise time, overlap loss occurs due to some of the load current flowing through the channel while it operates in the saturation region, with a drain voltage near the dc bus voltage. Once the low-side channel current has taken over the full load current from the high-side device, there is further overlap loss as the load current continues to flow through the saturated channel and the drain voltage falls. The total turn-on loss can be calculated from a turn-on waveform using

$$E_{on} = \int_0^{t_{on}} i_d v_{ds} dt \quad (4.9)$$

where the bounds of the integral should include the current rise time  $t_{cr}$  and voltage fall time  $t_{vf}$ . The instantaneous power used for this integral is shown in the example waveforms of Figure 4.29 and Figure 4.30.

During the turn-on current overshoot, the active device discharges its output capacitance through its own channel and this energy is fully lost, but this current is internal and cannot be observed during a DPT. The energy lost by this internal  $C_{oss}$  discharge is measured during turn-off and is generally considered part of the experimentally calculated  $E_{off}$ . This energy is often called  $E_{oss}$ , and can be calculated from the  $C_{oss}$  curve using

$$E_{oss} = \int_0^{V_{dc}} C_{oss}(v) \times v dv . \quad (4.10)$$

Theoretically, this energy should be equal to the turn-off loss at 0 A, but the components and measurement probes on the DPT board may contribute additional switch-node capacitance that adds loss to  $E_{off,0A}$ . The turn-off loss should be relatively constant at light load, until the overlap loss begins to increase significantly. A trend of  $E_{off}$  vs.  $I_L$  typically converges at light load to a value  $E_{off,0A}$  that can be used to back-calculate the stray capacitance at the switch-node if  $E_{oss}$  is known.

$$E_{off} = \int_{t_{off}} i_d v_{ds} dt . \quad (4.11)$$

where the bounds of the integral should include the voltage rise time  $t_{vr}$ . The instantaneous power used for this integral is shown in the example waveforms of Figure 4.29 and Figure 4.30. Choosing the best end point for this integral is a challenge in switching loss calculation, because the drain current rings around 0 A repeatedly as the transient ends, and the first zero crossing of the drain current waveform may not actually give the total losses. The integral should end at the point when the maximum amount of energy has been stored in the output capacitor, because after this point, all ringing energy should sum to zero. Depending on the magnitude of current ringing, the final boundary of the  $E_{off}$  integral may therefore also be chosen as the point of peak  $v_{ds}$  overshoot. In theory, this should occur at the first zero crossing of  $i_d$ , but this may not be true at all voltage and current conditions.

Figure 4.31 and Figure 4.32 show the switching losses of GaN Systems GS66508P, using DPT results at 25 °C with 7 V gate drive and 0  $\Omega$  symmetric gate resistance, and calculated using (4.9) and (4.11) as a function of dc bus voltage and load current. It is worth noting that the  $E_{off}$  calculation from experimental results is difficult and not very accurate at low current (e.g. below 2 A) because the turn-off transient extends for hundreds of nanoseconds and accumulates significant error due to small measurement inaccuracies in the current waveform. However, because of the high switching speed of GaN FETs, the turn-off loss trend should be relatively flat at light load, so the loss below 2 A can be extrapolated based on experimental data in the 2-5 A range.

In fact, attempting to compensate the low-current waveforms to improve the accuracy of energy calculations may have the opposite effect. Figure 4.33 shows the turn-on and turn-off energy losses calculated for the Infineon GIT, with no dc bias adjustment performed. The turn-off loss appears to increase slightly from 2 A to 1 A, due to an apparent dc bias error in the current measurement. The inset of the figure shows that the current does not settle to 0 A after the transient

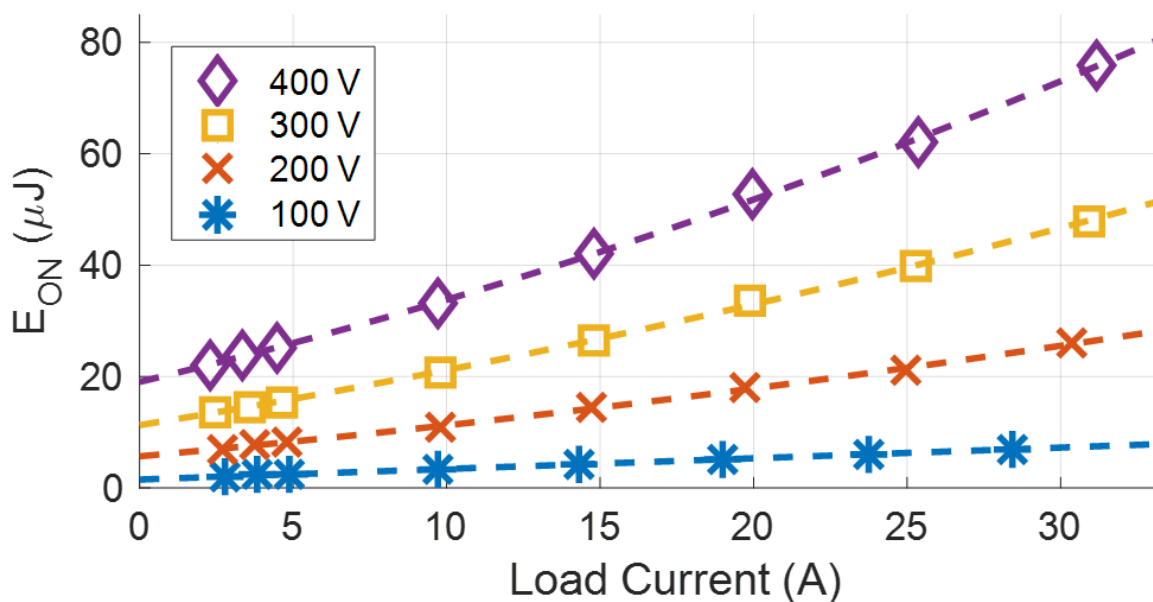


Figure 4.31. Turn-on switching energy loss calculated for GaN Systems GS66508P

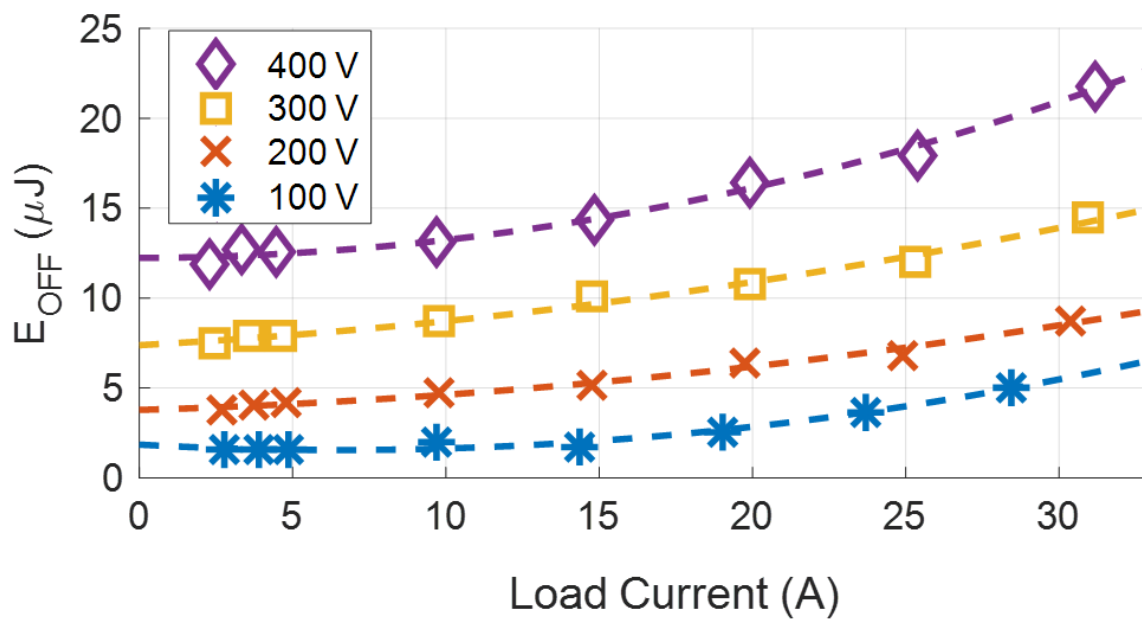


Figure 4.32. Turn-off switching energy loss calculated for GaN Systems GS66508P.

ends, but rather appears to resonate around a positive dc current. If each current waveform is shifted to compensate for the dc bias, so that the current always rings around 0 A after the transient is complete, the calculated  $E_{off}$  shows an apparent downward trend below 4 A as shown in Figure 4.34. However, the calculated  $E_{off}$  is constant from 3 A to 15 A, and this value matches well with the predicted  $E_{oss}$  from the  $C_{oss}$  waveform, so this downward trend below 3 A is incorrect. The data processed with no dc bias adjustment is therefore more accurate, despite the apparent error in the low current case.

In the turn-on waveform, the current overshoot during  $t_{vf}$  would normally be due partly to reverse recovery charge, but an enhancement-mode GaN FET does not experience reverse recovery. Instead, this overshoot is due to the displacement current that charges the high-side/synchronous device output capacitor as it turns off.

In the turn-off waveform, the voltage overshoot is due to the stored energy in the power loop inductance, which keeps the current flowing into the active device's output capacitance even after it has reached the dc bus voltage, overcharging it and resonating until the energy is damped out.

#### 4.3.6 Synchronous switch measurements

DPT measurements are typically performed on the low-side device, operating as the active switch, while the high-side device operates as the synchronous switch. The synchronous switch's behavior has a major impact on the switching transient of the active switch. Although using a diode for the high-side device may be acceptable, the results of such a test are only relevant in a buck converter where there is no synchronous switch. The turn-on and turn-off loss in the synchronous switch are typically assumed to sum to zero, because it operates in zero-voltage switching (ZVS) mode with its body diode or DLB mechanism. To confirm this, the  $v_{ds}$  and  $i_d$  waveforms of the high-side switch can be measured with the same passive probes and other methodology already

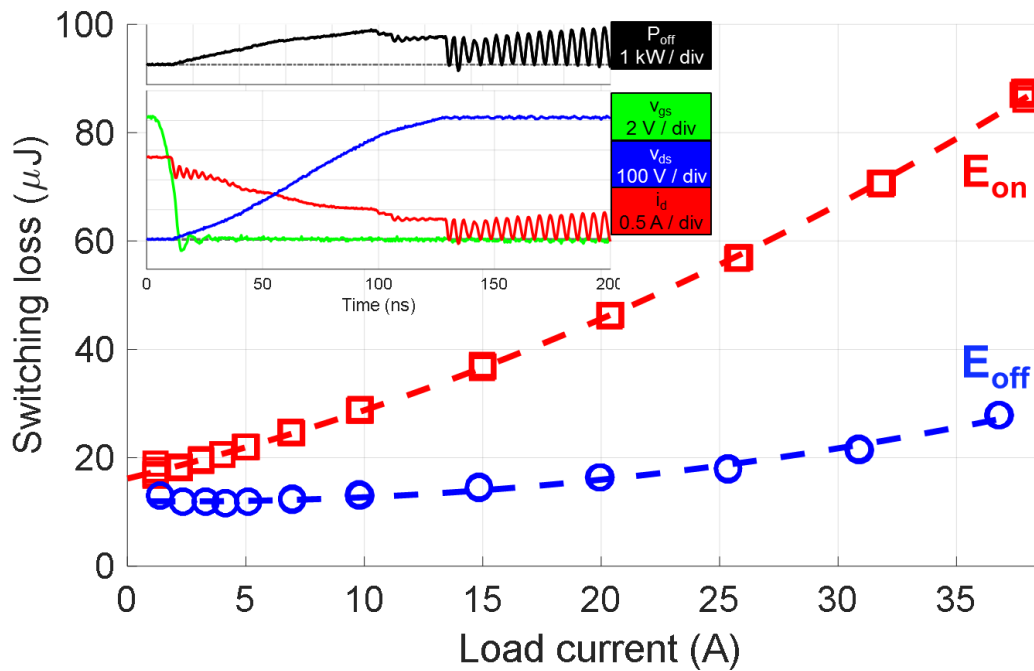


Figure 4.33. Turn-on and turn-off switching energy losses calculated for Infineon GIT at 400 V, with no dc bias adjustment. Inset time base waveform shows the turn-off transient at 1 A.

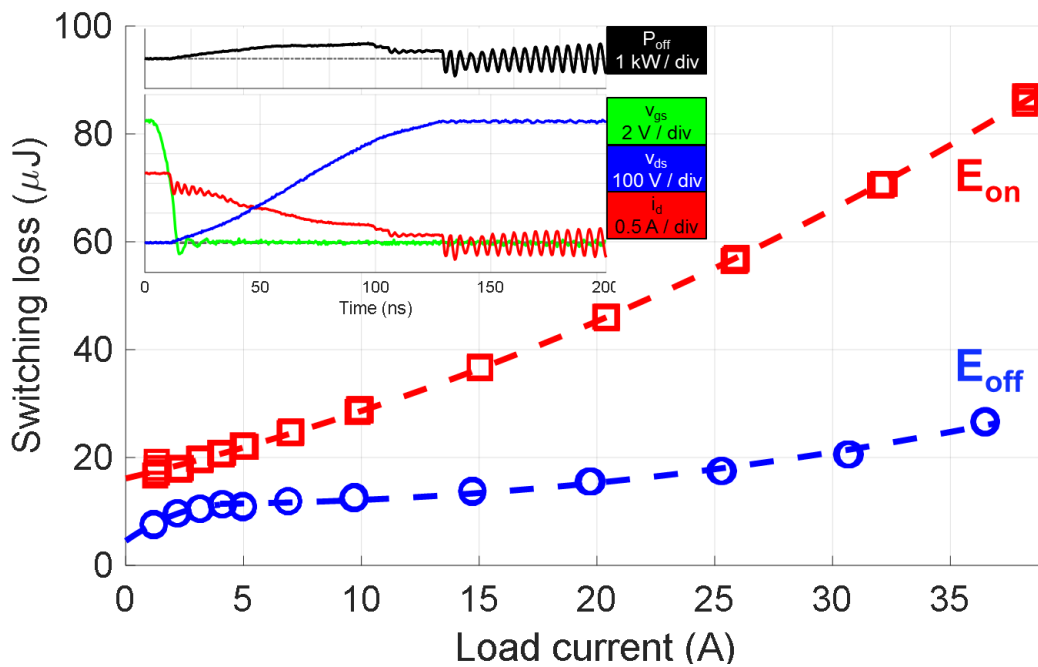


Figure 4.34. Turn-off switching energy loss calculated for Infineon GIT at 400 V, with dc bias adjustment applied to  $i_{\text{d}}$  measurement. Inset time base waveform shows the turn-off transient at 1 A.



described. In such a test, the DPT board must be grounded at the DC+ node with the rest of the board floating. This means that no other passive probes can be connected, and the polarity of the voltage probe must be reversed to measure  $v_{sd}$ . Measuring the gate voltage of the high-side switch is notoriously challenging, even with a differential probe. In some cases, it is more convenient to rearrange the test setup so that the low-side device acts as the synchronous switch, as shown in Figure 4.35.

The turn-on and turn-off waveforms from this test setup can be time-aligned to the active switch measurements in the typical DPT setup using the  $i_d$  waveform, which should be nearly identical in both cases but vertically offset by  $I_L$ . Figure 4.36 and Figure 4.37 show an example of these time-aligned waveforms during a hard turn-on and turn-off transient of the active switch. Measurement of the synchronous switch has many potential applications, including measurement

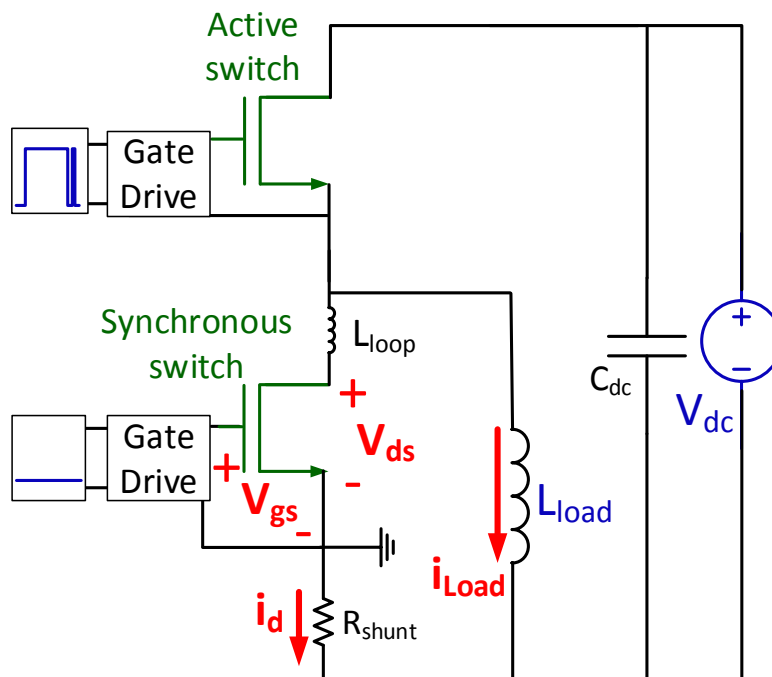


Figure 4.35. DPT circuit used for characterization of the synchronous device as the low-side switch.

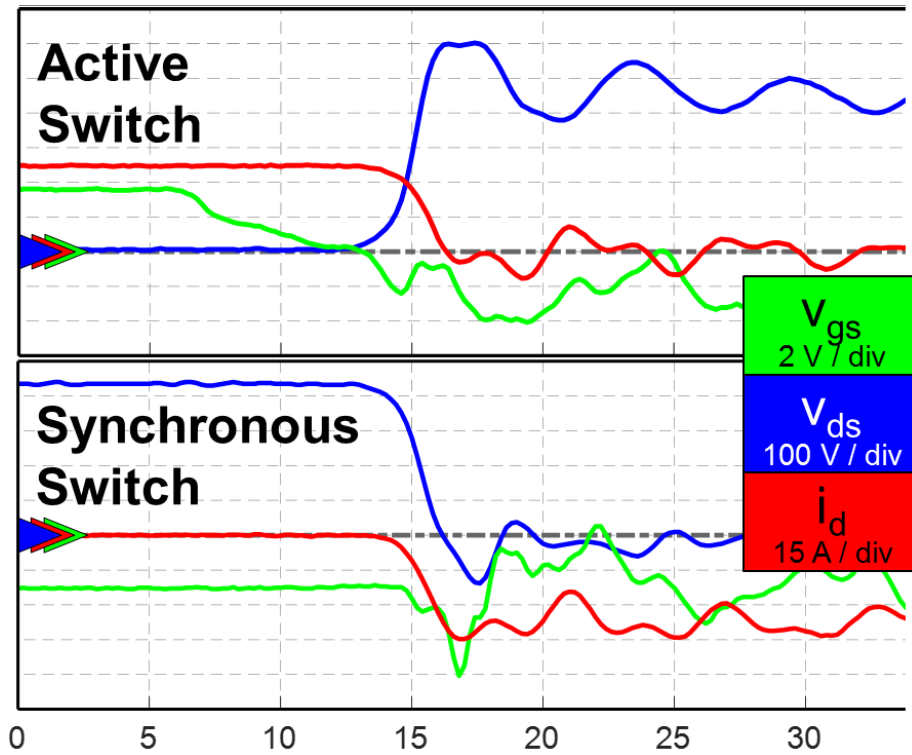


Figure 4.36. Switching waveforms for active and synchronous switches for the Infineon GIT during a hard turn-off of the active switch, captured with 450 V dc bus and 35 A load current.

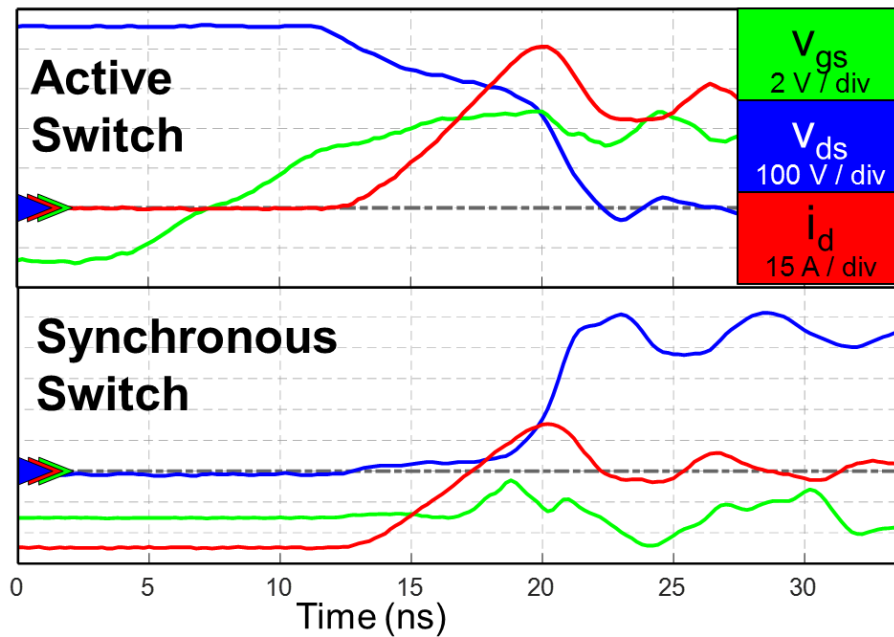


Figure 4.37. Switching waveforms for active and synchronous switches for the Infineon GIT during a hard turn-on of the active switch, captured with 450 V dc bus and 35 A load current.

of cross-talk loss as discussed in the next chapter.

#### 4.3.7 Calculating internal or unmeasured waveforms

Another technique for post-processing analysis is the calculation of waveforms representing internal device variables or other unmeasured parameters by combining the measured data with the static characterization results. Some of these procedures are described in the flow chart shown in Figure 4.38, and an example is shown in Figure 4.39.

For example, the voltage on the parasitic loop inductance and on the synchronous switch can be calculated using (4.7) and

$$v_{ds, sync} = (V_{dc} - v_{ds, active}) - i_d R_{shunt} - L_{loop} \frac{di_d}{dt} . \quad (4.12)$$

In a similar manner, the internal  $v_{ds}$  of the active switch can be calculated to compensate for the parasitic inductance internal to the device package, using

$$v_{ds, internal} = v_{ds, measured} - L_{ds} \frac{di_d}{dt} . \quad (4.13)$$

The inductances of the power loop and the internal package inductance may not be known initially, but both can be estimated from the post-processing of various dynamic waveforms. The loop inductance is a convenient result of the deskew procedure on an active switch during a hard turn-on. Similarly, the internal package inductance can be determined by applying (4.13) to the synchronous switch during a hard turn-on of the active switch as in Figure 4.37. In the turn-on transient, the drain voltage is clamped at  $\sim 0$  V by the body diode or DLB mechanism until  $i_d$  reaches 0 A. Therefore, the non-zero  $v_{ds}$  in Figure 4.37 from 12 to 17 ns is actually the voltage across the internal inductance. In this example, the internal  $L_{ds}$  can be approximated as  $\sim 2$  nH. This same technique can then be applied to compensate  $v_{ds}$  in other transient waveforms, including the active switch if the same device is used for both.

Additionally, the current flowing through the output capacitance of each switch can be calculated using the nonlinear capacitance curve from static characterization and

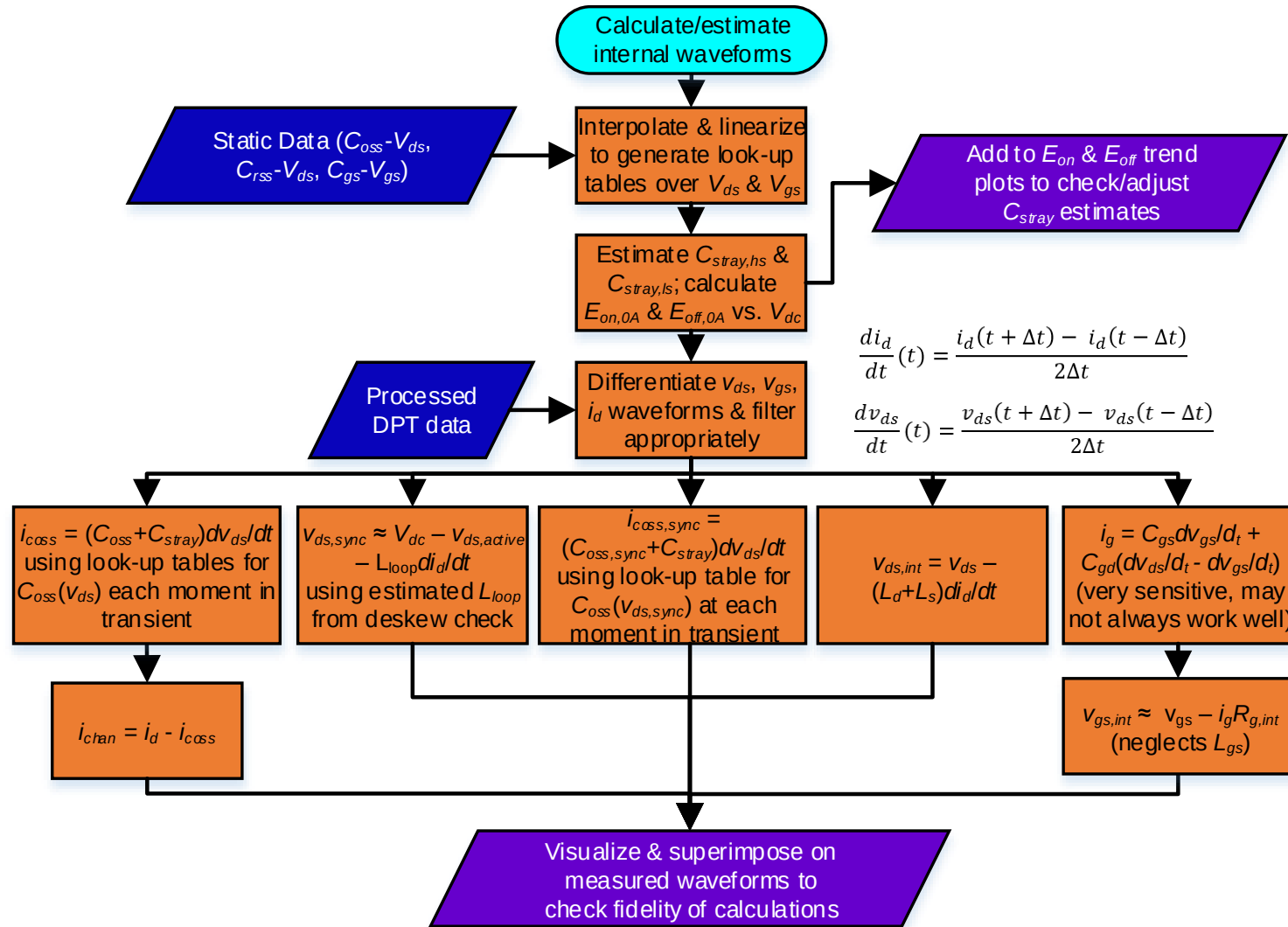


Figure 4.38. Flow chart describing the procedures to calculate waveforms for internal or unmeasured parameters.

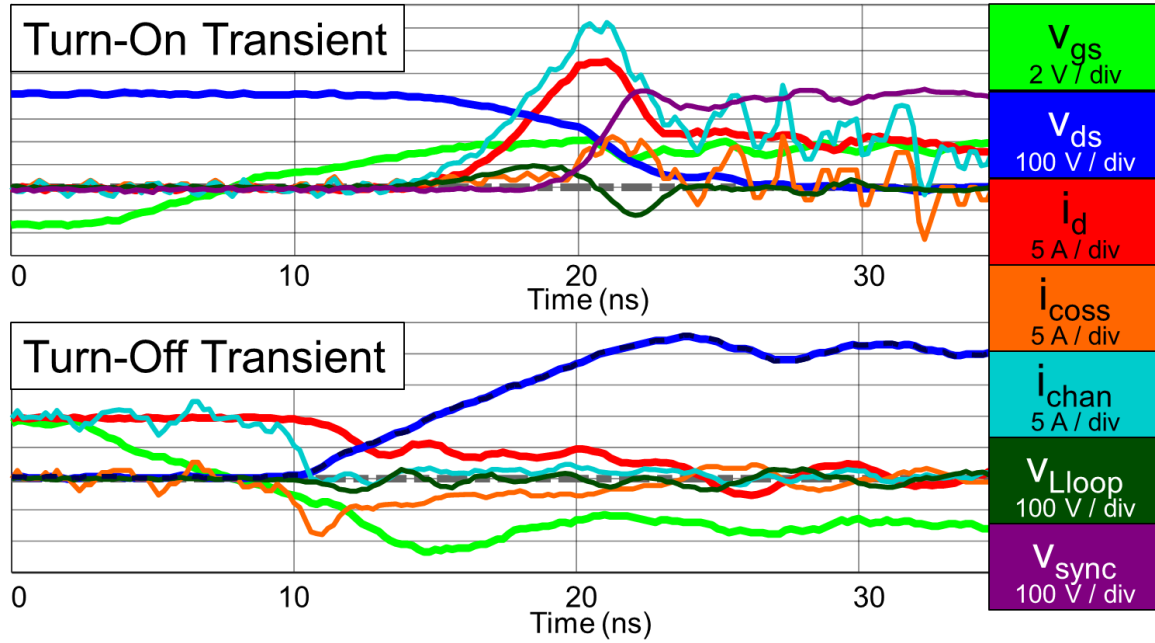


Figure 4.39. Turn-on and turn-off transients for Infineon GIT with additional unmeasured waveforms, calculated based on measured data.

$$i_{coss} = C_{oss} \frac{dv_{ds}}{dt}. \quad (4.14)$$

The capacitance must be determined at each instant during the transient as a function of the  $v_{ds}$  waveform at that time. Then, the internal channel current of the active switch can be calculated based on the drain current and this  $C_{oss}$  current, using

$$i_{chan} = i_d + i_{coss}. \quad (4.15)$$

A few of the useful outputs of this calculation include the peak channel current and the time required for the channel to turn off.

#### 4.4 Summary

Once both static and dynamic characterizations have been completed, a wealth of information is available for the converter design. The conduction and switching losses can be predicted for any given operating condition, including the additional loss component from DLB

conduction in dead time. Device breakdown can be prevented using the turn-off transient waveforms and the drain-source leakage current characteristic. Gate driver parameters and overall PCB layout can be designed and verified through DPT.

Performing a static characterization on a GaN device can be relatively straightforward with the right equipment, but there are many choices and settings to optimize before the results can be trusted. Dynamic characterization also requires specific measurement equipment, in addition to a well-designed DPT board with suitable probe connections. Post-processing of both static and dynamic test results can extract the desired information from a large data set of sweeps and waveforms. With an understanding of these techniques and challenges, characterization of GaN FETs can be a valuable asset to the converter design process.

## Chapter 5

### Experimental Study of Cross-Talk in a GaN-Based Phase Leg

#### 5.1 Introduction

As mentioned in the previous two chapters, cross-talk is a common issue with WBG power devices, particularly when the gate drive circuit is designed for the maximum achievable switching speed. Although active or multi-level driving solutions can be implemented to mitigate cross-talk, the most conventional method is simply to reduce the switching speed by using a higher turn-on gate resistance. This presents a design tradeoff between cross-talk loss and overlap loss, prompting an in-depth study of the relative contribution of losses from each. Because cross-talk loss occurs in both devices of the phase leg, the losses are difficult to characterize with the conventional double pulse test setup. A comprehensive study of the cross-talk mechanism for an enhancement-mode GaN device (GaN Systems GS66508P) was therefore performed to better predict overall switching losses.

#### 5.2 Test setup

The current flowing through  $C_{gd}$  is proportional to the  $dv_{ds}/dt$  in both the active and synchronous devices. The turn-on speed and magnitude of  $dv_{ds}/dt$  is highest at light load, high dc bus voltage, and low temperature. Driving with 0  $\Omega$  gate resistance at 400 V, 25 °C, and 1 A results in a peak  $dv_{ds}/dt$  of 200 kV/ $\mu$ s. This study will focus on experimental results at 400 V and 25 °C, because these conditions produce the fastest switching and the worst case for cross-talk. The driving voltage was chosen as 7 V, the maximum rated steady-state gate voltage from the device manufacturer.

Three separate gate drive cases were studied for switching loss measurement in the active device. The results of these experiments were compared to estimate loss due to cross-talk as well as overall switching loss.

The circuit shown in Figure 5.1 (a) was used to measure the overlap and  $C_{oss}$ -based switching losses, with limited impact from cross-talk. For this case, the synchronous device gate and source sense terminals were shorted together directly at the device pads, providing a low-impedance gate loop path for the  $C_{gd}$  displacement current to flow. Because of the internal device resistance and inductance, there may still be enough ringing on  $v_{gs,int}$  to turn the synchronous device on, but this could be considered the “best case” for limiting cross-talk. However, it is not practical to use this design for a synchronous switching buck converter or phase-leg topology.

The circuit shown in Figure 5.1 (b) could be considered the “worst case” for cross-talk, because the same gate resistance was used for both turn-on and turn-off. This is generally not recommended for WBG devices, but it is still sometimes used for the sake of simplicity.

Finally, the circuit shown in Figure 5.1 (c) is the one recommended by the device manufacturer. It uses an asymmetric gate drive, with a discrete gate resistor for turn-on that is bypassed by a low-impedance Schottky diode in the turn-off path. This could be considered the “practical case,” because it allows the designer to mitigate cross-talk while still controlling the switching states of both devices.

The synchronous device in a phase leg is typically considered to operate in ZVS and experience no switching losses, but this is no longer true with the effects of cross-talk. Figure 4.35 allows for experimental analysis of the switching transients in the synchronous device. The same DPT board and test setup is employed, but the load inductor is connected to the low-side device rather than the high-side device, and the logic inputs to the high-side and low-side of the gate driver are reversed. In this configuration, the synchronous device is the low-side device and therefore the device under test.



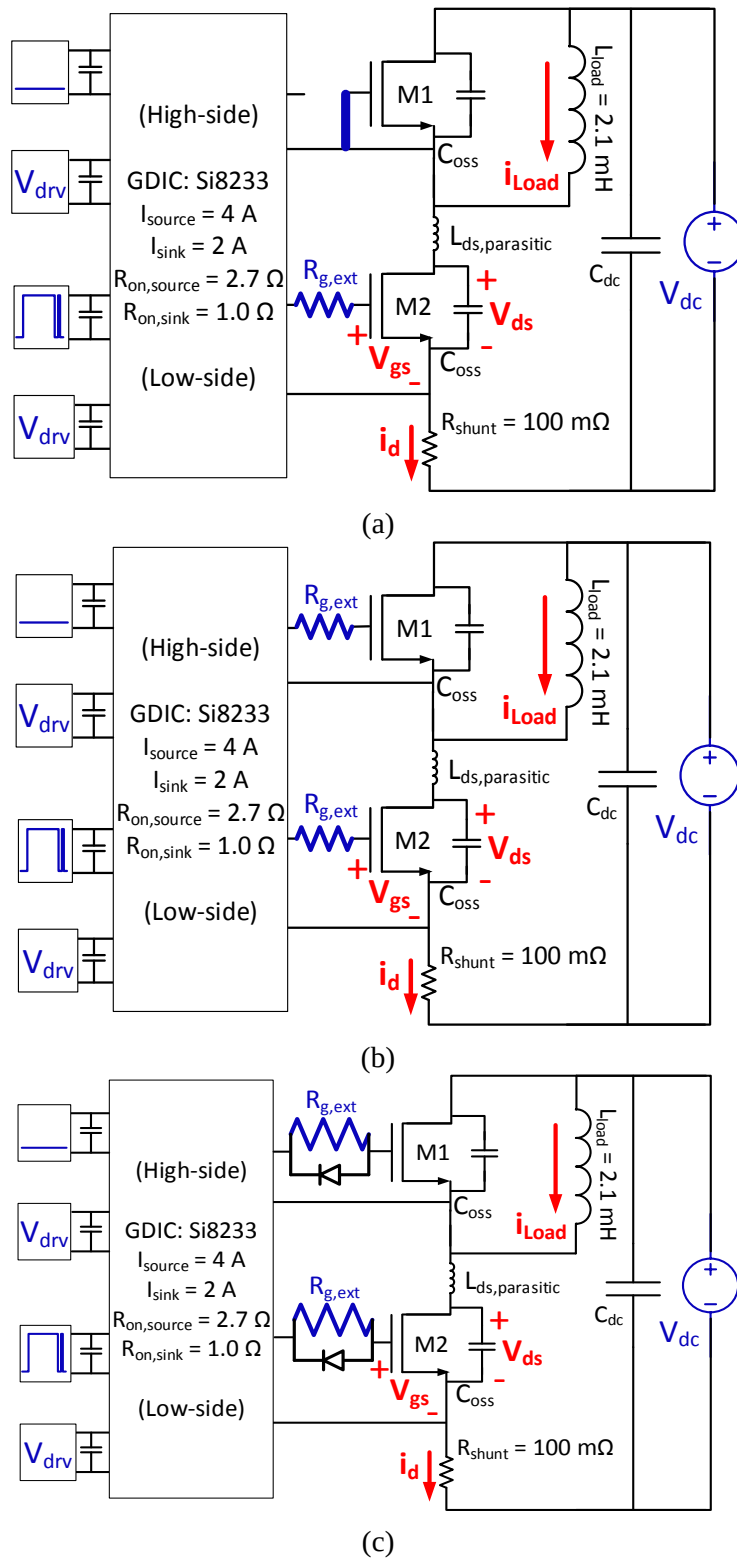


Figure 5.1. Double pulse test circuit schematic. (a) with no cross-talk, (b) with symmetric gate resistance, (c) with asymmetric gate resistance.

### 5.3 *Effect of cross-talk on active switch*

The effect of cross-talk on the turn-on transient can be seen clearly in Figure 5.2 and Figure 5.3. Figure 5.2 compares the best case and the worst case with a gate resistance  $R_{g,ext}$  of 10  $\Omega$ , showing a longer turn-on time and a shoot-through current of about 20 A in the worst case. Figure 5.3 compares the best case and practical case, showing very little effect from cross-talk with an asymmetric gate drive. However, the overall turn-on loss can still be greatly reduced by dropping the gate resistance to 0  $\Omega$ . In this case, using an asymmetric gate drive is not necessary, since the 0  $\Omega$  resistance is the primary path for turn-on or turn-off and bypasses the Schottky diode completely.

As expected, the turn-on loss of the active device is correlated to both load current and gate resistance. This is true for all three of the cases described. Figure 5.4 shows the turn-on loss for the cross-talk best case, with the synchronous device gate-source input shorted. Figure 5.5 shows the additional turn-on losses caused by cross-talk with the worst case, estimated by subtracting the best case loss from the worst case loss. These cross-talk losses become prohibitive with even as little as 5  $\Omega$  gate resistance. Part of this additional energy is lost as the shoot-through current flows through the saturated active device channel, and some extra overlap energy is lost, when the shoot-through current extends the turn-on transition.

Figure 5.6 shows the additional turn-on losses caused by cross-talk in the practical case, estimated by subtracting the best case loss from the calculated practical case loss. Unfortunately, Figure 5.6 does not show a clear trend of loss vs. gate resistance or load current. This calculation assumes that no spurious switching occurs in the best case, which may not be accurate due to ringing on the internal gate loop impedance. However, some general conclusions can be drawn. The results show that cross-talk losses with an asymmetric gate driver are approximately 5  $\mu\text{J}$  in the active device. An inverse correlation is expected between this loss and gate resistance, because

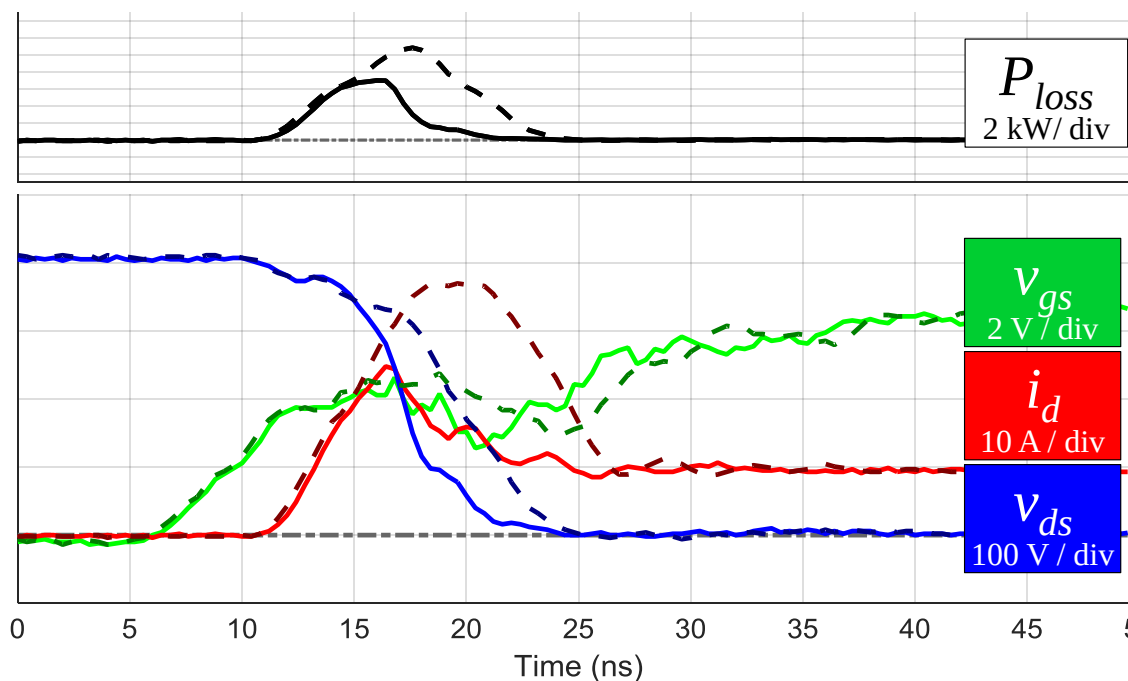


Figure 5.2. Turn-on transient waveforms of GS66508P at 400 V and 10 A with  $R_{g,ext} = 10 \Omega$ , showing the best case as a solid line and the worst case as a dashed line.

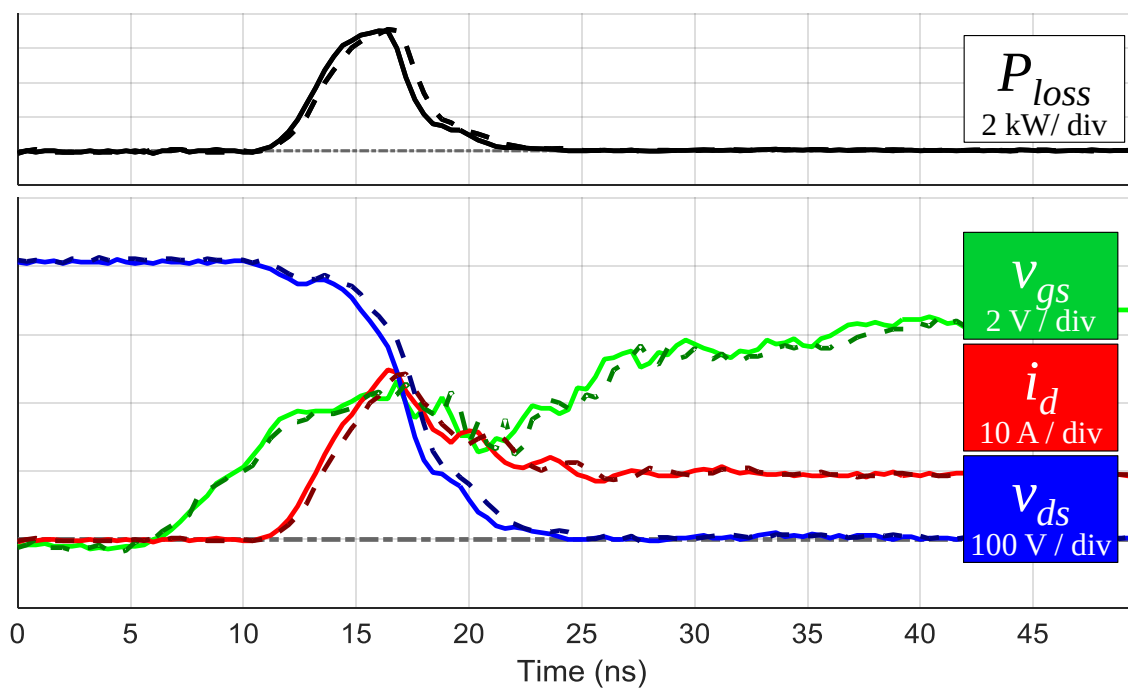


Figure 5.3. Turn-on transient waveforms of GS66508P at 400 V and 10 A with  $R_{g,ext} = 10 \Omega$ , showing the cross-talk best case as a solid line and the asymmetric drive case as a dashed line.

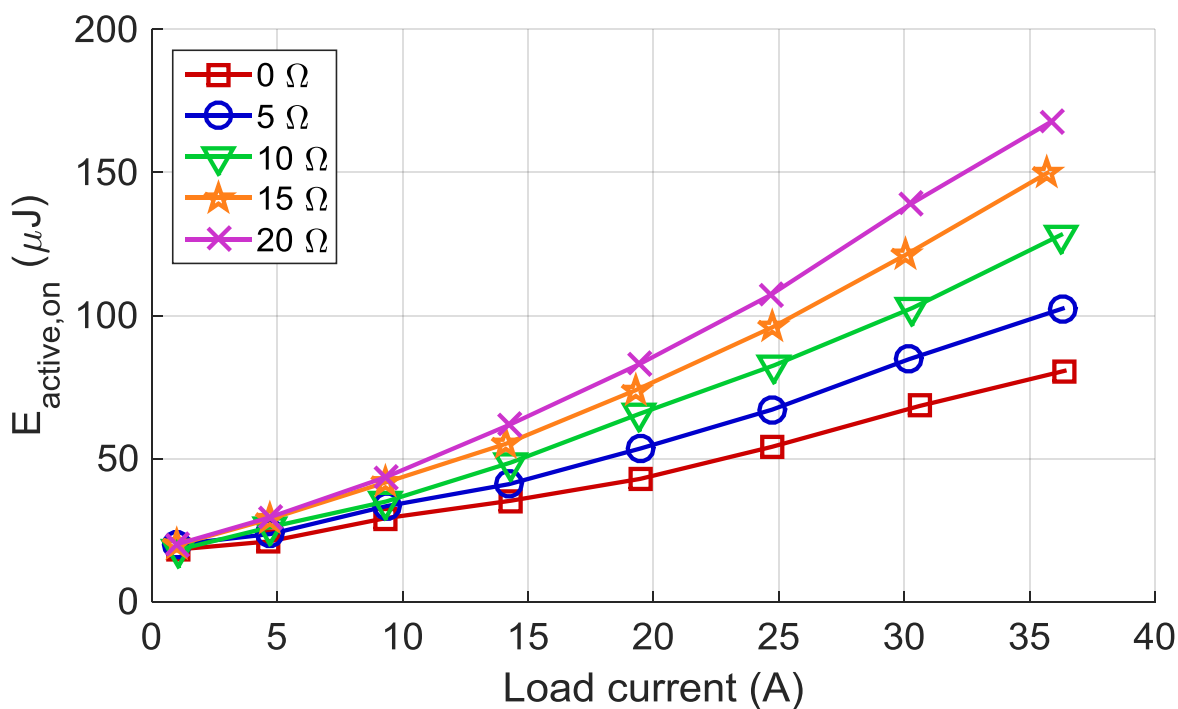


Figure 5.4. Turn-on loss of GS66508P for an active device, with the cross-talk best case gate drive circuit.

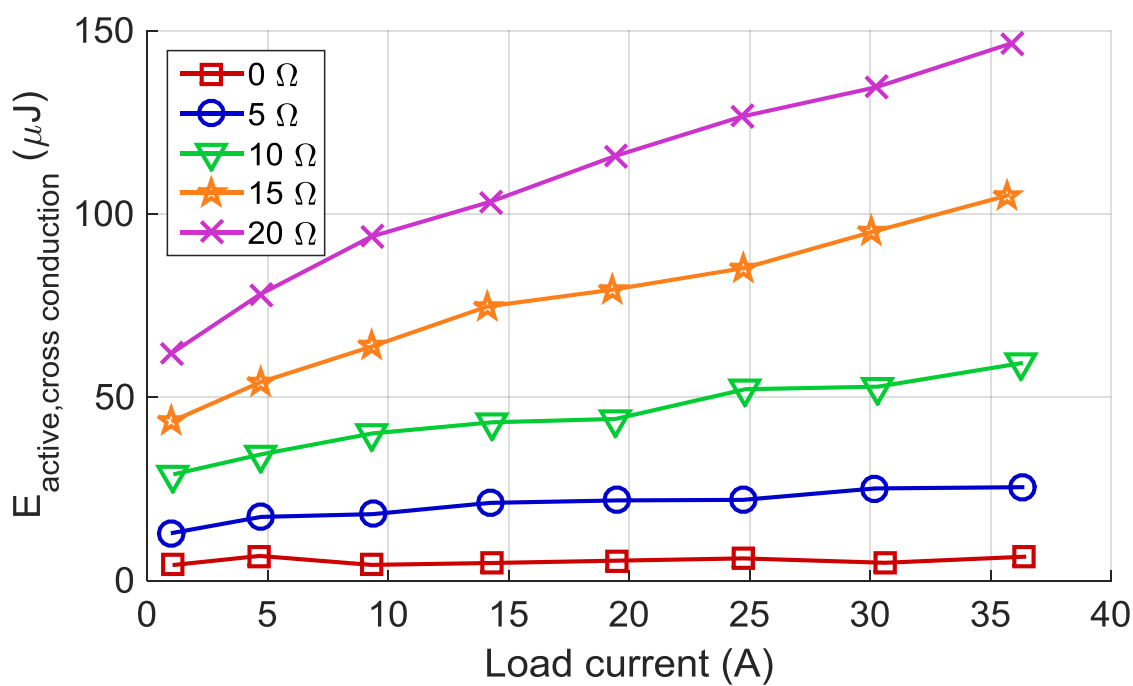


Figure 5.5. Additional turn-on loss of GS66508P due to cross-talk, with the cross-talk worst case gate drive circuit.

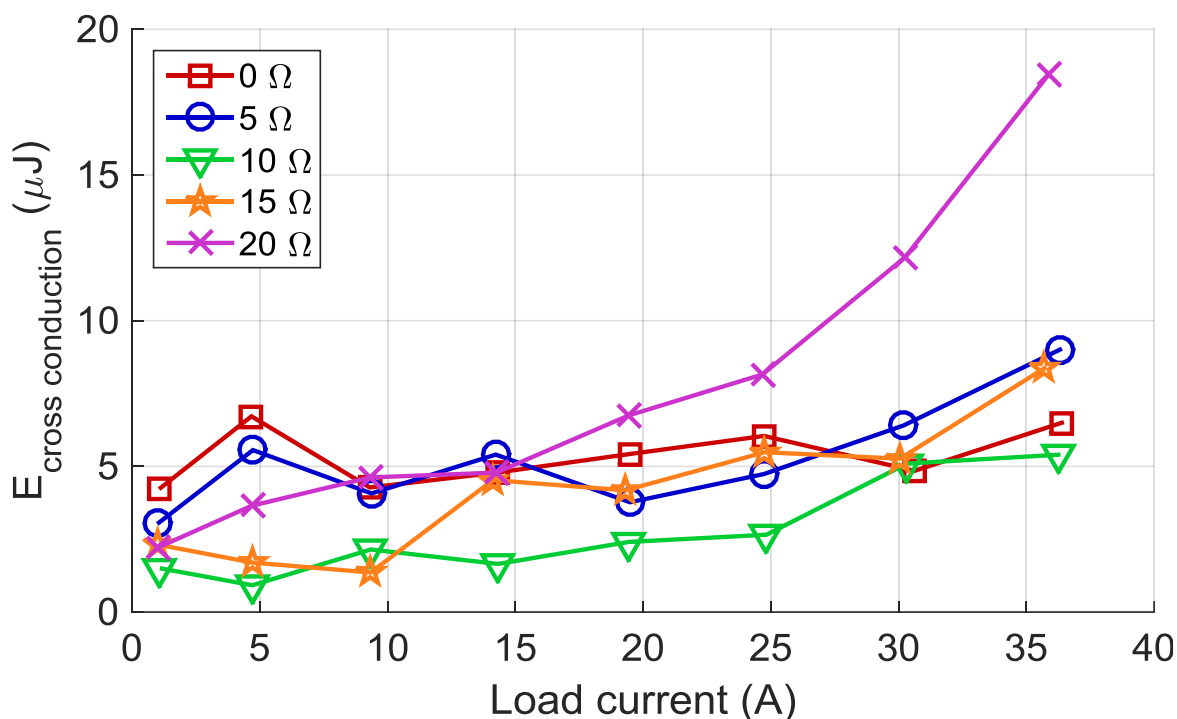


Figure 5.6. Additional turn-on loss of GS66508P due to cross-talk, with the practical case using an asymmetric gate drive.

the overall  $dv_{ds}/dt$  of both active and synchronous devices is strongly determined by the turn-on gate resistance of the active device. This is not obvious from the results shown in Figure 5.6, but some verification is provided in the synchronous device analysis presented in the next section.

Choosing a conventional (i.e. symmetric) gate drive circuit with a non-zero gate resistance also increases the turn-off loss, as shown in Figure 5.7. The active device turn-off loss with 0 Ω mostly consists of the energy stored in the device's output capacitance  $C_{oss}$ , but there is significant overlap loss as the turn-off gate resistance is increased. With an asymmetric gate drive, the turn-off loss is approximately the same as the 0 Ω case in Figure 5.7, because the Schottky diode provides a very low impedance path for turn-off gate current. Considering turn-on, turn-off, and cross-talk losses in the active devices, the 0 Ω gate resistance case clearly results in the lowest losses by a significant margin. However, the cross-talk losses in the synchronous device must also be considered.

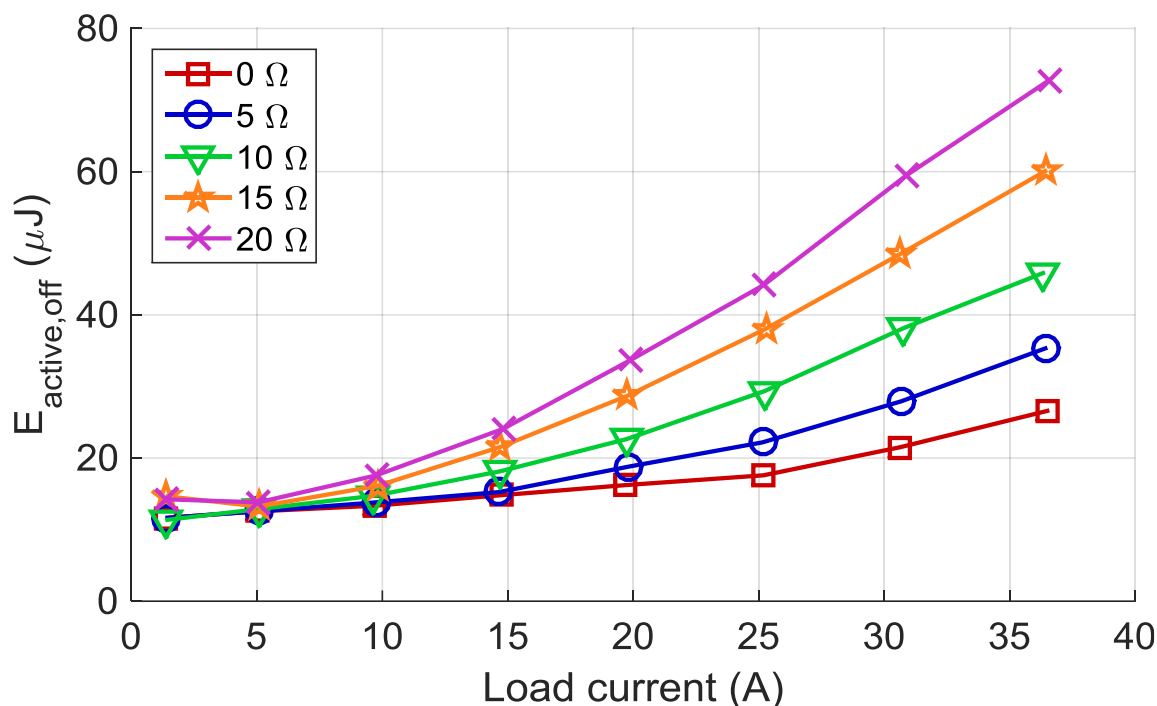


Figure 5.7. Turn-off loss of GS66508P for an active device in the cross-talk best case.

#### 5.4 Effect of cross-talk on synchronous switch

The losses occurring in the synchronous switch due to cross-talk can be estimated by comparing the measured energy lost to the synchronous device during the turn-on of the active device to the energy recovered from the synchronous device during the active device turn-off transient. Because the synchronous device switching transitions are ZVS, there should be no overlap losses and the speed of the turn-on and turn-off should not impact the switching energy in either case. Therefore, any loss occurring in the synchronous switch will be due to cross-talk. This loss is shown for a sweep of operating conditions in Figure 5.8. It is interesting to note that in the case of cross-talk, the load current does not have a significant effect. Since the voltage slew rate ( $dv_{ds}/dt$ ) during the hard turn-on transient is primarily a function of the gate driver speed and the dc bus voltage, these are the parameters that show the strongest relationship with cross-talk loss.

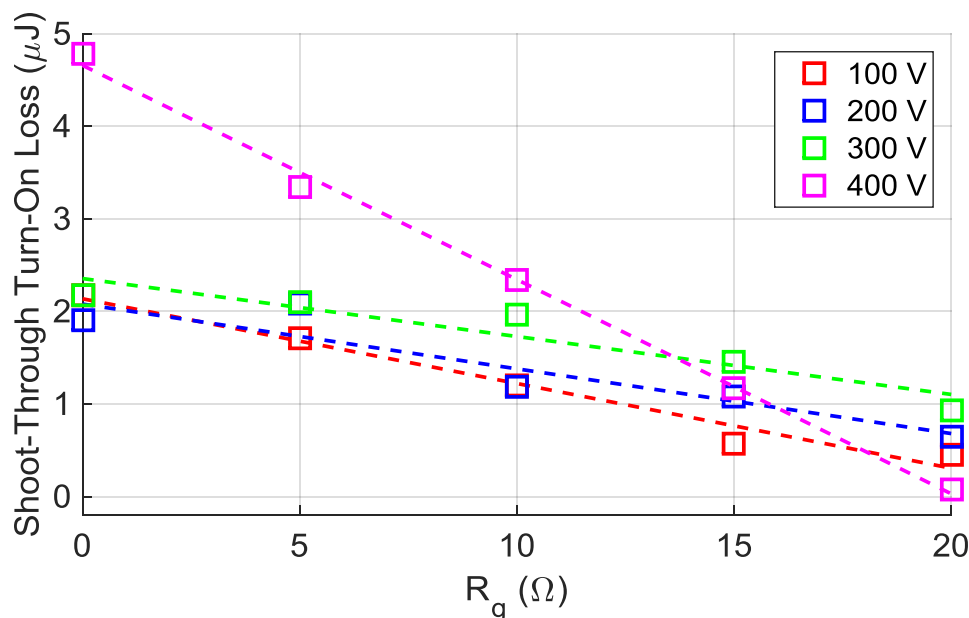


Figure 5.8. Cross-talk loss in the synchronous switch with GS66508P, as a function of  $R_g$  and  $V_{dc}$ .

Two example turn-on transients with 0  $\Omega$  and asymmetric 20  $\Omega$  drivers are compared in Figure 5.9. The asymmetric 20  $\Omega$  driver produces a much longer turn-on time and loss, but the loss is reduced by several  $\mu$ J due to reduced cross-talk.

After the turn-off  $dv_{ds}/dt$  transient is over, some additional energy is lost due to cross-talk in the 5-20 ns following the transient. The  $C_{gd}$  displacement current in the synchronous device induces a negative gate voltage for a short time after the turn-off, and the magnitude of this negative  $v_{gs}$  increases with higher gate resistance and higher load current. It is interesting to note that this negative spurious voltage occurs after the  $dv_{ds}/dt$  transient, not during the transient as is typical for cross-talk. Figure 5.10 compares the turn-off transient waveforms with 0  $\Omega$  and 20  $\Omega$ , showing a negative gate voltage of about -10 V in the 20  $\Omega$  case with 10 A load current. As explained previously, the forward voltage drop during DLB is approximately equal to the sum of the internal gate voltage and the drop across the channel resistance  $R_{sd,rev}$ . The conduction loss during the dead time following turn-off will thus increase with higher gate resistance and load current.

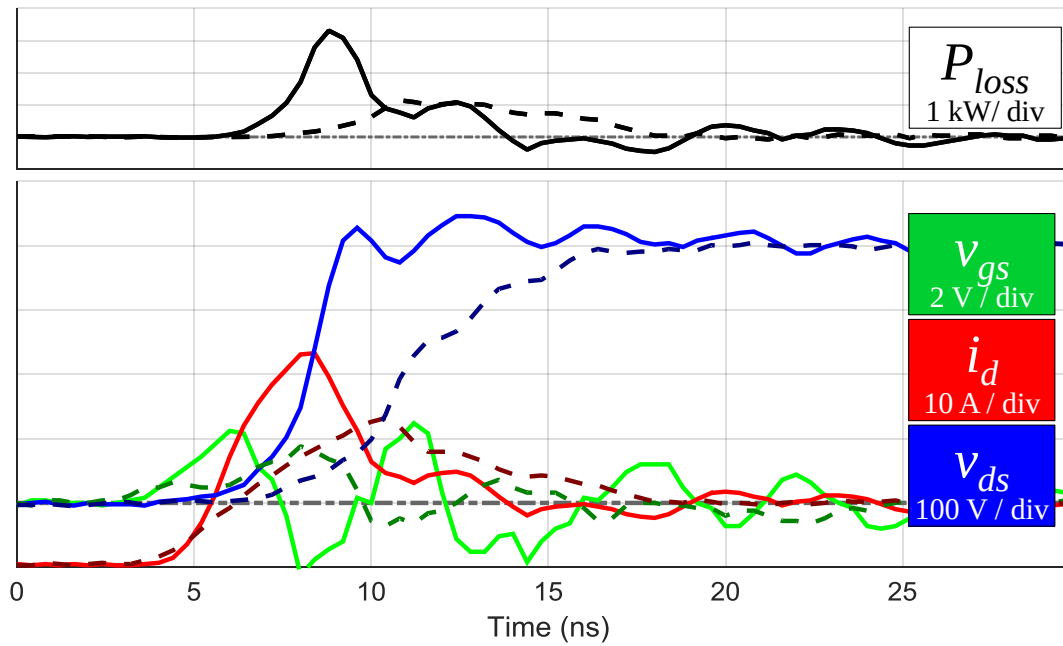


Figure 5.9. Synchronous device transient waveforms for GS66508P, during active device turn-on at 400 V and 10 A with an asymmetric gate drive circuit, showing  $R_{g,ext} = 0 \, \Omega$  with a solid line and  $R_{g,ext} = 20 \, \Omega$  with a dashed line.

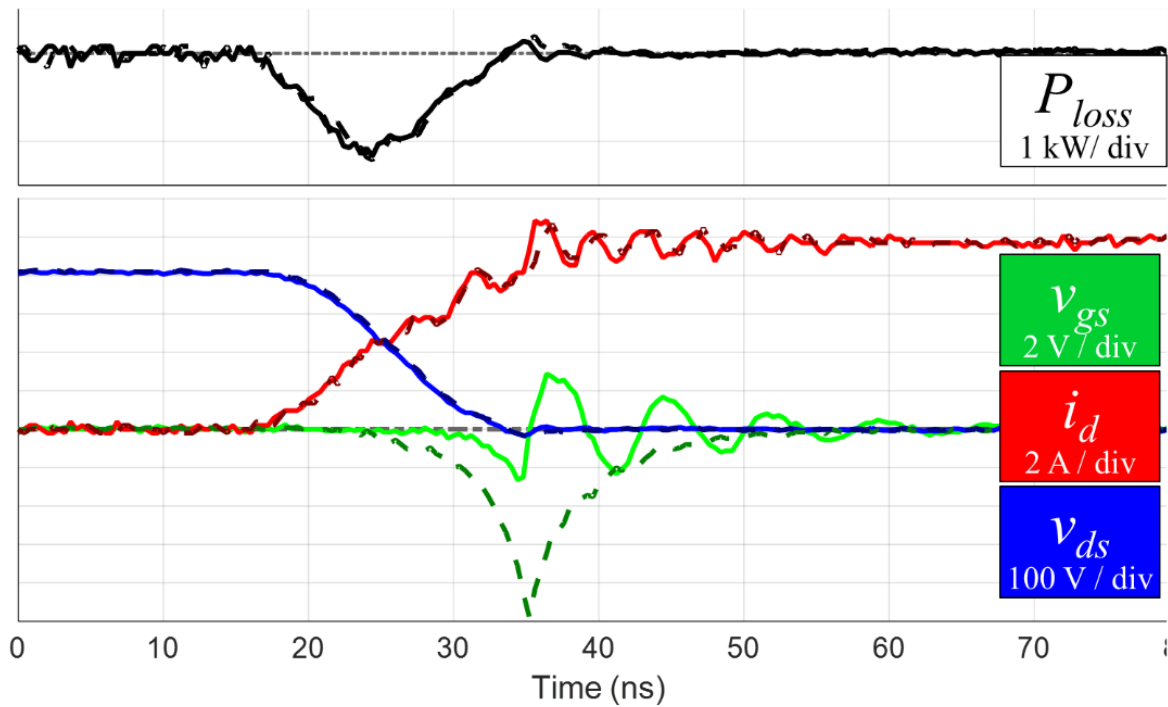


Figure 5.10. Synchronous device transient waveforms for GS66508P, during active device turn-off at 400 V and 10 A with an asymmetric gate drive circuit, showing  $R_{g,ext} = 0 \, \Omega$  with a solid line and  $R_{g,ext} = 20 \, \Omega$  with a dashed line.



Turn-off cross-talk can be mitigated with a Zener diode in the gate drive circuit, connected directly between the source sense and gate terminals to provide a low-impedance path in parallel with  $C_{gs}$  during the turn-off transient. This will also add parallel capacitance between the gate and source and slow down the turn-on transient, but it may be necessary in cases with extreme negative  $v_{gs}$  spikes that risk damage to the gate.

### 5.5 Tradeoff of asymmetric $R_g$ selection

From the results presented here, it is clear that a conventional gate drive circuit with non-zero gate resistance is not an effective option for this device, due to heavy overlap and cross-talk losses during both turn-on and turn-off transients. An asymmetric gate drive circuit presents an alternative, with lower cross-talk losses at turn-on and overlap losses at turn-off. However, the turn-on overlap loss is still increased significantly with higher gate resistance.

To choose the optimal asymmetric turn-on gate resistance, it is important to consider the tradeoff between overlap switching loss and cross-talk induced shoot-through loss. Figure 5.11 shows the total switching energy loss expected from a sweep of  $R_g$  and  $I_L$  conditions at 400 V dc bus, considering the cross-talk loss of both switches, as well as their  $C_{oss}$ -related loss and overlap loss.

An asymmetric gate drive with 20  $\Omega$  of turn-on gate resistance may reduce overall cross-talk loss by 5-10  $\mu\text{J}$  when compared to a conventional gate drive circuit with 0  $\Omega$ . However, this adds as much as 80  $\mu\text{J}$  at the full rated load. Based on these experimental results, an asymmetric gate drive circuit with 5-10  $\Omega$  may be appropriate for light load applications below 10 A with the device studied. However, this only results in approximately the same overall losses, and not a significant reduction. This design will also lower the peak  $dv_{ds}/dt$  during turn-on, which will be helpful in preventing spurious switching events due to interference in the signal path.

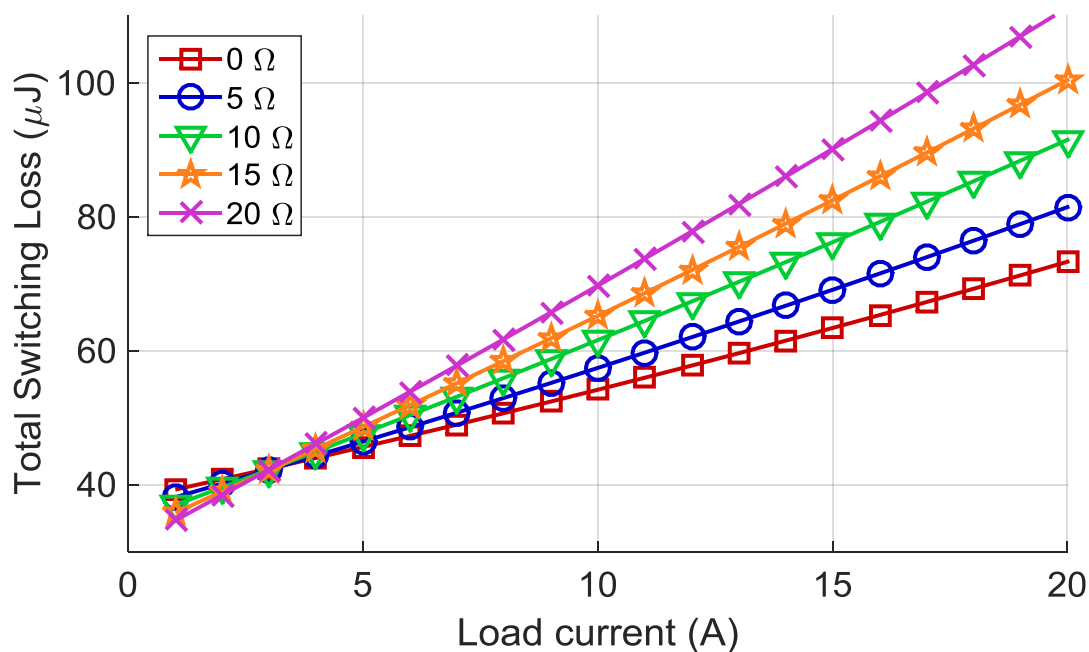


Figure 5.11. Overall switching energy loss as a function of  $R_g$  and  $I_L$ , demonstrating tradeoff between cross-talk and overlap losses.

## 5.6 Summary

The switching losses due to cross-talk for an enhancement-mode device have been studied, and a methodology has been developed that can be applied to other GaN or fast-switching devices. The experimental study included a range of gate resistances with three different driver configurations. Analysis of the results showed that the cross-talk loss increases at higher dc bus voltage, and with lower turn-on gate resistance. Conventional symmetric gate resistance driving circuits were shown to be prohibitively lossy, although a symmetric  $0\ \Omega$  gate resistance was shown to be the most effective option for higher load cases due to significant overlap loss reduction. In certain load conditions, the most efficient driving scheme may be an asymmetric gate resistance, but this tradeoff will depend on the device under test as well as the driving circuit, components, and even PCB layout being implemented. This study is therefore most effective as a methodology for performing such a characterization, as well as a road map for the trends that can be investigated in such a study.

## Chapter 6

### Modeling of Hard-Switching Transients in a GaN Phase Leg

#### 6.1 Introduction

Although the e-mode GaN HFET is similar to a MOSFET, its unique characteristics must be considered carefully in order to accurately analyze the experimental results. Therefore, a simplified model was developed to understand the turn-on and turn-off transients. Although this simplified model is not intended for simulation, the equations can be used to better understand and interpret experimental results. The model is aimed at understanding and explaining some of the trends and properties that were discovered during the characterization process, which are not explained by the conventional model of a MOSFET.

As such, equations for the internal device voltages and currents were developed for the subintervals of a turn-on and turn-off transient. These equations, however, do not consider the gate loop inductance, which will cause additional resonance during each subinterval, especially in the gate voltage waveform. It also does not fully consider the impacts of the load inductance and stray inductances in the power loop, except for the initial drop in voltage during turn-on.

The model was applied to help explain two specific features of the device. First, the consequences of the Miller effect on the turn-on and turn-off switching transients were analyzed, because the assumption of a simple Miller plateau was not observed in the experimental results. Second, a method to scale turn-on losses with elevated temperature was developed, based on room temperature  $E_{on}$  and static characterization data.

#### 6.2 Subcircuit model

The subcircuit model shown in Figure 6.1 was developed by overlaying the internal junction capacitances, parasitic capacitances, and channel resistance from Figure 3.12 on the physical device structure shown in Figure 3.5. Because the source and substrate are externally

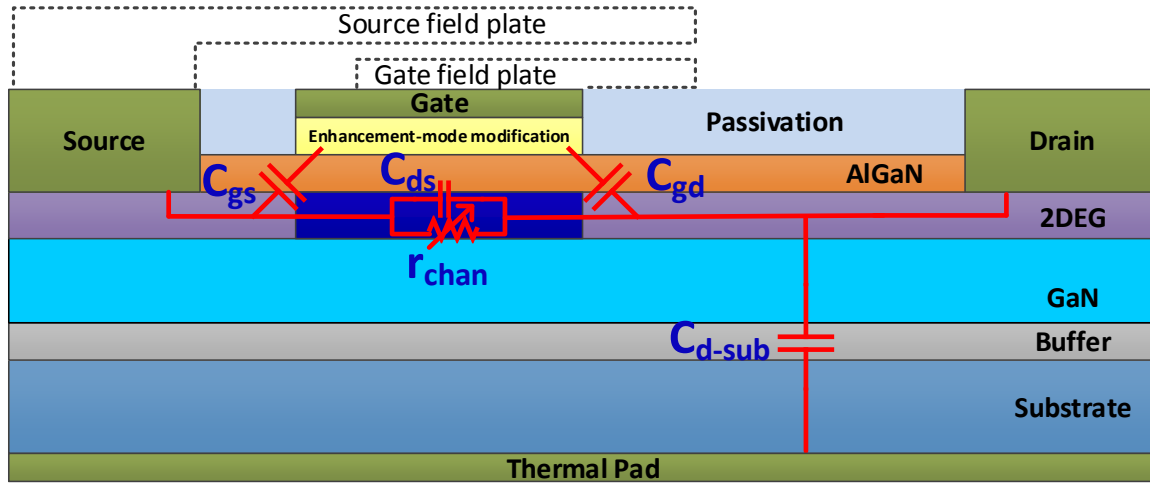


Figure 6.1. Subcircuit model for an enhancement-mode GaN HFET.

connected for the device considered here  $C_{d,sub}$  can be lumped with  $C_{ds}$ . The equivalent resistance of the channel is represented here as a variable resistor  $r_{chan}$ , although the behavior of the channel in the saturation region could be more accurately represented by a voltage-dependent current source  $i_{chan}$ . The field plate structure of the device will heavily impact the characteristics of the junction capacitances, so they are pictured in this figure as well. However, the exact structure for these field plates is unknown for the device considered here, so they will only be considered inasmuch as they impact the values for lumped capacitance  $C_{oss}$ ,  $C_{iss}$ , and  $C_{rss}$  which was measured with a precision impedance analyzer.

### 6.3 Hard turn-on transient behavior

The typical turn-on transient for a phase leg with GaN HFETs or other fast-switching devices is shown in Figure 6.2, with the current paths for each subintervals shown with arrows.

Initially, the load current flows through the synchronous device's diode-like reverse conduction mechanism (DLB) as shown in Figure 6.2 (a). This stage continues until the active device gate voltage reaches its threshold, and the active device channel begins to conduct current in the saturation region. During this turn-on delay time, the gate voltage, channel current, drain current, and drain-source voltage can be described by

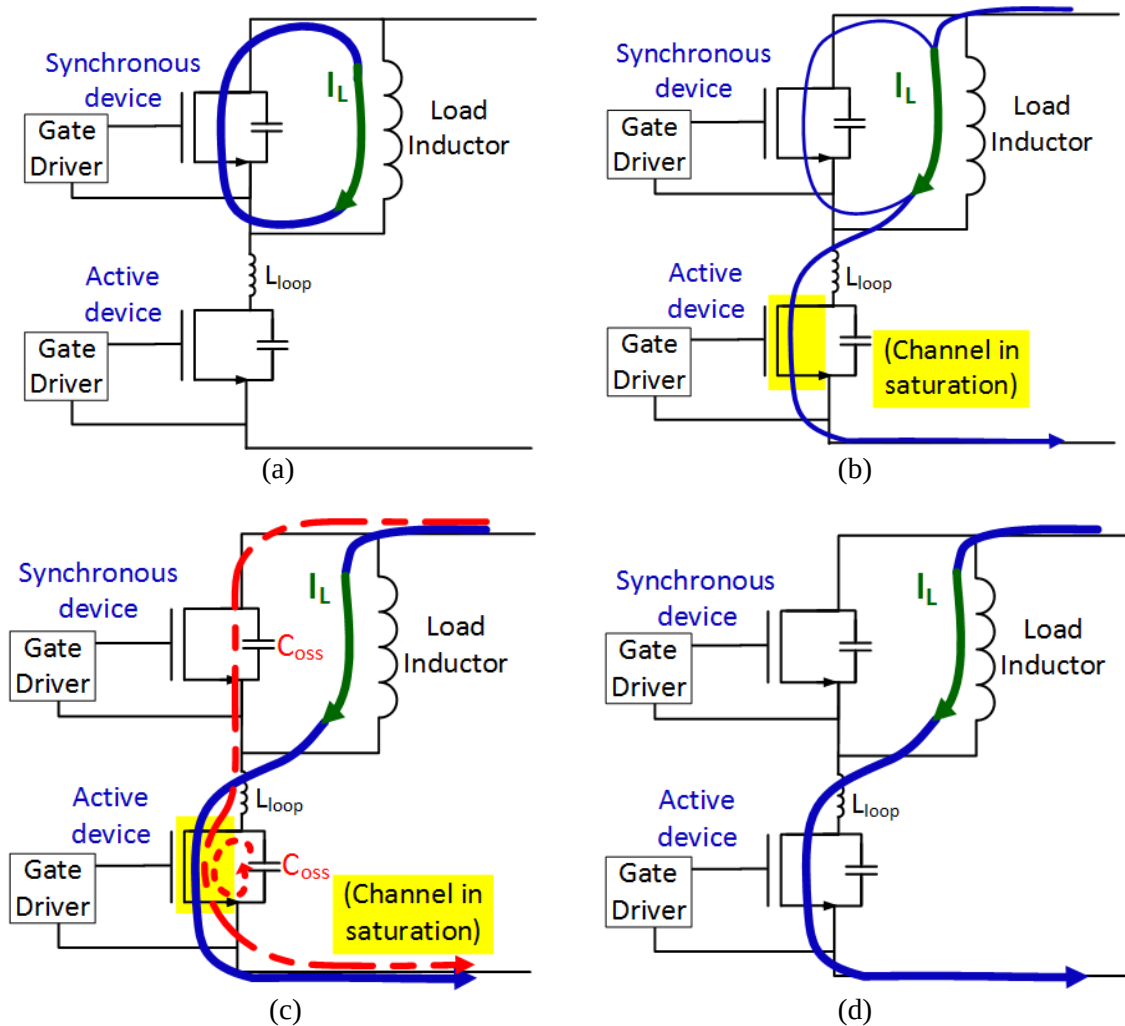


Figure 6.2. Current in a phase leg during a hard turn-on transient with fast-switching devices. (a) Before turn-on transient and during turn-on delay time; (b) During current rise time; (c) During voltage fall time; (d) After turn-on transient is complete.

$$v_{gs} = \int \left[ \frac{(V_{drv} - v_{gs})}{(R_{g,int} + R_{g,ext})C_{iss}} \right] dt \quad (6.1)$$

$$i_{chan} = 0 \text{ A} \quad (6.2)$$

$$i_d = 0 \quad (6.3)$$

$$v_{ds} = V_{dc} \quad (6.4)$$

Once the gate voltage reaches the threshold voltage, the device turns on in the saturation region, and the drain current begins to rise. At this time, the load current commutates from the synchronous device to the active device. The voltage on the synchronous device is clamped to zero, so it cannot begin to block any voltage yet. The parasitic power loop inductance  $L_{loop}$  blocks some of the dc voltage during this subinterval. With a dense board design, this drop should be relatively small compared to  $V_{dc}$ . During this current rise time, the gate voltage, channel current, drain current, and drain-source voltage can be described by

$$v_{gs} = \int \left[ \frac{(V_{drv} - v_{gs})}{(R_{g,int} + R_{g,ext})C_{iss}} + \left( \frac{C_{rss}}{C_{iss}} \right) \left( \frac{dv_{ds}}{dt} \right) \right] dt + V_{th} \quad (6.5)$$

$$i_{chan} = g_{fs}(v_{gs} - V_{th}) \quad (6.6)$$

where  $g_{fs}$  is the large-signal transconductance, a physical parameter of the device that can be measured experimentally by finding the slope of the transfer characteristic.

$$i_d = i_{chan} + C_{oss,active} \frac{dv_{ds}}{dt} \quad (6.7)$$

$$v_{ds} = V_{dc} - V_{sync,dlb} - L_{loop} \frac{di_d}{dt} \quad (6.8)$$

where  $V_{sync,dlb}$  is the forward voltage drop of the GaN FET when operating in DLB mode.

Once the current is fully commutated to the active device channel, the synchronous device turns off and can block dc voltage, so the voltage fall time begins. This point is also defined as the moment when  $v_{gs}$  reaches the Miller voltage. During the voltage fall time shown in Figure 6.2 (c),

the output capacitance in the active device is discharged into its saturated channel, and this energy is lost. Simultaneously, the output capacitance of the synchronous device is charged with current from the dc bus and decoupling capacitors, and this displacement current flows through the saturated active device channel and incurs additional loss. Here, the gate voltage, channel current, and drain current can be described by (6.5) - (6.7), but the drain-source voltage is now given by

$$v_{ds} = V_{dc} - V_{sync,dlb} - L_{loop} \frac{di_d}{dt} - \int \left( \frac{i_{chan} - I_L}{C_{oss,active} + C_{oss,sync}} \right) dt \quad (6.9)$$

where  $C_{oss,active}$  and  $C_{oss,sync}$  are the output capacitances of the two devices at the instantaneous voltage of each, because they are highly nonlinear.

The gate voltage is conventionally assumed to be constant during this subinterval, but the Miller plateau can be avoided with fast-switching devices and effective gate driver design. Further analysis on the Miller effect interactions during the voltage fall time will be discussed later in this chapter.

In a MOSFET phase leg, there will also be a reverse recovery current from the synchronous body diode during this time, but an e-mode GaN HFET has zero reverse recovery, so this can be ignored. A cascode GaN HFET will still experience some reverse recovery due to the Si device on the gate, but an antiparallel Schottky diode can eliminate reverse recovery in this case.

Another important factor in the voltage fall time is the shoot-through current across the phase leg induced by the Miller effect in the synchronous device, shown in Figure 6.3. The mechanism causing cross-talk in the synchronous device was discussed in Chapter 2 and Chapter 3, and shown in Figure 3.12. Chapter 5 also experimentally demonstrated the impact of cross-talk on turn-on loss. For analysis of the turn-on transient behavior, it is necessary to understand that the current in the active device channel due to cross-talk will be equal to the total current through the synchronous device as its channel turns partially on. Because the total active channel current is limited by the gate voltage, the shoot-through current will reduce the channel current available for

displacement of the two output capacitors as shown in Figure 6.3. Considering this new channel current component, (6.9) becomes

$$v_{ds} = V_{dc} - L_{loop} \frac{di_d}{dt} - \int \left( \frac{i_{chan} - I_L - i_{shoot-through}}{C_{oss,active} + C_{oss,sync}} \right) dt . \quad (6.10)$$

The current  $i_{shoot-through}$  can be determined by the induced gate voltage on the synchronous device, as in

$$i_{shoot-through} = g_{fs}(v_{gs,sync} - V_{th}) \quad (6.11)$$

$$v_{gs,sync} \approx V_s + (R_{g,int} + R_{g,ext,off} + R_{pd}) C_{gd,sync} \frac{dv_{ds,active}}{dt} \quad (6.12)$$

where  $V_s$  is the off-state supply voltage on the synchronous device gate drive (typically 0 V),  $R_{g,int}$  is the device's internal gate resistance,  $R_{g,ext,off}$  is the external gate resistance of the turn-off path, and  $R_{pd}$  is the pull-down on-resistance of the gate driver IC. This equation neglects the impact of the gate loop inductance, which may be significant in some cases.

Once the switch-node voltage reaches  $i_{chan}R_{ds-on}$ , the device falls into the ohmic region as

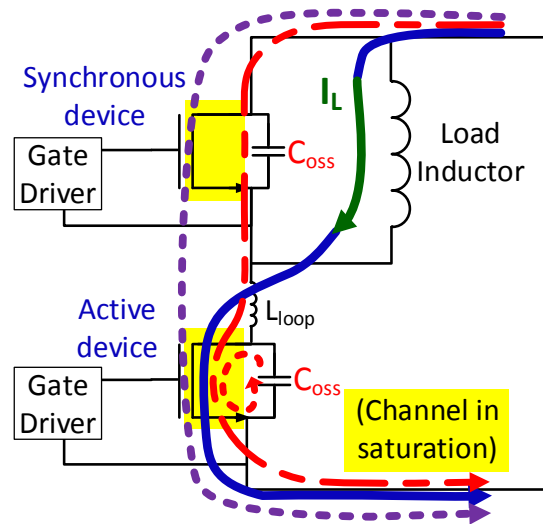


Figure 6.3. Impact of cross-talk on voltage fall time in a phase leg, showing the induced shoot-through current with a purple dashed line.



shown in Figure 6.2 (d), and the turn-on transient is essentially complete. However, there may be some ringing between the junction capacitances and parasitic loop inductances as the switch-node voltage settles to  $I_L R_{ds-on}$ . This ringing is not analyzed in depth here, because the experimental results presented earlier have shown that the net energy losses during this time are very small.

Figure 6.4 shows the theoretical turn-on waveforms divided into these subintervals. The lightly shaded area shows the charge associated with displacement current in the output capacitors of the two devices,  $q_{oss,active}$  and  $q_{oss,sync}$ , which contribute a fixed amount of turn-on energy loss for a given dc voltage, regardless of load current or temperature. These losses are given by

$$E_{on,Coss,sync} = \int_0^{V_{dc}} [C_{oss,sync}(v) + C_{stray,sync}] \times (V_{dc} - v) dv \quad (6.13)$$

$$E_{on,Coss,active} = \int_0^{V_{dc}} [C_{oss,active}(v) + C_{stray,active}] \times v dv . \quad (6.14)$$

The area with hatched shading in Figure 6.4 shows the charge associated with conduction of the load current through the saturated channel during the turn-on transient, which contributes energy loss that is dependent on the time duration of the transient. This loss is considered overlap loss, and can be improved with faster gate drive design. Some simplified equations for this overlap loss will be discussed later in this chapter.

Although the consequences of charging the synchronous device output capacitor are considered here, the actual energy deposited into  $C_{oss,sync}$  is not. The losses described by (6.13) and (6.14) both occur in the resistive channel of the active device. The energy stored in the synchronous device as it begins to block voltage should be recovered during the following turn-off transient, so it is not typically considered a component of phase leg switching losses. The turn-on energy loss  $E_{on}$  is conventionally defined as the sum of the overlap losses and (6.13), because the energy loss of (6.14) can only be seen experimentally during the turn-off transient.

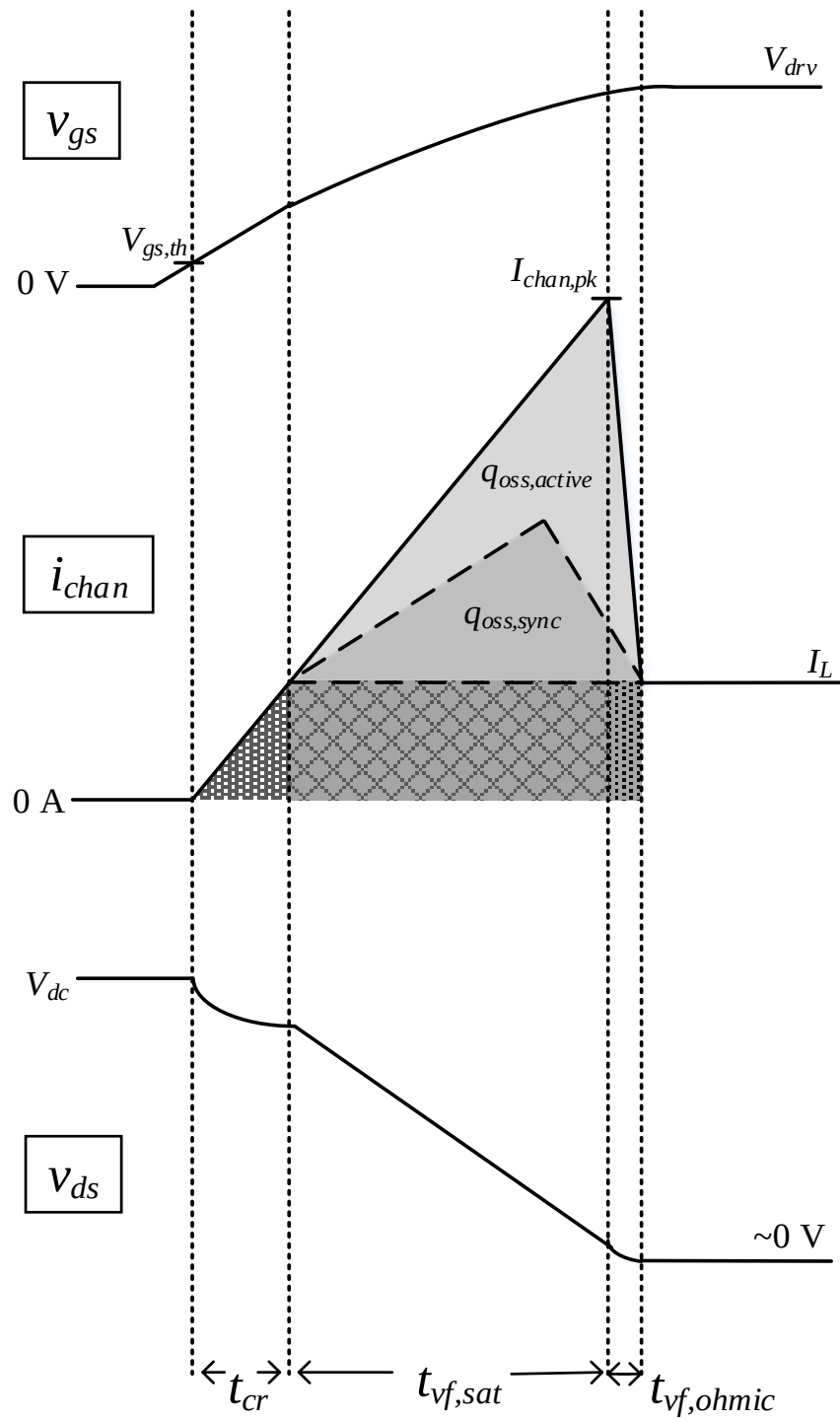


Figure 6.4. Theoretical turn-on transient waveforms of active device.

It is important to note that during this transient, the term  $V_{drv}$  represents the voltage at the output of the gate driver, which is not a constant. In a fast-switching device, the rise time of the driver may be longer than the turn-on delay time and affect the gate voltage during multiple subintervals. Also, the on-resistance of the pull-up resistor continues to limit the gate driver current even after the rise time is complete. A simplified driver voltage model is used here, which assumes a constant ramp rate during the pull-up rise time, then beyond that time, the driver voltage will be

$$V_{drv} = V_p - i_g R_{pu} \quad (6.15)$$

where  $V_p$  is the positive supply voltage on the driver and  $R_{pu}$  is the on-resistance of the pull-up transistor, generally given in the driver datasheet.

A final consideration for the turn-on transient is the voltage overshoot that occurs on the synchronous switch at the end of the transient, when the active switch  $v_{ds}$  approaches 0 V and its drain current  $i_d$  falls back down to  $I_L$ . This overshoot is approximately equal to  $L_{loop} di_d/dt$ , and  $di_d/dt$  can be estimated by solving and differentiating (6.7) and (6.9) as in

$$\frac{di_d}{dt} \approx \left( \frac{C_{oss, sync}}{C_{oss, active} + C_{oss, sync}} \right) \frac{di_{chan}}{dt} + (i_{chan} - I_L) \frac{d\left( \frac{C_{oss, sync}}{C_{oss, active} + C_{oss, sync}} \right)}{dt} . \quad (6.16)$$

However, it is difficult to intuitively interpret the derivative of capacitance with respect to time.

Therefore, it is helpful to define a parameter for this capacitance ratio

$$x_C = \frac{C_{oss, sync}}{C_{oss, active} + C_{oss, sync}} \quad (6.17)$$

and its derivative with respect to drain voltage rather than time. This ratio and its derivative can then be treated as a characteristic of the device itself, irrespective of switching speed, although still related to the operating dc bus voltage. The drain can be approximated as (6.18) throughout the voltage fall time by substituting this ratio into (6.16), and incorporating (6.31), which will be derived later in this chapter.

$$i_d \approx I_L + x_C i_{chan} \quad (6.18)$$

Now, (6.17) can then be re-written as

$$\frac{di_d}{dt} \approx x_C \left( \frac{di_{chan}}{dt} - \left( \frac{(i_{chan} - I_L)^2}{C_{oss, sync}} \right) \frac{dx_C}{dv_{ds}} \right). \quad (6.19)$$

From (6.19), it can be seen that  $di_d/dt$  is most affected by the magnitude and slope of the channel current, and the significance of the output capacitive curve's nonlinearity with respect to voltage. At the end of the turn-on transient, the channel current falls rapidly as it exits the saturation region and becomes ohmic, so it is difficult to model  $i_{chan}$  or  $di_{chan}/dt$  at this time. However, this equation is still helpful in understanding factors that impact the voltage overshoot on the synchronous switch at the end of the turn-on transient. This relationship will be investigated and verified experimentally in Chapter 8.

#### 6.4 Hard turn-off transient behavior

The hard turn-off transient is distinct from turn-on because of the direction of the load current when the transient occurs. As a result, the channel can be turned off completely before the end of the turn-off transient, whereas in turn-on, the channel must remain in the saturation region for the duration of the transient. The load current displaces charge between the active and synchronous device output capacitors. Because of the directions of the load current and displacement currents, the conductive channel in parallel with the output capacitors actually slows down the turn-off transient, thereby causing turn-off overlap loss until the gate voltage turns off the channel completely. This means that a fast gate driver can nearly eliminate all overlap losses during the turn-off transient and avoid any Miller plateau from occurring by dropping below  $V_{th}$  before  $dv_{ds}/dt$  is significant.

Figure 6.5 shows the subintervals involved in the turn-off transient of a phase leg. In Figure 6.5 (a), the load current continues to flow through the active device channel, as the gate voltage drops from the driving voltage to the Miller voltage. Here, the gate voltage is

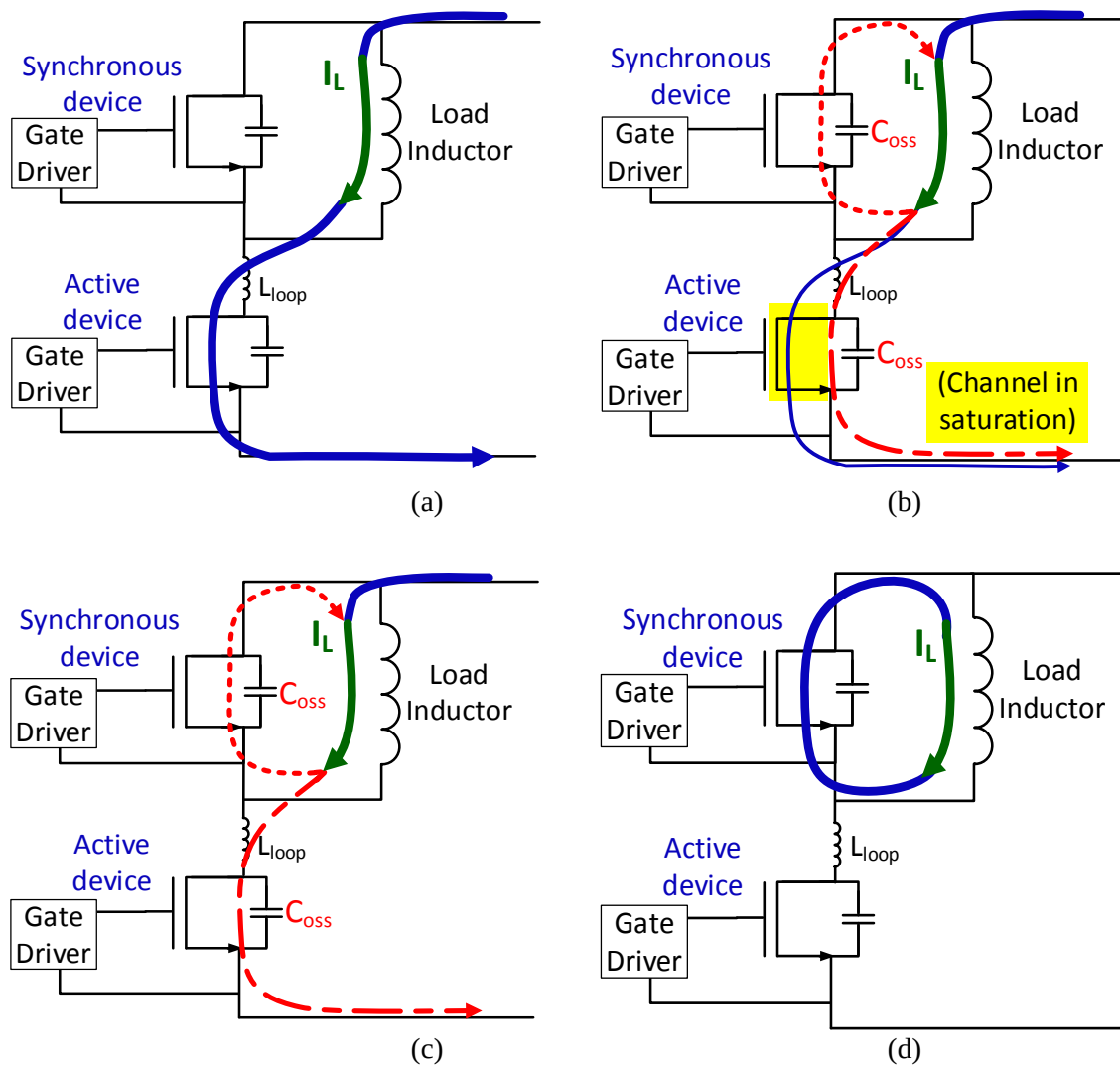


Figure 6.5. Current in a phase leg during a hard turn-off transient with fast-switching devices. (a) Before turn-off transient and during turn-off delay time; (b) During current fall and voltage rise time, while channel is turning off; (c) During current fall and voltage rise time, after channel is fully off; (d) After turn-off transient is complete.

$$v_{gs} = V_p - \int \left[ \frac{(v_{gs} - V_{drv})}{(R_{g,int} + R_{g,ext})C_{iss}} \right] dt \quad (6.20)$$

and this turn-off delay time continues until  $v_{gs}$  reaches the Miller voltage, when the device enters the saturation region. This Miller voltage is given by

$$V_{Miller} = \frac{I_L}{g_{fs}} + V_{th} . \quad (6.21)$$

Once the gate voltage reaches the Miller voltage, the device channel becomes more resistive than  $R_{ds-on}$ , and the load current begins to commute to the two parallel output capacitors of the active and synchronous devices. Figure 6.5 (b) shows this subinterval. Because neither capacitor is clamped by a diode or Ohmic channel, this allows both the voltage rise time and current fall time to occur simultaneously. During this time, the gate voltage can be described by

$$v_{gs} = V_p - \int \left[ \frac{(v_{gs} - V_{drv})}{(R_{g,int} + R_{g,ext})C_{iss}} + \left( \frac{C_{rss}}{C_{iss}} \right) \left( \frac{dv_{ds}}{dt} \right) \right] dt \quad (6.22)$$

and the currents can be described by (6.6) and (6.7). Based on the channel current, the drain-source voltage can then be described by

$$v_{ds} = \int \left( \frac{I_L - i_{chan}}{C_{oss,active} + C_{oss,sync}} \right) dt - L_{loop} \frac{di_d}{dt} \quad (6.23)$$

During this time, the portion of the load current that flows through the saturated channel causes resistive energy loss. However, the energy deposited into the active device output capacitor is not truly lost here. It is conventionally considered part of  $E_{off}$ , but this energy is not resistively lost until the next turn-on transient, and is given by (6.14).

With a slow gate driver or heavy load, the entire voltage rise time may be described by this subinterval. However, because of the low input capacitance of GaN HFETs, the saturated channel will actually turn off much earlier than the displacement of output capacitor charge. Once  $v_{gs}$  falls below the threshold voltage, the transient continues as shown in Figure 6.5 (c). The same equations

(6.7), (6.22), and (6.23) describe this second part of the voltage rise and current fall time, but the channel current is now 0 A, so  $dv_{ds}/dt$  increases as the full load current acts to displace output capacitor charges. Because no further resistive losses can occur, only lossless displacement occurs here, including the energy stored in  $C_{oss,active}$ , as well as the recovery of the energy stored in  $C_{oss,sync}$ .

After the charge displacement is complete, the voltage rise time and current fall time are over, and the full load current flows into the synchronous device, either in a body diode or in the GaN's DLB mode.

It is important to consider the nonlinear output capacitance when analyzing the turn-off transient. At the beginning of the transient, the total switch-node capacitance is relatively high, since the synchronous device has a low drain-source voltage. Therefore, the  $dv_{ds}/dt$  is initially quite low. The voltage drop across the resistive channel can potentially remain very low, as long as it turns off before  $v_{ds}$  increases enough for the switch-node capacitance to fall. If this condition is met, the turn-off overlap loss can be nearly zero.

As with conventional MOSFETs, the turn-off typically ends with a voltage overshoot on the active switch, but there is an interesting distinction for the GaN HFET. As opposed to a true body diode, the GaN DLB can support a momentary reverse voltage, if a negative voltage spike occurs on the synchronous device  $v_{gs}$ . This cross-talk mechanism was explained in Chapter 5 in greater detail. Unless the gate driver is designed to prevent turn-off cross-talk, the  $v_{ds}$  overshoot experienced by the active device will be

$$v_{ds,overshoot} = -\left(v_{ds,sync} + L_{loop} \frac{di_d}{dt}\right). \quad (6.24)$$

The magnitude of the  $di_d/dt$  at this moment can also be approximated as it was with the turn-on transient earlier, using the relationship given by (6.18) and (6.19). However, in most load conditions with a reasonably fast gate drive, the channel current will most likely fall to zero before the end of the turn-off transient. Therefore, (6.19) can be further reduced to

$$\frac{di_d}{dt} \approx \left( \frac{-I_L^2}{C_{oss,active} + C_{oss,sync}} \right) \frac{dx_C}{dv_{ds}}. \quad (6.25)$$

Here, the magnitude of the overshoot voltage has a second-order relationship with load current, and is also strongly related to the total switch-node capacitance curve as well as the nonlinearity of the  $C_{oss}$  curve near 0 V. Along with the turn-on overshoot, this relationship will be investigated and verified experimentally in Chapter 8.

### 6.5 *Analysis of the Miller effect and its impact on the voltage rise and fall transients of a GaN FET*

The Miller effect is a well-known phenomenon in three-terminal power devices, including the cross-talk discussed previously, as well as the Miller plateau in turn-on and turn-off transients. The term “Miller plateau” describes the seemingly flat point in the gate voltage waveform during the  $dv_{ds}/dt$  of either turn-on or turn-off transients. The cause for this effect is  $C_{gd}$ , the Miller capacitance shared by the gate loop and power loop, which causes a negative feedback on the changing gate voltage. It was mentioned earlier in this chapter that the turn-off Miller plateau can be avoided during turn-off with a fast gate drive. The turn-on Miller effect cannot accurately be described as a plateau for fast-switching devices. The effect of  $C_{gd}$  on  $dv_{gs}dt$  is important to consider for fast-switching devices such as GaN, but it should be treated as a finite change in slope rather than a plateau. The goal of this section is to derive a general model that describes the gate voltage in enhancement-mode (e-mode) GaN FETs, and consequently the switching speed  $dv_{ds}/dt$ . To verify these equations, experimental double pulse test (DPT) waveforms for the turn-on and turn-off of an e-mode GaN FET were compared with waveforms calculated using the proposed model. In particular, the shape of  $v_{ds}$  during the  $dv_{ds}/dt$  transient was examined. As a second verification, the peak  $dv_{ds}/dt$  of a GaN FET was calculated under a variety of operating conditions, and then compared with experimental results.



### 6.5.1 Derivation of transient model considering the Miller Effect

Figure 6.6 (a) shows a detailed equivalent circuit for a phase leg with e-mode GaN FETs. The device under test (DUT) for experimental comparison is the GS66508P from GaN Systems, which is a four terminal device with a Source Sense pin to decouple the gate and power loops. In this circuit, parasitic resistances, inductances, and capacitances of both switches, their gate drivers, and the remainder of the PCB are considered. The bottom device is considered as the active switch in this circuit, and the top device as the synchronous switch, although these can easily be reversed if the load current source is connected differently.

Figure 6.6 (b) shows a simplified equivalent circuit during turn-on or turn-off, replacing the switch with a current source and neglecting parasitic inductances. The power loop and gate loop inductances were ignored for this analysis, although in reality they do affect the  $dv_{ds}/dt$  transient behavior. The consequences of this simplification will be discussed later in this chapter.

Analysis of the gate node produces (6.26), which can be then rearranged into (6.27) using the lumped capacitances typically found in device datasheets (output capacitance  $C_{oss}$ , input capacitance  $C_{iss}$ , and reverse transfer capacitance  $C_{rss}$ ).

$$\frac{V_{drv} - v_{gs}}{R_g} = C_{gs} \frac{dv_{gs}}{dt} + C_{gd} \frac{d(v_{gs} - v_{ds})}{dt} \quad (6.26)$$

$$\frac{dv_{ds}}{dt} = \left( \frac{C_{iss}}{C_{rss}} \right) \frac{dv_{gs}}{dt} - \left( \frac{V_{drv} - v_{gs}}{R_g C_{rss}} \right) \quad (6.27)$$

If the gate voltage is assumed to plateau at the Miller voltage, (6.28) is equivalent to (2.4), the conventional Miller Plateau model. However, analysis can be performed at the drain node to develop the model further:

$$i_{chan} - I_L = C_{gd} \frac{d(v_{gs} - v_{ds})}{dt} - (C_{ds} + C_{sync}) \frac{dv_{ds}}{dt} \quad (6.28)$$

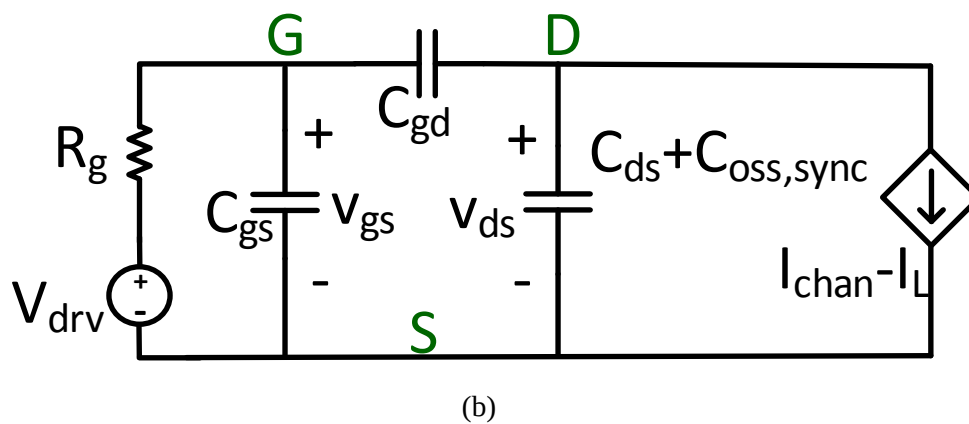
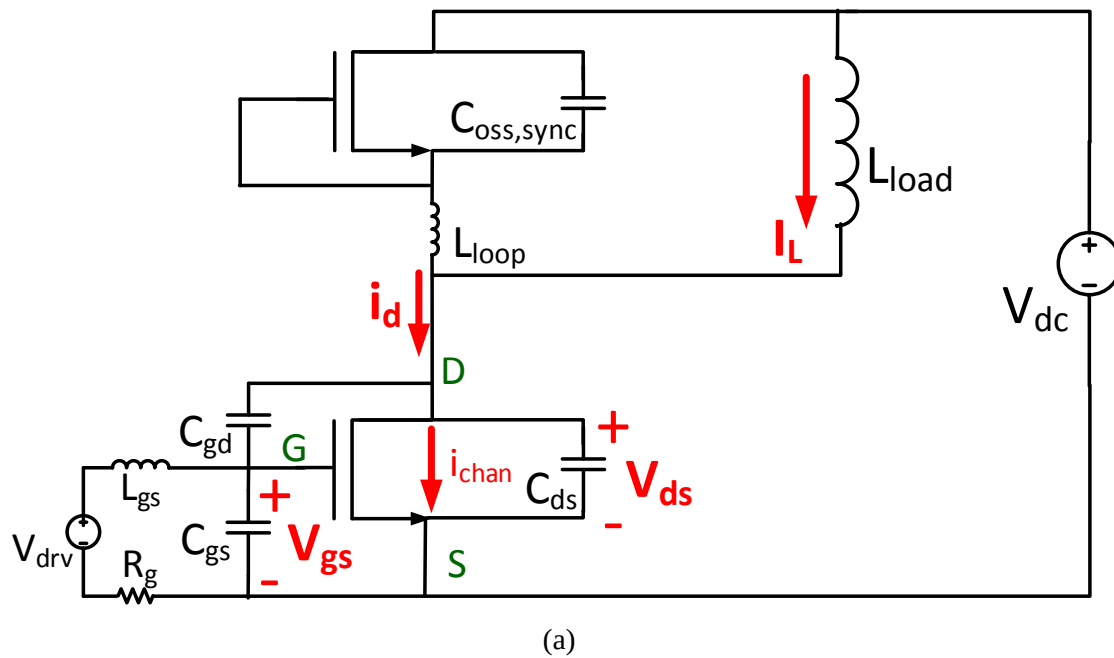


Figure 6.6. Equivalent circuit of active device during turn-on voltage fall time, (a) Detailed model including reverse recovery, (b) Simplified model with no reverse recovery.

Using the conventional model for saturated channel current, (6.28) can be further clarified by substituting

$$i_{chan} - I_L = g_{fs}(v_{gs} - V_{Miller}) \quad (6.29)$$

where  $V_{Miller}$  is the Miller voltage of the switch at a given operating condition, given by (6.21).

Combining (6.28) and (6.29) and lumping the capacitances produces

$$g_{fs}(v_{gs} - V_{Miller}) = -(C_{oss,active} + C_{oss,sync}) \frac{dv_{ds}}{dt} + C_{rss} \frac{dv_{gs}}{dt} . \quad (6.30)$$

Because the change in  $v_{gs}$  is very small compared to the change in  $v_{ds}$  during the  $dv_{ds}/dt$  interval, and the capacitance  $C_{oss,active} + C_{oss,sync}$  is also much greater than  $C_{rss}$ , the  $dv_{gs}/dt$  term can be neglected, and (6.30) can be simplified to

$$\frac{dv_{ds}}{dt} = \frac{-g_{fs}(v_{gs} - V_{Miller})}{C_{oss,active} + C_{oss,sync}} . \quad (6.31)$$

The junction capacitances of a GaN FET are nonlinear and unique to the device, so this analysis will avoid forcing an exponential curve on the nonlinear  $C_{oss}$  characteristic, and rather treat these as variables that can be determined from the datasheet or a curve tracer at any given  $v_{ds}$ . Even if these are both the same type of device,  $C_{oss,active}$  and  $C_{oss,sync}$  must be determined separately at any instant during the switching transient, as each will vary with respect to its voltage bias.

At this point, the model given by (2.5) diverges from the proposed model. In order to remove the  $v_{gs}$  term from the  $dv_{ds}/dt$  equation, [67] neglects both  $C_{gs}$  and  $C_{oss,sync}$ . But rather than eliminating the  $v_{gs}$  term, the equation can be rearranged to establish a differential equation for gate voltage, by combining (6.31) and (6.27) to reach

$$\frac{dv_{gs}}{dt} = \left( \frac{V_{drv} - v_{gs}}{R_g C_{iss}} \right) - \left( \frac{C_{rss}}{C_{oss,active} + C_{oss,sync}} \right) \left( \frac{g_{fs}}{C_{iss}} \right) (v_{gs} - V_{Miller}) . \quad (6.32)$$

This equation demonstrates the clamping behavior of the Miller effect on gate voltage. The first term on the right side represents the current supplied by the gate driver, and the second term accounts for the current demanded by  $C_{gd}$  due to the change in output voltage. The Miller effect

works in opposite polarity to the driver current during either the turn-on or turn-off transient, and the overall consequence is that the gate voltage is held close to the Miller voltage until the transient is complete. However, the gate voltage must rise above the Miller voltage during turn-on, and below it during turn-off, in order for any charge to be displaced in  $C_{oss}$ . The extent of the deviation from  $V_{Miller}$  depends on the relative magnitudes of these two terms. Although solving (6.30) analytically for  $v_{gs}$  is possible, the nonlinear capacitances make it more useful to perform discrete-time integration with a software platform such as MATLAB.

The gate voltage can be effectively modeled by (6.32) for both turn-on and turn-off, but (6.31) holds true for turn-on only. In the turn-off transient, the gate voltage may drop below the threshold voltage, which means that no channel current flows at all. Therefore, (6.31) can be modified for turn-off as the piecewise equation

$$\frac{dv_{ds}}{dt} \approx \begin{cases} \frac{I_L}{C_{oss}+C_{sync}}, & v_{gs} < V_{th} \\ \frac{g_{fs}(V_{Miller}-v_{gs})}{C_{oss}+C_{sync}}, & v_{gs} > V_{th} \end{cases}. \quad (6.33)$$

Most of the parameters in these equations can be determined from device or driver datasheets. The driving voltage  $V_{drv}$  can be modeled as an ideal voltage source with a linear rise or fall time specified by the gate driver datasheet, and the pull-up and pull-down resistances of the driver are included in the lumped gate resistance  $R_g$  for turn-on and turn-off, respectively. The large signal transconductance  $g_{fs}$  can be found from the device's transfer characteristic, as the average slope  $\Delta I_d/\Delta V_{gs}$  over the desired current range. Similarly, the Miller voltage  $V_{Miller}$  can be interpolated from the transfer characteristic at the operating current and temperature.

The Miller effect is only considered in this model during the voltage rise time and fall time. During the turn-on current rise time, while the channel current is rising to  $I_L$ ,  $v_{ds}$  is affected by the voltage drop across the parasitic loop inductances more than the Miller effect, as given by (6.8).

The loop inductance can be extracted from the board layout using a software tool, or estimated based on experimental results. In reality, both the loop inductance and the Miller effect take part in the current rise time and voltage rise/fall times, but here (6.8) is used only to determine  $v_{ds}$  at the start of the voltage fall time.

### 6.5.2 Verification with experimental results and simulation

Figure 6.7 and Figure 6.8 show the turn-on and turn-off waveforms produced from discrete-time calculation with the proposed model, as well as experimental results for GaN Systems GS66508P previously published in [204],[239]. Figure 6.7 shows the results with 20  $\Omega$  external gate resistance, and Figure 6.8 shows the faster switching case when 0  $\Omega$  external gate resistance is used. The  $v_{ds}$  and  $v_{gs}$  waveforms match well with experimental results, particularly the slope of the  $v_{ds}$  waveform and the shape of  $v_{gs}$  during the  $dv_{ds}/dt$  interval.

In both turn-on waveforms, the gate voltage continues to rise even after the  $dv_{ds}/dt$  transient begins, then dives sharply at the point when the Miller effect becomes stronger than the current supplied by the gate driver. In the turn-off waveforms, the gate voltage nearly plateaus during the transient, but continues decreasing steadily. In fact, with higher load current, the gate voltage may reverse direction and start to increase during the turn-off transient. For accurate consideration of gate current, it is important to note that in GaN FETs,  $C_{gs}$  is strongly nonlinear with respect to  $v_{gs}$  [245]. However, this data is not readily available in many device datasheets and must be measured experimentally. Alternatively, it can be extracted from the gate charge characteristic curve available on most device datasheets, as the slope of  $Q_g$  with respect to  $V_{gs}$ .

Figure 6.9 shows the  $v_{ds}$  waveforms calculated from (2.4), (2.5), and the proposed model, along with the experimental results. All three models become somewhat less accurate with lower gate resistance when switching speed increases, but the proposed model remains very close to the experimental results, while (2.4) and (2.5) predict a much shorter rise and fall time.

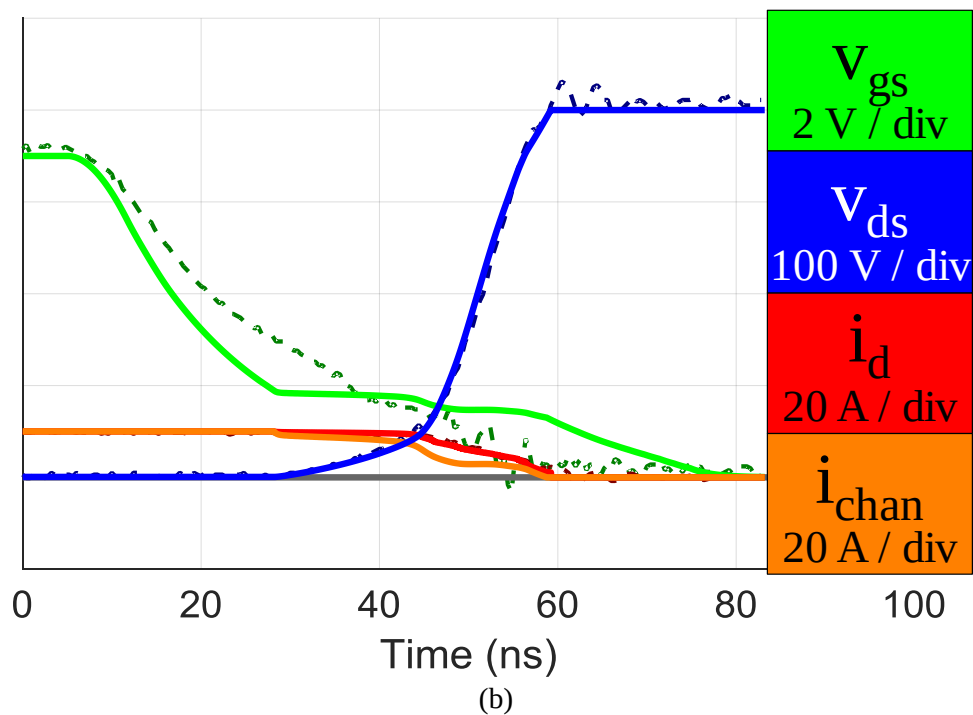
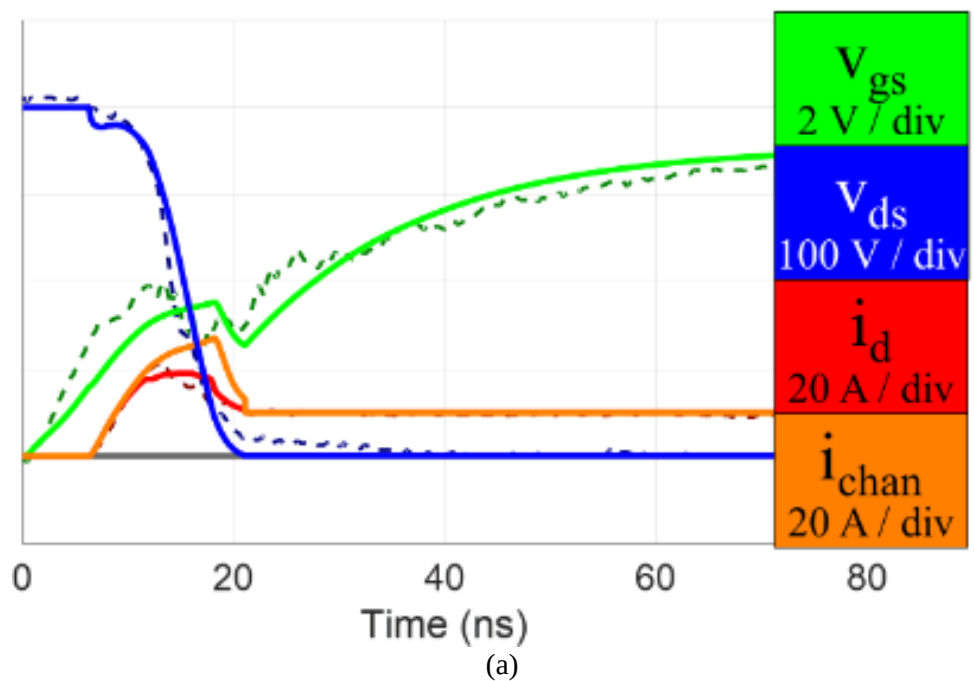


Figure 6.7. Turn-on (a) and turn-off (b) waveforms for GaN Systems GS66508P driven with Si8233 at 7 V and 20  $\Omega$ , with 400 V dc bus and 10 A inductive load current. Solid lines show discrete-time calculated waveforms using the proposed model, and dashed lines show experimental results from a double pulse test.

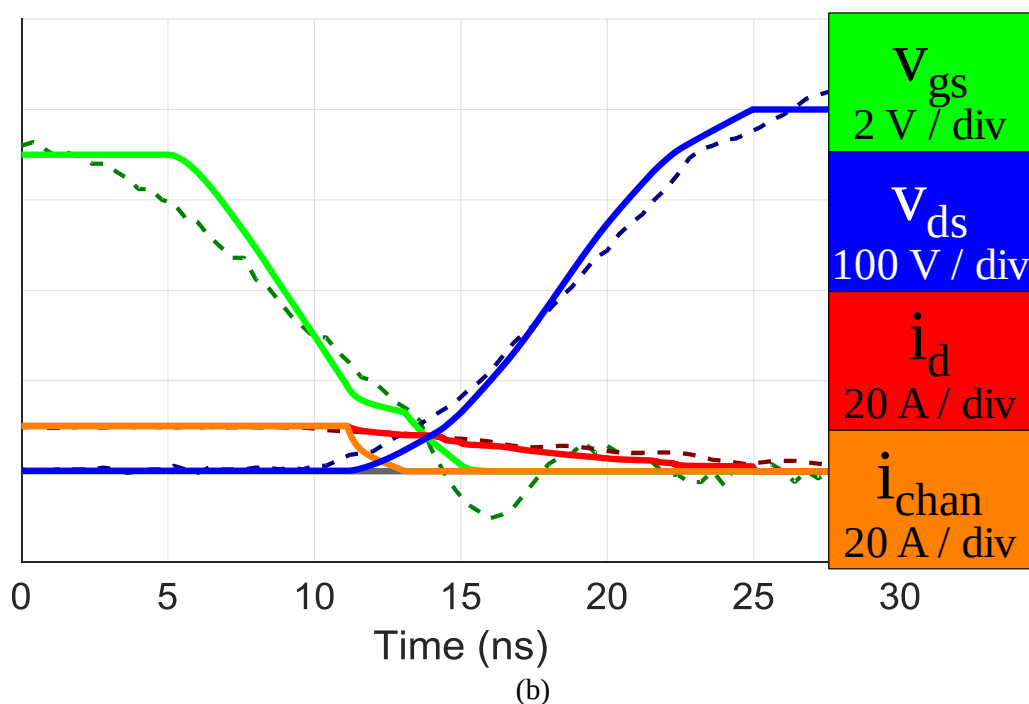
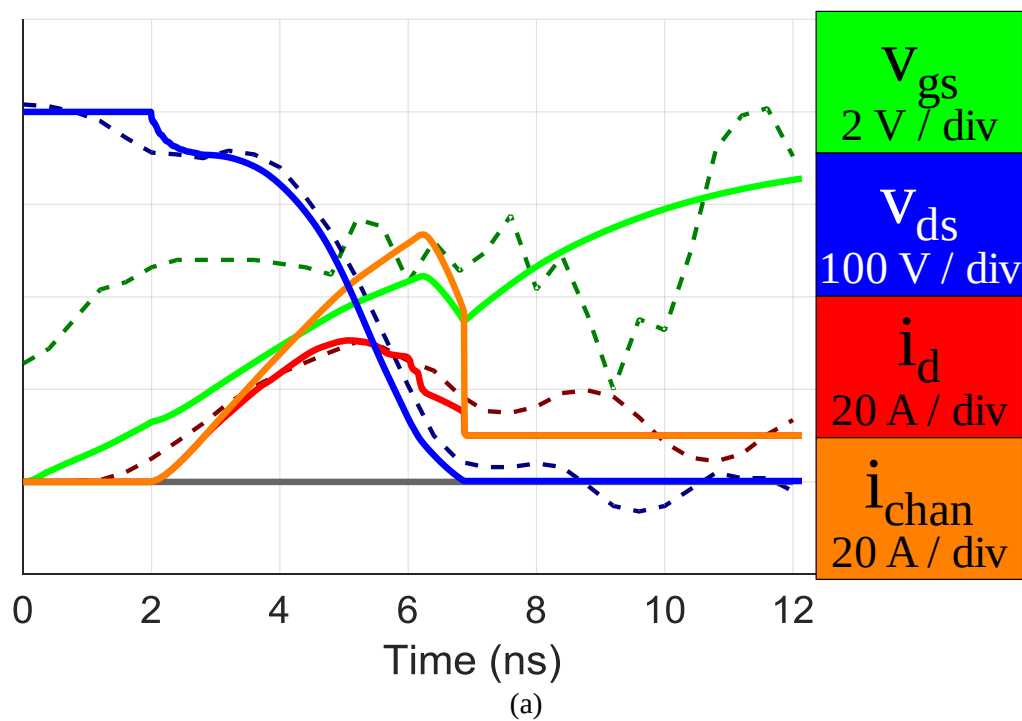


Figure 6.8. Turn-on (a) and turn-off (b) waveforms for GaN Systems GS66508P driven with Si8233 at 7 V and 0  $\Omega$ , with 400 V dc bus and 10 A inductive load current. Solid lines show discrete-time calculated waveforms using the proposed model, and dashed lines show experimental results from a double pulse test.

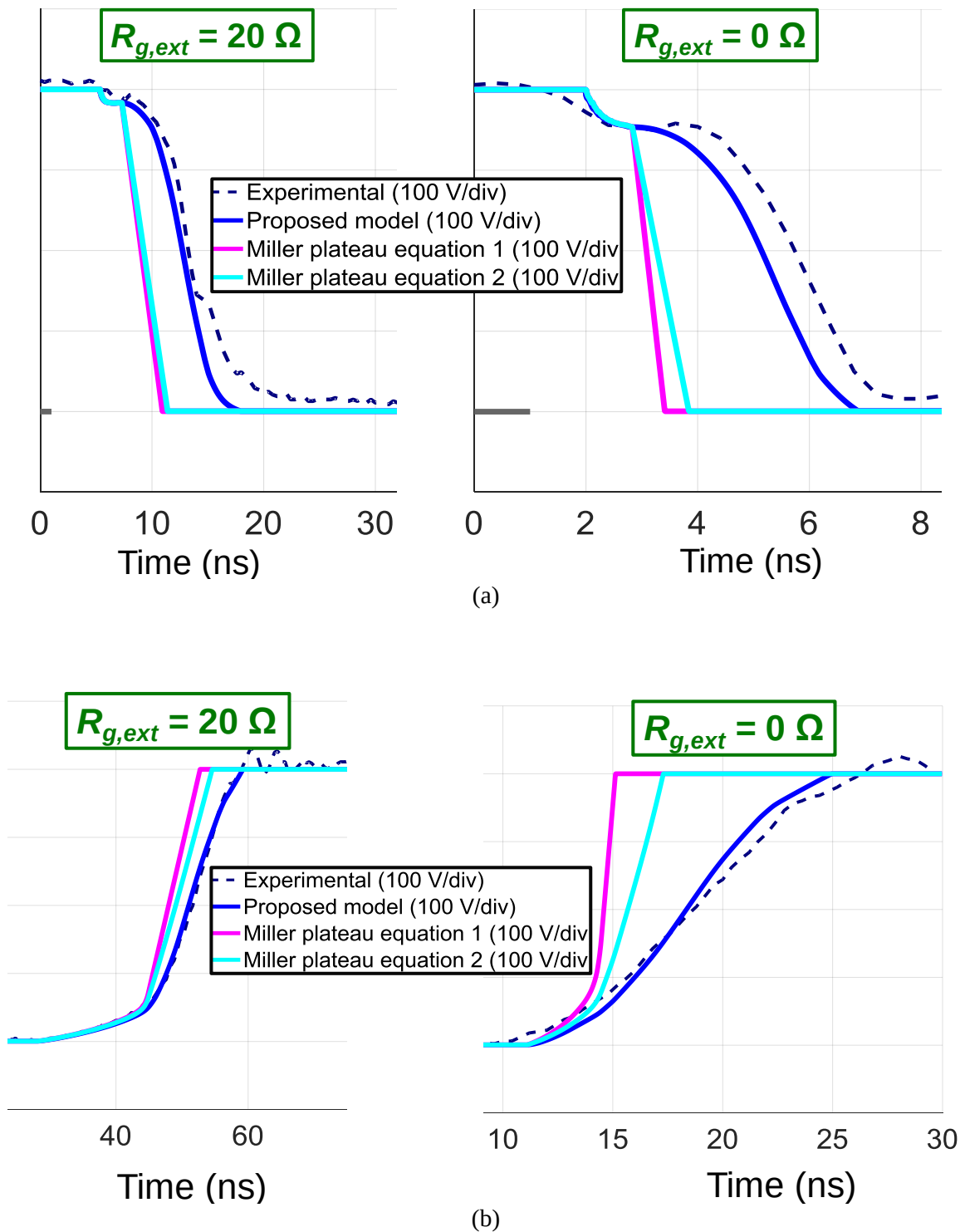


Figure 6.9. Turn-on (a) and turn-off (b)  $v_{ds}$  waveforms for GaN Systems GS66508P driven with Si8233 at 7 V, with 400 V dc bus and 10 A inductive load current



The neglected inductances cause a horizontal skew in the  $v_{gs}$  and  $v_{ds}$  waveforms, which reverse polarity when  $di_d/dt$  changes direction in the turn-on waveform. The skew between  $i_d$  and  $v_{ds}$  prevents accurate loss prediction with this model, and this error becomes even more significant as switching speed increases. For this reason, this model focuses on the slopes and overall shapes of these waveforms rather than switching loss.

### 6.5.3 Prediction of peak $dv_{ds}/dt$

The proposed model can also be applied to predict the peak  $dv_{ds}/dt$  during turn-on and turn-off. As further verification of the model's accuracy, these predictions are compared with experimental results and calculations using (2.4) and (2.5). The highest  $dv_{ds}/dt$  should occur at the highest  $v_{gs}$  during turn-on, when the channel conducts the most current, and at the lowest  $v_{gs}$  during turn-off, when the channel conducts the least current.

Determining the peak value of (6.31) in turn-on requires first finding the highest value of  $v_{gs}$ . This is accomplished by setting  $dv_{gs}/dt$  to 0 in (6.32) and calculating the peak  $v_{gs}$ .

$$V_{gs,pk} = \frac{\left(\frac{C_{oss} + C_{sync}}{R_g C_{rss}}\right) V_{drv} + g_{fs} V_{Miller}}{\left(\frac{C_{oss} + C_{sync}}{R_g C_{rss}}\right) + g_{fs}} \quad (6.34)$$

Now, (6.34) can be substituted into (6.31) to find the peak  $dv_{ds}/dt$  in turn-on. In order to determine the capacitances for this calculation from the datasheet curves, it is also necessary to estimate the  $V_{ds}$  where this peak  $dv_{ds}/dt$  will occur. Based on (6.31), the slope of  $dv_{gs}/dt$  will likely remain positive until  $C_{rss}$  suddenly increases in size and causes  $v_{gs}$  to begin dropping (often occurring when  $v_{ds}$  falls below 50-100 V). Conveniently, this is also the point where output capacitance begins to increase dramatically. Therefore, for solving (6.34),  $C_{oss}$  and  $C_{rss}$  can be determined from the curve at the voltage where  $C_{rss}$  experiences a steep slope, and  $C_{sync}$  can be determined from the curve at the dc link minus that voltage. Figure 6.10 shows an example of this parameter extraction using the 650 V GaN Systems GS66508P datasheet [166].

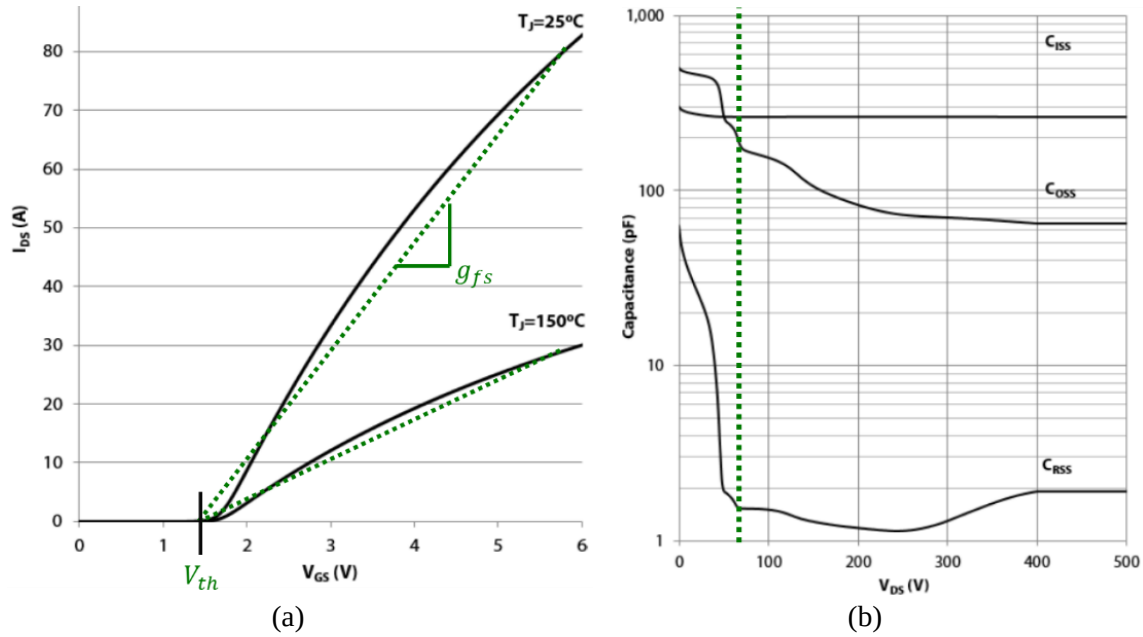


Figure 6.10. Parameter extraction for peak  $dv_{ds}/dt$  prediction, using the datasheet for GaN Systems GS66508P.

For turn-off, the peak  $dv_{ds}/dt$  will likely occur when  $v_{gs}$  is below  $V_{th}$ , as described in (6.34). The capacitances in this case are easier to determine, as the peak is likely to occur near the middle of the voltage rise time when the total output capacitance of both switches is nearly constant, so  $v_{ds}$  can be estimated at  $V_{dc}/2$  for parameter extraction.

Figure 6.11 shows the peak turn-on  $dv_{ds}/dt$  for the GS66508P, and Figure 6.12 shows the peak turn-off  $dv_{ds}/dt$ . The proposed method is much closer to the experimental results than (2.4) or (2.5). It is clear from these comparisons that all three models approach the experimental results at high gate resistance, when the device begins to behave more like a slower-switching Si MOSFET and a Miller plateau is likely to occur. However, at lower gate resistance, the gate voltage passes the Miller voltage by several volts during both transients, and the proposed model captures the peak  $dv_{ds}/dt$  much more accurately as a result.

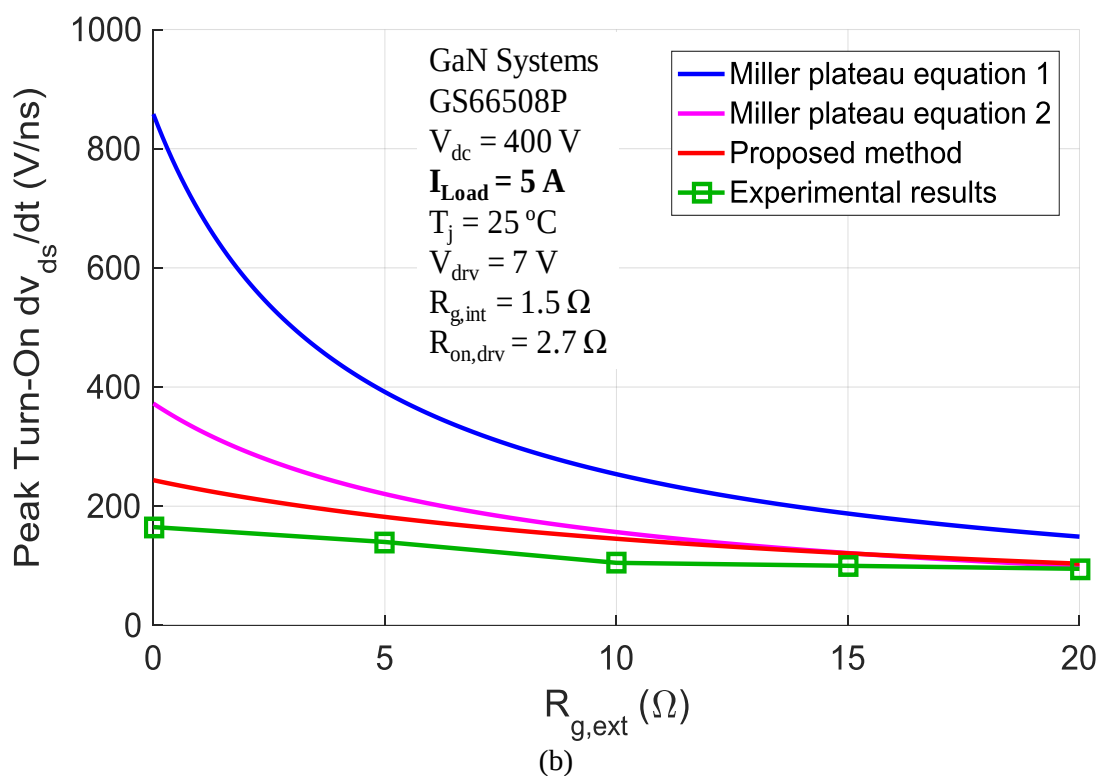
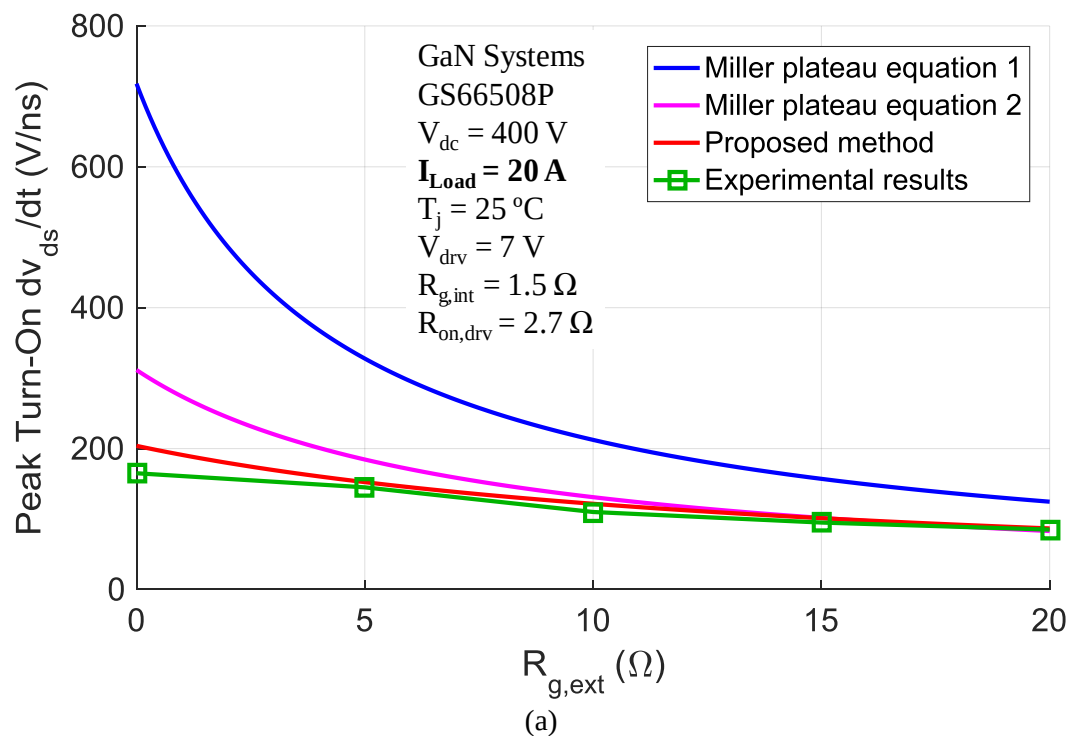


Figure 6.11. Peak turn-on  $dv_{ds}/dt$  predictions with different external gate resistances, for GaN Systems GS66508P driven with Si8233 at 7 V, with 400 V dc bus and (a) 20 A and (b) 5 A load currents.

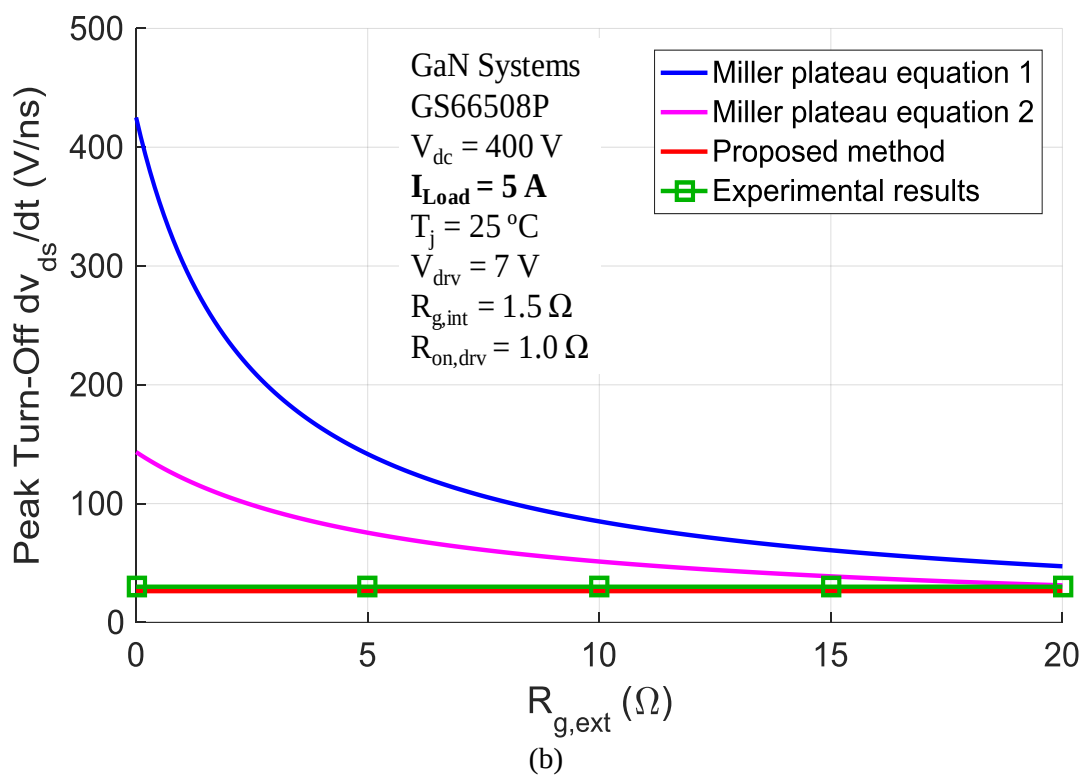
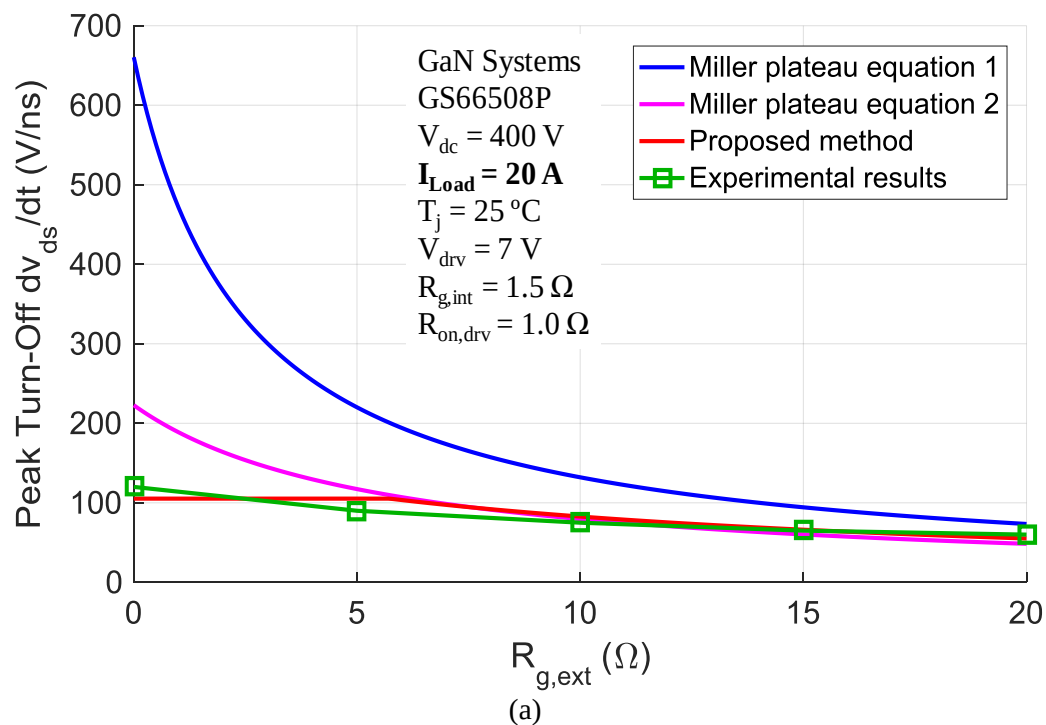


Figure 6.12. Peak turn-off  $dv_{ds}/dt$  predictions with different external gate resistances, for GaN Systems GS66508P driven with Si8233 at 7 V, with 400 V dc bus and (a) 20 A and (b) 5 A load currents.

## 6.6 *Analysis of the temperature dependency of the turn-on transient*

### 6.6.1 *Introduction*

One distinction between Si, SiC, and GaN semiconductors is their behavior at elevated junction temperature. Both Si and SiC exhibit little change in switching loss at higher temperature. However, enhancement-mode GaN devices have been shown to experience higher turn-on loss at elevated junction temperature, requiring a robust cooling design to prevent thermal runaway. This has been shown in the previous chapter as well as in [52], and it points to a fundamental difference between GaN and other power semiconductor materials.

The effect of temperature on GaN transconductance has been well-studied in prior literature, and is generally attributed to the decrease in 2DEG density and quantum well depth [248]. This work will show that the increased turn-on losses can be explained by the negative temperature coefficient of transconductance for these GaN devices. A relationship will be derived between junction temperature and turn-on loss, and verified experimentally with the GaN Systems GS66508P. The results shown in the previous chapter demonstrate that turn-on and turn-off overlap switching losses increase with temperature, but the increase in turn-on loss is much more significant and should not be ignored in GaN-based converter design.

Performing DPT at elevated temperature is very challenging with GaN devices, because of the chip-scale or PQFN packaging commonly used rather than bulkier TO-220 or TO-247 packages that are easier to heat. Elevating the temperature of the GaN device with a hot plate requires a connection on the top-side of the device or through the PCB, neither of which is convenient in a DPT. Alternatively, placing the entire board in an oven to heat the device compromises the other components, as well as affecting the integrity of measurement probes. Therefore, it is more desirable to perform the DPT at room temperature and scale the measured losses based on available static parameters.

The switching transients and losses of Si power MOSFETs have been well studied, but the interactions between device and board parasitics makes it difficult to analytically predict switching losses without experimental data. For this work, DPT experiments were performed at elevated temperatures, and a temperature-dependent model is proposed to predict the turn-on losses as junction temperature increases.

### 6.6.2 Relationship between transconductance and turn-on loss

The derived equations for current rise time and voltage fall time are given in

$$t_{cr} = \frac{I_L}{g_{fs} \left( \frac{dv_{gs}}{dt} \right)} \quad (6.35)$$

$$t_{vf,sat} = \sqrt{\frac{4 q_{oss}}{g_{fs} \left( \frac{dv_{gs}}{dt} \right)}} \quad (6.36)$$

The losses due to the displacement of  $C_{oss}$  stored energy in the active and synchronous devices are independent of turn-on time. The time-independent loss in the active device due to the synchronous device  $C_{oss}$  can be calculated from (6.13). The loss component due to the discharge of the active device  $C_{oss}$  into its own channel is given in (6.14) [247].

The remaining losses during  $t_{cr}$  and  $t_{vf,sat}$  are strongly dependent on the duration of the turn-on transient. During  $t_{cr}$ , the voltage is nearly constant at  $V_{dc}$  while the channel current rises linearly up to the load current. The time-dependent energy loss during this time can be calculated as

$$E_{on,cr} = \frac{1}{2} t_{cr} (V_{dc} I_L) \quad (6.37)$$

During  $t_{vf,sat}$ , the channel conducts the full load current while the voltage drops from  $V_{dc}$  to nearly 0 V. The voltage during  $t_{vf,sat}$  is determined by the nonlinear  $C_{oss}$  characteristic. If the voltage drop is initially approximated as linear, the time-dependent losses during this interval can be estimated with the simplified relationship

$$E_{on,td,vf} \approx \frac{1}{2} t_{vf,sat} (V_{dc} I_L) . \quad (6.38)$$

The total turn-on loss can be described as the sum of these four components, but the component given in (6.14) is generally considered as turn-off loss. This energy is actually lost during the turn-on transient, but it can only be experimentally measured during the turn-off transient, when the energy is stored in the active device  $C_{oss}$ . Therefore, the conventional definition of turn-on loss can be described as the sum of these three components:

$$E_{on} = E_{on,Coss,sync} + E_{on,cr} + E_{on,td,vf} . \quad (6.39)$$

### 6.6.3 Effect of temperature on transconductance

For a given device, the turn-on speed is mainly determined by the operating voltage and current, the  $C_{oss}$  characteristic, gate driver speed  $dv_{gs}/dt$ , and device transconductance  $g_{fs}$ . If  $dv_{gs}/dt$  and  $g_{fs}$  are both relatively high, the device channel will conduct more current, and the  $C_{oss}$  charge will be displaced quickly. However, GaN is distinct from Si and SiC in that its transconductance has a significant negative temperature coefficient. For the device under test (DUT) considered in this analysis, GaN Systems GS66508,  $g_{fs}$  was experimentally measured with a curve tracer over the rated temperature range. The calculation for average  $g_{fs}$  is given in (6.40), and the results over the device temperature range are shown in Figure 6.13.

$$g_{fs} = \frac{I_{dss(vgs=5V)} - I_{dss(vgs=2V)}}{(3 V)} \quad (6.40)$$

The average transconductance drops by about one half over the rated temperature range of the DUT. According to (6.6), this also reduces the channel current while the device is operating in saturation, and consequently lengthens  $t_{cr}$  and  $t_{vf,sat}$ . As given in (6.35) and (6.36), this increases the current rise time and  $E_{on,cr}$  by a factor of 2, and the voltage fall time and  $E_{on,td,vf}$  by a factor of  $\sqrt{2}$ .

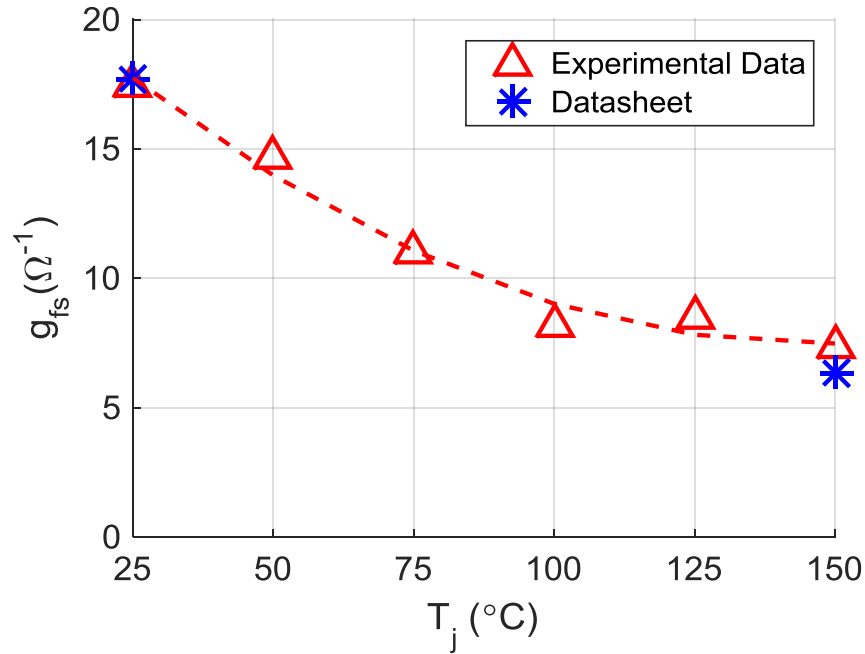


Figure 6.13. Average transconductance of GaN Systems GS66508P from static measurement over temperature.

#### 6.6.4 Special case if gate voltage saturates

In the experimental verification of this model, a special case was observed in which the analysis in the previous section no longer holds. If the  $t_{vf,sat}$  becomes long enough that the gate voltage  $v_{gs}$  reaches  $V_{drv}$  while the device is still displacing  $C_{oss}$  charge, then the gate voltage saturates at  $V_{drv}$  and can no longer increase. The channel current will be limited by the driving voltage after that time. Therefore, the voltage fall time can no longer be determined from (6.36). Instead, it must be modeled as two distinct subintervals,  $t_{vf,sat1}$  and  $t_{vf,sat2}$ .

This special case will occur when

$$t_{cr} + t_{vf,sat} > \frac{(V_{drv} - V_{gs,th})}{dv_{gs}/dt} . \quad (6.41)$$

The turn-on transient for this special case is shown in Figure 6.14. During the second subinterval, the channel current will be held constant at



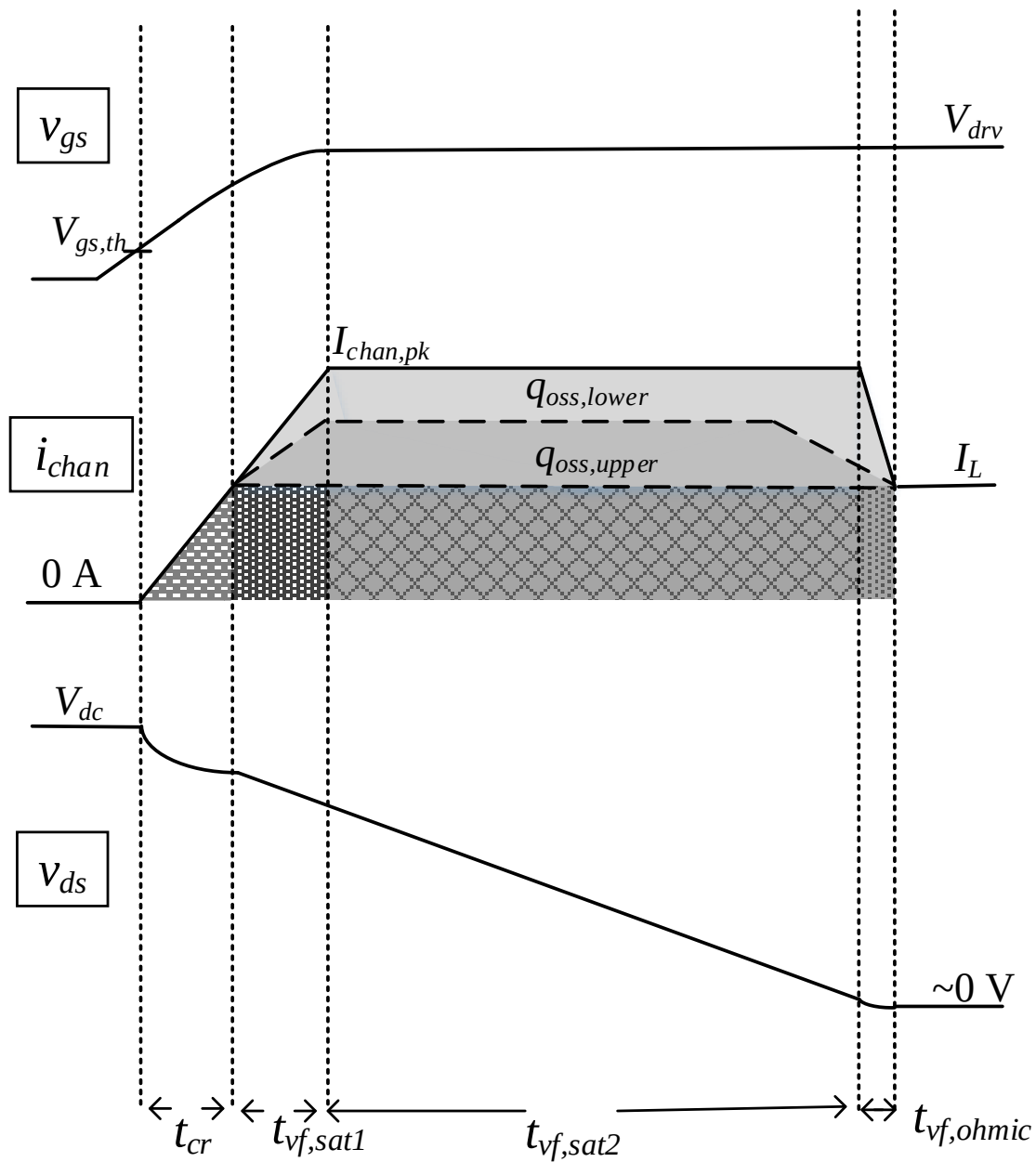


Figure 6.14. Turn-on transient analysis of the active device for the special case when gate voltage reaches its peak during the  $dv/dt$  transient.

$$i_{chan,tvfat2} = g_{fs}(V_{drv} - V_{gs,th}) . \quad (6.42)$$

Therefore, the displacement current will be fixed during this subinterval, rather than increasing as in  $t_{vf,sat1}$ . The  $C_{oss}$  charge will be displaced at a fixed, non-increasing rate, and the new subinterval  $t_{vf,sat2}$  can become quite long. The durations of  $t_{vf,sat1}$  and  $t_{vf,sat2}$  can be calculated as

$$t_{vf,sat1} = \frac{V_{drv} - V_{gs,th}}{dv_{gs}/dt} - t_{cr} \quad (6.43)$$

$$q_{sat1} = \frac{1}{2} g_{fs} \frac{dv_{gs}}{dt} t_{vf,sat1}^2 \quad (6.44)$$

$$q_{sat2} = 2q_{oss} - q_{sat1} \quad (6.45)$$

$$t_{vf,sat2} = \frac{q_{sat2}}{g_{fs}(V_{drv} - V_{gs,th}) - I_L} . \quad (6.46)$$

Since the voltage is still dropping from  $V_{dc}$  to 0 V during the combined voltage fall time, the linear simplification can still approximate the  $t_{vf}$  energy loss as

$$E_{on,vf} \approx \frac{1}{2} (V_{dc} I_L) (t_{vf,sat1} + t_{vf,sat2}) . \quad (6.47)$$

In the experimental verification of this model, the special case was only observed at higher junction temperatures. This did not occur at room temperature, because the recommended driving voltage and room temperature  $g_{fs}$  allowed for a saturation channel current much higher than the rated maximum load current. This case is more likely to occur when the driving voltage or transconductance is low, the displacement charge  $q_{oss}$  is high, and the Miller effect is relatively weak.

### 6.6.5 Consideration of nonlinear $C_{oss}$

For the analysis in the previous two sections, the voltage drop during the voltage fall time was treated as linear. This was necessary for the theoretical understanding of temperature dependence, but the nonlinear  $C_{oss}$  characteristic can be used to improve the accuracy of the model.

The linear approximation is inherently an underestimate, because the voltage is exponentially decreasing, and the average voltage during  $t_{vf}$  should be higher than  $V_{dc}/2$ .

The  $C_{oss}$  characteristic is given in the datasheet for most devices. For the DUT in this analysis,  $C_{oss}$  was measured with a precision impedance analyzer and also published in [166] among others. Figure 6.15 shows the total switch-node capacitance, which is the sum of the active device and synchronous device  $C_{oss}$  as the switch-node voltage falls from 400 V to 0 V and is calculated by

$$C_{sw}(v_{sw}) = C_{oss}(v_{sw}) + C_{oss}(V_{dc} - v_{sw}) . \quad (6.48)$$

The  $C_{oss}$ -related switching losses can be calculated from this curve, and the total charge displaced  $q_{sw}$  can be calculated as a function of switch-node voltage using

$$q_{sw}(v_{sw}) = \int_{v_{sw}}^{V_{dc}} C_{sw}(v) dv . \quad (6.49)$$

Figure 6.16 shows the results of this calculation. The total displacement charge in both devices is equal to  $2q_{oss}$  and can be found from the  $q_{sw}$  curve when  $V_{sw} = 0$  V.

Accounting for this nonlinear capacitance complicates the turn-on loss analysis, because the calculation requires integration of switch-node voltage over time as in

$$E_{on,td,vf} = I_L \int_0^{t_{vf,sat}} v_{sw}(t) dt \quad (6.50)$$

where  $v_{sw}(t)$  can be determined from a combination of the  $v_{sw}$  vs.  $q_{sw}$  characteristic given by (6.48) and the equation

$$q_{sw}(t) = \frac{1}{2} g_{fs} \frac{dv_{gs}}{dt} t^2 . \quad (6.51)$$

This calculation is more accurate, but requires a software tool such as MATLAB to solve. The  $C_{oss}$  characteristic can be imported and interpolated, then a discrete-time interval can be used to calculate  $q_{sw}$  and  $E_{on,td,vf}$ .

Similarly, (6.47) can be revised to

$$E_{on,td,vfsat1} = I_L \int_0^{t_{vf,sat1}} v_{sw}(t) dt \quad (6.52)$$

where  $v_{sw}(t)$  can be determined from (6.47) and (6.49), and

$$E_{on,td,vfsat2} = I_L \int_0^{t_{vf,sat2}} v_{sw}(t) dt \quad (6.53)$$

where  $v_{sw}(t)$  can be determined from (6.47) and

$$q_{sw}(t) = q_{sat1} + [g_{fs}(V_{drv} - V_{gs,th}) - I_L]t . \quad (6.54)$$

#### 6.6.6 Assumptions and simplifications for the model

##### a) Average transconductance

In this analysis, the average transconductance was used, because that parameter is listed in most device datasheets or can be calculated from published curves. However,  $g_{fs}$  is actually variable during the transient and increases as a function of the gate voltage  $v_{gs}$  and potentially also with output voltage  $v_{ds}$ . To investigate this relationship, the transconductance was measured dynamically for the DUT, using a double pulse test as described in the previous chapter. In a typical DPT, the externally measured  $v_{gs}$  is not an accurate representation of the true internal  $v_{gs}$  due to the voltage drop across the internal  $R_g$  and  $L_{gs}$  of the device package. For this dynamic  $g_{fs}$  characterization, an external gate resistance of 1 k $\Omega$  was used so that the voltage drop across the internal device impedance was negligible in comparison. Using these  $v_{gs}$  and  $I_{dss}$  measurements, a dynamic  $g_{fs}$  vs.  $v_{gs}$  characteristic was determined during the current rise time. Figure 6.17 shows the  $g_{fs}$  calculated from two turn-on transients and two turn-off transients, demonstrating the positive correlation between  $g_{fs}$  and  $v_{gs}$ . However, the average  $g_{fs}$  between 2 V and 5 V matches the static measurement shown in Figure 6.17 at 25 °C.

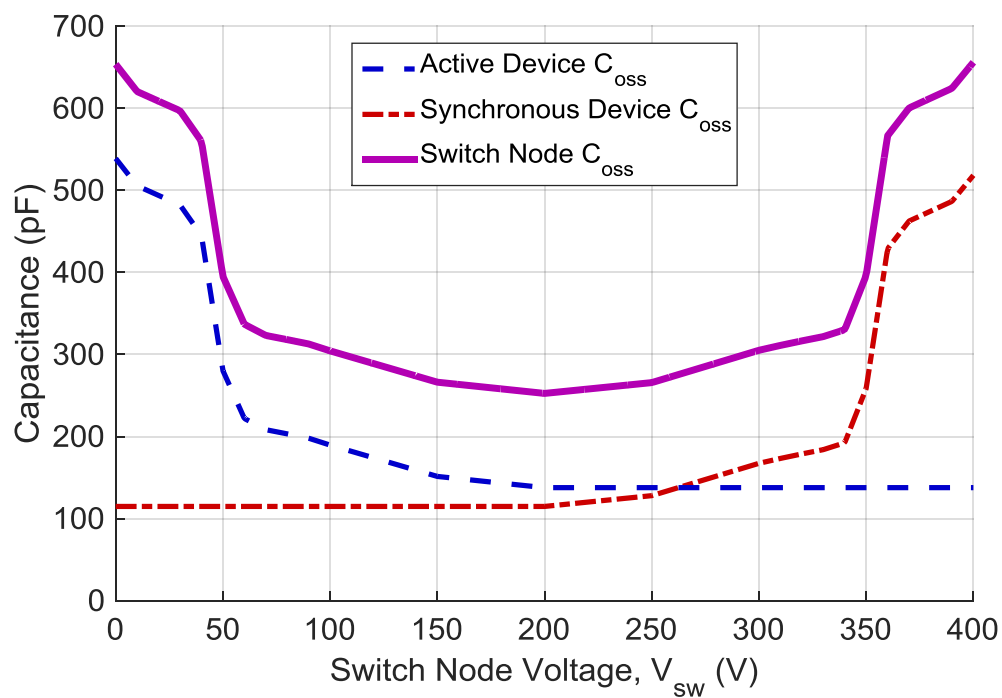


Figure 6.15. Output capacitance at the switch-node, with the DUT switching at 400 V.

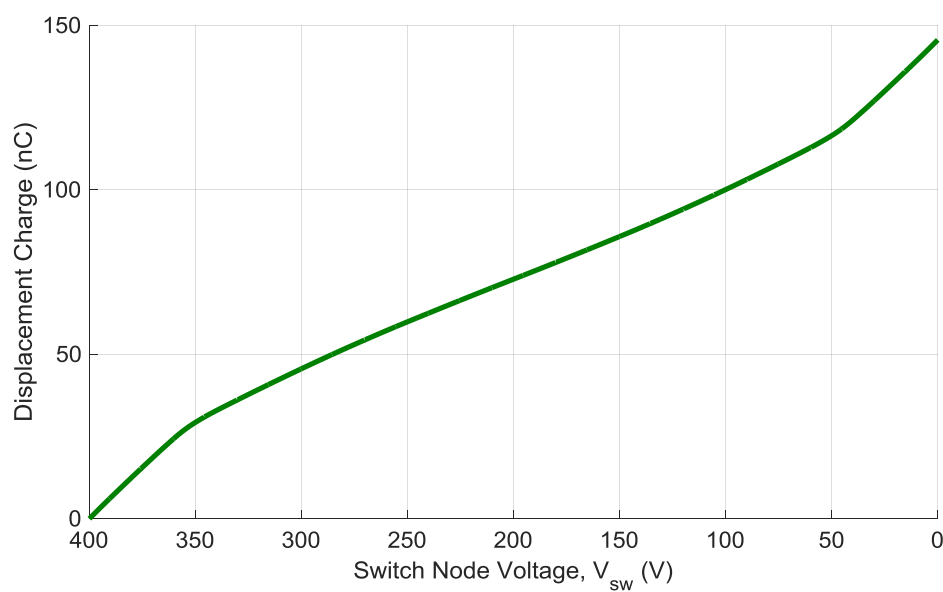


Figure 6.16. Charge displaced in the active and synchronous devices as the switching node voltage falls from 400 V.

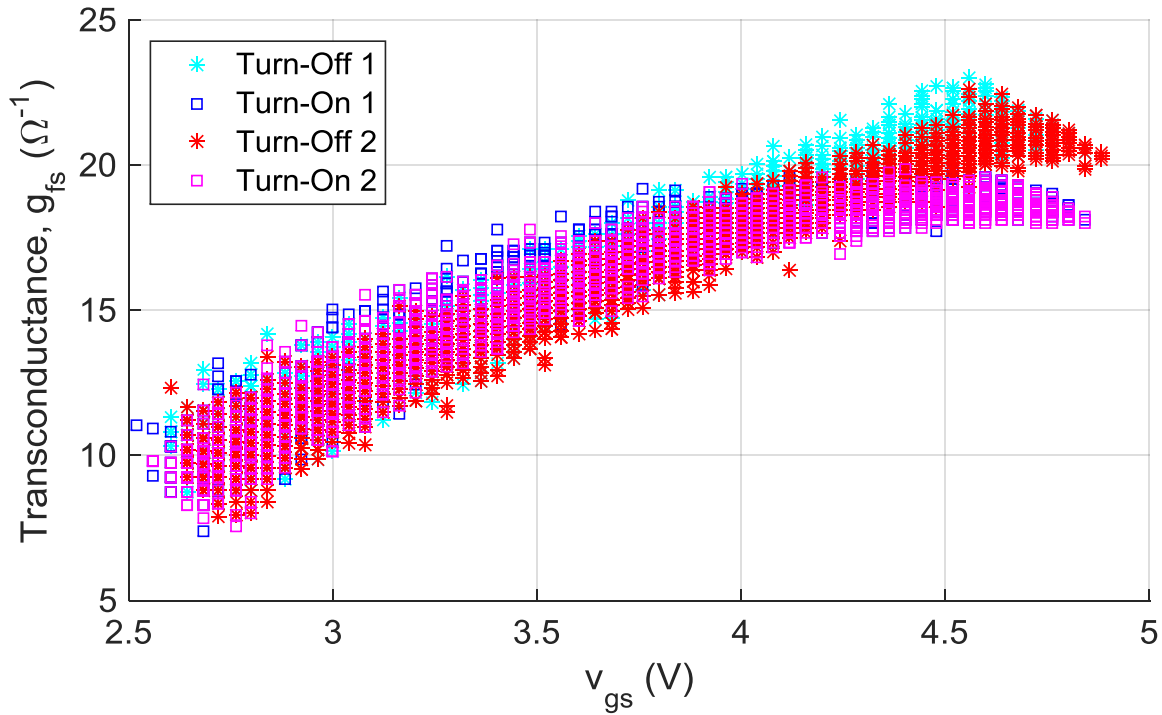


Figure 6.17. Transconductance of GS66508P measured during dynamic testing at 25 °C.

b) Constant gate voltage slope

The slope  $dv_{gs}/dt$  was approximated as a constant value for this analysis. However, this slope will drop exponentially as the gate voltage approaches the driving voltage. Because  $g_{fs}$  increases with gate voltage and  $dv_{gs}/dt$  decreases, the product  $g_{fs}dv_{gs}/dt$  remains fairly constant during the transient. It would improve the accuracy of the model to consider both  $dv_{gs}/dt$  and  $g_{fs}$  as  $v_{gs}$ -dependent variables, but this would add considerable complexity. Instead, it is effective to use the average values for both.

c) Negligible Miller effects

As shown earlier in this chapter, a fast gate drive circuit can minimize the Miller effect, so that  $dv_{gs}/dt$  is only somewhat reduced during the voltage fall time  $t_{vf,sat}$ . This requires a gate driver IC that can provide sufficient current, and the total impedance of the gate loop must be minimized

with low resistance and a dense layout. Common-source inductance is also critical, so a Kelvin gate connection should be used when possible.

Even if these conditions are met, there may still be significant ringing in the  $v_{gs}$ ,  $v_{ds}$ , and  $i_{chan}$  waveforms at the end of  $t_{vf,sat}$ , because  $C_{gd}$  gets much larger at low voltage. The ringing on  $C_{gd}$  will cause the device to alternate between the ohmic and saturation regions several times before  $C_{gd}$  has fully discharged. However, as long as it only occurs near the end of  $t_{vf,sat}$ , the losses due to this ringing are generally not very significant.

d) Constant threshold voltage

For some power devices, the threshold voltage  $V_{gs,th}$  may be affected by temperature. However, the DUT and most GaN devices have a very stable threshold voltage over temperature, so it was not considered as a significant factor in this analysis.

e) Low power loop inductance

The parasitic power loop inductance  $L_{loop}$  is usually minimized for GaN-based converters with a dense board design and optimal device packaging. However,  $L_{loop}$  still causes an initial drop in  $V_{sw}$  during  $t_{cr}$ , which may not be negligible. However, this drop occurs on the active device when its voltage is high and its capacitance is at its lowest, and the magnitude of  $L_{loop}$  is not affected by temperature, so the effects of  $L_{loop}$  were neglected in this analysis.

f) Cross-talk loss

Lastly, the additional loss in the saturated channel due to cross-talk in the synchronous device was not considered in this analysis. The DPT experiments for this work used a gate-source shorted synchronous device to minimize cross-talk effects. Additionally, the previous chapter showed that the cross-talk component of turn-on loss is not noticeably impacted by temperature. Cross-talk should not be ignored for turn-on loss estimation, but the magnitude of this loss can be considered separately from the temperature-dependent losses.

### 6.6.7 Simplified linear approximation

In GaN-based converter design, it is common to perform a DPT with the chosen device, driver, and layout to characterize the switching losses at the intended operating voltage and current condition. It is therefore desirable to scale these results for the intended operating temperature, without the need to elevate device temperature during testing. Although the detailed model could be used for this purpose, it is useful to consider the linearized model described by (6.37) and (6.38). Because the majority of overlap loss occurs during the voltage fall time, the turn-on loss can be estimated for a given temperature using a simple scaling factor with the approximation

$$E_{on,Tj} \approx E_{on,Coss,sync} + k_{Eon,Tj}(E_{on,25C} - E_{on,Coss,sync}) \quad (6.55)$$

where  $E_{on,25C}$  is the experimentally measured turn-on loss at the operating current and voltage,  $E_{on,Coss,sync}$  is the loss calculated with (6.13) based on the nonlinear  $C_{oss}$  characteristic, and  $k_{Eon,Tj}$  is the scaling factor

$$k_{Eon,Tj} = \sqrt{\frac{g_{fs,25C}}{g_{fs,Tj}}} . \quad (6.56)$$

This scaling factor will typically be between 1 and 2 depending on the GaN device under test, and it can be easily determined from the device datasheet. Typical datasheets show the transfer characteristic at various gate voltages, with 25 °C junction temperature and a higher  $T_j$  such as 125 °C or 150 °C. Average transconductance can be calculated from these characteristics using (6.40) at each temperature, and the  $g_{fs}$  at the intended operating temperature can be determined with linear interpolation.

This approximation requires no tuning or simulation, but its accuracy heavily depends on the experimental turn-on loss data at room temperature and the  $C_{oss}$  characteristic, as well as consideration for any additional capacitance from the PCB and test setup. It is also more limited in application than the detailed model, because it assumes that the voltage fall time is longer than the



current rise time. With high current and very low voltage, the scaling factor may begin to approach  $k_{Eon,Tj}^2$ .

### 6.6.8 Experimental verification

Double pulse testing (DPT) was performed on the DUT at junction temperatures ranging from 25 °C to 150 °C, with an 8 V gate drive and 0  $\Omega$  external gate resistance. Experimental test setup, results, and device characterization were detailed in the previous chapter. The channel current waveform was estimated using the technique described in Chapter 4. It is important to note that the measured external gate voltage is only an approximation of the true internal gate voltage, so it is not equivalent to the  $v_{gs}$  used in this theoretical analysis. Rather than rely on this waveform, the value for average  $dv_{gs}/dt$  was tuned based on experimental data for turn-on time and loss, and determined to be approximately 1 V/ns in the 400 V switching case.

Figure 6.18 shows the turn-on transients at 400 V and 30 A, with junction temperatures of 25 °C and 150 °C respectively. At 25 °C, the device exits the saturation region as the gate voltage is still increasing, reaching a peak channel current of 85 A before the device enters the ohmic region and the channel current quickly drops to  $I_L$ . At higher temperature,  $v_{gs}$  reaches the driving voltage before all of the  $C_{oss}$  charge has been displaced, resulting in the special case described previously. The channel current is then held at ~50 A until the  $C_{oss}$  charge has been displaced and the device drops into the ohmic region. In both waveforms, the ringing due to  $C_{gd}$  is very pronounced as the device enters the ohmic region, but the net energy loss during this ringing period is low, since  $v_{ds}$  has already dropped to nearly 0 V.

Using the derived model, switching times and energy loss were calculated across the current and temperature range at 200 V and 400 V. Experimental results were not used in these calculations, except for tuning  $dv_{gs}/dt$  as previously mentioned. Figure 6.19 - Figure 6.22 compare the experimental results with those predicted by the model. The calculated energy loss matches

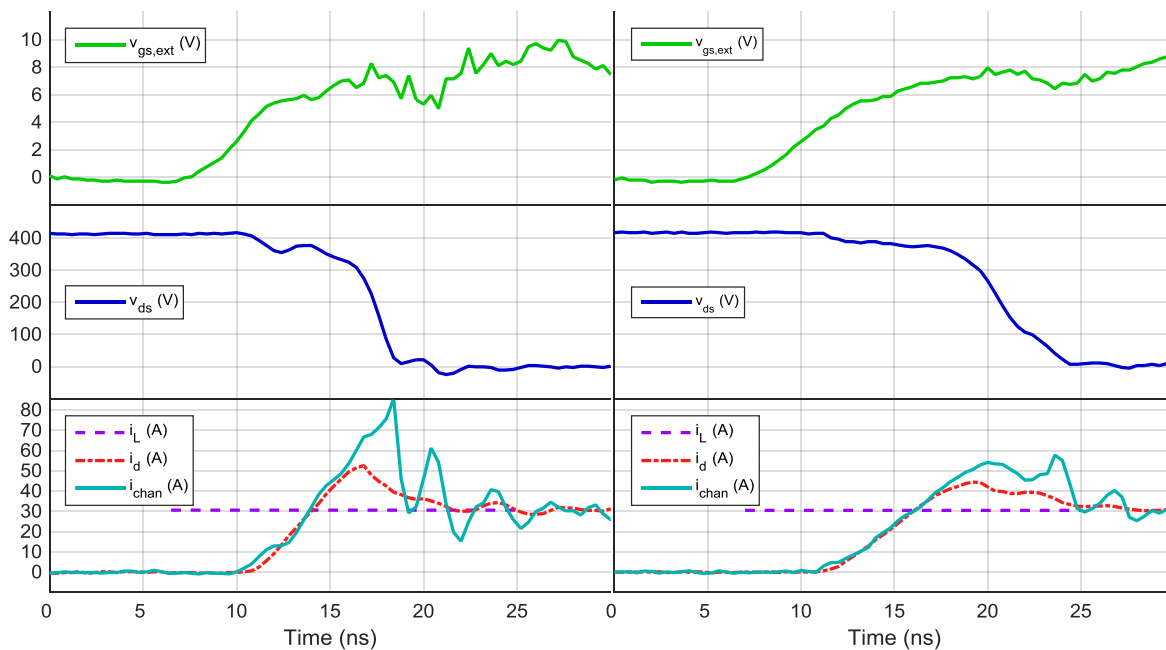


Figure 6.18. Experimental turn-on transient waveforms of the active device at 400 V and 30 A, (a) 25 °C and (b) 150 °C.

well with experimental results, although it is shown to be slightly less accurate in some cases. With low voltage or high load current, the assumptions made in Section V begin to break down, especially regarding the Miller effect and the significance of the initial voltage drop across the loop inductance. However, the model matches experimental results very well if the average  $dv_{gs}/dt$  is tuned appropriately.

Figure 6.23 and Figure 6.24 show the linear approximations at 400 V and 200 V, respectively. This approximation matches experimental results even more closely than the detailed theoretical model, because it is directly based on the DPT results at 25 °C. However, this approximation relies on even more assumptions than the detailed analytical model, so it may not be as accurate for all e-mode GaN devices and converter designs as it is for the DUT considered here.

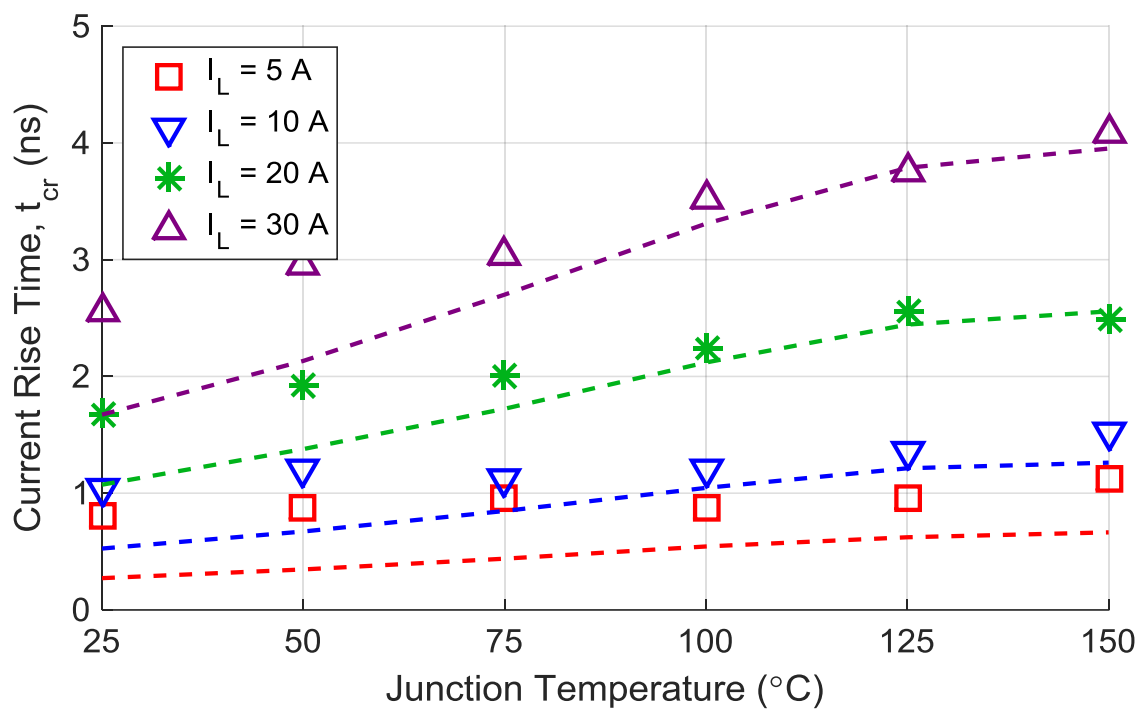


Figure 6.19. Experimental results for current rise time of the DUT at 400 V, with the dashed lines showing calculated  $t_{cr}$  based on the detailed analytical model.

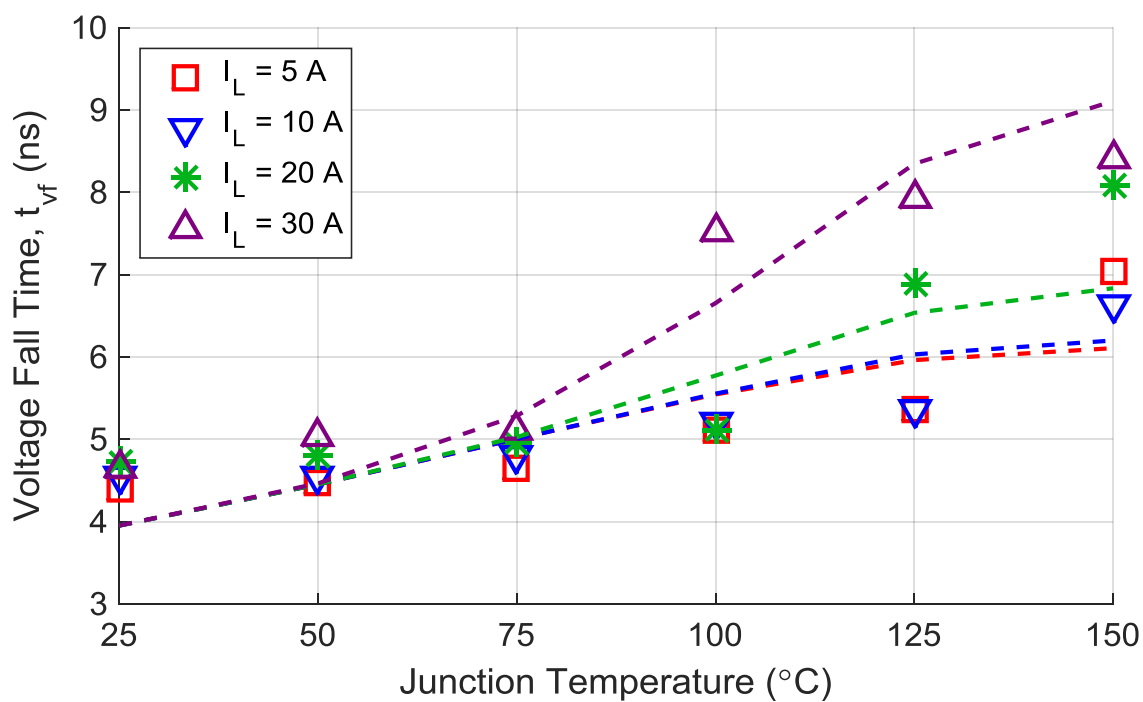


Figure 6.20. Experimental results for voltage fall time of the DUT at 400 V, with the dashed lines showing calculated  $t_{vf,sat}$  based on the detailed analytical model.

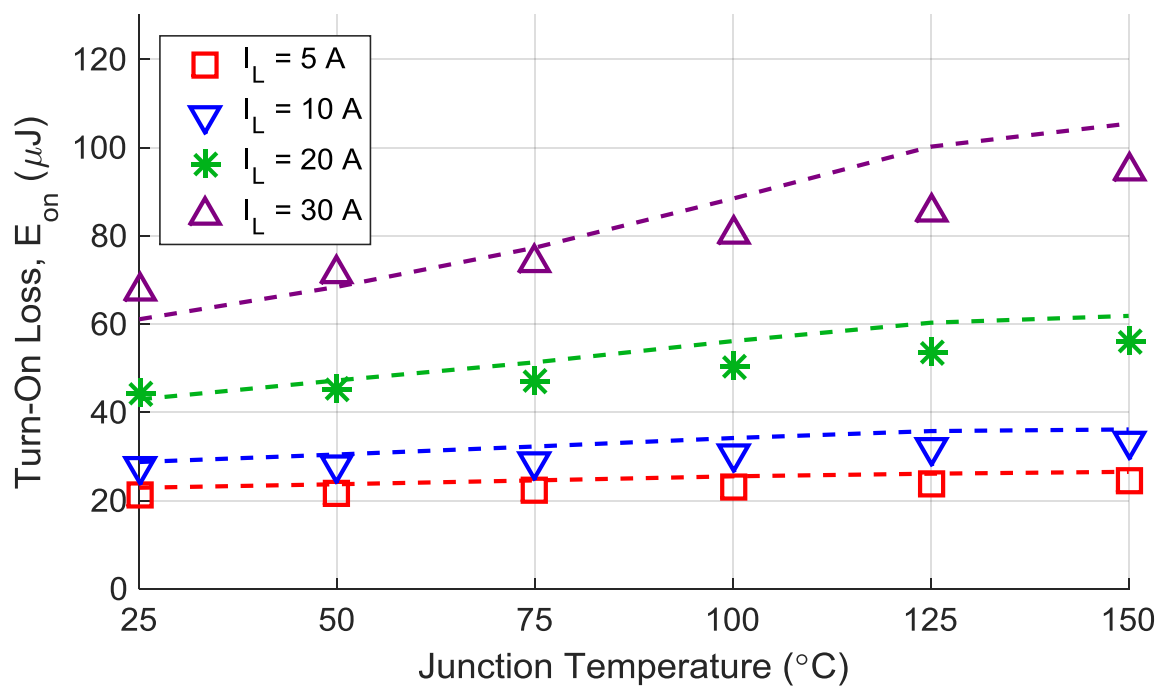


Figure 6.21. Experimental results for  $E_{on}$  of the DUT at 400 V, with the dashed lines showing predictions by the detailed analytical model

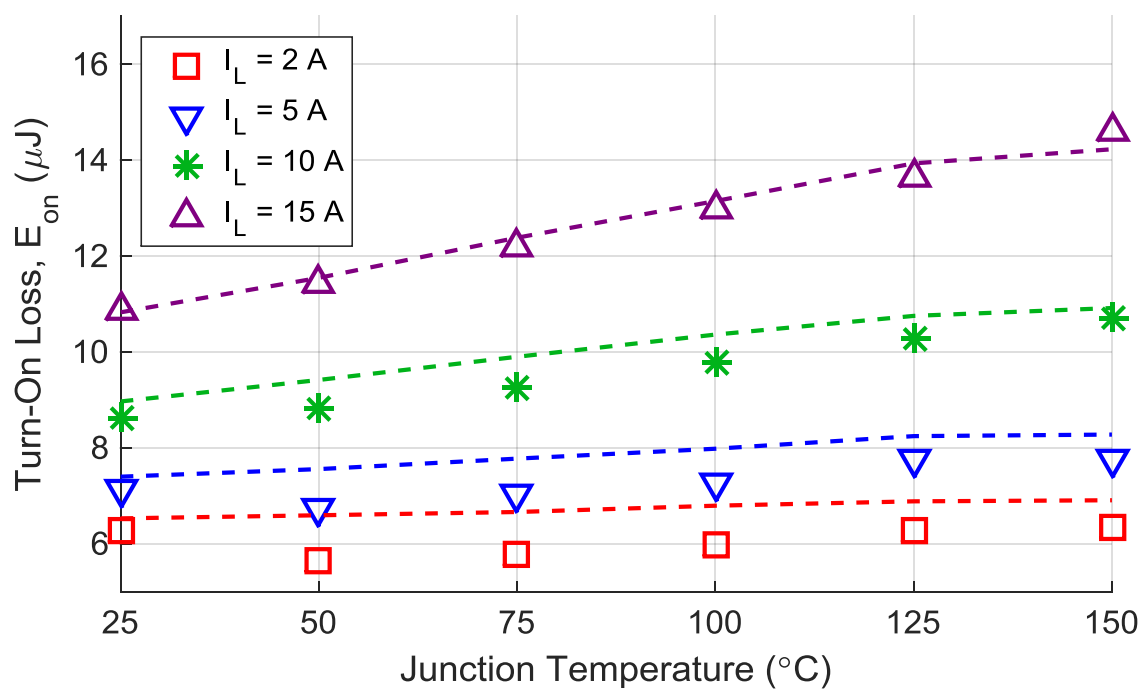


Figure 6.22. Experimental results for  $E_{on}$  of the DUT at 200 V, with the dashed lines showing predictions by the detailed analytical model.

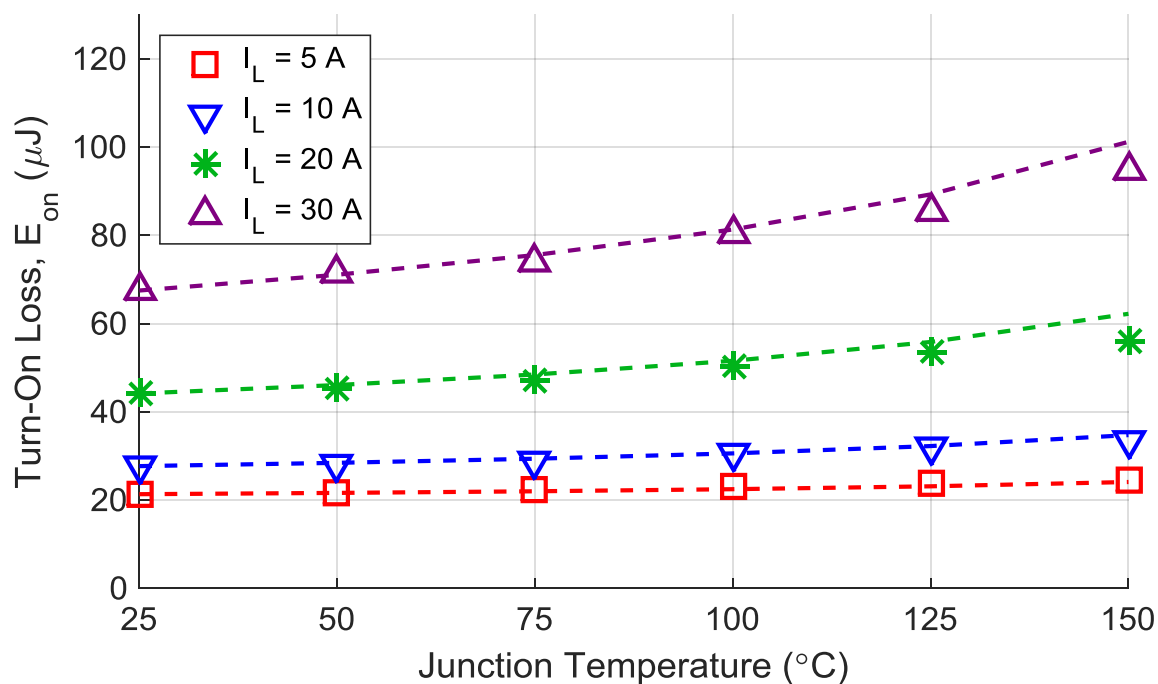


Figure 6.23. Experimental results for  $E_{on}$  of the DUT at 400 V, with the dashed lines showing the linear approximations calculated using published datasheet parameters and DPT data at 25  $^{\circ}\text{C}$ .

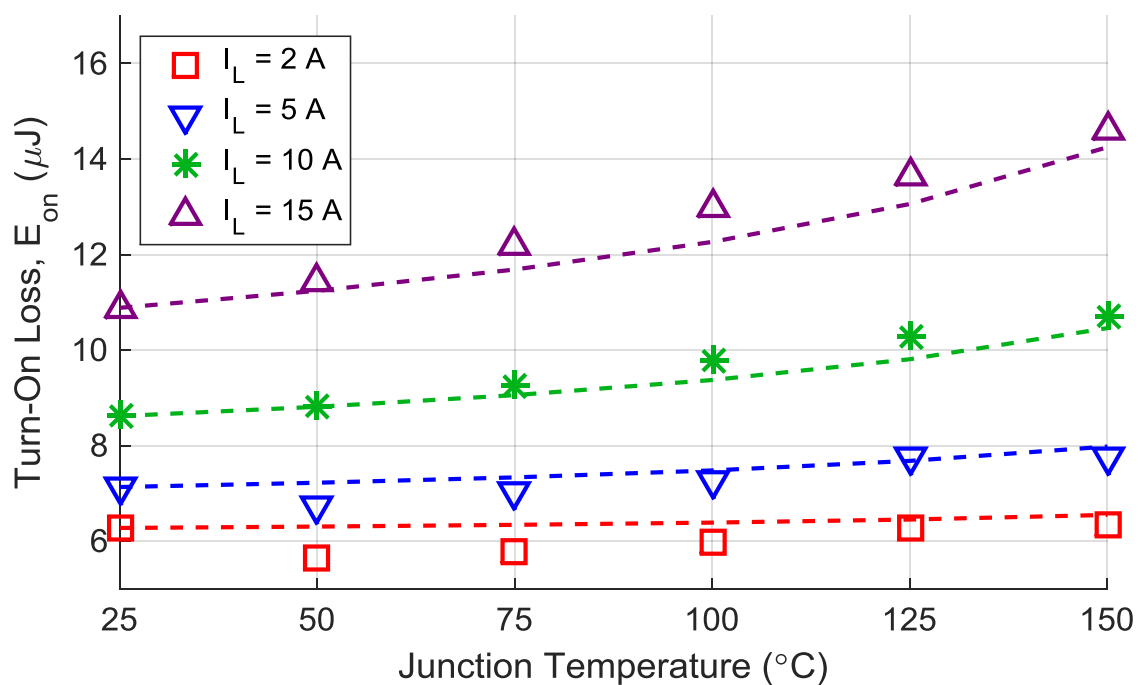


Figure 6.24. Experimental results for  $E_{on}$  of the DUT at 200 V, with the dashed lines showing the linear approximations calculated using published datasheet parameters and DPT data at 25  $^{\circ}\text{C}$ .

## 6.7 Summary

The general switching behavior of the enhancement-mode GaN HFET has been described with a subcircuit model and subinterval analysis. The voltage and current equations for each subinterval were given, neglecting some complexities such as power loop and gate loop inductance. These equations were then verified for overall waveform shape through comparison with experimental results and simulation. One of the significant elements studied in this model was the Miller effect during turn-on, which causes a reduced gate voltage slope during the voltage fall time, followed by a sharp drop near the end of the transient.

Another element of this analysis was the effect of temperature on the turn-on loss of the enhancement-mode GaN device. The root cause of temperature-dependent turn-on loss was attributed to decreased transconductance. Using theoretical analysis and experimental results, a turn-on loss model was developed to predict the effect of elevated junction temperature at any given current and voltage condition for a GaN device, based on the average transconductance over temperature. A detailed analytical model was developed, as well as a simplified linear approximation. The scaling factor  $k_{Eon,Tj}$  allows for typical room temperature DPT switching loss results to be adjusted for any operating temperature using only the transfer characteristic published on the device datasheet. This approximation was shown to be both simple and accurate. Accurate and comprehensive loss calculation is critical for effective thermal design, to prevent thermal runaway. Because turn-off loss does not change much with temperature, and  $T_j$  vs.  $R_{ds-on}$  trends are readily available, turn-on loss is the final component needed for calculating total losses. The proposed model closes the loop on GaN-based converter loss characterization, enabling a more robust design.

## Chapter 7

### A Fast Overcurrent and Short-Circuit Fault Protection Scheme for GaN GITs

#### 7.1 Introduction

Because of the relatively small die size of GaN devices, it is particularly important for the overcurrent protection scheme to respond quickly by turning off the faulted device and the entire converter. Recent literature has shown that a healthy GaN FET can be destroyed by a short circuit pulse as brief as 400-600 ns at 400 V [88-96], and in some cases even 200 ns [97-99]. This short-circuit capability increases significantly with lower bus voltages, but degradation may occur with any sustained short circuit condition.

Conventional desaturation overcurrent protection has been shown to function well for GaN in [100-102] with a total response time as low as 200 ns, but the desaturation detection circuit adds capacitive loading to the drain of the GaN device, increasing both the response time and the switching loss. The noise induced by the sensing diode in a desaturation circuit typically requires additional blanking time when implemented in a real converter, so even 200 ns may not be practically achievable. The unique characteristics of the GaN Gate Injection Transistor (GIT) enable an alternative protection scheme with the potential for fast response and negligible impact on switching performance.

#### 7.2 Theory of operation

Figure 7.1 shows a subcircuit model of the GaN GIT in steady-state, a modified version of the previously presented subcircuit model given in Figure 6.1. The p-doped GaN layer beneath the gate shifts the threshold positively to make the device enhancement-mode. The cause of this positive shift is the diode created at the junction of the p-GaN and the AlGaIn, which must be forward biased with a small current to complete the 2DEG channel and turn the device on. Since the effective diode occurs between the gate and the AlGaIn beneath it, a portion of the total 2DEG

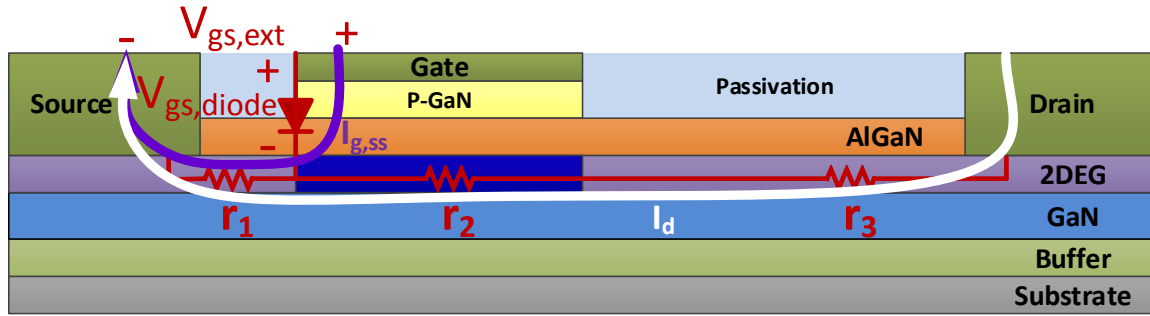


Figure 7.1. Subcircuit model for GaN GIT, showing explanation for  $I_d$ - $V_{gs}$  relationship when  $I_g$  is fixed.

channel resistance is located in series between this diode and the source terminal (or “Source Sense” pad, in the case of a four-terminal device with a Kelvin source). The distributed resistance of the 2DEG can be represented by three lumped parameters:  $r_2$  is the portion directly beneath the gate, which is depleted by the reverse-biased diode when the device is turned off;  $r_1$  is the portion on the source side of the gate; and  $r_3$  is the portion on the drain side of the gate. The lumped resistances  $r_1$  and  $r_3$  also include the contact metallizations and any other resistances between the 2DEG and the source and the drain terminals.

The typical gate drive circuit for a GIT provides a transient voltage pulse to the gate at the moment of turn-on, to enable fast and low-loss switching. Once this pulse decays, the driver provides a steady-state current to the gate,  $I_{g,ss}$ . This current is in the range of 10-50 mA, and keeps the diode forward-biased for full enhancement of the 2DEG channel. The driver is designed to provide whatever voltage is needed between the gate and source terminals to provide this steady-state current, typically in the range of 2.5-5 V as shown previously in Figure 4.15. This voltage varies with  $I_{g,ss}$ , as well as temperature and output conditions. Because of the location of  $r_1$  within the gate loop, this resistance acts as a current shunt to sense the total current flowing through it, as given by

$$V_{gs} = V_{gs,diode} + (I_d + I_g)r_1 . \quad (7.1)$$



Since  $I_{g,ss}$  is in the mA range, this means that the externally applied gate voltage  $V_{gs,ss}$  can be approximated with

$$V_{gs,ss} = V_{gs,diode} + I_d r_1 . \quad (7.2)$$

Once the turn-on transient is complete, this voltage can be used to sense the drain current and detect an overcurrent or short circuit condition.

### 7.3 Verification of concept with device characterization results

The relationship between  $I_d$  and  $V_{gs,ss}$  was confirmed with both static and dynamic characterization results, using the methodology described in Chapter 4. Figure 7.2 shows the results of testing with a curve tracer on an Infineon GIT with a sweep of junction temperatures and drain currents, matching the linear correlation given by (7.2), with  $r_1$  approximately equal to 14 mΩ. This correlation shows very little variance with temperature, which further reinforces the proposed protection scheme.

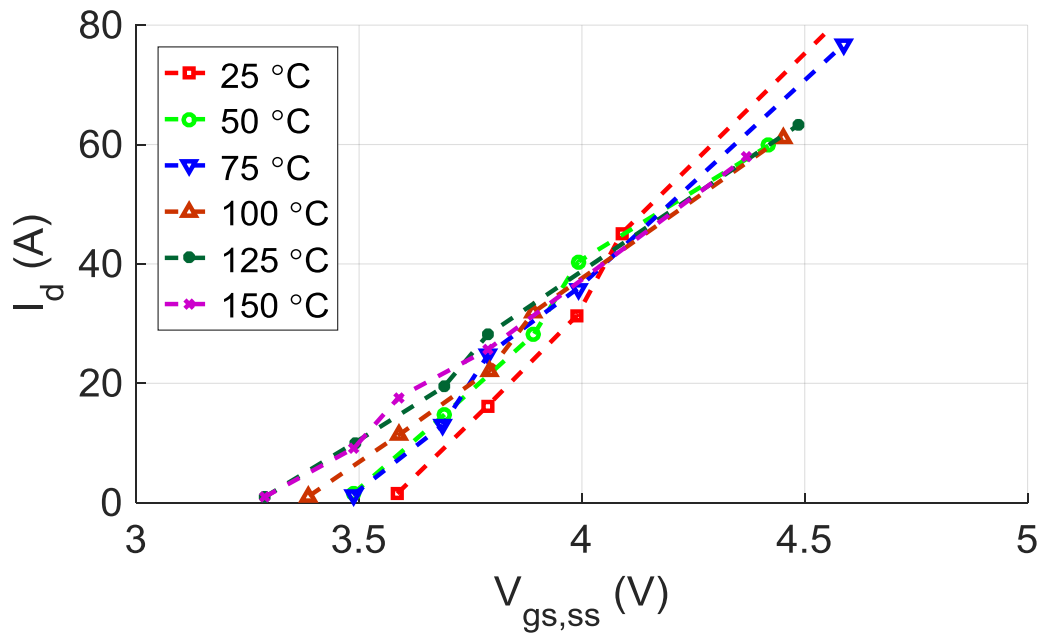


Figure 7.2.  $I_d$ - $V_{gs,ss}$  relationship from static characterization results for an Infineon GIT with  $I_{g,ss} = 25$  mA.

However, it is also important to consider the nature of this relationship in a transient case. Figure 7.3 shows the gate voltage measured during double pulse testing across a range of temperature and current conditions, with two different measurement intervals. The first samples  $V_{gs}$  at 20 ns after the end of the turn-on transient (i.e. when  $v_{ds}$  reaches 0 V). At this time, the gate voltage is still recovering from the higher voltage pulse generated by the driver for fast turn-on, and is therefore higher than indicated by the static characterization results. The second curve shows the same measurement sampled 120 ns after the end of the turn-on transient, and the results match very well with the static characterization across the full temperature range. This demonstrates the tradeoff between selection of the blanking time and the protection threshold, which will be discussed further in the next section.

Figure 7.4 shows the slope of  $V_{gs}$  with respect to both  $I_d$  and  $T_j$ , recorded at 120 ns after the turn-on transient end, using the same data shown in Figure 7.3. The sensitivity of the gate voltage to load current does indeed vary over the operating temperature range of the device, but the impact of temperature becomes negligible as the drain current approaches 30-40 A. Selecting an overcurrent threshold in this range makes it nearly immune to junction temperature variation.

#### 7.4 *Inductive overcurrent protection circuit design*

Figure 7.5 shows a schematic of the first implementation of the overcurrent protection circuit, based on the relationship between  $I_d$  and  $V_{gs}$ . This version of the circuit was designed specifically for limitation of inductive overcurrent conditions, rather than short-circuit fault conditions. The primary components of the circuit include the following:

- The gate driver IC (AN34092B from Panasonic), marked by the shaded box, which provides the transient voltage pulse at turn-on, as well as a constant current  $I_{g,ss}$  during steady-state
- The GIT itself (from Infineon), along with the discrete components of the gate drive circuit used to limit the turn-on and turn-off speeds, and the resistor  $R_{ig,ctrl}$ , which sets  $I_{g,ss}$

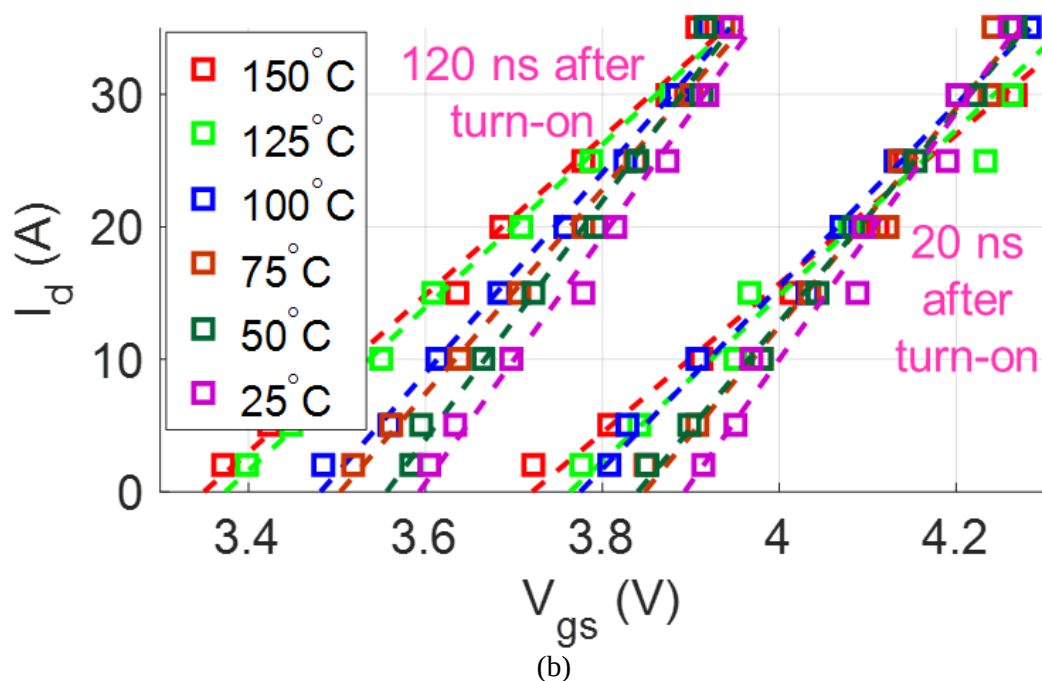
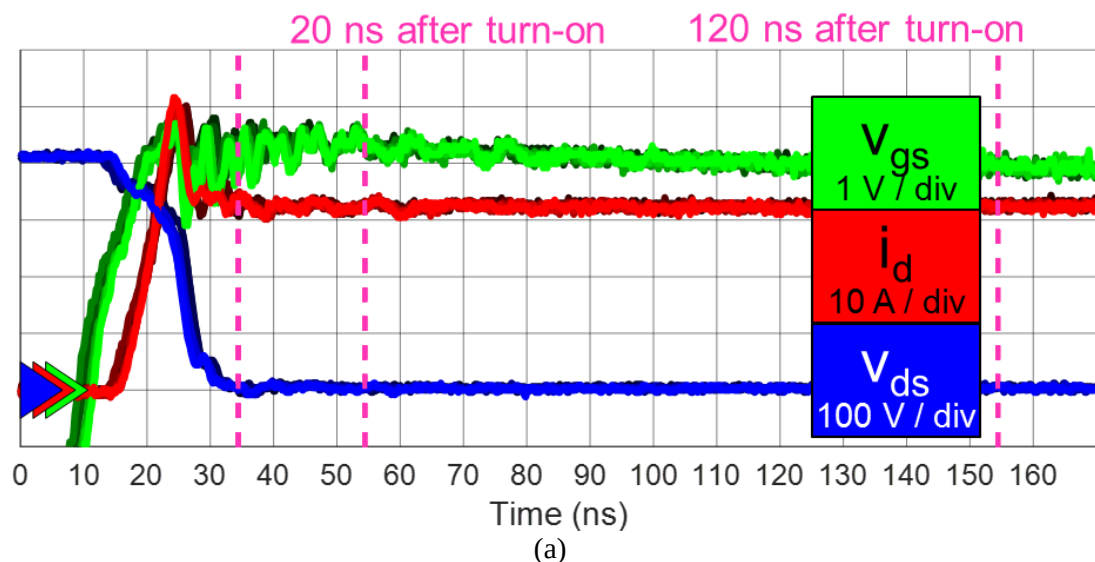


Figure 7.3.  $I_d$ - $V_{gs}$  relationship from dynamic characterization (DPT) results of an Infineon GIT with  $I_{g,ss} = 25$  mA. (a) Turn-on waveforms for six temperatures 25-150 °C superimposed; (b) Gate voltages for six temperatures measured at 20 ns and 120 ns after turn-on transient end, averaged over a 10 ns interval in each case to minimize impact of noise.

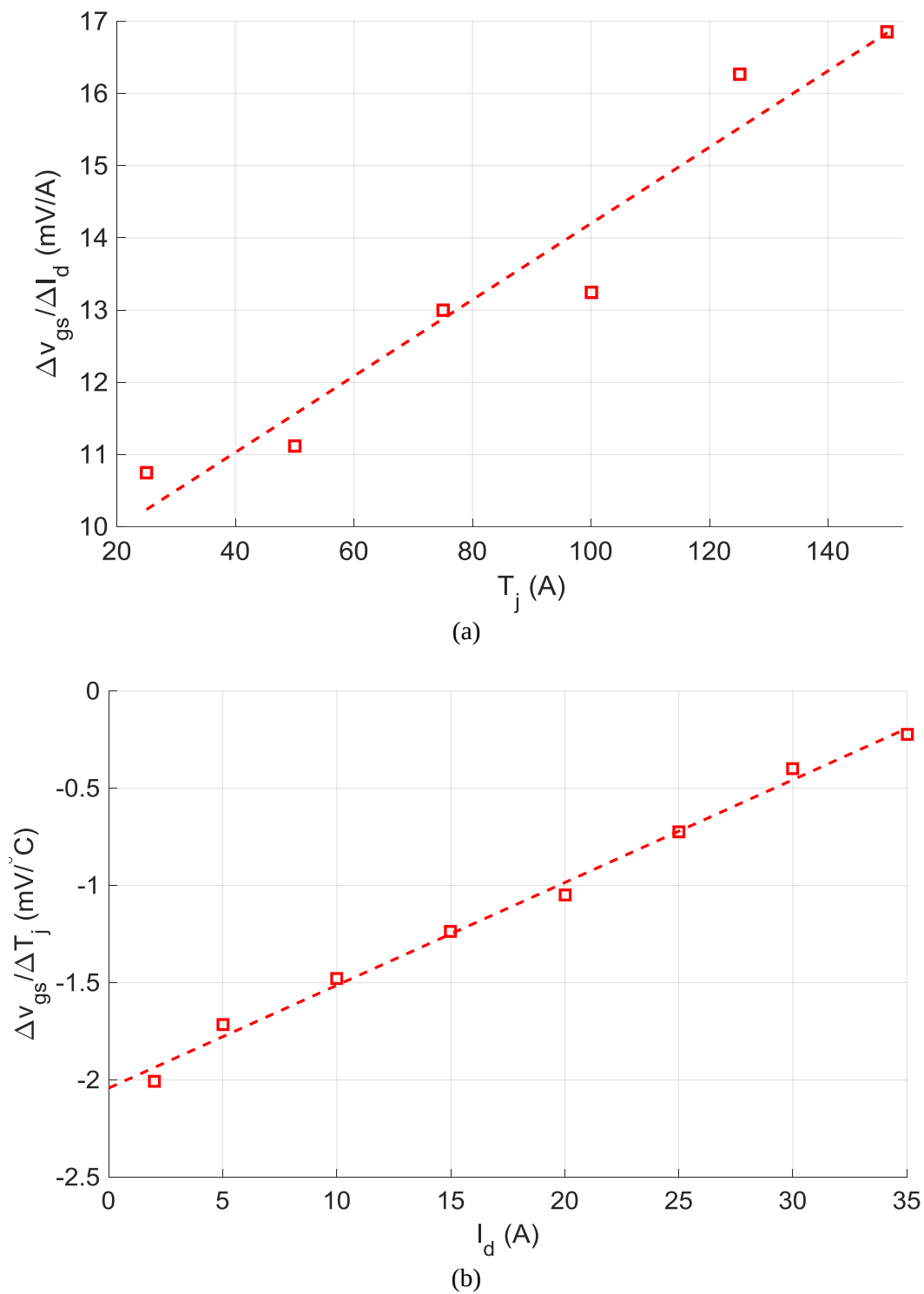


Figure 7.4.  $V_{gs}$  relationships with (a)  $I_d$  as a function of  $T_j$ , and (b)  $T_j$  as a function of  $I_d$ , from dynamic characterization (DPT) results of an Infineon GIT with  $I_{g,ss} = 25$  mA, measured at 120 ns after the turn-on transient end.

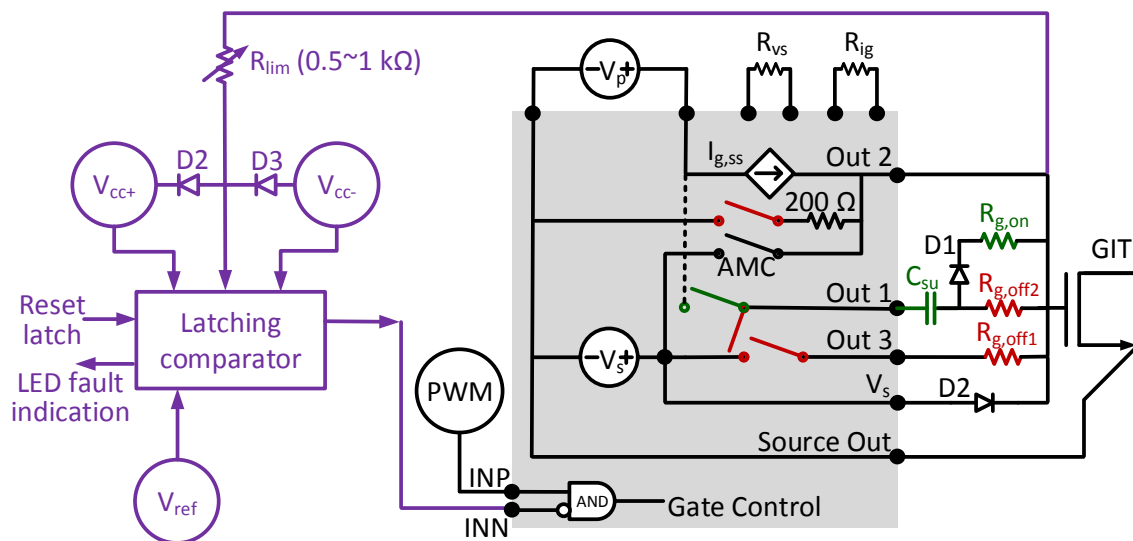


Figure 7.5. Schematic for first implementation of overcurrent protection circuit.

- An RC circuit at the buffered gate output, used to provide blanking time by filtering out any noise, spikes, and the gate overshoot experienced during the turn-on transient. In this implementation, the capacitance is provided by the diodes D2 and D3, which are PD3S160 from Diodes, Incorporated. These diodes also act to protect the comparator input from potential spikes in gate voltage, and also add  $\sim 80$  pF of filtering capacitance to the  $v_{gs}$  sense node as shown in Figure 7.6.
- A latching comparator (LT1711 from Linear Technology), which detects whether the filtered gate voltage is above a predefined reference voltage  $V_{ref}$ , and latches to a low state.
- An AND gate to combine the PWM control input and the output of the comparator, which should be high-state (logical 1) in normal conditions with no overcurrent fault. In this implementation, the AND gate is provided internally by the Panasonic gate driver.
- A reference voltage,  $V_{ref}$ , which can be set with a resistor divider or an adjustable regulator on the voltage supplying the driver,  $V_p$ .

The response time of the protection circuit will be the sum of the blanking time, the propagation delays of the components in the circuit, and the turn-off time of the GIT itself. The

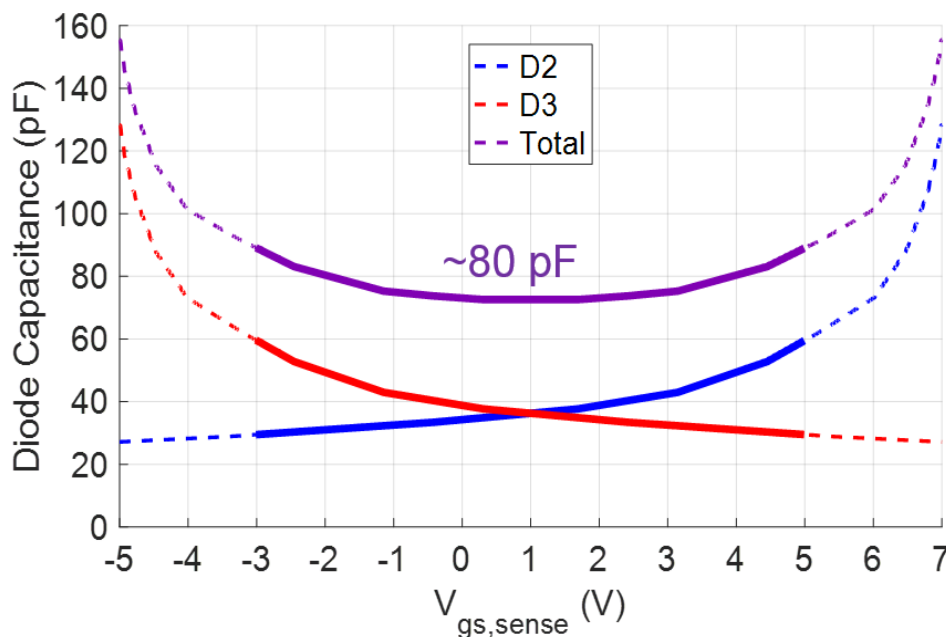


Figure 7.6. Effective filter capacitance added to  $v_{gs}$  sense node by diodes D2 and D3.

propagation delays of the comparator and driver are 11.5-15.5 ns and 32-47 ns respectively, indicating a total delay of 43.5 - 62.5 ns. Dynamic characterization of the Infineon GIT showed a total turn-off time of 12 ns with 400 V bus voltage and 30 A load current, using an off-state driving voltage of -3 V and 0  $\Omega$  turn-off gate resistance. This turn-off time includes the turn-off delay and the current fall time, which both decrease at higher load current, so 12 ns can be considered the worst-case for the likely protection threshold above the 30 A rating of the device. Taking into account the propagation delay of the circuit and the turn-off time of the GIT, the total response time of the protection circuit is estimated to be less than 80 ns, plus the blanking time, with a protection threshold greater than 30 A.

The blanking time and threshold voltage selection present a tradeoff that will depend on the experimentally selected gate driver circuit parameters and the slew rate of the fault current ( $di/dt$ ). This slew rate will depend on the exact circumstances of the overcurrent fault, which in this case is assumed to be an inductive overcurrent condition. For a shoot-through fault in which

one device is suddenly replaced by a short circuit (i.e. the device terminal have been shorted together),  $di_d/dt$  will be primarily limited by the power loop inductance and dc bus voltage, which is likely the worst case. For example, an overlap-induced shoot-through failure at 400 V with a loop inductance of 10 nH could reach a current slew rate as high a 40 A/ns. However, the much more likely case is that a PWM overlap occurs due to failure in the DSP, isolation, or gate driver. In this case, the highest  $di_d/dt$  will be equivalent to the  $di_d/dt$  that occurs during a normal turn-on current rise time, which can be in the range of 5-10 A/ns according to

$$\frac{di_d}{dt} \approx g_{fs} \frac{dv_{gs}}{dt} . \quad (7.3)$$

### 7.5 Short-circuit protection circuit design

In order to protect the GIT from short-circuit overcurrent faults, it was necessary to implement a soft turn-off (STO) function to reduce the gate voltage more slowly than the gate driver's normal turn-off speed. Turning off the GIT too quickly in a short-circuit fault condition may cause a high drain voltage overshoot that destroys it from overvoltage rather than overcurrent. This STO function is typically accomplished with a MOSFET connected between the gate terminal and the off-state driving voltage  $V_s$ , combined with a larger gate resistor and/or capacitor to slow down the turn-off speed [102],[103],[249]. The soft turn-off function shown in Figure 7.7 simplifies this circuit by eliminating the need for passive components. The speed of the turn-off is controlled instead by the MOSFET itself, which is operated in the saturation region to provide a fixed quantity of current to bring the gate voltage down slowly. As shown, the source of this STO MOSFET is connected to  $V_s$ , and its gate voltage is controlled by a NAND gate driven by the comparator output. This NAND gate (SN74LVC1G00 from TI) outputs a voltage  $V_{cc}$  (-5 V in this case) during normal operation, and 0 V when a fault occurs. Referenced to  $V_s$  (which in this case is -3 V), the STO MOSFET's  $V_{gs}$  is therefore -2 V during normal operation and 3 V when a fault occurs. SSM3K15AMFV from Toshiba was selected as the STO MOSFET, based on its transfer

characteristic. This MOSFET has a threshold voltage of 0.8-1.5 V, and provides 300 mA of drain current when operated in saturation with  $V_{gs} = 3$  V from 25 to 100 °C. The positive supply voltage of the NAND gate was initially designed to be adjustable. If another MOSFET is used, or a different GIT is being protected by the circuit, the direct utilization of 0 V for the positive NAND gate supply may not be effective, and this voltage may need to be provided by another regulator. However, in this case SSM3K15AMFV at  $V_{gs} = 3$  V was confirmed to turn off the faulted GIT slowly enough to prevent catastrophic drain overvoltage.

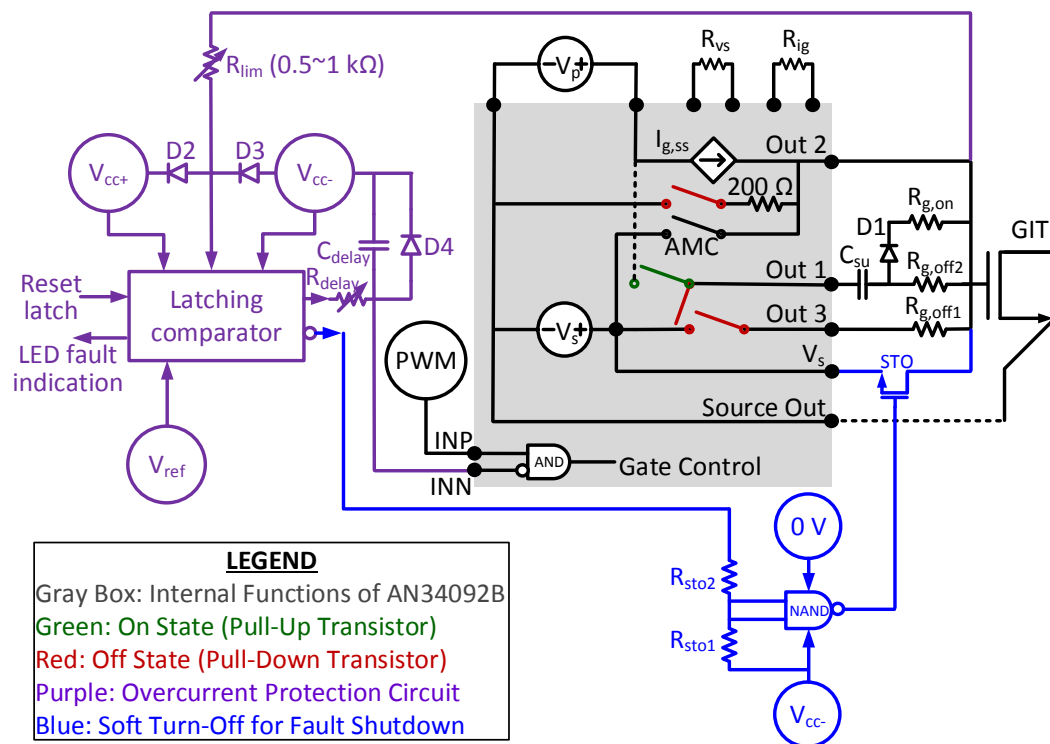
The STO MOSFET must draw enough current to slowly bring down the faulted GIT's gate voltage, but it must also absorb the steady-state current provided by the gate driver IC (25 mA in this case). To prevent damage to this MOSFET, this current must be terminated at some time after the STO triggers. The overcurrent detection comparator provides a delayed output that turns off the gate driver IC as previously implemented in Figure 7.5. This delay must be long enough to allow the STO function to complete, and was set as  $\sim 200$  ns in this implementation.

In the experimentally implemented version shown in Figure 7.7 (a), this circuit is fully isolated and referenced only to the source voltage of the protected device. The fault is visibly indicated using an LED driven at the comparator output, and a reset function is provided by a button connected to the latch pin of the comparator. Figure 7.7 (b) shows a variation of this circuit that is recommended for implementation in an operating converter. The STO function remains, but the delayed driver turn-off function is provided by a digitally isolated connection to the control DSP. The fault indication and reset functions are also provided by an isolated DSP link.

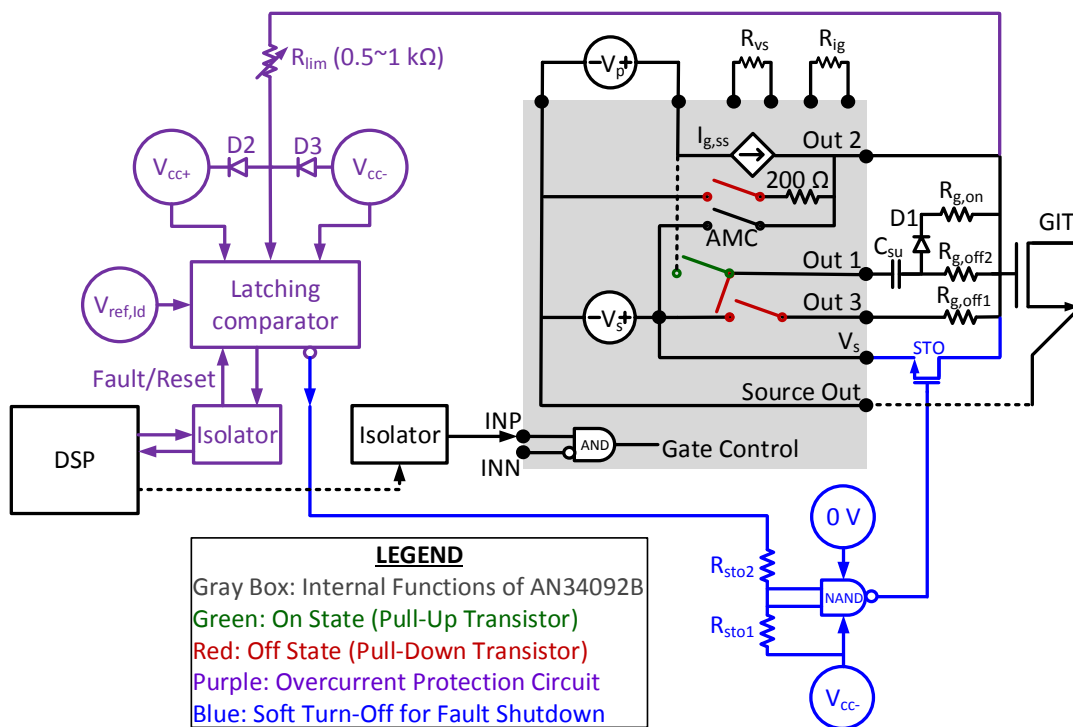
## 7.6 *Advantages of this protection scheme*

Compared with conventional desaturation protection, the proposed circuit has three main advantages:





(a)



(b)

Figure 7.7. Schematic for short-circuit protection circuit, including (a) version implemented for experimental verification, and (b) version recommended for converter implementation.

- 1) The first is response time, owing in part to the lack of any diodes that must turn on before the protection can be triggered. No sensing diodes are required in this case, because the voltage being sensed will always be in the range of  $\pm 5$  V. The ringing that results from the diode changing state is a major cause for increased blanking time and noise immunity concerns. Noise immunity concerns and excessive blanking time can therefore be avoided by sensing this relatively stable gate voltage instead of drain voltage.
- 2) The second is minimal impact on switching speed or loss. Desaturation protection adds capacitive loading in parallel with  $C_{oss}$ , which slows down the switching transient and adds loss. The only potential capacitive loading in the proposed circuit is the input impedance of the op-amp buffer circuit, applied in parallel with  $C_{gs}$ , which should have a negligible impact on driving loss and switching speed. However, any impact it does cause on switching speed can easily be compensated by tuning the parameters of the driving circuit ( $V_p$ ,  $V_s$ ,  $R_{g,on}$ ,  $R_{g,off}$ ,  $C_{su}$ ). The limiting factor for switching speed in the GIT is the rating for peak gate current, or other circuit consequences such as  $v_{ds}$  overvoltage or parasitic ringing, so there should generally be flexibility in tuning the driving circuit parameters to compensate for the loading of the buffer circuit.
- 3) The third advantage is the freedom to select any maximum current threshold, independent of the gate driver design or temperature. For desaturation protection, the maximum current is the saturation current at the selected driving voltage, so the converter designer must choose between faster switching (high gate voltage) or faster protection (low gate voltage). The desaturation current threshold that results from this selected gate voltage is highly sensitive to temperature, whereas this  $v_{gs}$ -based overcurrent threshold is nearly invariant to temperature in the range of interest (30-40 A).

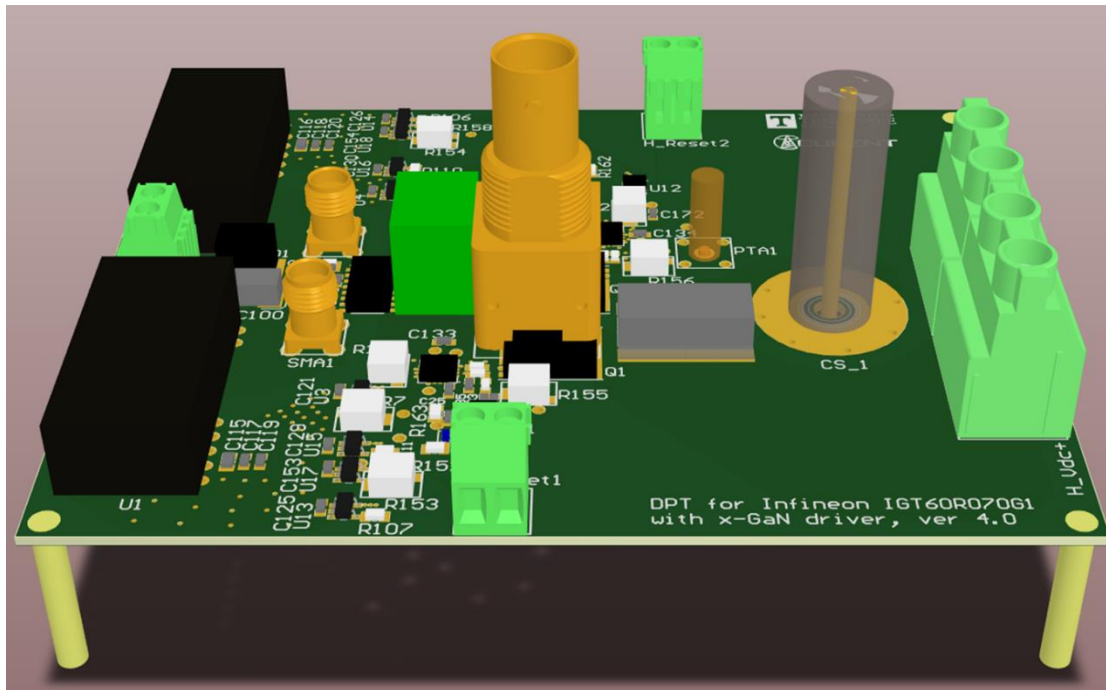
### 7.7 Test setup for experimental verification

The circuits shown in Figure 7.5 and Figure 7.7 (a) were both implemented in double pulse test (DPT) boards to verify their effectiveness in protecting a GIT in an inductive load overcurrent fault and a short-circuit fault, respectively. The overcurrent protection board from Figure 7.5 was constructed first, and verified at 400 V and 25 °C with a variety of load inductor sizes to adjust the current ramp rate  $di_d/dt$ . Next, the short-circuit protection board from Figure 7.7 (a) was constructed. Figure 7.8 shows a 3d model of this second test board. The components added to the existing DPT board design to implement the protection functions are highlighted, including regulators, comparators, soft turn-off circuits, passives, and connectors for reset buttons. The current-limiting resistor was selected at 1 k $\Omega$  for the first version of the circuit, resulting in a blanking time constant of 80 ns. For the short-circuit protection circuit,  $R_{lim}$  was reduced to 0.5 k $\Omega$  for a blanking time constant of 40 ns. In both boards, the reference voltage  $V_{ref,id}$  was selected as 3.8 V to correspond to the desired fault current threshold of 30-40 A.

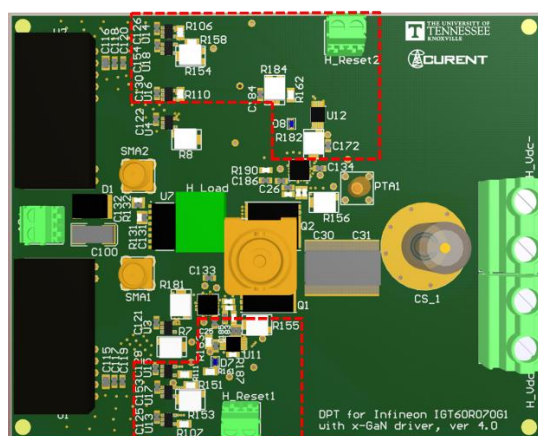
Figure 7.9 shows the test setup used for short-circuit fault testing, and a similar setup was used for the prior testing of inductive load overcurrent fault protection. The drain current, drain voltage, and gate voltage were measured using the same methodology used for DPT described in Chapter 4. Gate drivers were controlled using a benchtop dc power supply and a function generator, and the dc bus voltage was controlled by a second dc power supply with a common-mode choke and a dc bus capacitor bank. The junction temperature was controlled using a hot plate as described in Chapter 4, with the hot plate temperature chosen according to the  $T_j$ - $R_{ds,on}$  characterization of the device under test.

### 7.8 Results of inductive overcurrent testing

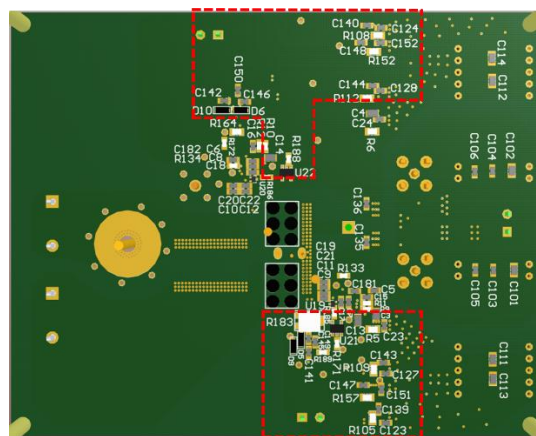
An example response to an inductive overcurrent fault is shown in Figure 7.10, with the highest test current ramp rate of 45 A/ $\mu$ s at 400 V and 25 °C. The response time was determined



(a)



(b)



(c)

Figure 7.8. DPT board used for experimental verification of short-circuit fault protection scheme. (a) Front view of assembled test board; (b) Top view of PCB with red boxes highlighting components added to DPT board for protection; (c) Bottom view of PCB with red boxes highlighting added components.

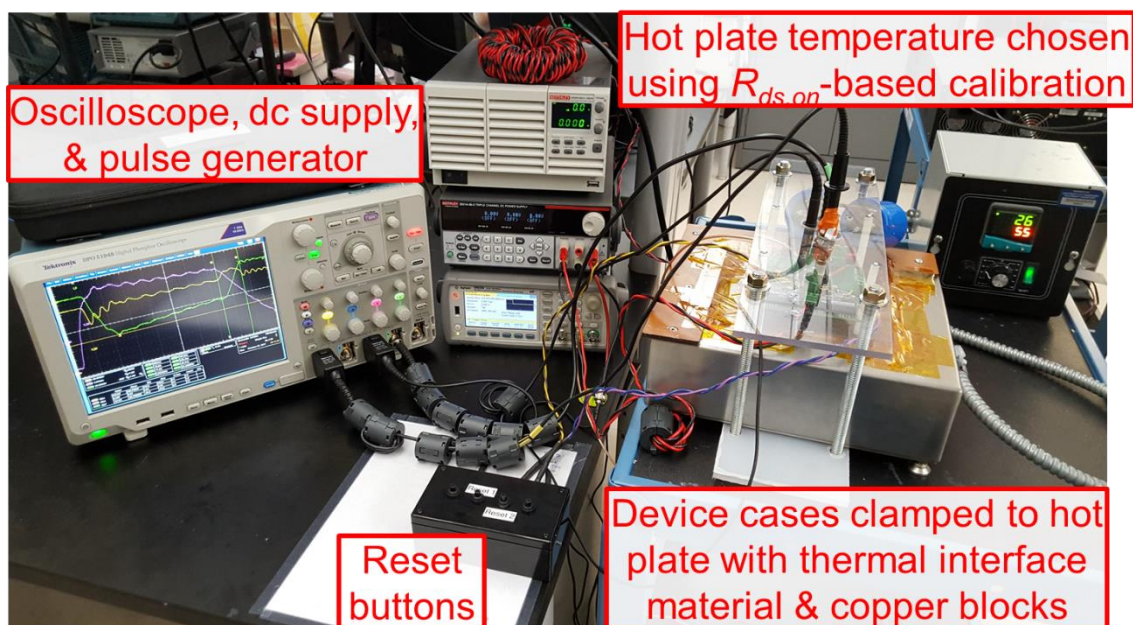


Figure 7.9. Test setup for experimental verification of short-circuit protection scheme, including junction temperature control with  $R_{ds,on}$ -calibrated hot plate.

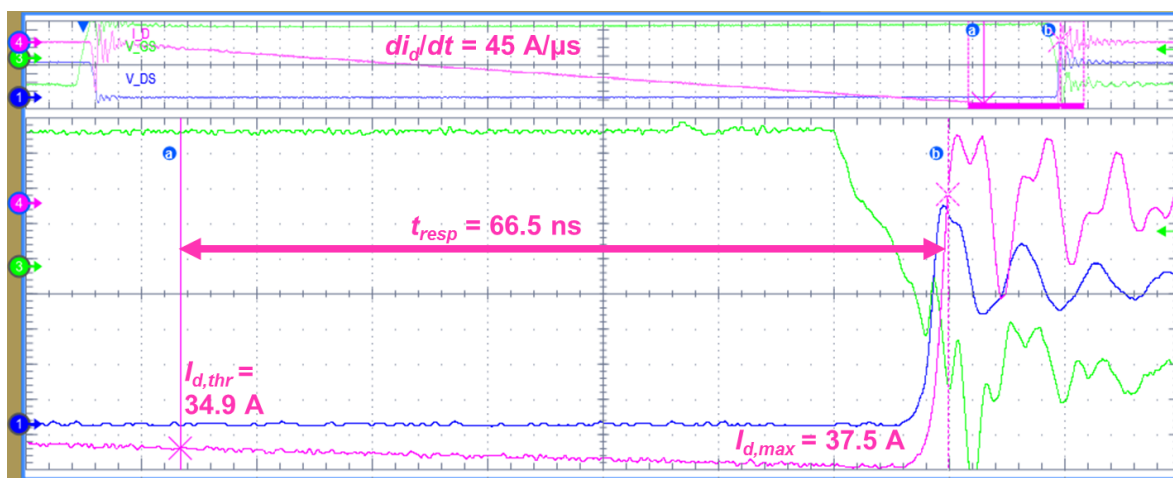


Figure 7.10. Waveform from inductive overcurrent fault test with  $45 \text{ A}/\mu\text{s}$  current ramp rate, at  $V_{dc} = 400 \text{ V}$  and  $T_j = 25 \text{ }^\circ\text{C}$ , with a fault threshold of  $V_{gs} = 3.8 \text{ V}$ . (Drain current is shown inverted due to polarity of current shunt connection.)

by recording the longest single pulse that did not trigger the fault protection, and comparing it with the longest possible pulse when the fault protection was triggered. The threshold current was defined as the drain current reached during the longest single non-fault pulse, and then the maximum fault current was defined as the peak current in the faulted case. The current ramp rate was varied by replacing the load with different inductances, and the results for response time, threshold current, and maximum fault current are shown in Figure 7.11 and Figure 7.12. The response time appears to asymptotically approach  $\sim 60$  ns as the current ramp rate increases, which fits well with the expected propagation delay of 55 – 75 ns. With higher fault current ramp rates, the impact of filtering on the sensed  $v_{gs}$  becomes less significant, and the effective blanking time approaches 0 ns. In this case, the total response time is made up of only the propagation delays of the protection circuit. However, the more severe current ramp rates also allow for a higher maximum fault current, which can permit a dangerously high drain voltage overshoot. For this reason, higher current ramp rates were not tested until the soft turn-off function was implemented.

### 7.9 *Results of short-circuit testing*

The short-circuit detection circuit was implemented for both switches in the DPT phase leg. However, only the protection circuit for the lower switch was enabled, including the soft turn-off function and the delayed driver turn-off. The high-side circuit was configured to detect the overcurrent/short-circuit condition but not turn off the high-side switch. The low-side switch was treated as the device under test (DUT), while the high-side switch was only used to cause a short-circuit fault for the DUT.

The DUT was tested with two types of short-circuit faults: fault under load (FUL), in which the low-side switch turns on first, followed by the high-side switch; and hard-switching fault (HSF), in which the high-side switch turns on first, followed by the low-side switch. FUL and HSF tests

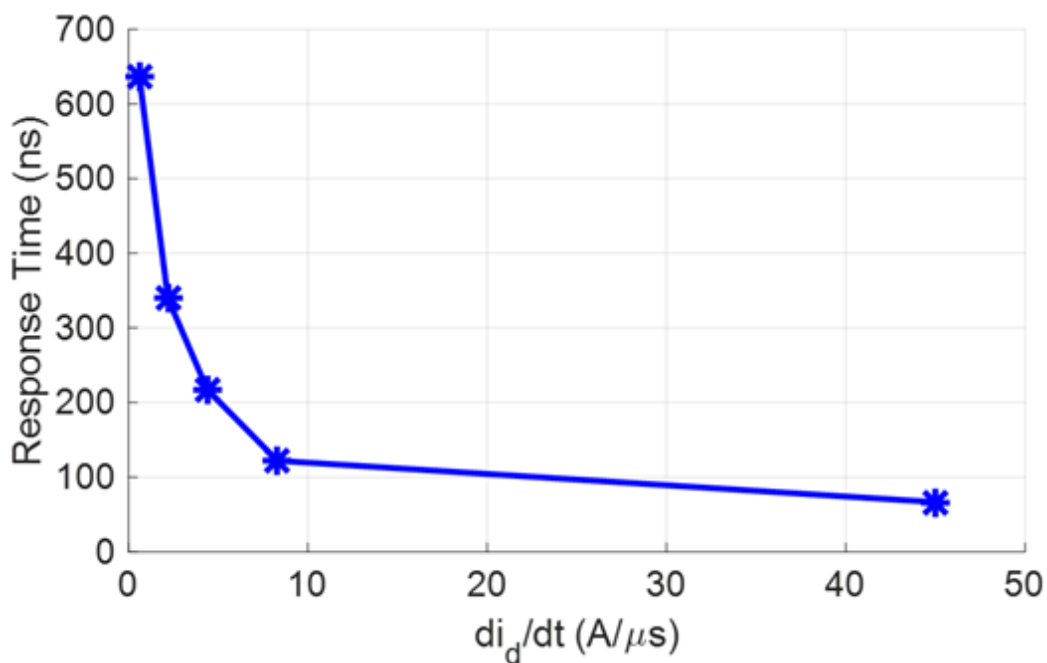


Figure 7.11. Protection circuit response time in an inductive overcurrent fault with varying current ramp rates, at  $V_{dc} = 400$  V and  $T_j = 25$  °C, with a fault threshold of  $V_{gs} = 3.8$  V.

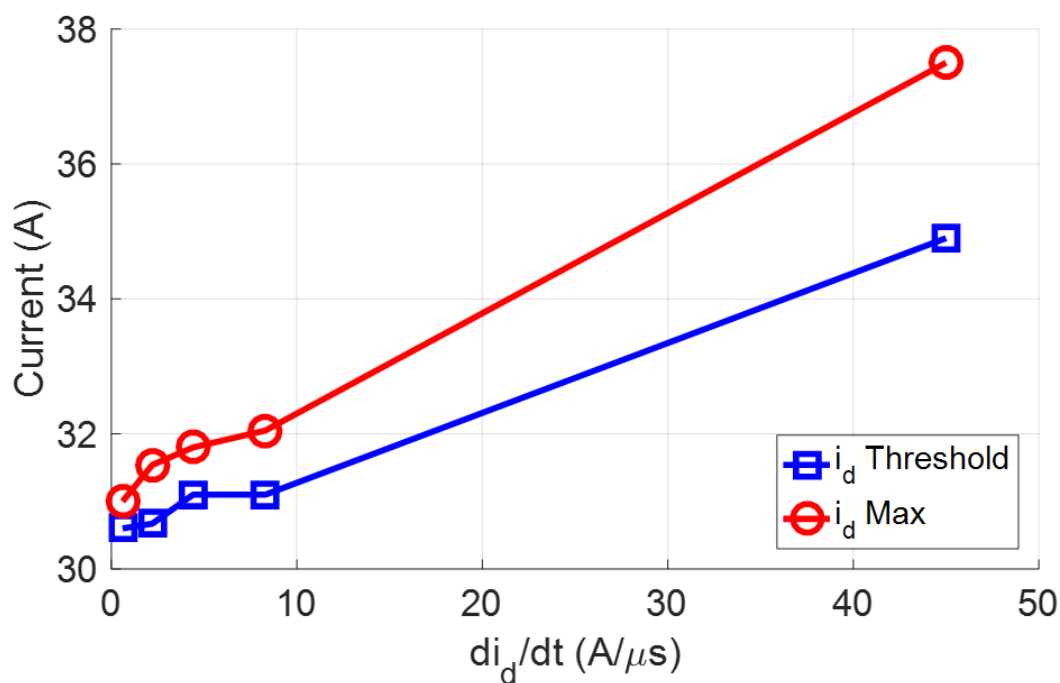


Figure 7.12. Overcurrent protection threshold current and maximum fault current, in an inductive overcurrent fault with varying current ramp rates, at  $V_{dc} = 400$  V and  $T_j = 25$  °C, with a fault threshold of  $V_{gs} = 3.8$  V.

were performed at 100 V, 200 V, 300 V, and 400 V at each temperature condition. Once a complete round of tests was performed at 25 °C, the temperature was raised in increments of 25 °C and re-tested. This process was repeated up to 125 °C, then the temperature was reduced in increments of 25 °C and tested again to confirm repeatability.

Example fault waveforms for each of these faults are shown in Figure 7.13 and Figure 7.14, at 400 V dc bus and 25 °C junction temperature. Appendix B shows the fault waveforms for the remaining test conditions. Using these results, the following parameters were calculated:

- Fault detection time, defined as the interval between  $i_d > 30$  A and the beginning of the soft turn-off, marked by a drop in  $v_{gs}$
- Soft turn-off time, defined as the interval between the drop in  $v_{gs}$  and the completion of fault protection when  $i_d = 0$  A
- Total fault response time, defined as the interval between  $i_d > 30$  A and  $i_d = 0$  A
- Peak short-circuit current, defined as the highest current reached during the fault
- Total fault energy, defined as the integral of  $P = i_d v_{ds}$  for the short-circuit fault interval
- Drain voltage overshoot, defined as the difference between peak  $v_{ds}$  that occurs during the soft turn-off and the bus voltage

These parameters are shown in Figure 7.15 - Figure 7.21 for the operating conditions tested. Solid lines in each figure show the tests performed with incremental 25 °C increases in junction temperature, and dashed line indicate the tests repeated with -25 °C steps. Comparison of solid and dashed lines demonstrates the repeatability of this testing.

As indicated in Figure 7.15, the detection time appears to increase with temperature. However, Figure 7.18 also indicates that the peak drain current decreases with temperature. A lower saturation current fits with the transfer characteristic measured over temperature in Chapter 4. This is also evidenced by the falling drain current during the fault itself, as channel self-heating occurs.



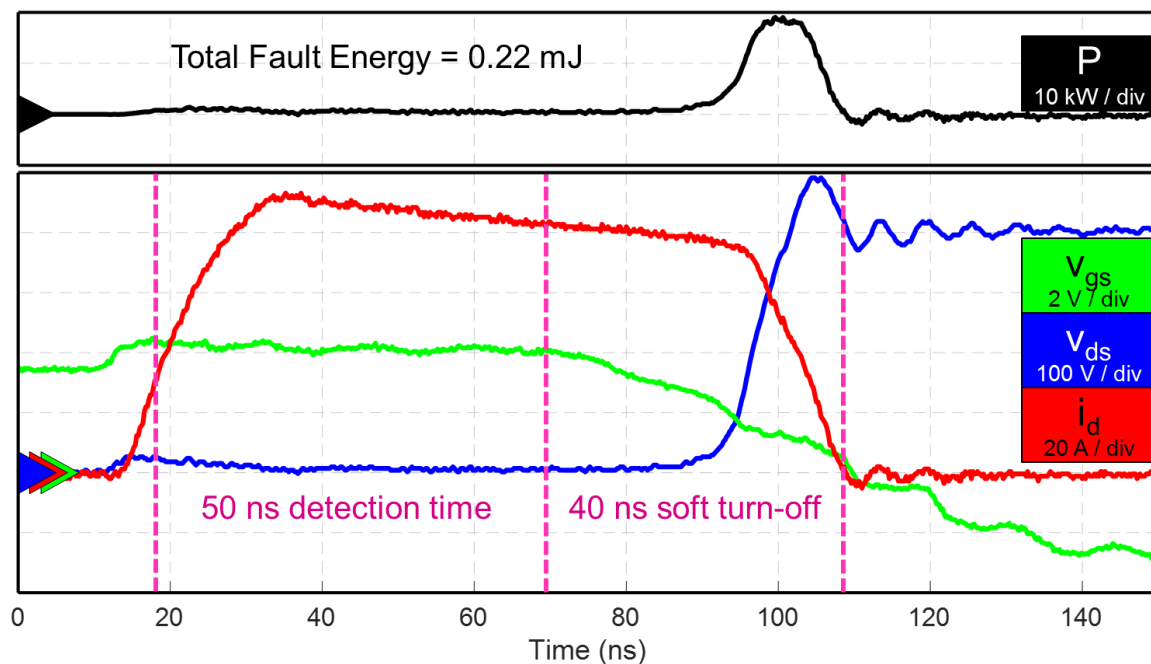


Figure 7.13. Waveform from a fault under load (FUL) short-circuit test at  $V_{dc} = 400$  V and  $T_j = 25$  °C, with a fault threshold of  $V_{gs} = 3.8$  V.

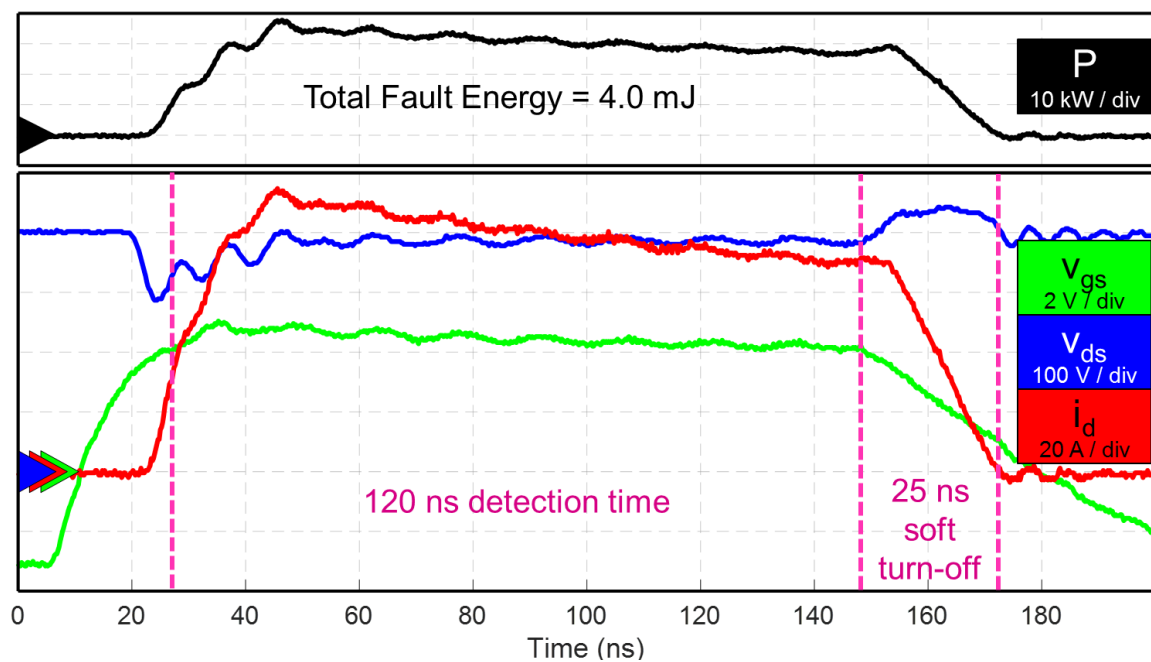


Figure 7.14. Waveform from a hard-switching fault (HSF) short-circuit test at  $V_{dc} = 400$  V and  $T_j = 25$  °C, with a fault threshold of  $V_{gs} = 3.8$  V.

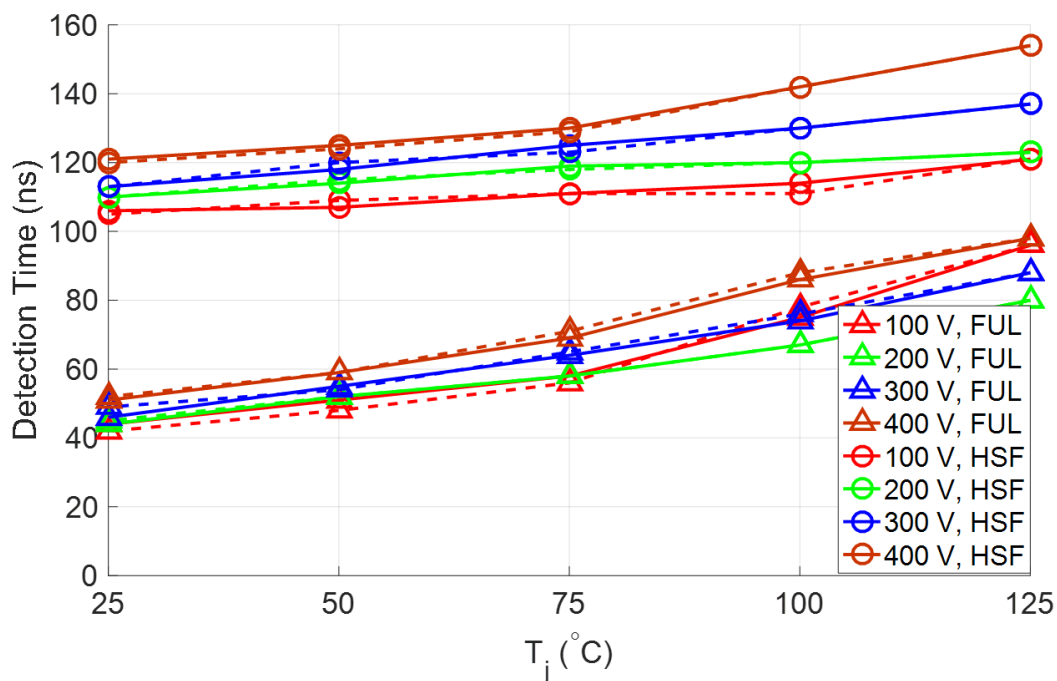


Figure 7.15. Fault detection time (from  $i_d > 30\text{ A}$  to drop in  $v_{gs}$ ) as a function of  $T_j$  and  $V_{dc}$ , in both fault under load (FUL) and hard-switching fault (HSF) conditions.

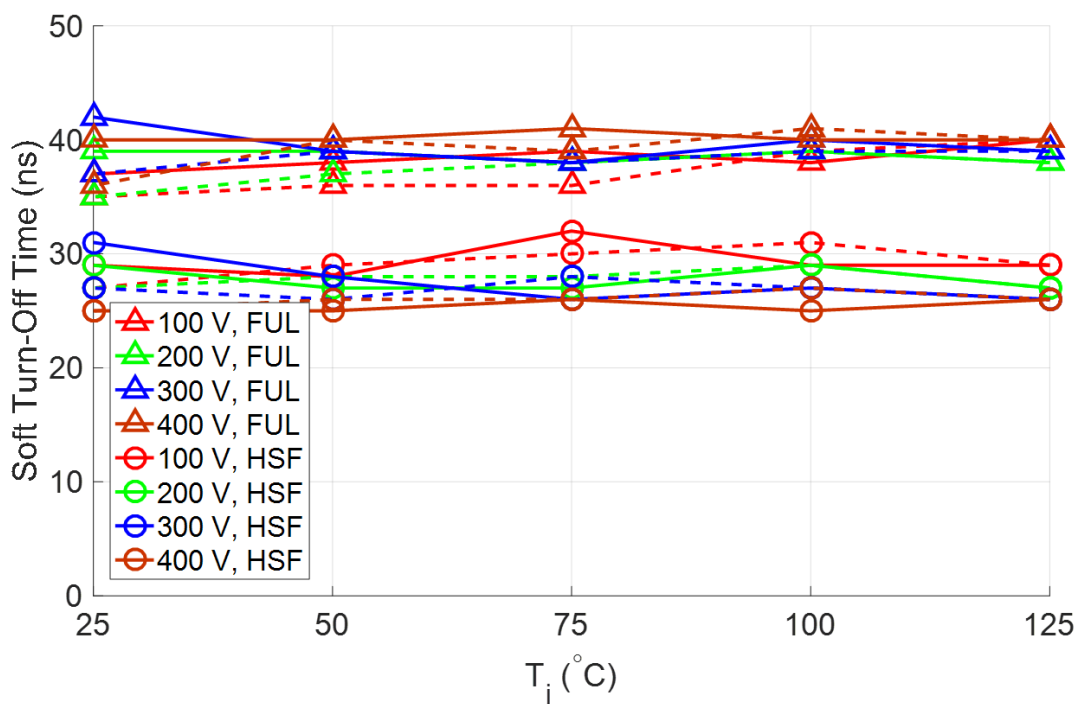


Figure 7.16. Soft turn-off time as a function of  $T_j$  and  $V_{dc}$ , in both fault under load (FUL) and hard-switching fault (HSF) conditions.

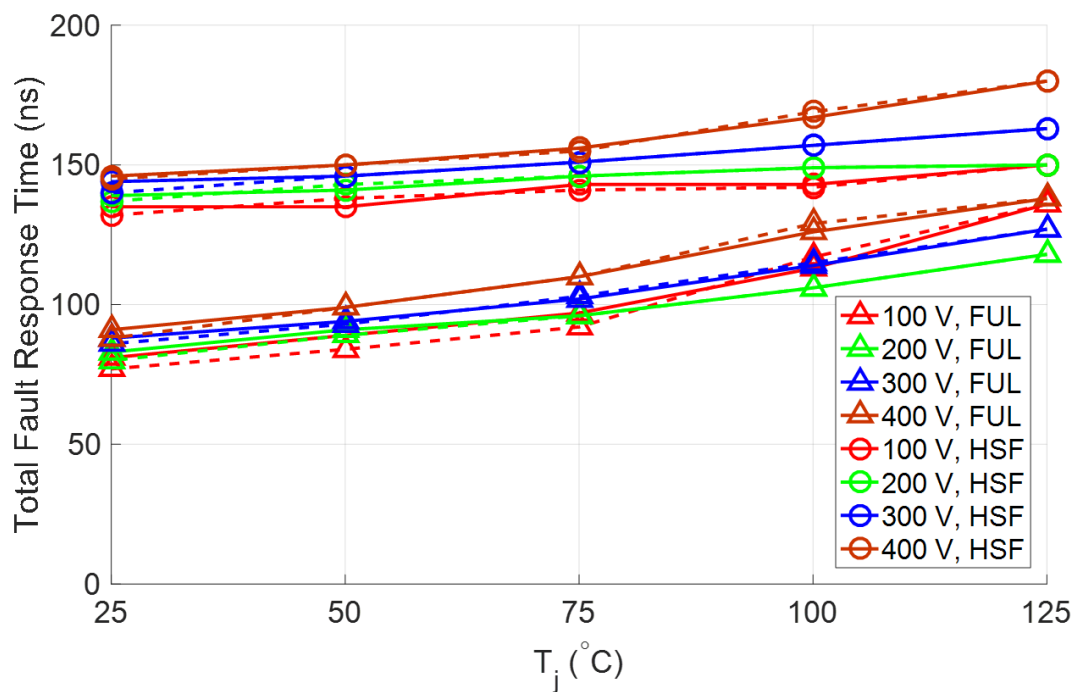


Figure 7.17. Total fault response time (from  $i_d > 30$  A to  $i_d = 0$ ) as a function of  $T_j$  and  $V_{dc}$ , in both fault under load (FUL) and hard-switching fault (HSF) conditions.

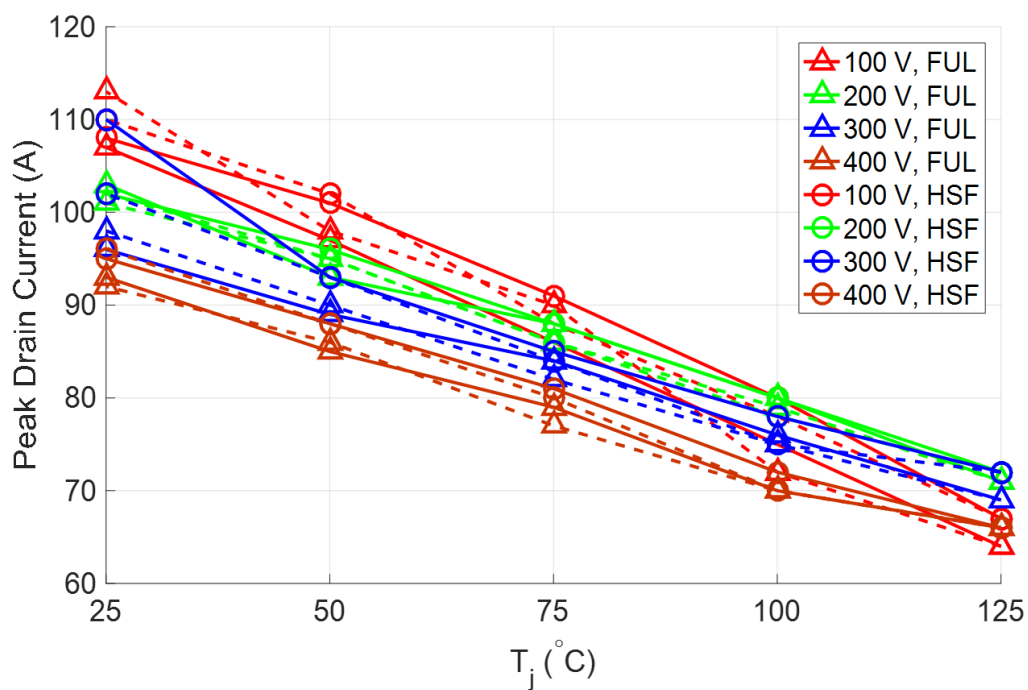


Figure 7.18. Peak short-circuit drain current as a function of  $T_j$  and  $V_{dc}$ , in both fault under load (FUL) and hard-switching fault (HSF) conditions.

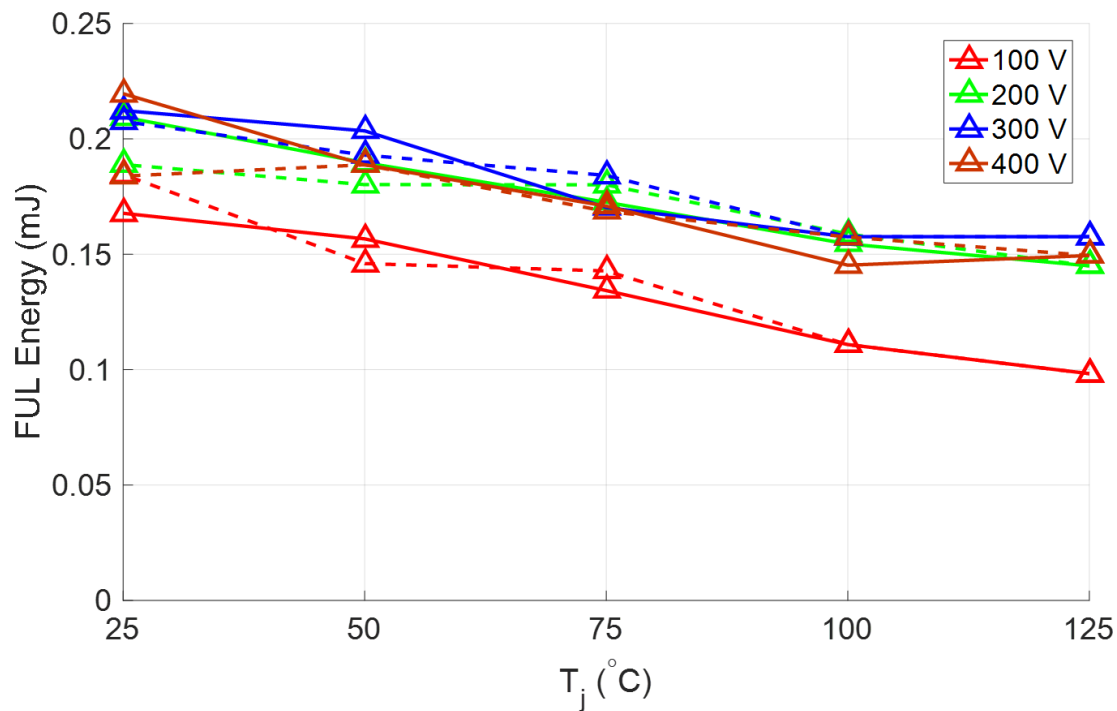


Figure 7.19. Total fault energy as a function of  $T_j$  and  $V_{dc}$ , in a fault under load (FUL).

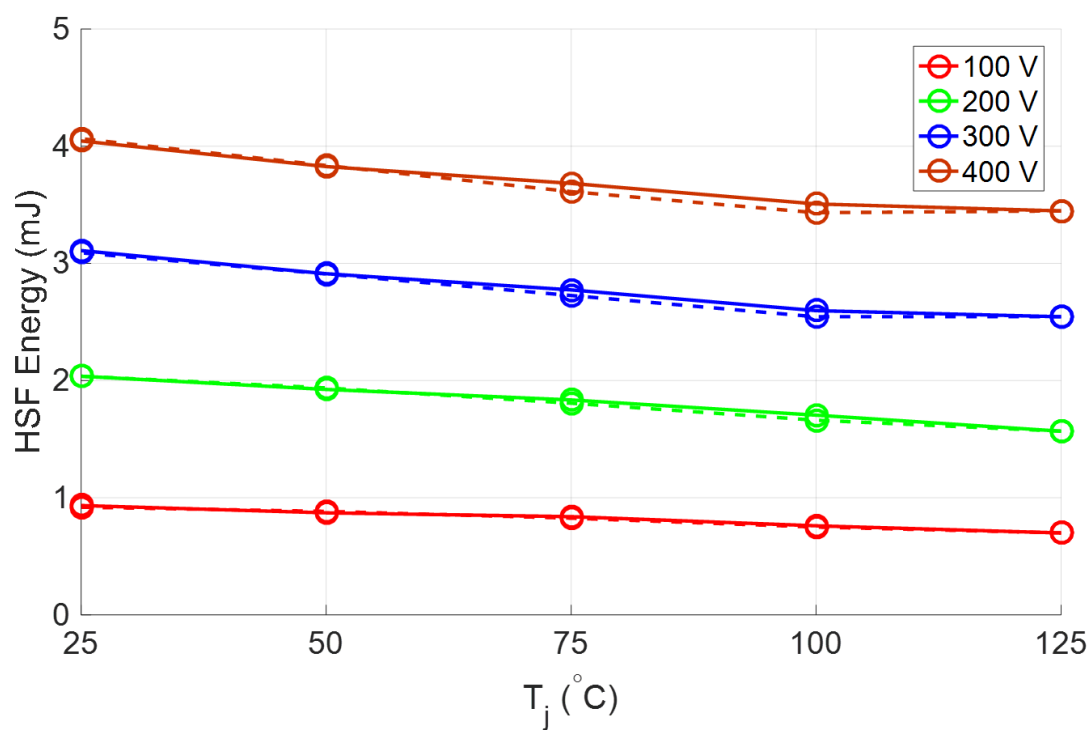


Figure 7.20. Total fault energy as a function of  $T_j$  and  $V_{dc}$ , in a hard-switching fault (HSF).

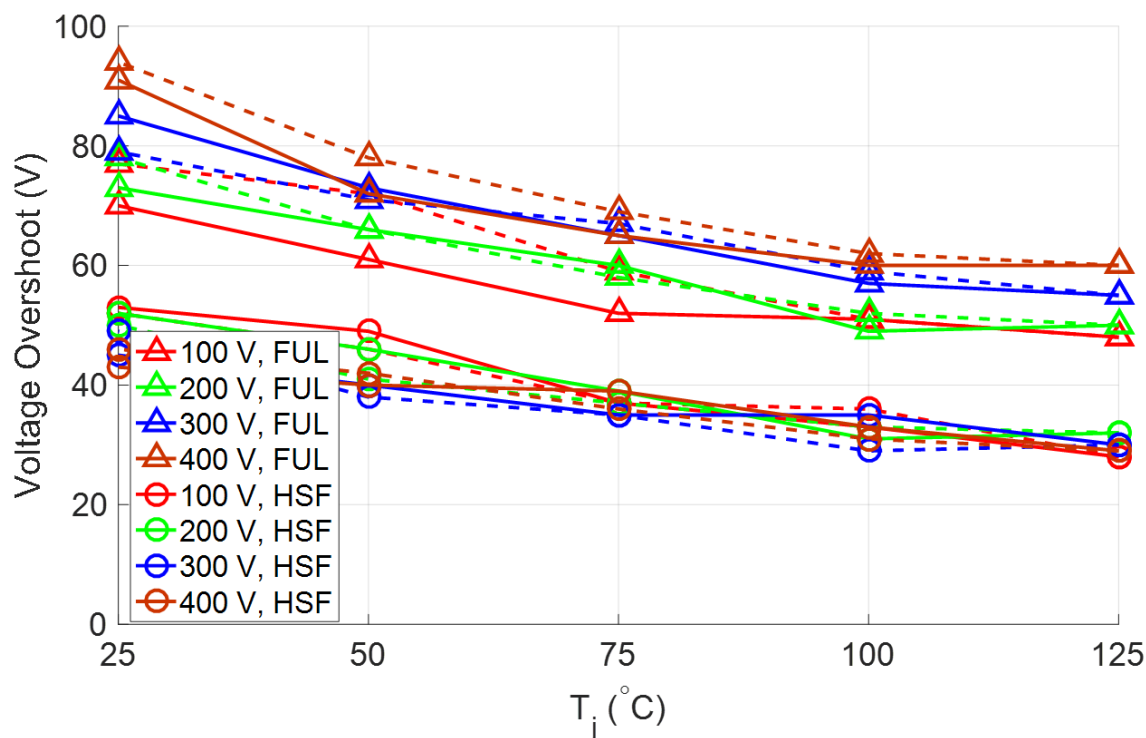


Figure 7.21. Peak drain voltage overshoot during soft turn-off, as a function of  $T_j$  and  $V_{dc}$ , in both fault under load (FUL) and hard-switching fault (HSF) conditions.

The short-circuit fault detection at higher temperature is slower because of the severity of the fault current, not directly a result of the elevated temperature. This can be seen more clearly in the trends of fault energy in Figure 7.19 and Figure 7.20. These trends show a relatively temperature-invariant fault response, with a slight reduction in fault energy at higher temperature. This is a desirable feature, since prior literature has explained that GaN devices have a lower critical fault energy at higher temperature [93],[96].

It is less desirable that the HSF fault energy increases almost linearly with bus voltage. However, it is worth noting that the high-side fault detection was triggered each time that a HSF was caused for the low-side switch. This is because a HSF for one switch in a phase leg is also a FUL for its complementary switch, as long as both devices are healthy at that time. When a FUL was generated on the low-side switch, the high-side switch never triggered for any of the operating

conditions tested. This indicates that implementing the protection circuit on both switches in a phase leg may prevent either switch from ever experiencing the longer fault duration and higher energy of a HSF fault. Once either switch turns off, the short circuit condition is ended.

#### 7.10 *Experimental measurement of fault threshold over temperature*

Next, the test board was verified to function normally when operated below the fault threshold. This test was performed by sending multiple pulses to the low-side switch in an inductive load configuration, as in a typical DPT. In this configuration, each hard-switching pulse occurs at a higher load current, verifying the circuit's immunity to successive hard-switching transient noise at each current level. Finally, when the protection circuit trips, this current was identified at the fault threshold. Figure 7.22 shows an example waveform from a test at 400 V and 25 °C, and Figure 7.23 shows the resulting fault current thresholds over varying bus voltage and junction temperature. It is evident from these results that the fault threshold is highly invariant to both temperature and bus voltage, while achieving strong noise immunity across the intended operating range.

This fault threshold testing was performed on the short-circuit protection circuit with a soft turn-off function, although the detection circuit is the same as in the inductive overcurrent protection version. However, the short-circuit protection circuit can effectively be used for both types of faults.

#### 7.11 *Impact of protection circuit on switching loss*

Both versions of the protection board were tested with the conventional DPT switching energy loss methodology described in Chapter 4, and compared with the previously captured switching energy loss for a similar board with no protection circuit. Figure 7.24 shows the total switching energy ( $E_{on} + E_{off}$ ) of DPT boards with and without the protection circuit. Comparisons of  $E_{on}$  and  $E_{off}$  are also separately compared in Figure 7.25 and Figure 7.26. The impact of adding the protection circuit is shown here to be negligible. The loading added to the gate node by the

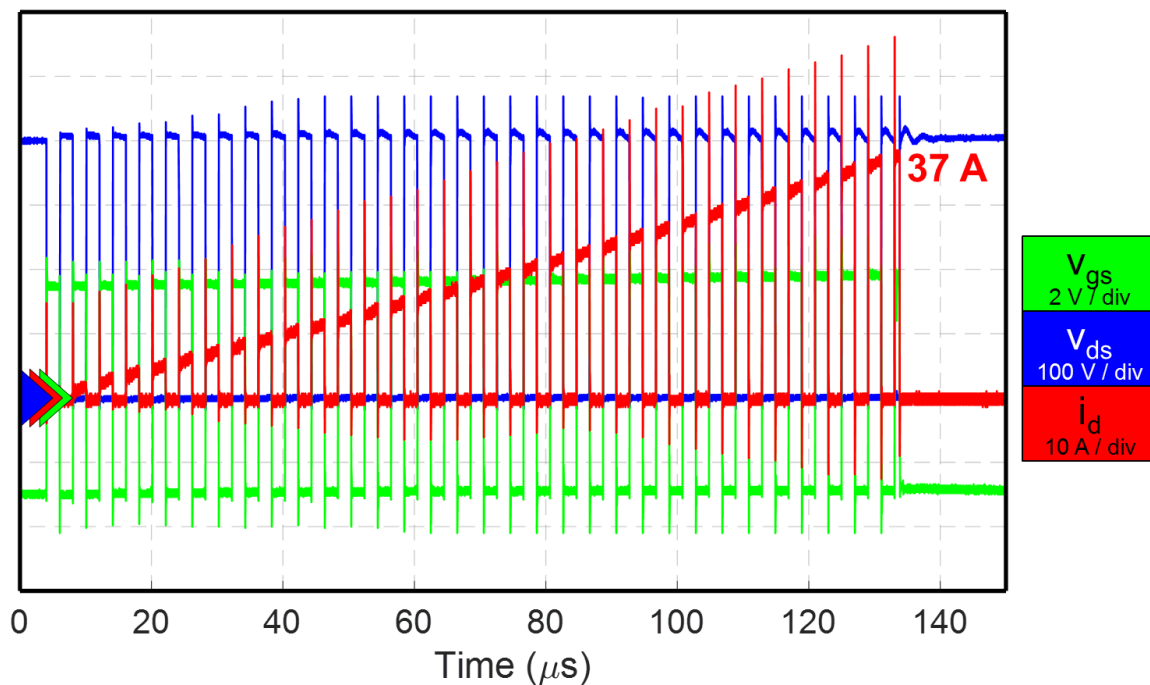


Figure 7.22. Multi-pulse inductive load test for fault threshold verification, at  $V_{dc} = 400$  V and  $T_j = 25$  °C, with a fault threshold of  $V_{gs} = 3.8$  V.

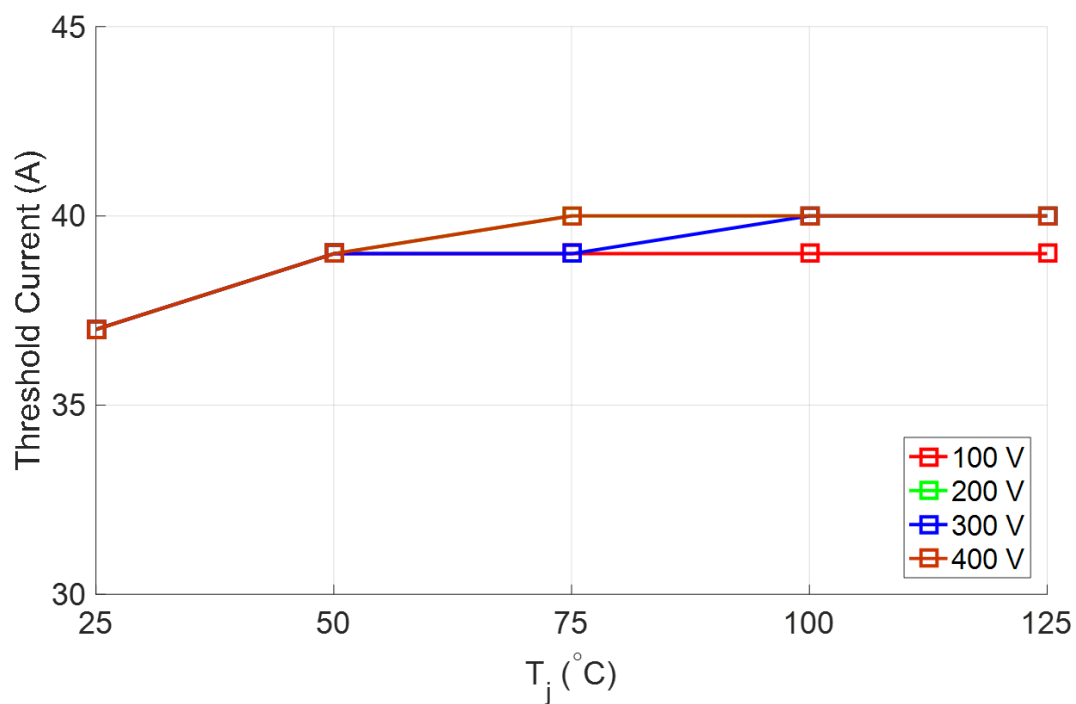


Figure 7.23. Fault threshold from multi-pulse inductive load testing, as a function of  $T_j$  and  $V_{dc}$ .

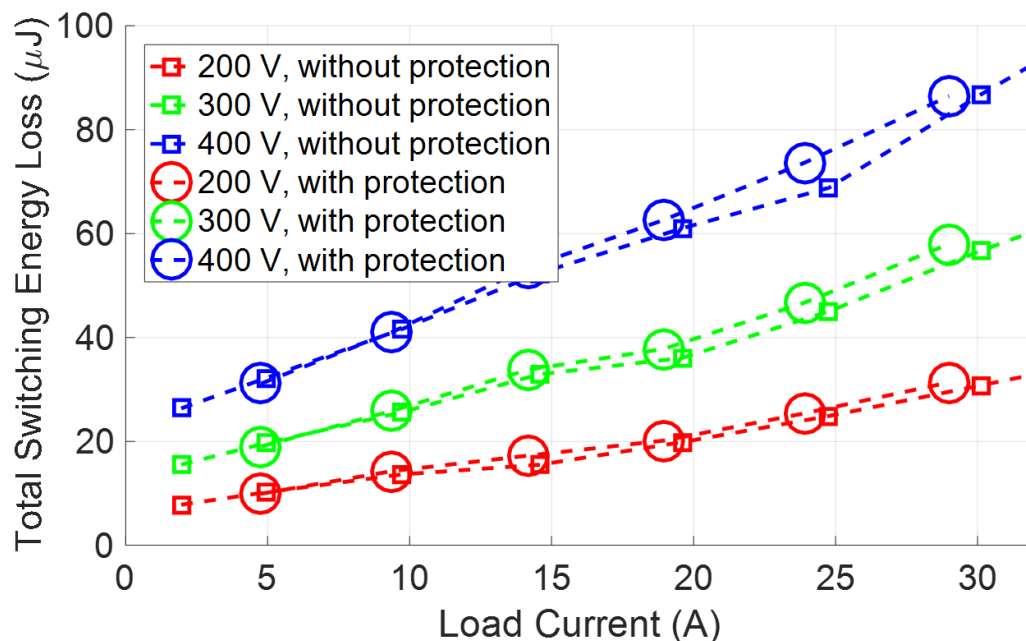


Figure 7.24. Total switching energy loss from inductive load DPT as a function of  $V_{dc}$  and  $I_L$  at  $T_j = 25^\circ\text{C}$ , using a DPT board with and without the fault protection circuit.

detection circuit was effectively limited by the  $0.5\text{ k}\Omega$  resistor. The turn-on energy does not appear to change at all with and without the protection circuit, and the impact on turn-off energy is only apparent in the 20-25 A range. If this slightly higher turn-off loss is considered too high for a particular application, the gate node loading could be reduced by increasing the current-limiting resistance higher than  $0.5\text{ k}\Omega$ , and the same blanking time could still be achieved by replacing D2 and D3 with diodes that have lower output capacitance.

### 7.12 Summary

The proposed protection scheme was experimentally verified to turn off affected switches during an inductive overcurrent fault or a short-circuit fault, across the recommended operated temperature and voltage of an Infineon GIT, driven by a Panasonic x-GaN driver IC. The scheme can theoretically be implemented for other GITs (different manufacturers, voltage ratings, die sizes) as long as they are driven by a current-mode gate driver in turn-on steady-state. The fault energy, response time, and temperature invariance will be affected by these changes. The gate driver itself



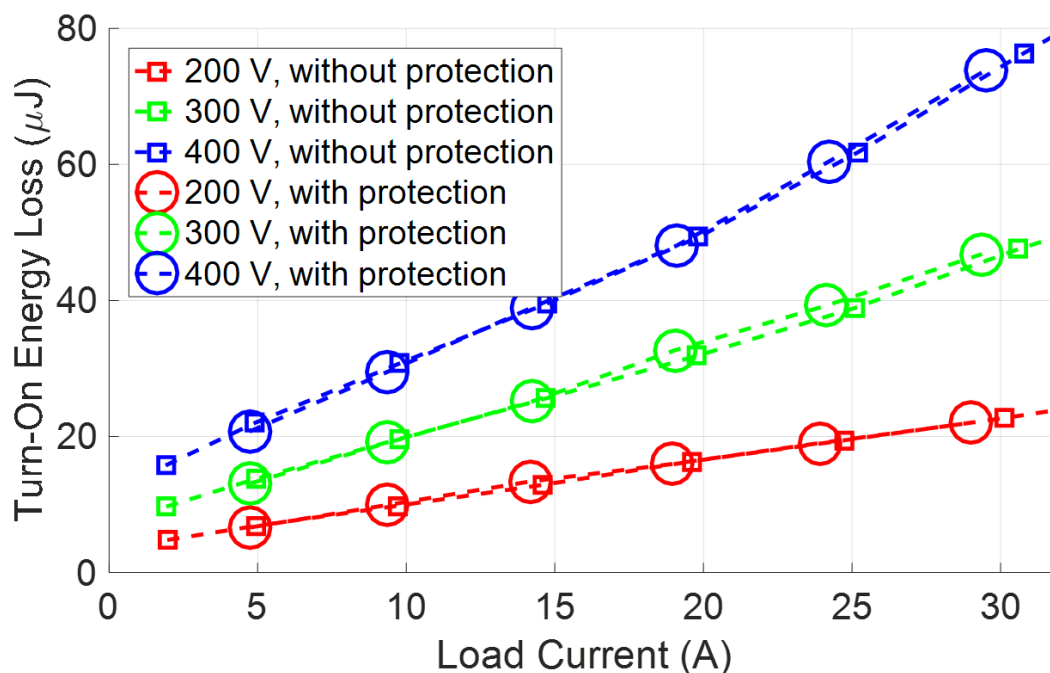


Figure 7.25. Turn-on switching energy loss from inductive load DPT as a function of  $V_{dc}$  and  $I_L$  at  $T_j = 25^\circ\text{C}$ , using a DPT board with and without the fault protection circuit.

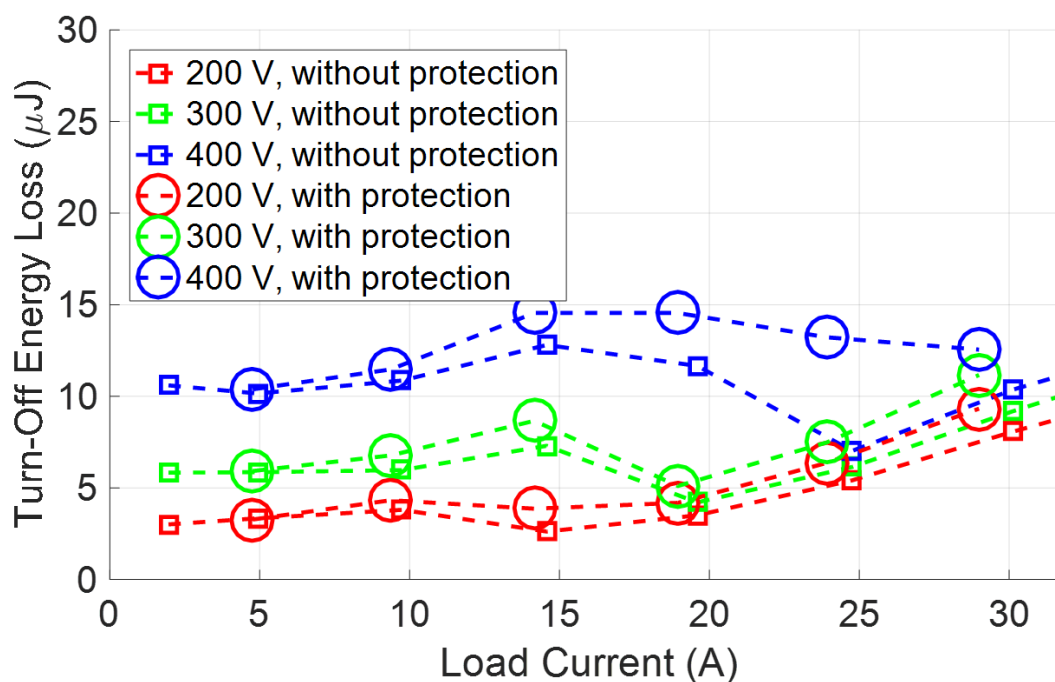


Figure 7.26. Turn-off switching energy loss from inductive load DPT as a function of  $V_{dc}$  and  $I_L$  at  $T_j = 25^\circ\text{C}$ , using a DPT board with and without the fault protection circuit.

plays a strong role in the effectiveness of the scheme. The driver appeared to clamp the gate voltage at a relatively low voltage ( $\sim 5$  V) during a short circuit, whereas another driver could potentially allow  $v_{gs}$  to increase until it reaches the dynamic driving voltage (10 V in this case). This could be much worse for the fault energy of the device, because it would allow a higher peak drain current. However, it would also reduce the detection time because of the higher gate voltage. The performance of this scheme in any other combination of gate driver and GIT would require further study to verify.

The detection time could be reduced by decreasing the current-limiting resistance lower than 0.5 k $\Omega$ , but this impacts the noise immunity during normal operating near the fault threshold current. Likewise, the duration of the soft turn-off could easily be reduced by selecting a different STO MOSFET or adjusting the positive supply voltage of the NAND gate that drives it. However, the given STO time was chosen in order to limit the maximum drain voltage overshoot to less than 100 V, as confirmed in Figure 7.21. Therefore, the total fault response times shown in Figure 7.17 are the best case for this protection circuit with the chosen components and design constraints. The total fault response time was measured as 70 – 180 ns across the full recommended operating temperature and voltage of the chosen GIT. Based on recent literature describing the short-circuit capability of GaN GITs and other GaN FETs, this response time should be sufficient to protect the device from destruction, and possibly even prevent significant degradation. Although the short-circuit capability and related degradation were out of this scope of work, the results in Figure 7.13 - Figure 7.21 indicate that no significant degradation occurred. The devices experienced very similar fault behavior in the first round of short-circuit testing (with junction temperature increasing in 25 °C steps) and in the second round of testing (with junction temperature decreasing in 25 °C steps). The same pair of GITs was used for the all short-circuit tests, without noticeable changes in peak current or fault energy.

## Chapter 8

### Design of a Hard-Switching GaN-Based Converter with Reduced Voltage and Current Margins

#### 8.1 Introduction

A GaN-based inverter was proposed for potential photovoltaic (PV) applications, with the motivation to demonstrate the cost reduction that can be achieved by replacing conventional Si MOSFETs with GaN FETs in the design of a typical commercial product. The lower cost is expected to come from reduced filter requirements at higher switching frequency, while fully utilizing the GaN FETs by reducing the voltage and current margins without violating the device ratings. The scope of this chapter includes the design of the power stage, particularly the gate driver, power loop, and heatsink design. This work is also intended to improve the understanding of the impact factors that determine the voltage and current limitations for a GaN FET, which may be relevant to any hard-switching GaN-based converter. The methodologies presented in Chapter 4 and transient behavior model in Chapter 6 were applied here to reduce the voltage and current margins of commercially available GaN FETs.

#### 8.2 Design targets

The commercial PV inverter selected for a design basis is ABB UNO-3.0-TL-OUTD, a transformerless (non-isolated) converter with a 3.0 kVA rating, which includes both a dc-dc stage and a dc-ac stage. This work will focus on the dc-ac stage only, with the assumption that the dc-dc boost stage will be bypassed by a large diode when the dc input voltage is within the targeted voltage range of the inverter stage. The ratings and parameters targeted for this design were modified from the UNO-4.2 specifications by scaling up the power slightly to 5 kVA and reducing the maximum operating input voltage to 450 V. Table 8.1 gives the remainder of the target specifications of this design. The California Energy Commission's (CEC) weighted average

*Table 8.1. Design targets for proposed inverter*

| <b>Specification</b>                 | <b>Target</b>                           |
|--------------------------------------|-----------------------------------------|
| Output Power Rating                  | 5 kVA                                   |
| DC Input Voltage (operating)         | 350 V - 450 V                           |
| DC Input Voltage (maximum withstand) | 600 V                                   |
| AC Output Voltage                    | 210-250 Vrms, (230 Vrms nominal), 60 Hz |
| AC Output Current (Maximum)          | 24 Arms (34 Apk)                        |
| CEC Efficiency                       | > 97.0 %                                |
| Grid Current THD                     | < 3 %                                   |
| Cooling                              | Natural convection                      |
| Isolation                            | Transformerless                         |
| EMC Standards                        | FCC Part 15 Class B quasi-peak          |

efficiency was used to assess the efficiency of the proposed inverter and compare it with the commercial product. The stated CEC efficiency of UNO-3.0-TL-OUTD is 96.0%, but this was adjusted to 97.0% for this project for two reasons. First, the boost bypass diode was assumed to account for approximately 0.3% loss based on an approximate forward voltage of 0.9 V. Second, the UNO-3.0-TL-OUTD is specified for operation up to 45 °C without derating, and the datasheet does not clearly state the temperature at which the inverter achieves this 96.0% CEC efficiency. The prototype was therefore targeted for an efficiency of 97.0% at the ambient temperature of the available laboratory space (23-25 °C). The inverter was initially intended for operation up to 550 V dc input, but this rating was reduced to 450 V for the first phase of the project.

The filter design was required to meet the EMC quasi-peak standards of the FCC, and to limit the total harmonic distortion (THD) to 3% or less. Although the filter design is outside the scope of this work, an analysis of the filter requirements as a function of switching frequency identified 140 kHz as a good candidate for filter cost reduction (including line filter and EMI filter),

and this determined the switching frequency for the power stage design. The impact of higher switching frequency on device losses was also considered in this decision, although the switching losses are a relatively minor contribution to the overall loss of this inverter design.

The requirement for natural convection cooling is typical for commercial PV inverters, and it is a major limiting factor on the maximum allowable device loss, and consequently on the design goal of voltage and current margin reduction.

The topology was selected as a full-bridge single-phase hard-switched inverter, with a virtual ground connection between the dc mid-point and the capacitive mid-point of the first stage line filter. Figure 8.1 shows the topology used in this work. This virtual ground was necessary in order to comply with dc common-mode current requirements (so-called “residual current”). Similarly, the hybrid unipolar modulation scheme was selected to minimize the residual current. Both of these selections were beyond the scope of this work. However, the hybrid unipolar modulation has a significant impact on the thermal design of the inverter, because it distributes the switching and conduction loss unevenly. The low-side switches experience the majority of the conduction loss, while the high-side switches experience all of the hard-switching loss. These design choices were treated as constraints for the work described in this chapter.

### 8.3 *Limiting factors on operating voltage and current margins*

In order to meet the voltage and current targets for this design, the key limiting factors on peak load current and operating dc voltage were identified for this hard-switching GaN-based topology. The power device was selected as a GaN gate injection transistor (GIT) from Infineon, rated at 600 V. The continuous current rating is given by the manufacturer as 31 A at a case temperature of 25 °C, and 14 A at a case temperature of 125 °C. However, this is primarily determined by the maximum junction temperature of 150 °C. The pulsed safe operating area is specified in the datasheet as more than double this limit for 100  $\mu$ s or less (60 A and 35 A). It was

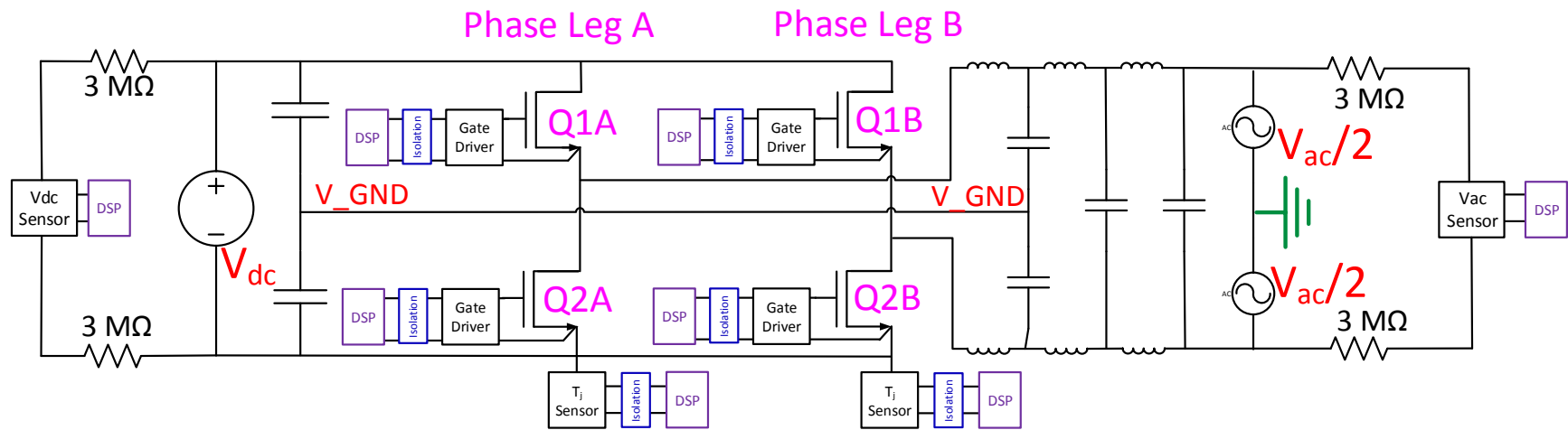


Figure 8.1. Topology of proposed full-bridge converter.

necessary to fully characterize the GIT in order to identify the factors that actually limit the operating voltage and current.

The first major factor is adhering to the absolute maximum 600 V rating of the device by limiting the overshoot voltages during switching transients. Achieving full utilization of the voltage and current rating therefore requires characterization of this overshoot voltage as a function of the operating voltage, current, and temperature, and design of a gate drive circuit to reduce the overshoot to an acceptable level within this range.

The second obstacle is the maximum junction temperature rating of 150 °C. The thermal design requirements were determined through detailed device loss modeling, and an improved thermal interface design for bottom-cooled GaN FETs was developed. After the inverter design was complete, a prototype was constructed for further characterization of its thermal performance and overall loss and efficiency.

#### 8.4 *Transient overshoot voltage limitation*

Relationships between peak overshoot voltage and other parameters were previously derived in Chapter 6. The key takeaway from that analysis was the difference between the overshoot voltage experienced by the active switch during a turn-off transient, and the overshoot experienced by the synchronous switch during a turn-on transient of the active switch. The turn-off transient overshoot is primarily related to the load current, although it can also be limited by decreasing the slew rate of the gate voltage ( $dv_{gs}/dt$ ), which increases overlap energy loss. Meanwhile, the turn-on overshoot voltage is not as sensitive to load current, and is in fact strongly related to the gate voltage speed  $dv_{gs}/dt$ . The capacitive gate drive circuit for the GIT applies a dynamic overdrive voltage, which can potentially result in a much higher overshoot voltage during the turn-on transient than in turn-off. The detailed relationships of these two overshoots to design choices and operating conditions were explored experimentally and analyzed to characterize this limitation.

### 8.4.1 *Static characterization of breakdown voltage*

The Infineon GIT used for this design is rated at 600 V, and remaining within this rating at all times is recommended to prevent lifetime degradation. However, it is also useful to further understand the behavior of the device when this voltage is exceeded, particularly over the rated operating temperature range. Figure 8.2 shows that this device experiences a drain-source leakage current that increases logarithmically as a function of voltage, so there is no clear “breakdown” voltage identifiable from this characterization. However, the leakage current also increases significantly as a function of junction temperature. It is important to remember that a GaN FET (including the GIT) has no avalanche breakdown mechanism, as previously discussed in Chapter 3. Rather, this leakage current is likely to cause time-dependent dielectric breakdown (TDDB), so it is difficult to ascertain a maximum allowable leakage current or drain-source voltage from this characteristic.

In Figure 8.3, the maximum allowable voltage is shown as a function of junction temperature, based on three arbitrarily selected maximum allowable leakage currents. From this curve, it is evident that the device is much more capable of withstanding higher voltage at room temperature than at elevated temperature. Even if the device is able to withstand higher than 600 V at room temperature, this may cause damage at a more realistic operating junction temperature of 100-150 °C. This work will therefore endeavor to keep the peak  $v_{ds}$  from exceeding the 600 V rating at any time, regardless of temperature.

### 8.4.2 *Consideration of loop inductance*

The overshoot voltage is primarily the product of  $di_d/dt$  and loop inductance  $L_{loop}$ . The loop inductance is determined by the parasitic inductance of the packaged devices and decoupling capacitors, along with the area encompassed in the power loop formed between them. The loop area was required to be laterally oriented because of the bottom-cooled thermal design. The total



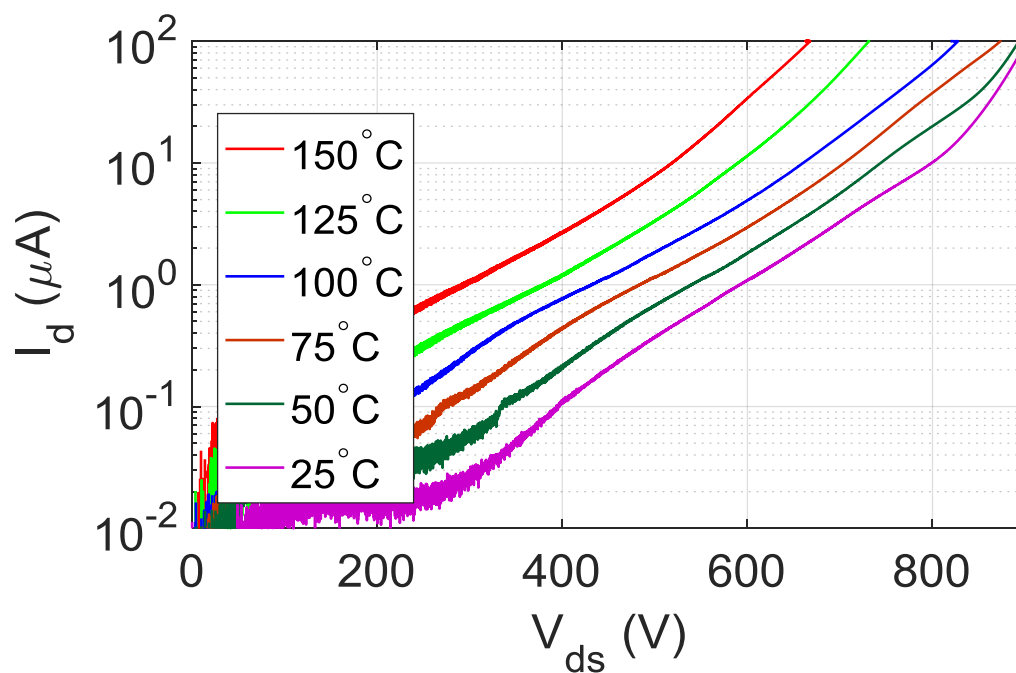


Figure 8.2. Leakage current characteristic for Infineon GIT in semilog scale, with  $V_{gs} = -3$  V.

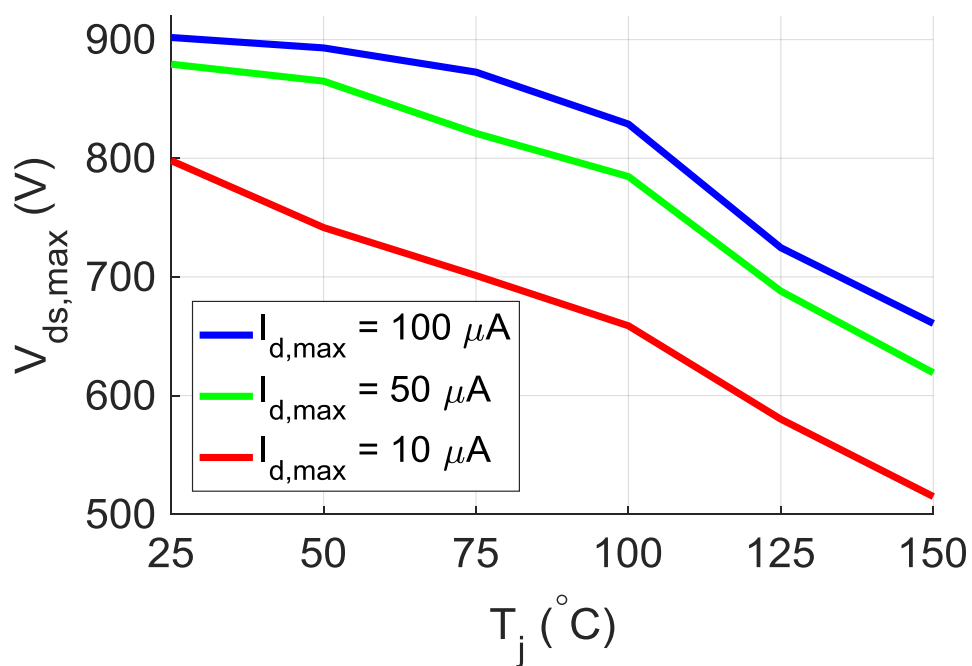


Figure 8.3. Maximum drain voltage vs. temperature for Infineon GIT, based on arbitrary selection of three maximum allowable drain currents.

inductance was experimentally characterized as 13 nH for the power loop shown in Figure 8.4 using the deskew technique in Chapter 4, including the  $\sim 3$  nH insertion inductance of the current measurement shunt SSDN-414-05. The turn-off transient overshoot on the active switch was then experimentally characterized, as well as the overshoot on the synchronous switch during a hard turn-on of the active switch, using the methodology in Chapter 4. The DPT board used for dynamic characterization was designed to permit bypassing of the shunt, as well as the added power loop area inserted by the shunt path. Bypassing the shunt was shown to reduce the turn-on and turn-off overshoot by approximately 30%.

A study was conducted to determine the impact of decoupling capacitor selection on the overshoot voltage. The PCB was designed to fit either of two capacitor types: the Ceralink capacitor B58031I7504M from TDK, and conventional ceramic capacitors with a 3640 footprint. In particular, 220 nF ceramic capacitors from Kemet were used for this comparison. Figure 8.5 shows three examples of decoupling capacitor configurations. Quantities of one, two, and four Ceralink capacitors were first tested. The turn-off and turn-on overshoot voltages are shown in Figure 8.6 and Figure 8.7, respectively. The reduction in overshoot from doubling the quantity of capacitors from two to four was not significant. Several configurations and quantities of Kemet ceramics were then tested, and compared against the two-Ceralink benchmark as shown in Figure 8.8 and Figure 8.9. Both horizontally-oriented and vertically-oriented stacks of Kemet capacitors were tested, and at first the vertical five-Kemet configuration was identified as the best option. However, this test was repeated with two different sets of five Kemet capacitors in the same configuration, and the resulting voltage overshoots were not shown to be repeatably lower than any other configuration. This configuration was selected for the final design, although it seems that fewer capacitors or a different orientation would have little effect on the peak drain voltage.

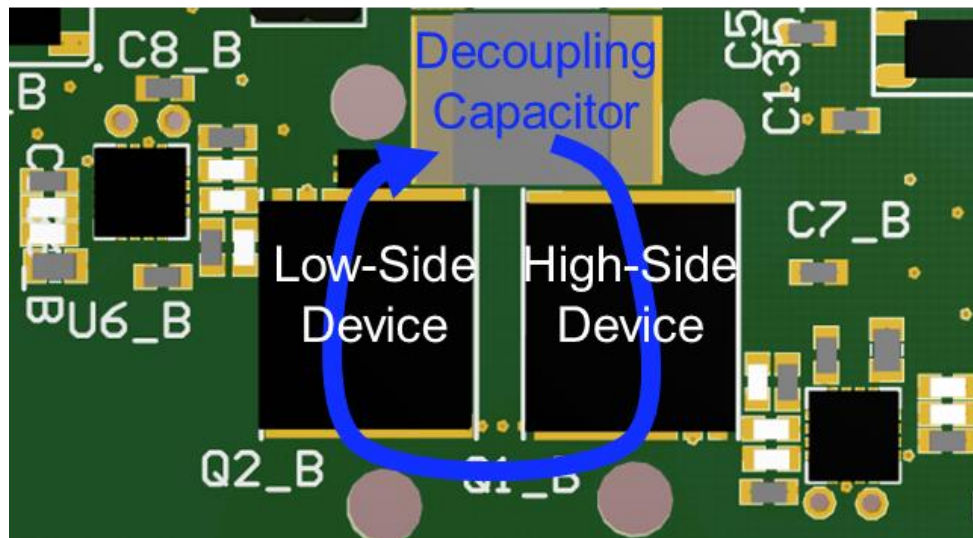


Figure 8.4. Lateral power loop layout with bottom-side cooling.

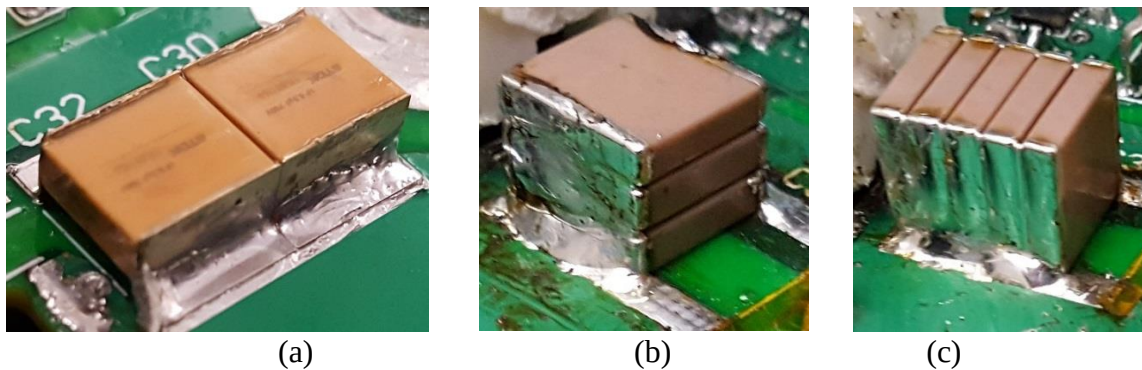


Figure 8.5. Configurations tested for decoupling capacitor banks; (a) two Ceralink capacitors from TDK ( $0.5 \mu\text{F}$ ); (b) three conventional ceramic capacitors from Kemet ( $220 \text{ pF}$  each), oriented horizontally; five conventional ceramic capacitors from Kemet ( $220 \text{ pF}$  each), oriented vertically.

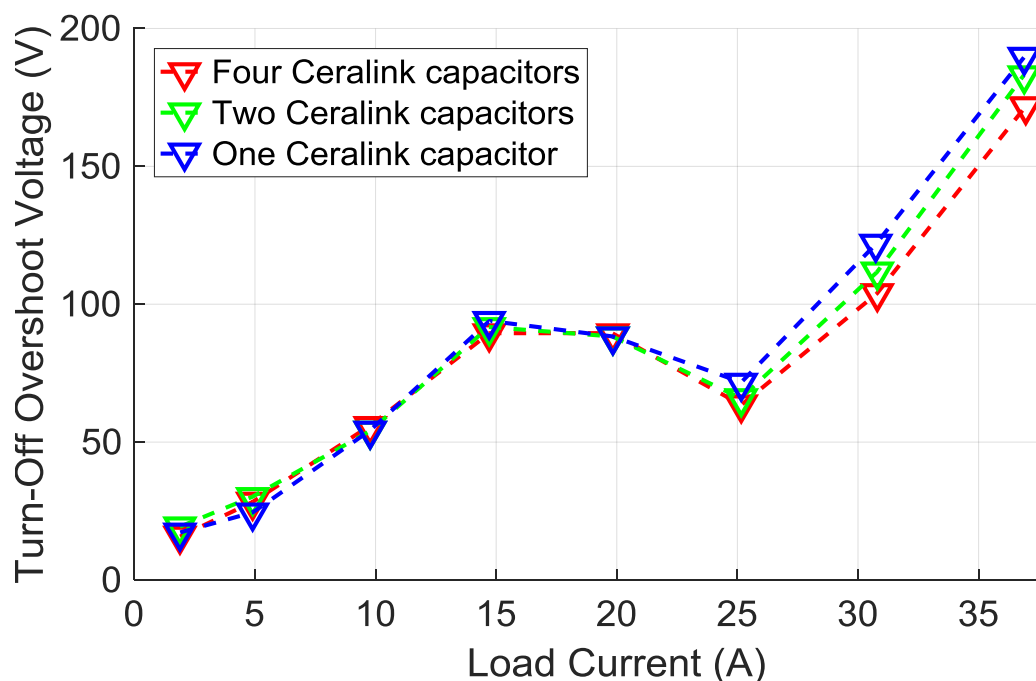


Figure 8.6. Overshoot voltage experienced by active switch  $v_{ds}$  during a hard turn-off transient at 400 V and 25 °C, tested with a variety of Ceralink decoupling capacitor configurations.

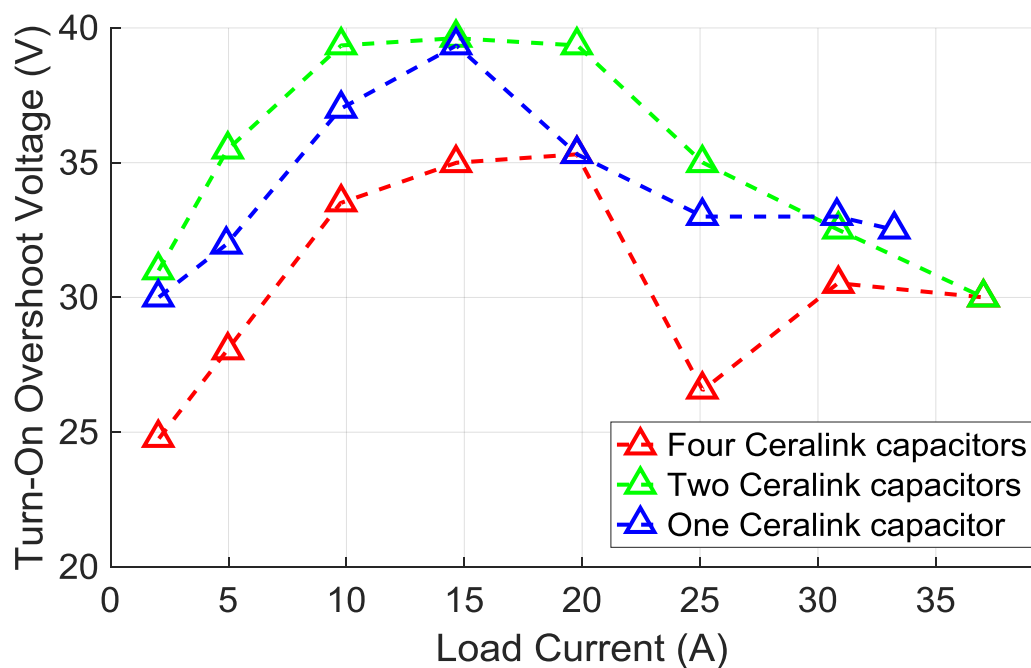


Figure 8.7. Overshoot voltage experienced by synchronous switch  $v_{ds}$  during a hard turn-on transient of the active switch at 400 V and 25 °C, tested with a variety of Ceralink decoupling capacitor configurations.

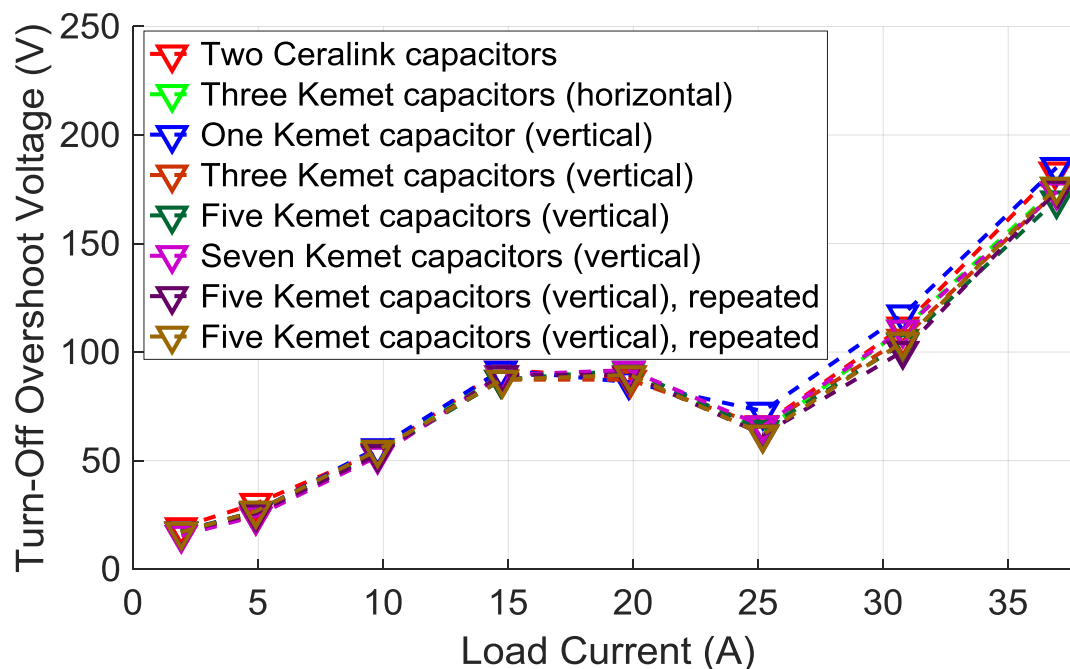


Figure 8.8. Overshoot voltage experienced by active switch  $v_{ds}$  during a hard turn-off transient at 400 V and 25 °C, tested with a variety of decoupling capacitor options.

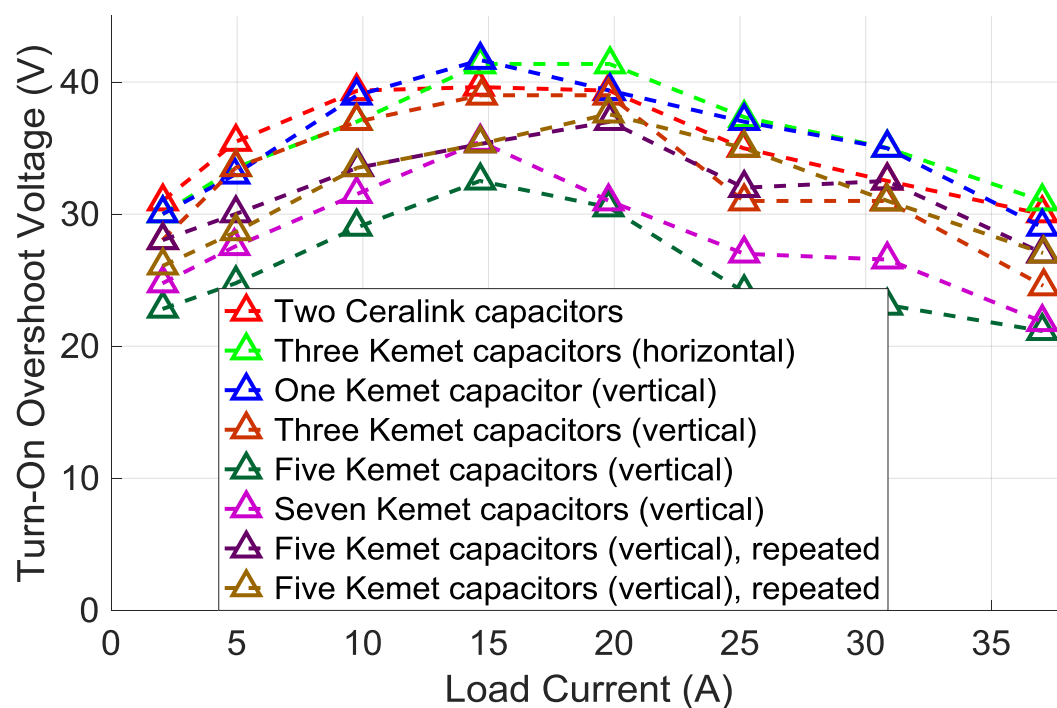


Figure 8.9. Overshoot voltage experienced by synchronous switch  $v_{ds}$  during a hard turn-on transient of the active switch at 400 V and 25 °C, tested with a variety of decoupling capacitor options.

### 8.4.3 Consideration of gate drive circuit parameters

The capacitive gate driver circuit recommended by manufacturers for the GaN GIT was previously described in Chapter 2. Figure 8.10 shows a schematic of the gate drive circuit used in this work, including an interpretation of the AN34092B functional block diagram in the on-state and off-state. The driver datasheet describes Out 1 as the dynamic turn-on output, Out 2 as the steady-state turn-on output, and Out 3 as the turn-off output (both dynamic and steady-state). However, it is clear from this circuit that both Out 1 and Out 3 are involved in the dynamic turn-off process. When the internal pull-up and pull-down transistors associated with Out 1 change state, the “speed-up capacitor”  $C_{su}$  provides a burst of current that supplements the dynamic turn-off gate current from Out 3. For this reason, a diode (D1) was added to the recommended gate driver circuit, so that the  $C_{su}$  current during turn-off can be tuned independently of turn-on speed. It is worth noting that the discharge of  $C_{su}$  during the turn-off transient is necessary in order to prepare for the next turn-on transient. If it still has stored charge when the next turn-on occurs, it will not provide the expected dynamic turn-on current. A second diode (D2) was also added in some iterations of the circuit to limit negative spikes in gate voltage during the turn-off transient.

Figure 8.11 and Figure 8.12 show the overshoot voltages at 400 V with various gate drive circuit configurations. The primary turn-off gate resistor  $R_{g,off1}$  was incremented from 0  $\Omega$  to 20  $\Omega$ , and the diodes D1 and D2 were included in various combinations. When D1 was included,  $R_{g,on}$  was set as 10  $\Omega$  and  $R_{g,off2}$  was set as 100  $\Omega$ . Interestingly, the turn-off overshoot showed an increase with higher  $R_{g,off1}$ , and no impact from inclusion of either diode. The trend of turn-off overshoot voltage with respect to current shows an initial peak around 15 A, followed by a slight dip and a continued increase above 25 A. This trend was found to change significantly as  $R_{g,off1}$  was increased, so that the overshoot continues to increase with current as predicted in Chapter 6 without any dip.

Gray Box: Internal Functions of AN34092B  
Green: On State (Pull-Up Transistor)  
Red: Off State (Pull-Down Transistor)  
Blue: Optional Diodes

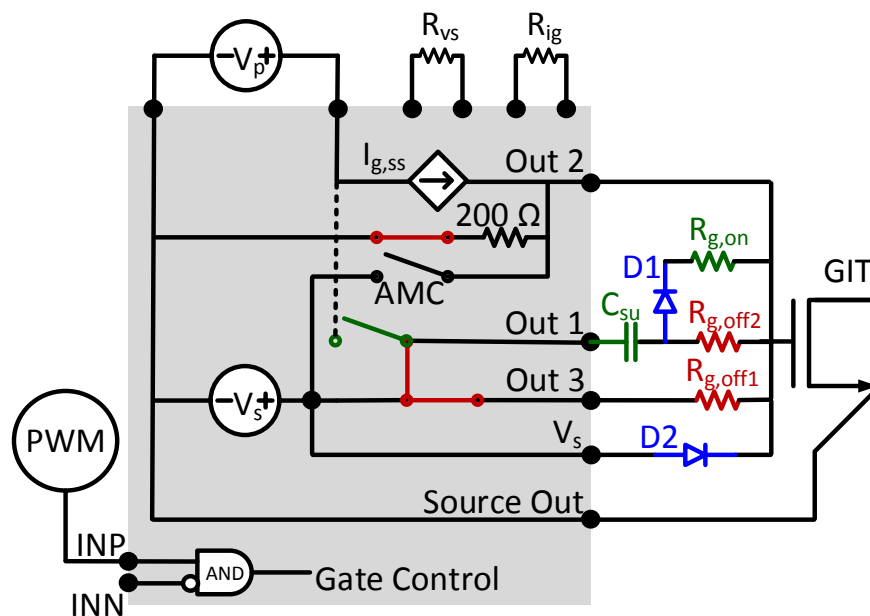


Figure 8.10. Functional schematic of gate driver circuit used in this work, based around commercially available “x-GaN” driver AN34092B from Panasonic; in on-state (top) and off-state (bottom).

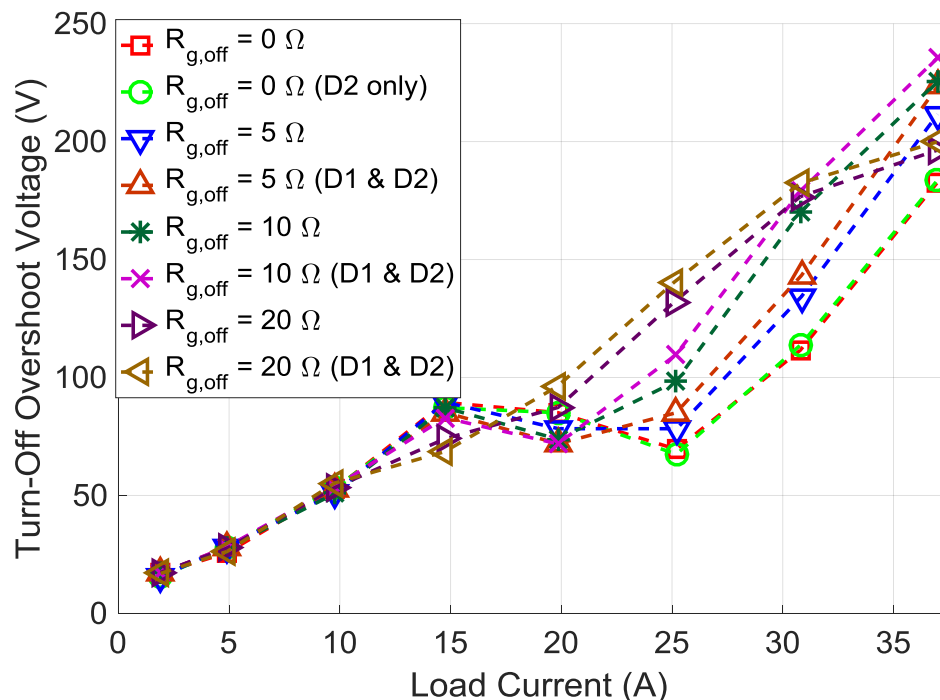


Figure 8.11. Overshoot voltage experienced by active switch  $v_{ds}$  during a hard turn-off transient at 400 V and 25 °C, with a variety of turn-off gate resistances and diode options.

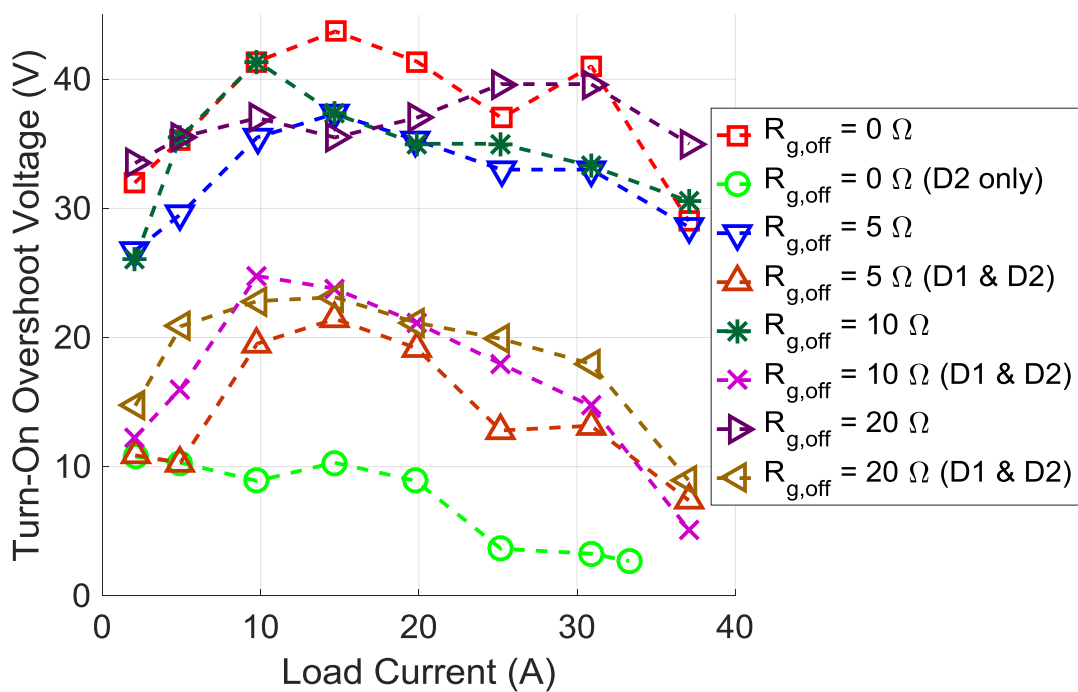


Figure 8.12. Overshoot voltage experienced by synchronous switch  $v_{ds}$  during a hard turn-on transient of the complementary switch at 400 V and 25 °C, with a variety of turn-off gate resistances and diode options.



Increasing the turn-off gate resistance actually increases the overshoot for part of the load current range. The only reduction in overvoltage occurs with  $20\ \Omega$  at 35 A, which is beyond the intended operating range of this inverter. The turn-off switching loss increases dramatically with any increase in  $R_{g,off1}$ , with no apparent benefit to overshoot voltage. On the other hand, this study showed that the inclusion of D2 reduced the turn-on overshoot voltage by 50% or more, without a significant impact on turn-on switching loss. This effect is likely due to the nonlinear capacitive loading introduced on the gate by this diode, although that phenomenon was not further explored as part of this work.

The lack of any impact from including D1 prompted further analysis of the turn-off gate driver circuit. According to the datasheet, the state-change of Out 3 and Out 1 both occur at the same instant. In fact, experimental observations indicate that the state-change of Out 1 is delayed by 45 ns after the Out 3 pull-down transistor is triggered, resulting in the piecewise gate current function

$$i_{g,off} = \begin{cases} \frac{v_{gs} - V_s}{R_{g,off1} + R_{g,int} + R_{pd3}} & 0 < t < 45\ ns \\ \frac{v_{gs} - V_s}{R_{g,off1} + R_{g,int} + R_{pd3}} + \frac{v_{gs} + v_{csu} - V_s}{R_{g,off2} + R_{g,int} + R_{pd1}} & t > 45\ ns \end{cases} \quad (8.1)$$

where  $R_{g,int}$  is the internal gate resistance of the GIT, and  $R_{pd1}$  and  $R_{pd3}$  are the pull-down resistances of Out1 and Out 3 respectively. The time  $t$  here is the time elapsed since the turn-off transient has begun. With no D1,  $R_{g,off2}$  can effectively be replaced in (8.1) with  $R_{g,on}$ , which in this case is  $10\ \Omega$ . With this equation in mind, both turn-off gate resistances were increased in more significant steps to  $100\ \Omega$  and  $1\ \text{k}\Omega$ . Figure 8.13 and Figure 8.14 show the impact of this large  $R_{g,off}$  on turn-off overshoot and switching energy.

As with the previous testing up to  $20\ \Omega$ , increasing  $R_{g,off1}$  by itself to  $100\ \Omega$  worsened both turn-off overshoot and energy. In the switching waveforms, a clear step-change in  $dv_{gs}/dt$  was

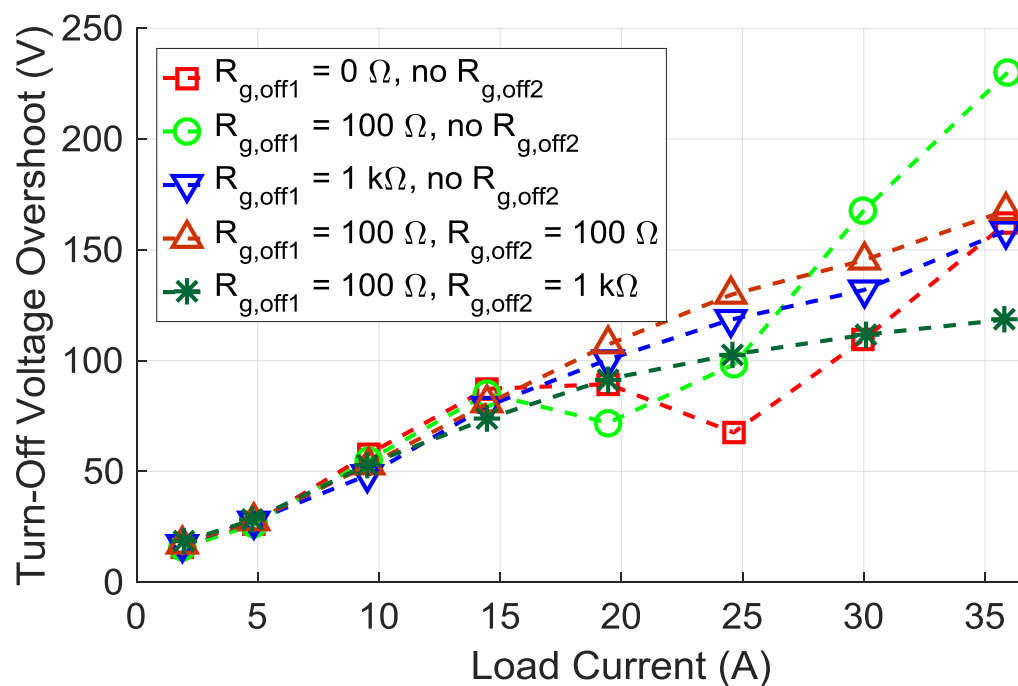


Figure 8.13. Overshoot voltage experienced by active switch  $v_{ds}$  during a hard turn-off transient, at 400 V and 25 °C with  $C_{su} = 470$  pF,  $R_{g,on} = 10 \Omega$ .

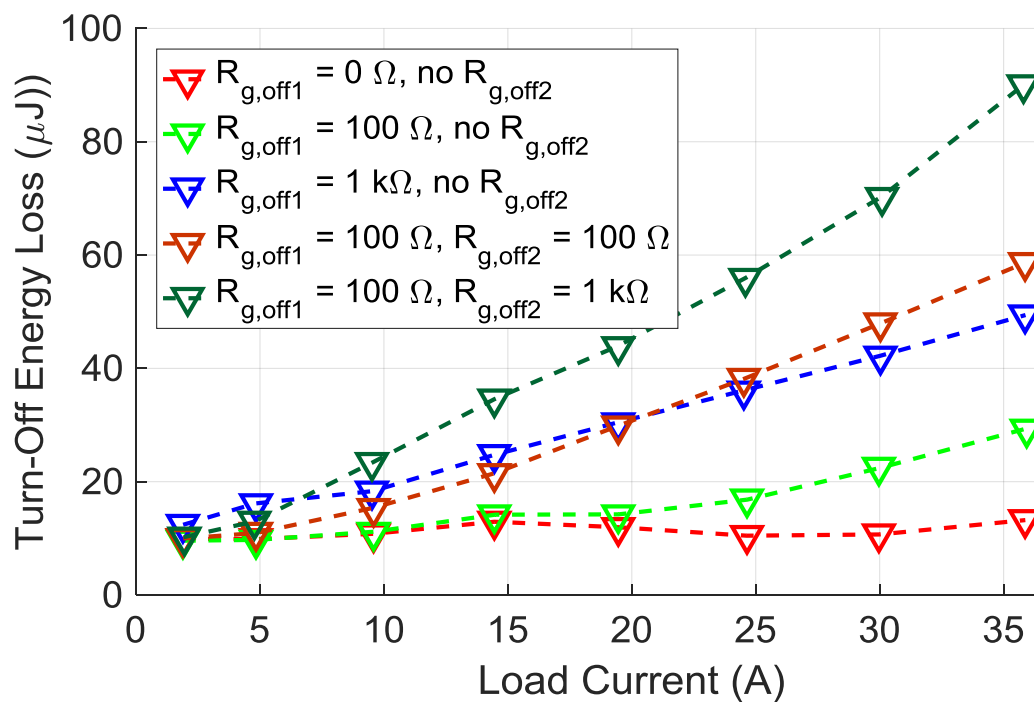


Figure 8.14. Turn-off loss at 400 V and 25 °C with  $C_{su} = 470$  pF,  $R_{g,on} = 10 \Omega$ .

visible at 45 ns after the start of the turn-off transient. Further increasing  $R_{g,off1}$  to 1 k $\Omega$  resulted in a substantial decrease in overshoot voltage in the 30-35 A range, and increasing  $R_{g,off1}$  and  $R_{g,off2}$  both to 100  $\Omega$  produces approximately the same overshoot and loss. Continuing to increase either parameter shows this same trend of lower overshoot and higher loss. Rather than suffer the higher switching loss, the final selected design used  $R_{g,off1} = 0 \text{ } \Omega$  with no D1 or  $R_{g,off2}$ . This limits the maximum load current for a given bus voltage, but the dip in the trend from 25-30 A is advantageous here. With the 30% overall reduction in overshoot when the current shunt is removed, this brings the maximum operating current to approximately 35 A without exceeding 100 V overshoot.

Next, the turn-on overshoot was considered. The shape of this dynamic turn-on current can be controlled with  $V_p$ ,  $C_{su}$ , and  $R_{g,on}$ . The first gate drive circuit implemented in this testing used a dynamic turn-on driving voltage of 15 V and a speed-up capacitance of 1 nF. This test destroyed the synchronous switches in two tests, with a peak voltage exceeding 900 V. For the majority of testing, these parameters were therefore reduced to 10 V and 470 pF, with  $R_{g,on} = 10 \text{ } \Omega$ . Once the turn-on overshoot voltage was reduced to 10 V as shown in Figure 8.12, a faster turn-on was again attempted. The turn-on loss was shown to improve by increasing  $C_{su}$  to 1 nF with  $V_p = 10 \text{ V}$ , and these results are shown in Figure 8.15 - Figure 8.18.

#### 8.4.4 Consideration of bus voltage and operating temperature

The impact of bus voltage and junction temperature on both overshoot voltages was also considered, to verify that the gate drive circuit parameter sweeps at 25  $^{\circ}\text{C}$  and 400 V are a reasonable representation of the anticipated results in the full operating range of the inverter. The turn-on overshoot for this device decreased at higher bus voltages, particularly at 300 V and lower, where both output capacitances remain in the highly nonlinear region of the  $C_{oss}$  curve for most of the transient. The turn-off overshoot voltage also decreased at higher bus voltage, but only in the

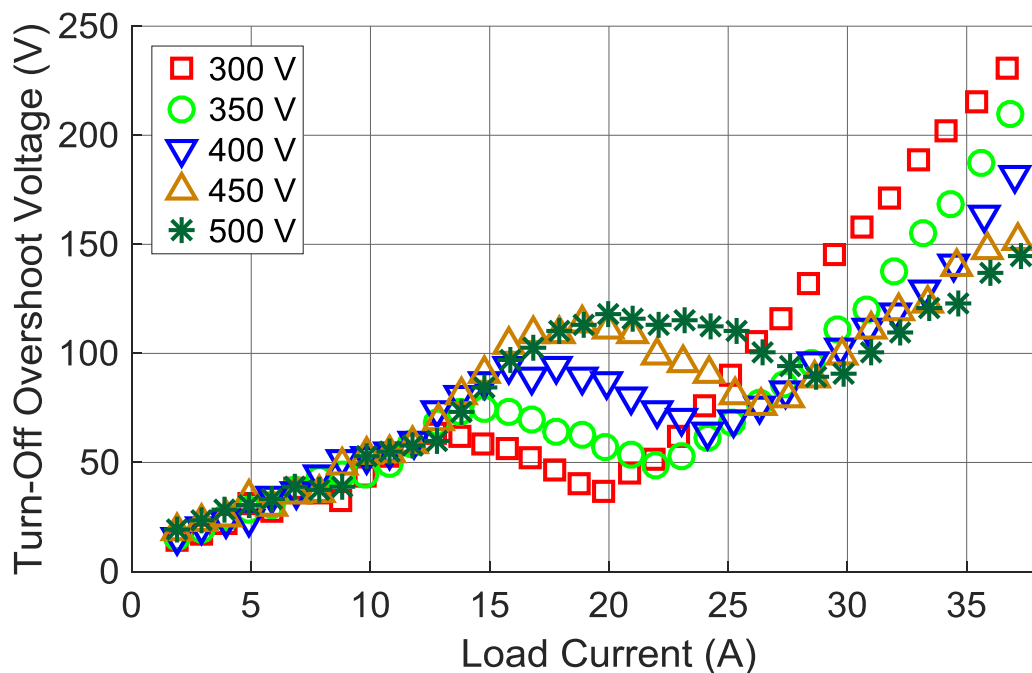


Figure 8.15. Overshoot voltage experienced by active switch  $v_{ds}$  during a hard turn-off transient at 25 °C with  $C_{su} = 1$  nF,  $R_{g,on} = 10$   $\Omega$ ,  $R_{g,off1} = 0$   $\Omega$ , and no  $R_{g,off2}$ .

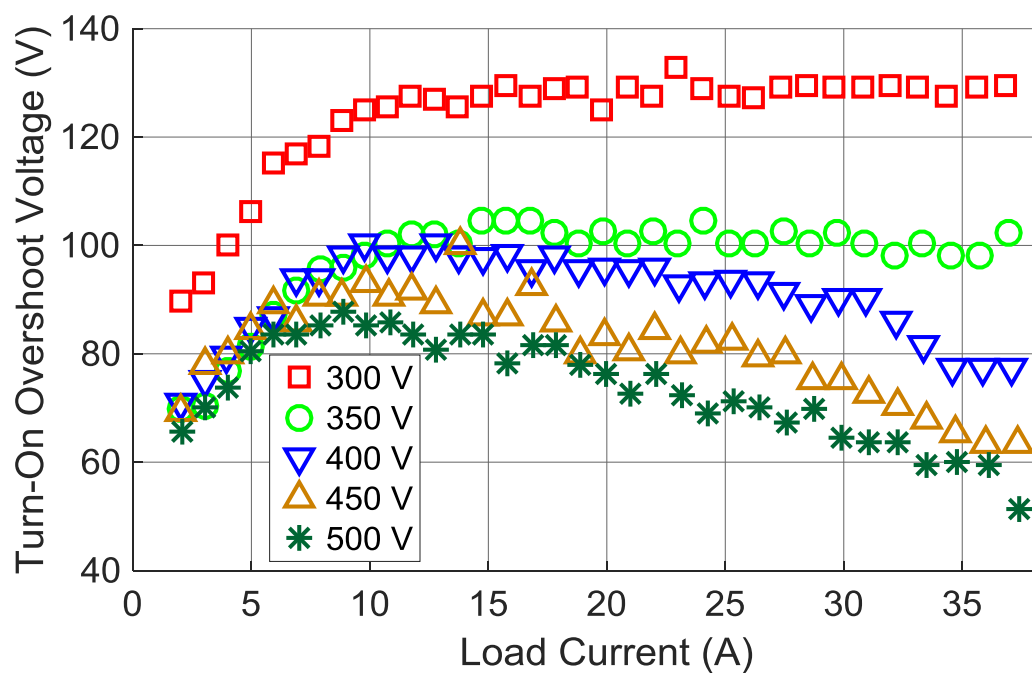


Figure 8.16. Overshoot voltage experienced by synchronous switch during a hard turn-on transient of the complementary switch at 25 °C with  $C_{su} = 1$  nF,  $R_{g,on} = 10$   $\Omega$ ,  $R_{g,off} = 0$   $\Omega$ , and no  $R_{g,off2}$ .

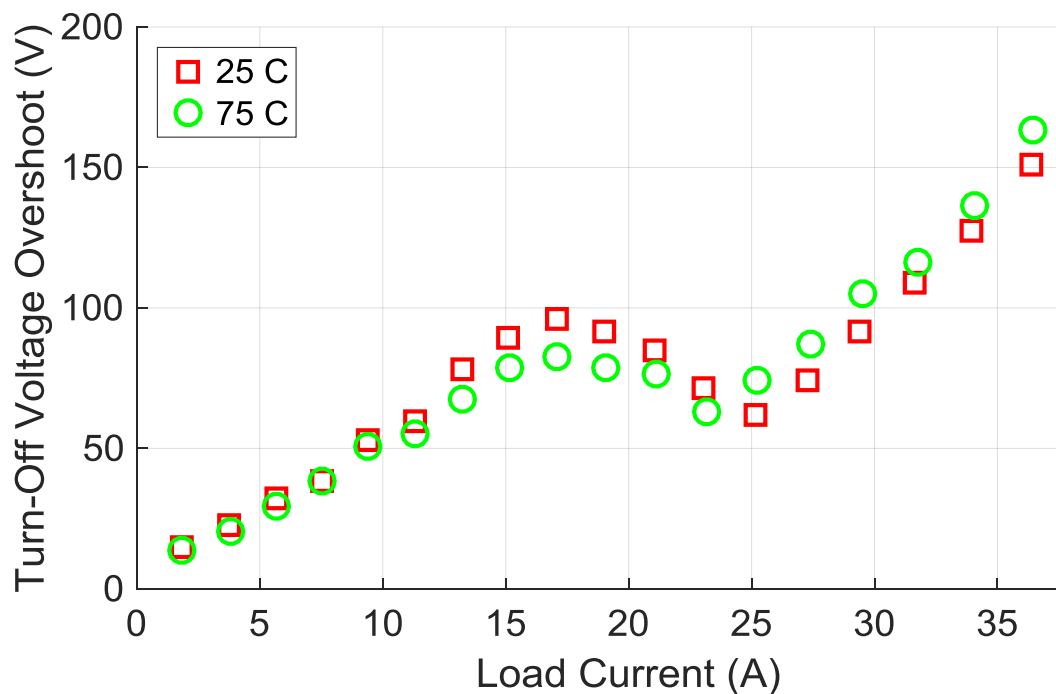


Figure 8.17. Overshoot voltage experienced by active switch during a hard turn-off transient at 400 V with  $C_{su} = 1 \text{ nF}$ ,  $R_{g,on} = 10 \text{ } \Omega$ ,  $R_{g,off} = 0 \text{ } \Omega$ , and no  $R_{g,off2}$ .

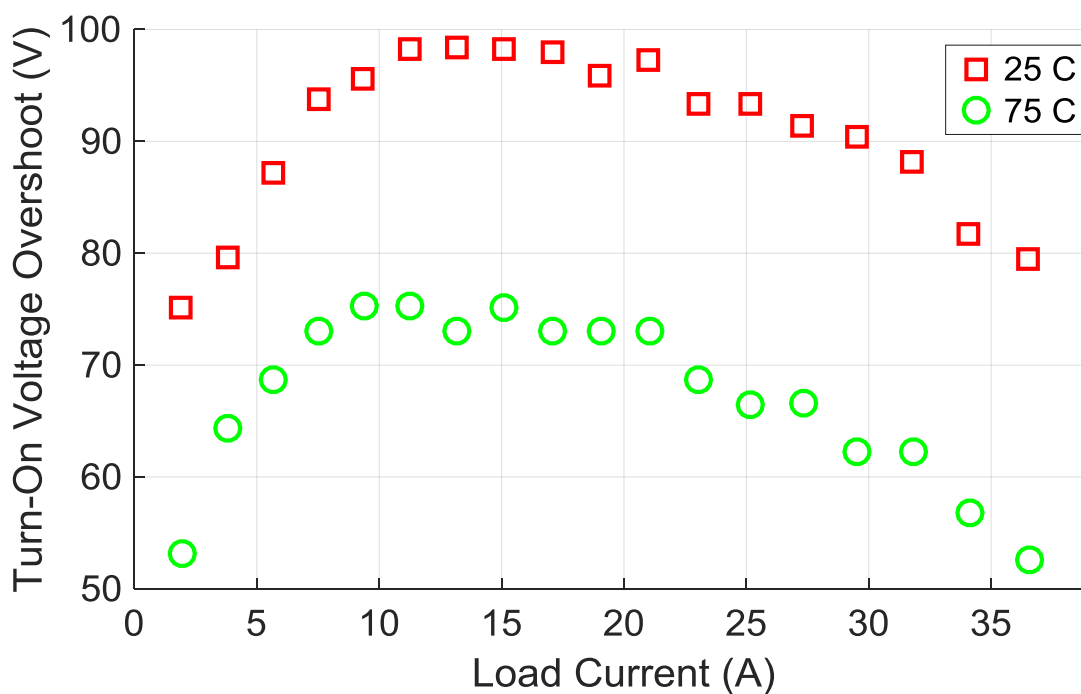


Figure 8.18. Overshoot voltage experienced by synchronous switch during a hard turn-on transient of the complementary switch at 400 V with  $C_{su} = 1 \text{ nF}$ ,  $R_{g,on} = 10 \text{ } \Omega$ ,  $R_{g,off} = 0 \text{ } \Omega$ , and no  $R_{g,off2}$ .

high current range. Between 12 and 25 A, the opposite trend was observed, and the bus voltage did not have an apparent effect on turn-off overshoot below 12 A.

The turn-on overshoot was observed to decrease significantly with higher temperature, and the turn-off overshoot did not change significantly. Therefore, room temperature was assumed to be the worst-case operating condition for both overshoots.

#### 8.4.5 Analysis of turn-on and turn-off overshoot waveforms

The experimental results were analyzed to further understand the key impact factors in turn-on and turn-off overshoot. General equations were previously derived in Chapter 6, which were applied in this analysis. Turn-off overshoot was expected to increase primarily with load current. The trend exhibited in Figure 8.15 in the mid-load range does not fit this expectation. However, it can be explained using the same equations derived in Chapter 6 involving the ratio of output capacitances,  $x_c$ . According to (6.19), the excitation of the loop inductance resonance is primarily caused by two factors: the change in channel current, and the change in  $x_c$  with respect to drain voltage ( $dx_c/dv_{ds}$ ). During the turn-off transient, these two factors can in fact be treated as two separate excitation events, according to

$$\frac{di_d}{dt}(a) = x_c \frac{di_{chan}}{dt} \quad (8.2)$$

$$\frac{di_d}{dt}(b) = -(I_L - i_{chan})^2 \left( \frac{x_c}{C_{oss, sync}} \right) \frac{dx_c}{dv_{ds}} \quad (8.3)$$

At the beginning of the turn-off,  $I_L = i_{chan}$ , so (8.3) is zero. Likewise, at the end of the turn-off transient, (8.2) is zero, because the channel has fully turned off by that time.

It is helpful to visualize the magnitudes of the parameters  $x_c$  and  $dx_c/dv_{ds}$  during the transient to understand this relationship. Figure 8.19 shows the calculated ratio  $x_c$  from the  $C_{oss}$  curve of the Infineon GIT, over the course of a switching transient at several dc bus voltages, and Figure 8.20 shows its derivate.

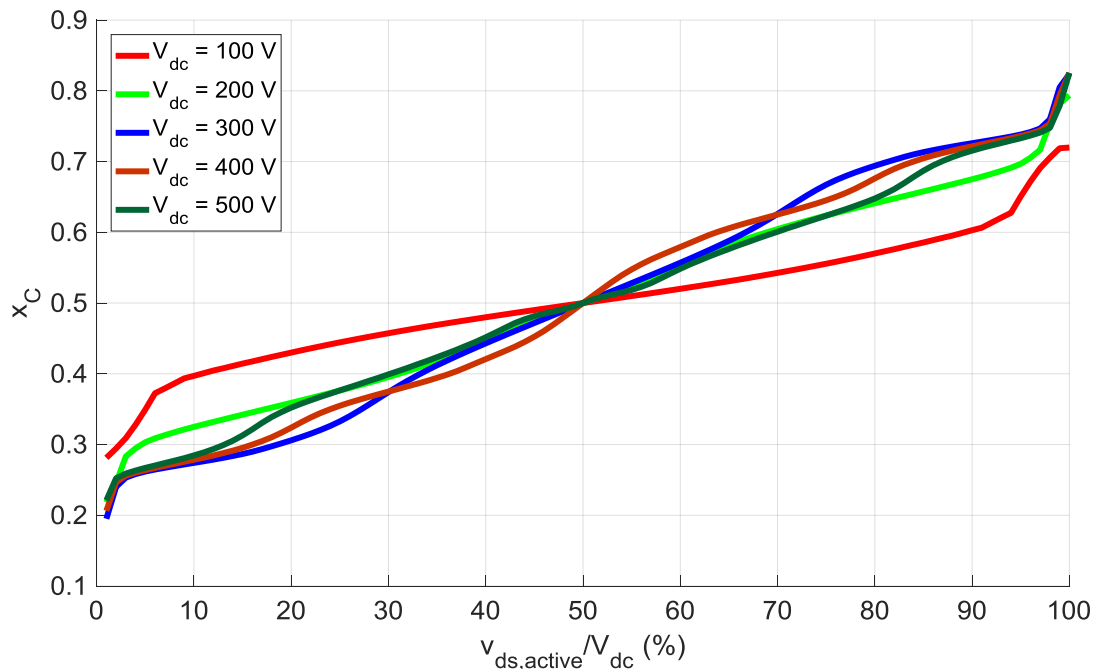


Figure 8.19. Ratio of synchronous switch output capacitance to total switch node capacitance,  $x_c$ , over the duration of the switching transient at several bus voltages.

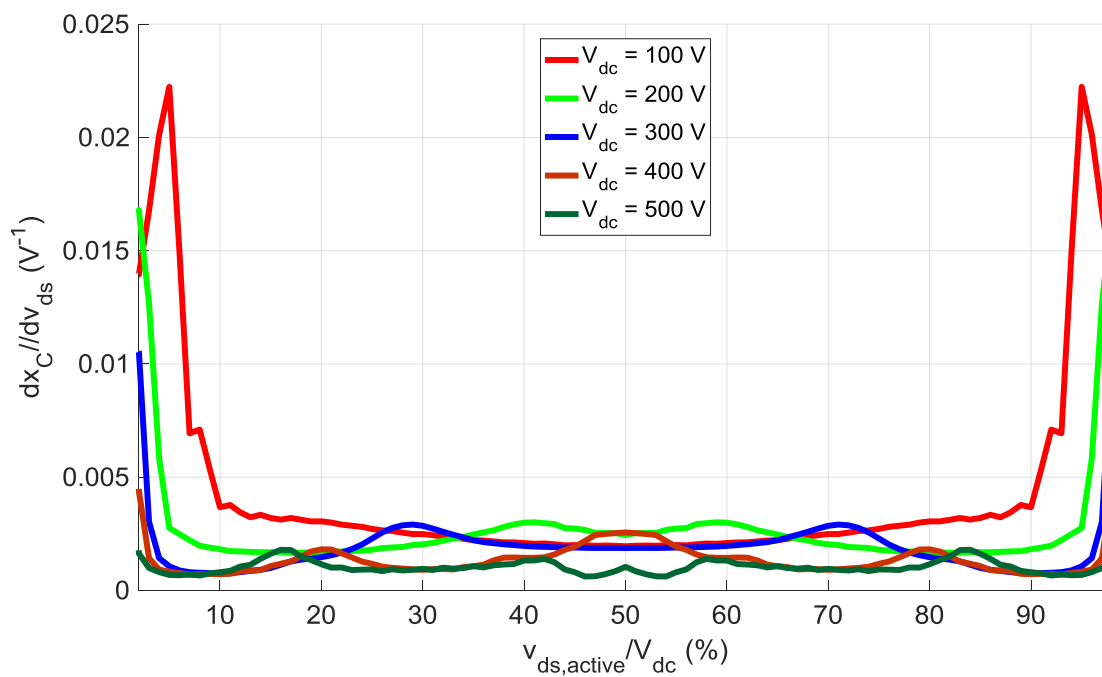


Figure 8.20. Derivative of output capacitance ratio  $x_c$  with respect to drain voltage, over the duration of the switching transient at several bus voltages.

Two major spikes in  $dx_C/dv_{ds}$  occur during the transient, although the first spike occurs when (8.3) is still approximately zero as mentioned. However, (8.2) contains the ratio  $x_C$ , so the nonlinearity of the capacitances still impacts the magnitude of this first excitation. The second spike in  $dx_C/dv_{ds}$  occurs near the end of the transient, causing the second excitation (8.3). Both  $x_C$  and its derivative show a negative correlation with the operating bus voltage, indicating that the magnitude of overshoot should decrease with higher bus voltage. This correlation is very pronounced up to 300 V, and becomes very weak at higher bus voltages.

The duration of the turn-off transient is inversely correlated to load current. At light load (e.g.,  $I_L < 10$  A), there is a long delay between  $di_d/dt(a)$  and  $di_d/dt(b)$ , allowing the resonance to be damped out somewhat before the second excitation occurs. At heavy load (e.g.,  $I_L > 25$  A), these two excitations occur at nearly the same time, because the duration of the turn-off transient is so short. For the mid-load region between 10 and 25 A, the interaction of these two events becomes more complex. Experimental results were compared for various operating conditions to explain this phenomenon. Figure 8.21 compares several load current conditions from DPT results of the Infineon GIT at 400 V, with the waveforms time-aligned to the instant when the drain voltage first reaches the bus voltage ( $v_{ds} = V_{dc}$ ). The 15 A and 20 A waveforms are highlighted to show the drain current resonating before the transient has completed. In contrast, the waveforms at 5 A and 10 A show the drain current dropping near the beginning and the end of the transient, and remaining relatively flat in between. The 25 A and 30 A waveforms show only one drop in drain current. In all cases, the drain current resonates after it drops, but  $di_d/dt$  only changes direction before that time with a load current of 15 A or 20 A. Figure 8.22 - Figure 8.24 show a similar comparison of waveforms, with a single load current shown in each figure, but with several bus voltages superimposed for comparison. The magnitude of overshoot voltage is not affected much by changing bus voltage, although there is a slight positive correlation in the mid-load range and a



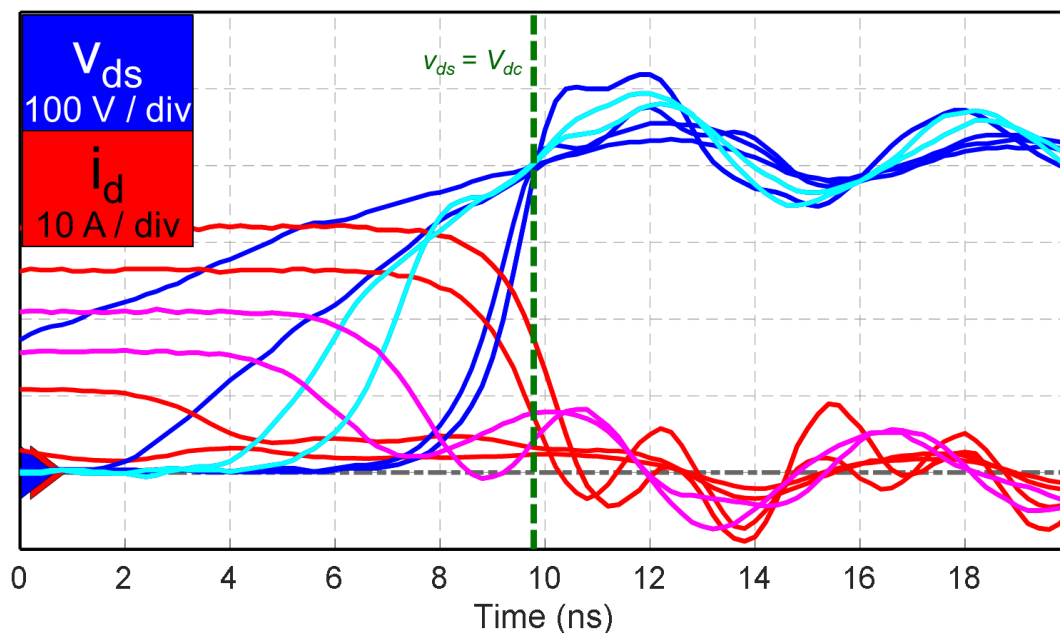


Figure 8.21. Experimental waveforms of active switch during a turn-off transient at 400 V, showing several load currents superimposed and time-aligned to  $v_{ds} = V_{dc}$ . Highlighted waveforms (magenta and cyan) indicate 15 and 20 A load conditions.

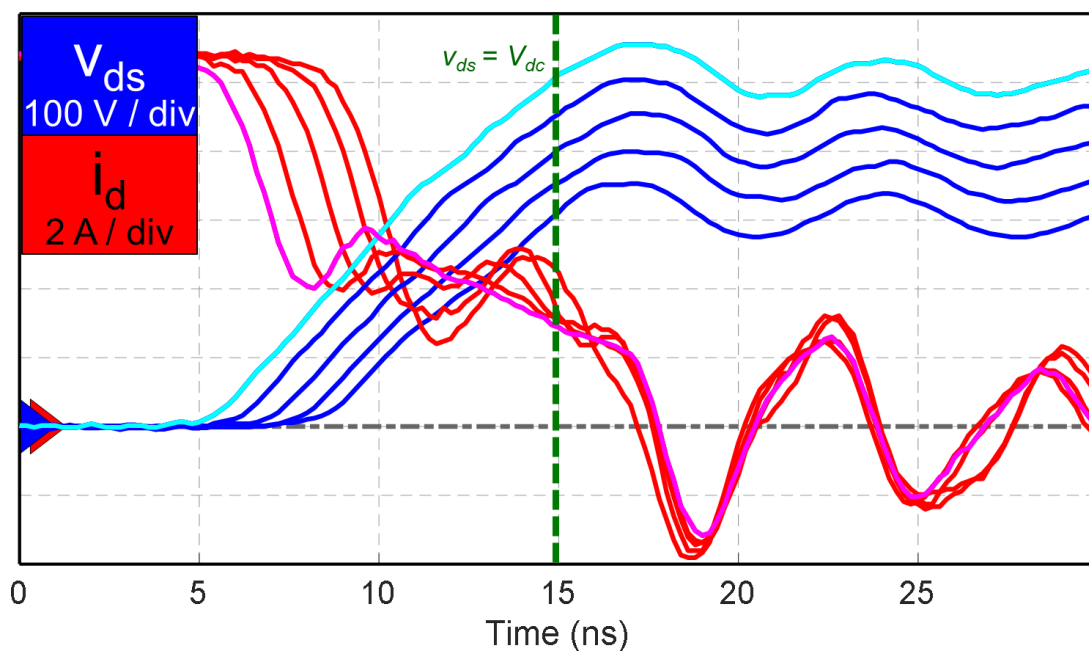


Figure 8.22. Experimental waveforms of active switch during a turn-off transient at 10 A, showing several bus voltages superimposed and time-aligned to  $v_{ds} = V_{dc}$ . Highlighted waveforms (magenta and cyan) indicate  $V_{dc} = 500$  V.

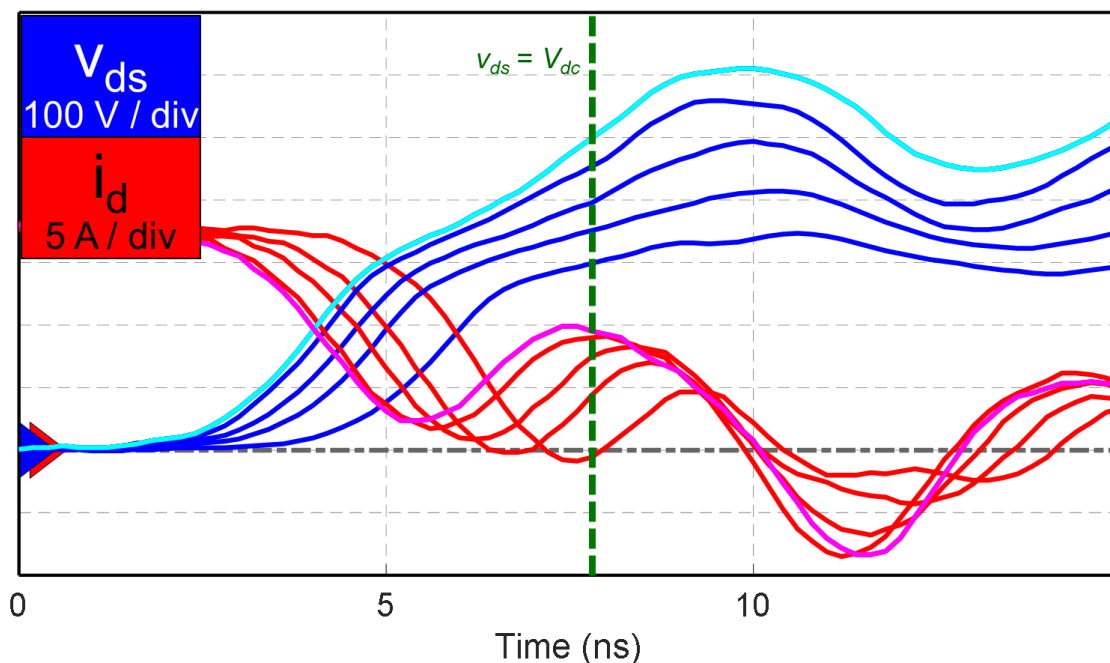


Figure 8.23. Experimental waveforms of active switch during a turn-off transient at 17 A, showing several bus voltages superimposed and time-aligned to  $v_{ds} = V_{dc}$ . Highlighted waveforms (magenta and cyan) indicate  $V_{dc} = 500$  V.

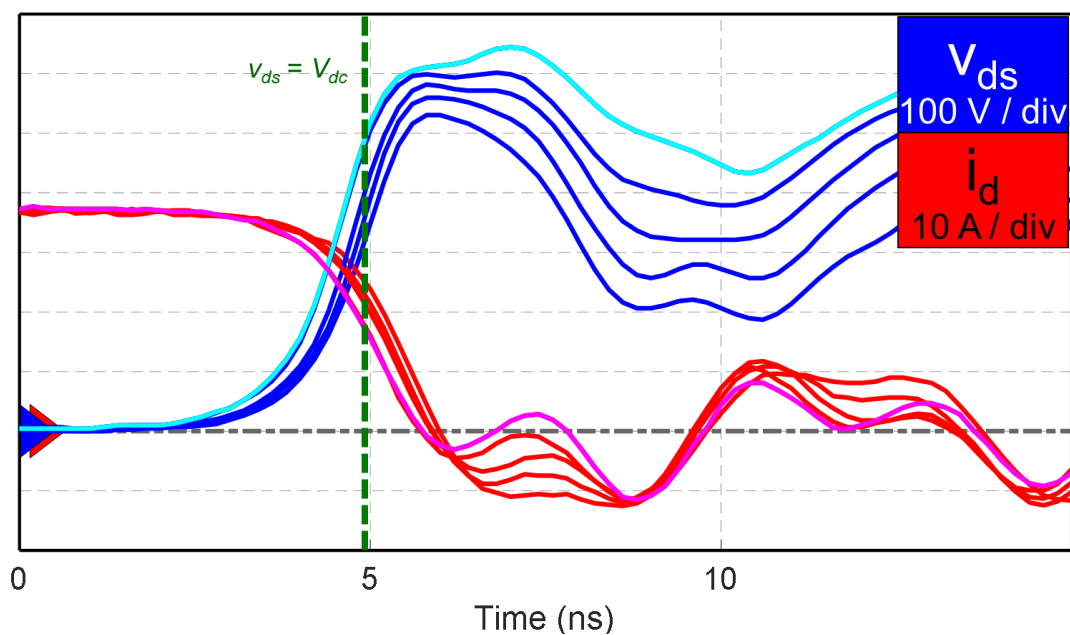


Figure 8.24. Experimental waveforms of active switch during a turn-off transient at 35 A, showing several bus voltages superimposed and time-aligned to  $v_{ds} = V_{dc}$ . Highlighted waveforms (magenta and cyan) indicate  $V_{dc} = 500$  V.

slight negative correlation in the heavy load range.

The resonant interaction of the off-state device  $C_{oss}$  and loop inductance  $L_{loop}$  is clearly complex, but with all other elements ignored, it can be represented as

$$i_d = I_o \cos(\omega t) \quad (8.4)$$

where  $I_o$  is the drain current when  $v_{ds}$  crosses  $V_{dc}$ , and  $C_{oss}$  therefore stores no resonant energy. The peak  $di_d/dt$  is therefore directly proportional to  $I_o$  as well. This relationship provides a more intuitive interpretation of the waveforms compared here. The trend in overshoot voltage with bus voltage corresponds to the trend in  $I_o$  indicated in Figure 8.23 and Figure 8.24.

This relationship between overshoot voltage and  $I_o$  can also shed light on the trends observed in turn-on overshoot voltage. Figure 8.25 and Figure 8.26 show the waveforms of the synchronous switch during a hard turn-on of the active switch, comparing several bus voltages and load currents. The synchronous switch drain current waveforms are nearly indistinguishable for all operating conditions after the zero crossing. The drain voltage waveforms are also similar, but the higher voltage conditions require more time for  $v_{ds}$  to reach  $V_{dc}$ , allowing the drain current overshoot to drop further. This explains why  $I_o$  is negatively related to  $V_{dc}$ , as is the overshoot voltage. Variation in  $I_L$  does not show a major impact on  $I_o$  or overshoot voltage in these experimental results. The biggest impact factor on turn-on overshoot is the gate drive speed, which determines the magnitude of this drain current peak according to

$$i_d - I_L = i_{chan} x_C = g_{fs} \frac{dv_{gs}}{dt} t x_C . \quad (8.5)$$

A faster gate drive with a higher  $v_{gs}$  slew rate increases the peak  $i_d$ , and thereby increases  $I_o$ . This be seen in Figure 8.27, which compares the slower turn-on ( $C_{su} = 470$  pF) at several load currents, superimposed and time-aligned. In this case,  $v_{ds}$  appears to have not yet reached  $V_{dc}$  at the  $I_o$  indicated in the figure. This is due to the internal package inductance of the device, but even compensating  $v_{ds}$  for this internal  $L_{ds}$  shows that the internal  $v_{ds}$  overshoot is less than 10 V. The

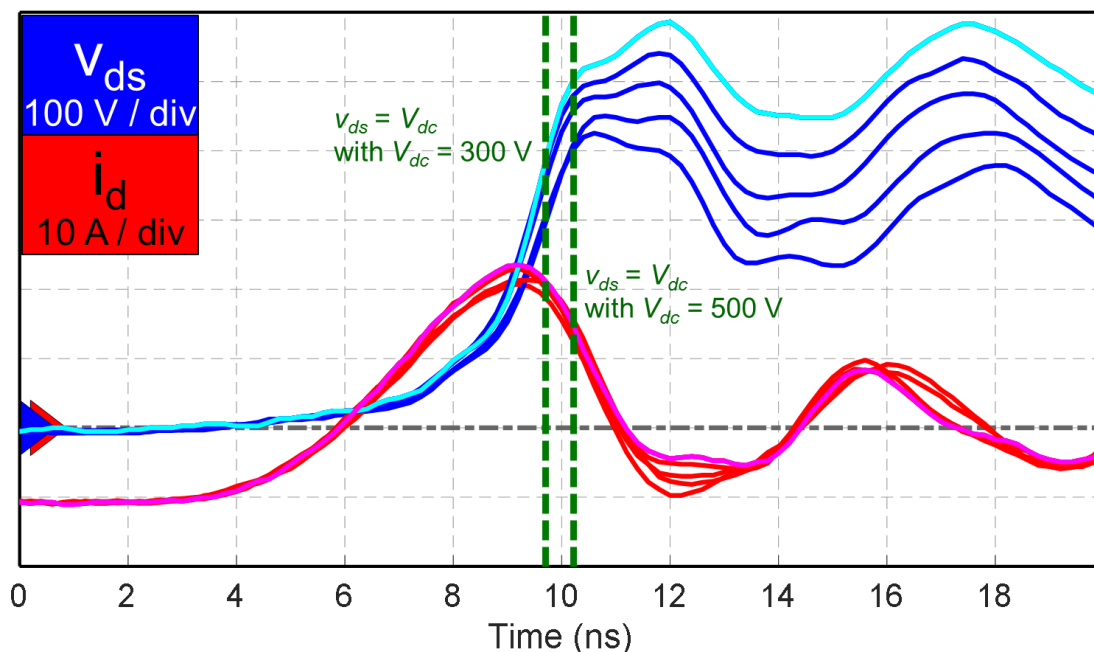


Figure 8.25. Experimental waveforms of synchronous switch during a turn-on transient of the active switch at 10 A, with  $C_{su} = 1$  nF, showing several bus voltages superimposed and time-aligned to  $i_d$  zero crossing. Highlighted waveforms (magenta and cyan) indicate  $V_{dc} = 500$  V.

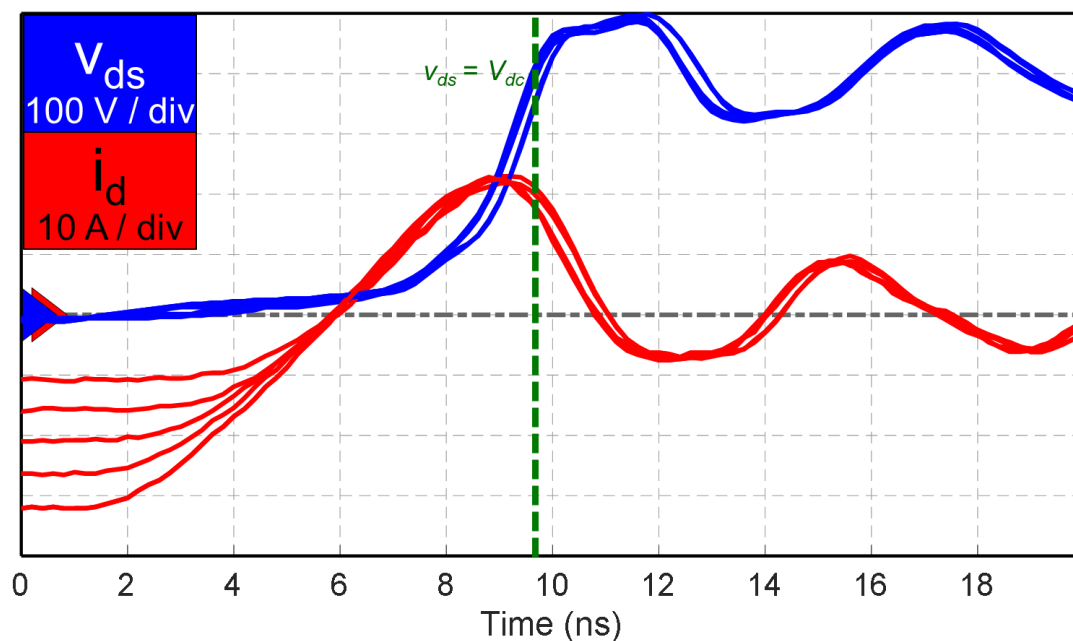


Figure 8.26. Experimental waveforms of synchronous switch during a turn-on transient of the active switch at 400 V, with  $C_{su} = 1$  nF, showing several load currents superimposed and time-aligned to  $i_d$  zero crossing.

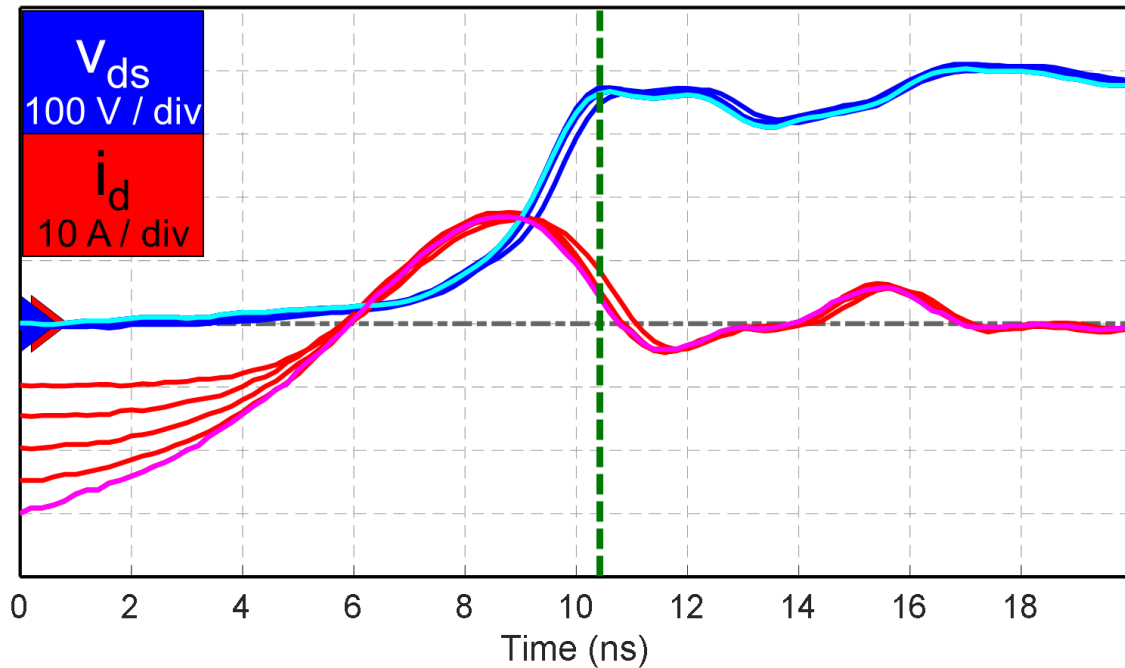


Figure 8.27. Experimental waveforms of synchronous switch during a turn-on transient of the active switch at 400 V, with  $C_{su} = 470$  pF, showing several load currents superimposed and time-aligned to  $i_d$  zero crossing. Highlighted waveforms (magenta and cyan) indicate  $I_L = 30$  A.

turn-on overshoot voltage was reduced from 100 V to under 10 V by slowing down the turn-on speed. In a similar way, an early test with an even faster gate drive circuit ( $V_p = 15$  V) caused an overshoot of several hundred volts, destroying the synchronous switch.

Although this is not intended as a generalized model of overshoot voltage, this analysis helps to interpret the experimental characterization results, and thereby informs the decisions for gate drive circuit parameters and maximum operating conditions used in this inverter. The gate drive circuit parameters were selected as  $V_p = 10$  V,  $R_{g,on} = 10$   $\Omega$ ,  $C_{su} = 470$  pF, and  $R_{g,off} = 0$   $\Omega$ . The primary constraint for this selected was reducing the overshoot voltages below 100 V at the maximum intended operating condition of 450 V with 34 A instantaneous load current. Although  $C_{su} = 1$  nF reduced the turn-on loss without exceeding 100 V turn-on overshoot, the final implemented inverter design used the lower value of 470 pF, as an added precaution to avoid damaging any more GITs. This may be increased in the next version of the experimental prototype.

## 8.5 Junction temperature limitation

The limitation on operating conditions imposed by the junction temperature constraint was addressed next. First, the device losses were modeled based on analysis of experimental characterization. Then, a thermal design was proposed and experimentally verified.

### 8.5.1 Device loss model using experimental characterization results

The switching losses were experimentally characterized with the selected gate drive circuit parameters across a range of voltage, current, and temperature conditions. The results were modeled using a combination of experimental curve fitting and the measured  $C_{oss}$  curve, so that the trend with voltage above 400 V could be accurately captured. Eq. (8.6) shows the resulting switching loss model for the Infineon GIT, using the coefficients listed in Table 8.2.

$$E_{sw}(V_{dc}, I_L, T_j) = K_1 I_L^2 V_{dc}^2 + K_2 I_L^2 V_{dc} + K_3 I_L^2 V_{dc} T_j + K_4 I_L V_{dc} + K_5 V_{dc}^2 + K_6 V_{dc} \quad (8.6)$$

This experimental switching loss model is shown in Figure 8.28, compared with the actual experimental results for verification.

In the case of an inverter, this loss must be averaged over a line cycle to calculate the total switching losses, as given in

$$E_{sw,avg} = \frac{1}{\pi} \int_0^{\pi} E_{sw}(V_{dc}, I_L, T_j) d\varphi = \frac{1}{\pi} \int_0^{\pi} E_{sw}(V_{dc}, \sqrt{2} I_g \sin(\varphi), T_j) d\varphi \quad (8.7)$$

where  $I_{grid}$  is the rms current of the inverter load. This integral can be solved as

$$E_{sw,avg} = K_1 I_{grid}^2 V_{dc}^2 + K_2 I_{grid}^2 V_{dc} + K_3 V_{dc} T_j + K_4 \left( \frac{2\sqrt{2}}{\pi} \right) I_{grid} V_{dc} + K_5 V_{dc}^2 + K_6 V_{dc}. \quad (8.8)$$

Other device losses must also be considered, such as conduction loss, driving loss, and reverse conduction loss during dead time. For this analysis, some approximations were made to reduce complexity. The power factor of the inverter was assumed to be unity at the switch-node, and the effects of filter-induced phase offset and ripple current were ignored. To verify that this

Table 8.2. Coefficients for experimental switching loss model of Infineon GIT

| Coefficient | Value                  |
|-------------|------------------------|
| $k_1$       | $3.0 \times 10^{-13}$  |
| $k_2$       | $-8.0 \times 10^{-11}$ |
| $k_3$       | $8.0 \times 10^{-13}$  |
| $k_4$       | $3.5 \times 10^{-9}$   |
| $k_5$       | $9.0 \times 10^{-11}$  |
| $k_6$       | $2.8 \times 10^{-8}$   |

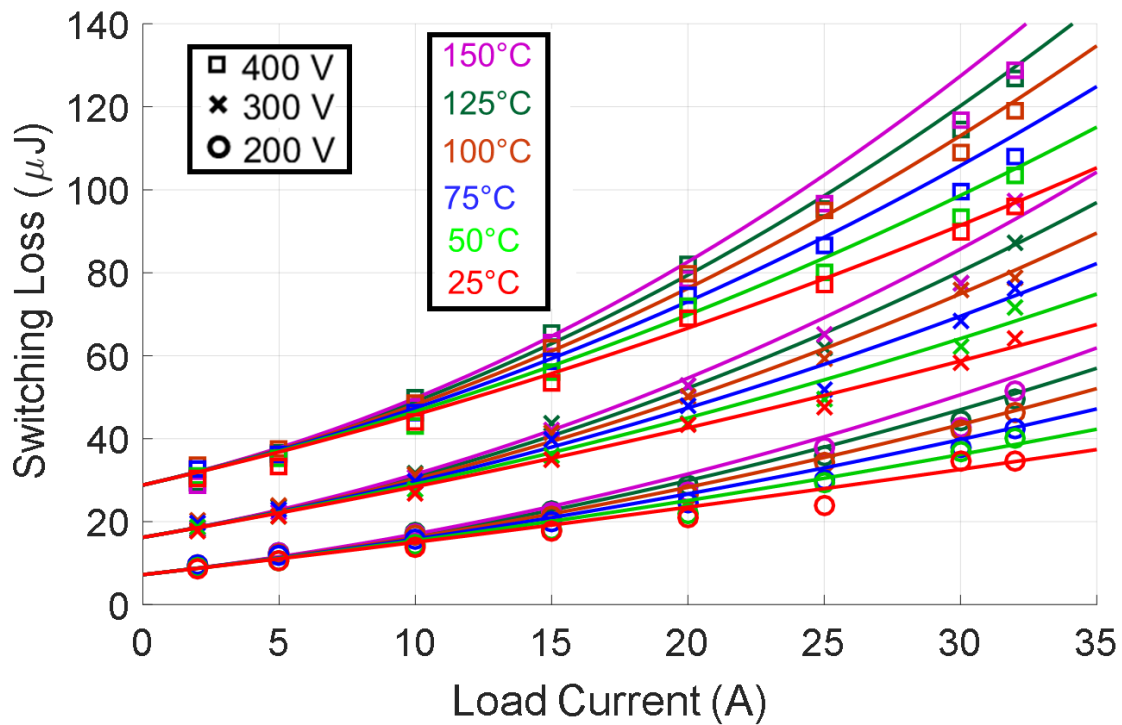


Figure 8.28. Total switching loss as a function of  $I_L$ ,  $T_j$ , and  $V_{dc}$ , based on dynamic characterization of Infineon GIT with the selected gate drive circuit, with the best fit model superimposed on experimental data.

assumption was valid, a more detailed model including ripple current and power factor was implemented for several discrete operating conditions and compared with the simplified model, and the difference was found to be negligible in this design.

Furthermore, the additional losses due to “double switching” when the output current is close to the zero crossing were ignored [250]. The reverse conduction losses in the dead time were estimated based on an assumption that the GIT operates in DLB mode for one half of the 100 ns dead time at the beginning and end of each pulse, which neglects the nonlinear variation of turn-off delay, turn-on delay, and voltage rise time throughout the fundamental cycle.

With these assumptions, the experimental model for switching loss, and the previously reported static characterization data, the total device losses were estimated as follows:

$$P_{hs} = \left(\frac{4M}{3\pi}\right) I_{grid}^2 R_{ds,on} + \frac{1}{2} E_{sw,avg} f_{sw} + P_{drv} \quad (8.9)$$

$$P_{ls} = \left(1 - \frac{4M}{3\pi}\right) I_{grid}^2 R_{ds,on} + P_{dlb} + P_{drv} \quad (8.10)$$

where  $P_{hs}$  and  $P_{ss}$  are the per-device loss in each of the high-side devices and low-side devices, respectively, and the remaining parameters are given by

$$M = \frac{\sqrt{2} V_{grid}}{V_{dc}} \quad (8.11)$$

$$P_{drv} = f_{sw} \left[ \frac{1}{2} Q_g (V_{gs,ss} - V_s) + \frac{1}{4} C_{su} (V_p - V_{gs,ss})^2 \right] + \frac{1}{2} V_{gs,ss} I_{gs,ss} \quad (8.12)$$

$$P_{dlb} = f_{sw} t_{dt} \left( \frac{2\sqrt{2}}{\pi} I_{grid} (V_{th} - V_s) + I_{grid}^2 (R_{sd,rev} - R_{ds,on}) \right) \quad (8.13)$$

where  $R_{ds,on}$  and  $R_{sd,rev}$  are taken from the static characterization results as a function of junction temperature,  $Q_g$  is taken from the device datasheet,  $V_p$  and  $V_s$  are 10 V and -3 V,  $V_{gs,ss}$  and  $I_{gs,ss}$  are 3.5 V and 25 mA,  $C_{su}$  is 470 pF, and the remaining parameters are based on the operating conditions of the converter.



Four combinations of input and output voltages were selected for experimental verification of the prototype inverter. The 450 V dc / 210 V ac condition was not selected, in case the maximum turn-off overshoot voltage was higher than expected at the 34 A peak current case. The 350 V dc / 250 V ac condition was also not selected, as this would result in overmodulation. Some of these parameters are dependent on junction temperature, which were estimated iteratively based on an initial thermal model. This model was based on specified and estimated thermal parameters as described in the next section, assuming that the junction temperature for all devices must remain below 125 °C for all operating conditions. Figure 8.29 shows the per-device losses calculated from this model based on the initially estimated thermal model.

### 8.5.2 Prediction of worst-case device losses and thermal design requirements

Because of the requirement for natural convection cooling and the necessarily close proximity of the devices to each other on the PCB, all of the devices must share a heatsink.

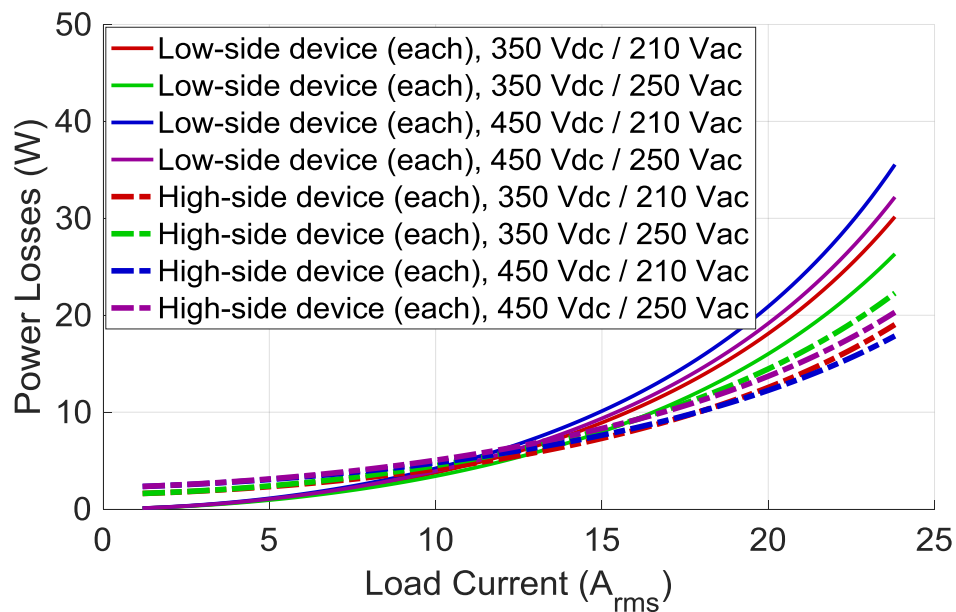


Figure 8.29. Predicted per-device power losses in each switch assuming a worst-case maximum junction temperature of 25 °C.

However, the peak junction temperatures for the hard-switching high-side devices and synchronous-switching low-side devices are not the same. Approximately 50% more loss occurs in the synchronous switches at full load. The junction-to-case thermal resistance of this Infineon GIT is stated at  $1\text{ }^{\circ}\text{C/W}$ . Even assuming no added thermal interface resistance, the synchronous switches would require a maximum case temperature of  $90\text{ }^{\circ}\text{C}$ , indicating that the heatsink thermal resistance for all four switches must be  $0.65\text{ }^{\circ}\text{C/W}$  or less. The addition of an electrically insulating thermal interface pad further reduces the maximum allowable heatsink thermal resistance, which does not leave much room for the conventional bottom-cooled device thermal design.

### 8.5.3 Thermal design for bottom-cooled devices using thermal interface blocks

Based on this initial analysis, the conventional thermal via approach discussed in [107],[108] is not sufficient to cool the devices under the worst-case operating conditions. With the Infineon GIT's thermal pad size of approximately  $0.5\text{ cm}^2$ , these references indicate that the resistance of the PCB vias alone would likely be greater than  $5\text{ }^{\circ}\text{C/W}$  per device.

On the other hand, the copper inlay approach demonstrated by [109] specifies a total thermal resistance of  $0.56\text{ }^{\circ}\text{C/W}$  for two devices, including thermal interface material. A similar approach was taken in this converter design, although it was heavily modified to improve thermal performance and provide flexibility in prototyping. Figure 8.30 and Figure 8.31 show the proposed thermal design that was implemented in the prototype. Rather than a copper PCB inlay, the PCB was designed with a rectangular cutout beneath the thermal pad of the GIT. Since the thermal pad is also shared with the source pad of this GIT's TOLL package, the dimensions of the cutout were selected as 10 mm by 6 mm, allowing enough space on the top side of the PCB to solder the drain, source, gate, and source sense pads. Copper thermal interface blocks (TIBs) were designed and fabricated in a precision machine shop, acting as thermal standoffs between the bottom of each device and the top surface of the heatsink, as well as heat spreaders to improve the vertical heat

flow. The top of the block matches the size of the PCB cutout and GIT thermal pad, while the bottom surface is flanged to the larger size of 10 mm by 25 mm. The total height of the TIB is 6 mm, ensuring at least 4 mm of clearance between the heatsink and PCB, and allowing for use of the bottom side of the PCB to improve the gate drive circuit layout. The PCB was also designed with unplated drill holes on the drain and source side of each device, aligned with smaller diameter holes in the TIBs. The holes in the TIBs can be used to clamp them to the heatsink with 2-56 threaded insulating screws and matching holes drilled and tapped into the heatsink. These screws can either be fully insulated high-temperature plastic (PTFE) or brass with insulating shoulder washers, depending on the amount of torque required. The holes in the PCB act as pass-throughs for inserting and removing the screws for heatsink assembly and disassembly, after the PCB, devices, and TIBs are all soldered together. To make assembly and rework of the prototype feasible by hand, the GITs were soldered to the PCB with lead-free solder, and the TIBs were then soldered to the bottom side of the GITs using lead solder. Lead-free solder melts at 217 °C and can be reflowed at 250 °C, whereas lead solder melts at 183 °C and can be reflowed at 210 °C, so the TIB can be soldered to the bottom of the GITs without desoldering the GITs from the PCB.

The thermal interface material was selected as 0.5 mm TGX from t-Global Technologies, which has a specified thermal resistance of 0.1 °C-in<sup>2</sup>/W with 15 psi of compression, and 0.05 °C-in<sup>2</sup>/W with 100 psi of compression. With the most conservative assumption of only 15 psi compression possible in this design, this results in a thermal resistance of 0.26 °C/W per device.

An additional 0.3 °C/W is estimated for the TIB, based on the ~400 W/m-K thermal conductivity of copper [251]. This is also a conservative estimate, as it neglects the heat spreading effect of the flanged TIB. Using these estimates and the calculated device losses, the required heatsink thermal resistance was then calculated as 0.56 °C/W for all four devices. The calculated junction temperatures across the operating range of the converter are given in Figure 8.32, using

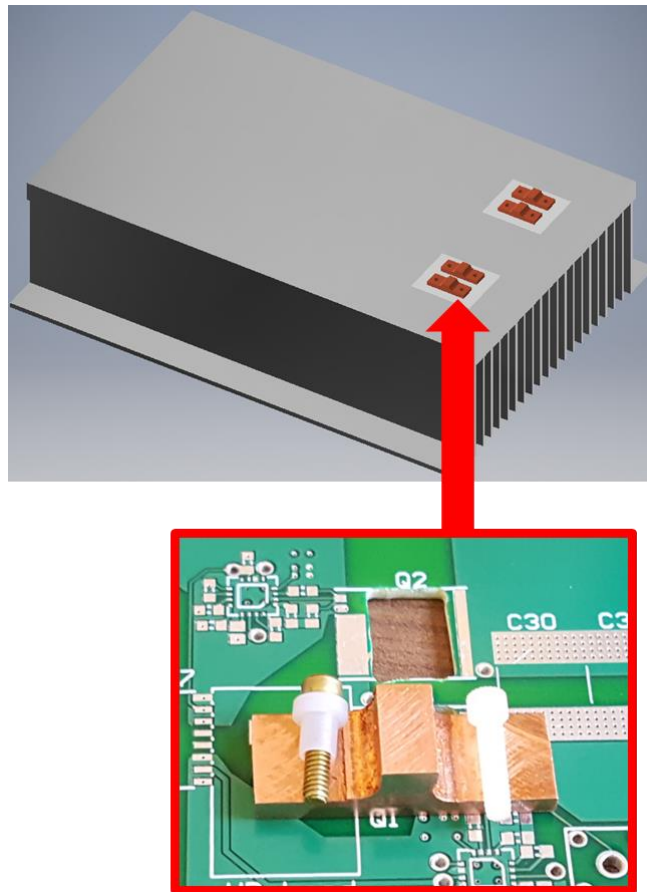


Figure 8.30. Thermal design for bottom-cooled GaN GITs with natural convection cooling, with copper TIBs that are attached to the heatsink with thermal interface material and insulating screws or washers.

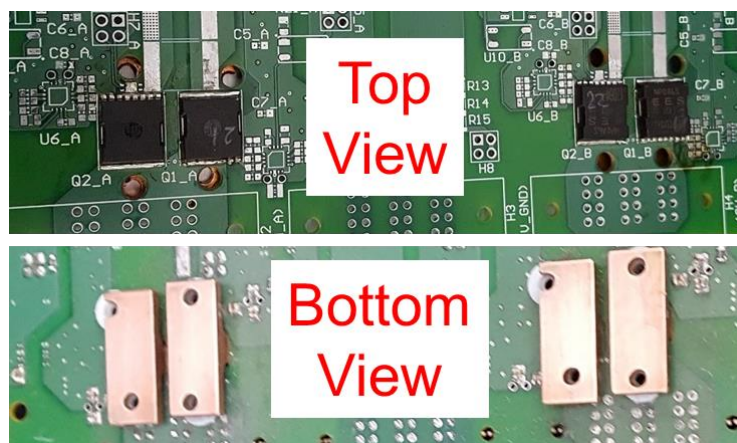


Figure 8.31. Power stage board with copper TIBs soldered to bottom of Infineon GITs through PCB cutouts.

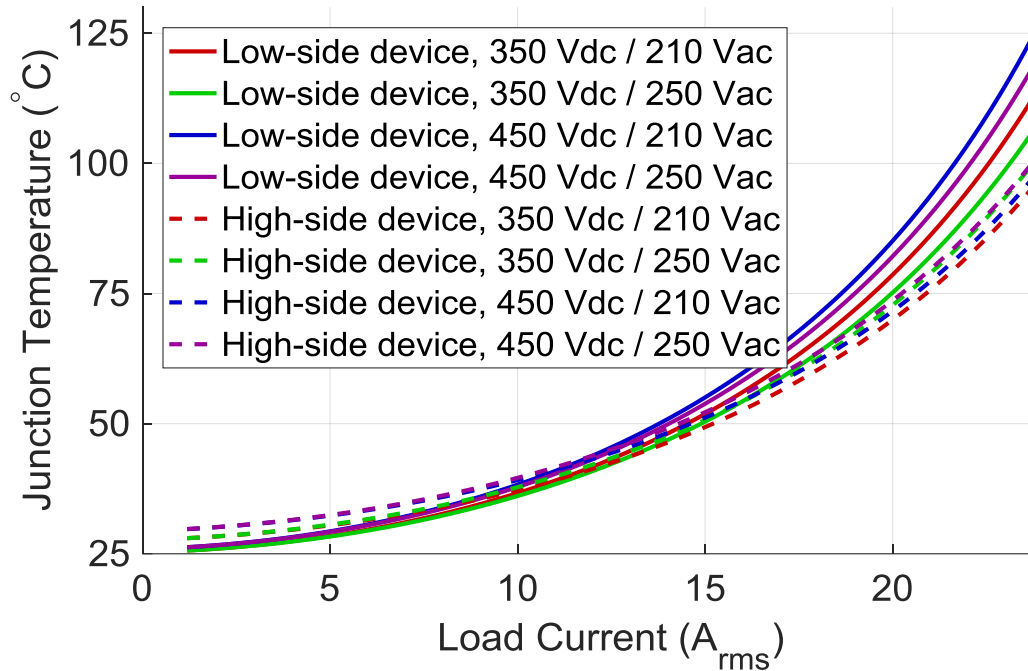


Figure 8.32. Predicted junction temperatures, with the calculated maximum allowable heatsink thermal resistance of  $0.43\text{ }^{\circ}\text{C/W}$ , specified thermal resistances for  $R_{\theta jc}$  ( $1.0\text{ }^{\circ}\text{C/W}$ ) and TGX thermal interface material ( $0.26\text{ }^{\circ}\text{C/W}$ ), and  $0.3\text{ }^{\circ}\text{C/W}$  estimated for copper TIB.

this maximum required heatsink thermal resistance. A survey of commercially available heatsinks for natural convection resulted in selection of an aluminum bonded fin heatsink for the first prototype: Aavid 477000, with a specified thermal resistance of  $0.22\text{ }^{\circ}\text{C/W}$  in natural convection.

## 8.6 Converter architecture and power stage board design

A prototype was constructed to implement the proposed inverter design, including a main power stage board, filter board, interface board, control board, and solid-state circuit breaker (SSCB) board. The scope of this work includes the power stage board and thermal design. The power stage board and overall converter architecture are shown in Figure 8.33 and Figure 8.34, respectively.

The interface board was designed with hardware and software protection for dc and over-voltage, ac over-current, and over-temperature. The temperature was monitored on the power stage, using sensors mounted to the two low-side switches. These switches are likely to be hotter than the high-side switches due to the much higher conduction loss, and the position of their source terminal at the stable  $-V_{dc}$  node makes them more convenient for online temperature sensing.

The control board was a DSP evaluation board from TI, docked vertically to the interface board to generate PWM signals and implement open-loop control. The initial power stage design did not include the proposed device-level protection circuit, so a SSCB was connected externally between the dc capacitors and decoupling capacitors to implement shoot-through protection. The breaker board uses a desaturation protection scheme for an IGBT that can block the current from the dc capacitors. The conduction loss due to this dc breaker is not considered as part of the total loss of the converter, and this board was removed during thermal steady-state testing of the inverter loss and temperature.

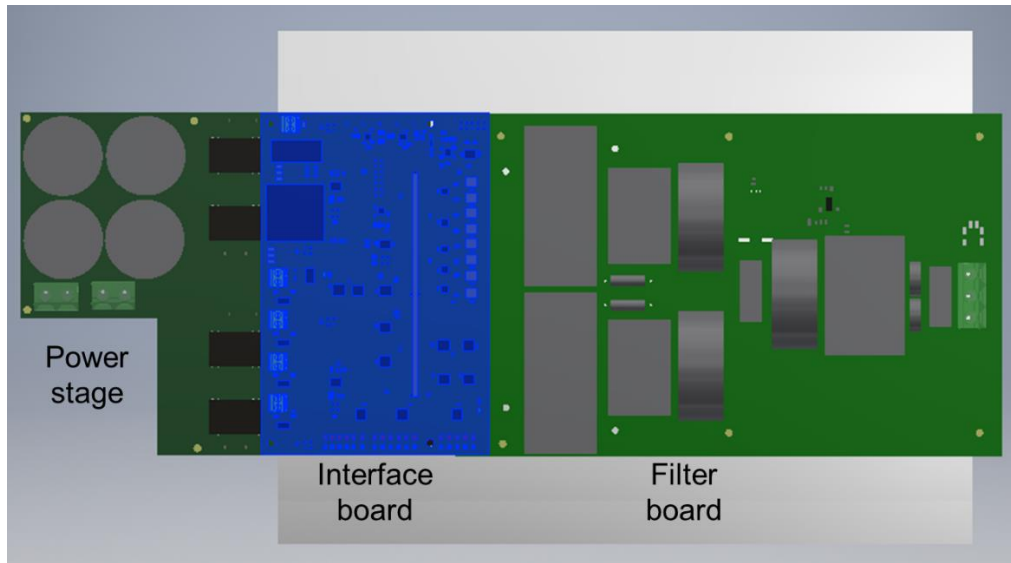
## 8.7 *Experimental characterization of thermal design*

The initial device loss measurements and temperatures were much higher than predicted by the model, partly because the thermal resistances were only estimated in the first version of the model. The thermal design was experimentally characterized using the methodologies presented in Section 2.7 to improve the accuracy of this model and identify key limiting factors.

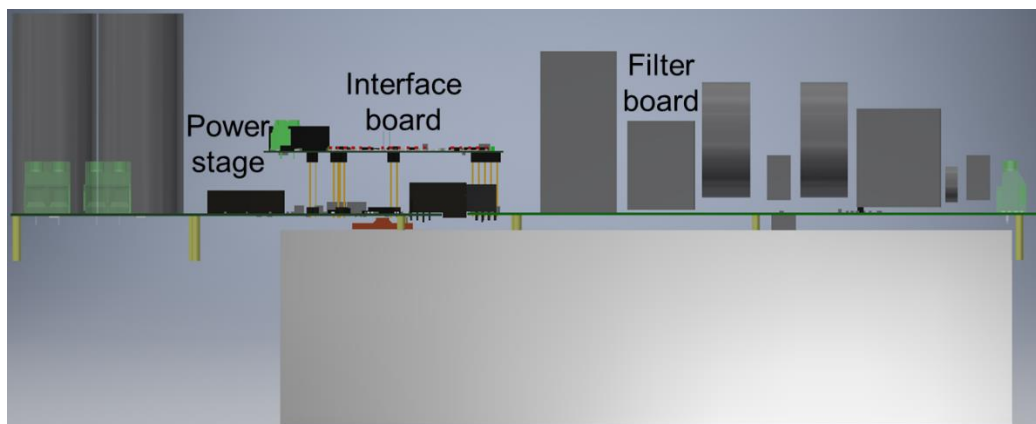
### 8.7.1 *Thermal equivalent circuit*

The thermal equivalent circuit for a single device is shown in Figure 8.35 (a). This circuit includes two stray thermal resistances: the thermal path from junction to ambient through the plastic encapsulant on the top side of the device package,  $R_{\theta,jea}$ ; and the thermal path from case to ambient through any exposed metal of the source-connected thermal pad on the bottom side of the package,  $R_{\theta,ca}$ . These two stray thermal resistances are typically negligibly large compared to the other

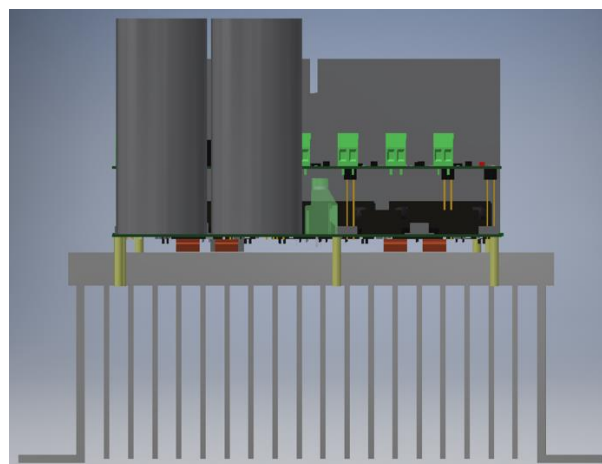
Figure 8.33. 3D model of power stage board, top view.



(a)



(b)



(c)

Figure 8.34. 3D model of converter architecture, (a) Top view, (b) Front view, (c) side view.



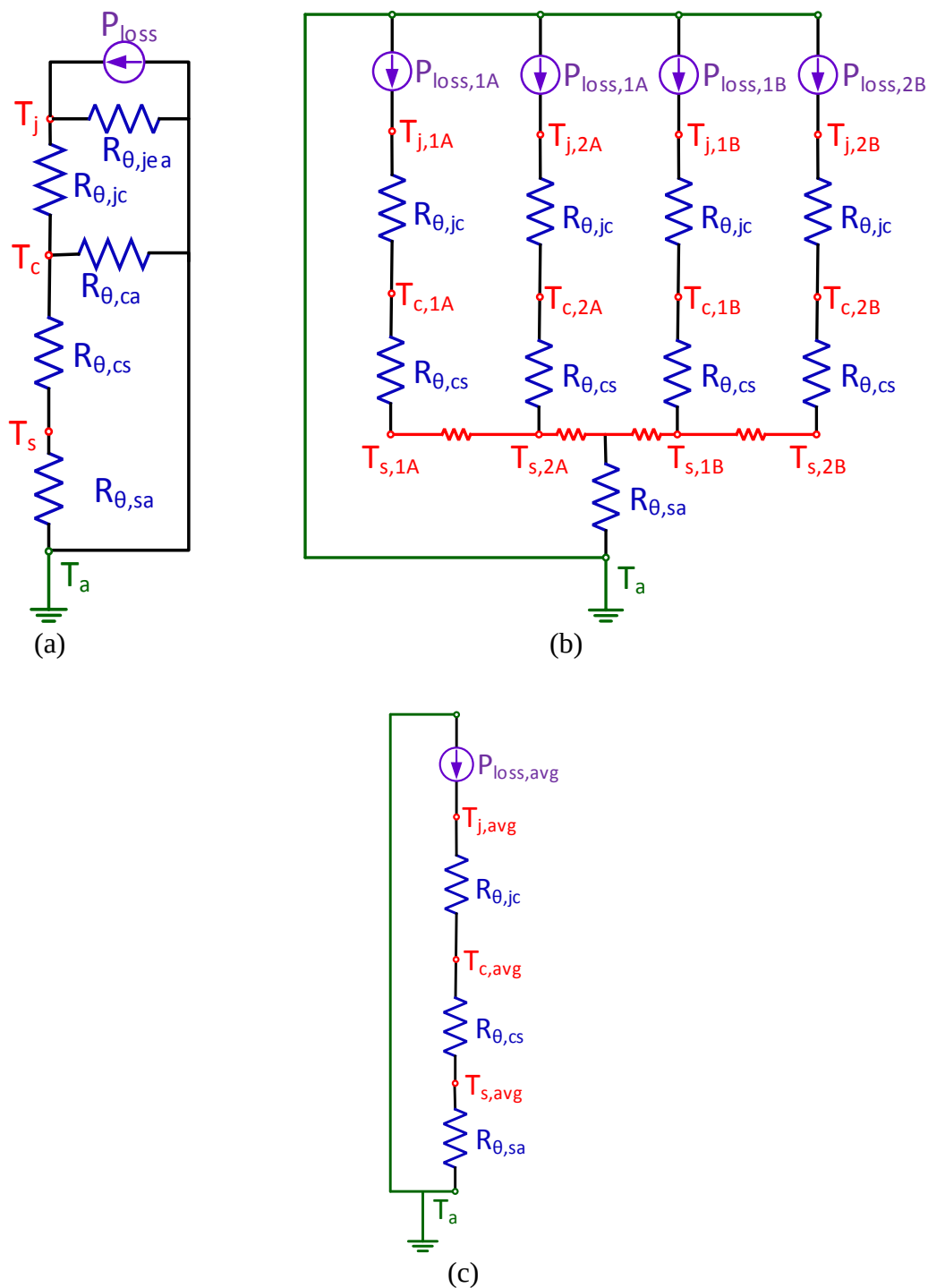


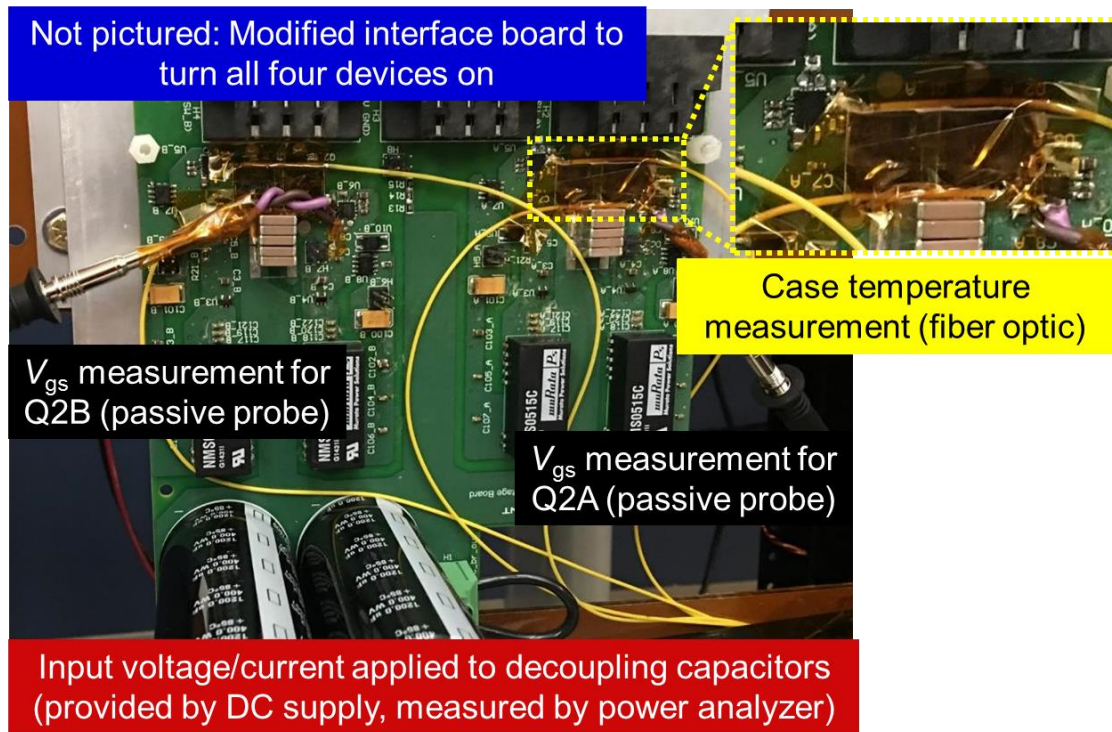
Figure 8.35. Thermal equivalent circuits considered in experimental characterization: (a) theoretical model for a single device with all thermal paths considered; (b) model for full-bridge converter with shared heatsink, simplified by eliminating high-resistance paths; (c) further simplified model for full-bridge with all four devices experiencing the same power dissipation.

parameters in the equivalent circuit. Figure 8.35 (b) shows the model for a full-bridge inverter with these stray resistances ignored.

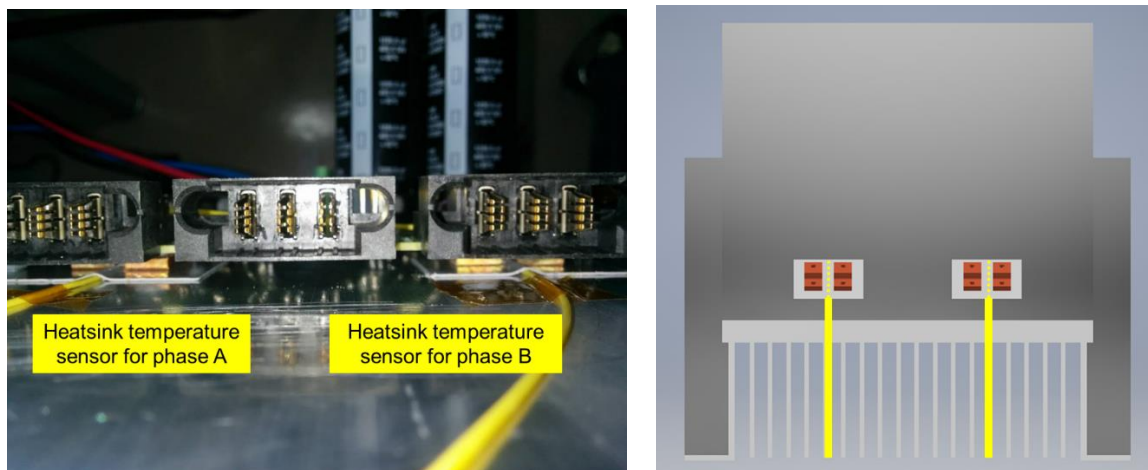
The heatsink was initially modeled as four independent temperatures, representing the locations directly beneath each of the four switches. Finally, Figure 8.35 (c) shows a simplified model with a single heatsink temperature and each switch assumed to experience an equal power loss, junction temperature, case temperature, and associated thermal resistances. This lumped average thermal model is not directly applicable to the inverter in operation, because the power losses are not equivalent for the high-side and low-side switches. However, this average model can be used to experimentally characterize the thermal resistances  $R_{\theta_{jc}}$ ,  $R_{\theta_{cs}}$ , and  $R_{\theta_{sa}}$ .

### 8.7.2 Methodology and test setup

The inverter was modified in order to closely emulate the average model of Figure 8.35 (c), by turning all four switches on simultaneously and providing a constant voltage to the dc input terminals shared by both phase legs. Assuming that all thermal resistances are identical, this provides an equally distributed power dissipation in all four devices, the sum of which can be measured by a power analyzer. Because these thermal resistances may not be exactly the same, the temperatures were measured for each device and averaged to minimize error. Figure 8.36 shows the test and measurement setup for this experimental characterization. The case temperatures and heatsink temperatures were measured using a fiber optic temperature monitoring system from Omega Instruments with six probes. Four probes were adhered to the source terminal of the switches, which are thermally connected to the device case. The two remaining probes were inserted beneath the TGX thermal interface material, between the copper TIBs of each phase leg. Two additional temperature measurements were made using thermocouples in free air on the left and right sides of the heatsink, to account for variations in ambient temperature during the test.



(a)



(b)

Figure 8.36. Test setup for experimental characterization of thermal equivalent circuit parameters; (a) Measurements for case temperature, gate voltage, on-resistance, and power dissipation; (b) Measurements for heatsink temperature.

The average junction temperature was calculated using two different temperature-sensitive electrical parameters (TSEPs). First, the on-resistance was measured using the power analyzer, since the four switches were connected in series and parallel such that the overall circuit resistance is equivalent to the average  $R_{ds,on}$  of each. A resistance of 1 m $\Omega$  was subtracted from the measured  $R_{ds,on}$  to account for stray resistance in the PCB traces and connectors. The temperature was then calculated from  $R_{ds,on}$  using the static characterization given in Figure 4.8. This relationship can be described by

$$T_j = (2.273 \times 10^3) R_{ds,on} - 100 \text{ [}^\circ\text{C]} . \quad (8.14)$$

Next, the gate voltages of the two low-side switches were measured using passive probes and an oscilloscope. Figure 7.4 describes the slope of steady-state gate voltage with junction temperature with the designed gate current of 25 mA. Because this relationship is most sensitive with zero drain current, the gate voltage was recorded for each low-side switch by momentarily turning off the high-side switch in its phase leg, thereby reducing its drain current to zero without turning it off. To avoid ground loop issues, only one passive probe was connected to the oscilloscope at any time. The gate voltage was recorded over ten seconds for each switch, then the junction temperature was calculated using

$$T_j = (490)(V_{gs,cal} - v_{gs}) + T_{j,cal} \text{ [}^\circ\text{C]} \quad (8.15)$$

where  $V_{gs,cal}$  is the gate voltage recorded for the given switch, using the same oscilloscope and probe, before testing began and the junction temperature was assumed to be equal to the ambient temperature  $T_{j,cal}$  recorded at that time. The recorded  $v_{gs}$  waveforms were converted to junction temperatures as shown in Figure 8.37 and Figure 8.38.

Six conditions were tested, with 6 - 30 W of power dissipation per device, and at least one hour given for the test setup to reach thermal steady-state in each condition.

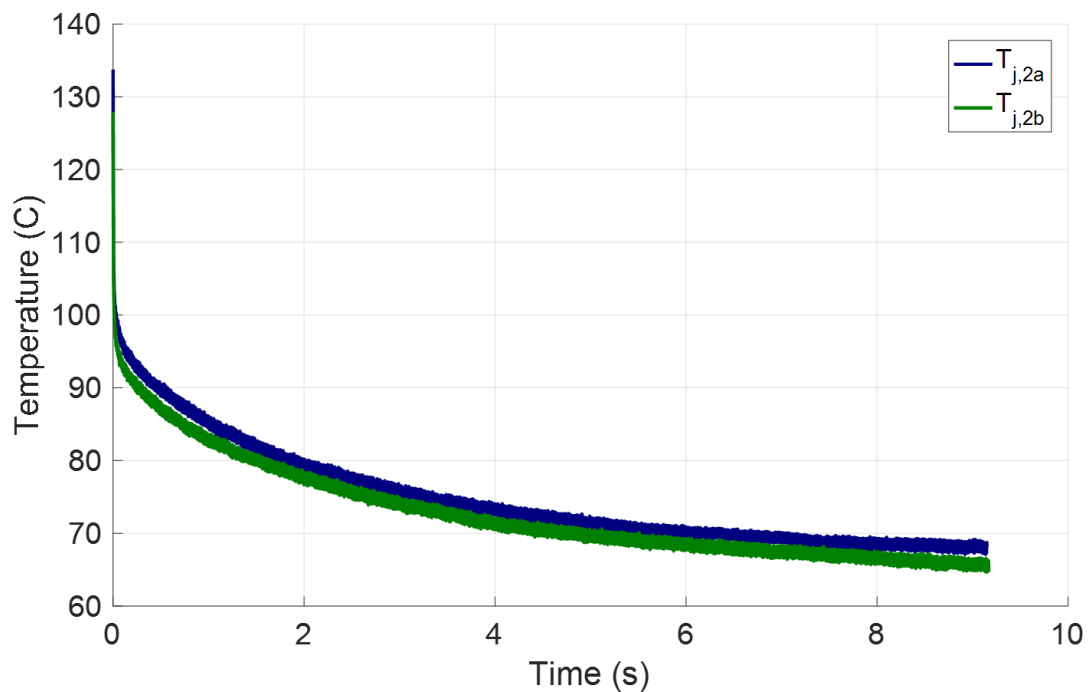


Figure 8.37. Junction temperatures calculated using gate voltage measurements shown as a function of time for 9 s after power dissipation is suddenly dropped from 30 W to 0 W.

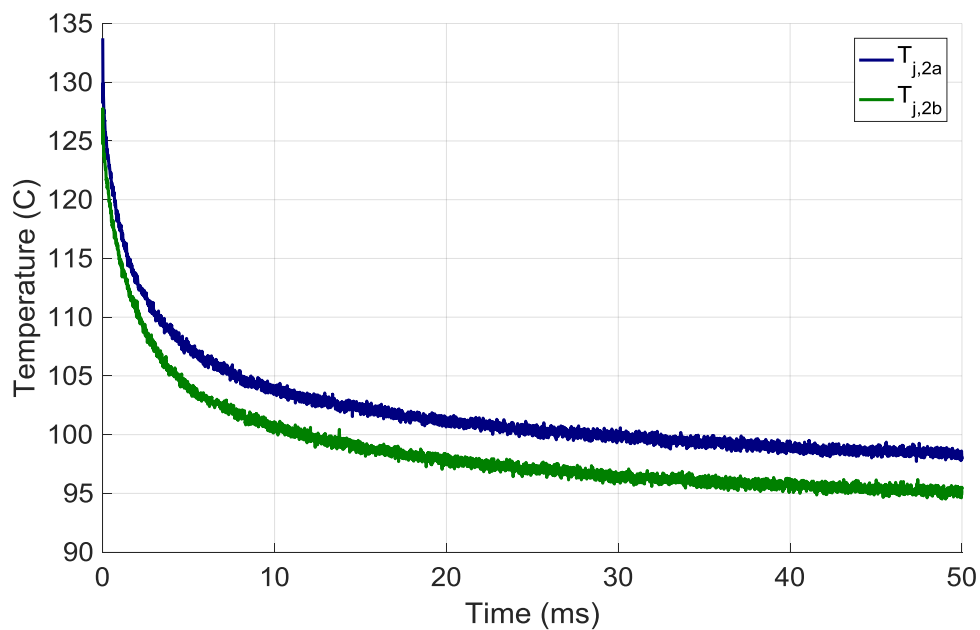


Figure 8.38. Junction temperatures calculated using gate voltage measurements, shown as a function of time for 50 ms after power dissipation is suddenly dropped from 30 W to 0 W.

### 8.7.3 Thermal resistance calculations

The thermal resistances shown in Figure 8.35 can be calculated for each power dissipation condition according to

$$R_{\theta,jc} = \frac{T_{j,avg} - T_{c,avg}}{P_{diss,each}} \quad (8.16)$$

$$R_{\theta,cs} = \frac{T_{c,avg} - T_{s,avg}}{P_{diss,each}} \quad (8.17)$$

$$R_{\theta,sa} = \frac{T_{s,avg} - T_{a,avg}}{P_{diss,total}} . \quad (8.18)$$

Prior literature described in Section 2.7 indicated that these parameters are not directly correlated to power. Rather, the junction-to-case thermal resistance is related to the junction temperature, and the heatsink-to-ambient thermal resistance is related to the heatsink temperature rise (the difference between ambient and the maximum heatsink temperature). The case-to-heatsink thermal resistance was expected to be relatively constant based on literature surveyed.

The  $v_{gs}$ -based  $T_j$  waveforms provide an opportunity to calculate the complex thermal impedance of the circuit rather than only the steady-state resistances. The case and heatsink thermal impedances have time constants that are relatively long compared to the junction, which typically includes multiple components with ms-scale time constants related to the layers of the die and the packaging. These shorter time constants may have a significant impact on the loss model, so it is useful to extract them from the overall thermal impedance of the circuit.

Oscillation in the  $v_{gs}$ -based  $T_j$  waveforms was damped out within 80  $\mu$ s after the high-side switches were turned off. However, the drop during this time varied with the power dissipation. Therefore, the junction temperature and complex thermal impedance from this measurement were calculated by applying an exponential curve fit to each waveform for the first 500 ms after the power dissipation was dropped to 0 W. Four exponential terms were identified in this curve fitting procedure, which were calculated using MATLAB according to

$$T_j = T_0 + P_{diss} \left( R_{\theta 1} e^{-\frac{t}{R_{\theta 1} C_{\theta 1}}} + R_{\theta 2} e^{-\frac{t}{R_{\theta 2} C_{\theta 2}}} + R_{\theta 3} e^{-\frac{t}{R_{\theta 3} C_{\theta 3}}} + R_{\theta 4} e^{-\frac{t}{R_{\theta 4} C_{\theta 4}}} \right). \quad (8.19)$$

Figure 8.39 and Figure 8.40 show the four RC components modeled by this curve fitting, including components with time constants from 1 s to 1 ms. The first component,  $R_{\theta 1}$ , was assumed to be a component of the case-to-heatsink thermal impedance because of its relatively long time constant of  $\sim 1$  s. The second and third components were estimated as constant thermal resistances of 0.2 and 0.4 °C/W with time constants of 30 ms and 4 ms, indicating thermal capacitances of 0.2 and 0.01 W-s/°C. The fourth component with the shortest time constant was calculated as a variable resistance, increasing from 0.1 to 0.6 °C/W over the measured range. This resistance was modeled as

$$R_{\theta 4} = (0.004)T_j \quad (8.20)$$

with a thermal capacitance of 0.003 W-s/°C. The steady-state junction temperature was calculated for each condition as (8.19) with  $t = 0$ . These  $v_{gs}$ -based temperature calculations matched very closely with the  $R_{ds,on}$ -based calculations using (8.16), as shown in Figure 8.42.

The total steady-state junction-to-case thermal resistance was then calculated as the sum of components  $R_{\theta 2}$ ,  $R_{\theta 3}$ , and  $R_{\theta 4}$ , shown in Figure 8.41. This calculation matched relatively well with the specified thermal resistance of 1 °C/W provided by the manufacturer. The steady-state case temperature was calculated from this curve fitting as

$$T_c = T_0 + P_{device} R_{\theta 1}. \quad (8.21)$$

The calculated case temperatures for both phase legs matched well with the measured case temperature for phase B, but the measured phase A case temperature was lower than these other values. Figure 8.43 shows these calculations for phase legs A and B. The thermal resistances of phase A and B appeared to be different if each component is considered individually, however the junction temperature and ambient temperature was the same for both phases. Therefore, either

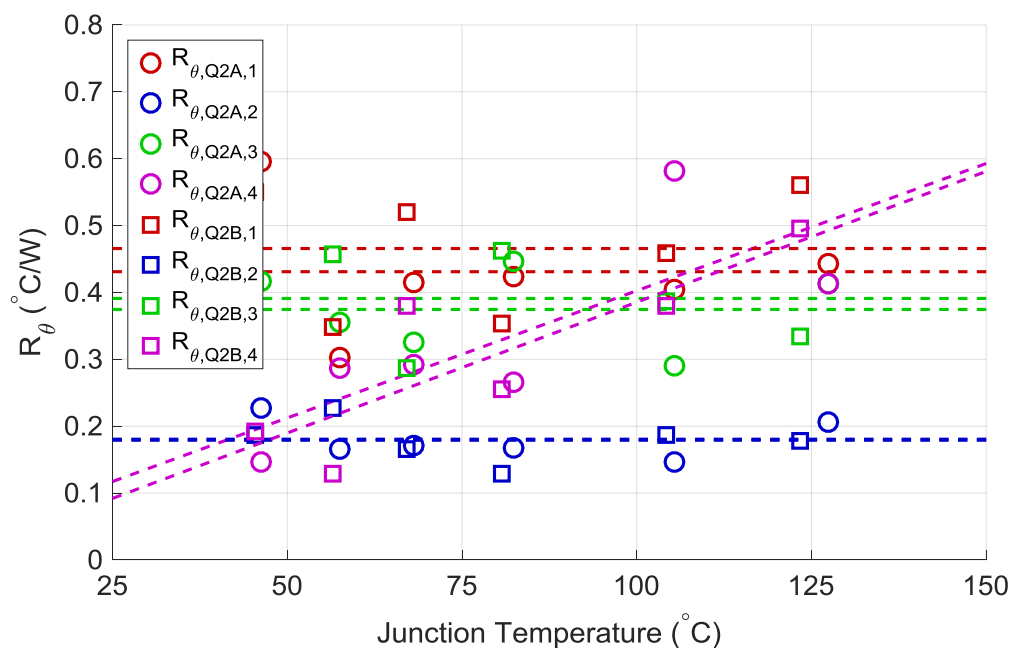


Figure 8.39. Thermal resistance components calculated from the first 500 ms of gate voltage measurements at various power dissipation conditions, shown as a function of peak junction temperature with best-fit lines.

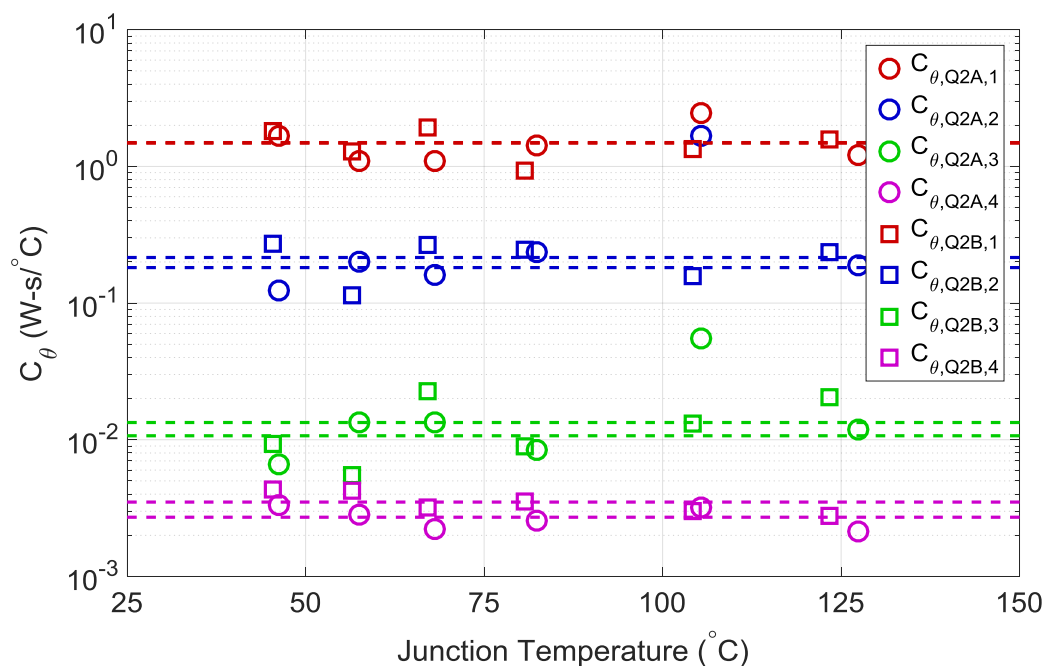


Figure 8.40. Thermal capacitance components calculated from the first 500 ms of gate voltage measurements at various power dissipation conditions, shown as a function of peak junction temperature on a semilog scale with best-fit lines.



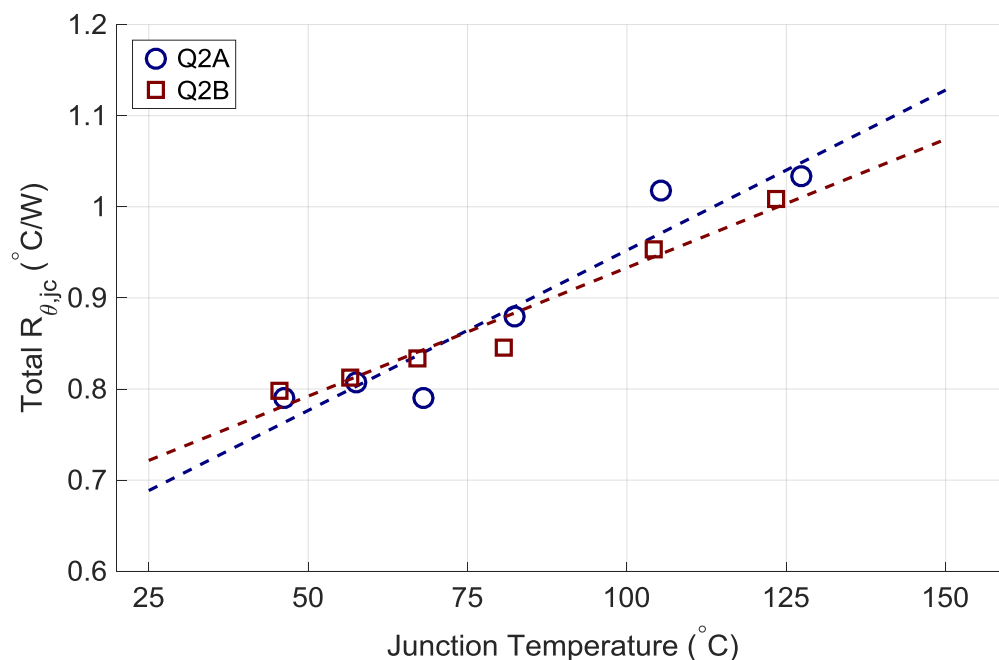


Figure 8.41. Total junction-to-case thermal resistance calculated from the first 500 ms of gate voltage measurements at various power dissipation conditions, shown as a function of peak junction temperature with best-fit lines.

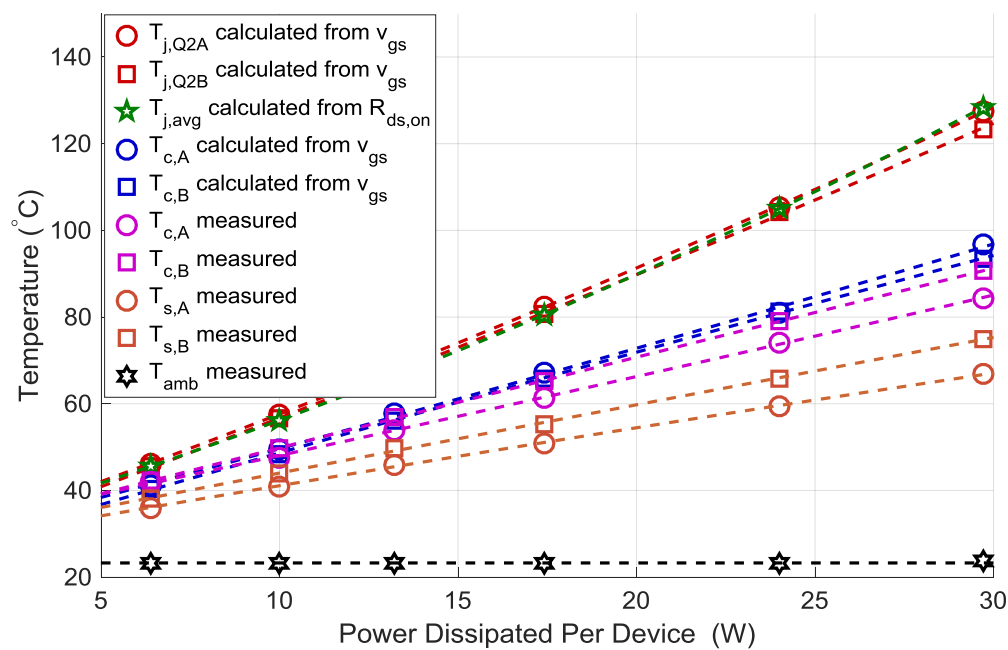


Figure 8.42. Case, heatsink, and ambient temperatures measured using fiber-optic temperature sensors, junction temperatures calculated from on-resistance, and both junction and case temperatures calculated from  $v_{gs}$  waveforms.

phase could be used to accurately model the junction temperature. The phase B case and heatsink temperature measurements were used for calculation of  $R_{\theta,cs}$  and  $R_{\theta,sa}$ , because the measured case temperature matched most closely with  $v_{gs}$ -based calculation. The case-to-heatsink thermal resistance was estimated as approximately 0.6 °C/W, which matches very well with the expected value of 0.56 °C/W from Section 8.5.3.

The heatsink temperature measurements were used to calculate its overall thermal resistance (shared by all four devices) as shown in Figure 8.44, as a function of the heatsink temperature rise  $\Delta T_{sa} = T_s - T_a$ . As with the case temperature, the phase B measurement was used to model this thermal resistance as

$$R_{\theta,sa} = (0.000133)\Delta T_{sa}^2 - (0.0128)\Delta T_{sa} + 0.740 . \quad (8.22)$$

This thermal resistance was only measured up to a temperature rise of 43 °C, where its curve becomes relatively flat near 0.45 °C/W.

## 8.8 *Experimental verification of loss model*

### 8.8.1 *Test setup*

The experimental prototype was operated for an hour or longer at several operating conditions, until it reached thermal steady-state. The prototype was oriented vertically and panel-mounted as shown in Figure 8.45 with nothing obstructing air flow behind, above, or below the heatsink. The input power was provided by an isolated dc supply, and the output was connected an electronic load. Both input and output power were monitored by a power analyzer, with the voltage measurements connected at the screw terminals of the power stage board to avoid as much stray resistance in the measured losses as possible. Temperature measurements were also collected for case and heatsink, as previously described for the thermal resistance characterization steps.

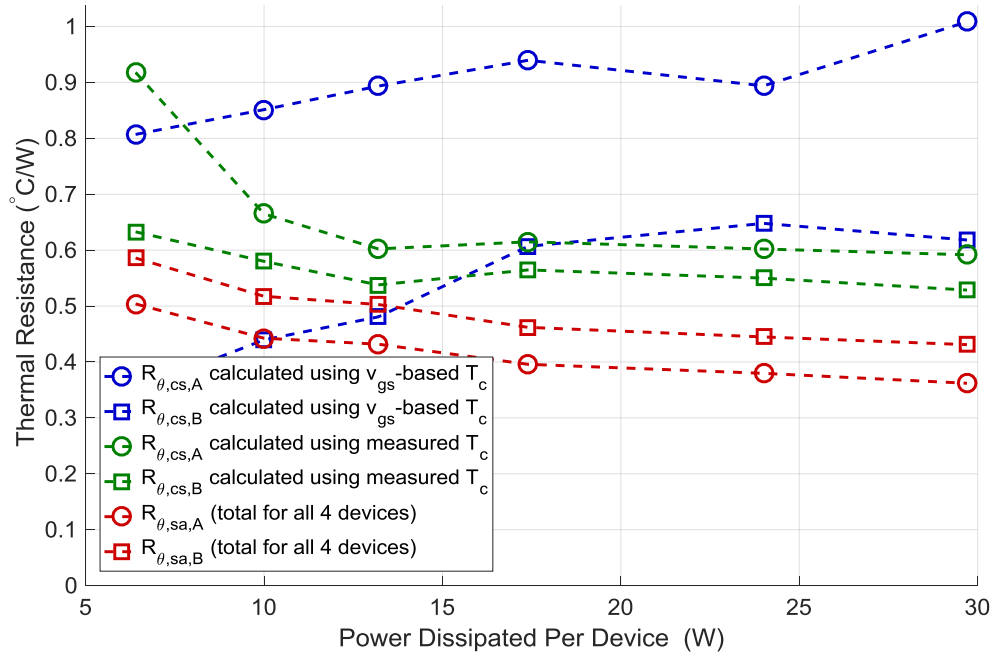


Figure 8.43. Case to heatsink thermal resistance and heatsink to ambient thermal resistance for each phase leg, calculated using various measurements and compared.

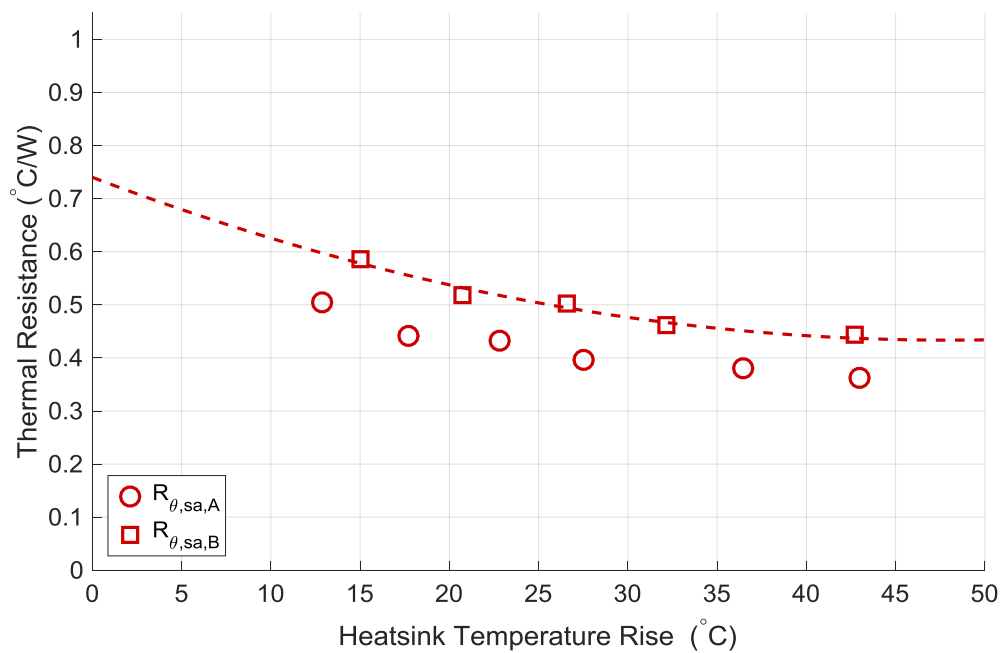


Figure 8.44. Heatsink to ambient thermal resistance calculated using measurements for each phase leg, shown as a function of heatsink temperature rise, with best-fit line for phase B only.

### 8.8.2 Results

The loss breakdown of the prototype is shown in Figure 8.46 at nominal operating conditions of 450 V dc / 230 V ac. All losses that would be measured by the power analyzer were considered, including device losses (switching, conduction, DLB), bleeder resistors on the dc capacitor bank, filter losses (line filter, EMI filter), and any stray resistances (PCB traces, wires, other board components neglected in the loss model). Initially, the stray resistance was measured as approximately 40 m $\Omega$  on the ac side, primarily coming from the ac contactor located on the filter board for hardware protection. However, this does not consider the ac equivalent resistance experienced by the ripple current between the devices and the filter. Therefore, the stray resistance may be slightly higher than 40 m $\Omega$ . Auxiliary control power is also included in this figure, although this was not considered part of the measured power stage loss.

The filter design was outside the scope of this work, and it was implemented and verified prior to the loss model verification testing. The loss of the line filter and EMI filter were calculated using a Saber simulation model as part of that separate work. These calculations were incorporated into the loss model of the inverter with curve-fitting as shown in Figure 8.47.

The results of the loss prediction model are shown in Figure 8.48 - Figure 8.53 for the four tested operating voltage combinations, and across the rms output current range of the inverter, including the device losses, junction temperatures, case temperatures, heatsink temperatures, thermal resistances, and overall power stage losses. In Figure 8.51 - Figure 8.53, the experimental measurements are also plotted for comparison with the model predictions. The measurement tolerance of the power analyzer was included as error bars in these figures, based on the specifications listed in its datasheet.

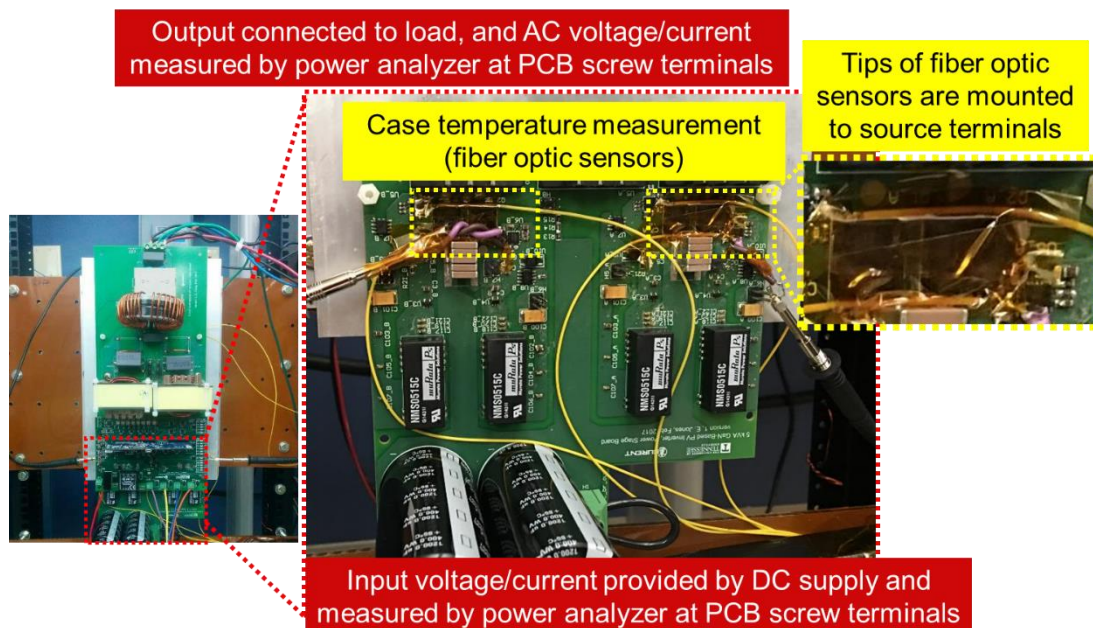
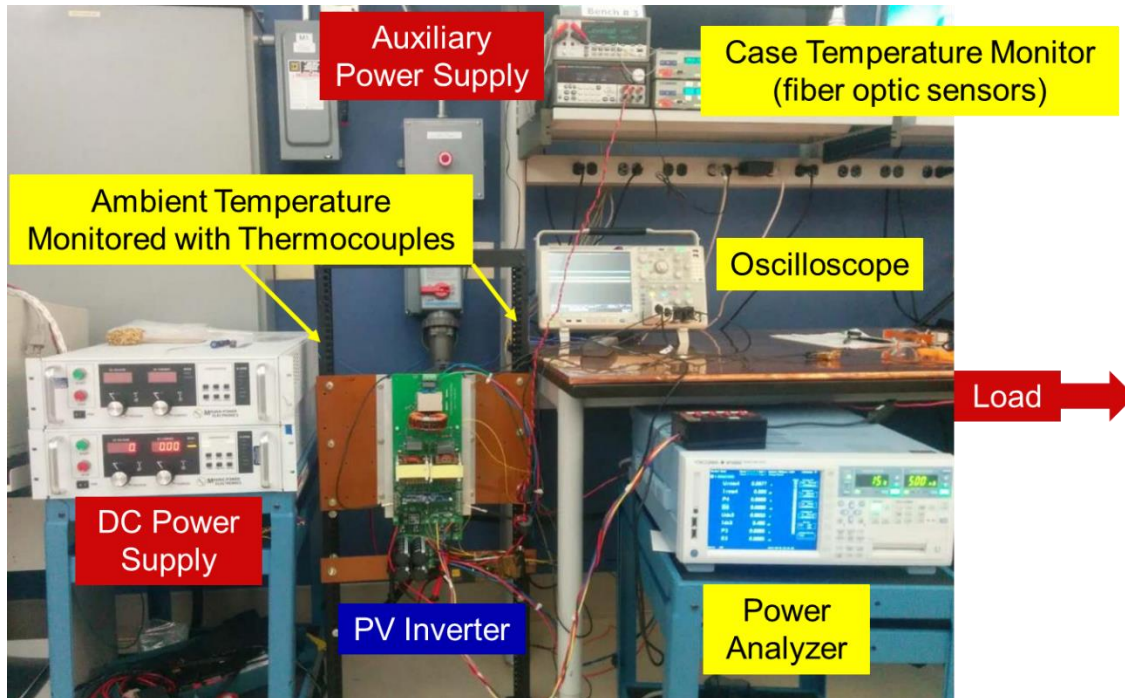


Figure 8.45. Test setup used for experimental characterization of converter loss model in thermal steady-state.

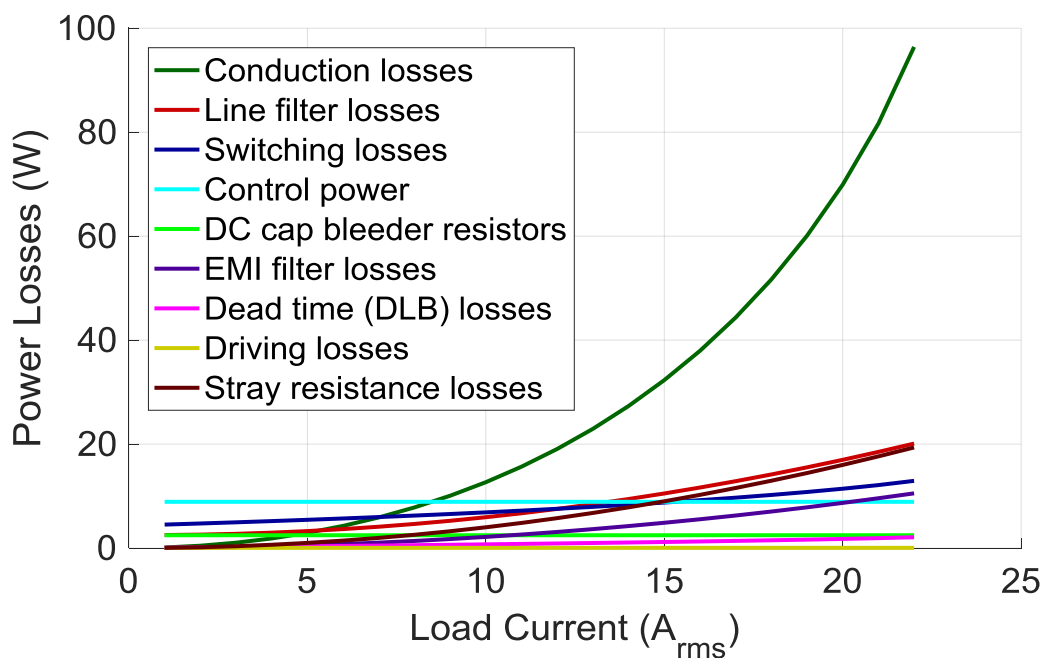


Figure 8.46. Predicted loss breakdown of prototype at nominal operating conditions 450 V dc, 230 V ac, up to full 5 kW loading condition.

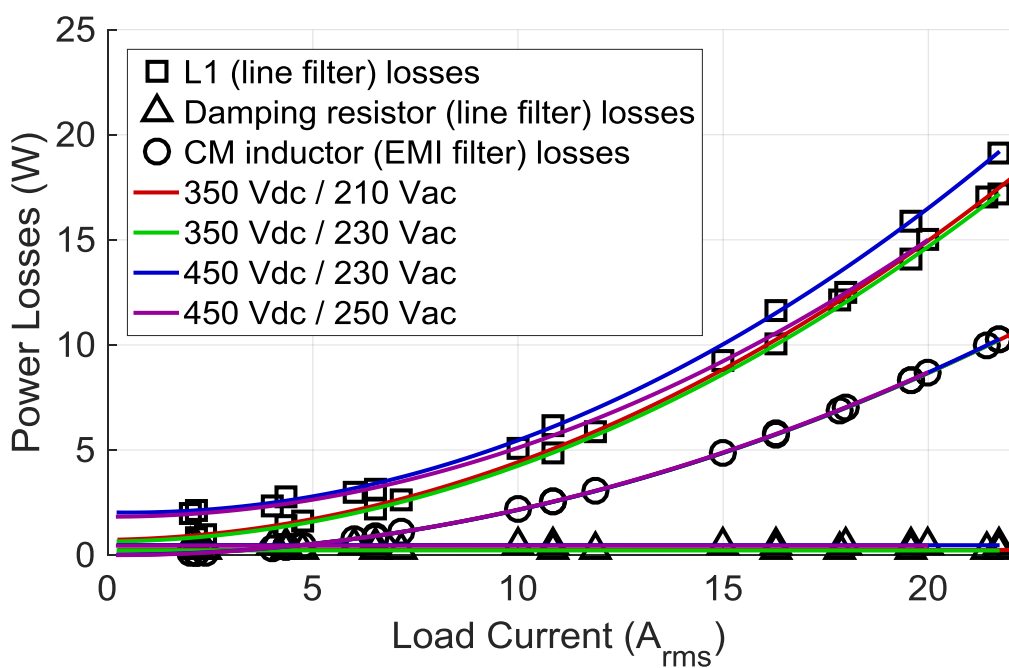


Figure 8.47. Predicted filter losses of prototype at four operating conditions considered in experimental verification, showing values calculated from Saber simulation (out of scope of this work) and best-fit curves used in loss model of converter.

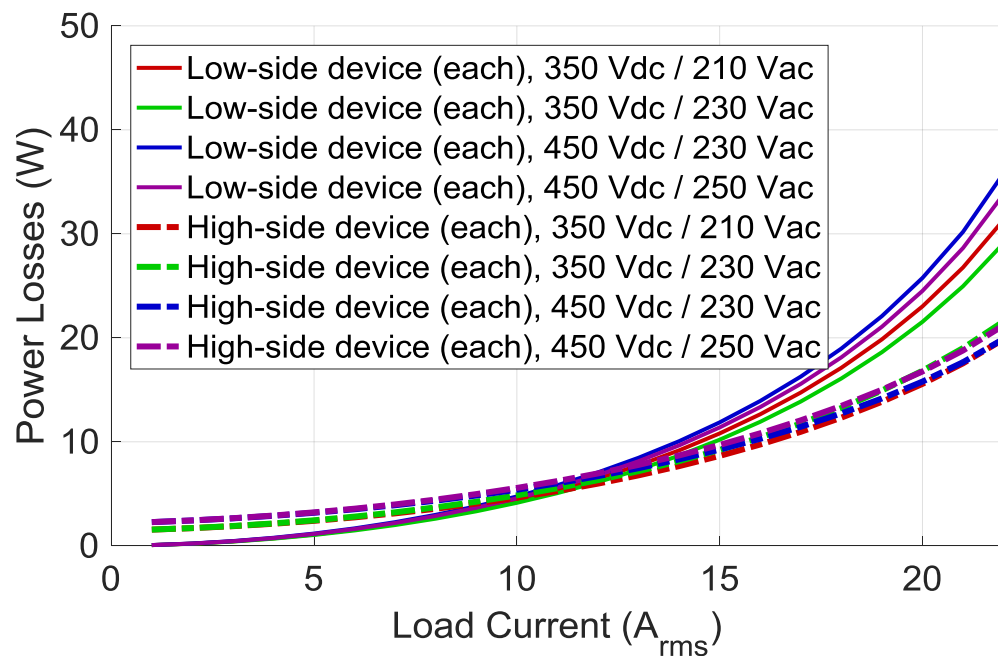


Figure 8.48. Predicted device losses of prototype at four operating conditions considered in experimental verification.

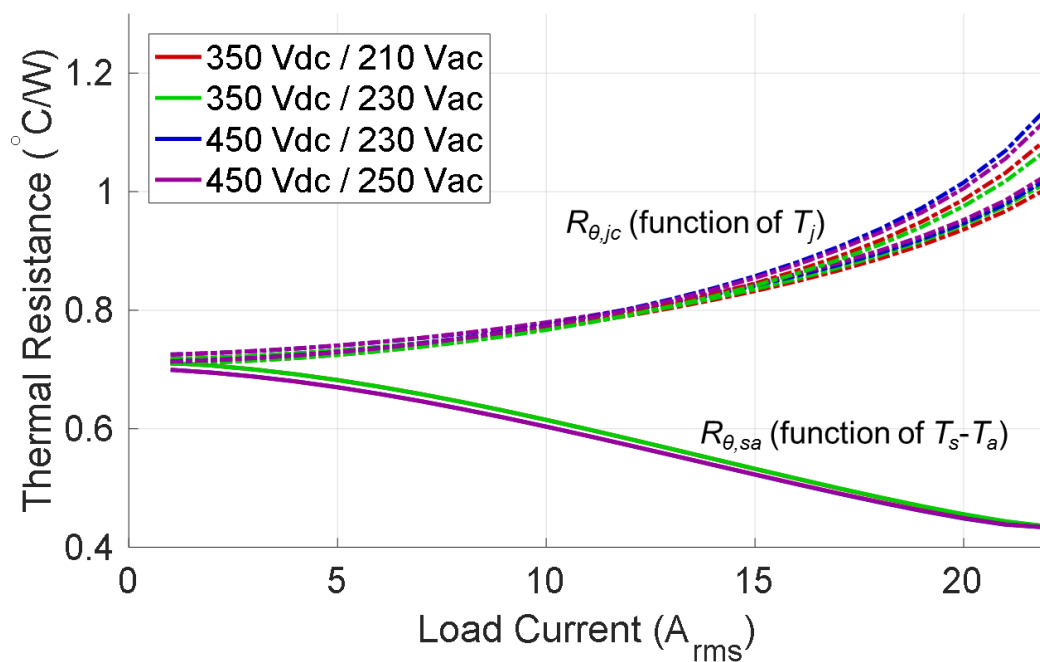


Figure 8.49. Variable thermal resistances used for loss model, based on experimental characterization of thermal model, at four operating conditions considered in experimental verification.

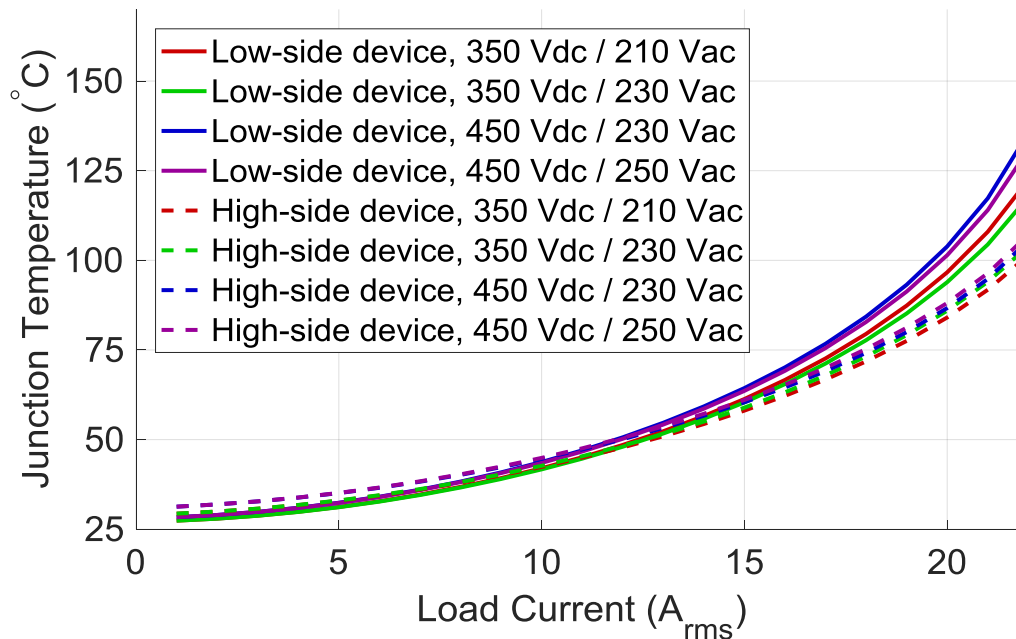


Figure 8.50. Predicted device junction temperatures for prototype at four operating conditions considered in experimental verification.

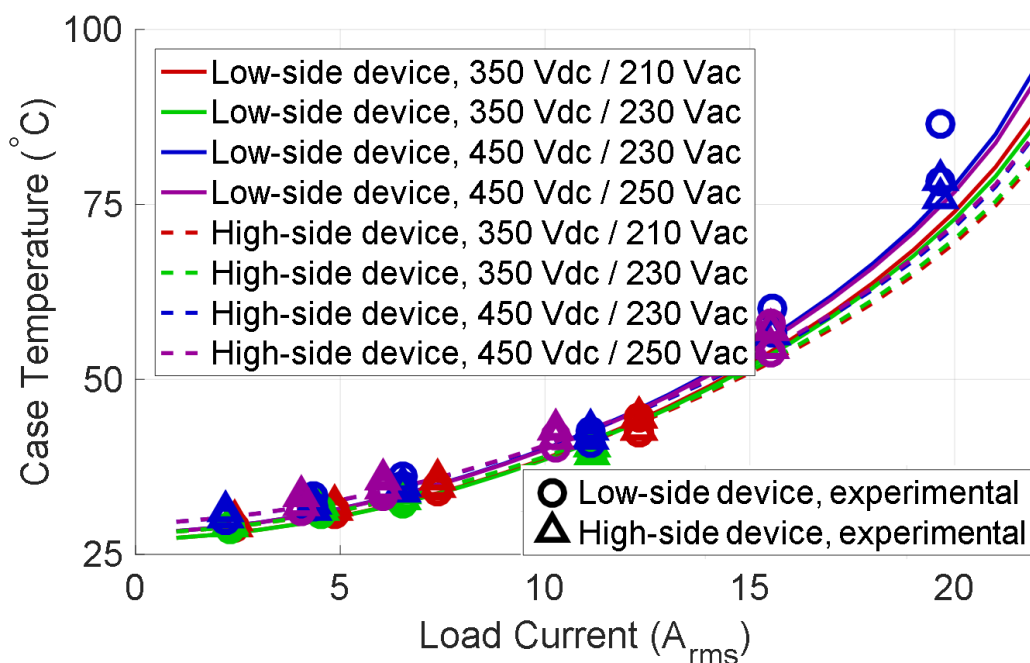


Figure 8.51. Predicted device case temperatures for prototype at four operating conditions considered in experimental verification, with measured values shown for comparison.



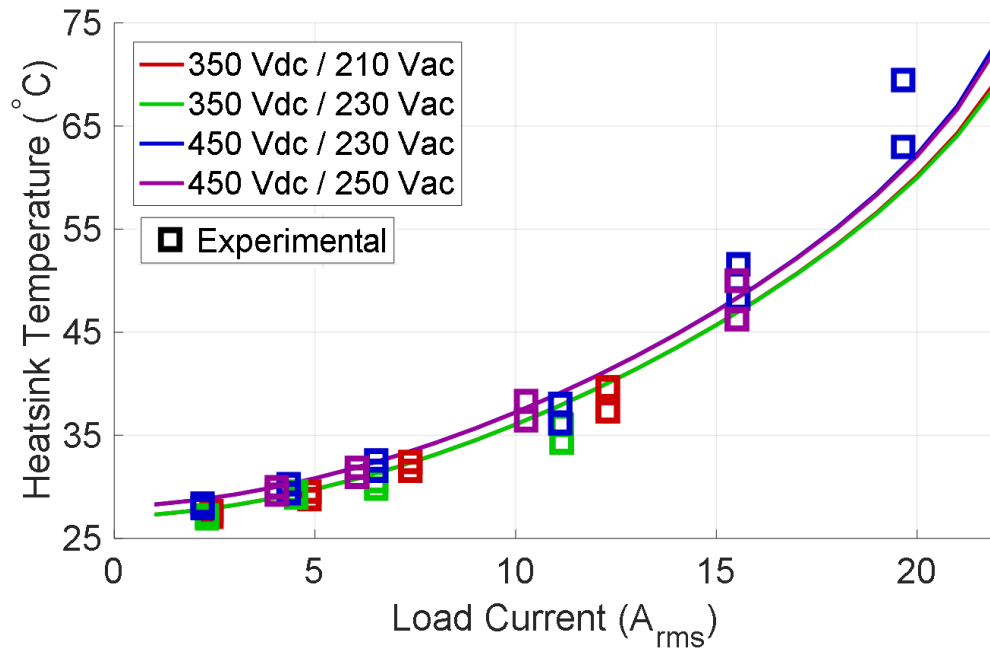


Figure 8.52. Predicted heatsink temperature for prototype at four operating conditions considered in experimental verification, with measured values shown for comparison.

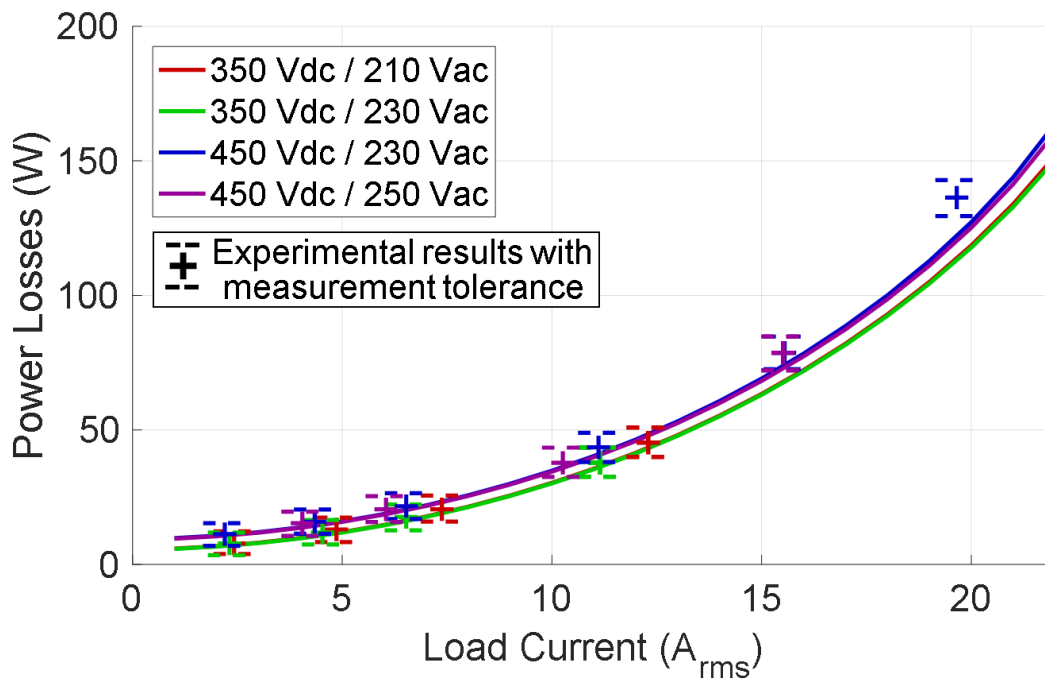


Figure 8.53. Predicted total power stage losses for prototype (all converter loss except auxiliary control power) at four operating conditions considered in experimental verification, with measured values and measurement tolerances (error bars) shown for comparison.

A discrepancy is evident between the loss and temperature measurements and the model predictions, accounting for approximately 10% of the measured power stage loss at 20 A<sub>rms</sub>. The discrepancy in loss could be explained by the underestimated stray resistance or error in the filter loss model, but the temperature discrepancy indicates that at least some of the extra loss is occurring in the GaN devices. The extra loss has an approximately second-order relationship with output current, so it likely stems from underestimated conduction loss (either in the device or stray resistance). In contrast, the model for this inverter's switching loss is proportional to dc voltage, with only a weak first-order relationship to rms current.

Prior literature has shown that dynamic  $R_{ds,on}$  can account for a significantly higher conduction loss than estimated based on the dc characteristics [252-256]. This phenomenon is difficult to characterize, and has not been performed on this GIT with hard switching in the  $< 1 \mu\text{s}$  time scale. The manufacturer presented in [257] that the effective  $R_{ds,on}$  for the Infineon GIT has been verified with soft switching to have less than 5% effective  $R_{ds,on}$  increase within 200 ns of the turn-on transient at 400 V, but the dynamic  $R_{ds,on}$  under hard switching was not tested in that time scale.

The thermal characterization study conducted in Section 8.7 may also explain some of this discrepancy. This showed that the thermal resistance from junction to case includes components with time constants as low as 1 ms. The line cycle is 16.7 ms, and the original loss model assumed that the junction temperature can be treated as a constant based on average power. This assumption is likely valid for calculation of the case temperature and heatsink temperature, both of which have much longer thermal time constants than the line cycle. However, the junction temperature may be varying significantly during the conduction period of each device, and the highest junction temperature likely occurs near the time of heaviest conduction loss. Further experimental study and analysis was necessary to incorporate this into the loss model.

### 8.8.3 Implementation of Dynamic Electro-Thermal Device Loss Model

The complex thermal impedance from the junction to case was incorporated into the inverter loss predictions with a dynamic electro-thermal model. This model was implemented in discrete-time with a step size of 0.5  $\mu$ s in MATLAB, based on the following equations:

$$R_{ds,on} = \frac{1}{2273} (100 + T_j) \quad (8.23)$$

$$T_{jc,2}(t) = T_{jc,2}(t - \Delta t) + \Delta t \frac{dT_{jc,2}}{dt}(t) \quad (8.24)$$

$$T_{jc,3}(t) = T_{jc,3}(t - \Delta t) + \Delta t \frac{dT_{jc,3}}{dt}(t) \quad (8.25)$$

$$T_{jc,4}(t) = T_{jc,4}(t - \Delta t) + \Delta t \frac{dT_{jc,4}}{dt}(t) \quad (8.26)$$

$$\frac{dT_{jc,2}}{dt}(t) = \frac{P_{device}(t) - \frac{T_{jc,2}(t)}{R_{\theta 2}}}{C_{\theta 2}} \quad (8.27)$$

$$\frac{dT_{jc,3}}{dt}(t) = \frac{P_{device}(t) - \frac{T_{jc,3}(t)}{R_{\theta 3}}}{C_{\theta 3}} \quad (8.28)$$

$$\frac{dT_{jc,4}}{dt}(t) = \frac{P_{device}(t) - \frac{T_{jc,4}(t)}{R_{\theta 4}}}{C_{\theta 4}} \quad (8.29)$$

$$T_j(t) = T_c + T_{jc,2}(t) + T_{jc,3}(t) + T_{jc,4}(t) \quad (8.30)$$

$$P_{device,Q1A} = \begin{cases} dI^2 R_{ds,on,Q1A} + E_{sw} f_{sw}, & 0 < \theta < \pi \\ 0, & \pi < \theta < 2\pi \end{cases} \quad (8.31)$$

$$P_{device,Q2A} = \begin{cases} (1-d)I^2 R_{ds,on,Q2A} + f_{sw} t_{dt} (I(V_{th} - V_s) + I^2 R_{ds,on,Q2A}), & 0 < \theta < \pi \\ 0, & \pi < \theta < 2\pi \end{cases} \quad (8.32)$$

$$P_{device,Q1B} = \begin{cases} 0, & 0 < \theta < \pi \\ dI^2 R_{ds,on,Q1A} + E_{sw} f_{sw}, & \pi < \theta < 2\pi \end{cases} \quad (8.33)$$

$$P_{device,Q2B} = \begin{cases} 0, & 0 < \theta < \pi \\ (1-d)I^2 R_{ds,on,Q2A} + f_{sw} t_{dt} (I(V_{th} - V_s) + I^2 R_{ds,on,Q2A}), & \pi < \theta < 2\pi \end{cases} \quad (8.34)$$

$$I(\theta) = \sqrt{2} I_{grid} \sin(\theta) \quad (8.35)$$

$$d(\theta) = \frac{\sqrt{2} V_{grid}}{V_{dc}} \sin(\theta) \quad (8.36)$$

$$t = \frac{\theta}{120\pi} \quad (8.37)$$

Because several of these equations are interdependent, they must be calculated iteratively over the full line cycle until the calculations converge. Figure 8.54 shows one complete line cycle of junction temperatures for all four devices with 450 V dc, 230 V ac, and 20 Arms after 15 iterations of these calculations. Figure 8.55 shows the average values of each device for this line cycle, over the 15 iterations implemented in MATLAB. Convergence is reached within 10 iterations. Figure 8.56 - Figure 8.58 demonstrate the impact of this dynamic model on the on-resistance, conduction loss, and switching loss. The loss in each device was recalculated with this revised model for each operating voltage and current combination, indicating the additional loss shown in Figure 8.59 above the previously calculated values. Figure 8.60 and Figure 8.61 show the recalculated case and heatsink temperatures, showing a closer match to experimental results. For example, the maximum discrepancy in case temperature has been reduced from 11 °C to 8 °C. The discrepancy in total power stage loss was also reduced from 10.3% to 6.6% at 20 A<sub>rms</sub>, as shown in Figure 8.62.

The most critical result of this revised model is the peak junction temperature, shown in Figure 8.63. While the previous model allowed for operation up to 21.3 A<sub>rms</sub> without violating the desired 125 °C junction temperature limit, the peak junction temperatures in this revised model limit the inverter to 19.3 A<sub>rms</sub>. Even considering the remaining discrepancy of 8 °C in the case temperature, this operating point falls within the 150 °C rating of the junction.

The remaining loss discrepancy could be explained by approximately 20 mΩ in additional stray resistance on the ac side, although some of this is likely to be effective resistance in the devices

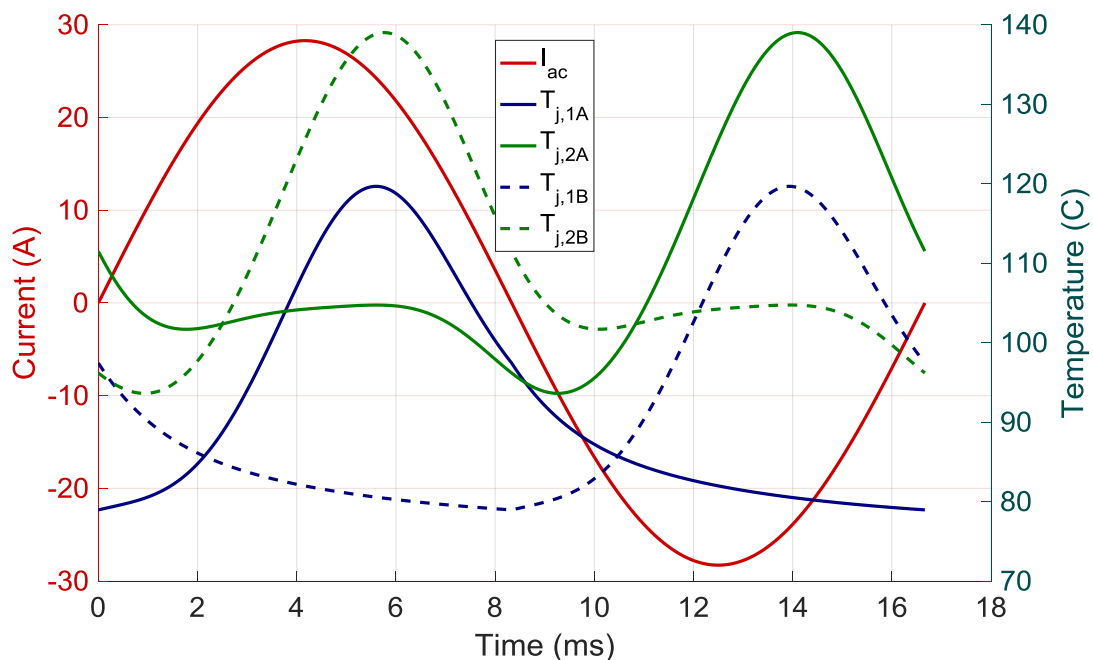


Figure 8.54. Instantaneous junction temperatures calculated using dynamic electro-thermal model, showing one complete line cycle at 450 V dc, 230 V ac, with 20 A<sub>rms</sub> output current.

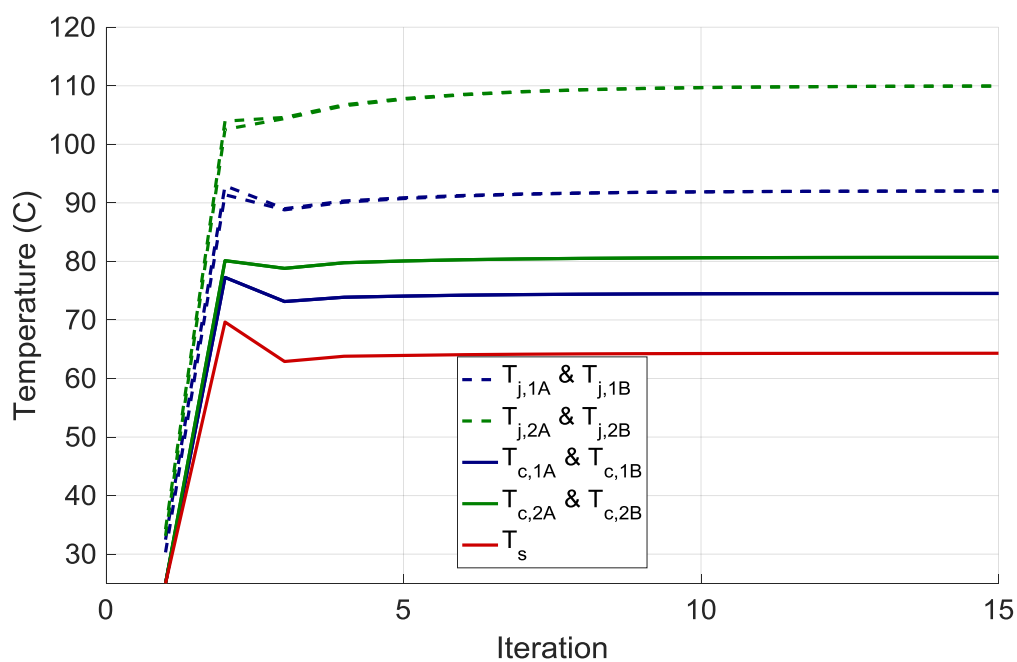


Figure 8.55. Average junction temperatures over one line cycle, calculated using dynamic electro-thermal model at 450 V dc, 230 V ac, with 20 A<sub>rms</sub> output current. Convergence is reached within 10 iterations.

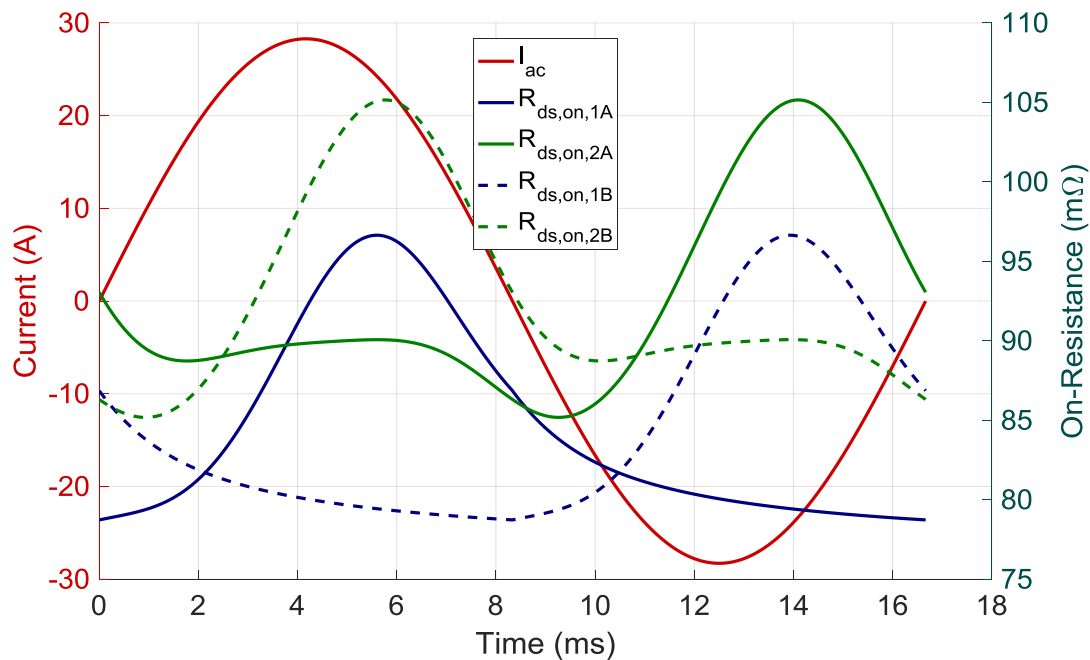


Figure 8.56. Instantaneous on-resistances calculated using dynamic electro-thermal model, showing one complete line cycle at 450 V dc, 230 V ac, with 20 A<sub>rms</sub> output current.

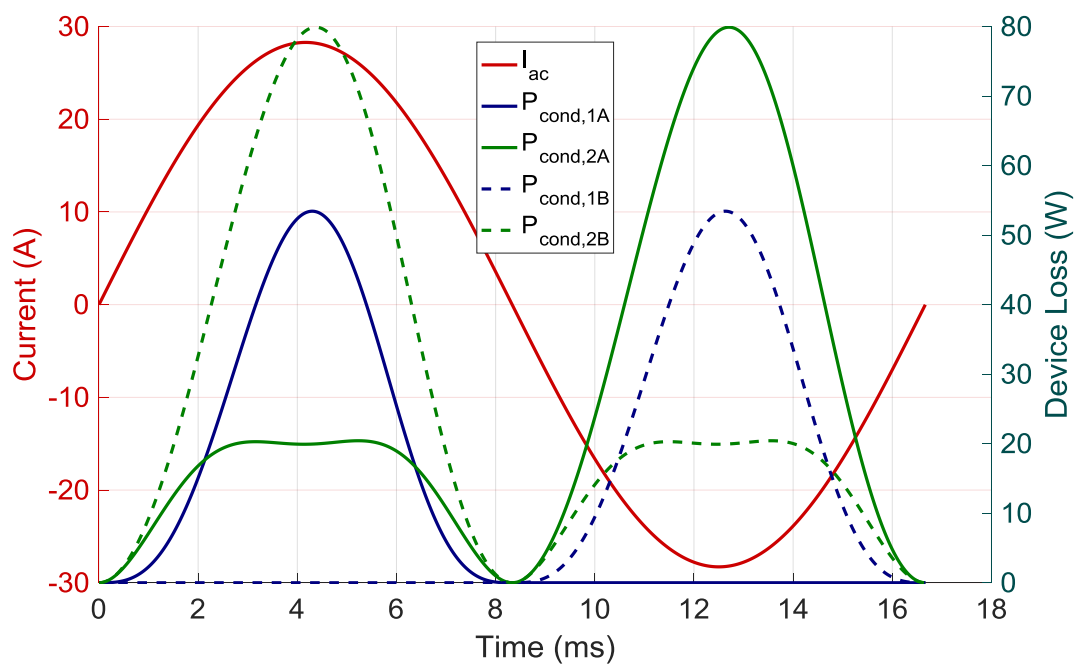


Figure 8.57. Instantaneous conduction losses calculated using dynamic electro-thermal model, showing one complete line cycle at 450 V dc, 230 V ac, with 20 A<sub>rms</sub> output current.

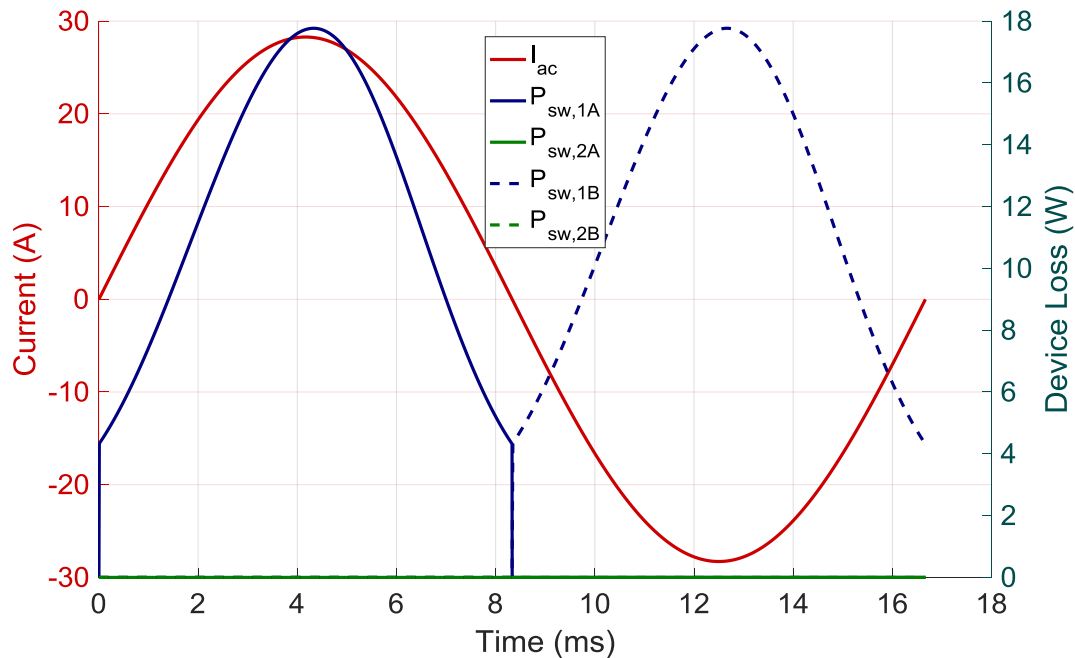


Figure 8.58. Instantaneous switching losses calculated using dynamic electro-thermal model, showing one complete line cycle at 450 V dc, 230 V ac, with 20 A<sub>rms</sub> output current.

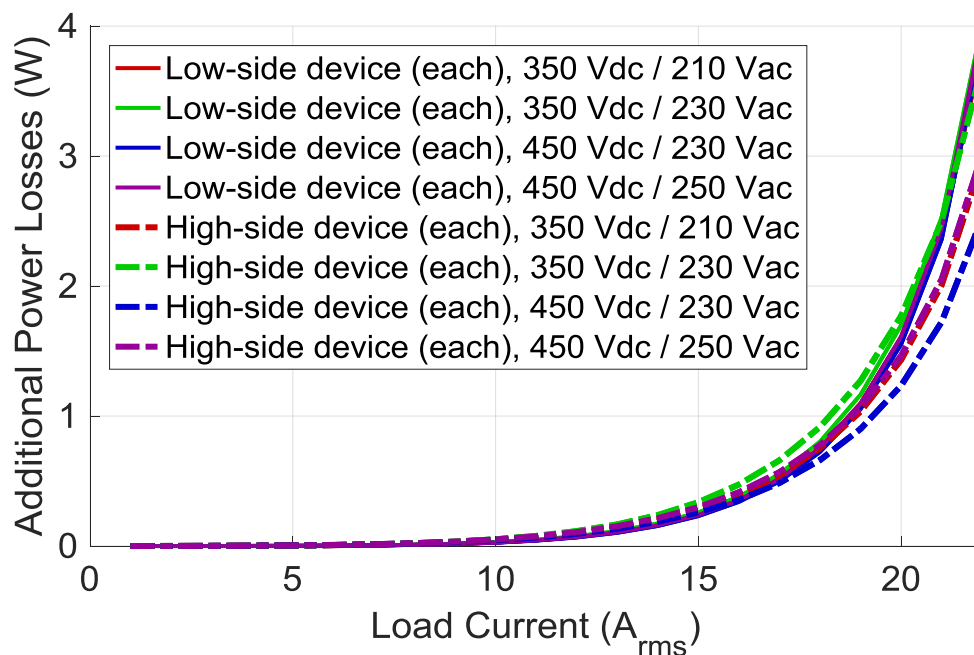


Figure 8.59. Additional per-device losses calculated using dynamic electro-thermal loss model, above what was calculated using previous steady-state loss model.

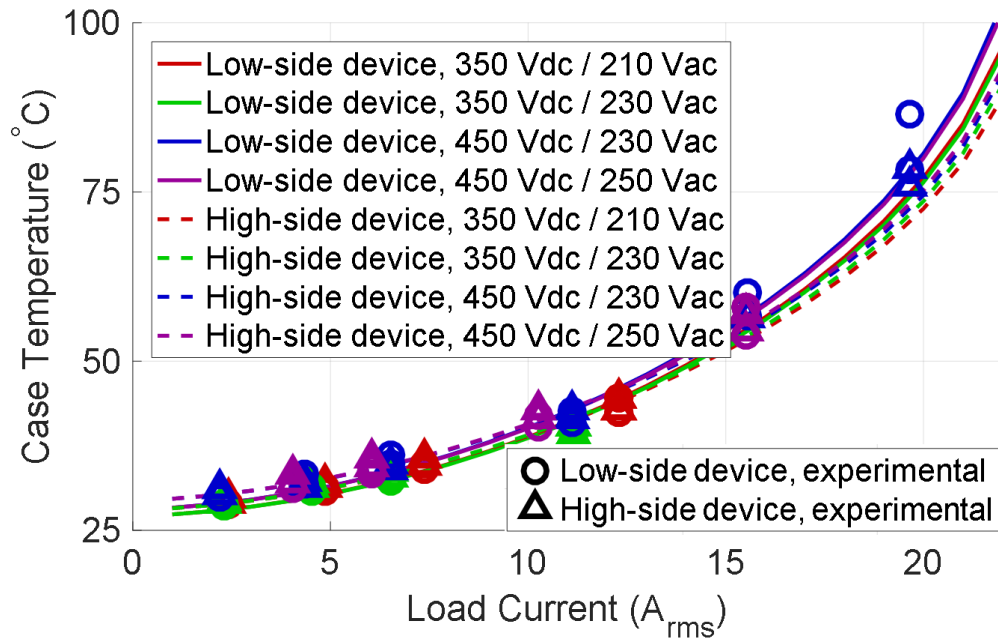


Figure 8.60. Device case temperatures calculated using dynamic electro-thermal model, for prototype at four operating conditions considered in experimental verification, with measured values shown for comparison.

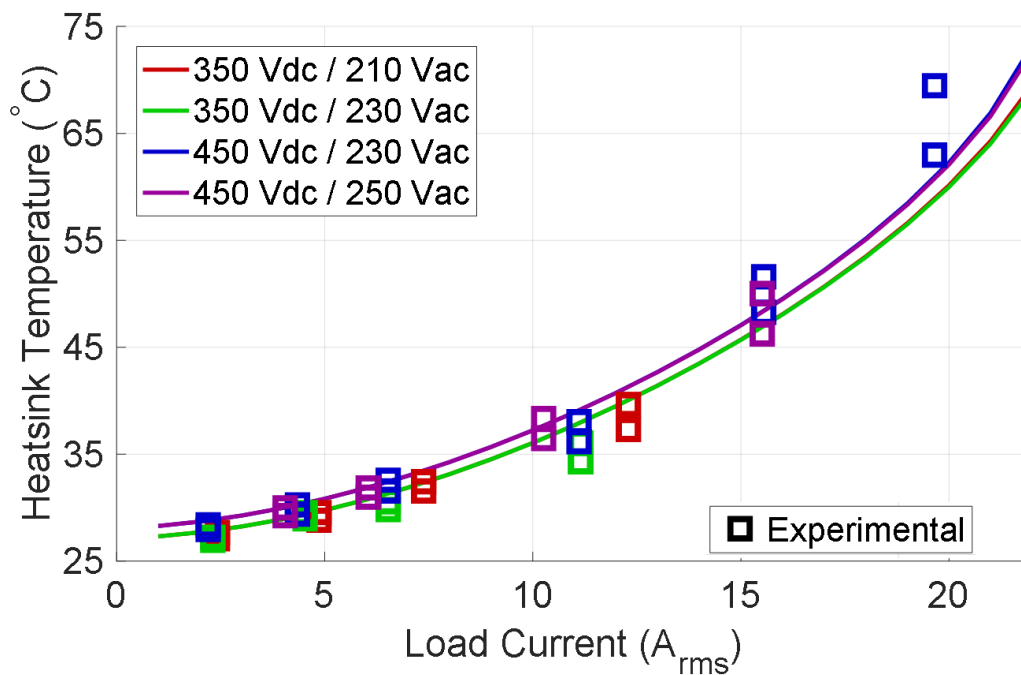


Figure 8.61. Heatsink temperatures calculated using dynamic electro-thermal model, for prototype at four operating conditions considered in experimental verification, with measured values shown for comparison.



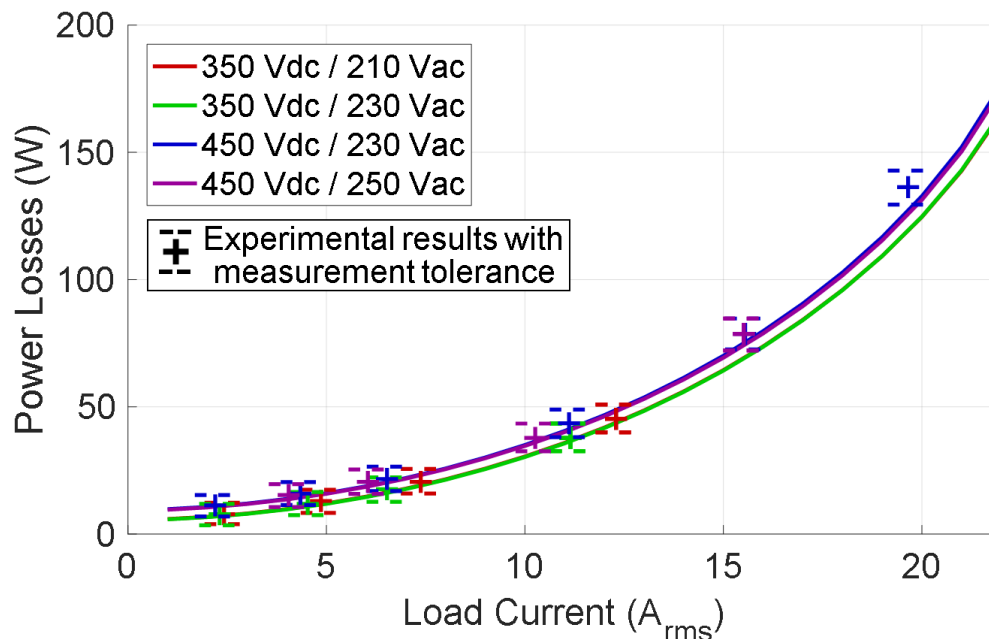


Figure 8.62. Overall converter power stage losses calculated using dynamic electro-thermal model, for prototype at four operating conditions considered in experimental verification, with measured values and measurement tolerances (error bars) shown for comparison.

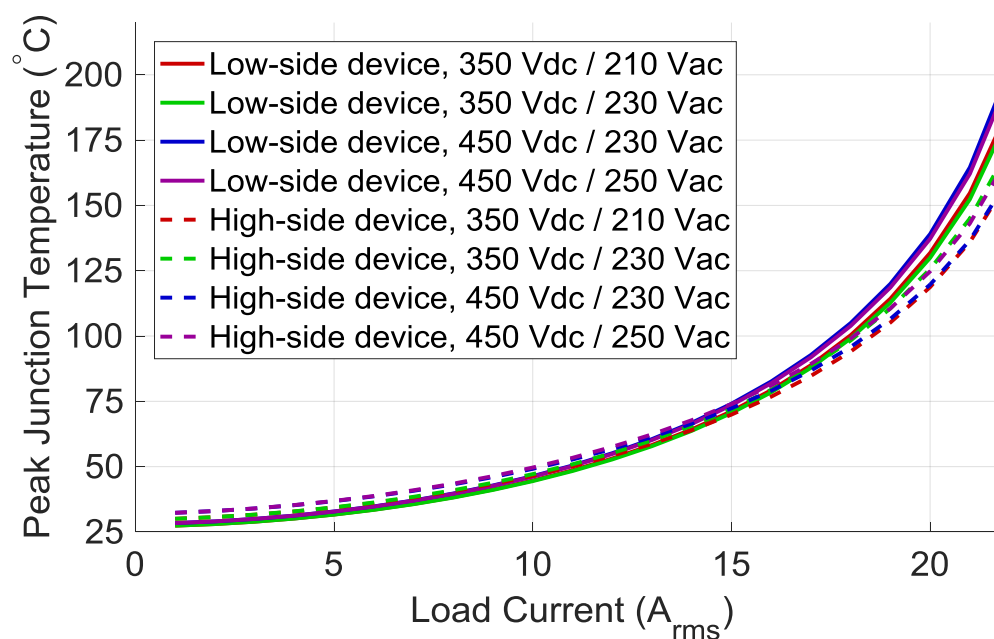


Figure 8.63. Peak junction temperatures calculated using dynamic electro-thermal model, for prototype at four operating conditions considered in experimental verification, with measured values shown for comparison.

due to the remaining temperature discrepancies. Adding in the 20 m $\Omega$  of extra resistance produces the efficiency curve shown in Figure 8.64, which matches very closely with experimental results. This efficiency curve has a CEC weighted average of 97.6%, exceeding the targeted 97.0%.

### 8.9 General application of this methodology for converter margin reduction

The methodology presented here may be utilized for margin reduction in other GaN-based converter designs, depending on how much characterization data is available for the GaN devices and surrounding components. Reducing the current margin without violating any ratings requires precise models for all device losses and thermal impedances. Most of these values are only available at one particular operating point in device data sheets, and others are not provided at all. For example, implementing the proposed loss model with the specified values for the devices and

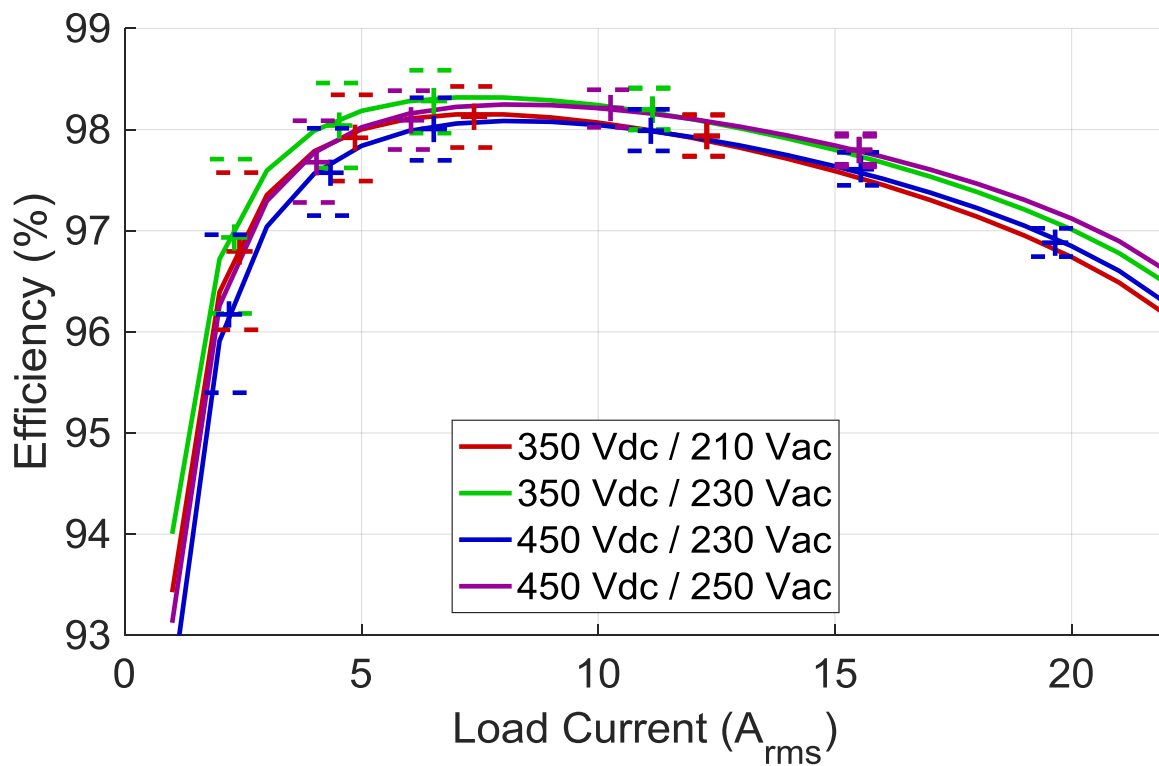


Figure 8.64. Prototype inverter efficiency, calculated using dynamic electro-thermal model and incorporating an addition 60 m $\Omega$  of stray resistance, indicating a CEC efficiency of 97.6%.

heatsink originally indicated that the inverter could operate safely up to 25 A<sub>rms</sub> (5.3 kW) without exceeding the desired maximum junction temperature of 125 °C. However, the detailed characterization indicated a maximum allowable current of 25% lower output power. In fact, operation up to that initially estimated maximum of 25 A<sub>rms</sub> would lead to thermal runaway and destroy the devices. According to the dynamic electro-thermal model, the peak junction temperature reaches 450 °C at 24.2 A<sub>rms</sub>. Even at a slightly higher ac current of 24.3 A<sub>rms</sub>, the junction temperature calculation no longer converges and rises asymptotically to infinity.

Similarly, the steady-state model predicts thermal runaway above 24 A<sub>rms</sub>. The steady-state model is sufficient for most cases, and the dynamic electro-thermal model may not be necessary in some converter designs. For example, the steady-state model is appropriate for a dc-dc converter, using a loss model similar to the instantaneous equations (8.6), (8.31)-(8.34). The steady-state electro-thermal model may also be appropriate for inverters in which  $R_{\theta,jc}$  represents a relatively minor component of the overall thermal resistance, such as with a larger die size device or smaller heatsink. In this particular inverter design,  $R_{\theta,jc}$  accounted for approximately 30% of the total temperature drop from junction to ambient at  $T_j = 125$  °C. However, if  $R_{\theta,jc}$  is much smaller than the heatsink and interface thermal resistances, the temperature swing from short time-constant impedances may be negligibly small compared to the overall temperature rise. In that case, the steady-state model is an effective method for loss and temperature analysis.

The importance of static and dynamic characterization in this generalized methodology also varies from case to case. The variation of on-resistance with temperature may be sufficiently characterized in the device data sheet and may not need to be repeated. Depending on the switching frequency of the converter, the total loss of the converter may be very sensitive to accurate switching loss and dead time loss models, which typically rely on static and dynamic characterization. In terms of mitigating transient overshoot voltage, it may not be necessary to

perform dynamic characterization prior to designing the converter. The conventional approach is simply to minimize parasitic inductance as much as possible, and then choose a relatively conservative switching speed until the voltage overshoot can be measured experimentally.

The methodology and analysis described in Section 8.4 can be directly applied to improve this conventional approach. For example, it may seem rational to initially reduce the dc voltage below the intended operating bus voltage, until the overshoot voltage is experimentally measured. However, negative trends have been demonstrated in both voltage overshoots with dc bus voltage, so this may not in fact be an effective approach. Similarly, reducing the switching speed and operating current for the initial testing may be logical steps in the initial experimental characterization. Indeed, Section 8.4 showed that the turn-on overshoot is strongly proportional to turn-on speed, but not to current. Likewise, the turn-off overshoot is strongly proportional to current, but it may not be very strongly related to turn-off speed in GaN devices. Therefore, these two transient voltage overshoots should be considered separately when experimentally verifying these limitations in a GaN-based converter. The turn-on speed can be increased to improve switching loss, by accurately measuring the synchronous switch drain voltage with high-bandwidth passive probes at the intended operating bus voltage, to ensure that it does not exceed the device's voltage rating. The maximum allowable load current can then be determined by measuring the drain voltage on the active switch during the turn-off transient. This turn-off overshoot can be reduced by slowing down the turn-off speed, but the results in Section 8.4 indicate that this may not be practical with GaN FETs. Rather, the turn-off overshoot can be treated as an inherent current limit at the system level. Of course, both of these overshoot phenomena can be improved by reducing the loop inductance, which should be an important consideration in the design prior to experimental characterization.

### 8.10 Summary

A full-bridge single-phase inverter was designed for potential PV applications, with a design focused on maximum utilization of commercial GaN GITs from Infineon to reduce the cost per kW. The key limiting factors in reducing the voltage and current margins of the device were identified as the maximum junction temperature and the overshoot voltage during turn-on and turn-off switching transients. The design of the power stage and thermal interconnection was aimed at mitigating these limitations through a combination of experimental characterization and modeling. The gate drive circuit was designed based on a limitation of  $< 100$  V overshoot up to 450 V dc and 34 A peak instantaneous load current (24 A<sub>rms</sub>). The device losses were experimentally characterized using the methodology presented in Chapter 4, using the gate drive circuit and power stage designed, and a device loss model was developed.

A thermal design was proposed for bottom-cooled devices, using copper thermal interface blocks to avoid excessive thermal resistance from PCB thermal vias. The thermal design was implemented with a heatsink selected for natural convection cooling, and the thermal equivalent circuit was experimentally characterized to improve the accuracy of the loss model. This characterization showed that both the heatsink and the Infineon GIT had higher thermal resistances than specified, although the thermal resistance of the copper thermal interface blocks was measured at 0.6 °C/W as initially estimated. The higher than specified thermal resistances were very limiting to the maximum operating conditions of the prototype. The prototype was experimentally verified to operate up to 5 kW without violating the specified maximum junction temperature at the maximum 250 V output voltage, but it must be derated with lower output voltage.

The experimental results indicated an extra conduction loss equivalent to approximately 20 mΩ of stray resistance, although some of this may be due to extra loss within the device

(potentially due to dynamic  $R_{ds,on}$ ). The CEC weighted average efficiency of 97.6% was calculated for this prototype, higher than the required 97.0%.

Although the initial target for maximum power was 5 kW, the inverter was derated based on the calculated peak junction temperatures. The 19.3 A<sub>rms</sub> limitation requires derating the inverter to 4.0 kW at the minimum AC voltage of 210 V<sub>rms</sub>, 4.4 kW at the nominal 230 V<sub>rms</sub>, and 4.8 kW at the maximum 250 V<sub>rms</sub>. Because the factors involved in this limitation are well-modeled the next version of this prototype can be modified to increase the rating. For example, a new heatsink with a thermal resistance of 0.15 °C/W would allow for operating up to 24 A<sub>rms</sub> (at least 5 kW from 210-250 V<sub>rms</sub>). This could also be accomplished with a 0.25 °C/W heatsink if the thermal interface resistance can be reduced from 0.6 to 0.3 °C/W, which may be possible by using newly available top-cooled versions of the same GaN GITs.

The next version of this prototype will include improvements to the heatsink design to increase the maximum current capability. It will also take advantage of top-cooled GaN GITs to design a vertical power loop and decrease the transient overshoot voltage, with the intention to push the dc input voltage up to 550 V without exceeding the 600 V device rating. A full thermal characterization will be performed on this top-cooled device, as well as static and dynamic characterization. The characterization and modeling from Chapter 4 and Chapter 6 were key components of this inverter design, providing the methodology for initial characterization of device losses and gate driver design. Future work will also include correction of the loss model to eliminate the remaining 6.6% error compared with the experimental results (equivalent to 20 mΩ of resistance). This will include a more accurate measurement of stray resistances in the circuit, as well as the dynamic  $R_{ds,on}$  in this GaN GIT.

## Chapter 9

### Conclusion

#### 9.1 *Current contributions*

Contributions from the work presented here include the following elements:

- a) Commercial and near-commercial GaN power devices were reviewed. This review is distinct in that it is given from the perspective of GaN-based converter design and application, rather than device fabrication, and that it covers a range of devices available today, rather than focusing on a single manufacturer's device. This review includes some typical structures of both vertical and horizontal devices, their commercial availability and ratings, and some of the unique properties of these devices. Following this user-oriented device review, the design challenges of GaN power devices were summarized, including board layout and gate driver requirements.
- b) The methodology for characterization of GaN FETs across a full sweep of voltage, current, and temperature conditions was presented, including results from two examples of 600 V enhancement-mode GaN FETs. These tests include static characteristics such as forward and reverse conduction behavior, on-resistance, transconductance, gate leakage current, and junction capacitance. Additionally, the dynamic characteristics were studied with a sweep of double pulse tests, measuring turn-on times and loss as well as turn-off times and loss. The waveforms were also studied in post-processing for other dynamic properties such as gate and drain overvoltages and estimation of other unmeasured waveforms based on available data. Three key contributions in this area are as follows: 1) a sub-nanosecond current deskew procedure based on power loop inductance voltage drop; 2) an accurate means of junction temperature control in both static and dynamic testing; and 3) methodology for estimating

additional waveforms that are internal to the device or otherwise difficult to measure, based on the measured static and dynamic testing results.

- c) In addition to the typical dynamic characterization, a methodology was developed to determine the turn-on loss due to cross-talk with various symmetric and asymmetric gate resistances. The losses in both the active and synchronous devices due to the shoot-through current caused by cross-talk were measured using this experimental methodology for the enhancement-mode GaN HFET characterized in (b). The negative spikes caused by this cross-talk were also studied for each case.
- d) A model was developed to explain the behavior of an enhancement-mode GaN HFET during the turn-on and turn-off  $dv_{ds}/dt$  transient. Using subcircuit analysis, equations for the driver voltage, gate voltage, gate current, drain-source voltage, channel current, and drain current were developed. Calculated waveforms using the proposed model were shown to match well with experimental results at several different operating conditions and gate resistances. This model was not developed for loss prediction or simulation, but rather to understand and explain the experimental waveforms and provide a basis for improved gate driver design for this device. Two key applications of this model were proposed: 1) improved understanding of the controllable circuit parameters that impact the speed of the  $dv_{ds}/dt$  transient and overvoltages; and 2) a technique for scaling experimentally measured turn-on loss to higher temperature.
- e) A fault protection scheme was developed to detect overcurrent and short-circuit faults and quickly turn off GaN GITs. This scheme was designed based on the modeling and characterization of one particular GaN GIT, then it was implemented and experimentally verified using engineering samples of that part. The circuit includes a comparator detection circuit for a filtered gate voltage, as well as a soft turn-off circuit for controlled fault shutdown without inducing excessive overvoltage. This protection circuit was experimentally verified in



short-circuit conditions in a range of voltage and temperature conditions, as well as inductive load overcurrent faults. The overcurrent threshold and total fault energy were shown to be highly immune to temperature variations, with a total response time under 180 ns at 400 V for all operating temperatures in both HSF and FUL fault types, with less than 100 ns detection time and a soft turn-off to prevent overvoltage damage. The model and characterization used to design the  $v_{gs}$ -based overcurrent detection was also shown to be useful in estimation the junction temperature of an on-state device with 0 A load current.

- f) A methodology was established for designing a full-bridge hard-switching inverter with reduced current and voltage margins, to fully utilize the capabilities of the GaN FETs. This methodology involves selection of gate drive circuit parameters, bus voltages, and load currents to ensure that the device does not exceed its pulsed drain voltage rating. The switching loss, conduction loss, and other device loss components were modeled using the static and dynamic characterization techniques described in Chapter 4. Additionally, the thermal equivalent circuit was experimentally characterized, including the device, interface, and heatsink. This thermal design includes a copper thermal interface block intended to connect the heatsink with the bottom-cooled GaN FETs through PCB cutouts, acting as both thermal standoffs and heat spreaders. Using the chosen gate drive circuit parameters, device loss models, and thermal equivalent circuit, the maximum current and voltage capabilities of the converter were determined. This model was verified experimentally, and then used to identify key research areas for further improvement in the current and voltage capabilities of the design.

## 9.2 *Proposed future work*

Future work in this area would likely be extensions of the current contributions, including the following key research areas:

- a) The dynamic characterization methodology described in Chapter 4 may be extended to include characterization of the dynamic  $R_{ds,on}$  (i.e. “current collapse”) mechanism described in Chapter 2, particularly in the case of hard switching. This mechanism was hypothesized to be the source of loss discrepancy between the model and experimental results in Chapter 8. Extensive literature is available on the subject of dynamic  $R_{ds,on}$  characterization, although there is an inherent challenge in measuring  $v_{ds}$  with mV-scale accuracy within ns of dropping from hundreds of volts in the off-state. Such a test setup is required to accurately capture the time-varying  $R_{ds,on}$  increase that occurs immediately after a hard turn-on, which has been shown to vary with junction temperature, bus voltage, and other operating conditions. In a hard-switching converter switching in the hundreds of kHz range, the increased  $R_{ds,on}$  within a few hundred ns of turn-on can be a significant loss contributor.
- b) The short circuit fault ruggedness of the GaN GIT used in Chapters 7 and 8 may be tested to determine minimum protection response to prevent degradation. The protection scheme demonstrated in Chapter 7 was verified to shut down the faulted switch within 100-200 ns of exceeding the overcurrent threshold, but it has not yet been shown whether this response is fast enough to prevent long-term degradation of the devices. Although no failures were seen during the experimental testing of the protection circuit, only one pair of devices was used during the short-circuit testing phase.
- c) Similarly, the overcurrent scheme may be tested with a larger sample size of devices from multiple manufacturers, part numbers, and sample batches, as well as with the same devices over time to check for drift. This testing would enhance the practicality of the protection scheme, since a real implementation would require consistent behavior over a statistical spread of devices without significant variation in performance over time. Testing of scheme with integration into an actual converter would also allow further verification of noise immunity,

including the isolation of the high-side device's protection circuit, and immunity to coupled noise from elsewhere in the power stage circuit.

- d) A more extensive sweep of gate drive circuit parameters may be performed with the GaN GIT, to establish best-case tradeoff of switching loss and overvoltage with a capacitive gate drive circuit. This may include sweeping the dynamic driving voltage, turn-on and turn-off gate resistances, and speed-up capacitance, as well as variation of other elements of the driving circuit. This sweep may identify a combination of gate drive circuit parameters that produces lower switching losses than in the experimental prototype presented in Chapter 8, without violating the pulsed voltage rating of the device during switching transient overshoots.
- e) The converter presented in Chapter 8 may be improved in terms of loss/efficiency and maximum power rating. This improvement is likely to come from a one or more of the following design areas: a more optimized heatsink selection/design; implementation of a vertical power loop using top-cooled GaN GITs; implementation of a different modulation scheme (e.g., symmetric unipolar) for more balanced device loss sharing; and higher switching frequency, if this results in overall filter size/cost/loss reduction without a significantly higher contribution from switching loss. In particular, the performance with newly available top-cooled GaN GITs may be compared with the performance previously achieved using bottom-cooled GITs. Although the difference in thermal resistance is not likely to be significant due to the prior successful implementation of thermal interface blocks, the vertical power loop using top-cooled GITs is expected to cut the total power loop inductance in half, which may reduce the turn-on and turn-off overshoot voltages by a similar margin. Comprehensive characterization of the hard-switching dynamic  $R_{ds,on}$  can also be performed using the methodology established in this work, which will improve the loss prediction model when the switching frequency is increased.

### 9.3 Publications

- E. Jones, P. Williford, Z. Yang, J. Chen, F. Wang, S. Bala, J. Xu, J. Puukko, “Maximizing the voltage and current capability of GaN FETs in a hard-switching inverter,” to be presented at IEEE International Conference on Power Electronics and Drive Systems, Dec. 2017.
- E. Jones, P. Williford, F. Wang, “A fast overcurrent protection scheme for GaN GITs,” presented at IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Nov. 2017.
- E. Jones, F. Wang, Z. Zhang, “Analysis of the  $dv/dt$  transient of enhancement-mode GaN FETs,” in *Proc. IEEE Applied Power Electronics Conference (APEC)*, Tampa, FL, Mar. 2017, pp. 2692-2699.
- E.A. Jones, F. Wang, D. Costinett, “Review of commercial GaN power devices and GaN-based converter design challenges,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707-719, Jun. 2016.
- E. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, “Temperature-dependent turn-on loss analysis for GaN HFETs,” in *Proc. IEEE Applied Power Electronics Conference (APEC)*, Long Beach, CA, Mar. 2016, pp. 1010-1017.
- E. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, “Cross conduction analysis for a enhancement-mode 650-V GaN HFET in a phase-leg topology,” in *Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, Nov. 2015, pp. 98-103.
- E.A. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, B. Liu, R. Ren, “Characterization of an Enhancement-Mode 650-V GaN HFET,” in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, CA, Sept. 2015, pp. 400-407.

- E.A. Jones, F. Wang, B. Ozpineci, "Application-based review of GaN HFETs," in *Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Knoxville, TN, Oct. 2014, pp. 24-29.

Co-authored publications:

- B. Liu, Z. Zhang, E. Jones, F. Wang, "Application of GaN in hard-switching converters: challenges and potential solutions," *Power Electronics*, vol. 51, no. 9, pp. 3-13, Sept. 2017.
- B. Liu, R. Ren, E. Jones, F. Wang, D. Costinett, Z. Zhang, "A modulation compensation scheme to reduce input current distortion in GaN based high switching frequency three-phase three-level Vienna type rectifiers," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 283-298, Jan. 2018.
- Z. Zhang, B. Guo, F. Wang, E. Jones, L. Tolbert, B. Blalock, "Methodology for wide band-gap device dynamic characterization," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9307-9318, Dec. 2017.
- Y. Li, E. Jones, F. Wang, "Circulating current suppressing control's impact on arm inductance selection for Modular Multilevel Converter (MMC)," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 182-188, Mar. 2017.
- R. Ren, B. Liu, E. Jones, F. Wang, D. Costinett, Z. Zhang, "Accurate ZVS boundary in high switching frequency LLC converter," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, Sept. 2016.
- C. Zhao, B. Trento, J. Liang, E. Jones, B. Liu, Z. Zhang, D. Costinett, F. Wang, L. Tolbert, J. Jansen, R. Kress, R. Langley, "Design and implementation of GaN-based, 100 kHz, 102 W/in<sup>3</sup> single-phase inverter for the Google Little Box Challenge," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 824-840, Jun. 2016.

- R. Ren, B. Liu, E. Jones, F. Wang, Z. Zhang, D. Costinett, "Dual-output, three-level GaN-based dc-dc converter for battery charger applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 2441 - 2448, Jun. 2016.
- R. Ren, B. Liu, F. Wang, E. Jones, "Dual-output, three level GaN-based DC-DC converter for battery charger applications" in *Proc. IEEE Applied Power Electronics Conference (APEC)*, Long Beach, CA, Mar. 2016, pp. 2441-2448.
- Y. Li, E. Jones, F. Wang, "The impact of voltage-balancing control on switching frequency of the modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2829-2839, Jun. 2015.
- Y. Li, E. Jones, F. Wang, "Switching-frequency ripple on dc link voltage in a modular multilevel converter with circulating current suppressing control," in *Proc. IEEE Applied Power Electronics Conference (APEC)*, Fort Worth, TX, Mar. 2014, pp. 191-195.
- Y. Li, E. Jones, F. Wang, "Analysis of the relationship between switching frequency and sub-module capacitor unbalanced voltage for a modular multilevel converter," in *Proc. IEEE Applied Power Electronics Conference (APEC)*, Fort Worth, TX, Mar. 2014, pp. 220-224.

Other publications/contributions:

- Co-authored and co-presented professional education seminar at IEEE Applied Power Electronics Conference (APEC) in Long Beach, CA, March 2016, titled "Wide bandgap device characterization"
- Handbook in progress to be published by the Institute of Engineering and Technology, with working title *Characterization of Wide Bandgap Power Semiconductor Devices*, co-authored with Dr. Fred Wang and Dr. Zheyu Zhang

- Co-authored two chapters in DOE Report on Wide Bandgap Semiconductors for Electric Vehicle Applications (not yet published), specifically two chapters on Si-based power device fundamentals and WBG (SiC and GaN) power devices
- Invention disclosure filed in 2014 for “a voltage-source converter topology with fault current blocking capability for HVDC transmission systems,” co-developed with one student and two faculty.
- Invention disclosure and provisional patent application filed in 2017 for “gate-sensing overcurrent protection scheme for GaN transistors.”

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## **Appendices**

**Appendix A**  
**Sample Code for Post-Processing DPT Data**

```

clear all;
clc;

%Specify the folder where the data is, if different from current working directory
testpoint_filepath = '400V_15A\';
%If using Tek5000 series, this should be file name except _Chx.csv at end
%If using Tek4000 series, this should be complete file name
%On and off file names can be the same, if you only save one waveform
filename_on = 0;%'tek0000ALL.csv'; %Set to 0 if you do not want to process turn-on waveform
filename_off = 'tek0005ALL.csv'; %Set to 0 if you do not want to process turn-off waveform

%Settings for data importing
TekDPO5xxx = false; %If using Tek 5000-series scope
TekDPO4xxx = true; %If using Tek 4000-series scope
plotlines = true; %Plot vertical lines showing transient subinterval triggers
biasadjust = false; %Adjust dc bias for vds and id
plot_channel_current = true; %Calculate and plot Coss and channel current (requires separate Coss import)
alignment_check = false; %Check id-vds alignment (deskew) graphically
compensate_Esw = true; %Compensate switching loss for conduction loss that would otherwise occur
during transient interval
id_channel_number = 4;
vds_channel_number = 1;
vgs_channel_number = 2;
i_adj = 1; %Vertical scale adjustment for current measurement, if not scaled properly in scope
id_alignment_ns = 0; %Number of ns to move id earlier in time for deskew correction (shifts id to the left
in plots)

%Transient waveform window areas, for analyzing and plotting
turnon_window_stepback = 30; %How long before transient midpoint to start waveform window, in ns
turnon_window_time = 80; %Total window time of desired turn-on ttransition view, in ns
turnoff_window_stepback = 30; %How long before transient midpoint to start waveform window, in ns
turnoff_window_time = 80; %Total window time of desired turn-on ttransition view, in ns
filter_samples = 1; %Number of samples to use for differentiation (minimum 1, higher filters noise better
but loses accuracy)

%Parameters for plotting time-base waveforms
vds_scale = 100; %V/div
vgs_scale = 2; %V/div
id_on_scale = 10; %A/div
id_off_scale = 5; %A/div
Pon_scale = 5e3; %W/div
Poff_scale = 1e3; %W/div
time_grid_increment = 10; %ns/div
linewidth = 3;
vdsColor = [0 0 1];
vgsColor = [0 1 0];
idColor = [1 0 0];
powerColor = [0 0 0];
ichanColor = [0 1 1];
icossColor = [1 0.5 0.2];
fontsize = 16;

%Device/PCB parameters

```

```

Lloop = 4.7e-9; %Estimated power loop inductance
Cstray = 10e-12;
Rdson = 52e-3; %On-resistance of device under test
Rshunt = 0.100; %Resistance of coaxial current shunt
Vbd = 2; %Forward voltage of body diode
Rbd = Rdson*2; %Series resistance of body diode. This can be set to 0 if not known.
% Deskew plot settings. Set them all to -1 if you are not sure yet.
deskew_start = 20; %Start time in ns for x scale
deskew_stop = 30; %Stop time in ns for x scale
deskewVmin = 300; %Min voltage for y scale
deskewVmax = 450; %Max voltage for y scale

if (filename_on > 0)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Turn-on waveform analysis %%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%This section of the code processes a full data set that has been captured
%for analyzing turn-on waveform data (all variables ending with "_onwf").
%This data set likely has turn-off data as well, so that data must be
%processed partially, but it is not used for turn-off transient analysis.

%Import data
if (TekDPO5xxx == true) && (TekDPO4xxx == false) %Import 5000 series data format
    M = csvread([testpoint_filepath filename_on '_Ch' num2str(vgs_channel_number) '.csv'],0,3);
    time_onwf = (M(:,1) - M(1,1));
    deltat_onwf = (M(2,1)-M(1,1));
    vgs_onwf = M(:,2);
    M = csvread([testpoint_filepath filename_on '_Ch' num2str(vds_channel_number) '.csv'],0,3);
    vds_onwf = M(:,2);
    M = csvread([testpoint_filepath filename_on '_Ch' num2str(id_channel_number) '.csv'],0,3);
    id_onwf = -M(:,2);
    vector_length = length(time_onwf);
elseif (TekDPO4xxx == true) && (TekDPO5xxx == false) %Import 4000 series data format
    M = csvread([testpoint_filepath filename_on],21,0);
    time_onwf = (M(:,1)-M(1,1));
    vgs_onwf = M(:,vgs_channel_number+1);
    vds_onwf = M(:,vds_channel_number+1);
    id_onwf = M(:,id_channel_number+1);
    deltat_onwf = (M(2,1)-M(1,1));
    vector_length = length(time_onwf);
else
    return; %Not a compatible data format
end

% Check for inf and replace with closest non-inf data point
for m=1:vector_length
    if((vds_onwf(m)==Inf)|(vds_onwf(m)==-Inf))
        vds_onwf(m) = vds_onwf(m-1);
    end
    if((id_onwf(m)==Inf)|(id_onwf(m)==-Inf))
        id_onwf(m) = id_onwf(m-1);
    end
end

```

```

    if((vgs_onwf(m)==Inf)|(vgs_onwf(m)==-Inf))
        vgs_onwf(m) = vgs_onwf(m-1);
    end
end

%Adjust id if not scaled properly in scope
id_onwf = id_onwf*i_adj;

% Time shift id to correct deskew (I-V misalignment)
id_alignment_pts = round(id_alignment_ns * 1e-9 / deltat_onwf);
id_length = length(id_onwf);
if (id_alignment_pts > 0)
    id_onwf(1:id_length-id_alignment_pts) = id_onwf(id_alignment_pts+1:id_length);
else
    id_onwf(-id_alignment_pts+1:id_length) = id_onwf(1:id_length+id_alignment_pts);
end

%%%%%%%%%%%%Full window view of turn-on data set%%%%%%%%

%Set up plot window
fig = figure(1); clf; hold on;
fig.Name = 'Turn-On Waveform: Full Capture';
fullPlot = gca;
fullPlot.XGrid = 'on';
fullPlot.YGrid = 'on';
fullPlot.GridLineStyle = '--';
fullPlot.GridColor = [0.6 0.6 0.6];
fullPlot.GridAlpha = 0.5;
fullPlot.FontSize = fontsize;
fullPlot.XAxis.Visible = 'on';
fullPlot.YAxis.Visible = 'off';
fullPlotYAxis = fullPlot.YAxis;

%Plot lines
xlabel(['Time (\mus)']);
fullPlotXAxisLength = time_onwf(end)*1e6;
ymax = 0; ymin = 0;
% V_DS
vdsOnLine = line((time_onwf)*1e6, vds_onwf/vds_scale);
vdsOnLine.Color = vdsColor;
vdsOnLine.LineWidth = linewidth;
% V_GS
vgsOnLine = line(time_onwf*1e6, vgs_onwf/vgs_scale);
vgsOnLine.Color = vgsColor;
vgsOnLine.LineWidth = linewidth;
% I_D
idOnLine = line(time_onwf*1e6, id_onwf/id_on_scale);
idOnLine.Color = idColor;
idOnLine.LineWidth = linewidth;

% Add triangles to show y=0 point in scope-view plots
fullPlotYAxisLength = fullPlotYAxis.Limits(2)-fullPlotYAxis.Limits(1);
hold on;

```



```

fill([0 0 fullPlotXAxisLength/30]+fullPlotXAxisLength/50, [-1 1 0]*fullPlotYAxisLength/20, vgsColor);
fill([0 0 fullPlotXAxisLength/30]+fullPlotXAxisLength/100, [-1 1 0]*fullPlotYAxisLength/20, idColor);
fill([0 0 fullPlotXAxisLength/30], [-1 1 0]*fullPlotYAxisLength/20, vdsColor);
line([0 0], [fullPlotYAxis.Limits], 'color','black','linewidth',2)
line([1 1]*fullPlotXAxisLength, [fullPlotYAxis.Limits], 'color','black','linewidth',2)
line([0 fullPlotXAxisLength], [1 1]*fullPlotYAxis.Limits(1), 'color','black','linewidth',2)
line([0 fullPlotXAxisLength], [1 1]*fullPlotYAxis.Limits(2), 'color','black','linewidth',2)

%%%%%%%%%%%% Find turn-off time indices %%%%%%%%%%%%%%
j = 1;
while (vds_onwf(j) > 0.5*max(vds_onwf)) %Find and skip first turn-on, if it exists
    j = j + 1;
end
j = j + ceil(turnon_window_time*1e-9/deltat_onwf); %Skip ahead
while (vds_onwf(j) < 0.5*max(vds_onwf)) %Now find turn-off transient of interest
    j = j + 1;
end
%Set beginning and end of turn-off transient (but this data will not be used for
%turn-off transient analysis, since it comes from the turn-on data set)
j = j - floor(turnoff_window_stepback*1e-9/deltat_onwf);
turnoff_start_onwf = j;
j = j + floor(turnoff_window_time*1e-9/deltat_onwf);
turnoff_end_onwf = j;

%%%%%%%%%%%% Find turn-on time indices %%%%%%%%%%%%%%
while (vds_onwf(j) > 0.5*max(vds_onwf))
    j = j + 1;
end
%Set beginning and end of turn-on transient (this is the data that will be
%used for analysis of the turn-on transient)
j = j - floor(turnon_window_stepback*1e-9/deltat_onwf);
turnon_start_onwf = j;
j = j + floor(turnon_window_time*1e-9/deltat_onwf);
turnon_end_onwf = j;

while (vds_onwf(j) < 0.5*max(vds_onwf))
    j = j + 1;
end
%If it is captured in data set, this will find the end of the second pulse
second_turnoff_start_onwf = j - floor(turnoff_window_stepback*1e-9/deltat_onwf);

%Plot dashed vertical lines indicating the turn-on and turn-off transient
%locations on the full turn-on waveform capture
if (plotlines == true)
    line([turnoff_start_onwf turnoff_start_onwf]*deltat_onwf*1e6,fullPlotYAxis.Limits,'Color',[1 0.2
0.7],'LineStyle','--','LineWidth',2);
    line([turnoff_end_onwf turnoff_end_onwf]*deltat_onwf*1e6,fullPlotYAxis.Limits,'Color',[1 0.2
0.7],'LineStyle','--','LineWidth',2);
    line([turnon_start_onwf turnon_start_onwf]*deltat_onwf*1e6,fullPlotYAxis.Limits,'Color',[1 0.2
0.7],'LineStyle','--','LineWidth',2);
    line([turnon_end_onwf turnon_end_onwf]*deltat_onwf*1e6,fullPlotYAxis.Limits,'Color',[1 0.2
0.7],'LineStyle','--','LineWidth',2);
end

```

```

% Estimate load current based on average value 20 ns prior to start of turn-off waveform
IL_onwf = mean(id_onwf(turnoff_start_onwf-floor(20e-9/deltat_onwf):turnoff_start_onwf));

%Adjust for any dc bias error (not generally recommended, but optional)
if (biasadjust == true)
    id_dcbias_onwf = mean(id_onwf(turnon_start_onwf-floor(20e-9/deltat_onwf):turnon_start_onwf));
    id_onwf = id_onwf - id_dcbias_onwf;
    vds_dcbias_onwf = mean(vds_onwf(turnon_end_onwf:second_turnoff_start_onwf)) - IL_onwf*Rdson;
    vds_onwf = vds_onwf - vds_dcbias_onwf;
    % Recalculate IL with bias adjusted
    IL_onwf = mean(id_onwf(turnoff_start_onwf-floor(20e-9/deltat_onwf):turnoff_start_onwf));
end

% Find steady-state on values for vgs based on average 20 ns prior to start of turn-off waveform
% (this should be the positive driving voltage)
Vdrv_onwf = mean(vgs_onwf(turnoff_start_onwf-floor(20e-9/deltat_onwf):turnoff_start_onwf));
% Find average vds between 20 ns after turn-off and beginning of turn-on
Vdc_onwf = mean(vds_onwf(turnoff_end_onwf+floor(20e-9/deltat_onwf):turnon_start_onwf));

%%%%%%%%%%%% Find turn-on trigger points for subinterval analysis %%%%%%%%%%%%%%
j = turnon_start_onwf;
while (vgs_onwf(j-1) < 0.2*Vdrv_onwf)
    j = j + 1;
end
while (mean(vgs_onwf(j-2:j-1)) < vgs_onwf(j))
    j = j - 1;
end
%t1 is point where vgs starts to rise
t1_onwf = j;
t1_time_onwf = (time_onwf(t1_onwf)-time_onwf(turnon_start_onwf))*1e9;
while (id_onwf(j) < IL_onwf)
    j = j + 1;
end
%t3 is point where id = IL
t3_onwf = j;
t3_time_onwf = (time_onwf(t3_onwf)-time_onwf(turnon_start_onwf))*1e9;
while (id_onwf(j-1) < id_onwf(j))
    j = j - 1;
end
%t2 is point where id starts to rise
t2_onwf = j;
if (t2_onwf < turnon_start_onwf)
    t2_onwf = turnon_start_onwf + 1;
end
t2_time_onwf = (time_onwf(t2_onwf)-time_onwf(turnon_start_onwf))*1e9;
while (vds_onwf(j) > 0)
    j = j + 1;
end
%t4 is point where vds crosses 0 V, or in some cases where it reaches its
%first trough point then starts increasing again (only if it never crosses
%zero)
t4_onwf = j;

```

```

if (t4_onwf > turnon_end_onwf)
    t4_onwf = turnon_end_onwf - 1;
end
t4_time_onwf = (time_onwf(t4_onwf)-time_onwf(turnon_start_onwf))*1e9;

%%%%%%%%%% Calculate switching times %%%%%%%%%%%
td_on = t2_time_onwf - t1_time_onwf; %turn-on delay time
tcr = t3_time_onwf - t2_time_onwf; %current rise time
tvf = t4_time_onwf - t3_time_onwf; %voltage fall time
t_on = t4_time_onwf - t1_time_onwf; %total turn-on time

%%%%%%%%%% Calculate switching energy %%%%%%%%%%%
Pon = vds_onwf.*id_onwf;
% Eonwf_cum((turnon_start_onwf:turnon_end_onwf)-turnon_start_onwf+1) =
cumtrapz(time_onwf(turnon_start_onwf:turnon_end_onwf),Pon((turnon_start_onwf:turnon_end_onwf)-
turnon_start_onwf+1));
if (compensate_Esw == true)
    %Optionally, compensate for conduction loss that would have occurred
    %during the time interval of switching, to avoid double-counting (Ideal
    %duty cycles D and 1-D usually used for conduction loss calculation,
    %neglecting switching transient time)
    Eon_comp = (IL_onwf * Rdson^2) * (t4_onwf-t2_onwf)*deltat_onwf;
else
    Eon_comp = 0;
end
% Turn-on loss is integral of I*V during tcr and tvf only
Eon = trapz(time_onwf(t2_onwf:t4_onwf),Pon(t2_onwf:t4_onwf)) - Eon_comp;

%%%%%%%%%% Calculate dv/dt %%%%%%%%%%%
j = t3_onwf;
while (vds_onwf(j) > Vdc_onwf*0.9)
    j = j + 1;
end
% Find adjusted t3 where vds = 0.9Vdc
t3_90percent = j;
while (vds_onwf(j) > Vdc_onwf*0.1)
    j = j + 1;
end
% Find adjusted t4 where vds = 0.1Vdc
t4_10percent = j;
tvf_9010 = (t4_10percent - t3_90percent)*deltat_onwf*1e9;
% Using 10 & 90% points neglects the exponential fall at start and end, and
% instead focuses on nearly-linear fall of vds
dvdt_on(1:t4_10percent-t3_90percent+1) = (vds_onwf(t3_90percent+1:t4_10percent+1) -
vds_onwf(t3_90percent:t4_10percent))./(deltat_onwf);
dvdt_on_pk = max(-dvdt_on); %Peak dv/dt
dvdt_on_avg = mean(-dvdt_on); %Average dv/dt, which is typically used to describe switching speed

%Display results in command window
disp('Turn-on waveform analysis:');
fprintf(' V_dc      %4.0f V',Vdc_onwf);
fprintf('\n I_L      %4.1f A',IL_onwf);
fprintf('\n Eon       %4.1f uJ',Eon*1e6);

```

```

fprintf('\n td_on      %4.1f ns',td_on);
fprintf('\n tcr       %4.1f ns',tcr);
fprintf('\n tvf        %4.1f ns',tvf);
fprintf('\n Avg dv/dt   %4.1f V/ns',dvd_t_on_avg*1e-9);
fprintf('\n Peak dv/dt  %4.1f V/ns\n\n',dvd_t_on_pk*1e-9);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Plot turn-on transient %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Set up plot window
ta = turnon_start_onwf;
tb = turnon_end_onwf;
fig = figure(2); clf; hold on;
fig.Name = 'Turn-On Transient';

% Setup Power Subplot and plot power line
powerSubPlot = subplot(2, 1, 1);
powerSubPlot.XGrid = 'on';
powerSubPlot.YGrid = 'on';
powerSubPlot.Position = [0.01 0.77 0.98 0.22];
powerSubPlot.XAxis.Visible = 'off';
powerSubPlot.YAxis.Visible = 'off';
powerSubPlot.FontSize = fontsize;
powerSubPlot.XTick = [0:time_grid_increment:turnon_window_time-
mod(turnon_window_time,time_grid_increment)];
powerSubPlot.YTick = [floor(min(Pon(ta:tb)/Pon_scale)):1:ceil(max(Pon(ta:tb)/Pon_scale))];
powerSubPlot.GridLineStyle = '--';
powerSubPlot.GridColor = [0.6 0.6 0.6];
powerSubPlot.GridAlpha = 0.5;
powerLine = line((time_onwf(ta:tb)-time_onwf(ta))*1e9, Pon(ta:tb)/(Pon_scale));
powerLine.Color = powerColor;
powerLine.LineWidth = linewidth;
powerYAxis = powerSubPlot.YAxis;
powerYAxis.Limits = [floor(min(Pon/Pon_scale)) ceil(max(Pon/Pon_scale))];
powerYAxis.Length = powerYAxis.Limits(2)-powerYAxis.Limits(1);
axis([0 turnon_window_time powerYAxis.Limits]);
% Add triangle to show y=0 point in scope-view plot
hold on;
fill([0 0 turnon_window_time/30], [-powerYAxis.Length/8 powerYAxis.Length/8 0],'black');
line([0 0], [powerYAxis.Limits], 'color','black','linewidth',2)
line([1 1]*turnon_window_time, [powerYAxis.Limits], 'color','black','linewidth',2)
line([0 turnon_window_time], [1 1]*powerYAxis.Limits(1), 'color','black','linewidth',2)
line([0 turnon_window_time], [1 1]*powerYAxis.Limits(2), 'color','black','linewidth',2)

if (plotlines == true)
%   line([t1_time_onwf t1_time_onwf],[powerYAxis.Limits],'Color',[1 0.2 0.7],'LineStyle','--
','LineWidth',2);
%   line([t2_time_onwf t2_time_onwf],[powerYAxis.Limits],'Color',[1 0.2 0.7],'LineStyle','--
','LineWidth',2);
%   line([t3_time_onwf t3_time_onwf],[powerYAxis.Limits],'Color',[1 0.2 0.7],'LineStyle','--
','LineWidth',2);
%   line([t4_time_onwf t4_time_onwf],[powerYAxis.Limits],'Color',[1 0.2 0.7],'LineStyle','--
','LineWidth',2);

```

```

end

% Setup id/vds/vgs subplot and plot these lines
measSubP = subplot(2, 1, 2);
measSubP.Position = [0.01 0.16 0.98 0.6];
measSubP.XGrid = 'on';
measSubP.YGrid = 'on';
measSubP.GridLineStyle = '--';
measSubP.GridColor = [0.6 0.6 0.6];
measSubP.GridAlpha = 0.5;
measSubP.FontSize = fontsize;
measSubP.XAxis.Visible = 'on';
measSubP.YAxis.Visible = 'off';
measSubP.XTick = [0:time_grid_increment:turnon_window_time-
mod(turnon_window_time,time_grid_increment)];
measSubP.YTick = [-100:1:100];
measYAxis = measSubP.YAxis;
xlabel(['Time (ns)']);
line([0 turnon_window_time],[0 0],'Color',[0.4 0.4 0.4],'LineStyle','-','LineWidth',3);
ymax = 0; ymin = 0;
% V_DS
vdsOnLine = line((time_onwf(ta:tb)-time_onwf(ta))*1e9, vds_onwf(ta:tb)/vds_scale);
vdsOnLine.Color = vdsColor;
vdsOnLine.LineWidth = linewidth;
ymax = max([ymax ceil(max(vds_onwf(ta:tb)/vds_scale))]);
ymin = min([ymin floor(min(vds_onwf(ta:tb)/vds_scale))]);
% V_GS
vgsOnLine = line((time_onwf(ta:tb)-time_onwf(ta))*1e9, vgs_onwf(ta:tb)/vgs_scale);
vgsOnLine.Color = vgsColor;
vgsOnLine.LineWidth = linewidth;
ymax = max([ymax ceil(max(vgs_onwf(ta:tb)/vgs_scale))]);
ymin = min([ymin floor(min(vgs_onwf(ta:tb)/vgs_scale))]);
% I_D
idOnLine = line((time_onwf(ta:tb)-time_onwf(ta))*1e9, id_onwf(ta:tb)/id_on_scale);
idOnLine.Color = idColor;
idOnLine.LineWidth = linewidth;
ymax = max([ymax ceil(max(id_onwf(ta:tb)/id_on_scale))]);
ymin = min([ymin floor(min(id_onwf(ta:tb)/id_on_scale))]);

% Calculate Coss and channel currents if option is selected
% To use this function, you must generate a file Coss.mat with a variable
% Coss stored in it, which can be created using file
% "Process_capacitance_curves.m". This Coss vector must be scaled such
% that the voltage is equal to the index of each point (i.e., Coss(12) is
% the Coss of your device when Vds = 12 V.
% You must also select "filter_samples" wisely, based on how noisy your
% data set is.
if (plot_channel_current == true)
    load Coss.mat;
    % Calculate dvdt using a centered moving average, which is accomplished
    % by looking forward and backward in time equally (filter_samples) then
    % dividing the difference in vds by 2*filter_samples*deltat

```

```

dvd_t_calc = [(vds_onwf(ta+filter_samples:tb+filter_samples) - vds_onwf(ta-filter_samples:tb-
filter_samples))/(deltat_onwf * 2 * filter_samples)];
% Use imported Coss.mat data to find Coss at each sampled time.
% Note that if vds < 1, Coss(1) is used, and if vds exceeds the Coss
% vector that was imported, it uses the highest vds point on the curve.
for mmm = 1:tb-ta + 1
    if (vds_onwf(mmm + ta - 1) < 1);
        Coss_calc(mmm) = Coss(1) + Cstray;
    elseif (vds_onwf(mmm + ta - 1) > length(Coss));
        Coss_calc(mmm) = Coss(end) + Cstray;
    else
        Coss_calc(mmm) = Coss(floor(vds_onwf(mmm + ta - 1))) + Cstray;
    end
    icoss_onwf(mmm) = -dvd_t_calc(mmm) * Coss_calc(mmm);
    ichan_onwf(mmm) = icoss_onwf(mmm) + id_onwf(mmm + ta - 1);
end
% Plot icoss line
icossOnLine = line((time_onwf(ta:tb)-time_onwf(ta))*1e9,icoss_onwf/id_on_scale);
icossOnLine.Color = icossColor;
icossOnLine.LineWidth = linewidth;
ymax = max([ymax ceil(max(icoss_onwf/id_on_scale))]);
ymin = min([ymin floor(min(icoss_onwf/id_on_scale))]);
% Plot ichan line
ichanOnLine = line((time_onwf(ta:tb)-time_onwf(ta))*1e9,ichan_onwf/id_on_scale);
ichanOnLine.Color = ichanColor;
ichanOnLine.LineWidth = linewidth;
ymax = max([ymax ceil(max(ichan_onwf/id_on_scale))]);
ymin = min([ymin floor(min(ichan_onwf/id_on_scale))]);
end

% Add triangles to show y=0 point in scope-view plots
axis([0 turnon_window_time ymin ymax]);
measYAxisLength = measYAxis.Limits(2)-measYAxis.Limits(1);
xTick = get(measSubP,'XTick');
measSubP.XTick = xTick(1:end-1);
hold on;
fill([0 0 turnon_window_time/30]+turnon_window_time/50, [-1 1 0]*measYAxisLength/20, vgsColor);
fill([0 0 turnon_window_time/30]+turnon_window_time/100, [-1 1 0]*measYAxisLength/20, idColor);
fill([0 0 turnon_window_time/30], [-1 1 0]*measYAxisLength/20, vdsColor);
% Add black border around plot
line([0 0], [measYAxis.Limits], 'color','black','linewidth',2)
line([1 1]*turnon_window_time, [measYAxis.Limits], 'color','black','linewidth',2)
line([0 turnon_window_time], [1 1]*measYAxis.Limits(1), 'color','black','linewidth',2)
line([0 turnon_window_time], [1 1]*measYAxis.Limits(2), 'color','black','linewidth',2)

% Optionally, plot the subinterval trigger points t1-t4 to help verify
% calculations. If lines do not appear to be where they should be, then
% algorithm for detecting trigger points may need to be modified for your
% data set.
if (plotlines == true)
    line([t1_time_onwf t1_time_onwf],[ymin ymax],'Color',[1 0.2 0.7],'LineStyle','--','LineWidth',2);
    line([t2_time_onwf t2_time_onwf],[ymin ymax],'Color',[1 0.2 0.7],'LineStyle','--','LineWidth',2);
    line([t3_time_onwf t3_time_onwf],[ymin ymax],'Color',[1 0.2 0.7],'LineStyle','--','LineWidth',2);

```

```

    line([t4_time_onwf t4_time_onwf],[ymin ymax],'Color',[1 0.2 0.7],'LineStyle','--','LineWidth',2);
end

% Optionally, calculate di/dt and graphically examine I-V alignment to
% improve/correct deskew setting
if (alignment_check == true)
    % Calculate didt using a centered moving average, which is accomplished
    % by looking forward and backward in time equally (filter_samples) then
    % dividing the difference in id by 2*filter_samples*deltat
    didt = [(id_onwf(ta+filter_samples:tb+filter_samples) - id_onwf(ta-filter_samples:tb-
filter_samples))/(deltat_onwf * 2 * filter_samples)];
    % This equation is based on a KVL of power loop, using settings
    % selected at beginning of this file.
    vds_calc = Vdc_onwf + Vbd + (IL_onwf-id_onwf(ta:tb))*Rbd - id_onwf(ta:tb)*Rshunt - Lloop*didt;
    % Adjust dc bias to make graphical alignment easier
    vds_calc_adjust = mean(vds_onwf(ta:t2_onwf)-vds_calc(1:t2_onwf-ta+1));
    vds_calc = vds_calc + vds_calc_adjust;
    % Plot vds and this new vds calculated using id waveform, and compare
    % the two graphically. If not well aligned, try adjusting
    % filter_samples or id_alignment_ns until the two match well.
    % IMPORTANT! - The deskew setting should not change unless your test
    % setup changes (board, cables, scope, shunt, etc.). Do not adjust
    % deskew or id_alignment_ns differently for different data points in
    % the same test data set.
    fig = figure(5); clf; hold on; hax = gca; grid on;
    set(fig, 'units', 'inches', 'position', [2 2 7.4 4.5])
    set(hax,'FontSize',fontsize);
    plot((time_onwf(ta:tb)-time_onwf(ta))*1e9,vds_onwf(ta:tb),'-', 'lineWidth',linewidth,'color',[0 0 0.8])
    plot((time_onwf(ta:tb)-time_onwf(ta))*1e9,vds_calc,'-', 'lineWidth',linewidth,'color',[0.5 0.1 0.5])
    line([t2_time_onwf t2_time_onwf],get(hax,'YLim'),'Color',[1 0.2 0.7],'LineStyle','--','LineWidth',2);
    line([t3_time_onwf t3_time_onwf],get(hax,'YLim'),'Color',[1 0.2 0.7],'LineStyle','--','LineWidth',2);

    xlabel('Time (ns)');
    ylabel('Voltage (V)');
    legend('v_{ds,meas}','v_{ds,calc}','location','Southwest')
    %This scaling must be selected at the beginning of the file.
    if deskew_start>=0
        axis([deskew_start deskew_stop deskewVmin deskewVmax]);
    end
end

end

if (filename_off > 0)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Turn-off waveform analysis %%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%This section of the code processes a full data set that has been captured
%for analyzing turn-off waveform data (all variables ending with "_offwf".
%This data set likely has turn-on data as well, so that data must be
%processed partially, but it is not used for turn-on transient analysis.

```

```

%Import data
if (TekDPO5xxx == true) && (TekDPO4xxx == false) %Import 5000 series data format
    M = csvread([testpoint_filepath filename_off '_Ch' num2str(vgs_channel_number) '.csv'],0,3);
    time_offwf = (M(:,1) - M(1,1));
    deltat_offwf = (M(2,1)-M(1,1));
    vgs_offwf = M(:,2);
    M = csvread([testpoint_filepath filename_off '_Ch' num2str(vds_channel_number) '.csv'],0,3);
    vds_offwf = M(:,2);
    M = csvread([testpoint_filepath filename_off '_Ch' num2str(id_channel_number) '.csv'],0,3);
    id_offwf = -M(:,2);
    vector_length = length(time_offwf);
elseif (TekDPO4xxx == true) && (TekDPO5xxx == false) %Import 4000 series data format
    M = csvread([testpoint_filepath filename_off],21,0);
    time_offwf = (M(:,1)-M(1,1));
    vgs_offwf = M(:,vgs_channel_number+1);
    vds_offwf = M(:,vds_channel_number+1);
    id_offwf = M(:,id_channel_number+1);
    deltat_offwf = (M(2,1)-M(1,1));
    vector_length = length(time_offwf);
else
    return; %Not a compatible data format
end

% Check for inf and replace with closest non-inf data point
for m=1:vector_length
    if((vds_offwf(m)==Inf)|(vds_offwf(m)==-Inf))
        vds_offwf(m) = vds_offwf(m-1);
    end
    if((id_offwf(m)==Inf)|(id_offwf(m)==-Inf))
        id_offwf(m) = id_offwf(m-1);
    end
    if((vgs_offwf(m)==Inf)|(vgs_offwf(m)==-Inf))
        vgs_offwf(m) = vgs_offwf(m-1);
    end
end

%Adjust id if not scaled properly in scope
id_offwf = id_offwf*i_adj;

% Time shift id to correct deskew (I-V misalignment)
id_alignment_pts = round(id_alignment_ns * 1e-9 / deltat_offwf);
id_length = length(id_offwf);
if (id_alignment_pts > 0)
    id_offwf(1:id_length-id_alignment_pts) = id_offwf(id_alignment_pts+1:id_length);
else
    id_offwf(-id_alignment_pts+1:id_length) = id_offwf(1:id_length+id_alignment_pts);
end

%%%%%%%%%%%%Full window view of turn-off data set%%%%%%%%

%Set up plot window
fig = figure(3); clf; hold on;

```



```

fig.Name = 'Turn-Off Waveform: Full Capture';
fullPlot = gca;
fullPlot.XGrid = 'on';
fullPlot.YGrid = 'on';
fullPlot.GridLineStyle = '--';
fullPlot.GridColor = [0.6 0.6 0.6];
fullPlot.GridAlpha = 0.5;
fullPlot.FontSize = fontsize;
fullPlot.XAxis.Visible = 'on';
fullPlot.YAxis.Visible = 'off';
fullPlotYAxis = fullPlot.YAxis;

%Plot lines
xlabel(['Time (\mus)']);
fullPlotXAxisLength = time_offwf(end)*1e6;
ymax = 0; ymin = 0;
% V_DS
vdsOffLine = line((time_offwf)*1e6, vds_offwf/vds_scale);
vdsOffLine.Color = vdsColor;
vdsOffLine.LineWidth = linewidth;
% V_GS
vgsOffLine = line(time_offwf*1e6, vgs_offwf/vgs_scale);
vgsOffLine.Color = vgsColor;
vgsOffLine.LineWidth = linewidth;
% I_D
idOffLine = line(time_offwf*1e6, id_offwf/id_on_scale);
idOffLine.Color = idColor;
idOffLine.LineWidth = linewidth;

% Add triangles to show y=0 point in scope-view plots
fullPlotYAxisLength = fullPlotYAxis.Limits(2)-fullPlotYAxis.Limits(1);
hold on;
fill([0 0 fullPlotXAxisLength/30]+fullPlotXAxisLength/50, [-1 1 0]*fullPlotYAxisLength/20, vgsColor);
fill([0 0 fullPlotXAxisLength/30]+fullPlotXAxisLength/100, [-1 1 0]*fullPlotYAxisLength/20, idColor);
fill([0 0 fullPlotXAxisLength/30], [-1 1 0]*fullPlotYAxisLength/20, vdsColor);
line([0 0], [fullPlotYAxis.Limits], 'color','black','linewidth',2)
line([1 1]*fullPlotXAxisLength, [fullPlotYAxis.Limits], 'color','black','linewidth',2)
line([0 fullPlotXAxisLength], [1 1]*fullPlotYAxis.Limits(1), 'color','black','linewidth',2)
line([0 fullPlotXAxisLength], [1 1]*fullPlotYAxis.Limits(2), 'color','black','linewidth',2)

%%%%%%%%%%%% Find turn-off time indices %%%%%%%%%%
j = 1;
while (vds_offwf(j) > 0.5*max(vds_offwf)) %Find and skip first turn-on, if it exists
    j = j + 1;
end
j = j + ceil(turnon_window_time*1e-9/deltat_offwf); %Skip ahead
while (vds_offwf(j) < 0.5*max(vds_offwf)) %Now find turn-off transient of interest
    j = j + 1;
end
%Set beginning and end of turn-off transient (this is the data that will be
%used for analysis of the turn-off transient)
j = j - floor(turnoff_window_stepback*1e-9/deltat_offwf);
turnoff_start_offwf = j;

```

```

j = j + floor(turnoff_window_time*1e-9/deltat_offwf);
turnoff_end_offwf = j;

%%%%%%%%%%%% Find turn-on time indices %%%%%%%%%%%%%%
while (vds_offwf(j) > 0.5*max(vds_offwf))
    j = j + 1;
end
%Set beginning and end of turn-on transient (but this data will not be used for
%turn-on transient analysis, since it comes from the turn-off data set)
j = j - floor(turnon_window_stepback*1e-9/deltat_offwf);
turnon_start_offwf = j;
j = j + floor(turnon_window_time*1e-9/deltat_offwf);
turnon_end_offwf = j;

while (vds_offwf(j) < 0.5*max(vds_offwf))
    j = j + 1;
end
%If it is captured in data set, this will find the end of the second pulse
second_turnoff_start_offwf = j - floor(turnoff_window_stepback*1e-9/deltat_offwf);

%Plot dashed vertical lines indicating the turn-on and turn-off transient
%locations on the full turn-on waveform capture
if (plotlines == true)
    line([turnoff_start_offwf turnoff_start_offwf]*deltat_offwf*1e6,fullPlotY Axis.Limits,'Color',[1 0.2
0.7],'LineStyle','--','LineWidth',2);
    line([turnoff_end_offwf turnoff_end_offwf]*deltat_offwf*1e6,fullPlotY Axis.Limits,'Color',[1 0.2
0.7],'LineStyle','--','LineWidth',2);
    line([turnon_start_offwf turnon_start_offwf]*deltat_offwf*1e6,fullPlotY Axis.Limits,'Color',[1 0.2
0.7],'LineStyle','--','LineWidth',2);
    line([turnon_end_offwf turnon_end_offwf]*deltat_offwf*1e6,fullPlotY Axis.Limits,'Color',[1 0.2
0.7],'LineStyle','--','LineWidth',2);
end

% Estimate load current based on average value 20 ns prior to start of turn-off waveform
IL_offwf = mean(id_offwf(turnoff_start_offwf-floor(20e-9/deltat_offwf):turnoff_start_offwf));

%Adjust for any dc bias error (not generally recommended, but optional)
if (biasadjust == true)
    id_dcbias_offwf = mean(id_offwf(turnon_start_offwf-floor(20e-9/deltat_offwf):turnon_start_offwf));
    id_offwf = id_offwf - id_dcbias_offwf;
    vds_dcbias_offwf = mean(vds_offwf(turnon_end_offwf:second_turnoff_start_offwf)) -
IL_offwf*Rdson;
    vds_offwf = vds_offwf - vds_dcbias_offwf;
    % Recalculate IL with bias adjusted
    IL_offwf = mean(id_offwf(turnoff_start_offwf-floor(20e-9/deltat_offwf):turnoff_start_offwf));
end

% Find steady-state on values for vgs based on average 20 ns prior to start of turn-off waveform
% (this should be the positive driving voltage)
Vdrv_offwf = mean(vgs_offwf(turnoff_start_offwf-floor(20e-9/deltat_offwf):turnoff_start_offwf));
% Find average vds between 20 ns after turn-off and beginning of turn-on
Vdc_offwf = mean(vds_offwf(turnoff_end_offwf+floor(20e-9/deltat_offwf):turnon_start_offwf));

```

%%%%%%%%%% Find turn-off trigger points for subinterval analysis %%%%%%%%%%%

```

j = turnoff_start_offwf;
while (vgs_offwf(j) > Vdrv_offwf*0.9)
    j = j + 1;
end
while (vgs_offwf(j-1) > vgs_offwf(j)) || (vgs_offwf(j-2) > vgs_offwf(j))
    j = j - 1;
end
%t5 is point where vgs starts to fall
t5_offwf = j;
t5_time_offwf = (time_offwf(t5_offwf)-time_offwf(turnoff_start_offwf))*1e9;
% Now, find time when vds has risen to 5% of Vdc
while (vds_offwf(j) < Vdc_offwf*0.05)
    j = j + 1;
end
% Then, go backward until vds stops decreasing significantly
while (vds_offwf(j) > mean(vds_offwf(j-15:j)))
    j = j - 1;
end
%t6 is point where vds starts to rise
t6_offwf = j;
t6_time_offwf = (time_offwf(t6_offwf)-time_offwf(turnoff_start_offwf))*1e9;
while (id_offwf(j) > 0) %Find first negative-sloped zero crossing of id
    j = j + 1;
end
% Check that vds > Vdc at this zero crossing. If not, find next
% negative-sloped zero crossing until this is true. (Usually it will be
% the first zero crossing, but this may get complicated in cases where the
% device package inductance is significant).
while (vds_offwf(j) < Vdc_offwf)
    while (id_offwf(j) < 0)
        j = j + 1;
    end
    while (id_offwf(j) > 0)
        j = j + 1;
    end
end
% t7 is first negative-sloped point where id crosses 0 A that occurs after
% vds exceeds Vdc. In some cases, this may be a trough point rather than a
% zero crossing then starts increasing again (only if it never crosses 0 A).
t7_offwf = j;
t7_time_offwf = (time_offwf(t7_offwf)-time_offwf(turnoff_start_offwf))*1e9;

% In very light-load cases, id may have a non-negligible dc bias error
% following the turn-off transient, which may prevent id from crossing
% zero. In these cases, it may work better to use the minimum id point,
% if it approaches 0 A but does not cross. Alternatively, you can use the
% peak vds point, which is nearby to the actual t7, but may not be exactly
% the same moment (very tough to know for sure in some waveforms).
[peak_vds maxvds_index] = max(vds_offwf(turnoff_start_offwf:turnoff_end_offwf));
[minid_off minid_index] = min(id_offwf(turnoff_start_offwf:turnoff_end_offwf));
if (t7_offwf > turnoff_end_offwf)
    % t7_offwf = maxvds_index(1) + turnoff_start_offwf - 1;

```

```

t7_offwf = minid_index(1) + turnoff_start_offwf - 1;
t7_time_offwf = (time_offwf(t7_offwf)-time_offwf(turnoff_start_offwf))*1e9;
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Calculate switching times %%%%%%%%%%%%%%
td_off = t6_time_offwf - t5_time_offwf; %turn-off delay time
tvr = t7_time_offwf - t6_time_offwf; %turn-off voltage rise time
t_off = t7_time_offwf - t5_time_offwf; %total turn-off time

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Calculate switching energy %%%%%%%%%%%%%%
Poff = vds_offwf.*id_offwf;
% Eoffwf_cum((turnoff_start_offwf:turnoff_end_offwf)-turnoff_start_offwf+1) =
cumtrapz(time_offwf(turnoff_start_offwf:turnoff_end_offwf),Pon((turnoff_start_offwf:turnoff_end_offwf)
-turnoff_start_offwf+1));
if (compensate_Esw == true)
    %Optionally, compensate for conduction loss that would have occurred
    %during the time interval of switching, to avoid double-counting (Ideal
    %duty cycles D and 1-D usually used for conduction loss calculation,
    %neglecting switching transient time)
    Eoff_comp = (IL_offwf * Rdson^2) * (t7_offwf-t6_offwf)*deltat_offwf;
else
    Eoff_comp = 0;
end
% Turn-on loss is integral of I*V during tvr only
Eoff = trapz(time_offwf(t6_offwf:t7_offwf),Poff(t6_offwf:t7_offwf)) - Eoff_comp;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Calculate dv/dt %%%%%%%%%%%%%%
j = t6_offwf;
while (vds_offwf(j) < Vdc_offwf*0.1)
    j = j + 1;
end
% Find adjusted t6 where vds = 0.1Vdc
t6_10percent = j;
while (vds_offwf(j) < Vdc_offwf*0.9)
    j = j + 1;
end
% Find adjusted t7 where vds = 0.9Vdc
t7_90percent = j;
tvr_1090 = (t7_90percent - t6_10percent)*deltat_offwf*1e9;
% Using 10 & 90% points neglects the exponential rise at start and end, and
% instead focuses on nearly-linear rise of vds
dvdt_off(1:t7_90percent-t6_10percent+1) = (vds_offwf(t6_10percent+1:t7_90percent+1) -
vds_offwf(t6_10percent:t7_90percent))./(deltat_offwf);
dvdt_off_pk = max(dvdt_off); %Peak dv/dt
dvdt_off_avg = mean(dvdt_off); %Average dv/dt, which is typically used to describe switching speed

% Calculate peak vds and vds overshoot, using the measured Vdc.
% Note that this assumes Vdc and vds both have some dc bias error
% immediately following the transient, since this Vdc is usually higher
% than the actual dc voltage coming from the benchtop supply.
vds_overshoot = peak_vds - Vdc_offwf;

```

```

%Display results in command window
disp('Turn-off waveform analysis:');
fprintf(' V_dc      %4.0f V',Vdc_offwf);
fprintf('\n I_L      %4.1f A',IL_offwf);
fprintf('\n Eoff      %4.1f uJ',Eoff*1e6);
fprintf('\n td_off    %4.1f ns',td_off);
fprintf('\n tvr      %4.1f ns',tvr);
fprintf('\n Avg dv/dt  %4.1f V/ns',dvd_t_off_avg*1e-9);
fprintf('\n Peak dv/dt %4.1f V/ns',dvd_t_off_pk*1e-9);
fprintf('\n Vds overshoot %4.1f V \n\n',vds_overshoot);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Plot turn-off transient %%%%%%%%%%%%%%%

% Set up plot window
ta = turnoff_start_offwf;
tb = turnoff_end_offwf;
fig = figure(4); clf; hold on;
fig.Name = 'Turn-Off Transient';

% Setup Power Subplot and plot power line
powerSubPlot = subplot(2, 1, 1);
powerSubPlot.XGrid = 'on';
powerSubPlot.YGrid = 'on';
powerSubPlot.Position = [0.01 0.77 0.98 0.22];
powerSubPlot.XAxis.Visible = 'off';
powerSubPlot.YAxis.Visible = 'off';
powerSubPlot.FontSize = fontsize;
powerSubPlot.XTick = [0:time_grid_increment:turnoff_window_time-
mod(turnoff_window_time,time_grid_increment)];
powerSubPlot.YTick = [floor(min(Poff(ta:tb)/Poff_scale)):1:ceil(max(Poff(ta:tb)/Poff_scale))];
powerSubPlot.GridLineStyle = '--';
powerSubPlot.GridColor = [0.6 0.6 0.6];
powerSubPlot.GridAlpha = 0.5;
powerLine = line((time_offwf(ta:tb)-time_offwf(ta))*1e9, Poff(ta:tb)/(Poff_scale));
powerLine.Color = powerColor;
powerLine.LineWidth = linewidth;
powerY Axis = powerSubPlot.Y Axis;
powerY Axis.Limits = [floor(min(Poff(ta:tb)/Poff_scale)) ceil(max(Poff(ta:tb)/Poff_scale))];
powerY Axis.Length = powerY Axis.Limits(2)-powerY Axis.Limits(1);
axis([0 turnoff_window_time powerY Axis.Limits]);
% Add triangle to show y=0 point in scope-view plot
hold on;
fill([0 0 turnoff_window_time/30], [-powerY Axis.Length/8 powerY Axis.Length/8 0], 'black');
line([0 0], [powerY Axis.Limits], 'color','black','linewidth',2)
line([1 1]*turnoff_window_time, [powerY Axis.Limits], 'color','black','linewidth',2)
line([0 turnoff_window_time], [1 1]*powerY Axis.Limits(1), 'color','black','linewidth',2)
line([0 turnoff_window_time], [1 1]*powerY Axis.Limits(2), 'color','black','linewidth',2)

if (plotlines == true)
%   line([t5_time_offwf t5_time_offwf],[powerY Axis.Limits],'Color',[1 0.2 0.7],'LineStyle','--
','LineWidth',2);

```

```

    line([t6_time_offwf t6_time_offwf],[powerY Axis.Limits],'Color',[1 0.2 0.7],'LineStyle','--',
    'LineWidth',2);
    line([t7_time_offwf t7_time_offwf],[powerY Axis.Limits],'Color',[1 0.2 0.7],'LineStyle','--',
    'LineWidth',2);
end

% Setup id/vds/vgs subplot and plot these lines
measSubP = subplot(2, 1, 2);
measSubP.Position = [0.01 0.16 0.98 0.6];
measSubP.XGrid = 'on';
measSubP.YGrid = 'on';
measSubP.GridLineStyle = '--';
measSubP.GridColor = [0.6 0.6 0.6];
measSubP.GridAlpha = 0.5;
measSubP.FontSize = fontsize;
measSubP.XAxis.Visible = 'on';
measSubP.YAxis.Visible = 'off';
measSubP.XTick = [0:time_grid_increment:turnoff_window_time-
mod(turnoff_window_time,time_grid_increment)];
measSubP.YTick = [-100:1:100];
measY Axis = measSubP.Y Axis;
xlabel(['Time (ns)']);
line([0 turnoff_window_time],[0 0],'Color',[0.4 0.4 0.4],'LineStyle','-','LineWidth',3);
ymax = 0; ymin = 0;
% V_DS
vdsOffLine = line((time_offwf(ta:tb)-time_offwf(ta))*1e9, vds_offwf(ta:tb)/vds_scale);
vdsOffLine.Color = vdsColor;
vdsOffLine.LineWidth = linewidth;
ymax = max([ymax ceil(max(vds_offwf(ta:tb)/vds_scale))]);
ymin = min([ymin floor(min(vds_offwf(ta:tb)/vds_scale))]);
% V_GS
vgsOffLine = line((time_offwf(ta:tb)-time_offwf(ta))*1e9, vgs_offwf(ta:tb)/vgs_scale);
vgsOffLine.Color = vgsColor;
vgsOffLine.LineWidth = linewidth;
ymax = max([ymax ceil(max(vgs_offwf(ta:tb)/vgs_scale))]);
ymin = min([ymin floor(min(vgs_offwf(ta:tb)/vgs_scale))]);
% I_D
idOffLine = line((time_offwf(ta:tb)-time_offwf(ta))*1e9, id_offwf(ta:tb)/id_off_scale);
idOffLine.Color = idColor;
idOffLine.LineWidth = linewidth;
ymax = max([ymax ceil(max(id_offwf(ta:tb)/id_off_scale))]);
ymin = min([ymin floor(min(id_offwf(ta:tb)/id_off_scale))]);

% Calculate Coss and channel currents if option is selected
% To use this function, you must generate a file Coss.mat with a variable
% Coss stored in it, which can be created using file
% "Process_capacitance_curves.m". This Coss vector must be scaled such
% that the voltage is equal to the index of each point (i.e., Coss(12) is
% the Coss of your device when Vds = 12 V.
% You must also select "filter_samples" wisely, based on how noisy your
% data set is.
if (plot_channel_current == true)
    load Coss.mat;

```

```

% Calculate dvdt using a centered moving average, which is accomplished
% by looking forward and backward in time equally (filter_samples) then
% dividing the difference in vds by 2*filter_samples*deltat
dvdt_calc = [(vds_offwf(ta+filter_samples:tb+filter_samples) - vds_offwf(ta-filter_samples:tb-
filter_samples))/(deltat_offwf * 2 * filter_samples)];
% Use imported Coss.mat data to find Coss at each sampled time.
% Note that if vds < 1, Coss(1) is used, and if vds exceeds the Coss
% vector that was imported, it uses the highest vds point on the curve.
for mmm = 1:tb-ta + 1
    if (vds_offwf(mmm + ta - 1) < 1);
        Coss_calc(mmm) = Coss(1) + Cstray;
    elseif (vds_offwf(mmm + ta - 1) > length(Coss));
        Coss_calc(mmm) = Coss(end) + Cstray;
    else
        Coss_calc(mmm) = Coss(floor(vds_offwf(mmm + ta - 1))) + Cstray;
    end
    icoss_offwf(mmm) = dvdt_calc(mmm) * Coss_calc(mmm);
    ichan_offwf(mmm) = -icoss_offwf(mmm) + id_offwf(mmm + ta - 1);
end
% Plot icoss line
icossOffLine = line((time_offwf(ta:tb)-time_offwf(ta))*1e9,icoss_offwf/id_off_scale);
icossOffLine.Color = icossColor;
icossOffLine.LineWidth = linewidth;
ymax = max([ymax ceil(max(icoss_offwf/id_off_scale))]);
ymin = min([ymin floor(min(icoss_offwf/id_off_scale))]);
% Plot ichan line
ichanOffLine = line((time_offwf(ta:tb)-time_offwf(ta))*1e9,ichan_offwf/id_off_scale);
ichanOffLine.Color = ichanColor;
ichanOffLine.LineWidth = linewidth;
ymax = max([ymax ceil(max(ichan_offwf/id_off_scale))]);
ymin = min([ymin floor(min(ichan_offwf/id_off_scale))]);
end

% Add triangles to show y=0 point in scope-view plots
axis([0 turnoff_window_time ymin ymax]);
measYAxisLength = measYAxis.Limits(2)-measYAxis.Limits(1);
xTick = get(measSubP,'XTick');
measSubP.XTick = xTick(1:end-1);
hold on;
fill([0 0 turnoff_window_time/30]+turnoff_window_time/50, [-1 1 0]*measYAxisLength/20, vgsColor);
fill([0 0 turnoff_window_time/30]+turnoff_window_time/100, [-1 1 0]*measYAxisLength/20, idColor);
fill([0 0 turnoff_window_time/30], [-1 1 0]*measYAxisLength/20, vdsColor);
% Add black border around plot
line([0 0], [measYAxis.Limits], 'color','black','linewidth',2)
line([1 1]*turnoff_window_time, [measYAxis.Limits], 'color','black','linewidth',2)
line([0 turnoff_window_time], [1 1]*measYAxis.Limits(1), 'color','black','linewidth',2)
line([0 turnoff_window_time], [1 1]*measYAxis.Limits(2), 'color','black','linewidth',2)

% Optionally, plot the subinterval trigger points t5-t7 to help verify
% calculations. If lines do not appear to be where they should be, then
% algorithm for detecting trigger points may need to be modified for your
% data set.
if (plotlines == true)

```

```
    line([t5_time_offwf t5_time_offwf],[ymin ymax],'Color',[1 0.2 0.7],'LineStyle','--','LineWidth',2);  
    line([t6_time_offwf t6_time_offwf],[ymin ymax],'Color',[1 0.2 0.7],'LineStyle','--','LineWidth',2);  
    line([t7_time_offwf t7_time_offwf],[ymin ymax],'Color',[1 0.2 0.7],'LineStyle','--','LineWidth',2);  
end  
  
end
```



**Appendix B**  
**Short-Circuit Fault Waveforms for a GaN GIT with Overcurrent Protection Circuit**

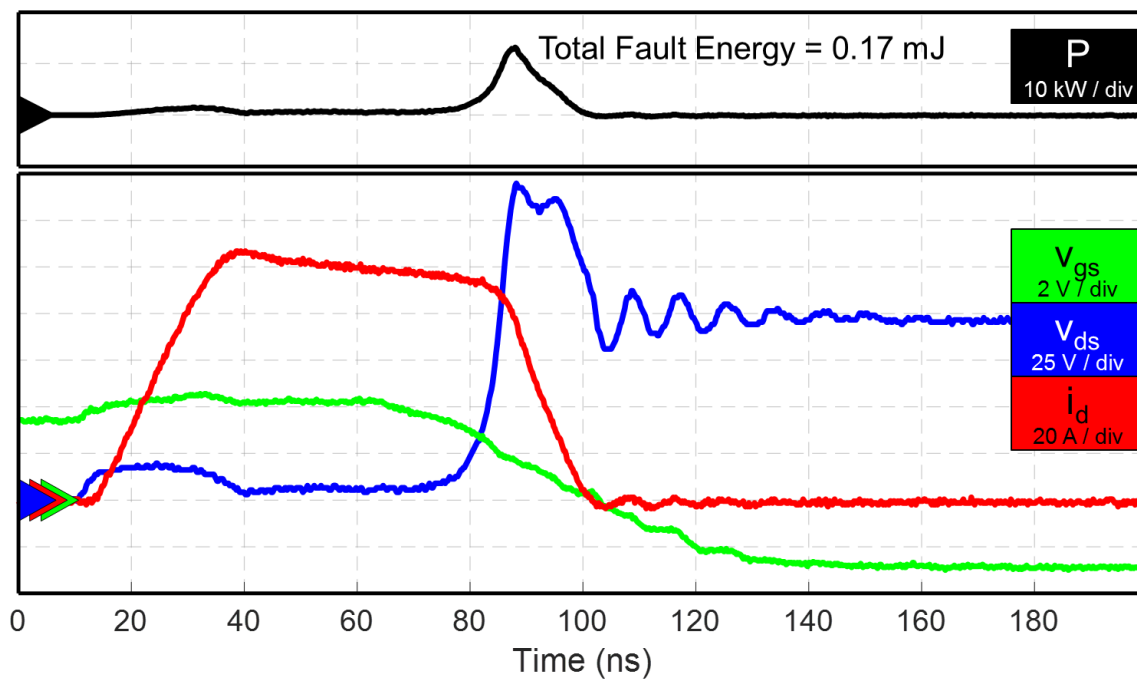


Figure B.1. Fault Under Load for Infineon GIT at 100 V, 25 °C

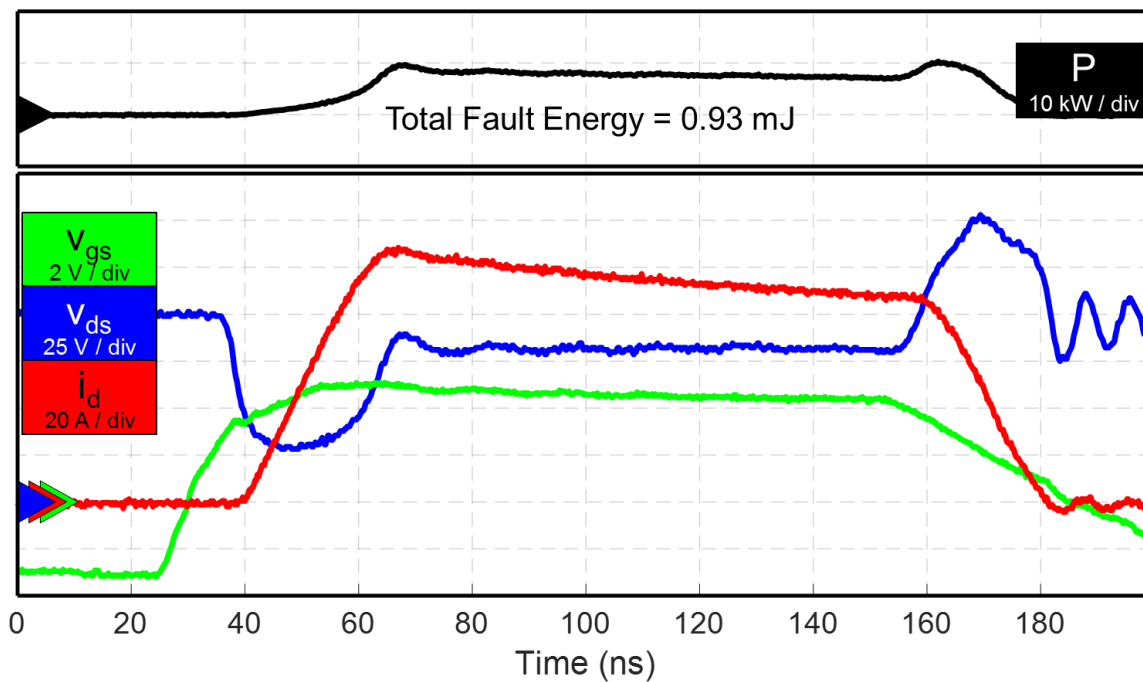


Figure B.2. Hard Switching Fault for Infineon GIT at 100 V, 25 °C

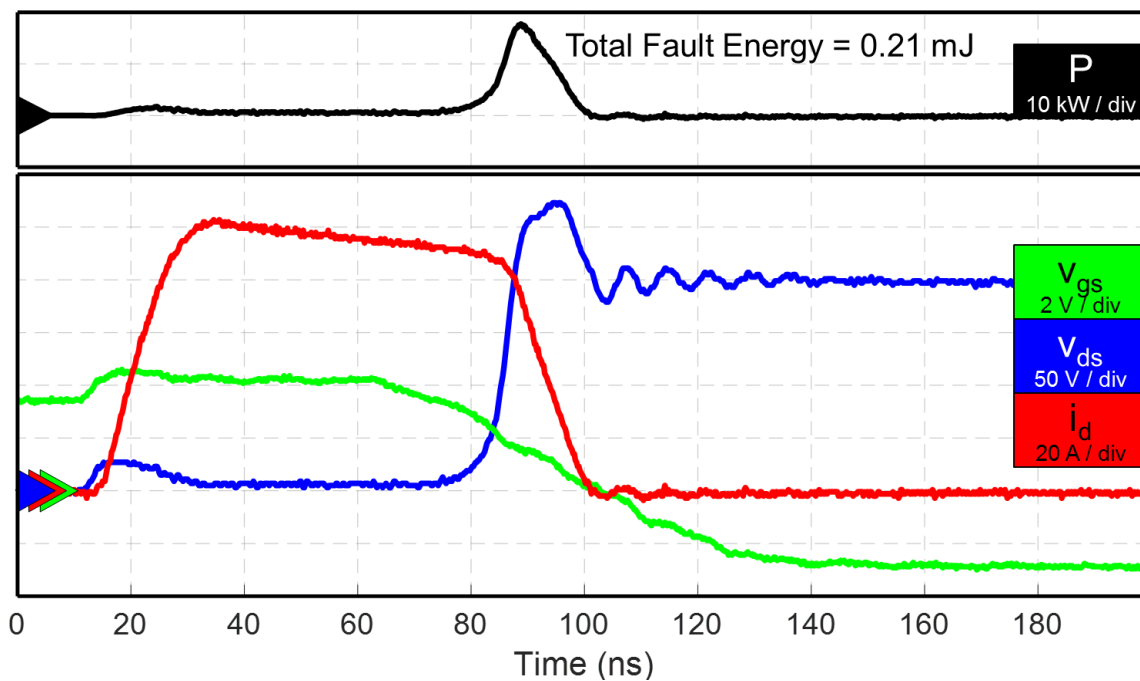


Figure B.3. Fault Under Load for Infineon GIT at 200 V, 25 °C

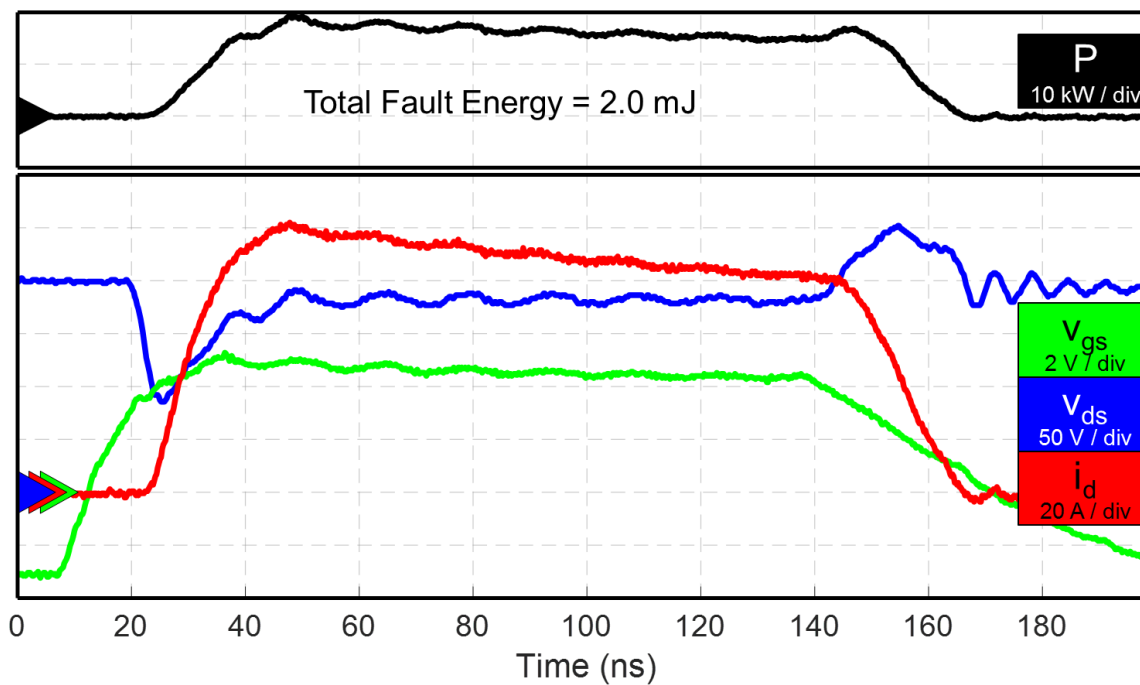


Figure B.4. Hard Switching Fault for Infineon GIT at 200 V, 25 °C

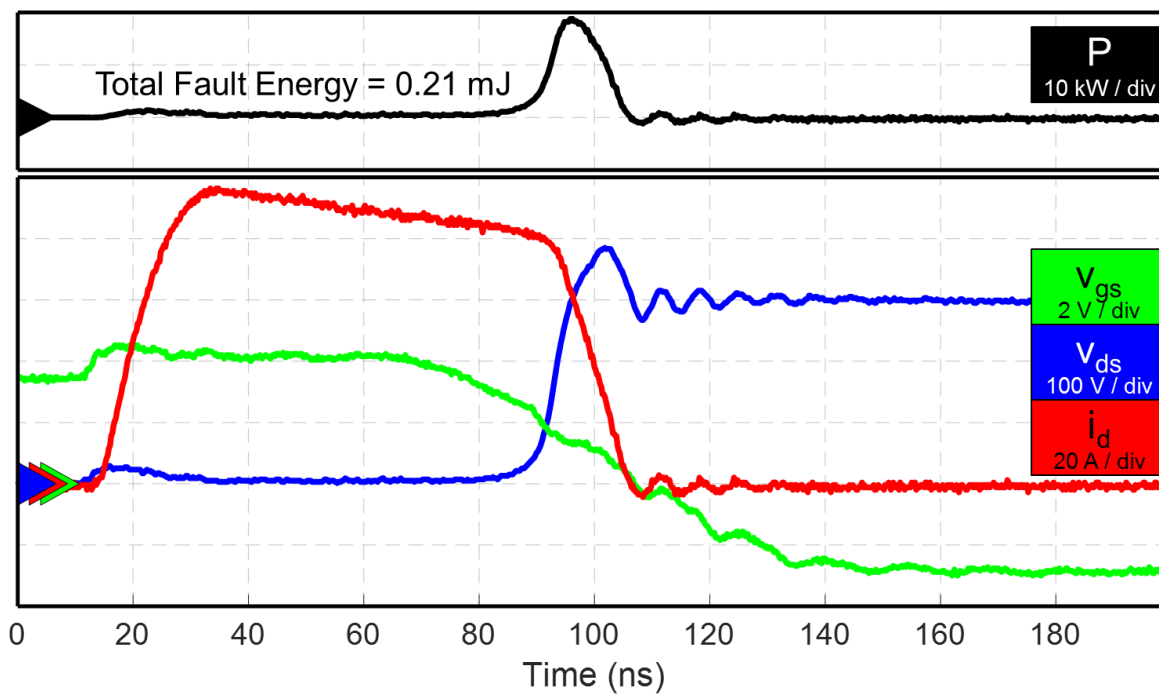


Figure B.5. Fault Under Load for Infineon GIT at 300 V, 25 °C

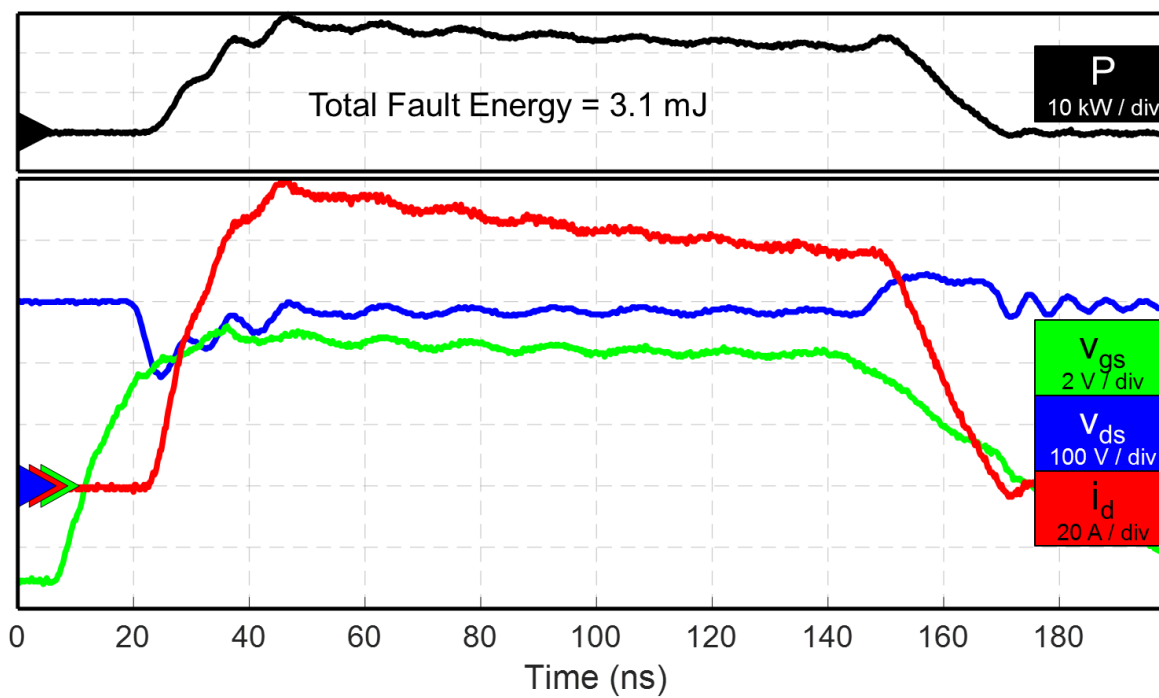


Figure B.6. Hard Switching Fault for Infineon GIT at 300 V, 25 °C

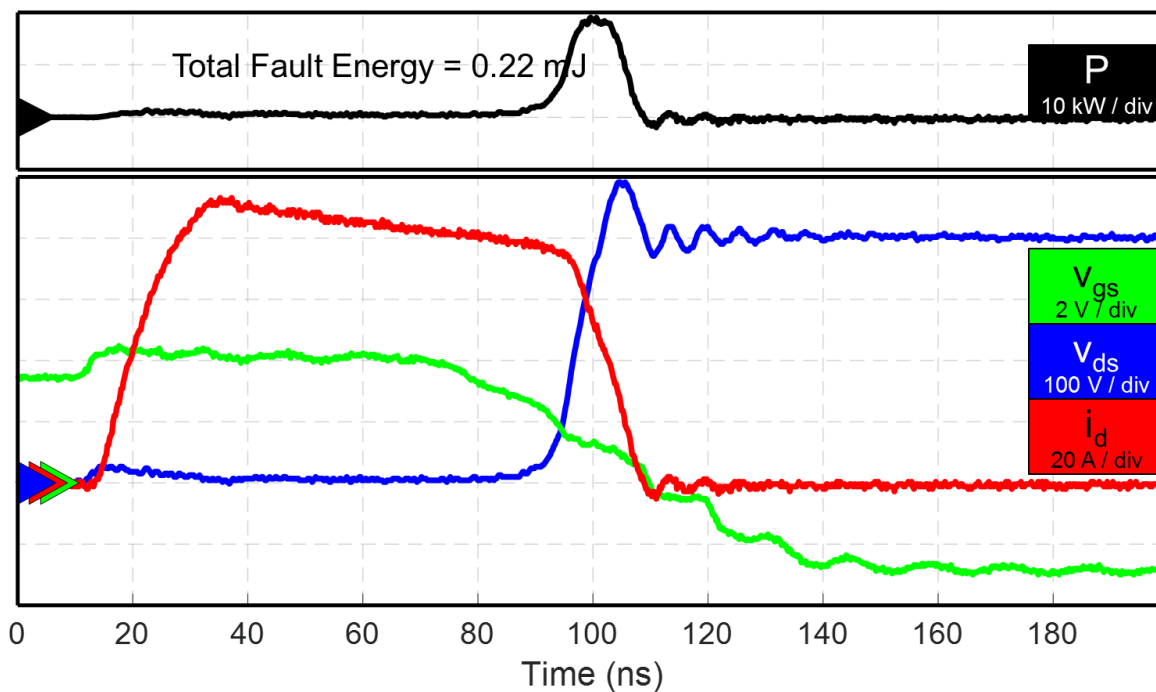


Figure B.7. Fault Under Load for Infineon GIT at 400 V, 25 °C

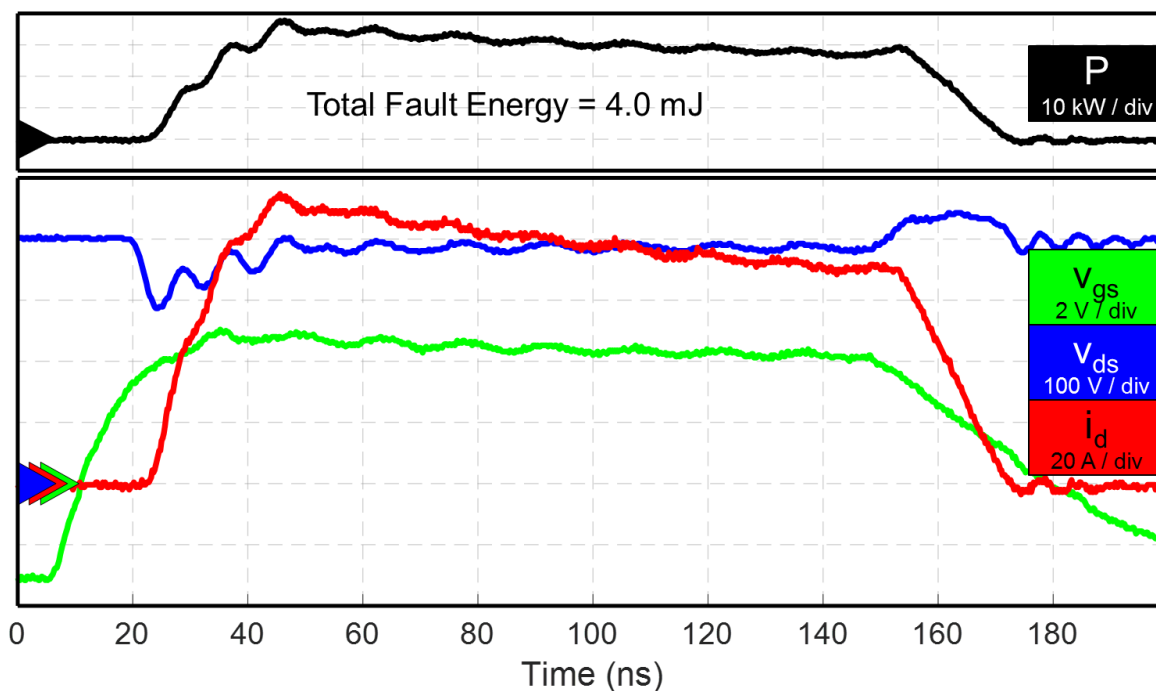


Figure B.8. Hard Switching Fault for Infineon GIT at 400 V, 25 °C

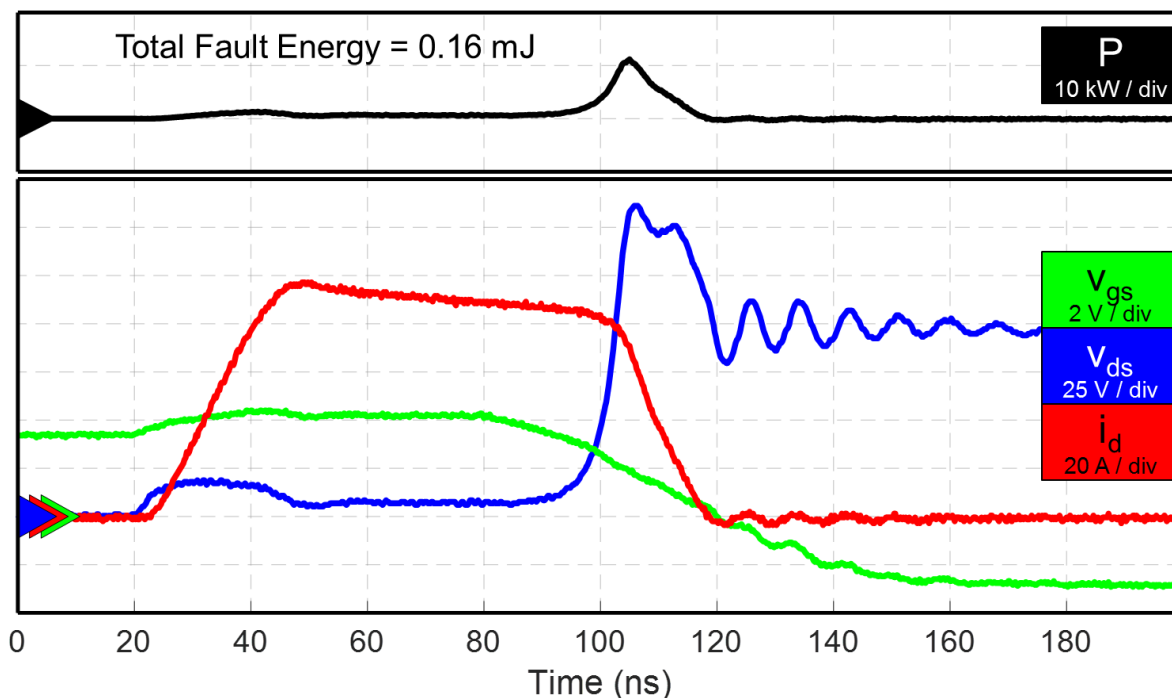


Figure B.9. Fault Under Load for Infineon GIT at 100 V, 50 °C

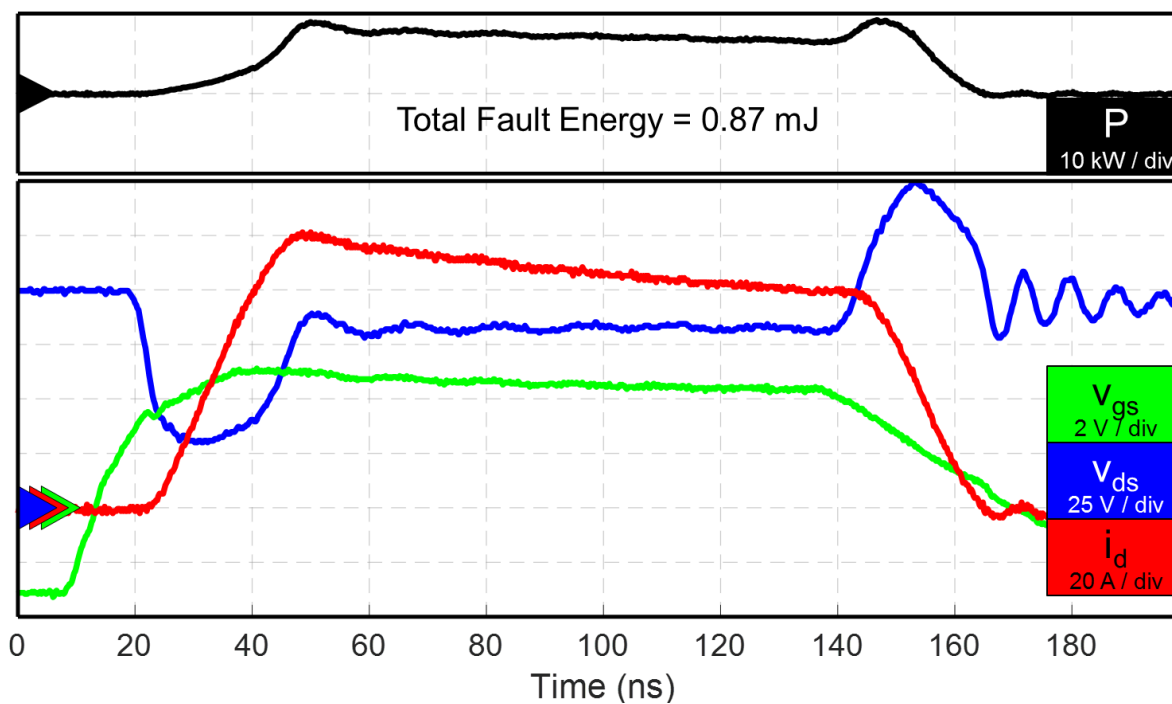


Figure B.10. Hard Switching Fault for Infineon GIT at 100 V, 50 °C

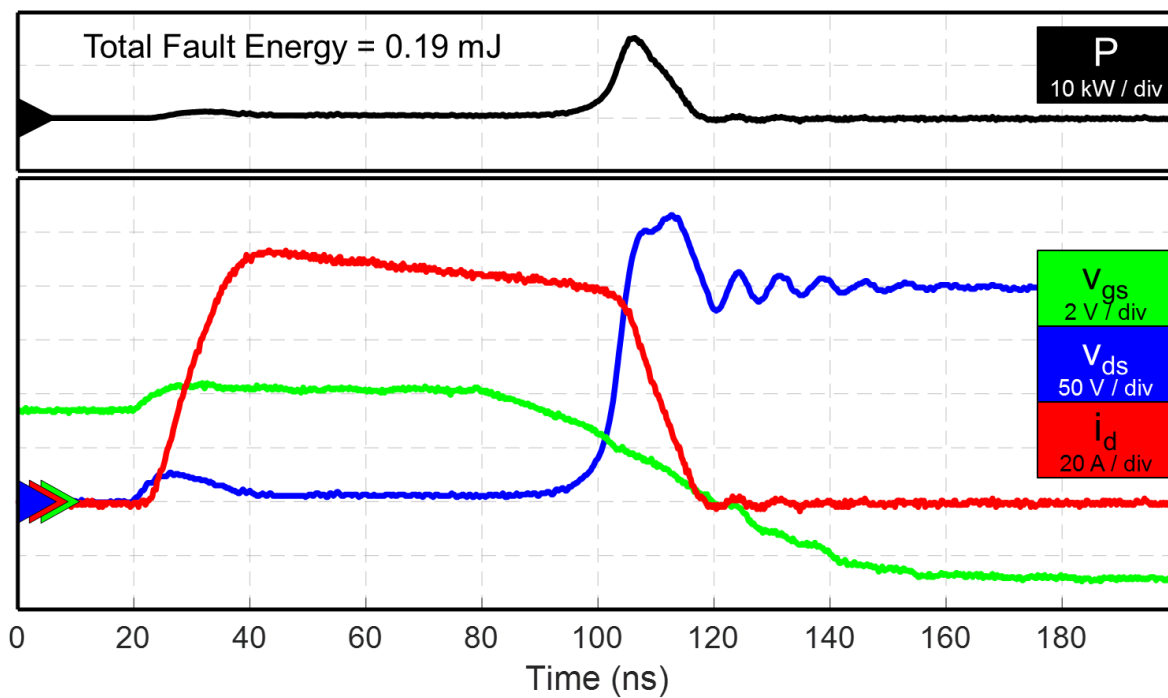


Figure B.11. Fault Under Load for Infineon GIT at 200 V, 50 °C

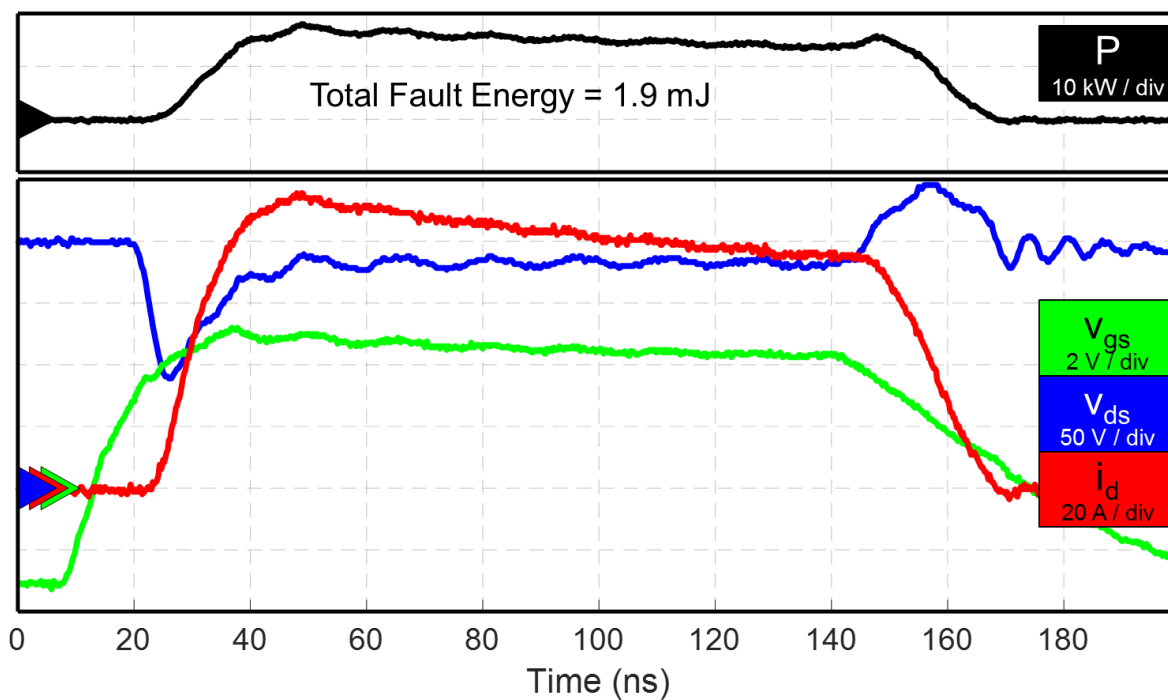


Figure B.12. Hard Switching Fault for Infineon GIT at 200 V, 50 °C

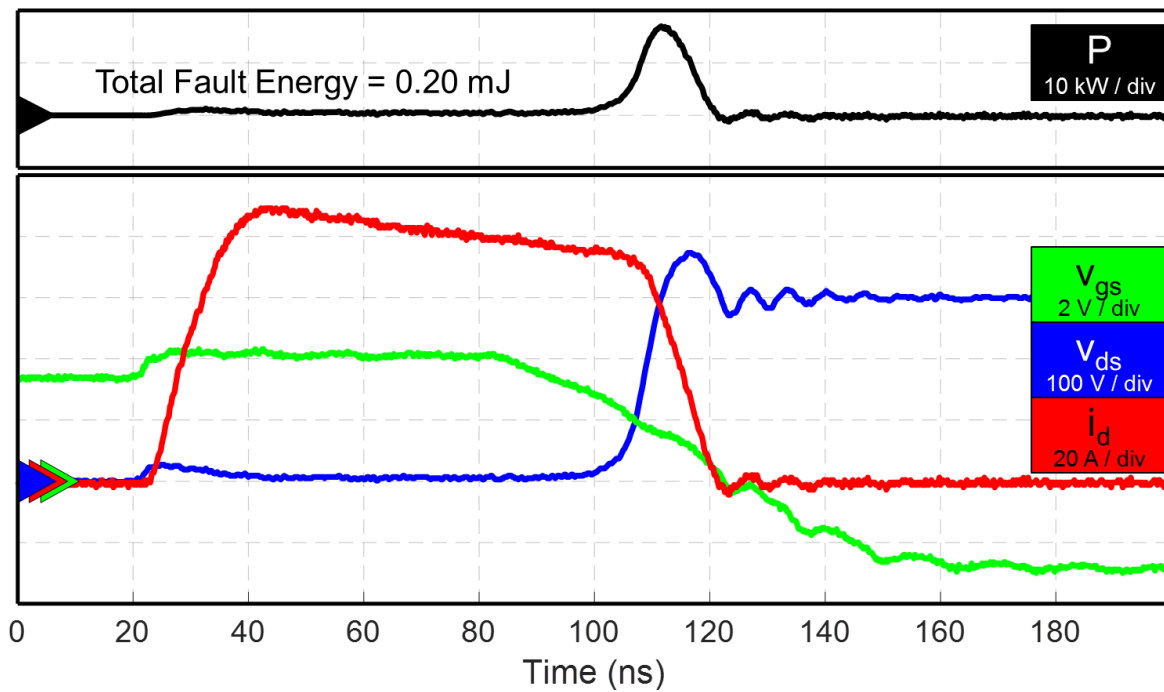


Figure B.13. Fault Under Load for Infineon GIT at 300 V, 50 °C

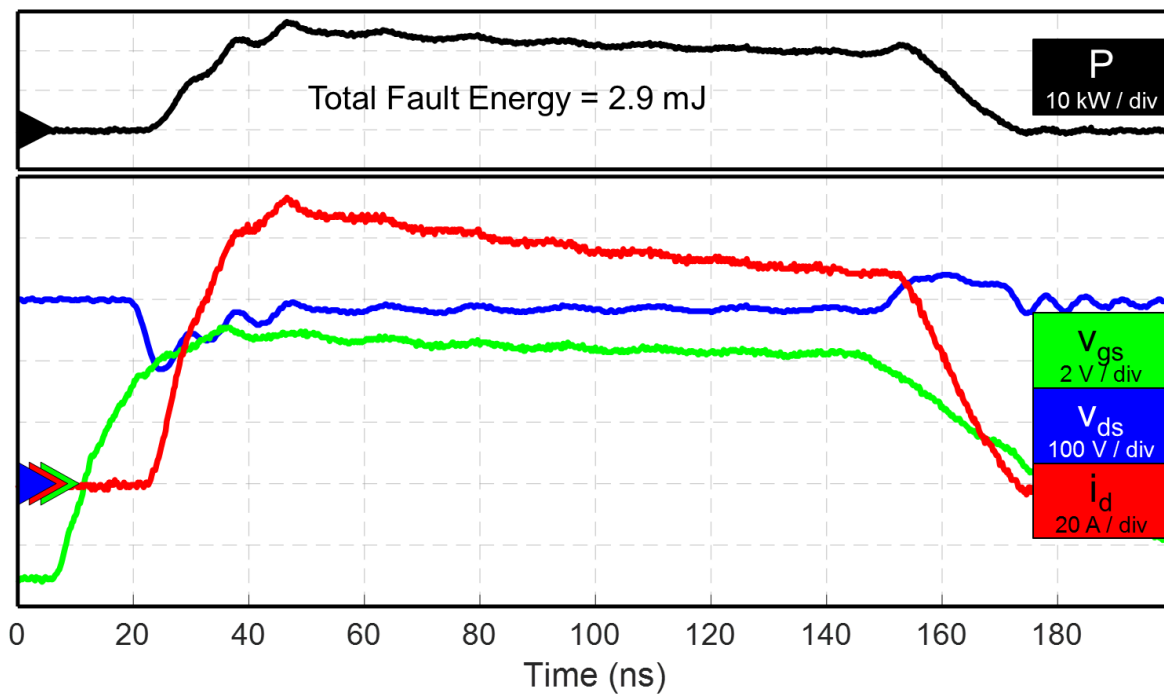


Figure B.14. Hard Switching Fault for Infineon GIT at 300 V, 50 °C



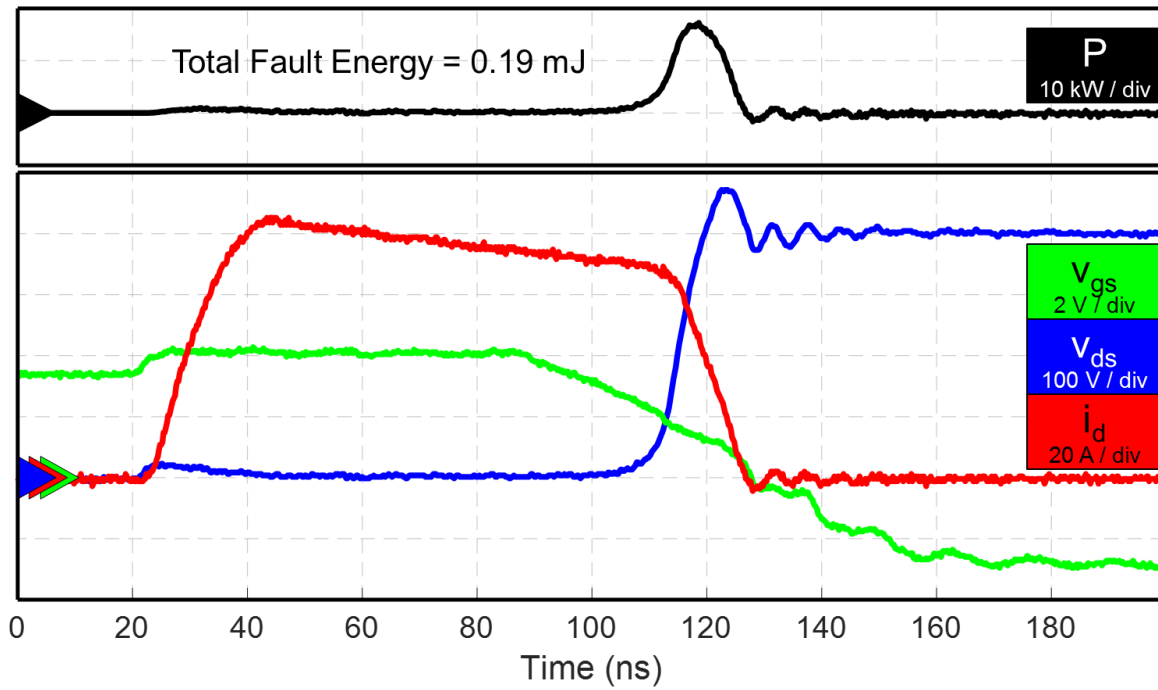


Figure B.15. Fault Under Load for Infineon GIT at 400 V, 50 °C

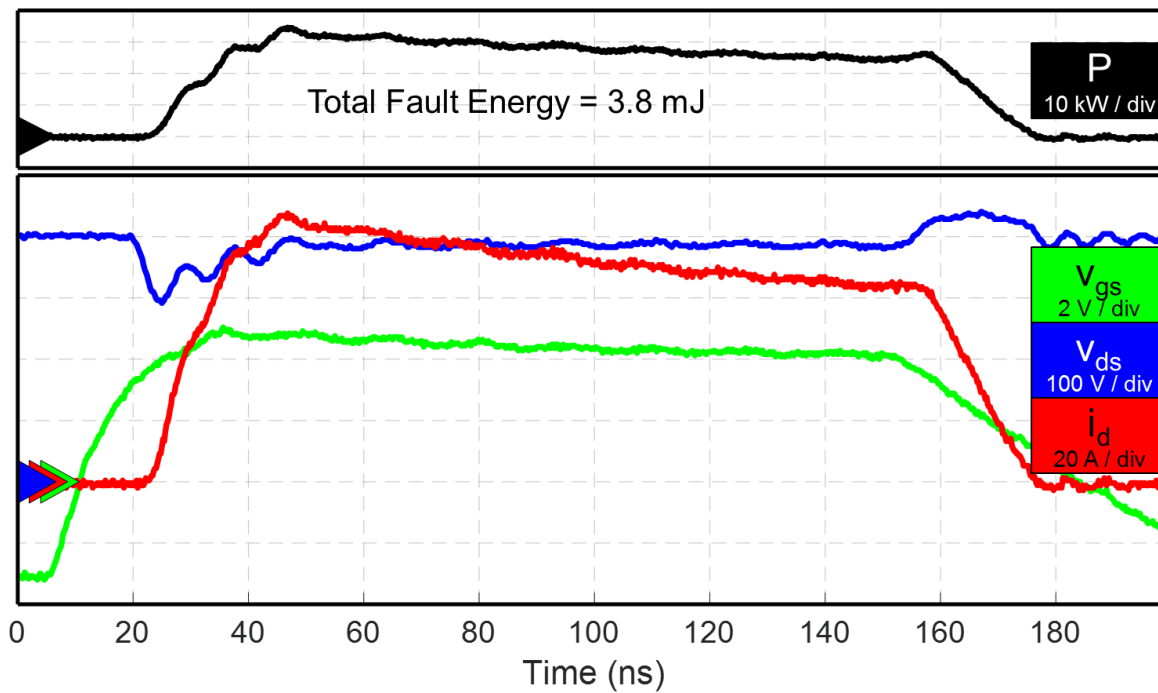


Figure B.16. Hard Switching Fault for Infineon GIT at 400 V, 50 °C

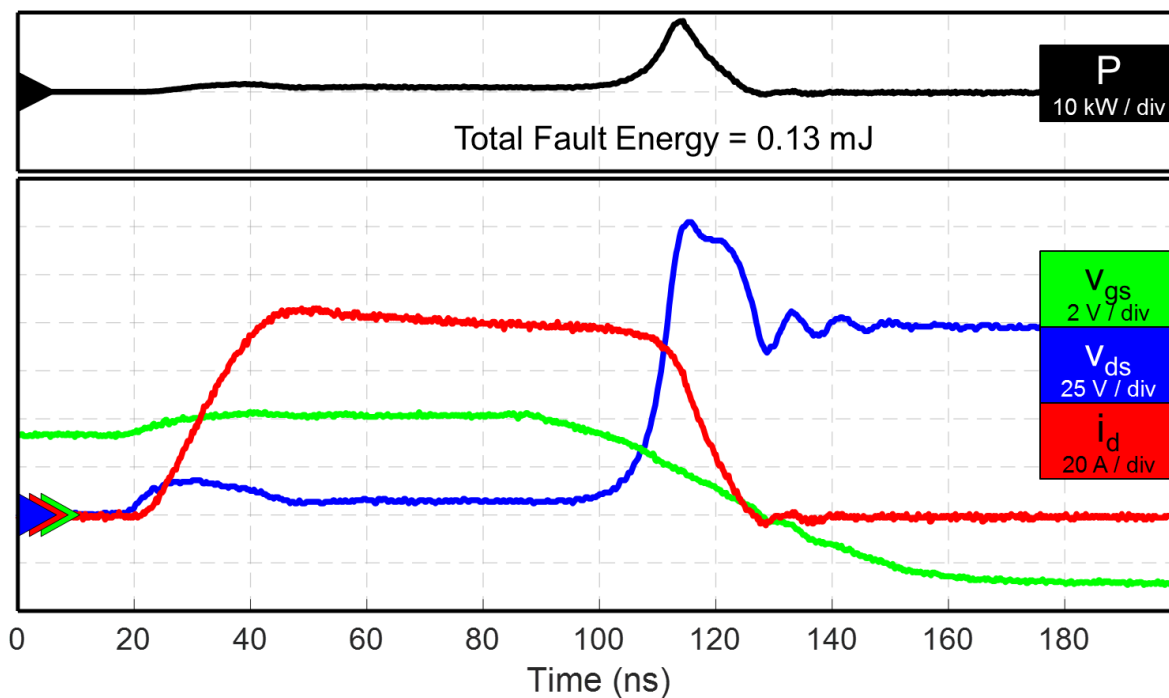


Figure B.17. Fault Under Load for Infineon GIT at 100 V, 75 °C

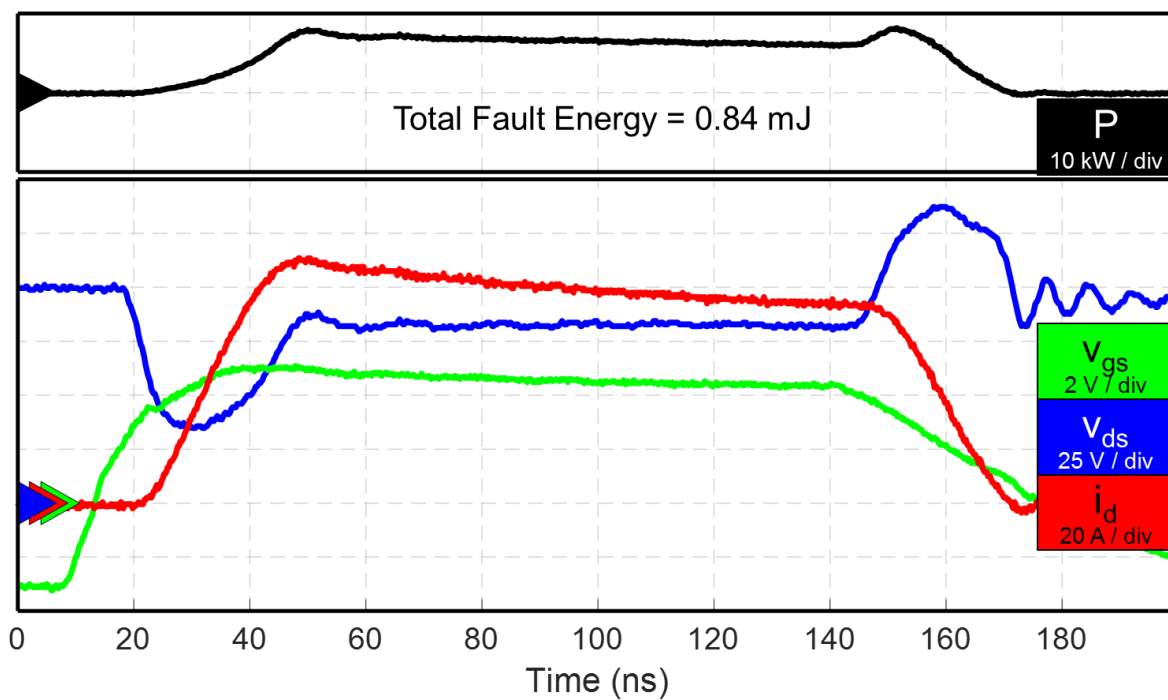


Figure B.18. Hard Switching Fault for Infineon GIT at 100 V, 75 °C

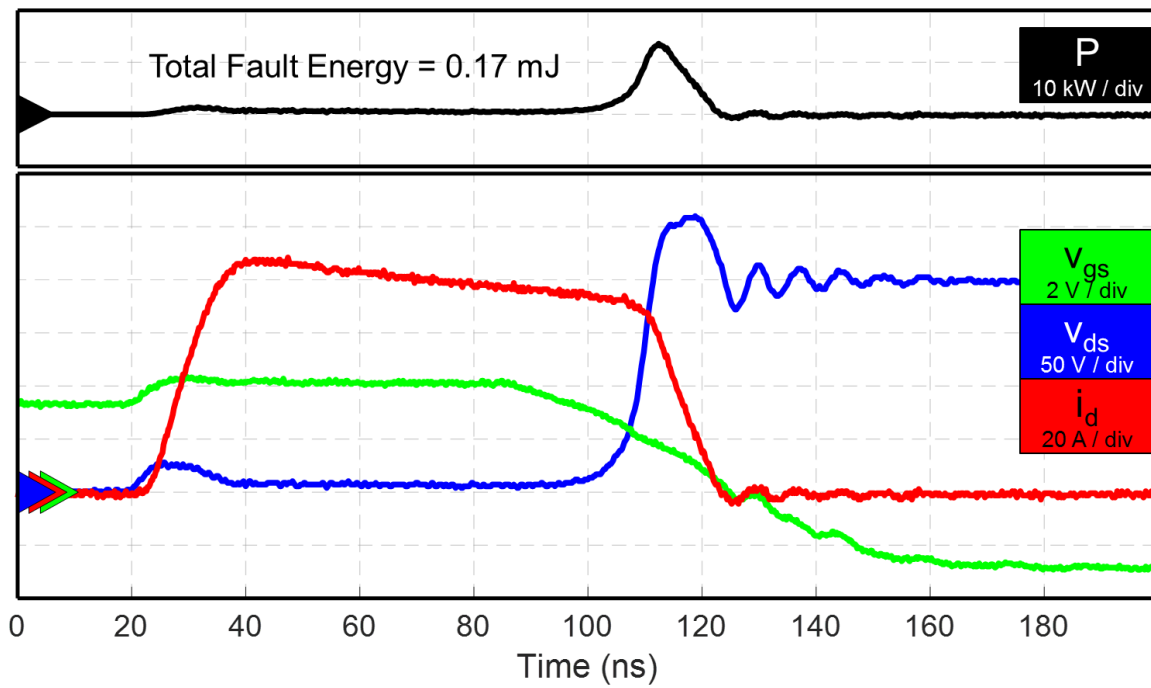


Figure B.19. Fault Under Load for Infineon GIT at 200 V, 75 °C

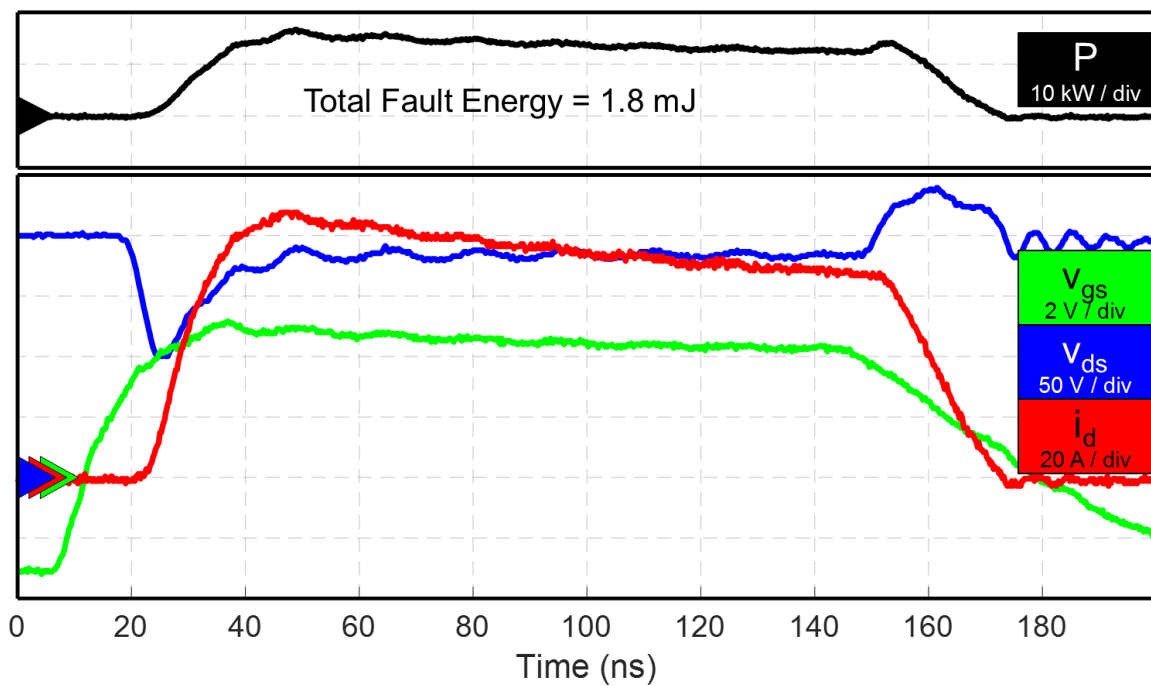


Figure B.20. Hard Switching Fault for Infineon GIT at 200 V, 75 °C

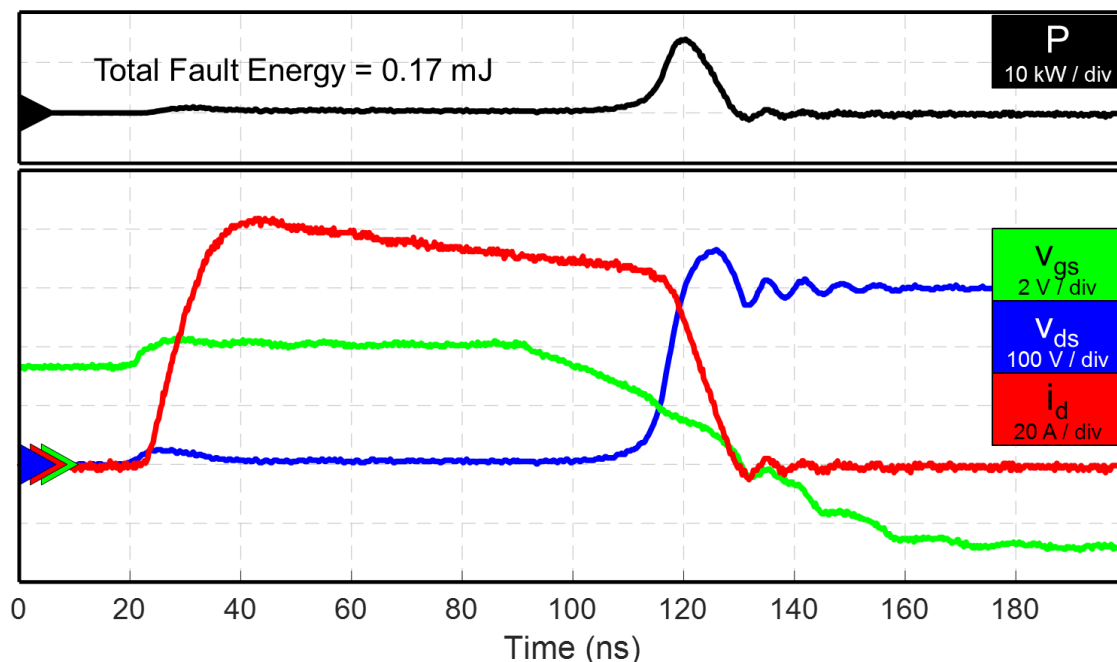


Figure B.21. Fault Under Load for Infineon GIT at 300 V, 75 °C

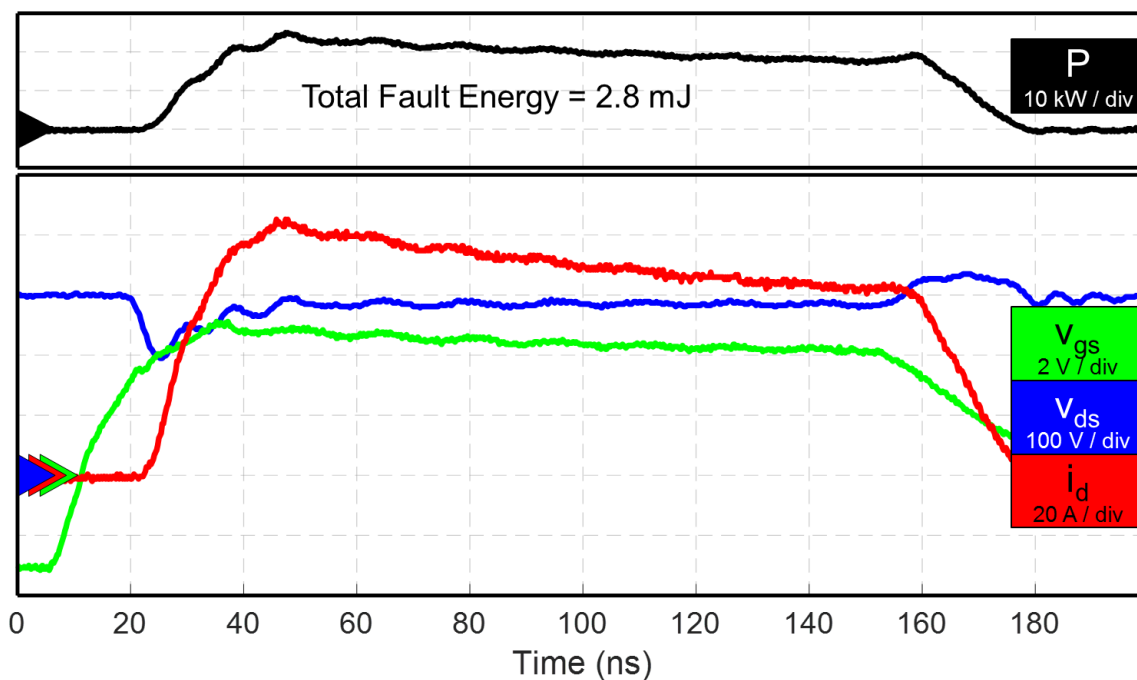


Figure B.22. Hard Switching Fault for Infineon GIT at 300 V, 75 °C

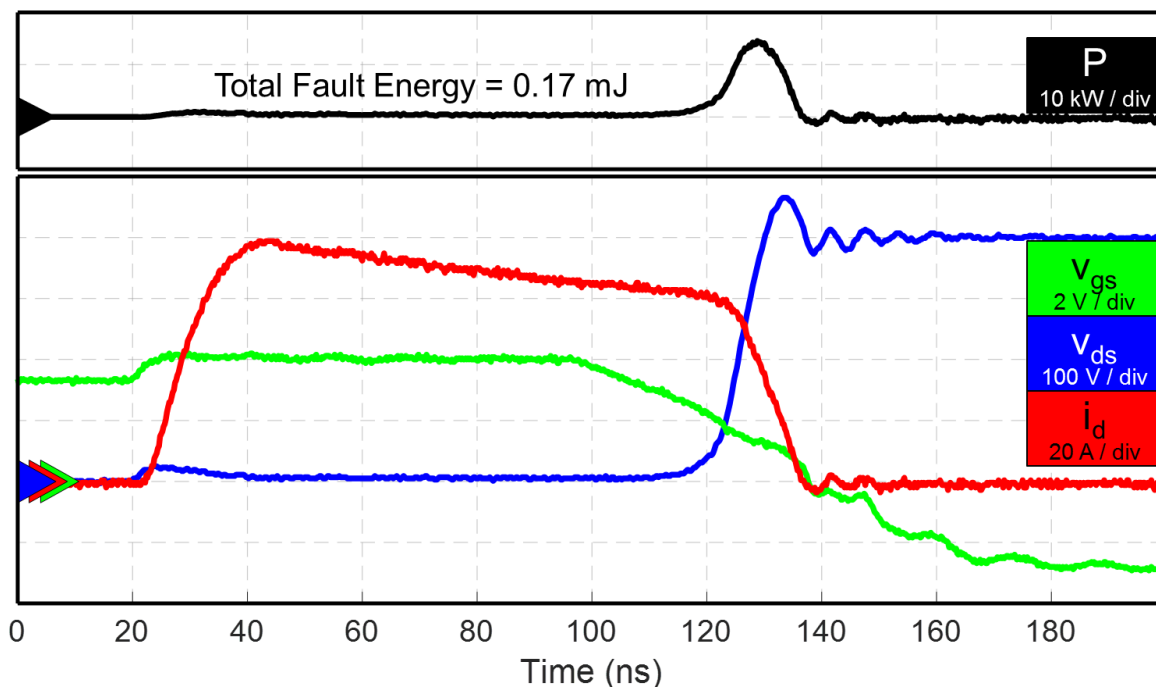


Figure B.23. Fault Under Load for Infineon GIT at 400 V, 75 °C

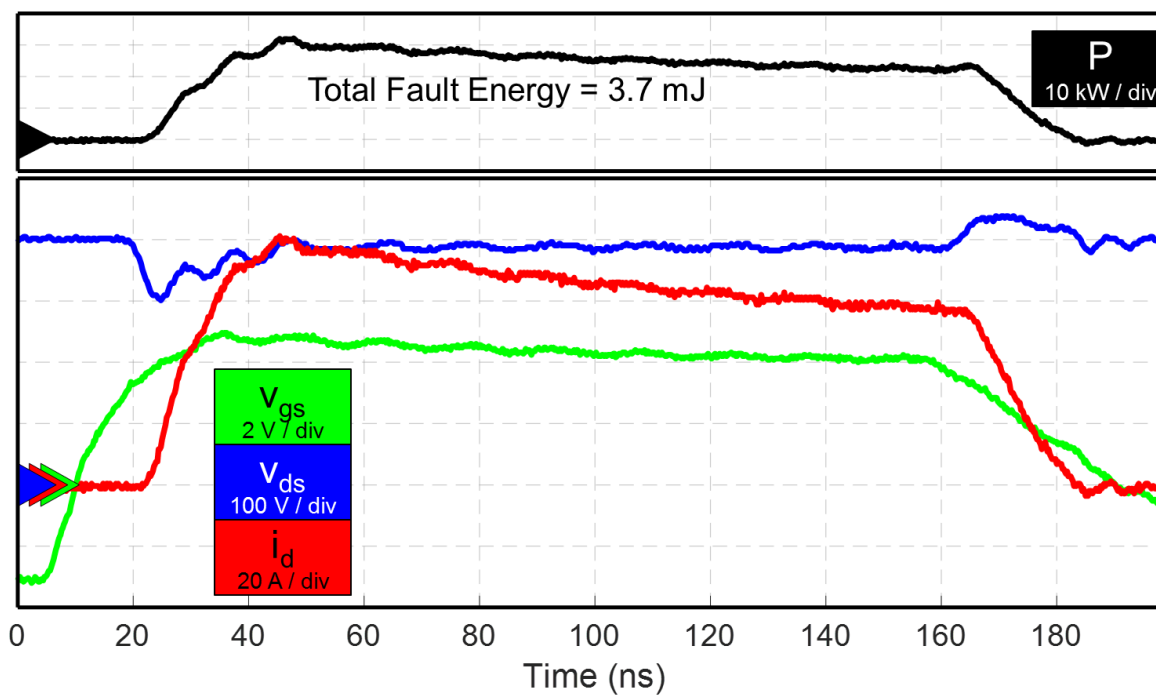


Figure B.24. Hard Switching Fault for Infineon GIT at 400 V, 75 °C

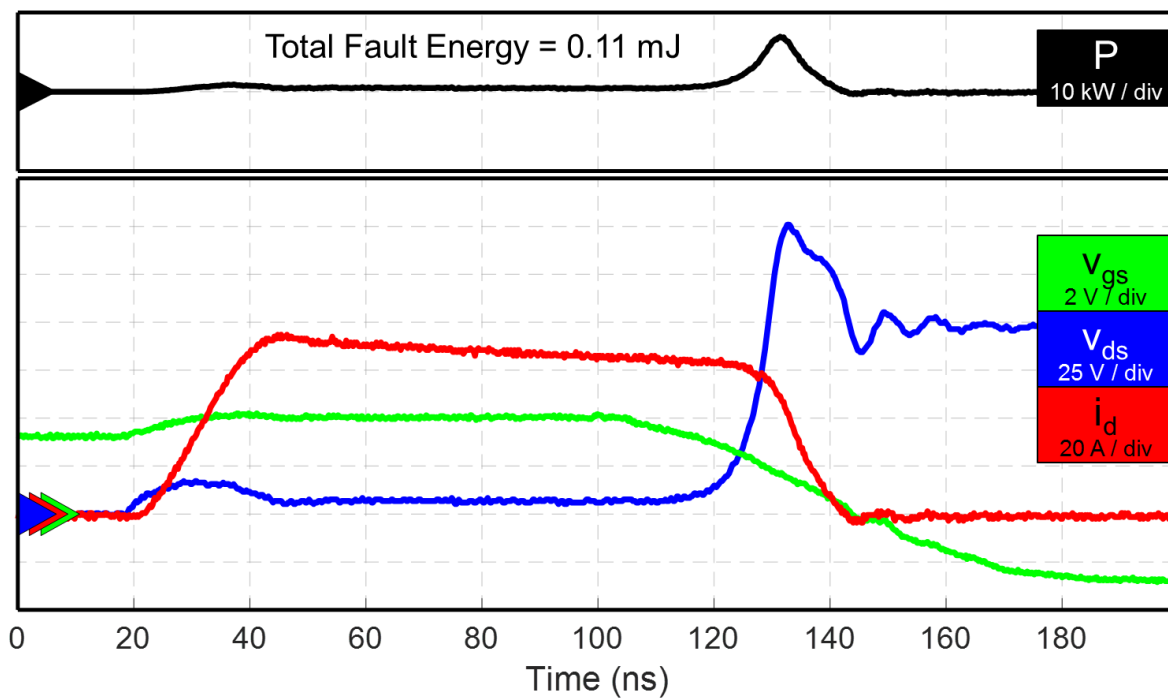


Figure B.25. Fault Under Load for Infineon GIT at 100 V, 100 °C

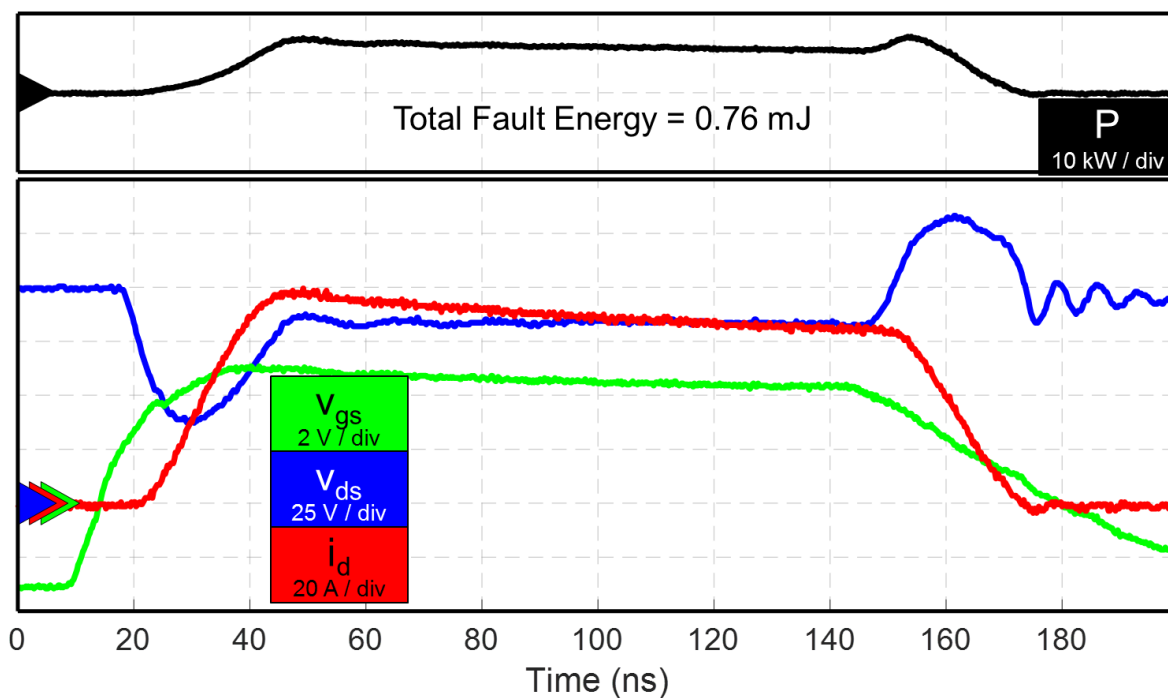


Figure B.26. Hard Switching Fault for Infineon GIT at 100 V, 100 °C

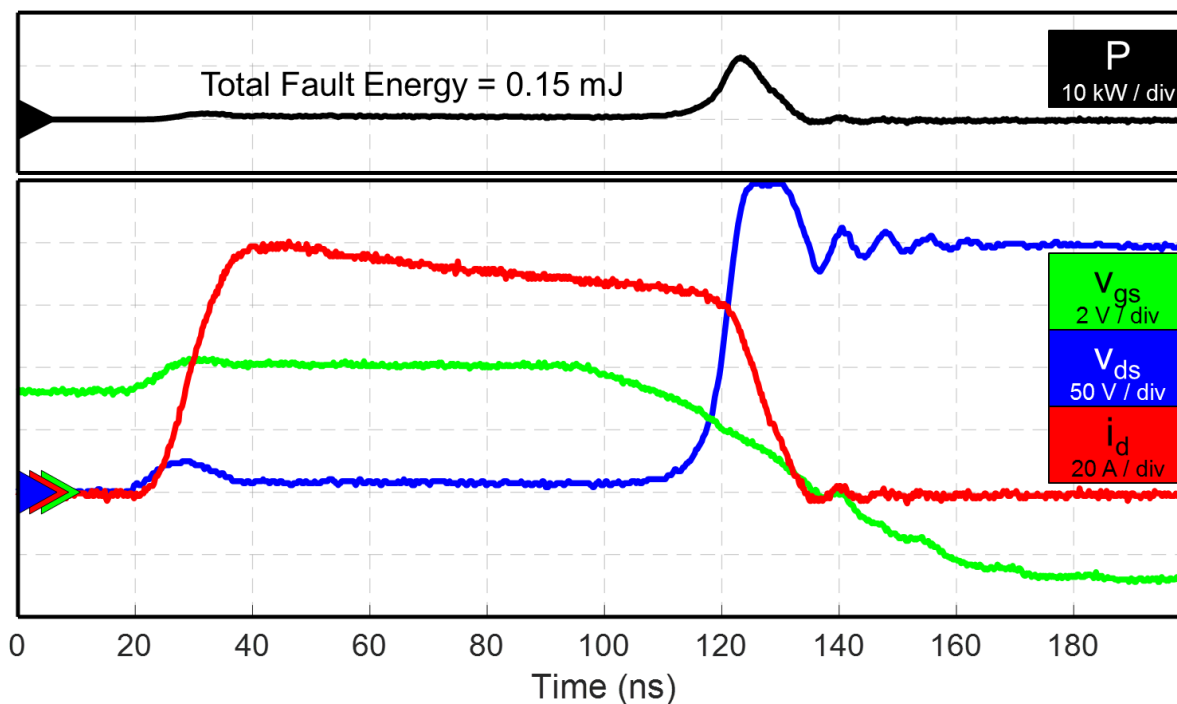


Figure B.27. Fault Under Load for Infineon GIT at 200 V, 100 °C

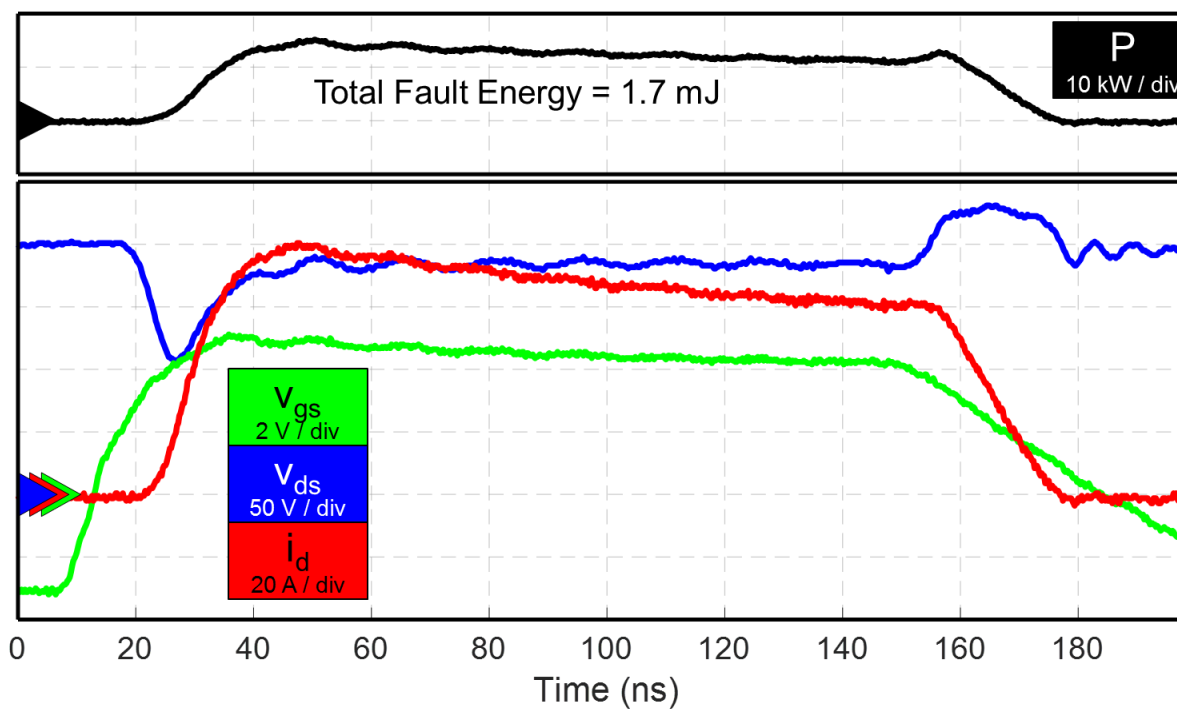


Figure B.28. Hard Switching Fault for Infineon GIT at 200 V, 100 °C

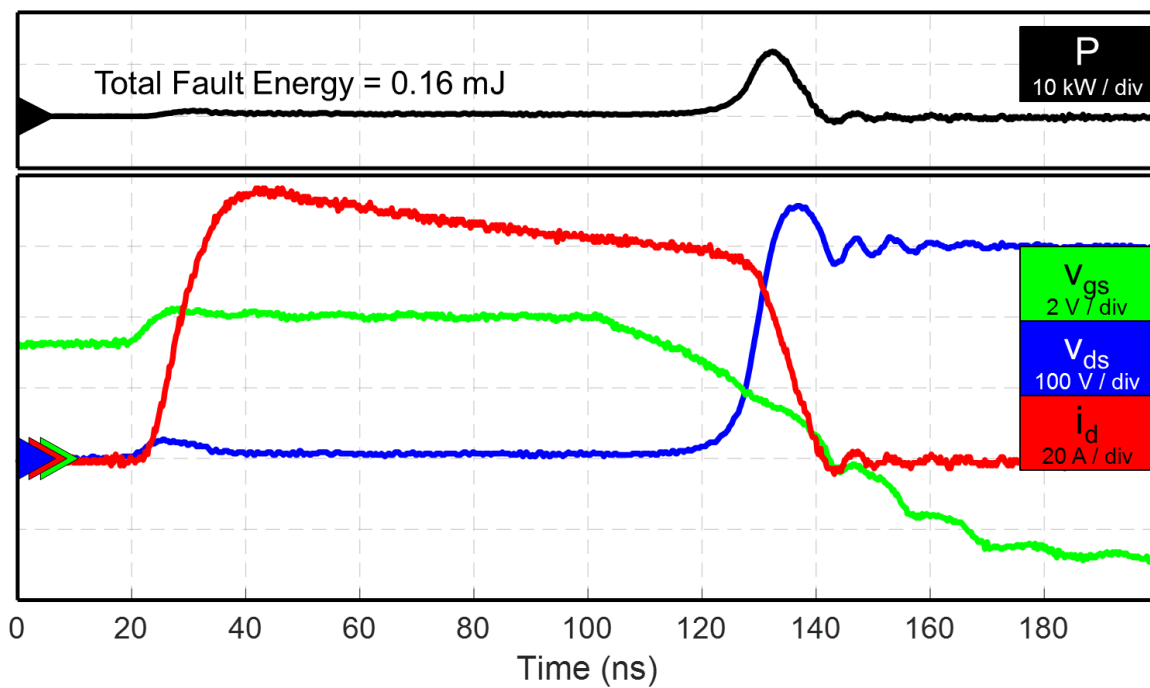


Figure B.29. Fault Under Load for Infineon GIT at 300 V, 100 °C

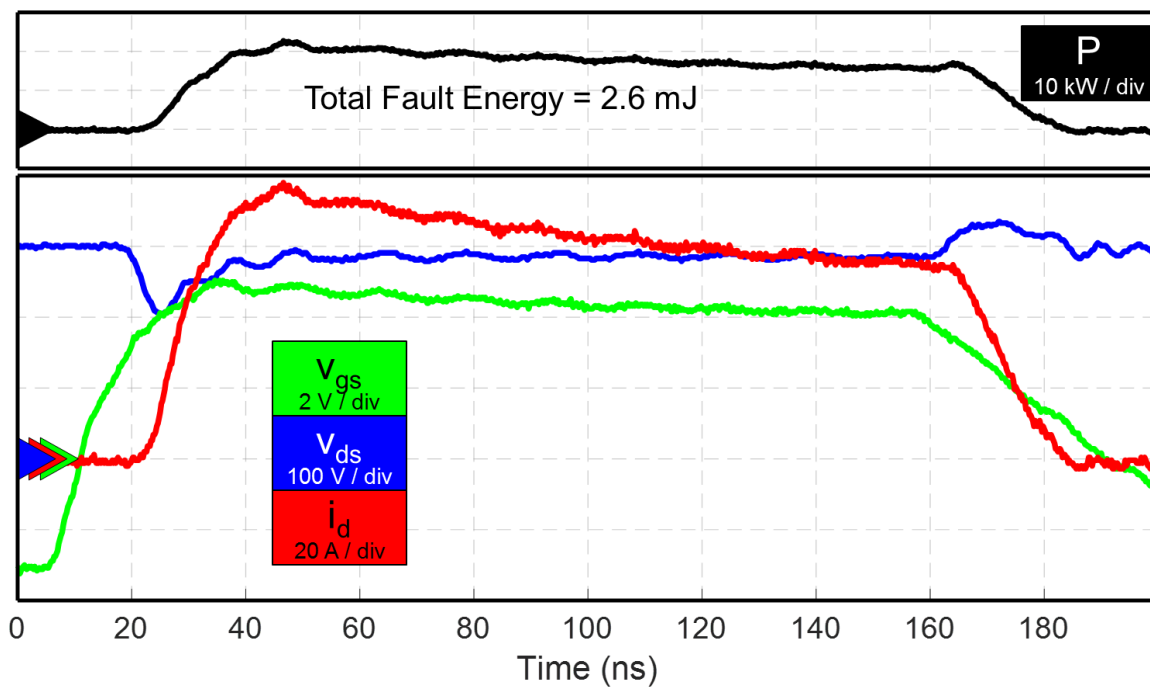


Figure B.30. Hard Switching Fault for Infineon GIT at 300 V, 100 °C



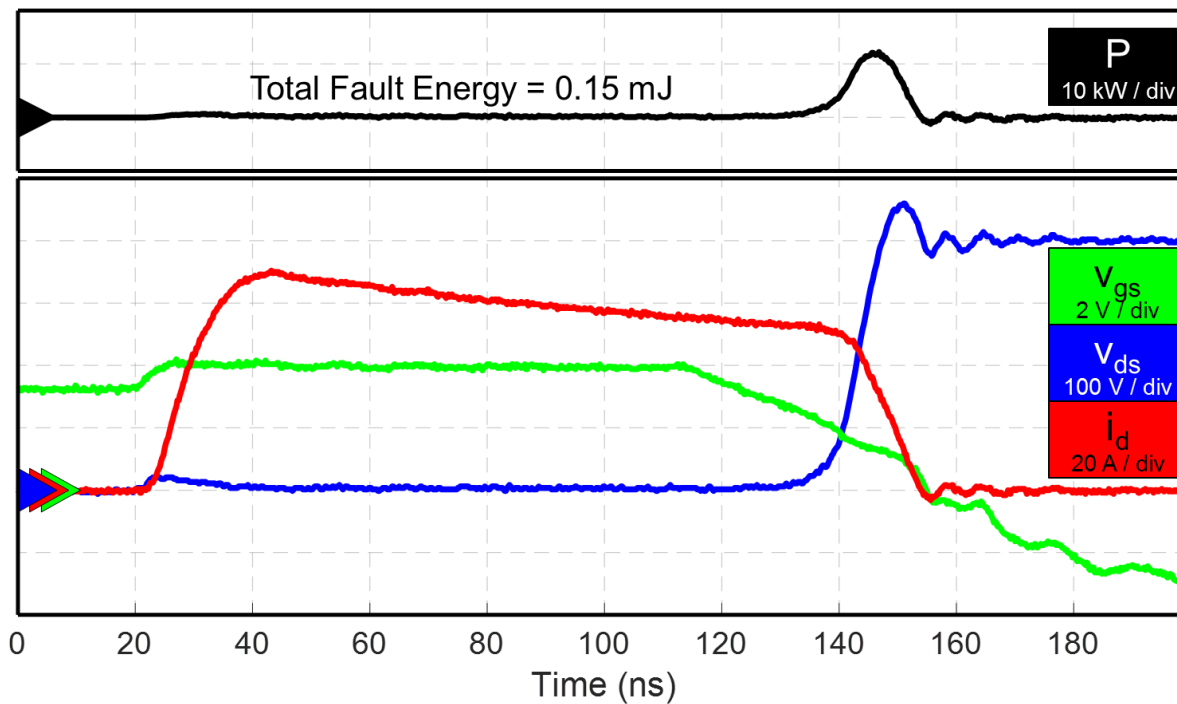


Figure B.31. Fault Under Load for Infineon GIT at 400 V, 100 °C

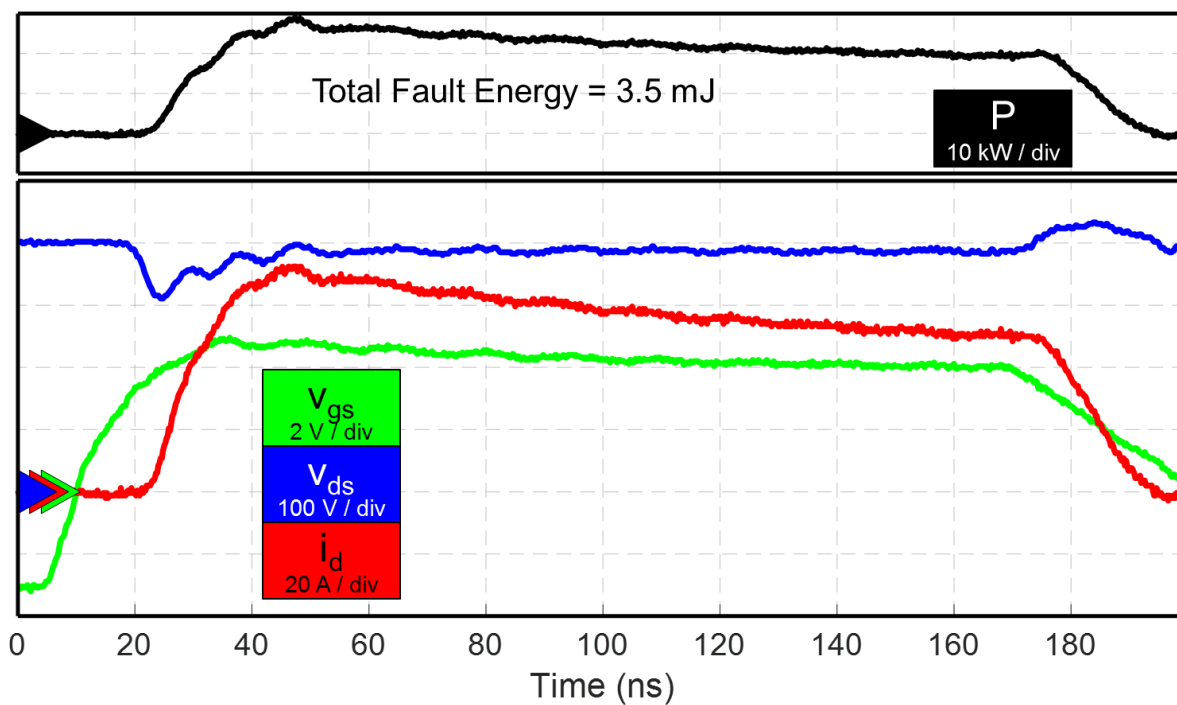


Figure B.32. Hard Switching Fault for Infineon GIT at 400 V, 100 °C

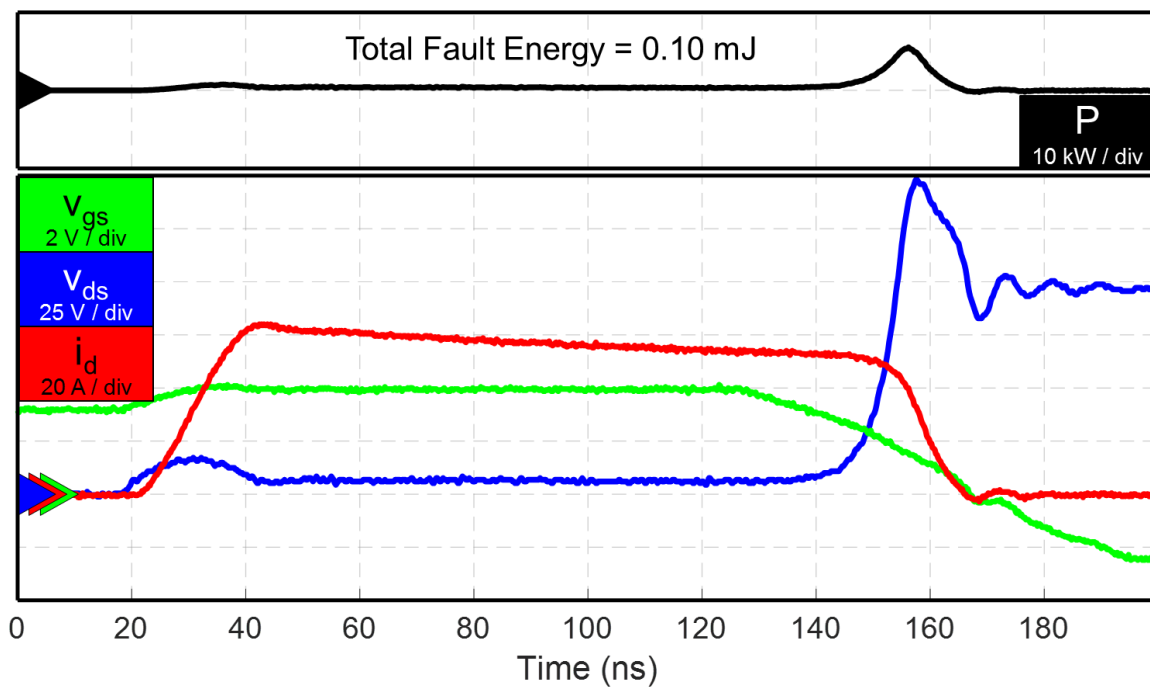


Figure B.33. Fault Under Load for Infineon GIT at 100 V, 125 °C

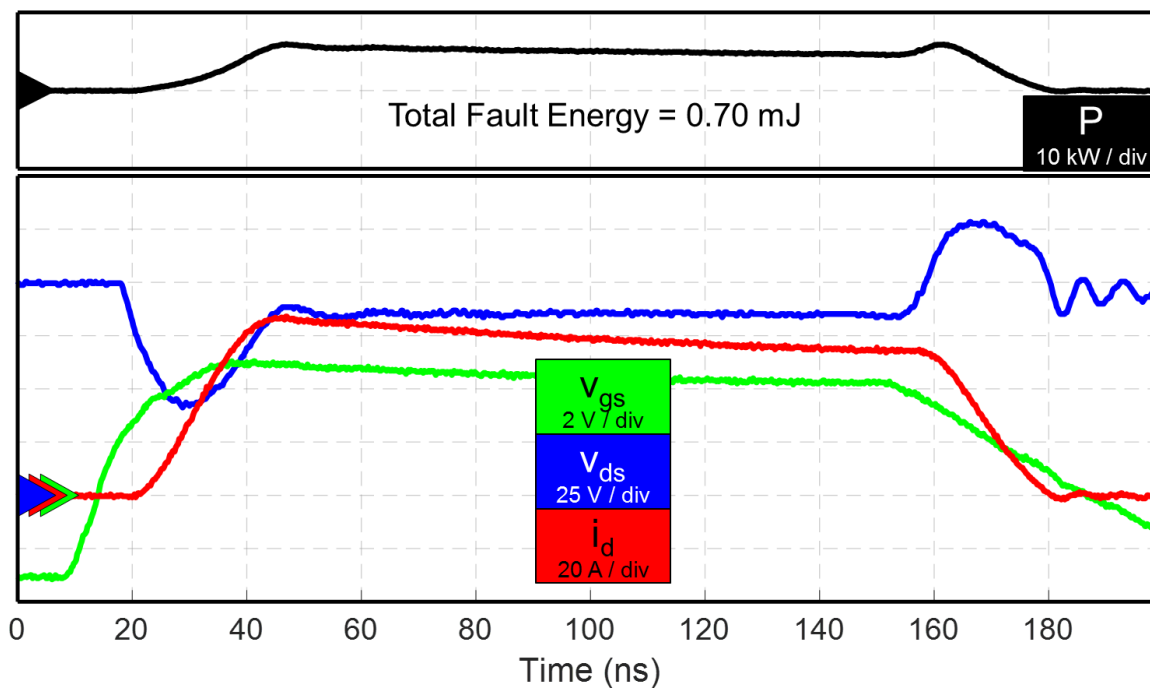


Figure B.34. Hard Switching Fault for Infineon GIT at 100 V, 125 °C

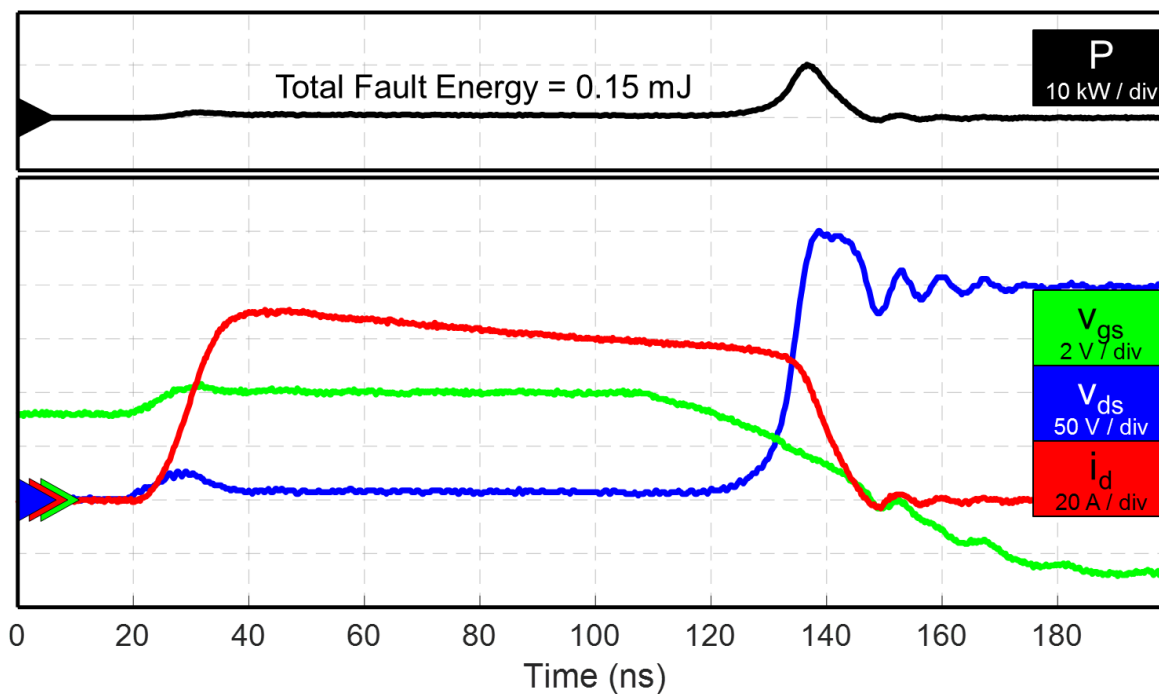


Figure B.35. Fault Under Load for Infineon GIT at 200 V, 125 °C

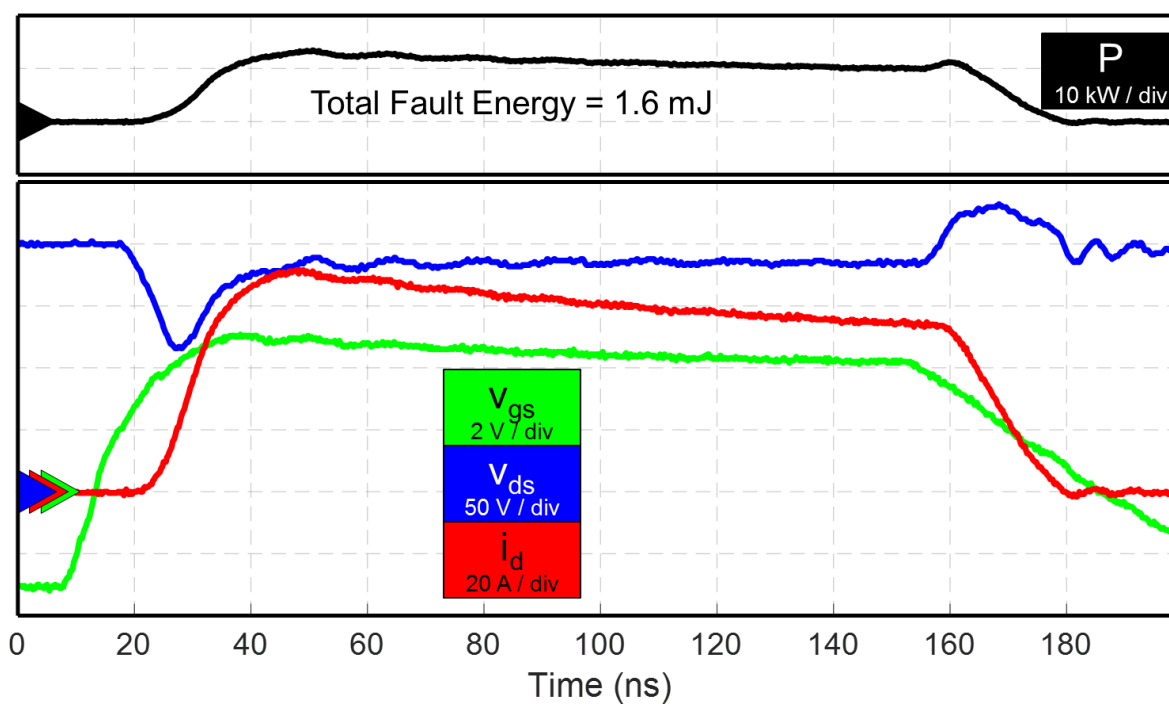


Figure B.36. Hard Switching Fault for Infineon GIT at 200 V, 125 °C

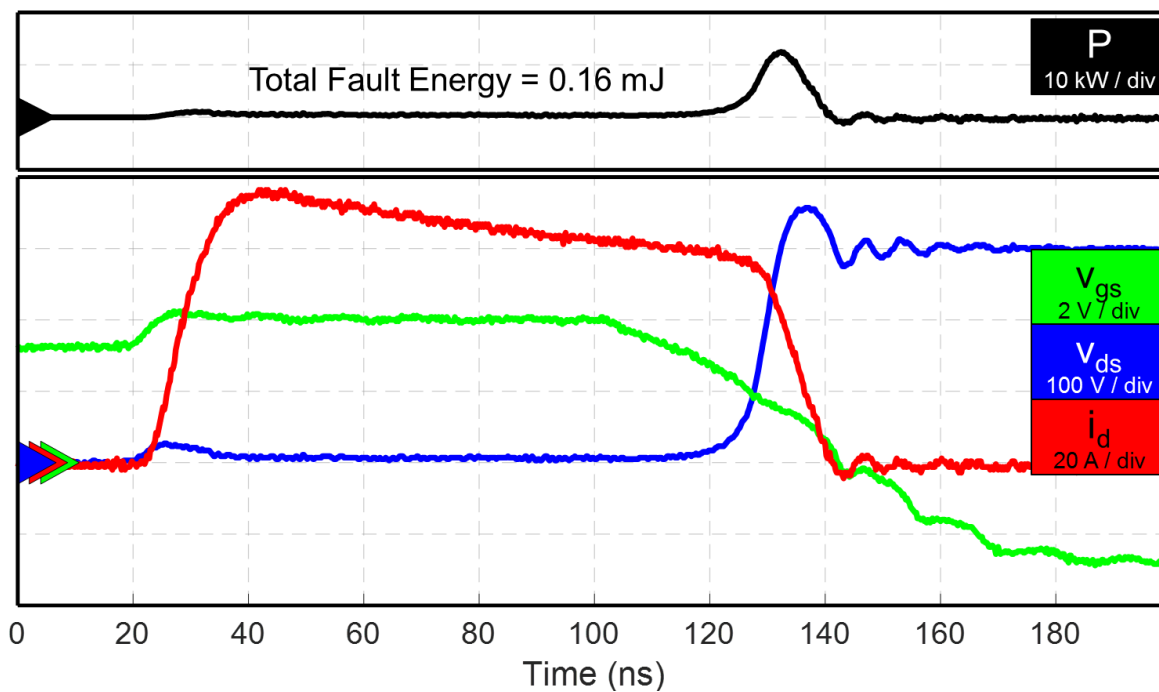


Figure B.37. Fault Under Load for Infineon GIT at 300 V, 125 °C

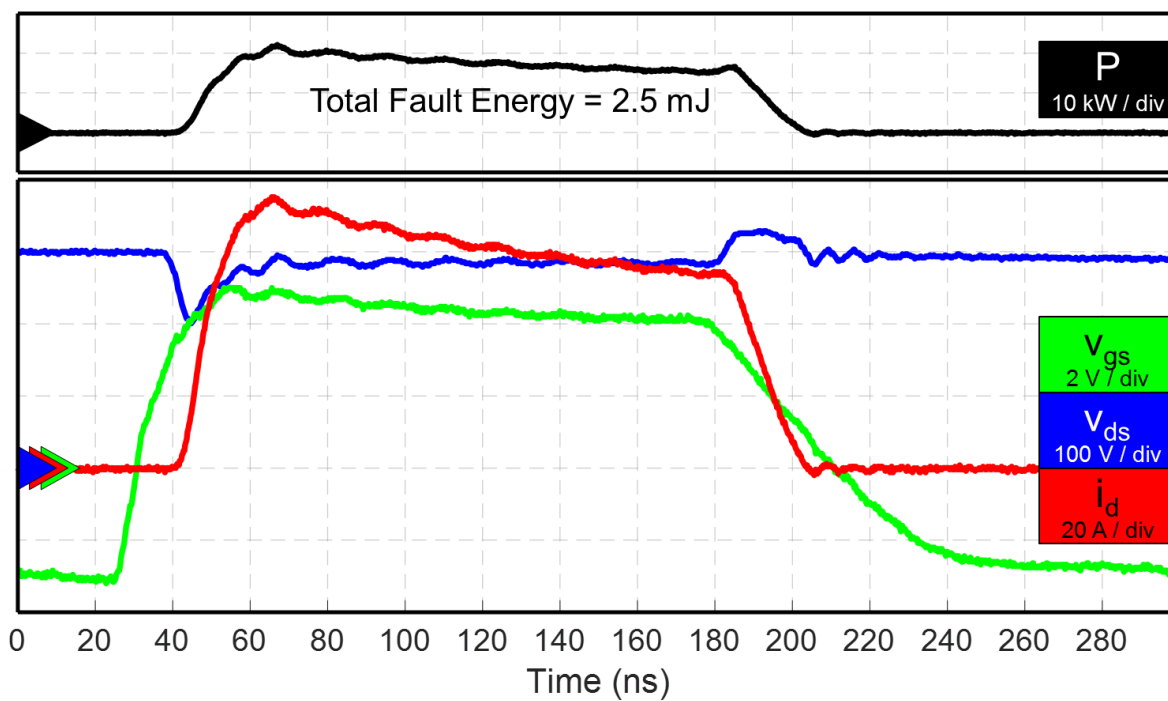


Figure B.38. Hard Switching Fault for Infineon GIT at 300 V, 125 °C

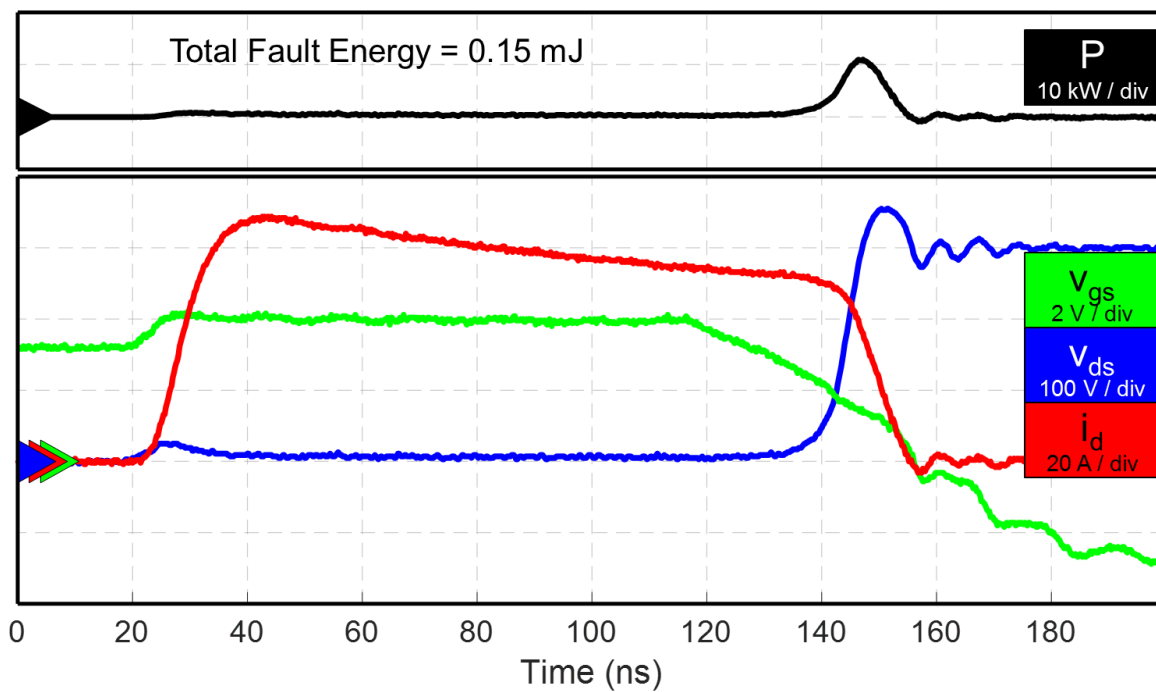


Figure B.39. Fault Under Load for Infineon GIT at 400 V, 125 °C

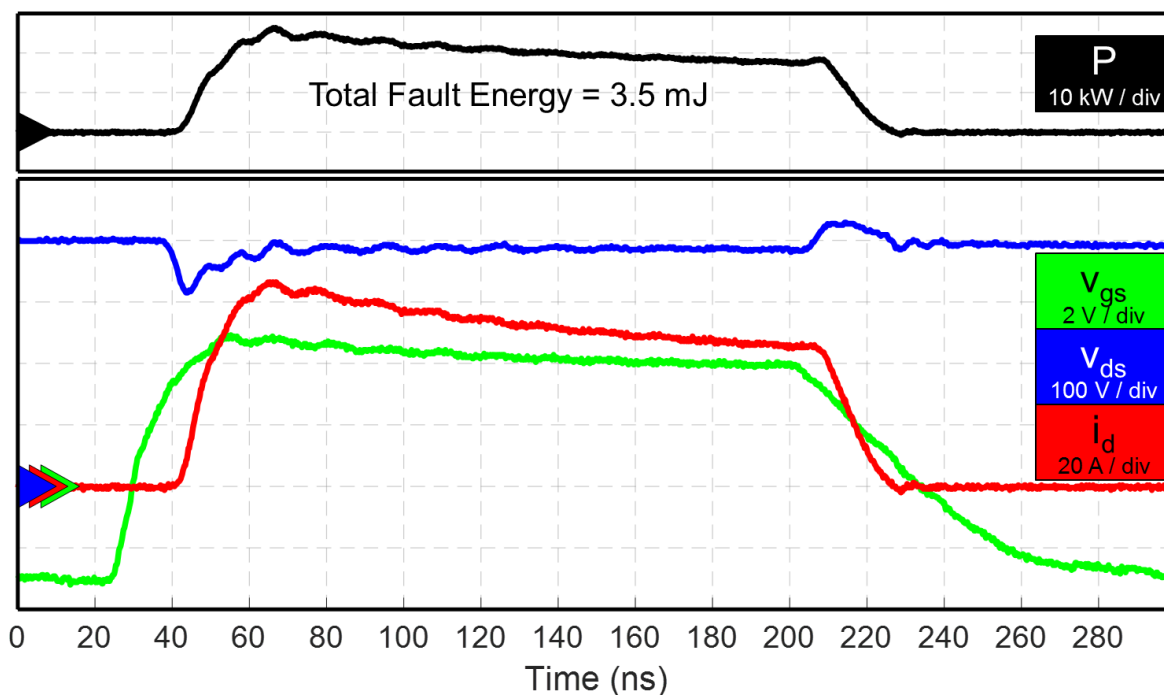


Figure B.40. Hard Switching Fault for Infineon GIT at 400 V, 125 °C

## **Vita**

Edward A. Jones was born in Richmond, Virginia, and attended the Virginia Polytechnic Institute and State University (Virginia Tech), where he graduated magna cum laude with an honors baccalaureate B.S.E.E. in 2007, with a concentration in Power Electronics and minors in Math and Religious Studies. As part of this degree, Edward wrote and defended an undergraduate thesis titled “Calorimetric measurement of efficiency for a boost-buck converter for automotive applications.” After graduating, he worked for General Electric as an electrical engineer for one year, then as a field application engineer for four years. During this time, his primary responsibility was the design, installation, and repair of measurement and monitoring systems for rotating equipment in the power industry and oil and gas industry, covering a territory that included the northeastern United States.

Since 2012, Edward has been working towards his Ph.D. in Electrical Engineering at the University of Tennessee, Knoxville. He has had three fellowships during his graduate career: the Chancellor’s Fellowship, the Bredesen Fellowship for Interdisciplinary Energy Research, and the CURENT Fellowship. At UTK, Edward’s research has focused on review and characterization of GaN devices, with the motivation to better understand the device behavior, and applying this understanding to improve gate driver design and optimization of GaN-based converters. He received the concurrent M.S.E.E. in Electrical Engineering from UTK in 2016.