

Review and Characterization of Gallium Nitride Power Devices

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Edward Andrew Jones
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Abstract

Gallium Nitride (GaN) power devices are an emerging technology that have only recently become available commercially. This new technology enables the design of converters at higher frequencies and efficiencies than those achievable with conventional Si devices. This thesis reviews the characteristics and commercial status of both vertical and lateral GaN power devices from the user perspective, providing the background necessary to understand the significance of these recent developments. Additionally, the challenges encountered in GaN-based converter design are considered, such as the consequences of faster switching on gate driver design and board layout. Other issues include the unique reverse conduction behavior, dynamic on-resistance, breakdown mechanisms, thermal design, device availability, and reliability qualification.

Static and dynamic characterization was then performed across the full current, voltage, and temperature range of this device to enable effective GaN-based converter design. Static testing was performed with a curve tracer and precision impedance analyzer. A double pulse test setup was constructed and used to measure switching loss and time at the fastest achievable switching speed, and the subsequent overvoltages due to the fast switching were characterized. The results were also analyzed to characterize the effects of cross-talk in the active and synchronous devices of a phase-leg topology with enhancement-mode GaN HFETs. Based on these results and analysis, an accurate loss model was developed for the device under test.

Based on analysis of these characterization results, a simplified model was developed to describe the overall switching behavior and some unique features of the device. The consequences of the Miller effect during the turn-on transient were studied to show that no Miller plateau occurs, but rather a decreased gate voltage slope, followed by a sharp drop. The significance of this distinction is derived and explained. GaN performance at elevated temperature was also studied, because turn-on time increases significantly with temperature, and turn-on losses increase as a

result. Based on this relationship, a temperature-dependent turn-on model and a linear scaling factor was proposed for estimating turn-on loss in e-mode GaN HFETs.

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Chapter 1

Introduction

1.1 Wide Bandgap Semiconductors

Wide bandgap (WBG) devices are an enabling technology for high-frequency, high-efficiency power electronics. WBG semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) provide advantages over conventional Silicon (Si) power devices, as shown in Figure 1.1 and Table 1.1. Some of these material properties are experimentally derived and vary between different reference sources, but there is a clear advantage in the properties of WBG semiconductors over Si. The higher breakdown field of a WBG semiconductor allows for devices to be optimized with thinner drift regions, resulting in power devices with lower specific on-resistance. This allows a smaller die size to achieve a given current capability, and therefore lower input and output capacitances. Higher saturation velocity and lower capacitances enable faster switching transients. In total, the material properties of WBG semiconductors result in a device with lower on-resistance and switching losses than a Si device with comparable voltage and current capabilities [1-4].

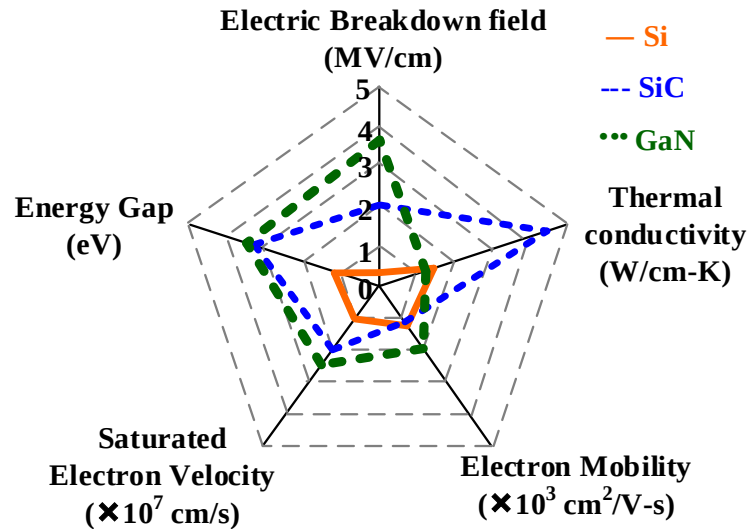


Figure 1.1 Comparison of Si, SiC, and GaN for power semiconductor applications [3],[4].

Table 1.1. Properties of wide bandgap semiconductors [3],[4].

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond	AlN
Bandgap, E_g (eV)	1.12	1.42	3.00	3.26	3.44	5.45	6.20
Electric breakdown field, E_c (MV/cm)	0.3	0.4	2.5	2.0	3.8	10.0	12.0
Electron mobility, μ_n (cm ² /V-s)	1500	8500	420 ^a 84 ^c	950 ^a 1190 ^c	1000 ^a 2000 ²	3800	300
Saturated electron drift velocity, v_s (x 10 ⁷ cm/s)	1.0	1.2	2.0	2.0	2.5	2.7	1.7
Dielectric constant, ϵ_r	11.8	13.1	9.7	10.0	9.5	5.5	8.5
Thermal conductivity, λ (W/cm-K)	1.5	0.46	4.9	4.9	1.3	22	2.85

^a Mobility along a-axis

^c Mobility along c-axis

² Mobility of 2DEG

SiC excels in high temperature applications, due to the thermal conductivity and overall device performance at elevated temperatures. However, the material characteristics of GaN make it a superior device in high-efficiency, high-frequency converters. The higher breakdown field enables a similarly rated GaN power device to typically outperform Si and SiC in terms of on-resistance, switching speed, or both, depending on the design of the device. Other WBG semiconductors such as GaAs, diamond, and AlN have also been heavily researched for power applications, but SiC and GaN have shown the most promise for near-term commercialization [1-4].

Figure 1.2 shows a timeline for the development of power semiconductor devices. In the 1950's, the thyristor or silicon controlled rectifier (SCR) was the only option for solid-state power electronics in the hundreds of volts. As the technology further developed, newer devices such as the JFET, power MOSFET, and IGBT were introduced with greatly improved performance and

higher voltage and current ratings. Now, in the 21st century, wide bandgap semiconductors are the latest in the trend toward higher-performance power electronics.

Commercialization of wide bandgap power devices began with the development of SiC diodes and JFETs. More recently, the 1200 V SiC MOSFETs and Schottky diodes have entered the market to compete with the 1200 V Si IGBT and Si diodes. SiC devices are available at lower voltages as well, including 600-900 V, but most of the SiC devices available today are rated at 1200 V. SiC MOSFETs are vertically diffused, with structures similar to the Si power MOSFET, including planar and trench MOSFETs. However, the doping, drift region width, and die size are very different [5],[6].

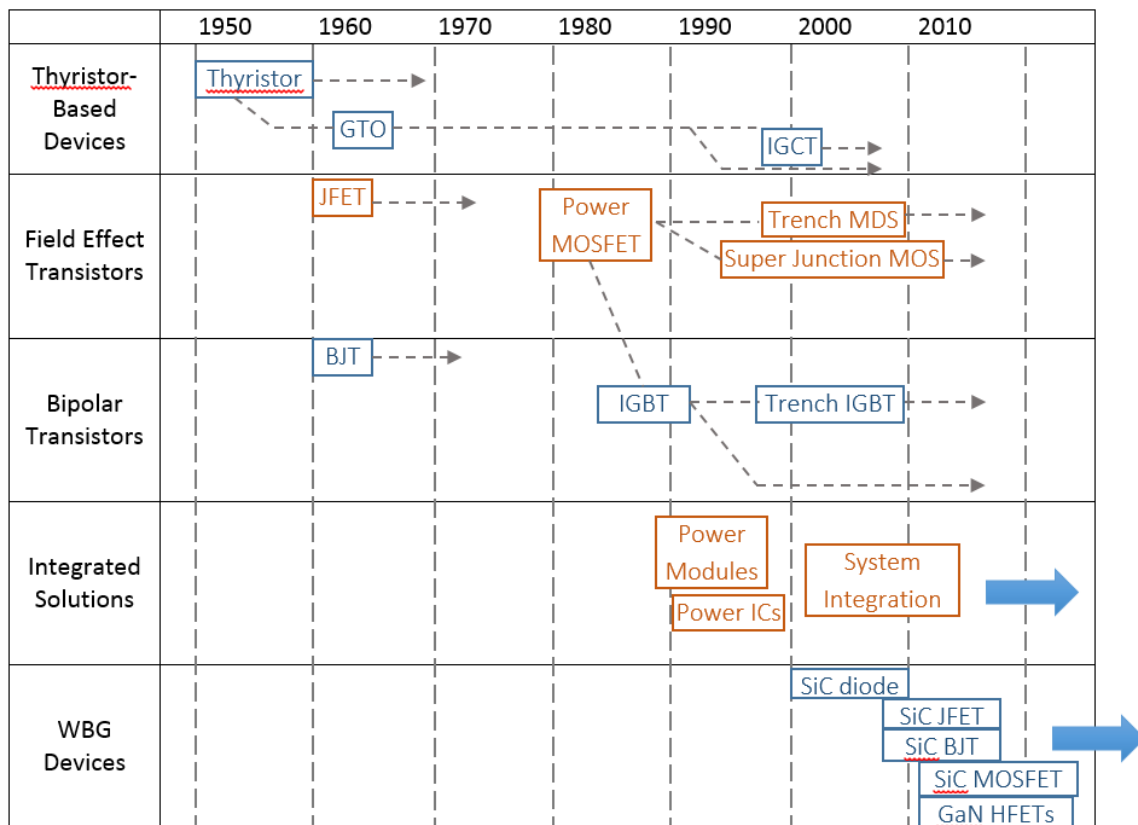


Figure 1.2. Timeline of the development of power semiconductor devices [7].

At the 600 V level, the Si Super Junction MOSFET has been the dominant technology for several years. This device structure uses deep trenches below the p-doped body regions to produce devices capable of blocking over 600 V, while maintaining a thin effective drift region to reduce the on-resistance and die size. This technique accomplishes the same goal of WBG devices using Si, however there are some undesirable drawbacks, such as a highly nonlinear output capacitance. The lateral GaN heterojunction field effect transistor (HFET), also called the high electron mobility transistor (HEMT), has recently presented another option for 600 V power devices.

The GaN HFET has been available at the 600 V level for only a few years, but EPC entered the market in 2009 with the first commercial GaN HFET rated at low voltage [8]. Today, at least ten companies have commercial or near-commercial GaN power devices, and this number continues to climb. The technology of GaN power devices is a primary thrust of this thesis, so more details will be covered in the next chapter.

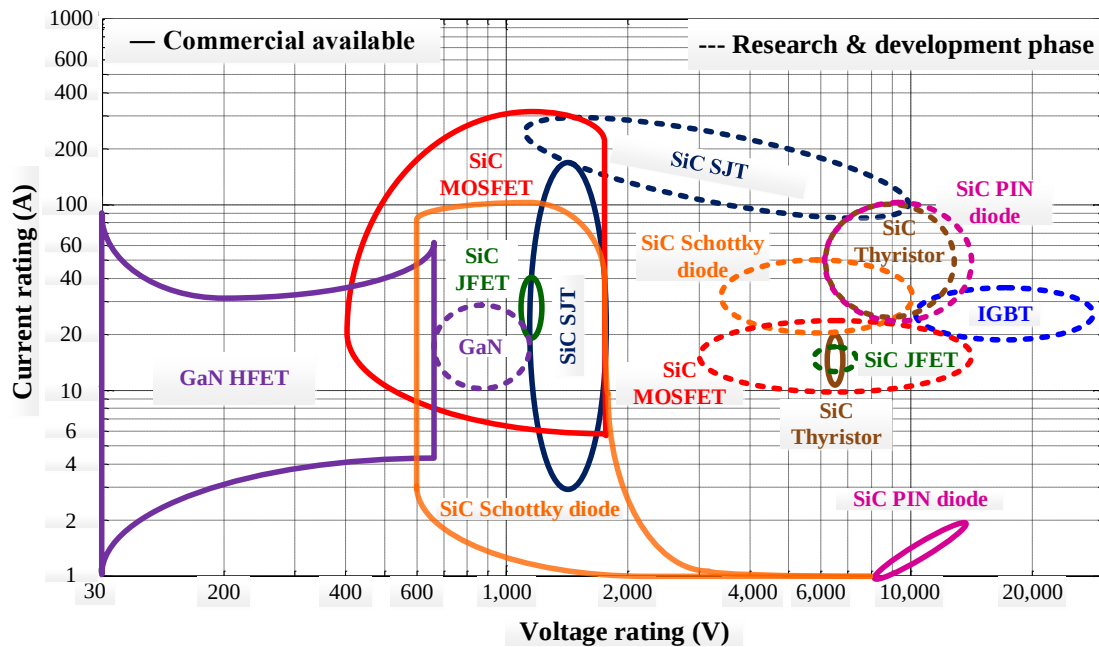


Figure 1.3. Ratings of selected WBG power devices [9].

Figure 1.3 shows the ratings of some commercially available and research phase WBG semiconductor devices. Lateral GaN devices have reached ratings up to 650 V and 90 A, while SiC MOSFETs occupy more of the high voltage and high power market segment. GaN and SiC together occupy a large area for both current and voltage, and WBG semiconductors can thereby enable efficient power electronics at power levels infeasible for conventional Si.

1.2 *Literature Review*

1.2.1 *Reviewing a Power Device*

The review of GaN power devices is a major goal of this paper, so it is helpful to first consider the elements of a typical review paper for power devices. Device reviews were popular in the 1980's and 1990's to update the power electronics community on the state of the art [10-16]. These papers particularly include summaries of power MOSFETs and IGBTs, as well as other types such as SCRs, BJTs, IGCTs, GTOs, and MCTs. More recently, similar reviews such as [17] discussed the new Super Junction devices available from several manufacturers. These reviews vary widely in both scope and perspective. In some, specific focus is given to the physical structures and fabrication steps of the devices, with an intended audience of device physicists and manufacturers. Another type of review is on the other end of the spectrum, covering power electronics at a very high level. These reviews describe the latest device types as black boxes, without much depth into the internal structure of each, then summarize the applications of these devices in various converter topologies based on their properties.

Some application notes such as [18],[19] follow a different review format, because they serve another specific purpose. These also serve as reviews, each for one device from a particular manufacturer, and they may cover the full spectrum from the material properties to application recommendations. For example, [19] provides a thorough introduction to Infineon's CoolMOS C7 Super Junction MOSFET, including the fabrication structure and recent improvements of that

particular device, properties of the device at a black-box level, and design concerns in a CoolMOS-based converter.

Since the advent of wide bandgap power electronics, device reviews have seen a second wave of popularity, covering materials such as SiC, GaN, and perhaps to a lesser extent diamond and GaAs. These fit into a similar spectrum to the reviews mentioned earlier, from material properties to device applications [1],[3],[4],[20-22].

Even more specifically, there have been a number of reviews focusing on GaN power devices, which informs Chapter 2 of this thesis. Some of these cover a range of GaN technologies for specific applications, such as electric vehicles [23],[24]. Others focus on one particular GaN technology by a single manufacturer [25-27]. Lastly, some GaN reviews describe the benefits and concerns of GaN devices in a particular circuit topology, such as resonant LLC or totem-pole PFC [28-30]. However, none of these reviews provide all of the necessary tools for a power designer's first GaN-based converter, so several of them must be read to cover the different aspects.

From surveying these previous review papers on GaN and other power devices, it is clear that a user-focused review of GaN HFETs should discuss the following topics:

- The material properties of GaN, as compared with the Si and SiC, and the advantages of these materials for power devices.
- The structures, behavior, and fabrication challenges of vertical devices, as well as a survey of commercial vertical GaN manufacturers.
- The structures and behavior of lateral devices, including a survey of the distinct device types used by commercial lateral GaN manufacturers, and the unique properties of lateral GaN such as diode-like reverse conduction behavior, dynamic R_{ds-on} , and breakdown mechanisms.
- Gate driver considerations for GaN power devices, such as the voltage and current capabilities, common mode transient immunity, and cross-talk mitigation.

- Converter-level considerations for GaN power devices, such as the reliability of the devices, thermal design, device packaging, PCB layout, large-scale device availability, and the overall switching behavior of the GaN devices as compared with conventional Si power devices.

1.2.2 *Device Characterization and Modeling*

Characterization and modeling of power devices is often an integral component of graduate theses, such as in [9],[31-37]. Often this characterization is performed for the purpose of developing or improving a model, or for optimizing the design of a particular converter topology. However, methodology for static and dynamic characterization of Si and SiC devices has been well-covered in these prior works. In particular, [35] details the test setup and measurements for a double pulse test, then [9] provides a thorough update of this methodology for SiC devices, and [34] performs a similar update for cascode GaN devices. Outside of theses, several works have provided methodology for characterization and modeling of GaN devices in particular [38-46]. These prior works do not provide characterization results of 600-V enhancement-mode insulated-gate GaN power devices, although the methodology is similar to what has been presented for other wide bandgap devices such as SiC and cascode GaN.

From these references, several key issues are critical for characterization of enhancement-mode GaN devices at the 600 V level:

- Static measurement with a curve tracer and impedance analyzer, including consideration of elevated temperature.
- Bandwidth and ground-lead inductance of voltage measurement probes.
- Bandwidth and accuracy of current measurement, particularly by means of coaxial current shunts.
- Reduction of common-mode ringing using chokes on all dc power supplies and measurement channels.

- Proper I-V alignment through deskew of the current measurement channel.

1.3 *Motivations and Objectives*

The primary motivation for this work is to provide a thorough user-focused description of GaN power devices for an audience of application-focused power designers. Rather than discussing only device physics or converter design principles, this thesis aims to bridge the gap between the two, providing the background necessary for a power electronics engineer to begin a project in GaN-based converter design.

The first step in achieving this goal is to review the latest publications from vertical and lateral GaN device manufacturers, covering the fundamental properties and commercial status of these devices. The second step is to review the unique characteristics and subsequent converter design challenges for GaN. Because the availability of commercial GaN devices is rapidly changing, this review will cover technology that is currently available and also recent developments that are targeted for near-term commercialization. Therefore, the material presented may be used to understand the uniqueness of commercial GaN devices available now, as well as provide the tools to identify and understand newer GaN technology as it continues to develop.

Once the fundamental technology is well-understood, the specific characteristics of one currently commercial enhancement-mode GaN power device will be presented and analyzed. The methodology used to perform the characterization will also be covered, so that similar data can be collected for other devices. Using the characterization results, a simplified model will be developed for the enhancement-mode GaN HFET, including equations governing the general switching behavior during turn-on and turn-off transients, as well as some unique properties of this device. Although this simplified model is not intended for simulation, the equations can be used to better understand and interpret experimental results. The model is aimed at understanding and explaining

some of the trends and properties that were discovered during the characterization process, and are not explained by the conventional model of a MOSFET.

1.4 Thesis Organization

This thesis is organized as follows. Chapter 2 reviews GaN power devices, including the basic structure and properties of vertical and lateral devices. The commercial status and design challenges associated with GaN power devices is also discussed. Chapter 3 discusses the methodology and test setup of GaN device characterization, as well as the results and analysis for a commercial enhancement-mode lateral GaN HFET. Chapter 4 then continues that analysis and develops a simplified model for the enhancement-mode GaN device that was characterized, including the general switching behavior, Miller effect, and the impact of elevated temperature on the turn-on transient. Finally, Chapter 5 summarizes the contributions presented and plans for future work.

Chapter 2

Review of GaN Power Devices

2.1 *Introduction*

Before designing power electronics with GaN power devices, it is useful to understand their characteristics and the challenges that typically accompany such a project. Several review and survey papers have been published on the relative characteristics of WBG devices, including the benefits and design challenges associated with each [4],[21],[47],[48]. Other reviews, such as [23],[25],[49-51], have provided useful background on GaN power devices and GaN-based converter design. Some of these reviews focus on one particular GaN technology or research direction, rather than covering the full range of commercial devices available today. In addition, the significant developments in the past few years require an update to these prior works. Therefore, this review aims to cover the aspects of GaN power devices that are relevant to the converter designer, as the landscape of commercially available devices continues to change. This includes explanation of device physics properties to an audience who may not have device physics backgrounds, as well as exploring converter design elements that are not commonly required for Si-based power electronics.

2.2 *Vertical GaN Devices*

Vertical GaN devices, using structures similar to their Si and SiC counterparts, can take greatest advantage of the superior GaN material properties. However, the lack of availability of high-quality, low-cost GaN wafers has limited these prospects. This section will review the recent progress in the commercialization of vertical GaN devices.

2.2.1 *GaN-on-GaN Power Devices*

Avogy and HRL have publicly disclosed efforts to develop and commercialize vertical devices through the Strategies for Wide Bandgap, Inexpensive Transistors for Controlling High-

Efficiency Systems (SWITCHES) program, funded by ARPA-E [52]. HRL has yet to announce any new vertical devices from this research, but Avogy has published some of its recent progress.

The first vertical structures published by Avogy were diodes, including the Schottky diodes and p-n diodes shown in Figure 2.2. Schottky diodes have been developed with blocking voltage up to 600 V, as well as p-n diodes up to 1700 V [53]. P-n junction diodes have also been fabricated with relatively large die areas, up to 16 mm², able to block 700 V and handle pulsed currents up to 400 A [54]. Samples have been announced on the Avogy website for 600, 1200, and 1700 V diodes with rated average current up to 5 A, in TO-220 packages [55].

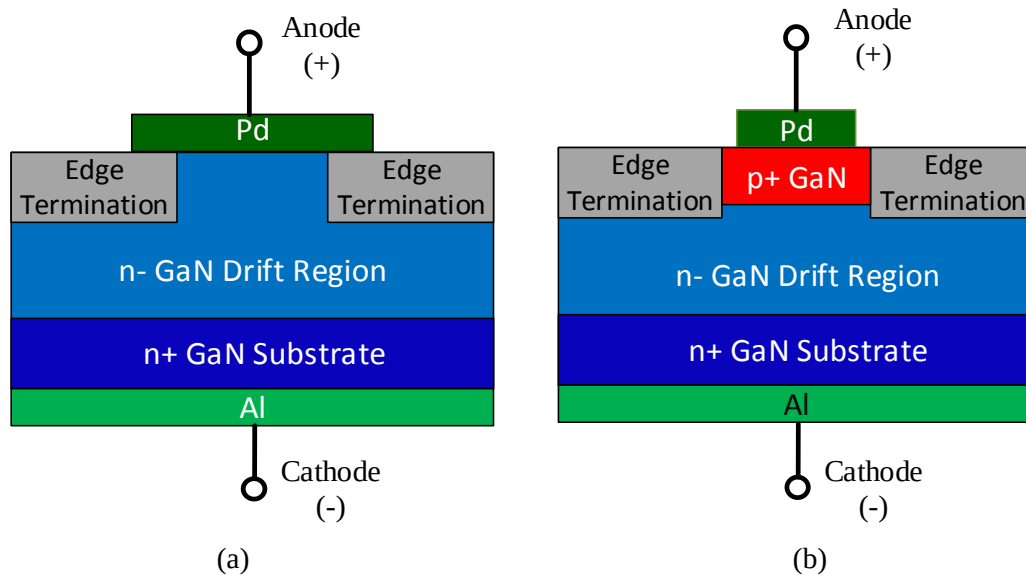


Figure 2.1. Vertical GaN-on-GaN diodes, including (a) Schottky and (b) p-n junctions [53].

Avogy has also developed a vertical GaN FET with 1.5 kV blocking capability and 2.3 A saturation current. The device, shown in Figure 2.2, is a combination of the conventional JFET structure and the heterojunction AlGaIn/GaN structure used in lateral devices. With a threshold

voltage of 0.5 V, this device is enhancement-mode and therefore normally-off [56]. Neither the diodes nor the FETs are commercially available at this time.

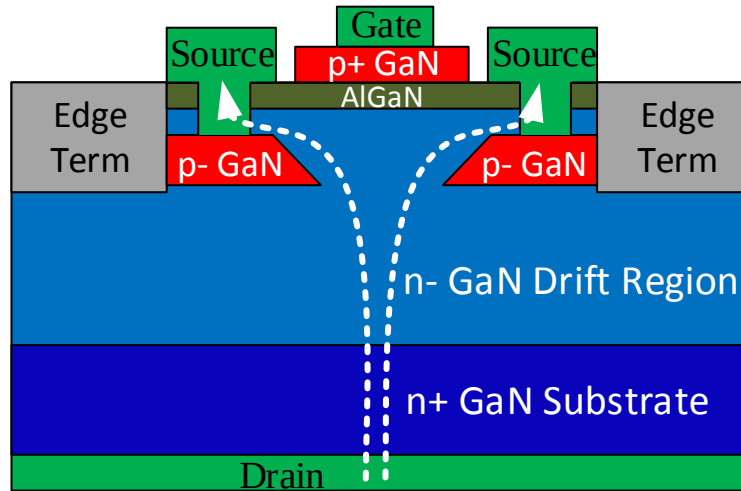


Figure 2.2. Vertical GaN-on-GaN normally-off JFET [56].

2.2.2 GaN-on-Si Vertical Power Devices

Vertical devices generally require homoepitaxial fabrication, meaning that the substrate and epitaxial layers are fabricated with the same type of semiconductor (i.e. GaN-on-GaN). However, MIT has developed a method of vertical MOSFET and diode fabrication using a heteroepitaxial GaN-on-Si structure, by etching through the Si substrate on the bottom side of the device to expose the GaN drift region [57]. Cambridge Electronics, Inc (CEI) has recently begun commercializing some of the GaN technology developed by MIT. Samples of CEI's GaN FETs have been announced at voltage ratings of 200 V and 650 V, with on-resistances of 550 m Ω and 290 m Ω [58].

Although the exact structure of the CEI devices has not been published, this device may utilize one of the patented vertical structures from [57] shown in Figure 2.3. In order to achieve a

fully vertical current path, the drain contact is metallized in a recess that is etched completely through the substrate and buffer layers, so that it directly contacts the bottom side of the GaN epitaxial layer [57]. This technique combines the performance benefits of vertical GaN MOSFETs with the lower cost of Si wafers. With the current challenges to produce GaN wafers at costs competitive with Si or SiC, this presents an interesting alternative to vertical GaN-on-GaN devices.

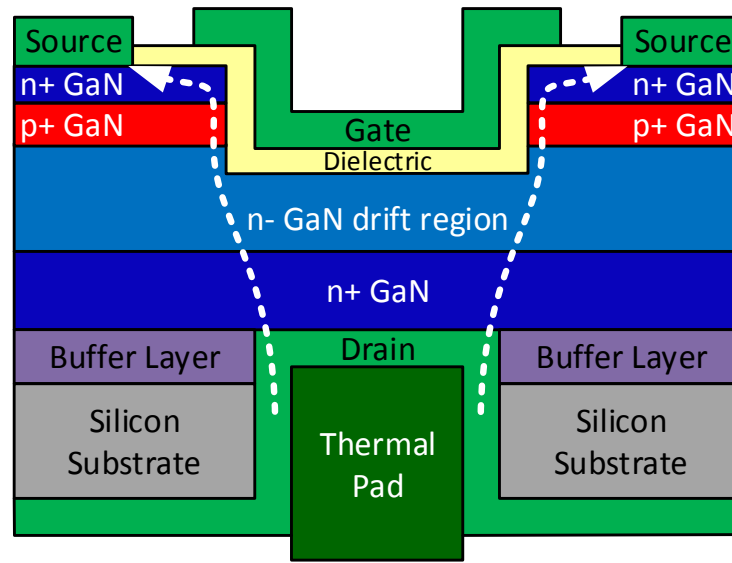


Figure 2.3. Vertical GaN-on-Si MISFET [57].

2.2.3 GaN Wafer Fabrication

Although wafer fabrication itself is not relevant in the converter design process, affordable GaN wafers are an important step toward commercialization of vertical GaN devices. These wafers form the substrate of a GaN-on-GaN device, on which the drift region is epitaxially deposited. As opposed to the melt-growth method used to produce Si wafers, GaN wafers are typically produced using hybrid vapor-phase epitaxy (HVPE) or chemical vapor deposition (CVD) on a foreign material such as sapphire. The foreign material is then removed, leaving only the GaN layer of the

wafer. This process is sometimes referred to as “pseudo-bulk” wafer fabrication, and presents many challenges due to the lattice mismatch between GaN and the foreign material [59].

Other technologies are currently being researched to fabricate true bulk GaN wafers, without the need for foreign substrates. The three most promising technologies are high nitrogen pressure solution growth (HNPSG), low pressure solution growth with sodium flux (Na-flux), and ammonothermal growth. HNPSG and Na-flux methods have been used to produce GaN on foreign substrates with several inches in diameter, and more limited success in producing true bulk GaN. Ammonothermal growth has been the most successful in production of bulk GaN, with over 2 inches in diameter fabricated in boule form. Each of these methods has its own challenges, as shown in Table 2.1.

Table 2.1. Comparison of GaN Wafer Fabrication Methods [59].

Fabrication Method	Approximate Growth Rates		Largest Crystal Size		Defect Density	Challenges
	$\mu\text{m/hr}$	mm/day	On Substrate	Boule	cm^{-2}	
HVPE	100	2.4	> 6 inch	--	105-106	Stresses, wafer curvature, growth front breakdown, growth direction
HNPSG	3	0.07	2 inch	Few mm	101-102	Scaling, growth rates, purity
Na-Flux	30	0.7	4 inch	Few mm	102-105	Scaling, sustained growth rates
Ammono-thermal	4	0.1	--	> 2 inch	104	Growth rates, purity

Figure 2.4 shows the relative cost and growth rates of GaN wafers from vapor and ammonothermal methods based on current predictions, as compared to Si wafers produced with seeded melt-growth and SiC wafers produced with seeded sublimation. The ammonothermal method has the potential to drastically reduce the cost of GaN wafer fabrication at the production

scale, but the current cost for small-scale ammonothermal GaN growth cannot compete with more established hybrid vapor phase epitaxy [59].

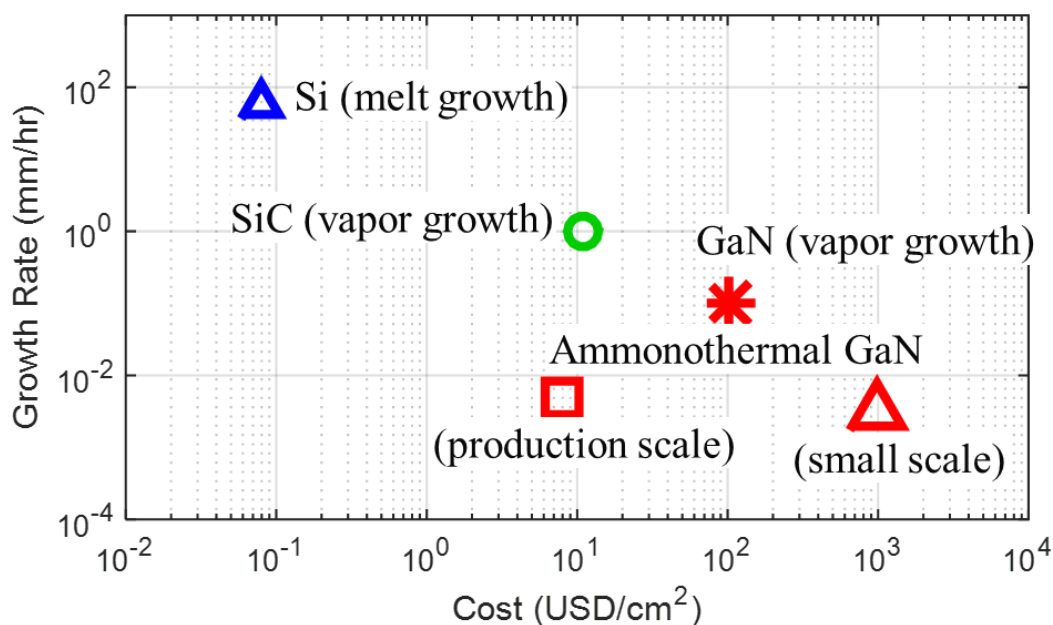


Figure 2.4. Cost and growth rate comparison of wafers with different growth techniques [59].

2.3 The Lateral GaN HFET

Because vertical GaN devices have not yet been produced on a commercial level, most of the GaN devices available today are lateral heterojunction field-effect transistors (HFETs), also known as high electron mobility transistors (HEMTs). These devices are typically rated at 600-650 V, although higher voltage devices have been announced by manufacturers. Because of the lateral heterojunction structure, these devices are fundamentally different from MOSFETs and have unique characteristics.

2.3.1 Basic Device Structure

Figure 2.5 shows the basic structure of the GaN HFET. The principle feature of this structure is the AlGaN/GaN heterojunction. At the interface between these two layers, a layer of high-mobility electrons called “two-dimensional electron gas” (2DEG) forms as a result of the crystal polarity, and is also augmented by piezoelectric crystal strain due to the lattice mismatch between AlGaN and GaN. The 2DEG forms a native channel between the source and drain of the device.

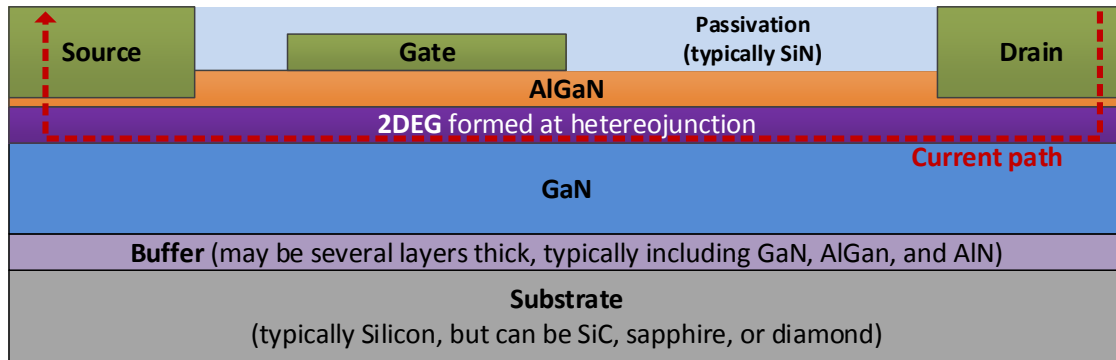


Figure 2.5. Basic structure of depletion-mode lateral GaN HFET (not drawn to scale) [49].

The substrate is typically Si, but other materials such as SiC, sapphire, and diamond can be used. In order to deposit the GaN layer on the substrate, a buffer layer must be deposited that provides strain relief between the GaN and the foreign material. This buffer often includes several thin layers of GaN, AlGaN, and AlN [49].

Because of the native 2DEG channel, the HFET is inherently a depletion-mode (normally-on) device. This is not desirable for voltage-source converters, because of the potential for shoot-through during startup or loss of control power. Several methods have therefore been used to fabricate normally-off GaN HFETs [49].

2.3.2 Cascode HFETs

A normally-off GaN device can be made with a depletion-mode HFET, using the cascode structure shown in Figure 2.6. A cascode device requires co-packaging of the depletion-mode HFET with a low-voltage enhancement-mode MOSFET. The two dies are connected in such a way that the output (drain-source) voltage of the MOSFET determines the input (gate-source) voltage of the HFET. Both devices share the same channel current while on, and the blocking voltage is distributed between them while off.

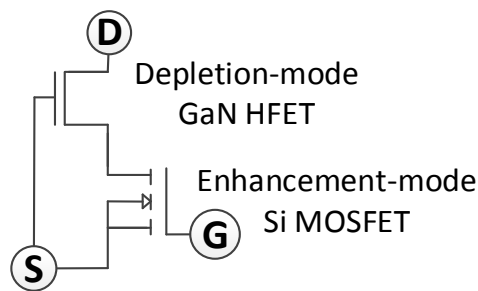


Figure 2.6. Device structure for the normally-off GaN cascode.

The two dies are connected inside the package with wire bonds or in a planar architecture. The switching performance of the cascode device relies heavily on the parasitic inductances in the package, especially between the two dies, and also on how well the junction capacitances of the two are matched. If the inductances are too high, or the capacitances are not matched well, the switching losses can increase significantly.

Table 2.2 shows the commercial status of cascode GaN devices. Transphorm is the only vendor currently selling cascodes on a large scale, although International Rectifier and MicroGaN have produced engineering samples. All three are rated at 600 V and use GaN-on-Si HFETs. MicroGaN has also produced a version of their cascode that acts as a diode rather than an active FET [26],[60-65].

RFMD was selling engineering samples of their 650 V GaN-on-SiC device in 2014, but has since discontinued this product line. The use of a SiC substrate allows for improved performance over GaN-on-Si cascodes, but this is not as common as GaN-on-Si due to the higher cost of SiC wafers.

Texas Instruments and VisiC were also included in Table 2.2, but it is important to note that they do not use the cascode circuit described in Figure 2.6. However, these devices utilize the same concept, where a depletion-mode GaN HFET is connected in series with other electronics inside the package to create a normally-off device. The key difference between these devices and a conventional cascode is that the gate driver for VisiC and TI connects directly to the gate terminal of the GaN HFET, but not directly to the source terminal, whereas a cascode allows connection to the GaN gate but not its source. In either case, the gate-source voltage is controlled by additional electronics inside the package. The VisiC device can be driven by a conventional MOSFET gate driver, and the TI device includes an integrated gate driver inside the device package [66-68].

Table 2.2. Commercial Cascode Devices

Manufacturer	Voltage Rating (V)	Current Rating (A)	R_{ds-on} (mΩ)	Q_g (nC)	Package	Availability
Transphorm [60]	600	9	290	6.2	PQFN/ TO-220	Online ordering
		17	150	6.2		
		34	52	19	TO-247	
International Rectifier / Infineon [26]	600	10	125	--	PQFN	Discontinued
MicroGaN [62]	600	--	320	--	TO-263	Samples
RFMD/Qorvo [63],[64]	650	25	85	16.2	PQFN	Discontinued
		30	45	15.7	TO-247	
Fujitsu [65]	500	--	100	14	TO-220	Unknown
Texas Instruments [66]	600	--	70	--	PQFN	Unknown
VisiC [67],[68]	650	50	15	35	PQFN	Samples

2.3.3 Enhancement-Mode HFETs

Although the 2DEG makes the lateral HFET natively depletion-mode, the gate can be modified to shift the threshold voltage positively and thereby make an enhancement-mode device. Several companies have produced e-mode GaN devices, and Table 2.3 lists a selection of these as well as their commercial availability at this time.

Most of these companies have published papers that show their device structure, and explain how their devices achieve a positive threshold voltage. Figure 2.8 shows some of these published techniques, which are used to deplete the 2DEG carriers beneath the gate when no voltage is applied. A positive voltage above the threshold is then required to enhance this depleted 2DEG beneath the gate and complete the channel.

Table 2.3. Commercial Enhancement-Mode Devices

Manufacturer	Voltage Rating (V)	Current Rating (A)	R_{ds-on} (m Ω)	Q_g (nC)	Package	Availability
EPC [69]	30	60	1.3	20	Near-chip scale, LGA	Online ordering
	40		1.5	19		
	60		2.2	16		
	80		2.5	15		
	100		3.2	13		
	200	9	43	1.8		
GaN Systems [70]	650	7	220	1.5	Near-chip scale	Online ordering
		15	110	3.0		
		22	73	4.6		
		30	55	5.8		
		60	27	12		
	100	90	7.4	12		
		45	15	6.6		
Panasonic [27],[71-73]	600	15	65	11	TO-220, DFN	Samples
		10	155	6	DFN	Online ordering
HRL [74],[75]	1200	10	500	--	--	Licensed to Navitas
	600	10	350	--	--	
Exagan [76]	600	100	--	--	--	Unknown
	1200	100	--	--	--	
Powdec [77]	1200	16	--	--	--	Unknown

EPC uses a p-doped layer of GaN beneath the gate as shown in Figure 2.7 (a), which creates a diode-like characteristic on the gate that shifts the threshold up by the magnitude of the diode voltage drop [25]. Panasonic also uses a p-doped layer of GaN in their latest x-GaN Gate Injection Transistors (GITs), although an earlier version of the GIT used p-doped AlGaN rather than GaN as shown in Figure 2.7 (b) [27],[71],[72],[78]. One key difference between these two methods is the forward voltage drop on the gate before steady-state gate current begins to flow, which may be due to the etching depth beneath the p-doped GaN layer. The EPC diode knee occurs at ~ 5 V, whereas the Panasonic diode knee occurs at ~ 3 V. The EPC device is typically driven with 4.5-5 V, just below the knee when diode current begins to increase. The Panasonic GIT is typically driven above the knee where several mA of steady-state current flows into the gate. This intentional injection of minority carriers enhances the conductivity of the 2DEG and reduces on-resistance, but it also increases the complexity of gate drive design [27],[69],[71],[72].

HRL first used plasma treatment to deposit fluorine ions beneath the gate as shown in Figure 2.7 (c), effectively depleting the 2DEG until it is re-enhanced by a positive gate voltage [74]. However, HRL's latest devices replace the plasma treatment with a recessed gate as shown in Figure 2.7 (e) [75]. This technique involves etching away the AlGaN beneath the gate to a precise depth, then replacing it with an insulating material. HRL chose AlN as the gate insulating layer. In 2015, HRL licensed its lateral GaN technology to Navitas Semiconductor [79].

Recessed gates are used by several other manufacturers as well, including Exagan and NEC, usually in conjunction with other modifications to further increase the threshold voltage [76],[80]. Sanken has developed devices using a non-insulated recessed gate as shown in Figure 2.7 (d) [81],[82]. However, Sanken has not published whether this technique is used in the device it is currently sampling.

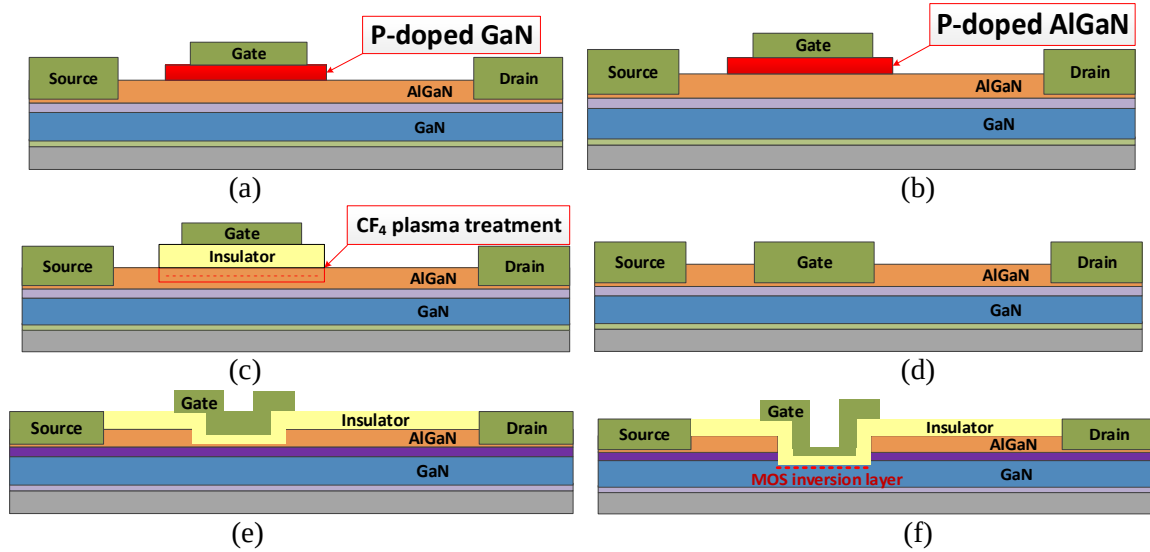


Figure 2.7. Gate modification techniques for enhancement-mode GaN HFETs, (a) P-doped GaN, (b) P-doped AlGaN, (c) Plasma treatment, (d) Recessed gate, (e) Insulated recessed gate, (f) Hybrid MIS-HFET [23],[25],[67],[71],[74-77],[83].

Figure 2.7 (f) depicts another option for enhancement-mode devices, a hybrid MIS-HFET. This structure requires etching past the AlGaN layer, and permanently removing the 2DEG beneath the gate. The 2DEG remains on the drain-side and source-side of the channel, but the two sides must be connected by a MISFET inversion layer beneath the gate in order to turn on the device [23].

Powdec has published an enhancement-mode structure that is similar to a cascode, but the lower-voltage device is fabricated on the top surface of the GaN device next to the HFET gate [77]. GaN Systems has not published its gate structure, but the GaN Systems devices appear to have an insulated gate as in Figure 2.7 (c), (e) or (f) [84].

2.3.4 Reverse Conduction Behavior

A MOSFET's body diode provides a path for reverse conduction through the p-n-doping of the body and drift regions. The GaN HFET does not have a body region or doping in the drift

region, so there is no body diode. However, there are reverse conduction mechanisms in both cascode and e-mode GaN devices.

In a cascode device, the body diode of the low-voltage Si MOSFET will turn on when the cascode is reverse biased. The Si body diode will then turn on the channel of the GaN HFET. In this way, the cascode approximates the behavior of a body diode. The reverse recovery charge of the low-voltage MOSFET is much less than that of a power MOSFET, so the additional switching losses due to reverse recovery are relatively low.

An enhancement-mode HFET has no body diode at all, but it demonstrates a mechanism that may be called “self-commutated reverse conduction” (SCRC) or “diode-like behavior.” The key to this mechanism is the symmetry of the device. The channel will turn on when the gate-source voltage V_{gs} exceeds its threshold, $V_{gs,th}$, and it will similarly turn on when the gate-drain voltage V_{gd} exceeds its own threshold voltage, $V_{gd,th}$. If the output of the device is reverse biased, the gate-drain voltage will be

$$V_{gd} = V_{gs} - V_{ds} . \quad (1)$$

When the gate-drain voltage exceeds the threshold voltage $V_{gd,th}$, which is typically approximately the same as the specified $V_{gs,th}$, the e-mode device channel will turn on and allow reverse current to flow. The voltage drop in the SCRC mode will then be

$$V_{sd} = V_{gd,th} - V_{gs} + I_d R_{sd,rev} \quad (2)$$

where $R_{sd,rev}$ is the effective channel resistance during SCRC. $R_{sd,rev}$ is typically higher than $R_{ds,on}$ and varies with T_j , V_{gs} , and I_d . When $V_{gs} < V_{gs,th}$, reverse current forces the device into saturation, but only just past the knee between ohmic and saturation regions. A more negative V_{gs} drives the device even further into saturation, and $R_{sd,on}$ becomes more dominated by the reverse transconductance rather than the ohmic on-resistance. Therefore, negative off-state driving voltage is generally undesirable for e-mode GaN devices, because the SCRC voltage drop and resistance

will increase. Figure 2.8 shows a typical characteristic for e-mode device, including the SCRC behavior with 0 V and -2 V applied to V_{gs} [49].

Compared to the voltage drop on a MOSFET body diode, the total SCRC V_{sd} is often quite high (3-5 V). E-mode GaN conduction losses may become excessive during long dead times. However, this “diode-like behavior” does not actually contain a diode, so there are no reverse recovery losses during switching. The lack of reverse recovery also reduces the dead time required to ensure ZVS switching, which is especially useful in soft switching applications [28].

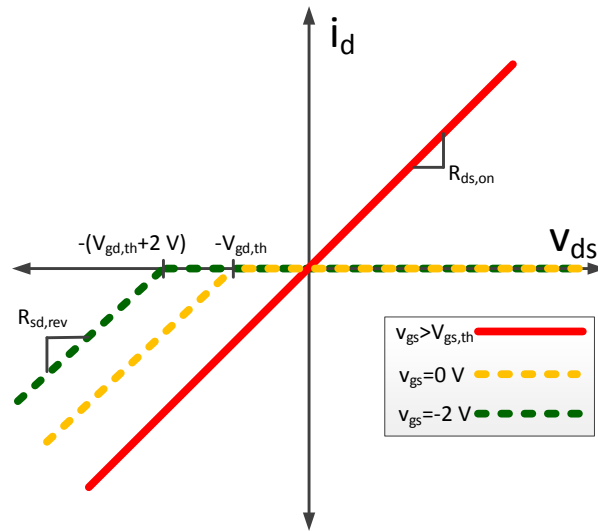


Figure 2.8. Reverse conduction characteristic of an e-mode GaN HFET.

Another option for either cascode or e-mode devices is to pair the HFET with an antiparallel Schottky diode, as is common with IGBTs. This will increase the output capacitance of the device, and therefore increase switching loss, but it may be a practical solution for some applications. In such a case, it is beneficial to package the diode with the HFET to minimize parasitics and reduce overall size [85].

2.3.5 Dynamic $R_{ds,on}$

Current collapse has been a widely reported phenomenon for lateral GaN devices, causing a temporary increase in on-resistance that is proportional to blocking voltage. This dynamic $R_{ds,on}$ occurs primarily through two mechanisms, demonstrated in Figure 2.9. The first is trapping of surface charges near the drain-edge of the gate terminal when the device is in its off-state. The lateral structure causes the gate-drain electric field to be strongest near the edge, and impurities in the surface passivation and interface trap these charges temporarily. During the following on-state, these trapped charges act as a “virtual gate,” weakening the 2DEG until they are released. The second mechanism is the injection of “hot electrons” into even deeper traps within the device, particularly in traps caused by carbon doping in the buffer layer. These trapped charges also weaken the 2DEG and increase $R_{ds,on}$, and may also cause long-term degradation to the device. Both of these effects are proportional to blocking voltage, and the hot electron effect has also been shown to increase with higher switching energy loss [86-88].

Measurement and characterization of dynamic $R_{ds,on}$ is challenging, because it requires accurate measurement of V_{ds} in the 0.1-V scale immediately after falling from several hundreds of volts. This can be accomplished by clamping the measurement node at a low voltage during the off-state, using a diode-based or active clamping circuit, then unclamping the measurement node voltage after turn-on. However, this clamping action causes ringing in the measurement that may require several hundred nanoseconds to dampen. Because dynamic $R_{ds,on}$ is a very time-dependent phenomenon, it is important to capture this measurement as early as possible. A comprehensive study of dynamic $R_{ds,on}$ over several operating conditions was performed in [89] using this clamping technique. Temperature, load current, and bus voltage are all significant factors. Also, switching frequency and duty cycle have a major effect on the overall increase in dynamic $R_{ds,on}$ during a

switching period. Therefore, additional conduction losses due to this phenomenon could be easily misdiagnosed as switching loss.

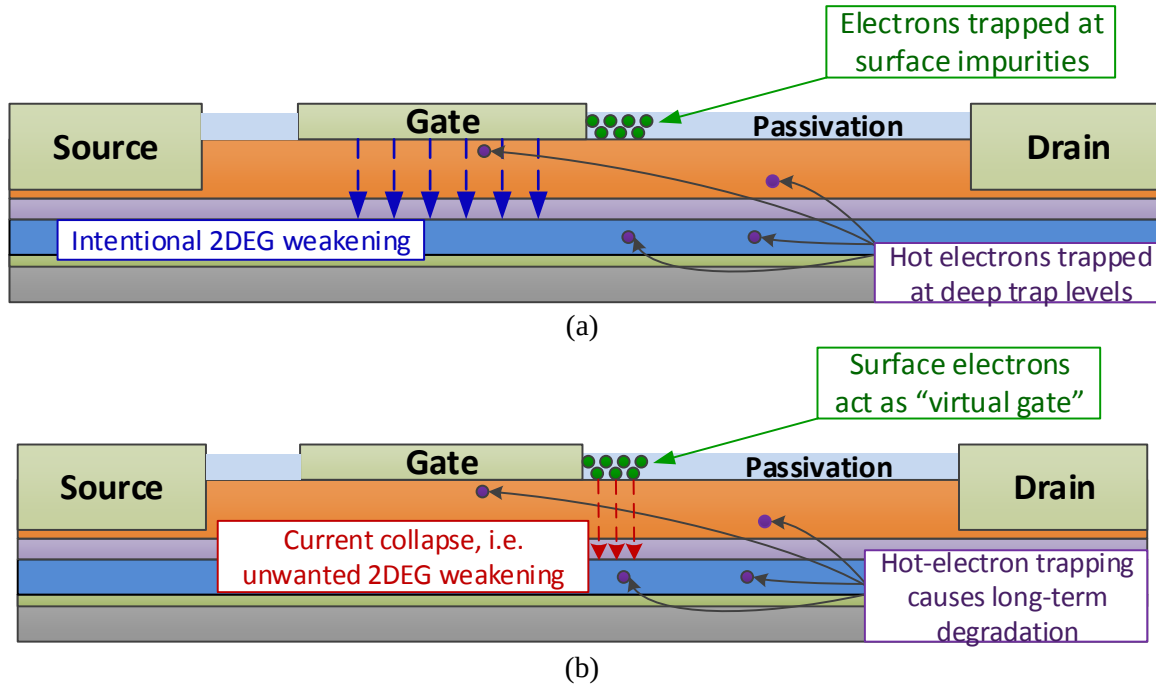


Figure 2.9. Mechanisms causing dynamic $R_{ds,on}$ in lateral GaN HFETs: (a) Trapping of charges when blocking voltage in off-state, (b) Consequences of trapped charges during following on-state.

GaN device manufacturers have made much progress in mitigating current collapse, primarily through the use of field plates. Each manufacturer may use a different structure and combination of field plates. Source and gate field plates help to redistribute the gate-drain electric field away from the gate edge. An example of basic field-plate structure is shown in Figure 2.10. The Si substrate can also act as a bottom field plate if it is connected to the source. Some manufacturers internally connect the substrate and source of their GaN HFETs, while others choose to electrically isolate the Si substrate to prevent current from flowing through it. If a separate thermal pad is provided in the device package, the manufacturer may recommend that the substrate be externally source-connected to help mitigate current collapse [90],[91]. Panasonic's x-GaN GIT

uniquely adds a second p-doped drain contact next to the ohmic drain to counteract dynamic $R_{ds,on}$ [78].

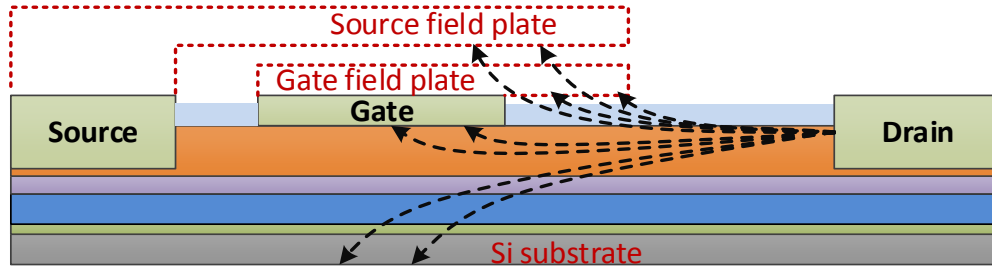


Figure 2.10. Field plates reshaping the gate-drain electric field to mitigate current collapse.

2.3.6 Breakdown Mechanisms

Design of voltage-source converters often rely on the MOSFET's ability to survive a limited exposure to voltages over the device rating, according to the specified avalanche energy rating. However, lateral GaN HFETs do not have the potential for avalanche breakdown, because they do not rely on a p-n junction for voltage blocking. Vertical GaN MOSFETs have avalanche capabilities, but lateral HFETs experience catastrophic dielectric breakdown when exposed to sufficient overvoltage [92]. This breakdown is destructive and non-recoverable. For this reason, GaN devices are typically rated much lower than the actual breakdown voltage. The dielectric may be designed at twice the rating to prevent lateral breakdown along surface states. While source-connecting the substrate is beneficial for current collapse mitigation, this also provides a vertical path for leakage current to flow, which is a second breakdown mechanism for some devices [93].

The gate in lateral HFETs is also susceptible to rupture. This failure mechanism may present as a gradual increase in steady-state current until the gate dielectric or Schottky junction completely breaks down [94]. Steady-state gate current is expected during normal operation for e-mode HFETs with p-doped gate caps. However, this has also been observed for insulated gate

devices when exposed to excessive voltage and elevated temperatures, even when both of these conditions are within the ratings of the device [84]. For this reason, it is useful to periodically check the health of devices under test by measuring steady-state gate current, with a simple test setup using a dc power supply and current meter.

2.4 Reliability Qualification

Power transistors such as MOSFETs and IGBTs are typically tested according to published JEDEC standards, and thereby qualified for particular reliability specifications. Testing for Si MOSFETS generally includes high-temperature reverse bias (HTRB), high temperature gate bias (HTGB), high temperature storage (HTS), temperature cycling (TC), high temperature high humidity reverse bias (H3TRB), unbiased autoclave (AC), moisture sensitivity level (MSL), and electrostatic discharge (ESD) testing. Reliability data based on these tests have been published for EPC and Transphorm devices [95-97].

However, because these JEDEC standards were written for Si MOSFETs, different reliability qualification standards may be required for GaN HFETs. One of the main challenges for new devices is the accelerated lifetime testing. Conventional Si devices are tested for accelerated lifetime based on well-established models and years of experience. GaN devices may not respond the same way in the same test conditions, and there have not been as many years with practical field reliability experience to back up the accelerated lifetime models [98]. A path to developing new standards specifically designed for GaN devices has been proposed by [99-101]. The unique breakdown mechanisms discussed in the previous section must be addressed, and the qualification process will likely be different for lateral and vertical GaN power devices.

2.5 Operating Temperature and Thermal Design

GaN devices exhibit a positive temperature coefficient for $R_{ds,on}$, similar to that of Si. Figure 2.11 shows the trend of $R_{ds,on}$ over temperature for several commercial GaN HFETs. These trends

are derived variously from data sheets and published characterizations. The threshold voltage of most GaN devices is relatively stable over temperature. According to [102] and Chapter 4 of this thesis, e-mode devices exhibit increasing switching loss with higher temperature due to the decreasing transconductance. This was shown experimentally in [41],[72],[84],[102]. Panasonic has the best reported performance at higher temperature of these devices listed.

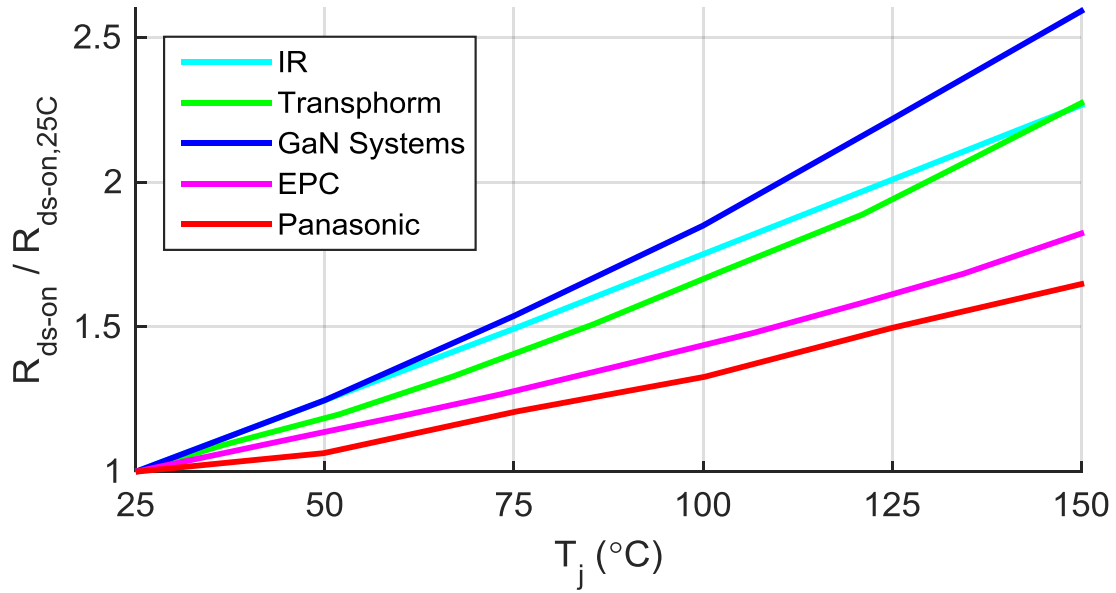


Figure 2.11. Normalized on-resistance of commercial GaN HFETs [26],[60],[69],[72],[84].

Thermal design for some GaN devices can be challenging, depending on the package type. Surface-mount devices with bottom-side cooling require a connection to a heatsink through the board, using thermal vias [103]. Top-cooled devices are also available from some vendors, and others use TO-220 packages that make thermal design easier. As compared with SiC, thermal design is especially critical for GaN-based converter design, because of the potential thermal runaway from both conduction loss and switching loss.

2.6 *Switching Behavior*

GaN devices switch much faster than Si devices with similar voltage and current ratings. The input capacitance C_{iss} and gate charge Q_g are lower for GaN HFETs than Si MOSFETs. The output capacitance C_{oss} is also lower for GaN due to the smaller die size, as mentioned previously. Compared with a Super Junction MOSFET, the output capacitance of GaN devices at high drain-source voltage is often roughly the same at high voltage, but is several orders of magnitude lower at low voltage. GaN switching speed can exceed 200 V/ns, and the turn-on and turn-off delay times can be under 10 ns at 400 V [84].

In hard-switched converters, the two significant sources of switching energy losses are the energy related to stored charge in the output capacitors (C_{oss} loss) and the loss from conduction of the load current through a saturated device channel (overlap loss). In [104], it was shown that two selected e-mode devices experienced lower C_{oss} -related loss than a selected cascode with similar ratings, but higher overlap loss during turn-off. This study concluded that the cascode was better for soft switching and the two e-modes were more suitable for hard switching. However, such a comparison is very difficult to make in a universal sense, because of differences in die size and current ratings from device to device.

The switching behavior for a given device depends on the gate driver IC, converter topology, and board layout. Switching losses and speeds are difficult to approximate from device datasheets. The approximate capabilities of a given device can be determined experimentally with a double pulse test (DPT). Performing a DPT for WBG devices is a challenge in itself [43], but DPT results for many commercial GaN devices have been published [41],[46],[72],[84],[104],[105]. Although these characterizations are still not accurate when applied to a different converter, they may allow for approximation of overall converter loss for the purposes of device selection and thermal design.

2.7 Device Packaging and PCB Layout

Fast switching transients magnify the impact of parasitic inductances in device packaging and printed circuit board (PCB) traces, because the voltage drop across any stray inductance is equal to

$$v_{stray} = L_{stray} \frac{di}{dt} . \quad (3)$$

Package parasitics such as L_d , L_s , and L_g worsen the ringing that occurs during and after the switching transient, which limits the switching speed and may cause damage to the device. The common-source inductance L_{cs} couples the high di/dt from the power loop into the lower-voltage gate loop. The voltage drop across L_{cs} reduces the applied gate voltage during turn-on and increases it during turn-off, thereby slowing down both switching transients and worsening the switching loss. It is crucial that common-source inductance be minimized, in the package as well as board layout. Some devices provide a Kelvin source connection, a separate connection to the source metallization that is only used by the gate loop, decoupling it more effectively from power loop transient effects [105-108].

Overall parasitics can be reduced by combining the high-side and low-side devices in a single module, with decoupling capacitors and optimized internal connections [109]. Integrating the gate driver into the module provides additional benefits, as demonstrated in [110],[111]. TI's LMG5200 is the first commercially available GaN intelligent power module (IPM), built with EPC devices and rated at 80 V. Sanken and TI both also make a driver-integrated module, with a single device and gate driver combined in a surface-mount package, but these are not yet available to order [83].

Lateral GaN devices offer the unique opportunity to monolithically integrate high-side and low-side devices on the same die and nearly eliminate package parasitics. This has been accomplished at 12 V by EPC and Panasonic, although isolation of the two devices on a shared die

may be difficult to accomplish at higher voltage [112],[113]. Furthermore, a GaN-based gate driver can be monolithically integrated on the same die as the HFET for ultra-fast switching capabilities. Navitas has demonstrated success with monolithic integration of a single device and GaN-based gate driver, and GaN Systems has also published work toward this aim [114-116].

2.8 *Commercial Device Availability*

As with any new technology, the relatively low availability of GaN power devices poses a barrier to widespread adoption [21]. Therefore, several of the leading GaN manufacturers have established industry partnerships and taken steps to increase availability of their devices. Transphorm has established agreements with both Fujitsu and ON Semiconductor, to mass produce and co-brand their cascode devices [117],[118]. Panasonic has a licensing agreement with Infineon to establish dual sourcing of the GIT [119]. GaN Systems has recently ramped up its production ten times at their foundry, TSMC [120]. With these recent steps toward mass production, availability of GaN power devices may no longer be a barrier to industrial adoption.

2.9 *Gate Driver Considerations*

Beyond understanding the internal device structures, it is important that the power electronics engineer understand how the structures will impact converter design. Because of the faster switching and unique characteristics of HFETs, common design practices for Si-based converters may not take full advantage of GaN. In fact, simply replacing a Si MOSFET with a GaN HFET will likely cause the converter to stop functioning, and may even destroy the GaN device itself. This section will cover the critical differences between Si and GaN devices, and important considerations for GaN-based converter design.

2.9.1 *Gate Voltage and Current*

Gate driver design for cascode devices is similar to driving conventional Si MOSFETs, because the input of a GaN cascode is a rugged Si MOSFET gate. However, e-mode GaN HFETs

have more specific gate driver requirements. The threshold voltage of an e-mode HFET is typically 1-2 V, and the recommended driving voltage is typically around 5 V. This only allows a few volts of ringing before spurious switching events occur, during both turn-on and turn-off transients. Gate rupture is also a known issue with e-mode GaN devices. Even a small gate voltage overshoot may destroy the device.

Relatively few gate driver ICs on the market are designed specifically for the requirements of GaN devices. The LM5113 from TI is a dual driver designed for GaN that can drive both high-side and low-side devices, and can isolate the high-side driver up to 100 V. Therefore, this driver is not suitable for higher-voltage applications. The LM5114 can drive any single GaN device, but it does not provide signal isolation [121].

Typically, gate driver ICs are chosen based on the specified current capability, but this number is not an accurate description of the IC's suitability for driving GaN, because of the relatively short switching time of the GaN device. Instead, the on-resistance and the rise and fall time of the pull-up/source and pull-down/sink transistors can be used for the comparison. The rise and fall time should be lower than the turn-on and turn-off delay times of the GaN device, or as close to them as possible, to avoid limitations on the switching speed during the crucial overlap times [122]. The source and sink on-resistances effectively add series gate resistance for the turn-on and turn-off paths and should be considered when choosing external gate resistors.

The Panasonic GIT is somewhat unique in its steady-state gate current requirement. Although the device is voltage-driven, full enhancement of the channel requires a small steady-state gate current in the mA range. The diode characteristic of the gate limits the input voltage below 5 V, but a higher driving voltage is desirable during the turn-on transient to enable faster switching. This can be accomplished with an RC-type gate driving circuit, or a multi-stage driver

as demonstrated in [123]. Panasonic has recently released a commercial driver IC for its device that includes this feature [124].

2.9.2 *Common Mode Transient Immunity*

Silicon Labs also makes a series of isolated gate driver ICs that are optimized for GaN devices, compatible with driving voltages from 3 to 30 V and bus voltages in the kV range. These devices use digital isolators based on RF modulation as opposed to optical isolators, providing superior common-mode transient immunity (CMTI). Insufficient CMTI may allow spurious switching events when the dv/dt exceeds the CMTI specification [125]. While several isolated drivers have specified typical CMTI of 50-100 kV/ μ s, this characteristic varies due to process variation and temperature. The actual CMTI may be as low as the specified minimum, which may be much lower than the typical value. Available isolation methods have been reviewed for several GaN-based converters [126],[127], and it is generally concluded that these RF-based digital isolators tolerate higher dv/dt than alternatives such as optocouplers or capacitive isolators. The newer Si827x family has a specified minimum CMTI of 200 kV/ μ s, much higher than any other available isolated gate driver [128]. Of course, even with a sufficient CMTI-rated gate driver IC, the PCB layout must be designed very carefully to prevent common-mode interference through stray impedances. To further improve CMTI, other techniques may be implemented in the gate drive circuit, such as a common-mode choke or differential connection of the digital signal inputs [129],[130].

2.9.3 *Cross-Talk*

Another source of spurious switching events is interference between high-side and low-side devices due to the Miller effect. This may cause cross-talk, also known as cross-conduction or Miller turn-on, a phenomenon in which one device is inadvertently turned on due to the dv/dt on its Miller capacitance when the complementary device in the same phase leg is intentionally turned

on. This cross-talk allows a shoot-through current to flow from the dc bus across the saturated channels of both devices, incurring additional switching losses. In a phase leg configuration, cross-talk losses may be especially noticeable during light load operation, when the overlap losses are nearly zero and the turn-on switching speed is highest [131].

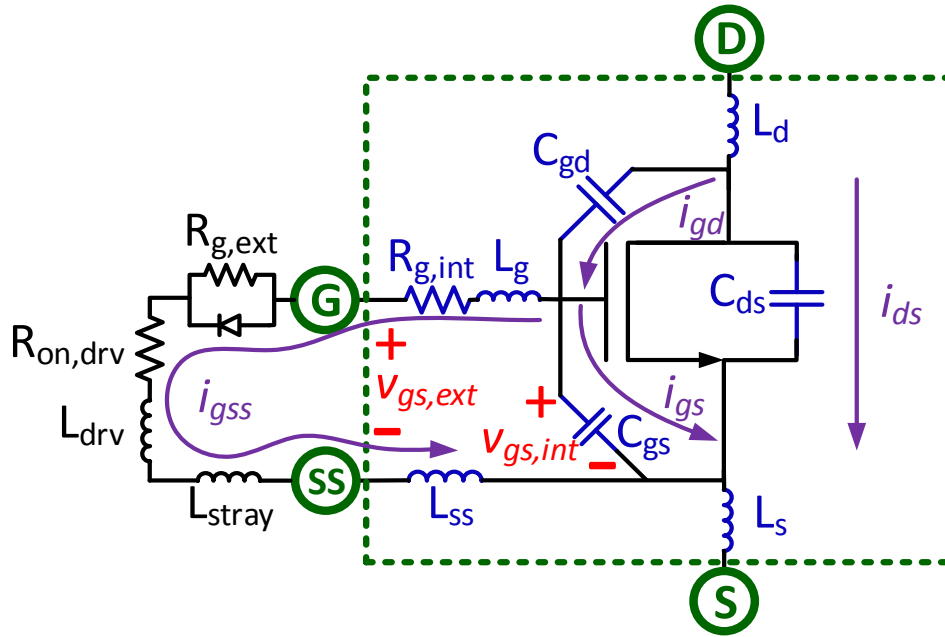


Figure 2.12. Mechanism causing cross-talk in the synchronous device of a phase leg.

Figure 2.12 shows the cross-talk mechanism for this device, including the parasitic impedances of the device, PCB, and gate driver IC. As current flows through the Miller capacitance C_{gd} to displace its charge, the same current will be split between the junction capacitance C_{gs} (i_{gs}) and the gate loop (i_{gss}). If i_{gs} deposits sufficient gate charge to raise $v_{gs,int}$ above its threshold during active device turn-on, the synchronous device will also turn on and cause shoot-through losses. Similarly, during active device turn-off, the synchronous device displacement current induces a

negative voltage on $v_{gs,int}$, which increases conduction losses during dead time when the device is operated in SCRC mode.

Kelvin-source connections are often used in WBG devices to reduce common-source inductance. This is overall beneficial to gate voltage oscillation, but the Kelvin terminal also creates a much higher gate loop inductance than in the power loop. This gate loop inductance resonates with the capacitances C_{gs} and C_{gd} during switching, causing excessive oscillation as well as a mismatch between the true internal gate voltage and the measured external gate voltage. It is difficult to characterize the cross-talk mechanism for WBG devices by directly viewing the external gate-source voltage because of this mismatch.

Cross-talk can be prevented by slowing down the turn-on transient (e.g. with a higher turn-on gate resistance) but this will also increase the overlap losses. The tradeoff between overlap and cross-talk loss will be different for every converter, based on the device, driver, switching speed, and operating conditions. However, there are several techniques to minimize cross-conduction effects. One common method to prevent cross-talk for SiC devices is to use a negative voltage supply for the off-state. However, this is non-ideal for enhancement-mode GaN devices, because it increases the reverse conduction losses during dead time. Another method to mitigate cross-talk is adding an external capacitor in parallel with the internal device C_{gs} , slowing the switching transients to limit dv_{ds}/dt while also providing a low-impedance path for the C_{gd} displacement current. However, this is also not desirable due to increased overlap and driving losses.

The simplest cross-talk mitigation method for GaN may be to use $0\ \Omega$ gate resistance for the turn-off path and a higher resistance for the turn-on path, however this will also increase overlap losses somewhat. Some drivers provide separate paths for gate current during turn-on and turn-off. If the driver does not provide separate paths, a Schottky diode can be added in parallel with the

gate resistor [132],[133]. The most effective solution for cross-talk mitigation may be an active gate driver as demonstrated in [131] for SiC.

2.10 Summary

The basic structures and characteristics of GaN power devices have been reviewed, including both vertical and lateral devices. The commercial status and specifications of normally-off GaN power devices were summarized. Currently, two manufacturers produce enhancement-mode GaN HFETs for open online ordering, as well as one cascode. Several lateral device manufacturers are providing samples of their e-mode and cascode devices, and vertical device samples may also be available soon. As the availability and performance of commercial GaN devices continues to improve, GaN-based converter design skills will need to keep pace with these device developments. Here, GaN-based converter design considerations were reviewed, including switching characterization, packaging, board layout, gate driver design, reverse conduction mechanisms, dynamic $R_{ds,on}$, and thermal design. The breakdown mechanisms and reliability concerns were also discussed, as well as the qualification process to characterize the reliability of commercial GaN devices. This review provided an introduction to GaN-based power devices, in order to help readers effectively use GaN to design high-frequency and high-efficiency converters.

Because this review discussed vertical GaN as well as cascode and e-mode lateral GaN, it presents the opportunity to compare these technologies in terms of performance and commercial readiness. In terms of maturity, cascode devices have been produced commercially for longer than most other GaN devices at the 600 V level, and have been shown to be capable of very high-speed and low-loss switching. However, the fewer internal components and interconnections of enhancement-mode HFETs may enable higher reliability as the technology continues to mature. Recently available vertical GaN devices are the youngest of these, and very little is known of their performance relative to their laterally-structured cousins, but the material properties of GaN

indicate that they should be able to achieve superior performance to SiC MOSFETs when the challenges of wafer and vertical device fabrication are overcome. At the moment, there is no clear winner between these three categories of GaN power devices, and each product may find its own niche at a particular range of voltage, current, and switching frequency.

Chapter 3

Characterization of an Enhancement-Mode GaN HFET

3.1 Introduction

As mentioned in the previous chapter, normally-off power GaN devices are currently produced as one of two fundamental types: cascode and enhancement-mode. Cascode GaN devices are a convenient way to produce a normally-off device, but they have reliability and switching performance limitations. Alternatively, an enhancement-mode GaN device can be directly fabricated with several different gate structures. The HFET is a fundamentally different device from Si or SiC MOSFETs, and e-mode modification techniques make each HFET unique from each other as well [49]. The detailed methodology for characterizing the static and switching performance of power devices, particularly Si and SiC, have been presented by previous works [32],[35],[43],[134]. However, some of these procedures and test setups must be revised for GaN devices, and the analysis of the results is different due to the fundamentally different device structure.

The GaN Systems GS66508 was the first e-mode GaN HFET commercially available at the 650 V and 30 A rating, although higher current rated devices have since become available in the past year. However, the full datasheet has not yet been made available with all the necessary static performance curves or switching loss data [70]. Performance characterization has been published about other commercial and near-commercial GaN devices, such as Transphorm, EPC, Panasonic, IR, and HRL [38],[41],[75],[135],[136]. The goal of this chapter is to provide a full range of performance data, for loss estimation in an enhancement-mode GaN-based converter with GS66508 devices.

Several devices were fully characterized for the static results, but the dynamic results are based on testing of only a few devices, because testing beyond the rated capabilities of the device

did not often allow devices to survive multiple rounds of testing. However, the dynamic performance of different devices from the same generation (E05) was compared throughout the characterization process, and it was found to be very consistent.

3.2 *Static Characterization*

3.2.1 *Curve Tracer Test Setup*

Static performance was tested using the Tektronix 371b curve tracer. The surface-mount device was soldered on a PCB and connected to the curve tracer with a four-wire Kelvin connection, and the results were compensated for the 3.7 m Ω wires soldered directly to the pads of the device. The device was heated by a digitally controlled custom Wencesco hot plate, connected through the board with thermal vias, an aluminum block, and thermal grease. Junction temperature was verified with a temperature transducer soldered beside the device on the same copper plane. This technique allowed for precise control of the steady-state junction temperature, despite the heat lost between the hot plate and the device.

A 1 k Ω resistor was connected in series with the gate, and the voltage drop across this shunt resistor was measured with a precision multimeter to determine dc gate current. The driving voltage was increased to compensate for the voltage drop, so the gate-source voltage in the following figures was the actual voltage on the device terminals, and not simply the driving voltage from the curve tracer.

3.2.2 *On-Resistance*

Figure 3.1 shows the first and third quadrant output characteristic of one of the tested devices at room temperature, including the on-state operation with the gate voltage above the threshold and the so-called “self-commutated reverse conduction” (SCRC) operation described in the previous chapter.

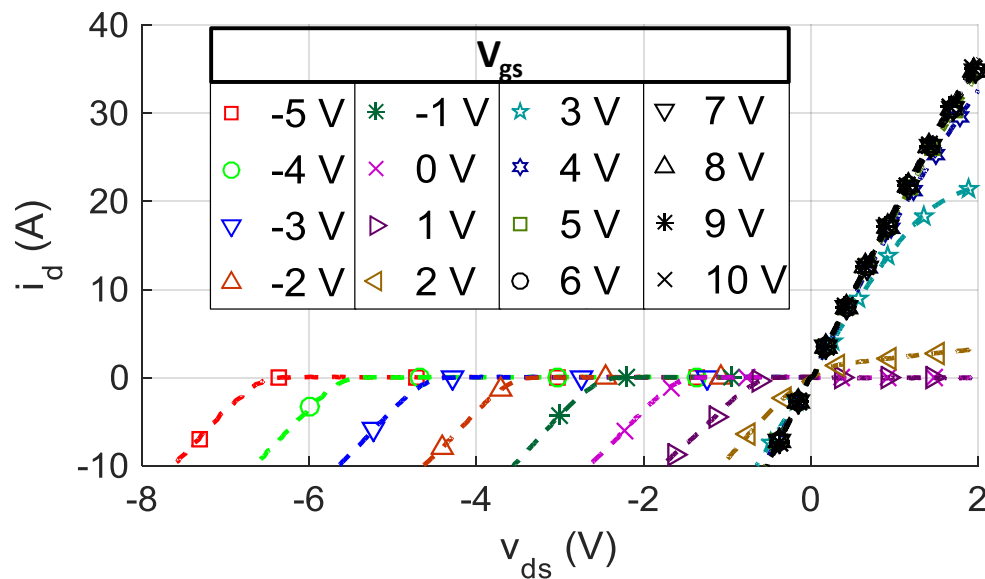


Figure 3.1. Output characteristic at $T_j = 25^\circ\text{C}$.

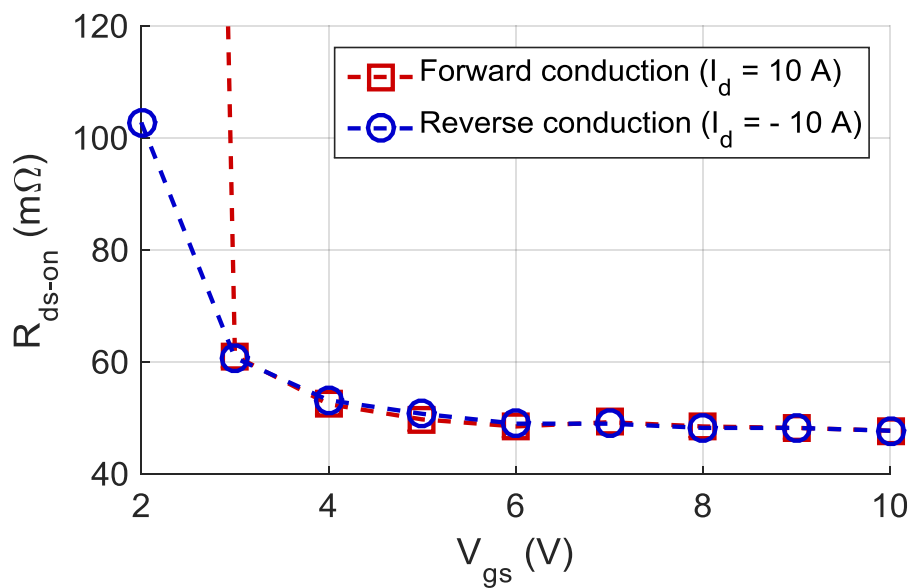


Figure 3.2. On-resistance at $T_j = 25^\circ\text{C}$, over increasing gate voltage.

Figure 3.2 shows the calculated R_{ds-on} with a load current of ± 10 A. As expected, the forward-conduction and reverse-conduction on-resistances were equivalent, and they both dropped with higher the gate voltage. However, the reduction in on-resistance was not very significant above 5 V.

Output characteristics were also recorded with junction temperatures up to 150 °C. As the junction temperature increases, on-resistance increased linearly with temperature, and increased by 2.5 times at the maximum operating temperature of 150 °C as shown in Figure 3.3. Several devices were tested across the temperature range, and this relative increase varied by as much as 10%.

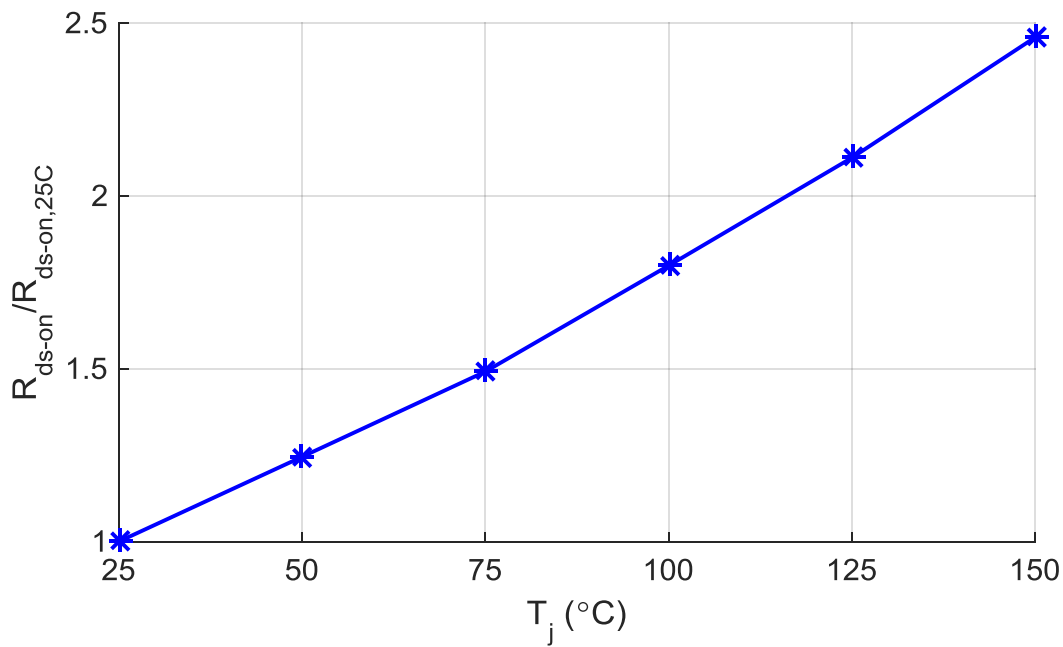


Figure 3.3. On-resistance over increasing junction temperature.

The published R_{ds-on} from the manufacturer was actually higher than the results shown here. This may be intended to account for some dynamic R_{ds-on} due to the current collapse phenomenon. However, dynamic R_{ds-on} is very difficult to measure accurately, and a special test fixture must be

designed for this purpose. The characterization of dynamic R_{ds-on} will be performed as part of a separate work.

The on-resistance also has a relationship with drain current, because higher current brings the drain-source voltage closer to the point of saturation. The results in the previous two figures are based on the on-resistance at 10 A, because there is no noticeable change from 0 A to 10 A. However, at the full rated current of 30 A, there is an increase of up to 10% at any given condition in the ohmic region. Figure 3.4 and Figure 3.5 show this relationship at 25 °C and 125 °C, respectively. In the higher temperature case, the channel enters the saturation region at a lower drain current than it does at room temperature, so there appears to be a stronger relationship with drain current. However, with a gate voltage of 5 V or higher and within the current rating of the device, the same increase of approximately 10% occurs at either temperature.

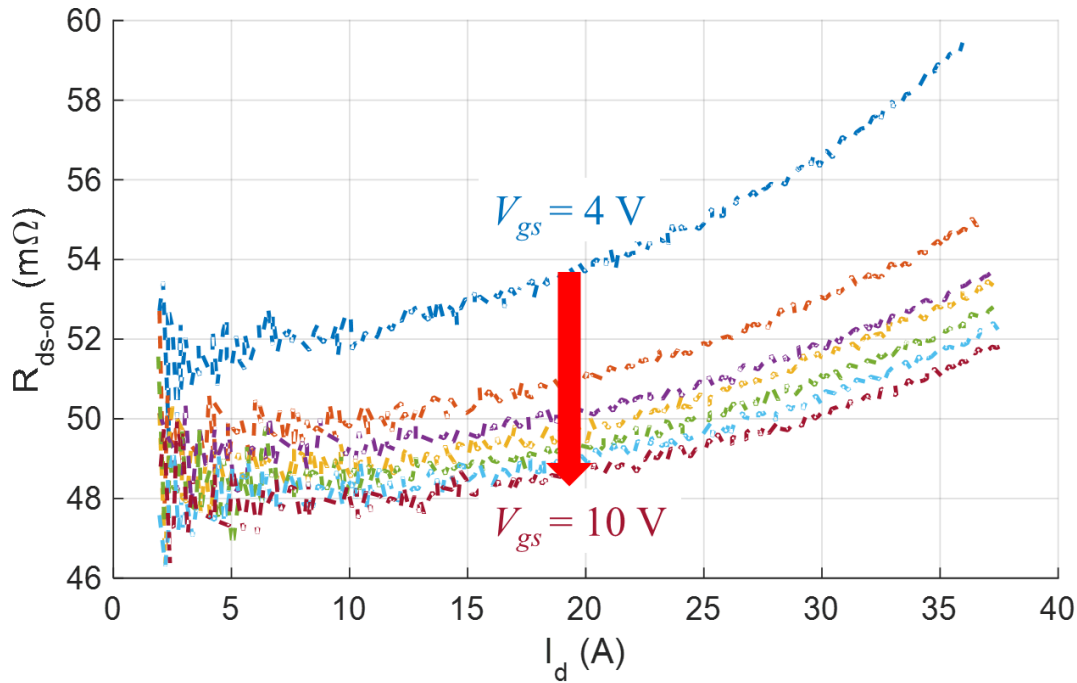


Figure 3.4. On-resistance vs. drain current at $T_j = 25\text{ °C}$.

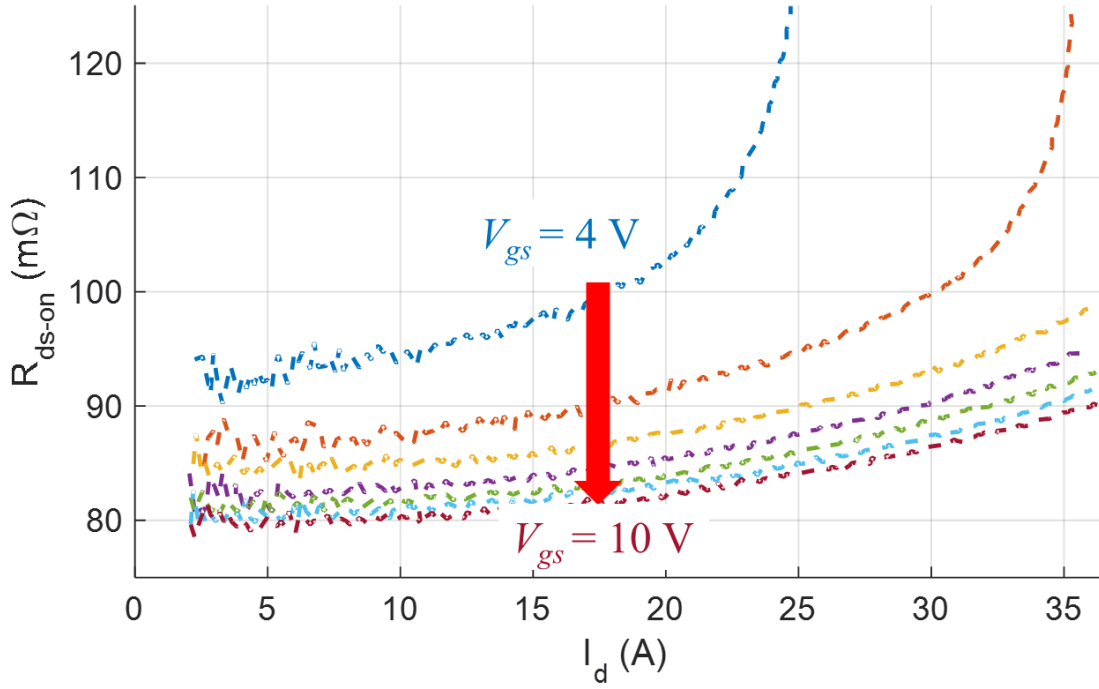


Figure 3.5. On-resistance vs. drain current at $T_j = 125\text{ }^{\circ}\text{C}$.

3.2.3 Self-Commutated Reverse Conduction (SCRC)

SCRC is the third quadrant operation in which the device behaves similar to a body diode, given by (2). It is noteworthy that in enhancement-mode GaN HFETs, the V_{ds} offset scales linearly as V_{gs} drops below the reverse threshold voltage ($\sim 1.6\text{ V}$). This is because SCRC is not truly diode behavior. Rather, the device turns on its own channel when a negative output voltage biases the gate-drain voltage V_{gd} above its threshold voltage. However, the effective channel resistance during SCRC, $R_{sd,rev}$, is higher than R_{ds-on} . When $V_{gs} < V_{gs,th}$, reverse conduction forces the device into saturation, but only just past the knee between ohmic and saturation regions. A more negative V_{gs} drives the device even further into saturation, and $R_{sd,on}$ becomes more dominated by the reverse transconductance rather than the typical ohmic on-resistance. Figure 3.6 shows $R_{sd,rev}$ at 10 A, over a range of V_{gs} and T_j . In addition to higher resistance, a more negative V_{gs} also increases the diode-like forward voltage drop as given in (2), so this is generally an undesirable mode of operation.

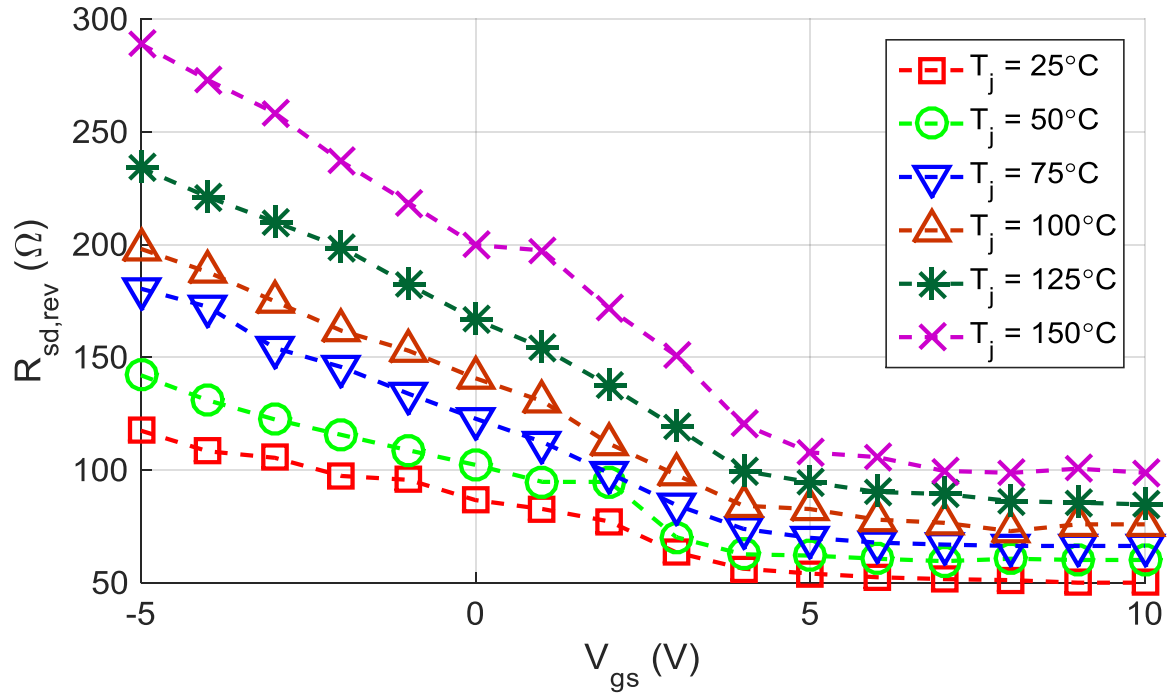


Figure 3.6. Reverse conduction on-resistance at 10 A.

3.2.4 Transfer characteristic

The transfer characteristic was measured with $V_{ds} = 5$ V to capture the saturation current I_{dss} , transconductance g_{fs} , and threshold voltage $V_{gs,th}$. The results are shown in Figure 3.7. One notable feature of this GaN HFET is that its transconductance drops significantly as the junction temperature increases. In contrast, Si and SiC devices do not typically experience much change in transconductance with elevated temperature. This characteristic is typical for e-mode GaN devices, and have consequences for switching loss that will be explained in the next section. Figure 3.8 shows the average transconductance across the temperature range, calculated using the average slope of the curves in Figure 3.7 between 2 V and 5 V, as compared with the values calculated similarly using the datasheet's transfer characteristics.

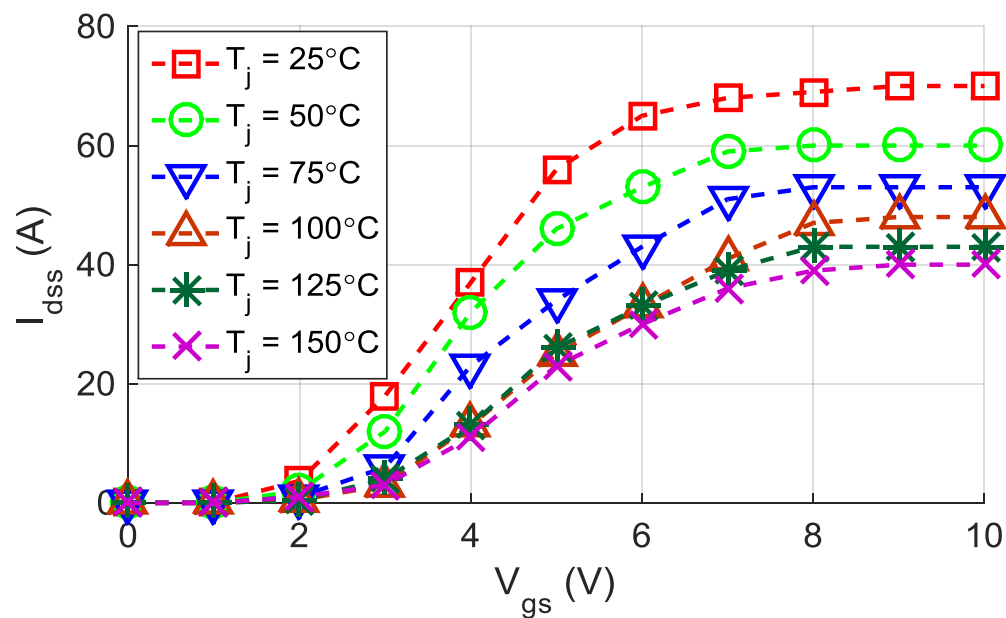


Figure 3.7. Transfer characteristic over increasing junction temperature, $V_{ds} = 5\text{ V}$.

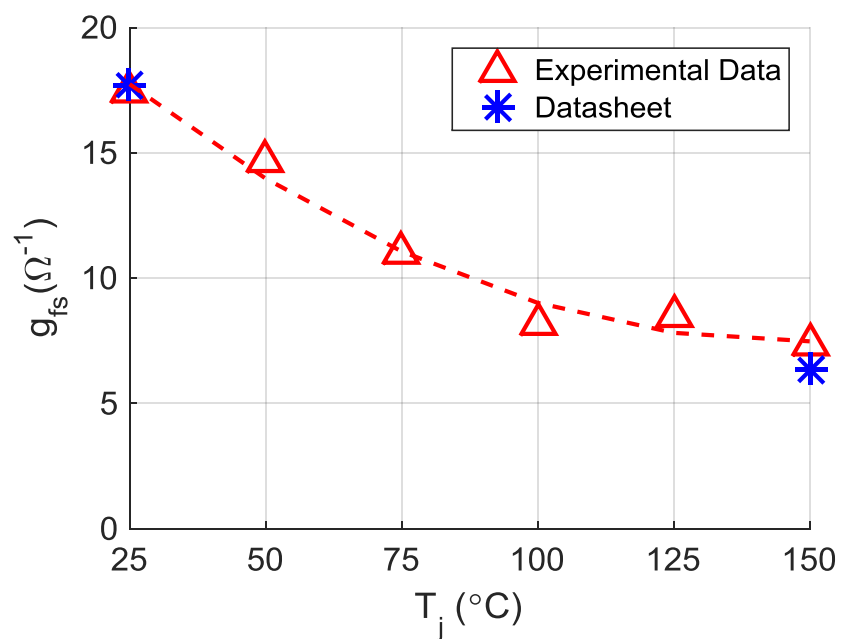


Figure 3.8. Average transconductance of GS66508P, calculated based on static testing and the transfer characteristics published in the datasheet.

3.2.5 Steady-State Gate Current

The manufacturer has not published any literature about the physical structure of this device's e-mode gate, but some GaN devices experience a diode-like gate current characteristic, such as with Panasonic and EPC, which use p-type doping underneath the gate to raise the threshold voltage. However, an insulated gate device may also experience such a steady-state gate current due to dielectric breakdown of the gate. Therefore, the gate current of the device was measured experimentally using the test setup shown in Figure 3.9. This test can be performed for any device, even on a board populated with a driver circuit, but the driver circuit must be disconnected to isolate the gate input from the gate loop on the board.

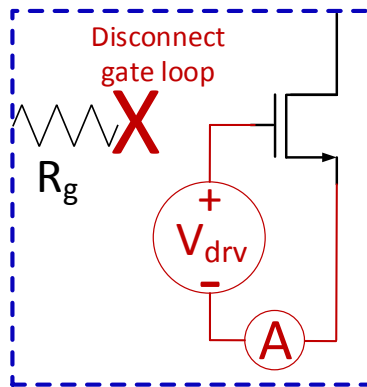


Figure 3.9. Test setup for measuring steady-state gate (leakage) current.

A steady-state gate leakage current was observed at the mA scale within the rated gate voltage range, shown in Figure 3.10 for one sample. The data sheet specifies 40 μA gate leakage current at the recommended driving voltage of 7 V and at 25 $^{\circ}\text{C}$, which was confirmed in this testing. However, the leakage current increases by an order of magnitude at higher junction temperature, and even further with increased driving voltage above 7 V. This does not necessarily

indicate a problem with the device, but should be considered in gate driver IC selection and converter design.

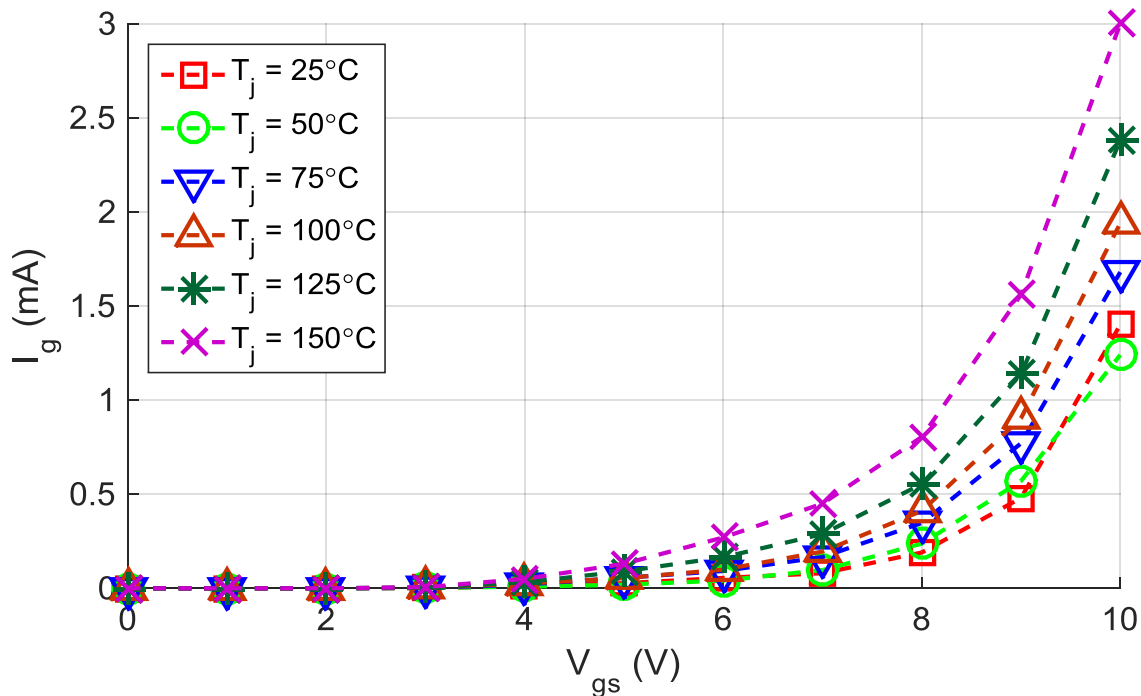


Figure 3.10. Steady-state gate (leakage) current of GS66508P over increasing gate voltage and junction temperature.

3.2.6 Junction Capacitances

The device output capacitance C_{oss} was measured with an impedance analyzer, with the gate and source shorted together and a positive voltage bias between the drain and source up to 200 V. The output capacitance characteristic is shown in Figure 3.11. The capacitance was first measured for both devices with the thermal pad disconnected, so that the capacitance between the drain and substrate was neglected. The two devices were also measured in place on the double pulse test board described in Section III, with the source and substrate connected on the board. The bare board itself introduced an additional 9 pF of parasitic capacitance on the low side and 12 pF on the

high side. These additional capacitances were subtracted for the device capacitance characteristic, since this will vary from board to board. The parasitic drain-substrate capacitance was calculated based on these measurements, and it was found to be quite significant across the full voltage range. This additional output capacitance can be bypassed on the board to reduce hard switching losses, because the source-substrate connection is optional. However, leaving the substrate (thermal pad) electrically floating is not recommended by the manufacturer due to the higher dynamic R_{ds-on} with this option.

This curve has been provided by the manufacturer datasheet since the time of the original test, and is shown in Figure 3.12. The C_{oss} matches well, but the datasheet shows a lower capacitance at high voltage than was measured experimentally. This plot also shows the characteristic for the input capacitance C_{iss} and reverse transfer (Miller) capacitance C_{rss} as well, which were not measured in this experimental setup. Therefore, the datasheet was used to determine for these capacitances in later switching transient analysis.

However, the input capacitance is strongly proportional to the input voltage, which cannot be determined from Figure 3.12. Instead, the published gate charge characteristic was used to determine the input capacitance before and after the dv/dt interval, using the slope of the line. During dv/dt , the Miller effect makes the gate charge characteristic cease to accurately represent the input capacitance, but the input capacitance can be estimated as constant during this period since it is the same before and after. An averaging filter was applied to the result, since the resolution of the datasheet induced some noise in the calculation. Although the calculated C_{iss} is shown to match the datasheet specification fairly well at 0 V gate bias, it increases significantly as the device nears its threshold voltage of ~ 1.6 V, then remains steady at approximately 650 pF as the device is further enhanced.

The terms used here are typical capacitances characterized in datasheets, because they are

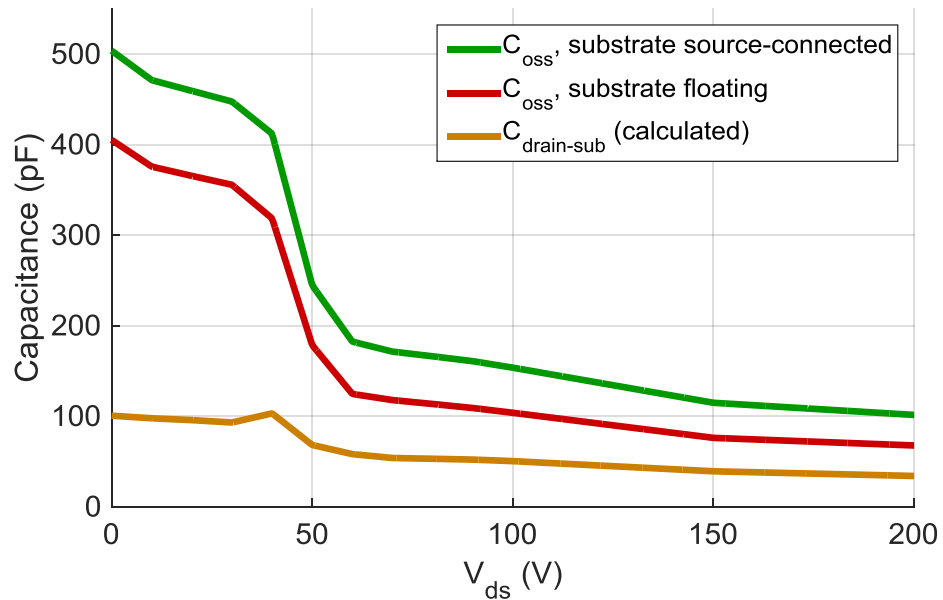


Figure 3.11. Output capacitance of GS66508P measured on-board and off-board.

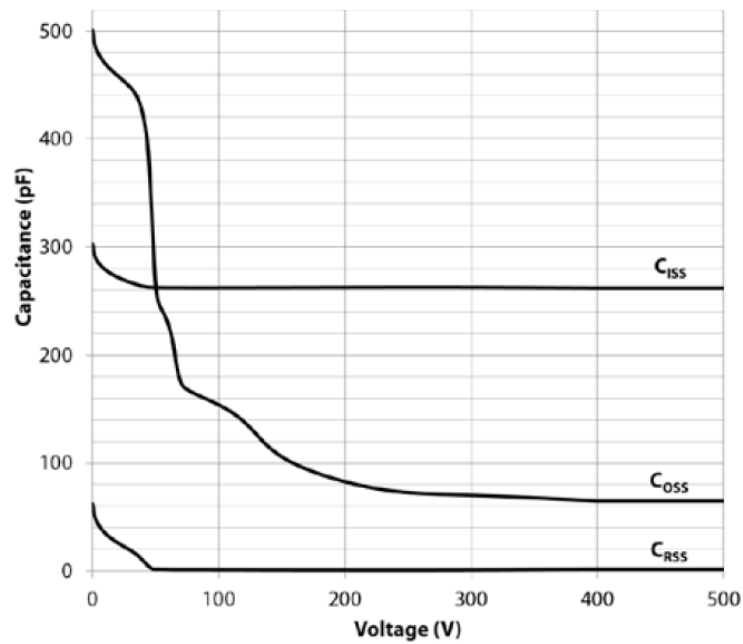


Figure 3.12. Published junction capacitance curves from GS66508P datasheet [70].

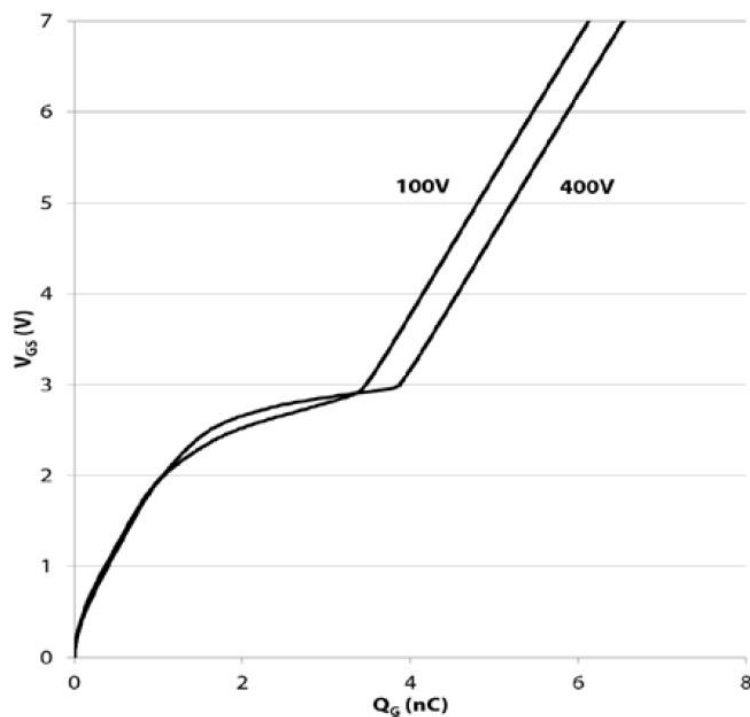


Figure 3.13. Published gate charge characteristic from GS66508P datasheet [70].

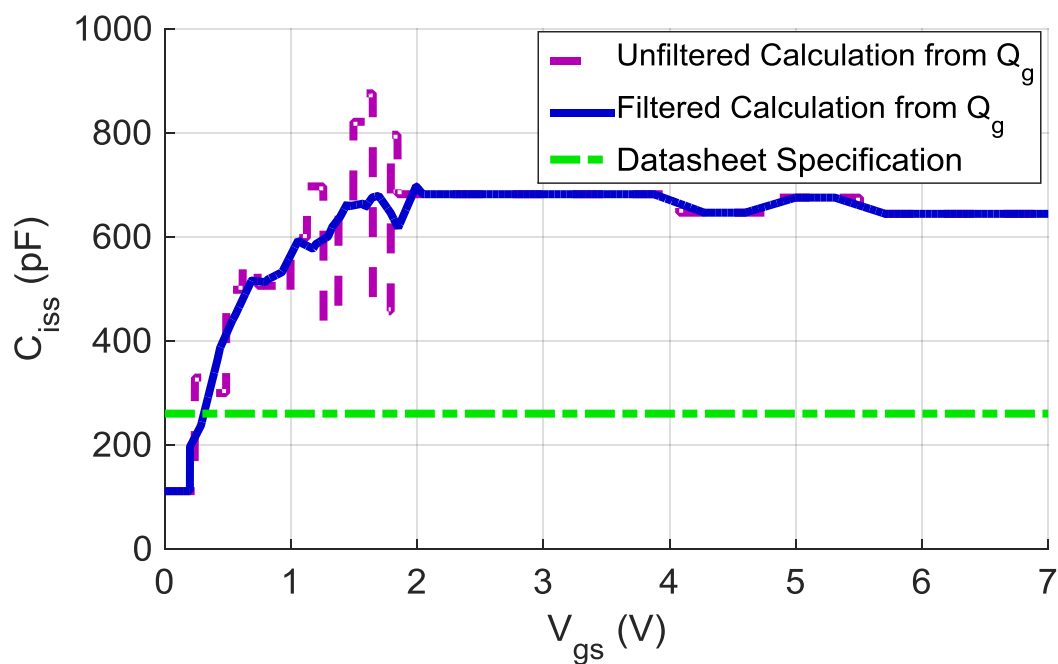


Figure 3.14. C_{iss} - V_{gs} curve calculated using published Q_g characteristic from GS66508P datasheet [70].

the most convenient to measure experimentally. However, the three internal junction capacitances of the device are C_{gs} , C_{gd} , and C_{ds} , which can be determined from the typical characteristics by the following equations.

$$C_{oss} = C_{ds} + C_{gd} \quad (4)$$

$$C_{iss} = C_{gs} + C_{gd} \quad (5)$$

$$C_{rss} = C_{gd} \quad (6)$$

3.3 *Dynamic Characterization*

3.3.1 *Double Pulse Test Setup*

The dynamic switching performance was characterized with a double pulse test (DPT) board, using the circuit shown in Figure 3.15 and test bench setup shown in Figure 3.16. Typical DPT methodology was followed, as described by [43]. The PWM input to the gate driver was provided by an Agilent 33522A function generator. Both devices were heated in the same method as in the static test setup. A 2.1-mH inductor was used as the load.

3.3.2 *Measurement System Setup*

The current and voltage waveforms were recorded with a Tektronix MSO4104B-L oscilloscope using a sample size of 0.4 ns. Gate voltage was measured with a TPP1000 low-voltage passive probe, with a bandwidth of 1 GHz. Drain-source voltage was measured with a TPP0850 high-voltage single-ended probe, with a bandwidth of 800 MHz. The drain current was measured with a 100 mΩ coaxial shunt from T&M Research, with a bandwidth of 2 GHz. The coaxial shunts were modified to reduce parasitic inductance by trimming the plastic around the base, so that the connecting nuts could clamp around the PCB with no need for metal standoffs or additional nuts.

For each test condition (dc bus voltage, load current, and junction temperature), five points were recorded for turn-on and turn-off. Data was then processed in MATLAB to construct time-base waveforms, and to calculate turn-on and turn-off energy and times as well as other relevant

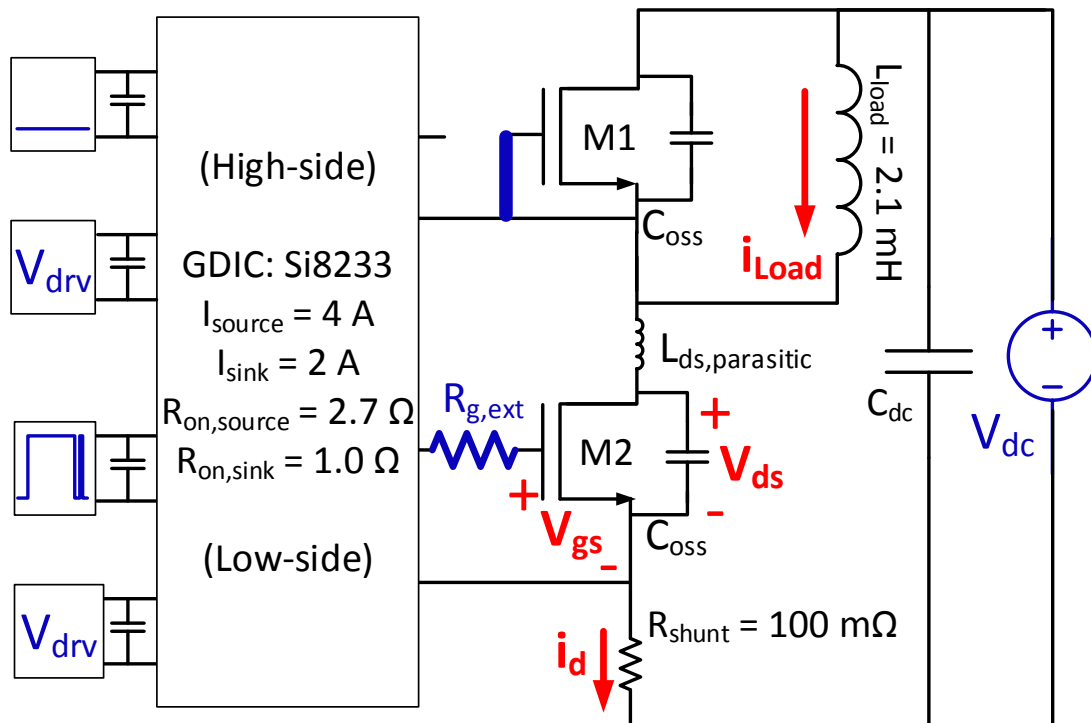


Figure 3.15. Double pulse test circuit schematic.

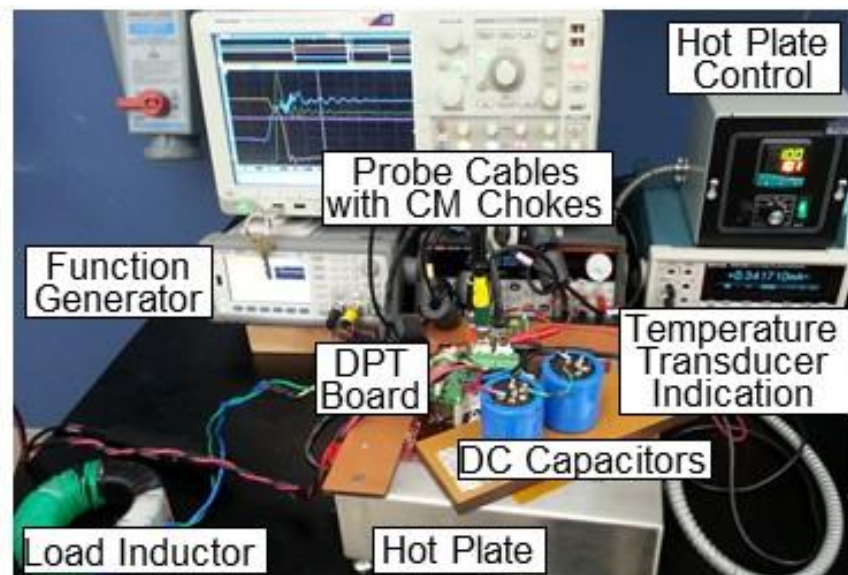


Figure 3.16. Double pulse test bench setup.

parameters. A low-amplitude, low-frequency oscillation was observed in the current measurement due to common-mode noise in the oscilloscope. Several chokes were used on all test leads and power cables to minimize this oscillation, and it was found to be insignificant for all turn-on measurements, and for turn-off measurements above 2 A.

3.3.3 *V-I Alignment and Deskew Technique*

The drain-source voltage and drain current were aligned in the oscilloscope to within 0.1 ns, by adjusting the current channel deskew until the initial drop in v_{ds} was graphically aligned to the calculated voltage drop across the parasitic load inductance L_{ds} on the oscilloscope during the turn-on transient. This method is most effective at high load current when the di/dt transient is most pronounced, so the alignment was initially performed with 37 A, then verified at other operating conditions to check for consistency. Figure 3.17 shows twenty of these alignment waveforms overlaid to verify proper alignment with an error of ± 0.1 ns.

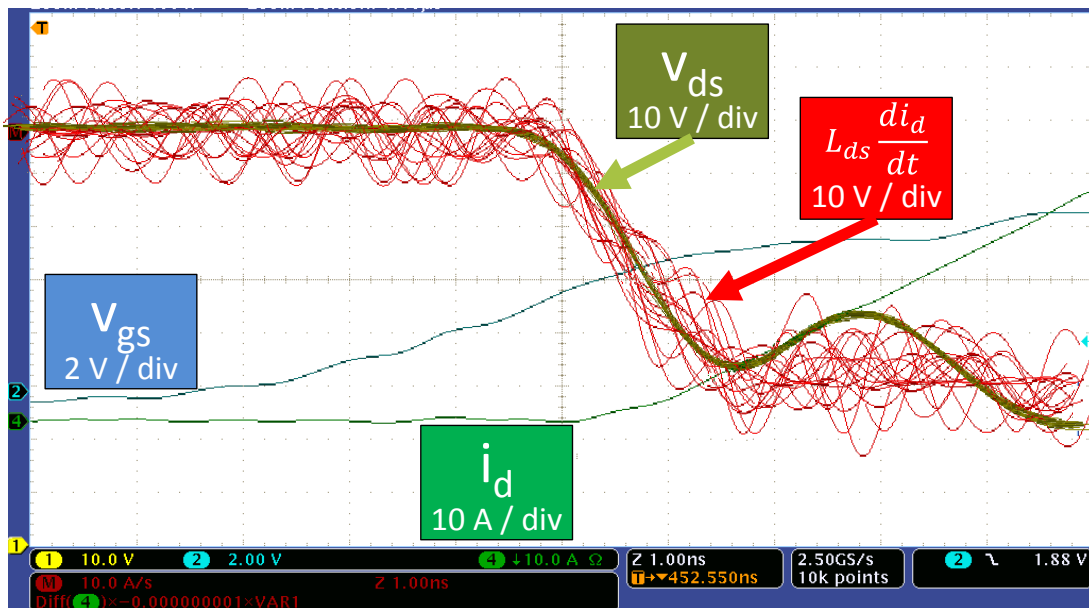


Figure 3.17. I-V alignment waveforms, used to verify current channel deskew.

3.3.4 DPT Board Design

The double pulse test board was designed with a very dense layout, to minimize gate loop and power loop inductance as recommended by [132]. Decoupling capacitors for both the gate loop and power loop were placed very close to the device so that the fastest switching speed could be achieved, and a four-layer board was used with large copper planes used for the power loop. Figure 3.18 shows the top view of the DPT board layout used in this work.

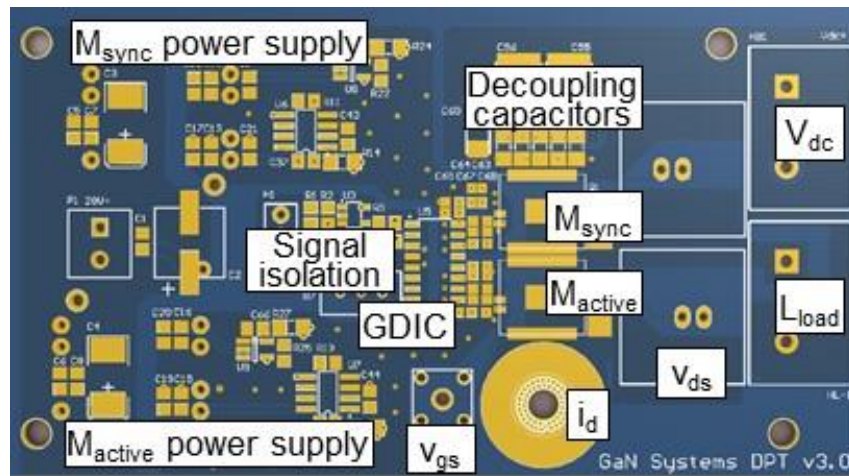


Figure 3.18. DPT board layout.

The active device was driven by the Si8233 gate driver IC, with a single gate resistance path to control the switching speed for turn-on and turn-off. Initially, different gate voltages and resistances were explored, but the best performance was achieved with 8 V (on) and 0 V (off) driving voltages and 0 Ω . A shoot-through current was observed in all cases during turn-on of the active/lower device, caused by Miller cross-conduction. This phenomenon was mitigated in this testing by shorting the gate and source of the synchronous device together with solder and bypassing its gate drive circuit. In a practical converter design, a gate driver is required for both switches. Ref. [122],[131] describe the cross-conduction mechanism in wide bandgap devices and

methods for practical mitigation, such as using a diode in the gate loop to separate the turn-on and turn-off gate resistances.

The Si8233 includes RF-based digital isolation specified at 45 V/ns common-mode transient immunity (CMTI), and isolated power supplies were used for the driving voltage. Additionally, small capacitors were added at the digital input of the gate driver IC to filter out noise and prevent false firing during turn-on transients.

3.3.5 Turn-On Transient Analysis

Figure 3.19 shows the processed turn-on waveforms at 25 °C with 400 V dc bus voltage and 10 A load current. The turn-on delay times $t_{d,on}$ is defined to begin when gate voltage begins to increase, detected based on the slope of the v_{gs} waveform. Likewise, the start of the current rise time t_{cr} was detected using the slope of the i_d waveform. The voltage fall time is defined to begin when the drain current reaches the load current, because the $L_{ds}di/dt$ drop across v_{ds} makes it difficult to detect the start of t_{vf} based on the voltage waveform. The end of t_{vf} was detected based on the slope change of v_{ds} near the zero-crossing.

The current overshoot during t_{vf} is due to the displacement current that charges the upper/synchronous device output capacitor as it turns off. During this same time, the active device discharges its output capacitance through its own channel and causes further loss, but this current is internal and cannot be observed during a DPT. The energy lost by this internal C_{oss} discharge is measured during t_{vr} , as the active device C_{oss} is charged during the preceding turn-off transient. It is also important to note that the current overshoot during t_{vf} does not include any reverse recovery in this case, as it would with a Si or SiC MOSFET body diode. The GaN device does not have a true body diode, so there is no stored minority carrier charge to remove when the synchronous device turns off.

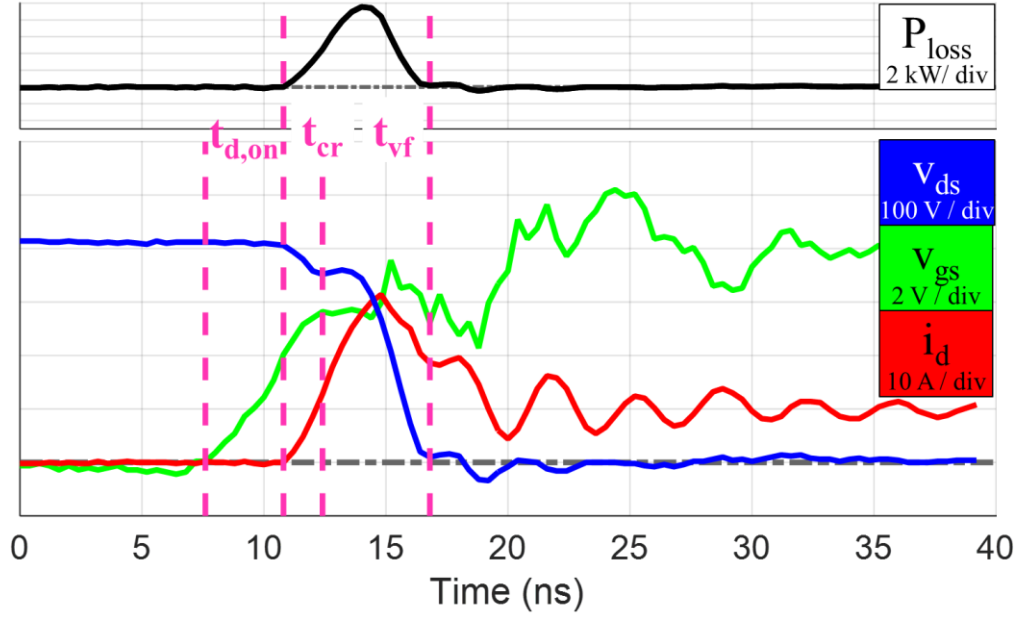


Figure 3.19. Turn-on waveform of GS66508P at 400 V, 10 A, 25 °C.

Although the channel current cannot be measured experimentally, it can be calculated for a given experimental waveform using the derivative of v_{ds} and the output capacitance characteristic, as in

$$i_{Coss} = C_{oss} \frac{dv_{ds}}{dt} \quad (7)$$

$$i_{chan} = i_d - i_{Coss} \quad (8)$$

Using these equations, Figure 3.20 can be generated using experimental results to show the current in the active device channel as well as the measured parameters.

Figure 3.21 - Figure 3.23 show the experimentally calculated turn-on times. Turn-on current rise time increases linearly with load current, whereas turn-on voltage fall time is more correlated to dc bus voltage. The turn-on delay was approximately 4 ns with no correlation to operating conditions.

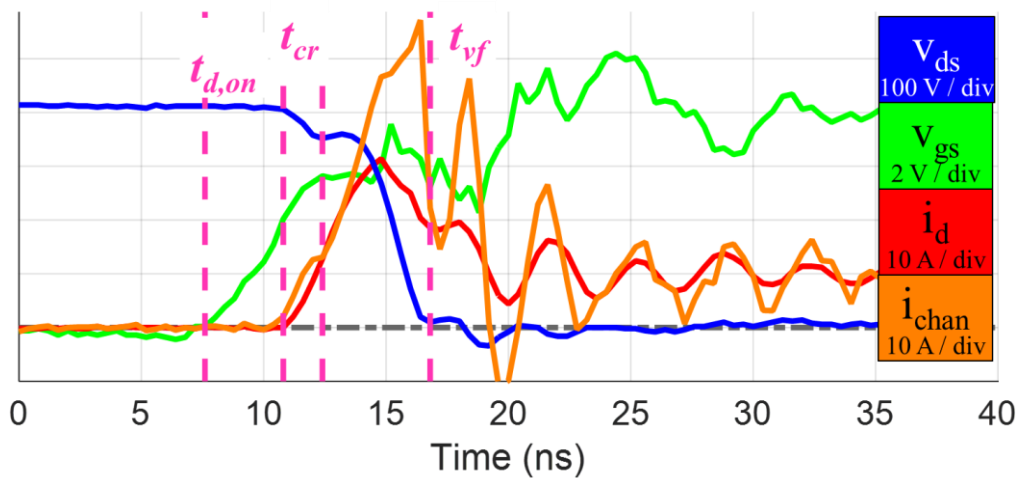


Figure 3.20. Turn-on waveform of GS66508P with calculated channel current at 400 V, 10 A, 25 °C.

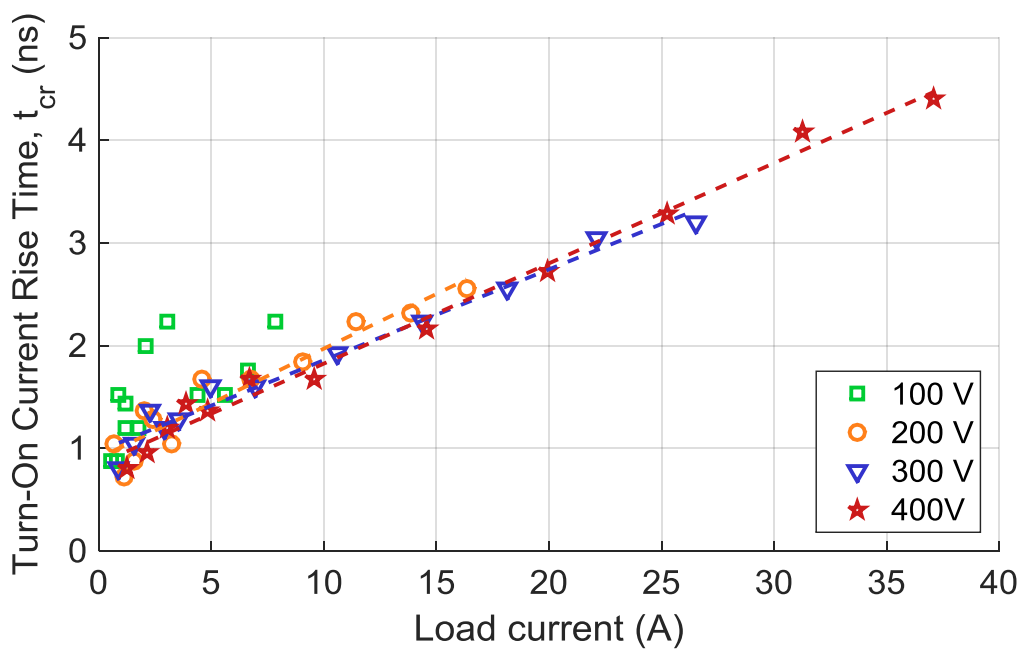


Figure 3.21. Turn-on current rise times of GS66508P at 25 °C.

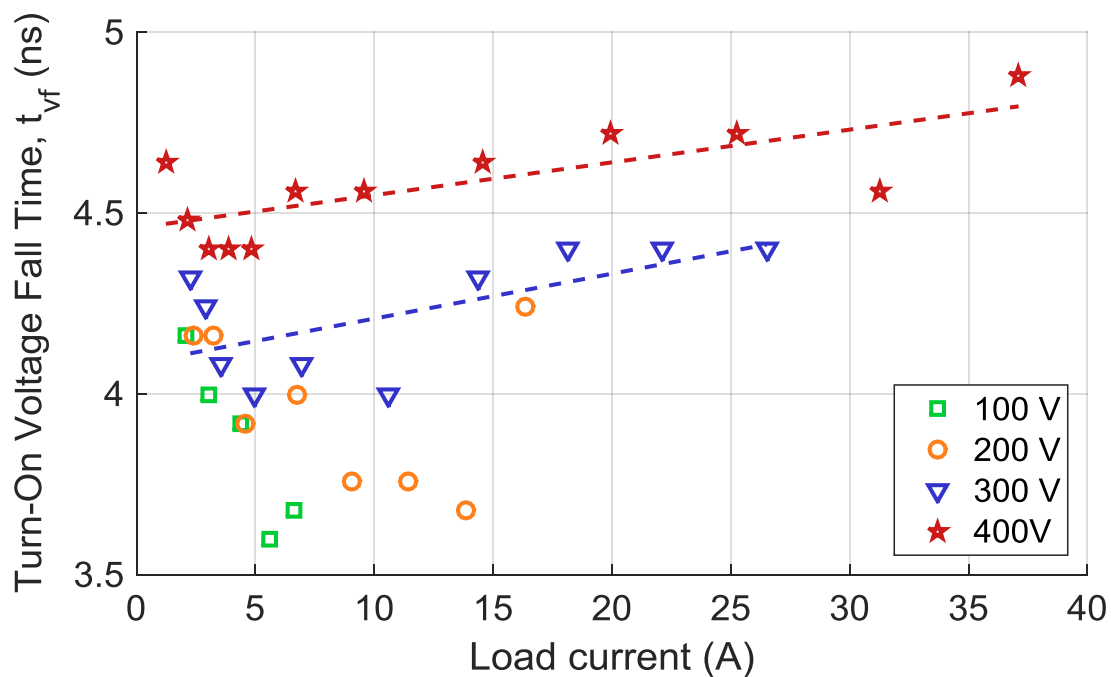


Figure 3.22. Turn-on voltage fall times of GS66508P at 25 °C.

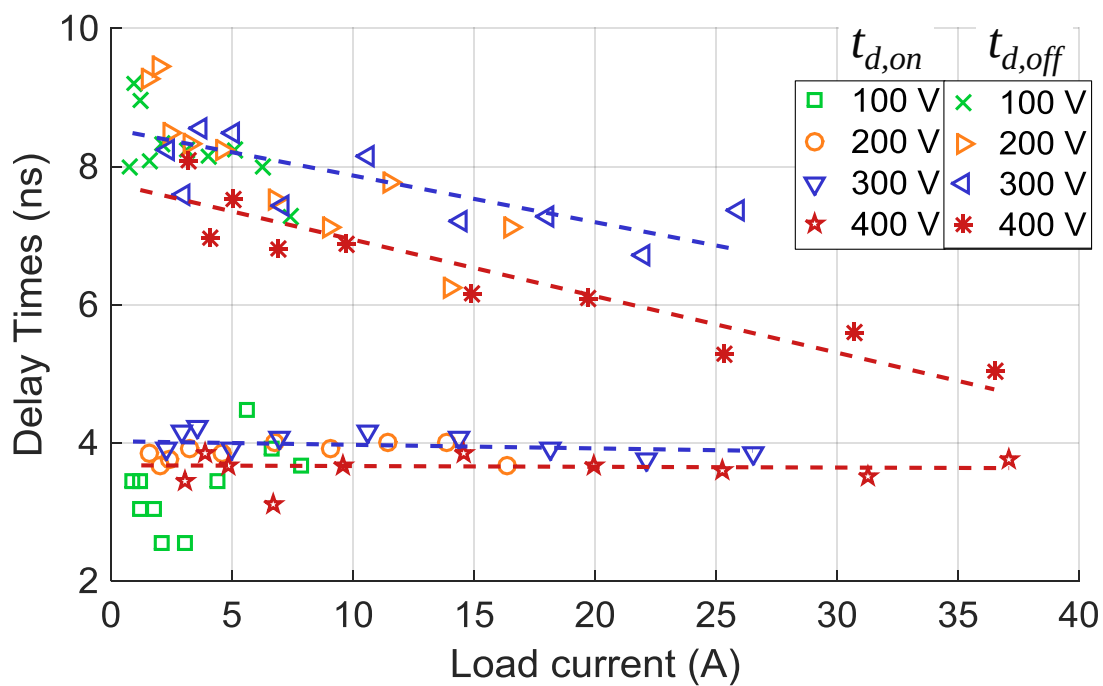


Figure 3.23. Switching delay times of GS66508P at 25 °C.

The gate loop inductance and resistance cause a v_{gs} overshoot at turn-on. In contrast with v_{ds} , the gate voltage overshoot is strongly correlated to junction temperature. Figure 3.24 shows this relationship. The overshoot exceeds the rated gate voltage in the light-load case, which could lead to long-term reliability issues, but only at an operating temperature below 50 °C. Reducing the driving voltage from 8 V to 7.5 V would bring the gate voltage overshoot down below the rated maximum, although this will also increase switching losses.

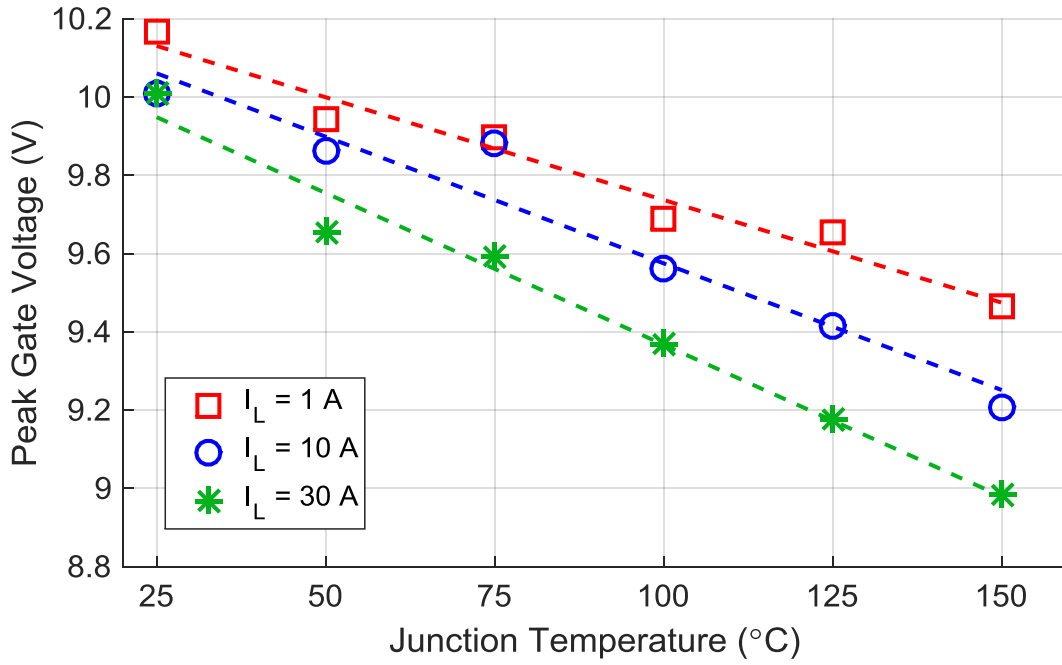


Figure 3.24. Gate-source voltage overshoot of GS66508P at 400 V.

3.3.6 Turn-Off Transient Analysis

Figure 3.25 shows the processed turn-off waveforms at 25 °C with 400 V dc bus voltage and 10 A load current. The turn-off delay times $t_{d,off}$ is defined to begin when gate voltage begins to decrease, detected based on the slope of the v_{gs} waveform. Likewise, the start of the current rise time t_{cf} was detected using the slope of the i_d waveform. The end of t_{cr} was detected based on the

zero-crossing of the i_d waveform. With a fast gate voltage transient such as this, the voltage rise transition is the same as the current fall transition, so t_{cf} and t_{vr} are equivalent.

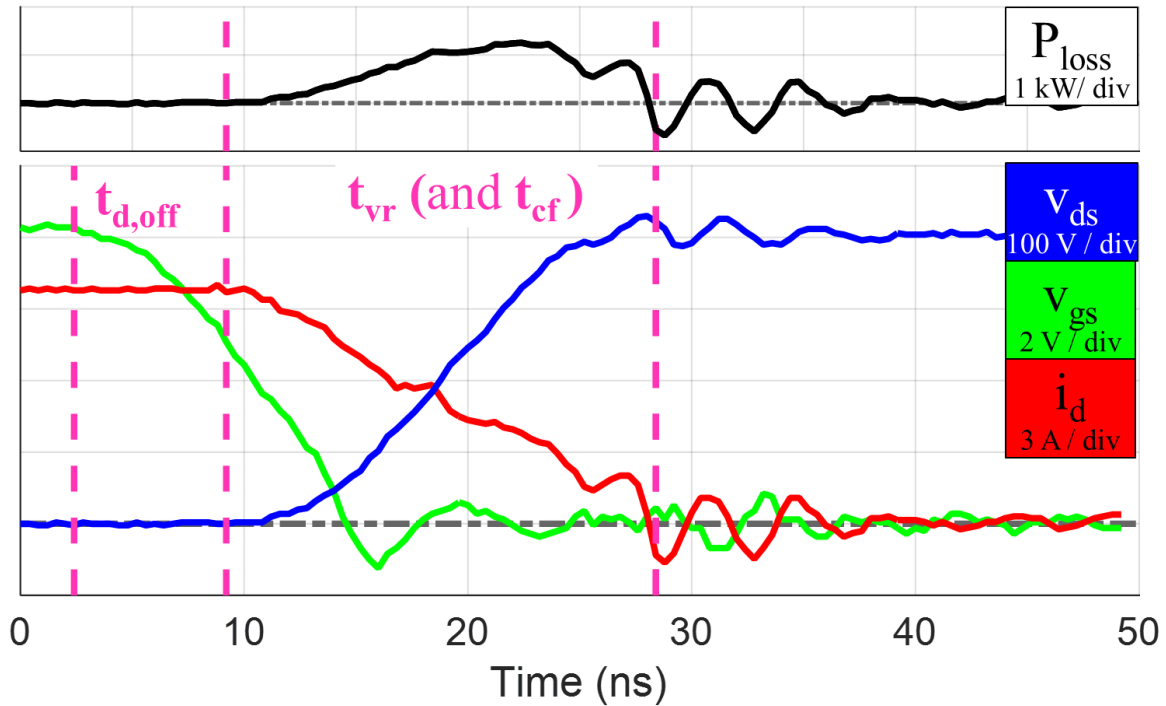


Figure 3.25. Turn-off waveform of GS66508P at 400 V, 10 A, 25 °C.

Similar to turn-on, the channel current can be calculated using these results so that Figure 3.26 can be generated to show the current in the active device channel.

Figure 3.27 shows the experimentally calculated turn-off times. Turn-off current fall time is strongly correlated to the inverse of load current, and is also slightly correlated to dc bus voltage. The turn-off delay was approximately 5-8 ns, showing a slight negative correlation with load current, and is shown in Figure 3.23.

It is well-known that the parasitic power loop inductance L_{ds} causes a drain-source voltage overshoot at turn-off. Figure 3.28 shows this voltage overshoot at 400 V over increasing load

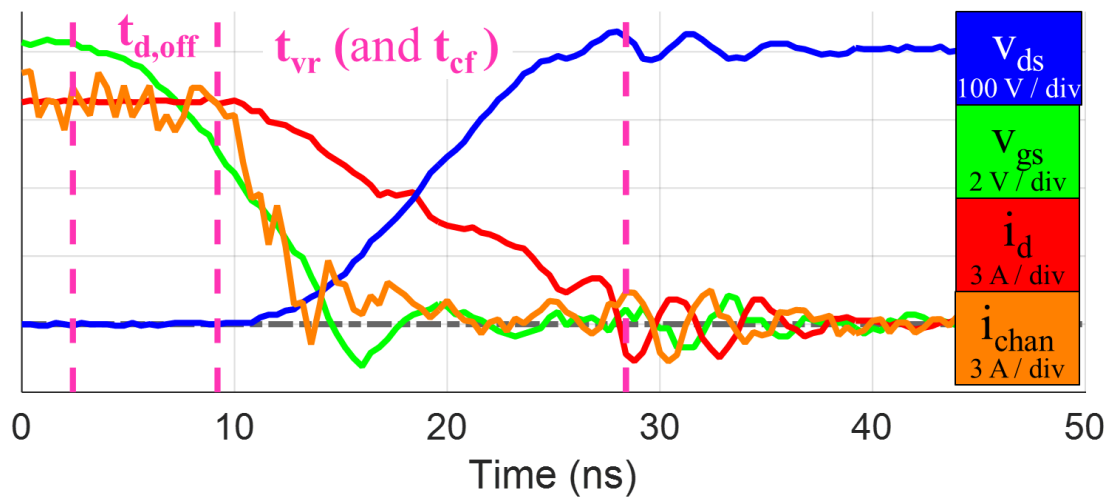


Figure 3.26. Turn-off waveform of GS66508P with calculated channel current at 400 V, 10 A, 25 °C.

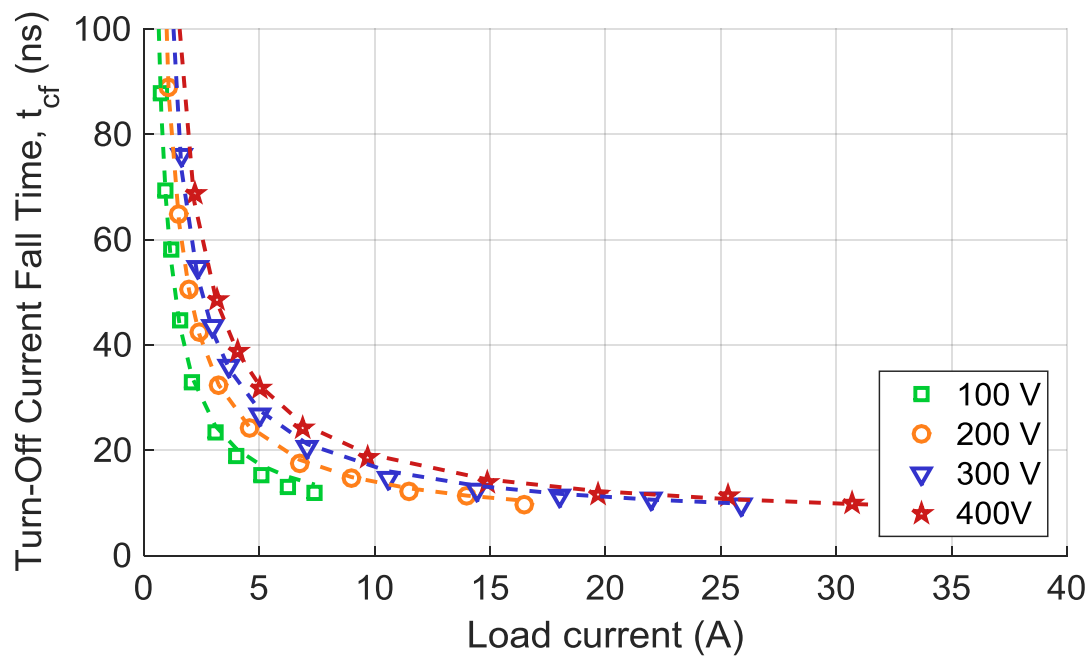


Figure 3.27. Turn-off current fall & voltage rise times of GS66508P at 25 °C.

current, which can be approximated well as a first-order relationship as shown with the dashed line. As mentioned previously, turn-off speed is not strongly proportional to temperature. Since this voltage overshoot is mainly due to the speed of the di/dt transient during turn-off, it is also not very temperature-dependent. The maximum voltage reached at 400 V operation and the rated load current of 30 A was 445 V, which is well within the voltage blocking capability of the device.

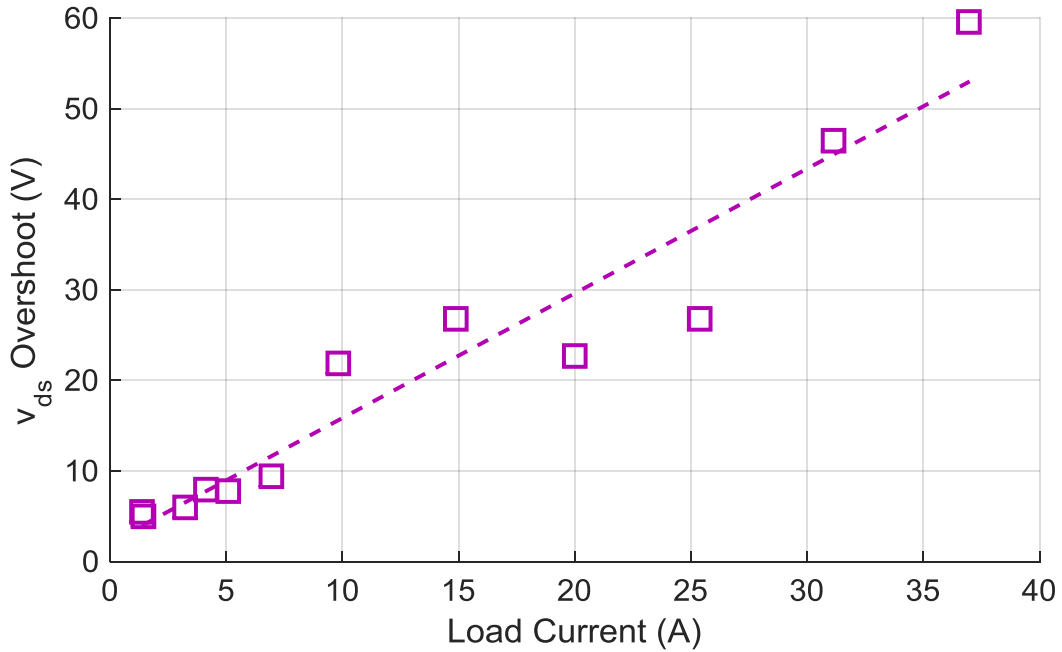


Figure 3.28. Drain-source voltage overshoot of GS66508P at 400 V.

3.3.7 Switching Losses

The turn-on energy E_{on} and turn-off energy E_{off} were calculated as the integral of power during t_{cr} and t_{vf} , and during t_{vr} , respectively, and are shown in Figure 3.29 and Figure 3.30. Both plots also show the theoretical no-load turn-on and turn-off loss, $E_{on,Coss}$ and E_{oss} , marked with asterisks on the y axis. These values were calculated as functions of V_{dc} , using (9) and (10), along with the measured C_{oss} curve in Figure 3.11.

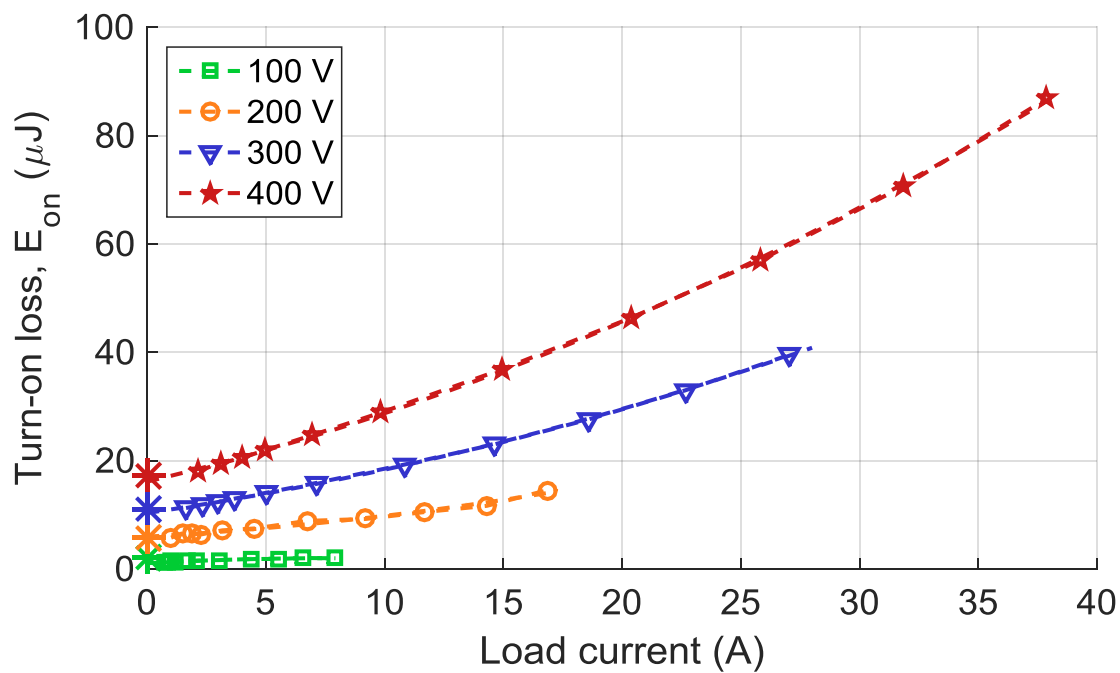


Figure 3.29. Turn-on energy of GS66508P at 25 °C.

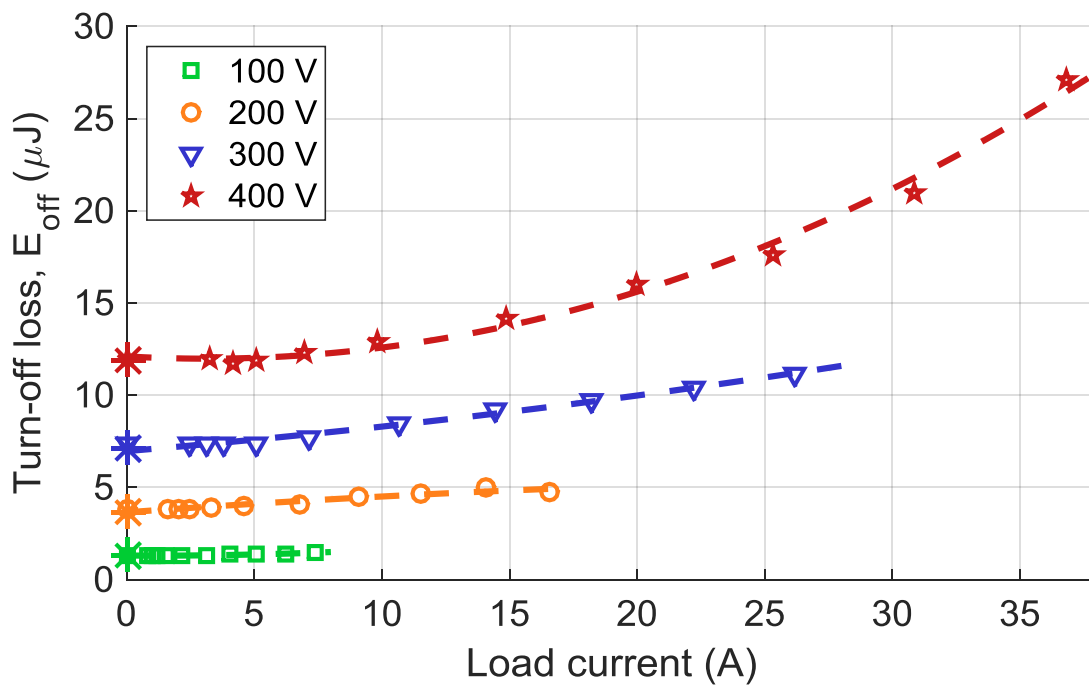


Figure 3.30. Turn-off energy of GS66508P at 25 °C.

$$E_{oss}(V_{dc}) = \int_0^{V_{dc}} [(C_{oss}(v) + C_{stray,active}) \times v] dv \quad (9)$$

$$E_{on,Coss}(V_{dc}) = V_{dc} \int_0^{V_{dc}} [C_{oss}(v) + C_{stray,sync}] dv - \int_0^{V_{dc}} [(C_{oss}(v) + C_{stray,sync}) \times v] dv \quad (10)$$

where $C_{stray,sync}$ and $C_{stray,active}$ are the stray capacitances of the board, components, and test setup associated with the synchronous device and active device, respectively [137].

The load-based trends at each tested dc bus voltage can be approximated well with second-order equations, shown with dashed lines in Figure 3.29 and Figure 3.30. Based on these trends, estimated E_{on} and E_{off} for a hard-switching converter can be calculated across the voltage and current range using (11) and (12) and the coefficients listed in Table 3.1 and Table 3.2.

$$E_{on} = k_1 I_L^2 + k_2 I_L + k_3 \quad (11)$$

$$E_{off} = k_4 I_L^2 + k_5 I_L + k_6 \quad (12)$$

Table 3.1. E_{on} Second Order Approximation Coefficients for GS66508P

Operating Conditions	k_1	k_2	k_3
400 V, 0-37 A	0.0223	1.0189	16.3105
300 V, 0-27 A	0.0162	0.6347	10.3635
200 V, 0-17 A	0.0131	0.2577	5.9747
100 V, 0-7 A	-0.0166	0.2505	1.0780

Table 3.2. E_{off} Second Order Approximation Coefficients for GS66508P

Operating Conditions	k_4	k_5	k_6
400 V, 0-37 A	0.0127	-0.0797	12.1061
300 V, 0-27 A	0.0018	0.1148	6.9711
200 V, 0-17 A	-0.0014	0.0992	3.6516
100 V, 0-7 A	0.0041	-0.0090	1.3076

In addition to the loss characterized here, the Miller cross-conduction phenomenon results in a shoot-through current through the phase leg, adding 5-10 μJ total losses in both devices. A gate resistance higher than 0 Ω will increase this shoot-through loss, unless an asymmetric gate drive with a diode in parallel with R_g is used, as explained in [133] and also later in this chapter.

As mentioned previously, the energy E_{oss} is stored in the active device's junction capacitor t_{vr} , then later lost inside the device during the following turn-on t_{vf} . However, in a soft-switching converter, the ZVS turn-on may recover that stored energy. However, the current and voltage overlap may still occur during the turn-off transient, and resistive loss may occur as a result. The overlap switching losses in a soft-switching converter can be estimated by subtracting E_{oss} from the hard-switching E_{off} , as given in

$$E_{off,soft-switching} = E_{off} - E_{oss} . \quad (13)$$

In addition to the board capacitances mentioned previously, dynamic testing indicated an additional stray capacitance of 30 pF from DPT components and the test setup.

3.3.8 Peak dv/dt

The peak dv/dt was calculated for the turn-on and turn-off transients, by calculating the slope of the voltage across every 0.4 ns sample of data and selecting the highest instantaneous slope during the transient. Figure 3.31 shows this calculated value at 25 $^{\circ}\text{C}$ across the measured voltage and current range.

The peak dv/dt is not as effective for measuring the switching speed as the turn-on and turn-off time presented previously. However, this calculation is an important parameter for selection of gate driving signal isolation. The isolator used in this work was only rated at 45 kV/ μs , but no CMTI problems were observed during testing. However, this may present more problems in long-term operation, because the dv/dt is shown to reach 200 kV/ μs .

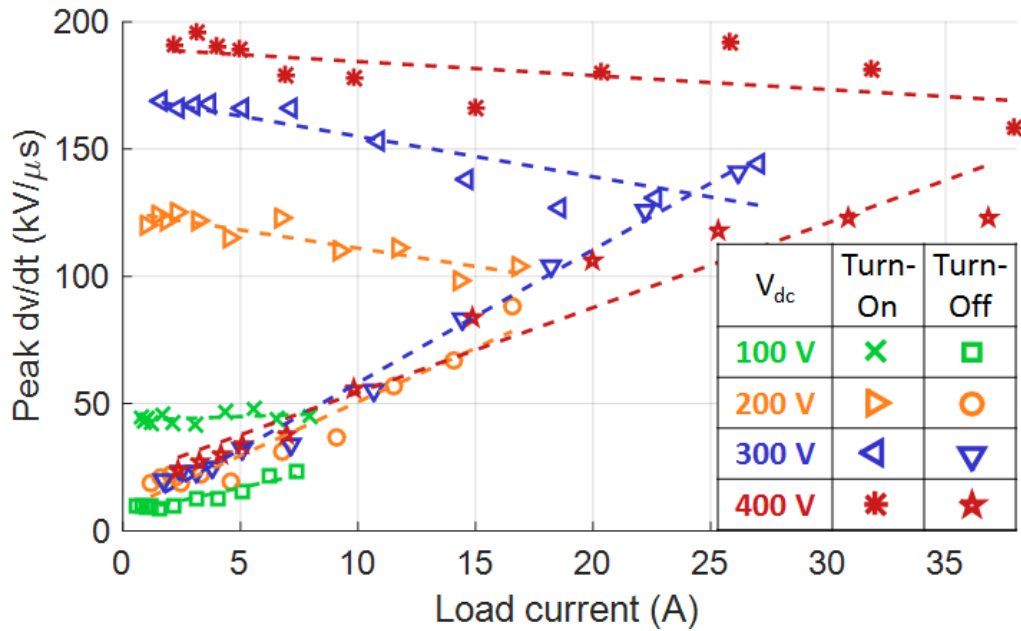


Figure 3.31. Peak dv/dt of GS66508P during turn-on and turn-off at 25 °C.

3.3.9 Observed Device Failures

Because the devices were tested beyond their rated limits for this characterization, several failure modes were observed. The most common failure was due to shoot-through overcurrent, caused by issues in the DPT board or test setup. With sufficient stored energy in the decoupling capacitors and insufficient overcurrent protection, this completely destroyed the device. With less stored energy or sufficient overcurrent protection, this only led to an electrical breakdown of the device and a partially burned package. In this case, all or most of the pins of the device were shorted together, including the drain, source, gate, and substrate. The measured resistance between any of these pins was less than 100 Ω .

The second most common failure mode was gate dielectric breakdown from electro-static discharge (ESD), caused by improper handling before or during soldering the device to the board. In this failure mode, the gate functioned as a diode with its voltage pulled down to ~ 0.3 V, and the

device was permanently turned off. However, the device could still conduct reverse current in SCRC operation.

Lastly, gate breakdown also occurred due to extended operation with v_{gs} at the maximum rated gate voltage of 10 V for several minutes. This did not seem to be a thermal breakdown, because the case temperature was measured with the board-mounted transducer and there was no noticeable temperature increase as the breakdown occurred. In this failure mode, the gate voltage was initially pulled low and the gate current increased dramatically, but the device could still effectively turn on and off. However, after some time with the increased gate current, all the pins were shorted together as in the overcurrent failure mode described previously. It was observed in continuous-run testing that the steady-state gate current significantly increased after several hours of testing, and eventually failed. The manufacturer has recently updated the datasheet for this device to specify the steady-state gate voltage rating at 7 V, and 10 V for pulsed gate voltage only. This new datasheet also recommends a driving voltage of 6 V, which will result in approximately the same on-resistance but larger switching loss. However, this reduction in driving voltage may be necessary to ensure the long-term reliability of the device.

3.3.10 Effects of Varying Gate Driver Voltage and Resistance

As previously mentioned, the recommended driving voltage for this device is between 6 and 7 V. Choosing a higher driving voltage of 8 V provides benefits in both turn-on and turn-off loss. For turn-on, increasing the driving voltage provides higher gate current during the entire turn-on transient, increasing turn-on speed and reducing E_{on} . The higher driving voltage also increases the peak gate current at the beginning of the turn-off transient, and the energy stored in the parasitic gate loop inductance L_{gs} provides a higher gate current during the Miller plateau. Therefore, the higher driving voltage reduces E_{off} as well, especially in the heavy load condition when the Miller plateau is longest. However, it should be noted that the manufacturer has recently modified the

device ratings, and the maximum driving voltage of 7 V would prohibit the 8 V driver. Instead, a voltage of 6 V is recommended, with a rated peak voltage of 10 V only for short pulses. This will lead to higher switching loss at turn-on and turn-off, but this design has not yet been comprehensively studied.

The preceding results assume 0 Ω external gate resistance, although the device includes an internal gate resistance of 1.5 Ω and the gate driver contributes an additional gate loop resistance (1 Ω for turn-on, 2.7 Ω for turn-off). Increasing the gate resistance causes additional switching losses, due to slower switching and also further cross-talk induced shoot-through. These results will be discussed in Section 3.4.

3.3.11 Effects of Elevated Temperature

The measured turn-on loss increased with elevated temperature, because of the reduced transconductance and saturation current indicated in Figure 3.7. Figure 3.32 shows a correlation

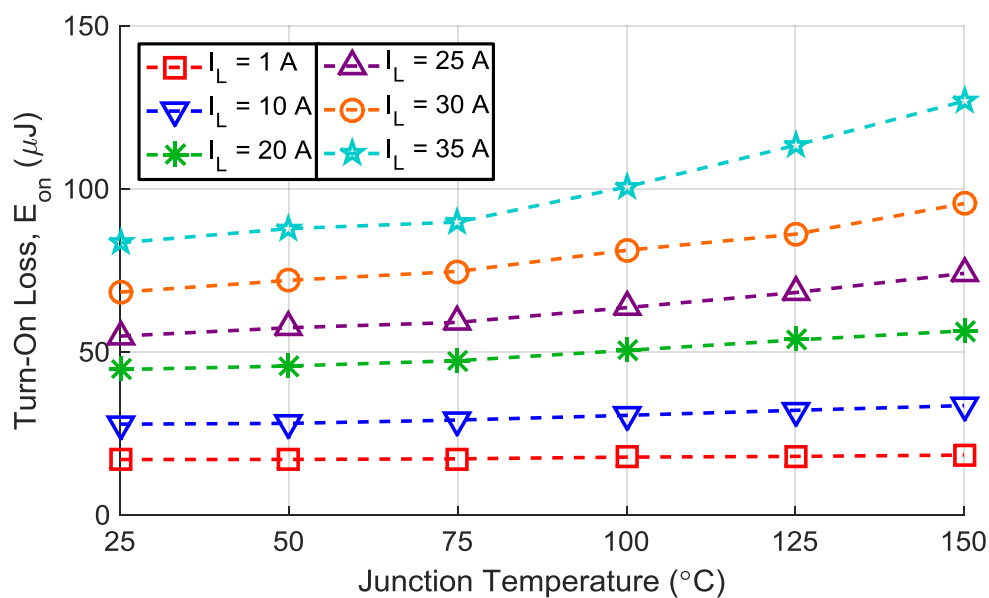


Figure 3.32. Turn-on energy of GS66508P at 400 V with elevated junction temperature.

with temperature that is stronger at higher load current. When the junction temperature is increased from 25 °C to 125 °C, the turn-on loss increases 5% at 1 A, 15% at 10 A, and 25% at 30 A. The positive temperature coefficient of turn-on loss has been previously demonstrated for other enhancement-mode GaN HFETs [41]. During the turn-on transient, the lower transconductance at elevated temperature makes the active device channel more resistive and therefore limits the displacement current through both output capacitances, increasing the turn-on time and loss. Turn-off loss did not show a strong correlation with temperature.

The effect of junction temperature on turn-on time and loss was analytically studied further, and will be discussed in the next chapter.

3.4 *Analysis of Cross-Talk*

Because cross-talk loss occurs in both devices of the phase leg, the losses are difficult to characterize with the conventional double pulse test setup. A comprehensive study of the cross-talk mechanism for this enhancement-mode GaN device was therefore performed to better predict overall switching losses, as well as a first step toward developing an improved gate driver in the future.

3.4.1 *Test Setup*

The current flowing through C_{gd} is proportional to the dv_{ds}/dt in both the active and synchronous devices. As previously mentioned, the turn-on speed and magnitude of dv_{ds}/dt is highest at light load, high dc bus voltage, and low temperature. Driving with 0 Ω gate resistance at 400 V, 25 °C, and 1 A results in a peak dv_{ds}/dt of 200 kV/ μ s. This study will focus on experimental results at 400 V and 25 °C, because these conditions produce the fastest switching and the worst case for cross-talk. The driving voltage was chosen as 7 V rather than 8 V for this study, because this testing was performed after the manufacturer changed the gate voltage ratings.

Three separate gate drive cases were studied for switching loss measurement in the active device. The results of these experiments were compared to estimate loss due to cross-talk as well as overall switching loss.

The circuit shown in Figure 3.33 (a) was used to measure the overlap and C_{oss} -based switching losses, with limited impact from cross-talk. For this case, the synchronous device gate and source sense terminals were shorted together directly at the device pads, which provides a low-impedance gate loop path for the C_{gd} displacement current to flow. Because of the internal device resistance and inductance, there may still be enough ringing on $v_{gs,int}$ to turn the synchronous device on, but this could be considered the “best case” for limiting cross-talk. However, it is not practical to use this design for a synchronous switching buck converter or phase-leg topology.

The circuit shown in Figure 3.33 (b) could be considered the “worst case” for cross-talk, because the same gate resistance was used for both turn-on and turn-off. This is generally not recommended for WBG devices, but it is still sometimes used for the sake of simplicity.

Finally, the circuit shown in Figure 3.33 (c) is the one recommended by the device manufacturer. It uses an asymmetric gate drive, with a discrete gate resistor for turn-on that is bypassed by a low-impedance Schottky diode in the turn-off path. This could be considered the “practical case,” because it allows the designer to mitigate cross-talk while still controlling the switching states of both devices.

The synchronous device in a phase leg is typically considered to operate in ZVS and experience no switching losses, but this is no longer true with the effects of cross-talk. Figure 3.34 allows for experimental analysis of the switching transients in the synchronous device. The same DPT board and test setup is employed, but the load inductor is connected to the low-side device rather than the high-side device, and the logic inputs to the high-side and low-side of the gate driver are reversed.

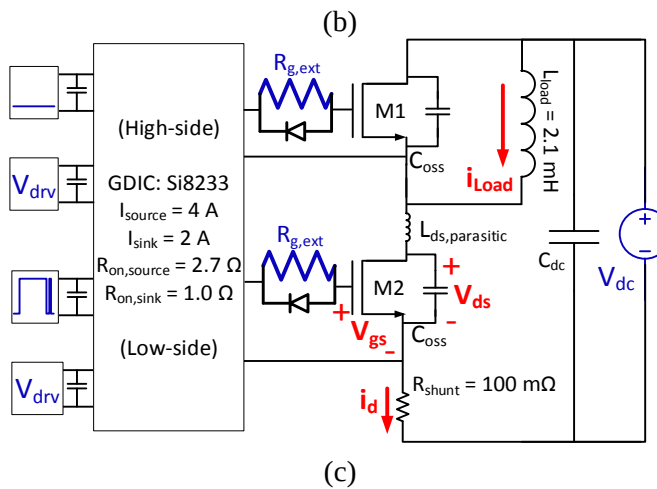
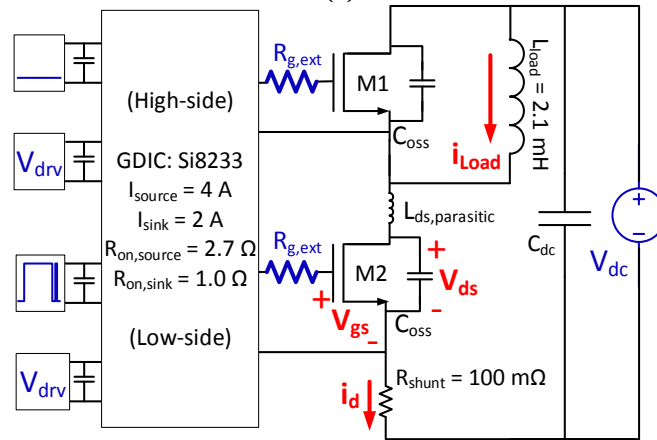
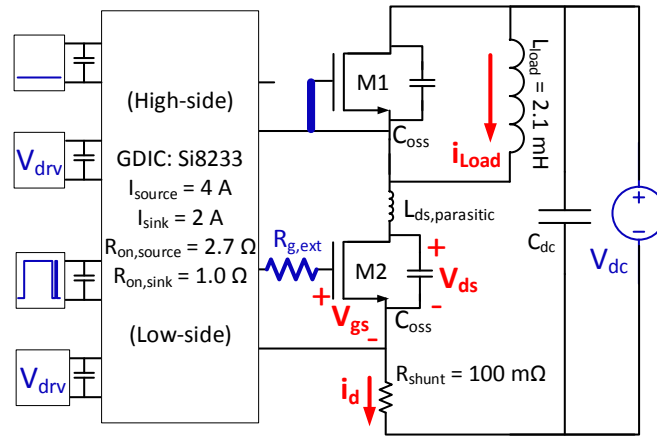


Figure 3.33. Double pulse test circuit schematic. (a) with limited cross-talk, (b) with worst-case cross-talk, (c) with asymmetric gate drive.

In this configuration, the synchronous device is the low-side device and therefore the device under test.

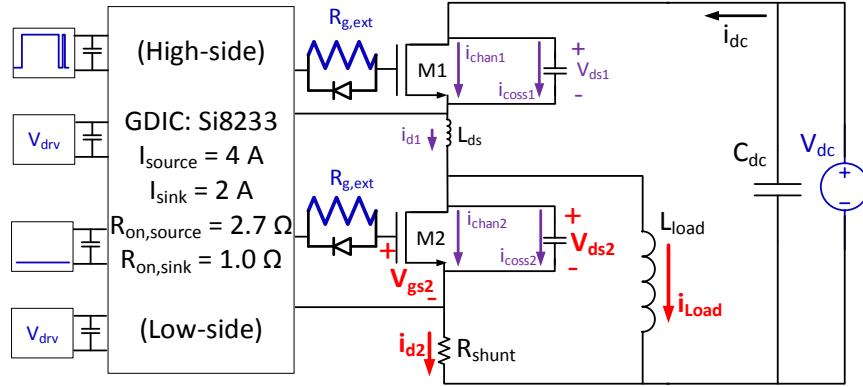


Figure 3.34. Double pulse test circuit schematic to measure synchronous device, with asymmetric gate drive.

3.4.2 Results for Active Device

The effect of cross-talk on the turn-on transient can be seen clearly in Figure 3.35 and Figure 3.36. Figure 3.35 compares the best case and the worst case with a gate resistance $R_{g,ext}$ of $10\ \Omega$, showing a longer turn-on time and a shoot-through current of about $20\ \text{A}$ in the worst case. Figure 3.36 compares the best case and practical case, showing very little effect from cross-talk with an asymmetric gate drive. However, the overall turn-on loss can still be greatly reduced by dropping the gate resistance to $0\ \Omega$. In this case, using an asymmetric gate drive is not necessary, since the $0\ \Omega$ resistance is the primary path for turn-on or turn-off and bypasses the Schottky diode completely.

As expected, the turn-on loss of the active device is correlated to both load current and gate resistance. This is true for all three of the cases described. Figure 3.37 shows the turn-on loss for the cross-talk best case, with the synchronous device gate-source input shorted. Figure 3.38 shows

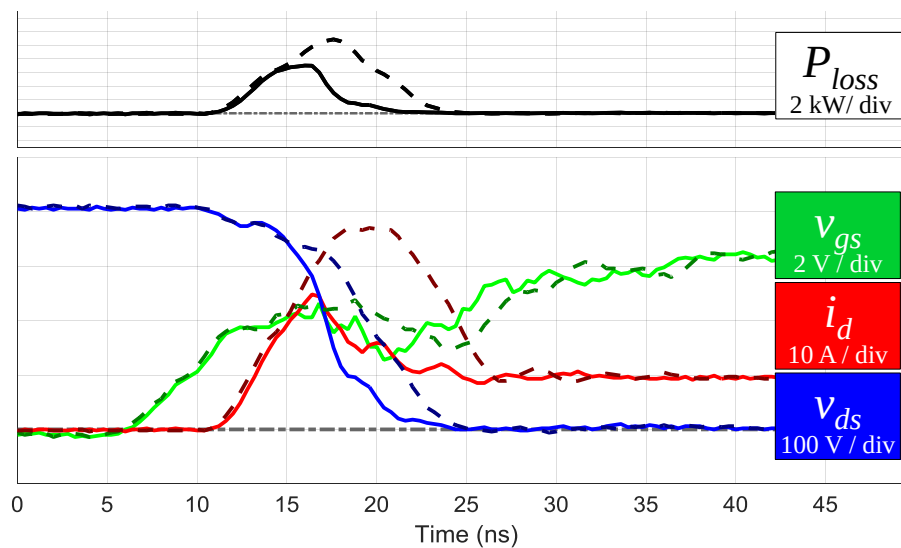


Figure 3.35. Turn-on transient waveforms of GS66508P at 400 V and 10 A with $R_{g,ext} = 10 \Omega$, showing the best case as a solid line and the worst case as a dashed line.

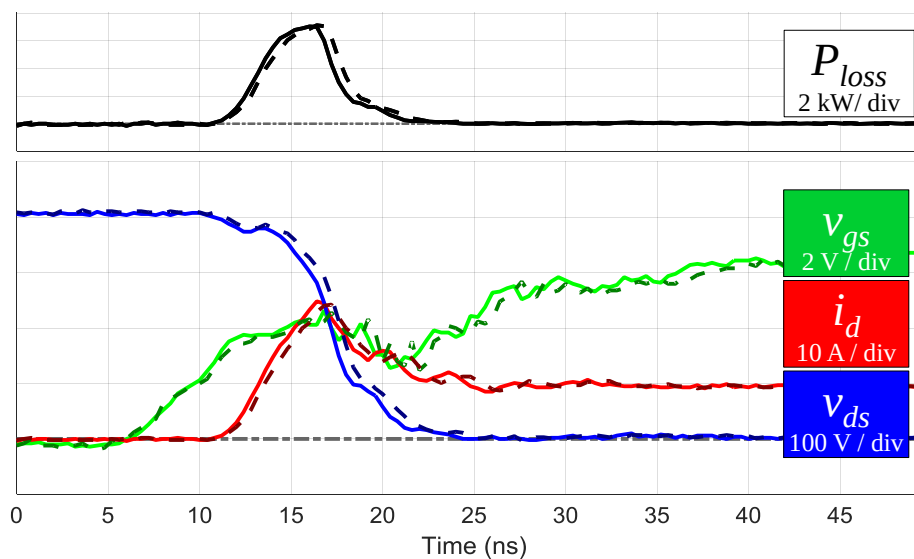


Figure 3.36. Turn-on transient waveforms of GS66508P at 400 V and 10 A with $R_{g,ext} = 10 \Omega$, showing the cross-talk best case as a solid line and the asymmetric drive case as a dashed line.

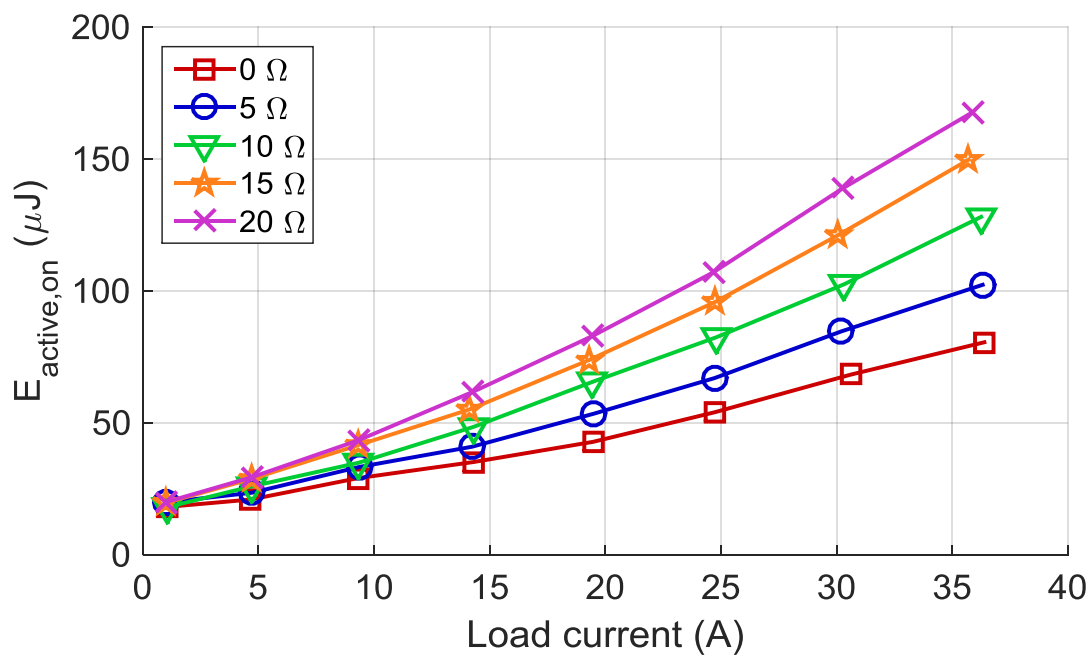


Figure 3.37. Turn-on loss of GS66508P for an active device, with the cross-talk best case gate drive circuit.

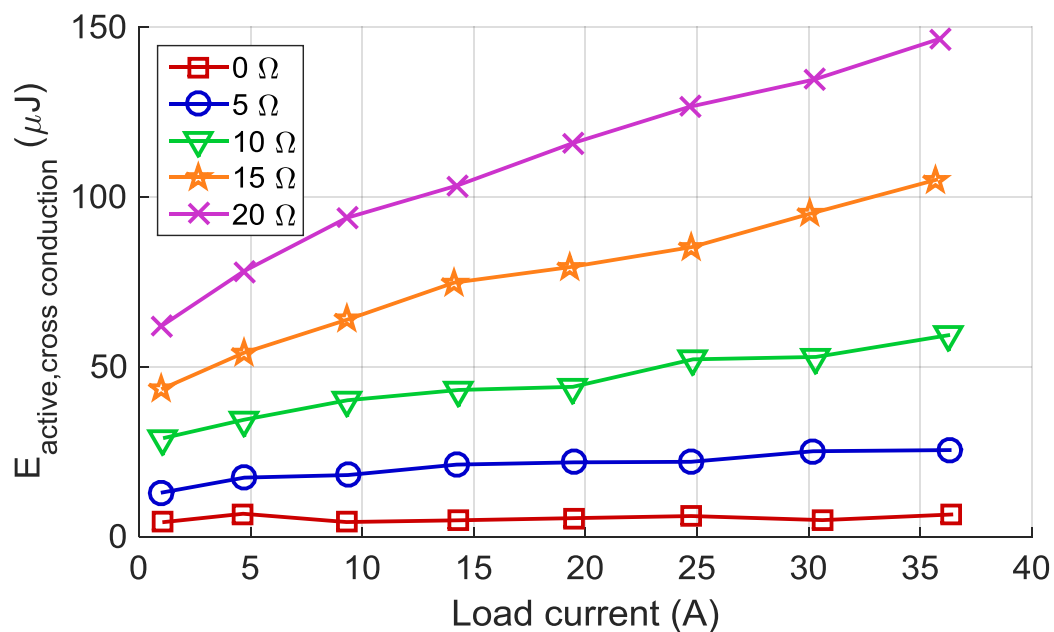


Figure 3.38. Additional turn-on loss of GS66508P due to cross-talk, with the cross-talk worst case gate drive circuit.

the additional turn-on losses caused by cross-talk with the worst case, estimated by subtracting the best case loss from the calculated worst case loss. These cross-talk losses become prohibitive with even as little as $5\ \Omega$ gate resistance. Part of this additional energy is lost as the shoot-through current flows through the saturated active device channel, and some additional energy is also lost, because the shoot-through current extends the turn-on transition and produces more I-V overlap loss.

Figure 3.39 shows the additional turn-on losses caused by cross-talk in the practical case, estimated by subtracting the best case loss from the calculated practical case loss. Unfortunately, Figure 3.39 does not show a clear trend of loss vs. gate resistance or load current. This calculation assumes that no spurious switching occurs in the best case, which may not be accurate due to ringing on the internal gate loop impedance. However, some general conclusions can be drawn. The results show that cross-talk losses with an asymmetric gate driver are approximately $5\ \mu\text{J}$ in the active device. An inverse correlation is expected between this loss and gate resistance, because the overall dv_{ds}/dt of both active and synchronous devices is strongly determined by the turn-on gate resistance of the active device. This is not obvious from the results shown in Figure 3.39, but some verification is provided in the synchronous device analysis presented in the next section.

Choosing a conventional (i.e. symmetric) gate drive circuit with a non-zero gate resistance also increases the turn-off loss, as shown in Figure 3.40. The active device turn-off loss with $0\ \Omega$ mostly consists of the energy stored in the device's output capacitance C_{oss} , but there is significant overlap loss as the turn-off gate resistance is increased. With an asymmetric gate drive, the turn-off loss is approximately the same as the $0\ \Omega$ case in Figure 3.40, because the Schottky diode provides a very low impedance path for turn-off gate current. Considering turn-on, turn-off, and cross-talk losses in the active devices, the $0\ \Omega$ gate resistance case clearly results in the lowest losses by a significant margin. However, the cross-talk losses in the synchronous device must also be considered.

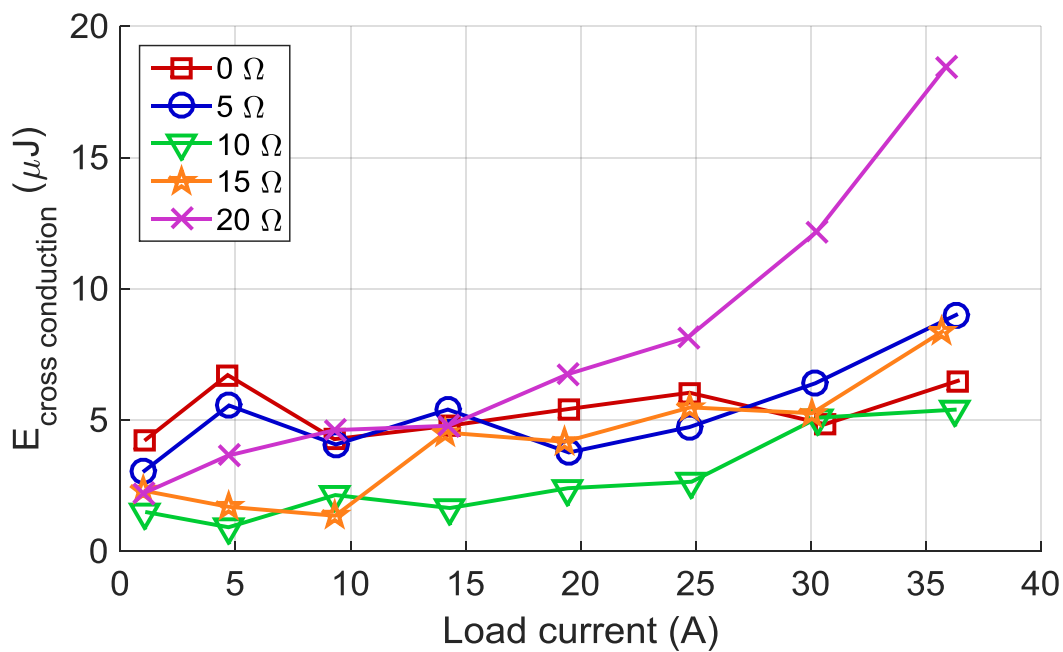


Figure 3.39. Additional turn-on loss of GS66508P due to cross-talk, with the practical case using an asymmetric gate drive.

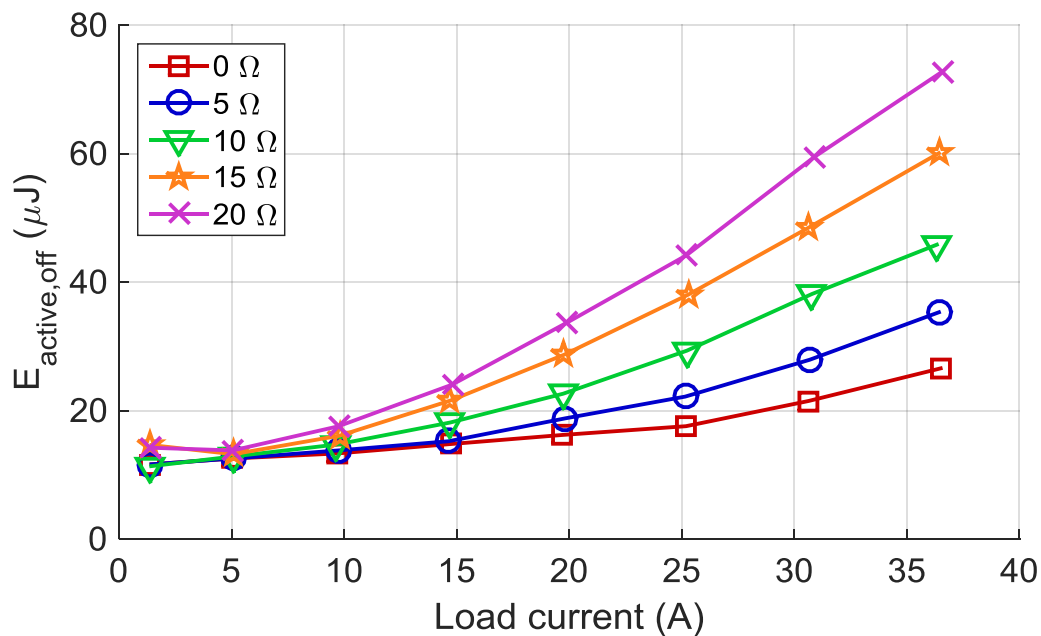


Figure 3.40. Turn-off loss of GS66508P for an active device in the cross conduction best case.

3.4.3 Results for Synchronous Device

Figure 3.41 shows the measured energy lost to the synchronous device during the turn-on of the active device, as well as the energy recovered from the synchronous device during the active device turn-off transient. Because the synchronous device switching transitions are ZVS, there should be no overlap losses and the speed of the turn-on and turn-off should not impact the switching energy in either case. However, it is clear from Figure 3.42 that there is at least 5 μJ of additional turn-on loss due to cross-talk with 0 Ω case, and nearly none with the asymmetric 20 Ω gate driver. The turn-on transients with 0 Ω and asymmetric 20 Ω drivers are compared in Figure 3.42. The asymmetric 20 Ω driver produces a much longer turn-on time and loss, but it is difficult to ascertain how much the shoot-through current is reduced. A shoot-through current waveform can be approximated by subtracting the calculated internal displacement current $C_{oss}dv_{ds}/dt$, but the excessive ringing makes this approach less effective.

There is also a mechanism causing loss during the active device turn-off transient, thereby preventing the energy in the synchronous device from being fully recovered. This mechanism is not clear from the experiments performed in this study. There may be some energy displaced in the junction capacitances of the device and lost in the saturated device channel during the turn-off transient. However, this may be a result of a measurement issue.

After the turn-off dv_{ds}/dt transient is over, some additional energy is lost due to cross-talk in the 5-20 ns following the transient. The C_{gd} displacement current in the synchronous device induces a negative gate voltage for a short time after the turn-off transient, and the magnitude of this negative v_{gs} increases with higher gate resistance and higher load current. It is interesting to note that this negative spurious voltage occurs after the dv_{ds}/dt transient, not during the transient as

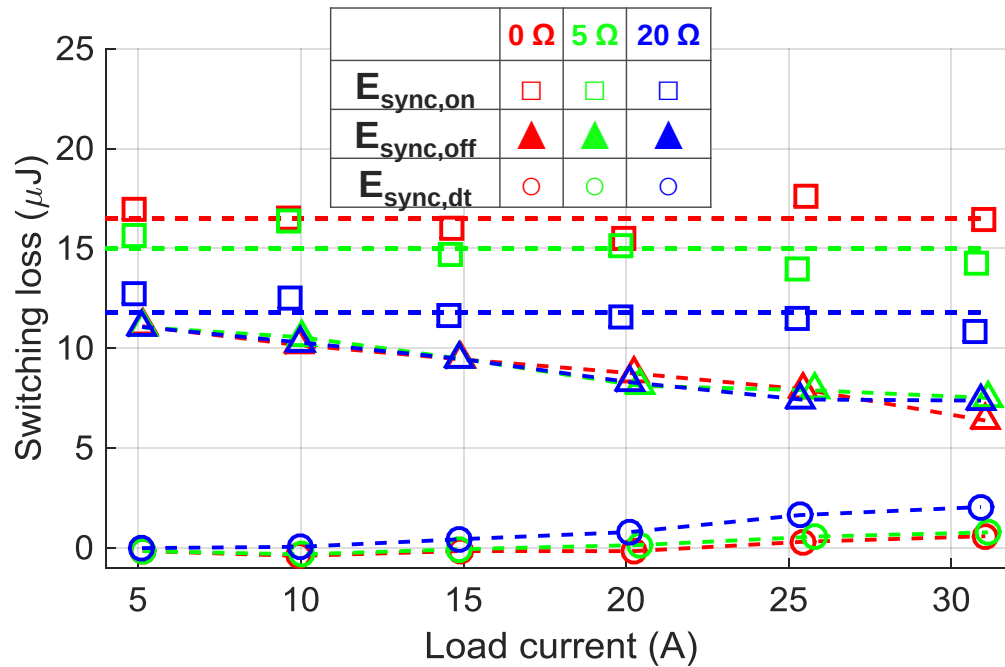


Figure 3.41. Synchronous device energy with GS66508P, including energy lost during active device turn-on dv/dt , energy recovered during active device turn-off dv/dt , and energy lost during dead time following active device turn-off.

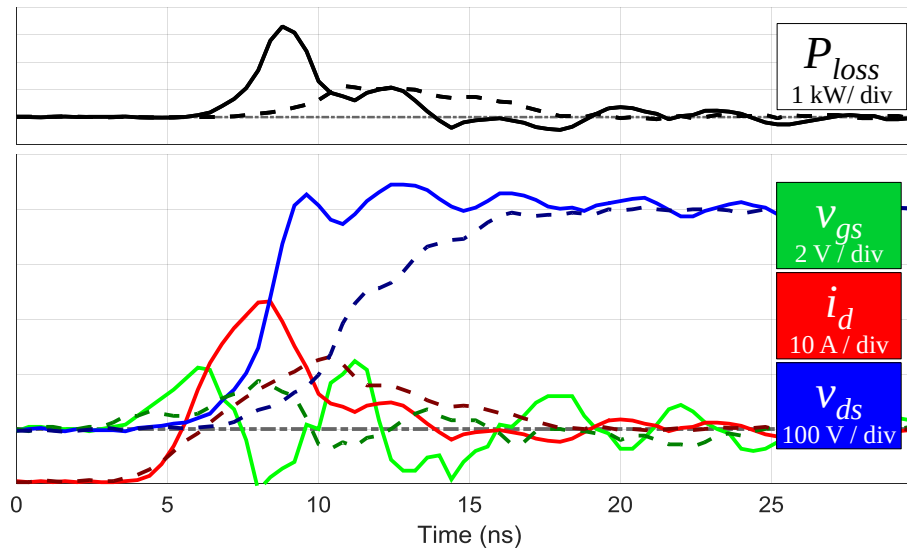


Figure 3.42. Synchronous device transient waveforms for GS66508P, during active device turn-on at 400 V and 10 A with an asymmetric gate drive circuit, showing $R_{g,\text{ext}} = 0 \Omega$ with a solid line and $R_{g,\text{ext}} = 20 \Omega$ with a dashed line.

is typical for cross-talk . The alignment of i_d , v_{ds} and v_{gs} measurements was re-checked to verify this phenomenon, and found to be correct. The nature of this spurious negative gate voltage requires further investigation, but the effect is clear. Figure 3.43 compares the turn-off transient waveforms with $0\ \Omega$ and $20\ \Omega$, showing a negative gate voltage of about $-10\ \text{V}$ in the $20\ \Omega$ case with $10\ \text{A}$ load current. As explained previously, the forward voltage drop during SCRC (“body diode”-like operation) is approximately equal to the sum of the internal gate voltage, the Miller voltage, and the drop across the channel resistance $R_{ds,on}$. The conduction loss during the dead time following turn-off will thus increase with higher gate resistance and load current, shown in Figure 3.41 as $E_{sync,dt}$.

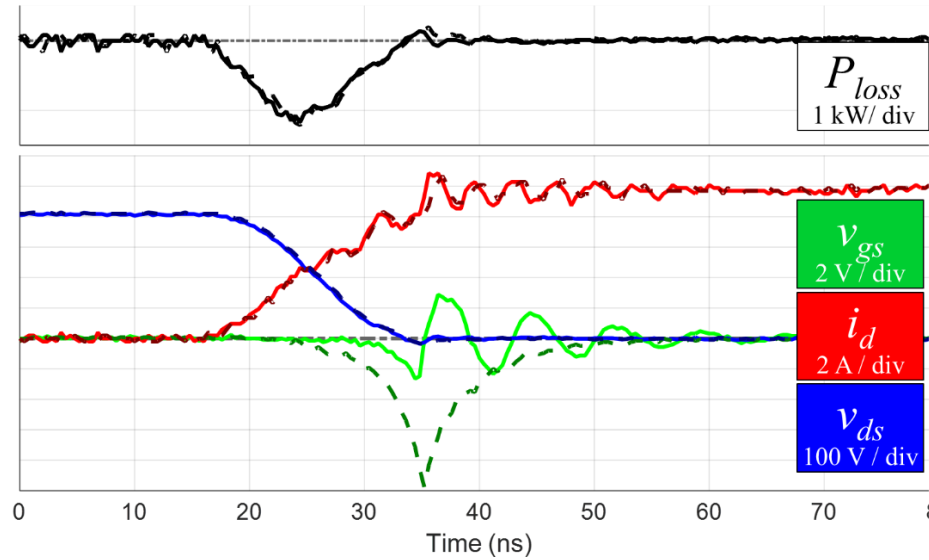


Figure 3.43. Synchronous device transient waveforms for GS66508P, during active device turn-off at $400\ \text{V}$ and $10\ \text{A}$ with an asymmetric gate drive circuit, showing $R_{g,ext} = 0\ \Omega$ with a solid line and $R_{g,ext} = 20\ \Omega$ with a dashed line.

Turn-off cross-talk can be mitigated with a second diode in the gate drive circuit, connected directly between the source sense and gate terminals to provide a low-impedance path in parallel with C_{gs} during the turn-off transient. This will also add parallel capacitance between the gate and

source and slow down the turn-on transient as well, and this tradeoff must be considered before implementing this option.

3.5 *Summary*

The static and dynamic characteristics of a 650-V enhancement-mode GaN devices were experimentally measured and presented here. The forward and reverse output characteristic, transfer characteristic, and gate current were presented over a range of voltages, currents, and junction temperatures. The junction capacitances were determined experimentally or derived from published datasheet curves.

The turn-on and turn-off transients were also studied for this device. A range of load currents and bus voltages were studied, with a focus on 7 V and 8 V based on the published device ratings at the time of experimentation. Best-fit equations for switching losses were presented, for both hard switching and soft switching topologies. Other useful results include the durations of switching transient subintervals, such as turn-on and turn-off delay times, turn-on current rise time, turn-on voltage fall time, and turn-off voltage fall time. The drain and gate overvoltages were presented, as well as peak dv/dt for noise and EMI purposes. Lastly, the impact of elevated temperature on these results was briefly explored, although this will be covered more thoroughly in the next chapter.

In further study of the switching losses due to cross-talk for an enhancement-mode device, a range of gate resistances was studied with three different driver circuits. It is clear that a conventional gate drive circuit with non-zero gate resistance is not an effective option for this device, due to heavy overlap and cross conduction losses during both turn-on and turn-off transients. An asymmetric gate drive circuit presents an alternative, with reduced cross conduction losses at turn-on and overlap losses at turn-off. However, the turn-on overlap loss is still increased significantly with higher gate resistance. An asymmetric gate drive with 20 Ω of turn-on gate

resistance may reduce overall cross conduction loss by 5-10 μJ when compared to a conventional gate drive circuit with 0 Ω . However, this adds as much as 80 μJ at the full rated load. Based on these experimental results, an asymmetric gate drive circuit with 5-10 Ω may be appropriate for light load applications below 10 A. However, this only results in approximately the same overall losses, and not a significant reduction. This design will also lower the peak dv_{ds}/dt during turn-on, which will be helpful in preventing spurious switching events due to interference in the signal path. However, it should be noted that since the time of this testing, the rated driving voltage has dropped from 10 V to 7 V, and the recommended voltage is now 6 V. With that lower driving voltage, the tradeoff for cross-talk loss and overall switching loss will be slightly different from what was presented here.

In conclusion, this device performed well in terms of switching speed and loss, and exhibited typical trends of both static and dynamic performance over voltage, current, and temperature conditions. The repeated failures due to gate rupture and graduate gate dielectric breakdown are concerning, but the maximum gate voltage rating from the manufacturer was reduced to 7 V after most of this testing was complete, and the recommended driving voltage of 6 V may help mitigate or eliminate this issue. Lastly, the very fast switching transients lead to more stringent requirements on the gate drive circuit, including both cross-talk immunity and common-mode transient immunity. Although these phenomena can be easily mitigated by operating the devices with a lower switching speed than their maximum capability, this can also be seen as an opportunity to improvement in gate driver design for high-speed devices.

Chapter 4

Model Development

4.1 *Introduction*

Although the e-mode GaN HFET is similar to a MOSFET, its switching behavior must be considered carefully in order to accurately analyze the experimental results. Therefore, a simplified model was developed to understand the turn-on and turn-off transients. Although this simplified model is not intended for simulation, the equations can be used to better understand and interpret experimental results. The model is aimed at understanding and explaining some of the trends and properties that were discovered during the characterization process, and are not explained by the conventional model of a MOSFET.

As such, equations for the internal device voltages and currents were developed for the subintervals of a turn-on and turn-off transient. These equations, however, do not consider the gate loop inductance, which will cause additional resonance during each subinterval, especially in the gate voltage waveform. It also does not fully consider the impacts of the load inductance and stray inductances in the power loop, except for the initial drop in voltage during turn-on.

Two specific features of the device were also considered here. First, the consequences of the Miller effect on the turn-on transient were analyzed, because the assumption of a simple Miller plateau was not observed in the experimental results. Second, a method to scale turn-on losses with elevated temperature was developed, based on room temperature E_{on} and static characterization data.

4.2 *Subcircuit Model*

The subcircuit model shown in Figure 4.1 was developed by overlaying the internal junction capacitances, parasitic capacitances, and channel resistance from Figure 2.12 on the physical device structure shown in Figure 2.5. Because the source and substrate are externally

connected for the device considered here, $C_{s,sub}$ can be neglected and $C_{d,sub}$ can be lumped with C_{ds} . $R_{ds,on}$ is treated as a series resistance in addition to the channel resistance represented by i_{chan} , because it primarily represents the drift region resistance along the 2DEG. This structure was also supported by measurement with a precision impedance analyzer.

The field plate structure of the device will heavily impact the characteristics of the junction capacitances. Figure 2.10 shows an example of such field plates. However, the exact structure for these field plates is unknown for the device considered here, so they are not shown in the subcircuit model.

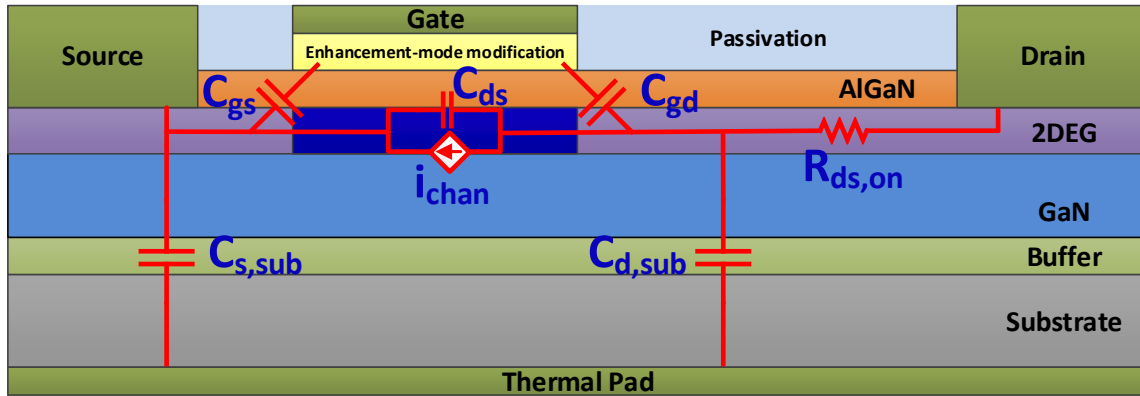


Figure 4.1. Subcircuit model for an enhancement-mode GaN HFET.

4.3 Turn-On Transient Behavior

The typical turn-on transient for a phase leg with GaN HFETs or other fast-switching devices is shown in Figure 4.2, with the current paths for each subintervals shown with arrows.

Initially, the load current flows through the synchronous device, either in a body diode, antiparallel diode, or the GaN diode-like reverse channel (SCRC) as shown in Figure 4.2 (a). This stage continues until the active device gate voltage reaches its threshold, and the active device

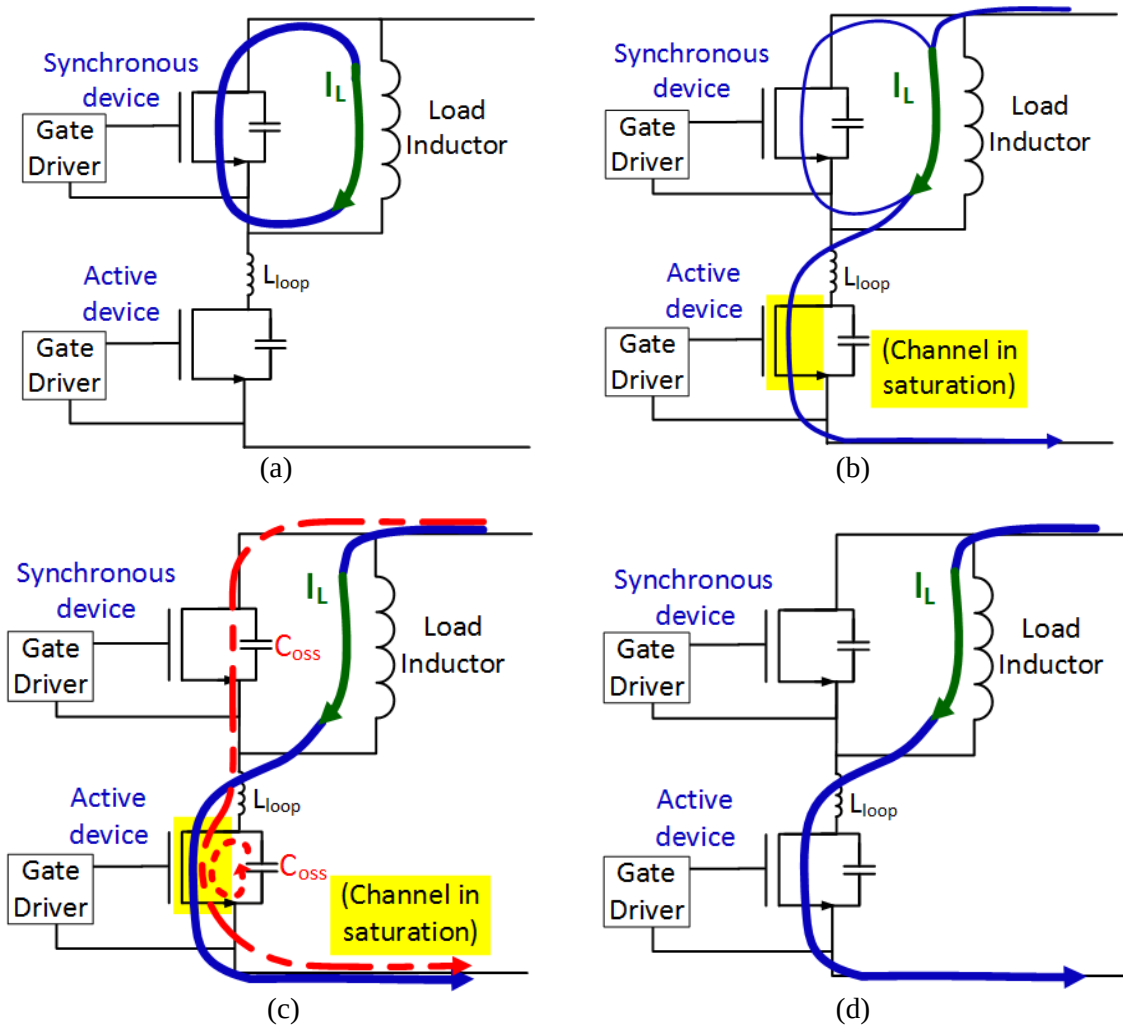


Figure 4.2. Current in a phase leg during a hard turn-on transient with fast-switching devices.
 (a) Before turn-on transient and during turn-on delay time; (b) During current rise time; (c) During voltage fall time; (d) After turn-on transient is complete.

channel begins to conduct in the saturation region. During this turn-on delay time, the gate voltage, channel current, drain current, and drain-source voltage can be described by

$$v_{gs} = \int \left[\frac{(V_{drv} - v_{gs})}{(R_{g,int} + R_{g,ext})C_{iss}} \right] dt \quad (14)$$

$$i_{chan} = 0 \text{ A} \quad (15)$$

$$i_d = 0 \quad (16)$$

$$v_{ds} = V_{dc} \quad (17)$$

Once the gate voltage reaches the threshold voltage, the device turns on in the saturation region, and the drain current begins to rise. At this time, the load current commutates from the synchronous device to the active device. The voltage on the synchronous device is clamped to zero, so it cannot begin to block any voltage yet. The parasitic power loop inductance L_{loop} blocks some of the dc voltage during this subinterval. With a dense board design, this drop should be relatively small compared to V_{dc} . During this current rise time, the gate voltage, channel current, drain current, and drain-source voltage can be described by

$$v_{gs} = \int \left[\frac{(V_{drv} - v_{gs})}{(R_{g,int} + R_{g,ext})C_{iss}} + \left(\frac{C_{rss}}{C_{iss}} \right) \left(\frac{dv_{ds}}{dt} \right) \right] dt + V_{th} \quad (18)$$

$$i_{chan} = g_{fs}(v_{gs} - V_{th}) = K(v_{gs} - V_{th})^2 \quad (19)$$

where K is a physical constant of the device determined experimentally.

$$i_d = i_{chan} + C_{oss,active} \frac{dv_{ds}}{dt} \quad (20)$$

$$v_{ds} = V_{dc} - L_{loop} \frac{di_d}{dt} \quad (21)$$

Once the current is fully commutated to the active device channel, the synchronous device turns off and can block dc voltage, so the voltage fall time begins. This point is also defined as the moment when v_{gs} reaches the Miller voltage, although there may be a small difference due to the discharge of the active device's output capacitor into its channel. During the voltage fall time shown in Figure 4.2 (c), the output capacitance in the active device is discharged into its saturated channel,

and this energy is lost. Simultaneously, the output capacitance of the synchronous device is charged with current from the dc bus and decoupling capacitors, and this displacement current flows through the saturated active device channel and incurs additional loss. Here, the gate voltage, channel current, and drain current can be described by (18)-(20), but the drain-source voltage is now given by

$$v_{ds} = V_{dc} - L_{loop} \frac{di_d}{dt} - \int \left(\frac{i_{chan} - I_L}{C_{oss,active} + C_{oss,sync}} \right) dt \quad (22)$$

where $C_{oss,active}$ and $C_{oss,sync}$ are the output capacitances of the two devices at the instantaneous voltage of each, because they are highly nonlinear.

The gate voltage is conventionally assumed to be constant during this subinterval, but the Miller plateau can be avoided with fast-switching devices and effective gate driver design. Further analysis on the Miller effect interactions in (18) and (22) during the voltage fall time will be discussed later in this chapter.

In a MOSFET phase leg, there will also be a reverse recovery current from the synchronous body diode during this time, but an e-mode GaN HFET has zero reverse recovery, so this can be ignored. A cascode GaN HFET will still experience some reverse recovery due to the Si device on the gate, but an antiparallel Schottky diode can eliminate reverse recovery in this case.

Another important factor in the voltage fall time is the shoot-through current across the phase leg induced by the Miller effect in the synchronous device, shown in Figure 4.3. The mechanism causing cross-talk in the synchronous device was discussed in Chapter 2 and shown in Figure 2.12. Chapter 3 also experimentally demonstrated the impact of cross-talk on turn-on loss. For analysis of the turn-on transient behavior, it is necessary to understand that the current in the active device channel due to cross-talk will be equal to the total current through the synchronous device as its channel turns partially on. Because the total active channel current is determined by the gate voltage, the shoot-through current will reduce the channel current available for

displacement of the two output capacitors as shown in Figure 4.3. Considering this new channel current component, (22) becomes

$$v_{ds} = V_{dc} - L_{loop} \frac{di_d}{dt} - \int \left(\frac{i_{chan} - I_L - i_{shoot-through}}{C_{oss,active} + C_{oss,sync}} \right) dt . \quad (23)$$

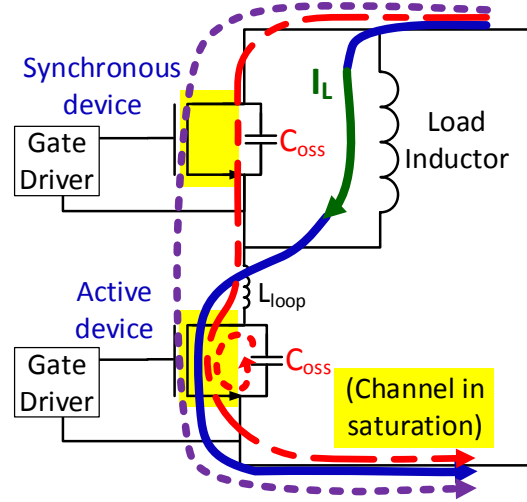


Figure 4.3. Impact of cross-talk on voltage fall time in a phase leg, showing the induced shoot-through current with a purple dashed line.

The current $i_{shoot-through}$ can be determined by the induced gate voltage on the synchronous device, as in

$$i_{shoot-through} = K(v_{gs,sync} - V_{th})^2 \quad (24)$$

$$v_{gs,sync} \approx V_n + (R_{g,int} + R_{g,ext,off} + R_{pd})C_{gd,sync} \frac{dv_{ds,active}}{dt} \quad (25)$$

where V_n is the negative supply voltage on the synchronous device gate drive (typically 0 V), $R_{g,int}$ is the device's internal gate resistance, $R_{g,ext,off}$ is the external gate resistance of the turn-off path, and R_{pd} is the pull-down on-resistance of the gate driver IC. This equation neglects the impact of

the gate loop inductance, which may be significant in this case. However, for the purposes of describing general turn-on transient behavior, this is sufficient.

Once the switch-node voltage reaches $i_{chan}R_{ds-on}$, the device falls into the Ohmic region as shown in Figure 4.2 (d), and the turn-on transient is generally complete. However, there may be some ringing between the junction capacitances and parasitic loop inductances as the switch-node voltage settles to $I_L R_{ds-on}$. This ringing is not analyzed in depth here, because the experimental results presented earlier have shown that the net energy losses during this time are very small.

Figure 4.4 shows the theoretical turn-on waveforms divided into these subintervals. The lightly shaded area shows the charge associated with displacement current in the output capacitors of the two devices, $q_{oss,active}$ and $q_{oss,sync}$, which contribute a fixed amount of turn-on energy loss for a given dc voltage, regardless of load current or temperature. These losses are given by

$$E_{on,Coss,sync} = \int_0^{V_{dc}} C_{oss,sync}(v) \times (V_{dc} - v) dv \quad (26)$$

$$E_{on,Coss,active} = \int_0^{V_{dc}} C_{oss,active}(v) \times v dv . \quad (27)$$

These equations are essentially the same as (9) and (10) given earlier, with the only difference being the variable names and accounting for stray capacitances. The area with hatched shading in Figure 4.4 shows the charge associated with conduction of the load current through the saturated channel during the turn-on transient, which contributes energy loss that is dependent on the time duration of the transient. This loss is considered overlap loss, and can be manipulated with gate drive design. Some simplified equations for this overlap loss will be discussed later in this chapter.

Although the consequences of charging the synchronous device output capacitor are considered here, the actual energy deposited into $C_{oss,sync}$ is not. The losses described by (26) and (27) both occur in the resistive channel of the active device. The energy stored in the synchronous

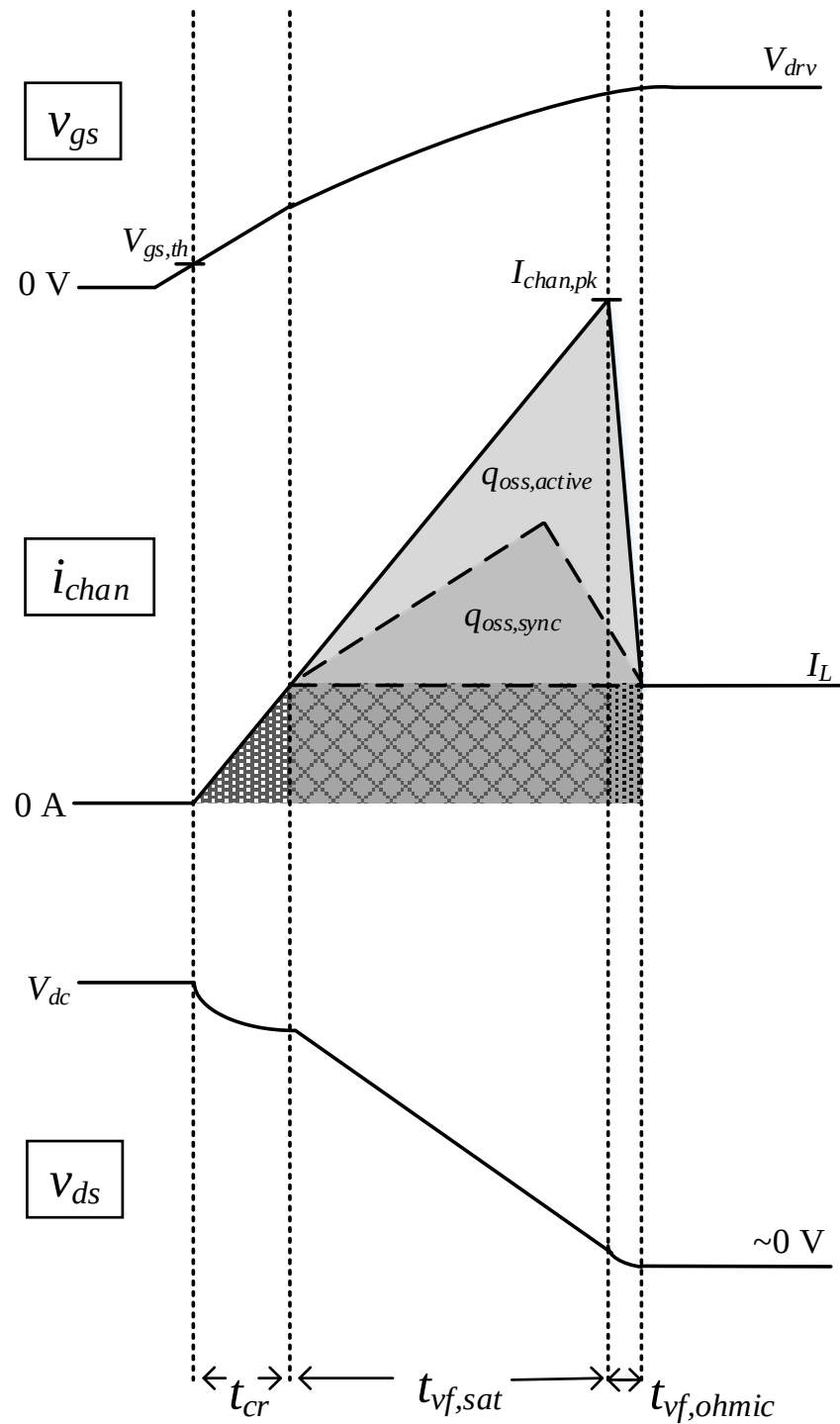


Figure 4.4. Theoretical turn-on transient waveforms of active device.

device as it begins to block voltage should typically be recovered during the following turn-off transient, so it is not typically considered a component of phase leg switching losses. The turn-on energy loss E_{on} is conventionally defined as the sum of the overlap losses and (26), because the energy loss of (27) can only be seen experimentally during the turn-off transient.

It is important to note that during this transient, the term V_{drv} represents the voltage at the output of the gate driver, which is not a constant. In a fast-switching device, the rise time of the driver may be longer than the turn-on delay time and affect the gate voltage during multiple subintervals. Also, the on-resistance of the pull-up resistor continues to limit the gate driver current even after the rise time is complete. A simplified driver voltage model may assume a constant ramp rate during the pull-up rise time, then beyond that time, the driver voltage will be

$$V_{drv} = V_p - i_g R_{pu} \quad (28)$$

where V_p is the positive supply voltage on the driver and R_{pu} is the on-resistance of the pull-up transistor, generally given in the driver datasheet.

4.4 Turn-Off Transient Behavior

The turn-off transient is often described as the opposite of the turn-on transient, but there is a significant difference between the two. In a turn-off transient, the channel can be pinched off completely before the end of the transient, whereas in turn-on, the channel must remain in the saturation region for the duration of the transient. The load current displaces charge between the active and synchronous device output capacitors. Because of the directions of the load current and displacement currents, the conductive channel in parallel with the output capacitors actually slows down the turn-off transient, thereby causing the turn-off overlap losses. This means that a fast gate driver can nearly eliminate all overlap losses during the turn-off transient and avoid any Miller plateau from occurring by pinching off the channel before the dv/dt is significant.

Figure 4.5 shows the subintervals involved in the turn-off transient of a phase leg. In Figure 4.5 (a), the load current continues to flow through the active device channel, as the gate voltage drops from the driving voltage to the Miller voltage. Here, the gate voltage is given by

$$v_{gs} = V_p - \int \left[\frac{(v_{gs} - V_{drv})}{(R_{g,int} + R_{g,ext})C_{iss}} \right] dt \quad (29)$$

and this turn-off delay time continues until v_{gs} reaches the Miller voltage, when the device enters the saturation region. This Miller voltage is given by

$$V_{Miller} = \frac{I_L}{g_{fs}} + V_{th} = \sqrt{\frac{I_L}{K}} + V_{th} . \quad (30)$$

Once the gate voltage reaches the Miller voltage, the device channel becomes more resistive than R_{ds-on} , and the load current begins to commute to the two parallel output capacitors of the active and synchronous devices. Figure 4.5 (b) shows this subinterval. Because neither capacitor is clamped by a diode or Ohmic channel, this allows both the voltage rise time and current fall time to occur simultaneously. During this time, the gate voltage can be described by

$$v_{gs} = \int \left[\frac{(V_{drv} - v_{gs})}{(R_{g,int} + R_{g,ext})C_{iss}} + \left(\frac{C_{rss}}{C_{iss}} \right) \left(\frac{dv_{ds}}{dt} \right) \right] dt + V_p \quad (31)$$

and the currents can be described by (19) and (20). Based on the channel current, the drain-source voltage can then be described by

$$v_{ds} = \int \left(\frac{I_L - i_{chan}}{C_{oss,active} + C_{oss,sync}} \right) dt - L_{loop} \frac{di_d}{dt} . \quad (32)$$

During this time, the portion of the load current that flows through the saturated channel causes resistive energy loss. However, the energy deposited into the active device output capacitor is not truly lost here. It is conventionally considered part of E_{off} , but this energy is resistively lost in the turn-on transient and is given by (27).

With a slow gate driver or heavy load, the entire voltage rise time may be described by this subinterval. However, because of the low input capacitance of GaN HFETs, the saturated channel

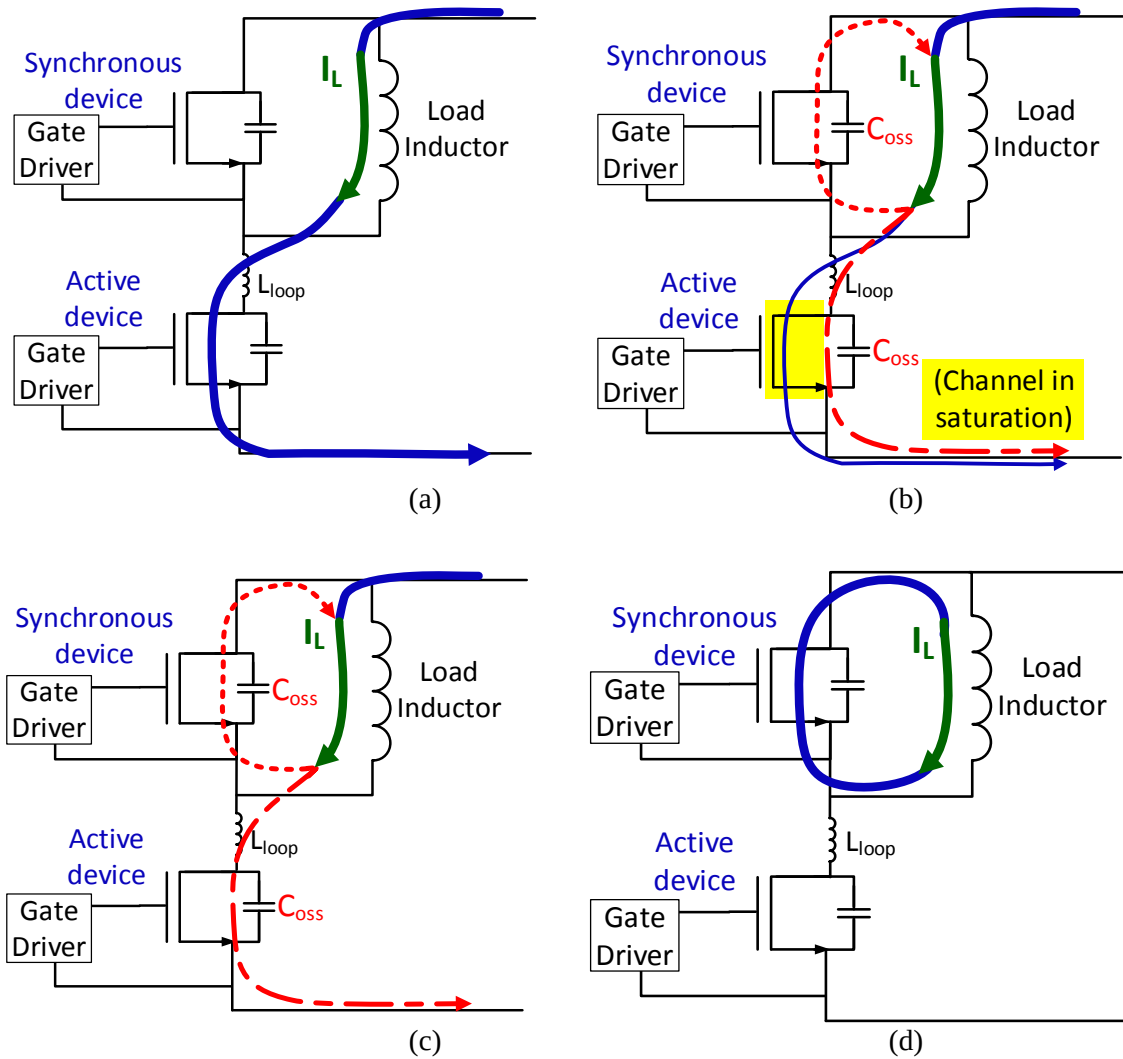


Figure 4.5. Current in a phase leg during a hard turn-off transient with fast-switching devices. (a) Before turn-off transient and during turn-off delay time; (b) During current fall and voltage rise time, while channel is turning off; (c) During current fall and voltage rise time, after channel is fully off; (d) After turn-off transient is complete.

will actually pinch off much earlier than the displacement of output capacitor charge. Once v_{gs} falls below the threshold voltage, the transient continues as shown in Figure 4.5 (c). The same equations (31), (20), and (22) describe this second part of the voltage rise and current fall time, but the channel current is now 0 A, so dv_{ds}/dt increases as the full load current acts to displace output capacitor charges. Because no further resistive losses can occur, only lossless displacement occurs here, including the energy stored in $C_{oss,active}$ given in (27), as well as the recovery of the energy stored in $C_{oss,sync}$.

After the charge displacement is complete, the voltage rise time and current fall time are over, and the full load current flows into the synchronous device, either in a body diode or in the GaN's diode-like SCRC mode. It should also be noted that during the ringing that occurs after voltage rise time, v_{ds} may overshoot V_{dc} because of the load inductance L_{loop} . This is true for Si and SiC devices as well, but there is an interesting distinction for the GaN HFET. As opposed to a true body diode, the GaN SCRC mode can support a momentary reverse voltage, if a negative voltage spike occurs on the synchronous device v_{gs} . Unless the gate driver is designed to prevent it, the Miller effect may cause such a spike to occur, and the v_{ds} overshoot experienced by the active device will be

$$v_{ds,overshoot} = -\left(v_{ds,sync} + L_{loop} \frac{di_d}{dt}\right). \quad (33)$$

It is important to consider the nonlinear output capacitance is when analyzing the turn-off transient. At the beginning of the transient, the total switch-node capacitance is relatively high, since the synchronous device has a low drain-source voltage. Therefore, the dv_{ds}/dt is initially quite low. The voltage drop across the resistive channel can potentially remain very low, as long as it pinches off before v_{ds} increases enough for the switch-node capacitance to fall. If this condition is met, the turn-off overlap loss can be nearly zero.

4.5 Analysis of the Miller Effect During the GaN HFET Turn-On Transient

4.5.1 Introduction

The Miller effect is a well-known phenomenon in three-terminal power devices, including the cross-talk discussed previously, as well as the Miller plateau in turn-on and turn-off transients. The term “Miller plateau” describes the seemingly flat point in the gate voltage waveform during the dv_{ds}/dt of either turn-on or turn-off transients. The cause for this effect is the Miller capacitance C_{gd} , the capacitance shared by the gate loop and power loop, which causes a negative feedback on the changing gate voltage. It was mentioned earlier in this chapter that the turn-off Miller plateau can be avoided at turn-off with a fast gate drive. However, the turn-on Miller effect cannot accurately be described as a plateau for fast-switching devices. The effect of C_{gd} on dv_{gs}/dt is important to consider for fast-switching devices such as GaN, but it should be treated as a finite change in slope rather than a plateau. This section derives a model to explain the interaction and determine the severity of the Miller effect on gate voltage during turn-on.

4.5.2 Derivation of Turn-On Gate Voltage with Miller Effect

Figure 4.6 (a) shows the equivalent circuit of the active device during the turn-on voltage fall time, neglecting the power loop inductance for this analysis. Since there is no reverse recovery in e-mode GaN HFETs, that component can also be neglected. Figure 4.6 (b) shows a further simplified version of this circuit.

Analysis of this equivalent circuit leads to

$$i_{chan} - I_L = C_{gd} \frac{dv_{gs} - dv_{ds}}{dt} - (C_{ds,act} + C_{oss,sync}) \frac{dv_{ds}}{dt} \quad (34)$$

which can be reduced to

$$g_{fs}(v_{gs} - V_{Miller}) = -(C_{oss,act} + C_{oss,sync}) \frac{dv_{ds}}{dt} + C_{gd} \frac{dv_{gs}}{dt} . \quad (35)$$

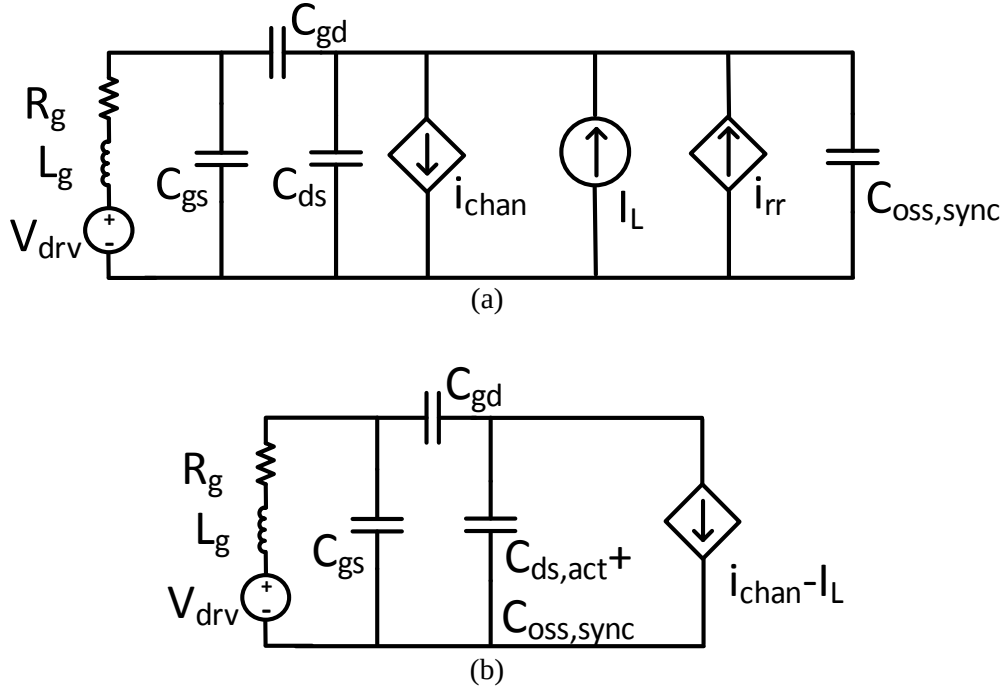


Figure 4.6. Equivalent circuit of active device during turn-on voltage fall time, (a) Detailed model including reverse recovery, (b) Simplified model with no reverse recovery.

Because of the relative magnitudes of dv_{ds}/dt and dv_{gs}/dt as well as the junction capacitances, the C_{gd} term can be neglected, leading to a relationship between gate-source voltage and drain-source voltage given by

$$\frac{dv_{ds}}{dt} \approx \frac{-g_{fs}(v_{gs} - V_{Miller})}{C_{oss, act} + C_{oss, sync}}. \quad (36)$$

Substituting (36) into (18), the rate of change of gate voltage can be approximated as

$$\frac{dv_{gs}}{dt} \approx \frac{V_{drv} - v_{gs}}{R_g C_{iss}} - \left(\frac{C_{rss}/C_{iss}}{C_{oss, act} + C_{oss, sync}} \right) g_{fs}(v_{gs} - V_{Miller}). \quad (37)$$

The first term in this expression represents the voltage supplied by the gate driver, and the second term represents the feedback current due to the Miller effect. In general, this feedback can produce a Miller plateau, if the magnitude of the second term is always greater than the first term. In such a case, the gate voltage is clamped very near to the Miller voltage. If v_{gs} falls below the

Miller voltage, the polarity of this term reverses, and the gate voltage increases above it again. However, this will cause the turn-on transient to be very long, since the channel current is locked near to the load current, and there is very little excess channel current available to displace the output capacitance charges.

For the GaN device considered in this analysis, C_{rss} is relatively low for most of the turn-on transient, until v_{ds} falls below 50 V. The magnitude of the second term is therefore much lower than the first, and the gate voltage continues to rise at a somewhat reduced rate. Then, when C_{rss} increases at low voltage, the second term is much greater than the first, and the gate voltage falls quickly until the device enters the Ohmic region of operation.

4.5.3 Verification with Experimental Results and Simulation

To verify that the equations given in this section, particularly (37), accurately model the turn-on voltage fall time of an enhancement-mode GaN device, turn-on transient waveforms were generated using discrete-time calculations in MATLAB for several operating conditions. Then, the resulting waveforms were compared against simulation and experimental results.

These equations noticeably neglect the effects of inductance in the gate loop, as mentioned previously. For this discrete-time calculation, the power loop inductance was also neglected during the voltage fall time, but it is considered during the current rise time, where it causes an initial drop in v_{ds} . This change was made to eliminate resonance, so that the equations would iteratively converge.

For comparison, the operating conditions were chosen as 400 V, 10 A, and 25 °C, with a positive driver supply voltage of 7 V and pull-up resistance of 2.7 Ω based on the experimental setup. The constant K was chosen as 7, based on static characterization results for g_{fs} . Figure 4.7, Figure 4.8, and Figure 4.9 show the results with an external gate resistance of 0 Ω , 20 Ω , and 100 Ω , respectively. The driver voltage has a 5 ns rise time. With a low external gate resistance, the driver

voltage continues to be pulled down somewhat by the on-resistance R_{pu} when the gate current is high. However, with a higher external gate resistance, the relative drop on R_{pu} is small compared to $R_{g,ext}$, so the driver voltage stays mostly constant after the rise time is finished.

During the voltage fall time, the gate voltage shown in green is affected by the Miller feedback term as expected. In Figure 4.7, the slope of v_{gs} is only reduced slightly, until v_{ds} reaches 50 V and the Miller feedback causes v_{gs} to momentarily drop near to the Miller voltage. Then, the device enters the Ohmic region of operation, and v_{gs} continues to rise again. In Figure 4.8, the Miller effect is more prominent in its effect on v_{gs} , and in the extreme case of Figure 4.9, a Miller plateau occurs. The gate voltage remains nearly constant around the Miller voltage of 2.8 V.

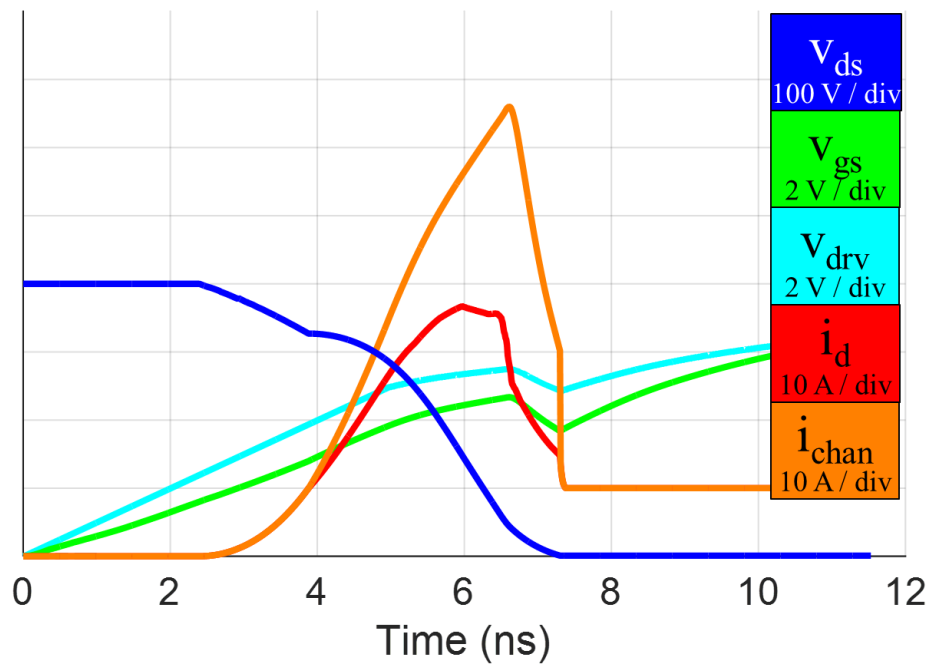


Figure 4.7. Calculated waveforms at 400 V, 10 A, with $R_{g,ext} = 0 \Omega$.

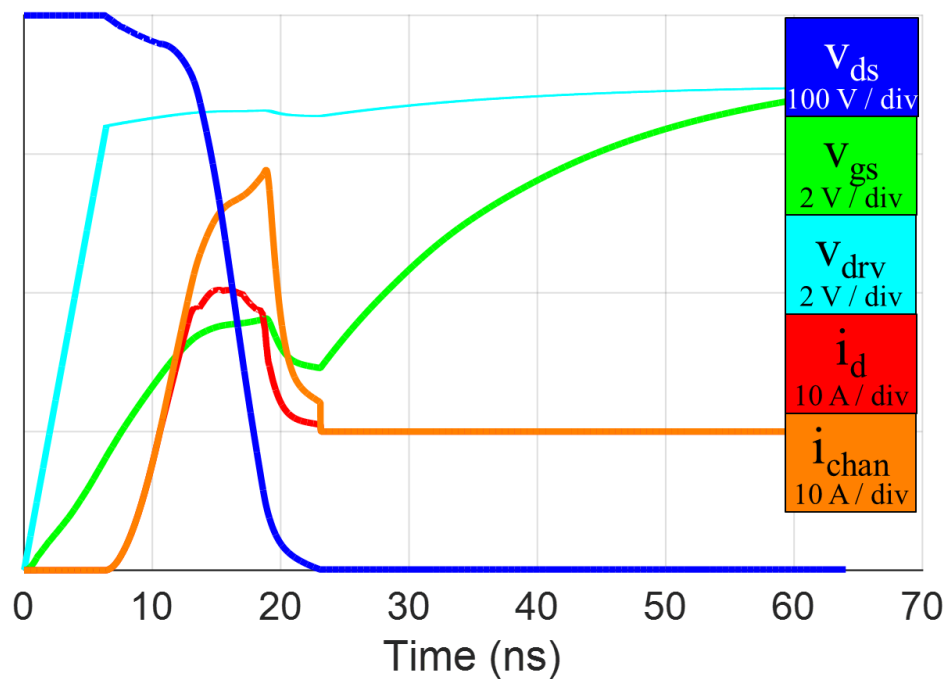


Figure 4.8. Calculated waveforms at 400 V, 10 A, with $R_{g,ext} = 20 \Omega$.

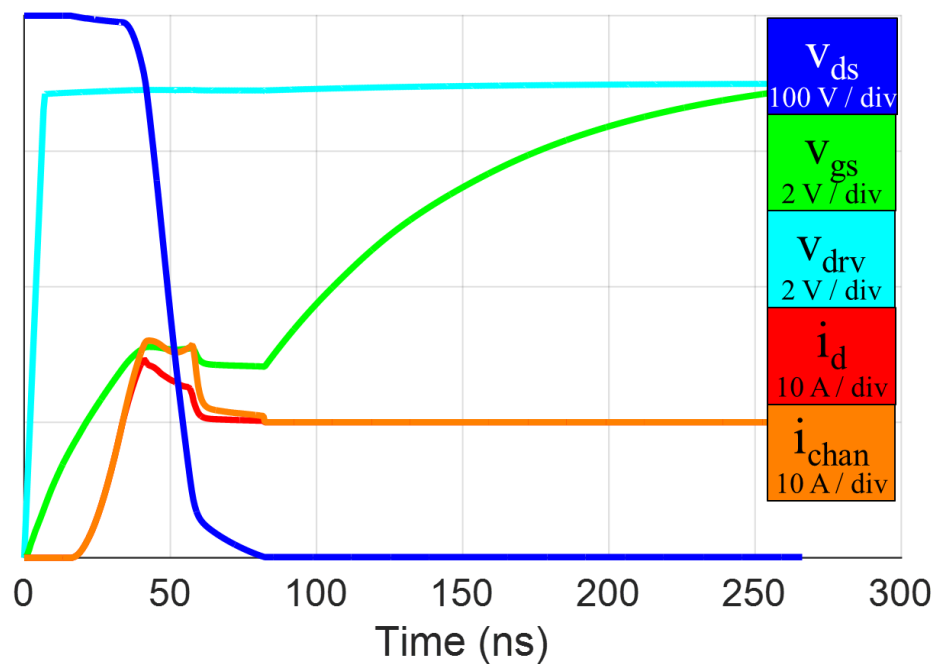


Figure 4.9. Calculated waveforms at 400 V, 10 A, with $R_{g,ext} = 100 \Omega$.

Figure 4.10 shows experimental gate voltage and channel current waveforms for the previously mentioned device under test, GaN Systems GS66508P, tested at 400 V and 10 A. Accurate extraction of the internal gate voltage from experimental results is difficult, because of the voltage drop across the internal gate resistance and inductance, as well as overall measurement noise. In experimental gate voltage waveforms, there often appears to be a Miller plateau due to the increased gate current during the voltage fall time, which induces a higher voltage drop across the internal gate resistance. By calculating the gate current from the C_{iss} characteristic and gate voltage waveform, the drop across this internal resistance can be estimated and subtracted as shown in Figure 4.10 as $v_{gs,adj}$. However, this does not account for the drop across the internal inductance.

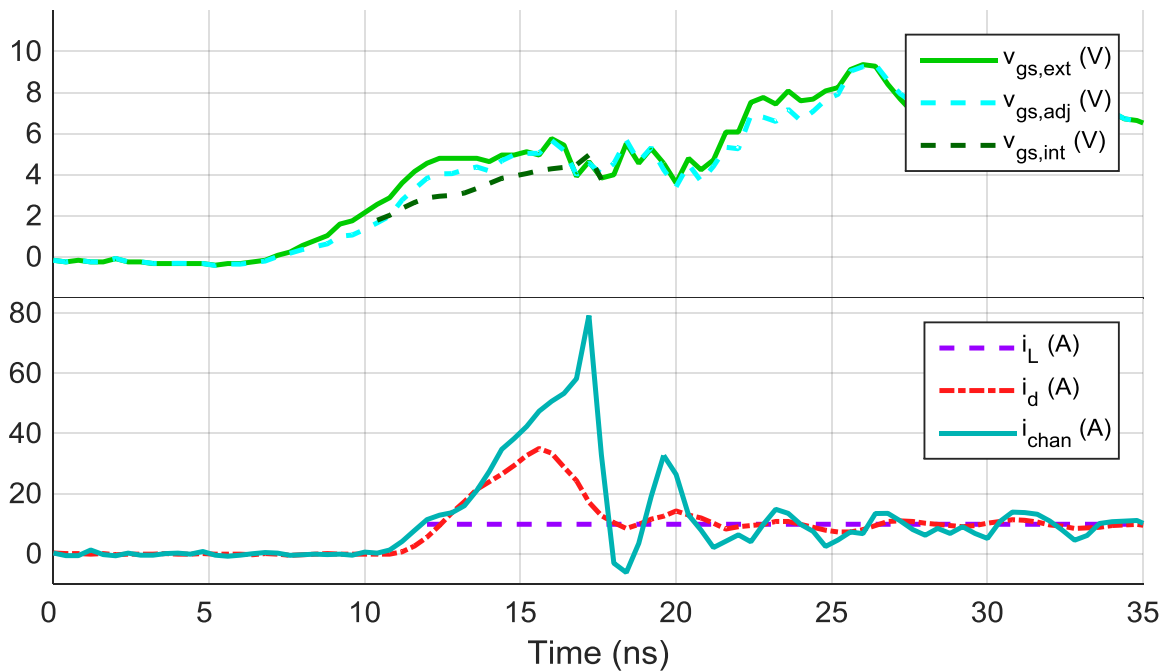


Figure 4.10. Experimental waveforms manipulated to estimate internal gate voltage.

Another technique to estimate internal gate voltage uses the calculated channel current and (19), which can be used effectively whenever the channel is operating in the saturation region. This is shown as $v_{gs,int}$. In both of these estimations for internal gate voltage, the slope is lower during the voltage fall time than it is during the current rise time, but it is still increasing. No plateau seems to occur, but v_{gs} begins to drop near the end of the voltage fall time. This is difficult to determine from the experimental waveform, because the exact point where the device enters the Ohmic region relies on more precise v_{ds} measurement than is feasible with a high dynamic range.

Next, the v_{gs} waveform shape was compared against a SPICE simulation, using the simulation model provided by the manufacturer. It should be noted that the simulations using this model did not accurately represent the oscillations seen in experimental results due to power loop and gate loop resonance. However, the simulation provides a helpful verification for the equations presented here, since that same ringing is neglected in the equations as well. Figure 4.11 and Figure 4.12 show the simulated turn-on waveforms with external gate resistances of 0 Ω and 100 Ω , respectively, both at the same operating conditions mentioned previously of 400 V, 10 A, and 25 $^{\circ}\text{C}$.

It appears in these waveforms that even when no Miller plateau occurs, the gate voltage slope always decreases to varying degrees during the voltage fall time, according to the negative feedback term in (37). The end of the voltage fall time tends to show a sharp drop in gate voltage that approaches the Miller voltage, just before the device enters the Ohmic region. This drop may be partly responsible for the resonance that occurs in the gate voltage waveform with faster turn-on, since the magnitude of the drop increases with lower gate resistance. Because no Miller plateau occurs, this also improves the typical model to explain how gate resistance is linked with the duration of the voltage fall time. These equations may be useful for gate driver design as well as development of a more accurate simulation model.

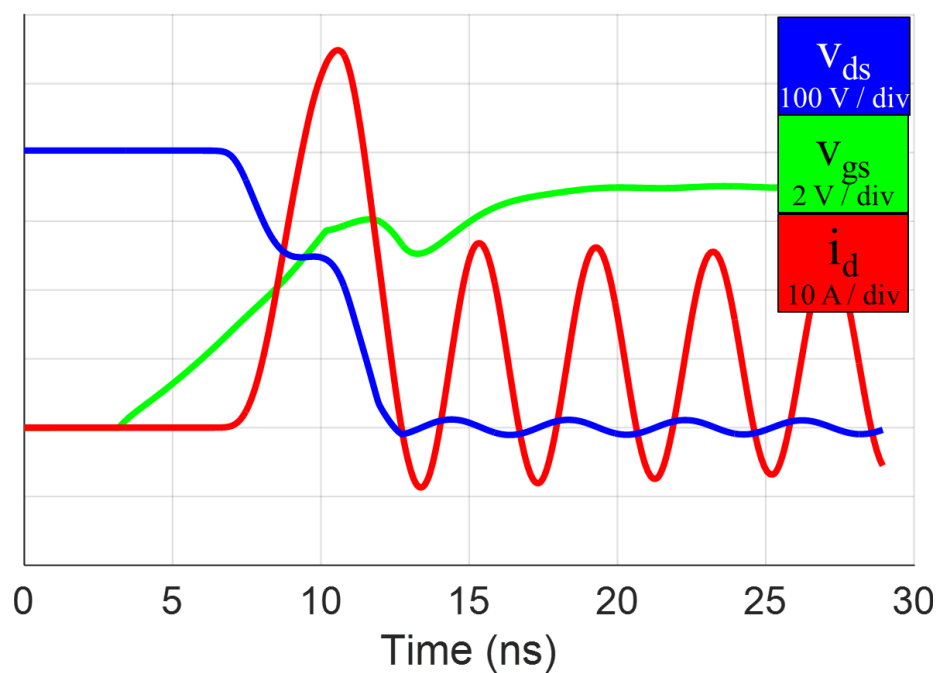


Figure 4.11. Turn-on waveform simulated in SPICE with $R_{g,ext} = 0 \Omega$.

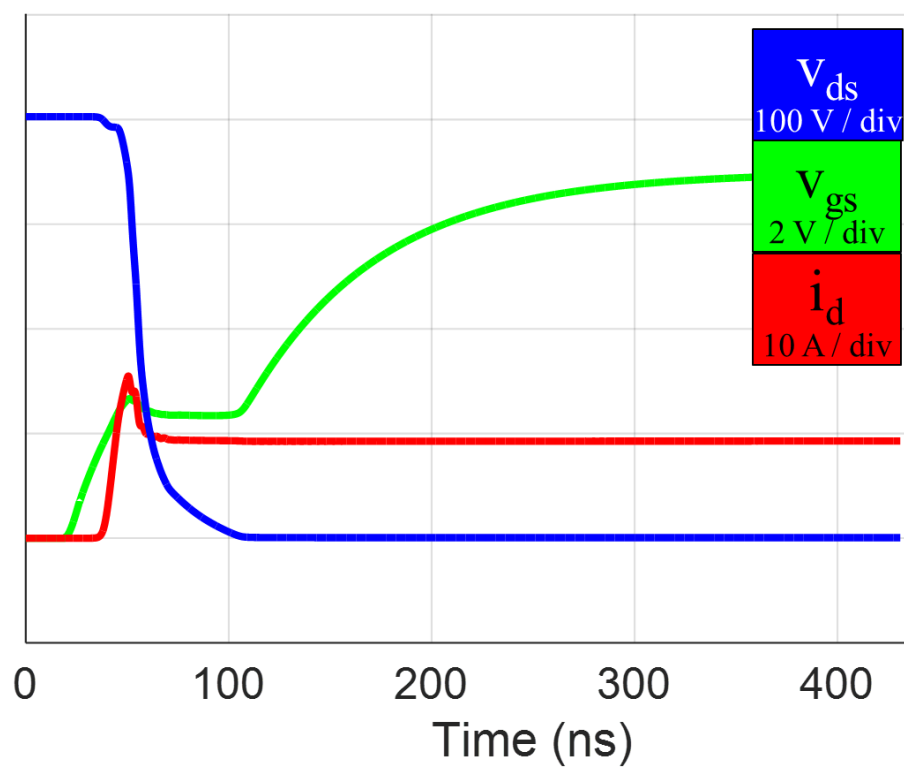


Figure 4.12 Turn-on waveform simulated in SPICE with $R_{g,ext} = 100 \Omega$.

4.6 *Analysis of the Temperature Dependency of the Turn-On Transient*

4.6.1 *Introduction*

One distinction between Si, SiC, and GaN semiconductors is their behavior at elevated junction temperature. Both Si and SiC exhibit little change in switching loss at higher temperature. However, enhancement-mode GaN devices have been shown to experience higher turn-on loss at elevated junction temperature, requiring a robust cooling design to prevent thermal runaway. This has been shown in the previous chapter as well as in [41], and it points to a fundamental difference between GaN and other power semiconductor materials.

The effect of temperature on GaN transconductance has been well-studied in prior literature, and is generally attributed to the decrease in 2DEG density and quantum well depth [138]. This work will show that the increased turn-on losses can be explained by the negative temperature coefficient of transconductance for these GaN devices. A relationship will be derived between junction temperature and turn-on loss, and verified experimentally with the GaN Systems GS66508P. The results shown in the previous chapter demonstrate that turn-on and turn-off overlap switching losses increase with temperature, but the increase in turn-on loss is much more significant and should not be ignored in GaN-based converter design.

Performing DPT at elevated temperature is very challenging with GaN devices, because of the chip-scale or PQFN packaging commonly used rather than bulkier TO-220 or TO-247 packages that are easier to heat. Elevating the temperature of the GaN device with a hot plate requires a connection on the top-side of the device or through the PCB, neither of which is convenient in a DPT. Alternatively, placing the entire board in an oven to heat the device compromises the other components, as well as affecting the integrity of measurement probes. Therefore, it is more desirable to perform the DPT at room temperature and scale the measured losses based on available static parameters.

The switching transients and losses of Si power MOSFETs have been well studied, but the interactions between device and board parasitics makes it difficult to analytically predict switching losses without experimental data. For this work, DPT experiments were performed at elevated temperatures, and a temperature-dependent model is proposed to predict the turn-on losses as junction temperature increases.

4.6.2 Assumptions and Simplifications for the Model

a) Average transconductance

In this analysis, the average transconductance was used, because that parameter is listed in most device datasheets or can be calculated from published curves. However, g_{fs} is actually variable during the transient and increases as a function of the gate voltage v_{gs} as described by (19), as well as with output voltage v_{ds} . To investigate this relationship, the transconductance was measured dynamically for the DUT, using a double pulse test as described in the previous chapter. In a typical DPT, the externally measured v_{gs} is not an accurate representation of the true internal v_{gs} due to the

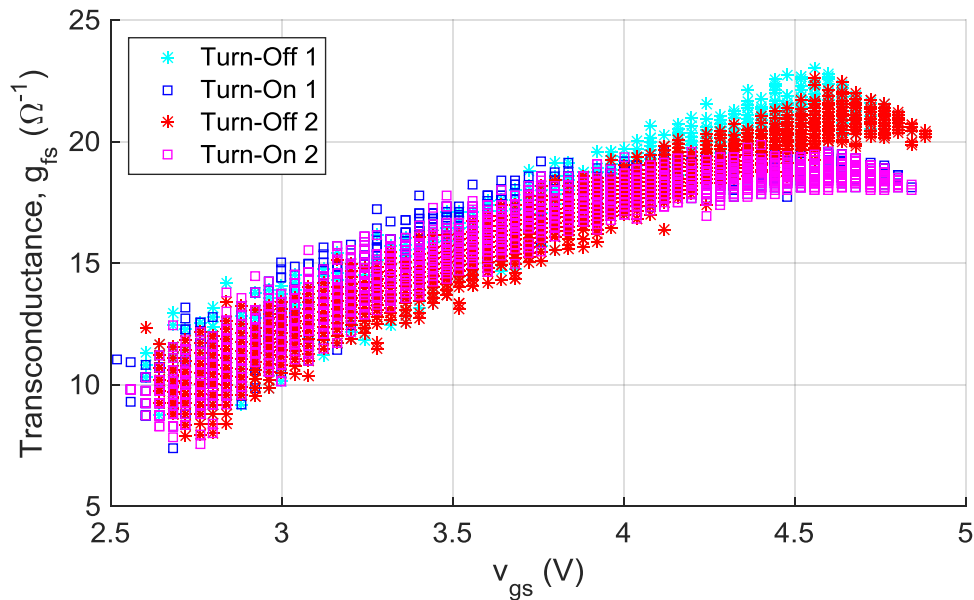


Figure 4.13. Transconductance of GS66508P measured during dynamic testing at 25 °C.

voltage drop across the internal R_g and L_{gs} of the device package. For this dynamic g_{fs} characterization, an external gate resistance of 1 k Ω was used so that the voltage drop across the internal device impedance was negligible in comparison. Using these v_{gs} and I_{dss} measurements, a dynamic g_{fs} vs. v_{gs} characteristic was determined during the current rise time. Figure 4.13 shows the g_{fs} calculated from two turn-on transients and two turn-off transients, demonstrating the positive correlation between g_{fs} and v_{gs} . However, the average g_{fs} between 2 V and 5 V matches the static measurement shown in Figure 3.8 at 25 °C.

b) Constant gate voltage slope

The slope dv_{gs}/dt was approximated as a constant value for this analysis. However, this slope will drop exponentially as the gate voltage approaches the driving voltage. Because g_{fs} increases with gate voltage and dv_{gs}/dt decreases, the product $g_{fs}dv_{gs}/dt$ remains fairly constant during the transient. It would improve the accuracy of the model to consider both dv_{gs}/dt and g_{fs} as v_{gs} -dependent variables, but this would add considerable complexity. Instead, it is effective to use the average values for both.

c) Negligible Miller effects

As shown earlier in this chapter, a fast gate drive circuit can minimize the Miller effect, so that dv_{gs}/dt is only somewhat reduced during the voltage fall time $t_{vf,sat}$. This requires a gate driver IC that can provide sufficient current, and the total impedance of the gate loop must be minimized with low resistance and a dense layout. Common-source inductance is also critical, so a Kelvin gate connection should be used when possible.

Even if these conditions are met, there may still be significant ringing in the v_{gs} , v_{ds} , and i_{chan} waveforms at the end of $t_{vf,sat}$, because C_{gd} gets much larger at low voltage. The ringing on C_{gd} will cause the device to alternate between the ohmic and saturation regions several times before

C_{gd} has fully discharged. However, as long as it only occurs near the end of $t_{v\text{fsat}}$, the losses due to this ringing are generally not very significant.

d) Constant threshold voltage

For some power devices, the threshold voltage $V_{gs,th}$ may be affected by temperature. However, the DUT and most GaN devices have a very stable threshold voltage over temperature, so it was not considered as a significant factor in this analysis.

e) Low power loop inductance

The parasitic power loop inductance L_{loop} is usually minimized for GaN-based converters with a dense board design and optimal device packaging. However, L_{loop} still causes an initial drop in V_{sw} during t_{cr} , which may not be negligible. However, this drop occurs on the active device when its voltage is high and its capacitance is at its lowest, and the magnitude of L_{loop} is not affected by temperature, so the effects of L_{loop} were neglected in this analysis.

f) Cross-talk loss

Lastly, the additional loss in the saturated channel due to cross-talk in the synchronous device was not considered in this analysis. The DPT experiments for this work used a gate-source shorted synchronous device to minimize cross-talk effects. Additionally, the previous chapter showed that the cross-talk component of turn-on loss is not noticeably impacted by temperature. Cross-talk should not be ignored for turn-on loss estimation, but the magnitude of this loss can be considered separately from the temperature-dependent losses.

4.6.3 Relationship Between Transconductance and Turn-On Loss

The derived equations for current rise time and voltage fall time are given in (38) and (39), respectively.

$$t_{cr} = \frac{I_L}{g_{fs}\left(\frac{dv_{gs}}{dt}\right)} \quad (38)$$

$$t_{vf,sat} = \sqrt{\frac{4 q_{oss}}{g_{fs} \left(\frac{dv_{gs}}{dt} \right)}} \quad (39)$$

The losses due to the displacement of C_{oss} stored energy in the active and synchronous devices are independent of turn-on time. The time-independent loss in the active device due to the synchronous device C_{oss} can be calculated from (26). The loss component due to the discharge of the active device C_{oss} into its own channel is given in (27) [137].

The remaining losses during t_{cr} and $t_{vf,sat}$ are strongly dependent on the duration of the turn-on transient. During t_{cr} , the voltage is nearly constant at V_{dc} while the channel current rises linearly up to the load current. The time-dependent energy loss during this time can be calculated as

$$E_{on,cr} = \frac{1}{2} t_{cr} (V_{dc} I_L) \quad (40)$$

During $t_{vf,sat}$, the channel conducts the full load current while the voltage drops from V_{dc} to nearly 0 V. The voltage during $t_{vf,sat}$ is determined by the nonlinear C_{oss} characteristic. If the voltage drop is initially approximated as linear, the time-dependent losses during this interval can be estimated with the simplified relationship

$$E_{on,td,vf} \approx \frac{1}{2} t_{vf,sat} (V_{dc} I_L) \quad (41)$$

The total turn-on loss can be described as the sum of these four components, but the component given in (27) is generally considered as turn-off loss. This energy is actually lost during the turn-on transient, but it can only be experimentally measured during the turn-off transient, when the energy is stored in the active device C_{oss} . Therefore, the conventional definition of turn-on loss can be described as the sum of (26), (40), and (41), as in

$$E_{on} = E_{on,Coss,sync} + E_{on,cr} + E_{on,td,vf} \quad (42)$$

4.6.4 Effect of Temperature on Transconductance

For a given device, the turn-on speed is mainly determined by operating voltage and current, the C_{oss} characteristic, gate driver speed dv_{gs}/dt , and device transconductance g_{fs} . If dv_{gs}/dt

and g_{fs} are both relatively high, the device channel will conduct more current, and the C_{oss} charge will be displaced quickly. However, GaN is distinct from Si and SiC in that its transconductance has a significant negative temperature coefficient. For the device under test (DUT) considered in this analysis, GaN Systems GS66508, g_{fs} was experimentally measured with a curve tracer over the rated temperature range. The calculation for average g_{fs} is given in (43), and the results over the device temperature range are shown in Figure 3.8 along with a second-order curve fit.

$$g_{fs} = \frac{I_{dss}(v_{gs}=5V) - I_{dss}(v_{gs}=2V)}{(3 V)} \quad (43)$$

The average transconductance drops by about one half over the rated temperature range of the DUT. According to (19), this also reduces the channel current while the device is operating in saturation, and consequently lengthens t_{cr} and $t_{vf,sat}$. As given in (38)-(42), this increases the current rise time and $E_{on,cr}$ by a factor of 2, and the voltage fall time and $E_{on,td,vf}$ by a factor of $\sqrt{2}$.

4.6.5 Consideration of Special Case at Elevated Temperature

With elevated temperature, there is a special case in which the analysis in the previous section no longer holds. If the $t_{vf,sat}$ becomes long enough that the gate voltage v_{gs} reaches V_{drv} while the device is still displacing C_{oss} charge, then the gate voltage can no longer increase. The channel current will be limited by the driving voltage after that time. Therefore, the voltage fall time can no longer be determined from (38). Instead, it must be modeled as two distinct subintervals, $t_{vf,sat1}$ and $t_{vf,sat2}$.

This will not generally occur at room temperature, because the recommended driving voltage and room temperature g_{fs} typically allow for a saturation channel current much higher than the rated maximum load current. This special case will occur when

$$t_{cr} + t_{vf,sat} > \frac{(V_{drv} - V_{gs,th})}{dv_{gs}/dt} . \quad (44)$$

The turn-on transient for this special case is shown in Figure 4.14. During the first subinterval, (19) still applies, but during the second subinterval, the channel current will be held constant at

$$i_{chan,tvfsat2} = g_{fs}(V_{drv} - V_{gs,th}) . \quad (45)$$

Therefore, the displacement current will be fixed during this subinterval, rather than increasing as in $t_{vf,sat1}$. The C_{oss} charge will be displaced at a fixed, non-increasing rate, and the new subinterval $t_{vf,sat2}$ can become quite long. The durations of $t_{vf,sat1}$ and $t_{vf,sat2}$ can be calculated as

$$t_{vf,sat1} = \frac{V_{drv} - V_{gs,th}}{dv_{gs}/dt} - t_{cr} \quad (46)$$

$$q_{sat1} = \frac{1}{2} g_{fs} \frac{dv_{gs}}{dt} t_{vf,sat1}^2 \quad (47)$$

$$q_{sat2} = 2q_{oss} - q_{sat1} \quad (48)$$

$$t_{vf,sat2} = \frac{q_{sat2}}{g_{fs}(V_{drv} - V_{gs,th}) - I_L} . \quad (49)$$

Since the voltage is still dropping from V_{dc} to 0 V during the combined voltage fall time, the linear simplification can still approximate the t_{vf} energy loss as

$$E_{on,vf} \approx \frac{1}{2} (V_{dc} I_L) (t_{vf,sat1} + t_{vf,sat2}) . \quad (50)$$

4.6.6 Consideration of Nonlinear C_{oss}

For the analysis in in the previous two sections, the voltage drop during the voltage fall time was treated as linear. This was necessary for the theoretical understanding of temperature dependence, but the nonlinear C_{oss} characteristic can be used to improve the accuracy of the model. The linear approximation is inherently an underestimate, because the voltage is exponentially decreasing, and the average voltage during t_{vf} should be higher than $V_{dc}/2$.

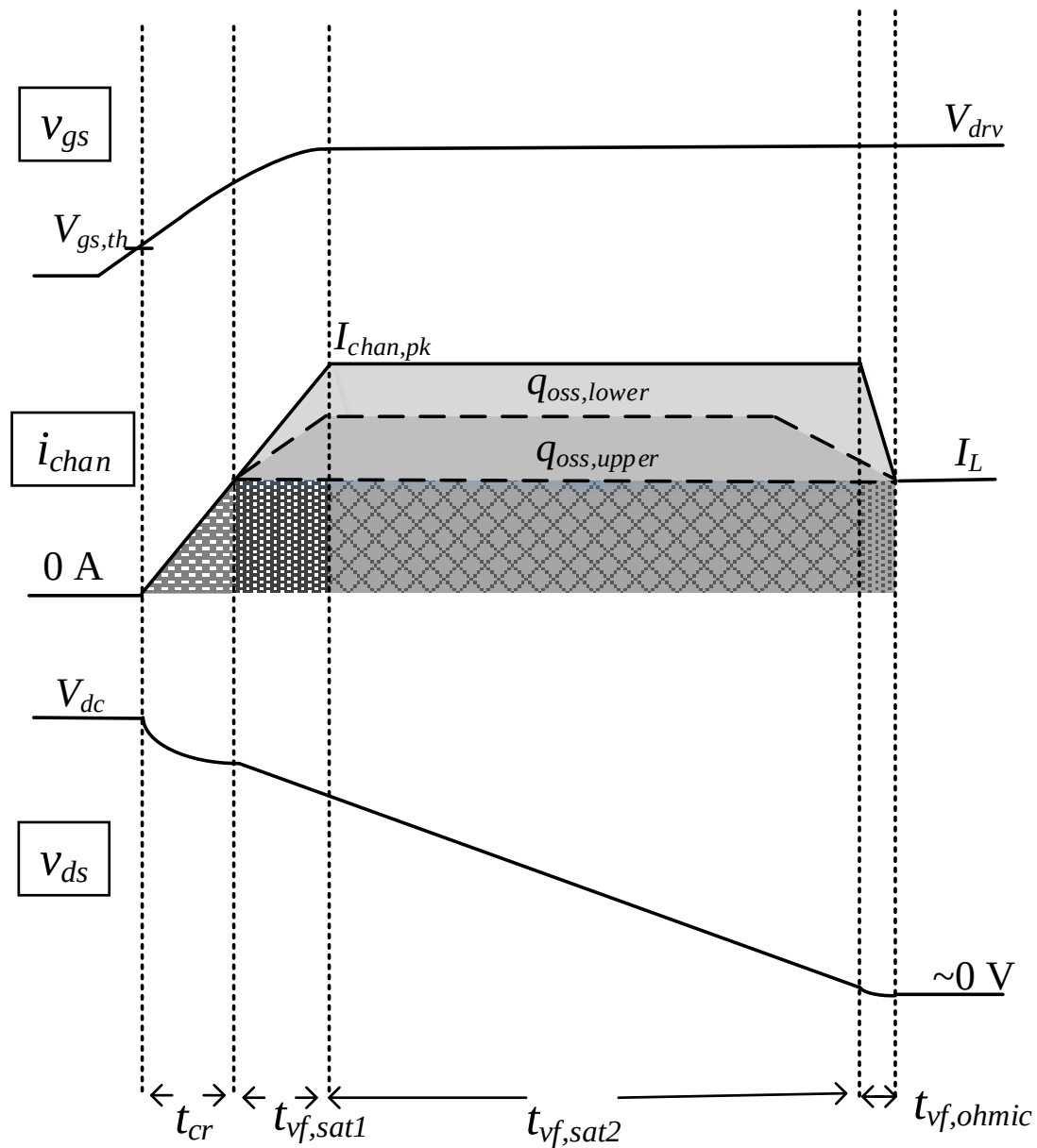


Figure 4.14. Turn-on transient analysis of the active device for the special case when gate voltage reaches its peak during the dv/dt transient.

The C_{oss} characteristic is given in the datasheet for most devices. For the DUT in this analysis, C_{oss} was measured with a precision impedance analyzer and also published in [70] among others. Figure 4.15 shows the total switch-node capacitance, which is the sum of the active device and synchronous device C_{oss} as the switch-node voltage falls from 400 V to 0 V and is calculated by

$$C_{sw}(v_{sw}) = C_{oss}(v_{sw}) + C_{oss}(V_{dc} - v_{sw}) . \quad (51)$$

The C_{oss} -related switching losses can be calculated from this curve using (26) and (27), and the total charge displaced q_{sw} can be calculated as a function of switch-node voltage using

$$q_{sw}(v_{sw}) = \int_{v_{sw}}^{V_{dc}} C_{sw}(v) dv . \quad (52)$$

Figure 4.16 shows the results of this calculation. The total displacement charge in both devices is equal to $2q_{oss}$ and can be found from the q_{sw} curve when $V_{sw}=0$ V.

Accounting for this nonlinear capacitance complicates the turn-on loss analysis, because the calculation requires integration of switch-node voltage over time as in

$$E_{on,td,vf} = I_L \int_0^{t_{vf,sat}} v_{sw}(t) dt \quad (53)$$

where $v_{sw}(t)$ can be determined from a combination of the v_{sw} vs. q_{sw} characteristic given by (52) and the equation

$$q_{sw}(t) = \frac{1}{2} g_{fs} \frac{dv_{gs}}{dt} t^2 . \quad (54)$$

This calculation is more accurate, but requires a software tool such as MATLAB to solve. The C_{oss} characteristic can be imported and interpolated, then a discrete-time interval can be used to calculate q_{sw} and $E_{on,td,vf}$.

Similarly, (41) can be revised to

$$E_{on,td,vfsat1} = I_L \int_0^{t_{vf,sat1}} v_{sw}(t) dt \quad (55)$$

where $v_{sw}(t)$ can be determined from (52) and (54), and

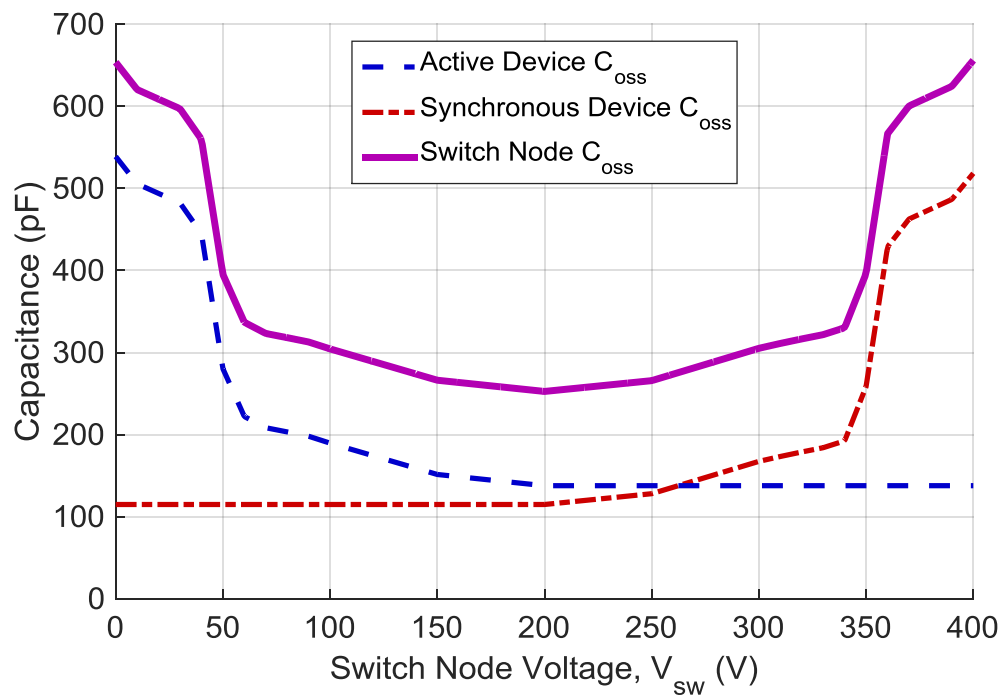


Figure 4.15. Output capacitance at the switch-node, with the DUT switching at 400 V.

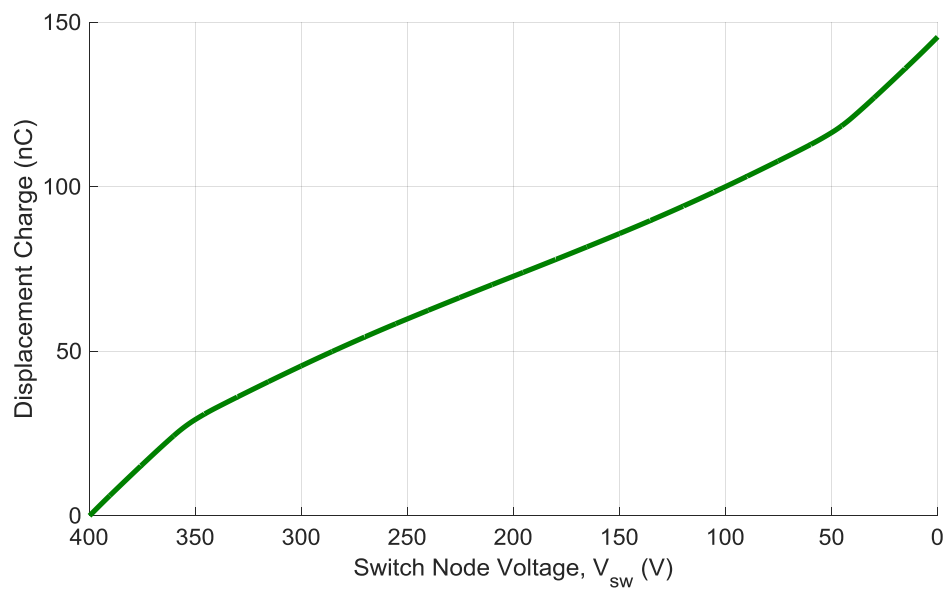


Figure 4.16. Charge displaced in the active and synchronous devices as the switching node voltage falls from 400 V.

$$E_{on,td,vfsatz} = I_L \int_0^{t_{vf,satz}} v_{sw}(t) dt \quad (56)$$

where $v_{sw}(t)$ can be determined from (52) and

$$q_{sw}(t) = q_{sat1} + [g_{fs}(V_{drv} - V_{gs,th}) - I_L]t . \quad (57)$$

4.6.7 Linear Approximation

In GaN-based converter design, it is common to perform a DPT with the chosen device, driver, and layout to characterize the switching losses at the intended operating voltage and current condition. It is therefore desirable to scale these results for the intended operating temperature, without the need to elevate device temperature during testing. Although the detailed model could be used for this purpose, it is useful to consider the linearized model described in (40)-(42). Because the majority of overlap loss occurs during the voltage fall time, the turn-on loss can be estimated for a given temperature using a simple scaling factor with the approximation

$$E_{on,Tj} \approx E_{on,Coss,sync} + k_{Eon,Tj}(E_{on,25C} - E_{on,Coss,sync}) \quad (58)$$

where $E_{on,25C}$ is the experimentally measured turn-on loss at the operating current and voltage, $E_{on,Coss,sync}$ is the loss calculated with (26) based on the nonlinear C_{oss} characteristic, and $k_{Eon,Tj}$ is the scaling factor

$$k_{Eon,Tj} = \sqrt{\frac{g_{fs,25C}}{g_{fs,Tj}}} . \quad (59)$$

This scaling factor will typically be between 1 and 2 depending on the GaN device under test, and it can be easily determined from the device datasheet. Typical datasheets show the transfer characteristic at various gate voltages, with 25 °C junction temperature and a higher T_j such as 125 °C or 150 °C. Average transconductance can be calculated from these characteristics using (43) at each temperature, and the g_{fs} at the intended operating temperature can be determined with linear interpolation.

This approximation requires no tuning or simulation, but its accuracy heavily depends on the experimental turn-on loss data at room temperature and the C_{oss} characteristic, as well as consideration for any additional capacitance from the PCB and test setup. It is also more limited in application than the detailed model, because it assumes that the voltage fall time is longer than the current rise time. With high current and very low voltage, the scaling factor may begin to approach $k_{Eon,TJ}^2$.

4.6.8 Experimental Verification

Double pulse testing (DPT) was performed on the DUT at junction temperatures ranging from 25 °C to 150 °C, with an 8 V gate drive and 0 Ω external gate resistance. Experimental test setup, results, and device characterization were detailed in the previous chapter. The internal C_{oss} current of the active device was calculated using (7) and added to the measured drain current to estimate the channel current waveform. It is important to note that the measured external gate voltage is only an approximation of the true internal gate voltage, so it is not equivalent to the v_{gs} used in this theoretical analysis. Rather than rely on this waveform, the value for average dv_{gs}/dt was tuned based on experimental data for turn-on time and loss, and determined to be approximately 1 V/ns in the 400 V switching case.

Figure 4.17 shows the turn-on transients at 400 V and 30 A, with junction temperatures of 25 °C and 150 °C respectively. At 25 °C, the device exits the saturation region as the gate voltage is still increasing, reaching a peak channel current of 85 A before the device enters the Ohmic region and the channel current quickly drops to I_L . At higher temperature, v_{gs} reaches the driving voltage before all of the C_{oss} charge has been displaced, in the special case described in Section III. The channel current is then held at ~50 A until the C_{oss} charge has been displaced and the device drops into the ohmic region. In both waveforms, the ringing due to C_{gd} is very pronounced as the

device enters the ohmic region, but the net energy loss during this ringing period is low, since v_{ds} has already dropped to nearly 0 V.

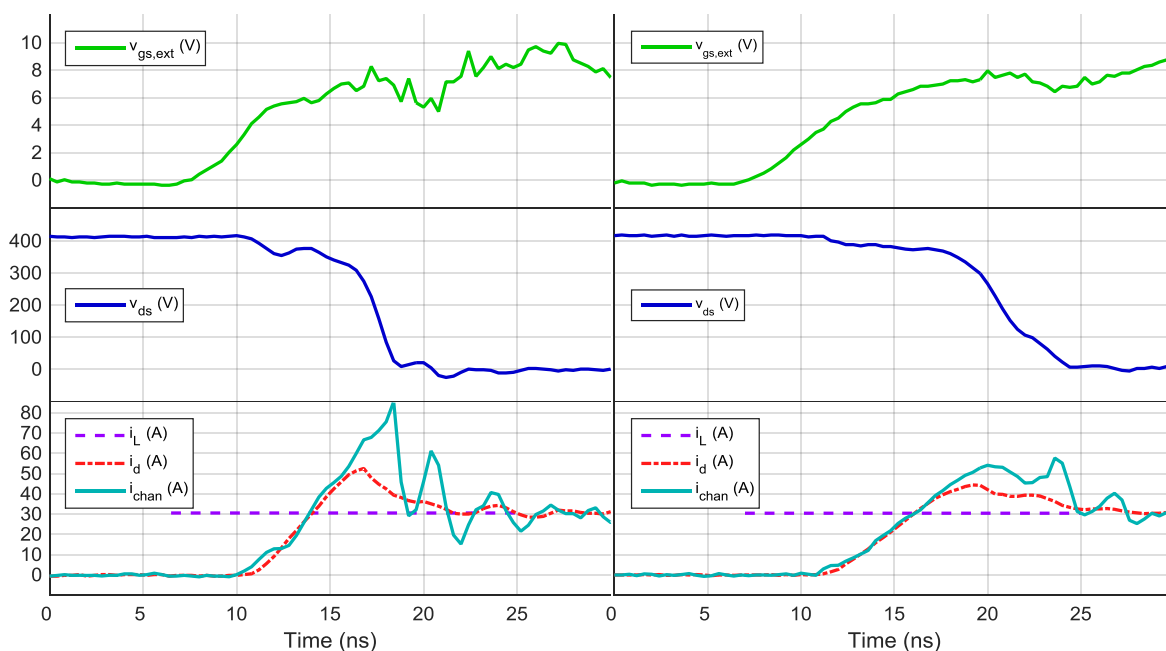


Figure 4.17. Experimental turn-on transient waveforms of the active device at 400 V and 30 A, (a) 25 °C and (b) 150 °C.

Using the derived model, switching times and energy loss were calculated across the current and temperature range at 200 V and 400 V. Experimental results were not used in these calculations, except for tuning dv_{gs}/dt as previously mentioned. Figure 4.17 - Figure 4.21 compare the experimental results with those predicted by the model. The calculated energy loss matches well with experimental results, although it is shown to be slightly less accurate in some cases. With low voltage or high load current, the assumptions made in Section V begin to break down, especially regarding the Miller effect and the significance of the initial voltage drop across the loop inductance. However, the model matches experimental results very well if the average dv_{gs}/dt is tuned appropriately.

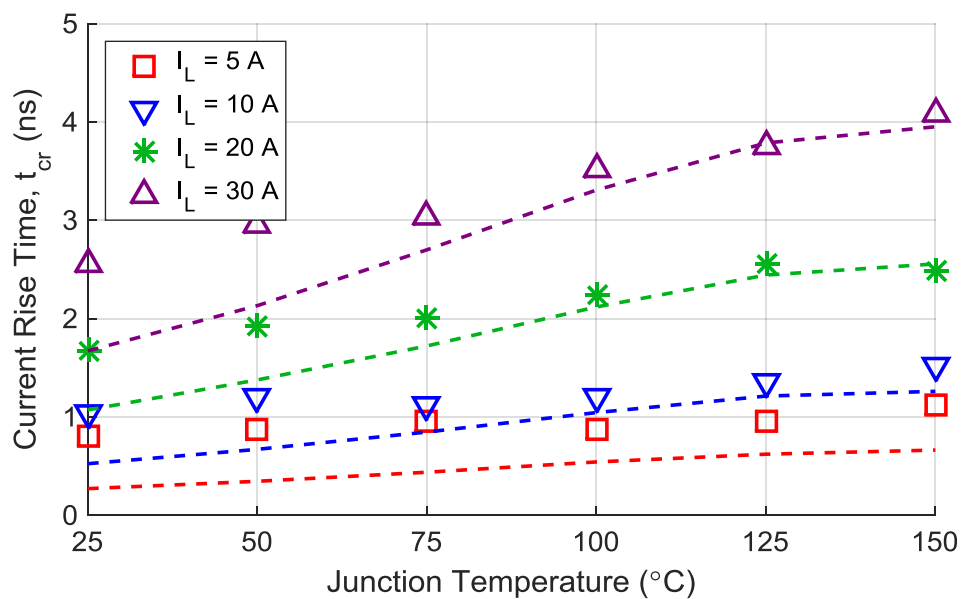


Figure 4.18. Experimental results for current rise time of the DUT at 400 V, with the dashed lines showing calculated t_{cr} based on the detailed analytical model.

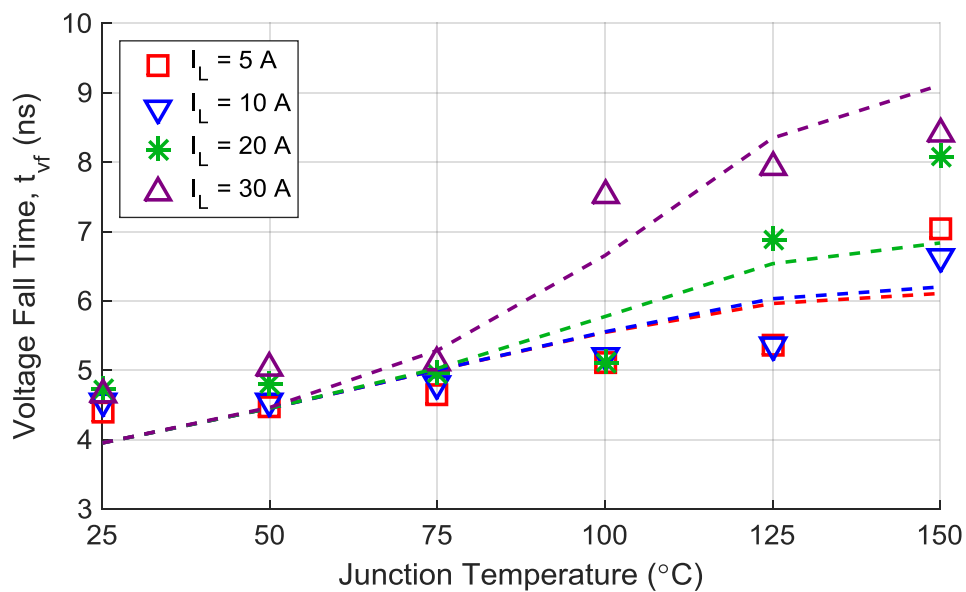


Figure 4.19. Experimental results for voltage fall time of the DUT at 400 V, with the dashed lines showing calculated $t_{vf,sat}$ based on the detailed analytical model.

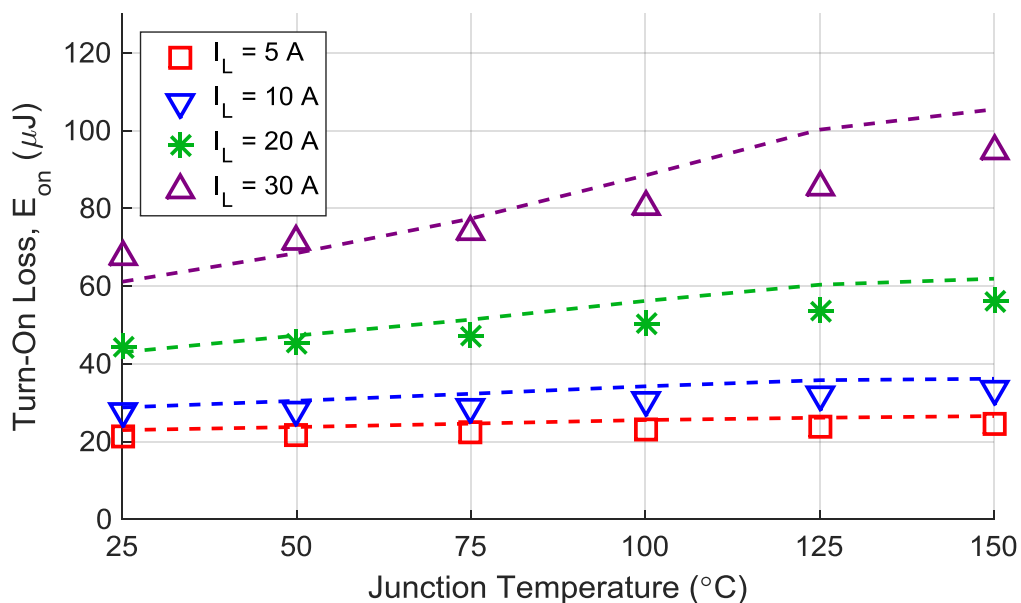


Figure 4.20. Experimental results for E_{on} of the DUT at 400 V, with the dashed lines showing predictions by the detailed analytical model

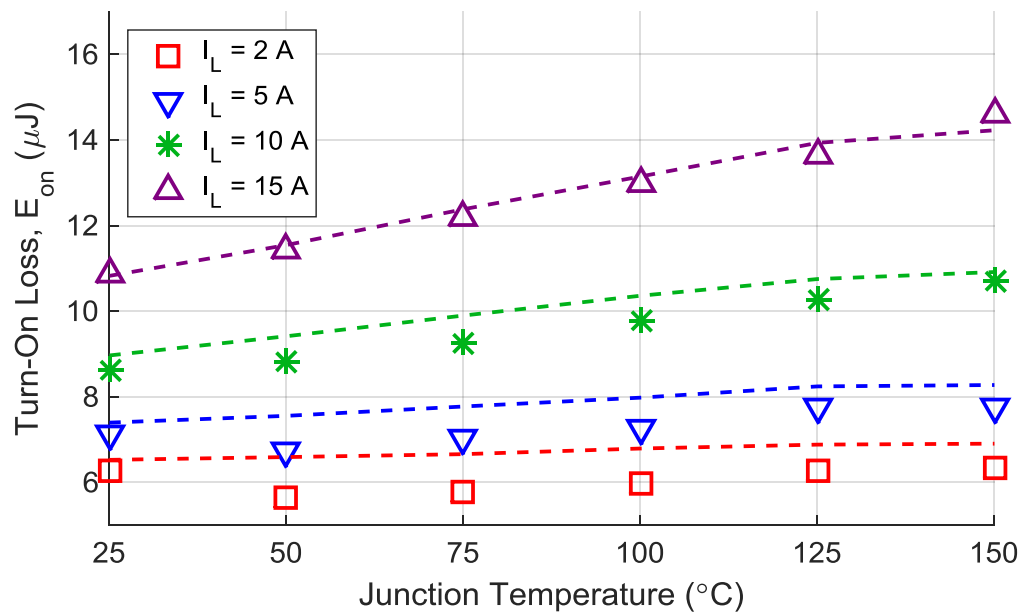


Figure 4.21. Experimental results for E_{on} of the DUT at 200 V, with the dashed lines showing predictions by the detailed analytical model.

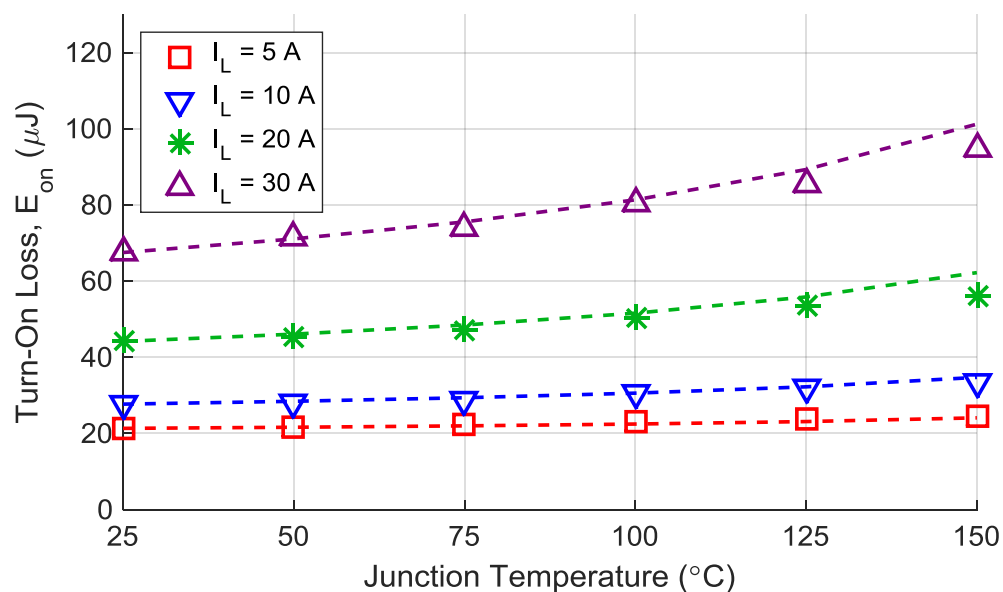


Figure 4.22. Experimental results for E_{on} of the DUT at 400 V, with the dashed lines showing the linear approximations calculated using published datasheet parameters and DPT data at 25 $^{\circ}\text{C}$.

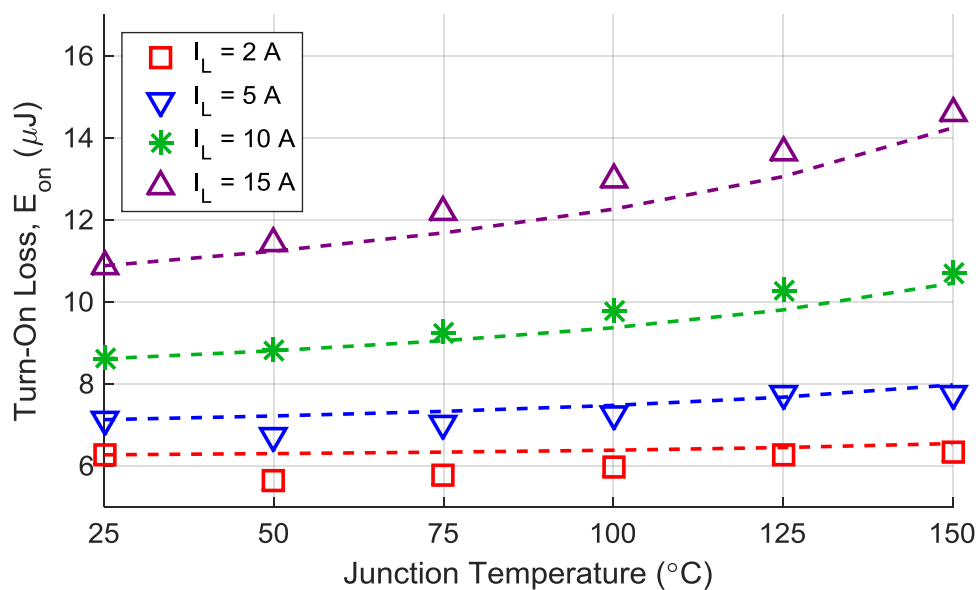


Figure 4.23. Experimental results for E_{on} of the DUT at 200 V, with the dashed lines showing the linear approximations calculated using published datasheet parameters and DPT data at 25 $^{\circ}\text{C}$.

Figure 4.22 and Figure 4.23 show the linear approximations based on (58) and (59), at 400 V and 200 V respectively. This approximation matches experimental results even more closely than the detailed theoretical model, because it is directly based on the DPT results at 25 °C. However, this approximation relies on even more assumptions than the detailed analytical model, so it may not be as accurate for all e-mode GaN devices and converter designs as it is for the DUT considered here.

4.7 Summary

The general switching behavior of the enhancement-mode GaN HFET has been described with a subcircuit model and subinterval analysis. The voltage and current equations for each subinterval were given, neglecting some complexities such as power loop and gate loop inductance. These equations were then verified for overall waveform shape through comparison with experimental results and simulation. One of the significant elements studied in this model was the Miller effect during turn-on, which causes a reduced gate voltage slope during the voltage fall time, followed by a sharp drop near the end of the transient.

Another element of this analysis was the effect of temperature on the turn-on loss of the enhancement-mode GaN device. The root cause of temperature-dependent turn-on loss was attributed to decreased transconductance. Using theoretical analysis and experimental results, a turn-on loss model was developed to predict the effect of elevated junction temperature at any given current and voltage condition for a GaN device, based on the average transconductance over temperature. A detailed analytical model was developed, as well as a simplified linear approximation. The scaling factor $k_{Eon,Tj}$ allows for typical room temperature DPT switching loss results to be adjusted for any operating temperature using only the transfer characteristic published on the device datasheet. This approximation was shown to be both simple and accurate. Accurate and comprehensive loss calculation is critical for effective thermal design, to prevent thermal

runaway. Because turn-off loss does not change much with temperature, and T_j vs. R_{ds-on} trends are readily available, turn-on loss is the final component needed for calculating total losses. The proposed model closes the loop on GaN-based converter loss characterization, enabling a more robust design.

Chapter 5

Conclusion

5.1 Contributions

Contributions from the work presented here include the following elements:

- a) Commercial and near-commercial GaN power devices were reviewed. This review is distinct in that it is given from the perspective of GaN-based converter design and application, rather than device fabrication; and that it covers a range of devices available today, rather than focusing on a single manufacturer's device. This review includes some typical structures of both vertical and horizontal devices, their commercial availability and ratings, and some of the unique properties of these devices. Following this application-focused device review, the design challenges of GaN power devices were summarized, including board layout and gate driver requirements.
- b) One enhancement-mode GaN HFET was characterized across a full sweep of voltage, current, and temperature conditions, with several gate voltages and resistances. These tests include static characteristics such as forward and reverse conduction behavior, on-resistance, transconductance, gate leakage current, and junction capacitance. Additionally, the dynamic characteristics were studied with a sweep of double pulse tests, measuring turn-on times and loss as well as turn-off times and loss. The waveforms were also studied for other dynamic properties such as gate and drain overvoltages and peak dv/dt .
- c) In addition to the typical dynamic characterization, a methodology was developed to determine the turn-on loss due to cross-talk with various symmetric and asymmetric gate resistances. The losses in both the active and synchronous devices due to the shoot-through current caused by cross-talk were measured using this experimental methodology for the

enhancement-mode GaN HFET characterized in (b). The negative spikes caused by this cross-talk were also studied for each case.

- d) A model was developed to explain the behavior of the gate voltage of an enhancement-mode GaN HFET during the turn-on dv/dt transient, which is typically considered to be a Miller plateau. Using subcircuit analysis, equations for the driver voltage, gate voltage, gate current, drain-source voltage, channel current, and drain current were developed. This model was simplified substantially by neglecting the parasitic inductances in the gate loop and power loop, so that the ringing in the waveforms was not accurately described. However, a discrete time calculation of these variables was shown to match well with both experimental results and SPICE simulation results, with the exception of that ringing. This model was not developed to accurately predict losses, but rather to understand and explain the experimental waveforms and provide a basis for improved gate driver design for this device.
- e) Using similar equations, a second model was developed to predict the increase in turn-on losses for an enhancement-mode GaN HFET with elevated temperature at any particular voltage, current, and gate driver design. This model is also not intended to predict losses in itself. However, using static data available from most device datasheets, the experimentally measured turn-on losses at room temperature can be scaled to predict the turn-on loss for that same operating point at a higher temperature. This calculation was verified with experimental results, including a detailed version of the model and a simplified linear approximation.

5.2 *Future Work*

Future tasks for the work presented here will include the following elements:

- a) The experiments to capture cross-talk switching losses will be repeated to further understand the apparently unrecovered energy from the synchronous device, which may have been a measurement error or may represent a physical phenomenon that is not yet clear. These

experiments will be conducted with a range of driving voltages in addition to asymmetric gate resistances, bus voltages, load currents, and junction temperatures as originally conducted. As a result of these experiments, the overall switching losses at 6 V will also be measured, now that the manufacturer has revised its specifications to recommend lower than 7 V for the driver supply.

- b) The switching losses measured with single-trigger double pulse tests will be verified with continuous operation of the DPT board as a buck converter, with a load including both resistive and inductive components. The load current, switching frequency, and input voltage can be varied in this testing, to determine switching and conduction losses and compare them with the loss characterization presented here.
- c) The currently available SPICE simulation model will be improved upon, to more accurately represent the resonance in current and voltage waveforms that occur during switching transients. This will involve further measurement of the junction capacitances, particularly at low and negative voltage, as well as more precise transfer characteristics across a range of temperatures with a higher drain-source voltage.
- d) Using the results from tasks (a)-(c), an improved gate driver will be developed and experimentally verified. The motivation for this driver will be to achieve low switching losses while maintaining an acceptable amplitude of ringing on the gate voltage to prevent spurious switching, and consequently the over-voltage on both the gate and drain to prevent damage to the device. These two goals are closely related, as the conventional gate drive design methodology dictates that the switching speed must be reduced to minimize this undesirable ringing. If an intelligent gate driver can reduce the ringing amplitude, a GaN-based converter design can more practically take advantage of the fastest achievable switching speed of the device, without risking device breakdown.

5.3 Publications

E. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, "Temperature-dependent turn-on loss analysis for GaN HFETs," in *Proc. IEEE Applied Power Electronics Conference (APEC)*, Long Beach, CA, Mar. 2016, pp. 1010-1017.

E. Jones, Z. Zhang, F. Wang, "Wide bandgap device characterization," professional education seminar, presented at IEEE Applied Power Electronics Conference (APEC), Long Beach, CA, Mar. 2016.

E.A. Jones, F. Wang, D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics* (accepted), 2016.

E. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, "Cross conduction analysis for an enhancement-mode 650-V GaN HFET in a phase-leg topology," in *Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, Nov. 2015, pp. 98-103.

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C. Zhao, B. Trento, J. Liang, E. Jones, B. Liu, Z. Zhang, D. Costinett, F. Wang, L. Tolbert, J Jansen, R. Kress, R. Langley, "Design and Implementation of GaN-Based, 100 kHz, 102W/in³ Single-Phase Inverter for the Google Little Box Challenge," *IEEE Journal of Emerging and Selected Topics in Power Electronics* (accepted), 2016.

R. Ren, B. Liu, E. Jones, F. Wang, Z. Zhang, D. Costinett, "Dual-output, Three-level GaN-based Dc-Dc Converter for Battery Charger Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics* (accepted), 2016.

R. Ren, B. Liu, F. Wang, E. Jones, "Dual-output, three level GaN-based DC-DC converter for battery charger applications" in *Proc. IEEE Applied Power Electronics Conference (APEC)*, Long Beach, CA, Mar. 2016, Pp. 2441-2448.

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Vita

Edward A. Jones was born in Richmond, Virginia, and attended the Virginia Polytechnic Institute and State University (Virginia Tech), where he graduated magna cum laude with an honor baccalaureate B.S.E.E. in 2007, with a concentration in Power Electronics and minors in Math and Religious Studies. As part of this degree, Edward wrote and defended an undergraduate thesis titled “Calorimetric Measurement of Efficiency for a Boost-Buck Converter for Automotive Applications.” After graduating, he worked for General Electric as an electrical engineer for one year, then as a field application engineer for four years. During this time, his primary responsibility was the design, installation, and repair of measurement and monitoring systems for rotating equipment in the power industry and oil and gas industry, covering a territory that included the Northeastern United States.

Since 2012, Edward has been working towards his Ph.D. in Electrical Engineering at the University of Tennessee, Knoxville. He has two fellowships: the Chancellor’s Fellowship, and the Bredesen Fellowship for Interdisciplinary Research. At UTK, Edward’s research has focused on review and characterization of GaN devices, with the motivation to better understand the device behavior for an improved gate driver design. While a student, he has also served as the President of the CURENT Student Leadership Council, as well as other officer positions in the SLC. His anticipated Ph.D. graduation date is December 2017.