

POWER QUALITY CONTROL AND COMMON-MODE NOISE MITIGATION FOR INVERTERS IN ELECTRIC VEHICLES

A Dissertation Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Yang Huang

August 2022

Copyright © 2022 by Yang Huang

All rights reserved.

*This dissertation and all of my academic achievements
are dedicated to the memory of my two grandmothers.*

ACKNOWLEDGEMENT

Upon the completion of this dissertation, I am grateful to those who have offered me encouragement and support during the journey of achieving my academic and career goals. First, special acknowledgment is given to my respectable supervisor, Dr. Hua Bai, whose patient instruction and constructive suggestions are beneficial to me a lot. His profound knowledge and professional insights offered me numerous valuable comments and suggestions throughout my doctoral study. Without his painstaking teaching and insightful advice, the completion of this thesis would have been impossible.

I am also deeply grateful to Dr. Leon Tolbert, he is so professional and exceptional, not only in this field but in the whole academic society. His instruction and support on my research and writing indeed set an example for me to be professional. Thanks to Dr. Fred Wang, Dr. Daniel Costinett, and Dr. Helen Cui for their generous suggestions and instructions in my research projects. I want to say thanks to my Master's degree advisor, Dr. Mengqi Wang, she is the first scholar that sparked my interest in electrical engineering and encouraged me to go further study.

I would like to thank Dr. Bing Chen. In our 4-year collaboration in the Daimler projects, his practical advice on my research greatly helped me correct my academic pathways, these taught me that good research should always link to reality, an excellent engineer and research outcome should never be out of industrial practice.

I have been blessed with loving and supportive people throughout my academic career, and I have been encouraged by so many. My parents and grandparents have always invested and believed in me. Their name should be mentioned here, Xiaoping Huang,

Xiaohui Tang, Shilu Tang, Yanzhi Gong, Zhiquan Huang, and Shulan Chen. Their unconditional love is the driving force for me to pursue a doctoral degree, and our link has never been weakened even though we are separated by the entire Pacific. Also, to my pet Wanwan, who has companied me for the past 5 years and welcomed me back home at every tired staying-up night, thank you!

I would also like to thank the University of Tennessee and CURENT for all the kind support and resources for the students. I also cherish the friendship and help from all colleagues, alumni, and friends, including but not limited to Mr. Liyan Zhu, Dr. Yu Yan, Mr. Ziwei Liang, Mr. Ximu Zhang, Mr. Jared Walden, Mr. Ziang Yu, Mr. Fanning Jin, Dr. Ruiyang Qin, Dr. Jingjing Sun, Dr. Zhe Yang, Dr. Xingxuan Huang, Dr. Jie Li, Dr. Ren Ren, Dr. Ruirui Chen, Dr. Zhou Dong, Dr. Bo Liu, Dr. Shuyao Wang, Ms. Niu Jia, Mr. Xingyue Tian, Mr. Xin Xia, Mr. Dingrui Li, Mr. Zihan Gao, Ms. Le Kong, Mr. Liang Qiao, Mr. Peter Pham, Mr. Jared Baxter, Mr. Andrew Foote, Dr. Yu Jiang, Mr. Ziming Wang, Ms. Paychuda Kritprajun, Dr. Haiguo Li, Mr. Nattapat Praisuwanna, Ms. Xi Chen, and Dr. Yanting Zhang. Finally, I would like to extend my gratitude to all staff, including but not limited to Mr. Robert Martin, Dr. Chien-Fei Chen, Dr. Anne Skutnik, Mr. Ryan Smiley, Ms. Wendy Smith, and Mr. Jay Cooley, their professional help has always been so reliable.

Receiving a doctoral degree is not the end, life remains challenging. A meaningful life is always about endless pursuit. My favorite basketball player, Kevin Garnett once said: “It’s been a journey, to say the least, but in some ways, I’m beginning a new one. This game is all about moving forward, shoot. So was Life. It’s one footprint after another. And just when we think we’ve made our mark, it’s washed away. But I’ll be back tomorrow.”

Go Vols!

ABSTRACT

Inverters are widely utilized in electric vehicle (EV) applications as a major voltage/current source for onboard battery chargers (OBC) and motor drive systems. The inverter performance is critical to the efficiency of EV system energy conversion and electronics system electro-magnetic interference (EMI) design. However, for AC systems, the bandwidth requirement is usually low compared with DC systems, and the control impact on the inverter differential-mode (DM) and common-mode (CM) performance are not well investigated. With the wide-band gap (WBG) device era, the switching capability of power electronics devices drastically improved. The DM/CM impact that was brought by the WBG device-based inverter becomes more serious and has not been completely understood.

This thesis provides an in-depth analysis of on-board inverter control strategies and the corresponding DM/CM impact on the EV system. The OBC inverter control under vehicle-to-load (V2L) mode will be documented first. A virtual resistance damping method minimizes the nonlinear load harmonics, and a neutral balancing method regulates the unbalanced load impact through the fourth leg. In the motor drive system, a generalized CM voltage analytical model and a current ripple prediction model are built for understanding the system CM and DM stress with respect to different modulation methods, covering both 2-level and 3-level topologies. A novel CM EMI damping modulation scheme is proposed for 6-phase inverter applications. The performance comparison between the proposed methods and the conventional solution is carried out. Each topic is supported by the corresponding hardware platform and experimental validation.

TABLE OF CONTENTS

Chapter 1 Introduction	1
1.1 Background of Electric Vehicles	1
1.1.1 EV Overview	1
1.1.2 EV Charger	3
1.1.3 EV Motor Drive System	7
1.2 Research Objectives and Approaches.....	9
1.2.1 Motivation.....	9
1.2.2 Strategy	11
1.3 Dissertation Organization	12
Chapter 2 Literature Review	13
2.1 EV Charger Power Quality Control.....	13
2.1.1 EV and Distributed Energy Resources	13
2.1.2 General Approaches for Unbalanced Load Compensation.....	14
2.2 Motor Drive System and CMV Mitigation.....	26
2.2.1 Motor Drive System and the Origin of CMV	26
2.2.2 General Approaches for CM EMI Mitigation.....	30
2.3 Existing Research Interests	56
Chapter 3 THREE-PHASE INVERTER POWER QUALITY MODELING AND CONTROL.....	58
3.1 Modeling of Three-phase Four-wire Inverter at V2L Mode.....	59
3.2 Neutral Point Voltage Control	61

3.3 Virtual Resistance Control.....	68
3.3.1 Resistive Load.....	68
3.3.2 Resistance–Inductive Load	74
3.3.3 Resistance–Capacitive Load	77
3.4 Simulation Result.....	79
3.4.1 Simulation of the Virtual Resistance	79
3.4.2 Simulation of the Neutral-point Control	82
3.5 Experimental Validation	86
3.6 Summary	92
Chapter 4 THREE-PHASE INVERTER COMMON-MODE VOLTAGE MODELING	93
4.1 CMV Analysis for Different PWM Patterns.....	94
4.1.1 CM Modulation Signal	94
4.1.2 CMV Modeling with Double Fourier Integral.....	98
4.1.3 CM Energy Distribution	103
4.2 DM Current Ripple Prediction.....	105
4.3 Comprehensive Comparison.....	112
4.4 Experimental Validation	117
4.5 Impact of Control Bandwidth	124
4.5.1 CBW Impact on CM Signal.....	127
4.5.2 CBW Impact on DM Signal.....	130
4.6 Summary	133

Chapter 5 Common-mode voltage Elimination for DUAL THREE-PHASE INVERTERs	135
5.1 Modulation of Six-phase Motor Drive System.....	136
5.2 Mathematical Model of CMV in DTM System.....	138
5.2.1 SPWM-based ZCMVM for Low/Medium Modulation Index ($MI \leq 0.785$) .	138
5.2.2 SVM-based RCMVM for High Modulation Index ($0.785 < MI \leq 0.906$)	143
5.2.3 SVM-based RCMVM for Overmodulation ($0.906 < MI < 1$)	147
5.3 Implementation and Simulation Result.....	150
5.3.1 Low/Medium modulation range ($0 < MI \leq 0.785$).....	153
5.3.2 High/overmodulation range simulation ($0.785 < MI \leq 1$).....	155
5.3.3 Differential-mode performance	155
5.3.4 Dynamic performance.....	159
5.4 Experimental Validation	162
5.4.1 CMV Measurement.....	165
5.4.2 DM Current Ripple measurement.....	174
5.5 Summary	176
Chapter 6 Three-level InveRter Common-mode voltage MODELING AND reduction	178
6.1 Three-level Active Neutral Point Clamped Inverter Modulation	179
6.2 CMV Analytical Model for 3-Level Modulation.....	179
6.2.1 CSVM	179
6.2.2 NTSVM	184
6.2.3 RCMVM	187

6.3 CMV Performance Evaluation.....	190
6.4 Summary	193
Chapter 7 Conclusion and Future Work	195
7.1 Conclusion	195
7.1.1 Summary of The Work	195
7.1.2 Contributions.....	196
7.2 Future Work.....	200
REFERENCE.....	204
VITA.....	226

LIST OF TABLES

Table 3.1: Simulation parameters	84
Table 4.1: Three-phase current THD	107
Table 4.2: Current slope under different space vectors.	109
Table 4.3: Predicted peak CMC vs Measured Result	126
Table 4.4: Three-phase current THD with different f_c - f_θ pair	132
Table 5.1: ZCMVM rules	145
Table 5.2: Test bench parameters	164

LIST OF FIGURES

Figure 1.1: Global electric car stock, 2010-19 [1].	2
Figure 1.2: Power electronics structure in an EV.	4
Figure 1.3: Charging network comparison in the U.S.	6
Figure 1.4: WBG Application roadmap in different power conversion scenarios [10].	8
Figure 1.5: Intercity travel from Salt Lake City to Denver [11].	10
Figure 2.1: Topology-based APF.	15
Figure 2.2: Structure of the converter-fed, islanded microgrid [17].	15
Figure 2.3: Schematic diagram of wind–hydro hybrid system [18].	15
Figure 2.4: Three-phase topologies.	17
Figure 2.5 Three-phase Inverter neutral structure.	17
Figure 2.6 Neutral point connection method of three-phase inverters.	17
Figure 2.7: Three-phase four-wire inverter with split DC-link capacitors.	19
Figure 2.8: Control strategy of a 4-leg inverter with symmetrical components [29].	21
Figure 2.9: A three-phase 4-leg inverter with the unbalance compensator.	21
Figure 2.10: Bidirectional charger topologies.	23
Figure 2.11: ANF control diagram.	25
Figure 2.12: Three-phase two-level VSI motor drive system.	27
Figure 2.13: Motor shaft current path.	29
Figure 2.14: CM EMI noise mitigation methods categorization.	29
Figure 2.15: Circuit diagram of three major passive CM filters.	31
Figure 2.16: Typical motor drive system with CM filters incorporated [56].	31

Figure 2.17: Implementation of feedforward CM noise voltage cancellation [62].	33
Figure 2.18: Switching node voltage comparison.	36
Figure 2.19: CM EMI emissions comparison.	36
Figure 2.20: Comparison between the CM EMI emissions of Si MOSFET and GaN HEMT-based drives at an extended frequency range [70].	36
Figure 2.21: Space vectors of RSPWM proposed in [77].	39
Figure 2.22: Space vectors of NSPWM proposed in [79].	41
Figure 2.23: PWM pulse pattern of SVPWM, AZSPWM1, and NSPWM and the corresponding CMV [82].	41
Figure 2.24: CMC reduction performance comparison.	44
Figure 2.25: 3-level VSI for motor drives.	46
Figure 2.26: Output voltage vector diagram of the 3-L NPC inverter [92].	46
Figure 2.27: 7 switching states with zero CMV [93].	48
Figure 2.28: Multilevel inverter CMV [93].	48
Figure 2.29 The drive system for a DTM.	50
Figure 2.30: Principle of the proposed end-to-end cyclic sequence of PWM signal.	52
Figure 2.31 Carriers in one switching cycle.	52
Figure 3.1: Topology of a three-phase four-wire inverter used in a V2L EV charger.	60
Figure 3.2: Equivalent circuit of ICNM.	60
Figure 3.3: Control block diagram of a single-phase equivalent circuit.	60
Figure 3.4: Single-phase SPWM control block diagram.	62
Figure 3.5: Structure of the neutral phase.	64
Figure 3.6: Control block diagram of the neutral-point voltage.	67

Figure 3.7: Simplified circuit model for each phase.....	69
Figure 3.8: Bode plot of the system transfer function.	69
Figure 3.9: System transfer function bode plot with virtual resistance.	71
Figure 3.10: Voltage loop mathematical model with a virtual resistor.....	71
Figure 3.11: Bode plot of the feedback loop transfer function.	73
Figure 3.12: Step response for the whole system.	73
Figure 3.13: System transfer function Bode plot with RL load.....	75
Figure 3.14: Bode plot of the system transfer function at RL load with virtual resistance.	75
Figure 3.15: Bode plot of the feedback loop transfer function with virtual resistance.....	76
Figure 3.16: System transfer function bode plot with RC load.	78
Figure 3.17: Bode plot of the system transfer function under the RC load with virtual resistance.....	80
Figure 3.18: Bode plot of the feedback loop transfer function with virtual resistor for the RC load.	80
Figure 3.19: Simulation results for 2 kW output power.	81
Figure 3.20: FFT analysis of the output phase voltage.....	83
Figure 3.21: Output waveform of the steady-state system with resistive load.	84
Figure 3.22: DC-link capacitor voltage oscillation at different unbalance current ΔI_c	85
Figure 3.23: Dynamic balancing waveform with different loads @ $R_v=4.2 \Omega$	87
Figure 3.24: Three-phase four-wire inverter.....	88
Figure 3.25: Output voltage and current of each phase with resistive load.....	90
Figure 3.26: Unbalanced load test without neutral-point control.	91

Figure 3.27: Unbalanced load test with neutral-point control.	91
Figure 4.1: Various SVM pulse patterns and CMV distribution.	95
Figure 4.2: Modulation signal of SVPWM, AZSPWM, DPWM1, and DPWMMin.	95
Figure 4.3: FFT result for CM modulation signal of SVPWM, AZSPWM, DPWM1, and DPWMMin.	97
Figure 4.4: CMV spectrum of SVPWM, AZSPWM, DPWM1, and DPWMMin.	97
Figure 4.5: DFI integral bounds.	100
Figure 4.6: AZSPWM generation logic.	100
Figure 4.7: DFI integral bounds AZSPWM.	102
Figure 4.8: Comparison of DFI result and simulation.	104
Figure 4.9: CM energy distribution.	104
Figure 4.10: General procedure of DFI analysis for CMV.	106
Figure 4.11: Three-phase current waveform.	107
Figure 4.12: Equivalent circuit for current ripple prediction under different space vectors.	109
Figure 4.13: DM current ripple at various PWMs.	111
Figure 4.14: Current ripple vs. modulation index.	113
Figure 4.15: Current ripple prediction.	113
Figure 4.16: CM- & DM-performance comparison for various PWM methods.	114
Figure 4.17: Current ripple prediction comparison.	116
Figure 4.18: Peak CMC prediction.	116
Figure 4.19: Field-oriented control with HPWM.	118
Figure 4.20: HPWM flow chart.	119

Figure 4.21: Test bench setup.	120
Figure 4.22: CMV measurement.	122
Figure 4.23: CM current spectrum @ f_s	122
Figure 4.24: CMV spectrum with respect to different switching frequency.	123
Figure 4.25: CM current spectrum with respect to different switching frequency @DPWMMin.	123
Figure 4.26: Surface plot of peak CMC with different f_s and MI	125
Figure 4.27: Field-oriented control block diagram.	126
Figure 4.28: CM spectrum @ $f_s=40$ kHz with respect to different CBW.	128
Figure 4.29: CME distribution with respect to different f_c (simulation).	128
Figure 4.30: Measured CMV spectrum with respect to different CBW.	129
Figure 4.31: DM signal spectrum of the three-phase current (simulation) comparison with different control bandwidth.	131
Figure 4.32: Measured CM current spectrum with different CBW.	132
Figure 5.1: Three-phase center-aligned modulation and corresponding CMV.	137
Figure 5.2: Modulation scheme and the corresponding CMV.	139
Figure 5.3: ZCMVM modulation waveforms @ $MI=0.5$	141
Figure 5.4: ZCMVM modulation waveforms @ $MI=0.5$	144
Figure 5.5: ZCMVM pulse manipulation rules in different zones.	146
Figure 5.6: RCMVM modulation waveforms @ $MI=0.906$	148
Figure 5.7: RCMVM overmodulation waveforms.	149
Figure 5.8: Modulation scheme and the corresponding CMV.	151
Figure 5.9: Proposed pulse manipulation method.	152

Figure 5.10: Simulated CMV with ZRCMVM @ $MI=0.3$	154
Figure 5.11: Simulated phase current waveform.	154
Figure 5.12: CMV waveform under high/overmodulation.	156
Figure 5.13: CMV spectrum under high/overmodulation.....	156
Figure 5.14: DC-link capacitor current comparison.	158
Figure 5.15: Differential-mode impact at the output side.....	158
Figure 5.16: Modulation waveform for a MI step change.	160
Figure 5.17: Transient process for region switch.....	160
Figure 5.18: Transient process for speed change.....	161
Figure 5.19: DTM test bench.	163
Figure 5.20: CMV waveform.....	166
Figure 5.21: Dead time effect on CMV.	167
Figure 5.22: CMV comparison between CSVM and ZRCMVM in the linear range.	169
Figure 5.23: CMV comparison between CSVM and ZRCMVM in overmodulation range.	169
Figure 5.24: CMV comparison between CSVM and ZRCMVM at full modulation.	170
Figure 5.25: CMC spectrum comparison in the linear modulation range.....	172
Figure 5.26: CMC spectrum comparison in the overmodulation range (mode-I).	172
Figure 5.27: CMC spectrum comparison in the overmodulation range (mode-II).	173
Figure 5.28: Phase current waveforms.	175
Figure 5.29: Phase current ripple measurement.....	175
Figure 6.1: Three-phase three-level ANPC inverter motor drive system.	180
Figure 6.2: 3L-ANPC CSVM modulation waveform.....	180

Figure 6.3: DFI integral bounds for SVPWM in a 3L-ANPC inverter.....	181
Figure 6.4: Comparison of DFI result and simulation for 3L-ANPC inverter.....	183
Figure 6.5: NTSVM vector plane and reference synthesis.	185
Figure 6.6: DFI integral bounds for NTSVM in a 3L-ANPC inverter.	185
Figure 6.7: Comparison of DFI result and simulation for 3L-NTSVM.....	186
Figure 6.8: Comparison of DFI result and simulation for 3L-NTSVM CMV peak @ f_s . ..	186
Figure 6.9: NTSVM vector plane and reference synthesis.	188
Figure 6.10: DFI integral bounds for RCMVM in a 3L-ANPC inverter.	188
Figure 6.11: Comparison of DFI result and simulation for 3L-RCMVM.	189
Figure 6.12: Comparison of DFI result and simulation for 3L-RCMVM CMV peak @ f_s	189
Figure 6.13: CMV profile comparison.	191
Figure 6.14: CMV spectrum comparison.	191
Figure 6.15: Peak CMV comparison in LW/WM frequency range.....	192
Figure 6.16: DM performance comparison.....	194
Figure 7.1: 3-level GaN-based ANPC inverter prototype.	201

Chapter 1 INTRODUCTION

1.1 Background of Electric Vehicles

1.1.1 EV Overview

Benefiting from advances in battery technology, evolved automotive industry, electric grid automation, and artificial intelligent (AI)-driven autonomous techniques, the global electric vehicle (EV) adoption expanded significantly over the last decade. Supportive policies and technological advances have been evoked and proposed continuously for the EV market. Figure 1.1 shows the global EV stock statistics from IEA [1]. EV sales surged by an annual average of 60% in the 2014-19 period, with 7.2 million in 2019.

According to the U.S. Bureau of Transportation Statistics [2], in 2020, EV sales had a fifth consecutive year of growth, as well as the demand. Multiple underlying reasons contribute to the tremendous development of the EV market, including traditional carmakers markets contracted, purchase subsidies policy for buying renewable energy vehicles, and growing consumer expectations of novel technology enhancement and new models.

In addition, EVs are widely believed to be the solution that meets the environmental goals of reducing air pollution and addressing climate change. It is claimed that EVs could displace oil demand of 2 million barrels a day as early as 2023. Considering the growing energy crisis gradually becomes a consensus, the transportation electrification prospects are bright and optimistic.

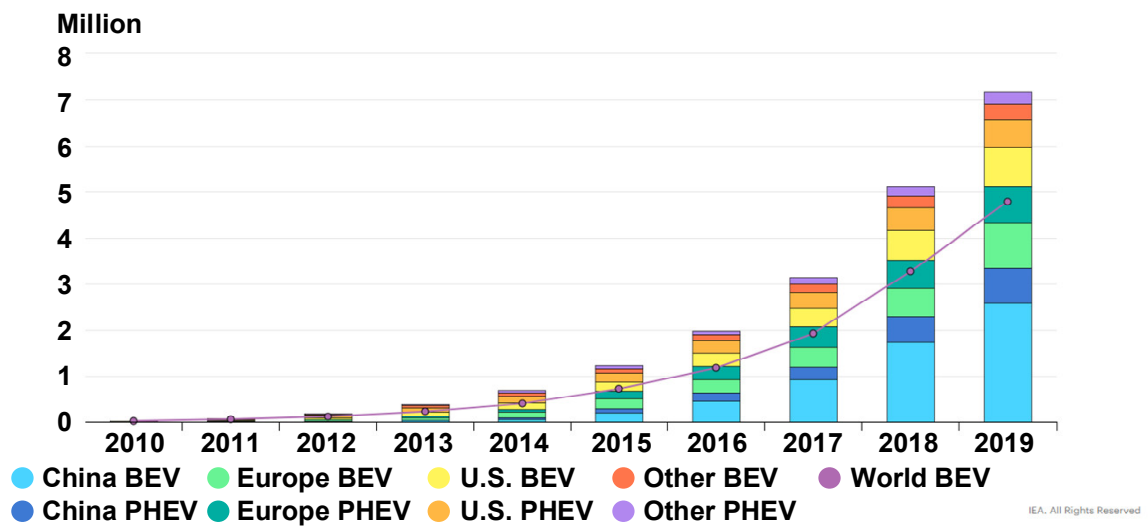


Figure 1.1: Global electric car stock, 2010-19 [1].

As shown in Figure 1.2, the typical electric structure of EVs could be generally divided into several parts: on-board charger (OBC), high-voltage battery, DC subsystem, motor drive system, and high-power propulsion motor. In OBCs and motor drive systems, the two major onboard power conversion devices, the inverters determine how EV interacts with the three-phase AC grid and three-phase AC motors. As EVs are becoming a part of the power grid, the EV battery chargers should have the capability of ensuring the power quality of the grid [3, 4]. Meanwhile, to compete with traditional vehicles, the EV powertrain system should be upgraded with a higher power capability, smaller footprint, and longer durability. All the featured characteristics of EVs are highly determined by the power converter design, more specifically, the inverter. As the interface between AC and DC system, on the OBC side, the inverter plays the role of the power conversion and transfer between grid and DC bus or even forms its local grid during the power grid outage. On the motor drive side, the inverter determines the vehicle propulsion status and affects the motor lifespan if inappropriately designed or controlled. Therefore, the EV inverter design and control are crucial for the whole industry's advancements.

1.1.2 EV Charger

As the “fuel station” of EVs, the chargers are the key feature of EVs compared with traditional vehicles. During the development of charging techniques, the charger is specified into three categories: Level-1 (L1), Level-2 (L2), and DC fast charging (DCFC). L1 is slow charging (3.5-6.5 miles of driving range per hour charging) that is oriented to a long-time charging scenario (at home or work). L2 is considerably faster than L1 (14-35 miles of driving range per hour charging), but must be installed in a charging station, which

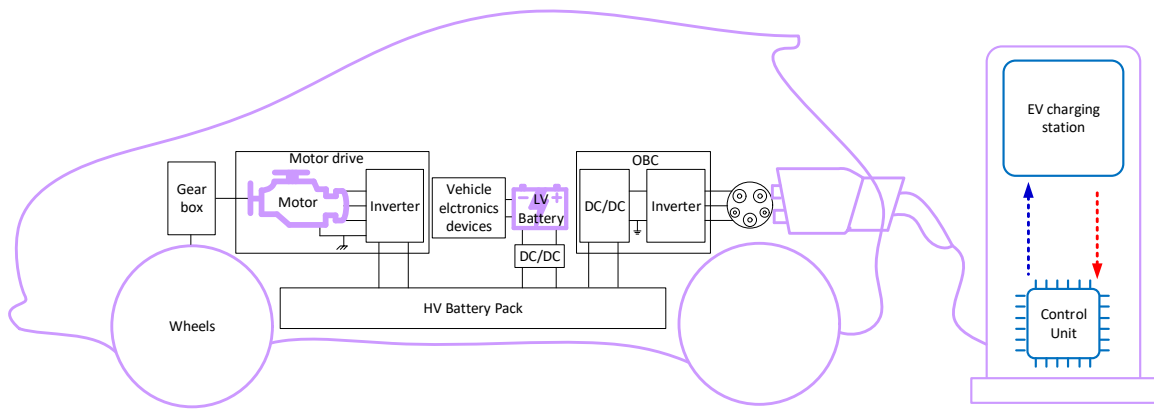


Figure 1.2: Power electronics structure in an EV.

is the replacement of a traditional gas station. L1 and L2 charging use a universal connector (standard J1772 or Tesla connector) that can be plugged into any EV. DCFC provides the fastest charging speed (up to 100 miles of driving range per half-hour charging) with a high-voltage DC connection, say 480 V DC. Mostly commonly used DCFC examples are CHAdeMO, CCS Combo, and Tesla Supercharger [5].

Driven by the ambitious EV market development, the charging infrastructure construction and electric powertrain design become the major topics in EV-related applications, projects, and research. Figure 1.3 shows the SAE and Tesla charging infrastructure distribution in the U.S. as of May 2021 [6]. At the national level, there are 25,000 DCFC and 98,000 L2 charging plugs available in the U.S., for a total of 123,000 charging plugs. Despite the low installation in areas with a low population, the significant efforts and progress that have been made over the past decades in terms of charging stations indicate the new era of EVs has come.

In addition, EV's role has changed to be more than a vehicle to serve the travel demand. The battery property determines that the EVs can act as a distributed energy source. Considering the grid side demand, the OBC should be designed to have the ability for the grid-paralleled operation, outdoor usage, and household electricity supply during the blackout. The inverter in the EV charger must be specifically designed for flexibly dealing with multiple operation modes, such as grid-to-vehicle (G2V), vehicle-to-grid (V2G), vehicle-to-home (V2H), and vehicle-to-load (V2L). EVs in the future will be more like distributed energy storage units than only loads [7]. These features of EV operation modes provide new approaches for efficient and flexible energy utilization [8].

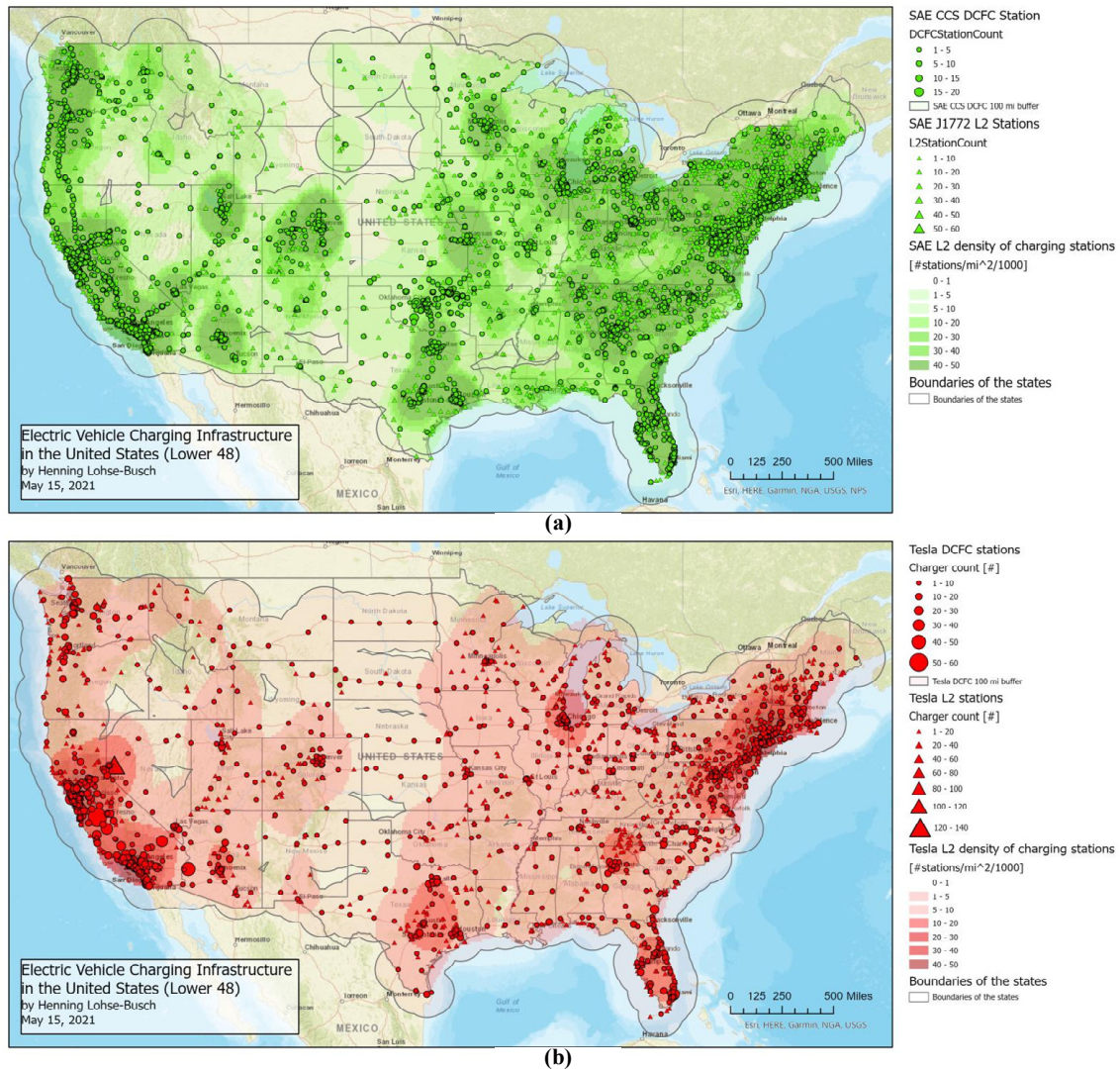


Figure 1.3: Charging network comparison in the U.S.

(a) SAE, (b) Tesla [6].

1.1.3 EV Motor Drive System

Across all sectors, electric motors account for approximately 40% of total U.S. electricity demands [9]. As EVs are developing, such a percentage is only going to be continuously rising. Different from traditional petrol vehicles, the EV propulsion system is dependent on the EV motor drive system. Many types of motors can be used to drive the vehicle, for example, DC motor (DCM), induction motor (IM), and permanent magnet synchronous motor (PMSM).

For EV applications, the motor drive system design is required to have features like high power density, high efficiency in full operation range, high reliability, low cost and high torque in the low-speed range, constant power operation, and fast dynamic response. A conventional motor drive system for high-power applications is usually bulky and occupies significant space.

With the trend of wide bandgap (WBG) devices, the efficiency and power density could be further boosted. According to Onsemi's study, WBG devices, as the next generation of semiconductor devices, are featured in high-performance power conversion, thereby, are also promising in EVs. Figure 1.4 illustrates how WBG devices complement Si devices as well as offer new capabilities for power electronic applications [10]. EV traction and charging are the next target areas.

However, WBG devices increase switching frequency/speed to the motor, causing additional problems, such as electromagnetic interference (EMI) issue. If Si devices are replaced by WBG devices in all power conversion applications, the high switching frequency and high turn-on/off-speed (dv/dt) enabled by WBG devices could increase

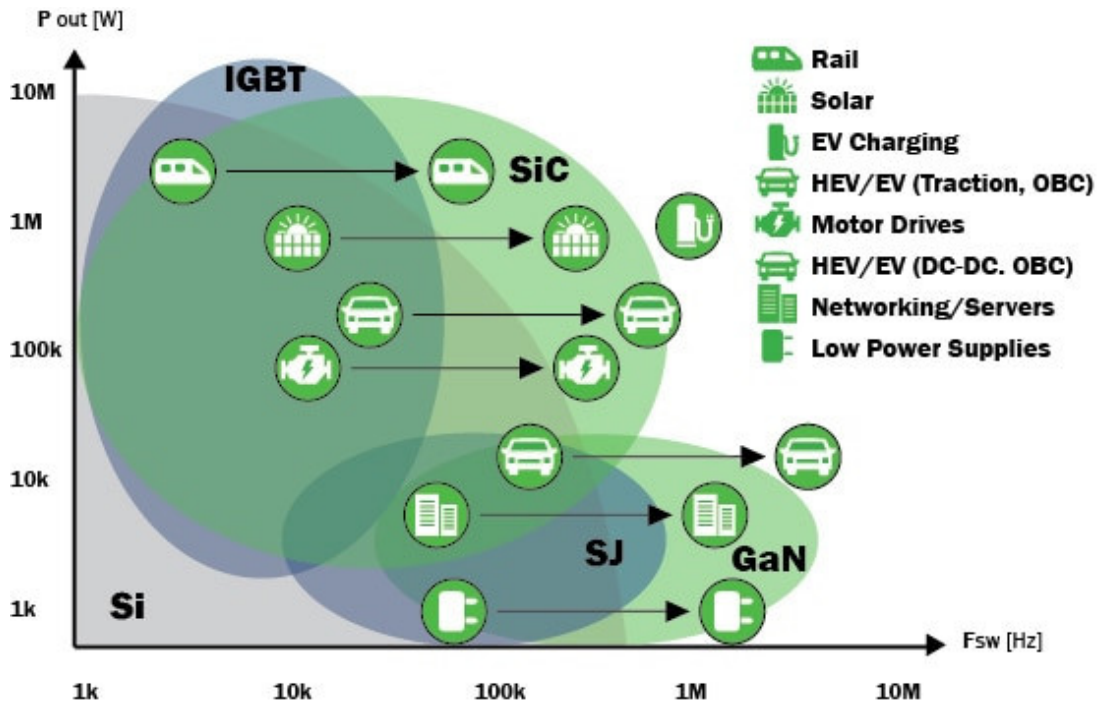


Figure 1.4: WBG Application roadmap in different power conversion scenarios [10].

common-mode (CM) noise emission in the system. Appropriate solutions are needed to limit CM EMI in power converters employing WBG devices. Otherwise, a larger CM EMI filter might be needed, which will ruin the benefits that WBG devices bring to the system in terms of size and volume reduction.

Meanwhile, high voltage batteries became popular in EVs due to the benefit of faster charging and reduced loss. In [11], a comparison has been made between multiple EVs and traditional petrol-driven vehicles in terms of inter-city travel. As shown in Figure 1.5, to have comparable travel time as petrol-driven vehicles, it is required to have a charger power of higher than 400 kW. With extreme fast charging techniques, the output voltage should be at least 800 V [12]. The high DC-link voltage not only enables the extremely fast charging but also leads to a smaller motor current for higher efficiency and smaller cables [13]. However, such high voltage blocking capability is critical to the device from both performance and cost points of view, because the high voltage switch is usually costly and lossy.

One solution is the multilevel technique, given a multilevel system not only lowers the device voltage stress but also enhances the output power quality due to the finer waveform composition compared with the traditional 2-level system.

1.2 Research Objectives and Approaches

1.2.1 Motivation

Based on the introduction above, the onboard inverters for EV applications shall have the following features.

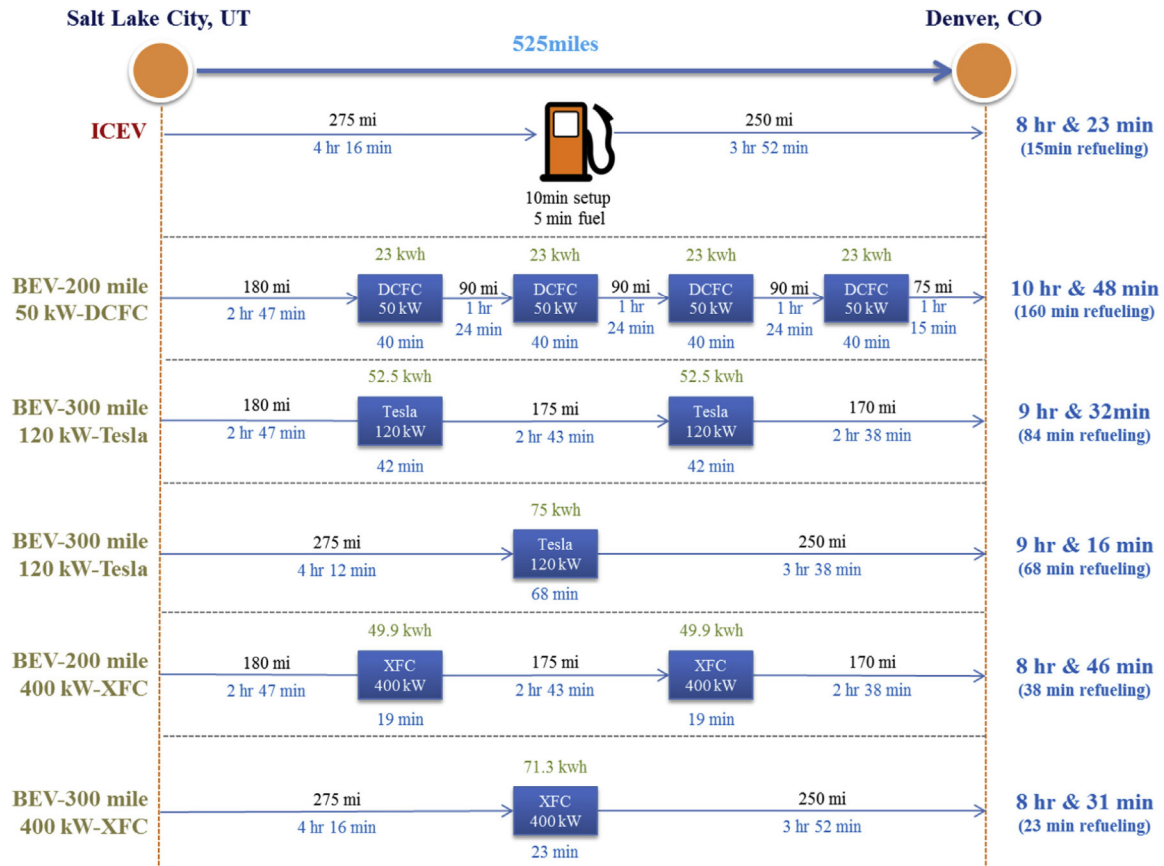


Figure 1.5: Intercity travel from Salt Lake City to Denver [11].

- (1) On the charger side, the inverter should be able to be operated in a vehicle-to-load (V2L) mode to supply the external load, including dealing with unbalanced load for power quality control.
- (2) On the motor drive side, the inverter-caused common-mode (CM) noise should be reduced or eliminated.

With the focus on the on-board inverter power quality and CM EMI performance regulation, this dissertation studies the effective methods for unbalanced load control and characterizes and improves the system CM EMI performance. The research explores the enhancement of onboard inverter performance and stimulates more related research in this area.

1.2.2 Strategy

To evaluate the V2L mode performance, three aspects need to be considered.

- (1) the topology selection, which needs to have the capability of both single-phase and three-phase operation modes.
- (2) Stabilize the DC-link when supplying the external loads.
- (3) The unbalanced load regulation method.

To study the common-mode voltage (CMV) reduction method in a motor drive system, three aspects are noted.

- (1) Compare different schemes that could reduce the CMV.
- (2) Analytically characterize the CMV with respect to different modulation schemes.
- (3) Develop CMV reduction method in a multi-phase and multi-level structure.

1.3 Dissertation Organization

The dissertation is organized as follows:

Chapter 1 introduces the research background, corresponding objectives, and challenges.

Chapter 2 reviews the research activities in the corresponding areas including three-phase inverter power quality control, motor drive method, and CM EMI reduction, as well as multiphase inverter development.

Chapter 3 investigates the V2L mode operation for a three-phase inverter in an OBC as well as the power quality control method. The DC-link capacitor voltage balancing, and unbalanced load control method will be introduced.

Chapter 4 characterizes the CMV for a three-phase motor drive system based on the mathematical model with double Fourier integral (DFI). With the proposed CMV model, the performance of different CMV reduction PWMs will be compared.

Chapter 5 extends the inverter to a six-phase level with a novel CMV cancellation method. The modulation range covers from the linear range to the overmodulation range.

Chapter 6 validates the feasibility of the proposed CMV prediction model in the 3-level system under different 3-level modulation schemes. The corresponding CM and DM performances are investigated and compared.

Chapter 7 summarizes the accomplished work and contributions, as well as the detailed future work.

Chapter 2 LITERATURE REVIEW

This chapter reviews the state-of-the-art of EV charger power quality control and EV motor drive system CM mitigation methods from multiple approaches, such as topologies, algorithms, and filters. Opportunities and challenges exist in these topics.

2.1 EV Charger Power Quality Control

2.1.1 EV and Distributed Energy Resources

EVs have been exhibiting a rapid development in the transportation industry, which is considered to operate at high efficiency thereby high miles per gallon. These promising features make EVs commercially competitive. In addition, as the substitution of fuel, EV batteries have a massive energy storage capacity, which could potentially be utilized as distributed energy sources or backup power supply for households or outdoor usage [7]. For example, recently, the recreational vehicle made by Ford Motor Company has applied this technology to provide electricity for various electric appliances.

When operated under the V2L mode, the EV creates autonomous microgrids, which face challenges when operated under unbalanced and nonlinear loads. Different from the grid-tied application, the load voltage and frequency are not supported by the utility grid. The unbalanced voltage is rich in harmonics, which could cause severe problems on the devices, for example, load current vibration, over-voltage, overheating, etc. [14].

The existing power quality control and unbalanced load methods can be generally categorized into 3 types, active power filters, inverter topologies, and control techniques. Each of these methods will be reviewed in the next section.

2.1.2 General Approaches for Unbalanced Load Compensation

2.1.2.1 Active Power Filter

Theoretically, the caused low power quality problems could be damped by using active power filters (APFs) to compensate for the negative sequence and harmonic voltage [15]. There are three different approaches to categorize APFs, i.e., based on topology type, converter type, and phase (wire) count.

As shown in Figure 2.1, the topology-based APF is categorized into the shunt APF (ShAPF), series APF (SeAPF), and hybrid APF (HAPF). APFs reduce the negative sequence harmonic voltage caused by the system resonance [16], which improves the terminal voltage quality of electrical utilities because of the high voltage utilization rate, as well as the high reactive power compensation to avoid voltage drop. However, installing APFs for each EV will be heavy and costly.

2.1.2.2 Inverter Topology

Instead of installing APFs, the topology selection and the corresponding control strategies for unbalanced load compensation are preferred. Most inverters have the neutral connected to the ground for safety concerns, where the zero-sequence current could circulate in the system. To eliminate the zero-sequence current, a Δ -Y transformer [17] or zigzag transformer [18] could be used as shown in Figure 2.2 and Figure 2.3. However, line frequency transformers are usually too heavy and costly to be desired in general applications.

Different from the three-leg three-wire system, the four-wire structure offers more freedom. The fourth wire is connected from the neutral point to the middle point of the split

DC-link capacitors (three-leg four-wire) or the middle point of the additional phase leg (four-leg four-wire). These two types of four-wire topologies are shown in Figure 2.4.

In the three-leg four-wire system, each leg could be controlled as three single-phase half-bridge inverters independently [19]. Therefore, the adjustment of each phase with SPWM will be straightforward and accordingly to the slightly unbalanced load. However, under severe unbalanced and nonlinear load, a large neutral current will flow through the neutral path and result in a perturbation in the control loop. Another issue of such a structure is the voltage unbalance of the two large DC-link capacitors connected in series [20].

In [21], a three-phase inverter with split DC-link capacitors is proposed. Two three-phase inverter topologies are proposed. As shown in Figure 2.5, one is with split DC-link capacitors, and another is with a neutral leg connection to the ground through a neutral inductor. For the split DC-link capacitors, the structure is simple, but the capacitance will be impractically high as all the neutral current will flow through the DC-link capacitors, especially under the unbalanced load, not to mention the likely neutral point shifting issue. For the neutral leg inverter, the neutral point is stabilized, and the voltage utilization rate is around 15% higher. However, the additional phase leg cannot be controlled independently to sustain the neutral point, which results in much-complicated control schemes, such as 3D space vector modulation [21-23].

One concept is that the two topologies could be further combined to form a new topology. Inspired by this, as shown in Figure 2.6, reference [24] realizes the classical control of the combined topology. A simple controller modeling and design is proposed. The neutral point control is decoupled from the three-phase inverter. References [25] and

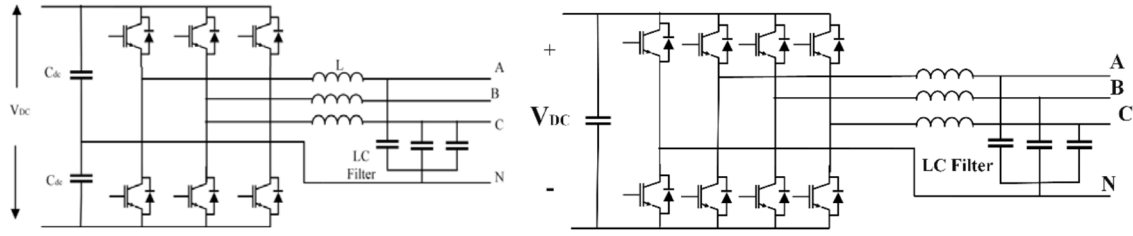


Figure 2.4: Three-phase topologies.

Left: With split DC-link Capacitors, Right: With the four-leg.

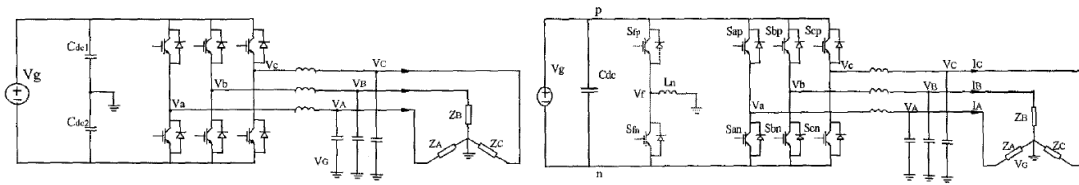


Figure 2.5 Three-phase Inverter neutral structure.

Left: With Split DC-link Capacitors, Right: With a neutral leg [21].

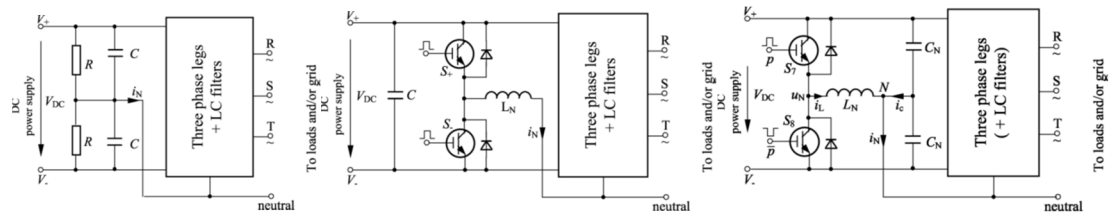


Figure 2.6 Neutral point connection method of three-phase inverters.

Left: 4-wire with split DC-link, Middle: 4-leg converter, Right: 4-leg 4-wire [24].

[26] pointed out that even though we can use a three-phase four-leg inverter by simply adding one more bridge, the fourth leg is high-frequency operated. As a zero-sequence path is provided, the caused CM EMI noise will appear. Though for V2L, the CM noise is not the main concern.

In [27], another discussion on the combination of the split dc-link and the fourth leg is performed as shown in Figure 2.7. A 9 kW three-phase four-wire inverter is designed with a split DC-link capacitor and neutral inductor. The optimized neutral inductor and filter inductor are proposed. The output voltage closed-loop control in the $\alpha\beta 0$ frame is presented to suppress the 3rd order harmonics. However, the light load performance was not mentioned. In addition, the filter inductor is 3 mH and the neutral inductance is 2.8 mH, still relatively large due to the low-switching frequency.

2.1.2.3 Unbalanced Load Control Strategies

In this section, various control strategies aiming at unbalanced load compensation are described. Different compensation characteristics are achieved.

For all three-phase structures, one general control strategy is symmetrical-component-based. This strategy originated from the symmetrical sequence decomposition [28]. According to the superposition principle, for any three-phase power system under both balanced and unbalanced conditions, the three-phase phasors could be formulated as a linear combination of three symmetrical sets of phasors through a complex linear transformation. One set of phasors has the same phase sequence as the original system (positive sequence), the second set has the reverse phase sequence (negative sequence), and the third set has the phasors in phase with each other (zero-sequence). As a result, three

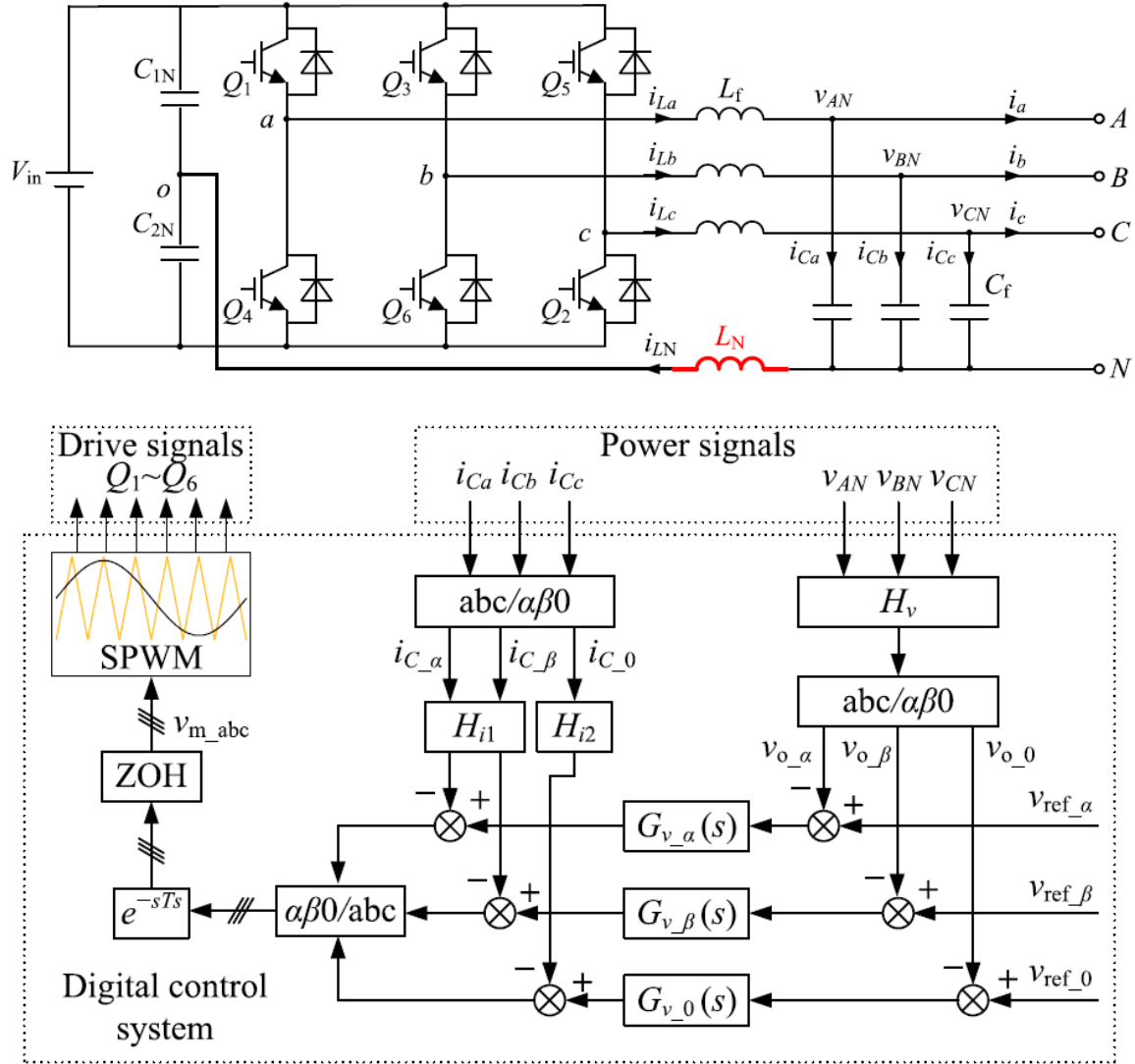


Figure 2.7: Three-phase four-wire inverter with split DC-link capacitors.

Top: Topology, Bottom: Control block diagrams [27].

unbalanced phasors are converted into three independent phasor sets, which simplifies the asymmetric load analysis.

In the conventional control strategy, the voltage and current are decomposed into dq0 components in a rotating reference frame. Under a balanced load, the d/q components are DC constants, and the 0 component is zero. Under an unbalanced load, the double line frequency disturbance will appear as the negative sequence in the d and q components while the zero sequence stays stationary.

In [29], to control a four-leg inverter, a symmetrical sequence decomposition-based control method is proposed to independently regulate the output voltage and current. In the dq0 frame, each component is controlled accordingly as DC components [30]. According to the symmetrical component decomposition, the unbalanced voltage and current are decomposed into three sets of sequences, then transferred into the dq0 frame. Through this process, the independent control is realized for three different sequences. As shown in Figure 2.8, the first channel controls the positive sequence of voltages and currents in a positive frame. The second channel regulates the negative sequence of voltages and currents in a negative frame. The third channel still compensates for the zero sequence components in a negative frame, which is realized by 120° spatially displacement of the zero-sequence [31]. Finally, the conventional PI controller is utilized in the voltage and current control loops.

In [32], a load unbalance compensator (LUC) is proposed to control a three-phase four-leg inverter as shown in Figure 2.9(a). When unbalanced currents occur in the standalone microgrid, the corresponding unbalanced current is injected into the loads for compensation. With ABC/dq0 transformation, the positive and negative current sequences

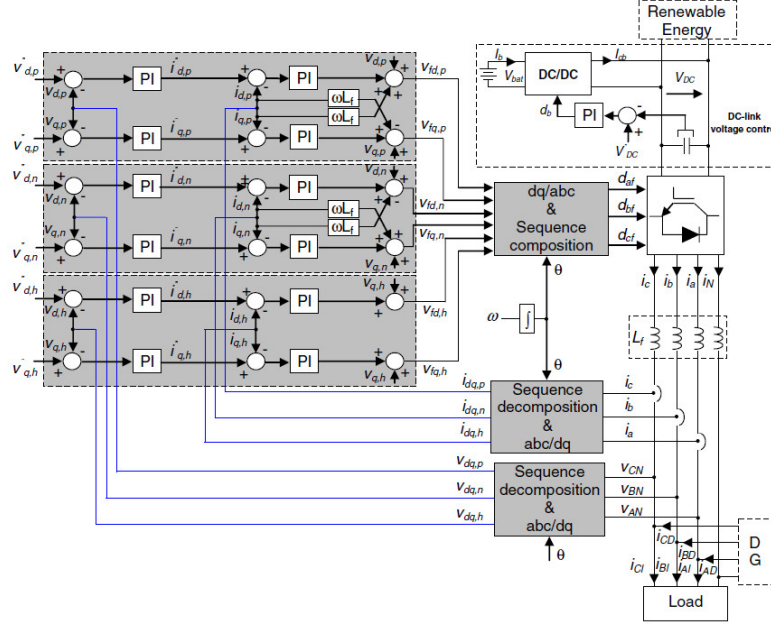


Figure 2.8: Control strategy of a 4-leg inverter with symmetrical components [29].

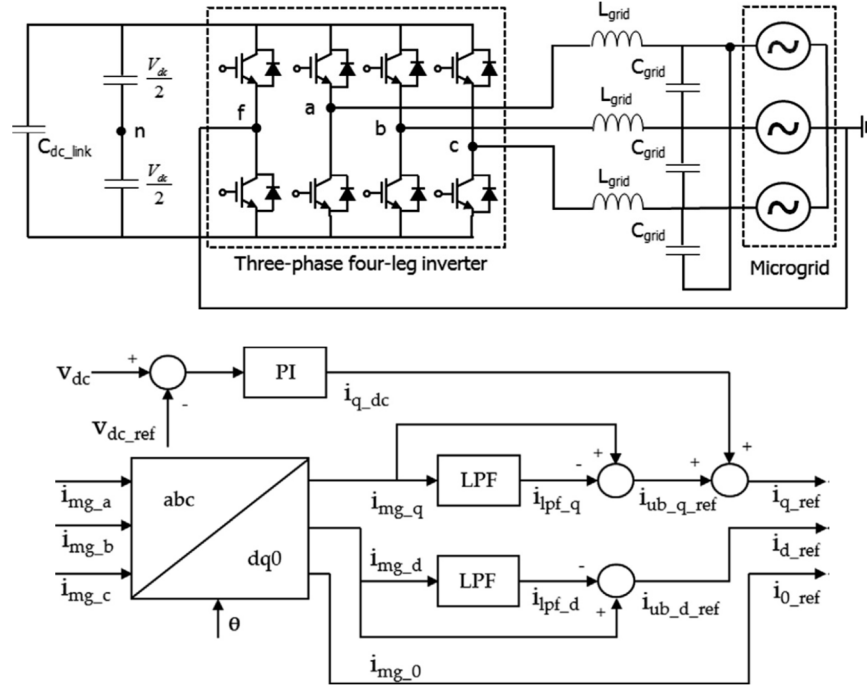


Figure 2.9: A three-phase 4-leg inverter with the unbalance compensator.

Top: Topology, Bottom: Control algorithm [32].

of the unbalance current have AC harmonics in the dq reference frame. As shown in Figure 2.9(b), this could be extracted with a low pass filter. PI controllers are used to eliminate dq current components. A feed-forward loop considering grid voltage and inductance voltage is applied to improve the steady-state and dynamic performance.

Compared with coordinates transformation, which controls the three-phase as one reference, regulating each phase as an independent reference is also possible and more straightforward. Such a method is named the per-phase control method. As each phase voltage and current are controlled independently, each phase should have a common reference point, therefore, it is only valid in the three-phase four-wire inverters, where there's a neutral line.

Some recent research literature on V2L includes the fuzzy logic control in V2L applications [34] which introduces the priority of charging and discharging when using EV batteries to support the grid. Bidirectional V2G and V2L chargers are proposed in [35], as shown in Figure 2.10(a), a single-phase battery charger diagram with bi-directional capability. By scanning a sine table as the reference voltage, a voltage mode controller is designed by adjusting the duty-cycle value of the PWM modulator. In [36], a similar topology is proposed but with two types of AC output standards (120 V for normal households and 240 V for heavy-duty loads) by a split-phase transformer. As shown in Figure 2.10(b), by controlling the phase-leg A and B with two identical capacitor current loops, where each current loop owns a voltage outer loop with a PR controller. Each current loop output will control one half-bridge while the neutral branch is switching with a 50% duty cycle. However, such a control strategy is simple but vulnerable to electric faults, further fault analysis and system dynamic response are not performed. In addition, the

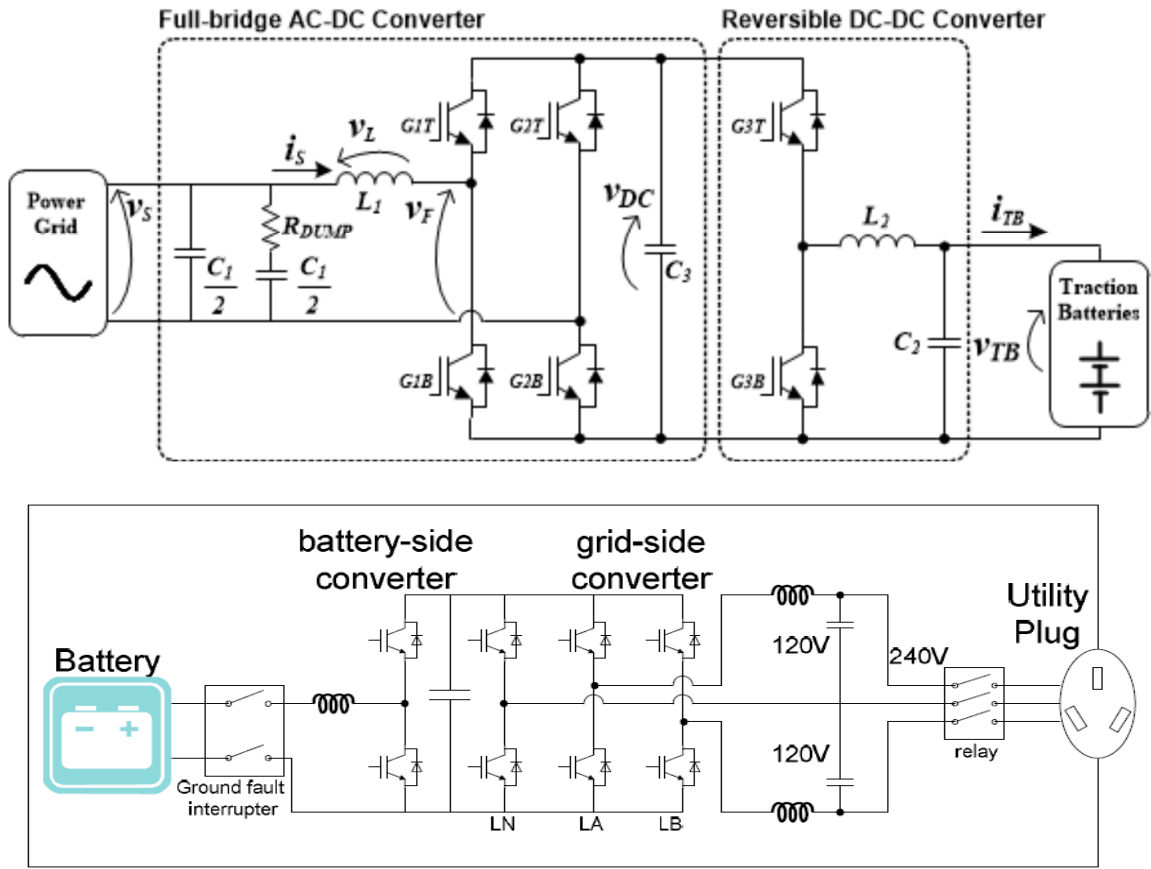


Figure 2.10: Bidirectional charger topologies.

Top: Single-phase bidirectional converter,
 Bottom: Three-phase bi-directional charger [40, 41].

single-phase structure has limited power supply capacity and flexibility to external load supply.

Digital filtering is one important solution to secure power quality. A notch filter, also known as virtual damping, has been studied by many publications. In [33], the author presents a control technique suitable for AC generators by adding a virtual bleeding resistor. As well as a repetitive-based voltage harmonics abatement to enhance the quality of the output voltage. Reference [34] based on the standalone voltage-source inverter (VSI) with an LC filter, applied a virtual resistor in the system to damp resonance and enhance the quality of the output voltage. However, there is no analysis for the three-phase unbalanced load. The dynamic performance is not addressed either. To suppress harmonics of the output voltage and current, a notch filter is widely used in inverter applications, which was initially implemented in [35], where genetic algorithms have been adopted to fine-tune the notch filter. In [36], a novel active damping control strategy with a notch filter is proposed and the design method of notch parameters is also given. In [37], the adaptive notch filter was used only for decomposing the current of nonlinear loads into harmonics, active, and reactive current. Reference power generation by an inverter under ideal grid voltages using an adaptive notch filter (ANF) is presented in [38]. Chilipi et al. in [39] proposed the notch filter-based control scheme for reference power generation and power quality control, which is not vulnerable to grid voltage distortions and can always ensure clean and balanced grid current. The control scheme is shown in Figure 2.11, where an ANF is inserted to the positive and negative sequence control loop. Again, the question remains on how to apply notch filters in V2H/V2L mode, especially in the unbalanced load condition. Which is less addressed and is one of the scopes of this dissertation.

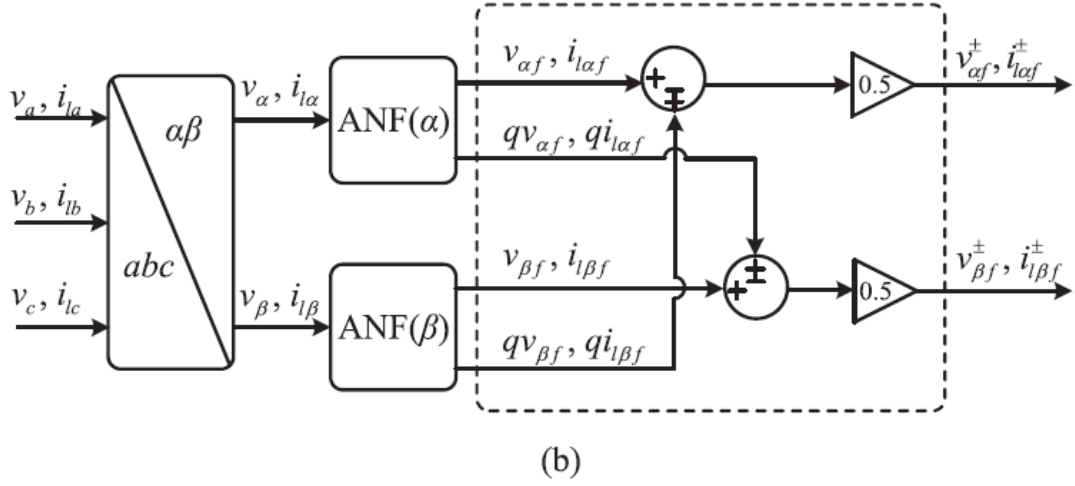
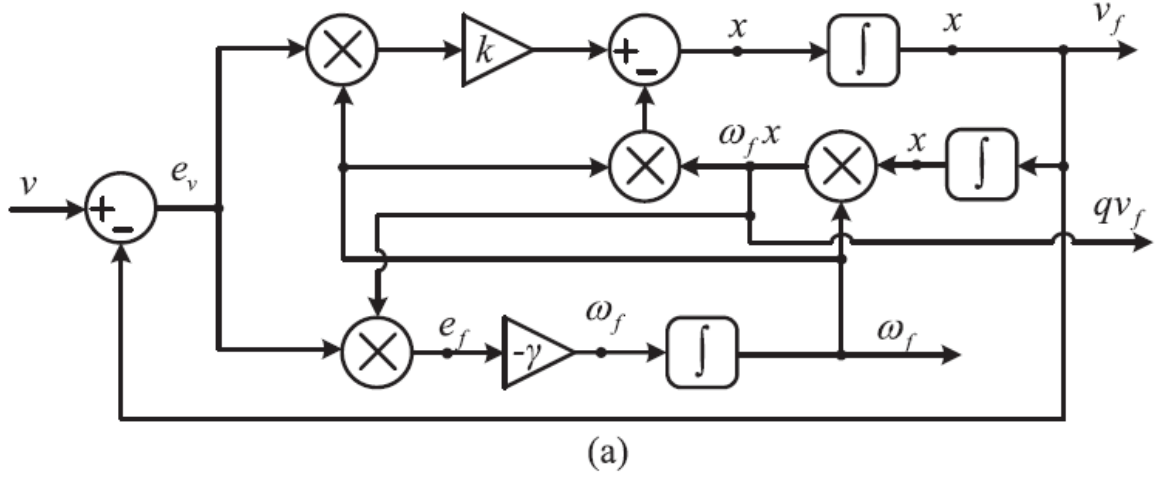


Figure 2.11: ANF control diagram.

(a) ANF, (b) ANF-based positive and negative sequence components extractor [39].

2.2 Motor Drive System and CMV Mitigation

2.2.1 Motor Drive System and the Origin of CMV

As the heart of EVs, the motor drive system has to operate in a harsh environment with the humidity of up to 85% and the ambient temperature ranging from -40 and 135 °C [42]. With a high driving duty cycle, wide constant-power range, and high torque density, the motor lifetime is critical. As a major cause of motor lifetime shortening, CMV in electric drives generates leakage current, which consequently results in EMI problems, power loss, and damage to motor insulation.

A three-phase voltage source inverter (VSI) is commonly used in AC motor drive systems, driving permanent magnet synchronous motors (PMSMs) or induction motors [43]. A conventional 2-level three-phase inverter-fed motor drive system containing 6 switches (S1~S6) with two complementary switches per leg is shown in Figure 2.12.

The motor case and the middle point of the DC-link are typically grounded to the chassis for safety [44]. Between the AC neutral and grounding chassis, the parasitic capacitor (C_s) and the cable-to-ground parasitics provide the path for the CM current (CMC). Thus, the CM noise is a type of electrical noise that has been induced by power electronics converters with respect to the reference ground [45]. Ever since the PWM inverter is implemented in variable-speed motor drives (VSD), the CM EMI issue drew a lot of attention due to the significant EMI emission and negative effect on the motor drive system [46, 47]. It becomes only worse with the fast-switching WBG devices. In a conventional 2-level drive system, the CMV could be generally formulated as:

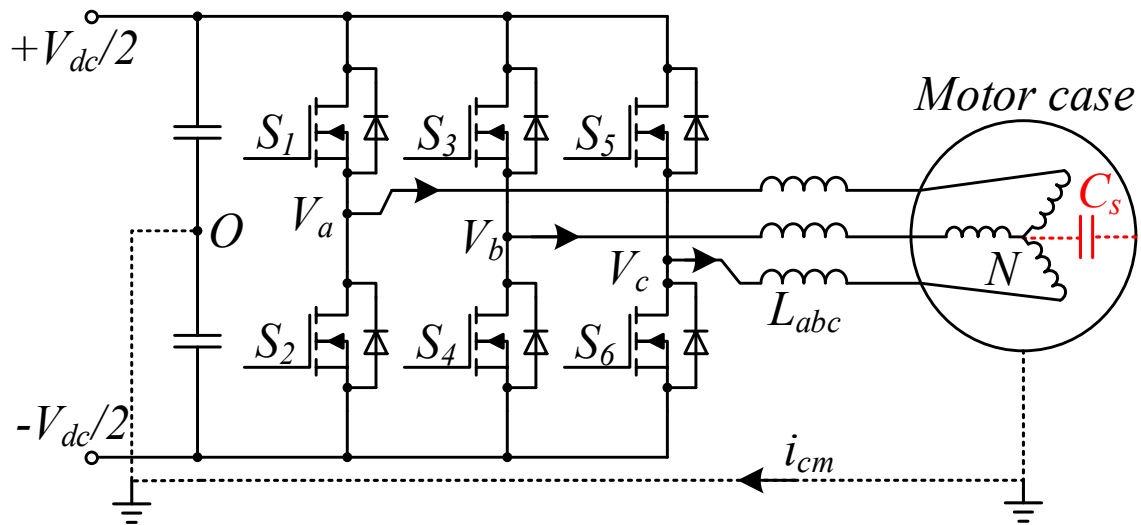


Figure 2.12: Three-phase two-level VSI motor drive system.

$$V_{CM} = (V_{ao} + V_{bo} + V_{co})/3 \quad (2.1)$$

The CMV contains a number of harmonic components. These CM components not only lead to signal distortion in the local system but also interfere with other devices through common ground and cause disturbance [48]. In the motor drive system, the shaft voltage resulting from the CMV source can be problematic. A shaft current path in the motor system is shown in Figure 2.13. Typically, the motor bearings are oil-lubricated, which has insulation between the shaft and bearings. However, in the high-voltage application, especially in the motor starting process, if the lubricant film has not well covered the bearings, the shaft voltage will break down the film and generate significant-high current. Due to the small metal contacting surface between bearings and shaft, the current density is high enough to partially damage and melt the surface, the spilled high-temperature melted bearing alloy will cause a series of small pits on the inner surface of the bearing rings, thereby wearing the mechanical structures and subsequently causing the insulation failure and shortening the motor lifetime, also known as premature failures.

As WBG devices gradually become the alternatives for Si devices, the operating frequency also inevitably increases to achieve better power density and efficiency. However, the increased EMI issue is also coming with it. To meet the strict EMC regulations to be compatible with complex electronics systems in EVs and prolong the motor lifetime, plenty of work has been done on the CM noise mitigation techniques in the past 30 years. Some of which have been widely recognized and implemented in industrial applications. The existing CM noise (CMN) mitigation methods for the DC-fed motor drive can be generally classified into 5 categories: CM filters, gate drive techniques, modulation schemes, inverter topologies, and PCB layout, as organized in Figure 2.14.

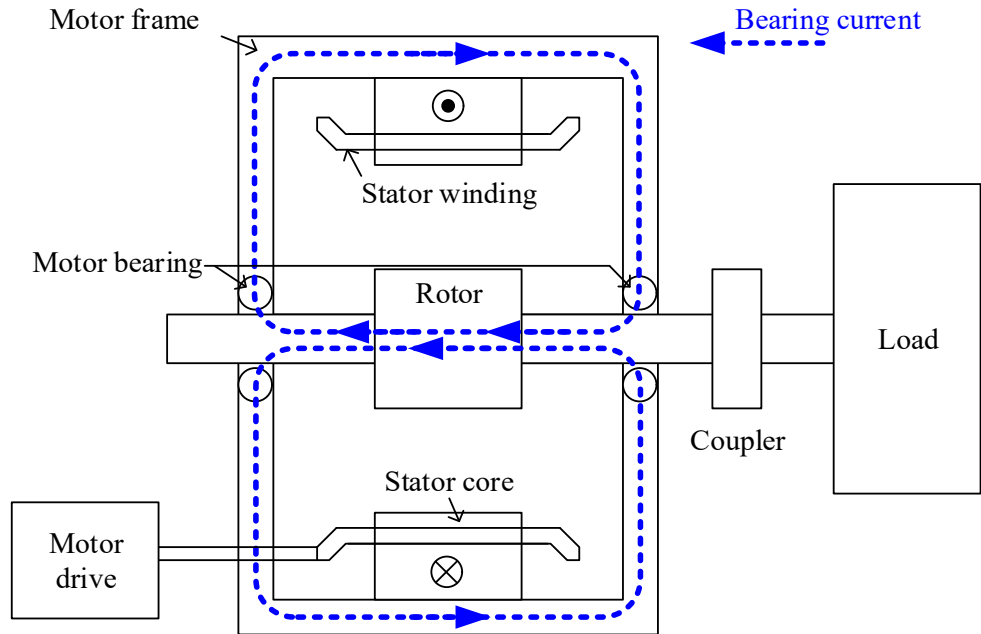


Figure 2.13: Motor shaft current path.

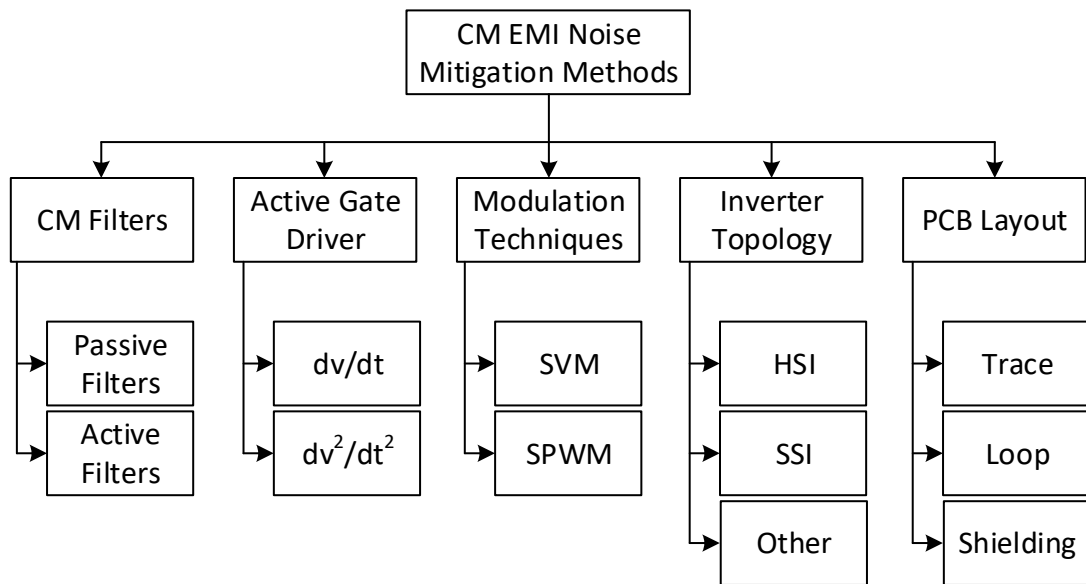


Figure 2.14: CM EMI noise mitigation methods categorization.

2.2.2 General Approaches for CM EMI Mitigation

2.1.2.1 CM Filters

CM filters are widely adopted in most power electronics converters to alleviate the CM EMI issue [49-54]. The typical solution is to install CM choke and Y-capacitor in the CM path to adjust the CM impedance, thereby providing CMC re-distribution or attenuation. As a result, less noise will appear on the motor side or EMI measurement parts (e.g., line impedance stabilization network (LISN)).

Generally, there are two types of CM filters: passive CM filters and active CM filters. Passive CM filters, just as the name implies, consist of passive components. The basic passive components are CM inductors (also known as CM choke), CM capacitors (also known as Y-cap), and CM transformers. Figure 2.15 gives the general circuit diagram of each component.

By using the combination of the CM filter components, various CM filter topologies are created. The most conventional topology with CM filter implemented for motor drives is as shown in Figure 2.16 [55, 56]. There are two CM filters, one on the DC- and the other on the AC side, respectively. Between the DC input and DC bus, the LC-type CM filter could help to attenuate the DC-side CMN on the LISN to meet the required standard. A three-phase CM choke is installed in the AC line to reduce the CMC flowing through the three-phase path and motor.

Figure 2.16 shows the single-stage CM filter insertion. In reality, according to specific EMI standards, the CM filter could be two or three stages. With different combinations, the multi-stage filters can be named C-, LC-, LCL-, or LCLC-type.

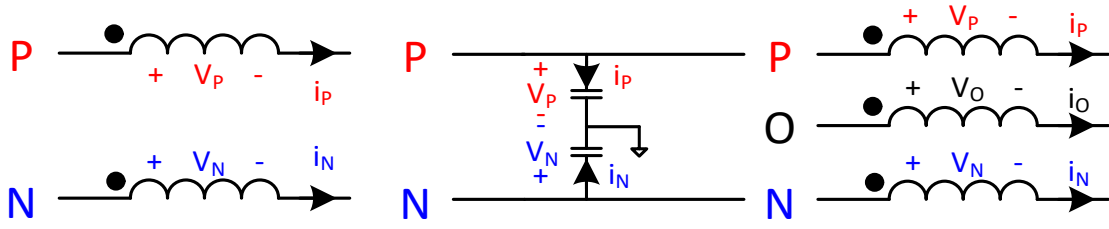


Figure 2.15: Circuit diagram of three major passive CM filters.

Left: CM inductor, Middle: CM capacitor, Right: CM transformer.

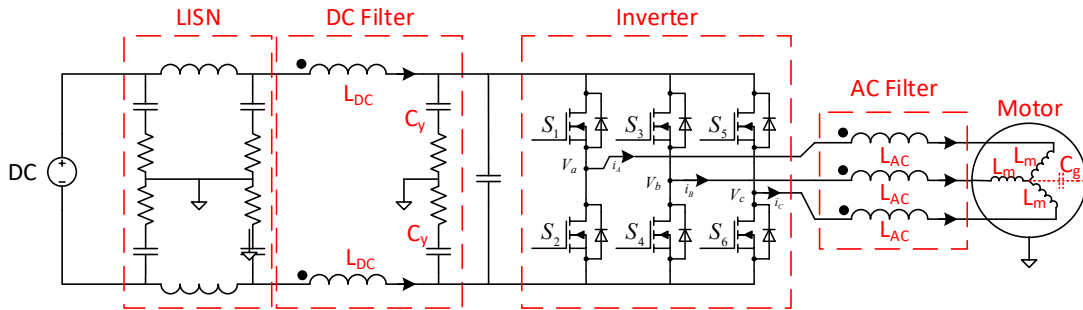


Figure 2.16: Typical motor drive system with CM filters incorporated [56].

Passive CM filters are quite easy to implement and design, as well as exhibit high reliability [57]. However, CM filters are all inserted in the power flow path, which will inevitably undertake the same power stress as the inverter and motor. This will not only generate significant losses but also result in bulky and heavy passive components. Generally, the properly designed CM filter will still take up 10% - 25% of the overall motor drive system volume [44, 58, 59]. Therefore, although WBG devices enable higher system operating frequency and reduce the size of the passive components, the increased CMN also requires a larger CM filter, discounting the benefits of system size shrinking enabled by WBG devices and imposing a significant penalty on the system power density.

As for active CM filters, different from passive CM filters, active CM filters not only contain passive components but also have semiconductor devices [60-62]. Such a combination is a promising approach to overcome bulky passive filters because the stop frequency of passive filters should be set as high as needed to secure a wide range of EMI filtering. Figure 2.17 show the implementation of feedforward type voltage-detecting and current-detecting active CM filters respectively.

In the voltage-detecting type, the stepped-down CMV is detected on the AC line through a voltage divider. The detected voltage is then fed to a class-AB amplifier with diode biasing, which is designed with a unity gain, i.e., a voltage follower. The advantages of such voltage detection are high efficiency and low crossover distortion. The amplified voltage signal is received by a voltage CM transformer (CMT), with its secondary winding in series connected in the DC loop. Therefore, with a proper design of the voltage-divider ratio and CMT turns, the CMV can be canceled out by injecting an opposite signal in the CM path. The disadvantage of this implementation is mainly concerned with high voltage

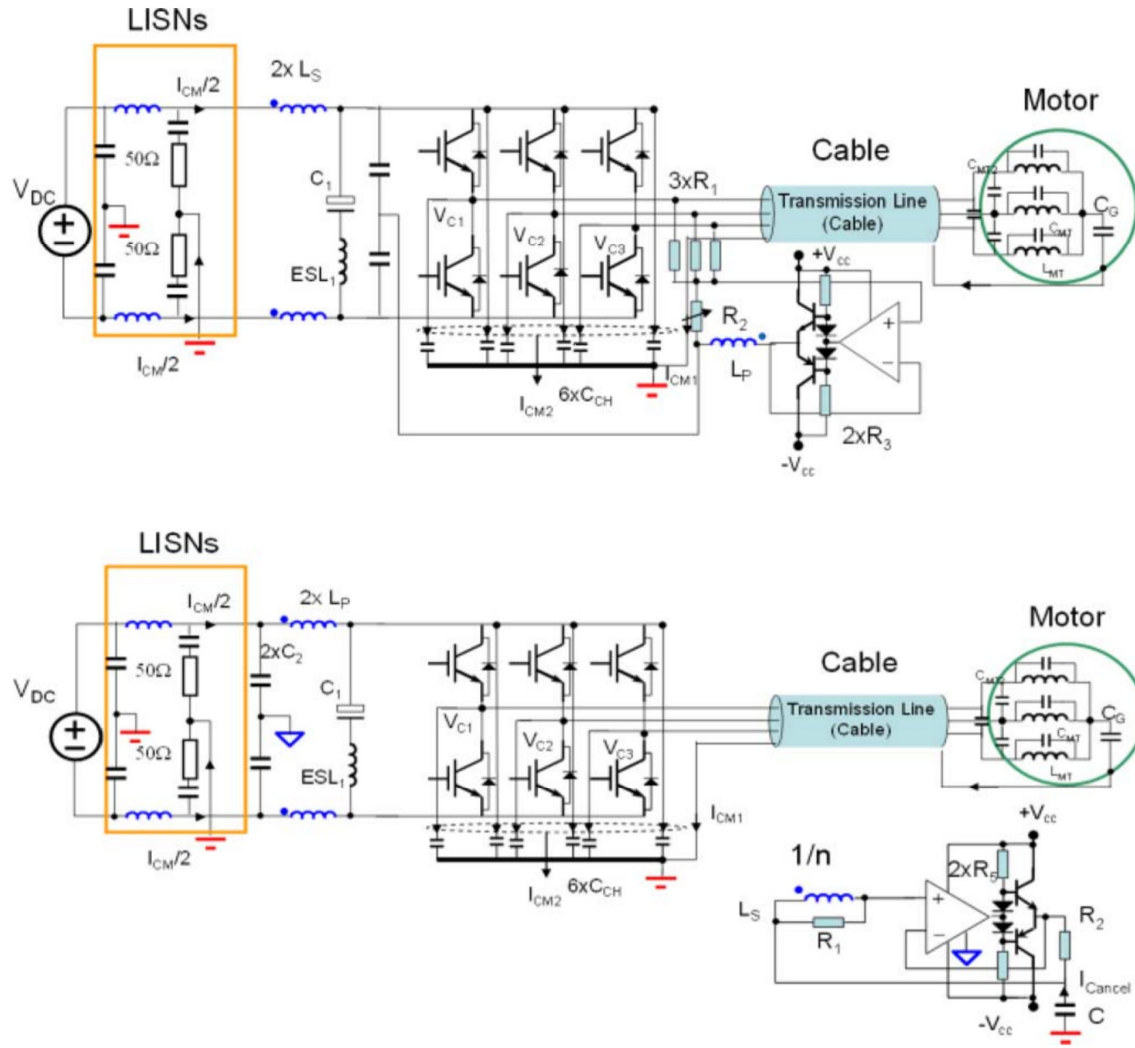


Figure 2.17: Implementation of feedforward CM noise voltage cancellation [62].

Top: CM voltage cancellation, Bottom: CM current cancellation.

applications, where the primary winding of the CMT can be very big to avoid the large magnetizing current, while the secondary side winding inductance will also be large due to the high turn ratio of the CMT. As a result, the size and weight of the CMT will be significant. In the current-detecting type, the CMC is detected on the DC line through a current CMT, the sampled current will generate a voltage drop on the paralleled resistor R_1 , which will then be fed into the amplifying stage. Such that induces current on the output resistor R_2 and send back to the input side for comparison. The excessive current is injected into the ground through the grounding capacitor C for CMC cancellation. Note that the grounding point is connected to the DC bus middle point and all Y-cap common points. Compared to the voltage cancellation method, the current CMT only needs 1 turn on the primary winding, resulting in a significant reduction in the size and weight of voltage CMT.

In summary, active CM filters consist of both passive components and active switches. With appropriate compensation control on the switching devices, the passive components do not need to be as bulky as using passive filters only. Usually, active filters reduce low-frequency EMI noise, and passive filters reduce high-frequency EMI noise. The hybrid combination enables the size and weight reduction compared to the filters that use passive components only because the passive filter does not need to be designed to cover a wider frequency range. However, the design of active filters introduces the complexity of system control because of the requirement of precision, attenuation, and quick response. Some active filtering methods are also subject to the system rating as they require corresponding current or voltage detection, which introduce considerable power loss.

2.1.2.2 Gate Driving Techniques

For power switching devices, the gate drive profile directly determines the corresponding switching behavior, thereby affecting the CMV spectrum of the inverter. Direct adjustment of the turn-on/off gate resistances could reduce the di/dt for the switching transient, therefore, limiting the voltage overshoot and reverse recovery issue, as well as the conductive EMI noise reduction [63, 64]. However, the optimization of the gate resistance also brings significant performance degradation in switching speed and switching loss because of the slowed switching transient (dv/dt). Therefore, active gate drive (AGD) techniques have been carefully studied in the literature [65-68]. The main idea of AGD is to trim or smoothen the switching transient.

Gate drive techniques serve for switching devices, thereby also related to the CM EMI emission. It is known that the fast-switching capability of WBG devices enables size shrinking of passive components, however, leads to high dv/dt as well as the CM EMI, which could be even more severe for a medium voltage motor drive system [69]. Reference [70] did the comparison of CM EMI emission between GaN HEMT-, SiC MOSFETs- and Si IGBTs-based drive systems in the conductive EMI range. The switching speed comparison between SiC and Si, GaN, and Si are shown in Figure 2.18. WBG devices have superior switching speed. However, in the measured conductive CM EMI spectrum, as shown in Figure 2.19, WBG devices only emit a few decibels more noise than Si devices. Virtually no difference can be observed in most of the frequency ranges. In contrast, the spectrum of higher switching frequency is higher than that of the lower switching frequency curve over the whole testing frequency range. When expanding the spectrum to the radiative frequency span, as illustrated in Figure 2.20, the GaN-based drive eventually

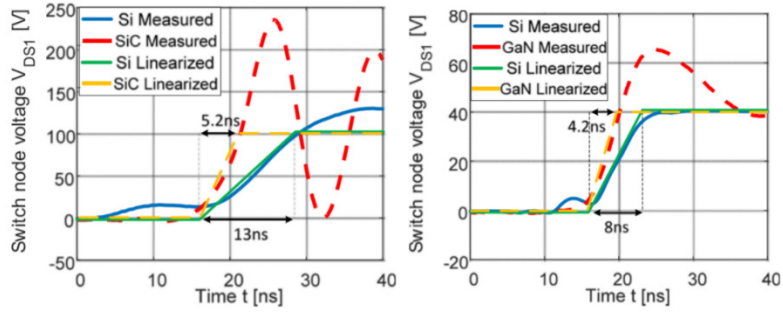


Figure 2.18: Switching node voltage comparison.

Left: Si IGBT vs. SiC MOSFET, Right: Si IGBT vs. GaN HEMT [70].

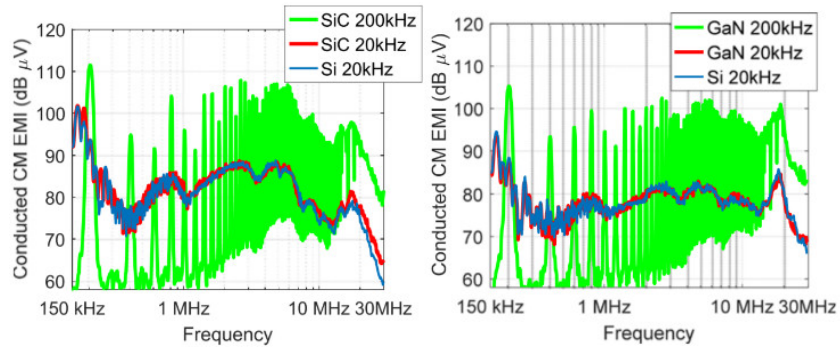


Figure 2.19: CM EMI emissions comparison.

Left: Si IGBT vs. SiC MOSFET, Right: Si IGBT vs. GaN HEMT [70].

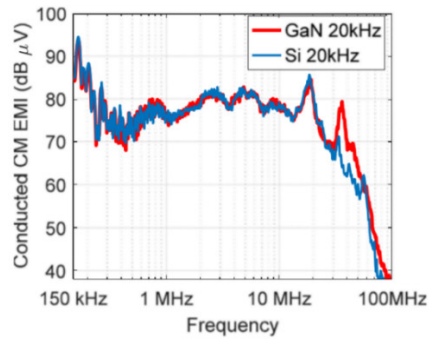


Figure 2.20: Comparison between the CM EMI emissions of Si MOSFET and GaN HEMT-based drives at an extended frequency range [70].

has higher EMI emission than the Si-based drive beyond 30 MHz. However, in motor drive applications, only conductive EMI is concerned, i.e., the influence of dv/dt on the CMN spectrum is very limited in the conductive EMI range where the motor drive is concerned, whereas the impact of switching frequency is more prominent.

According to the review, limiting the switching speed does not help much with the CM EMI noise mitigation. In fact, reducing high dv/dt to reshape the switching profile is a conflict to enable fast switching devices in the modern power electronics area. Therefore, this dissertation will skip the detailed review of this approach. A direct conclusion of the gate-drive-based CM reduction technique is given instead. The gate drive techniques aiming at EMI reduction will sacrifice the switching loss and increase application difficulties. While its actual impact on the CMN spectrum is barely limited in the radiative EMI range. Thus, promoting the AGD techniques to industrial applications is still challenging.

2.1.2.3 Modulation

CMV originates from the switching behavior of the inverter, i.e., the PWM switching pattern has a significant impact on the inverter CMV. Therefore, a series of improvements to the PWM schemes were proposed for motor drives [71]. The distinct competitive advantage of the PWM schemes based on CMV reduction is that no extra circuit is needed, except for the improvement of software control.

Typically, there are two different categories of CMN reduction PWM techniques. One is named reduced CMV PWM (RCMV-PWM), which is realized by avoiding the usage of zero-state vectors in the space vector PWM (SVPWM) technique, resulting in the CMV amplitude reduction from $V_{dc}/2$ to $V_{dc}/6$, where V_{dc} is the DC bus voltage. Another

type is named random PWM (RPWM), which could average out the peak value of the CMN spectrum by randomly determining the switching period and switching patterns. The random PWM techniques were carried out for harmonics reduction for the inverter output voltage in the very beginning which reduces the susceptibility of the system to vibration and acoustic noise in the supplied drive systems. Since this literature review is focused on the CM EMI noise reduction rather than DM noise, the RPWM part will not be addressed.

The essential approach of RCMV-PWM is using active switching states (V1-V6) only but avoiding zero-state vectors (000 or 111) so that the peak value of the CMV could be reduced from $V_{dc}/2$ to $V_{dc}/6$. Various kinds of RCMV-PWMs have been proposed based on the zero-vector replacement [72-76].

Reference [77] has proposed an RCMV-PWM method that uses only three odd states (V1, V3, V5) or three even states (V2, V4, V6) to synthesize the reference voltage vector. Because this modulation method uses three states that have a 120° difference from each other instead of using the states that are close to the reference in SVPWM, it is named remote state PWM (RSPWM). As shown in Figure 2.21(left), compared to the conventional SVM, the sector division frame has been rotated by 30° for the proposed RCMV-PWM. Thus, the CMV in odd sectors (1, 3, 5) is maintained at $-V_{dc}/6$, while in the even sector (2, 4, 6) the CMV remains at $+V_{dc}/6$. Therefore, RSPWM successfully avoids $\pm V_{dc}/2$ peak CMV and achieves CMV reduction.

The limitations and challenges of this RCMV-PWM are obvious. As shown in Figure 2.21(right), under this new space vector pattern, the linear modulation range is reduced and limited below 0.58. Moreover, the state will inevitably suffer the odd-to-odd or even-to-even transition, which will make two phase legs switch simultaneously. When

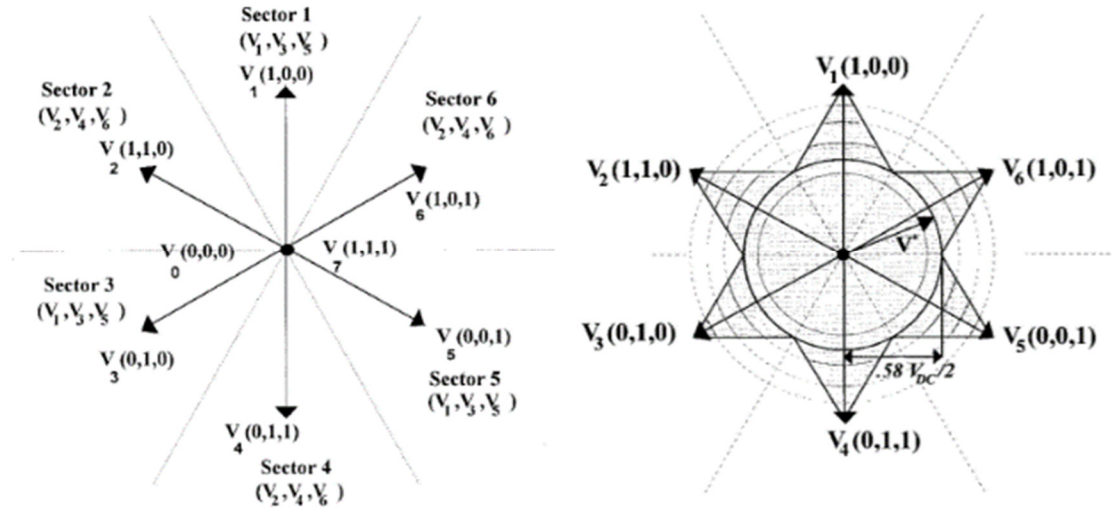


Figure 2.21: Space vectors of RSPWM proposed in [77].

Left: Sector division, Right: Linearity range.

considering the dead-time, the asynchronization of two phase-legs will generate unexpected CMV spikes during the transition [78].

In [79], another RCMV-PWM has been proposed and named near state PWM (NSPWM). The NSPWM utilizes 3 space vectors to synthesize the reference voltage, including the vector closest to the reference voltage and its two adjacent vectors. The sector division that is specially defined for NSPWM is as shown in Figure 2.22, which is essentially a conventional sector division frame with 30° rotation.

The shortcoming for NSPWM is also evident. NSPWM is linear only in 0.61-0.907, and in the lower linear range, NSPWM produces higher harmonic components, i.e., higher current THD than conventional PWM methods (SVPWM, SPWM). The generated bipolar line-to-line voltage will also increase the current ripple, resulting in potential winding insulation failure [80]. In addition, it causes excessive overvoltage at the motor terminal, especially when there's a long cable connection between the motor and the inverter. According to the reflected-wave phenomenon, the terminal voltage might exceed twice the DC-link voltage [81].

The most widely recognized RCMV-PWM so far is active zero state PWM (AZSPWM) [82, 83]. Compared with SVPWM, AZSPWM still uses the two boundary voltage vectors for the sector that the reference vector locates to synthesize the command vector, while equivalently synthesizing the “active zero” switching states with two second nearest vectors with equal duty ratio. As shown in Figure 2.23, compared with other RCMV-PWM methods, the consequence of such modulation schemes appearing on the pulse pattern is essentially the inverse alignment of the pulse with the medium-duty cycle among three phases, which shaves the CMV peak to $\pm V_{dc}/6$. The biggest difference

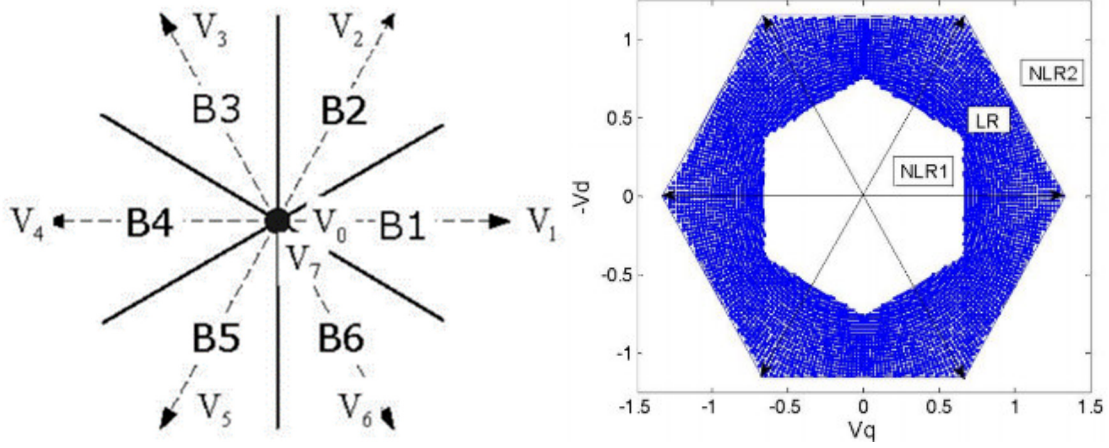


Figure 2.22: Space vectors of NSPWM proposed in [79].

Left: Sectors division, Right: Linearity range.

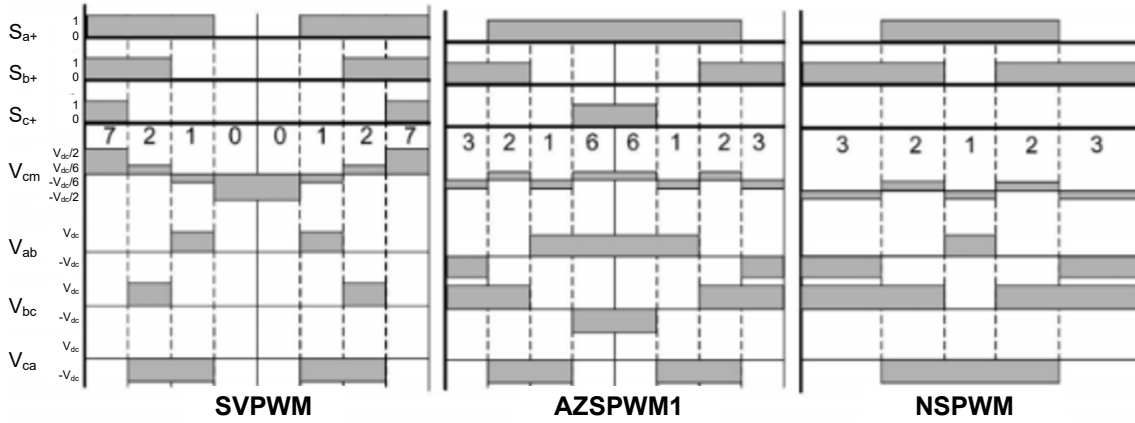


Figure 2.23: PWM pulse pattern of SVPWM, AZSPWM1, and NSPWM and the corresponding CMV [82].

between AZSPWM and the aforementioned RCMV-PWM schemes is that AZSPWM can still access the full vector plane as SVPWM does. However, the switching pattern of AZSPWM will result in increased phase current ripple, especially at the zero-crossing section, and it still suffers from the bipolar line-to-line voltage as well.

Different RCMV-PWM has their advantages and limits. Researchers are thinking about a combination of different modulation schemes to make the best use of the advantages and bypass the disadvantages. By comparing the performance of various RCMV-PWM with respect to modulation index, Reference [72] finds out that NSPWM shows the best performance for high modulation index cases but is unfeasible out of that region, while AZSPWM exhibits superiority in the low modulation index range. Therefore, a combined modulation scheme is proposed to use NSPWM and AZSPWM for different modulation indexes and set the boundary at 0.61. It takes the benefits of both modulation schemes while playing away from the shortcomings. To be more specific, it guarantees the linearity range for more effective usage of DC bus voltage and achieves CMV reduction with acceptable DM ripple.

Prior literature has empirically or experimentally shown that AZSPWM has a lower CMV than conventional SVPWM, but the side effects of AZSPWM have not been formulated [132] with regard to the potential CMV reduction limits caused by the increasing sideband components [133], and the higher phase current THD due to larger winding current ripple. Even the previous literature has observed such limitations, without an analytical model it is hard to show the overall pros and cons of various PWMs, especially when their performance is highly dependent on the modulation index. An analytical model of CMV and phase-current ripple, instead of a simulation-based model, is

highly demanded to optimize the performance of the overall motor drive system, which is one of the focuses of this dissertation.

In summary, all existing RCMV-PWM schemes need a trade-off between CMV amplitude reduction and phase current distortion. Moreover, these RCMV-PWM schemes will suffer from the bipolar line-to-line voltage, limited linearity range, and CMV spikes introduced by the simultaneous switching of two phase legs, making it more challenging in real practice. One last thing to be pointed out is the reduction of CMV peak with RCMV-PWM does not necessarily mean CMC across the whole frequency range is reduced. As shown in Figure 2.24, since the step change of the CMV waveforms during the transition remains as $V_{dc}/6$, the attenuation on the high-frequency CMC is not obvious because the caused CMC response keeps the same profile with fixed CMV step change. From the whole switching period point of view, the CMC impact is the same.

2.1.2.4 Topology

The inverter topology is where the CMV output. Properly selecting the topology can improve the CMV profile fundamentally. The most widely implemented topology in motor drives is the conventional 2-level VSI, in which the output of each phase leg could only be either the positive or negative DC-link voltage, i.e., $\pm 1/2 V_{dc}$ with respect to the ground. The CMV of a 2-level inverter can be formulated as the average of all phase leg outputs. There are only four possible values for CMV depending on the switching states, i.e., $\pm 1/6 V_{dc}$ or $\pm 1/2 V_{dc}$. It is believed that by modifying the inverter topology, the CMV could be reduced or even be nulled fundamentally if more voltage potential could be introduced. To explore this concept, the CMV reduction and cancellation with novel

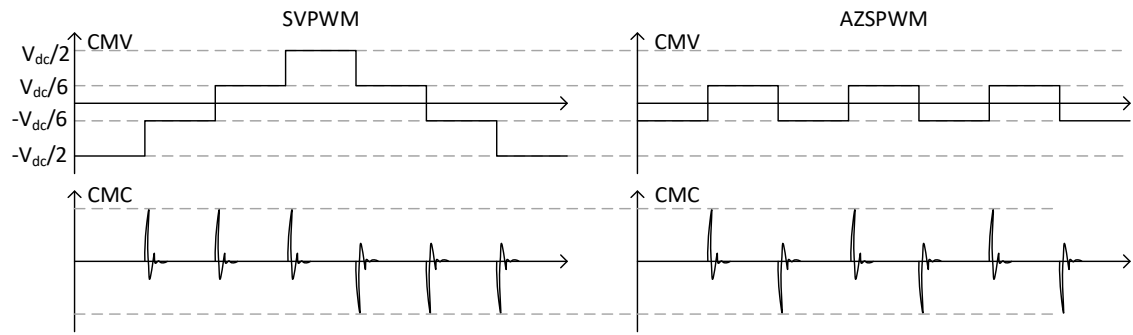


Figure 2.24: CMC reduction performance comparison.

inverter topologies have been studied, such as multi-level inverters, soft-switching inverters, etc.

Multi-level inverters (MLIs) are initially investigated almost 40 years ago [84]. The main purpose is to reduce the output current THD and lower the voltage blocking requirements for switching devices which makes MLIs very popular in medium voltage applications. Subsequently, people found the ability of CMN suppression for MLIs is also superior to 2-level inverters [85-89]. Because of the increased number of voltage levels in MLIs, the options for CMV levels are also more flexible with more switching states being introduced.

By adding two more switches per phase leg, the 3-level inverter could be obtained. The major types of 3-level inverters are neutral point clamped (NPC) type, T-type [90], and flying capacitor type [91]. As shown in Figure 2.25, with a 3-level inverter topology, an extra voltage level, zero, could be introduced, i.e., the output voltage for each phase can vary from three potential values, $V_{dc}/2$, 0, $-V_{dc}/2$. Hence, there are 27 space vectors in total, as shown in Figure 2.26 [92], where 1, 0, -1 represent the phase voltage is positive DC-bus, 0, and negative DC-bus, respectively.

For the “inner” 7 vectors, there are multiple (2 or 3) possible switching states lead to the same space vectors, leaving enough redundancy for manipulation of different switching states combinations. In addition, the CMV potential levels have been expanded to 0, $\pm V_{dc}/6$, $\pm V_{dc}/3$, and $\pm V_{dc}/2$, and still can access the full modulation range.

The benefits that a 3-level inverter could bring to CMV reduction are summarized below:

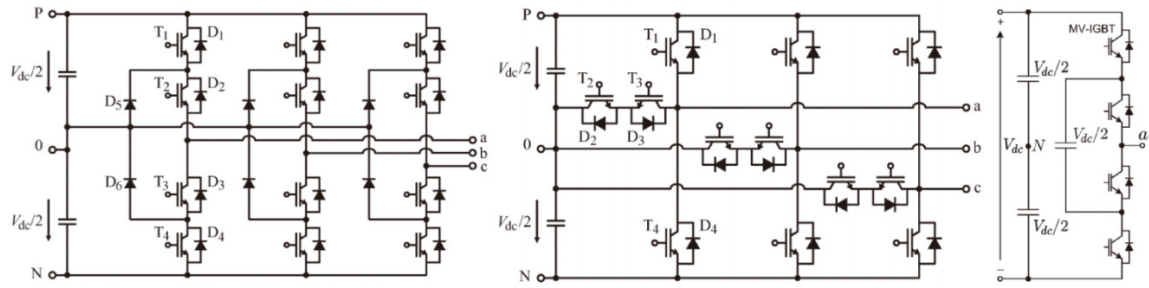


Figure 2.25: 3-level VSI for motor drives.

Left: Neutral point clamped inverter,

Middle: T-type inverter [90],

Right: Flying capacitor inverter [91].

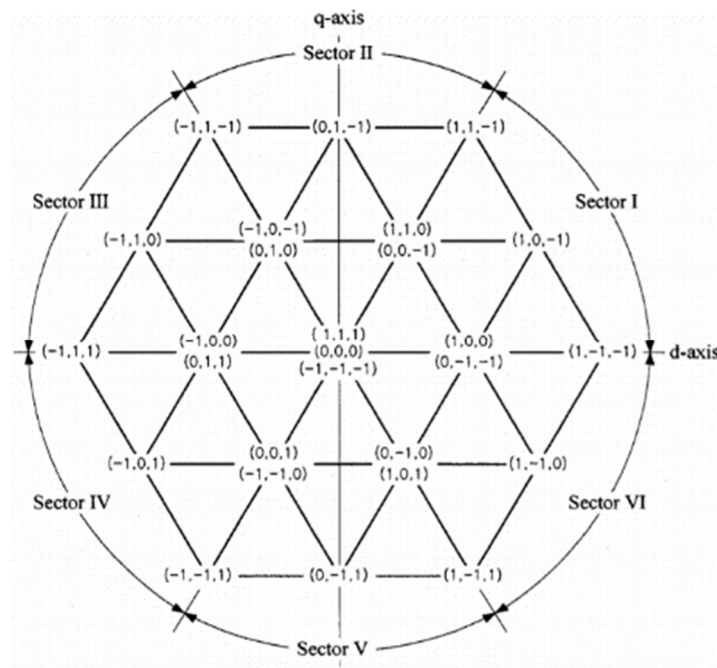


Figure 2.26: Output voltage vector diagram of the 3-L NPC inverter [92].

- (1) The step-change for CMV is only $V_{dc}/6$ instead of $V_{dc}/3$ in the 2-level inverter, resulting in lower CM voltage spectral amplitude.
- (2) The zero vectors (111 and 000) that generate maximum CMV ($V_{dc}/2$) in a 2-level inverter does not necessarily to be used in a 3-level inverter so that the peak CMV can be shaved to $V_{dc}/3$.
- (3) As the 3-level inverter provides great flexibility in choosing switching states, it is possible to always choose switching states with lower CMV contribution, whereas keeping the same output current quality.

As aforementioned, there is a possibility that by properly assigning the space vector combinations, the CMV can be eliminated. Reference [93] has validated this concept to achieve zero CMV generation with only 7 vectors. These 7 vectors generate zero CMV, which form a space vector frame as shown in Figure 2.27. Note that in this method, the transition of different states does not introduce simultaneous the switching on 2 phase legs, though the maximum modulation index is reduced to 86.6% of the conventional SVM for the 2-level inverter. The experimental result is shown in Figure 2.28, where the DC-link voltage is 750 V and the modulation index equals 0.58. The CMV reduction is significant.

Some other MLI topologies are investigated in [94-96] with the same principles applied. The higher number of levels could make even better CM performance for the same reason presented above. However, the greater number of levels might not be suitable for real application. One obvious disadvantage of MLIs is more than twice the number of switches compared to conventional 2-level inverters. Accordingly, gate signals, gate drivers, and the complexity of the control strategy will only increase the cost of

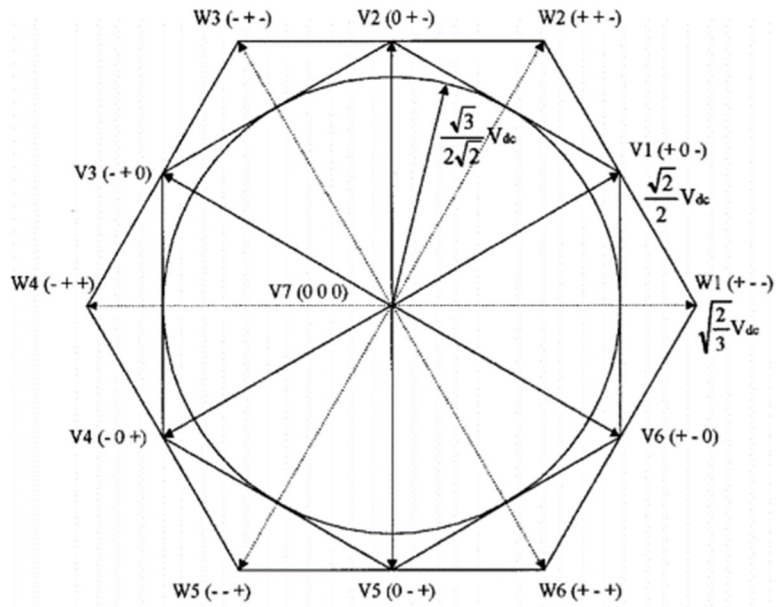


Figure 2.27: 7 switching states with zero CMV [93].

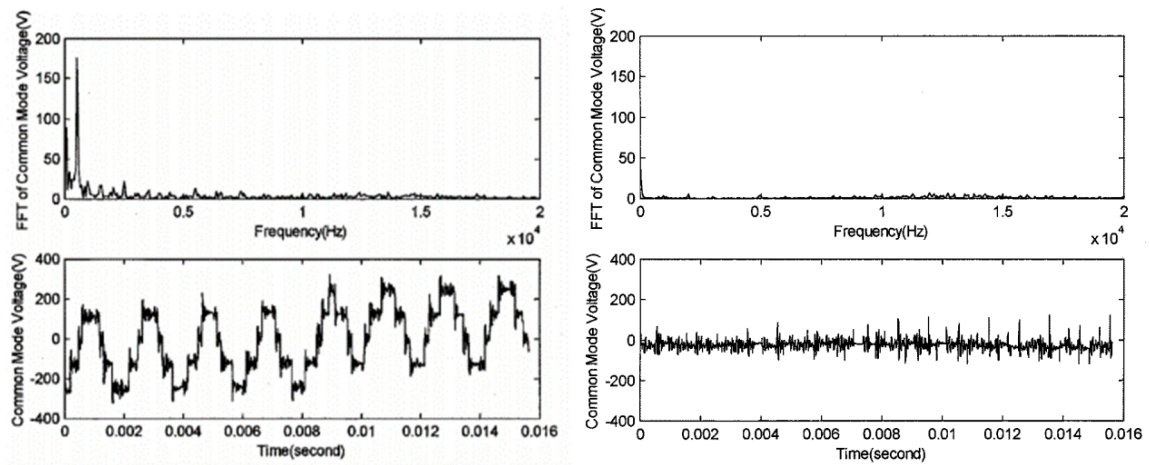


Figure 2.28: Multilevel inverter CMV [93].

Left: with conventional SVM, Right: with proposed zero-CMV SVM [93].

manufacturing. Designers have to weigh these advantages and disadvantages in MLSS when selecting the topology, the number of voltage levels, device types, etc.

As discussed in Chapter 1 of this proposal, the dv/dt strongly affects the CM EMI emission. In soft-switching inverters (SSI), the soft-switching transition is realized by the extra resonance between the parasitic and auxiliary components, which significantly slows the dv/dt , yielding the reduction of the high-frequency EMI noises.

As aforementioned, due to the physical limitation, the traditional center-aligned pulse width modulation (PWM) generates CMV varying between $\pm V_{dc}/6$ or $\pm V_{dc}/2$ in a three-phase two-level inverter. These values show that the CMV can never be zero. In the past decades, motors with a phase number higher than three, such as dual-three-phase motors (DTMs), have drawn the attention of the EV industry as the three-phase system cannot eliminate the CMV [97, 98]. Figure 2.29 shows one type of the DTM driven by dual inverters, where the neutral points for two sets of three-phase windings are separated with a winding angle difference of 30° . Such motors show advantages over conventional three-phase motors in terms of reliability; power density; fault tolerance; torque pulsations; and current stress, thereby becoming popular in safety-critical and high-power applications [99-104].

Compared to the DTM drive with a single neutral point [105, 106], a neutral-point-separated DTM provides more flexibility on the control for each set of winding, therefore reducing the control complexity. In terms of the CMV performance, as the phase count is an even number, by imposing $V_{dc}/2$ to one phase and $-V_{dc}/2$ to the other, there exists the possibility to eliminate the CMV [107, 108].

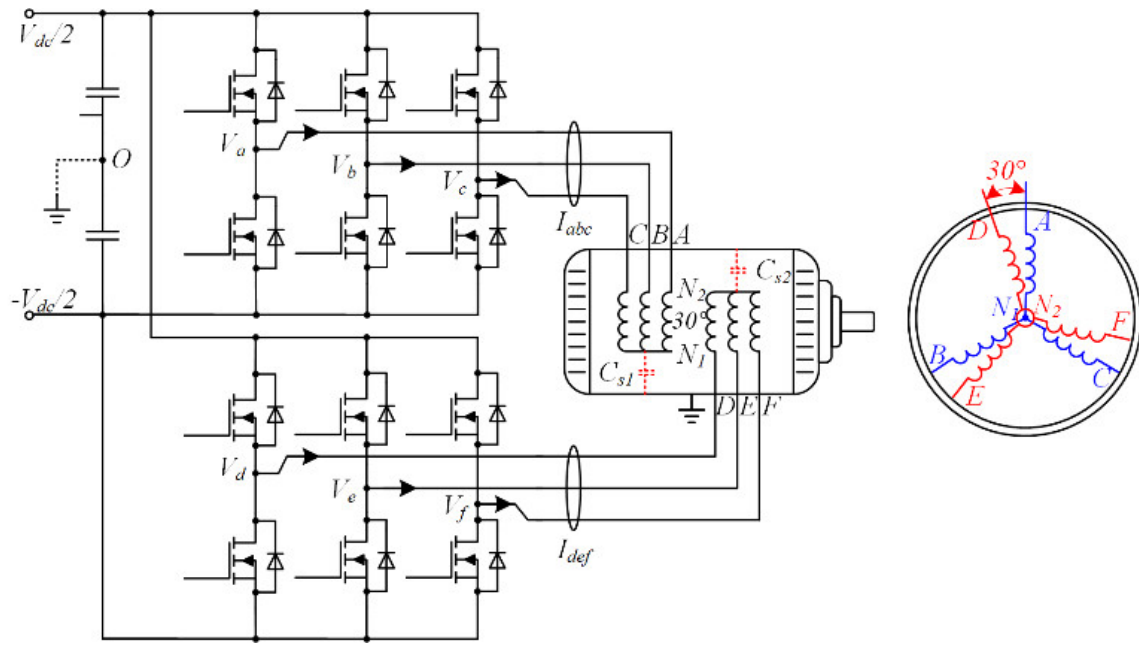


Figure 2.29 The drive system for a DTM.

A number of papers can be found investigating the CMV elimination for VSDs. In [109], a CMV elimination modulation scheme is proposed for a dual three-phase permanent magnet synchronous motor (PMSM). As shown in Figure 2.30, the proposed PWM shifting techniques realized an end-to-end cyclic PWM sequence to achieve CMV cancelation between two sets of three-phase windings. However, the algorithm is much more complex than the CSVM, and the proposed modulation method shows a limited linearity range, where the high modulation and overmodulation scenarios are not considered.

In [110], a CMV suppression strategy for synchronized SVM in the overmodulation region is proposed. However, due to three-phase structure limitations, the result can only restrict the peak CMV to a fixed $V_{dc}/6$ level without the possibility for further reduction. In [111], the authors present an SVPWM algorithm for five-phase converters operating in the overmodulation region with forbidden zero vectors. Nevertheless, the zero vectors usage in the overmodulation range has already been gradually decreased. Avoiding zero vectors brings less effectiveness to the CMV reduction in this range. In addition, the odd phase number cannot effectively reduce the CMV. Multilevel inverters are proposed in [112, 113] with the CMV reduction in the overmodulation region. However, the cost of switches for three-level and five-level inverters is much higher than the conventional six-phase structure, which is more preferred in automotive applications [114].

Instead of direct pulse shifting, a sawtooth carrier-based modulation is proposed in [115] for the asymmetrical DTM, which is intuitive but difficult to implement in digital controllers. As shown in Figure 2.31, the proposed sawtooth carriers for each phase in the same three-phase set are the same, while mirror-symmetrical in one carrier cycle for the two different three-phase sets. This could reduce both the peak amplitude and optimize the

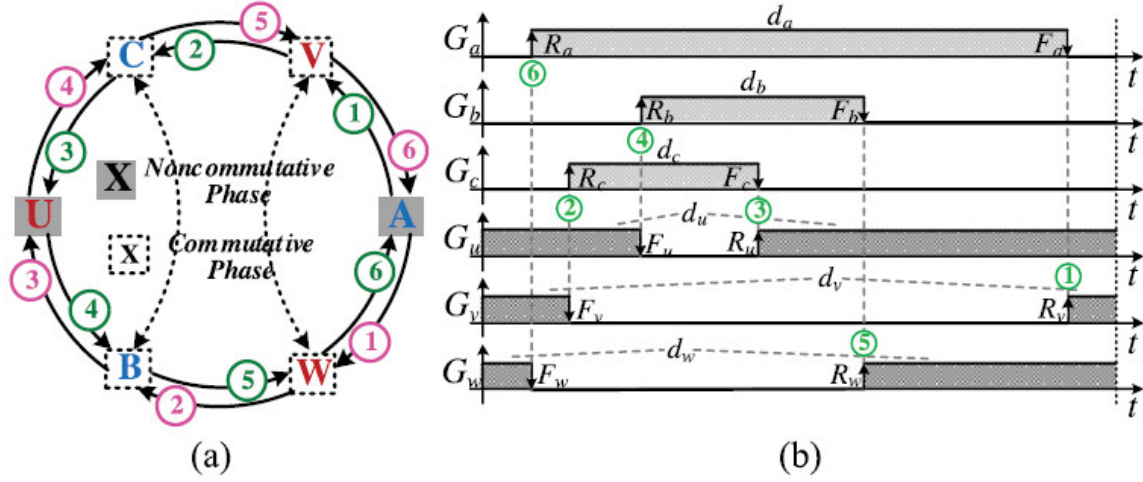


Figure 2.30: Principle of the proposed end-to-end cyclic sequence of PWM signal.

(a) End-to-end connection sequence for the six-phase PWM signal,

(b) One of the PWM signal patterns to cancel out the generalized total CMV [109].

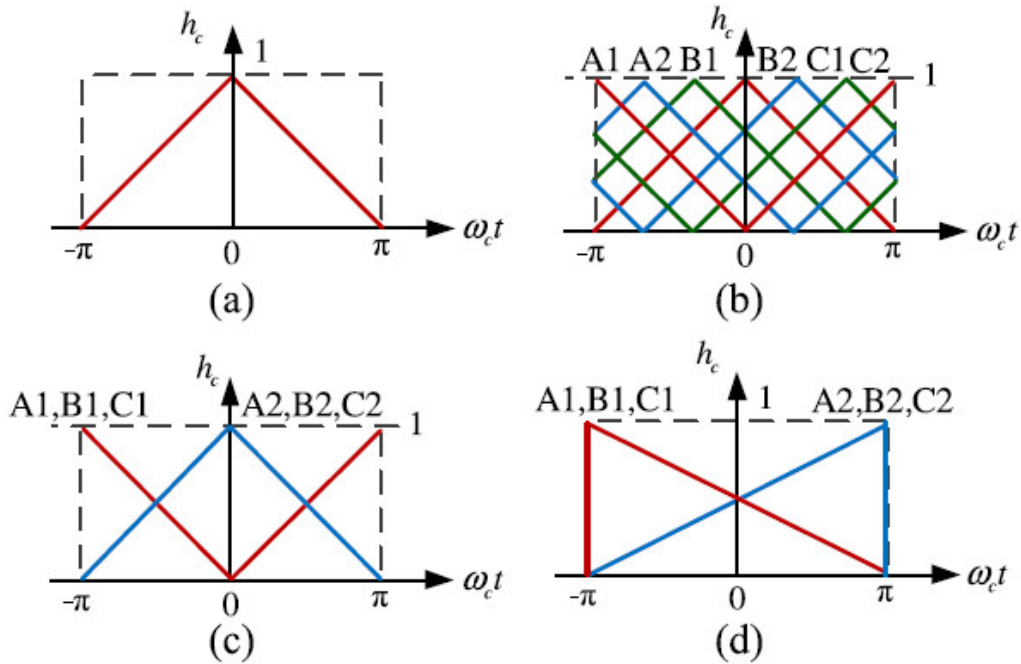


Figure 2.31 Carriers in one switching cycle.

(a) SPWM, (b) PSSPWM-1, (c) PS-SPWM-2, (d) proposed SC-SPWM [115].

frequency distribution of the CMV in frequency span. The results show that the proposed modulation has the best performance in CMV reduction on amplitude and changing frequency among these four SPWM methods but leads to a higher phase current distortion. Besides, the linearity range is still limited.

Given different space vectors yield different CMV levels, some modulation methods are proposed in [116, 117] to use specific space vector combinations for the CMV cancelation, where the limited vector usage constrains the vector plane, resulting in a limited linearity range. In [118], a new active zero state PWM (AZSPWM) for a six-phase system is proposed where the CMV is reduced by 1/3 in the full linearity modulation range. Nevertheless, the side effects of AZSPWM, i.e., a much higher phase current ripple exist and are yet to be solved according to the previous review. Besides, AZSPWM cannot eliminate CMV, making it unable to fully utilize the benefit of the DTMs. In [119, 120], the differential-mode performance improvement for DTMs is investigated. The solutions focus more on the motor control algorithms instead of the modulation mechanism, where the CM performance is not addressed.

2.1.2.5 Circuitry layout

Since the EMI noise is strongly susceptible to the signal propagation path, the PCB parasitics will play an important role in noise spectrum manipulation. Driven by this idea, a large amount of research work on system parasitic characterization has been carried out, which typically concentrates on layout optimization and parasitic cancellation [119-125], and proper adjustment of the circuit orientation to cancel the electric and magnetic field coupling [121-123]. As a fundamental skill of all electrical engineers, this part will not be addressed in detail.

In summary, the PCB layout optimization methods are useful but very limited. In actual application, the design is usually restricted by various limitations. For example, the size, shape, weight, or even PCB layer count. Taking all these constraints into account, the PCB design might be already close to the optimal design for specific circumstances with not much room for improvement.

2.1.2.6 Summary

Based on the general review above, major CM EMI noise mitigation methods in the three-phase motor drive system have been investigated. Each of them has its intrinsic limitations and disadvantages. A summative comparison of each CM EMI noise reduction approach will be listed in this chapter.

(1) CM filters are the most widely adopted solution for nearly all kinds of motor drives. To obtain higher CMC attenuation, the CM chokes need to provide higher impedance, which results in more coil turns, larger core cross-sectional area, higher magnetic material permeability, and even more stages of filtering. These essentially determine that as the desired cutoff frequency increases, the larger core is inevitably needed. The bulky size and heavy weight make the system power density drop and become lossy and costly as well. The cooperation of passive and active filters can help shrink the passive components and gain better EMI filtering performance in a wider frequency range. However, the additional active switches and control circuits may make the situation more complex.

(2) AGDs for CMN mitigation count on reshaping the switching profile. By reducing the sharp dv/dt or di/dt edge, the high-frequency CM EMI noise could

be limited. However, it comes with the penalty of higher switching loss because of slower switching speed. It has been proven that the impact on CM EMI noise mitigation is very limited other than the high-frequency range. In addition, its basic idea of avoiding high dv/dt is going against the mainstream trends of modern power semiconductor devices development and does not seem a good match to WBG devices.

(3) Modulation schemes with CMV reduction capability are the most advantageous solutions compared to all other approaches. No extra hardware effort needs to be paid but just a revision on the PWM patterns. Hence saving space, loss, and cost. The drawbacks for the PWM schemes based CMV reduction typically appear in the limited modulation index range and potential quality degradation on the DM signals (i.e., higher THD of output phase current). In addition, the contribution to the high-frequency noise spectrum mitigation and CMC EMI mitigation is limited.

(4) Inverter topologies with CMN reduction considerations are the most promising solution for modern motor drive systems for multiple reasons. First, compared with the approaches above, the added circuit part typically consists of switches, which do not consume the system space as much as CM filters do. Second, the fast-switching capabilities of WBG devices greatly reduce the penalty on power loss introduced by auxiliary circuits. Third, unlike the RCMV-PWM methods, topology-based CMN reduction does not affect the DM signals, so the system output quality is guaranteed. The only barrier to these topologies' practical

implementation is the increased control complexity on both algorithms and increased gate driver numbers.

- (5) PCB layout optimization techniques are very cost-effective since they can be realized without extra hardware installation or any software modification, but just more attention to the physical components layout. However, because the work is done in such an experience-based part, the strategies that can play are very limited for specific designs. Its case dependence makes it lack generality and cannot be considered the major solution for CMN mitigation in the motor drive system.

2.3 Existing Research Interests

According to the literature review in this chapter, some existing research interests could be summarized in the following aspects.

For the inverter on the EV charger sides:

- (1) When dealing with load unbalance issues, a neutral path is necessary.
- (2) DC-link capacitor balancing control is important for a stable neutral referent point.
- (3) Digital filtering is needed to regulate load unbalance scenarios.

For the inverter on the EV motor drive sides:

- (1) CM EMI reduction is a must for the next generation of EV with WBG devices.
- (2) Different CM EMI mitigation approaches have their effectiveness in certain aspects. Overall, choosing appropriate modulation methods and inverter topology turned out to be a more balanced and preferred option.

- (3) An analytical model of a specific modulation scheme is needed to determine the corresponding CMV reduction performance and the potential DM impact.
- (4) Using a six-phase structure could potentially eliminate the CMV, but further study is required to expand the linearity range.
- (5) Using multilevel structure to reduce the CMV, including the CM analytical modeling.

This dissertation will focus on the summarized research opportunities, one is enhancing the steady-state performance of a three-phase four-wire inverter at the V2L mode. The other is analytically characterizing the CM and DM performance of specific modulation methods for both two-level and three-level inverters and investigating the CMV elimination approach in the six-phase motor drive system.

Chapter 3 THREE-PHASE INVERTER

POWER QUALITY MODELING AND CONTROL

This chapter concentrates on modeling and control strategy development of the V2L feature of the EV charger regarding the unbalanced load regulation and load harmonic suppression.

In the V2L mode, the onboard power electronics devices will have various load conditions as sources. For example, when operating in V2L mode, the vehicle is needed to provide a single-phase or three-phase AC source for external electrical appliances. To convert the energy from batteries to loads, there is a chance that the external loads are unbalanced due to multiple single-phase usage or false connection. The neutral point stability and output harmonic are likely to lose control. To safely operate in V2L mode, dealing with the unbalanced load becomes important. In some cases, multiple nonlinear loads will introduce considerably high harmonic contents when the operating point meets the system resonant point. Dealing with system output harmonic is also a task.

The structure of this chapter is organized as follows. The first section will introduce the proposed model of the V2L structure. Then, the neutral-point voltage control under the unbalanced load case will be introduced and analyzed theoretically. The third section will evaluate the proposed virtual resistor damping method with respect to different load type. In the fourth section, comprehensive simulation validation will be performed. Finally, the proof-of-concept prototype is fabricated in the lab and the experimental results will be presented in the last section to demonstrate the inverter operation with the unbalanced load and verify the proposed concept on the output harmonic suppression.

3.1 Modeling of Three-phase Four-wire Inverter at V2L Mode

One mission of this dissertation is to solve the load-unbalance issue that stable the steady-state performance and quick dynamic response of a three-phase four-wire inverter at the V2L mode. Regarding this goal, the three-phase four-wire four-leg inverter is studied. The topology is shown in Figure 3.1. On the AC side, the conventional three-phase two-level inverter is composed of MOSFETs $S_{a1} \sim S_{c2}$. At the DC-bus side, there are split DC-link capacitors C_{N1} and C_{N2} , where the midpoint of the split DC-link capacitors serves as the neutral point. The fourth leg formed by S_{n1} , S_{n2} , and L_N is to regulate the neutral-point voltage caused by the load unbalance. L_f and C_f are the grid-side filter inductor and capacitor, respectively.

With the fourth leg stabilizing the neutral point, each phase can be essentially equivalent to a buck converter and controlled independently with the conventional SPWM. The neutral leg is operated independently for the sake of neutral-point balancing [21]. The independently controlled neutral module (ICNM) equivalent circuit of each phase is shown in Figure 3.2.

According to KCL and KVL, Eqn (3.1) can be obtained.

$$\begin{cases} \frac{di_{L_f}}{dt} = \frac{1}{L_f} (V_{ph} - V_{C_f}) \\ i_{L_f} = i_o + i_{C_f} \\ \frac{dV_{C_f}}{dt} = \frac{1}{C_f} i_{C_f} \end{cases} \quad (3.1)$$

Ultimately the V2L mode needs to control the output voltage, yielding the control scheme of each phase voltage shown in Figure 3.3.

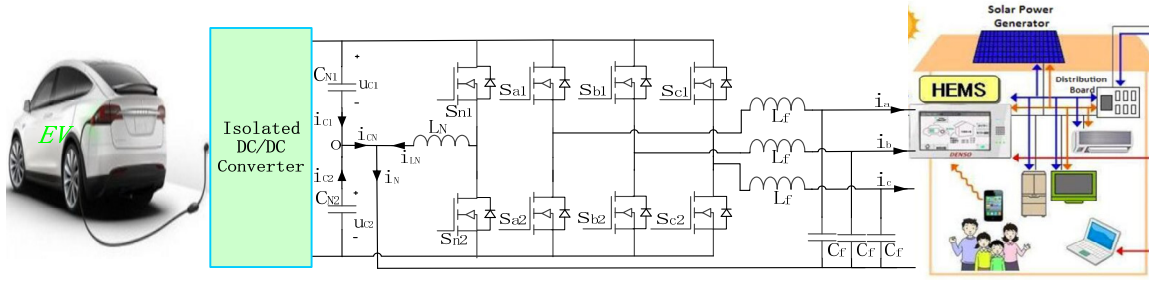


Figure 3.1: Topology of a three-phase four-wire inverter used in a V2L EV charger.

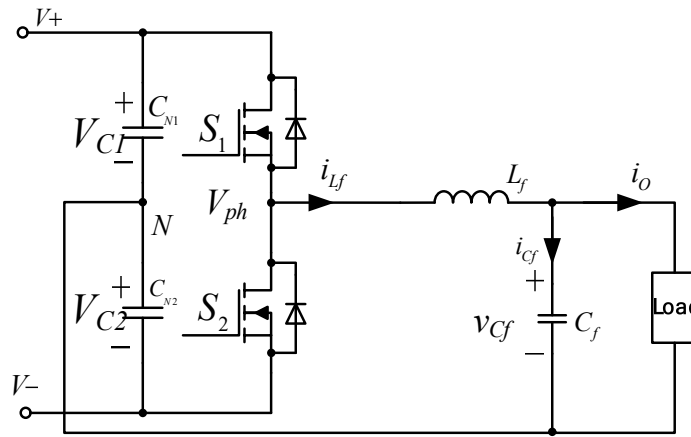


Figure 3.2: Equivalent circuit of ICNM.

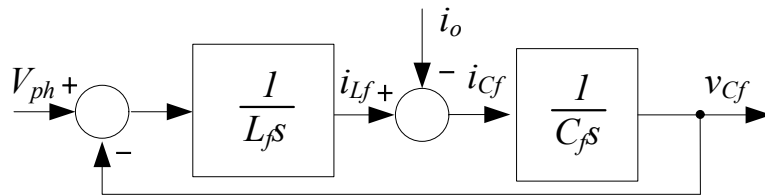


Figure 3.3: Control block diagram of a single-phase equivalent circuit.

The digitized model is shown in Figure 3.4, where V_{phx} and i_{phx} are AC values of each phase voltage and current, respectively. φ is the corresponding phase angle and G_{phx_s} is a PI controller.

In the V2L mode, the three-phase output voltage needs to be stable and symmetric, even though the phase current varies as the load changes. Therefore, the main goal of the outer voltage loop is to guarantee stable three-phase voltage generation. The inner current loop is responsible for the fast system response and implements the system over-current protection.

3.2 Neutral Point Voltage Control

At the V2L mode, the three-phase output voltage is supplied by a DC-bus capacitor tank. Therefore, the system can be equivalent to a voltage source inverter (VSI). Assuming the mathematical expression of the three-phase voltage is shown in (3.2).

$$\begin{cases} V_a = \sqrt{2} V_m \cos(\omega t) \\ V_b = \sqrt{2} V_m \cos\left(\omega t - \frac{2}{3}\pi\right) \\ V_c = \sqrt{2} V_m \cos\left(\omega t + \frac{2}{3}\pi\right) \end{cases} \quad (3.2)$$

We have the three-phase current expressed in (3.3) with the three-phase resistor load.

$$\begin{cases} I_a = \sqrt{2} I_m \cos(\omega t) \\ I_b = \sqrt{2} I_m \cos\left(\omega t - \frac{2}{3}\pi\right) \\ I_c = \sqrt{2} (I_m + \Delta I_c) \cos\left(\omega t + \frac{2}{3}\pi\right) \end{cases} \quad (3.3)$$

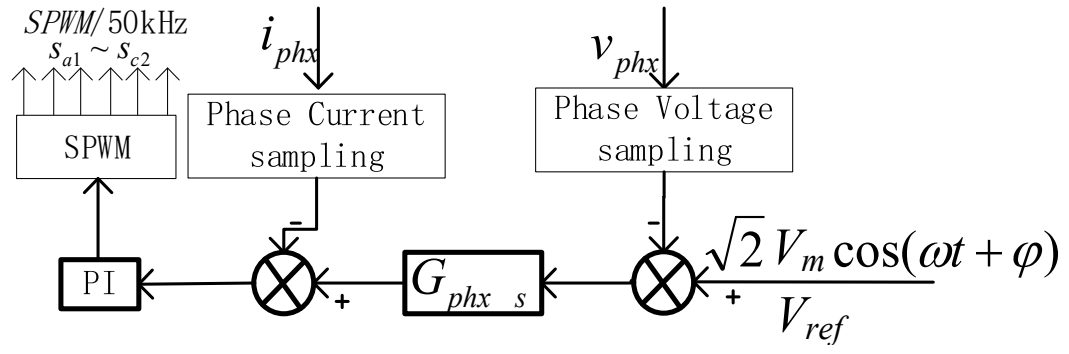


Figure 3.4: Single-phase SPWM control block diagram.

where I_m is the RMS value of each phase current and ΔI_c is the unbalanced component on the current of phase C. Such asymmetric load causes the neutral-point current, which further creates the neutral-point unbalance. To evaluate the impact of the load asymmetry on the neutral-point voltage unbalance, we divide the DC-link voltage as (3.4).

$$v_{dc} = V_{dc} + \tilde{v}_{dc} \quad (3.4)$$

where U_{dc} is the DC component of the capacitor voltage and $\tilde{v}_{dc}$ is the AC component overlapped on the DC part. The larger $\tilde{v}_{dc}$, the larger voltage oscillation across DC-link capacitors. Using KCL, Eqn (3.5) is obtained, referring to Figure 3.5.

$$i_{C1} + i_{C2} = i_{CN} \quad (3.5)$$

where i_{CN} creates the voltage difference between the upper and lower DC-link capacitors. When the neutral point is balanced, the voltage change across split capacitors of the DC-link is identical, i.e., $\Delta V_{C1} = \Delta V_{C2}$. Here i_{C1} and i_{C2} are expressed as:

$$\begin{cases} v_{C1} = \frac{C_{N1}}{C_{N1} + C_{N2}} i_{CN} \\ v_{C2} = \frac{C_{N2}}{C_{N1} + C_{N2}} i_{CN} \end{cases} \quad (3.6)$$

Furthermore, the voltage across each split DC-link capacitor can be derived as:

$$\begin{cases} v_{C1} = \frac{1}{C_{N1}} \int i_{C1} dt + V_{oC1} \\ v_{C2} = \frac{1}{C_{N2}} \int i_{C2} dt + V_{oC2} \end{cases} \quad (3.7)$$

where V_{oC1} and V_{oC2} are DC voltage of C_{N1} and C_{N2} , respectively. The current integrals are AC components. According to (3.6) and (3.7), the voltage oscillation of C_{N1} and C_{N2} are formulated as:

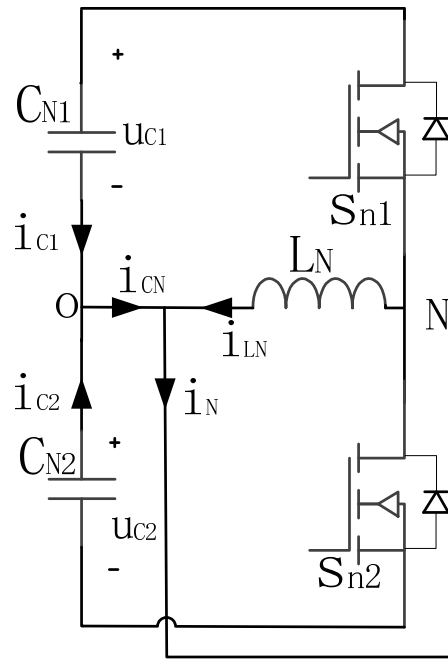


Figure 3.5: Structure of the neutral phase.

$$\begin{cases} \tilde{v}_{C1} = \frac{1}{C_{N1}} \cdot \frac{C_{N1}}{C_{N1} + C_{N2}} \int i_{CN} dt \\ \tilde{v}_{C2} = -\frac{1}{C_{N2}} \cdot \frac{C_{N2}}{C_{N1} + C_{N2}} \int i_{CN} dt \end{cases} \quad (3.8)$$

Therefore, the neutral-point current i_{CN} determines the voltage oscillation across split DC-link capacitors and the neutral-point oscillation. In Figure 1, according to KCL, we have:

$$\begin{cases} i_N = i_{LN} + i_{CN} \\ i_N + i_a + i_b + i_c = 0 \end{cases} \quad (3.9)$$

Combined with (3), the neutral-point current is derived as

$$i_{CN} = -\sqrt{2}\Delta I_c \cos\left(\omega t + \frac{2}{3}\pi\right) - i_{LN} \quad (3.10)$$

When the fourth leg is disabled, the current on the neutral inductor (i_{LN}) can be regarded as 0. Assuming the capacitance of each split DC-link capacitor is identical, we have the instantaneous voltage of C_{N1} and C_{N2} derived as

$$\tilde{v}_{C1} = -\tilde{v}_{C2} = \frac{1}{C_{N1} + C_{N2}} \int i_{CN} dt = -\frac{\sqrt{2}}{2\omega C} \Delta I_c \sin\left(\omega t + \frac{2}{3}\pi\right) \quad (3.11)$$

Eqn (3.11) indicates when the capacitance of each split DC-link capacitor is identical, the unbalanced load will not affect the overall DC-link voltage, i.e., the average voltage of each split DC-link capacitor is exactly half of the total DC-link voltage. However, it will result in the voltage oscillation on each split DC-link capacitor, i.e., the oscillation of the neutral-point voltage. The oscillation frequency is equal to the output AC voltage and current. The oscillation amplitude is proportional to the degree of the load unbalance and inversely proportional to the DC-link capacitance and output AC voltage frequency.

As the unbalance rate goes to a certain level, the fourth leg needs to be activated to suppress the voltage oscillation of the neutral point.

Figure 3.5 shows the neutral-phase structure. C_{N1} and C_{N2} are in series connections. The neutral point is connected to the middle point of the fourth leg through an inductor L_n for DC-link capacitor energy transfer.

According to KCL and KVL, we have:

$$\begin{cases} i_{CN} = C_{N1} \frac{dv_{C1}}{dt} - C_{N2} \frac{dv_{C2}}{dt} \\ v_{NO} = L_N \frac{di_{LN}}{dt} \\ i_N = i_{CN} + i_{LN} \\ i_a + i_b + i_c + i_N = 0 \end{cases} \quad (3.12)$$

Define the voltage difference between two capacitors as:

$$\sigma = v_{C1} - v_{C2} \quad (3.13)$$

Assume that over a switching period, the average of the firing pulse is p (p with the magnitude of ± 1). The duty cycle of the fourth leg is [124]:

$$D = \frac{1+p}{2} \quad (3.14)$$

Combined with (3.13),

$$v_{NO} = Dv_{C1} - (1-D)v_{C2} = \frac{1+p}{2}v_{C1} - \frac{1-p}{2}v_{C2} = \frac{p}{2}v_{dc} + \frac{1}{2}\sigma \quad (3.15)$$

Assume $C_{N1}=C_{N2}=C$, to balance the neutral-point voltage, i.e., $\sigma \approx 0$, the neutral-point voltage control block diagram is shown in Figure 3.6, based on the Laplace transform of (3.12).

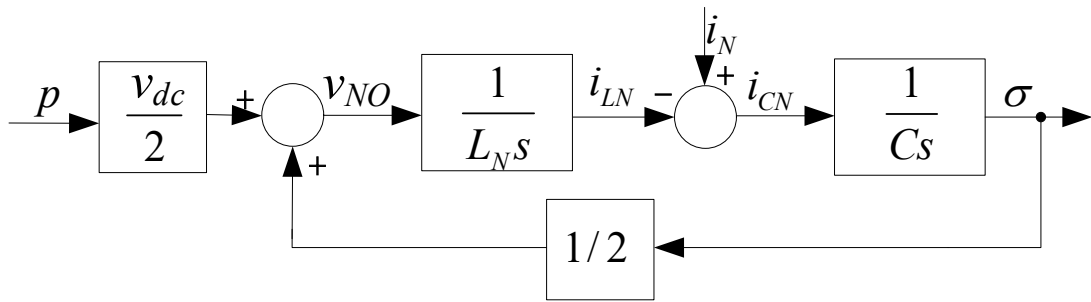


Figure 3.6: Control block diagram of the neutral-point voltage.

3.3 Virtual Resistance Control

With a balanced neutral-point voltage provided, a three-phase inverter can be modeled as three independent single-phase systems. Thus, all the analysis in this section can be simplified as a single-phase SPWM inverter, where the output three-phase voltage should be stable no matter how the load changes within the rated power range.

3.3.1 Resistive Load

The simplified circuit model is shown in Figure 3.7.

According to KVL, in s-domain (3.16)-(3.17) are valid.

$$v_{spwm} = \left[\left(\frac{1}{j\omega C} // R_L \right) + j\omega L \right] i_L(t) \quad (3.16)$$

$$\begin{cases} \frac{i_L}{v_{spwm}}(s) = \frac{R_L Cs + 1}{LCR_L s^2 + Ls + R_L} \\ \frac{v_c}{i}(s) = \frac{R_L}{R_L Cs + 1} \end{cases} \quad (3.17)$$

Therefore, the voltage transfer function for every single phase can be written as:

$$\frac{v_c}{v_{spwm}}(s) = \frac{R_L}{R_L LCs^2 + Ls + R_L} \quad (3.18)$$

Such transfer function determines the system stability. As for designers, the inductor (L) and capacitor (C) is pre-determined by the system power capability, switching frequency, THD, etc., while the load (R_L) varies with the power. The bode plot of such system transfer function with different R_L is then shown in Figure 3.8.

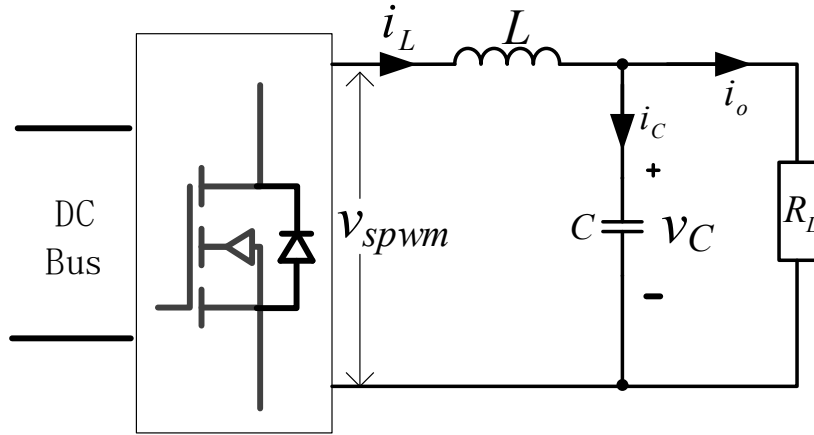


Figure 3.7: Simplified circuit model for each phase.

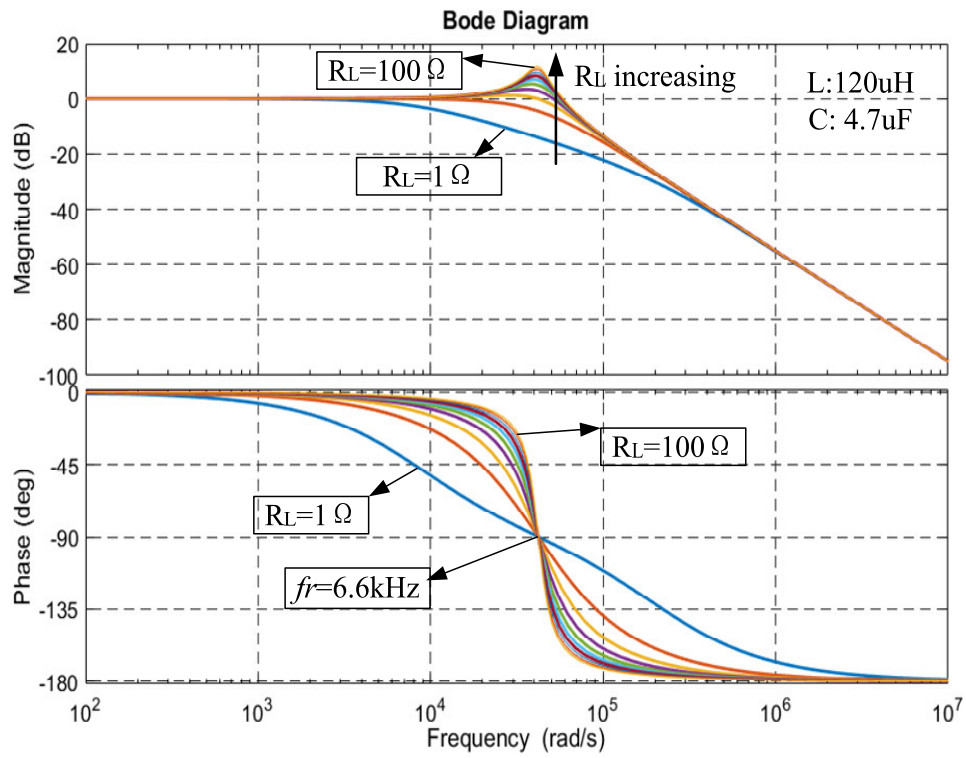


Figure 3.8: Bode plot of the system transfer function.

Here the inductance and capacitance of the LC filter are set to 120 μH and 4.7 μF , respectively while the load R_L varies from 0 to 100 Ω . As the load decreases, i.e., R_L increases, the gain at the resonance point increases as well. The high gain will potentially lead to high voltage harmonics. When $R_L \rightarrow \infty$, i.e., no-load, the large voltage harmonics are expected on the phase output. On the other hand, if R_L is too small, the system will be unable to reach the reference output voltage, i.e., losing control. To guarantee the stable output and low harmonics, the battery-side DC/DC converter is used to control the DC-link voltage, and the DC/AC stage can vary the switching frequency to shift harmonics away from the resonance point. Another approach is to adopt the virtual resistor.

Assume there is one resistor R_v in parallel to the load resistor R_L . The equivalent load then is formulated as:

$$R'_L = \frac{R_L R_v}{R_L + R_v} \quad (3.19)$$

Replacing R_L in (3.3-3) with R'_L yields:

$$\frac{V_{c-v}}{v_{spwm-v}}(s) = \frac{R_v}{R_v LCs^2 + \left(\frac{R_v}{R_L} + 1 \right) Ls + R_v} \quad (3.20)$$

According to (3.20), let $R_v=4.2 \Omega$. The system bode plot at different loads is redrawn as Figure 3.9.

A comparison of Figure 3.8 and Figure 3.9 indicates that the virtual resistance helps to stabilize the gain at the resonant point as the load varies from 1~100 Ω , which suppresses the voltage distortion, and effectively enhances the system controllability. The system voltage control loop can be expressed as below in Figure 3.10.

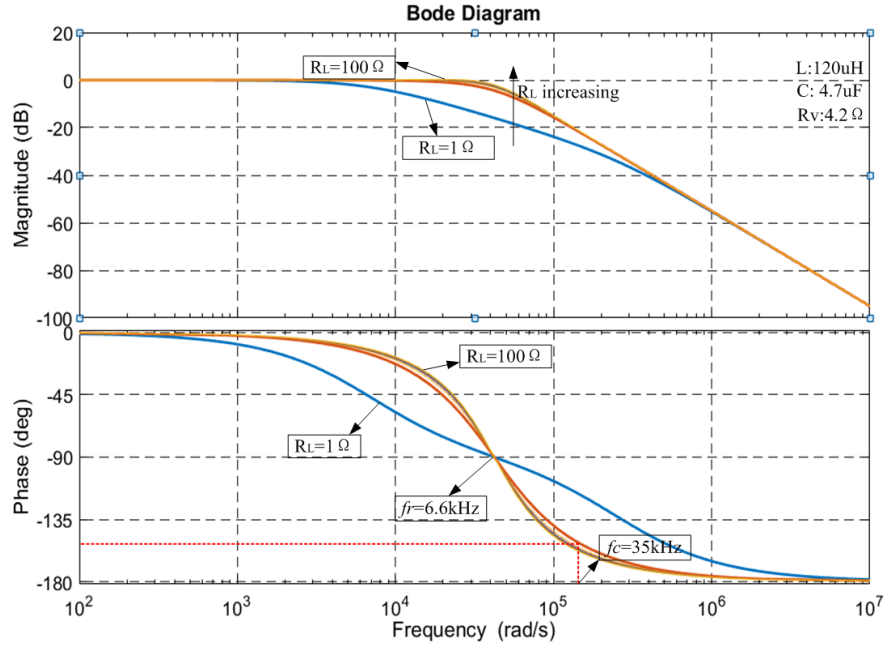


Figure 3.9: System transfer function bode plot with virtual resistance.

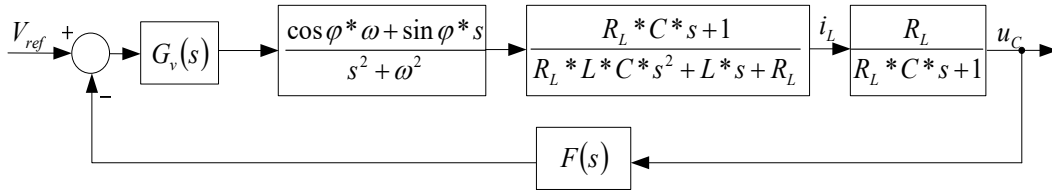


Figure 3.10: Voltage loop mathematical model with a virtual resistor.

Here $G_v(s)$ is a PI compensator, expressed as

$$G_v(s) = K_p + \frac{K_i}{s} \quad (3.21)$$

where K_p is proportional gain and K_i is the integral gain. $F(s)$ is the system feedback function with virtual resistance. According to (3.18) and (3.20), $F_R(s)$ can be shown in (3.22). Figure 3.11 shows the corresponding bode plot.

$$F_R(s) = \frac{R_v R_L C L s^2 + (R_v + R_L) L s + R_v R_L}{R_v R_L C L s^2 + R_v L s + R_v R_L} \quad (3.22)$$

According to Figure 3.11, the transfer function of the feedback loop can be treated as a notch filter around the resonance frequency, which effectively suppresses the harmonics amplification caused by the open-loop transfer function.

The virtual resistance not only affects the output voltage harmonics but also influences the transient performance of the whole system. The step response of the whole system is shown in Figure 3.12. The vertical axis represents the overshoot of the grid voltage during the start-up process.

The virtual resistance changes from 1 Ω to 10 Ω with 10 kW output power. The optimal virtual resistance is chosen as $R_v=4.2 \Omega$, given that the system has acceptable overshoot and dwelling time. Meanwhile, the system cut-off frequency can be defined as R_v/L_f [125], i.e., the cut-off frequency has been selected as 35 kHz, and the phase margin of 35° is also achieved from Figure 3.9.

It should be pointed out that such resistance selection is highly related to system specifications. An acceptable system dynamic response should be aware of in terms of the voltage overshoot and short dwelling time.

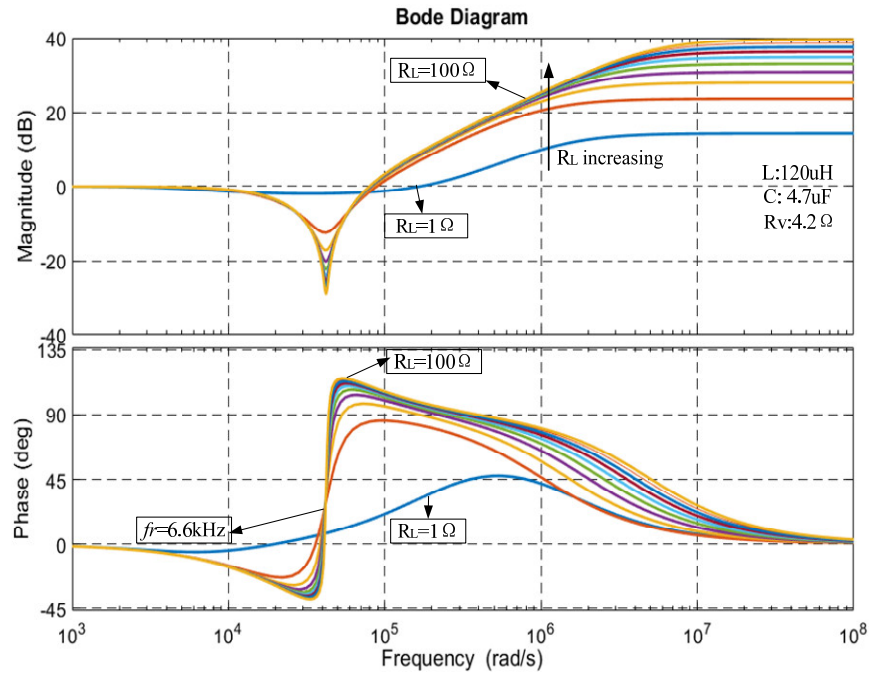


Figure 3.11: Bode plot of the feedback loop transfer function.

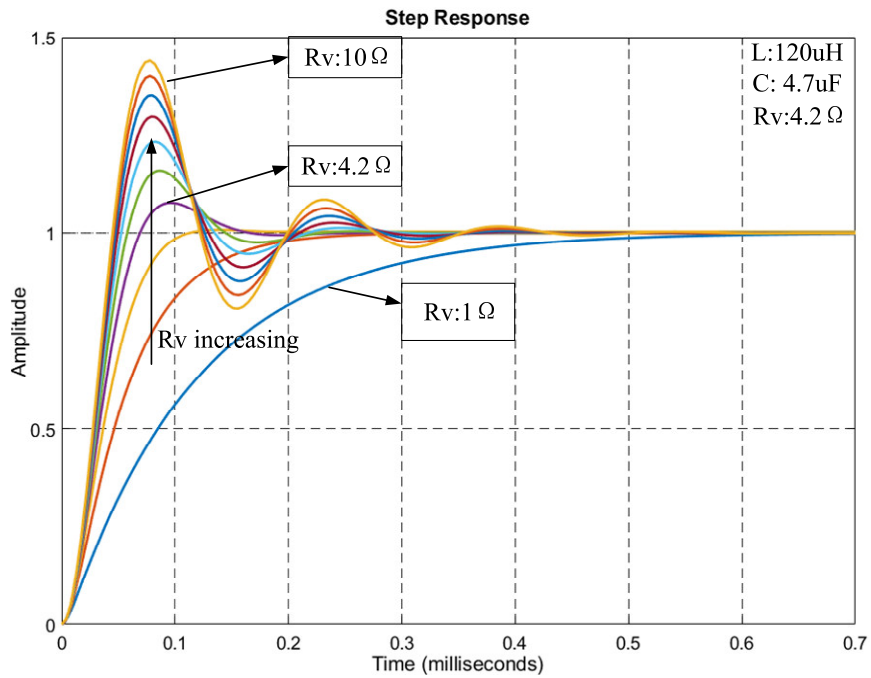


Figure 3.12: Step response for the whole system.

3.3.2 Resistance–Inductive Load

A similar analysis can be performed when the load is the resistance-inductive type, such as motors. In this case, the load impedance can be expressed as:

$$Z_{RL}(s) = R_L + L's \quad (3.23)$$

where L' is the equivalent serial-connected inductance of the RL load. In (3.17), by replacing R_L with Z_{RL} , we get the system transfer function as:

$$\frac{v_{c-RL}}{v_{spwm-RL}}(s) = \frac{L's + R_L}{L'LCs^3 + R_L LCs^2 + (L' + L)s + R_L} \quad (3.24)$$

The corresponding system bode plot at different loads is shown in Figure 3.13. The series-connected inductance for each curve varies from 1 μ H to 1 mH.

Similar to the pure resistive load, the virtual resistor can be introduced to stabilize the output and lower harmonics. Assuming there is one resistor R_v in parallel to Z_{RL} , we can derive the equivalent load impedance as:

$$Z'_{RL-v}(s) = (R_L + L's) // R_v \quad (3.25)$$

The system transfer function with the virtual resistance can be expressed as (3.26). The bode plot is shown in Figure 3.14.

$$\frac{v_{c-RL-v}}{v_{spwm-RL-v}} = \frac{R_v L's + R_L R_v}{R_v LL'Cs^3 + (R_L R_v LC + LL')s^2 + (R_L L + R_v L + R_v L')s + R_L R_v} \quad (3.26)$$

$$F_{RL}(s) = \frac{R_L R_v LL'Cs^3 + (R_L^2 R_v LC + R_L LL')s^2 + [R_L L(R_L + R_v) + R_v R_L L']s + R_v R_L^2}{R_L R_v LL'Cs^3 + (R_L^2 R_v LC + R_L LL')s^2 + (R_L R_v L + R_L R_v L')s + R_v R_L^2} \quad (3.27)$$

Furthermore, according to (18) and (26), the feedback transfer function $F_{-RL}(s)$ can be shown in (3.27), with the bode plot at $R_v=4.2 \Omega$ shown in Figure 3.15. The in series

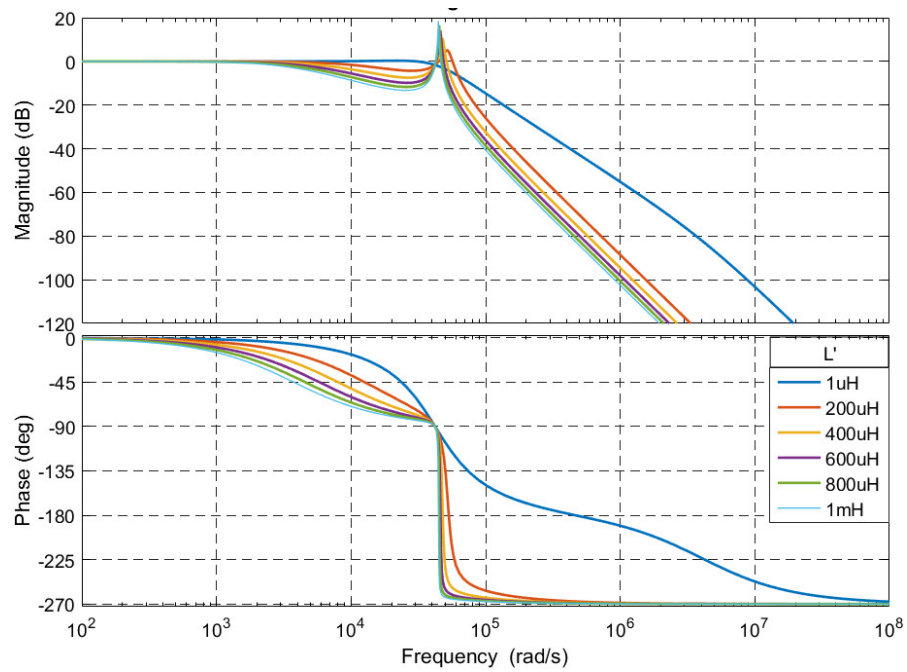


Figure 3.13: System transfer function Bode plot with RL load.

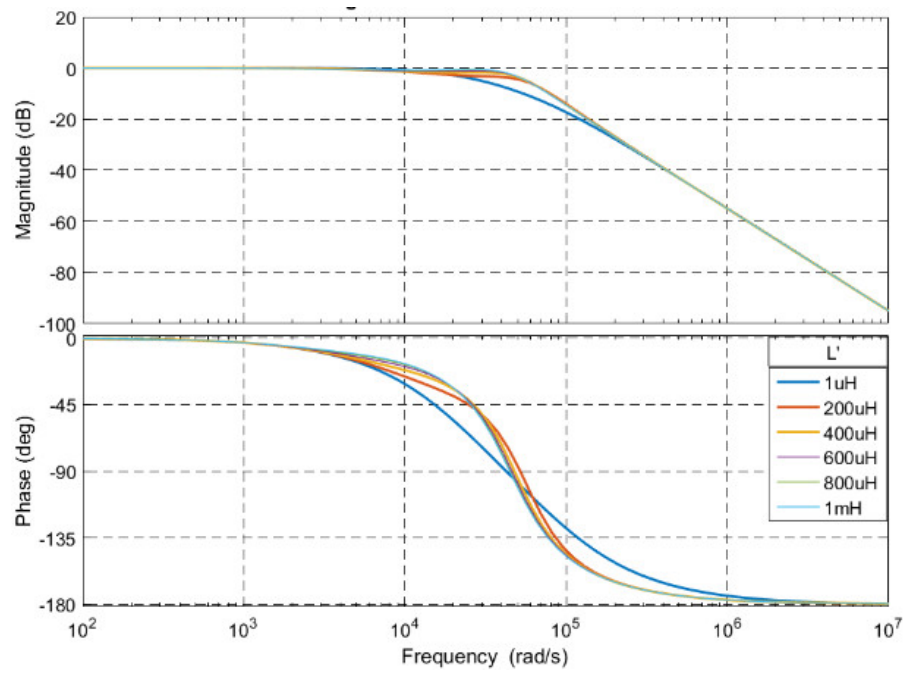


Figure 3.14: Bode plot of the system transfer function at RL load with virtual resistance.

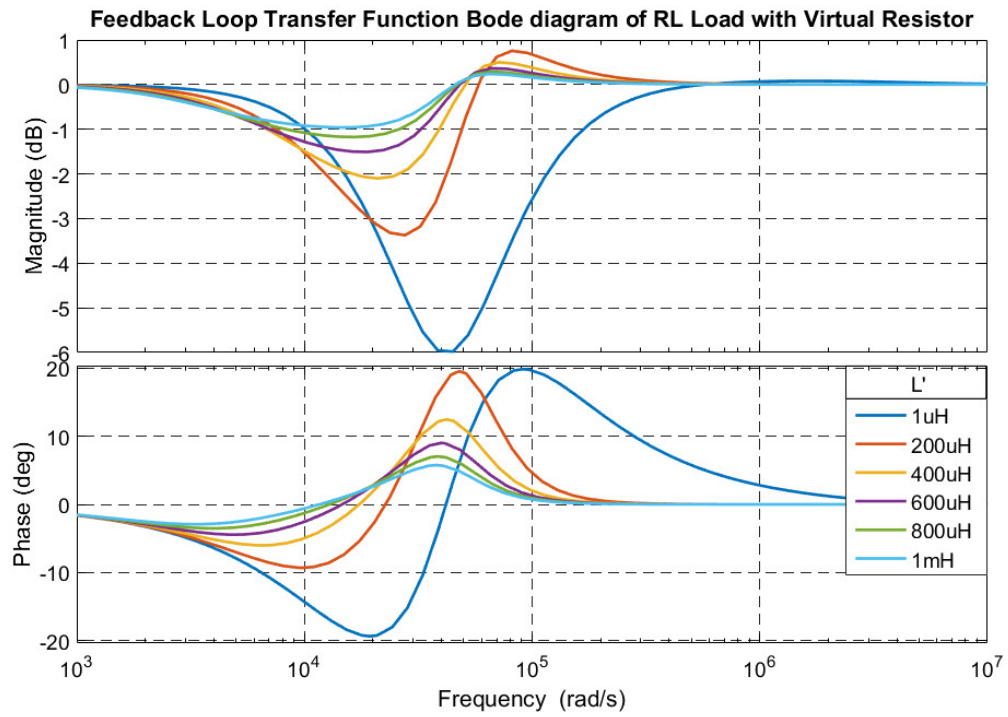


Figure 3.15: Bode plot of the feedback loop transfer function with virtual resistance.

connected inductance for each curve varies from 1 μH to 1 mH. The comparison of Figure 3.13 and Figure 3.14 shows that as the load inductance increases, the resonant frequency shifts to lower values, but the gain at the resonance point is reduced with the virtual resistance being introduced.

In Figure 3.15, the performance of the transfer function of the feedback loop can also be treated as a notch filter that suppresses the harmonics gain at the resonance frequency. Thus, the virtual resistor is applicable for the R_L load case.

3.3.3 Resistance–Capacitive Load

When the load is the switching mode power supply (SMP), it can be modeled as the resistive-capacitive load. Under this circumstance, the corresponding load impedance can be expressed as (3.28).

$$Z_{RC}(s) = R_L + \frac{1}{C's} \quad (3.28)$$

where C' is the equivalent serial-connected capacitance of the RC load. In (3.17), replacing R_L with Z_{RC} changes the system transfer function as:

$$\frac{v_{C-RC}}{v_{spwm-RC}}(s) = \frac{C'R_L s + 1}{R_L L C C' s^3 + L C s^2 + (L + R_L C')s + 1} \quad (3.29)$$

The corresponding system bode plot at different loads is shown in Figure 3.16. The series-connected capacitance varies from 1 μF to 200 μF .

Similar to the pure resistive load and resistance-inductive load, as the load capacitance C' increases, the gain at the resonance point increases as well. We can attempt to apply the virtual resistor again.

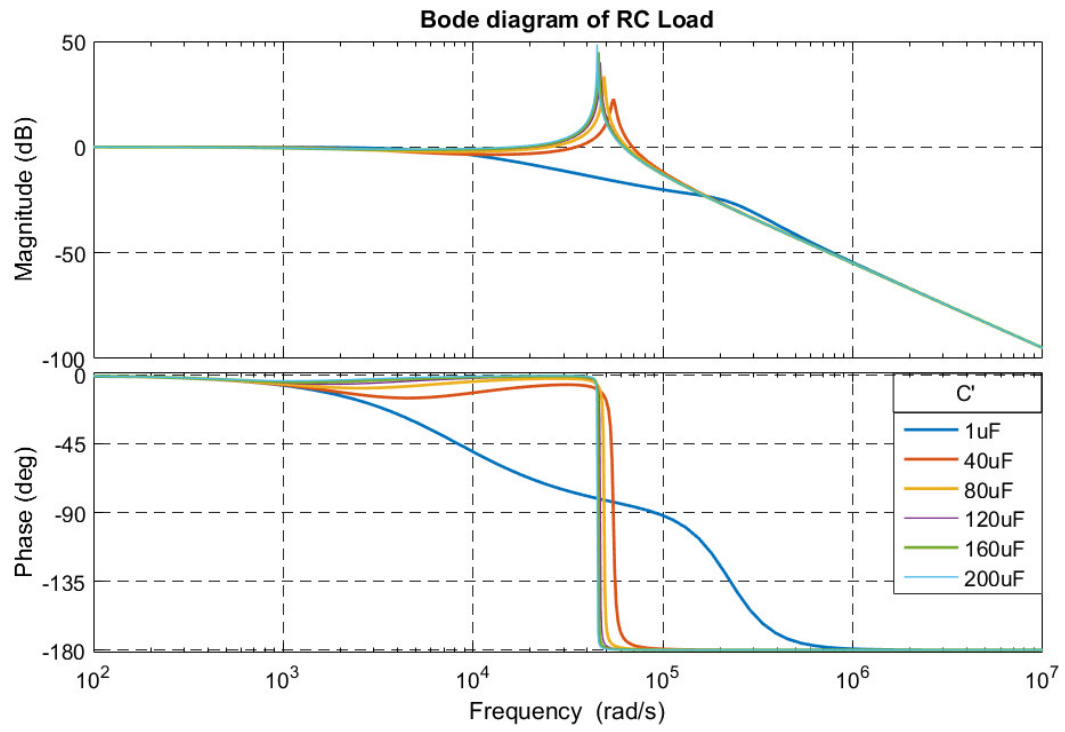


Figure 3.16: System transfer function bode plot with RC load.

Assuming a virtual resistor R_v is paralleled with the resistive-capacitive load, we can derive the equivalent load impedance as:

$$Z'_{RC-v}(s) = \left(R_L + \frac{1}{C's} \right) // R_v \quad (3.30)$$

Based on a similar analysis, the system with the virtual resistance has the transfer function formulated as (3.30), with the bode plot shown in Figure 3.17.

$$\frac{v_{c-RC-v}}{v_{spwm-RC-v}} = \frac{R_v C' R_L s + R_v}{R_L R_v L C C' s^3 + (R_v L C + R_v L C' + R_L L C') s^2 + (R_L R_v C' + L) s + R_v} \quad (3.31)$$

$$F_{RL}(s) = \frac{R_L^2 R_v L C' C s^3 + [R_L L C' (R_L + R_v) + R_v L C R_L] s^2 + (L R_L + R_v R_L^2 C') s + R_v R_L}{R_L^2 R_v L C C' s^3 + (R_L R_v L C + R_L R_v L C') s^2 + (R_v L + R_L^2 R_v C') s + R_v R_L} \quad (3.32)$$

According to Figure 3.17, the gain at the resonance point is effectively reduced compared to Figure 3.16 because of the virtual resistance.

Furthermore, according to (18) and (31), the feedback transfer function $F_{RC}(s)$ can be shown in (3.32), with the corresponding bode plot at $R_v=4.2 \Omega$ shown in Figure 3.18. It indicates that the overall open loop system performance is still a notch filter at the resonance frequency, i.e., the virtual resistor is valid for the RC load scenario.

3.4 Simulation Result

3.4.1 Simulation of the Virtual Resistance

Simulation results are shown in Figure 3.19 to verify the effectiveness of virtual resistance damping. In Figure 3.19, the DC bus voltage $V_{dc}=500$ V, resistive load $R_L=23 \Omega$ for each phase, the output line-line voltage $V_{L-L}=208$ V and $R_v=4.2 \Omega$. As observed in Figure 3.19(a),

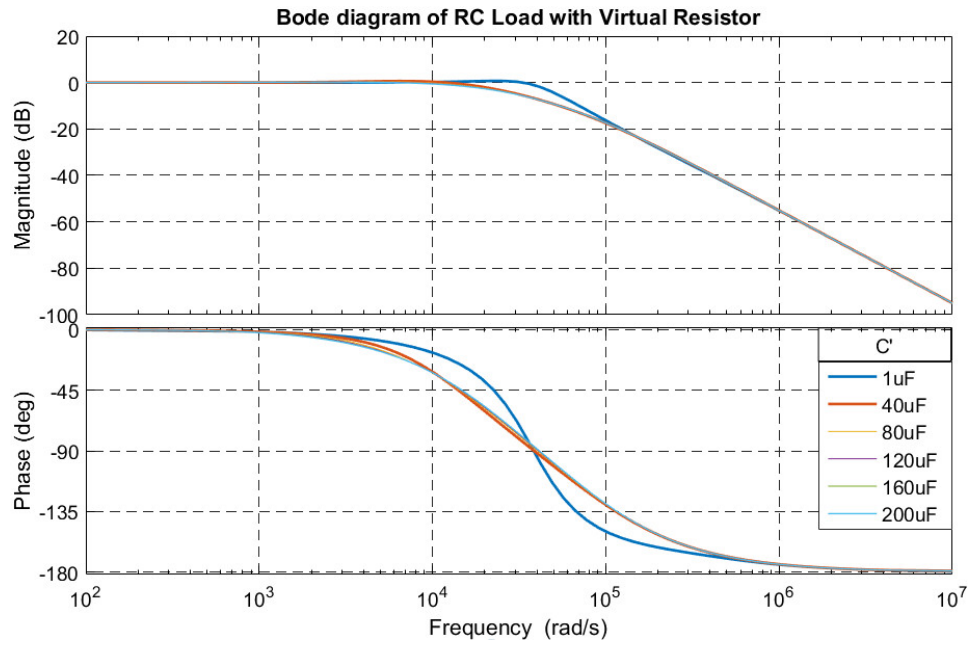


Figure 3.17: Bode plot of the system transfer function under the RC load with virtual resistance.

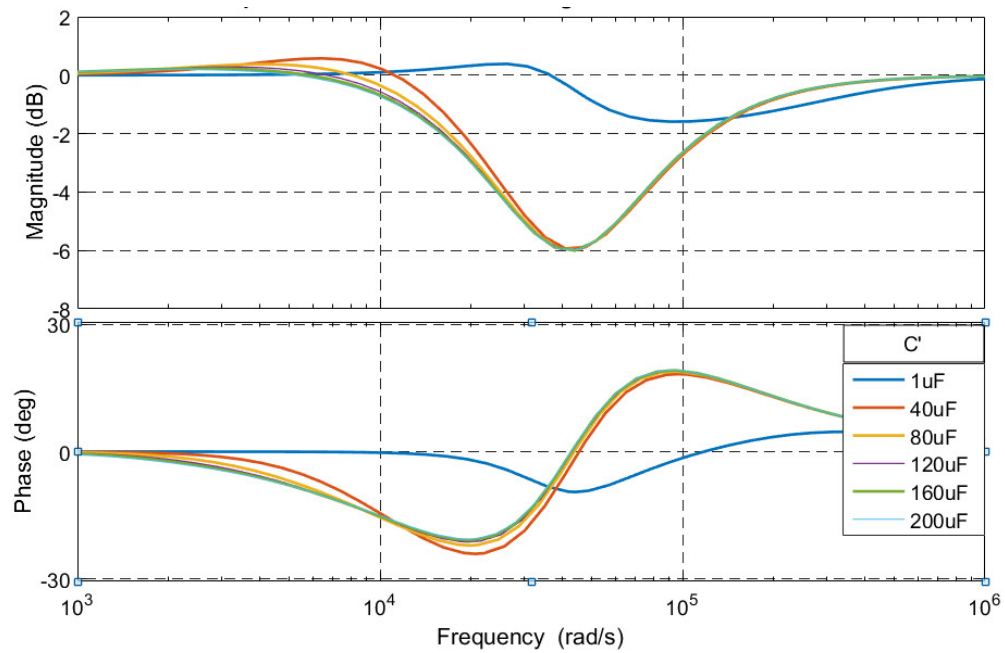
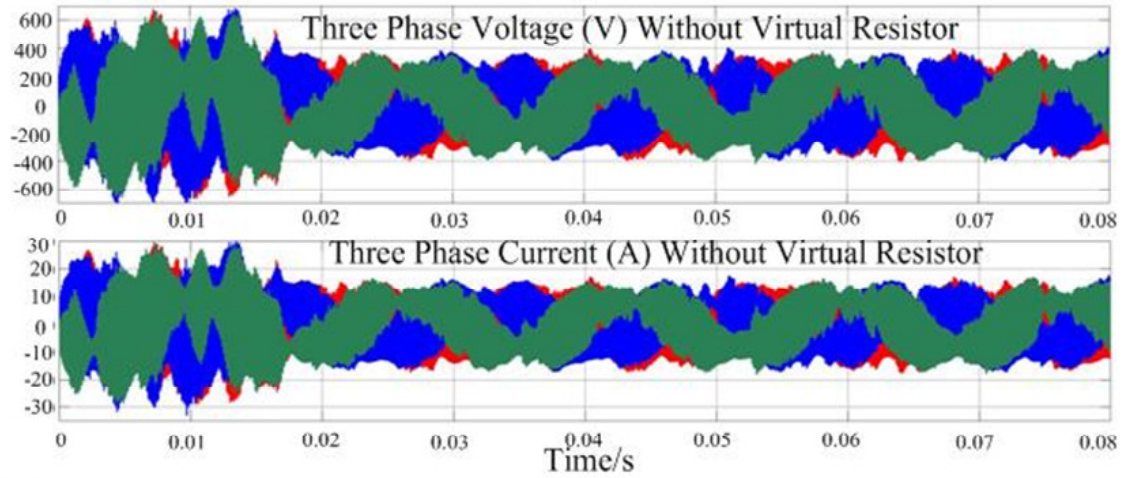
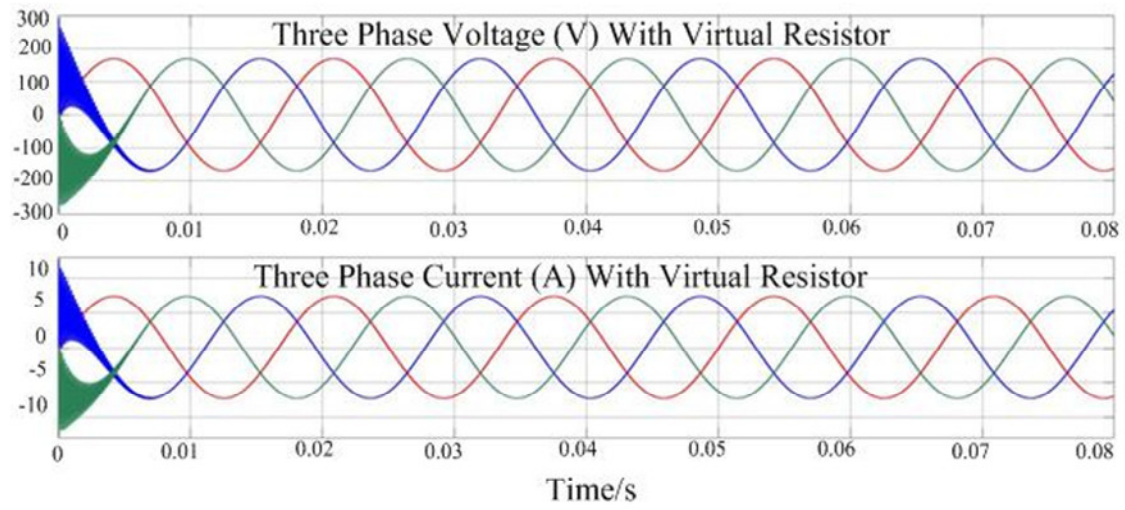


Figure 3.18: Bode plot of the feedback loop transfer function with virtual resistor for the RC load.



(a)



(b)

Figure 3.19: Simulation results for 2 kW output power.

(a) Output waveforms without virtual resistance,

(b) Output waveforms with virtual resistance.

the output voltage and current contain high-frequency harmonics. In Figure 3.19(b), the output voltage is much smoother with the virtual resistance.

As shown in Figure 3.20, the THD numbers of the PWM voltage with and without the virtual resistor are similar. The virtual resistor applied in the system greatly reduces the harmonics around the resonant frequency of the grid-side LC filter and pushes the voltage harmonics to the higher-frequency range, specifically around the switching frequency. This makes it easy to filter out the harmonics.

A 10 kW V2L simulation model is built with related simulation parameters listed in TABLE 3.1. The 10 kW steady-state simulation result is shown in Figure 3.21.

3.4.2 Simulation of the Neutral-point Control

To emulate the impact of the load asymmetry on the neutral-point voltage, the load resistance of Phase A and B is set to be $47\ \Omega$. The load on phase C is changed to $94.1\ \Omega$, $47\ \Omega$, and $23.5\ \Omega$, which makes the load current on Phase C equal to 1.275 A, 2.55 A, and 5.1 A, respectively.

With the neutral-phase control disabled, i.e., turning off S_{n1} and S_{n2} , the voltage of DC-link capacitors will oscillate with the frequency the same as that of the output voltage. As shown in Figure 3.22, the higher the load-unbalance rate, the larger the voltage oscillation of DC-link capacitors.

Substituting ΔI_c for 1.275 A, 2.55 A, and 5.1 A into (3.11), we obtained DC-link capacitor voltage oscillation as 43 V, 22.1 V, and 11.1 V, respectively, perfectly matching the simulation result in Figure 3.22. To enable the neutral phase (S_{n1} and S_{n2}) thereby effectively balancing the DC-link capacitor voltage, we need to sample the neutral inductor

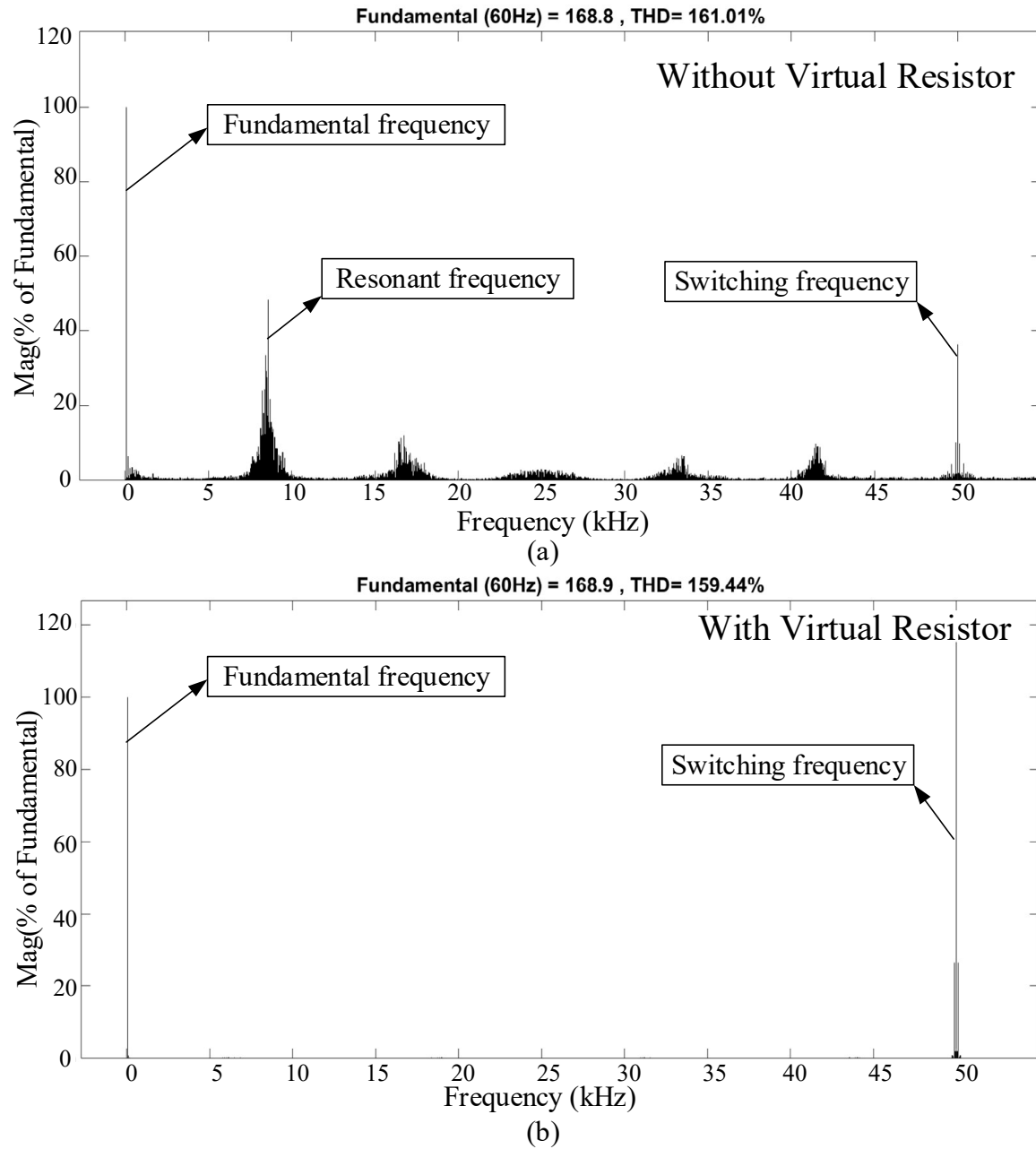


Figure 3.20: FFT analysis of the output phase voltage.

(a) FFT analysis of output voltage without virtual resistance,

(b) FFT analysis of output voltage with virtual resistance.

Table 3.1: Simulation parameters

Component/Parameter	Value
Grid filter inductance	120 μH
Grid filter capacitance	4.7 μF
DC-link capacitance C_{N1}, C_{N2}	220 μF
Neutral inductance	120 μH
Switching frequency	50 kHz
DC bus input voltage	500 V
Output voltage frequency	60 Hz
Output line-line voltage	208 Vrms
Virtual resistor R_v	4.2 Ω
Unbalance current ΔI_c	1.275/2.55/5.1 A

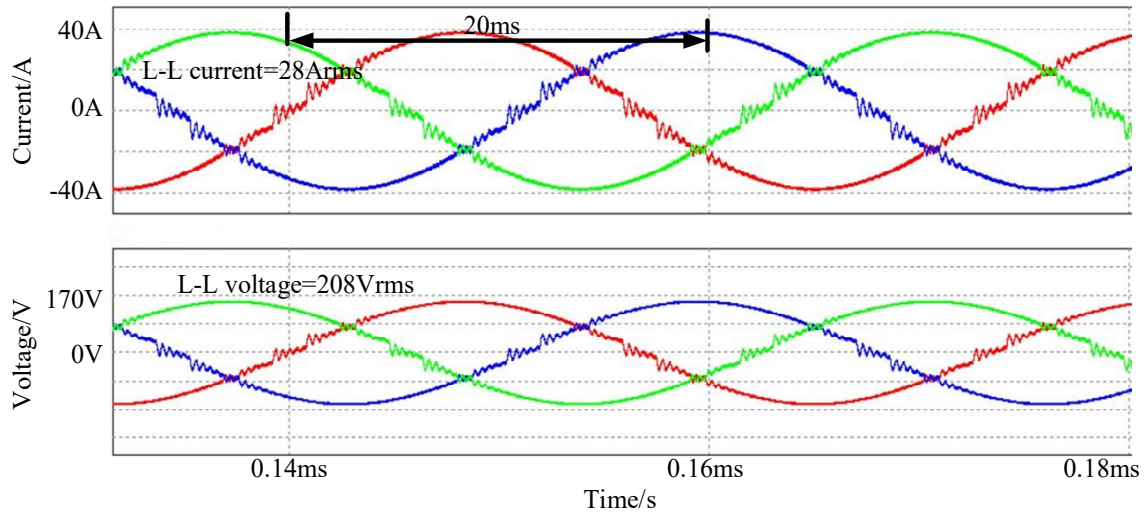


Figure 3.21: Output waveform of the steady-state system with resistive load.

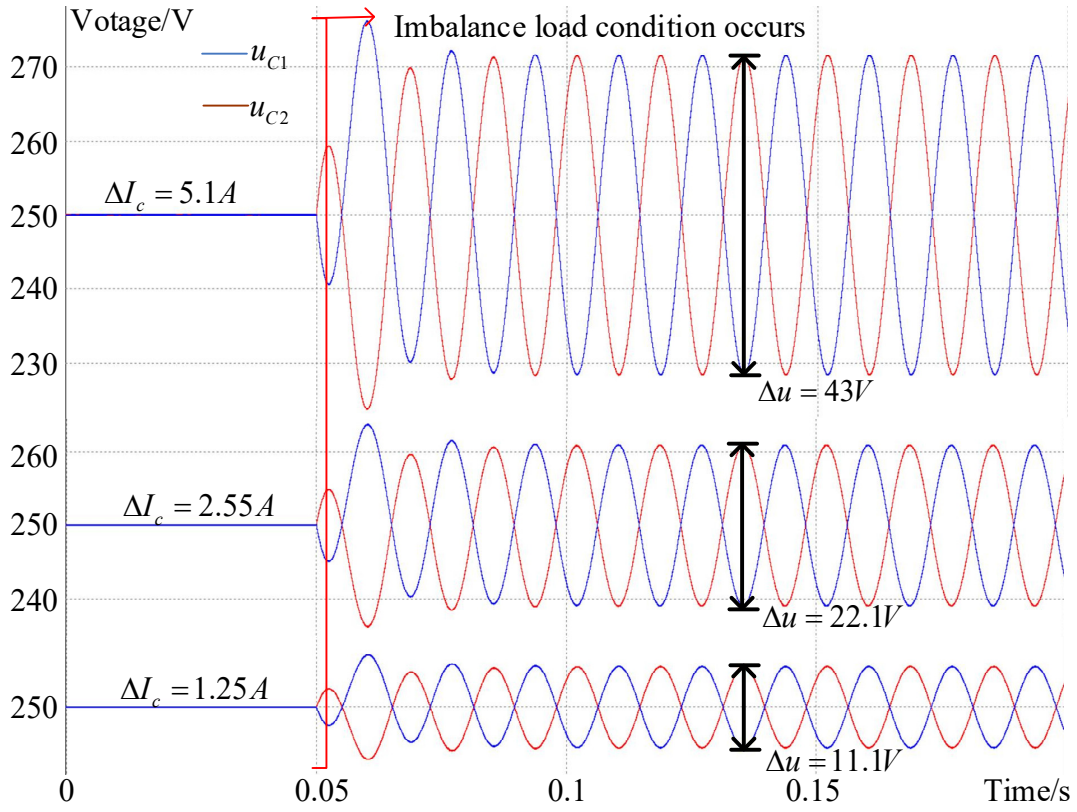


Figure 3.22: DC-link capacitor voltage oscillation at different unbalance current ΔI_c .

current, DC-link high-side, and low-side capacitor voltage. As shown in Figure 3.23(a) under resistive load, the output line-line voltage is 208 Vrms. When the three-phase load is balanced, the neutral current is zero. At $t=0.03$ ms, another load resistance is added to one phase, creating the neutral-point current in the middle plot. Enabling the fourth leg then yields the ± 5 V neutral-point voltage difference. Meanwhile, simulation results of the resistance-inductive load and resistance-conductive load are shown in Figure 3.23(b) and (c), respectively. $47\ \Omega/500\ \mu\text{H}$ is for the resistance-inductive load and $47\ \Omega/100\ \mu\text{F}$ is for the resistance-capacitive load. At $t=0.03$ ms, another resistor is paralleled to $47\ \Omega$ and keeping the $500\ \mu\text{H}$ and $100\ \mu\text{F}$ in the system. Simulation results validated the effectiveness of the proposed neutral-point voltage control, i.e., the method suppresses the oscillation of the DC-bus voltage at the asymmetric load scenario.

3.5 Experimental Validation

To validate the V2H function, a charger prototype is built as shown in Figure 3.24(a), where split DC-link capacitors are formed by two film capacitors in a series connection. The whole charger contains two stages. In addition to the three-phase four-wire inverter used as the AC/DC stage, the other stage is a bidirectional DC/DC converter. To realize the high efficiency and high power density, SiC MOSFETs from Rohm, SCT3030KL (1200 V, 72 A) and SCT3022AL (650 V, 93 A) are applied for AC/DC and DC/DC stages, respectively. A Digital Signal Processor TMS320F28335 is used for each stage. The switching frequency of the DC/DC stage is 100~200 kHz and that of the PFC stage is 50 kHz. The onboard battery pack has a voltage range of 250~400 V DC and the expected output voltage is three-phase 208~480 V AC. The DC/DC stage employs the

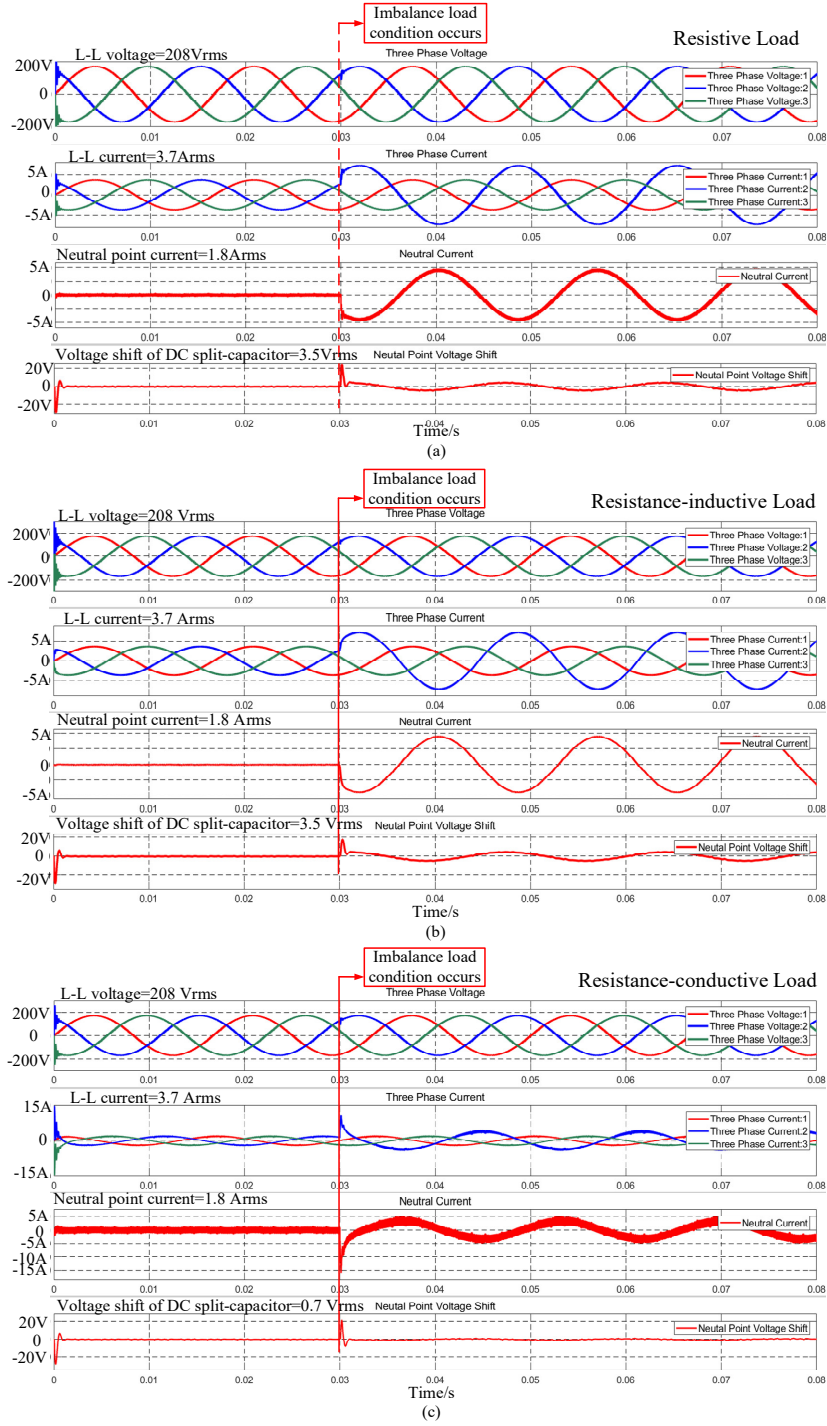
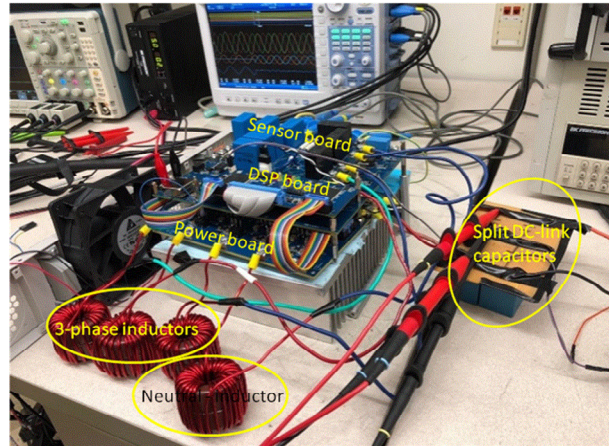


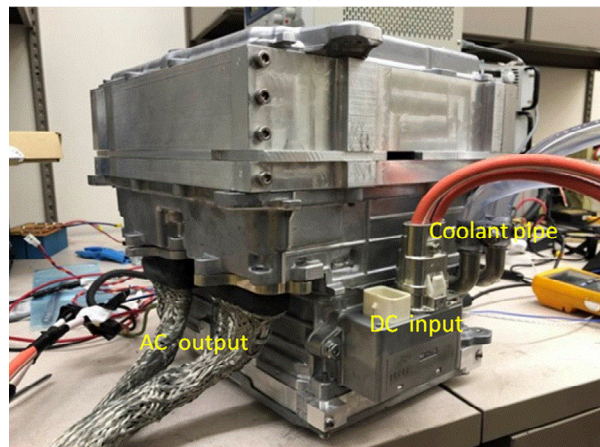
Figure 3.23: Dynamic balancing waveform with different loads @ $R_v=4.2 \Omega$.

(a) Resistive load ($R_L=47 \Omega$), (b) Resistance-inductive load ($R_L=47 \Omega$, $L'=500 \mu\text{H}$),

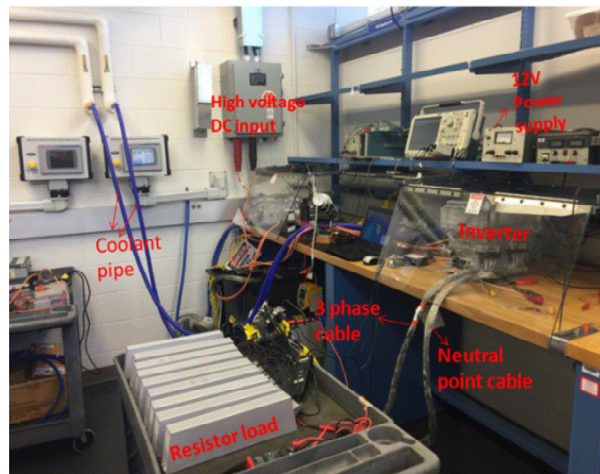
(c) Resistance-conductive load ($R_L=47 \Omega$, $C'=100 \mu\text{F}$).



(a)



(b)



(c)

Figure 3.24: Three-phase four-wire inverter.

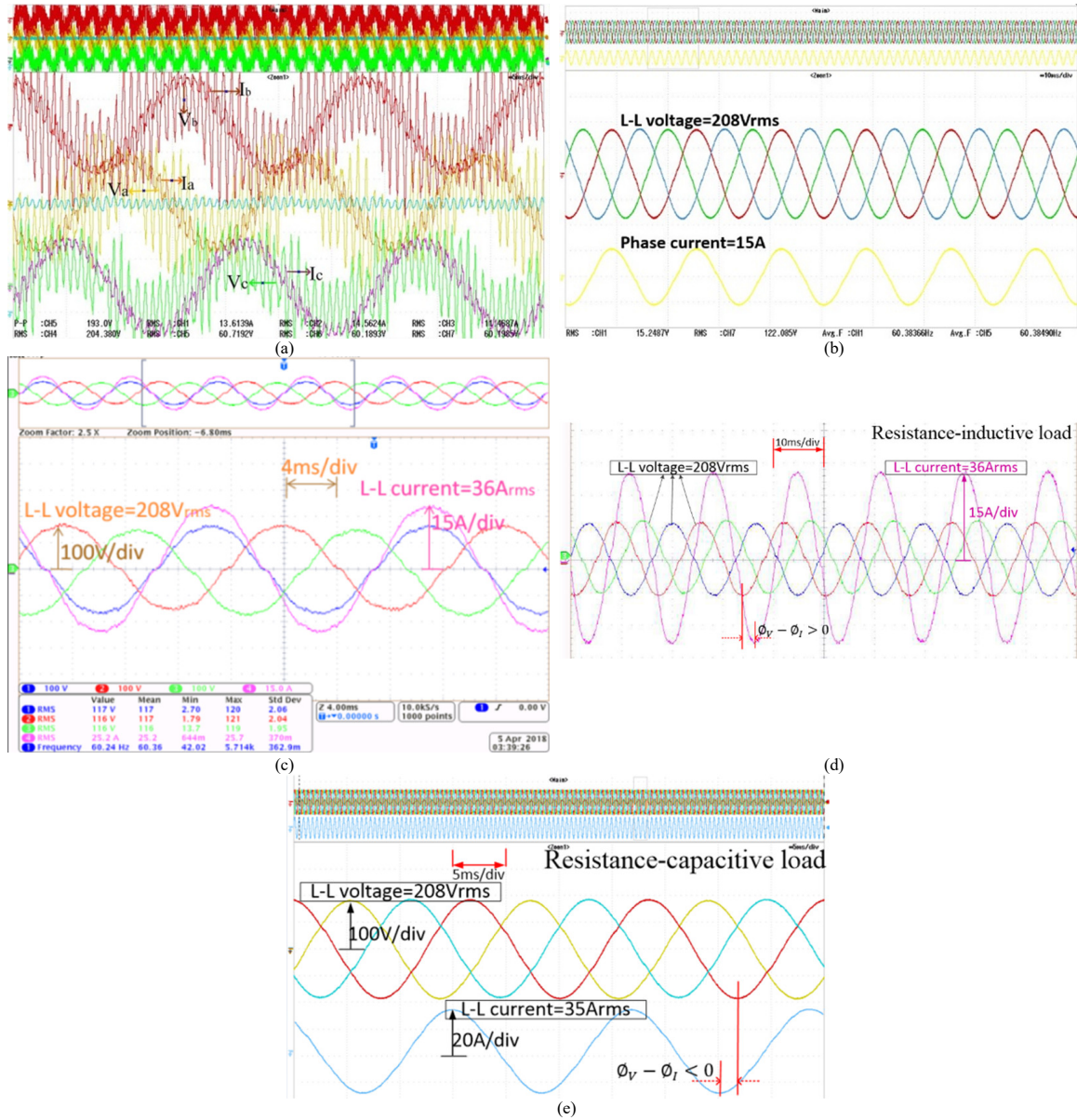
(a) System prototype, (b) On-board enclosure, (c) Onsite test bench setup.

voltage control to keep the DC-bus voltage at around 500 V. Since the focus of this chapter is on the inverter stage, the DC/DC part, which is the DAB with single phase shift control, will not be detailed here. Figure 3.24(b) shows the charger that is fitted into the onboard enclosure with the water-cooling system. The overall test bench is shown in Figure 3.24(c), where the equipment is provided by Ford on-site test lab. The load is resistive and rated at 10 kW.

Figure 3.25 shows the output voltage and current of each phase with different virtual resistance under a balanced load. A comparison of Figure 3.25(a) and (b) indicates that the virtual resistor suppressed the resonant harmonics significantly. Experimental results of the resistive load, resistance-inductive load, and resistance-capacitive load are shown in Figure 3.25(c), (d), and (e), respectively.

The load resistance of each phase is 47 Ω . Another 47 Ω resistance is paralleled to Phase C to create the load unbalance. Figure 3.26(a)~(b) shows the output voltage, output current, and the voltage of each split DC-link capacitor when the neutral balancing control is disabled. When applying the neutral-point voltage control, the corresponding result is shown in Figure 3.27(a)~(b).

A comparison of Figure 3.26 and Figure 3.27 indicates that without the neutral-point voltage control, the load unbalances create the neutral line current, which subsequently leads to the voltage oscillation on both the phase output and DC-link capacitors. With the neutral-point voltage control method, the voltage oscillation is drastically suppressed, avoiding the potential neutral-point unbalance, and stabilizing the three-phase output voltage, which greatly enhances the system performance in the V2L mode.



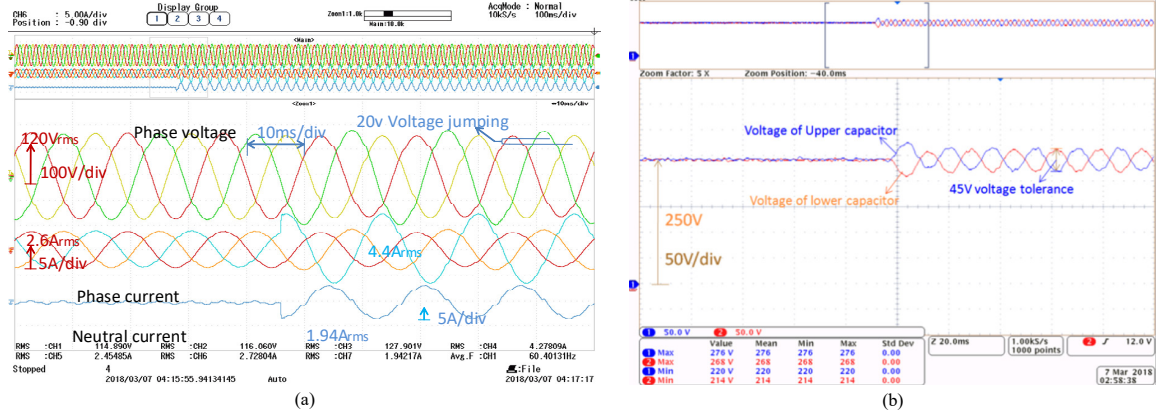


Figure 3.26: Unbalanced load test without neutral-point control.

(a) Three-phase output voltage and current, (b) Voltage of split DC-link capacitors.

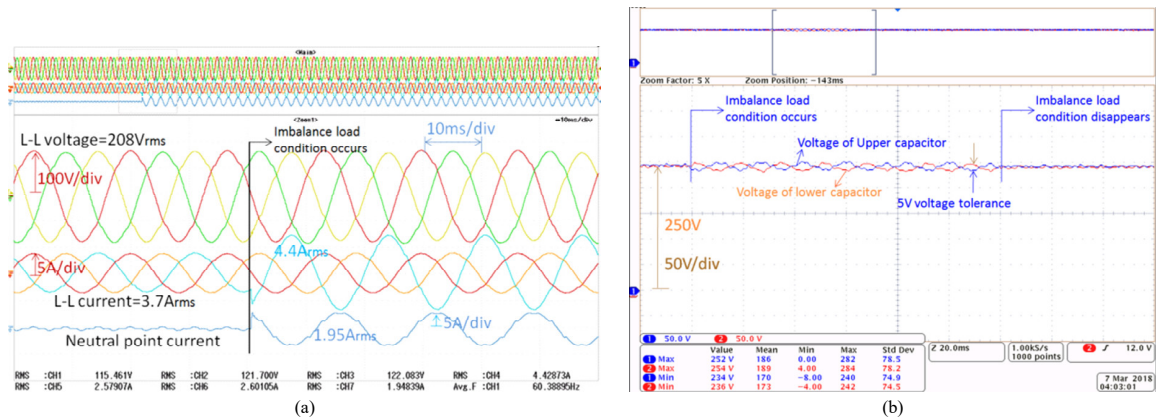


Figure 3.27: Unbalanced load test with neutral-point control.

(a) Three-phase output voltage and current, (b) Voltage of split DC-link capacitors.

3.6 Summary

This chapter designed a three-phase four-wire inverter for the V2L application. Utilizing split DC-link capacitors and another leg effectively deals with the load unbalance and suppresses the voltage oscillation of the neutral-point and phase output. The mathematical model is built to analyze the relationship between voltage oscillation and the unbalance rate. The virtual resistance is introduced to damp the harmonics at the resonant point to strengthen the system reliability and output quality. Note such virtual resistance is not only valid for the resistive load, but also the RC and RL load, and thus widens the V2L application.

A MATLAB/Simulink model is used to confirm the control strategy and system parameter selection for the 10 kW scenario. Finally, a 10 kW prototype is built and successfully realized the load-unbalance control. The main contribution of this chapter is:

- (1) Applying the virtual resistance to the phase voltage of the EV charger to generate the smooth AC voltage at the V2L mode.
- (2) Validating the design effectiveness to deal with the unbalanced load and various other types of loads, e.g., R, RC, and RL.

Chapter 4 THREE-PHASE INVERTER

COMMON-MODE VOLTAGE MODELING

This chapter concentrates on the common-mode voltage modeling and analytical characterization for various modulation schemes.

The need for analytical models and tools to investigate common-mode (CM) and differential-mode (DM) signals in motor drive systems is evident in previous literature, which focuses on simulations and experiments. In this chapter, an analytical model of CM voltage for various PWM schemes is presented as a double Fourier integral, and the DM current is described by mathematical equations. The model is applied to different modulation schemes such as space vector PWM (SVPWM), discontinuous PWM (DPWM), and active zero state PWM (AZSPWM) for two-level and three-level multiphase inverters. The impact of these four modulation schemes on the CMV and DMI are comprehensively compared across varying modulation indices. In this system, a high-resolution field-programmable gate array is used to implement the control algorithm and assess the impact of control bandwidth on CMV and DMI.

The structure of this chapter is organized as the following. In Section 1 the CMV modeling will be presented. In Section 2, DM current ripple analysis will be performed to evaluate the DM performance. Four different PWM methods are compared to each other through theoretical analysis and simulation in both CM and DM viewpoints in Section 3. Section 4 gives the experimental verification of CM reduction performance. Furthermore, Section 5 discusses how the control bandwidth affects CM and DM performance, and Section 6 extends the analysis to a three-level NPC inverter.

4.1 CMV Analysis for Different PWM Patterns

4.1.1 CM Modulation Signal

As shown in Figure 4.1(a), conventional center-aligned SVPWM results in the CMV with a peak of $\pm V_{dc}/2$. For AZSPWM, pulses are inversely aligned with the medium-length duty cycle of the three phases. This modulation scheme avoids the adoption of zero vectors, which reduces the peak of CMV to $\pm V_{dc}/6$. DPWM1 and DPWMMin also reduce the CMV by shaving the peak to either $+V_{dc}/2$ or $-V_{dc}/2$ in each switching cycle, as shown in Figure 4.1(c)~(d). Nevertheless, all these SVM methods listed in Figure 4.1 are a combination of SPWM and an injected 3rd-order CM modulation signal [126]. The main difference between different PWM patterns lies in the corresponding CM modulation signals. Figure 4.2(a)~(d) shows the modulation signal and CM modulation signal for SVPWM, DPWM1, and DPWMMin at high (0.8) and low (0.2) modulation index (MI) scenarios, respectively.

Eqn (4.1) gives the modulation index of space vector modulation (SVM). Under this definition, the maximum linear modulation index is 0.906. Note that there are still some other modulation methods having the CMV reduction capability, for instance, remote state PWM (RSPWM) and near state PWM (NSPWM). These two PWM schemes have limited DC-bus-voltage utilization, e.g., 0.61-0.907 for NSPWM, and <0.58 for RSPWM, which severely limits the motor operation range. Therefore, these PWM methods will not be discussed here.

$$MI = \frac{\pi}{2} \frac{V_{ref}}{V_{dc}} \quad (4.1)$$

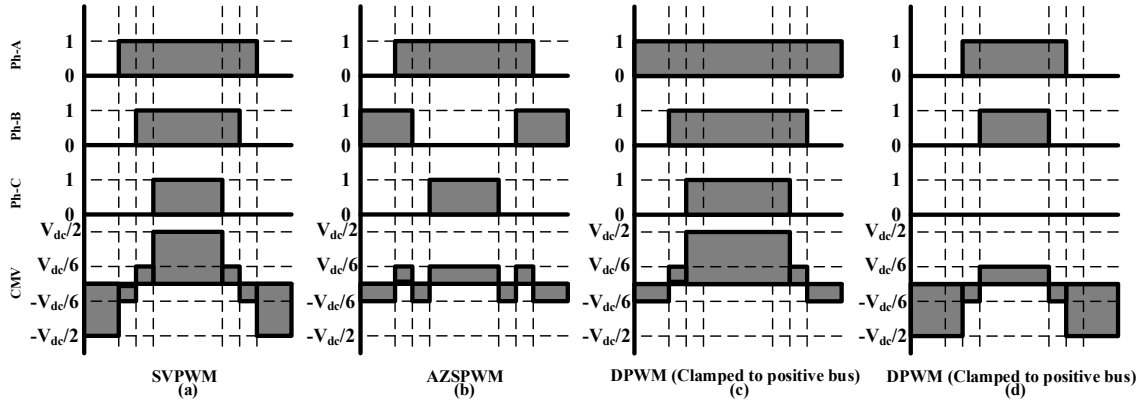


Figure 4.1: Various SVM pulse patterns and CMV distribution.

(a) SVPWM, (b) AZSPWM,

(c) DPWM-positive bus clamping, (d) DPWM-negative bus clamping.

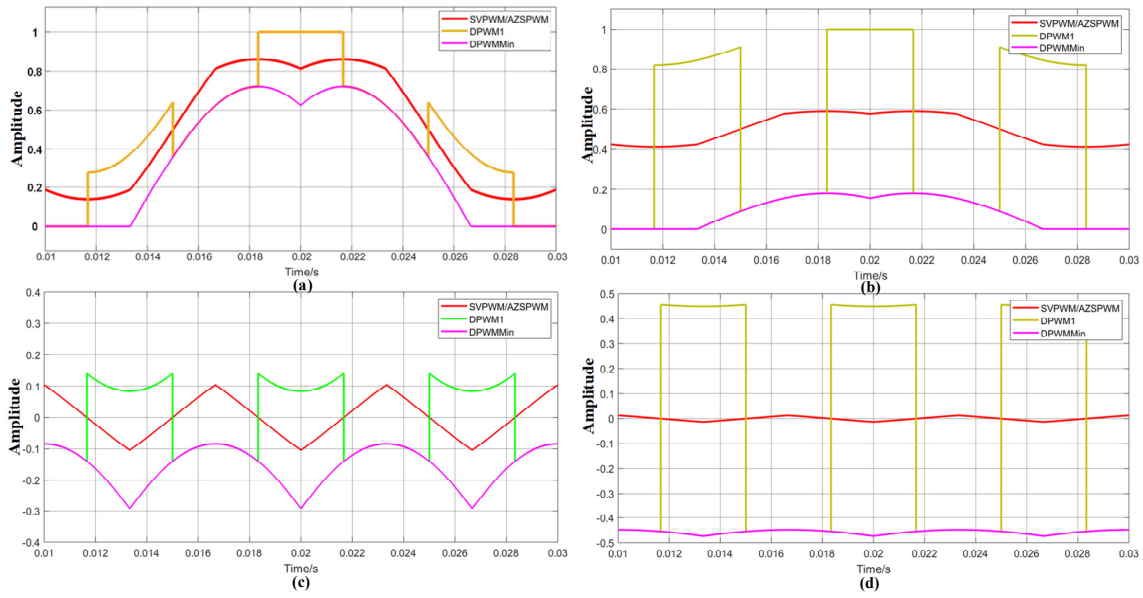


Figure 4.2: Modulation signal of SVPWM, AZSPWM, DPWM1, and DPWMMin.

(a) @MI=0.8, (b) @MI=0.2.

CM modulation signal of SVPWM, AZSPWM, DPWM1, and DPWMMin.

(c) @MI=0.8, (d) @MI=0.2.

When running at the same speed and torque, all four PWMs have the same fundamental frequency. However, their CM modulation signals result in different CMV distributions. The FFT result of the CM modulation signals, as shown in Figure 4.3, indicates that DPWM will bring higher CMV in lower modulation indices. In this simulation, the fundamental frequency (f_0) was set to 50 Hz. DPWMMin draws high CMV within the frequency range of $0 \sim 3f_0$ and DPWM1 draws high CMV in the frequency of $>3f_0$. This is particularly true when the modulation index is low, as validated in Fig. 4.3 where $MI=0.2$.

Figure 4.4(a)~(d) shows the CMV spectrum of SVPWM, AZSPWM, DPWM1, and DPWMMin at high modulation index (0.8) and low modulation index (0.2) with the zoomed-in view at the switching frequency point, respectively. The fundamental frequency is 50 Hz (f_0), $f_s=10$ kHz and the DC-link voltage is 150 V. Several conclusions can be drawn:

- (1) In the low-frequency range ($<3f_0$), DPWMMin has a higher CMV than others. For the frequency of $3f_0 \sim f_s$, DPWM1 always has a higher CMV. These can be explained by the FFT analysis shown in Figure 4.4.
- (2) SVPWM and AZSPWM have almost the same performance excluding the carrier harmonics (integer numbers of f_s). At f_s , AZSPWM reduces the CMV sharply compared with SVPWM. However, the sideband near f_s for AZPWM increases, which cannot be explained by the FFT analysis shown in Figure 4.3 and 4.4. The existence of such sideband CMV questions whether AZSPWM has the best CMV reduction.

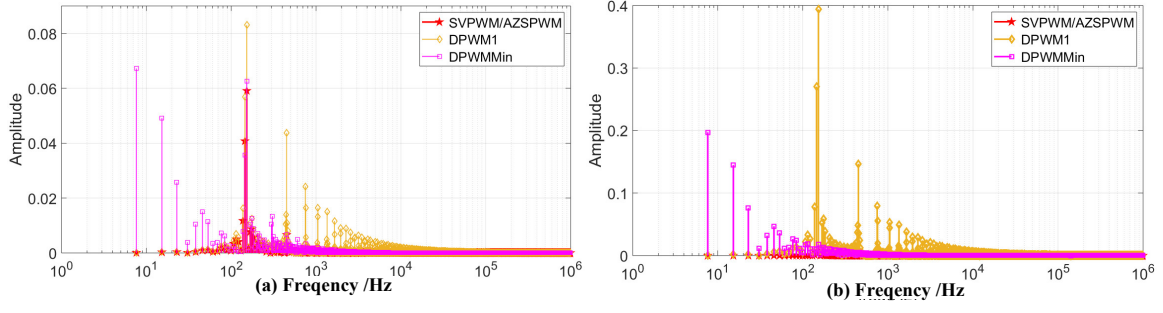


Figure 4.3: FFT result for CM modulation signal of SVPWM, AZSPWM, DPWM1, and DPWMMin.

(a) @ $MI=0.8$, (b) @ $MI=0.2$.

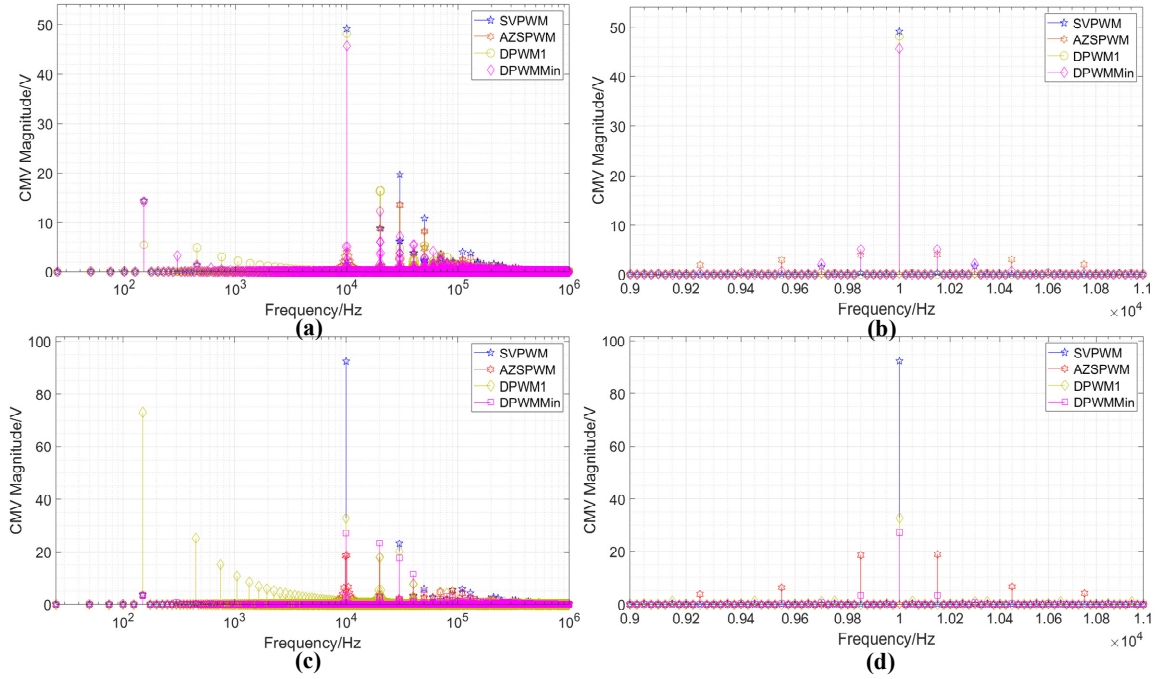


Figure 4.4: CMV spectrum of SVPWM, AZSPWM, DPWM1, and DPWMMin.

(a) @ $MI=0.8$ Wide frequency range, (b) @ $MI=0.8$ Zoomed-in view @ f_s ,

(c) @ $MI=0.2$ Wide frequency range, (d) @ $MI=0.2$ Zoomed-in view @ f_s .

4.1.2 CMV Modeling with Double Fourier Integral

It is essential to use a low-frequency modulation waveform to compare with a high-frequency carrier waveform in any PWM method. The phase leg outputs a series of pulses switching between the upper and lower DC bus, which not only have the fundamental component but also incorporate a series of unwanted harmonics due to switching processes [127]. Double Fourier integral (DFI) analysis is a mathematical tool that can provide analytical solutions to precisely identify harmonic components of a PWM signal. In inverter applications, assume the target function ($f(t)$) is the voltage between the middle point of the phase leg and the middle point of the DC bus. $f(t)$ is a cyclic signal related to both $x(t)$ and $y(t)$ with period= 2π . Here, $x(t)=\omega_s t+\theta_s$ and $y(t)=\omega_0 t+\theta_0$, representing the time variation of the high-frequency modulating wave and low-frequency modulated wave, respectively. By doing the DFI analysis on the PWM waveform, $f(t)$ can be expanded as (4.2).

$$\begin{aligned}
 f(x,y) = & \frac{A_{00}}{2} + \sum_{n=1}^{\infty} \left\{ A_{0n} \cos(n(\omega_0 t + \theta_0)) + B_{0n} \sin(n(\omega_0 t + \theta_0)) \right\} \\
 & + \sum_{m=1}^{\infty} \left\{ A_{m0} \cos(m(\omega_s t + \theta_s)) + B_{m0} \sin(m(\omega_s t + \theta_s)) \right\} \\
 & + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left\{ A_{mn} \cos(m(\omega_s t + \theta_s) + n(\omega_0 t + \theta_0)) + B_{mn} \sin(m(\omega_s t + \theta_s) + n(\omega_0 t + \theta_0)) \right\}
 \end{aligned} \tag{4.2}$$

where m is the carrier index variable, n is the baseband index variable, and

$$\begin{cases} A_{mn} = \frac{1}{4\pi} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x,y) \cos(mx + ny) dx dy \\ B_{mn} = \frac{1}{4\pi} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x,y) \sin(mx + ny) dx dy \end{cases} \tag{4.3}$$

Eqn (4.2) divides the target function into 4 parts. The first term corresponds to the DC offset of the PWM waveform. Its existence depends on the reference point, which can be chosen as the lower DC bus or middle point of the DC bus. The second term represents the components of the fundamental frequency and its baseband harmonics. The third item represents the carrier wave harmonics, which are high-frequency components such as f_s , $2f_s$, and $3f_s$. The final double summation term is the entire group of all possible frequencies that appear as groups around the carrier harmonics frequencies. For example, $f_s \pm f_0$, $f_s \pm 2f_0$, $2f_s \pm 3f_0$, etc. The high-frequency components and the sideband group are the main objects to be analyzed.

For specific PWM schemes, according to (4.2) and (4.3), the Fourier coefficients A_{mn} and B_{mn} should be determined through DFI. For the conventional SVPWM, the integral bounds follow the shape of corresponding modulation waveforms. Figure 4.5 shows the integral bounds for SVPWM and DPWMMin, both at full modulation index within one periodical area $(-\pi, \pi)$.

Theoretically, AZSPWM will share the same modulation waveform as SVPWM. The only difference is, to inversely align the medium-length duty in half of the six sectors, PWM pulses need to be shifted by half of the switching period. Therefore, an equivalent DFI model specifically for AZSPWM is built, as shown in Figure 4.6. Assume the PWM duty cycle is D . Logically, to shift this PWM by 180° , the first step is to generate another PWM with the duty cycle equal to $1-D$. By reversing the polarity of the newly generated PWM, the 180° -shifted PWM is obtained.

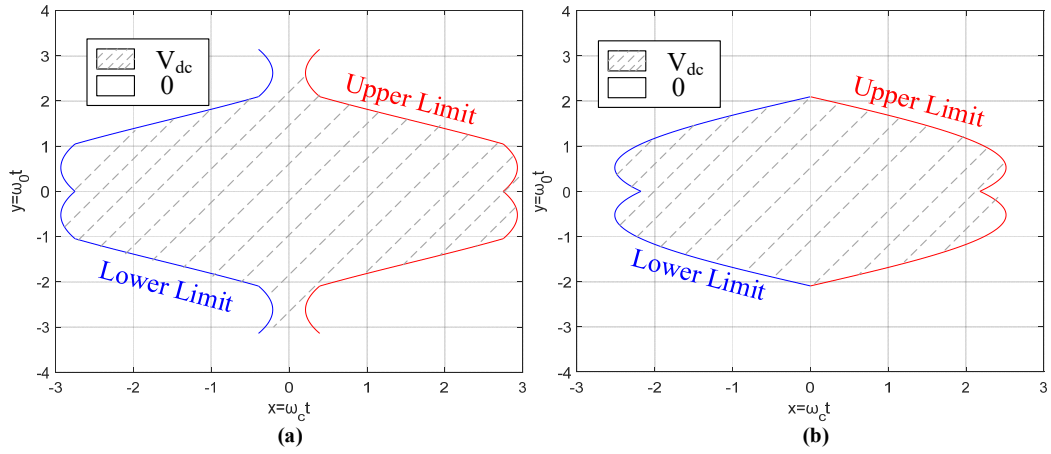


Figure 4.5: DFI integral bounds.

(a) SVPWM, (b) DPWMMIn.

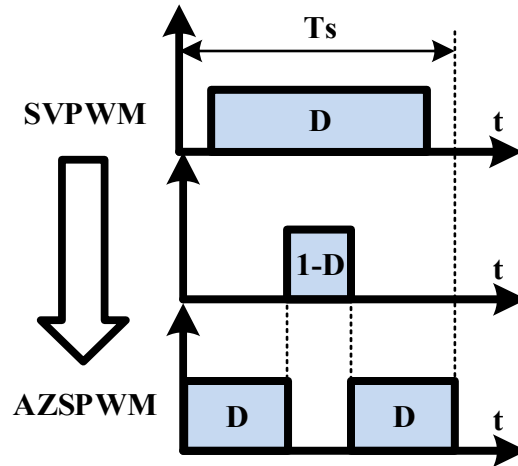


Figure 4.6: AZSPWM generation logic.

According to the logic operation derived above, the integral bounds of AZSPWM are redrawn in Fig. 4.7.

It is worth noting that only flipping the integral bounds in Figure 4.7 is not enough. During the integration, the upper and lower limits of the related section should also be swapped according to the AZSPWM generation logic in Figure 4.6. Hence, the DFI model for AZSPWM is generated as Eqns (4.4) ~ (4.6). By substituting different m and n , the carrier harmonics and sideband components can be calculated.

$$\begin{aligned}
A_{mn} + jB_{mn} = & \int_{-\pi}^{-\frac{2\pi}{3}} \int_{-\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{\pi}{6}\right)\right]}^{\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{\pi}{6}\right)\right]} e^{j(mx+ny)} dx dy \\
& + \int_{-\frac{2\pi}{3}}^{-\frac{\pi}{3}} \int_{-\frac{\pi}{2}\left[1+\frac{3}{2}M\cos(y)\right]}^{\frac{\pi}{2}\left[1+\frac{3}{2}M\cos(y)\right]} e^{j(mx+ny)} dx dy \\
& + \int_{-\frac{\pi}{3}}^0 \int_{-\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{\pi}{6}\right)\right]}^{\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{\pi}{6}\right)\right]} e^{j(mx+ny)} dx dy \\
& + \int_0^{\frac{\pi}{3}} \int_{\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{5\pi}{6}\right)\right]}^{-\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{5\pi}{6}\right)\right]} e^{j(mx+ny)} dx dy \\
& + \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} \int_{\frac{\pi}{2}\left[1+\frac{3}{2}M\cos(y)\right]}^{-\frac{\pi}{2}\left[1+\frac{3}{2}M\cos(y)\right]} e^{j(mx+ny)} dx dy \\
& + \int_{\frac{2\pi}{3}}^{\pi} \int_{\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{5\pi}{6}\right)\right]}^{-\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{5\pi}{6}\right)\right]} e^{j(mx+ny)} dx dy
\end{aligned} \tag{4.4}$$

$$V_{ao} = \left| A_{mn} + jB_{mn} \right| \frac{V_{dc}}{2\pi^2} \tag{4.5}$$

$$V_{CM} = \frac{V_{ao} \left[1 + 2\cos\left(2n \cdot \frac{2\pi}{3}\right) \right]}{3} \tag{4.6}$$

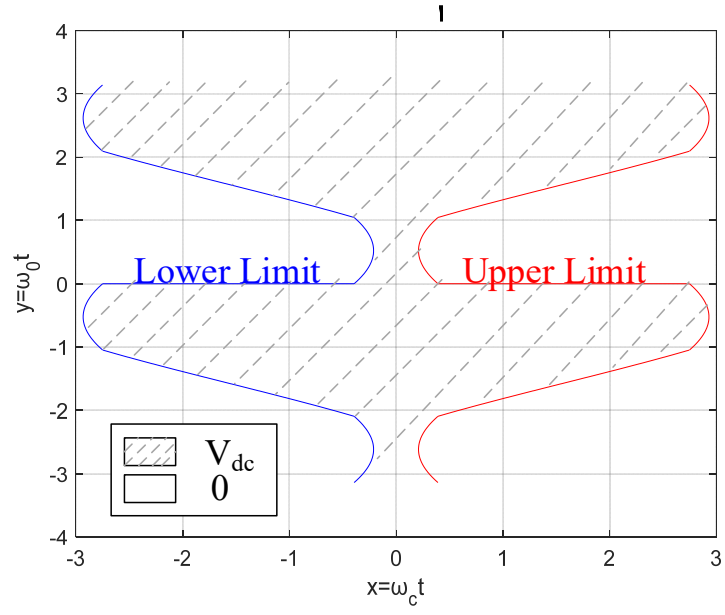


Figure 4.7: DFI integral bounds AZSPWM.

The calculation and simulation are based on a 50 Hz fundamental frequency, 10 kHz switching frequency, 150 V DC bus voltage, and 0.8 modulation index. As Figure 4.8(a) shows, the calculated carrier harmonics and the sideband component of both phase voltage and CMV are very close to the simulated result. Note that for computation, only the $f_s \pm 15f_0$ sideband harmonics around switching frequency are plotted. Figure 4.8(b) shows the zoomed-in view of the range around the switching frequency (10 kHz). It can be observed that AZSPWM almost eliminates the CMV component at the switching frequency, but inevitably causes the sideband components to increase.

4.1.3 CM Energy Distribution

The CMV spectrum gives a visual impression of how the CM voltage is distributed. However, in reality, the CM energy distribution, especially the CM energy (CME) in a certain frequency range, rather than the CME at a specific frequency point is more important. To analyze CME, the square sum of each component within a certain frequency range is calculated as below.

$$f(x,y) = \sum_{f=f_c - nf_0}^{f_c + nf_0} (V_{CM}(f))^2 \quad (4.7)$$

where n is the integer that defines the frequency range around f_c . Z_{CM} is the impedance of the CM path.

With Eqns (4.4) ~ (4.7), the CME distribution could be plotted in Figure 4.9. AZSPWM reduces CME drastically at all operational ranges. However, at a low MI near f_s , DPWM1 and DPWMMin are not necessarily worse than AZSPWM. As the MI goes lower, the CM performance of DPWMMin and AZSPWM becomes comparable around f_s .

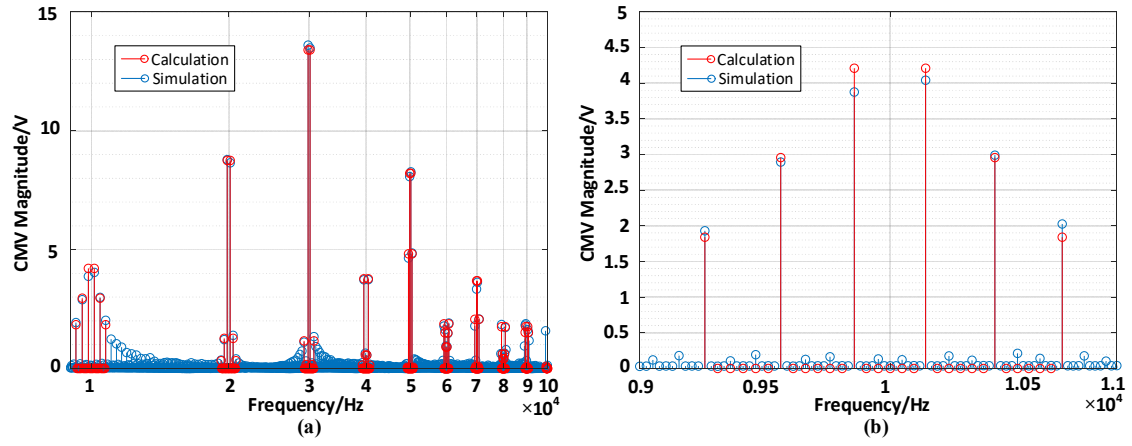


Figure 4.8: Comparison of DFI result and simulation.

(a) Wide frequency range, (b) Zoomed-in @ f_s .

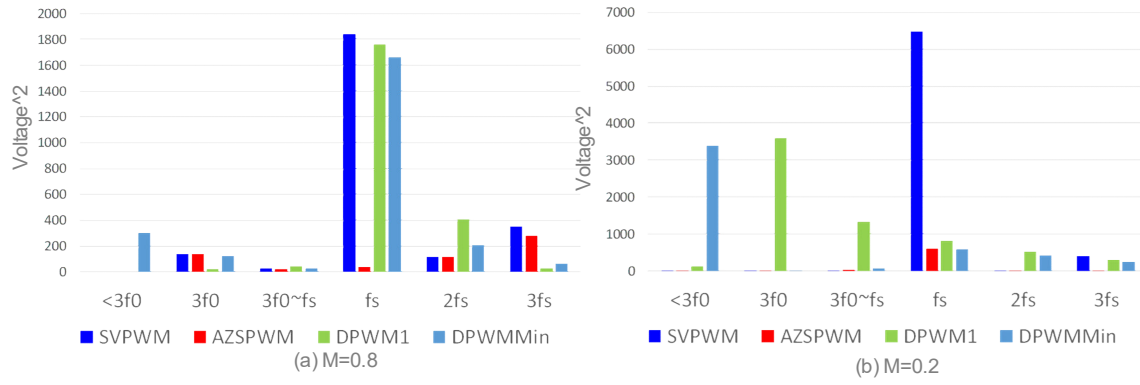


Figure 4.9: CM energy distribution.

(a) $MI=0.8$, (b) $MI=0.2$.

Considering the very-low-frequency CMV has little impact on the motor CMC, in terms of the CME:

(1) High MI : $SVPWM > DPWM1 > DPWMMin > AZSPWM$.

(2) Low MI : $SVPWM > DPWM1 \approx DPWMMin \approx AZSPWM$.

A general procedure of DFI analysis for CMV can be summarized as shown in Figure 4.10.

4.2 DM Current Ripple Prediction

As an important factor to evaluate the output power quality of inverters, the phase current ripple needs to be modeled. For three-phase inverter control, lots of modulation methods are proposed for different purposes, such as higher linearity range, or lower common-mode voltage. Some of the modulation schemes will sacrifice the differential-mode performance of the inverter due to a larger induced current ripple, as a result, the output current THD increases. High levels of THD can result in malfunctions of equipment, overheating on cables and transformers, or corruption on digital signals and communications.

The simulated three-phase current of the inverter for the low (0.2) and high (0.8) modulation index is shown in Figure 4.11. Here, $f_0=50$ Hz, $f_s=10$ kHz, and the DC bus voltage is 150 V.

The corresponding current THD is listed in Table. 4.1, which indicates AZSPWM always has the highest DMI THD, though it has the best CMV reduction, especially for a low modulation index. As modulation increases, THD for AZSPWM goes down.

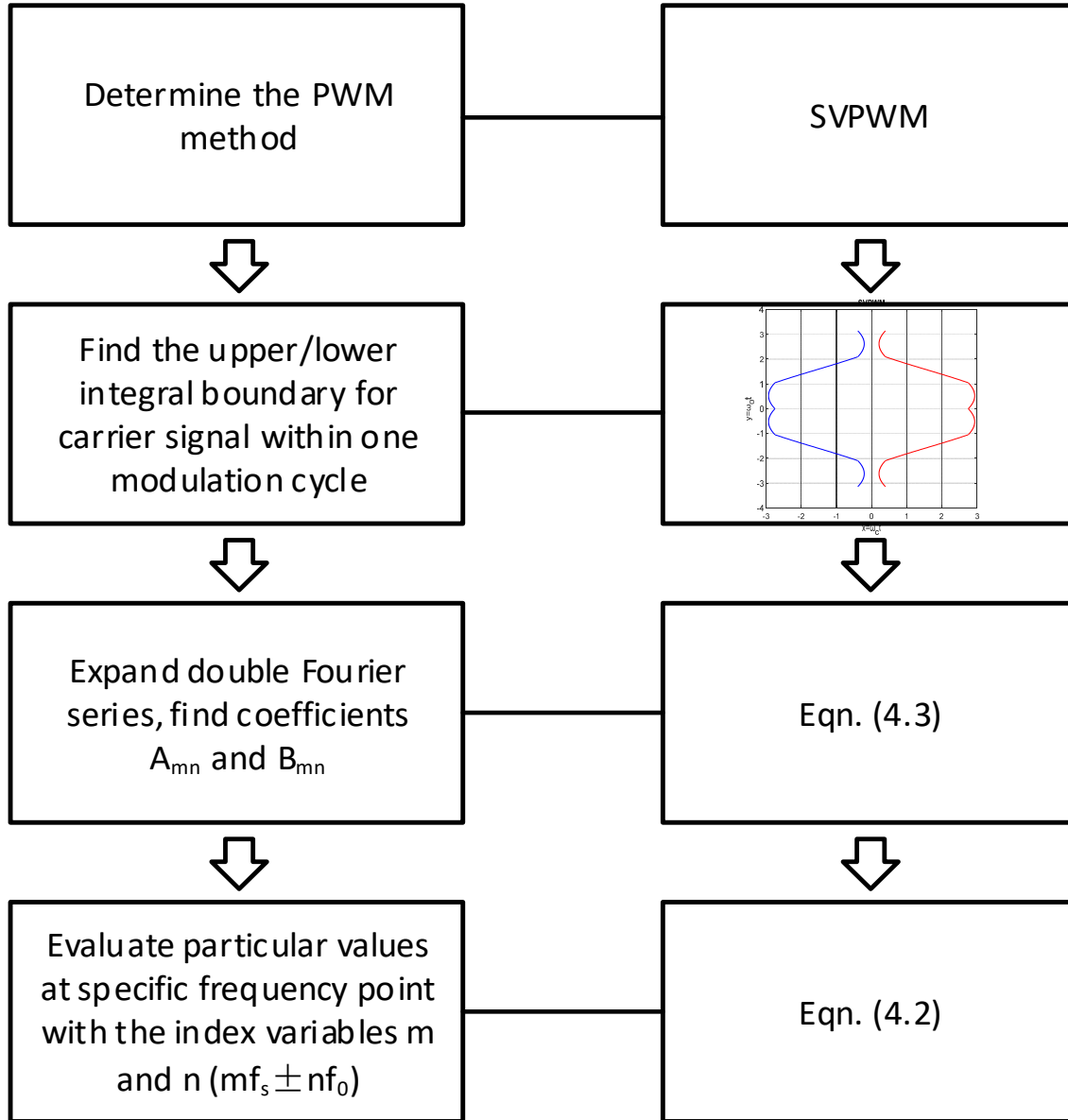


Figure 4.10: General procedure of DFI analysis for CMV.

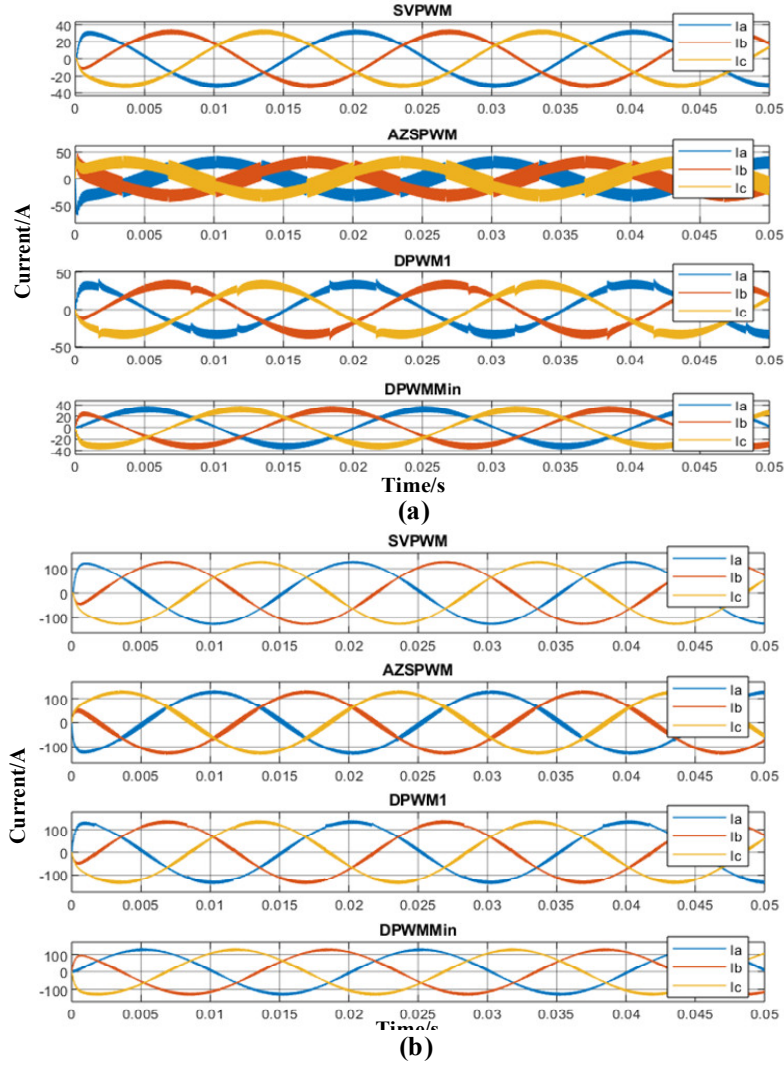


Figure 4.11: Three-phase current waveform.

(a) @MI=0.2, (b) @MI=0.8.

Table 4.1: Three-phase current THD

MODULATION INDEX	SVPWM	AZSPWM	DPWM1	DPWMMIN
0.2	5.49%	37.46%	11.27%	10.62%
0.8	2.95%	5.84%	3.96%	4.02%

Therefore, the analytical model of the phase-current ripple is also needed. Since AZSPWM inversely aligns the pulse with the medium-length duty cycle, it results in a higher voltage drop across the winding inductance, which yields higher di/dt at the zero-crossing section. To analytically investigate the current ripple induced by different PWM schemes, the current ripple prediction is needed. In this section, an analytical model of phase current ripple will be proposed to evaluate the ripple under different modulation methods.

To predict the phase current ripple, the equivalent circuit under each space vector is needed. Figure 4.12 shows the Thevenin equivalent circuit with a total of eight switch combinations. The ripple is essentially the di/dt introduced by the voltage drop across the winding inductance (motor load is used here as an example). The current changing slope can then be derived through KVL and KCL.

Table. 4.2 lists the current slope under different space vectors [128, 129], in which D_a represents phase A's duty cycle, D_b represents phase B's duty cycle, and D_c represents phase C's duty cycle, respectively.

To show the detailed current ripple prediction process, conventional space vector modulation (CSVM), also known as space vector pulse width modulation (SVPWM), is used as an example. The pulse pattern of CSVM is shown in Figure 4.1(a), the used space vector sequence is 000-100-110-111-110-100-000. In different subintervals, the voltage across the winding inductance of phase A (V_{ao}) is different. As a result, the current will change linearly in each segment according to different slopes and operation times. For instance, in the scenario shown in Figure 4.1(a), the current ripple could be calculated with (4.9).

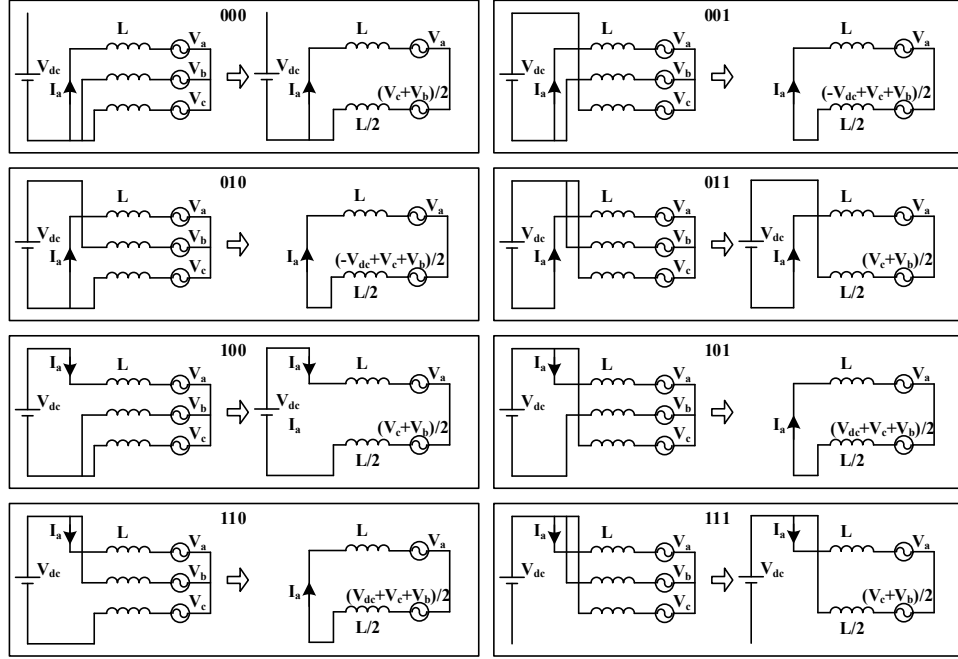


Figure 4.12: Equivalent circuit for current ripple prediction under different space vectors.

Table 4.2: Current slope under different space vectors.

Space Vector	Current Slope
000/111	$\frac{V_{dc}}{3L} (D_b + D_c - 2D_a)$
100/011	$\frac{V_{dc}}{3L} (D_b + D_c - 2D_a - 2)$
110	$\frac{V_{dc}}{3L} (D_b + D_c - 2D_a + 2)$
001/010	$\frac{V_{dc}}{3L} (D_b + D_c - 2D_a - 1)$
101	$\frac{V_{dc}}{3L} (D_b + D_c - 2D_a + 1)$

To show the detailed current ripple prediction process, conventional space vector modulation (CSVM), also known as space vector pulse width modulation (SVPWM), is used as an example. The pulse pattern of CSVM is shown in Figure 4.1(a), the used space vector sequence is 000-100-110-111-110-100-000. In different subintervals, the voltage across the winding inductance of phase A (V_{ao}) is different. As a result, the current will change linearly in each segment according to different slopes and operation times. For instance, in the scenario shown in Figure 4.1(a), the current ripple could be calculated with (4.9).

$$\Delta I = Slope_{111} \cdot Time = \frac{V_{dc}}{2} (D_b + D_c - 2D_a - 2) D_c T_s \quad (4.9)$$

With the current ripple prediction method, the reason why AZSPWM has a larger current ripple can be explained. According to the simulation result in Figure 4.11, the largest ripple current for AZSPWM happens at each zero-crossing part, which is located in Sector 2 and 5. The segments with a negative slope are 010 and 011, according to Table 4.2. The predicted current ripple is:

$$\Delta I = \frac{V_{dc}}{3L} (D_b + D_c - 2D_a - 2) D_c T_s + 2 \frac{V_{dc}}{3L} (D_b + D_c - 2D_a - 1) \left(\frac{1 - D_a - D_c}{2} \right) T_s \quad (4.10)$$

Figure 4.13 shows the current ripple prediction in Sector-1. The actual ripple current is determined by the DC-link voltage, motor armature inductance, switching frequency, and instantaneous duty cycle. On the right-hand side of Figure 4.13, the simulated ripple behavior is aligned with the prediction.

Assume the switching frequency is 10 kHz, the fundamental frequency is 120 Hz, and the armature inductance is 120 μ H. According to Eqn (9), the maximum ripple of any

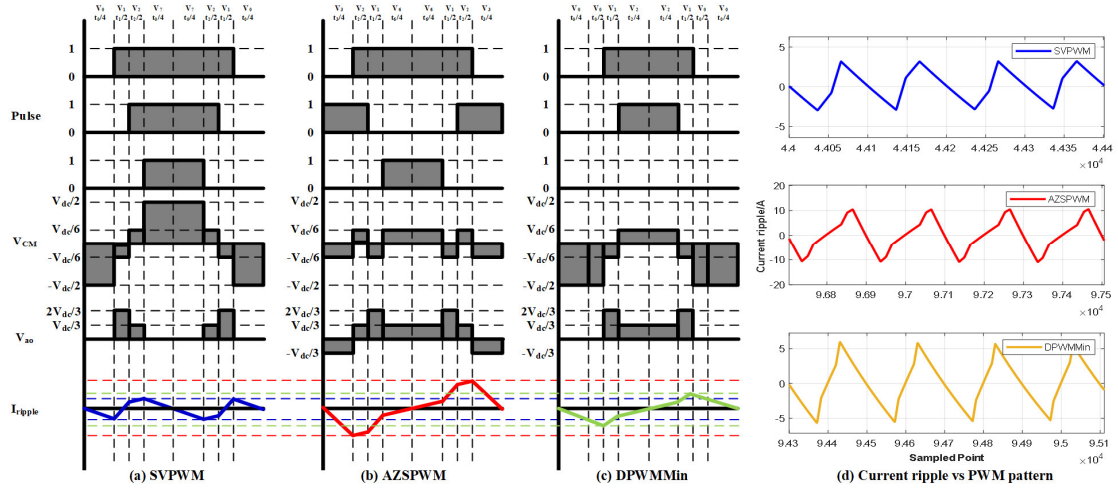


Figure 4.13: DM current ripple at various PWMs.

(a) SVPWM, (b) AZSPWM, (c) DPWMMin, (d) Current ripple vs PWM pattern.

PWM scheme can be calculated with respect to different modulation indices. Figure 4.14 shows the predicted current ripple amplitude as the modulation index varies from 0.1 to 0.7 for SVPWM, AZSPWM, and DPWMMin, respectively. With the modulation index increasing, the current ripple of AZSPWM decreases, while for SVPWM and DPWMMin the current ripple increases. However, even the smallest current ripple of AZSPWM is still greater than the highest value when applying SVPWM or DPWMMin. This turns out to be one significant drawback of AZSPWM.

By doing the same current prediction in all sectors for different PWM schemes, the current ripple behavior can be compared to a different modulation index. The prediction result is shown in Figure 4.15. It is observed that, as the modulation index increases, the current ripple of SVPWM and DPWMMin will also increase while dropping for AZSPWM. Furthermore, at the same modulation index, AZSPWM always generates the highest current ripple, followed by DPWMMin, and SVPWM shows the lowest current ripple.

4.3 Comprehensive Comparison

Figure 4.16 shows a direct comparison of the CM- and DM-performance of SVPWM, AZSPWM, and DPWMMin. It can be found that in the low MI range, the current THD of AZSPWM is significantly higher than SVPWM and DPWMMin. In the medium and high MI zone, the corresponding CME of AZSPWM is significantly lower than other PWMs, though its DM current THD is still worse than others.

Since different modulation schemes have different performances in both CM and DM aspects. Using the modulation schemes at the specific operating point could maximize the advantages while avoiding the drawbacks. For example, taking motor current ripple,

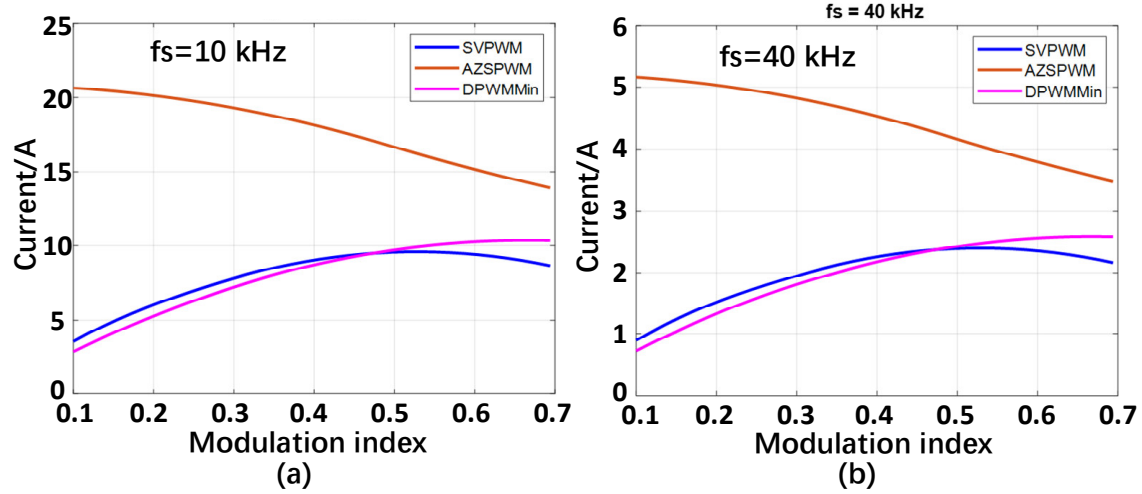


Figure 4.14: Current ripple vs. modulation index.

(a) $f_s = 10$ kHz, (b) $f_s = 40$ kHz.

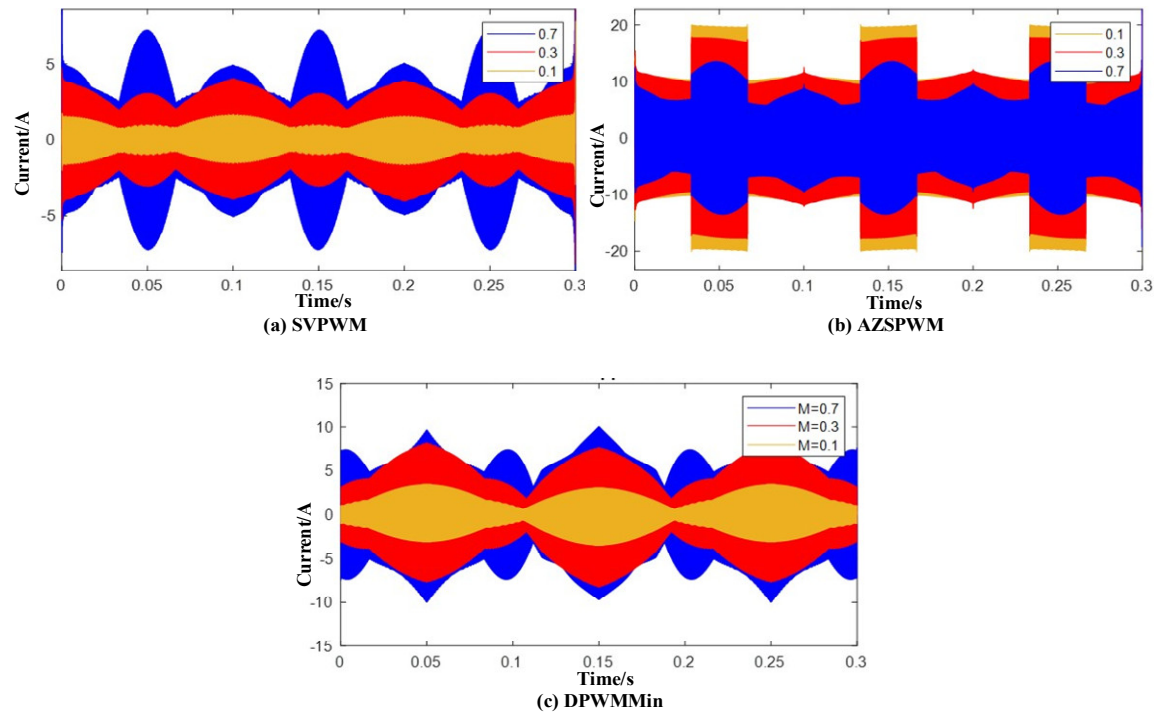


Figure 4.15: Current ripple prediction.

(a) SVPWM, (b) AZSPWM, (c) DPWMMin.

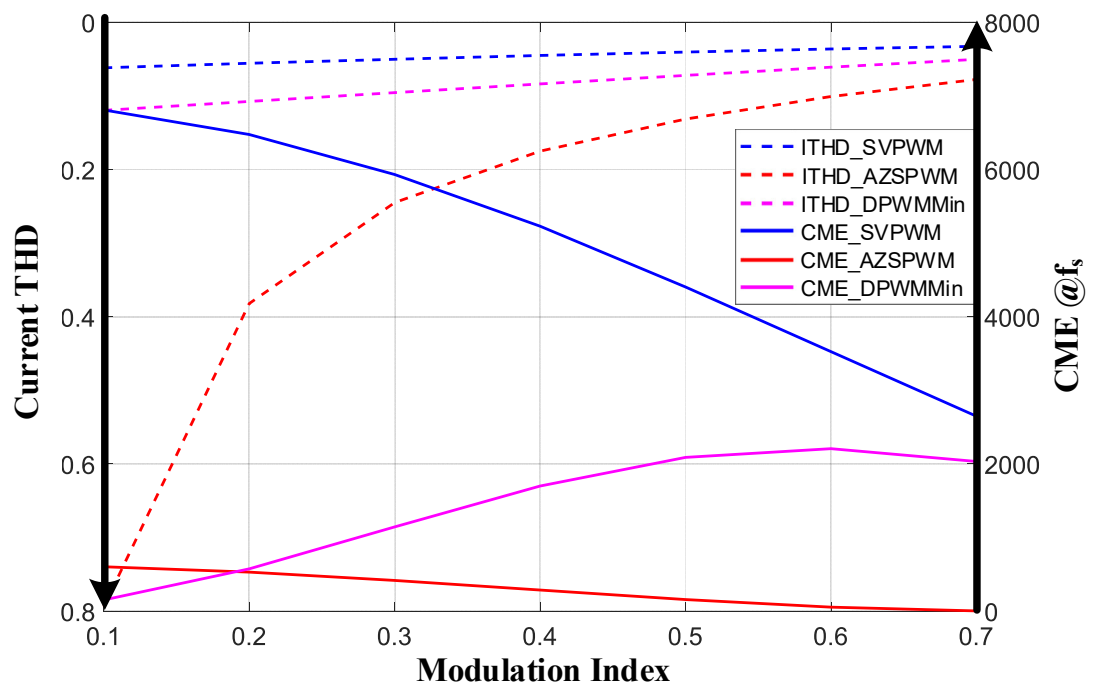


Figure 4.16: CM- & DM-performance comparison for various PWM methods.

CM current, loss, and switching frequency to build a multifactor control method could realize an online adaptive operation. Such a modulation method combination can be named hybrid PWM (HPWM).

As for the DM performance, the concerning part is the output current ripple. according to the proposed current prediction model, the current ripple of three PWMs is plotted in Figure 4.17. It shows that with different MI and switching frequencies, the general relationship is that AZSPWM has the highest current ripple, DPWMMin ranks the second, and CSVM shows the lowest ripple. The ripple of all PWMs reduces as the switching frequency increases. For CSVM and DPWMMin, the ripple increases as the MI increases, while AZSPWM shows the opposite trend. The current ripple of each PWM merges at full modulation. As for the CM performance. A 3D plot is shown in Figure 4.18. It shows the peak CMC vs the f_s and MI . Obviously, in different zones, the CM reduction performance is different. For example, at a certain range that is marked in the circle, the red color shows on the tops, which means the AZSPWM has the highest CMC while the DPWM shows the best reduction performance. These mention us that if some proper combinations of these PWMs could be found, the inverter could always pick one with the ideal CM performance among others at specific operating conditions.

As the CM and DM performance prediction model for different PWM are built. If a modulation scheme could take motor current ripple, CMC, loss, and switching frequency to build a multifactor control method could realize an online adaptive operation, the controller could online determine the optimal PWM according to the CM/DM performance and system loss, as well as the switching frequency with a minimum requirement of computation resources based on the torque and speed command.

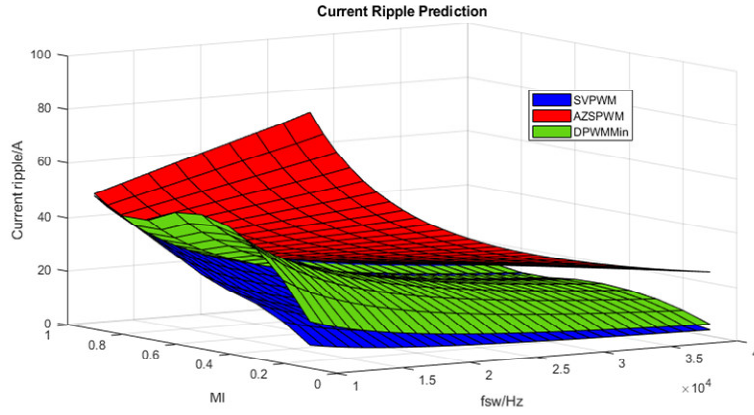


Figure 4.17: Current ripple prediction comparison.

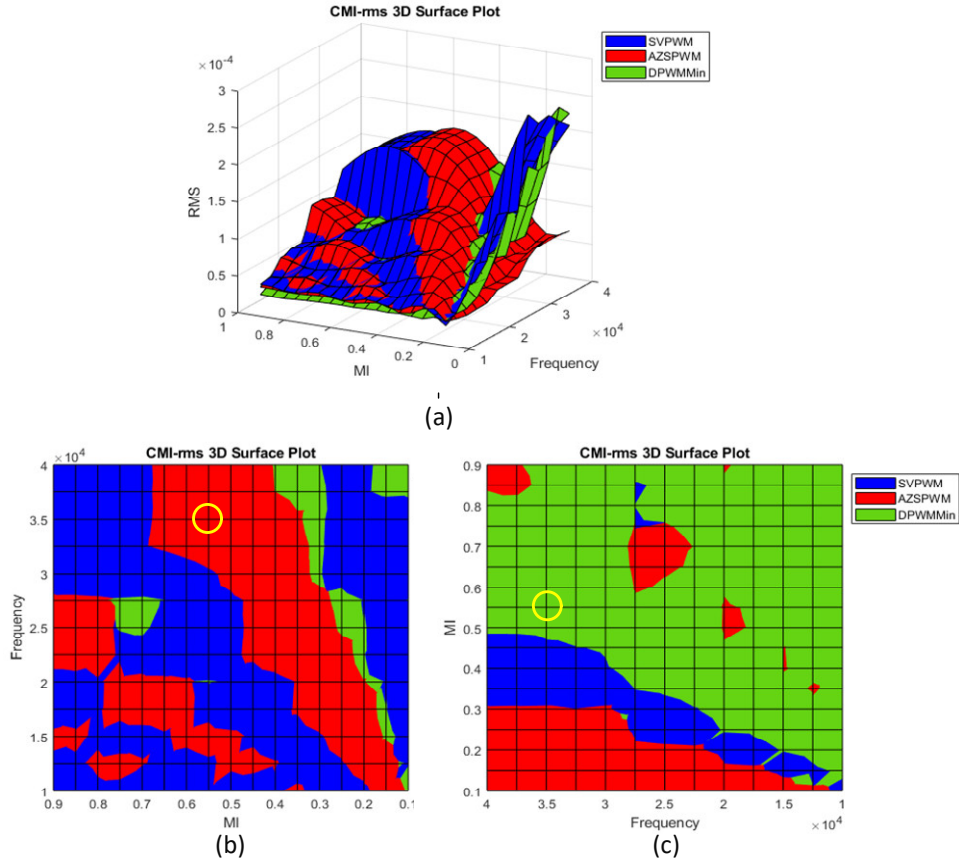


Figure 4.18: Peak CMC prediction.

(a) 3D view, (b) Top view, (c) Bottom view.

HPWM intends to use different modulation schemes based on the specific scenario. To simplify the structure, as shown in Figure 4.19, the PMSM close-loop control is still FOC-based. However, in the PWM modulator, the controller will need to evaluate the system parameters and determine which PWM shows the best CM and DM performance. This process is the core computation part of the HPWM algorithm. The HPWM flow chart is shown in Figure 4.20. The basic idea is, to loop the switching frequency in a certain user-defined range and find the frequency range with the lowest CMC and output current ripple. Pick the frequency with minimum loss as the present operation frequency. To combine the CM/DM performance evaluation, there exist several challenges, especially a large amount of computation time is need for DFI. Explore some machine learning methods to actively evaluate the CM performance could make the on-chip analysis of different PWMs possible.

4.4 Experimental Validation

An FPGA-controlled SiC inverter is designed to set up a motor drive test bench. As shown in Figure 4.21(a). The designed inverter is air-cooled and rated at 30 kW. The SiC device is from CREE (C2M0025120D) and rated at 1200 V 90 A. The CMC measurement relies on the line impedance stabilization network (LISN). The test bench layout is shown in Figure 4.21(b). LISN provides a stable and normalized source impedance ($50\ \Omega$) for CM measurement and prevents external noise from the source side. The measured CMC is sent to the EMI analyzer through the power combiner, which allows the CM component to pass while suppressing the DM component. The FPGA controller communicates with the host computer through Ethernet. The whole system sits on a copper grounding plate, where the inverter heatsink, motor case, and LISN are grounded.

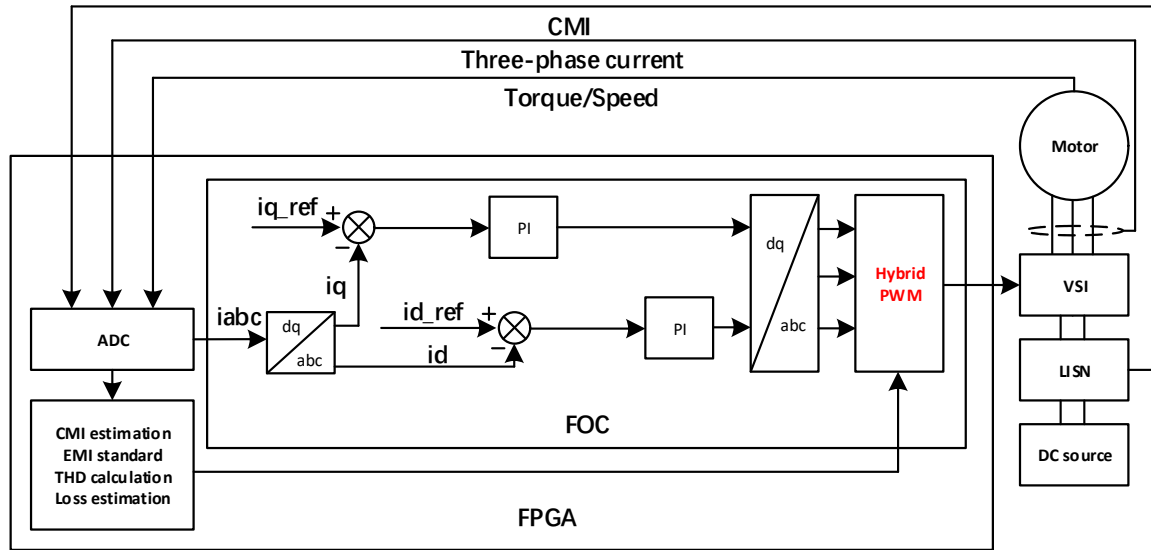


Figure 4.19: Field-oriented control with HPWM.

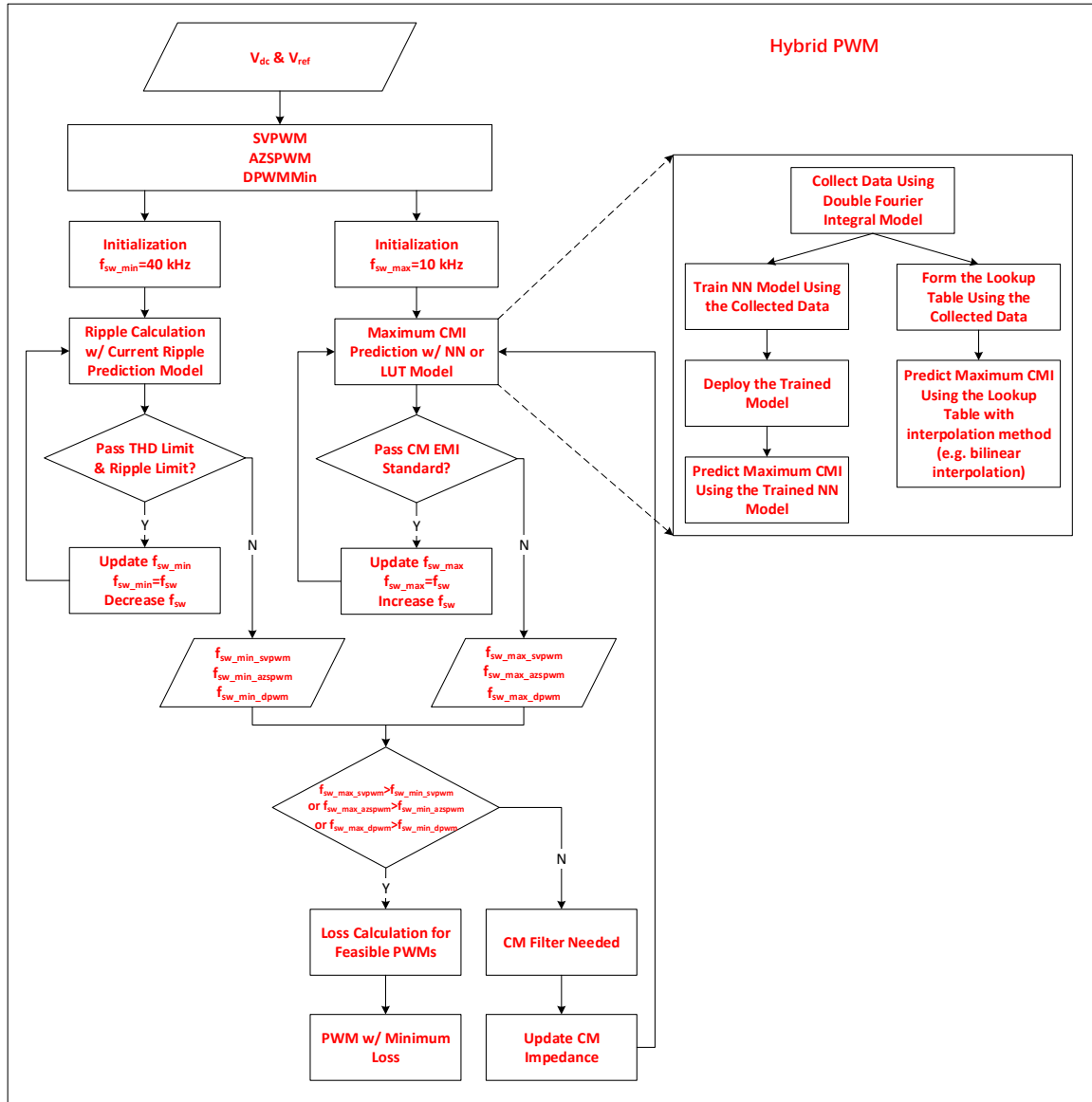
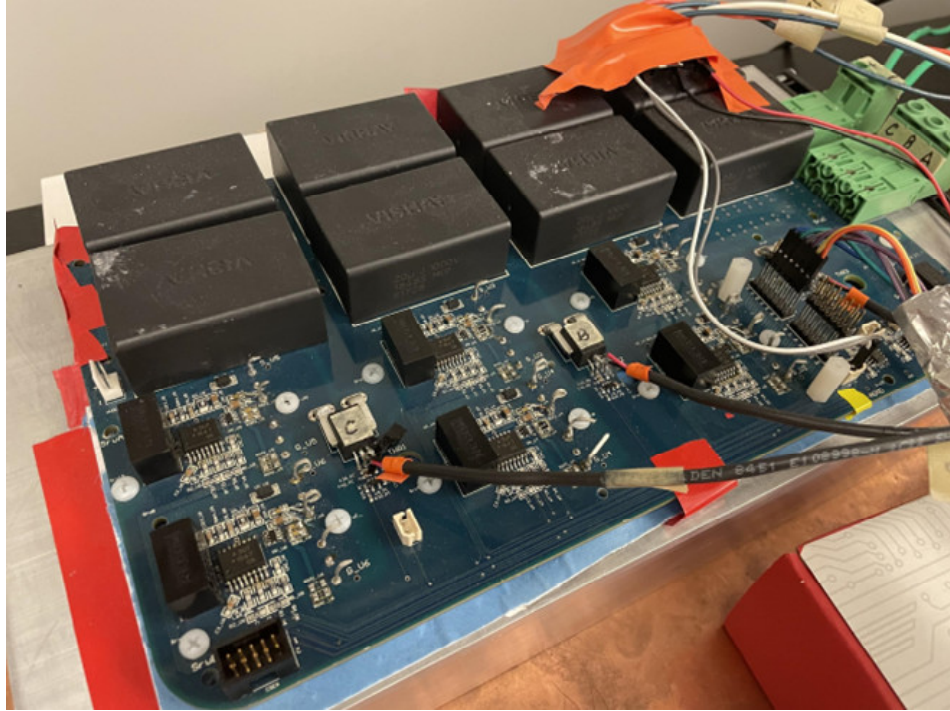
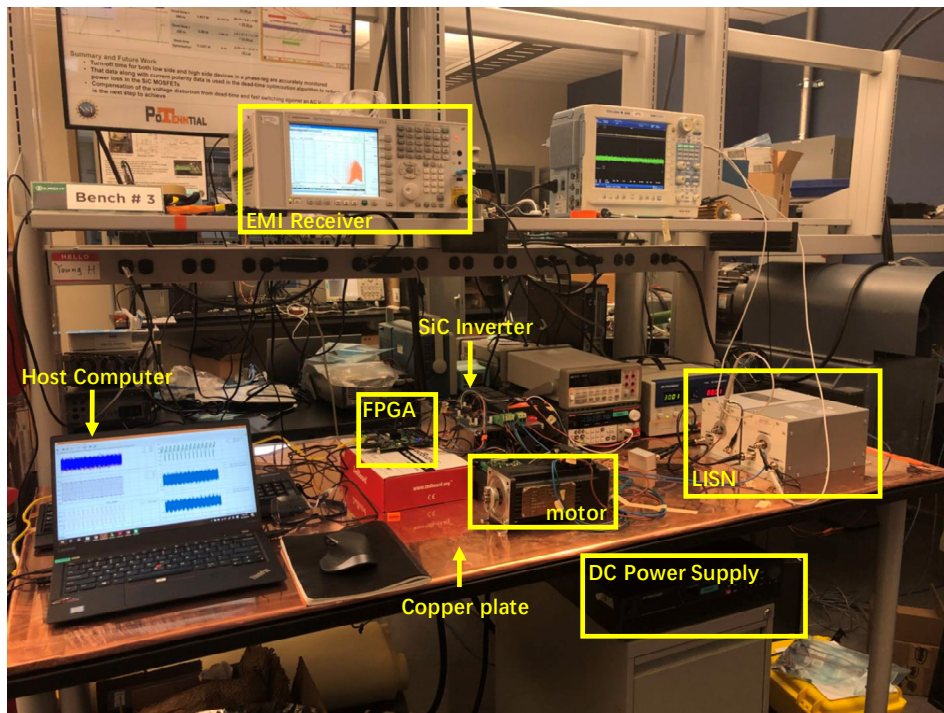


Figure 4.20: HPWM flow chart.



(a)



(b)

Figure 4.21: Test bench setup.

(a) 30 kW SiC inverter, (b) Test bench layout.

By switching different PWM schemes at low speed (300 RPM), which is the low- MI (0.2) case, the CMV measurement is collected and plotted, as shown in Figure 4.22(a). The zoomed-in view at the switching frequency is shown in Figure 4.22(b).

As evident in Figure 4.23 at the switching frequency, SVPWM has the highest CM component by translating the CMV decibel plot to the CMC amplitude spectrum; DPWM1 and DPWMMin have lower CM components, and AZPWM has the lowest CM current—even though its CM component on the sideband rises compared to other PWM schemes. This observed behavior at the switching frequency is aligned with the simulation result.

Note that the modulation index in this test is very low (0.2). At f_s , AZSPWM has the best CMV reduction performance. However, in terms of the spectrum near f_s ($f_s \pm 500$ Hz) of AZSPWM and DPWMMin, the CMV reduction performance is comparable, the lowest among all PWM schemes. DPWM1 is in the middle, and SVPWM has the highest CMV. This also confirms that at a low modulation index, the CM reduction performance of AZSPWM and DPWMMin are close, as predicted in Figure 4.9.

The CMC for each PWM method at different switching frequencies is also measured, as shown in Figure 4.24. At a specific switching frequency, the peak value of CM components increases with the switching frequency. Figure 4.25 shows the CMC increase as switch frequency increases. This leads to a bulky design of the CM filter as the switching frequency increases, which is the main challenge when adopting WBG devices.

With the same test bench, three different PWM patterns mentioned in this chapter are generated by the Zedboard to drive the motor. The EMI receiver is used to measure the CMC and generate the spectrum. The spectrum is focused on the range from 150 kHz to 300 kHz (LW band in CISPR-25), and the predicted peak CMC is also within this region.

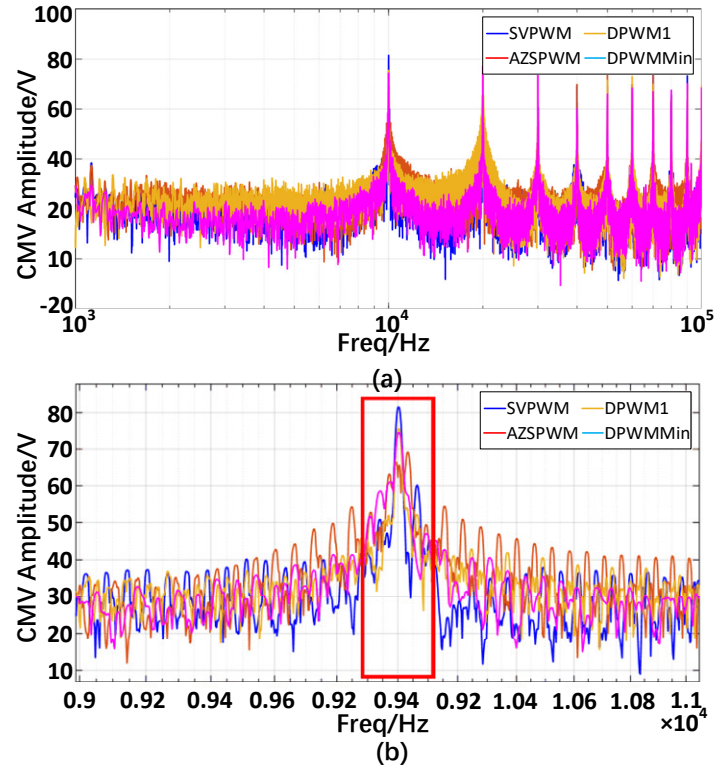


Figure 4.22: CMV measurement.

(a) Wide frequency range, (b) Zoomed-in view @ f_s .

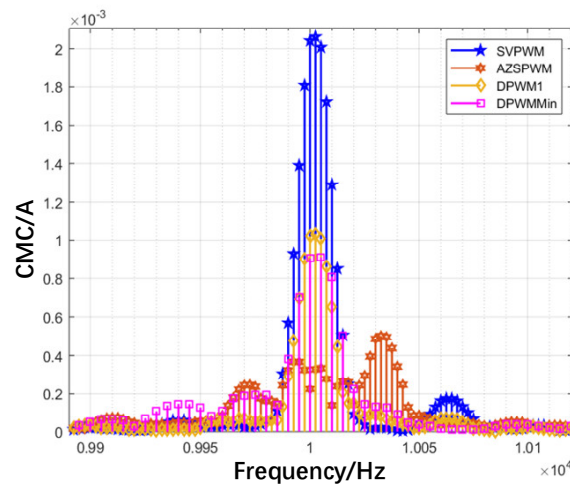


Figure 4.23: CM current spectrum @ f_s .

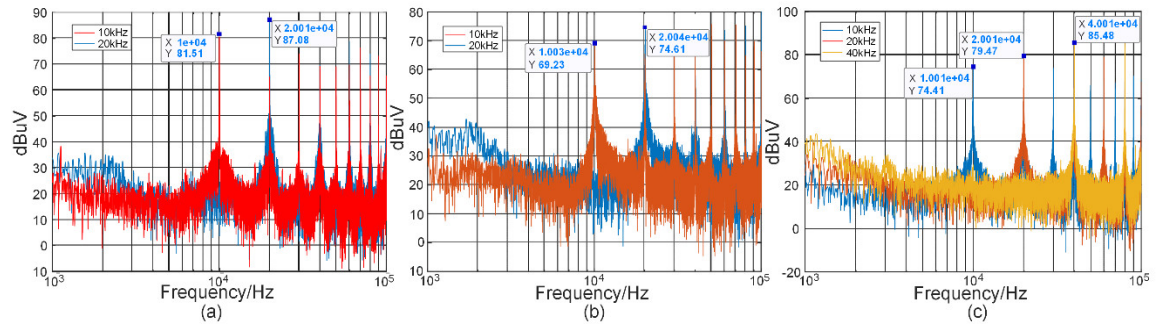


Figure 4.24: CMV spectrum with respect to different switching frequency.

(a) SVPWM, (b) AZSPWM, (c) DPWMMin.

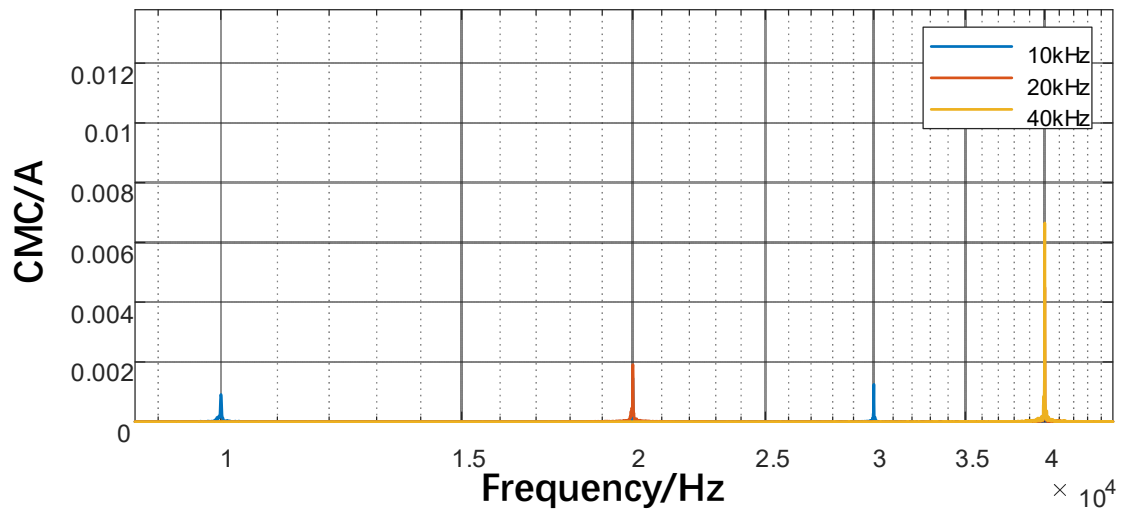


Figure 4.25: CM current spectrum with respect to different switching frequency

@DPWMMin.

Figure 4.26 shows the measurement results at 10 kHz switching frequency and 0.31 MI . Within the frequency range from 150 kHz to 300 kHz, the maximum common mode currents are labeled in the figures. The maximum common mode currents with SVM, AZSPWM, and DPWMMin are 3.32583 mA, 2.66876 mA, and 1.36647 mA, respectively. The predicted peak CMC is compared with the measurement results in Table 4.3, where the absolute error percentages are around 10%.

4.5 Impact of Control Bandwidth

As a trend in the EV domain, the adoption of higher-resolution microcontrollers, such as FPGAs become popular. With their unique parallel computation capability, FPGAs can update the duty cycle every switching period [130], yielding a sampling or control frequency (f_c) equal to the switching frequency (f_s). This finely tunes the PWM patterns resulting in lower current THD. However, little research work has been performed on its effect on CMV reduction. Some extended studies will be presented in this section.

As the switching frequency of WBG devices is gradually pushed to a higher level to maximize the potential of SiC devices, the high control frequency, i.e., high control bandwidth (CBW) becomes more and more important. In this paper, all the control logic is realized through Xilinx System Generator blocks and fixed-point arithmetic with high precision (32-bit) multiplications. The HDL code can be automatically generated as soon as the simulation in MATLAB/Simulink environment is verified. Then the generated HDL bitstream can be directly implemented into the Xilinx 7000-series FPGA chip to achieve field-oriented control (FOC), with the control diagram shown in Figure 4.27. Note the traditional microprocessor executes the control algorithm in serial sequence, which limits

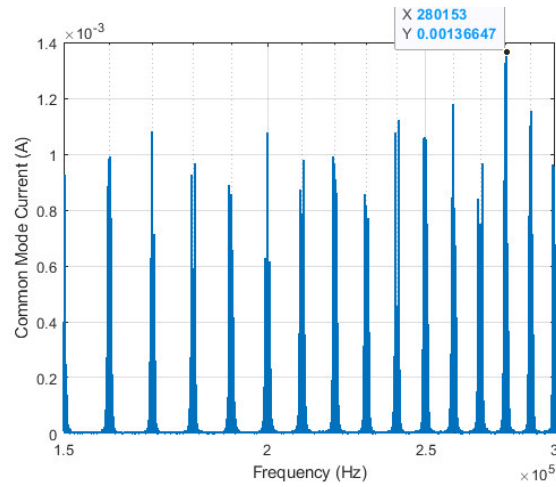
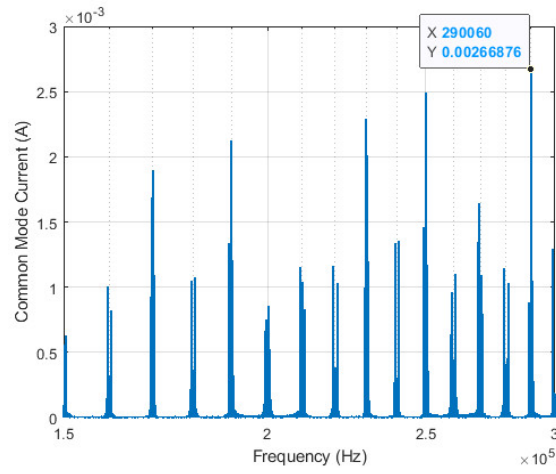
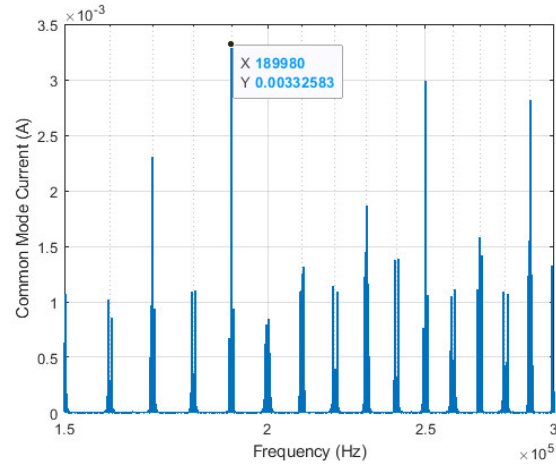


Figure 4.26: Surface plot of peak CMC with different f_s and MI .

Top: CSVM, Middle: AZSPWM, Bottom: DPWMMin.

Table 4.3: Predicted peak CMC vs Measured Result

PWM	Measurement (A)	Prediction (A)	Error (%)
CSVM	0.00332583	0.00346765	4.2641
AZSPWM	0.00266876	0.00244687	8.3145
DPWMMin	0.00136647	0.00125049	8.4876

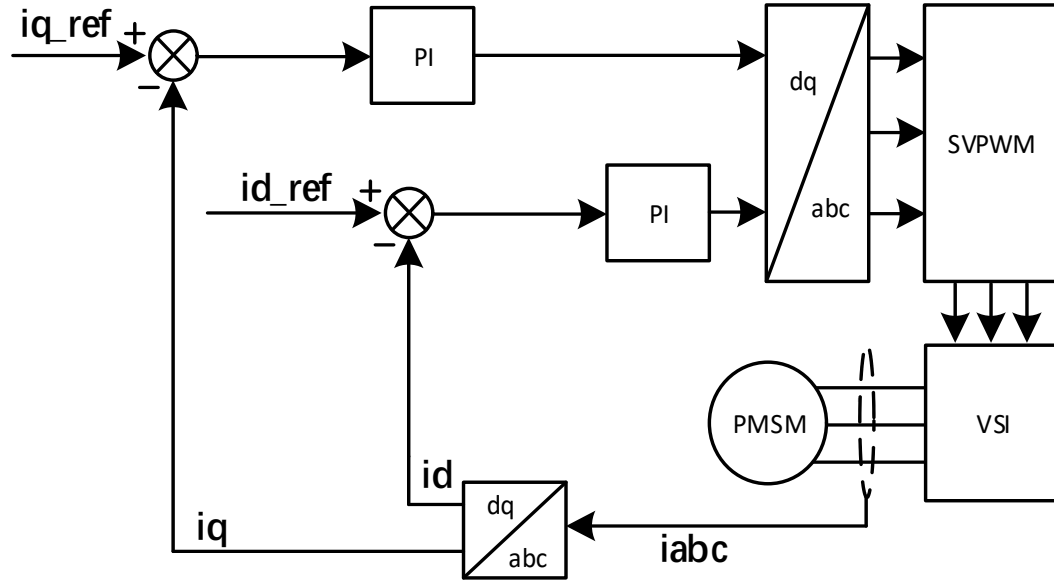


Figure 4.27: Field-oriented control block diagram.

the overall system processing efficiency and yields a low control frequency, i.e., $f_c \ll f_s$. In FPGAs, all the control logic is implemented in parallel, which means it can update the PWM every clock cycle, i.e., $f_c = f_s$. The control bandwidth impact on CM and DM performance has rarely been mentioned in the previous research work, which is the subject of this section.

4.5.1 CBW Impact on CM Signal

Assume in a SiC inverter, $f_s = 40$ kHz and $f_0 = 50$ Hz. To investigate the impact of f_c , the author purposely set $f_c = 1/8f_s$, $1/4f_s$, and $1/2f_s$, which means to update the PWM duty cycle every 2, 4, and 8 switching periods, respectively.

Figure 4.28 gives the CMV FFT result when $f_c = 40$ kHz, $f_c = 1/8f_s = 5$ kHz. A zoomed-in view shows that for $f < f_s$, the CMV with low f_c is always higher than the curve with full control bandwidth, except at some notched frequency points ($n \cdot f_c$). However, overall, there is no significant CME difference.

By calculating the CME distribution, as shown in Figure 4.29, the conclusion is:

- (1) f_c will affect CM current distribution in the frequency range $< f_s$, but the impact is minor.
- (2) CM current at the switching frequency point is still the dominant component, regardless of f_c .

Therefore, f_c does not contribute to the CM reduction. This conclusion is confirmed by measurements in Figure 4.30. In these measurements, the CM component is at $f = n \cdot f_c$ notches in the low-frequency range matching well with simulation results. The dominant part is still at $f = f_s$.

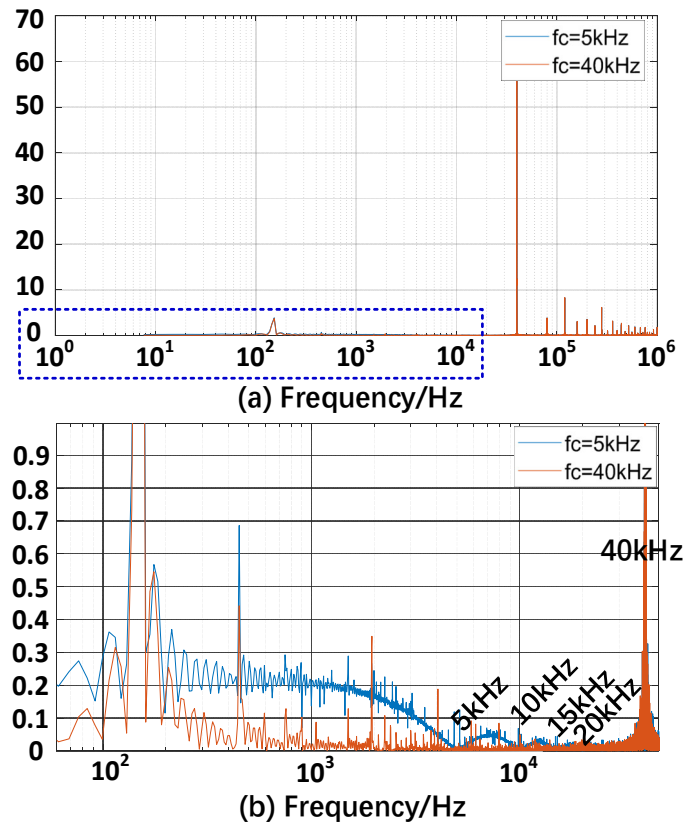


Figure 4.28: CM spectrum @ $f_s=40\text{ kHz}$ with respect to different CBW.

(a) Wide range ($f_c=1/8f_s$, simulation) (b) Zoomed-in view.

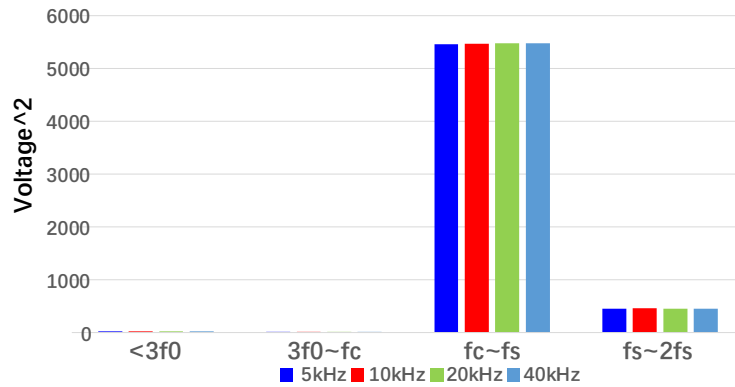


Figure 4.29: CME distribution with respect to different f_c (simulation).

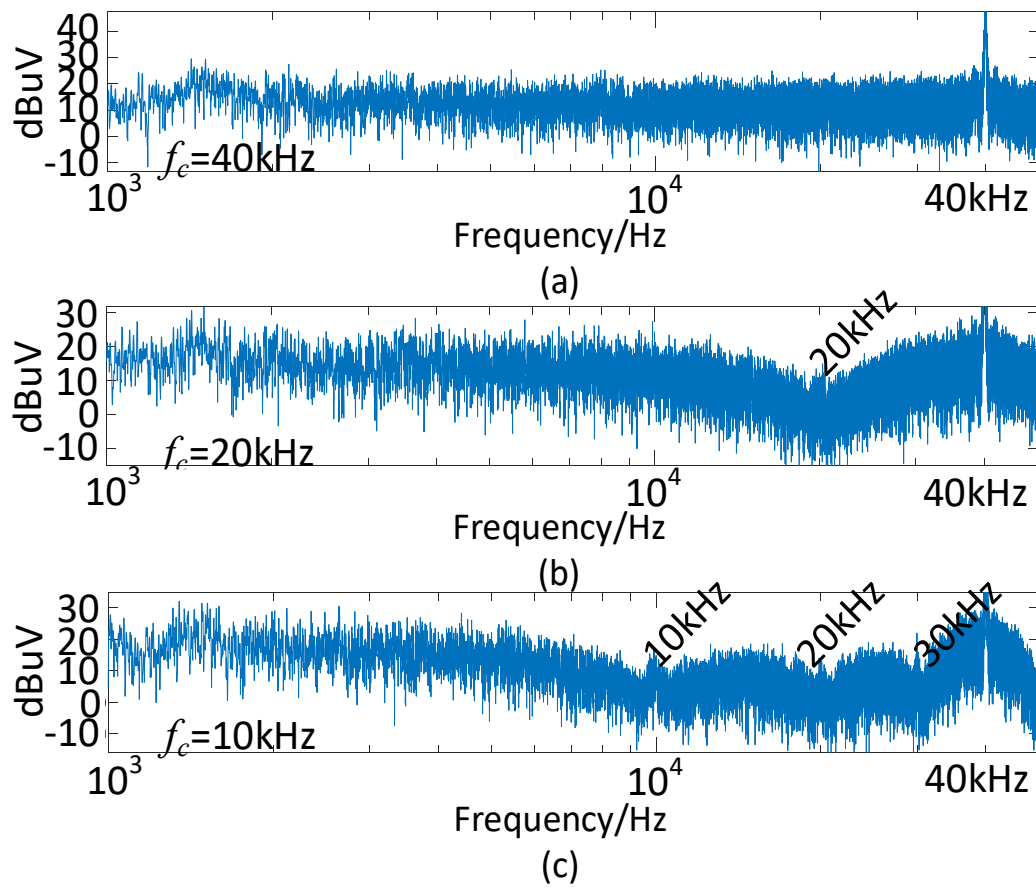


Figure 4.30: Measured CMV spectrum with respect to different CBW.

(a) 40 kHz, (b) 20 kHz, (c) 10 kHz.

4.5.2 CBW Impact on DM Signal

The PWM updating frequency will lower the resolution of the output waveform. For a 40 kHz inverter, set $f_c = 1/8f_s$, $1/4f_s$, $1/2f_s$ respectively. The spectrum of the DM current is compared in Figure 4.31. For each case, the DM components at $n*f_c$ will appear as long as $f_c \neq f_s$. For $f_c = f_s$ case, the simulated current THD is 1.775%. As f_c decreases, the current THD increases. Table 4.4 shows the THD simulation result with various f_c at $f_0 = 500$ Hz and 1 kHz, respectively.

The conclusion is:

- (1) The influence that f_c brings to the DM signal is more obvious. Since the modulation signal changes along f_c , the resolution drops as $f_c < f_s$, which affects the shape of the output current.
- (2) For $f_c \neq f_s$, the spectrum has high components not only at f_0 and f_s , but also at $n*f_c$.
- (3) The lower f_c , the higher DM current THD.
- (4) FPGA with a high control bandwidth will benefit DM more than CM.

To validate the impact of using FPGA, the CMC at different f_c is collected. The inverter switching frequency is 40 kHz. f_c is set to 40 kHz, 20 kHz, and 10 kHz, respectively.

The CMC spectrum is plotted in Figure 4.32(a). Figure 4.32(b) provides a zoomed-in view of the CMC spectrum at the switching frequency point (40 kHz). It shows that no matter what the control frequency is, the impact on the CMC is negligible, i.e., the control frequency does not affect the CM energy.

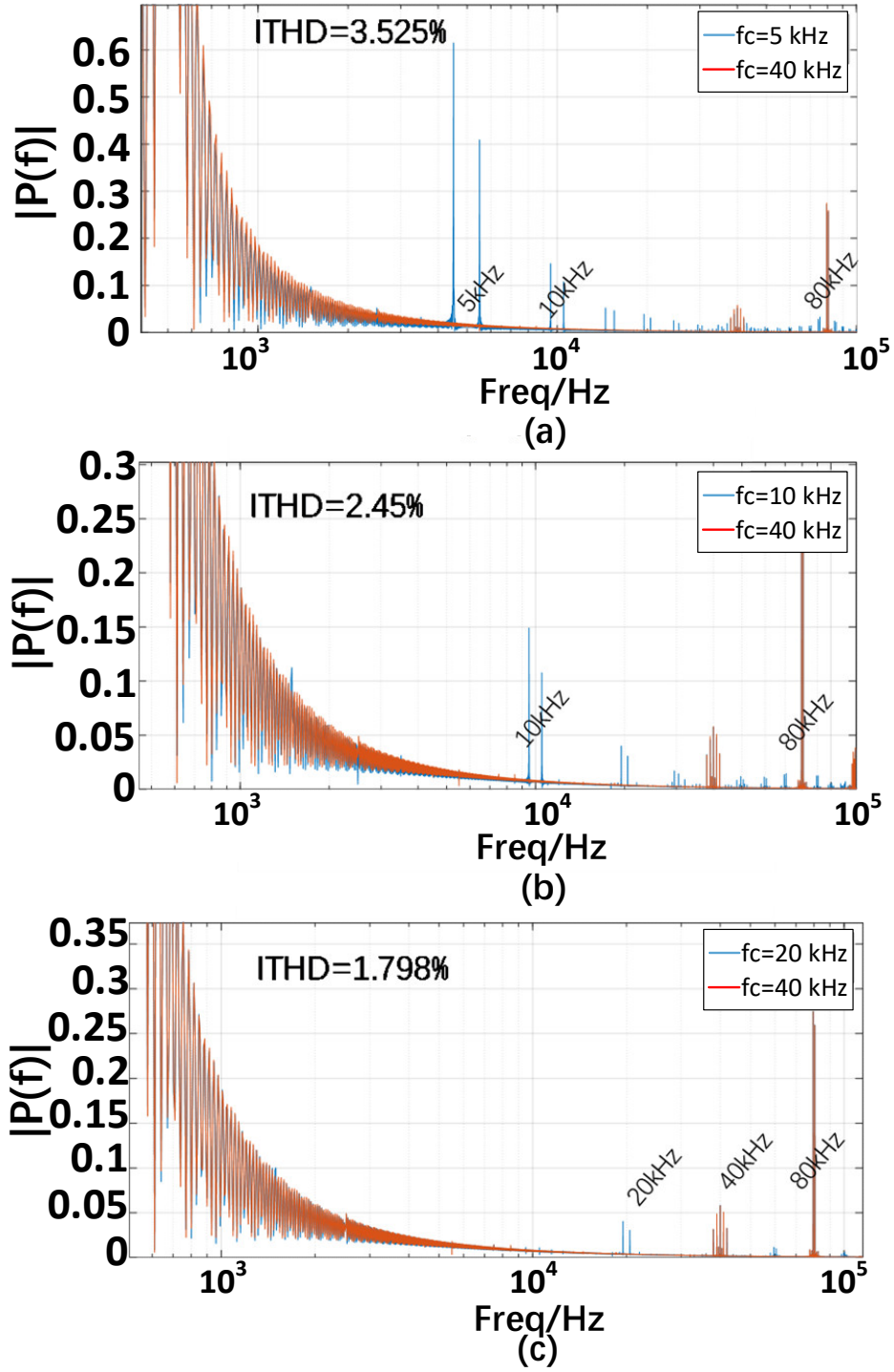


Figure 4.31: DM signal spectrum of the three-phase current (simulation) comparison with different control bandwidth.

(a) $f_c = 1/8 f_s$, (b) $f_c = 1/4 f_s$, (c) $f_c = 1/2 f_s$.

Table 4.4: Three-phase current THD with different f_c - f_0 pair

CBW (f_c)	5 kHz	10 kHz	20 kHz	40 kHz
THD ($f_0=500$ Hz)	3.525%	2.45%	1.798%	1.775%
THD ($f_0=1$ kHz)	9.175%	3.339%	3.026%	2.581%

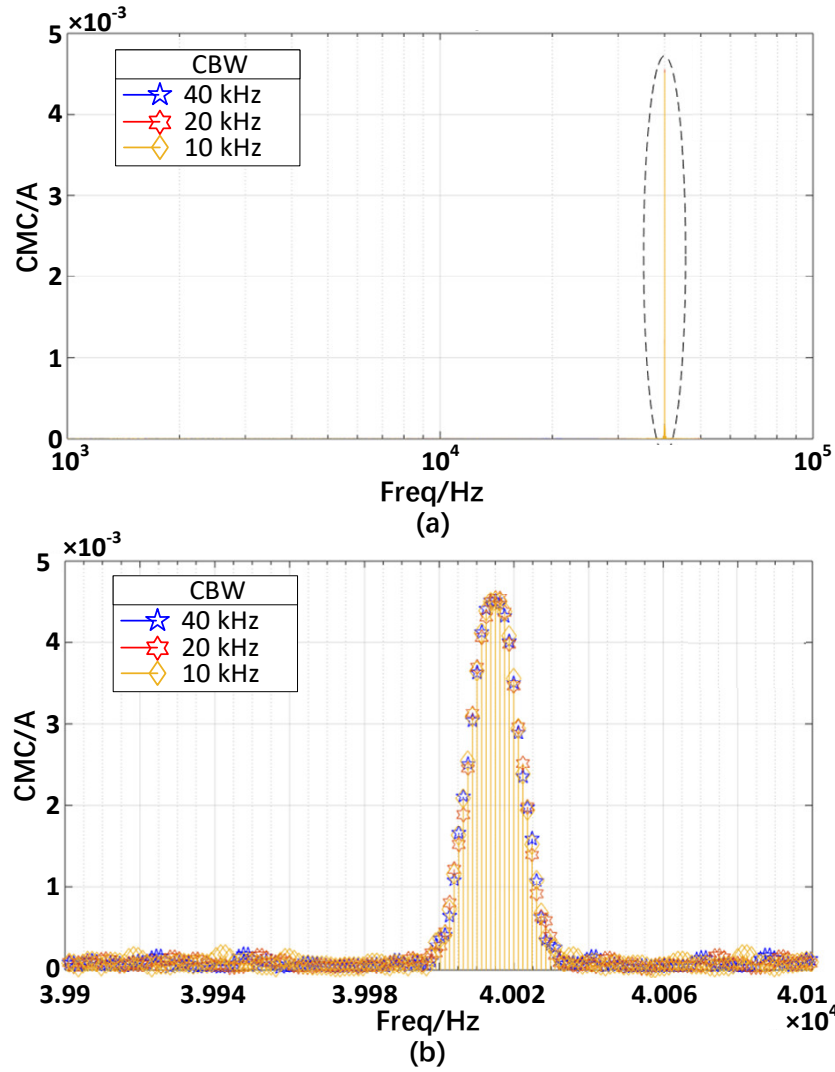


Figure 4.32: Measured CM current spectrum with different CBW.

(a) Wide frequency range, (b) Zoomed-in view @ f_s .

4.6 Summary

This chapter has given a comprehensive consideration of the three-phase motor drive system by building analytical models of CMV and DMI for various PWM control, which have been validated by simulation and experiments. The DFI model quantifies existing sideband harmonics in AZSPWM CMV and shows excellent extendibility to a multi-level inverter. Together with the DMI model predicting current ripple and THD, some conclusions have been drawn that are different from previous literature:

(3) Due to such sideband harmonics, the CM performance of AZSPWM is not necessarily better than DPWMs, especially at a low modulation index.

(4) AZSPWM causes a higher phase current ripple than other PWM.

How to apply the best PWM under different operation scenarios remains unknown, but such an analytical model provides us with a powerful tool, allowing a comprehensive vision for further evaluations. Compared to the traditional solution, e.g., the simulation model in Simulink, the proposed analytical model could help designers to summarize the principle of CMV effectively. By using DFI, the analytical result of CMV could be coupled with the CM impedance, thereby conducting the CMC. The impact of all other variables, such as motor and controller parameters, could be actively evaluated through analytical equations instead of repeating the simulation. However, for some novel and complex modulation methods with irregular modulation waveforms, the DFI bounds might be difficult to derive, which will increase the difficulty of applying the proposed model.

According to the performance evaluation, each PWM has its merits and drawbacks. Applying a single method in a full modulation range is not an optimal solution. Combining

several PWMs with respect to specific operational scenarios can be a balanced approach, which is also the future work of this paper.

It is also found that FPGA's high control frequency can benefit the DM reduction while having little impact on the CMC. An analytical model considering other non-ideal factors such as the sampling frequency and delay is also subject to future work.

Chapter 5 COMMON-MODE VOLTAGE ELIMINATION FOR DUAL THREE-PHASE INVERTERS

This chapter concentrates on the common-mode voltage elimination based on the six-phase motor drive system.

Due to the physical limits of the three-phase structure, none of those reduced-CMV PWMs that have been reviewed in the previous chapters can fully eliminate the CMV. As the motor phases have been extended to even numbers, such as six phases, opportunities to eliminate the CMV by a proper modulation scheme emerge. This chapter proposes a new modulation method to fully eliminate or reduce the CMV for the full modulation span of a dual-three-phase motor drive system, thereby helping to shrink the CM filter. Mathematical models are built indicating the effectiveness of eliminating the CMV in the linear range of the modulation index and reducing the CMV in the overmodulation range. The simulation results along with experiments implemented on the FPGA-controlled dual three-phase inverters validated the effectiveness of the proposed control algorithm in a full modulation span.

The structure of this chapter is organized as the following. Section 1 introduces the modulation method and CMV in the six-phase motor drive system. Section 2 proposes a pulse manipulation scheme in six-phase structure for CMV elimination. A detailed mathematical model of the for the proposed method is built. Section 3 uses the Simulink model to study the theoretical modulation behavior. In Section 4, the experimental result is presented to indicate its effectiveness in the full modulation range. Section 5 is the summary.

5.1 Modulation of Six-phase Motor Drive System

Space vector modulation (SVM) is widely adopted in the three-phase motor drive system. With the switching frequency increasing particularly when using wide-bandgap (WBG) devices, the common-mode voltage (CMV) becomes the major drawback. As shown in Figure 5.1, traditional center-aligned pulse width modulation (PWM) generates CMV varying between $\pm V_{dc}/6$ or $\pm V_{dc}/2$ in a three-phase two-level inverter.

Eqn (5.1) defines the CMV in a three-phase system, where V_{ao} , V_{bo} , V_{co} denote the voltage between the phase leg output and the DC-link middle point. These values show the CMV can never be zero, which subsequently yields a large CM choke for the sake of complying with CM standards, such as CISPR 25 in electric vehicles (EVs). Both cost and weight are then added to the inverter system. As the six-phase motors draw more attention in the past decades, eliminating the CMV becomes possible in two-level inverters.

Eqn (5.2) formulates the CMV for a DTM. Due to the even phase count, the CMV elimination becomes theoretically feasible.

For safety concerns, the motor case and the middle point of the DC-link are typically grounded to the chassis [44]. The parasitic capacitor (C_s) across the winding neutral and chassis will provide the path for the CM current (CMC), induce shaft voltage, and bearing current [131-134]. This will cause insulation failure, greatly shorten the motor lifespan, and cause significant EMI problems. To make the situation worse, wide bandgap (WBG) devices such as SiC MOSFETs are more commonly being used in motor drive systems. Their superior switching performance results in high CMV by introducing a high switching frequency (f_s) and high dv/dt [99, 135].

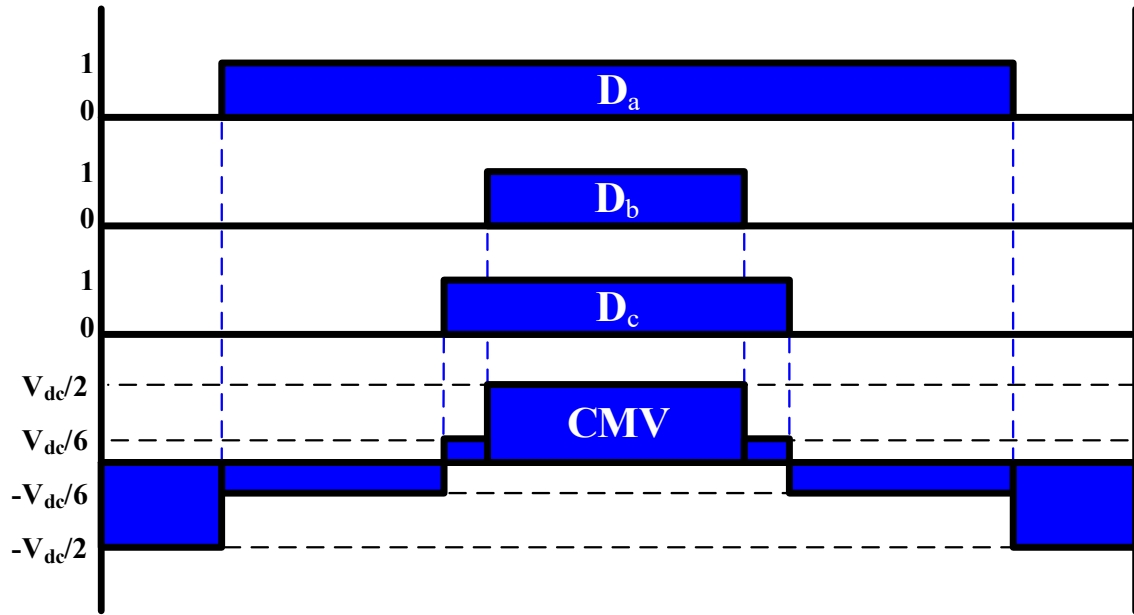


Figure 5.1: Three-phase center-aligned modulation and corresponding CMV.

$$V_{CM} = \frac{(V_{ao} + V_{bo} + V_{co})}{3} \quad (5.1)$$

$$V_{CM} = \frac{(V_{ao} + V_{bo} + V_{co} + V_{do} + V_{eo} + V_{fo})}{3} \quad (5.2)$$

In the six-phase modulation, we can take the conventional sinusoidal PWM (CSPWM) as an example. The gate signals of all switches are still center-aligned, as shown in Figure 5.2. Here, D_{a-f} denotes the duty cycle of each phase, and the overall CMV exhibits a 7-level profile with a peak value equal to $\pm V_{dc}/2$. Given each switch-on action results in the step of $V_{dc}/2$ at the corresponding phase-leg output and a switch-off action generates $-V_{dc}/2$, every switching action at any phase results in a step change of the CMV. For a conventional PWM control, in one switching period switching actions of two phases cannot happen simultaneously, which still yields a large CMV.

By shifting or splitting PWM signals to create switch-on/off pairs among phases while keeping the duty cycle of phases unchanged, CMV can be eliminated as the $\pm V_{dc}/2$ step-changes at different phases offset each other. This approach is named zero CMV modulation (ZCMVM) illustrated in the right plot of Figure 5.2 [109]. Such a pulse shifting mechanism does not change the total number of switching actions in one switching period. Therefore, the switching loss remains the same as CSPWM or CSVM.

5.2 Mathematical Model of CMV in DTM System

5.2.1 SPWM-based ZCMVM for Low/Medium Modulation Index ($MI \leq 0.785$)

Aligning the switch-on/off edges to cancel the CMV is the precondition to cancel CMV in the DTM system. The question remains as to whether this alignment can be applied

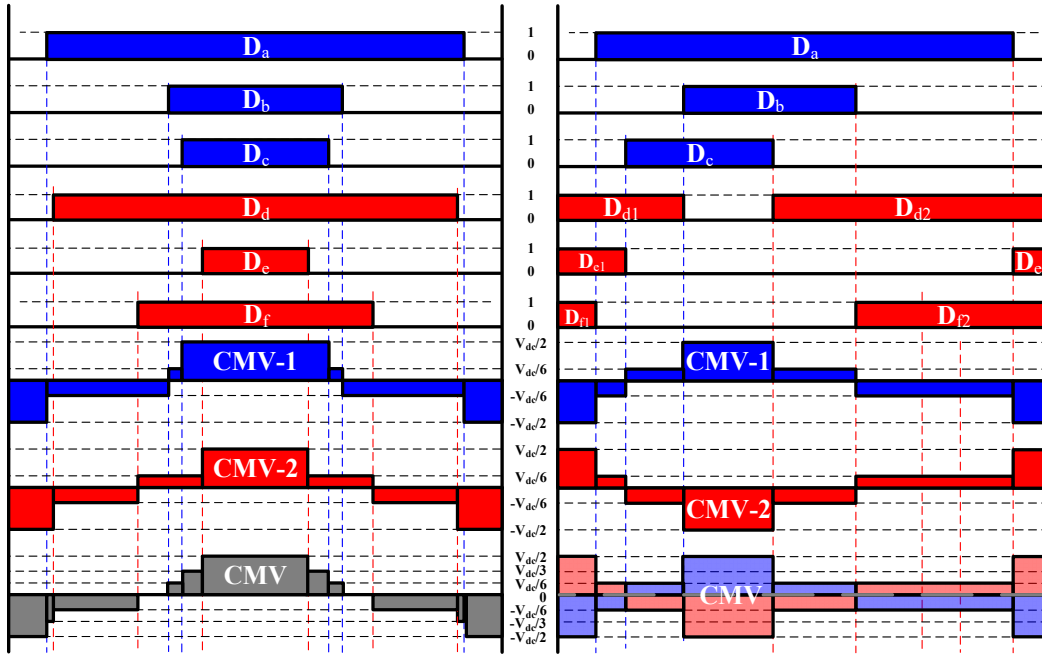


Figure 5.2: Modulation scheme and the corresponding CMV.

Left: CSPWM, Right: ZCMVM.

in the whole switching period and extended to the whole modulation range. A mathematical model of CMV is important to explore the possibility. For SPWM, the duty cycle for each phase can be expressed as Eqn (6.2-1), where MI is the modulation index, x represents the phase number ($a-f$), and $\theta=0, 2\pi/3, 4\pi/3, \pi/6, 5\pi/6, 3\pi/2$ for phase-A-F, respectively. Here, two sets of windings, ABC and DEF have a 30° phase difference according to the DTM definition.

$$D_x = \frac{1}{2} + \frac{2MI}{\pi} \cos(\omega t + \theta) \quad (5.3)$$

$$MI = \frac{\pi}{2} \frac{V_{ref}}{V_{dc}} \quad (5.4)$$

The PWM shifting and splitting rules can be referred to Figure 5.3. Assume the PWM signal of Phase-A follows CSPWM without any shift or split, pulse shifting happens to phase-B/C and pulse splitting happens to phase-D/E/F. The newly split pulses at the beginning of each switching period denote as $d1/e1/f1$, and those at the end of the switching period denote as $d2/e2/f2$. As a result, Eqns (5.5)-(5.10) could be derived. If all of the switch-on/off pairs can be aligned, D_{e2} must be equal to D_{f1} .

The PWM shifting and splitting rules can be referred to Figure 5.3. Assume the PWM signal of Phase-A follows CSPWM without any shift or split, pulse shifting happens to phase-B/C and pulse splitting happens to phase-D/E/F. The newly split pulses at the beginning of each switching period denote as $d1/e1/f1$, and those at the end of the switching period denote as $d2/e2/f2$. As a result, Eqns (5.5)-(5.10) could be derived. If all of the switch-on/off pairs can be aligned, D_{e2} must be equal to D_{f1} .

$$D_{f1} = \frac{1 - D_a}{2} \quad (5.5)$$

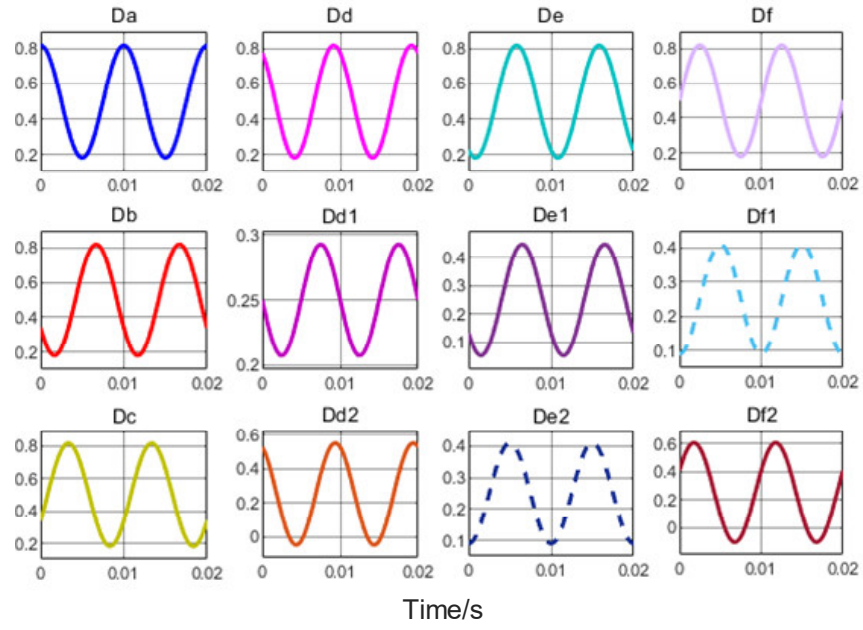


Figure 5.3: ZCMVM modulation waveforms @ $MI=0.5$.

to phase-B/C and pulse splitting happens to phase-D/E/F. The newly split pulses at the beginning of each switching period denote as $d1/e1/f1$, and those at the end of the switching period denote as $d2/e2/f2$. As a result, Eqns (5.5)-(5.10) could be derived. If all of the switch-on/off pairs can be aligned, D_{e2} must be equal to D_{f1} .

The PWM shifting and splitting rules can be referred to Figure 5.3. Assume the PWM signal of Phase-A follows CSPWM without any shift or split, pulse shifting happens to phase-B/C and pulse splitting happens to phase-D/E/F. The newly split pulses at the beginning of each switching period denote as $d1/e1/f1$, and those at the end of the switching period denote as $d2/e2/f2$. As a result, Eqns (5.5)-(5.10) could be derived. If all of the switch-on/off pairs can be aligned, D_{e2} must be equal to D_{f1} .

$$D_{f1} = \frac{1 - D_a}{2} \quad (5.5)$$

$$D_{f2} = D_f - D_{f1} \quad (5.6)$$

$$D_{d1} = 1 - D_b - D_{f2} \quad (5.7)$$

$$D_{d2} = D_d - D_{d1} \quad (5.8)$$

$$D_{e1} = 1 - D_c - D_{d2} \quad (5.9)$$

$$D_{e2} = D_e - D_{e1} \quad (5.10)$$

By substituting (5.3) to (5.5)-(5.10), D_{e2} and D_{f1} could be found as (5.11).

$$D_{e2} = D_{f1} = \frac{1}{4} - \frac{MI}{\pi} \cos(\omega t) \quad (5.11)$$

This validates that shifting and splitting PWMs to align all switching pairs are theoretically feasible regardless of the modulation index. However, the challenge is that such rules might not apply when the modulation index is high. For instance, when the modulation index is 0.5, Figure 5.3 shows the original modulation waveforms for D_{a-f} and

the updated modulation waveforms for $D_{d-fl,2}$. The reference waveform of D_{f2} reaches below 0, which is physically not applicable thereby causing the phase current distortion. The root cause is, in some cases, the PWM shifting and splitting rule twists the original duty cycle to force the edges to align. If Phase-A is always fixed as the reference phase, and the duty cycle of Phase-B/C becomes larger, the PWM shifting will be difficult to realize as there is very limited room to move pulses. The solution is to fix the phase with the too high or low duty cycle as the stationary phase while shifting the other two.

To locate the stationary phase properly, Figure 5.4 introduces the proposed zone division rule. By solving Eqn (5.12), a fundamental period could be divided into 6 zones by every 60° . The zone and corresponding stationary phase are given in Figure 5.4 as well.

$$D_{max} = 1 - D_{min} \quad (5.12)$$

5.2.2 SVM-based RCMVM for High Modulation Index ($0.785 < MI \leq 0.906$)

As the stationary phase varies from zone to zone, the ZCMV requirement also changes. The rule and corresponding switching sequences are given in Table. 5.1. Figure 5.5 illustrates the PWM manipulation rule in each zone. The proposed ZCMVM above is essentially an SPWM-based method, which limits the maximum linearity range to 0.785. To increase the DC-bus voltage utilization, SVM is one of the most popular schemes where the 3rd order harmonic is injected. Whether the same ZCMV rule could apply to SVM then needs further investigation. For SVM, the duty cycle for each phase is formulated as Eqn (5.13), where x represents the phase index and $\theta=0, 2\pi/3, 4\pi/3, \pi/6, 5\pi/6, 3\pi/2$ for phase-A-F, respectively, and the D_{3rd} is the corresponding 3rd order harmonic injection. For each set of three-phase windings, the injected 3rd voltage harmonics have a 30° difference.

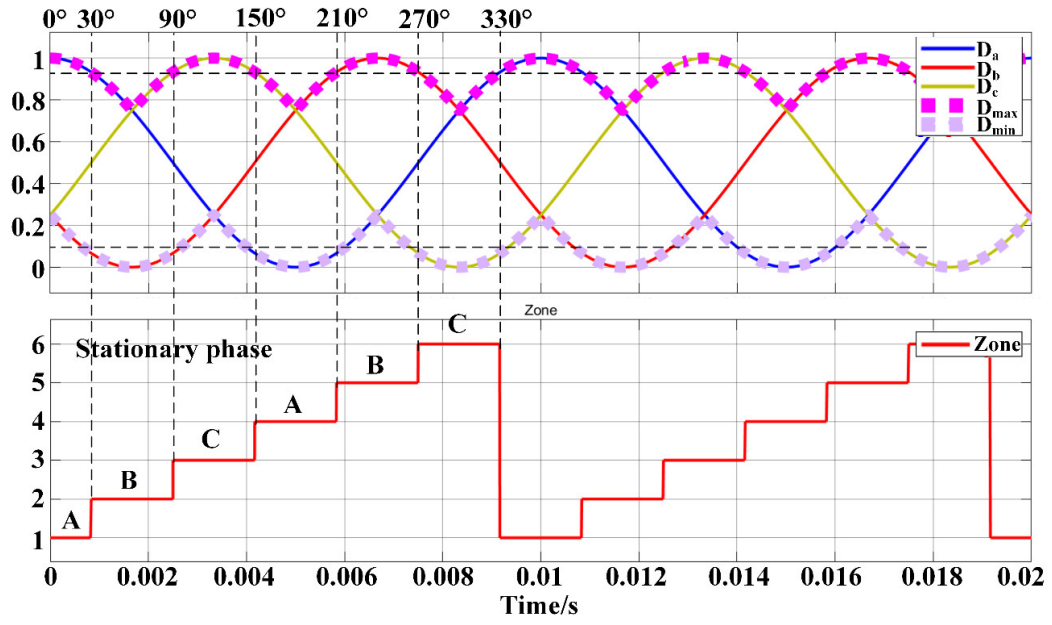


Figure 5.4: ZCMVM modulation waveforms @ $MI=0.5$.

Table 5.1: ZCMVM rules

Zone 1,4	Stationary phase	S_a	S_b	S_c	S_d	S_e	S_f	ZCMV requirement
$\omega t(^{\circ})=0\sim 30$ & 150~210 & 330~360	A	0	0	0	1	1	1	$D_{e2}=D_{f1}$
		1	0	0	1	1	0	
		1	0	1	1	0	0	
		1	1	1	0	0	0	
		1	1	0	1	0	0	
		1	0	0	1	0	1	
		0	0	0	1	1	1	
Zone 2, 5	Stationary phase	S_a	S_b	S_c	S_d	S_e	S_f	ZCMV requirement
$\omega t(^{\circ})=30\sim 90$ & 210~270	B	0	0	0	1	1	1	$D_{d1}=D_{f2}$
		0	0	1	1	0	1	
		1	0	1	1	0	0	
		1	1	1	0	0	0	
		1	0	1	0	0	1	
		1	0	0	1	0	1	
		0	0	0	1	1	1	
Zone 3, 6	Stationary phase	S_a	S_b	S_c	S_d	S_e	S_f	ZCMV requirement
$\omega t(^{\circ})=90\sim 150$ & 270~330	C	0	0	0	1	1	1	$D_{e1}=D_{d2}$
		0	0	1	1	0	1	
		0	1	1	0	0	1	
		1	1	1	0	0	0	
		1	0	1	0	0	1	
		0	0	1	0	1	1	
		0	0	0	1	1	1	

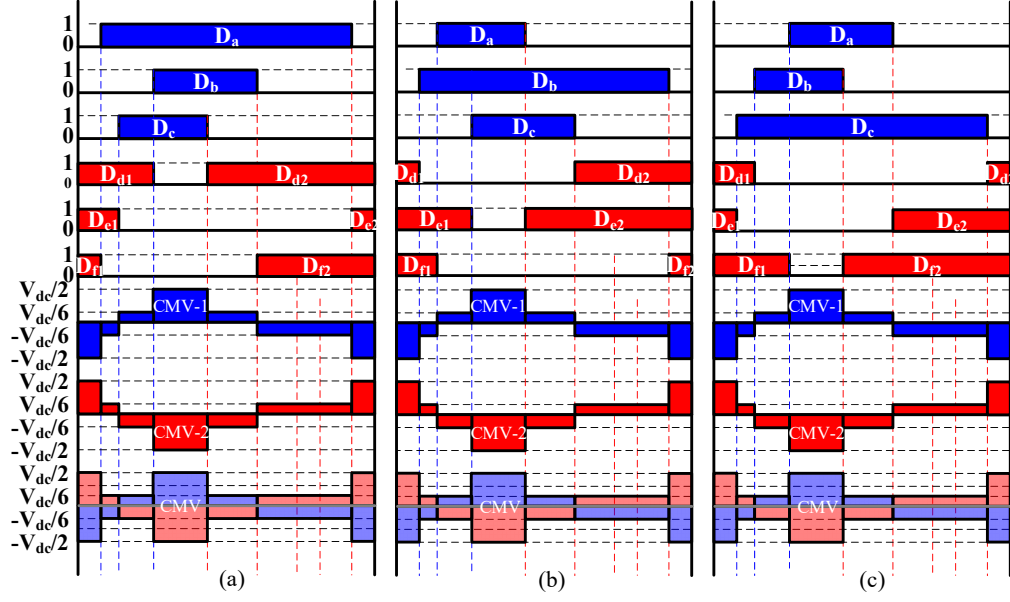


Figure 5.5: ZCMVM pulse manipulation rules in different zones.

(a) zone-1,4, (b) zone-2, 5, (c) zone-3, 6.

$$D_x = \frac{1}{2} + \frac{2MI}{\pi} \cos(\omega t + \theta) + D_{3rd} \quad (5.13)$$

If following Figure 5.5 and Eqns (5.5)-(5.10), as shown in Eqn (5.14), D_{e2} is not equal to D_{f1} , the CMV cannot be eliminated. However, it still might reduce the CMV. If this is validated, the strategy for $MI > 0.785$ can be renamed from ZCMVM to reduced-CMV modulation (RCMVM).

$$D_{e2} - D_{f1} = 3(D_{3rd-abc} + D_{3rd-def}) \quad (5.14)$$

Note that pulse manipulation needs to avoid phase current distortion. For a split PWM, if the left piece cannot align the edge, the algorithm might force the alignment to happen by enlarging its length. As a result, the right piece length goes negative, which is not feasible but only causes the phase current distortion. Figure 5.6 shows the modulation waveforms for RCMVM when $MI = 0.906$. None of the adjusted duty cycles go below zero.

5.2.3 SVM-based RCMVM for Overmodulation ($0.906 < MI < 1$)

For the conventional SVM, the overmodulation capability is necessary to maximize the DC-bus voltage utilization. In [117, 118], the authors divided the overmodulation range into two segments, i.e., $0.906 < MI < 0.952$ (mode-I) and $0.952 < MI < 1$ (mode-II) and enhanced the THD performance compared with other overmodulation methods. This paper based on their work adopts the same RCMVM method as the MI increases.

The modulation waveforms for two overmodulation modes are shown in Figure 5.7. Since in the overmodulation range the zero-vector operating time is reduced as well as the CMV, the total CMV reduction will not be as significant as in the linearity modulation range. When $MI = 1$, there are no differences between CSVM and the proposed RCMVM.

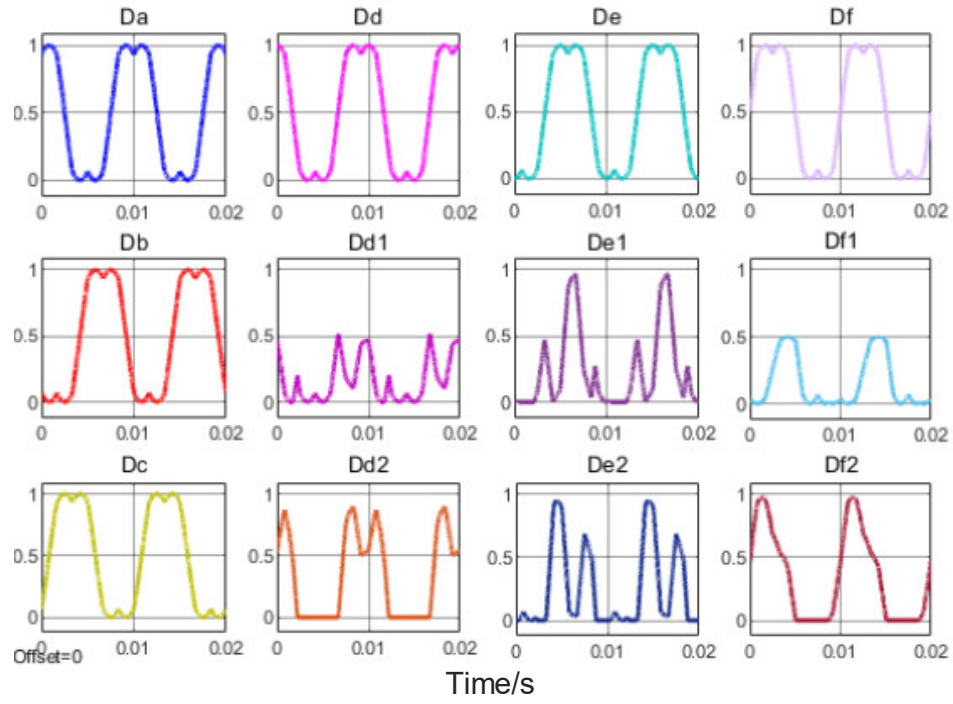


Figure 5.6: RCMVM modulation waveforms @ $MI=0.906$.

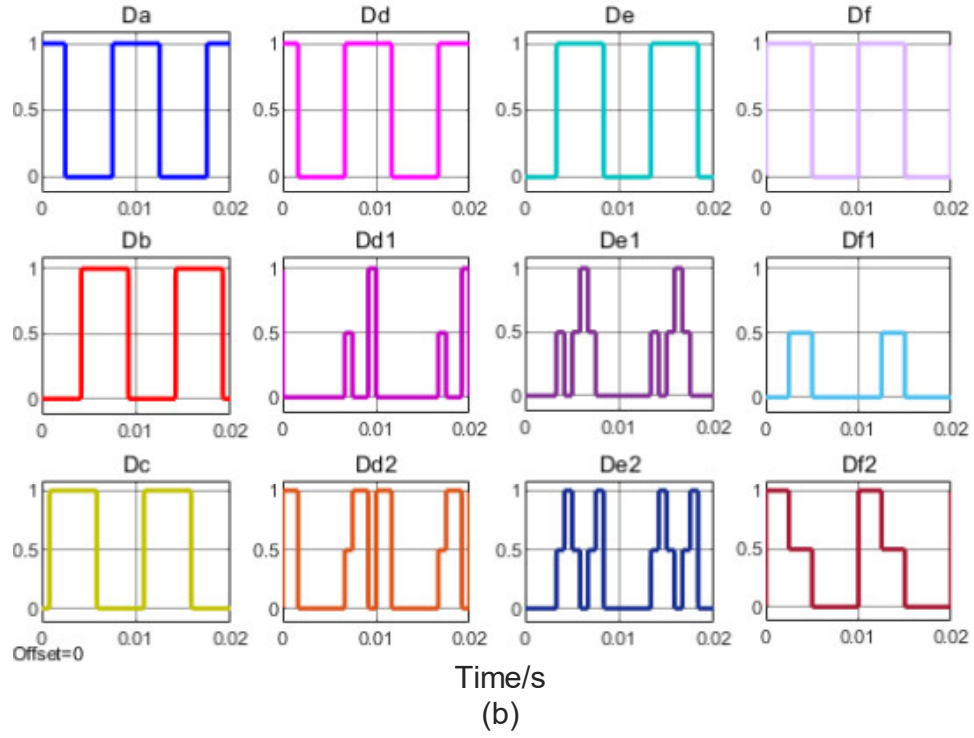
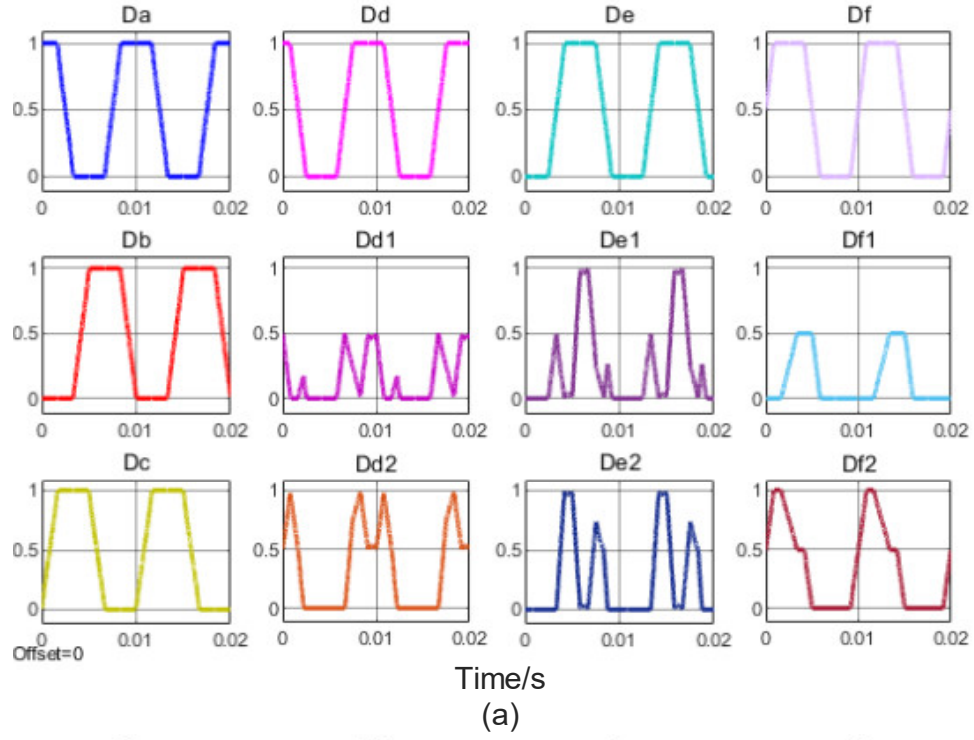


Figure 5.7: RCMVM overmodulation waveforms.

(a) $MI=0.95$, (b) $MI=1$.

The mechanism of pulse manipulation in high modulation and overmodulation is the same, trying to align rising and falling edges to reduce the CMV. For the edges that fail to be aligned, the CMV will remain. This will happen not in the linear modulation range, but in the over-modulation range. Figure 5.8 illustrates the RCMVM operation, where the falling edge of D_c and the rising edge of D_{d2} failed to be aligned. As a result, the CMV between this interval still exists though the rest of the CMV in other areas is canceled. Therefore, the proposed modulation scheme eliminates the CMV in the low and medium modulation index range ($0 < MI \leq 0.785$) and reduces the CMV in the high and overmodulation range ($0.785 < MI \leq 1$), which is named zero/reduced CMV modulation (ZRCMVM).

5.3 Implementation and Simulation Result

Changing the carrier waveforms can realize the PWM shifting and splitting. However, for the proposed ZRCMVM, the PWM shifting/splitting occurs rapidly, causing significant difficulty in carrier waveform modification. In this paper, another efficient PWM manipulation method is proposed. As shown in Figure 5.9, by calculating the ON/OFF duty cycle for each phase, we can compare it with the carrier and calculate the intermediate part with the “AND” logic to obtain the duty cycle. By moving and splitting the ON/OFF duty cycle, the PWM manipulation can be realized, as shown in Eqns (5.15)-(5.17).

This method is applicable in an FPGA, utilizing Xilinx-provided model-based coding tools for MATLAB Simulink. In the EV domain, high-resolution microcontrollers, such as FPGAs draw more attention nowadays. With the unique parallel computation

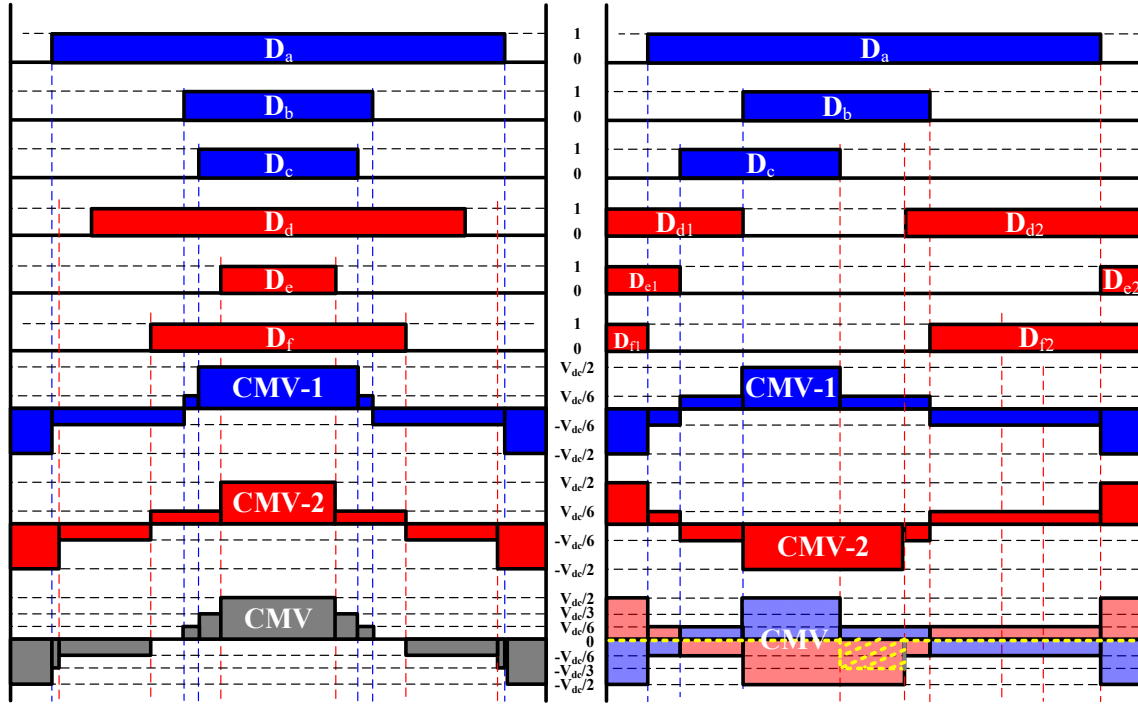


Figure 5.8: Modulation scheme and the corresponding CMV.

Left: CSPWM, Right: ZCMVM.

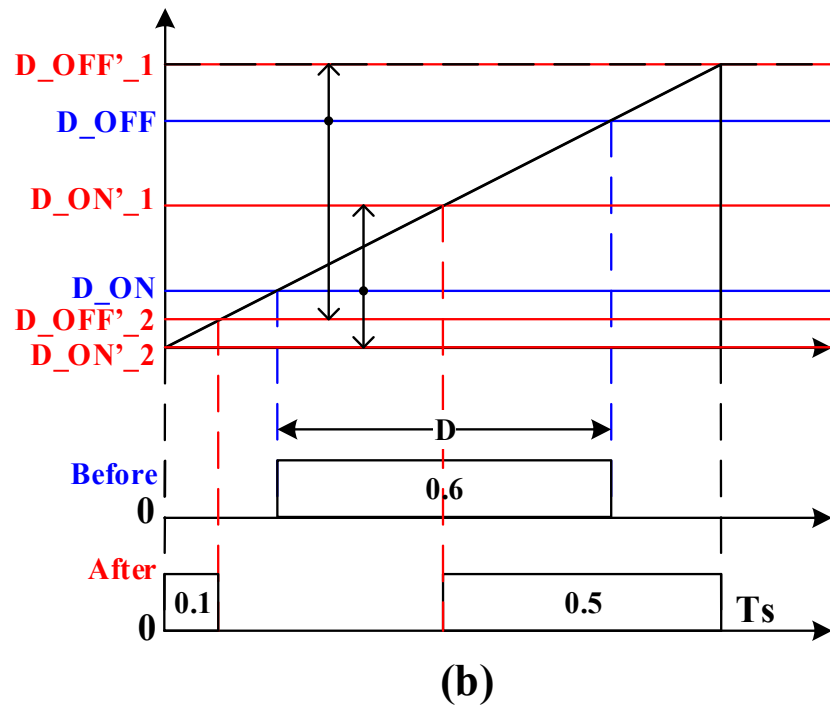
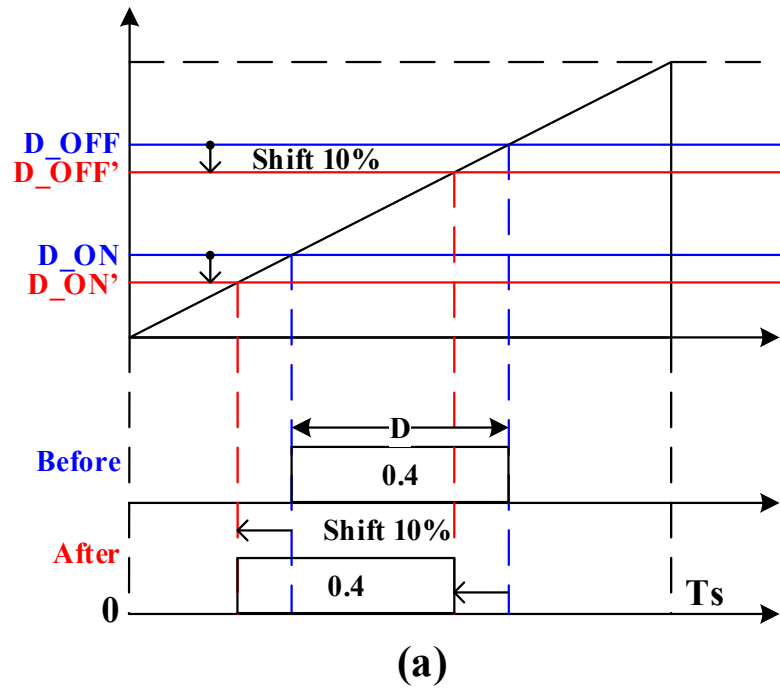


Figure 5.9: Proposed pulse manipulation method.

(a) Shifting, (b) Splitting.

capability, FPGAs can update duty cycles every switching period, reaching a higher control bandwidth. In this paper, all control logic is realized through Xilinx System Generator. As the simulation is finished, the control code is ready as well to power two inverters for the DTM.

$$D_{on-x} = \frac{1}{2} - \frac{1}{2} \left[\frac{2MI}{\pi} \cos(\omega t + \theta) + \frac{1}{2} \right] \quad (5.15)$$

$$D_{off-x} = \frac{1}{2} + \frac{1}{2} \left[\frac{2MI}{\pi} \cos(\omega t + \theta) + \frac{1}{2} \right] \quad (5.16)$$

$$D_x = D_{off-x} - D_{on-x} \quad (5.17)$$

5.3.1 Low/Medium modulation range ($0 < MI \leq 0.785$)

Figure 5.10 simulates the CMV at different zones, where the modulation index is 0.3, DC bus voltage is set to 30 V for the targeted 48 V motor drive application, the switching frequency is 10 kHz and the fundamental frequency is 100 Hz. The CSPWM is also depicted as a green dashed line. Note that the dead time is not considered in this simulation. The PWMs for each phase are moved properly and the CMV is eliminated by ZRCMVM.

In the CMV elimination process, the stationary phase changes every 60° to avoid potential phase current distortion. As a result, the load current is shown in Figure 5.11. It shows with the proposed method of changing the stationary phase per 60° , the phase current distortion disappears, the linear range is secured. If no proper regulation, as the modulation index increases, the distortion become worse. The linear modulation range will be drasftically limited.

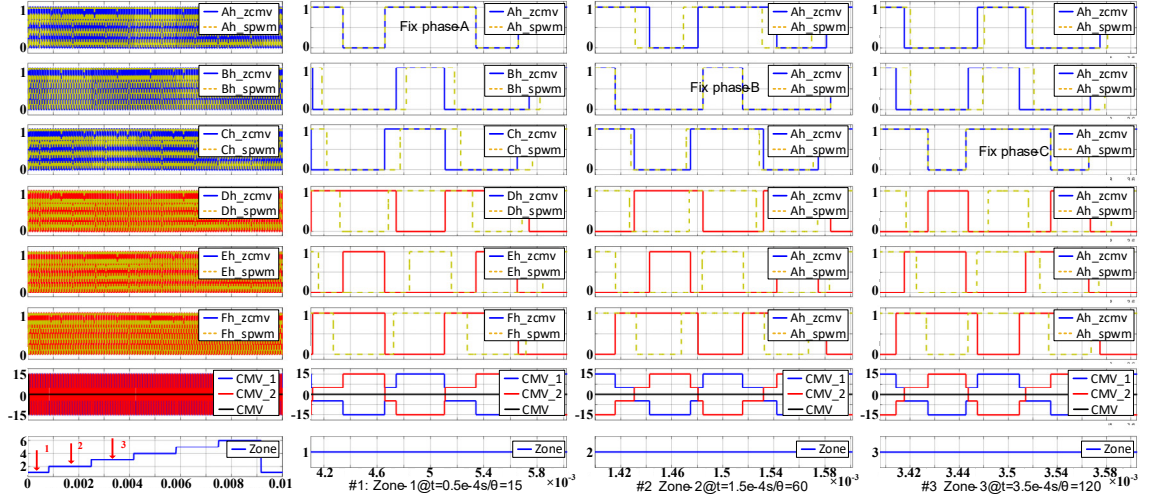


Figure 5.10: Simulated CMV with ZRCMVM @MI=0.3.

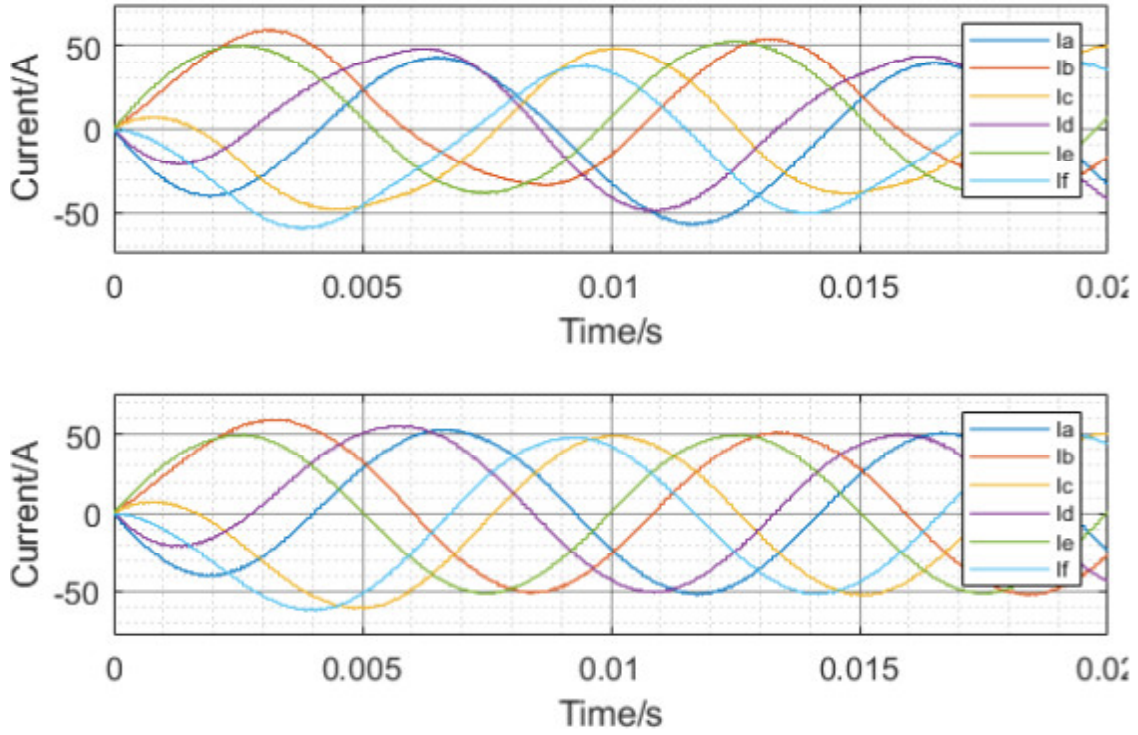


Figure 5.11: Simulated phase current waveform.

Top: without zone division, Bottom: with zone division.

5.3.2 High/overmodulation range simulation ($0.785 < MI \leq 1$)

When the modulation index exceeds 0.785, the ZRCMVM is adjusted to the reduced-CMV mode. Figure 5.12 shows the simulation result at the maximum linearity modulation point ($MI=0.906$), the ending point of the overmodulation range mode-1 ($MI=0.95$), and the full modulation point ($MI=1$), respectively. In this range, the CMV starts to appear, although most of the $\pm V_{dc}/2$ components are eliminated due to the proper pulse manipulation. As the modulation enters the overmodulation range, the zero-vector time duration decreases, yielding a lower CMV even for the conventional SVM. When full modulation is achieved, there is no room for any PWM manipulation, and the performance of CMV reduction for CSVM and ZCMVM becomes identical. Such simulation results are aligned with the previous analytical analysis.

The fast Fourier transform (FFT) result of Figure 5.12 is shown in Figure 5.13. Aligned with the time domain analysis above, the proposed ZRCMVM generated CMV but still reduced compared to CSVM. Starting from the short-wavelength conductive CM EMI range (150 kHz–300 kHz) defined in CISPR-25, the maximum CMV components are reduced by half when $MI=0.906$ and by 1/3 in the overmodulation Mode-I. When full modulation is realized, the CMV spectrum of CSVM and ZRCMVM becomes identical.

5.3.3 Differential-mode performance

The impact of various CMV reduction methods on the DM performance needs to be closely monitored, given the phase current ripple and THD are closely related to PWM patterns. Some PWMs, such as AZSPWM, aim to reduce the CMV by splitting certain phase pulses to avoid using zero-vectors but generate a much larger ripple current on both

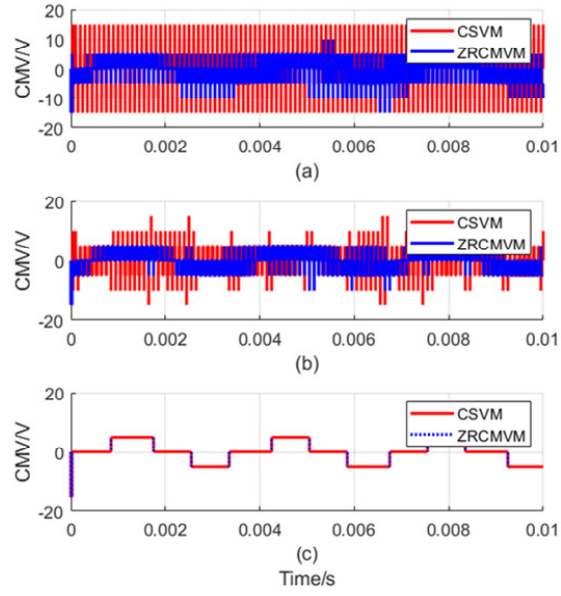


Figure 5.12: CMV waveform under high/overmodulation.

(a) $MI=0.906$, (b) $MI=0.95$, (c) $MI=1$.

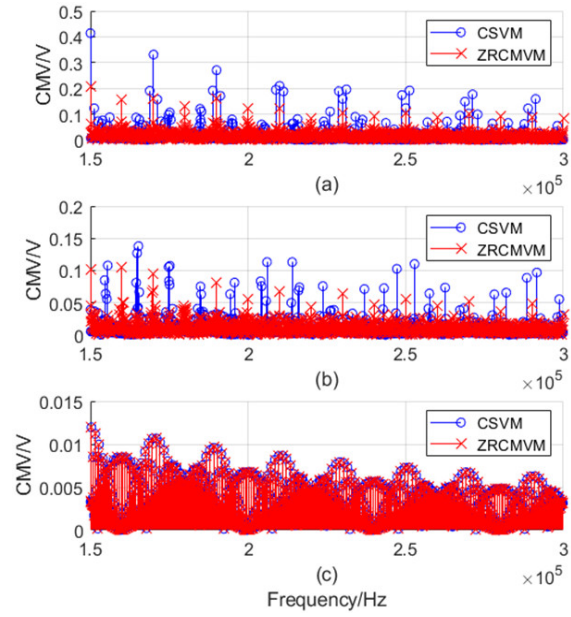


Figure 5.13: CMV spectrum under high/overmodulation.

(a) $MI=0.906$, (b) $MI=0.95$, (c) $MI=1$.

the DC-link side and the AC motor side. This not only worsens the harmonic performance but also causes acoustic noise during the operation. Therefore, the PWM manipulation process in the proposed ZRCMVM also needs to be evaluated. The simulation results of the input/output DM performance are shown in Figure 5.14 and Figure 5.15, performed with a 30 V DC bus voltage to fit the 48 V six-phase motor application, 10 kHz switching frequency, and 100 Hz fundamental frequency. Here, CPWM denotes a combined PWM pattern, which uses CSPWM for $MI < 0.785$ and CSVN for $MI > 0.785$ to have a fair comparison with the proposed ZRCMVM.

On the input side, the DC-link capacitor current is critical to the DC-link capacitor selection, which strongly affects the system size. Figure 5.14 shows the simulation result of the DC-link capacitor current for CPWM, ZRCMVM, and AZSPWM. The DC-link capacitor current of ZRCMVM, though slightly larger than CPWM, shows similarity to CPWM with a maximum difference of 5 A. Such a small difference has very little impact on the capacitor selection. For AZSPWM, the DC-link capacitor current ripple is significantly larger than ZRCMVM, which requires larger DC-link capacitors. Here we simulated the current RMS values.

On the output side, the major DM performance lies in the phase current ripple. Based on the simulation result shown in Figure 5.15(a), the proposed ZRCMVM always has a higher ripple in the linear modulation range than CPWM. As the modulation index increases, the ripple difference between ZRCMVM and CPWM decreases. In the overmodulation range, the difference is negligible. From the THD perspective, as shown in Figure 5.15(b), the current THD of ZRCMVM continuously drops as the modulation index increases. The overall gap is narrow and acceptable. Compared to ZCMVM and

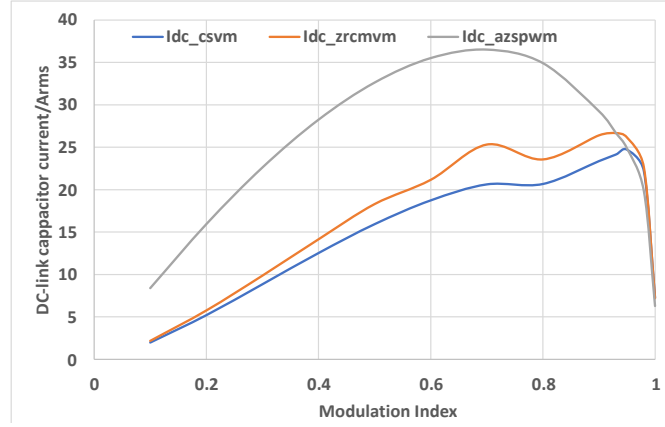


Figure 5.14: DC-link capacitor current comparison.

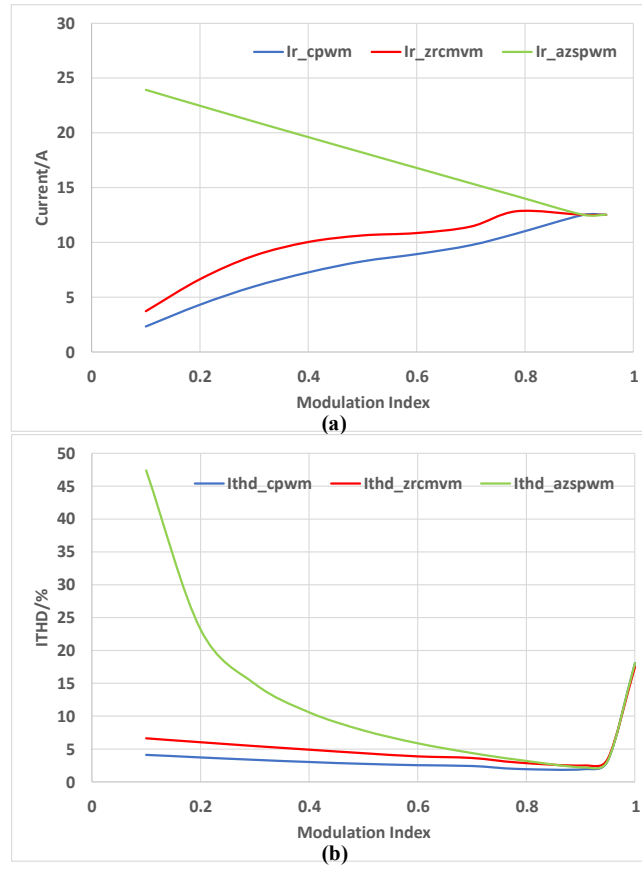


Figure 5.15: Differential-mode impact at the output side.

(a) Phase current ripple comparison, (b) Phase current THD comparison.

CPWM, AZSPWM has very poor performance in terms of both current ripple and THD, especially in the low modulation index range. Reference [114] has proposed the phase current prediction model for AZSPWM to explain the essential cause, i.e., the split medium length PWM extends the time that the voltage imposed on the phase inductance, resulting in a larger current ripple. Such comparison shows the superiority of ZRCMV when considering the DM performance that other reduced-CMV PWMs will not offer.

5.3.4 Dynamic performance

Throughout the whole modulation span, there are two different modulation mechanisms. For $MI \leq 0.785$, the strategy is CSPWM-based ZCMV modulation. And for $MI > 0.785$, the strategy is CSVM-based RCMV modulation. In motor drive applications, the modulation index varies dynamically as the motor changes its status. Therefore, the transient performance when the modulation index passes through the boundary should be investigated.

Given the step change of the MI from 0.75-0.82 at 0.01 s. As shown in Figure 5.16, the sinusoidal modulation waveform will change to the space vector modulation waveform, which is injected with 3rd order harmonics. The simulation of the transient process for a region switch is shown in Figure 5.17. As the MI jumps into the RCMV modulation range, the CMV starts to appear. The amplitude of the phase current increases accordingly with no inrush. This is another support for the conclusion in section C that the proposed modulation method shows less impact on the differential-mode performance.

The motor speed change refers to a fundamental frequency variation. Figure 5.18 shows the six-phase current waveform and CMV waveform during a fundamental

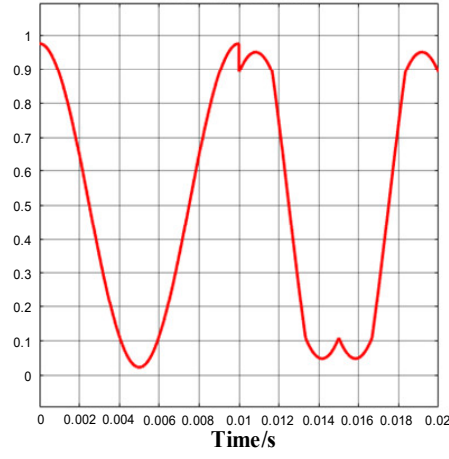


Figure 5.16: Modulation waveform for a MI step change.

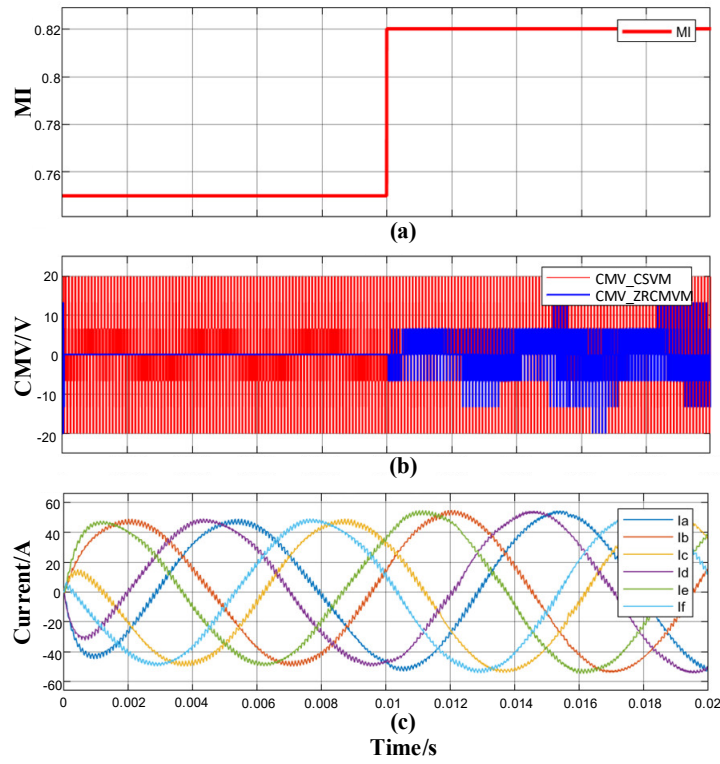
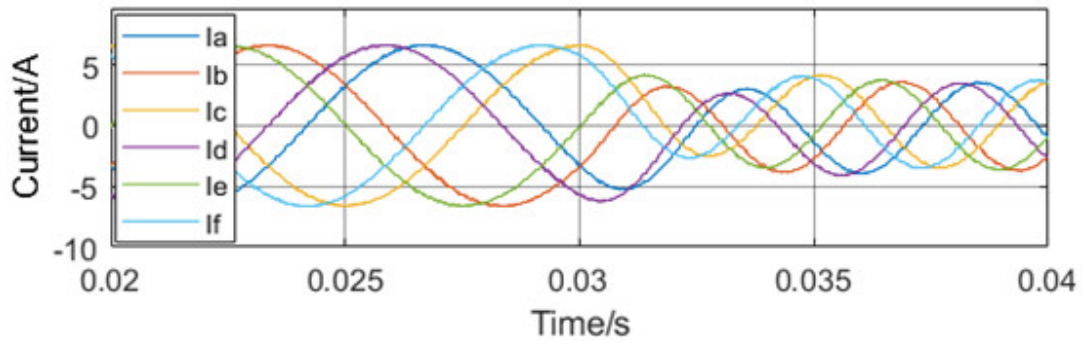
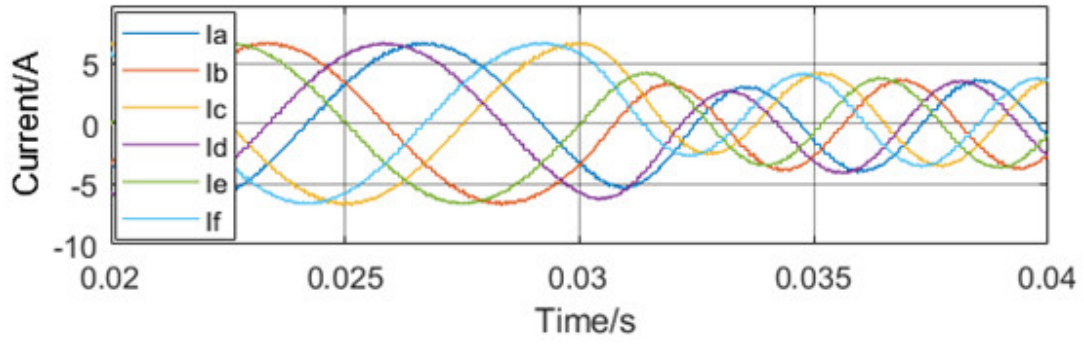


Figure 5.17: Transient process for region switch.

(a) Modulation index, (b) CMV, (c) Three-phase current.



(a)



(b)

Figure 5.18: Transient process for speed change.

(a) CSPWM, (b) ZRCMVM.

frequency change from 100 Hz to 200 Hz at 0.03 s. The transition during the speed change is smooth with no spikes or fluctuations, and the CMV elimination performance is not affected.

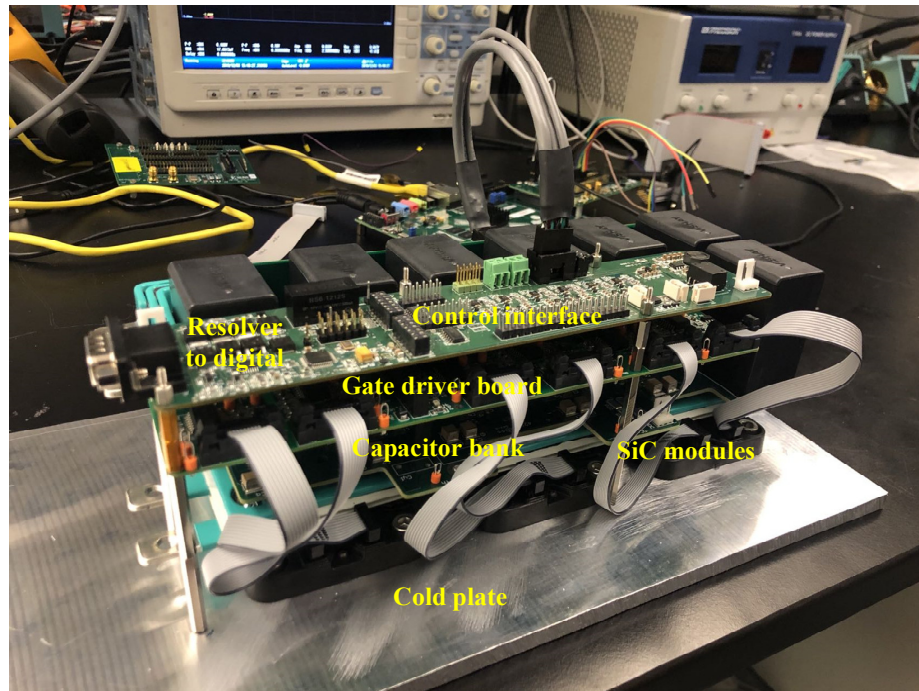
The transient simulation shows that the system dynamic performance is the same with CSPWM/CSVM, this is because the proposed ZRCMVM does not change the modulation waveform, but directly redistributes the PWM pulse generated by CSPWM/CSVM. Therefore, from the space vector point of view, the trajectory never changes. This applies to the whole modulation range. The only difference it brings to the system for DM is the current ripple change due to the irregular pulse assignment.

5.4 Experimental Validation

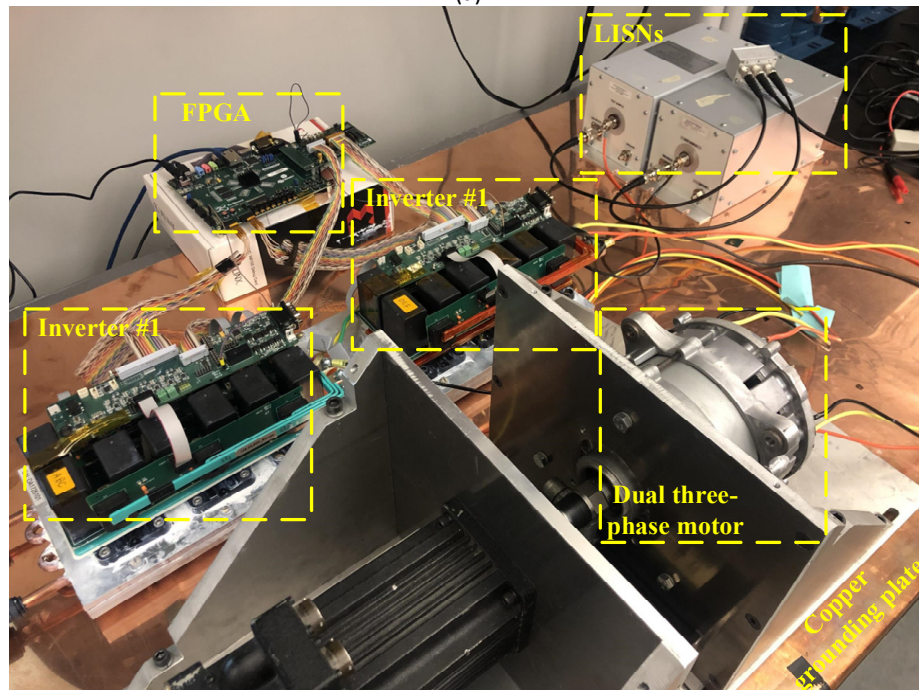
With the Xilinx System Generator toolbox, the Simulink model can be translated into the FPGA code. To set up the experimental validation, two three-phase inverters are designed to set up a DTM drive test bench, as shown in Figure 5.19(a). The SiC power module is from Wolfspeed (CAS325M12HM2, 1.2 kV, 444 A). Two inverters sit on a large cold plate for water cooling. The motor is rated at 48 V/10 kW with two separated neutral points.

The 48 V technology has been widely accepted in mild hybrid EVs, which enable considerable savings in fuel consumption with moderate additional costs [136-139]. Therefore, in this paper, a 48 V DTM is used as an example.

Figure 5.19(b) shows the test bench layout. The detailed test bench parameters are listed in Table 5.2. The whole system with LISNs sits on a grounded copper plate based on EMI measurement criteria.



(a)



(b)

Figure 5.19: DTM test bench.

(a) 100 kW SiC inverter, (b) Test bench layout.

Table 5.2: Test bench parameters

Item	Value	Unit
DC bus voltage	30	V
Output Power	5	kW
Switching frequency (f_s)	10	kHz
Fundamental frequency (f_o)	100	Hz

5.4.1 CMV Measurement

The CMV waveform is measured in 4 different modulation zones, as shown in Figure 5.20, the CMV measurement is processed in the ZCMV-linearity range ($MI=0.6$), RCMV-linearity range ($MI=0.8$), RCMV-overmodulation mode-I ($MI=0.95$), and RCMV-Full modulation ($MI=1$). Here, CMV1 and CMV2 represent the CMV on each set of three-phase windings, respectively.

According to the proposed CMV reduction strategy, for $MI < 0.785$, the waveform of CMV1 and CMV2 is mirror-symmetrical along the time axis to cancel each other thereby eliminating the overall CMV. For $MI > 0.785$ the CMV is reduced, even the waveform of CMV1 and CMV2 is not vertically mirrored. The experimental result shows good execution of the ZRCMVM method, despite the CMV spikes caused by the 300 ns dead time. Specifically, the unexpected CMV spike happens at the instants when two phases commutate simultaneously [140].

The dead-time effect is shown in Figure 5.21. Due to the existence of dead time, some CMV patterns are extended for a short period, which makes the symmetrical CMV on each three-phase set asymmetrical on the edge. As a result, at each commutation point, a $V_{dc}/3$ CMV pulse will be generated. For conventional center-aligned modulation, the simultaneous phase commutation caused CMV spike is negligible since the commutation always happens at the edge of the zero vector. In addition, the two-phase simultaneous commutations only happen once in a sector plane (twice for six-phase as there exists a 30° vector plane rotation). As a result, the CMV caused by deadtime is minimal. However, for the proposed ZRCMVM, each switching edge pair is intentionally assigned to be aligned, which means the two-phase simultaneous commutation happens in every switching cycle.

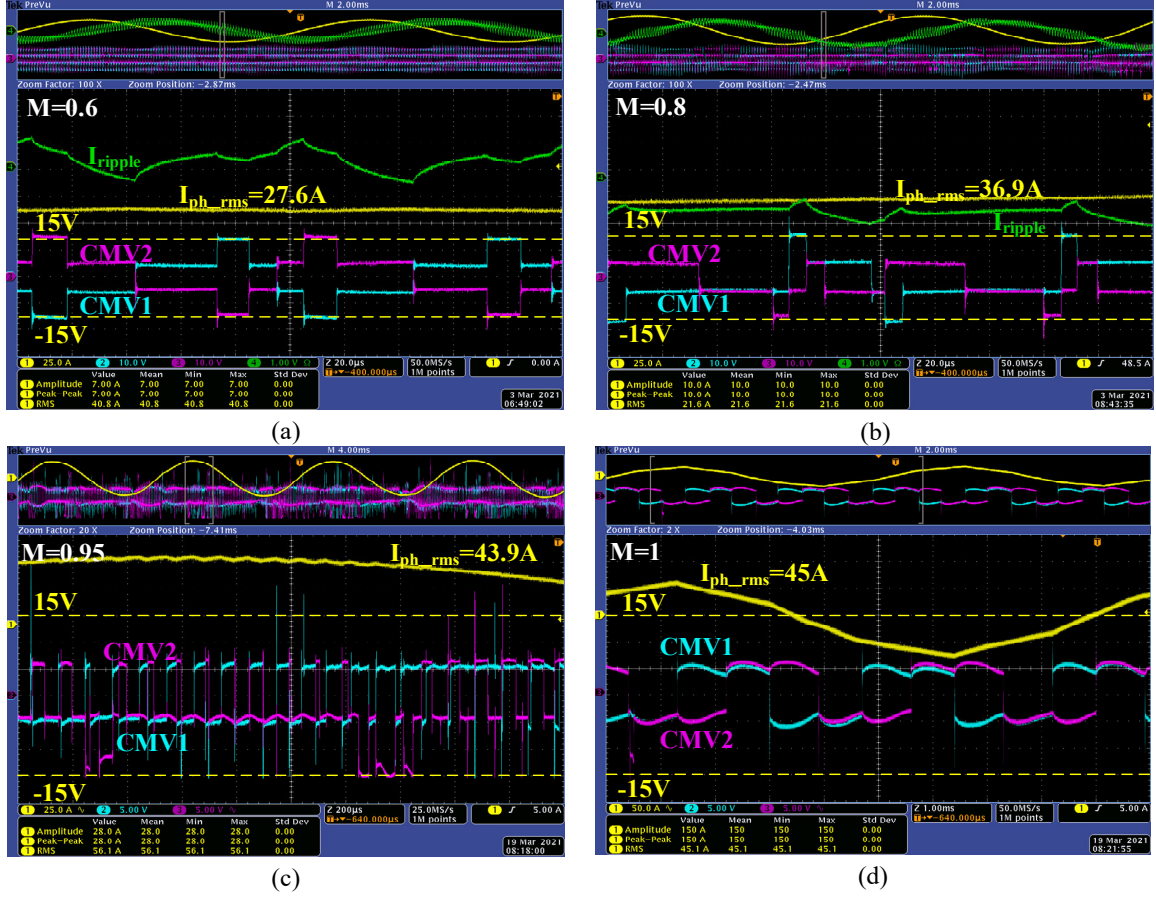


Figure 5.20: CMV waveform.

(a) ZCMV in linearity range ($MI=0.6$),

(b) RCMV in linearity range ($MI=0.8$),

(c) RCMV in overmodulation range mode-I ($MI=0.95$),

(d) RCMV in overmodulation range mode-II ($MI=1$, full modulation).

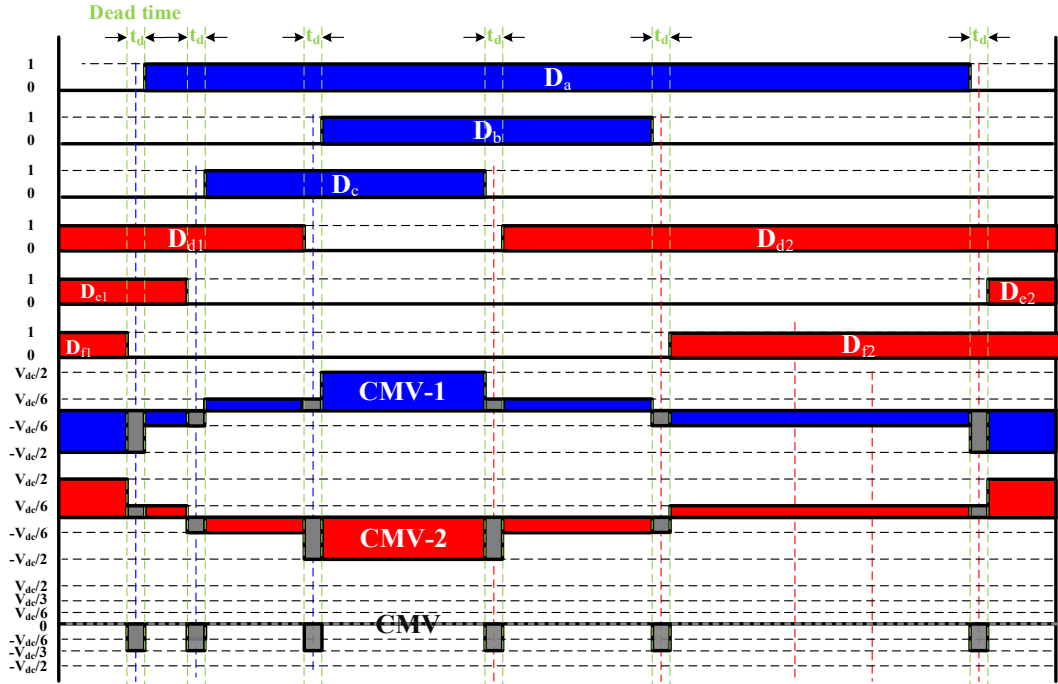


Figure 5.21: Dead time effect on CMV.

Therefore, the dead time caused by CMV spikes has more impact on the CM EMI performance for the ZRCMVM. There is much literature that has discussed the dead-time effect on the CMV and the corresponding compensation work. However, current direction and output voltage polarity detection are typically needed, which requires extra hardware support, such as current or voltage sensors [141-144]. Since this chapter targets the new modulation method mechanism, the dead time compensation will not be further investigated here.

At the same test condition, the measurement data of CSVM is also collected and compared with the proposed ZRCMVM, as shown in Figure 5.22 and Figure. 5.23. In the linearity range, compared with CSVM, ZRCMVM eliminates the CMV voltage levels in the medium and low modulation index and reduces CMV in the high modulation index range.

In this stage, the superiority of ZRCMVM is significant as it enters the overmodulation range, the CSVM also reduces the zero-state vector operation time with less zero-state duration. As a result, the CMV of CSVM starts to decrease. Though ZRCMVM still shows better CMV reduction performance, the gap between CSVM and ZRCMVM is narrowed.

Eventually, when the system reaches the full modulation, the two modulation schemes have no difference in the CMV performance, as shown in Figure 5.24, and the two CMV waveforms both become 3-level profile ($-V_{dc}/6$, 0 , $V_{dc}/6$). The observed CMV behavior is aligned with the theoretical analysis in Section II and the simulation result in Section III.

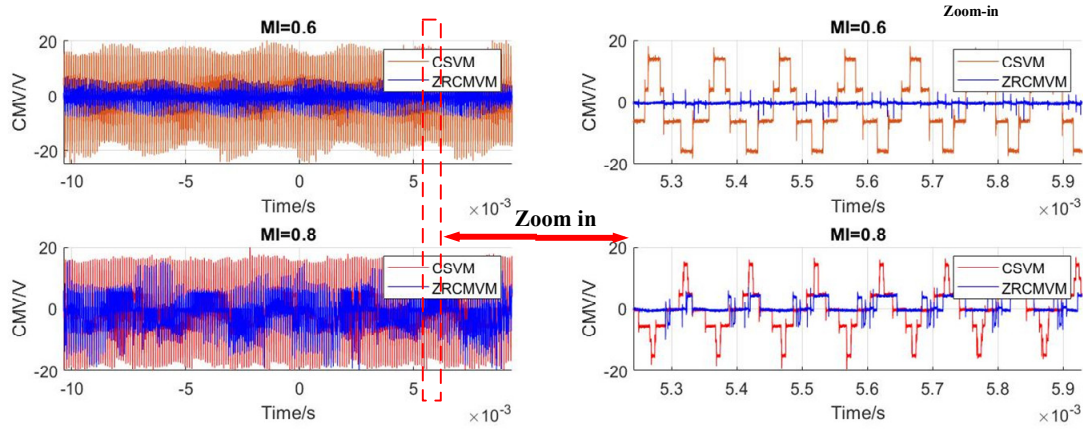


Figure 5.22: CMV comparison between CSVM and ZRCMVM in the linear range.

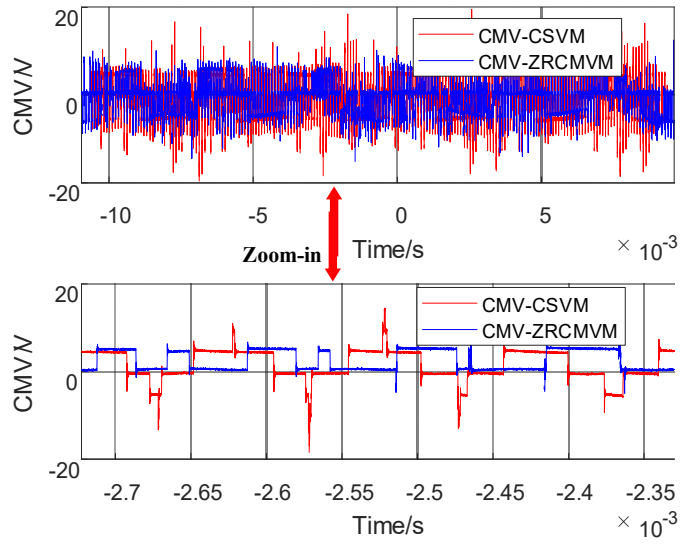


Figure 5.23: CMV comparison between CSVM and ZRCMVM in overmodulation range.

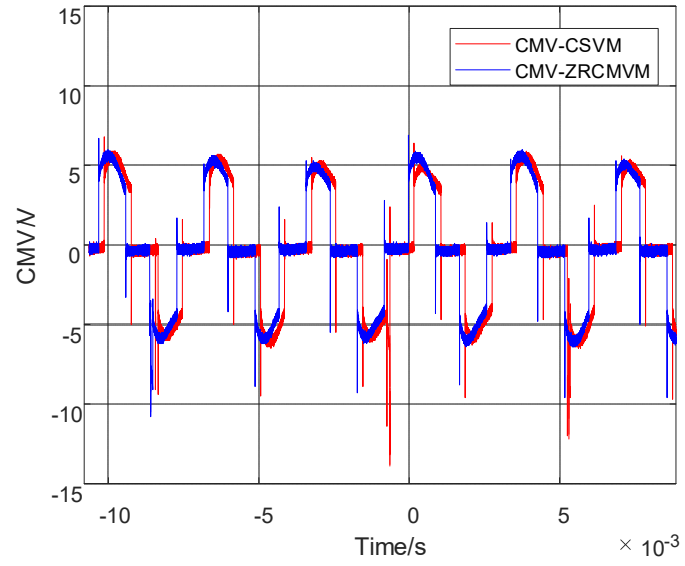


Figure 5.24: CMV comparison between CSVM and ZRCMVM at full modulation.

The experimental results above provide a direct performance comparison between CSVM and ZRCMVM through the time domain CMV waveform. However, in the motor drive system, the essential harm that the inverter brings to the motor lifespan is caused by the CM current (CMC). To further confirm the effectiveness of the proposed ZRCMVM, a quantitative comparison of the CMC is necessary, which relies on the line impedance stabilization network (LISN). LISN provides a stable and normalized source impedance ($50\ \Omega$ in this test) for the CMC measurement and prevents the external noise from interfering with the source side [82]. The measured CMC is then sent to the EMI analyzer through the power combiner, which allows the CMC component to pass while suppressing the DM component. The whole system sits on a copper grounding plate, where the inverter heatsink, motor case, and LISN are grounded.

The proposed model aims to eliminate the CMV profile through modulation, however, some dv/dt components still exist because of the switching actions and dead-time effect. Therefore, the high-frequency EMI noise dominated by the high-speed transient processes will not be effectively reduced compared to CSVM. Considering the CM filter is typically designed with respect to the low-frequency range as the high-frequency components are relatively easier to damp, the CM EMI spectrum on the low-frequency conductive range is measured, as shown in Figure 5.25, Figure 5.26, and Figure 5.27. This range (150 kHz-300 kHz) is defined in CISPR-25 as the longwave (LW) broadcast band, which is strongly affected by the modulation-based CMV reduction.

In the linear range when $MI=0.6$, the CMC reduction is significant. The maximum reduction is around 23 dBuV. Note that such measured voltage is the CMC multiplied with $50\ \Omega$ resistance inside the LISN. A drastic reduction of the CMC in the low-frequency

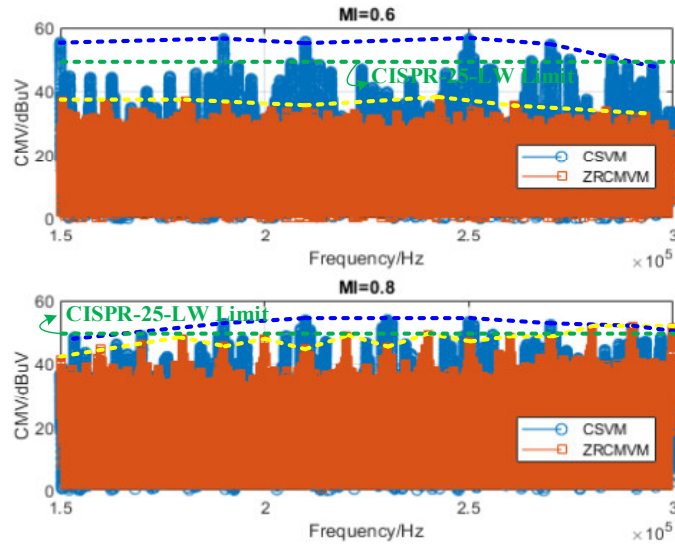


Figure 5.25: CMC spectrum comparison in the linear modulation range.

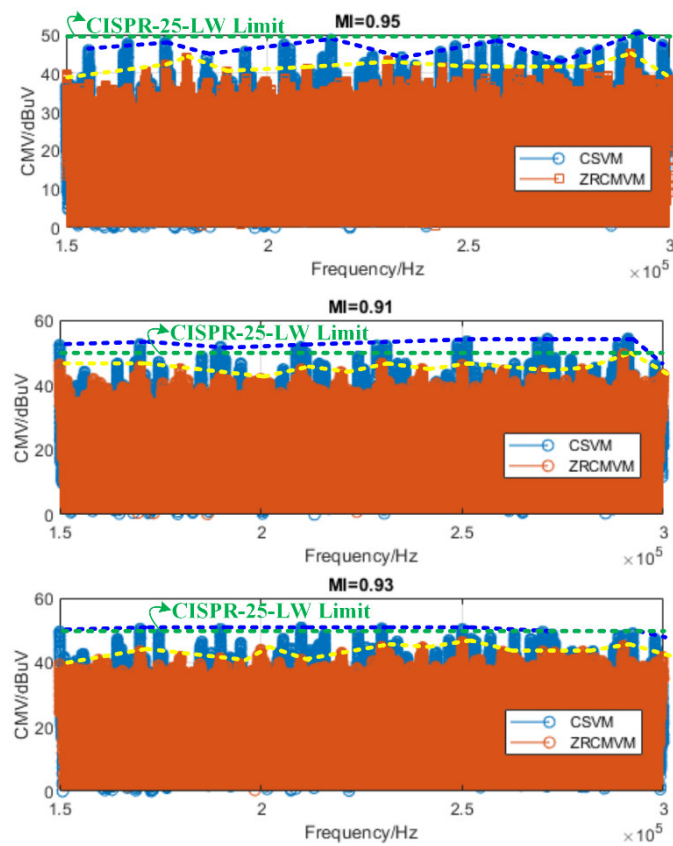


Figure 5.26: CMC spectrum comparison in the overmodulation range (mode-I).

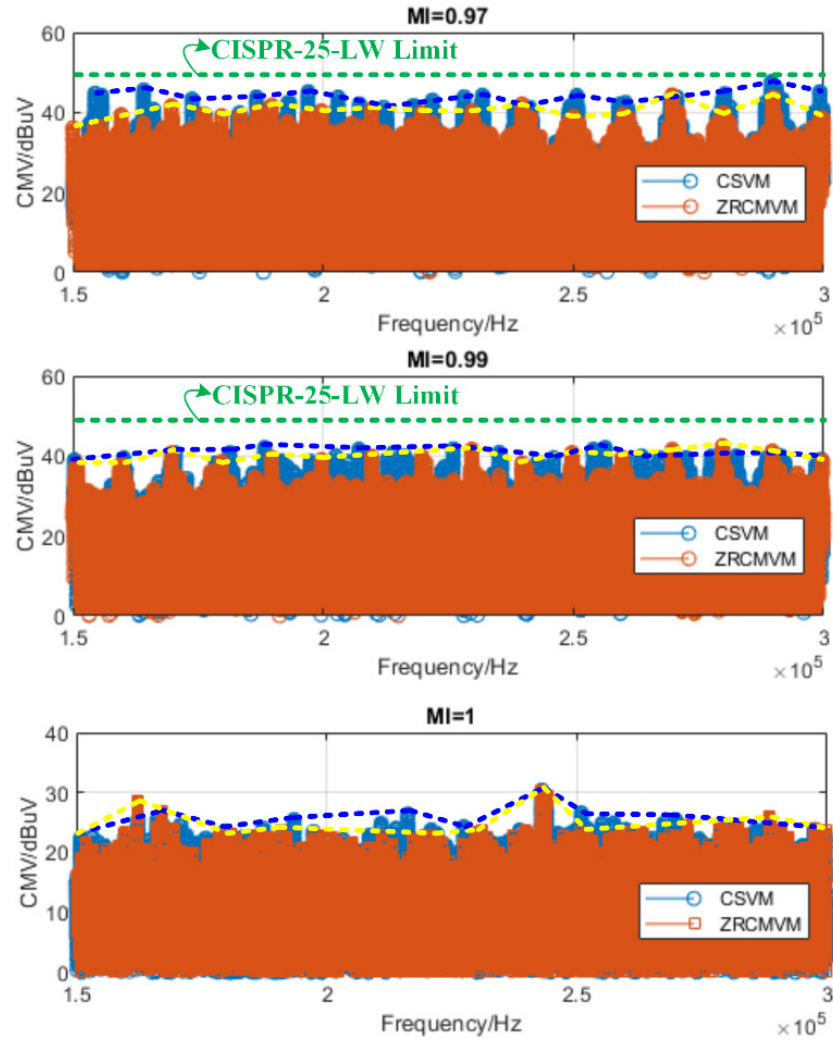


Figure 5.27: CMC spectrum comparison in the overmodulation range (mode-II).

range is attributed to the proposed ZRCMVM. For $MI=0.8$, the modulation aims at RCMV, and the maximum reduction is lowered to around 8 dBuV, still exhibiting ~60% CMC reduction.

In the overmodulation range, as the system approaches full modulation, the theoretical CM performance of both modulation schemes should gradually merge. The CM EMI spectrum of CSVM and ZRCMVM are approaching each other due to the reduced CMV of CSVM itself. At the end of overmodulation mode-I, where $MI=0.95$, the maximum reduction on the spectrum envelop at this point, is ~6 dBuV. From the obtained spectrum at $MI=1$, the envelopes for CSVM and ZRCMVM are nearly overlapped. Therefore, the EMI spectrum measurements confirm the ZRCMVM performance behavior through a full modulation span, which is modeled in the previous sections.

5.4.2 DM Current Ripple measurement

The measured phase current in different modulation ranges is shown in Figure 5.28 with an inductive load. The phase current quality in the linear range is secured by ZRCMVM, however, in the overmodulation range, the current starts to distort. In Section III, the differential impact of ZRCMVM is investigated. It shows that even though ZRCMVM is based on pulse manipulation, the phase current ripple caused by ZRCMVM is not significantly larger than CSVM.

To further verify the differential-mode performance, the tested phase current ripple is captured through an RF current probe. As shown in Figure 5.29, the modulation index varies from 0.1 to 0.9, where the corresponding phase current RMS value increases from 4.75 A to 39 A. The phase current ripple of ZRCMVM is not larger than CSVM. The total

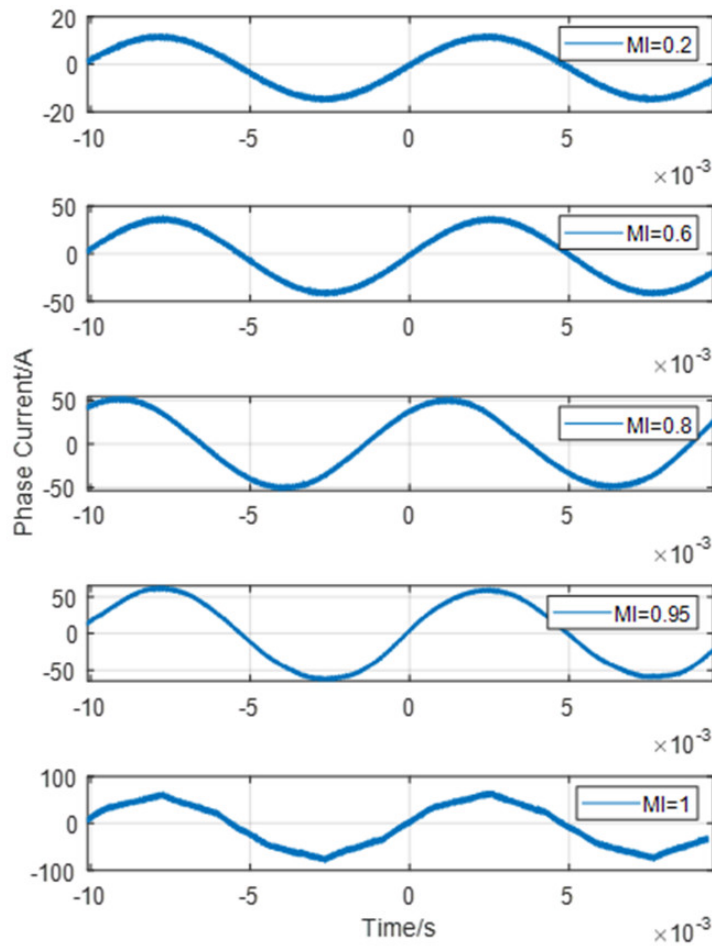


Figure 5.28: Phase current waveforms.

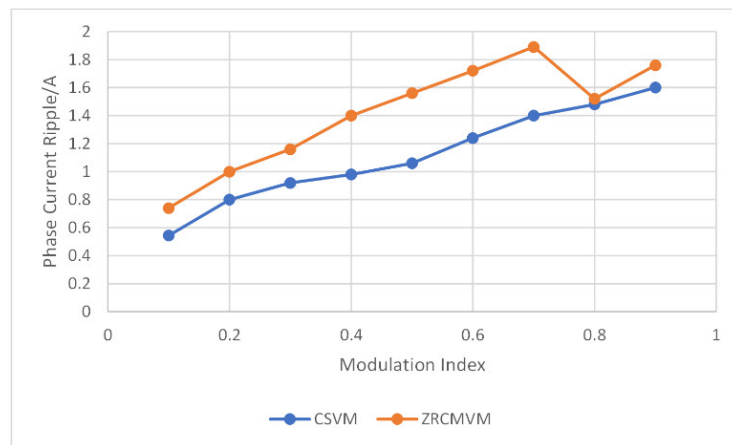


Figure 5.29: Phase current ripple measurement.

ripple to phase current RMS ratio increment is less than 1.7%. Such performance not only prevents worsening phase current THD but also avoids loud acoustic noise, especially when the switching frequency is below 20 kHz.

5.5 Summary

This chapter proposed a CMV elimination/reduction modulation scheme that covers the full modulation range. In the low/medium modulation range ($0 < MI \leq 0.785$), the modulation is CSPWM based, where the objective is to fully eliminate the CMV. In the high/overmodulation range ($0.785 < MI \leq 1$) when SVPWM is adopted, due to the need for 3rd order harmonic injection, zero CMV is hard to realize. The proposed modulation strategy, however, can still reduce the CMV. The overall CMV is drastically reduced from the perspective of full modulation operation. In summary, the proposed ZRCMVM has the following advantages:

- (1) The modulation is based on basic PWM methods, only adding additional pulse manipulation processes. The overall implementation difficulty is low.
- (2) Nearly 80% of operation points can work under zero CMV conditions, which covers most realistic scenarios. The rest of the operation points can still see significant CMV reduction.
- (3) Compared with some reduced-CMV modulation methods, e.g., AZSPWM, the phase current ripple caused by the pulse manipulation in ZRCMVM is much smaller, especially in the high/overmodulation range. Though the 3rd order harmonic injection is applied when $MI > 0.785$, due to the high modulation

index, the ripple has a negligible difference compared to CSVM. This will benefit the current quality and lower acoustic noise.

- (4) The total switching loss of ZRCMVM is the same as CSVM as no extra switching action is introduced. Compared to some methods adding extra switching actions to reduce CMV, the efficiency using the proposed ZRCMVM will not be reduced.

With the Xilinx System Generator Platform, the simulated modulation algorithm is easily converted to the FPGA code. The experimental results prove the effectiveness of ZRCMVM on the CMV reduction, without sacrificing the DM performance in the full modulation range. The pulse shifting/splitting method is not restricted to any specific modulation scheme. For various 3rd order harmonic injections (triangle wave is injected in this paper for CSVM), the same approach might also apply.

Chapter 6 THREE-LEVEL INVERTER COMMON-MODE VOLTAGE MODELING AND REDUCTION

As the 2-level structure has been investigated comprehensively, this chapter concentrates on the 3-level structure CMV reduction.

Recently, high voltage batteries such as 800V instead of 400V became popular in EVs because of the benefit of fast charging, longer mileage, and lower loss. This requires either the device to have high voltage blocking capability, or the inverter to be multiple levels, such as 3-level neutral point clamped (NPC) inverter and active neutral point clamped (ANPC) inverter. Considering the cost and manufacture issue, using lower voltage blocking devices in the multilevel inverter is more preferred, which not only lowers the device voltage stress but also enhances the output power quality because of the increased voltage levels.

The CM performance of a 3-level inverter will be discussed in this chapter. In addition, the applicability of the proposed analytical CMV model to a 3-level inverter will be studied.

The structure of this chapter is organized as follows. Section 1 summarizes the 3-level modulation methods. Section 2 builds the DFI model for each modulation method for the CMV analytical characterization, including conventional space vector modulation, and two more 3-level modulation schemes that more preferred in the 3-level system. In Section 3, the simulation result is presented to validate the 3-level modulation CMV modeling, as well as investigating the DM impact that each modulation could bring to the system. Section 4 is the summary.

6.1 Three-level Active Neutral Point Clamped Inverter Modulation

Compared to a conventional two-level inverter, the three-level phase output voltage has 3 voltage levels ($0, +V_{dc}/2, -V_{dc}/2$). The 3-level ANPC inverter topology is shown in Figure 6.1. For each phase leg, there are 4 high-frequency switches ($S_{x1H}, S_{x1L}, S_{x3H}, S_{x3L}$, x represents phase a, b , or c) and 2 line-frequency switches (S_{x2H}, S_{x2L}). One conventional modulation method is to use the space vector modulation waveform to compare with the level-shifted carriers to generate the high-frequency PWM. The modulation mechanism is shown in Figure 6.2. In the positive half cycle, the top switches S_{a1H} and S_{a3H} will be controlled by the Top Switch Carrier, while S_{a2H} stays on. All bottom switches (S_{a1L}, S_{a2L} , and S_{a3L}) are off. In the negative half cycle, the bottom switches S_{a1L} and S_{a3L} will be controlled by Bottom Switch Carrier while S_{a2L} remains on. The top switches (S_{a1H}, S_{a2H} , and S_{a3H}) then remain off. According to the switching profile of SVPWM in 3L-ANPC and following the general procedure of DFI analysis for CMV shown in Figure 4.9, the corresponding DFI integral bounds can be derived for the 3-level modulation schemes.

6.2 CMV Analytical Model for 3-Level Modulation

6.2.1 CSVM

As shown in Figure 6.3, there are 8 sections for each fundamental cycle. Especially, in sections 1, 2, 5, and 6, there are three integration areas. In sections 3, 4, 7, and 8, there is only one integration area (ignore the area where the pole voltage is 0). For instance, in section 1, the integration segments should be $(-\pi, 1-)$, $(1-, 1+)$, and $(1+, \pi)$. In section 3, the integration segments should be $(3-, 3+)$.

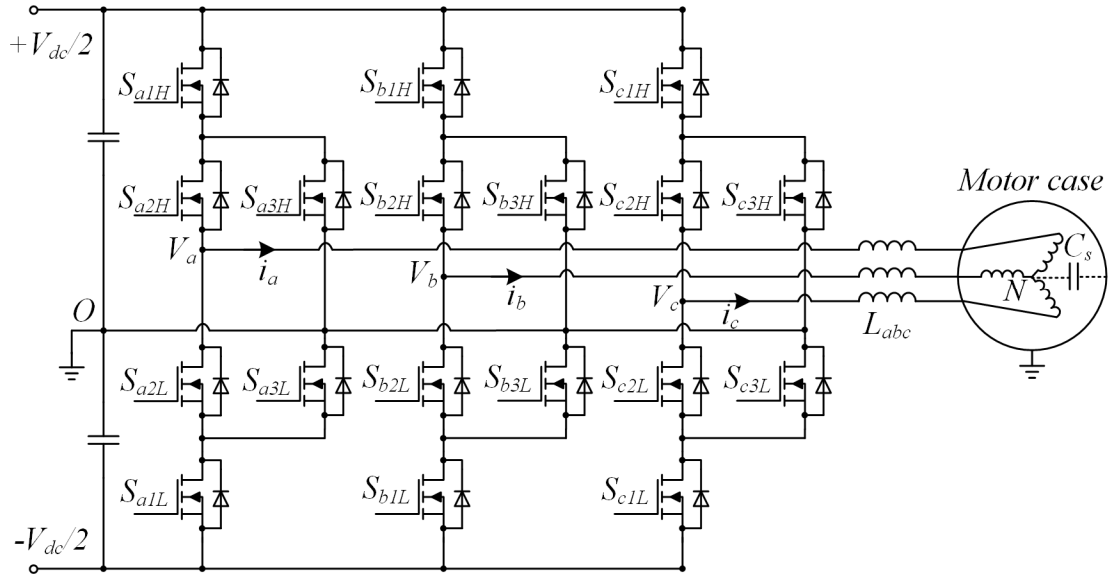


Figure 6.1: Three-phase three-level ANPC inverter motor drive system.

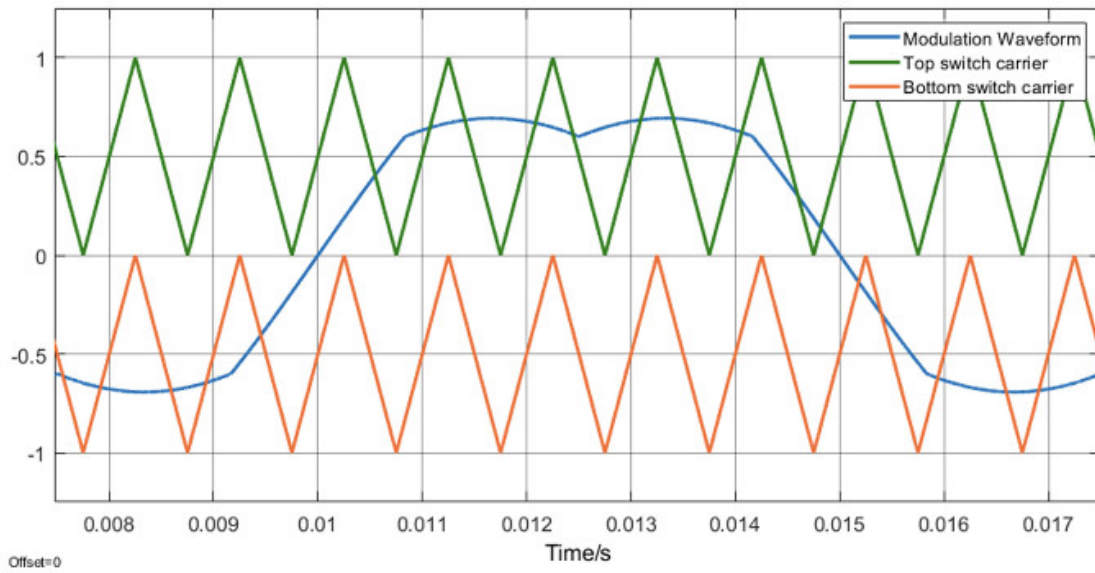


Figure 6.2: 3L-ANPC CSVM modulation waveform.

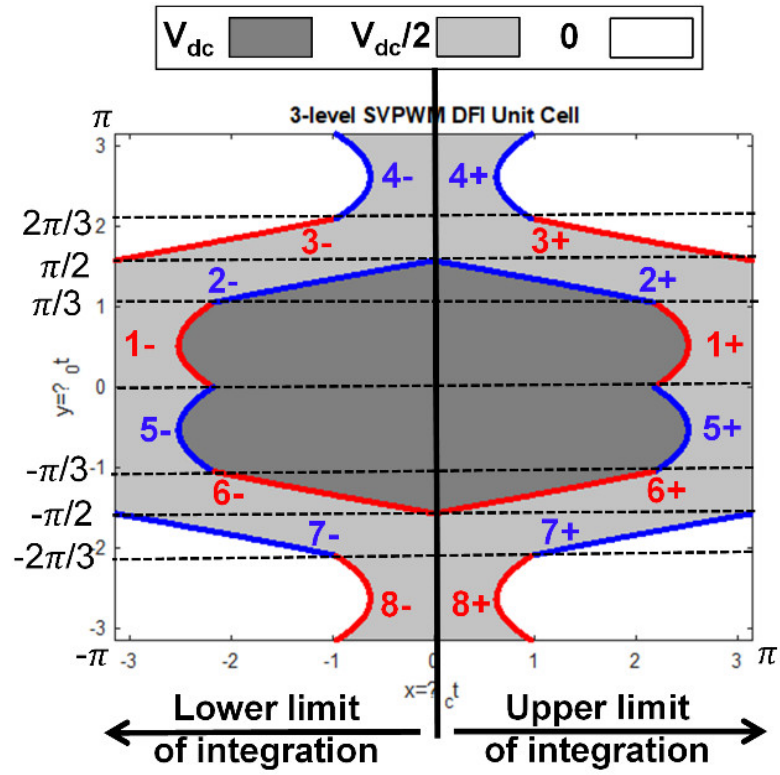


Figure 6.3: DFI integral bounds for SVPWM in a 3L-ANPC inverter.

$$\begin{aligned}
A_{mn} + jB_{mn} &= \frac{1}{2\pi} \int_{-\pi}^{\pi} \int_{\text{lower limit in sector } i}^{\text{upper limit in sector } i} V e^{j(mx+ny)} dx dy \\
&= \int_{-\pi}^{-\frac{2\pi}{3}} \int_{8-}^{8+} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy + \int_{-\frac{2\pi}{3}}^{-\frac{\pi}{2}} \int_{7-}^{7+} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy \\
&+ \int_{-\frac{\pi}{2}}^{-\frac{\pi}{3}} \int_{6-}^{6+} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy + \int_{-\frac{\pi}{3}}^{-\frac{\pi}{6}} \int_{6-}^{6+} V_{dc} e^{j(mx+ny)} dx dy \\
&+ \int_{-\frac{\pi}{6}}^{-\frac{\pi}{3}} \int_{6+}^{\pi} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy \\
&+ \int_{-\frac{\pi}{3}}^0 \int_{5-}^{5+} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy + \int_{-\frac{\pi}{3}}^0 \int_{5-}^{5+} V_{dc} e^{j(mx+ny)} dx dy \\
&+ \int_{-\frac{\pi}{3}}^0 \int_{5+}^{\pi} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy \\
&+ \int_0^{\frac{\pi}{3}} \int_{1-}^{1+} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy + \int_0^{\frac{\pi}{3}} \int_{1-}^{1+} V_{dc} e^{j(mx+ny)} dx dy \\
&+ \int_0^{\frac{\pi}{3}} \int_{1+}^{\pi} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy \\
&+ \int_{\frac{\pi}{3}}^{\frac{\pi}{2}} \int_{2-}^{2+} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy + \int_{\frac{\pi}{3}}^{\frac{\pi}{2}} \int_{2-}^{2+} V_{dc} e^{j(mx+ny)} dx dy \\
&+ \int_{\frac{\pi}{3}}^{\frac{\pi}{2}} \int_{2+}^{\pi} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy \\
&+ \int_{\frac{\pi}{2}}^{\frac{2\pi}{3}} \int_{3-}^{3+} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy + \int_{\frac{\pi}{2}}^{\frac{2\pi}{3}} \int_{4-}^{4+} \frac{V_{dc}}{2} e^{j(mx+ny)} dx dy
\end{aligned} \tag{6.1}$$

The DFI model for CSVM in a 3L-ANPC is then generated from (6.1). Using (4.5)~(4.6) and substituting different values for m and n , the carrier harmonics and sideband components of the CMV can be calculated and compared to the simulation at $f_0=100$ Hz, $f_s=10$ kHz, 200V DC bus voltage, and 0.8 modulation index. As shown in Figure 6.4, the calculated carrier harmonics and the sideband component of both phase voltage and CMV are very close to the simulation. Here only the $f_s \pm 15f_0$ sideband harmonics around f_s are plotted. Therefore, the proposed analytical approach for CMV can be extended to multi-level scenarios.

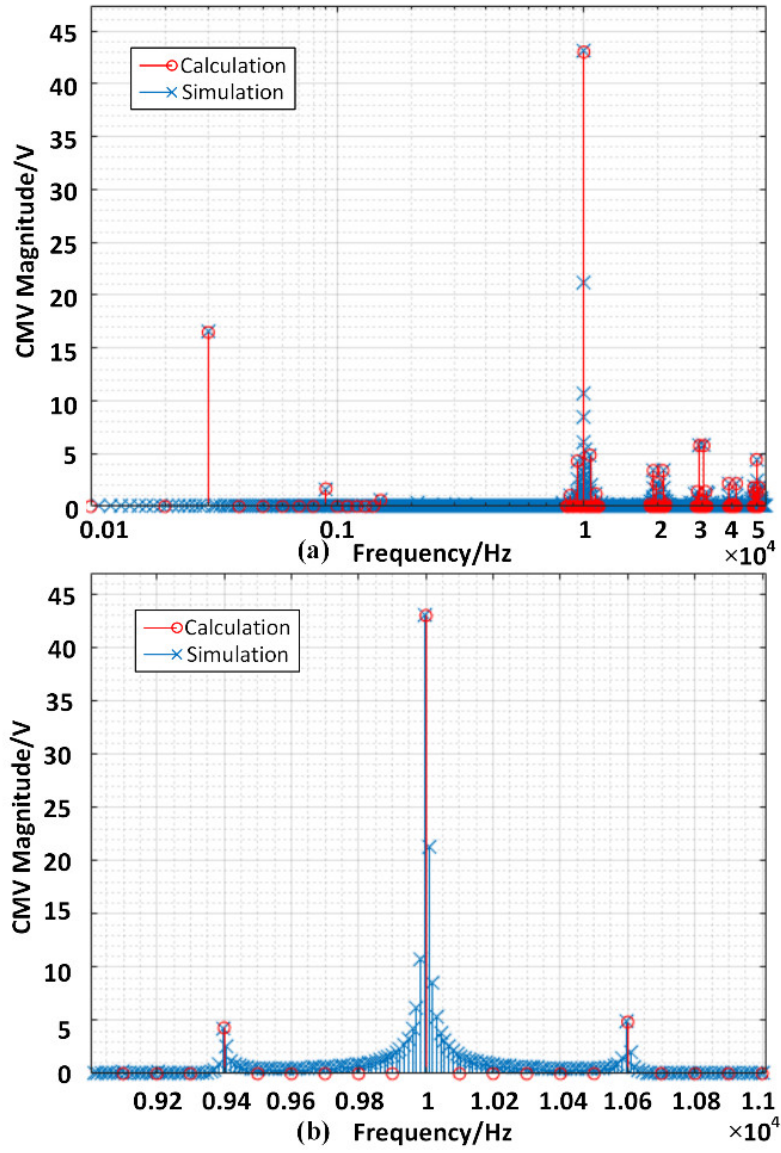


Figure 6.4: Comparison of DFI result and simulation for 3L-ANPC inverter.

(a) Wide frequency range, (b) Zoomed-in view @ f_s .

6.2.2 NTSVM

Direct CSVM modulation does not consider the modulation from the vector assignment point of view. However, determining the switching states, and the corresponding vector duration time is critical to synthesize the reference voltage vector [145]. As the total switching states count of a multilevel converter shows a cubic increase with the converter levels, the computational effort for the CSVM overwhelms quickly and is not preferred to be used for multilevel converters. Instead, using the nearest three vectors to synthesize the reference voltage is arguably the best approach as it saves the computation resources and forms precise vector decomposition. This modulation scheme is called nearest three vector modulation (NTSVM).

The NTSVM mechanism is illustrated in Figure 6.5. Where the reference vector (blue) locates in sector-1 and subsector-2, the NTSVM requires to use the vectors on the three vertices of the subsector-2 triangle. Different from CSVM, which has a simplified modulation waveform that could be directly extended from a 2-level inverter, the modulation waveform of NTSVM is very complicated because of the subsector alternation. Depending on the modulation index, the modulation waveform shows a very different profile. The DFI bounds could be derived and plotted as shown in Figure 6.6. Following the same steps that were applied in section 6.2.1, the analytical CMV spectrum vs the simulation result could be obtained. Figure 6.7 shows the comparison given DC bus voltage = 800 V, $MI=0.8$, $f_s=10$ kHz and $f_0=100$ Hz. In Figure 6.8, the peak CMV at the switching frequency point at different modulation indices is estimated and compared with the simulation. The result shows very accurate CMV prediction performance for NTSVM.

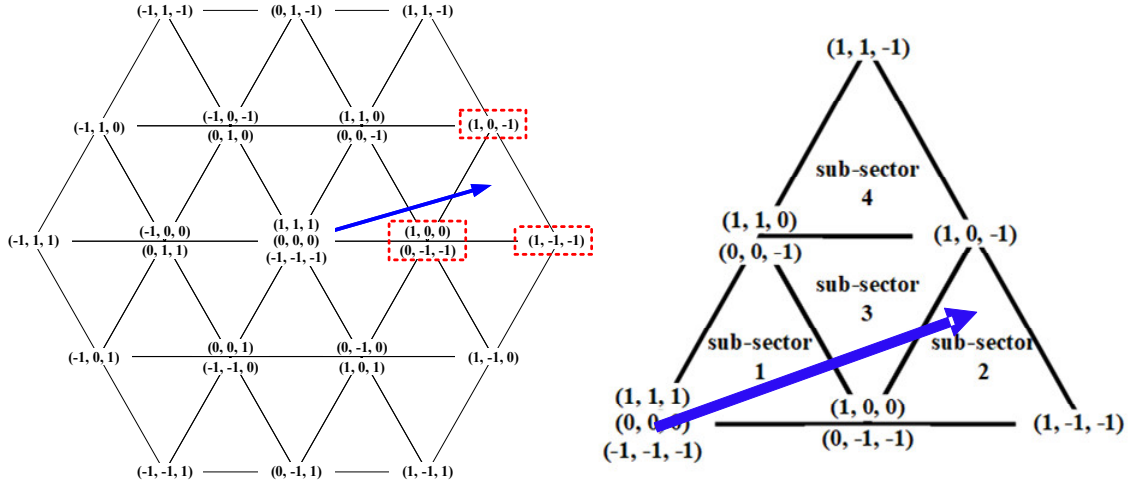


Figure 6.5: NTSVM vector plane and reference synthesis.

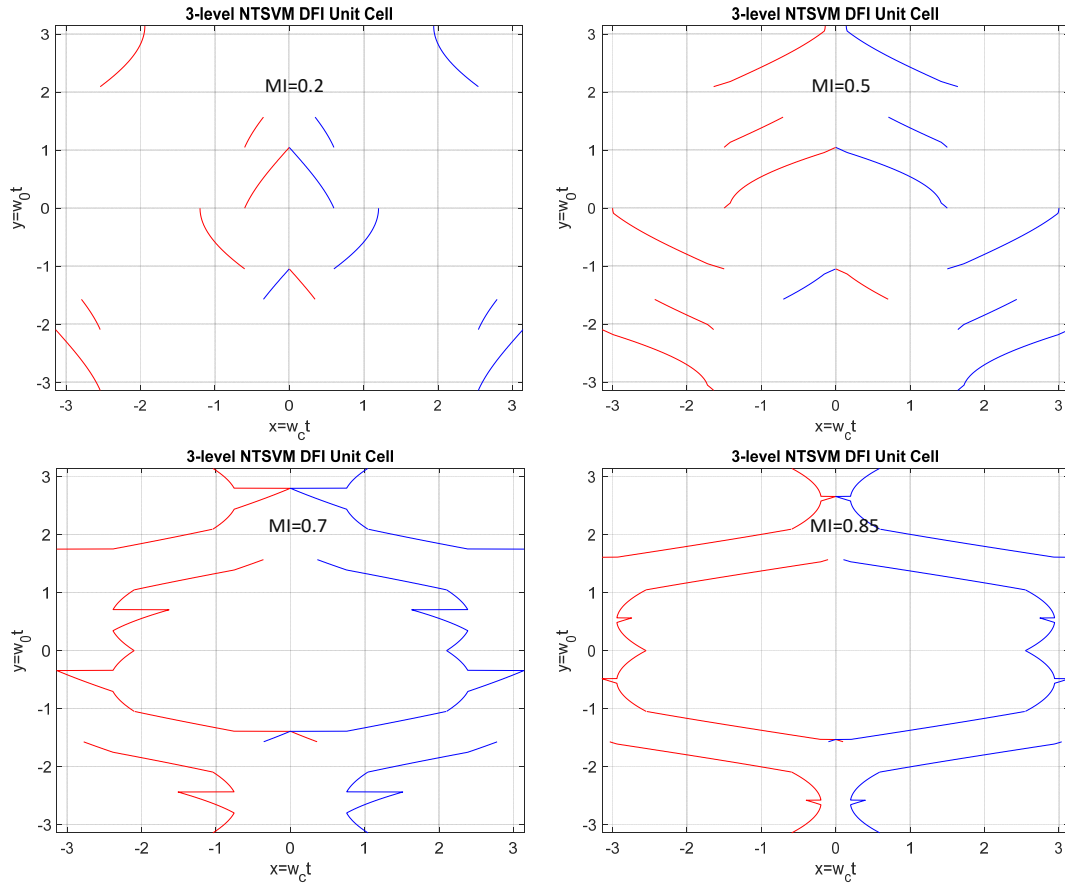


Figure 6.6: DFI integral bounds for NTSVM in a 3L-ANPC inverter.

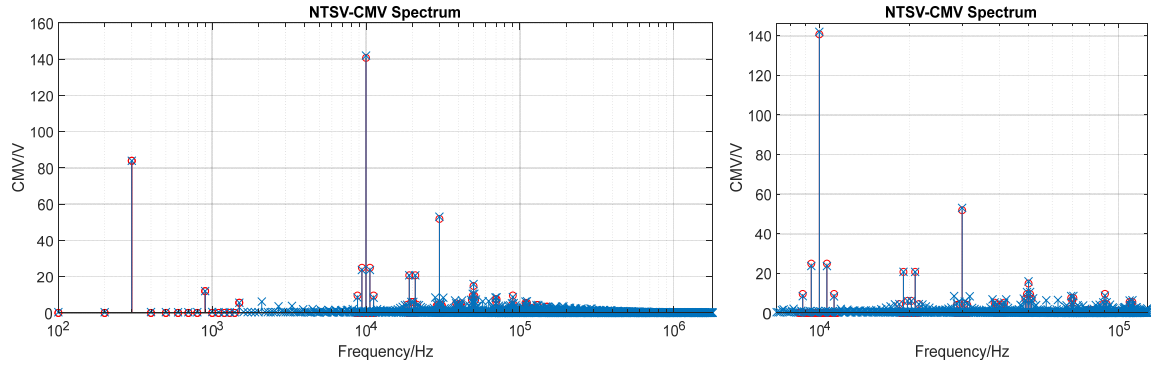


Figure 6.7: Comparison of DFI result and simulation for 3L-NTSVM.

Left: Wide frequency range, Right: Zoomed-in around f_s .

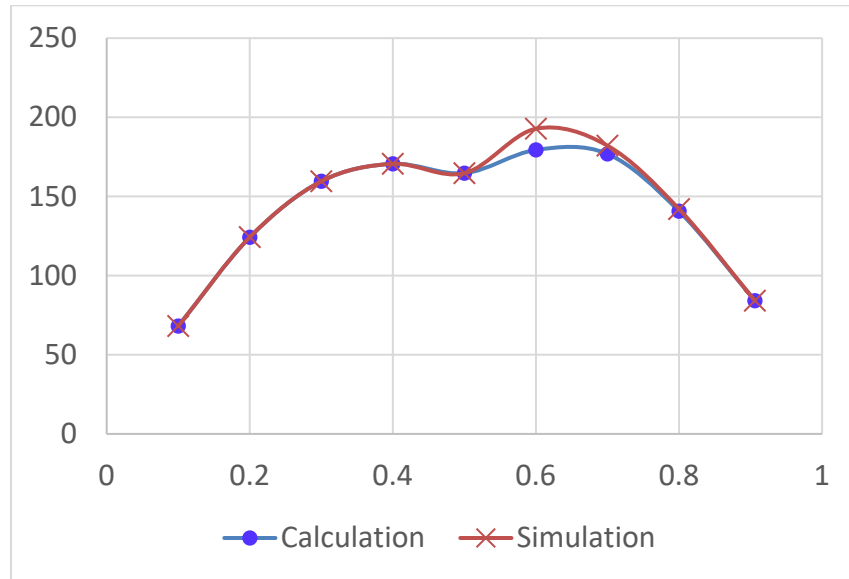


Figure 6.8: Comparison of DFI result and simulation for 3L-NTSVM CMV peak @ f_s .

6.2.3 RCMVM

NTSVM alternates the space vectors based on the minimum switching action principle to save the switching loss. However, some of the vectors will result in CMV higher than $V_{dc}/6$. Therefore, by avoiding using the 8 voltage vectors that generate $V_{dc}/6$ CMV, the system CMV could be constrained within $V_{dc}/6$. These 8 vectors are marked in Figure 6.9. Other than that, the vector synthesis mechanism is the same as NTSVM. Due to the forced forbidden of some vectors, which means the 8 redundant switching states will not be used during modulation, the minimum switching action mechanism could not be realized. For example, in NTSVM sub-sector 2, the vector sequence minimum switching action would be (1, 0, 0), (1, 0, -1), (1, -1, -1) (0, -1, -1). However, in RCMVM sub-sector 2, the (0, -1, -1) vector is banned because it generates $V_{dc}/2$ CMV, the switching sequence becomes (1, 0, 0), (1, 0, -1), (1, -1, -1) (1, 0, 0). The last state transition includes an extra switching. Therefore, compared with NTSVM, the switching loss of RCMVM will be increased.

Similar to NTSVM, the modulation waveform of RCMVM is also complicated compared with CSVM. The DFI bounds could be derived and plotted as shown in Figure 6.10. The analytical CMV spectrum vs the simulation result could be obtained through the CMV spectrum estimation model.

Figure 6.11 shows the comparison given DC bus voltage = 800 V, $MI=0.8$, $f_s=10$ kHz and $f_0=100$ Hz. In Figure 6.12, the peak CMV at the switching frequency point at different modulation indices is estimated and compared with the simulation. The result shows very accurate CMV prediction performance for RCMVM.

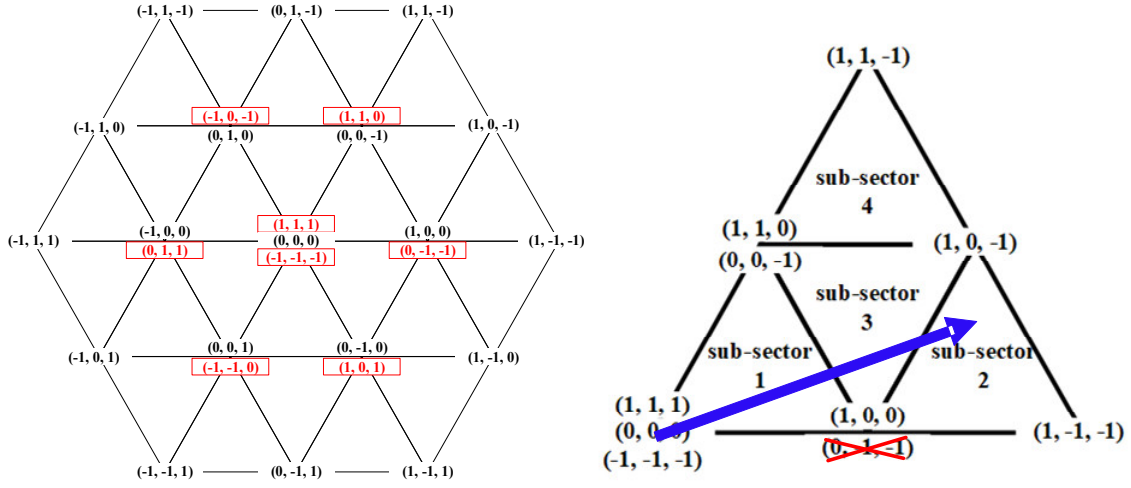


Figure 6.9: NTSVM vector plane and reference synthesis.

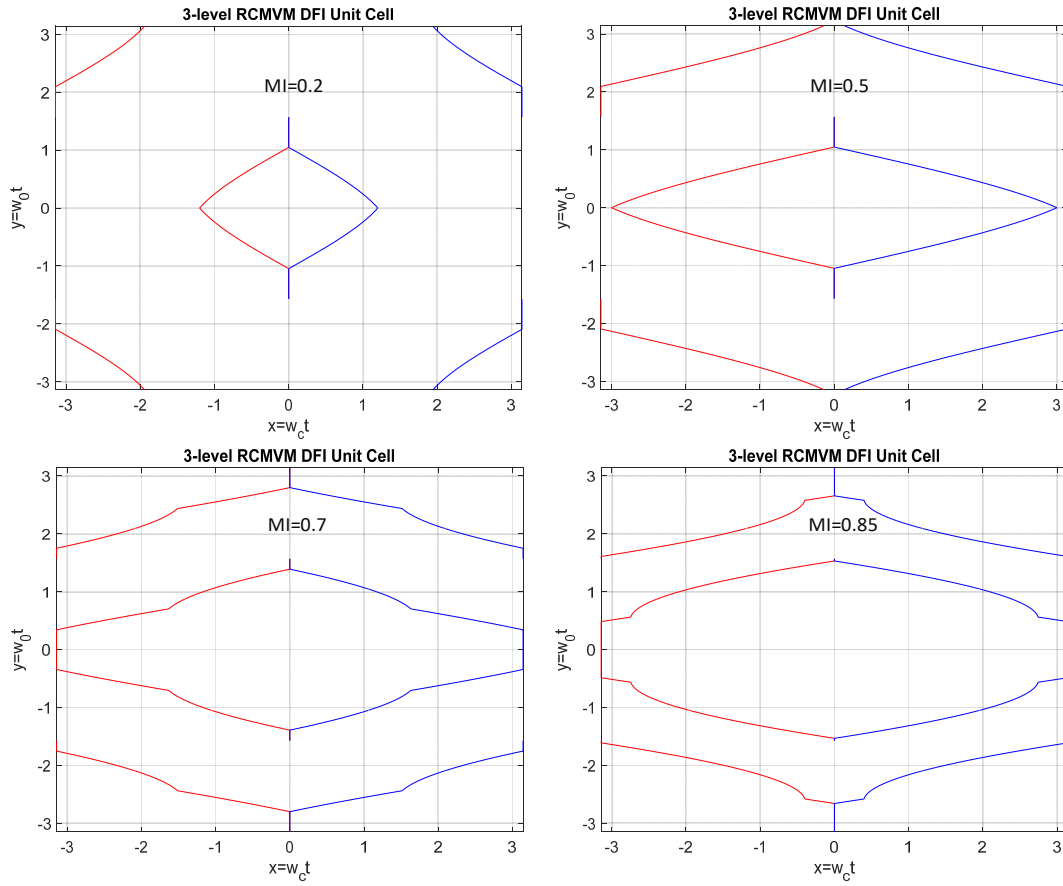


Figure 6.10: DFI integral bounds for RCMVM in a 3L-ANPC inverter.

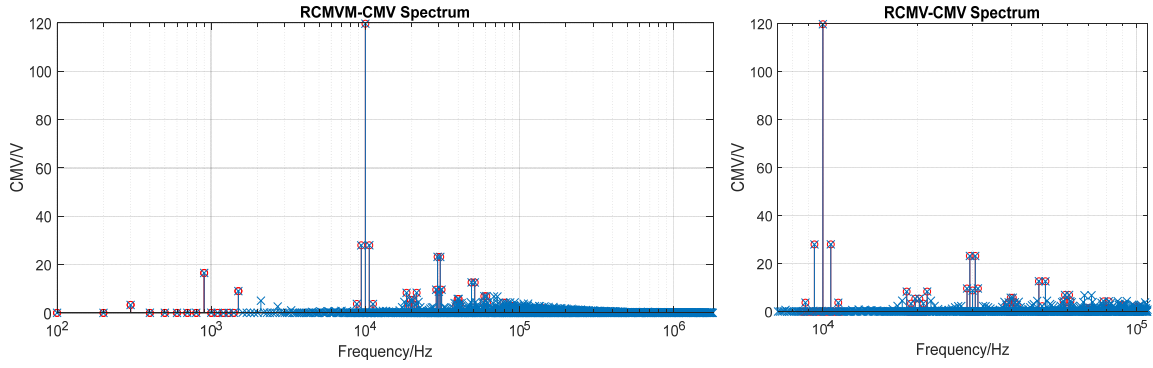


Figure 6.11: Comparison of DFI result and simulation for 3L-RCMVM.

Left: Wide frequency range, Right: Zoomed-in around f_s .

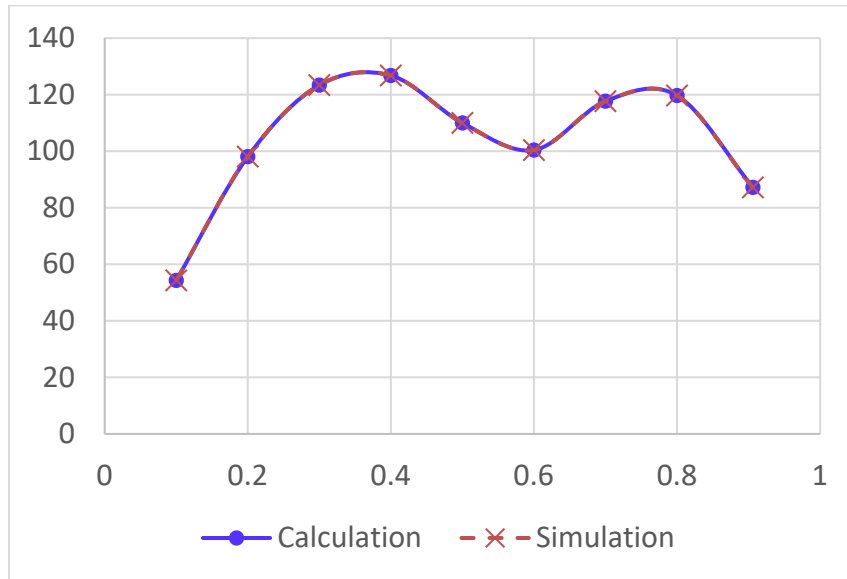


Figure 6.12: Comparison of DFI result and simulation for 3L-RCMVM CMV peak @ f_s .

6.3 CMV Performance Evaluation

Due to the smaller voltage step change in the 3-level inverter, the 3-level modulation generates a smaller CMV profile compared with conventional 2-level modulation.

The simulation comparison is shown in Figure 6.13. Given 800 V DC-link voltage, with 2L-CSVM, the peak CMV could reach $V_{dc}/2$. However, the 3L-NTSVM could reduce the CMV peak to $V_{dc}/3$, while 3L-RCMVM could further limit the CMV to $V_{dc}/6$. Therefore, the 3-level system naturally has smaller CMV in terms of the CMV time-domain peak value. The zoomed-in view shows the CMV pattern within a switching period. The 2-level CSVM CMV is a 4-level profile, 3-level NTSVM shows 3-level waveform with half of the fundamental period clamped to $V_{dc}/3$ and the rest half clamped to $-V_{dc}/3$. RCMVM result in a 3-level profile as well but the peak is restricted to $\pm V_{dc}/6$.

Figure 6.14 shows the corresponding CMV spectrum. In the LW/MW frequency range (150 kHz to 1.8 MHz, defined in the CISPR-25 EMI standard), the RCMVM CMV reduction is significant. NTSVM helps reduce the CMV by 8.43 dB μ V and RCMVM further lowers the CMV by 10.82 dB μ V.

The above comparison is compared with 2L-CSVM. When compared with 3L-CSVM, the CMV reduction performance is summarized and listed in Figure 6.15. In a complete linearity modulation range, RCMVM shows the best CMV reduction performance in terms of the peak CM components in the LW spectrum. In the MW range, the reduction performance is comparable to the NTSVM, but still much better than the CSVM.

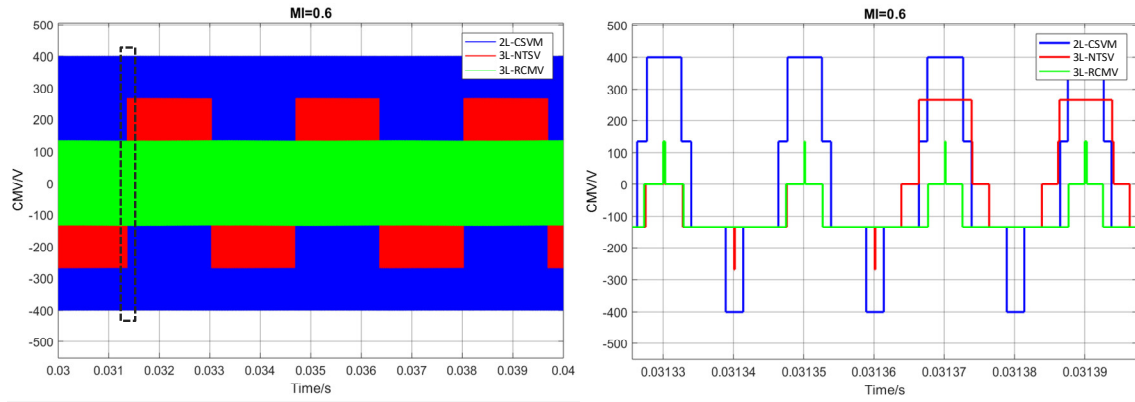


Figure 6.13: CMV profile comparison.

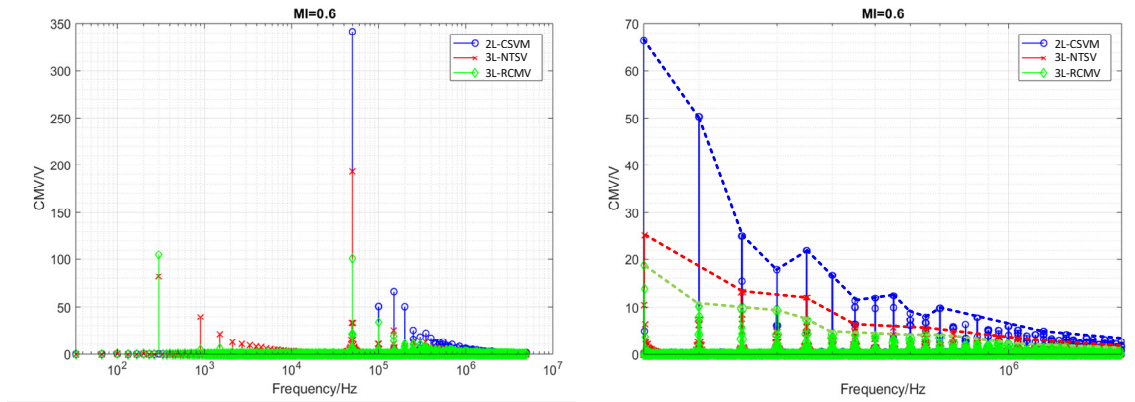


Figure 6.14: CMV spectrum comparison.

Left: Wide frequency range, Right: LW/MW frequency range.

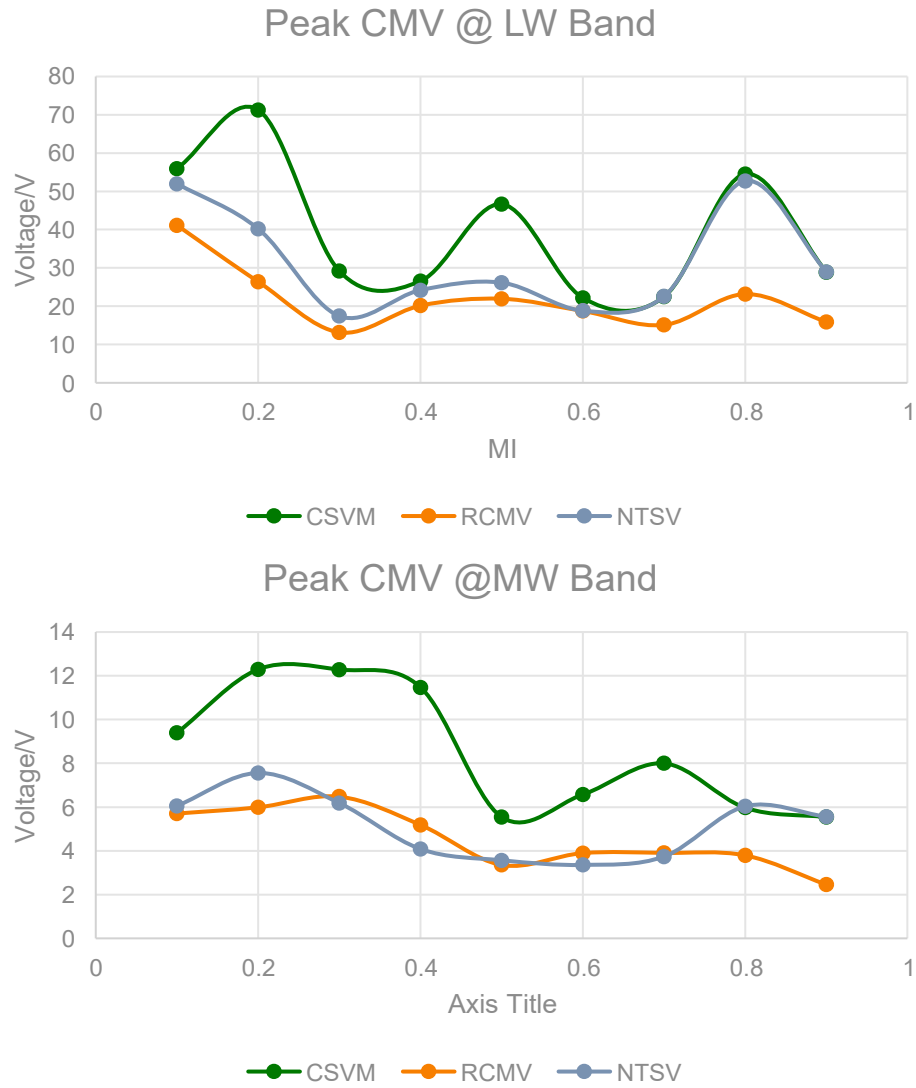


Figure 6.15: Peak CMV comparison in LW/WM frequency range.

(top) LW band, (bottom) MW band.

Similar to the previous chapters, when considering the CM performance of a certain modulation method, the corresponding DM performance also needs to be investigated. Figure 6.16 collects the DM performance of 3-level CSVM, NTSVM, and RCMVM.

According to the DM performance comparison, though RCMVM provides the best CMV reduction, it introduces higher output current ripple and THD. While NTSVM and CSVM show little difference. Compared with the 2-level inverter, the three-level inverter has one extra DM performance factor, the neutral point shift. This is defined as the voltage difference between the voltage across the top and bottom capacitors. Due to the selective mechanism of RCMVM, the neutral point balancing performance will be weakened. CSVM shows the most stable neutral point voltage.

6.4 Summary

The GaN-based multi-level topology could benefit the EV application under a high-voltage scenario from both power density and efficiency aspects. This chapter first successfully extended the proposed CMV prediction model to the 3-level inverter. With NTSVM and RCMVM, though the modulation waveforms are complex, the suggested CMV prediction procedure shown in Figure 4.10 still applies. The computation result matches the simulation result very accurately. In addition, the CM and DM performance of a 3-level inverter with different modulation schemes are investigated and compared. The CMV reduction performance of RCMVM is not considerably better than NTSVM but has worse DM performance.

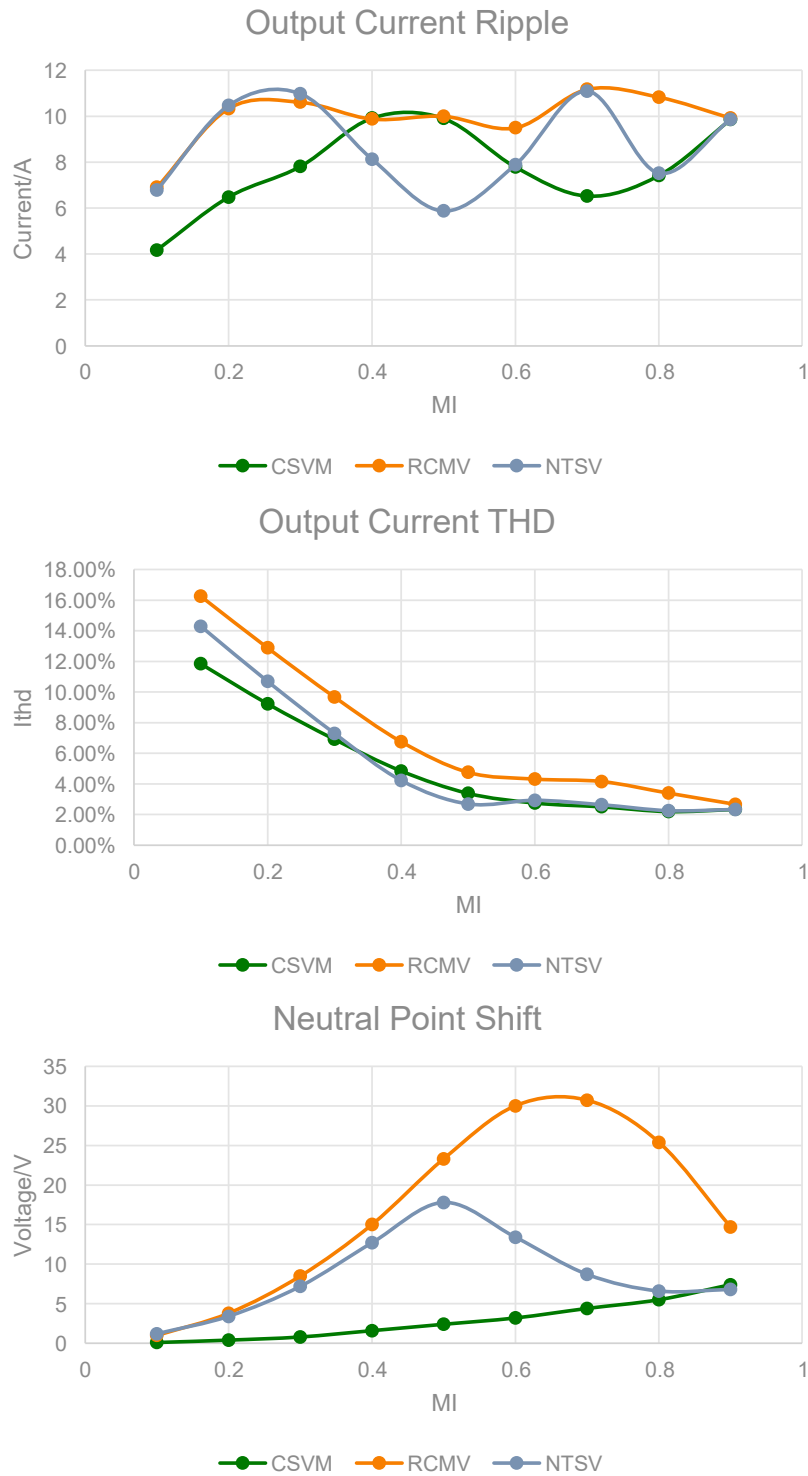


Figure 6.16: DM performance comparison.

Top: Output current ripple, Middle: Output current THD, Bottom: Neutral point shift.

Chapter 7 CONCLUSION AND FUTURE WORK

Based on the work presented in chapters 1-6, the conclusions of this dissertation are summarized. The potential future research is also discussed in this chapter.

7.1 Conclusion

7.1.1 Summary of The Work

In this dissertation, both inverters on the EV charger side and motor drive side are studied. Each side has a different issue to resolve.

On the charger side, a control strategy for a three-phase four-wire topology is proposed to deal with the V2L application. With the additional fourth leg, the voltages on the split DC-link capacitors are properly balanced under unbalanced load. A virtual resistance is introduced to damp the harmonics under V2L mode at the resonant point, the system reliability is significantly strengthened, and power quality is secured.

On the motor drive side, methods of characterizing the CMV for three-phase inverters are proposed based on DFI because the modulation not only causes CMV but also affects the system DM performance. An analytical model of output current ripple is also built for a comprehensive evaluation of various PWM control techniques. During the experimental validation through FPGA, the control bandwidth impact on the system CM and DM performance is also investigated. A hybrid PWM concept is proposed to actively switch the modulation method so that the system could always pick the PWM with the ideal performance among others at specific operating conditions. The on-chip CMC prediction result shows good accuracy and is a solid preparation for future code integration.

In addition, based on the six-phase motor drive system, a CMV reduction modulation method is proposed that covers the full modulation span. In the low/medium modulation range ($0 < MI \leq 0.785$), the proposed modulation could eliminate the CMV. In the high/overmodulation range ($0.785 < MI \leq 1$), the proposed modulation could reduce the CMV, while the DM performance is not significantly deteriorated.

Considering the high voltage trend in EV applications, multilevel converters could be introduced for the high voltage designs. Various 3-level modulation methods are investigated. The proposed CMV analytical tool is successfully extended to the 3-level inverter for the CM spectrum prediction. Based on that, both CM and DM performance are compared and validated through a 50 kW/ 800 V GaN-based 3-level inverter.

7.1.2 Contributions

7.1.2.1 Contributions of The Work

The contributions of this work are summarized as follows:

- (1) A neutral point voltage control method is proposed to balance the split DC-link capacitor voltages under load fluctuation.
- (2) A virtual resistance harmonic filter is modeled and applied to suppress the load current harmonics under unbalanced load. A 10 kW SiC-based bidirectional onboard charger with V2L function is delivered.
- (3) An analytical model of CMV regarding various modulation methods is proposed for quantifying CM performance, as well as the DM current ripple prediction model for comprehensive modulation scheme performance

evaluation. A 30 kW SiC-based 3-phase 2-level inverter for the 3-phase motor drive is delivered.

- (4) A CMV elimination/reduction modulation scheme is proposed based on the six-phase motor drive system, which realizes full modulation span CMV reduction, including overmodulation range. Two 100 kW SiC-based 3-phase 2-level inverters for the 6-phase motor drive were built and tested.
- (5) The CMV analytical model is successfully extended to the 3-level system. The model is validated and compared the performance of different 3-level modulation schemes through both CM and DM aspects. A 50 kW GaN-based 3-phase 3-level inverter for the high voltage motor drive is built and tested.

7.1.2.2 Publication List

- (1) Yang Huang, Jared Walden, Ximu Zhang, Yu Yan, Hua Bai, Fanning Jin, and Bing Cheng. "A Novel Zero/Reduced Common-mode Voltage Modulation Scheme for A Dual three-phase Motor Drive System in Full Modulation Span." *IEEE Transactions on Power Electronics* 37, no. 6 (2022): 6765 - 6779.
- (2) Yang Huang, Jared Walden, Andrew Foote, Hua Bai, Dingguo Lu, Fanning Jin, and Bing Cheng. "Analytical characterization of CM and DM performance of three-phase voltage-source inverters under various PWM patterns." *IEEE Transactions on Power Electronics* 36, no. 4 (2020): 4091-4104.
- (3) Yang Huang, Ximu Zhang, Jared Walden, Hua Bai, Fanning Jin, Xiaodong Shi, and Bing Cheng. "A Novel SPWM-based Common-mode Voltage elimination Modulation Method for Dual Three-phase Motors." In *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 5105-5110. IEEE, 2021.

- (4) Yang Huang, Jared Walden, Hua Bai, Dingguo Lu, Fanning Jin, and Bing Cheng. "Using Double Fourier Series to Analytically Model Common-mode Voltage for Various Modulation Methods in Three-phase Voltage-source Inverters." In *2020 IEEE Transportation Electrification Conference & Expo (ITEC)*, pp. 671-676. IEEE, 2020.
- (5) Ximu Zhang, Yang Huang, Jared Walden, Hua Bai, Fanning Jin, Xiaodong Shi, and Bing Cheng. "Using Machine Learning Technology to Online Predict the Maximum Common Mode Current of Three-phase Motor Drive Inverter." In *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1373-1379. IEEE, 2021.
- (6) Yongsheng Fu, Yu Li, Yang Huang, Xi Lu, Ke Zou, Chingchi Chen, and Hua Bai. "Unbalanced load regulation based on virtual resistance of a three-phase four-wire inverter for EV vehicle-to-home applications." *IEEE Transactions on Transportation Electrification* 5, no. 1 (2018): 162-173.
- (7) Yongsheng Fu, Yu Li, Yang Huang, Hua Bai, Ke Zou, Xi Lu, and Chingchi Chen. "Design methodology of a three-phase four-wire EV charger operated at the autonomous mode." *IEEE Transactions on Transportation Electrification* 5, no. 4 (2019): 1169-1181.
- (8) Yongsheng Fu, Yang Huang, Hua Bai, Xi Lu, Ke Zou, and Chingchi Chen. "A High-efficiency SiC Three-Phase Four-Wire inverter with Virtual Resistor Control Strategy Running at V2H mode." In *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pp. 174-179. IEEE, 2018.

- (9) Yu Yan, Yang Huang, RuiRui Chen, and Hua Bai. "Building Common-Mode Analytical Model for Dual Active Bridge Incorporating with Different Modulation Strategies." *IEEE Transactions on Power Electronics* 36, no. 11 (2021): 12608-12619.
- (10) Yu Yan, Yang Huang, Liyan Zhu, Ruirui Chen, Hua Bai, and Fred Wang. "Transformer Current Spike Elimination for Dual Active Bridge Converter Considering Multiple-Phase-Shift Modulation." In *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 348-354. IEEE, 2022.
- (11) Hua Kevin Bai, Daniel Costinett, Leon M. Tolbert, Ruiyang Qin, Liyan Zhu, Ziwei Lia4ng, and Yang Huang. "Charging Electric Vehicle Batteries: Wired and Wireless Power Transfer: Exploring EV charging technologies." *IEEE Power Electronics Magazine* 9, no. 2 (2022): 14-29.
- (12) Kevin Bai, Yang Huang, and Ximu Zhang. "Hybrid PWM Control for EV Motor Drive Systems." *UK Patent: UTRF 21135 _MB 2021ID02353*
- (13) Kevin Bai, Yang Huang, and Ximu Zhang. "A Novel Zero Common-mode Voltage Modulation Scheme for Dual-three-phase Motor Drive." *UK Patent: UTRF 21136 _MB 2021ID02354*
- (14) Kevin Bai, Zhou Dong, Yang Huang, Fred Wang, and Ching-Hsiang Yang. "Flex PCB Bonded GaN Power Module for Inverter and Solid State Circuit Breaker." (*Patent in review*)
- (15) Kevin Bai, Helen Cui, Yang Huang, Niu Jia, and Fred Wang. "A Planar Common-Mode Choke with Round DC Bus Bars." (*Patent in review*)

7.2 Future Work

On the basis of the work presented in this dissertation, some recommended future work is discussed here.

(1) 3-level hardware development and test.

To validate the 3-level modulation performance, a water-cooled 50 kW rated GaN-based 3-level inverter is built. The GaN HEMTs are from GaN System, GS66516T (650 V, 60 A). 3 pieces are paralleled at each switching position. The switching frequency is set to 50 kHz which is controlled by the FPGA, and the DC-link voltage is at most 800 V for high voltage applications. The prototype is shown in Figure. 7.1. The inverter is a stacked system with the bottom board carrying the power devices and the top board for the DC-link capacitors and input/output interfaces. To verify the performance that is investigated in Chapter 6, the follow-up experiments are expected to perform on this prototype..

(2) Comprehensive CM/DM EMI filter design and optimization.

The average noise of the electromagnetic environment increases by about 10 dB every 10 to 20 years. The increase of environmental noise and electromagnetic noise year by year has a direct impact on the safe and reliable operation of vehicles. In order to improve the convenience and functionality of the in-vehicle system, the required electromagnetic components and the amount of bus data will also increase, and the electrical appliances will interfere and influence each other. The requirements of the various wireless communication systems such as in-vehicle remote control systems, Bluetooth, Wi-Fi, V2X, and millimeter waves face challenges in electromagnetic compatibility and information security. In such a condition, EMI filters are a must to be

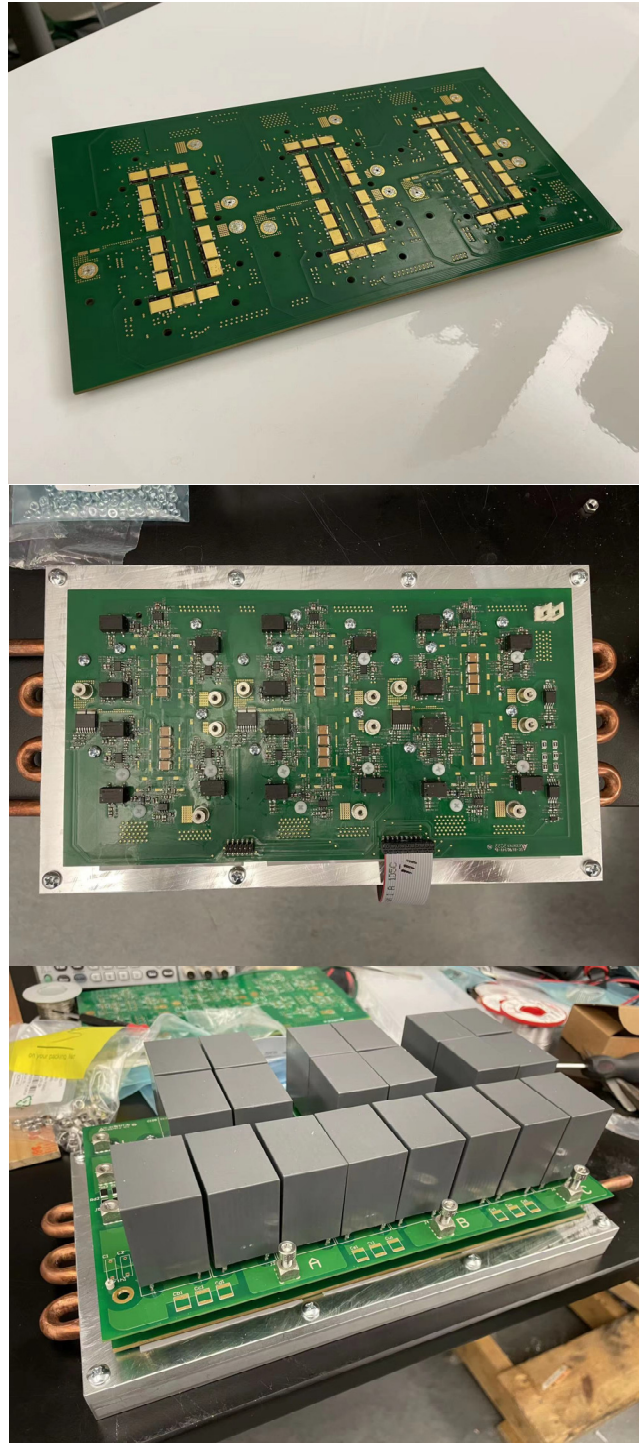


Figure 7.1: 3-level GaN-based ANPC inverter prototype.

Top: Bottom view, Middle: Top view, Bottom: Final assembly.

adopted in the motor drive system. According to the discussion in this dissertation, with the trend of WBG devices, the higher switching frequency can effectively reduce passive parts in the system, but also requires a bigger EMI filter to suppress the increased EMI noise, considering the past design is usually experience-based, the size redundancy will be significant. Though some software-based efforts, such as modulation techniques, can reduce the CMV without additional hardware, different modulations still have their unique impact on both CM and DM performance. Considering the high switching frequency and dead time effect, the high-frequency band EMI is a challenge. A proper filter modeling and design integration should be considered that takes all CM and DM impacts under different working conditions into consideration. The benefit of each modulation method should be quantified with the filter size for comparison and form a comprehensive filter design procedure.

(3) Motor bearing current monitoring and suppression.

As the source of the CM EMI in motor drive systems, several solutions have been proposed from the power converter's perspective, such as the inverter modulation schemes, and topologies. However, as important as the source, the conduction path has not drawn enough attention to be studied. It is the motor internal parasitics that provide low impedance CMC thereby leading to the CM EMI emission. However, suppressing CMC to meet the standards is not the only goal. As discussed in the previous chapter, one main issue that CMC brings to the system is the bearing damage. The bearing current is a part of CMC. CMV magnitude and conduction loop path are the necessary conditions for the current generation, but the loop for bearing current is different from a simple circuit, there is no relatively clear circuit, and it is difficult to measure the current. A comprehensive

bearing current modeling procedure will benefit the bearing current prediction algorithm to monitor the bearing status online and take action when hazardous happens. Further development of bearing current models that can aid in the reduction of these currents is needed

REFERENCE

- [1] C. IEA, "Global ev outlook 2020," URL: <https://www.iea.org/reports/global-ev-outlook-2020>, 2020.
- [2] U.S. Bureau of Transportation Statistics [Online]. Available: <https://www.bts.gov/data-spotlight/electric-vehicle-use-grows>.
- [3] K. Kurohane, T. Senjyu, A. Yona, N. Urasaki, T. Goya, and T. Funabashi, "A Hybrid Smart AC/DC Power System," *IEEE Transactions on Smart Grid*, vol. 1, no. 2, pp. 199-204, 2010.
- [4] L. Young-Joo, A. Khaligh, and A. Emadi, "Advanced Integrated Bidirectional AC/DC and DC/DC Converter for Plug-In Hybrid Electric Vehicles," *IEEE Transactions on Vehicular Technology*, vol. 58, no. 8, pp. 3970-3980, 2009.
- [5] C. V. R. Project. *Electric Vehicle Charging Overview* [Online]. Available: <https://cleanvehiclerebate.org/eng/ev/technology/fueling/electric>.
- [6] H. Lohse-Busch, "America's Electric Vehicle Charging Infrastructure in 2021," ed, 2021.
- [7] M. S. Shemami, M. S. Alam, and M. J. Asghar, "Load shedding mitigation through plug-in electric vehicle-to-home (V2H) system," in *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2017: IEEE, pp. 799-804.
- [8] W. Zhou, M. Li, H. Yin, and C. Ma, "An adaptive fuzzy logic based energy management strategy for electric vehicles," in *2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE)*, 2014: IEEE, pp. 1778-1783.

- [9] I. C. Kizilyalli, E. P. Carlson, D. W. Cunningham, J. S. Manser, Y. A. Xu, and A. Y. Liu, "Wide band-gap semiconductor based power electronics for energy efficiency," USDOE Advanced Research Projects Agency-Energy (ARPA-E), 2018.
- [10] onsemi. *Wide Bandgap Solutions of Vehicle Electrification* [Online]. Available: <https://www.onsemi.com/solutions-applications/segments/industrial-cloud-power/cloud-power/wide-bandgap>.
- [11] A. Meintz *et al.*, "Enabling fast charging—Vehicle considerations," *Journal of Power Sources*, vol. 367, pp. 216-227, 2017.
- [12] D. Ronanki, A. Kelkar, and S. S. Williamson, "Extreme fast charging technology—Prospects to enhance sustainable electric transportation," *Energies*, vol. 12, no. 19, p. 3721, 2019.
- [13] H. Tu, H. Feng, S. Srdic, and S. Lukic, "Extreme fast charging of electric vehicles: A technology overview," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 4, pp. 861-878, 2019.
- [14] R. Aboelsaud, A. Ibrahim, and A. G. Garganeev, "Review of three-phase inverters control for unbalanced load compensation," *International Journal of Power Electronics and Drive Systems*, vol. 10, no. 1, p. 242, 2019.
- [15] W. U. Tareen, S. Mekhilef, M. Seyedmahmoudian, and B. Horan, "Active power filter (APF) for mitigation of power quality issues in grid integration of wind and photovoltaic energy conversion system," *Renewable and Sustainable Energy Reviews*, vol. 70, pp. 635-655, 2017.

- [16] Z. Wang, Q. Wang, W. Yao, and J. Liu, "A series active power filter adopting hybrid control approach," *IEEE Transactions on Power Electronics*, vol. 16, no. 3, pp. 301-310, 2001.
- [17] D. Soto, C. Edrington, S. Balathandayuthapani, and S. Ryster, "Voltage balancing of islanded microgrids using a time-domain technique," *Electric power systems research*, vol. 84, no. 1, pp. 214-223, 2012.
- [18] P. K. Goel, B. Singh, S. S. Murthy, and N. Kishore, "Isolated wind-hydro hybrid system using cage generators and battery storage," *IEEE transactions on industrial electronics*, vol. 58, no. 4, pp. 1141-1153, 2009.
- [19] J. Liang, T. C. Green, C. Feng, and G. Weiss, "Increasing voltage utilization in split-link, four-wire inverters," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1562-1569, 2009.
- [20] M. K. Mishra, A. Joshi, and A. Ghosh, "Control schemes for equalization of capacitor voltages in neutral clamped shunt compensator," *IEEE Transactions on Power Delivery*, vol. 18, no. 2, pp. 538-544, 2003.
- [21] R. Zhang, D. Boroyevich, V. H. Prasad, H.-C. Mao, F. C. Lee, and S. Dubovsky, "A three-phase inverter with a neutral leg with space vector modulation," in *Proceedings of APEC 97-Applied Power Electronics Conference*, 1997, vol. 2: IEEE, pp. 857-863.
- [22] M. J. Hossain, F. H. M. Rafi, G. Town, and J. Lu, "Multifunctional three-phase four-leg PV-SVSI with dynamic capacity distribution method," *IEEE Transactions on Industrial Informatics*, vol. 14, no. 6, pp. 2507-2520, 2018.

- [23] R. Zhang, V. H. Prasad, D. Boroyevich, and F. C. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," *IEEE Transactions on power electronics*, vol. 17, no. 3, pp. 314-326, 2002.
- [24] Q.-C. Zhong, L. Hobson, and M. G. Jayne, "Classical control of the neutral point in 4-wire 3-phase DC-AC converters," *Electrical Power Quality and Utilisation. Journal*, vol. 11, no. 2, pp. 73-81, 2005.
- [25] C. Liu, J. Lai, F. Lee, D. Chen, and R. Zhang, "Common-mode components comparison for different SVM schemes in three-phase four-legged converter," in *Proceedings IPEMC 2000. Third International Power Electronics and Motion Control Conference (IEEE Cat. No. 00EX435)*, 2000, vol. 2: IEEE, pp. 633-638.
- [26] S. Bifaretti, A. Lidozzi, L. Solero, and F. Crescimbeni, "Comparison of modulation techniques for active split dc-bus three-phase four-leg inverters," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014: IEEE, pp. 5631-5638.
- [27] Z. Lin, X. Ruan, L. Jia, W. Zhao, H. Liu, and P. Rao, "Optimized design of the neutral inductor and filter inductors in three-phase four-wire inverter with split DC-link capacitors," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 247-262, 2018.
- [28] C. Hochgraf and R. H. Lasseter, "Statcom controls for operation with unbalanced voltages," *IEEE transactions on power delivery*, vol. 13, no. 2, pp. 538-544, 1998.
- [29] I. Vechiu, H. Camblong, G. Tapia, B. Dakyo, and O. Curea, "Control of four leg inverter for hybrid power system applications with unbalanced load," *Energy Conversion and Management*, vol. 48, no. 7, pp. 2119-2128, 2007.

- [30] I. Vechium, H. Camblong, G. Tapia, O. Curea, and B. Dakyo, "Modelling and control of four-wire voltage source inverter under unbalanced voltage condition for hybrid power system applications," in *2005 European Conference on Power Electronics and Applications*, 2005: IEEE, pp. 10 pp.-P. 10.
- [31] I. Vechiu, O. Curea, and H. Camblong, "Transient operation of a four-leg inverter for autonomous applications with unbalanced load," *IEEE Transactions on Power Electronics*, vol. 25, no. 2, pp. 399-407, 2009.
- [32] G.-H. Kim, C. Hwang, J.-H. Jeon, J.-B. Ahn, and E.-S. Kim, "A novel three-phase four-leg inverter based load unbalance compensator for stand-alone microgrid," *International Journal of Electrical Power & Energy Systems*, vol. 65, pp. 70-75, 2015.
- [33] L. Fazio, L. Peretti, and M. Zigliotto, "Repetitive control and virtual bleeder resistor for AC generator sets with harmonic-sensitive loads," in *2008 4th IET Conference on Power Electronics, Machines and Drives*, 2008: IET, pp. 144-148.
- [34] A. K. Adapa and V. John, "Virtual resistor based active damping of LC filter in standalone voltage source inverter," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018: IEEE, pp. 1834-1840.
- [35] M. Liserre, A. Dell'Aquila, and F. Blaabjerg, "Genetic algorithm-based design of the active damping for an LCL-filter three-phase active rectifier," *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 76-86, 2004.
- [36] Q. Zhao, F. Liang, and W. Li, "A new control scheme for LCL-type grid-connected inverter with a Notch filter," in *The 27th Chinese Control and Decision Conference (2015 CCDC)*, 2015: IEEE, pp. 4073-4077.

- [37] D. Yazdani, A. Bakhshai, and P. K. Jain, "A three-phase adaptive notch filter-based approach to harmonic/reactive current extraction and harmonic decomposition," *IEEE Transactions on Power electronics*, vol. 25, no. 4, pp. 914-923, 2009.
- [38] A. B. Shitole, H. M. Suryawanshi, S. Sathyan, and M. M. Renge, "Adaptive notch filter based synchronization technique for integration of distributed generation systems to utility grid," in *IECON 2014-40th Annual Conference of the IEEE Industrial Electronics Society*, 2014: IEEE, pp. 5457-5461.
- [39] R. S. R. Chilipi, N. Al Sayari, K. H. Al Hosani, and A. R. Beig, "Adaptive notch filter-based multipurpose control scheme for grid-interfaced three-phase four-wire DG inverter," *IEEE Transactions on Industry Applications*, vol. 53, no. 4, pp. 4015-4027, 2017.
- [40] J. Pinto *et al.*, "Bidirectional battery charger with grid-to-vehicle, vehicle-to-grid and vehicle-to-home technologies," in *IECON 2013-39th Annual Conference of the IEEE Industrial Electronics Society*, 2013: IEEE, pp. 5934-5939.
- [41] X. Zhou, G. Wang, S. Lukic, S. Bhattacharya, and A. Huang, "Multi-function bi-directional battery charger for plug-in hybrid electric vehicle application," in *2009 IEEE energy conversion Congress and exposition*, 2009: IEEE, pp. 3930-3936.
- [42] W. Cao, A. A. S. Bukhari, and L. Aarniovuori, "Review of electrical motor drives for electric vehicle applications," *Mehran University Research Journal of Engineering & Technology*, vol. 38, no. 3, pp. 525-540, 2019.
- [43] C. R. Harahap and T. Hanamoto, "Speed control of permanent magnet synchronous motor using FPGA for high frequency SiC MOSFET inverter," *Journal of Engineering Science and Technology (JESTEC)*, vol. 9, pp. 11-20, 2014.

- [44] D. Jiang, F. Wang, and J. Xue, "PWM impact on CM noise and AC CM choke for variable-speed motor drives," *IEEE Transactions on Industry Applications*, vol. 49, no. 2, pp. 963-972, 2013.
- [45] G. Skibinski, J. Pankau, R. Sladky, and J. Campbell, "Generation, control and regulation of EMI from AC drives," in *IAS'97. Conference Record of the 1997 IEEE Industry Applications Conference Thirty-Second IAS Annual Meeting*, 1997, vol. 2: IEEE, pp. 1571-1583.
- [46] S. Ogasawara, H. Ayano, and H. Akagi, "Measurement and reduction of EMI radiated by a PWM inverter-fed AC motor drive system," *IEEE Transactions on Industry Applications*, vol. 33, no. 4, pp. 1019-1026, 1997.
- [47] E. Zhong and T. A. Lipo, "Improvements in EMC performance of inverter-fed motor drives," *IEEE Transactions on Industry Applications*, vol. 31, no. 6, pp. 1247-1256, 1995.
- [48] N. Das and M. K. Kazimierczuk, "Applications of silicon carbide power devices in three-phase voltage-fed induction motor drives for electric vehicles," in *2007 Electrical Insulation Conference and Electrical Manufacturing Expo*, 2007: IEEE, pp. 278-285.
- [49] A. Muetze and C. R. Sullivan, "Simplified design of common-mode chokes for reduction of motor ground currents in inverter drives," *IEEE Transactions on Industry Applications*, vol. 47, no. 6, pp. 2570-2577, 2011.
- [50] H. Akagi and S. Tamura, "A passive EMI filter for eliminating both bearing current and ground leakage current from an inverter-driven motor," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1459-1469, 2006.

- [51] F.-Y. Shih, D. Y. Chen, Y.-P. Wu, and Y.-T. Chen, "A procedure for designing EMI filters for AC line applications," *IEEE transactions on power electronics*, vol. 11, no. 1, pp. 170-181, 1996.
- [52] A. Muetze, "Scaling issues for common-mode chokes to mitigate ground currents in inverter-based drive systems," *IEEE Transactions on Industry Applications*, vol. 45, no. 1, pp. 286-294, 2009.
- [53] H. Akagi and T. Doumoto, "A passive EMI filter for preventing high-frequency leakage current from flowing through the grounded inverter heat sink of an adjustable-speed motor drive system," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1215-1223, 2005.
- [54] P.-S. Chen and Y.-S. Lai, "Effective EMI filter design method for three-phase inverter based upon software noise separation," *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2797-2806, 2010.
- [55] S. Wang, Y. Y. Maillet, F. Wang, and D. Boroyevich, "Hybrid EMI filter design for common mode EMI suppression in a motor drive system," in *2008 IEEE Power Electronics Specialists Conference*, 2008: IEEE, pp. 181-187.
- [56] X. Zhang, D. Boroyevich, P. Mattavelli, J. Xue, and F. Wang, "EMI filter design and optimization for both AC and DC side in a DC-fed motor drive system," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013: IEEE, pp. 597-603.
- [57] X. Gong, I. Josifović, and J. A. Ferreira, "Modeling and reduction of conducted EMI of inverters with SiC JFETs on insulated metal substrate," *IEEE transactions on power electronics*, vol. 28, no. 7, pp. 3138-3146, 2012.

- [58] M. L. Heldwein and J. W. Kolar, "Impact of EMC filters on the power density of modern three-phase PWM converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1577-1588, 2009.
- [59] F. Luo *et al.*, "Analysis of CM volt-second influence on CM inductor saturation and design for input EMI filters in three-phase DC-fed motor drive systems," *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1905-1914, 2010.
- [60] Y.-C. Son and S.-K. Sul, "A new active common-mode EMI filter for PWM inverter," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1309-1314, 2003.
- [61] M. C. Di Piazza, G. Tinè, and G. Vitale, "An improved active common-mode voltage compensation device for induction motor drives," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 4, pp. 1823-1834, 2008.
- [62] S. Wang, Y. Y. Maillet, F. Wang, D. Boroyevich, and R. Burgos, "Investigation of hybrid EMI filters for common-mode EMI suppression in a motor drive system," *IEEE Transactions on Power Electronics*, vol. 25, no. 4, pp. 1034-1045, 2009.
- [63] R. S. Chokhawala, J. Catt, and B. R. Pelly, "Gate drive considerations for IGBT modules," *IEEE Transactions on industry applications*, vol. 31, no. 3, pp. 603-611, 1995.
- [64] E. Hertz, S. Busquets-Monge, D. Boroyevich, M. Arpilliere, and H. Boutillier, "Analysis of the tradeoffs between thermal behavior and EMI noise levels in a boost PFC circuit," in *Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No. 01CH37248)*, 2001, vol. 4: IEEE, pp. 2460-2465.

- [65] V. John, B.-S. Suh, and T. A. Lipo, "High-performance active gate drive for high-power IGBT's," *IEEE Transactions on Industry Applications*, vol. 35, no. 5, pp. 1108-1117, 1999.
- [66] S. Park and T. M. Jahns, "Flexible dv/dt and di/dt control method for insulated gate power switches," *IEEE Transactions on Industry Applications*, vol. 39, no. 3, pp. 657-664, 2003.
- [67] J. D. Kagerbauer and T. Jahns, "Development of an active dv/dt control algorithm for reducing inverter conducted EMI with minimal impact on switching losses," in *2007 IEEE Power Electronics Specialists Conference*, 2007: IEEE, pp. 894-900.
- [68] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation," *IEEE Transactions on Industry Applications*, vol. 47, no. 5, pp. 2154-2165, 2011.
- [69] J.-S. Lai, X. Huang, E. Pepa, S. Chen, and T. W. Nehl, "Inverter EMI modeling and simulation methodologies," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 3, pp. 736-744, 2006.
- [70] D. Han, S. Li, Y. Wu, W. Choi, and B. Sarlioglu, "Comparative analysis on conducted CM EMI emission of motor drives: WBG versus Si devices," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8353-8363, 2017.
- [71] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "Switching-behavior improvement of insulated gate-controlled devices," *IEEE Transactions on Power Electronics*, vol. 12, no. 4, pp. 645-653, 1997.

- [72] A. M. Hava and E. Ün, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1998-2008, 2010.
- [73] W. Hofmann and J. Zitzelsberger, "PWM-control methods for common mode voltage minimization-a survey," in *International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2006. SPEEDAM 2006.*, 2006: IEEE, pp. 1162-1167.
- [74] C.-C. Hou, C.-C. Shih, P.-T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE transactions on Power Electronics*, vol. 28, no. 4, pp. 1971-1979, 2012.
- [75] J. Shang, Y. W. Li, N. R. Zargari, and Z. Cheng, "PWM strategies for common-mode voltage reduction in current source drives," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5431-5445, 2013.
- [76] A. M. Hava and E. Ün, "Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 241-252, 2009.
- [77] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE transactions on industry applications*, vol. 35, no. 2, pp. 469-476, 1999.
- [78] Y.-S. Lai, P.-S. Chen, H.-K. Lee, and J. Chou, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time

- effects-part II: applications to IM drives with diode front end," *IEEE transactions on industry applications*, vol. 40, no. 6, pp. 1613-1620, 2004.
- [79] E. Un and A. M. Hava, "A near-state PWM method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters," *IEEE Transactions on Industry Applications*, vol. 45, no. 2, pp. 782-793, 2009.
- [80] R. M. Tallam, R. J. Kerkman, D. Leggate, and R. A. Lukaszewski, "Common-mode voltage reduction PWM algorithm for AC drives," *IEEE Transactions on Industry Applications*, vol. 46, no. 5, pp. 1959-1969, 2010.
- [81] H. Chen and H. Zhao, "Review on pulse - width modulation strategies for common - mode voltage reduction in three - phase voltage - source inverters," *IET Power Electronics*, vol. 9, no. 14, pp. 2611-2620, 2016.
- [82] Y.-S. Lai and F.-S. Shyu, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part I: basic development," *IEEE Transactions on Industry Applications*, vol. 40, no. 6, pp. 1605-1612, 2004.
- [83] Y. Lai, "New random technique of inverter control for common mode voltage reduction of inverter-fed induction motor drives," *IEEE Transactions on Energy Conversion*, vol. 14, no. 4, pp. 1139-1146, 1999.
- [84] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on industry applications*, no. 5, pp. 518-523, 1981.

- [85] F. Wang, "Motor shaft voltages and bearing currents and their reduction in multilevel medium-voltage PWM voltage-source-inverter drive applications," *IEEE Transactions on Industry Applications*, vol. 36, no. 5, pp. 1336-1341, 2000.
- [86] Z. Wang, X. Yin, H. Cheng, Z. Zhang, and J. Yang, "A novel PWM scheme to eliminate common-mode voltages in cascaded multi-level inverters," in *2003 IEEE PES Transmission and Distribution Conference and Exposition (IEEE Cat. No. 03CH37495)*, 2003, vol. 2: IEEE, pp. 780-785.
- [87] T. Kato, K. Inoue, A. Aki, and M. Azabu, "On-line reduction of switching losses and common-mode voltages of multi-level PWM inverter by a new space vector modulation," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2015: IEEE, pp. 1-6.
- [88] E. Asa, K. Colak, M. Bojarski, and D. Czarkowski, "A novel multi-level phase-controlled resonant inverter with common mode capacitor for wireless EV chargers," in *2015 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2015: IEEE, pp. 1-6.
- [89] D. A. Rendusara, E. Cengelci, P. N. Enjeti, V. R. Stefanovic, and J. W. Gray, "Analysis of common mode voltage-" neutral shift" in medium voltage PWM adjustable speed drive (MV-ASD) systems," *IEEE transactions on power electronics*, vol. 15, no. 6, pp. 1124-1133, 2000.
- [90] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Transactions on industrial electronics*, vol. 60, no. 12, pp. 5515-5527, 2012.

- [91] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on industrial electronics*, vol. 57, no. 8, pp. 2553-2580, 2010.
- [92] H.-J. Kim, H.-D. Lee, and S.-K. Sul, "A new PWM strategy for common-mode voltage reduction in neutral-point-clamped inverter-fed AC motor drives," *IEEE Transactions on Industry Applications*, vol. 37, no. 6, pp. 1840-1845, 2001.
- [93] H. Zhang, A. Von Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE transactions on industry applications*, vol. 36, no. 6, pp. 1645-1653, 2000.
- [94] R. Kanchan, P. Tekwani, M. Baiju, K. Gopakumar, and A. Pittet, "Three-level inverter configuration with common-mode voltage elimination for induction motor drive," *IEE Proceedings-Electric Power Applications*, vol. 152, no. 2, pp. 261-270, 2005.
- [95] S. Figarado, T. Bhattacharya, G. Mondal, and K. Gopakumar, "Three-level inverter scheme with reduced power device count for an induction motor drive with common-mode voltage elimination," *IET Power Electronics*, vol. 1, no. 1, pp. 84-92, 2008.
- [96] F. Hong, J. Liu, B. Ji, Y. Zhou, J. Wang, and C. Wang, "Interleaved dual buck full-bridge three-level inverter," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 964-974, 2015.
- [97] E. Levi, R. Bojoi, F. Profumo, H. Toliyat, and S. Williamson, "Multiphase induction motor drives-a technology status review," *IET Electric Power Applications*, vol. 1, no. 4, pp. 489-516, 2007.

- [98] E. Levi, "Multiphase electric machines for variable-speed applications," *IEEE Transactions on industrial electronics*, vol. 55, no. 5, pp. 1893-1909, 2008.
- [99] Q. Yan, X. Yuan, Y. Geng, A. Charalambous, and X. Wu, "Performance evaluation of split output converters with SiC MOSFETs and SiC Schottky diodes," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 406-422, 2016.
- [100] R. Bojoi, M. Lazzari, F. Profumo, and A. Tenconi, "INDUSTRIAL POWER CONVERSION SYSTEMS DEPARTMENT-Industrial Drives Committee-Digital Field-Oriented Control for Dual Three-Phase Induction Motor Drives," *IEEE Transactions on Industry Applications*, vol. 39, no. 3, pp. 752-760, 2003.
- [101] G. K. Singh, K. Nam, and S. Lim, "A simple indirect field-oriented control scheme for multiphase induction machine," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 4, pp. 1177-1184, 2005.
- [102] S. Hu, Z. Liang, W. Zhang, and X. He, "Research on the integration of hybrid energy storage system and dual three-phase PMSM drive in EV," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 8, pp. 6602-6611, 2017.
- [103] S. Bhattacharya, D. Mascarella, G. Joós, J.-M. Cyr, and J. Xu, "A dual three-level T-NPC inverter for high-power traction applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 668-678, 2016.
- [104] X. Jiang, W. Huang, R. Cao, Z. Hao, and W. Jiang, "Electric drive system of dual-winding fault-tolerant permanent-magnet motor for aerospace applications," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7322-7330, 2015.

- [105] Y. Zhao and T. A. Lipo, "Space vector PWM control of dual three-phase induction machine using vector space decomposition," *IEEE Transactions on industry applications*, vol. 31, no. 5, pp. 1100-1109, 1995.
- [106] K. Chinmaya and G. K. Singh, "Experimental analysis of various space vector pulse width modulation (SVPWM) techniques for dual three - phase induction motor drive," *International Transactions on Electrical Energy Systems*, vol. 29, no. 1, p. e2678, 2019.
- [107] Ó. López *et al.*, "Space-vector PWM with common-mode voltage elimination for multiphase drives," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8151-8161, 2016.
- [108] A. L. Julian, *Active common mode voltage reduction in voltage source inverters*. The University of Wisconsin-Madison, 1997.
- [109] Z. Shen, D. Jiang, Z. Liu, D. Ye, and J. Li, "Common-mode voltage elimination for dual two-level inverter-fed asymmetrical six-phase PMSM," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3828-3840, 2019.
- [110] Y. Duan, Z. Li, Y. Guo, and X. Zhang, "Synchronized SVPWM Strategy for Common Mode Voltage Reduction of High Power Inverters in the Overmodulation Region," in *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, 2019: IEEE, pp. 1-5.
- [111] M. J. Duran, J. Prieto, and F. Barrero, "Space vector PWM with reduced common-mode voltage for five-phase induction motor drives operating in overmodulation zone," *IEEE transactions on power electronics*, vol. 28, no. 8, pp. 4030-4040, 2012.

- [112] P. Tekwani, R. Kanchan, and K. Gopakumar, "A dual five-level inverter-fed induction motor drive with common-mode voltage elimination and DC-link capacitor voltage balancing using only the switching-state redundancy—Part I," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 5, pp. 2600-2608, 2007.
- [113] P. Rajeevan and K. Gopakumar, "A hybrid five-level inverter with common-mode voltage elimination having single voltage source for IM drive applications," *IEEE Transactions on Industry Applications*, vol. 48, no. 6, pp. 2037-2047, 2012.
- [114] S. Sharma, M. V. Aware, and A. Bhowate, "Symmetrical Six-Phase Induction Motor-Based Integrated Driveline of Electric Vehicle With Predictive Control," *IEEE Transactions on Transportation Electrification*, vol. 6, no. 2, pp. 635-646, 2020.
- [115] Z. Liu, Z. Zheng, Z. Peng, Y. Li, and L. Hao, "A sawtooth carrier-based PWM for asymmetrical six-phase inverters with improved common-mode voltage performance," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9444-9458, 2017.
- [116] L. Fangke, L. Haifeng, L. Yongdong, and C. Jianyun, "A Modulation Method to Eliminate Common-mode Voltage of Dual Three-Phase Motor," in *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2019: IEEE, pp. 1-5.
- [117] S. A. Yerkal, M. Aware, B. Umre, M. Waghmare, and A. Kumar, "Common Mode Voltage Elimination in a Three-to-Six Phase Indirect Matrix Converter Using SVM Technique," in *2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2020: IEEE, pp. 1-6.

- [118] J.-H. Baik, S.-W. Yun, and J.-Y. Yoo, "A new active zero state PWM for six-phase inverter," in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019-ECCE Asia)*, 2019: IEEE, pp. 933-938.
- [119] Z. Wang, X. Wang, X. Yang, C. Wen, Y. Gong, and Y. Hu, "Mitigation of DC-link current ripple for dual three-phase flux-adjustable hybrid PMAC drives using collaborative switching strategy," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 9, pp. 7202-7216, 2019.
- [120] Y. Ren and Z.-Q. Zhu, "Reduction of both harmonic current and torque ripple for dual three-phase permanent-magnet synchronous machine using modified switching-table-based direct torque control," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 6671-6683, 2015.
- [121] S. Wang, R. Chen, J. D. Van Wyk, F. C. Lee, and W. G. Odendaal, "Developing parasitic cancellation technologies to improve EMI filter performance for switching mode power supplies," *IEEE Transactions on Electromagnetic compatibility*, vol. 47, no. 4, pp. 921-929, 2005.
- [122] S. Wang and F. C. Lee, "Negative capacitance and its applications on parasitic cancellation for EMI noise suppression," in *2007 IEEE Power Electronics Specialists Conference*, 2007: IEEE, pp. 2887-2891.
- [123] W. Tan, X. Margueron, T. Duquesne, and N. Idir, "An improved parasitic capacitance cancellation method for planar differential mode inductor in EMI filters," in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, 2012: IEEE, pp. 1-6.

- [124] W. Zhao, X. Ruan, D. Yang, X. Chen, and L. Jia, "Neutral point voltage ripple suppression for a three-phase four-wire inverter with an independently controlled neutral module," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2608-2619, 2016.
- [125] J. P. R. A. Mello, C. B. Jacobina, and M. B. de Rossiter Corrêa, "Three-phase four-wire inverters based on cascaded three-phase converters with four and three legs," *IEEE Transactions on Industry Applications*, vol. 53, no. 6, pp. 5539-5552, 2017.
- [126] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: a comprehensive analysis [three-phase inverters]," *IEEE transactions on industrial electronics*, vol. 49, no. 1, pp. 186-196, 2002.
- [127] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters: principles and practice*. John Wiley & Sons, 2003.
- [128] D. Jiang and F. Wang, "A general current ripple prediction method for the multiphase voltage source converter," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2643-2648, 2013.
- [129] D. Jiang and F. Wang, "Current-ripple prediction for three-phase PWM converters," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 531-538, 2013.
- [130] F. Jin, H. Bai, D. Lu, and B. Cheng, "Maximizing potentials of SiC inverters for permanent magnet synchronous motor control by using FPGA," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018: IEEE, pp. 259-263.

- [131] S. Ogasawara and H. Akagi, "Modeling and damping of high-frequency leakage currents in PWM inverter-fed AC motor drive systems," *IEEE Transactions on Industry Applications*, vol. 32, no. 5, pp. 1105-1114, 1996.
- [132] D. Busse, J. Erdman, R. J. Kerkman, D. Schlegel, and G. Skibinski, "Bearing currents and their relationship to PWM drives," *IEEE Transactions on Power Electronics*, vol. 12, no. 2, pp. 243-252, 1997.
- [133] H. Akagi and T. Shimizu, "Attenuation of conducted EMI emissions from an inverter-driven motor," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 282-290, 2008.
- [134] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE transactions on Industry Applications*, vol. 32, no. 2, pp. 250-259, 1996.
- [135] L. Wang, Y. Shi, and H. Li, "Anti-EMI noise digital filter design for a 60-kW five-level SiC inverter without fiber isolation," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 13-17, 2017.
- [136] R. Bojoi, A. Cavagnino, M. Cossale, and A. Tenconi, "Multiphase starter generator for a 48-V mini-hybrid powertrain: Design and testing," *IEEE Transactions on Industry Applications*, vol. 52, no. 2, pp. 1750-1758, 2015.
- [137] J. Seong *et al.*, "DBC-packaged inverter power module for integrated motor-inverter design used in 48 V mild hybrid starter-generator (MHSG) system," *IEEE Transactions on Vehicular Technology*, vol. 68, no. 12, pp. 11704-11713, 2019.
- [138] A. Cavagnino, A. Tenconi, and S. Vaschetto, "Experimental characterization of a belt-driven multiphase induction machine for 48-V automotive applications: Losses

- and temperatures assessments," *IEEE Transactions on Industry Applications*, vol. 52, no. 2, pp. 1321-1330, 2015.
- [139] J. Seong *et al.*, "Multiphysics simulation analysis and design of integrated inverter power module for electric compressor used in 48-V mild hybrid vehicles," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1668-1676, 2019.
- [140] J. Holtz, W. Lotzkat, and A. M. Khambadkone, "On continuous control of PWM inverters in the overmodulation range including the six-step mode," *IEEE transactions on power electronics*, vol. 8, no. 4, pp. 546-553, 1993.
- [141] L. Guo, N. Jin, C. Gan, L. Xu, and Q. Wang, "An improved model predictive control strategy to reduce common-mode voltage for two-level voltage source inverters considering dead-time effects," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3561-3572, 2018.
- [142] G. Tan, X. Wu, Z. Wang, and Z. Ye, "A generalized algorithm to eliminate spikes of common-mode voltages for CMVRPWM," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6698-6709, 2015.
- [143] X. Zhang, R. Burgos, D. Boroyevich, P. Mattavelli, and F. Wang, "Improved common-mode voltage elimination modulation with dead-time compensation for three-level neutral-point-clamped three-phase inverters," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013: IEEE, pp. 4240-4246.
- [144] N. Aizawa, M. Kikuchi, H. Kubota, I. Miki, and K. Matsuse, "Dead-time effect and its compensation in common-mode voltage elimination of PWM inverter with

- auxiliary inverter," in *The 2010 International Power Electronics Conference-ECCE ASIA-*, 2010: IEEE, pp. 222-227.
- [145] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE transactions on industry applications*, vol. 37, no. 2, pp. 637-641, 2001.

VITA

Yang Huang was born in July 1993, in Chongqing, China. He received his B.S. degree from Southeast University, Nanjing, China in 2016, and his M.S. degree from the University of Michigan-Dearborn, MI, USA in 2018, both in Electrical Engineering. In 2018, he began his doctoral research study in Power Electronics at the Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT), University of Tennessee-Knoxville, TN, USA. His major research topics are EV charger design, FPGA-based controller design, motor drive techniques, and common-mode noise reduction. He has a wide spectrum of interests including photography, painting, stargazing, reading, playing bass guitar and basketball. He is incredibly grateful for all the support from his family and friends and excited about the new life after graduation.