To the Graduate Council:

I am submitting herewith a dissertation written by Rajagopal Vijayaraghavan entitled "Process and Temperature Compensated Wideband Injection Locked Frequency Dividers and their Application to Low-power 2.4-GHz Frequency Synthesizers." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Syed K. Islam

Major Professor

We have read this dissertation
and recommend its acceptance:

Benjamin Blalock

Charles L.Britton

Stephen F.Smith

Dayakar Penumadu

Accepted for the Council:

Carolyn R. Hodges

(Vice Provost and Dean the Graduate School)

(Original signatures are on file with official students records)

Process and Temperature Compensated Wideband Injection Locked Frequency Dividers and their Application to Low-Power 2.4-GHz Frequency Synthesizers

A Dissertation
Presented for the
Doctor of Philosophy Degree
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Rajagopal Vijayaraghavan
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Dedication

This dissertation is dedicated to my wife Ramya
my parents, my in-laws, my teachers and my dear god

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ABSTRACT

There has been a dramatic increase in wireless awareness among the user community in the past five years. The 2.4-GHz Industrial, Scientific and Medical (ISM) band is being used for a diverse range of applications due to the following reasons. It is the only unlicensed band approved worldwide and it offers more bandwidth and supports higher data rates compared to the 915-MHz ISM band. The power consumption of devices utilizing the 2.4-GHz band is much lower compared to the 5.2-GHz ISM band. Protocols like Bluetooth and Zigbee that utilize the 2.4-GHz ISM band are becoming extremely popular.

Bluetooth is an economic wireless solution for short range connectivity between PC, cell phones, PDAs, Laptops etc. The Zigbee protocol is a wireless technology that was developed as an open global standard to address the unique needs of low-cost, low-power, wireless sensor networks. Wireless sensor networks are becoming ubiquitous, especially after the recent terrorist activities. Sensors are employed in strategic locations for real-time environmental monitoring, where they collect and transmit data frequently to a nearby terminal. The devices operating in this band are usually compact and battery powered. To enhance battery life and avoid the cumbersome task of battery replacement, the devices used should consume extremely low power. Also, to meet the growing demands cost and sized has to be kept low which mandates fully monolithic implementation using low cost process.

CMOS process is extremely attractive for such applications because of its low cost and the possibility to integrate baseband and high frequency circuits on the same chip. A fully integrated solution is attractive for low power consumption as it avoids the need for power hungry drivers for driving off-chip components. The transceiver is often the most power hungry block in a wireless communication system. The frequency divider (prescaler) and the voltage controlled oscillator in the transmitter's frequency synthesizer are among the major sources of power consumption. There have been a number of publications in the past few decades on low-power high-performance VCOs. Therefore this work focuses on prescalers.

A class of analog frequency dividers called as Injection-Locked Frequency Dividers (ILFD) was introduced in the recent past as low power frequency division. ILFDs can consume an order of magnitude lower power when compared to conventional flip-flop based dividers. However the range of operation frequency also knows as the locking range is limited. ILFDs can be classified as LC based and Ring based. Though LC based are insensitive to process and temperature variation, they cannot be used for the 2.4-GHz ISM band because of the large size of on-chip inductors at these frequencies. This causes a lot of valuable chip area to be wasted. Ring based ILFDs are compact and provide a low power solution but are extremely sensitive to process and temperature variations. Process and temperature variation can cause ring based ILFD to loose lock in the desired operating band.

The goal of this work is to make the ring based ILFDs useful for practical applications. Techniques to extend the locking range of the ILFDs are discussed. A novel and simple compensation technique is devised to compensate the ILFD and keep the locking range tight with process and temperature variations. The proposed ILFD is used in a 2.4-GHz frequency synthesizer that is optimized for fractional-N synthesis. Measurement results supporting the theory are provided.

TABLE OF CONTENTS

1. INTRODUCTION …… **1**
1.1 2.4-GHZ ISM BAND …….. 1
1.1.1 Wireless Local Area Networks (WLANs)…….. 1
1.1.2 Bluetooth……. 3
1.1.3 Home Networking…… 3
1.1.4 Zigbee…….. 4
1.2 RESEARH MOTIVATION…….. 5
1.3 RESEARCH GOALS……... 9
1.4 DISSERTATION OVERVIEW…… 10

2. INJECTION-LOCKED FREQUENCY DIVIDER THEORY AND PRIOR ART……. **11**

3. WIDEBAND RING ILFD BASED ON NOVEL PROCESS AND TEMPERATURE COMPENSATION…….. **31**
3.1 MODIFIED SYMMETRIC DELAY CELL BASED WIDEBAND ILFD……... 32
3.2 PROCESS AND TEMPERATURE STABILIZED (PATS) RING OSCILLATOR DESIGN…….. 39
3.3 TRACKING AND CALIBRATION CIRCUITRY…….. 45
3.3.1 Tracking Circuitry…….. 46
3.3.2 Calibration Circuitry…….. 48
3.4 POST-LAYOUT SIMULATION RESULTS…….. 49

4. 2.4-GHz FREQUENCY SYNTHESIZER BASED ON PROCESS AND TEMPERATURE COMPENSATED RING ILFD…….. **54**
4.1 PLL BASED FREQUENCY SYNTHESIS……. 54
4.2 VOLTAGE CONTROLLED OSCILLATOR(VCO) DESIGN……... 64
4.2.1 VCO Architecture…….. 64
4.2.2 VCO Simulation Results…….. 69
4.3 MULTI-MODULUS DIVIDER DESIGN…… 71
4.3.1 Divider Architecture…….. 71
4.3.2 Divider Simulation Results…….. 73
4.4 CHARGE PUMP AND PHASE FREQUENCY DETECTOR……. 74
4.5 DIGITAL SIGMA-DELTA MODULATOR (SDM)……... 79
4.6 FREQUENCY SYNTHESIZER IMPLEMENTATION AND SIMULATION……... 82

5. CHIP IMPLEMENTATION, TEST SETUP AND MEASUREMENT RESULTS..... **99**
5.1 CHIP IMPLEMENTATION..... 99
5.2 PROCESS AND TEMPERATURE COMPENSATED ILFD CHARACTERIZATION..... 105
5.3 PROTOTYPE FREQUENCY SYNTHESIZER TESTING..... 126

6. CONCLUSION AND FUTURE WORK..... **136**
6.1 ANTICIPATED ORIGINAL CONTRIBUTION..... 136
6.2 FUTURE WORK..... 136

REFERENCES..... **138**

VITA..... **145**

LIST OF TABLES

Table 3.1. Delay cell transistor sizes…… 38
Table 3.2. Locking range for different latch transistor sizes…… 38
Table 3.3. Achieved and required change in V_{cntrl} for process compensation…….. 49
Table 3.4. Threshold voltage simulation of the delay cell across process corners…… 50
Table 3.5. Threshold voltage simulation of the delay cell with temperature for nominal process corner…….. 50
Table 3.6. Locking range simulation for various control word…… 52
Table 3.7. Comparison of locking range for divide-by-4 across process corners with and without compensation…….. 52
Table 3.8. Comparison of locking range for divide-by-6 across process corners with and without compensation…….. 53
Table 3.9. Worst-case power consumption of the ILFD, V_{DD}=1.8V……... 53
Table 3.10. Comparison with previously published ILFDs…….. 53
Table 4.1. Bluetooth specifications……. 82
Table 4.2. PLL parameters……... 98
Table 5.1. Measured natural frequency of oscillation of the ring oscillator on 6 different chips…… 107

LIST OF FIGURES

Figure 1.1. Fractional-N PLL based frequency synthesizer…… 8
Figure 2.1. Model for the ILFD…… 13
Figure 2.2. Schematic of the ILFD……... 13
Figure 2.3. Phase noise spectrum of an ILFD[5]…… 19
Figure 2.4. Schematic of a static frequency divider……... 20
Figure 2.5. ILFD based on a simple modification to a static divider…… 22
Figure 2.6. Schematic of the conventional ILFD and the proposed QDL……... 23
Figure 2.7. Conceptual diagram of the QDL…… 25
Figure 2.8. Schematic of n-stage modulus-N divider……... 26
Figure 2.9. Modulo -3 divider…….. 28
Figure 2.10. Modulo-5 divider……. 28
Figure 2.11. Schematic of the bias control circuitry for the divider…….. 30
Figure 3.1. Schematic of the ILFD based on symmetric load ring Oscillator….. 33
Figure 3.2. Model for a ring oscillator with latches…….. 35
Figure 3.3. Model for the delay cells…… 35
Figure 3.4. Process and temperature compensation circuitry…… 42
Figure 3.5. Tracking circuitry…….. 47
Figure 3.6. Calibration circuitry……... 48
Figure 3.7. f_o Variation with process and temperature…….. 50
Figure 4.1. PLL based frequency synthesizers……... 55
Figure 4.2. Open-loop pole-zero plot of the 3rd order PLL…… 58
Figure 4.3. PLL model with noise injected from various blocks…….. 60
Figure 4.4. Schematic of a 3th order loop filter……. 64
Figure 4.5. LC VCO based on current-reuse topology and band switching… 65
Figure 4.6. Discrete and continuous tuning of the VCO [18]…… 67
Figure 4.7. Model of the LC tank with integrated inductors…… 68
Figure 4.8. Simulated tuning range of the VCO……. 70
Figure 4.9. VCO worst-case phase noise……. 70
Figure 4.10. Schematic of the multi-modulus divider…….. 72
Figure 4.11. Schematic of the 2/3 divider used in the multi-modulus Divider… 72
Figure 4.12. Multi-modulus divider simulation results……. 73
Figure 4.13. Schematic of the charge pump…… 75
Figure 4.14. Timing circuitry for the charge pump……. 75
Figure 4.15. Phase frequency detector for minimizing the dead zone of the PLL…… 79
Figure 4.16. 3rd Order MBSL-I sigma-delta modulator…….. 81
Figure 4.17. Phase noise at the output of the MBSL-I SDM with a division step=1…… 85
Figure 4.18. Phase noise at the output of the MBSL-I SDM with a division step=4…… 86
Figure 4.19. Phase noise at the output of the MBSL-I SDM with a division

step=8…… 87
Figure 4.20. Phase noise at the output of the PLL due to MBSL-I SDM with a division step=1……... 89
Figure 4.21. Phase noise at the output of the PLL due to MBSL-I SDM with a division step=4…….. 90
Figure 4.22. Phase noise at the output of the PLL due to MBSL-I SDM with a division step=8…….. 91
Figure 4.23. Phase noise at the output of the PLL due to the Charge Pump Noise……. 92
Figure 4.24. Phase noise of the VCO……... 93
Figure 4.25. Phase noise at the output of the PLL due to the VCO…… 94
Figure 4.26. Overall phase noise at the output of the PLL due to MBSL-I SDM with a division step=1…….. 95
Figure 4.27. Overall phase noise at the output of the PLL due to MBSL-I SDM with a division step=4……. 96
Figure 4.28. Overall phase noise at the output of the PLL due to MBSL-I SDM with a division step=8……. 97
Figure 5.1. Chip microphotograph……... 100
Figure 5.2. Implementation details of the 2.4-GHz frequency synthesizer… 102
Figure 5.3. Power supply scheme…… 103
Figure 5.4. 4-Layer printed circuit board for circuit characterization……... 104
Figure 5.5. ILFD with GSG Pads for on-wafer characterization……... 106
Figure 5.6. Output spectrum of the ILFD for an input signal frequency = 1.8 GHz……. 109
Figure 5.7. Output spectrum of the ILFD for an input signal frequency = 2.4 GHz……. 110
Figure 5.8. Output spectrum of the ILFD for an input signal frequency = 2.9 GHz……. 111
Figure 5.9. Output spectrum of the ILFD when out of locking range……. 112
Figure 5.10. Measured tuning range of the LC VCO……. 113
Figure 5.11. Maximum frequency generated by the LC VCO…… 114
Figure 5.12. Minimum frequency generated by the LC VCO…… 115
Figure 5.13. Locked spectrum at the output of the of the ILFD for an input of 2.652 GHz…… 116
Figure 5.14. Locked spectrum at the output of the of the ILFD for an input of 2.057 GHz…… 117
Figure 5.15. Phase noise of the LC VCO at an offset frequency of 600 KHz….. 119
Figure 5.16. Phase noise of the LC VCO at an offset frequency of 1 MHZ…… 120
Figure 5.17. Phase noise of the free running oscillator at an offset frequency of 600 KHz…… 121
Figure 5.18. Phase noise of the free running oscillator at an offset frequency of 1 MHz…….. 122
Figure 5.19. Phase noise of the Injection Locked oscillator at an offset frequency of 600 KHz…… 123

Figure 5.20. Phase noise of the injection locked oscillator at an offset frequency of 1 MHz…….. 124
Figure 5.21. Variation of the oscillation frequency of the ring oscillator with temperature……. 125
Figure 5.22. Interface circuitry between sigma-delta modulator and the multi-modulus divider……. 127
Figure 5.23. Output spectrum of the of the PLL based frequency synthesizer while synthesizing 2.4 GHz……. 129
Figure 5.24. Output spectrum of the PLL based frequency synthesizer while synthesizing 2.4 GHz showing reference spurs……. 130
Figure 5.25. Output spectrum of the PLL based frequency synthesizer while synthesizing 2.2 GHz showing reference spurs……. 131
Figure 5.26. Output spectrum of the PLL based frequency synthesizer while synthesizing 2.6 GHz ……... 132
Figure 5.27. Measured phase noise while synthesizing 2.4 GHz at offset frequencies of 1 MHz and 2 MHz……. 134
Figure 5.28. Measured phase noise while synthesizing 2.2 GHz…… 135
Figure 5.29. Measured phase noise while synthesizing 2.6 GHz…… 135

CHAPTER 1

INTRODUCTION

1.1 2.4-GHz ISM BAND

The past five years have seen a dramatic increase in the level of radio awareness among the consumer community, brought about largely through the prevalence of the use of mobile and cordless phones [1]. The 2400-2483.5 MHz band also known as the 2.4-GHz band, is being used for an increasingly diverse range of wireless applications; it is the only unlicensed band approved worldwide. The 2.4-GHz band offers more bandwidth than the 915 MHz ISM band. Thus, wider channel spacing, supporting higher data rates is possible. Wireless applications utilizing this band include Wireless Local Area Networking (WLAN), Bluetooth, Home Networking and ZigBee. Reference [1] gives a detailed description and requirements of each standard. A gist of the above standards will be outlined here using the information provided in [1].

1.1.1 Wireless Local Area Networks (WLANs)

WLANs standard provides a cordless solution to office connectivity and are used widely for internal networking of PCs and peripherals. They can be used in two ways; as an indoor substitute or complement to conventional wired LANs and as outdoor system for point-to-point data transfer. WLANs have revolutionized the office environment by providing more flexibility to the user. For example, the users may be require a wide range of information in a conference or meeting room where they are present for a fairly brief

period of time. In outdoor applications, WLANs can be seen as an alternative to the costly hire of leased lines, installation of licensed point-to-point microwave links, or the capital-intensive installation of cable. WLANs can also be useful for point to multipoint applications, for example local authorities operating on multiple sites; university and school campuses, and increasingly dispersed company campuses.

IEEE 802.11 and 802.11b are the key international standards influencing the WLANs development. These standards, widely accepted around the world, have led to a significant increase in the user confidence; this has been boosted by the introduction of the "WiFi" brand, allowing immediate recognition of interoperable products. These define the specifications for Frequency Hopping Spread Spectrum (FHSS), operating at a maximum of 3 Mbps and Direct Sequence Spread Spectrum (DSSS), offering 11 Mbps products. IEEE 802.11 defines operations of WLAN systems at frequencies between 2400 and 2483.5 MHz. FHSS WLAN systems utilize 79 hopping channels between 2402 and 2480 MHz with channel spacing of 1 MHz. DSSS WLAN systems utilize 9 (IEEE 802.11) or 11 (IEEE 802.11b) frequency channels with channel spacings of 22 MHz. The development of the technical standards is ongoing. FCC intends to increase the channel bandwidth of FHSS systems to 3 MHz and 5 MHz to enable them to operate at 11 Mbps. The transmitted power is in the order of 100 mW (20 dBm). The demands for WLAN-ready equipped PC have increased almost by 5 orders of magnitude in the past five years. The annual unit sales in the year 2000 was 39,000 and the sales in 2005 was 3,800,000.

1.1.2 Bluetooth

"Bluetooth" is a global wireless connectivity standard that has been developed by a consortium of IT and telecommunications companies. It is intended to replace proprietary cable links which connect IT and telecommunication devices to one another and replace them with a single universal short range radio link. It is intended to provide very short range (10 m or less) connectivity, unlike WLANs that provides connectivity up to a few kilometers, and can be used for individual cables linking mobile phones, PCs, modems, printers etc. The range of applications that can be addressed by Bluetooth is extensive [1].

Bluetooth uses FHSS, 1000 hops/s technology to ensure robust performance in a noisy radio environment, supporting both voice and data, up to a data rate of 1 Mbps. The Bluetooth standard uses the same 2402-2480 MHz spectrum as the IEEE 802.11 standards but the transmitted power is significantly lesser (1 mW or 0 dBm). The demand for Bluetooth-equipped units has also increased considerably since the year 2000. The total installed units have grown from 96,000 in year 2000 to 20,000,000 units in 2004.

1.1.3 Home Networking

The concept of home networking extends the benefits of WLANs to home and small office environments. In the United States the drive towards home networking is being led by the HomeRF consortium. The HomeRF vision sees a wide range of electronic home equipment being wirelessly networked within the home and made accessible remotely via public telecommunication or data networks. In common with Bluetooth, an open, non-proprietary standard for home networking has been developed for home networking. The

HomeRF open standard is titled SWAP (Shared Wireless Access Protocol). All of them currently use FHSS technology. HomeRF products can support data rate up to 10 Mbps.It uses FHSS, 50 hops/s modulation. The transmitted power is in the order of 100 mW.

1.1.4 Zigbee

The ZigBee protocol is intended for use in embedded applications requiring low data rates and low power consumption. ZigBee's current focus is to define a general-purpose, inexpensive, self-organizing, mesh network that can be used for industrial control, embedded sensing, medical data collection, smoke and intruder warning, building automation, home automation, etc. The resulting network will use very small amounts of power, so individual devices might run for a year or two using the originally installed battery.

Zigbee devices are required to conform to the IEEE 802.15.4-2003 low-rate Wireless Personal Area Network (WPAN) standard. This standard specifies operation in the unlicensed 2.4-GHz band. There are 16 ZigBee channels, with each channel requiring 3 MHz of bandwidth. The center frequency for each channel can be calculated as, FC = 2400 + 5(k) MHz, where k = 1, 2... 16. The radios use direct-sequence spread spectrum coding, which is managed by the digital stream into the modulator. Orthogonal QPSK that transmits two bits per symbol is used in the 2.4-GHz band. The maximum output power of the radios is generally 1 mW.

1.2 Research Motivation

Power consumption, size and cost have to be kept low in order to meet the growing demands of mobile wireless communications. To meet these requirements it is desirable to implement the transceivers monolithically using low-cost integrated circuit technology. CMOS offers an attractive solution when compared to BiCMOS and GaAs chips because of its low cost. Further, it has the potential to integrate baseband digital modules and the RF modules in the same chip leading to the concept of a compact system-on-chip (SOC) solution. Due to the extensive scaling down of CMOS technology and increasing operating speed, it is has become possible to implement high-performance Radio Frequency circuits and systems using CMOS processes that were possible only with Si based BiCMOS or GaAs processes [2]. CMOS-based circuits operating at 60 GHz have already been reported [3].

Most devices used in wireless communications are hand-held and battery operated, demanding very low power consumption. This is true especially for devices used in wireless sensor networks that are becoming ubiquitous, especially after the recent terrorist activities. Sensors are employed in strategic locations for real-time environmental monitoring, where they collect and transmit data frequently to a nearby terminal. Low power consumption enhances battery life and reduces the cumbersome process of replacing the batteries in these devices. Wireless communication protocols also place very stringent frequency specifications and have restrictive phase noise requirements to reduce the effects of large blocking signals. Meeting these requirements with very low power consumption is a huge challenge for CMOS-based frequency

synthesizers, due to the high-frequency parasitic effects, high noise and low-quality passive elements available in standard CMOS processes. The frequency synthesizer, which provides the local oscillator signals for the transmitter and receiver section, consumes a significant portion of the transceiver power. Most of the frequency synthesizers used in wireless communications is PLL-based. The voltage controlled oscillator (VCO) and the prescaler are the two blocks in a synthesizer that work at RF frequencies and consume about eighty percent of the power. Low-power and high-performance VCOs have been a major topic of research over the last decade. The field has been well explored, with numerous publications appearing over the past few years. Therefore, this work focuses on prescaler.

A class of analog prescalers (frequency dividers) known as Injection-Locked Frequency Dividers (ILFD) has gained tremendous popularity in the recent years as low power dividers. There have been a number of publications on ILFDs [4-9] as candidates for low-power frequency dividers. The ILFDs have shown potential to consume up to an order of magnitude lower power when operating at gigahertz frequencies compared to conventional frequency dividers employing flip-flops [4]. The main drawback of the ILFDs is their limited locking range which is also sensitive to process and temperature variations. ILFDs can be both ring oscillator-based and LC tank-based. LC tank-based ILFDs, although more stable with temperature and process variations, are not very attractive for the 2.4 GHz regime due to the size of the on-chip inductors at these frequencies. The locking range of the LC-based ILFDs is also much less than that of ring oscillator-based ILFDs [7]. Ring oscillator-based ILFDs are compact and consume low-

power while operating in the 2.4-GHz band, but are extremely sensitive to process and temperature variations. Their locking ranges could be adversely affected by process and temperature variations that can sometimes throw them out of the desired locking range. This can be true even for ring based wideband ILFDs, as reported in [6,10].

Prior work on ILFDs [4,5,7-10] lacks a treatment on the impact of process and temperature on the locking range of ILFDs, although the references provide a thorough treatment on the ILFD theory. A temperature and process-stabilized 2.4 GHz ILFD proposed in [6] and the low power ILFDs of [7,8] use a ring-oscillator delay element configuration that is prone to power supply noise and substrate noise [11]; this is not desirable in a fully integrated environment. Also, [6] lacks measurement results and mathematical treatment. Few frequency synthesizers employing ring oscillator based ILFDs are found in literature. The frequency synthesizer proposed in [12] uses a process and temperature compensated ILFD prescaler of [6] that has the above mentioned drawback. Also, the work lacks measurement results. The locking range of the ILFD used in [6] is limited and this prevents it from being used for multi-band applications [13].

Most of the applications mentioned in section 1.1 use FHSS techniques that require agile frequency synthesizers to switch rapidly from one frequency to another [13]. This requires fast-settling frequency synthesizers. The use of ILFD based prescalers, for reducing power consumption, achieves a fixed frequency division ratio ahead of the programmable divider as shown in Figure 1. Therefore, the reference frequency to the PLL has to be reduced to achieve tight channel spacing. A lower reference frequency

corresponds to a lower loop-bandwidth and hence a slower settling time if an integer-N PLL architecture is used [14]. A fractional-N PLL [15-17] decouples the relation between channel bandwidth and settling time and is therefore attractive for fast-settling FHSS systems. This is useful especially when ILFD based prescalers are used and tight channel spacing is required. The block diagram of the fractional-N frequency synthesizer is shown in Figure 1. It is capable of achieving a fractional division ratio by using a delta-sigma modulator that controls the division ratio of a multi-modulus divider every clock cycle such that the average division ratio is a fractional number. There are various types of delta-sigma modulators, each with different noise properties. Also, achieving a fixed division ratio ahead of the programmable divider that the delta-sigma modulator drives,

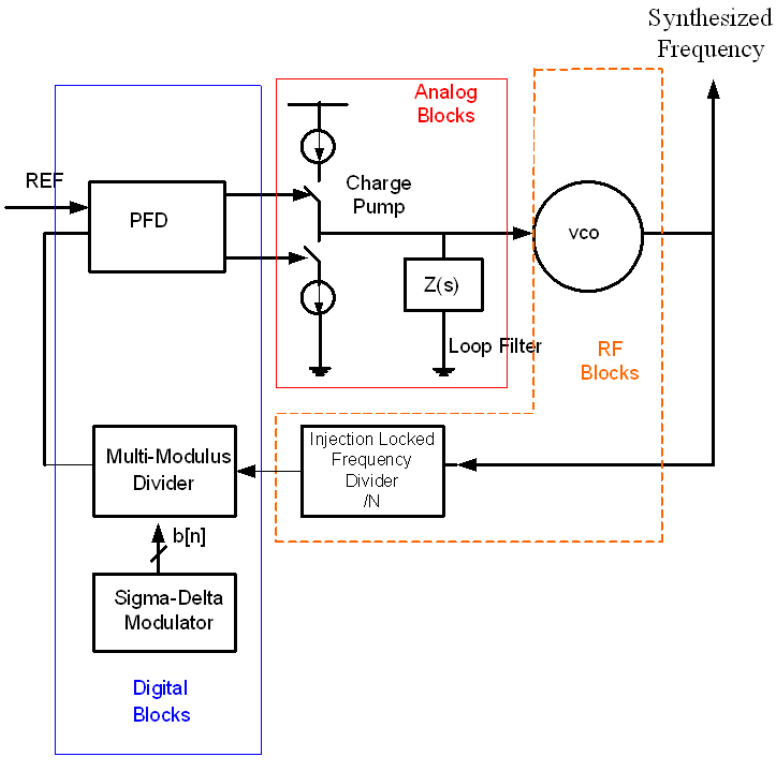


Figure 1.1. Fractional-N PLL based frequency synthesizer

may lead to a increased in-band noise. This work models these effects and studies the appropriate kind of delta-sigma modulator suitable for noise reduction.

1.3 Research Goals

Although ring-based ILFDs have existed for the past few years, their use in practical applications becomes limited or even impossible if their sensitivity to temperature and process is not addressed. The aim of this research is therefore to:

1. Devise a simple and effective scheme for compensating a wideband, low-power divide-by-4 ILFD over process variations and a temperature range of -20°C to 100°C to achieve lock over a wide frequency range.
2. Impart multiband operation capability over the specified process and temperature range using special on-chip calibration/tuning circuitry.
3. Provide a detailed analysis on wideband ILFDs and provide insights for obtaining a wide locking range for division modulus of 2 or higher. Highlight the common phenomena underlying most of the existing wideband ring-based ILFDs and extend it to an architecture that is convenient to compensate over process and temperature variations.
4. Design a frequency synthesizer that has fractional-N capability built into it and is capable of operation in the 2.4-GHz ISM band using the proposed ILFD. Study the effects on the phase noise due to the fixed division imposed in the prescaler.

1.4 Dissertation Overview

The dissertation is organized as follows. In Chapter 2, the theory of operation of ring-based (wideband) ILFDs is described. This is followed by a discussion of the prior art in ring-based ILFDs. Chapter 3 introduces the proposed wideband ILFD and the process and temperature compensation scheme for the ILFD. Simulation results supporting the proposed theory are also provided. Chapter 4 gives a brief description on PLL-based frequency synthesizers and discusses the architecture of the other important blocks of the PLL-based frequency synthesizer that include the phase frequency detector, charge pump, VCO, and the programmable divider. Fractional-N synthesis techniques based on the sigma-delta modulator is introduced next. The influence of the choice of ILFD divide ratio on the noise of the synthesizer is analyzed using MATLAB. This is followed by a noise analysis of the entire Fractional-N PLL. Chapter 5 provides the chip implementation details and the 4-layer printed circuit board (PCB) design. Wafer probing techniques for characterizing the ILFD are described next. Measurement results supporting the theory are provided in the latter part of Chapter 5. Finally, Chapter 6 provides future directions and conclusions.

CHAPTER 2

INJECTION-LOCKED FREQUENCY DIVIDER THEORY AND PRIOR ART

Injection-locked frequency dividers (ILFD) can be described as free-running oscillators that lock to a sub-harmonic of an injected input signal. The injection-locking phenomenon has been known to exist for a long time. Miller proposed a regenerative frequency-locking circuit based on this principle [19]. Miller used a frequency multiplier in the feedback loop to achieve division ratios greater than 2. The free-running aspect differentiates ILFDs from regenerative dividers that require an input signal to produce an output. Adler [20] studied the injection-locking phenomena for various types of oscillators and showed that it is a fundamental property of oscillators. It was observed in a wide variety of oscillators with the same qualitative behavior observed in each case. Divide-by-2 prescalers operating beyond 5 GHz have been reported in various technologies like GaAs, SiGe, Si-BJT and CMOS. However, in this work only CMOS-based ILFDs are considered.

As mentioned in the previous chapter, ILFDs can be LC tank-based or ring-based. In this work only the later type of ILFDs, particularly implemented using CMOS processes, will be considered, as they are more area and power efficient when operating in the lower GHz regime. However, it should be noted that as the operating frequencies increase beyond 10 GHz, LC based ILFDs consume much lower power when compared to their ring counterparts.

Ring-based ILFDs can be classified based on their architecture or locking range as:

- Single ended and differential ILFDs (based on architecture), and
- Wideband and narrowband ILFDs (based on locking range)

This chapter briefly describes the various ring oscillator-based ILFDs existing in the literature and also explains the theory behind their operation. Publications on CMOS ring based ILFDs started to appear frequently from 2001. The work by the authors of [4] laid the foundation for future work on this topic. The ILFD proposed in [4] was a differential and narrowband ILFD for low-power divider applications to be used in wireless telemetry. The major contribution of this paper was to provide a model for ILFDs and derive an analytical expression for the locking range of the ILFD. The ILFD circuit design could be optimized based on the analytical expressions. Figure 2.1 shows the model of the ILFD and Figure 2.2 shows the transistor-level schematic of the ILFD. The delay cells consisted of symmetric delay elements ("Maneatis load", after its inventor) with replica feedback biasing [21]. The Maneatis loads were chosen for their high dynamic substrate and supply noise rejection, which becomes important to reduce jitter in a fully integrated environment. A brief explanation of the ILFD theory based on [4] will be presented next. This will help the reader understand the circuit's general operation as well as that of other types of ILFDs to follow.

The input signal with a frequency f_{IN} is injected into the tail transistor of the first stage of the multi-stage ring oscillator that has a natural frequency of oscillation (with no signal injection) of f_0. In the absence of the injected signal, the Barkhausen criteria for stable oscillation are satisfied at f_0. Each stage of the n-stage ring oscillator causes a total phase

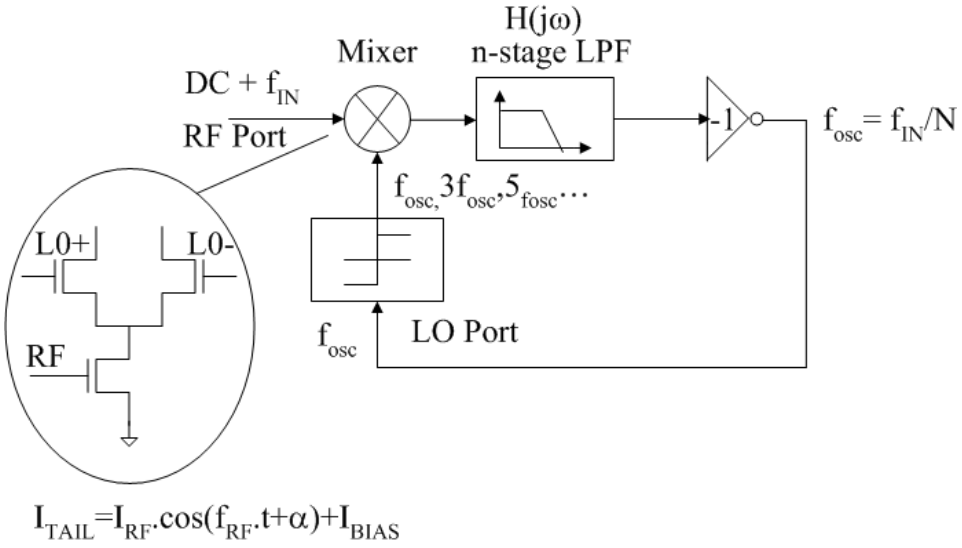


Figure 2.1. Model for the ILFD

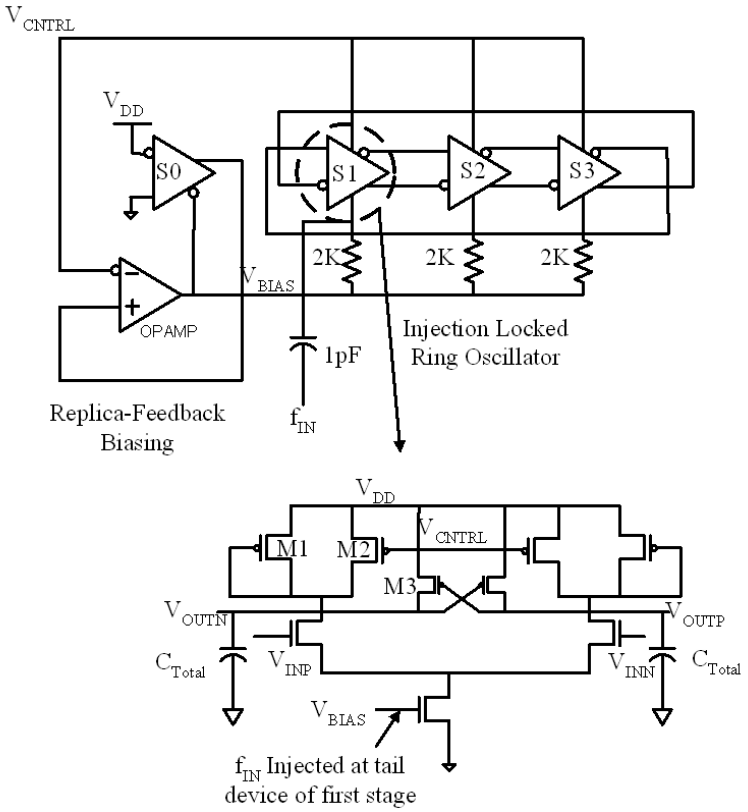


Figure 2.2. Schematic of the ILFD

shift of π/n, where n is the number of stages, which added to the 180° phase shift due to the inverted connection between the last and the first stage, causes a 360° phase shift around the loop at f_0. Also, the loop gain must be greater than unity at the oscillation frequency. The injected signal at f_{IN} causes a phase shift in the first stage of the ring oscillator that changes the frequency of oscillation to a frequency f_{OSC} that is different from f_0. The ring now oscillates at a frequency $f_{OSC,}$ at which the loop compensates the phase shift due to the first stage to provide an overall phase shift of 360°. The frequency f_{OSC} can be expressed as $f_0 + \Delta f$.

The first stage of the ring oscillator can be modeled as a single-balanced mixer with the input frequency f_{IN} injected to the RF port and the frequency f_{OSC} applied to the input pairs. Due to the odd symmetry of the input differential pairs (which is true when the inputs switch fast), odd harmonics of the input frequencies, f_{OSC}, $3f_{OSC}$, $5f_{OSC}$ etc are created by the differential pair. The harmonics are mixed with the input signal that is injected into the tail transistors. If the amplitude of the incoming RF signal is high enough to "hard-switch" the tail transistor, all harmonics of the tail current source are created. The subsequent stages of the ring oscillator can be modeled as low-pass filters that filter out frequencies higher than f_{0SC}. Thus, if the frequency of the incoming signal $f_{IN}=N.f_0$, where N is an integer, the output frequency is given by $f_{IN}-(N-1)f_{OSC}$. The output frequency f_{OSC} tracks f_{IN}/N as long as the other stages of the ring oscillator are able to provide sufficient magnitude and a total phase shift of 360° at the frequency $f_{OSC} =f_0+ \Delta f$. For the ring oscillator-type ILFDs, the amplitude criteria is easily satisfied and the phase criteria determines the locking range [4]. Thus, if the incoming frequency

departs sufficiently from the natural frequency of oscillation, the loop fails to lock to the incoming frequency. It is therefore necessary to keep the natural frequency of oscillation essentially fixed over process and temperature.

The locking range of the divider was derived in [4] when the amplitude of injection is weak. It was later extended for strong injection amplitudes and verified using simulations. For an n-stage ring oscillator using Maneatis loads, the locking range is given by,

$$\frac{\Delta\omega}{\omega_0} = \frac{4}{n \cdot \sin\left(\frac{2\pi}{n}\right)} \tan^{-1}\left(\frac{k_0}{\sqrt{1-k_1^{\,2}}}\right) \tag{2.1}$$

where,

$$k_0 = \eta_i \left|\frac{C_{N-1} - C_{N+1}}{C_1}\right| \tag{2.2}$$

$$k_1 = \eta_i \left|\frac{C_{N-1} + C_{N+1}}{C_1}\right| \tag{2.3}$$

and,

$$\eta_i = \frac{I_{RF}}{2 \cdot I_{DC}} \tag{2.4}$$

η_i is the injection efficiency and N is the division ratio. C_k are the Fourier coefficients of the mixing function, and can be approximated by,

$$C_k = \begin{Bmatrix} \frac{1}{k\pi}(-1)^{(k-1)/2}, k = odd \\ 0, otherwise \end{Bmatrix} \tag{2.5}$$

Equation (2.1) gives the double-sided locking range for weak input signals. It can be seen that the locking range is a function of the injection efficiency η_i and the magnitude of the Fourier coefficients C_{N-1} and C_{N+1} . Also, k_i^2 is a small number and for small values of injected signals, k_0 is small. Therefore, the locking range increases linearly with injected signal strength. Also, the assumption that the mixer's switching function is a square wave is accurate if the ratio of the output swing to the overdrive voltage of the differential pair transistors is much greater that one. This is true for the case of the ring oscillator which employs Maneatis loads. If this assumption fails, the Fourier coefficients are drastically reduced, thus degrading the locking range.

The following non-idealities affect the injection efficiency and lead to a reduced/compressed locking range:

1) Transconductance drop due to velocity saturation, device non-linearity and drain junction parasitics.
2) Large input amplitude, causing the tail transistor to operate in the non-linear region. This causes a decrease in the injection efficiency due to the increase in I_{DC} due to even order non-linearities. This phenomenon leads to a compression of the locking range.
3) The parasitic capacitances within the mixer reduce the magnitude of the RF current which feeds the switching differential pair. Specifically, the drain capacitance of the tail device provides a shunt path for the RF current, reducing the injection efficiency.

To summarize the above discussion, as the amplitude of injection increases from weak ($\eta_i << 1$) to strong ($\eta_i > 1$), the locking range increases linearly for weak injection and then begins to saturate for strong injection as given in reference [4].

Measurement results on the ILFD fabricated in a 0.24 μm CMOS process showed the potential to divide by various even division ratios. However, the locking range was very narrow, which degraded further for higher-order division. For a 3-stage ILFD the locking range for divide by 2 and 4 stages were 125 MHz and 56 MHz, respectively. For a 5-stage ILFD Division by 2, 4, 6 and 8 had locking ranges of 12.7 MHz, 32 MHz, 17 MHz and 20 MHz respectively. In all the above cases, an input signal of -3dBm was injected. The worst-case power consumption from the divider sore was 993 μW.

Reference [5] provides a unified model for various types of ILFDs. A generalized procedure for accurately simulating the locking ranges of ILFDs is outlined. However, the most important contribution of this work is on the transient response and phase noise of ILFDs. It is important to understand the transient response of the ILFDs because it reveals much about its phase-noise filtering properties. The following paragraph gives a brief summary [5] that will be useful for understanding the transient response and phase noise of the ILFD.

Let the input signal to the ILFD be denoted as $v_I = V_{DC} + V_I \cos(N\omega_0 t + \alpha)$ and the output signal as $v_0 = V_0 \cos(\omega_0 t + \varphi)$, where phase is considered for both input and output. The output phase of the ILFD can be perturbed by two sources, the phase noise of the input

signal and the internal phase noise of the ILFD. There is a fixed phase relationship between the input and output signals in the steady state. If α remains fixed, and φ deviates due to the internal phase noise, the IFLD would eventually return to its original steady-state value. If α steps suddenly to a different value, then φ would stabilize to a new steady-state value in the absence of noise. The transient response of the ILFD was shown to be exponential for weak injected signals and small frequency or phase perturbations around the natural frequency of oscillation [5]. The output phase returns with a time constant given by,:

$$\tau = \frac{1}{N}\left|\frac{S}{k_1 - k_0}\right| \tag{2.6}$$

where S, is the slope of the phase response of the filter linearized around the natural frequency of oscillation and k_1 and k_0 are defined by (2.2) and (2.3). It can be seen that the parameters that increase the phase-limited locking range also reduce the time constant leading to a faster settling time.

The phase-limited locking range of an ILFD is approximately 1/N times the 3-dB bandwidth of the first-order system response. A detailed analysis of the phase noise of the ILFD is given in [5] and will not be repeated here. The results of the analysis indicate that the ILFD behaves basically like a first-order PLL. The internal free-running phase noise of the ILFD is filtered with a high-pass filter, while the noise from the external source is filtered with a low-pass filter. The total phase noise of the ILFD is given by the expression,

$$L_{\phi,total}(\Delta\omega) = L_{\phi,free}(\Delta\omega).\frac{\Delta\omega^2}{\Delta\omega^2 + \omega_p^2} + L_{\alpha,ext}(\Delta\omega).\frac{(\Delta\omega_p / N)^2}{\Delta\omega^2 + \omega_p^2} \quad (2.7)$$

Where, $L_{\varphi,free}(\Delta\omega)$ is the free-running phase noise of the ring oscillator and $L_{\alpha,ext}(\Delta\omega)$ is the phase noise of the input source, which is usually the VCO of the PLL. It can be seen from equation (2.7) and Figure 2.3 that the internal phase noise of the free-running ring oscillator is low-pass filtered. Thus, the close-in phase noise ($1/f^3$) caused due to up-converted flicker noise in the ring oscillator is filtered. The extent of filtering also depends on the pole frequency, ω_p, which is analogous to the loop-bandwidth of the first order PLL. However, the difference is that ω_p can be increased by increasing the strength of the injection signal. Also, the output tracks the input phase noise with a scale factor $1/N^2$.

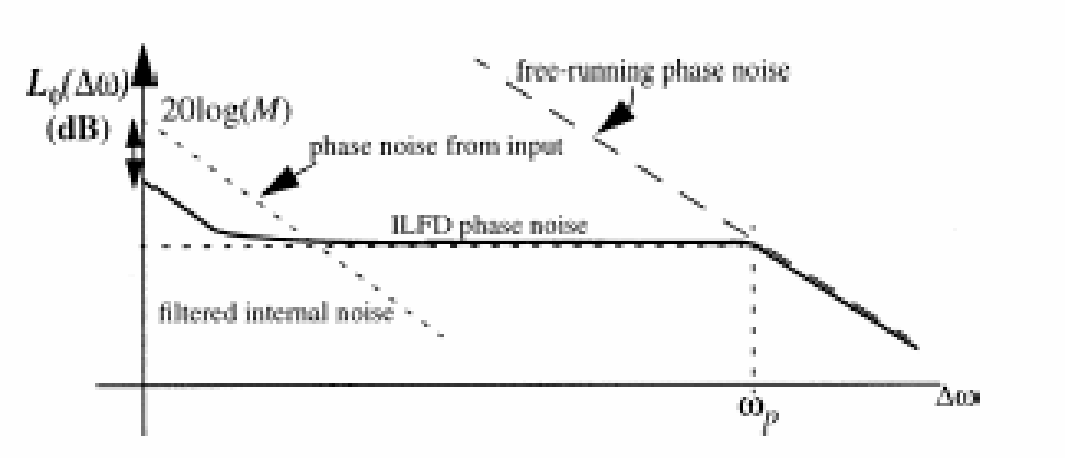


Figure 2.3. Phase noise spectrum of an ILFD [5]

The work by the authors of [10] presents an ILFD that is obtained by a simple modification of a static divider. Figure 2.4 shows a static frequency divider which employs two D-latches in a master-slave configuration with negative feedback. Each stage has two transistors for sensing (M3 and M4), two cross-coupled transistor pairs for latching (M5 and M6), and two clock transistors (M1 and M2). The clock is inverted before applying to the slave (bottom stage). When the clock signal is in the "high" state the master (top stage) is in the sense mode and the slave is in the latch mode. When the clock is "low" the roles are exchanged. To enable operation at higher frequencies, the topology removes the clock transistors beneath the cross coupled pair when compared to the conventional topologies [22]. This leads to an increased gate-source voltage and thus the transconductance of the latch transistors. The width of the latch transistors can

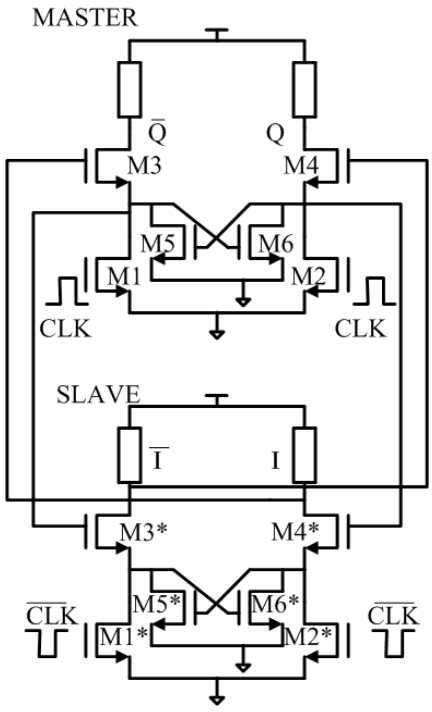


Figure 2.4. Schematic of a static frequency divider

therefore be reduced leading to decreased parasitics and enabling higher frequency operation. Authors of reference [22] have shown that increasing the g_m of the latches leads to better divider performance by using the sensitivity curve of the divider. The sensitivity cure of the divider gives the minimum amplitude of the input signal for which the divider functions properly. It has also been shown in reference [22] that as the g_m of the latches were increased the minimum signal amplitude reduces.

Static dividers like the ones presented in Figure 2.4 have a very wide bandwidth. They can also operate down to arbitrarily low frequencies. The delay through the D- flip flops determines the maximum frequency of operation of the static dividers. For achieving higher division ratios more static stages have to be cascaded which leads to an increased power consumption. The static divider can be converted to an ILFD using a simple modification as shown in Figure 2.5 [10]. The input clock is applied to the master stage and only a DC biasing signal is applied to the clock transistors of the slave stage. The transistor pairs M1, M3 and M2, M4 acts like mixers while the other stages acts like low pass filters. When compared to the static dividers, ILFDs use the non-linearities inherent in mixing to realize division. Therefore, they do not require extra stages for division by ratios higher than 2. The presence of strong latches in the circuit topology can give an important advantage in obtaining wide locking range even for frequency division ratios greater than 2. Measurement results show that the divider proposed in [10] has a locking range of 1.6 GHz for division by 4 and 1.1 GHz for division by 6 and consumes 7 mW from a 1.8-V power supply. The maximum input signal frequency applied was 11.3 GHz and 7.6 GHz for divide by 6 and 4 circuits, respectively.

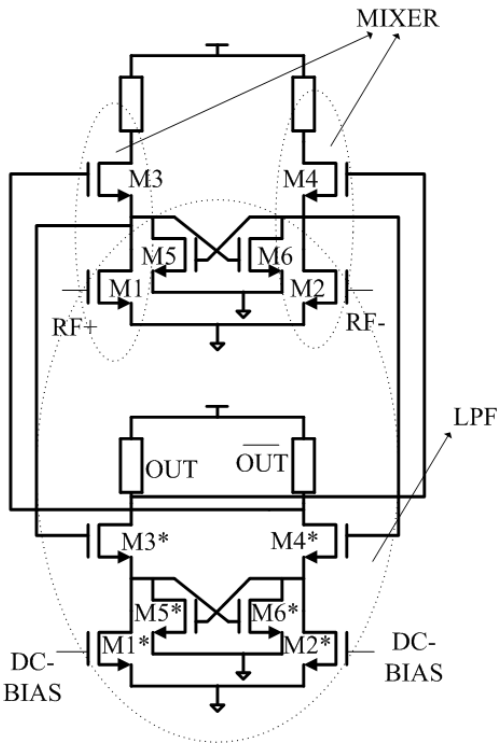


Figure 2.5. ILFD based on a simple modification to a static divider

The work presented next is an ILFD that achieves the lowest power consumption reported to date in the literature. It is an example of a wideband single-ended ILFD. Figure 2.6 shows the proposed divider architecture, along with a conventional three-stage inverter-based ILFD. In a conventional divider a transistor is connected in series with an inverter stage to modulate the oscillations. This makes it difficult to scale the supply voltage down. It also decreases the open loop gain of the oscillator and narrows the locking range as the series transistor source-degenerates the input transistor. The design proposed in [7] solves the above problem by directly modulating the output of the ring

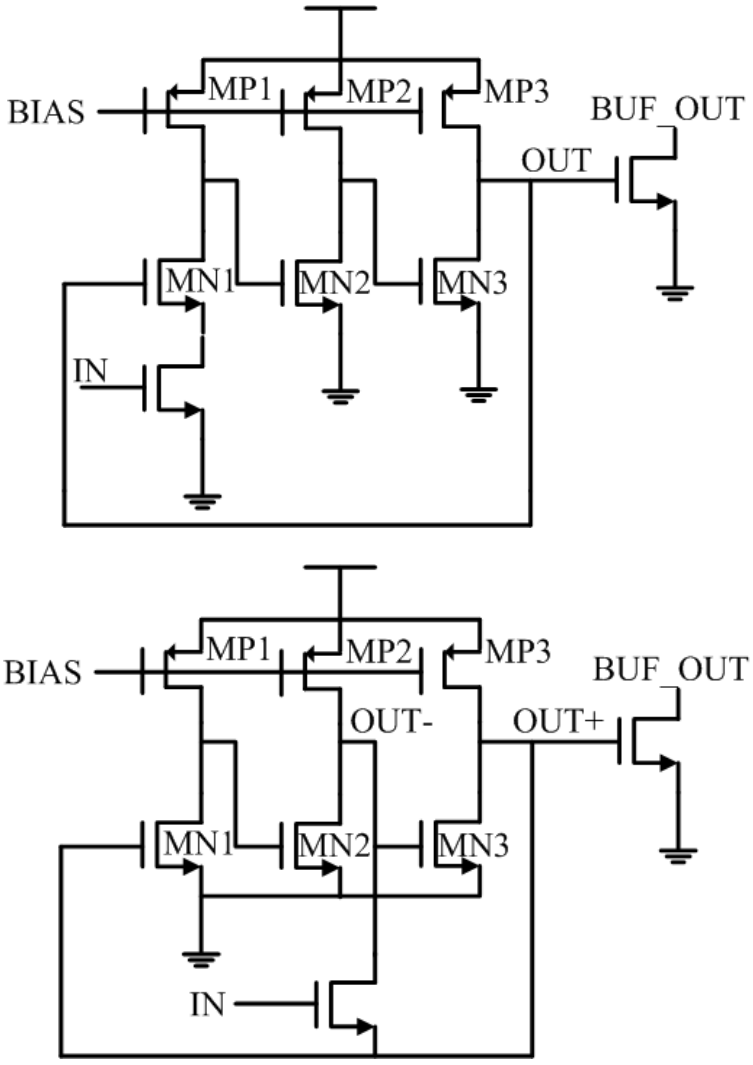


Figure 2.6. Schematic of the conventional ILFD and the proposed QDL

oscillator by using a switch inserted between two inverter outputs. This new divider topology was termed quasi-differential locking divider (QDL). The QDL has low-voltage operation capability due to the absence of the series connected transistor.

The conceptual diagram of the QDL is shown in Figure 2.7. Nodes OUT+ and OUT- compose the quasi-differential outputs. Three states A, B and C can be considered for the QDL and they iterate in a cycle given by A-B-C-B. In states A and C, the input becomes high and the switch equalizes the voltage between nodes OUT+ and OUT-. The direction of the current flow is opposite in both the cases. In state A current flows from OUT+ to OUT- and in state B it is reversed. In state B the input is low and the oscillator in the QDL operates at its resonant frequency. Since the input has two cycles and the differential outputs have one cycle per iteration, the QDL operates as a divide-by-two prescaler. If the input frequency is greater than twice the self-resonant frequency, the phase of the input voltage of the switch precedes the phase of the differential voltage between the two nodes of the switch. If the input frequency is less than twice the self-resonant frequency the phase of the input voltage of the switch lags the phase of the differential voltage between the two nodes of the switch. In both cases, the phase of the differential outputs is locked to the input.

To improve the performance of the QDL, the transistor sizes were optimized to increase the DC differential voltage between OUT+ and OUT-. This increases the peak current flowing through the input transistor and leads to an enhanced locking range. The QDL has a measured locking range of 2.3 GHz and was capable of divide-by-two operation up

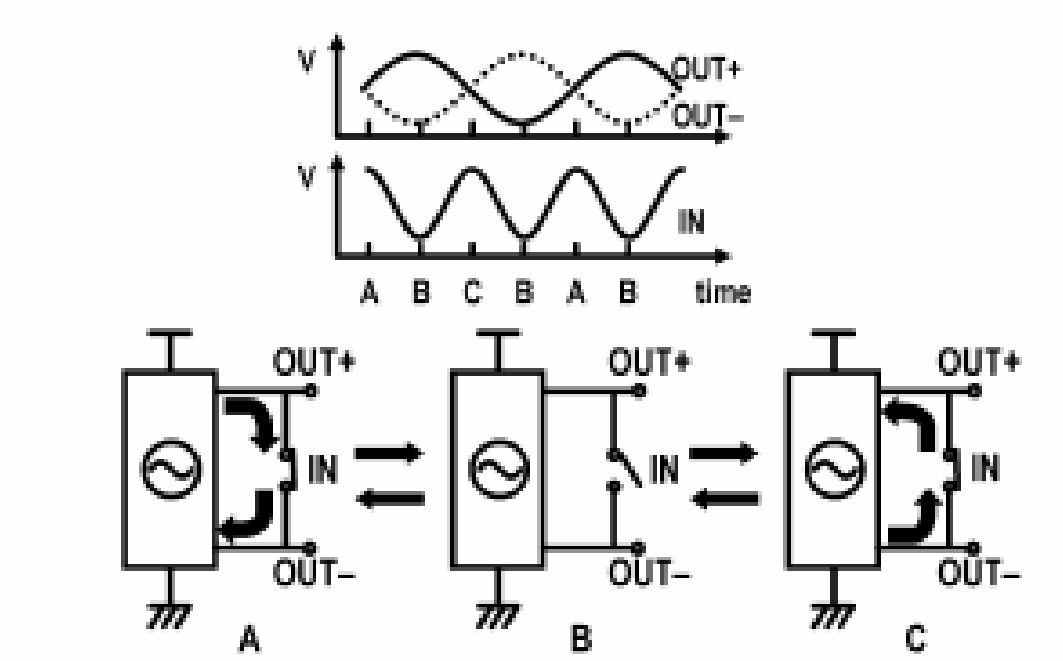


Figure 2.7. Conceptual diagram of the QDL

to 4.3 GHz when the power supply voltage was 0.7 V. The power consumption in this case was 44 μW. For 1.8 V operation the divider could reach a maximum operating frequency of 16 GHz with a power consumption of 1.6 mW.

The ILFDs presented thus far were only capable of achieving division by even moduli. Also, their locking range degrades with an increasing division modulus. In reference [8], a novel single-ended wideband ILFD for various modulus applications is presented. Figure 2.8 shows the proposed divider. For modulo-N operation, the divider consists of N delay stages and the incident signal is applied to all the delay cells. When the loop is locked, the input node of the injector V_X should be synchronized with the incident signal V_{RF} at the incident frequency ω_i and the Barkhausen criteria for oscillation should be

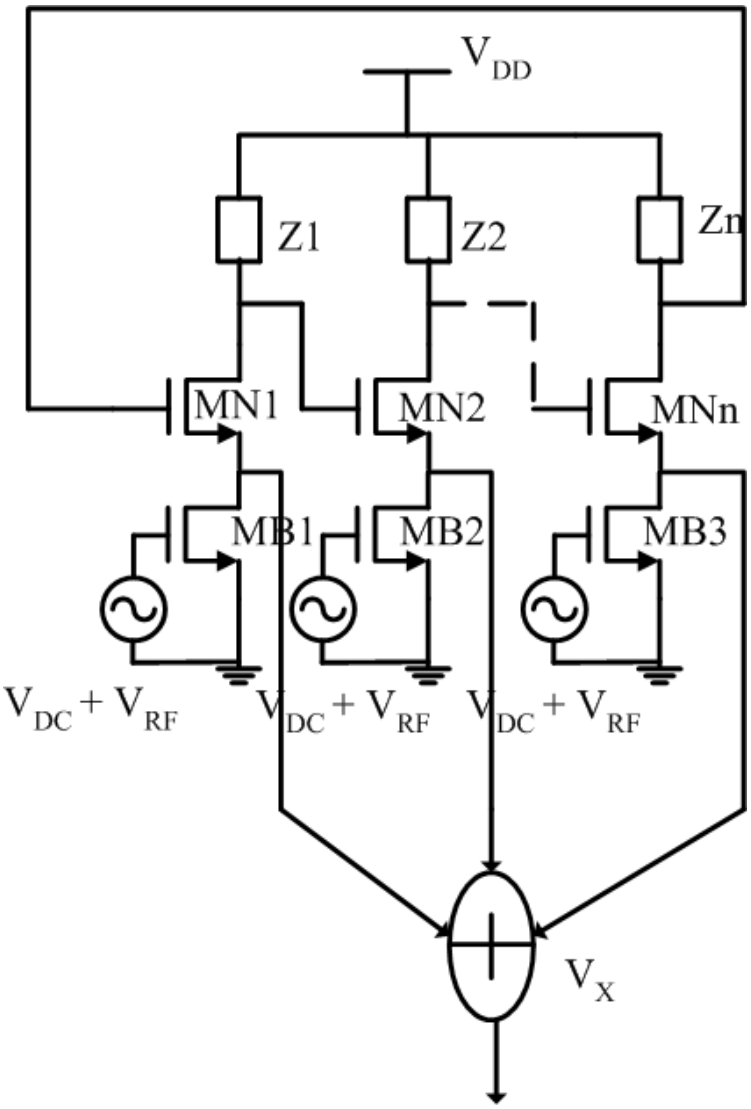


Figure 2.8. Schematic of n-stage modulus-N divider

satisfied. Assume Vj = A sin [$\omega_0 t + (2\pi j/n)$ and source voltage V_{kj} of transistor M_j is a non-linear function of V_j when the RF signal is not injected. V_{kj} can be expressed as,

$$V_{kj} = a_0 + a_1 V_j^1 + a_2 V_j^2 + a_3 V_j^3 + \ldots. \quad (8)$$

If V_{kj} is summed up using a wired-or connection, it can be shown that,

$$V_X = b_0 + \gamma_1 a_n A^n \sin [n\omega_0 t\ ] + \gamma_2 a_{2n} A^{2n} \sin[n\omega_0 t\ ] + \ldots\ , \quad (9)$$

where γ_j would be greater than one. It turns out that the lowest operating frequency that can be sustained at V_X is the N- order harmonic of Vj, and all the lower-order harmonic tones are suppressed. Therefore, when an excitation signal in the vicinity of $N\omega_0$ is incident, the power spectral density at the input of the injector V_X would be concentrated at the vicinity of the $n\omega_i$ rather than spreading over all the harmonic tones of $n\omega_0$. This implies a more effective injection scheme. Since the coefficient of the N^{th}-order harmonic is increased to $\gamma_1 a_n$, the locking ranges can be increased. In summary, an N-stage oscillator-based ILFD is feasible for a modulo-N operation. The achievable locking frequency would be N times higher than the free running frequency of the ring oscillator, provided the incident signal is effectively injected.

Figure 2.9 and 2.10 [8] show the prototype modulo-3 and modulo-5 dividers implemented in a standard 0.25 μm CMOS process using the above technique. The signals are summed at the common source of the ring delay elements. The capacitance introduced by the output buffers limits the operating speed of the dividers. This can be improved by using inductive loads to tune out the buffer capacitance as shown in Figure 2.9 (b). The measured locking range was close to 900 MHz. The divider consumes 1.75 mW and operates up to 7.1 GHz for modulo-3 operation; for modulo-5 operation, the

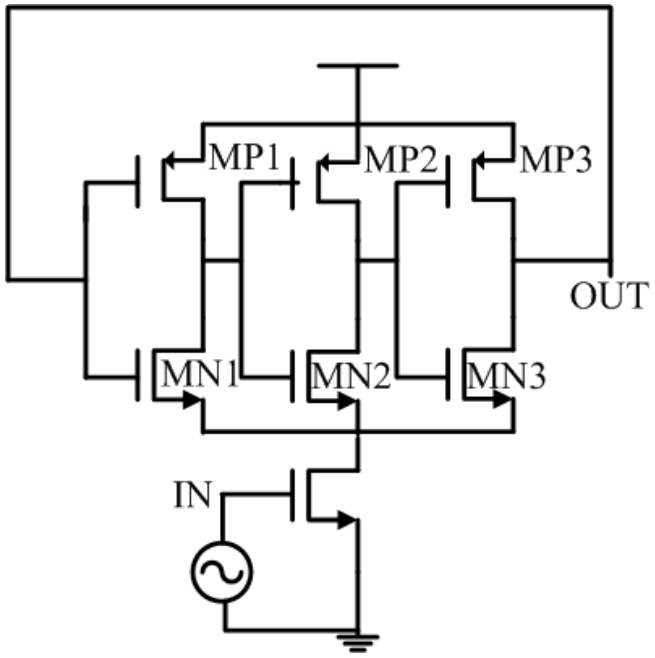


Figure 2.9. Modulo -3 divider

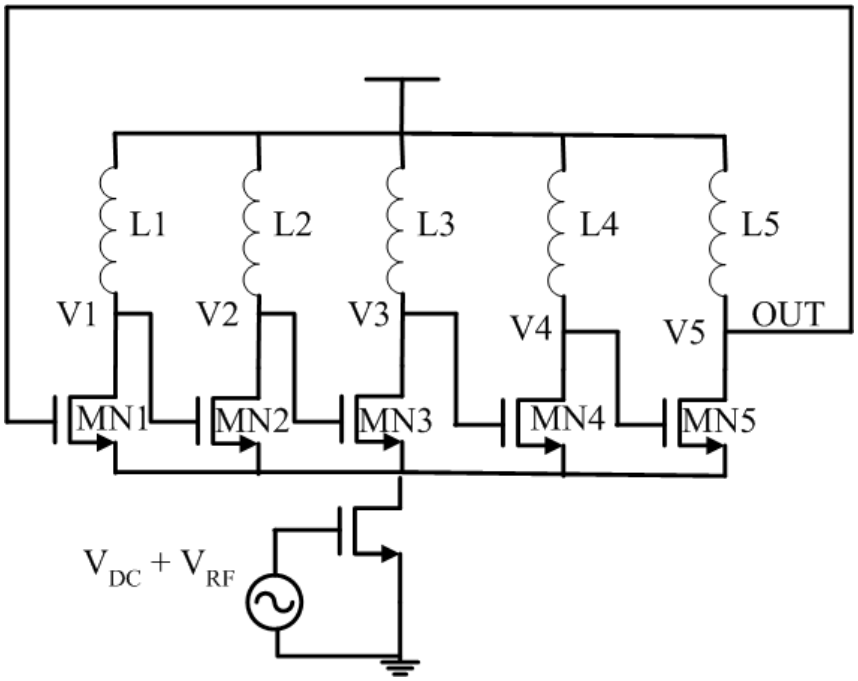


Figure 2.10. Modulo-5 divider

power consumption and operating frequency are 3.75 mW and 18 GHz respectively.

All the above mentioned work is based on measurement results. Although, Reference [6] is based on simulation results, it is still useful since as it addresses process and temperature compensation of ILFDs. The architecture is similar to the one presented in [10], except that the resistor loads are replaced by PMOS devices in saturation. The bias to the PMOS load is adjusted to keep the resonant frequency of the oscillator constant with process and temperature. Figure 2.11 shows the schematic of the bias control circuitry for the divider.

For a constant bias current I_0, the gate voltage of the transistor M1, V_g, tracks the changes in process and temperature. This is compared with a bandgap voltage and the difference is amplified by a differential amplifier to produce a current I_{ax} . This current adjusts the total bias current to compensate the changes in process and temperature variations. An auxiliary circuit as shown in [6] is used for tracking the changes in input frequency. The auxiliary circuit uses the control voltage to the VCO, when the divider is integrated in a PLL, to adjust the divider resonant frequency to track the VCO frequency. The ILFD was capable of achieving a locking range of 2.2 GHz – 2.4 GHz over process variations and a temperature range of -20 ° C – 100 ° C while consuming only 2 mW from 2.5 V power supply.

Some of the popular work on LC-based ILFDs can be found in references [23-26]. Readers interested in LC-based ILFDs can find more details in these papers.

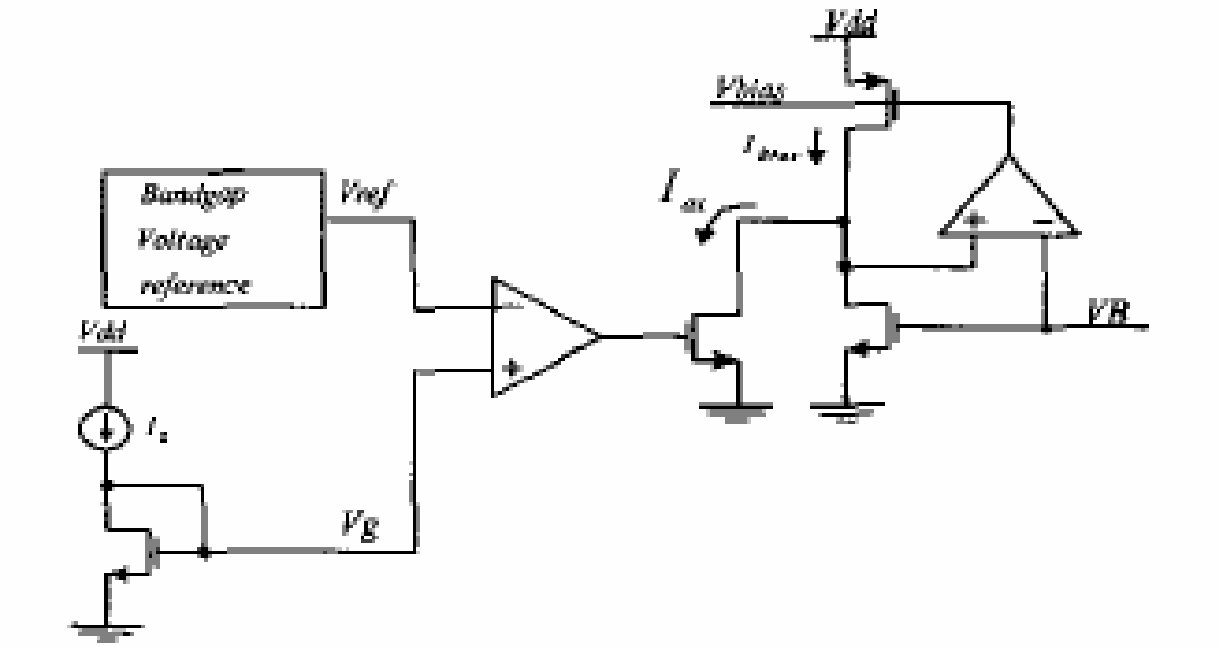


Figure 2.11. Schematic of the bias control circuitry for the divider

CHAPTER 3

WIDEBAND RING ILFD BASED ON NOVEL PROCESS AND TEMPERATURE COMPENSATION

It is clear from the previous chapters that ring-based ILFDs are highly attractive for low-power prescaler applications in the multi GHz regime. However, to make the ring-based ILFDs suitable for practical applications, they should possess the following characteristics:

1. Capability to function correctly over a wide range of frequencies, i.e., wideband operation capability.
2. Ability to maintain the desired locking range over process and temperature variations.

Ring oscillators are extremely sensitive to process and temperature variations. Therefore their natural frequency of oscillation f_0, i.e., the frequency at which Barkhausen criteria is satisfied, can change with process and temperature variations. As shown in the previous chapter, the ILFDs can function as a divider only around a range of frequencies, $f_o \pm \Delta f$, known as the locking range. Alternatively, a divide-by-N ILFD can track input frequencies only in the range $N*(f_0 + \Delta f/2)$**.** Although wideband ILFDs were reported in the literature, their sensitivity to process and temperature was not examined. The only work that addresses this issue is reference [6]. However, the delay stages used are extremely sensitive to power supply and substrate noise. Power supply can directly modulate the current flowing in the delay stages leading to an increased jitter. Also, the delay elements are non-linear which can lead to noise-folding and a hence a worse phase-

noise performance. Although the above can be tolerated for divider applications, it cannot be when the injection-locked ring oscillator is used as a secondary oscillator [27]. In applications where spectral purity is a primary concern and additional power dissipation can be tolerated, a primary oscillator (either LC-tank based or ring based) running at 2X frequency is more efficiently used to drive an ILFD configured as a divide-by-2 that filters the phase noise of the primary oscillator.

3.1 Modified Symmetric Delay Cell based Wideband ILFD

To alleviate the sensitivity of the oscillator to supply and substrate noise, a Maneatis load (symmetric load) with replica feedback biasing is used in this work [21]. The delay cell, shown in Figure 3.1, is similar to the one used in [4]. In [4], the main purpose of the latch was to make the zero crossing faster and hence reduce flicker noise up conversion [28]. However, in this work, the latches in the delay cells are made stronger to increase the locking range and also to achieve a division ratio greater than 2 [10]. The use of strong latches improves higher order non-linearities and enables division by higher order modulus [4,10]. The modified symmetrical delay cell is biased using a replica feedback circuit as shown in Figure 3.1 [21]. The replica feedback circuitry adjusts the bias on the tail transistors to achieve a swing between V_{DD} and V_{Cntrl}. Thus, the voltage swing is independent of the power supply which leads to static power supply noise rejection. The latch uses a PMOS- transistor to maintain the swing between V_{DD} and V_{Cntrl}. The sources of the latches were tied to V_{DD} to increase the g_m of the latches similar to that in [10].

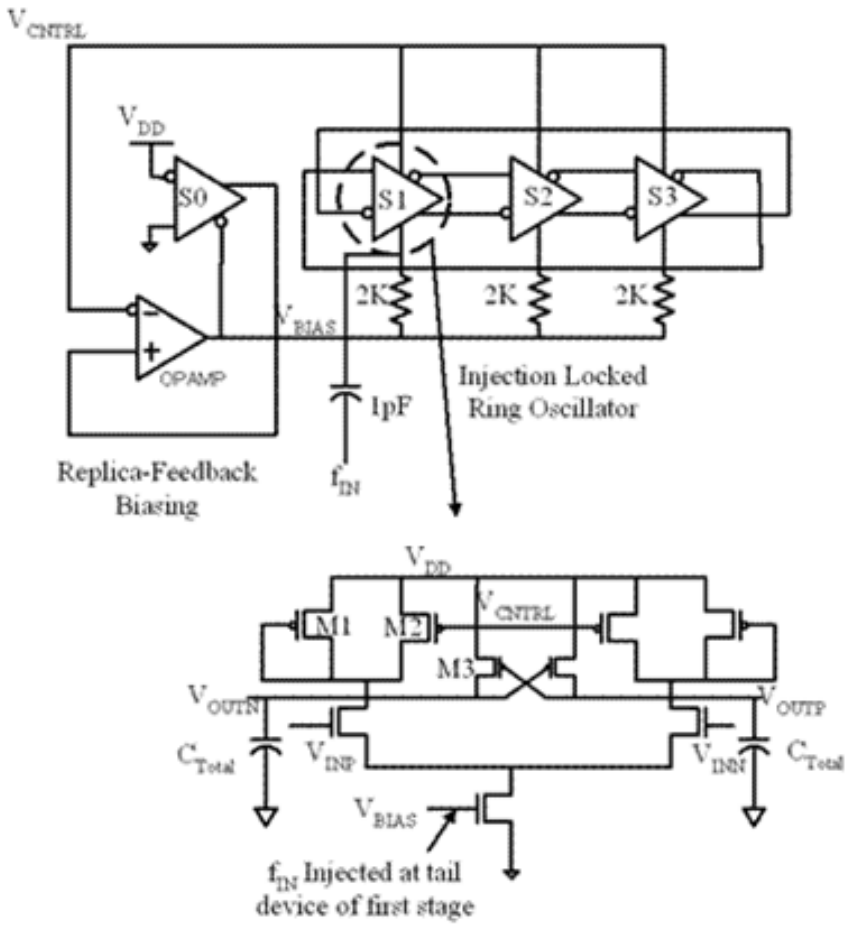


Figure 3.1. Schematic of the ILFD based on symmetric load ring oscillator

The use of strong latches changes the expression of the frequency of oscillation, which is derived next. Reference [11] derives an expression for a ring oscillator with delay cells using latches and incorporating hysteresis. The same methodology is adapted to our design. The principal difference between [11] and the work presented here is in the delay cell architecture. The delay stages encounter rail-to-rail swings in [11], whereas, in this work, the output voltage swing is between the control voltage (V_{cntrl}) and V_{DD} due to the replica feedback biasing. Also, the delay cell used here has weak hysteresis because of the relatively lower overdrive on the PMOS. Therefore, a three-stage ring oscillator is used to guarantee startup of oscillations.

The N-stage ring oscillator employing resistive loads and latches can be modeled as shown in Figure 3.2. Resistance R and C model the output impedance and the input parasitic capacitance of the delay elements. The delay elements can be modeled as shown in Figure 3.3. The operation of the circuit can be explained as follows. When the input signal V_{INP} makes a transition from low to high, the outputs start charging/discharging with an RC time constant until a threshold voltage level (V_{th}) is reached, where the latches become active and initiate a positive feedback. Until this point the latch behaves like a capacitive load that is taken in into account by C_{TOTAL}. The delay cell can be viewed much like the delay cell in [11] with a resistively loaded inverter and a PMOS-only latch. At the threshold voltage (for a low-to-high transition of V_{INP}), the differential pair transistor is in saturation and the latch transistor in triode, therefore the expression for the threshold point can be derived by equating the currents through the transistors and is given by,

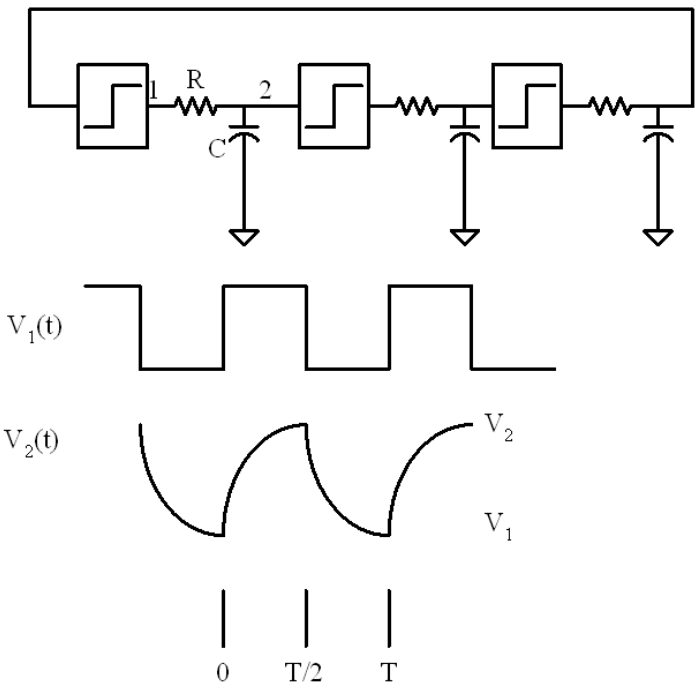


Figure 3.2. Model for a ring oscillator with latches

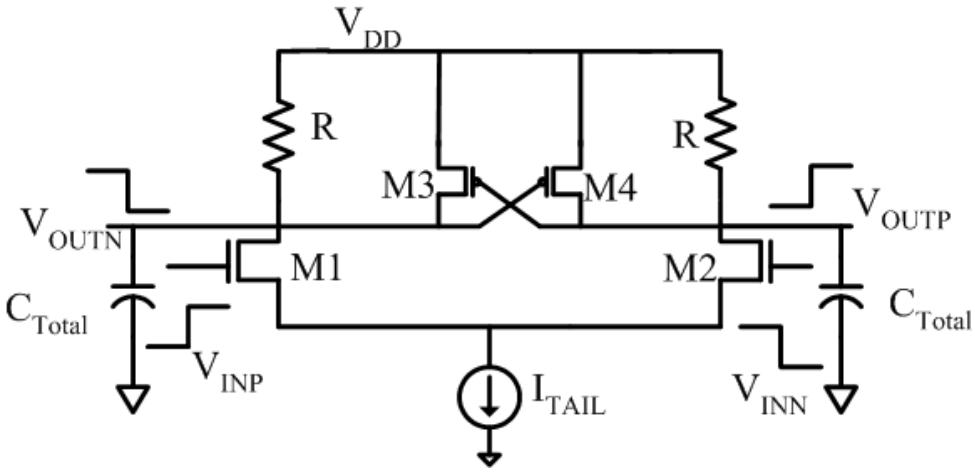


Figure 3.3. Model for the delay cells

$$V_{th} = V_{TN} + \sqrt{\frac{2\beta_3}{\beta_1}[(V_{dd} - V_{TN} - |V_{TP}|)|V_{TP}| - \frac{1}{2}V_{TP}{}^2]} \tag{3.1}$$

The threshold voltage can also be found using DC simulations. The threshold voltage can be changed by changing the aspect ratio of the input transistor M1 and the latch transistor M3 of Figure 3.3.

The time delay of the oscillator is calculated by assuming that the initial voltage for each rising edge at node 1 is V_1 and the initial voltage for each falling edge is V_2 as shown in Figure 3.2. $V_2(t)$ is given by,

$$V_2(t) = \begin{cases} V_{DD}(1 - e^{\frac{-t}{RC}}) + V_1 . e^{\frac{-t}{RC}}, for \cdots 0 < t < \frac{T}{2} \\ V_2 e^{\frac{-(t-\frac{T}{2})}{RC}}, for \ldots t > \frac{T}{2} \end{cases} \tag{3.2}$$

With periodic boundary conditions $V_1(T/2) = V_2$ and $V_2(t) = V_1$, equation (3.2) can be rewritten as equation (3.3) and (3.4),

$$V_{DD}(1 - e^{-\frac{T}{2RC}}) + V_1 e^{-\frac{T}{2RC}} = V_2 \tag{3.3}$$

$$V_2 e^{-\frac{T}{2RC}} = V_1 \tag{3.4}$$

Solving the above equation for $V_1$and V_2 we have,

$$V_1 = \frac{V_{DD}}{1 + e^{\frac{T}{2RC}}} \tag{3.5}$$

$$V_2 = \frac{V_{DD}.e^{\frac{T}{2RC}}}{1+e^{\frac{T}{2RC}}} \tag{3.6}$$

At t=T/2N after $V_2(t)$ starts rising from V_1, it must cross over V_{th} to trigger the next stage Therefore,

$$V_{th} = V_2\left(\frac{T}{2N}\right) = V_{DD}\left(1 - \frac{e^{-\frac{T}{2NRC}}}{1+e^{-(\frac{T}{2RC})}}\right) \tag{3.7}$$

The time delay can be obtained by solving equation (3.7). For N>2 the above equation becomes tedious to solve. The general solution to the above equation is of the form

$$T = R \cdot C \cdot N \cdot \ln(f(V_{DD,}V_{th})) \tag{3.8}$$

For N=2, equation (3.7) gives,

$$T = 4RC\ln\left[\frac{V_{DD} - \sqrt{(2V_{th} - V_{DD})(3V_{DD} - 2V_{th})}}{2(V_{DD} - V_{th})}\right] \tag{3.9}$$

From equations (3.8) and (3.9) it can be seen that the delay of the oscillator gets modified by a correction term that is given by $\ln[f(V_{DD},V_{th})]$ and the frequency gets modified by the inverse of the correction term.

Table 3.1 shows the aspect ratios of the transistors in the delay stages. The oscillator is configured as shown in Figure 3.1. For the given sizes and a control voltage of 0.9 V (chosen arbitrarily) the ring oscillates at a frequency f_0 of 620 MHz. The input signal to be divided was injected into the tail transistor of the first stage; the strength of the injected signal was -3 dBm. The locking range for divide-by-4 was determined using transient simulations in SpectreRF. The design was implemented using the IBM 7RF 180

Table 3.1. Delay cell transistor sizes

Load Transistors (M1,M2)	4μm/0.55μm
Latch Transistor (M3,M4)	3.6μm/0.20μm
Input Transistors	2.2μm/0.20 μm
Tail Current Transistors	5μm/0.3 μm

Table 3.2. Locking ranges for different latch transistor sizes

Size of Latch Transistor	**Locking Range (GHz)**
3.6μm/0.6μm	0.5
3.6μm/0.4μm	0.8
3.6μm/0.2μm	1.15

nm standard CMOS process. The locking range is shown in Table 3.2; it increases as the latch size increases. However, the natural frequency of oscillation decreases with an increasing latch size.

It can be observed that the first stage of the oscillator acts like a mixer while the others act like a low-pass filters. Since the non-linearities generated in the first stage are more important since it determines the maximum possible phase shift, the ILFD still achieves a wide locking range even if the latches are removed from the second and third stages. This decreases the load on the delay stages and helps achieve a higher frequency of oscillation for a given power dissipation, which translates to better power efficiency for the divider. The delay stages, however, see different loads, which might lead to higher flicker noise upconversion. By removing the latches from the second and third stages, the frequency of oscillation was increased to 1.1 GHz and the divider was capable of dividing frequencies between 4 GHz and 4.9 GHz down by four. In both cases, the core power dissipation was 1.2 mW from a 1.8 V power supply.

3.2 Process and Temperature Stabilized (PATS) Ring Oscillator Design

Following the previous section, the frequency of oscillation of the modified symmetric delay element based ring oscillator can be expressed as,

$$f_0 = \frac{1}{R \cdot C_{Total} \cdot N \cdot \ln[f(V_{DD,} V_{th})]} \tag{3.10}$$

where R represents the load resistance, C the total capacitance, N the number of stages and V_{th} the switching threshold of the latches. The replica feedback biasing sets the lower limit of the output swing to the control voltage (V_{Cntrl}) and upper limit to V_{DD}, so f_0 is given by [29],

$$f_0 = \frac{I_d}{N \cdot (V_{DD} - V_{Cntrl}) \cdot C_{Total} \cdot \ln[f(V_{DD}, V_{th})]} \tag{3.11}$$

where, I_d is the total current through the load element. Drain currents for channel lengths of small dimensions follow short-channel equations. For a fairly large gate-source voltage (V_{gs}) the electric field in the channel is much greater that the saturation electric field (E_{sat}) and the drain current loses its dependence on the channel length [30]. Under such conditions, the magnitude of the drain current of the PMOS devices can be expressed as,

$$| I_d | = \frac{1}{2} K_p' W (V_{gs} - | V_{th,p} |) E_{sat} \tag{3.12}$$

The V_{gs} of the PMOS load devices can be expresses as,

$$V_{gs} = V_{DD} - V_{cntrl} \tag{3.13}$$

The replica-bias circuitry sets the lower swing of the ring oscillator to V_{cntrl} and the upper limit is V_{DD}. Using (3.13) and (3.12) in (3.11), we have,

$$f_0 = \frac{\frac{1}{2} K_p' W (V_{DD} - V_{cntrl} - V_{thp}) \cdot E_{sat}}{N \cdot (V_{DD} - V_{cntrl}) \cdot C_{Total} \cdot \ln(f(V_{DD}, V_{th}))} \tag{3.14}$$

Equation (3.14) shows the dependence of *f* on process and temperature due to V_{thp}, K_p', E_{sat} and W. The trend in variation of these parameters with process and temperature is given in [31]. Our goal is to generate V_{cntrl} in such a way that the variation of *f* over process and temperature changes is minimized.

The device sizes and the V_{cntrl} required for achieving a natural frequency of oscillation with minimal variations around 625 MHz over the temperature range of -20°C to 100°C and the nominal process corner was initially determined using simulations. Power dissipation plays a major role in the choice of device sizes and V_{cntrl}. Simulation shows that the threshold voltage V_{th} is a weak function of process and temperature, therefore the term containing it can be neglected. f_0 can now be expressed as a product of two terms (1 and 2) given by [24], each of which are dependent on process and temperature,.

$$f_0 \alpha \frac{V_{DD} - V_{cntrl} - V_{thp}}{V_{DD} - V_{cntrl}} \cdot \frac{\frac{1}{2} K_p' W \cdot E_{sat}}{N \cdot C_{Total}} \tag{3.15}$$

Assuming a constant V_{cntrl} with temperature, *f* depends on the products of term 1 that has a negative slope with temperature and term 2 that has a positive slope with temperature. Term 2 of equation (3.15) depends on K_p' which varies with temperature primarily due to the change of mobility with temperature [31],

$$K_p' = \frac{K_{po}'}{T^{1.5}} \tag{3.16}$$

V_{thp}'s dependence on temperature can be expressed as,

$$V_{thp} = V_{thp,o} - m_{VT} \cdot T \tag{3.17}$$

where $V_{thp,o}$ and K_{po}' are the threshold voltage and K_p' at absolute zero, respectively. V_{thp} decreases with temperature with negative slope m_{VT}. Thus, term 2 in (3.15) increases with increases in temperature (assuming V_{DD} and V_{cntrl} stay constant with temperature). There exists a bias point (V_{cntrl}) and a device size for which the variations in terms 1 and 2 cancel out as predicted in [32]. Further, both terms 1 and 2 depend on the process. Thus, their temperature dependence varies across process corners. For the ring oscillator, it was determined that a V_{cntrl} of 0.86V, for a load device aspect ratio of 4 μm/0.55 μm, was the bias point required to cancel the variation of the bias current (and hence the frequency) with temperature due to the change in mobility and threshold voltages.

After selecting the bias point required for canceling temperature variations for the nominal process corner, the next step is to compensate the ring oscillator over process variations. Term 1 of (3.15) varies with process due to changes in threshold voltage whereas term 2 varies due to changes in K_p'. For typical CMOS processes, changes in K_p' due to process (mainly due to the variations in t_{ox}) are well controlled compared to the variation in threshold voltage [30]. Therefore, the variation in frequency due to the first term is much larger than the variation due to the second term. The V_{cntrl} generation circuitry to compensate for process and temperature is shown in Figure 3.4. The transistor M_1 provides a reference voltage (V_{TREF}) to the part of the circuit that generates the V_{cntrl} for the ring oscillator boosted up by the non-inverting gain stage. M1 is biased using a temperature-insensitive current reference that can be generated as in [25]. The voltage V_{TREF} tracks the change in threshold voltage due to process variations. Thus, V_{cntrl} changes with process to track the changes in V_{thp} with process.

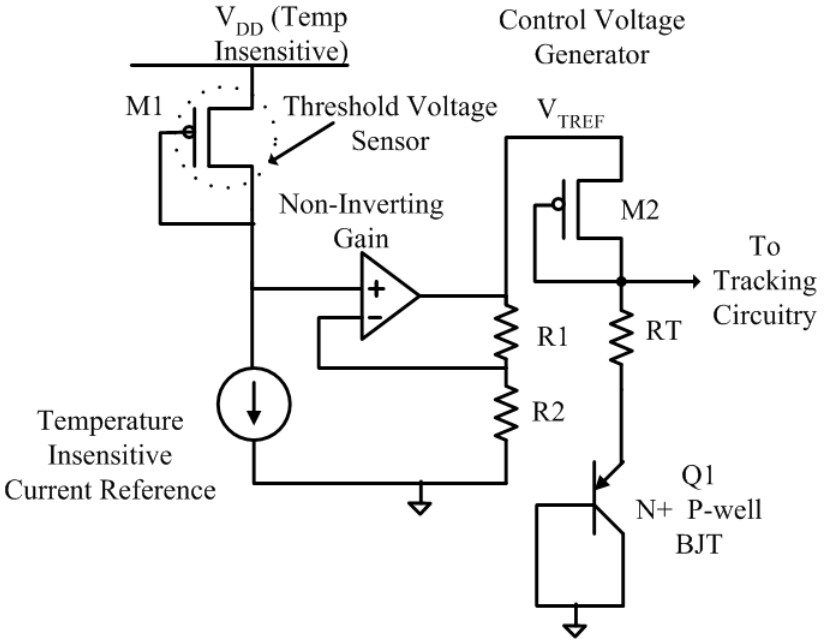


Figure 3.4. Process and temperature compensation circuitry

As a first step we will address the effect on *f* due to the first term of (3.15), as the change due to the V_{thp} dominates the changes in *f* due to K_p'. If the changes in V_{cntrl} were to exactly compensate for the changes in V_{thp} over process, the numerator of the first term would be independent of process. The denominator, however, is still sensitive to process variations, due to changing V_{cntrl}. We therefore derive a condition, which when satisfied, cancels out the variation of the first term with process corners at least to a first order. The first term can be expressed as in [27] and [28] for the nominal case and any process corner in the set {FF, SS, FS, SF},

$$f_{nom} \alpha \frac{V_{DD} - V_{cntrl} - V_{thp,nom}}{V_{DD} - V_{cntrl}} \tag{3.18}$$

$$f_{process} \alpha \frac{V_{DD} - (V_{cntrl} + \Delta V_{cntrl,process}) - (V_{thp,nom} + \Delta V_{tp,process})}{V_{DD} - (V_{cntrl} + \Delta V_{cntrl,process})} \tag{3.19}$$

For all process corners the change in V_{cntrl} is in the opposite direction to that of the change in the threshold voltage of the PMOS transistor, V_{thp}. V_{cntrl} is chosen to be 0.86V for the reasons stated above.

To cancell the frequency variation due to the first term in (3.15),

$$f_{nom} = f_{process} \tag{3.20}$$

After performing some simple math we arrive at the following condition,

$$\frac{\Delta V_{cntrl,process}}{V_{DD} - V_{cntrl}} = \frac{\Delta V_{thp,process}}{V_{thp,nom}} \tag{3.21}$$

The change in V_{thp}, $\Delta V_{th,process}$ from its nominal value $V_{thp,nom}$ is found for all the process corners through DC simulations in HSPICE using foundry-provided BSIM3 V3.2 transistor models. This information is used to set $\Delta V_{cntrl,process}$ such that (3.21) is satisfied for all the process corners. The aspect ratio of transistors M_1, M_2 and resistors R1, R2 were used to achieve the required values of ΔV_{cntrl}, over all process corners.

At this point we have achieved our first goal, so we now turn our attention towards our second goal, compensating the second term in (3.16) for process variations. The second term is expressed as (3.22) after some minor modifications to (3.25),

$$f \propto \frac{\frac{1}{2}\mu \cdot c_{ox} W \cdot E_{sat}}{N \cdot (C_{gs,terms} + C_{gd,terms})} \tag{3.22}$$

where K_p' is expressed as the product of mobility (μ) and oxide capacitance (c_{ox}).The gate capacitance term dominates the total capacitance equation and is proportional to c_{ox} and width of the device (W). Therefore, these terms are expected to have a proportional change with process. An exact expression for the change in the above parameters with

process that accounts for all short-channel effects [33] becomes quite complicated and mathematical optimization becomes tedious. It is much easier to solve the above problem through simulations using accurate foundry provided models in HSPICE that implements the BSIM3 V3.2 equations. The changes in frequency of the ring oscillator around the nominal value after achieving the first goal quantify the changes in frequency due to the second term in equation (3.15).

At this point it was found that the oscillator had already attained a value close to the required stability to implement an ILFD that locks over a wide frequency range over process corners. This indicates that second term in equation (3.15) does not have a significant impact on the natural frequency of the oscillator. The stability characteristics over process are further enhanced by noticing that terms 1 and 2 of (3.15) have opposite dynamics for the majority of process corners and hence (3.21) can be further adjusted to compensate small variations due to (3.22). The circuit used to compensate process variations (figure 3.4) imparts temperature dependence on V_{cntrl}. For the size and bias of M2 required for process compensation, it was found that V_{cntrl} had a positive slope with temperature. This can be compensated using the negative slope of V_{BE} of a BJT. Also, the slope of V_{cntrl} with temperature changes with process. This can be addressed by adjusting RT and the aspect ratio of M2 such that the frequency deviation around the nominal process corner at room temperature is minimized.

3.3 Tracking and Calibration Circuitry

Modern radios, used in the third and fourth generation wireless standards, are required to support multistandard and multiband operation for backward compatibility between various generations of standards and increased capacity [13]. This requires divider operation in a wide range of frequency bands and channel bandwidths for fully integrated PLL frequency synthesizers to work properly under process variation and operating conditions. Increasing the strength of the latch to achieve a wide locking range reduces the free running frequency of the oscillator [10]. The tail current shown in Figure 3.1. needs to be increased to counter this problem. Thus, dividing multi-GHz frequencies and achieving a wide locking range by using oversized latches is a power-hungry solution. The tracking/calibration circuit is used to extend the locking range of the ILFD without over-sizing the latches and hence reduces power dissipation.

The tracking/calibration circuitry adjusts the natural frequency of oscillation thereby shifting the locking range up or down. It can do so by either sensing the control voltage to the VCO or using a digital control word at power-up. In the former case it is referred to as the tracking circuitry and in the latter case as calibration circuitry. For covering a wide band of frequencies over process and temperature variations in modern day low-voltage CMOS processes, the VCO is implemented with very high gain. This is detrimental in terms of phase noise [34]. Therefore, VCOs with wide tuning range are often implemented as a combination of digital and analog tuning circuits to reduce the VCO gain [13]. The digital tuning scheme thus divides a wideband tuning range into smaller bands. The continuous tuning control is the control line for the PLL. A PLL calibration

circuit is used to assign the proper subband for a given channel frequency so that the PLL can lock with in the tuning range. The same calibration circuit that assigns a digital word at power up to control the VCO tuning range can also generate a digital control word to control the locking range of the ILFD. This is possible only if the ILFD is itself capable of maintaining lock over a certain band of frequency with process and temperature variation.

3.3.1 Tracking Circuitry

The V_{cntrl} generated by the process and temperature compensation circuitry is converted to a current in the tracking circuitry. The tracking circuitry shown in Figure 3.5 takes the control voltage to the VCO, when integrated into a PLL based frequency synthesizer, as an input and produces logic signals UP, UPB, DOWN and DOWNB that control the switches of charge-pump like circuitry. The logic level of these signals depends on voltage levels "V1" and "V2" that can be programmed externally. If the VCO control voltage is between the range 0-"V1", an additional current of 2μA is pumped in to the resistor in addition to the current $V_{cntrl}/R1$(usually >> 2μA). This increases the control voltage to the ILFD to a level that is approximately 50 mV above V_{cntrl}. Thus, the natural frequency of oscillation of the ring oscillator is reduced. When the VCO control voltage is between "V1" and "V2" the switches S1 and S2 are both "off" and the control voltage to the ILFD is maintained at V_{cntrl}. When the control voltage to the VCO is greater than "V2", a current of 2μA is pumped out of the resistor R2 and the control voltage to the ILFD reduces by 50mV. The accuracy of the control voltage to the ILFD can be made high by employing techniques used in [17] for current mirror and charge pump matching.

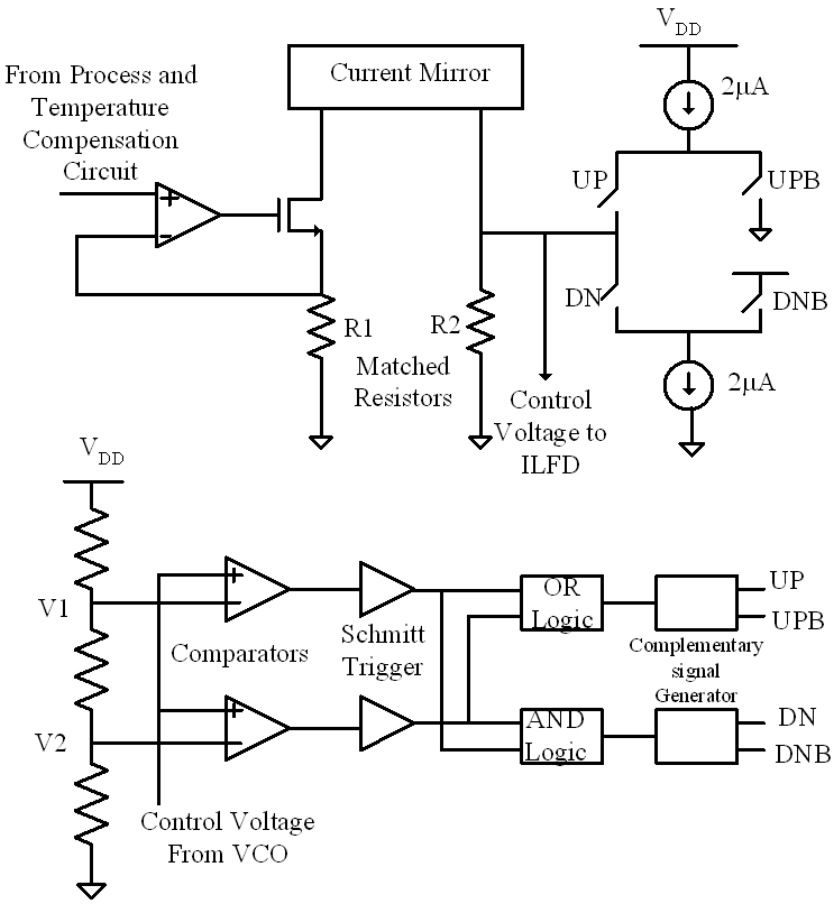


Figure 3.5. Tracking circuitry

The Schmitt trigger is used to avoid stability problems when the control voltages to the VCO equal “V1” or “V2”.

3.3.2 Calibration Circuitry

The calibration circuitry functions similarly to the tracking circuitry. The only difference is that the digital words U(0:1), D(0:1) and their complements control the voltage to the ILFD. Finer tuning capacity is added to the circuitry of Figure 3.6 so that the natural frequency of oscillation lies close to the middle of the band. This assists faster settling as discussed in Chapter 2. Through simulations across process and temperature, the digital word to achieve locking in a desired band is determined. The word can be used at power-up from basedband. The same concept could also be extended to do *automatic calibration,* as proposed in [13].

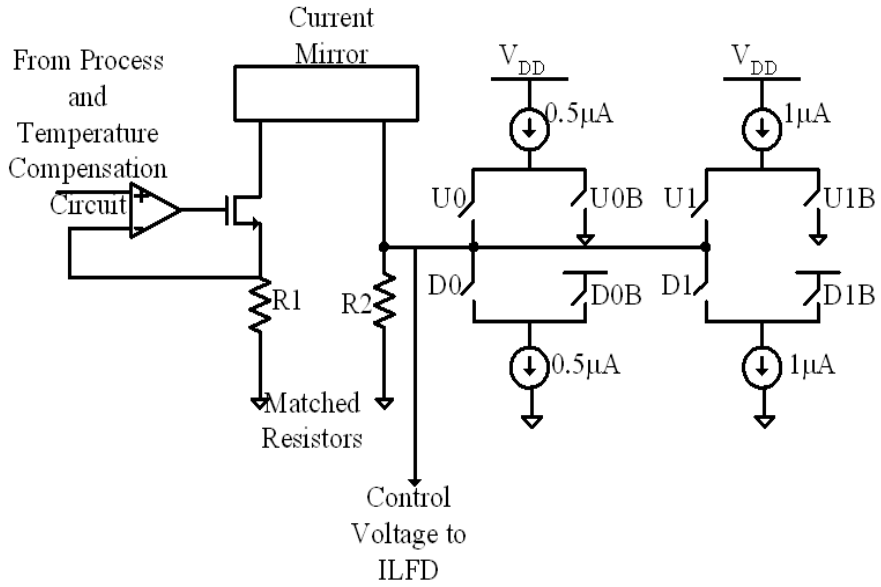


Figure 3.6. Calibration circuitry

3.4 Post-Layout Simulation Results

The ILFD is implemented using the IBM 7RF standard 0.18 μm CMOS process. Simulation is performed using SpectreRF^{TM} using foundry (IBM)-provided models. Figure 3.7 shows the frequency variation of the PATS 3-stage ring oscillator with process and temperature variation. The worst-case frequency change around the nominal process corner and room temperature is 26% without compensation. The compensation circuitry reduces the worst-case frequency deviation around the nominal corner to 4.5%. Table 3.3 provides the change in control frequency required and the change in control frequency achieved using the compensation methodology. Table 3.4 and 3.5 show the variation of predicted by theory the threshold voltage shows minimal variations with process and temperature variations. The locking range of the ILFD is determined through transient response using SpctreRF^{TM}. Transient simulations using BSIM3 V3.2 transistors models accounts for the non-linearities of the circuit. Hence, the locking range can be predicted with good accuracy although it is a time-consuming process. Harmonic balance simulations can reduce simulation time and increase accuracy [27].

Table 3.3. Achieved and required change in V_{cntrl} for process compensation

Process	**V_{th} (V)**	**ΔV_{th} (V)**	**Required ΔV_{cntrl} (V) Using (3.21)**	**Achieved ΔV_{cntrl} (V)**
TT	0.420	-	-	-
FF	0.390	- 0.029	- 0.0595	- 0.0610
SS	0.448	+ 0.028	+ 0.0574	+ 0.0620
SF	0.409	- 0.011	- 0.0232	- 0.0230
FS	0.431	+ 0.010	+ 0.0216	+ 0.0215

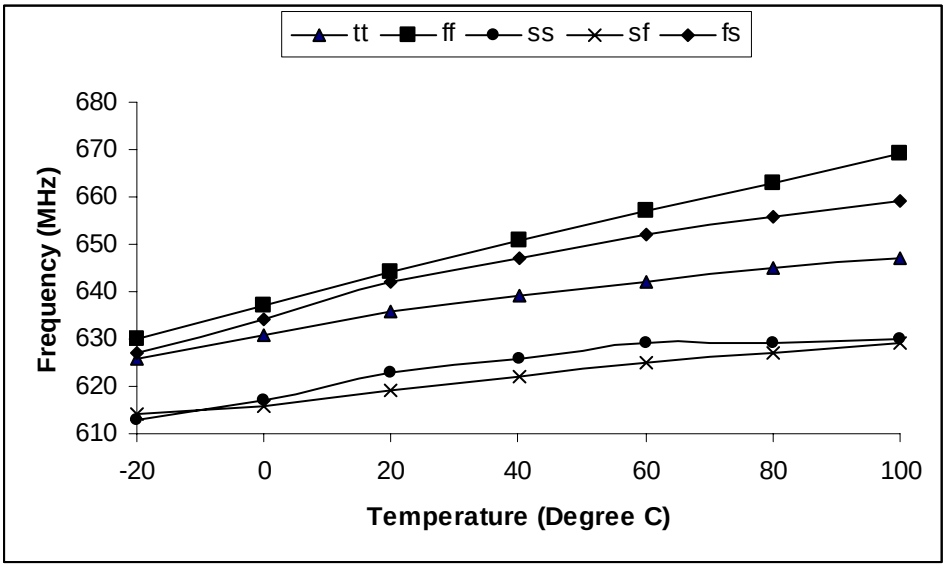


Figure 3.7. f_o variation with process and temperature

Table 3.4. Threshold voltage simulation of the delay cell across process corners

Process	Threshold Voltage (V)
TT	1.32381
FF	1.32778
SS	1.32049
SF	1.32754
FS	1.31979

Table 3.5. Threshold voltage simulation of the delay cell across temperature for nominal process corner

Temperature (° C)	Threshold Voltage (V)
-20	1.32302
10	1.32355
40	1.32408
70	1.32459
100	1.32518

For the locking range simulations we have taken into account the variation of the current produced by the current reference of Figure 3.4. A 10% change in current with process was used. An ideal current source of 10 μA, 9 uA and 11 uA was used for nominal, SS and FF process corners respectively. Table 3.6 provides the locking range of the temperature and process compensated ILFD for divide-by-4 across all process corners and a temperature range of -20°C to 100°C. A comparison of the locking range with and without the compensation circuitry for various process corners is shown in Table 3.7.

Table 3.8 shows the locking range for divide-by-6 with and without the compensation circuitry. A drastic improvement is seen due to the addition of the compensation circuitry. The worst-case power consumption of the ILFD is shown in Table 3.9. Buffers are added to drive external loads and they consume 33% of the total power. The compensation circuitry consumes 26% of the total power and the divider core consumes only 20% of the total power. Table 3.10 shows a comparison of previously published ILFDs. This table however reports only the core power consumption.

Table 3.6. Locking Range simulation for various control words

D(0:1)	UP(0:1)	Locking Range (GHz)
00	00	2.90-3.25
00	01	2.75-3.15
00	10	2.65-3.05
00	11	2.50-2.95
11	00	2.40-2.80
11	01	2.25-2.60
11	01	2.00.-2.40
11	01	1.80-2.25

Table 3.7. Comparison of locking range for divide-by-4 across process corners with and without compensation

Process Corner	Locking Range No Comp (MHz)	Locking Range With Comp (MHz)
TT	1800-2950	1800-2950
FF	2300-3500	1900-3100
SS	1300-2200	1750-2750
SF	2300-3400	1900-3050
FS	1400-2400	1800-3000

Table 3.8. Comparison of locking range for divide-by-6 across process corners with and without compensation

Process Corner	**Locking Range No Comp (MHz)**	**Locking Range With Comp (MHz)**
TT	3300-3900	3300-3900
FF	3700-4400	3450-4100
SS	2900-3500	3200-3800
SF	3600-4250	3400-4000
FS	3000-3550	3200-3800

Table 3.9. Worst-case power consumption of the ILFD, V_{DD}=1.8V

Divider Core	330μA	594 μW
Replica-Bias	310 μA	558 μW
Buffers	546 μA	982 μW
Compensation Circuitry	430 μA	774 μW

Table 3.10. Comparison with previously published ILFDs

Reference	[4]	[8]	[23]	[9]	[6]	[10]	**This Work**
Locking Range	0.06	0.01	0.2	1	0.4	1.6	**1.4**
Max Input Frequency (GHz)	2.8	18.2	1.8	10.0	2.6	7.6	**3.5**
Power Dissipation (mW)	.99	1.75	1.75	12.60	~1	6.84	**0.6**
Input Power (dBm)	-5	5	7	-	0	0	**0**
Division	4	5	2	8	4	4	**4**
Tracking/Calibration	no	no	yes	no	yes	no	**Yes**
Sensitivity of delay elements to noise	Low	High	Low	Low	High	High	**Low**
Temp., Process Sensitivity	High	High	High	High	Low	High	**Low**
CMOS (μm)	0.24	0.25	0.5	0.18	0.25	0.18	**0.18**

CHAPTER 4

2.4-GHZ FREQUENCY SYNTHESIZER BASED ON PROCESS AND TEMPERATURE COMPENSATED RING ILFD

This chapter starts with an introduction to PLL based frequency synthesizers. Key implementation issues related to the implementation of the voltage controlled oscillator (VCO), phase frequency detector (PFD), charge pump, loop filter, multi-modulus divider and the digital sigma-delta modulator are discussed. Simulation results of the key blocks of the PLL are presented. This is followed by the simulation of the noise performance of the entire fractional-N frequency synthesizer using MATLAB.

4.1 PLL Based Frequency Synthesis

The PLL-based frequency synthesizer is the most popular type of frequency synthesizer for wireless communication applications, especially for multi-GHz applications [14]. Figure 4.1 shows the general block diagram of a charge-pump PLL based frequency synthesizer. The variable of interest in the case of a PLL is the phase of the signal. The block diagram shows the transfer function of each block in a PLL. The difference between a generic PLL and a frequency synthesizer is that the divider in a frequency synthesizer can be programmed to achieve various division ratios. The PLL-based frequency synthesizer is basically a feedback system that produces various frequencies by locking to a clean reference source, which is usually a crystal oscillator. The output frequency that is synthesized is given by,

$$F_{OUT} = F_{REF} * M \tag{4.1}$$

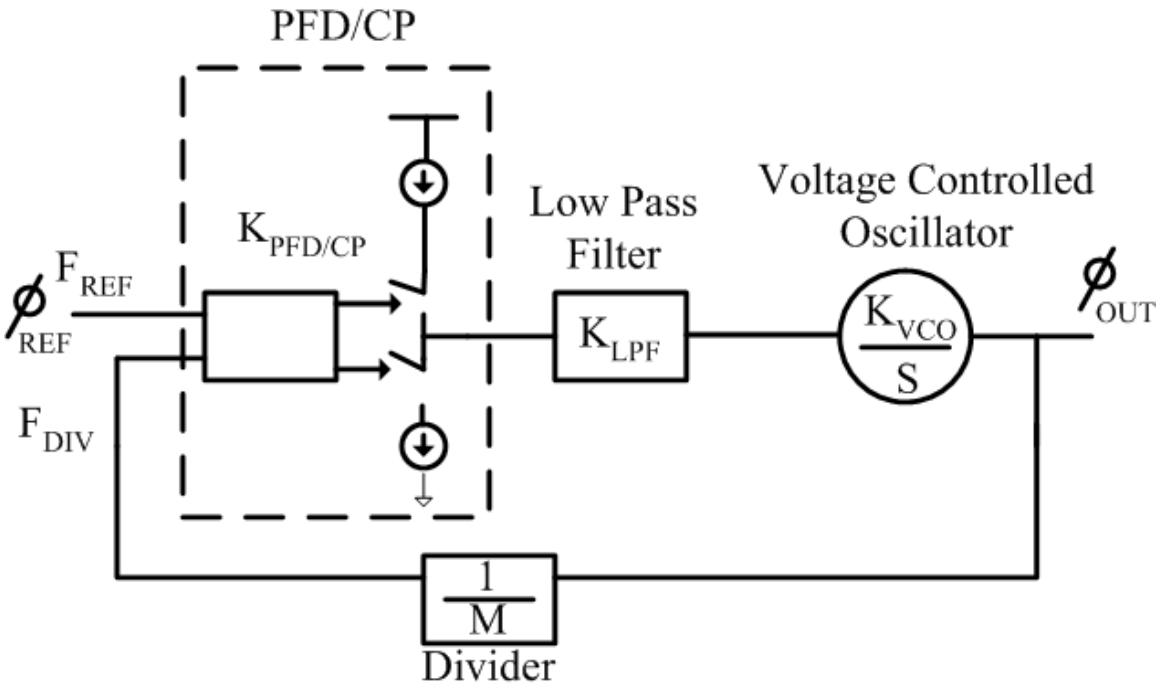


Figure 4.1. PLL based frequency synthesizers

When in lock, the signal F_{DIV} tracks F_{REF} in both frequency and phase. The dynamics of the PLL and its noise filtering property depends on the order of the loop filter. Depending on the order of the loop filter the PLL can be classified in to various categories. The open-loop transfer function of the PLL is given by,

$$H_{OL} = \frac{K_{PFD}K_{LPF}(s)K_{VCO}}{S \cdot M} \tag{4.2}$$

As seen in equation 4.2, the PLL is of order 1 even if the loop filter is a simple scalar function. The closed loop function is given by,

$$H_{CL} = \frac{K_{PFD}K_{LPF}(s).K_{VCO}}{S + \frac{1}{M}K_{PFD}K_{LPF}(s).K_{VCO}} \tag{4.3}$$

As stated earlier, charge pump based PLLs are used in a number of applications. This is because the PFD in a charge pump based PLL helps increase the lock range and speed up

the capture process. Theoretically, the locking range of such PLLs is limited by the range of frequencies the VCO can synthesize. The steady-state phase error for a charge pump based PLL is zero because the charge pump combined with the loop filter forms an integrator with infinite DC gain.

The parameter K_{PFD} of the charge pump based PLL is simply given by [11],

$$K_{PFD} = \frac{I_{CP}}{2\pi} \tag{4.3}$$

The PFD converts the phase difference between the divided-down signal F_{DIV} and the reference signal F_{REF} into a current that is converted into a voltage in the loop filter. The loop filter can be simply a capacitor, which leads to two poles at zero in the open loop transfer function and can lead to stability problems. Therefore, a resistor is always used in series with the capacitor. We begin our analysis with this simple loop filter configuration. The transfer function K_{LPF} with a resistor R1 and capacitor C1 in series is given by,

$$K_{LPF} = \frac{1 + sR1C1}{sC1} \tag{4.4}$$

The open loop and the closed loop transfer function of the PLL are now given by,

$$H_{OL} = \frac{K_{PFD} \cdot K_{VCO}(sR1C1 + 1)}{S^2 \cdot C1 \cdot M} \tag{4.5}$$

$$H_{CL} = \frac{\frac{K_{PFD}}{M} K_{VCO} R1(s + \frac{1}{R1C1})}{s^2 + s\frac{K_{PD}}{M} K_{VCO} R1 + \frac{K_{PD} K_{VCO}}{C1}}. \tag{4.6}$$

The denominator of equation 4.6 can be compared to a generalized second-order system, the damping factor of which is given by,

$$\varsigma = \frac{R1}{2}\sqrt{\frac{K_{PD}}{M}K_{VCO}C1} \tag{4.7}$$

As seen by the above equation the damping factor is increased by adding the resistor R1. If R1 is not present, the damping factor would become zero, causing the loop to become unstable.

In a charge pump-based PLL the output of the charge pump is often noisy due to the mismatches between the "UP" and "DOWN" currents. The short pulses caused due to this can produce reference spurs at the output of the PLL by modulating the VCO. Therefore a capacitor C2 is added in parallel to reduce the voltage ripple at the VCO control line. Adding the capacitor introduces a pole to both the open-loop and closed-loop transfer function (make it a 3rd-order PLL) and filters high-frequency noise and spurs. This technique of adding a pole and zero to stabilize the transfer function is usually called lead-lag compensation.

Figure 4.2 shows the pole-zero plot of the open-loop transfer function of the PLL. The frequency at which the magnitude of the open loop response reaches unity is called the unity-gain frequency (ω_U) or the loop-bandwidth. It has a zero at,

$$\omega_Z = \frac{1}{R1C1} = \frac{1}{\tau_z} \tag{4.8}$$

and a pole at,:

$$\omega_P = \frac{C1 + C2}{R1 \cdot C2 \cdot C1} = \frac{1}{\tau_P} \tag{4.9}$$

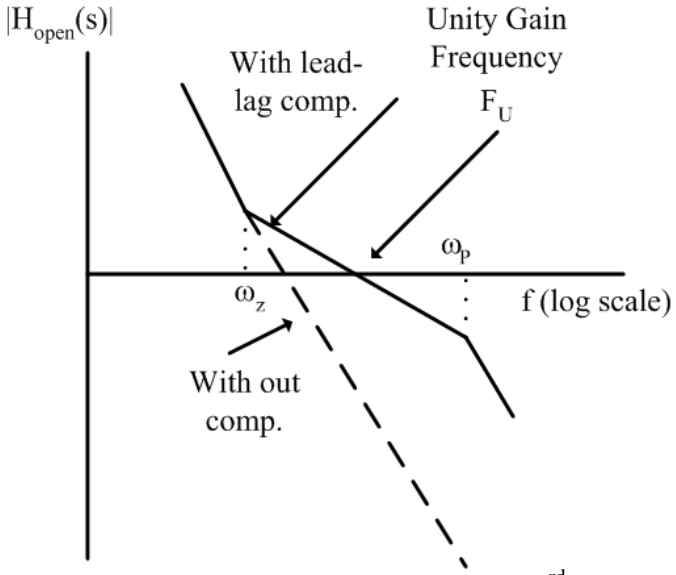


Figure 4.2. Open-loop pole-zero plot of the 3rd order PLL

The open loop transfer function now becomes,

$$H_{OL} = \frac{K_{PFD}K_{VCO}}{M}\frac{1+s\tau_Z}{s^2(C1+C2)[1+s.\tau_P]} \tag{4.10}$$

where τ_Z and τ_p are given by equations 4.8 and 4.9 respectively and $K_{PFD} = I_{CP}/2\pi$. The closed-loop function can be expressed as,

$$H_{OL} = \frac{M \cdot H_{OL}}{1+H_{OL}} \tag{4.11}$$

The crossover frequency ω_u can be approximated by,

$$\omega_u = \frac{I_{CP} \cdot K_{VCO} \cdot R1}{2\pi.M}\frac{C1}{C1+C2} \approx \frac{I_{CP} \cdot K_{VCO} \cdot R1}{2\pi \cdot M} \tag{4.12}$$

To achieve a good phase margin, the zero is placed a factor α below the loop-bandwidth (ω_u) and the pole is placed a factor β above the loop-bandwidth. The factors α and β are

usually chosen to be roughly 4. The size of the loop filter components can be expressed in terms of the other loop parameters as shown in reference [14] as,

$$R1 = \frac{2\pi \cdot M}{I_{CP} \cdot K_{VCO}} \cdot .\omega_u \tag{4.13}$$

$$C1 = \frac{\alpha}{R1 \cdot \omega_u} = \frac{I_{CP} \cdot K_{VCO} \cdot \alpha}{2\pi \cdot M \cdot \omega_u^2} \tag{4.14}$$

$$C2 = \frac{1}{\beta \cdot R1 \cdot \omega_u} = \frac{I_{CP} \cdot K_{VCO}}{2\pi \cdot M \cdot \beta \cdot \omega_u^2} \tag{4.15}$$

We now find the transfer function for noise injected in various parts of the loop to the output of the PLL. This gives an understanding how noise from various blocks of the PLL are filtered at the output. Figure 4.3 shows the model of the PLL with noise injected at various parts of the loop. The second-order loop filter will be used for the analysis. The noise transfer function from each noise source to the output of the PLL is given by the expressions (4.12) – (4.16). The current noise from the charge pump is converted into a voltage in the loop filter and modulates the VCO. The resistor R1 is usually the most significant noise contributor from the loop filter. The thermal noise from the loop filter resistor after getting transformed by the term given by the second expression of (4.20) modulates the VCO.

As seen in the expressions the noise from the reference, charge pump and feedback divider are low-pass filtered while the noise from the VCO is high-pass filtered. The noise from the resistor R1 is band-pass filtered. Therefore, the choice of the loop-

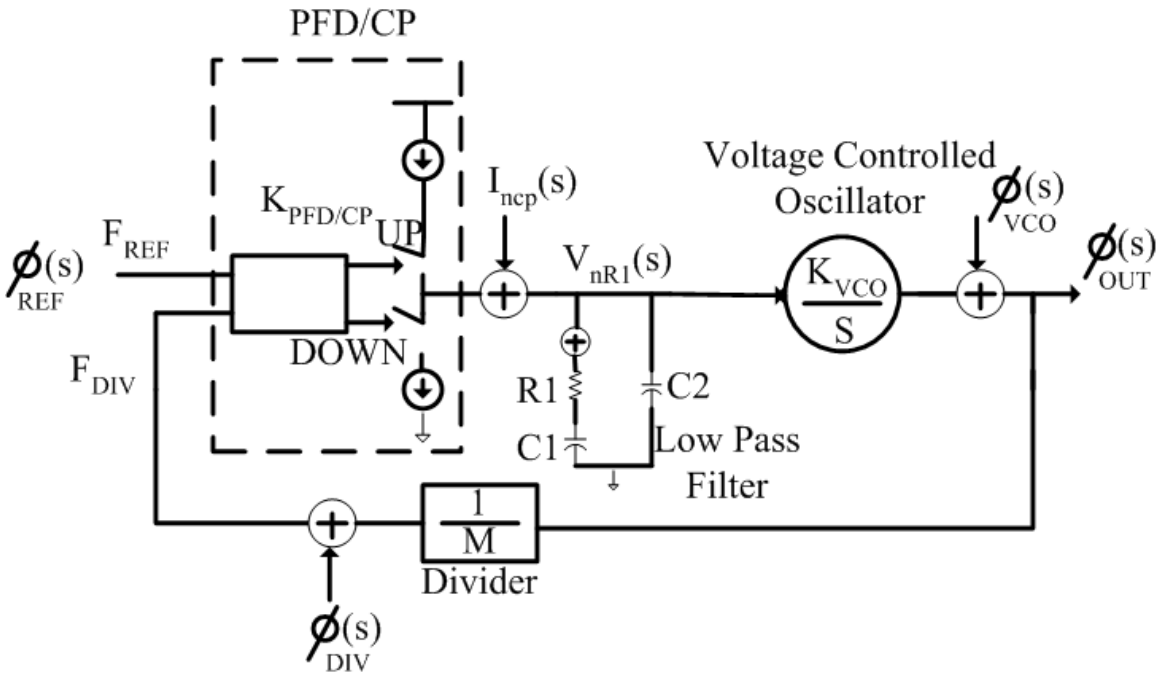


Figure 4.3. PLL model with noise injected from various blocks

$$\frac{\phi_{OUT}(s)}{\phi_{REF}(s)} = \frac{K_{PFD} \cdot K_{LPF}(s) \cdot K_{VCO}}{s + \frac{K_{PFD} \cdot K_{LPF} \cdot K_{VCO}}{M}} \tag{4.16}$$

$$\frac{\phi_{OUT}(s)}{I_{nCP}(s)} = \frac{K_{LPF}(s) \cdot K_{VCO}}{s + \frac{K_{PFD} \cdot K_{LPF} \cdot K_{VCO}}{M}} \tag{4.17}$$

$$\frac{\phi_{OUT}(s)}{\phi_{VCO}(s)} = \frac{s}{s + \frac{K_{PFD} \cdot K_{LPF}(s) \cdot K_{VCO}}{M}} \tag{4.18}$$

$$\frac{\phi_{OUT}(s)}{\phi_{DIV}(s)} = \frac{K_{PFD} \cdot K_{LPF}(s) \cdot K_{VCO}}{s + \frac{K_{PFD} \cdot K_{LPF}(s) \cdot K_{VCO}}{M}} \tag{4.19}$$

$$\frac{\phi_{OUT}(s)}{V_{nR1}(s)} = \frac{K_{VCO}}{s + \frac{K_{PFD} \cdot K_{LPF}(s) \cdot K_{VCO}}{M}} \frac{1 + \frac{C1}{C2}}{1 + s \cdot R1 \cdot (C1 + C2)} \tag{4.20}$$

bandwidth depends on which source is a significant noise contributor. Usually, the reference source has a very low phase noise in a frequency synthesizer. The VCOs noise is the significant noise source beyond the loop-bandwidth and hence the source of out-of-band phase noise in a wireless frequency synthesizer [14]. Therefore, the loop-bandwidth is chosen wide enough to attenuate the noise from the VCO. A wide loop-bandwidth however, can be detrimental in terms of reference feed-through that can be caused due to the mismatches in the charge pump [35]. The noise from the charge pump can contribute significantly to the overall phase noise even at high offset frequencies, if the loop parameters are not correctly chosen. This is illustrated with an example.

The noise at the output of the PLL due to the charge pump current noise can be expressed as (4.17). For large offset frequencies, i.e., larger than ω_p, the loop filter impedance can be approximated by $\frac{1}{s.C1}$. The equation (4.13) can now be expressed as,

$$\frac{\phi_{OUT}(s)}{I_{nCP}(s)} = \frac{2\pi \cdot M}{I_{CP}} \cdot \frac{\beta \omega_f^{\,2}}{s^2} \tag{4.21}$$

The current noise from the charge pump is converted into voltage noise by the loop filter impedance. The voltage noise modulates the VCO to produce noise sidebands at the output of the PLL. The single-sided spectral noise density can be calculated using narrowband FM approximation [14] and is given by,

$$\Im_{CP}(\Delta\omega) = \frac{1}{2}\left(\frac{2\pi M \beta \omega_u^{\,2}}{I_{CP}\Delta\omega^2}\right)^2 \times \alpha_{cp} 4kT \frac{2.I_{CP}}{(V_{GS} - V_T)_{CP}} \tag{4.22}$$

Where α_{CP} is the fraction of time that the charge pump is "on" when the PLL is locked. If the following parameters are chosen:

charge pump current = 10μA ,α_{CP} = 0.1, V_{GS}-V_T = 0.5V, β=4, and M = 64,

the singe-side phase noise at an offset of 600 KHz with a loop-bandwidth of 100 KHz can be calculated using (4.18) to be -119 dBc/Hz. This value is higher than the typical phase noise contribution from a well designed VCO. To lower the charge pump noise contribution, the "on" time of the charge pump could be lowered or the V_{GS}-V_T of the charge pump can be increased. The first action increases the spurs at the output of the VCO and the second action can reduce the output voltage range that is necessary to cover the frequency range of interest. For the purpose of integrating the loop filter on-chip, the value of resistor R1 is usually made high to reduce the value of the capacitors C1 and C2. This can also lead to a significant noise contribution at the output of the PLL. The phase noise at the output of the PLL can be approximated by,

$$\Im_{R1}(\Delta\omega) = \frac{1}{2}\left(\frac{K_{VCO}}{I_{CP}.\omega_u}\right)\left(\frac{\omega_u}{\Delta\omega}\right)^4 \times kT(4\pi.M\beta)^2 \qquad (4.23)$$

Using the above value of loop parameters in (4.23), the value of the resistor R1 and the capacitors C1 and C2 can be calculated using (4.13)-(4.15) to be 10 kΩ , 640 pF and 64 pF respectively. The SSB phase noise at an offset frequency of 600 KHz due to R1 is calculated to be 108 dBc/Hz. This number can be brought down by either increasing I_{CP} or by reducing the loop-bandwidth, which directly translates into increasing the capacitor C1 as given by (4.14). To reduce the noise by 12dB it was found that the size of the capacitor should be increases approximately. 6 times increasing its size to 4 nF. Such large sizes make it hard or even impossible to be integrated onto a chip.

A solution that reduces the output phase noise of the charge pump and the filter impedance at large offsets is to add another pole in the filter transfer function at the same frequency or at a little span from the frequency ω_p. With the addition of the extra pole, the loop transfer function falls at 60 dB /dec for frequencies beyond the frequency ω_p. This suppresses the phase noise at higher offset frequencies and allows the sizing of the loop parameters to be relaxed. The schematic of the loop filter with the additional pole added to its transfer function is shown in Figure 4.4. An extra pole is now placed on top of ω_p by making R2*C3 = τ_P. The noise contribution due to the charge pump and the resistor R1 are now given by,

$$\Im_{CP}(\Delta\omega) = kT.(4\pi.M.\beta^2)^2.\frac{2\alpha_{CP}}{I_{CP}.(V_{GS}-V_T)_{CP}}.\left(\frac{\omega_u}{\Delta\omega}\right)^6 \tag{4.24}$$

$$\Im_{R1}(\Delta\omega) = .\left(\frac{K_{VCO}}{I_{CP}.\omega_u}\right).\left(\frac{\omega_u}{\Delta\omega}\right)^6.k.T.(4\pi.M.\beta^4) \tag{4.25}$$

Equations (4.24) and (4.25) show that phase noise improves by a factor of $(\beta\omega_u/\Delta\omega)^2$ with the addition of an extra pole. The resistor R2 now contributes to the phase noise and its contribution to the phase noise at higher offset frequencies is more than that due to R1 [14]. The phase noise at the output of the PLL due to R2 is given by,

$$\Im_{R2}(\Delta\omega) = \left(\frac{K_{VCO}}{I_{CP}\omega_u\gamma}\right)\left(\frac{\omega_u}{\Delta\omega}\right)^4 kT(4\pi M\beta^2) \tag{4.26}$$

To reduce the phase noise, the size of R2 is made smaller than R1 by a factor γ and the size of C3 is made larger that C2 by the same amount. This can lead to a larger chip area.

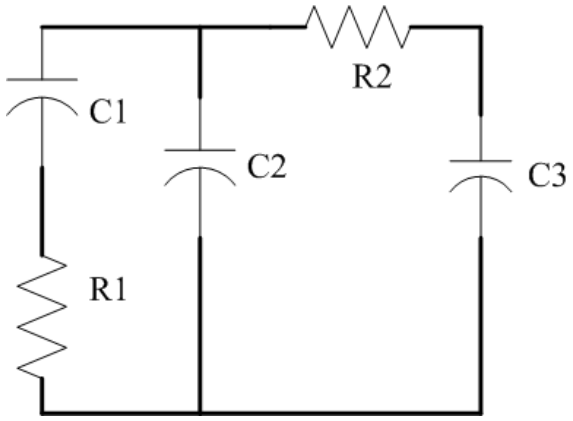


Figure 4.4 . Schematic of a 3th order loop filter

To improve the phase margin of the overall loop, the factor β is now made larger due to the presence of two poles at ω_p.

4.2 Voltage Controlled Oscillator (VCO) Design

4.2.1 VCO Architecture

The VCO in a frequency synthesizer operates at radio frequencies and consumes about 60% of the total PLL subsystem power. The phase noise of the VCO is high-pass filtered in a PLL and therefore the noise contribution to the synthesizer's phase noise at high offset frequencies (and hence the out-of-band interference) is dominated by the VCO phase noise. Due to the spectral purity demanded by radio applications an, LC or tank VCO is the most popular choice [28]. It uses the current-reuse topology consisting of both PMOS and NMOS devices, as shown in Figure 4.5. The cross-coupled pair gives the necessary negative resistance required to cancel the losses in the tank. The negative resistance is contributed by both NMOS and PMOS devices and is given by,

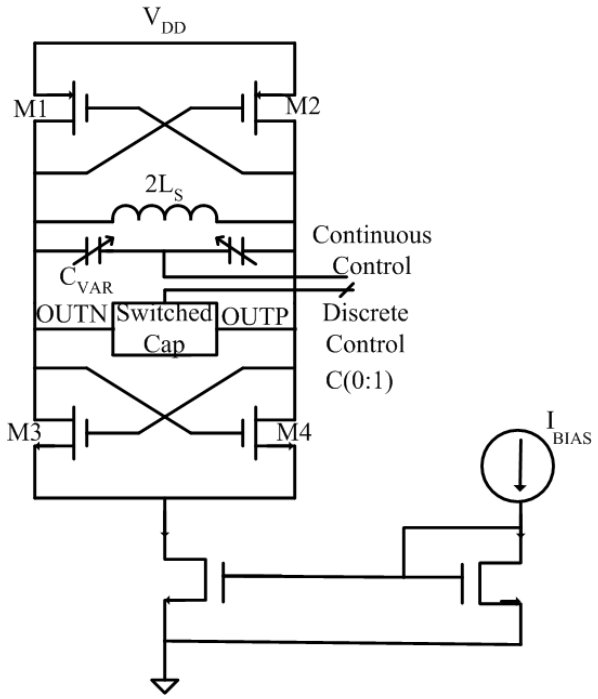


Figure 4.5. LC VCO based on current-reuse topology and band switching

$$R = \frac{-1}{g_{m,n} + g_{m,p}} \tag{4.27}$$

Hence, this architecture is leads to reduced power consumption. Increasing the current leads to an increased voltage swing across the tank (current-limited mode) until a point is reached (voltage-limited mode) where increasing the current does not improve the voltage swing anymore. The phase noise of the VCO improves in the current-limited mode and saturates (and might even become worse) in the voltage-limited mode [15]. Therefore, the VCO should be operated in the region between these limits for best phase noise performance for a given power dissipation [28]. The PMOS and NMOS devices are sized to have an equal g_m to achieve symmetry and minimize flicker noise up-conversion. The current-reuse architecture causes the voltage swing to be limited by the power supply

rails. If phase noise is the primary concern and power can be sacrificed, the PMOS-only or NMOS-only architecture is attractive [15], where swings with magnitude beyond V_{DD} could be achieved. The current mirrors used for biasing the VCO are sized 1:1 to minimize flicker noise up-conversion [11]. The reader is referred to [15, 28] for a detailed treatment on LC VCOs and their phase noise.

In modern-day CMOS processes, with low supply voltages, the gain of the VCO (K_{VCO}) needs to be very high to generate the wide range of frequencies to cover the frequency band of interest under process and temperature variations. An increased K_{VCO} renders the VCO very sensitive to flicker noise up-conversion and also to power supply and substrate noise [11, 34]. Supply and substrate noise can reach extremely high levels in a fully-integrated environment and can cause the VCO to jitter in the time domain and causes spurious sidebands in the frequency domain [35, 36, and 37]. The spurs in the frequency domain leads to increased RMS phase errors [35]. The magnitude of the spurs generated by the VCO is directly proportional to K_{VCO}. The impact of supply and substrate noise on the performance of the PLL is dealt in [36, 37]. Also, the reference noise caused due to the charge pump is a direct function of the VCO gain [35]. The VCO will therefore be implemented using the popular band-switching topology, which uses both discrete and continuous control as shown in Figure 4.6 [13]. The band-switching topology uses a digital word (coarse tuning) to shift the frequency range of operation and a fine tuning to tune (or lock) to a particular frequency. The sizes of the switches and capacitors scale in

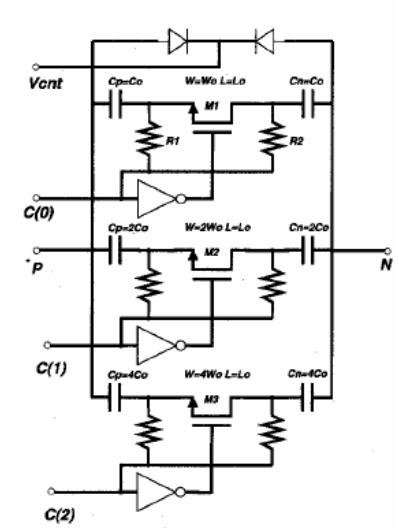


Figure 4.6. Discrete and continuous tuning of the VCO [18]

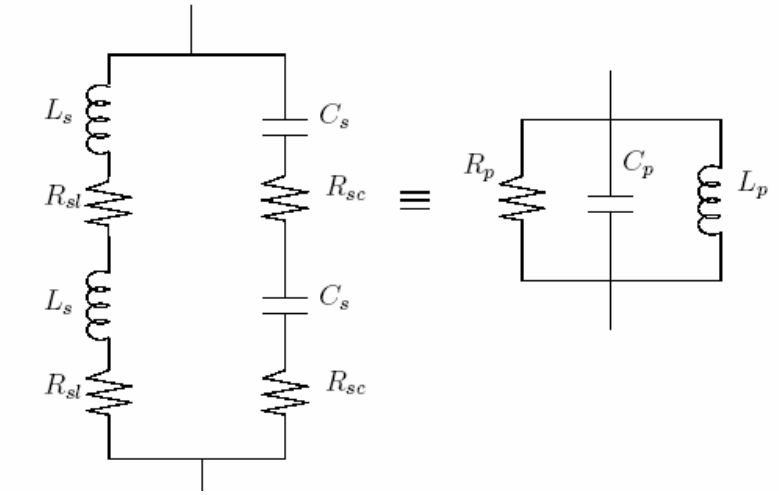
powers of two (binary weighted). Resistors are connected as shown in Figure 4.4 to prevent a drop in Q when the switches are turned "off" as explained in [13]. The resistors can be implemented using MOS devices operating in the triode region.

The phase noise of the VCO is inversely proportional to the square of the overall Q of the tank and the average power dissipated in the resistive part of the tank. The higher the voltage swing across the tank, the better the phase noise [14, 17]. The voltage swing across the tank can be maximized by either (1) increasing the L/C ratio or (2) increasing the Q of the inductors [17]. The LC tank is modeled as shown in Figure 4.7, where the expression for the equivalent parallel resistance of the tank is shown. In CMOS processes the Q of the inductors are often in the order of 8-10 due to the lossy substrate [38, 39]. Therefore, the overall Q of the tank is dominated by the inductor's Q. Differential octagonal inductors are used in the design since they have higher Q

compared to single ended inductors [38]. The IBM 7RF 0.18 μm design kit used here supports such inductors with a Q of approximately 8. Accumulation-mode MOS varactors [40, 41] are used for their wider tuning ranges.

Therefore, based on the above discussion the following steps were followed for the VCO design.

1. Choose the maximum L/C ratio to get the desired tuning range. The goal is to maximize the inductance. Once the Inductor value is obtained, implement it using the structure that gives the optimal inductance for a given area.



$$R_p \approx 2\,R_{sl}\,(1+Q_{sl}^2)$$
$$= 2\sqrt{\frac{L_s}{C_s}}\sqrt{(1+Q_{sl}^2)}$$

Figure 4.7. Model of the LC tank with integrated inductors

2. For the desired frequency, calculate the effective parallel resistance of the tank [14, 17].
3. Choose the bias current and the sizes of the PMOS and NMOS transistors to obtain a negative resistance that is 2-3 times the value required to cancel the resistance of the tank. This ensures enough gain to start up oscillations over process changes. This also leads to fast startup of oscillations.
4. Choose equal transconductance for PMOS and NMOS transistors to reduce flicker noise up conversion.
5. The bias current should also be chosen such that the VCO operates in the region between current and voltage-limited regimes.

4.2.1 VCO Simulation Results

This section provides the post-layout simulation results for the LC VCO. It was simulated using SpectreRF^{TM}. Figure 4.8 shows the tuning curves of the VCO for various control words. The K_{VCO} was found to be 190 MHz/V for the nominal corner at room temperature. The K_{VCO} varies between 210 MHz/V to 180 MHz/V across process and temperature. Figure 4.9 shows the SSB phase noise of the VCO for nominal process corners. The phase noise is -118 dBC/Hz at an offset frequency of 1 MHz drops to -130dBc/Hz at an offset frequency of 3 MHz.

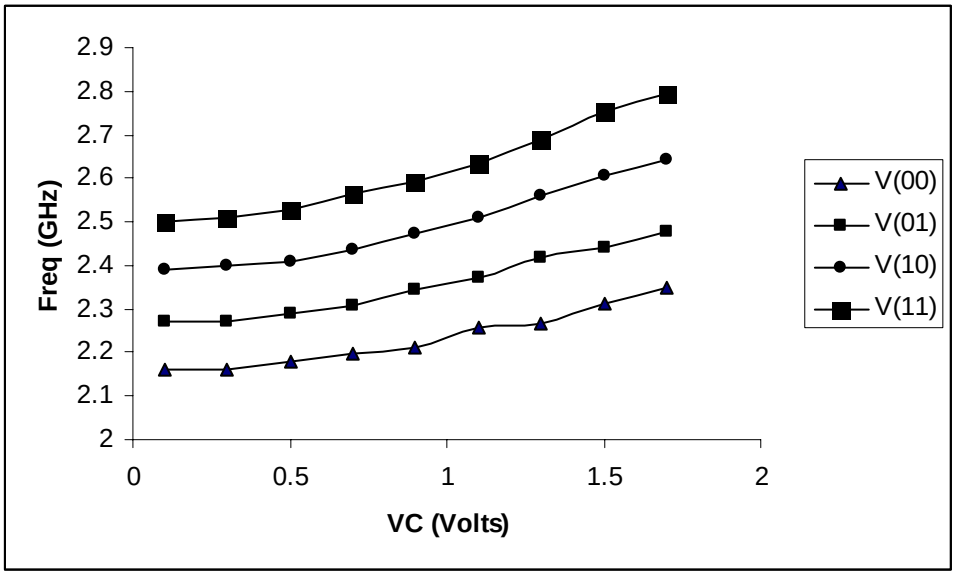


Figure 4.8. Simulated tuning range of the VCO

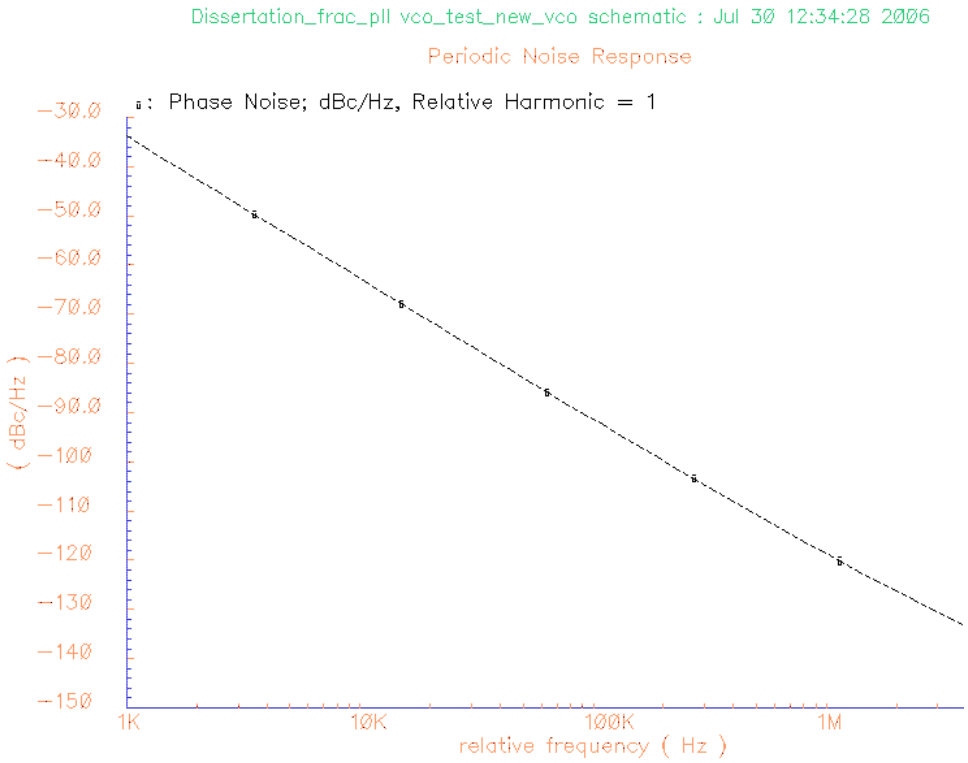


Figure 4.9. VCO worst-case phase noise

4.3 Multi-Modulus Divider Design

4.3.1 Divider Architecture

The architecture of the multi-modulus divider is shown in Figure 4.10 [35]. It consists of a chain of 2/3 divider cells connected in a ripple-counter fashion. The divider is capable of achieving a division ration of 8 to 15, depending on the digital control word P(0:2). This topology offers the following advantages:

a) lower power dissipation as the clock lines are fed to the adjacent divider cells only; and
b) highly modular design, resulting in the same circuit for adjacent divider cells. This enables layout reuse.

The block diagram of the 2/3 divider is shown in Figure 4.11. If the signal "P" is high the divider divides its input by 3, otherwise it divides by 2. To minimize the noise due to jitter accumulation in the asynchronous divider, the signal mod_0 is used to clock the PFD input. The signal mod_4 is chosen to be logic "High". The multi-modulus divider is implemented using true single phase clocking (TSPC) [15] flip-flops to minimize power consumption and to provide a larger swing compared to SCL logic. The larger swing also minimizes the phase noise of the divider. The phase noise due to the multi-modulus divider is neglected because the division ratio is moderate and the use of CMOS logic that employs a relatively high voltage swing [15]. The division ratios are given by,

$$N = 2^N + p_{N-1}2^{N-1} + p_{N-2}2^{N-2} + ... + P_0 \quad . \tag{4.28}$$

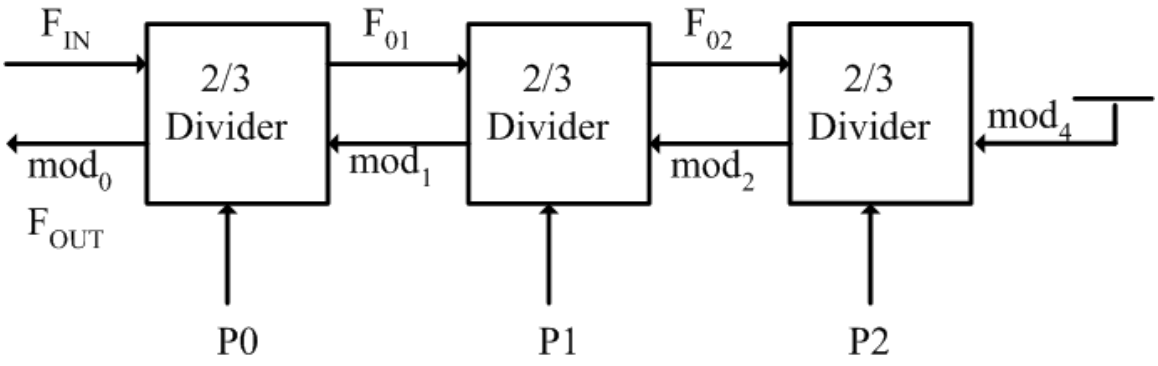


Figure 4.10. Schematic of the multi-modulus divider

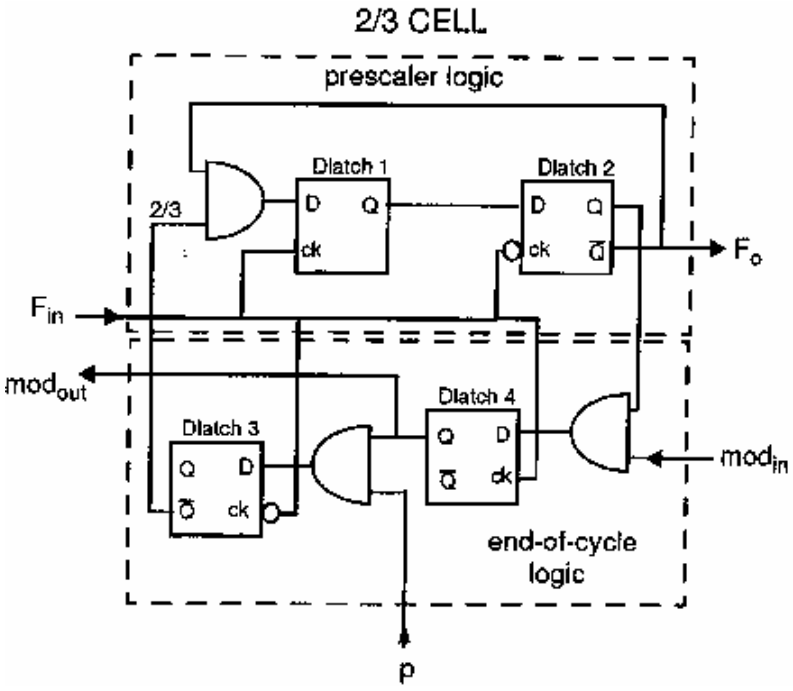


Figure 4.11. Schematic of the 2/3 divider used in the multi-modulus divider

4.3.2 Divider Simulation Results

The last cell in the chain generates the mod_2 signal which propagates "up" the chain, being reclocked by each cell along the way. An active mod signal enables division by 3, once in a division cycle provided the p input is "1". If the programming input is "0", the cell keeps dividing by 2. Despite the state of the p input, the mod signal is reclocked and output towards the higher frequency cells. The multi-modulus divider was simulated across process corners to verify correct functionality. The divider is capable of dividing between 8 for $P_0P_1P_2$ = "000" to 15 for $P_0P_1P_2$ = "111". Figure 4.12 shows the mod_n signals. The signal mod_0 has the lowest duty cycle and is used to drive the PFD. As shown in the figure the mod_2 signal has the widest duty cycle.

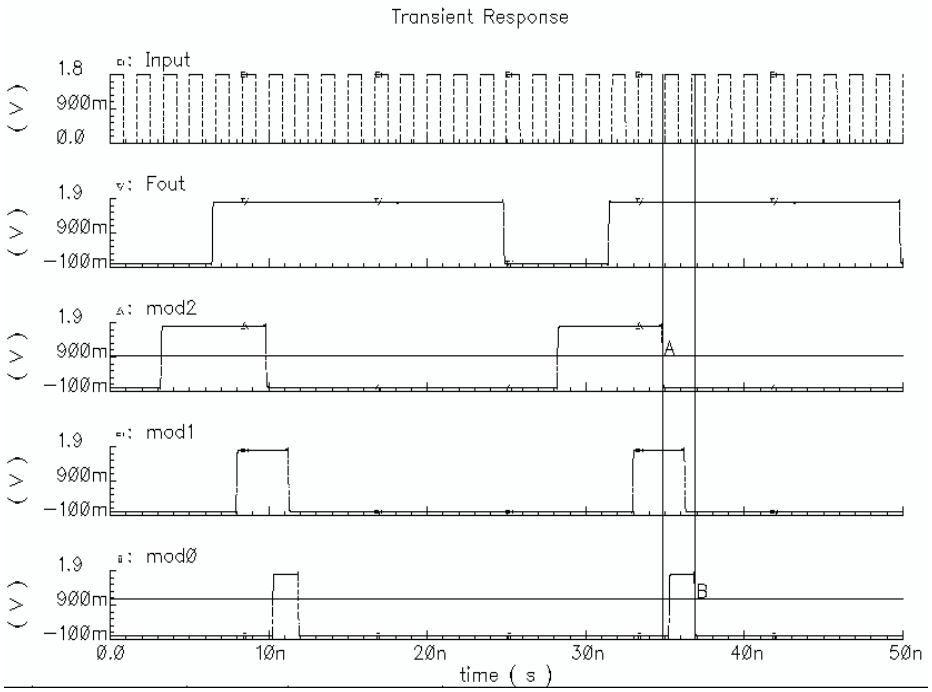


Figure 4.12. Multi-modulus divider simulation results

4.4 Charge Pump and Phase Frequency Detector

Unlike the charge pump (CP) and PFD of an integer-N PLL, additional constraints are placed on the PFD and CP of a fractional-N PLL. The sigma-delta modulator's noise is affected due to the following non-idealities present in the PFD/CP:

a. gain mismatch in Up and Down currents of the CP;

b. dynamic mismatch in Up and Down currents of the CP;

c. reset Delay mismatch in the PFD; and

d. propagation delay mismatch in the PFD;

A thorough treatment of how the above affects the sigma-delta modulator phase noise is given in [17]. The PFD/CP should be designed to minimize these effects in addition to reference spur suppression, which is caused at switching instances. The PFD/CP design of [15] is used in this work. The schematic of the CP is shown in Figure 4.13. The charge pump is controlled by the timing circuitry of Figure 4.14 to obtain fast switching and high spurious suppression.

To minimize reference spurs the following precautions are taken. The current sources are never switched off to prevent current switching effects on the drains of the current sources. When the charge pump is in the off-state, current is re-directed in to a dummy branch. Since the current sources are always "on", no start-up delay occurs and the charge pump responds immediately to changing control signals. Spurs are also caused due to charge injection from the switches as they turn on and off [42]. Using NMOS and PMOS switches in parallel and controlling them with signals that change sufficiently fast serves to minimize the spurs.

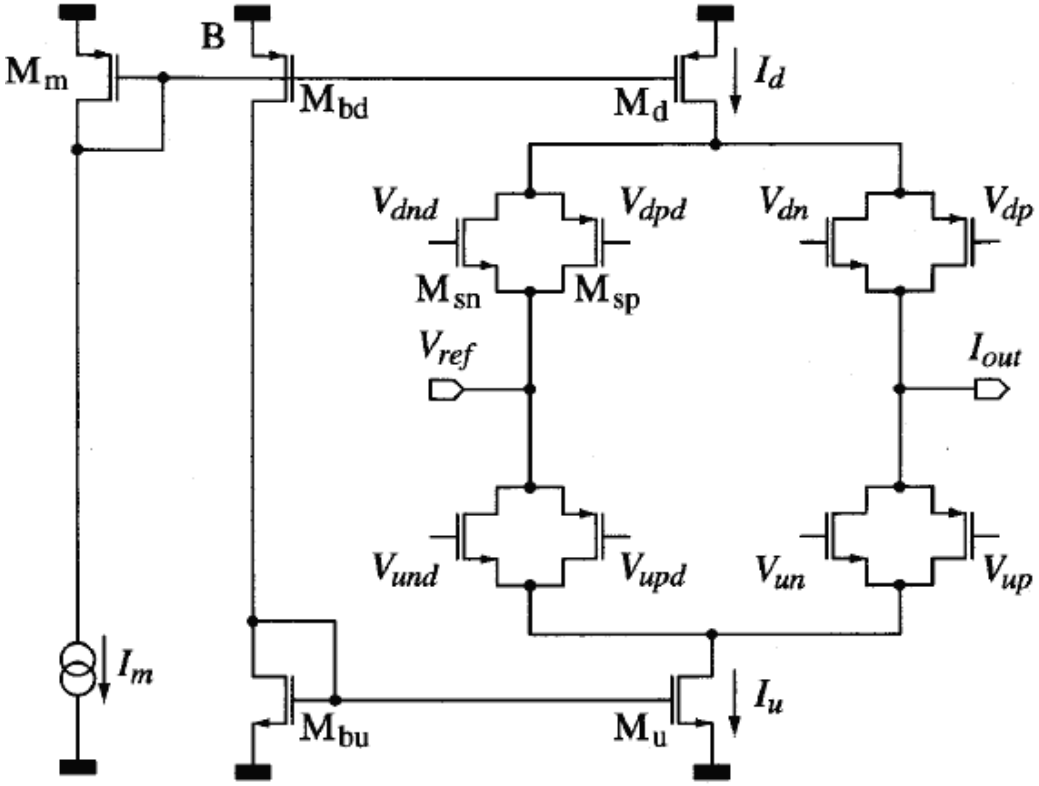


Figure 4.13. Schematic of the charge pump

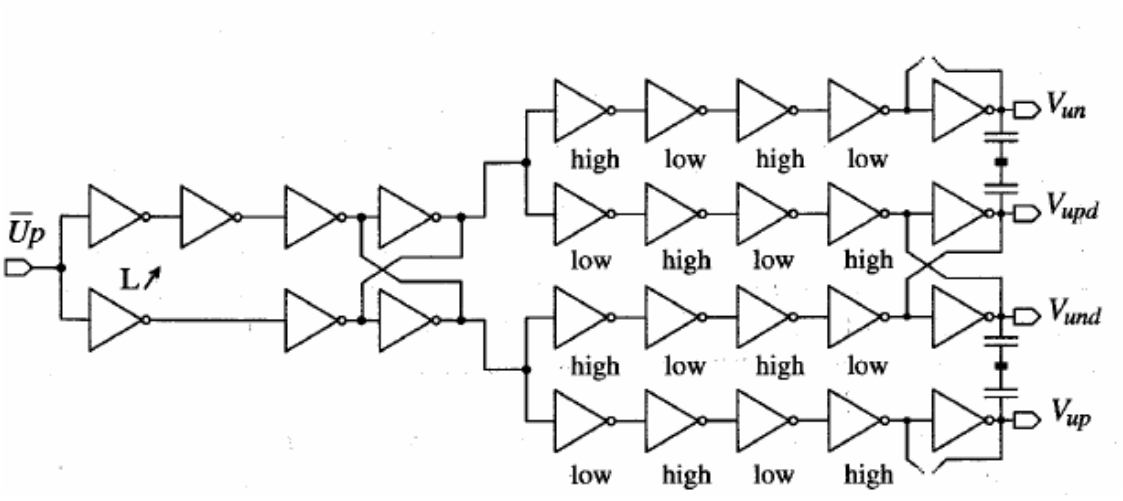


Figure 4.14. Timing circuitry for the charge pump

Latches are placed in the output of the timing control circuitry to achieve this task. To realize the control signals for the NMOS and PMOS switches, a customized control circuitry was implemented. The control signals are named in a systematic way. The first letter of the suffix u or d denotes up or down and the second letter denotes the type of switch. A suffix d is added in the end for the dummy branch. The outputs from the PFD, UPB and DOWNB, are used to generate the control signal for the charge pump. The generation of the control signals for the "up" branch is shown in Figure. Initially two signals with 180 degrees phase shift are created from UPB. To provide the same delay to both the signals, the top and bottom inverter strings are sized differently so that both have the same global delay. Latches are provided at the end of the inverter string to increase the switching speed. Both the current branches can be "off" simultaneously for a short period of time due to finite switching time. To prevent this, the dummy branch is controlled in such a way that it closes after the main branch closes and it opens before the main branch opens. This is accomplished with a group of inverters whose threshold voltages are made high or low as described in [15].

The CP gain mismatch is caused due to the current mismatch in the up and down branches. The output voltage level of the charge pump changes with time and this can further affect the current matching between the NMOS and PMOS current sources. One way to prevent this is to use cascode current sources. The mismatch in the current mirrors is primarily due to threshold voltage, V_t, mismatch and beta (β) mismatch. Assuming a device square-law relationship and assuming that the mismatch in threshold voltage and beta are uncorrelated, the mismatch in current can be formulated as,

$$\sigma^2\left(\frac{\Delta I_d}{I_d}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \frac{4}{(V_{gs} - V_t)^2}\sigma^2(\Delta V_t) \tag{4.29}$$

where,

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}} \tag{4.30}$$

$$\sigma(\Delta V_t) = \frac{A_{VT}}{\sqrt{WL}} \tag{4.31}$$

In current mirrors if,

$$V_{gs} - V_t << \frac{2A_{VT}}{A_B} \tag{4.32}$$

then the mismatch due to threshold voltage dominates over beta mismatch. Using the values of A_{VT}=5mV/μm and A_β =1.04%/μm for a typical 0 .18 μm CMOS process [17], equation (4.32) gives,

$$\frac{2A_{VT}}{A_B} = 1 \tag{4.33}$$

Equation (4.29) reduces to,

$$\sigma^2\left(\frac{\Delta I_d}{I_d}\right) = \frac{1}{WL}\frac{4A_{VT}{}^2}{(V_{gs} - V_t)^2} \tag{4.34}$$

The above equation was used to ensure good matching by sizing the devices with a V_{gs}-V_t of 300 mV, using transistor lengths greater than minimum and using multiple-finger devices. Choosing a higher value of V_{gs}-V_t results in a reduced output voltage swing at the output of the charge pump and hence a lower voltage range available to the VCO when passive loop filters are used. Active loop filters can prevent this, but they add noise. Therefore, there is a trade-off involved between the mismatch and output voltage swing.

The CP implemented in this work has a voltage swing of 0.5-1.1 V. Dynamic mismatch occurs due to the finite time involved in switching the NMOS and PMOS switch transistors "on" and "off". Decreasing the switching time using minimum size transistors for the switches and using latches in the control circuitry largely prevents this.

The PFD is implemented as shown in Figure 4.15 [15]. The classical PFD circuit is not very attractive for use in a sigma-delta fractional-N frequency synthesizer. The phase error generated by the sigma-delta modulators can vary up to 5 % (or larger dependent on the reference frequency). In conventional PFDs with lesser reset delay time, up to 5% of the available phase error range is highly non-linear. Therefore, the phase error-to-current transfer characteristic is highly non-linear, causing noise leakage and spurious tones. To combat this problem, a delay circuit consisting of inverters and capacitors as shown in the figure is introduced. This enhances the PFD sensitivity for small phase errors. A total delay of 3 ns was implemented. If the propagation delay through the NAND gate and the delay circuit is dependent on whether the up or down signal changes first, the net "on" time of the charge pump changes. This causes PFD reset delay mismatch and an increased noise level at the output of the sigma-delta modulator. Methods suggested in [17] to reduce the PFD reset mismatch errors are:

1) Prescalar output pulse width less than the minimum on-time of the CP;
2) Prescalar output pulse width larger than the maximum difference between reference and feedback edges plus reset delay;
3) DFF with reset propagation delay independent of the clock level; or
4) DFF clock level periodically alternates when the reset pulse occurs.

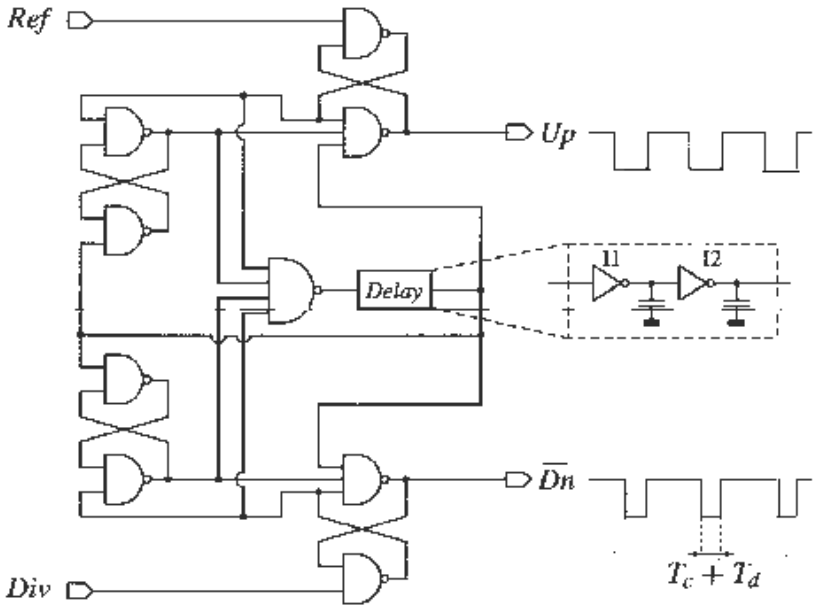


Figure 4.15. Phase frequency detector for minimizing the dead zone of the PLL

4.5 Digital Sigma-Delta Modulator (SDM)

The basic idea behind fractional-N synthesis is division by fractional ratios, instead of only integer ratios. To accomplish fractional division, the same frequency divider as in integer-N frequency synthesizer is used, but the division is controlled using a digital sigma-delta modulator (SDM) [15]. The input to the SDM is a K-bit word. The SDM is clocked using the reference clock to the PLL. The sigma-delta modulator maps the K-bit input word to an n-bit output word that controls the division modulus of the multi-modulus divider. For every reference clock cycle the divider divides by a different ratio such that the effective divide ratio is a fractional number that depends on the input K given by,

$$N_{FRAC} = N + \frac{K}{2^n} \tag{4.35}$$

where, n length of the accumulator of the sigma-delta modulator. By increasing the length of the accumulator of the sigma-delta modulator, a finer division ratio and hence finer channel resolution can be obtained. Since the division modulus changes every clock cycle the fractional-N PLL is never is locked; instead, it is said to be in quasi-lock. The average charge flowing in to the loop-filter is zero during lock [17]

The sigma-delta modulator is usually of an order greater than 2 to exhibit better randomizing properties and decrease in-band noise [15]. Lower-order sigma delta modulators with DC inputs leads to the existence of patterned noise that pose a serious problem [15]. Higher order sigma-delta modulators can be either multi-stage noise shaping (MASH) or multi-bit single-loop (MBSL) types. The sigma-delta modulator acts as a noise shaper, pushing the quantization noise to higher frequencies. The high frequency noise is rejected due to the low-pass transfer function from the output of the SDM to the output of the PLL. Employing higher-order SDMs to achieve lower in-band noise leads increases the high frequency noise that increases out-of-band noise. To reduce the effect of high frequency noise, the PLL should use loop filters whose order should be equal to or greater than that of the SDM. Thus usually 3^{rd}-order SDMs are used. The MBSL-I architecture is used in this work because of its lower high-frequency noise [15, 17] compared to the MASH-111 SDM. The variation of the division modulus to implement the same division ration is lesser for the MBSL SDMs when compared to MASH SDM. This reduces the effect of the CP and PFD non-idealities. The MBSL-I modulator to be used for this work is given in Figure 4.16. It consists of a single, 3^{rd}-order discrete time filter with feedforward and feedback coefficients, which influence the

noise transfer function (NTF). The value of the coefficients is derived from a 3rd order, high-pass Butterworth filter implementation. The implemented filter has a cut-off frequency sufficiently less than half the reference frequency. The implemented SDM has a cut-off frequency of $0.167f_{ref}$, leading to a transfer function given by [15],

$$H_{qn,b} = \frac{(1-z^{-1})^3}{1-0.968z^{-1}+0.587z^{-2}-0.106z^{-3}} \tag{4.36}$$

For ease of implementation in a standard CMOS process, the NTF is modified such that the coefficients are approximated to powers of two. The modified NTF that preserves stability and causality is given by,

$$H_{qn,b} = \frac{(1-z^{-1})^3}{1-z^{-1}+0.5z^{-2}} \tag{4.37}$$

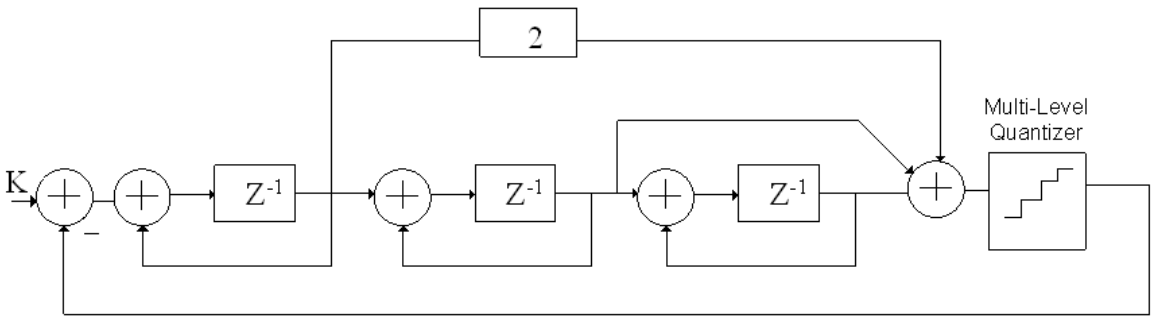


Figure 4.16. 3rd order MBSL-I sigma-delta modulator

Although the MBSL I is more complex when compared to the MASH converter, it has the following advantages (1) better flexibility in terms of noise shaping (2) lower pass band gain, which means lower high frequency quantization noise and (3) less intensive divider modulus switching in the time domain, which leads to reduced noise due to CP/PFD non idealities as discussed earlier [15, 17].

4.6 Frequency Synthesizer Implementation and Simulation

Among the applications using the 2.4-GHz ISM band, Bluetooth has the most stringent channel spacing. The specifications of a frequency synthesizer adhering to the Bluetooth standard are given below in Table 4.1. The goal is to design a frequency synthesizer to satisfy or out-perform the above specifications using injection locked prescalers to minimize power consumption. The total phase noise at the output of the fractional-N PLL using a

Table 4.1. Bluetooth specifications

Bandwidth	2402-2483 MHz
Channel Spacing	1 MHz
Switching Time	220μS
Out of Band Spurs	-47 - -30 dBm
Phase Noise @ 2 MHz	-121 dBc/Hz

digital sigma-delta modulator is given by,

$$S_{\phi,TOTAL} = S_{\phi,VCO} + S_{\phi,Divider} + S_{\phi,SDM} + S_{\phi,FILTER} + S_{\phi,CP} + S_{\phi,PFD} \ , \tag{4.38}$$

where, $S_{\varphi,X}$ denotes the phase noise contributed due to the individual blocks of the PLL. The outputs of the CP/PFD, loop filter, divider and the SDM are low pass filtered at the output of the PLL, whereas the output of the output of the VCO is high pass filtered. Therefore, the phase noise at large offset frequencies is dominated by the VCO. The noise at the output of the PLL due to the sigma-delta modulator is given by,

$$S_{\phi,SDM}(f_m) = \left|H(f_m)^2\right| \frac{\pi^2}{3F_S} \left[2\sin\left(\frac{\pi f_m}{F_S}\right)\right]^{2(n-1)} \tag{4.39}$$

where, $H(f_m)$ denotes the loop transfer function from the output of the SDM to the output of the PLL and F_S is the sampling frequency (F_{ref}). The SDM has a significant amount of high-frequency noise due to its noise-shaping property. Therefore, the loop-bandwidth has to be chosen such that their phase noise at large offset frequency is significantly less than that of the VCO. The loop-bandwidth also determines the settling time, phase noise and the spur attenuation [15, 17, and 8]. A reduction in loop-bandwidth is advantageous for reducing the phase noise due to the SDM, CP/PFD, loop filter and the divider. However, reduced loop-bandwidth leads to a slower settling time and also reduced data rate if in-loop modulation techniques need to be employed [43]. Therefore, an optimal loop-bandwidth needs to be determined.

The SDM plays a key role in determining the loop-bandwidth since the noise contribution due to other blocks can be alleviated by careful design. The expression for phase noise

due to the SDM given by (4.39) does not account for the non-linearities due to the non-ideal effects in the PFD/CP and prescaler [17]. References [17, 15] give a fast non-linear simulation technique for modeling these effects. The loop-bandwidth to reduce the SDM noise well below the VCO noise was found using a custom MATLAB code that models the above mentioned non-idealities. The parameters used to model the non-idealities were determined using simulation as outlined in reference [17]. It is found out that a 3^{rd} -order loop filter is required to minimize the effects of the MBSL-I SDM. The loop filter was designed using the method given in [23]. The phase margin of the loop was set to be 56° and the settling time was found to be 36 μs.

The custom MATLAB code was also used to determine the phase noise due to the MBSL-I SDM, phase noise at the output of the PLL due to the MBSL-I SDM and the over all phase noise at the output of the PLL (contributed by CP, VCO, reference and the divider). The above noise performance was plotted for various cases:

(a) No ILFD (division step =1);

(b) ILFD that achieves a fixed division of 4 ahead of the multi-modulus divider (division step=4); and

(c) ILFD that achieves a fixed division of 8 ahead of the multi-modulus divider (division step=8).

Figures 4.17 – 4.19 show the phase noise of the MBSL-I SDM for several steps due to division by various factors achieved by the ILFD. Simulation results show that as the division step size increases, the noise of the SDM increases. The noise increases by

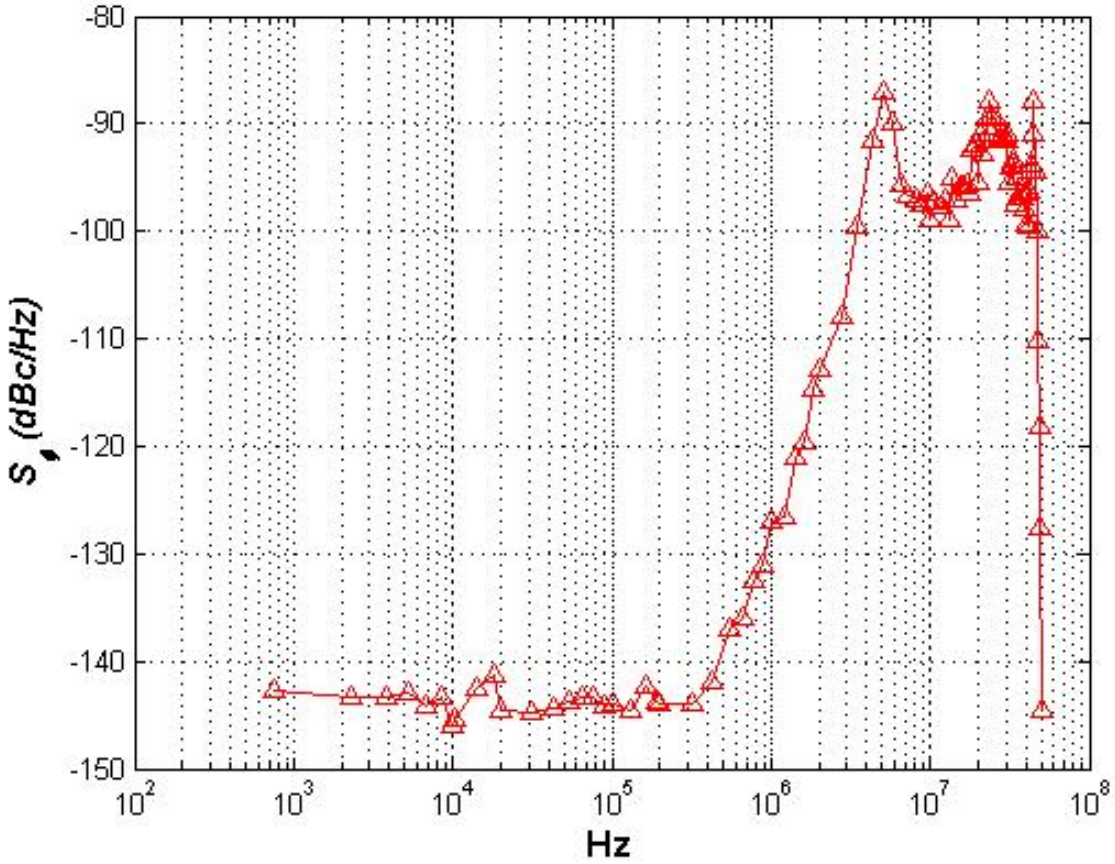


Figure 4.17. Phase noise at the output of the MBSL-I SDM with a division step=1

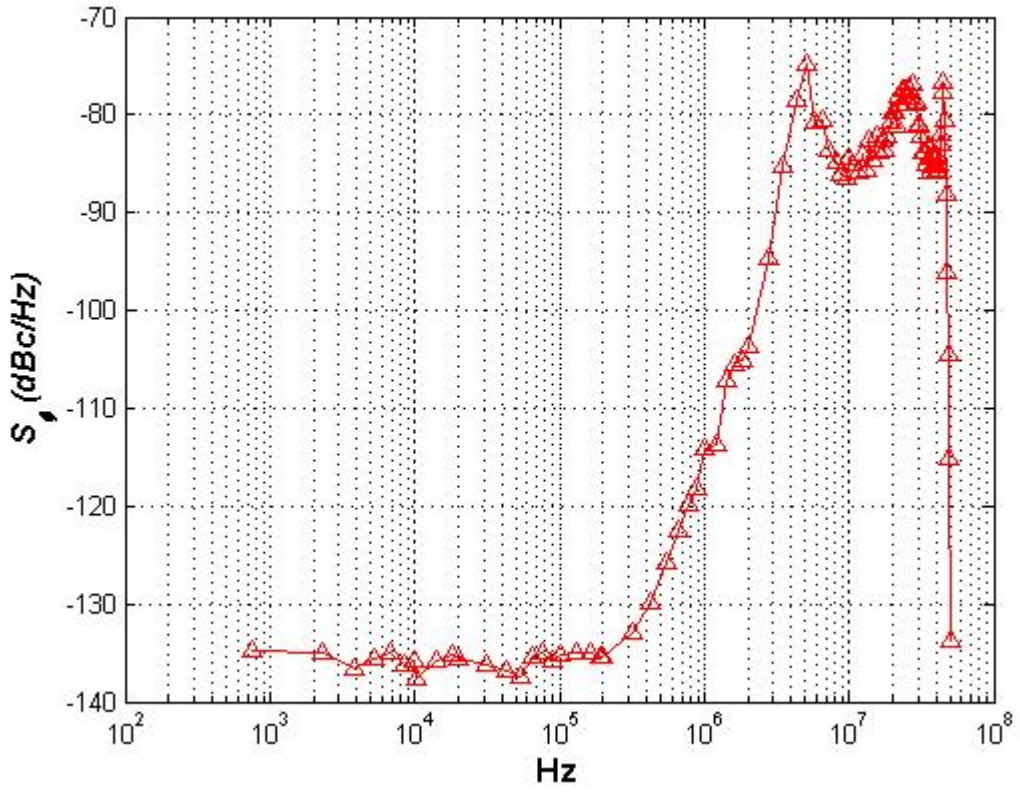


Figure 4.18. Phase noise at the output of the MBSL-I SDM with a division step=4

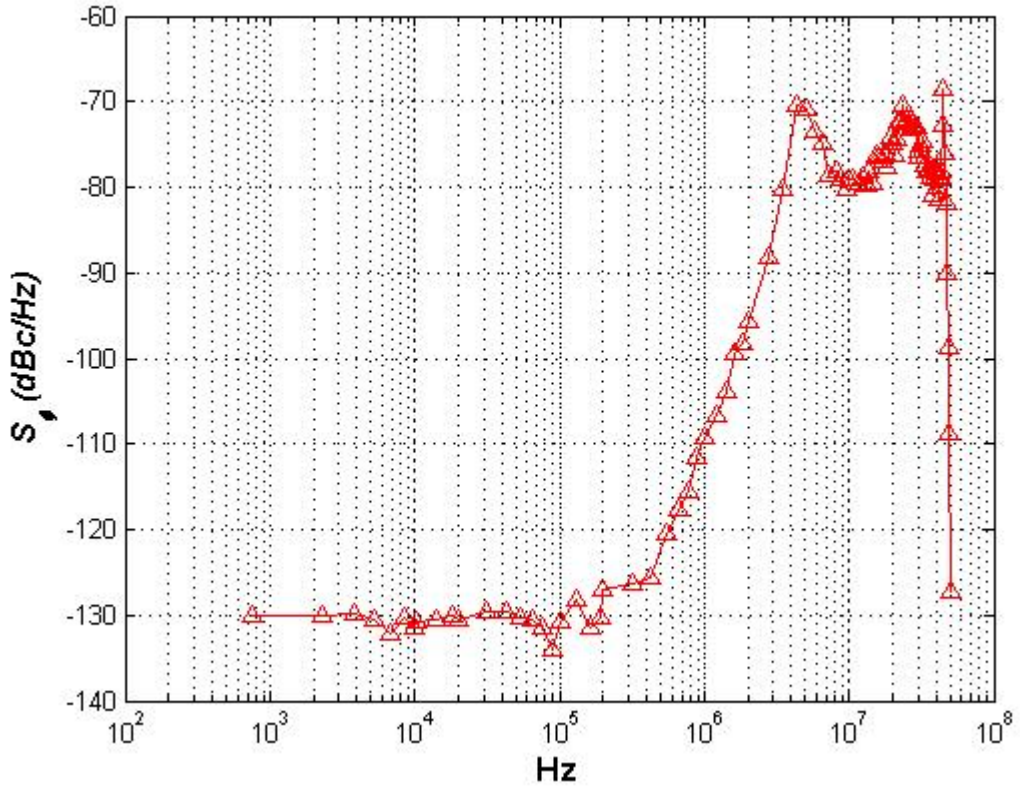


Figure 4.19. Phase noise at the output of the MBSL-I SDM with a division step=8

approximately 12 dB when the divider step increases from 1 to 8. The transfer function of the SDM to the output of the PLL is a low pass function. Therefore, the low-frequency noise appears at the output of the PLL boosted by the closed-loop transfer function. The high frequency noise (i.e noise beyond the loop-bandwidth) is attenuated. The loop-bandwidth and the order of the filter are chosen such that the noise is sufficiently attenuated at the offset frequency of interest, which in the case of the Bluetooth application is 2 MHz. The phase noise at the output of the PLL due to the SDM for the above mentioned cases is shown in Figures 4.20-4.22. The noise at the output of the PLL due to the charge pump is shown in Figure 4.23. The VCO phase noise and the noise at the output of the PLL due to the VCO are shown in Figures 4.24 and 4.25 respectively. The noise due to the charge pump and the VCO are low-pass and high-pass filtered respectively as shown in section 4.1. The loop parameters are designed such that the charge pump noise dominates the in-band noise and the VCO noise dominates the out-of-band noise, as seen from Figures 4.26- 4.28. Thus, the desired phase noise of -121 dBc/Hz at an offset frequency of 2 MHz from the carrier is met, even when the divider step is 8. Table 4.2 summarizes the PLL parameters required to achieve the required phase noise specifications.

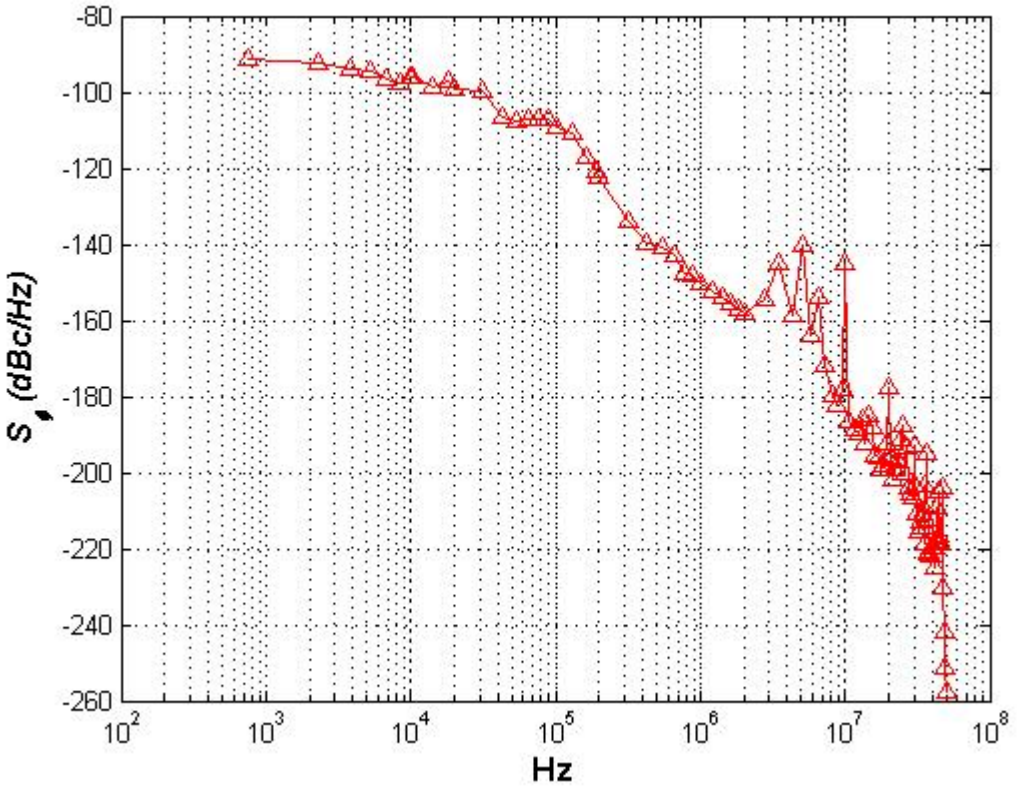


Figure 4.20. Phase noise at the output of the PLL due to MBSL-I SDM with a division step=1

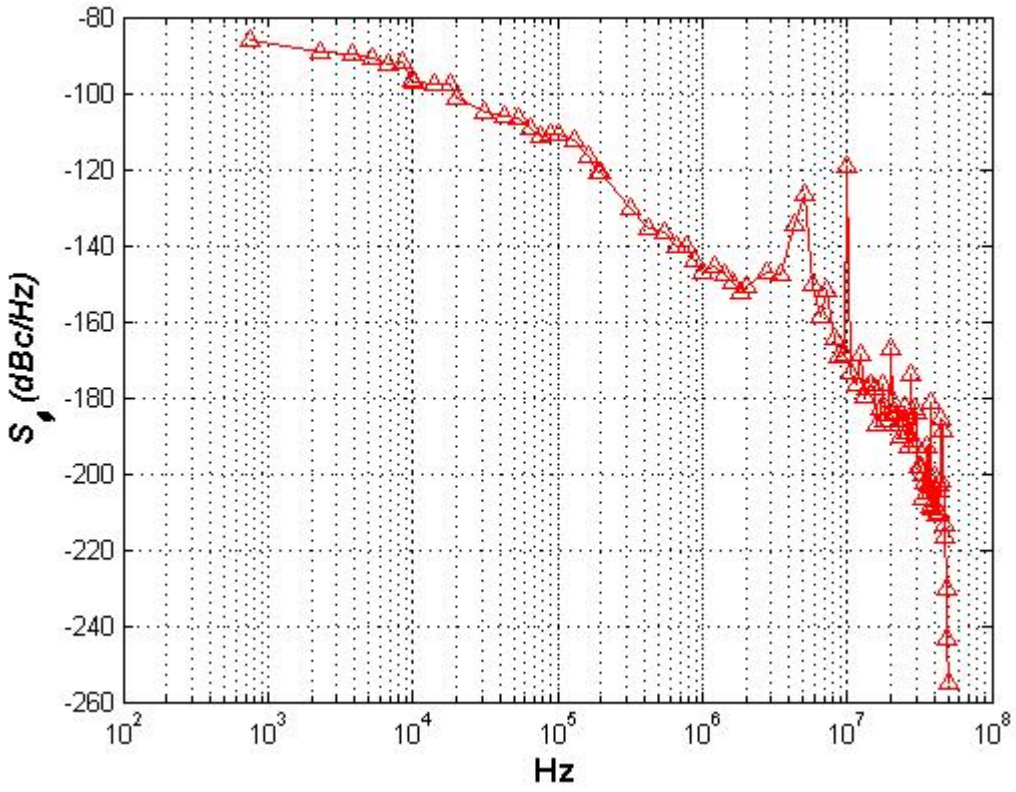


Figure 4.21. Phase noise at the output of the PLL due to MBSL-I SDM with a division step=4

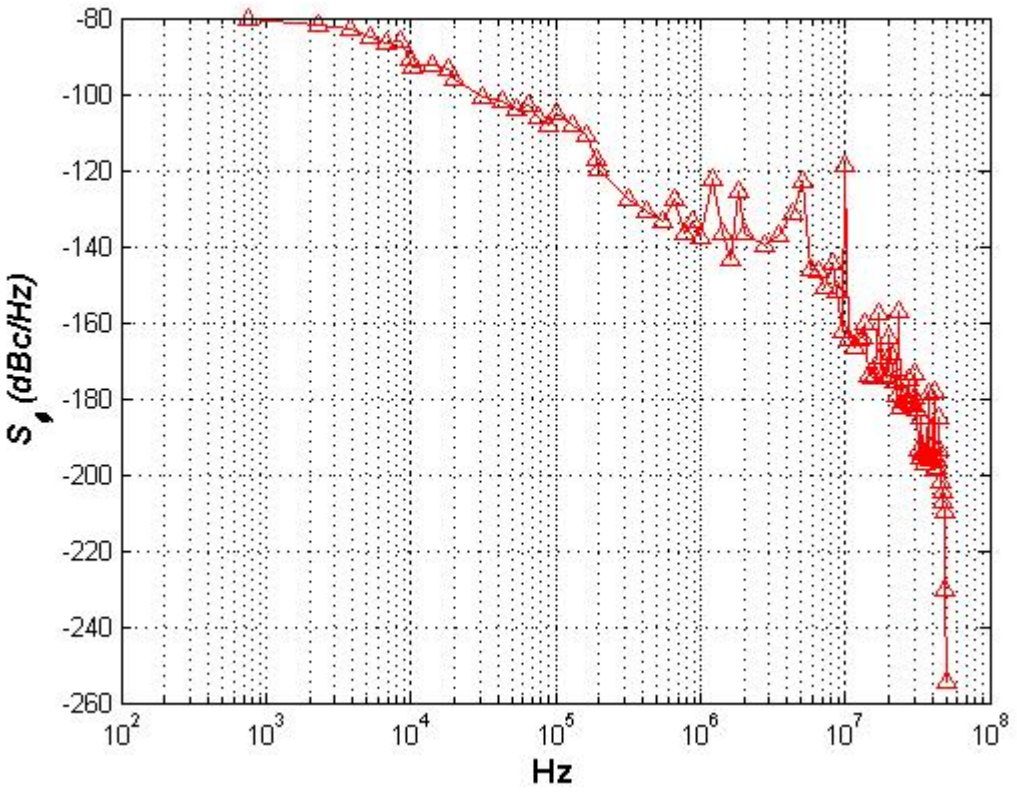


Figure 4.22. Phase noise at the output of the PLL due to MBSL-I SDM with a division step=8

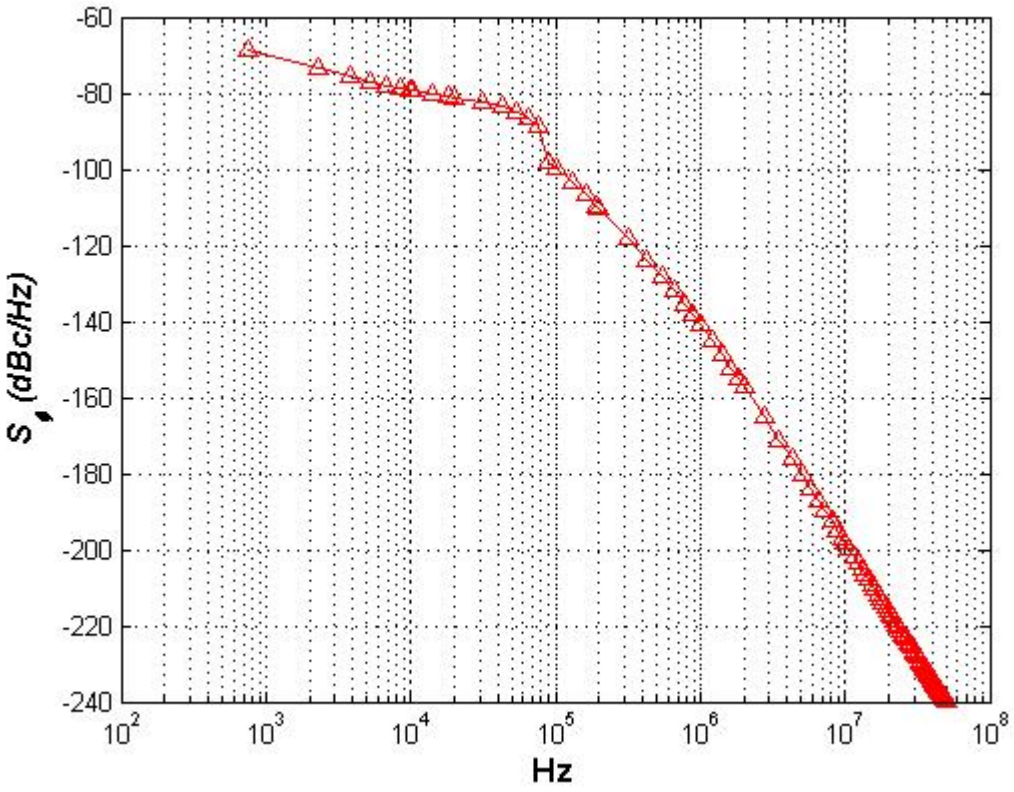


Figure 4.23. Phase noise at the output of the PLL due to the charge pump noise

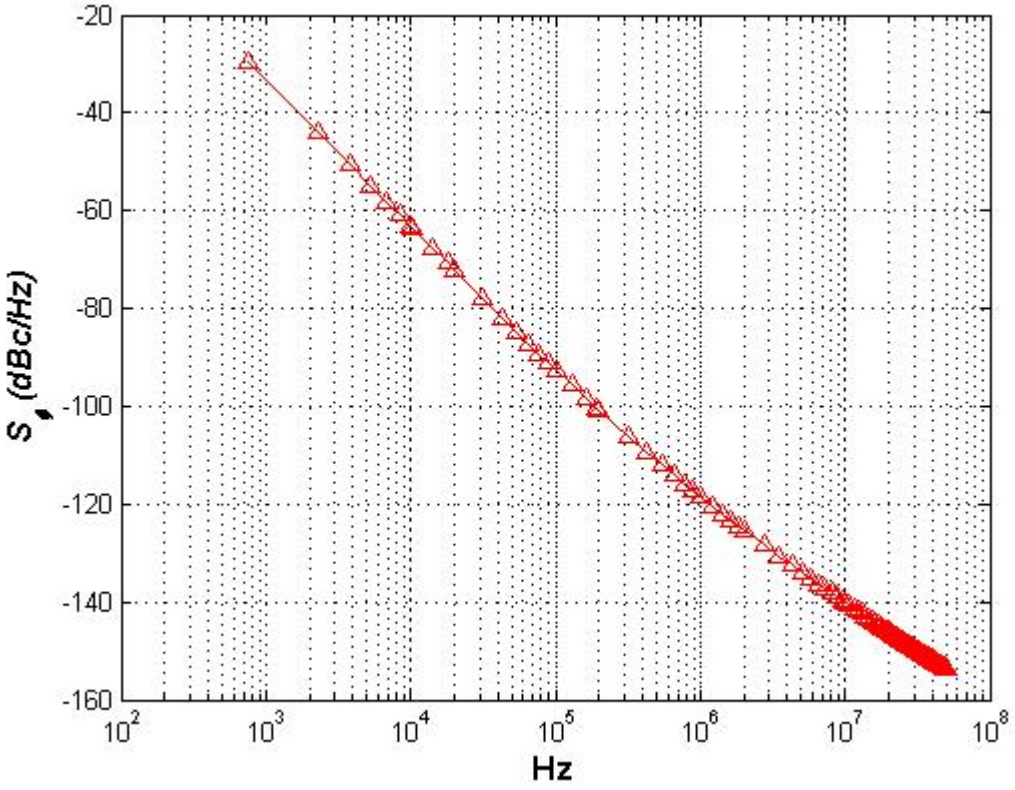


Figure 4.24. Phase noise of the VCO

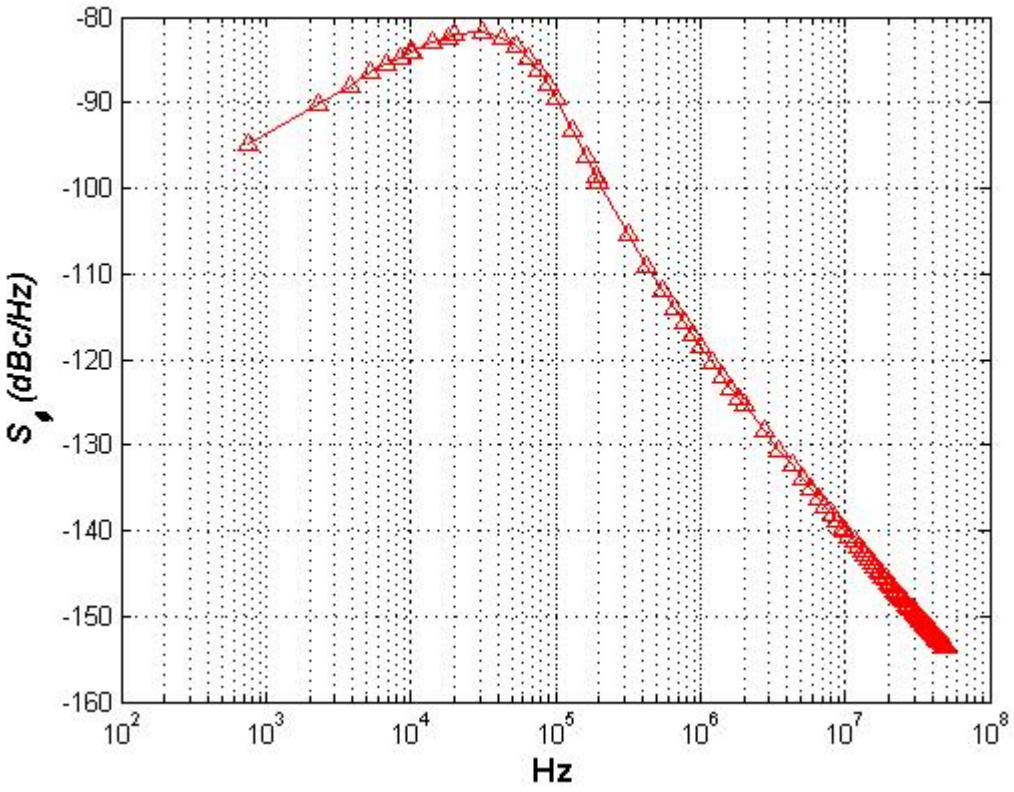


Figure 4.25. Phase noise at the output of the PLL due to the VCO

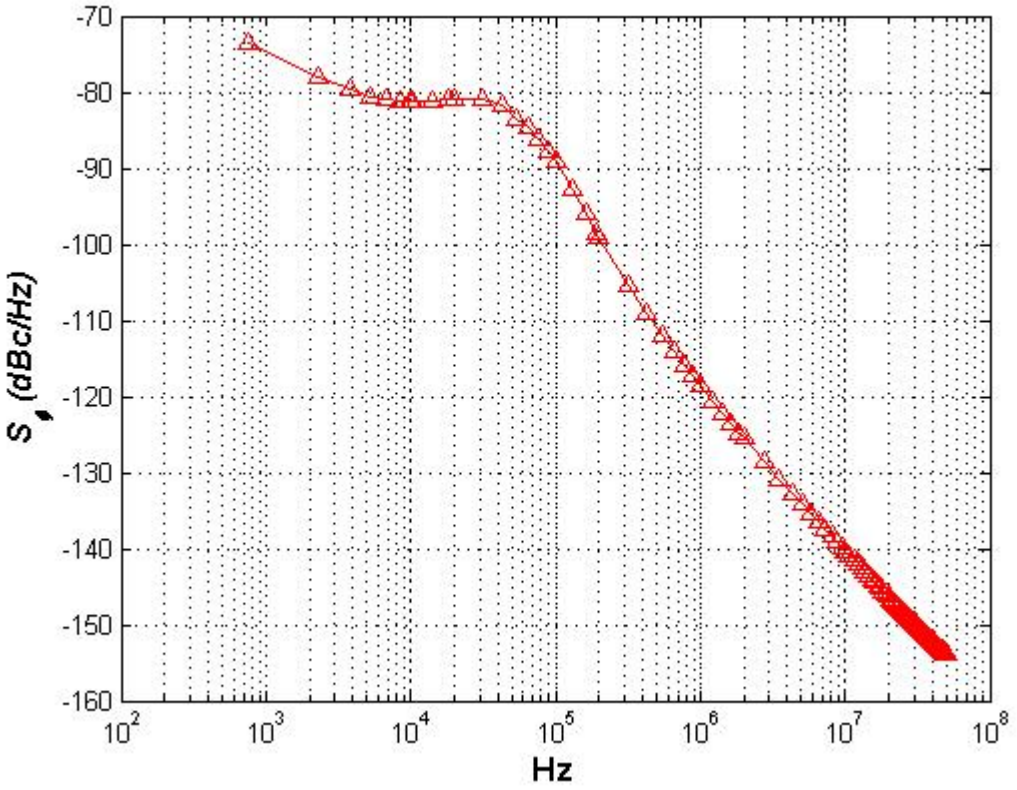


Figure 4.26. Overall phase noise at the output of the PLL due to MBSL-I SDM with a division step=1

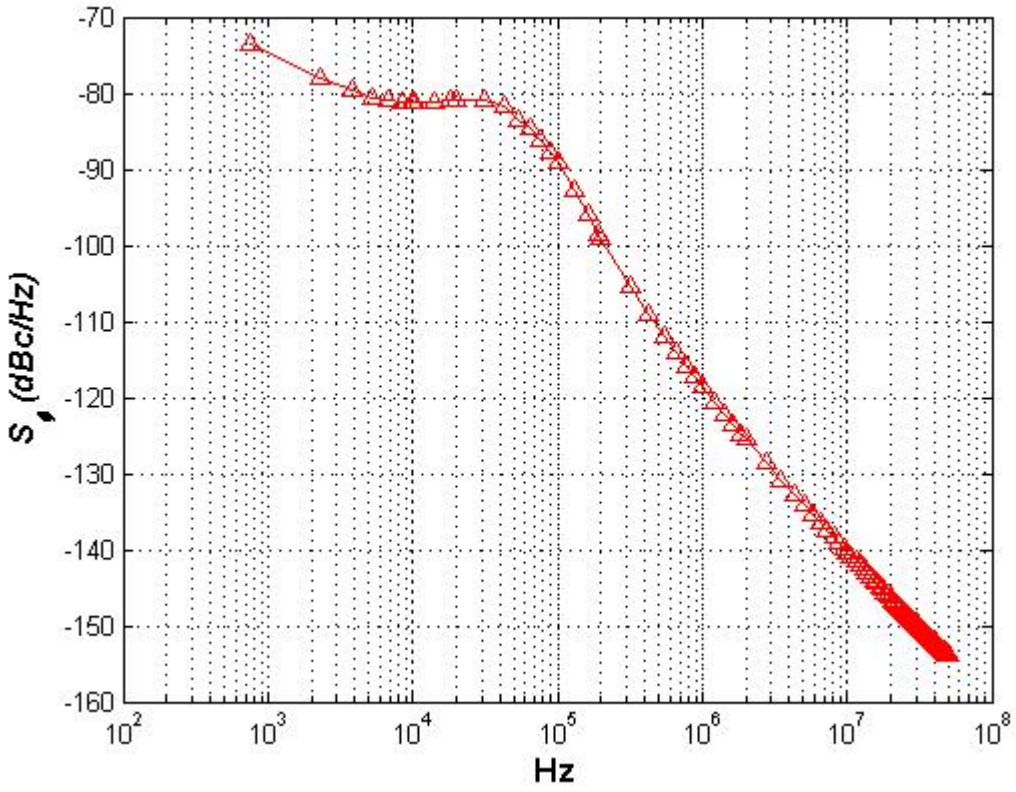


Figure 4.27. Overall phase noise at the output of the PLL due to MBSL-I SDM with a division step=4

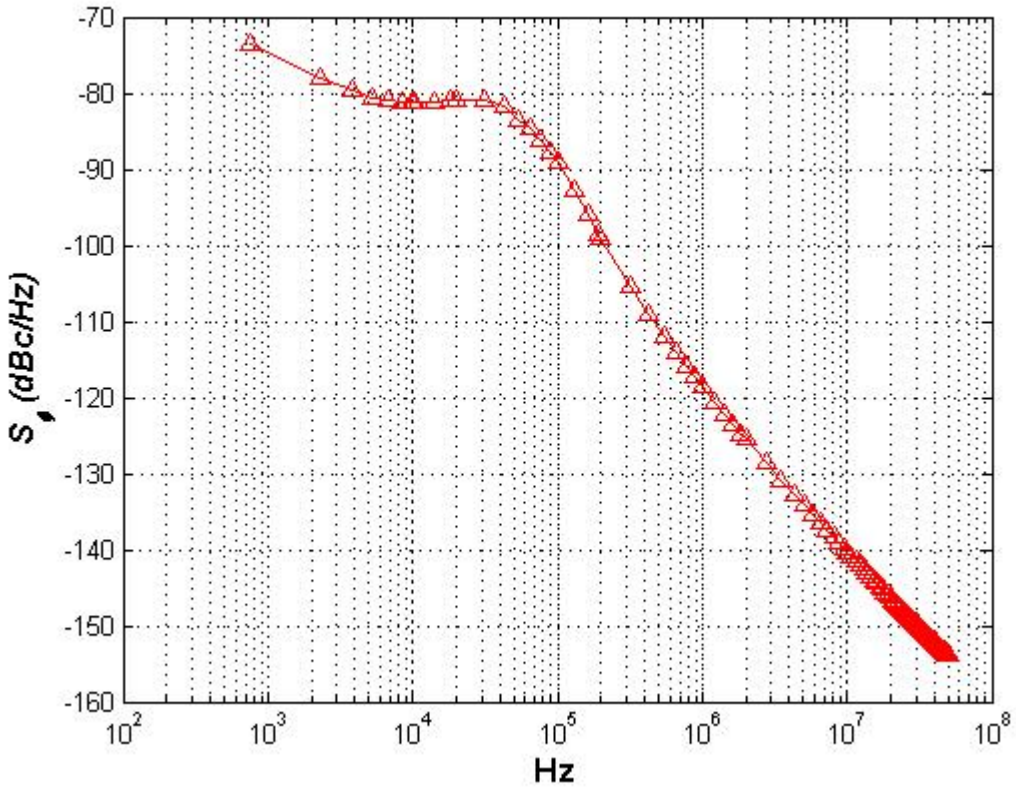


Figure 4.28. Overall phase noise at the output of the PLL due to MBSL-I SDM with a division step=8

Table 4.2. PLL parameters

Loop-bandwidth	60 KHz
I_{CP}	80E-6
C1	7nF
C2	353pF
C3	353pF
R2	1.4K
R3	1.4K
K_{VCO}	200 MHz/V
Phase Margin	56°
F_{ref}	50 MHz
Division Modulus	8-15

CHAPTER 5

CHIP IMPLEMENTATION, TEST SETUP AND MEASUREMENT RESULTS

5.1 Chip Implementation

This chapter discusses the test and characterization of the process-and-temperature compensated ILFD and the implementation of the prototype 2.4-GHz frequency synthesizer using the wideband ILFD. Fractional-N capability is provided to the frequency synthesizer even though the complete Fractional–N synthesizer was not implemented. On-wafer probing was used to characterize the ILFD. This enables multiple chips to be characterized rapidly. This technique will be discussed following the chip implementation details and the chip-testing prototype printed circuit board (PCB) design.

Figure 5.1 shows the chip microphotograph. The sensitive analog blocks are well separated from the digital blocks. The supply and the ground pins of each block are placed close to each other to avoid long loops and hence noise pickup. The bond wires that connect the digital power supply to the package are placed orthogonally to the bond wire that connect to the sensitive analog blocks. This reduces coupling of noise on the power supply line of the switching digital blocks into the power supply of the analog blocks. Thick metal wires implemented using the top metal layers are used for the power lines. It is also a good practice to use multiple pads for supply and substrate connection to reduce the inductance and hence the ground and power supply bounce. The last feature was not used here due to pin number limitations.

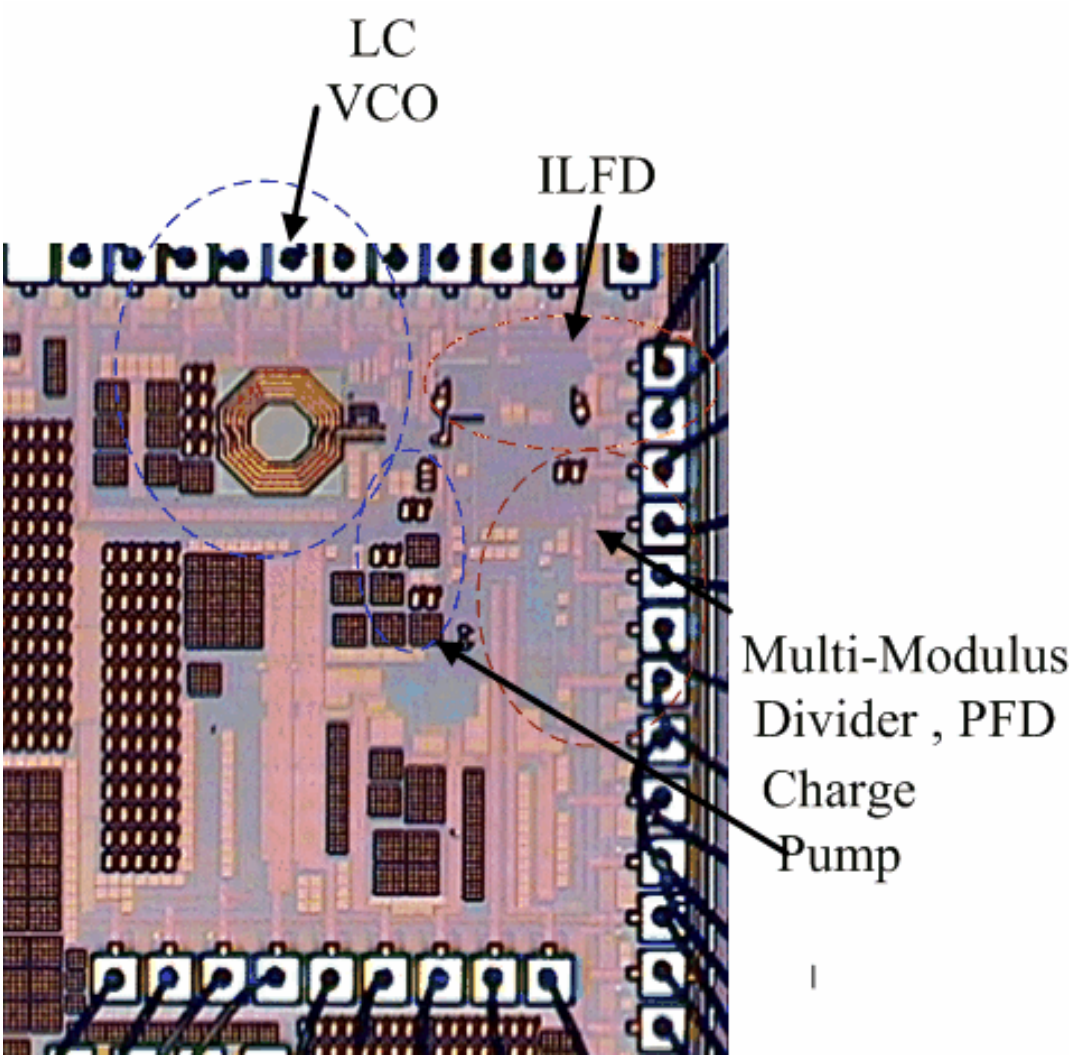


Figure 5.1. Chip microphotograph

Figure 5.2 shows the implementation details of the prototype frequency synthesizer. The dotted lines indicate the chip boundary and denote the components of the synthesizer that are on-chip. As shown in the figure, all the blocks of the PLL except the loop filter are implemented on-chip. The loop-filter was implemented off-chip due to the area limitations on the chip. Its should be noted that using the dual-path loop filter and capacitor multiplication techniques [15,16] could lead to a significant area reduction. However, these techniques were not implemented in the prototype design. Most of the bias currents were provided off-chip using P-JFET and N-JFET based current sources. The power supply to the JFETs (VDD_High and VSS_low) was +3 V and -3 V respectively to ensure enough voltage headroom for the JFET current sources. The output of the VCO was buffered using the setup shown in Fig. 5.2. The transistors P1_B and P2_B and the 50 Ω loads were implemented on the chip and the PCB respectively. Similarly, the PMOS transistor (P3_B) buffering the output of the ILFD and the bias-tee structure are implemented on chip and PCB respectively. The reference signal was provided using a 50 MHz crystal oscillator.

The power supply scheme is shown in Figure 5.3 and is similar to the one implemented in [17]. The supply and ground pins to all the sensitive analog blocks that include the charge-pump, the VCO, and ILFD prescaler are provided separately. The digital blocks that include the PFD, calibration circuitry, and all other digital circuitry were run on a separate power and ground bus. This was done to isolate the power supply noise on the power and ground buses to avoid disturbances to the high-performance analog blocks. The power supplies to the analog blocks were separately filtered using three-terminal

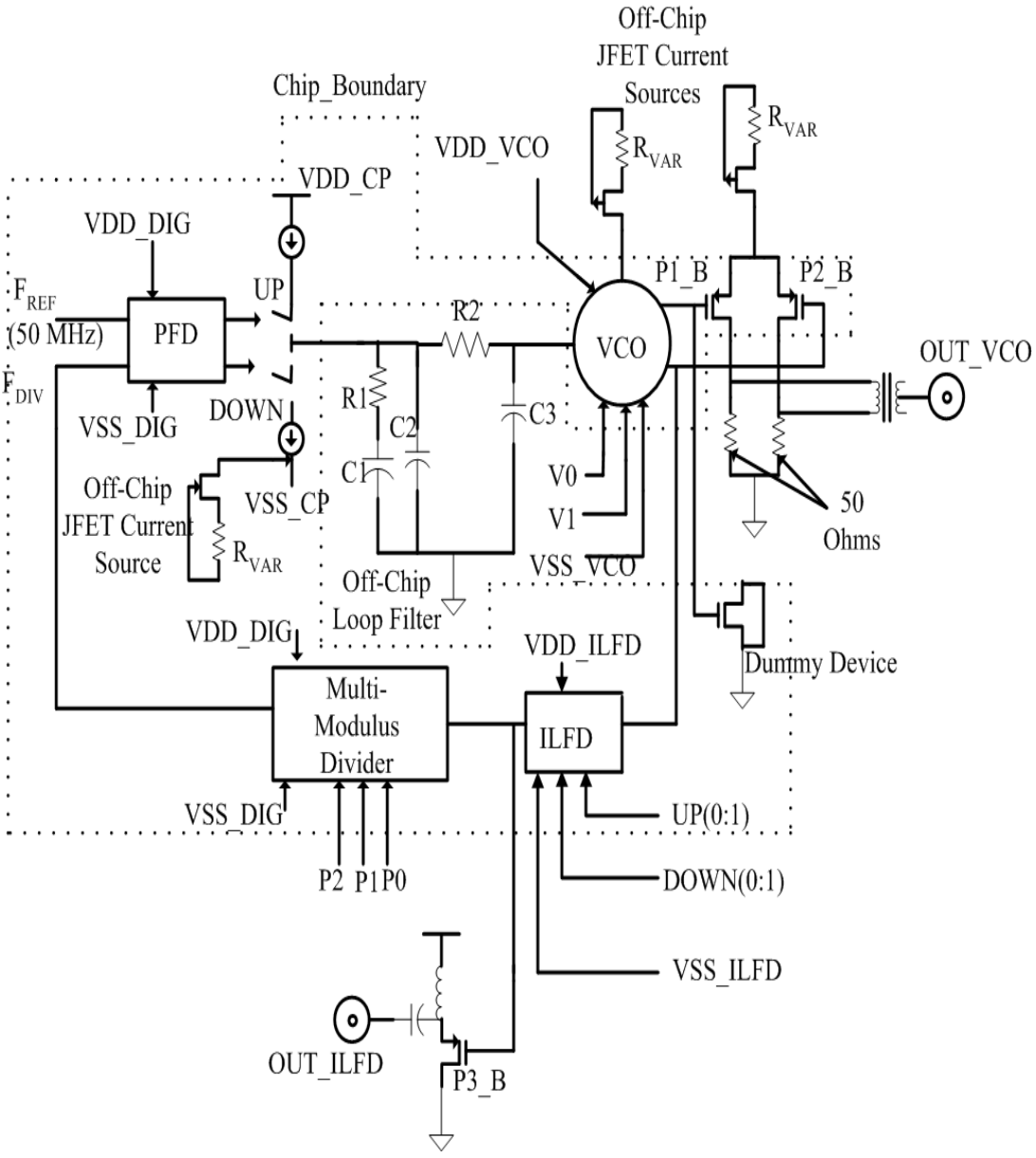


Figure 5.2. Implementation details of the 2.4-GHz frequency synthesizer

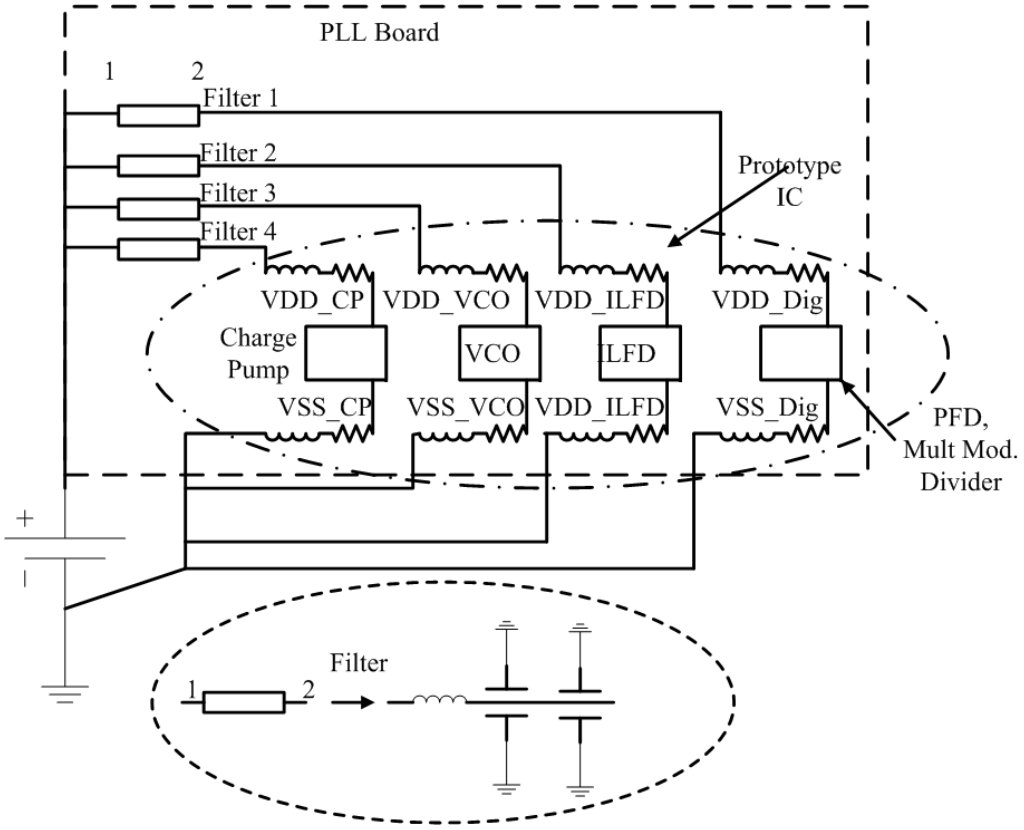


Figure 5.3. Power supply scheme

capacitors[17] and tied to the common power supply on the PCB.

A 4-Layer FR-4 PCB was fabricated to house the test structures and the chip. Figure 5.4 show the photograph of the impedance-controlled PCB. 50-Ω transmission lines were fabricated on the top layer to match the impedance all the way from the output of the VCO to the SMA connector on the board that connects to the spectrum analyzer. The dimensions of the transmission lines were calculated using the board parameters provided by the vendor. The "Linecalc" program available in Agilent's Advanced Design System (ADS) package was used for this purpose. The transmission lines were grounded co-planar waveguides type fabricated using the top and the 2nd layer on the PCB. The top layer also houses all the power buses. The power buses were made thick to avoid resistive

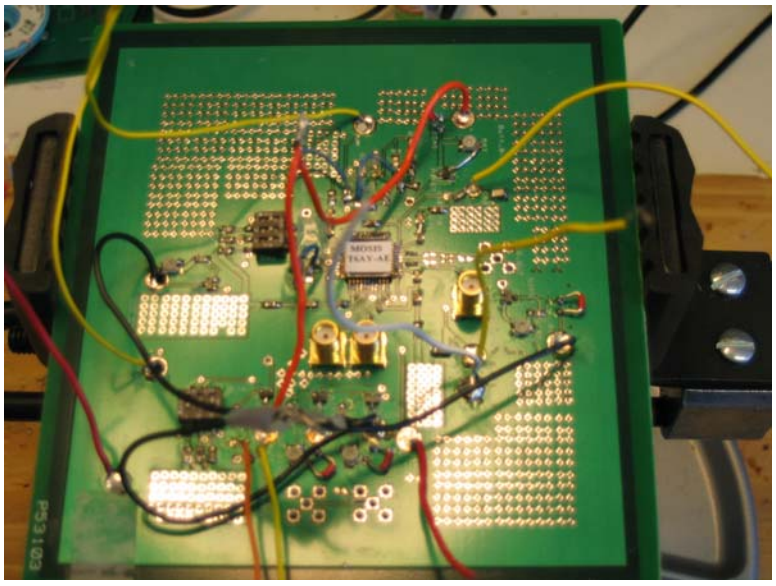


Figure 5.4. 4-Layer printed circuit board for circuit characterization

drops. The entire second layer on the PCB acts as a ground plane. The third layer on the PCB was made the power plane; the last layer housed the traces for bias lines. A plethora of vias were used to connect the power and ground planes on the top and bottom layers to the power and ground plane respectively. This was done to reduce the inductance contributed by the vias and avoid bounces on the supply and ground lines.

5.2 Process and Temperature Compensated ILFD Characterization

Wafer-probing technique was used for measuring the ILFD. As mentioned previously, this technique allows fast characterization of multiple chips. The test structure for measurement using this technique is shown in Figure 5.5. It consists of two sets of G-S-G pads, one connecting to the input and another to the output of the ILFD. G-S-G (which means Ground-Signal-Ground) structures are always used for high frequency measurements and characterization. The special probe used for this purpose is called a G-S-G probe. The ground pads on each sides of the signal provide a low-impedance path to ground and hence minimize signal coupling to adjacent lines. Power supply and bias currents were provided using DC probes. First, the ring oscillator was characterized to determine how its natural frequency of oscillation varied with process and temperature and hence the effectiveness of the compensation scheme. The output of the ring oscillator (ILFD) was buffered using a PMOS transistor. The bias to the transistor was provided using a bias-tee. The “RF+DC”, “DC” and “RF” terminal of the bias-tee were connected to the “Signal” pad of the G-S-G structure, 1.8V and the spectrum analyzer respectively. The oscillation frequency of the ring oscillator on 6 different chips was measured at room temperature. The chips were chosen from various corners from the set of 40 die provided.

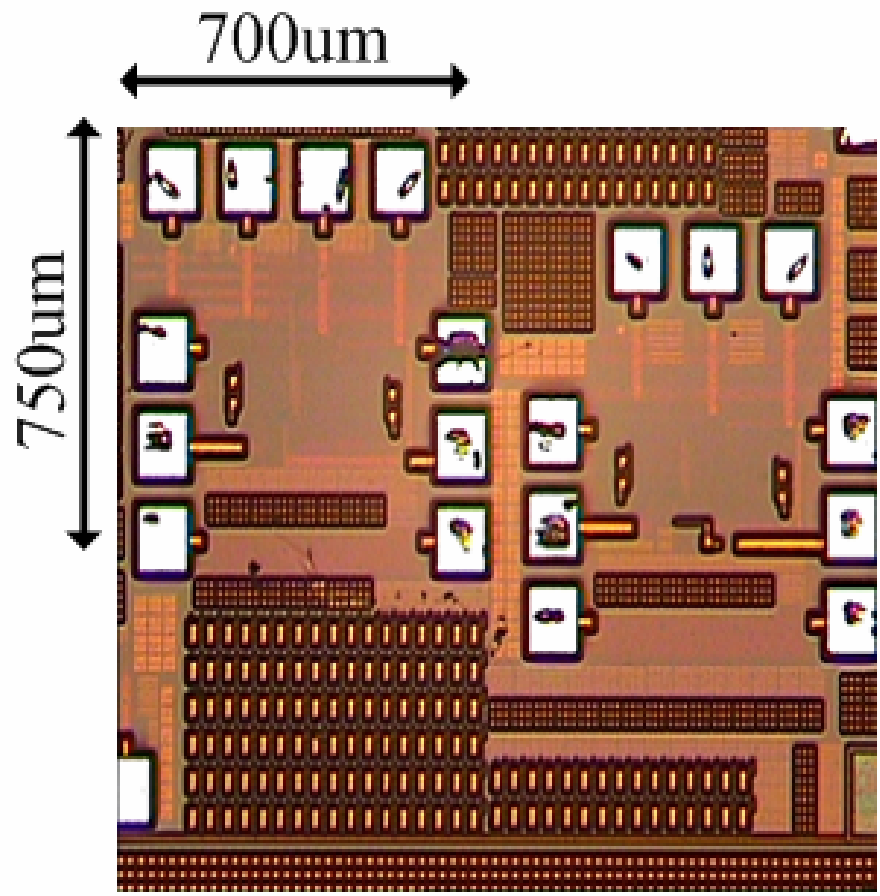


Figure 5.5. ILFD with GSG pads for on-wafer characterization

Table 5.1 shows the results of the measurement. The dimensions of each chip were 3mm x 3mm and therefore the chips selected from the corners will be subject to maximal process variations. The results show just a worst case deviation of 3.5 % variation with process from the mean value of 625 MHz. Simulation results show a frequency of oscillation of 650 MHz using the TT corner at room temperature and a variation of 3% across process corners. The measurement results were found to be in good agreement with the simulation results. The inaccuracy in the simulated frequency is attributed to modeling of the extracted parasitics. The worst-case power consumption was approx 2.2 mW from a 1.8 V power supply. The ring oscillator (chip 5) was injection-locked to act as a fixed divide-by-4 circuit by applying an input signal using a RF signal generator. The power of the signal applied was 0 dBm. The measured locking range was found to be 0.95 GHz. The locking range could be extended by slightly modifying the control voltage. It should be noted, however, that changing this voltage too much will affect the temperature compensation as discussed in Chapter 3. Therefore this voltage is changed only 50 mV above and below

Table 5.1. Measured natural frequency of oscillation of the ring oscillator on 6 different chips

Chip Number	**Frequency of Oscillation (f_O) (MHz)**
1	630
2	619
3	647
4	637
5	624
6	627

its nominal value. Using the provision to measure the control voltage on the chip, it was found to be 860 mV. This value was close to the desired range of values that were set in Chapter 3 for process and temperature compensation. By varying the control voltage 50 mV above and below the nominal value, the highest frequency for which a lock is achieved was extended to 3.4 GHz and the lowest frequency was 1.6 GHz. The control voltage was optimized by manually adjusting the control voltage and applying it through the DC probes directly on to the wafer.

The calibration circuitry was not implemented on the chip because it required many digital signals as inputs, while the number of DC test probes was limited to four. Figures 5.6, 5.7 and 5.8 show the spectrum of the output signal from the divider for an input signal of 1.8 GHz, 2.4 GHz and 2.9 GHz respectively. Figure 5.9 shows the spectrum of the ILFD when it looses lock. Simulation results show a locking range of 1.15 GHz for the latch size of 2.6μm/0.2μm that was implemented on the chip. The disagreement can again be attributed to the capacitances seen by the drain of the tail transistors that are not modeled in schematic simulations. The same ILFD circuitry has a locking range of 0.55 GHz (3.3 GHz to 3.85 GHz) while functioning as a divide-by-6 circuit. This again is in good agreement with simulation results that shows a locking range of 0.7 MHz. The discrepancy can again be attributed to the same reason as above. The combination of the LC tank VCO and the ILFD were next tested to determine if the ILFD was capable of achieving a lock (divide-by-4) over the entire range of frequencies generated by the LC VCO. The 4-layer PCB was used for this purpose.

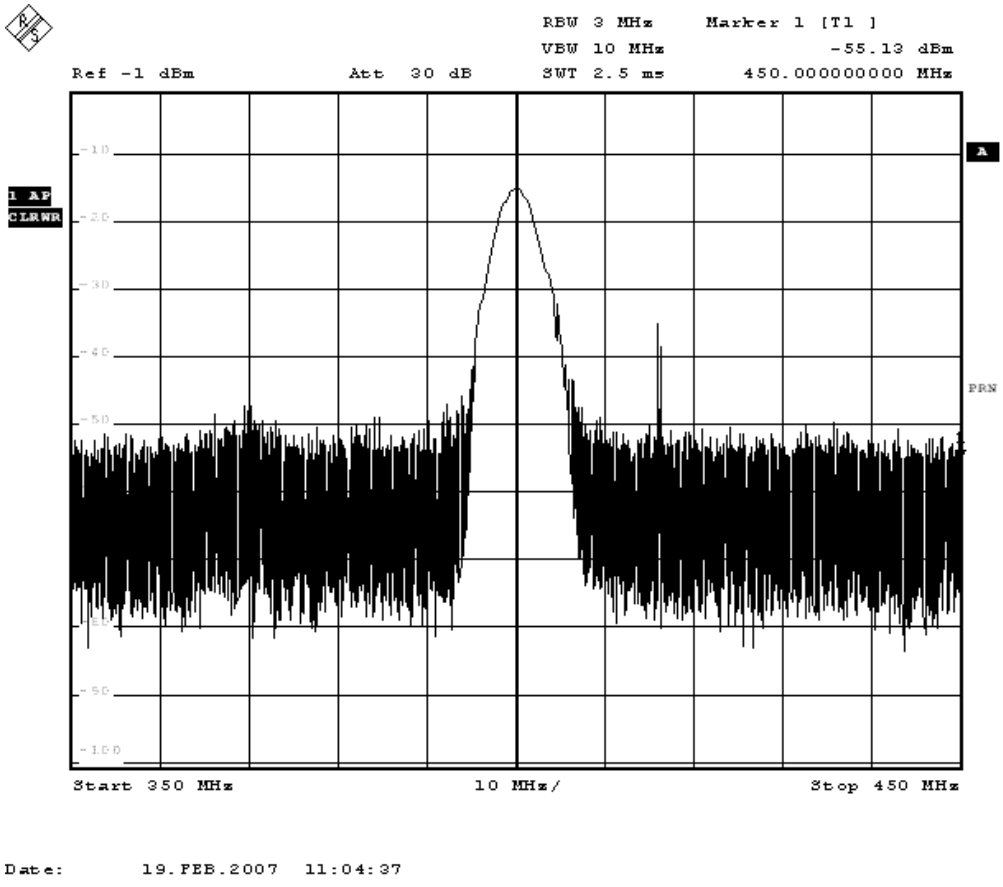


Figure 5.6. Output spectrum of the ILFD for an input signal frequency = 1.8 GHz

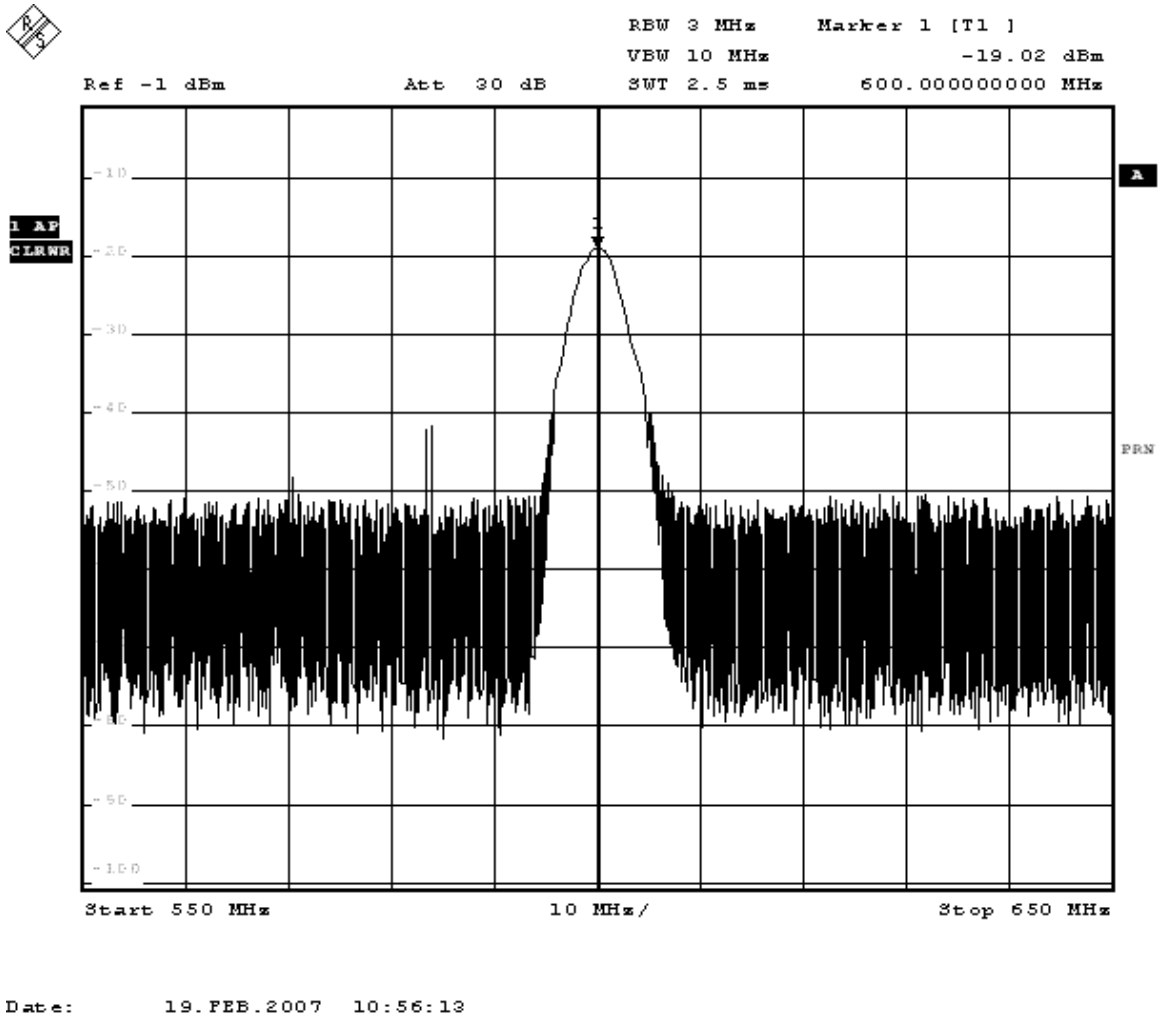


Figure 5.7. Output spectrum of the ILFD for an input signal frequency = 2.4 GHz

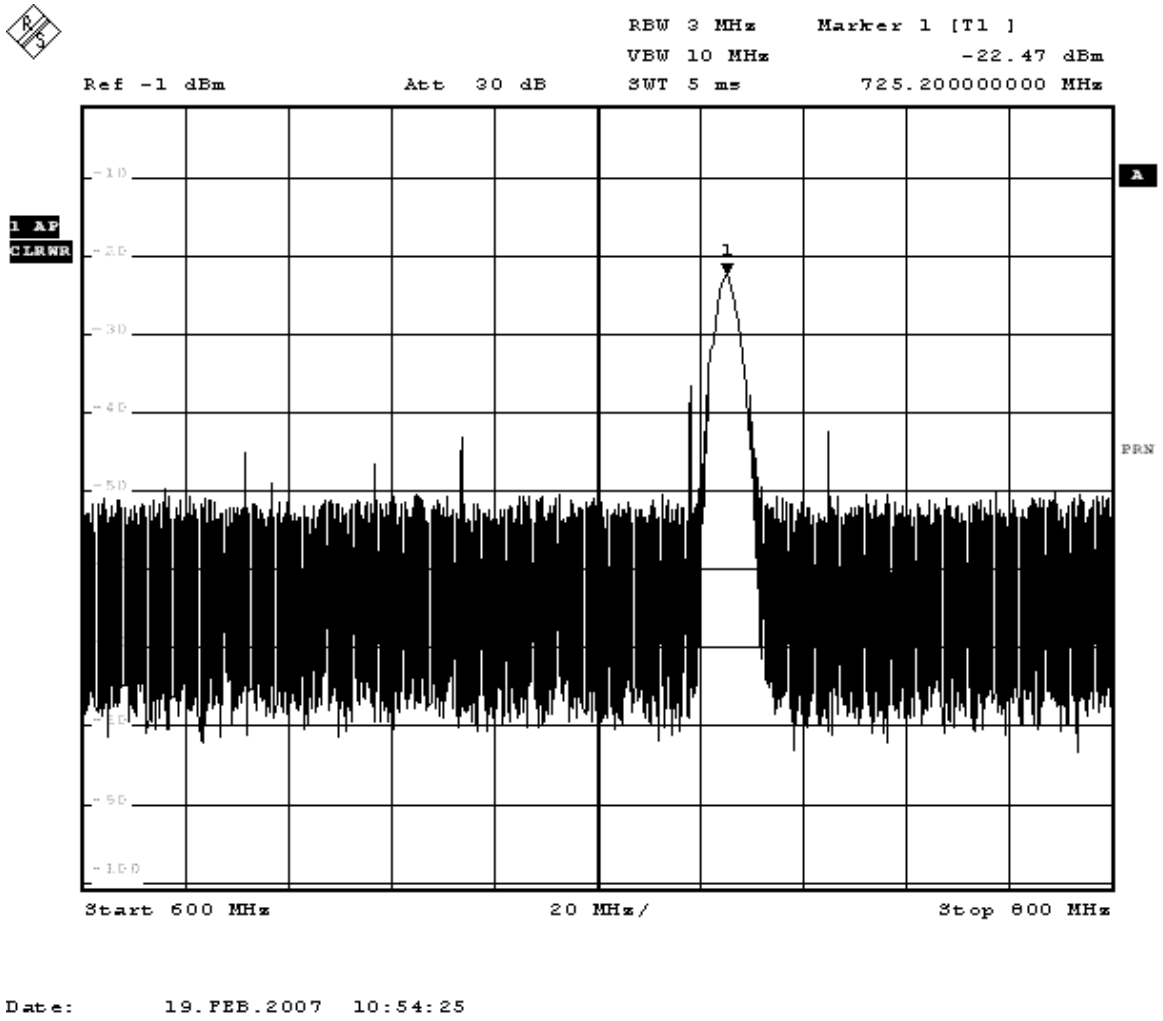


Figure 5.8. Output spectrum of the ILFD for an input signal frequency = 2.9 GHz

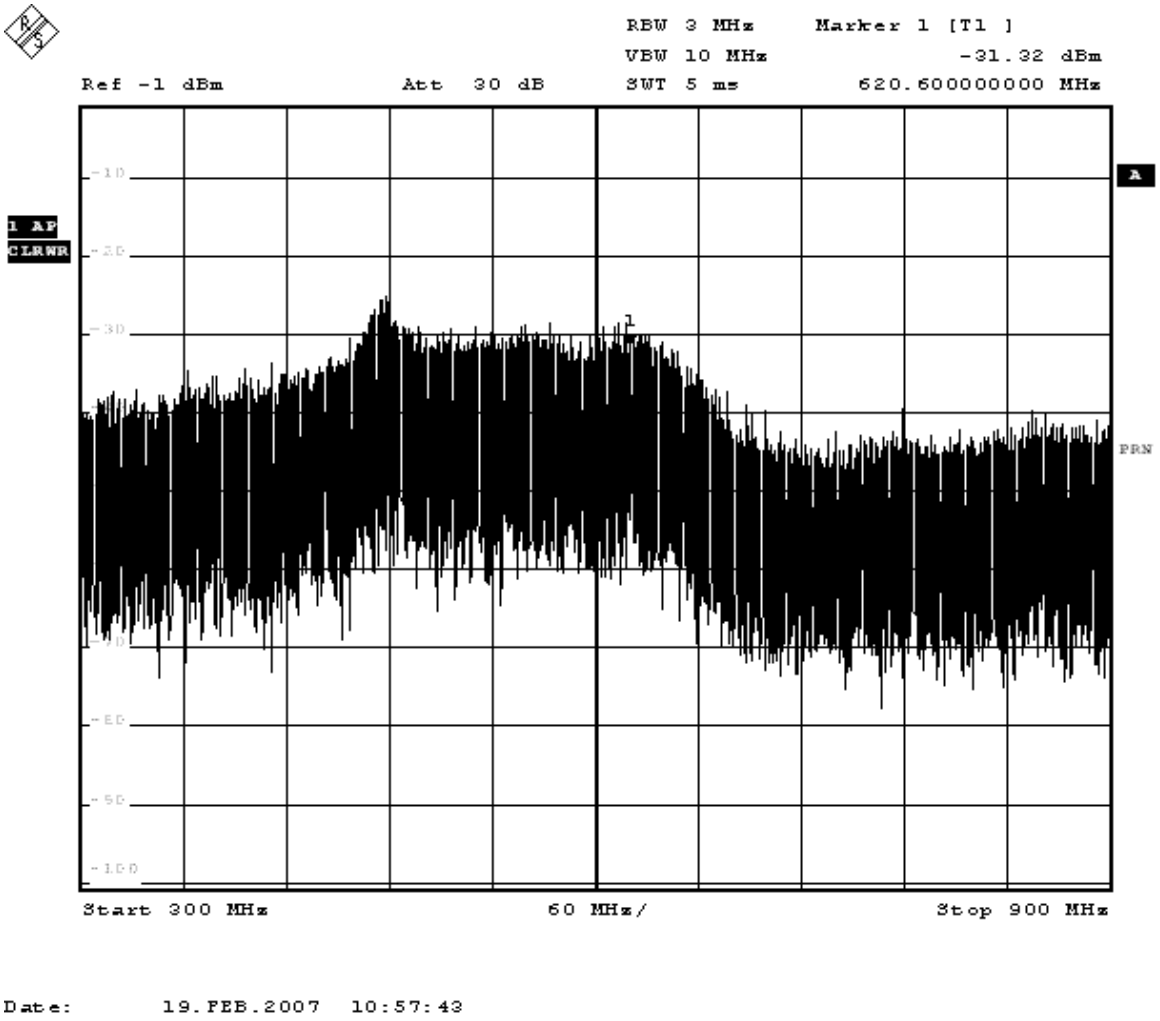


Figure 5.9. Output spectrum of the ILFD when out of locking range

Figure 5.10 shows the measured tuning curve of the ILFD. The tuning curve was determined for each capacitor control bit as shown in Figure 5.10. The measurement results were found to be in good agreement with the simulation results given in chapter 4. The measured VCO gain (K_{VCO}) was found to be 200 MHz/V. The ILFD was tested to determine if it could achieve lock over the extreme frequencies generated by the VCO. The minimum and maximum frequencies generated by the VCO were 2.057 GHz and 2.652 GHz for a control word of "11" (0V) and "00"(1.8V) respectively. The figure inside the brackets gives the value of the analog control voltage. Figures 5.11 and 5.12 shows the spectrum of the maximum and minimum frequencies generated by the LC tank oscillator. Figures 5.13 and 5.14 shows the spectrum of the ILFD output. As seen from the Figures 5.13 and 5.14, the ILFD is capable of locking to the entire range of frequencies generated by the LC VCO.

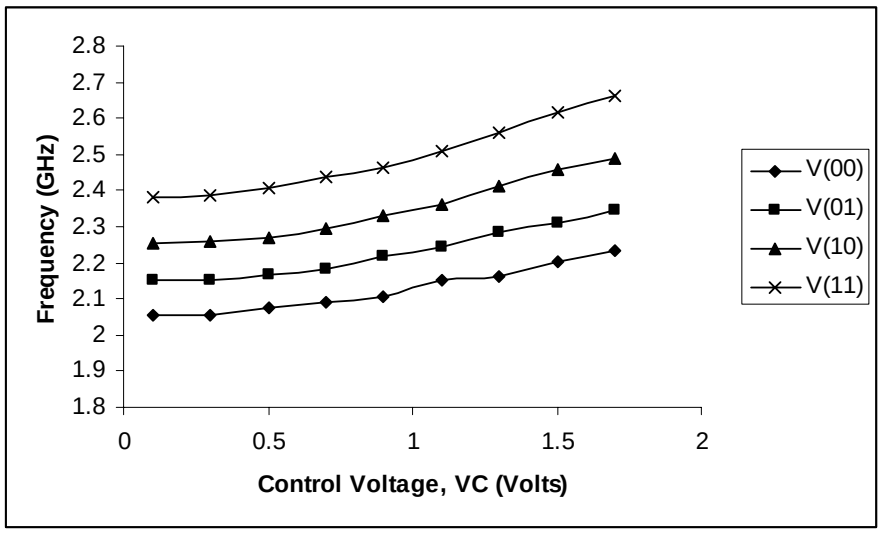


Figure 5.10. Measured tuning range of the LC VCO

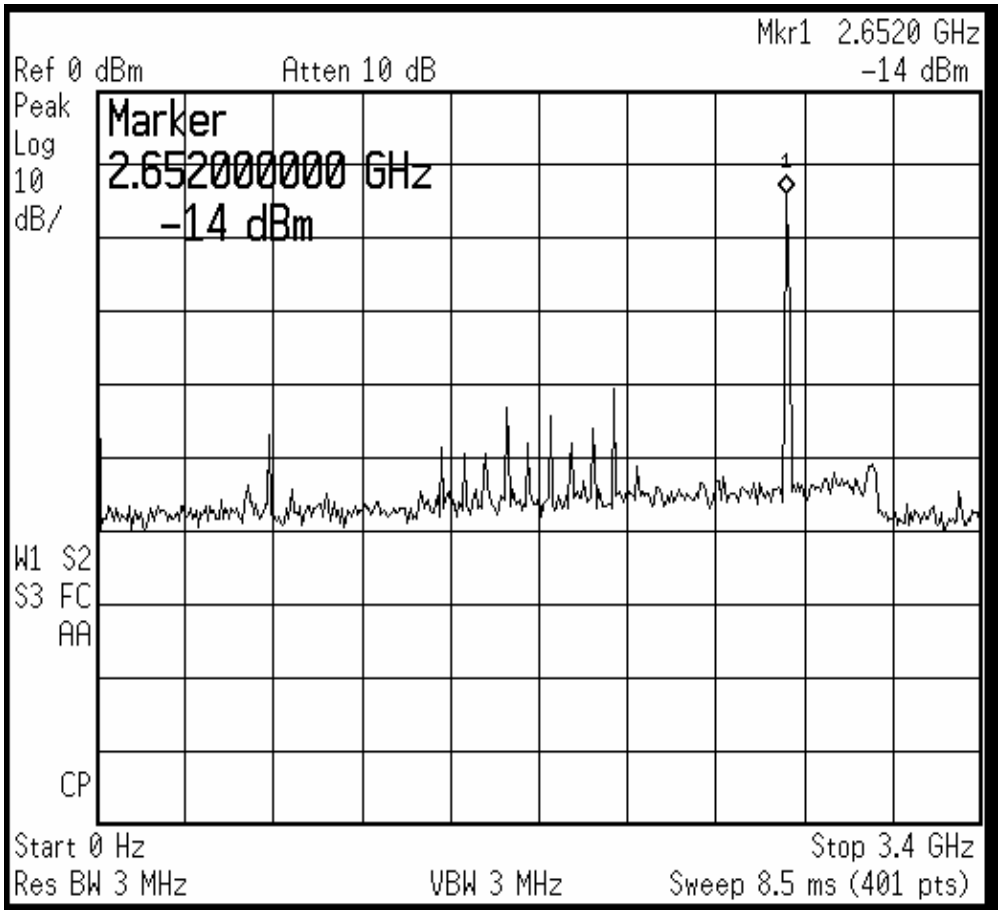


Figure 5.11. Maximum frequency generated by the LC VCO

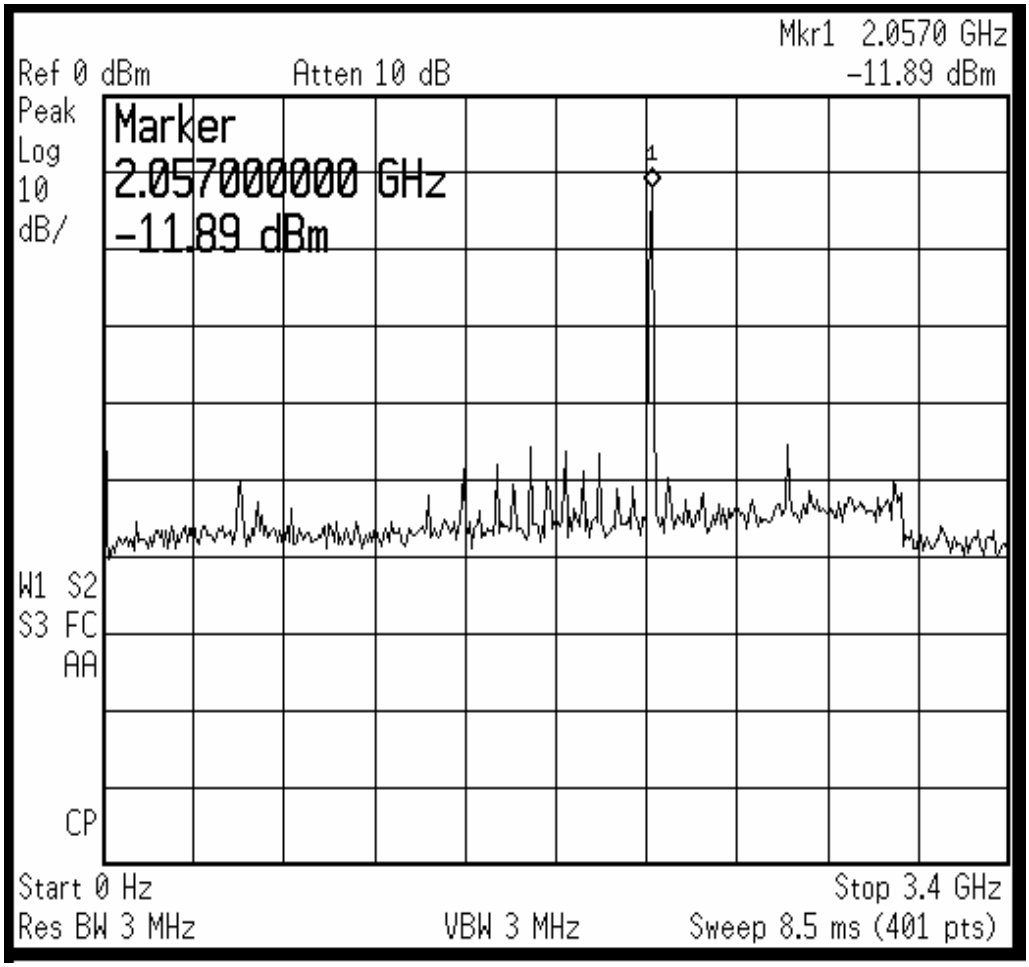


Figure 5.12. Minimum frequency generated by the LC VCO

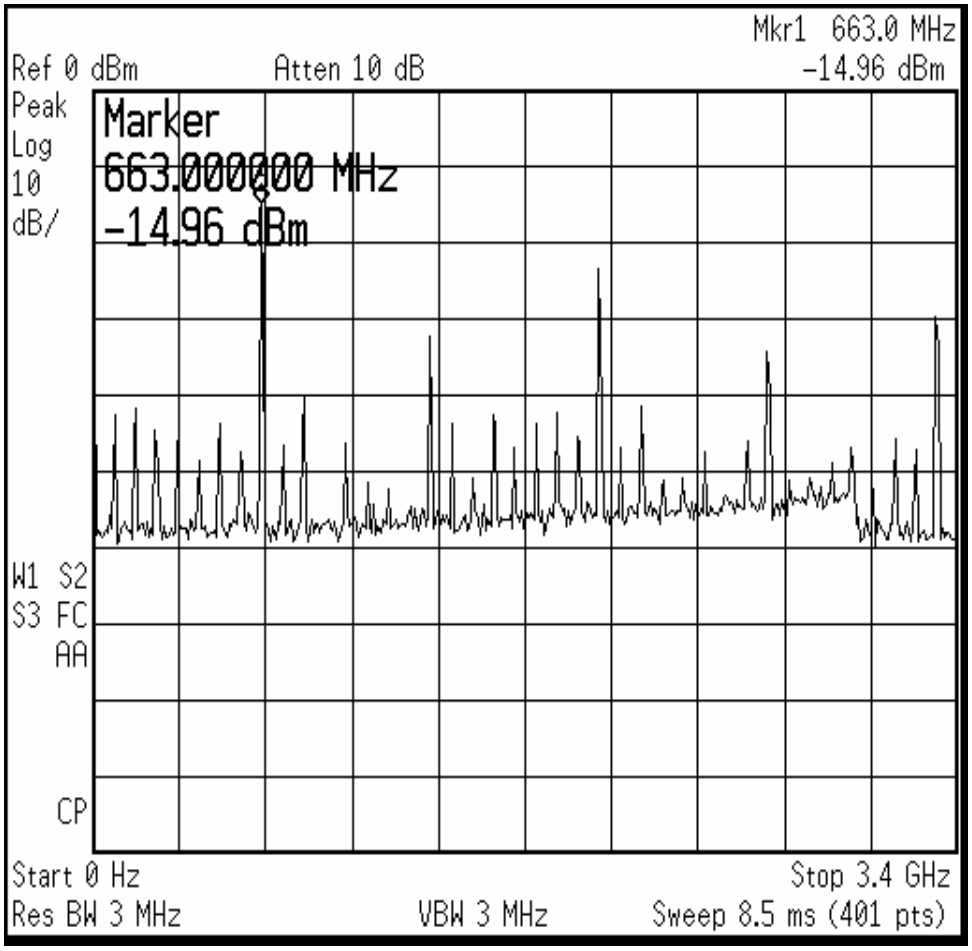


Figure 5.13. Locked spectrum at the output of the of the ILFD for an input of 2.652 GHz

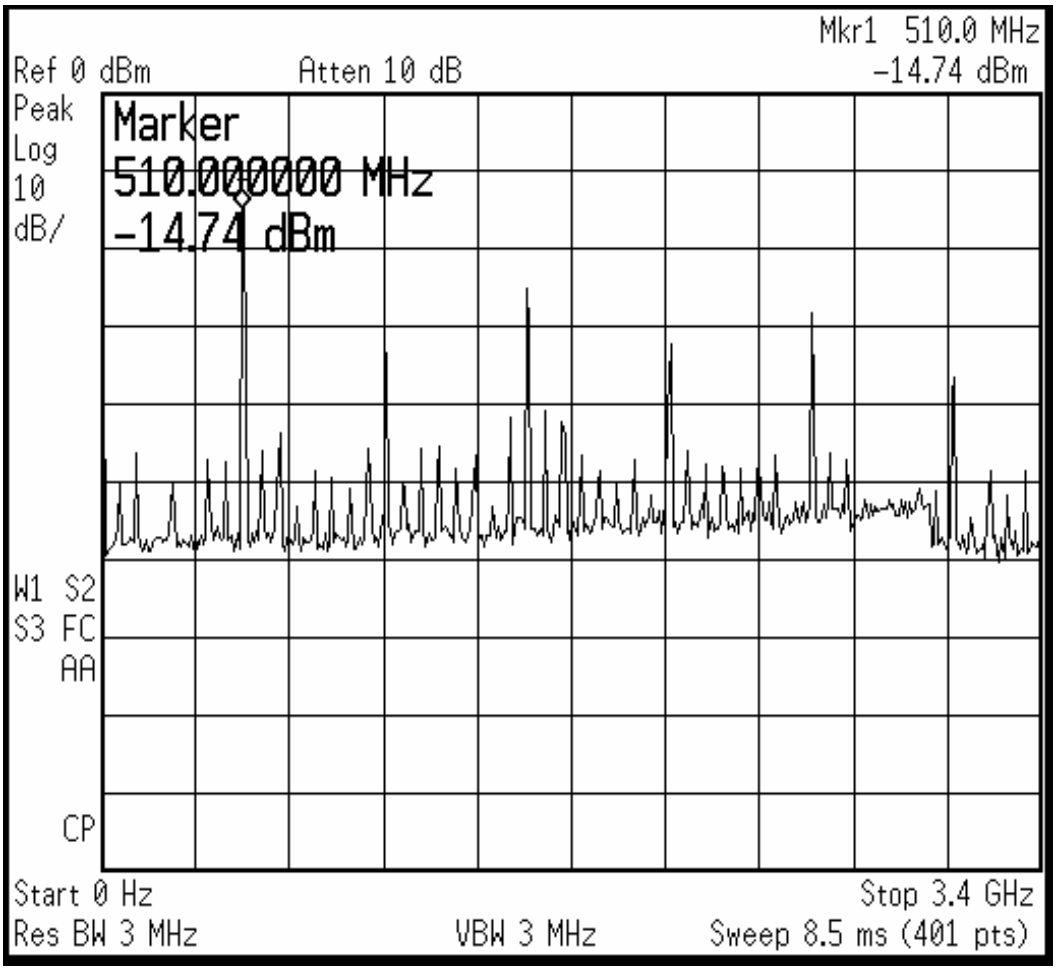


Figure 5.14. Locked spectrum at the output of the of the ILFD for an input of 2.057 GHz

The output frequency of the divide-by-4 ILFD when dividing an input frequency of 2.057 GHz is shown as 510 MHz instead of 514 MHz. This is due to inaccuracy of the markers on the spectrum analyzer when a large range of frequencies are being measured. When the frequency is zoomed in, it shows the correct value of 514 MHz.

Figures 5.15 and 5.16 show the phase noise of the LC oscillator when oscillating at a frequency of 2.428 GHz. The control word in this case was V (00). Since 2.428 GHz is in the middle of the tuning curve, the phase noise is expected to be the worst. The phase noises at offset frequencies of 600 KHz and 1 MHz were found to be -109 dBC/Hz and -114.62 dBc/Hz, respectively. This also includes the phase noise added due to the buffers. The natural frequency of oscillation (free running frequency) of the ring oscillator in the ILFD was found to be 637 MHz. Figures 5.17 and 5.18 show the phase noise of the free-running ring VCO. The phase noises at offset frequencies of 600 KHz and 1 MHz were found to be -67 dBC/Hz and -74 dBc/Hz respectively. The phase noise of the locked oscillator (divide-by-4 ILFD) is shown in Figure 5.19 and 5.20. The output of the divider in this case was 607 MHz and the phase noise at offset frequencies of 600 KHz and 1 MHz was found to be -119 dBC/Hz and -123 dBc/Hz respectively. As predicted by the theory, the phase noise at the output of the ILFD is filtered out to the loop-bandwidth. For a wideband ILFD the loop-bandwidth is high, and therefore the phase noise filtering is better. The phase noise was measured using the E4407B series spectrum analyzer, with phase noise measurement capabilities manufactured by Agilent Technologies.

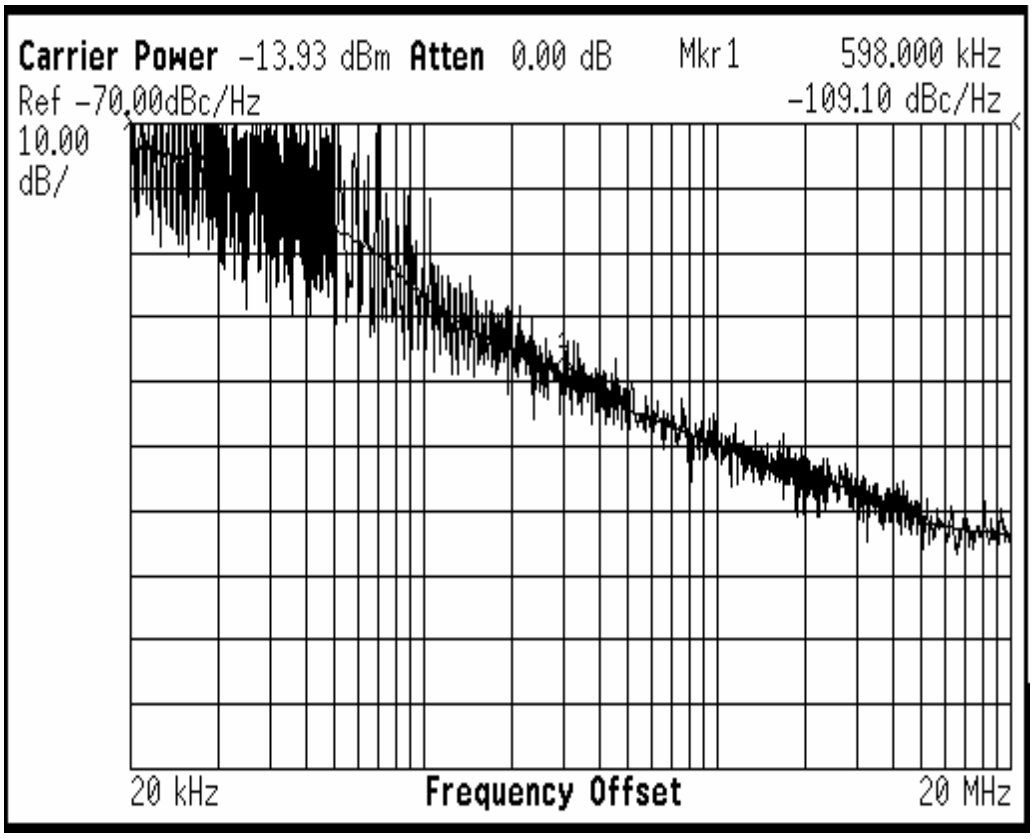


Figure 5.15. Phase noise of the LC VCO at an offset frequency of 600 KHz

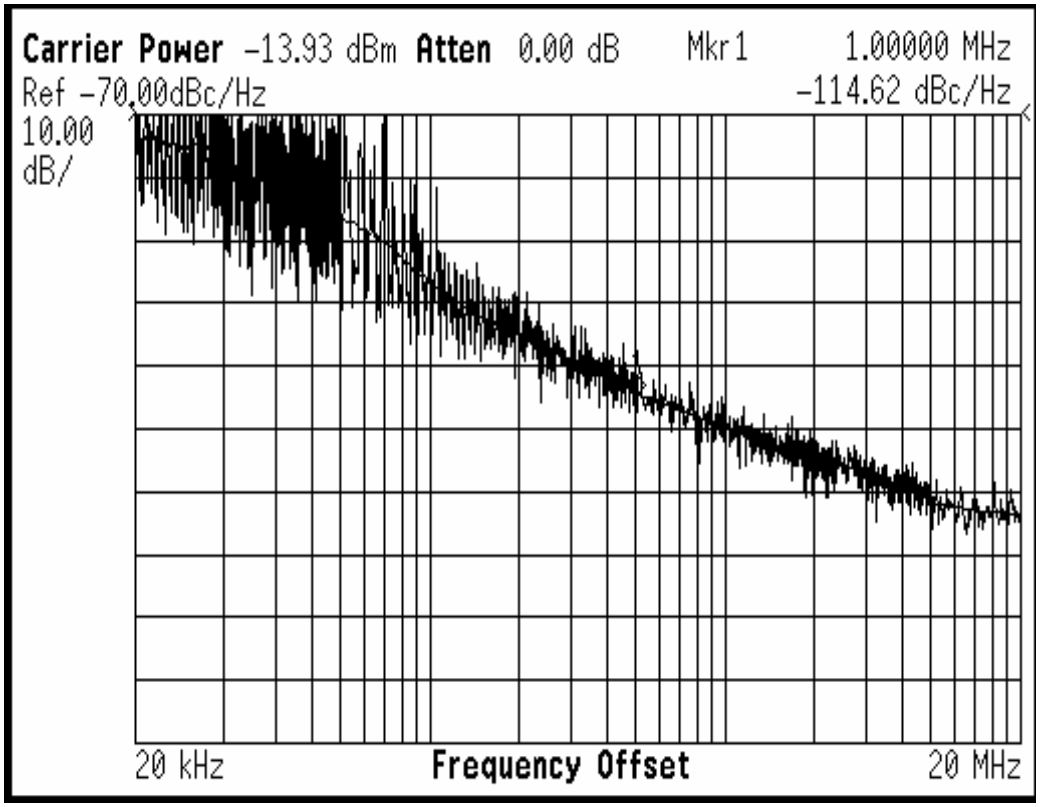


Figure 5.16. Phase noise of the LC VCO at an offset frequency of 1 MHz

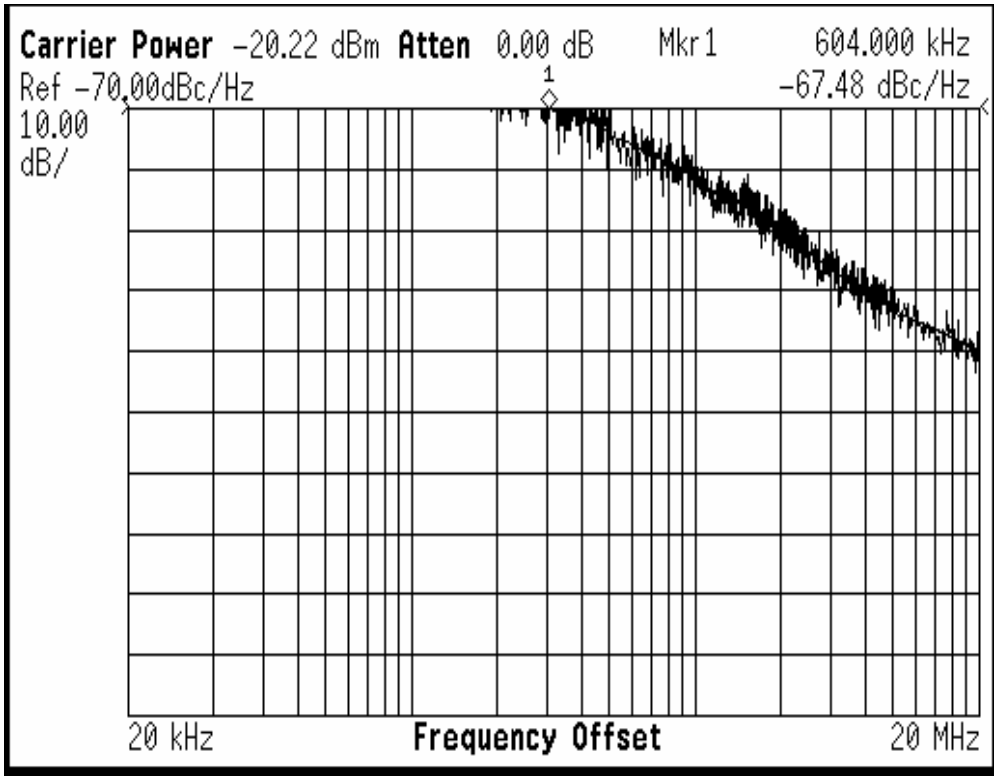


Figure 5.17. Phase noise of the free running oscillator at an offset frequency of 600 KHz

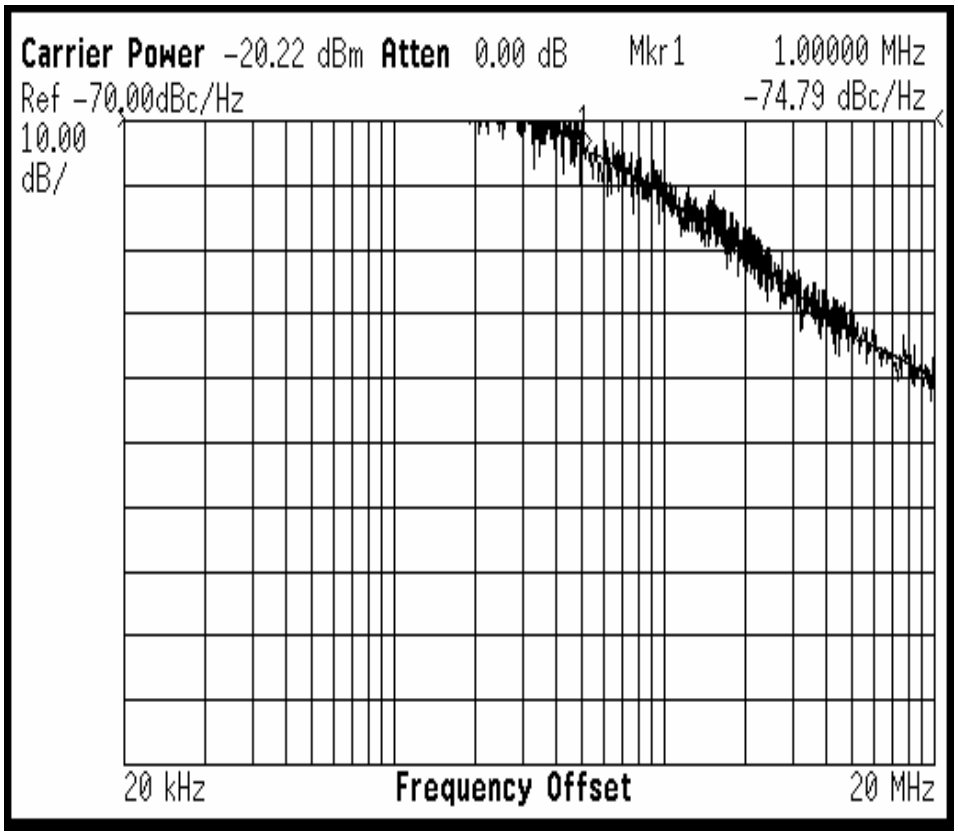


Figure 5.18. Phase noise of the free running oscillator at an offset frequency of 1MHz

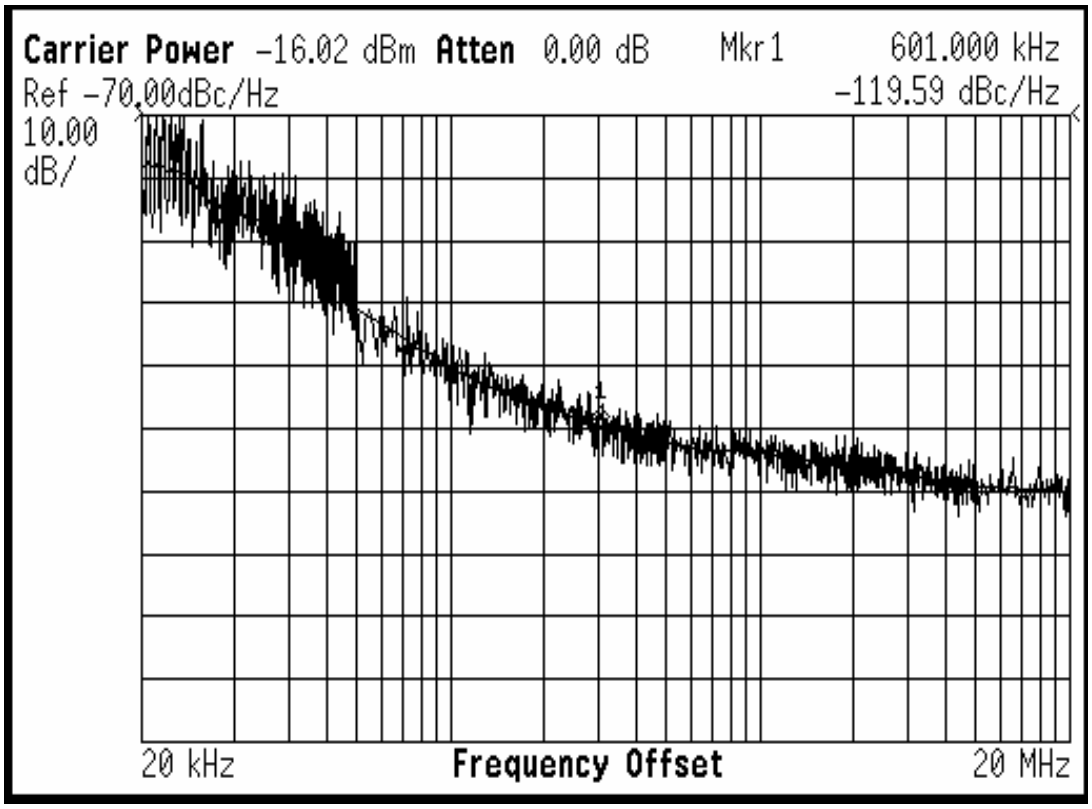


Figure 5.19. Phase noise of the injection locked oscillator at an offset frequency of 600 KHz

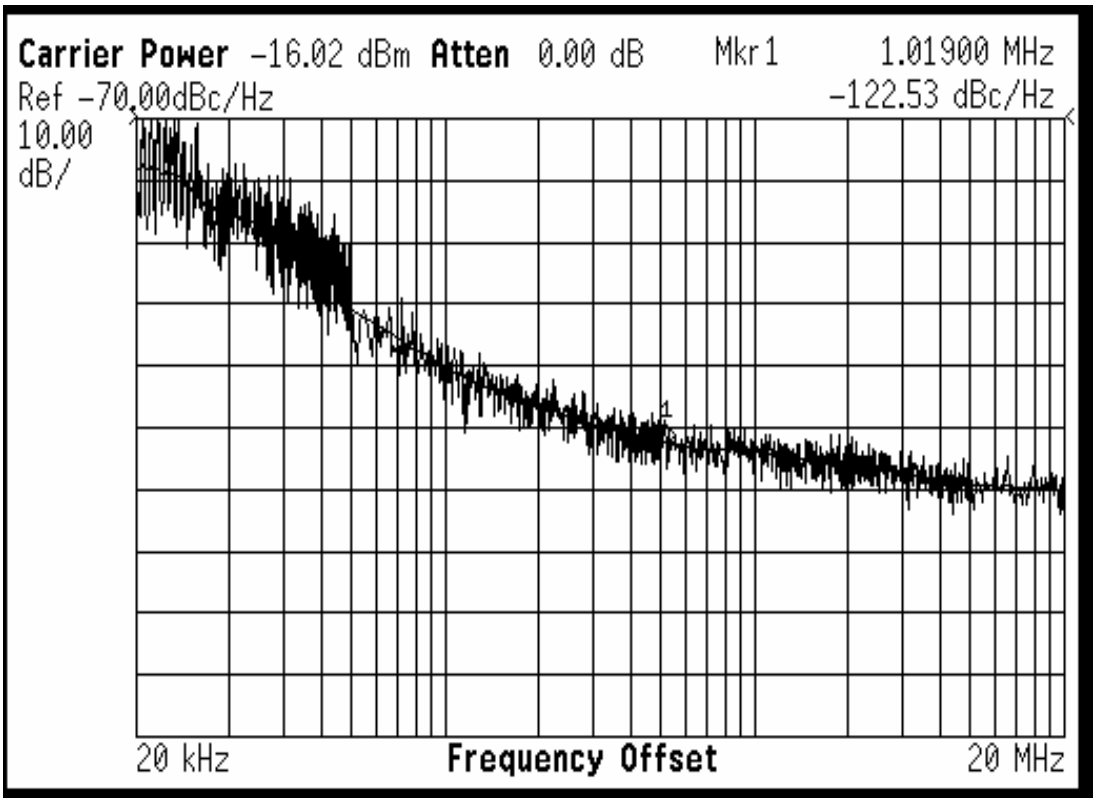


Figure 5.20. Phase noise of the injection locked oscillator at an offset frequency of 1 MHz

Due to the non-availability of the on-wafer temperature characterization facility, the temperature characterization of the ILFD was accomplished by using the FR-4 board in an oven. The oscillation frequency was measured directly using a spectrum analyzer. The temperature of the oven was set to 80 °C and the FR4 board was placed inside the oven. The board was kept in the oven for 15 minutes before the oscillation frequency was measured. The temperature was lowered in steps of 20°C and the oscillation frequency for each case was recorded. A time interval of 15-20 minutes was set between each measurement. Figure 5.21 shows the result of the temperature characterization. The oscillation frequency varied from a room temperature value of 632 MHz by only 4.2% at 80 °C. Since the board contains JFET current sources, a part of the variation in frequency is also due to the variation of the JFET bias currents with temperature.

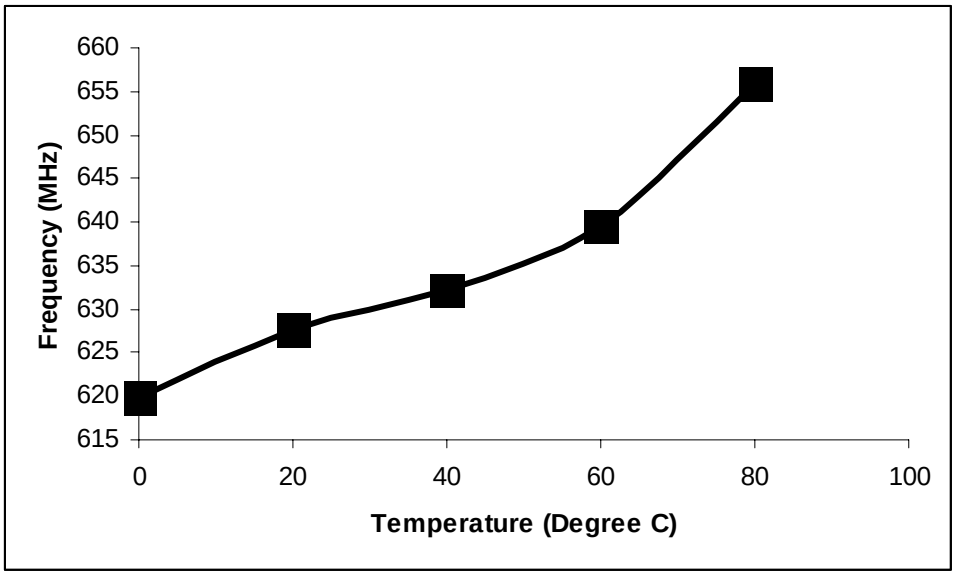


Figure 5.21. Variation of the oscillation frequency of the ring oscillator with temperature

For the above test the bias currents to the LC VCO was disconnected. The ring VCO now oscillates at its resonant frequency due to the absence of input signal. To measure the locking range with temperature, the bias to the LC VCO was connected and the tuning range was measured for a control word of "00" and "11". These control words determine the settings for the extreme frequency variation of the LC VCO. For both the settings the tuning range was measured at 0°C and 80°C. It was found that the ring VCO locks to the entire range of frequencies generated by the LC VCO. Thus the locking range of the ILFD is well controlled with temperature variation. The ILFD has a tuning range of at least 700 MHz over a temperature variation of 0°C to 80°C.

5.3 Prototype Frequency Synthesizer Testing

The prototype frequency synthesizer was characterized using the 4-layer PCB. A 50-MHz crystal oscillator manufactured by ECS, Inc. was used as the reference source. Only an integer-N synthesizer was implemented in this work using the process and temperature compensated ILFD. Although, the original intention was to implement a fractional–N synthesizer. As shown in Chapter 4 the loop parameters were optimized to achieve fractional-N operation, thus making the current architecture suitable for fractional-N operation. A digital sigma-delta modulator can be designed on an FPGA [17] and interfaced with the multi-modulus divider to implement a fractional-N synthesizer.

To synchronize the arrival of the control bits to the divider when the sigma-delta modulator is implemented on the board using FPGAs, the circuit used in Figure 5.22 is

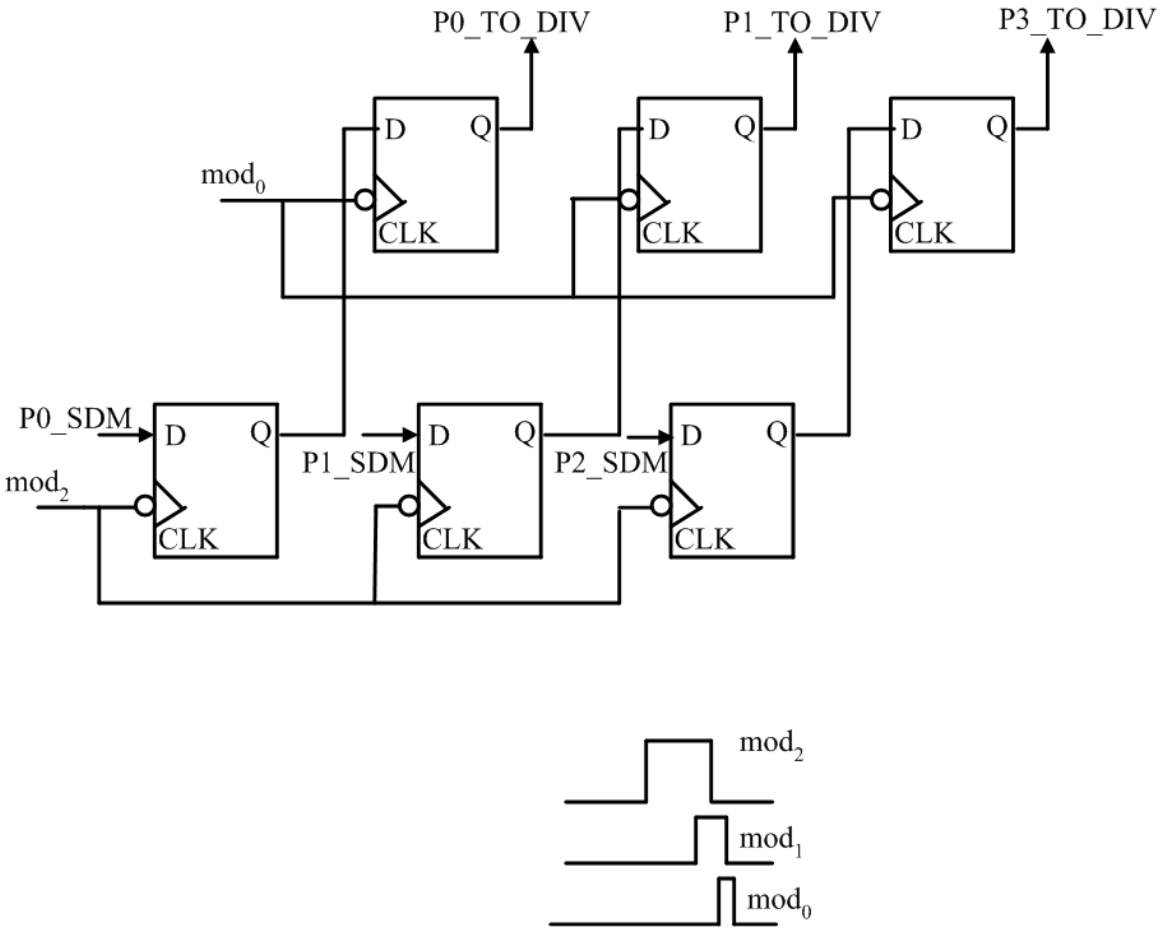


Figure 5.22. Interface circuitry between sigma-delta modulator and the multi-modulus divider

used to interface the sigma-delta modulator to the multi-modulus divider. The different delays of the bits from the output of the sigma-delta modulator into the multi-modulus divider can cause the noise of the synthesizer to increase significantly. This was observed in the work by [17]; the interface circuit was used to prevent this. This circuit was also used by the author of reference [17], but was not mentioned in that paper.

The synchronization circuitry uses two levels of flip-flops. Either the mod_2 signal or the reference signal can be used as a clock to the sigma-delta modulator on the FPGA. The first-level of negative-edge triggered flip-flops are clocked by the mod_2 signal. This is the signal with the largest duty cycle. The inputs to the first level of flip-flops are the divider control bits from the sigma-delta modulator. The control bits get propagated to the second level of flip-flops when the mod_2 signal falls to zero. The second levels of flip-flops are clocked by the mod_0 signal. This is the signal with the smallest duty cycle and it goes low a certain time delay after mod_2. This ensures that all the control signals to the multi-modulus reach the divider at the same time. Since the loop parameters were optimized for fractional-N operation, all frequencies that correspond to the 2.4 GHz Bluetooth applications could not be synthesized. To demonstrate the feasibility of using the proposed ILFD for a frequency synthesizer, the specific frequencies of 2.2 GHz, 2.4 - GHz and 2.6 GHz were synthesized. This corresponds to a divider setting of 11, 12 and 13 respectively with a fixed divide-by-4 in by the ILFD. Figures 5.23- 5.26 show the spectrum of the output of the frequency synthesizer while generating 2.4-GHz, 2.2 GHz and 2.6 GHz respectively. The reference spurs in each case are found to be well below

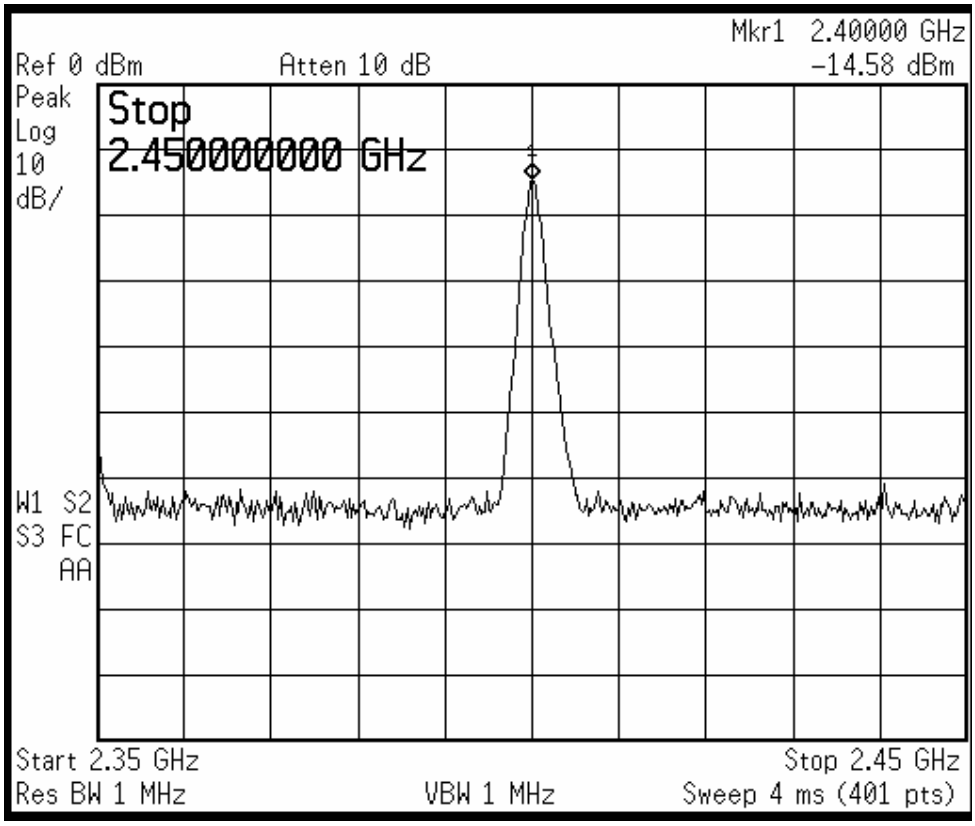


Figure 5.23. Output spectrum of the PLL base frequency synthesizer while synthesizing 2.4 GHz

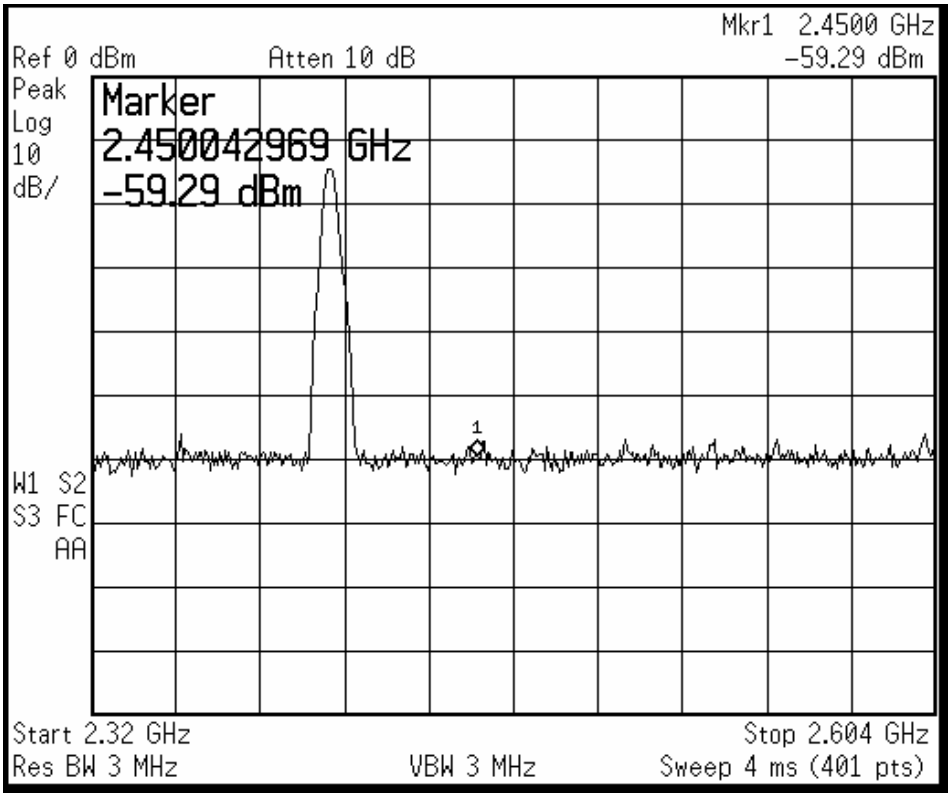


Figure 5.24. Output spectrum of the PLL base frequency synthesizer while synthesizing 2.4 GHz showing reference spurs

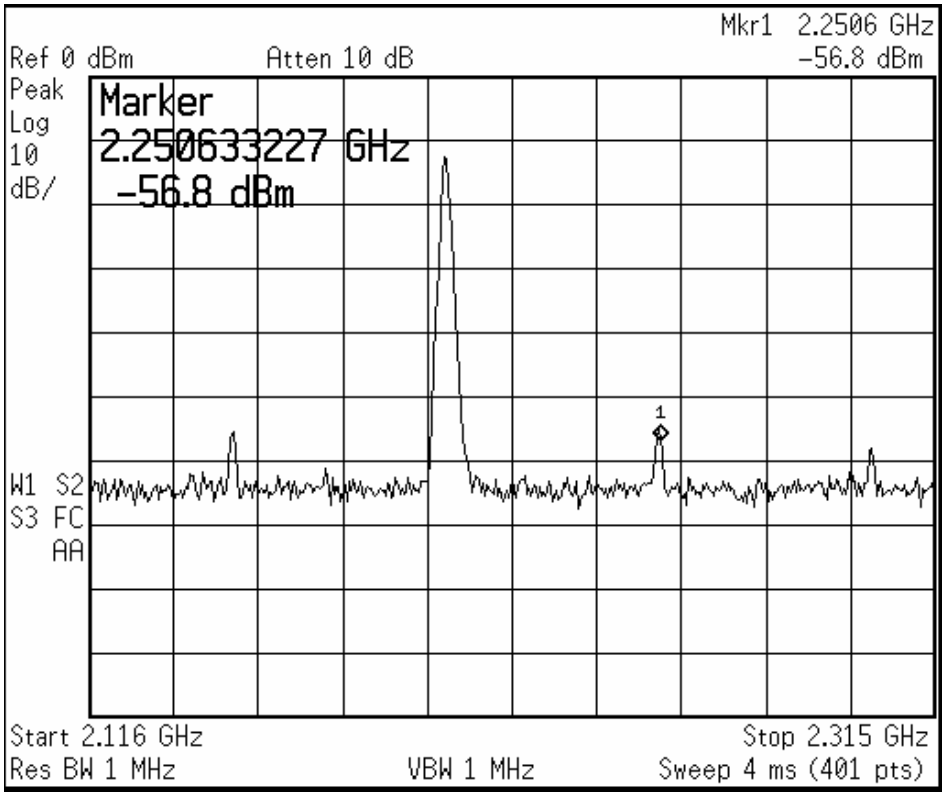


Figure 5.25. Output spectrum of the PLL base frequency synthesizer while synthesizing 2.2 GHz showing reference spurs

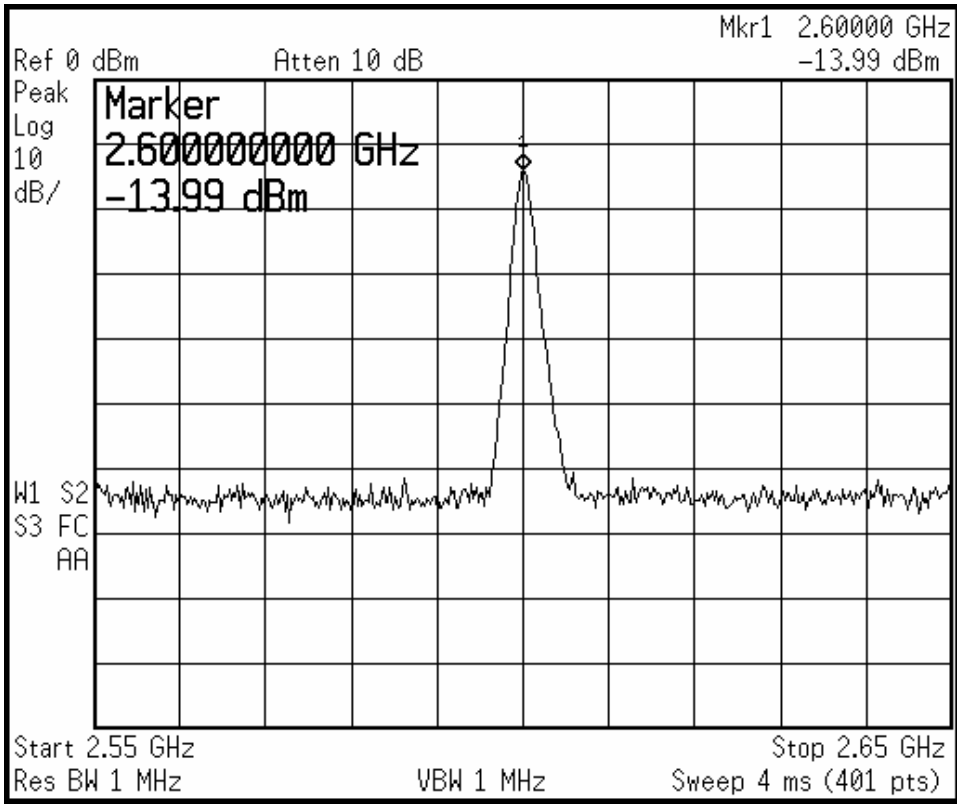
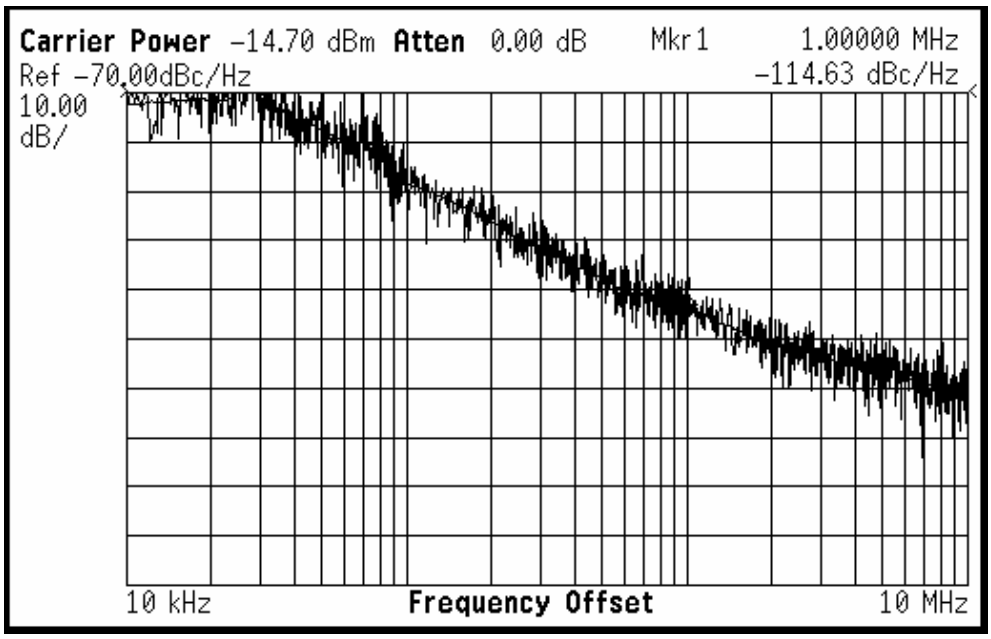


Figure 5.26. Output spectrum of the PLL base frequency synthesizer while synthesizing 2.6 GHz

the carrier. While generating 2.4 GHz and 2.6 GHz, the control bits to the VCO were set to “00”, and while generating the control voltage was changed to “11”. Figures 5.27-5.29 show the measured phase noise of the frequency synthesizer while generating 2.4 GHz, 2.2 GHz and 2.6 GHz, respectively. The measured phase noise at 2 MHz offset was found to be approx -121 dBc/Hz, satisfying the phase noise requirement for Bluetooth application. The bias current to the VCO was adjusted until oscillations ceased. The minimum value of the bias current for which the oscillator started up was found to be about 1 mA; this was the value of current used while measuring the phase noise.



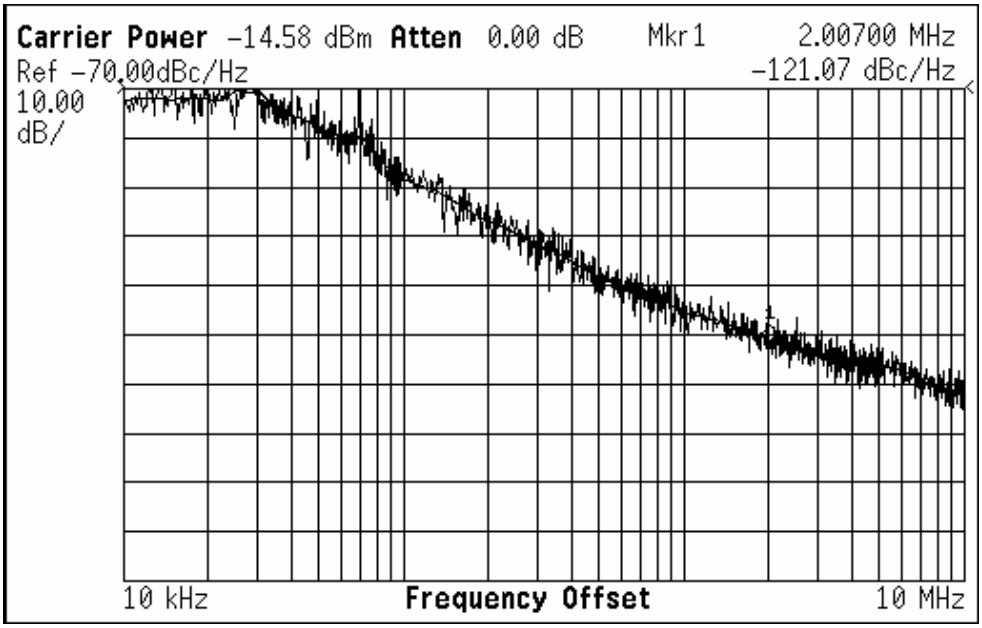


Figure 5.27. Measured phase noise while synthesizing 2.4 GHz at offset frequencies of 1 MHz and 2 MHz.

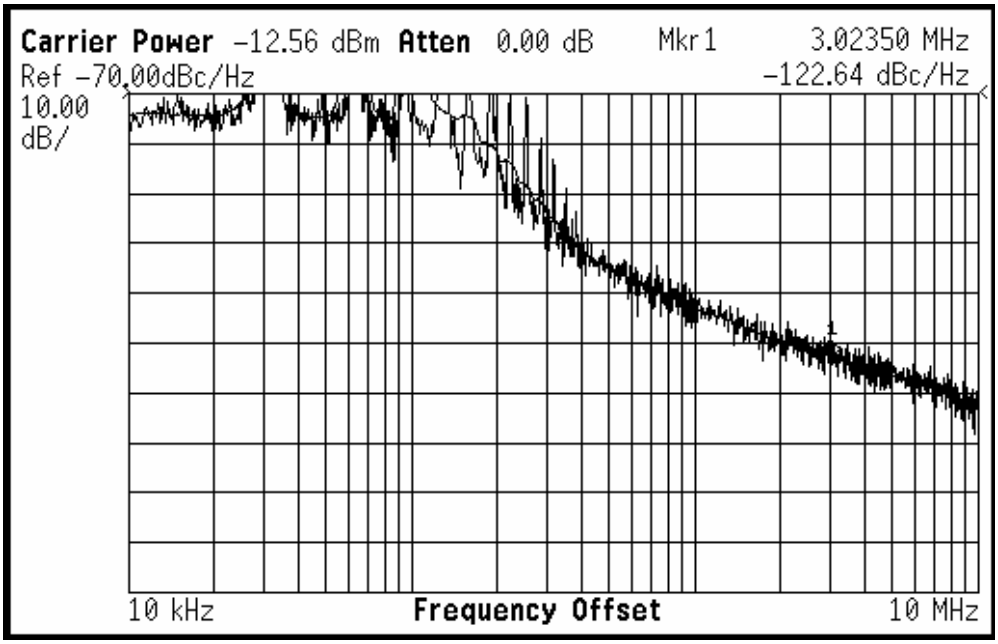


Figure 5.28. Measured phase noise while synthesizing 2.2 GHz

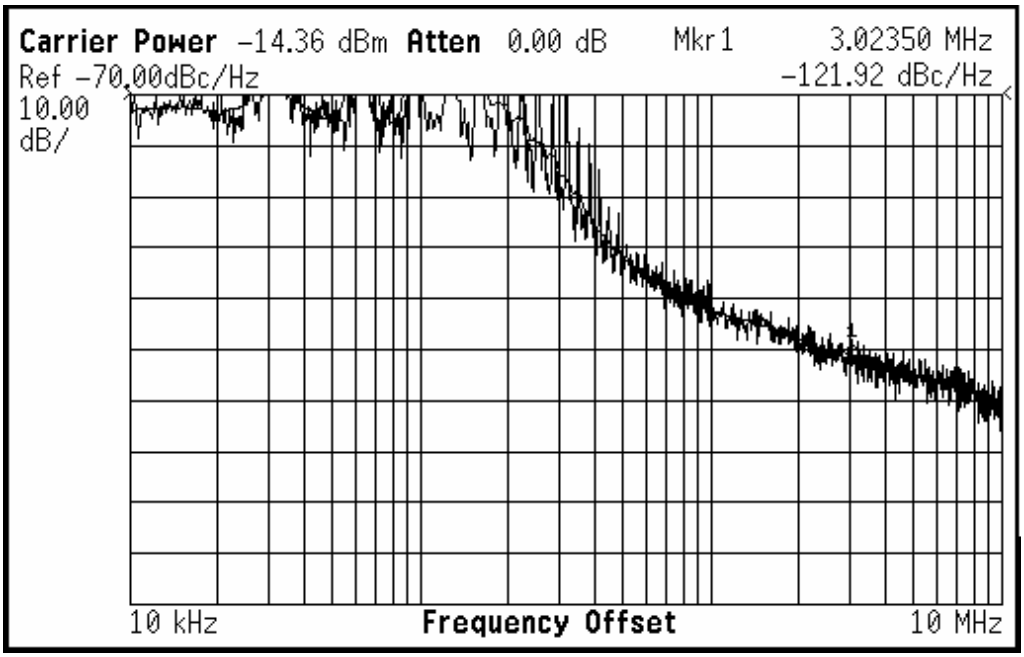


Figure 5.29. Measured phase noise while synthesizing 2.6 GHz

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Anticipated Original Contribution

- A Process and Temperature Stabilized (PATS) ring oscillator based on modified symmetrical delay cells
- A methodology for design of the PATS ring oscillator based on the velocity saturated drain current equation of short-channel MOSFET
- Expression for the frequency of oscillation of the ring oscillator using the modified delay cells
- Tracking/calibration circuitry that extends the locking ranges without consuming excessive power. This enables the prescalar to be used for multi-band operation
- Injection locked prescalar that has a locking range of wide-locking range (1.4 GHz) over all the process corners and a temperature range of 0°C to 100°C based on PATS ring oscillator
- Analysis of the effect of the fixed divide-by-4 prescaler on the over all noise of the PLL
- Design of a 2.4-GHz Frequency Synthesizer based on the proposed ILFD

6.2 Future Directions

- Comprehensive characterization of the ILFD with temperature. This Could not be done at this point due to the non-availability of the equipments at ORNL (Re-location and Construction)

- Design of Sigma-Delta Modulator on a FPGA/Chip
- Integrating the loop filter and bias currents on-chip
- Add features for in-loop GMSK modulation

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Vita

Rajagopal Vijayaraghavan was born on June 8, 1977 in Hyderabad, the capital city of the state Andhra Pradesh, India. He completed his secondary education at Jawahar Vidyalaya senior secondary school, Chennai, India. He got his Bachelors degree in electronics & communication from University of Madras and Masters degree in electrical engineering from University of Texas, Dallas in 1998 and 2001 respectively.

Rajagopal has been working towards his Ph.D degree since January 2003 under the supervision of Dr.Syed Kamrul Islam, who is also his major advisor. His research focuses on CMOS-based mixed-signal and radio frequency circuits that include PLL-based frequency synthesizers, frequency dividers and voltage-controlled oscillators. He has also worked on a variety of research projects that includes control circuits for use in maskless lithography using carbon nano-fibers, high temperature gate-driver circuitry for SiC power transistors and front-end circuitry for bioluminescent bioreporter based bio-sensors. As a graduate student Rajagopal has published 5 journal papers and 6 conference papers.

Towards the final stages of his Ph.D, he joined Cadence Design Systems, Inc. Cary, NC where he works on high speed serial links. Rajagopal is happily married to Ramya, who is currently working as a research associate in the nano-scale sciences and devices group at Oak Ridge National Labs, TN. His other interests include sports, travel and religion.