

An Integrated IGBT Active Gate Driver with
Fast Feed-Forward Variable Current

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Abstract

The Insulated-Gate Bipolar Transistor (IGBT) is a hybrid of bipolar and MOSFET transistors. As a consequence, IGBTs can handle higher current typical of bipolar transistors with the ease of control typical of MOSFETs. These characteristics make IGBTs desirable for high power Switch Mode Power Supplies (SMPS). In high power systems such as these, devices must be very reliable, as device failures may result in safety hazards such as fires in addition to the failure of the system.

Conventional Gate Driver (CGD) circuits typically design for reliability in these systems by including a resistor between the gate driver and gate of the IGBT. This slows the switching waveforms, reducing stress on the IGBT while sacrificing efficiency. This solution is suboptimal, however, and as such Active Gate Drivers (AGD) have been designed to control voltage and current slopes through the IGBT by modulating the gate signal.

AGD circuits found on the market today consist of a combination of an CGD with external components to implement the variable current necessary for protection. This requires a large amount of area on a Printed Circuit Board (PCB), and thus can be costly. Therefore, it can be desirable to integrate the AGD functionality into an on-chip system.

In this thesis, an AGD is designed, fabricated and analyzed to show that IGBT gate voltage can be controlled in a manner capable of reducing overvoltage, as well as slowed when desired using an on-chip system. The current provided by this gate driver is controlled by feedback signals indicating the switching state of the device, as well as input bits that determine total output current.

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Chapter 1

Introduction and Overview

Introduction

After three decades of development, insulated gate bipolar transistor (IGBT) power semiconductors are frequently implemented in a wide variety of switching voltage source power electronic converters where they are typically driving a clamped inductive load [1], [2]. IGBTs are typically chosen over MOSFETs as they are available in high-voltage and high-current ratings, are capable of withstanding short-circuit current up to 10 μ s, which contributes to the reliability of the power system, and they are easily controlled by the gate signal. They are generally robust devices, but due to the nature of their applications they are vulnerable to fail. It is estimated that around 38% of faults in industrial variable speed ac drives are due to the failure of the power device [3].

In addition, recent renewable energy applications have increased the demands on IGBTs, requiring higher voltage and current ratings, increased power density, faster switching speeds, better efficiencies, and increased reliability [4],[5]. There is therefore an increasing demand for and interest in developing systems capable of mitigating IGBT failures, especially in high power or high efficiency systems where faults can be very costly. In extreme cases where reliability is an absolute necessity, systems may even incorporate material redundancy with dual packs of IGBT units [6], [7]. For the most part, however, IGBT reliability is improved through intelligent design of the gate driver.

Conventional gate driver (CGD) circuits will typically design for reliability through the addition of a resistor in series between the gate driver and the IGBT gate. These resistors have the effect of reducing gate current and slowing switching waveforms, and are optimized to minimize switching losses and suppress crosstalk and electromagnetic interference while reducing the stresses on the IGBT during switching transients. However, fast switching transients reduce switching losses [5], and using series gate resistance effectively slows switching transients, reducing overall efficiency. Therefore, the design issues facing CGD design are at odds and very difficult to achieve simultaneously. Thus, active gate drive (AGD) circuits can be designed in order to more adequately achieve each of these goals [8], attaining reliability without sacrificing efficiency to the degree that CGD circuits do.

Motivation

Given the typical applications of IGBTs involves high power, design concerns such as component size and cost have been overshadowed by concerns of efficiency and reliability. As such, many active gate driver designs on the market prioritize functionality as the primary concern, resulting in systems comprised of discrete components with large footprints and cost. As increasingly high power systems emerge that are intended for commercial use such as electric vehicles or renewable energy systems, size and cost are becoming a greater concern. In this respect, simplicity in gate driver design can be a desirable trait such that cost and size may be reduced.

In most literature surrounding the subject of intelligent gate drive of IGBTs, systems proposed employ separate components for the gate current adjustments, resulting

in entire systems requiring large amounts of board area. Current gate driver microchips on the market can include protections for fault scenarios, but require external components to modulate the gate current, also resulting in a larger overall footprint.

This thesis proposes integration of feed forward protection from voltage and current overshoot into an on-chip system such that a single microchip can independently and intelligently drive and protect an IGBT using voltage and current slope feedback, while requiring minimal external components.

Overview

This thesis presents an IGBT gate driver IC designed to achieve desired switching behavior of an IGBT module through modulation of the gate current. This includes protection from voltage and current overshoot when necessary while minimizing switching losses. Emphasis is placed on low propagation delay from detection of IGBT state to modulation of gate current.

In Chapter 2, state-of-the-art methods of controlling IGBT switching transients are first reviewed and a closed loop integrated IGBT gate driver with di/dt and dv/dt control is proposed. Thereafter common IGBT stressors are overviewed, and the solutions implemented by the proposed IC for these stressors are presented.

Chapter 3 provides an in-depth analysis of the topologies chosen in the IC from system level to block level. Subsequently, simulation results are presented and discussed.

Chapter 4 gives the measured results achieved from first-run silicon, along with the test setup used to acquire these results. Measured results are compared to theoretical and simulated results obtained in the previous chapter.

Chapter 5 provides conclusions from the work, detailing enhancements that could be applied to the IC. In addition, possible courses for future work are presented.

Chapter 2

IGBT Switching Behavior and Control

Active Gate Driver Control

The primary task of an IGBT active gate driver is to switch the device at a desired di/dt and dv/dt in order to keep the IGBT within the safe operating area (SOA) [9]. This is accomplished by influencing the gate current, similar to the use of a series gate resistor in a CGD. As opposed to with CGD circuits, additional functionality is added to reduce the effect of gate resistance when not needed. This has been accomplished through the use of switchable or adjustable gate resistors [10], current sources / sinks [11-20], or gate voltages [21]. All of these approaches provide variable gate current to ensure operation in the SOA by achieving desired voltage and current slopes. Illustrations of these control methods can be seen in Figure 2.1. In part (a) of Figure 2.1, switches are opened or closed to change the gate resistance of the current path [10]. In part (b), the gate voltage can be continuously modulated by an external amplifier and variable voltage source. In part (c), gate current can be adjusted through the use of parallel current sources and sinks [22]. This approach is most akin to the one shown in this thesis, however the current sources are external devices used in addition to the current drive provided by a CGD. Lastly, in part (d), current sources are used as opposed to switching the gate node to respective voltage rails [23]. This provides the gate current drive immunity to effects from output devices leaving saturation or minimal inclusion of gate resistance. With the exception of the proposed IC, these systems are implemented as board-level solutions, and thus can grow to be large area depending on the type of IGBT being driven.

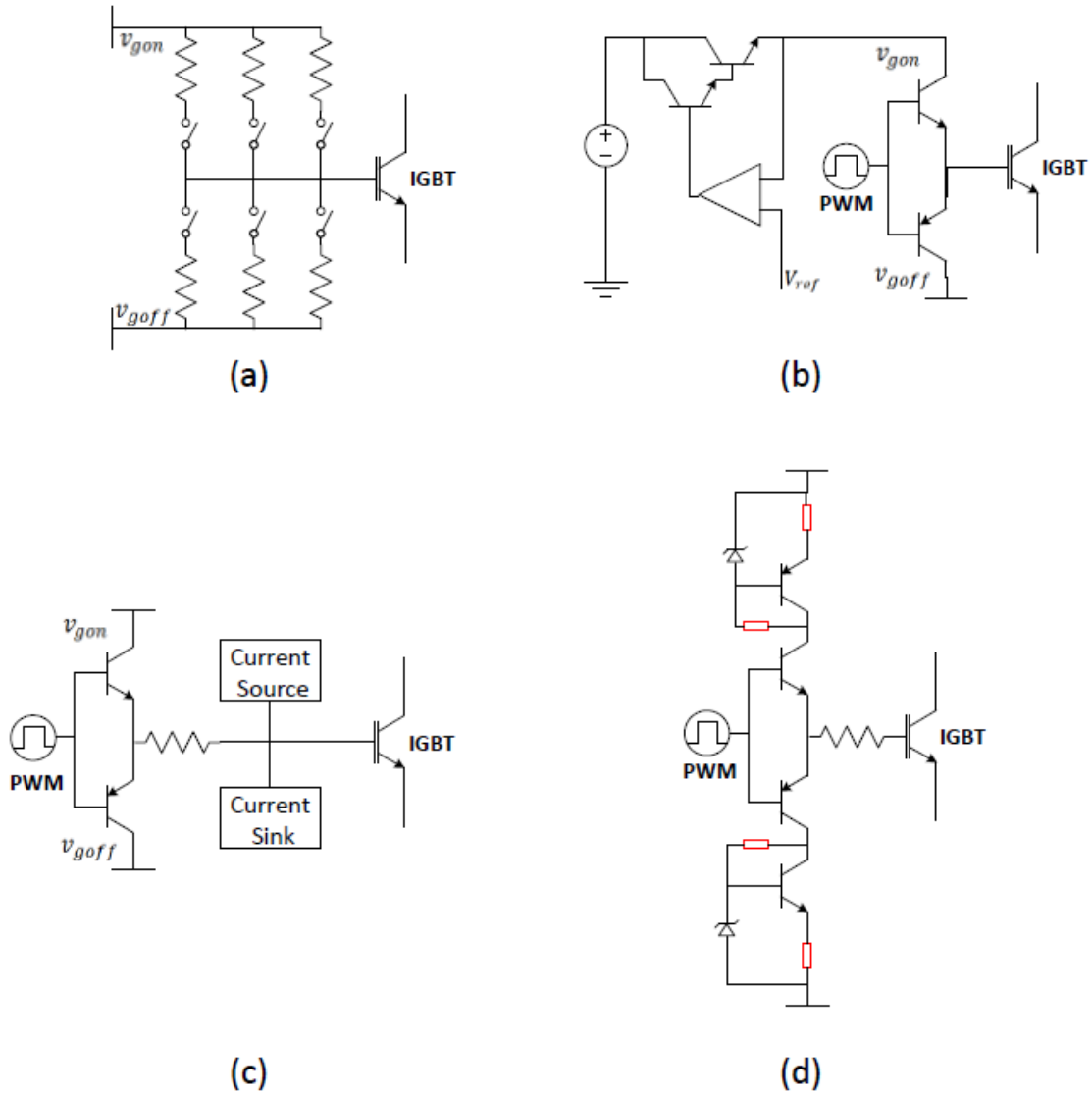


Figure 2.1 Example Gate Current Control Topologies: (a) Switchable Gate Resistors [10], (b) Variable Gate Voltage [8], (c) Current Sources and Sinks [22], (d) Current Source Gate Drive [23]

Additional features of active gate drivers including short circuit, overload, and desaturation protection have been extensively researched and developed, but will not be investigated in detail in this paper. As will be seen later, some IC gate drivers incorporate one or a few of these protections into their design, however they are most often designed off chip. Examples of these protections and their methodology can be seen in [24-29].

In order for active gate drivers to modulate the gate control signal and keep the IGBT in the SOA, they must receive feedback indicating the current state of the IGBT. This information can then be either processed by a digital control unit or be a part of an analog control loop. Digital control units presented in [30-32] offer sophisticated control of the V_{GE} , V_{CE} , and I_C of the IGBT by providing customized current profiles for each phase of the switching action. However, digital processing requires A/D and D/A conversions with delays from 50 ns up to 200 ns in the signal paths. As such, solutions such as these are not feasible for switching transients faster than 2 μ s, are expensive as the cost of the A/D and D/A converters is high, and are incapable of handling any significant change in system state between programmed switching operations.

As such, control methods using analog closed loop feedback of the di/dt and dv/dt signals [33], [34] are often chosen for better analog control bandwidth due to passive measurement circuits, possession of simple control amplifier stages, and requirement of less board area as well as cheaper components than similar digital solutions. Feedback solutions such as these can use different combinations of feedback signals for protection. It has been shown that protection control can be accomplished using only di/dt feedback

to protect during turn-on and turn-off [35-37], or di/dt feedback can be used for protection only during turn-on [38], [39]. Alternately, only dv/dt feedback can be used for protection during turn-off [39], or separate solutions can be used for protection during both turn-on and turn-off using both di/dt and dv/dt [40-42].

However, as the protection capability of an active gate driver increases, so too does its complexity. Increasingly complex control methodologies require comprehensive systems comprised of multiple active components and controllers, as well as passive components for operation status detection and biasing of the active components. These additional components require board area, raise overall system cost, and introduce new failure modes of the gate driver itself. It is therefore sometimes desirable to keep the gate driver control method as simple as possible to not only reduce cost, but reduce the number of failure modes while retaining a high analog control bandwidth. Active gate driver IC microchips on the market now typically add to the necessary conventional gate driver functionality with a few protection features such as Under Voltage Lockout (UVLO) or short circuit detection and/or protection. Only through the use of external components are protections such as those for overvoltage during turn-off and overcurrent during turn-on typically implemented. In Table 1.0 is a comparison of some of the gate driver ICs found on the market today, along with the gate driver presented in this thesis.

Table 1. Gate Driver Market Comparison

Gate Driver	Current Drive Sinking/Sourcing (A)	Max Output Voltage Swing (V)	Propagation Delay (ns)	Features and Notes
IX2204	4/2	35	70	UVLO, SC detection
EL7158	12/12	12	22.5	High Current
IGD508E	15/15	40	100	SC Detection & Protection
LM5114	7.6/1.3	44	12	Low delay, UVLO
Proposed	2.5/2.5	20	23	Low delay, Overvoltage & Overcurrent Protection

The gate drivers chosen for comparison in Table 1.0 were selected to show the tradeoff between the features of current drive, output voltage driving capability, propagation delay from an input signal to an output current, and additional control features. Going from the first to second IC shown, an increase in current drive and decrease of propagation delay is achieved, however the output voltage swing is much lower, and thus is best suited for MOSFET and not IGBT applications. Looking at the third gate driver shows that some intelligent features such as protection from short circuit of the IGBT sacrifices a large amount of propagation delay, and would thus not be well suited for high frequency or feedback control applications. Finally, the fourth gate driver provides low propagation delay and large voltage swing, though it is optimized for low-side IGBT configuration, and as such has much larger sinking than sourcing capability. It should be noted again that none of the gate drivers except for the proposed IC provide any sort of dynamic current during nominal switching. Instead, gate drivers such as these will be used for conventional gate driver functionality with short circuit protection, along with external circuits designed for additional protection.

The gate driver proposed in this thesis consists of only one IC capable of directly driving the gate of an IGBT, receiving di/dt and dv/dt signal feedback to determine the switching state of the IGBT, and using this information to modulate current to the gate of the IGBT. The method of detecting di/dt and dv/dt feedback will not be discussed as cost and size minimization of these circuits is a separate issue, however different methods of detection are compared in [43]. The intention of the proposed gate driver IC is to integrate IGBT protection functionality on-chip, in this case voltage and current overshoot mitigation of the IGBT by directly driving the IGBT and integrating the protection functionality into the gate driver IC. As can be noted from Table 1.0, this additional integrated functionality requires chip area and thus comes at the cost of output current drive capability. Therefore, the proposed IC is best suited for smaller IGBTs being used at higher switching speeds.

The proposed driver mitigates IGBT faults in a manner similar to most AGD circuits, through the modulation of gate current during fast switching transients. The variable gate current provided by the IC is achieved through the use of parallel current sources and sinks. An illustration is shown in Figure 2.2. When it is desired to reduce gate current, feedback output drivers of the opposite type (i.e. NMOS/PMOS) are activated to sink or source some of the current that was previously being provided to the IGBT gate. Each of these output drivers consist of segmented blocks that are individually activated, sinking or sourcing 100 mA each. The Primary Drivers consist of 25 blocks, while the Feedback drivers consist of 30 blocks. This way, output current can

be adjusted in 100 mA increments from 2.5 A to –500 mA to precisely control the speed that the IGBT will switch.

The four possible states that the gate driver can assume are reflected in this figure. Looking at Figure 2.2, in part (a) and (b) the Primary drivers are enabled, functioning as a conventional gate driver sinking and sourcing current to the gate of the IGBT according to an input PWM signal. In part (c) and (d) the complementary Feedback Drivers are activated by feedback di/dt and dv/dt signals. As there are more Feedback Drivers than Primary Drivers, the resultant current into the IGBT gate can be either positive or negative.

The gate driver is configurable such that the degree as well as timing of the gate signal modulation can be optimized for a particular IGBT or protection method. For example, the IC can be programmed to simply reduce gate current when the switching transient slopes are too high, effectively emulating a series gate resistor that is only present when needed. Alternately, the gate driver could be programmed for fault protection by turning off very slowly, or even turn back on, during a short circuit scenario when the switch is already on. If desired, multiple drivers could be placed in parallel to include both types of protection. Gate current levels as well as dynamic current adjustment levels are controlled by 20 input bits. These bits can be changed during testing of the IC and optimized for a particular IGBT. Once the desired current levels have been determined, these pins can simply be tied to the supply rail or GND in order to avoid the use of an external controller.

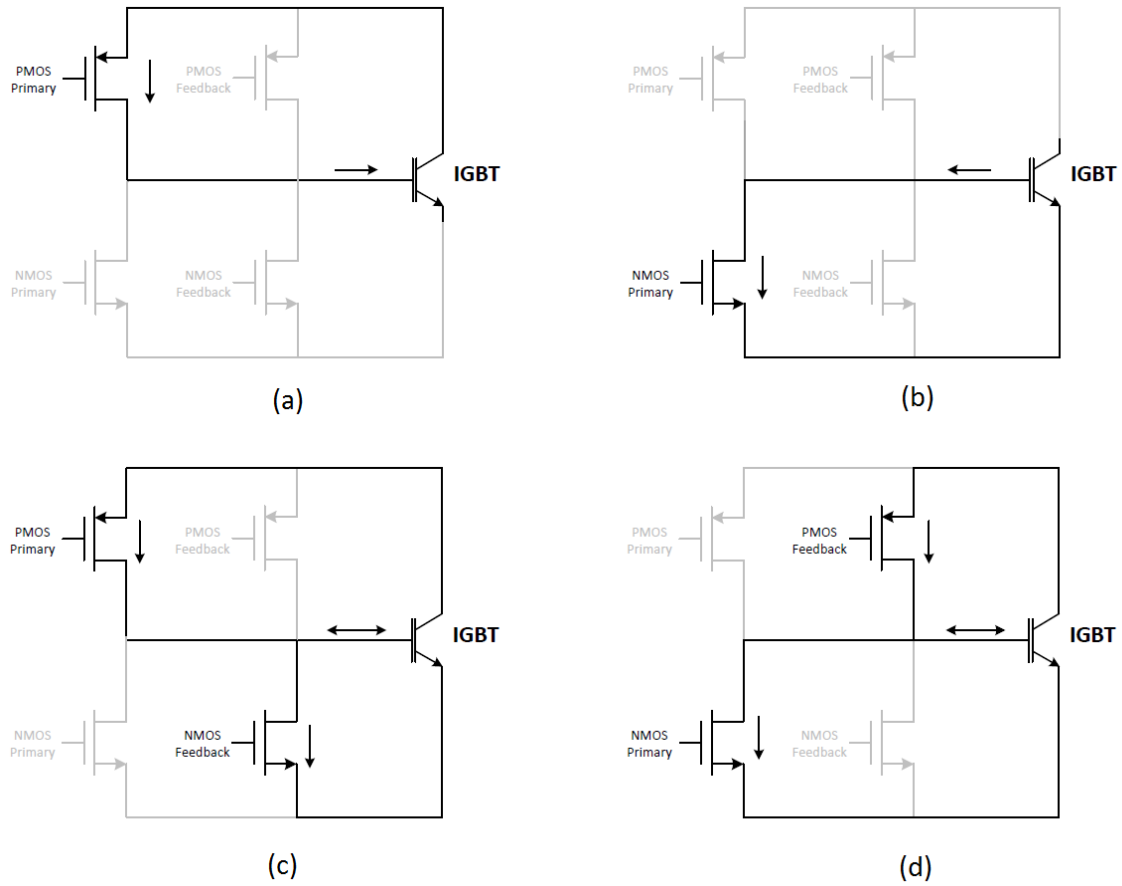


Figure 2.2 Proposed Gate Current Control Method: (a) PWM high no feedback compensation, (b) PWM low with no feedback compensation, (c) PWM high with feedback compensation, (d) PWM low with feedback compensation

Turn-On Overcurrent

The sub circuits in Figure 2.3 are found in many SMPS designs, and will be used to illustrate some of the issues encountered during switching transitions. Both figures, while exhibiting different circuit states, will yield the same analysis. The switch in these figures may be any semiconductor power switch, however IGBT modules are considered here. The diode in these sub circuits may be either a discrete diode or the intrinsic body diode, both of which will exhibit similar characteristics for the purposes of this discussion. Prior to the IGBT switch turning on, the diode will be carrying the entirety of the inductor current while the switch has no current through it aside from parasitic currents. As the switch begins to turn on and increase its current, the diode current will decrease at a rate determined by its material properties. Note that according to Kirchhoff's Current Law (KCL) the inductor current equals the sum of the switch current

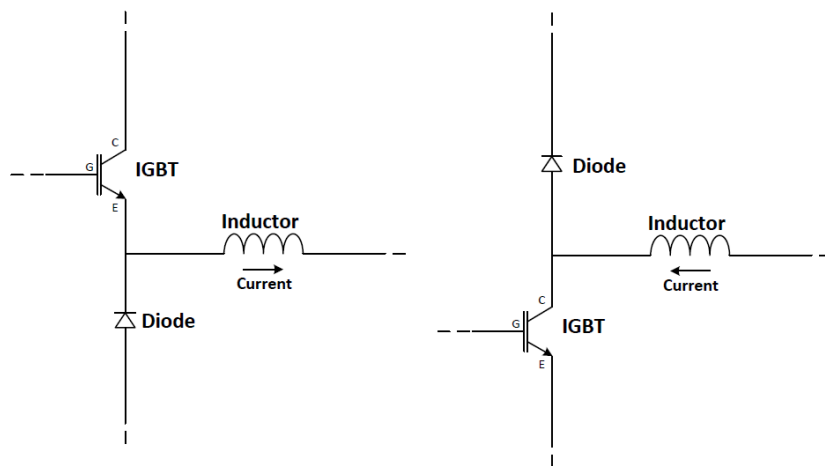


Figure 2.3 Generalized Switchmode Subcircuit

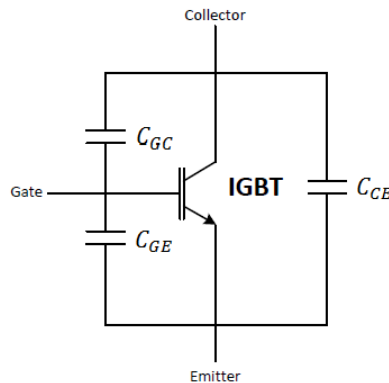


Figure 2.4 IGBT Module Parasitic Capacitances

and the diode current. That is, the diode current is directly proportional to the switch current.

IGBTs possess parasitic capacitances between each of its three terminals, seen in Figure 2.4. These parasitic capacitances allow for a phenomenon known as the Miller-Effect. The Miller Effect is associated with the feedback of the collector-emitter voltage V_{ce} through the gate-collector capacitance C_{GC} .

Any change in the voltage across the capacitances in Figure 2.4 will result in a current, with the currents direction dependent on the polarity of the voltage change. It is also worth noting that the value of the gate-collector capacitance is not constant, but instead changes its value according to the collector-emitter voltage. This means that while turning on the IGBT, once the voltage across the collector-emitter nodes of the switch begins to fall, current that was previously charging the gate emitter capacitance and increasing the gate voltage will instead charge the gate-collector capacitance with no effect on the gate voltage. The gate-collector capacitance value is increased the most

when the collector emitter voltage approaches zero, therefore even after the collector emitter voltage has come to a low value the gate-collector capacitance is increased greatly and continues to consume the entirety of gate current. Provided there is a constant current sourced into the gate of the IGBT by the gate driver, the gate voltage will be kept relatively constant while the gate collector capacitance is increasing and being charged. It is only once the current needed for charging the gate-collector capacitance becomes smaller than the bias current that the gate voltage begins to rise again. This phenomenon is known as the Miller plateau and can be observed in Figure 2.5.

As the IGBT continues to turn on and conduct more current, the diode will reach zero current and subsequently pass into what is called reverse recovery mode [44]. During this phase, the diode will conduct negative current as the diode returns from its forward bias state and is replacing the charge carriers intrinsic to the diode. Again, note that because the switch current and diode current are proportional, the switch will be

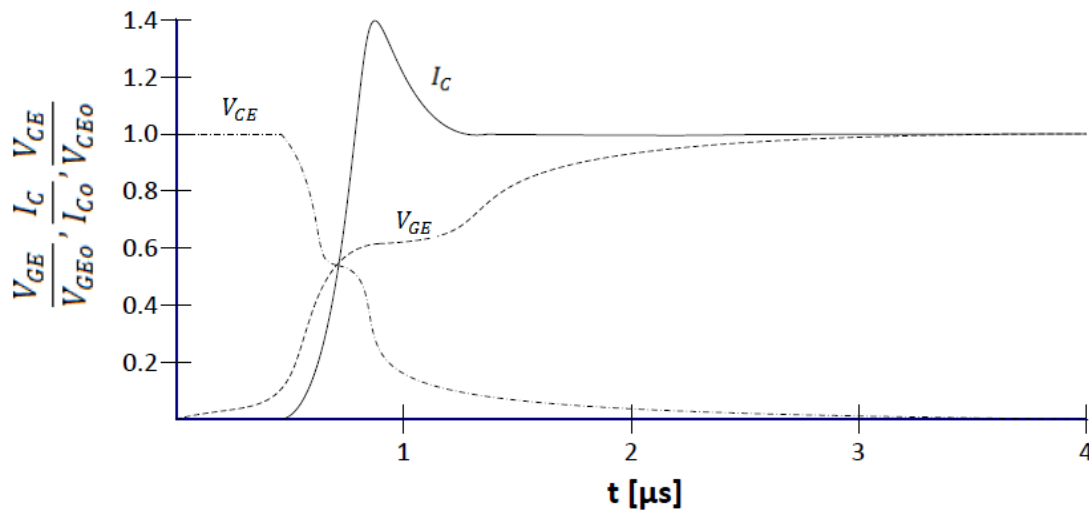


Figure 2.5 Generalized IGBT Turn On Switching Waveforms

providing the current for the diode's reverse recovery. Once the diode conducts enough reverse current to reach its zero-bias state the current will begin to approach zero at exponentially decreasing rate. This negative current will then charge the diode capacitance, creating a voltage across the diode and reducing the voltage across the switch. It is not until this point that the switch will appear to be turning on in the sense that the voltage across it is reducing.

If the diode does not complete its reverse recovery process before the IGBT begins to carry all of the inductor current, then the IGBT will be forced to conduct more than the steady state operational current, or that of the inductor. This can be seen in Figure 2.5, which depicts generalized IGBT turn on waveforms. The IGBT current will continue to increase its current as long as there is enough charge stored in the diode to support the rate of increase in current. After it has reached its maximum value, the diode's reverse current begins approaching zero. The IGBT current then reduces to carry only the inductor current as the it is no longer providing the current for the diode's reverse recovery.

During low load conditions, i.e. when the inductor current is low, there will be less stored charge in the diode when the IGBT begins to turn off. This means that the reverse voltage of the diode will increase more quickly as the effective capacitance of the diode is lowered and the diode voltage will snap back to zero current more quickly. When this occurs, the switch node will experience ringing proportional to the amount of stray inductance and the level of current overshoot. If the ringing has too much

amplitude the diode's breakdown voltage will be exceeded and it will cross into avalanche, likely resulting in a failure of the component.

Current overshoot through the IGBT is mitigated by reducing the gate drive current through the use of a series gate resistance. This improves device reliability by effectively slowing the rate at which the IGBT turns on and increases current. As the switch current is directly correlated to the reverse recovery current, a lower current slope allows more time for the diode to receive the reverse recovery charge that it needs before the IGBT begins pulling all of the inductor current.

While the addition of gate resistance effectively increases the reliability of the IGBT by preventing current overshoot and diode overvoltage, it has the disadvantage of increasing switching time. This can be seen in Figure 2.6, which demonstrates switching waveforms at different gate resistances. In the figure the dotted line represents a generalized switching waveform with an increased gate resistance. While the current overshoot is reduced, the overall time of the switching transition is increased. As

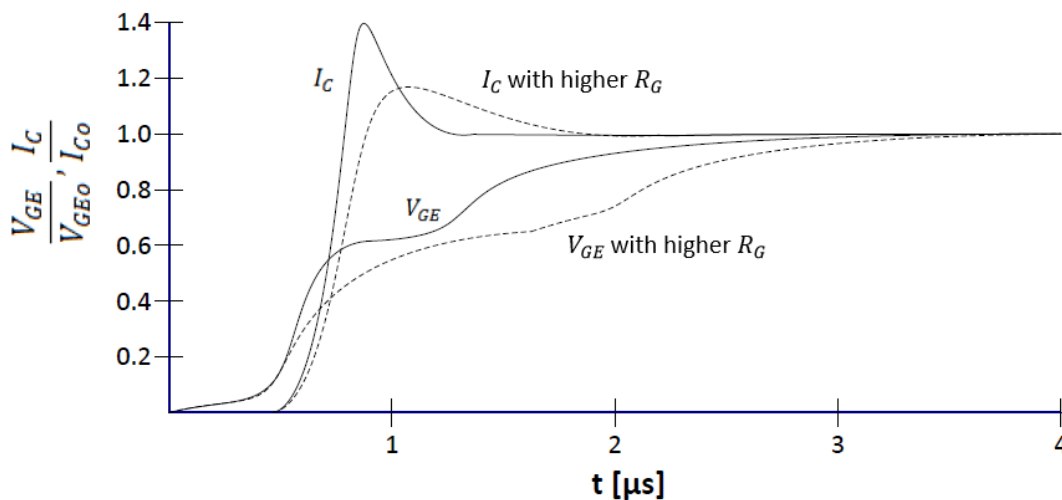


Figure 2.6 IGBT Turn On Waveforms with Additional Gate Resistance

increasing the switching time decreases efficiency, an optimization process is used to balance the reliability and efficiency of the design. Often, the limiting factor in the design for reliability is the minimum load supported, as it is during this condition that the diode is most likely to break down due to low stored charge, and a resultant high reverse voltage peak. Therefore, the series gate resistance is increased until an acceptable amount of ringing is seen at the switch node while supporting minimum load. This means that when the SMPS is supporting anything above minimum load, the switching response is overly damped, sacrificing efficiency at higher loads in order to satisfy reliability requirements, and effectively reducing overall switching efficiency.

Active gate drivers such as the one proposed in this thesis reduce gate current only when switching transients, in the case the current slope, are detected to be too large. This way, adjustable current drive can emulate the presence of a gate resistor by slowing the switching speed when needed, without unnecessarily slowing switching transitions when it is undesirable to do so, such as during heavy loads. Given the short timescale during which switching transitions occur, it is desirable to have minimal delay between detection of an overly large current slope, and reduction of gate current. In the proposed gate driver IC, integration of feedback mechanisms into the IC allows for fast adjustment of gate current as current modulation takes place within the microchip. Additionally, the proposed gate driver has the capability of adjusting the current slope threshold at which gate current is reduced, as well as the degree that the current is reduced. This flexibility can be used to optimize the gate driver for individual systems driving different IGBT modules. Therefore, the gate driver can be configured to emulate the desired series gate

resistance, and only do so when an undesirably large current slope through the IGBT is detected.

Turn-Off Overvoltage

When the switch is being turned off, seen in Figure 2.7, the Miller Effect will cause current to travel from the collector node into the gate as the collector-emitter voltage rises. However, in order for the collector-emitter voltage to rise, the gate voltage must be brought below the threshold value. Therefore, the gate voltage will first decrease at a rate determined by gate discharge current until the collector-emitter voltage begins to rise. Once the collector-emitter voltage begins to increase the gate-collector capacitance will decrease sharply. This decrease in gate-collector capacitance will cause stored charge to increase the gate voltage, further preventing the gate from lowering its voltage and keeping it in the Miller plateau. This charge that was previously stored in the

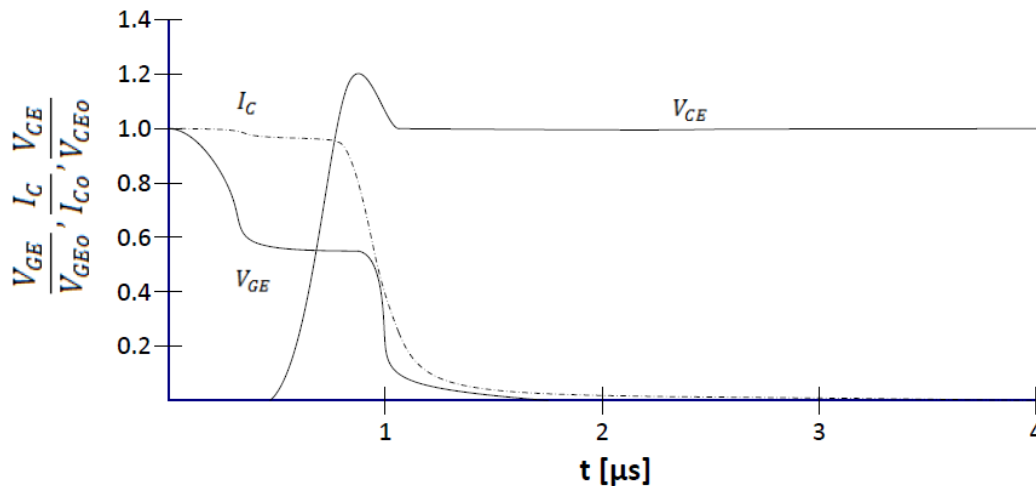


Figure 2.7 Generalized IGBT Turn Off Switching Waveforms

gate-collector capacitance will then need to be drained by the gate driver, consuming all of the gate current for a time. Once the gate-collector capacitance is fully discharged, which occurs partly through the Miller plateau, the collector emitter voltage begins to rise. The switch will stay within the Miller plateau until the collector-emitter voltage roughly reaches the steady state operating voltage. Gate current will then be directly discharging the gate emitter capacitance, and the gate voltage will again decrease at a rate proportional to gate driver current.

During IGBT turn off, when collector emitter voltage reaches the switch node voltage, current through the IGBT begins to decrease. The slope of this current reacts with parasitic inductance to create an overvoltage across the IGBT. Inclusion of series gate resistance can slow the switching transients and reduce the current slope responsible for the voltage overshoot. Again, this comes at the cost of decreased switching efficiency. In addition, this current slope for IGBTs is sensitive to a desaturation of the semiconductor [45-47]. Lower gate current resultant of high series resistances can result in stored charge in the drift region of the IGBT being partly extracted, increasing the current slope through the IGBT, and actually increasing the overvoltage. Therefore, in some designs the issue may be faced where a series gate resistance of a certain value is needed for optimal turn-on of the IGBT, but results in increasing the voltage overshoot during turn-off. As such it is desirable to independently modulate the turn-off and turn-on waveforms rather than including a gate resistance that affects both.

Instead of inclusion of a gate resistor, IGBT overvoltage encountered during turn

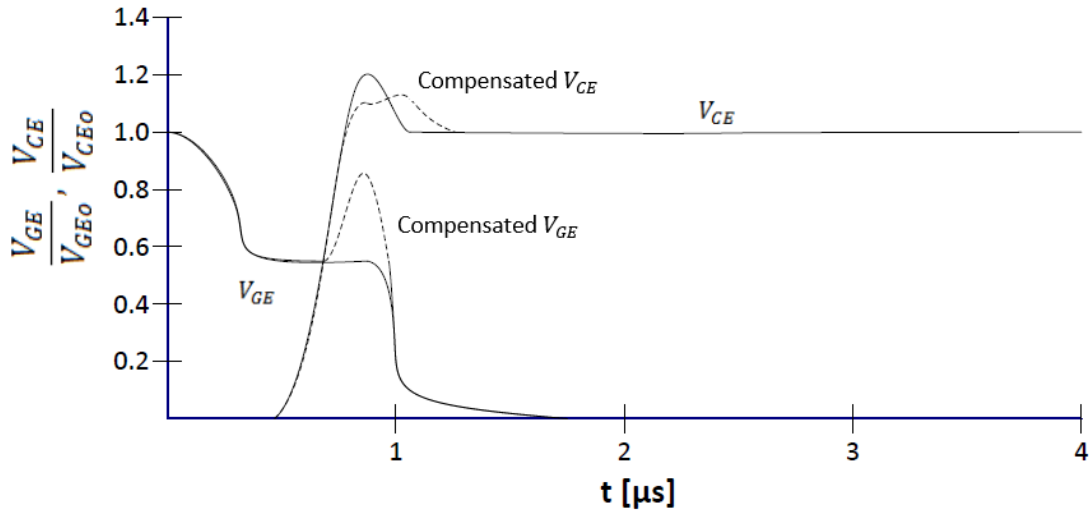


Figure 2.8 IGBT Turn On Waveforms with Voltage Overshoot Compensation

off can be reduced using a different method. By temporarily modulating the gate voltage during the turn-off process when either the voltage across the IGBT is increasing or the current through the IGBT decreasing, the current slope that is responsible for the voltage overshoot can be reduced, effectively reducing the overvoltage [48]. The resulting waveform can be seen in Figure 2.8.

This type of compensation is implemented in the proposed IC by detecting the voltage and current slopes of the IGBT and modulating the gate current in order to maintain a gate emitter voltage that drives the IGBT with the desired overshoot. Depending on the IGBT, switching speed, and other parasitic inductances arising from layout of the entire system, the voltage overshoot will have different magnitudes. For some applications simply reducing the gate current during the phase that the voltage across the collector and emitter of the IGBT is increasing will be enough to mitigate

voltage overshoot. For other applications it may be necessary to stop gate current altogether, or even reverse current flow, and turn the transistor back on during this phase. The proposed IGBT can be configured for either of these scenarios by modifying gate current in 100 mA increments, or even reversing gate current up to 500 mA if needed.

Chapter 3

Design of the Dynamic Current Gate Driver

System Overview and Block Diagram

The gate driver is designed with the following goals. It is to provide up to 2.5 A of sinking or sourcing current dictated by a PWM signal. This current is to be adjustable in 100-mA increments, and provided from -5 V to 15 V . The gate driver is also designed to accept di/dt and dv/dt feedback, which is used to adjust the output current from $\pm 2.5\text{ A}$ to $\pm 500\text{ mA}$, also in 100-mA increments. The gate driver is designed to have minimal propagation delay such that the di/dt and dv/dt signals influence the output current drive as quickly as possible. In addition, the delay of the di/dt and dv/dt signals may be adjusted through an input DC current bias. The block diagram for the system can be seen in Figure 3.9. There are four primary block types: Comparators, Analog Delay, Selection Logic, and Current Drivers.

While the IGBT gate sees voltages from -5 V to 15 V , these voltages will henceforth be referred to as 0 to 20 V unless otherwise specified for ease of reference as this range more accurately describes the gate drivers internal voltages.

The gate driver utilizes a push-pull output stage configuration to provide both sinking and sourcing current drive. The Primary and Feedback PMOS Drivers will source current to charge the IGBT gate to 20 V, while the Primary and Feedback NMOS Drivers will sink current to discharge the IGBT gate to 0 V. The Primary Current

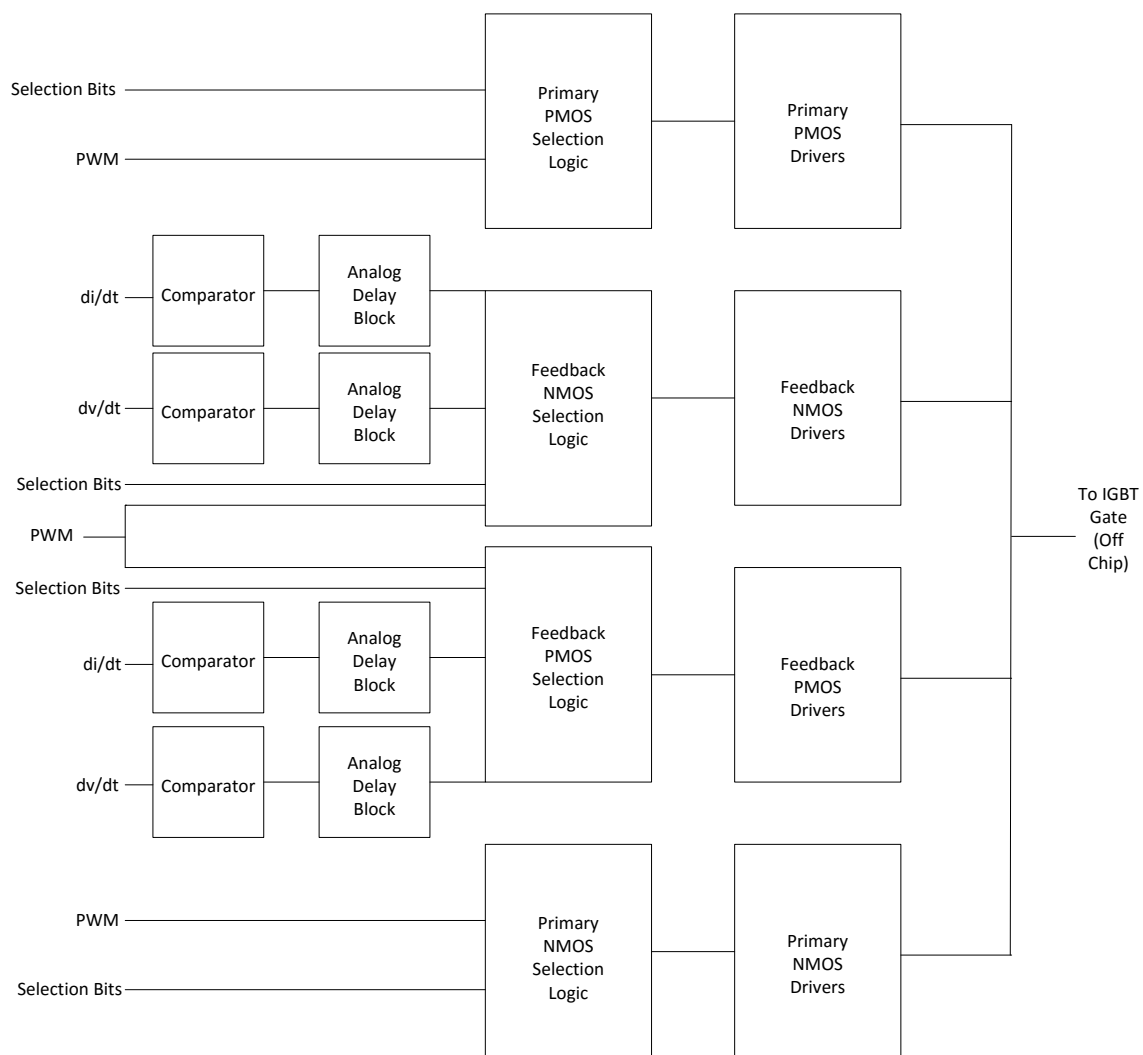


Figure 3.9 Proposed IC Top Level Block Diagram

Drivers, seen in the block diagram as the top and bottom signal paths, act as a conventional gate driver. That is, they will charge and discharge the gate of an IGBT to the supply rail with the same polarity as an input PWM signal. The Primary NMOS and PMOS Driver Blocks consist of 25 individual driver blocks in parallel, each sized to allow 100 mA of current.

Included before these driver blocks are Selection Logic blocks. These Selection Logic blocks receive a decimal value between 0 and 31 in the form of 5 separate binary bits that exist as 0 V or 5 V to convey a “0” or a “1”, respectively. This 5-bit number is decoded using logic gates, and the Selection Logic block then enables the decoded number of 100 mA Primary Current Driver blocks. This allows the adjustment of the Primary Current Driver output current from 0 A to 2.5 A in 100-mA increments. Individual selection bits are used for the PMOS and NMOS Current Drivers, allowing for separate current levels for sinking and sourcing.

These selection bits are static and not intended to be changed dynamically. They are included such that the gate driver can be optimized for different IGBT modules. Therefore, once the gate driver has been optimized for a particular configuration, these bits can be tied to the 5 V supply rail or GND, without the use of a controller.

As seen in the block diagram in Figure 3.9, the middle two signal paths are responsible for driving the Feedback NMOS and PMOS drivers, and provide additional functionality as compared to a conventional gate driver. The Feedback Drivers are used to reduce the current provided by the Primary Drivers. That is, the Feedback NMOS drivers sink current sourced by the Primary PMOS drivers, and the Feedback PMOS

Drivers source current to be sunk by the Primary NMOS drivers. This effectively reduces the final current that is sunk or sourced by the gate driver to its load. Like the Primary Current Drivers, the Feedback Current drivers consist of individual 100-mA blocks in parallel that are controlled by preceding Selection Logic blocks. However, the Feedback Drivers consist of 30 instead of 25 driver blocks, sinking or sourcing up to 3.0 A. Therefore, if more Feedback Drivers are enabled than Primary Drivers of the opposite type, the gate driver will reverse its output current direction.

As an added functionality, if the propagation delay of the signals is too short and the Feedback Current Drivers are being activated prematurely, the Analog Delay block is included to tune exactly when the Feedback Drivers are enabled. This way, the feedback di/dt and dv/dt signals are used to determine when the IGBT is switching, and the Analog Delay block can be used to control precisely when current level is modulated. This delay is adjusted by sourcing a small DC current, creating a delay related to input current.

The comparators are used to receive the di/dt and dv/dt signals. The comparators receive an input voltage proportional to the di/dt and dv/dt of the IGBT provided from off-chip. By using a comparator, a threshold voltage can be set to dictate how high the di/dt and dv/dt signals must be to activate the Feedback Current Drivers. Once a di/dt or dv/dt signal is detected to be above the desired threshold, an output a digital logic signal is sent to enable the appropriate Feedback Current Driver.

The gate driver is capable of driving the IGBT gate to 15 V or $-5V$. In order to accomplish this, the blocks within the IC must operate between different sets of rail voltages. The lowest voltage the IC sees must be the substrate voltage, therefore what is

negative 5 V to the IGBT is GND for the IC, what is GND to the IGBT is 5 V to the IC, and so on. All signals passing through the chip are binary “high” or “low” signals. The devices in the process used to create this chip have a gate-oxide thickness that tolerates approximately 7 V of gate-to-source voltage, so transistor gates were designed to experience 5 V of voltage swing. Therefore, each blocks' voltage rails are separated by 5 V, and level shifters are utilized between blocks where necessary.

A major constraint of the system design was that the digital logic gates within the Selection Logic blocks could only exist between the 5 V and GND rails of the IC due to a technology constraint. Because of this, positive di/dt or dv/dt signals that will exist between 5 V and 10 V relative to the IC have to be level shifted down to be passed into the Selection Logic block. Furthermore, as the PMOS drivers consist of transistors that will have a “high” voltage of 20 V as seen by the IC, and their gates cannot experience more than 7 V of voltage swing, the PMOS Driver blocks must exist between 15 V and 20 V relative to the IC. This requires that the signals be level shifted up from GND to 5 V, up to 15 V to 20 V.

Circuits that have a low voltage rail of 5 V or above require isolation to prevent device breakdown into the substrate. This includes Comparators that detect positive di/dt or dv/dt input signals, PMOS current drivers, and level shifters.

Comparators

The input comparators receive a voltage signal from off chip proportional to the di/dt and dv/dt across the IGBT collector and emitter terminals, and sense when these

signals exceed a given threshold. A separate comparator is used for each signal, and both of the Feedback Current Driver signal paths have a pair of input comparators, resulting in 4 total comparators in the design. As the ground of the IGBT is 5 V referenced to the gate driver, a zero reading for the di/dt and dv/dt signals will rest at 5 V. When a positive di/dt or dv/dt is detected across the IGBT, the voltage will increase above 5 V, and when a negative di/dt or dv/dt is detected, the voltage will decrease below 5 V. As such, some comparators will exist between 0 V and 5 V, while others will exist between 5 V and 10 V.

In a practical application of the proposed gate driver, the required inputs for the NMOS current drivers to be active are a negative dv/dt and a positive di/dt , therefore the comparator for dv/dt would exist between 0 V and 5 V while the di/dt comparator would exist between 5 V and 10 V. Conversely, for the PMOS drivers a positive dv/dt reading and negative di/dt reading are required, placing the dv/dt comparator between 5 V and 10 V and the di/dt comparator between 0 V and 5 V. For testing purposes, as feedback signals were to be emulated, both the comparators for the PMOS Feedback current drivers were placed between 5 V and 10 V, and both the input comparators for the NMOS Feedback current drivers placed between 0 V and 5 V. The threshold that determines the input voltage at which the comparator outputs an active high signal is received from off-chip, resulting in a total of 4 threshold values.

In order to use the same comparator design for both positive and negative signal detection, a rail-to-rail input stage was implemented. This is because for the comparators

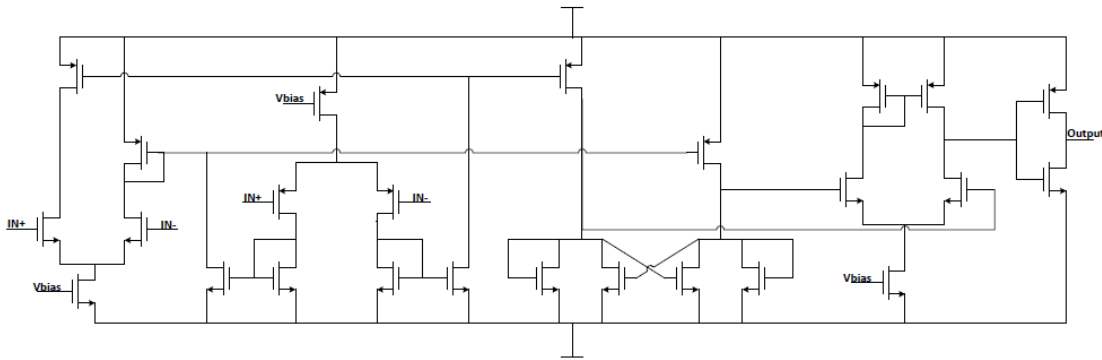


Figure 3.10 Comparator Schematic

existing between 0 V and 5 V, the input signal will rest on the higher supply rail and swing down when a negative di/dt or dv/dt is detected. On the other hand, for the comparators existing between 5 V and 10 V, the input signal will rest on the lower supply rail and swing upwards when a positive di/dt or dv/dt is detected.

The comparators consist of three separate stages, seen in Figure 3.10 [61]. The first stage consists of complimentary PMOS and NMOS differential pairs in order to achieve the rail-to-rail functionality desired. The second stage consists of a positive feedback active load. This stage is responsible for receiving current mode signals from both the NMOS and PMOS input differential pairs, deciding which signal is larger through the use of positive feedback, and converting it into a differential voltage mode signal for use by the third stage. Subsequently, the third stage consists of a differential amplifier configured to amplify the differential voltage received from the second stage and output a single-ended voltage signal to an output buffer.

The tail current sources of the comparator are biased using two Beta Multiplier Reference (BMR) circuits. Due to the fact that the comparators exist between two

different pairs of voltages, two BMR circuits exist that create the bias voltages of approximately 7.5 V and 2.5 V. The schematic seen in Figure 3.11 is an example of a Beta Multiplier Reference circuit. The designed output voltage was set at midrail such that it could properly bias both NMOS and PMOS devices. Layout extracted simulations placed the resulting output voltage at 3.2 V, which simulations showed to be acceptable. Examples and details of BMR circuit design can be seen in [49].

The most desirable metric of the comparator is minimum propagation delay, as will tend to be the case throughout the IC. For the first stage this required a large transconductance of the input differential pair, and thus large W/L ratios for MOSFET sizing as well as biasing with large current. To accomplish this, the tail current transistors of the complimentary input pairs were sized in order to provide 4 mA of current, leaving 2 mA of current per differential branch.

For the second and third stages propagation delay was minimized by balancing

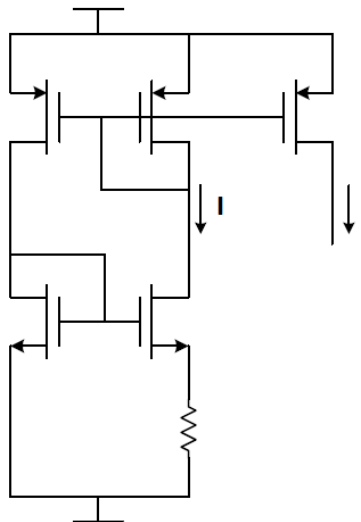


Figure 3.11 Beta Multiplier Reference Circuit Diagram [49]

the transistor W/L ratios with the surrounding stages. These stages must be large enough to quickly charge and discharge the gates of the subsequent stage, while also being as small as possible to be charged and discharged by the previous stage as quickly as possible. For example, in the second stage, the positive feedback cross-coupled gate connected transistors should be relatively small such that they may change states and quickly determine which current is larger, while the tail current transistors feeding current to these transistors should be larger in order to ensure that enough current is available to charge and discharge the differential pair of the third stage, as well as feed current to the positive feedback decision transistors. The third stage was designed in a similar fashion as the first stage, with a tail current transistor biased by the BMR and sized to pull 4 mA. The input differential pair transistors were sized again to minimize propagation delay, making them as large as the second stage was capable of quickly driving.

Figure 3.12 depicts the resulting propagation delay of the comparator when a square wave is input, with the comparison voltage set to mid rail. It can be observed that the rising edge and falling edge have slightly different propagation delays. While efforts were made during design of the comparator to have equal propagation delay for both edges, parasitics resulting from layout resulted in unequal delays. The resulting positive edge propagation delay is approximately 3 ns, while the falling edge propagation delay is 2 ns, resulting in a 1 ns difference in delay times.

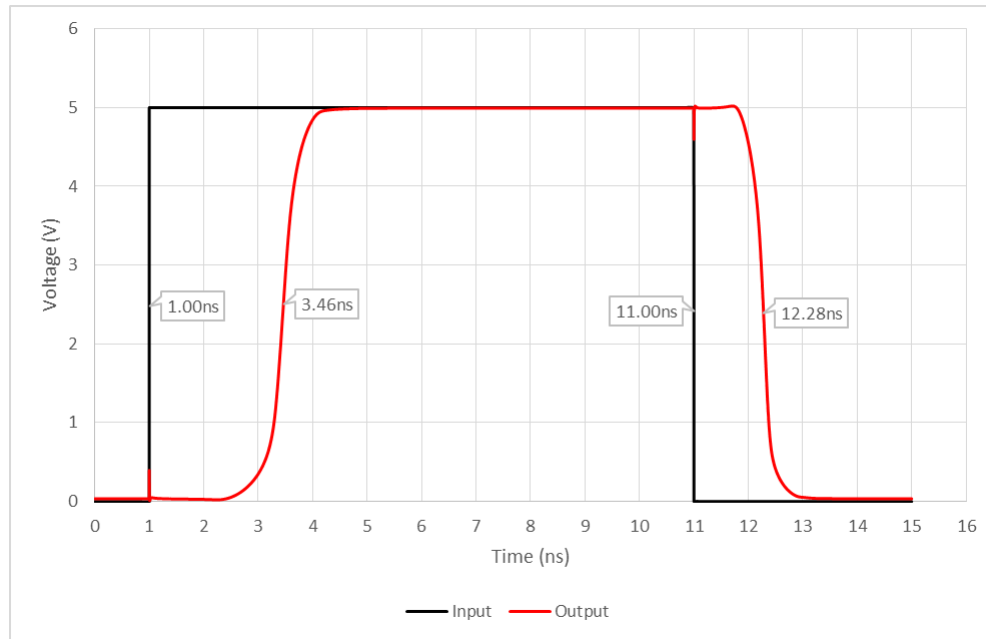


Figure 3.12 Comparator Propagation Delay

Level Shifters

Within the System Level Block Diagram seen in Figure 3.9 there are two points where the feedback signal must be level shifted. The first is after the comparators that feed into the PMOS Feedback Current Drivers. At this point, the signals must be shifted *down* from between 5 V and 10 V to between 0 V and 5 V. The second point is after the Feedback PMOS Selection logic block. At this point the signals are instead shifted *up* from 0 V and 5 V up to 15 V and 20 V. Unfortunately, both of these level shifters are within the signal path for the Feedback PMOS Current Drivers. As level shifters are the largest contributor to signal propagation delay, this means that the Feedback PMOS Driver signal path will be significantly slower than the Feedback NMOS signal path.

Two separate level shifters were designed in order to accommodate shifting both to a higher and to a lower voltage range. The same general topology was used for both;

however, the entire topology was “flipped”, switching NMOS devices into PMOS devices and visa versa to create complementary versions.

Within the level shifters, there must be a node that is allowed to swing the full range of the input to output voltage. That is, this node must be capable of handling the highest and lowest voltages of the input and output signals without causing any devices to breakdown. This was accomplished in both circuits through the use of Drain Extended MOSFET devices, or DEMOS transistors. While these transistors have similar gate oxide thickness to other MOSFETs in this process technology and cannot handle any larger voltage differences between the gate and source, the drain of the device is extended in order to allow for larger voltages between the drain and the gate and source of the device. For this IC, devices were chosen that are capable of handling up to 20 V of voltage swing at the drain of the devices. In the topology chosen, both an N-type DEMOS and a P-type DEMOS have their drains tied together, thus allowing the node connecting them to make the full voltage swing.

With a node capable of handling the voltage swing, the task of translating the signal from high voltage to low voltage is still necessary, as the high voltage node itself is not tied to any gates and is thus passive. Therefore, the topology in Figure 3.13 and 3.14 is chosen. Here, two input DEMOS devices are driven with complementary signals. Therefore, when the input signal is high, one branch will allow current while the other branch will not. When current is passing through one of the branches charge will accrue at source of the DEMOS, creating the voltage desired. However, this node is also connected to the drain of a load transistor that is driven by the complementary branch.

Therefore, if the complementary branch begins to provide current, it will turn on this load transistor, depleting the node that was previously being charged and changing the voltage, also changing the voltage on the source of the DEMOS in the other branch. Through this use of positive feedback between the two branches, two node voltages will be created that swing between the new higher or lower voltage rails, achieving the level shifting desired. A second stage is then included with a similar method of positive feedback in order to create a stage that exists solely between the desired voltage rails. This is necessary as the first positive feedback nodes may not always swing the between entirety of the new voltage rails, and it is desirable to output signals that have high and low logic values equal to those of the voltage rails.

Propagation delay is the most desired metric again, and as was the case when designing for minimum propagation delay in the comparators, sizing of the transistors is done stage by stage. Following the signals through the circuit, each transistor is sized to be small enough to minimize its gate capacitance and be quickly driven by the previous stage, while being large enough and having sufficient transconductance to provide the current necessary to quickly drive the subsequent stage. For the level shifters, this means that the first input DEMOS transistors were made as large as the inverter was capable of driving. The next complementary DEMOS pair that holds the high voltage nodes was similarly sized to be large enough in aspect ratio (W/L) such that their transconductance did not impede the switching of the positive feedback tied transistors. Note that this pair of DEMOS devices are of the opposite type of the preceding two DEMOS devices.

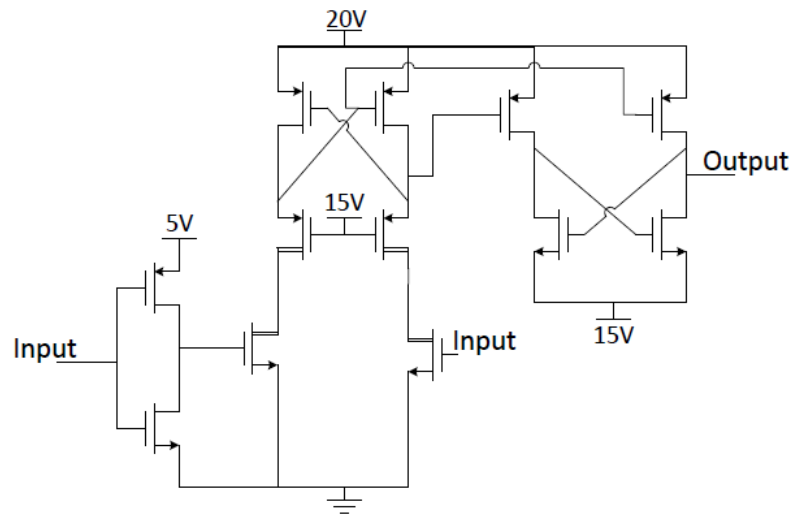


Figure 3.13 Level-Up Shifter Schematic

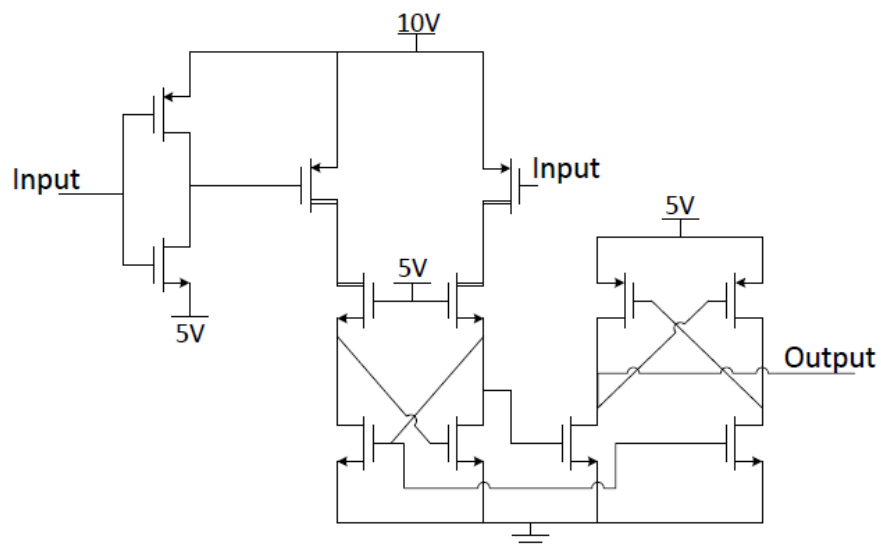


Figure 3.14 Level-Down Shifter Schematic

Next, the positive feedback transistors were made relatively smaller. Even though their transconductance directly affects how quickly the feedback nodes control drain current, their drain-to-source capacitance holds the actual level shifted voltage, and determine the amount of current that is needed to change voltage level. Finally, the output stage of the circuit is sized to be large enough to drive the subsequent stage, or the input inverter of the analog delay block.

The level shifters that translate signals to a higher voltage precede the PMOS current driver cells. As the output driver cells consist of large transistors, they will possess large gate capacitances that require higher current in order to quickly turn on and off. Therefore, the level shifter variant that translates signals upwards required a larger output stage than the level-down shifter.

Simulation results can be seen in Figures 3.15 and 3.16. Note that the level-up shifter results in a noninverting shifted waveform, while the level-down shifter results in an inverted waveform. This is due to the fact that the output of the two topologies is selected from two complementary and inverted nodes, which can be seen in Figures 3.13 and 3.14. Output nodes were selected in order to yield equal rising and falling edge propagation delays.

The Level-Up Shifter demonstrates significantly larger propagation delay than the Level-Down Shifter. This is due to the fact that the Level-Up Shifter is increasing the voltage rails of the signal by 15 V as opposed to decreasing by 5 V, and thus requires more current and more time to accrue the charge necessary to build this difference in voltage. The simulated delays are recorded below in Table 2.

Table 2. Level Shifter Propagation Delays

	<i>Rising Edge Delay</i>	<i>Falling Edge Delay</i>
Level-Up Shifter	8.13 ns	9.29 ns
Level-Down Shifter	3.37 ns	2.72 ns

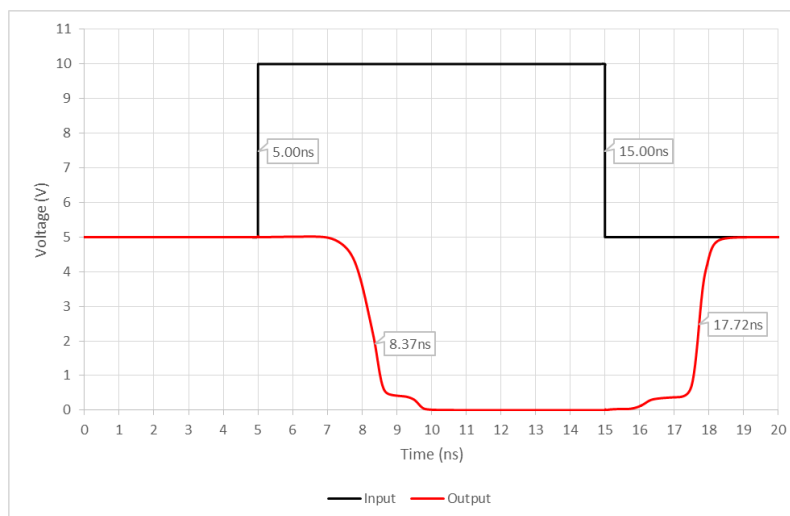


Figure 3.15 Level-Down Shifter Propagation Delay

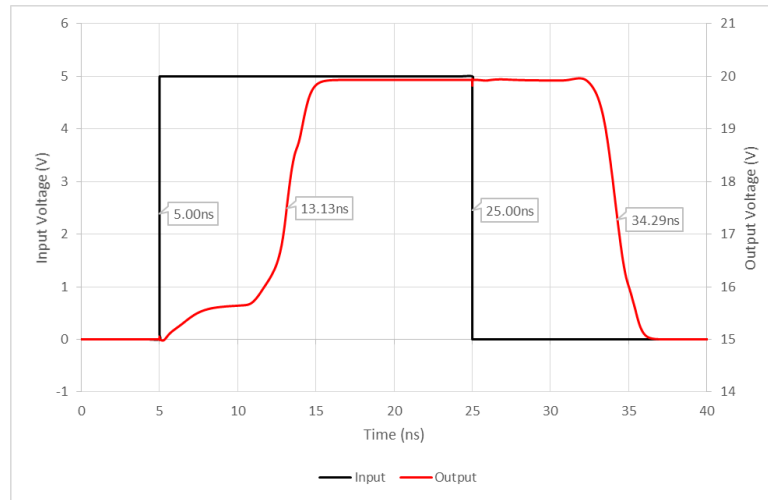


Figure 3.16 Level-Up Shifter Propagation Delay

Analog Delay Block

The analog delay blocks receive the di/dt and dv/dt signals from the comparators or level-down shifters. The purpose of the delay block is to introduce an adjustable delay between the input di/dt and dv/dt signals and the current driver blocks. This delay is essential for timing when exactly the Feedback Current Drivers are enabled. The delay block exists between the GND and 5 V rails of the chip, and thus does not require any isolation. The blocks are intended to adjust the delay of each signal individually.

The delay of each signal is determined by an input current sourced from off-chip. In addition, each delay block has a bypass transmission gate that may be activated in the case that minimal delay is desired. These transmission gates are enabled by an off-chip voltage of 5 V. In total, there are 8 signals sourced from off chip to control the delay blocks, 4 current-mode signals that determine the delay of the circuit, and 4 voltage signals that determine if a transmission gate is activated to bypass the delay block.

The topology used is what is referred to as a series of current-starved inverters [62]. This is shown in Figure 3.17 where the first two inverter stages source current into BJT devices. These BJT devices sink an amount of current equal to a current provided from off chip, and in turn determines the amount of current that flows through the first two inverter stages. The less current that each inverter stage is allowed by the BJT, the longer it takes to charge or discharge the subsequent stage input node, and thus a delay is introduced. This delay may be adjusted by changing the amount of current allowed through the BJT devices. Two current-starved stages are necessary in order to ensure that the positive and negative edges of a square wave signal are equally delayed. Two additional inverter stages are also included. The third inverter stage is present to keep the number of inversions even, while the fourth inverter stage also includes blocking transistors that are turned off whenever the bypass transmission gate is active.

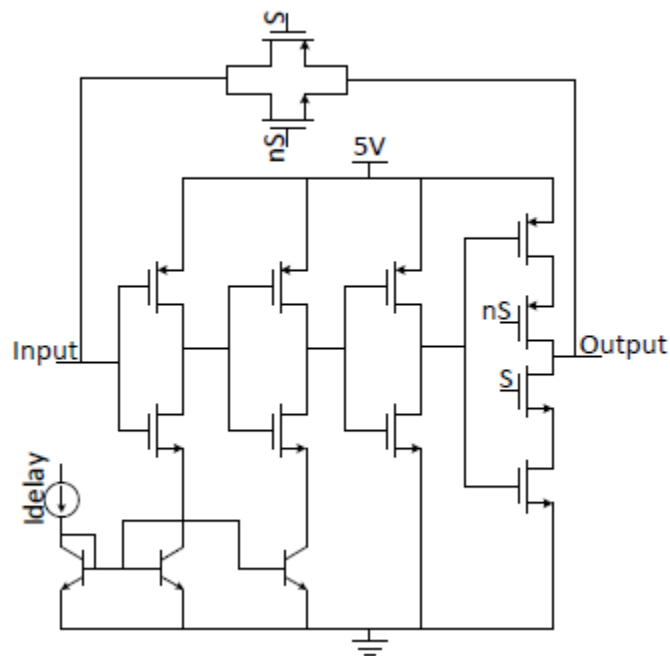


Figure 3.17 Analog Delay Block Schematic

In order to size the current-starved inverter stages it is necessary to know the desired range of delays as well as range of input currents used to set those delays. For this IC, a delay of 500 ns is achieved with an input current of 10 μA , and the minimal possible delay was to be approached with an input current of 100 μA . These ranges are set by the sizing of the current-starved inverter stages. The larger they are, the more current drive is required to switch them, thus more delay is introduced at low bias currents.

The amount of propagation delay introduced is not linearly related to the input current. Instead, it increases exponentially as the input current is reduced. Near this threshold, very minute changes in current will drastically influence the delay of the signal. To avoid requiring a precision current source, the first two inverter stages are properly sized to avoid uncontrollable propagation delay. The current mirroring BJT devices are all equally sized in order to deprive each stage of equal amounts of current. The final two stages are buffers, and were optimized for minimal delay.

The resulting range can be seen in Figure 3.18. Layout parasitics increased the delay produced by 10 μA from 500 ns to 600 ns. Additionally, Figure 3.19 depicts that the transmission gate introduces negligible delay.

Current Level Selection Logic

Each of the 4 current level selection blocks (Primary NMOS, Primary PMOS, Feedback NMOS, Feedback PMOS) are responsible for selecting the level of current to be driven by their corresponding set of output drivers. To make this decision, the

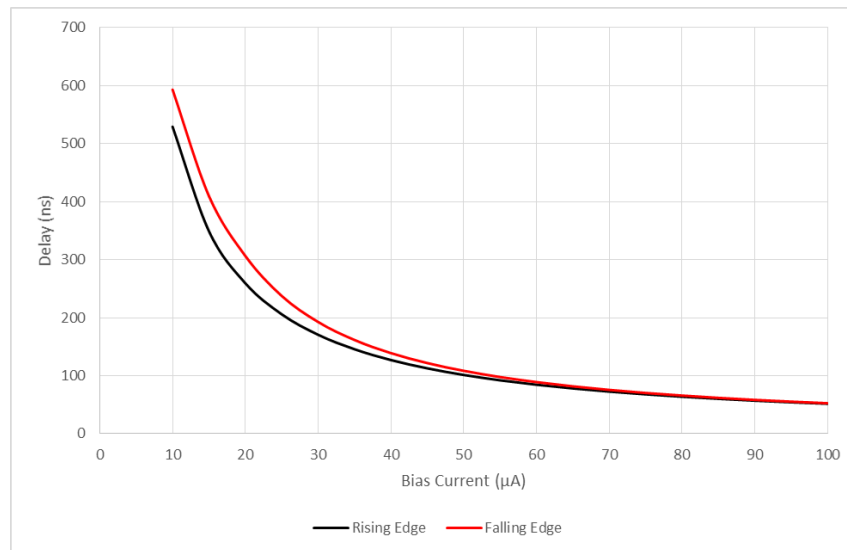


Figure 3.18 Analog Delay Block Delay Range

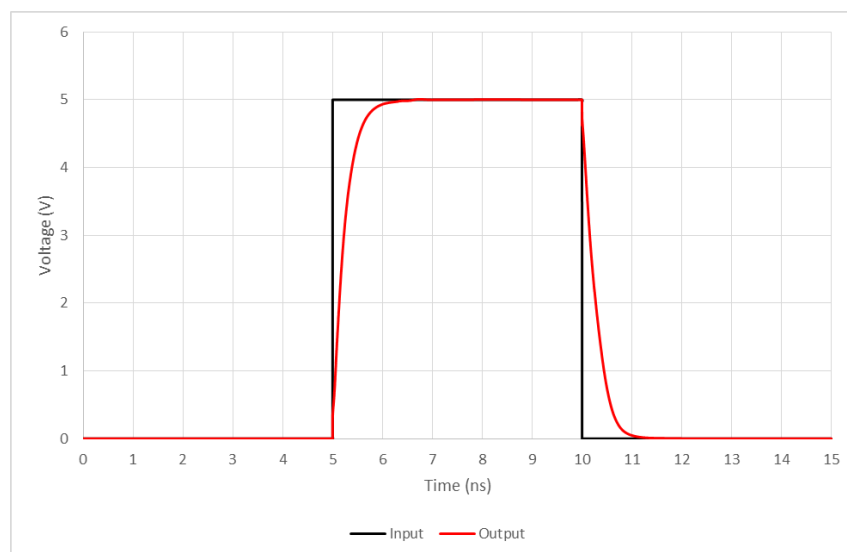


Figure 3.19 Analog Delay Block Transmission Gate Propagation Delay

Selection Blocks require 5 input binary selection bits and a PWM signal. The Selection Blocks for the Feedback current drivers also require the di/dt and dv/dt signals.

The PWM, di/dt , and dv/dt signals all determine when each respective Current Driver Block (NMOS/PMOS, Primary/Feedback) should be enabled. The resulting amount of current to be output is determined by 5 input selection bits. The input selection bits are interpreted as a binary number, and this number of current drivers are then activated. An input of “0 0 0 0 0” will provide no current, an input of “0 0 0 0 1” will provide 100 mA of current, an input of “0 0 0 1 0” will provide 200 mA, and so on.

As the current drivers consist of 100 mA blocks, the Selection Blocks possess one logic output for each 100 mA driver. Therefore, the Primary Selection Logic blocks have 25 total outputs, and the Feedback Selection Logic blocks have 30 total outputs, one to each current driver block. Each current driver block will have its own logic function to determine if it should be activated. The driver blocks are activated when the input selection value is equal to or greater than a certain number. For example, one driver may be active whenever the input value is 12 or greater, while another is active only when the input is 22 or greater. The resulting truth table can be seen in Table 3, where the selection bits are labelled as 0-4, with 0 being the least significant bit.

The logic functions in Table 3 responsible for interpreting the input selection bits are present in each of the four Current Level Selection blocks. As such it is designed as a standalone block to be reused in each of the four Selection blocks. While the input selection bits directly control the amount of output current, they are not intended for dynamic current adjustment in the manner discussed in Chapter 2. The dynamic current

is provided by the Feedback Current Drivers. Therefore, the functions present in Table 3 are used as static logic outputs. These static logic outputs are used in conjunction with the dynamic signals, i.e. PWM input, di/dt , and dv/dt , to determine when current driver blocks should be active. These dynamic signals are desired to have minimal propagation delay through the Current Level Selection blocks, and should therefore see as few logic gates as possible. Therefore, the dynamic signals are combined into one final logic gate with the resultant logic output from the static logic. This way dynamic signals only experience the delay from one logic gate. Example logic paths can be seen in Figure 3.20, where it can be seen that for the Primary Current Driver blocks the dynamic PWM signal only passes through one logic gate, and for the Feedback Current Driver blocks the dynamic PWM, di/dt , and dv/dt signals also see only one logic block.

Current Drivers

The schematics for the PMOS and NMOS output stages can be seen below in Figures 3.21 and 3.22, respectively. It can be seen that the PMOS output stage has one less buffer stage. This is due to the fact that a level shifter precedes each PMOS current driver block. The level shifters designed have more proportional delay on the rising and falling edges when providing an inverted output signal. Therefore, with an extra inversion in the PMOS signal path, one less buffer stage is used to retain an even number of inversions.

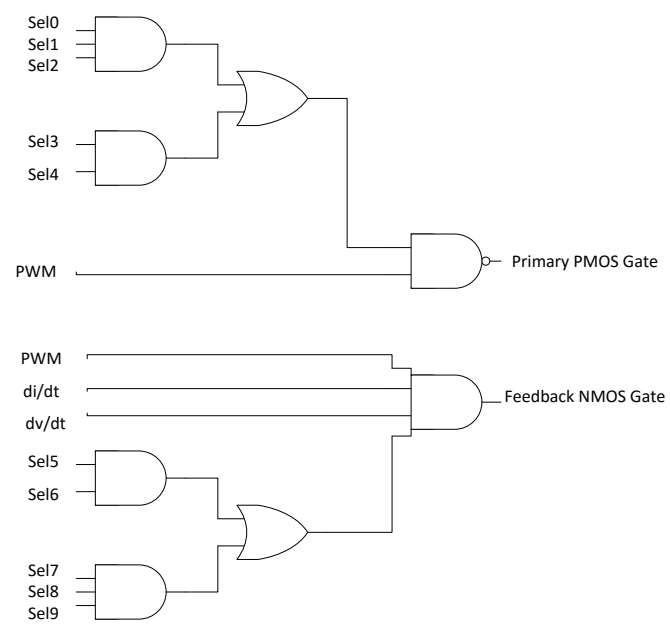


Figure 3.20 Current Level Selection Block Example Gates

Table 3. Current Level Selection Block Truth Table

Current Driver	Selection bits
1	$0+1+2+3+4$
2	$1+2+3+4$
3	$0*1+2+3+4$
4	$2+3+4$
5	$0*2+3+1*2+4$
6	$2*1+3+4$
7	$2*1*0+3+4$
8	$3+4$
9	$3*(0+1+2)+4$
10	$3*(1+2)+4$
11	$3*(0*1+2)+4$
12	$3*2+4$
13	$3*2*0+3*2*1+4$
14	$3*2*1+4$
15	$0*1*2*3+4$
16	4
17	$4*(0+1+2+3)$
18	$4*(1+2+3)$
19	$4*(0*1+3+2)$
20	$4*(3+2)$
21	$4*(3+2*0+2*1)$
22	$4*(3+2*1)$
23	$4*(3+2*1*0)$
24	$4*3$
25	$4*3*0+4*3*1+4*3*2$
26	$4*3*1+4*3*2$
27	$4*3*2+4*3*1*0$
28	$4*3*2$
29	$4*3*2*1+4*3*2*0$
30	$4*3*2*1$

With the output transistor width dictated by the current driving capability, preceding buffer stages were included in order to properly drive the output transistor. The buffers preceding the output transistor have exponentially increasing widths in order to minimize propagation delay [63]. For the PMOS current driver blocks seen in Figure 3.22, the output of the preceding level shifter was sized to properly drive the single buffer before the output transistor. Figure 3.23 and 3.24 show the current drive of the PMOS and NMOS transistors over output voltage. It can be seen that the output current remains at or near 100 mA until the output voltage comes within 5 V of the rail. This is to be expected because the transistors are leaving saturation as the drain to source voltage approaches 0 V. Figure 3.24 shows two separate curves for the NMOS current drivers. The black curve is the result of intended design simulation, where 100 mA is sourced, while the red curve is from simulations extracted from layout, and only sinks 75 mA of current. This occurred due to a redesign late in the design process. The output transistor was sized larger than the processes layout design rules allowed, and was split into two

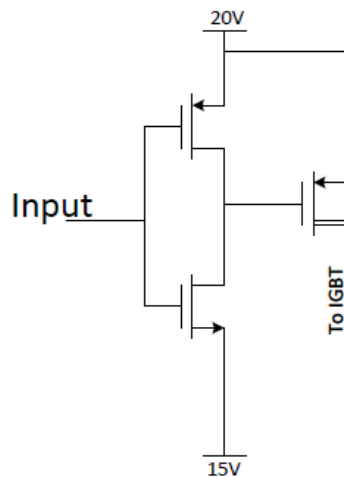


Figure 3.21 PMOS Current Driver Block Schematic

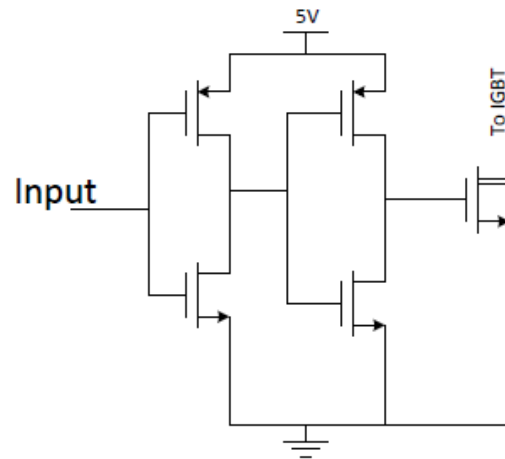


Figure 3.22 NMOS Current Driver Block Schematic

separate transistors of half width to satisfy the design rules. The two half width transistors did not output equivalent current, and the output driver cells had already been placed and could not be grown any larger without redesign of the majority of the IC. This was not an issue with the PMOS transistors, and thus layout extracted simulations of the PMOS current drivers yielded the expected 100-mA current drive. The propagation delay of both current driver blocks was less than 1 ns.

System Testing and Performance

There are four different states that arise from the combination of the PWM, di/dt , and dv/dt signals. The Primary Current Drivers should be active during the correct PWM state, whereas the Feedback Current Drivers activate when the correct di/dt and dv/dt inputs result in the comparator triggering, in conjunction with the proper PWM input.

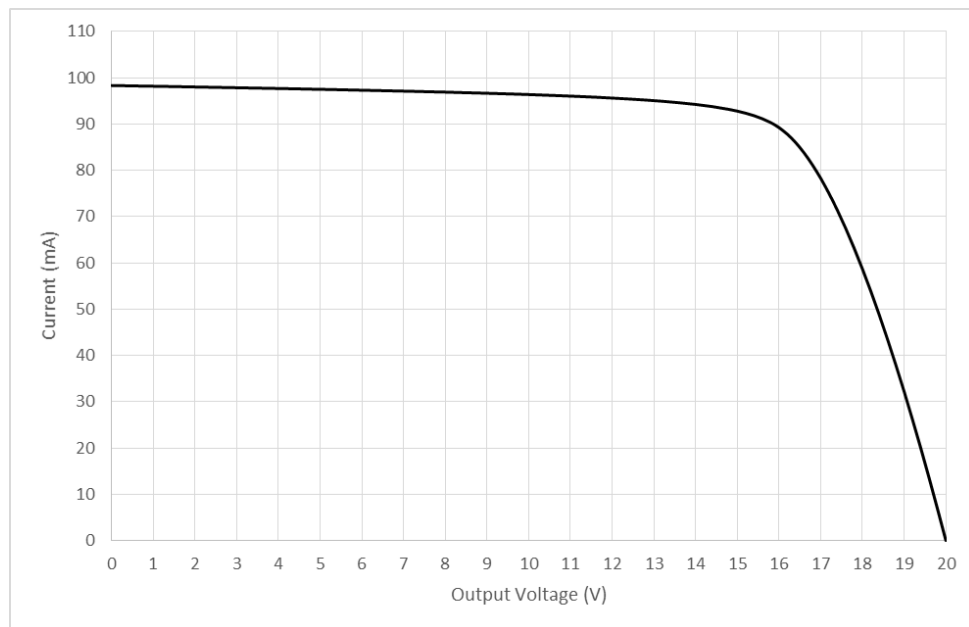


Figure 3.23 PMOS Current Driver Drive Current

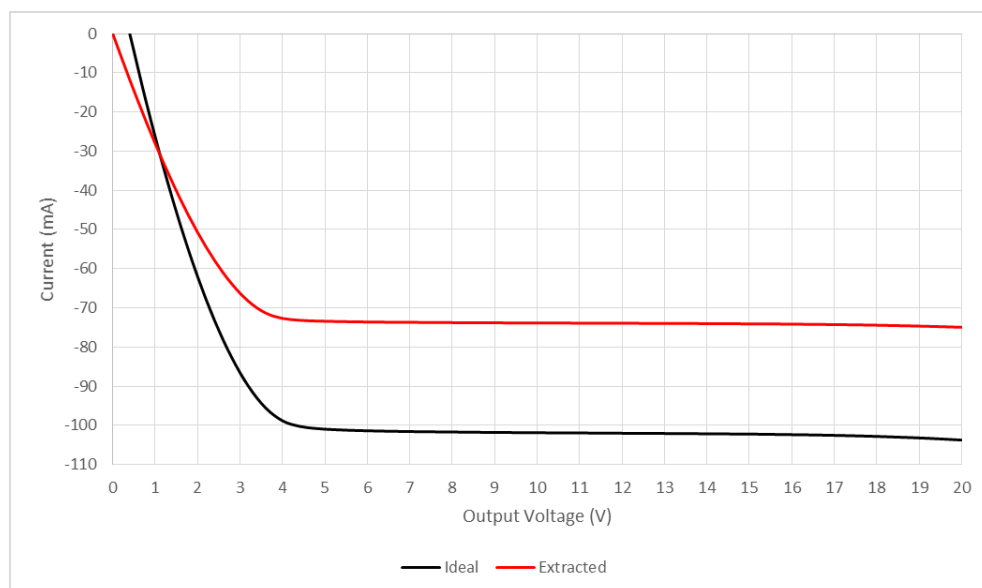


Figure 3.24 NMOS Current Driver Current Drive

For example, the Feedback NMOS Current Drivers should be active while the Primary PMOS Current Drivers are active and the di/dt and dv/dt signals are low. The input di/dt and dv/dt signals were originally intended to be active high signals, however the pin assignment of the positive and negative input to the comparators was reversed, resulting in an active low signal. A table summarizing the propagation delay of each of the signal paths as well as maximum current drive can be seen below as Table 4.

The simulation stimuli used to test overall functionality can be seen in the Appendix as Figure A.38. In it the PWM, di/dt and dv/dt signals are swept to cover all four states, ensuring that the correct current drivers are active and determining the overall propagation delay of each signal path. The resulting current drives can be seen in the Appendix as Figures A.39 through A.42. It can be seen that the Feedback PMOS signal path has significantly more delay than the others. This was expected due to the fact that the signal must pass through both the Level-up and Level-down Shifters, which produce the largest delays of all blocks.

Table 4. Chip Level Simulation Current Driver Metrics

Current Drivers	<i>Activation Delay (ns)</i>	<i>Deactivation Delay (ns)</i>	<i>Max Current Drive (A)</i>
Primary PMOS	10.27	11.38	2.41
Primary NMOS	3.81	2.68	1.85
Feedback PMOS	25.65	23.63	2.89
Feedback NMOS	5.78	7.3	2.22

Design and simulation of the proposed IC was segmented into separate circuits in the signal path. By minimizing propagation delay of each individual circuit, total propagation delay could be minimized. Simulations were done for each individual circuit as well as for the entire signal path to ensure that each intermittent circuit was capable of driving the subsequent circuit. Layout extraction simulations and redesign to abide by layout design rules impacted intended circuit performance by increasing propagation delay as well as reducing current drive of NMOS current drivers. Overall, an acceptable performance in terms of propagation delay and current drive was achieved in relation to the initial design choices. The resulting IC layout, bonding diagram, and pin definitions can be seen in the Appendix as Figures A.45, A.46, and Table 7, respectively.

Chapter 4

Results and Discussion

Test Setup

The test circuits as well as biasing and power supply connections necessary for testing the gate driver were assembled on a printed circuit board, shown in the Appendix as Figure A.44. The fabricated IC had 46 necessary pin connections, and was bonded to a package with 48 output pins. A custom chip mount was used that was capable of replacing the device under test (DUT) for testing of multiple chips.

Supply voltages of 0 V, 5 V, 10 V, 15 V, and 20 V were all needed to power the IC. Given the nature of the gate driver charging the IGBT gate from 0 V to 20 V, the traces connecting the 0 V and 20 V pads to power supplies were made wider in order to carry additional current, and were connected to the additional remaining 2 connection pins in order to reduce series resistance of the primary current path. The 5 V, 10 V, and 15 V supply voltages are necessary given the nature of input signals being detected and the restrictions of devices used in fabrication. In future work, voltage regulator circuits could be included in the gate driver to increase simplicity. Each supply voltage connection was connected to an array of capacitors to filter out a wide bandwidth of noise generated by the power supplies. This capacitor array was compromised of 100 μF electrolytic, 1 μF tantalum, and 0.1 μF ceramic capacitors.

24 of the 46 pins consisted of logic bits that received either 0 V or 5 V inputs. These bits consisted of either static logic bits used to determine the level of output current, or decision bits that determined feedback signals should pass through the analog

delay block or a bypass transmission gate. Neither of these types of bits are intended to be dynamic signals. As such dip switches were connected that could manually turn these bits on or off during testing.

In order to set the threshold value for the comparators, simple resistive dividers consisting of two tunable potentiometers were placed between the necessary voltage rails. This meant that for the input feedback signals determining the state of the Feedback NMOS Current Drivers, potentiometers were placed between 0 V and 5 V; and for the input feedback signals determining the state of the Feedback PMOS Current drivers, potentiometers were placed between 5 V and 10 V. By using potentiometers, the threshold voltage could be adjusted from rail to rail without replacing any components in order to test the input detection range of the comparators.

Input dynamic signals consisting of the di/dt and dv/dt signals along with the PWM signal, were input onto the board using female SMA connectors. SMD footprints for 0- Ω resistors were included between the di/dt and dv/dt signal inputs if it was desired to reduce the number of input signals and thus waveform generators required.

Bias currents required by the analog delay blocks was supplied by iterations of the circuit seen in Figure 4.25. In it, an LM317 adjustable voltage regulator is biased with a potentiometer such that the output voltage may be adjusted. This voltage is connected to the noninverting terminal of a LM741 op amp. This op amp will regulate the voltage across a variable resistor to allow adjustment of the current through a PNP-type BJT. With this configuration, the potentiometer biasing the LM317 can be used as a coarse

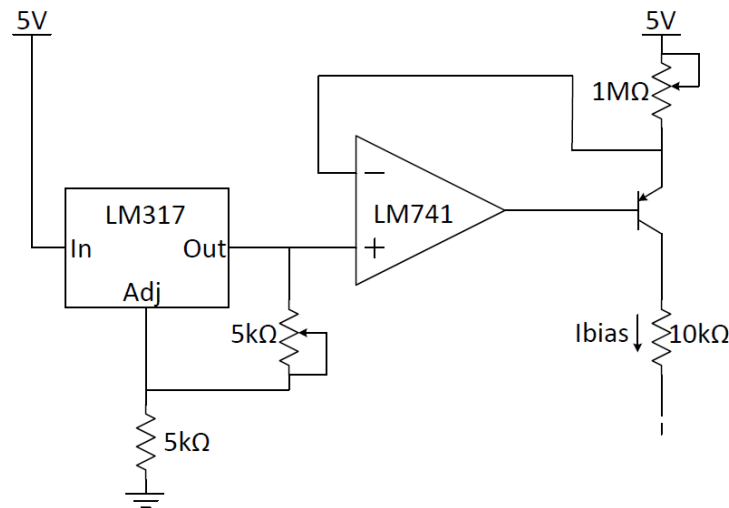


Figure 4.25 Test Board Current Source Schematic

current adjustment, while the potentiometer being driven by the LM741 and BJT transistor can function as a fine current adjustment. A 10 k Ω resistor is then placed between the collector of the BJT and the input of the IC such that the voltage across it may be measured to determine the input current. This is included rather than measuring the voltage across the potentiometer, as determining the current by measuring the potentiometer would require measurement of both its resistance and voltage, whereas with the static resistor only one measurement is necessary to determine the current. As there are 4 analog delay blocks, each with adjustable delay, there are a total of 4 current source circuits on the PCB.

The output of the IC consisted of 4 separate pins. Rather than connecting the pins together, which would be in the best interest of reducing series resistance of the output current path, they were kept separate in order to allow for measuring the current drive of each current path individually. An illustration can be seen in Figure 4.26. Each of the

output current paths may be connected onto the same node through the addition of a $0\text{-}\Omega$ resistor, represented by the switches in Figure 4.26. These resistors can be removed as needed in order to isolate certain output current paths. The final output node has through-hole connections for multiple capacitors, which can be sized as desired for different tests, as well as an extra connection that a wire may be bonded to. This wire can be used to tie the output node to an external source, such as a power supply or the gate of a transistor. This wire can also serve as a method for measuring total output current.

Current levels were measured with a Hall Effect current probe, represented by the inductor with an antenna around it (see Figure 4.26). Hence, wires were soldered onto the board in order to allow for the clipping of the sensor around each wire. Each current path would be connected to the final output node either through one of these wires intended for current measuring, or the $0\text{-}\Omega$ resistor placed on the board. The output node was connected to a power supply unit to allow for current conduction at a set output node

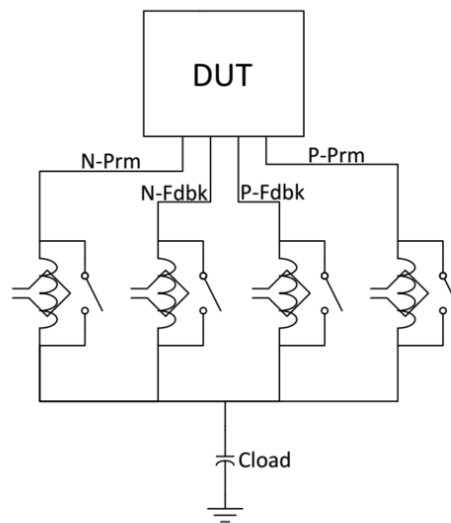


Figure 4.26 Test Board Output Configuration

voltage. As the gate driver is not intended for continuous current conduction, very short pulses are applied to the input dynamic signals to keep average DC current through the IC small and avoid overheating. The output node voltage would be placed at a high voltage when current supplied by NMOS drivers was being measured, and placed at a low voltage when current provided by PMOS drivers was being measured.

When measuring current output with the Hall Effect current probe, the delay of the input signal to output current and rise time of the current signal was not considered. This is due to the fact that both of these parameters are highly dependent on the load driven by the IGBT, as well as parasitics of the current path. The parasitic inductance created by the wire used for measuring current is directly correlated to the rise time of the output current, and thus the two were never measured simultaneously. When conducting current drive tests, measurements were made when each current output was individually connected without any others, and again when all of the current paths were connected.

When propagation delay was measured the wires intended for use with the current probe were removed to eliminate any parasitics introduced by the wire. The output node was left open, representing only a very small capacitance. This way, the voltage of the output node will change abruptly once the current drivers are activated, allowing the use of a voltage probe as opposed to a current probe with limited bandwidth.

In this configuration, because the output node is left open, two current paths of opposite type must be connected in order to change the voltage of the output node. For example, this means that when measuring the propagation delay of the Feedback PMOS signal path, the Primary NMOS drivers would also need to be activated to drain the

output node of charge when the Feedback drivers were not active. Furthermore, there must be more active Feedback drivers than active Primary drivers in order to reverse net current provided by both Feedback and Primary drivers. This configuration uses a static PWM signal and dynamic di/dt and dv/dt signals. By keeping the PWM signal static the Primary drivers of one type would stay active, and toggling the di/dt and dv/dt signals would toggle the active state of the Feedback drivers.

Once the general functionality of the IC was verified, it was then appropriate to drive a switching device. As the fabricated gate driver was capable of driving an output node up to 7.5 V for reasons discussed later, a PHP3055E MOSFET was used. This was done by soldering a wire from the output node of the PCB to the power MOSFET. This wire, however, consists of relatively large parasitic inductance that affects the rate at which the gate driver can increase or decrease current drive. While undesirable, the PCB was not designed for this purpose, and addition of this relatively large parasitic inductance was unavoidable.

Thus, the output node was tied to the gate of the power MOSFET that was configured in a double pulse switching test circuit, seen in Figure 4.27. This circuit is intended to test the switching behavior of a device driven by the fabricated IC. A conventional double pulse test allows for current to build up through an inductor by leaving the switch on. Once the desired amount of current is achieved the switch is turned off. At this point the switch may then be turned back on, emulating switching conditions seen by a power transistor. Double pulse tests are known to result in waveforms representative of ones in an actual switching mode power supply circuit [50].

In the circuit of Figure 4.27, a Shottky diode is used to reduce reverse recovery current, and a PHP3055E MOSFET is driven.

Once the double pulse switching circuit was assembled, there were two tests that were performed. First, to test the ability of the gate driver to mitigate overvoltage during turn-off, the power MOSFET is input an emulated dv/dt signal that coincided with the actual dv/dt of the device. This is seen in Figure 4.28 where the green waveform is the V_{GS} of the power MOSFET, the yellow waveform is the V_{DS} of the power MOSFET, and the violet waveform is the di/dt and dv/dt signal emulated by the waveform generator to coincide with the actual dv/dt of the MOSFET. Note that here the emulated waveform does not also emulate the dv/dt seen after the Miller Plateau. While this is unrealistic, at this point the di/dt of the transistor would no longer be feeding an active signal to the gate driver, and as both dv/dt and di/dt are required to be active in order to activate the

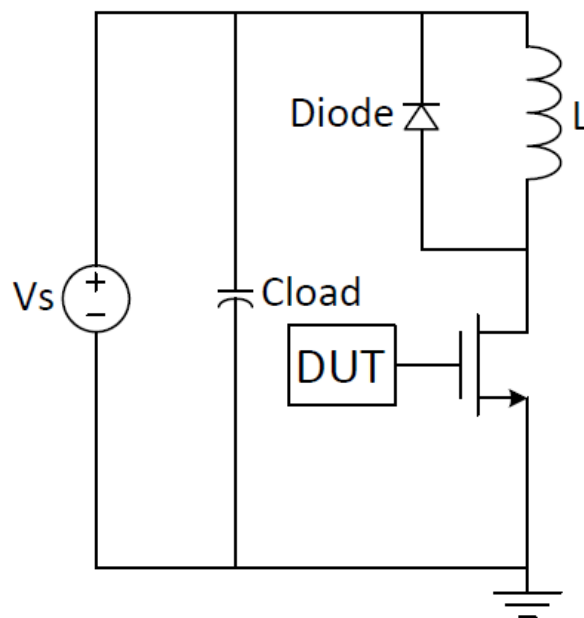


Figure 4.27 Double Pulse Switching Test Example Schematic

Feedback drivers, the Feedback drivers would not be active during this point. Thus the emulated Feedback signal is realistic in the sense that it reflects when the Feedback drivers would be fed an overall active signal.

The second type of test desired in the double pulse switching configuration is testing of the current drive capability of the gate driver. The power MOSFET used is not very representative of an actual IGBT as it possesses only 4 nF of gate capacitance. Had the gate driver been capable of driving up to 20 V, a CM200DY-12NF IGBT device was to be driven. Without the high voltage drive capability, however, the IGBT cannot be switched on, thus testing could not be performed. In order to emulate the gate capacitance of this IGBT, additional capacitance was added to the gate terminal of the power MOSFET. Given the CM200DY-12NF IGBT requires 1000 nC of charge to reach 20 V, this charge could be emulated on the MOSFET with a total capacitance of 133 nF when driving up to 7.5 V. In this configuration, the same amount of total charge is delivered by the gate driver during a switching transient, giving a representative switching time that the gate driver could produce on a real IGBT.

Current Drive

An overlay of each of the output current levels for the Primary PMOS drivers can be seen below in Figure 4.29. The output current is in response to a 20- μ s duration positive pulse of the PWM signal. Note that the current probe used had an offset of 110

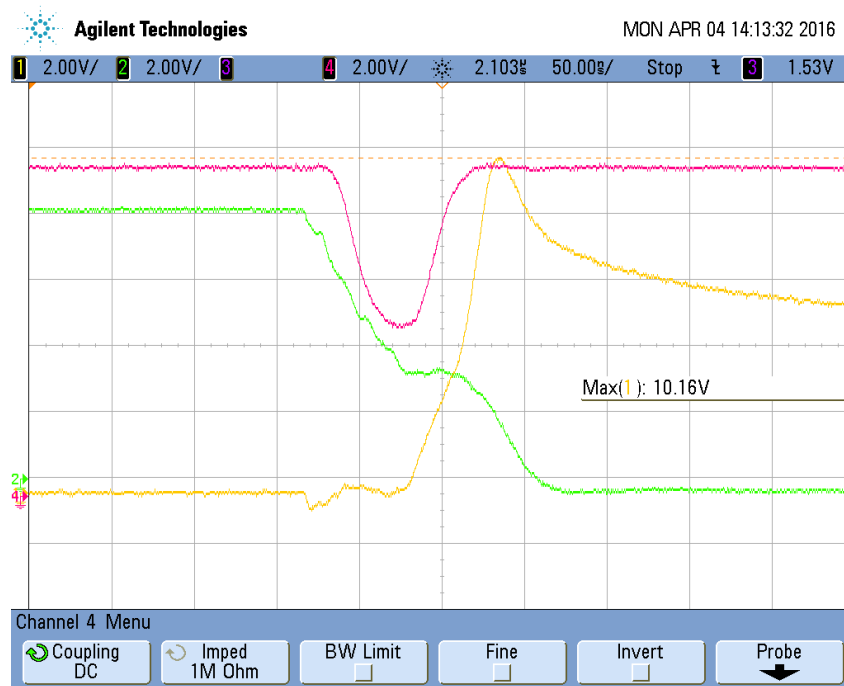


Figure 4.28 Double Pulse Testing Control Waveforms

mA, as can be seen by the fact that the current before the pulse is negative. It is observed that an output current of approximately 100 mA to 2.5 A is produced.

Discrete steps of 100 mA are observed in Figure 4.29, however, the 19th and 20th current drivers are activated simultaneously. This was a systematic issue seen in all the fabricated chip samples, and is likely the result of a fault in the digital selection block. However, other current paths did not exhibit this problem, thus it can be deduced that layout of the selection block for the Primary PMOS driver blocks, or possibly connections from the selection block to the current drivers themselves were responsible for the issue.

The numerical measured output current in each state can be seen in Appendix Table 6. Of the current driver paths, the Primary PMOS current blocks best resembled simulation results, providing an average of 100 mA per driver block enabled.

It should be noted that the PMOS current drivers were supplying current from 7.5 V, as opposed to the 20 V intended in design. The fabricated IC was capable of driving the output only to 7.5 V safely, likely due to an isolation issue in the layout. Due to the fact that the input comparators still operated between 5 V and 10 V without any breakdown issues, it is deduced that the error in layout was in either the level-up shifter or the PMOS drivers themselves. As a result, the 20 V rail was left at 7.5 V, and the 15 V rail left at 0 V.

Unlike the Primary PMOS Current Drivers, the Feedback PMOS drivers output an average of 38 mA per current driver. This average current level is not indicative of the actual performance of the driver blocks. First, the Primary PMOS drivers consisted of the same current driver cells as well as level-up shifters as the Feedback drivers. This would indicate that the design of the level-up shifter and driver cells were not the cause of the problem. Second, as the timing of the Feedback PMOS drivers behaved as expected, the comparators and level-down shifters were operating correctly. This leaves the digital selection block as a likely cause of the inconsistent current levels. As can be seen in Appendix Table 6, which depicts the current levels at each configuration of selection bits, while the average drive of each current block is 38 mA, this is a due to the fact that some drivers fail to turn on, or otherwise do not turn on completely. In the end, this can only be a result of the layout of the IC. Overall there is enough evidence to show

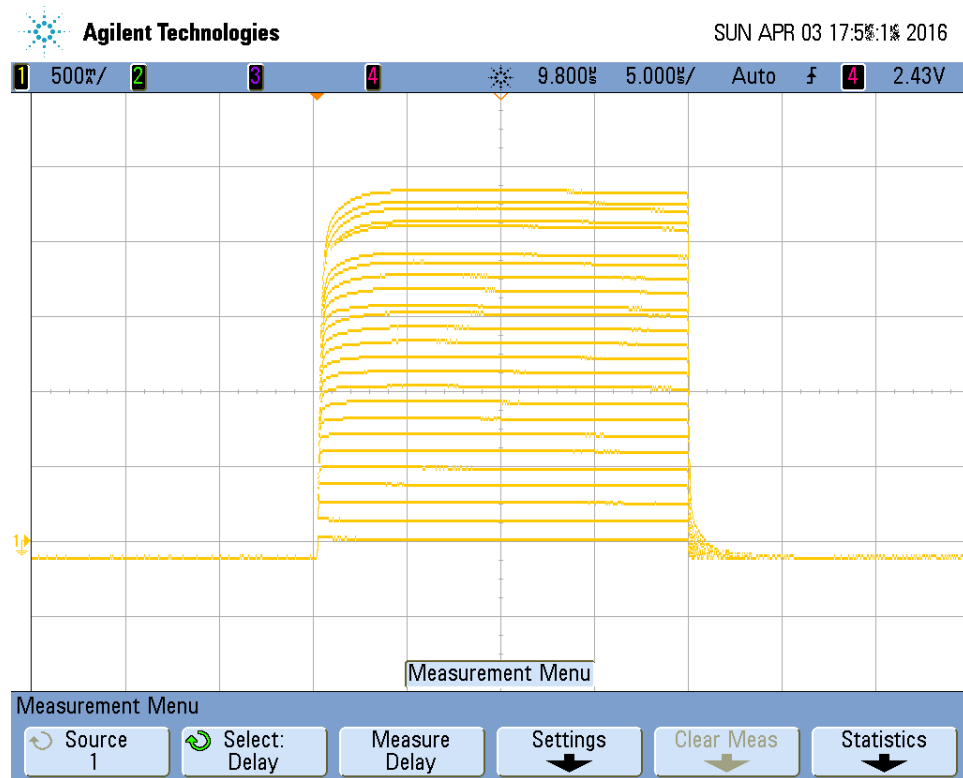


Figure 4.29 PMOS Current Drive Waveform Overlay

that the design performed as expected and is capable of scaling up to a desired current.

Primary and Feedback NMOS current driver output can be seen in Appendix Table 6. The NMOS current driver outputs were very similar to simulation results. Due to the layout issue mentioned in Chapter 3, the NMOS drivers were simulated to output 75 mA. Experimental results placed the average current output per driver for Primary NMOS at 77 mA, and 83 mA for the Feedback NMOS output drivers. Neither of the NMOS driver paths had any issues with drivers activating simultaneously such as with the PMOS current drivers. This shows that the output driver cell approach is feasible, and can be designed to create the desired steps in output current.

Finally, the output current in relation to output voltage was also measured. This was done for both PMOS and NMOS channels, by connecting the output to a voltage source and allowing current to flow in response to input pulses. As the current drivers were only driving from 0 V to 7.5 V, it was desirable to see just how much current drive was lost due to this. The results can be seen in Figure 4.30, where normalized currents are shown relative to the current drive provided at 7.5 V of V_{DS} . In the figure, measured results are seen as bold lines, and coming closer to the voltage rail that it was being pulled to. In particular, the PMOS current drive appears to be more linear than simulation results, with no knee, indicating that it may have not reached maximum current drive. This could mean that the PMOS current drivers could actually provide more than 100 mA of current per driver at voltages above 7.5V. However, as the PMOS drivers did output the simulated amount of current drive, it is difficult to be certain.

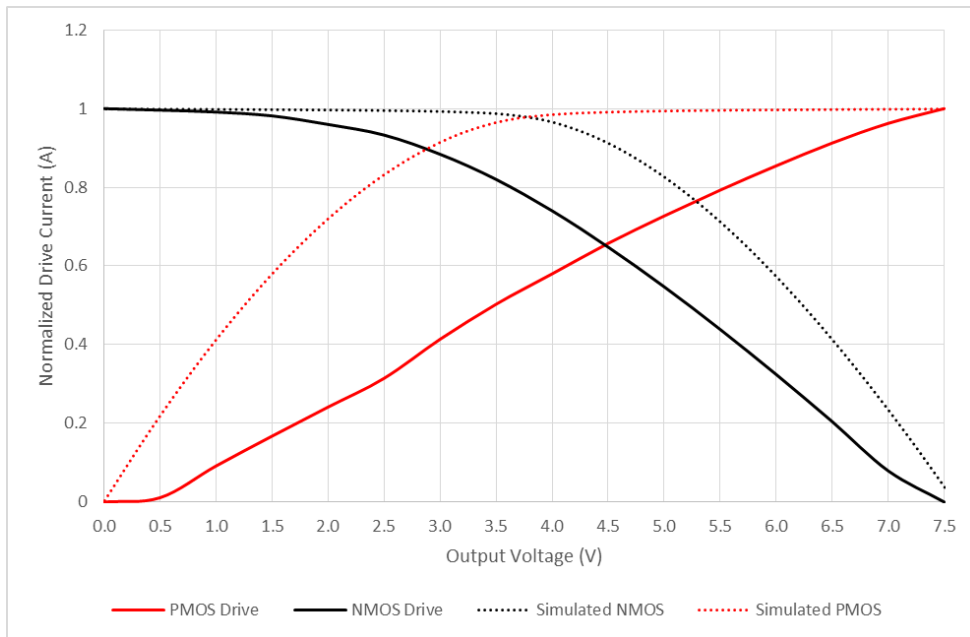


Figure 4.30 Output Driver Current vs Output Voltage

Propagation Delay

For the propagation delay tests it was desirable to observe the time between the rising edge of an input voltage signal, e.g. PWM for the Primary driver blocks and di/dt or dv/dt for the Feedback driver blocks, as well as the range and adjustability of the delay introduced by the analog delay block. While testing the delay of the Primary PMOS and NMOS current drivers, given the test setup discussed in the previous section, both the Primary NMOS and PMOS drivers needed to be active to charge and discharge the output node. As such the output node would not build charge until both the PMOS drivers had deactivated, and the NMOS drivers had activated. Thus, the larger delay of the two Primary drivers was observed, as this would be the delay seen in any typical application.

An example waveform observing propagation delay can be seen in Figure 4.31. This figure shows the input PWM signal in violet, and the output node voltage in yellow. In the test setup discussed in the previous section for propagation delay it was mentioned that the output node was left open. As can be seen in Figure 4.31, the output node voltage rises very quickly given the small load capacitance. This allows for accurate measurement of the propagation delay, observed as 18.4 ns. The falling edge waveform, which can be seen in the Appendix as Figure A.43, yields a propagation delay of 20.2 ns. Additional waveform captures measuring delay can be seen in the Appendix as Figure A.39-A.42. Final results and comparison to simulation values are provided in Table 5.

These delays, while larger than simulated results, are still relatively low compared to other gate drivers on the market. As gate drivers produced by the same company that fabricated the IC yield a minimum propagation delay of 12 ns, it is reasonable to

conclude that optimization of the design could yield even smaller propagation delays. It should also be noted that it is unknown at what rise time and fall time input PWM signals are applied to test gate drivers on the market. As can be seen in Figure 4.31, a rise time of approximately 20 ns is applied. Input signal rise time can impact propagation delay, and thus may be artificially inflating the observed propagation delay. Simulations were performed with a rise time of 1 ns, and produced delays of approximately 12 ns.

Given experimental results will typically fall behind simulation results, it is not surprising to see an increase in propagation delay, however an increase by a multiple of 1.5 places the test setup in question. As no waveform generators with faster than 20 ns of rise time were available, these propagation delays were the best observed.

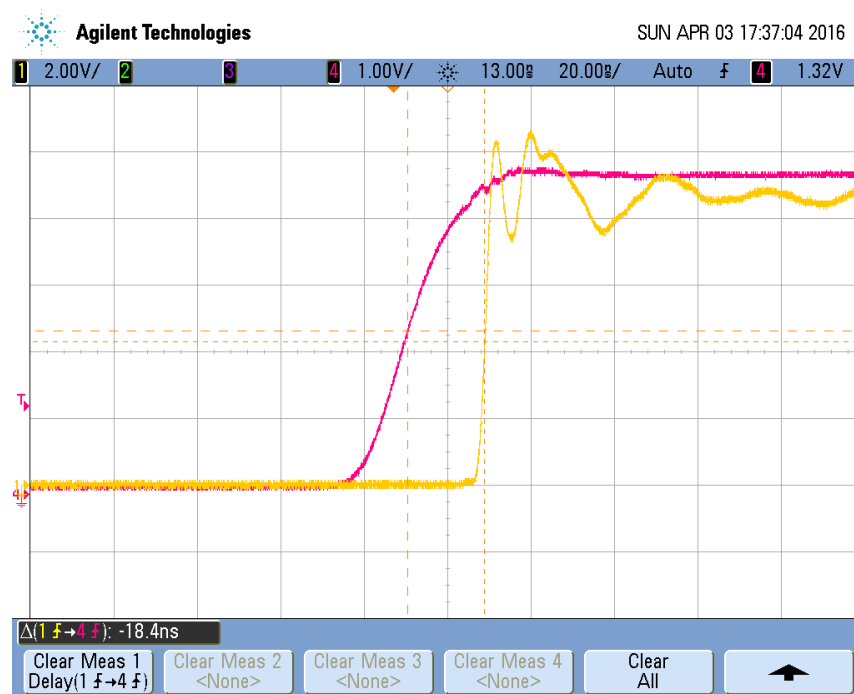


Figure 4.31 Experimental Primary Current Driver Propagation Delay Waveform

Table 5. Chip Level Simulation Propagation Delays and Active States

	<i>Simulated (ns)</i>	<i>Experimental (ns)</i>	<i>Percent Increase (%)</i>
Primary rising edge	10.27	18.4	79
Primary falling edge	11.38	20.2	76
Feedback PMOS activation	25.65	40	56
Feedback PMOS deactivation	23.63	44	86
Feedback NMOS deactivation	7.3	26	356
Feedback NMOS activation	5.78	23	397

Regarding mismatch between propagation delay of rising and falling waveforms, simulations showed that the falling edge had a 10.8% greater delay than the rising edge. Experimental results yielded a 9.7% increase in delay from rising to falling edge. These results are very similar, and suggest that the increase in delay was uniform between rising and falling edges. This also means that care must be taken in simulation to match rising and falling edge delay to the greatest degree possible. While in simulations the absolute difference in delays was only 1.1 ns, the inflation of overall propagation delay increased this disparity to 1.8 ns.

Keep in mind that this is the propagation delay of the Primary gate driver portion of the IC, and as such can be compared to other conventional gate drivers. The Feedback gate driver signal path, however, requires additional circuitry and cannot be compared to most gate drivers found on the market today.

Given the adjustable delay of the Feedback driver signal path, measurement included testing of the analog delay block. The overlay of waveforms seen in Figure 4.38 demonstrates the variable delay of the PMOS Feedback signal path. The violet waveform

is the input di/dt and dv/dt signal tied together, and the yellow waveform is the voltage of the open output node. The minimum delay observed occurs when the analog delay block is bypassed with a transmission gate, and is seen as the furthest left rising edge yellow waveform. During testing the delay was tuned in 50-ns intervals and the input current recorded up to 500 ns of delay, then the step size was increased to 100 ns intervals. This test is repeated 4 times total, for the activation and deactivation times for both Feedback PMOS and Feedback NMOS signal paths.

Signal paths retained similar increases between simulated and experimental results in rising and falling edge propagation delays, however each signal path yielded different levels of increase, as can be seen in Table 5. This is mostly noted in the delay of the Feedback NMOS signal path, which increased propagation delay by a factor of

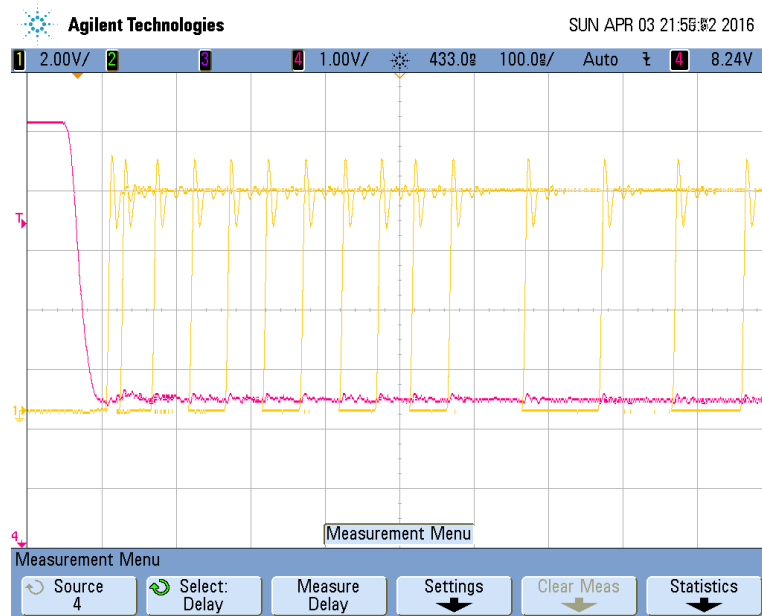


Figure 4.32 Experimental Adjustable Delay of Feedback NMOS Current Drivers

nearly 4. This may be a result of the fact that simulated propagation delay of this signal path was very small to begin with, and the resultant delay of 23 ns and 26 ns are not large absolute values, but are large relative to the compared simulation results. However, the Feedback NMOS signal path simulation indicated less propagation delay than the Primary drivers, and in experimental results yielded a higher propagation delay. This means that blocks only present in the Feedback signal path were contributing more delay than expected. Given the topology of the NMOS signal path this means the input comparators are the only possible source of the additional delay, as the same digital selection blocks were used as in the Primary drivers.

As expected, the Feedback PMOS signal path exhibited the largest signal delay. This is likely a cause of the level-down shifter that had to be implemented after the input comparators. Comparing the delay between the Feedback PMOS and NMOS drivers, and considering the fact that the Feedback PMOS signal path has an additional level-down and level-up shifters, it can be stipulated that the level shifters contribute approximately 20 ns of delay time. Compared to the simulated 11 ns of delay time from both level shifter, this would mean an increase of 81%. This increase is very similar to increases in delays seen throughout the chip, further supporting this stipulation.

If you subtract the delay of the Primary drivers from the PMOS signal path, you would ostensibly get the propagation delay of the remaining blocks, the comparator and level-down shifter. Given the fact that the level-down shifter is stipulated to have only increased delay by 81% to 6 ns, this would mean that the comparator will have contributed approximately 15 ns of delay, while having simulated a propagation delay of

only 2 ns. This hypothesis is congruous with the fact that the Feedback NMOS signal path had unexpectedly high propagation delay, with the comparator as the main suspected source of this delay. While impossible to prove without probing inside of the chip itself, it is highly likely that the comparator contributed significantly higher propagation delay than simulations predicted.

Characterization of the analog delay block included testing the propagation delay at different input bias currents, and comparing with simulation results. Given the fact that there are no testing pins at nodes before and after the analog delay block, total delay of the signal path was measured and considered. Given the desired range of delay times was 1 μ s or less, delay was tuned and then input current measured across the sense resistor described in the previous section. Measuring the current through the sense resistor would have an affect on the delay of the circuit, as differences in current as small as 1 μ A could significantly impact the induced delay of the delay block. Testing results are compiled in Figure 4.33 and 4.34. In Figure 4.33, the propagation delay of the PMOS Feedback signal path is varied, and in Figure 4.34 the propagation delay of the NMOS Feedback signal path is varied. Both waveforms have the rising edge, or delay time for activation as the black curve, and falling edge or delay time for deactivation as the red curve. For both the PMOS and NMOS signal paths the correct range and characteristics were achieved, with predictable increase in total propagation delay. Measurements were recorded up to 900 ns, as can be seen in each curve. Propagation delays of above 400 ns required less than 10 μ A of current, and thus precise control of the delay in this range, while possible, would require precise control over a small amount of input current.

Delays in the 10's of ns to 100's of ns, however, can be easily tuned with between 10 and 100 μA . It may then be desirable to slightly increase the target range of the delay block by shrinking the current starved inverters. Delay was very stable, however, changing this range would be purely a tradeoff in quiescent current and difficulty in biasing with small currents. The simple test circuit used in the previous circuit had no problem keeping a stable current in these ranges, and could reliably produce delays up to 4 μs , though a delay this large would not typically be needed. Overall the analog delay block performed very similar to simulations, and achieved all of its design goals. The only improvements on design would be purely for ease of application.

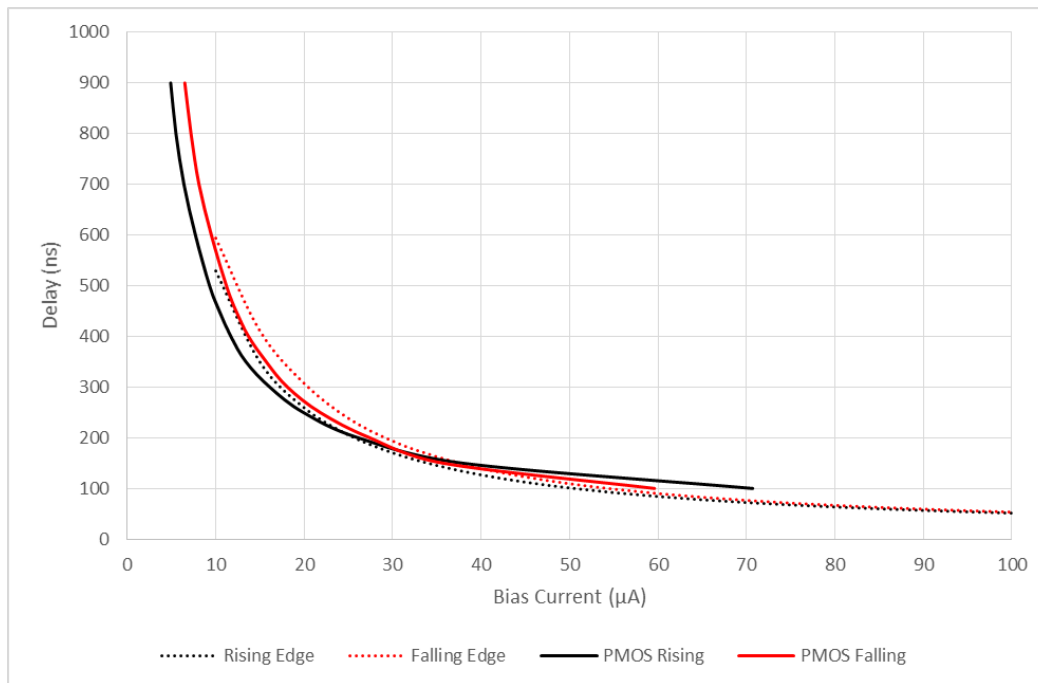


Figure 4.33 Measured Delay Range of Feedback PMOS Current Drivers

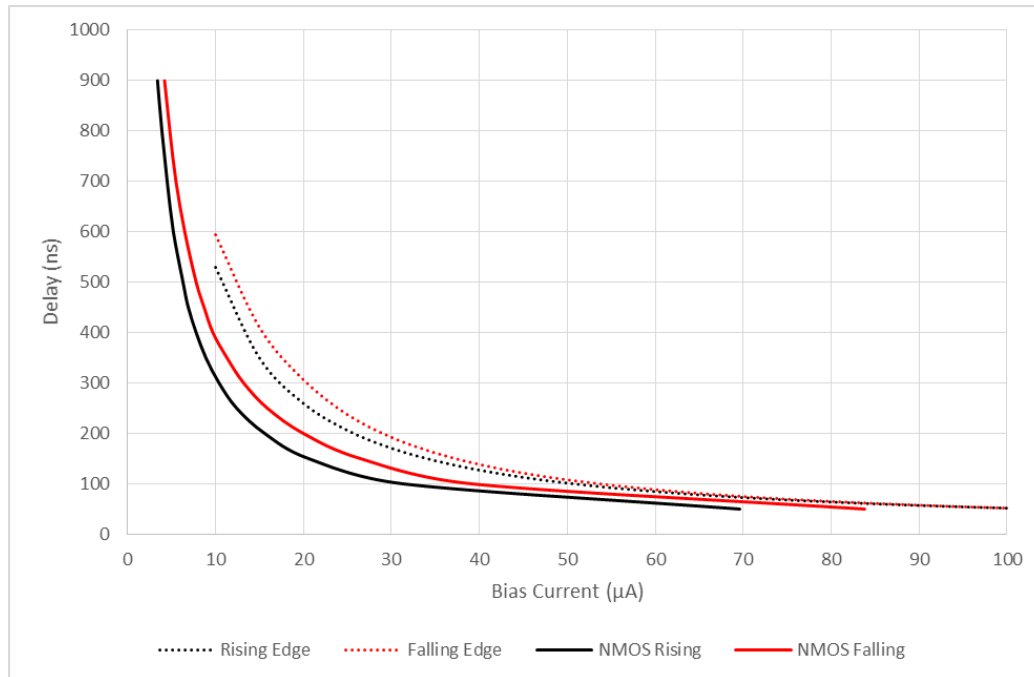


Figure 4.34 Measured Delay Range of Feedback NMOS Current Drivers

Double Pulse Testing

The resulting waveforms from the first test setup designed to evaluate protection functionality can be seen in Figure 4.35. Please refer to Figure 4.28 from the first section of this chapter in regards to stimuli used for this test setup. In Figure 4.35, three separate waveform captures are presented. Here the green waveform is the gate-to-source voltage of the MOSFET, and the yellow waveform is the drain-to-source voltage. In the top oscilloscope screenshot, the turn-off transients of the MOSFET are observed where only 5 Primary gate drivers are active. In the second, 6 Feedback PMOS drivers are activated, and in conjunction with the emulated feedback signal, cause for current to be placed back



Figure 4.35 Experimental Voltage Compensation Waveforms

into the gate of the power MOSFET near the end of the Miller plateau. This current injection results in a reduction of the maximum drain-to-source voltage from 10.16 V observed in the first waveform to 9.16 V. In the third waveform capture, 8 Feedback PMOS drivers are activated, further reducing the maximum voltage seen to 8.79 V. These waveforms together demonstrate the ability of the gate driver to vary gate current in response to feedback currents and effectively reduce voltage overshoot seen during turn-off. It should be noted, however, that this is performed on a very small gate capacitance of 4 nF presented by a MOSFET, and not the larger gate capacitance presented by an IGBT.

While still in this test configuration with no additional capacitance on the gate of the power MOSFET, control of the Feedback current in the time domain could be demonstrated. This can be seen in Figure 4.36. In it, the top violet waveform is the emulated di/dt waveform, the second purple waveform is the input PWM signal, third is the gate voltage, and fourth is the gate current. Between part (a) and (b), the analog delay is increased, and it can be seen that the voltage spike of the gate voltage is moved forward in the time domain. With this functionality present, it is possible to tune the exact time during which the gate current is reduced or reversed, in order to provide optimal protection from overvoltage during turn-off.

Moving onto the second configuration, 133 nF of capacitance was added to the gate of the power MOSFET in order to represent the total gate charge necessary to turn on an example IGBT module. The MOSFET is then turned on and off in a double pulse test, seen in Figure 4.37. The resulting waveform has a rise time and fall time of less

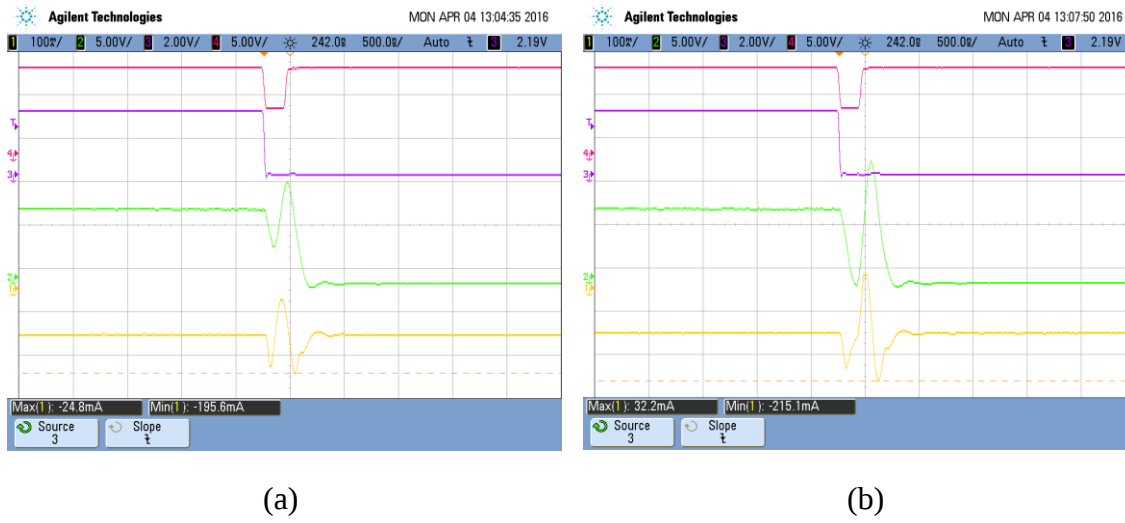


Figure 4.36 Experimental Adjustable Delay Waveforms

than 1 μ s, which is a typical switching time for an IGBT. This shows that had the gate driver been capable of driving up to 20 V, an IGBT likely could have been successfully switched at a reasonable speed. It is also worth noting that because the gate driver only operated to 7.5 V, the output driver devices leave saturation sooner, providing less than maximum current drive for a larger portion of the switching transient.

The proposed IC was fabricated and tested. By designing and fabricating a printed circuit board with an IC socket, multiple copies of the proposed IC were tested for functionality. Test setup was designed to best reflect the performance of the IC. The tests performed on the IC samples showed that the design was capable of sinking and sourcing the expected amount of current, however was only capable of doing so up to 7.5V and not the intended 20V due to an isolation issue in the layout phase. Propagation delay was higher than simulated, but still relatively small compared to comparable IC gate drivers on the market. Double Pulse Switching tests were performed to simulate driving an



Figure 4.37 Experimental Switching Waveforms driving 133nF Gate Capacitance

IGBT in a switching configuration, and feedback signals were emulated to show that the proposed IC was capable of dynamically adjusting drive current and compensating voltage and current overshoot.

Chapter 5

Conclusions and Future Work

In conclusion, the proposed gate driver is a viable alternative to large, area consuming active gate driver circuits. The tested IC was capable of performing feed-forward protection strategies in a timescale that is common for most switch mode power supply circuits. Variable gate current was achieved, resulting in a total of four separate output current levels that could be alternated between quickly using input dynamic signals. These output current levels could be adjusted as intended. Problems with the tested IC such as inability to drive to high voltages and low current drive from one signal path are likely related, and easily remediated through layout.

The proposed gate driver does not provide as much current as gate drivers on the market today, but this is due to the area of the chip being used for dynamic current adjustment. If all the output current drivers were configured to function as a conventional gate driver, and the layout of the IC optimized, the gate driver could have easily achieved and even exceeded current drive provided by other gate drivers on the market. The sacrifice of this gate current for protection functionality is congruous with tradeoffs seen throughout gate drivers on the market, especially given the low propagation delay of the IC.

As such, there is much that can be done given the results of this thesis. Were a new chip to be fabricated, many improvements could be made. Of course the high voltage issue should be fixed in order to properly drive an IGBT, which would ideally remedy the PMOS Feedback current drive issue. As the comparator is suspected to be an

unexpectedly large source of propagation delay, its design could be reinvestigated. Different level shifter topologies could be investigated to further reduce propagation delay. Layout of NMOS current drivers can be improved to achieve the desired 100 mA increments. Large amounts of area was left open on the IC as the number of drivers was limited by the number of selection bits, so output current could easily be increased by increasing the current step size.

Aside from improvements on the chosen topology of the gate driver, different topologies could be considered. Given it is uncommon to want to briefly turn the IGBT back off during turn-on transients, less Feedback NMOS drivers could be included, only including enough to slow the turn-on switching transient a reasonable amount, leaving this area open for additional Primary NMOS drivers.

Also, given the Primary current drivers that make up a conventional gate driver will most often be used at maximum output current, larger steps in output current can be designed. Taking larger steps in output current would provide massive decrease in total area dedicated to output drivers, as well as require fewer input pins. This is because even though the output devices grow in size, less level shifter and buffers driving the output devices are required, and complexity of the digital selection logic is reduced.

Testing configurations of future gate driver ICs could be designed to minimize loop inductance to the gate of an IGBT, and this IGBT could be included in an entire SMPS circuit. From here the loop could be closed by detecting the di/dt and dv/dt of the IGBT and the gate driver could be tested in a closed-loop circuit.

Overall, as a proof-of concept the tested IC shows that the chosen topology is functionally viable, and with layout area optimization as well as topology tuning, could produce a gate driver with impressive protection capabilities, current drive, and speed.

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Appendix

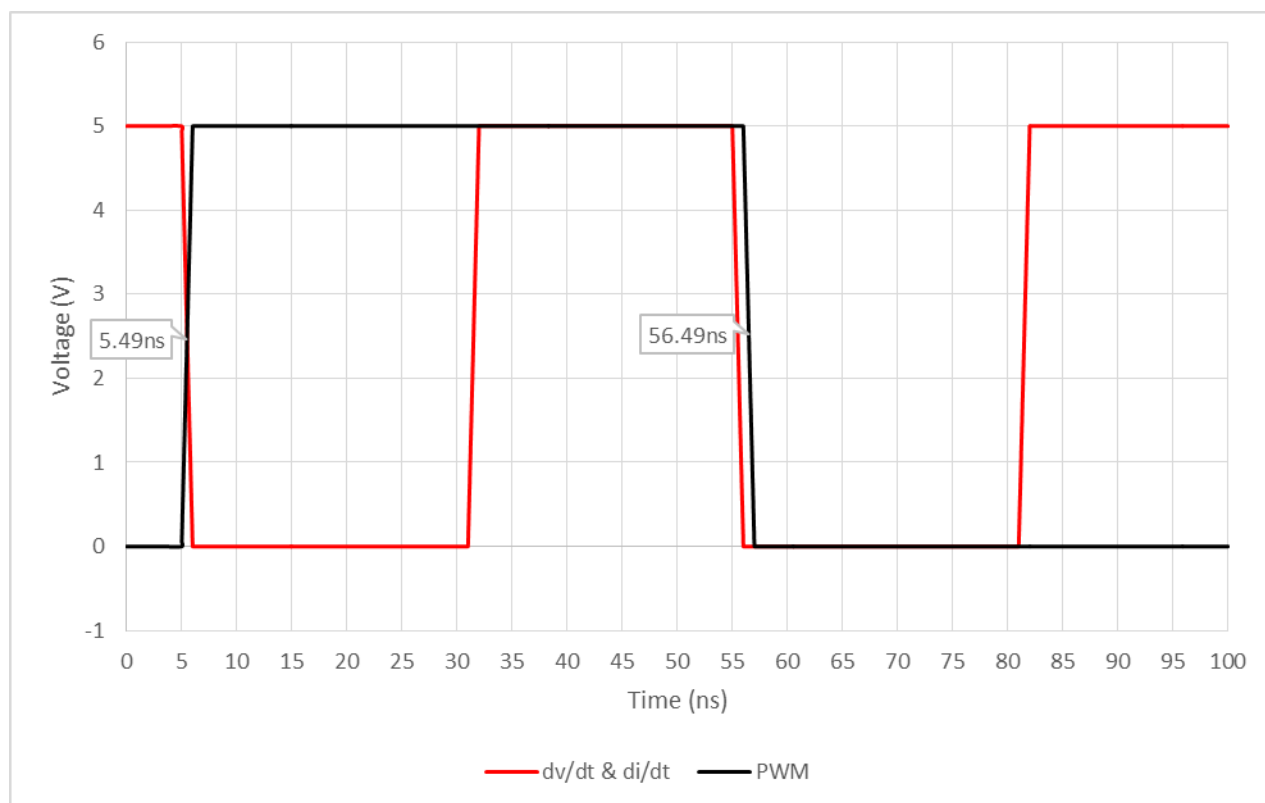


Figure A.38 Chip Level Simulation Input Dynamic Signals

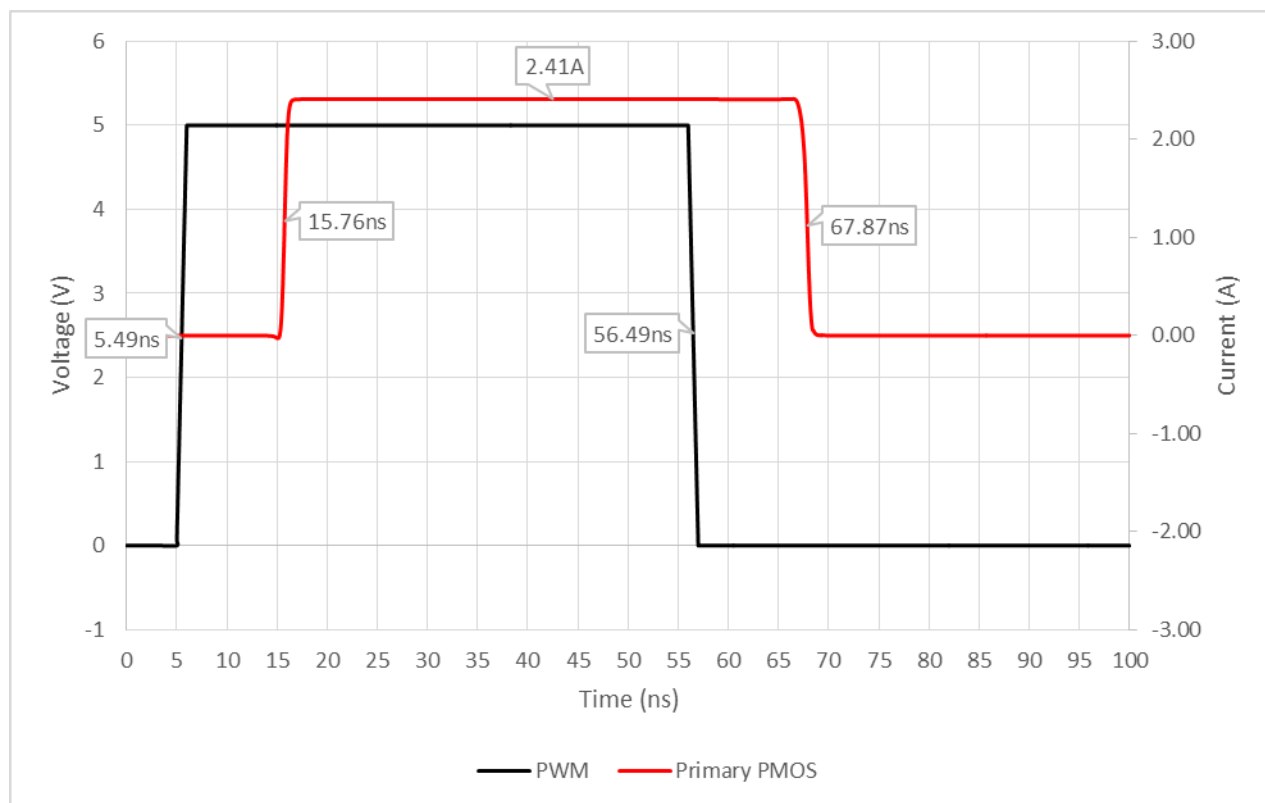


Figure A.39 Chip Level Simulation Primary PMOS Propagation Delay

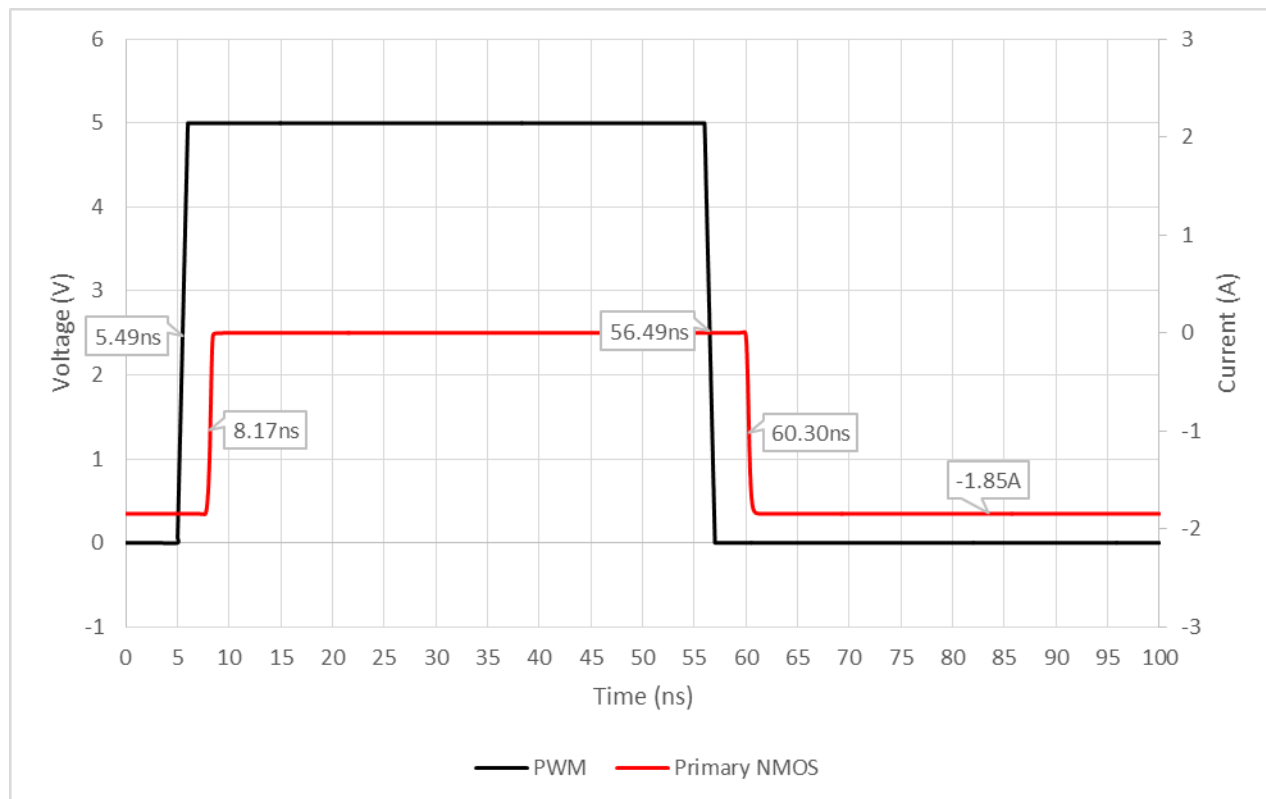


Figure A.40 Chip Level Simulation Primary NMOS Propagation Delay

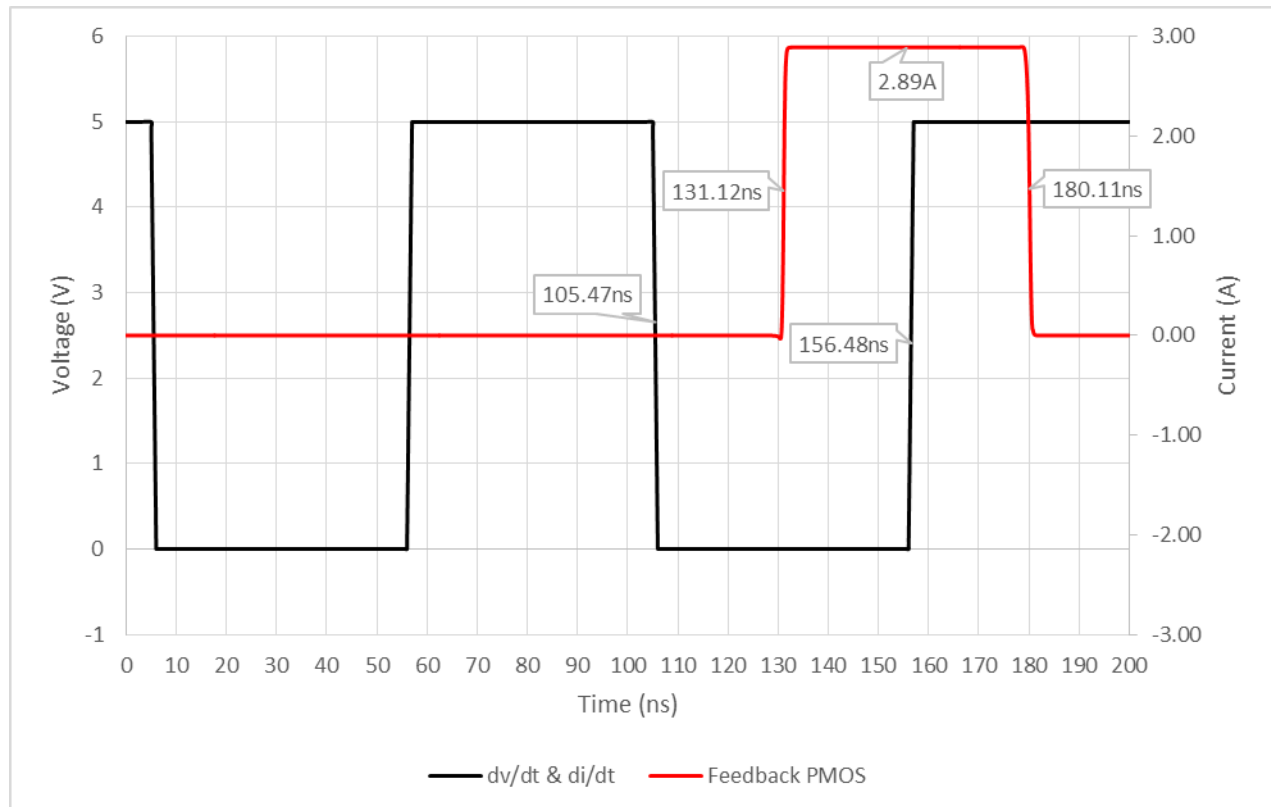


Figure A.41 Chip Level Simulation Feedback PMOS Propagation Delay

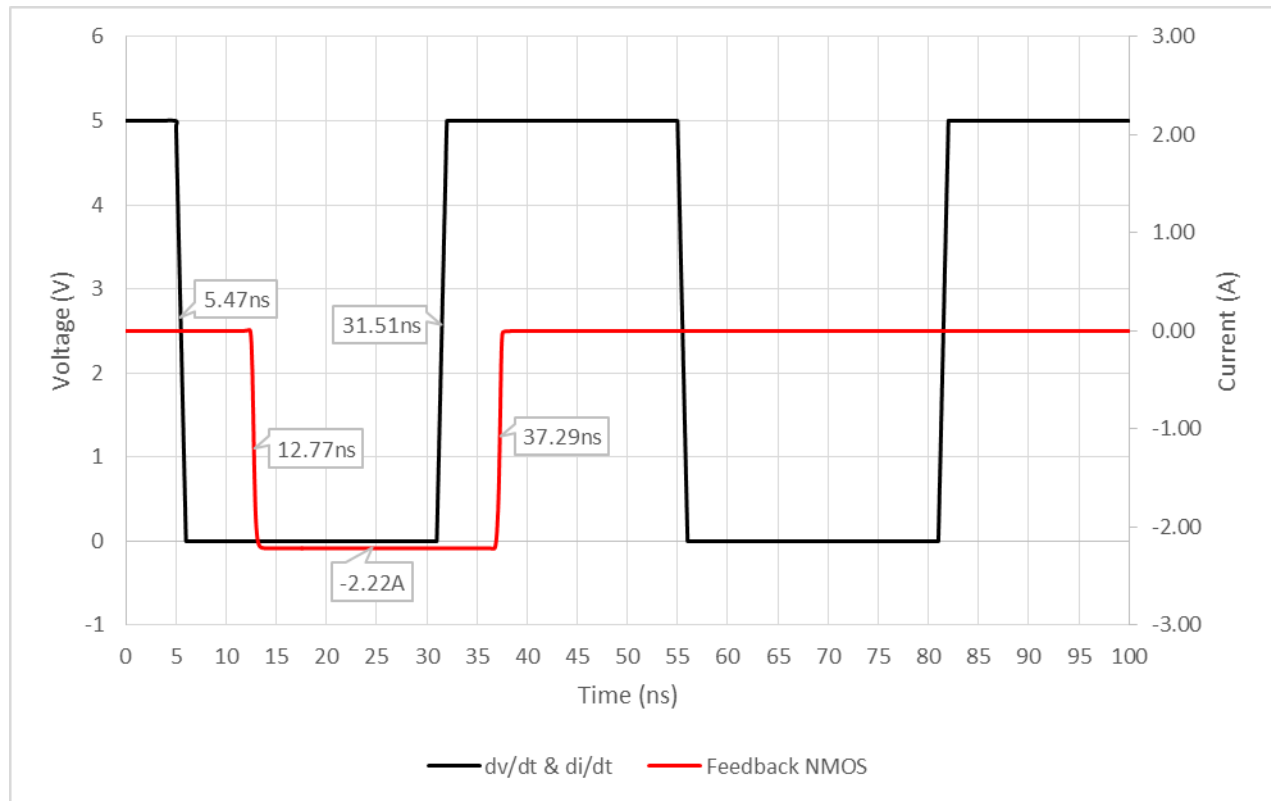


Figure A.42 Chip Level Simulation Feedback NMOS Propagation Delay

Table 6. Experimental Current Driver Metrics

Active Gate Drivers	Primary NMOS Current (A)	Feedback NMOS Current (A)	Primary PMOS Current (A)	Feedback PMOS Current (A)
1	.094	0.157	0.071	0.05
2	.201	0.261	0.192	0.17
3	0.298	0.35	0.314	0.23
4	0.39	0.449	0.426	0.23
5	0.479	0.541	0.484	0.33
6	0.567	0.633	0.542	0.39
7	0.656	0.719	0.651	0.47
8	0.735	0.807	0.753	0.53
9	0.816	0.896	0.858	0.58
10	0.895	0.981	0.951	0.61
11	0.974	1.066	1.048	0.67
12	1.054	1.149	1.14	0.75
13	1.127	1.23	1.228	0.78
14	1.1295	1.313	1.33	0.81
15	1.2815	1.394	1.49	0.89
16	1.3644	1.473	1.59	0.92
17	1.43	1.553	1.71	0.94
18	1.496	1.65	1.78	0.97
19	1.56	1.73	1.96	0.98
20	1.62	1.81	2.01	1.03
21	1.684	1.89	2.12	1.05
22	1.747	1.97	2.19	1.08
23	1.806	2.04	2.36	1.09
24	1.86	2.11	2.42	1.11
25	1.92	2.19	2.48	1.13
26	-	2.25	-	1.14
27	-	2.36	-	1.16
28	-	2.45	-	1.16
29	-	2.49	-	1.16
30	-	2.5	-	1.16

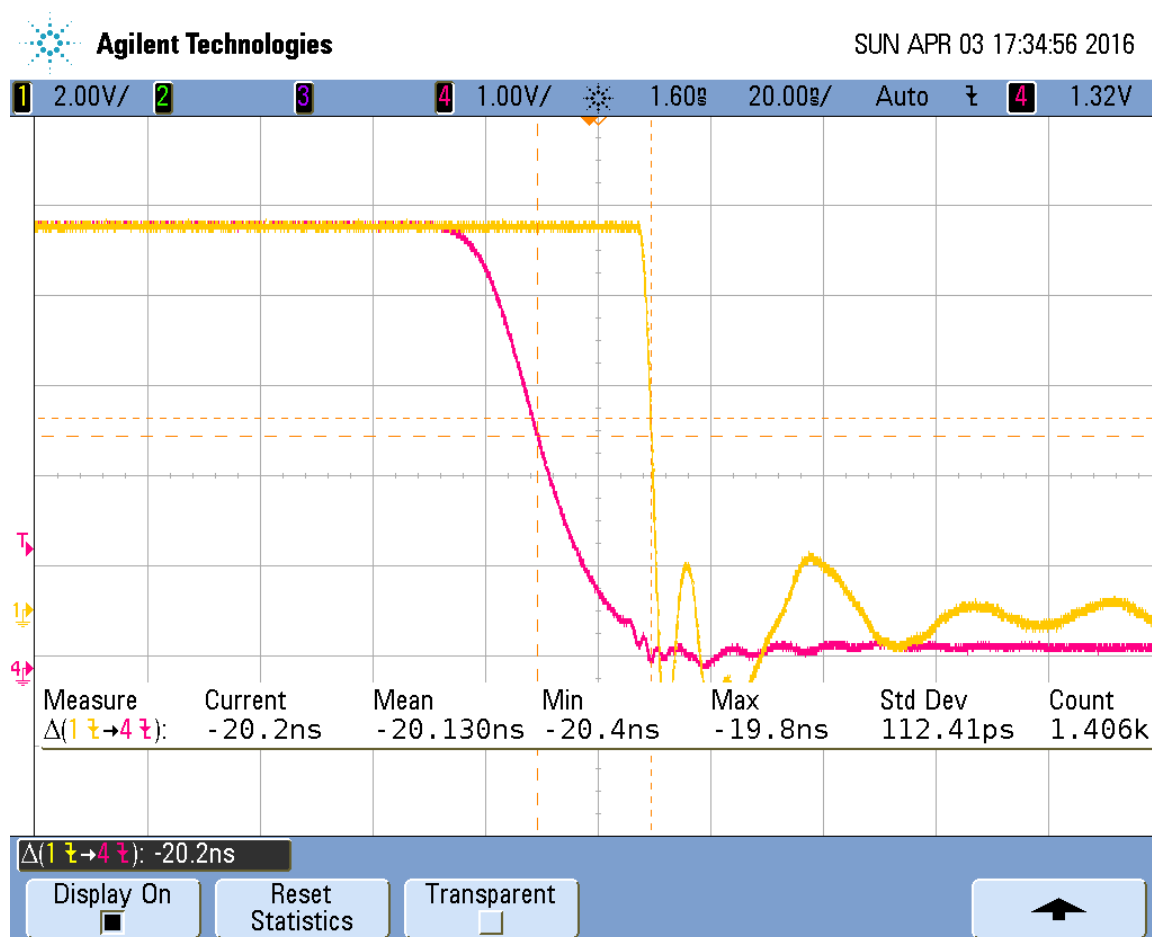


Figure A.43 Experimental Falling PWM edge Waveform

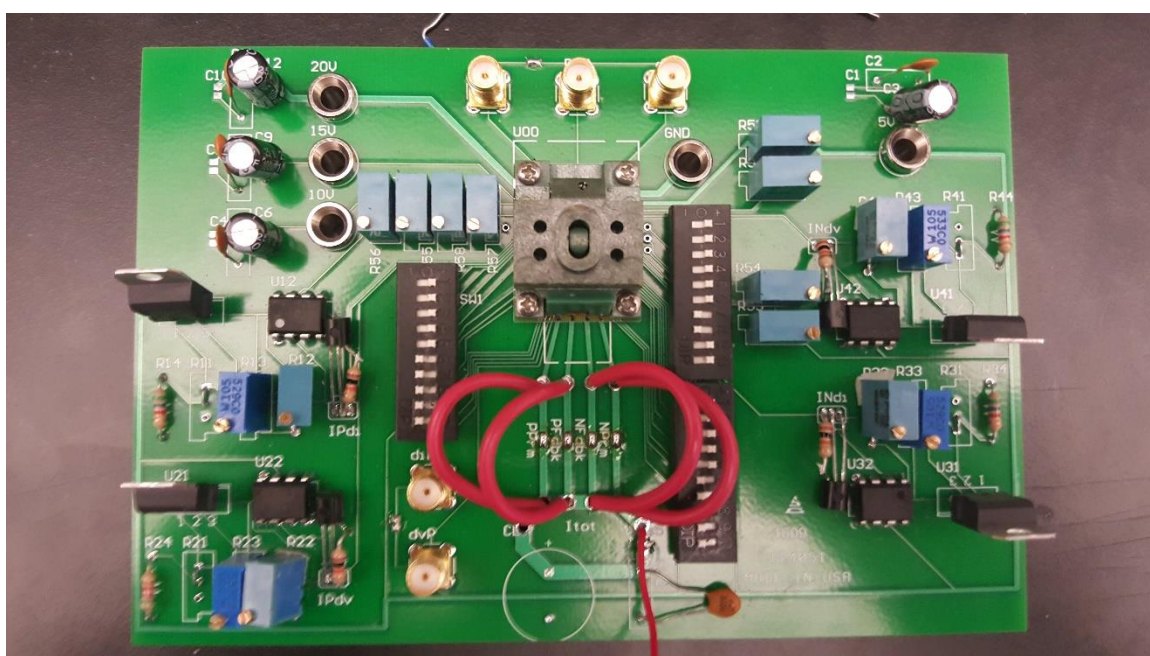


Figure A.44 Testing PCB

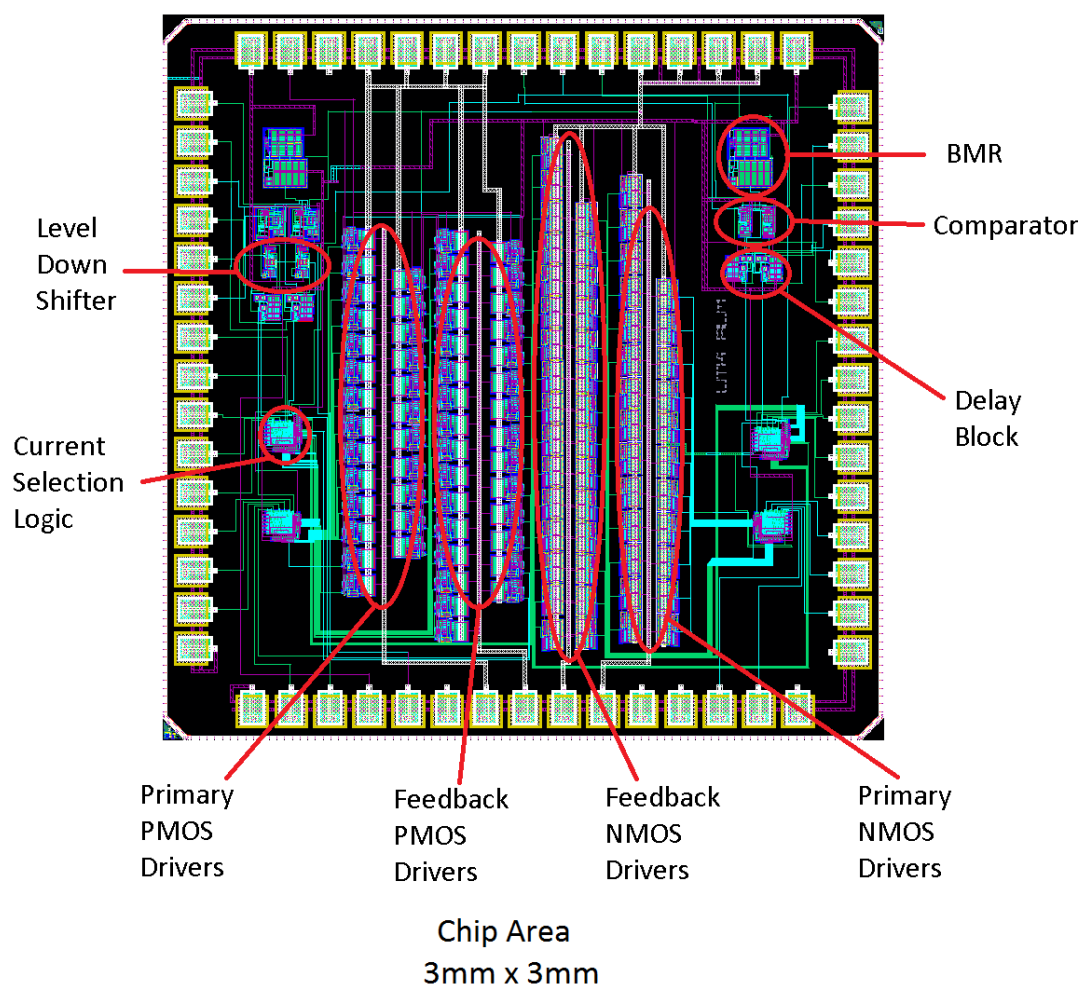


Figure A.45 IC Layout

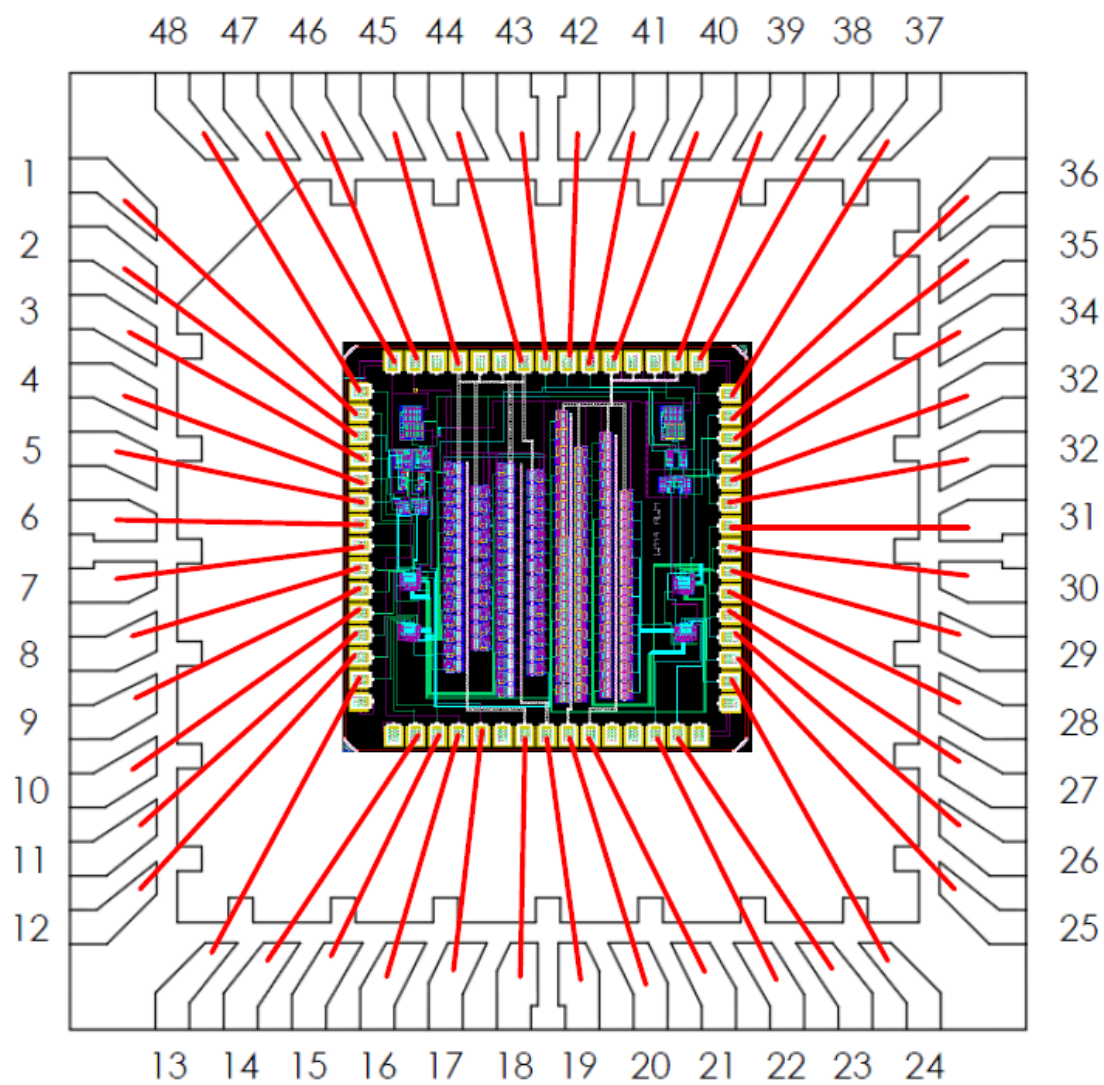


Figure A.46 IC Bonding Diagram and Pinout

Table 7. IC Pinout Definitions

<i>Pin Number</i>	<i>Pin Function</i>	<i>Pin Number</i>	<i>Pin Function</i>
1	PMOS di/dt delay T-gate state	32	NMOS di/dt Comparator Threshold
2	PMOS di/dt delay current input	33	NMOS di/dt delay current input
3	PMOS dv/dt delay current input	34	NMOS di/dt T-gate state
4	PMOS dv/dt delay T-gate state	35	NMOS dv/dt T-gate state
5	PMOS dv/dt Comparator Threshold	36	NMOS dv/dt delay current input
6	PMOS Feedback Selection Bit 4	37	NMOS dv/dt Comparator Threshold
7	PMOS Feedback Selection Bit 3	38	5 V Supply Voltage
8	PMOS Feedback Selection Bit 2	39	Ground Supply Voltage
9	PMOS Feedback Selection Bit 1	40	Ground Supply Voltage
10	PMOS Feedback Selection Bit 0	41	dv/dt input signal
11	PMOS Primary Selection Bit 4	42	PWM input signal
12	PMOS Primary Selection Bit 3	43	di/dt input signal
13	PMOS Primary Selection Bit 2	44	20 V Supply Voltage
14	PMOS Primary Selection Bit 1	45	20 V Supply Voltage
15	PMOS Primary Selection Bit 0	46	15 V Supply Voltage
16	PMOS input di/dt signal	47	10 V Supply Voltage
17	PMOS input dv/dt signal	48	PMOS di/dt Comparator Threshold
18	PMOS Primary Output		
19	PMOS Feedback Output		
20	NMOS Feedback Output		
21	NMOS Primary Output		
22	NMOS Primary Selection Bit 0		
23	NMOS Primary Selection Bit 1		
24	NMOS Primary Selection Bit 2		
25	NMOS Primary Selection Bit 3		
26	NMOS Primary Selection Bit 4		
27	NMOS Feedback Selection Bit 4		
28	NMOS Feedback Selection Bit 3		
29	NMOS Feedback Selection Bit 2		
30	NMOS Feedback Selection Bit 1		
31	NMOS Feedback Selection Bit 0		

Vita

Alex McHale was born in Painesville Ohio in 1991, and moved to Tennessee before the age of 5. After attending high school in Thompsons Station, TN, he moved to Knoxville to pursue his undergraduate degree in Electrical Engineering at The University of Tennessee, Knoxville. He then decided to continue his education and pursue a Masters of Science in Electrical Engineering.