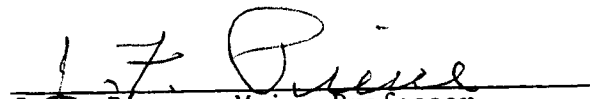
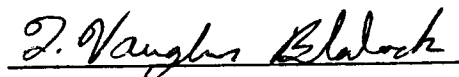
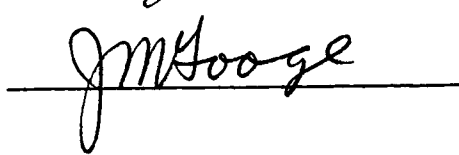


To the Graduate Council:

I am submitting herewith a thesis written by Bruce Wayne Coyne entitled "A Hybridized Charge-Sensitive Preamplifier with Improved Timing Resolution." I recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.


J. F. Pierce, Major Professor

We have read this thesis and
recommend its acceptance:

Accepted for the Council:


Vice Chancellor
Graduate Studies and Research

A HYBRIDIZED CHARGE-SENSITIVE PREAMPLIFIER WITH
IMPROVED TIMING RESOLUTION

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Bruce Wayne Coyne

August 1980

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ABSTRACT

The charge liberated by the detection of a nuclear event contains timing and energy information. Several systems have been proposed to obtain both timing and energy data. However, the signal processing usually degrades either the energy or timing data. Four preamplifier configurations used to process the charge signal and provide both timing and energy data are analyzed theoretically. The results indicate that one configuration in particular does not degrade either signal if certain risetime and noise criteria are satisfied.

A preamplifier design using the optimum configuration is presented. Certain timing section characteristics are verified using a computer simulation program. The final design was constructed using hybrid construction techniques. Experimental results are presented.

The preamplifier design satisfies the initial design goals. However, to verify the choice of a circuit configuration and the final design, the preamplifier timing performance was evaluated using a laser diode pulser together with various silicon surface barrier detectors. The timing performance of the new preamplifier is compared to that obtained from a commercial fast risetime compensated preamplifier. The new preamplifier energy resolution is equivalent to that of a conventional preamplifier and the timing resolution is typically 50% better.

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CHAPTER 1

INTRODUCTION

Background of Problem

The detection of nuclear radiation with a silicon surface barrier detector depends upon the liberation of charge (electron-hole pairs) as the nuclear particle is absorbed by or passes through the detector. The amount of charge liberated is dependent upon the energy absorbed by the detector material. The energy absorbed by the detector is dependent upon the detector material and the detector size (thickness). The mean particle energy required per electron-hole pair produced is 3.6eV for silicon. The detector thickness is related to the amount of charge liberated only if the detector thickness is insufficient to completely stop the nuclear particle. The charge liberated is collected as the holes and electrons are swept to the appropriately biased detector contacts by the electric field. For silicon surface barrier detectors the maximum mobility is 10^7 cm/sec for an electric field strength of 1000V/cm or greater.¹ Due to the high carrier mobility the charge collection time of the detector can be well below one nanosecond(ns), approaching 100psec and below for very thin detectors. (For a thorough treatment of detection of nuclear events see Knoll (1979),¹ Nicholson (1974),² and Bertolin and Coche (1968).³

The charge liberated by a nuclear event is usually collected using a charge-sensitive preamplifier. The preamplifier produces a voltage pulse with a peak amplitude proportional to the amount of charge

liberated in the detector. This voltage pulse amplitude is therefore directly related to the energy absorbed and contains the necessary information to perform energy spectroscopy.

Time spectroscopy involves the measurement of the time relationship between two events. The time information is contained in the leading edge of the charge collection waveform, or the risetime of the detector signal. To avoid degrading the timing information, the leading edge must be processed with a minimum of risetime degradation. With silicon surface barrier detectors having charge collection times of $\ln$ sec and less, the timing resolution can easily be limited by the preamplifier if sufficiently fast risetimes are not possible. Several methods have been used to obtain both energy and timing signals from the same preamplifier, but usually at the expense of degrading at least one signal. Sherman and Roddick have used two different methods to obtain both timing and energy data, parallel preamplifiers⁴ and charge loop error signal.⁵ The charge loop output signal has been used to obtain timing information by designing a very fast risetime preamplifier as reported by Karlovac and Mayhugh.⁶ In addition, Quaranto, Martini and Detoviani have used a series arrangement with a current preamplifier which requires a special detector mount.⁷ A review paper concerning the detector pulse shape and timing, containing a very extensive bibliography has been published.⁸ The question of the method to use in deriving the timing signal versus detector pulse shape has been considered by Gross⁹ and will not be addressed in this thesis.

Scope of Thesis

The objective of this thesis is to optimize the design of a preamplifier that provides both energy and time information. Four basic methods for obtaining energy and timing data are discussed in Chapter 2. The energy and timing resolution are analyzed in some detail for all four methods. The third chapter of this thesis covers the design of a preamplifier using the basic configuration which yields the optimum energy and timing resolution as predicted in Chapter 2. The fourth chapter includes a PCAP analysis which was used in the design of the circuit presented in Chapter 3 and also to investigate the effects of certain stray parameters. The actual performance of the circuit design developed in Chapter 3 is included in Chapter 5. The timing performance of the new circuit design was measured using a laser diode pulser¹⁰ and compared with that obtained for a fast risetime compensated charge loop. The last chapter contains suggestions for further work and areas where improved performance might be obtained.

CHAPTER 2

CONFIGURATION ANALYSIS

Introduction

The timing signal can be obtained by a variety of methods. However, only three do not require the use of a special detector mount. These three methods are as follows:

1. Use of the energy signal for the timing signal as shown in Figure 2.1.
2. Parallel preamps, one for the timing data and one for the energy data as shown in Figure 2.2.
3. Pick-off of timing signal at some point in a conventional charge sensitive loop prior to any integrating stages as shown in Figure 2.3.

Single Output System

The system that uses the energy output signal for the timing data is the easiest to implement and is also the least expensive because no additional components are required. However, this approach has performance limitations not present in other approaches. A block diagram of such a system is shown in Figure 2.4. All noise sources are included and the amplifier is assumed to have a single-pole response. As indicated in Figure 2.4 the amplifier is a charge sensitive type. Assuming that all the charge is collected by the feedback capacitor (C_F), the output voltage (V_O) is

$$V_O = Q/C_F \quad (2.1)$$

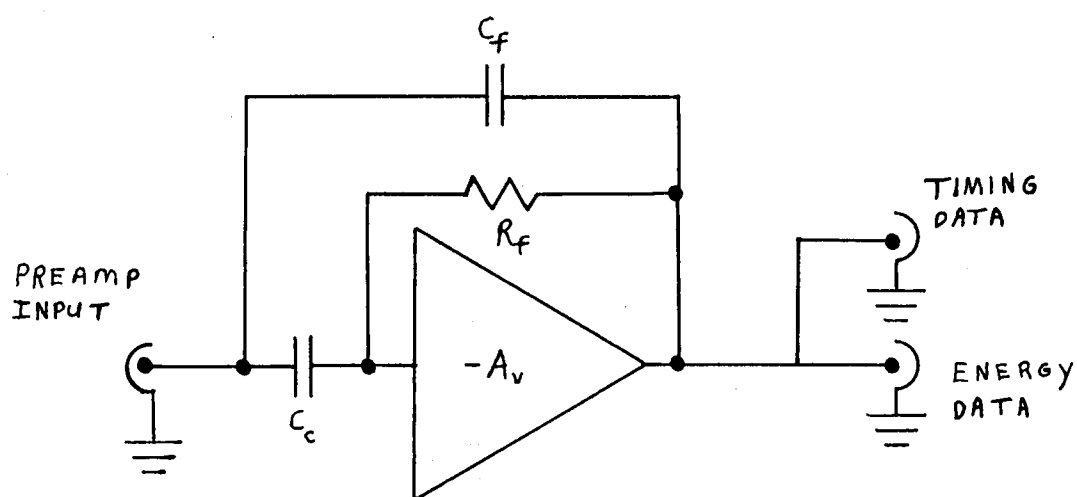


Figure 2.1. Charge preamplifier output used for timing.

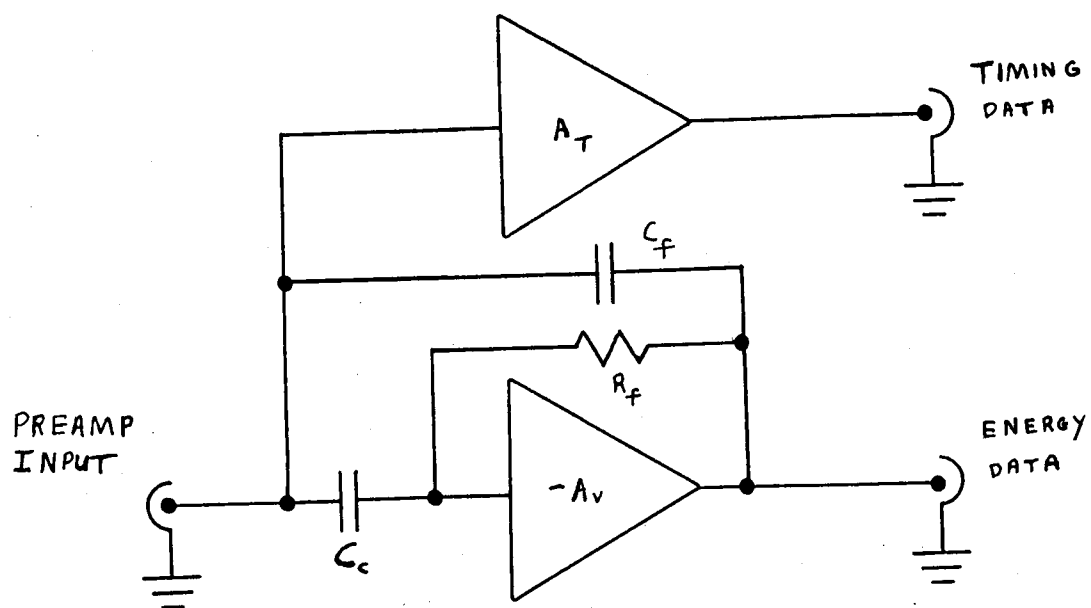


Figure 2.2. Parallel pick-off.

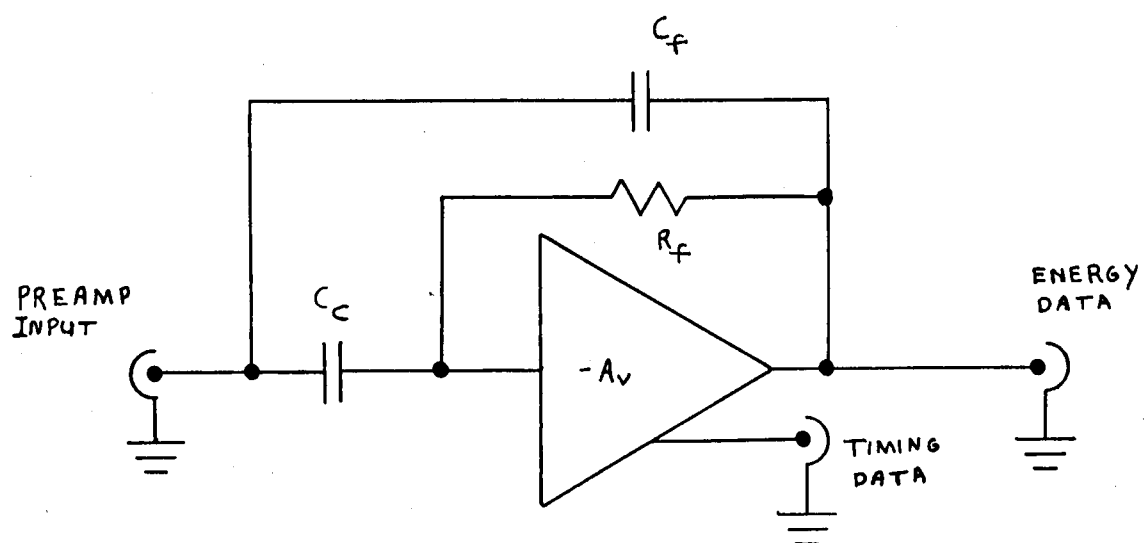


Figure 2.3. Drain pick-off.

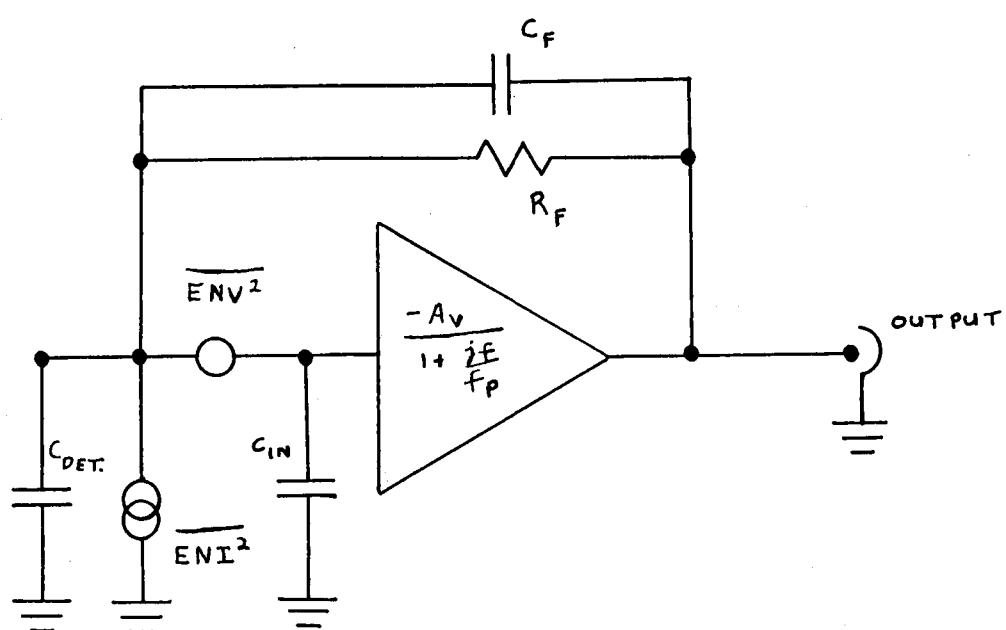


Figure 2.4. Single output system.

The amount of charge liberated in the detector depends upon the energy absorbed by the detector and the detector material. For silicon, the charge per million electron volts (MeV) of energy is

$$Q = \frac{(E)(e)}{w} \quad (2.2)$$

Where E is the energy in MeV, e is the charge per electron and w is the work function. For silicon, the charge is 4.45×10^{-14} C/per MeV of absorbed energy. The corresponding output voltage is 44.5mV/pF/MeV as shown in Equation (2.1). Therefore, the output voltage does not depend upon either the detector capacitance or the input capacitance. If the amplifier is assumed to have the gain characteristics shown in Figure 2.4, the loop transmission (T) is

$$T = -A_v \left(\frac{C_F}{C_F + C_D + C_{IN}} \right) \frac{1}{1 + jf/f_p} \quad (2.3)$$

where C_{IN} is the capacitance of the input FET plus the stray capacitance. The gain bandwidth product (GBP) of this amplifier is

$$GBP = \frac{F_p A_v C_f}{C_f + C_{IN}} \quad (2.4)$$

For the case in which C_{IN} is equal to zero, the GBP is

$$GBP = F_p A_v \quad (2.5)$$

The high frequency minus 3dB point can be determined by the relationship

$$F_{hi} = \frac{GBP}{Gain} \quad (2.6)$$

From this relationship, the high frequency -3dB point is

$$F_{hi} = \frac{F_p A C_f}{C_F + C_D + C_{IN}} \quad (2.7)$$

When a charge-sensitive preamplifier is used with a surface barrier detector, usually

$$C_{IN} \gg C_F \quad (2.8)$$

and

$$C_D \gg C_{IN} \quad (2.9)$$

Therefore, Equation (2.7) can be reduced to

$$F_{hi} = \frac{F_p A C_f}{C_D} \quad (2.10)$$

This equation indicates that the high frequency -3dB limit is inversely proportional to detector capacitance. The risetime τ_r is

$$\tau_r = \frac{0.35}{F_{hi}} \quad (2.11)$$

and is, therefore, directly proportional to detector capacitance.

The most important specification for a charge sensitive amplifier is its noise performance. For the timing output the noise performance is most commonly given as an rms noise voltage at the output for a given

bandwidth. For the charge sensitive output, the noise performance is most commonly given in terms of energy resolution (Noise Line Width, N.L.W.) at full width maximum (FWHM)² in electron volts (eV). The noise sources can be reduced to two separate and uncorrelated sources referred to the input and are shown as a series noise voltage ($\overline{ENV^2}$) and a parallel noise current ($\overline{ENI^2}$). The series noise voltage includes FET series noise, second stage noise contributions, detector contact resistance noise, and any other significant noise sources in the amplifier. The parallel noise current includes detector leakage noise current, FET gate leakage noise current, parallel noise due to R_f and parallel noise due to the detector load resistor. The circuit shown in Figure 2.5 includes a noise model for a charge sensitive amplifier and a surface barrier detector where $\overline{i_{R_f}^2}$ is the noise current due to R_f , $\overline{i_{R_D}^2}$ is the noise current due to the detector load resistor, $\overline{i_D^2}$ is the shot noise contribution due to the detector leakage current, $\overline{i_g^2}$ is the noise current due to FET gate leakage, and $\overline{e_A^2}$ is the series noise voltage identified as $\overline{ENV^2}$ in Figure 2.4. Figure 2.5 can be reduced to Figure 2.4 if

$$\overline{ENV^2} = \overline{e_A^2} \quad (2.12)$$

and

$$\overline{ENI^2} = 2e(I_D + I_g) + \frac{4KT}{R_D || R_f} + \frac{KT\omega^2 C_{gs}^2}{g_m} \quad (2.13)$$

for the FET noise model as shown in Figure 2.6. The output noise

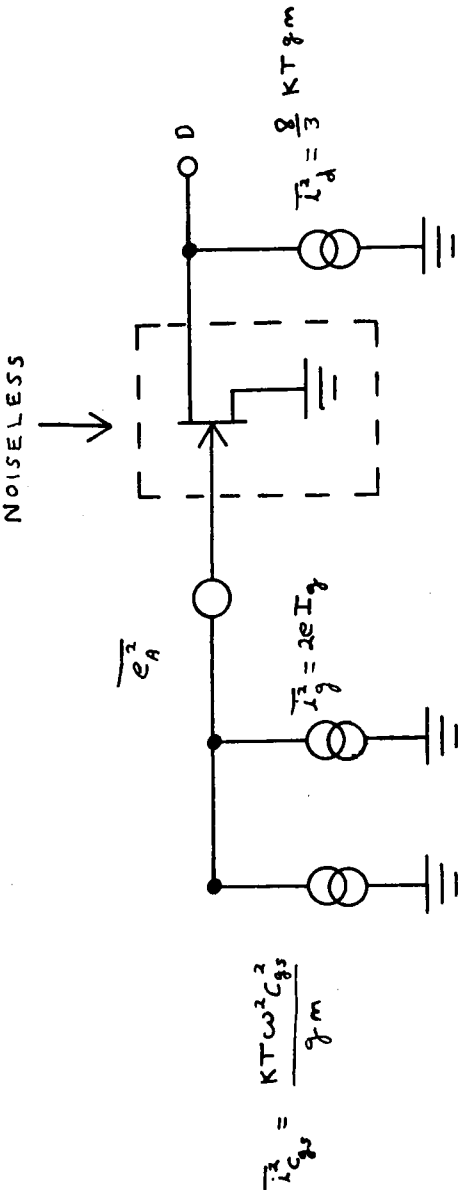


Figure 2.6. Noise model for FET.

voltage due to the input noise voltage $(\overline{E_o^2} | \overline{ENV^2})$ is

$$\overline{E_o^2} | \overline{ENV^2} = \overline{ENV^2} \left(\frac{C_f + C_D}{C_f} \right)^2 \quad (2.14)$$

The output noise voltage due to the input parallel noise current is

$$\overline{E_o^2} | \overline{ENI^2} = \overline{ENI^2} | jX_{C_F} |^2 \quad (2.15)$$

where X_{CF} is the impedance of the feedback element. The total output noise voltage, $\overline{E_o^2}$, is

$$\overline{E_o^2} = \overline{ENV^2} \left(\frac{C_F + C_D}{C_F} \right)^2 + \overline{ENI^2} | jX_{C_F} |^2 \quad (2.16)$$

The output noise voltage in Equation (2.16) will be used to evaluate the timing performance of a preamplifier in a later section of this chapter.

The noise performance of a preamplifier used for energy spectroscopy is usually given in electron volts (eV) at FWHM (N.L.W.). The resolution of a charge sensitive amplifier is affected by several factors, including some further along in the signal processing chain. A thorough treatment of resolution in spectroscopy systems is contained in Chapter 3, 4 and 5 of Nuclear Electronics.² The total equivalent input noise voltage $(\overline{e_n^2})$ is

$$\overline{e_n^2} = \left[\overline{ENV^2} + \overline{ENI^2} | jX_{C_T} |^2 \right] \quad (2.17)$$

where jX_{C_T} is

$$jX_{CT} = \frac{1}{2\pi f(C_D + C_{IN} + C_F)} \quad (2.18)$$

The equivalent noise voltage at the FET input is

$$\overline{V^2} = \left[\overline{e_A^2} + \frac{KTC^2_{gs}}{gmC_T^2} + \frac{1}{\omega^2 C_T^2} \left((2eI_g + 2eI_D) + \frac{4KT}{R_F} + \frac{4KT}{R_D} \right) \right] \quad (2.19)$$

and C_T is

$$C_T = C_{IN} + C_F + C_D \quad (2.20)$$

To conform to the convention used by Nicholson. Equation (2.19) can be rewritten as

$$\overline{dV^2} = \left[\overline{e_A^2} + \frac{KT}{gm} \frac{C_{gs}^2}{C_T^2} + \frac{1}{\omega^2 C_T^2} \left((2eI_g + 2eI_D) + \frac{4KT}{R_F} + \frac{4KT}{R_D} \right) \right] df \quad (2.21)$$

This equation is in the form of

$$\overline{dV^2} = \left(a^2 + \frac{b^2}{\omega^2} \right) \quad (2.22)$$

The first term of Equation (2.22) is not a function of frequency, while the second term is inversely proportional to frequency. The series noise term can be written as

$$a^2 = \left[\overline{e_A^2} + \frac{KT}{gm} \frac{C_{gs}^2}{C_T^2} \right] \quad (2.23)$$

and the parallel noise term as

$$b^2 = \frac{1}{2\pi C_T^2} \left(2e(I_g + I_D) + 4KT \left(\frac{1}{R_F} + \frac{1}{R_D} \right) \right) \quad (2.24)$$

The equivalent noise charge (ENC), using ideal pulse shaping, can be written as

$$(\text{ENC})_\infty = [C_T^2 (2\pi ab)]^{1/2} \quad (2.25)$$

The optimum shaping time (τ_{OPT}) is

$$\tau_{\text{OPT}} = a/b \quad (2.26)$$

The result obtained using realizable pulse shaping is always larger than that given by Equation (2.25) due to the difficulty in obtaining an infinite cusp pulse shape. The various pulse shapes are related to the infinite cusp shape by a figure of merit F . Using the figure of merit and the shaping time (τ) the ENC can be found by

$$\text{ENC} = \left[(\text{ENC})_\infty^2 \frac{F^2}{2} \left(\frac{\tau_{\text{OPT}}}{\tau} + \frac{\tau}{\tau_{\text{OPT}}} \right) \right]^{1/2} \quad (2.27)$$

The ENC is expressed in terms of coulombs, and the resolution is typically given in eV. The ENC can be converted to eV by

$$N.L.W. (FWHM) = \frac{(ENC) (2.36) (w)}{e} , \quad (2.28)$$

where w is the work function (3.6eV per electron-hole pair for silicon), e is the charge per electron and 2.36 is used to convert the measurement to FWHM. For silicon, Equation (2.28) can be written as

$$N.L.W. (FWHM) = (5.3 \times 10^{19}) (ENC) \text{ eV} . \quad (2.29)$$

The timing resolution of a system can be approximated by

$$\sigma_T = \frac{\sigma_v}{dv/dt} \quad (2.30)$$

where σ_T is the standard time resolution σ_v is the root mean square noise voltage at the output of the amplifier and dv/dt is the slope of the signal at the output point. Using Equations (2.16) and (2.11), the time resolution can be approximated as

$$\sigma_T = \frac{\left[\left[\frac{1}{ENV^2} \left(\frac{C_F + C_D}{C_F} \right)^2 \right]_{f_L}^{f_H} + \int_{f_L}^{f_H} \frac{1}{ENI^2} |jX_{C_F}|^2 df \right]^{1/2}}{\frac{0.8 V_O f_H}{0.35}} \quad (2.31)$$

This equation and Equation (2.28) provide the time and energy resolution for the system shown in Figure 2.1, p. 5. These are two equations that

will be used to develop a comparison of the three configurations in a later section of this chapter.

Parallel Timing Pick-Off

The parallel pick-off as shown in Figure 2.2, p. 6, has been used extensively before^{4, 11}, and provides more flexibility in the design of the fast stage and the charge sensitive loop. The parallel pick-off configuration has certain disadvantages as will be shown in this section. A model containing the basic noise sources for the parallel pick-off including those in the timing section is shown in Figure 2.7. The effect of the noise sources associated with the fast section must be taken into account when analyzing the noise of the charge loop. The induced noise current ($\overline{I_1^2} | \overline{ENI_F^2}$) due to the gate leakage current of the fast stage is

$$\overline{I_1^2} | \overline{ENI_F^2} = \frac{\overline{ENI_F^2} | Z_{DET}|^2}{(|Z_{DET}| + |Z_{C2}| + |Z_L|)^2} \quad (2.32)$$

where Z_{DET} is the impedance of the detector, Z_{C2} is the impedance of C_2 , and Z_L is the impedance of the inductor. The induced noise current due to the induced gate noise voltage by the FET channel capacitance of the fast stage ($\overline{I_1^2} | \overline{ENV_F^2}$) is

$$\overline{I_1^2} | \overline{ENV_F^2} = \frac{\overline{ENV_F^2} | Z_{DET}|^2}{[|Z_{IN}| (|Z_{DET}| + |Z_L| + |Z_{C2}|) + |Z_{C1}| (|Z_{DET}| + |Z_L| + |Z_{C2}|) + |Z_D| (|Z_L| + |Z_{C2}|)]^2} \quad (2.33)$$

where Z_{IN} is the input impedance of the fast stage. The induced noise current due to $R_D(\overline{I_1^2}|_{R_D})$ is

$$\overline{I_1^2}|_{R_D} = \frac{(Z_L R_D)^2 \frac{4KT}{R_D}}{[R_D|Z_L| + |Z_{C2}|(|Z_L| + R_D) + |Z_D|(|Z_L| + |R_D|)]^2} \quad (2.34)$$

The squared value of the equivalent input noise current into the charge sensitive amplifier is the sum of the contributions due to the fast stage and the contribution from the sources included in the analysis of the conventional charge loop, or

$$\overline{ENI_Q^2} = \overline{ENI_S^2} + \overline{I_1^2}|_{ENV_F^2} + \overline{I_1^2}|_{R_D} + \overline{I_1^2}|_{ENI_F^2} \quad (2.35)$$

The output noise voltage due to the fast stage contribution and the charge loop parallel noise source is

$$\overline{e_{oQ}^2} = \left(\overline{ENI_S^2} + \overline{I_1^2}|_{ENV_F^2} + \overline{I_1^2}|_{ENI_F^2} + \overline{I_1^2}|_{R_D} \right) Z_{C_F}^2 \quad (2.36)$$

The output noise voltage due to the series equivalent noise voltage source ($\overline{ENV^2}$) is given by Equation (2.14). The total output noise voltage of the charge loop is the sum of Equations (2.14) and (2.36) or

$$\overline{E_O^2} = \left(\overline{ENI_S^2} + \overline{I_1^2}|_{ENV_F^2} + \overline{I_1^2}|_{ENI_F^2} + \overline{I_1^2}|_{R_D} \right) Z_{C_F}^2 + \overline{ENV_S^2} \left(\frac{C_F + C_D}{C_F} \right)^2 \quad (2.37)$$

The equivalent input noise can be converted to ENC by replacing $\overline{ENI^2}$

in Equation 2.27 with $\overline{ENI_Q^2}$ in (2.35), or

$$\overline{e_n^2} = \left[\overline{ENV_S^2} + \overline{ENI_Q^2} Z_{PP}^2 \right] \quad . \quad (2.38)$$

In this equation Z_{PP} is the input impedance of the amplifier and is

$$Z_{PP} = \left| \frac{1}{(C_{IN_QLOOP} + C_{DET} + C_{IN_FAST})\omega} \right| \quad . \quad (2.39)$$

The effect of the inductor as shown in Figure 2.7 is neglected in Equation (2.39) since the inductor is included to add delay and primarily to shunt R_D at lower frequencies where the gain of the shaping amplifier is large.

The output noise voltage of the timing section can also be found from Figure 2.7. The output noise voltage due to the series noise is

$$\overline{e_{oF}^2} = (\overline{ENV_F^2}) (A_{VF})^2 \quad , \quad (2.40)$$

where A_{VF} is the voltage gain of the fast stage. The output noise voltage of the fast stage due to the parallel noise current is

$$\overline{e_{oF}^2} = (\overline{ENI_F^2} + \overline{ENI_{RD}^2}) Z_{PF}^2 A_V^2 \quad , \quad (2.41)$$

where Z_{PF} is

$$Z_{PF} = \frac{1}{\left| (C_{DET} + C_{INF})\omega \right| \left| (L\omega \parallel R_D) \right|} \quad . \quad (2.42)$$

However, for timing information, the important part of the signal is the leading edge, therefore the noise bandwidth may be reduced by insuring a high-pass function (differentiation) such that the signal passes sufficient width to trigger amplitude discriminators. The use of a high pass filter greatly reduces the contribution of low frequency noise and allows Equation (2.42) to be reduced to

$$Z_{PF} = \left| \frac{1}{(C_{DET} + C_{INF})\omega} \right| \quad (2.43)$$

The total output noise voltage for the fast stage is

$$\overline{e_{oF}^2} = (\overline{ENV_F^2}) A_{VF}^2 + (\overline{ENI_F^2} + \overline{ENI_{R_D}^2}) Z_{PF}^2 A_{VF}^2 \quad (2.44)$$

The parallel timing pick-off approach yields a conversion gain of

$$V_{OT} = \left(\frac{Q}{C_{DET} + C_{IN}} \right) A_{VF} \quad (2.45)$$

where Q is the equivalent charge liberated by the charged particle and is given by Equation (2.2). Equation (2.45) indicates that the output voltage of the parallel timing stage is directly proportional to the energy absorbed by the detector and inversely proportional to the detector capacitance (for detector capacitance much greater than the input capacitance of the fast amplifier). Unlike the previous approach, the timing output signal risetime does not depend upon the detector

capacitance. The timing resolution figure of merit is given by Equation (2.30) and will increase with detector capacitance due to the decrease in output voltage (signal slope).

Drain Pick-Off

In this approach (as shown in Figure 2.3, p. 7) the timing signal is picked off as an error signal at the drain of the charge sensitive input FET with additional gain.⁵ This approach provides the most cost and space effective solution since the majority of the components are shared by both signal sections, thus reducing duplication to a minimum. The timing output generally has a wave shape as shown in Figure 2.8. The risetime of the signal is determined by the high-frequency characteristics of the input FET and any subsequent gain stages. The time T_i is essentially the delay time of the charge sensitive amplifier and T_f is due to the risetime of the charge sensitive section. The response of the charge loop is the same as for the previously discussed approaches and the conversion gain is given by Equation (2.2). The output voltage as a function of energy for the timing signal (Figure 2.9) is

$$V_{OT} = \left(\frac{Q}{C_{IN} + C_{DET}} \right) g_m A_i R_L, \quad (2.46)$$

where g_m is the transconductance of the input FET and A_i is additional current gain. The output noise voltage, $\overline{V_{OT}^2}$, from the timing section is

$$\overline{V_{OT}^2} = (g_m A_i R_L)^2 \overline{ENV^2} + (g_m A_i R_L)^2 (\overline{ENI^2}) Z_p^2, \quad (2.47)$$

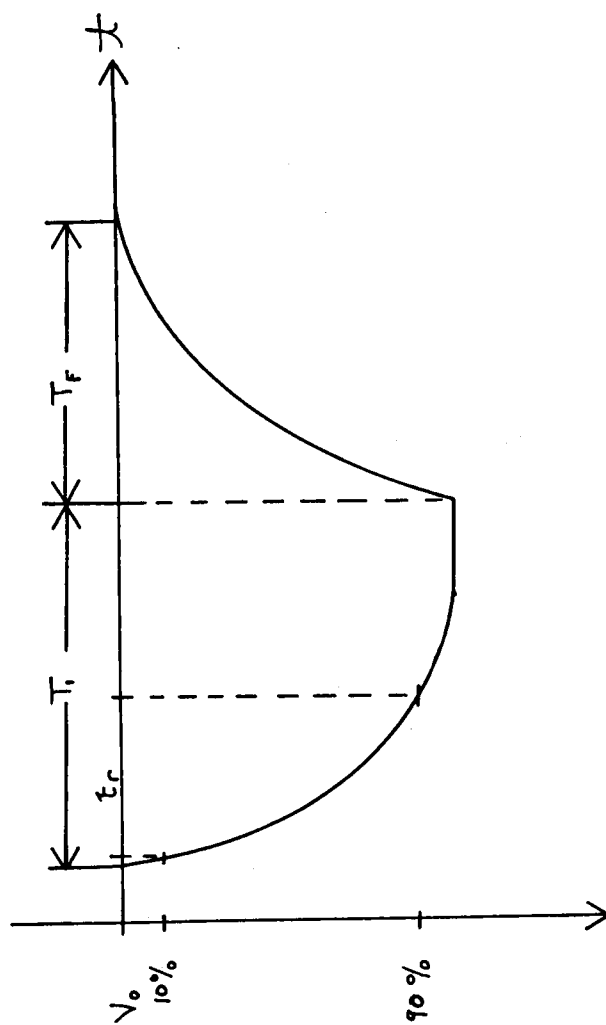


Figure 2.8. Shape of the drain pick-off signal as obtained at the FET drain.

the total input impedance (Z_p) is

$$Z_p = \frac{1}{|(C_F + C_{DET} + C_{IN})\omega| || R_F}, \quad (2.48)$$

and is approximately

$$Z_p = \left| \frac{1}{(C_F + C_{DET} + C_{IN})\omega} \right|. \quad (2.49)$$

The output noise voltage of the charge loop, $\overline{e_o^2}$, is

$$\overline{e_o^2} = \overline{ENV^2} \left(\frac{C_F + C_{DET} + C_{IN}}{C_F} \right)^2 + \overline{ENI^2} \overline{Z_p^2}. \quad (2.50)$$

The ENC can be found by substituting the value for $\overline{ENV^2}$ and $\overline{ENI^2}$ in Equation (2.17) and converting to the form given by Equation (2.21).

The ENC can then be computed using Equations (2.25) and (2.27).

Design Examples

The equations developed for the four amplifier configurations in the previous sections can be used to determine the optimum design approach. The optimum approach as defined in this study is the one that yields the best possible time resolution with no degradation of the energy resolution. Using this criterion, a cursory examination of the equations for energy resolution indicates that the parallel pick-off approach will consistently give inferior performance due to the added input capacitance. However, for the sake of clarity, all noise and time resolution comparisons will be made. The specifications in Table 2.1 will be used in all four configurations.

TABLE 2.1
 DEVICE PARAMETERS USED IN THE DESIGN EXAMPLES

AMPLIFIER PARAMETERS	ASSUMED VALUE
g_m	20m $\mathcal{U}$
C_{in}	15pF
R_F	500M Ω
C_F	1pF
R_D	100M Ω
τ TIMING	1nsec
τ DIFF	350nsec
GATE LEAKAGE CURRENT	10pA

Single pole system. The single pole system is shown in Figure 2.10. To find the equivalent input noise voltage, the second stage noise contribution will be neglected. For the FET specifications assumed, the $\overline{ENV^2}$ is

$$\overline{ENV^2} = \frac{8KT}{3g_m} = \frac{8}{3} \frac{(1.38 \times 10^{-23})(300)}{20 \times 10^{-3}} = 5.52 \times 10^{-19} \text{V}^2/\text{HZ} . \quad (2.51)$$

The $\overline{ENI^2}$ (assuming no detector leakage) is

$$\begin{aligned} \overline{ENI^2} &= 2eIg + \frac{4KT}{R_D} + \frac{4KT}{R_F} = \\ (2)(1.6 \times 10^{-19})(10 \times 10^{-12}) &+ (4)(1.38 \times 10^{-23})(300) \left(\frac{1}{500 \times 10^6} + \frac{1}{100 \times 10^6} \right) \\ &= 2.02 \times 10^{-28} \text{A}^2/\text{HZ} . \quad (2.52) \end{aligned}$$

To find the energy resolution of the preamplifier, the figure of merit (F) and the work function of silicon (w) must be known. A typical value of F for a state of the art shaping amplifier is 1.16 and the value of w for silicon is 3.6. The N.L.W. can be calculated using Equations (2.20 to 2.29), (2.51) and (2.52). The results have been calculated for various shaping times and detector capacitances and are shown in Table 2.2. If a preamplifier is to be used with a surface barrier detector, the electrical specifications are usually given for a shaping time of 2μsec. However, the experimenter will almost always use a shaping time of 0.5μsec because the leakage current of the detector

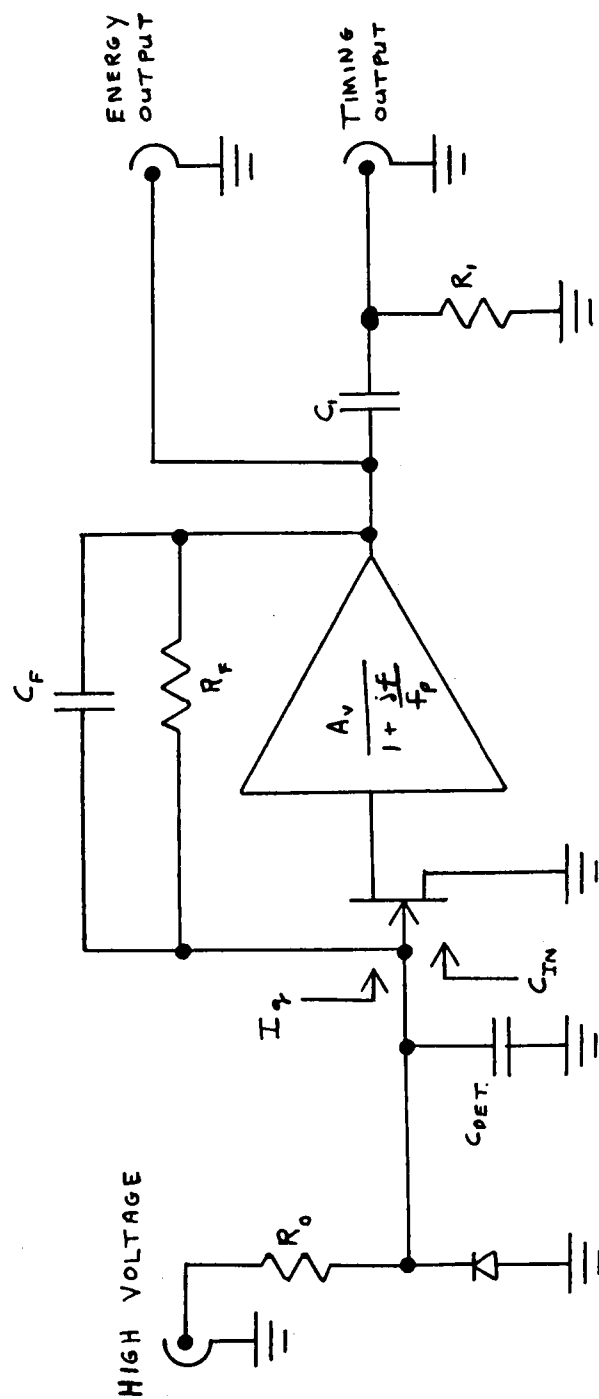


Figure 2.10. Single output system.

TABLE 2.2
N.L.W. OF SINGLE POLE, CONVENTIONAL CHARGE LOOP

$C_{DET.}$	$\tau_{OPT.}$	SHAPING TIME					
		0.25 μ sec	0.5 μ sec	1.0 μ sec	2.0 μ sec	3.0 μ sec	6.0 μ sec 10 μ sec
0 pF	0.78 μ sec	1.02keV	813eV	786eV	939eV	1.11keV	1.53keV 1.96keV
10 pF	1.3 μ sec	1.65keV	1.22keV	1.02keV	1.04keV	1.17keV	1.55keV 1.97keV
20 pF	1.83 μ sec	2.28keV	1.66keV	1.29keV	1.19keV	1.25keV	1.58keV 1.99keV
50 pF	3.4 μ sec	4.21keV	3.0 keV	2.19keV	1.72keV	1.62keV	1.74keV 2.06keV
100pF	6.0 μ sec	7.44keV	5.27keV	3.77keV	2.77keV	2.40keV	2.14keV 2.28keV
200pF	11.2 μ sec	13.9 keV	9.84keV	6.98keV	4.99keV	4.15keV	3.22keV 2.94keV

forces the optimum shaping time to a value that is less than $2\mu\text{sec}$.

The results obtained at $2\mu\text{sec}$ and $0.5\mu\text{sec}$ are shown in Figure 2.11.

The timing resolution is given by Equation (2.31) and is a function of the output risetime, bandwidth, amplitude and detector capacitance. The noise bandwidth will be determined by the risetime and the differentiation (high pass) network consisting of R and C in Figure 2.10. For convenience, this time constant (τ_{diff}) is assumed to be 350nsec . However, in practice, this value would be reduced to the lowest possible value to minimize noise bandwidth. This is shown in Figure 2.12. The noise bandwidth (N.B.W.) is

$$\text{N.B.W.} = \frac{\pi}{2} f_{hi} - \frac{2}{\pi} f_{LO} \quad , \quad (2.53)$$

where f_{LO} is

$$f_{LO} = \frac{0.35}{\tau_{\text{diff}}} \quad , \quad (2.54)$$

and f_{hi} is

$$f_{hi} = \frac{0.35}{\tau_r} \quad . \quad (2.55)$$

The output noise voltage e_o is

$$e_o = \left[\int_{\frac{2f_{LO}}{\pi}}^{\frac{\pi f_{hi}}{2}} \overline{ENV^2} \left(\frac{C_F + C_{DET} + C_{IN}}{C_F} \right)^2 df + \int_{\frac{2f_{LO}}{\pi}}^{\frac{\pi f_{hi}}{2}} \overline{ENI^2} |jX_{C_F}|^2 df \right]^{1/2} \quad . \quad (2.56)$$

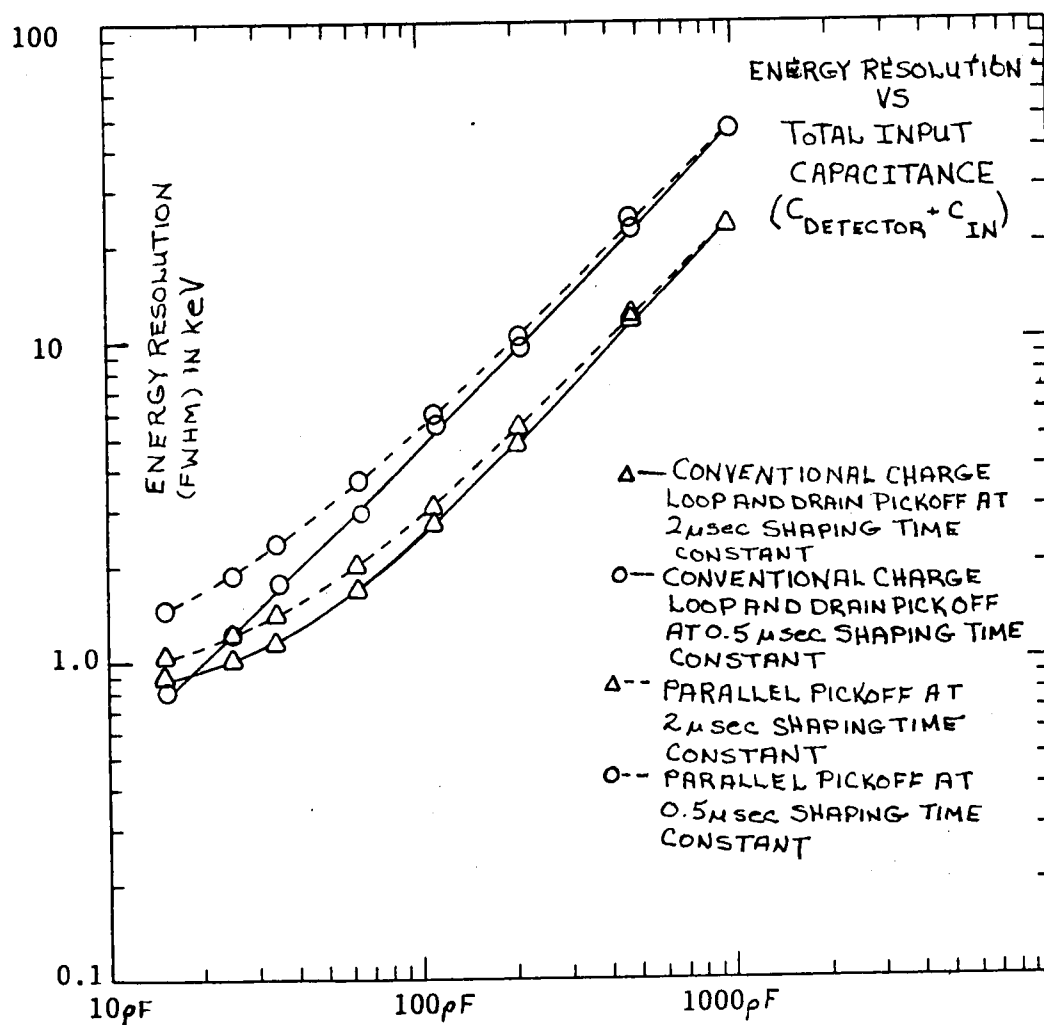


Figure 2.11. Energy resolution versus total input capacitance.

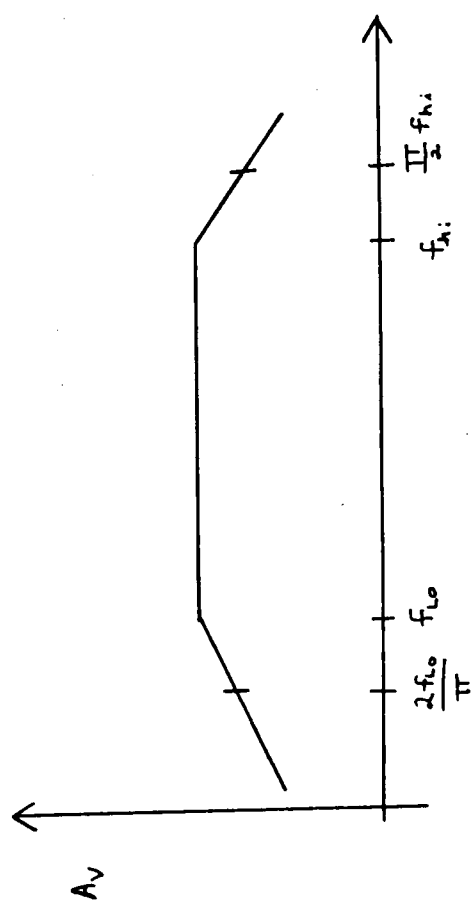


Figure 2.12. Noise bandwidth of timing loop.

As shown by Equation (2.56), decreasing τ_{diff} will reduce the contribution from the parallel noise and reduce the output noise voltage due to the series noise voltage. Increasing the low frequency cut off is feasible for timing data, since all essential information is contained in the leading edge. To determine the output noise voltage of the amplifier, the risetime must be known. This value is assumed to be 10nsec for zero detector capacitance. Table 2.3 contains the amplifier risetimes for values of detector capacitance up to 200pF where

$$\tau_r = \frac{C_{DET} + C_{IN} + C_F}{5.6 \times 10^{-4}} \quad (2.57)$$

The output noise voltage can be found by using the data in Table 2.3 and Equations (2.51 to 2.53) and (2.56). These data, along with the N.B.W. are shown in Table 2.4. The output amplitude of the timing signal is independent of the input capacitance and is given by Equation (2.1). The output voltage for an energy range of 0.1MeV to 100MeV is given in Table 2.5. The slope of the output signal (dv/dt) is given by the 10% to 90% output voltage divided by the risetime, or

$$\frac{dv}{dt} = \frac{0.8V_o}{\tau_r} \quad (2.58)$$

The time resolution can be found by dividing the output noise voltage (e_{orms}) by Equation (2.58) as shown in Equation (2.31). The results for various values of detector capacitance as a function of energy are shown in Figures 2.13 through 2.18.

TABLE 2.3
CHARGE LOOP OUTPUT RISETIME FOR SINGLE POLE SYSTEM

$C_{DET.}$	τ_r
0 pF	10 nsec
10 pF	16.7nsec
20 pF	23.3nsec
50 pF	43.4nsec
100pF	76.7nsec
200pF	143 nsec

TABLE 2.4
OUTPUT NOISE VOLTAGE FOR SINGLE POLE CHARGE LOOP

$C_{DET.}$	$\overline{e_o^2} _{ENV^2}$	$\overline{e_o^2} _{ENI^2}$	N.B.W.	e_{orms}
0 pF	$1.41 \times 10^{-16} V^2/Hz$	$4.28 \times 10^{-6} V^2/Hz$	54.5 MHz	0.090.2mV
10 pF	$3.73 \times 10^{-16} V^2/Hz$	f^2	32.3 MHz	0.112 mV
20 pF	$7.15 \times 10^{-16} V^2/Hz$		23.0 MHz	0.131 mV
50 pF	$2.4 \times 10^{-15} V^2/Hz$		12.1 MHz	0.172 mV
100pF	$7.43 \times 10^{-15} V^2/Hz$		6.53MHz	0.222 mV
200pF	$2.58 \times 10^{-14} V^2/Hz$		1.81MHz	0.218 mV

TABLE 2.5
ENERGY OUTPUT FOR SINGLE POLE CHARGE LOOP

E_{in}	V_o
0.1MeV	4.45mV
0.2MeV	8.9 mV
0.5MeV	22.3 mV
1.0MeV	44.5 mV
2.0MeV	89 mV
5.0MeV	223 mV
10.0MeV	445 mV
20.0MeV	890 mV
50.0MeV	2230 mV
100.0MeV	4400 mV

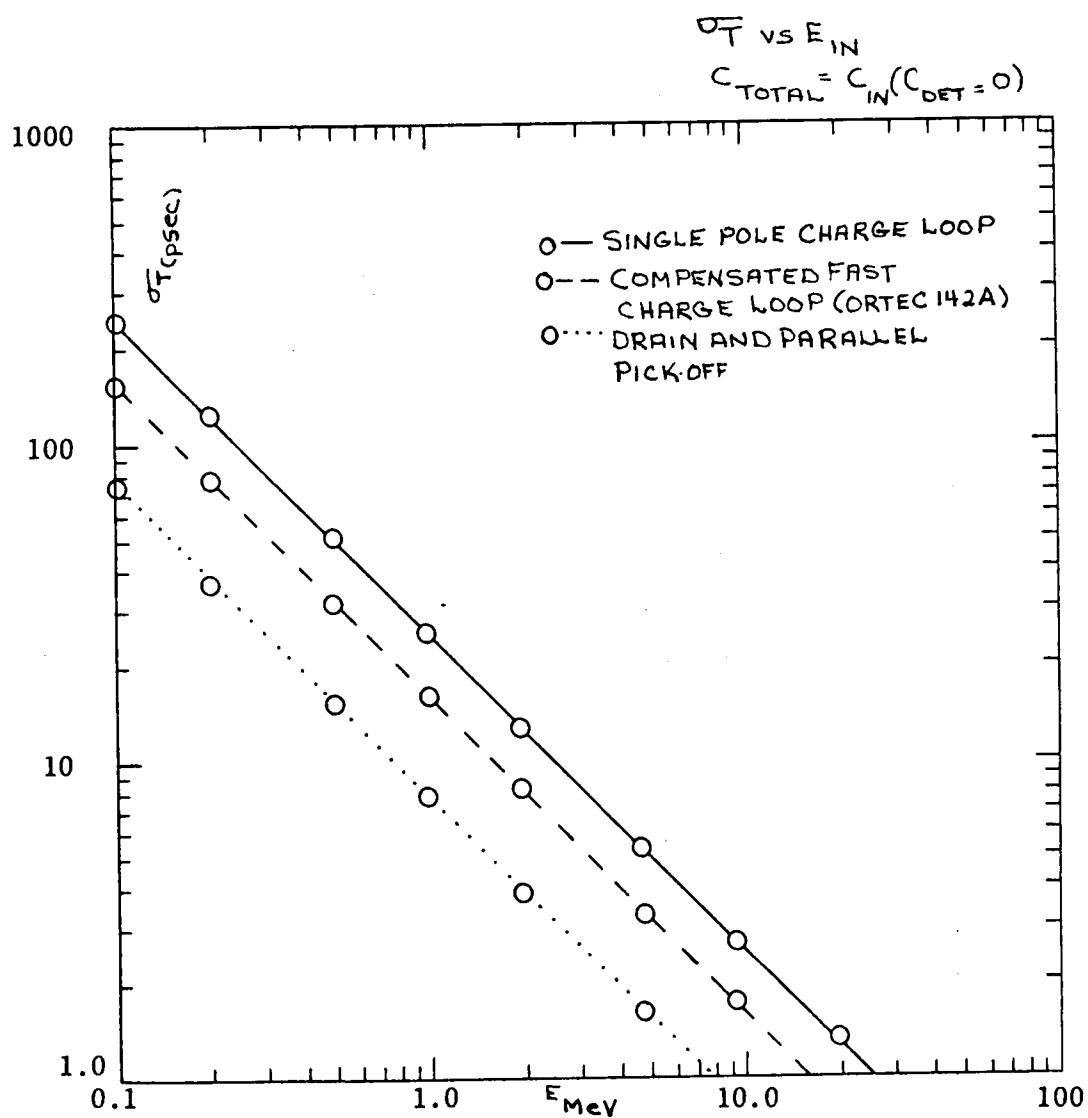


Figure 2.13. Timing resolution versus absorbed energy for C detector equal zero.

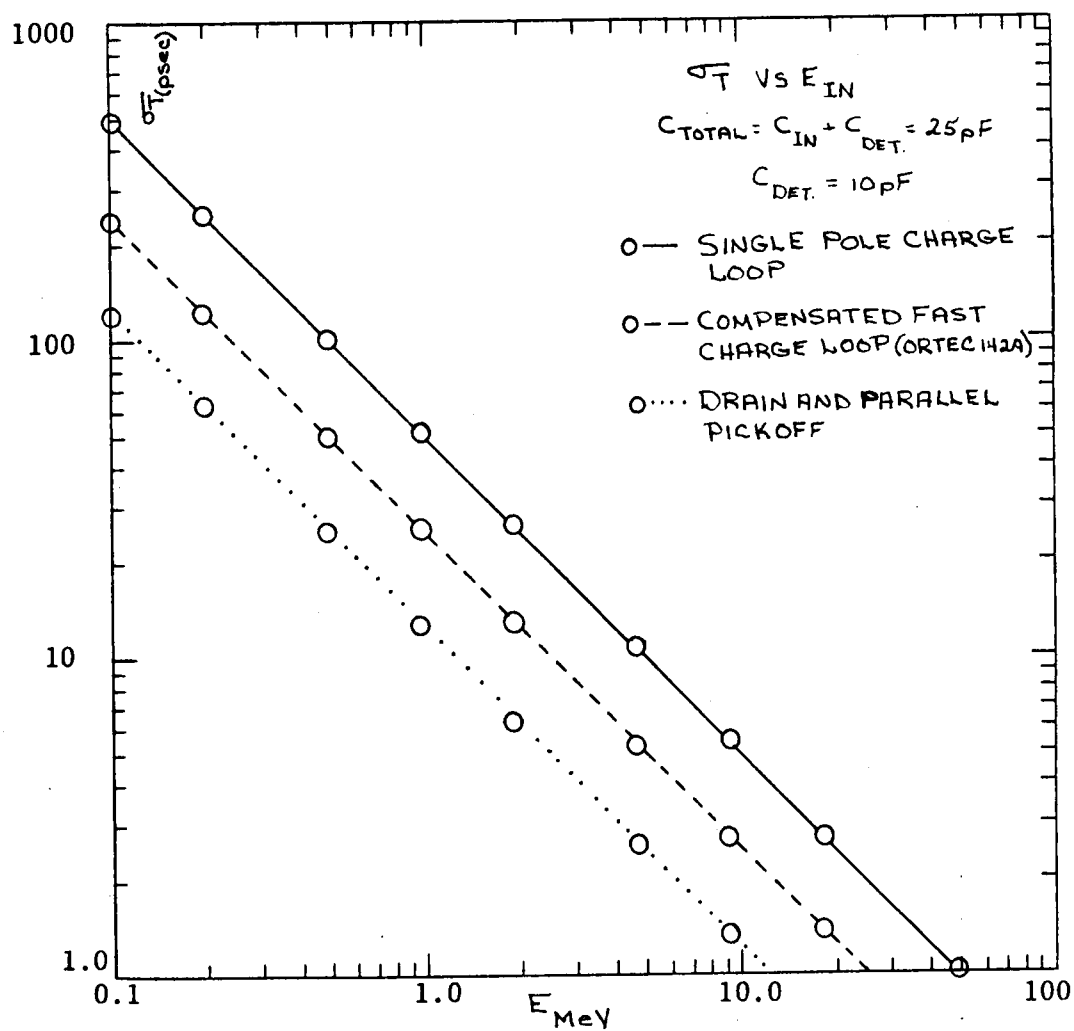


Figure 2.14. Timing resolution versus absorbed energy for a detector capacitance of 10pF.

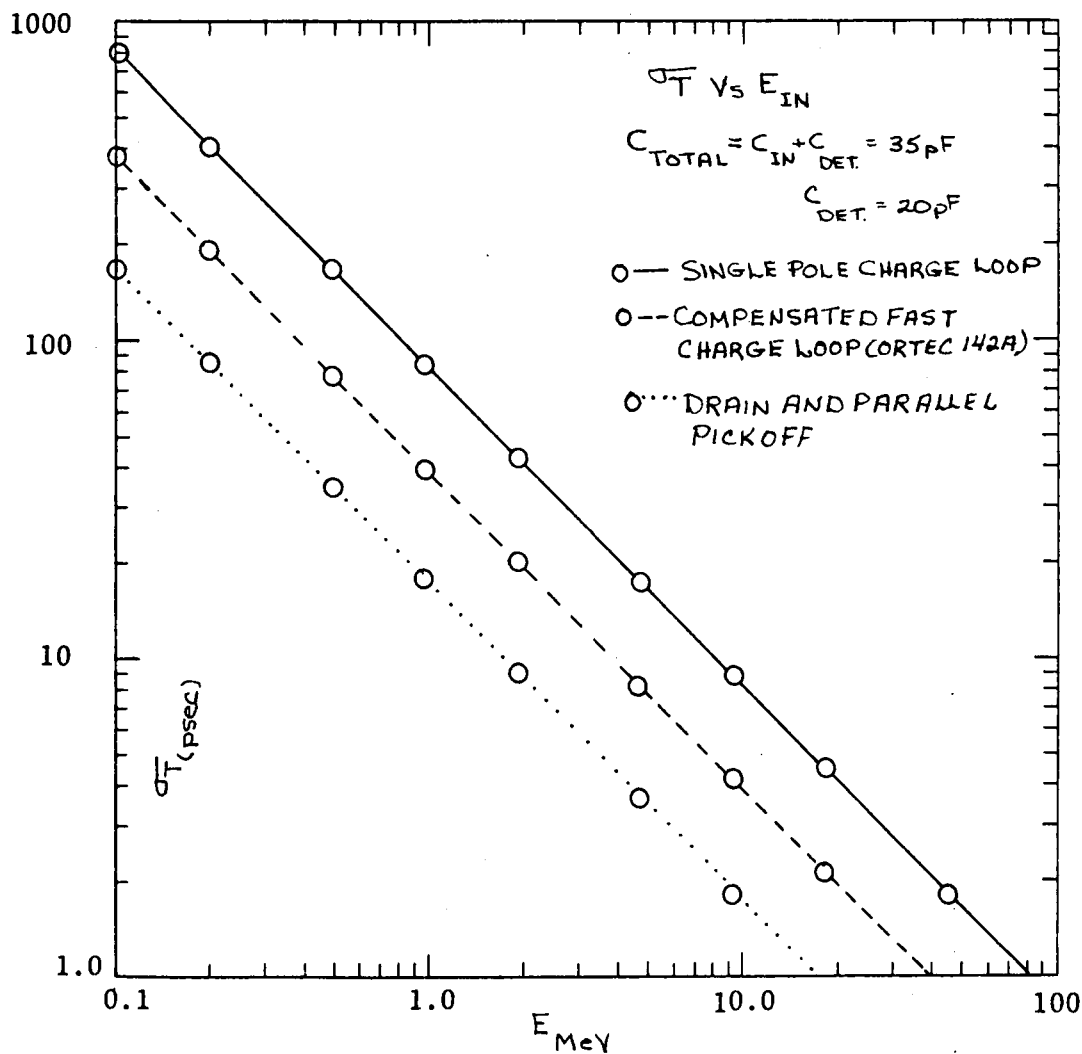


Figure 2.15. Timing resolution versus absorbed energy for a detector capacitance of 20pF.

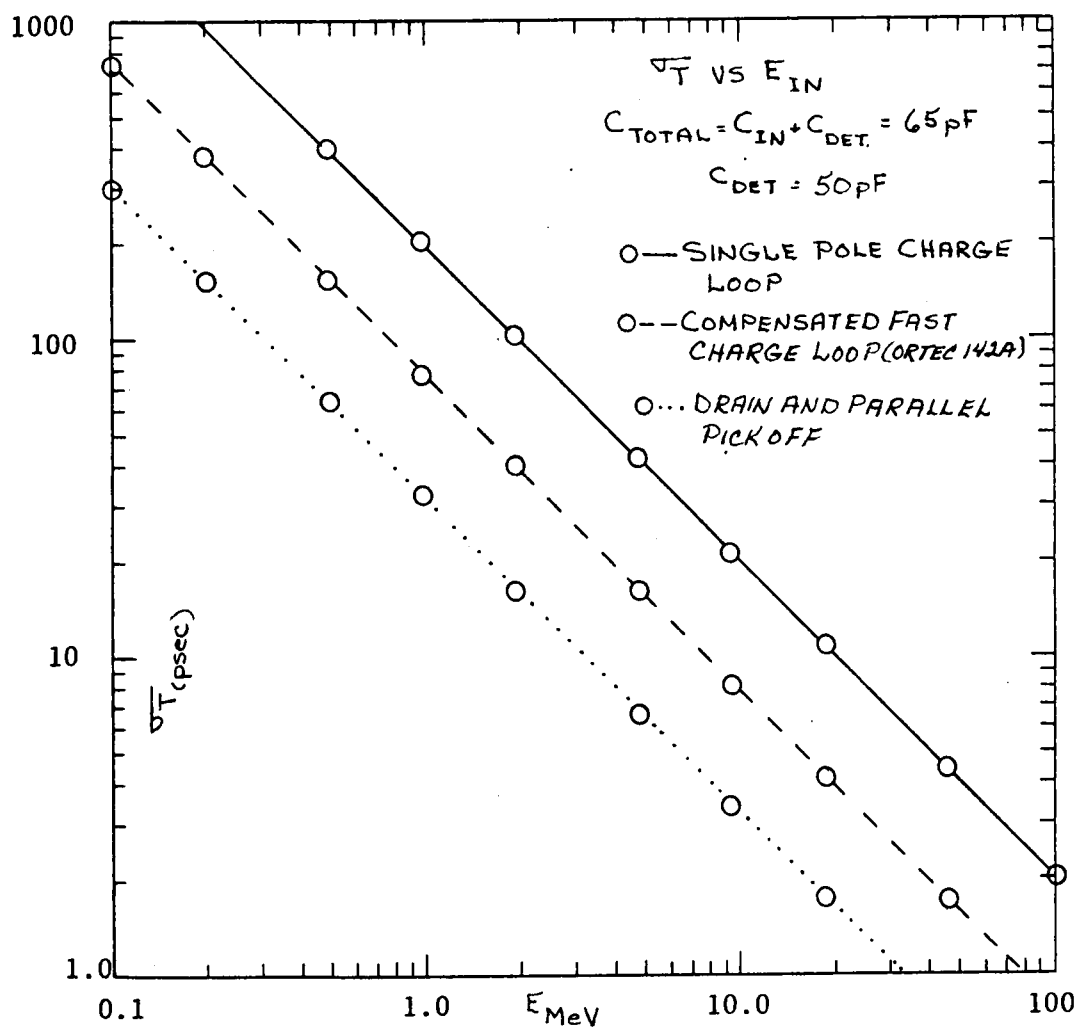


Figure 2.16. Timing resolution versus absorbed energy for a detector capacitance of 50 pF.

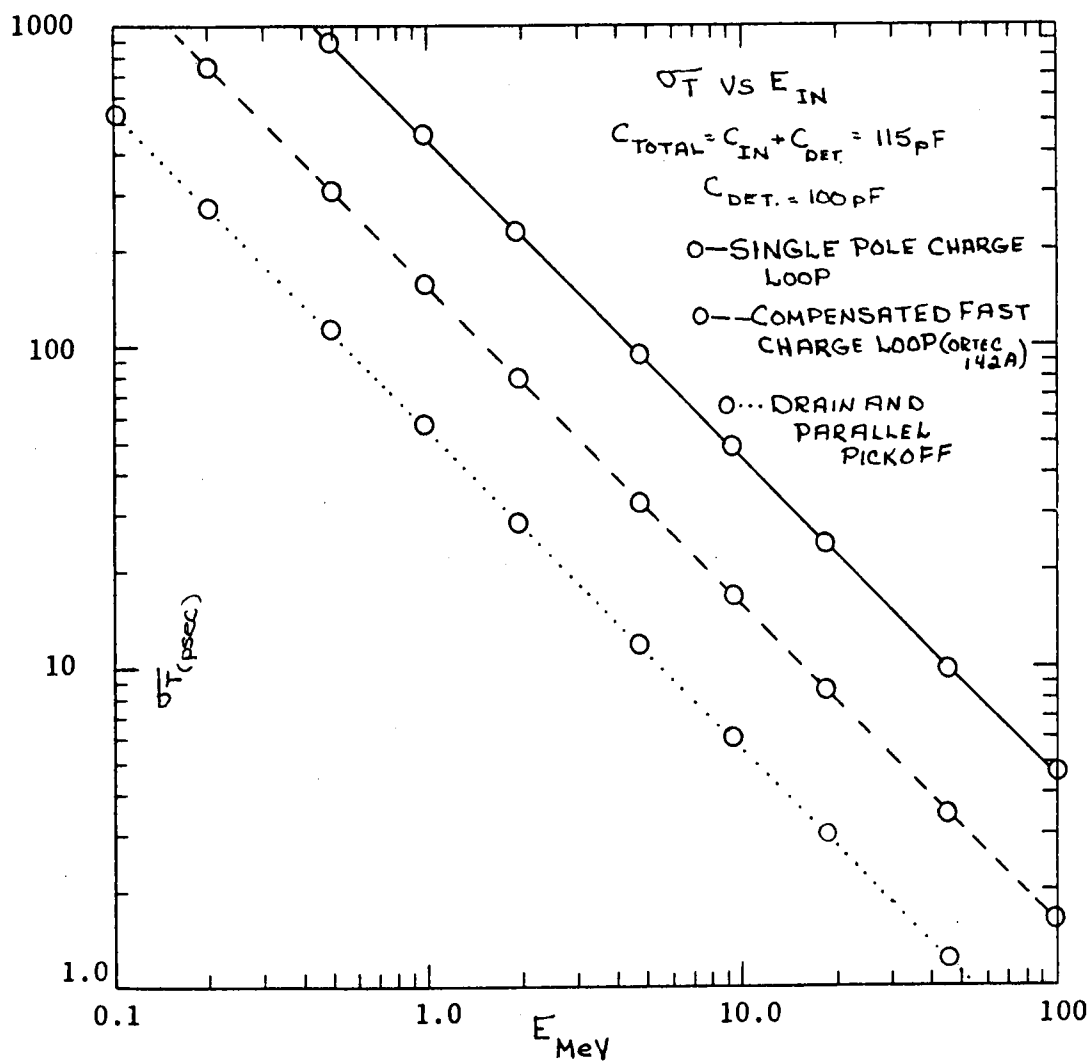


Figure 2.17. Timing resolution versus absorbed energy for a detector capacitance of 100pF.

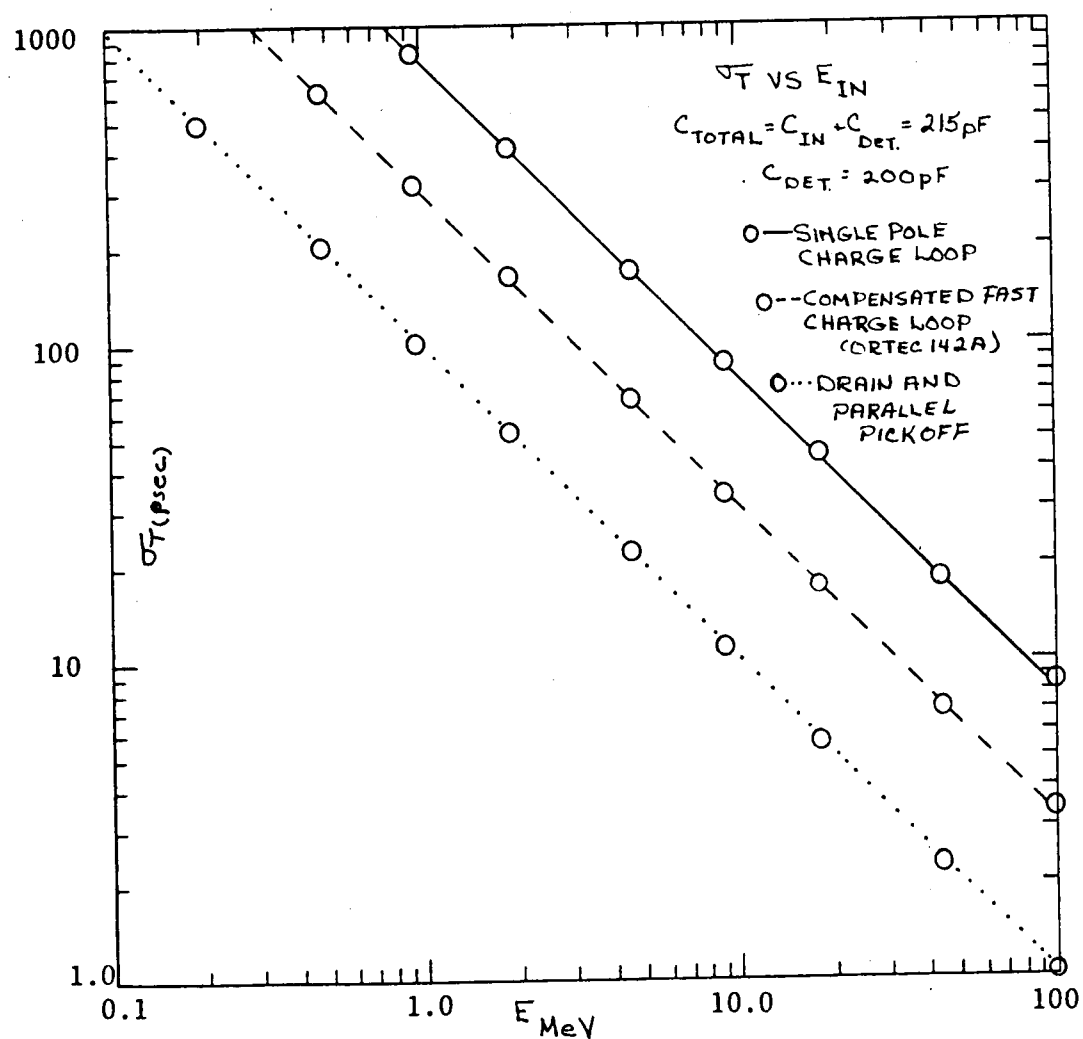


Figure 2.18. Timing resolution versus absorbed energy for a detector capacitance of 200pF.

Compensated fast charge loop. The results obtained in the previous section indicate that significant improvements in time resolution could be made if the risetime of the amplifier could be reduced. Such an amplifier has been designed by Karlovac and Mayhugh.⁶ This design approach was chosen to optimize both energy and timing performance. As noted in the paper, significant problems with stability develop when short lengths of cable are installed between the preamplifier and detector. The stability problem due to long cables is reduced as the risetime is increased. The block diagram in Figure 2.10, p. 29, also indicates this approach. The N.L.W. will be the same as the single-pole approach assuming equivalent noise sources and is shown in Figure 2.11, p. 32, and Table 2.1, p. 27. The risetime of such a system is taken from the paper and is given in Table 2.6. The output noise voltage can be calculated in the same way as for the single-pole system and is given in Table 2.7. The conversion gain is given by Equation (2.1) and is shown in Table 2.5, p. 37. The time resolution can be found by Equation (2.31). The results for various values of detector capacitance versus energy are shown in Figures 2.13 through 2.18.

Drain pick-off. The block diagram of the drain pick-off approach is shown in Figure 2.2, p. 7. The charge loop is conventional and will yield the same energy results as the previous two examples. The N.L.W. is shown in Figure 2.11, p. 32. The timing output will be assumed to have a voltage gain of 10 and a risetime of 1nsec, independent of detector capacitance. The timing output noise voltage e_{OT} is

TABLE 2.6
RISETIME OF FAST RISETIME COMPENSATED PREAMPLIFIER

$C_{DET.}$	τ_r
0 pF	4nsec
10 pF	4nsec
20 pF	5nsec
50 pF	6nsec
100pF	8nsec
200pF	10nsec

TABLE 2.7
OUTPUT NOISE VOLTAGE OF FAST RISETIME
COMPENSATED PREAMPLIFIER

$C_{\text{DET.}}$	$\overline{e_o^2} _{\text{ENV}^2}$	$\overline{e_o^2} _{\text{ENI}^2}$	N.B.W.	e_{orms}
0 pF	$1.41 \times 10^{-16} \text{V}^2/\text{Hz}$	$4.28 \times 10^{-6} \text{A}^2/\text{Hz}$	136 MHz	0.141mV
10 pF	$3.73 \times 10^{-16} \text{V}^2/\text{Hz}$	f^2	136 MHz	0.228mV
20 pF	$7.15 \times 10^{-16} \text{V}^2/\text{Hz}$	↓	109 MHz	0.282mV
50 pF	$2.4 \times 10^{-15} \text{V}^2/\text{Hz}$		91 MHz	0.470mV
100pF	$7.43 \times 10^{-15} \text{V}^2/\text{Hz}$		68.1MHz	0.714mV
200pF	$2.58 \times 10^{-14} \text{V}^2/\text{Hz}$		54.4MHz	1.19mV

$$e_{OT} = \left[A_V^2 \overline{ENV^2} \int_{\frac{2f_{LO}}{\pi}}^{\frac{\pi f_{hi}}{2}} df + A_V^2 \overline{ENI^2} \int_{\frac{2f_{LO}}{\pi}}^{\frac{\pi f_{hi}}{2}} |jX_{CTOTAL}| df \right]^{1/2} \quad (2.59)$$

The conversion gain for the timing output is

$$V_{OT} = \frac{(440mV)E}{C_{TOTAL}} \quad , \quad (2.60)$$

where E is the energy in MeV and C_{TOTAL} is

$$C_{TOTAL} = C_{IN} + C_F + C_{DET} \quad . \quad (2.61)$$

Values for the peak timing output voltage are given in Table 2.8 for energies from 0.1MeV to 100MeV and for capacitance values up to 200pF. The timing output noise voltage is given in Table 2.9. As indicated in this table, the timing output noise voltage is nearly independent of detector capacitance. The time resolution, $\overline{T}$, is

$$\overline{T} = \frac{e_{orms}}{0.8V_o/\tau_r} \quad . \quad (2.62)$$

The timing resolution is shown in Figures 2.13 through 2.18 for various values of detector capacitance and energies.

Parallel pick-off. The parallel pick-off system is shown in Figure 2.3, p. 7. The equivalent input noise voltage for the charge sensitive section is given by Equation (2.51). The equivalent input

TABLE 2.8

TIMING OUTPUT VOLTAGE OF DRAIN PICK-OFF PREAMPLIFIER
AS A FUNCTION OF DETECTOR CAPACITANCE

E_{in}	OpF	10pF	20pF	50pF	100pF	200pF
0.1MeV	2.9mV	1.76mV	1.26mV	0.68mV	0.38mV	0.2 mV
0.2Mev	5.9mV	3.52mV	2.51mV	1.35mV	0.76mV	0.41mV
0.5MeV	14.7mV	8.8 mV	6.29mV	3.38mV	1.91mV	1.02mV
1.0MeV	29.3mV	17.6 mV	12.6 mV	6.77mV	3.8 mV	2.05mV
2.0MeV	58.7mV	35.2 mV	25.1 mV	13.5 mV	7.65mV	4.1 mV
5.0MeV	147 mV	88 mV	62.9 mV	33.8 mV	19.1 mV	10.2 mV
10 MeV	293 mV	176 mV	126 mV	67.7 mV	38.3 mV	20.5 mV
20 MeV	587 mV	352 mV	251 mV	135 mV	76.5 mV	40.9 mV
50 MeV	1470mV	880 mV	629 mV	338 mV	191 mV	102 mV
100MeV	2930mV	1760 mV	1260 mV	677 mV	383 mV	205 mV

TABLE 2.9
OUTPUT NOISE VOLTAGE OF DRAIN PICK-OFF PREAMPLIFIER

C_{DET}	$\overline{e_o^2} _{ENV^2}$	e_{orms}	N.B.W.
0 pF	$5.52 \times 10^{-17} V^2/Hz$	0.176mV	549MHz
10 pF	↓	0.175mV	↓
20 pF		0.174mV	
50 pF		↓	
100pF		↓	
200pF			

noise current is given by Equation (2.35). The total input capacitance seen by the charge sensitive amplifier is

$$C_{TO} = C_{IN} + C_{IN_{FAST}} + C_{DET} + C_F \quad . \quad (2.63)$$

Following the method used in the previous sections, the N.L.W. can be found. The results were calculated for various shaping times and the results are given in Table 2.10. The results for shaping times of 0.5μsec and 2.0μsec are shown in Figure 2.11, p. 32. The timing performance is identical to the drain pick-off stage since the same FET, gain and risetime have been assumed. These results are shown in Figures 2.13 through 2.18 (pp. 38 through 43).

Conclusions

A comparison of the various approaches for N.L.W. indicates that the parallel pick-off design has higher N.L.W. The higher N.L.W. is due to the added input capacitance and leakage current of the second stage. The optimum shaping time is longer for the drain pick-off than the other approaches, again due to the added capacitance and gate leakage. These differences could be reduced by using a lower capacitance and lower gate leakage device for the fast amplifier. However, care must be used to insure that the noise performance of the timing section is not degraded by using a low transconductance device. The timing performance of the four approaches are shown in Figures 2.13 through 2.18 (pp. 38 through 43). The parallel and drain pick-off systems have identical performance and are superior to the fast charge loop. One possible problem is that practical minimum discriminator thresholds are on the order of 30mV. The 30mV discriminator level will result in an

TABLE 2.10
N.L.W. OF PARALLEL PICK-OFF PREAMPLIFIER

C_{DET}	τ_{OPT}	0.25 μ sec	0.5 μ sec	1.0 μ sec	2.0 μ sec	3.0 μ sec	6.0 μ sec	10 μ sec
0 pF	1.56 μ sec	1.96keV	1.44keV	1.15keV	1.12keV	1.22keV	1.58keV	1.99keV
10 pF	2.1 μ sec	2.60keV	1.88keV	1.43keV	1.27keV	1.31keV	1.61keV	2.01keV
20 pF	2.6 μ sec	3.25keV	2.33keV	1.73keV	1.44keV	1.43keV	1.66keV	2.03keV
50 pF	4.1 μ sec	5.18keV	3.68keV	2.66keV	2.03keV	1.84keV	1.86keV	2.13keV
100pF	6.7 μ sec	8.41keV	5.96keV	4.25keV	3.10keV	2.65keV	2.30keV	2.38keV
200pF	12 μ sec	14.9 keV	10.5 keV	7.46keV	5.33keV	4.43keV	3.40keV	3.07keV

inadequate signal amplitude to trigger a start or stop function for the conventional charge loop below energies of approximately 0.7MeV. Additional gain will be required and the noise and risetime of this gain will increase the time resolution. The drain and parallel pick-off methods provide the best time resolutions. However, when additional gain is required, these systems will be more dependent on the noise and particularly the risetime of the additional gain. This dependence is due to the fast risetime characteristic of the signal from these two amplifiers. The net effect will be to reduce the difference (possibly even provide worse performance) between the drain or parallel pick-off and the conventional charge loop. However, where no N.L.W. degradation can be tolerated and the best time resolution is required, the drain pick-off arrangement will provide superior performance.

CHAPTER 3

DRAIN PICK-OFF

Introduction

The results of the previous chapter show that in order to obtain a timing signal with no degradation of the N.L.W., either of the two approaches shown in Figure 3.1 may be used. In order to obtain the best timing performance, either of the two preamplifiers in Figure 3.2 may be used. If both energy and time resolution must be optimized, the preamplifier shown in Figure 3.3 should be used. The design of a preamplifier utilizing the drain pick-off approach is presented. The theoretical results of the timing section and energy section are presented.

Timing Chain

The time resolution of the timing section is determined by the equivalent input noise and the risetime of the timing section. The noise performance in a good design should be determined by the input device. The second stage should contribute less than 5% to 10% of the total input noise. The timing section risetime is controlled by three stages as shown in Figure 3.4. The limitations imposed on the timing chain risetime due to the first stage are associated with the detector, input cable length and input capacitance. The detector contact resistance, excessive contact resistance due to the input connector, cable capacitance and preamplifier input capacitance form an integrator network with a time constant of

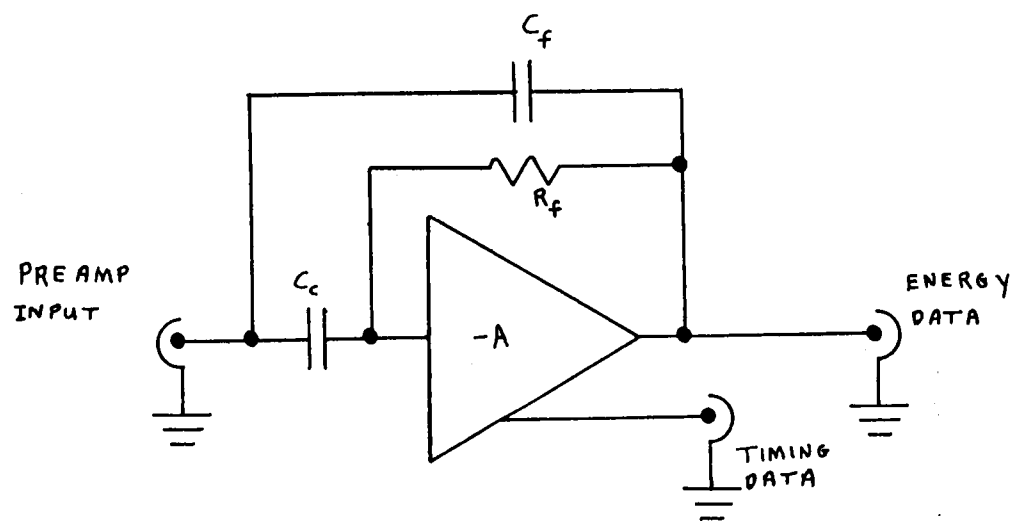
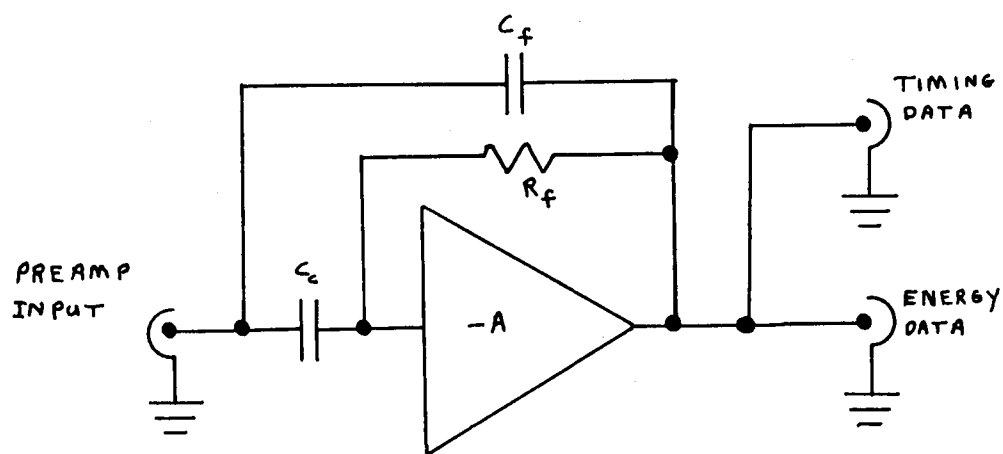


Figure 3.1. (a) Conventional or risetime compensated preamplifier using energy signal for timing output; (b) Drain pick-off preamplifier.

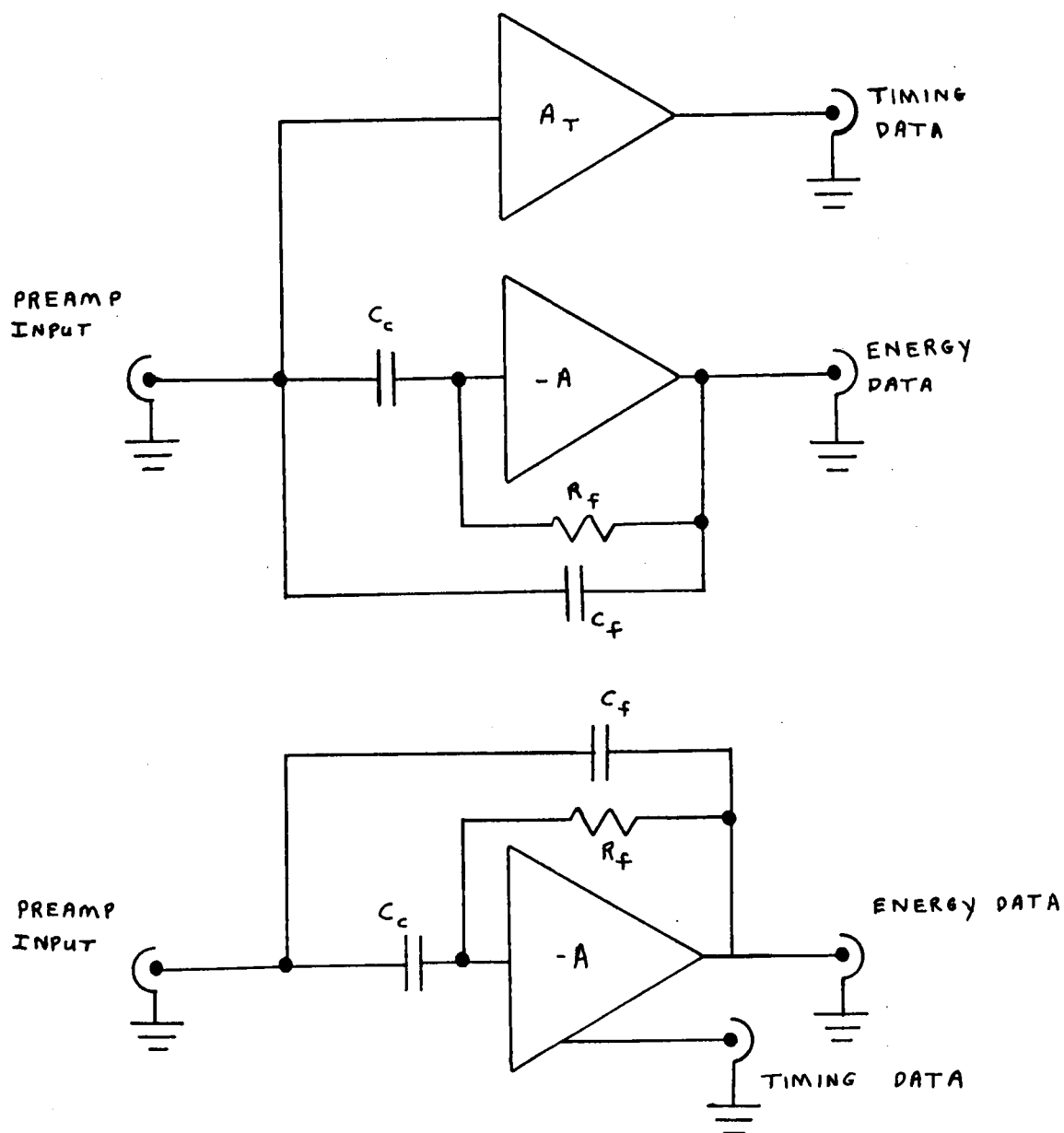


Figure 3.2. (a) Parallel pick-off preamplifier; (b) Drain pick-off preamplifier.

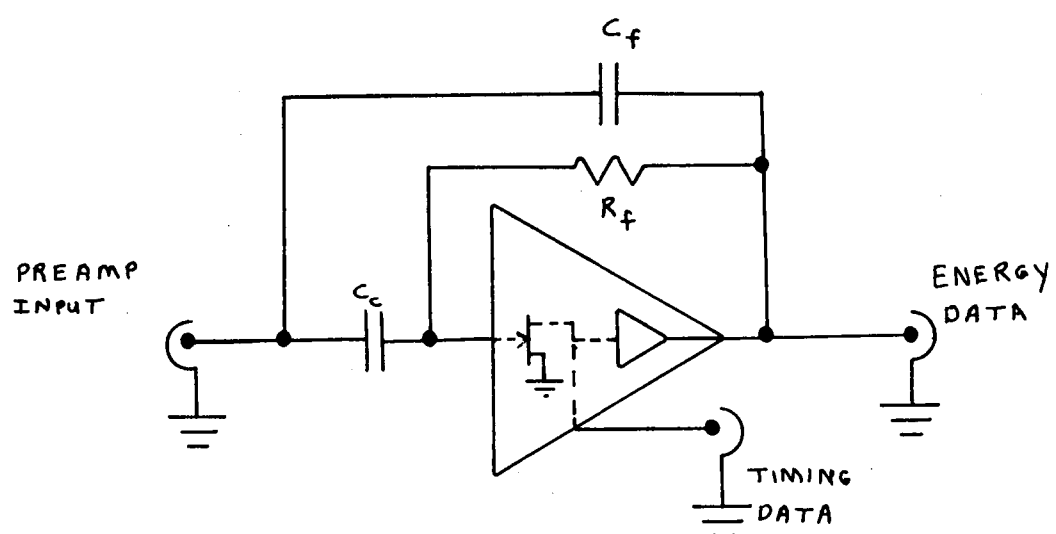


Figure 3.3. Drain pick-off preamplifier.

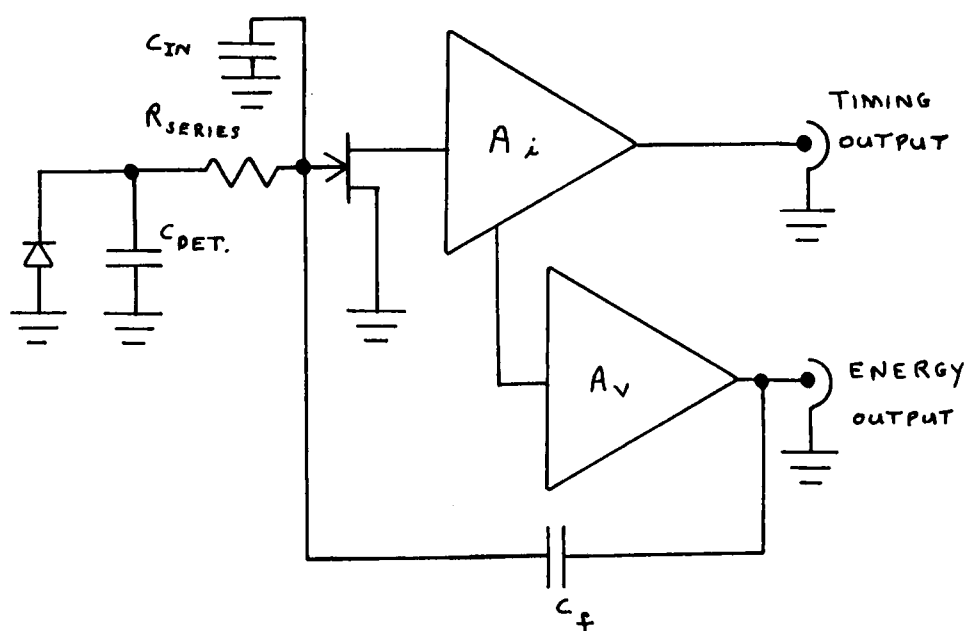


Figure 3.4. Basic drain pick-off preamplifier including stages controlling timing risetime.

$$\tau_{\text{STRAY}} = \left(R_{\text{SERIES}} \right) C_{\text{in}} , \quad (3.1)$$

where R_{SERIES} is the series contact resistance and C_{in} is the FET input capacitance. For typical values of R_{SERIES} equal to 2Ω , and C_{in} equal to 15pF the input time constant τ_{STRAY} is

$$\tau_{\text{STRAY}} = (2\Omega)(15 \times 10^{-12}\text{pF}) = 30 \times 10^{-12}\text{sec} . \quad (3.2)$$

This value is negligible compared to realizable risetimes and can be neglected.

The FET noise and frequency response limitations have been thoroughly investigated by V. Radika.¹² The FET high frequency cutoff point is defined as the frequency at which the transconductance decreases to $1/\sqrt{2}$ of its d.c. value. The high frequency cutoff point (f_o) is

$$f_o = \frac{\beta g_m}{C_{gs}} , \quad (3.3)$$

where β is a constant determined by device geometry and C_{gs} is the gate to source capacitance. Equation (3.3) can be rewritten to show the dependence of f_o on device geometry

$$f_o = \left(\frac{\mu W_{oo}}{L^2} \right) \left(\frac{2\beta}{3} f_2 W_g \right) , \quad (3.4)$$

where μ is the carrier mobility, L is the channel length, W_{oo} is the saturation voltage, f_2 is a figure of merit with a broad maximum and β is a constant dependent upon charge density profile. The value of β is equal to approximately 1/3 for uniform charge distribution. The value of W_{oo} cannot increase above a practical limit of 4 to 6 volts in order to limit power dissipation. Increased power dissipation would

result in increased low frequency noise and higher gate leakage current. With limits on the value of W_{oo} , f_o can be increased by increasing the carrier mobility by using a material such as gallium arsenide or by decreasing the channel length.

In order for the input FET to perform both functions, low noise energy spectroscopy and fast timing, the transconductance must be high and C_{gs} must be low. The choice of FET's on their noise performance cannot be made on gm alone as the excess noise, or $1/f$ noise, can be a significant contribution depending upon where the low frequency noise corner occurs. The high frequency cutoff of the FET can be approximated by Equation (3.3) and the results verified by experimentally determining the FET cutoff frequency experimentally using the measured FET rise time and Equation (3.5)

$$f_o = \frac{0.35}{\tau_{rFET}} \quad , \quad (3.5)$$

where τ_{rFET} is experimentally measured.

The following FET types were evaluated according to Equation (3.3), SFB8558, 2N4393, 2N6454, 2N6452, 2N3972, SFC5960 and the results are in Table 3.1. The FET risetimes were experimentally measured using the circuit in Figure 3.5. The pulser used was an avalanche pulser with a risetime of approximately 300psec. The cutoff frequency determined by Equation (3.3) and (3.5) do not agree for any device measured. The results are within reasonable error for the 2N3972, however the remaining devices have differences in excess of 200%. The constant β in Equation (3.3) is approximated as $1/3$ for FET's with uniform charge

TABLE 3.1
THEORETICAL FET CUTOFF FREQUENCY

FET	gm	C _{gs}	f _o *
2N4393	20 m℧	3.5pF	1.9 GHz
SFC14978	263 m℧	--	--
2N6454	28 m℧	5 pF	1.87GHz
2N6452	243 m℧	5 pF	1.62GHz
SFC5960	26.8m℧	--	--
2N3972	16.7m℧	6 pF	928 MHz

$$^* f_o = \frac{gm}{3C_{gs}}$$

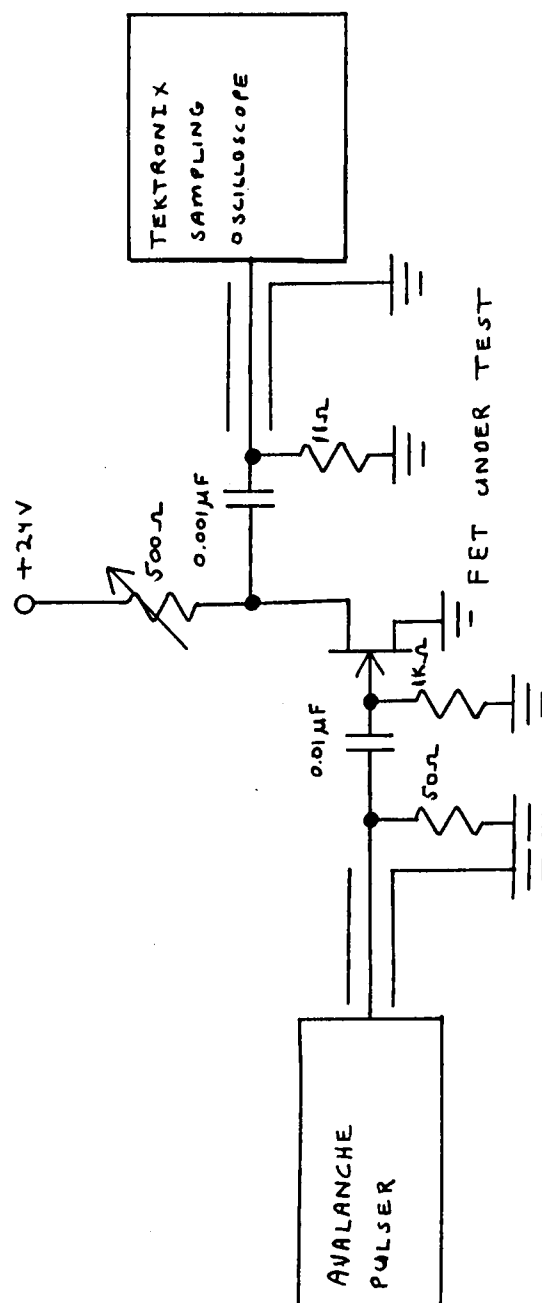


Figure 3.5. Circuit used to measure FET risetime.

distribution. The results obtained indicate that the constant β is in error or the devices tested did not have uniform charge distribution. The results of Table 3.2 are not invalid as a direct measurement of the FET risetime is adequate. The 2N4393 FET is the fastest of the six types tested, yielding an average risetime of 422psec. This risetime is significant and must be considered when designing the timing chain of risetimes approaching 1nsec are required. The risetime requirement of the second stage can be determined by

$$\tau_{r2nd\ stage} = \sqrt{(1nsec)^2 - (\tau_{rFET})^2}, \quad (3.6)$$

where the second stage risetime is $\tau_{r2nd\ stage}$. For an FET risetime of 422psec, (assuming the 2N4393 FET) Equation (3.6) requires the second stage risetime to be 900psec or less to yield an overall timing section risetime of 1nsec. The requirement that the second stage contribute 10% or less of the total input noise requires that the input noise due to the second stage $\left(\overline{ENV_{2nd}^2}\right)$ is less than $5.22 \times 10^{-20} V^2/Hz$ or 33Ω series noise resistance based on the design example in Chapter 2.

The derivation of the timing signal from the error signal at the FET drain has historically been accomplished by using parallel amplifier stages, one for the timing data and one for the energy data.^{4,11} The use of parallel devices places more stringent requirements on the second stage design and device type due to the added noise sources. A possible configuration that eliminates the need for parallel stages is shown in Figure 3.6. The circuit in the dotted section is a current gain stage

TABLE 3.2
EXPERIMENTAL FET CUTOFF FREQUENCY

FET	τ_r	f_o^*	
2N4393	422psec	829MHz	AVERAGE OF 6
SFC1497	630psec	556MHz	AVERAGE OF 6
2N6454	668psec	524MHz	AVERAGE OF 6
2N6452	599psec	584MHz	AVERAGE OF 5
SFC5960	720psec	486MHz	AVERAGE OF 5
2N3972	488psec	717MHz	AVERAGE OF 5

$$^*f_o = \frac{0.35}{\tau_r}$$

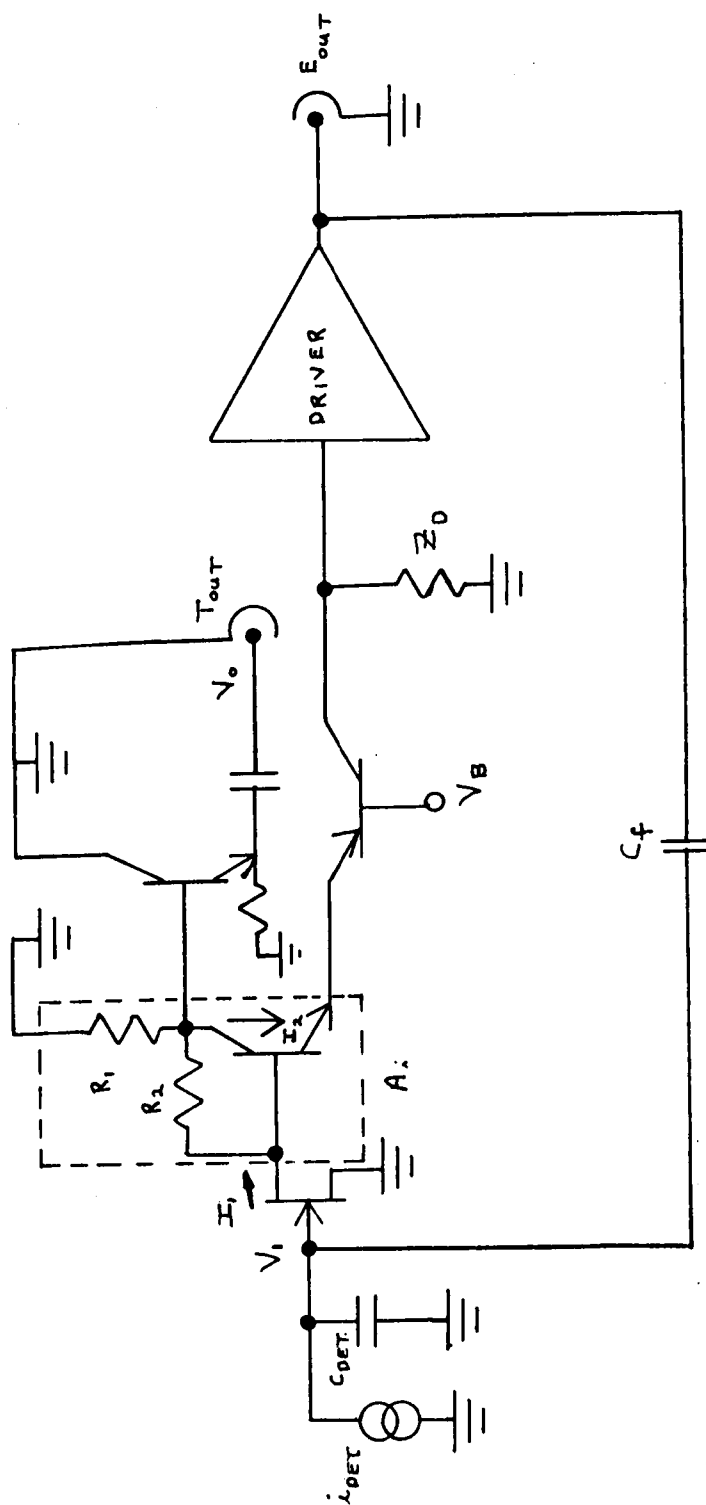


Figure 3.6. Proposed drain pick-off circuit.

(shunt feedback). The current gain (A_i) is

$$A_i = \frac{I_2}{I_1} = \frac{R_2 + R_1}{R_1} \quad (3.7)$$

The loop transmission of the charge loop is

$$T = \frac{g_m A_i Z_D (C_{DET} + C_{IN})}{C_f} \quad (3.8)$$

The voltage gain from the FET input to the timing output for the error signal is

$$\frac{V_o}{V_{in}} \approx g_m A_i R_L \quad (3.9)$$

Use of a stage similar to that shown in Figure 3.6 provides timing information and also provide an increase in the loop transmission of the charge sensitive section. The output current of the current gain section (I_o) is converted to a voltage by R_1 for the timing output. The use of this stage within the forward loop of a charge sensitive preamplifier was first described by Blalock,¹³ however, the timing data output was not used. A detailed description of its performance can be found in his paper. A similar approach was described by Karlovac and Mayhugh.⁶ An excellent analysis of suitable current gain stages is presented by Millard in a doctoral dissertation.¹⁴ The choice of the broadband current gain stage will draw upon the results obtained by Blalock and Millard as no attempt will be made to design a faster stage than is currently available.

Several suitable current gain stages are shown in Figure 3.7. The single-pole approximate analysis of the circuit in Figure 3.7a yields a bandwidth of

$$f_{-3dB} \approx \frac{f_T}{A_O} \quad , \quad (3.10)$$

where A_O is

$$A_O \approx \frac{I_O}{I_{in}} \approx \frac{R_F + R_L}{R_L} \quad , \quad (3.11)$$

and f_T is the gain bandwidth product of Q1. The performance of the single stage current gain configuration can be predicted using Equation (3.10). For a gain of 10 and an f_T of 5GHz, the high frequency cutoff point can be approximated as

$$f_{-3dB} = \frac{f_T}{A_O} = \frac{5\text{GHz}}{10} = 500\text{MHz} \quad . \quad (3.12)$$

The stage shown in Figure 3.7b was introduced by Rush.¹⁵ This stage has a lower input impedance than that of Figure 3.7a. The high frequency transfer characteristics are the same as for the circuit in Figure 3.7a if f_{α} of the input transistor is at least an order of magnitude greater than the current gain cutoff frequency.

The shunt-feedback stage developed by Millard¹⁴ (Figure 3.7c) is an improvement over the single stage configuration (Figure 3.7a). An emitter follower is placed inside the loop before Q1. The emitter follower shifts the dominate pole from the base of Q2 to the base of Q1. Due to the use of an emitter follower at the input, the input capacitance is greatly reduced as compared to that of Figure 3.7a. The circuit of

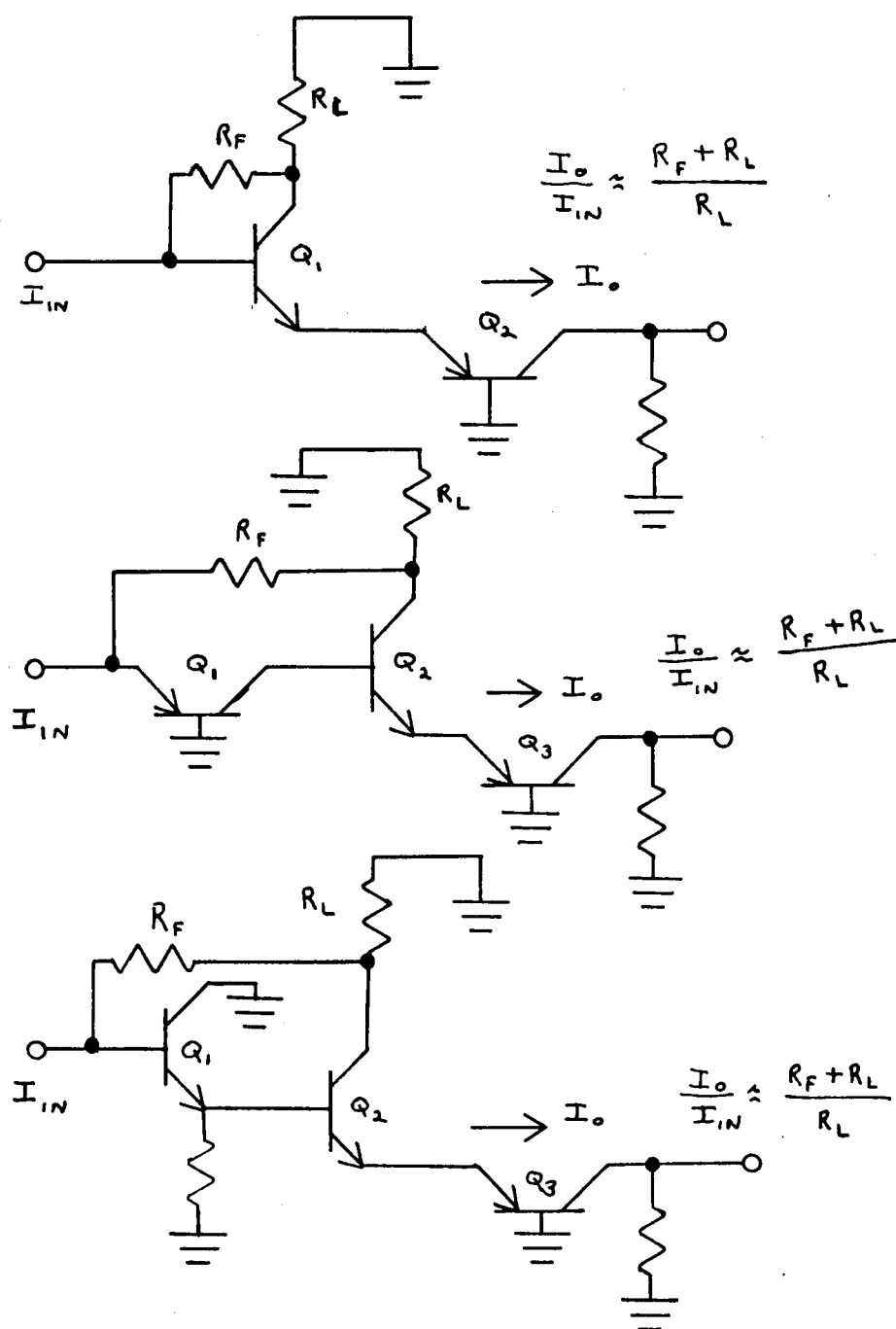


Figure 3.7. (a) Single stage shunt feedback circuit;
 (b) Two stage shunt feedback circuit;
 (c) Shunt feedback circuit proposed by Millard.

Figure 3.7c can be redrawn as in Figure 3.8 to facilitate analysis. The midband loop transmission ($A\beta$) is

$$A\beta = (A_{b_1b_2})(A_{b_2c_2})(A_{c_2b_1}) \quad , \quad (3.13)$$

where $A_{b_1b_2}$ is the voltage gain from the base of Q1 to the base of Q2, $A_{b_2c_2}$ is the voltage gain from the base of Q2 to the collector of Q2, and $A_{c_2b_1}$ is the gain from the collector of Q2 to the base of Q1. The midband gain from the base of Q1 to the base of Q2 is

$$A_{b_1b_2} = \frac{(\beta_2+1)(r_{e_2}+r_{e_3}) \parallel R_E}{[(\beta_2+1)(r_{e_2}+r_{e_3}) \parallel R_E] + r_{e_1}} \quad , \quad (3.14)$$

which can be approximated as unity. The midband gain from the base of Q2 to the collector of Q2 is

$$A_{b_2c_2} = \frac{-R_{Leq_2}}{(r_{e_2}+r_{e_3})} \quad , \quad (3.15)$$

where R_{Leq_2}

$$R_{Leq_2} = R_L \parallel (R_F + R_{in_1}) \quad , \quad (3.16)$$

and R_{in_1}

$$R_{in_1} = (\beta_1+1)[r_{e_1}+R_E \parallel (\beta_2+1)(r_{e_2}+r_{e_3})] \quad . \quad (3.17)$$

Equation (3.15) can be approximated as

$$A_{b_2c_2} \approx \frac{-R_L}{r_{e_2}+r_{e_3}} \quad . \quad (3.18)$$

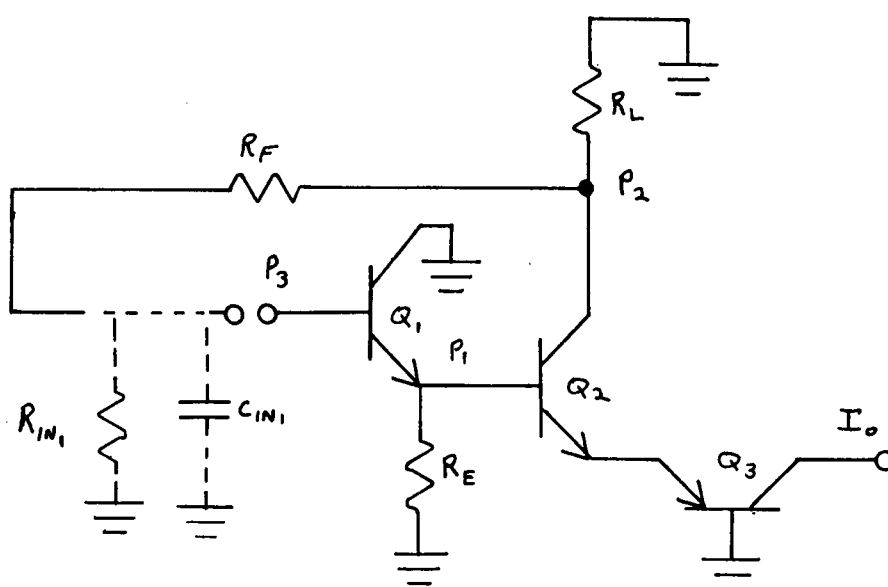


Figure 3.8. Figure 3.7c redrawn to facilitate analysis.

The midband gain from the collector of Q2 to the base of Q1 is

$$A_{c_2b_1} = \frac{R_{in_1}}{R_{in_1} + R_F}, \quad (3.19)$$

where R_{in_1} is given by Equation (3.17). The value of R_{in_1} will typically be much greater than R_F , such that $A_{c_2b_1}$ can be approximated as unity. The midband loop transmission can be approximated as

$$A\beta_{mid} \approx \frac{-R_L}{r_{e_2} + r_{e_3}}. \quad (3.20)$$

The loop transmission as approximated by Millard is

$$A\beta = \frac{-R_L}{(r_{e_2} + r_{e_3})(1 + j\omega R_F C_{in_1})}, \quad (3.21)$$

and the approximate frequency at which the loop transmission becomes unity is

$$f_{-3dB} \approx \frac{0.159}{C_{in}(r_{e_2} + r_{e_3})A_o}. \quad (3.22)$$

If good circuit layout techniques and high frequency devices are used, C_{in} can be held to the order of 2 to 6pF. If Q2 and Q3 are biased such that r_{e_2} and r_{e_3} are on the order of 5 ohms, the high-corner frequency for a gain of 10 is

$$f_{-3dB} \approx \frac{0.159}{C_{in_1}(r_{e_2} + r_{e_3})A_o} \approx \frac{0.159}{3pF(10)(10)} \approx 530MHz. \quad (3.23)$$

This value is not significantly different from that predicted for the circuit in Figure 3.7a. However, note that the loop transmission for the circuit in Figure 3.7a is significantly less than that predicted by Equation (3.13) due to the low input impedance since most high frequency transistors have relatively low beta's. A nodal analysis of the circuit in Figure 3.7c is of little value because too many assumptions are necessary to obtain a simplified equation for the frequency response. In order that both circuits be compared equally, the computer simulation program called PCAP was used. The results are presented in Chapter 4. The shunt feedback stage is incorporated in the charge loop as shown in Figure 3.9.

If the timing signal is to be driven over any length of cable, a buffer will be required to prevent loading and excessive capacitance at the collector of Q2 in Figure 3.7c. A common collector stage which can be used to minimize the loading is shown in Figure 3.10. The input resistance of Q5 is high compared to R_L , if the timing output is always terminated into a 50 load. The input resistance of Q5 is

$$R_{in5} = (\beta_5 + 1)(r_{e5} + r_{E5} || 50\Omega) \approx 1.4K\Omega \quad (3.24)$$

for a beta of 25 and a collector current of 5mA. The input capacitance is

$$C_{in} \approx C_{ob} + \frac{1}{2\pi(r_e + R_{eq})f_T} \approx 1.5pF \quad (3.25)$$

for a C_{ob} of 0.8pF and an f_T of 5GHz. The input capacitance given by

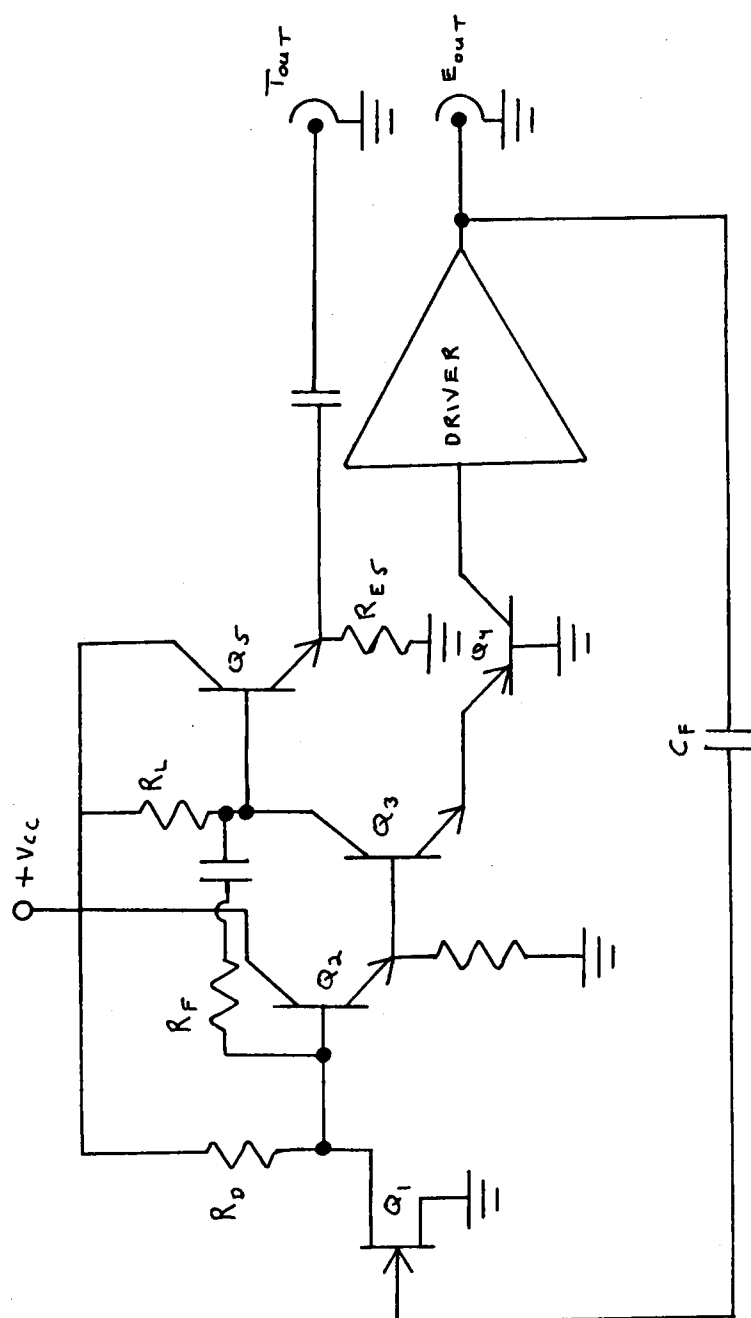
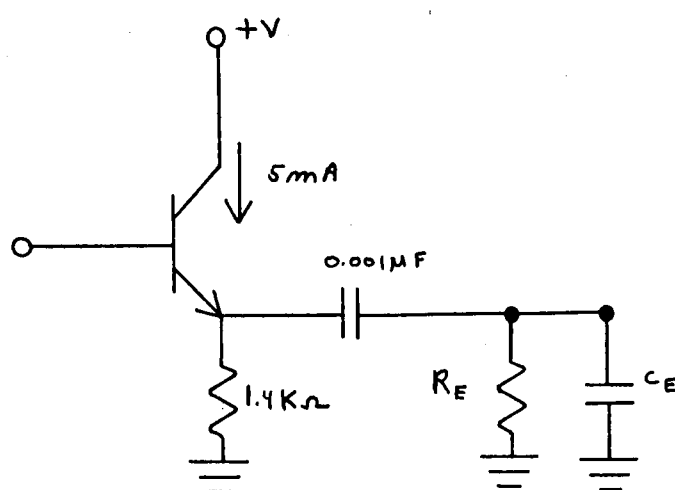


Figure 3.9. Shunt-feedback stage as incorporated in charge loop.



$$f_T = 56\text{Hz}$$

$$C_{ob} = 0.8\text{pF}$$

$$C_{be} = 6\text{pF}$$

$$r_c = 5\Omega$$

$$R_E = 50\Omega$$

$$r'_b = 50\Omega$$

$$\beta = 2.5$$

Figure 3.10. Timing output buffer.

Equation (3.25) should represent no significant loading effect on the current gain stage. However, the capacitive loading must be considered when analyzing the current gain stage for stability.

From a component point of view, the use of a common collector stage as a buffer is the simplest and most efficient. The only problem associated with this approach is the possibility of negative resistance input impedance due to capacitive loading. The circuit used to evaluate this possibility is shown in Figure 3.10. The maximum negative resistance¹⁶ is

$$N.R._{max} = r_{b'} + \frac{a_1 - \omega_m^2(a_1 b_1 - a_2 b_2)}{(1 - \omega_m^2 b_1)^2 + \omega_m^2 b_2^2}, \quad (3.25)$$

where

$$\omega_m = 2\pi f_{m(N.R.)}, \quad (3.26)$$

$$f_{m(N.R.)} \approx f_\beta [M + (M+1) \sqrt{M}]^{1/2}, \quad (3.27)$$

$$f_\beta = f_T / \beta, \quad (3.28)$$

$$M = (r_{b'} e^{C_{b'e}}) / R_E C_E, \quad (3.29)$$

$$a_1 = (\beta + 1)(r_e + R_E), \quad (3.30)$$

$$a_2 = r_{b'} e^{R_E (C_{b'e} + C_E)}, \quad (3.31)$$

$$b_1 = r_{b'} e^{R_E (C_{b'c} C_{b'e} + C_{b'c} C_E + C_{b'e} C_E)}, \quad (3.32)$$

$$b_2 = (\beta+1)(r_e + R_E) C_{b'e} + R_E C_E + r_{b'e} C_{b'e} \quad (3.33)$$

For the set of conditions in Figure 3.10, the maximum negative resistance is 12.3 ohms. This value is highly dependent upon capacitive loading. Therefore, a larger value of resistance is inserted in the base lead of the buffer transistor as shown in Figure 3.1, p. 54. The value of this resistance must be sufficiently low so as not to form an integrator network with the input capacitance of the buffer transistor. This value is

$$\tau_{in} \approx R_s (C_{ob} + C_{b'g}) \quad (3.34)$$

and R_s is the series resistance. For the circuit parameters in Figure 3.11, the value of τ_{in} is

$$\tau_{in} \approx (100)(0.8\text{pF} + 0.6\text{pF}) = 0.14\text{nsec} \quad (3.35)$$

This value is sufficiently low so that the overall risetime is not degraded noticeably.

Charge Loop

The remainder of the charge loop consists of a driver circuit which is shown in Figure 3.12. This configuration was chosen due to its simplicity and very good isolation of the dominate pole of the charge loop from loading effects. The zener diode (D1) is used for level shifting to allow roughly equal negative and positive voltage servings with good linearity. The voltage at the dominate node was

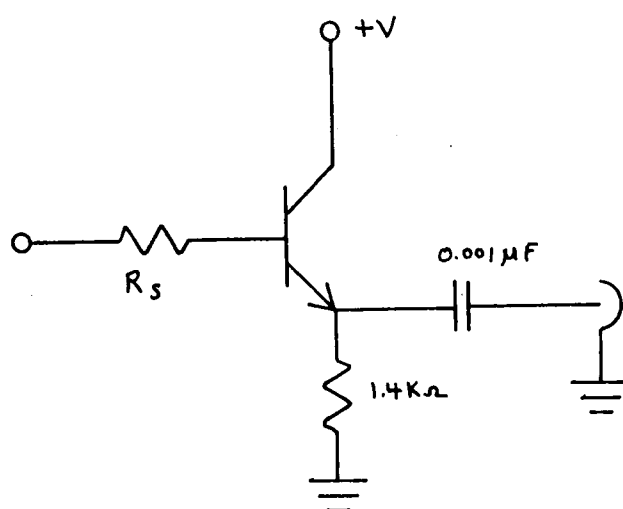


Figure 3.11. Actual timing output buffer to eliminate negative resistance oscillations.

selected so that transistor Q_{CB} had sufficient collector reverse bias on positive signal swings and transistor Q_{IS} had sufficient collector reverse bias on negative signal swings. The charge loop slew rate and drive requirements are not demanding since the design risetime is approximately 15nsec for a 100 MeV energy range. The overall circuit is shown in Figure 3.15. If the risetime of the charge loop is limited to 15nsec for detector capacitances of zero, the phase shift associated with the current gain stage composed of Q2 and Q3 can be neglected. The phase shift associated with the driver stage can not be neglected and will be examined later in this section. The midband value of the loop transmission is

$$T \approx (g_{m1})(A_i)(R_D) \frac{C_F}{C_F + C_{DET} + C_{IN}} \quad (3.36)$$

The loop transmission will have poles of interest at the emitter of Q4, the collector of Q4, the source of Q7 and the emitter of Q8. Note that for the purpose of simplicity, the loop transmission at low frequency is approximated using the capacitance values of C_f , C_{in} and C_{DET} . The low frequency loop transmission will depend upon the resistance of the detector, which is a reverse biased diode, and the feedback resistor (R_f in Figure 3.13). The pole at the emitter of Q4 is

$$\tau_{Q4} = (R_{in_{E3}} || R_{in_{E4}})(C_{in_{E3}} + C_{in_{E4}}) \quad (3.37)$$

The resistance looking into the emitter of Q3 is

$$R_{in_{E3}} \approx r_{e3}(T) \quad , \quad (3.38)$$

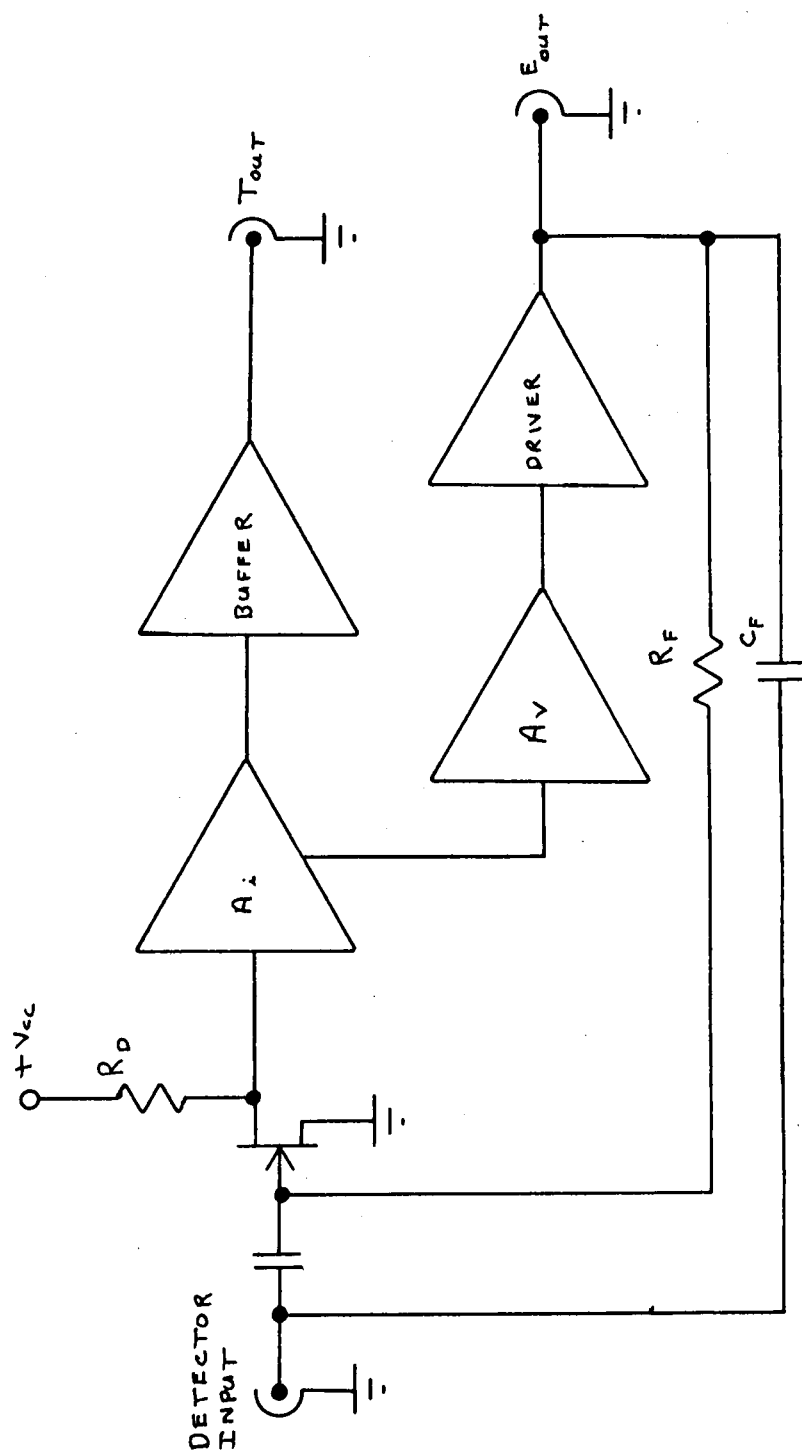


Figure 3.13. Complete preamplifier.

or

$$R_{in_{E_3}} \approx \frac{R_4 r_{e_3}}{r_{e_2} + r_{e_3}} \quad (3.39)$$

The resistance looking into the emitter of Q4 is

$$R_{in_{E_4}} \approx r_{e_4} \quad (3.40)$$

where the base is AC bypassed. The total resistance at the emitter of Q4 can be approximated as

$$R_{in_{E_3}} || R_{in_{E_4}} \approx R_{in_{E_4}} \approx r_{e_4} \quad (3.41)$$

The capacitance looking into the emitter of Q3 is

$$C_{in_{E_3}} \approx \frac{1}{2\pi \left[r_{e_3} + \frac{R_{b_3}}{\beta + 1} \right] f_T} \quad (3.42)$$

The capacitance looking into the emitter of Q1 is

$$C_{in_{E_4}} \approx C_{b'e} = \frac{1}{2\pi r_e f_T} \quad (3.43)$$

Since the f_T for Q4 is much less than that of Q3, the total capacitance at the emitter of Q3 and 4 is approximately

$$C_{in_{E_3}} + C_{in_{E_4}} \approx C_{b'e_4} \quad (3.44)$$

The time constant associated with this pole is

$$\tau_{E_4} \approx C_{b'e_4} r_{e_4} \quad (3.45)$$

The pole at the dominant node is

$$\tau_{C4} \approx (C_{OC4} + C_{IN7} + C_{OC5} + C_{DOM}) (R_{OC4} || R_{OC5} || R_{IN7} || R_{13}) \quad (3.46)$$

The output capacitance of Q4 is

$$C_{O4} \approx C_{ob4} \quad (3.47)$$

The output capacitance of Q5 is

$$C_{O5} \approx C_{ob5} \quad (3.48)$$

The input capacitance of Q7 is

$$C_{IN7} \approx C_{gd} + \frac{C_{gs}}{1 + g_m R_{Leq}} \quad (3.49)$$

The output resistance of Q4 and Q5 is

$$R_{O5,4} = \frac{(\beta+1)(r_{ce})}{1 + \frac{R_b}{R_e}} \quad (3.50)$$

The value of R_b is

$$R_b = r_b + Z_\beta \quad (3.51)$$

The value of C3 is chosen to minimize noise rather than to fully bypass the base of Q5. For the values in Figure 3.13, the impedance looking into the collector of Q4 is

$$R_{O4} = \frac{(\beta+1)(r_{ce})}{1 + R_b/R_e} \approx \frac{(201)(10K\Omega)}{1 + 1.5K\Omega/60\Omega} \approx 77.3K\Omega \quad (3.52)$$

where R_b is approximated as r_b . The impedance looking into the collector of Q5 is

$$R_{O5} \approx \frac{(\beta+1)r_{ce}}{1+R_b/r_e} \approx \frac{201(10K\Omega)}{1+2K\Omega/270\Omega} \approx 239K\Omega \quad (3.53)$$

The time constant at the dominate node can be approximated as

$$\tau_{DOM} \approx \left(C_{ob4} + C_{ob5} + C_{gd7} + \frac{C_{gs7}}{1+g_m R_{Leg7}} + C_{DOM} \right) (R_{O5} || R_{O4} || R_{IN7} || R_{13}) \quad (3.54)$$

The phase shift introduced by the complimentary output stage does not present a problem because the crossover frequency is low. However, if the crossover occurred at a higher frequency, this excess phase shift could greatly reduce the phase margin. The transfer function of the common collector buffer can be approximated as

$$A_{VD} \approx \frac{A_{MID}}{[1+s(\tau_{IN}+\tau_{OUT})]} \quad (3.55)$$

and the time constant can be approximated as

$$\tau_{\theta} \approx \tau_{IN} + \tau_{OUT} \quad (3.56)$$

The common collector input time constant is

$$\tau_{IN} \approx (R_{O7} || R_{12} || R_{IN8}) \left(C_{gs7} + C_{ob7} + \frac{1}{2\pi(r_e + r_E)f_T} \right) \quad (3.57)$$

and the output time constant is

$$\tau_{OUT} \approx (R_{OQ_8} || R_L) \left(\frac{1}{2\pi[r_e + R_b/\beta + 1]f_T} + C_L \right) \quad (3.58)$$

The overall expression for the loop transmission is approximately

$$A\beta \approx \frac{-K}{(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)} \quad (3.59)$$

where

$$f_1 = \frac{0.159}{\tau_{Q4}} \quad (3.60)$$

$$f_2 = \frac{0.159}{\tau_{DOM}} \quad (3.61)$$

and

$$f_3 = \frac{0.159}{\tau_{Q8}} \quad (3.62)$$

The value of capacitance required at the dominate node for a crossover frequency associated with the desired risetime can be approximated assuming all remaining poles are neglected. The expression for the loop transmission then becomes

$$A\beta \approx \frac{-K}{1+jf/f_2} \quad (3.63)$$

The loop transmission equation is then solved for the value of f_2 required for Equation (3.59) to equal unity at the desired frequency. The time constant at the dominate node can then be found by

$$\tau_{\text{DOM}} = \frac{0.159}{f_2} \quad (3.64)$$

The total capacitance required at the dominate node required to satisfy Equation (3.63) can be determined by

$$C_{\text{DOM}} = \frac{\tau_{\text{DOM}}}{R_{O5} || R_{O4} || R_{IN7} || R_{13}} \quad (3.65)$$

The value of the capacitor (C_c) required to compensate the circuit can then be determined by

$$C_c = C_{\text{DOM}} - \left(C_{ob4} + C_{ob5} + C_{gd7} + \frac{C_{gs7}}{1 + g_m R_{Leq7}} \right) \quad (3.66)$$

For the devices and bias condition in Figure 3.14, the time constants are as follows:

$$\tau_{E4} \approx (C_{b'e4})(r_{e4}) = (122\text{pF})(5.2\Omega) \approx 0.634\text{nsec} \quad (3.67)$$

$$\begin{aligned} \tau_{C4} = \tau_{\text{DOM}} &= \left(C_{ob4} + C_{ob5} + C_{gd7} + \frac{C_{gs7}}{1 + g_m R_{eq7}} \right) (R_{O5} || R_{O4} || R_{13} || R_{IN7}) \\ &= (4\text{pF} + 4.5\text{pF} + 0.8\text{pF}) (239\text{K}\Omega || 77.3\text{K}\Omega || 1.5\text{M}\Omega || \infty) = 0.523\mu\text{sec} \end{aligned} \quad (3.68)$$

and

$$\tau_{Q8} = 2.2\text{nsec} + 0.6\text{nsec} = 2.8\text{nsec} \quad (3.69)$$

For the devices in Figure 3.13 and C_{DET} equal to zero,

$$C_{\text{IN}} = C_{gs} + C_{gd} (1 - A_{VT}) + C_{\text{STRAY}} = 14\text{pF} + 9\text{pF} + 2\text{pF} = 25\text{pF} \quad (3.70)$$

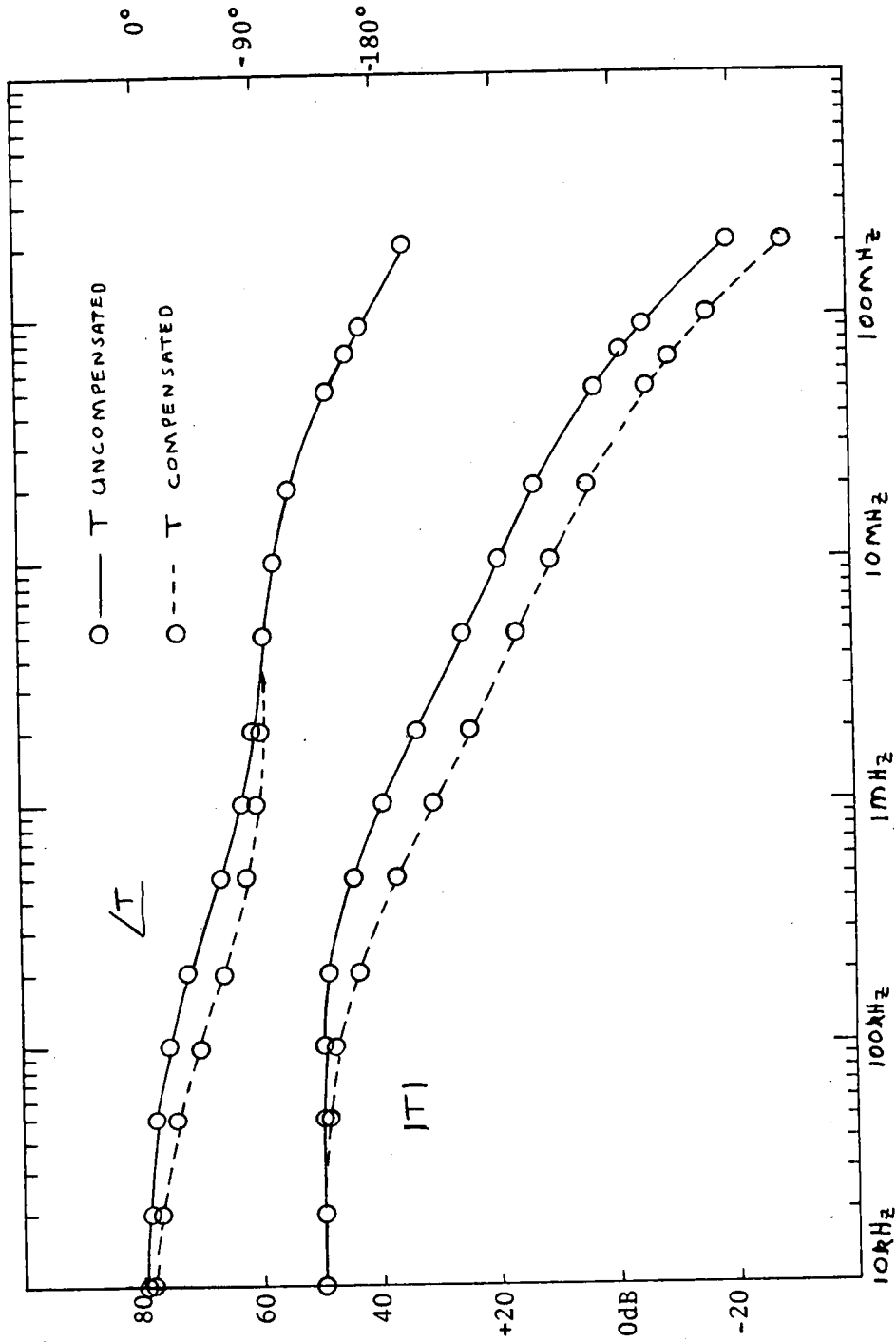


Figure 3.14. Loop transmission of charge loop.

$$R_D \approx R_{O5} || R_{O4} || R_{13} \approx 56.2K\Omega \quad , \quad (3.71)$$

$$A_i = \frac{R_L + R_F}{R_L} \approx \frac{750 + 120}{120} \approx 7.25 \quad , \quad (3.72)$$

$$g_m \approx 20m\Omega \quad , \quad (3.73)$$

and

$$\begin{aligned} T_{m1D} &\approx -(g_m)(A_i)(R_D) \frac{C_F}{C_{IN} + C_{DET} + C_F} \\ &= (20 \times 10^{-3})(7.25)(56.2K\Omega) \frac{1pF}{26pF} = -326 \quad , \quad (3.74) \end{aligned}$$

As shown in Figure 3.14 and Table 3.3, the loop transmission can be approximated as

$$T = \frac{-326}{(1 + jf/251MHz)(1 + jf/304kHz)(1 + jf/56.8MHz)} \quad , \quad (3.75)$$

Note that Equation (3.75) does not include the phase shift due to the current gain stage or the excess phase shift due to the common collector output. The frequency at which T is equal to unity is approximately 64MHz and the phase margin is approximately 27° as obtained from Figure 3.14. While this system is stable with no addition compensation, the overshoot would be appreciable and the risetime much less than desired. The crossover frequency can be reduced by increasing the capacitance at the dominate node and lowering the frequency of the dominate pole. The desired value of risetime is 15nsec and the overshoot should be 20% or less, with a phase margin of 50 degrees or

TABLE 3.3
UNCOMPENSATED LOOP TRANSMISSION OF CHARGE LOOP

F	T	$\angle T^\circ$
10kHz	50.3 dB	- 1.9
20kHz	50.2 dB	- 3.8
50kHz	50.1 dB	- 9.4
100kHz	49.8 dB	- 18.3
200kHz	48.7 dB	- 33.6
500kHz	44.6 dB	- 59.3
1MHz	39.5 dB	- 74.3
2MHz	33.8 dB	- 84.0
5MHz	25.9 dB	- 92.7
10MHz	19.8 dB	-101
20MHz	13.4 dB	-113
50MHz	3.3 dB	-142
60MHz	0.863dB	-150
70MHz	- 1.32 dB	-156
80MHz	- 3.31 dB	-162
90MHz	- 5.14 dB	-167
100MHz	- 6.8 dB	-172
200MHz	-19.5 dB	-203

NOTE: $T = \frac{-326}{(1 + jf/251\text{MHz})(1 + jf/304\text{kHz})(1 + jf/56.8\text{MHz})}$

greater. Based on these values, the crossover frequency should be 23.3MHz and the dominate pole should occur at 71.5kHz. However, to achieve the risetime of 15nsec, a design goal of 10nsec was chosen. This goal will allow for variations in capacitance and resistance at the dominate node along with changes in the stray capacitance at the input. A crossover frequency occurs at 35MHz when the dominate pole occurs at 107kHz. A compensating capacitance of 15pF lowers the dominate pole to 108kHz. The expression for the compensated loop transmission is

$$T_C = \frac{-326}{(1 + jf/251\text{MHz})(1 + jf/108\text{kHz})(1 + jf/56.8\text{MHz})} \quad (3.76)$$

The Bode plot of Equation (3.76) is shown in Figure 3.14 and the data points are given in Table 3.4. The crossover frequency is 30MHz and the phase margin is 54°. A crossover frequency of 30MHz will yield a risetime of 8nsec and 10% overshoot. A risetime of 8nsec is significantly less than the 15nsec design goal and is chosen to insure all production units will meet the risetime specification with nominal parameter variations. The slew rate is limited in the negative direction by the current set by the current source. This value is nominally 5mA. The total capacitance at the dominate node is approximately 25pF. For the above values, the negative slew rate is 200V/μsec. The low negative slew rate will degrade the negative risetime for certain values of detector capacitance and energy levels. The low negative slew rate is acceptable because positive output signals are obtained in the majority of the applications. The degradation is present only for very high

TABLE 3.4
COMPENSATED LOOP TRANSMISSION OF CHARGE LOOP

F	T	$\angle T^\circ$
10kHz	50.2 dB	- 5.3°
20kHz	50.1 dB	- 10.5°
50kHz	49.4 dB	- 25 °
100kHz	47.6 dB	- 43 °
200kHz	43.8 dB	- 62 °
500kHz	36.8 dB	- 78.4°
1MHz	31 dB	- 85 °
2MHz	25 dB	- 89 °
5MHz	16.9 dB	- 95 °
10MHz	10.8 dB	-102 °
20MHz	4.38dB	-114 °
30MHz	0.26dB	-124 °
40MHz	- 3 dB	-134 °
50MHz	- 5.71dB	-143 °
100MHz	-15.8 dB	-172 °
200MHz	-28.5 dB	-203 °

NOTE:

$$T = \frac{-326}{(1 + jf/251\text{MHz})(1 + jf/108\text{kHz})(1 + jf/56.8\text{MHz})}$$

$$C_{\text{DOM}} = 4\text{pF} + 4.5\text{pF} + 0.81\text{pF} + 15\text{pF} + 2\text{pF}_{\text{STRAY}}$$

$$R_{\text{DOM}} = 56.2\text{K}\Omega$$

energies and low capacitance detectors. Detectors used for timing are generally not low capacitance as detector thickness is minimized to reduce the detector charge collection time.

Two important parameters in the design of a charge sensitive preamplifier are the dynamic input capacitance (C_{DY}) and the integral nonlinearity. The dynamic input capacitance can be derived using the model in Figure 3.15. The loop equations are

$$V_S = I_1(Z_1 + Z_I) - I_F Z_I \quad (3.77)$$

and

$$0 = I_1 Z_1 (1+A) + I_F [Z_F + (1+A)Z_I] \quad (3.78)$$

Solving for the input impedance as seen by the voltage source (V_S)

$$\frac{V_S}{I_1} = Z_{INS} = Z_1 + \frac{Z_I Z_F}{Z_F + (1+A)Z_I} \quad (3.79)$$

If Z_1 is zero, Equation (3.79) becomes

$$Z_{IN} + \frac{Z_I Z_F}{Z_F + (1+A)Z_I} \quad (3.80)$$

and can be represented as an admittance, Y_{in} , where

$$Y_{IN} = \frac{1}{Z_{IN}} = \frac{1}{Z_I} + \frac{(1+A)}{Z_F} \quad (3.81)$$

This expression for the input admittance clearly separates the components of the input impedance. If the impedance Z_I is high, Equation (3.80) can be approximated as

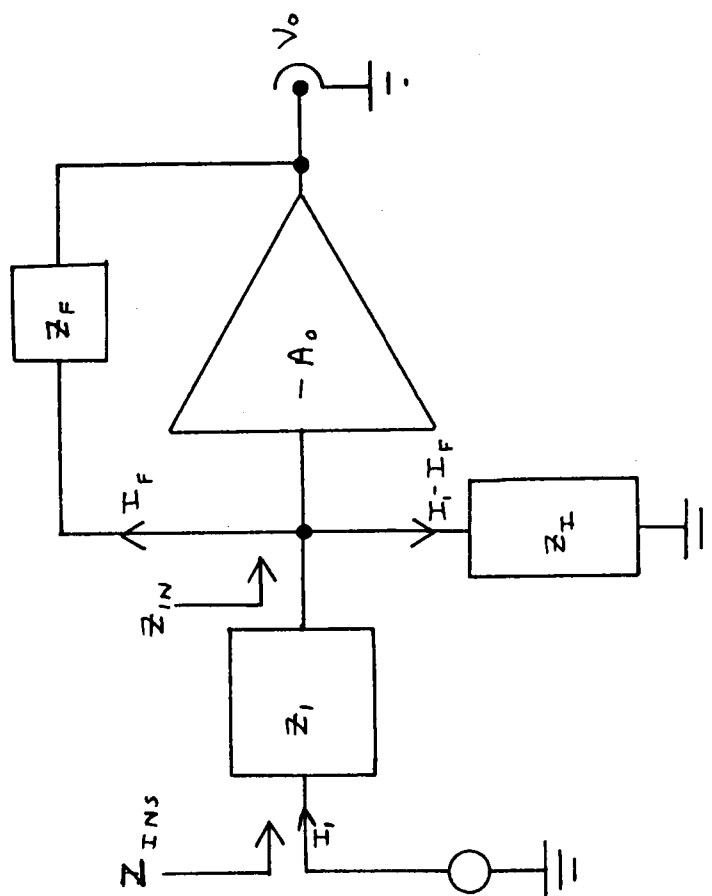


Figure 3.15. Circuit used to derive dynamic input capacitance

$$Z_{IN} \approx \frac{Z_F}{1+A} \quad , \quad (3.82)$$

where

$$Z_F = \left| \frac{1}{C_F \omega} \right| \quad , \quad (3.83)$$

and

$$Z_{IN} = \left| \frac{1}{C_F(1+A)\omega} \right| \quad . \quad (3.84)$$

From Equation (3.84) the dynamic input capacitance is

$$C_{DY} = (1+A)C_F \quad . \quad (3.85)$$

The dynamic input capacitance specification is of importance when detectors having large values of capacitance are used. The input charge will divide between the dynamic input capacitance and the capacitance of the detector as shown in Figure 3.16. The net result will be a decrease in the signal-to-noise ratio as detector capacitance increases. The theoretical dynamic input capacitance at a shaping time of 2μsec is

$$C_{DY2\mu\text{sec}} = C_f(A_{02\mu\text{sec}}) = 8150\text{pF} \quad . \quad (3.86)$$

The integral nonlinearity of an ac-coupled charge sensitive preamplifier contributes to line width (FWHM) as a function of output voltage. This nonlinearity, or distortion, can be produced by several sources. One dominate source is the impedance variation at the dominate node as a function of output voltage.

Any gain variations inside the loop are divided by the loop transmission. Therefore, to minimize nonlinearities, the loop

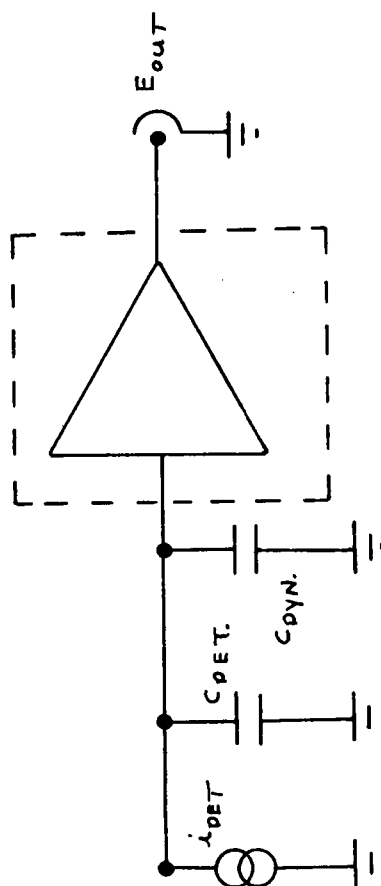


Figure 3.16. Effective location of dynamic input capacitance.

transmission must be maximized. Since this preamplifier is designed to operate with time constants from $10\mu\text{sec}$ to $0.5\mu\text{sec}$ (center frequencies from approximately 30kHz to 350kHz), the loop transmission can be maximized with a change in the closed loop response of the current gain stage. By increasing the loop transmission, the dynamic input capacitance will be increased as shown by Equation (3.86). The current gain stage can be redrawn as shown in Figure 3.17 where

$$A_i = \frac{Z_1 + Z_2}{Z_2} \quad , \quad (3.87)$$

$$Z_1 = R_1 + \frac{1}{C_1 S} \quad , \quad (3.88)$$

and

$$Z_2 = R_2 \quad . \quad (3.89)$$

The current gain is then

$$A_i = \frac{R_1 + R_2}{R_2} \left[\frac{S + 1/(R_1 C_1 + R_2 C_1)}{S} \right] \quad . \quad (3.90)$$

This equation has a pole at the origin and a zero at

$$f_z = \frac{1}{2\pi(R_1 C_1 + R_2 C_1)} \quad . \quad (3.91)$$

The effect of the compensation is shown in Figure 3.18 and Table 3.5 for values of C_1 equal to $0.01\mu\text{F}$, $0.0047\mu\text{F}$, 1000pF , and 200pF . Expressions for the loop transmission for various values of C_1 , as follows:

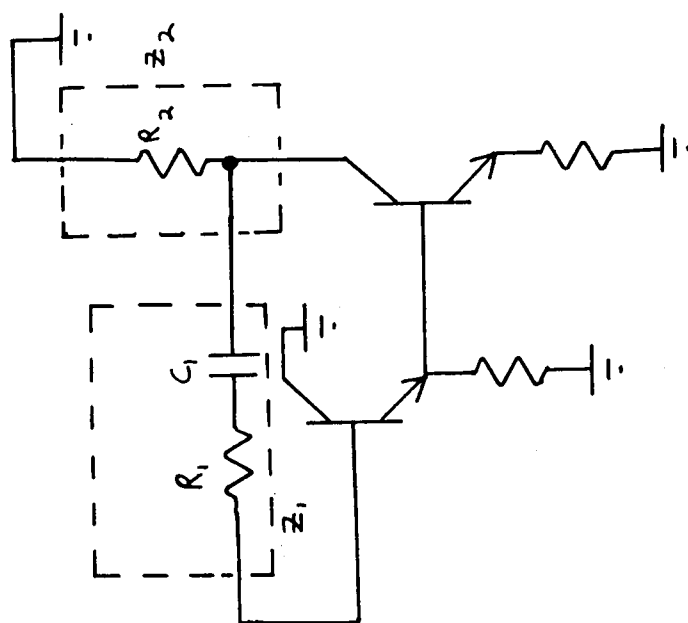


Figure 3.17. Compensation used to increase midband loop transmission.

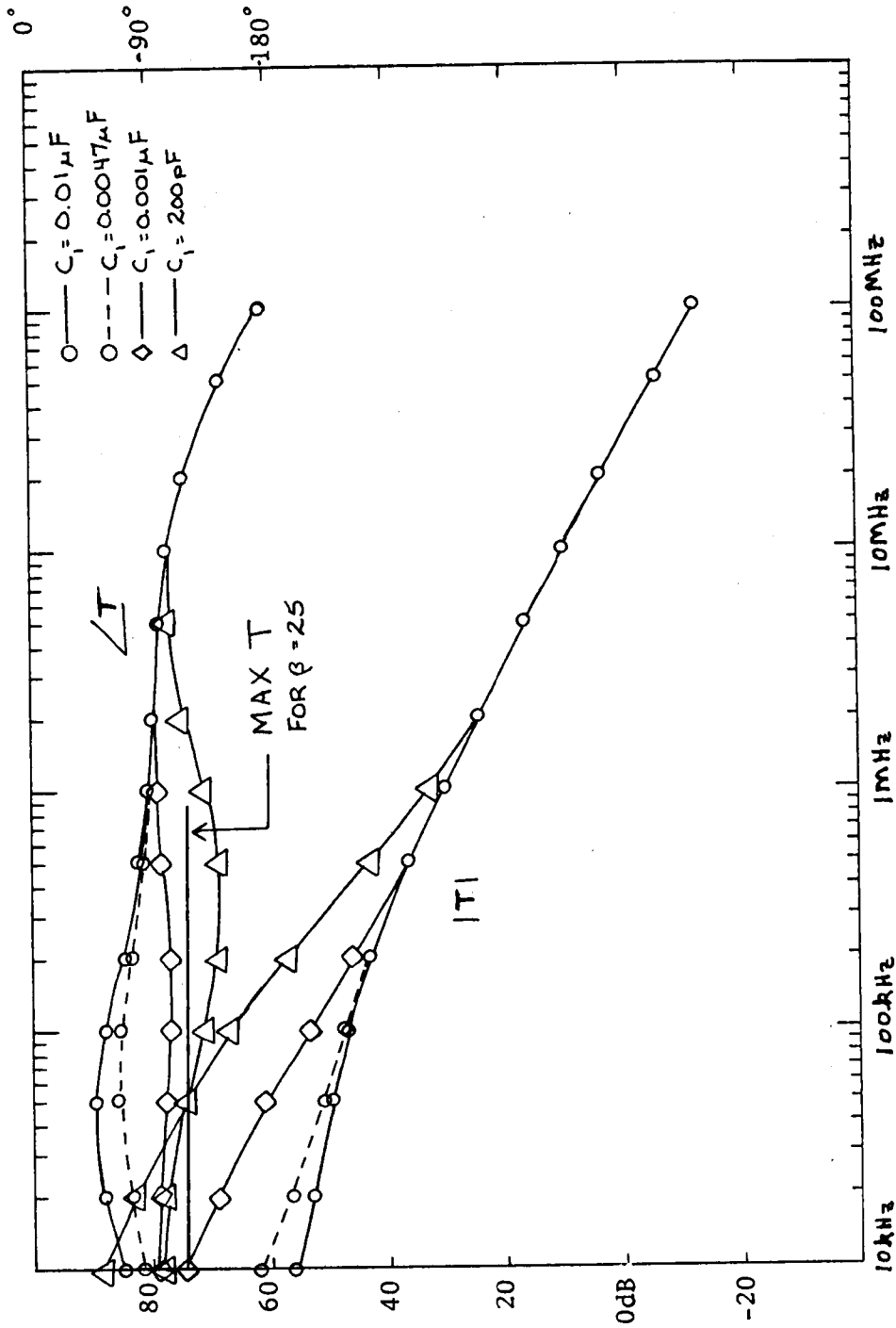


Figure 3.18. Charge loop, loop transmission as a function of C_1 .

TABLE 3.5
LOOP TRANSMISSION OF CHARGE LOOP AS A FUNCTION OF C_1

f	$C_1=0.01\mu\text{F}$			$C_1=0.0047\mu\text{F}$			$C_1=0.001\mu\text{F}$			$C_1=200\text{pF}$		
	T	LT		T	LT		T	LT		T	LT	
10kHz	56.3 dB	- 66.6°		62 dB	- 80.9°		75.1 dB	- 92.2°		89.1 dB	- 95°	
20kHz	52.4 dB	- 52.9°		56.6 dB	- 73.3°		69.1 dB	- 94.3°		83 dB	- 99.3°	
50kHz	49.6 dB	- 45°		51.1 dB	- 63°		60.7 dB	- 99.6°		74.3 dB	- 112°	
100kHz	47.4 dB	- 53.3°		47.9 dB	- 64.2°		53.6 dB	- 104°		66.5 dB	- 127°	
200kHz	43.5 dB	- 67.1°		43.6 dB	- 73°		46.1 dB	- 104°		56.9 dB	- 140°	
500kHz	36.4 dB	- 80.5°		36.4 dB	- 83°		37 dB	- 98.5°		42.8 dB	- 140°	
1MHz	30.5 dB	- 86.1°		30.6 dB	- 87.3°		30.7 dB	- 95.4°		33.2 dB	- 128°	
2MHz	24.6 dB	- 90°		24.6 dB	- 90.5°		24.6 dB	- 94.6°		25.4 dB	- 114°	
5MHz	16.6 dB	- 95.1°		16.6 dB	- 95.4°		16.6 dB	- 97°		16.7 dB	- 105°	
10MHz	10.5 dB	- 102°		10.5 dB	- 102°		10.5 dB	- 103°		10.5 dB	- 107°	
20MHz	4.04dB	- 114°		4.04dB	- 114°		4.04dB	- 114°		4.06dB	- 116°	
50MHz	- 6.04dB	- 143°		- 6.04dB	- 143°		- 6.04dB	- 143°		- 6.04dB	- 144°	
100MHz	- 16.2 dB	- 172°		- 16.2 dB	- 172°		- 16.2 dB	- 172°		- 16.2 dB	- 173°	

for C_1 equal to $0.01\mu\text{F}$,

$$T = \frac{-5.734 \times 10^6 (1+jf/18.29\text{kHz})}{jf[(1+jf/251\text{MHz})(1+jf/108\text{kHz})(1+jf/56.8\text{MHz})]} ; \quad (3.92)$$

for C_1 equal to $0.047\mu\text{F}$,

$$T = \frac{-1.22 \times 10^7 (1+jf/38.9\text{kHz})}{jf[(1+jf/251\text{MHz})(1+jf/108\text{kHz})(1+jf/56.8\text{MHz})]} ; \quad (3.93)$$

for C_1 equal to $0.0001\mu\text{F}$,

$$T = \frac{-5.734 \times 10^7 (1+jf/183\text{kHz})}{jf[(1+jf/251\text{MHz})(1+jf/108\text{kHz})(1+jf/56.8\text{MHz})]} ; \quad (3.94)$$

and for C_1 equal to 200pF ,

$$T = \frac{-2.87 \times 10^8 (1+jf/914\text{kHz})}{jf[(1+jf/251\text{MHz})(1+jf/108\text{kHz})(1+jf/56.8\text{MHz})]} . \quad (3.95)$$

As shown in Figure 3.18, the most suitable value of C_1 is $0.001\mu\text{F}$ due to the phase shift characteristic. The loop transmission is higher for C_1 equal to 200pF . However, if the dominate pole occurs at a lower frequency and if the detector capacitance is very large, the phase shift may approach 180° at a frequency below 1MHz . The value of C_{DY} at $2\mu\text{sec}$ is approximately $17,400\text{pF}$ for C_1 equal to $0.001\mu\text{F}$.

The time pick-off circuit is shown in Figure 3.19. The value of T_{MID} is

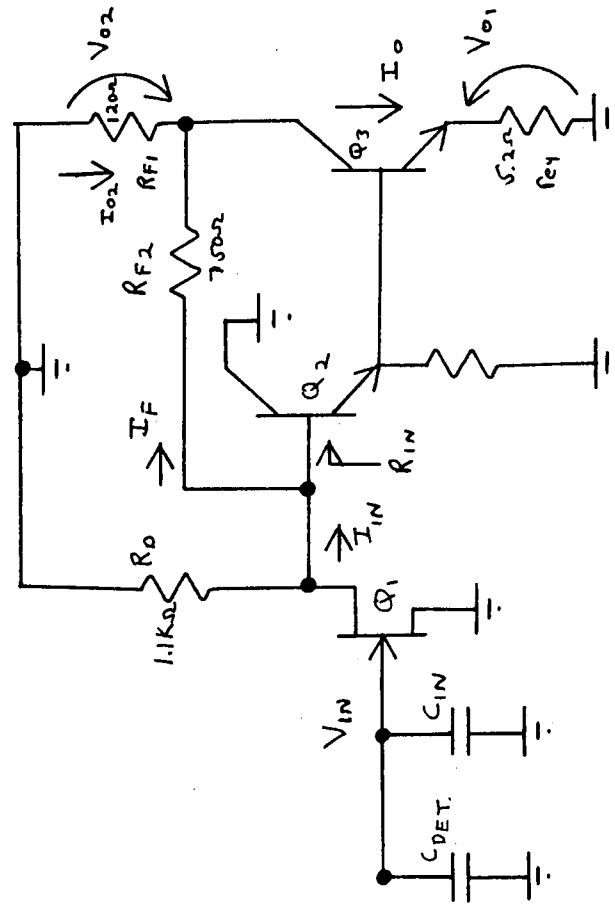


Figure 3.19. Circuit used to determine actual timing gain.

$$T_{MID} \approx \left(\frac{R_{F1}}{r_{e3} + r_{e4}} \right) \left(\frac{R_D || R_{IN}}{R_D || R_{IN} + R_{F2}} \right) \quad (3.96)$$

The value of the closed loop gain for the shunt feedback stage is

$$\frac{I_o}{I_g} = \frac{R_{F1} + R_{F2}}{R_{F1}} \frac{|T|}{1 + |T|} \approx 6.25, \quad (3.97)$$

which is slightly less than predicted by Equation (3.7). The value of V_{o1} is

$$V_{o1} = I_o r_{e4}, \quad (3.98)$$

while the value of I_{o2} is

$$I_{o2} \approx \frac{R_{F2}}{R_{F1}} I_F \quad (3.99)$$

and the timing output voltage (V_{o2}) is

$$V_{o2} = I_F \left(\frac{R_{F2}}{R_{F1}} \right) R_{F1} = I_F R_{F2} \quad (3.100)$$

If all the signal current is assumed to flow into the shunt-feedback stage, the voltage gain from the gate of the FET to the collector of Q3 is

$$\frac{V_{o2}}{V_{IN}} \approx -g_m R_{F2} \quad (3.101)$$

The actual gain will be lower than that predicted by Equation (3.101) because the current division and low loop transmission and may be as low as 11.6. To be more useful, the timing gain should be converted to a

voltage out for a given input energy as a function of detector capacitance. For a voltage gain of 11.6, the timing conversion gain can be expressed as

$$V_{o2} = \frac{-510\text{mV}(E_{IN})}{C_{DET} + C_{STRAY} + C_{IN}} \quad , \quad (3.102)$$

where E_{IN} is the energy in MeV, and $C_{DET} + C_{STRAY} + C_{IN}$ is the total in picofarads.

The high frequency loop transmission of the shunt feedback stage can be approximated by

$$T = \left(\frac{R_{F1}}{r_{e3} + r_{e4}} \right) \left(\frac{R_D || R_{IN}}{R_D || R_{IN} + R_{F2}} \right) \left(\frac{1}{1 + jf/f_1} \right) \quad , \quad (3.103)$$

where f_1 is

$$f_1 = \frac{0.159}{(C_{gd} + C_{ob2})(R_D || (R_{F2} + R_{F1})) || R_{IN2}} \quad . \quad (3.104)$$

For the devices used in Figure 3.19, the loop transmission is

$$T = \frac{-6.32}{(1 + jf/84\text{MHz})} \quad , \quad (3.105)$$

and the Bode plot is shown in Figure 3.20.

The crossover frequency is approximately 540MHz and the phase margin is approximately 90°. This will yield a risetime of 650psec. However, these results are optimistic and will be investigated using PCAP (Chapter 4). The total risetime for the timing signal using the

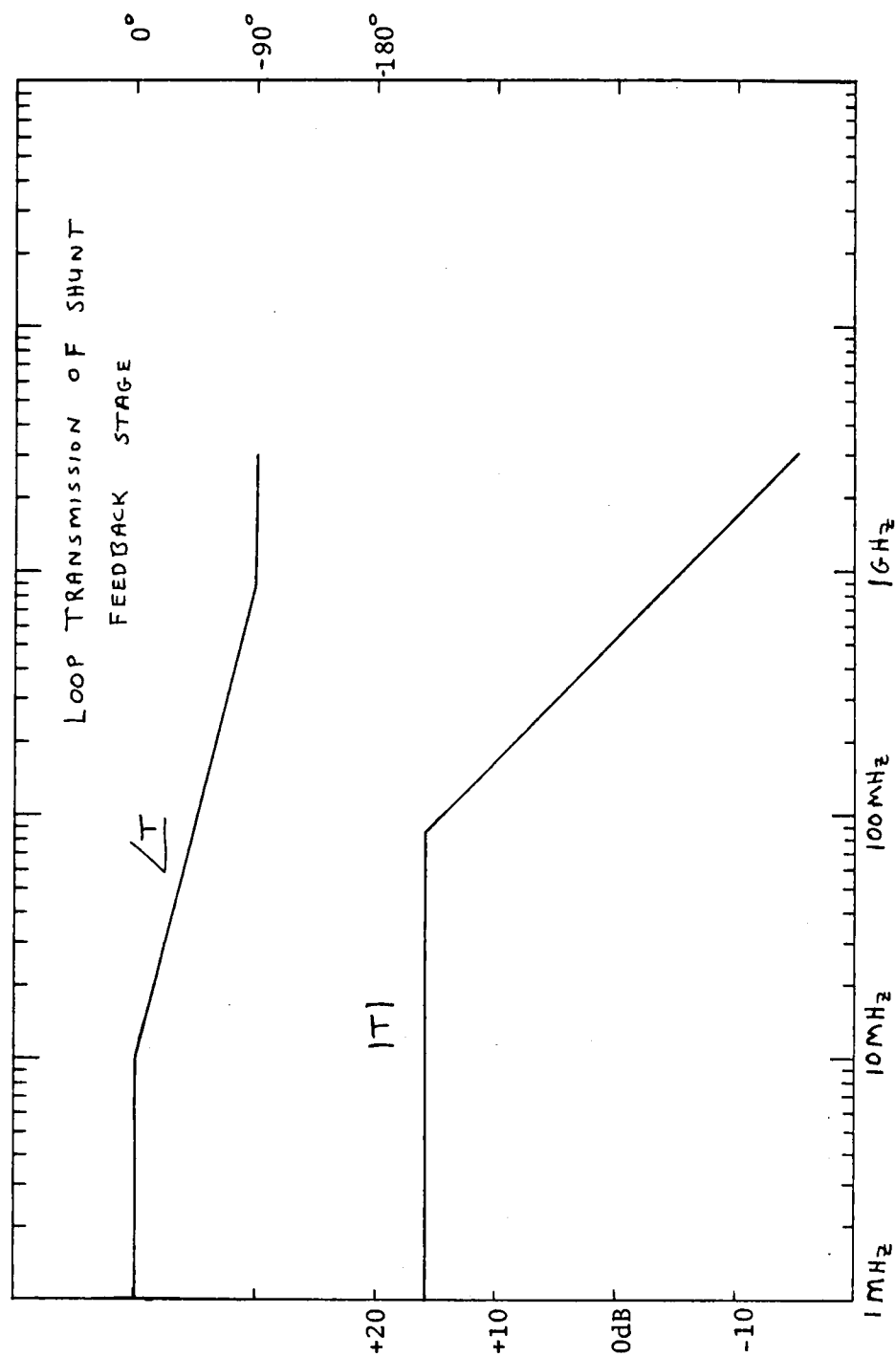


Figure 3.20. Loop transmission of shunt feedback stage.

2N4393 FET is

$$\tau_{rTOUT} = \sqrt{\tau_{rFET}^2 + \tau_{rSHUNT-FEEDBACK}^2} = 775 \text{psec} \quad (3.106)$$

Minimum degradation is expected from the common-collector buffer if hybrid construction is used to minimize strays and a device is used with an f_T in the several GHz range.

Noise Analysis

The basic noise analysis was covered in Chapter 2. However, the second stage noise contribution will now be examined. The noise model for the bipolar transistor¹⁷ is shown in Figure 3.21 where

$$\overline{e_x^2} = 4KTr_x \quad , \quad (3.107)$$

$$\overline{i_b^2} = 2eI_B \quad , \quad (3.108)$$

$$\overline{i_c^2} = 2eI_C \quad , \quad (3.109)$$

$$\overline{i_e^2} = \frac{4KT}{R_E} \quad , \quad (3.110)$$

and

$$\overline{e_b^2} = 4KTr_b \quad . \quad (3.111)$$

The total noise current referred to the collector is

$$\overline{i_{cn}^2} = \frac{\beta^2(\overline{e_x^2}) + \beta^2\overline{e_b^2} + \overline{i_b^2}(R_b + r_x + R_e)^2 + (R_b + r_x + r_\pi + R_e)^2\overline{i_c^2} + \beta^2 R_E^2 \overline{i_e^2}}{[R_b + r_\pi + r_x + (\beta+1)R_e]^2} \quad . \quad (3.112)$$

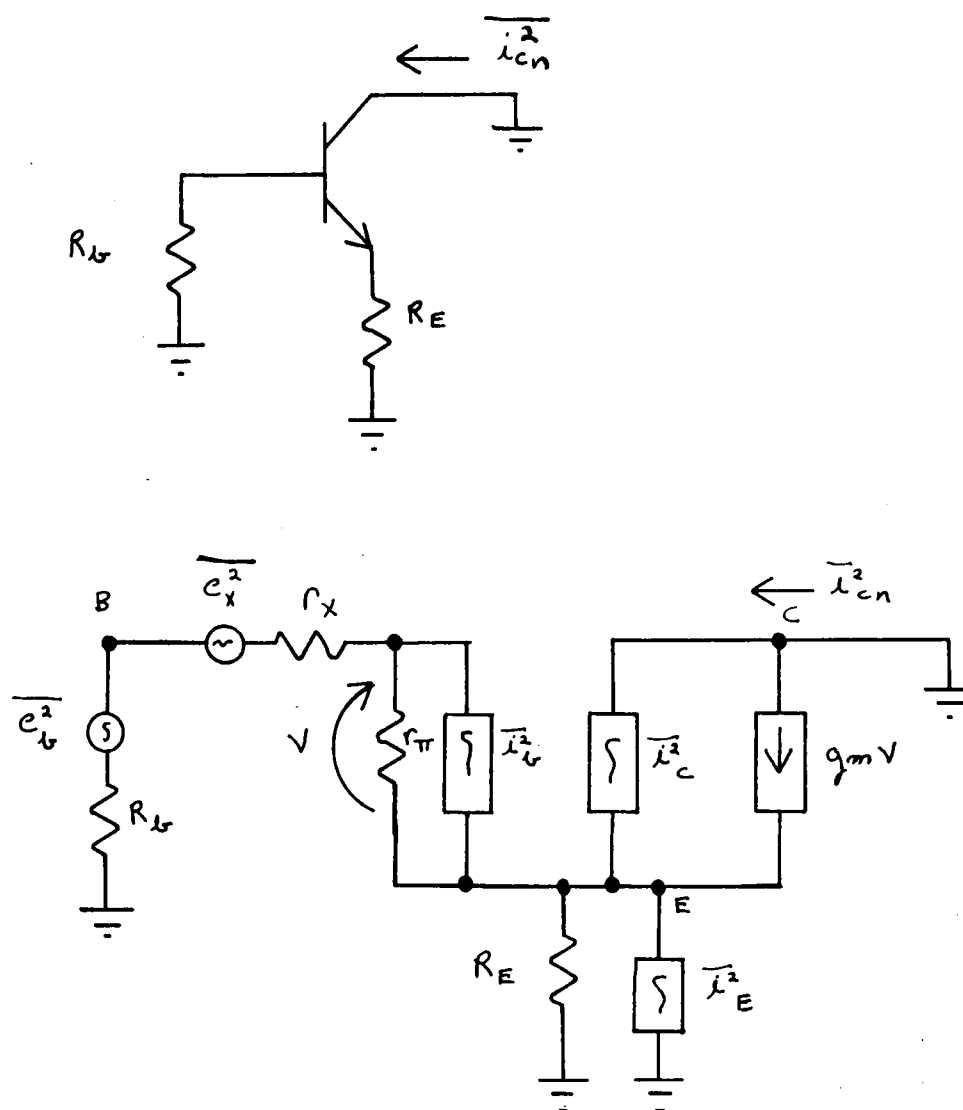


Figure 3.21. (a) Bipolar transistor configuration;
(b) Hybrid π noise model.

The noise model for the second stage is shown in Figure 3.22. The noise contribution from R_D and R_F are considered separate from the contribution of the active devices comprising the second stage. The equivalent second stage input noise current due to Q_1 is

$$\overline{i_{eq}^2}|_{Q_1} = \frac{\overline{e_b^2} + \overline{e_{x_1}^2} + \overline{i_{b_1}^2} (r_x + R_b + R_e)^2 + (r_x + R_b + r_\pi + R_e) \frac{\overline{i_c^2}}{\beta^2} + R_E^2 \overline{i_e^2} K^2}{[R_b + r_x + r_\pi + (\beta + 1)R_e]^2} \quad \text{A}^2/\text{Hz} \quad (3.113)$$

where R_e is

$$R_e = R_E || R_{IN_2} \quad , \quad (3.114)$$

and K is a current division term due to loading of the second stage

$$K = \frac{R_{IN_2}}{R_{IN_2} + R_E} \quad . \quad (3.115)$$

The noise contribution of the second transistor can be neglected since its contribution will be reduced by Beta. The output noise current is

$$\overline{i_o^2} = \overline{A_i^2} \left(\overline{i_{eq_1}^2} + \frac{4KT}{R_D} + \frac{4KT R_F}{(R_F + Z_{CF})^2} \right) \quad \text{A}^2/\text{Hz} \quad (3.116)$$

The noise current contribution of R_F is altered due to the series impedance of C_F , because X_C is not negligible at frequencies of interest for the charge loop. The effect of the impedance of C_F will result in two approximations, one for the charge loop and one for the timing loop. The output noise current for very high frequencies (timing loop) is

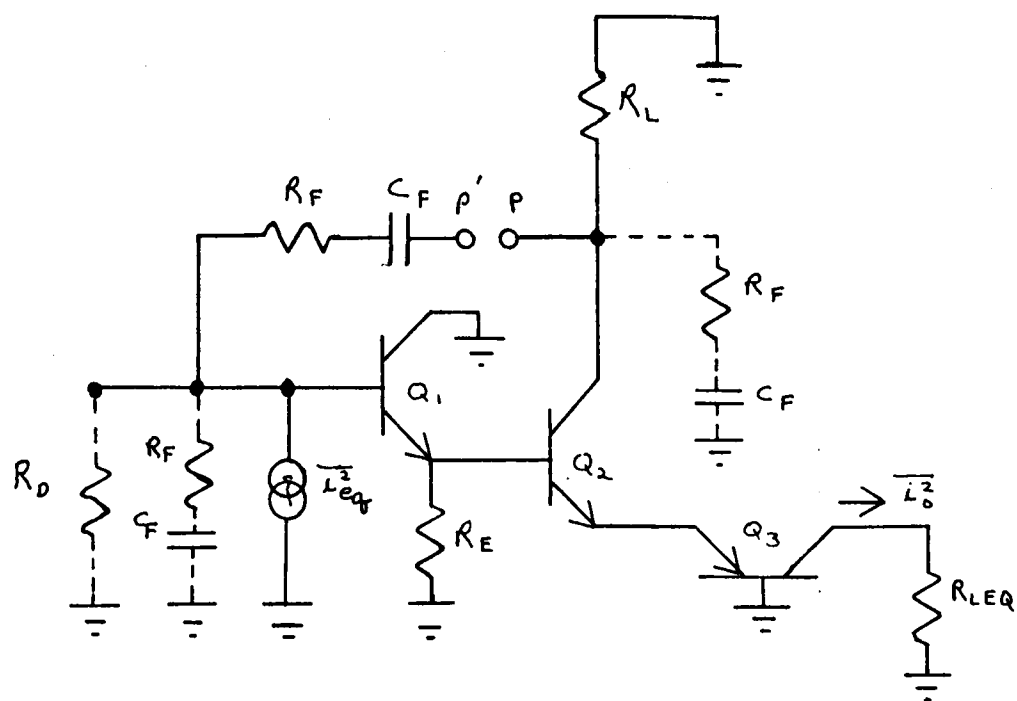
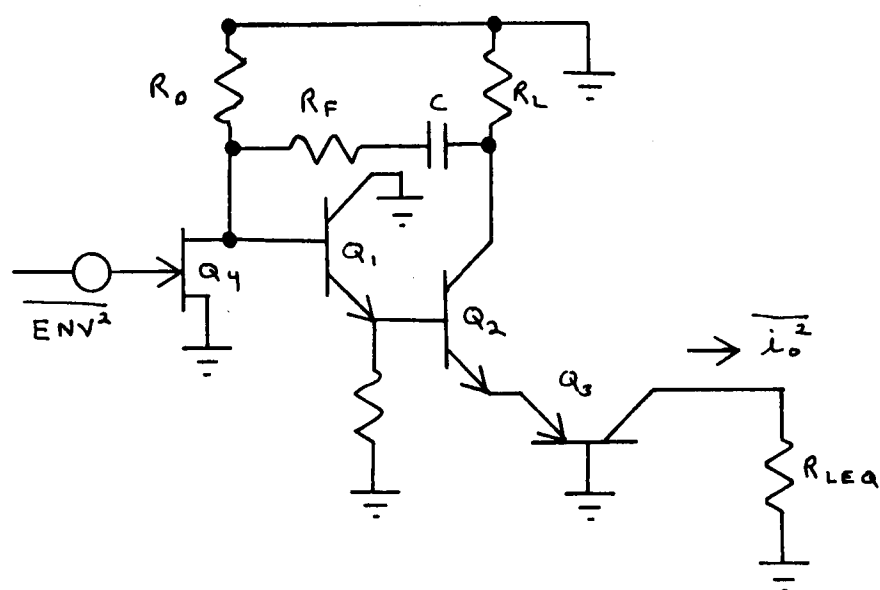


Figure 3.22. (a) Circuit used to find $\overline{ENV^2}$;
(b) Circuit used to find i_{eq}^2 .

$$\overline{i_{OT}^2} = A_{iT}^2 \left(\overline{i_{eq1}^2} + 4KT \left(\frac{1}{R_D} + \frac{1}{R_F} \right) \right) A^2/\text{Hz} \quad (3.117)$$

This noise current can be referred to the input as a series noise voltage by dividing the output noise current by the gain from the input.

For the charge loop,

$$\overline{ENV^2}_{\text{QLOOP 2nd STAGE}} = \frac{\overline{i_{eq1}^2} + \frac{4KT}{R_D} + \frac{4KTR_F}{(R_F + |Z_{CF}|)^2}}{gm^2} V^2/\text{Hz} \quad (3.118A)$$

and for the timing loop,

$$\overline{ENV^2}_{\text{TLOOP 2nd STAGE}} = \frac{\overline{i_{eq1}^2} + 4KT \left(\frac{1}{R_D} + \frac{1}{R_F} \right)}{gm^2} V^2/\text{Hz} \quad (3.118B)$$

The equivalent input noise voltage of the FET is

$$\overline{ENV^2}_{\text{FET}} = \frac{8}{3} \frac{KT}{gm} V^2/\text{Hz} \quad (3.119)$$

The total equivalent input noise voltage for the charge loop is

$$\overline{ENV^2}_{\text{QLOOP}} = \frac{8}{3} \frac{KT}{gm} + \frac{\overline{i_{eq1}^2} + \frac{4KT}{R_D} + \frac{4KTR_F}{(R_F + |Z_{CF}|)^2}}{gm^2} V^2/\text{Hz} \quad (3.120)$$

and for the timing loop

$$\overline{ENV^2}_{\text{TLOOP}} = \frac{8KT}{3gm} + \frac{\overline{i_{eq1}^2} + 4KT \left(\frac{1}{R_D} + \frac{1}{R_F} \right)}{gm^2} V^2/\text{Hz} \quad (3.121)$$

The equivalent input noise current ($\overline{ENI^2}$) is given by Equation (2.13). Using the equations developed for the equivalent input noise voltage and equivalent input current, the noise performance can be calculated as outlined in Chapter 2. The circuit diagram and necessary data for the noise analysis are given in Figure 3.13, p. 79. Based on these parameters, the charge loop equivalent input noise voltage is $5.975 \times 10^{-19} \text{V}^2/\text{Hz}$. The FET contribution is $5.52 \times 10^{-19} \text{V}^2/\text{Hz}$. The noise resistance can be divided into two parts

$$R_{NS_{\text{LOOP}}} = R_{N_{\text{FET}}} + R_{N_{\text{2nd STAGE}}} \quad (3.122)$$

The total series noise resistance is 36.1Ω and the second stage contribution is 2.75Ω . The second stage contribution is slightly more than 7.5% of the total.

The equivalent input noise voltage for the timing loop is slightly more since the impedance of the compensation capacitor in the second stage will be negligible. The total equivalent input noise voltage is $6.478 \times 10^{-19} \text{V}^2/\text{Hz}$. The FET contribution is $5.52 \times 10^{-19} \text{V}^2/\text{Hz}$. The total series noise resistance for the timing section is 39.12Ω and the second stage contribution is 5.78Ω . The second stage contribution is approximately 15% of the total. The total equivalent input noise current is unchanged from that found in Chapter 2.

The N.L.W. can be found using the same approach as in Chapter 2, except C_{IN} is 25pF. The results are shown in Table 3.6 and Figure 3.23.

TABLE 3.6
THEORETICAL N.L.W.

C_{DET}	$\tau_{\text{OPT}} \backslash \tau_s$	0.5 μsec	2 μsec
0pF	1.36 μsec	1.27keV	1.06keV
10pF	1.90 μsec	1.72keV	1.21keV
20pF	2.45 μsec	2.18keV	1.38keV
50pF	4.08 μsec	3.59keV	1.99keV
100pF	6.8 μsec	5.96keV	3.10keV
200pF	12.2 μsec	10.7 keV	5.42keV

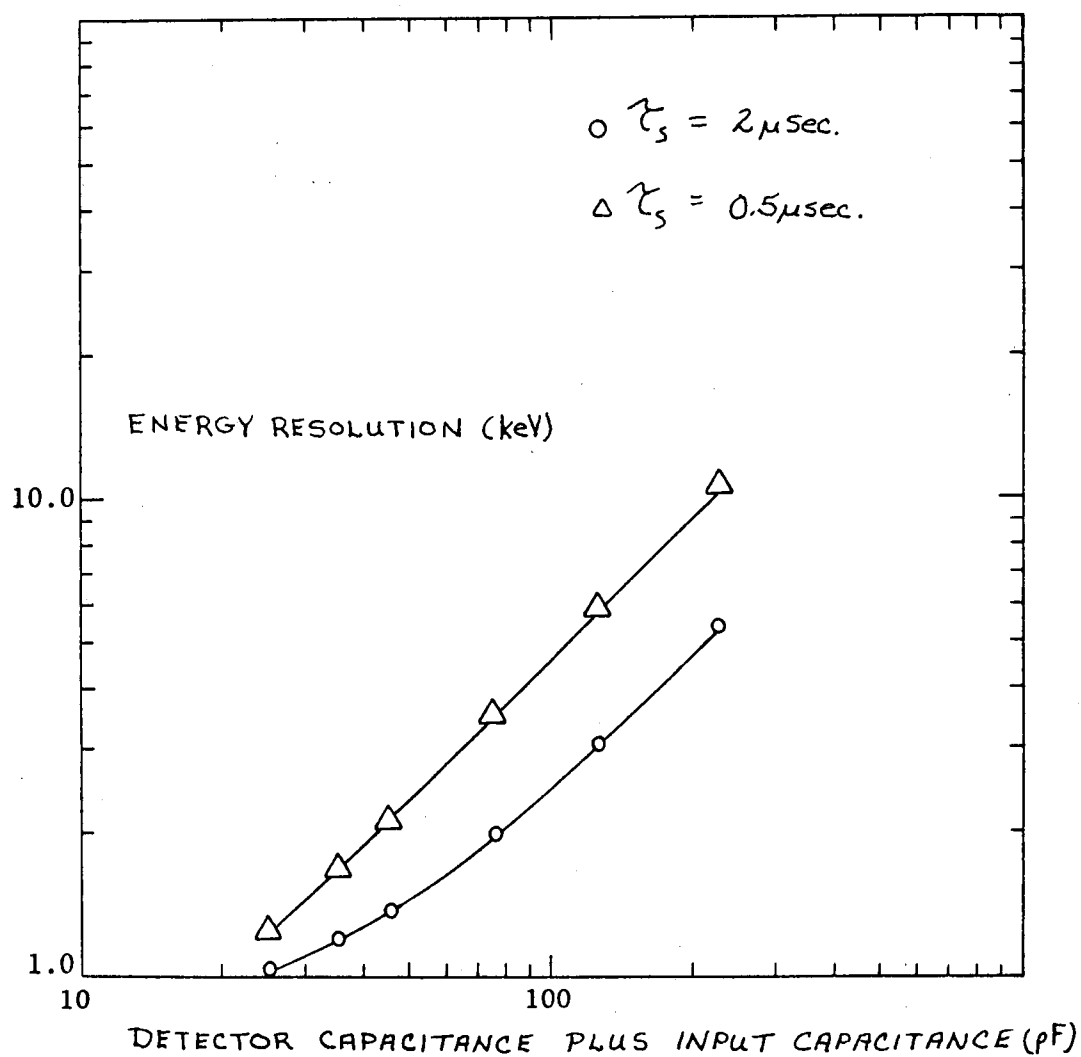


Figure 3.23. Theoretical energy resolution versus total input capacitance.

The theoretical time resolution can be calculated using the method outlined in Chapter 2. The theoretical time resolution is given in Table 3.7 for various energies and detector capacitances.

Conclusions

The N.L.W. and time resolution of the design developed in this chapter are slightly worse than the ideal system proposed in Chapter 2. The higher N.L.W. and time resolution are due to the input capacitance being slightly higher than desired due to the choice of input FET and the second stage noise contribution which was neglected in Chapter 2. The circuit of Figure 3.24 was constructed using hybrid technology. All components inside the dotted lines were mounted on the hybrid substrate. The remaining components were mounted on a conventional printed wiring board. The experimental results are presented in Chapter 5. The parameters of interest are energy resolution, timing resolution, timing risetime, timing conversion gain, energy loop risetime integral nonlinearity and dynamic input capacitance.

The second stage shunt feedback section and the common collector output stage are examined in Chapter 4 using the computer simulation program PCAP. The computer simulation serves to validate the assumptions made in the analysis and in selecting the circuit configuration.

TABLE 3.7
THEORETICAL TIMING RESOLUTION

E_{IN}	1MeV	2MeV	5MeV	10MeV	20MeV	50MeV	100MeV
0pF	11.8psec	5.89psec	2.36psec	1.18psec	0.589psec	0.236psec	0.118psec
10pF	16.5psec	8.24psec	3.30psec	1.65psec	0.824psec	0.33 psec	0.165psec
20pF	21.1psec	10.6 psec	4.2 psec	2.12psec	1.06 psec	0.424psec	0.212psec
50pF	35.3psec	17.7 psec	7.07psec	3.53psec	1.77 psec	7.07 psec	0.353psec
100pF	58.9psec	29.4 psec	11.8 psec	5.8 psec	2.94 psec	1.18 psec	0.589psec
200pF	106 psec	53 psec	21.2 psec	10.6 psec	5.3 psec	2.12 psec	1.06 psec

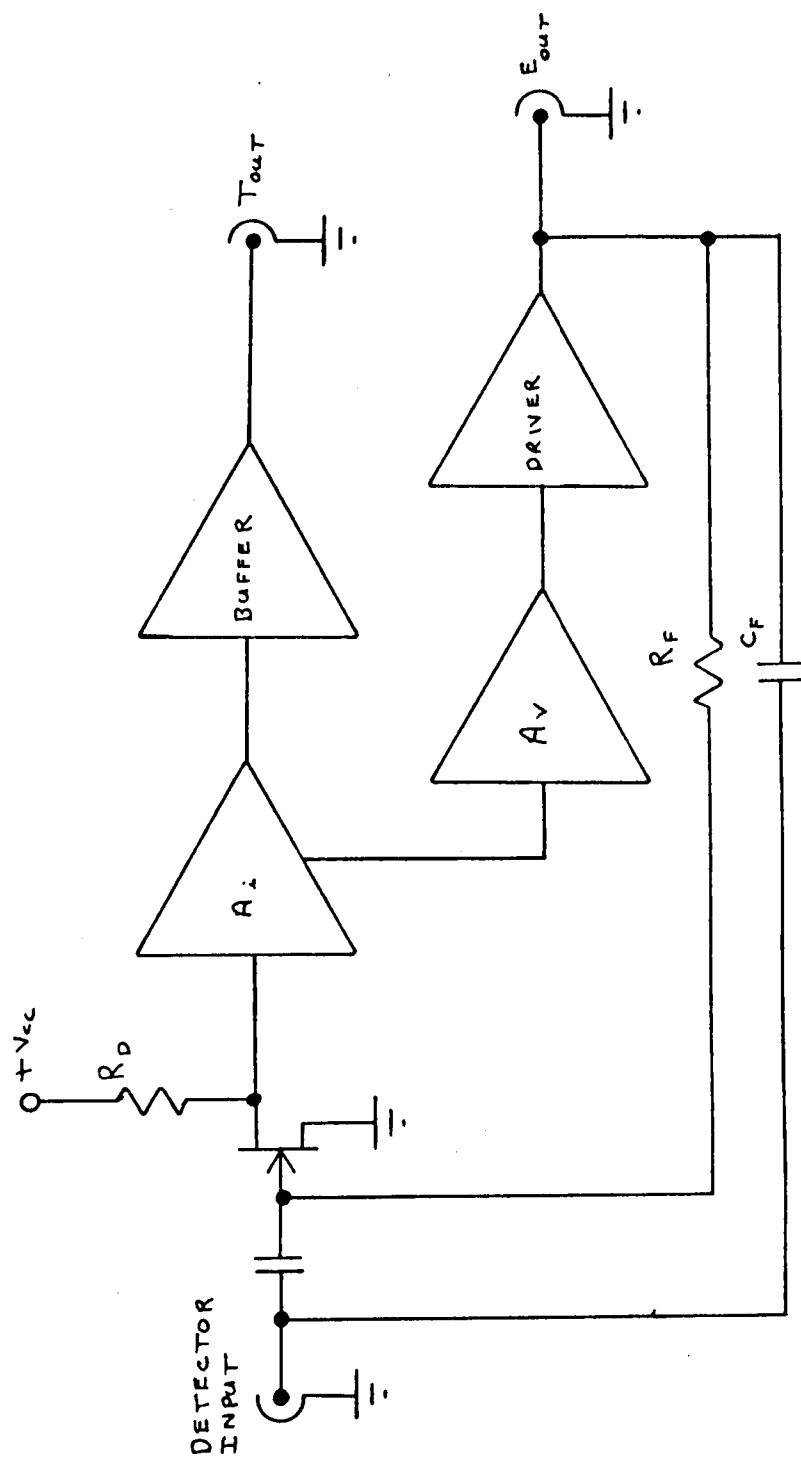


Figure 3.24. Proposed preamplifier.

CHAPTER 4

COMPUTER SIMULATION

Introduction

A circuit design process frequently involves the use of approximations which may produce optimistic results and mask problem areas. The availability of simulation programs such as PCAP allows a circuit to be modeled within the limitations of the active device model. In the design process of the current gain stage as presented in Chapter 3, certain approximations and assumptions were made. A computer simulation program, PCAP, will be used to verify these assumptions and to investigate the effect of certain parameter variations on the loop transmission of the current gain stage.

Shunt Feedback Stage Comparison

The choice of current stages in Chapter 3 was based on a single pole approximation. Using PCAP, the loop transmission of the two circuits in Figure 4.1 was simulated. The component values and device parameters are indicated. This model was used to indicate the relative performance of each configuration in a circuit without the capacitive loading of the FET or any bias resistors. The effects of the FET capacitance and bias resistor are modeled in a later section. The simulation program solved for the loop transmission from the points labeled P and P'. The loop transmission and phase shift are shown in Figure 4.2 for the single stage configurations. As shown by Figure 4.2, the

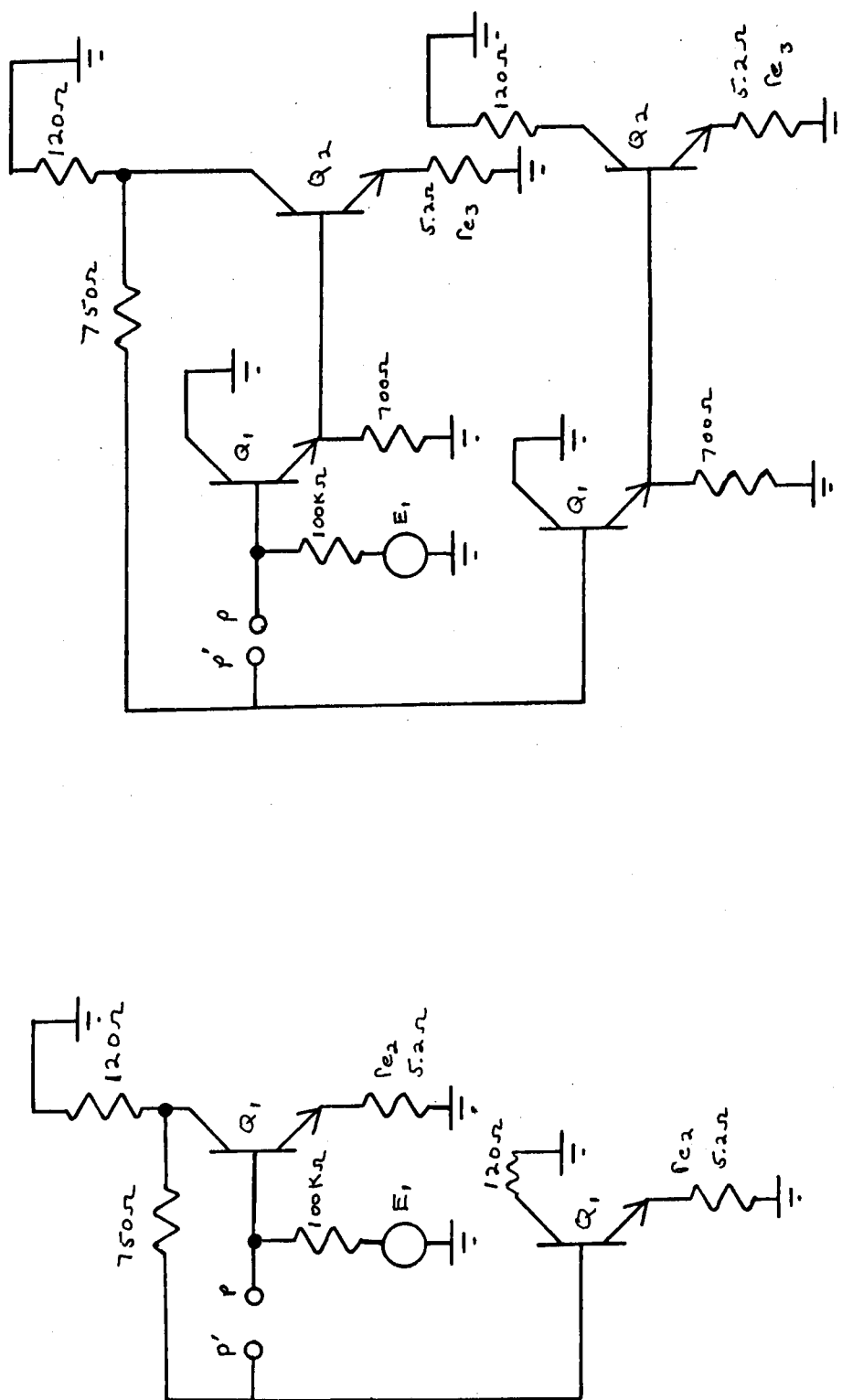


Figure 4.1.1. (a) Circuit used to model T of single-stage shunt-feedback network; (b) Circuit of two-stage shunt-feedback network.

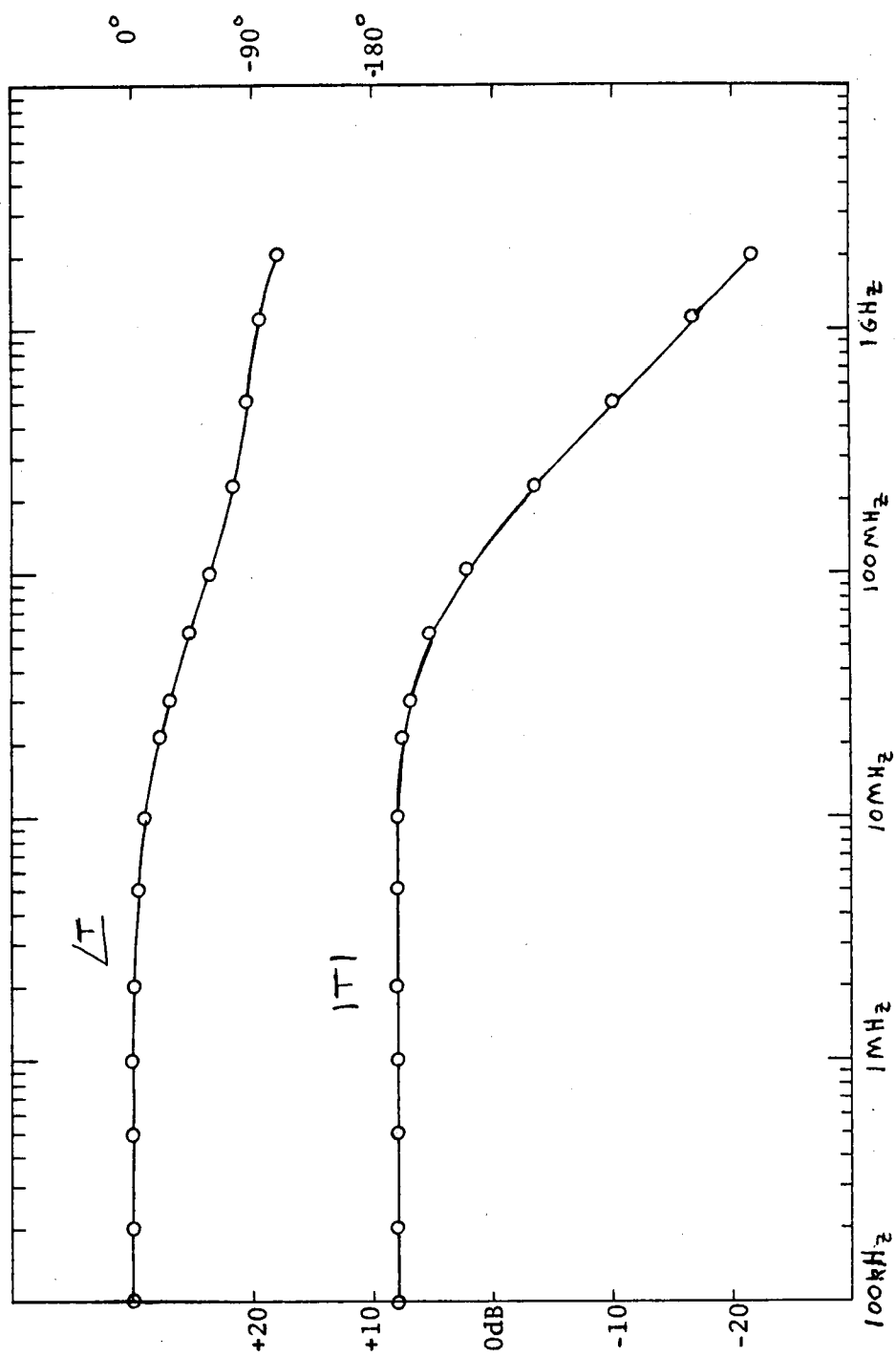


Figure 4.2. T of single-stage shunt-feedback network.

loop transmission is unity at a frequency of 140MHz with a phase margin of approximately 112° . This circuit is stable, but the results are significantly less than predicted by the approximations in Chapter 3. The lower crossover frequency is due to the low loop transmission and high input capacitance. The closed loop gain for the single stage shunt feedback circuit was simulated. The circuit is shown in Figure 4.3. The closed loop gain was measured at the emitter and at the collector since signals from both points will be used. The computer simulation is shown in Figure 4.4. The closed loop gain from the input to the emitter (A_{I_O}) is ideally 7.25 and the computer simulation yields 5.4. The lower than ideal value is due to the low value of loop transmission. The closed loop -3dB frequency is approximately 240MHz. The risetime will be approximately 1.45nsec which is too slow for the required performance. The closed loop gain from the input to the collector ($A_{I_{O1}}$) is ideally 6.25. The computer solution yields 4.38. The lower than ideal value is also due to the loop transmission. A very important consideration for the overall charge loop stability is the excess phase shift introduced by the current gain stage. The single-stage version has a phase shift of -6° at 30MHz. The six degrees of phase shift is not negligible but will not cause any serious degradation in performance due to the high phase margin (57°).

The computer simulation of T for the two-stage shunt-feedback section is shown in Figure 4.5. The crossover frequency is approximately 1.15GHz with a phase margin of 70° . The closed loop gain of the circuit in Figure 4.6 was simulated and the results are shown in Figure 4.7.

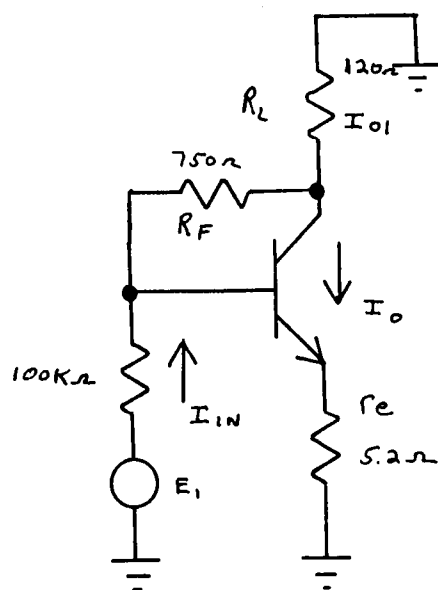


Figure 4.3. Circuit used to model closed loop gain.

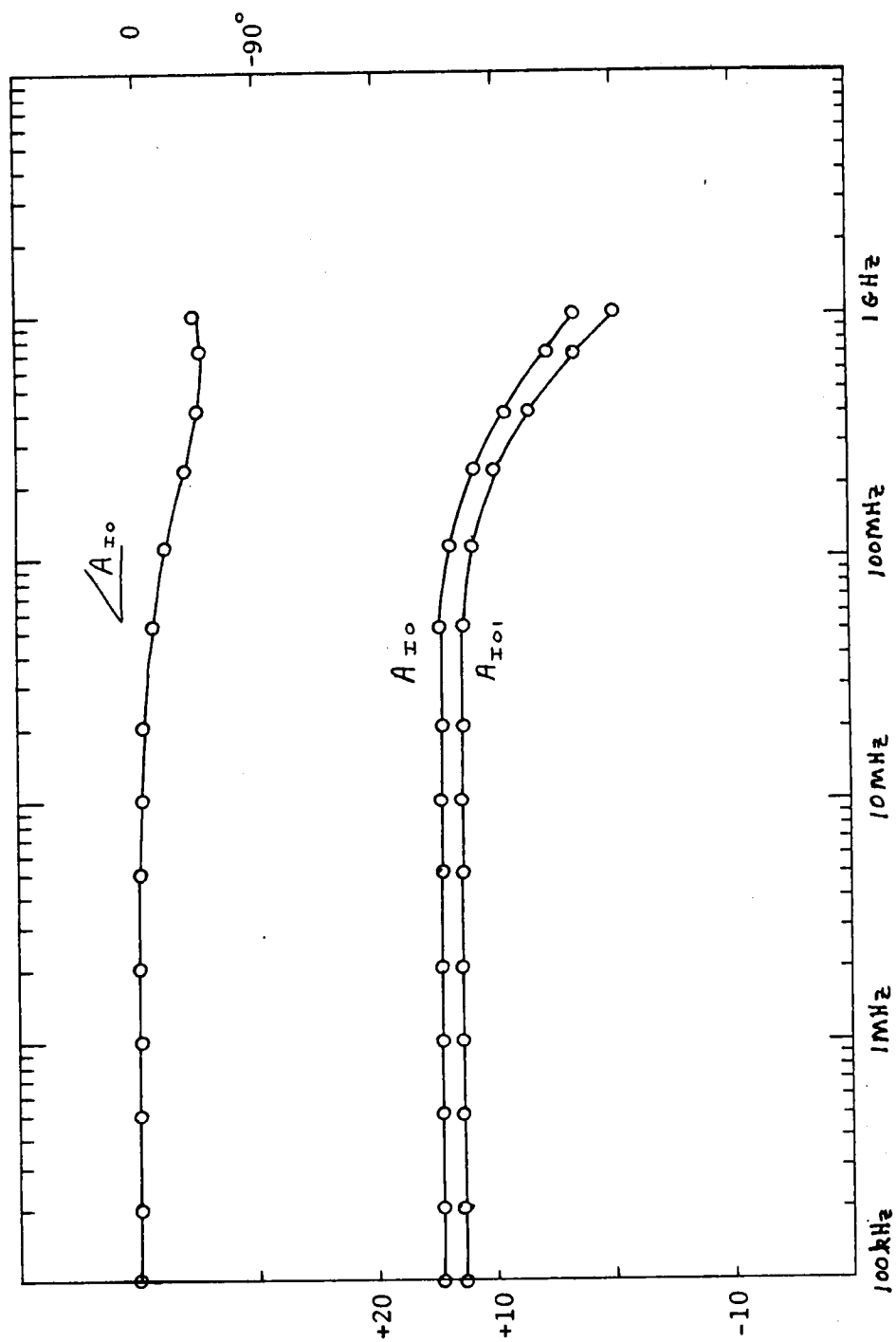


Figure 4.4. Closed-loop gain versus frequency.

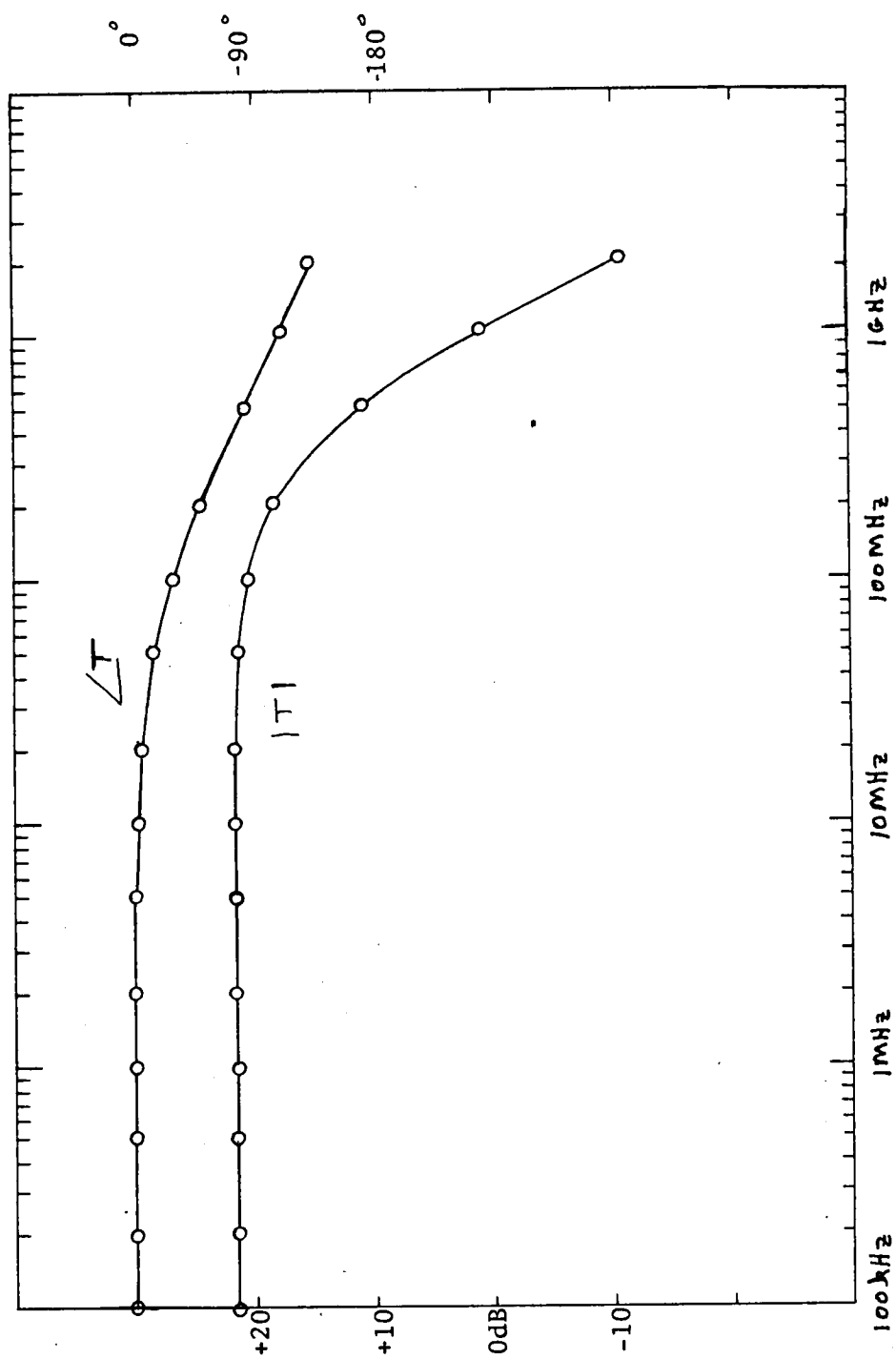


Figure 4.5. T of two-stage shunt-feedback network.

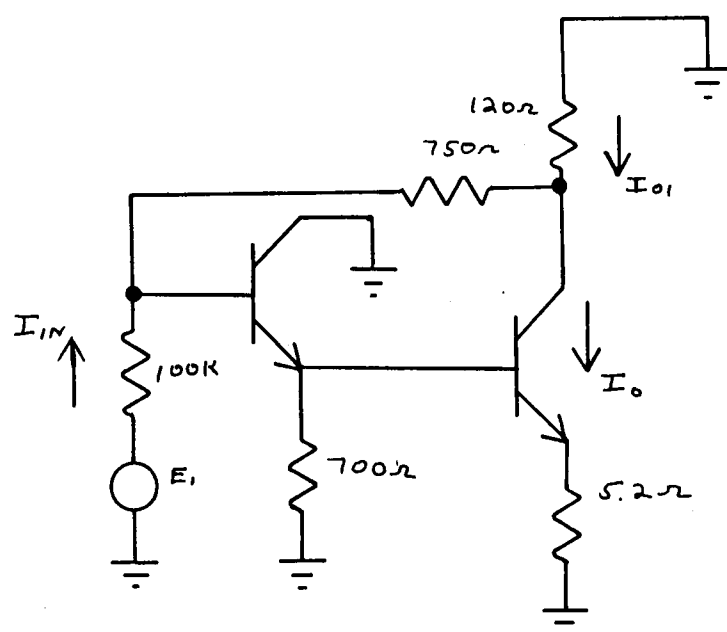


Figure 4.6. Circuit used to model closed-loop gain of two-stage circuit.

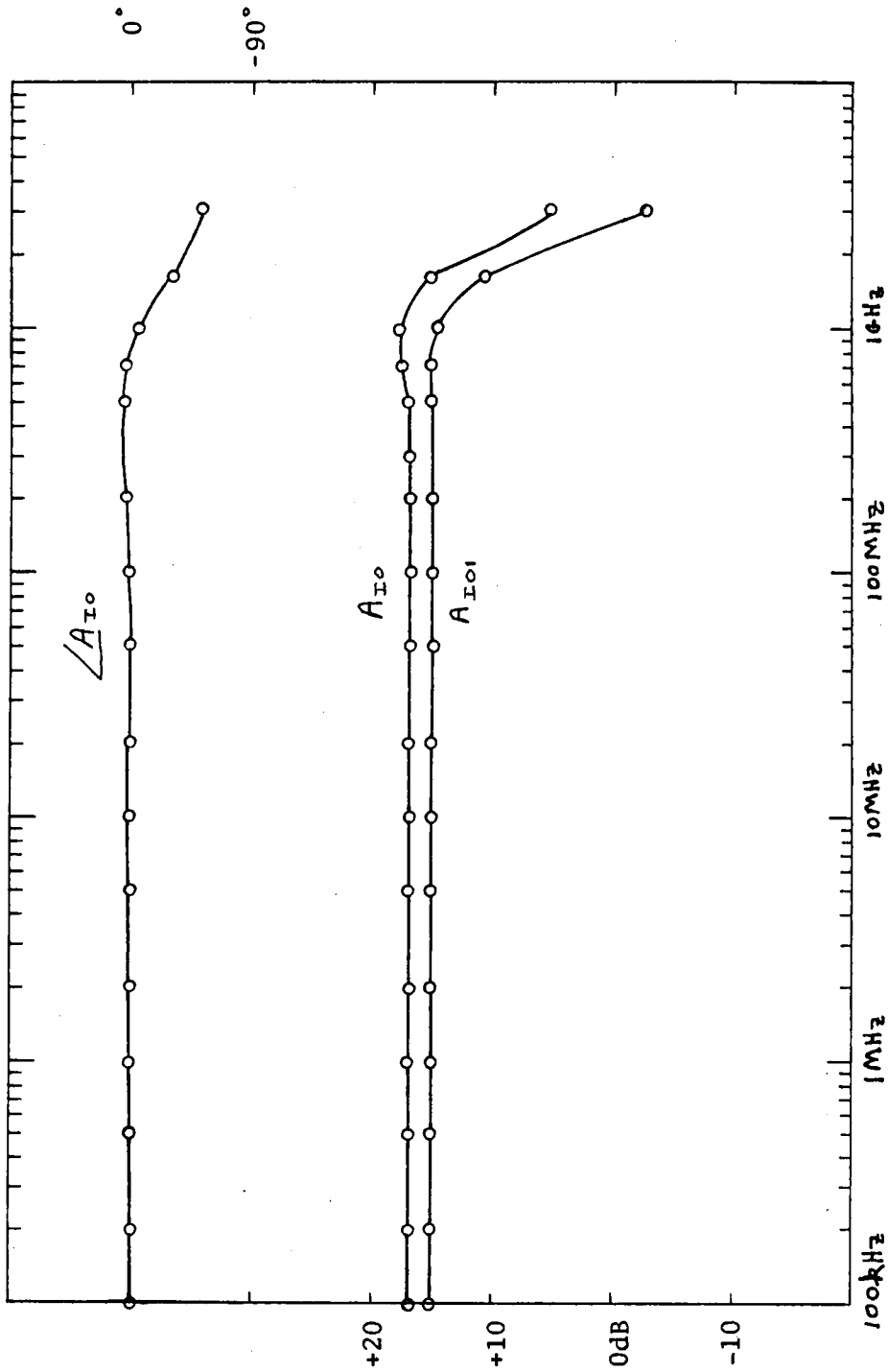


Figure 4.7. Closed-loop gain versus frequency of two-stage circuit.

The closed loop gain from the input to the output emitter (A_{IO}) is ideally 7.25. The computer solution yields 6.96 which is much closer to the ideal value than the single-stage version. The closed-loop gain from the input to the output collector is ideally 6.25 and the computer solution yields 5.67 which is reasonably close to the ideal value. The computer results indicate that the -3dB frequency is 1.75GHz. The -3dB frequency of 1.75GHz should yield a risetime of approximately 200psec. The closed-loop excess phase shift is essentially zero for frequencies of interest for the charge loop. The -3dB frequency of 1.75GHz is very optimistic due to the ideal loading conditions. The intent of this section was to show the relative merits of the two circuits. The results show that the two-stage shunt-feedback amplifier has significant advantages over the single-stage version. However, this advantage may not be as great for the nonideal circuit due to the location of the dominant pole for the two-stage configuration. This possibility is investigated in the next section.

Effects of Input Capacitance on Shunt-Feedback Stage

To model the shunt-feedback stage under actual operating conditions, the circuits in Figure 4.8 were used. The values of R_D is 1.1K Ω and C_D was set equal to 2pF, 4pF and 6pF. The value of C_D was varied to check the frequency response variations for changes in circuit strays and FET output capacitance. The effect of C_D on the single-stage circuit is shown in Figures 4.9 and 4.10. The effect on the loop transmission is significant. The crossover frequency varies from

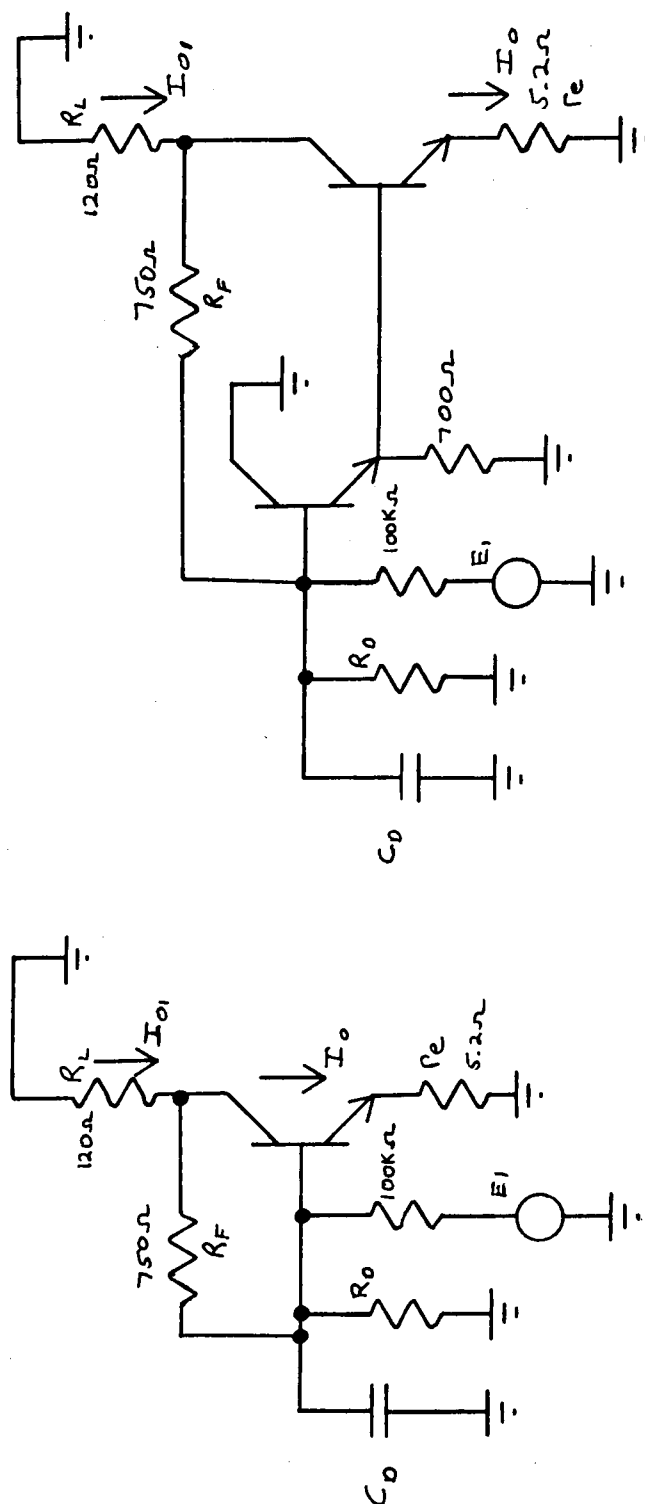


Figure 4.8. (a) Circuit used to determine effect of R_D and C_D on single-stage shunt-feedback circuit;
(b) Circuit used to determine effect of R_D and C_D on two-stage shunt-feedback circuit.

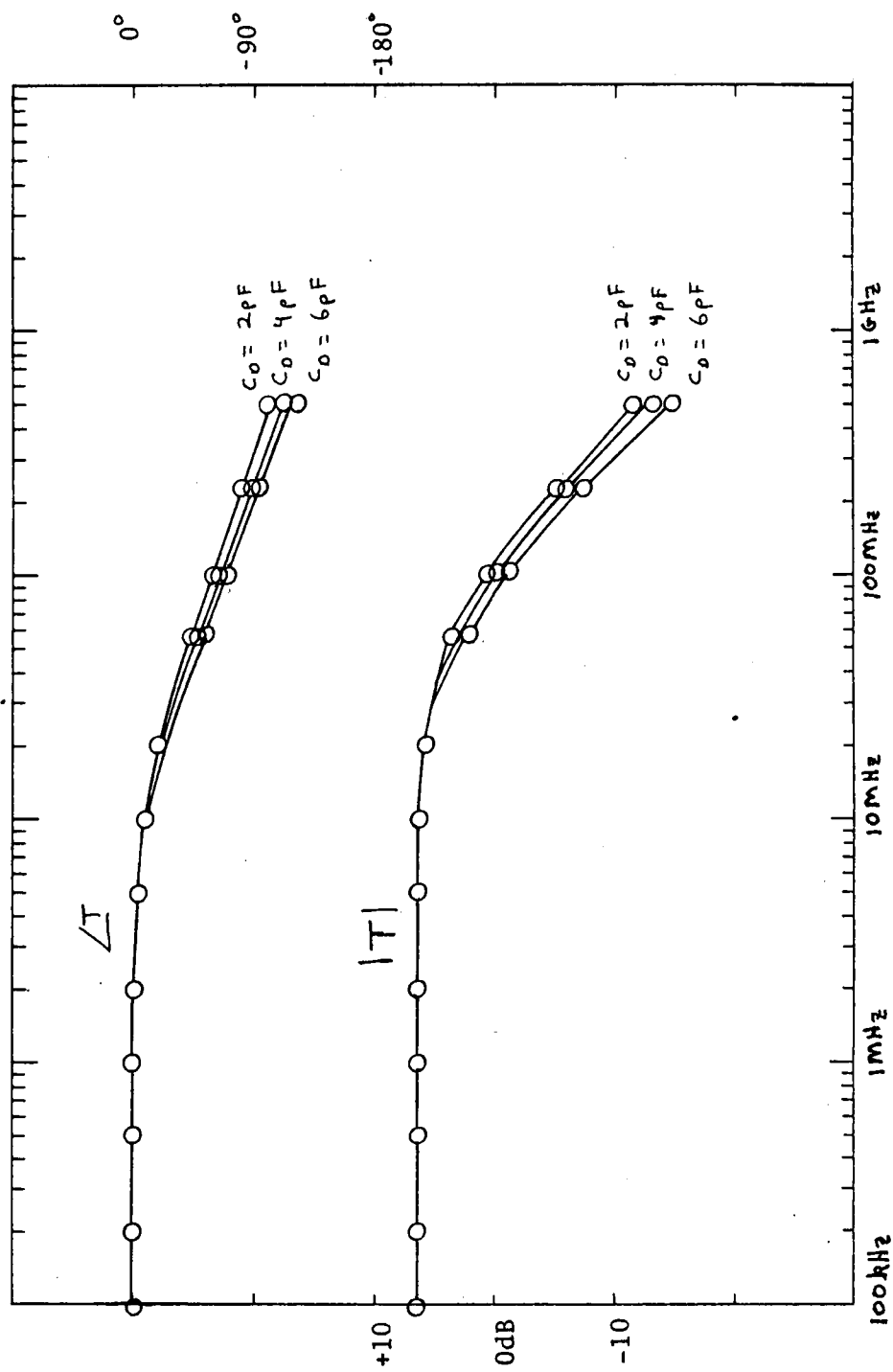


Figure 4.9. Effect of C_D on single-stage amplifier.

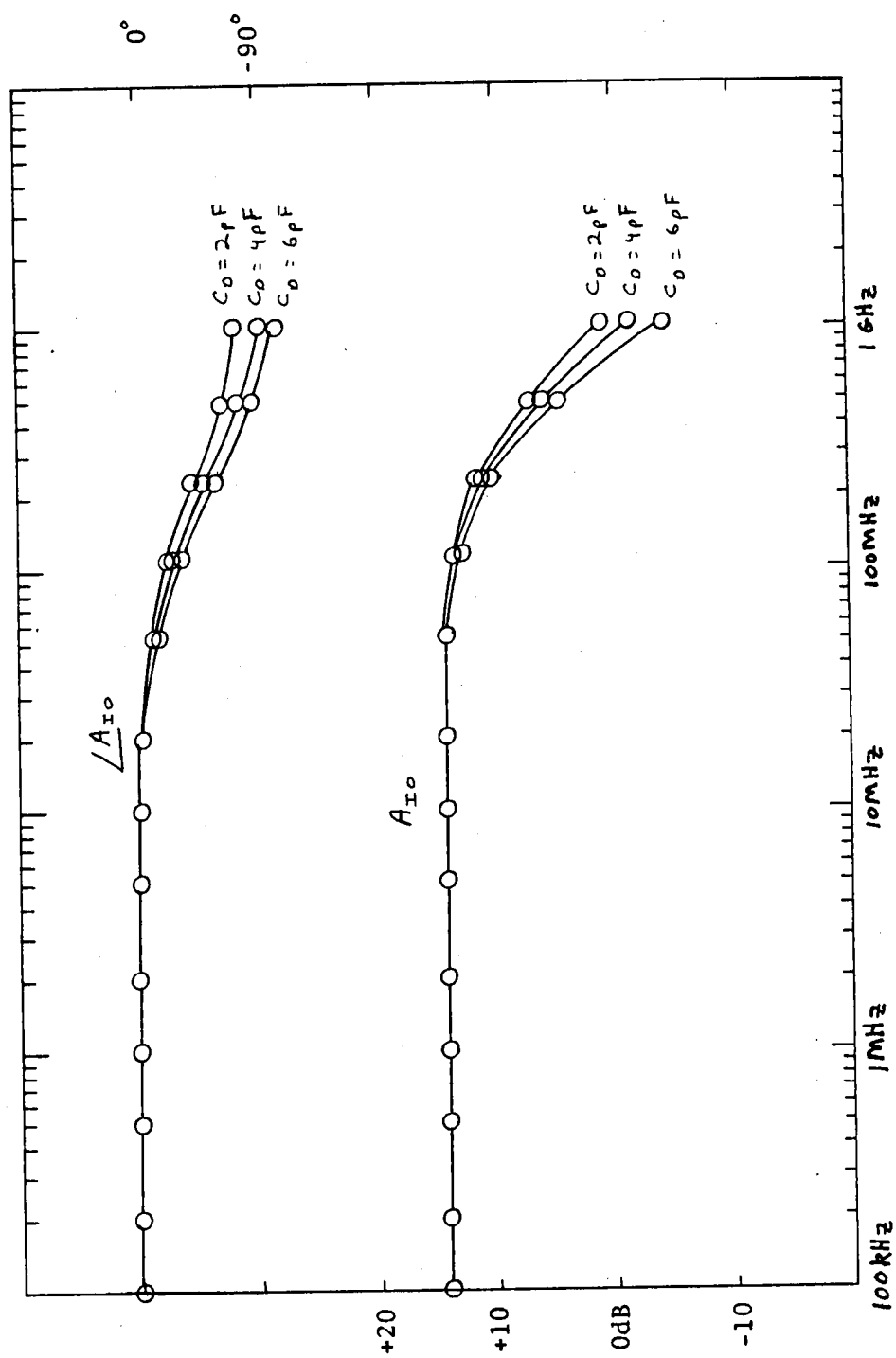


Figure 4.10. Effect of C_D on single-stage amplifier.

approximately 108MHz for C_D equals 2pF to 84MHz for C_D equals 6pF. The phase margin remains in excess of 90° for the variations of C_D from 2pF to 6pF. The effect of C_D on the closed loop gain is shown in Figure 4.10. The -3dB frequency varies from 140MHz for C_D equals 2pF to 120MHz for C_D equals 6pF. This change is not significant but does yield less than optimum results. The loop transmission and closed loop response for the two-stage shunt-feedback amplifier are shown in Figures 4.11 and 4.12. The values of C_D selected are 2pF, 4pF and 6pF. The effect of C_D on the loop transmission is very significant. The loop transmission crossover frequency varies from 440MHz for C_D equal to 2pF to 225MHz for C_D equal to 6pF. This change clearly shows the importance of minimizing the stray capacitance at the input of the two-stage shunt-feedback amplifier. The -3dB frequency is similarly affected, varying from 760MHz at 2pF to 400MHz at 6pF. The design value of C_D is 4pF. The two-stage circuit is clearly superior to the single-stage version under the circuit constraints imposed by the overall design goals. The predicted risetime of the two stage circuit for C_D equal to 4pF is 733psec. This value of risetime will result in an overall risetime of approximately 845psec which is less than the design goal of 1nsec. The gain of the second stage from input to the emitter is 6.48 and the gain to the collector is 5.28. Both values are lower than ideal due to the low loop transmission. The expression for the ideal closed loop gain is

$$A_I = \frac{R_F + R_L}{R_L} \quad (4.1)$$

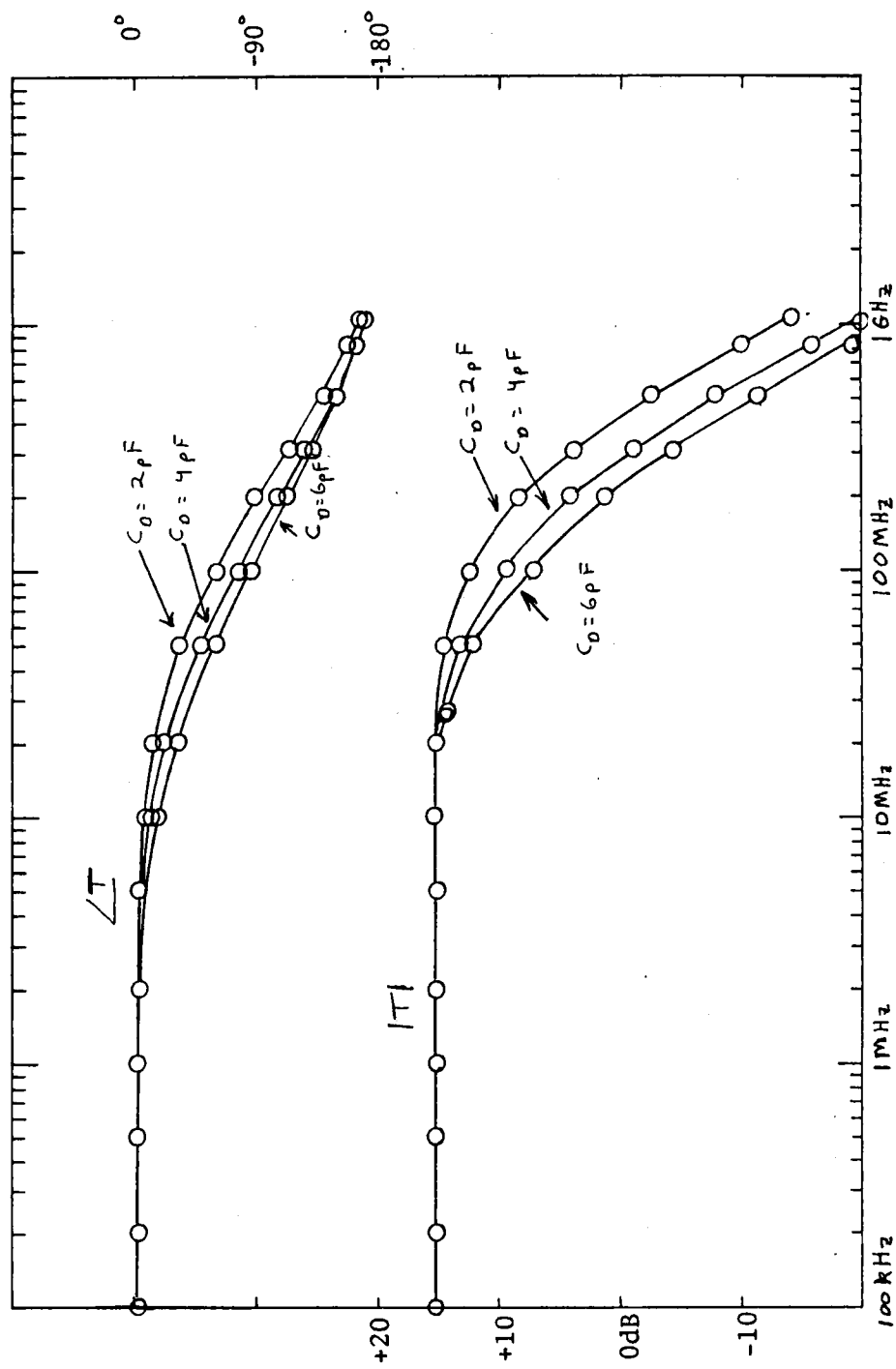
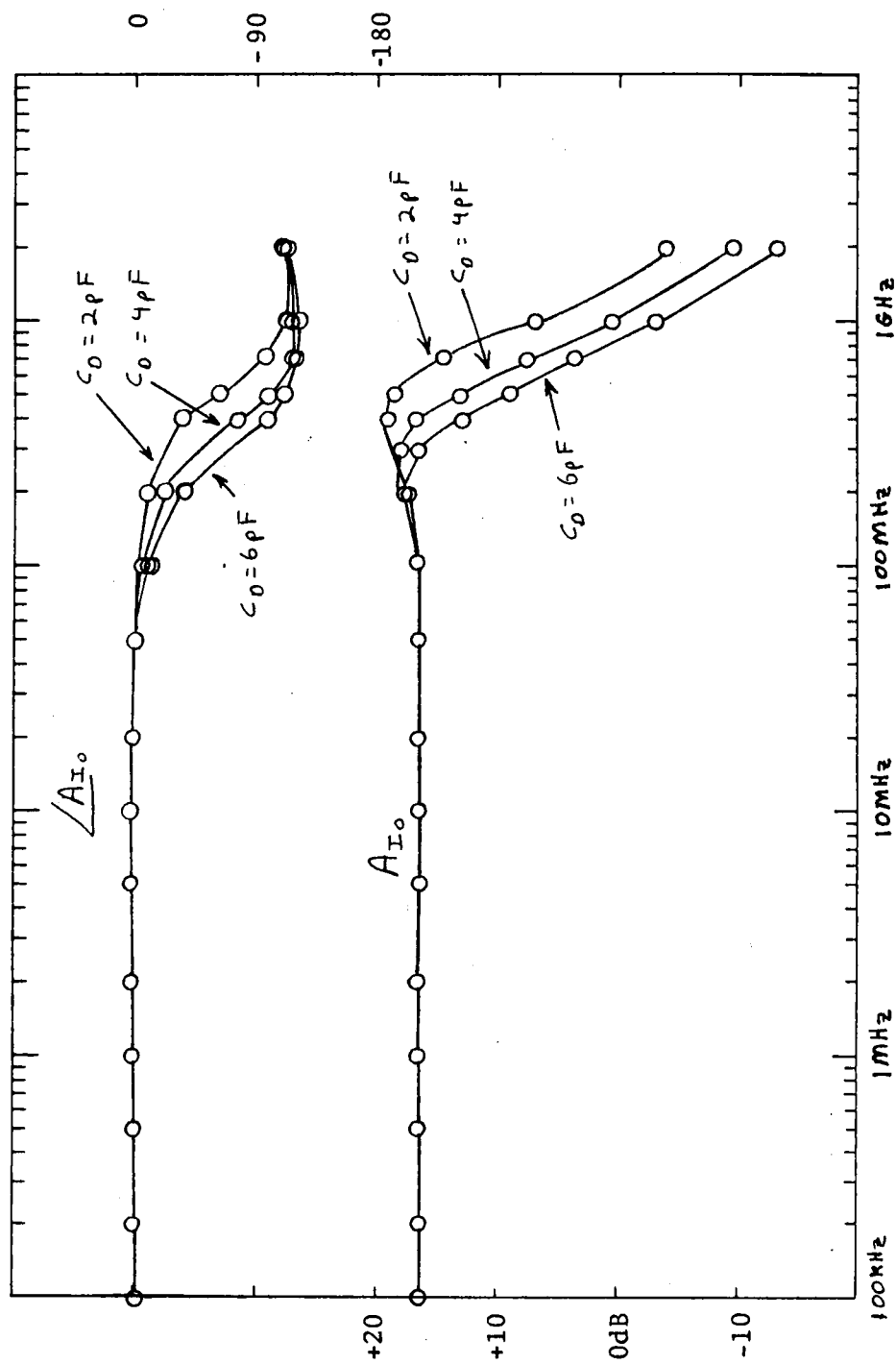


Figure 4.11. Effect of C_D on two-stage amplifier.

Figure 4.12. Effect of C_D on two-stage amplifier.

and the expression for the actual gain is

$$A_I = \left(\frac{R_F + R_L}{R_L} \right) \frac{T}{1+T} \quad (4.2)$$

Conclusion

In this chapter, the superiority of the two-stage circuit was verified with a computer simulation program PCAP. The risetime of the two-stage circuit as predicted by the computer simulation agrees very closely with that predicted in Chapter 3. In addition, the sensitivity of both circuits to the total input capacitance was simulated. The two-stage circuit is more sensitive to input capacitance as predicted in Chapter 3.

The circuit of Figure 3.24, p. 113 was constructed as outlined at the conclusion of Chapter 3. The results are presented in Chapter 5. The parameters of interest are risetime (charge loop and timing loop), gain for the timing loop, noise, integral nonlinearity and dynamic input capacitance.

CHAPTER 5

EXPERIMENTAL RESULTS

Introduction

The previous two chapters have resulted in the design as shown in Figure 3.24, p. 113. The performance specifications were covered in Chapter 3 but will be summarized again. The charge loop risetime for zero detector capacitance is $<15\text{nsec}$. The calculated risetime is 8nsec with 10% overshoot. The N.L.W. as measured with a $2\mu\text{sec}$ shaping time is less than 1.6keV for zero detector capacitance and less than 3.6keV for 100pF detector capacitance. The integral nonlinearity is less than 0.05% over a 100MeV range. The dynamic input capacitance is greater than $10,000\text{pF}$ at $2\mu\text{sec}$. The timing loop risetime is less than 1nsec . The conversion gain for the timing signal should be 440mV per MeV of energy per picofarad of total input capacitance plus detector capacitance. The series noise resistance for the timing loop is less than 40 ohms .

The circuit design presented in Chapter 3 should easily meet these specifications. Such a circuit was constructed using hybrid technology to minimize and control stray capacitances and inductances. The major benefits of hybrid technology in this design are the control and consistency of the strays, and minimization of signal path length (excess phase shift due to delay). The hybrid consists of the circuit inside the dashed lines of Figure 3.24, p. 113. The printed circuit board was laid out to minimize path length of the FET drain to the hybrid and of

the timing output connector. The circuit enclosure was then designed to be as small as feasible yet provide a heat conductive path from the hybrid substrate to the metal enclosure. The heat conductive path was necessary to allow operation in a vacuum chamber with the preamplifier connected directly to the detector. The power dissipation can be very significant because all heat transfer will be by radiation and conduction in a vacuum. Heat removal by convection does not exist. To facilitate the heat removal, the hybrid was mounted on the back of the printed circuit board and allowed to contact the metal enclosure. When fully assembled this package measures one inch high by 1.85 inches in diameter.

Charge Loop Performance

The performance of the charge loop is easily measured compared to the timing loop. The risetime of the charge loop was designed for a small signal risetime of 15nsec in either positive or negative direction when driving a 100 Ω load resistor. The signal source for the input was a tail pulser driving a charge terminator as shown in Figure 5.1. The risetime for values of detector capacitance up to 200pF was measured for signal inputs equivalent to 10MeV and the results are shown in Figure 5.2. The wave form for a 10MeV positive-going signal for zero detector capacitance is shown in Figure 5.3. The positive direction will be the direction of the energy output signal for the majority of detectors. The output signal will be reversed for detectors using a

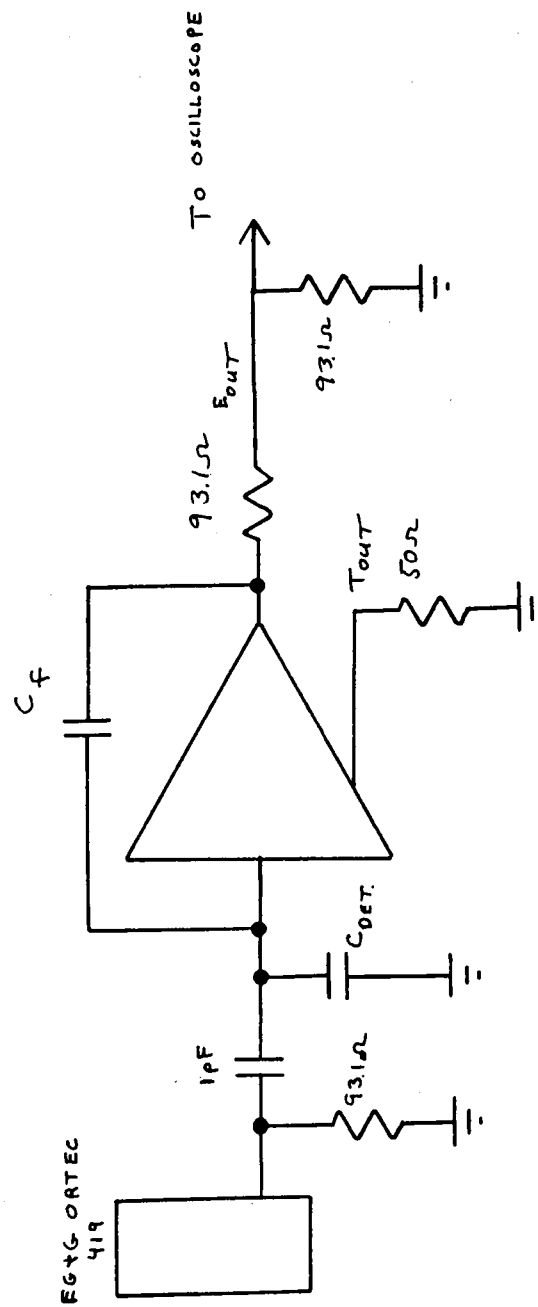


Figure 5.1. Circuit used to measure charge-loop risetime.

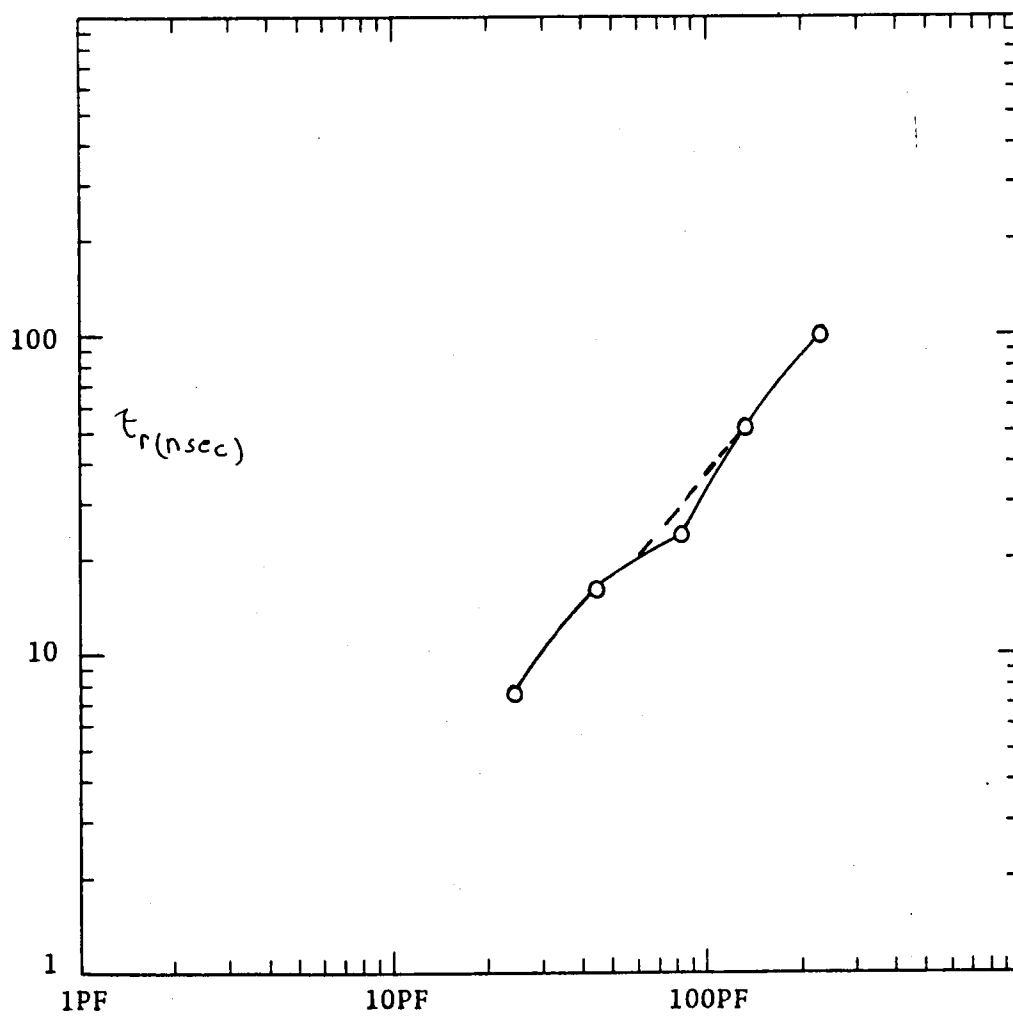


Figure 5.2. Charge-loop risetime versus total input capacitance.

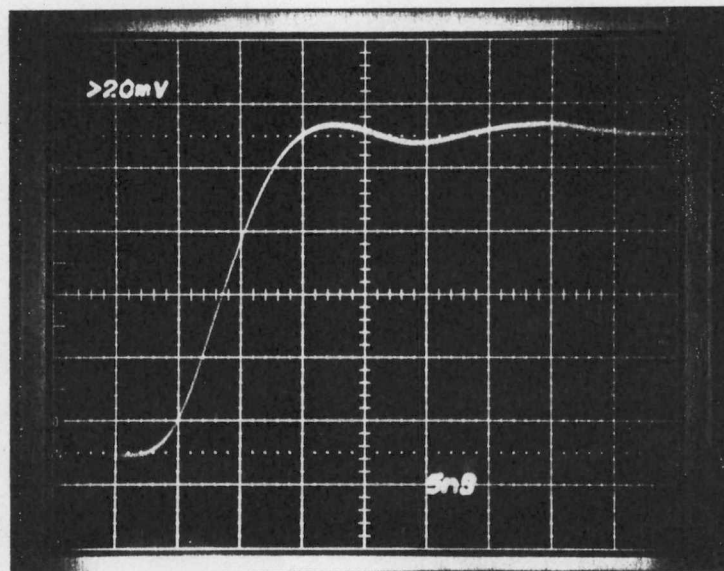


Figure 5.3. Actual charge loop output signal for a 10MeV equivalent input signal, $C_{\text{DETECTOR}} = 0\text{pF}$.

negative bias supply (ruggedized detectors). The risetime at zero detector capacitance for 10MeV is 7.5nsec and the overshoot is 6%. The risetime at 10MeV for 100pF detector capacitance is 52nsec with no overshoot. The risetimes were also measured with 100MeV signals. The results for positive outputs are shown in Table 5.1 for comparison with the risetimes of negative output signals at energies of 10MeV and 100MeV. The risetime for positive signals was 7.5nsec with 10% overshoot. The calculated value for the risetime was 8nsec with 10% overshoot. The negative output risetime is 7.5nsec for small signal and degrades to 15nsec for a 100MeV input. The degraded risetime is due to slew rate limiting at the dominate node. The slew rate is controlled by the total capacitance at the dominate node and the available charging current. The slew rate for the design is Figure 3.24, p. 113 was calculated as $200\text{V}/\mu\text{sec}$. The measure value was $210\text{V}/\mu\text{sec}$. The value of $210\text{V}/\mu\text{sec}$ is in agreement with the negative output risetime of 15nsec for a 100MeV input.

The N.L.W. was measured in terms of keV silicon with a tail pulser calibrated to 5.48MeV using an alpha emitting radioactive source such as Am^{241} . The pulser produces a voltage signal which is converted to a charge pulse by a series capacitor. The equivalent energy of the charge pulse is controlled by varying the output voltage of the pulse generator. The pulser was adjusted to produce a 1MeV equivalent energy input to the preamplifier detector input. The output of the preamplifier was

TABLE 5.1
CHARGE LOOP RISETIME AS A FUNCTION OF DETECTOR
CAPACITANCE FOR 100MeV EQUIVALENT INPUT
SIGNALS BOTH POSITIVE
AND NEGATIVE POLARITY

DETECTOR CAPACITANCE	POSITIVE OUTPUT		NEGATIVE OUTPUT	
	τ_r	%O.V.S.	τ_r	%O.V.S.
0pF	7.0nsec	6%	15nsec	0
20pF	16 nsec	0	15nsec	0
50pF	21 nsec	0	22nsec	0
100pF	50 nsec	0	50nsec	0
200pF	100 nsec	0	100nsec	0

connected to a shaping amplifier as shown in Figure 5.4. The shaping amplifier time constant was chosen to minimize the noise contribution and provide signal gain. The gain of the shaping amplifier was adjusted to provide a precise positive 2.35 volt output signal. The signal input to the preamplifier is now removed. The output of the shaping amplifier is then connected to the true rms meter such as an HP 3400A. The noise voltage can then be read from the noise meter in terms of keV FWHM per millivolt of rms noise. The purpose of adjusting the amplifier to a precise 2.35 volt signal is to accomplish the conversion between rms and FWHM. The N.L.W. was measured at shaping times of 2 μ sec and 0.5 μ sec for values of capacitance from 0pF to 100pF. The results are shown in Figure 5.5 as a function of detector capacitance. The noise as measured at 2 μ sec was 1.43keV for zero detector capacitance. For purposes of comparison, the theoretical results are indicated by the dashed lines. The measured values are slightly higher than the predicted values. The higher value at zero detector capacitance is probably due to a higher gate leakage current than assumed or a lower value of bias resistor than 100M Ω . It should be noted that the only component selected was the input FET and this was selected primarily for noise performance at 100pF detector capacitance. The results at 100pF detector capacitance are within 6% of the calculated value. This is very close agreement and the results are better than the design goal of 1.6keV and 3.6keV.

The integral nonlinearity was measured using the circuit shown in Figure 5.6. The preamplifier input signal is adjusted to produce the

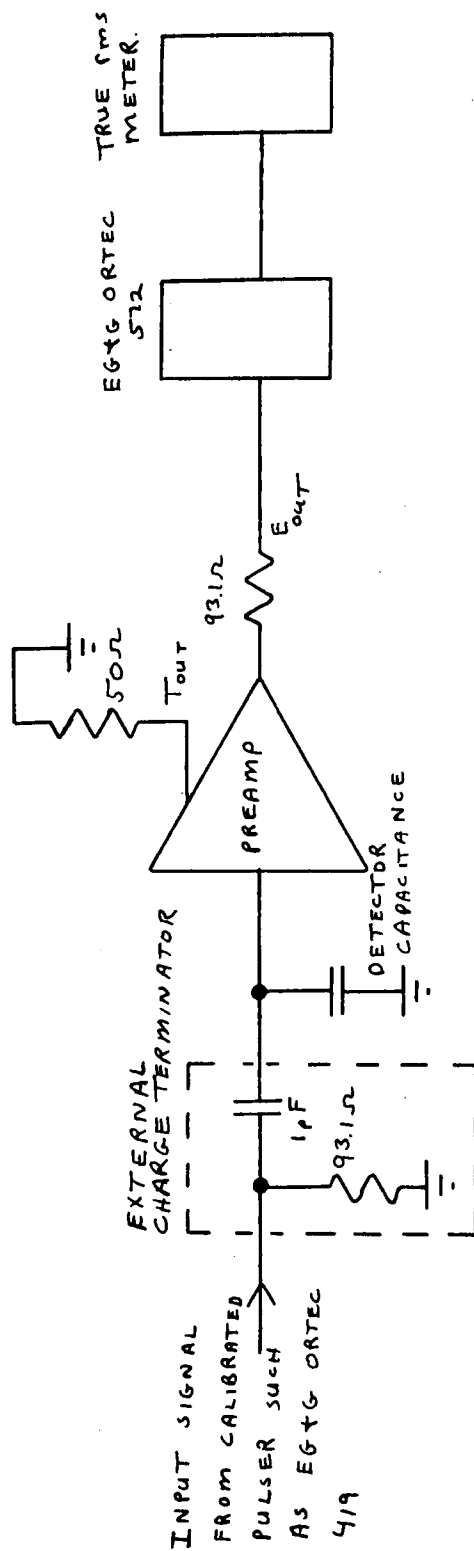


Figure 5.4. System used to measure energy resolution of charge loop.

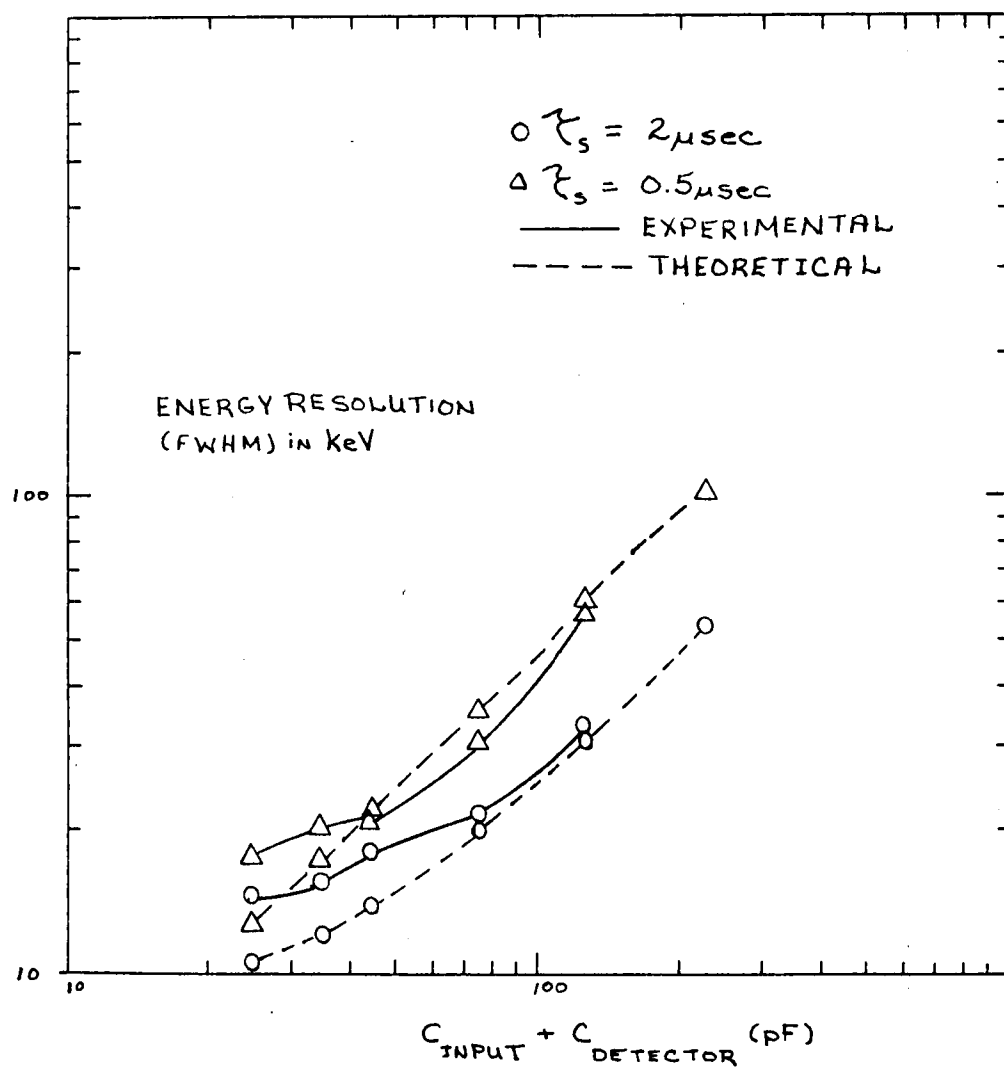


Figure 5.5. Energy resolution (FWHM) keV versus detector capacitance.

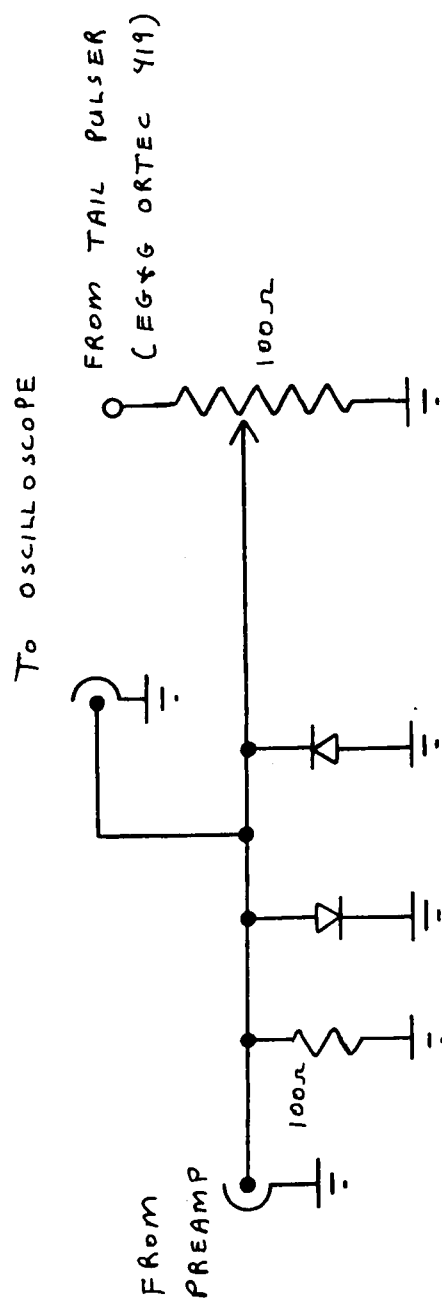


Figure 5.6. Circuit used to measure integral nonlinearity.

required preamplifier output signal. The preamplifier output is then connected to the point shown and the pulser direct output is connected to the point shown. The zero adjust dial is then used to position the waveform at the zero crossing producing a null as shown in Figure 5.7. This null point should be adjusted to occur at a time well past the settling time but not drastically down the waveform. A null time of 8μsec was chosen for this measurement which is slightly shorter than current industrial practice. The longer this null time, the better the results. Using this method, the integral nonlinearity is

$$L_I = \frac{2X\Delta VE}{V_{omax}} \times 100\% \quad , \quad (5.1)$$

where ΔVE is the change in voltage at the zero crossing point. The 2X multiplier is due to the attenuation of the null network. The integral nonlinearity as measured over a $\pm 100\text{MeV}$ range was below measurable levels. The integral nonlinearity over a $\pm 160\text{MeV}$ range was -0.005%. This result is significantly less than the design goal and is the primary result of using the current gain stage with a pole located at zero ideally. In actuality, the pole occurs at a higher frequency due to limitations on Beta which limits the maximum available current gain. However, the net result is to increase T for frequencies of interest as shown in Chapter 3.

The dynamic input capacitance is an indirect measurement on the open loop gain of the charge loop as shown by Equation (3.85). In addition, a high dynamic input capacitance is required to eliminate signal loss for large values of detector capacitances. The resultant

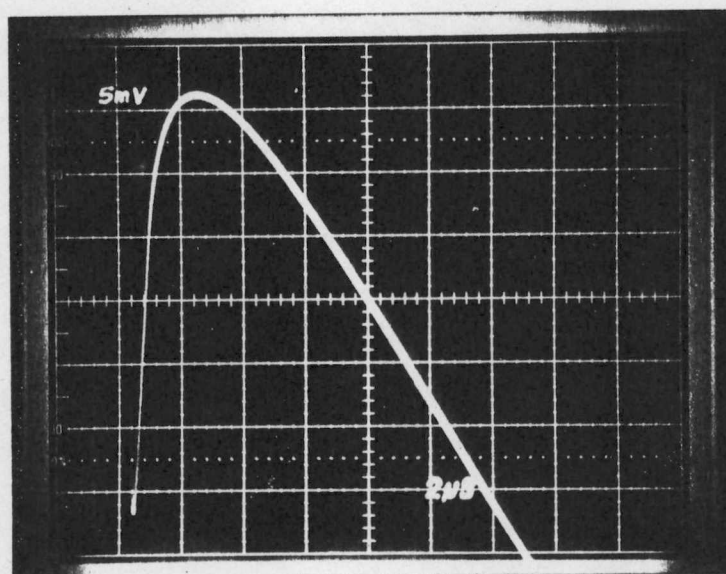


Figure 5.7. Integral nonlinearity null waveform.

signal loss will cause the signal to noise ratio to decrease, resulting in less than optimum energy resolution. The signal loss for a 100pF detector with a preamplifier whose dynamic input capacitance is 5000pF is approximately 2%. If the same preamplifier has a dynamic input capacitance of 20,000pF, the signal loss is only approximately 0.5%. The dynamic input capacitance was measured at 2 μ sec and 0.5 μ sec. The circuit used for this measurement is shown in Figure 5.8. The pulser was set to provide a 10MeV input signal to the preamplifier and the shaping amplifier was adjusted to provide a ± 8 volt output at the selected time constant with no detector capacitance connected to the preamplifier. A 1000pF test capacitor (C_T) was then connected to the preamplifier input in parallel with the input signal. The resultant drop in the output voltage of the shaping amplifier was used to calculate the dynamic input capacitance using a voltage division approach. The result at 2 μ sec was 22,000pF. The calculated value is 16,400pF which is less than the actual result. This error is due to the variations from nominal in total feedback capacitance plus strays and a higher open loop gain than calculated. The error is approximately 40% which, if due only to the open loop gain, would result from a 3dB higher loop transmission. This particular parameter is difficult to predict accurately and a 3dB error is within reasonable limits. This method could be used to measure the open loop gain if the measurement was made over a broad range of frequencies and would then provide an indirect measurement of the loop transmission.

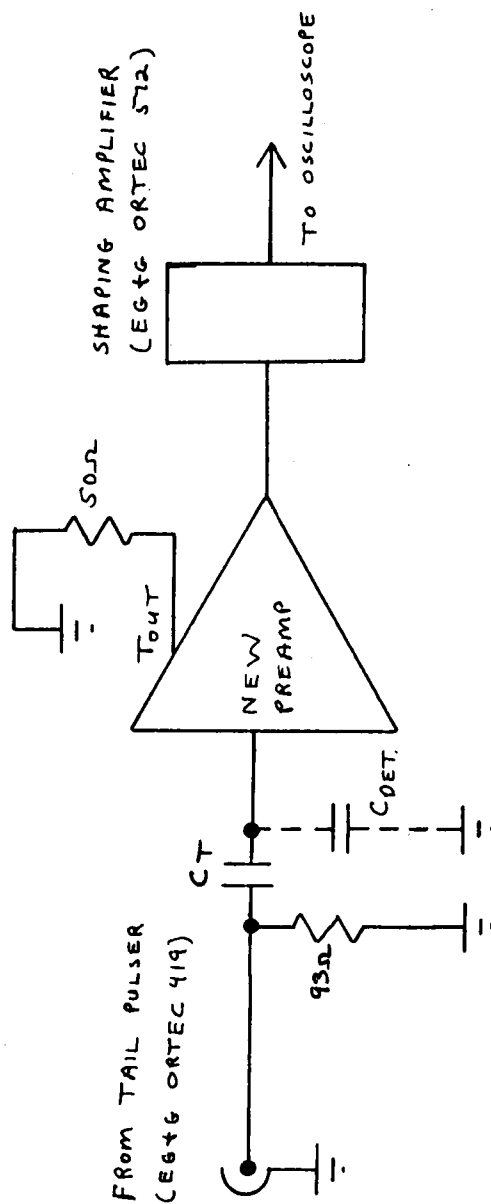


Figure 5.8. Circuit used to measure dynamic input capacitance.

The critical specifications of the charge loop were measured and found to be in close agreement with the predicted results. The performance easily meets the design goals and has sufficient margins to allow for component variations on a production basis. This approach does not require that each unit be modified or repaired to meet performance goals. With the use of hybrid technology, repair or modification is not possible on a production basis.

Timing Loop Performance

The timing loop performance is significantly more difficult to verify due to the level of performance. The techniques used to measure the charge loop will not be adequate. The risetime must be measured using a very fast risetime pulser. The pulser must have a risetime significantly lower than 1nsec. The pulser and oscilloscope contribution must be subtracted in quadrature. The very best real time oscilloscopes have risetimes on the order of 0.7nsec. To minimize the effect of the oscilloscope, a fast sampling oscilloscope is required. In addition, the risetime as a function of detector capacitance cannot be measured due to the unpredictable response of capacitors when pulsed with signals having risetimes less than 1nsec. During the testing of the timing loop, significant variations were observed for types of capacitors and even different capacitors of the same type and value. Due to these problems the risetime will be measured with no detector capacitance. The timing loop risetime was measured at zero detector capacitance using a fast avalanche pulser. The combined avalanche pulser and

oscilloscope risetime is 230psec. The pulser waveform is shown in Figure 5.9. The timing loop output signal level was set at -50mV. The total system risetime was 700psec. The net risetime of the preamplifier is 660psec. The resultant timing loop waveform is shown in Figure 5.10. The predicted value of the timing loop risetime is 775psec. The actual result is approximately 15% lower than the theoretical result. This error can be attributed to lower capacitance at the FET drain and a lower FET risetime than predicted.

The timing loop gain cannot be measured accurately using a calibrated pulser and a capacitor due to the same problem as with measuring the risetime. The timing loop gain can be measured using a detector of known capacitance, a radioactive source such as Am^{241} , and a laser diode pulser.¹⁵ The laser diode pulser is calibrated using the Am^{241} source to allow a wide range of equivalent energies. The detector and Am^{241} source are installed in a vacuum chamber to prevent energy loss due to the atmosphere because alpha particles are very easily stopped due to their high mass. The timing loop conversion gain was measured for values of detector capacitance ranging from 10pF to 209pF. The results are shown in Table 5.2. The conversion gain cannot be calibrated directly from these data because the input capacitance and any strays associated with connecting the detector to the preamplifier must be taken into account. The total input capacitance and connecting strays can be approximated as 35pF. The theoretical input capacitance is 25pF and includes 10pF of connecting strays. The equation used to arrive at the actual conversion gain is

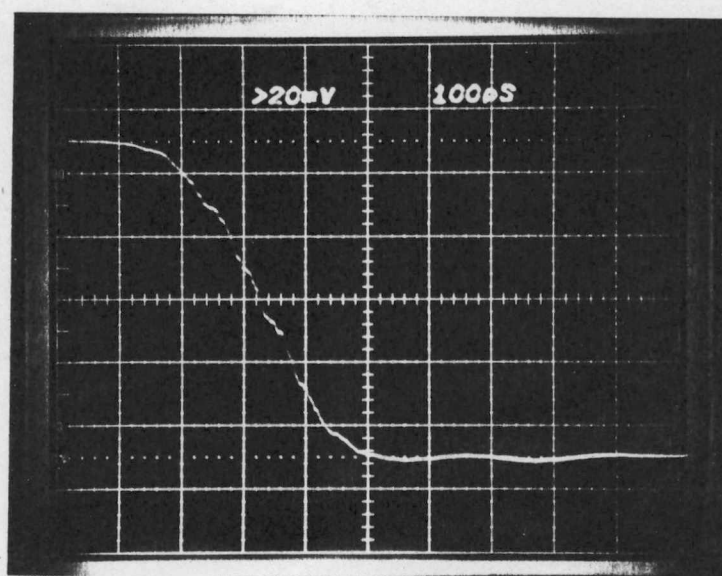


Figure 5.9. Avalanche pulser waveform.

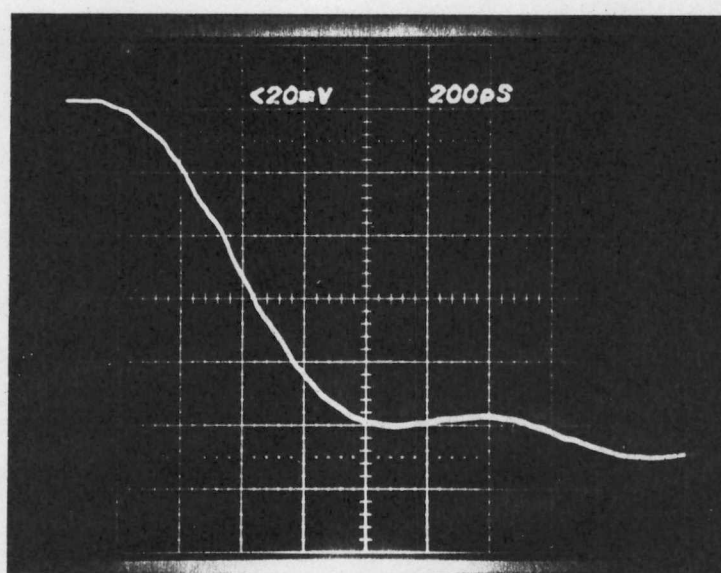


Figure 5.10. Timing loop output leading edge.

TABLE 5.2

TIMING LOOP OUTPUT VOLTAGE FOR A 10MeV EQUIVALENT
INPUT PULSE DERIVED FROM A LASER DIODE PULSER

C_{DETECTOR}	T_{OUT}
10.3pF	-56mV
55 pF	-30mV
100 pF	-19mV
209 pF	-12mV

$$A_T = \frac{E_O(\text{mV})(C_{IN} + C_{DET})}{E_{IN}(\text{MeV})}, \quad (5.2)$$

where C_{IN} is given in pF. The results are shown in Table 5.3. The results vary due to the significance of the input capacitance. The average value is $0.48\text{V/MeV}/C_{TOT}$ where C_{TOT} is the sum of C_{IN} and $C_{DETECTOR}$. The calculated value was $0.512\text{V/MeV}/C_{TOT}$. The actual value is approximately 5% lower than the predicted value.

The equivalent input noise voltage is measured using the configuration shown in Figure 5.11. The residual system noise (the rms output noise voltage with the wide band amplifier input terminated in 50Ω) is first measured and recorded. The total system noise is measured with various values of test capacitors connected to the preamplifier input. The total output rms noise voltage is shown in Table 5.4. As expected, this value is independent of capacitance. The minor variations are probably due to stray pickup which is influenced by how well the capacitors are shielded. The residual system noise is subtracted from the total output noise voltage to determine the output noise voltage due to the preamplifier alone. The total system output noise voltage due to the preamplifier is 0.81mV . The output noise of the preamplifier as measured at the noise meter input can be referred to the output of the preamplifier by dividing by the amplifier gain. This result will be the preamplifier rms output noise as measured over a fixed bandwidth. In this case it is the noise bandwidth of the noise meter which is approximately 28MHz . In general, the noise meter bandwidth will not be the

TABLE 5.3

TIMING LOOP CONVERSION GAIN AS CALCULATED FROM
TABLE 5.2 USING EQUATION (5.2)

C_{DETECTOR}	A_T	$\frac{\text{mV} \times \text{MeV}}{C_{\text{TOTAL}}}$
10.3pF		463
55 pF		492
100 pF		468
209 pF		515

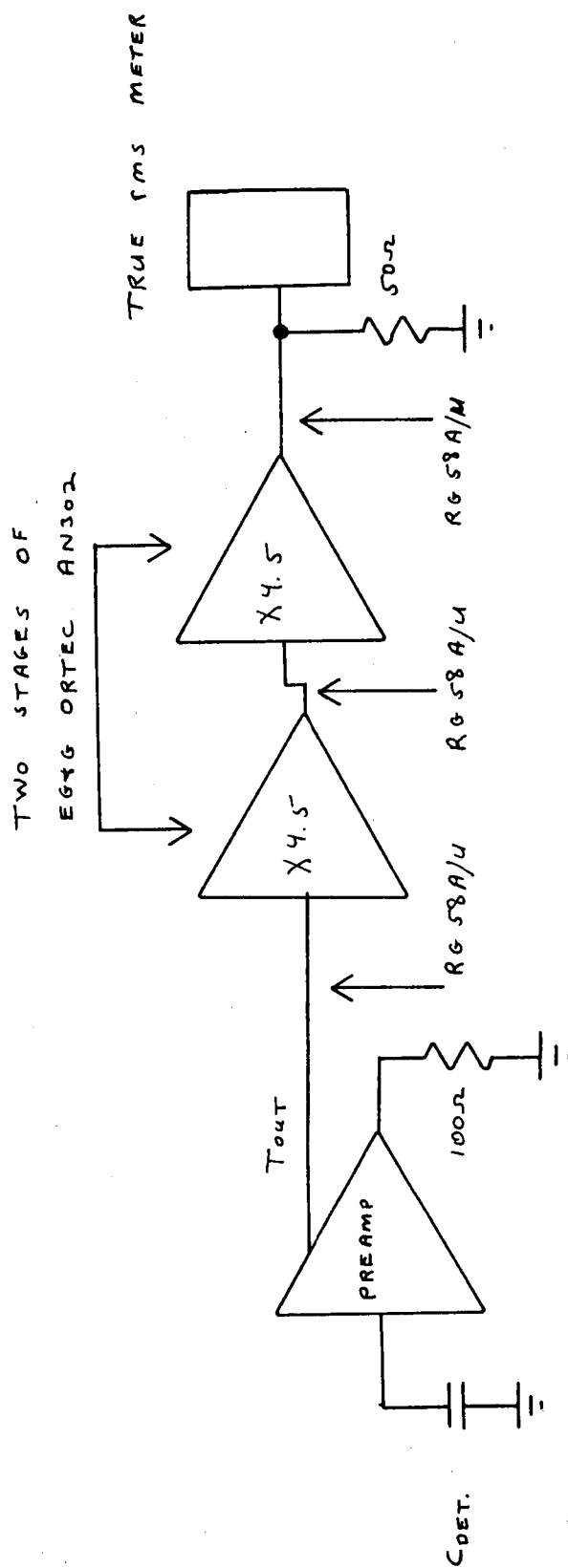


Figure 5.11. Circuit closed to measure the timing loop noise.

TABLE 5.4
TOTAL SYSTEM OUTPUT NOISE AS A FUNCTION
OF DETECTOR CAPACITANCE

C_{DETECTOR}	SYSTEM OUTPUT NOISE
0pF	0.86mVrms
100pF	0.87mVrms
200pF	0.86mVrms
500pF	0.85mVrms
1000pF	0.84mVrms

limiting bandwidth as much smaller bandwidths are generally desirable. Due to the wide bandwidth of the preamplifier under test, it was desirable that the noise measurement be made over as large a bandwidth as possible. The bandwidth of the additional gain stage is much greater than that of the H.P. 3400A true rms meter. Therefore, the limiting bandwidth is the high frequency noise corner of the H.P. 3400A and the low frequency noise corner of the preamplifier. The low frequency noise corner of the preamplifier is

$$f_{\text{LON}} = \frac{2}{\pi} \frac{0.159}{\tau_{\text{diff}}} \quad , \quad (5.3)$$

and is equal to 2.02MHz. The high frequency noise corner of the H.P. 3400A used in the measurement was measured and found to be 28MHz. The actual noise bandwidth is the difference between the high and low frequency noise corners. This value is 26MHz. The preamplifier output noise is 40 μ V as measured over a 26MHz bandwidth.

The equivalent input noise is found by dividing the preamplifier output noise voltage by the voltage gain from the input to the output. This value is approximately 11 as measured in the previous section. The equivalent input noise voltage is 3.64 μ V as measured over a noise bandwidth of 26MHz. The equivalent input noise voltage is of little importance due to its units. The value can be raised or lowered by changing the measurement bandwidth. A more useful set of measurements is the input noise power spectral density with units of V^2/H_z and the equivalent input noise resistance. The equivalent input noise resistance is the value of resistance that would produce the same output noise voltage if the amplifier is totally noise free. The input noise power spectral

density can be found from the input noise voltage and the bandwidth over which it was measured. For the value of equivalent input noise voltage and the bandwidth of the measurement, the input noise power spectral density is $5.086 \times 10^{-19} \text{ V}^2/\text{Hz}$. The equivalent series noise resistance can be found by dividing the above value by $4KT$. The equivalent series noise resistance is 30.7Ω . The predicted value for the input noise power spectral density is $6.478 \times 10^{-19} \text{ V}^2/\text{Hz}$. The calculated value of the equivalent series noise resistance is 39.12 . These values are approximately 30% lower than the calculated values. The lower values of noise resistance can be attributed to an FET transconductance that is higher than assumed in Chapter 3 and a Beta higher than the minimum value assumed for the second stage device.

The new preamplifier meets all design specifications. However, no measurements have been made to determine its true timing resolution. To determine the timing resolution requires an accelerator. However, an alternative method is available. A laser diode pulser has been used for experimental characterization of the timing resolution of detector preamplifier.¹⁰ This system was used to compare the timing resolution of the new preamplifier with that of a fast risetime compensated preamplifier. The system is shown in Figure 5.12. This measurement is not a measure of the timing resolution of the preamplifier as the detector contribution and the laser diode contribution cannot be subtracted. The electronic resolution can be measured and subtracted in quadrature. The electronic resolution was found to be 16.5psec. The values of detector capacitances used are 10pF, 55pF, 100pF and 209pF. The FWHM, $\text{FW } \frac{1}{10} \text{ M}$ and $\text{FW } \frac{1}{100} \text{ M}$ was recorded for each detector

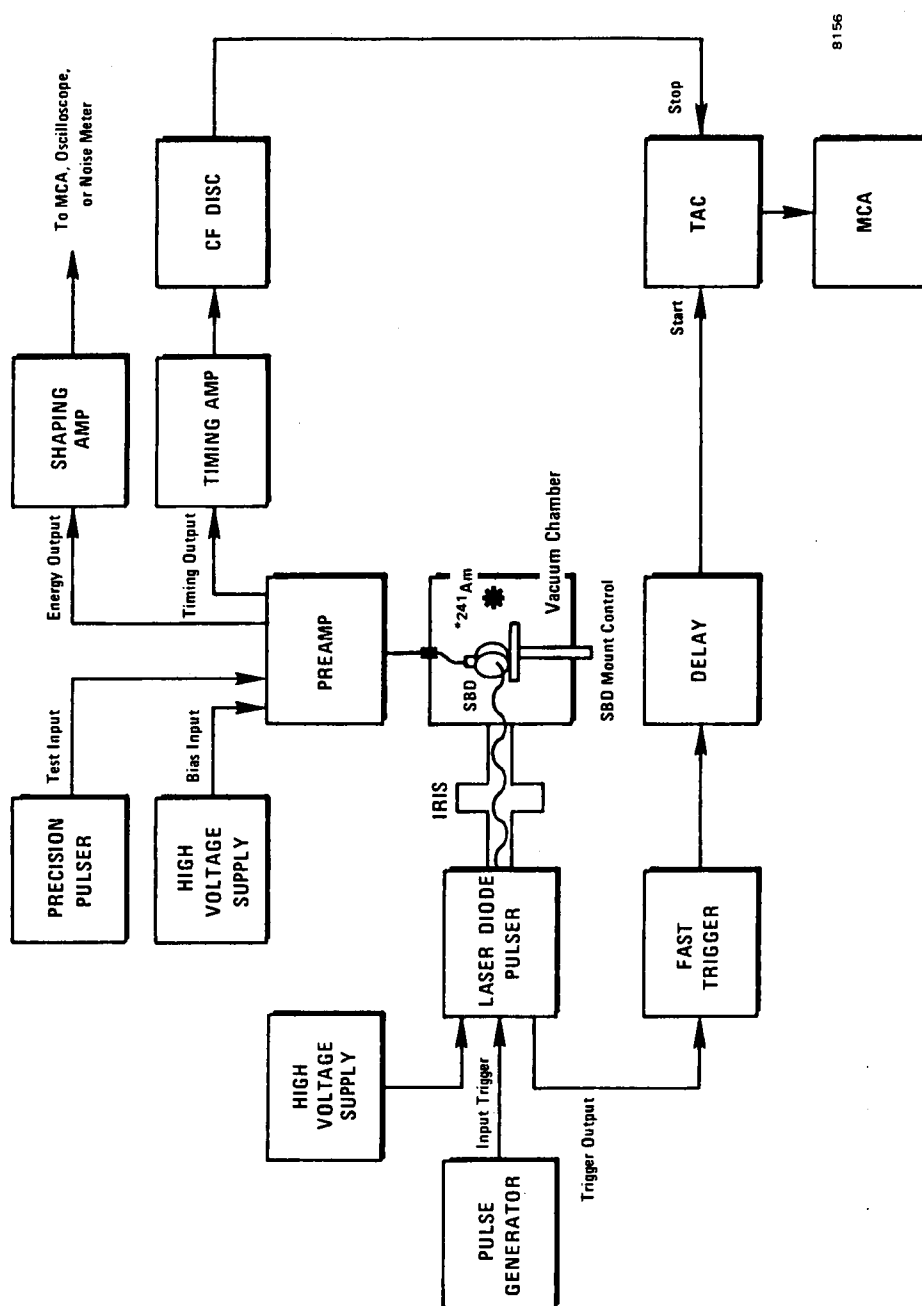


Figure 5.12. Timing system used with laser diode pulser.

at energies from 1MeV to 66MeV with each preamplifier. The results are shown in Figures 5.13 through 5.24. The dotted line represents the extrapolated data with the electronic system less preamplifier contribution removed in quadrature. As seen in each figure, the new preamplifier yields significantly lower results. The data converges at higher energies due to the overall system resolution as controlled by the laser diode and detector. The differences between the preamplifiers are clearly seen at the lower energies. At 1MeV, the new preamplifier is typically a factor of 2 better and at 10MeV a factor of 50%.

Conclusions

The new preamplifier is clearly superior to the fast risetime compensated preamplifier. However, the results obtained by using the laser diode pulser cannot be compared to the ideal numbers obtained in Chapter 3. The previous results on the timing section of the new preamplifier meets all specifications. The charge loop performs as expected and the combination of high performance charge loop and timing channel has been successfully integrated without sacrificing the performance of either channel. The next chapter will cover suggestions for further work.

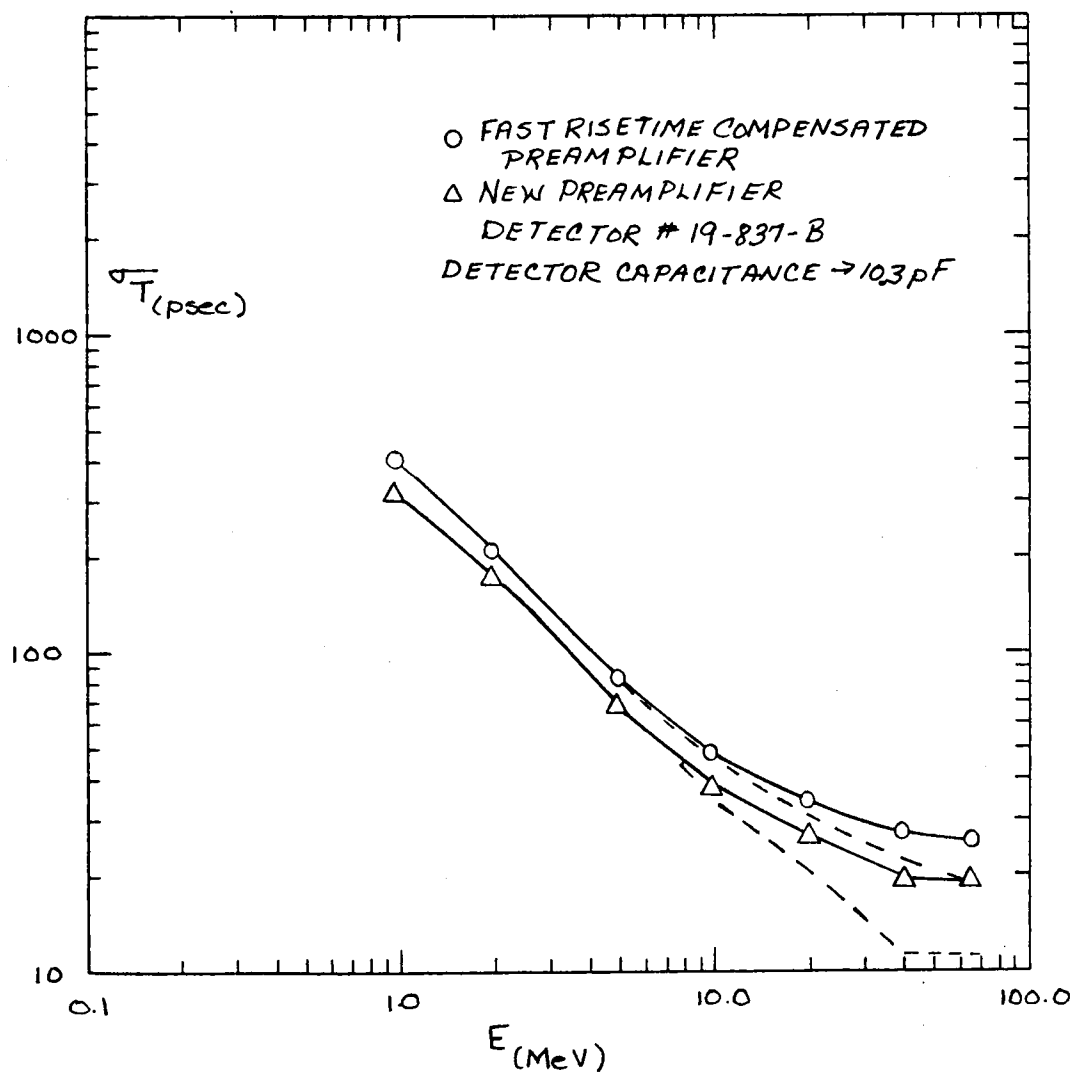


Figure 5.13. FWHM versus E , for a detector capacitance of 10.3 pF.

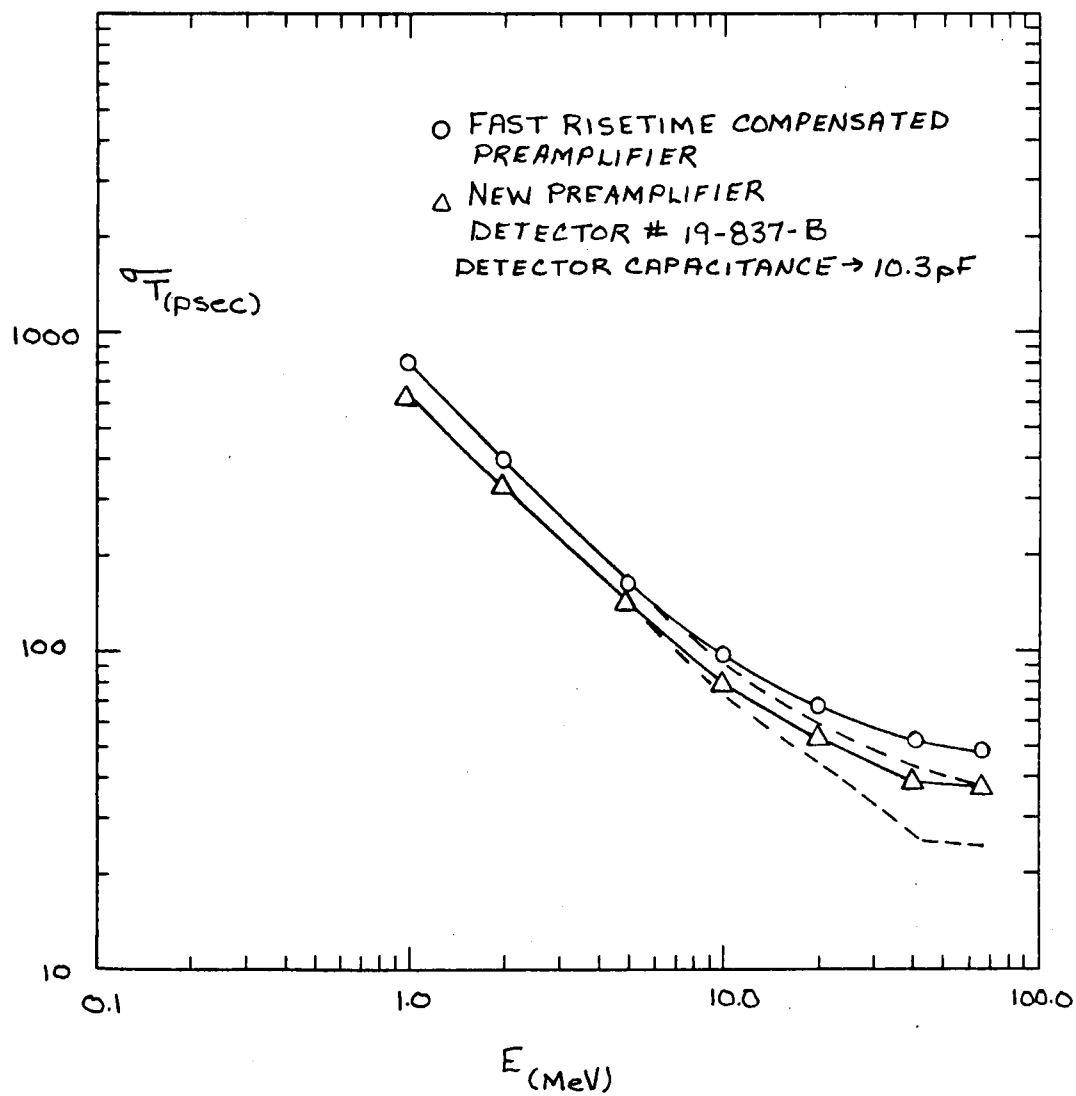


Figure 5.14. FW 1/10M versus E , for a detector capacitance of 10.3 pF.

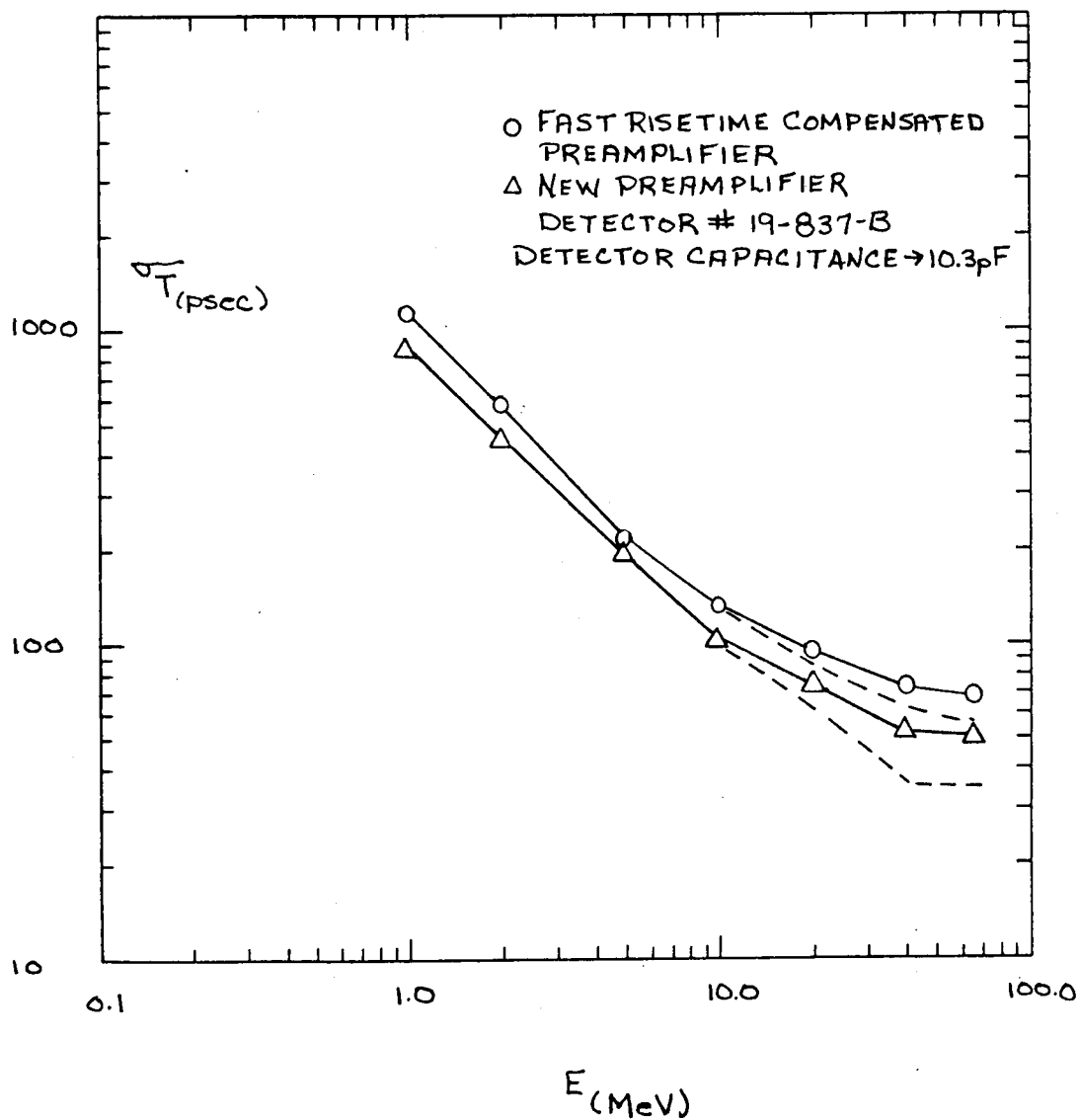


Figure 5.15. FW 1/100M versus E, for a detector capacitance of 10.3pF.

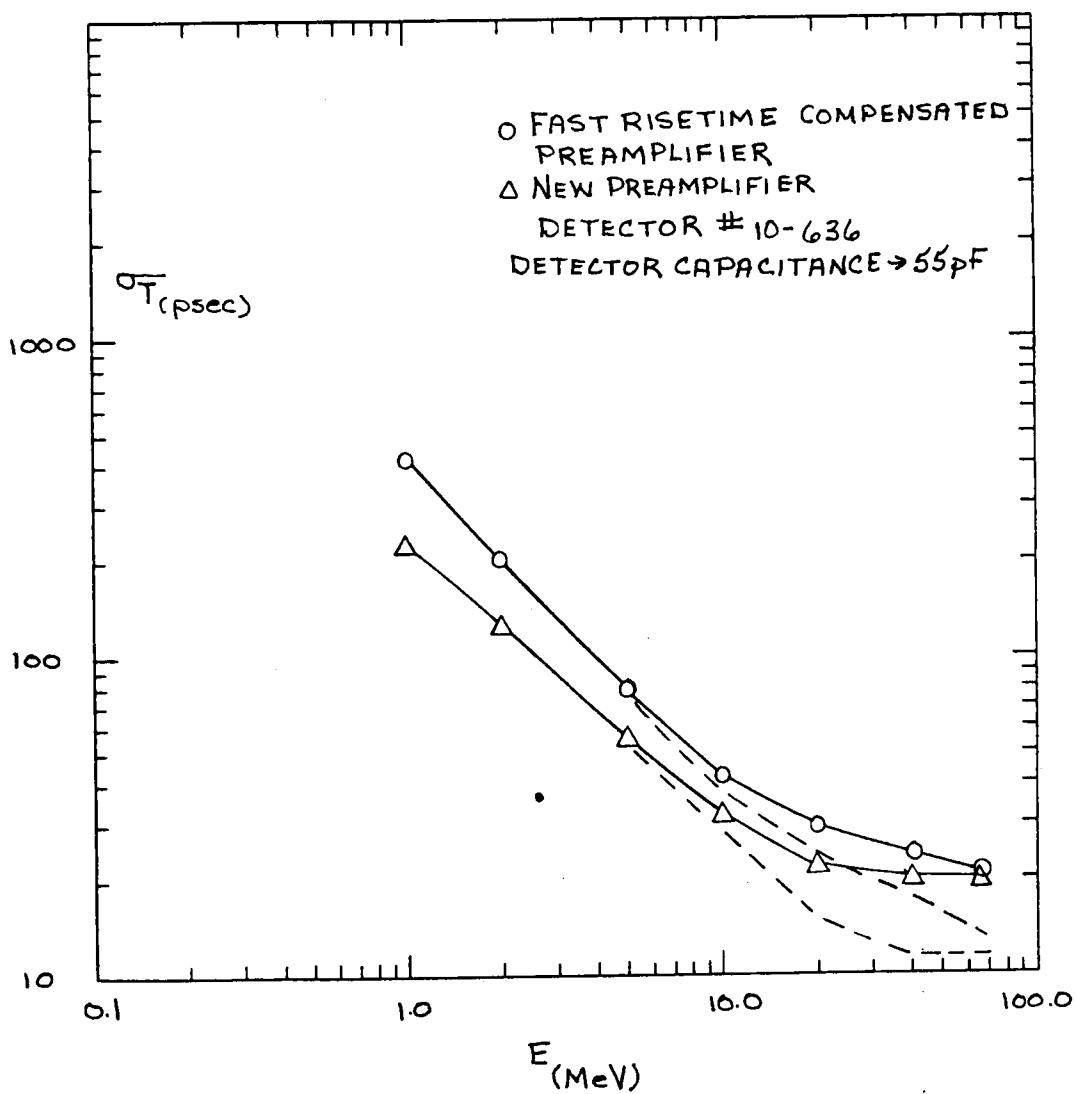


Figure 5.16. FWHM versus E , for a detector capacitance of 55pF.

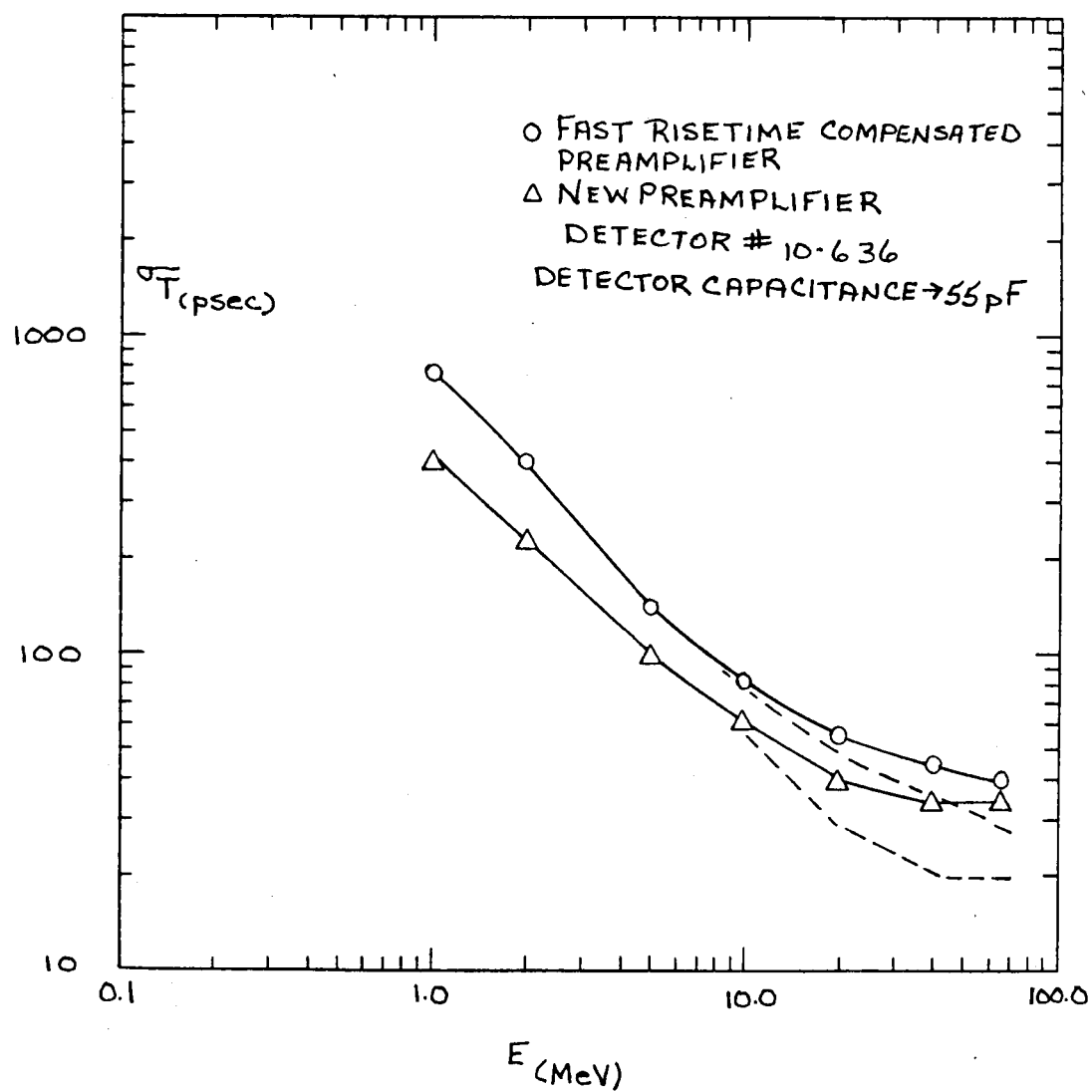


Figure 5.17. FW 1/10M versus E , for a detector capacitance of 55pF.

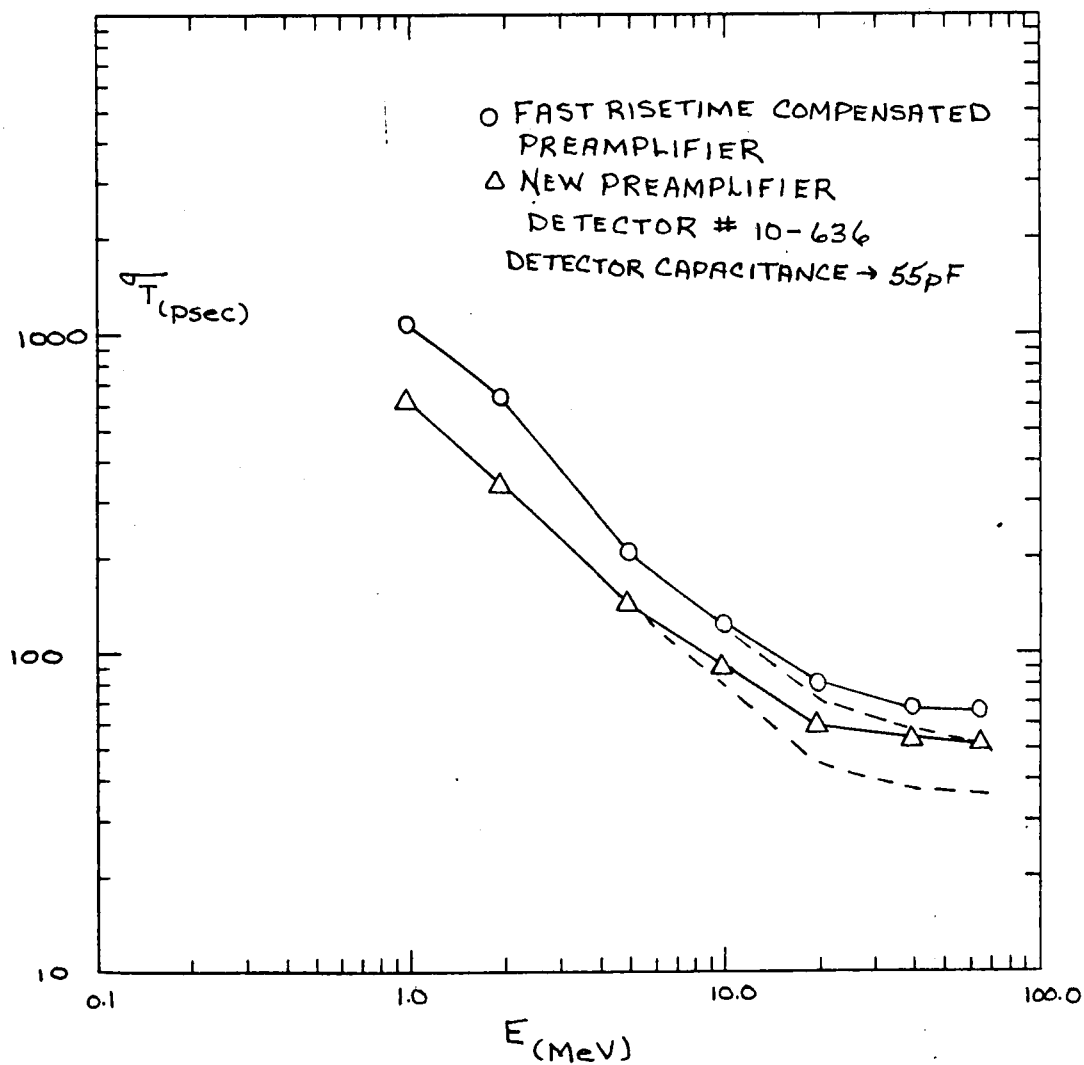


Figure 5.18. FW 1/100M versus E , for a detector capacitance of 55pF.

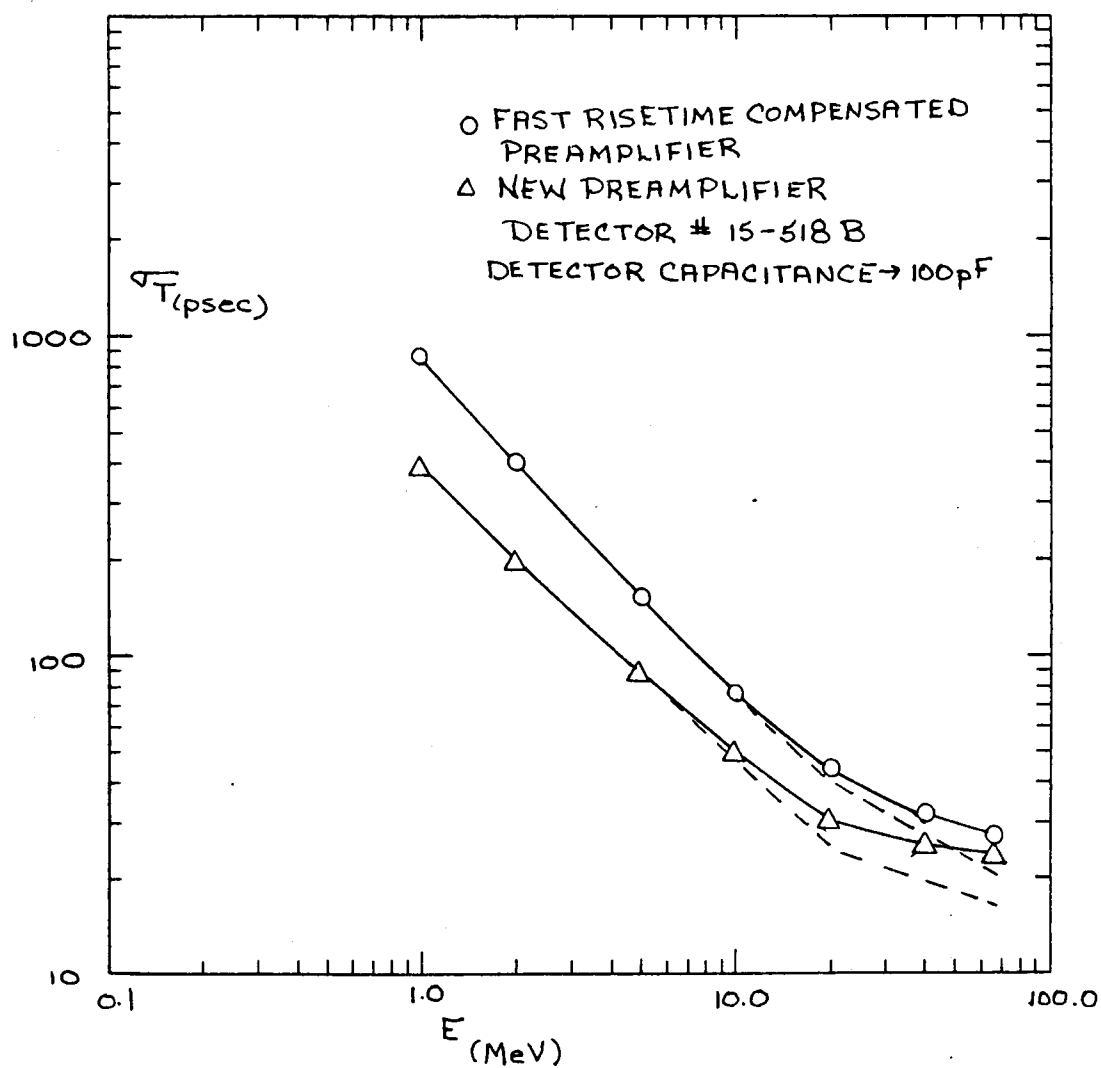


Figure 5.19. FWHM versus E , for a detector capacitance of 100pF.

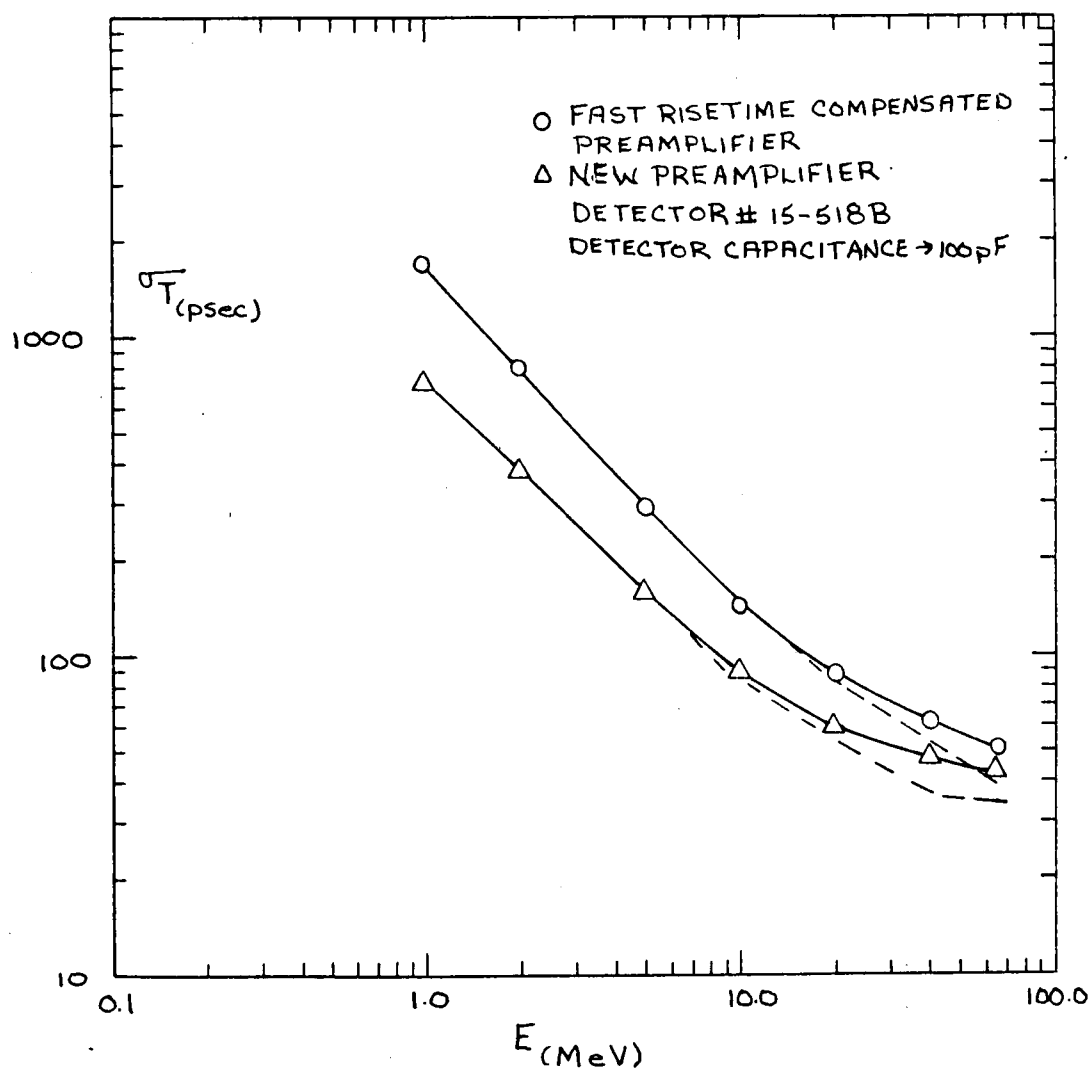


Figure 5.20. FW 1/10M versus E , for a detector capacitance of 100pF.

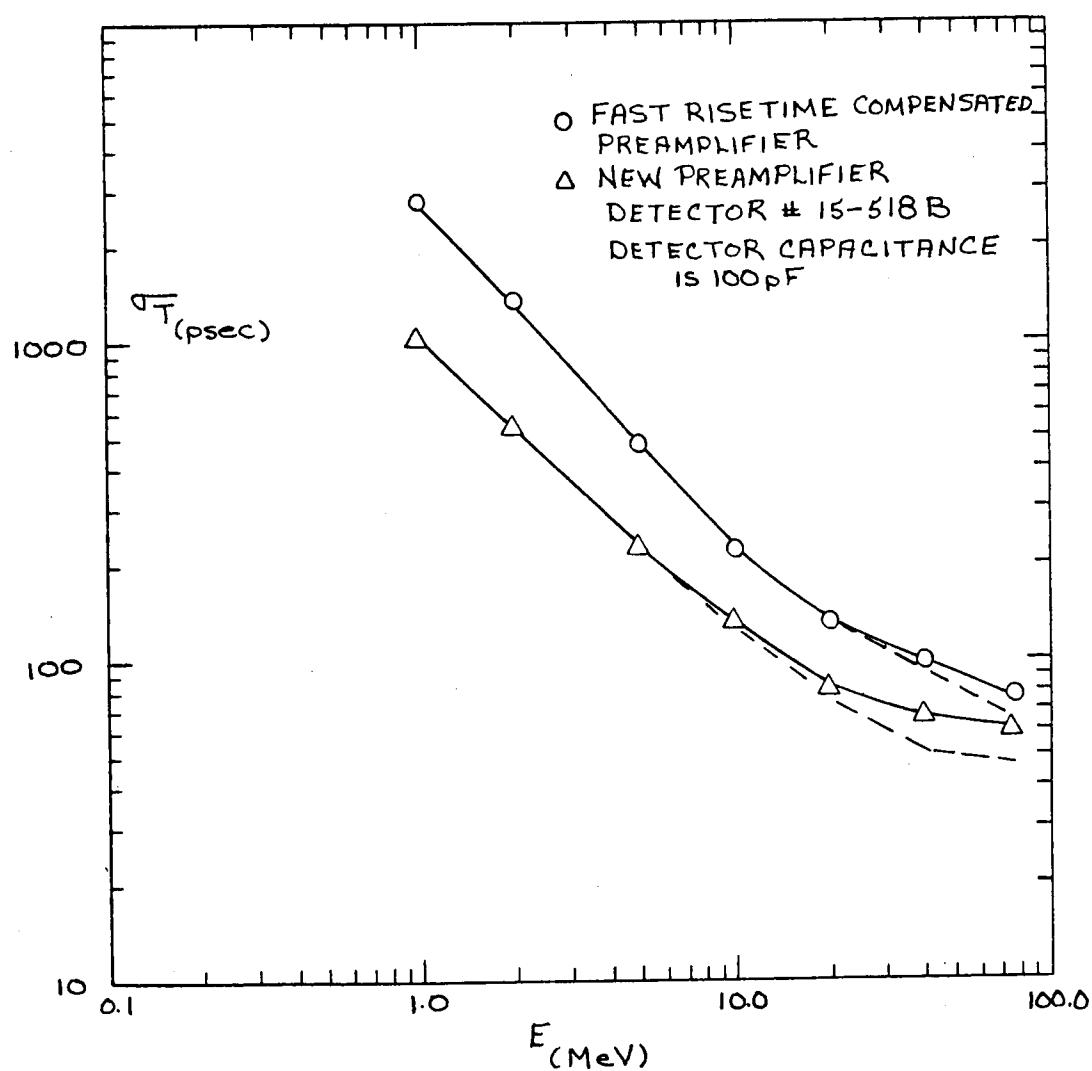


Figure 5.21. FW 1/100M versus E , for a detector capacitance of 100pF.

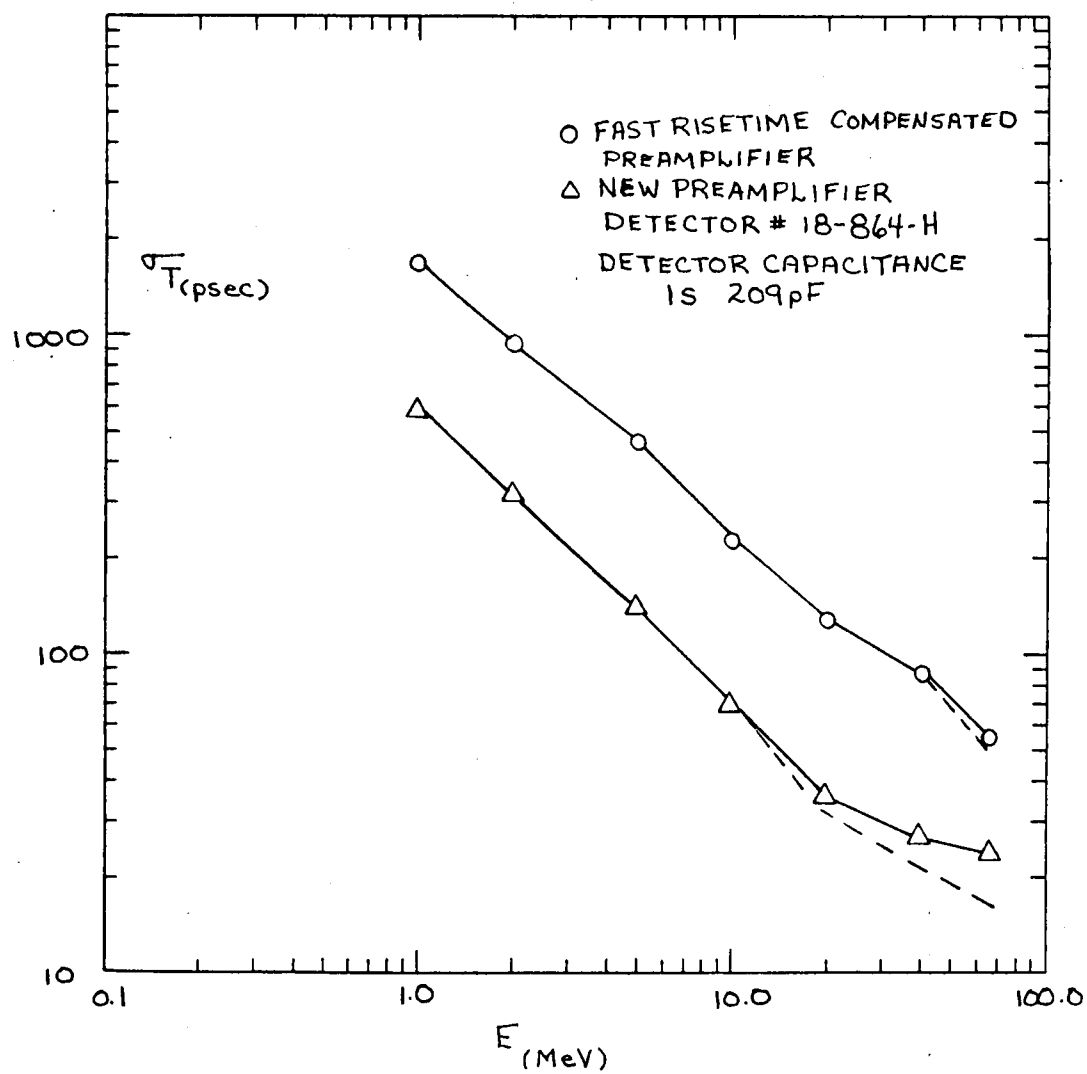


Figure 5.22. FWHM versus E , for a detector capacitance of 209pF.

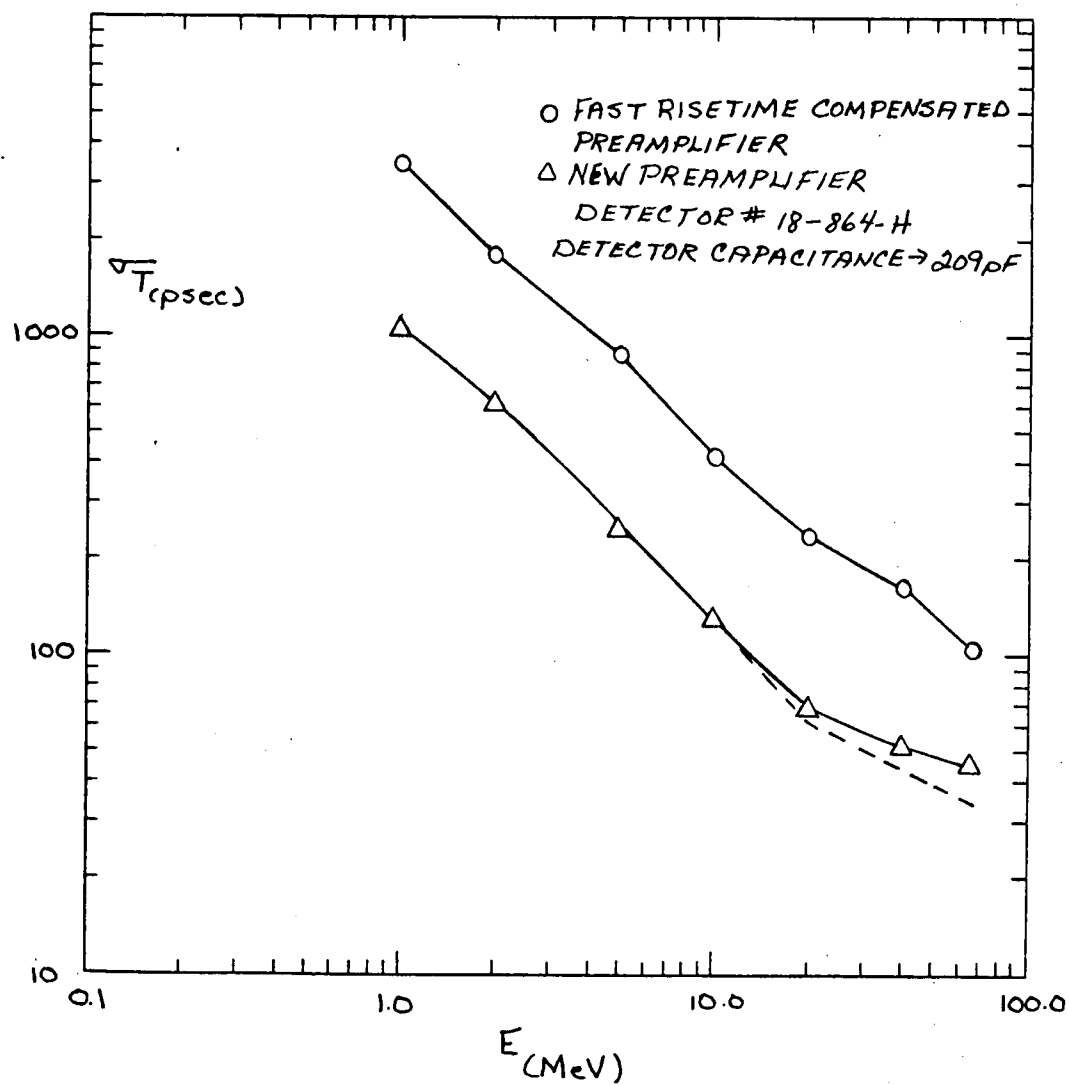


Figure 5.23. FW 1/10M versus E , for a detector capacitance of 209pF.

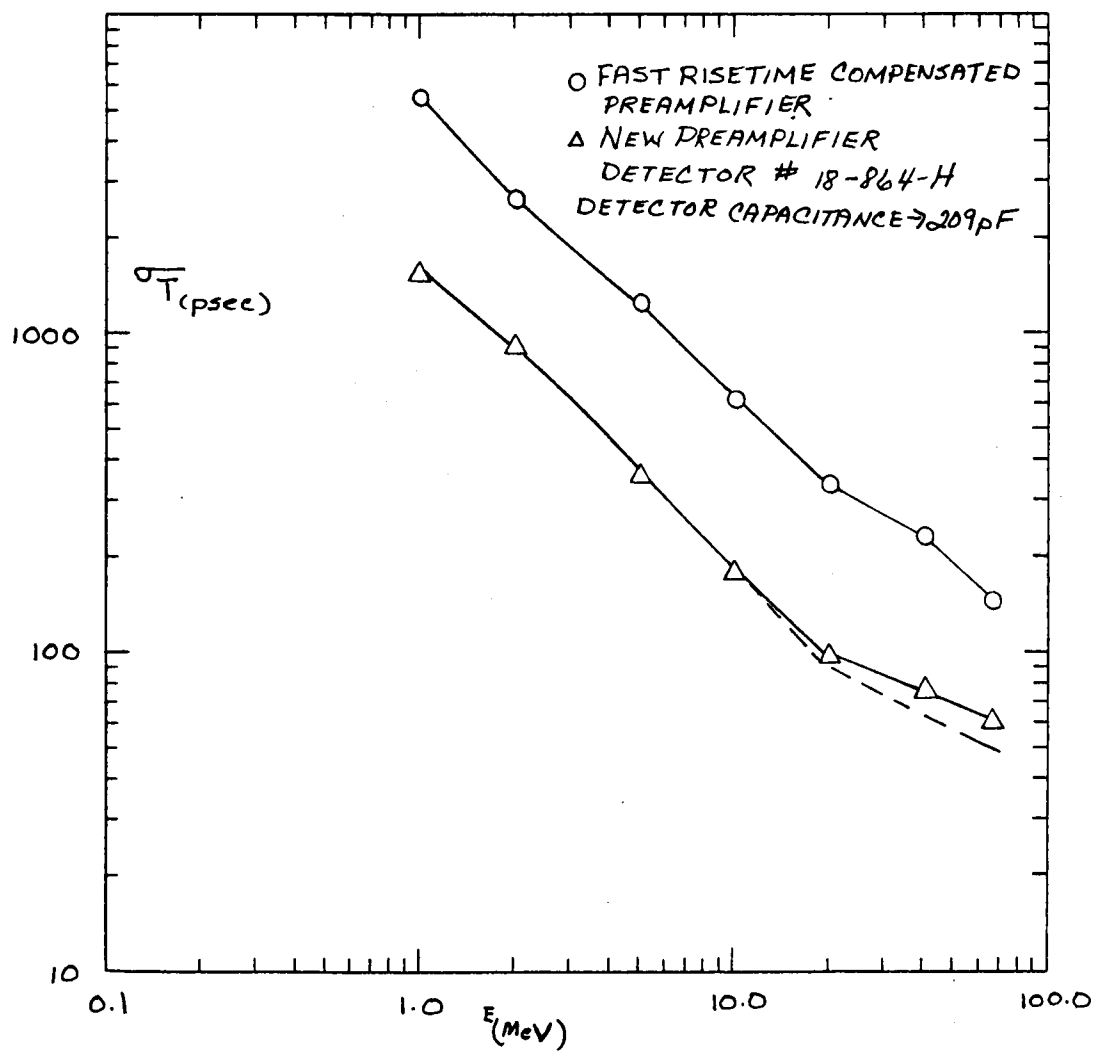


Figure 5.24. FW 1/100M versus E , for a detector capacitance of 209 pF.

CHAPTER 6

SUMMARY

The development of a charge sensitive preamplifier with a timing signal pick-off was covered in this study. The timing and energy resolutions of four different methods of deriving the timing signal were analyzed. The configuration that optimizes the timing resolution with no energy degradation was chosen. This amplifier was constructed using hybrid technology and tested. The new preamplifier timing resolution was compared to that of a fast risetime compensated preamplifier.

A chapter of this thesis was devoted to an analysis of the four methods of obtaining timing data. The four methods were: conventional charge loop, fast risetime compensated charge loop, parallel pick-off, and drain pick-off. The drain pick-off approach was chosen since the energy N.L.W. and timing resolution could both be optimized. Additional advantages of this approach over the parallel approach are lower component count, increased reliability due to fewer components, lower power requirements, smaller size, and lower cost due to lack of component duplication.

The third chapter of this thesis covered the actual design of the proposed preamplifier. The major specifications such as noise, resolution, and risetime were covered. The choice of input FET's was investigated using transconductance and risetime as a basis for type selection. The choice of current gain stages to provide the timing signal was investigated and a choice made based on the fastest risetime. The current gain stage was investigated in depth in a later chapter. After

the choice of the FET's and current gain stages was made, the complete charge loop was designed and the specifications summarized.

The current gain section was analyzed in greater detail in Chapter 4 by use of a computer simulation program. The program used was PCAP. The results were investigated for various values of input capacitance. The circuit chosen in Chapter 3 was the superior one, as verified by PCAP, though the performance was seriously degraded by input capacitance.

The circuit design was constructed utilizing hybrid technology and tested. The results were presented in Chapter 5. The design goals were satisfied and the results agreed very closely with the predicted values. The most important test was the timing resolution as measured with a laser diode pulser. The timing resolution was compared with that obtained using a fast risetime compensated preamplifier. The new preamplifier was significantly better. The absolute timing resolution of the preamplifier alone could not be extracted from the system data. However, the overall performance indicated that the new preamplifier yields improved energy N.L.W. and timing resolution.

The overall performance of the preamplifier can be increased by several methods. The basis for further work is the selection of an input FET with higher transconductance and lower risetime. The lower risetime will reduce the timing resolution slightly due to the small contribution of the FET. The higher value of transconductance would result in a lower noise voltage for both the timing and energy channels. The larger value of transconductance would result in lower timing

resolution and energy N.L.W. In addition, the higher transconductance would result in a larger timing output signal and a corresponding higher slope. The higher slope will yield improved timing performance. If a higher transconductance FET is used, the timing resolution can be further decreased by use of a common-base stage between the FET and the current gain stage. The common-base stage will reduce the total capacitance at the input of the current gain stage and decrease the risetime contribution of the second stage which is highly dependent on input capacitance. The most obvious problem with this approach is the inclusion of another source of noise near the input. The higher transconductance FET is required to offset the increased noise due to the common-base stage. Due to the level of performance obtained from the current gain stage, significant decreases in timing resolution by using different configurations is unlikely without serious redesign of the charge loop. The easiest way to improve the overall performance of the preamplifier is in FET performance. The results of an extensive evaluation of FET performance may yield a device more suitable than that used in this design, resulting in improved performance and the incorporation of a common-base stage.

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He is married to the former Linda K. Adams of Powell, Tennessee.