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Design of a High-Voltage, Differential Drive Bradbury-Nielsen Gate Amplifier with Ultra-High Slew Rate and Input Isolation

A Thesis Presented for the

Master of Science Degree

The University of Tennessee, Knoxville

Kevin Christopher Omoumi

May 2011

Acknowledgements

I would like to express my deep appreciation for the members of my committee for their support in completing this work and continuing to support and educate the engineers of the future; Dr. Benjamin J. Blalock, Dr. Syed K. Islam, and Dr. Leon Tolbert. In particular, I would like to give a special thanks to Dr. Blalock for his continued guidance and support with my education and work on this thesis. I would also like to give thanks to all ICASL colleagues, past and present.

I would like to extend a special thanks to Dr. Andreas Piechaczek of the Oak Ridge National Lab (ORNL) for his intellectual and financial support and guidance on this project. Without his dedication and support, this project would not have happened. Also from ORNL, I would like to thank Dr. Charles Britton for his intellectual support and assistance.

I wish to thank the members from RIS Corp. that provided abundant and valuable support, guidance, and suggestions. I would like to give special thanks to Allen Blalock and Dr. Richard Todd.

Special thanks go to my family, friends, and fiancée, who have always been unconditionally supportive of my decisions. Their caring hearts and love have carried me through the rough times, making all my accomplishments possible.

Abstract

To isolate and study various components of a nuclear reaction, elaborate equipment must be developed to aid in this process. This thesis presents the design and implementation of an ultra-high slew rate Bradbury-Nielsen gate driver circuit with high-voltage input isolation. This design will be used in a multi-pass time-of-flight isomer spectrometer and separator application integrated into an overall instrument called the Oak Ridge Isomer Spectrometer and Separator (ORISS). The output drive signals of this circuit are transmitted through a vacuum feed-through system to supply the necessary signals to the Bradbury-Nielsen gate contained within the vacuum. A differential driving signal with a 100-V magnitude and switching times on the order of nanoseconds is presented in this design. The "on time" of this signal is comparable to the amount of time required for it to transition states, creating complex design constraints. The implementation of this design is based on a 4-layer printed circuit board and the use of commercial off-the-shelf (COTS) components.

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Chapter 1

Introduction

1.1 Motivation

The possibilities for using the energy and byproducts produced in a nuclear reaction are practically limitless. Extensive research into the field of nuclear energy is being conducted worldwide. By better understanding the phenomena involved with these nuclear reactions, the results of such research could provide the ability to harness the energy yielded for the use of clean energy, transportation, portable power sources, and even weapons. A Bradbury-Nielsen gate (BNG) can be used in conjunction with other multi-pass time-of-flight (MTOF) equipment to separate isomers from other impurities in an ion beam producing a pure beam of that isomer. Isomers are chemical species with the same molecular formula but possessing different properties due to the altered arrangements of their atoms [1]. Isomers are used in many applications across countless fields from the medical realm to the food industry. The possibility of discovering or isolating an isomer with unique properties could be groundbreaking.

1.2 Overview

This thesis presents the design and implementation of a high slew rate Bradbury-Nielsen gate driver circuit for a multi-pass time-of-flight isomer spectrometer and separator application. These electronics are part of an overall instrument called Oak Ridge Isomer Spectrometer and Separator (ORISS).

The remaining five chapters of this thesis present the research and design required to develop an overall solution to the design problem presented later in this paper. Chapter 2

explores the underlying physics of the system in which these electronics will be integrated. A previous design solution is also explored in this chapter.

Chapter 3 provides a design overview including the various stages needed for the overall circuit. The constraints of the design are also discussed in this chapter.

The implementation of the design is discussed in detail in Chapter 4. This chapter includes topics such as specific design considerations, component selection, simulation results, and board layout techniques.

Chapter 5 presents the test setup used along with results measured during testing of the electronics system.

Conclusions of the thesis are given in Chapter 6. Future work to be conducted is also discussed in this chapter.

Chapter 2

Background and Existing Electronics

2.1 Ion Optics

ORISS is used to produce pure beams of isobars and enrich or fully separate isomers. This research will provide support for scientists to study the decay of unstable nuclei that are in unexplored regions of the chart of nuclides. Since some nuclides (species of atoms) decay with a very fast half-life, making them hard to study, the separation of long-lived isomers is important to be able to research their properties [2].

This system should have a high mass resolving power while maintaining a high transmission percentage and small footprint. Mobility makes this isomer separation solution much more versatile and capable of performing multiple tasks. Since the footprint of this system is relatively small, the system can be moved or reoriented if needed to comply with new system components. ORISS should allow for the continued study of exotic nuclei's decay spectroscopy [2].

The Bradbury-Nielsen gate driver electronics are essential to the ion optics of the ORISS project. In this multi-pass time-of-flight mass separator (MTOF-MS), ions are excited from a source on one end of the separator system. These ions should subsequently all have the same energy. The ions then pass through a series of electrostatic mirrors and lenses. The group of ions is reflected back and forth between these mirrors in a periodic manner hundreds or even thousands of times. Since the ions have the same energy but some have more mass, ions with more mass should have less velocity. Since these ions are all traveling in a fixed path through a vacuum, a spatial separation between different ions forms. Once enough separation has been

incurred between each ion of interest, all the ions are allowed to pass through the electrostatic mirror. At this point, they are traveling toward the separator. In this case, the Bradbury-Nielsen electrostatic fast ion gate is used for ion separation [3]. The BNG is further discussed in the next section. Figure 2.1 and Figure 2.2 show two similar system-level diagrams of the various components of the process described above [4]. Additional resources can be reviewed in the Appendix.

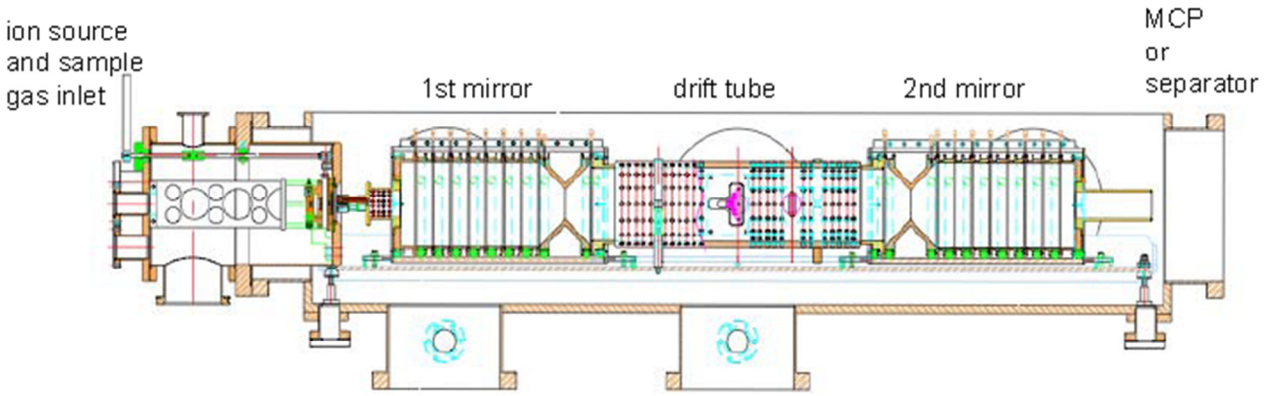

Figure 2.1: MTOF System-Level Diagram (reprinted with permission from A. Piechaczek [4])

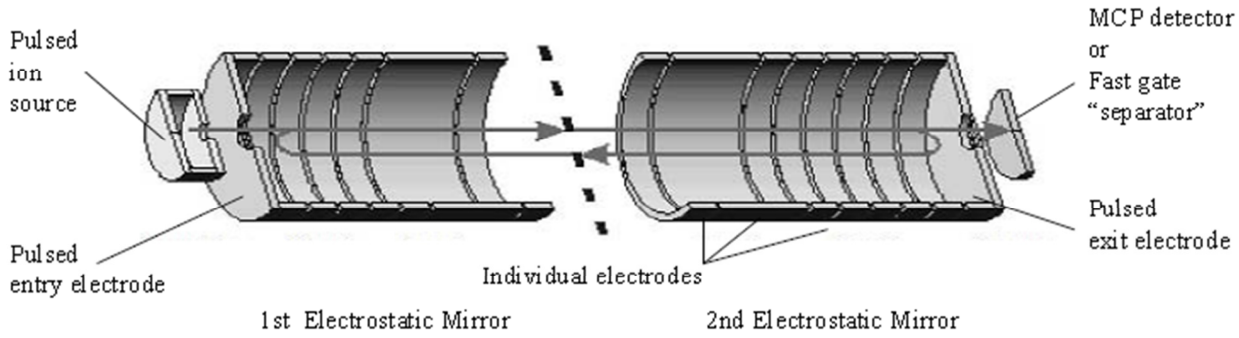

Figure 2.2: MTOF Trajectory (reprinted with permission from A. Piechaczek [4] [10])

2.2 Bradbury-Nielsen Gate (BNG)

The Bradbury-Nielsen gate is critical to the isomer separation process. When the ions are drifting at spaced out intervals due to the mass-induced variations in velocity, the BNG is expected to isolate specified ions based on the timing of their flight. The gate itself is two sets of interdigitated electrodes. They are in a parallel configuration and made up of very small and closely spaced wires. When no potential is applied to the gate, it is "open" and an ion beam can pass through the gate with no deflection. When a deflected signal is desired, alternate potentials are applied to each set of electrodes and cause the ions to be deflected from their intended trajectory. The deflection angle is mainly determined by the spacing and diameter of the wires and the voltage applied to each of the electrodes. By spacing thinner wires closer together, less voltage is required to cause deflection. In the same sense, the angle of deflection will be greater as the voltage applied is increased [5]. For this application, the complementary electrode voltages are 50 V. The BNG that is used has wires with a diameter of 10 µm that are spaced 100 µm from one another. Figure 2.3 shows how this deflection occurs [6].

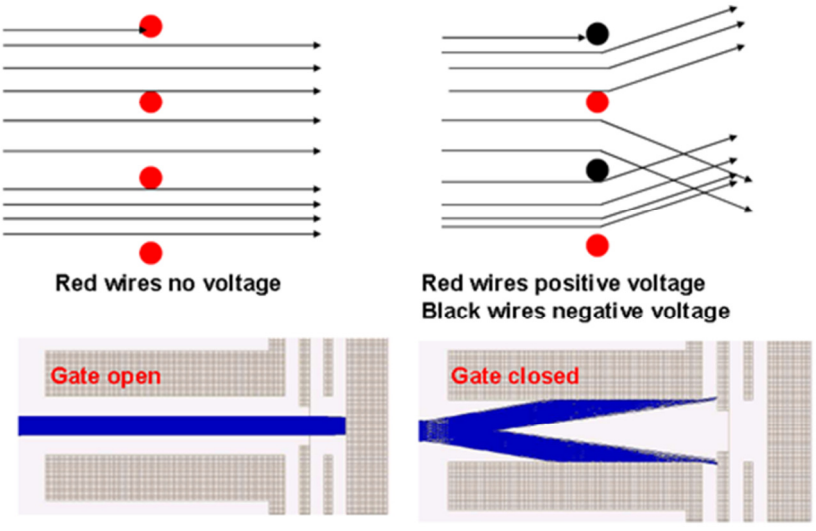

Figure 2.3: Bradbury-Nielsen Gate Ion Deflection (reprinted with permission from A. Piechaczek [6])

2.3 Previous Electronics Design

The previous electronics design was not sufficient at supplying the necessary differential output drive desired for the ORISS application. The output rise and fall times were drastically asymmetrical and the minimum pulse width was on the order of microseconds instead of nanoseconds. This design utilized an optocoupled input isolation scheme. The signal was eventually used to control two sets of complementary BJT pairs. In order to turn these devices on and off quickly, charge injection compensation techniques were used at the base of each device to obtain faster switching times. Simulations confirmed the operation of the output stage and are described in figures below (Figure 2.4, Figure 2.5, and Figure 2.6). The results are summarized in Table 2.1. This design is also limited to supply voltages with a maximum magnitude of 25 V. The absolute maximum rated collector-to-emitter voltage for the devices selected is only 40 V. Operating at voltages close to this value could damage the devices or cause the design to fail. Test results from this circuit were attempted. However, when the circuit was obtained and tested, there was a problem in the circuit and no output signals could be measured. Pictures of the previous electronics design are given in the Appendix. It can clearly be seen that the rise and fall times are very asymmetric.

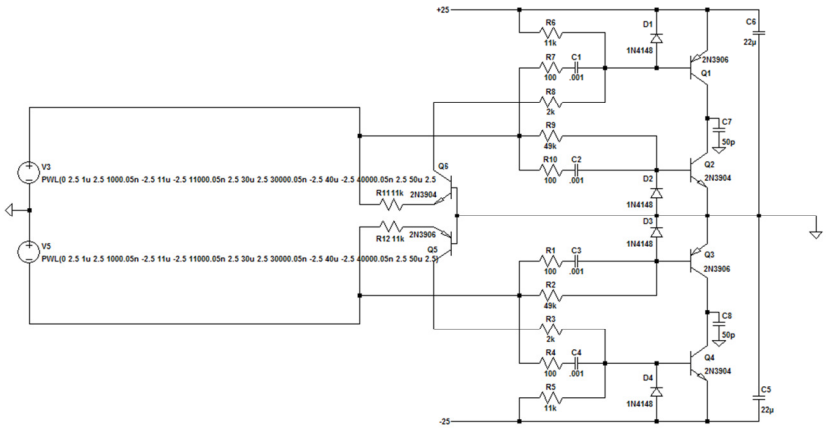

Figure 2.4: Simulation Schematic – Previous Electronics

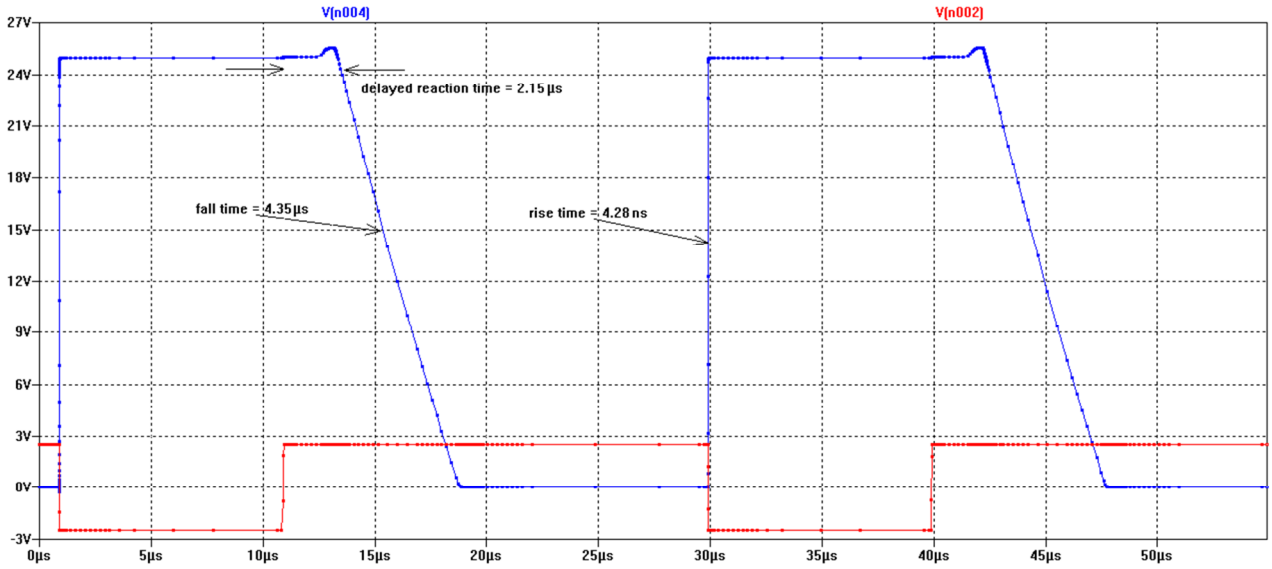

Figure 2.5: Positive-Side Simulation Results – Previous Electronics

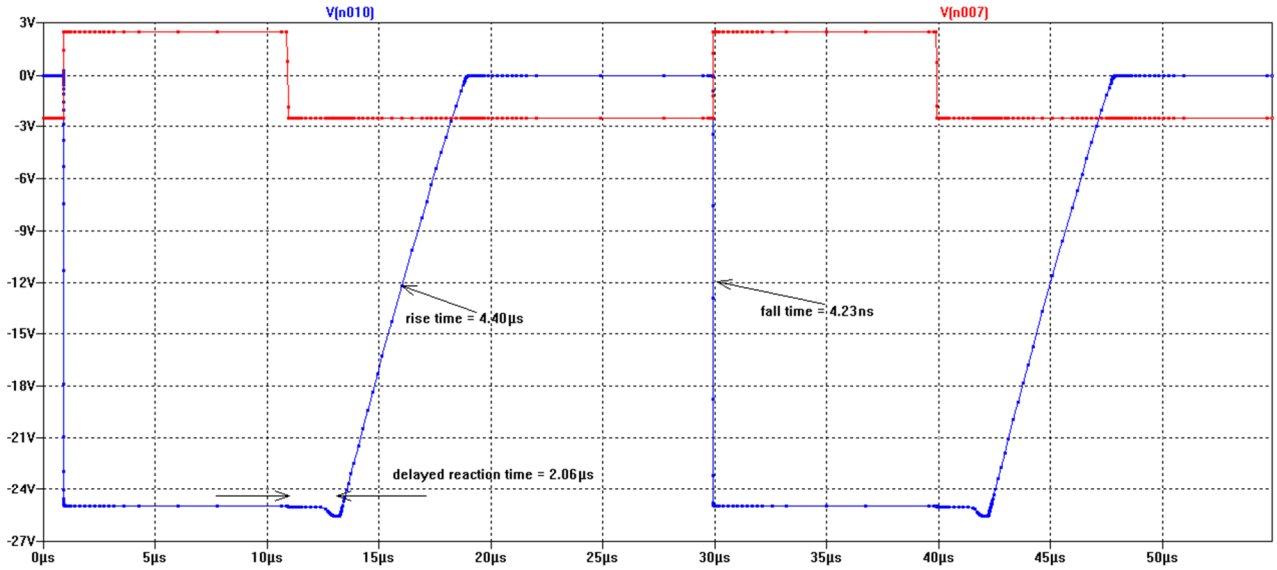

Figure 2.6: Negative-Side Simulation Results – Previous Electronics

Table 2.1: Simulated Rise and Fall Times – Previous Electronics

	Positive Side	**Negative Side**
Rise Time	4.28 (ns)	4.40 (µs)
Fall Time	4.35 (µs)	4.23 (ns)
Reaction Time	2.15 (µs)	2.06 (µs)

Chapter 3

Design Overview

3.1 Design Constraints

In order to drive the BNG, the electronics design requires a low-voltage transistor-transistor logic (TTL) signal (or combination of signals) input to produce fully differential high-voltage output signals. The output signals should switch in phase with one another and have complementary high and low voltage levels. The overall system should essentially act as a single-ended multi-input amplifier circuit with a differential output.

The existing electronics that are used to drive the BNG were insufficient for the amount of resolution desired for isomer separation. The updated design adheres to a tighter set of constraints to improve the separator resolution of ORISS. To operate well as an electrostatic gate and separate isomers, the output signals must be able to provide a "window" of time in which the ions can pass through to the detector, while deflecting the ions at all other times. These signals keep the BNG "closed" for the majority of time and have the ability to quickly "open" the gate for varied amounts of time. The "open" time is adjustable, but by having the smallest possible pulse width (PW), higher gating resolution is attainable. The required output signals are dictated by the specifications of this "window". The required voltage for an "open" gate is 0 V on both channels to allow for all ions to pass through the gate undisturbed. For nominal operation, the "closed" voltages are at complementary levels of 50 V (one channel at +50 V and the other at −50 V) for ion deflection. Adjustable output signal voltage levels down to a minimum magnitude of 25 V may be desired for future revisions of the ion optics solution. For this reason, the ability to adjust the output signal voltage levels should be considered when designing the power supply

network and choosing the output stage devices. Since the common point of the output is level shifted by several hundred Volts, input isolation is desired, in addition to an abundant margin for safety, to approximately 2 kV. For minimum operation requirements, at least 600 V of input isolation is required.

For optimum operation, the output signal rise and fall times (measured 10 to 90 percent) are approximately 15 ns, or less, for each 50 V signal. These essentially translate into very quick turn-on and turn-off times for the BNG. In order to have very good isomer separation resolution, the pulse width of the output signals needs to be minimized. Typical pulse widths can range between 10 ns and 10 μs. The repetition rate at which the gate needs to be "opened" and "closed" is typically 200 Hz. The maximum rate at which the gate will be operated is 10 kHz. Regardless of the repetition rate, the duty cycle always remains under five percent. In most cases, the duty cycle is less than one percent. To provide proper impedance matching for the termination of the input control signal, the input impedance for the final design is 50 Ω. Jitter (timing uncertainty) in the output signals must also be at a minimum, ideally less than 10 ns. All constraints for the design are summarized in Table 3.1.

Table 3.1: BNG Driver Design Constraints

Parameter	**Value**	**Units**
Isolation Voltage (desired)	2	kV
Isolation Voltage (required)	600	V
Supply Voltages	±50	V
Rise/Fall Time (10-90%, 0-50 V/50-0 V)	15	ns
Pulse Width Minimum	10	ns
Pulse Width Maximum	10	μs
Frequency Range Minimum (typical)	200	Hz
Frequency Range Maximum	10	kHz
Input Impedance	50	Ω
Jitter	< 10	ns
Duty Cycle	< 5	%

3.2 System Level Design Overview

An electronics system of this complexity needs various stages to accommodate for each of the project parameters. An input stage is required to provide the necessary isolation voltage as well as input signal termination. Once the signal is received on the board and input isolation is provided, the drive strength of the signal is increased so that the output stage has sufficient drive to develop fast switching edges. The output stage is necessary to obtain the high-voltage output signals that are desired to drive the BNG. These three stages will provide a basic signal path from the input to the output of the system. However, another critical element of this design is the power supply network. Each of the three stages described above must have appropriate power levels supplied to them. All of these design aspects are described in further detail in the following sections. A system-level diagram is given in Figure 3.1. A segmented overview of the board layout is shown in Figure 3.2. The details of this design and layout will be discussed in Chapters 3 and 4.

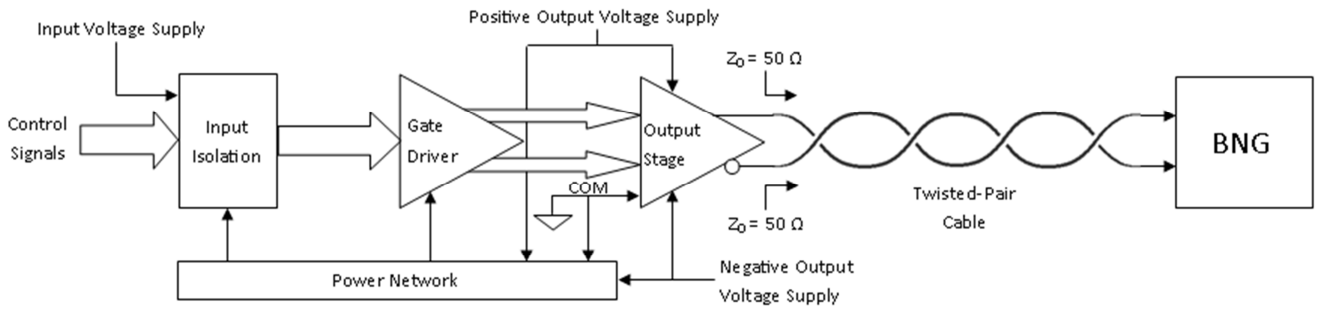

Figure 3.1: System-Level Block Diagram

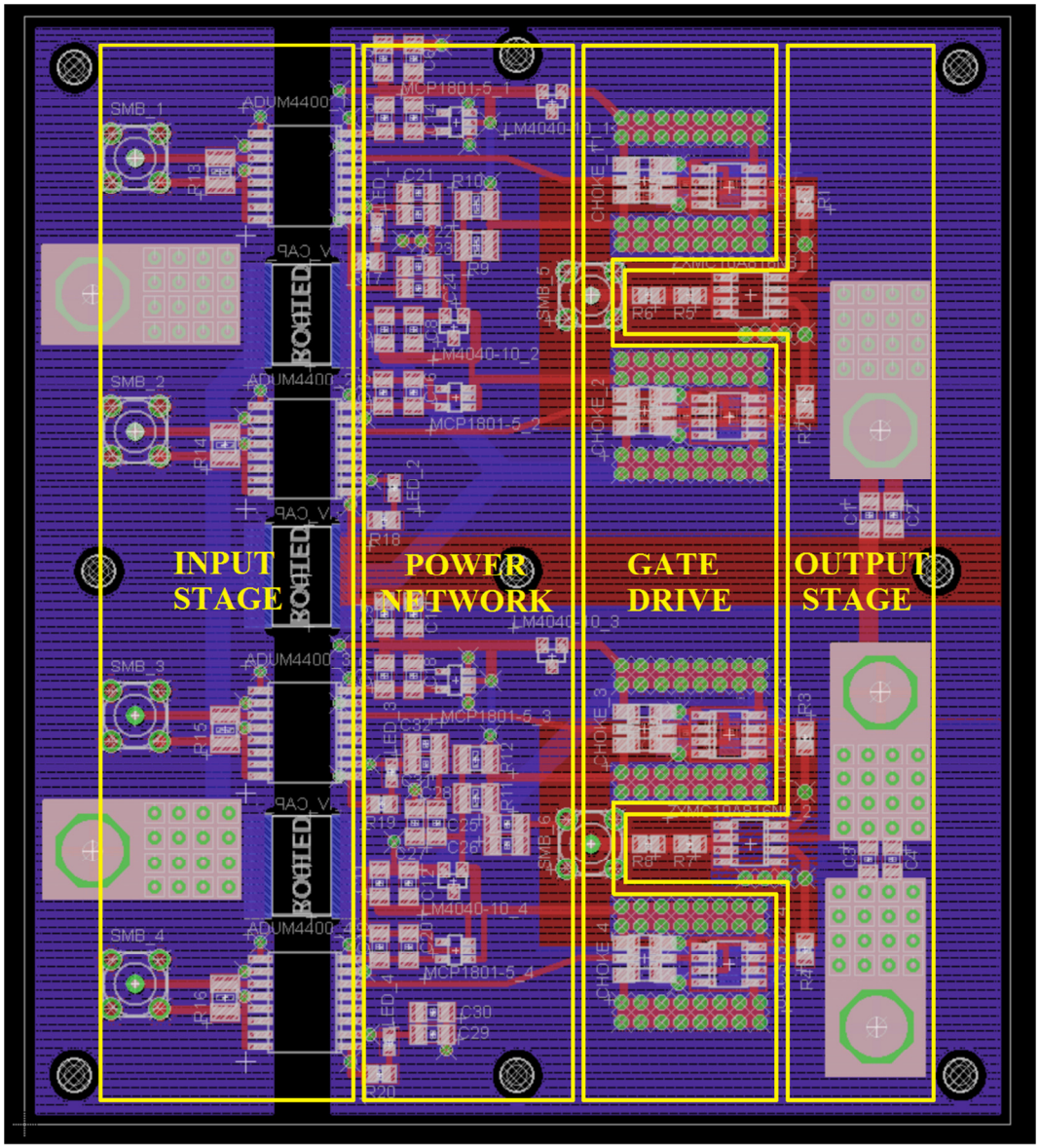

Figure 3.2: Segmented Overview of the Board Layout

3.2.1 Input Stage

The optimum solution for the ion optics requires that the output signals supplied to the BNG be level shifted by several hundred volts. Since this is a critical aspect of the overall application's solution, it must be incorporated in the design of the BNG driver electronics. An isolation voltage of around 600-V DC is absolutely critical for the solution derived from the ion optics, while at least some margin above this value is desired. This voltage becomes the common

potential for all of the electronics that will be isolated from the input. The ideal isolation voltage is 2-kV DC. However, this amount of isolation voltage may be difficult to obtain while still considering all other design constraints. This is discussed in further detail in later sections.

In addition to the input isolation, the input stage must also transmit the undistorted input signal(s) from a signal generator to the rest of the electronics. For appropriate impedance matching, the input signal(s) should be 50 Ω terminated. Most signal generators have output impedance adjustment in which the load conditions can be specified. By setting the expected load to 50 Ω and specifying an input impedance of the same value on the board, the voltage levels can be set accordingly. One way that a signal generator could accomplish this type of termination is by the method of resistive voltage division. The signal produced by the generator is designed to supply a voltage, V_{SIGNAL}, to a 100-Ω load. If this signal is transmitted to a system with a 50-Ω input impedance through a 50-Ω series resistance, then the resulting signal is matched and has a voltage level of $V_{SIGNAL}/2$. This method is implemented as part of the input stage and can be observed in Figure 3.3. However, additional design considerations must be made to determine the specific input signal(s) needed. This topic will be addressed in Chapter 4.

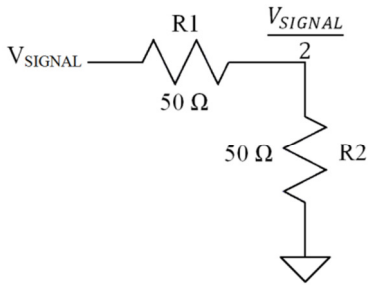

Figure 3.3: Input Signal Matching

3.2.2 Output Stage

For this application, two single-ended signals are combined to form one differential output. A maximum output signal magnitude of 50 V is required by each side to drive the BNG. In order to maintain such high voltages, power transistors will be needed. By using complementary MOSFET transistors instead of complementary BJT transistors that were used in the original electronics output stage, the necessary voltage levels are obtained while maintaining very fast output signal rise and fall times. The output stage is configured in a push-pull configuration. This type of output structure will be used for both the positively and negatively oriented output signals. The RC network charge injection techniques used to improve the switching speeds in the previous design are not needed to obtain the necessary switching speeds in this configuration. Both the rise and fall times of each of the output signals should be improved and be much more symmetrical.

3.2.3 Gate Drive

High voltage capable transistors are essential for the output stage of this system, as well as the ability to rapidly drive a relatively large capacitive load thus power transistors are warranted. The input capacitance of most power transistors is substantial, so the input capacitance and maximum allowable drain-to-source voltage are two very important specifications to consider when selecting power transistors. If no additional drive capability is included in the input isolation design, an additional stage to increase the input signal drive strength is required to properly control the output stage. One method for providing such drive is by using four separate gate drivers with level shifted supply voltages for each of the power transistors in the output stage. Chapter 4 describes the method used to accomplish this.

3.2.4 Power Network

The power system design is critical for the BNG electronics to function properly. The circuit must be supplied with various voltages at positive and negative levels while sustaining large transient currents due to switching. When each output signal transitions from either high to low, or low to high, a large transient current spike is supplied by the power circuitry in order to maintain fast switching speeds. Fortunately, since these transients only last for very short periods of time, they can be supplied almost entirely by capacitive circuit elements. However, the quiescent current of the entire system must be supplied by a power network with a robust design that remains stable throughout these types of transitions. Since the output side of the electronics is electrically isolated from the input side, all voltages on this side are referenced to a common potential. For most simulation and testing purposes, this common voltage is ground. In the final system, this common potential will be around 600-V DC. The bias voltages and currents are established by a network of voltage references, linear regulators, resistors, and capacitors. These are all powered by a single common potential and two complementary voltages referenced to the common potential. In the general case, these voltages are ground (0 V), +50 V, and −50 V, respectively.

Chapter 4

Design Implementation

4.1 Signal Path Design Considerations and Selection Process

A great amount of research and consideration went into the selection of each of the components used in this design. The following sections highlight the main reasons that each device was chosen. There are four main channels used to create the differential output signal needed. One channel is used to drive the PMOS device on the positive side of the board, while another channel drives the PMOS on the negative side. Likewise, each NMOS is also driven by its respective channel. A more detailed block diagram has been provided in Figure 4.1 illustrating each of these individual channels. A single signal channel's path is highlighted on the board layout in Figure A.4 in the Appendix. The individual components that make up each channel are discussed in greater detail in the remaining sections of Chapter 4.

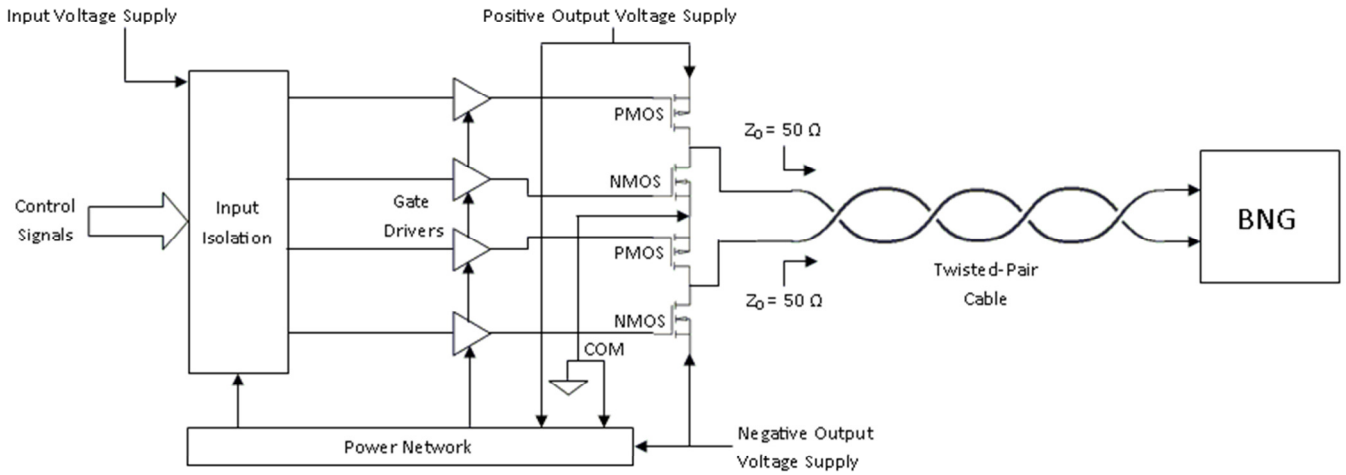

Figure 4.1: Detailed System-Level Block Diagram

4.1.1 Input Isolator – Analog Devices ADuM4400

Various methods of input isolation were considered for implementation of this design. The first type of input isolation reviewed is direct transformer-isolated gate driving. Transformers only couple AC signals and typically must have a 50 percent duty cycle so that the core flux can be reset [7]. Since this application requires a very low duty cycle and uses some control signals that very closely resemble a DC signal, this method of input isolation is not practical as a direct gate driving solution. The design of an elaborate modulation and demodulation scheme, and possibly another signal buffer stage, would be required in order to use a standard transformer as the input isolation. Another drawback inherent in the use of a commercial off-the-shelf (COTS) transformer for gate driving purposes is the amount of board area required to implement such a design.

The use of an optocoupler is another input isolation option. This method of isolation is the most common form used in applications today. An optocoupler transforms an input current into a light signal by using a light emitting diode (LED). This data is then transmitted across an isolation barrier and received by a phototransistor. The signal is then converted back into a current and the signal transmission across the barrier is complete, resulting in input-to-output isolation. Although optocouplers implement a very clever solution to provide input isolation, there are some inherent characteristics that make an optically coupled design less than optimal for this application. Optocouplers are very inefficient since the required current to provide a transmitted signal is on the order of milliamps. Typically, signal transmission refers to voltage referenced signals. By transmitting current based signals, additional design must be performed in order to obtain the necessary signals after transmitting across the barrier. A buffer amplification stage is also necessary in order to drive a power transistor with such a signal. Since timing and

reliability are critical for this application, a more reliable solution is needed. Optical coupling solutions have inherently long propagation delays which, along with other performance characteristics, degrade greatly with time and usage. This phenomenon is present in almost all electronic devices; however, the parameter variation in an optocoupler can greatly affect its performance over time [8].

Capacitive coupling was another consideration. This method also has an inherent flaw that makes it a poor choice for this application. It is very susceptible to common-mode transients [8]. This presents a high probability for false triggering. Since the isolation device must control the input signal(s), a signal sent throughout the circuit unexpectedly could be costly and catastrophic to the results obtained from the experiment. Since there was no integrated circuit (IC) that utilizes this technology found, an encoding and decoding scheme for the signals would be required on the board.

The iCoupler series seems to provide the most comprehensive isolation solution for the constraints of this project [7]. The specific iCoupler chosen was the Analog Devices ADuM4400, C grade. This device provides sufficient input isolation while accounting for most of the shortcomings inherent in the other input isolation methods that were considered. Its maximum working insulation voltage is 846-V DC while providing one of the shortest minimum pulse widths. Some devices that may have had shorter pulse widths could not support such a low duty cycle or operating frequency [9]. The ADuM4400 is essentially an on-chip transformer input isolation solution. However, the implementation of this device already includes on-chip encoding and decoding along with a refresh circuit that enables DC input signals [9]. This refreshing scheme also allows for input signals with a duty cycle much lower than the typical 50 percent required by transformer input isolation.

Since the iCoupler is based on transformer isolation technology, it remains reliable over time and has a very high common-mode transient immunity. One main characteristic that makes the ADuM4400 an optimal selection for this design is its minimum attainable pulse width. The typical pulse width limit for this device is just under 10 ns. This coincides with the minimum PW in the range of possible timing window sizes needed in this application. Since the minimum window size of the output signals is directly determined by the inherent delays and minimum specifications of each device throughout the rest of the circuit, the ADuM4400 will allow for a solution that can encompass the majority of the pulse width range. The isolation voltage of this device is well over the required 600 V. However, it does not provide an ideal amount of margin above this isolation voltage. After collaboration with the other members working on the overall system, it was decided that the benefits of this device outweigh the desire to have a higher isolation voltage.

Some iCoupler based devices incorporate gate drive capabilities in their design and were originally considered. However, none of these isolators had sufficient isolation voltage, drive strength, and minimum pulse width for use in this application. In some cases of gate driving devices, problems with false triggering can occur. This will be discussed in further detail later, but one way to prevent this possibility is to incorporate a common-mode choke into the design. If a single device is used for input isolation and signal drive, additional components such as the common-mode choke cannot be utilized.

4.1.2 Gate Driver – Texas Instruments UCC37322

The MOSFET gate driver is one of the most critical devices to be integrated into the signal path of the BNG driver. The gate driving device must be able to receive a level-shifted, low-voltage signal and produce a sufficient amount of charge to quickly turn the power

transistors (MOSFETs) on or off. For this application, the worst-case capacitive load that a gate driver must sustain is the intrinsic input capacitance of the PMOS device. The input capacitance is a combination of the gate-to-source and gate-to-drain capacitance, measured to be approximately 717 pF. The input capacitance of the NMOS device is substantially less at 497 pF. The output signal of the driver needs to have the fastest possible rise and fall times to enable the output stage to produce a signal that also has very fast switching speeds. The optimum gate-to-source voltage according to the manufacturer's datasheet is 10 V. If the switching speed of the gate driver is assumed to be between 1 and 5 nanoseconds (ns), then the amount of transient current that the gate driver must supply can be calculated using Equation 4.1 [10].

$$I = C \times \frac{dV}{dt} \tag{4.1}$$

Using this method, for some cases the gate driver must supply up to 7 A of current to the MOSFET gate(s) during switching, depending on the rise or fall time. Since the current may actually have a peak value larger than what was calculated, a gate driver that is capable of supplying well over 7 A of current is needed to obtain maximum switching speeds. The UCC37322 is capable of supplying 9 A of current according to industry standards, but is also capable of driving many applications that require 12 A [11]. The simulated currents waveforms can be seen in the Simulations section. The currents calculated for this range of parameters are given in Table 4.1.

Table 4.1: Calculated Transient Gate Currents

Output Device	Capacitance (pF)	ΔV (V)	Δt (ns)	Current (A)
NMOS	497	10	1	4.97
	497	10	2	2.49
	497	10	3	1.66
	497	10	4	1.24
	497	10	5	0.99
PMOS	717	10	1	7.17
	717	10	2	3.59
	717	10	3	2.39
	717	10	4	1.79
	717	10	5	1.43

The gate driver design utilizes a sophisticated output stage called "TrueDrive" and can be seen in Figure 4.2. In this design, BJT transistors are used to supply maximum gate drive current to the load during the Miller plateau region while the FETs make the gate driver's output have rail-to-rail swinging capability [12]. However, since the circuit must draw such large currents in nanoseconds of time, bypass capacitors are needed in order to help supply this current and maintain steady supply voltages. These capacitors also prevent any unwanted voltage spikes or droops from manifesting in the power network. They are sized to be at least ten times larger than the capacitive load that the UCC37322 is driving.

Every capacitor has a characteristic impedance curve over various frequencies. Capacitors generally perform well up to a certain self-resonant frequency determined by the capacitor's intrinsic characteristics such as its value, equivalent series resistance (ESR), and equivalent series inductance (ESL). When the capacitor is used at frequencies past its particular self-resonant frequency, it becomes more inductive than capacitive and no longer functions as an ideal capacitor [13]. To mitigate this effect, several capacitors with complementary impedance

curves are paralleled in order to provide sufficient bypassing over a large bandwidth. These capacitors were chosen to have the smallest possible ESR and ESL [10].

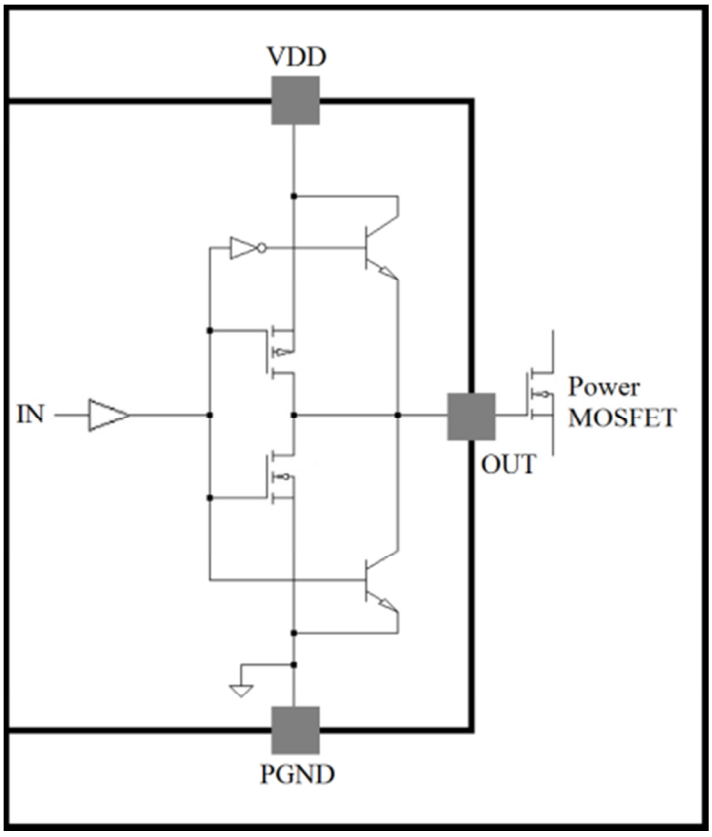

Figure 4.2: TrueDrive Output Stage [12]

Since there is a large amount of current flowing through the gate driver, the power dissipation also needs to be considered. This calculation can be helpful in determining whether the chosen device can withstand such conditions and aid in deciding if any heat considerations need to be made. The total power dissipated by the gate driver can be estimated by Equation 4.2. Since this equation is proportional to frequency of the gate driver output signal, the amount of power dissipation will vary as the operating frequency changes. The frequency range of the BNG driver is from 200 Hz (typical) to 10 kHz (maximum). Using Equation 4.2 [10] and the frequency range set by the design constraints, the minimum and maximum power dissipation is calculated for each gate driver. The parameters for this calculation can be found in Table 4.2, and the results are shown in Table 4.3. The maximum amount of power dissipated is less than 20 mW. Since the maximum allowed power for the package chosen is 650 mW, there are no power concerns or heating effects while supplying this amount of transient current to the power switches.

$$P_D = P_{D(ON)} + P_{D(OFF)}$$

$$P_D = \frac{R_{OH} \times V_{CC} \times Q_G \times f_{SW}}{R_{OL} + R_{Gext}} \tag{4.2}$$

Table 4.2: Gate Driver Parameters

	Name	Description	Value/Range	Units
NMOS	R_{OH}	Driver R_{OUT} at High Output	15 – 25	Ω
	V_{CC}	Gate Supply Voltage	10	V
	Q_G	MOSFET Gate Charge	9.2	nC
	f_{SW}	Switching Frequency	200 - 10000	Hz
	R_{OL}	Driver R_{OUT} at Low Output	1.1 - 2.5	Ω
	R_{Gext}	External Series Gate Resistance	1	Ω
PMOS	R_{OH}	Driver R_{OUT} at High Output	15 – 25	Ω
	V_{CC}	Gate Supply Voltage	10	V
	Q_G	MOSFET Gate Charge	16.5	nC
	f_{SW}	Switching Frequency	200 - 10000	Hz
	R_{OL}	Driver R_{OUT} at Low Output	1.1 - 2.5	Ω
	R_{Gext}	External Series Gate Resistance	1	Ω

Table 4.3: Gate Driver Power Calculations

Device	Frequency (Hz)	R_{OH} (Ω) (typ/max)	R_{OL} (Ω) (typ/max)	Power Dissipated (mW)
NMOS Gate Driver	200	1.1	15	0.131
		1.1	25	0.219
		2.5	15	0.079
		2.5	25	0.131
	10,000	1.1	15	6.571
		1.1	25	10.952
		2.5	15	3.943
		2.5	25	6.571
PMOS Gate Driver	200	1.1	15	0.236
		1.1	25	0.393
		2.5	15	0.141
		2.5	25	0.236
	10,000	1.1	15	11.786
		1.1	25	19.643
		2.5	15	7.071
		2.5	25	11.786

The UCC37322 also has separated input and output supply pins, another important feature for this application. A small amount of impedance, internal to the chip, exists between the input and output power supplies. This feature makes input decoupling of the power and ground connections possible [11]. The importance of this feature is described in the next section.

4.1.3 Common-mode Choke – TDK Corporation ACM2520-801-3P

With such high current transients, common-mode signals can sometimes be transferred back to the input of the gate driver, resulting in a false trigger. One common technique to prevent this from happening is to utilize a common-mode choke (CMC). Since the gate driver's input and output supply pins are separated internally, the CMC can be placed between these pins as well as between the input isolator output signal and the gate driver input signal to implement this technique. The purpose of a CMC is to reject unwanted common-mode transients, while allowing desired differential-mode drive signals to be transmitted virtually undisturbed. One such signal from the input isolator is present in the circuit as current in more than one of the CMC windings flowing in opposite directions. Since these currents form a loop, they should produce opposite polarity magnetic fields with the same magnitude, which cancel with one another. As a result, the CMC provides low impedance paths for both signals to travel virtually unaffected. However, if common-mode transient signals try to enter the CMC, the magnetic fields created by the in-phase currents sum together. When this occurs, the CMC appears as a high impedance path rejecting the unwanted signals [14]. High current transitions can cause transient signals to travel through the ground and power planes. Since these signals would enter the CMC as common-mode signals, they are eliminated and cannot cause false triggering in the gate driver.

Similar to the bypass capacitors, CMCs have a self-resonant frequency. A choke with a high enough self-resonant frequency was selected to ensure proper performance. The highest frequency contained in an input signal to the gate driver is directly proportional to the rise or fall time of the signal. For this design, the fastest rise or fall time of this signal is around five nanoseconds. The self-resonant frequency of the CMC is approximated by Equation 4.3 [15], resulting in a required bandwidth of at least 70 MHz.

$$BW \cong \frac{0.35}{\tau_r} \tag{4.3}$$

The ACM2520-801-3P is ideal for this application since it utilizes a three-channel choking design and has an inherent self-resonant frequency well above the required bandwidth of this application. As can be seen from Figure 4.3, this CMC has a self-resonant frequency around 600 MHz. At the driving signal's typical switching speed, the CMC should only add an additional 10 Ω of series impedance into the signal path [16].

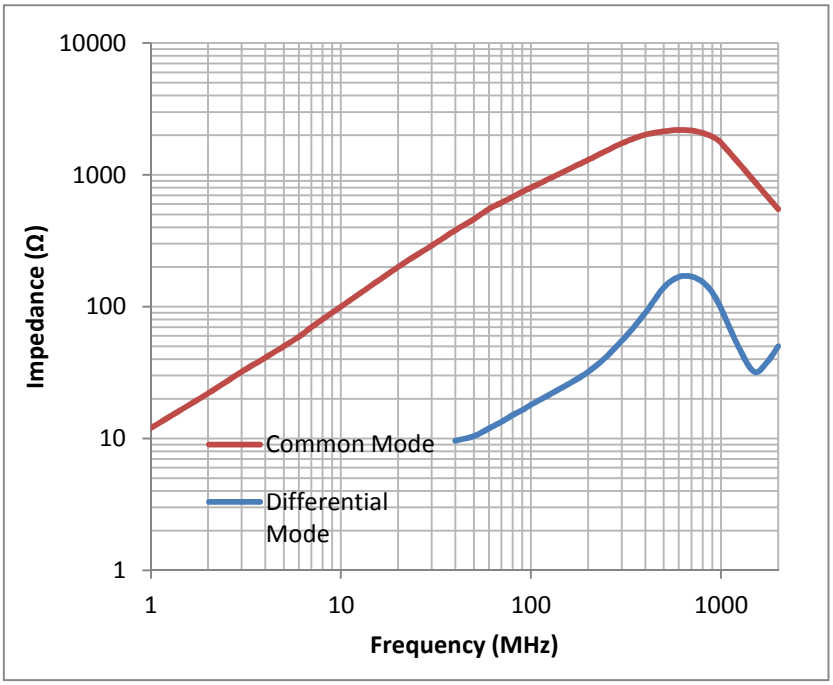

Figure 4.3: Common-Mode Choke Impedance vs. Frequency Characteristics [16]

4.1.4 Output Transistors – Zetex ZXMC10A816N8

The output transistors are a crucial element in the design and performance of the BNG driver electronics. There are many aspects of the design and selection to be considered for the power transistors. The first parameter to consider is the power limitations of each device. Since the output signals desired have a magnitude of 50 V, each transistor must be able to support at least this amount of drain-to-source voltage magnitude. For a more robust design, a maximum voltage rating of 100 V was selected to give the design a safety margin for overshoot and voltage spikes.

The other key component of an output device's power limitations is its current capabilities. Two main types of current limits must be considered, the continuous and pulsed current present from the drain to source. Since these devices are being implemented as switches, ideal switch performance is desired. An ideal switch should have infinite impedance when open and zero impedance when closed. It should also be able to transition instantly. A MOSFET is not ideal by any means. However, for optimum performance within a circuit, transistors should have characteristics that reproduce the ideal behavior of an ideal switch as closely as possible. For this reason, the *on* resistance of a power transistor is usually very low. In this type of amplifier output stage, only one output transistor should be turned on at a time. As a result, the continuous drain-to-source current in each of the transistors should be extremely low. However, if both devices are turned on at the same instant, according to Ohm's Law, the shoot through current flowing through each device can be extremely high for a short amount of time due to the devices' low *on* resistances and high drain-to-source voltages. The amount of current generated through this phenomenon would greatly exceed the constant and pulsed current ratings of these devices resulting in a catastrophic failure of the device. Special attention is given to the timing of the

input signals such that this shoot through current does not occur. By implementing a certain amount of time in the control signals in which both devices are turned off, shoot through current is avoided. For the positive side of the driver circuitry, the PMOS remains on most of the time pulling the output up to 50 V. When the output signal needs to switch, the input signal driving the PMOS must turn off before the NMOS is turned on, and the input is pulled down to 0 V. The time in which the PMOS and NMOS are both off is referred to as the input signal dead-time. Just as with the 50-V to 0-V transition, the NMOS must be completely off before the PMOS turns back on. The input signal dead-time must be implemented on this 0-V to 50-V transition as well. Just as with the positive side, all negative side transitions must be offset with a small amount of dead-time as well. For the negative side, the NMOS is pulling the output down to −50 V. For this reason, the NMOS must be off before the PMOS turns on pulling the output up to 0 V. The signal setup continues for the other negative side transition. An example of the input signal timing can be seen in Figure 4.4. The value of Δt is determined by inherent propagation delays within the circuit. This value can vary due to component variations, trace lengths and widths, and other delay inducing components within the design. The value for this will be discussed later. Pulse width 1 and pulse width 2 are adjustable and directly determine the pulse width of the differential output signal. The “high” voltage level of each input signal can range between 3.3 and 5 V. In the figure below, 4 V was chosen because the signal generator used in the test setup provides 4-V TTL control signals.

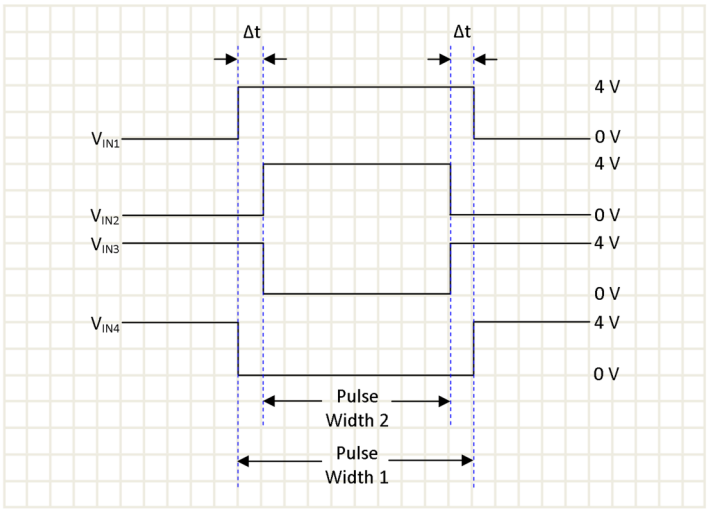

Figure 4.4: Input Signal Timing

To obtain symmetrical output signals, other parameters of the MOSFETs must be considered. Since this design utilizes complementary *n*-channel and *p*-channel MOSFETs, matched devices and symmetrical output signals can be very difficult to obtain. A PMOS transistor is inherently slower than an equally sized NMOS equivalent. This is mainly due to the carrier mobility inherent in each device. In order to get more closely matched complementary transistors, the device parameters of the PMOS must be adjusted in order to obtain the same performance as the NMOS. As a result, other parameters of the device change and cause mismatch in the two devices. Since the speed and drive strength of the PMOS is enhanced to match the electrical performance of the NMOS, the amount of input capacitance, and therefore gate charge required to turn the device *on* and *off*, also increases. While it is impossible to have completely matched *n* and *p*-channel devices, fabricating both devices on the same substrate can help eliminate some matching discrepancies. This also ensures closer matching over process variations from chip to chip. The parameters of the ZXMC10A816N8 match very closely and are ideal for obtaining the most symmetric signal attainable. By looking at their datasheet, these transistors seem to be the same transistor with slightly different input capacitances. Any

asymmetry caused by this difference will hopefully be mitigated by the PMOS gate drivers. Since these gate drivers typically drive much larger capacitive loads, a difference of approximately 200 pF in the input capacitances should not greatly affect the symmetry of the signals [17].

4.2 Power Network Design

In order for this system to work properly, a robust supply of power must be available for each of the components to use when needed. Table 4.4 in the next section shows each of the voltage levels needed and which device utilizes them. These voltage levels are also labeled in Figure 4.5. The input voltage to the system sets the voltage level for the output signals. For normal operation and testing, these voltages are +50 V, ground, and −50 V. The power network circuit utilizes theses supplies and creates all other necessary voltage levels. The output side of each input isolator is powered by a 5 V potential that is level shifted with reference to the common voltage of the output side. All gate drivers are powered by a level shifted 10 V supply. The level to which each of these is shifted depends on which transistor channel is being driven. When used in the ORISS application, the common potential is approximately 600 V and all voltages are referenced to this voltage instead of ground in the output section.

4.2.1 Power Considerations, Required Voltages, and Selection Process

The power network is created using the 50-V difference between the positive supply rail and the common potential. This circuit is then replicated and utilized for the negative voltage supplied as well. The overall power system circuit can be seen in Figure 4.5.

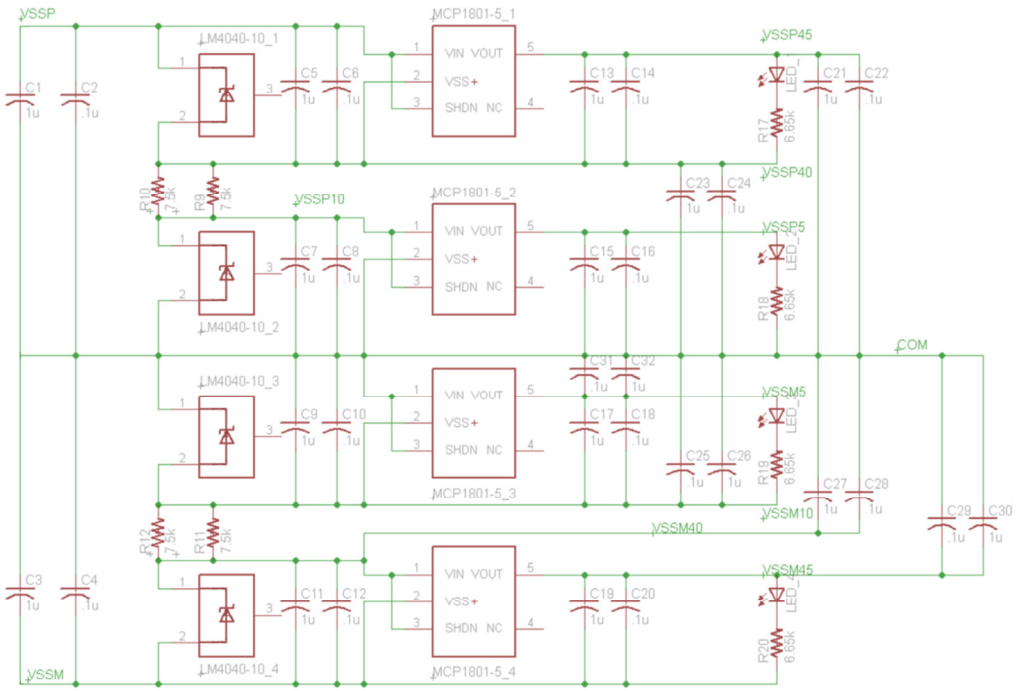

Figure 4.5: Power Network Circuit

The power supplied to each of the gate drivers is created using four voltage references and four resistors. Each gate driver uses its supplied input signal to produce an output signal that swings between each of its supply rails. For the PMOS drivers, each VDD supply voltage of the driver is connected to the source of the output transistor it is driving. This will be positive 50 V for the PMOS on the positive voltage side of the electronics and the common potential (ground or 600 V) for the PMOS on the negative voltage side. The ground pin of each NMOS driver is connected to its respective NMOS source terminal. This is the common potential (ground or 600 V) for the positive voltage side and −50 V for the negative voltage side. To obtain a 10 V gate-to-source driving signal for these devices, the voltage is created with respect to the output transistor's source voltage. The polarity of the 10-V supply is positive for each NMOS and negative for each PMOS. The National Semiconductor LM4040 is used here to implement this voltage level scheme. By using these 10 V voltage references with biasing resistors between

each, all necessary voltages are created. Two 7.5 kΩ resistors are paralleled and placed between the two voltage references for each side. This was done to establish the appropriate quiescent current for all devices in the system and allow the resistors to share this current flow. For a system with 50-V power supplies, this current is calculated using Equation 4.4. In this configuration, there is around 8 mA of bias current. Since the two resistors are sharing the standing current, their power ratings do not need to be as high as would be necessary if all current was flowing through a single passive device. All gate driver voltages created can be seen in Table 4.4.

$$I_{bias} = \frac{(V_{SSP/M} - 20)}{7.5k\Omega \,||\, 7.5k\Omega} \tag{4.4}$$

Table 4.4: Required Voltages

Voltage Name	Device Pin Supplying	Voltage (V)
VSSP	ZXMC10A816N8_1 PMOS Source	50
VSSP	UCC37322_1 VDD	50
VSSP45	ADuM4400_1 VDD	45
VSSP40	UCC37322_1 GND	40
VSSP40	ADuM4400_1 GND	40
VSSP10	UCC37322_2 VDD	10
VSSP5	ADuM4400_2 VDD	5
COM	UCC37322_2 GND	0
COM	ADuM4400_2 GND	0
COM	ZXMC10A816N8_1 NMOS Source	0
COM	ZXMC10A816N8_2 PMOS Source	0
COM	UCC37322_3 VDD	0
VSSM5	ADuM4400_3 VDD	−5
VSSM10	UCC37322_3 GND	−10
VSSM10	ADuM4400_3 GND	−10
VSSM40	UCC37322_4 VDD	−40
VSSM45	ADuM4400_4 VDD	−45
VSSM50	UCC37322_4 GND	−50
VSSM50	ADuM4400_4 GND	−50
VSSM50	ZXMC10A816N8_2 NMOS Source	−50

The voltage that is needed to supply the output side of the input isolators must also be referenced to the gate driver supply voltages. The gate driver's low-level logic input voltage is typically 1.6 V above its ground voltage, while the high-level logic input voltage required to operate the gate driver is typically 2.2 V. To account for this, each of the isolator's ground pin is connected to each of the corresponding gate driver's ground pin [11]. The isolator's outputs are then powered by a 5 V supply in order to get a gate driver input signal 0 to 5 V. To set these voltages, a fixed 5 V low-dropout (LDO) linear regulator is used. The device used to set these voltage levels is the MCP1801which is made by Microchip. These devices use the 10 V input created by the voltage references and output a 5 V voltage reference. Capacitors are added between the input and output pins of the regulator for stability. The manufacturer recommends that at least 1 μF of capacitance is added between the output and ground pins for voltage stability of the device. A capacitance between the input and ground pins equivalent or greater than the output capacitor is required for optimum performance of the device [18]. Additional capacitors are added to the power supply circuit for bypassing and to eliminate voltage fluctuations.

Light-emitting diodes (LED) are used at each 5 V output to be an indication of whether the circuit is biased correctly. Since there is very little bias current in this circuit, the amount of current drawn by the LEDs is restricted to a very small amount. Research shows that LEDs are typically biased with 20 mA of current. For this application, 0.5 mA of current is supplied to each LED. A 650 nanometer (nm) red LED made with aluminum gallium indium phosphide (AlGaInP) on a Gallium Arsenide (GaAs) substrate was selected. The semiconductor physics of such materials produce an LED that requires low power and still emits a large amount of light, even at low forward currents. Once this part was tested for light intensity in the lab, it was integrated into the design for power indication. The LED circuit used can be seen in Figure 4.6.

The resistor in the circuit was sized based on the desired forward current and the intrinsic forward voltage drop across the LED. As previously stated, the desired forward current is 0.5 mA due to the limited quiescent current in the circuit. The forward voltage characteristic curve from the datasheet (Figure 4.7) indicates that a forward voltage around 1.7 V will be inherent in the LED at the desired operating current. Using Ohm's Law ($V = IR$), a resistance value of 6.65 kΩ was selected.

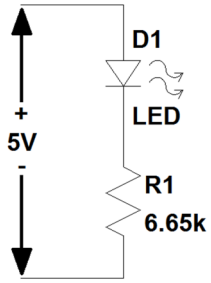

Figure 4.6: LED Circuit Schematic

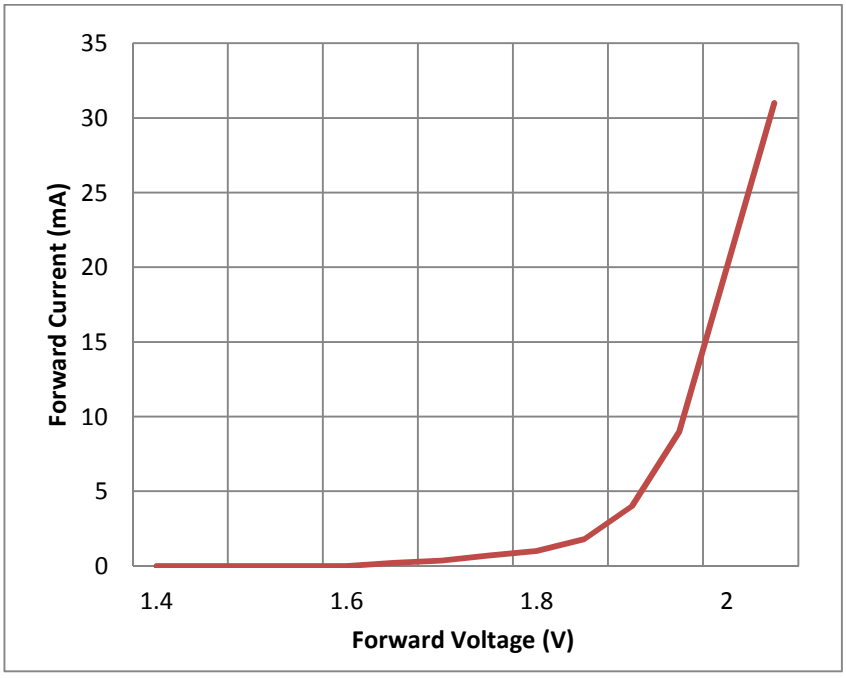

Figure 4.7: Forward Voltage vs. Current Characteristic Curve [19]

4.3 Load Modeling

By using a network analyzer, the impedance of the BNG was found to be almost purely capacitive. The differential capacitance between the two signals can be modeled as a load of approximately 60 picofarads (pF) at 10 kHz. At 10 MHz, the differential capacitance was measured to be about 85 pF. A difference of this magnitude will mostly impact the design by how much termination resistance is used at the output to match each cable. This will be discussed in more depth in Chapter 5. Since the switching speeds of the output signals are very fast, these cables act as transmission lines and contribute to the load of the electronics. At both frequencies, six inches of Teflon coated wire contributed approximately 15 pF between each signal path and ground. The signal was originally sent to the BNG over six inches of wire, from which the impedance measurement originated. For the updated design, the cables are each 18 inches long. From this, the parameters for the transmission line model of the load can be determined.

The measured capacitance contributed by the wire is approximately 15 pF for every six inches. For the modeling done for design simulation purposes, the cable was assumed to be lossless and have a characteristic impedance of 50 Ω per cable. The assumption that the transmission line is lossless means that the series resistance and parallel admittance are both zero. This assumption also yields the simplified equation used for calculating the distributed elements [20]. This equation is given in Equation 4.5. For the modeled load that is used, it is assumed that 18 inches of cable will be used. The value for the per unit capacitance was measured to be

$$C' = 15\,\frac{pF}{0.5\,ft} = 30\,\frac{pF}{ft} \times \frac{1\,ft}{12\,in} = 2.5\,\frac{pF}{in} = 0.098\,\frac{pF}{mm}.$$

Using the assumption that the characteristic impedance is 50 Ω and Equation 4.5 [20], the per unit inductance is determined.

$$Z_0 = \sqrt{\frac{L'}{C'}} \tag{4.5}$$

$$50 = \sqrt{\frac{L'}{2.5\frac{pF}{in}}}\,(\Omega)$$

$$L' = 2500 \times 2.5x10^{-12}\frac{H}{in} = 6.25\frac{nH}{in} = 0.25\ \frac{nH}{mm}$$

For simulations, the load cabling is 18 inches long (approximately 457.2 mm). The distributed load for this model uses 10 segments to model a transmission line. Therefore, each segment contributes to 1.8 inches of the cable. This means that each segment will have an inductance of $= L' \times l$, where *l* is the length of each segment.

So,

$$L = 6.25\frac{nH}{in} \times 1.8\ in = 11.25\ nH$$

for each segment. For the capacitance per segment, the capacitance per inch and the size of each segment (in inches) have been calculated, so

$$C = C' \times l = 2.5\frac{pF}{in} \times 1.8\ in = 4.5\ pF.$$

This capacitance value is between each line and ground. Since the output signals are fully differential, each capacitive element can be lumped together by the series combination of each distributed capacitance.

$$C_1 + C_2 = \frac{C_1 \times C_2}{C_1 + C_2} = 2.25\ pF$$

The values calculated above can be seen below (Figure 4.8) in the distributed element transmission line model that was used in simulations. Along with the transmission line model, the worst case capacitive load, which was measured to be 85 pF at 10 MHz, is also included in the figure. Output termination resistors can also be seen here. These will be discussed in later sections.

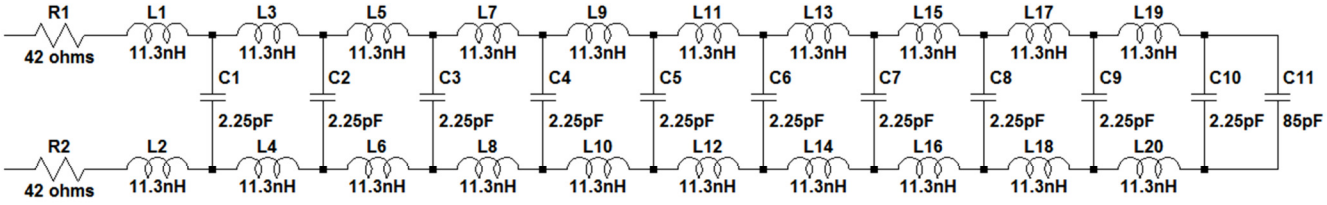

Figure 4.8: Distributed Element Transmission Line Load Model

4.4 Simulation Results

LTSPICE, PSPICE, and HSPICE were initially used to simulate various aspects of this design. However, the most valuable results obtained were done using LTSPICE. Regardless of the simulator used, access to some device models was limited. Since the optocoupler series is relatively new, no SPICE models were found for use in simulations. It may have been possible to create a usable model from the specifications given on the datasheet. However, since the isolation breakdown and high-voltage operation would be difficult to determine in a simulator environment, this portion of the design was left for testing in the lab. SPICE models for the gate

driver could not be found either. However, a model for an output signal of a gate driver with similar specifications as the one used in this design was found. By using this gate driver output signal, the remainder of the circuit can be simulated. The circuit used to replicate this gate drive signal is shown in Figure 4.9. An example of the signal produced by this topology can be seen in Figure 4.10.

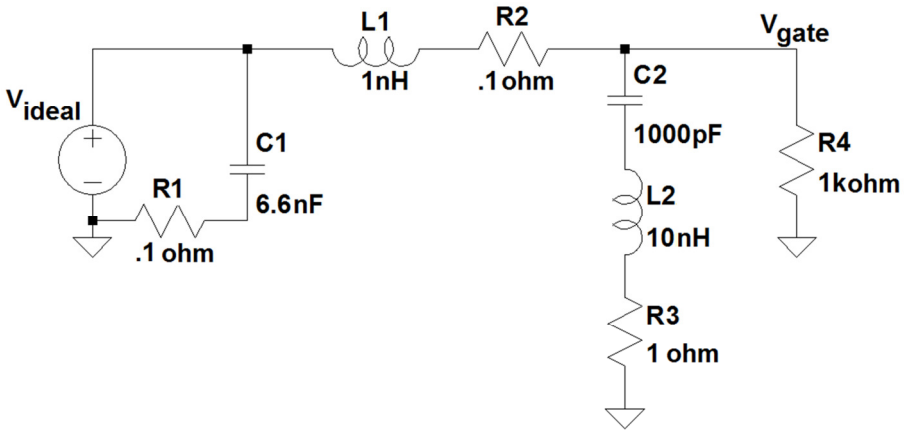

Figure 4.9: Simulated Gate Driver Output Signal Circuit

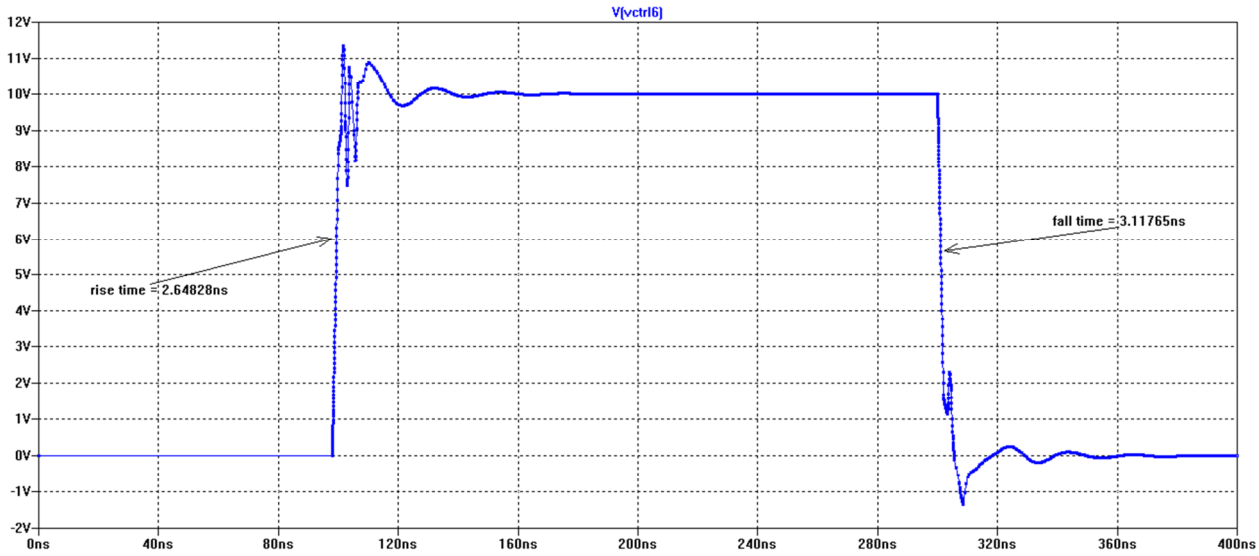

Figure 4.10: Simulated Gate Driver Output Signal

Signals similar to the one seen above are used to drive the gates of each power MOSFET. The output stage is modeled as accurately as possible in the simulations as shown by the circuit in Figure 4.11. Models for the exact power transistors used were not found. However, transistor models with very similar parameters and made by the same manufacturer were found and used. The model for the ZXMP10A17E6 was used for the PMOS, and the model for the ZXMN10B08E6 was used to simulate the NMOS. The capacitive bypass networks were also added to the output stage along with parasitic series inductance of 5 nH on each of the MOSFET sources. 1 Ω of series gate resistance was added to each gate and the distributed transmission line load model was also utilized in simulations. The signals obtained through these simulations can be seen in Figure 4.12 through Figure 4.17. Although both the single-ended and differential results are given, the Bradbury-Nielsen gate will only be subject to the differential signal since both output signals will always be driving the BNG simultaneously in a differential configuration.

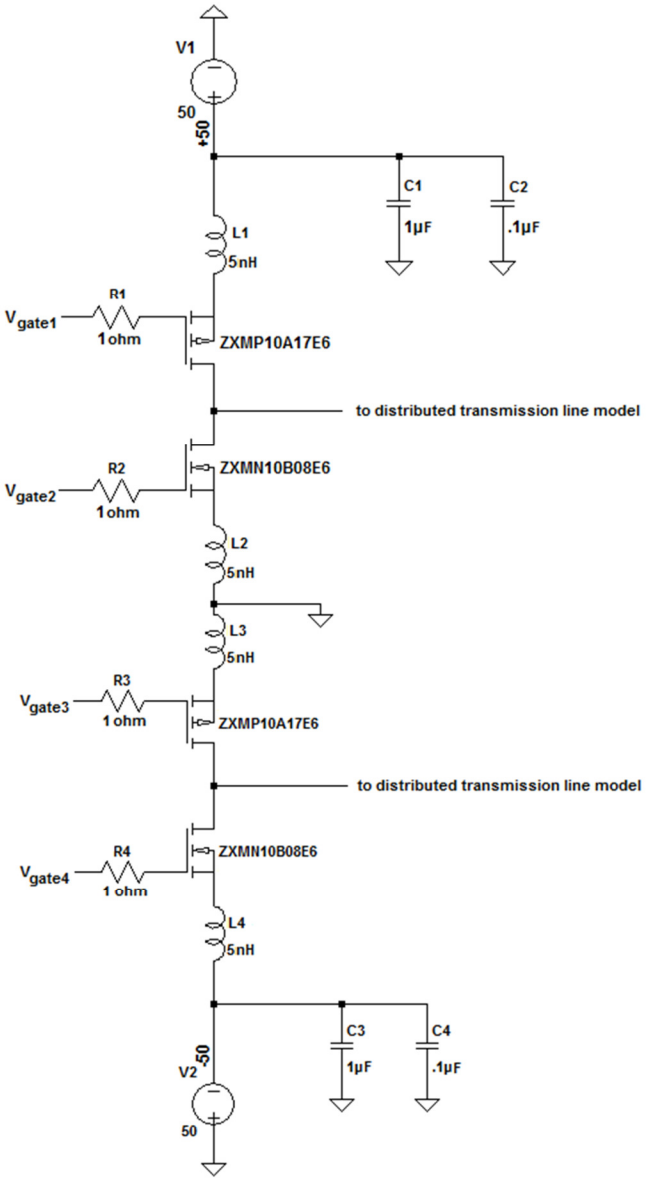

Figure 4.11: Simulated Output Stage Circuit

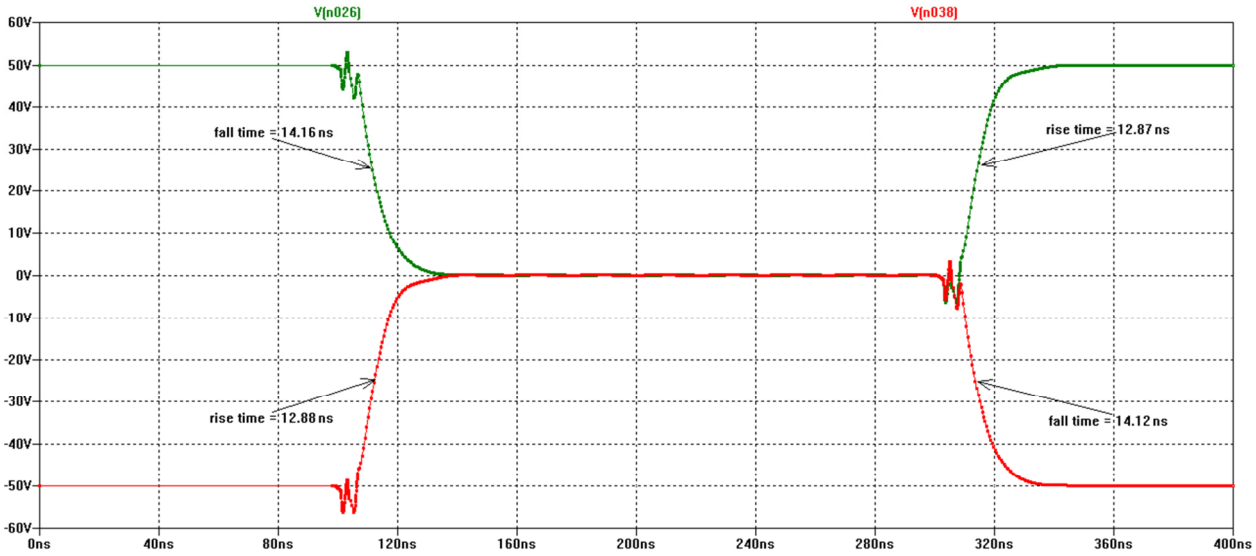

Figure 4.12: Simulated Single-Ended Output Signals – Normal Operation

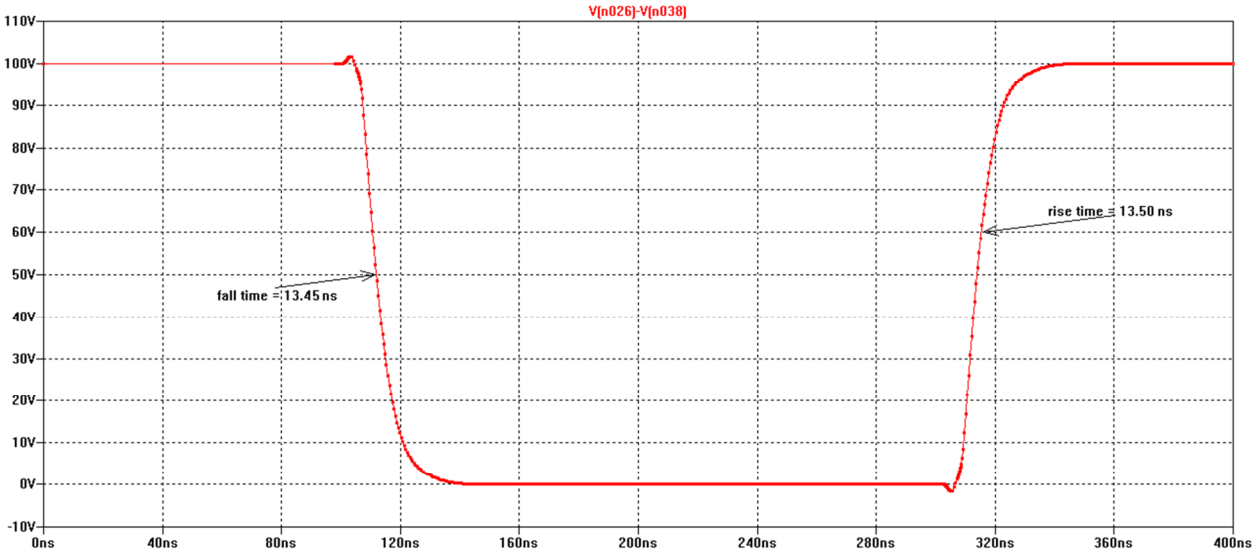

Figure 4.13: Simulated Differential Output Signal – Normal Operation

By observing the switching times of the gate driver signals, the rise and fall times of these signals are around 2 to 3 ns. From earlier calculations, the maximum transient gate currents at these transition speeds can be estimated to be around 3 A. This is confirmed in the simulated transient current seen in Figure 4.14 below.

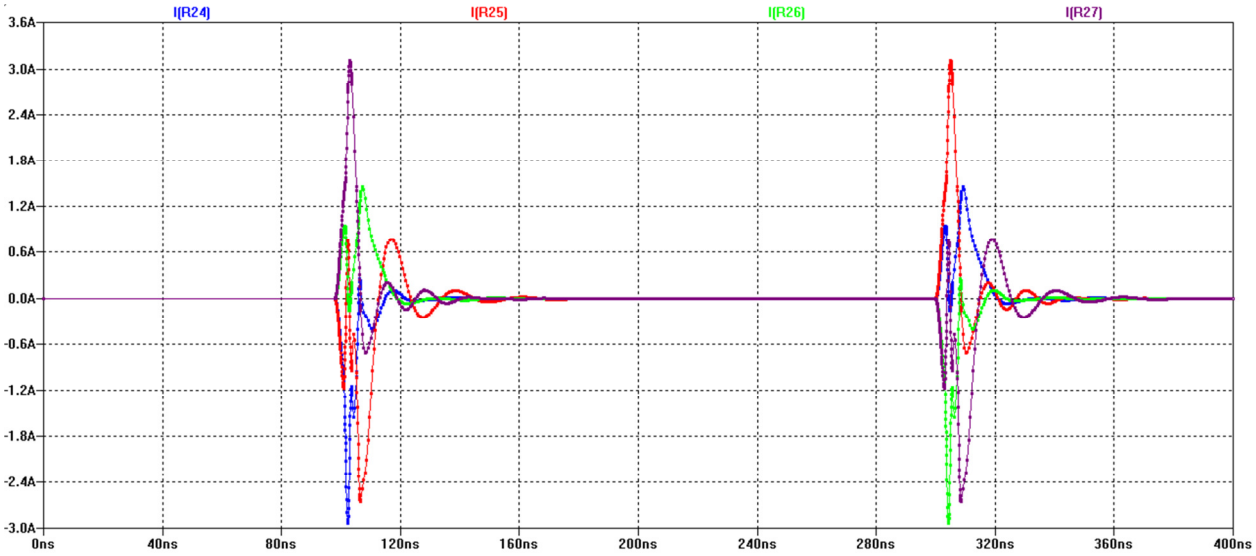

Figure 4.14: Simulated Transient Currents – Normal Operation

Simulations are also done to determine the minimum pulse width that can be obtained while maintaining sufficient signal integrity. Lower pulse widths are achievable; however, around 40 ns was the minimum value at which the signal remained adequate. These signals are shown in Figure 4.15 and Figure 4.16. The transient currents for these signals are also shown below in Figure 4.17. All rise and fall time results are outlined in Table 4.5.

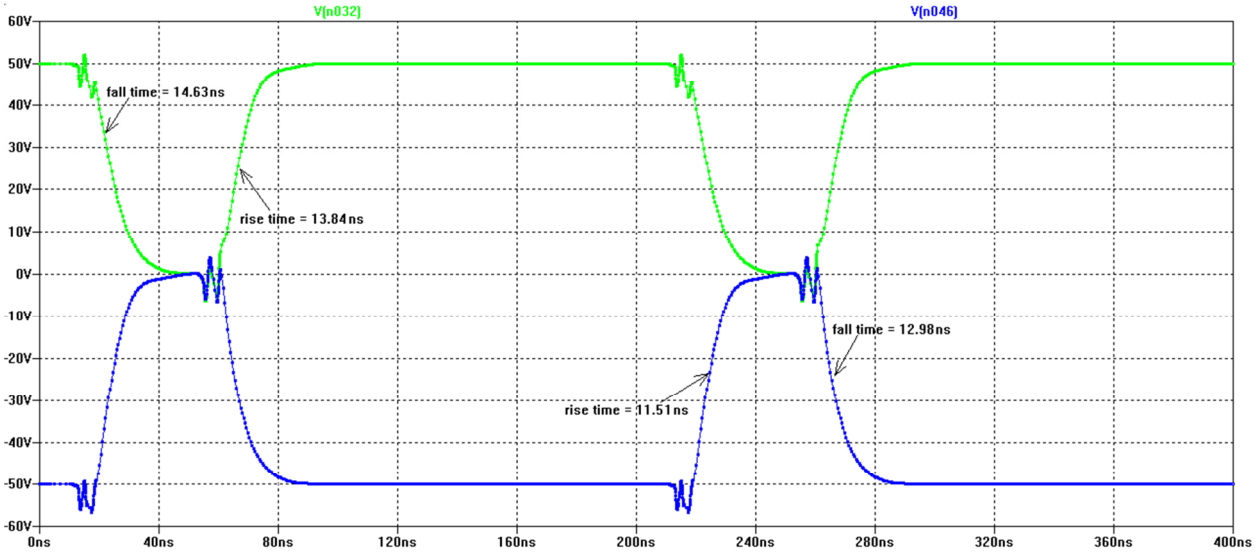

Figure 4.15: Simulated Single-Ended Output Signals – Minimum Pulse Width

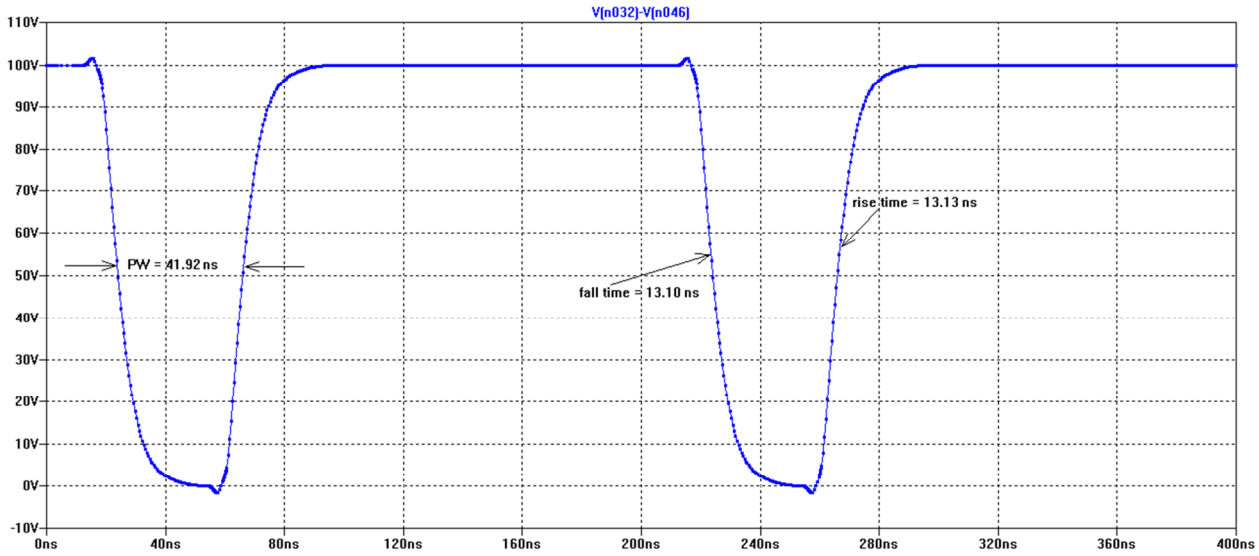

Figure 4.16: Simulated Differential Output – Minimum Pulse Width

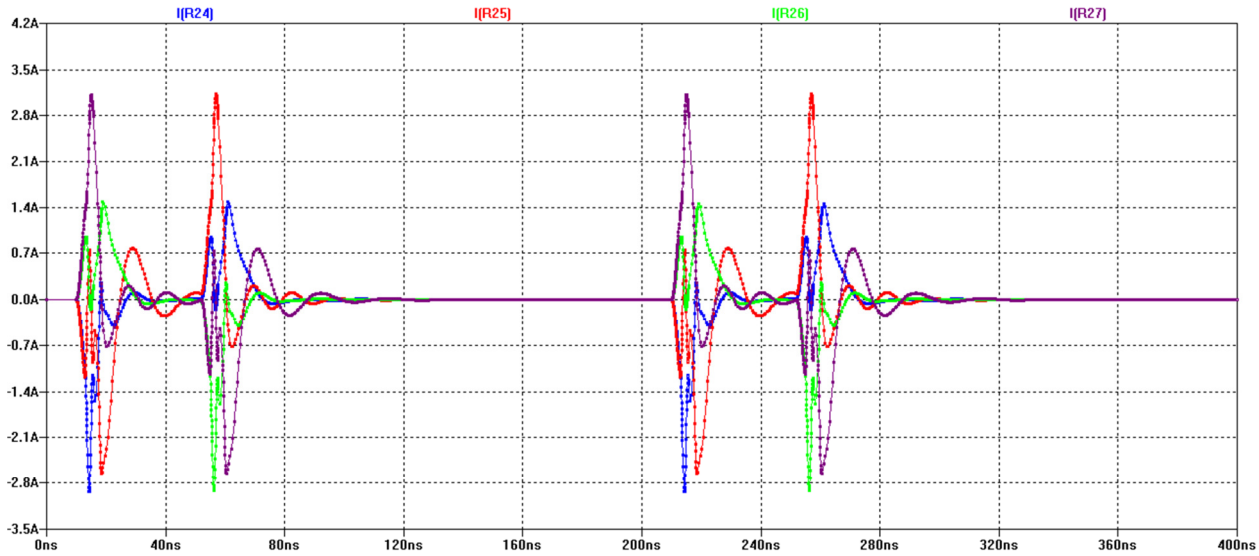

Figure 4.17: Simulated Transient Currents – Minimum Pulse Width

Table 4.5: Simulated Rise and Fall Times

Signal	Rise Time (ns)	Fall Time (ns)
+50 - Normal	12.87	14.16
−50 - Normal	12.88	14.12
Differential - Normal	13.50	13.48
+50 - Minimum PW	13.84	14.63
−50 - Minimum PW	11.51	12.98
Differential - Minimum PW	13.13	13.10

The simulation results show that this design can provide the needed voltage levels while maintaining the desired switching speeds. By observing the rise and fall times obtained, it can be concluded that this design should provide sufficient overall performance once implemented.

4.5 Board Design and Layout

Although the main design process has already been reviewed, additional design considerations are made for the physical layout of the BNG driver printed circuit board (PCB). A detailed system-level diagram is shown in Figure 4.18. Easily Applicable Graphical Layout Editor (EAGLE) is the computer-aided design (CAD) tool that was used to create the schematic and layout of the PCB. A 4-layer board is utilized for the implementation of this design. The top and bottom layers are for routing while the two inner metal layers establish the power planes. The 4-layer board stackup can be seen in Figure 4.19. The overall system board schematic and layout are shown in Figure 4.20 and Figure 4.21.

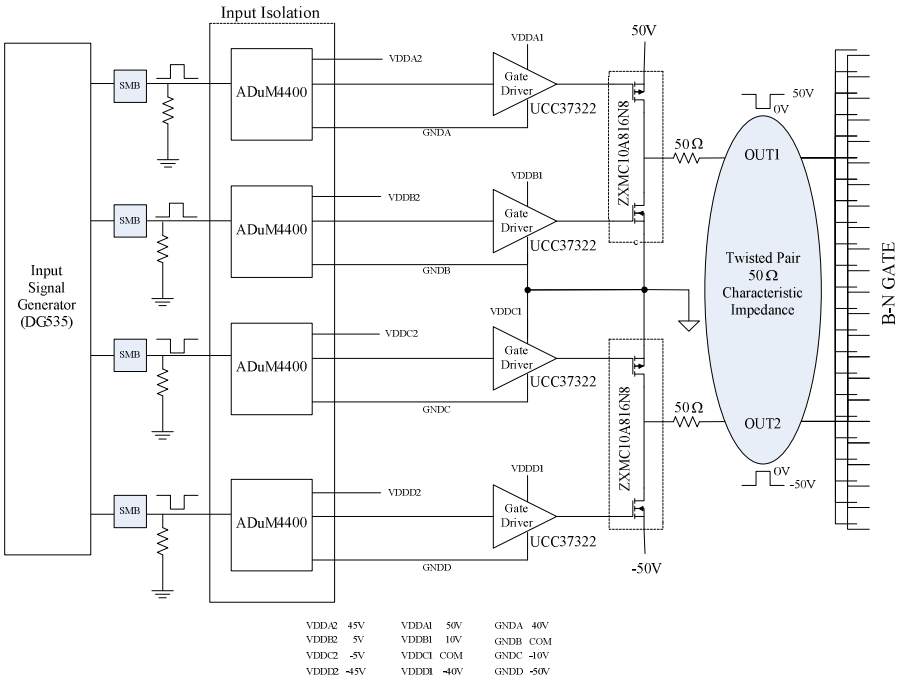

Figure 4.18: Detailed System-Level Diagram

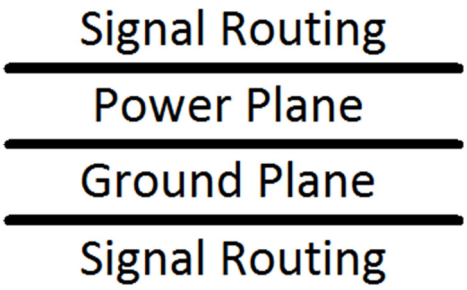

Figure 4.19: 4-Layer Stackup

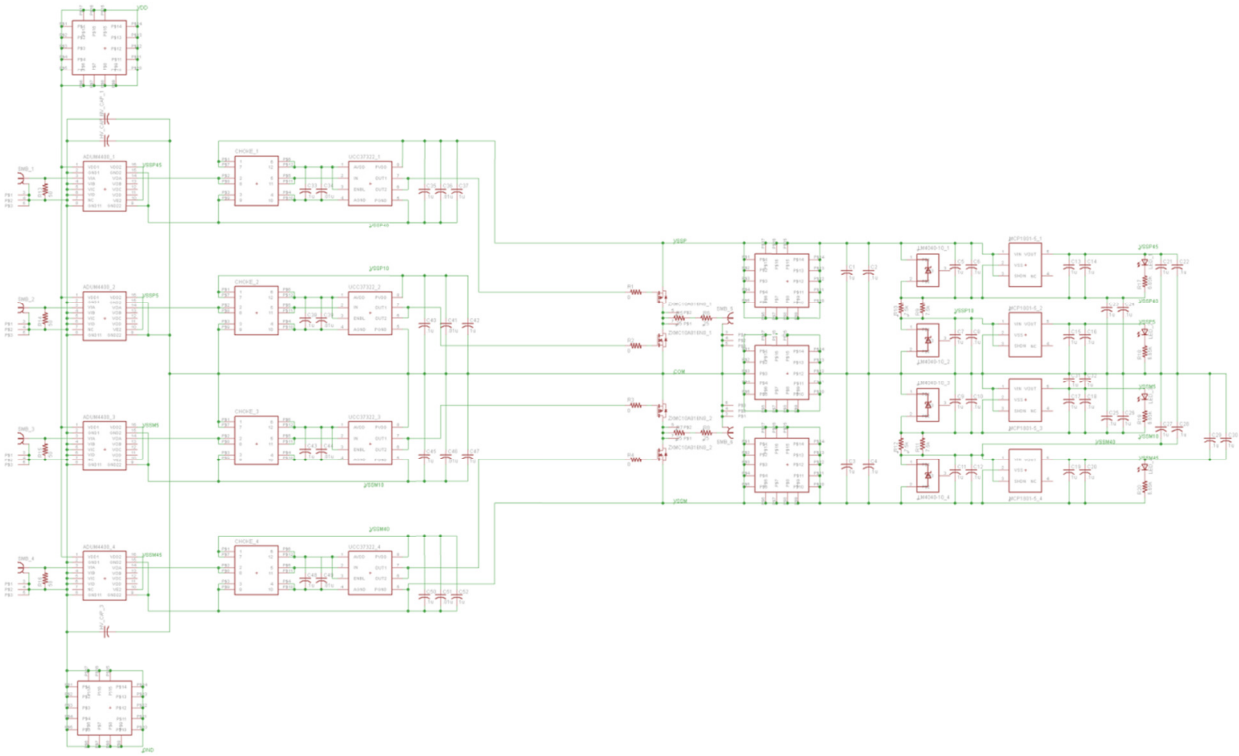

Figure 4.20: System Schematic

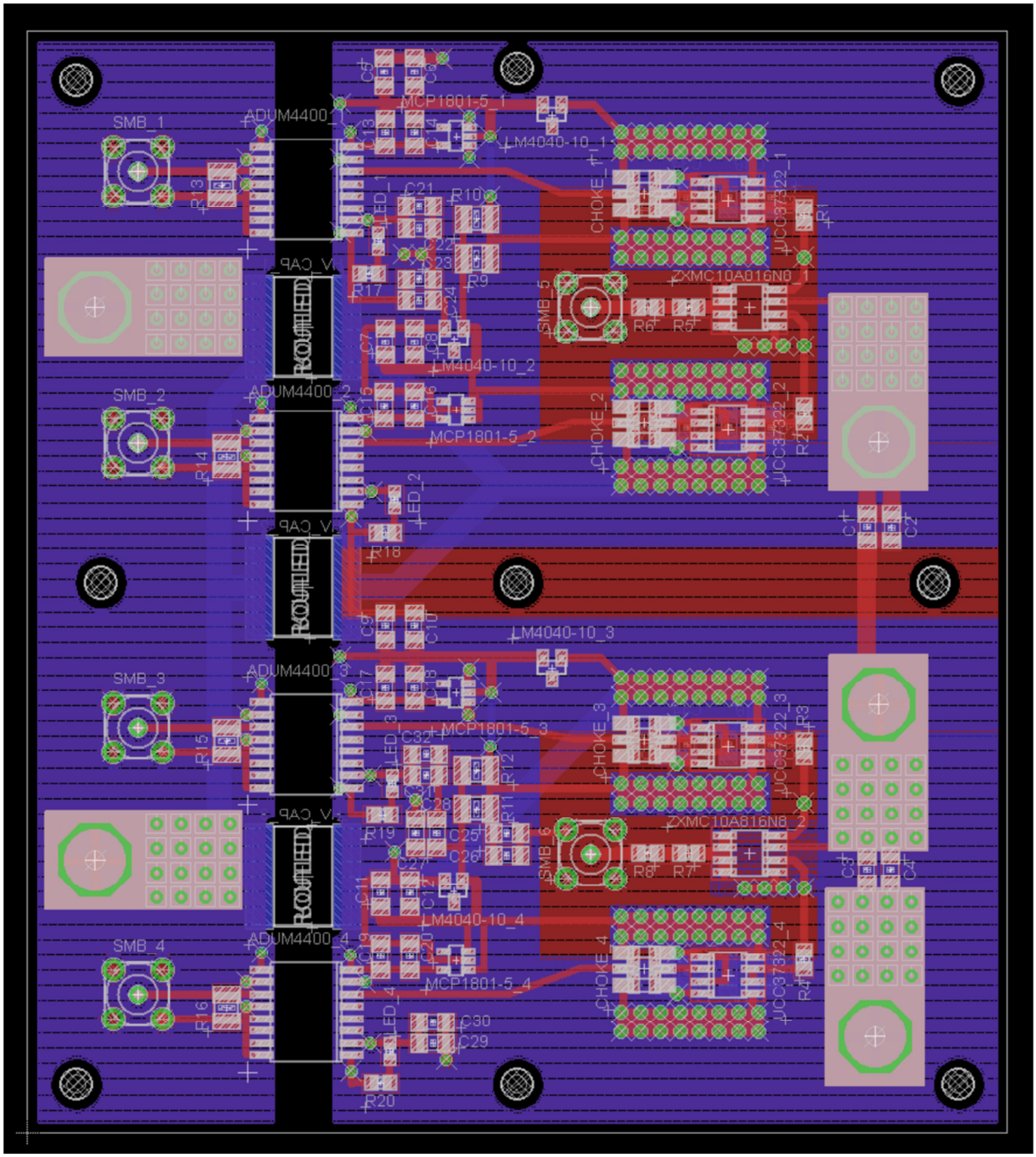

Figure 4.21: Board Layout

4.5.1 Power Plane Configuration

To provide proper input isolation for the design, the board is electrically and physically segmented into input and output sections. The input and output sides are separated by 250 mils to provide sufficient electrical isolation from the high voltage that is present. Three high-voltage (2 kV) X7R capacitors are used to bypass the output common potential plane to the input ground plane. The value of each high-voltage capacitor used is 0.1 μF.

For the power layer of the board, the input and output power planes are separated by the same 250 mils as the ground layer. There are also separate power planes on the output side for the output supply voltages. For the general case, this will be +50 V and −50 V. To provide as little coupling and interference as possible, these two planes also have a relatively large separation between them. These planes are separated by 300 mils. A large segment in the middle of each of the two output power supply planes is cut out. This is to allow for much smaller power planes in the inner layer of the board to provide the other necessary voltages created by the power network circuit. This was done to reduce the ESR and ESL of the voltages that are supplied to the components. The abundant use of parallel vias along with large power supply planes attempt to reduce the ESR and ESL in the circuit as much as possible for optimum performance. Since each via used contributes ESR and ESL, paralleling vias greatly reduce these parasitics. The layout of the ground and power planes can be seen in Figure 4.22 and Figure 4.23, respectively.

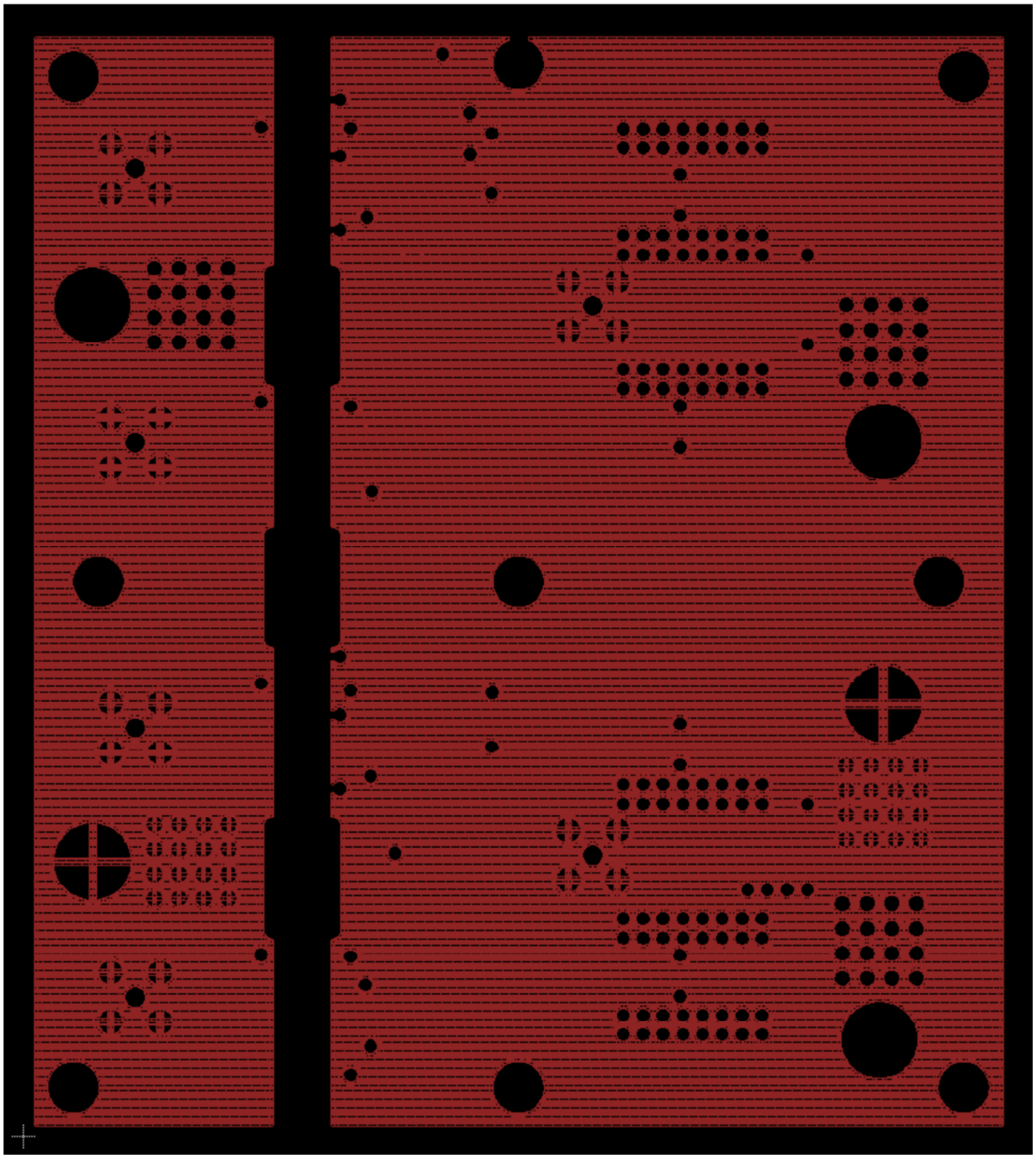

Figure 4.22: Ground plane

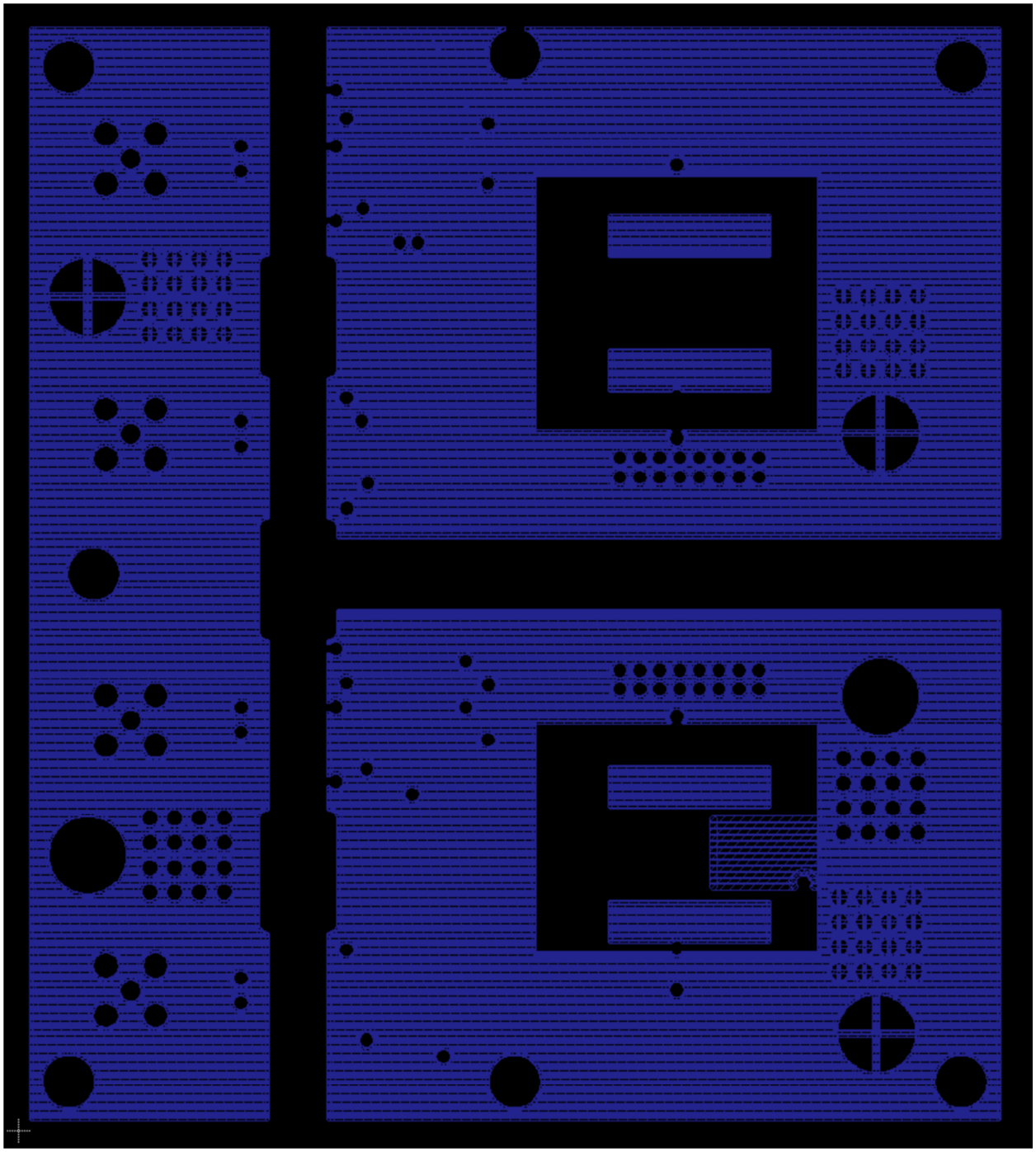

Figure 4.23: Power Plane

4.5.2 Bypassing Capacitors

As previously discussed with the gate driver design, most of the transient current supplied during switching was supplied by parallel capacitors with complementary impedance curves. Since the gate drive circuit is the most critical part of the signal path for current supply, three different capacitors were used. X7R capacitors with values of 1 µF, 0.1 µF, and 0.01 µF are used for bypassing, transient current supply, and minimizing noise. These capacitors are placed as close to the gate driver supply pins as possible to help reduce the ESR and ESL. For this same reason, the smaller valued capacitors are also placed closer to the pins than the larger components. A combination of all three capacitor values is used for the output power supply of the gate driver. The input power supplied to the gate driver utilizes a 0.1 µF and a 0.01 µF capacitor in parallel for bypassing. This capacitor network is placed as close as possible to the gate driver power pins. This technique was also used with the output transistors, output side of the input isolators, voltage references, and the linear regulators. Since bypassing and current requirements are not as stringent at these supplies, a combination of 1 µF and 0.1 µF capacitors were used. The capacitive network configuration used for each gate driver is shown in Figure 4.24.

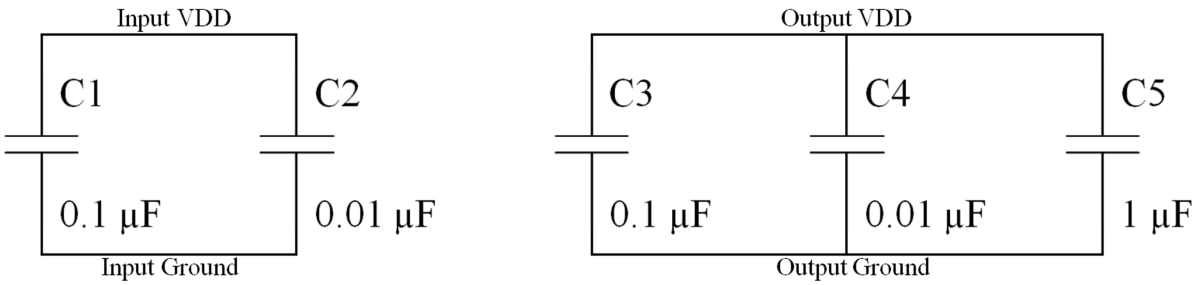

Figure 4.24: Gate Driver Bypass Network

4.5.3 Layout Placement and Routing

Another important consideration for the board design is trace length in the signal path and ground return loops. Every PCB trace has some ESR and ESL associated with it. By minimizing routing lengths in the signal path and maximizing cross-sectional area of traces, series parasitics can be greatly reduced. This is important because current takes the path of least resistance at low frequencies. However, at high frequencies, current will flow through the path of least impedance [13]. For this reason, parasitic capacitances are very important to consider as well. The use of supply planes and large area traces can produce relatively large parasitic capacitances between the two. For this reason, most of the critical signal paths do not have power planes under them. For those that do, the cross-sectional area of the crossing traces is kept to a minimum.

The length of the ground return loop in this design is also critical. The length of the loop, among other variables, is directly proportional to the amount of ESR and ESL that will be present in the loop. Larger amounts of ESR and ESL translate into noise and voltage variations. By minimizing the loop lengths, the performance of the circuit will more closely align with its ideal operation. Since large transient currents are present, the location of these loops is also important. Large current transients can induce voltage differences and noise in critical signal paths of the design. To avoid this, the ground return loops are placed on the board layout in locations in which they are as isolated from important circuit signals as much as possible.

Symmetry in the layout of the PCB can also prove to be critical in high-speed designs. For high-speed signals, board traces are effectively transmission lines. If trace lengths are symmetrical, critical signals should propagate throughout the circuit simultaneously. For this design, symmetry is important so that the timing of the input signals can be anticipated correctly. If asymmetry in the layout is causing propagation delay skew from channel to channel, the input

timing created could become irrelevant. If this were to occur, the output transistors could turn on at the same instant causing shoot through current and damaging the devices.

4.5.4 Gate Drive Suppression and Output Termination

Sometimes the gate driver output signal is switching too fast causing excessive ringing that can potentially damage the output devices. To diminish these effects, a current limiting series gate resistance can be added to the signal path. This slightly dampens the signal and limits the transient current, making it capable of driving the power MOSFET without damaging its gate oxide. For this design, a series gate resistance of 1 Ω was added. Another technique utilized in this design is transient voltage suppression at the gates. Since the gate input signal should ideally be at 10 V, 12-V Zener diodes were added between the gate and source of each device to clamp the gate-to-source voltage in the event of large overshoot.

Since the output signal of the BNG driver must be transmitted along an 18-inch cable, some form of termination is needed in order to obtain the desired signal. Careful consideration must be taken in order to implement a termination solution that does not affect the amount of drive strength needed. Series resistance was selected since it is the optimum method of termination for this design. Although this method will cause a slight degradation of signal rise time, the advantage of series termination is lower power and ultimately less drive strength required [21]. Due to various phenomena that were not accounted for in the transmission line model such as losses in the line, the termination resistor will most likely be less than the expected 50 Ω. This can be observed in the simulation results section. A termination resistance of 42 Ω yielded the best simulation results. If a parallel termination method was used, the required resistance would load the output of the BNG driver greater than the anticipated load that the electronics was designed to drive. The system has not yet been tested with the BNG and the

exact signal cabling that will be used in the final system. Since this is the case, the best way to determine the amount of termination needed is to connect the BNG driver in the final system and tune the termination value based on the resulting performance.

4.5.5 Preliminary Design of Input Logic Circuitry

Some consideration was given to the creation of an input logic circuit in order to produce all the necessary signals from a single input signal. This would eliminate the need to supply the board with four separate, precisely timed input signals. The schematic of this design can be observed in Figure 4.25. After preliminary simulations and discrete part prototyping, the design was implemented on a PCB. The schematic shown below creates a delayed input signal using an RC network. This signal along with the original input signal are sent through an AND and an OR gate to produce signals similar to those in Figure 4.4. The inverter chains and RC networks are then used to invert one signal from each of the previous logic gates and tune the circuits to be identically timed. The input logic design was not completed due to time constraints. However, the design was started and a preliminary test result can be seen in the Appendix.

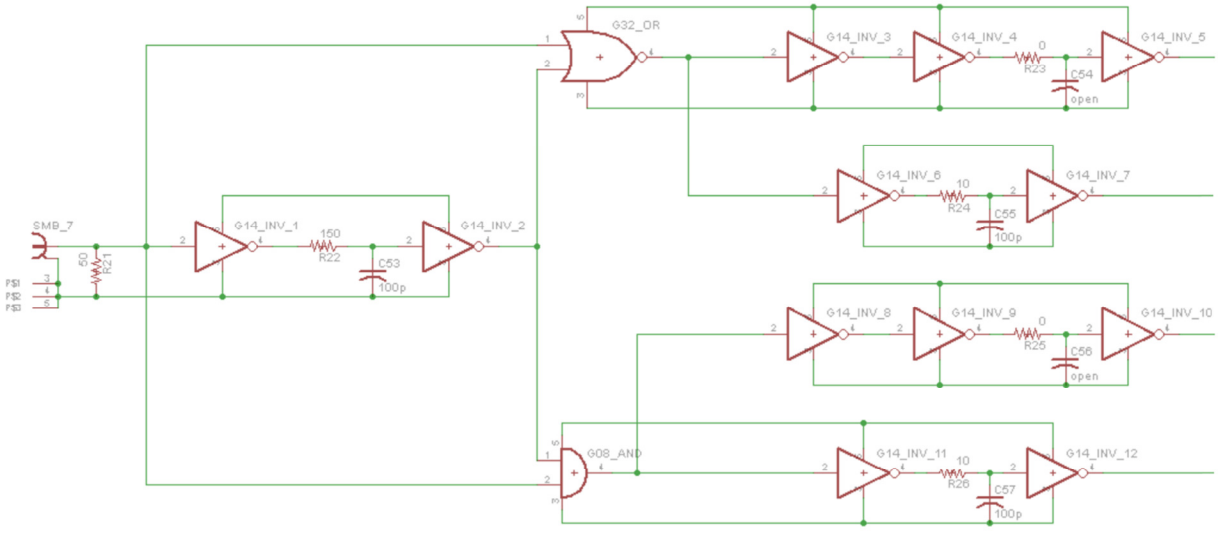

Figure 4.25: Input Timing Logic Schematic

Chapter 5

Test System and Measurement Results

5.1 Test Setup

For the proper operation of this system the following components are required: four input signals, three power supply voltages, ground, and a common potential. The three voltage levels to be supplied to the device under test (DUT) are 4 V, +50 V, and −50 V. For all testing described here, the common potential is ground. All four input signals are created with the Stanford Research Systems DG535. By utilizing four pulse channels, two fully adjustable signals are created. The DG535 also produces the complementary signals of these two adjustable signals. For the test setup, one DG535 output channel and its complement can be used for the positive side PMOS channel and negative side NMOS channel. The other channel and its respective complement can be used for the two remaining channels. The setup can be seen in Figure 5.1 below.

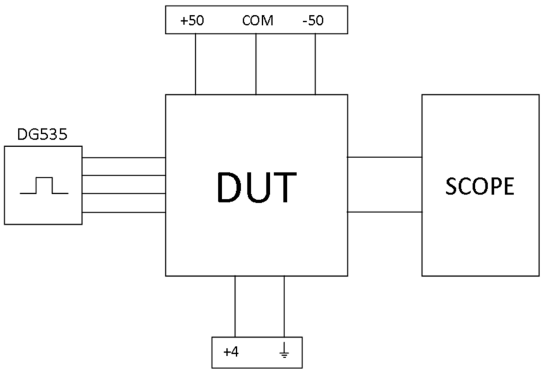

Figure 5.1: Test Setup Block Diagram

To comprehensively test the performance of this design, many variables were changed during testing to ensure consistent testing results. One main variation in the test configuration is

the load. Two main loading conditions were used throughout testing: no load and an 18-inch twisted pair of wire with a 68 pF capacitor attached across the end of the pair. In addition to varying the load of the system, various frequencies and pulse widths were also used. The frequency range outlined in the design constraints is from 200 Hz (typical) to 10 kHz (maximum). These two frequencies were the ones mainly used during testing. The pulse width of the output signal was another important specification of the design to be considered. The desired pulse width for the system is from 10 ns to 10 µs. To test for an output offset problem, the system was supplied with DC inputs. The output performed exactly as expected. Since the design works all the way to DC, the 10 µs side of the range should be perform as expected. For this reason, most of the testing focus is on the minimum pulse width and a typical pulse width of 150 to 200 ns.

5.2 BNG Driver Results

There are many test results shown in the figures (Figure 5.2 through Figure 5.21) below. Some are single-ended output signals, i.e. measured from one output signal path with respect to ground. The remaining signals are either input control signals used to drive the circuitry or differential output signals. The input signals are shown to illustrate the required control signals necessary to create the resulting output signals. Since the oscilloscope probe that was used to measure these signals was grounded very close to the high-voltage output signals, a good deal of noise was injected into some of the probed signals due to high transient currents flowing in the ground plane. This should not reflect on the actual performance of the circuitry, but rather the inherent difficulties with the measurement capabilities available.

The single-ended output signals are given to demonstrate the functionality of each side independently of the other. Since the load of this system is relatively small, approximately 60 to

85 pF, the high impedance scope probes actually load the circuit while attempting to obtain measurements. Each of the probes contributes around 15 pF of distributed capacitance to the load. The long cable of the probe also adds transmission line effects to the circuit in addition to the cabling connecting the load, which is already exhibiting transmission line qualities. These phenomena make it very difficult to view the single-ended signals without interference from the probe itself. However, there are several single-ended signals shown below to demonstrate these effects and give context to the signals that are ultimately desired, the differential output signals.

The differential signals are the most essential signals to observe in this system since they are representative of the signals supplied directly to the Bradbury-Nielsen gate. Since both single-ended signals are acting on the load simultaneously, the difference of the two essentially creates a single differential signal. In fact, the differential measurement is done in this exact manner. The negative-side output signal is subtracted from the positive-side output signal, creating a single differential signal.

To show the versatility of this design, various testing conditions, outlined in the previous section, were used to attain the figures below. While the results obtained using a BNG representative load are the most valuable results gathered from testing, the board was also tested under “no load” conditions. By doing measurements with and without a load, the two results can be compared to determine some of the contribution the load has on the circuit. However, this design was optimized for the loaded scenario.

Some of the signals acquired exhibit a small amount of what appears to be DC offset. This was investigated by supplying the appropriate DC input voltages to hold the output at ground. A DC voltage measurement was then taken at the output nodes. This confirmed that

there was no major, inherent DC offset in the design. Since the oscilloscope probes have an attenuation ratio of 10:1 and are measuring relatively large voltages, this could be a result of poor resolution in the probe or the need for calibration.

Minimum jitter is also a constraint of this design. Since jitter is difficult to measure or calculate, it was observed visually on the oscilloscope. Due to this method of measurement, a numeric value cannot be determined for the amount of jitter in the circuit. However, the design constraint was less than 10 ns of jitter. The output signals seem to exhibit much less than this amount.

All rise and fall times for 50-V transitions are under the required 15-ns constraint. The differential signal's rise and fall times for 100-V transitions are even close enough to be within this constraint. The average value of rise and fall times for the differential signals with the load is around 16.8 ns while the average for the no load case is about 10.7 ns. These fast switching times along with the high output voltages translate into an ultra-high value for the differential slew rate of this BNG amplifier. Using Equation 5.1 [22] and the average differential signal rise/fall time, the slew rate is approximately 6 kV/μs. The lowest possible pulse width required by the design constraints is 10 ns. Considering the signal transitions take longer than this to complete, 10 ns is optimistic. While it is possible that a lower pulse width may be possible, the minimum pulse width with optimum signal performance maintained is just under 50 ns. In relative terms, this is extremely close to the required range of pulse widths which spans from 10 ns to 10 μs.

$$SR = \frac{dV_{OUT}}{dt} \tag{5.1}$$

Figure 5.2 shows the input signals supplied to the circuit during nominal operation. Each signal is oriented in such a way that each of the output signals will remain at their respective +50

V and −50 V for the majority of the time, deflecting all ions from passing through the aperture. The “on” or “off” time of each input signal corresponds to the amount of time that ions are allowed to pass through the gate and received at the detector. A time delay of approximately 25 ns can also be seen between each of the transitioning edges in signals VIN1 and VIN2. This is done to prevent shoot through current in the output stage of the circuit. Essentially identical timing can also be seen in signals VIN3 and VIN4. By assuming the inherent delay throughout each signal path is closely matched, this timing scheme is used to achieve similarly timed output signals. As described in previous chapters, many layout and design techniques were used to ensure that each channel exhibits equivalent inherent propagation delays.

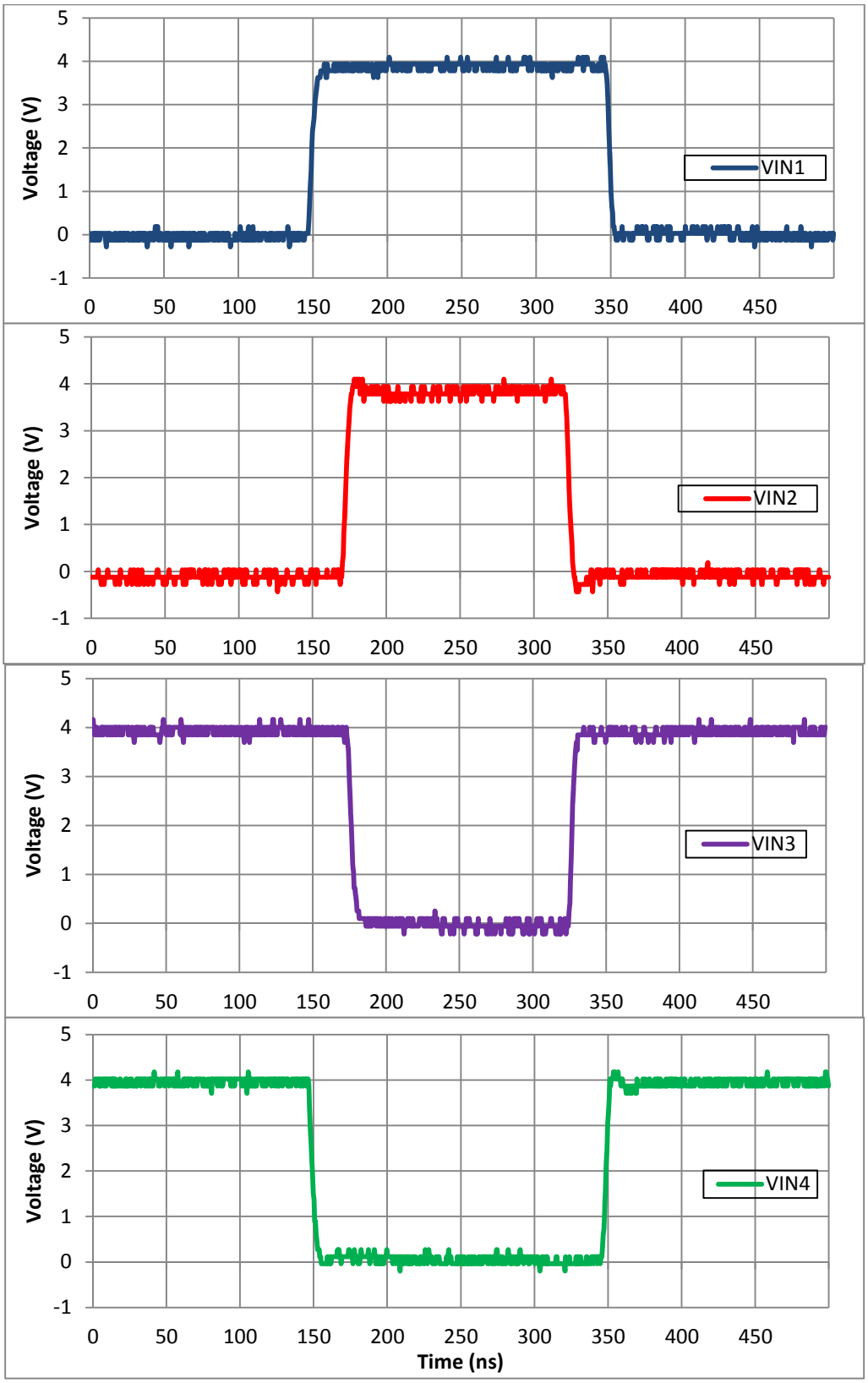

Figure 5.2: Input Signals

Figure 5.3 and Figure 5.4 show the intermediate signals throughout each signal path that drive the output stage. Figure 5.3 is the output signals of each input isolator device. The voltage transition level of each of these signals is set at 5 V from the ground potential of each gate driver. These voltages are supplied by the power supply network to the output of each isolation device. The ringing that is exhibited in each of these signals is most likely due to the high current transitions due to the output switching being coupled through the scope probes. The timing of each of these transient rings corresponds to the timing of the output signal transitions.

The signals in Figure 5.4 show the signals that drive each of the output transistors. These signals are essentially amplified versions of the signals from Figure 5.3 with higher current drive capabilities. As described above, the signals in Figure 5.4 also contain noise coupled from the output signal transitions when measured.

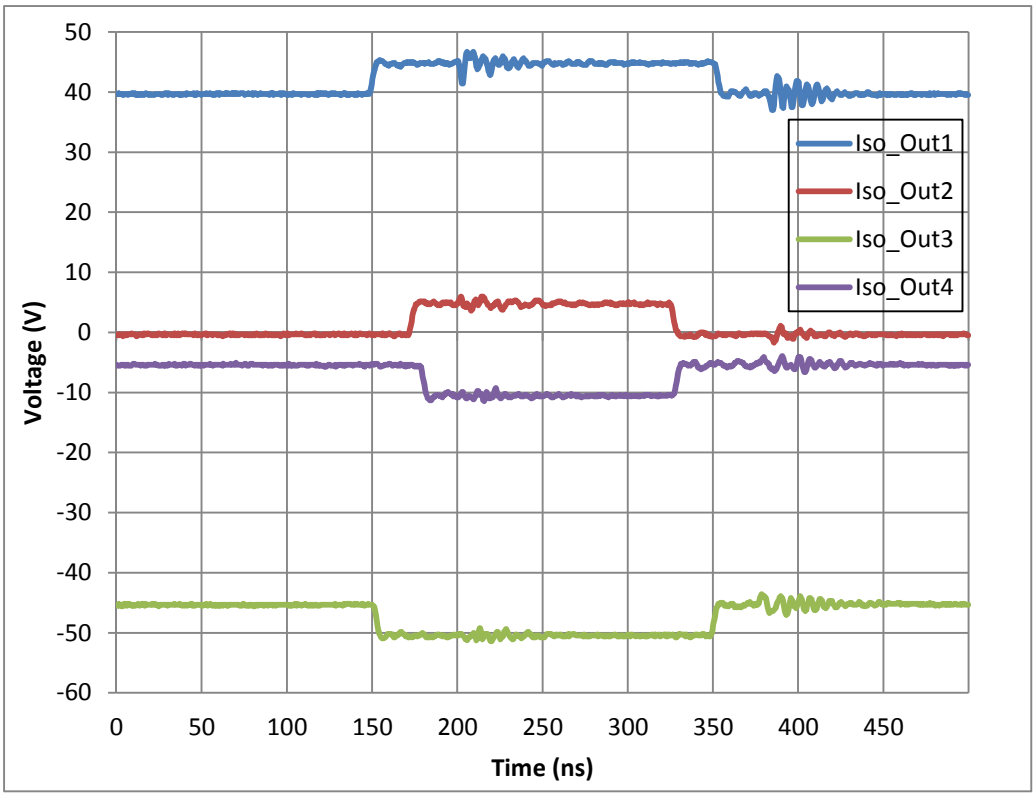

Figure 5.3: Input Isolator Output Signals

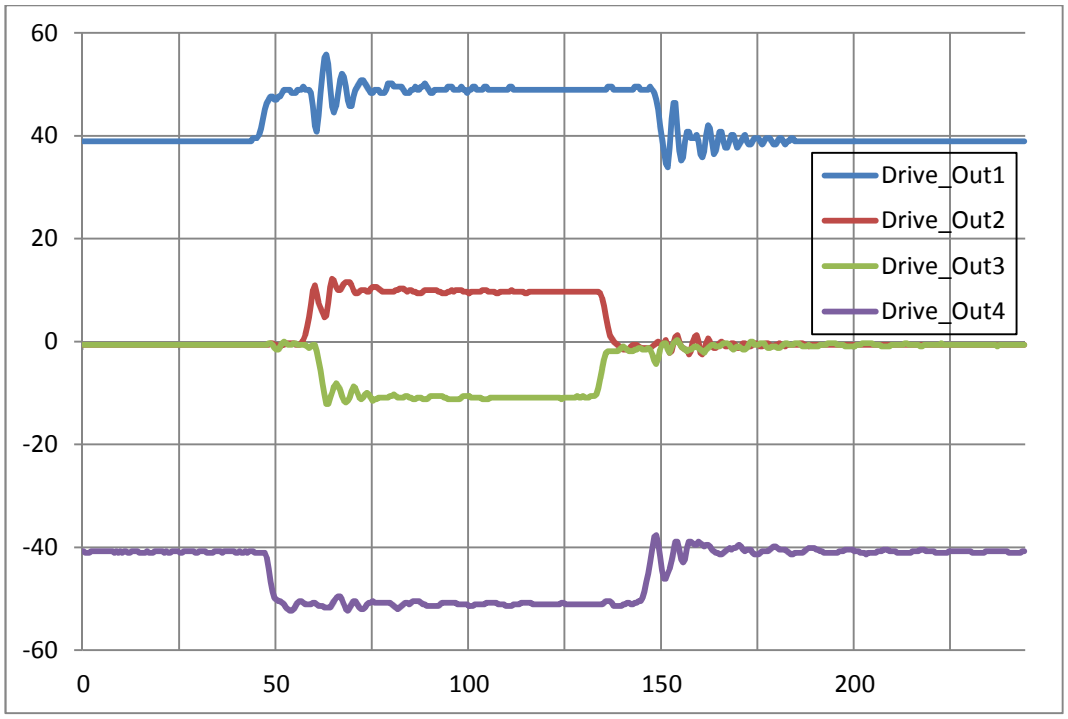

Figure 5.4: Gate Driver Output Signals

It is important to remember that the BNG is only subject to the differential signal created at the output. The single-ended results are only shown below to give perspective of how each side works independently and is then applied to the load to create the differential signal driving the gate. Much of the undesired signal attributes that can be seen in the single-ended signals are contributed by the parasitics added to the circuit by the measurement equipment. These effects are not as prominent in the differential signal since some of them are essentially canceled out when measured differentially. Figure 5.5 shows each of the single-ended outputs of the circuit with 200 Hz input signals and no load. The typical operation frequency of this design when integrated into the final application will be around 200 Hz but will have a load. However, this measurement is given to exhibit general functionality of the design at this frequency. Figure 5.6 is the differential signal measurement derived from the single-ended signals in Figure 5.5. Any

offset that is apparent is due to the high-voltage measurement calibration of the scope probes as described above.

Some inherent ringing is still present in the differential signal. However, since there is no load other than that contributed by the scope probes in this measurement, the differential output signal is underdamped resulting in some unwanted ringing. As can be seen in later figures, adding a load to the circuit helps to dampen the differential output signal.

A slight timing mismatch is also apparent in Figure 5.6 indicated by a small distortion in the transitioning edge of the signal. Since there is no load in this case and the rise and fall times are relatively fast, slight timing mismatch that is inherent between the +50 V and −50 V signals is manifested by this type of distortion. Once the circuit is loaded, the transitioning times are slowed and this amount of mismatch becomes insignificant and no longer apparent.

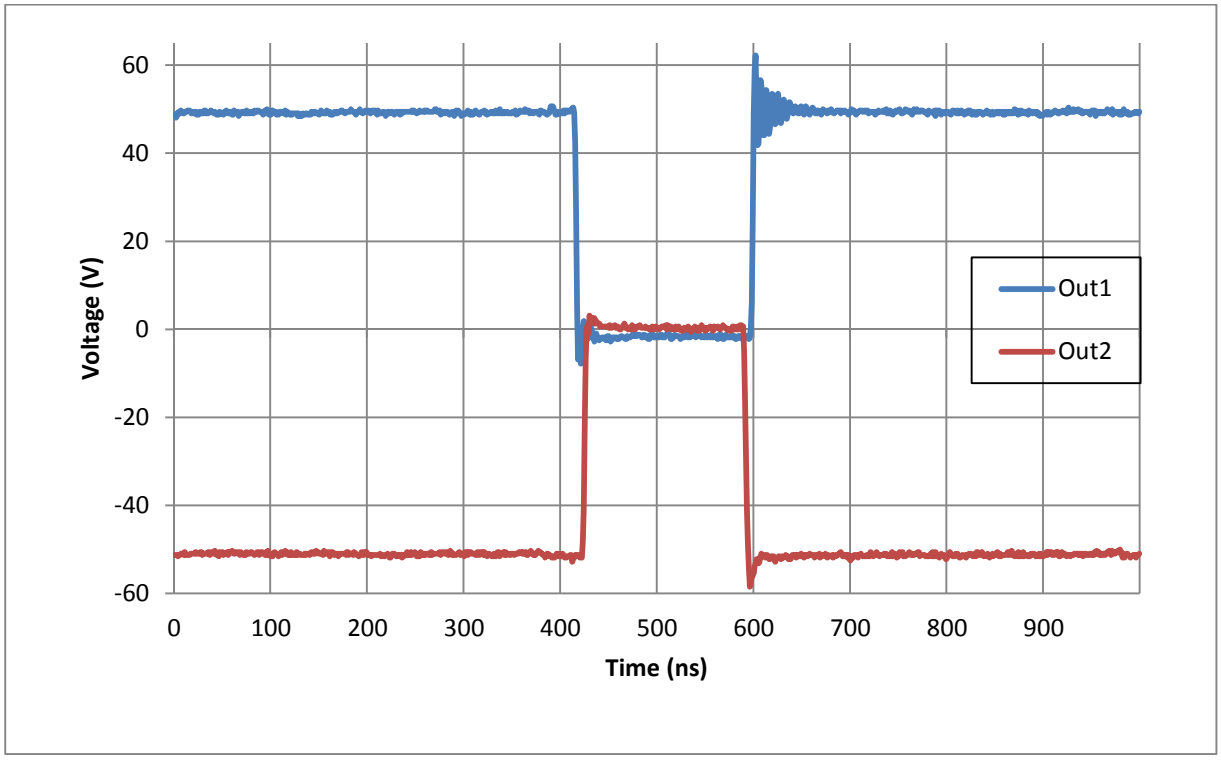

Figure 5.5: Single-Ended Output Signals – 200 Hz, No Load

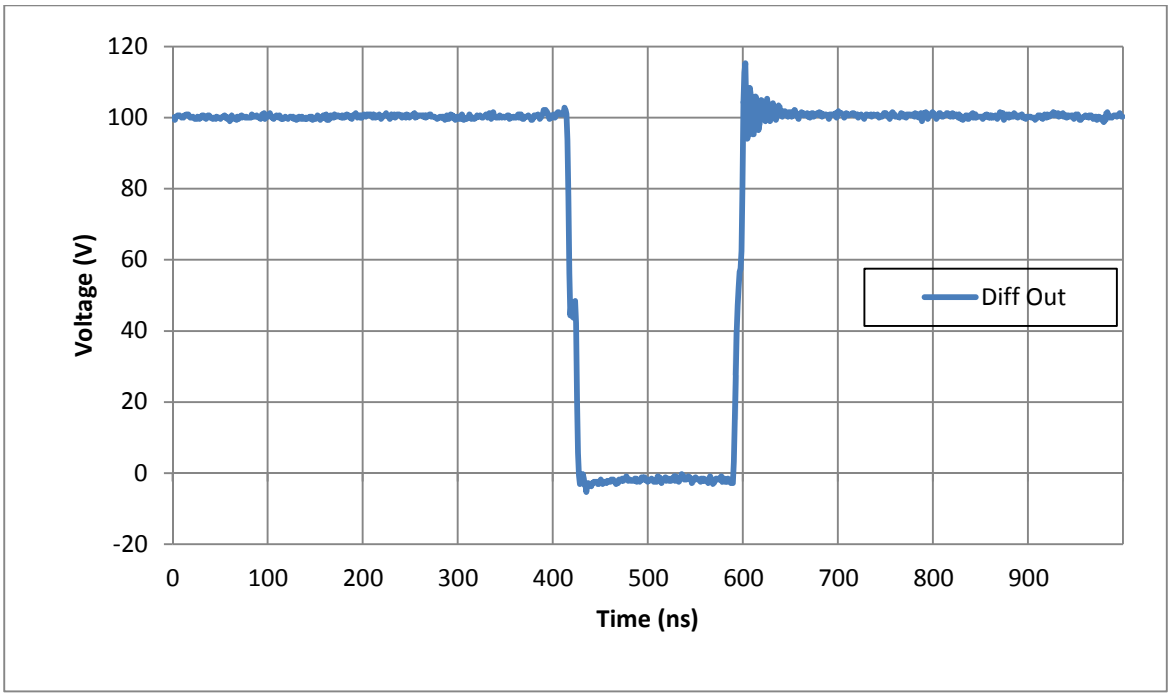

Figure 5.6: Differential Output Signal – 200 Hz, No Load

Figure 5.7 and Figure 5.8 show similar signals as above but are measured after a load is added to the circuit. An 18-inch twisted pair of wire with a 68 pF capacitive load is added to the circuit to represent the BNG's impedance along with the cabling needed to connect the electronics to the BNG through the vacuum. By observing the single-ended signals in Figure 5.7, the signals seem to be more distorted than in the no load case. However, the addition of cabling as part of the load causes the load to act as a transmission line causing ringing while measurements are taken. Since these effects are basically the same magnitude in both single-ended signals, they effectively cancel out in the differential signal. The signal seen in Figure 5.8 is a good representation of a signal that is supplied to the BNG after the electronics are implemented in the final ORISS application. This signal was measured at the typical operating frequency of 200 Hz.

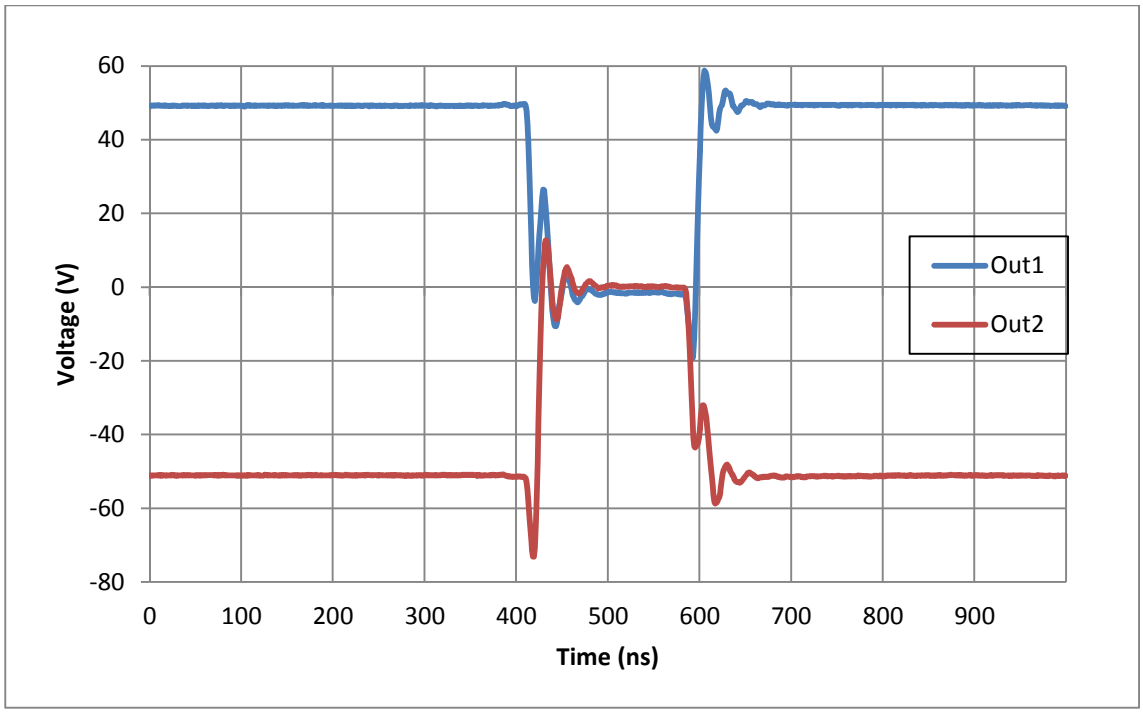

Figure 5.7: Single-Ended Output Signals – 200 Hz, 18-in. Twisted-Pair Cable, 68 pF Load

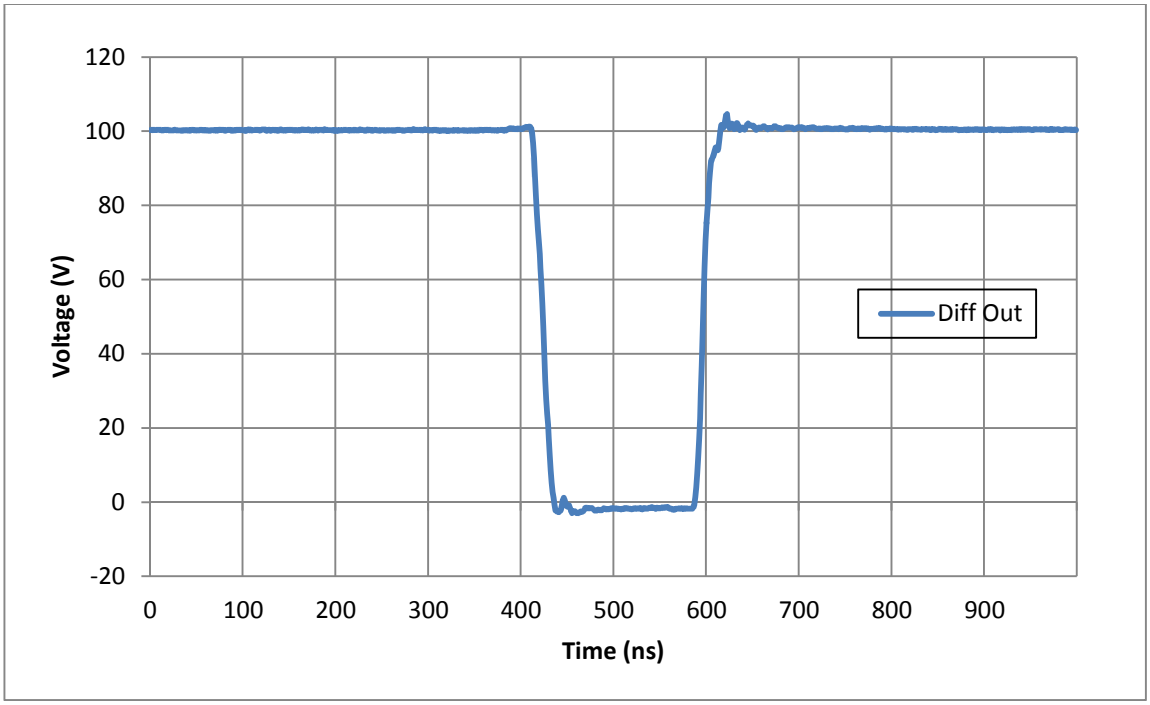

Figure 5.8: Differential Output Signal – 200 Hz, 18-in. Twisted-Pair Cable, 68 pF Load

These measurements were repeated for the no load and the loaded case to ensure proper operation of the design at the high side of the desired operable frequency range, 10 kHz. Similar phenomena that were described above can also be seen in Figure 5.9, Figure 5.10, and Figure 5.11. However, these signals are used to illustrate basic functionality and give perspective to how the differential signals were derived. The important signal that could potentially be used to drive the BNG is shown in Figure 5.12. Just as with the loaded, differential signal exhibited at 200 Hz, the 10 kHz signal in Figure 5.12 also has sufficient attributes with almost no apparent distortion or inadequacies.

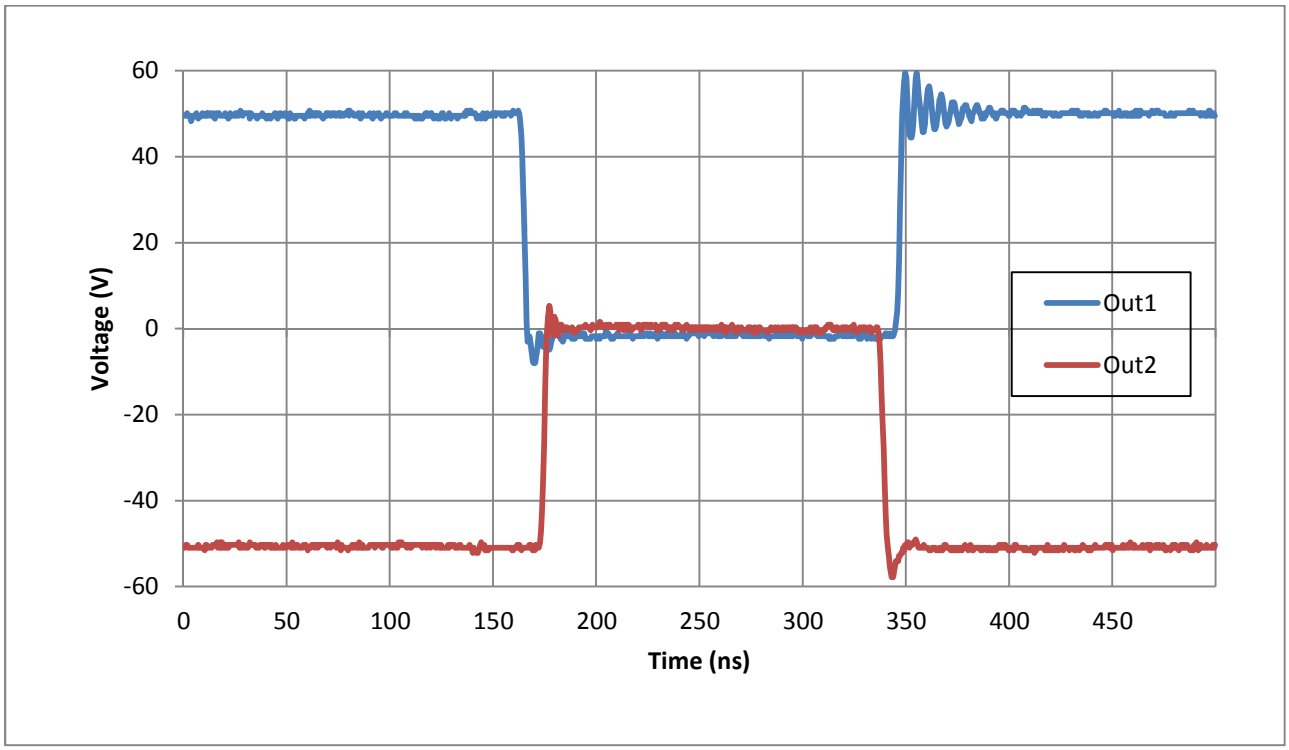

Figure 5.9: Single-Ended Output Signals – 10 kHz, No Load

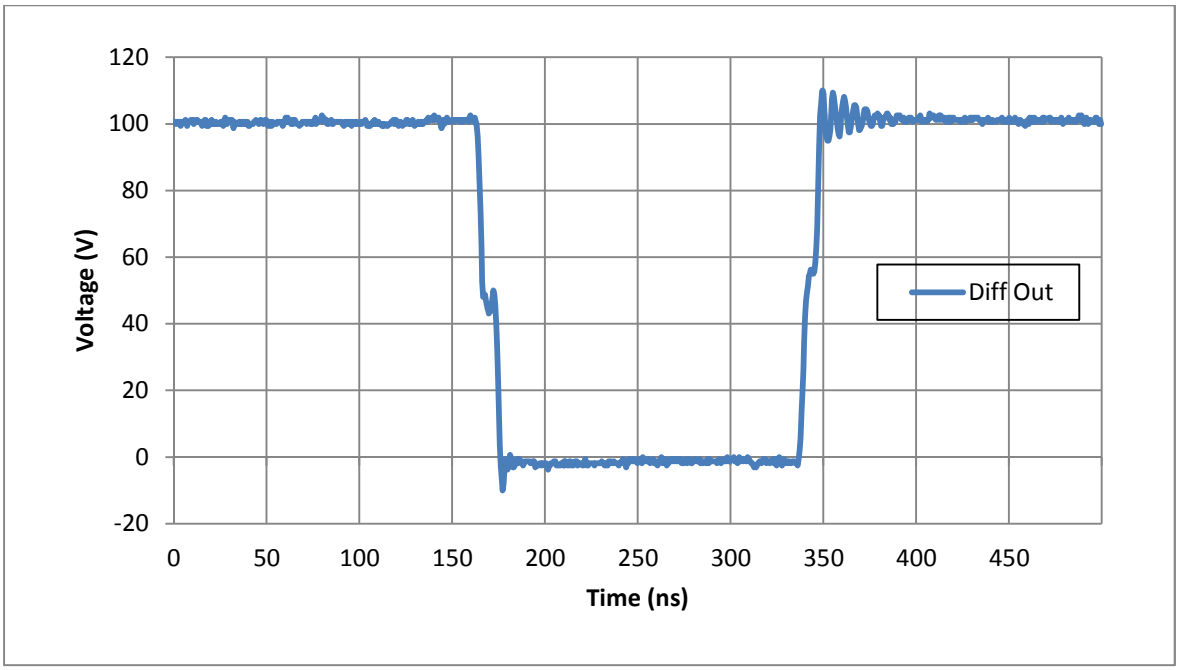

Figure 5.10: Differential Output Signal – 10 kHz, No Load

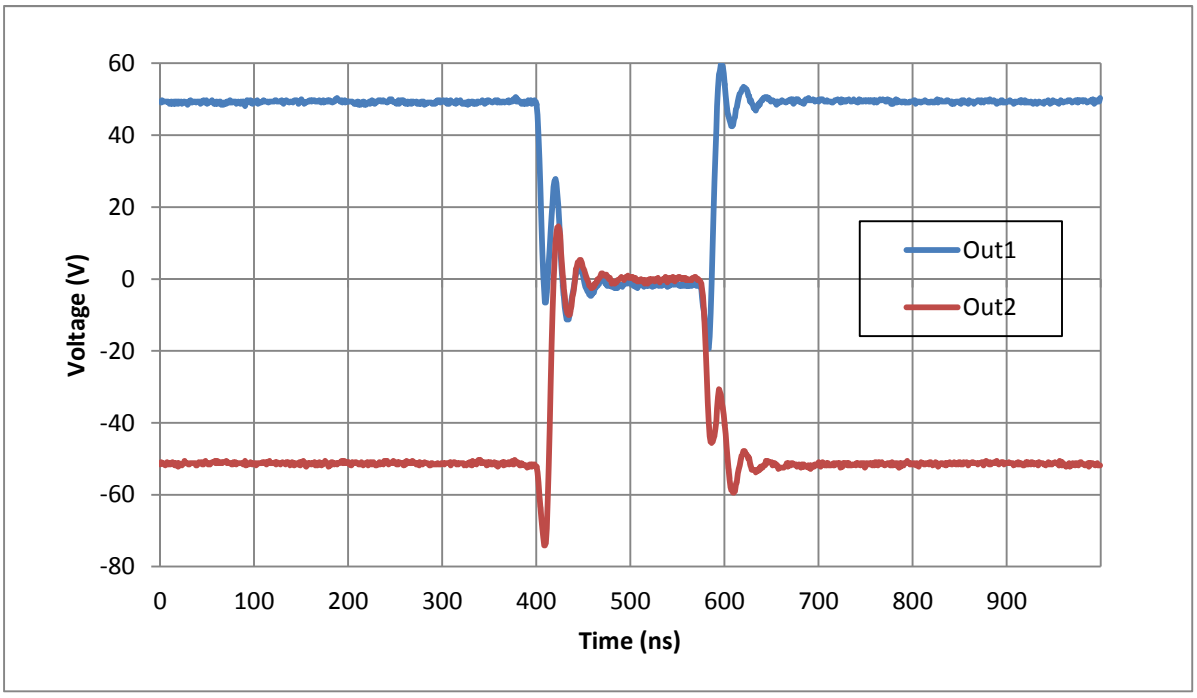

Figure 5.11: Single-Ended Output Signals – 10 kHz, 18-in. Twisted-Pair Cable, 68 pF Load

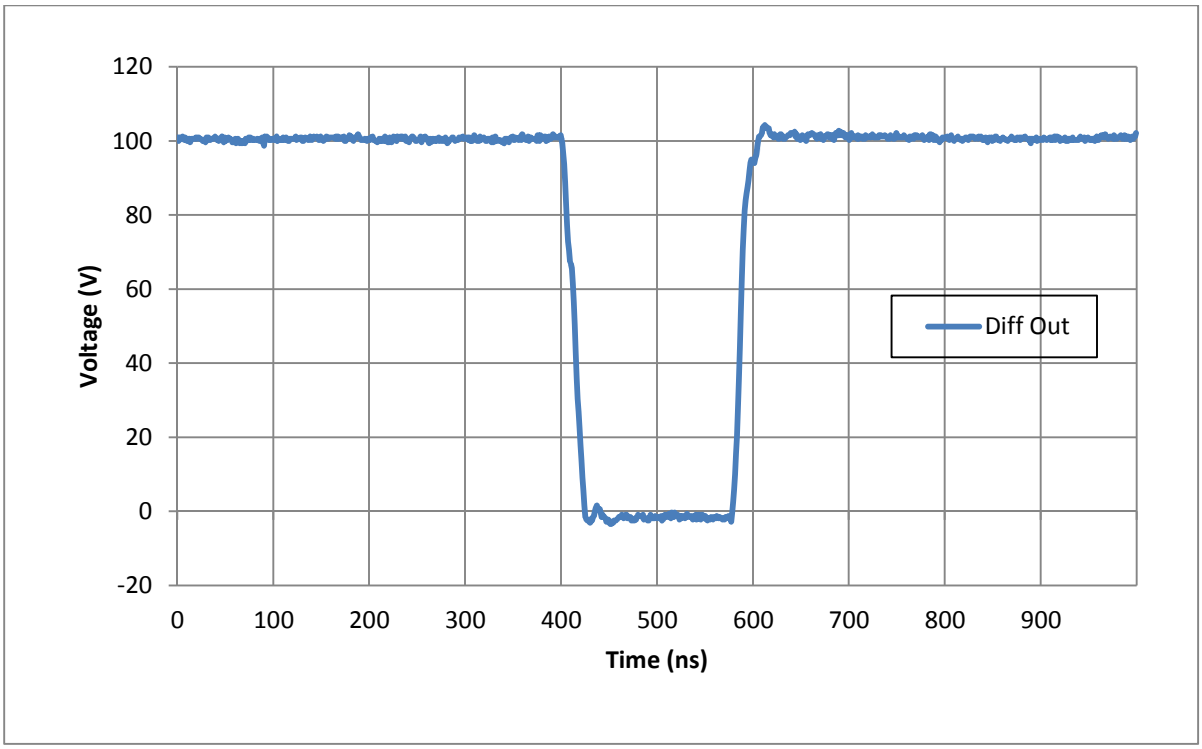

Figure 5.12: Differential Output Signal – 10 kHz, 18-in. Twisted-Pair Cable, 68 pF Load

General functionality of this design with a typical pulse width around 200 ns has been explored. The results shown by the differential signals at 200 Hz and 10 kHz with a representative BNG equivalent load are promising. Now that most attributes have been thoroughly tested, the minimum pulse width possible is a vital parameter to investigate and test. Figure 5.13 shows the input signals supplied to attain a minimum pulse width of the differential output signal. Just as in previous testing, a delay of around 20 ns is induced between signals to prevent shoot through current in the output stage. The pulse widths of the input signals used are about 70 ns and 30 ns to achieve an overall output signal pulse width of around 50 ns.

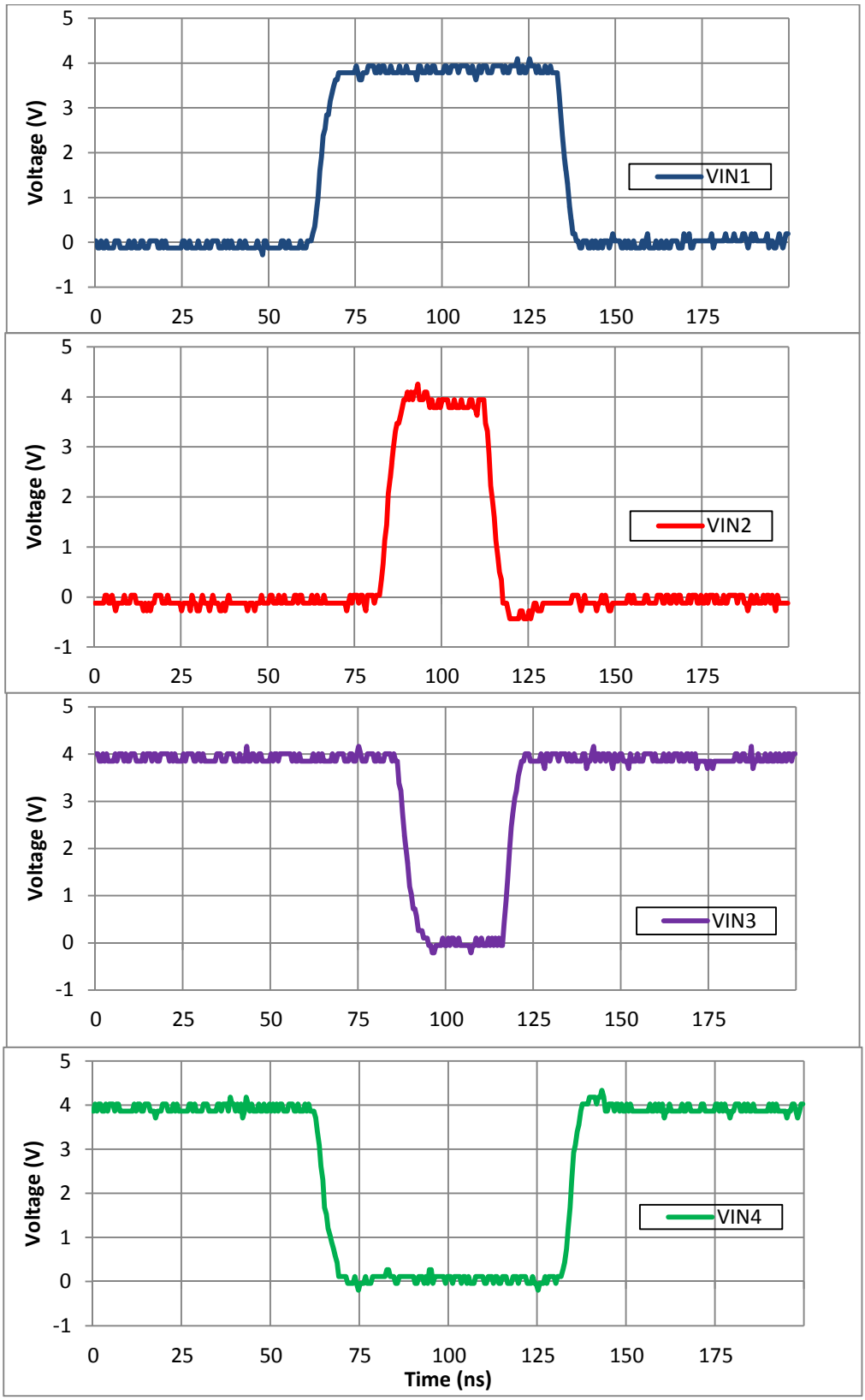

Figure 5.13: Input Signals – Min PW

The no load measurement of the single-ended output signals shown in Figure 5.14 seems to exhibit a larger amount of time delay between each of the signals. However, this is relative to the much smaller pulse width causing this difference to seem larger. As later results show, this delay only slightly affects the minimum transition times attainable. Figure 5.15 follows the same trend as the other previously discussed no load cases. Once a load is added to this configuration, the results are much more desirable.

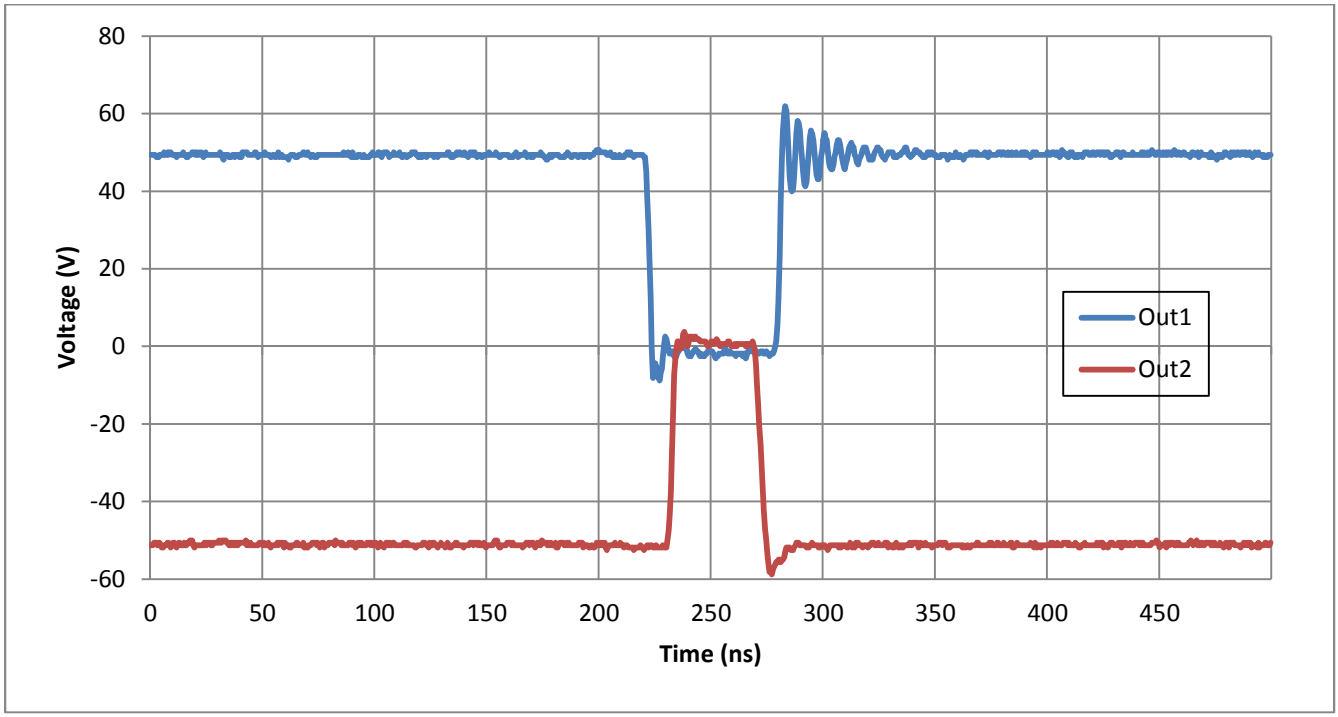

Figure 5.14: Single-Ended Output Signals – 200 Hz, No Load – Min PW

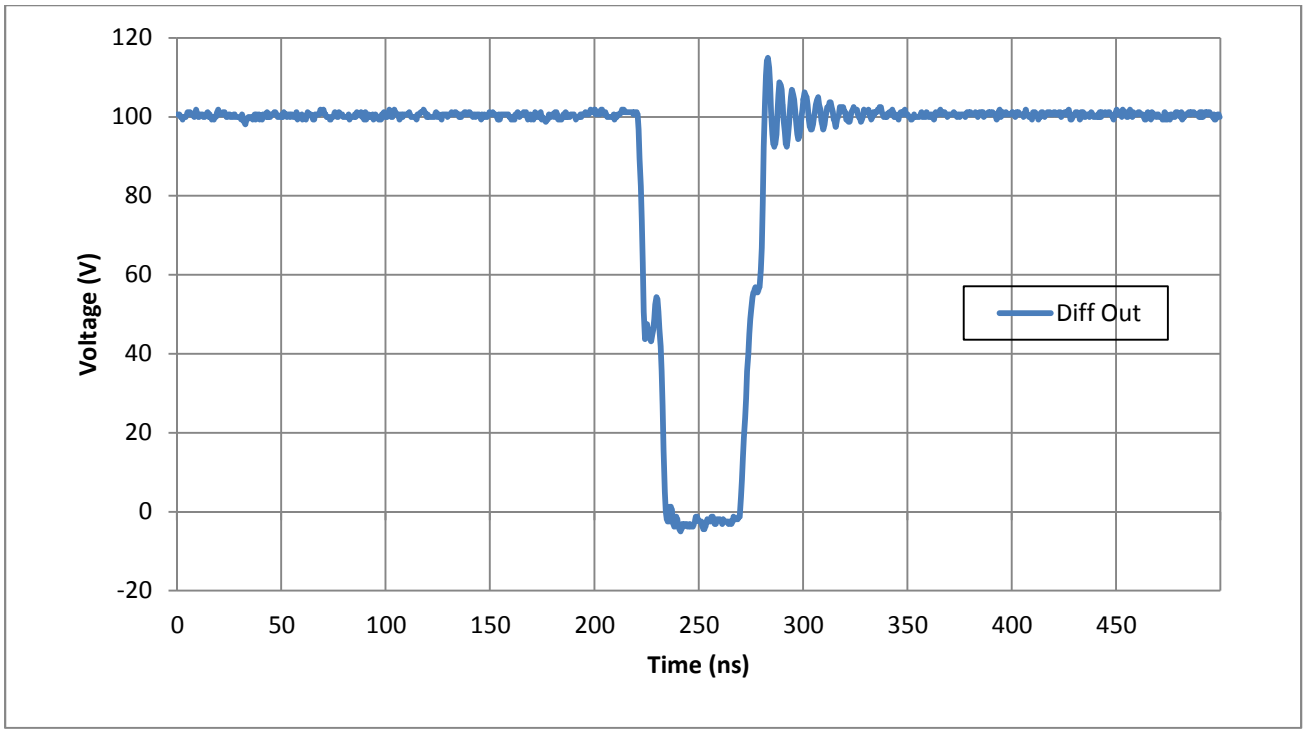

Figure 5.15: Differential Output – 200 Hz, No Load – Min PW

Figure 5.16 and Figure 5.17 are the measurement results using the minimum pulse width at an operating frequency of 200 Hz and the using the typical testing load. The differential output signal shown in Figure 5.17 has a minimum pulse width of about 50 ns and has little to no distortion. With attributes such as these, this signal should be very effective when utilized in the application to separate isomers.

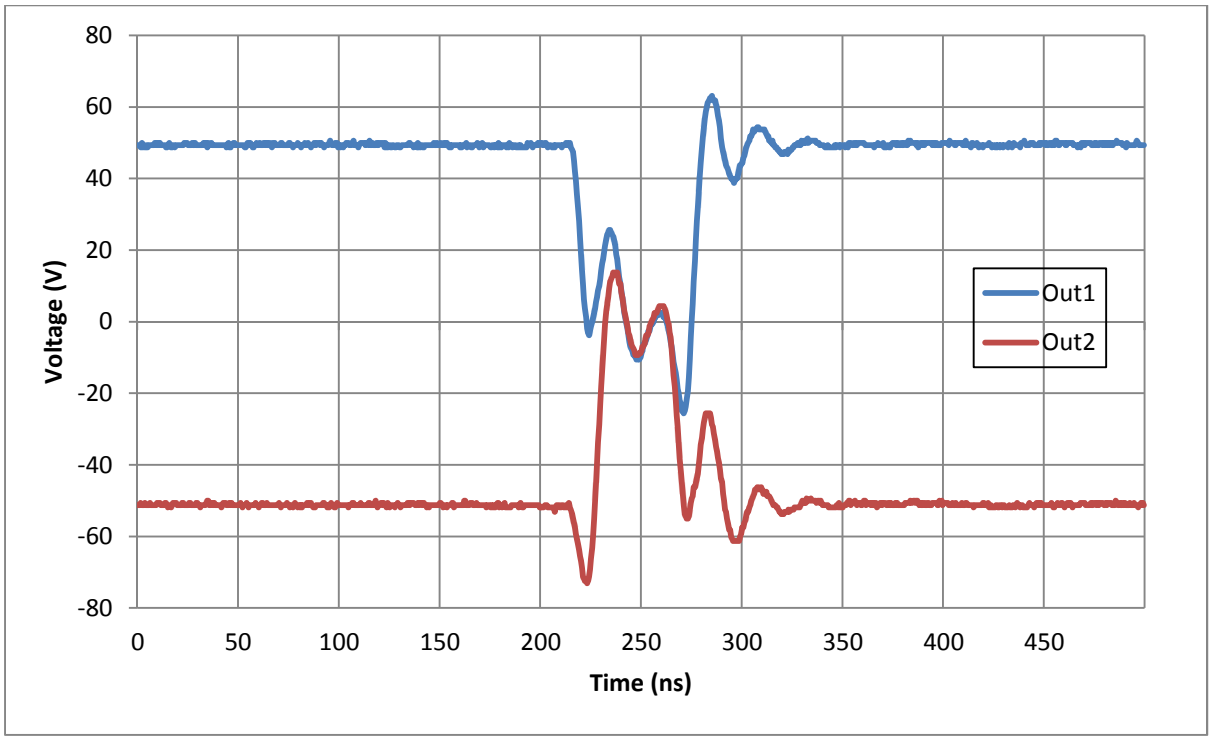

Figure 5.16: Single-Ended Output Signals – 200 Hz, 18-in. Twisted-Pair Cable, 68 pF Load – Min PW

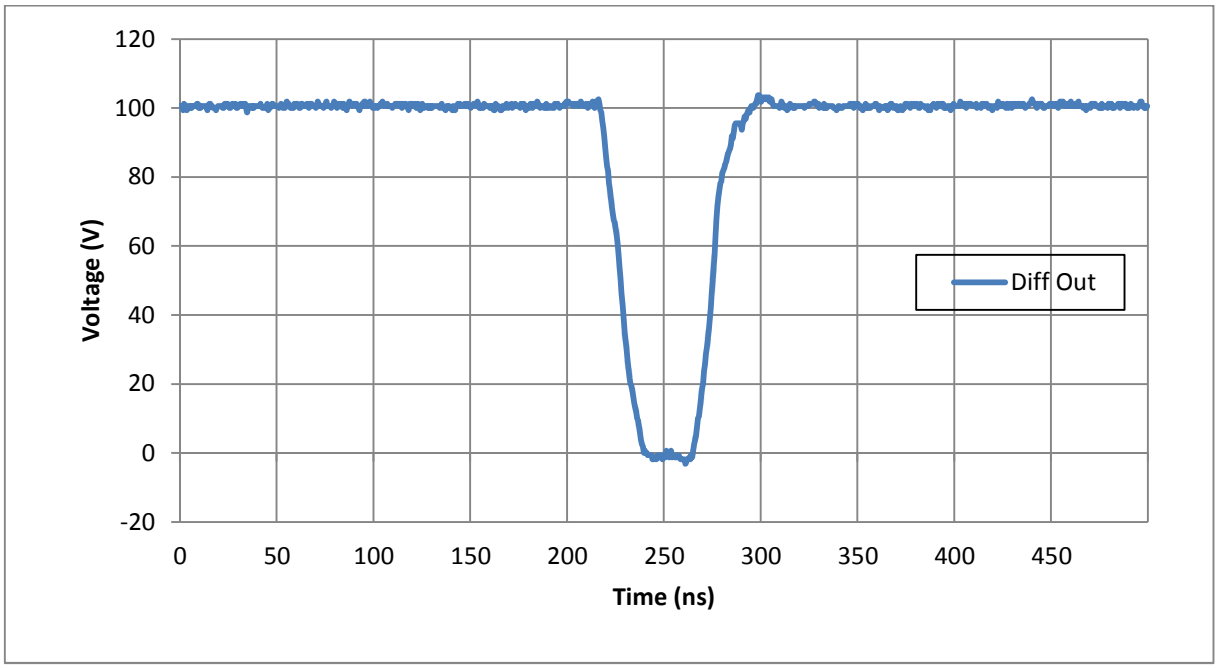

Figure 5.17: Differential Output Signal – 200 Hz, 18-in. Twisted-Pair Cable, 68 pF Load – Min PW

Figure 5.18 through Figure 5.21show the single-ended and differential signals for the same minimum pulse width test conditions used above. However, these tests are conducted to ensure proper operation at a frequency of 10 kHz. Figure 5.21 also exhibits the desired characteristics of a BNG driving signal. The performance of this system has been thoroughly tested and can be observed by the inspection of Figure 5.2 through Figure 5.21. Table 5.1 summarizes the results obtained during these measurements. Through further study of the figures and table in this section, one can conclude that the results of these tests were successful. In addition, the results had small variations across various test setups indicating a very robust design. Since the BNG is only subject to the differential output signals, the data obtained from these signals are shown in bold in Table 5.1.

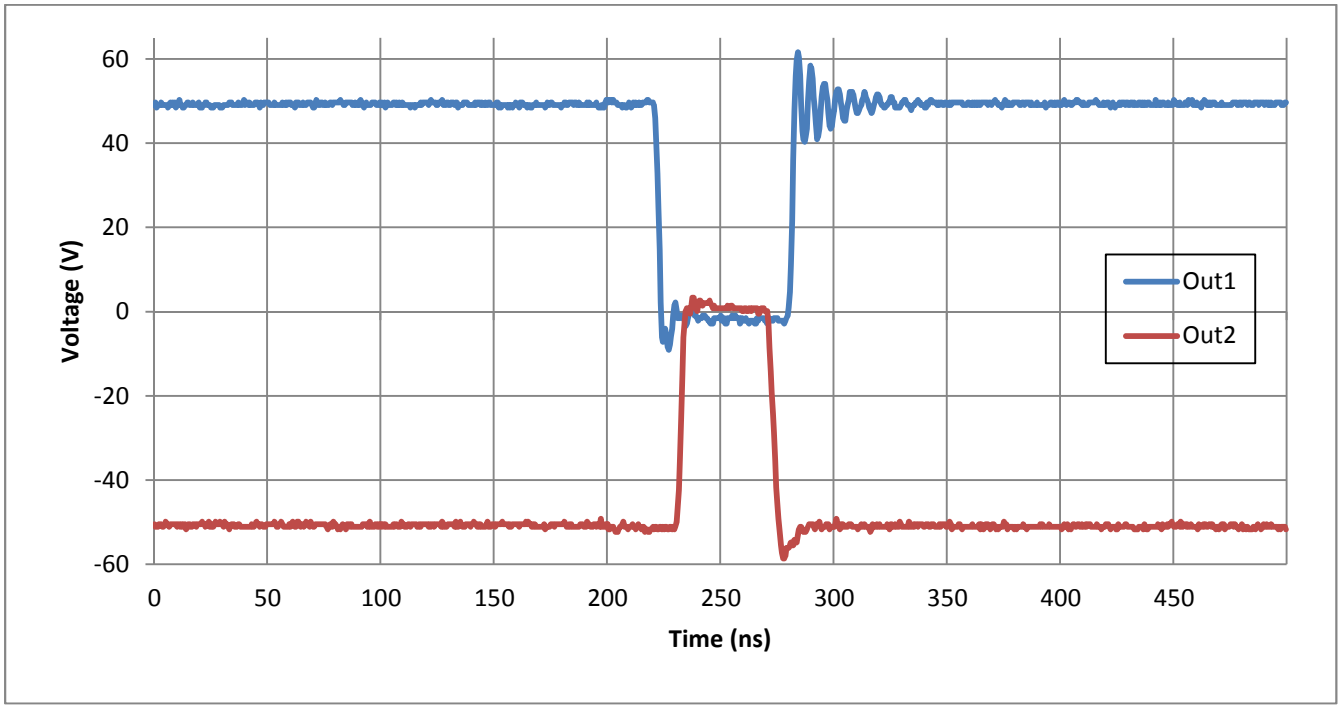

Figure 5.18: Single-Ended Output Signals – 10 kHz, No Load – Min PW

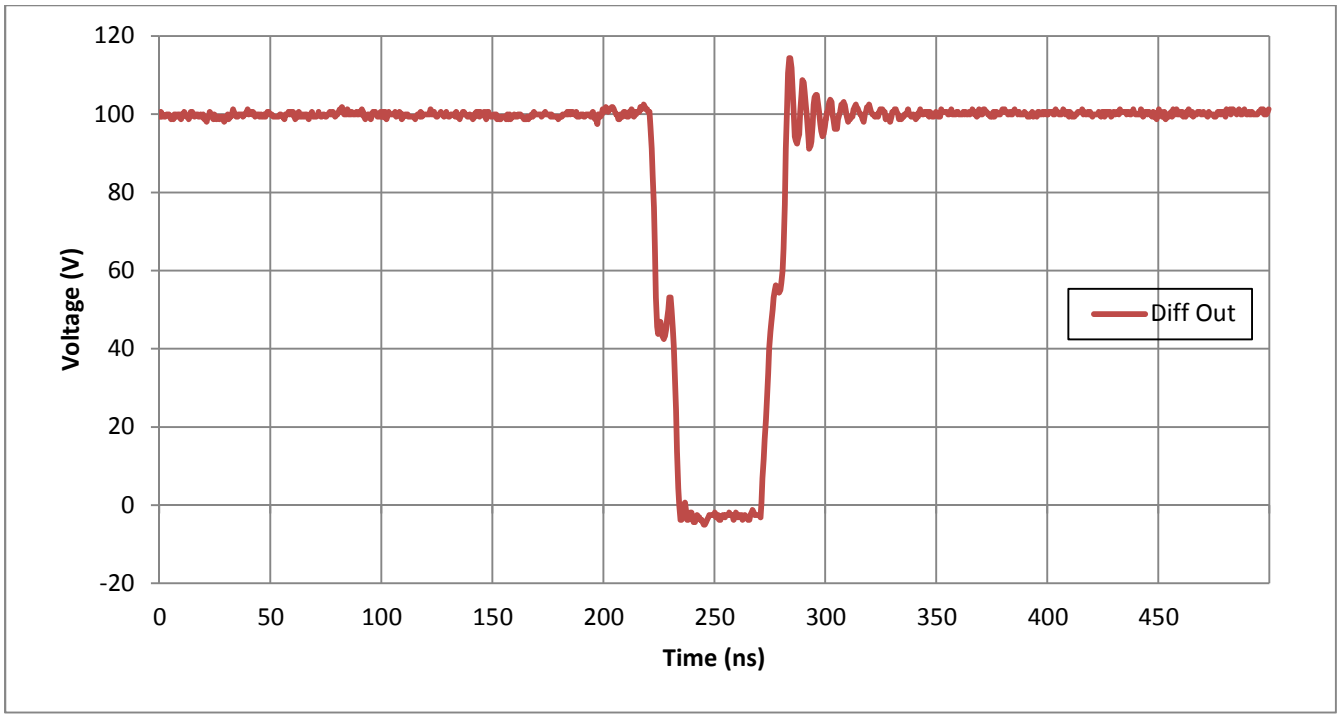

Figure 5.19: Differential Output Signal – 10 kHz, No Load – Min PW

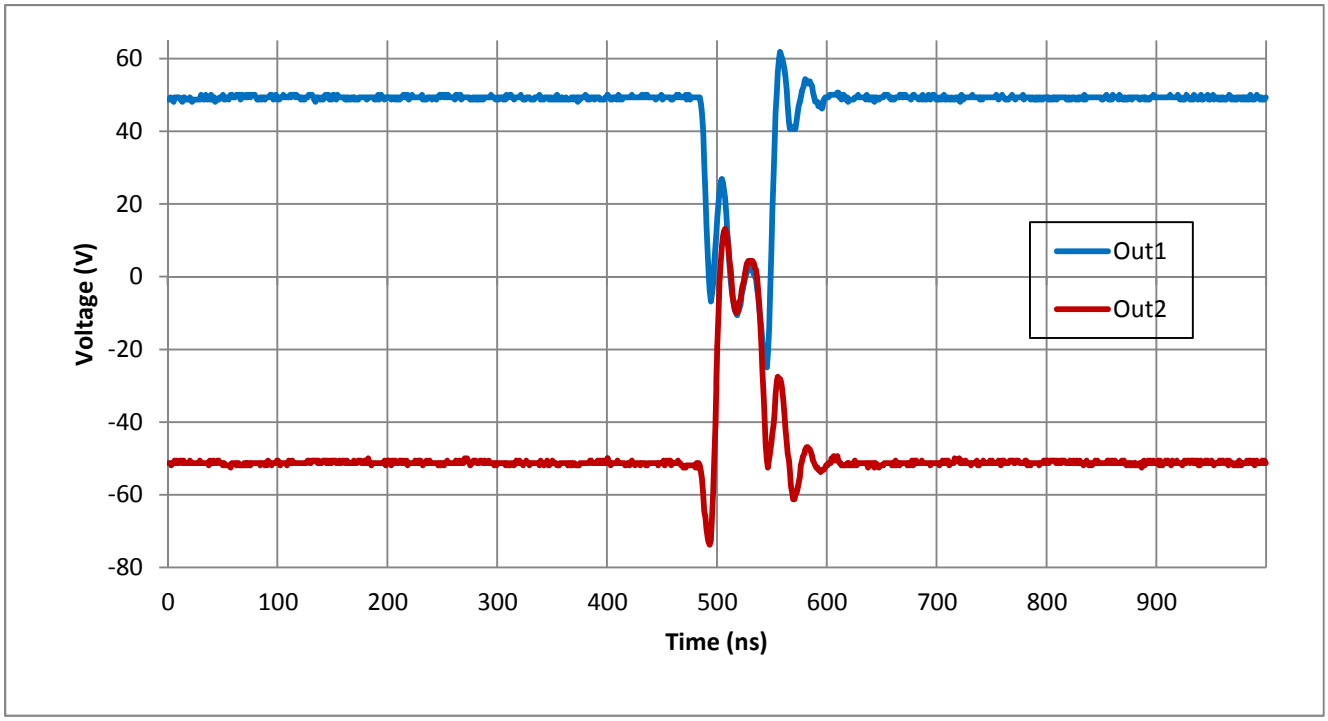

Figure 5.20: Single-Ended Output Signal – 10 kHz, 18-in. Twisted-Pair Cable, 68 pF Load – Min PW

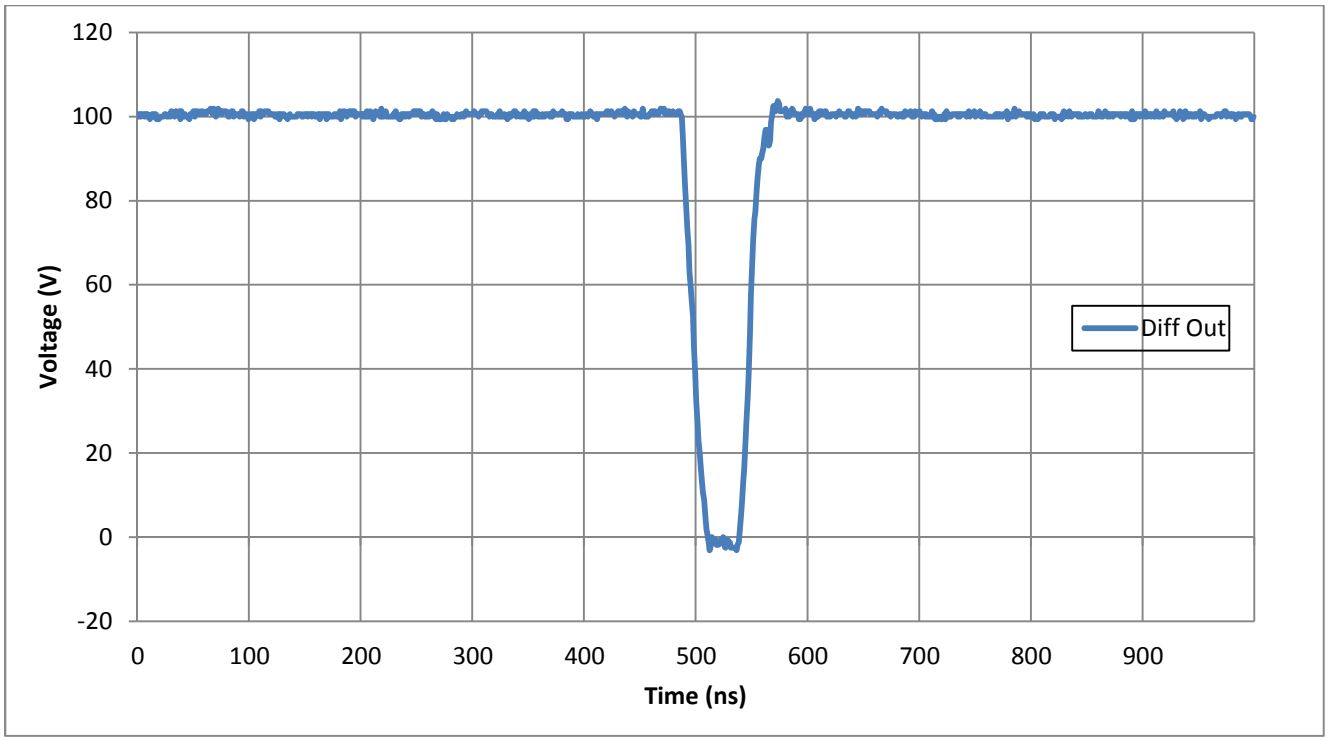

Figure 5.21: Differential Output Signal – 10 kHz, 18-in. Twisted-Pair Cable, 68 pF Load – Min PW

Table 5.1: Test Results Output Signal Rise and Fall Times

		+50		−50		Differential	
Load	**Frequency (Hz)**	**Rise Time (ns)**	**Fall Time (ns)**	**Rise Time (ns)**	**Fall Time (ns)**	**Rise Time (ns)**	**Fall Time (ns)**
None	200	2.5	2.5	3	4	**9**	**10.5**
18 in./68pF	200	5	5	5	9	**14**	**18**
None	10,000	3	2.5	3	3.5	**10**	**11**
18 in./68pF	10,000	4	6	4	8	**14**	**18**
None - Min PW	200	2.5	2.5	3	4.5	**10.5**	**12**
18 in./68pF - Min PW	200	6.5	5	6	4	**17**	**17.5**
None - Min PW	10,000	2.5	2.5	3	4	**10.5**	**12**
18 in./68pF - Min PW	10,000	7	5	5	8	**18**	**18**

Chapter 6

Conclusions

6.1 Summary

The design of an ultra-high slew rate Bradbury-Nielsen gate driver was presented in this thesis. A 100-V differential output signal with very low pulse width capabilities and high-voltage input isolation was implemented in order to separate isomers with high resolution. This design was initially tested for basic functionality using no load. A load to match the inherent impedance of the BNG was then constructed. This load also provides a method of signal transmission into the vacuum such that the desired signal is supplied to the BNG. All factors considered, it was determined that a 18-inch twisted-pair cable with a 68 pF capacitor connected between the leads would be the most representative load of the gate after implemented in the overall system. A similar load model was developed and used for simulation purposes. The results obtained from simulation closely resembled the results of the implemented design.

Full functionality of this design was confirmed in the measured results. While constraints of the design required 15-ns rise/fall times for a 50-V transition, this implementation is capable of transitioning 100 V in a similar amount of time with an average time of 16.8 ns. All design constraints for this BNG driver were met, or exceeded, with the exception of the minimum pulse width. This constraint was implausible for this design since the rise and fall time minimums were greater than the minimum pulse width requirement. The pulse width constraint was established due to the desire for extremely high resolution of the overall separation solution. By establishing such a low required value, an optimum minimum is attained. The design described in this thesis is able to maintain a pulse width of less than 50 ns with high signal fidelity. The pulse width of

this signal could be reduced, but the signal integrity could not be assured at such low values. By possessing a pulse width slightly higher than twice the rise or fall time, an optimum resolution of the separator is attained.

6.2 Future Work

Although this design is more than sufficient for the ORISS system, additional design considerations could be considered. Since access to the BNG was limited, the electronics have not been tested with its true load. Testing with this configuration is desired before finalizing this design within the system. The exact contribution of the load is not known, so the termination resistance of the output signal to the BNG needs to be calibrated once it is integrated into the system. Access to high voltage levels was also limited during testing in the ICASL lab. Additional testing with a common-mode offset voltage reference around 600 V should also be conducted to ensure the expected input isolation from the iCoupler is sufficient.

Adjustable output voltage levels were also mentioned in design considerations. This design should provide similar performance results down to the desired 25 V. However, testing to confirm this should be conducted. If any problems exist when lowering the voltage supply levels, the biasing resistors in the power network could be adjusted to compensate for any deficiencies.

As can be seen from the input timing logic test results in the Appendix, some refinement of this logic is required before implementation within the system. Although some signal optimization is needed, the timing of the signals seems to be sufficient to use as control signals to the system.

Finally, on-board power generation for ±50 V could be desired in the future. If adjustable power supplies are deemed undesirable, a fixed supply created from 110-V AC could be

implemented for simplified ease-of-use. This is something that needs to be reviewed once the designed is incorporated into ORISS.

References

[1] Nigel Saunders, *Creative Chemistry*, (2009, December 29), http://www.creative-chemistry.org.uk/molecules/isomers.htm.

[2] H. K. Carter, *Construction, Optimization and First Experiments: Oak Ridge Isomer Spectrometer and Separator (ORISS)*, 2009.

[3] V. A. Shchepunov, *et al*., *Non-linear Beam Dynamics in High Resolution Multi-pass Time of Flight Mass Separator*, Particle Accelerator Conference. Knoxville, TN. 2005.

[4] H. K. Carter, *et al.*, *Development of Compact Isobar Separator for Study of Exotic Decays using Multi-pass Time-of-Flight Principle: MTOF*.

[5] Joel R. Kimmel, Friedrich Engelke, Richard N. Zare, "Novel method for the production of finely spaced Bradbury-Nielsen gates," *Review of Scientific Instruments*, Volume 72, Number 12, December 2001.

[6] H. K. Carter, *et al.*, *Development of Compact Isobar Separator for Study of Exotic Decays*, 2007.

[7] International Rectifier, *Transformer-Isolated Gate Driver Provides very large duty cycle ratios*, AN-950.

[8] Ronn Kliger, "IEEE Instrument & Measurement Magazine," *Integrated Transformer-Coupled Isolation*, March 2003.

[9] Analog Devices, *5 kV RMS Quad-Channel Digital Isolators: ADuM4400/ADuM4401/ADuM4402*, Datasheet, 2009.

[10] Abhijit D. Pathak, *MOSFET/IGBT Drivers Theory and Applications*, Application Note AN0002, 2001.

[11] Texas Instruments, *Single 9-A High Speed Low-Side MOSFET Driver with Enable*, Datasheet, SLUS504E. 2002, September 27. Revised December 2010.

[12] Texas Instruments, *Power Management: MOSFET Gate Drivers from Texas Instruments*, Datasheet, SLUB005A, 2006.

[13] John Ardizzoni, "Analog Dialogue," *A Practical Guide to High-Speed Printed-Circuit-Board Layout*. 2005, September.

[14] Pulse: A Technitrol Company, *Understanding Common Mode Noise*, G019.A (4/99).

[15] J. F. Pierce and T. J. Paulus, *Applied Electronics*, Bell & Howell Company, 1972.

[16] TDK, *Common Mode Filters (SMD) For High-speed Differential Signal Line/General Signal Line*, Datasheet, 008-02/20100405/e9712_acm.

[17] Zetex, *ZXMC10A816N8 100 V SO8 Complementary Dual enhancement mode MOSFET*, Datasheet, Issue 1.3, March 2009.

[18] Microchip, *MCP1801: 150 mA, High PSRR, Low Quiescent Current LDO*, Datasheet, DS22051C, 2009.

[19] X. M. He, Kingbright, *1.6x0.8mm SMD Chip LED LAMP (0.25mm Height)*, 2009, March 30.

[20] Fawwaz T. Ulaby, *Fundamentals of Applied Electromagnetics: 2004 Media Edition*, Pearson Education, Inc., 1997.

[21] Altera Corporation, *High-speed Board Layout Guidelines*, Application Note 224, Version 1.2, August 2009.

[22] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation 2nd Edition*, John Wiley & Sons Inc., 2005.

Appendix

Figure A.1 shows the overall ORISS system in which the drift tube and electrostatic mirrors can be observed. In this portion of the system, the ions begin to form a spatial separation caused by their various velocities. This variation of velocities is caused by a small difference in mass that exists between each type of isomer contained in the beam. As previously described, the BNG, along with the electronics need to drive it, are placed in front of the detection device in order to separate the ions. In the case of Figure A.1, the BNG is positioned just before the section labeled "MCP."

The previously used electronics can be seen in Figure A.2 and Figure A.3. Figure A.2 shows the entire electronics system used including the power management circuit. A magnified view of the circuit that produces the required signals can be seen in Figure A.3.

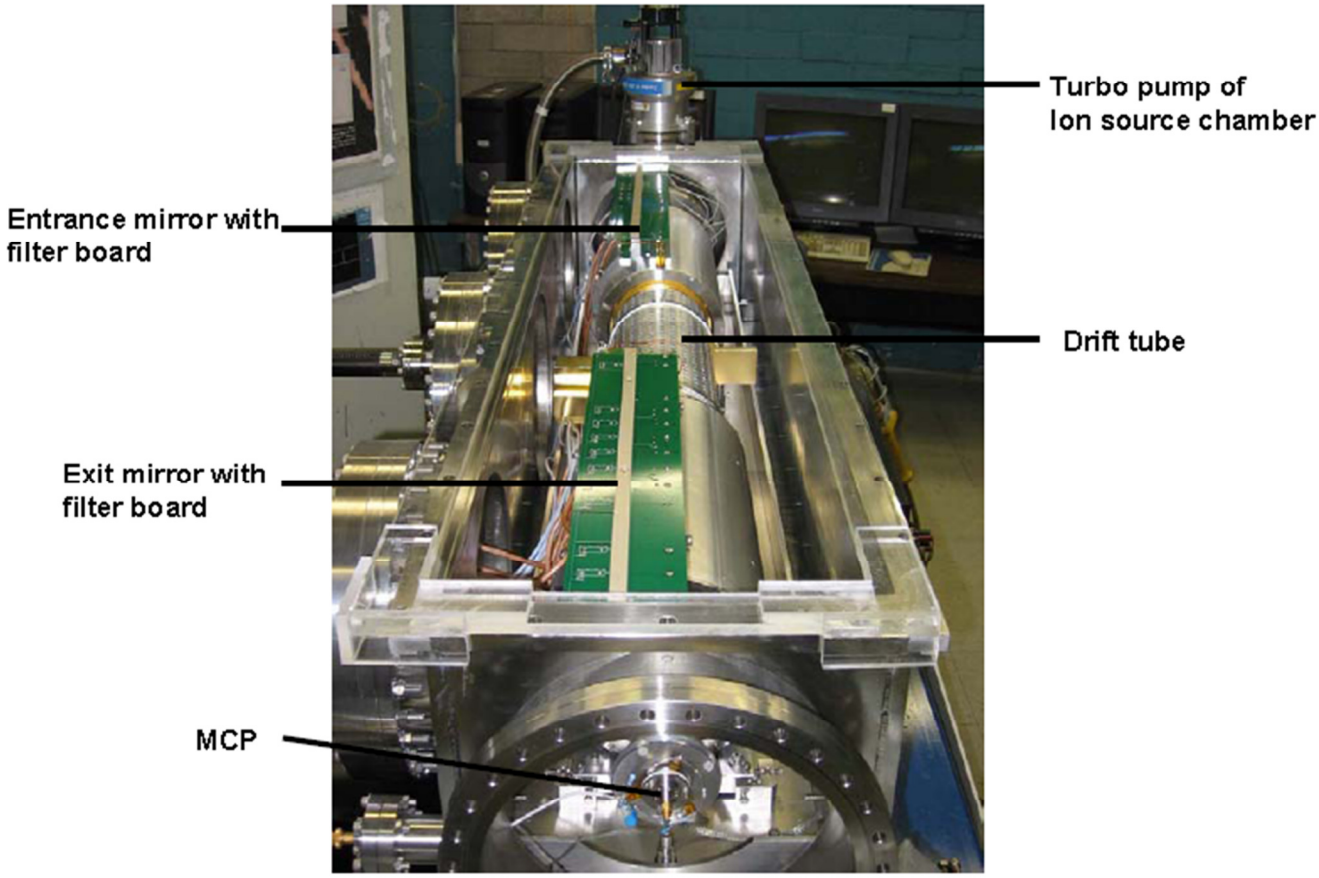

Figure A.1: ORISS MTOF System (reprinted with permission from A. Piechaczek [4])

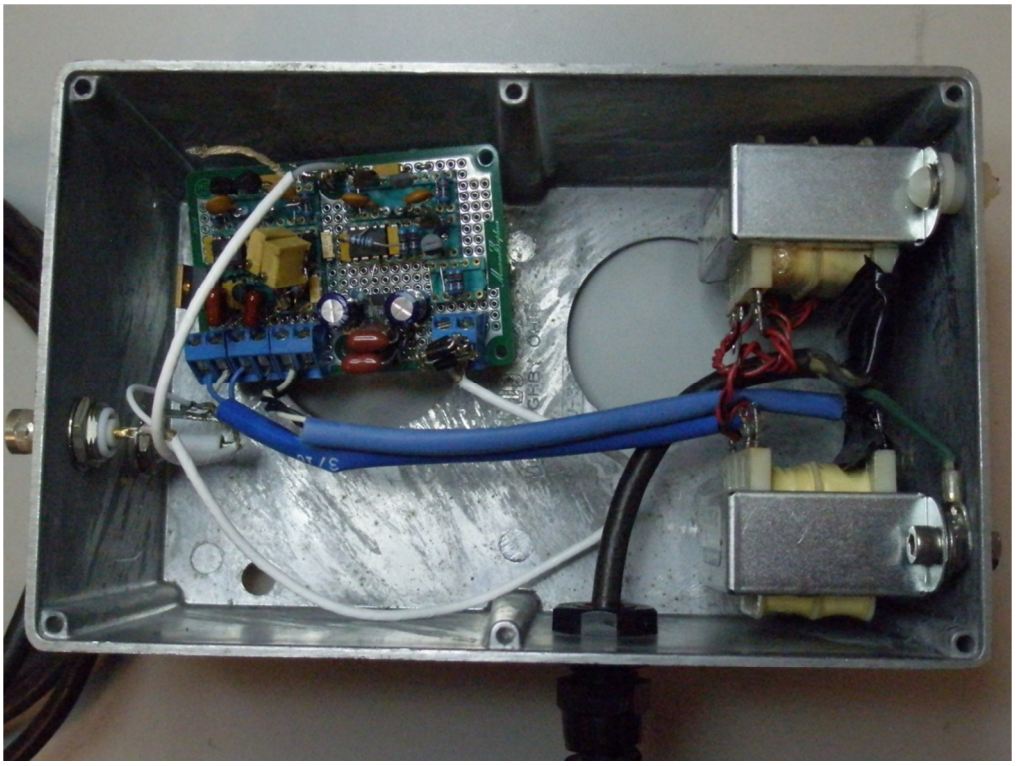

Figure A.2: Previous Electronics System Design

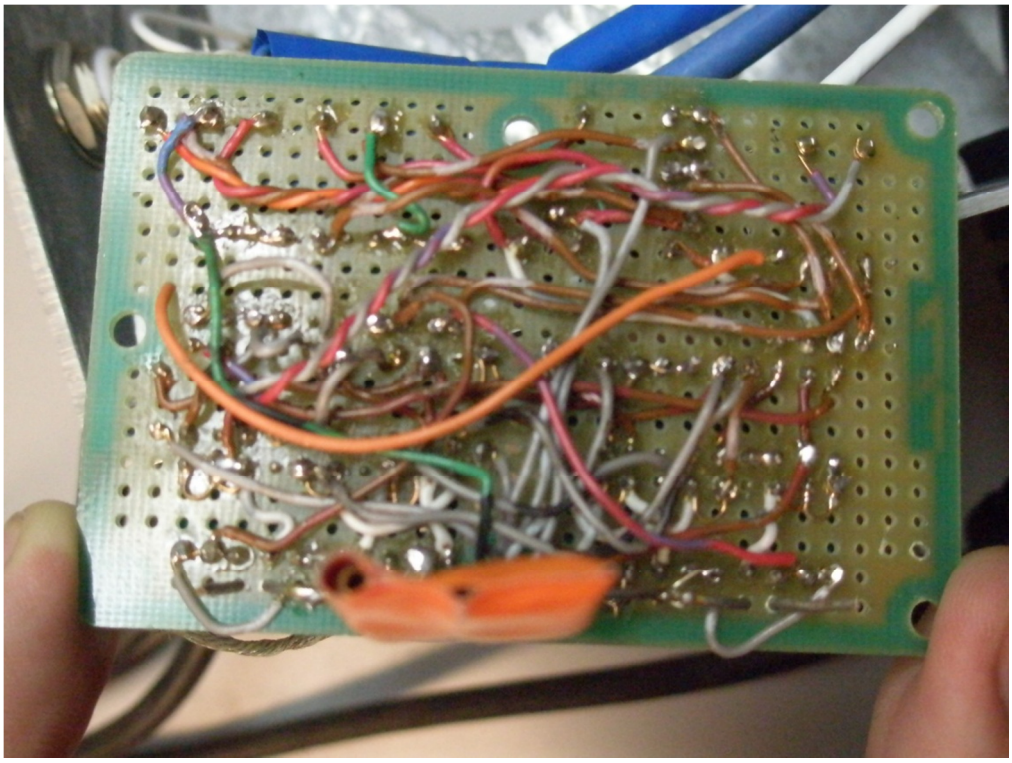

Figure A.3: Previous Electronics Board

The signal path of a single channel of the BNG driver circuit is highlighted on the board layout in Figure A.4. Each of the main components of this path is also labeled.

Pictures of the fabricated and populated board can be seen in Figure A.5, Figure A.6, and Figure A.7. Figure A.5 and Figure A.6 are photos of the top and bottom of the final board, respectively. An additional photo (Figure A.7) demonstrates the board containing the load used for testing. This load is an 18-inch twisted-pair cable with a 68 pF capacitive load attached.

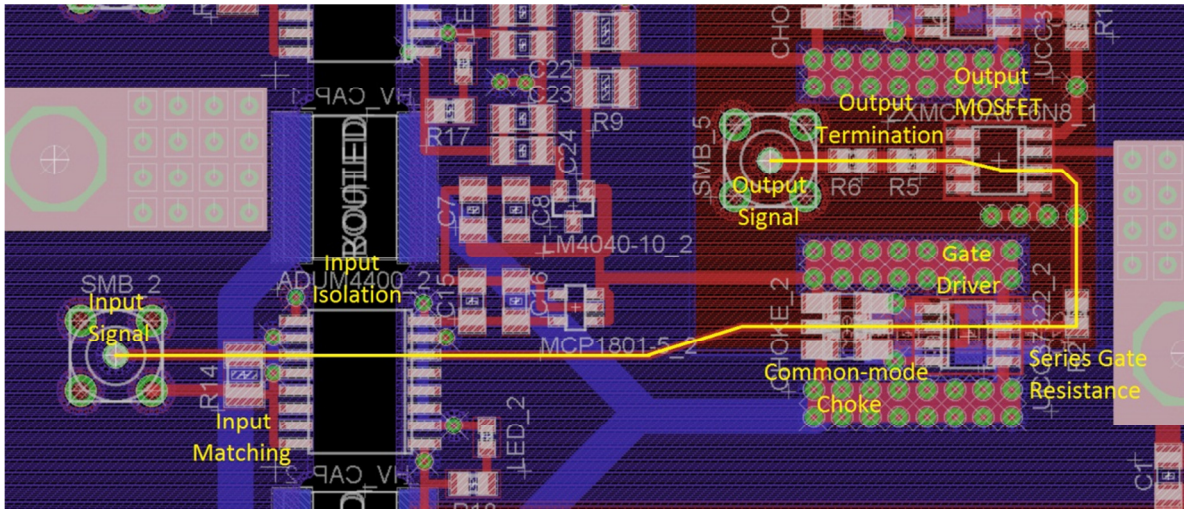

Figure A.4: Single Channel Signal Path

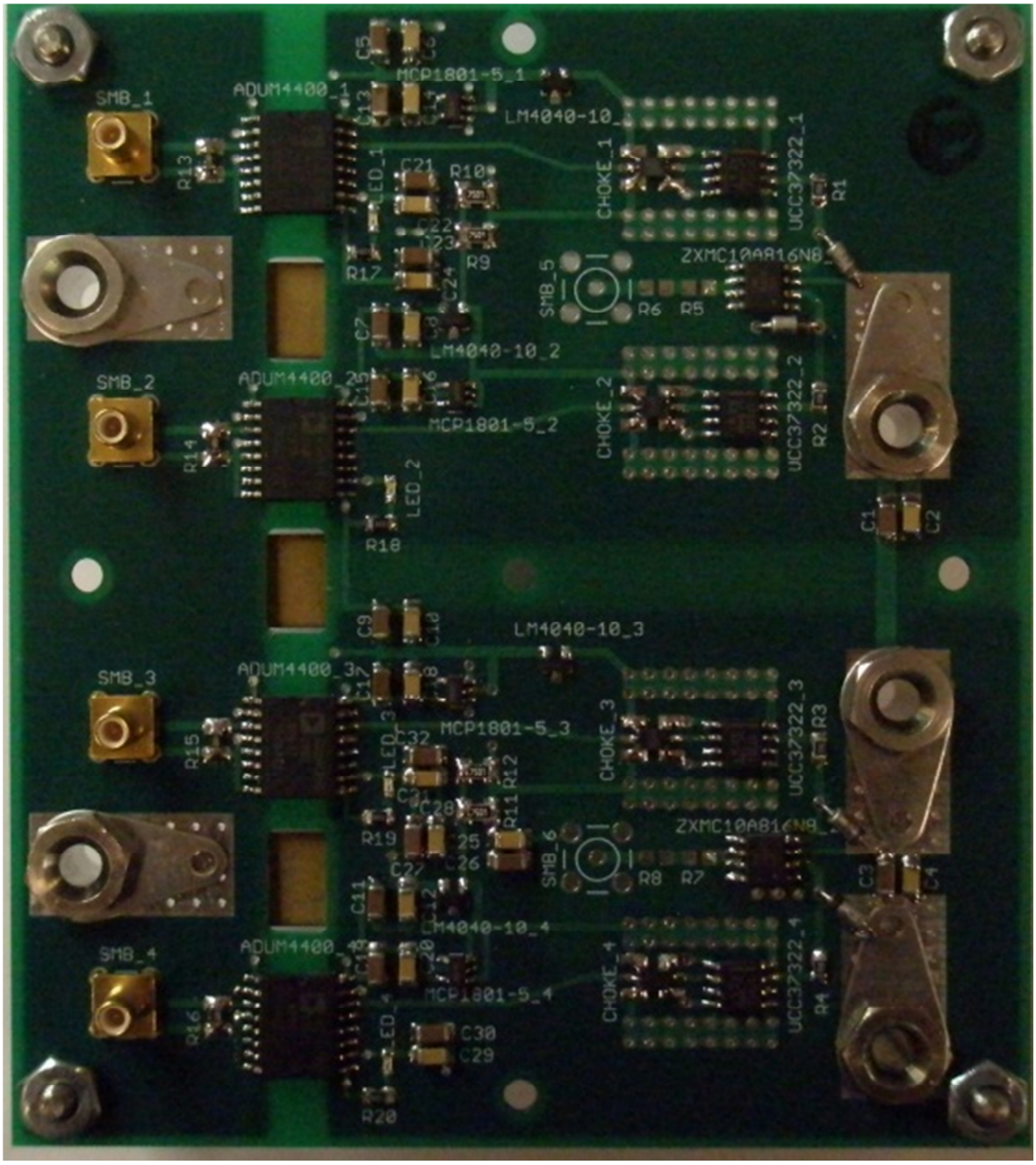

Figure A.5: BNG Driver Board (Top)

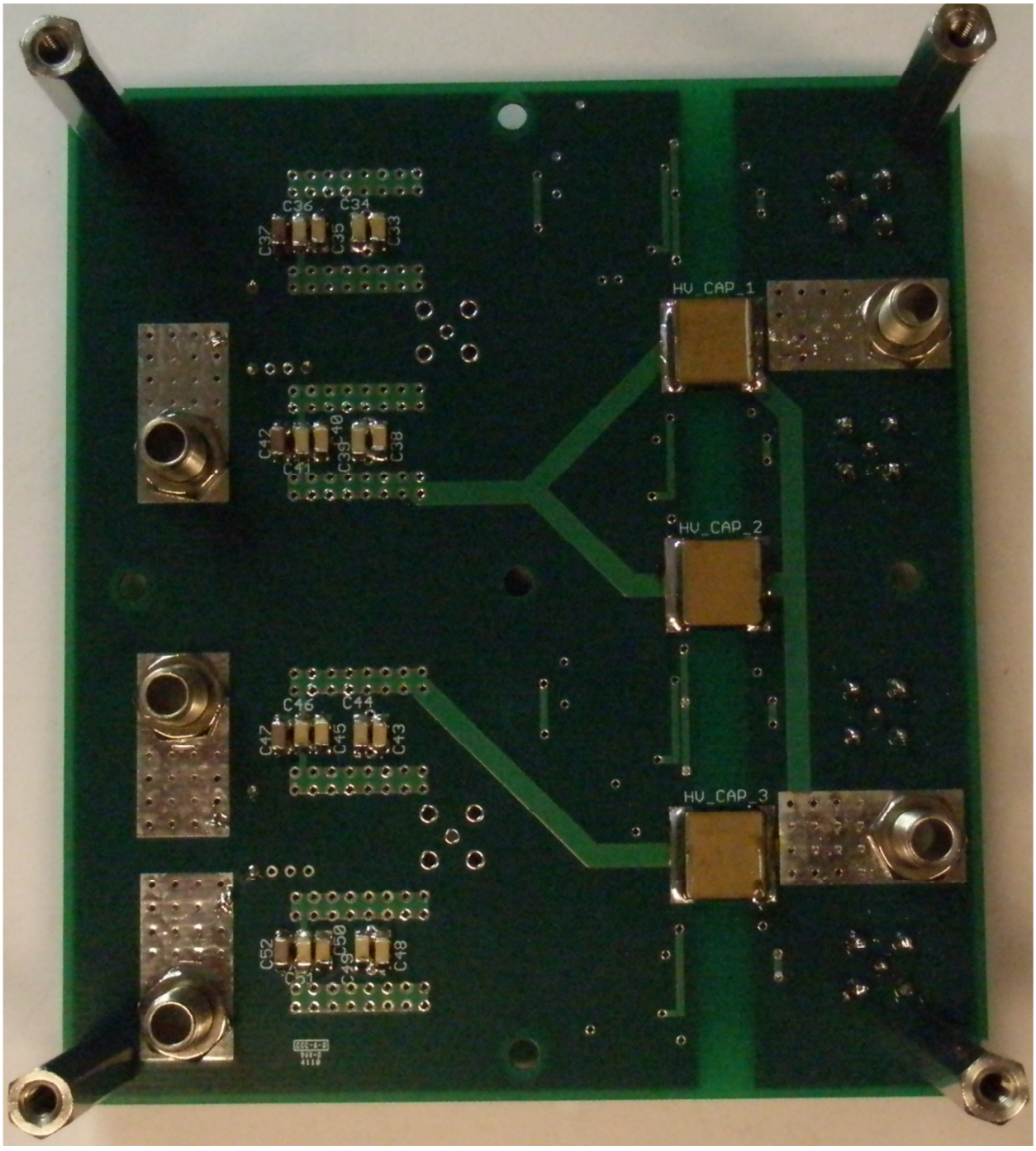

Figure A.6: BNG Driver Board (Bottom)

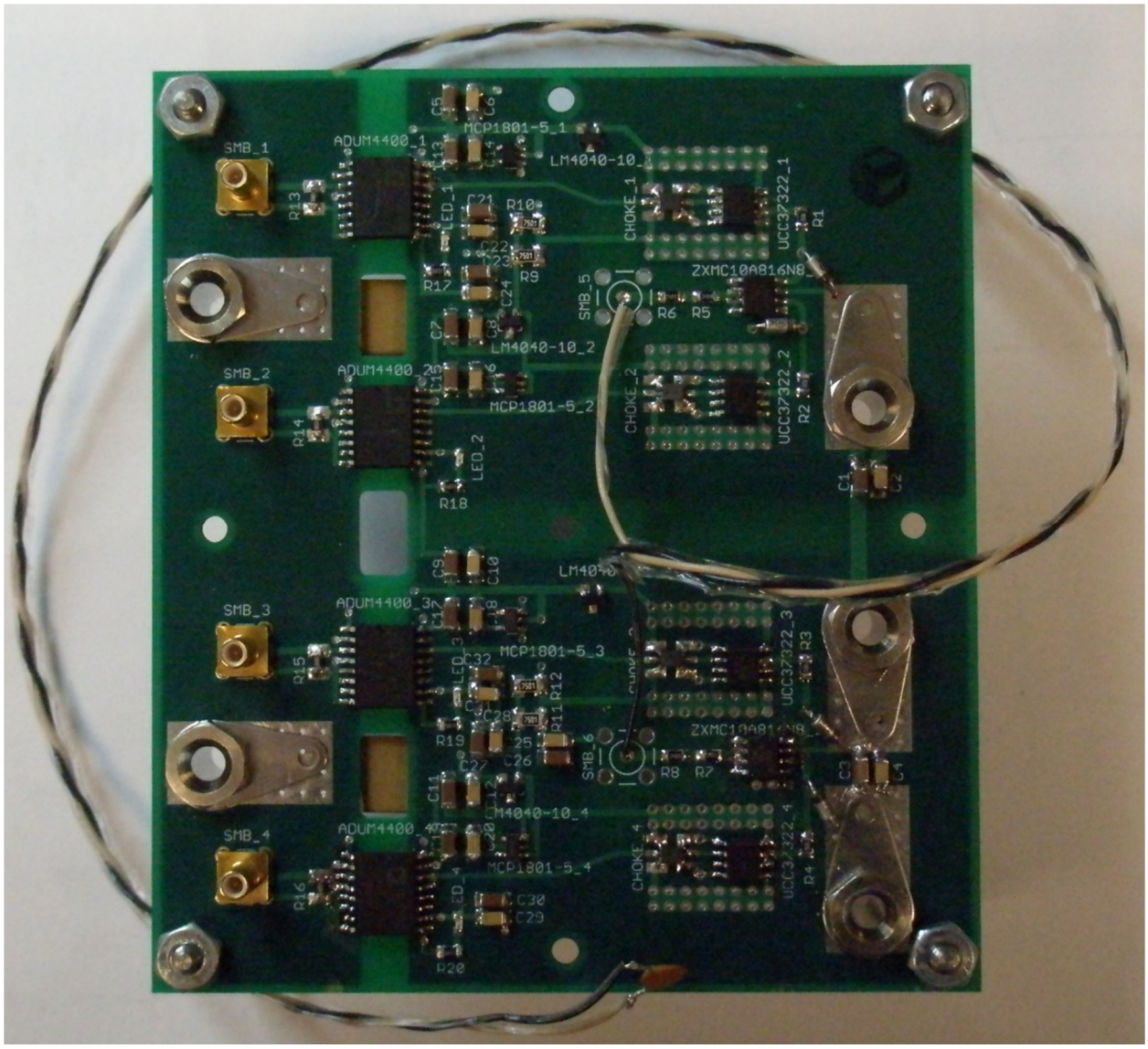

Figure A.7: BNG Driver Board with Load

The test setup used for all measurement results can be see in Figure A.8. Two 1 A power supplies are used to provide the +50 V and −50 V and are connected to the board along with the DG535 signal generator. All results are measured with a 4-channel oscilloscope that can also be observed in Figure A.8.

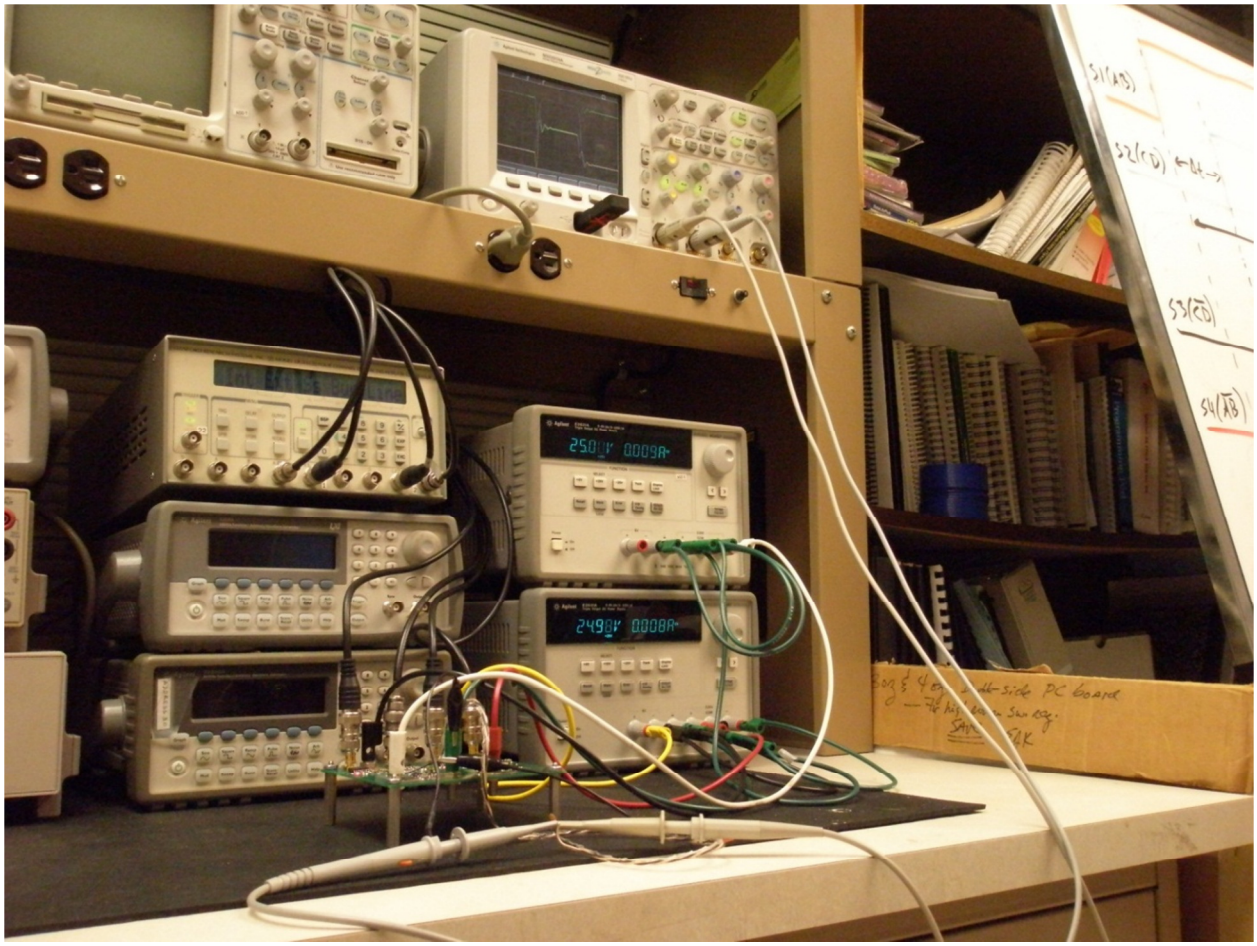

Figure A.8: Test Setup

Some measured test results for the preliminary design of the input logic is given in Figure A.9. The timing of these signals is close to that of the desired signals. However, signal integrity and more precise timing fuel the need for additional design considerations to be made for this circuit before integrating it into the BNG driver design. Future work is needed in order to obtain control signals that will be reliable with little distortion to ensure proper operation of the circuit.

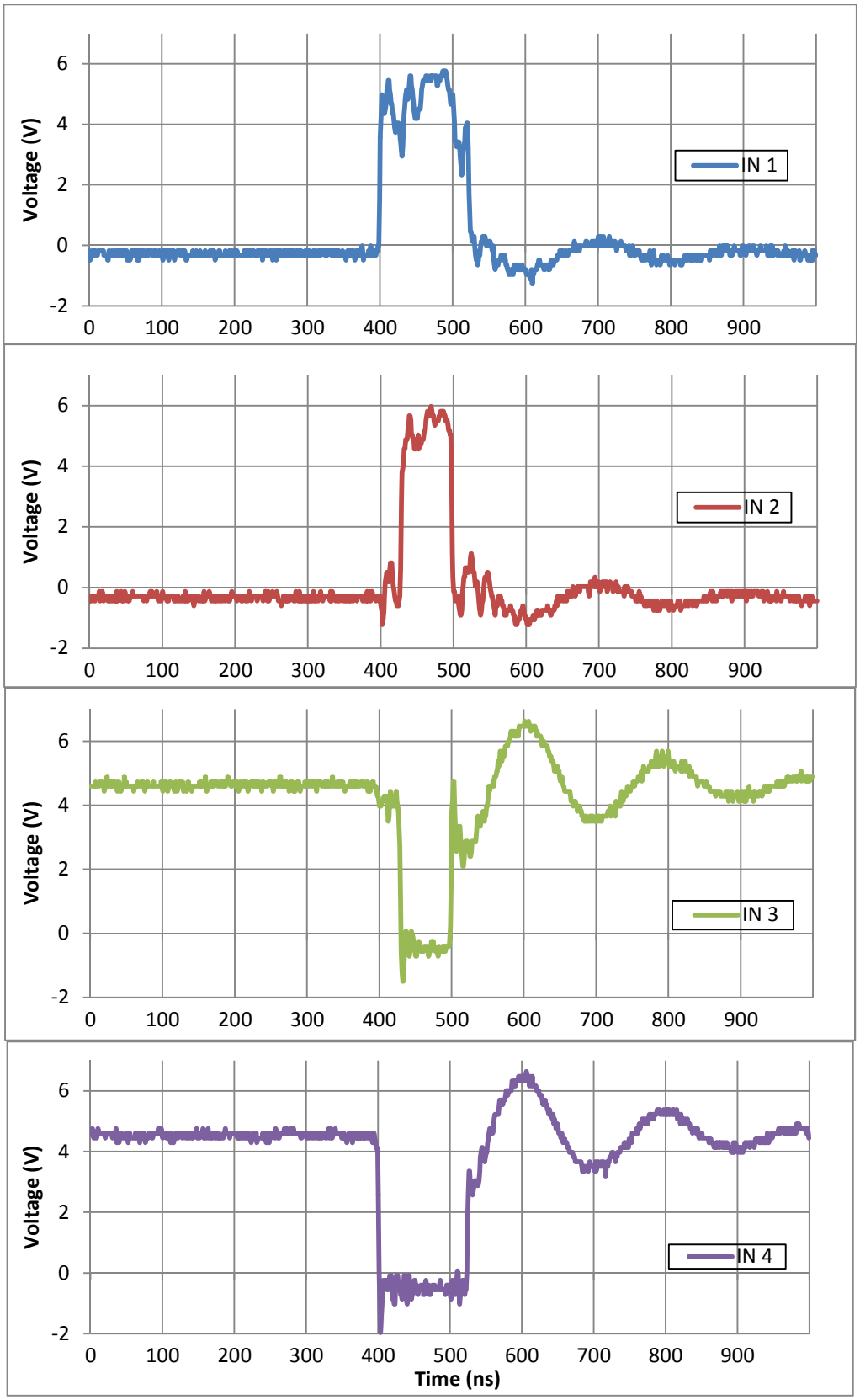

Figure A.9: Tested Input Timing Logic Output

Vita

Kevin Christopher Omoumi was born in Nashville, Tennessee on May 15th, 1986. He grew up in Cookeville, Tennessee where he avidly watched his father work as an engineer. When he graduated from White County High School in Sparta, TN in 2004 as valedictorian, Kevin had decided to become an engineer. He entered the Engineering School at the University of Tennessee in August of 2004 with a goal of obtaining a Bachelor of Science in Electrical Engineering. During this time, Kevin worked for various companies including Microsoft, National Instruments, AT&T, and Oak Ridge National Laboratory (ORNL). Just before graduation, Kevin began working in the Integrated Circuits and Systems Laboratory (ICASL) with Dr. Benjamin Blalock. Upon graduating Summa Cum Laude, he decided to further his education in the field of solid-state electronics with a Master of Science in Electrical Engineering. During his thesis work in ICASL, Kevin worked as a graduate teaching assistant (GTA) and a graduate research assistant (GRA). After completing his M.S. with Suma Cum Laude, Kevin plans to continue living in Knoxville, TN and begin work for a well-respected company.