Switching Performance Evaluation, Design, and Test of a Robust 10 kV SiC MOSFET Based Phase Leg for Modular Medium Voltage Converters

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Xingxuan Huang
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Dedicated to my parents, Rigao Huang and Xiaoqing Yang.

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Per aspera ad astra.

ABSTRACT

10 kV SiC MOSFETs are one of the most promising power semiconductor devices for next-generation high-performance modular medium voltage (MV) converters. With extraordinary device characteristics, 10 kV SiC MOSFETs also bring a variety of challenges in the design and test of MV converters. To tackle these inherent challenges, this dissertation focuses on a robust half bridge (HB) phase leg based on 10 kV SiC MOSFETs for modular MV converters. A baseline design and test of the phase leg is established first as the foundation of the research in this dissertation.

Thorough evaluation of 10 kV SiC MOSFETs' switching performance in a phase leg is necessary before applying them in MV converters. The impact of parasitic capacitances and the freewheeling diode is investigated to understand the switching performance more extensively and guide the converter design.

One non-negligible challenge is the flashover fault resulting from the premature insulation breakdown, a short circuit fault with extremely fast transients. A device model is established to thoroughly analyze the behavior of 10 kV SiC MOSFETs when the fault occurs in a phase leg. Subsequently, the gate driver and protection design considerations are summarized to achieve lower short circuit current and overvoltage and ensure the survival of the MOSFET that is in ON state when the fault happens.

Furthermore, it is challenging to design the overcurrent/short circuit protection with fast response and strong noise immunity under fast switching transients for 10 kV SiC MOSFETs. The noise immunity of the desaturation (desat) protection is studied quantitatively to provide design guidelines for noise immunity enhancement. Then, an

improved desat protection scheme with digital blanking time is developed with <350 ns response time, which is validated with short circuit tests at 6.5 kV. Based on the investigation results of the noise immunity, the strong noise immunity of the developed protection is also successfully validated. A desat protection scheme with ultrafast response is also proposed after considering the high negative *dv/dt* during the turn-on transient of 10 kV SiC MOSFETs. The ultrafast response (<160 ns response time) and the strong noise immunity are validated with short circuit tests and ac-dc continuous test at 6.5 kV.

In addition, a simple test scheme is proposed and validated experimentally, in order to qualify the HB phase leg based on the 10 kV SiC MOSFET comprehensively for the modular MV converter applications. The test scheme includes the ac-dc continuous test with two phase legs in series to create the testing condition similar to what is generated in a modular MV converter, especially the high *dv/dt*. The test scheme can fully test the capability of the phase leg to withstand high *dv/dt* and its resulting noise.

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CHAPTER 1. INTRODUCTION

This chapter provides an overview of the research presented in this dissertation, including the background, motivations, objectives, and outline of this dissertation. It should be noted that part of the content in this chapter is from the author's Master's thesis titled *Design and Switching Performance Evaluation of a 10 kV SiC MOSFET Based Phase Leg for Medium Voltage Applications* [1].

1.1 Modular Medium Voltage Converters

Nowadays, power electronics converters with high power conversion efficiency are playing an indispensable part as the essential infrastructure for our society. Particularly, medium voltage (MV, from 1 to 35 kV AC) power converters with high power rating are required to support numerous critical and fundamental applications, including MV motor drives [2] and the modern grid.

MV motor drives are indispensable driving forces in industrial, transportation, and military applications. With the same power rating, MV motor drives achieve lower losses and higher power density compared to low voltage drives [3]. Motors and their drives consume a large percentage of electricity supplied to the industry, hence MV drives with higher efficiency and better performance are promising to make a profound difference in terms of reducing the manufacturing cost and accelerating decarbonization of the industry all over the world.

MV power converters have a wide range of applications in the modern power grid. Various MV converters are needed to support grid operation, such as solid state circuit breaker and fault current limiter for protection [4], [5], active power filter (APF) for

improved power quality [6], static synchronous compensator (STATCOM), and unified power flow controller [7]. New MV converters for grid applications have also been developed to achieve more advanced functions, such as solid-state transformer [8] and continuously variable series reactor [9]. MV converters can interface renewable energy sources with the grid efficiently due to fewer stages and less complicated structure, hence drawing increasing attention as the capacity of the installed renewable energy sources keeps soaring. MV dc transmission system enabled by MV converters is promising in interfacing utility-level solar farms and offshore wind farms to the grid with lower cost and higher efficiency [1], [10]. MV power conditioning system (PCS) is essential to realize novel system configurations in distribution grids, including working as the interface of a microgrid to form an asynchronous microgrid, which benefits the microgrid on dynamic decoupling, resilience promotion, and other aspects [11]-[13]. Besides asynchronous microgrids, the MV PCS can be applied in combined heat and power system, flexible manufacturing plants to improve the system flexibility and assist renewable energy integration [14].

Among various MV converters, modular MV converters with modular topology stand out due to reduced complexity in converter design and debugging and easy extension to higher voltage level. Modular multi-level converter (MMC), cascaded H-bridge converter, and other modular topologies composed of many identical modules, have been gaining increasing popularity in MV converters [11], [15]. In MV applications with relatively high voltage and high power rating, topologies which are not modular, such as flying capacitor multi-level converter and neutral point clamped multilevel converter, are

less competitive compared to modular MV converters. With reduced complexity and inherent scalability, modular MV converters have extraordinary potential to benefit a great variety of MV applications at different voltage levels [16].

Si-based power semiconductor devices dominate in current MV converters, including IGBTs, thyristors, integrated gate-commutated thyristors (IGCTs), and gate turn-off thyristors (GTOs) [1]. The Si IGBT shown in Fig. 1-1 is prevalent in MV converters because of simple gate driver design and relatively high switching frequency. Thyristors, GTOs, and IGCTs are usually only considered for extremely high power applications, due to their low conduction loss at large current. Si MOSFETs shown in Fig.1-1, typically with lower switching loss than Si IGBTs, are not suitable in MV converters, suffering from exceptionally large conduction loss [1], [17].

However, Si IGBTs have gradually become the bottleneck in the development of high-performance MV converters [1]. The limitations of Si IGBTs for MV applications include relatively low blocking voltage, high switching loss, and low switching frequency [1]. The design and fabrication process of Si IGBTs are mature and approaching the limit of Si material. Power semiconductor devices with higher blocking voltage are highly desirable, yet the voltage rating of Si IGBTs commercially available for MV applications is limited to 6.5 kV, due to the conduction loss. Also, because of current i_2 in Fig. 1-1(a) that cannot be actively shut down and the resulting tail current, it is difficult to further reduce the switching loss of Si IGBTs [17]. Therefore, the switching frequency of MV converters based on 6.5 kV Si IGBTs is usually limited to 1 kHz. In summary, Si IGBTs

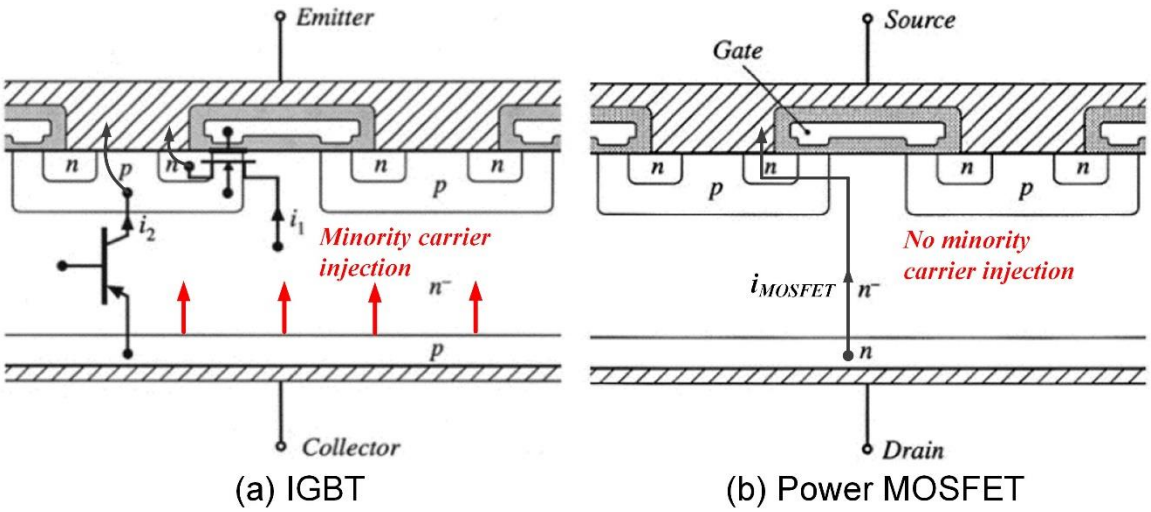


Fig. 1- 1. Physical structure and current flow of IGBT and power MOSFET [1], [17].

with limited blocking voltage and low switching frequency are not suitable for future high-performance MV converters [1].

Recently, the rapid development of silicon carbide (SiC) material for power electronics applications has laid a solid foundation for better power semiconductor devices for MV applications. As displayed in Table 1, with much wider bandgap than Si, SiC has superior material properties relevant to power electronics applications, such as electric breakdown field, saturated electron drift velocity, and thermal conductivity [1], [18], [19]. SiC has several different polymorphic crystalline structures, and only 4H-SiC is considered and discussed in this dissertation because it has the best prospect in practical power electronics applications [20].

Excellent material properties of SiC bring the SiC power semiconductor devices higher blocking voltage, higher operation temperature, and potential for higher switching frequency. Tremendous progress has been made in SiC power semiconductor devices, resulting in a wide range of high voltage (>3.3 kV) SiC power semiconductor devices designed and produced for MV applications, including junction barrier Schottky (JBS) diode, MOSFET, IGBT, thyristor, etc [1], [21]-[25]. Due to the ten times higher critical electric field of SiC material, high voltage SiC devices can achieve much higher voltage rating than their Si counterparts [23]. With rated voltage ranging from 6.5 kV to 20 kV, these emerging SiC devices leveraging the superior characteristics of SiC material provide an unprecedented opportunity to expand what can be accomplished with MV converters.

1.2 10 kV SiC MOSFETs for MV Applications

The 10 kV SiC MOSFET is one of the most promising high voltage SiC power

Table 1. Material properties of Si and SiC for power electronic applications.

Properties	**Silicon (Si)**	**Silicon Carbide (SiC)**
Bandgap	1.12 eV	3.26 eV
Electric breakdown field	0.3 MV/cm	2.0 MV/cm
Thermal conductivity	1.5 W/cm-K	4.9 W/cm-K
Electron mobility	1500 cm^2/V-s	950 cm^2/V-s (along a-axis) 1190 cm^2/V-s (along c-axis)
Saturated electron drift velocity	1.0 x 10^7 cm/s	1.0 x 10^7 cm/s
Dielectric constant	11.8	10.0

semiconductor devices to replace Si IGBTs in MV applications [1], [26]-[29]. As the leader in SiC power semiconductor devices, Wolfspeed has designed and fabricated three generations of 10 kV SiC MOSFETs, with the specific on-resistance reduced from 160 $m\Omega\text{-}cm^2$ to 100 $m\Omega\text{-}cm^2$ at room temperature [26]-[29]. Compared to Si IGBTs for MV applications, 10 kV SiC MOSFETs have higher voltage rating and operation temperature, lower switching loss, and faster switching speed, as shown in Fig. 1-2 [1]. These benefits at the device level further facilitate comprehensive benefits at the converter level, such as simpler converter topology and design, higher efficiency, smaller size and weight, and higher control bandwidth [1]. Therefore, 10 kV SiC MOSFETs are one of the prospective building blocks of the future high-performance MV converters.

10 kV SiC MOSFETs have relatively low on-resistance because of low specific on-state resistance of SiC unipolar devices [30]. To achieve the same blocking voltage level, much thinner drift layer and much higher doping density can be used if Si wafer is replaced by SiC wafer [1]. Therefore, the on-resistance of SiC majority carrier devices is tremendously reduced compared to their Si-based counterparts at the same voltage level. Fig. 1-3 shows the comparison of the specific on-resistance and its theoretical limit of SiC and Si majority carrier devices [30]. The newest generation of 10 kV SiC MOSFETs has specific on-resistance close to its theoretical limit.

Furthermore, 10 kV SiC MOSFETs have faster switching speed, >20X lower switching losses, and hence are able to switch at much higher frequency than 6.5 kV Si IGBTs with similar current rating [22], [29]. Due to the lower specific on-resistance shown in Fig. 1-3, SiC MOSFETs typically have small die size, including 10 kV SiC MOSFETs.

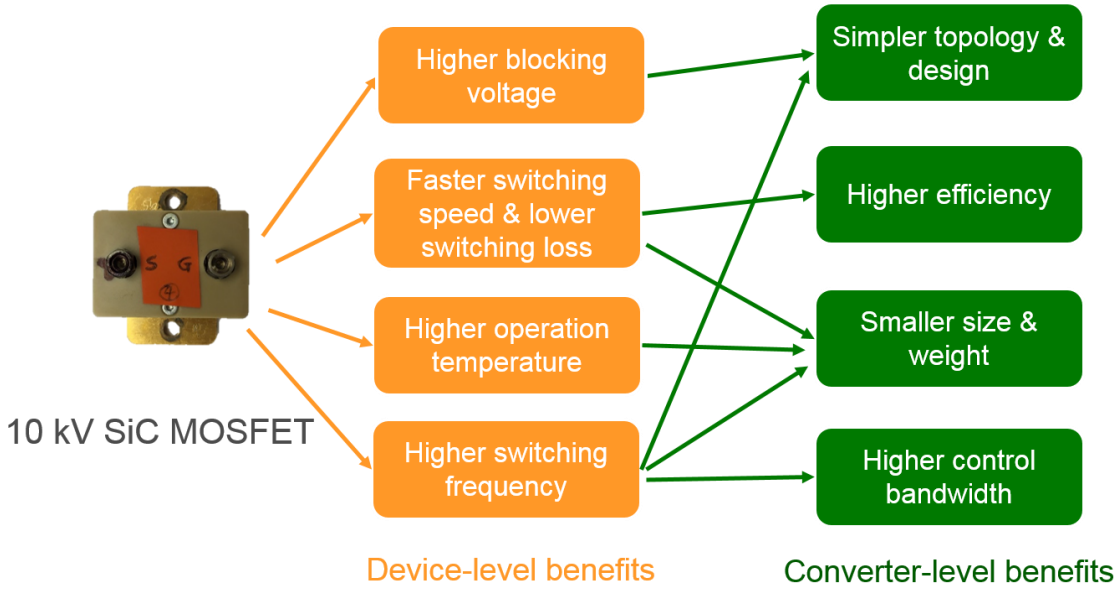


Fig. 1- 2. Device-level and converter-level benefits of 10 kV SiC MOSFETs [1].

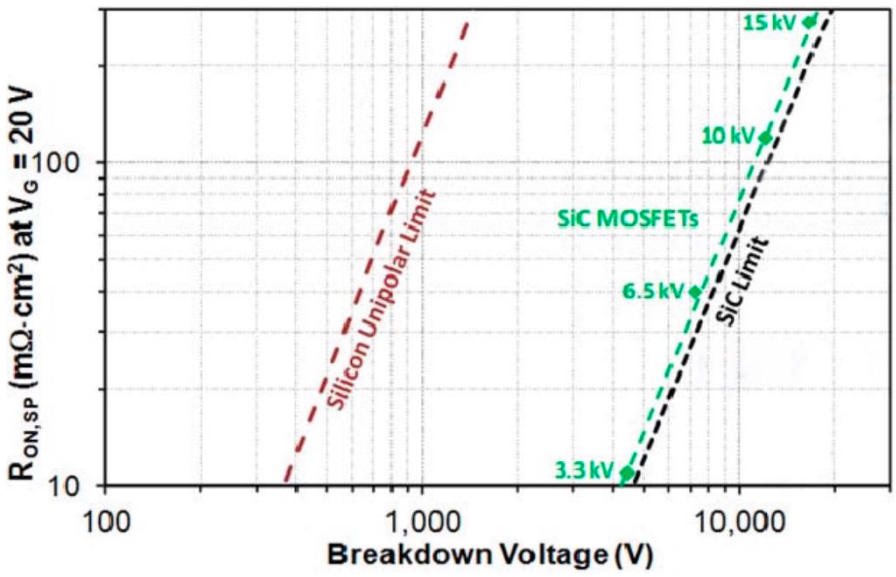


Fig. 1- 3. Specific on-resistance vs. breakdown voltage for Si and SiC [30].

As a result, the parasitic capacitances are smaller, contributing to the faster switching speed. The high saturated electron velocity of SiC material reinforces the fast switching speed of 10 kV SiC MOSFETs. From a fundamental standpoint, the 10 kV SiC MOSFET as a majority carrier device, has faster switching transients by eliminating the injection of minority charges and hence the turn-off tail current, as illustrated in Fig. 1 [17]. Because of the shorter minority carrier lifetime of SiC material [20], the body diode of 10 kV SiC MOSFETs also has much lower reverse recovery loss than Si-based PiN diodes, which also supports high switching frequency capability of 10 kV SiC MOSFETs.

MV converters benefit from the superior performance of 10 kV SiC MOSFETs in numerous aspects [27], [31]. The fast switching speed and low switching energy loss give rise to the low converter switching loss and reduced volume and weight of the cooling system. The switching frequency can be increased to tens of kilohertz to achieve smaller size of passive components and higher power density. The high blocking voltage of 10 kV SiC MOSFETs decreases the number of required power semiconductor devices and simplifies the converter topology and design [11]. With 10 kV SiC MOSFETs, two-level topologies can be adopted for MV drives with 4.16 kV line-to-line voltage.

High switching frequency enabled by 10 kV SiC MOSFETs can support the high-speed direct motor drives without the gearbox, leading to MV drives with smaller footprint and higher system density [32], [33]. Simpler multi-level topologies can be used to directly interface the distribution grid by using 10 kV SiC MOSFETs, without the series connection of switching devices. Moreover, high control bandwidth enabled by 10 kV SiC MOSFETs is capable of supporting more advanced control functions for grid-connected MV

converters. For instance, the transformerless PCS based on 10 kV SiC MOSFETs designed for 13.8 kV asynchronous microgrid can achieve APF function to filter 19th order harmonics (1140 Hz) in the distribution grid [13]. These benefits from 10 kV SiC MOSFETs are also of great significance in some emerging critical applications, such as electric vehicle (EV) fast charger and data center power supply [31], [34]-[36].

In addition to benefits, superior device-level characteristics of 10 kV SiC MOSFETs bring new challenges. For instance, the drain-to-source voltage V_{ds} of the 10 kV SiC MOSFET typically falls from 6 kV to nearly 0 V within 100 ns during the turn-on transient. Because of high blocking voltage, the high *dv/dt* lasts for much longer time than the high *dv/dt* generated by low voltage (<3.3 kV) SiC MOSFETs. It is challenging to design MV power conversion systems based on the 10 kV SiC MOSFET while fully utilizing its device-level benefits. The gate driver should isolate high voltage with high *dv/dt* in power and signal transmission. The common-mode (CM) current caused by high *dv/dt* should be tackled, and the cross-talk issue should be evaluated and addressed [24]. Not only can the high PWM voltage coupled with high *dv/dt* and switching frequency lead to accelerated insulation degradation, but also the premature insulation failure hence becomes a more serious issue which should be taken into consideration in MV converter design based on 10 kV SiC MOSFETs [37]-[39]. Moreover, the fast switching speed makes the switching transients of 10 kV SiC MOSFETs more sensitive to the parasitics in the power stage, especially parasitic capacitances. It is important to address these challenges in order to fully leverage the comprehensive benefits of 10 kV SiC MOSFETs.

1.3 Motivation and Objective

The half bridge (HB) phase leg is one of the most fundamental building blocks for modular MV converters [1]. It can function as the basic building block of MMCs and other topologies based on MMC. Two HB phase legs can form a full bridge or H-bridge, the fundamental building block of various MV converters, such as the cascaded H-bridge converter. The investigation results of the HB phase leg based on 10 kV SiC MOSFETs are the foundation for the study and design of modular MV converters. The device's switching performance in a HB phase leg is also widely accepted to guide the converter loss estimation and design. Hence, this dissertation concentrates on the study of the HB phase leg based on 10 kV SiC MOSFETs. In this dissertation, the phase leg is defined as the HB phase leg with two identical switches allowing bi-directional current. To support the bi-directional current flow, each switching device should have a freewheeling diode.

The premier motivation of this work is to design and build a robust 10 kV SiC MOSFET based HB phase leg for modular MV converters and tackle the challenges brought by the intrinsic characteristics of 10 kV SiC MOSFETs. The challenges are summarized in Fig. 1-4.

With much faster switching speed than Si IGBTs, switching transients of 10 kV SiC MOSFETs are more sensitive to the parasitics in the converter. Particularly, parasitic capacitances in the MV converter heavily influence the switching energy loss and *dv/dt* [31]. Nonetheless, the test setup used to test 10 kV SiC MOSFETs is often designed and built to minimize the parasitics in the power stage, and hence have different characteristics from MV converters. As a result, the previous study is unable to identify and investigate

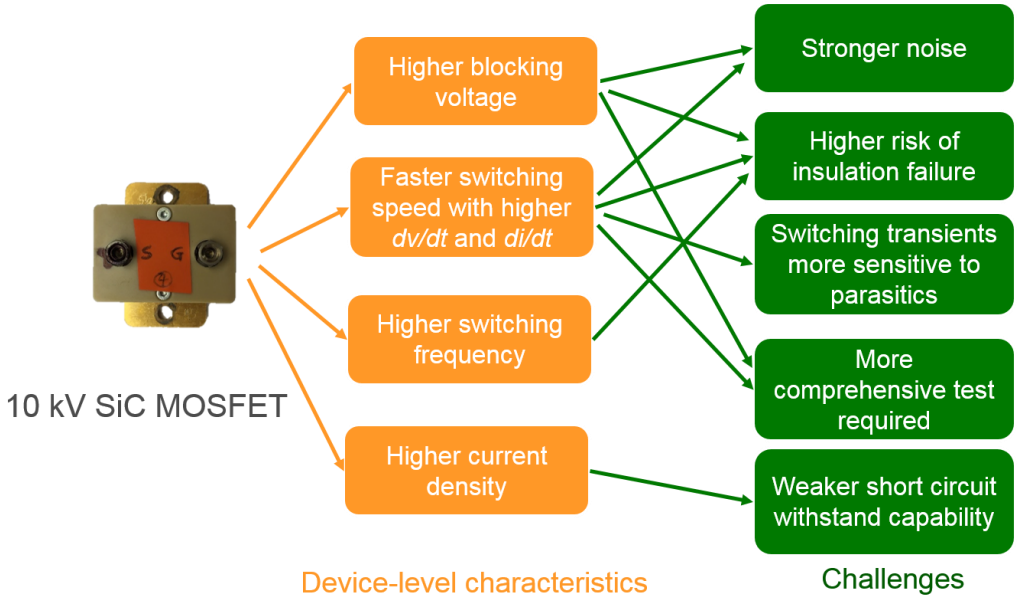


Fig. 1- 4. Summary of challenges brought by 10 kV SiC MOSFETs.

the impact of parasitic capacitances in the power stage on the switching performance, leading to inaccurate switching performance evaluation results. The freewheeling diode also impacts the switching performance of the 10 kV SiC MOSFET in the phase leg, which can be implemented with body diode and an external anti-parallel JBS diode. Adding the external anti-parallel JBS diode also introduces additional parasitic capacitance. Therefore, this dissertation aims to investigate how switching transients and performance of 10 kV SiC MOSFETs are impacted by the parasitic capacitances and the freewheeling diode.

10 kV SiC MOSFETs can generate PWM voltage with high magnitude, switching frequency, and *dv/dt*. As a result, insulation design is more difficult and challenging in the phase leg, and there is higher risk of premature insulation failure [39]. The insulation failure can generate a flashover fault, the most serious type of short circuit fault in MV converters [37]. In this dissertation, it is defined that the flashover fault happens because protective insulation fails resulting in a shorted component, such as the MOSFET package, the isolated power supply, or the voltage sensor. Thereby, this dissertation aims to take the flashover fault into account and endeavor to reduce the damage if a flashover fault happens in the phase leg design.

With small chip area and high current density, 10 kV SiC MOSFETs possess worse short-circuit ruggedness than Si IGBTs. It is hence challenging to design the protection which is required to have faster response to turn off the MOSFET safely under short circuit/overcurrent conditions. Now that the flashover fault is one type of short circuit fault that should be considered in the phase leg based on 10 kV SiC MOSFETs, the requirement for the overcurrent/short circuit protection becomes even stricter.

The high *dv/dt* and *di/dt* generated by 10 kV SiC MOSFETs also result in stronger noise which disturbs the normal operation of the phase leg. Particularly, the overcurrent/short circuit protection with fast response could be falsely triggered due to the strong noise interference. It is of profound significance to analyze the interference mechanism of the noise and address the noise immunity problem of the overcurrent/short circuit protection. Hence, one objective of this dissertation is to design the overcurrent/short circuit protection with fast response and strong immunity simultaneously after fully understanding how the noise interferes with the protection.

The comprehensive testing and qualification of the HB phase leg based on 10 kV SiC MOSFETs are necessary to ensure robust operation of the modular MV converter. It is desirable to test the phase leg comprehensively so that problems can be found at the phase leg level before assembling and testing the full converter, which is much more complex than one phase leg. The qualification of phase legs based on 10 kV SiC MOSFETs is more crucial and challenging compared to their counterparts based on Si IGBTs, considering the higher dc voltage and much higher *dv/dt* and hence much more challenging insulation and noise immunity design. Meanwhile, the qualification should not be too complicated and time-consuming. One target of this dissertation is to develop a simple and comprehensive test scheme to fully qualify the HB phase leg based on 10 kV SiC MOSFETs.

1.4 Dissertation Outline

The focus of this dissertation is a robust 10 kV SiC MOSFET based phase leg which can function as a building block of a modular MV converter. The robust phase leg should

be able to make full use of the benefits of fast-switching 10 kV SiC MOSFETS and realize normal long-term operation without any insulation and noise issue under the high *dv/dt* generated by 10 kV SiC MOSFETs. Moreover, the robust phase leg should be able to safely protect 10 kV SiC MOSFETs in the phase leg from various overcurrent and short circuit faults, including the worst type of short circuit fault, the flashover fault.

To address these challenges summarized in Fig. 1-4, the research of the phase leg in this dissertation is conducted from three perspectives: switching performance investigation, design, and testing. A detailed outline of this dissertation is as follows.

Chapter 2 reviews the previous switching performance investigation of 10 kV SiC MOSFETs. The previous study about the design and testing of the 10 kV SiC MOSFET based phase leg is also reviewed.

Chapter 3 introduces the baseline design and testing of the 6.5 kV HB phase leg based on the discrete 10 kV/20 A SiC MOSFETs.

Chapter 4 investigates the impact of parasitic capacitances in the MV converter on the switching performance of the 10 kV SiC MOSFET. How the added anti-parallel SiC JBS diode and the body diode impact switching transients and losses is also studied in depth. The switching performance with and without the anti-parallel JBS diode is compared quantitatively to demonstrate the different that the added JBS diode can make.

Chapter 5 studies the behavior of the 10 kV SiC MOSFET under a flashover fault due to insulation failure, the worst short circuit fault in MV converters with extremely fast transients. Gate driver design considerations are discussed from the standpoint of a flashover fault.

Chapter 6 focuses on the desat protection designed to protect 10 kV SiC MOSFETs from short circuit/overcurrent conditions with fast response and strong noise immunity simultaneously. Noise immunity of the desat protection for high voltage SiC MOSFETs is analyzed thoroughly to support the noise immunity improvement under high *dv/dt*. A desat protection scheme with ultrafast protection response is also proposed for 10 kV SiC MOSFETs, which can also be adopted for other high voltage SiC MOSFETs.

Chapter 7 introduces a simple test scheme to test the HB phase leg based on 10 kV SiC MOSFETs comprehensively, which in particular can fully test the phase leg's capability of operating under high *dv/dt* and the resulting noise.

Chapter 8 concludes the research presented in this dissertation, and the future work about the phase leg design and the switching performance investigation is presented in detail.

CHAPTER 2. LITERATURE REVIEW

Numerous efforts have been spent on the HB phase leg based on 10 kV SiC MOSFETs recently in order to apply the 10 kV SiC MOSFET in high-performance MV power conversion systems in the future. In this chapter, the previous research efforts with 10 kV SiC MOSFETs will be summarized, including switching performance evaluation, phase leg design, and comprehensive test and assessment. Since the literature about 10 kV SiC MOSFETs is still limited, the research about other high voltage SiC devices will also be reviewed. It should also be noted that part of the content in Chapter 2 is from the author's Master's thesis [1].

2.1 Switching Performance Evaluation

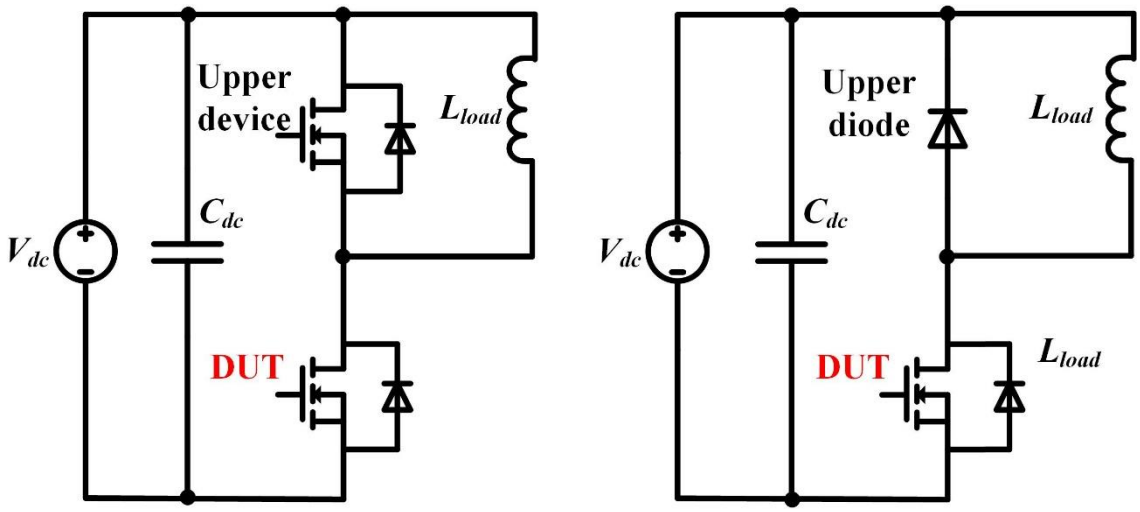
With fast switching speed, the switching performance of 10 kV SiC MOSFETs is sensitive to numerous influencing factors. Switching performance evaluation should be conducted in detail in order to understand how to control the switching transients and improve the switching performance. The switching performance essential to the MV converter design is the research focus, especially the switching energy loss and *dv/dt*. Switching loss contributes to a large portion of the total converter loss in converters based on SiC power semiconductor devices with high switching frequency, and it has profound influence on the switching frequency selection and passive component design. The noise caused by the high *dv/dt* generated by 10 kV SiC MOSFETs poses great challenge to the gate driver design with an isolated power supply, its associated control circuits and signals as well as the protection design with strong noise immunity [23], [24].

2.1.1 Characterization and Influencing Factors of Switching Performance

The most common method used to characterize the switching performance of a power semiconductor device is DPT with the clamped inductive load circuit [18], [40]. The basic operation principle of DPT is that the gate-to-source voltage V_{gs} of the device under test (DUT) has two short pulses for the characterization of both turn-on and turn-off transient in hard switching condition. Detailed working principles of DPT will not be covered in this dissertation. The essential aspects of DPT include the control signal for the DUT, the load inductor, the freewheeling path, and the measurement setup.

Two circuit configurations are usually used in DPT for the switching performance characterization, depending on the complementary switch which conducts the load current when the DUT is OFF. As shown in Fig. 2-1, the phase leg configuration is one of them, in which the upper device is always OFF. Yet the body diode of the upper device can provide the current path when the DUT is turned off. The other circuit configuration is the switch/diode pair, where a discrete diode with similar current and voltage rating to the DUT is used as the freewheeling diode. The DUT is usually the lower device because of its grounded source and the convenience in measurement. With a hotplate or oven, the junction temperature of the DUT can be regulated.

The HB phase leg can be easily reconfigured as a phase leg configuration for DPT with the purpose of switching performance evaluation. Although the data obtained in DPT with switch/diode pair are not accurate to indicate the *dv/dt* and switching loss of a phase leg applied in a converter, DPT with switch/diode pair is helpful in understanding the turn-on and turn-off transient and the influence of temperature and gate driver on the switching performance. Therefore, the switching performance evaluation with the switch/diode pair



(a) (b)

Fig. 2- 1. Two circuit configurations used in DPT: (a) phase leg configuration; (b) switch/diode pair.

will also be reviewed.

Numerous researchers have used DPT to evaluate the switching performance of high voltage SiC devices. The switching behavior and the impact of some factors have been revealed by analyzing the switching waveforms and data. In [41], the DPT setup with switch/diode pair is built to investigate the switching performance of the 15 kV SiC MOSFET under different gate resistances and junction temperatures. It is found that adopting a smaller turn-on gate resistance leads to faster turn-on transient with higher *dv/dt* and lower energy loss. The turn-on process can also be accelerated with lower turn-on loss and faster transients by increasing the junction temperature. The turn-off transient is mainly dominated by capacitive charging process and hence is less dependent on gate driver parameters and the junction temperature. The switching performance of 15 kV SiC IGBTs has also been characterized with the switch/diode pair [41], [42], with both switching energy loss and *dv/dt* analyzed in detail.

The 3rd generation 10 kV SiC MOSFET from Wolfspeed has been first characterized by Wolfspeed researchers with DPT in phase leg configuration [29], [43]. The influence of the gate resistance and the drain current on the switching performance is investigated in detail, as shown in Fig. 2-2, while the detailed analysis of the impact of the junction temperature is not provided. The large gate resistance slows down both turn-on and turn-off transient. Especially, the larger gate resistance leads to a substantial increase in the measured turn-on energy loss. Turn-on energy loss dominates the total switching energy loss. The investigation results coincide well with the conclusions in the investigation of 15 kV SiC MOSFETs with switch/diode pair in [41].

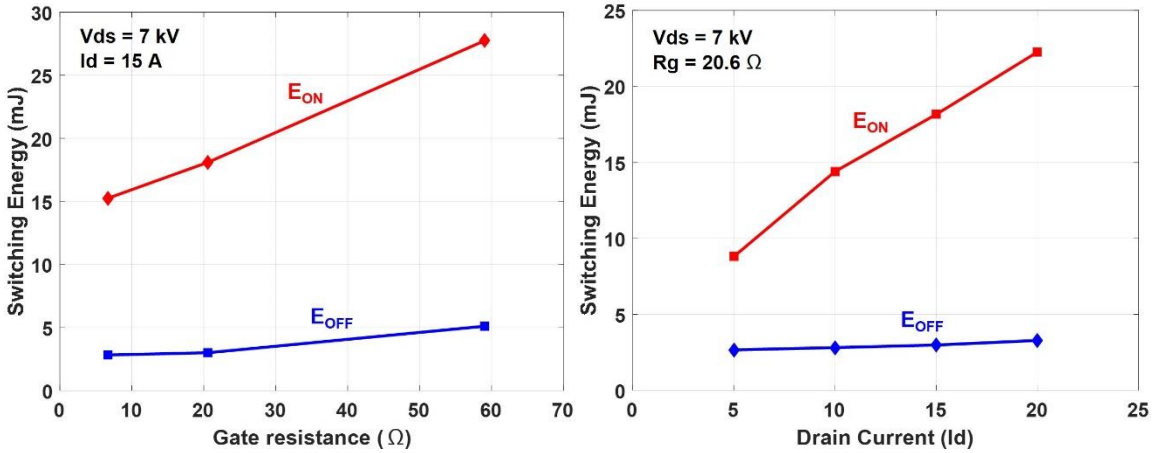


Fig. 2- 2. Switching energy loss as a function of external gate resistance (left) and drain current (right) for the 3rd generation 10 kV SiC MOSFET at 150 ˚C [29].

The temperature-dependent switching performance of the 3rd generation 10 kV SiC MOSFET is systematically studied in [44] in a HB phase leg. A detailed device model in Fig. 2-3 is built to perform the systematic study of the switching behavior and performance. Temperature has slight impact on the turn-on transient and negligible effect on the turn-off transient, as indicated in the switching waveforms in Fig. 2-4 and Fig. 2-5 ($R_{g,off}$ = 3 Ω, $R_{g,on}$ = 15 Ω). During the turn-off transient, the channel current drops to zero quickly due to low channel current (< 20 A) and high *dv/dt*. The turn-off process is thereby mainly the charging/discharging process of parasitic output capacitances of the MOSFETs, and *dv/dt* is higher at higher load current. The parasitic capacitances are independent of temperature. The junction temperature has little influence on the turn-off transient, and the measured turn-off loss is mainly the energy stored in the output capacitance of the DUT [44], [45].

Turn-on transient is slightly impacted by the temperature. The turn-on *dv/dt* is higher at higher junction temperature due to the lower gate threshold voltage. Meanwhile, the overshoot in drain current I_d increases because of the increased displacement current in the parasitic capacitances. The turn-on loss reduces slightly at higher temperature. Generally, junction temperature only slightly impacts the switching transients of the 3rd generation 10 kV SiC MOSFET, and higher junction temperature makes the turn-on transient faster. Such temperature-dependent switching behaviors of 15 kV SiC MOSFETs have also been reported [46], [47].

In summary, characterization results show that the junction temperature only has slight influence on the switching performance. The turn-on transient of 10 kV SiC MOSFETs is mainly controlled by the gate driver parameters, while the turn-off transient

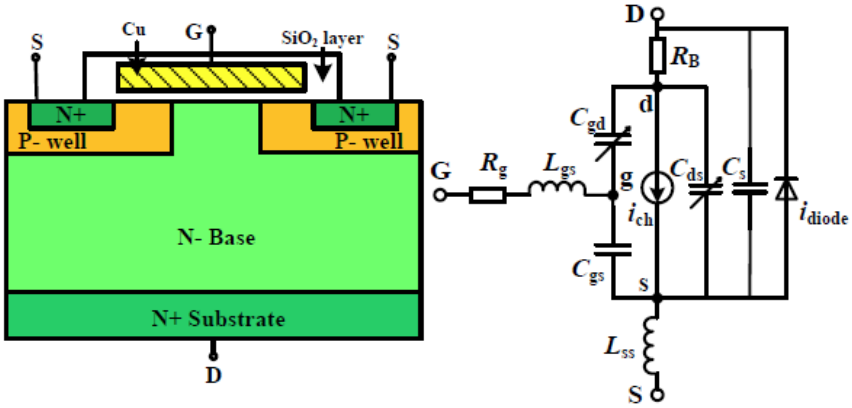


Fig. 2- 3. Detailed device model of 10 kV SiC MOSFET [44].

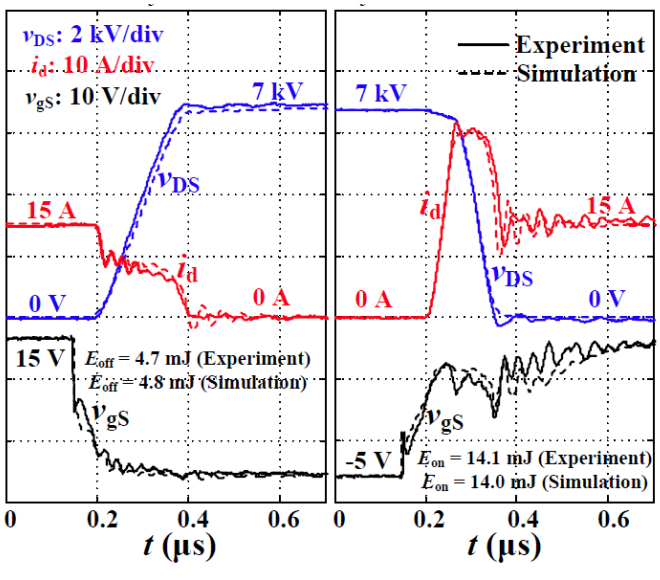


Fig. 2- 4. Turn-on and turn-off waveforms of the 10 kV SiC MOSFET at 25 ˚C [44].

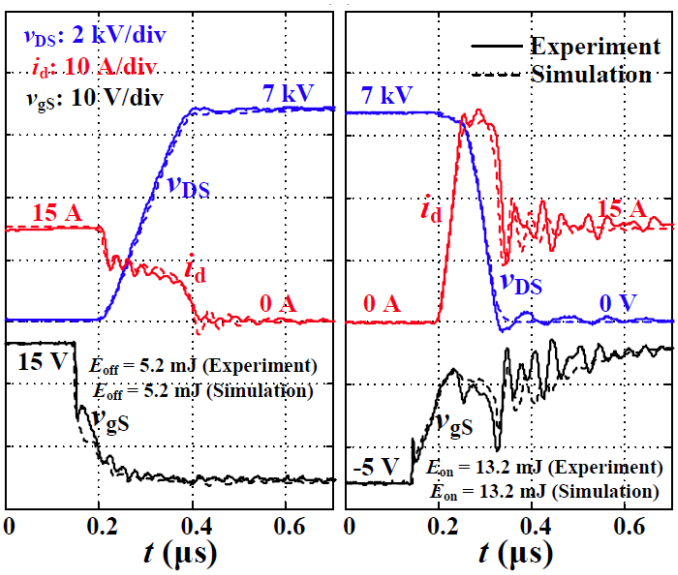


Fig. 2- 5. Turn-on and turn-off waveforms of the 10 kV SiC MOSFET at 125 ˚C [44].

is mainly determined by the parasitic capacitances and the load current since the channel current decreases to zero quickly.

Nevertheless, most previous investigation has not investigated the impact of parasitic capacitances in the MV converter on the switching performance of high voltage SiC devices. The conventional DPT setup used in previous investigation is designed to minimize the circuit parasitics and is hence different from the real converters with parasitics from numerous sources. For instance, the load inductor in conventional DPT setup typically has a single-layer winding to reduce the parasitic capacitance as much as possible, which is often not the case in MV converters [42], [44]. In fact, the fast switching speed of SiC devices makes their switching transients sensitive to the parasitic capacitances [1], [48], [49]. If the parasitic capacitance is negligible in DPT setup, the switching transients and losses obtained in DPT could deviate significantly from experimental results in real converters based on SiC devices. The switching loss in real converters could be significantly higher than what is estimated based on DPT results [50]. Therefore, it is necessary to investigate the impact of parasitic capacitances in the converter on the switching performance of 10 kV SiC MOSFETs.

2.1.2 Impact of Freewheeling Diode on Switching Performance

It is required that every switch in the phase leg should provide the freewheeling diode in voltage source converters. The freewheeling diode provides the conduction path for the load current when both switches are turned off in the HB phase leg. The freewheeling diode is also one of the influencing factors of the switching performance that should not be neglected.

In terms of SiC MOSFETs, their own body diode with small reverse recovery charge can serve as the freewheeling diode [20]. Meanwhile, an external anti-parallel SiC Schottky diode with negligible reverse recovery charge can be added to function as the freewheeling diode. Anti-parallel Schottky diode is recommended in converters based on low voltage (< 3.3 kV) SiC MOSFETs to achieve stable switching energy loss at different junction temperatures [18], [51]. This is because the body diode of the low voltage SiC MOSFET has significantly worse reverse recovery performance as junction temperature rises [51], [52]. The SiC Schottky diode should be selected to ensure that the reduction in switching loss due to improved reverse recovery performance is more substantial than the switching loss increase brought by its output capacitance [18], [51].

10 kV SiC JBS diode can be added as the anti-parallel diode to improve the loss due to reverse recovery in the phase leg based on 10 kV SiC MOSFETs. Experimental results have revealed that the anti-parallel 10 kV SiC JBS diode has nearly zero reverse recovery charge at various temperatures [53]. Currently, the body diode of 10 kV SiC MOSFET is sufficiently reliable to function as the freewheeling diode [54], [55]. Several years ago, most 10 kV SiC MOSFETs available for switching performance evaluation possess an anti-parallel JBS diode inside the package, because the MOSFET will degrade if its body diode conducts current [56]. With the anti-parallel JBS diode inside the package, the JBS diode conducts a major portion of the freewheeling current, and it is thereby difficult to study the reverse recovery performance of the body diode and the impact of the body diode or the external JBS diode on the switching transients and performance of 10 kV SiC MOSFETs over a wide temperature range.

The reverse recovery performance of a diode is also commonly characterized with a setup similar to the DPT setup for MOSFETs, as drawn in Fig. 2-6. If the body diode of a MOSFET is under test, the channel of that MOSFET is always kept off. When the upper switch *S* turns on, the diode current is forced to commutate to the upper switch, and the reverse recovery performance can be evaluated by measuring the diode current. With DPT, researchers at Wolfspeed have characterized the body diode of the 3rd generation 10 kV/20 A SiC MOSFET, revealing that the body diode has a reverse recovery charge of 1.2 μC and 1.8 μC at 25 ˚C and 150 ˚C, respectively [22]. The measured reverse recovery current, however, also includes the displacement current in parasitic capacitance C_j which is charged during the turn-on process of the upper switch. Because of the high *dv/dt* of the upper switch, the 10 kV SiC MOSFET in this case, the capacitive current accounts for a large portion of the measured reverse recovery current.

The substantial effect of the capacitive current on the reverse recovery characterization of 10 kV SiC diodes is demonstrated in [57]. After eliminating the effect of the capacitive current, the calculated reverse recovery current I_{rr} of the body diode in 10 kV/10 A SiC MOSFET is lower than 2 A at 25 ˚C and 125 ˚C. The reverse recovery charge of the body diode is not calculated. It is concluded that the body diode of the 10 kV SiC MOSFET has small reverse recovery current at different temperatures.

In summary, the freewheeling diode in the phase leg plays an essential role in the switching transients of 10 kV SiC MOSFETs, especially the turn-on transient. The reverse recovery characterization of the freewheeling diode for 10 kV SiC MOSFETs should consider the effect of the capacitive current due to the parasitic capacitance of the diode.

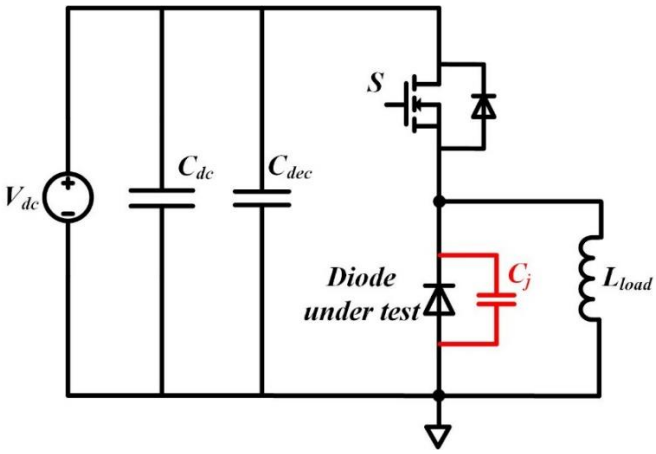


Fig. 2- 6. Circuit diagram of DPT for diode reverse recovery characterization.

The reverse recovery current of the body diode in 10 kV/10 A SiC MOSFET is lower than 2 A at 25 ˚C and 125 ˚C. The detailed impacts of the reverse recovery of the body diode on the switching performance are still unknown at different temperatures. Neither is the outcome after adding the anti-parallel JBS diode with nearly zero reverse recovery charge, which should be investigated to provide a guideline about the freewheeling diode selection.

2.2 Design of 10 kV SiC MOSFET Based Phase Leg

As illustrated in Fig. 1-4, device-level characteristics of 10 kV SiC MOSFETs bring numerous challenges in the design of the phase leg, especially in the gate driver design and overcurrent protection design. The relevant previous work about the gate driver and overcurrent protection design is reviewed in this section. The literature about the flashover fault, an emerging topic in SiC-based MV converters, is also covered in this section.

2.2.1 Gate Driver Design

The basic function of a gate driver is to drive the MOSFET with appropriate driving voltage and current and protect the MOSFET in short circuit/overcurrent conditions [1]. When a short circuit or overcurrent fault happens, the gate driver should be able to detect the fault and turn off the device safely. Particularly, the study of protection design will be reviewed in the next subsection.

Fig. 2-7 displays the basic block diagram of a gate driver for the MOSFET. The gate driver consists of signal isolator, gate drive IC, buffer circuit, and the isolated power supply grounded at the source terminal of the MOSFET. The signal isolator isolates the control circuit from the power loop. The function of gate drive IC and buffer is to drive the device with the designed voltage level and sufficient current with low switching losses and

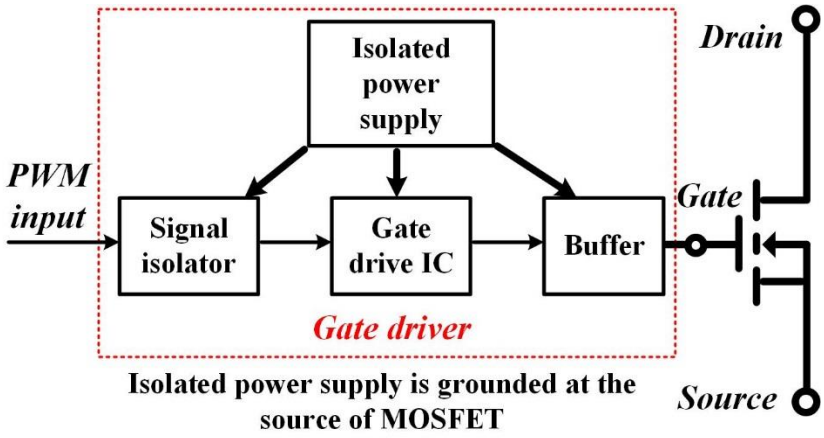


Fig. 2- 7. Basic function diagram of a gate driver for a power MOSFET [1].

acceptable switching speed. The isolated power supply is not within scope of this dissertation, and hence will not be reviewed in this chapter.

In the phase leg based on 10 kV SiC MOSFETs and other high voltage SiC devices, the signal isolator should withstand high PWM voltage coupled with high *dv/dt*. The main challenge is to have high isolation voltage and high common mode transient immunity (CMTI) (>100 V/ns) simultaneously [1]. The signal isolator for high voltage SiC devices is dominated by the solution with fiber optic transmitter and receiver. The isolation voltage and CMTI of this solution can be extremely high if the power supplies in each side offer sufficient isolation [1]. With fiber optic cable, the clearance and creepage requirements are easily satisfied.

The gate drive IC and buffer operate together with gate resistors and other auxiliary circuitry to drive the MOSFET and control the switching speed. The buffer is optional and only adopted to boost the driving current. The gate drive voltage and gate resistors are selected based on the static characteristics, switching performance, and short circuit performance. The off-state gate voltage $V_{g,off}$ for 10 kV SiC MOSFETs usually ranges from -6 V and -1 V to ensure reliable turn-off. For 10 kV SiC MOSFETs, gate drive voltage in on state $V_{g,on}$ ranges from 15 V to 20 V. The on-resistance of the 10 kV SiC MOSFET only has slight difference as $V_{g,on}$ increases from 15 V to 20 V [44], yet higher $V_{g,on}$ leads to significantly higher short circuit current and energy loss, and hence stricter requirement on the response time of the protection [58], [59].

After $V_{g,on}$ and $V_{g,off}$ are selected, gate resistances are tuned to achieve the desired switching transients and losses. Different gate resistances can be designed for turn-on and

turn-off transients. In the case of 10 kV SiC MOSFETs, gate resistances are selected based on the trade-off between switching loss and switching speed, especially during the turn-on transient. Then, the required peak driving current can be calculated as follows.

$$I_{source} = \frac{V_{g,on} - V_{g,off}}{R_{g,on}} \tag{2.1}$$

$$I_{sink} = \frac{V_{g,on} - V_{g,off}}{R_{g,off}} \tag{2.2}$$

The selection of gate drive IC should particularly consider the peak driving current, rise/fall time, and propagation delay. The peak source/sink drive current of the gate drive IC should be higher than the required current, otherwise a buffer is needed. The buffer can be a IC with high driving current or BJT-based current boosters in parallel [60], [61]. Short rise/fall time and propagation delay time are required to fully utilize the fast switching speed of the 10 kV SiC MOSFETs.

The cross-talk issue should also be evaluated and tackled in the gate driver design for high voltage SiC devices. In a half bridge phase leg, if *dv/dt* is too high during the turn-on transient, the spurious gate voltage in the other switching device could be higher than the gate threshold voltage due to the Miller current, resulting in partial shoot-through and higher losses [62]. The cross-talk issue will set the upper limit for the turn-on *dv/dt* of SiC MOSFETs, if it is not addressed. The partial shoot-through has been reported in the phase leg based on high voltage SiC MOSFETs when the turn-on gate resistance is low [46].

Active Miller clamping is a common method to suppress the cross-talk without sacrificing the switching speed significantly [63]-[65]. The gate driver for 10 kV/10 A SiC MOSFET in [63] adopts an active Miller clamping design. When high *dv/dt* occurs during the turn-on transient of one MOSFET, the gate driver for the other MOSFET in off state

provides a low impedance path for the Miller current and clamps V_{gs} to ensure reliable turn-off. The clamping circuit is only activated when the device is turned off.

Analytical analysis of cross-talk in low voltage SiC MOSFETs is also effective in the evaluation of cross-talk of high voltage SiC devices. In fact, previous analysis shows that cross-talk is not serious in some high voltage SiC devices. After evaluating the cross-talk of 3rd generation 10 kV/20 A SiC MOSFET from Wolfspeed, it is concluded that specific anti-cross-talk design is not necessary in the gate driver [44]. The excellent performance in cross-talk is attributed to the much larger input capacitance of the 10 kV/20 A SiC MOSFET, compared to its Miller capacitance. The calculated maximum increase in V_{gs} is 5.0 V in the worst case when all Miller capacitive current charges the input capacitance of the MOSFET. Therefore, partial shoot-through does not occur when $V_{g,off}$ is below -4 V. DPT results of 10 kV SiC MOSFETs show that cross-talk has little impact on the turn-on transient and loss (15 Ω turn-on gate resistance). Yet the spurious gate voltage is not measured to provide the direct evidence.

In summary, the previous gate driver design for high voltage SiC devices usually focuses on realizing fast switching speed and reliable isolation. Signal isolation is typically achieved by fiber optics. The selection of components emphasizes the driving capability and low delay. Cross-talk in the 3rd generation 10 kV SiC MOSFET is significantly alleviated by its large input capacitance, yet it is an issue for some high voltage SiC devices [65]. With emphasis on the fast switching speed, most gate driver design for high voltage SiC devices in the literature has not focused continuous operation. The feedback signal sent back to the controller only reports the overcurrent fault. Considering the higher cost

of high voltage SiC devices, more efforts can be spent on the continuous operation of the gate driver and the device. Also, the impact of a flashover fault on gate driver design has not been fully discussed in MV converters based on high voltage SiC devices, which will be reviewed in Subsection 2.2.3.

2.2.2 Overcurrent Protection Design

The overcurrent/short circuit protection function in the gate driver plays a more crucial part in MV converters, in which power semiconductor devices are more costly. The overcurrent/short circuit protection scheme should have fast response, good noise immunity, and simple implementation for both discrete devices and power modules [1]. Featuring smaller die, lower thermal capacitance, and higher current density, SiC devices have shorter short circuit withstand time than Si IGBTs and MOSFETs. Fast response to clear the fault is thereby desired, which often contradicts the strong noise immunity. The noise resulting from fast switching transients of SiC devices makes it more challenging to achieve fast response with satisfactory noise immunity. Short response time is also desirable as it benefits the long-term reliability of SiC MOSFETs. In this subsection, overcurrent protection schemes for SiC MOSFETs are reviewed.

Desaturation (Desat) protection scheme dominating the overcurrent protection of Si IGBTs has been successfully implemented in a variety of SiC MOSFETs, including 10 kV SiC MOSFETs [60], [66], [67]. Desat protection monitors V_{ds} of the MOSFET, and the protection is triggered once the monitored V_{ds} exceeds the threshold. The desat diode with the same voltage rating as the MOSFET is necessary to isolate the high voltage in the

drain terminal. The design shown in Fig. 2-8 for 1.2 kV SiC MOSFET has achieved a response time of 210 ns [66].

Desat protection possesses numerous salient advantages, which give rise to its popularity in the gate drivers for Si IGBTs and SiC MOSFETs. Desat protection is effective in detecting all kinds of overcurrent and short circuit faults, although it does not directly measure the device current. Desat protection features simple implementation for both discrete devices and modules, and usually only off-the-shelf components are required. Some gate driver ICs with desat protection function make it even simpler to implement the protection. Satisfactory noise immunity can be achieved, although it is often realized at the cost of increasing response time.

In desat protection, the blanking time is required to disable the protection during the turn-on transient until V_{ds} reaches steady state. Usually the response speed of desat protection is limited by the blanking time. In the design practices, the response time is also often sacrificed to enhance noise immunity. In terms of the desat protection for 10 kV SiC MOSFETs and other high voltage SiC MOSFETs, some methods are introduced to avoid false triggering during the turn-on and turn-off transient, yet the relationship between noise immunity and response time has never been thoroughly investigated. It is still unknown how fast the desat protection can be with noise immunity not sacrificed.

The threshold current of desat protection is determined by the device's output characteristic and the threshold voltage. With the same drain current, SiC MOSFETs have significantly higher V_{ds} at higher junction temperature. Thus, desat protection for SiC MOSFETs has different threshold currents as junction temperature varies. The threshold

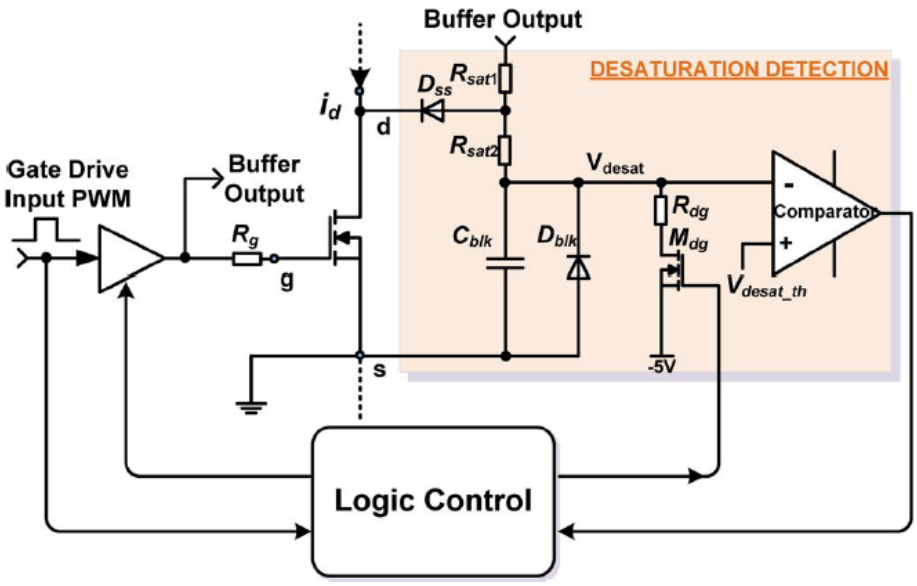


Fig. 2- 8. Implementation of desat protection for SiC MOSFETs [66].

current is higher at lower junction temperature. Also, since the drain current of SiC MOSFETs does not have hard saturation, the current rise during the response time should be taken into account when determining the threshold current.

Other overcurrent protection schemes for SiC MOSFETs have been proposed by evaluating the current in a way independent of the I-V characteristic of the MOSFET to obtain a constant threshold current. The stray inductance in series with the source terminal of the SiC MOSFET can be used as a sensor to derive the current and serve for the protection, with the carried *di/dt* information [66], [67]. It is difficult to implement this method for SiC MOSFETs with different packages and ensure high noise immunity. A sufficient, but not too large, parasitic inductance with readily connectible terminals is indispensable to implement this method. Then debugging and testing are necessary to measure the stray inductance for the threshold selection and check the noise immunity. Protection schemes based on the current sensor are also investigated. It is concluded that Rogowski coil has excellent overall performance in terms of accuracy, bandwidth and linearity among numerous current sensing methods, such as shunt resistor, Hall sensor, and current transducer [68]-[70].

High-bandwidth Rogowski coil sensor with an active integrator has been demonstrated in the protection of SiC discrete devices and modules [69], [71]-[76]. PCB-based Rogowski coil stands out due to low profile, integration capability, and repeatability. The protection scheme based on Rogowski coil detects the fault within 100 ns, regardless of the short circuit type and the junction temperature. The total response time is short and constant in different conditions, so the threshold current can be easily selected.

Nonetheless, the active integrator has to be reset periodically when the device is off to overcome the difficulty of Rogowski coil in measuring DC current, otherwise the sensor error keeps increasing [73], [74]. To ensure the accuracy of the sensor and the protection, the device should be turned off periodically with the off-state longer than a minimum length. It is generally complicated and expensive to implement this method in order to achieve good accuracy and noise immunity [71]-[76].

The protection scheme based on the air-gapped current transformer has been adopted to protect discrete 10 kV SiC MOSFETs [37]. By measuring the device current directly with a current transformer in the source path of the MOSFET, the protection scheme with ultrafast response can clear the short circuit fault within 150 ns. However, when using this scheme to protect a 10 kV SiC MOSFET module with a half-bridge configuration or other configurations, the current of the top device can only be measured at its drain terminal, leading to the high isolation voltage between primary winding and secondary winding of the current transformer for the top device. Higher cost and more complicated implementation are hence necessary to achieve reliable insulation between the primary side and the secondary side. The clearance and creepage requirements also increase the size of the current transformer. It is hence difficult to implement this protection scheme based on current transformer in 10 kV SiC MOSFET modules. It is a competitive solution for the discrete SiC MOSFETs, but not suitable for SiC MOSFET modules.

In addition, the protection method based on the measured gate charge and V_{gs} during the turn-on transient has been reported [77]. The response speed is fairly acceptable, but it

is only demonstrated that it can clear one kind of short circuit fault. Its response to other kinds of short circuit and overcurrent cases is still uncertain.

In summary, desat protection and the protection based on Rogowski coil sensor are the two methods suitable for protecting both the SiC discrete devices and modules with excellent overall performance. With fast response, the method based on Rogowski coil sensor requires complicated and high-cost implementation to realize sufficient sensor accuracy and noise immunity when protecting SiC MOSFETs with fast transients and both conducted and radiated EMI noise. Desat protection is hence more competitive thanks to its simple implementation and adoption of off-the-shelf components. Yet the relatively long response time of desat protection due to blanking time and noise immunity consideration may prevent its usage in some cases. The trade-off between response time and noise immunity of desat protection should be examined carefully to maintain strong noise immunity while speeding up the response.

2.2.3 Impact of Flashover Fault on Gate Driver Design

In MV converters based on 10 kV SiC MOSFETs and other high voltage SiC devices, the flashover fault due to insulation breakdown becomes a much more serious issue compared to traditional MV converters utilizing Si IGBTs, due to high PWM voltage coupled with high switching frequency (>5 kHz) and *dv/dt* (>20 V/ns) [37]-[39]. The insulation design of MV converters based on 10 kV SiC MOSFETs is faced with unprecedented challenges, and there is a higher risk of premature breakdown in the insulation of some essential components of the MV converter, which subsequently generates a flashover fault with extremely fast transients.

In the last decade, increasing research efforts have been spent in investigating the relationship between the PWM voltage with semi-square shape and the accelerated degradation of the insulation material. The insulation materials widely adopted in the power electronics applications are selected as the test samples for the research, including Polyethylenterephtalat (PET) insulation foil [39], Polyimide (PI) films [78], ethylene propylene rubber (EPR) [38], and other materials. It is concluded that if partial discharge (PD) is initiated inside the insulation material, the total PD charge and its detrimental impact on the insulation material increases as the magnitude, *dv/dt*, and switching frequency of the applied PWM voltage become higher, leading to accelerated insulation failure and shorter lifetime [39], [79].

In fact, it is difficult to accurately determine the real partial discharge inception voltage (PDIV) of the insulation material exposed to the PWM-type voltage, since a typical PD tester can only output 50/60 Hz sinusoidal voltage, resulting in higher measured PDIV. In practical applications, the real PDIV of the insulation material inside MV converters can be further reduced in harsh operating conditions, which makes it even tougher to achieve PD-free insulation design [78]. Moreover, high *dv/dt* and switching frequency exacerbate the overvoltage and dielectric loss inside the insulation material, both of which can also cause premature insulation breakdown [39], [80]. Therefore, premature insulation failure and the resulting flashover fault are one of the crucial challenges that should be tackled when designing MV converters based on 10 kV SiC MOSFETs.

The issue brought by premature insulation breakdown and the flashover fault can be addressed from two perspectives. This issue can be tackled by enhancing the insulation

design to minimize the risk of premature insulation breakdown. The research in this field is out of the scope of this dissertation. The other perspective involves the gate driver and protection design to achieve better performance of the 10 kV SiC MOSFET and reduce the damage caused by a flashover fault. The flashover fault with extremely high dv_{ds}/dt (> 1 kV/ns) and di/dt (>30 A/ns) particularly poses a great threat to the 10 kV SiC MOSFET already in ON state, which should be protected from damage, unless the insulation inside its own package fails [37].

So far the flashover fault has received little attention in the design of a MV phase leg or converter based on high voltage SiC devices. The flashover fault in a HB phase leg based on 10 kV SiC MOSFETs is analyzed partially in [37]. It is demonstrated that the short circuit protection successfully protects the MOSFET that is in ON state when the flashover fault happens. However, the behavior of the 10 kV SiC MOSFET with Kelvin source is not analyzed thoroughly, and the gate driver and protection design considerations are not comprehensively studied and summarized after considering the flashover fault. Therefore, comprehensive study about the behavior and gate driver design considerations of 10 kV SiC MOSFETs under a flashover fault is of great significance, but still absent in the literature.

2.3 Testing of 10 kV SiC MOSFET Based Phase Leg

The phase leg should be fully tested to validate its capability to operate continuously at rated voltage and power and function as a robust module of a modular MV converter. The thermal performance, insulation design, and the capability to withstand high dv/dt and its resulting noise of the phase leg should be thoroughly tested and qualified.

Testing and debugging the phase leg is much less challenging than testing the whole modular MV converter. Thus, the phase leg testing should be carefully designed so that all issues of the phase leg can be pinpointed and solved before assembling and testing a modular MV converter, which will make the converter testing more efficient. Continuous test of the phase leg is hence indispensable, which should create conditions similar to the real condition in a modular MV converter. The testing should be designed and implemented to make sure that all components in the phase leg are fully validated at the rated condition, including insulation voltage, CM voltage, *dv/dt*, device current, etc. Particularly high *dv/dt* and the resulting high CM current could generate strong noise and lead to the malfunction of the gate driver and the phase leg. Achieving the *dv/dt* that will occur in the modular MV converter should be one of the focuses when devising the continuous test.

How to test the HB phase leg or the converter based on high voltage SiC devices comprehensively has not received much discussion in previous literature. DPT and short circuit test are usually conducted before the continuous test to validate the SiC device and the gate driver. MV converters based on high voltage SiC devices have been designed and tested at rated voltage and power, yet the detailed incremental testing steps are not covered [31],[34]. In [81], comprehensive testing and qualification of the gate driver and its isolated power supply for high voltage SiC MOSFETs and IGBTs are discussed in detail, including DPT, short circuit test, and continuous test. The testing focuses on validating the gate driver's thermal performance and its performance in withstanding the CM voltage and current, instead of the performance of the HB phase leg. The dc-dc continuous test as the buck-boost converter is adopted since it can generate CM voltage with high magnitude.

Nonetheless, the dc-dc continuous test generates the *dv/dt* different from that which occurs in the phase leg when it functions as part of a modular MV converter, especially when the converter is used in dc/ac applications.

In [65], a detailed testing methodology is developed to fully qualify a HB phase leg based on the 10 kV SiC MOSFET module, which is built to serve as the building block of a MMC converter. In the system-level testing of the phase leg, the continuous test with pump-back configuration is required in both dc-dc and dc-ac mode. The continuous test involves two identical HB phase legs. One phase leg draws the power from the dc source, and the other phase leg pumps the power back to the source. However, the pump-back test setup is different from the MMC converter and other modular MV converters with multiple modules connected in series, where the phase leg can experience much higher *dv/dt* and hence CM current than those in the continuous test with pump-back configuration. For example, the phase leg in one MMC can experience ≥2X *dv/dt* of a single high voltage SiC device. In terms of the capability of withstanding high *dv/dt* and CM voltage, the phase leg cannot be fully qualified with the testing method in [65]. In [82], the developed three-phase pump back continuous test for the HB phase leg also has this issue, which cannot fully qualify the phase leg in terms of high *dv/dt* and CM voltage.

In summary, the testing of the phase leg based on high voltage SiC devices has not received much attention, although many MV converters based on high voltage SiC devices have been demonstrated. The continuous test setups developed to test the phase leg in the literature are not able to fully qualify the phase leg for modular MV converter applications, in which the thorough qualification of phase leg's capability to withstand high *dv/dt* and

its resulting noise cannot be provided. Test setups in the literature can only generate the *dv/dt* of a single high voltage SiC device, but the phase leg can experience much higher *dv/dt* in a modular MV converter.

2.4 Summary

Previous work on the switching performance evaluation of 10 kV SiC MOSFETs and other high voltage SiC devices as well as the design and testing of the phase leg based on high voltage SiC devices is reviewed in this chapter. The switching performance evaluation with DPT is reviewed together with influencing factors of the switching performance. Two influencing factors that have not been investigated in detail include the parasitic capacitance and the freewheeling diode, which can be realized by the body diode or adding an external anti-parallel JBS diode.

Existing work on the design and testing of the HB phase leg is summarized, especially the gate driver design together with the overcurrent protection. Among the reviewed overcurrent protection methods, desat protection stands out in the protection for 10 kV SiC MOSFETs, because of its excellent overall performance in terms of response speed, noise immunity, and ease of implementation. Desat protection is not as fast as other methods based on Rogowski coil and current transformer, which may prevent its usage in some occasions. It is still challenging to design the desat protection with faster response while maintaining excellent noise immunity. In addition, the premature insulation breakdown and the resulting flashover fault become non-negligible in MV converters based on 10 kV SiC MOSFETs. Yet the gate driver design after taking the flashover fault into account are still not studied comprehensively.

In terms of testing, the comprehensive testing of the phase leg has not attracted much attention yet in the research community. The main drawback of the test methods in the literature is their inability to fully test the phase leg's capability to withstand high *dv/dt* and the resulting noise. This drawback is non-negligible because the phase leg could experience much higher *dv/dt* and hence stronger noise interference in a modular MV converter.

CHAPTER 3. BASELINE DESIGN AND TEST OF A 10 KV SIC MOSFET BASED PHASE LEG

A baseline design of a HB phase leg based on 10 kV SiC MOSFETs with continuous operation capability is introduced in this chapter, which is validated by an ac-dc continuous test at 6.5 kV dc-link voltage. The target of the baseline design is that the phase leg can operate as a building block of a modular MV converter. Thus, the baseline design serves as the foundation for the research about switching performance evaluation and phase leg design. Baseline testing procedures and results of the phase leg are also presented in detail.

It should also be noted that part of the content in this chapter is from the author's Master's thesis [1]. Also, part of the content in this chapter is from the author's paper published in *IEEE ECCE 2019* conference [83] and the author's paper published in *IEEE APEC 2020* conference [84].

3.1 Overview of the Phase Leg

3.1.1 10 kV SiC MOSFET

The half bridge phase leg is based on 10 kV/20 A discrete SiC MOSFETs from Wolfspeed (XPM3-10000-0350B). The device has a non-isolated package with a large drain plate also for heat dissipation, as shown in Fig. 3-1. Inside the package is one 3rd generation 10 kV/350 mΩ SiC MOSFET die [29]. Due to an issue in device package design, mechanical and electrical connection between the wire bond and the gate terminal of the package is not robust.

Characterization results with a curve tracer show that the 10 kV SiC MOSFETs available for the phase leg construction have almost the same on-resistance in forward conduction and reverse conduction with the same gate-to-source voltage and junction temperature. The 3rd generation 10 kV/350 mΩ SiC MOSFET from Wolfspeed does not have the degradation issue during the body diode conduction [54], [55]. Therefore, the body diode is used as the freewheeling diode, and external anti-parallel JBS diode is not needed in the phase leg. Gate-to-source voltage V_{gs} has little influence on the on-resistance as long as it exceeds 15 V, as indicated in Fig. 3-1.

3.1.2 Architecture of the Phase Leg

The designed 6.5 kV half bridge phase leg consists of two MOSFETs, two isolated power supplies, the gate driver, the heatsink, the PCB busbar, and the dc-link capacitor. The architecture of the phase leg is shown in Fig. 3-2(a). Such architecture is designed to ensure that the phase leg has the capability to operate as a building block for a modular MV converter. The communication interface marked in green in Fig. 3-2(a) communicates with the controller via fiber optics. Four terminals are available for connection, including DC+, DC-, midpoint of dc-link, and midpoint of the half bridge phase leg. The phase leg has an 8.75 μF dc-link capacitor, realized by four 1.9 kV film capacitors in series. The rated dc-link voltage of the phase leg is 6.5 kV, with 1.1 kV margin for overvoltage during the switching transients.

The detailed three-dimensional (3D) design of the phase leg is drawn in Fig. 3-2(b). A gate driver board is placed above the two MOSFETs to drive the devices, powered by two isolated power supplies. The PCB busbar finally finishes the power loop by connecting

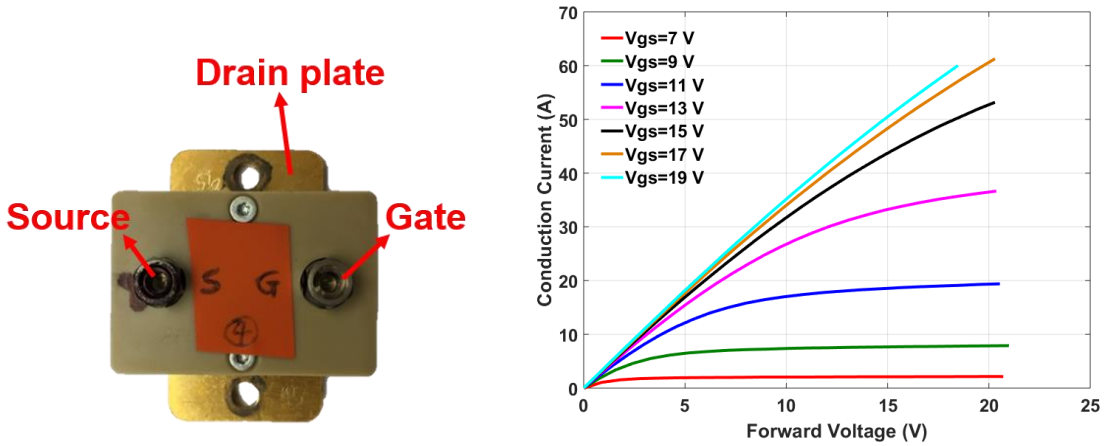
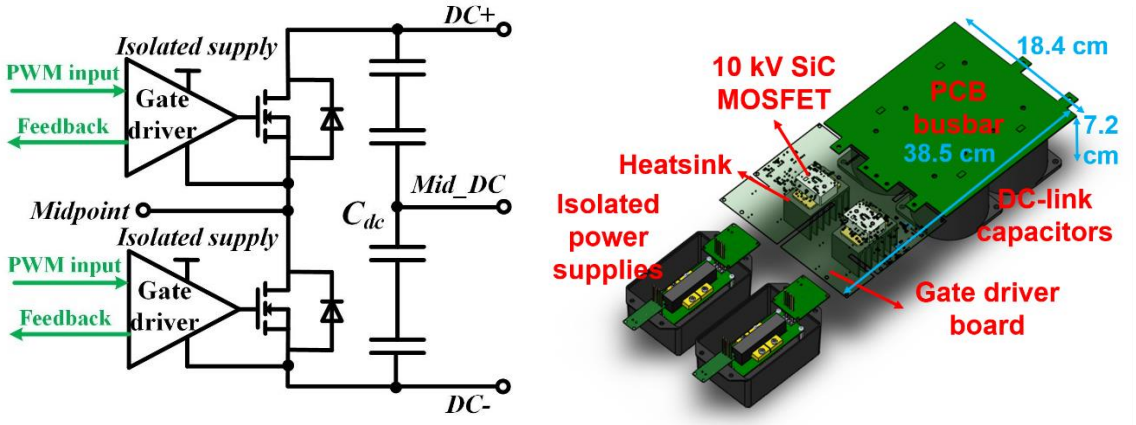


Fig. 3- 1. Discrete 10 kV SiC MOSFET in the half bridge phase leg (left) and its forward characteristic at room temperature (right).



(a) (b)

Fig. 3- 2. Half bridge phase leg based on 10 kV SiC MOSFETs: (a) Architecture of the phase leg; (b) Detailed 3D model of the phase leg.

the dc-link capacitor with the MOSFETs. FR4 is the insulation material in the PCB busbar, and better material can be adopted for more reliable insulation in the future.

Each MOSFET in the phase leg has a separate floating heatsink for heat dissipation. The heatsink is not isolated from the MOSFET, hence the heatsink has the same potential as the drain plate of the MOSFET it is connected to. During continuous operation, a fan is used to cool devices and heatsinks. In the design, clearance distance requirements in IPC-2221B standard and creepage requirements in UL 60950-1 standard are followed to ensure reliable insulation [85], [86].

3.2 Gate Driver Design

The gate driver for the 10 kV/20 A SiC MOSFETs is designed to realize fast switching speed and continuous operation of the MOSFET. To achieve the target, specifications of the gate driver are developed and summarized in Table 2. The main challenges are high voltage insulation and high *dv/dt*. The gate driver board is designed to meet the clearance and creepage requirement for 10 kV to achieve robust insulation [39]. The dead time function is desirable to prevent shoot-through. Feedback signal sent back to the controller in every switching cycle is necessary for the controller to monitor the status of the communication and gate driver during continuous operation. If a short circuit or overcurrent fault is detected, a fault signal is sent back to the controller via a feedback signal.

The specifications in Table 2 have been successfully achieved in the designed gate driver, which is composed of signal transfer and feedback stage, gate driving stage, and overcurrent protection stage. The block diagram of the gate driver is shown in Fig. 3-3.

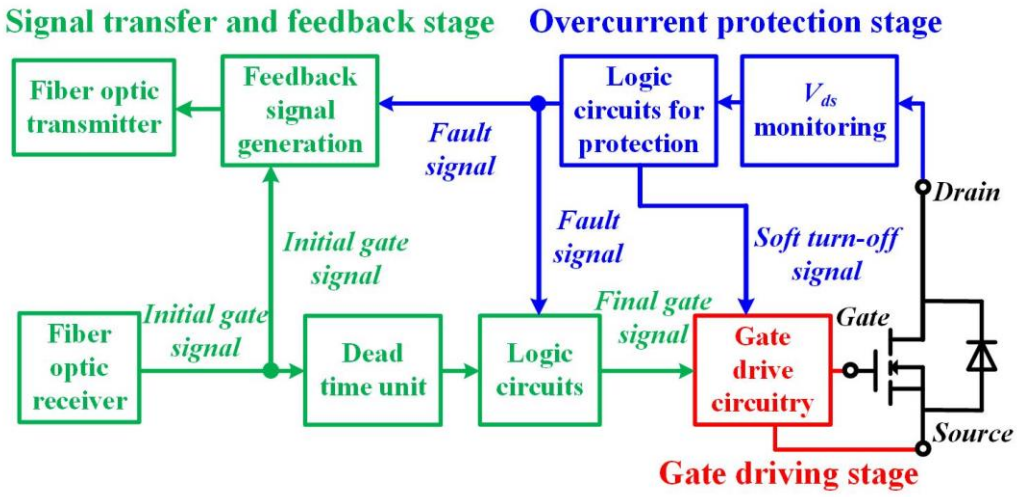


Fig. 3- 3. Block diagram of designed gate driver for 10 kV SiC MOSFETs.

Table 2. Specifications of the designed gate driver.

Specification	**Requirement**	**Design result**
Driving voltage range	Minimum: -5 V; Maximum: +20 V	-5 V for off state; 15 V for on state
Peak driving current	> 8 A	9 A
Rise and fall times	< 30 ns	22 ns rise time; 15 ns fall time
Short circuit protection	< 1.5 µs response time with soft turn-off	< 1.3 µs response time with soft turn-off
Status feedback	Status feedback signal sent back to controller in every switching cycle	Feedback signal generated for every rising or falling edge in gate signal
Dead time	Dead time realized in the gate driver with hardware	500 ns dead time realized

3.2.1 Signal Transfer and Feedback Stage

Signal transfer and feedback stage is responsible for the communication between the controller and the gate driver during continuous operation. The communication is realized with fiber optics to provide ample signal isolation between the controller and the gate driver.

The dead time function is implemented with a delay IC in this stage. With an AND logic IC and the delay IC, the dead time is realized by applying 500 ns delay to the rising edge of the initial gate signal and zero delay to the falling edge. The updated gate signal becomes the final gate signal for gate drive IC if overcurrent fault is not detected. The final gate signal is always LOW if the overcurrent protection is triggered until it is reset. The generation of the gate signal sent to the gate drive IC is summarized in Fig. 3-4.

The feedback signal sent from the gate driver is essential during continuous operation. In most gate drivers for SiC MOSFETs reported in the literature, the feedback signal is only designed to transmit the overcurrent fault signal. In this case, the controller knows nothing about the status of the gate driver and communication until the overcurrent or short circuit fault happens. Such delay is not acceptable in a MV converter based on 10 kV SiC MOSFETs. Hence, a feedback signal sent back to the controller is desirable to monitor the status of communication and gate driver in every switching cycle. In fact, this function is provided by numerous commercial gate drivers from Power Integrations, but the circuit design details are not disclosed.

To realize this target, a simple feedback scheme is designed to generate a feedback signal acknowledging every rising edge and falling edge in the received gate signal. As can be seen in Fig. 3-5, the feedback scheme utilizes the delay IC in the dead time unit and a

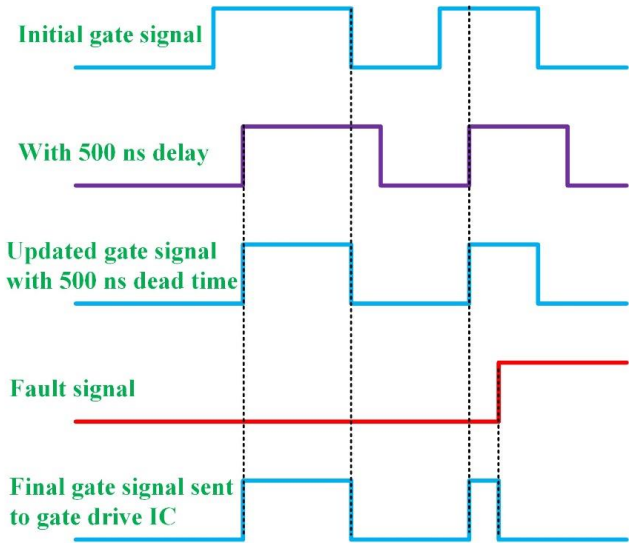


Fig. 3- 4. Diagram of the generation of final gate signal sent to gate drive IC with 500 ns dead time realized in gate driver.

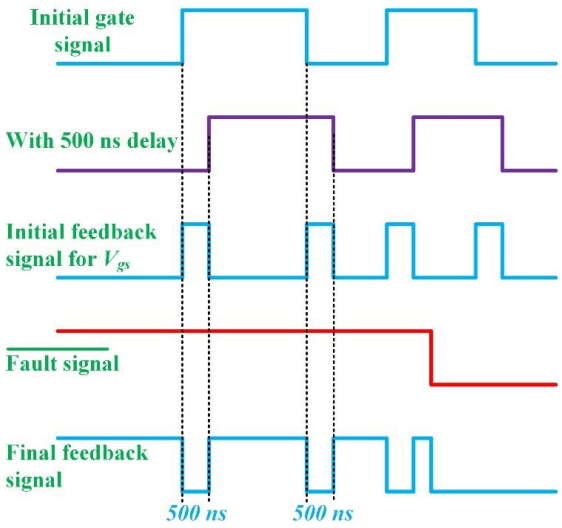


Fig. 3- 5. Diagram of the generation of final feedback signal sent back to controller.

XOR logic gate. The final feedback signal is also able to report the overcurrent fault. After the gate signal from the controller has a rising edge or falling edge, the feedback signal should stay LOW for 500 ns. Since the overcurrent fault signal lasts for a much longer time, the overcurrent fault is recognized by the controller if the feedback signal remains LOW for over 600 ns.

Several considerations should be recognized in the selection of the length of the signal to acknowledge the rising or falling edge in the received gate signal. This feedback scheme requires the conduction time of the 10 kV SiC MOSFET to be longer than the signal for the acknowledgement. Long feedback signal for the acknowledgement limits the duty cycle when the MOSFET operates at higher frequency. Discrete 10 kV SiC MOSFETs have switching frequency up to 80 kHz in soft-switching converters [31], [34]. The long feedback signal for the acknowledgement also leads to long delay time for the controller to identify the overcurrent fault based on the received feedback signal. The feedback signal for the edge acknowledgement should not be too short for the controller to read. In this case, it could be overwhelmed by the highly unpredictable noise in the feedback signal. Finally, the feedback signal for the edge acknowledgement is determined to be 500 ns LOW to achieve strong noise immunity, and it only requires the duty cycle higher than 4% at 80 kHz switching frequency.

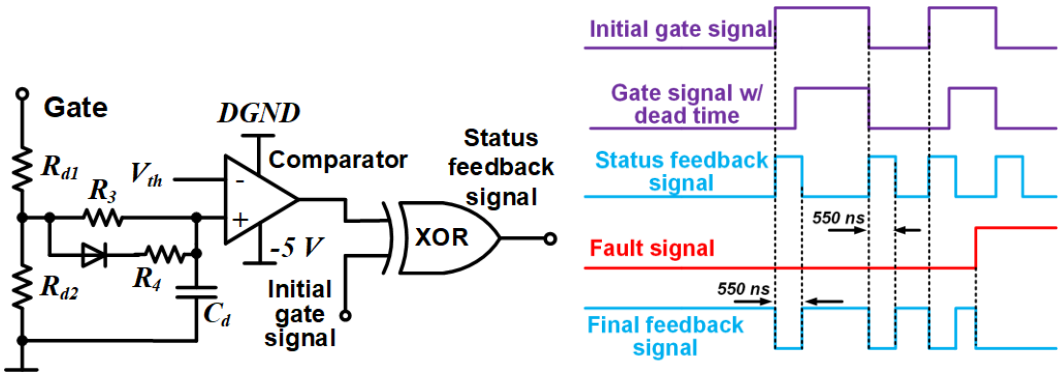
The simple feedback scheme can monitor the status of fiber optic communication and some components of the gate driver. If the feedback signal does not turn LOW within 200 ns after the rising or falling edge in the gate signal, a fault is detected by the controller. However, the simple feedback scheme cannot confirm that the gate signal is properly

transformed to the correct V_{gs} of MOSFET. If the gate driver IC fails, the status feedback signal will not report the fault in time. An updated feedback scheme is developed to overcome this drawback by generating the feedback signal based on the measured V_{gs}.

Details of updated feedback scheme are displayed in Fig. 3-6, including the designed circuit. The measured gate voltage from the voltage divider is compared with the gate threshold voltage to check if the MOSFET is turned on or off. The voltage divider and the comparator are grounded at -5 V which should be the same as -5 V for the gate loop, and DGND has the same potential as the source of MOSFET. Threshold voltage of the comparator is selected so that the comparator outputs HIGH when V_{gs} is higher than +3 V, the gate threshold voltage of the 10 kV SiC MOSFET at 100 ˚C [44]. The selected voltage divider ratio is 1/5, and the comparator threshold voltage is -3.4 V. Then, the comparator output signal is sent to a XOR logic gate together with the initial gate signal to generate status feedback signal. The length of status feedback signal is 550 ns, which is slightly longer than 500 ns with the purpose of simplifying circuit design. As illustrated in Fig. 3-7(a), benchtop test results show that the final feedback signal coincides well with the design in Fig. 3-6(b). Fig. 3-7 also demonstrates that the feedback signal can monitor the status of the gate driver during the ac-dc continuous test of the phase leg in every switching cycle.

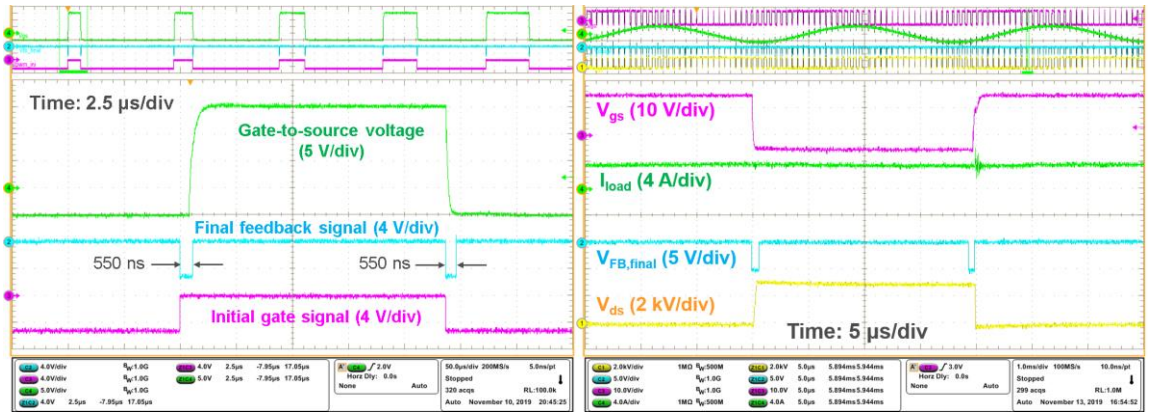
3.2.2 Gate Driving Stage

The gate drive IC is selected based on the developed specifications in Table 2. The main considerations are peak driving current, rise/fall time, and propagation delay. The desat protection function in gate drive IC is not considered, and more details are introduced in the design of overcurrent protection stage. Signal isolation is also not required since the



(a) (b)

Fig. 3- 6. (a) Designed circuit for the update scheme to realize status feedback function; (b) Generation of final feedback signal with the updated feedback scheme.



(a) (b)

Fig. 3- 7. Experimental waveforms of final feedback signal with the updated feedback scheme: (a) 0 V dc bus voltage; (b) 3 kV ac-dc continuous test of phase leg.

fiber optics provide ample isolation. The peak driving current of the gate drive IC should be higher than 8 A, otherwise a buffer is needed which further increases the propagation delay. Among numerous candidates, IXDD609SI from IXYS with 9 A peak driving current is selected due to its short propagation delay and rise/fall time.

The on-state and off-state driving voltage are 15 V and -5 V, respectively. 15 V is adopted to achieve lower current and energy loss in short circuit condition. -5 V for off-state ensures reliable turn-off of the device. The turn-on and turn-off gate resistance are 15 Ω and 3 Ω, respectively, to achieve the trade-off between switching speed and switching loss. With -5 V V_{gs} in off state, active Miller clamping circuit to prevent cross-talk is not necessary for the 10 kV/20 A SiC MOSFET, thanks to its large ratio between input capacitance and Miller capacitance [44]. The 15 Ω turn-on resistance and 3 Ω turn-off resistance are also helpful in limiting the turn-on *dv/dt* to 100 V/ns and the spurious gate voltage.

3.2.3 Overcurrent Protection Stage

Among the several overcurrent protection schemes for SiC MOSFETs, desat protection scheme is selected to protect the discrete 10 kV/20 A SiC MOSFETs. Desat protection requires relatively easy implementation to achieve satisfactory response time, good noise immunity, and effective protection in different cases. In this chapter, the response time is defined as the time interval between the starting point of the short circuit fault and the moment when the short circuit current reaches the peak value.

The designed desat protection scheme protects the 10 kV SiC MOSFET in short circuit/overcurrent condition with a response time of less than 1.3 μs. After the fault is

detected, soft turn-off is applied with a gate resistance of 47 Ω to safely turn off the MOSFET, and the fault is reported to the controller via the feedback signal. The short circuit withstand time of the 10 kV/20 A SiC MOSFETs typically ranges from 2 μs to 10 μs. Such a wide range of short circuit performance is reasonable since the device is still in R&D stage and not mature enough for commercial applications. Wolfspeed has also reported the 3rd generation 10 kV SiC MOSFET with enhanced short circuit performance and over 13.6 μs short circuit withstand time at 5 kV [22]. Therefore, the protection should respond within 1.5 μs after a short circuit or overcurrent fault occurs to safely protect the MOSFET. Considering the tolerance of components and other non-ideal factors, the specification for the response time is 1.3 μs.

The threshold voltage of desat protection is determined based on the I-V characteristic of the 10 kV/20 A SiC MOSFET, which is heavily influenced by the junction temperature, as illustrated in Fig. 3-8. The threshold current is lower at higher junction temperature due to the higher on-state voltage drop. The threshold voltage is selected based on the I-V characteristic at 125 ˚C, otherwise the protection might be falsely triggered during the normal operation at higher junction temperature. The threshold current should be set as low as possible, since the drain current of the SiC MOSFET still increases rapidly in active region as the drain-to-source voltage V_{ds} keeps increasing during the short circuit fault. At 125 ˚C, the selected threshold current is 20 A, the rated current of the 10 kV SiC MOSFET. Taking into account slight variances in the I-V characteristic among different devices, the selected threshold voltage is 15 V, leading to 42.85 A threshold current at 25 ˚C. The specifications of the designed desat protection are summarized in Table 3.

Table 3. Specifications of the designed desat overcurrent protection.

Specification	Detail
Response time	<1.3 μs
Threshold current	20 A at 125 ˚C 42.85 A at 25 ˚C
Soft turn-off	Turn-off with 47 Ω gate resistance
Output signal to controller	Always LOW signal via fiber optics if triggered
Voltage rating of desat diode	>10 kV

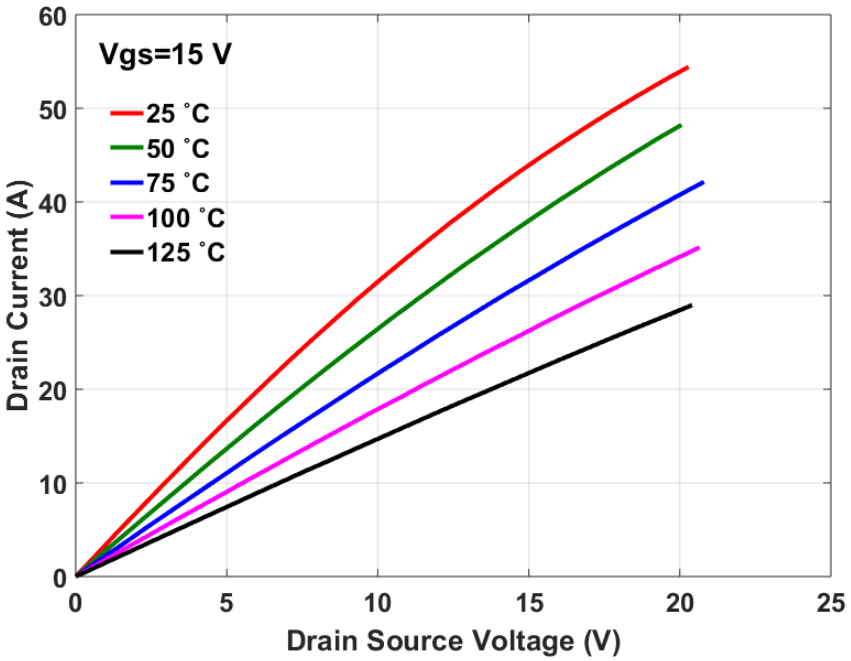


Fig. 3- 8. Output characteristic of the 10 kV /20 A SiC MOSFET under different temperatures.

In addition, the voltage drop on the desat diode should be considered when determining the threshold voltage. The desat diode blocks the dc-link voltage when the MOSFET is in OFF state to protect the desat protection circuitry. The rated voltage of the desat diode should be the same as that of the MOSFET to achieve good reliability. The desat diode with 10 kV blocking voltage is implemented with four 3.3 kV SiC Schottky diodes (GAP3SLT33-220FP) in series together with balancing resistors. The pads in PCB for the 3.3 kV diode are coated with insulation material (Konform SR). With the capability to block voltage up to 13 kV, such design ensures robust insulation between the drain terminal of the MOSFET and the protection circuitry. Selecting 3.3 kV SiC diode makes the design more robust in terms of commercial availability, compared to the solution based on a 10 kV SiC diode which is difficult to purchase. Also, the parasitic capacitance in parallel with the desat diode is reduced effectively, which significantly benefits the noise immunity of the protection under high *dv/dt*. Still, the implementation with four diodes introduces 4 V total voltage drop [87]. Thus, the eventual selected threshold voltage is 19 V for the desat protection.

Desat protection can be implemented by either the gate driver IC with integrated desat protection function or the circuitry based on discrete components. The gate driver IC with desat protection function typically requires a large blanking capacitor to suppress the noise, leading to long response time. Also, the 19 V threshold voltage for the 10 kV/20 A SiC MOSFET is much higher than the threshold voltage of desat protection provided by the gate drive ICs available in the market. The circuitry based on discrete components is

hence designed to realize desat protection, whose details are shown in Fig. 3-9, in which the parasitic capacitances marked in red should be considered in the design.

Resistors R_{blk}, R_{damp}, and blanking capacitor C_{blk} together realize the blanking time which prevents the false triggering during the turn-on transient when the drain-to-source voltage V_{ds} drops quickly to on-state voltage. The clamping diode D_{blk} is installed to clamp V_{desat} and prevent the input voltage of the comparator from exceeding the allowed input voltage range. The comparator and the logic control circuit are grounded at V_{clamp} (-5 V). Resistor R_{cla} (20 Ω) and MOSFET M_{cla} clamp V_{desat} at V_{clamp} (-5 V) when the 10 kV SiC MOSFET is shut off, and they prevent false triggering due to the high positive *dv/dt* during the turn-off transient of the 10 kV SiC MOSFET.

The response time of desat protection is mainly determined by the blanking time. The blanking time should be in effect until the drain-to-source voltage V_{ds} drops to on-state voltage without ringing. If blanking time is too short, V_{desat} can exceed the threshold voltage before it is clamped by D_{desat}. It is necessary to check the turn-on transients of the 10 kV SiC MOSFET to set a suitable blanking time. Preliminary DPT results show that required blanking time is longer if the load current is higher. According to the DPT results at 6.25 kV/20 A with the same gate driver parameters in Fig. 3-10, it takes 480 ns for V_{ds} to reach steady state, after V_{gs} starts to rise. The junction temperature has little influence on the length of this time interval. Considering the delay in gate drive IC, the blanking time should be longer than 550 ns to avoid false triggering of the protection when the 10 kV SiC MOSFET turns on normally. Avoiding false triggering during the turn-off transient with positive *dv/dt* is also necessary for desat protection. The displacement current through the

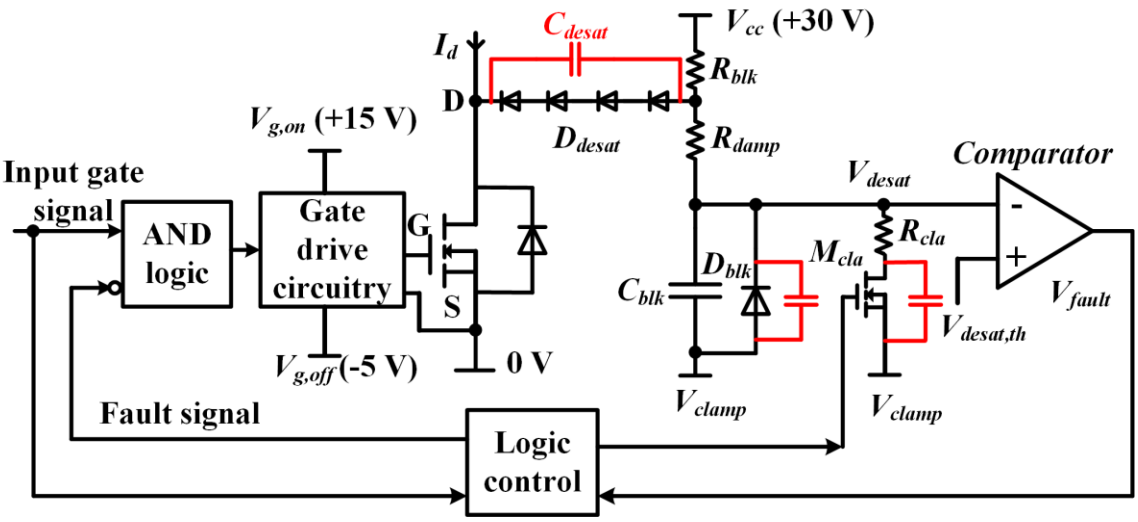


Fig. 3- 9. Implementation of desat protection in the gate driver for 10 kV SiC MOSFETs.

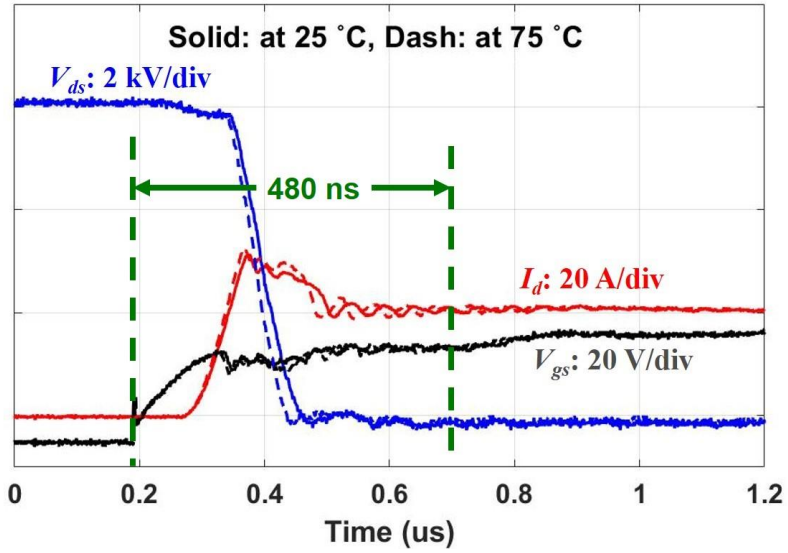


Fig. 3- 10. Turn-on transient of the 10 kV SiC MOSFET at 6.25 kV/20 A.

parasitic capacitance of D_{desat} charges C_{blk} and increases V_{desat} during the turn-off transient with high *dv/dt*, and the protection can be falsely triggered. The oscillation excited by the high positive *dv/dt* makes the situation worse. To dampen the oscillation, a small resistor R_{damp} (47 Ω) is added [66]. R_{cla} and M_{cla} are designed to clamp V_{desat} before high positive *dv/dt* occurs [66]. In other words, the clamp should be effective within the turn-off delay time. Once the gate signal has a falling edge, M_{cla} will start to turn on to clamp V_{desat} after a delay of 80 ns. V_{desat} is clamped at -5 V before the positive *dv/dt* occurs during the turn-off transient. A RC circuit is added in the gate of M_{cla} to realize the 80 ns delay and suppress the noise at the gate of M_{cla}.

The blanking time is tuned by changing R_{blk} and C_{blk}. The blanking time is the time it takes to charge V_{desat} from V_{clamp} to the 19 V threshold voltage $V_{desat,th}$. Hence, all parasitic capacitances between V_{desat} and -5 V V_{clamp} should be considered, including nonlinear parasitic capacitances from D_{blk} and M_{cla} as well as the parasitic capacitances due to the PCB layout. The blanking time is calculated with the following equation, in which the effect of the voltage divider connected with V_{desat} is neglected.

$$t_{blk} = C_{total}(R_{blk} + R_{damp})\ln\left(\frac{V_{cc} - V_{clamp}}{V_{cc} - V_{desat,th}}\right) \tag{3.1}$$

In the equation, C_{total} is the total capacitance between V_{desat} and -5 V. A large C_{blk} is preferred to suppress the noise in V_{desat} and achieve better noise immunity. Finally, 6.49 kΩ R_{blk} and 75 pF C_{blk} are selected to provide 1.2 μs blanking time and strong noise suppression. In one prototype of the gate driver, the distribution of 1.26 μs total response time is shown in Table 4, determined by the experiment in the initial test at 0 V dc-link voltage. The parasitic capacitances account for 44.3% of the total blanking time (1.22 μs).

Table 4. Distribution of the total response time in one gate driver prototype.

Total response time	**1.26 µs**
Comparator and control delay	0.04 µs
Blanking time due to the installed C_{blk} (75 pF)	0.6 µs
Blanking time due to all parasitic capacitances	0.54 µs
Blanking time due to delay in the gate of M_{cla}	0.08 µs

The shorter response time is achievable by reducing R_{blk} and parasitic capacitance brought by D_{blk} and M_{cla} as well as PCB layout. By choosing 4 kΩ R_{blk} and 56 pF C_{blk}, the response time will be reduced to 730 ns.

3.3 Baseline Test of the Phase Leg

The designed half bridge phase leg should be tested comprehensively to be qualified for a building block of a modular MV converter. The ac-dc continuous test at rated voltage is thus required. Considering high dc-link voltage together with high *dv/dt* and the immaturity of the MOSFETs, the testing becomes more important and challenging. The cautious testing procedures should be designed to quickly identify any issues and prevent damage of the expensive 10 kV SiC MOSFETs. In this section, the baseline testing procedures and testing results of the phase leg will be presented.

3.3.1 Testing Procedures

Detailed and systematic testing procedures have been developed to standardize the testing. Generally, the baseline test is designed to be nondestructive and reduce the risk of damage of the expensive and fragile MOSFETs. Before the testing at phase leg level, each part is tested individually. The testing of the phase leg is conducted step by step with four steps in total, as listed in Table 5. The testing steps should be conducted in sequence. Only after the phase leg operates well in the previous step could the testing move on to the next step.

In the initial test, it is necessary to check the electrical connection between the MOSFET die and the gate driver board. Particularly, the connection of gate terminal is a concern, since the wire bond for the gate is a weak point. The gate-to-source voltage V_{gs}

Table 5. Details of four steps in the systematic testing of the phase leg.

Step	Name	Purposes
No. 1	Initial test	1. Electrical connection check; 2. Gate drive function and protection at 0 V
No. 2	Double pulse test (DPT)	Fundamental test of MOSFETs and the phase leg up to 6.5 kV/ 20 A
No. 3	Short circuit test	Desat protection of the gate driver at 6.5 kV dc-link voltage
No. 4	Continuous test	Continuous operation of the half bridge phase leg at 6.5 kV dc-link voltage

is measured and checked with the PWM gate signal applied, especially the rising edge and falling edge. The rising time and falling time of V_{gs} are measured and compared with the estimated value. If the rising or falling time is too short, the gate region of the die is not well connected with the gate driver board. Desat protection together with soft turn-off is examined by disconnecting the desat diode from the drain terminal and feeding in the gate signal. In addition to the soft turn-off, attention should be paid to the response time and feedback signal. In summary, this step checks the gate loop and the circuitry for desat protection and soft turn-off.

The next step is DPT of both the upper MOSFET and lower MOSFET. DPT is the fundamental electrical test for the MOSFETs, including the functionality and insulation capability of all components. Even if the insulation failure occurs in this step, the damage is still limited. DPT of the upper MOSFET also provides the preliminary test of the capability of the gate driver and the isolated power supply to withstand high common mode voltage with high *dv/dt*.

The short circuit test is conducted for the upper and lower MOSFETs as the No. 3 step to make sure that the overcurrent protection can protect the MOSFET at rated dc-link voltage. Two types of short circuit tests are commonly conducted: hard switching fault (HSF) and fault under load (FUL) [88]-[90]. The desat protection has shorter response time and lower energy loss under FUL due to the positive *dv/dt* in the drain-to-source voltage, and the *dv/dt* results in negligible increase in V_{gs} and short circuit current of the 10 kV/20 A SiC MOSFET [66], [90]. Therefore, only HSF short circuit test is conducted. After the

HSF short circuit test of the lower MOSFET is finished, the test setup is reconfigured to test the desat protection for the upper MOSFET.

Continuous test is the last step to test the continuous operation capability of the phase leg at 6.5 kV rated voltage. In the ac-dc continuous test, the half bridge phase leg is configured as a half bridge inverter with inductive load (175 mH), as shown in Fig. 3-11. The continuous test as an inverter enables both MOSFETs in the phase leg to conduct time-varying and bi-directional current in one line cycle. It is thereby a more comprehensive test than the continuous test as a dc-dc converter.

175 mH is the highest inductance that can be realized with the high voltage inductive load in the laboratory, and the rated peak current for continuous operation is 9 A. 300 Hz fundamental frequency is chosen to further increase the impedance of the inductive load and limit the magnitude of output sinusoidal current. The active power is the power loss in the test setup. The continuous test adopts bipolar SPWM modulation to regulate output sinusoidal current, with the switching frequency of 10 kHz. The peak value of the fundamental component of the output AC current I_{out} is calculated with the equation below.

$$I_{out} = \frac{0.5 m V_{in}}{2\pi f_{line} L_{load}} \tag{3.2}$$

The modulation index m regulates the magnitude of the output ac current as the dc-link voltage V_{in} increases. L_{load} is 175 mH, and f_{line} is 300 Hz, the fundamental frequency of the test. The continuous test should last for at least five minutes. The continuous test is also conducted at lower dc-link voltage first, and the results are carefully evaluated before the test at higher dc-link voltage.

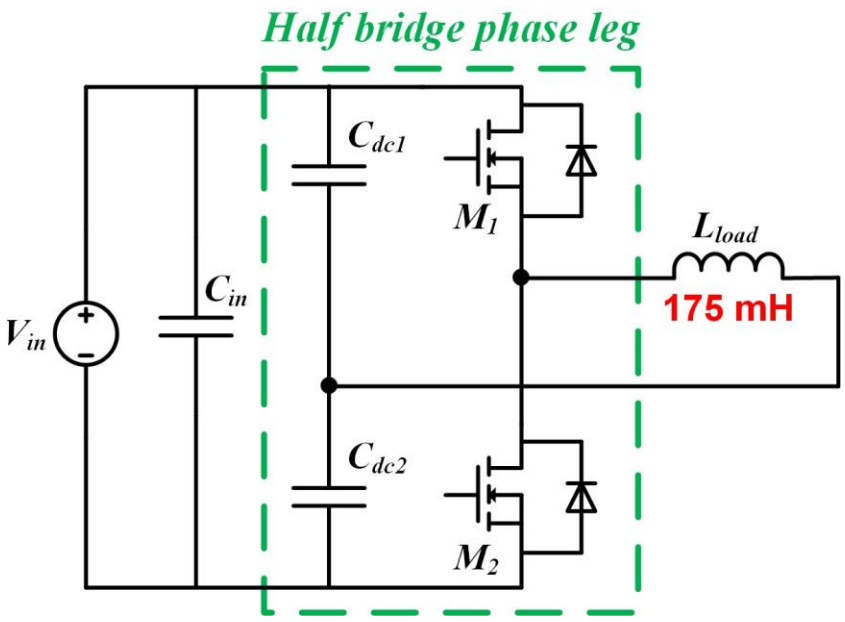


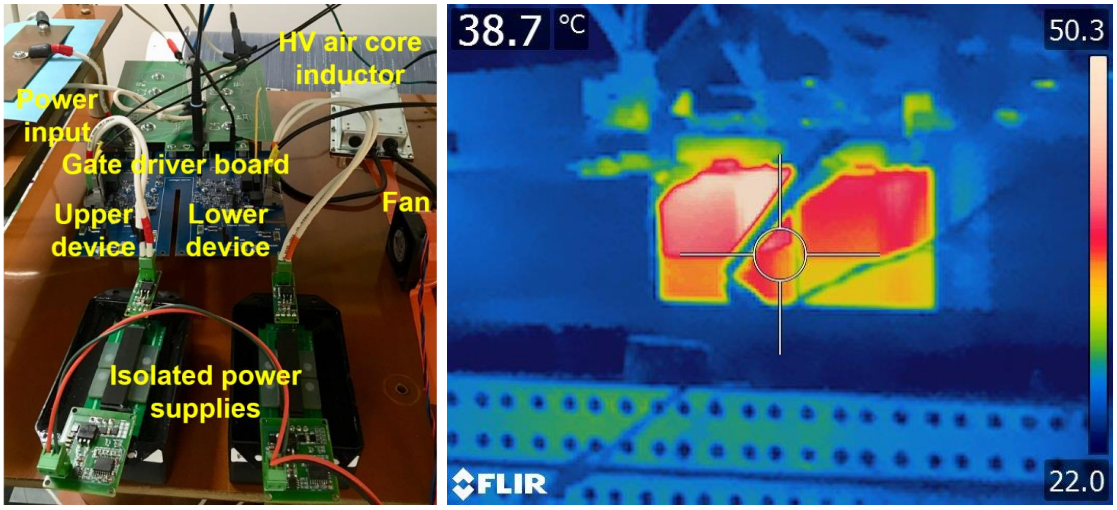
Fig. 3- 11. Circuit diagram of the continuous test of the designed phase leg.

3.3.2 Testing Results

The built half bridge phase leg has been tested by following the developed testing procedures. Other than step No. 1, all testing procedures should be conducted with the designed high voltage test platform. The test platform is equipped with high voltage dc power supply from Spellman, different high voltage load inductors, the input capacitor, the controller with fiber optic interface, and so on. Therefore, the test platform can be easily configured for DPT, short circuit test for both lower and upper MOSFET, and the continuous test. The half bridge phase leg prototype in the test platform can be seen in Fig. 3-12(a). The 7 mH air core inductor serves as the load inductor in DPT, and the fan is only used for the continuous test.

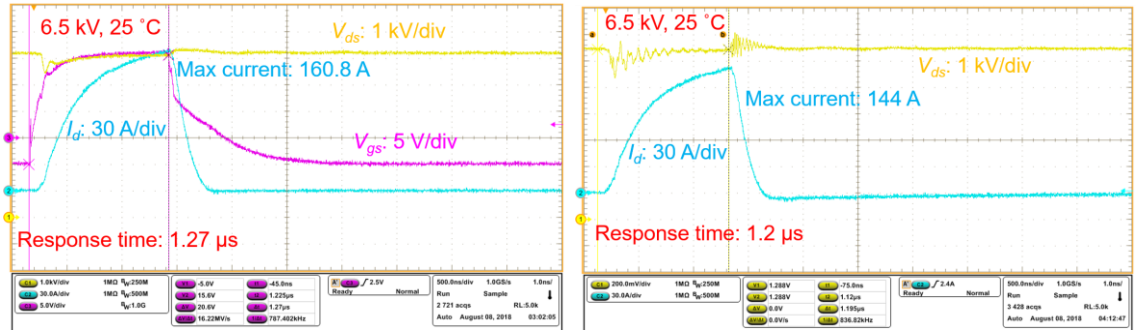
Testing results have shown that the designed phase leg is capable of operating continuously at 6.5 kV rated dc-link voltage, with satisfactory performance in all testing procedures. Results of the short circuit test and the continuous test will be discussed in detail. The DPT results are not shown in this chapter, since DPT results and switching performance will be studied in depth in Chapter 4.

Short circuit test results explicitly prove that the designed protection is able to protect the MOSFET at 6.5 kV. As shown in the HSF test waveform of the lower MOSFET in Fig. 3-13(a), the soft turn-off with a *di/dt* of 0.57 A/ns is triggered after the 1.27 μs response time, leading to negligible overvoltage under 160.8 A peak current. The MOSFET is safely turned off at 6.5 kV rated voltage. The HSF test result of the upper MOSFET at 6.5 kV is displayed in Fig. 3-13(b), and the MOSFET is safely turned off with 1.2 μs response time. The peak current is still lower than 20X rated current of the MOSFET. V_{gs} of the upper MOSFET cannot be measured due to the high common mode voltage, still the



(a) (b)

Fig. 3- 12. (a) Phase leg prototype in the high voltage test platform; (b) Thermal image of the phase leg prototype during 6 kV ac-dc continuous test.



(a) (b)

Fig. 3- 13. HSF short circuit test waveforms: (a) Lower device in the phase leg; (b) Upper device in the phase leg.

di/dt and voltage overshoot indicate the soft turn-off. The response time of desat protection for both MOSFETs meets the 1.3 μs specification, and the slight difference is caused by the components' tolerances.

The ac-dc continuous switching test of the phase leg has been conducted with the dc-link voltage up to 6.5 kV. The continuous switching test as a half bridge inverter outputs the sinusoidal load current, as can be seen in the top window of the continuous test waveform at 6.5 kV in Fig. 3-14. With a modulation index of 0.5, the maximum load current is ~6 A. The high frequency component in the load current during the switching commutation is due to the displacement current in the parasitic capacitance of the load inductor.

The main window of the waveform features the turn-off transient of the lower MOSFET as the synchronous device with 5.5 A load current. The body diode of the lower MOSFET still conducts after its channel is shut off, so V_{ds} of the lower device is nearly zero until the upper MOSFET turns on. V_{ds} of the lower MOSFET is measured with a high voltage differential probe, and V_{gs} of the lower MOSFET is monitored with a 1 GHz passive voltage probe. Without any anti-cross-talk circuit, V_{gs} of the lower MOSFET increases slightly due to high positive *dv/dt* (>70 V/ns), yet the margin between its peak and the gate threshold voltage is still large. This waveform demonstrates that the cross-talk is not a serious issue in the 10 kV/20 A SiC MOSFETs due to their high input capacitance compared to Miller capacitance. The designed phase leg also has good thermal performance. Fig. 3-12(b) displays the thermal image of the phase leg during the ac-dc continuous test at 6 kV/6 A, in which the peak temperature is less than 60 ˚C.

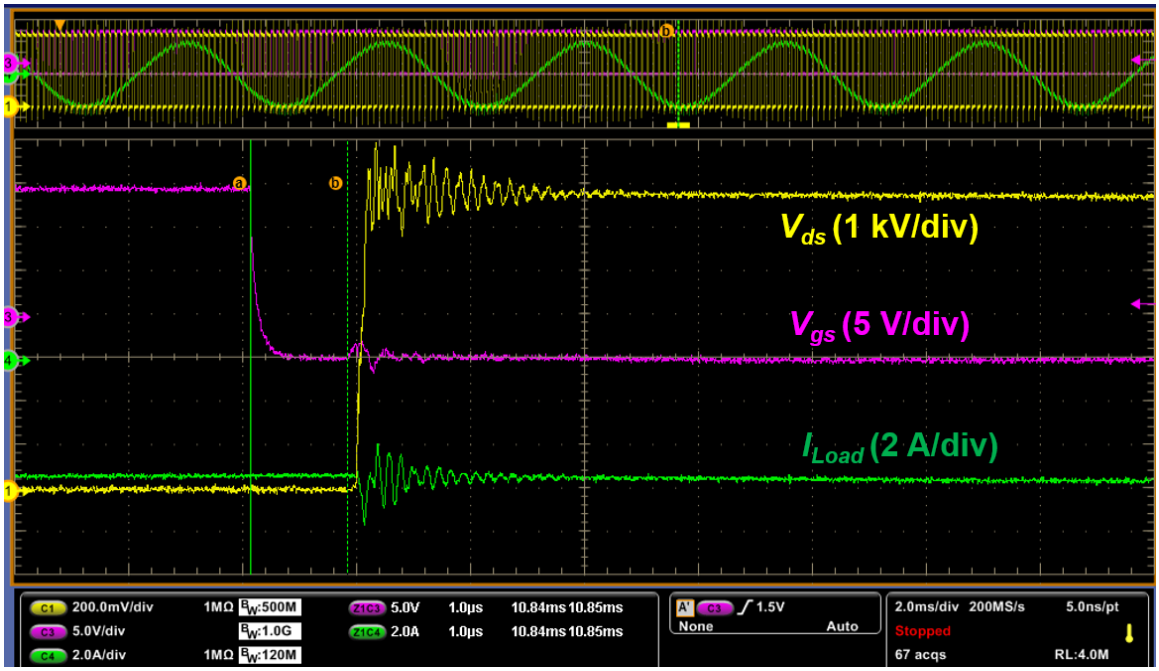


Fig. 3- 14. Zoom-in waveform of the continuous test of the phase leg at 6.5 kV.

3.4 Summary

Based on the discrete 10 kV/20 A SiC MOSFETs from Wolfspeed, the baseline design and test of the 6.5 kV half bridge phase leg are presented in this chapter. The designed gate driver fully utilizes the fast switching speed of 10 kV SiC MOSFETs and supports the continuous operation of the phase leg, with overcurrent protection, dead time function, and status feedback signal in every switching cycle. The feedback signal from the gate driver helps the controller monitor the status of the fiber optic communication and gate driver in every switching cycle.

Baseline testing procedures are developed to test the phase leg, including DPT, HSF short circuit test, and ac-dc continuous switching test. With strict sequence, the testing procedures are designed to endeavor to minimize the risk of device damage. Testing results show that the designed protection responds within 1.3 μs under the conventional short circuit conditions, and the peak current is lower than 10X rated current of the MOSFET. Yet the influence of a flashover fault is not considered in the baseline design and test. The continuous operation capability of the phase leg is validated by the continuous test at 6.5 kV as a half bridge inverter. In general, the HB phase leg presented in this chapter provides an ideal platform for the investigation and improvement covered in next chapters of this dissertation to make the phase leg more robust.

CHAPTER 4. SWITCHING PERFORMANCE EVALUATION

The parasitic capacitances in the power stage of 10 kV SiC MOSFET-based converters and their influence on the switching performance of the HB phase leg are investigated in this chapter. The baseline phase leg design in Chapter 3 is leveraged in the DPT setup for the switching performance evaluation. The parasitic capacitances are mainly caused by the heatsink, the anti-parallel SiC JBS diode, and the load inductor, as summarized in Fig. 4-1 [1]. In this chapter, the impact of the parasitic capacitances from the three sources on the switching behavior and performance will be evaluated in detail.

It should also be noted that part of the content in this chapter is from the author's Master's thesis [1]. In addition, some of the content in this chapter is from the author's conference paper published in *2018 IEEE WiPDA* [91]and the author's paper published in *2018 IEEE ECCE* [92].

The circuit diagram of a DPT setup based on the HB phase leg introduced in Chapter 3 is shown in Fig. 4-2. A large input capacitor is added in parallel with the dc-link capacitor to serve as the energy storage capacitor during the DPT. Before DPT, the dc-link voltage is charged to the desired voltage level by a 15 kV/800 mA high voltage dc power supply from Spellman. It is required that the negative terminal of the DC power supply is solidly grounded. Then, the power supply is shut down, so DPT is completed by using the energy stored in the dc-link capacitor C_{dc} and the input capacitor C_{in}. The two auxiliary power supplies for the gate driver board and the oscilloscope are grounded at the grounding point of the half bridge phase leg. A 100 kΩ resistor is inserted between the grounding point of the phase leg and the grounding point of the dc power supply, which makes the

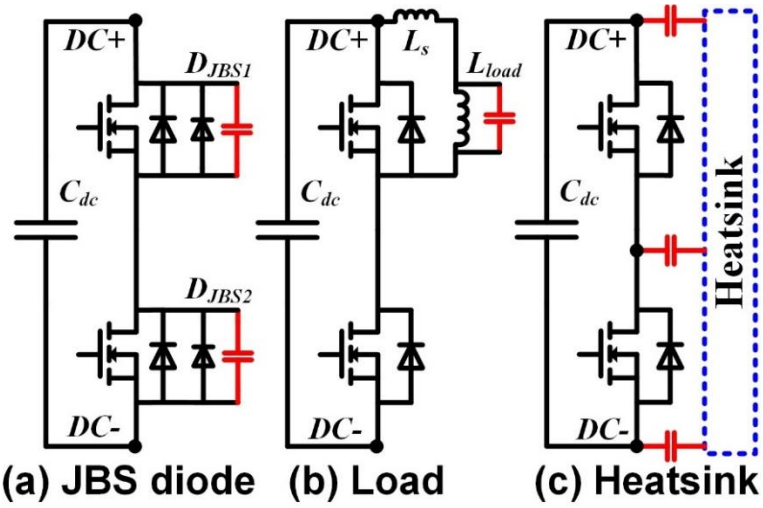


Fig. 4- 1. Three major sources of the parasitic capacitance in the power stage [1].

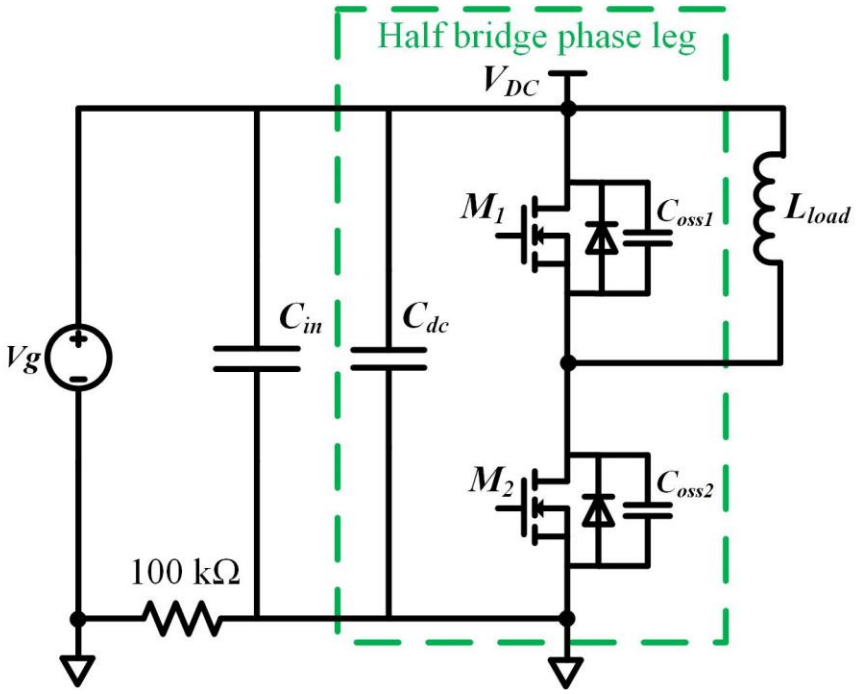


Fig. 4- 2. Circuit diagram of the DPT based on the designed half bridge phase leg.

DPT setup a single point grounded system during DPT.

The compact HB phase leg design poses a challenge to the accurate measurement of the fast switching transient of the drain current I_d and the drain-to-source voltage V_{ds} of the DUT, which is the lower device in the HB phase leg. The voltage measurement is conducted with a 75 MHz high voltage passive probe through Kelvin connection. Commercial Rogowski coil and current probe are the two current measurement methods commonly used in the DPT of high voltage SiC MOSFETs. The commercial Rogowski coil current transducer is preferable in the current measurement of the compact phase leg due to its flexibility, but it has a low bandwidth of 30 MHz. Also, the measurement results of Rogowski coil are easily interfered by fast switching transients with high *dv/dt* [71]. Therefore, a current probe (TCP0030A from Tektronix) is selected due to its higher bandwidth (120 MHz) and better noise immunity under high *dv/dt*. An additional wire is inserted in the power loop of the phase leg to accommodate the current probe, resulting in an increase of 72 nH in the power loop inductance. Table 6 summarizes the adopted measurement setup for the DPT. In addition, common mode chokes are used to suppress the impact of CM current on the measurement. The test setup together with the measurement setup can be seen in Fig. 4-3. The probes are connected with a high-speed oscilloscope on the top layer of the cabinet in which the high voltage test platform is established. The cabinet is solidly grounded at the grounding point of the phase leg.

4.1 Impact of Parasitic Capacitance in Load Inductor

The load inductor in practical applications has non-negligible equivalent parallel capacitance (EPC), hence introducing considerable parasitic capacitance in the converter.

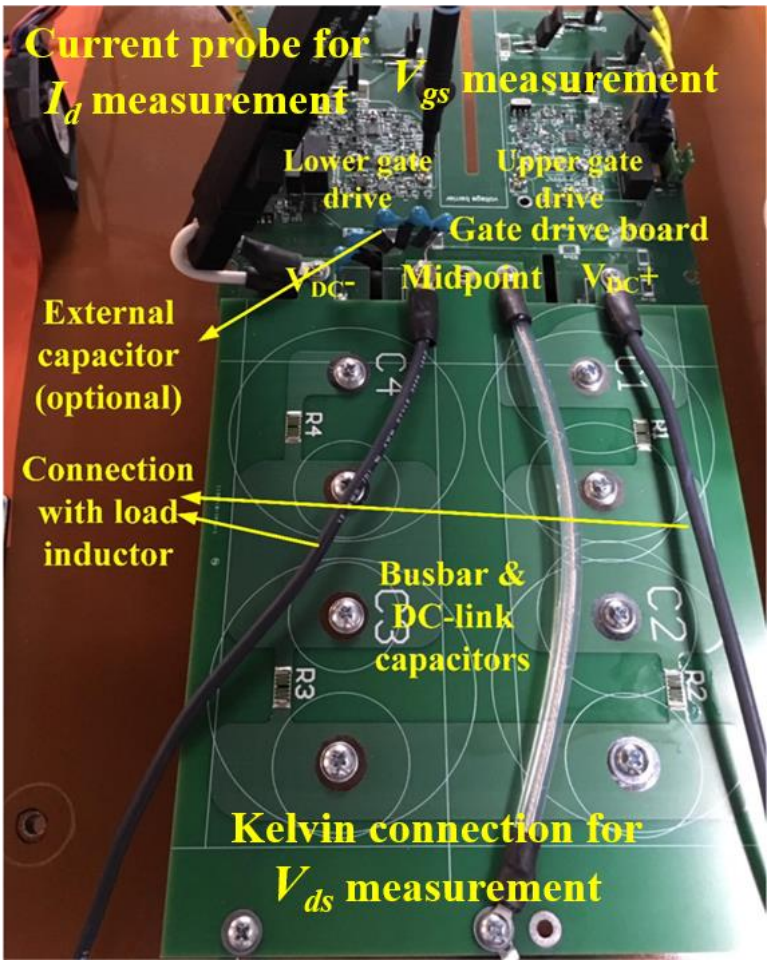


Fig. 4- 3. DPT test setup based on the designed half bridge phase leg together with measurement setup.

Table 6. Summary of the selected measurement setup for the DPT.

Measurement	**Drain current**	**Drain-to-source voltage**	**Gate-to-source voltage**
Probe	Tektronix TCP0030A	Tektronix P6015A	Tektronix TPP1000
Bandwidth	120 MHz	75 MHz	1 GHz

EPC of the load inductor is charged or discharged during the switching transients, and hence should not be neglected when investigating the switching performance. To evaluate the impact of EPC of the load inductor, an 85 mH inductor manufactured by Control Transformer for 15 kV distribution grid applications is used as the load inductor in the DPT setup, which passes the hipot test at 31 kV and can serve in practical MV applications. Keysight E4990A impedance analyzer shows that it has a parasitic EPC of 35.1 pF.

High voltage wire or cable is needed to connect the load inductor with the switching devices, bringing parasitics in series with the load. Usually the distance between the load and the switching devices of the MV converter is considerable. In the experimental setup, high voltage (15 kV) AWG 12 wire is used for the connection between the phase leg and the inductor, since the high voltage cable is expensive and not available in the laboratory. The high voltage wire with a length of 5.92 m in the DPT setup can be modeled as a 6.46 μH inductor in series with a small resistance, since its parasitic capacitance is negligible. The parasitic inductance L_s in Fig. 4-1 is thus 6.46 μH and should be considered in the analysis. MV converters for industrial applications use MV cables for the connection, which effectively increases EPC of load due to its shielding layer. In the DPT setup, the EPC of load inductor can be adjusted by adding the external EPC in parallel with the load inductor, as can be seen in Fig. 4-4. Two capacitors (27 pF and 106 pF) have been used to increase EPC of the load inductor. Considering MV cables' significant impact on EPC of load in practical converters, such increase in EPC by adding external capacitors is reasonable.

DPT results at 6.25 kV reveal that the larger parasitic EPC in the load inductor



Fig. 4- 4. High voltage load inductor with external capacitor to increase its EPC.

slows down both turn-on and turn-off transient of the 10 kV SiC MOSFET and results in higher total switching energy loss. The turn-on energy loss increases as the parasitic EPC of the load increases, while the turn-off energy loss decreases, as shown in the DPT results as load current varies from 4 A to 20 A in Fig. 4-5. Larger EPC in the load inductor results in higher total switching energy loss because the turn-on energy loss dominates. An increase of 106 pF in the EPC (4X EPC) results in 16% increase in total switching energy loss at 4 A and 11.1% increase at 20 A. As load current increases from 4 A to 20 A, the percentage increase in total switching energy loss becomes lower.

The increase in turn-on energy loss is mainly attributed to the increased current overshoot and longer voltage fall time during the turn-on transient. With increased EPC in the load inductor, a larger effective capacitance needs to be charged from 0 V to 6.25 kV during the turn-on transient. The current overshoot during the turn-on process of the 10 kV SiC MOSFET is higher, since its turn-on current overshoot is dominated by the charging current of parasitic capacitances in parallel with the synchronous device [57]. The longer voltage fall time leads to lower turn-on *dv/dt*, as indicated in Fig. 4-6. In the switching transient analysis, the *dv/dt* is calculated as the average *dv/dt* when V_{ds} of the MOSFET changes between 90% and 10% of the dc-link voltage.

Meanwhile, the turn-off energy loss decreases as EPC of the load inductor becomes larger. The turn-off transient becomes slower with longer voltage rise time if the load inductor has a larger EPC. In fact, the turn-off transient is slowed down more substantially than the turn-on transient. The drain current of DUT drops more quickly, and meanwhile its V_{ds} rises more slowly, as shown in the switching waveform in Fig. 4-7. The measured

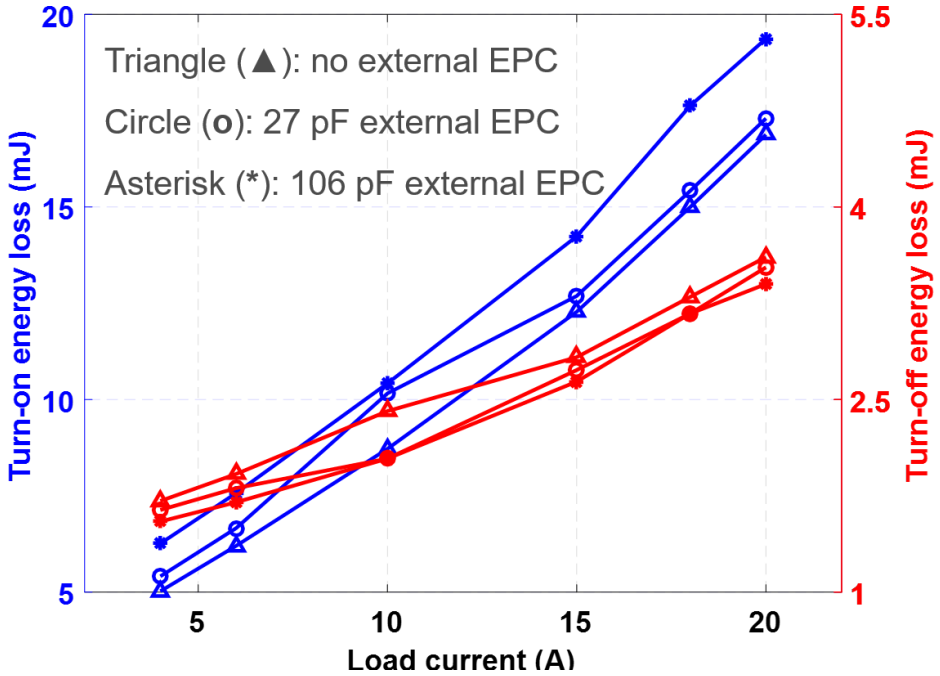


Fig. 4- 5. Turn-on and turn-off energy loss at 6.25 kV when load inductor has different EPCs.

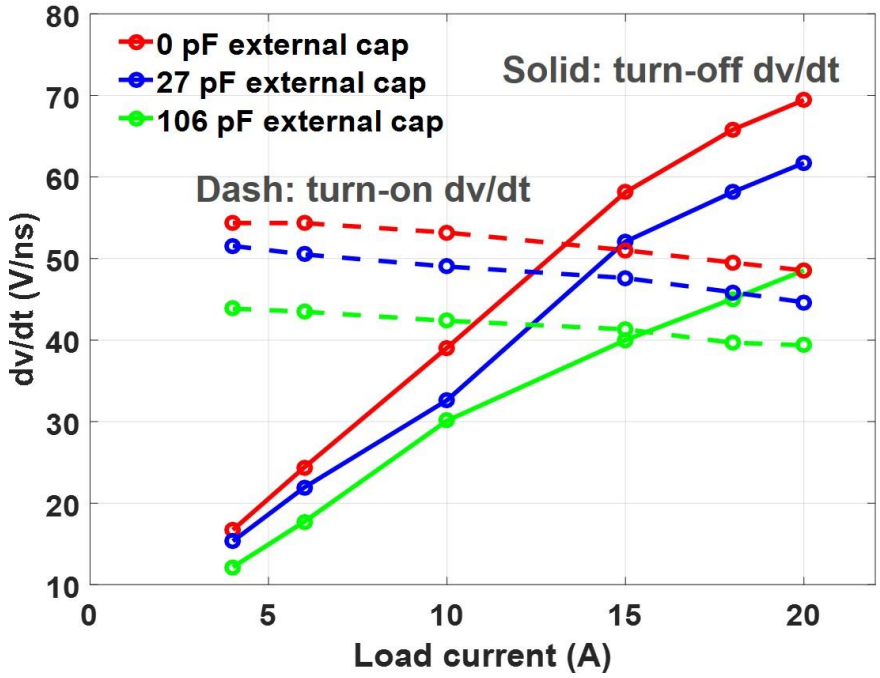


Fig. 4- 6. Turn-on and turn-off *dv/dt* at 6.25 kV when the load inductor has different EPCs.

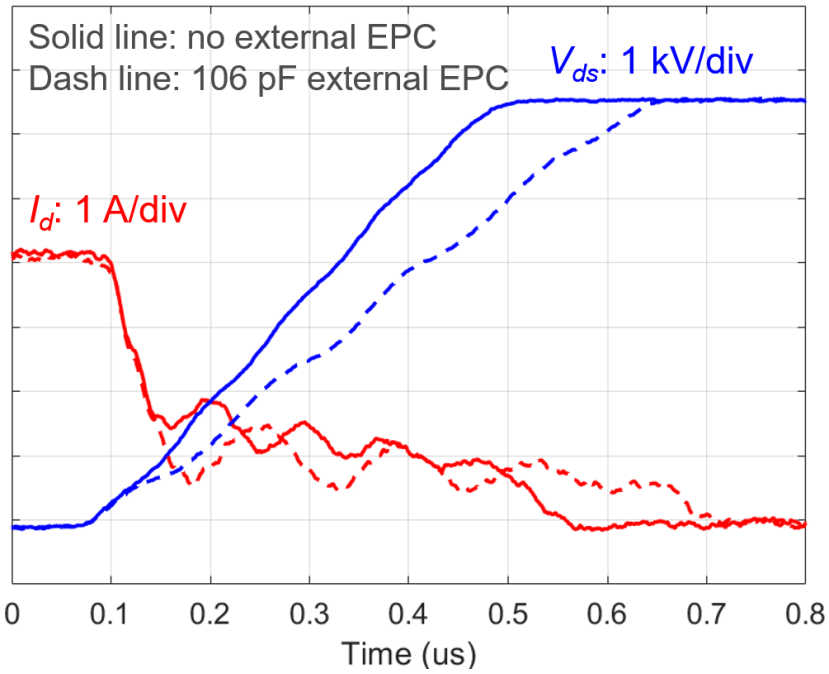


Fig. 4- 7. Turn-off transient waveform at 6.25 kV when load inductor has different EPCs.

turn-off loss of the 10 kV SiC MOSFET consists of the loss due to the overlap between V_{ds} and the channel current and the energy stored in the output capacitance of the DUT. The overlap loss decreases, while the energy stored in the capacitance remains the same. Therefore, the measured turn-off loss benefits from the increased EPC in the load inductor.

The switching transients are heavily shaped by the resonance between the parasitic inductance L_s and EPC of the load inductor, which results in considerable ringing in the load current during switching transients. The turn-off transient, particularly, is influenced which counts on the load current to charge the output capacitance of the DUT. The impact of the resonance on the turn-off transient is easily observed at lower load current when the turn-off time is longer (see Fig. 4-7). Drain current has significant ringing during the current fall time, resulting in the slight ringing in V_{ds}. The ringing is attributed to the considerable oscillation in the load current owing to the large L_s. At higher load current, the slew rate of V_{ds} changes dramatically during the turn-off transient, as can be seen in Fig. 4-8. The low instantaneous *dv/dt* period is caused by the slower discharge of the EPC in the load inductor and hence the negative *di/dt* in the load current. Then, the instantaneous *dv/dt* becomes high again since the load current rises as the resonance continues. Fig. 4-8 also illustrates that larger EPC in the load inductor leads to longer voltage rise time and lower average *dv/dt*, but the peak *dv/dt* is still almost the same.

In summary, the resonance between the parasitic inductance L_s and EPC brings oscillation in the load current and hence the ringing in V_{ds} and I_d, especially during the turn-off transient. Larger EPC in the load inductor results in higher turn-on energy loss, lower turn-off energy loss, and higher total switching energy loss. Higher EPC in the load also

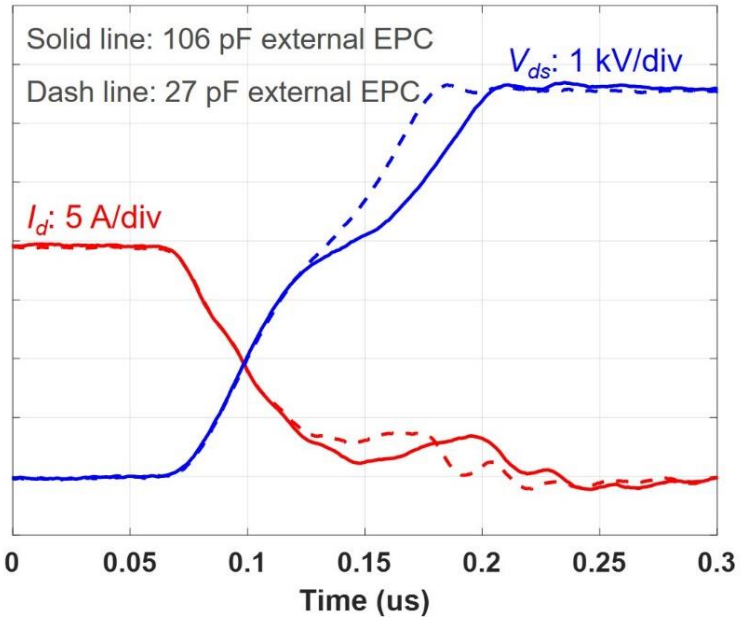


Fig. 4- 8. Turn-off transient waveform at 6.25 kV/20 A when the load inductor has different EPCs.

slows down both the turn-on and turn-off transient and reduces the average *dv/dt*, but it does not necessarily alleviate the peak *dv/dt* stress. In this case, both the peak *dv/dt* and the average *dv/dt* should be focused on in the switching performance evaluation.

4.2 Impact of Parasitic Capacitances Due to Heatsink

The heatsink is also able to cause non-negligible parasitic capacitances in the converter. Parasitic capacitances brought by the heatsink design and their impacts on the switching transients are complicated, depending on the heatsink design and grounding scheme of the heatsink [48], [93]. In this work, DPT is conducted in the phase leg with two different thermal designs to analyze the effect of the parasitic capacitance due to the heatsink on the switching performance of the 10 kV SiC MOSFET.

Two thermal designs have been implemented in the HB phase leg, as summarized in Fig. 4-9. Thermal design A with two separate heatsinks for two MOSFETs is the thermal design for the half bridge phase leg introduced in Chapter 3. The two heatsinks are not grounded, and their potentials follow the potential of the drain plate they are connected to. Thermal design B has only one grounded heatsink for the two MOSFETs. The thermal pad with high voltage insulation capability is added between the devices' drain plates and the grounded heatsink. Therefore, two considerable parasitic capacitances between the drain plate and the heatsink, C_{p1}, and C_{p2}, are generated. C_{p1} is in parallel with the lower MOSFET since its source is also grounded. C_{p2} between the dc-link and the ground can be neglected when analyzing the switching transients of the DUT. In terms of parasitic capacitance, thermal design A is a better design, in which the parasitic capacitance due to heatsink is too small to consider, yet the heatsink for the lower MOSFET has high *dv/dt*

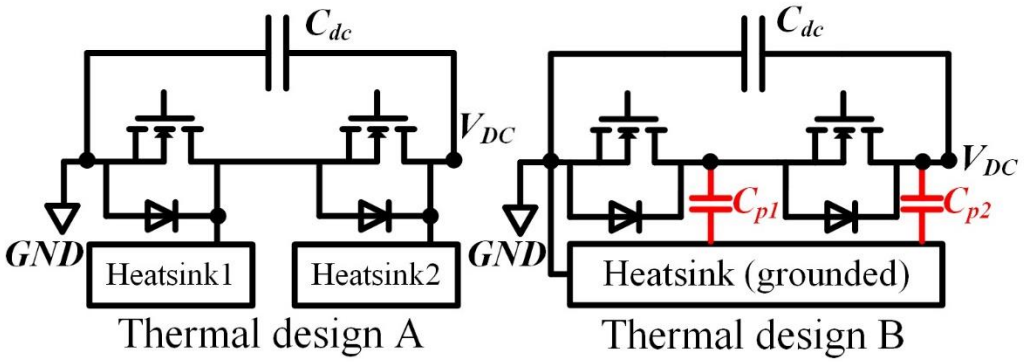


Fig. 4- 9. Two thermal designs implemented in the half bridge phase leg.

during switching transients. The parasitic capacitance between the two heatsinks in thermal design A is less than 0.3 pF.

In reality, the phase leg with thermal design B utilizes a grounded hotplate as the heatsink, and a 3.4 mm ceramic layer with 20.8 kV/mm insulation capability is placed between the MOSFETs and the grounded hotplate for insulation. The calculated capacitance of C_{p1} is 29.7 pF, which is small due to the thick ceramic layer. In fact, the parasitic capacitance is likely to be so small in MV converters using 10 kV SiC MOSFET power modules instead of the discrete device with the large drain plate. The thermal design can be easily switched between thermal design A and thermal design B. An air core inductor with single-layer winding is used as the load inductor to reduce the impact of parasitics from the load. Measurement setup for DPT is the same as Table 6.

DPT results at 6.25 kV show that the parasitic capacitance generated in thermal design B significantly slows down the turn-off transient and increases the turn-off loss. With thermal design B, the turn-off transient of the DUT is significantly slower with lower turn-off *dv/dt* and increased turn-off loss. The slower turn-off transient can be explained by the existence of C_{p1} which effectively increases the output capacitance of the DUT. A significant part of the measured turn-off loss of the 10 kV SiC MOSFET is the energy stored in the output capacitance of the DUT. Thus, as shown in Fig. 4-10, the increase in turn-off loss with thermal design B, ~0.65 mJ, is approximately the same as the energy stored in C_{p1} from 0 V to 6.25 kV. Since C_{p1} is small in the implemented phase leg with thermal design B, there is little difference in the turn-on transient of the DUT in the phase leg with thermal design A and thermal design B, as can be seen in Fig. 4-10 and Fig. 4-11.

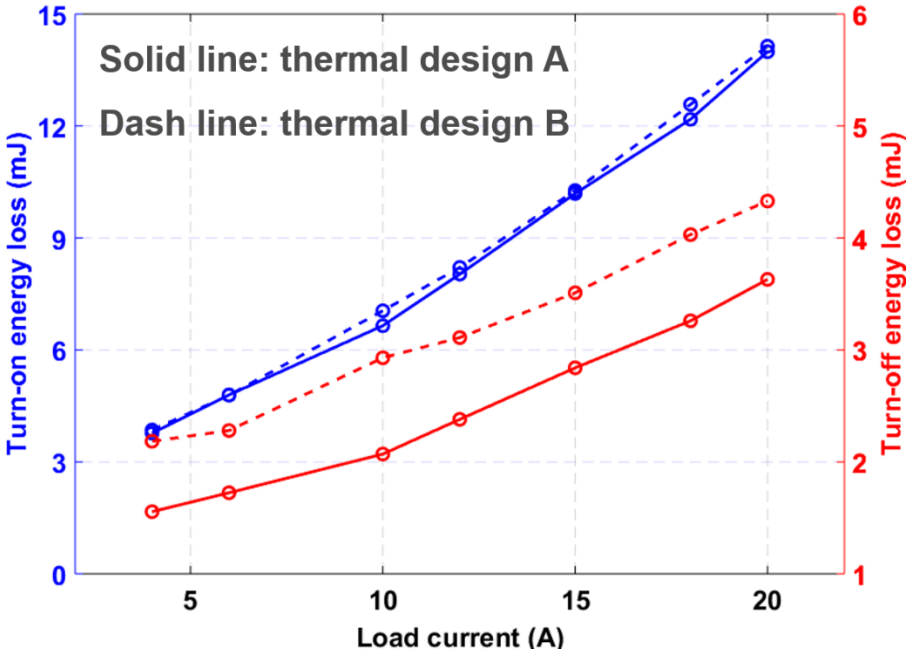


Fig. 4- 10. Comparison of turn-on and turn-off energy loss between the thermal design A and B at 6.25 kV.

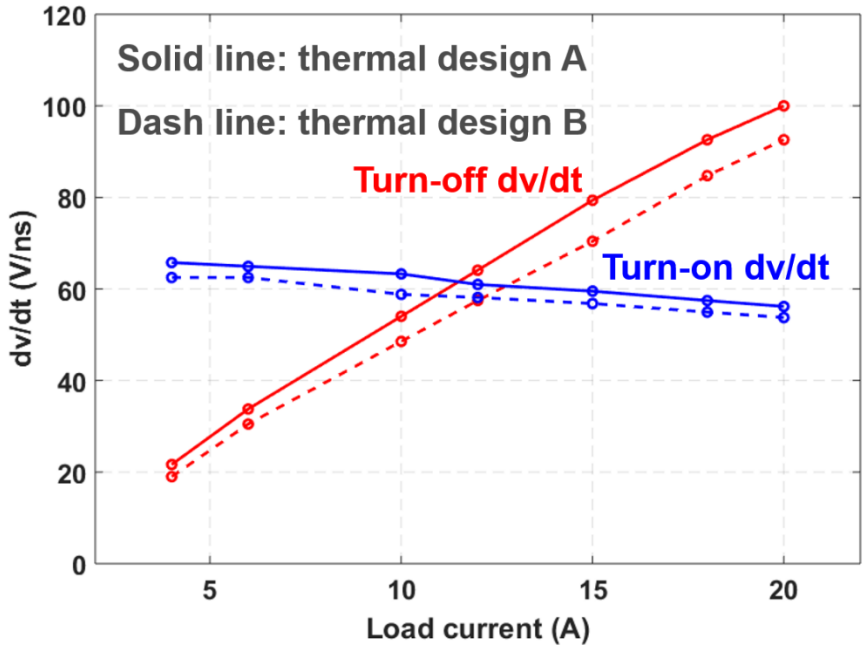


Fig. 4- 11. Comparison of turn-on and turn-off *dv/dt* between thermal design A and B at 6.25 kV.

With a 29.7 pF increase in the output capacitance of the DUT, the total switching energy loss at 6.25 kV increases by 13.4% at 4 A, and it only has 4.8% increase at 20 A load current. Therefore, thermal design A is a better design in terms of switching loss.

The large drain plate of the discrete 10 kV SiC MOSFET for heat extraction makes it easy to form large parasitic capacitances due to the heatsink. With thermal design B, C_{p1} could be larger than 29.7 pF since the thermal pad between the device and the heatsink is usually thinner than 1.5 mm for low thermal resistance. For instance, assuming the adoption of the insulated thermal pad SARCON 100X-m with a thickness of 1 mm, C_{p1} will be 53.9 pF. To investigate the influence of a larger C_{p1} caused by thermal design B, an external capacitor (106 pF) is added in parallel with the lower device in the phase leg with thermal design A, which is shown as the external capacitor in Fig. 4-3.

Test results show that a large parasitic capacitance caused by the thermal design B also slows down the turn-on transient and results in significantly increased switching energy loss. The influence of the external 106 pF capacitor on the switching performance of the DUT is summarized in Fig. 4-12. The switching energy loss and *dv/dt* data are normalized based on test results with thermal design A, which can be seen in Fig. 4-10 and Fig. 4-11. Typically the turn-on energy loss increases by ~10% after the 106 pF capacitor is added. Meanwhile, the total switching energy loss has a percentage increase of 44.5% and 20.1%, at 4 A and 20 A, respectively, which is mainly contributed by the increased turn-off loss. Hence, the total switching loss of the converter based on the discrete 10 kV SiC MOSFET increases by >20% if a 106 pF parasitic capacitance is introduced by the

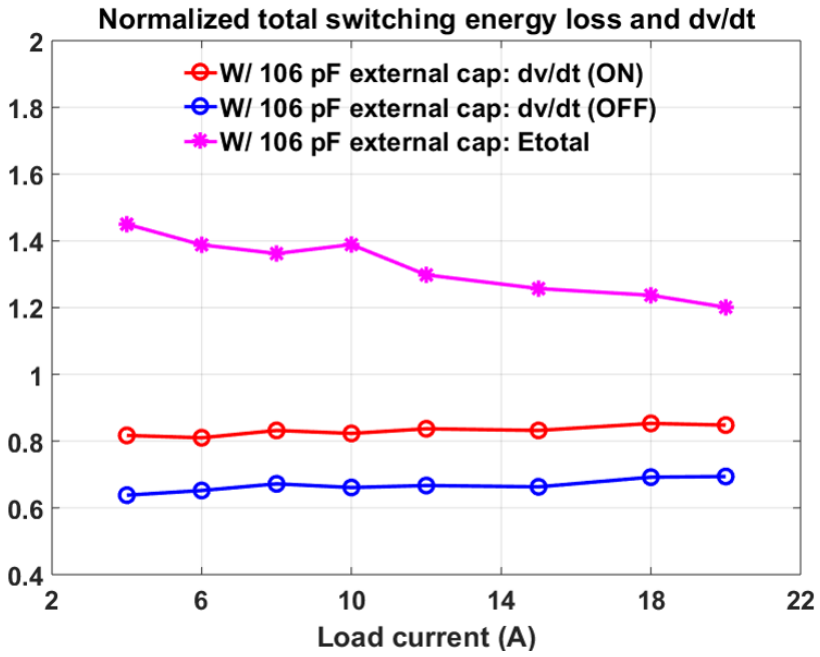


Fig. 4- 12. Impact of the 106 pF parasitic capacitance due to heatsink on the switching energy loss and *dv/dt* (Normalized based on data from thermal design A).

grounded heatsink. The impact of the considerable parasitic capacitance caused by thermal design B on the converter switching loss is more significant at light load.

4.3 Impact of Body Diode and Anti-parallel JBS Diode

In this section, the impact of the body diode and the anti-parallel JBS diode on the switching performance of the 3rd generation 10 kV SiC MOSFET from Wolfspeed (CPM3-10000-0350-ES) is investigated in detail at various junction temperatures. The 10 kV SiC MOSFET module with an anti-parallel JBS diode in each switch, as shown in Fig. 4-13, provides a suitable platform for the investigation. The switching performance of three device configurations for one switch is tested and compared, by which the impact of the body diode and the anti-parallel JBS diode can be quantitatively analyzed. The investigation can also guide the 10 kV SiC MOSFET based converter design in the selection of the freewheeling diode.

4.3.1 Device under Test and Experimental Setup

The 10 kV SiC MOSFETs are packaged in a module (H-bridge) by Danfoss Silicon Power, as displayed in Fig. 4-13. Each MOSFET in the module has a 10 kV/20 A anti-parallel SiC JBS diode (CPW3-10000-Z015B-ES from Wolfspeed). The detailed configuration of one switch in the module is drawn as Configuration A in Fig. 4-14. In addition to the 10 kV MOSFET and JBS diode, a low voltage Si Schottky diode is added in each switch which can prevent reverse current flowing through the body diode. Both the Schottky diode and JBS diode could be bypassed with a designed interface board. The body diode can handle the reverse current up to 20 A without any thermal issue, although its conduction loss is slightly higher than the JBS diode (11% higher at 15 A, 125 ˚C) [92].

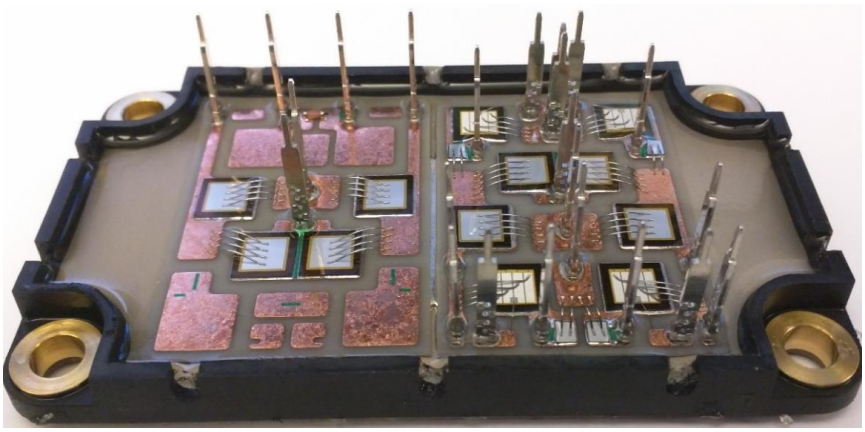


Fig. 4- 13. 10 kV SiC MOSFET module (H-bridge) packaged by Danfoss.

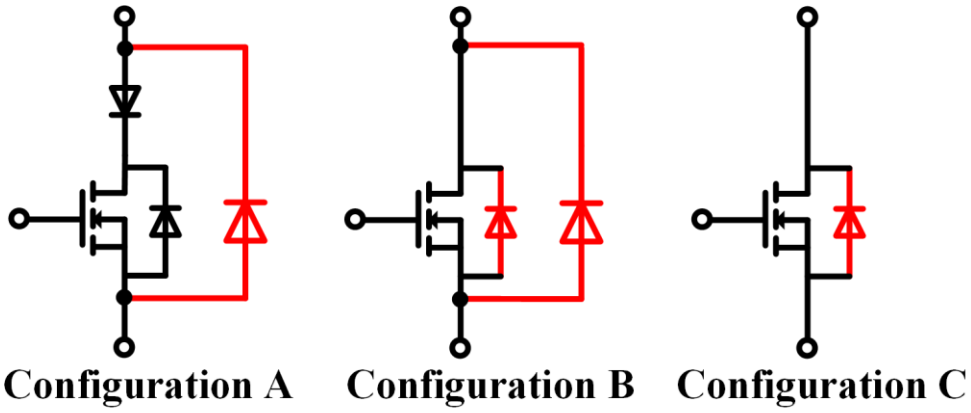


Fig. 4- 14. Three device configurations for one switch available in the 10 kV SiC MOSFET module.

The switching performance of three different device configurations can be tested, as shown in Fig. 4-14. The three device configurations have different combinations of freewheeling diodes during switching commutation. The diode in red serves as the freewheeling diode. For example, the current commutates between the channel of the MOSFET and the anti-parallel JBS diode in Configuration A, while the switching commutation occurs between the channel of the MOSFET and the body diode in Configuration C. With the high voltage DPT setup, the performance of different device configurations can be quantitatively compared, and the impact of the body diode and the anti-parallel JBS diode on the switching transients can be investigated in detail.

DPT setup is established for the switching performance investigation under various temperatures. The setup is similar to that introduced in Section 4.1, so only the differences are introduced. The 10 kV SiC MOSFET module is connected with the interface board and gate driver board through vertical pins. The Si Schottky diode and the anti-parallel JBS diode can be bypassed with the switches in the interface board [1]. Hence, the reconfiguration between different device configurations can be easily realized. The turn-on and turn-off gate resistance are 22 Ω and 11 Ω, respectively. The gate drive IC outputs 20 V/-5 V to drive the MOSFET. The grounded hotplate (H0909AA from Wenesco) under the module regulates the device junction temperature. A thermal pad is applied for electrical insulation between the module and the hotplate. The thermal pad also results in a temperature difference of several degree Celsius between the MOSFET and the hotplate. The temperature difference can be obtained and compensated with an offline test. The only difference in measurement setup is the drain current measurement with the Rogowski coil

(CWT Ultra mini from PEM). The compact module design makes it difficult to accommodate a high-bandwidth current probe to measure the drain current. When placing the Rogowski coil in the experimental setup, the positions close to the switch node with high *dv/dt* should be avoided [1]. The DPT setup can be seen in Fig. 4-15, in which the 10 kV SiC MOSFET module is placed between the gate driver board and the grounded hotplate.

Configuration C with only the body diode is suitable for the evaluation of the impact of the body diode on the switching performance. Switching performance of the phase leg with Configuration C from 25 ˚C to 125 ˚C is investigated. The turn-on energy loss decreases as the junction temperature increases, as shown in Fig. 4-16. This phenomenon is different from what has been reported in low voltage SiC MOSFETs [18], [52]. The body diode of the 1.2 kV SiC MOSFET causes a significant increase of turn-on energy loss at higher temperature due to the rapid increase of reverse recovery charge as temperature rises. As for the 10 kV SiC MOSFET, the switching loss decreases with the increasing temperature, indicating stable reverse recovery performance of the body diode as temperature changes. The current overshoot during the turn-on transient increases at higher temperature due to larger displacement current caused by higher *dv/dt*. Still, the faster switching speed and higher *dv/dt* makes the turn-on loss lower at higher temperature, as shown in Fig. 4-16 and Fig. 4-17. At 3 kV/20 A, the turn-on loss decreases by 16% as the junction temperature increases from 25 ˚C to 125 ˚C. For the 10 kV SiC MOSFET, utilizing the body diode as freewheeling diode leads to lower switching energy loss as temperature rises.

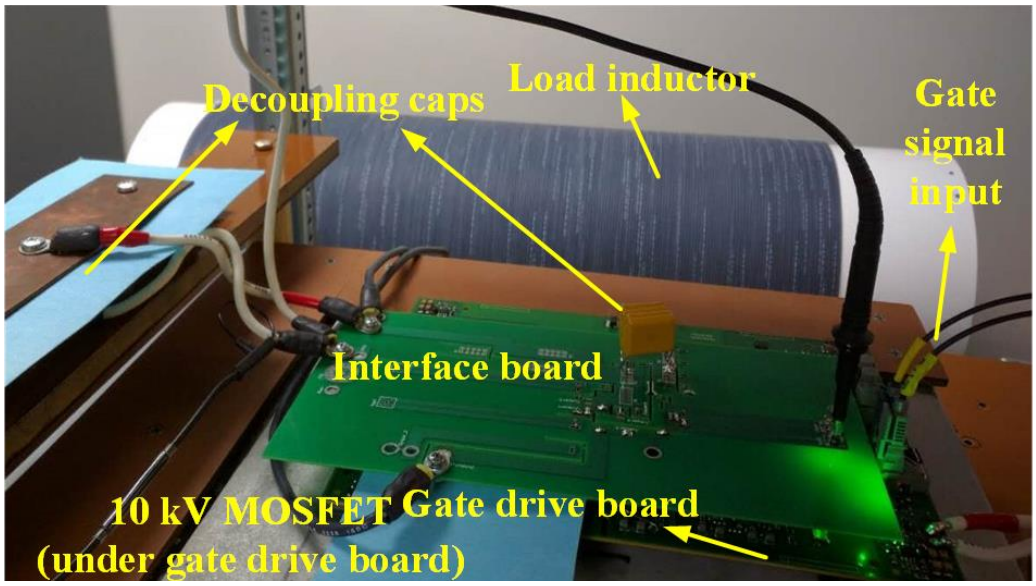


Fig. 4- 15. Picture of DPT setup to evaluate the impact of body diode and anti-parallel JBS diode.

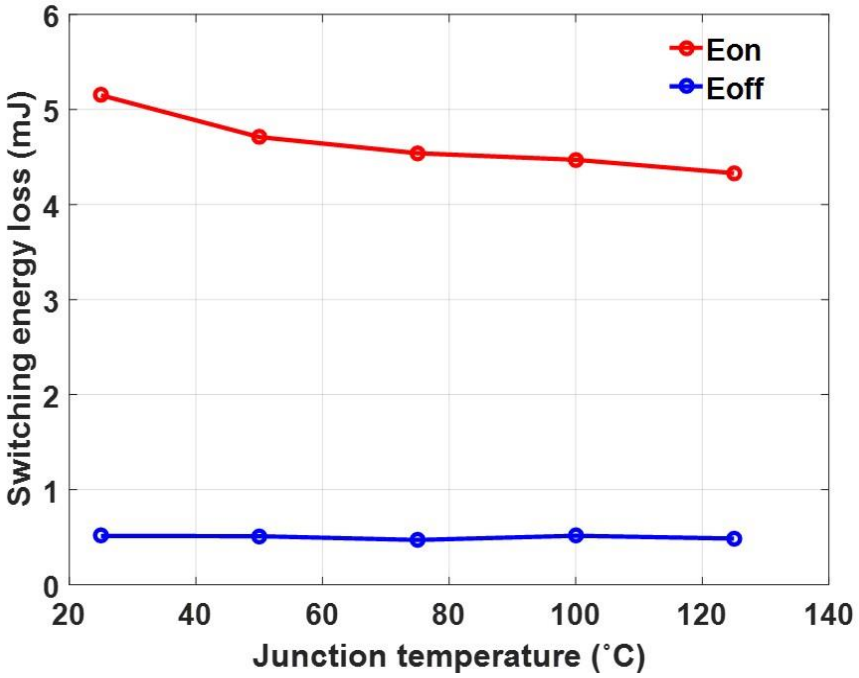


Fig. 4- 16. Switching energy loss vs. temperature (Configuration C, 3 kV/20 A).

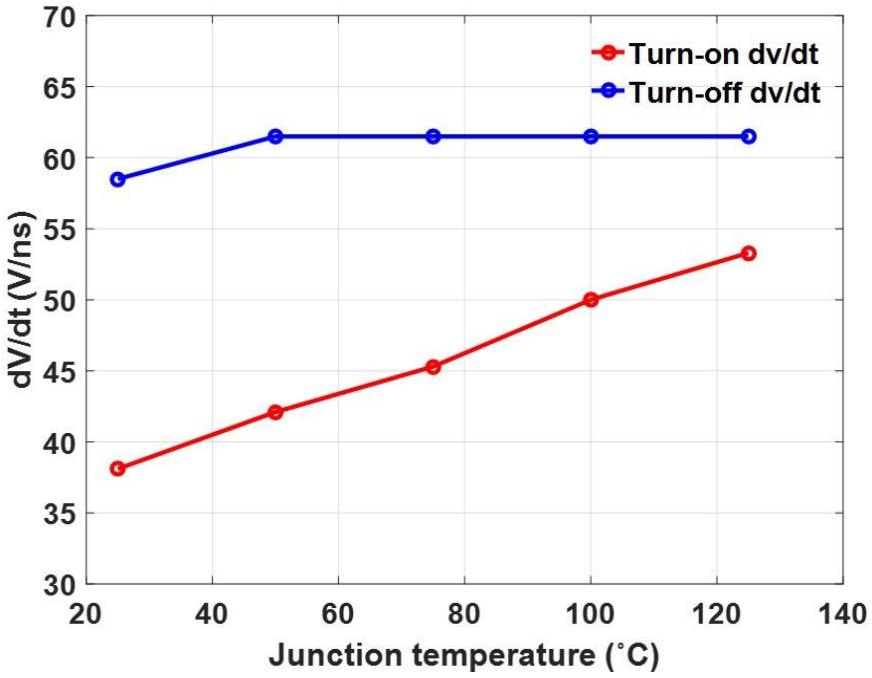


Fig. 4- 17. Turn-on and turn-off *dv/dt* vs. temperature (Configuration C, 3 kV/20 A).

Switching performance comparison of Configuration A and B affirms that the reverse recovery of the body diode has little impact on the switching transients of the DUT. Experimental results show that the switching performance of Configuration A is almost the same as that of Configuration B, as shown in data obtained at 3 kV and 125 ˚C in Table 7. Detailed switching transients displayed in Fig. 4-18 also indicate the almost identical switching performance between Configuration A and B, which is tested at 75 ˚C. Since Configuration A and B have almost the same switching performance, the reverse recovery performance of the body diode is almost as good as that of the JBS diode. Considering the nearly zero reverse recovery charge of the SiC JBS diode [53], the reverse recovery of the body diode of the 10 kV SiC MOSFET is also negligible.

The excellent reverse recovery performance of the body diode is originally due to the negligible minority carrier injection in on-state of the body diode. Output characteristic of the body diode indicates the impact of excess carrier injection and its reverse recovery performance. When the body diode has large on-state current, the conductivity modulation due to injection of excessive minority carriers effectively reduces the resistance of the body diode, but also results in reverse recovery current since they should be swept out during the turn-off transient. Therefore, the minority carrier injection and reverse recovery of the body diode can be evaluated by investigating the on-resistance of the body diode as a function of the on-state current. Table 8 lists the measured resistance of the body diode as a function of the conduction current at different temperatures, based on measured output characteristic of the body diode. At 125 ˚C, the body diode resistance only drops by 6.67% as current increases from 5 A to 25 A. Resistance of the body diode is almost a constant as

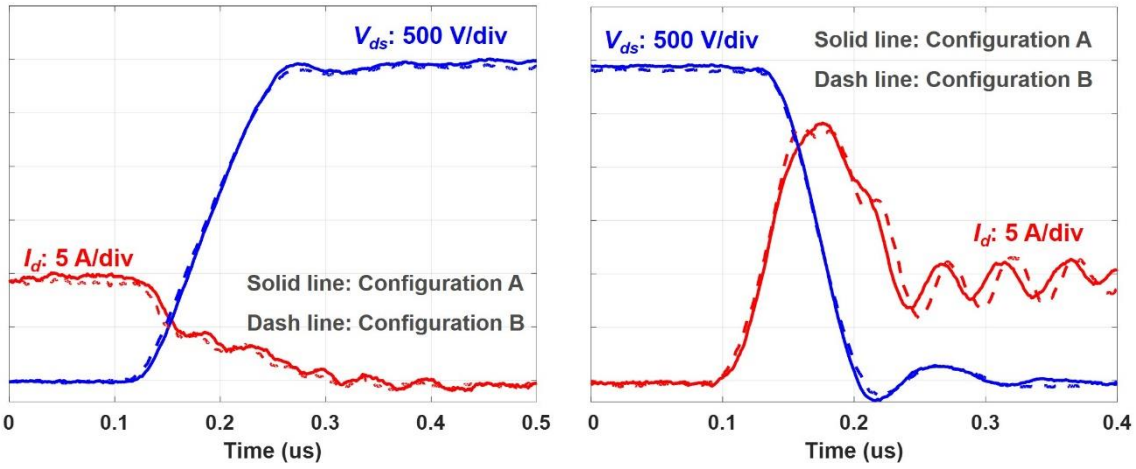


Fig. 4- 18. Switching transient waveforms of Configuration A and B at 75 ˚C (3 kV, 10 A).

Table 7. Switching performance of Configuration A and B at 3 kV, 125 ˚C.

Load current	Parameter	Configuration A	Configuration B
10 A	*dv/dt* (OFF)	22.6 V/ns	22.0 V/ns
	Loss (OFF)	0.76 mJ	0.72 mJ
	dv/dt (ON)	54.5 V/ns	50.0 V/ns
	Loss (ON)	2.71 mJ	2.87 mJ
20 A	*dv/dt* (OFF)	48.0 V/ns	46.1 V/ns
	Loss (OFF)	0.76 mJ	0.82 mJ
	dv/dt (ON)	51.1 V/ns	49.0 V/ns
	Loss (ON)	4.06 mJ	4.49 mJ

Table 8. Measured resistance of body diode at different temperatures.

Current	**5 A**	**10 A**	**15 A**	**20 A**	**25 A**
Resistance of body diode at 25 ˚C	372.3 mΩ	352.2 mΩ	342.5 mΩ	337.2 mΩ	335.9 mΩ
Resistance of body diode at 75 ˚C	549 mΩ	530 mΩ	513.7 mΩ	508 mΩ	504.4 mΩ
Resistance of body diode at 125 ˚C	741 mΩ	722 mΩ	709.6 mΩ	697.7 mΩ	691.6 mΩ

the current increases, indicating the slight impact of excess carrier injection. It can be concluded that the body diode of the 3rd generation 10 kV SiC MOSFET has excellent reverse recovery performance over a wide temperature range.

4.3.3 Impact of Anti-parallel JBS Diode

In terms of the switching performance, outcomes of adding external anti-parallel SiC JBS diode are studied to provide a guideline for MV converter design. Configuration B is achieved by adding an anti-parallel JBS diode in Configuration C. The effect of adding a 10 kV anti-parallel JBS diode is hence analyzed with the comparison of the switching performance between Configuration B and C.

Fig. 4-19 shows the switching transient waveforms of the phase leg based on Configuration B and C at 3 kV/20 A, 125 ˚C. Configuration C without anti-parallel diode during turn-off has higher *dv/dt*, shorter turn-off time, and lower measured turn-off energy loss. Meanwhile, adding external anti-parallel JBS diode only has slight impact on the turn-on transient. Table 9 illustrates the impact of the anti-parallel JBS diode on the switching performance of the 10 kV SiC MOSFET at different temperatures tested at 3 kV/20 A, including *dv/dt* and switching energy loss. The anti-parallel diode also increases the turn-on energy loss slightly. The turn-off transient is significantly slower after adding the anti-parallel JBS diode, leading to about 70% increase in turn-off energy loss. At 25 ˚C and 75 ˚C, the total switching energy loss increases by 8.6% and 13.6% at 3 kV/20 A, respectively, after adding the JBS diode. In terms of the switching performance, adding the anti-parallel diode increases the switching loss of the 10 kV SiC MOSFET and significantly slows down its turn-off transient.

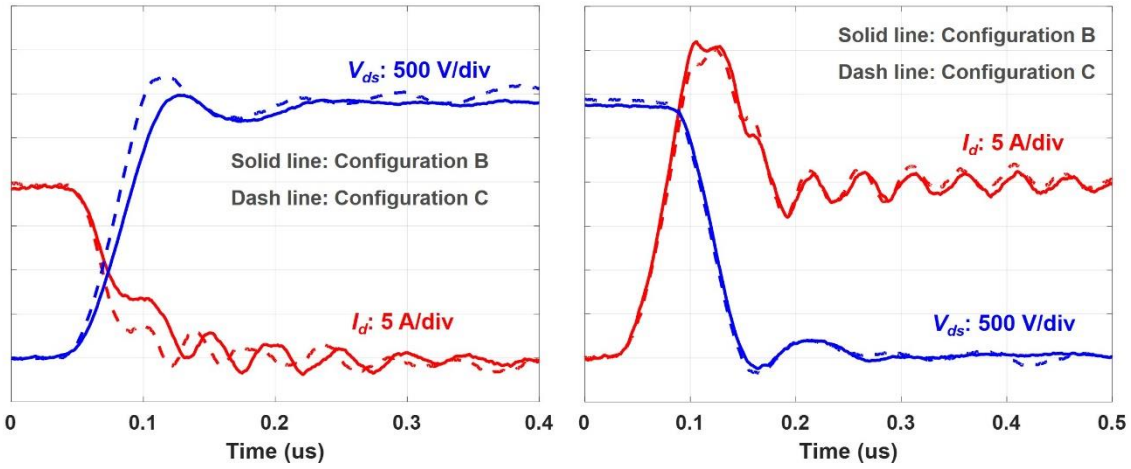


Fig. 4- 19. Switching transient waveforms of Configuration B and C at 125 ˚C.

Table 9. Switching performance comparison between Configuration B and Configuration C at 3 kV/20 A.

Configuration	**Parameter**	**At 25 ˚C**	**At 75 ˚C**	**At 125 ˚C**
Configuration B (W/ anti-parallel JBS diode)	*dv/dt* (OFF)	48 V/ns	48 V/ns	46.15 V/ns
	Loss (OFF)	0.83 mJ	0.83 mJ	0.824 mJ
	dv/dt (ON)	36.2 V/ns	46.2 V/ns	48.98 V/ns
	Loss (ON)	5.32 mJ	4.86 mJ	4.49 mJ
Configuration C (W/O anti-parallel JBS diode)	*dv/dt* (OFF)	57.14 V/ns	60 V/ns	58.54 V/ns
	Loss (OFF)	0.513 mJ	0.47 mJ	0.485 mJ
	dv/dt (ON)	35.82 V/ns	45.3 V/ns	50 V/ns
	Loss (ON)	5.15 mJ	4.54 mJ	4.33 mJ

The external anti-parallel JBS diode influences the reverse recovery and adds a nonlinear capacitor across the drain and source of the MOSFET, from the perspective of the switching performance evaluation. The body diode of the tested 10 kV SiC MOSFET has excellent reverse recovery performance over a wide temperature range. The benefit of JBS diode in the reverse recovery is thus negligible. Then, in the switching transient analysis, adding the anti-parallel JBS diode can be modeled by adding a nonlinear capacitor in parallel with the MOSFET. The nonlinear capacitor introduced by the anti-parallel JBS diode has an equivalent capacitance of 64.97 pF in terms of the energy at 3 kV [92].

With the anti-parallel JBS diode, the added nonlinear capacitor slows down the turn-off transient, which is dominated by the capacitive charging process. The increase in the output capacitance of the device results in longer voltage rise time and lower turn-off *dv/dt*. The measured turn-off loss increases since the parasitic capacitance caused by the anti-parallel diode also stores energy during the turn-off transient, which will be dissipated in the channel during the next turn-on transient in hard-switching condition. The energy stored in the output capacitance of the JBS diode at 3 kV is calculated as follows.

$$E_{JBS,3kV} = \int_0^{3kV} C_{JBS} v \, dv = 0.292 \, mJ \tag{4.1}$$

The energy stored in the output capacitance of the JBS diode is only slightly lower than the increased turn-off loss after adding the anti-parallel diode.

In terms of the turn-on transient, the influence of the nonlinear capacitance caused by the anti-parallel diode is limited. The turn-on transient is mainly influenced by gate driver parameters and temperature [44], [45]. The added nonlinear capacitance is not the dominant factor during the voltage fall time. The larger output capacitance of the MOSFET

due to the anti-parallel diode results in higher current overshoot during the turn-on transient. As shown in Fig. 4-19, Configuration B with the anti-parallel JBS diode has slightly higher current spike because of larger output capacitance and displacement current. Thereby, the turn-on energy loss is also slightly higher after adding the anti-parallel JBS diode, as can be seen in Table 9.

4.4 Summary

The HB phase leg prototype developed with the baseline design in Chapter 3 has been utilized to perform DPT to study the impact of the parasitic capacitances in the MV converter on the switching performance of 10 kV SiC MOSFETs.

Higher EPC in the load inductor makes both the turn-on and turn-off transient slower, leading to increased total switching energy loss. An increase of 106 pF in EPC (4X EPC) results in 16% increase in total switching energy loss at 4 A and lower percentage increase (11%) at 20 A. The detailed impact on *dv/dt* is also studied, which is a more important parameter in MV converters, compared to low voltage converters. The parasitic inductance in series with the load causes ringing during the switching transients, especially the turn-off transient. As a result, higher EPC in the load inductor reduces the average *dv/dt*, but not necessarily reduces the peak *dv/dt*.

When designing a SiC-based MV converter, the EPC of the load inductor should be minimized, which will increase the switching loss and cannot be counted on to reduce the peak *dv/dt* stress. Meanwhile, the influence of the EPC on the switching loss and *dv/dt* should be considered in gate driver design and loss calculation. Because the average *dv/dt*

can be different from the peak *dv/dt* due to the EPC and other parasitics, both the peak *dv/dt* and the average *dv/dt* should be examined when designing the gate driver.

Two different thermal designs bringing different parasitic capacitances have been implemented in the phase leg. The 106 pF parasitic capacitance that could be caused by the grounded heatsink, slows down both turn-on and turn-off transient significantly, leading to around 40% increase in total switching energy loss when load current is lower than 10 A. In terms of switching loss, the best heatsink design for the 10 kV SiC MOSFET with non-isolated package is to have a floating heatsink for each MOSFET, in order to minimize the resulting parasitic capacitance. At the converter level, parasitic capacitances result in higher percentage increase in switching loss when converter operates at lighter load.

The influence of the body diode and the anti-parallel SiC JBS diode on the switching performance of the 10 kV SiC MOSFET is also investigated in detail. The investigation and analysis are based on experimental results of three different device configurations of one semiconductor switch with different freewheeling diodes. The reverse recovery of the body diode is negligible at various temperatures. Using its body diode as the freewheeling diode, the 10 kV SiC MOSFET has lower switching loss as junction temperature rises. Adding the anti-parallel JBS diode does not benefit the reverse recovery performance and introduces additional parasitic capacitance, which increases the switching loss (>8.6% at 3 kV/20 A) and significantly slows down its turn-off transient. The body diode has satisfactory reverse recovery performance and conduction characteristic at different temperatures to serve as the freewheeling diode for the 10 kV SiC MOSFET.

CHAPTER 5. ANALYSIS AND GATE DRIVER CONSIDERATIONS OF 10 KV SIC MOSFETS UNDER FLASHOVER FAULT

The short circuit performance of 10 kV SiC MOSFETs under HSF and FUL has been investigated [59]. Nonetheless, it is also essential to study the behavior of 10 kV SiC MOSFETs under a flashover fault, the most serious type of short circuit fault in MV converters [37]. In fact, a flashover fault can be regarded as the most extreme case of FUL with exceptionally fast transients (>1 kV/ns dv_{ds}/dt and >30 A/ns di/dt).

The flashover fault poses a great threat to the 10 kV SiC MOSFET already in ON state [37]. When a flashover fault happens, the MOSFET that is already in ON state should be protected from damage, unless the insulation inside its own package fails. A detailed and comprehensive analysis of 10 kV SiC MOSFETs under a flashover fault is necessary for protection design and survival of the MOSFET from a flashover fault.

This chapter focuses on the analysis of 10 kV SiC MOSFETs under a flashover fault to provide guidelines for gate driver design from the perspective of the flashover fault. A simplified model of a 10 kV SiC MOSFET is established, with the focus on its behavior in the active region. Both 10 kV SiC MOSFETs with and without Kelvin source are analyzed in terms of their behavior under a flashover fault, and gate driver design considerations are discussed accordingly. Section 5.4 compares the energy loss generated by a flashover fault and HSF as well as FUL fault and discusses the protection design, followed by the summary of this chapter.

It should also be mentioned that part of the content in this chapter is from the author's conference paper published in *IEEE ECCE 2020* [94].

5.1 Model of 10 kV SiC MOSFET

The 10 kV SiC MOSFET investigated in this chapter is the 3rd generation 10 kV SiC MOSFET from Wolfspeed [29]. The 10 kV/20 A SiC MOSFET with only one die is studied as an example, as shown in Fig. 3-1. Power modules with higher current rating are realized by paralleling multiple dies with 20 A current rating. In order to study the behavior of 10 kV SiC MOSFETs under a flashover fault, a simplified model of the 10 kV/20 A SiC MOSFET is established. Fig. 5-1 displays the equivalent circuit of the MOSFET model.

The established model of a 10 kV SiC MOSFET is based on the classic quadratic model of a MOSFET [95] and the model in [44]. The 10 kV SiC MOSFET model is composed of two parts, which model the bare die and the package, respectively. As shown in Fig. 5-1, components inside the red box are used to model the bare die. The MOSFET channel is modeled with a controlled current source dependent on internal gate-to-source voltage $V_{gs,int}$, gate threshold voltage $V_{g,th}$, transconductance factor k_p, and internal drain-to-source voltage $V_{ds,int}$. The channel current i_{ch} is always zero when the MOSFET operates in cutoff mode.

$$i_{ch} = 0 \left(V_{gs,int} - V_{g,th} < 0\right) \tag{5.1}$$

In the ohmic region, where $V_{gs,int} - V_{g,th}$ is higher than $V_{ds,int}$, $V_{ds,int}$ increases as channel current rises, which can be described with the following equation.

$$i_{ch} = k_p \left[\left(V_{gs,int} - V_{th}\right)V_{ds,int} - \frac{{V_{ds,int}}^2}{2}\right] \tag{5.2}$$

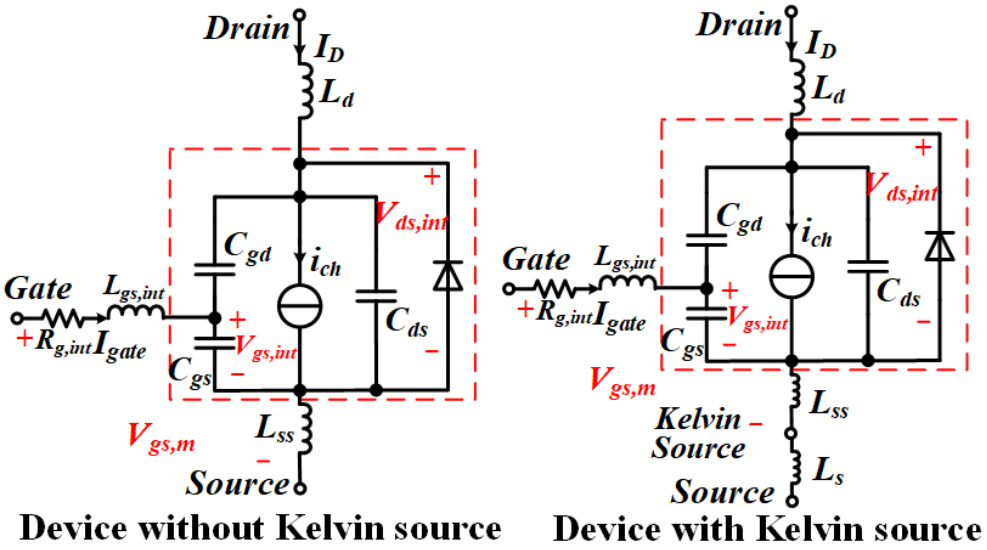


Fig. 5- 1. Equivalent circuit of the established 10 kV SiC MOSFET model.

As $V_{ds,int}$ keeps increasing and exceeds $V_{gs,int} - V_{g,th}$, which is still higher than 0 V, the MOSFET operates in the active region, and the channel current will gradually saturate, as described in (5.3).

$$i_{ch} = \frac{k_p}{2}\left(V_{gs,int} - V_{g,th}\right)^2 \tag{5.3}$$

Gate threshold voltage $V_{g,th}$ of the 10 kV SiC MOSFET is a function of junction temperature and $V_{ds,int}$, but it is dominated by $V_{ds,int}$ as $V_{ds,int}$ keeps increasing in the active region due to the short channel effect [96]. Higher $V_{ds,int}$ reduces $V_{g,th}$ and hence leads to higher saturation current of the channel, based on (5.3). k_p can be extracted with a curve tracer, and it is almost independent of junction temperature.

In the established model of the MOSFET channel, k_p is 2.02 A/V^2. $V_{g,th}$ is a function of junction temperature and the internal drain-to-source voltage $V_{ds,int}$. Considering the extremely fast transient during the flashover fault, the junction temperature indeed soars rapidly to eventually over 400 ˚C, so the impact of initial junction temperature before the flashover fault is negligible. The influence of initial junction temperature is hence neglected to simplify the model. As $V_{ds,int}$ increases, the depletion layer becomes thicker leading to decreased $V_{g,th}$. Once $V_{ds,int}$ exceeds 4 kV, the depletion layer starts to occupy the N+ substrate region, and its thickness saturates, so $V_{g,th}$ remains the same as long as $V_{ds,int}$ is higher than 4 kV. According to [59], the saturation current increases with a coefficient of 0.111/kV as $V_{ds,int}$ rises from 500 V to 4000 V. When $V_{ds,int}$ is lower than 500 V, $V_{g,th}$ is 2.85 V in the MOSFET model in this chapter, which is the extracted $V_{g,th}$ at 125 ˚C. Based on (5.3) and the saturation current at different $V_{ds,int}$, the gate threshold voltage at different $V_{ds,int}$ from 500 V to 4 kV can be calculated accordingly.

Also, base resistance R_{base} due to the thick N- base region is not considered since it models the N- base resistance when the MOSFET operates in the ohmic region. When the MOSFET stays in the active region, the impact of N- base region is considered by the channel model with short channel effect and the nonlinear C_{ds} model. The body diode is modeled with a resistor in series with its forward voltage drop, based on the measured I-V characteristic.

Parasitic capacitances of the 10 kV SiC MOSFET are also modeled based on extracted data with the curve tracer. Gate-to-source capacitance C_{gs} is modeled with a linear capacitor of 5.4 nF. Both gate-to-drain capacitance C_{gd} and drain-to-source capacitance C_{ds} are a nonlinear function of the internal drain-to-source voltage $V_{ds,int}$. Both C_{ds} and C_{gd} are realized by a variable capacitor model, which is determined by a look-up table established with the curve tracer data. The look-up table should include as many data points as possible, especially in the highly nonlinear region where C_{gd} and C_{ds} decrease dramatically as $V_{ds,int}$ rises slightly. The parasitic capacitance in parallel with C_{ds} contributed by such external components as heatsinks is not considered in this chapter.

Internal module parasitics of the MOSFET package should also be carefully modeled. So, the model for the MOSFET with and without Kelvin source is slightly different in Fig. 5-1. Common source inductance L_{ss} is 1 nH for discrete 10 kV SiC MOSFETs without Kelvin source [6]. With a Kelvin source, L_{ss} can be reduced drastically, and L_s represents the parasitic inductance in the source terminal that is exclusively in the power loop. L_d is the parasitic inductance in the drain terminal. Internal gate resistance $R_{g,int}$ (2 Ω) and internal gate loop inductance $L_{gs,int}$ (1 nH) model the parasitic resistance and

inductance in the gate loop inside the device package, which are caused by mechanical connectors, the bond wire, etc. L_d and L_s typically have negligible impact on the short circuit performance of the 10 kV SiC MOSFET, since it only increases the power loop inductance slightly. Nonetheless, L_d, L_s, and L_{ss} result in the difference between the internal drain-to-source voltage $V_{ds,int}$ and the measured drain-to-source voltage $V_{ds,m}$. In fact, L_{ss}, together with $R_{g,int}$ and $L_{gs,int}$ also makes the measured gate-to-source voltage $V_{gs,m}$ different from the internal gate-to-source voltage $V_{gs,int}$.

5.2 10 kV SiC MOSFET under Flashover Fault

In this section, the 10 kV SiC MOSFET under a flashover fault is analyzed with the circuit model in Fig. 5-2, which models a typical flashover fault in a HB phase leg. The flashover fault happens when the low-side MOSFET under investigation is already turned on. In order to model the insulation breakdown, the ideal switch, high-side switch in the phase leg, is shorted and generates the flashover fault [37]. Due to the extremely high *di/dt* in the power loop, common source inductance L_{ss} plays an essential role in the behavior of the 10 kV SiC MOSFET under a flashover fault. Therefore, both the 10 kV SiC MOSFET with Kelvin source and without Kelvin source are evaluated in this section.

5.2.1 Flashover Fault and Simulation Model

The flashover fault due to insulation failure in MV converters can be devastating because of its extremely fast dynamics. The circuit model used to simulate a flashover fault is shown in Fig. 5-2. According to simulation and experimental results in [37], generating a flashover fault by closing an ideal switch in the phase leg is a valid method to simulate a flashover fault, and it is not necessary to add more parasitics in the ideal switch. In this

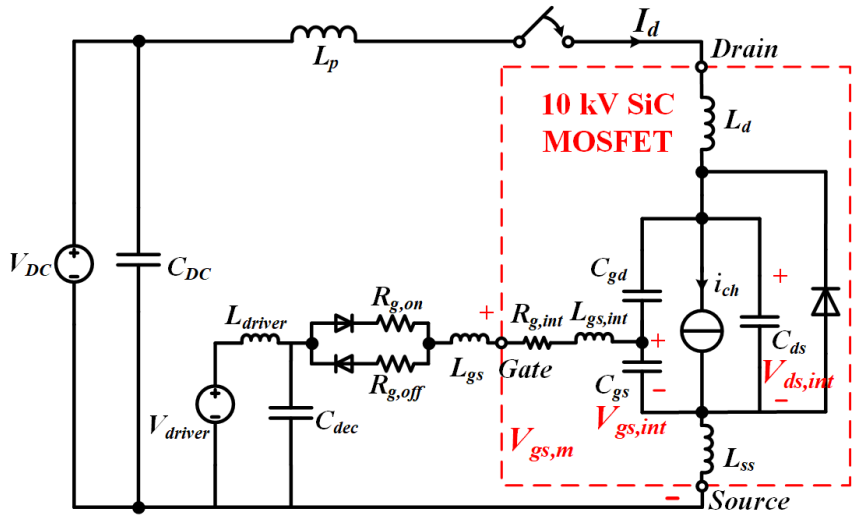


Fig. 5- 2. Circuit model of the 10 kV SiC MOSFET in ON state under flashover fault modeled by closing an ideal switch.

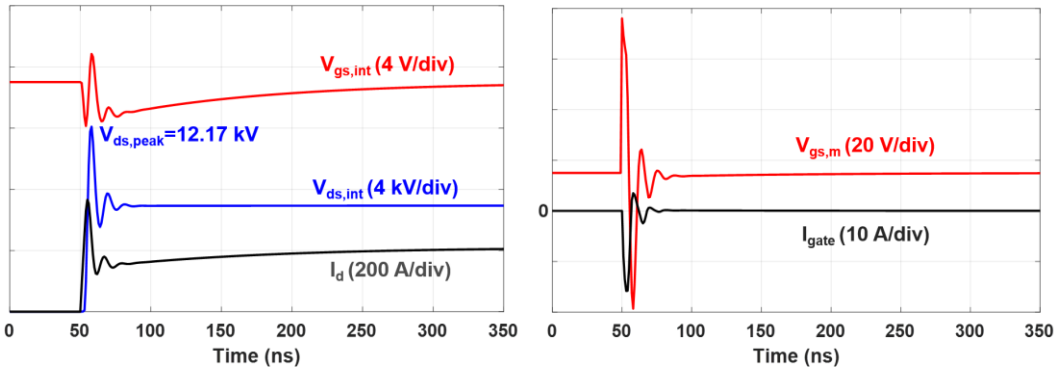
case, the main discrepancy between simulation and experimental results is caused by the MOSFET model which cannot model all nonlinear effects in short circuit conditions, instead of the flashover fault model [37]. Before the fault happens, the MOSFET is fully ON with 15 V $V_{gs,int}$. In summary, the simulation model can effectively model a flashover fault in a real HB phase leg.

The simulation model in Fig. 5-2 is established in PLECS. The phase leg has a power loop inductance L_p of 80 nH and a dc-link capacitance of 8.75 µF. The 10 kV SiC MOSFET gate driver has a gate loop inductance L_{gs} of 5 nH, and the decoupling capacitor C_{dec} is 2.18 µF. V_{driver} is always 15 V in the simulation.

5.2.2 10 kV SiC MOSFET without Kelvin Source

In 10 kV SiC MOSFETs without Kelvin source, the gate loop is heavily influenced by extremely fast voltage and current transients due to the flashover fault. High *di/dt* disturbs the gate loop by inducing a high voltage across L_{ss}. Meanwhile, high *dv/dt* and Miller capacitance C_{gd} introduce the Miller current. The simulation waveforms at 7 kV are displayed in Fig. 5-3, in which turn-on gate resistance $R_{g,on}$ and turn-off gate resistance $R_{g,off}$ are 15 Ω and 2.5 Ω, respectively. The fault occurs at t=50 ns.

The high *di/dt* resulting from the flashover fault induces a high positive voltage across L_{ss}, leading to -16.2 A instantaneous gate current I_{gate} and reduced $V_{gs,int}$, as shown in Fig. 5-3(b). The channel current decreases accordingly. Meanwhile, the drain current is not allowed to change rapidly because of the power loop inductance, hence C_{ds} is effectively charged, leading to high *dv/dt* and a large overshoot in $V_{ds,int}$. $V_{gs,int}$ and drain current effectively decrease as the oscillation continues, since the gate current discharging



(a) (b)

Fig. 5- 3. Simulation waveforms of flashover fault at 7 kV with 1 nH common source inductance L_{ss}, 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off}$: (a) Waveforms of $V_{ds,int}$, I_d, and $V_{gs,int}$; (b) Waveforms of $V_{gs,m}$ and gate current I_{gate}.

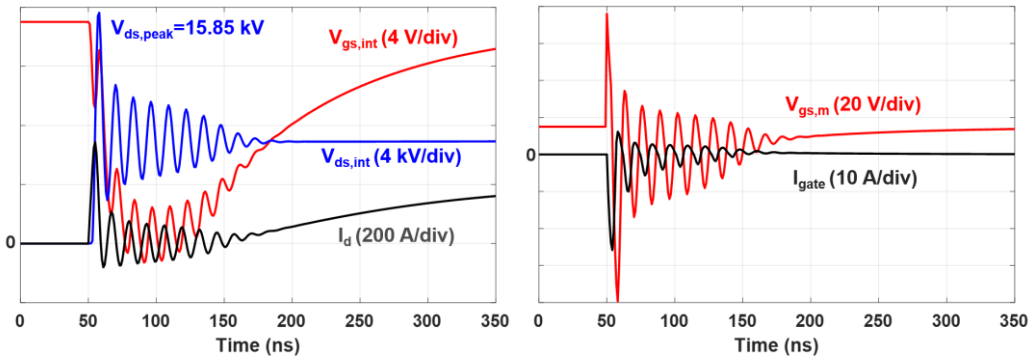
C_{gs} is higher because the selected $R_{g,off}$ is 1/6 of $R_{g,on}$. After the oscillation ends, it takes ~300 ns for $V_{gs,int}$ to rise back to 15 V, and then the drain current reaches the saturation current. In this case, the risk of device damage due to overvoltage is considerable.

The Miller current from C_{gd} counteracts the effect of voltage across L_{ss} on $V_{gs,int}$ and channel current. With asymmetrical gate resistance, the negative spike of I_{gate} is more substantial than its positive spike, and $V_{gs,int}$ continues decreasing until the oscillation ends. This phenomenon is slightly alleviated by the Miller current. When positive *di/dt* occurs, the voltage drop across L_{ss} generates current to discharge C_{gs}. Meanwhile the Miller current due to the positive *dv/dt* (>1 kV/ns) enters the gate loop and effectively increases $V_{gs,int}$.

In addition, if the asymmetry in gate resistance becomes worse with a smaller $R_{g,off}$, the effect of the voltage across L_{ss} completely dominates. If $R_{g,off}$ is 0 Ω, $V_{gs,int}$ drops rapidly to 0 V within 30 ns once a flashover fault happens, as displayed in Fig. 5-4(a). The tremendous decline in $V_{gs,int}$ is attributed to the gate current I_{gate} with high negative peaks shown in Fig. 5-4(b) due to asymmetrical gate resistance. Such "self turn-off" behavior is also reported in [37]. It results in smaller short circuit current and energy loss, but the disadvantage is the extremely high peak voltage (15.85 kV) in $V_{ds,int}$. The channel is effectively shut off for a short time, and severe ringing (77 MHz) occurs in $V_{ds,int}$ due to the resonance between the 80 nH L_p and 48 pF C_{ds} (when $V_{ds,int} > 3$ kV).

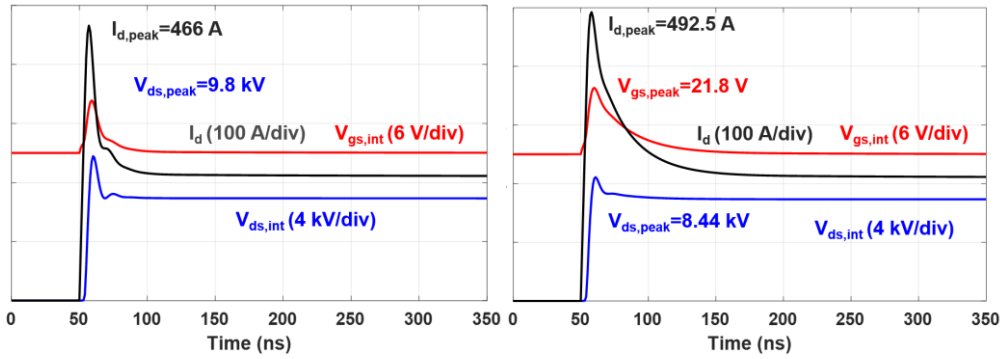
5.2.3 10 kV SiC MOSFET with Kelvin Source

With a Kelvin source in the 10 kV SiC MOSFET, extremely fast transients under a flashover fault are mainly coupled to the gate loop via the Miller capacitance C_{gd}. If L_{ss}



(a) (b)

Fig. 5- 4. Flashover fault simulation results at 7 kV with 1 nH L_{ss}, 15 Ω $R_{g,on,}$ and 0 Ω $R_{g,off}$: (a) Waveforms of $V_{ds,int}$, I_d, and $V_{gs,int}$; (b) Waveforms of $V_{gs,m}$ and I_{gate}.



(a) (b)

Fig. 5- 5. Simulation waveforms of flashover fault at 7 kV with 0.15 nH L_{ss} and 15 Ω $R_{g,on}$: (a) 0 Ω $R_{g,off.}$ (b) 2.5 Ω $R_{g,off.}$

is negligible, the flashover fault induces positive voltage spike in $V_{gs,int}$ and high device current and energy loss, according to simulation waveforms in Fig. 5-5. To simulate this case, it is assumed that L_{ss} is 0.15 nH with an 85% reduction compared to the MOSFET without Kelvin source.

With negligible L_{ss}, the significant oscillations in the gate loop and power loop are eliminated. In this case, the extremely high *dv/dt* and the nonlinear Miller capacitance result in a substantial spike in $V_{gs,int}$. $V_{gs,int}$ increases by 45% to 21.8 V with 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off}$. The peak drain current is higher than 2X saturation current of the channel (211 A), leading to high short circuit energy loss. On the other hand, the overvoltage in $V_{ds,int}$ is reduced compared to the case without Kelvin source, because of increasing $V_{gs,int}$ and channel current at the early stage of a flashover fault. The MOSFET damage due to overvoltage is not likely in this case, which is obviously a major concern for the MOSFET without a Kelvin source. However, the device damage due to high energy loss and junction temperature is the concern that should be tackled in gate driver design.

5.3 Gate Driver Design Considerations

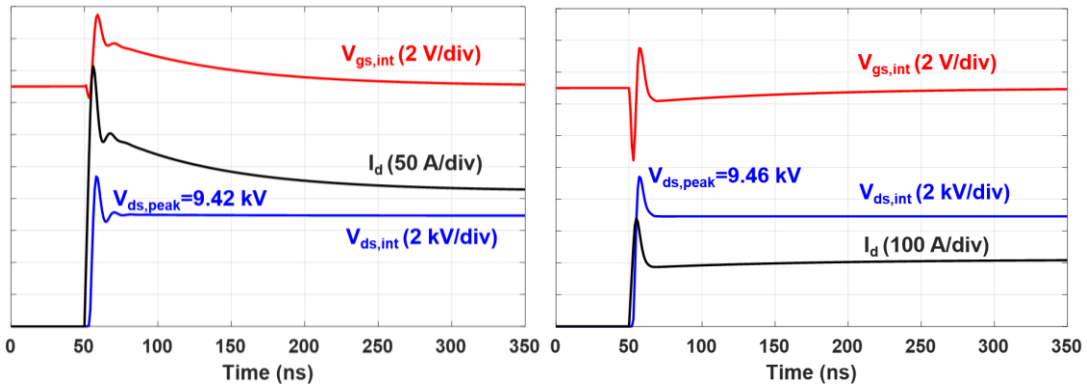
This section discusses how to improve the performance of the 10 kV SiC MOSFET and reduce the risk of device damage under a flashover fault from the perspective of gate driver design. The design target is to lower peak $V_{ds,int}$ and $I_{d,peak}$ under a flashover fault. Gate driver design guidelines are provided for gate resistance selection, gate loop inductance, and whether to add an external capacitor across gate and source terminal. The short circuit energy loss and the impact of a flashover fault on short circuit protection design are not covered in this section, since both are investigated in detail in Section 5.4.

5.3.1 10 kV SiC MOSFET without Kelvin Source

Without a Kelvin source available in device package, a relatively high turn-off gate resistance should be selected. The small $R_{g,off}$ and significant asymmetry in gate loop result in reduced $V_{gs,int}$ and substantial voltage overshoot that could damage the MOSFET at the beginning of a flashover fault. Such asymmetrical gate resistance should be avoided in the 10 kV SiC MOSFET gate driver. As shown in Fig. 5-3, Fig. 5-4, and Fig. 5-6(a), as $R_{g.off}$ keeps increasing from 0 Ω to 7.5 Ω (with 15 Ω $R_{g,on}$), the peak value of $V_{ds,int}$ decreases from 15.85 kV to 9.42 kV. Hence, higher $R_{g,off}$ is preferred to reduce the voltage stress when a flashover fault happens. In fact, increasing $R_{g,off}$ from 0 Ω to 7.5 Ω has negligible impact on the turn-off loss and *dv/dt* of the 10 kV/20 A SiC MOSFET during the normal operation, because the current of the MOSFET channel drop to zero very quickly [44].

Adding an external capacitor across gate and source terminal of the MOSFET suppresses oscillations in the gate loop and reduces voltage overshoot in $V_{ds,int}$ during the flashover fault, as can be seen in Fig. 5-6(b). With 15 Ω $R_{g,on}$ and 2.5 Ω $R_{g,off.}$, the peak $V_{ds,int}$ reduces from 12.17 kV to 9.46 kV after adding a 500 pF external capacitor between gate and source terminal of the MOSFET. Adding a larger external capacitor is not recommended since the capacitor will result in higher converter switching loss. A smaller capacitor only increases switching loss slightly, yet it will be less effective in reducing the overvoltage of $V_{ds,int}$. Generally, the best solution to suppressing overvoltage in $V_{ds,int}$ is a relatively large $R_{g,off}$ to achieve lower $R_{g,on}/R_{g,off}$, although a small external capacitor is also effective.

In addition, a small gate loop inductance L_{gs} is desirable from the perspective of flashover fault. A large gate loop inductance L_{gs} causes higher $V_{gs,int}$ and device current



(a) (b)

Fig. 5- 6. Simulation waveforms of flashover fault at 7 kV with 1 nH L_{ss}: (a) 15 Ω $R_{g,on}$ and 7.5 Ω $R_{g,off}$, (b) 15 Ω $R_{g,on}$ and 2.5 Ω $R_{g,off}$. as well as a 500 pF external capacitor.

and energy loss during the flashover fault, since the large impedance of L_{gs} alleviates the asymmetric impedance in the gate loop and hence the effect of L_{ss}. On the other hand, larger L_{gs} strengthens the effect of Miller current, and a larger portion of Miller current flows to C_{gs}. Compared to the case in Fig. 5-3(a), the peak device current surges from 367 A to 435 A when L_{gs} rises from 5 nH to 30 nH. Hence a large gate loop inductance should be avoided in PCB layout.

5.3.2 10 kV SiC MOSFET with Kelvin Source

If L_{ss} is negligible, a smaller turn-off gate resistance and gate loop inductance are preferable to reduce current and energy loss during a flashover fault. To suppress positive voltage spike in $V_{gs,int}$ due to Miller current, it is crucial to reduce the gate loop impedance when the gate current is negative. $R_{g,off}$ as well as L_{gs} thereby should be as small as possible, while $R_{g,on}$ should still be determined by the switching performance during the normal operation. As displayed in Fig. 5-7, a large $R_{g,off}$ (7.5 Ω) causes 7.9 V spike in $V_{gs,int}$ and 12.2% increase in peak current compared to the case with 0 Ω $R_{g,off}$ (5.2 V spike in $V_{gs,int}$, 466 A peak short circuit current), and the 523 A peak device current is 2.5X device saturation current, which will be increased further to 539 A with 30 nH L_{gs} due to poor PCB layout.

With negligible L_{ss}, adding an external capacitor across the gate and source terminal is not recommended because it only reduces the peak current slightly. With a 1 nF external capacitor, the peak current only drops by 2.9% compared to 492.5 A in Fig. 5-5(b). Because of 2 Ω $R_{g,int}$ and 1 nH $L_{gs,int}$ inside the device package, it is not likely that a small external capacitor can reduce device current under the flashover fault substantially.

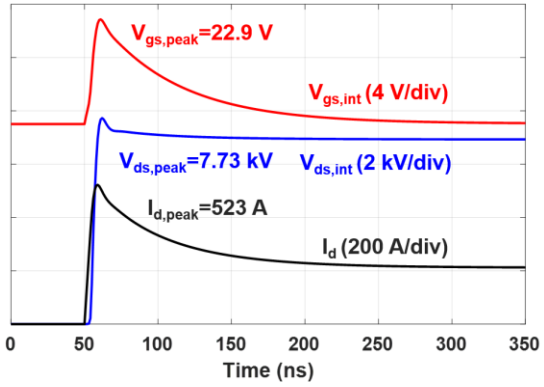


Fig. 5- 7. Simulation waveforms of flashover fault at 7 kV with 0.15 nH L_{ss}, 15 Ω $R_{g,on,}$ and 7.5 Ω $R_{g,off.}$

5.3.3 Summary

The 10 kV SiC MOSFET gate driver design guidelines are summarized in Table 10, to achieve lower device damage risk and better performance under a flashover fault.

5.4 Short Circuit Energy Loss and Protection Design

A flashover fault usually generates high energy loss, because $V_{ds,int}$ and I_d soar rapidly to reach dc-link voltage and saturation current, respectively. In this section, the energy loss of the 10 kV SiC MOSFET under a flashover fault is investigated quantitatively, which is essential in short circuit protection design. Nonetheless, the response time of short circuit protection is typically determined based on short circuit performance under HSF and FUL, instead of the flashover fault. As a result, the designed protection may not be fast enough to safely turn off the MOSFET under a flashover fault. A fair comparison between the flashover fault and the FUL fault as well as the HSF fault is made to quantitatively show how much higher energy loss a flashover fault produces. Response time required to safely clear the flashover fault is provided to guide short circuit protection design.

5.4.1 Simulation of FUL and HSF

The same 10 kV SiC MOSFET model in the simulation of a flashover fault is adopted in the simulation of FUL in order to make a fair comparison. To emulate a FUL, the ideal switch in Fig. 5-2 should be replaced by a power semiconductor device with much higher saturation current so that the 10 kV SiC MOSFET eventually withstands complete dc-link voltage during the fault.

When simulating a FUL, the ideal switch is replaced by a 10 kV SiC MOSFET module composed of three identical 10 kV/20 A dies in parallel. Such implementation

Table 10. Gate driver design considerations from the standpoint of flashover fault

10 kV SiC MOSFET	**w/ Kelvin source**	**w/o Kelvin source**
Gate loop inductance L_{gs}	Reduce L_{gs} in layout	Reduce L_{gs} in layout
Turn-off gate resistance $R_{g,off}$	Select a relatively small $R_{g,off}$	Select a larger $R_{g,off}$ to avoid high $R_{g,on}/R_{g,off}$
External capacitor across gate and source	Adding an external capacitor is not effective	Adding an external capacitor is effective but not recommended

ensures sufficiently high saturation current and makes full use of the established 10 kV SiC MOSFET model in Section 5.1. The gate resistance of the 10 kV SiC MOSFET module is selected to ensure fast turn-on process to emulate the short circuit in the load side. The power loop inductance and dc-link capacitance are the same as those in the flashover fault simulation.

In the simulation of a HSF, the ideal switch in the HB phase leg in Fig. 5-2 is completely shorted. C_{DC} and L_p are not changed. The HSF occurs once the 10 kV SiC MOSFET is turned on. During the fault, $V_{ds,int}$ remains close to the dc-link voltage, so gate threshold voltage $V_{g,th}$ is not dominated by $V_{ds,int}$ any more. Instead, $V_{g,th}$ decreases dramatically as device junction temperature T_j rises rapidly under the HSF fault. $V_{g,th}$ in the model of the MOSFET channel should hence be modified for more accurate simulation result under the fault. An empirical model of $V_{g,th}$ as a function of T_j is derived based on the experimental data of the 10 kV/20 A SiC MOSFET under a HSF. The nonlinear model of $V_{g,th}$ is realized with a look-up table in PLECS. The instantaneous T_j during the fault is estimated with the energy loss and thermal capacitance of the drift region of the device, which is 6.4 mJ/K [59]. Other parts of the MOSFET model in Section 5.1 remain unchanged to make a fair comparison.

5.4.2 Comparison between Flashover and FUL Fault

Common source inductance L_{ss} makes a difference in the behavior of the 10 kV SiC MOSFET under the flashover fault. A large L_{ss} reduces $V_{gs,int}$ and device current in the early stage of a flashover fault. However, as displayed in Fig. 5-8, a large L_{ss} is only able to significantly reduce short circuit energy loss as $R_{g,off}$ approaches zero, inevitably giving

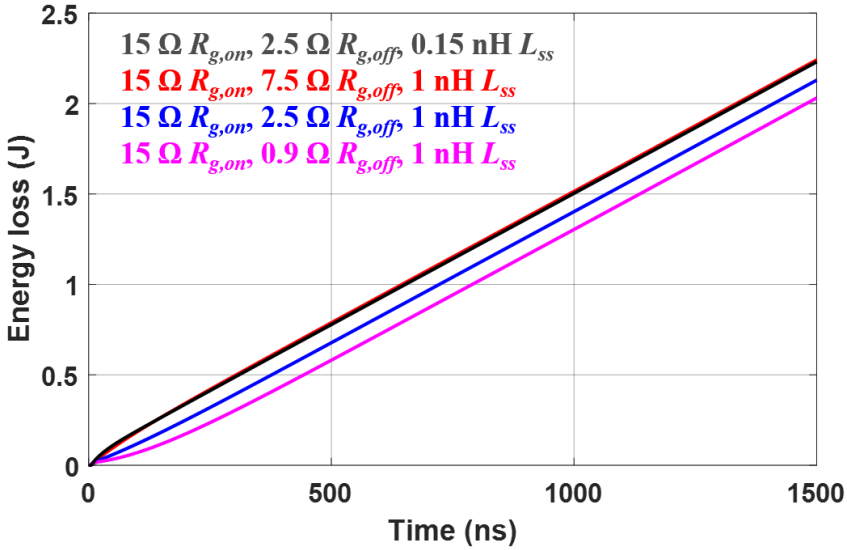


Fig. 5- 8. Short circuit energy loss under flashover fault at 7 kV with different gate resistances and common source inductance.

rise to huge spike in $V_{ds,int}$ which can damage the MOSFET. Therefore, it is not realistic to take advantage of a large L_{ss} to reduce energy loss during a flashover fault. In summary, if gate resistance is correctly selected to prevent device damage from overvoltage under a flashover fault, common source inductance has little influence on the energy loss during a flashover fault.

Simulation waveforms of the 10 kV SiC MOSFET under both the flashover and the FUL fault at 7 kV are displayed in Fig. 5-9, both of which last for 1.5 μs. The gate driver for the 10 kV SiC MOSFET with Kelvin source has 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off.}$ Compared to a flashover fault, a FUL results in much slower transient. After the FUL fault occurs, it takes 760 ns for $V_{ds,int}$ and I_d to reach their saturation levels. $V_{ds,int}$ rises slowly with an average *dv/dt* of 13.6 V/ns. In fact, there is a 230 ns delay before $V_{ds,int}$ starts to increase with a high slew rate. The slow transient contributes to lower energy loss under the FUL fault than that under a flashover fault, with details shown in Fig. 5-10. In the first 500 ns, the energy loss under the FUL is 0.1 J, while the flashover fault has a 0.77 J energy loss. After 1.5 μs, the flashover fault produces 49.5% higher energy loss than the FUL.

With 49.5% higher device energy loss under the flashover fault than the FUL, a shorter response time is required in the short circuit protection design to prevent device damage due to high energy loss. In fact, after $V_{ds,int}$ and I_d reach steady state, the energy loss difference between FUL and flashover fault is ~0.74 J. The energy loss difference is mainly established in the first 500 ns of the fault. For instance, based on Fig. 5-10, the energy loss under the flashover fault reaches 1.5 J at t=1 μs, while the energy loss under the FUL

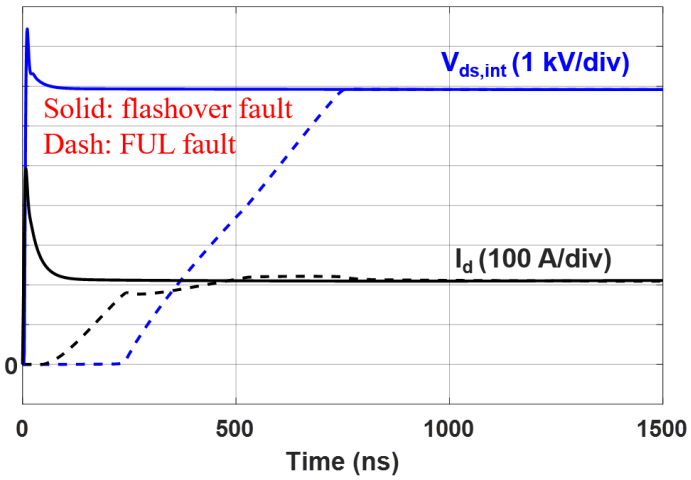


Fig. 5- 9. Simulation waveforms of FUL and flashover fault at 7 kV with 0.15 nH L_{ss}, 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off.}$

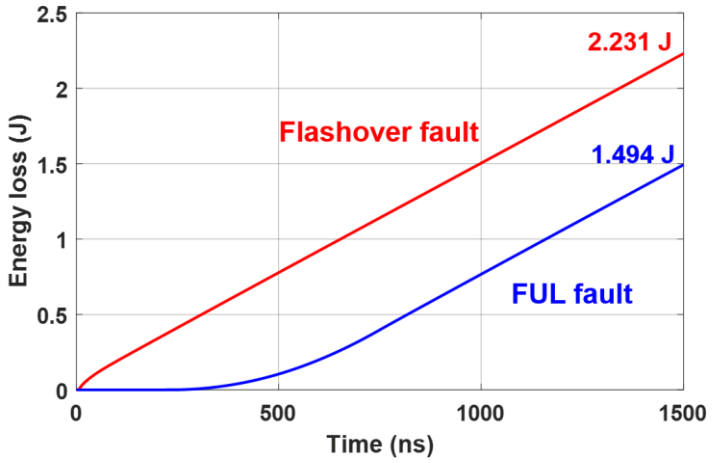


Fig. 5- 10. Short circuit energy loss comparison between FUL and flashover fault at 7 kV with 0.15 nH L_{ss}, 15 Ω $R_{g,on}$, and 2.5 Ω $R_{g,off}$.

reaches 1.5 J at t=1.5 μs. From the perspective of critical energy, in order to achieve the same margin, the short circuit response time under a flashover fault should be ~500 ns shorter than that under a FUL.

5.4.3 Comparison between Flashover Fault and HSF Fault

Similar analysis can be conducted to compare the performance of the 10 kV SiC MOSFET under the flashover fault and the HSF, with details displayed in Fig. 5-11 and Fig. 5-12. Under both faults, L_{ss} is 0.15 nH, and the MOSFET is driven with 15 Ω $R_{g,on,}$ and 2.5 Ω $R_{g,off}$. Fig. 5-11 displays the typical behavior of the 10 kV SiC MOSFET under a HSF. $V_{ds,int}$ has a small dip and subsequently climbs back to the dc-link voltage (7 kV) quickly, and the device always operates in the active region.

After 1.5 μs, the flashover fault produces 29.5% higher energy loss than a HSF. The 0.51 J energy loss difference between the two kinds of faults is mainly due to the short circuit current during the first 800 ns. The device current under the flashover fault soars immediately with a huge overshoot, while the short circuit current under the HSF rises slowly with an average *di/dt* of 0.223 A/ns. After the device current saturates, the instantaneous power loss under the two faults is almost the same.

Based on the simulation result, in order to limit the energy loss to the same level, the short circuit response time under the flashover fault should be ~350 ns shorter than that under the HSF. For example, if 1.5 J critical energy is assumed, the flashover fault should be cleared within 997 ns, and the HSF fault should be cleared within 1.348 μs to guarantee the same margin in short circuit protection.

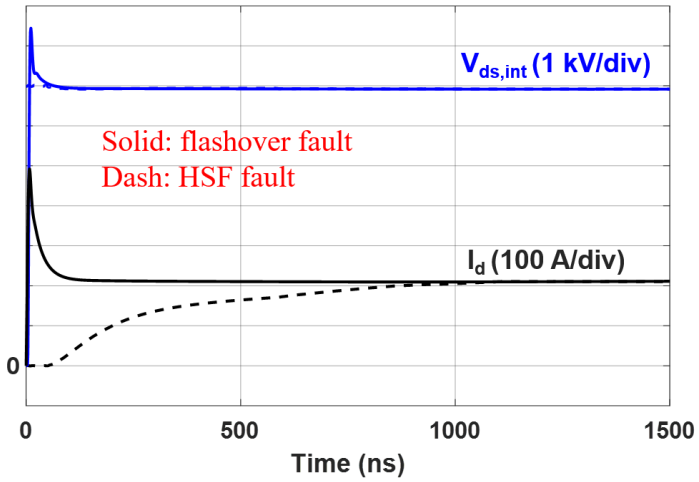


Fig. 5- 11. Simulation waveforms of HSF and flashover fault at 7 kV with 0.15 nH L_{ss}, 15 Ω $R_{g,on}$, and 2.5 Ω $R_{g,off}$.

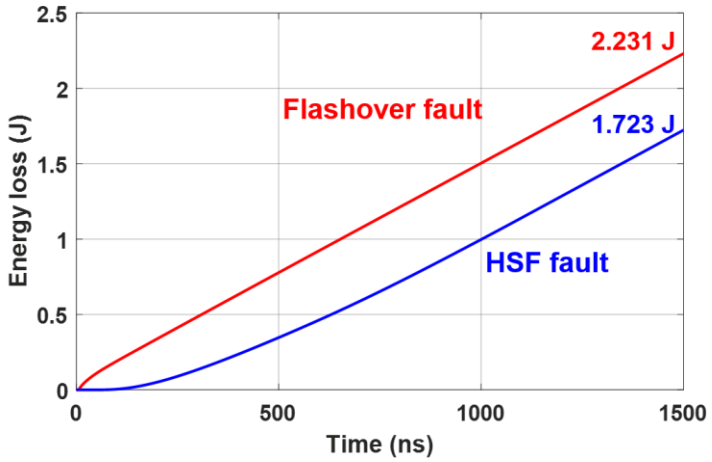


Fig. 5- 12. Short circuit energy loss comparison between HSF fault and flashover fault at 7 kV with 0.15 nH L_{ss}, 15 Ω $R_{g,on}$, and 2.5 Ω $R_{g,off}$.

5.5 Summary

The 10 kV SiC MOSFET under a flashover fault due to insulation failure is analyzed comprehensively, where *dv/dt*, *di/dt*, and energy loss are higher than those under FUL and HSF short circuit fault. Extremely fast transients impact the gate loop via common source inductance and Miller capacitance. In order to reduce the risk of device damage under a flashover fault, a relatively higher $R_{g,off}$ is suggested for 10 kV SiC MOSFETs without Kelvin source to avoid a large $R_{g,on}/R_{g,off}$, while a relatively small $R_{g,off}$ is recommended for the MOSFET with Kelvin source. Design guidelines for gate loop inductance or adding an external capacitor across gate and source terminal are also provided to achieve better device performance under a flashover fault.

Short circuit performance under a flashover fault, FUL, and HSF is compared at 7 kV and 15 V gate-to-source voltage. With 49.5% higher energy loss under the flashover fault, the required response time to clear the flashover fault should be ~500 ns shorter than that designed to clear the FUL. The response time to clear the flashover fault should be ~350 ns shorter than the response time determined by the HSF. In terms of future work, more accurate short circuit model of the MOSFET and experimental results are needed to make the analysis results more accurate.

CHAPTER 6. OVERCURRENT PROTECTION DESIGN WITH STRONG NOISE IMMUNITY AND FAST RESPONSE

This chapter is aimed at further accelerating the response of the desat protection for 10 kV SiC MOSFETs and other high voltage (> 3.3 kV) SiC MOSFETs. To pursue desat protection with faster response, the noise immunity of the desat protection under high *dv/dt* is examined carefully, which yields systematic design guidelines to improve the noise immunity significantly. An improved desat protection scheme is introduced with much faster response than the desat protection in the baseline design in Section 3.2, and strong noise immunity is maintained. Last but not least, a desat protection scheme with ultrafast response is proposed and successfully validated with excellent noise immunity and ultrafast protection response (<160 ns response time) at the same time.

It should also be mentioned that part of the content in this chapter is from the author's paper published in *IEEE APEC 2020* [84] and the author's another paper published in *IEEE APEC 2021* [97].

6.1 Noise Immunity Analysis and Enhancement of Desat Protection

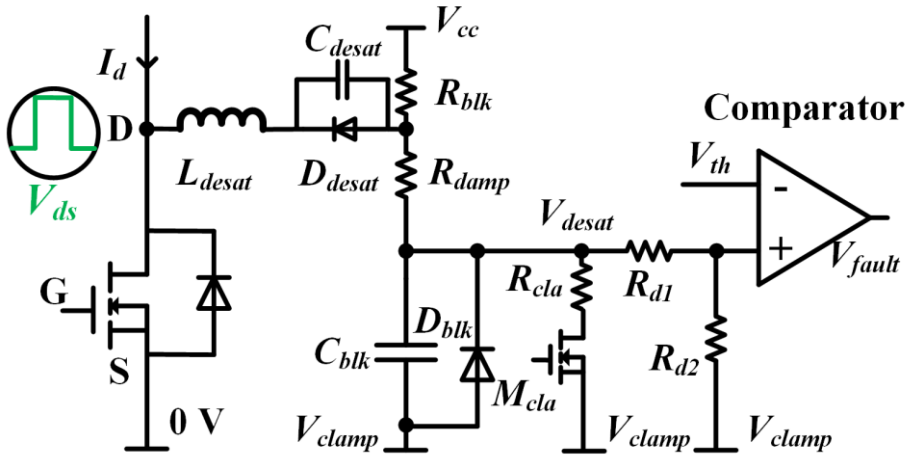
When pursuing desat protection with faster response for high voltage SiC MOSFETs, there is a concern that its noise immunity will be sacrificed. The desat protection could be falsely triggered. Therefore, the noise immunity of the desat protection circuitry should be thoroughly evaluated in order to realize desat protection with fast response.

This section comprehensively analyzes desat protection for high voltage (>3.3 kV) SiC MOSFETs, and especially how to build in noise immunity under high *dv/dt*. The study

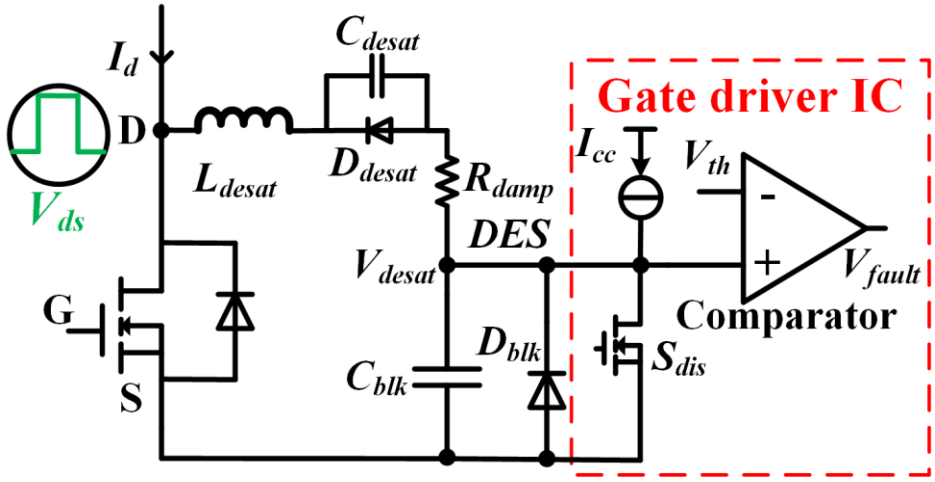
aims to lay a solid foundation to identify the better trade-off between noise immunity and response speed of desat protection. Both positive *dv/dt* and negative *dv/dt* are investigated. Analysis results reveal that the high *dv/dt* with long duration caused by high voltage SiC MOSFETs' switching results in strong noise interference in the desat protection circuitry. The impact of numerous influencing factors is investigated analytically, such as parasitic capacitances, parasitic inductance, damping resistance, and clamping impedance. Under high positive *dv/dt*, extremely small parasitic capacitances (<0.01 pF) between the drain terminal and protection circuitry could still compromise noise immunity of the desat protection circuitry that has a high-impedance voltage divider. Comprehensive design guidelines are summarized to boost the noise immunity, including circuit design, component selection, and PCB layout. The noise immunity margin under the positive *dv/dt* is also derived quantitatively to guide the noise immunity improvement. The noise immunity analysis results and developed noise immunity improvement methods are validated with simulation and experimental results.

6.1.1. Overview of Desat Protection Circuitry

Desat protection for high voltage SiC MOSFETs can be implemented with circuitry composed of discrete components or with a gate driver IC with an integrated desat protection function, as illustrated in Fig. 6-1. The gate driver IC with desat protection function (MC33153 and FOD8318 from On Semiconductor, STGAP1AS from STMicroelectronics, etc) enables more compact layout, yet leads to too low of a threshold current for some high voltage SiC MOSFETs due to its low threshold voltage (<10 V) for desat protection [60], [61], [98]. With a voltage divider and a discrete comparator, desat



(a)



(b)

Fig. 6- 1. Two implementations of desat protection for high voltage SiC MOSFETs: (a) Based on discrete components; (b) Realized with gate driver IC.

protection based on discrete components has better flexibility to achieve a desired response time and threshold current for various high voltage SiC MOSFETs. In this section, noise immunity of both implementations will be analyzed in detail.

6.1.2 Noise Immunity Analysis

The noise interference and spurious triggering of desat protection are mainly caused by high dv_{ds}/dt generated by high voltage SiC MOSFETs. High dv/dt can disturb the operation of the desat protection circuitry via the parasitic capacitance C_{desat} of the desat diode D_{desat}, including both implementations in Fig. 6-1. Fig. 6-2 and Fig. 6-3 illustrate the influence of high dv/dt and the resulting displacement current on the desat protection circuitry based on discrete components. In addition to C_{desat}, the parasitic inductance L_{desat} should also be considered. A well-known mechanism of spurious triggering is caused by interference from high dv_{ds}/dt that results in the blanking capacitor voltage V_{desat} or the comparator input voltage V_{comp} rising substantially and then exceeding the comparator threshold voltage V_{th} [59], [66].

Positive dv_{ds}/dt results in a positive spike in V_{desat} and hence heavily impacts the noise immunity of the desat protection circuitry. Traditionally, R_{damp} is added to damp the oscillation. In the protection circuitry composed of discrete components, R_{cla} and a transistor M_{cla} are installed to clamp V_{desat} [66]. As illustrated in Fig. 6-2, R_{cla} and M_{cla} are introduced with the purpose of absorbing the displacement current of C_{desat} due to the high positive dv_{ds}/dt, without which V_{desat} will increase dramatically and could lead to spurious triggering. R_{cla} and M_{cla} are necessary if the output voltage of the gate driver IC cannot serve as V_{cc} since the magnitude of V_{cc} is required to be higher than the on-state gate voltage

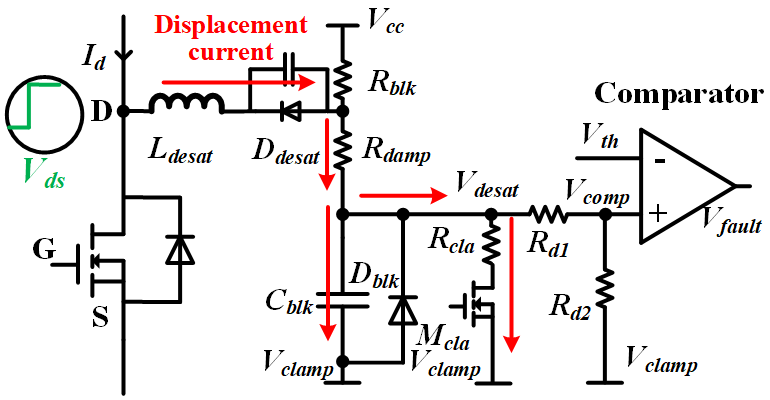


Fig. 6- 2. Displacement current due to C_{desat} and positive dv_{ds}/dt in desat protection circuitry.

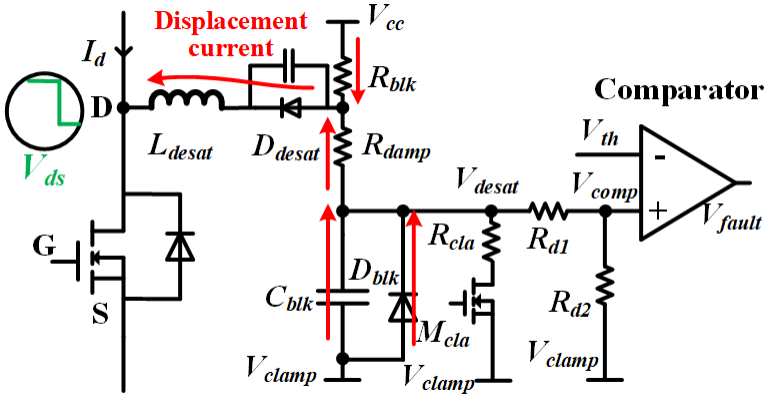


Fig. 6- 3. Displacement current caused by C_{desat} and negative dv_{ds}/dt in desat protection circuitry.

$V_{gs,on}$. This is often the case when designing desat protection for high voltage SiC MOSFETs requiring relatively high desat threshold voltage. As for the desat protection circuitry realized by the gate driver IC, the discharge switch S_{dis} can absorb the displacement current from C_{desat}. Still, there will be positive spikes and oscillations in V_{desat} due to high positive dv_{ds}/dt, which will be studied in this section.

With the interference of negative dv_{ds}/dt generated by high voltage SiC MOSFETs, usually the comparator will not be falsely triggered. Instead, V_{desat} and V_{comp} could experience a voltage dip if the displacement current of C_{desat} is much higher than the current from V_{cc} or I_{cc}. As shown in Fig. 6-3, C_{blk} will be discharged to contribute to the displacement current of C_{desat}, and V_{desat} and V_{comp} will decline during the voltage fall time of V_{ds}. In this case, the voltage dip in V_{desat} or V_{comp} could falsely trigger some comparators and hence the desat protection, due to the mechanism named phase reversal or phase inversion because the comparator input voltage is lower than the allowed minimum input voltage [99]-[101]. To alleviate the impact of the negative dv/dt, the clamping diode D_{blk} (as shown in Fig. 6-1) is often added.

In this section, the desat protection designed for the 10 kV/20 A SiC MOSFET used to build the phase legs in this dissertation is studied as an example for noise immunity analysis. Parameters of the desat protection circuitry are shown in Fig. 6-4, and the circuit model is established in PLECS. Although the study example is a desat protection circuitry implemented with discrete components, the study results will also benefit noise immunity analysis of the desat protection realized by the gate driver IC. Thus, noise immunity of the desat protection realized by the gate driver IC will also be examined in detail.

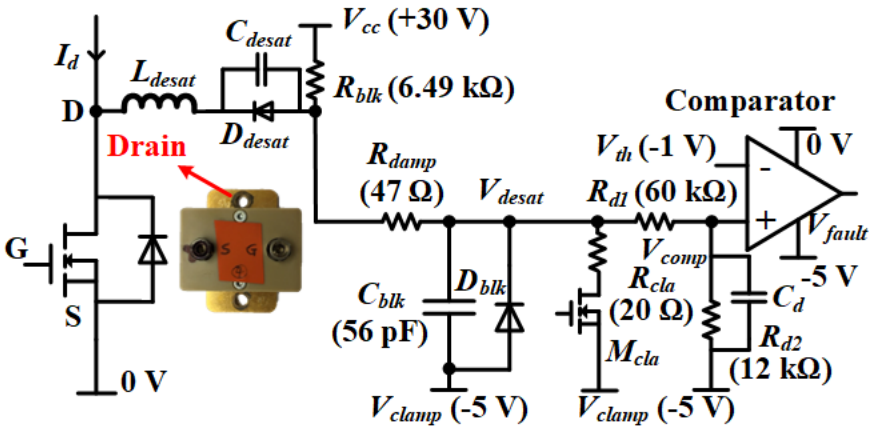


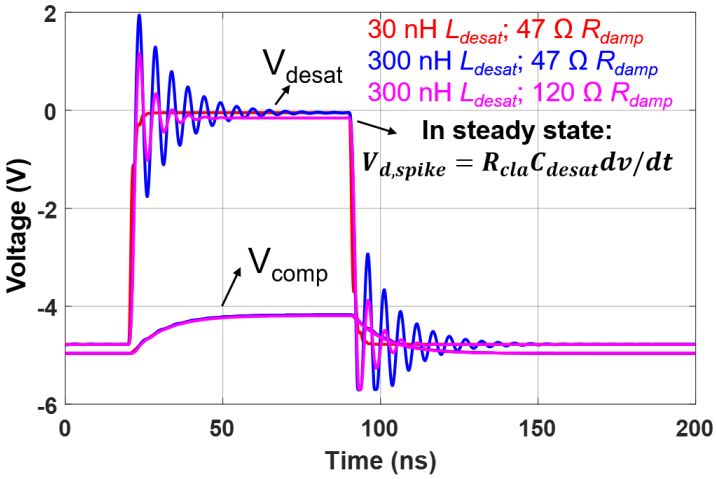
Fig. 6- 4. Desat protection for 10 kV/20 A SiC MOSFET from Wolfspeed.

Parasitic capacitance of the desat diode C_{desat} is nonlinear and decreases rapidly as V_{ds} increases. Meanwhile, the resulting displacement current does not change significantly since dv_{ds}/dt is low when the parasitic capacitance of the desat diode is large. The nonlinear C_{desat} of the diode (three 3.3 kV SiC Schottky diodes in series) is hence modeled with its charge-equivalent linear capacitance (2.3 pF) [87], [102].

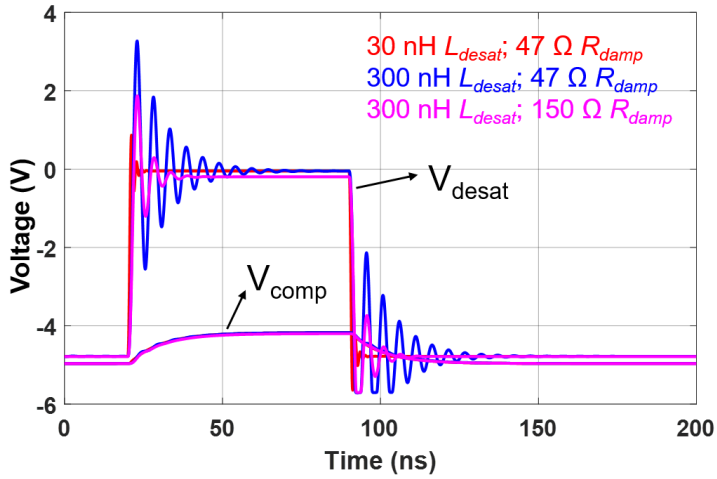
6.1.2.1 Analysis of Blanking Capacitor Voltage V_{desat}

In this subsection, V_{desat} under the negative dv/dt will not be discussed in detail. The worst voltage dip in V_{desat} under negative dv/dt happens when D_{blk} enters the conduction mode. In such case, the voltage dip is simply determined by the forward voltage drop of D_{blk}, V_{diode}. The maximum positive spike in V_{desat} under negative dv/dt cannot be higher than that under positive dv/dt. Thus, this subsection focuses on how positive dv/dt shapes V_{desat}. The analysis of V_{desat} will benefit the noise immunity analysis of both hardware implementations shown in Fig. 6-1.

Under a constant dv/dt of +100 V/ns as V_{ds} rises from 0 to 7 kV, simulation waveforms of V_{desat} are displayed in Fig. 6-5. Because of M_{cla} and R_{cla} ($R_{cla} << R_{blk}$), V_{desat} is clamped to V_{clamp} (-5 V) before V_{ds} starts to rise at t = 20 ns. This is a reasonable assumption because V_{desat} should be clamped at V_{clamp} before high positive dv/dt is generated, no matter whether the high voltage SiC MOSFET is the active switch or the synchronous switch. During the 70 ns voltage rise time t_{rise}, V_{desat} reaches steady state after the oscillation is damped. At steady state, the spike of V_{desat} is proportional to R_{cla}, C_{desat}, and dv_{ds}/dt, all of which heavily influence noise immunity.



(a)



(b)

Fig. 6- 5. Simulation waveforms of desat protection for 10 kV/20 A SiC MOSFETs: (a) C_{blk}=56 pF; (b) C_{blk}=20 pF.

The peak value of V_{desat} during the voltage rise time of V_{ds} is determined by the oscillations at the early stage of voltage rise time. According to simulation waveforms in Fig. 6-5, higher L_{desat} leads to higher peak value of V_{desat}. If C_{blk} is decreased from 56 pF to 20 pF, the oscillations caused by high positive dv_{ds}/dt will result in higher peak in V_{desat}. A larger R_{damp} is effective in suppressing the oscillations and positive spike in V_{desat}, especially when the circuitry has a large L_{desat} and/or a small C_{blk}.

High frequency oscillation of V_{desat} at the beginning of t_{rise} can be analyzed via circuit analysis in the frequency domain. The simplified circuit model used to analyze V_{desat} is drawn in Fig. 6-6. Because M_{cla} is fully on with low impedance before high dv/dt is generated, R_{blk} and the voltage divider formed by R_{d1} and R_{d2} with high impedance can be neglected. The difference between V_{clamp} (-5 V) and 0 V (defined as potential of the source of the 10 kV SiC MOSFET) is also neglected to simplify the analysis.

The relationship between V_{ds} and V_{desat} can be expressed as:

$$\frac{V_{desat}(s)}{V_{ds}(s)} = \frac{sC_{desat}R_{cla}}{s^3LC_{desat}R_{cla}C_{blk} + s^2\left(LC_{desat} + R_{damp}C_{desat}R_{cla}C_{blk}\right) + s\left(C_{desat}R_{cla} + C_{blk}R_{cla} + C_{desat}R_{damp}\right) + 1} \tag{6.1}$$

Based on the Bode plot of $V_{desat}(s)/V_{ds}(s)$ in Fig. 6-7, the peak magnitude is reached at the resonance frequency $\omega_r = \frac{1}{\sqrt{L_{desat}C_{desat}}}$. ω_r is the oscillation frequency of V_{desat} in simulation waveforms in Fig. 6-5. Because V_{ds} has high dv/dt, it is rich with high frequency components, and those components can excite an oscillation at the resonance frequency. The peak magnitude of $V_{desat}(s)/V_{ds}(s)$, $V_{d,pk}$, can be expressed as follows.

$$V_{d,pk} = \frac{R_{cla}}{\sqrt{\left(R_{cla} + R_{damp}\right)^2 + \frac{\left(R_{cla}R_{damp}C_{blk}\right)^2}{L_{desat}C_{desat}}}} \tag{6.2}$$

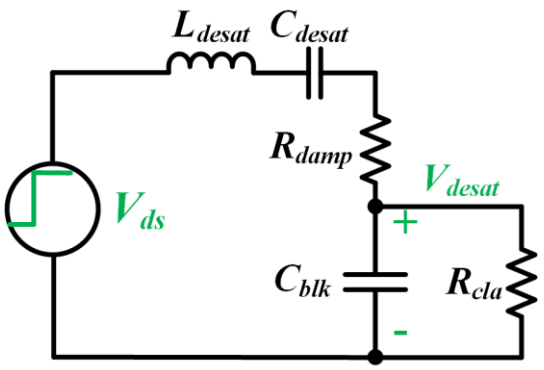


Fig. 6- 6. Simplified circuit model for the analysis of V_{desat}.

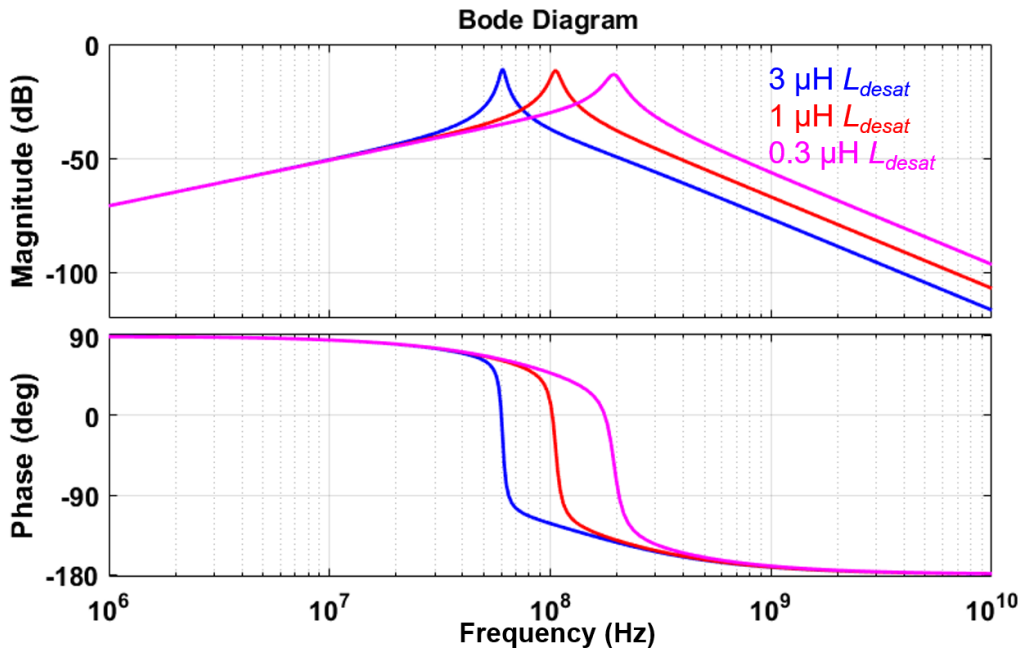


Fig. 6- 7. Bode plot of $V_{desat}(s)/V_{ds}(s)$ as L_{desat} increases (parameters in Fig. 6-4).

$V_{d,pk}$ is an important indicator of the peak value of V_{desat} during the voltage rise time. Higher L_{desat} results in slightly higher $V_{d,pk}$ and thus higher spike in V_{desat} caused by the oscillations. Based on Fig. 6-7, the resonance frequency ω_r becomes lower as L_{desat} increases. According to Fourier analysis of V_{ds}, the magnitude of $V_{ds}(j\omega_r)$ increases as ω_r becomes lower and lower. This is another reason why a higher L_{desat} makes V_{desat} oscillate with higher peak value.

The effect of R_{damp} on the peak value of V_{desat} can also be explained by the analysis of the peak magnitude of $V_{desat}(s)/V_{ds}(s)$. As indicated in Fig. 6-8, $V_{d,pk}$ declines substantially with a higher R_{damp} selected. If R_{damp} is 0 Ω, $V_{d,pk}$ will reach the maximum value of 0 dB. A low R_{cla} effectively shields V_{desat} from the influence of high positive dv_{ds}/dt, which reduces both $V_{d,pk}$ and the steady state level of V_{desat} during the voltage rise time. According to (6.2), increasing C_{blk} also reduces $V_{d,pk}$ and the high frequency oscillations in V_{desat}, which is demonstrated in simulation waveforms in Fig. 6-5.

Also, the analysis of V_{desat} in this subsection is applicable for the desat protection realized with a gate driver IC with integrated desat protection function in Fig. 6-1(b), in which V_{desat} determines the comparator output. In this case, V_{desat} can also be analyzed with the circuit model in Fig. 6-6, since the current source I_{cc} can be neglected due to its high impedance. R_{cla} is mainly dominated by the on-state resistance of the discharge switch S_{dis}, which is turned on as the high voltage SiC MOSFET is in OFF state. As a result, R_{cla} is only determined by the gate driver IC.

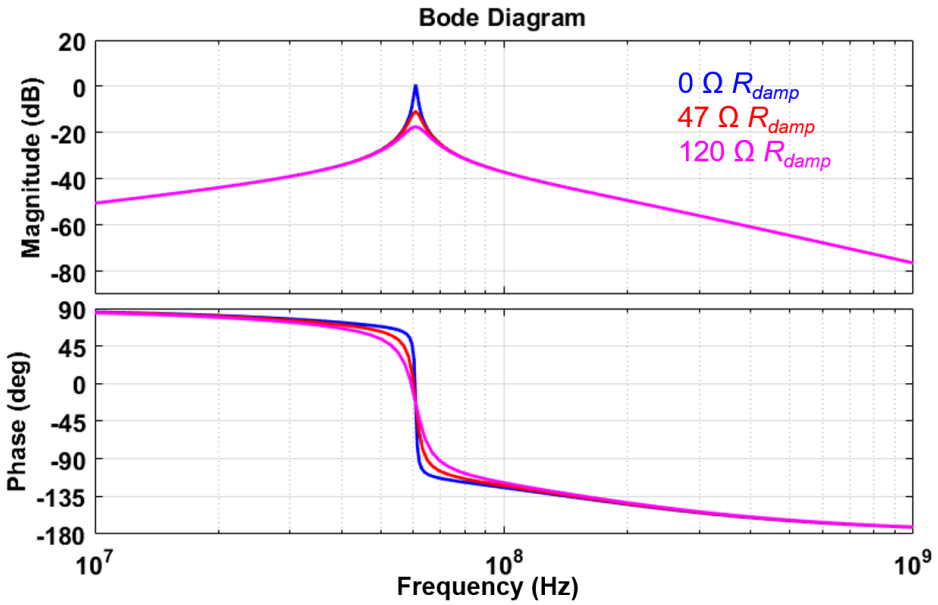


Fig. 6- 8. Bode plot of $V_{desat}(s)/V_{ds}(s)$ as R_{damp} increases (L_{desat}=3 µH).

6.1.2.2 Analysis of Comparator Input Voltage V_{comp} under Positive *dv/dt*

In the desat protection based on discrete components, V_{comp} plays a more critical role in noise immunity than V_{desat}. According to Fig. 6-5, there are no high frequency oscillations in V_{comp}, because the voltage divider and C_d caused by the comparator and PCB layout form an effective low pass filter.

However, extremely small parasitic capacitances between the drain terminal and PCB traces or polygons of the protection circuitry should be considered. As drawn in Fig. 6-9, these parasitic capacitances (< 0.1 pF) are critical due to the high positive *dv/dt* with considerable voltage rise time t_{rise} generated by high voltage SiC MOSFETs. C_{p1} and C_{p2} effectively increase the value of C_{desat}. Particularly, C_{p3} coupled with the voltage divider results in a substantial positive spike in V_{comp}.

To simplify the study, it is assumed that V_{ds} rises with a constant *dv/dt*. The displacement current of C_{p3} can hence be modeled by a constant dc current source I_{p3}. During the voltage rise time t_{rise}, V_{desat} can be modeled as a constant dc voltage source after neglecting the voltage divider, $R_{blk,}$ and high frequency oscillations in V_{desat}. Before high positive *dv/dt* occurs, V_{comp} is already clamped to V_{clamp}. With superposition theorem, V_{comp} in *s* domain can be calculated as:

$$V_{comp}(s) = V_{desat}(s)\frac{R_{d2}}{sC_dR_{d1}R_{d2} + R_{d2} + R_{d1}} + I_{p3}(s)\frac{R_{d1}R_{d2}}{sC_dR_{d1}R_{d2} + R_{d1} + R_{d2}} \quad (6.3)$$

In the equations in this section, the reference point of V_{desat} and V_{comp} is V_{clamp} (-5 V), unless their reference point is explicitly noted. $V_{desat}(s)$ is mainly determined by the displacement current flowing through C_{desat}, C_{p1}, and C_{p2}, which are named I_{desat}, I_{p1}, and I_{p2}, respectively. The equation of $V_{desat}(s)$ is expressed as (6.4).

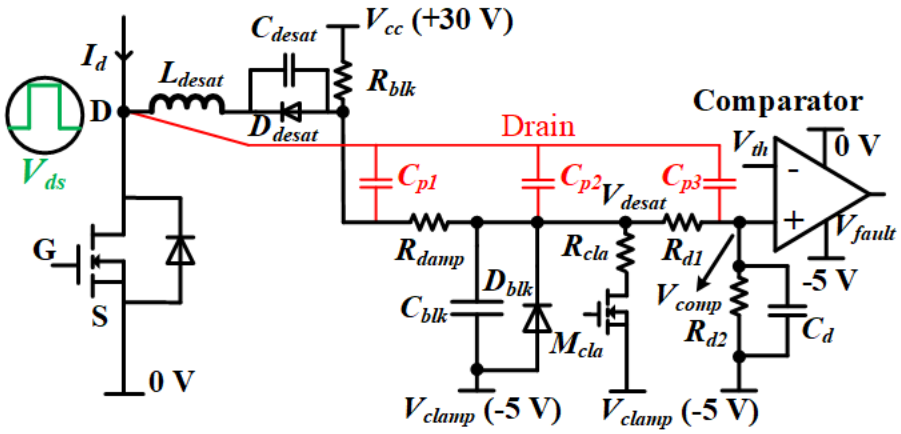


Fig. 6- 9. Desat protection circuitry considering parasitic capacitances between drain and protection circuitry.

$$V_{desat}(s) = \left(I_{desat}(s) + I_{p1}(s) + I_{p2}(s)\right)\frac{R_{cla}}{1 + sC_{blk}R_{cla}} \quad (6.4)$$

In equation (6.4), the effect of the voltage divider and R_{blk} is neglected because of their high impedance. The high frequency oscillation in V_{desat} is also neglected. Once the high *dv/dt* is generated, V_{desat} rises to a constant value quickly thanks to the extremely small time constant $R_{cla}C_{blk}$, which is usually much smaller than t_{rise}. Hence, V_{desat} can be modeled as a dc voltage source during the voltage rise time. V_{desat} is rewritten as:

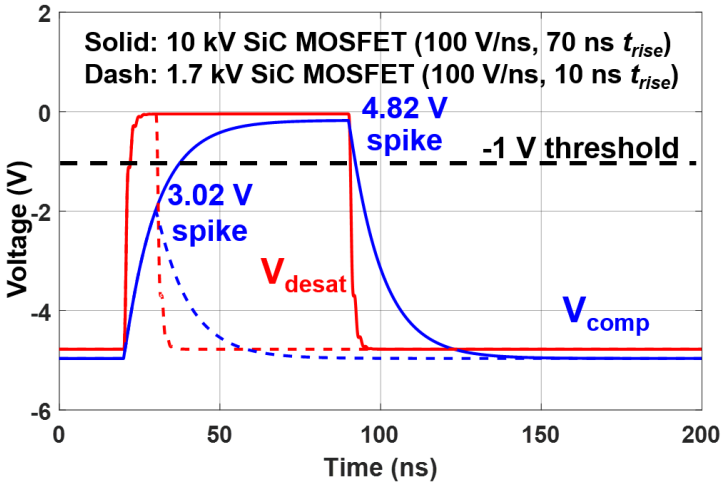
$$V_{desat} = R_{cla}\left(C_{desat} + C_{p1} + C_{p2}\right)\frac{dv}{dt} \quad (6.5)$$

Meanwhile, I_{p3} can also be modeled as a constant dc current source due to the constant *dv/dt* assumption. The peak voltage spike V_{spike} of V_{comp}, can be derived with (6.6), which is the value of $V_{comp}(t)$ at the end of the voltage rise time t_{rise}. The reference point of V_{spike} is also V_{clamp} (-5 V).

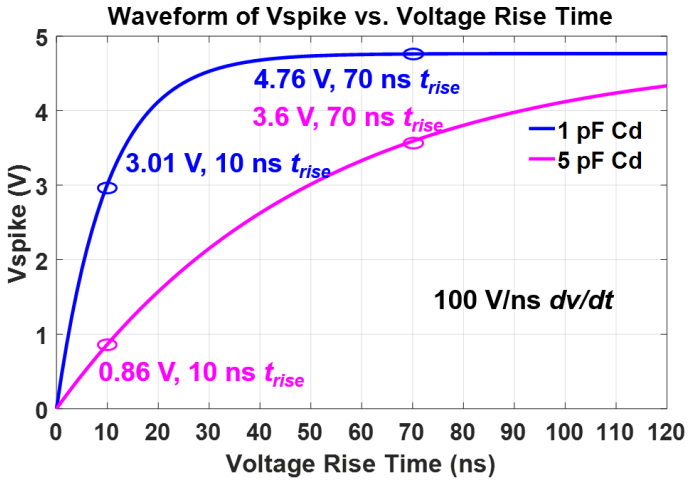
$$V_{spike} = V_{comp}(t_{rise}) = \left[R_{d1}C_{p3} + R_{cla}\left(C_{desat} + C_{p1} + C_{p2}\right)\right]\frac{R_{d2}}{R_{d1} + R_{d2}}\frac{dv}{dt}\left[1 - e^{\frac{-t_{rise}}{C_d(R_{d1}//R_{d2})}}\right] \quad (6.6)$$

High *dv/dt* with long voltage rise time generated by high voltage SiC MOSFETs can make the desat protection circuitry vulnerable to noise and spurious triggering. Fig. 6-10 shows that 0.004 pF C_{p3} induces a sufficiently high spike in V_{comp} which can falsely trigger the protection for 10 kV SiC MOSFETs in Fig. 6-4, which is 60% higher than that in 1.7 kV SiC MOSFETs with the same *dv/dt* and much shorter t_{rise}. In the simulation, C_{p1}, C_{p2}, and C_{p3} are 0 pF, 0 pF, and 0.004 pF, respectively, and C_{desat} is still modeled with a 2.3 pF capacitor.

With the established model of V_{spike} in (6.6), the impact of the voltage rise time t_{rise} can be analyzed quantitively, as plotted in Fig. 6-10(b). Longer t_{rise} results in higher spike in the comparator input voltage V_{comp}, making the protection more susceptible to spurious



(a)



(b)

Fig. 6- 10. (a) Simulation results of V_{desat} and V_{comp} with 0.004 pF C_{p3} and 1 pF C_d considered for 10 kV and 1.7 kV SiC MOSFETs with 100 V/ns *dv/dt*; (b) Calculation result of V_{spike} as a function of t_{rise}.

triggering. As t_{rise} becomes longer, V_{spike} starts to increase more slowly and eventually saturate. The maximum value of V_{spike} can be expressed as:

$$V_{spike,max} = \left[R_{d1}C_{p3} + R_{cla}\left(C_{desat} + C_{p1} + C_{p2}\right)\right]\frac{R_{d2}}{R_{d1} + R_{d2}}\frac{dv}{dt} \quad (6.7)$$

Fig. 6-10 also illustrates that the measured V_{spike} in simulation waveforms coincides well with the calculation result based on (6.6). However, if t_{rise} is not considerably longer than the time constant $R_{cla}C_{blk}$, V_{desat} cannot be modeled by a constant dc voltage source, and the expression of V_{spike} is modified as (6.8).

$$V_{spike} = \left[R_{d1}C_{p3} + R_{cla}\left(C_{desat} + C_{p1} + C_{p2}\right)\left(1 - e^{\frac{-t_{rise}}{C_{blk}R_{cla}}}\right)\right]\frac{R_{d2}}{R_{d1} + R_{d2}}\frac{dv}{dt}\left[1 - e^{\frac{-t_{rise}}{C_d(R_{d1}//R_{d2})}}\right] \quad (6.8)$$

Based on (6.8), the magnitude of V_{spike} as a function of voltage rise time and *dv/dt* is evaluated in Fig. 6-11, in which C_{p1}, C_{p2}, C_{p3}, and C_d are still 0 pF, 0 pF, 0.004 pF, and 1 pF, respectively. In terms of generating high V_{spike} in the desat protection circuitry based on discrete components, the worst case occurs when high *dv/dt* and long voltage rise time appear simultaneously. Thus, the desat protection of high voltage (> 3.3 kV) SiC MOSFETs with high *dv/dt* and longer duration is more vulnerable to noise generated by *dv/dt*, compared to other power semiconductor devices such as lower voltage (< 3.3 kV) SiC MOSFETs or 3.3 kV, 4.5 kV, and 6.5 kV Si IGBTs which are currently dominant in MV applications, as shown in Fig. 6-11.

6.1.2.3 Analysis of Comparator Input Voltage V_{comp} under Negative *dv/dt*

When negative *dv/dt* is generated, V_{comp} will also be shaped heavily by the displacement currents from parasitic capacitances, especially C_{desat} and C_{p3}. Different from

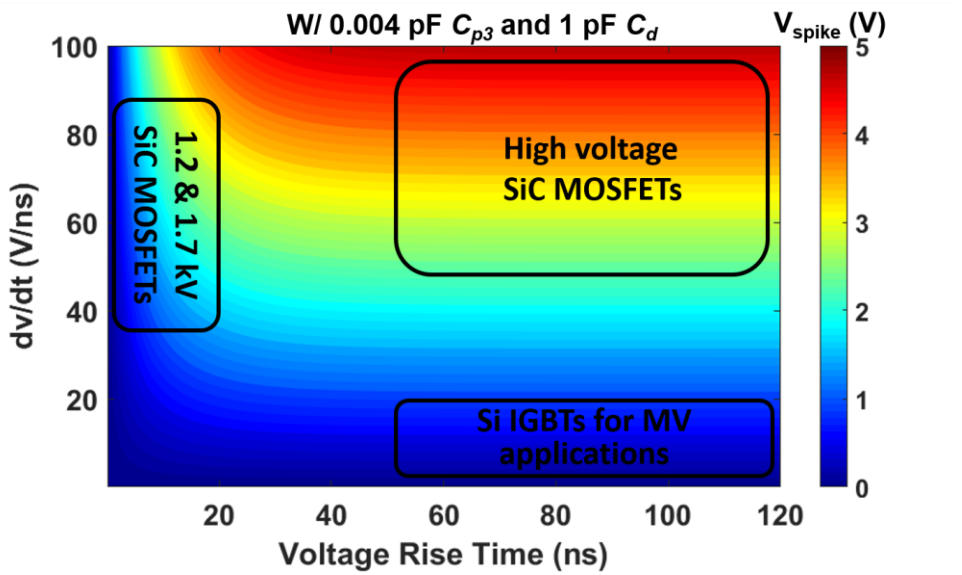


Fig. 6- 11. Contour plot of V_{spike} as a function of *dv/dt* and voltage rise time t_{rise}.

the case with positive *dv/dt*, V_{comp} is not necessarily clamped to V_{clamp} before negative *dv/dt* is generated, leading to different initial conditions. Yet, V_{comp} can still be analyzed with the analytical method used to study V_{comp} under high positive *dv/dt*.

To analyze V_{comp}, V_{desat} under negative *dv/dt* should be examined first to eliminate the nonlinearity brought by D_{blk}. The influence of C_{p3} on V_{desat} can be neglected, because C_{p3} is much smaller than C_{desat}. If zero voltage switching (ZVS) can be achieved with the high voltage SiC MOSFET, M_{cla} is already fully ON to clamp V_{comp} at V_{clamp} before negative dv_{ds}/dt occurs, and M_{cla} always has low impedance during the voltage fall time t_{fall}. In this case, $V_{desat}(t = +\infty)$, the final value of V_{desat} at the end of voltage fall time, is derived as follows, assuming t_{fall} is infinitely long.

$$V_{desat}(t = +\infty) = \frac{(V_{cc} - V_{clamp})R_{cla}}{R_{cla} + R_{blk}} + \left(C_{desat} + C_{p1} + C_{p2}\right)\frac{dv}{dt}R_{cla} \tag{6.9}$$

If the high voltage SiC MOSFET switches without any soft switching, M_{cla} will have high impedance during the entire voltage fall time, and $V_{desat}(t = +\infty)$ can be calculated as below.

$$V_{desat}(t = +\infty) = V_{cc} - V_{clamp} + \left(C_{desat} + C_{p1} + C_{p2}\right)\frac{dv}{dt}R_{blk} \tag{6.10}$$

In either case, V_{desat} will decline quickly and be clamped by the diode D_{blk} after the negative *dv/dt* is generated if $V_{desat}(t = +\infty)$ is much lower than zero due to the sufficiently high displacement current. In both cases, with the requirement in (6.11) satisfied, V_{desat} can be modeled as a constant dc voltage source, $-V_{diode}$, during the voltage fall time.

$$-\left(C_{desat} + C_{p1} + C_{p2}\right)\frac{dv}{dt} \gg \frac{V_{cc} - V_{clamp}}{R_{blk}} \tag{6.11}$$

where $\frac{dv}{dt}$ in the equation is negative. The minimum negative spike in V_{comp} at the end of the voltage fall time, $V_{spike,n}$, can be calculated with the following equations.

$$V_{spike,n} = V_{n,max} + (V_{ini} - V_{n,max})e^{\frac{-t_{fall}}{C_d(R_{d1}//R_{d2})}} \tag{6.12}$$

$$V_{n,max} = \frac{R_{d2}}{R_{d1} + R_{d2}}\left(R_{d1}C_{p3}\frac{dv}{dt} - V_{diode}\right) \tag{6.13}$$

V_{ini} is the initial value of V_{comp} when the voltage fall time starts. The reference point of $V_{spike,n}$ and V_{ini} is also V_{clamp}. In the cases where ZVS can be achieved, V_{ini} is 0 V. In the hard switching cases, V_{ini} is usually slightly higher than 0 V. With analysis based on parameters in Fig. 6-4 and 0 V V_{ini}, as shown in Fig. 6-12, the negative voltage spike becomes more substantial as the voltage fall time increases. As can be seen in (6.12) and (6.13), C_{p3} together with high negative *dv/dt* contributes to a large portion of the negative spike in V_{comp}, which makes V_{comp} much lower than the ground potential of the comparator during the voltage fall time. The duration of the negative spike increases as the voltage fall time becomes longer. The analytical results of $V_{spike,n}$ in Fig. 6-12 match well with the simulation results in Fig. 6-13. Simulation results also show that adding D_{blk} is not effective in reducing the negative spike in V_{comp} caused by the displacement current from C_{p3}. In general, higher negative *dv/dt* together with longer duration of *dv/dt* generates stronger interference on the comparator input voltage.

Therefore, high negative *dv/dt* with long duration generated by high voltage SiC MOSFETs leads to long negative transient input voltage in the desat comparator and poses a substantial challenge to the comparator's ability to withstand negative input voltage. To avoid false triggering due to the negative *dv/dt*, the phase reversal issue of the desat comparator must be tackled and is covered in the next subsection.

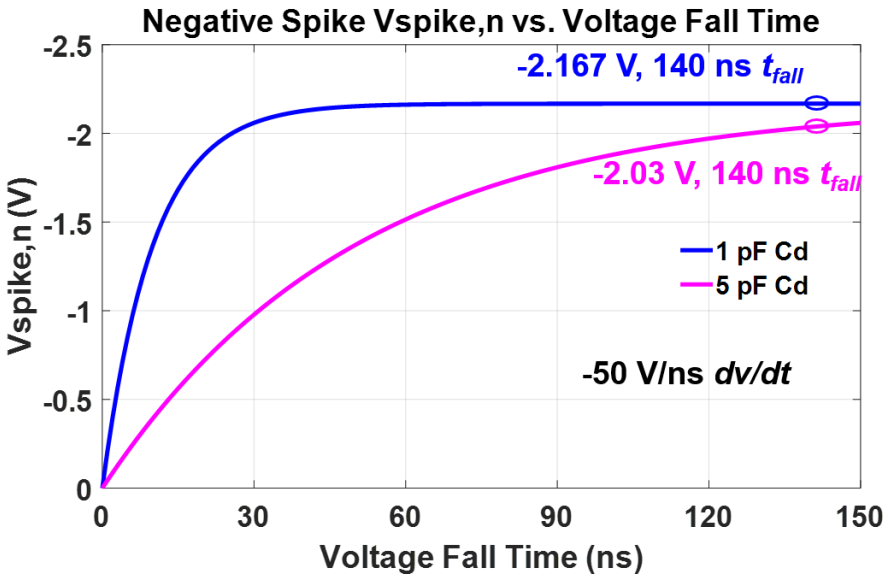


Fig. 6- 12. Calculation result of $V_{spike,n}$ under the negative dv/dt (-50 V/ns).

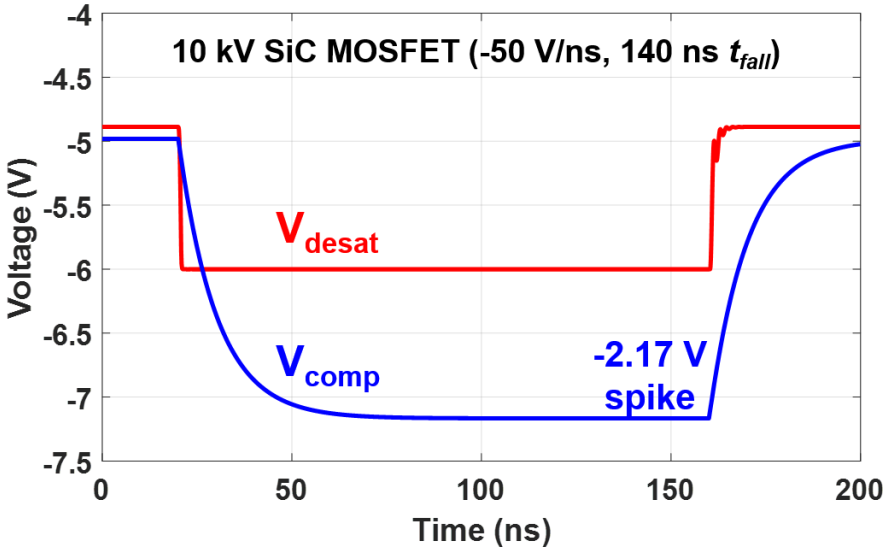


Fig. 6- 13. Simulation results of V_{desat} and V_{comp} with 0.004 pF C_{p3} and 1 pF C_d.

6.1.3 Noise Immunity Improvement

Positive dv_{ds}/dt can falsely trigger desat protection by generating positive voltage spikes in V_{desat} and V_{comp}. On the other hand, negative dv_{ds}/dt can falsely trigger the comparator and the desat protection by the phase reversal mechanism. Based on the two mechanisms of false triggering, this subsection discusses how to improve the noise immunity of the desat protection for high voltage SiC MOSFETs.

6.1.3.1 Desat Protection Realized with Gate Driver IC

To improve noise immunity under negative dv_{ds}/dt, a Schottky diode with low forward voltage drop should be selected for D_{blk}. The gate driver IC should be selected accordingly to ensure it can withstand V_{desat} without any phase reversal issue when D_{blk} is in conduction mode.

The analysis of V_{desat} in the previous subsection lays a solid foundation for noise immunity improvement under the positive dv_{ds}/dt. The peak positive spike in V_{desat} should be reduced during the voltage rise time. The design guidelines for better noise immunity are summarized in Table 11. The design guidelines in Table 11 have little influence on the protection response speed. Among the guidelines in Table 11, the top priority is to implement the desat diode with lower parasitic capacitance to suppress the displacement current. Then, the oscillations in V_{desat} can be alleviated by reducing L_{desat} and adding R_{damp}. After reducing C_{desat} and L_{desat} and adding R_{damp}, strong noise immunity should be achieved in most cases, unless the selected gate driver IC leads to a large R_{cla}. Selecting a gate driver IC with low R_{cla} is highly recommended, yet it is difficult to know R_{cla} based on the manufacturer's datasheet. Although increasing C_{blk} is also effective in reducing the peak

Table 11. Summary of design guidelines to improve noise immunity of desat protection realized by a gate driver IC

Guideline	**Detailed guideline**	**Design trade-off**
Reduce C_{desat}	Select or implement desat diode with as low parasitic capacitance as possible	Increasing cost and perhaps size
Reduce L_{desat}	Achieve lower parasitic inductance in PCB layout and connection	Case by case
Add R_{damp}	Use slightly higher R_{damp} if L_{desat} is more considerable; Requirement: $R_{damp} << R_{blk}$	No considerable trade-off; little impact on response time

of V_{desat} during the voltage rise time, it is not recommended to use a large C_{blk} to suppress oscillation in V_{desat} because that will lead to a long response time.

6.1.3.2. Desat Protection Based on Discrete Components

In the desat protection circuitry based on discrete components, we also readily improve noise immunity under the influence of negative *dv/dt*. One essential guideline is to select comparators without the phase reversal issue to avoid false triggering due to the negative spike in V_{comp}. In case it is uncertain whether the selected comparator can prevent phase reversal, a Schottky diode can also be installed to suppress a negative voltage spike in V_{comp}. Phase reversal is not an uncommon issue in comparators with traditional PNP-transistor input stage [101]. Nowadays, several comparators have a CMOS input stage and are designed to prevent phase reversal. On the other hand, op-amps and comparators with phase reversal issue should not be used in SiC-based MV converters with high *dv/dt*.

In terms of noise immunity improvement under positive *dv/dt*, the noise immunity margin V_{margin} in V_{comp} can be quantitatively calculated as follows.

$$V_{margin} = V_{th} - V_{clamp} - V_{spike} \tag{6.14}$$

V_{th} is the threshold voltage of the comparator. V_{th}-V_{clamp} is closely coupled with the threshold voltage of desat protection $V_{desat,th}$ and the voltage divider design. The reference point of V_{th} and $V_{desat,th}$ is 0 V. The quantitative analysis is as follows.

$$V_{th} - V_{clamp} = \left(V_{desat,th} - V_{clamp}\right)\frac{R_{d2}}{R_{d1} + R_{d2}} \tag{6.15}$$

V_{spike} can be calculated with (6.6), since high voltage SiC MOSFETs usually have long t_{rise}. Then, the expression of V_{margin} can be rewritten as:

$$V_{margin} = \frac{R_{d2}}{R_{d1}+R_{d2}}\left(V_{desat,th} - V_{clamp} - \left[R_{d1}C_{p3} + R_{cla}\left(C_{desat} + C_{p1} + C_{p2}\right)\right]\frac{dv}{dt}\left(1 - e^{\frac{-t_{rise}}{C_d(R_{d1}//R_{d2})}}\right)\right) \tag{6.16}$$

Noise immunity under high positive *dv/dt* can be improved by achieving a higher V_{th}-V_{clamp} and reducing V_{spike}. Since $V_{desat,th}$ is determined by the I-V characteristic and threshold current of the MOSFET, elevating $V_{th} - V_{clamp}$ will lead to a higher voltage divider ratio $\frac{R_{d2}}{R_{d1}+R_{d2}}$ and a higher V_{margin}. Comparators' capability of supporting a high V_{th}-V_{clamp} is critical when selecting the desat comparator. Hence, comparators with higher power supply voltage can support higher $V_{th} - V_{clamp}$ and noise immunity margin. For example, 5 V comparators are more preferable than 3.3 V comparators. Also, comparators with rail-to-rail input voltage range are suggested so that V_{th}-V_{clamp} can be as close to the power supply voltage of the comparator as possible.

Also, comparators with longer propagation delay contribute to better noise immunity of the desat protection, which aids in the comparator to not respond to the extremely short spikes in V_{comp}. Longer propagation delay of the comparator requires V_{comp} to maintain above comparator threshold voltage for a longer time in order to trigger the comparator. In other words, longer propagation delay leads to higher equivalent comparator threshold voltage. The voltage reference used as threshold voltage of the comparator should also be stable and immune from the impact of high *dv/dt*. The selection and design guidelines about the comparator are summarized in Table 12 to improve the noise immunity of the desat protection.

To reach higher noise immunity margin, V_{spike} can be suppressed by reducing R_{cla}, the parasitic capacitances, the voltage divider impedance, and increasing C_d. If R_{cla} is reduced from 20 Ω to 2 Ω in the desat protection design in Fig. 6-4, V_{spike} is decreased to 4.1 V with 14% reduction. The reduction is not significant because the noise immunity

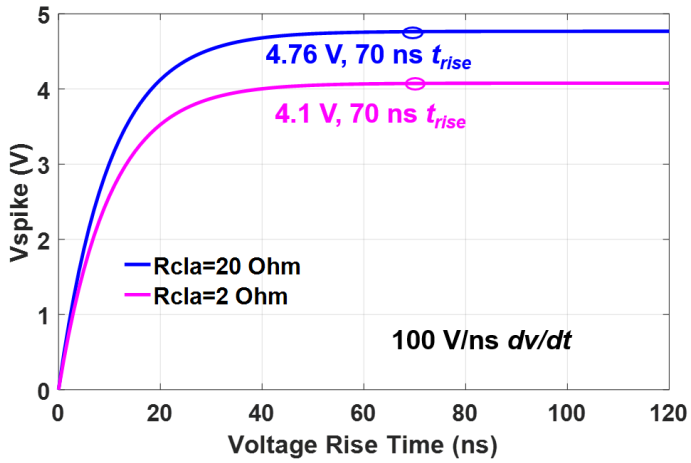
Table 12. Summary of selection and design guidelines for the comparator for noise immunity improvement

Parameter	**Selection or design guideline**
Power supply voltage	Higher power supply voltage is preferred
Input voltage range	Higher input voltage range is preferred
Propagation delay	Slightly longer propagation delay is preferred; Trade-off: longer delay leads to desat protection with slower response
Threshold voltage	Higher threshold voltage preferred; Filter capacitor added to stabilize threshold voltage
Phase reversal	Comparators without phase reversal issue should be selected; If not sure about phase reversal issue, a Schottky diode can be added to clamp V_{comp}
Pull-up resistance (only for comparators with open drain output)	Pull-up resistance should be small for better noise immunity

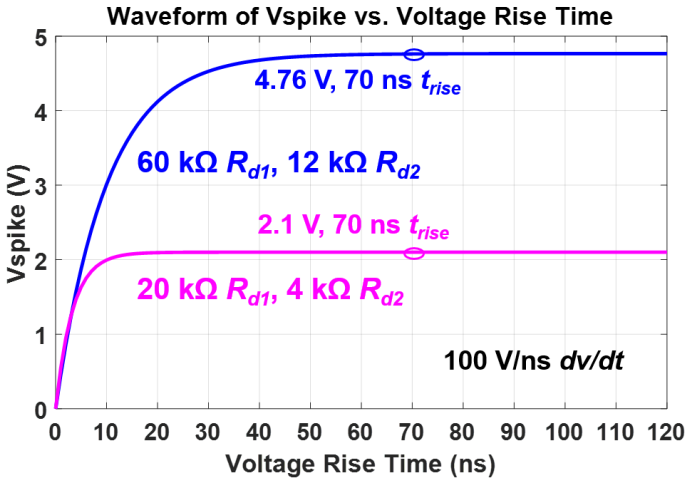
margin in this case is dominated by the displacement current from C_{p3}, instead of the displacement current from the desat diode. Therefore, if the voltage divider impedance is reduced by 67%, as shown in Fig. 6-14, V_{spike} can be reduced from 4.76 V to 2.1 V. If C_{p3} is suppressed to 0.001 pF, V_{spike} will be reduced to 1.8 V, with details shown in Fig. 6-15. Increasing C_d can also lower V_{spike} and improve the noise immunity. Fig. 6-10(b) demonstrates that V_{spike} is brought down to 3.6 V with 24% reduction by increasing C_d from 1 pF to 5 pF. Increasing C_d is more effective in improving noise immunity when t_{rise} is shorter, as indicated in the contour plot of V_{spike} in Fig. 6-16. With a long t_{rise}, a large C_d is needed to achieve significant reduction in V_{spike}, which will slow down the response of desat protection. When increasing C_d, the trade-off between response time and noise immunity should be considered.

Ac-dc continuous test of the half bridge phase leg based on 10 kV/20 A SiC MOSFETs is utilized to validate noise immunity methods based on discrete components [1]. Parameters of the desat protection implemented in the phase leg are displayed in Fig. 6-4. Voltage signals of the desat protection for the lower MOSFET are measured with a 1 GHz TPP1000 probe (3.9 pF input capacitance) [103]. Powered by 0 V and -5 V rails, ADCMP600 from Analog Devices is selected as the comparator based on the guidelines in Table 12 [104]. The comparator does not have a phase reversal issue and features an input common-mode voltage range beyond the power supply rails. So, the desat comparator will not be falsely triggered due to the interference of the negative dv_{ds}/dt.

Continuous test results at 6 kV dc link voltage in Fig. 6-17 show that the peak positive spike in V_{comp} is 2.56 V with an ideal V_{margin} of 1.44 V under the positive dv/dt.



(a)



(b)

Fig. 6- 14. Calculation result of V_{spike} as a function of t_{rise}: (a) Impact of R_{cla}; (b) Impact of voltage divider impedance.

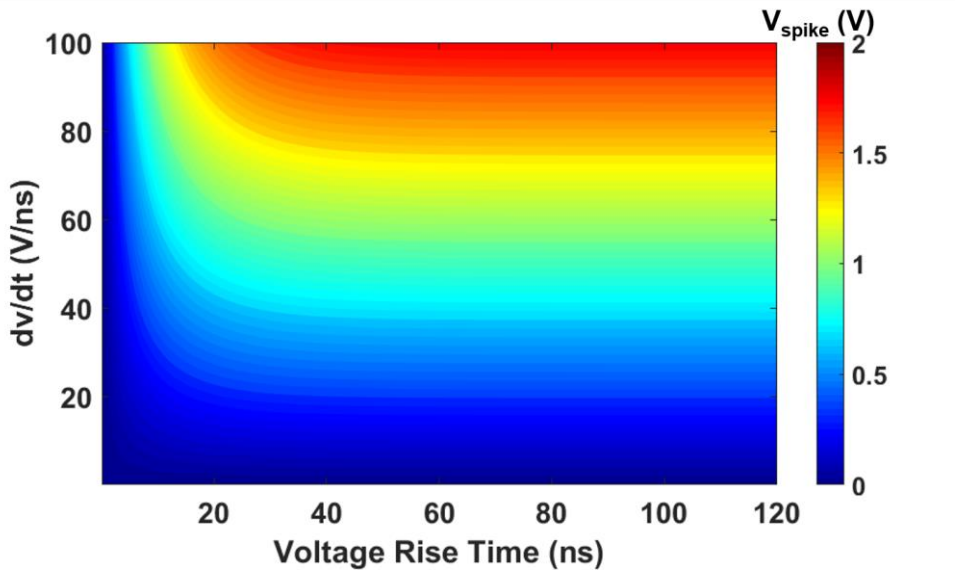


Fig. 6- 15. Contour plot of V_{spike} as a function of *dv/dt* and t_{rise} (0.001 pF C_{p3}).

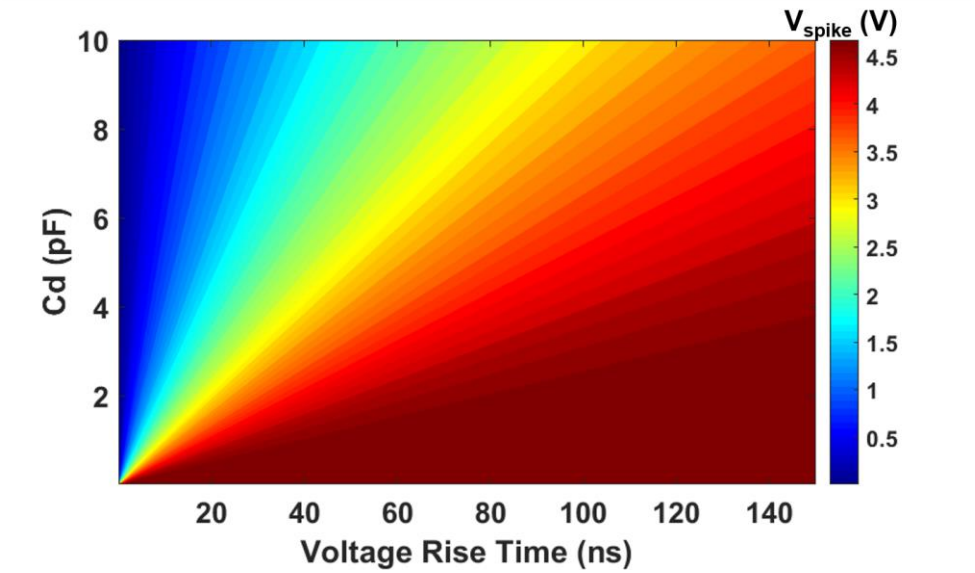


Fig. 6- 16. Contour plot of V_{spike} as a function of C_d and t_{rise} (0.004 pF $C_{p3;}$ 100 V/ns *dv/dt*).

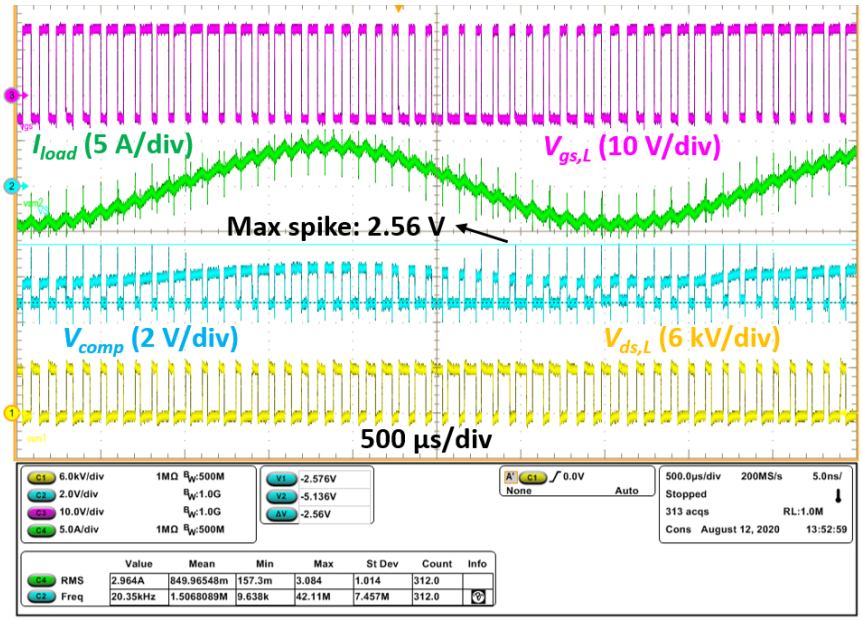
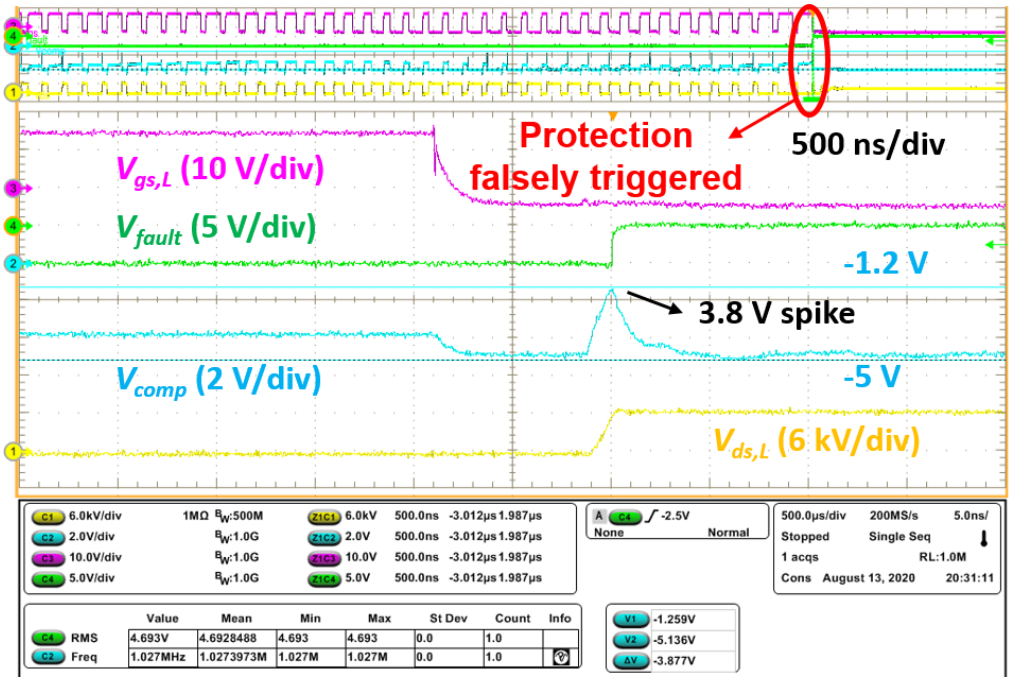


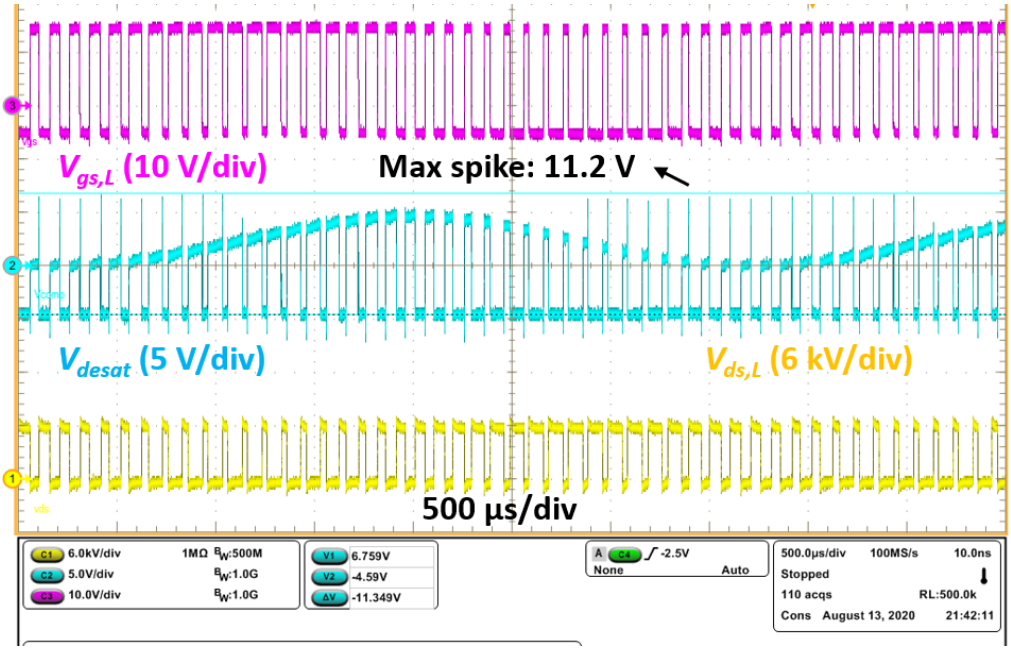
Fig. 6- 17. Waveforms of 6 kV continuous ac-dc test of a phase leg based on 10 kV SiC MOSFETs with desat protection in Fig. 6-4.

Selecting higher R_{cla} will reduce V_{margin} significantly. As shown in Fig. 6-18, the desat protection for the lower MOSFET is falsely triggered by the positive *dv/dt* (~65 V/ns) during the 6 kV ac-dc continuous test, with R_{cla} increased from 20 Ω to 90 Ω. The measured spike V_{spike} in V_{comp} which falsely triggers the protection is 3.8 V. The equivalent C_d is 5.3 pF with the input capacitance of the passive probe considered. From (6.3), we can see that V_{comp} is composed of two components. The measured peak voltage spike in V_{desat} is 11.2 V, which generates a positive spike of 1.55 V at V_{comp}. The remaining 2.25 V of the 3.8 V spike in V_{comp} is due to the displacement current from C_{p3}.

R_{d1} in the desat protection circuitry shown in Fig. 6-4 is implemented with two resistors in series, as illustrated in Fig. 6-19. Therefore, the drain terminal is coupled with the voltage divider via two parasitic capacitances, $C_{p3,a}$ and $C_{p3,b}$. $C_{p3,a}$ and $C_{p3,b}$ are mainly caused by the large drain plate of the 10 kV SiC MOSFET and the heatsink with the same potential as the drain plate [1], [91]. The finite element analysis in Ansys Q3D reveals that $C_{p3,a}$ and $C_{p3,b}$ are 0.0031 pF and 0.00131 pF, respectively. Based on the analysis in the previous subsection, the additional spike in V_{comp} due to $C_{p3,a}$ and $C_{p3,b}$ can be calculated as 1.54 V, which is slightly lower than the measured result, 2.25 V. The discrepancy is mainly because the Ansys Q3D analysis only extracts the parasitic capacitance caused by the drain plate and the heatsink. Other objects in the phase leg which have the same potential as the drain terminal of the MOSFET are not included in the Q3D model. In other words, the finite element analysis results still underestimate the capacitive coupling between the voltage divider and the drain terminal of the MOSFET.



(a)



(b)

Fig. 6- 18.Waveforms of 6 kV continuous ac-dc test of a phase leg based on 10 kV SiC MOSFETs with 90 Ω R_{cla}. (a) Waveform of V_{comp} when desat protection is falsely triggered. (b) Waveform of V_{desat}.

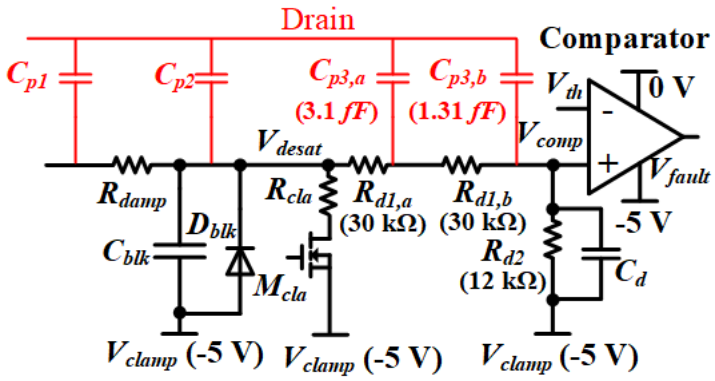


Fig. 6- 19. Details of capacitive coupling between the voltage divider in the desat protection circuitry and the drain terminal of the 10 kV SiC MOSFET.

To suppress the capacitive coupling between the protection circuitry and the drain terminal, an external copper shielding layer connected with the source of the MOSFET is installed beneath the desat protection circuitry, since the drain plate of the MOSFET and the heatsink are under the gate driver board. With 90 Ω R_{cla}, the copper shielding reduces the peak voltage spike in V_{comp} from 3.8 V to 2.2 V, and false triggering of desat protection is eliminated, as shown in Fig. 6-20. The experimental results also demonstrate that the parasitic capacitances caused by the drain plate and the heatsink result in 1.6 V spike in V_{comp}, which coincides well with the calculated value, 1.54 V. The role played by $C_{p3,a}$ and $C_{p3,b}$ in the generation of a positive voltage spike in V_{comp} is hence demonstrated. Shielding is also shown to be an effective method to suppress the noise propagated to desat protection circuitry via extremely small parasitic capacitances.

Based on the analysis and experimental results, a new iteration of desat protection circuitry is designed to further boost its noise immunity under high positive *dv/dt*. Numerous methods are adopted simultaneously in PCB layout and component selection. Compared to the design in Fig. 6-4, R_{d1} and R_{d2} are reduced by 66.7%, and R_{d1} is implemented by a single 20 kΩ resistor. R_{cla} is reduced from 20 Ω to 10 Ω. All components of the desat protection circuitry are placed on the top layer of the PCB, and thereby completely shielded by large grounding planes in the inner layers of the PCB. This PCB design not only significantly suppresses the influence from parasitic capacitances C_{p1}, C_{p2}, and C_{p3}, but also leads to parasitic capacitance which effectively increases C_d. According to Q3D analysis, the extracted C_{p3} is 0.82 fF, and inner shielding layers results in an

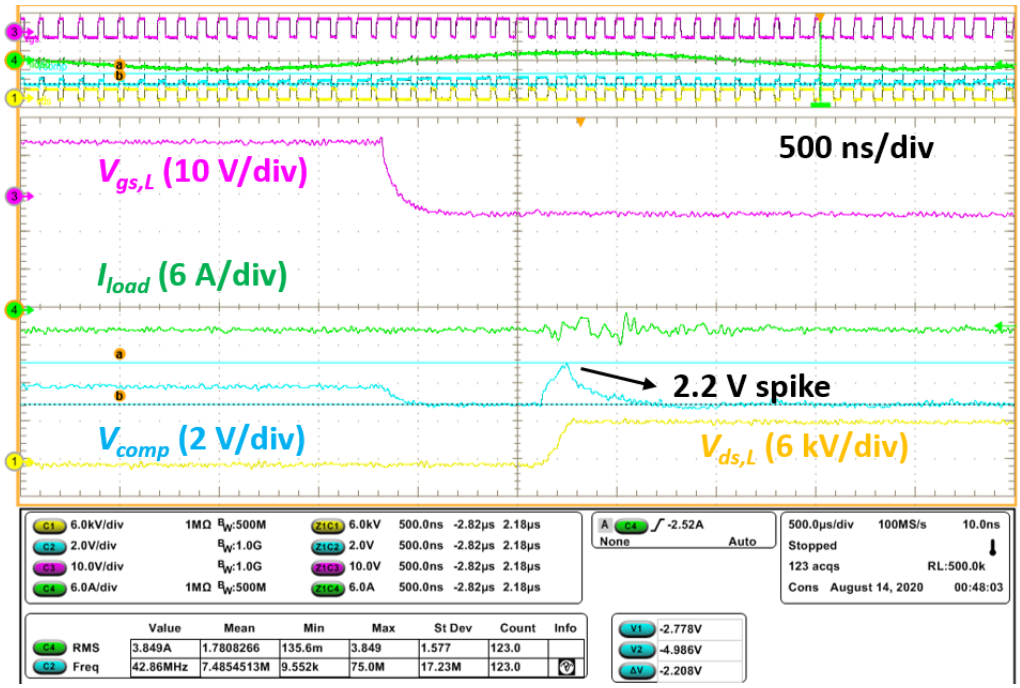


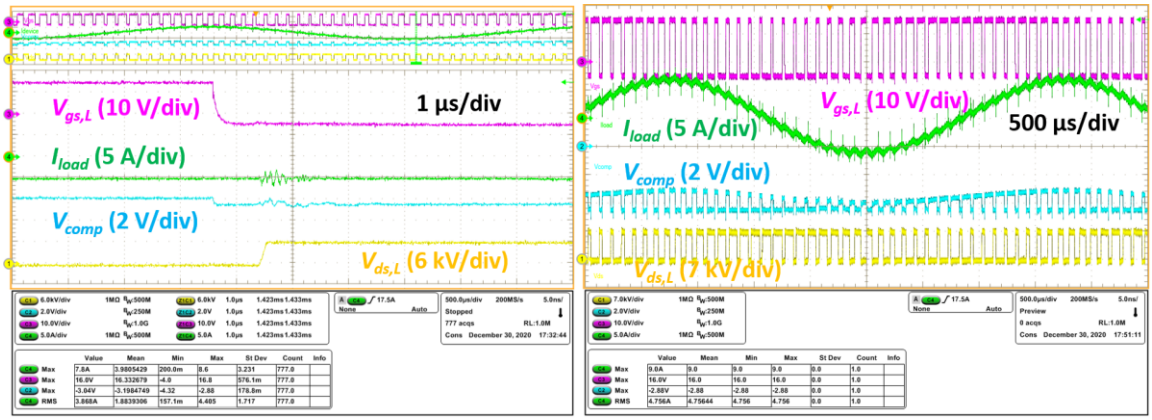
Fig. 6- 20. Waveforms of 6 kV continuous ac-dc test of a phase leg with 90 Ω R_{cla} and an external shielding layer installed.

increase of 1.3 pF in C_d. Further decreasing R_{cla} will benefit the noise immunity margin, but R_{cla} and M_{cla} could be damaged due to high instantaneous current if they are not selected carefully. According to the analytical model, the new iteration should achieve much higher noise immunity margin under +65 V/ns *dv/dt*, with V_{spike} reduced to 0.42 V.

Ac-dc continuous test results of the new desat protection design in Fig. 6-21 show that the spike in V_{comp} is significantly reduced. The measured peak spike in V_{comp} under the *dv/dt* of +65 V/ns is 0.5 V, which coincides well with the calculated result, 0.42 V. The voltage spike in V_{comp} is mainly caused by displacement current from the desat diode. Compared to the original design in Fig. 6-4, the noise immunity margin V_{margin} increases by 143%. The waveform of V_{comp} during 7 kV ac-dc continuous test reaffirms the substantial improvement of the new design in noise immunity.

Based on the theoretical analysis and experimental results, design guidelines to realize better noise immunity of the desat protection are summarized in Table 13. The design guidelines in Table 13 do not have substantial impact on the response speed of the desat protection, although some may slightly slow the protection response. Similar to the desat protection realized by a gate driver IC, it is not recommended to select larger C_{blk} to improve noise immunity of the desat protection based on discrete components. So, strong noise immunity and fast response do not contradict with each other. By following the design guidelines in Table 13, the response speed of the desat protection based on discrete components should only be limited by the blanking time requirement.

Fundamentally speaking, the noise coupled with the voltage divider usually plays a more dominant role, which has the capability of generating considerable voltage spike



(a) (b)

Fig. 6- 21. Waveforms of V_{comp} of new desat protection board with improved noise immunity: (a) 6 kV ac-dc continuous test; (b) 7 kV ac-dc continuous test.

Table 13. Summary of design guidelines to improve noise immunity of desat protection based on discrete components

Design guideline	**Detailed guideline**	**Design trade-off**
Reduce C_{p1}, C_{p2}, and C_{p3}	Design shielding layer and/or box when doing PCB layout	Slightly slower response due to slightly higher C_d
Reduce R_{d1}	Reduce voltage divider impedance	Slightly higher loss and slightly slower protection response
Reduce C_{desat}	Select or implement desat diode with as low parasitic capacitance as possible	Increasing cost and perhaps size
Reduce R_{cla}	Select a low R_{cla}	R_{cla} and M_{cla} need to handle higher pulse current
Reduce L_{desat}	Achieve lower parasitic inductance in PCB layout and connection	Case by case
Add R_{damp}	Use slightly higher R_{damp} if L_{desat} is relatively large Requirement: $R_{damp} << R_{blk}$	No considerable trade-off; little impact on response time
Increase C_d	Add a small external capacitor (<10 pF) to increase C_d	Slightly slower protection response

via extremely small parasitic capacitances (<0.01 pF) that are common in numerous MV phase legs and converters with different topologies. So, among the design guidelines in Table 13, two design guidelines related to the voltage divider are effective for numerous MV converters based on high voltage SiC MOSFETs and have a higher priority, including reducing voltage divider impedance and reducing C_{p3} by adding a shielding layer or box. Because of the high *dv/dt* with long duration, it is important to reduce C_{p3} as much as possible in MV converters based on high voltage SiC MOSFETs, even when it is already smaller than 0.01 pF.

6.1.4 Summary

Noise immunity of the desat protection for high voltage SiC MOSFETs is analyzed in this section. Two mainstream implementations of the desat protection are studied, including the desat protection circuitry based on discrete components and the implementation with a gate driver IC with integrated desat protection function. The desat protection can be falsely triggered by both high positive dv_{ds}/dt and negative dv_{ds}/dt generated by high voltage SiC MOSFETs. Because of the long duration of the high *dv/dt* generated by high voltage SiC MOSFETs, the extremely small parasitic capacitance (< 0.01 pF) coupled with the voltage divider could have large influence on the noise induced into the desat protection circuitry based on discrete components. Other factors' effects on noise are also studied, such as parasitic inductance, voltage divider impedance, damping resistance, and duration of high *dv/dt*.

The main concern with negative dv_{ds}/dt is the resulting negative voltage spike that can falsely trigger the desat comparator with the phase reversal issue. Hence, the noise

immunity under the negative dv_{ds}/dt can be improved by selecting comparators without phase reversal issue and adding clamping diodes.

The more challenging issue is the high positive dv_{ds}/dt, which lasts for a much longer time than that generated by 1.2 kV and 1.7 kV SiC MOSFETs. The analytical model of the noise immunity margin is established to support the noise immunity improvement under high positive dv/dt. The noise immunity analysis and improvements are supported by simulation and experimental results. Different methods and their experimental validation based on the derived noise immunity margin are presented to enhance the noise immunity. Comprehensive design guidelines to boost noise immunity are summarized, including circuit design, component selection, and PCB layout. None of the design guidelines recommended in this dissertation to improve noise immunity will slow the protection response significantly, and hence can be fully leveraged when designing the desat protection with fast response and strong noise immunity.

6.2 Improved Desat Protection with Digital Blanking Time

In this section, an improved desat protection scheme is designed to achieve fast response in overcurrent/short circuit conditions, while also featuring strong noise immunity and simple implementation. The response time in this chapter is defined as the time it takes for the device current to start to decrease after it exceeds the threshold current.

6.2.1 Working Principles

Details of the improved desat protection scheme are provided in Fig. 6-22. The fundamental idea is the same as the conventional desat protection for SiC MOSFETs, which is to monitor V_{ds} and output V_{desat} to indicate the device current. Once the overcurrent

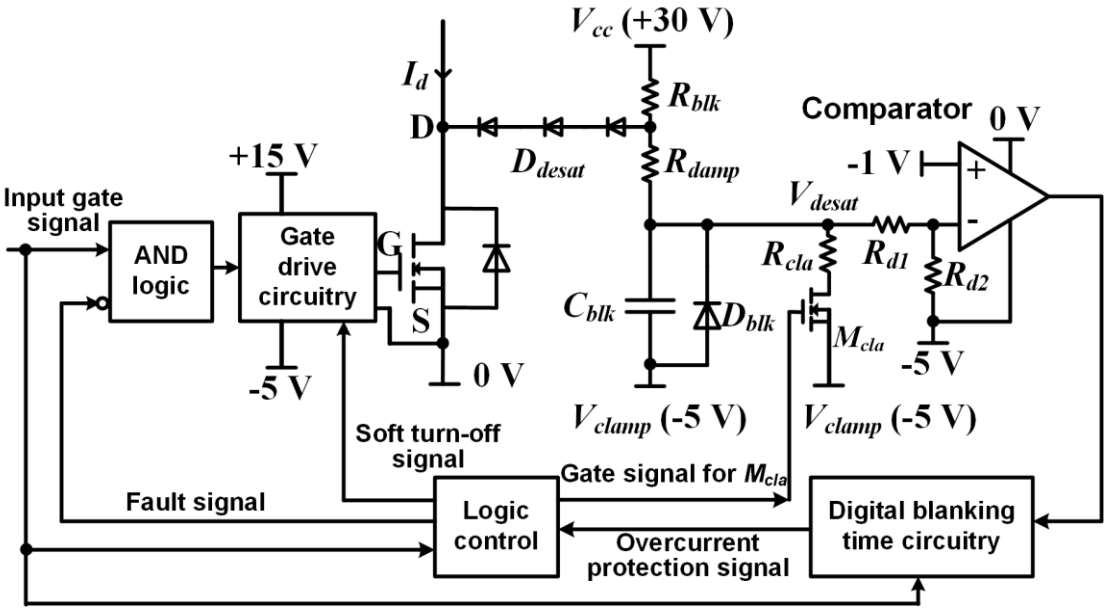


Fig. 6- 22. Improved desat protection in the gate driver for 10 kV SiC MOSFETs.

protection signal is generated, an SR latch will lock the signal and output a fault signal to activate the soft turn-off of the MOSFET and notify the controller.

Response time of the conventional desat protection is mainly determined by the blanking time to avoid false triggering during the turn-on transient [66]. Based on DPT results in Fig. 3-10, 10 kV/20 A SiC MOSFETs require a blanking time longer than 550 ns to ensure that V_{ds} reaches steady state. With the conventional desat protection scheme which is adopted in the baseline phase leg design in Chapter 3, a relatively large blanking capacitor C_{blk} is selected to provide a long blanking time (> 550 ns), leading to long response time in all types of short circuit faults [61], including HSF, FUL, and flashover fault.

The improved desat protection scheme utilizes the digital blanking time to enable the use of a small blanking capacitor C_{blk}. The blanking time is realized by digital ICs and hence is independent of C_{blk}. A 600 ns digital blanking time is designed after the rising edge of the input gate signal of the gate driver IC to disable the output signal from the desat comparator. In other words, even if the comparator output voltage flips during the 600 ns digital blanking time, the protection will not be triggered since the protection is equivalently disabled by the blanking time. A Zener diode D_{blk} with sufficient power rating ensures V_{desat} lower than 21 V to protect the comparator.

The screening effect is only effective for 600 ns after the rising edge of the gate signal for gate driver IC. During the normal turn-on transient, V_{ds} of the MOSFET has already reached steady state when the digital blanking time expires, thus the protection will not be falsely triggered. If the digital blanking time is much shorter than 550 ns, overcurrent protection might be triggered immediately after the digital blanking time expires.

With the digital blanking time, a small blanking capacitor is used to enable V_{desat} to follow V_{ds} quickly when the MOSFET is fully on, leading to fast response when a FUL or a flashover fault happens. In other words, the response time when a FUL or a flashover fault happens is no longer influenced by the required blanking time. The response time under a HSF is still strongly impacted by the length of the digital blanking time. If a HSF occurs, the protection will be triggered immediately after the digital blanking time is over. If the digital blanking time is longer, the time it takes to clear the fault will be longer.

6.2.2 Implementation

The improved desat protection scheme with 600 ns digital blanking time is implemented with numerous digital ICs. The protection scheme can be easily realized with a microcontroller, yet the gate driver is not equipped with a microcontroller. Instead, the digital blanking time and other digital signals of the protection scheme are generated by logic ICs and delay ICs.

When implementing the protection scheme, it is necessary to generate a signal to screen the output signal from the comparator to realize the 600 ns digital blanking time. The designed signal with digital blanking time is output by a XOR logic gate, and the details can be seen in Fig. 6-23. One input of the XOR gate is the initial gate signal with 1 μs delay. The other input of the XOR gate is the gate signal after the 400 ns dead time insertion, which is the final gate signal for gate driver IC during normal operation. The signal with digital blanking time stays HIGH for 600 ns after the rising edge of gate signal for gate driver IC, and then stays LOW as long as gate signal is still HIGH. It is able to disable the signal from desat comparator to realize digital blanking time since they both are sent to an OR logic

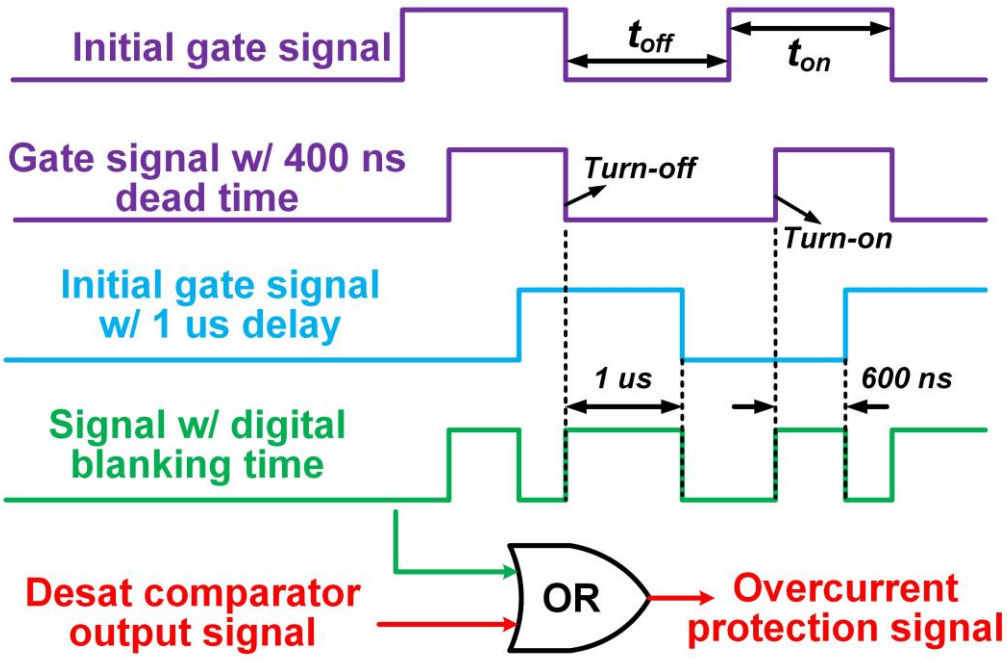
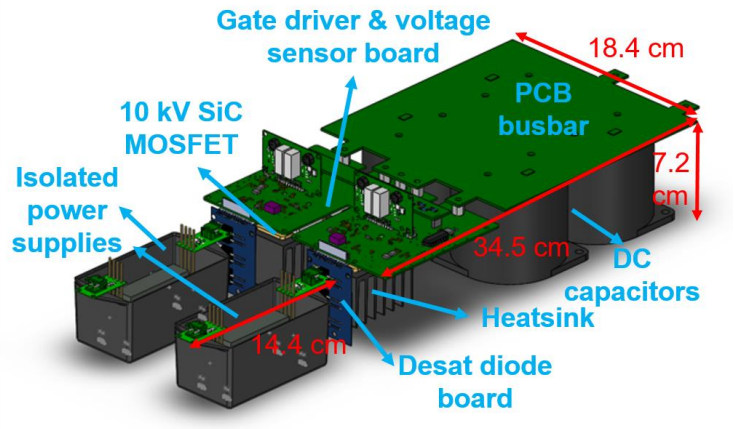


Fig. 6- 23. Implementation details of 600 ns digital blanking time.

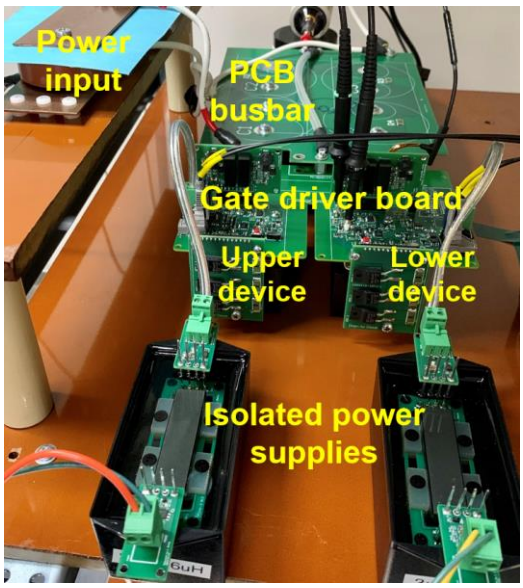
gate. Thereby, even if the desat comparator outputs LOW during the 600 ns blanking time, the overcurrent protection signal stays HIGH, and the fault signal will not be generated.

Such implementation scheme of 600 ns digital blanking time also screens the comparator output signal for 1 μs after the falling edge of gate signal. As shown in Fig. 6-23, the signal with digital blanking time from an XOR gate maintains HIGH for 1 μs after the falling edge of gate signal. In fact, overcurrent protection is not required when the MOSFET is turned off. Moreover, such effect also eliminates false triggering during the fast turn-off transient with high positive *dv/dt* and leads to better noise immunity. One disadvantage is that such implementation requires the MOSFET to stay OFF for at least 600 ns, otherwise the signal with digital blanking time can be wrong. This requirement sets an upper limit for the duty cycle of the MOSFET, which is 94% when the switching frequency is as high as 100 kHz.

The 10 kV desat diode D_{desat} is realized by the series connection of three 3.3 kV SiC Schottky diodes (GAP3SLT33-220FP) [87]. Each SiC diode is in parallel with a 50 MΩ/4 kV resistor (HVC4020V5005JET from Ohmite) to ensure voltage balancing during steady state and switching transients. Also, insulation design for the 10 kV desat diode usually results in increased gate driver footprint, as can be seen in Fig. 3-2. To overcome this drawback, a daughterboard perpendicular to the motherboard is designed to accommodate the 10 kV desat diode, in which diodes are soldered as surface-mount devices, as shown in Fig. 6-24(a). A high voltage wire is used to connect the daughterboard with the drain terminal of the MOSFET. The daughterboard is coated with insulating material (Super Corona Dope) to reduce the insulation distance requirement. Hence, the desat diode does



(a)



(b)

Fig. 6- 24. (a) Detailed 3D design of the phase leg. (b) Prototype of half bridge phase leg with improved desat protection in high voltage test platform.

not increase the gate driver footprint and the volume of the phase leg. Series connection of SiC diodes also effectively reduces the parasitic capacitance C_{desat}. 3 V voltage drop of the desat diode should be considered when determining the threshold voltage. Based on the I-V characteristic of the 10 kV SiC MOSFET, the designed protection threshold is 15 V, leading to 20 A threshold current at 125 ˚C and 42.85 A threshold current at 25 ˚C. The final threshold voltage is 18 V to compensate the 3 V voltage drop of the desat diode.

6.2.3 Discussions of Response Time

The improved desat protection scheme has fast response when a FUL or flashover fault happens, depending on how fast V_{desat} can follow V_{ds}. When a HSF happens, the response time is mainly determined by the length of digital blanking time. If a longer digital blanking time is implemented, response to clear a HSF will be slower, while the response time under a FUL or a flashover fault will not be influenced. Therefore, tuning R_{blk}, R_{damp}, and C_{blk} only changes the response time under the FUL or flashover fault.

With the improved desat protection scheme, the response time under the FUL and flashover fault is adjusted by changing R_{blk} and C_{blk}. A 90 Ω R_{damp} is introduced to dampen the oscillations. Under the FUL or flashover fault, the capability of V_{desat} to track V_{ds} depends on C_{blk} and I_{chg}, the current available to charge C_{blk}. To achieve faster tracking speed and shorter response time, a small C_{blk} and a high I_{chg} are desired, and I_{chg} can be calculated as follows.

$$I_{chg} = \frac{V_{cc} - V_{desat}}{R_{blk} + R_{damp}} - \frac{R_{blk}}{R_{blk} + R_{damp}} I_{desat} \tag{6.17}$$

V_{cc} in the equation is the power supply voltage, +30 V, and I_{desat} is the displacement current of the desat diode. A smaller R_{blk} and a V_{cc} higher than +30 V lead to faster response, but the power loss of R_{blk} when the 10 kV SiC MOSFET is turned off also rises.

Under the flashover fault and the FUL with high positive dv_{ds}/dt at the beginning of the fault, the desat diode almost immediately becomes reverse biased, and all current from V_{cc} is used to charge C_{blk}. Under the flashover fault with extremely high dv_{ds}/dt and di/dt, I_{desat} turns zero and then its direction changes within several nanoseconds. Assuming that the short circuit current reaches the peak when V_{gs} starts to drop, the response time in this case can be estimated as follows.

$$V_{desat}(t) = \left[\frac{(V_{cc} - V_{clamp})R_{blk,eq}}{R_{blk}} + V_{clamp} - V_{ini,d}\right]\left(1 - e^{\frac{-t}{C_{blk}R_{blk,eq}}}\right) + V_{ini,d} \tag{6.18}$$

$$t_{res} = C_{blk}R_{blk,eq}\ln\left[\frac{(V_{cc} - V_{clamp})R_{blk,eq} + R_{blk}(V_{clamp} - V_{ini,d})}{(V_{cc} - V_{clamp})R_{blk,eq} + R_{blk}(V_{clamp} - V_{desat,th})}\right] \tag{6.19}$$

In the equations, $R_{blk,eq}$ ($R_{blk,eq}$ = R_{blk} // (R_{d1}+R_{d2})) is the parallel resistance of R_{blk} and R_{d1}+R_{d2}. C_{blk} should be the total capacitance between V_{clamp} and V_{desat}, including the parasitic capacitances. $V_{ini,d}$ is the value of V_{desat} right before the fault happens. The impact of the positive dv_{ds}/dt during the fault is also neglected.

In terms of the FUL, the other case is that the desat diode is still in conduction mode at the beginning of the fault. As the short circuit current accumulates, V_{ds} increases accordingly without a high dv/dt, so V_{desat} also rises. When the short circuit current reaches the threshold current, V_{desat} is already close to the protection threshold voltage $V_{desat,th}$, significantly higher than $V_{ini,d}$ in the equation (6.19). Thereby, the response time under this kind of FUL is significantly shorter than the response time calculated with (6.19).

Finally, 12 pF C_{blk} and 3.25 kΩ R_{blk} are selected for the improved desat protection scheme to secure <200 ns response time under the FUL and the flashover fault. The estimated response time is 139.5 ns based on (6.19), assuming 3 V $V_{ini,d}$ at 0 A device current. R_{blk} will have 377 mW power loss when the MOSFET is off. Under the FUL and flashover fault with high positive dv_{ds}/dt, the considerable I_{desat} makes the response time even shorter. If the flashover fault happens when the device current is negative, the response will be slightly slower. Generally, <200 ns response time under the FUL and flashover fault can be guaranteed.

6.2.4 Experimental Results

Captured waveforms of the lower MOSFET of the phase leg under HSF short circuit fault can be seen in Fig. 6-25. When conducting the HSF short circuit test, the upper MOSFET is shorted with a high voltage wire with a parasitic inductance of 171 nH. The improved desat protection responds immediately after the 600 ns digital blanking time expires, triggering the soft turn-off process. The turn-off di/dt is -0.438 A/ns leading to small voltage overshoot in V_{ds}. The short circuit response time is 340 ns, and the total short circuit energy loss is 178 mJ. Before the protection is triggered, V_{desat} has already exceeded the 18 V protection threshold voltage, proving the effectiveness of the digital blanking time. The digital blanking time is slightly shorter than 600 ns, which is likely owing to the propagation delay in the gate driver IC.

Fig. 6-26 displays the test result of the same phase leg under FUL fault at 6.5 kV. When both MOSFETs are turned off, the measured V_{ds} of the lower MOSFET is ~2 kV, lower than $V_{dc}/2$, because the lower MOSFET of the phase leg has lower leakage resistance

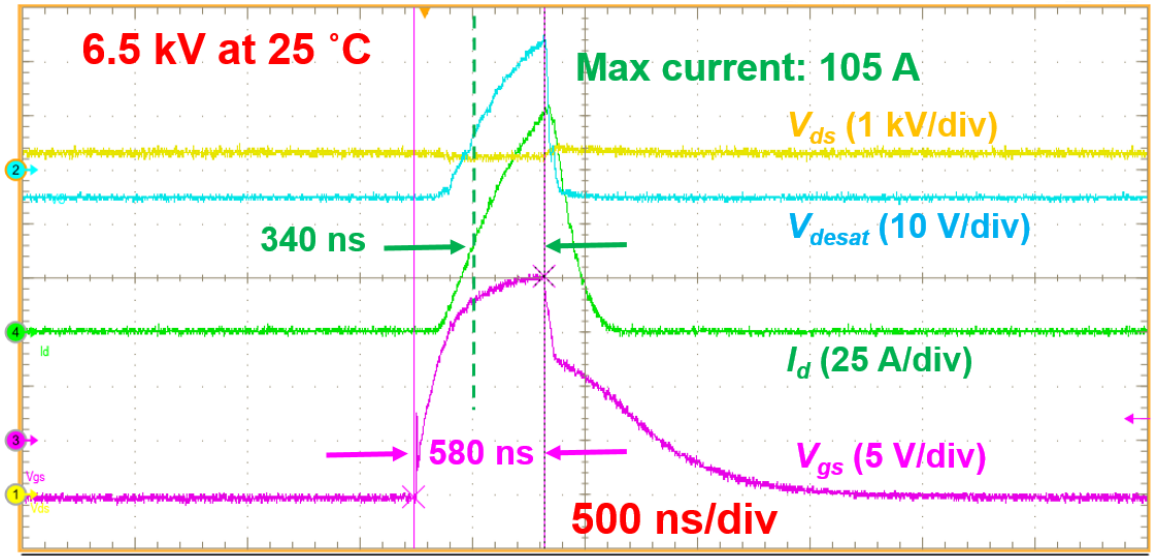


Fig. 6- 25. HSF short circuit test waveform of lower MOSFET in the phase leg.

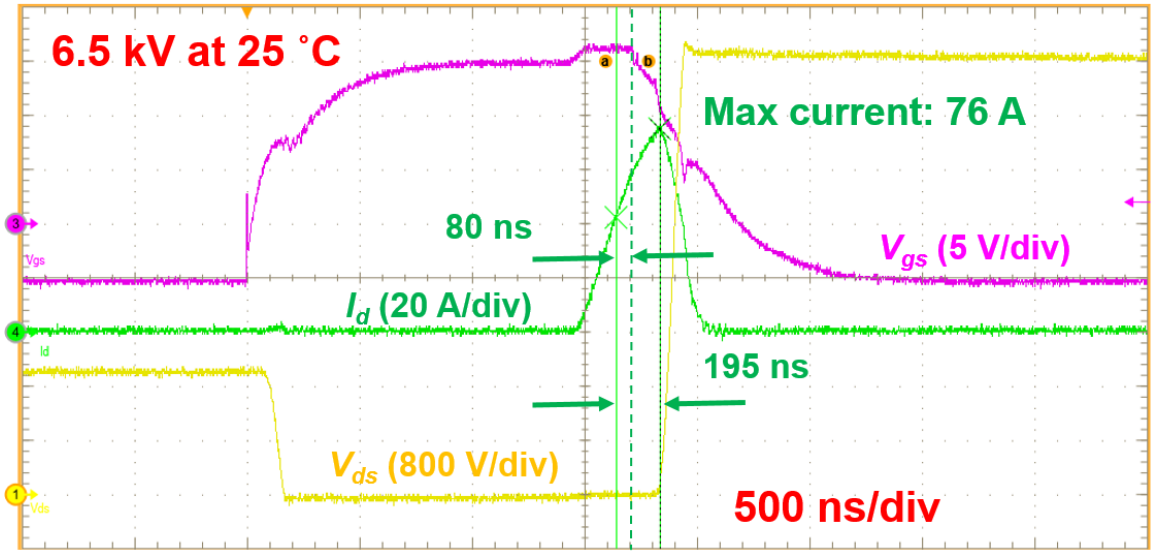


Fig. 6- 26. FUL short circuit test waveform of lower MOSFET in the phase leg.

than the upper MOSFET. A FUL fault is generated by turning on the upper MOSFET when the lower MOSFET is already in ON state. As short circuit current increases rapidly, V_{ds} of the lower device and V_{desat} rise accordingly, while most of dc-link voltage occurs across the upper MOSFET under a HSF fault. After 290 ns, V_{gs} starts to decrease to turn off the device, and meanwhile the short circuit current continues to increase. V_{ds} does not increase with high *dv/dt* (66 V/ns) until the short circuit current starts to drop. In this case, the displacement current caused by *dv/dt* has little impact on V_{desat} before the protection is triggered.

The measured response time under the FUL fault is 195 ns thanks to the small C_{blk}. Under this kind of FUL fault, the measured waveforms show that the short circuit current continues increasing for 115 ns after soft turn-off process is initiated. In this kind of FUL fault, it is difficult to estimate the response time because of difficulty in predicting when the short circuit current reaches the peak. The peak short circuit current is 76 A, significantly lower than that under HSF fault. The total power loss is 29.77 mJ, including the turn-off loss. Also, the measured V_{gs} waveform is distorted by the voltage drop on the common source inductance L_{ss}. When the short circuit current increases, the positive voltage drop on L_{ss} results in the measured V_{gs} higher than 15 V. Voltage drop on L_{ss} also changes drastically when short circuit current reaches the peak, since the *di/dt* changes from 0.24 A/ns to -0.4 A/ns.

Unfortunately, there is no experimental setup available in the lab for a flashover fault test with an extremely high *dv/dt*. Since <200 ns response time has been verified in

the FUL fault test, similar response should also be achieved under the flashover fault, and the higher positive dv_{ds}/dt during the flashover fault could lead to shorter response time.

Continuous test of the phase leg is conducted to fully qualify the noise immunity of the improved desat protection. In the continuous ac-dc test, the HB phase leg is configured as an inverter with the fundamental frequency of 300 Hz, the same as the continuous test in the baseline test in Chapter 3 [1]. Fig. 6-27 displays the continuous test waveform at 6.5 kV. The total dead time is 600 ns with 200 ns dead time generated by the controller. The modulation index is 0.55 to output the load current with the peak value of ~6 A. V_{desat} used for overcurrent protection also has a sinusoidal shape, indicating that it is able to follow V_{ds} quickly when the MOSFET is in ON state. It can also be seen that V_{desat} is clamped at -5 V when MOSFET is turned off. Successful ac-dc continuous switching test demonstrates the excellent noise immunity of the improved desat protection.

6.3 Desat Protection with Ultrafast Response

This section presents a desat protection scheme with ultrafast response for 10 kV SiC MOSFETs. Its working principle is the same as the conventional desat protection for the 10 kV SiC MOSFET, yet its blanking time is designed by fully considering the influence of negative dv_{ds}/dt during its fast turn-on transient. Meanwhile, the noise immunity is not impaired by following the design guidelines in Section 6.1. In this section, the 10 kV/20 A SiC MOSFET is used as an example to illustrate this desat protection scheme with ultrafast protection [1]. The desat protection scheme can also be designed to protect other high voltage SiC MOSFETs from short circuit/overcurrent faults.

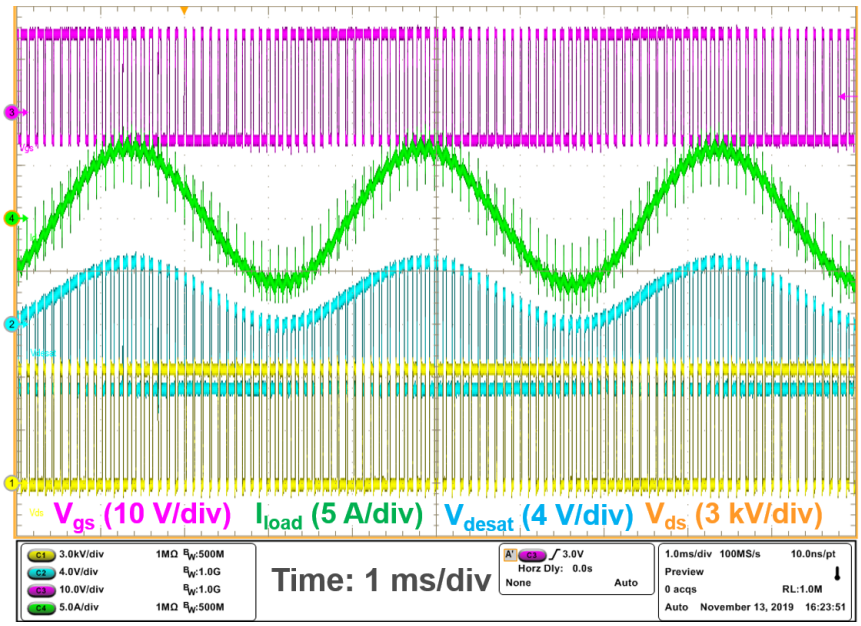


Fig. 6- 27. Waveforms of ac-dc continuous test at 6.5 kV.

6.3.1 Working Principles

One advantage of the proposed desat protection scheme with ultrafast response is that it has the same circuitry as the conventional desat protection. Fig. 6-28 shows the circuit diagram of the desat protection with ultrafast response for the 10 kV/20 A SiC MOSFETs, the same as the desat protection introduced in Chapter 3.

The blanking time is required in desat protection to prevent false triggering during the turn-on transient. Usually it is assumed that V_{desat} will be dominated by the capacitive charging process during the blanking time. Based on this assumption, the waveform of V_{desat} is drawn in Fig. 6-29(a). After V_{gs} starts to rise, V_{desat} will still be clamped at V_{clamp} for a time interval t_{cla} since it takes time to turn off M_{cla}. t_{cla} can be adjusted by tuning $R_{goff,cla}$, the turn-off gate resistance of M_{cla}. After M_{cla} is turned off, V_{desat} will keep increasing as the charging process goes on. The length of blanking time t_{blk} can be expressed as follows.

$$t_{blk} = t_{cla} + t_{RC} \tag{6.20}$$

In the equation, t_{RC} is the time interval it takes for V_{desat} to rise from V_{clamp} to $V_{desat,th}$ as a result of R-C charging process. To avoid false triggering during the blanking time, the conventional desat protection possesses a R-C network with a large time constant so that V_{desat} is always lower than $V_{desat,th}$ during the blanking time [1], [66]. The improved desat protection in Section 6.2 introduces the digital blanking time so that desat protection is effectively disabled during the blanking time.

However, the assumption is not valid during the fast turn-on transients of high voltage SiC MOSFETs. High dv_{ds}/dt with long duration during the turn-on transients has not been considered, which also plays a critical part in shaping V_{desat} via the parasitic

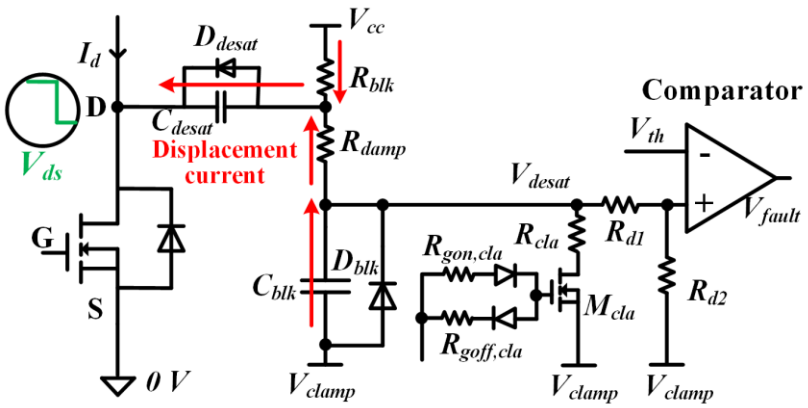
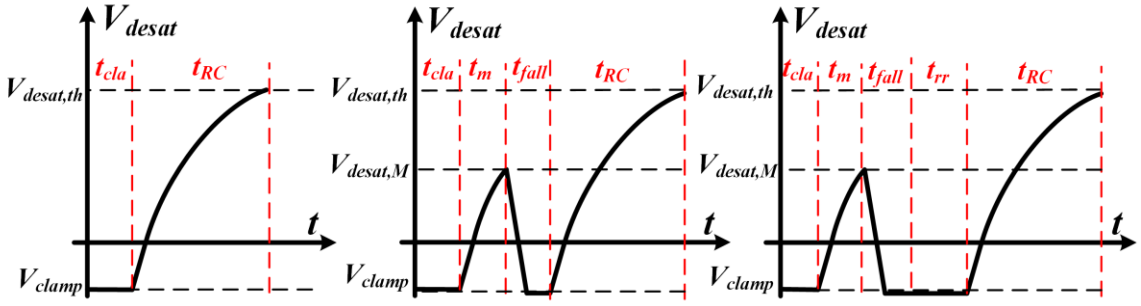


Fig. 6- 28. Circuit diagram of desat protection with ultrafast response for 10 kV/20 A SiC MOSFET



(a) (b) (c)

Fig. 6- 29. Waveforms of V_{desat} during blanking time: (a) impact of high *dv/dt* neglected; (b) reverse recovery process neglected; (c) both high *dv/dt* and reverse recovery considered.

capacitance C_{desat}. The high dv_{ds}/dt during the normal turn-on transient is negative and generates the displacement current that should be sourced by the desat protection circuitry as displayed in Fig. 6-28. As a result, V_{desat} will be heavily shaped by high negative dv_{ds}/dt during the blanking time.

The normal turn-on transients of high voltage SiC MOSFETs have high *dv/dt* for low switching loss and hence draws a large displacement current $C_{desat}dv_{ds}/dt$. Typically, the current provided by V_{cc} in desat protection is too low to supply the required displacement current. Once high *dv/dt* is generated during the normal turn-on transients, V_{desat} will stop rising and start decreasing as C_{blk} is discharged to provide $C_{desat}dv_{ds}/dt$. Because of the long duration of voltage fall time and small C_{blk} with limited stored charge, C_{blk} will be discharged quickly, and the diode D_{blk} will be forward biased to clamp V_{desat} until the voltage fall time with high *dv/dt* ends. In this case, at the end of the voltage fall time, V_{desat} is reset to its original value if the forward voltage drop of D_{blk} is neglected. The real blanking time t_{blk} after considering the effect of high *dv/dt* during the fast turn-on transient of high voltage SiC MOSFETs is as follows.

$$t_{blk} = t_{cla} + t_m + t_{fall} + t_{RC} \tag{6.21}$$

t_{fall} is the voltage fall time of V_{ds} with high *dv/dt* during the normal turn-on transients. t_m is the time interval between the end point of t_{cla} and the starting point of t_{fall}. Details are illustrated in Fig. 6-29(b).

In fact, V_{desat} will not necessarily start rising immediately after the high negative *dv/dt* disappears. If D_{blk} is a clamping diode with p-n junction, V_{desat} will still be clamped until the reverse recovery process is over [17]. Also, the body diode of the MOSFET M_{cla}

has reverse recovery effect. As shown in Fig. 6-29(c), the real blanking time after considering high *dv/dt* will be even longer because of the reverse recovery effect [17].

$$t_{blk} = t_{cla} + t_m + t_{fall} + t_{rr} + t_{RC} \tag{6.22}$$

In the equation, t_{rr} is the reverse recovery time during which V_{desat} will still be clamped at V_{clamp}. The reverse recovery process can be eliminated by selecting a Schottky diode as D_{blk} and a bipolar junction transistor (BJT) as M_{cla}.

Since the real blanking time of desat protection can be effectively prolonged by the high *dv/dt* and the reverse recovery process, a R-C network with a much smaller time constant can be designed to realize the desat protection with ultrafast response without false triggering issue during the normal turn-on transients. To achieve the desat protection scheme with ultrafast response, R_{blk} and C_{blk} are selected so that V_{desat} will continue to decrease and later be clamped during the voltage fall time with high *dv/dt*. A Si diode with p-n junction and a Si MOSFET are selected to serve as D_{blk} and M_{cla}, respectively, in order to take advantage of the reverse recovery effect for longer blanking time.

During the voltage fall time with high negative *dv/dt*, $V_{desat}(t)$ can be analyzed with the superposition theorem. To simplify the analysis, a constant *dv/dt* is assumed during the voltage fall time of V_{ds}, and R_{damp} is neglected. Also, the nonlinear parasitic capacitance of the desat diode is modeled with its charge-equivalent linear capacitance C_{desat} [102]. After considering the constant dc voltage source V_{cc} and the constant dc current source $C_{desat}dv/dt$, V_{desat} in frequency domain is expressed as:

$$V_{desat}(s) = \left(\frac{V_{cc} - V_{clamp}}{R_{blk}} + C_{desat}\frac{dv}{dt}\right)\frac{R_{blk,eq}}{1 + sC_{blk}R_{blk,eq}} + V_{clamp} \tag{6.23}$$

$R_{blk,eq}$ ($R_{blk,eq} = R_{blk}$ // (R_{d1}+R_{d2})) is the parallel resistance of R_{blk} and R_{d1}+R_{d2}. Then, during

the voltage fall time, V_{desat} in time domain can be solved as follows.

$$V_{desat}(t) = V_{desat}(t = +\infty) + \left[V_{desat,M} - V_{desat}(t = +\infty)\right] e^{\frac{-t}{C_{blk} R_{blk,eq}}} \tag{6.24}$$

It should be noted that the reference point of V_{desat} in this section is 0 V. $V_{desat,M}$ is the value of V_{desat} at the starting point of the voltage fall time. Also, the *dv/dt* is negative during the voltage fall time. $V_{desat}(t = +\infty)$ can be expressed as:

$$V_{desat}(t = +\infty) = \left(V_{cc} - V_{clamp}\right) \frac{R_{blk,eq}}{R_{blk}} + C_{desat} \frac{dv}{dt} R_{blk,eq} + V_{clamp} \tag{6.25}$$

To ensure that V_{desat} can be clamped at V_{clamp}, the fundamental requirement is that $V_{desat}(t = +\infty)$ should be lower than V_{clamp}. The requirement can be rewritten as:

$$R_{blk,eq} > \frac{V_{clamp} - V_{cc}}{C_{desat} \frac{dv}{dt}} \tag{6.26}$$

If R_{blk} cannot satisfy the requirement in (6.26), V_{desat} will never drop to the voltage level lower than V_{clamp}. C_{blk} only influences how quickly V_{desat} drops. Also, the higher the negative *dv/dt* becomes, the more quickly V_{desat} can drop during the voltage fall time, which also means V_{desat} can drop to V_{clamp} more easily.

Similar analysis can be conducted for the desat protection realized with a gate driver IC shown in Fig. 6-1(b). If the displacement current flowing through C_{desat} is sufficiently large due to high *dv/dt*, V_{desat} will keep dropping and finally be clamped by D_{blk}. The real blanking time can be much longer with the help of high *dv/dt* and the reverse recovery of D_{blk}. In order to ensure that V_{desat} can be clamped by D_{blk} during the voltage fall time with high *dv/dt*, the requirement is expressed as:

$$\left(C_{desat} \frac{dv}{dt} - I_{cc}\right) t_{fall} > C_{blk} (V_{desat,M} - V_{clamp}) \tag{6.27}$$

Therefore, a smaller C_{blk} can be adopted to speed up the protection response significantly.

It is not necessary to select C_{blk} based on the traditional blanking time requirement in desat protection, which does not consider the influence of high negative *dv/dt* on V_{desat}. In fact, The smaller C_{blk} is, the more quickly V_{desat} will drop to V_{clamp} during the voltage fall time.

6.3.2 Design Details

In this subsection, design details of the desat protection with ultrafast protection will be covered for 10 kV/20 A discrete SiC MOSFETs shown in Fig. 3-1 [1]. The protection circuitry is the same as the conventional desat protection based on discrete components in Fig. 6-1(a). A Si clamping diode with p-n junction is installed as D_{blk}, and a Si MOSFET is installed as M_{cla}. Together, they contribute to a reverse recovery time t_{rr} of 370 ns, as shown in the waveform of V_{desat} in Fig. 6-30.

The experimental waveform of V_{desat} in Fig. 6-30 is obtained during the ac-dc continuous power test of the HB phase leg based on 10 kV/20 A SiC MOSFETs at 6 kV. Again, the phase leg is configured as a half bridge inverter, and details are introduced in Chapter 3. After high negative dv_{ds}/dt is generated, V_{desat} is clamped at a voltage level slightly lower than -5 V V_{clamp}, which proves that D_{blk} becomes forward biased. Without the clamping diode D_{blk}, the period during which V_{desat} is clamped after the voltage fall time is reduced by 210 ns, as displayed in Fig. 6-31. It is hence proved that the clamping diode D_{blk} participates in clamping V_{desat} with its reverse recovery process. After removing D_{blk}, t_{rr} is reduced to 160 ns, which is attributed to the reverse recovery process of the body diode of Si MOSFET M_{cla} (BSS138). Generally, the experimental waveforms in Fig. 6-30 and Fig. 6-31 validate the analysis about the impact of negative *dv/dt* and reverse recovery effect on V_{desat} during the blanking time in Fig. 6-29.

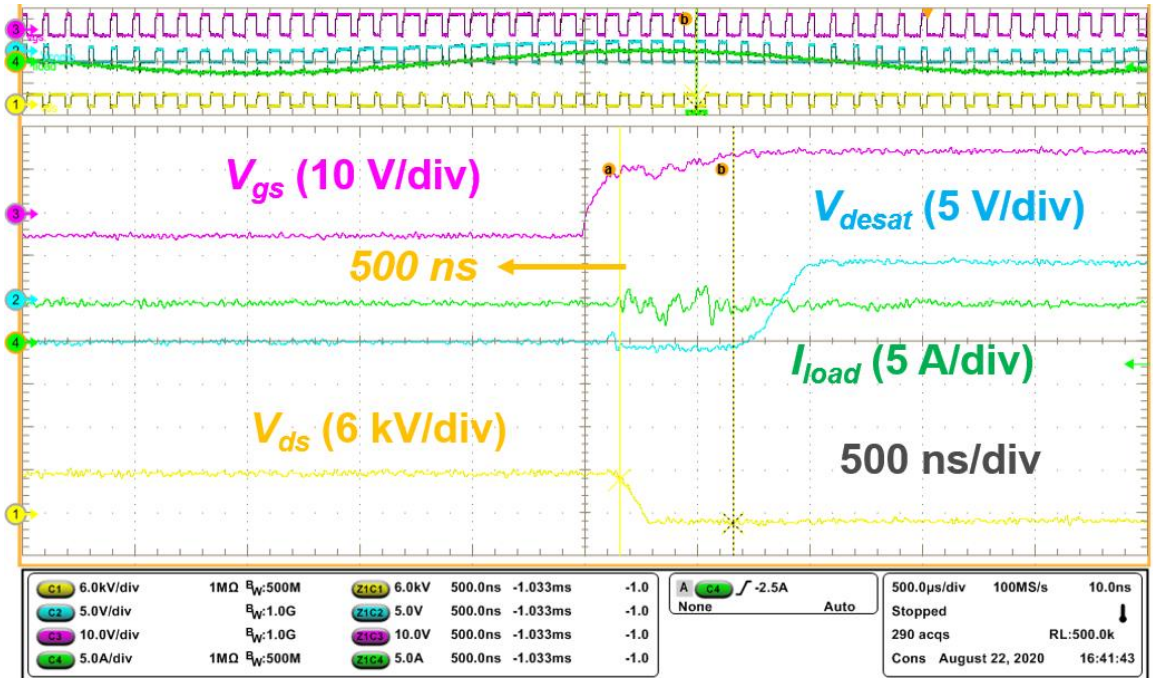


Fig. 6- 30. Waveform of V_{desat} during 6 kV ac-dc continuous test (with D_{blk}, 56 pF C_{blk}, 6.5 kΩ R_{blk}, 470 Ω $R_{goff,cla}$).

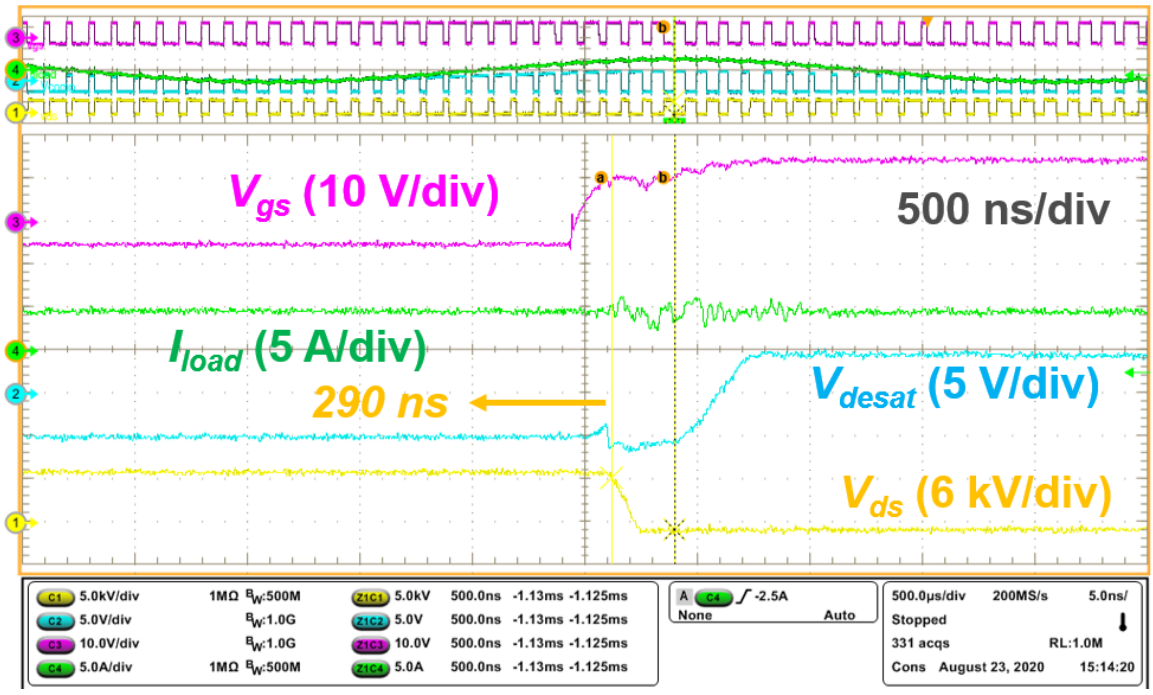


Fig. 6- 31. Waveform of V_{desat} during 6 kV ac-dc continuous test (without D_{blk}, 56 pF C_{blk}, 6.5 kΩ R_{blk}, 470 Ω $R_{goff,cla}$).

With a t_{rr} of 370 ns, according to (6.22), using the R-C network with a much smaller time constant can still result in the effective blanking time longer than 550 ns, which is required based on the switching characteristic of the 10 kV SiC MOSFET shown in Fig. 3-10.

When designing the R-C network, the primary consideration is that V_{desat} can drop rapidly and finally be clamped during the voltage fall time. Thus, according to (6.26), R_{blk} can be selected based on $C_{desat}\frac{dv}{dt}$ first, which is the displacement current flowing through the desat diode. As displayed in Fig. 6-32, turn-on *dv/dt* of the 10 kV SiC MOSFET increases rapidly as the MOSFET switches at higher voltage levels, while C_{desat}, the charge-equivalent linear capacitance of the desat diode, reduces significantly as the switching voltage rises [102]. As a result, the displacement current $C_{desat}\frac{dv}{dt}$ increases by 237% as the voltage increases from 200 V to 6500 V, as indicated in Fig. 6-33. To satisfy the requirement in (6.26) at all voltage levels under 6500 V, $R_{blk,eq}$ should be at least 1.01 kΩ. R_{blk} is finally selected as 3.25 kΩ after considering 200% margin.

The margin is introduced for a series of reasons. $V_{desat}(t = +\infty)$ should be much lower than V_{clamp} in order to guarantee that V_{desat} can drop to V_{clamp} and be clamped by D_{blk} before the voltage fall time of V_{ds} is over, which is usually shorter than 150 ns. The forward voltage drop of D_{blk} should be considered as well. The margin is also helpful in ensuring V_{desat} can be clamped at V_{clamp} when the MOSFET switches with lower turn-on *dv/dt*. For example, the turn-on *dv/dt* will be lower than the *dv/dt* data in Fig. 6-32 if the MOSFET switches with higher gate resistance or the load current higher than 5 A. Also, $R_{blk,eq}$ is always slightly lower than R_{blk}. Therefore, the 200% margin is necessary.

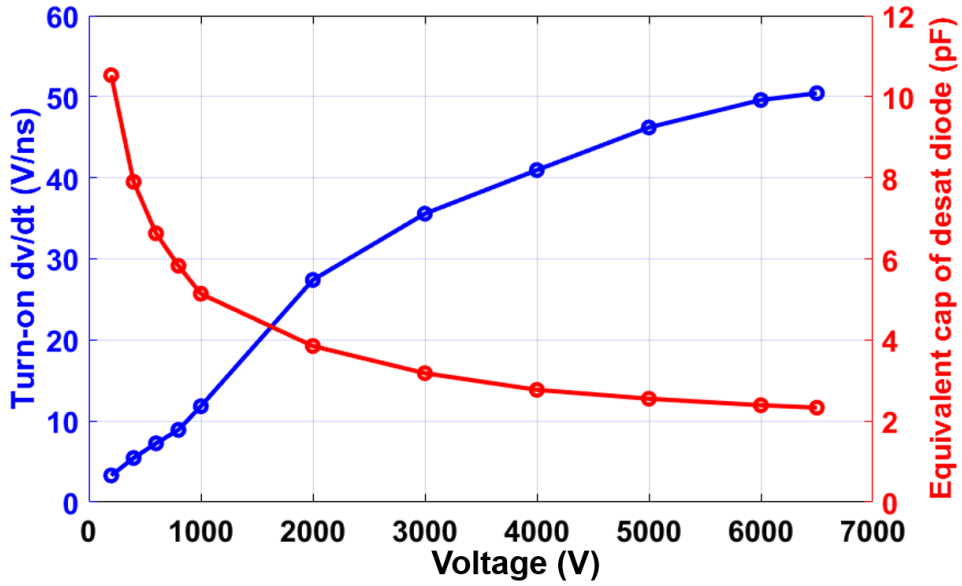


Fig. 6- 32. Turn-on *dv/dt* (at 5 A and 25 ˚C) of 10 kV/20 A SiC MOSFETs and equivalent capacitance of desat diode at different voltage levels.

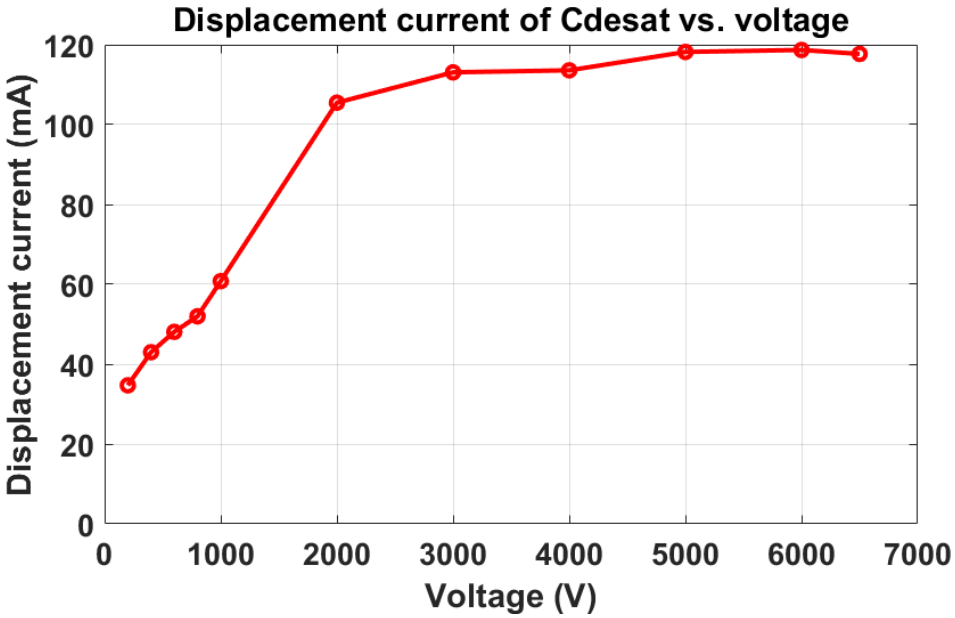


Fig. 6- 33. Displacement current flowing through desat diode ($C_{desat}dv/dt$, calculated based on data in Fig. 6-32) at different voltage levels.

When selecting R_{blk}, it is not recommended to add too much margin, which will slow down the protection response. Also, the selection of R_{blk} is heavily impacted by the switching speed of the 10 kV SiC MOSFET. Higher turn-on *dv/dt* caused by the smaller gate resistance enables the use of a smaller R_{blk}, and makes protection response even faster.

As for the selection of C_{blk}, C_{blk} should be as small as possible to ensure that V_{desat} is brought down to V_{clamp} rapidly before the voltage fall time is over. Another important consideration is that a small C_{blk} supports the fast protection response. The lower limit of C_{blk} is determined by the requirement that $V_{desat,M}$ should not exceed the threshold voltage before the high negative *dv/dt* is generated during the turn-on transient, as shown in (6.28). The effect of the capacitor C_d in the voltage divider is neglected here, to simplify the analysis.

$$V_{desat,M} = V_{clamp} + \frac{(V_{cc} - V_{clamp})R_{blk,eq}}{R_{blk}}[1 - e^{\frac{-(t_d - t_{cla})}{C_{blk}R_{blk,eq}}}] < V_{desat,th} \tag{6.28}$$

t_d is defined as the time interval between the rising edge of V_{gs} and the starting point of the voltage fall time with high *dv/dt*. In other words, t_d is the sum of t_m and t_{cla}. If $V_{desat,M}$ is higher than $V_{desat,th}$ due to the small C_{blk}, the desat protection will be falsely triggered before the voltage fall time. The requirement for C_{blk} can be rewritten as:

$$C_{blk} > \frac{t_d - t_{cla}}{R_{blk,eq} \ln\left[\frac{(V_{cc} - V_{clamp})R_{blk,eq}}{(V_{cc} - V_{clamp})R_{blk,eq} + R_{blk}(V_{clamp} - V_{desat,th})}\right]} \tag{6.29}$$

The lower limit of C_{blk} is mainly determined by t_d and t_{cla}. Based on measured switching transients of 10 kV SiC MOSFETs, t_d is a strong function of the load current and junction temperature, as shown in Fig. 6-34. Higher load current leads to longer t_d, because of the longer current rise time during the turn-on transient. At higher junction temperature,

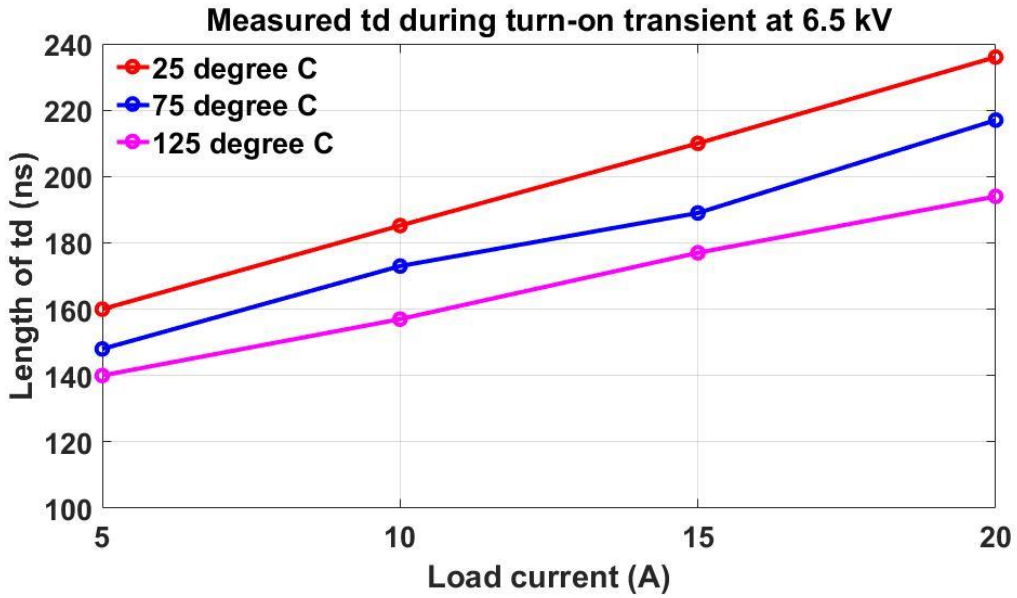


Fig. 6- 34. Measured t_d during the turn-on transient of the 10 kV/20 A SiC MOSFET at 6.5 kV dc bus voltage.

t_d becomes shorter due to the lower gate threshold voltage $V_{g,th}$ and shorter turn-on delay time. The dc voltage does not have a significant influence on t_d, as shown in the waveforms of V_{ds} in Fig. 6-35 during the turn-on transient with dc voltage ranging from 1 kV to 6.5 kV at 10 A load current. As dc voltage decreases from 6.5 kV to 1 kV, t_d only reduces by 7.6%, which could be attributed to the slightly higher $V_{g,th}$ at higher dc voltage. In summary, t_d is dominated by the load current and junction temperature during the normal turn-on transient of the 10 kV/20 A SiC MOSFETs.

As higher load current and lower junction temperature lead to longer t_d, the selection of C_{blk} should be based on the maximum load current of the phase leg and lowest device junction temperature. To support higher load current of the phase leg, a higher C_{blk} should be selected, and the response time to clear short circuit faults will be longer.

In fact, C_{blk} in this chapter is the lumped capacitance between V_{desat} and V_{clamp}. The nonlinear parasitic capacitance of D_{blk} and M_{cla}, and the parasitic capacitance due to PCB layout, should all be included in C_{blk}. C_{blk} contributed by parasitic capacitances can be modeled with a linear capacitor, based on the waveform of V_{desat} measured in the benchtop test with 0 pF capacitor installed as C_{blk}. The benchtop test results show that C_{blk} due to parasitic capacitances can be modeled by an equivalent linear capacitance of 51.2 pF.

C_{blk} should be selected based on the maximum t_d at rated device current (20 A) and room temperature. According to measured turn-on transient waveforms of the 10 kV/20 A SiC MOSFET, the maximum t_d is 235 ns at 6.5 kV/20 A. Then, if we neglect t_{cla} by using a small $R_{goff,cla}$, the selected C_{blk} should be 54.4 pF. In fact, V_{desat} might start to rise before V_{gs} starts to increase from -5 V because of the 40 ns propagation delay of the gate driver

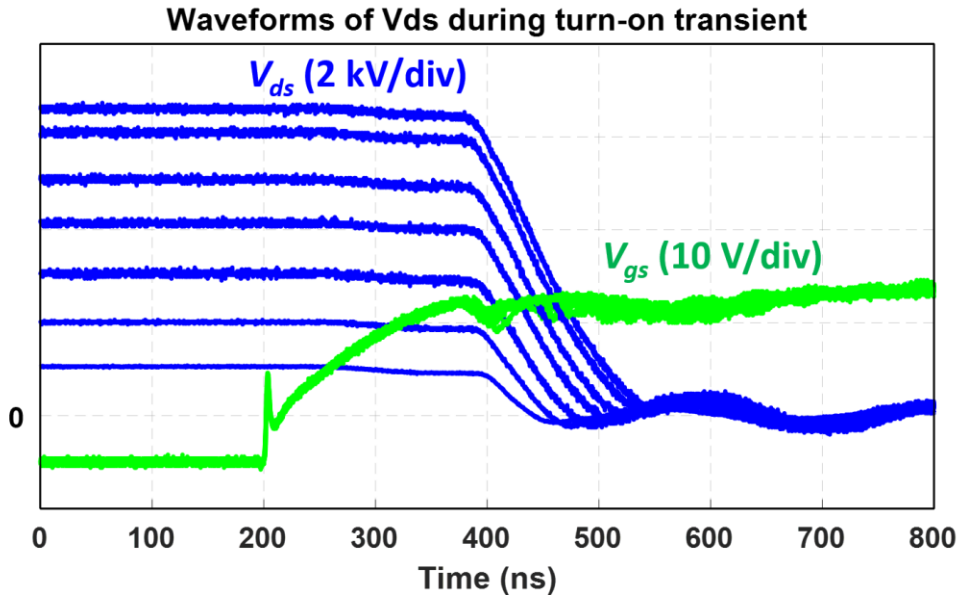


Fig. 6- 35. Waveforms of V_{ds} during the turn-on transient of the 10 kV/20 A SiC MOSFET at different dc voltage levels (at 10 A and 25 ˚C).

IC. So, the maximum t_d we use for selecting C_{blk} is increased to 285 ns, and C_{blk} is finally selected as 66 pF. Considering the 51.2 pF C_{blk} caused by parasitic capacitances, the installed C_{blk} is 15 pF. This is called the desat protection design 1 with ultrafast protection response. In reality, measurement results show that this design has 20 ns t_{cla} due to the 110 Ω $R_{goff,cla}$.

Based on (6.29), the lower limit of C_{blk} can be smaller by selecting a higher $R_{goff,cla}$ to prolong t_{cla}. Adopting longer t_{cla} and smaller C_{blk} can speed up the response of the desat protection under the FUL and the flashover short circuit fault. The protection response under the FUL and the flashover fault will not be affected by t_{cla}, since M_{cla} is already turned off when the two kinds of fault happen, while a smaller C_{blk} will accelerate the protection response under the two kinds of fault. So, we can design the desat protection design 2 with ultrafast protection response by selecting a larger $R_{goff,cla}$ and a smaller C_{blk}.

In this case, we achieve the lowest feasible C_{blk} by not installing any capacitor in the position of C_{blk}. The equivalent C_{blk} is hence 51.2 pF. Then, t_{cla} should be selected based on the 285 ns maximum t_d to avoid the false triggering due to the large $V_{desat,M}$. According to (6.29), the requirement for t_{cla} can be written as:

$$t_{cla} > t_d - C_{blk}R_{blk,eq}\ln\left[\frac{(V_{cc}-V_{clamp})R_{blk,eq}}{(V_{cc}-V_{clamp})R_{blk,eq}+R_{blk}(V_{clamp}-V_{desat,th})}\right] \tag{6.30}$$

So, t_{cla} is selected as 65 ns in order to make sure that $V_{desat,M}$ is still lower than the protection threshold voltage when t_d is as long as 285 ns. Compared to the desat protection design 1, the desat protection design 2 with ultrafast response has longer t_{cla} to enable a smaller C_{blk}, as shown in Table 14.

Table 14. Summary of parameters of two desat protection designs with ultrafast response

	Desat protection design 1	**Desat protection design 2**
$R_{goff,cla}$	110 Ω	348 Ω
Measured t_{cla}	20 ns	65 ns
Installed C_{blk}	15 pF	0 pF
Equivalent C_{blk}	66.2 pF	51.2 pF
R_{blk}	3.25 kΩ	3.25 kΩ
Calculated t_{HSF}	305 ns	285 ns

t_{cla} is an influencing factor of the protection response under the HSF fault, although it is independent of the protection response under the FUL fault and the flashover fault. Under the HSF fault, the time interval t_{HSF} between the rising edge of V_{gs} and the falling edge of V_{gs} after the protection is triggered to clear the HSF fault can be estimated as follows.

$$t_{HSF} = t_{cla} + C_{blk}R_{blk,eq} \ln\left[\frac{(V_{cc} - V_{clamp})R_{blk,eq}}{(V_{cc} - V_{clamp})R_{blk,eq} + R_{blk}(V_{clamp} - V_{desat,th})}\right] \quad (6.31)$$

In the equation, the impact of displacement current from C_{desat} is neglected during the HSF fault, in order to simplify the analysis. After applying the requirement in either (6.29) or (6.30) in equation (6.31), we can obtain the following result.

$$t_{HSF} > t_d \quad (6.31)$$

So, no matter how t_{cla} and C_{blk} are designed, t_{HSF} should always be longer than the maximum t_d. The calculated t_{HSF} of the two protection designs can be seen in Table 14, both of which are longer than the maximum t_d. In summary, with the proposed desat protection scheme, the response under a HSF is limited by t_d, which is determined by the turn-on characteristic of the 10 kV SiC MOSFET. With high negative *dv/dt* considered during the turn-on transient, the response time under a HSF is no longer determined by the effective blanking time. Because of the smaller C_{blk}, the desat protection design 2 can have faster response to clear FUL and flashover faults. Yet the desat protection design 2 has almost the same response to clear the HSF fault as the desat protection design 1.

In terms of the protection response under the FUL fault and the flashover fault, the response is limited by how low C_{blk} can be in reality. The lowest C_{blk} that can be achieved feasibly is determined by parasitic capacitance between V_{desat} and V_{clamp}. Then, the required

t_{cla} and $R_{goff,cla}$ can be selected accordingly, based on (6.30). It should be mentioned that the selection of t_{cla} will not influence the turn-on characteristic of M_{cla}, since the turn-off gate resistance of M_{cla} is different from its turn-on gate resistance.

In addition, when designing the desat protection scheme with ultrafast response for the implementation realized with a gate driver IC shown in Fig. 6-1(b), t_{cla} cannot be selected, since it is determined by the gate driver IC. Without this design freedom, the protection response under the FUL fault and the flashover fault cannot be tuned. C_{blk} should be selected based on the maximum t_d and the t_{cla} determined by the gate driver IC.

6.3.3 Experimental Results

The desat protection design 1 with ultrafast response is fully tested with short circuit tests and ac-dc continuous switching test. HSF short circuit test result at 6.5 kV (short circuit inductance: 71 nH) demonstrates that the HSF fault with a peak current of 71.2 A is cleared with a response time of 120 ns. Meanwhile, the desat protection in the baseline design in Chapter 3 has a response time of 1075 ns under the HSF fault at 6.5 kV, based on the definition of response time in this chapter. With 89% reduction in response time under the HSF fault, the desat protection design 1 with ultrafast response has successfully achieved much faster response than the desat protection in the baseline phase leg design. Moreover, the 120 ns response time achieved by the desat protection design 1 with ultrafast response is 65% shorter than the response time of the improved desat protection in Section 6.2 when clearing the HSF fault.

As shown in Fig. 6-36, the protection responds and initiates the soft turn-off process within 370 ns after V_{gs} starts to rise, which is slightly longer than the calculated 305 ns t_{HSF}

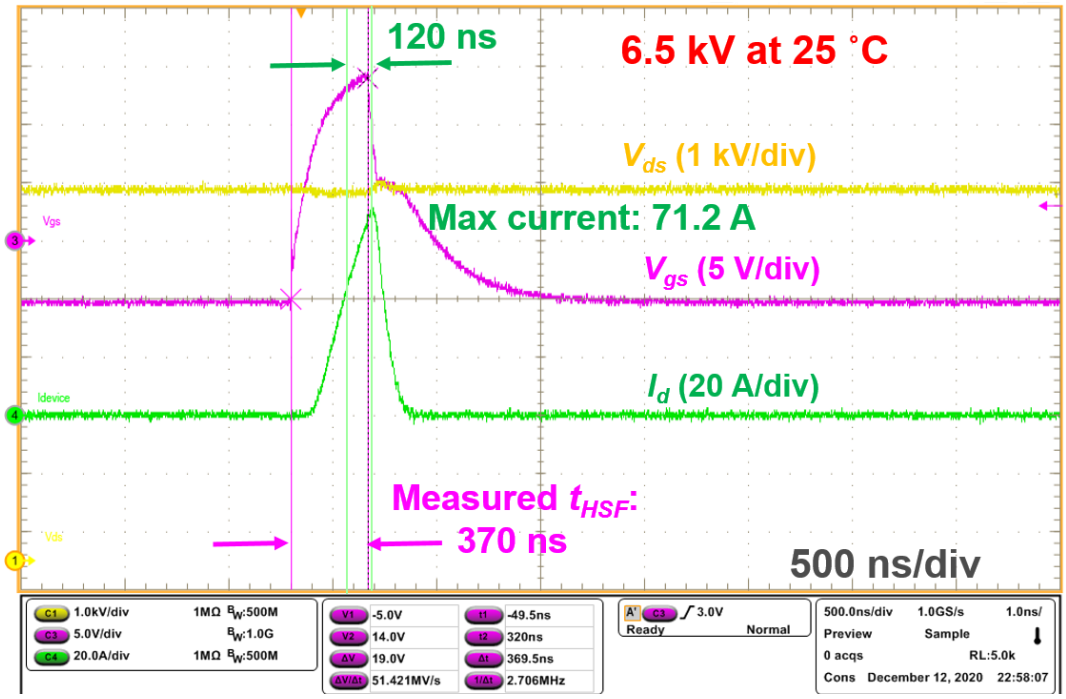


Fig. 6- 36. HSF short circuit test waveform of 10 kV SiC MOSFET with desat protection design 1 with ultrafast response.

in Table 14. The difference is mainly due to the total propagation delay when the gate driver is trying to turn off the MOSFET, especially the 40 ns propagation delay in the gate driver IC. The other reason is that the low negative *dv/dt* in V_{ds} during the HSF fault slows down the rise of V_{desat} slightly. It should be mentioned that the measured waveform of V_{gs} during HSF fault is distorted by the voltage drop on the common source inductance, especially when the *di/dt* of short circuit current suddenly changes.

FUL short circuit test of the lower MOSFET in the phase leg is also conducted at 6.5 kV, as displayed in Fig. 6-37. The FUL short circuit is generated by turning on the upper MOSFET with the same process as the FUL test in Section 6.2. The response time under FUL fault is 215 ns after the device current reaches the threshold current (42.5 A at 25 ˚C). In fact, the device current continues increasing after the soft turn-off process is initiated, until it reaches the peak current of 80 A. The detection time before triggering the soft turn-off process is only 95 ns.

In addition to the ultrafast protection response, the strong noise immunity of the protection design 1 with ultrafast response is fully validated with the ac-dc continuous test at 6.6 kV. During the ac-dc continuous test, the protection was never falsely triggered. The waveform captured during the ac-dc continuous switching test can be seen in Fig. 6-38. When the lower MOSFET of the phase leg serves as the synchronous device with negative load current, V_{desat} does not have significant positive spikes. In this case, the lower MOSFET can achieve ZVS turn-on with sufficiently high load current, and V_{desat} is quickly clamped by the desat diode after V_{gs} starts to rise. Even if the load current is too low to achieve ZVS, the spike of V_{desat} is still low because of the low load current and short t_d.

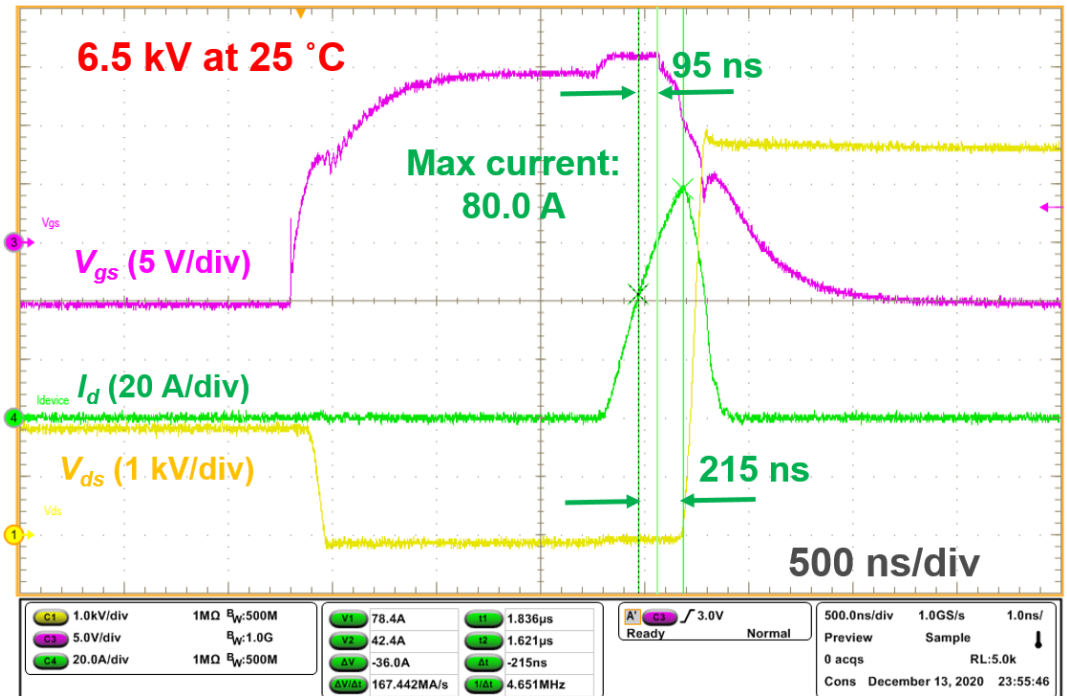
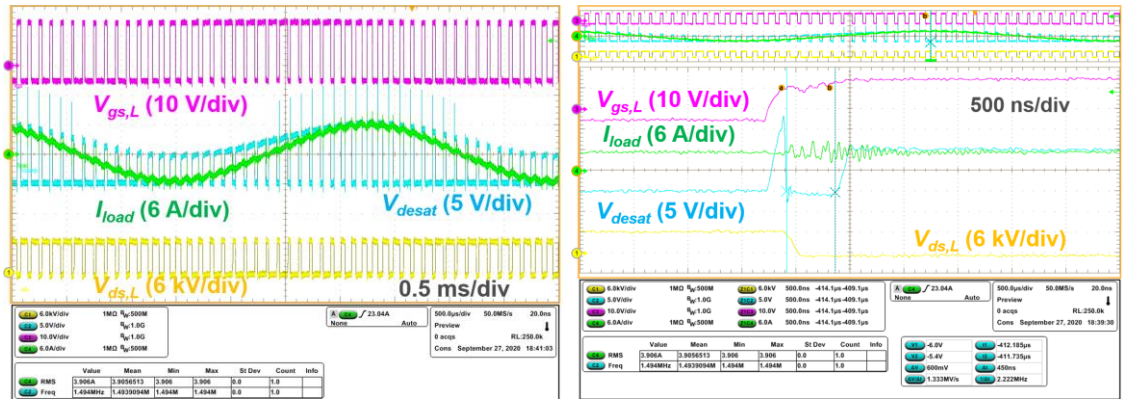


Fig. 6- 37. FUL short circuit test waveform of 10 kV SiC MOSFET with desat protection design 1 with ultrafast response.



(a) (b)

Fig. 6- 38. Waveforms captured during 6.6 kV ac-dc continuous test with desat protection design 1 with ultrafast response.

When the load current is positive, the lower MOSFET cannot achieve ZVS and serves as the active switch in the phase leg. The magnitude of $V_{desat,M}$ becomes considerable, and $V_{desat,M}$ has a sinusoidal shape because higher device current leads to longer t_d. The magnitude of $V_{desat,M}$ in Fig. 6-30 and 6-31 is low due to the large time constant of R-C network and the large $R_{goff,cla}$ (470 Ω). As shown in zoom-in waveform with ~5.5 A load current in Fig. 6-38(b), because of the small $R_{goff,cla}$, V_{desat} rises almost immediately after V_{gs} starts to rise. V_{desat} exceeds 10 V before quickly dropping to ~-5 V because of the high negative *dv/dt* during the fast turn-on transient.

The desat protection design 2 with ultrafast response is also validated with a series of short circuit tests and ac-dc continuous test. With the desat protection design 2 with ultrafast response, HSF short circuit test result at 6.5 kV proves that the HSF fault with a peak current of 68 A is cleared with a response time of 115 ns, as displayed in Fig. 6-39. The HSF short circuit test setup is the same as the desat protection design 1 with ultrafast response. The measured time interval t_{HSF} between the rising edge and falling edge of V_{gs} is 358 ns, still slightly higher than the calculated 285 ns t_{HSF} in Table 14, which is similar to the case in protection design 1.

Although the test setup generating a flashover fault is not available in the laboratory, the FUL test setup can be adjusted to generate a FUL which is closer to a flashover fault. In the phase leg, the upper MOSFET used to generate a FUL has 15 Ω turn-on gate resistance. To make the FUL closer to a flashover fault, the turn-on gate resistance of the upper MOSFET is reduced to 3 Ω, resulting in higher *di/dt* during the FUL. Further

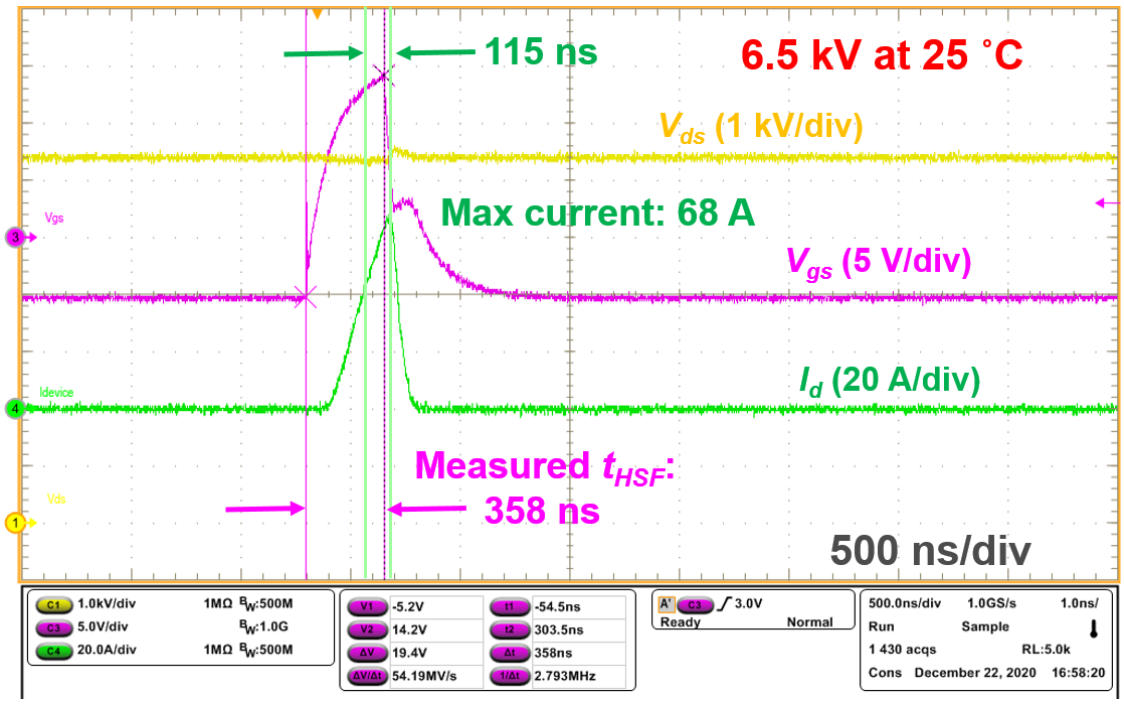


Fig. 6- 39. HSF short circuit test waveform of 10 kV SiC MOSFET with desat protection design 2 with ultrafast response.

reducing $R_{g,on}$ is not feasible, because the required gate current will exceed the output current capability of the gate driver IC (IXDD609).

The FUL short circuit fault is successfully cleared at 6.5 kV with the desat protection design 2 with ultrafast response. With a R-C network with a smaller time constant, V_{desat} can follow V_{ds} with a shorter delay. The response time is further reduced to 155 ns, and the detection time before triggering the soft turn-off process is only 82 ns, which is also reduced compared to the desat protection design 1. To continue reducing the detection time and response time, C_{blk} caused by parasitic capacitances should be minimized, as discussed in Subsection 6.3.2.

The detailed waveforms can be seen in Fig. 6-40. Because of higher *di/dt* during the current rise time, the peak short circuit current is higher than 80 A, although the desat protection design 2 with ultrafast response has shorter response time than the desat protection design 1. After the FUL fault is generated, the measured V_{gs} reaches 18 V because of the high voltage drop on common source inductance caused by the high *di/dt*.

The noise immunity of the protection design 2 is also fully validated with the ac-dc continuous power test at 6.6 kV, during which the protection was never falsely triggered. Even though C_{blk} is completely realized by parasitic capacitances, strong noise immunity is still achieved by following design guidelines in Section 6.1. Especially, C_{p3} is reduced to less than 0.001 pF. Because of the larger $R_{goff,cla}$ (348 Ω) and longer t_{cla}, $V_{desat,M}$ is reduced substantially compared to the desat protection design 1 under the same test condition (6.6 kV, 0.55 modulation index), as shown in Fig. 6-41. With longer t_{cla}, $V_{desat,M}$ still has a sinusoidal shape with the ac load current whose fundamental component has a peak value

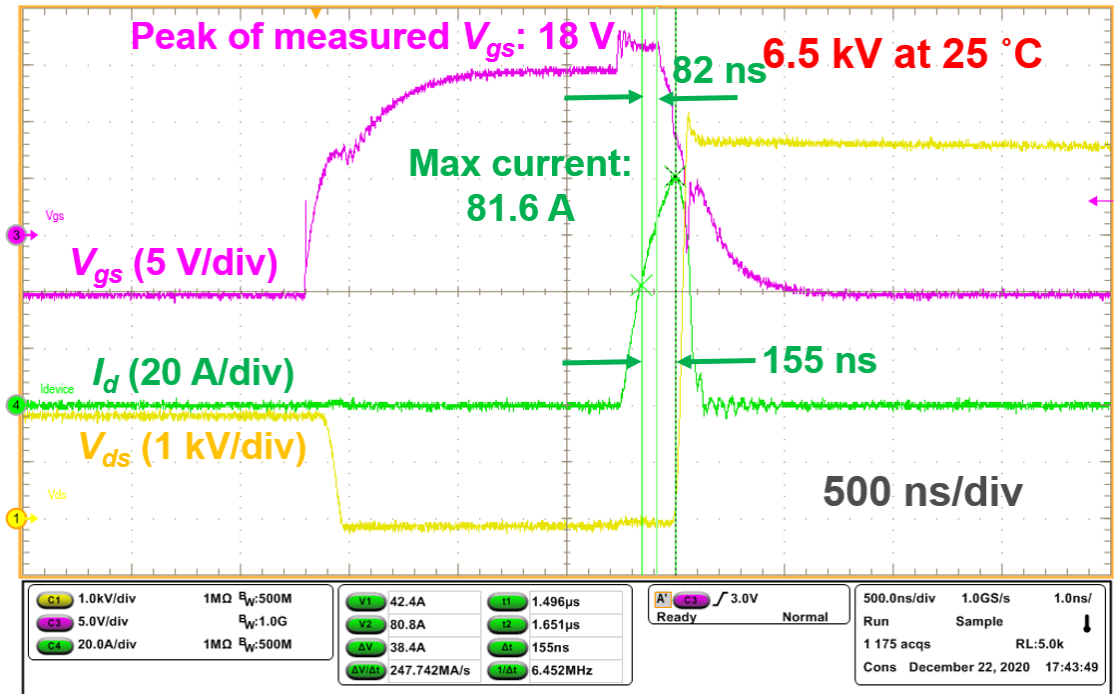
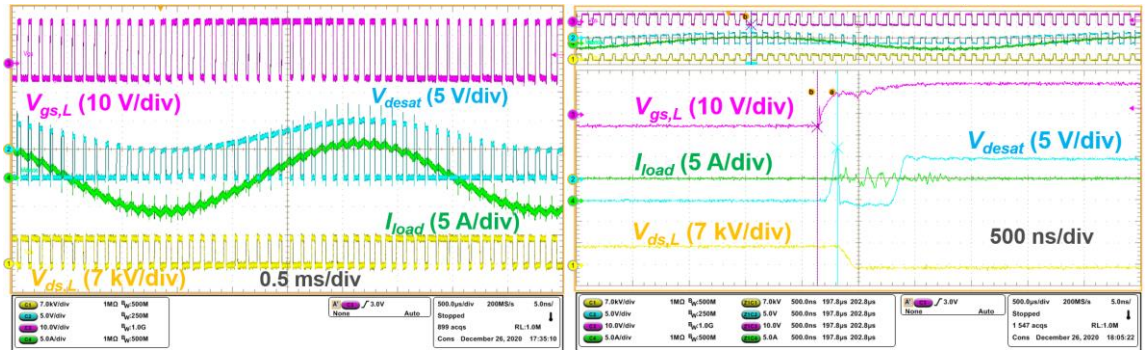


Fig. 6- 40. FUL short circuit test waveform of 10 kV SiC MOSFET with desat protection design 2 with ultrafast response.



(a) (b)

Fig. 6- 41. Waveforms captured during 6.6 kV ac-dc continuous power test with desat protection design 2 with ultrafast response.

of ~6 A. The zoom-in waveform in Fig. 6-41(b) confirms that V_{desat} is clamped at -5 V after V_{ds} of the lower MOSFET starts to fall with high *dv/dt*. Fig. 6-41(b) also reveals that t_{cla} in desat protection design 2 is significantly longer than t_{cla} in desat protection design 1 with ultrafast response. In summary, both strong noise immunity and ultrafast response of the desat protection design 2 are demonstrated with experimental results at rated voltage. Both HSF and FUL can be cleared with a response time of <160 ns.

6.3.4 Discussion

The proposed desat protection scheme in this section feature several advantages in terms of protecting 10 kV SiC MOSFETs. To start with, it possesses ultrafast protection response and strong noise immunity simultaneously. Although the desat protection circuity has a R-C network with a small time constant, the noise immunity will not be sacrificed by following the design guidelines in Section 6.1. The ultrafast protection response can effectively help reduce the short circuit current and energy loss, which makes it more competitive in applications where the high short circuit current is a significant concern because of the high saturation current of the MOSFET.

Furthermore, the implementation of the desat protection scheme with ultrafast response is as simple as the conventional desat protection design. Compared to the conventional desat protection design, no additional circuitry and components are required. The only modification is that R_{blk}, C_{blk}, and the clamping diode should be selected differently.

Moreover, the circuity of the desat protection scheme with ultrafast response is compatible with that of the conventional desat protection design. The conventional desat

protection design can be easily modified to switch to the proposed desat protection design with ultrafast response, without ordering a new PCB. Again, only R_{blk}, C_{blk}, and the clamping diode D_{blk} should be replaced. Thus, the designer has the flexibility to switch between the conventional design protection and the proposed desat protection with ultrafast protection. Also, the proposed desat protection scheme with ultrafast response is effective for the two mainstream implementations for high voltage SiC MOSFETs in Fig. 6-1.

In fact, high negative *dv/dt* generated by low voltage (<3.3 kV) SiC MOSFETs can also play a role in shaping V_{desat} during their turn-on transients. The impact of high negative *dv/dt* on V_{desat} can counteract the capacitive charging process leading to higher V_{desat}, which will also result in longer effective blanking time. The main difference is that the duration of the high *dv/dt* generated by low voltage SiC MOSFETs is much shorter. To apply the proposed ultrafast desat protection scheme in low voltage SiC MOSFETs, the key is to ensure that V_{desat} drops quickly to make D_{blk} enter the forward conduction mode within the short voltage fall time with high *dv/dt*.

The limitation of the proposed desat protection scheme with ultrafast protection is that it cannot have ultrafast response in short circuit faults with high negative *dv/dt*. In normal turn-on transients with high negative *dv/dt*, it takes advantage of the negative *dv/dt* to effectively prolong the blanking time. As a result, if high negative *dv/dt* is generated during the short circuit fault, it will take a long time for V_{desat} to reach the protection threshold, leading to much longer response time than the cases without high negative *dv/dt*. However, it is not common to have high negative *dv/dt* during the short circuit and overcurrent conditions, as shown in Fig. 6-42. During the FUL fault and flashover fault,

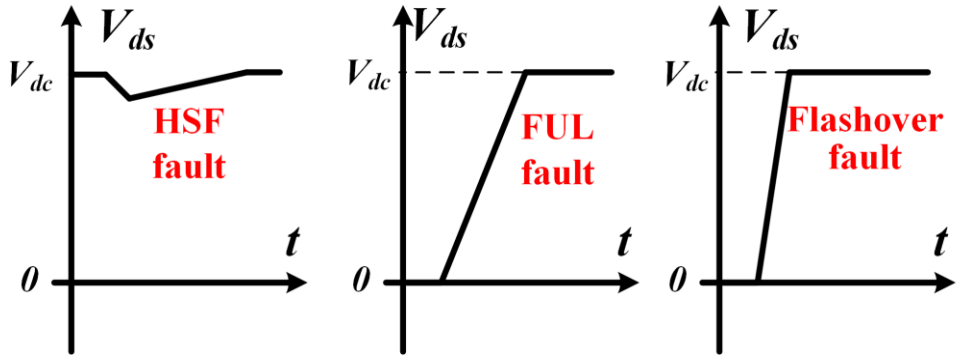


Fig. 6- 42. Typical waveforms of V_{ds} under HSF, FUL, and flashover fault.

the waveform of V_{ds} is dominated by a high positive *dv/dt*. During the HSF fault, usually V_{ds} only experiences a small dip with a low negative *dv/dt* for a short time. Also, the resulting displacement current is small because of the small parasitic capacitance of the desat diode at high V_{ds}.

6.3.5 Summary

In this section, a desat protection scheme with ultrafast protection response is proposed for 10 kV SiC MOSFETs. The proposed protection scheme with ultrafast response can be applied in both the desat protection circuitry based on discrete components and the desat protection circuitry realized with a gate driver IC. The proposed protection scheme has the same fundamental working principle and circuitry as the conventional desat protection. However, the blanking time requirement is satisfied by fully taking advantage of the high negative *dv/dt* during the turn-on transient of 10 kV SiC MOSFETs and the reverse recovery effect of the clamping diode. With the long duration of the high negative *dv/dt* generated by 10 kV SiC MOSFETs, the two factors can be easily utilized to effectively prolong the blanking time. Therefore, a much smaller blanking capacitor C_{blk} and a R-C network with a much smaller time constant can be used in the desat protection circuitry, leading to ultrafast protection response under various short circuit conditions. The design considerations and trade-offs of the R-C network are presented in detail. The ultrafast response and strong noise immunity of the proposed protection scheme are validated in numerous short circuit tests and ac-dc continuous switching test. The proposed protection scheme can clear the HSF with a response time of 115 ns and the FUL within

155 ns, which is the fastest reported response for a protection scheme based on desat protection when protecting a discrete 10 kV SiC MOSFET.

6.4 Summary

The noise immunity of the desat protection for 10 kV SiC MOSFETs and other high voltage SiC MOSFETs is analyzed extensively and quantitatively to achieve the desat protection with fast response and strong noise immunity simultaneously. The influence of both high positive dv_{ds}/dt and high negative dv_{ds}/dt is investigated. The high positive dv_{ds}/dt is identified as the major concern which could falsely trigger the desat protection via the extremely small parasitic capacitance (< 0.01 pF) coupled with the voltage divider in the desat protection circuitry. The mathematical model of the noise immunity margin is established to evaluate the noise immunity and support the noise immunity improvement. According to Fig. 6-11, the worst case for noise immunity margin is the high positive dv_{ds}/dt with a long voltage rise time, which explains why the desat protection for high voltage SiC MOSFETs is more vulnerable to noise than desat protection for other devices. Systematic design guidelines are summarized to enhance the noise immunity of the desat protection, which are supported by the simulation results and experimental results.

An improved desat protection scheme with 600 ns digital blanking time is developed for 10 kV SiC MOSFETs to realize fast response and excellent noise immunity concurrently. The digital blanking time implementation decouples the length of blanking time from the R-C network in desat protection circuitry. The R-C network with a smaller time constant can hence be used to accelerate the protection response, especially the response under the FUL and the flashover fault. Short circuit test results at 6.5 kV

demonstrate that the HSF can be cleared with a response time of 340 ns, and the response time is 195 ns under the FUL. Meanwhile the noise immunity is not impaired by leveraging the design guidelines obtained from the noise immunity analysis.

A desat protection scheme with ultrafast response is proposed to protect 10 kV SiC MOSFETs. By leveraging the analysis results and design guidelines in Section 6.1, the proposed desat protection scheme is able to achieve ultrafast response and strong noise immunity simultaneously. The proposed desat protection scheme with ultrafast response achieves sufficiently long blanking time by taking advantage of the high negative *dv/dt* with long duration during the fast turn-on transient and the reverse recovery effect of the clamping diode D_{blk}, instead of relying on a large blanking capacitor. Thus, a small blanking capacitor and a R-C network with a small time constant can be adopted in the protection circuitry for ultrafast response under HSF, FUL, and the flashover fault. Short circuit test results at 6.5 kV demonstrate that the proposed protection scheme has achieved ultrafast response: 115 ns response time under a HSF fault and 155 ns response time under a FUL fault.

CHAPTER 7. COMPREHENSIVE TEST SCHEME OF A 10 KV SIC MOSFET BASED PHASE LEG

The comprehensive test scheme for a phase leg based on 10 kV SiC MOSFETs should be able to provide an operating condition similar to the real condition in a modular MV converter, such as device current, *dv/dt*, CM voltage, and so on. Specifically, the test scheme should fully validate its thermal performance, insulation design, and the capability to withstand high *dv/dt* and the resulting noise when the phase leg operates as part of a modular MV converter. For example, high *dv/dt* can distort PWM signals and falsely trigger protections via various mechanisms [24], [105], and such issues should be found at the stage of phase leg testing, instead of MV converter testing.

In this chapter, a simple test method is proposed to fully qualify a HB phase leg based on 10 kV SiC MOSFETs, especially its ability to withstand high *dv/dt*. First, the proposed test scheme is introduced in detail, whose essential step is the ac-dc continuous test in which two phase legs are connected in series to resemble the operation of modular MV converters with multiple cascaded phase legs. Second, an open loop voltage balancing scheme is introduced to balance the voltage of two cascaded phase legs. Detailed simulation and experimental results are provided to validate the proposed test method, followed by the summary of this chapter. It should be noted that part of the content in this chapter is from the author's conference paper published in *IEEE EPE 2020* [106].

7.1 Overview of Test Scheme

The proposed test scheme for the HB phase leg is a simple three-step scheme with the focus on the ac-dc continuous test. The first step is the component qualification and

phase leg assembly. Initial tests are conducted to check the gate loop and gate driver functions in the second step. In the first step, components should be tested and qualified individually before the phase leg assembly, including gate driver, voltage sensor, MOSFETs, and busbar. After the phase leg is assembled, the vital functions of the gate driver are examined, including rising/falling edge of gate-to-source voltage V_{gs}, feedback signal, short circuit protection as well as soft turn-off. The last step is the ac-dc continuous test which should be conducted carefully by starting from low dc-link voltage operation. Compared to the baseline testing procedures introduced in Chapter 3, the proposed test scheme does not require DPT and short circuit test for each MOSFET, and hence is much simpler, less time-consuming, and more efficient, which is important when many phase legs need to be tested. It is acceptable to skip DPT and short circuit test since the 10 kV/20 A SiC MOSFET and its package in the phase leg have become more mature and reliable. In other words, DPT and short circuit test are necessary if the device is still in early stage with its performance not fully guaranteed. Meanwhile, more comprehensive tests of the gate driver functions are required in the second step.

7.1.1 Overview of ac-dc Continuous Test

A proposed ac-dc continuous test circuit with two cascaded phase legs is the core of the test scheme, as shown in Fig. 7-1. The proposed ac-dc continuous test circuit has a simple configuration, including a high voltage dc power supply, which is commercially available from various manufacturers, an input capacitor, two cascaded HB phase legs, and the load. During the normal operation with the voltage of two phase legs well-balanced, the dc component of the phase leg voltage is approximately equal to the input voltage V_g.

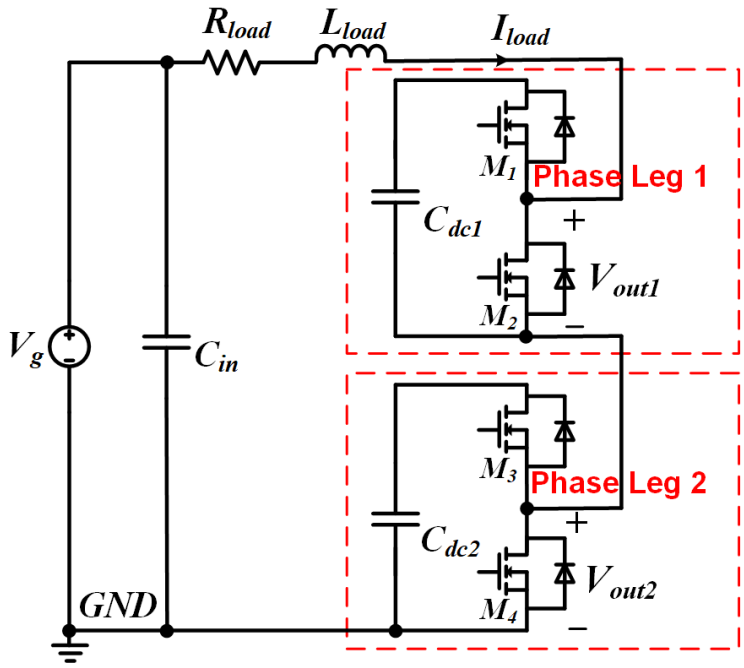


Fig. 7- 1. Circuit diagram of the proposed ac-dc continuous test circuit for the qualification of half bridge phase legs.

Thereby, the high voltage dc power supply should be able to output the rated dc bus voltage of the HB phase leg. The load can be easily realized with inductors and the resistive load built for the test of MV converters. R_{load} can be adjusted to achieve the desired active power. Typically, the active power and the value of R_{load} are limited by the output current capability of the dc power supply.

The proposed continuous test circuit has two cascaded phase legs to resemble numerous modular MV converters with a string of phase legs in series, including MMC and cascaded H-bridge converter. During the ac-dc continuous test, Phase Leg 1 in Fig. 7-1 is the phase leg under test, with floating potential and high *dv/dt* in all of its terminals resulting from the switching actions in Phase Leg 2. Phase Leg 2 can be regarded as part of the ac-dc continuous test setup. Usually Phase Leg 2 has the same gate resistance and switching speed as the phase leg under test. The gate resistance of Phase Leg 2 can also be reduced to further increase the *dv/dt* in order to fully test the *dv/dt* immunity of the phase leg under test. A fiber optic voltage probe which is able to withstand high common mode voltage can be used to accurately monitor the gate signal, the output signal of the short circuit protection, and other signals [107], to evaluate the noise immunity of the phase leg under test under high *dv/dt*. In parallel with the ac-dc continuous test, the thermal design can be evaluated online by measuring device temperature with a fiber optic temperature sensor. Acoustic partial discharge detection method is effective in the online validation of the insulation design under PWM voltage with high *dv/dt* [108].

7.1.2 Modulation Scheme

In the ac-dc continuous test, a modulation scheme is implemented to force the phase leg under test to undergo high *dv/dt* that might be generated by the modular MV converter. Cascaded phase legs are leveraged to generate ≥2X *normal dv/dt* of a single 10 kV SiC MOSFET, which is likely to occur in the modular MV converter with many modules in series. In this chapter, *normal dv/dt* is defined as the *dv/dt* of a single 10 kV SiC MOSFET with the selected gate resistance for the phase leg. Bipolar SPWM modulation with the same modulation index is implemented in both Phase Leg 1 and 2. With zero phase shift between the PWM signals for Phase Leg 1 and 2, M_1 shares the same gate signal with M_3, and M_2 and M_4 receive the same gate signal.

If Phase leg 2 and the phase leg under test have the same switching speed and switching frequency, the source of M_1 in Phase Leg 1 will undergo the voltage rise from 0 to $2V_g$ with 2X normal turn-on *dv/dt* of M_1 as M_1 and M_3 turn on simultaneously. The source potential of M_1 drops from $2V_g$ to 0 with 2X normal turn-off *dv/dt* of M_1, as M_1 shuts off. In modular MV converters, in fact, such switching actions with 2X *normal dv/dt* could occur when multiple cascaded modules switch their modes simultaneously [109]. The voltage step change between 0 and $2V_g$ with 2X *normal dv/dt* results in 2X CM current flowing through the gate driver and its isolated power supply. Also, the high voltage insulation capability of the isolated power supply for the gate driver can be tested in this case.

In addition, the gate resistance of Phase Leg 2 can be tuned and different from the phase leg under test. If the gate resistance for MOSFETs in Phase Leg 2 is adjusted to be lower than the gate resistance in Phase Leg 1 to achieve higher *dv/dt*, >2X *normal dv/dt*

and CM current can be realized for the phase leg under test. Meanwhile, the DC- terminal of the phase leg under test undergoes *dv/dt* higher than the *normal dv/dt* of 10 kV SiC MOSFETs in a modular MV converter. Hence, the *dv/dt* that the phase leg under test experiences during the continuous test can be fully controlled for the purpose of evaluating the *dv/dt* immunity margin. The noise immunity of the phase leg under high *dv/dt*, especially the short circuit protection and the isolated power supply, can thereby be fully tested. Subsequently, the phase leg under test can be tested and debugged to achieve the capability to handle the desired level of *dv/dt*. With such modulation scheme, the ac-dc continuous test setup is a suitable platform to test the capability of the phase leg to withstand high *dv/dt* when operating as a building block of a modular MV converter.

The ac-dc continuous test setup has the capability to validate the thermal and insulation design of the phase leg under test at the rated dc bus voltage and current. The rated dc bus voltage of the phase leg can be realized by increasing V_g. The load voltage is a PWM-type voltage with step changes between V_g and -V_g. Normally the load current has a sinusoidal shape due to the high impedance of the load inductor at high frequency. The magnitude of the load current can be adjusted by changing the modulation index and the fundamental frequency. The peak value of the fundamental component of the load current $I_{fund,pk}$ can be estimated with the equation below.

$$I_{fund,pk} = \frac{mV_g}{\sqrt{(2\pi f_{line} L_{load})^2 + {R_{load}}^2}} \tag{7.1}$$

In the equation, f_{line} is the fundamental frequency, and m is the modulation index, both of which are determined by the modulation signal. The dc component of the load current

$I_{load,DC}$ is determined by the active power consumed in the continuous test setup, which can be calculated with the following equation.

$$I_{load,DC} = \frac{P_{loss} + R_{load} I_{RMS}^2}{V_g} \tag{7.2}$$

I_{RMS} is the RMS value of the load current, and P_{loss} is the power loss in the ac-dc continuous test setup. If the resistive load is not installed, the dc component of the load current will be almost zero.

7.2 Open-loop Voltage Balancing Scheme

Voltage balancing is essential to the proposed ac-dc continuous test circuit with two cascaded HB phase legs. In order to further simplify the test setup and control, an open loop voltage balancing scheme is adopted, whose details are presented in this section.

The two cascaded phase legs ideally have balanced dc capacitor voltage, since the two capacitors always have the same current with the designed modulation scheme. In ideal conditions, M_1 and M_3 always conduct at the same time to achieve natural voltage balancing. In reality, the two phase legs could have different dead times due to nonideal factors in the controller and the gate driver board. Also, there could be slight phase shift between V_{gs} of M_1 and M_3, or V_{gs} of M_2 and M_4. For example, the fiber optic transmitter or receiver with the same part number could have different propagation delay. Especially, longer dead time contributes to higher dc capacitor voltage no matter what the direction of the load current is. Without any voltage balancing method, the dc capacitor voltage of the two phase legs would diverge from each other, and the dc capacitor voltage of the phase leg with shorter dead time finally drops to zero. This can be explained by the difference between the average capacitor current of the two phase legs, which is named the offset

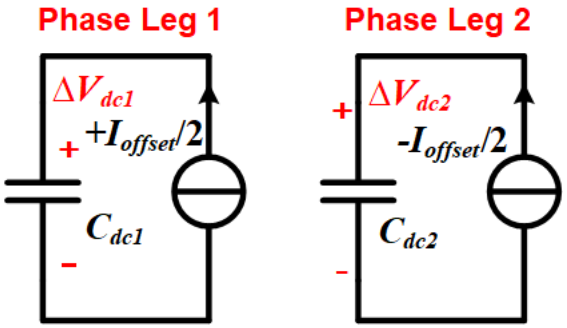
current, I_{offset}. In the dc circuit model in Fig. 7-2(a), the dc capacitor voltage of the two phase legs is marked as ΔV_{dc1} and ΔV_{dc2}, because the initial dc voltage is neglected. The dc voltage difference V_{offset}, defined as $\Delta V_{dc1} - \Delta V_{dc2}$, will continue to increase in magnitude as long as I_{offset} exists due to the different dead times, and the voltage of one phase leg will eventually drop to zero.

The magnitude and polarity of I_{offest} is determined by the load current as well as the dead time difference and phase shift between V_{gs} for the MOSFETs of the two phase legs. In fact, the magnitude and polarity of I_{offest} can be time-varying. For instance, assuming 20 ns phase shift between V_{gs} for M_1 and M_3 (V_{gs} for M_1 leading) and zero phase shift between V_{gs} for M_2 and M_4, the instantaneous I_{offset} is almost zero when the load current is positive, because M_1 and M_3 are synchronous devices whose body diodes conduct current during the dead time. If the load current is negative, the phase shift between V_{gs} for M_1 and M_3 will play a part, and the instantaneous $I_{offset}(t)$ can be described with the following equation.

$$I_{offset}(t) = \frac{1}{T_s}\left(\int_{t}^{t+DT_s} I_{load}(t)dt - \int_{t+\Delta t}^{t+\Delta t+DT_s} I_{load}(t)dt\right) \tag{7.3}$$

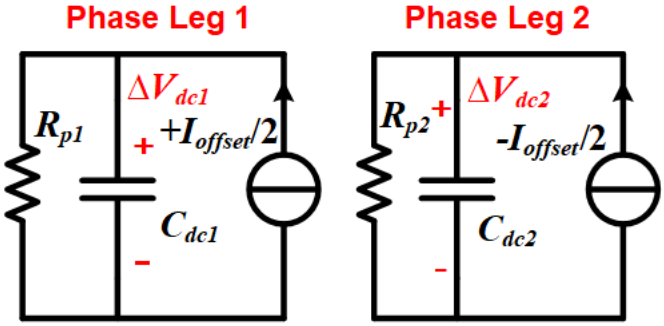
In the equation, T_s is the switching period, D is the duty cycle, and Δt is the phase shift. The equation shows that the magnitude and polarity of I_{offset} depend on the instantaneous phase angle of the load current. In fact, it is likely that different dead time and slight phase shift between V_{gs} for M_1 and M_3 as well as between V_{gs} for M_1 and M_3 influence I_{offset} simultaneously. As a result, the average I_{offset} over a line cycle is not zero in steady state, and hence the voltage balancing cannot be achieved.

An open loop method with an external parallel resistor is developed to suppress the impact of I_{offset} and achieve voltage balancing. As can be seen in Fig. 7-2(a), I_{offset} that could



$$V_{offset} = \Delta V_{dc1} - \Delta V_{dc2} = 0.5 I_{offset} t \left(\frac{1}{C_{dc1}} + \frac{1}{C_{dc2}}\right)$$

(a)



$$V_{offset} = \Delta V_{dc1} - \Delta V_{dc2} = 0.5 I_{offset} (R_{p1} + R_{p2})$$

(b)

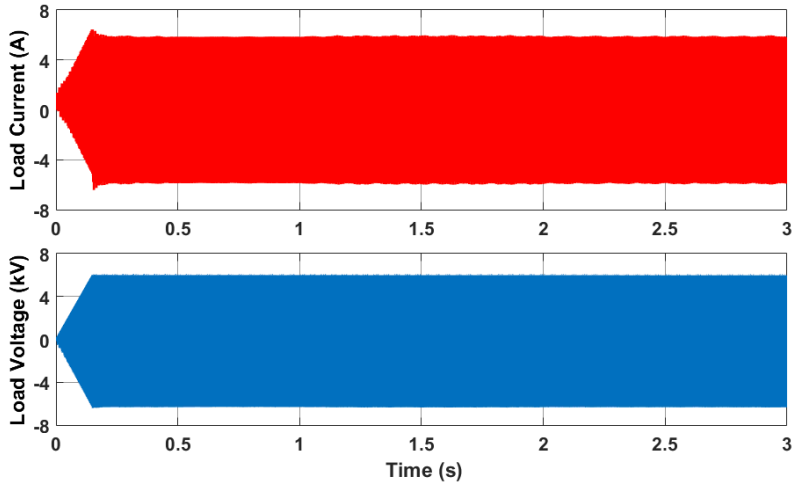
Fig. 7- 2. (a) DC circuit model of the two phase legs used to study V_{offset}. (b) DC circuit model of the two phase legs after adding a resistor in parallel with the capacitor.

be caused by numerous nonideal factors can only flow through the capacitor, and hence keeps charging or discharging the capacitor. After adding a resistor in parallel with the capacitor, as shown in Fig. 7-2(b), all of the offset current will be absorbed by the resistor, and the capacitor voltage will reach steady state. The dc capacitor voltage of the two phase legs in steady state still has some difference V_{offest}, whose equation is shown in Fig. 7-2(b). V_{offest} is only determined by the added parallel resistor and the magnitude of I_{offset} and is independent of the capacitance and parasitics of the dc capacitor.

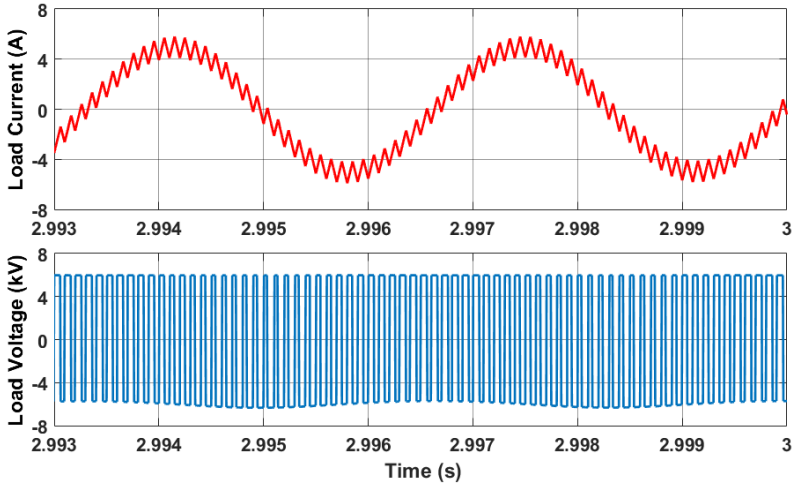
It is difficult to calculate the average I_{offset} in a line cycle in an analytical way. However, the average I_{offset} can be obtained easily based on simulation results. The parallel resistor should be selected based on the trade-off between the V_{offest} and the power loss of the resistor. A small parallel resistance is attractive due to better voltage balancing results, yet bulky power resistors must be selected which may also require additional heatsinks or fans and lead to a complicated experimental setup. A large parallel resistance results in a simple test setup, but the large V_{offset} makes it difficult to control the voltage of the phase leg under test in a convenient way, and increases the risk of device damage due to overvoltage.

7.3 Simulation Results

The proposed ac-dc continuous test circuit with the open loop voltage balancing method is simulated in Matlab/Simulink. Fig. 7-3 shows simulation results of the case with zero phase shift between gate signals for the two phase legs and 500 ns dead time for both phase legs. The dc capacitor voltage of the two phase legs is hence perfectly balanced, and the PWM-type load voltage and the load current with a sinusoidal shape can be seen in the



(a)



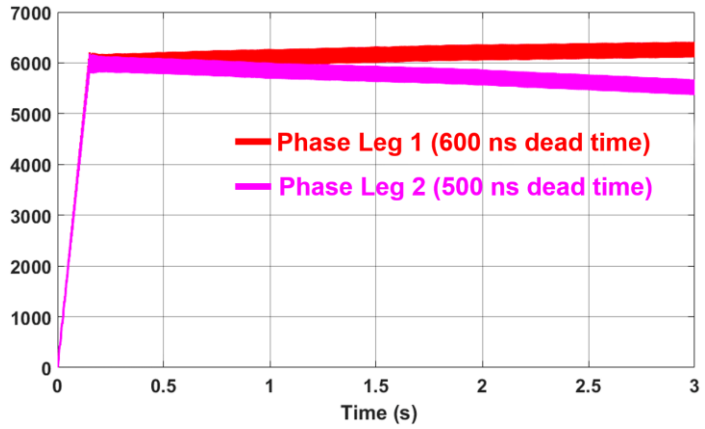
(b)

Fig. 7- 3. Simulated waveforms of load voltage and load current at 6 kV dc-link voltage (modulation index m=0.25, R_{load} =1 Ω, L_{load} =175 mH): (a) Overview (V_g ramps up from 0 to 6 kV within 0.15 s); (b) Zoom-in waveforms.

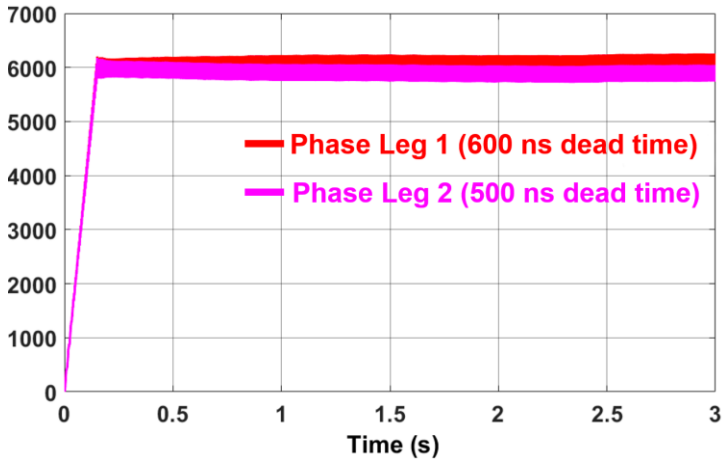
simulation waveforms. The load current is regulated at ~6 A peak with almost zero DC component, since R_{load} is 1 Ω. In addition, Fig. 7-4 displays the simulated phase leg voltage waveforms without and with the open loop voltage balancing method to prove its effectiveness. The case where two phase legs have significantly different dead time is simulated since it provides a large I_{offset}. Without the added parallel resistor, the voltage of Phase Leg 2 with 100 ns shorter dead time keeps decreasing, and V_{offset} increases rapidly to ~800 V within 3 s. The calculated I_{offset} based on simulation results is 2.4 mA, and the calculated V_{offset} at t=3 s is 782 V based on the equation in Fig. 7-2(a). Then a relatively small parallel resistor is added in both phase legs in order to achieve voltage balancing even faster and reduce computational burden in the simulation. After adding a 100 kΩ resistor, the voltage of two phase legs is balanced, and reaches steady state with a constant V_{offset} of ~200 V, close to the calculated 240 V V_{offset}, based on the equation in Fig. 7-2(b). The dc capacitor voltage of the phase leg has the line frequency ripple with a peak-to-peak value of ~300 V, similar to the submodule voltage ripple observed in a MMC converter.

7.4 Experimental Setup and Results

The proposed ac-dc continuous test circuit is realized with the experimental setup shown in Fig. 7-5. The high voltage dc power supply from Spellman (Part Number: ST15P12) can output the dc voltage up to 15 kV with the maximum power of 12 kW. The input capacitor C_{in} is implemented with a capacitor bank whose equivalent capacitance is 46.7 μF. The load inductor is implemented with two high voltage inductors in series with a total inductance of 175 mH. The resistive load is not installed due to the 0.8 A output current limit of the power supply. In fact, in order to reduce the output current ripple of the

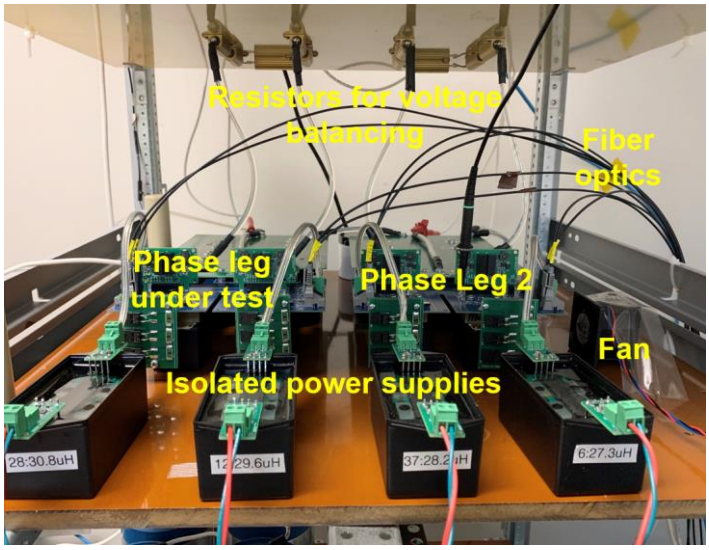


(a)

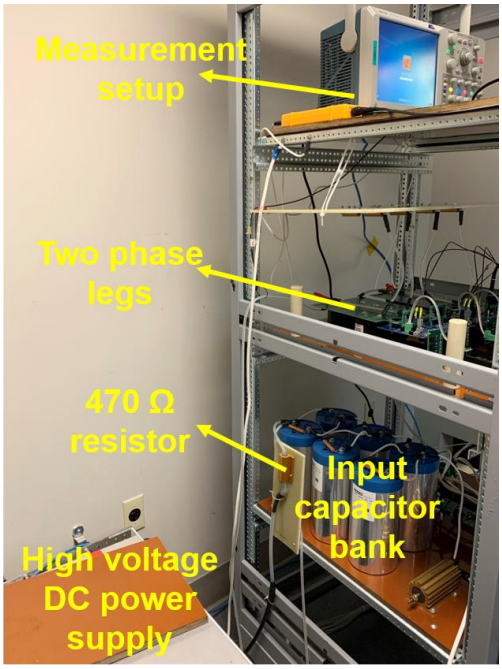


(b)

Fig. 7- 4. Simulated phase leg voltage waveforms (modulation index m=0.25, V_g= 6 kV, R_{load} =1 Ω, L_{load} =175 mH): (a) Without parallel resistor for voltage balancing; (b) With a 100 kΩ parallel resistor for voltage balancing.



(a)



(b)

Fig. 7- 5. Experimental setup of the ac-dc continuous test circuit: (a) Zoom-in view of the two cascaded phase legs; (b) Overview of the whole test setup (the load inductor is not visible).

dc power supply, a 470 Ω resistor is inserted between the DC+ terminal of the power supply and C_{in}, otherwise an overcurrent fault will be reported from the power supply.

As can be seen in Fig. 7-5(a), two phase legs are placed next to each other. Each phase leg has two 24 V isolated power supplies with 20 kV insulation capability to provide the auxiliary power [110], whose primary side is connected to a 120 V AC power adapter. Each phase leg has a 500 kΩ resistor for voltage balancing which is composed of five 100 kΩ resistors (RH050100K0FE02 from Vishay) in series to support the continuous test up to 6 kV V_g. Without any additional heatsinks or fans, the 500 kΩ resistor has a power rating of 100 W, which is 39% higher than its expected power loss at 6 kV. The 500 kΩ resistor can support the test setup even when nonideal factors result in I_{offset} up to 4 mA and the voltage of one phase leg up to 7 kV. As shown in Fig. 7-5, the resistors for voltage balancing are placed on a garolite board.

The cabinet is solidly grounded by connecting it with the grounded case of the high voltage dc power supply to achieve single-point grounding. The DSP controller and human-machine interface (HMI) are far away from the high voltage test setup and isolated via fiber optics. The selected fundamental frequency is 300 Hz, which is higher than 60 Hz in order to limit the magnitude of the load current. The switching frequency of the 10 kV SiC MOSFETs is 10 kHz.

Experimental results of the ac-dc continuous test at 2.1 kV dc-link voltage are displayed in Fig. 7-6 and Fig. 7-7. Before the continuous test, both phase legs have passed the first two steps of the proposed test scheme. Both phase legs have the same gate resistance: 15 Ω for turn-on, and 3 Ω for turn-off. In terms of the measurement setup, a

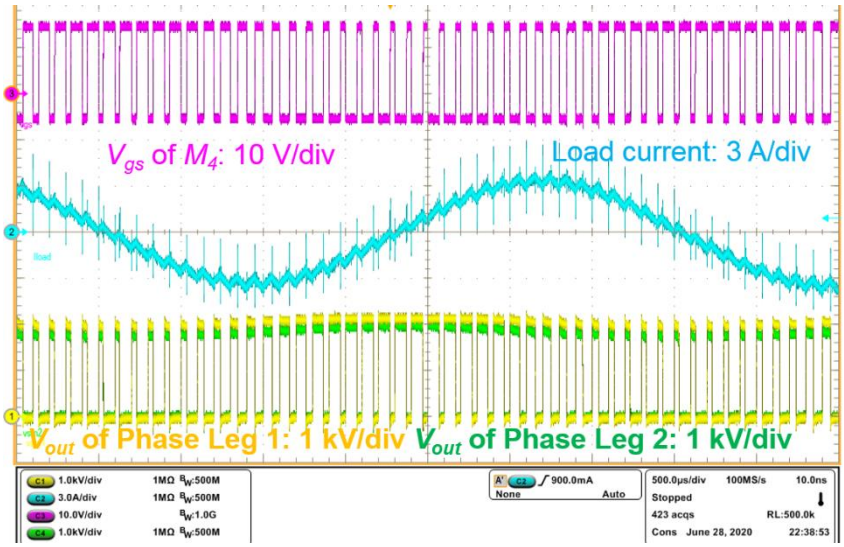
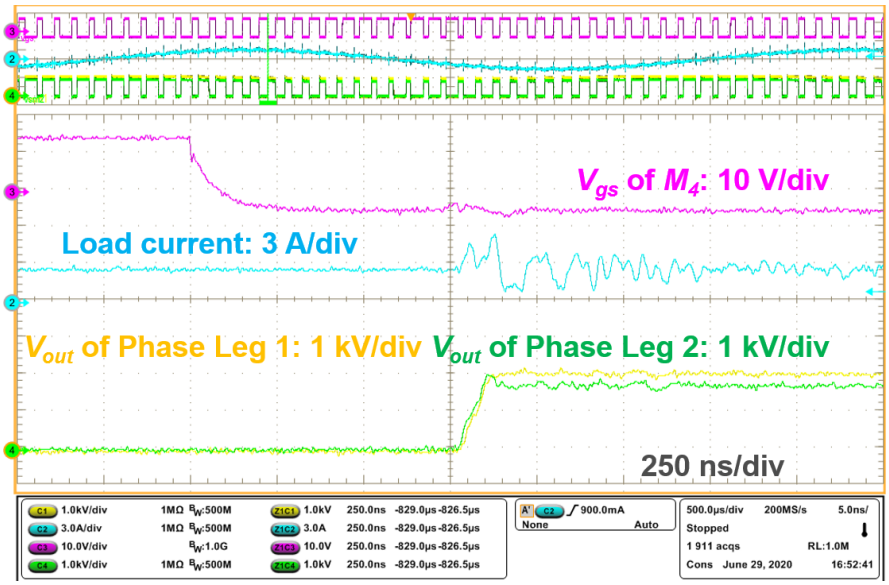
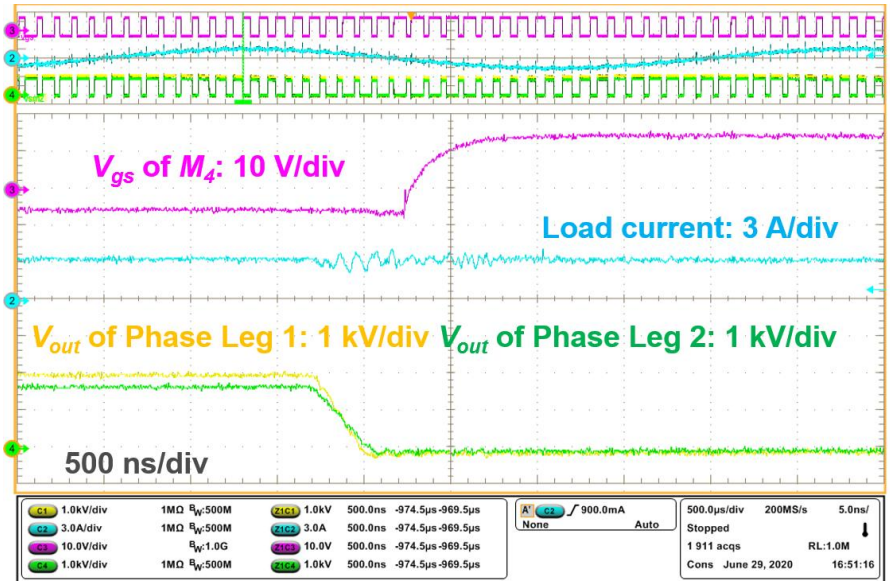


Fig. 7- 6. Waveforms of the continuous test with the proposed ac-dc continuous test circuit at 2.1 kV.



(a)



(b)

Fig. 7- 7: Zoom-in waveforms of the continuous test with the proposed ac-dc continuous test circuit at 2.1 kV: (a) Phase leg output voltage rises; (b) Phase leg output voltage decreases.

CWT Ultra Mini Rogowski coil from PEM is adopted for the load current measurement, and two differential voltage probes are used to measure the output voltage of the two phase legs. V_{gs} of M_4 is monitored by a low voltage passive probe TPP1000 from Tektronix, whose source is solidly grounded. With a modulation index of 0.45, the sinusoidal load current with 10 kHz ripple has a peak value of ~3 A, which coincides with the estimation result and the simulation result.

The voltage of two phase legs is well balanced with the help of the 500 kΩ parallel resistor. The voltage difference between the two phase legs V_{offset} is less than 250 V with a dc-link voltage of 2.1 kV. In fact, only one pair of PWM signal is generated in the DSP controller, so the same gate signal is sent to the gate driver of M_1 and M_3 via fiber optics, as well as M_2 and M_4. The voltage difference is mainly attributed to the phase shift between the V_{gs} of M_1 and M_3, and M_2 and M_4, which is due to the propagation delay difference of the components in the gate driver board. According to the zoom-in waveforms in Fig. 7-7, the output voltage of the two phase legs rises and drops almost simultaneously, with a phase shift of <20 ns. It is thereby proved that the designed modulation scheme forces the source of M_1 to undergo 2X *dv/dt* that M_2 and M_3 withstand. The *dv/dt* that M_1 and M_2 of the phase leg under test experience continuously will be higher if Phase Leg 2 is modified to switch with higher *dv/dt*.

The ac-dc continuous test is successfully conducted at 6 kV dc-link voltage, with the waveforms displayed in Fig. 7-8. Since the differential voltage probe is not capable of withstanding 6 kV common mode voltage with high *dv/dt*, the output voltage of the phase leg under test (Phase Leg 1) cannot be measured any more. The output voltage of Phase

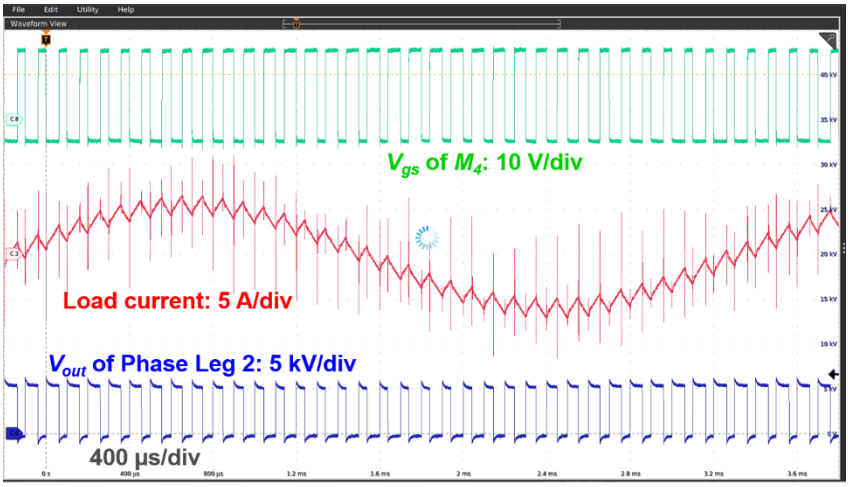


Fig. 7- 8: Waveforms of the continuous test with the proposed ac-dc continuous test circuit at 6 kV.

Leg 2 is measured with a high voltage passive probe, P6015A from Tektronix. At 6 kV, the modulation index is reduced to 0.25 because the continuous operation of the load inductor only allows <9 A peak current [1]. The maximum load current flowing through the inductor and MOSFETs is ~6 A. Because the source of M_1 experiences 2X *normal dv/dt* of the 10 kV SiC MOSFET, substantial displacement current flows through EPC of the load inductor, as clearly indicated in the measured load current waveform. Measurement results of the output voltage of Phase Leg 2 show that the dc capacitor voltage of Phase Leg 2 varies from 5.1 kV to 5.4 kV. Therefore, it is estimated that the voltage of the phase leg under test (Phase Leg 1) varies from 6.6 kV to 6.9 kV. The proposed open loop voltage balancing method effectively achieves voltage balancing in the ac-dc continuous test setup. With a larger I_{offset} due to the higher load current, the voltage difference V_{offset} is higher than 1 kV. In addition, more accurate phase leg voltage measurement results and V_{offset} can be obtained with better high voltage differential voltage probes in the future.

7.5 Summary

This chapter focuses on a simple test scheme to test phase legs based on 10 kV SiC MOSFETs comprehensively. The test scheme provides a comprehensive and efficient qualification of the phase leg, including its thermal design, insulation design, and its capability to withstand high *dv/dt*. In the test scheme, an ac-dc continuous test circuit with two phase legs in series is developed to qualify the phase leg as the final step. With the designed modulation scheme, the phase leg under test needs to continuously withstand 2X *normal dv/dt* of 10 kV SiC MOSFETs, which could occur during the operation of a real modular MV converter. In fact, the *dv/dt* that the phase leg under test will undergo is

controllable so that the capability of the phase leg to operate normally under high *dv/dt* can be fully tested and evaluated. An open loop voltage balancing method with the external parallel resistor is adopted to simplify the test setup. The developed continuous test circuit is fully validated with the built test setup and the ac-dc continuous test up to 6 kV.

CHAPTER 8. CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

10 kV SiC MOSFETs with superior device performance are one of the essential enablers of future MV converters with higher efficiency and control bandwidth as well as much smaller size and weight. To apply them in modular MV power conversion systems, a series of challenges caused by device-level characteristics of 10 kV SiC MOSFETs should be addressed, such as high blocking voltage and high *dv/dt*. This dissertation, throughout which these challenges are analyzed and tackled, intends to investigate the switching performance evaluation, design, and testing of a robust 10 kV SiC MOSFET based phase leg for modular MV converters.

First, a baseline design of a 6.5 kV HB phase leg based on 10 kV SiC MOSFETs is presented for continuous operation as a building block of a modular MV converter. The developed gate driver is equipped with numerous functions to support continuous operation of the phase leg. Baseline testing procedures are developed to validate the baseline design.

Then, how the parasitic capacitances in the MV converter and the freewheeling diode influence the switching performance is evaluated in detail. Higher EPC of the load inductor makes switching transients slower, leading to lower turn-off loss and higher total switching energy loss. The parasitic capacitance caused by the heatsink prolongs switching transitions and increases the switching loss. With negligible reverse recovery charge, the body diode is suitable to serve as the freewheeling diode in the HB phase leg. Adding the

10 kV anti-parallel JBS diode is not recommended because it introduces additional parasitic capacitance and leads to higher switching loss.

The 10 kV SiC MOSFET under the flashover fault caused by premature insulation failure is studied in detail, where *dv/dt* and *di/dt* are much higher than those under conventional short circuit faults. To reduce the overvoltage and short circuit current under a flashover fault, a higher $R_{g,off}$ is suggested for 10 kV SiC MOSFETs without Kelvin source to avoid a large $R_{g,on}/R_{g,off}$, while a small $R_{g,off}$ is recommended for the MOSFET with Kelvin source. The analysis also provides design guidelines about the gate loop inductance and whether to add an external capacitor across gate and source terminal. Based on simulation results at 7 kV, the short circuit energy loss is compared between the flashover fault and two conventional short circuit faults, HSF and FUL. The required response time to clear a flashover fault should be shorter than the response time determined by conventional short circuit faults.

The noise immunity of the desat protection for 10 kV SiC MOSFETs and other high voltage SiC MOSFETs is examined quantitatively and comprehensively in the pursuit of the desat protection with faster response and strong noise immunity. The main concern is the high positive dv_{ds}/dt: the high dv_{ds}/dt together with the long voltage rise time makes the desat protection for high voltage SiC MOSFETs more vulnerable to noise than the desat protection for other Si and SiC devices, as shown in Fig. 6-11. Design guidelines are summarized to improve noise immunity of the desat protection. Leveraging the knowledge acquired in noise immunity analysis, an improved desat protection scheme with digital blanking time is developed for 10 kV SiC MOSFETs to realize fast response and excellent

noise immunity concurrently. The response time is 340 ns under the HSF, and the response time is 195 ns under the FUL at 6.5 kV. Furthermore, a proposed desat protection scheme with ultrafast response can protect the 10 kV SiC MOSFET with even shorter response time: 115 ns under the HSF and 155 ns under the FUL. The proposed desat protection scheme with ultrafast response also features excellent noise immunity and simple circuitry that is compatible with the conventional desat protection circuitry.

Finally, a simple test scheme has been proposed and validated to thoroughly test HB phase legs based on 10 kV SiC MOSFETs. With an ac-dc continuous test circuit featuring two phase legs connected in series, the test scheme provides a comprehensive and efficient qualification of the phase leg as a robust building block for modular MV converters, including its thermal design, insulation design, and its capability to withstand high *dv/dt* and its resulting noise. In the continuous test circuit, the *dv/dt* is controllable to fully test the operation of the phase leg under high *dv/dt*.

8.2 Future Work

With much higher *dv/dt* and *di/dt* than Si IGBTs, the switching transients of 10 kV SiC MOSFETs are sensitive to both parasitic capacitances and parasitic inductances in the MV converter. Only parasitic capacitances' impact on switching transients is studied in this work, since the parasitic inductance is not a dominant influencing factor in the switching transient of the 10 kV/20 A SiC MOSFET [31]. However, parasitic inductance, especially the power loop inductance, could cause much more significant ringing and higher overvoltage in 10 kV SiC MOSFET modules with higher current rating and higher *di/dt*, and hence should be addressed in future work [111].

Regarding the gate driver design for 10 kV SiC MOSFETs, one of the challenges is how to deal with the CM current and its resulting noise, which is not covered in detail in this dissertation. The CM current results from the parasitic capacitance C_{ps} of the isolated power supplies in the modular MV converters and the high *dv/dt*. The CM current could lead to the malfunction of the gate driver if it is sufficiently large. However, how the CM current impacts the normal operation of the gate driver has not been thoroughly investigated, and the interference mechanisms should be clearly identified. Gate driver design guidelines should be provided to solve the problems induced by the CM current, in addition to reducing C_{ps} of the isolated power supply.

In this dissertation, the noise immunity analysis of desat protection circuitry assumes that the *dv/dt* is a constant during the voltage rise/fall time of V_{ds}. Nevertheless, *dv/dt* is not necessarily a constant in some cases. For example, the instantaneous *dv/dt* can change significantly when only partial ZVS is achieved due to low load current. In this case, the peak *dv/dt* is substantially higher than the average *dv/dt* calculated between 90% and 10% of V_{ds}. It will be useful to study the noise immunity of desat protection circuitry when the constant *dv/dt* assumption is not valid. How the average *dv/dt* and the peak *dv/dt* interfere with the circuitry will be revealed in such analysis, and the analysis results will make the noise immunity margin model more comprehensive.

In terms of the flashover fault study, a comprehensive discussion of methods to alleviate the impact of a flashover fault is still greatly needed. It is also necessary to establish a high voltage test platform for the flashover fault and develop protocols to ensure that the test is safe and nondestructive. The experimental validation of the analysis based

on simulation results as well as discussions based on test results will benefit the study of the flashover fault and guide the SiC-based MV converter design in the future.

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VITA

Xingxuan Huang was born in June, 1995, in Jiangxi Province, China. He started his undergraduate study in Xi'an Jiaotong University in 2012 at Xi'an, China, and graduated with a bachelor's degree in Electrical Engineering in 2016. He then moved to the US and began his graduate research with a concentration on power electronics at The University of Tennessee at Knoxville (UTK) in 2016 and received his MS degree in Electrical Engineering from UTK in 2019. In his spare time, he enjoys outdoor activities in East Tennessee, such as jogging, hiking, kayaking, etc.