Analysis and Development of Multiple Phase Shift Modulation in A SiC-Based Dual Active Bridge Converter

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ABSTRACT

Renewable energy adoption is a popular topic to release the stress of climate change caused by greenhouse gas. Electricity is ideal secondary energy for clean primary energy such as nuclear, wind, photovoltaic, and so on. To extend the application of electricity and reduce fossil energy consumption by transportation sectors, electric vehicles (EVs) become promising technology that can further inspire the development of renewable energy.

Battery as the core in an EV provides the energy to the motor and all onboard electric equipment. The battery charger is mainly composed of a power factor correction (PFC) and isolated DC-DC converter. Therefore, power electronics equipment plays an important role in automotive products. Meanwhile, in recent years, the market capacity for wide band-gap devices, SiC MOSFET, continues to increase in EV applications.

Dual active bridge (DAB) is an excellent candidate for isolated DC-DC converter in EV battery chargers. The characteristics include an easy control algorithm, galvanic isolation, and adjustable voltage gain. Different modulation strategies are developed to improve the performance and stability by using multiple phase shift (MPS) control. This thesis focuses on the utilization of different modulation strategies to realize smooth transition among MPS control in full operational range with securing zero-voltage-switching (ZVS) to eliminate the crosstalk in the hard-switching process. The influence of MPS control on ZVS resonance transient is also addressed to find out the accurate minimum required energy of the inductor to finish the ZVS transition. Furthermore, a

general common-mode voltage model for DAB is proposed to analyze the impact of MPS control on the common-mode performance.

TABLE OF CONTENTS

Chapter 1 INTRODUCTION 1

1.1 DC-DC Converter Applications in EV Charger 1

1.1.1 Battery Chargers of EVs 2

1.1.2 The Dual Active Bridge in EV Battery Charger 4

1.2 SiC MOSFET Implementations in Renewable Energy Applications 8

1.2.1 Benefits of SiC MOSFET Implementations 8

1.2.2 Challenges of SiC MOSFET Implementations 13

1.3 Research Objectives and Thesis Layout 20

Chapter 2 LITERATURE REVIEW 23

2.1 Zero-Voltage-Switching Realization 23

2.2 Definition of Modulation Strategies in DAB Converter 29

2.3 Modulation Strategies in Dual Active Bridge 31

2.3.1 Single Phase Shift (SPS) Modulation 31

2.3.2 Dual-Phase Shift (DPS) Modulation 36

2.3.3 Triple Phase Shift (TPS) Modulation 41

2.3.4 Multiple Phase Shift (MPS) Modulation 43

2.3.5 Hybrid Modulation 45

2.4 Common-mode (CM) Analysis in Dual Active Bridge 47

2.5 Current Spike Elimination Method in Dual Active Bridge 53

2.6 Summary 62

Chapter 3 SMOOTH TRANSITION PROCESS IN MULTIPLE PHASE SHIFT MODULATION 66
3.1 Zero-voltage-switching (ZVS) in DAB-Based Battery Charger 66
3.2 Modulation Strategy within the Whole Operational Range 71
3.3 Switching Waveform of Multiple-Phase-Shift Modulation 76
3.3.1 Switching modes when $V_{in} > nV_o$ 76
3.3.2 Switching modes when $V_{in} < nV_o$ 82
3.4 Boundary Conditions and State Machine 88
3.5 Charger Utility Control 95
3.5.1 Pre-charge Mode 95
3.5.2 Grid to Vehicle (G2V) and Vehicle to Grid (V2G) Modes 95
3.6 Experimental Verification 102
3.7 Conclusion 105
Chapter 4 COMPLETE ZERO-VOLTAGE-SWITCHING ANALYSIS IN DUAL ACTIVE BRIDGE 109
4.1 Non-linear Capacitance of Switches 109
4.2 Circuit Patterns 113
4.2.1 Modulation without Inner Phase Shift 113
4.2.2 Modulation with Inner Phase Shift 117
4.3 Simulation in MATLAB 120
4.4 Experiment Verification 122

4.5 Comparison between Existing ZVS Current Requirement 127
4.6 Conclusion 127
Chapter 5 ANALYTICAL COMMON-MODE VOLTAGE MODEL IN DUAL ACTIVE BRIDGE 132
5.1 Consideration of Parasitic Capacitance in DAB Common-mode Analysis 132
5.1.1 Parasitic Capacitor in Grounded Heatsink 132
5.1.2 Common-mode Capacitance in Transformer 133
5.2 General Common-mode Parasitic Capacitance in DAB 136
5.3 Generalized Common-mode Voltage Model 138
5.4 Consideration of Common-mode Voltage Based on Multiple Phase Shift Modulation 147
5.5 Experimental Verification 151
5.5.1 Testing the CMV 153
5.5.2 Testing the CM Current 160
5.6 The Influence of Modulation on the Common-mode Chock Design 160
5.7 Conclusion 169
Chapter 6 TRANSFORMER CURRENT SPIKE ELIMINATION DURING THE LOAD TRANSIENT 171
6.1 Root Cause of the Current Spike in Transformer 171
6.2 Unified Transformer Current in Multiple Phase Modulation 176
6.3 Active Compensation Between Different Patterns 179

6.4 Duty Cycle Compensation to Eliminate Current Spike 182
6.4.1 Load Current Increasing 182
6.4.2 Load Current Decreasing 184
6.5 Control Algorithm Implementation 186
6.6 Experimental Verification 186
6.7 Conclusion 190
Chapter 7 CONCLUSION AND FUTURE WORK 194
7.1 Conclusions 194
7.2 Future Work 195
7.2.1 Small-signal Model for MPS Modulation 195
7.2.2 Voltage Balancing Control for DAB Converter with Input-Series-Output-Parallel 196
LIST OF REFERENCES 201
VITA 227

LIST OF TABLES

Table 1.1. Comparison of power losses and heatsink size between Si-IGBT and SiC MOSFET in 22kW EV Charger [30]. 11

Table 2.1. Summary of different modulation strategies. 48

Table 3.1. Definition and Values of Symbols 73

Table 3.2. Boundary Conditions. 94

Table 4.1. ZVS Transition time in Figure 4.6 (a). 123

Table 4.2. ZVS Transition time in Figure 4.6 (b). 123

Table 4.3. Prototype Setup 124

Table 4.4. Transition time comparison 124

Table 4.5. Comparison of minimum initial inductor energy 130

Table 5.1. General CM Parasitic Capacitance in DAB 140

Table 5.2. Summary of Parasitic Capacitance 145

Table 5.3. Secondary-side CMV Comparison between Analytical Model and Experiment 157

Table 5.4. Dimension of the CM Filter and Charger Prototype 168

Table 6.1. Prototype Setup. 173

LIST OF FIGURES

Figure 1.1. Global electric passenger car stock, 2010-2020 [7]. 3

Figure 1.2. EV battery charger: (a) off-board charger; (b) on-board charger [8] 3

Figure 1.3. The differences between AC/DC charging stations and onboard chargers [14]. 5

Figure 1.4. Comprehensive functions of EV battery chargers [15]. 5

Figure 1.5. Topology of the DAB converter. 5

Figure 1.6. EV on-board battery charger: (a) 2kW automotive DAB converter [11]; (b) 3.7 kW, single-phase, single-stage, bidirectional and isolated DAB ac–dc converter prototype [20]: (c) 20 kW DAB converter [21]. 7

Figure 1.7. An SST-enabled hybrid dc/ac microgrid system [26]. 9

Figure 1.8. Rated voltage range for Si and SiC (MOSFET and IGBT) [29]. 11

Figure 1.9. Breakdown of SiC-based on-board vehicle battery charger for: (a) mass considerations and..... 12

Figure 1.10. Main application areas of SiC and GaN power devices [35]. 14

Figure 1.11. 2019-2025 Power SiC device market forecast [36]. 14

Figure 1.12. Switching waveforms of CMF20120D (SiC-MOSFET), IPW65R065C7 (Si-MOSFET) and IKW25N120T2 (Si-IGBT) [37]. 15

Figure 1.13. Mechanism of bridge-leg crosstalk during switching transients of QH: (a) Turn-on transient; (b) Turn-off transient; (c) switching waveforms [42]. 17

Figure 1.14. Illustration of the impact of high-signal edge rates on WBG converter spectral content [43]. 19
Figure 1.15. Sources of EMI in EVs [44]. 19
Figure 2.1. Energy-based ZVS realization in a half bridge: (a) half bridge circuit; (b) voltage across the switches and the inductor current during ZVS transient [56]. 25
Figure 2.2. DAB converter with the output bridge replaced by an equivalent voltage source during turnoff of devices T1, T4 of input bridge; (b) minimum inductor current required at the instant of turnoff of T1, T4 to resonate the pole voltage from $+V_i$ to $-V_i$ [57]. 25
Figure 2.3. Soft-switching transition of a MOSFET bridge leg and an inductor L: (a) free-wheeling interval with inductor current $i_L = I_1$; (b) switch S_2 turns off and resonant transition starts with an additional current path through the dc source (For simplicity reasons, the parasitic output capacitances are assumed to be linear.); (c) end of transition when the drain-source voltage of S_2 has reached the source voltage [63].27
Figure 2.4. Simulation results in (a) Ltspice and (b) Simulink showing the 28
Figure 2.5. Main operation waveforms of the phase-shift control method [69]. 30
Figure 2.6. Transformer Voltage: (1) SPS [69]; (2) DPS [70]; (3) TPS [71]. 30
Figure 2.7. Power vs phase shift in DAB SPS [87]. 33
Figure 2.8. Typical voltage and current waveforms for Vin>nVo and Vin=nVo: (a) Common mode; (b) Boundary mode; (c) Extreme mode, Vin=nVo [19]..... 33
Figure 2.9. Datasheet of CREE's SiC MOSFET - C2M0025120D [95]. 35

Figure 2.10. ZVS operation range [69]. 35
Figure 2.11. EPS control switching waveform [67]. 37
Figure 2.12. Characteristics of EPS modulation: (a)3-D curves of the unified backflow power varied with D_1 and D_2 ; (b) power versus D_2 [67]. 37
Figure 2.13. Typical waveforms for EPS: (a) Buck mode (V1.nV2) for S1 leading Q1, (b) Buck mode (V1>nV2) for S1 lagging Q1 [98]. 38
Figure 2.14. Switching waveform: (a) SDPS modulation; (b) PDPS modulation [13]. ... 40
Figure 2.15. Single-phase charging module [13]. 40
Figure 2.16. Switching waveform: (a) overlap TPS modulation; (b) non-overlap TPS [99]. 42
Figure 2.17. Output power versus primary active-phase-shift when $V_{in} < nV_o$ [99]. 42
Figure 2.18. Switching waveform of in-phase TPS [106]. 44
Figure 2.19. DAB operating modes at different voltages and loads [88]. 44
Figure 2.20. (a) Experimental DAB waveforms at 5.1 kW. (b) Phase-shift jumping region [99]. 46
Figure 2.21. The work mode transition of HPPS control with different loads [108]. 46
Figure 2.22. Six lumped capacitances model [115]. 50
Figure 2.23. Single-phase full-bridge with parasitic capacitances and switching nodes [118]. 50
Figure 2.24. Six possible two-capacitor CM winding capacitance models for a two-winding transformer [116]. 51

Figure 2.25. Equivalent circuit of the H-bridge in CM [117]. 51
Figure 2.26. Measured EMI spectrum and the predicted EMI spectrum envelope of the LLC prototype with the proposed CM choke [114]. 52
Figure 2.27. Conventional single-phase DAB system with half-bridge on MVDC side [118]. 54
Figure 2.28. Application of the grid-connection DAB converter. 56
Figure 2.29. Block diagram of the MPS control scheme with the output current and input voltage feedforward for DAB DC-DC converters [76]. 58
Figure 2.30. Topology of DAB converter with digital control [124]. 58
Figure 2.31. Transient waveforms under the SPS updating strategy with a constant power flow: (a) Increase in power; (b) Decrease in power [128]. 60
Figure 2.32. Waveforms of the working mode transition without dc bias current [130]. 61
Figure 2.33. Gate signal generation: (a) for the primary-side switches;(b) for the secondary-side switches [130]. 63
Figure 2.34 Generalized closed-loop control block diagram for the DAB converter [127]. 63
Figure 3.1. Three-phase PFC + DAB for a two-stage battery charger. 67
Figure 3.2. Prototype of the battery charger. 69
Figure 3.3. Influences of switching action on the gate signal in a bridge leg (experimental results): (a) hard-switching-on; (b) soft-switching-on. 69
Figure 3.4. Charging profile of an EV battery charger. 72

Figure 3.5. Drain-source current for each switch when turning on: (a) primary side P1; (b) secondary side S1. 75
Figure 3.6. Definition of different phase shifts. 75
Figure 3.7. Switching waveform of state4 (SPS): (a) design waveform; (b) experiment waveform @ input voltage 700V, output voltage 200 and 11kW. 77
Figure 3.8. Switching waveform of state3 (DPS): (a) simulation waveform; (b) experiment waveform @ input voltage 700V, output voltage 200 and 10kW. 77
Figure 3.9. Switching waveform of state2 (DPS): (a) design waveform; (b) experiment waveform @ input voltage 700V, output voltage 200 and 8kW. 79
Figure 3.10. Switching waveform of state1(DPS): (a) simulation waveform; (b) experiment waveform @ input voltage 700V, output voltage 200 and 4kW. 79
Figure 3.11. Switching waveform of state0 (TPS): (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 200 and 1kW. 81
Figure 3.12. Switching waveform of state4, SPS: (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 450V, and 20kW. . 83
Figure 3.13. Switching waveform of state5, DPS: (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 450V and 17kW. .. 83
Figure 3.14. Switching waveform of state6, DPS: (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 450V, and 12.6kW. 84

Figure 3.15. Switching waveform of state7, DPS: (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 450V, and 4kW. ... 86
Figure 3.16. Switching waveform of state8, TPS: (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 450V and 1.8kW. . 86
Figure 3.17. Long-dead-time effect: (a) with dead-time effect; (b) without dead-time effect. 89
Figure 3.18. Dead-time effect (experiment). 89
Figure 3.19. Setting the boundary current based on dead time. 91
Figure 3.20. Battery charging curve and related operational states. 93
Figure 3.21. Connections among different states. 93
Figure 3.22. Different phase shifts vs Power: (a) V_o 200V; (b) V_o 450V. 96
Figure 3.23. Pre-charge process. 96
Figure 3.24. Switching performance at the beginning of the pre-charge mode. 97
Figure 3.25. Control algorithm of G2V mode. 99
Figure 3.26. G2V and V2G modes. 101
Figure 3.27. Switching modes boundary between G2V and V2G. 101
Figure 3.28. 200V constant voltage source load to validate the smooth transitions between different modulation strategies. 103
Figure 3.29 10Ω resistive load to validate the smooth transition between different modulation strategies. 103
Figure 3.30. Pre-charge mode with zoom-in waveforms. 104

Figure 3.31. Transition test between V2G and G2V from -10A to +10A with zoom-in waveforms. 106
Figure 3.32. Transition between current control mode and voltage control mode: (a) overall waveform; (b) transition from current control mode to voltage control mode; (c) transition from voltage control mode to current control mode. 107
Figure 4.1. Simplified circuit for ZVS analysis based on H-bridge. 110
Figure 4.2. Characteristics of nonlinear output capacitance in one bridge leg: (a) ZVS transition; (b) C_{oss}; (c) E_{oss}; (d) Q_{oss}. 111
Figure 4.3. H-bridge ZVS transient process without the inner phase shift: (a) transient process; (b) transient process waveforms; (c) for SPS; (d) for DPS..... 114
Figure 4.4. H-bridge ZVS transient process with inner phase shift: (a) transient process; (b) transient process waveform; (c) implementation in SPS; (d) implementation in DPS; (e) and (f) examples for DPS. 118
Figure 4.5. Simulink model of primary-side H-bridge in DAB..... 121
Figure 4.6. Simulation and estimation result of ZVS transition without inner phase shift: (a) ±400V reflected output voltage; (b) ±500V reflected output voltage. 121
Figure 4.7. H-bridge prototype. 125
Figure 4.8. Example of the switching waveform. 125
Figure 4.9. I-V curve comparison based on the modulation without inner phase shift @ [V_{in}, V_s, $i_L(0)$]..... 126

Figure 4.10. I-V curve comparison based on the modulation with inner phase shift-lower switch ZVS @ [V_{in}, V_s, $i_L(0)$]. 126
Figure 4.11. I-V curve comparison based on the modulation without inner phase shift-upper switch ZVS @ [V_{in}, V_s, $i_L(0)$]. 128
Figure 4.12. Comparison of minimal initial inductor current: (a) Without inner phase shift; (b) With inner phase shift 1; (c) With inner phase shift 2. 129
Figure 5.1. Equivalent parasitic capacitance of different switches to heatsink: (a) TO-247 package switch; (b) the equivalent capacitor to ground in TO-247 package [149]; (c) GS66508T [150]; (d) the equivalent capacitor to ground of GS66508T. 134
Figure 5.2. Transformer considering parasites in the CM analysis: (a) the distribution of the parasitic capacitance between the primary side and secondary side of the transformer: (b) the transformer model with parasitic capacitances. 135
Figure 5.3. General parasitic capacitance from topology to ground in DAB converter. 137
Figure 5.4. General common-mode topology of the DAB converter. 137
Figure 5.5. Decomposed circuit with Superposition theorem: (a) CM loop with first phase leg at the primary side; (b) CM loop with second phase leg at the primary side; (c) CM loop with first phase leg at the secondary side; (d) CM loop with second phase leg at the secondary side. 139
Figure 5.6. Thevenin's theorem application: (a) Two-port network; (b) equivalent voltage source; (c) equivalent impedance. 142
Figure 5.7. Common-mode loops in the DAB converter. 145

Figure 5.8. Switching waveforms of different modulations: (a) SPS; (b) PDPS; (c) SDPS; (d) TPS. 148
Figure 5.9. Ltspice simulation result of input and output CMV in TPS modulation @ input voltage 400V, output 150V, and 500W. 150
Figure 5.10. Experimental set-up. 152
Figure 5.11. CMV in different modulation strategies: (a) TPS @ 150V output voltage: (b) PDPS @ 150V output voltage; (c) TPS @ 250V output voltage; (d) SDPS @ 250V output voltage; (e) SPS (continued). 155
Figure 5.12. CMV spectrums of different modulation strategies: (a) TPS, PDPS, and SPS when M<1; (b) all discussed modulation strategies. 158
Figure 5.13. The comparison of the CMV distribution between experiments and simulation model. 159
Figure 5.14. Prototype structure with LISNs. 161
Figure 5.15. CMI spectrums of different modulation strategies tested with LISNs: (a) TPS, PDPS, and SPS when M<1; (b) all modulation strategies. 162
Figure 5.16. EV high-voltage pack [151]. 164
Figure 5.17. CM current flows between the high-voltage battery and vehicle chassis. . 164
Figure 5.18. Model-based predicted CM envelop and the measured CM spectrum. 165
Figure 5.19. Component at 300kHz in CM spectrum with SDPS modulation. 165
Figure 5.20. Component at 300kHz in CM spectrum with MPS modulation. 167
Figure 5.21. CM chock design with the analytical CM model. 167

Figure 5.22. Two-stage CM filter. 168

Figure 5.23. A typical block diagram of a DC charging station [14]. 168

Figure 6.1. The structure of the closed-loop control in the DAB converter. 173

Figure 6.2. Simulation waveform during load transient with the transformer current spike: (a) load current increasing with the current spike in the transformer; (b) zoomed-in waveforms. 174

Figure 6.3. The switching waveform of the proposed modulation strategies: (a) the modulations without the unified switching current; (b) PDPS and TPS when $V_{in}>nV_o$; (c) SDPS and TPS when $V_{in}<nV_o$; (d) SDPS when $V_{in}=nV_o$. 175

Figure 6.4. Example of phase shift vs output..... 180

Figure 6.5. Transformer current spike elimination strategy: (a) Operational area for different modulations; (b) example of the active compensation between SPS and other modulations. 181

Figure 6.6. Current Spike elimination: (a) modulation switching from TPS to SPS (light load to heavy load); (b) modulation switching from TPS to PDPS (light load to medium load); (c) modulation switching from PDPS to SPS (medium load to heavy load); (d) modulation switching from SPS to TPS (heavy load to light load)); (e) modulation switching from PDPS to TPS (medium load to light load)); (f) modulation switching from SPS to PDPS (heavy load to medium load)..... 183

Figure 6.7. Structure of the control loop in DAB. 187

Figure 6.8. Duty-cycle compensation method: (a) calculation of duty cycle; (b) implementation of compensation duty cycle. 188
Figure 6.9. Transformer current spike when step change of phase shift happens, without the duty cycle compensation: (a) from TPS to SPS; (b) from SPS to TPS..... 189
Figure 6.10. Experimental waveforms during load transient: (a) TPS0 to PDPS1 without active compensation; (b) PDPS1 to PDPS2 without active compensation; (c) TPS0 to SPS with active compensation; (d) TPS7 to SDPS5 without active compensation; (e) TPS7 to SDPS6 without active compensation; (f) TPS7 to SPS with active compensation. 191
Figure 6.11. Experimental waveforms during load transient: (a) SDPS6 to SDPS5 without active compensation; (b) SDPS6 to SPS with active compensation..... 192
Figure 7.1. Magnitude of the averaged small-signal model at 100Hz: (a) SPS; (b) MPS [124]..... 197
Figure 7.2. Topology of the DAB ISOP DC-DC converter [161]..... 199
Figure 7.3. Example of the central controller method. 199
Figure 7.4. Control-loop for ISOP DAB converters. 200

Chapter 1 INTRODUCTION

This chapter starts with an introduction to the background of renewable energy. The necessity of developing renewable energy is discussed. As an important part of renewable energy, the development of the electric vehicle (EV) is also demonstrated. A dual active bridge (DAB) converter with characteristics of galvanic isolation and adjustable voltage plays an essential role in EV battery chargers. Then SiC devices as an excellent alternative to the traditional Si devices are introduced in power electronic equipment, which comes with both benefits and challenges. Finally, the layout of the thesis is provided.

1.1 DC-DC Converter Applications in EV Charger

In 2020, according to the data released by U.S. Energy Information Administration (EIA), U.S. primary energy consumption is 92.94 quadrillion British thermal units (Btu), which mainly includes fossil fuels, nuclear energy, and renewable energy [1]. From the source point of view, around 79% of the total energy consumption comes from fossil fuels, and only 12% is renewable energy. From the user end, most energy is dissipated in the industrial, transportation, and residential sectors. The heavy usage of fossil fuels brings a burden on the environment. So how to develop renewable energy becomes an important topic worldwide. Despite the pandemic in 2020, the annual growth rate of renewable energy capacity in the world increased by 45% [2]. As the secondary energy, total U.S. electricity consumption in 2020 was about 3.8 trillion kWh and 13 times greater than electricity use in 1950 [3], which is mainly composed of residential, commercial, and

industrial parts. Such tremendous demand needs to consume enormous primary energy.To keep the sustainable development, the U.S. EIA projects that the share of renewables in the U.S. electricity generation mix will increase from 21% in 2020 to 42% in 2050 [4].

1.1.1 Battery Chargers of EVs

As a main end-use sector of energy consumption, transportation represents nearly 35% of U.S. total energy consumption. And 90% of the energy source to support transportation is petroleum [1]. As a replacement for the transitional vehicles driven by petroleum, the global market for electric vehicles shows fast growth. In 2020, the global electric passenger car stock is more than 10 million in Figure 1.1. Based on the current trends and policies, it projects the number of electric cars, vans, heavy trucks, and buses on the road worldwide to reach 145 million by 2030 [5].

With the increasing demand for EVs, the battery charger becomes a new rising technique. On the market, there are two types of battery chargers in Figure 1.2. One is off-board chargers, as shown in Figure 1.2 (a). Without adding cost and weight directly to EVs, the power rating of the AC/DC converter and DC/DC could be enlarged, e.g., 22kW to 50kW.

Another one is the onboard charger, which is installed inside the vehicles. The structure of the onboard charger is shown in Figure 1.2 (b), comprising of AC/DC and DC/DC converter. Hence the volume and the power density of onboard chargers have strict requirements. The power rating of the onboard charger is usually from 3.7kW to 22kW [6]. On-board chargers are widely used in plug-in hybrid electric vehicles (PHEV) or as the alternative to the off-board charger in EVs. The difference between on-board chargers and

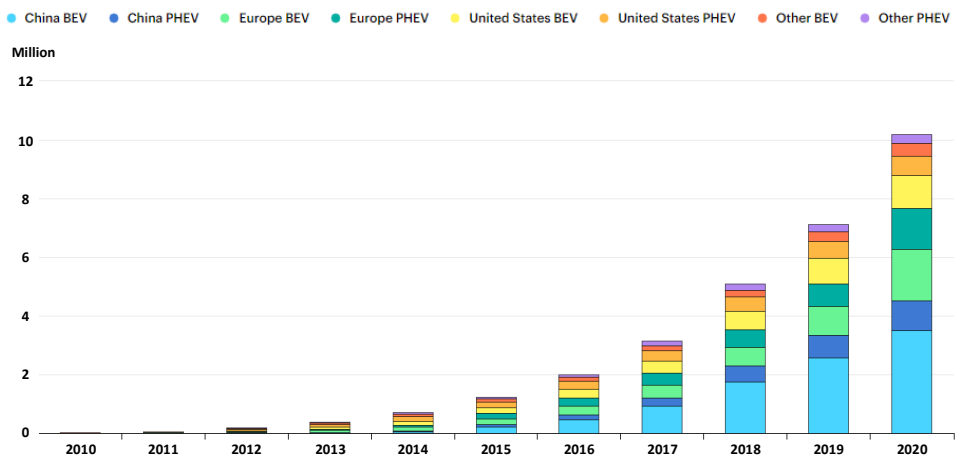
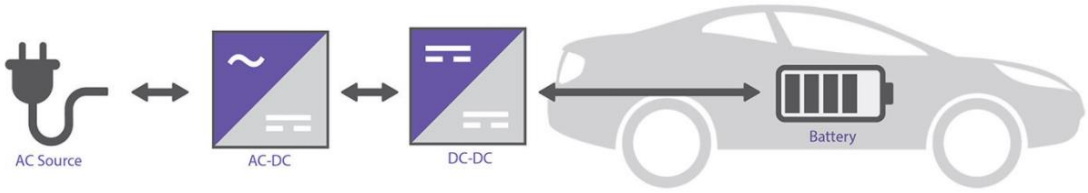
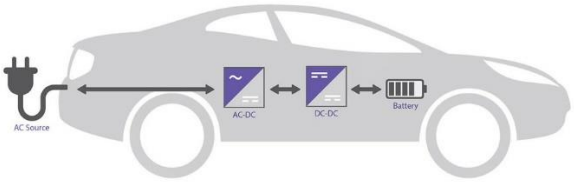


Figure 1.1. Global electric passenger car stock, 2010-2020 [7].



(a)



(b)

Figure 1.2. EV battery charger: (a) off-board charger; (b) on-board charger [8]

an off-board type is shown in Figure 1.3. More detailed SAE charging configurations and the rating terminology can be found in [9].

1.1.2 The Dual Active Bridge in EV Battery Charger

A DC-DC converter is an essential part of the EV battery charger. At first, for safety concerns, DC-DC converter needs to have galvanic insulation to make sure the high voltage battery on the vehicle is isolated from the local grid. Secondly, the normal battery voltage in EV could be 200V ~ 800V [10]. Such a DC-DC converter should be able to operate under a wide voltage range. Last but not the least, the battery inside the vehicle can be regarded as part of the energy storage system. So the bidirectional feature of the DC-DC converter allows the power to flow back to the grid. Figure 1.4 shows the comprehensive functions of EV battery chargers. For example, the energy stored in the batteries can be sent to the AC grid or DC micro-grid, to provide the grid service or even form its local grid during the grid outage.

According to the three requirements discussed above, a DAB converter is an excellent candidate for the DC-DC converter inside the EV battery charger [11-13]. The topology is shown in Figure 1.5. At the same time, the DAB converter is easy to control by adjusting the phase shift between primary-side and secondary-side H-bridges. Also, because of the symmetric structure, the performances in G2V mode and V2G mode are the same.

Owing to the simple structure and integrated leakage inductor, a DAB converter has the advantage in power density, which is an appealing characteristic in onboard chargers. Figure 1.6 shows three examples of EV onboard chargers. The DAB converter is adopted

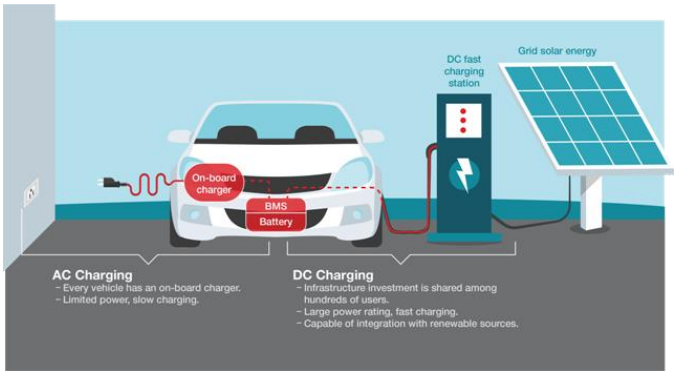


Figure 1.3. The differences between AC/DC charging stations and onboard chargers [14].

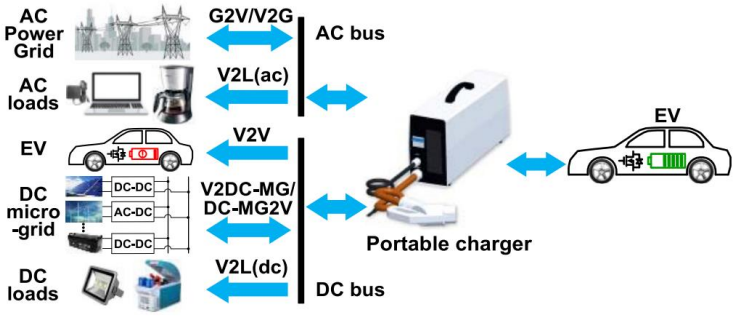


Figure 1.4. Comprehensive functions of EV battery chargers [15].

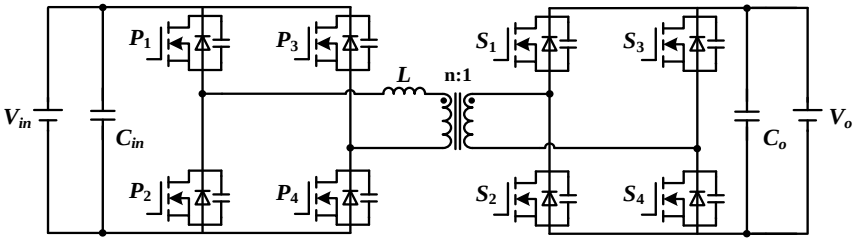


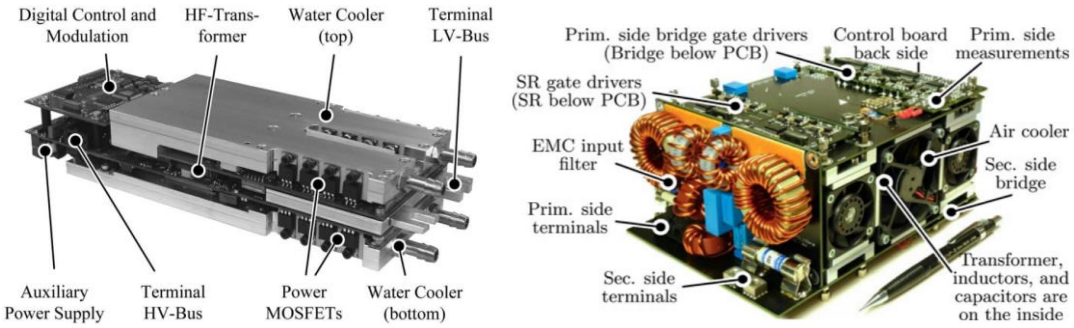
Figure 1.5. Topology of the DAB converter.

in all of them. The quite compact design could be found in Figure 1.6 (a) and (b) with water cooler and air-forced cooling, respectively. Considering the 20kW power rating, the prototype shown in Figure 1.6 (c) also has a simple structure with limited dimensions.

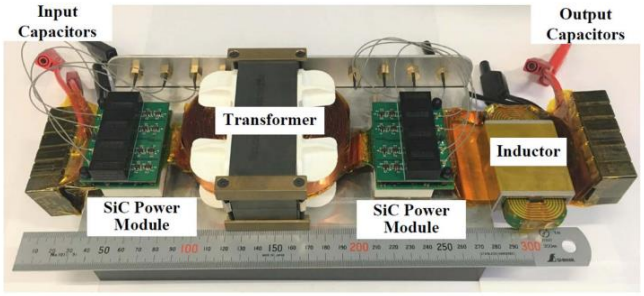
Other DC-DC converters such as LLC have similar functions as DAB. But because of the asymmetric structure of LLC, the performance in reverse conduction mode is not as good as in the forward conduction mode [15]. Also with the increase in voltage rating and current rating, the resonant tank of an LLC converter can occupy a pretty large space [16, 17]. Even though a CLLC converter has a symmetric structure and the same performance in bidirectional power flow [18], the resonant tank on both sides of the transformer makes CLLC disadvantageous in the consideration of power density.

For DAB, there are still some challenges. With the wide operation voltage in the battery charger, the performance cannot be guaranteed [19]. The ratio of the input voltage and the output voltage cannot be always equal to the transformer turn ratio. For the traditional DAB control strategy, when the input voltage and the output voltage are not matched, the switches can suffer the hard-switching on, and high switching-off current at light load or medium load, which will worsen the efficiency and induce the stability issues.

On the other hand, EV applications accelerate the spread of power electronics equipment. The new generation power devices like 10kV or 15kV SiC MOSFET brings a significant opportunity for power electronics to further grow in medium-voltage grid application. While a 60Hz step-down transformer is a connection between the medium-voltage distribution grid and local low-voltage AC grid, the appearance of a solid-state transformer



(a) (b)



(c)

Figure 1.6. EV on-board battery charger: (a) 2kW automotive DAB converter [11]; (b) 3.7 kW, single-phase, single-stage, bidirectional and isolated DAB ac–dc converter prototype [20]: (c) 20 kW DAB converter [21].

shows the advantage of less loss, weight, and volume in grid applications. Furthermore, an SST can directly create the local DC grid. The local AC grid can be provided by another stage of the inverter using the local DC grid. The concept of the new microgrid is shown in Figure 1.7. The proposed new microgrid can also integrate the energy storage system used as an uninterruptable power system (UPS), PV system, and EV chargers. Usually, AC-DC and DC-DC converters exist in the connection between renewable energy sources and the local grid. Without the AC grid, a DC-DC converter can directly deliver the power between two DC grids. The DAB converter can also be found in energy storage systems (ESS) [22-24] and PV applications [25].

1.2 SiC MOSFET Implementations in Renewable Energy Applications

To increase the efficiency and the power density of the power electronics equipment, a higher switching frequency is selected to shrink the sizes of passive components, such as an inductor, transformer, and capacitor. If such semiconductor devices exhibit lower conduction loss and switching loss, we can further reduce the size of the cooling system.

1.2.1 Benefits of SiC MOSFET Implementations

Owing to the higher energy gap and electric field, silicon carbide (SiC) devices can have higher breakdown voltage compared with Si devices. At the same time, with the same breakdown voltage, SiC devices have lower on-state resistance because of the shorter doped drift region. Taking advantage of higher thermal conductivity and melting point, SiC devices can work at higher junction temperatures. With higher electron velocity, SiC

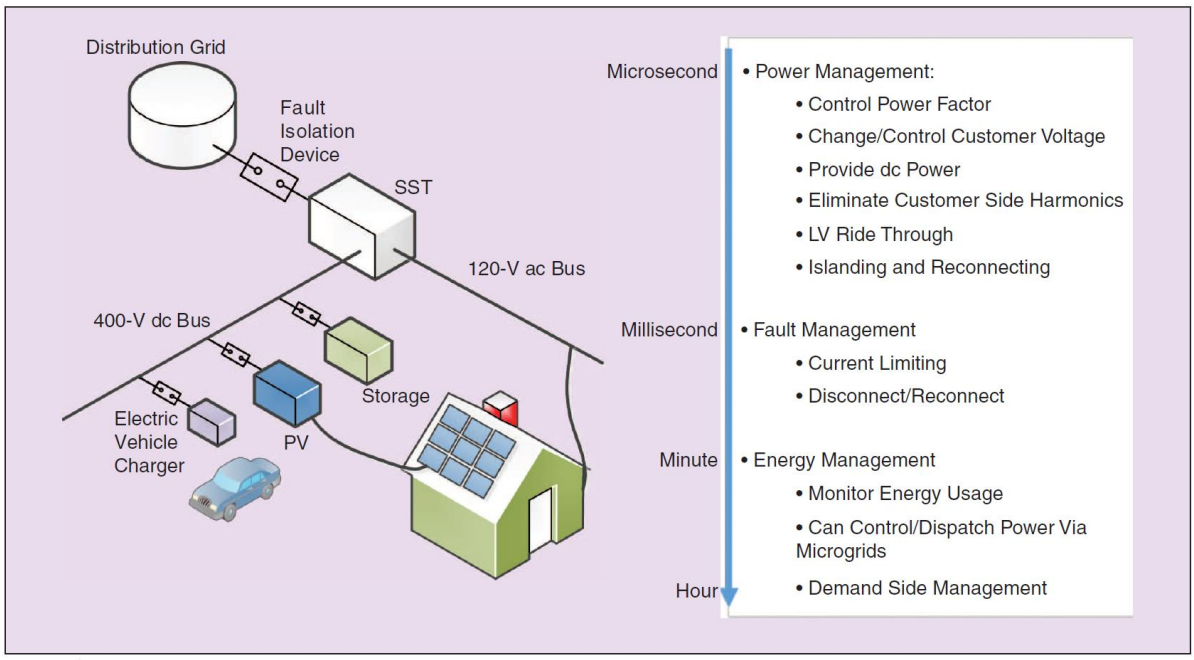


Figure 1.7. An SST-enabled hybrid dc/ac microgrid system [26].

devices typically have a higher switching speed. More detailed characteristics of SiC material are discussed in [27]. Looking at Si MOSFET and SiC MOSFET in Figure 1.8, the voltage rating of the traditional Si MOSFET is less than 1.2kV, but the voltage rating of SiC MOSFET starts with 600V. So the comparison of the traditional Si device and SiC device is between the Si IGBT and the SiC MOSFET. Also, SiC MOSFET can significantly reduce the switching-off loss and reverse recovery loss. Presently, SiC MOSFET can be a good replacement for Si MOSET when the application voltage is higher than 600V.

Table 1.1 provides the comparison of power loss and heatsink dimensions between Si IGBT and SiC MOSFET in an active rectifier for a 22kW EV battery charger. By applying SiC MOSFET, the total power loss is much lower than Si-IGBT-based design at 20kHz switching frequency. The switching loss and the diode reverse recovery loss are significantly reduced owing to the characteristics of SiC MOSFET. Even for 60kHz, the design based on SiC MOSFET still has obvious advantages of loss and heatsink size compared with the Si-IGBT design@20kHz.

For a SiC-based on-board EV battery charger, the mass and the volume are mainly composed of the heatsink, filter capacitors, and magnetics in Figure 1.9. By increasing the switching frequency, the size of the passive components including capacitors and inductors can be reduced under the same requirements of output ripple [28]. In a summary, the implementation of SiC MOSFET can reduce switch loss and increase the power density of power electronics equipment.

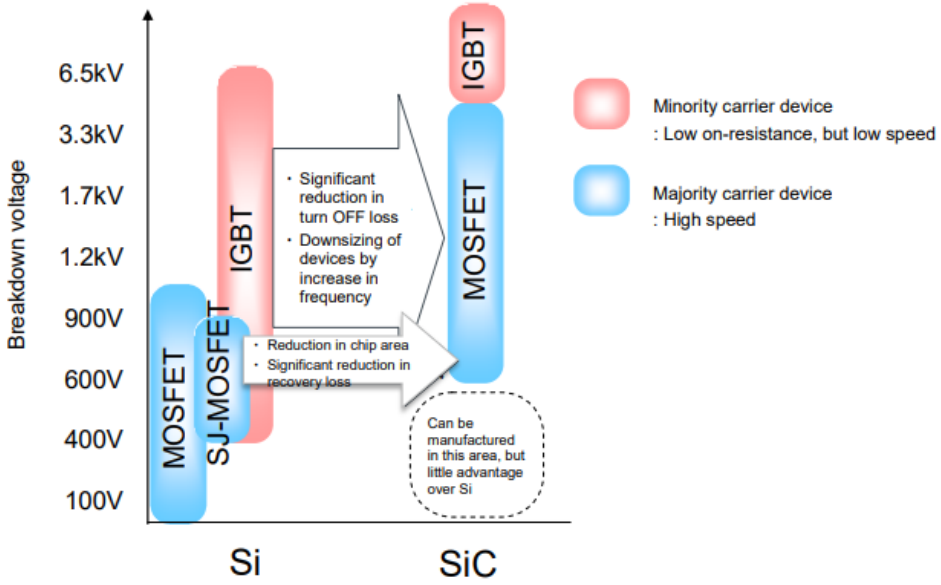
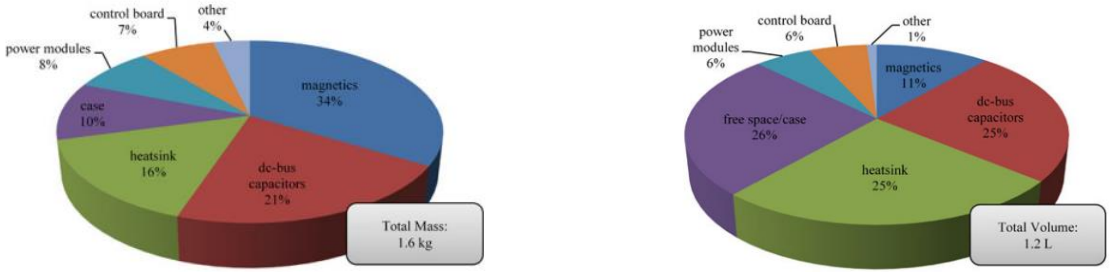


Figure 1.8. Rated voltage range for Si and SiC (MOSFET and IGBT) [29].

Table 1.1. Comparison of power losses and heatsink size between Si-IGBT and SiC MOSFET in 22kW EV Charger [30].

	Si-IGBT	SiC-MOSFET	
Switching frequency	20kHz	20kHz	60kHz
Total power Loss	1115W	286W	481W
Heatsink Dimension	2260cm^3	177cm^3	463cm^3



(a) (b)

Figure 1.9. Breakdown of SiC-based on-board vehicle battery charger for: (a) mass considerations and (b) volume considerations [31].

The voltage rating for automotive applications is higher than 600V. However, for renewable energy and microgrid, the voltage rating for the power electronic devices can be even higher, as shown in Figure 1.10. Therefore 1200V SiC MOSFETs can also find use in the renewable energy market.

In recent years, the power SiC device market is increasing. The biggest demand belongs to automotive applications as shown in Figure 1.11. The energy and the industrial application also contribute to the growth of the SiC device market. Per forecast, the capacity of the market will continue increasing within the next following years. By 2025, the SiC market will be over $2500 million, and the automotive will have more than $1500 million. Therefore SiC-based power electronic converters in automotive applications are expected to play more important roles in the near future.

1.2.2 Challenges of SiC MOSFET Implementations

Owing to higher electron velocity, SiC MOSFET yields high di/dt and high dv/dt during the hard switching transients [32, 33]. Figure 1.12 shows the comparison of the switching speed between SiC-MOSFET, Si-MOSFET, and Si-IGBT. They all have a similar current rating. But the voltage rating of the Si MOSFET is lower than SiC MOSFET and Si IGBT. Compared with Si-IGBT, SiC MOSFET has a much higher switching speed resulting in higher di/dt and higher dv/dt, which can induce reliability issues such as overvoltage, crosstalk [34], and electromagnetic interference (EMI). With the increase of the switching frequency, the common-mode noise needs to be paid more attention.

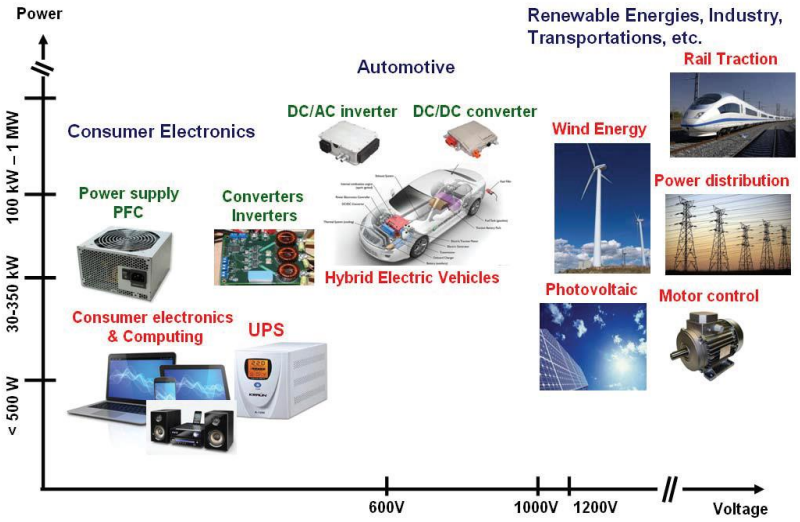


Figure 1.10. Main application areas of SiC and GaN power devices [35].

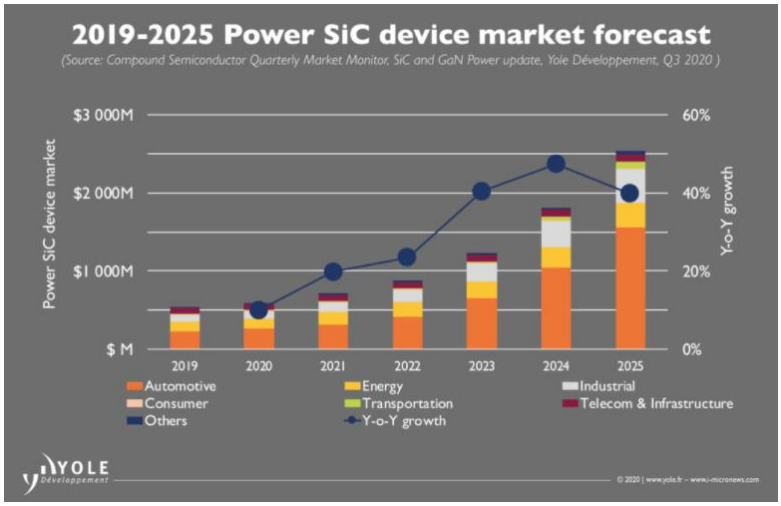
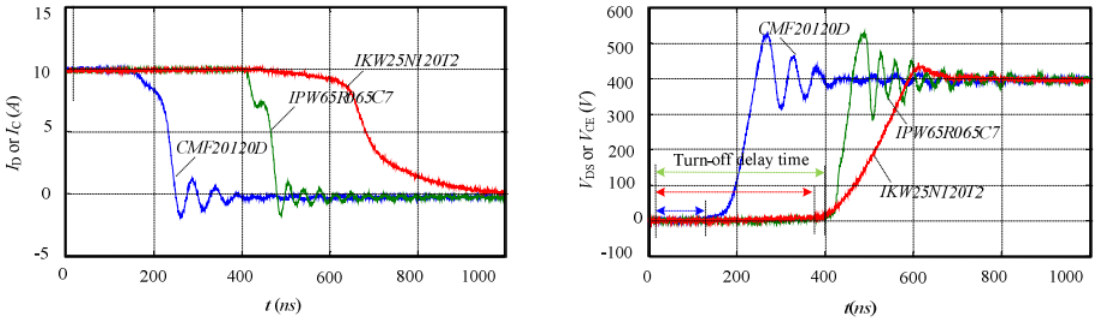


Figure 1.11. 2019-2025 Power SiC device market forecast [36].



(a) (b)

Figure 1.12. Switching waveforms of CMF20120D (SiC-MOSFET), IPW65R065C7 (Si-MOSFET) and IKW25N120T2 (Si-IGBT) [37].

Crosstalk happens in the half-bridge when the switching action happens [38, 39] caused by high dv/dt of the middle point of the bridge leg, parasitic capacitor of the switches, and the gate-loop impedance, which mainly happens during the hard-switching transient. For example, in Figure 1.13 (a) when the top switch turns on, V_{ds} of the bottom switch then increases, which charges C_{gd} of the bottom switch. The charging current flows into the gate drive circuit and induces the positive voltage between gate and source caused by the gate resistor. If such positive voltage is higher than the threshold voltage of the switch, the bottom switch will be mis-triggered when the top switch is still on. Eventually, the shoot-through happens at the half bridge in Figure 1.13 (c).

Also, when the top switch turns off, C_{gd} the bottom switch is discharged, as shown in Figure 1.13 (b). Such discharging current flows out of the gate drive circuit, creating a negative voltage spike between gate and source at the bottom switch, as shown in Figure 1.13 (c). In a real application, SiC MOSFETs are using negative voltage during off-state to avoid miss-triggering. Therefore, the oxide between gate and source keeps enough breakdown voltage. However, if the negative voltage spike is lower than the required minimum gate-source voltage and continuously applied between gate and source, it can accelerate the aging of the gate-source oxide, which eventually breaks down the gate.

Another reliability issue caused by high di/dt and high dv/dt during hard-switching transient is high overvoltage [40, 41]. The overvoltage is induced by the resonance between the parasitic inductance in the switching loop and capacitance. Typically, the parasitic

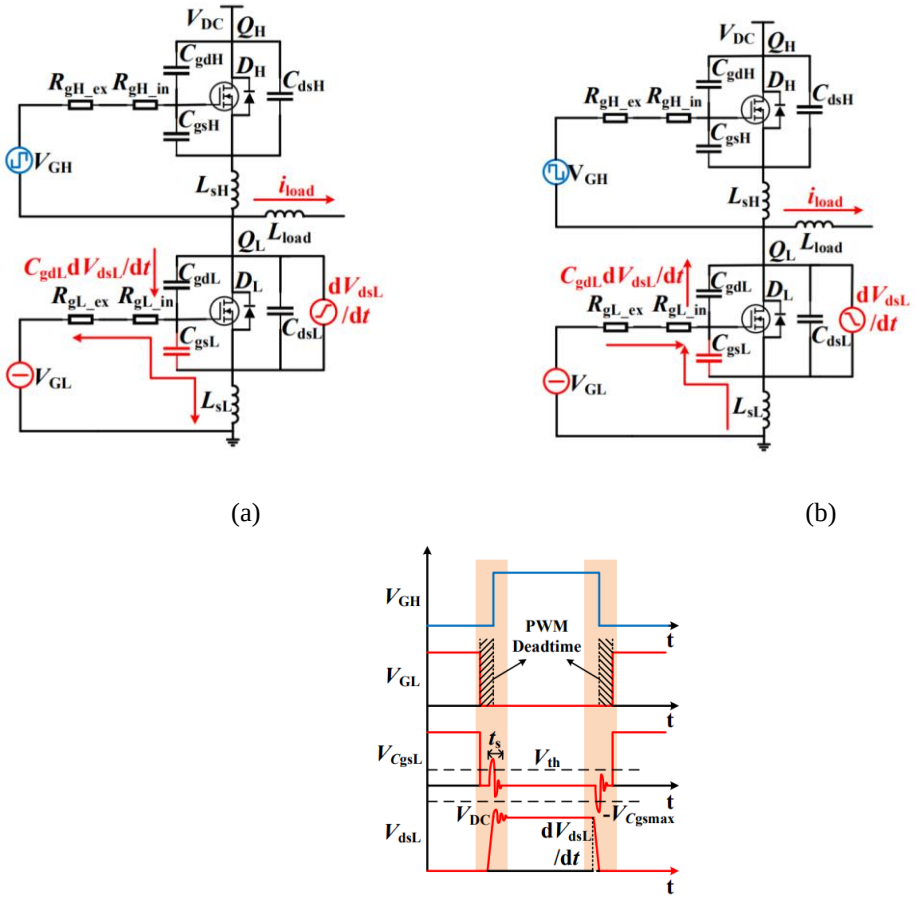


Figure 1.13. Mechanism of bridge-leg crosstalk during switching transients of QH: (a) Turn-on transient; (b) Turn-off transient; (c) switching waveforms [42].

inductance exists in PCB traces, switch lead, bus bar, and even decoupling capacitors. Higher di/dt and higher dv/dt can cause higher overvoltage.

With a higher switching speed of the SiC MOSFET, the EMI content appears from 1MHz to 30MHz in the spectrum [43], as shown in Figure 1.14. With the higher switching frequency, more components appear from 150 kHz. The EMI consists of the different-mode noise and the common-mode noise. The differential mode noise appears as the current ripple, which is related to the main power components in the circuit and easily observed. The common-mode (CM) noise is generated high-frequency voltage pulse through the parasitic capacitance in the circuit, which is seldom addressed in DAB converter. The parasitic capacitances are charged or discharged by the switching node, which further induces higher CM current flowing into the ground.

The CM sources in automotive applications include motor drive systems, electric motors, shielded and unshielded cables, and battery chargers [44] as shown in Figure 1.15. So the CM performance of EV battery chargers should be also taken into consideration. For example, CISPR 25[45] or CISPER 22 [46] provide the guideline of EMC specifications for automotive applications. For the DAB converter in battery chargers, the output is directly connected to a high-voltage battery. For an off-board charger, the CM current generated by the DAB converter flowing into the vehicle can accelerate the degradation of the insulation between chassis and high voltage batteries or influence the other electronic equipment for example multimedia equipment and radars.

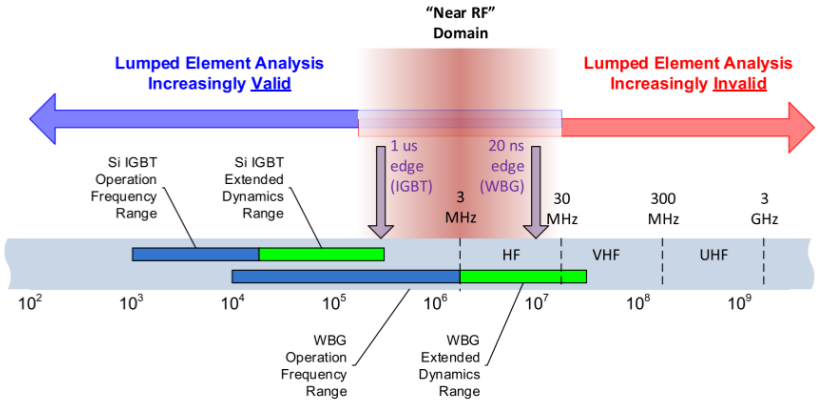


Figure 1.14. Illustration of the impact of high-signal edge rates on WBG converter spectral content [43].

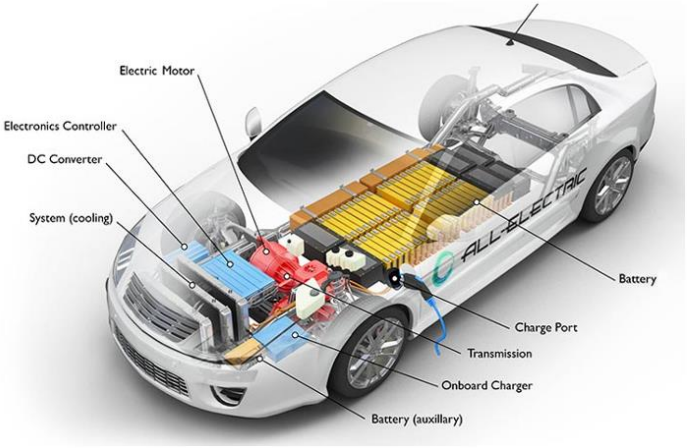


Figure 1.15. Sources of EMI in EVs [44].

1.3 Research Objectives and Thesis Layout

As the importance of the DAB converter and SiC MOSFET discussed above, this thesis focuses on the implementation of a SiC-based DAB converter. To achieve better performance of DAB with the wide-voltage-range operation, the control algorithms are important to regulate the power and realize zero-voltage switching. The different modulation strategies of the DAB converter focus on different operation points by applying the inner phase shift at the primary-side or secondary-side H-bridge to realize ZVS, eliminating reactive power or reducing the switching loss. With the application of SiC MOSFETs, most reliability issues happen during the hard-switching-on transients. So for the DAB converter, ZVS is important. Starting with the problems in EV charging applications, this thesis addresses the solutions to common issues in DAB converters associated with different modulation strategies. The detailed research objectives are shown below.

(2) The essence of ZVS realization is the resonance process between switch C_{oss} and the inductor in the DAB converter. The ZVS analysis is carried out considering MPS control. The minimum required inductor energy to finish the ZVS transition is provided based on different conditions. Also, the ZVS transition time is derived to set the reference for dead time selection.

(3) Common-mode performance is a missing part of previous DAB research. With the implementation of SiC MOSFET, a higher switching frequency is used to get the compact design of the power electronics equipment. Since the heatsink of SiC MOSFET usually is

grounded, it then provides additional common-mode loops. A general common-mode analytical model is then proposed to compare the different common-mode behaviors in MPS control.

(4) Multiple-phase-shift control (MPS) contains different modulation strategies. A simplified method of integrating different modulation strategies is proposed. The boundary conditions are defined to realize a smooth transition between modulation strategies. Securing ZVS is the prerequisite when selecting modulation strategies to eliminate the potential crosstalk during the hard-switching-on process of SiC MOSFET.

(5) Dynamic response is important in the grid-connection DAB converter. During the load current transient, there is a current spike appearing in the transformer and the DC offset in the next following cycles caused by the fast-changing phase shift. The current spike elimination method is necessary, especially in MPS modulation.

The layout of this thesis is listed below.

Chapter 2 is the literature review for the principle of ZVS realization, the existing modulation strategies for the DAB converter, and the common-mode knowledge in the isolated DC-DC converter.

Chapter 3 proposes a smooth transient process for MPS control and the boundary condition definition with full-load-range and wide-voltage-range ZVS realization.

Chapter 4 is the ZVS transition analysis in the DAB converter considering different switching actions in MPS control.

Chapter 5 discusses the common-mode parasitic capacitance and the general common-mode voltage (CMV) model for the DAB. Based on the CMV model, the influence of MPS control on common-mode behaviors and common-mode choke design is also proposed.

Chapter 6 proposes a new design theory of the modulation strategies considering the current spike elimination during load transient and the ZVS realization in the steady state.

Chapter 7 is the conclusion of the proposed work and the work in the future.

Chapter 2 LITERATURE REVIEW

This chapter provides the literature review for the proposed work. To eliminate crosstalk without complicating the hardware gate-drive design, ZVS is necessary for all switches in the DAB converter. Firstly, the existing discussion about ZVS theory is reported. Then how to realize ZVS in the DAB by utilizing different modulation strategies is discussed aiming at different operation conditions. Finally, the common-mode concern in the DAB converter is addressed.

2.1 Zero-Voltage-Switching Realization

To prevent the potential aging problem or breakdown at the gate-source terminal caused by a negative voltage spike during the crosstalk, there should be enough margin left for the normal off-state gate-source voltage. To prevent the mis-triggering of the switch caused by the positive voltage during the crosstalk, complicated gate drivers have been developed in [47-49]. The basic reasons for the positive voltage spike are the high dv/dt during the hard switching-on and C_{gd} of the switches. Hence one potential solution without renovating the gate driver is the realization of ZVS. Because the essence of the ZVS is the resonance between the inductor and the switch C_{oss}, dv/dt during ZVS transition should be much smaller than that during hard switching-on.

To achieve ZVS for active switches, in previous literature there are two main methods. The first one is the current-based identification [50-52], and the second one is the energy-based identification [53-56]. For current-based ZVS theory, the condition used to judge if the ZVS transition can be finished is the polarity of the inductor current. For example, in

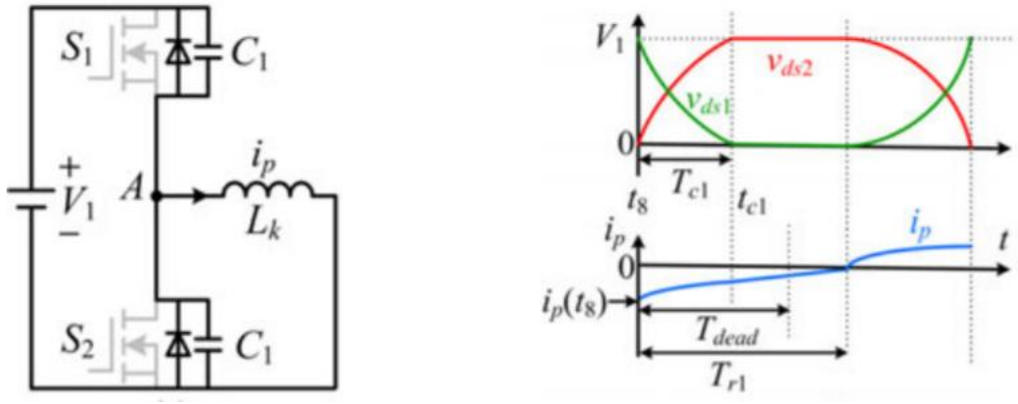
Figure 2.1 (a) to realize ZVS for S_2, it only needs to make sure the current flowing through the leakage inductance is positive, which means the inductor current can be used to discharge the C_{oss} of S_2. The same theory can be also applied to other switches. For energy-based theory in ZVS realization, not only does the inductor current needs the right polarity but also the value of the inductor current needs to be large enough to finish the discharging process of switch C_{oss}. In Figure 2.1, to finish the ZVS transition, the energy stored in the inductor needs to be larger than the sum of the discharging energy in the C_{oss} of S_2 and the charging energy in the C_{oss} of S_1. The minimum required inductor current can be expressed as

$$i_{Lk} \geq V_1 \sqrt{2C_{oss} / L_k} \,. \tag{2-1}$$

The transient of ZVS is shown in Figure 2.1 (b). With the charging and the discharging of the switches' C_{oss}, the energy stored in the inductor is then drained out.

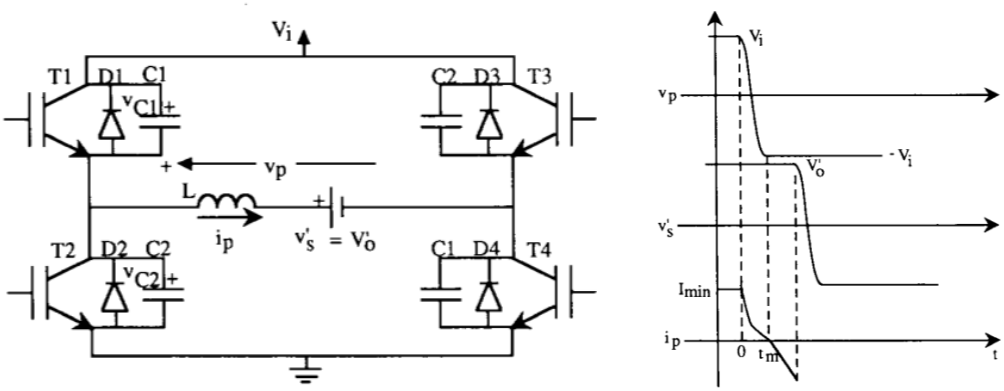
How to realize ZVS in the dual-active-bridge (DAB) application has been discussed in early literature [57]. Including single-phase-shift (SPS), dual-phase-shift (DPS), triple-phase-shift (TPS), and multi-phase-shift (MPS), various modulation strategies have been proposed to achieve ZVS in full-load and wide-voltage ranges [58, 59]. Note achieving ZVS relies on the resonance [60, 61] between transformer leakage inductance L_s and switch output capacitance C_{oss}.

Figure 2.2 shows the ZVS realization for the output H-bridge. Including reflected input voltage, output voltage, and 4 switches' C_{oss}, all of them participate in the resonance process during ZVS transition in single-phase shift modulation. Such resonant loop,



(a) (b)

Figure 2.1. Energy-based ZVS realization in a half bridge: (a) half bridge circuit; (b) voltage across the switches and the inductor current during ZVS transient [56].



(a) (b)

Figure 2.2. DAB converter with the output bridge replaced by an equivalent voltage source during turnoff of devices T1, T4 of input bridge; (b) minimum inductor current required at the instant of turnoff of T1, T4 to resonate the pole voltage from $+V_i$ to $-V_i$ [57].

however, can be different under other different modulation strategies, which have been ignored in the previous analysis. Some literature [62, 63] proposed the equivalent capacitance based on the half-bridge model, where the charge-based, energy-based, or other types of equivalent capacitance are employed for different purposes. In Figure 2.3, an example of ZVS realization based on the half-bridge model is explained in detail. The main transient process of charging and discharging C_{oss} is shown in Figure 2.3 (b). The energy stored in the inductor is dissipated in the input voltage source. So there is the minimum initial inductor energy required to finish the ZVS transition. However, the proposed derivation can only be applied to the topology with a half-bridge structure. For the DAB converter, the basic building block to analyze ZVS realization should be H-bridge [57, 62]. At the same time, considering the inner phase shift in DPS and TPS modulation, the resonance loop between the inductance and switch C_{oss} can be more complicated.

To make sure the switch C_{oss} is fully discharged before the switch is turned on, the dead time should be long enough. In [62], the resonance time interval is derived according to the nonlinearity of C_{oss} in the SPS modulation. Figure 2.4 shows the relationship between V_{ds} across the discharged C_{oss} and time in the proposed simulation. But the proper derivation of ZVS transition time with the consideration of different modulation strategies has not been also addressed yet. In [64], parasitic parameters of the transformer are further considered, when it is comparable with switch C_{oss}.

To achieve ZVS in real converters, two essential parameters should be carefully selected: the initial inductor energy and the dead time. Increasing the initial inductor current helps

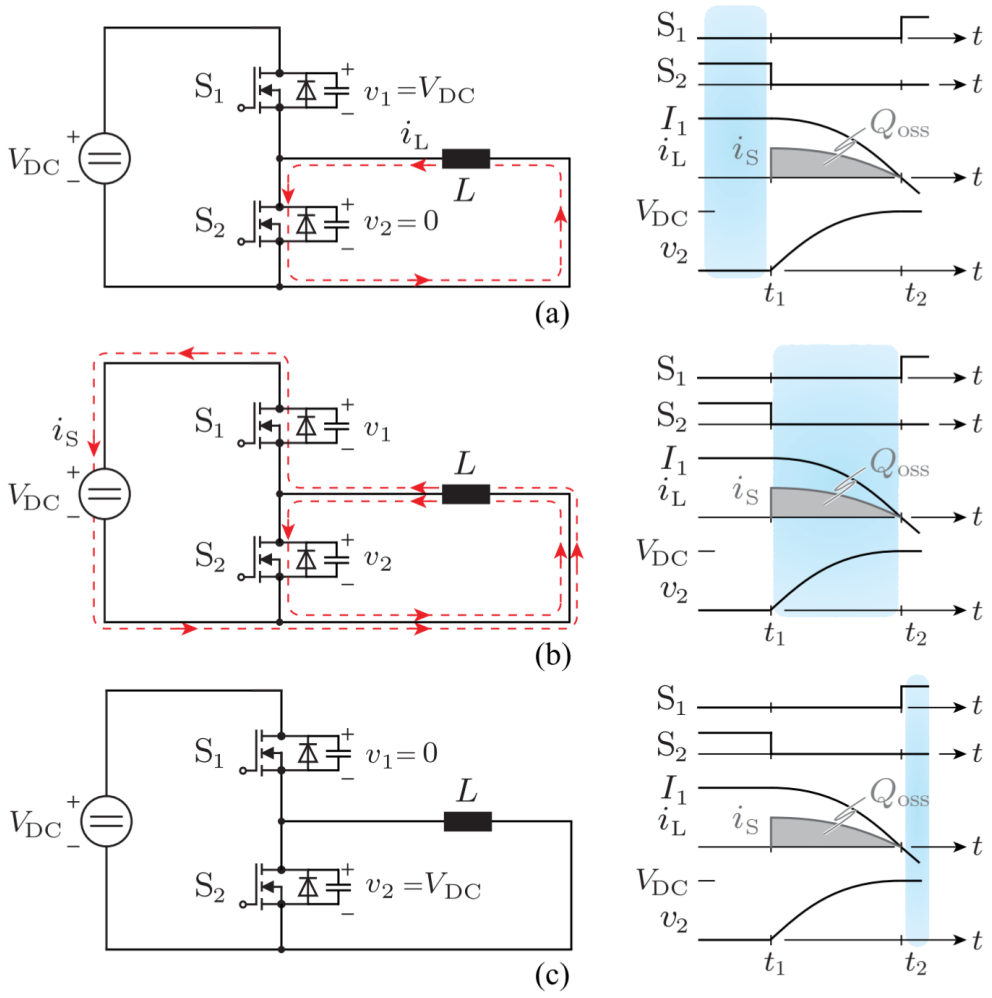


Figure 2.3. Soft-switching transition of a MOSFET bridge leg and an inductor L: (a) free-wheeling interval with inductor current $i_L = I_1$; (b) switch S_2 turns off and resonant transition starts with an additional current path through the dc source (For simplicity reasons, the parasitic output capacitances are assumed to be linear.); (c) end of transition when the drain-source voltage of S_2 has reached the source voltage [63].

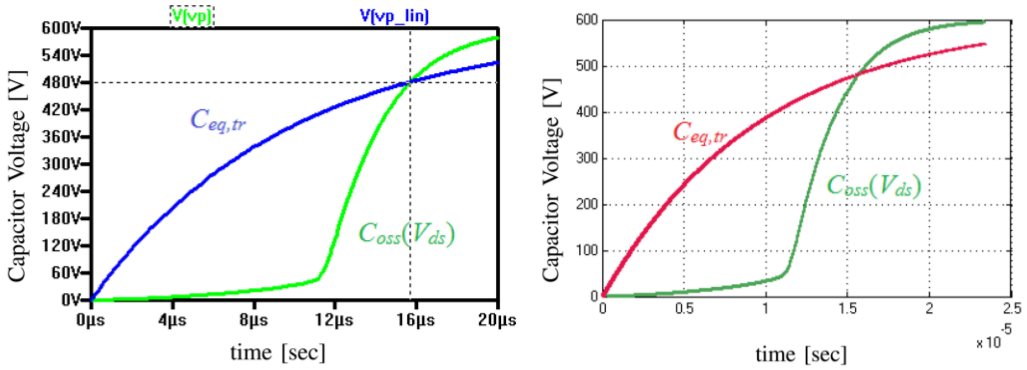


Figure 2.4. Simulation results in (a) Ltspice and (b) Simulink showing the comparison between the voltage waveform of an IPB60R385CP as it is charged by a series 600-V source and 100-kΩ resistor [62].

ZVS realization [65]. Similarly, a longer dead time guarantees the completion of ZVS but increases loss because of the increased reverse conduction time. To achieve optimal performance, it is important to calculate the required initial energy and ZVS transition time accurately in all circumstances, which is lacking in the present study.

2.2 Definition of Modulation Strategies in DAB Converter

In the DAB converter, there are 8 active switches. For most of the modulation strategies, each switch operates with a 50% duty cycle and the PWM signals of the switches located in the same phase leg are complementary [66]. Figure 2.5 shows the basic operation waveform of the DAB modulation strategy. The diagonal switches in H-bridge turn on and off simultaneously. So the output of the H-bridge is a square waveform. The power flow is regulated by the phase shift between the primary-side H-bridge and the secondary-side H-bridge.

With the first phase leg as the reference, the relationship between the first phase leg and the other three-phase legs can be regarded as three degrees of freedom, which offers high flexibility for the DAB control. Different modulation strategies then are defined according to the voltage waveform at both sides of the transformer. The simplified model is shown in Figure 2.6. When primary side and secondary side voltage are both square AC waves with a 50% duty cycle, the modulation strategy is a single-phase shift (SPS). If either the primary or the secondary side voltage is a three-level wave [67, 68], the modulation strategy is dual-phase shift (DPS). If they are both three-level waves [23, 66], the

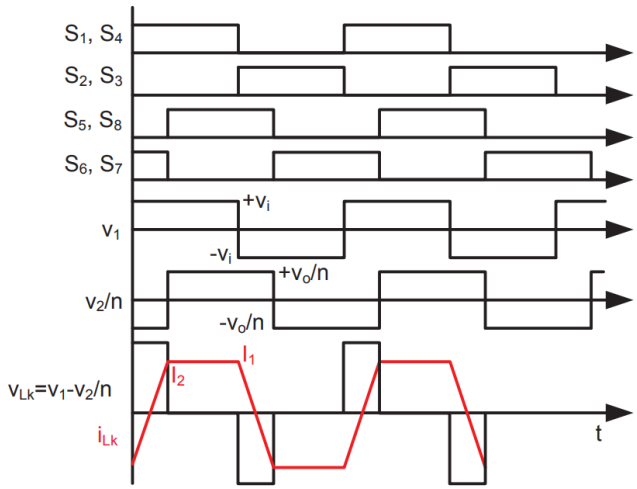


Figure 2.5. Main operation waveforms of the phase-shift control method [69].

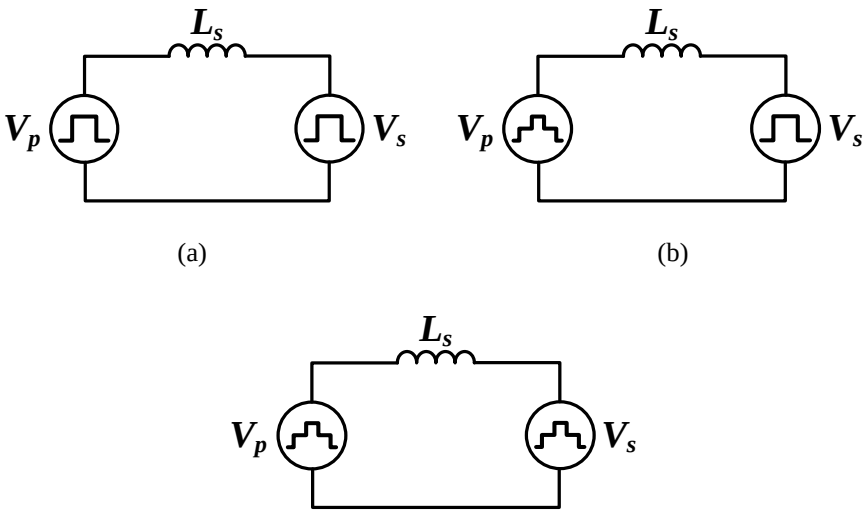


Figure 2.6. Transformer Voltage: (1) SPS [69]; (2) DPS [70]; (3) TPS [71].

modulation strategy is named triple phase shift (TPS) (If the primary side phase shift and the secondary side phase are always the same, the modulation strategy is still DPS [72].).

To optimize the performance of a DAB converter, selecting the proper modulation strategy under different operation circumstances is necessary. To evaluate such strategies, there are several major factors to be considered, such as efficiency [73, 74], dynamic response [75-77], and EMI characteristics [78, 79]. No mention that hard-switching-on can cause EMI concerns [80], which will in return deteriorate the system reliability and increase electric stress. For example, crosstalk in one phase leg counts on the advanced gate-drive circuit to suppress [81]. This is another reason why so many modulation strategies are developed under the premise of the realization of ZVS [12, 67, 82-84]. And the reduction of DC-bias current at the transformer is also an important topic [85, 86].

2.3 Modulation Strategies in Dual Active Bridge

2.3.1 Single Phase Shift (SPS) Modulation

The conventional SPS is the simplest way to manage the power delivery in DAB. The switching waveform is shown in Fig. 4. Typically, the definition of the phase shift between the primary side and the secondary side is

$$\phi = \frac{t_{P1} - t_{S1}}{T_s / 2} \tag{2-2}$$

Then the power flowing through the DAB converter is

$$P = \frac{nV_{in}V_o\phi(1-\phi)}{2L_sT_s}. \tag{2-3}$$

Based on the equation above, the relationship between the power and phase shift can be plotted in Figure 2.7. When the secondary-side switch S_5 is leading the primary-side switch S_1, the power flows from the secondary side to the primary side. When $|\phi|=0.5$, the converter reaches the maximum power. Here the voltage gain is defined as

$$M = \frac{nV_o}{V_{in}}. \tag{2-4}$$

A. Switching Current in SPS Modulation

The switching waveforms shown in Figure 2.8 are based on single-phase shift. In Figure 2.8 (c), when the voltage gain is equal to 1, the transformer currents at t_0 and t_1 are the same. At t_0, the switching action happens at the primary side, and the polarity of the transformer current should be negative to realize ZVS for primary-side switches. At t_1, the switching action happens at the secondary side, and the polarity of the transformer current should be positive to realize ZVS for secondary side switches. However, when the voltage gain is smaller than 1, as shown in Figure 2.8 (a) with the power decreasing, the transformer current at t_0 and t_1 are both decreasing. Finally, the polarity of the current at t_1 becomes negative, which means the switches at the secondary side are suffering hard-switching-on in Figure 2.8 (b). When the voltage gain is larger than 1, with the decreasing of the power, the polarity of the transformer current at t_0 becomes positive, which means the primary-side switches lose ZVS.

B. ZVS Realization

ZVS realization is the most common topic in the research of DAB. It can help to improve efficiency, and at the same time enhance the system's reliability. For most SiC MOSFETs,

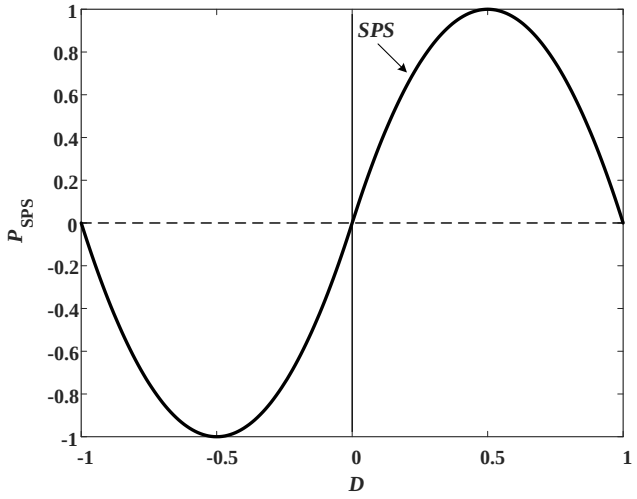


Figure 2.7. Power vs phase shift in DAB SPS [87].

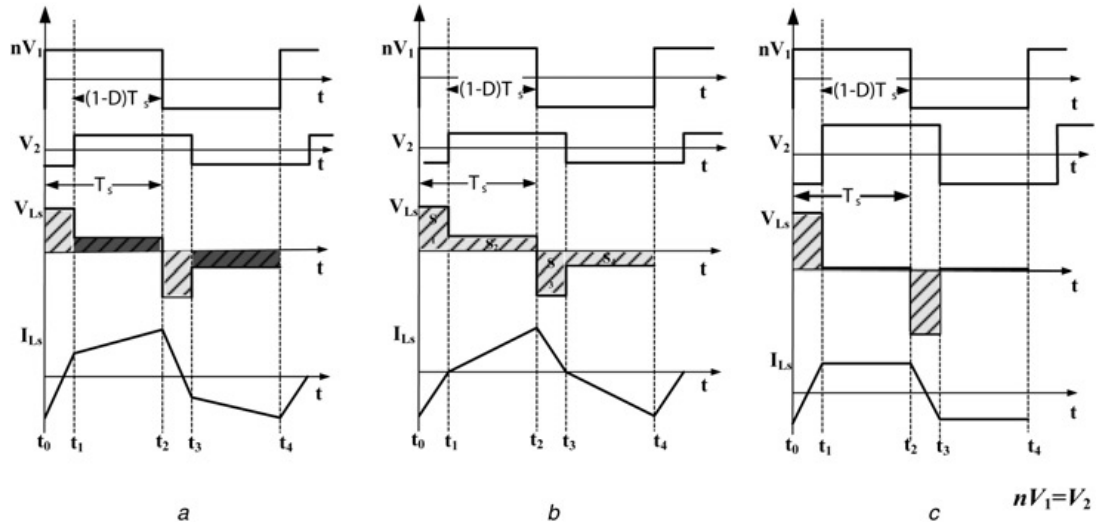


Figure 2.8. Typical voltage and current waveforms for Vin>nVo and Vin=nVo: (a) Common mode; (b) Boundary mode; (c) Extreme mode, Vin=nVo [19].

the switching-on energy is much higher than the switching-off energy, as shown in Figure 2.9. ZVS realization can then help to save the switching loss. Many literatures also plot the ZVS range through the full-load-range and wide-voltage range [58, 88, 89]. Figure 2.10 shows the ZVS range when using SPS. Under the same phase shift, the closer to the unit voltage gain, the easier it is to achieve ZVS. When voltage gain is equal to 1, it can always realize ZVS. When voltage gain is fixed (not equal to 1), the smaller the phase shift, i.e., the smaller power, the harder it is to realize ZVS.

The ZVS range plotted in Figure 2.10 is with the current-based model. For the more accurate method, for example, energy-based analysis [90], the actual ZVS range will shrink. The realization of ZVS is quite important because it can eliminate the switching-on loss and diode reverse recovery loss, and enhance the system stability.

For SPS control, only one control freedom is used to regulate power, which is the basic and simplest modulation in DAB. The performance of SPS is only based on voltage gain and the actual load. When voltage gain is nearly 1, it is an excellent modulation strategy to achieve full-load-range ZVS and eliminate considerable reactive power and current stress [91]. However, with only one control freedom, no more room is available to secure ZVS. Especially when M is much smaller or greater than the unit value or the converter operates under light load, switches will lose ZVS [92-94]. Hence more modulation strategies are developed to further improve the DAB performance.

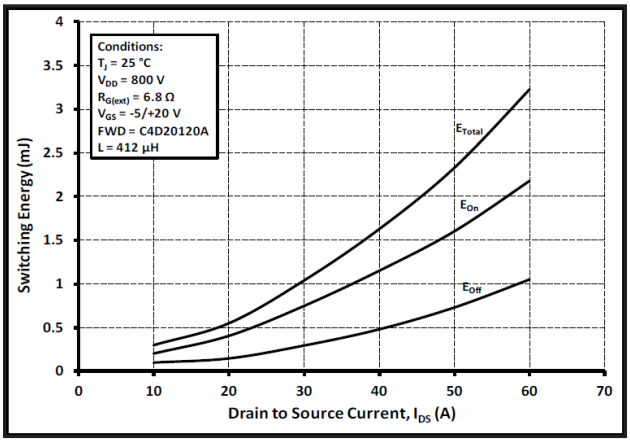


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800V)

Figure 2.9. Datasheet of CREE's SiC MOSFET - C2M0025120D [95].

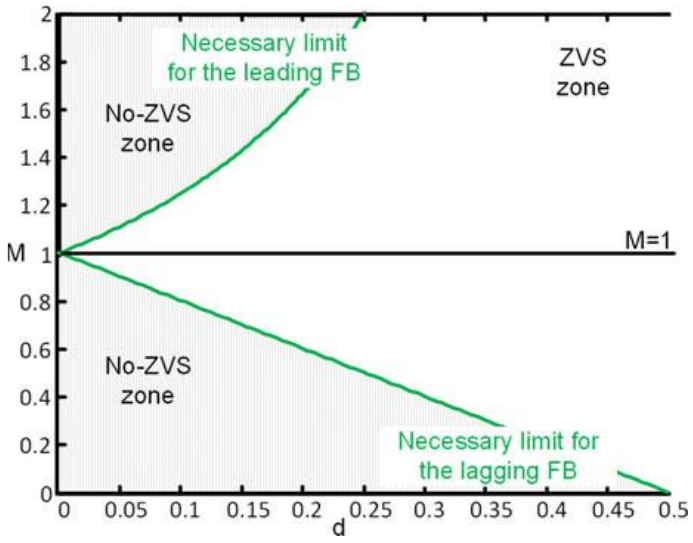


Figure 2.10. ZVS operation range [69].

2.3.2 Dual-Phase Shift (DPS) Modulation

A. Extend Phase Shift (EPS)

An inner phase shift is implemented at either primary-side or secondary-side H-bridge when voltage gain is smaller or larger than 1 in EPS modulation. There is an inner phase shift at the primary side. A zero stage appears at the transformer primary-side voltage, which alters the slope of the transformer current. The switching waveform of EPS modulation is shown in Figure 2.11. Because of the additional phase shift, the relationship between regulated power and phase shifts is different from SPS. Figure 2.12 shows the comparison between EPS and SPS control. With EPS, the output power range is widened, i.e., the ability to regulate power has been enhanced. Under a single power rating, EPS control has infinite combinations of D_1 (inner phase shift) and D_2 (phase shift between primary and secondary sides), regulating power more flexibly.

In the discussion of EPS modulation, different literature has different focuses. The EPS modulation shown above is developed to eliminate the reactive power [93, 96]. But other EPS modulations focus on the extension of the ZVS range [97, 98]. Figure 2.13 shows the switching waveforms of EPS modulation for ZVS realization. When the voltage gain is larger than 1, there is an inner phase shift introduced into the primary side of the H-bridge. So by adjusting the relationship between the inner phase shift and the phase shift between the primary side and the secondary side, all switches can realize ZVS. With the power decreasing, the traditional EPS modulation in Figure 2.13 (a) can also change to Figure 2.13 (b).

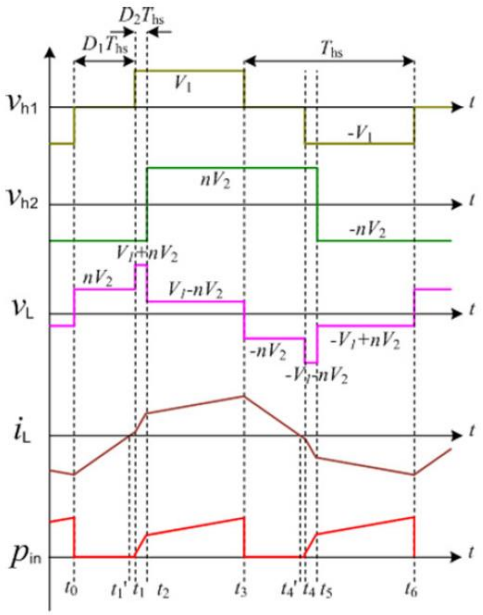


Figure 2.11. EPS control switching waveform [67].

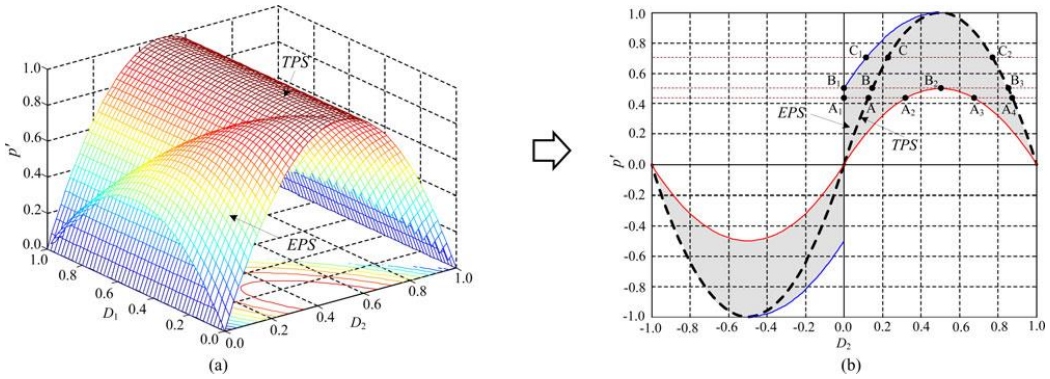
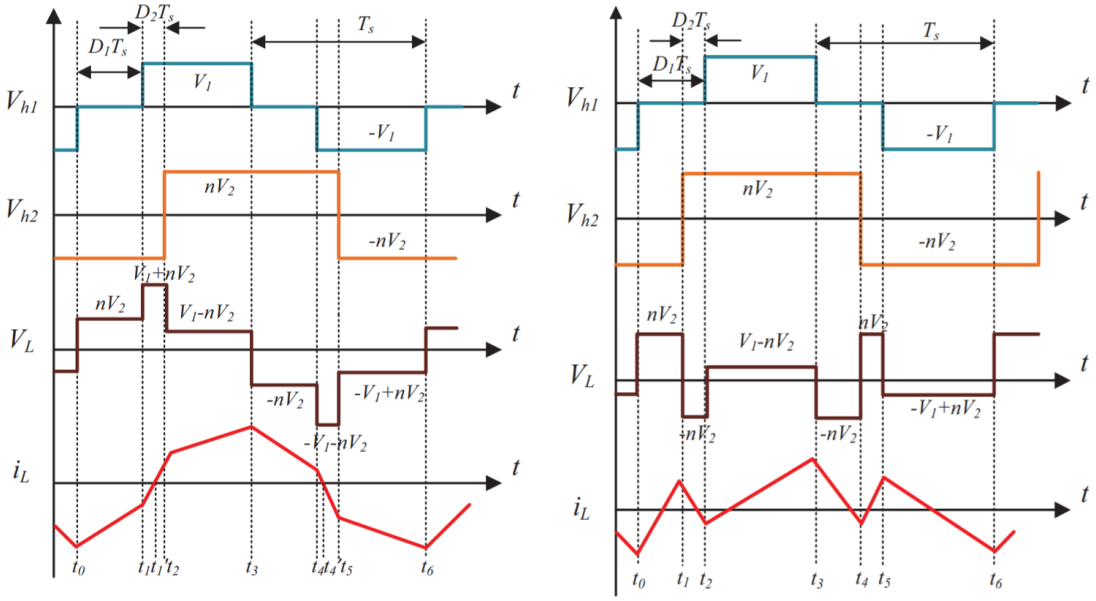


Figure 2.12. Characteristics of EPS modulation: (a)3-D curves of the unified backflow power varied with D_1 and D_2 ; (b) power versus D_2 [67].



(a) (b)

Figure 2.13. Typical waveforms for EPS: (a) Buck mode (V1.nV2) for S1 leading Q1, (b) Buck mode (V1>nV2) for S1 lagging Q1 [98].

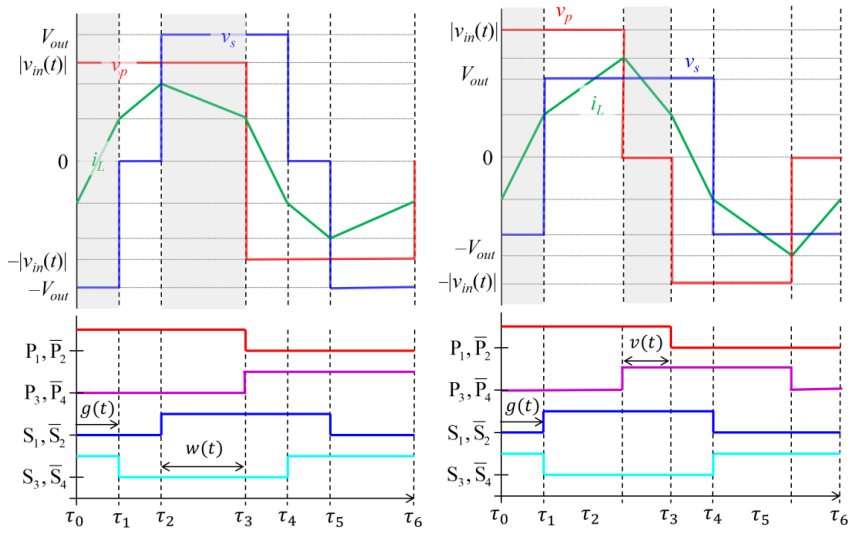
B. Primary-dual-phase-shift (PDPS) and Secondary-dual-phase-shift (SDPS)

PDPS and SDPS control are similar to EPS control. The switching waveforms are shown in Figure 2.14. PDSP control has an inner phase shift at the primary side when the voltage gain is smaller than 1. SDPS has an inner phase shift at the secondary side when the voltage gain is larger than 1. Their principle and function are different from EPS. Usually, PDPS and SDPS control are used to realize ZVS at the medium load range with the wide voltage range [13]. In [12, 13, 99], both modulation methods are applied in electric vehicle chargers, where the input voltage of the DAB converter contains a double-line-frequency ripple (form 0 to maximum value). Figure 2.15 shows the topology of a single-phase charging module. The switching frequency is also changing with the input voltage. The relationship between the primary-side/secondary-side inner phase shift and the primary-secondary phase shift is shown in (4) and (5), respectively. Both modulation strategies keep the transformer current at τ_1 and τ_3 the same, which is achieved by restricting the relationship between different phase shifts.

With the PDSP and SDPS control, the ZVS range shown in Figure 2.10 can be further widened, especially when the voltage gain is away from the unity value. A similar DPS modulation is also developed in [24] for an off-line UPS system.

$$v(t) = \frac{V_{in} - nV_o}{V_{in}}(0.5 - \phi) \tag{2-5}$$

$$w(t) = \frac{V_{in}}{2nV_o}(1 - 2\phi) \tag{2-6}$$



(a) (b)

Figure 2.14. Switching waveform: (a) SDPS modulation; (b) PDPS modulation [13].

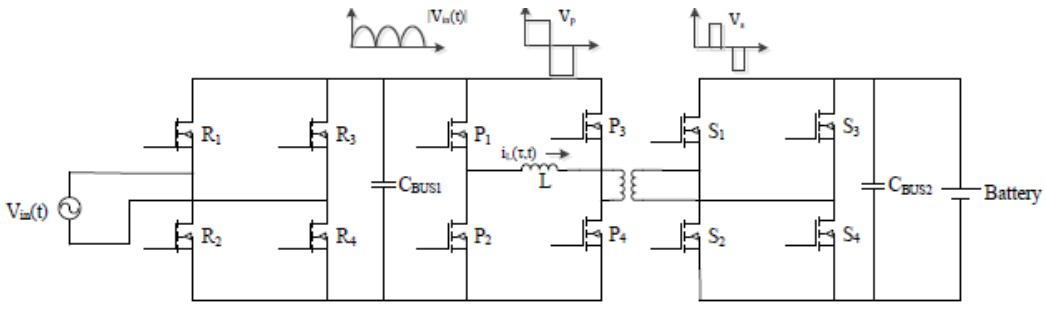


Figure 2.15. Single-phase charging module [13].

2.3.3 Triple Phase Shift (TPS) Modulation

For DPS, two control freedom degrees are used. With the development of modulation strategies, all three-phase shifts including outer phase shift, primary-side inner phase shift, and secondary-side inner phase shift are controlled separately to achieve better performance. Many modulation candidates with three-level voltage are listed in [88, 100, 101].

A. Overlap and Non-Overlap Triple-Phase-Shift

Triangular current modulation (TRM) and triperidol current modulation (TZM) control are more suitable for applications that require low reactive power [23, 66]. Their ZVS performance, however, is not adequate. Overlap and Non-overlap TPS modulations are proposed to achieve ZVS through a wide operation range. The switching waveforms are shown in Figure 2.16.

The realization of ZVS depends on the transformer current when the switching action happens. With three control freedom degrees, shaping the transformer current is quite flexible, making the ZVS condition decoupled from delivered power [99]. With non-overlap TPS control, ZVS can be realized even at an extra light load or the input voltage of nearly 0. Its main drawback is its poor power capability because of the low utilization of both sides voltage. It also generates considerable reactive power to fulfill the ZVS condition. For higher power transfer, overlap TPS is used to maintain ZVS for all switches and regulate the power at the same time. The applicable power range of the two modulation strategies is shown in Figure 2.17. Similar modulation strategies are also used in [13, 94].

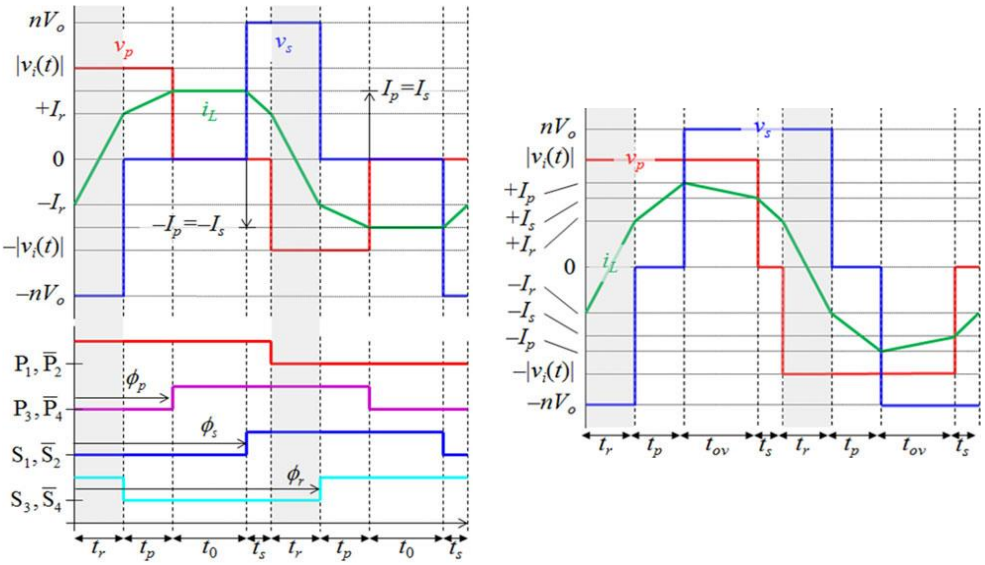


Figure 2.16. Switching waveform: (a) overlap TPS modulation; (b) non-overlap TPS [99].

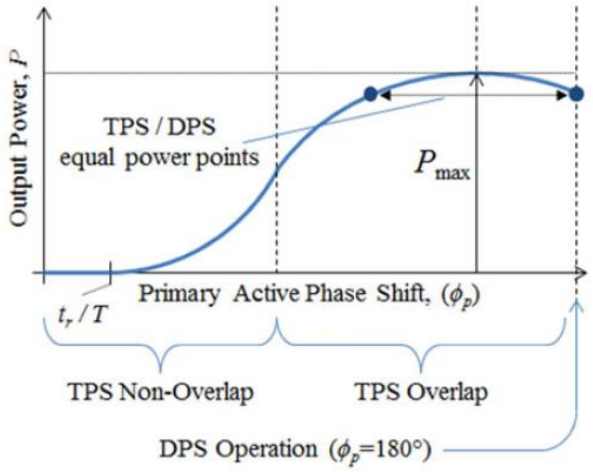


Figure 2.17. Output power versus primary active-phase-shift when $V_{in} < nV_o$ [99].

Both overlap and non-overlap TPS are developed to cover a wide voltage range, such as the application shown in Figure 2.15.

B. In-phase Triple-Phase-Shift

The polarity of the slope of the transformer current changes three times in one half switching period, as shown in Figure 2.18. With in-phase TPS, DAB can realize ZVS for all switches. Compared to the modulation shown in Figure 2.16, in-phase TPS has lower reactive power and current stress when the input voltage is not rectified sinusoidal waveform, making it a better alternative to DPS control under the light load [102].

2.3.4 Multiple Phase Shift (MPS) Modulation

With the utilization of all control freedom degrees, more MPS modulation strategies are proposed. In [88], the combination of SPS, DPS, and TRM modulation is developed, with the operation areas of different modulation strategies plotted in Figure 2.19. At heavy load and around the unity voltage gain, SPS is used to regulate power and ensure ZVS realization. When the voltage gain shifts away from 1 or at the light load, the modulation method switches to Optimal-Modulation (DPS), which can realize ZVS for all switches. At the light load, Triangular-Current-Modulation (TRM) is used to eliminate reactive power for the sake of efficiency.

Similar modulation strategies are also proposed in [23, 93, 101, 103, 104]. [105] utilizes SPS, EPS, TZM, and TRM together to regulate power through the whole operation range.

The combination of DPS (PDPS and SDPS) and TPS (overlap TPS and non-overlap TPS) modulation is also developed to realize ZVS for all switches when the input voltage has

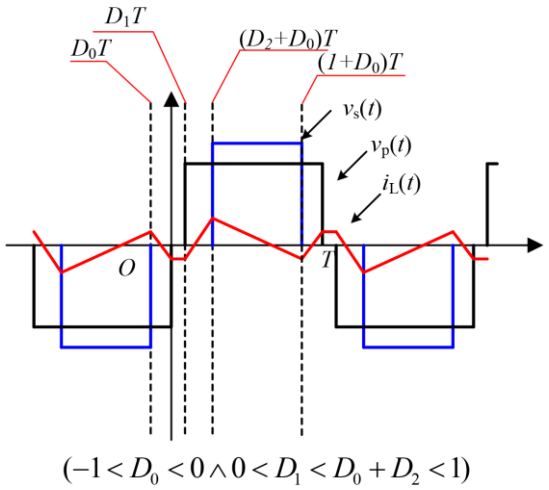


Figure 2.18. Switching waveform of in-phase TPS [106].

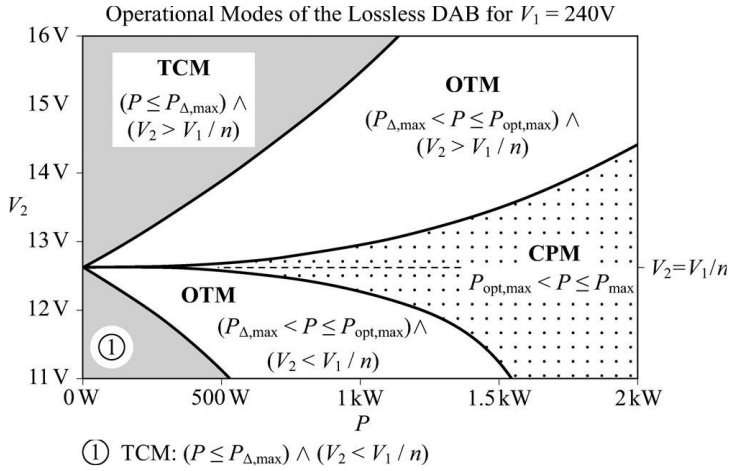


Figure 2.19. DAB operating modes at different voltages and loads [88].

the double line frequency ripple in [13, 99]. Under the light load, TPS is employed to improve efficiency. When power increases, TPS reaches the maximum power, then DPS modulation takes over. At the same time, the switching frequency also varies with the load. With the increase of power, the switching frequency decreases. Experimental results are shown in Figure 2.20, indicating the transformer current envelope follows grid voltage, as shown in Figure 2.20 (a). The boundary between DPS and TPS modulation is shown in Figure 2.20 (b). A similar MPS modulation is also proposed in [84], which also includes in-phase TPS modulation.

Overlap and non-overlap TPS modulations are more suitable for applications where ZVS is necessary. Overlap TPS modulation has higher power capability. For in-phase TPS modulation, it can also secure ZVS. Note most TPS modulations are developed where the voltage gain is far from 1, with a light load.

2.3.5 Hybrid Modulation

For traditional phase-shift control, there are three control freedoms to regulate the power and the switching current. But if combining the duty-cycle control and phase-shift control, there will be more control freedoms, which means more flexible control algorithms.

[107, 108] propose the integration of pulse-width-modulation and phase shift modulation, which is called a hybrid modulation strategy. Parts of the switches will operate in PWM mode instead of a constant 50% duty cycle. Figure 2.21 shows the PWM signal of a hybrid modulation. The PWM signals at the secondary side are not 50% duty cycle when the reflected secondary-side voltage is higher than the primary-side voltage. So

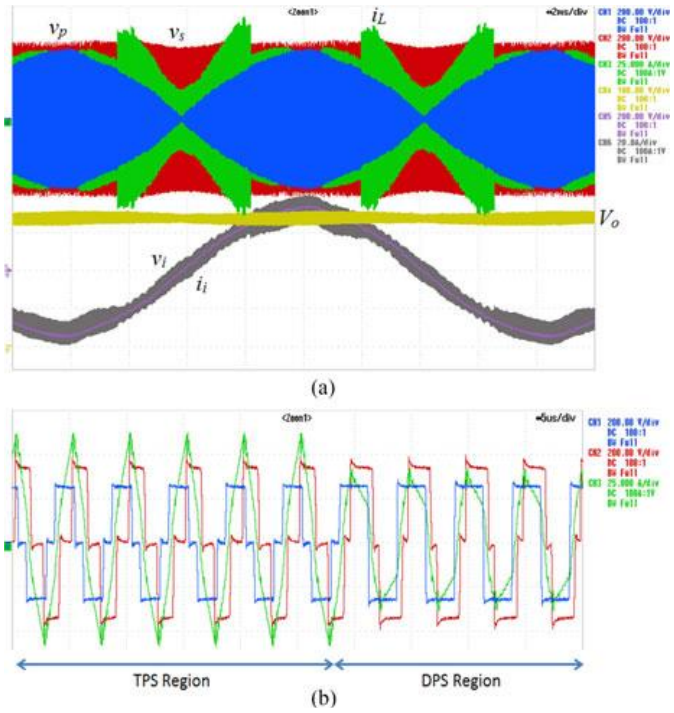


Figure 2.20. (a) Experimental DAB waveforms at 5.1 kW. (b) Phase-shift jumping region [99].

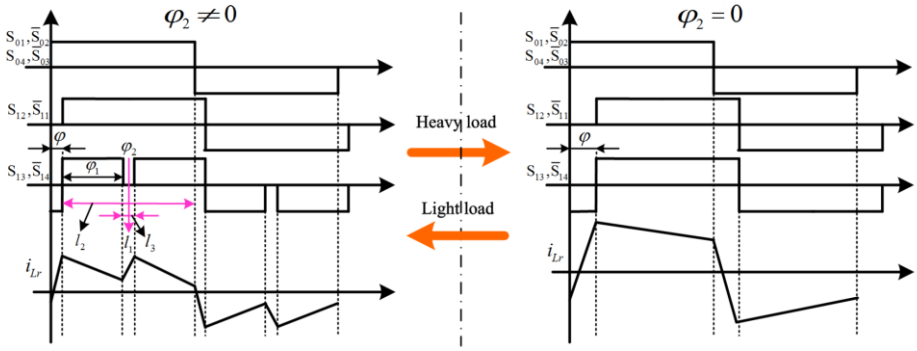


Figure 2.21. The work mode transition of HPPS control with different loads [108].

typically hybrid modulation strategy is used to eliminate the reactive power and relieve the current stress at the light load under-voltage mismatch condition, i.e., $V_{in} \neq nV_o$. [109] also aims at extending the range of ZVS to further tune the performance of the DAB converter.

In a summary, different modulation strategies have been discussed in detail under different loads and voltages. But they all have the limitation of ZVS realization in different operational conditions. So how to utilize the modulation strategies and realize smooth transition needs to be answered. The performances of the different modulation strategies are summarized in Table 2.1.

2.4 Common-mode (CM) Analysis in Dual Active Bridge

To reach higher power density, SiC MOSFET begins to be adopted in automotive, photovoltaic, and aircraft, which however induces more common-mode noise caused by high switching frequency and high dv/dt in the spectrum from 150 kHz to 30 MHz. With the increase of the switching frequency, more components appear from 150 kHz. With the high dv/dt, more CM noise appears from 1 MHz. In the DAB converter, there are capacitors to support the stable voltage potential and choke the current ripple caused by switching action. Typically, based on the requirement of the current ripple, an LC filter is applied at the input or the output of the DAB converter [110, 111]. So the differential-mode (DM) noise can be easily dumped. But as for the common-mode (CM) noise, seldom papers have addressed the common-mode performance in a DAB converter.

The transient processes caused by switching actions coupled with common-mode parasitic capacitance then excite the common-mode current (CMC) [43, 112, 113]. Such

Table 2.1. Summary of different modulation strategies.

	SPS	EPS	DPS	SDPS/PDPS	OTPS	NTPS	ITPS
Recommend voltage gain	1	<1 or >1	<1 or >1	<1 or >1	<1 or >1	$\ll 1$ or $\gg 1$	<1 or >1
Recommend load	Heavy	Medium	Medium	Heavy or Medium	Heavy or Medium	Light	Light
ZVS under recommend load	All	All	All	All	All	All	All

capacitance includes the winding capacitance of the high-frequency transformer in regular isolated DC-DC converters [114] in Figure 2.22 and the parasitic capacitance of the grounded heatsink [43] in Figure 2.23, all providing the path for CMC. To represent the potential parasitic capacitors in the transformer the six lumped capacitor model is developed [115], including the capacitor between the primary-side windings, the capacitor between the secondary-side windings, and the capacitor across the primary side and the secondary side. [116] proposed the concept of the necessary number of capacitors in the transformer CM analysis. In a summary, only two capacitors are enough to represent the six lumped models in the equivalent circuit of the transformer when considering the CMC path. Figure 2.24 shows all the cases of the two-capacitor model. Based on the different purposes, the different equivalent capacitors can be here to help analyze the circuit performance. In [114], the two capacitors between the dotted terminal and the undotted terminal are used to analyze the CM performance in a half-bridge LLC converter.

With various EMI standards available, a CM analytical model of DAB is necessary to estimate the CM behavior with different modulation strategies. The mechanism of common-mode voltage (CMV) generation is discussed in [117, 118], concluding that two H-bridges are the CMV sources. Figure 2.25 shows the equivalent circuit of the H-bridge in the CM loop.

With the CM sources and the existing CM capacitance, the equivalent CMV model can be established [114, 117], which eventually derives the CMC envelope [114] thereby guiding the design of the CM filter. Figure 2.26 shows the comparison between the

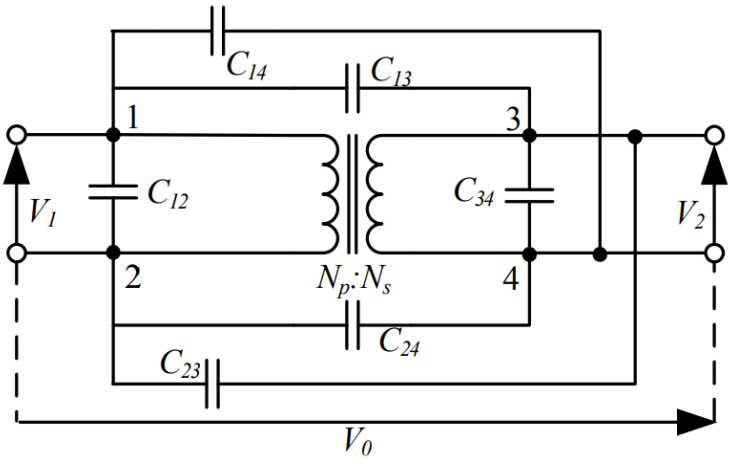


Figure 2.22. Six lumped capacitances model [115].

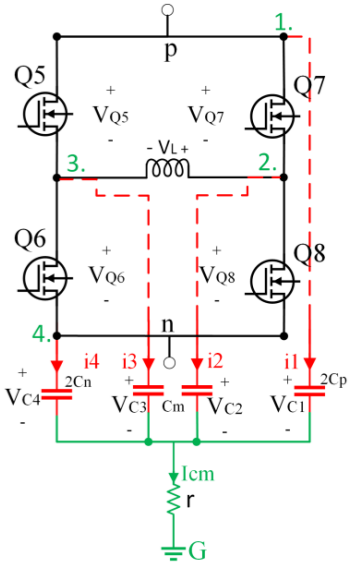


Figure 2.23. Single-phase full-bridge with parasitic capacitances and switching nodes [118].

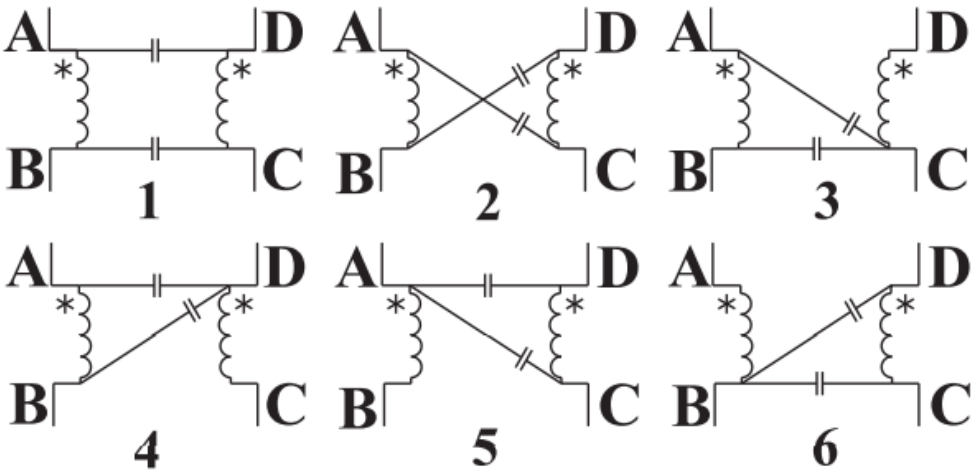


Figure 2.24. Six possible two-capacitor CM winding capacitance models for a two-winding transformer [116].

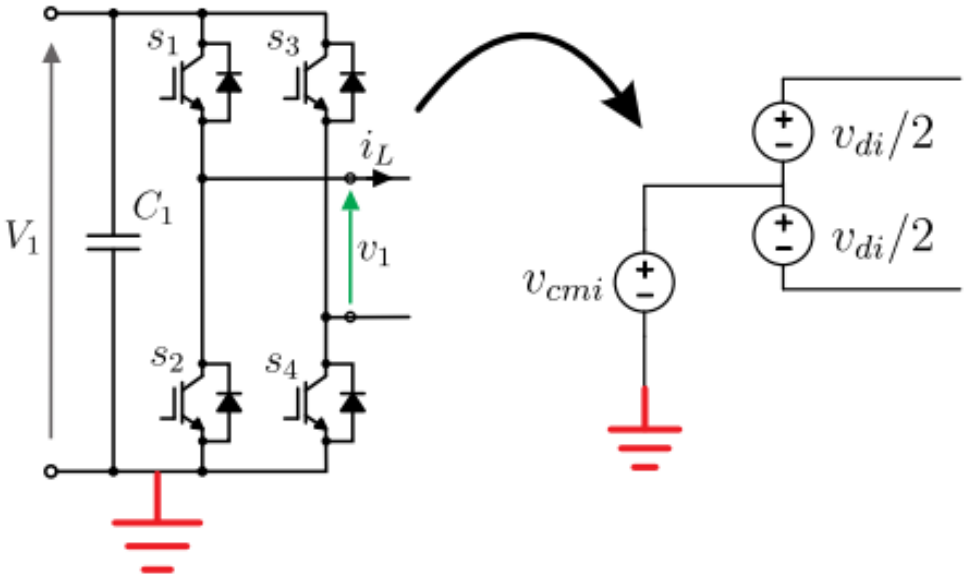


Figure 2.25. Equivalent circuit of the H-bridge in CM [117].

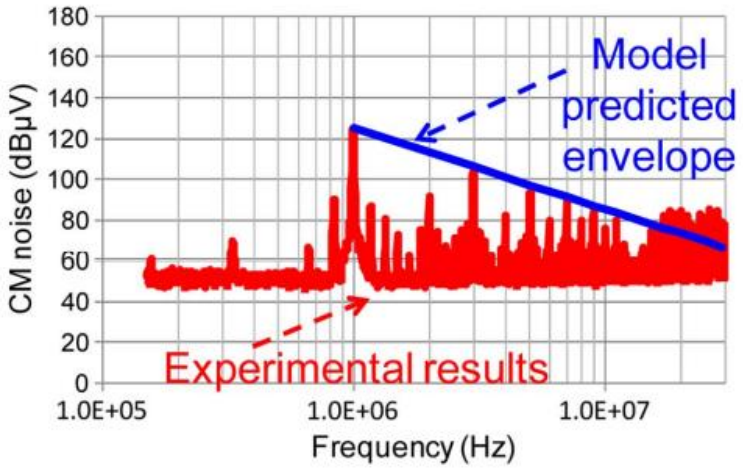


Figure 2.26. Measured EMI spectrum and the predicted EMI spectrum envelope of the LLC prototype with the proposed CM choke [114].

experimental result and the predicted result of the EMI spectrum in an LLC converter.

[118] mentioned the potential parasitic capacitance and CM performance in a half-bridge DAB converter, which is shown in Figure 2.27. The parasitic capacitance is considered from the middle points of the half-bridge to the grounded heatsink. The parasitic capacitance at both sides of the transformer and from the transformer to the ground are listed in the figure. [119] discussed the mitigation of CM current in series input and parallel output (SIPO) series resonant DAB converter. [117] proposed a method of using a modified H-bridge structure inspired by a PV inverter to reduce the CMC flowing through the transformer in aerospace applications. Still, there is no general CMV model established yet.

Furthermore, when applying MPS modulation in a DAB converter, different modulation strategies show different steady-state performance in terms of reactive power, current stress, and efficiency. In [111], the consideration of stability based on SPS and DPS modulation strategies is also addressed, but there is no discussion about the influence of modulation strategies on the DAB CM performance. An analytical CM model to quantify the CM performance under different modulation strategies is an inward search.

2.5 Current Spike Elimination Method in Dual Active Bridge

As discussed above, most of the newly proposed modulation strategies only focused on steady-state performance such as securing zero-voltage switching (ZVS) and reducing the transformer current RMS, instead of the reliability issues during transient states. Such requirements of the load transient, however, vary with applications. For example, when

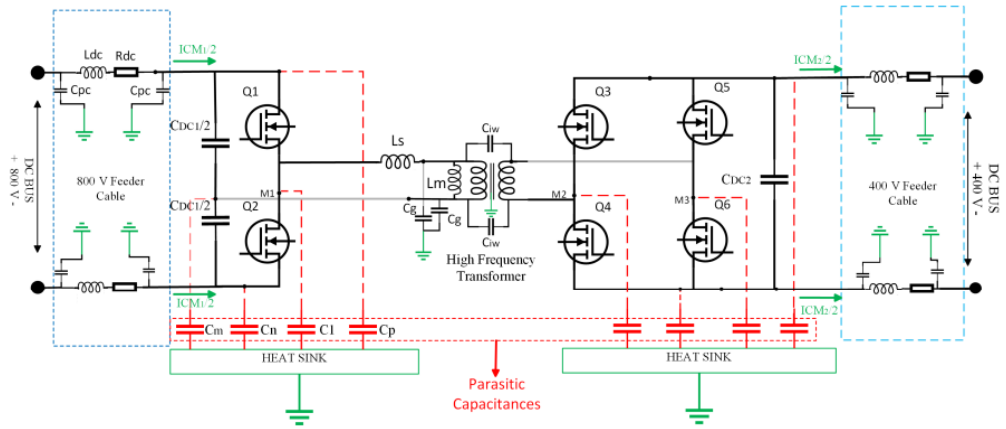


Figure 2.27. Conventional single-phase DAB system with half-bridge on MVDC side [118].

charging the EV batteries, the load current should be adjusted based on the command from the battery management system. in real practice, we can tune such the reference charging current into a ramp function, which means the charging current can change continuously during the load transient. For the DAB converter, the phase shift regulating the load current can then change continuously. Therefore, in the charging process of the battery, there is less requirement for the dynamic response.

But when the EV battery charger operates in the vehicle to grid (V2G) mode or vehicle to load (V2L) mode, the discharge current should have the ability to respond to the fast load transient. The same thing happens when applying the DAB converter to the grid-connection equipment as mentioned in Chapter I. The low voltage DC bus interfaced to the DAB converter integrates different kinds of load, as shown in Figure 2.28, which then requires the DAB converter to respond to the fast load transient. A typical application of the DAB converter is to serve as the interface between a high-voltage and a low-voltage DC bus. While the low-voltage bus can be a DC microgrid connected to different types of loads (motor drive or resistive load), an energy source, or an energy storage device, it also can feed the high-voltage DC bus when necessary. For medium-voltage devices for grid applications (10 kV device), the switching loss is much higher than that in lower voltage SiC devices (1700 V) [120], which means ZVS for the medium-voltage device is necessary.

To improve the dynamic performance, a small-signal model is built to accurately describe the magnitude and the phase information in the frequency domain [121, 122]. [123] gives a detailed explanation of the influence of using digital control in real

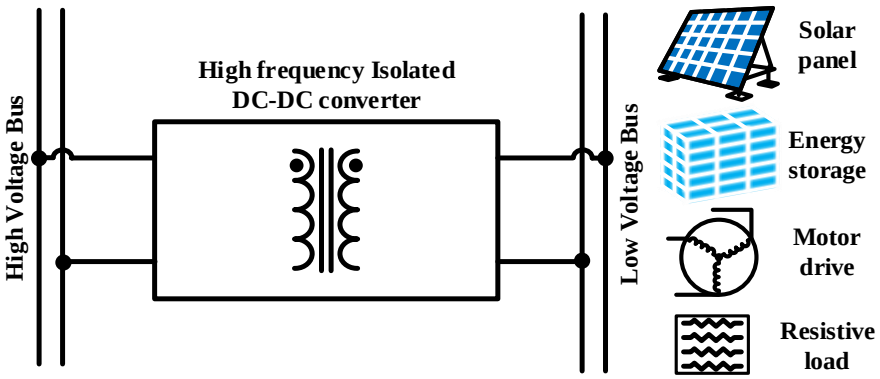


Figure 2.28. Application of the grid-connection DAB converter.

applications. [124] further explores the difference between small-signal models in different modulation strategies. To increase the dynamic response of a DAB converter, the feedforward control can be applied in the control loop as shown in Figure 2.29. The input voltage, the output voltage, the output current, the output voltage reference, and the converter parameters are used to predict the phase shifts in the next switching cycle. In this way, the phase shifts are mainly derived from the feedforward control. The PI control is paralleled with the feedforward control to compensate for the static state error of the controlled variables. Figure 2.29 is an example of feedforward control in DAB when controlling the output voltage [76]. When controlling the output current or the output power a similar control method can also be adopted for the DAB converter [125, 126]. The basic theory of the feedforward control is using the power equation of the DAB to derive the phase shift. When the reference voltage or current changes, the derived phase shift can change swiftly.

For the digital control, the typical used micro control units (MCU) are DSPs and FPGAs. The MCU integrates the analog-to-digital converter (ADC), data processing, protection, communication, and PWM signal generation functions in Figure 2.30. The interrupts are trigged periodically to execute the code already saved in the flash and finish the functions mentioned above. For a DAB converter, the phase shifts are updated in each interrupt period and then are applied to the PWM generator. Hence the change of the PWM signals for eight switches in a DAB is not continuous. When a DAB converter has a fast-dynamic response to fulfill the output specs in load transients [127], it can cause the reliability issues,

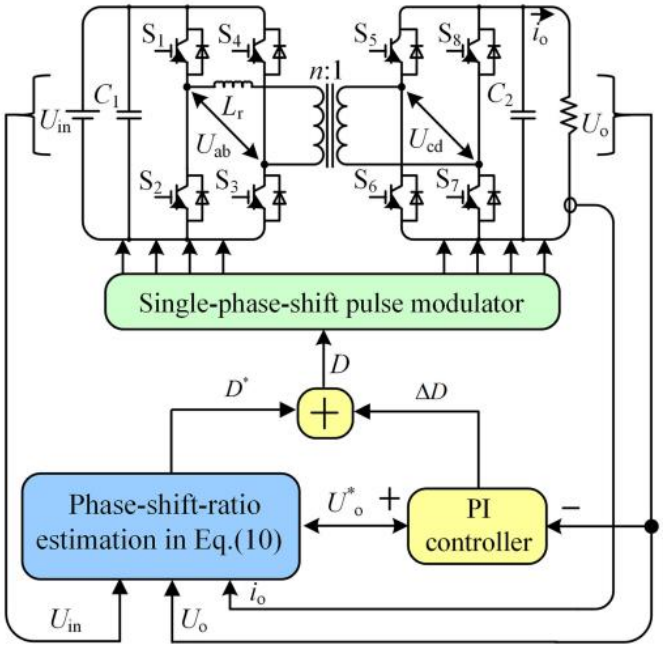


Figure 2.29. Block diagram of the MPS control scheme with the output current and input voltage feedforward for DAB DC-DC converters [76].

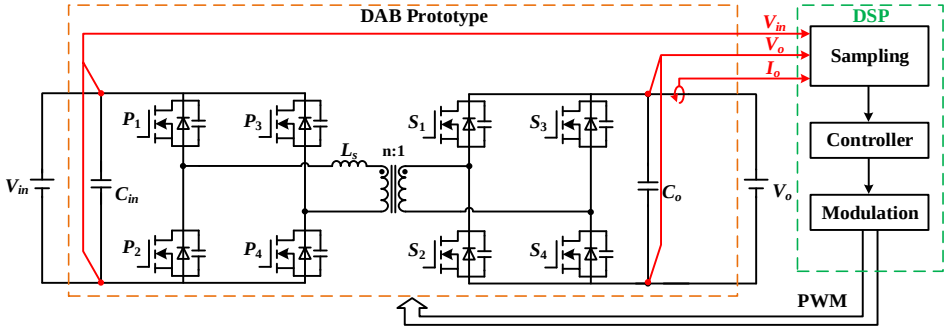
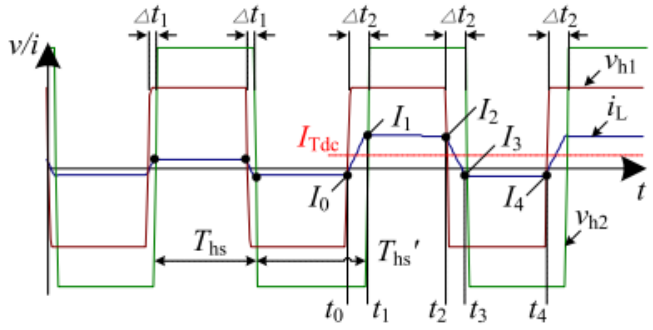


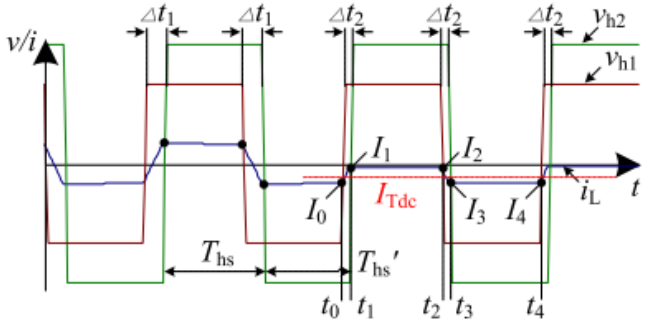
Figure 2.30. Topology of DAB converter with digital control [124].

such as the current spike in the transformer further yielding the saturation of the magnetic core or even damaging semiconductor devices. The root of such an issue is the abrupt change of phase shifts thus transformer-current waveform, as described in the previous literature [86, 128]. Figure 2.31 is an example of the switching waveform during the load transient with SPS modulation. When the load current increases in Figure 2.31 (a), there is a current spike in the transformer. In the next switching cycles, there is also the DC offset current in the transformer. This offset current will be consumed by the loop resistance gradually. When the load current decreases in Figure 2.31 (b), the offset current will also exist for the serval switching cycle until later diminished.

Meanwhile, when adopting MPS modulation in the DAB converter, the load transient can cause the fast switching between different modulation strategies. Thus, the transformer current spike becomes a more common issue. Some simple active compensation methods were discussed to mitigate the transformer current change by modifying the duty cycle of certain switches in the next switching cycle compared to the previous during the phase shift change [86, 129-131]. As shown in Figure 2.32, the compensation method is applied when the load transient happens. When the modulation strategy switches from TPS to DPS, there is an intermediate state inserted between two different modulations to compensate for the potential transformer current spike. Traditionally all the switches in DAB keep the 50% duty cycle, and the power is only regulated by the phase shift. To mitigate the transformer current spike, the duty cycles in the intermediate state do not keep at 50%, which makes the control freedoms more flexible. [130] provides the solution for the additional duty



(a)



(b)

Figure 2.31. Transient waveforms under the SPS updating strategy with a constant power flow: (a) Increase in power; (b) Decrease in power [128].

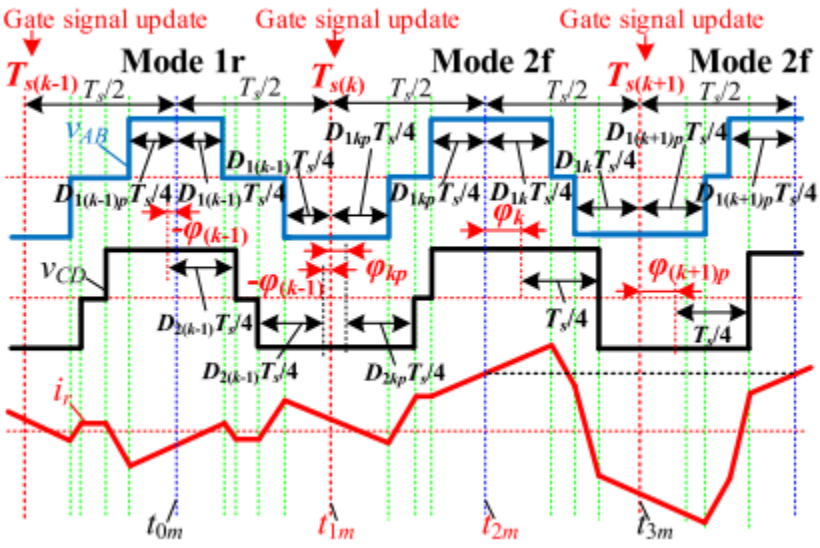


Figure 2.32. Waveforms of the working mode transition without dc bias current [130].

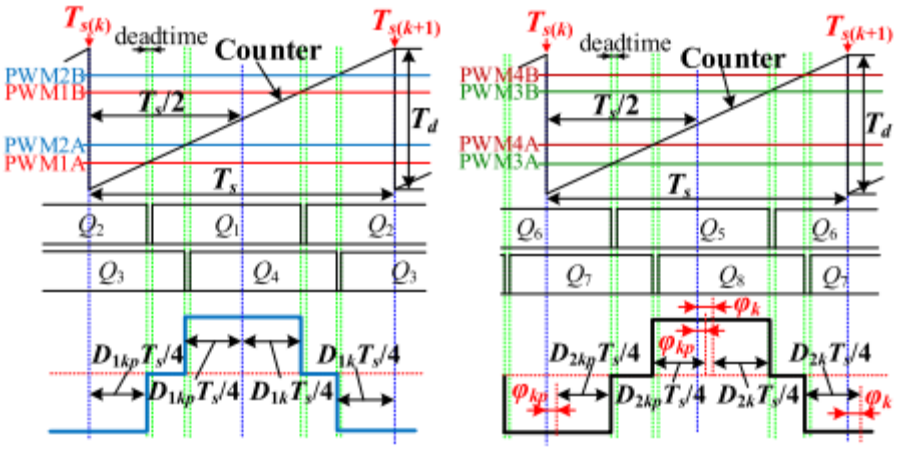
cycle control in the intermediate state-based DSP PWM generation. The detailed sequence and arrangement of the switches are discussed in Figure 2.33.

Figure 2.34 shows the structure of the control loop when applying the duty-cycle compensation method after deciding the phase shifts and the switching pattern in the next switching cycle. Such active compensation during the transients, however, can make the control complicated when applying MPS modulation to cover a wide voltage and power range. Because the transformer currents are independent in each modulation mode, the compensation method has to consider all transitions among all modulation modes.

2.6 Summary

At first, this chapter presents different ZVS theories, such as energy-based theory and current-based theory. The essence of ZVS realization is also pointed out, which is the resonance between the loop inductance and switch C_{oss}. The concept of equivalent capacitance considering the voltage-dependent characteristics of switch C_{oss} is proposed and applied in ZVS derivation.

To ensure the realization of ZVS in DAB, SPS, DPS, and TPS modulations can all be used in different operating ranges. SPS is normally used when voltage gain is nearly 1 or away from the unity value or at the medium load, PDPS, SDPS, or overlap TPS are good choices for the sake of ZVS. At light load, non-overlap TPS has the advantage of realization of ZVS even when the input or the output voltage is extremely low. In-phase TPS owns advantages of ZVS realization when the input or the output voltage is not extremely low. MPS combines different modulations strategies and utilizes their advantages in different



(a) (b)

Figure 2.33. Gate signal generation: (a) for the primary-side switches;(b) for the secondary-side switches [130].

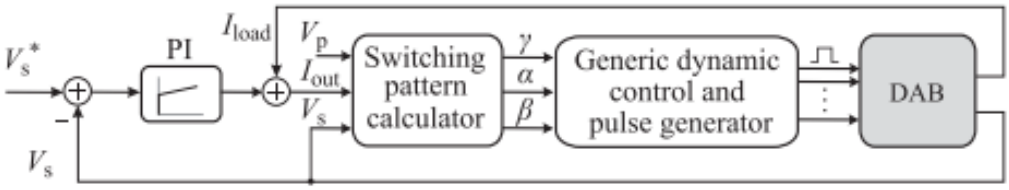


Figure 2.34 Generalized closed-loop control block diagram for the DAB converter [127].

at a heavy load. In this case, all switches can realize ZVS. When the voltage gain is far operation conditions, which helps DAB to become an excellent candidate for various applications. However, there are still some questions to be answered in future research. One important question is how to switch among different modulation modes seamlessly. Many literatures discuss the utilization of different modulation strategies and assign them to different operation areas. However, none of them talks about transitions at boundary points between different modulations, particularly given such transitions can cause a current spike in the transformer.

Besides, with the application of wide band-gap (WBG) devices, the power density can be further increased with a higher switching frequency, which however tends to worsen the CM performance. Considering automotive standards, the EMI noise in this region needs to be paid more attention to. With the consideration of CM performance, the potential parasitic capacitance in the CM loop is investigated, including the parasitic capacitance of the active switches and the transformer. But there is no general CMV model for DAB to analyze the CM behavior, especially when applying MPS modulation strategies.

Finally, to meet the dynamic response specs for DAB in V2G, V2L, or other grid connection modes, the feedforward control can be utilized to predict the phase shifts based on the input, the output, the DAB parameters, and the feedback reference. Caused by the digital control, the current spike in the transformer brought by the fast load transient introduces a new challenge to the DAB control. This becomes a more common phenomenon when applying MPS modulation. The active compensation method with the

duty-cycle control can help to eliminate the transformer current spike and offset it by inserting the intermediate state between different modulations. But with more modulation strategies, the compensation method tends to be more complicated.

Chapter 3 SMOOTH TRANSITION PROCESS IN MULTIPLE PHASE SHIFT MODULATION

As the modulation strategies have been discussed in many literatures, the better steady-state performances have been validated compared with SPS control. The challenge lies in the difficulty of combining different modulation strategies through the wide-voltage range and full-load range. Also securing zero voltage switching (ZVS) is important to minimize the risk of the switch-bridge crosstalk caused by the hard switching-on, thereby enhancing the system reliability. With DPS and TPS control being introduced to extend the range of ZVS, the design principle then needs to consider the proper selection of the modulation strategies, the boundary conditions between different modulation strategies, and secure the smooth transition between the modulation strategies throughout the whole operation range [101]. Experimental results are validated on a SiC-based charger with an output voltage of 200~450VDC and power of 0~20kW.

3.1 Zero-voltage-switching (ZVS) in DAB-Based Battery Charger

To build a bidirectional EV battery charger, a boost PFC + DAB circuit is a widely used candidate [132, 133], as shown in Figure 3.1. Unlike other conventional resonant circuits such as LLC [134], the DAB converter uses fewer passive components thereby potentially increasing the power density.

For higher power designs such as 20kW, two switches in paralleled are applied in the real prototype. In this prototype, ROHM's 1200V and 650V SiC MOSFET are selected in the DAB part, which has the competitive price on the market in 2018. The existing

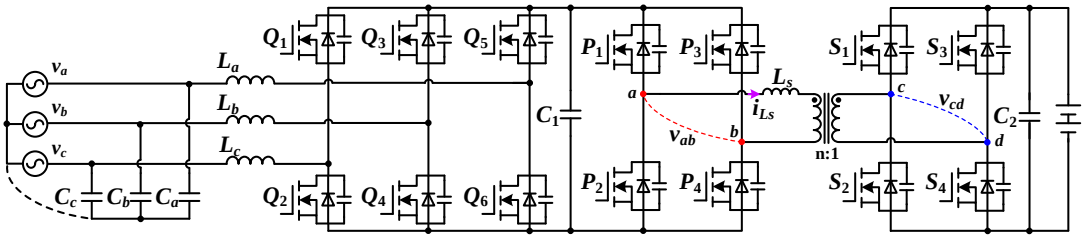


Figure 3.1. Three-phase PFC + DAB for a two-stage battery charger.

prototype with ROHM's SiC MOSFET is shown in Figure 3.2. Two 650V/93A ROHM SiC MOSFETs were paralleled for the DAB secondary side. Two 1200V/72A ROHM SiC MOSFETs were paralleled to form the DAB primary side. Air cooling is adopted, given it is an off-board charger. For the prototype, the length is 35cm, the width is 31cm and the height is 6.5cm. The overall power density is ~3kW/L. A drawback of ROHM SiC MOSFET is that the maximum negative voltage during off-state is only -4V. To avoid the acceleration of aging on the gate, the recommended maximum off-state voltage on the gate is only -2V, which however brings the risk of the crosstalk when the complementary switch in one phase shift suffers hard switching-on. So it is important to ensure ZVS, therefore, suppressing crosstalk between complementary switches and reducing the probability of the leg shoot-through [135]. Experimental gate-signal waveforms in Figure 3.3 (red curves) of the hard-switching-on and soft-switching-on are compared. The crosstalk is eliminated during soft switching-on, which reduces the chance of shoot through. Various efforts have focused on suppressing the switch crosstalk in previous literature, mainly on the design of gate-drive circuits [23, 71, 72].

This research focuses on the ZVS realization of the DAB converter. The high dv/dt during the hard-switching-on can cause the positive voltage spike on the complimentary switch, which can trigger the complimentary switch and cause the failure [40].

The previous literature also takes advantage of the realization of ZVS to eliminate the crosstalk in the half bridge. The inductive power transfer system in [136] discussed the side-effect and the limitation caused by the crosstalk during the fast dv/dt in hard switching

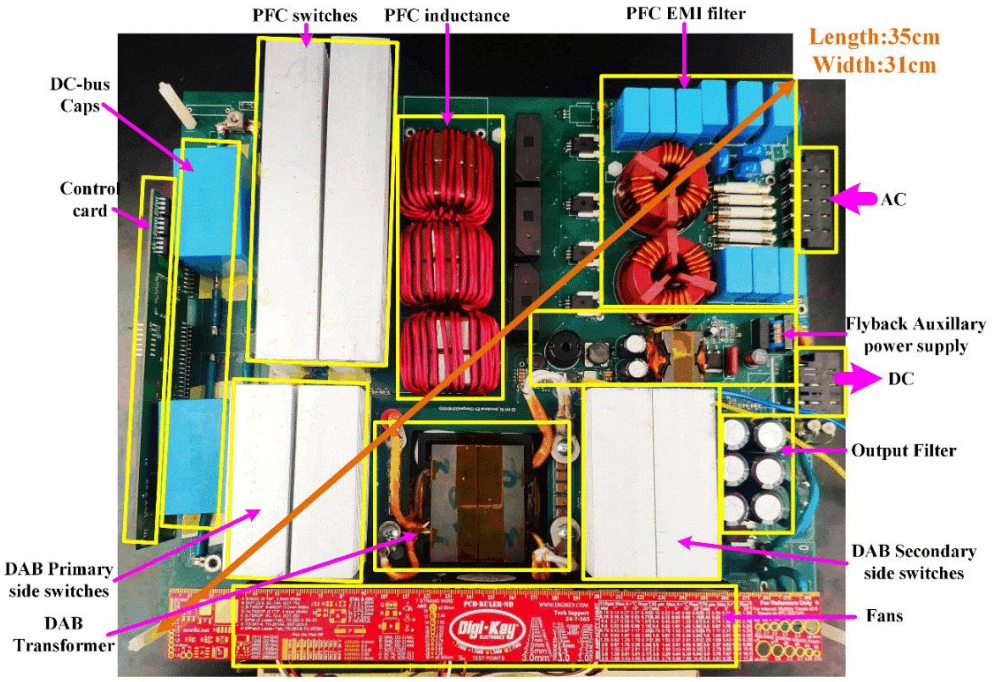
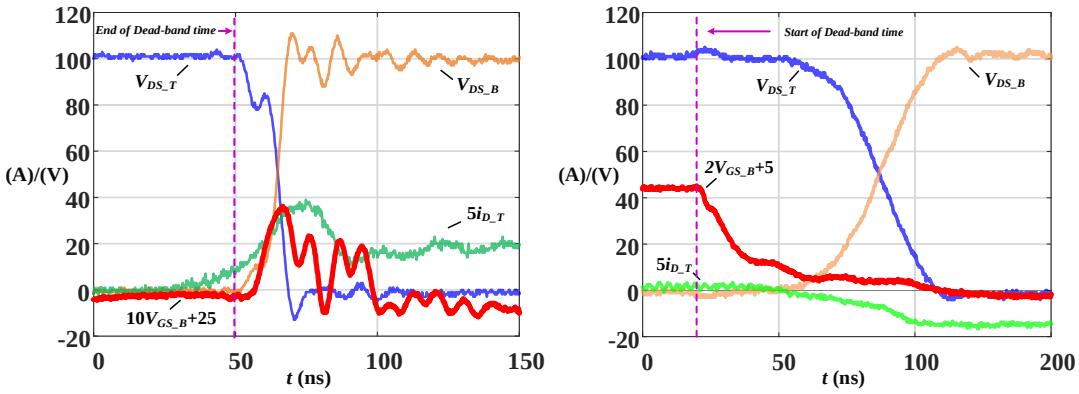


Figure 3.2. Prototype of the battery charger.



(a) (b)

Figure 3.3. Influences of switching action on the gate signal in a bridge leg (experimental results): (a) hard-switching-on; (b) soft-switching-on.

transient when using SiC MOSFET. By designing an additional compensation network to realize ZVS, the performance of the proposed converter is improved. Also [137] designed a LLC converter with ZVS realization to prevent the serious crosstalk caused by high dv/dt from the false conduction and failure of the fast switching devices. In [138], the proposed DAB converter also tries to extend ZVS to prevent the system missing-protection and the damage of the complementary switches due to the crosstalk.

The test result with the hard-switching-on influence on the complimentary switch was tested in the developed prototype shown in Fig. 3.3 (a). The voltage spike at the bottom switch V_{gs} when the top switch hard turns on is over 1.2 V under 100V. The threshold voltage is around 2.3 V, which introduces the high possibility of the crosstalk when continuing increasing the voltage rating to 700 V. By realizing ZVS for the switches, there is no voltage spike at the complimentary switches. The test result of the ZVS influence on the complimentary switch is shown in Fig. 3.3 (b). For more detailed explanations: (1) ZVS shows lower dv/dt (a resonant process). The voltage spike is caused by the current flowing through the C_{gd}. During the ZVS transition, C_{gd} is a part of the resonance, so the voltage across the C_{gd} changes slowly following the ZVS resonance compared with high dv/dt in hard-switching-on. (2) The voltage transient (dv/dt) in ZVS happens during the dead time. Before the top switching turns on, the voltage transient has been finished. There is no overlap of the dv/dt interval and the top switch on-state interval. By realizing ZVS for the switches, the possibility of the failure causing the crosstalk during hard-switching-on is eliminated.

The profile of such a battery charger is shown in Figure 3.4. Before connecting charger output terminals to the battery, the output capacitors should be pre-charged to the battery voltage [92, 139], then the charging current ramps up to maximum current followed by constant current (CC), constant power (CP), and constant voltage (CV) modes. When the battery is charged with the maximum current or power, ZVS can be realized easily by SPS modulation because of the heavy load condition. But during the transition, for example, the pre-charge process or current ramping-up, the switches are at the risk of hard switching on. So, it is important to extend the ZVS range even in the transient process.

3.2 Modulation Strategy within the Whole Operational Range

When V_{in} is not equal to nV_o, DPS control can be adopted to secure the ZVS for all switches in a certain range [99, 140]. When the load is very light, a TPS algorithm can be employed, which maintains ZVS down to zero power. As a result, one solution is to gradually switch from SPS to DPS and then to TPS as the charger transitions from heavy load to light load. The definition of symbols is shown in Table 3.1. To simplify the analysis, the DC-link voltage is fixed to V_{in}=700V, which can fulfill the needs for the three-phase grid of 380~480VAC when using the conventional three-phase two-level PFC converter.

In traditional SPS control, the secondary-side switches easily lose ZVS at the medium load or light load when the reflected battery voltage is lower than the DC link voltage. When the reflected battery voltage is higher than the DC-link voltage, the primary side switches easily lose ZVS at the medium load or light load. The drain-source current when

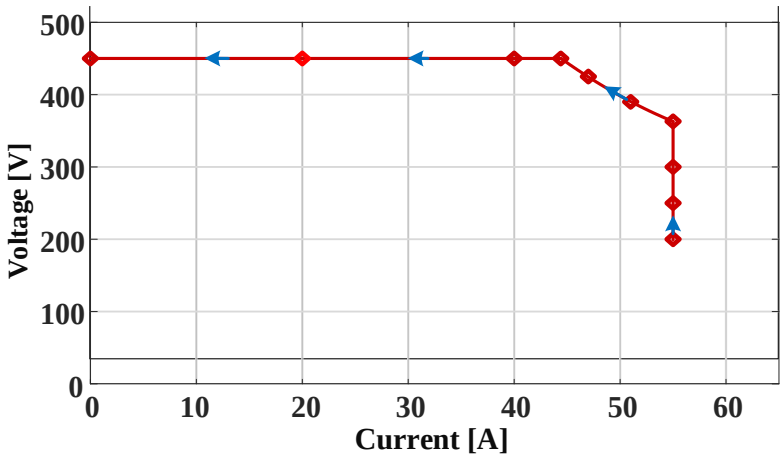


Figure 3.4. Charging profile of an EV battery charger.

Table 3.1. Definition and Values of Symbols

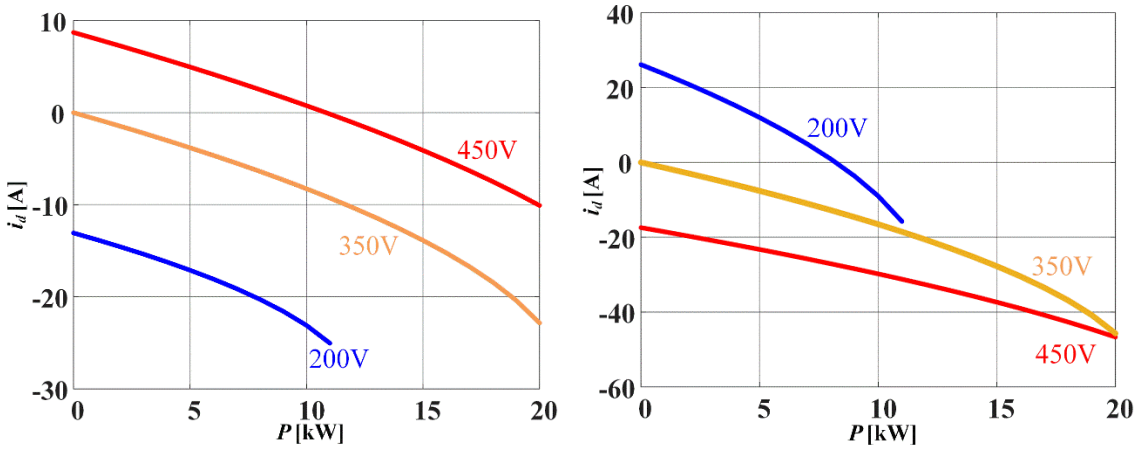
Names	Values
Inductance reflected the primary side (L_s)	28.7μH
Transformer turn ratio (n)	2:1
Battery voltage (V_o)	200~450VDC
DC-link voltage (V_{in})	700VDC
Switching frequency (f_s)	100kHz
Switching period (T_s)	100μs
Primary side switches	SCT3030KL
Primary side switches equivalent C_{oss} (700V)	239pF*2
Secondary side switches	SCT3022ALHR
Secondary side switches equivalent C_{oss} (350V)	351pF*2
Paralleled switches	2

switches turn on is shown in Figure 3.5. When the current is positive, it means that switch is suffering a hard-switching-on.

The control strategy is then divided into two main regions based on the relationship between DC-link voltage and the reflected battery voltage. Within these two main regions, each area is further divided into several states. When the input voltage is higher than the reflected output voltage, primary-dual-phase-shift (PDPS) control is applied. Otherwise, secondary-dual-phase-shift (SDPS) can contribute to better performance. Regardless of states, to realize ZVS the magnitude of the leakage inductance current I_r must be sufficient to completely discharge/charge the drain-source capacitance of devices within bridge legs during the dead time. The minimum required current for ZVS realization has been discussed in Chapter 2 considering different modulation strategies.

All three phase shifts are defined in Figure 3.6. P_1~P_4 are gate signals of primary-side switches and S_1~S_4 are for secondary-side switches. All switches have a 50% duty cycle. To specify the implementation of MPS control, the whole operational area is divided into 8 states. The detailed operation principles are discussed in the following content.

$$\begin{cases} \phi = \dfrac{\Delta t_1}{T_s / 2} \\ \phi_p = \dfrac{\Delta t_2}{T_s / 2} \\ \phi_s = \dfrac{\Delta t_3}{T_s / 2} \end{cases}. \tag{3-1}$$



(a) (b)

Figure 3.5. Drain-source current for each switch when turning on: (a) primary side P1; (b) secondary side S1.

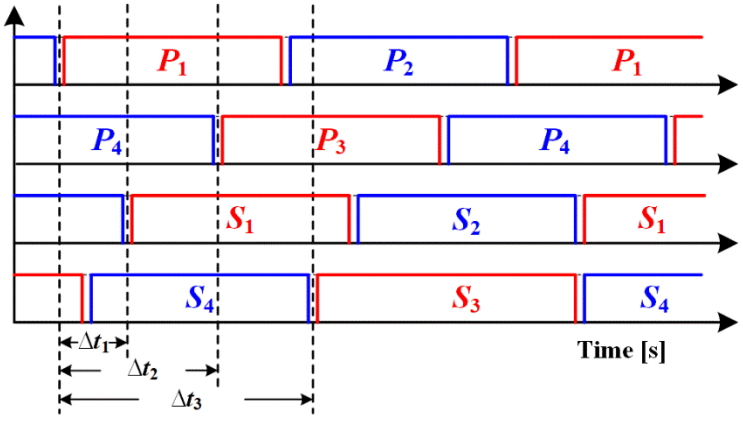


Figure 3.6. Definition of different phase shifts.

3.3 Switching Waveform of Multiple-Phase-Shift Modulation

3.3.1 Switching modes when $V_{in} > nV_o$

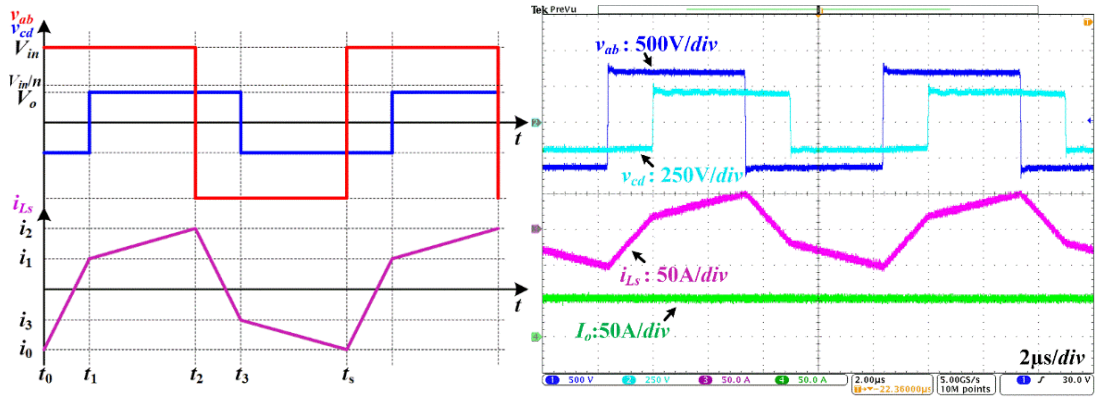
State 4: At the heavy load, SPS can realize ZVS for all switches. The switching mode is shown in Figure 3.7. When $V_{in} > nV_o$, the peak current always appears when the primary-side switches turn off. In SPS control, all the phase shift relationships are shown in (3-2).

$$\begin{cases} \phi_p = 1 \\ \phi_s = 1+\phi \\ P = \dfrac{V_{in}V_o\phi(1-\phi)}{2L_s f_s} \end{cases}. \tag{3-2}$$

In State 4, if $0<\Phi<0.5$, when Φ is decreasing, the power decreases at the same time. Based on the demanded power, we can reverse calculate Φ and then Φ_p or Φ_s. This applies to the states below.

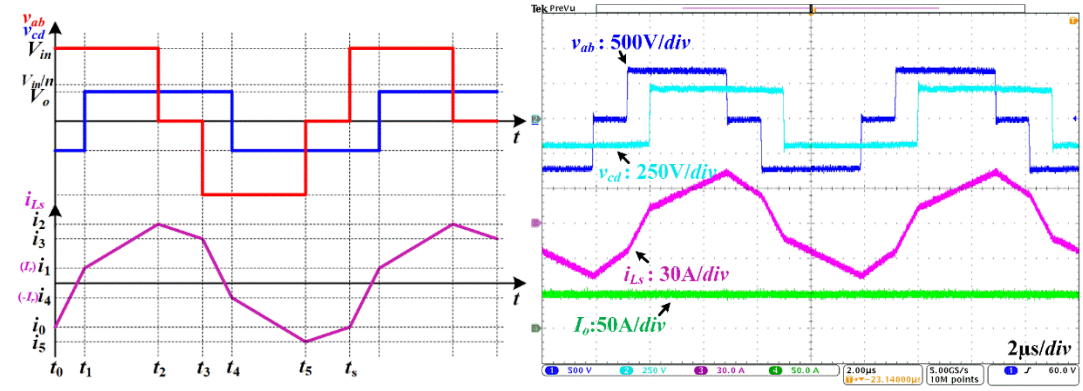
State 3: With the power decreasing, DPS takes over. The primary side inner phase shift Φ_p then decreases. In Figure 3.8, the leakage inductance current i_1 when secondary side switches turn on is fixed at I_r to maintain secondary-side ZVS. i_0 then starts to increase. With fixed i_1, the primary side inner phase shift Φ_p can be derived based on Φ for the sake of the symmetry of the transformer current in one switching period. The relationship between different phase shifts and power is shown in (3-3).

$$\begin{cases} \phi_p = \dfrac{nV_o - 4L_s f_s I_r}{V_{in}} + 2\phi \\ \phi_s = 1+\phi \\ P = \dfrac{(\phi V_{in} + nV_o)(V_{in} - nV_o) - \phi^2 V_{in}(V_{in} + nV_o)}{4L_s f_s} + nV_o I_r + \phi V_{in} I_r \end{cases}. \tag{3-3}$$



(a) (b)

Figure 3.7. Switching waveform of state4 (SPS): (a) design waveform; (b) experiment waveform @ input voltage 700V, output voltage 200 and 11kW.



(a) (b)

Figure 3.8. Switching waveform of state3 (DPS): (a) simulation waveform; (b) experiment waveform @ input voltage 700V, output voltage 200 and 10kW.

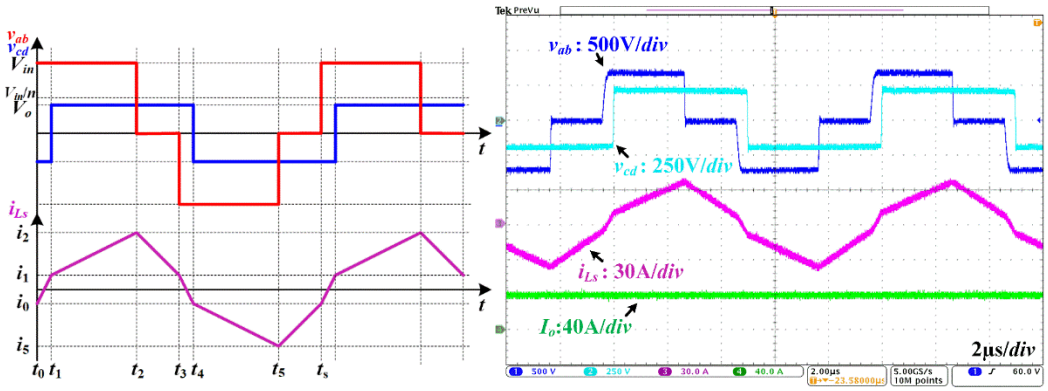
State 2: When i_0 increases to $-I_r$, i_1 begins to decrease at the same time, as shown in Figure 3.9 until they are both equal to 0. Then the phase shift Φ is 0, leaving half of the primary and secondary switches unable to fully realize ZVS, i.e., quasi ZVS (QZVS). Here we define QZVS as when the parasitic capacitance of switches can only be partly discharged before turning on. It is not full ZVS, but still much better than hard switching. The absolute values of leakage inductance current at i_0 and i_1 are the same in this state, both of which can be derived based on Φ. Furthermore, Φ_p can be also derived as (3-4).

$$\begin{cases} \phi_p = 1 - \dfrac{(V_{in} - nV_o)(1-\phi)}{V_{in}} \\ \phi_s = 1 + \phi \\ P = \dfrac{(V_{in} - nV_o)(1-\phi)nV_o + (V_{in} + nV_o)\phi V_{in}}{4L_s f_s} \cdot \dfrac{(1-\phi)nV_o}{V_{in}} \end{cases} . \quad (3\text{-}4)$$

State 1: With the charging power continually decreasing, i_0 increases and fulfills ZVS for secondary-side switches, and i_1 continues decreasing, as shown in Figure 3.10. Φ_p is decreasing as well. In this state, half of the switches can only realize QZVS. The absolute values of i_0 and i_1 are the same. Φ_p is shown in (3-5).

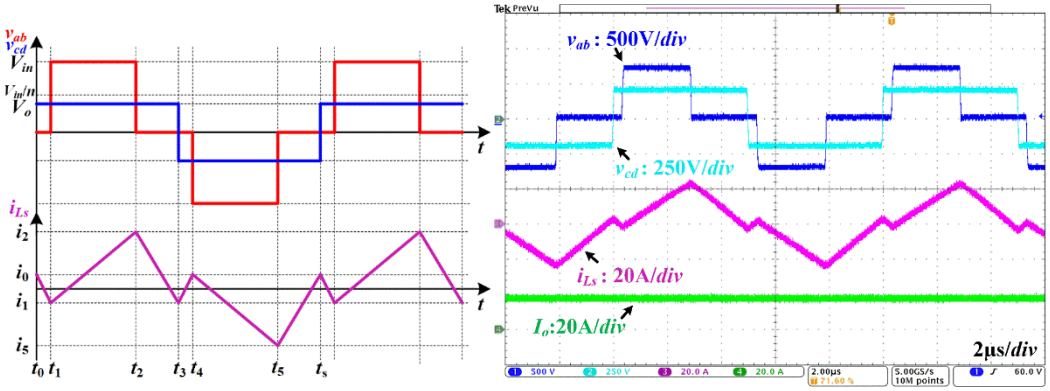
$$\begin{cases} \phi_p = \dfrac{nV_o(1+\phi)}{V_{in}} \\ \phi_s = 1 + \phi \\ P = \dfrac{(V_{in} - nV_o)(1+\phi) + \phi V_{in}}{4L_s f_s V_{in}} \cdot (1+\phi)n^2 V_o^2 \end{cases} . \quad (3\text{-}5)$$

When Φ is equal to 0, (3-4) and (3-5) indicate the power in State 2 is equal to the power in State 1, which means Φ=0 is the boundary condition between State 2 and State 1. In State 1, with Φ decreasing, the power also decreases. In (3-5), even when Φ turns



(a) (b)

Figure 3.9. Switching waveform of state2 (DPS): (a) design waveform; (b) experiment waveform @ input voltage 700V, output voltage 200 and 8kW.



(a) (b)

Figure 3.10. Switching waveform of state1(DPS): (a) simulation waveform; (b) experiment waveform @ input voltage 700V, output voltage 200 and 4kW.

negative, power can still be positive.

State 0: When the absolute values of i_0 and i_1 are equal to I_r, TPS can take over. There will be an inner phase shift on both sides. i_0 is fixed at I_r. i_1 is fixed at $-I_r$. The primary and secondary side switches can all realize ZVS. All the phase shifts in Figure 3.11 are presented in (3-6).

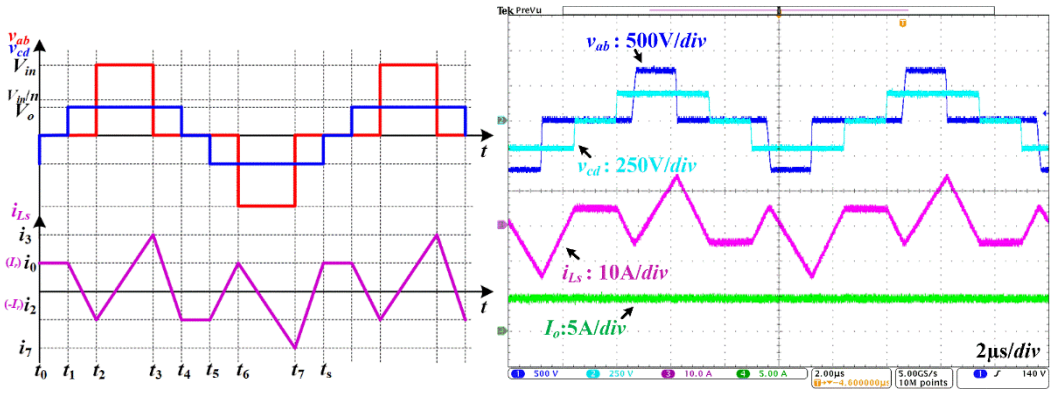
Relationships between transformer current and different time intervals are shown in (3-7).

$$\begin{cases} \phi = \dfrac{t_0 - t_2}{T_s / 2} \\ \phi_p = \dfrac{t_3 - t_2}{T_s / 2} \\ \phi_s = \dfrac{t_5 - t_2}{T_s / 2} \end{cases}. \tag{3-6}$$

$$\begin{cases} 2I_r = \dfrac{nV_o}{2L_s f_s} \dfrac{t_2 - t_1}{T_s / 2} \\ \dfrac{V_{in} - nV_o}{2L_s f_s} \dfrac{t_3 - t_2}{T_s / 2} = \dfrac{nV_o}{2L_s f_s} \dfrac{t_4 - t_3}{T_s / 2} \\ t_5 - t_1 = T_s / 2 \end{cases}. \tag{3-7}$$

Based on (3-6) and (3-7), the primary side inner phase shift and secondary side phase shift are

$$\begin{cases} \phi_p = \dfrac{nV_o(1+\phi)}{V_{in}} \\ \phi_s = 1 - \dfrac{4L_s f_s I_r}{nV_o} \\ P = \left(\dfrac{(V_{in} - nV_o)(1+\phi)nV_o}{4L_s f_s V_{in}} - I_r\right)(1+\phi)nV_o \end{cases}. \tag{3-8}$$



(a) (b)

Figure 3.11. Switching waveform of state0 (TPS): (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 200 and 1kW.

The phase shifts under no-load conditions can be estimated by using the power equation in (3-8).

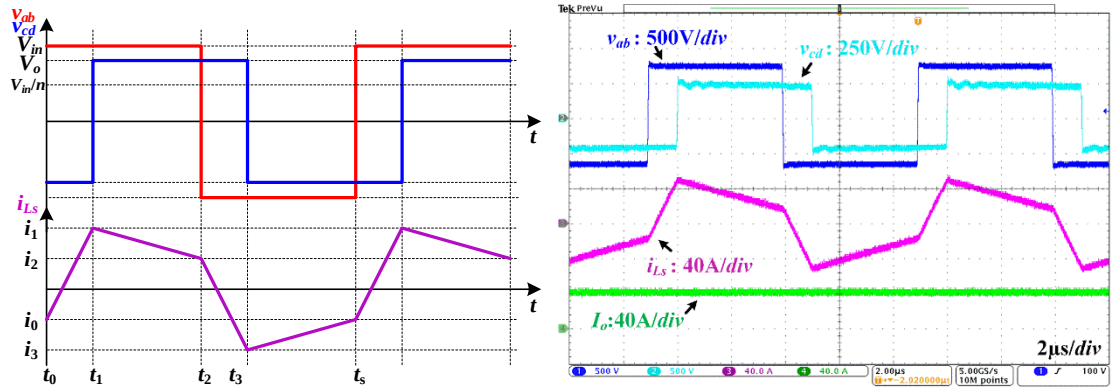
3.3.2 Switching modes when $V_{in} < nV_o$

Once the reflected battery voltage is greater than the DC-link voltage, the peak current will appear when secondary-side switches turn off. Note that the current shown in the figures is the primary-side current. The secondary-side switching-off current should be n times larger. Figure 3.12 describes SPS control.

State 5: When the power is lower, DPS takes over to secure ZVS which introduces Φ_s. The leakage inductance current i_0 is fixed at I_r to maintain the primary-side ZVS and i_1 begins to decrease, as shown in Figure 3.13. With fixed i_0, Φ_s in (3-9) can be derived based on Φ, as shown below. Note that even though (3-9) is complicated, Φ and power change monotonously in a certain range.

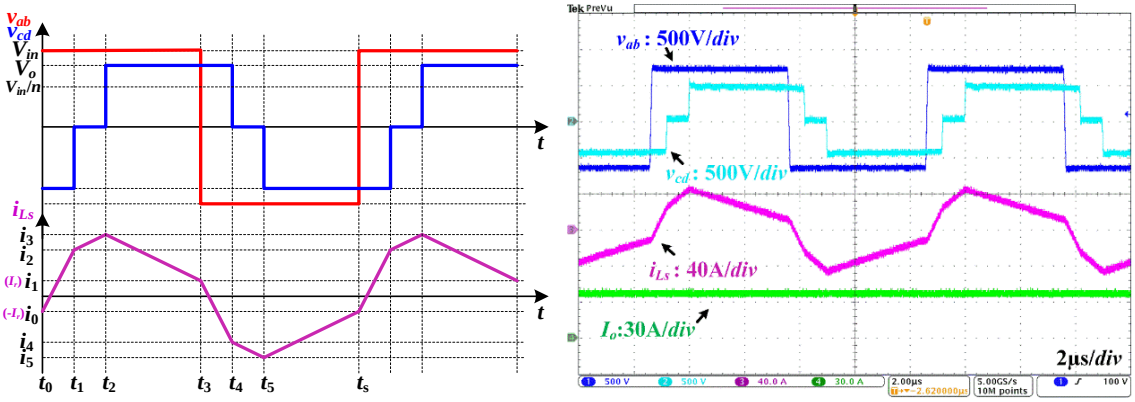
$$\begin{cases} \phi_p = 1 \\ \phi_s = \dfrac{4L_s f_s I_r - V_{in}}{nV_o} + 2 - \phi \\ P = \phi n V_o I_r - \dfrac{\phi^2 n V_o (V_{in} - nV_o)}{4L_s f_s} + nV_o (I_r - \dfrac{(V_{in} - nV_o)x}{4L_s f_s})x \\ x = \dfrac{V_{in} - 4L_s f_s I_r}{nV_o} + \phi \end{cases} . \quad (3\text{-}9)$$

State 6: When i_1 decreases to I_r, i_0 begins to increase, as shown in Figure 3.14 until they are both equal to 0 when Φ=0. In this state, half of the primary-side and secondary-side switches can realize QZVS. The absolute values of i_0 and i_1 are the same. By assuming i_0 is equal to $-i_1$, the value of i_0 and i_1 can be derived based on Φ. Then the primary-side



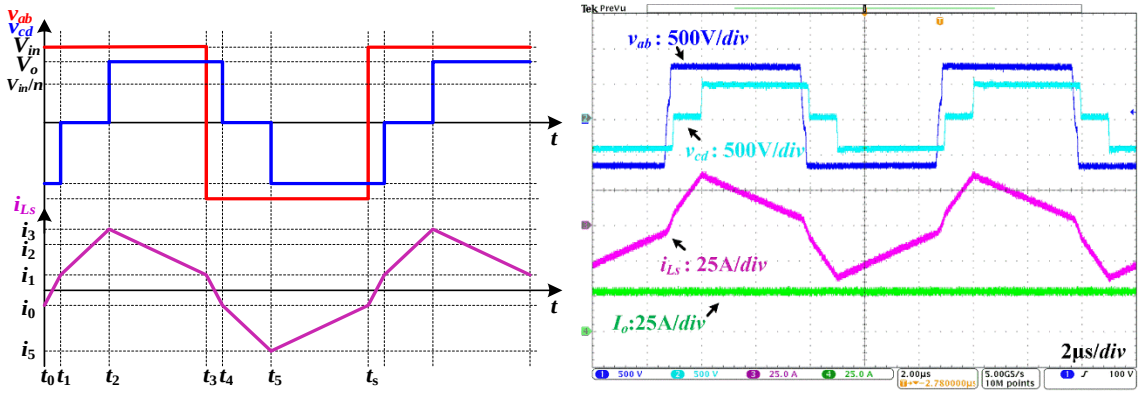
(a) (b)

Figure 3.12. Switching waveform of state4, SPS: (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 450V, and 20kW.



(a) (b)

Figure 3.13. Switching waveform of state5, DPS: (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 450V and 17kW.



(a) (b)

Figure 3.14. Switching waveform of state6, DPS: (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 450V, and 12.6kW.

inner phase shift Φ_s can be derived in (3-10) for the symmetry of the transformer current.

$$\begin{cases} \phi_p = 1 \\ \phi_s = 2 - \dfrac{V_{in}(1-\phi)}{nV_o} \\ P = \dfrac{(V_{in} - nV_o)\phi nV_0 + V_{in}(1-\phi)(nV_o - V_{in})}{4L_s f_s nV_o}(1-\phi)V_{in} \end{cases} . \quad (3\text{-}10)$$

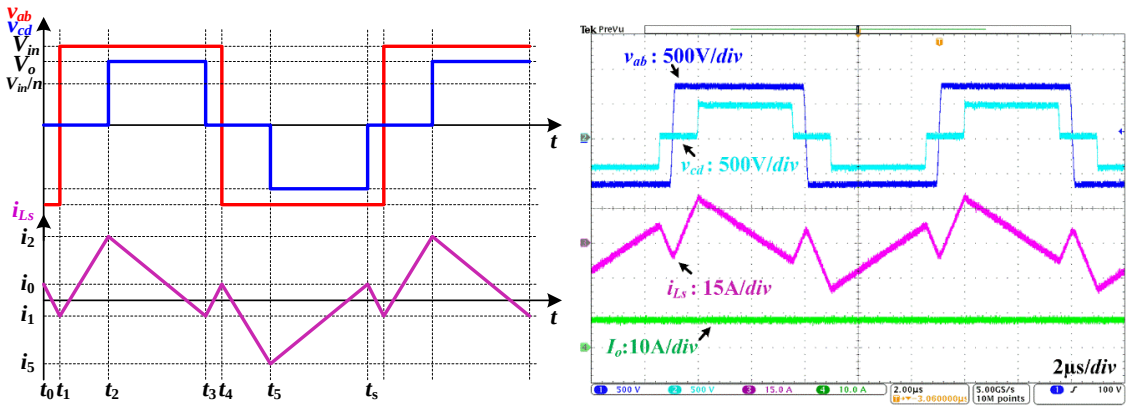
State 7: i_0 continues increasing with i_1 decreasing, as shown in Figure 3.15. Their absolute values are still the same. Half of the switches can realize QZVS. The derivation of i_0, i_1, and Φ_s is shown in (3-11).

$$\begin{cases} \phi_p = 1 \\ \phi_s = \dfrac{nV_o(2+\phi) - V_{in}(1+\phi)}{nV_o} \\ P = \dfrac{(2\phi+1)nV_o - (1+\phi)V_{in}}{4L_s f_s} \cdot \dfrac{(1+\phi)V_{in}^2}{nV_o} \end{cases} . \quad (3\text{-}11)$$

When $\Phi = 0$, the power is equal to that in State 7, which means $\Phi=0$ is the boundary condition between State 6 and State 7. In State 7, Φ is a negative value, but the power is still positive. Again, note that Φ is the phase shift between P_1 and S_1, not necessarily meaning the phase shift between primary voltage and secondary voltage.

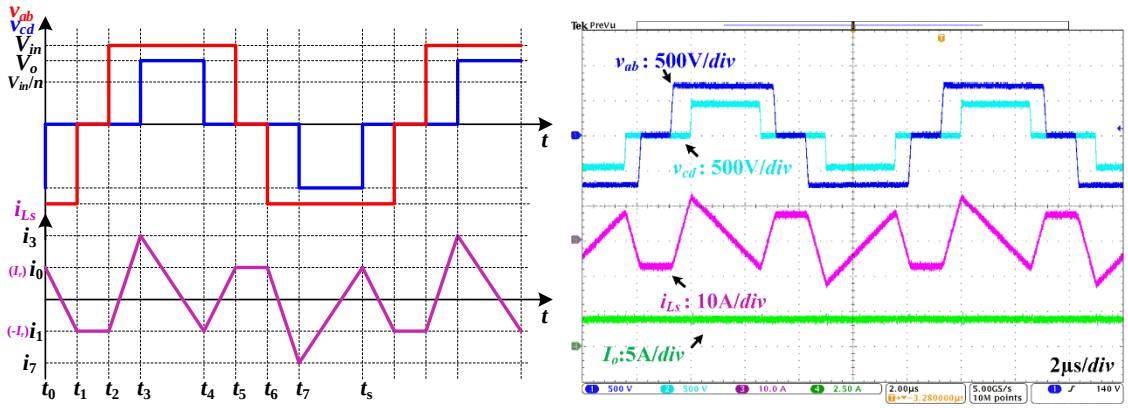
State 8: When the absolute values of i_0 and i_1 are equal to I_r, TPS can take over. Both are fixed at I_r. Φ_p begins to decrease, as shown in Figure 3.16. All switches can realize ZVS. All phase shifts are presented in (3-12).

Relationships between transformer current and different time intervals are shown in (3-13).



(a) (b)

Figure 3.15. Switching waveform of state7, DPS: (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 450V, and 4kW.



(a) (b)

Figure 3.16. Switching waveform of state8, TPS: (a) simulation waveform; (b) experimental waveform @ input voltage 700V, output voltage 450V and 1.8kW.

According to (3-12) and (3-13), relationships between the different phase shifts are (3-14).

$$\begin{cases} \phi = \dfrac{t_2 - t_0}{T_s / 2} \\ \phi_p = \dfrac{t_5 - t_2}{T_s / 2} \\ \phi_s = \dfrac{t_7 - t_2}{T_s / 2} \end{cases}. \tag{3-12}$$

$$\begin{cases} 2I_r = \dfrac{V_{in}}{2L_s f_s} \dfrac{t_1 - t_2}{T_s / 2} \\ \dfrac{V_{in}}{2L_s f_s} \dfrac{t_3 - t_2}{T_s / 2} = \dfrac{nV_o - V_{in}}{2L_s f_s} \dfrac{t_4 - t_3}{T_s / 2} \\ t_7 - t_3 = T_s / 2 \end{cases}. \tag{3-13}$$

$$\begin{cases} \phi_p = 1 + \phi + \dfrac{4L_s f_s I_r}{V_{in}} \\ \phi_s = \dfrac{nV_o(2+\phi) - V_{in}(1+\phi)}{nV_o} \\ P = \left(\dfrac{(nV_o - V_{in})(1+\phi)V_{in}}{4L_s f_s} - nV_o I_r\right) \dfrac{(1+\phi)V_{in}}{nV_o} \end{cases}. \tag{3-14}$$

In State 8, even at no load condition, ZVS can be realized.

In a summary, at heavy load and light load, all the switches can realize ZVS such as State 0, State 3, State 4, State 5, and State 8. At the medium load, all switches can only realize QZVS, which still imposes much less electric stress than pure hard switching on. None of the switches turn on when the drain-source current of switches is positive, which is helpful to relieve the stress on the switch gate and prevent the crosstalk between complementary switches.

3.4 Boundary Conditions and State Machine

Normally, the minimum ZVS current is related to the voltage across C_{oss}. The dead time should be long enough to make sure equivalent C_{oss} can be fully discharged by the inductor current. The energy-based analysis adopts a variable dead time, in which the dead time is just ended when the parasitic capacitance is fully discharged. However, since the system parameters may change with various influential factors, setting accurate dead time is rather complex. In real practice, a fixed dead time is often used, especially when a larger I_r to discharge the output capacitance of the switch faster is needed. This means that the ZVS process possibly can be finished before the end of dead time. In Figure 3.17 (b), P_1 turns on before the current of the inductor increases to 0, i.e., ZVS. In Figure 3.17 (a), either the dead time is the long or the initial absolute value of i_0 is small. First, C_{oss} is fully discharged, resulting in the current flowing through the body diode. Once the inductor current is greater than 0, C_{oss} will be recharged. The switch P_1 then turns on when $i_{Ls} > 0$, which means switch P_1 realizes QZVS. Figure 3.18 shows the experimental result demonstrating the dead-time effect.

In the proposed control strategy, State 0, State 3, State4, State 5, and State 8 must fully realize ZVS. The proper boundary conditions must consider this dead-time effect.

First, the dead time will be decided. To realize the ZVS process it must be no less than one-fourth of resonant time based on the minimum ZVS current [60, 141], i.e.,

$$t_{rmax} = \frac{\pi\sqrt{L_s C_{oss.eq}}}{2}. \tag{3-15}$$

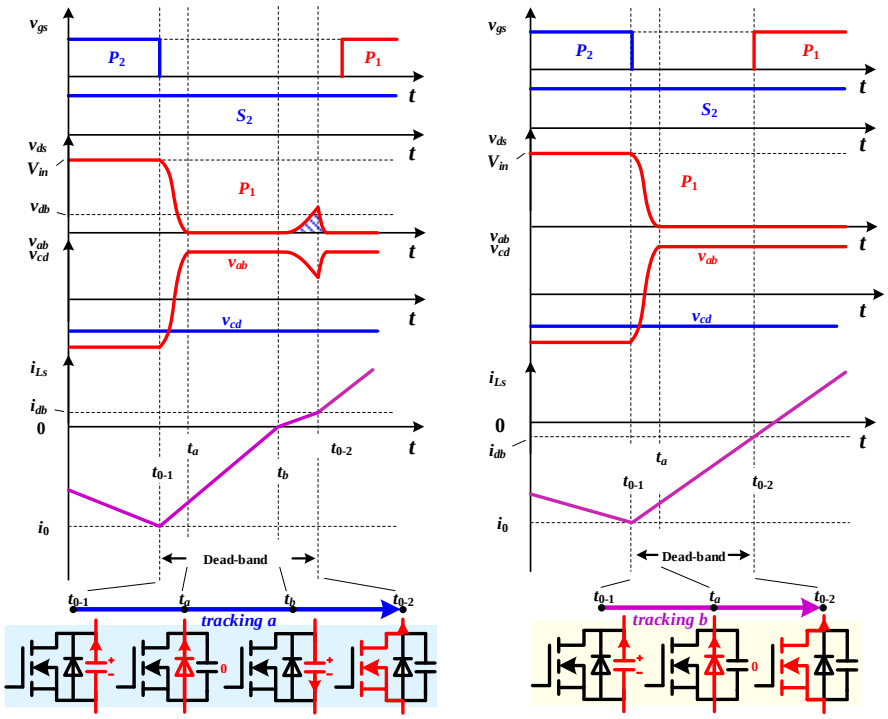


Figure 3.17. Long-dead-time effect: (a) with dead-time effect; (b) without dead-time effect.

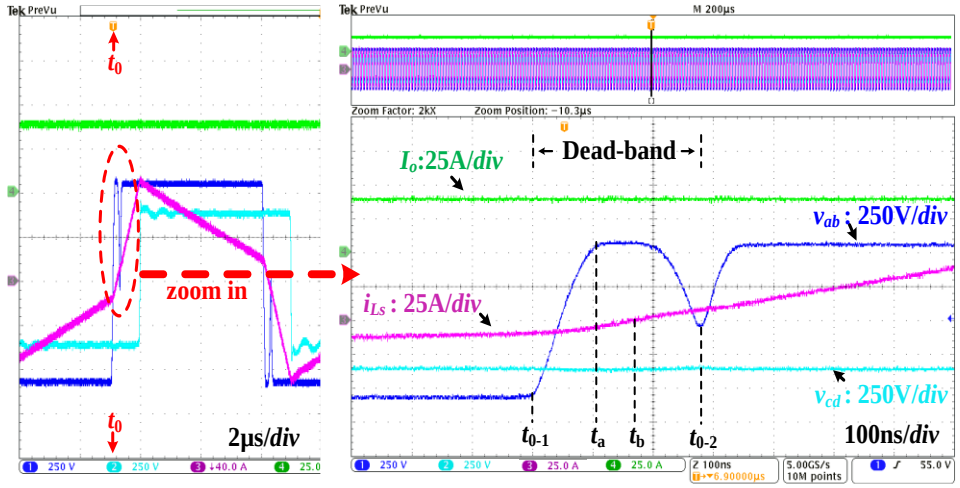


Figure 3.18. Dead-time effect (experiment).

Also, consider a small margin for the dead time,

$$t_{db} = t_{rmax} + t_{margin} . \tag{3-16}$$

According to the parameters of the switches used in this paper, 230ns is an appropriate value for dead time t_{db}. The boundary current is shown as the purple line in Figure 3.19, which decays to 0 at the end of the dead time. The current $i_{0\text{-}1}$ is then the boundary value to avoid the negative impact of the fixed dead time and is composed of resonant current Δi_r (energy-based ZVS current) and linear changing current Δi_l.

$$i_{0-1} = \Delta i_r + \Delta i_l = \Delta i_r + \frac{V_{in} + nV_o}{L_s}(t_{db} - t_r) . \tag{3-17}$$

Δi_r is derived from (1) and Δi_l is derived from trigonometry in [141, 142]. In Figure 3.19, the inductor voltage v_{Ls} is always smaller than $V_{in}+nV_o$, which means Δi_r is smaller than Δi_{r1}, as shown in (3-18)(3-19)(3-20).

$$L_s \frac{di_{Ls}}{dt} < V_{in} + nV_o . \tag{3-18}$$

$$\int_{t_{0-1}}^{t_a} di_{Ls} < \int_{t_{0-1}}^{t_a} \frac{V_{in} + nV_o}{L_s} dt . \tag{3-19}$$

$$\Delta i_r < \frac{V_{in} + nV_o}{L_s} t_r = \Delta i_{r1} . \tag{3-20}$$

Combining (3-17) and (3-20),

$$i_{0-1} < \frac{V_{in} + nV_o}{L_s} t_{db} . \tag{3-21}$$

I_{r1} is a simplified value for $i_{0\text{-}1}$, which also has a small margin to avoid the fixed dead-time effect.

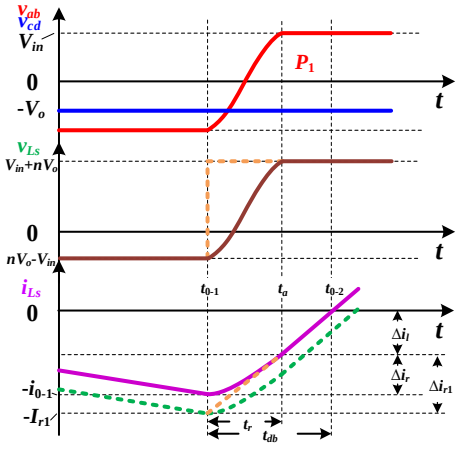


Figure 3.19. Setting the boundary current based on dead time.

For the boundary of State 3 and State 4 and the boundary of State 4 and State 5,

$$I_{r1} = \frac{(V_{in} + nV_o)t_{db}}{L_s}. \tag{3-22}$$

Note that this is the boundary current for certain operation states. The boundary of State 0 and State 1 is

$$I_{r2} = \frac{nV_o t_{db}}{L_s}. \tag{3-23}$$

For the boundary of State 7 and State 8, the current is related to the DC-link voltage instead of the battery voltage, i.e.,

$$I_{r3} = \frac{V_{in} t_{db}}{L_s}. \tag{3-24}$$

Based on the analysis above, the charging profile can be divided into 9 parts as shown in Figure 3.20. I_{r1}, $I_{r2,}$ and I_{r3} are the minimum current to realize ZVS when using a fixed dead time. Such current is usually slightly larger than the energy-based ZVS current. For the EV battery charger, there will be no abrupt change in the battery voltage. The output power will change rather slowly, making the fast-dynamic response for a battery charger less desired. However, smoothly switching among the nine states above must be addressed. In the proposed control strategy, a state machine is used to help switch from one state to the other, as shown in Figure 3.21. In the last section, the relationship between Φ and power (P) in each state has been formulated. The phase shift will be used to decide operation conditions (Cd1~10). Boundary conditions represented by Φ are listed in Table 3.2.

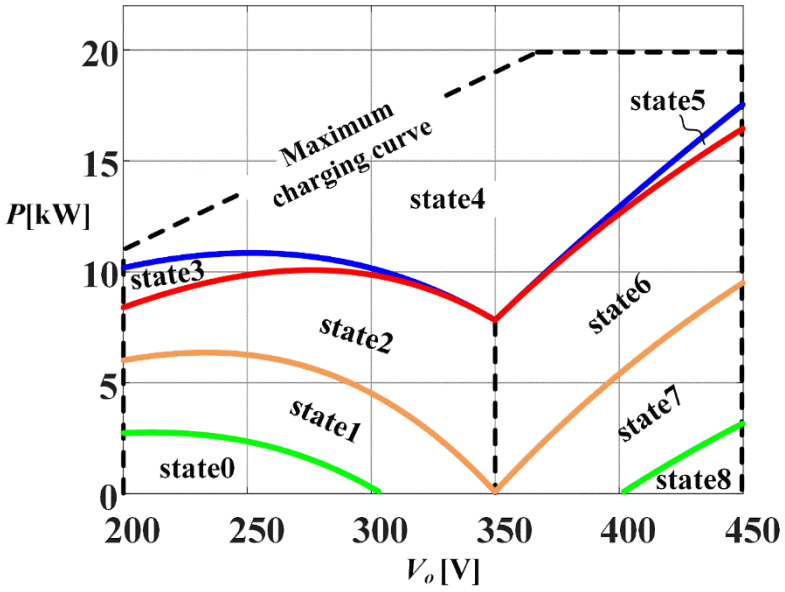


Figure 3.20. Battery charging curve and related operational states.

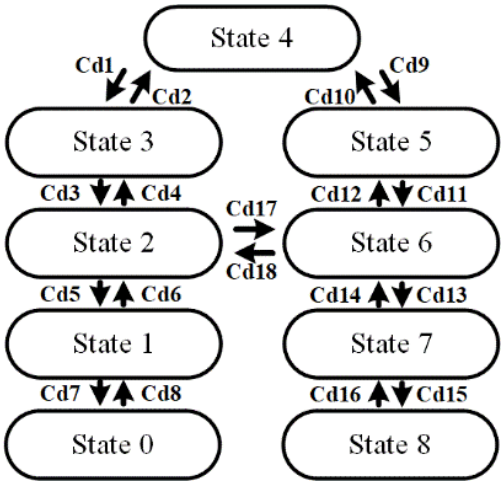


Figure 3.21. Connections among different states.

Table 3.2. Boundary Conditions.

#	Equation	#	Equation
Cd1	$\phi < \frac{2L_s f_s I_{r1} - nV_o + V_{in}}{2V_{in}}$	Cd10	$\phi \le \frac{2L_s f_s I_{r1} + nV_o - V_{in}}{nV_o}$
Cd2	$\phi \ge \frac{2L_s f_s I_{r1} - nV_o + V_{in}}{2V_{in}}$	Cd11	$\phi < \frac{4L_s f_s I_{r1}}{V_{in} + nV_o}$
Cd3	$\phi > \frac{4L_s f_s I_{r1}}{V_{in} + nV_o}$	Cd12	$\phi \ge \frac{4L_s f_s I_{r1}}{V_{in} + nV_o}$
Cd4	$\phi \le \frac{4L_s f_s I_{r1}}{V_{in} + nV_o}$	Cd13	$\phi < 0$
Cd5	$\phi < 0$	Cd14	$\phi \ge 0$
Cd6	$\phi \ge 0$	Cd15	$\phi < -\frac{4L_s f_s I_{r3}}{V_{in}}$
Cd7	$\phi \le -\frac{4L_s f_s I_{r2}}{nV_o}$	Cd16	$\phi \ge -\frac{4L_s f_s I_{r3}}{V_{in}}$
Cd8	$\phi \ge -\frac{4L_s f_s I_{r2}}{nV_o}$	Cd17	$V_{in} < nV_o$
Cd9	$\phi < \frac{2L_s f_s I_{r1} + nV_o - V_{in}}{2nV_o}$	Cd18	$V_{in} \ge nV_o$

Figure 3.22 shows that all three-phase shifts are changing continually within the full-power range, which means the transition among states is smooth.

3.5 Charger Utility Control

3.5.1 Pre-charge Mode

For a battery charger, the output capacitors should be pre-charged to the battery voltage before turning on the output relay and beginning the charging cycle. With the proposed control algorithm able to cover all power ranges, the pre-charge process can be realized by the DAB operated at the nearly no-load condition. With the closed-loop voltage control, the reference voltage should gradually increase to the battery voltage. This transition process is shown in Figure 3.23. To simplify the analysis and ensure ZVS performance, when the output voltage is lower than 200V, ZVS current I_{r2} is fixed at a constant value to make sure primary side switches can realize ZVS.

The sequence of the pre-charge mode should be State1, 0, 1, 7, and 8, as illustrated in the red line in Figure 3.23. In the very beginning, because the output voltage is 0 while the DC-link voltage is 700V, the primary-side voltage will be a narrow pulse and the secondary side voltage will be a square waveform, as shown in Figure 3.24. This prevents the leakage inductance current from damaging switches.

3.5.2 Grid to Vehicle (G2V) and Vehicle to Grid (V2G) Modes

In the G2V mode, the whole charging process at the DAB stage is: (1) the output capacitors should be pre-charged before connected to the battery; (2) ramping up the output

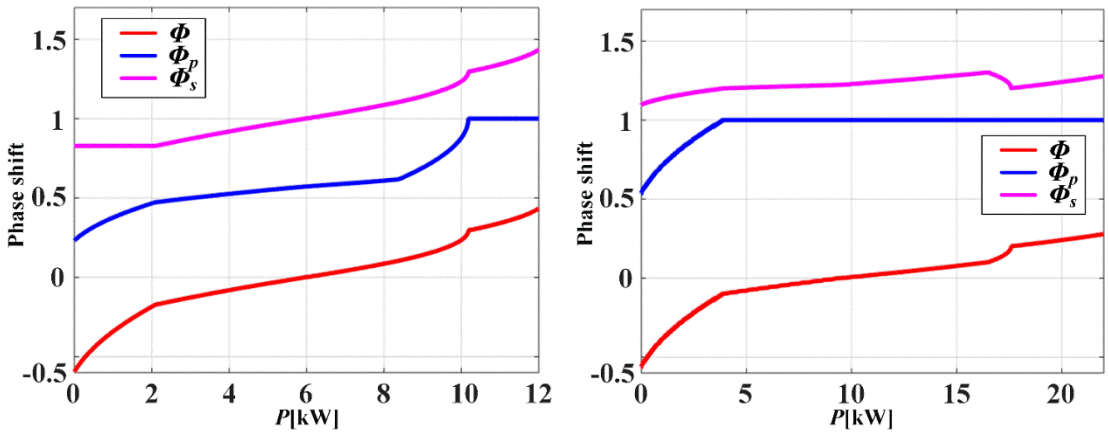


Figure 3.22

(a) (b)

Figure 3.22. Different phase shifts vs Power: (a) V_o 200V; (b) V_o 450V.

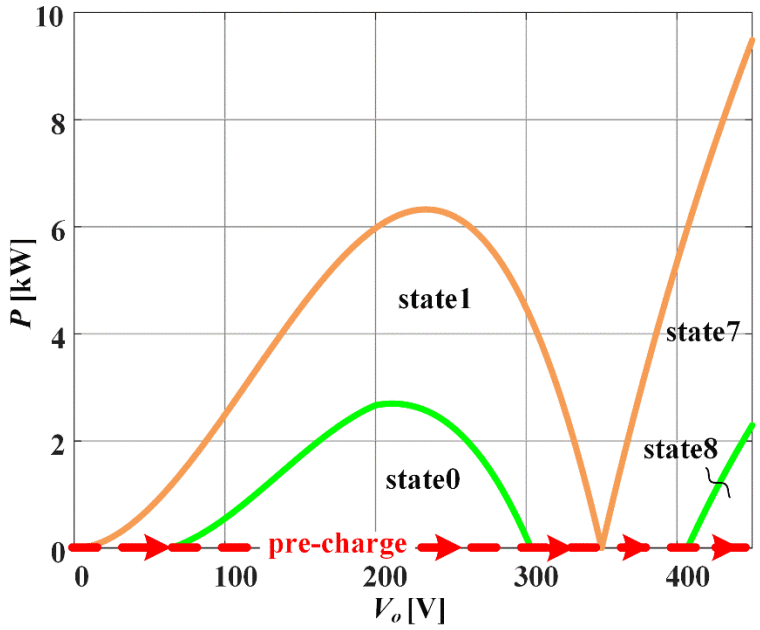


Figure 3.23. Pre-charge process.

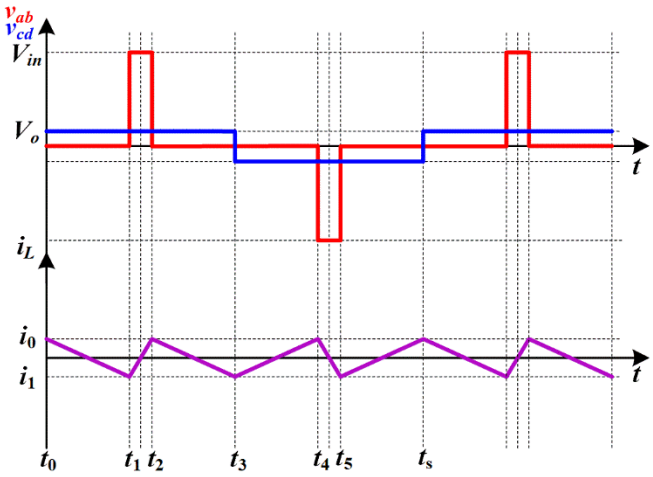


Figure 3.24. Switching performance at the beginning of the pre-charge mode.

current and then using a constant current to charge the battery; (3) entering constant power charging process; (4) finishing in constant voltage charging. When the MCU of the charger receives the charging command, the charger should switch to the corresponding charging mode smoothly.

The proposed charging control algorithm is shown in Figure 3.25. Note different operation modes have their own PI controllers with different parameters. To realize transitions smoothly between different operation modes, PI controllers should communicate and share the value of integral with each other in every interrupt period. For instance, in one interrupt period, the charger operates in the CC mode, while in the next period it needs to switch to CP mode. The MCU then assigns the output values of the integrator as

$$integral_{power} = integral_{voltage} = integral_{current} . \tag{3-25}$$

Assume the PI controller tracks the reference current. The $error_{current}$ is then equal to 0 in the steady-state.

$$\phi = K_{pcurrent} error_{current} + integral_{current} . \tag{3-26}$$

In the next period, the output of the constant-power-mode PI controller needs to be equal to

$$\phi = K_{ppower} error_{power} + integral_{power} . \tag{3-27}$$

If the reference power is changing continuously, the $error_{power}$ should be 0 and the phase shifts will be considered the same as the last value.

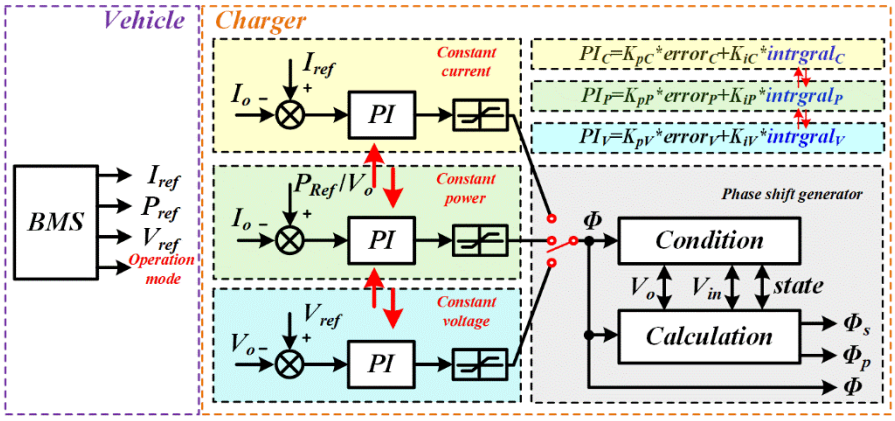


Figure 3.25. Control algorithm of G2V mode.

The charger can then transition smoothly among different charging modes in real time.

As a part of an energy storage system with bidirectional capability, the DAB-based battery charger should also have the ability to deliver the power back to the grid. Conventional SPS control only uses one phase shift, making G2V and V2G operations totally symmetric. The analysis here shows the operation states of the proposed control strategy are also symmetric, as shown in Figure 3.26.

Here we particularly focus on the transition between V2G and G2V modes, as shown in Figure 3.26. The pink curve is under no-load condition and the absolute values of each switching point are all fixed at I_{r2}. The average current in half switching period is Figure 3.27. Here we define the G2V mode as the positive direction of power flow, with the green curve indicating its leakage inductor current. The primary-side phase shift and the phase shift between secondary-side legs are both shrinking during the transition. The primary-side transformer voltage leads the secondary side. The current at t_2 increases, which means the equivalent current in the half period increases with the positive power. The orange curve shows the light-load V2G mode. Here, the primary-side voltage falls behind the secondary side. The current at t_1 decreases, which means the average current in the half period decreases, corresponding to a negative power. G2V and V2G modes can naturally switch within one switching period. It is worth pointing out that in the G2V mode, the phase shift between switch P_1 and S_1 is the reference. This is decided by the PI controller while other phase shifts are calculated based on it, given that the relation between power and phase shift Φ is monotonic. In the V2G mode, the phase shift between P_3 and S_3 is

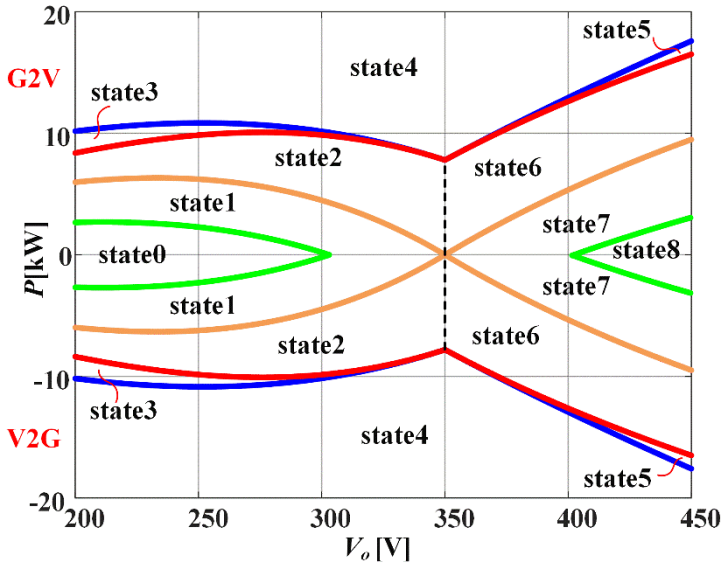


Figure 3.26. G2V and V2G modes.

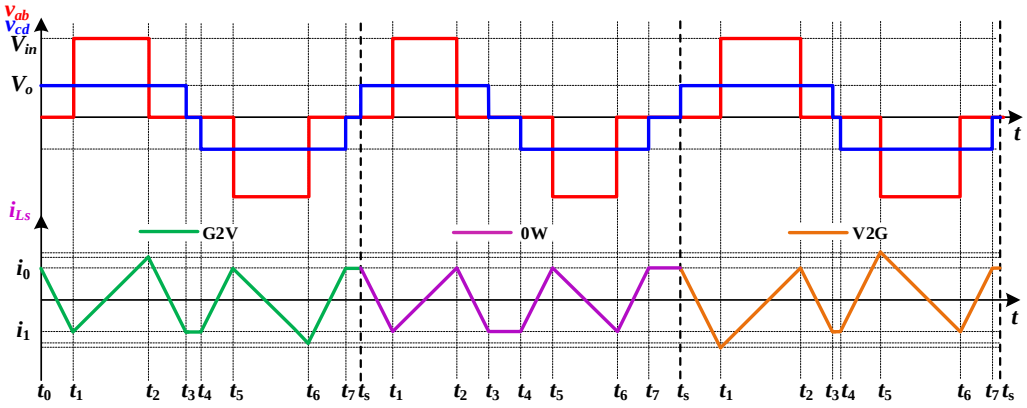


Figure 3.27. Switching modes boundary between G2V and V2G.

then considered as the reference phase shift.

3.6 Experimental Verification

To validate the proposed smooth transition discussed above, the constant current load test is shown in Figure 3.28. Based on closed-loop current control, the reference current increases from 0 to 55A when the output voltage is 200V. With the power increasing, the switching modes transition from State 0 to State 4, and the transformer peak current also increases gradually. The transition process can be treated as the combination of multiple steady-state tests. Both the transformer peak current and output voltage indicate smooth transitions.

Also, a 10Ω resistive load test is adopted to validate the smooth transition between different modulation strategies, which is shown in Figure 3.29. The voltage closed-loop control is used to make sure the output voltage increases linearly. The modulation strategies start with DPS control. When the reflected output voltage is lower than the input voltage, with the increase of the output voltage, the switching modes transition from State 1 to State 2. Then, when the reflected output voltage is higher than the input voltage, the switching modes transition from State 2 to State 6. The transition process from 0V to 450V is then realized seamlessly.

The pre-charge experiment is shown in Figure 3.30. With the closed-loop voltage control, the reference of the output voltage increases gradually. Here, the transformer current reflects different switching modes. At the beginning of the pre-charge process, the current increases from 0 in State 1. Once switched to State 0, the transformer peak current should

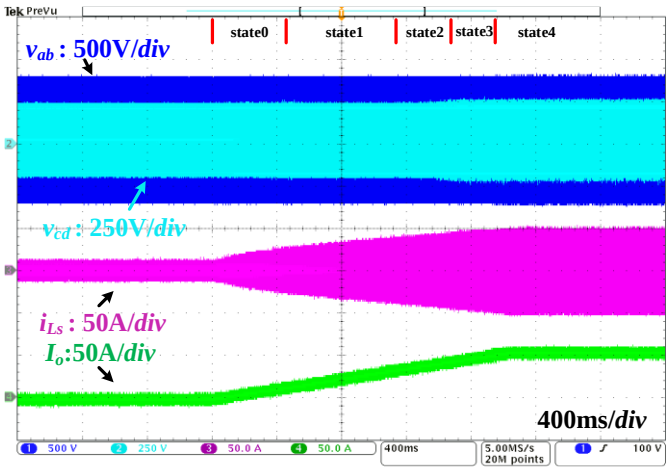


Figure 3.28. 200V constant voltage source load to validate the smooth transitions between different modulation strategies.

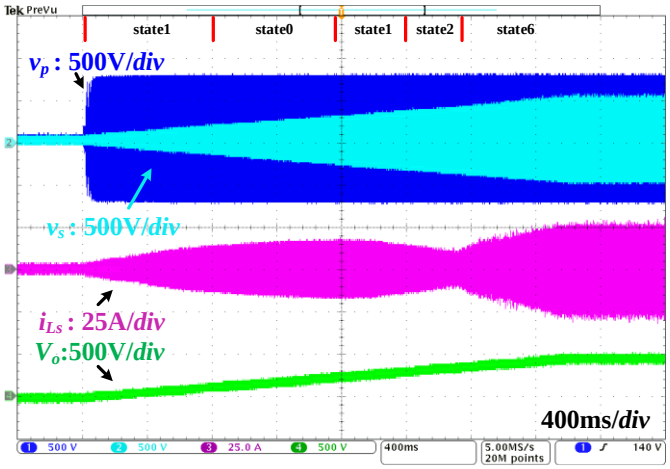


Figure 3.29 10Ω resistive load to validate the smooth transition between different modulation strategies.

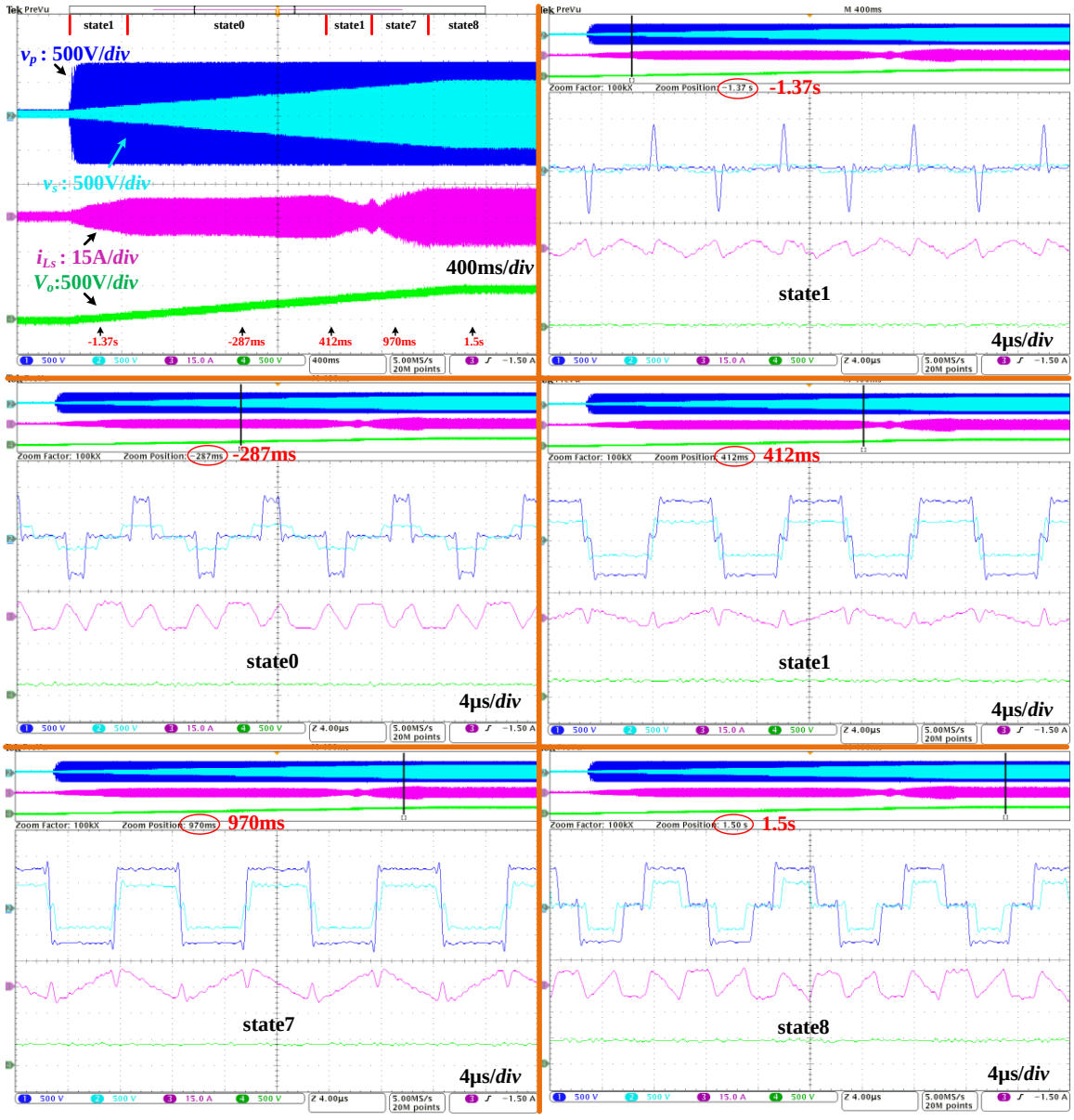


Figure 3.30. Pre-charge mode with zoom-in waveforms.

be equal to I_{r1}. The next state is State 1 and the maximum current decreases. There is a small oscillation when the output voltage is ~350V, i.e., half of the DC-link voltage. Around that point, the current is close to zero with the DAB entering the SPS control. Note such a small oscillation does not influence the pre-charge process or bring any inrush current. When switched to State 7, the maximum transformer current increases quickly until reaching State 8, when the maximum current is equal to I_{r2}. In the pre-charge mode, the transition process is smooth even going through several states. With the current closed-loop control, the reference current is 0 and the output voltage increases gradually.

In Figure 3.31Figure 3.32, a transition test between V2G and G2V modes at 200V is provided. The discharging current from -10A decreases to 0 and the charging current increases from 0 to 10A gradually.

To verify the smooth transition between different operational modes, the experiment is carried out under a lower voltage and current rating in Figure 3.32. The load comprises a resistor and a voltage source. The DAB converter and the output voltage provide the energy to the resistor at the same time. At first, under the current control mode, the output current increases linearly. When switched to the voltage control mode, the output voltage source is slightly higher than the reference voltage, making the output current decrease. Finally, after switching back to the current control, even if the output voltage source changes the voltage, the DAB converter can still keep the output current.

3.7 Conclusion

Considering the cost of the EV charger, the most affordable SiC MOSFETs are used,

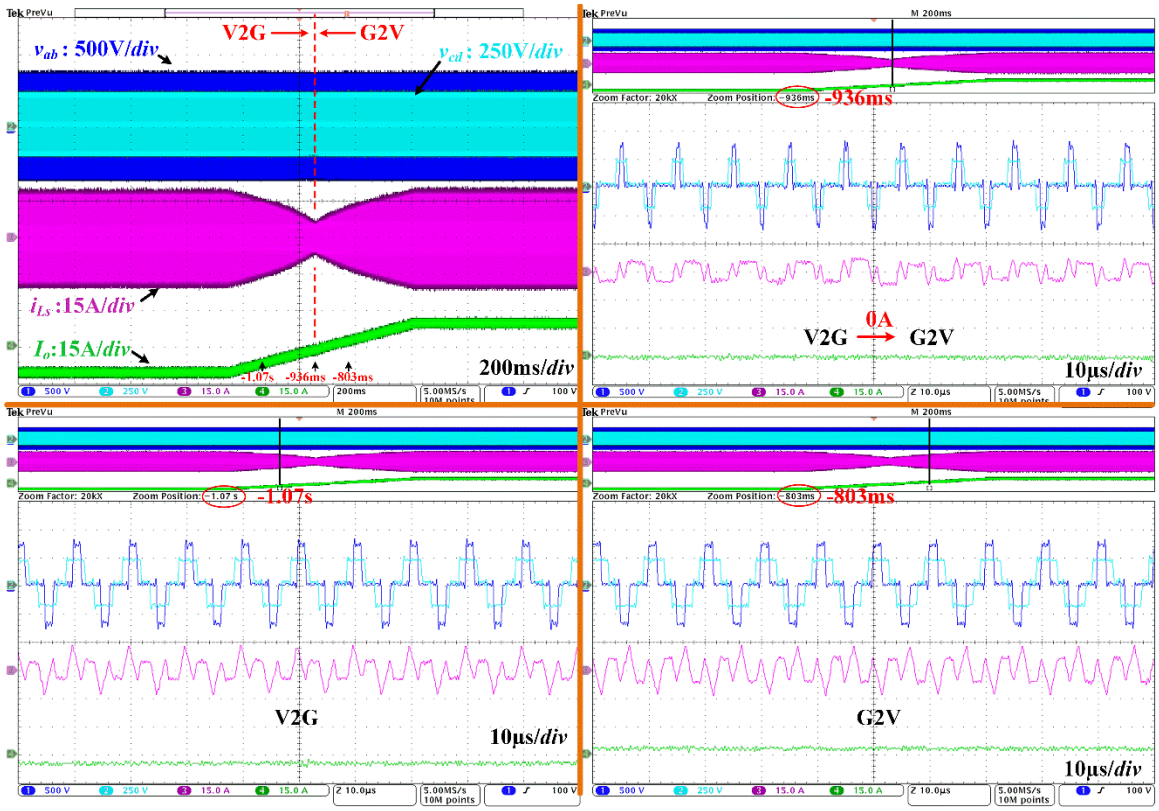
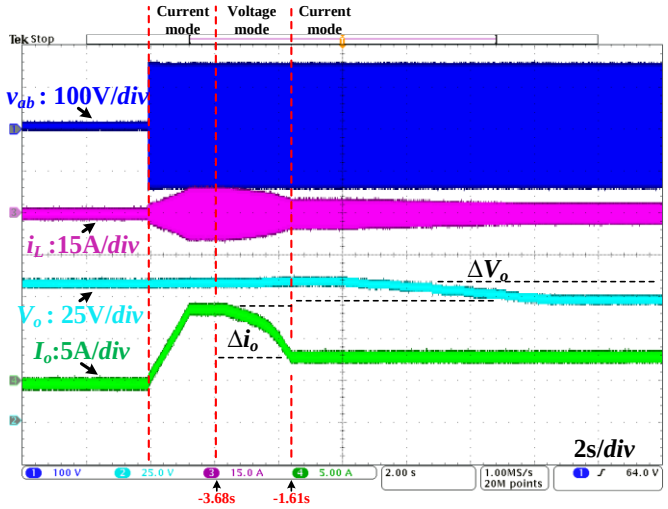
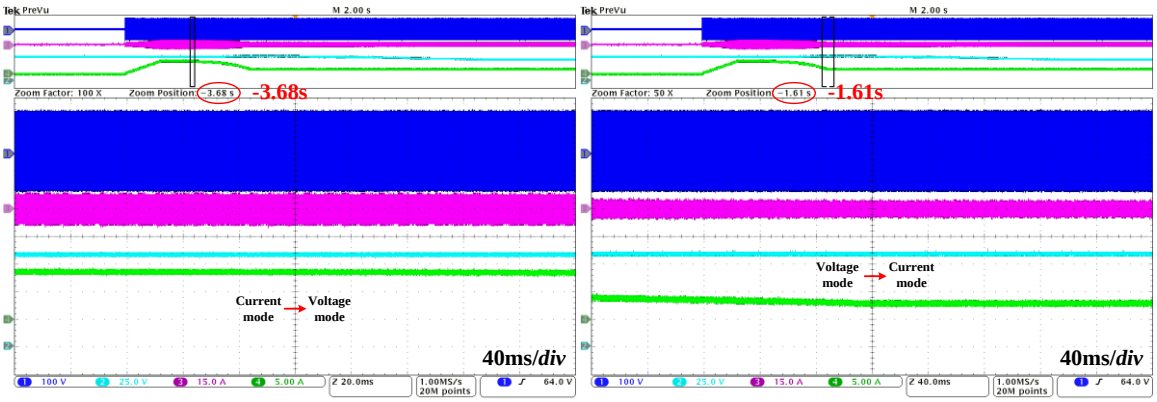


Figure 3.31. Transition test between V2G and G2V from -10A to +10A with zoom-in waveforms.



(a)



(c) (d)

Figure 3.32. Transition between current control mode and voltage control mode: (a) overall waveform; (b) transition from current control mode to voltage control mode; (c) transition from voltage control mode to current control mode.

which however are more sensitive to the crosstalk, increasing the need for ZVS operation to avoid the shoot through. This chapter is pertinent to the real operating conditions of a battery charger and includes the tests of several transition processes to verify the practicability of the proposed MPS modulation. Such control provides a significant payback, i.e., using the most affordable SiC for the hardware and enhancing the reliability with the software control, promoting the SiC and DAB application in EV chargers, and addressing their challenges at the system level.

In this chapter, with a DAB-based 20kW off-board battery charger, the operation can be further divided into 8 states by using MPS modulation to secure better performance of the DAB converter. By utilizing DPS control and TPS control, DAB can realize ZVS even at zero loads when the input voltage and the output voltage are not matched. By applying inner phase shift into primary-side and secondary-side H-bridges, there are more control freedoms, and the power transfer could be more flexible. The boundary conditions and smooth transition between different modulation strategies are validated through the experiments.

Chapter 4 COMPLETE ZERO-VOLTAGE-SWITCHING ANALYSIS IN DUAL ACTIVE BRIDGE

To secure ZVS for all eight switches in DAB, previous literature mostly focuses on half-bridge to analyze switching transitions, which, however, is rather incomplete due to ignoring the impact of modulations strategies and cannot fulfill all circumstances. For example, in the last chapter, for each switch, the required ZVS current is different in different modulation strategies. In this chapter, the whole H-bridge is used as a unit to analyze the ZVS transient process, addressing the ZVS setting in different modulation strategies [143]. To analyze the detailed ZVS process during dead time, an H-bridge circuit is extracted out of DAB as shown in Figure 4.1, where V_{in} is the input voltage source and V_s is the reflected secondary-side voltage, which can be $+nV_o$, $-nV_o$, or 0 according to the secondary side modulation. Because of the symmetry of DAB structure, analyzing one side, say primary-side H-bridge is sufficient. The minimal initial inductor energy to complete the ZVS process is also quantified, which in return can reduce the transformer current thereby enhancing the efficiency. Furthermore, the accurate ZVS transition time is derived by incorporating the non-linearity of switch output capacitance, which can be further used to set the dead time.

4.1 Non-linear Capacitance of Switches

The ZVS process of one leg is shown in Figure 4.2 (a). In the transition process, C_{oss} of complementary switches gets charged and discharged simultaneously. The energy exchange during ZVS realization happens between the inductor, C_{oss}, input voltage source

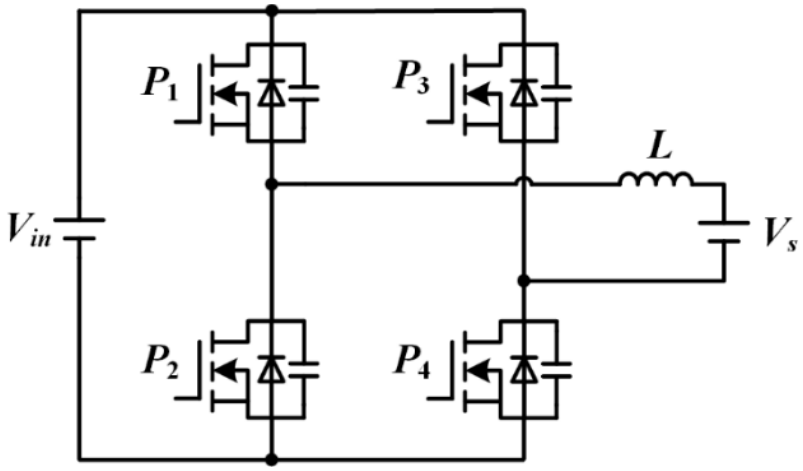


Figure 4.1. Simplified circuit for ZVS analysis based on H-bridge.

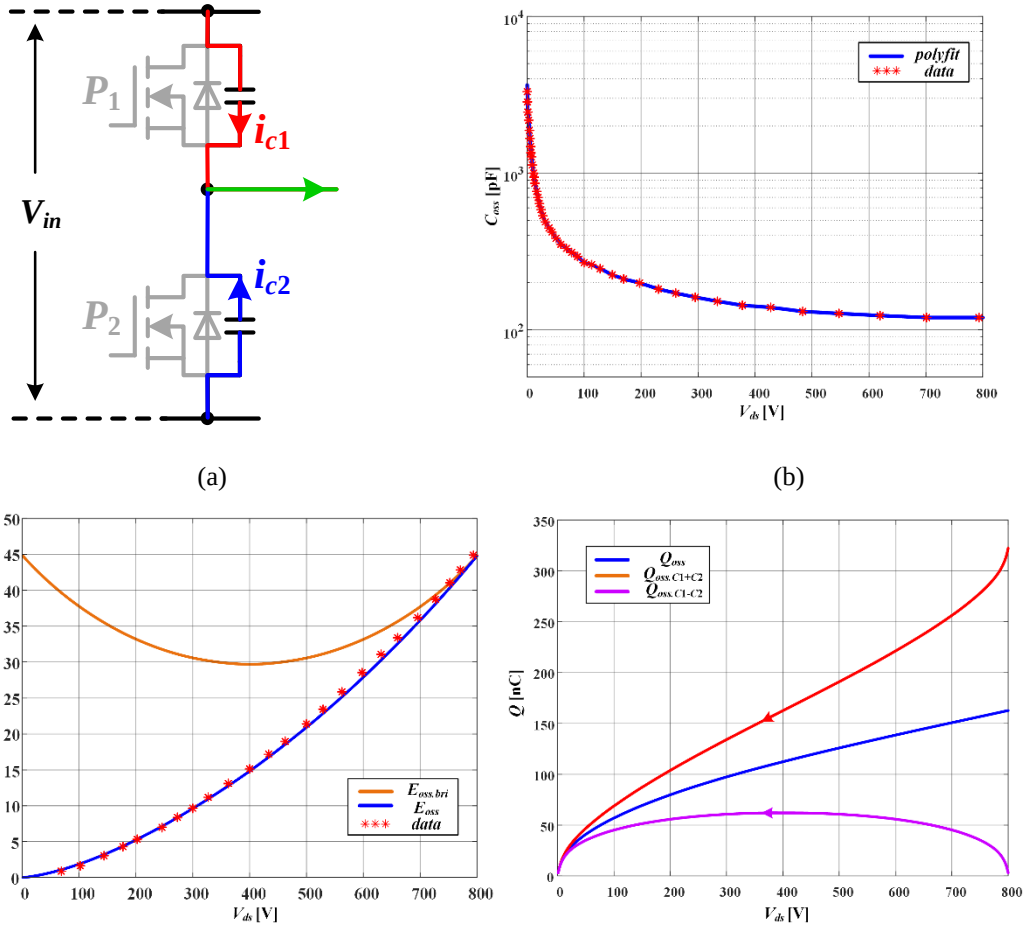


Figure 4.2. Characteristics of nonlinear output capacitance in one bridge leg: (a) ZVS transition; (b) C_{oss}; (c) E_{oss}; (d) Q_{oss}.

V_{in} and reflected output voltage source V_s. To quantify such exchanged energy accurately, the charge flowing through the inductor, the voltage sources, and the charge remaining in C_{oss} all need to be mathematically formulated.

Curve fitting is usually used by referring to data points from the switch datasheet. For instance, Figure 4.2 (b) shows C_{oss} created by the interpolant method using the original data points from the datasheet of SCT3030KL [144].

The E_{oss} curve is then calculated based on the C_{oss} curve, as shown in Figure 4.2 (c), which is compared with the data imported from the datasheet. This then allows us to calculate the stored energy of one leg in the ZVS process within the range of the 800V input voltage, as shown in the orange curve.

The charge stored in C_{oss} is shown by the blue curve in Figure 4.2 (d), which is calculated based on the C_{oss} curve. Note x-axis is V_{ds} of the bottom switch P_2. The charge flowing out/in the bridge middle point is the red curve in Figure 4.2 (d), which is the sum of the charge flowing through two switches. The difference between charges flowing through two switches is the purple curve. The data presented in Figure 4.2 (c) and (d) will then be utilized to estimate the ZVS process in the following sections.

Switch P_2 will be used as an example to analyze the ZVS process in different conditions. If the parasitic capacitance between drain and source is comparable with C_{oss}, it should be included when fitting the curve to ensure an accurate estimation.

4.2 Circuit Patterns

4.2.1 Modulation without Inner Phase Shift

Considering the primary H-bridge without inner phase shift, P_1 and P_4 switch on and off at the same time. In this case, C_{oss} of P_1 and P_4 are charged or discharged simultaneously with the same V_{ds} value. The input and output voltage sources, four switch capacitances, and the inductance all participate in the resonant process. However, the existing half-bridge analysis cannot describe the true resonant loop, leading to inaccurate calculation of minimal inductor energy. Figure 4.3 (a) illustrates the real ZVS transient process with the control scheme shown in Figure 4.3 (c)~(d). Time intervals in the shadow represent the transient in Figure 4.3 (a). The current flowing through switches is shown in Figure 4.3 (b).

Such a ZVS transient process happens when P_1 & P_4 are switched off while P_2 &P_3 are not on yet. In the beginning, the current flows out of the input voltage source, and V_{in} supplies the power for the ZVS process. But the polarity of the current is gradually reversed, indicating V_{in} begins to consume energy. Actually, the power supplied or dissipated by the input voltage source is 0, though such input voltage source influences the ZVS transition time, as derived below. Assuming the voltage across the output capacitance of P_1 is v, the relationship between the capacitance voltage and inductor current is shown in (4-1)(4-2).

$$\begin{cases} V_{in} = V_{C1}(t) + V_{C2}(t) \\ v = V_{C1}(t) \end{cases} \tag{4-1}$$

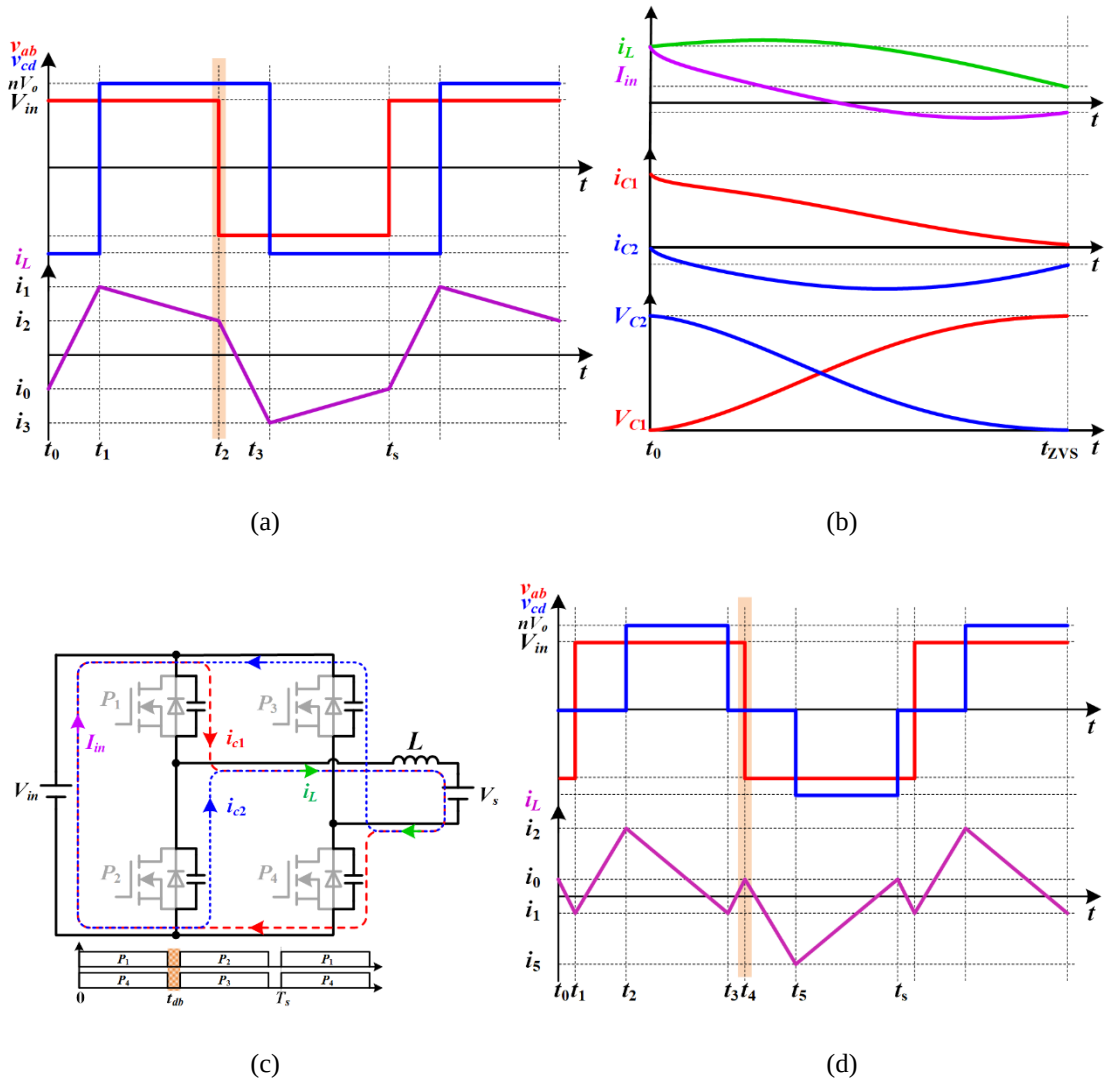


Figure 4.3. H-bridge ZVS transient process without the inner phase shift: (a) transient process; (b) transient process waveforms; (c) for SPS; (d) for DPS.

To get the power consumed by the voltage source in the circuit, the charge flowing through the inductor and DC source in the transient process is needed, which is

$$\begin{cases} i_{in}(v) = i_{C1}(v) - i_{C2}(V_{in} - v) \\ i_L(v) = i_{C1}(v) + i_{C2}(V_{in} - v) \\ i_{C1}(v) = C_1(v)\dfrac{dv}{dt} \\ i_{C2}(v) = -C_2(V_{in} - v)\dfrac{d(V_{in} - v)}{dt} \end{cases} \tag{4-2}$$

To get the power consumed by the voltage source in the circuit, the charge flowing through the inductor and DC source in the transient process is needed, which is

$$\begin{cases} Q_{i_L}(v) = \int_0^v (C_1(v) + C_2(V_{in} - v))dv \\ Q_{i_{in}}(v) = \int_0^v (C_1(v) - C_2(V_{in} - v))dv \end{cases} \tag{4-3}$$

So the energy dissipated in the input and the output voltage sources in the transient process is

$$E_{diss}(v) = -Q_{i_{in}}(v)V_{in} + Q_{i_L}(v)V_s \tag{4-4}$$

The total initial energy stored in the inductor and H-bridge is

$$E_{init} = \frac{1}{2}Li_L^2(0) + 2E_{oss.bri}(0)\,. \tag{4-5}$$

The remained energy in the H-bridge and inductor at the end of ZVS is

$$E(v) = \frac{1}{2}Li_L^2(v) + 2E_{oss.bri}(v) = E_{init} - E_{diss}(v)\,. \tag{4-6}$$

Combining (4-4) ~ (4-6), the inductor current can be derived based on the certain voltage, which is

$$i_L(v) = \sqrt{i_L^2(0) + \frac{2}{L}(2E_{oss.bri}(0) - 2E_{oss.bri}(v) - Q_{i_L}(v)V_s + Q_{i_{in}}(v)V_{in})}\,. \qquad (4\text{-}7)$$

For the ZVS transition time, we need to simplify (4-1)~ (4-2) to get the relationship between v and inductor current as

$$\frac{(C_1(v) + C_2(V_{in} - v))dv}{i_L(v)} = dt\,. \qquad (4\text{-}8)$$

Based on this (4-7), the inductor current can also be expressed as a function of v. In the transient process, the output capacitance of P_1 is charged. So v increases from 0 to V_{in}, and the transition time increases from 0 to t_{ZVS}. Then,

$$t_{ZVS} = \int_0^{t_{ZVS}} dt = \int_0^{V_{in}} \frac{(C_1(v) + C_2(V_{in} - v))}{i_L(v)}\,dv\,. \qquad (4\text{-}9)$$

In the whole transient process, the charge flowing through C_1 and C_2 are the same. According to (4-3), the total charge flows through the input voltage source is 0, as shown in (4-10).

$$\begin{cases} \int_0^{V_{in}} Q_{in}(v)dv = 0 \\ E_{oss.bri}(0) = E_{oss.bri}(V_{in}) \end{cases} \qquad (4\text{-}10)$$

Thus, the only energy exchange in the whole ZVS process without an inner phase happens between the inductor and the output voltage source. To complete the ZVS transient process, the minimum inductor energy is

$$\frac{1}{2}Li_L^2(0) \geq 2Q_{oss}(V_{in})V_s \qquad (4\text{-}11)$$

If a half-bridge is used to analyze the transient process, the input voltage source may also dissipate or supply power, which results in overestimation or underestimation of the required energy. To accurately estimate the ZVS transition time, the instantaneous capacitance of the H-bridge instead of a constant equivalent capacitance should be considered, along with the interaction with the input voltage source, even though V_{in} does not contribute any energy.

4.2.2 Modulation with Inner Phase Shift

When the voltage gain is far away from 1 or at light load, DAB can lose ZVS easily. Many modulation strategies [2,3] adopt the inner phase shift to extend the ZVS range, such as DPS, TPS, and MPS. These modulation strategies yield a three-level waveform with different ZVS settings. In this case, only two switch output capacitances participate in the resonant process. A switch in the other leg provides the bypass for the inductor current, which makes the current flowing through the input and the output voltage sources different. The resonant loop with inner phase shift is different from the loop discussed in Chapter III.

In Figure 4.4 (a) and (c), the ZVS transient processes for the lower switch P_2 happen with an inner phase shift added at the primary side. Figure 4.4 (e) and (f) show the related waveforms. Figure 4.4 (a) corresponds to $t=t_2$ in Figure 4.4 (e) and (f). Figure 4.4 (c) is for $t=t_3$ in Figure 4.4 (e) and $t=t_4$ in Figure 4.4 (f). In Figure 4.4 (a), the current flowing through the input voltage source is the same as the charging current of C_1.

$$Q_{in}(v) = \int_0^v C_1(v)dv\,. \tag{4-12}$$

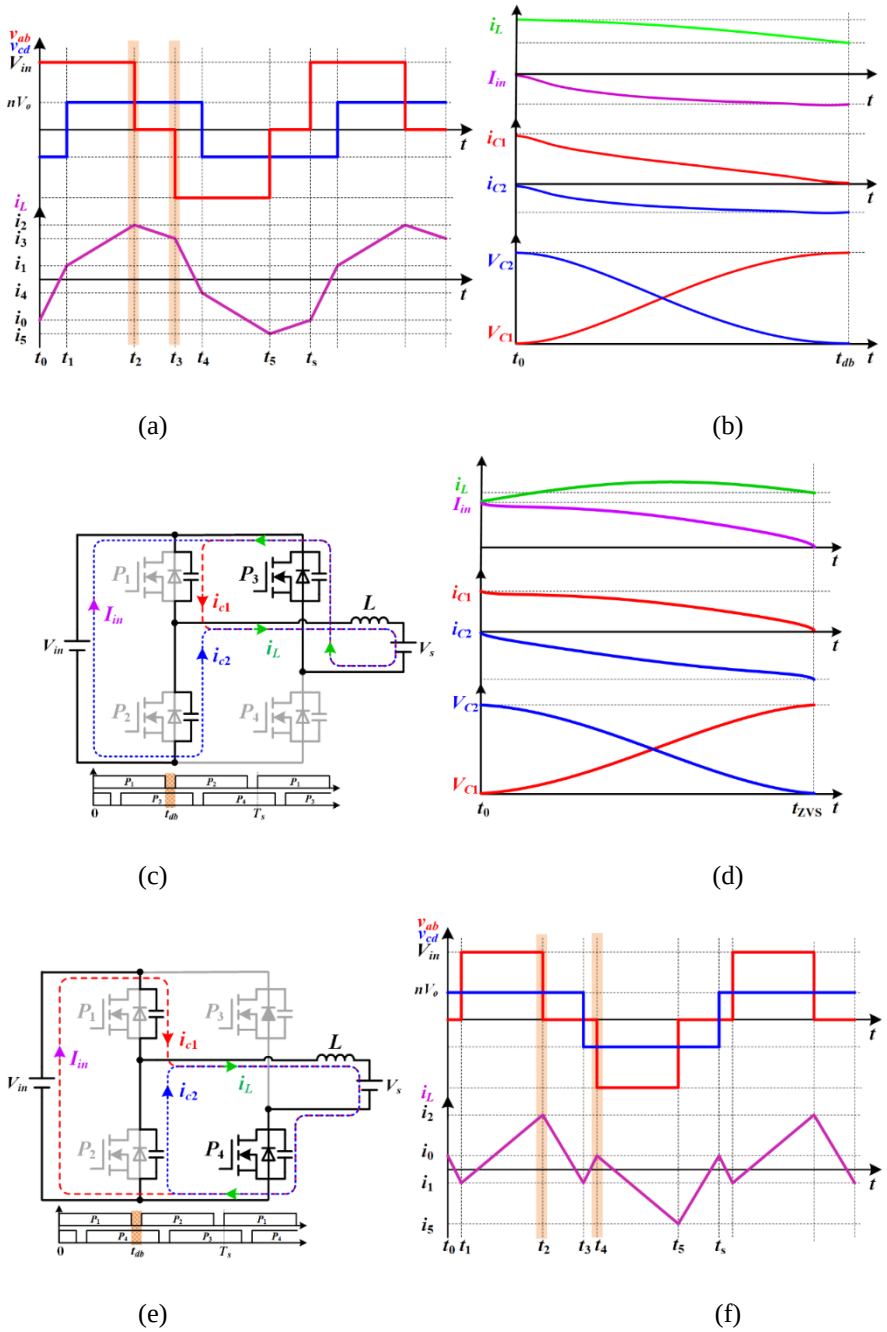


Figure 4.4. H-bridge ZVS transient process with inner phase shift: (a) transient process; (b) transient process waveform; (c) implementation in SPS; (d) implementation in DPS; (e) and (f) examples for DPS.

Different from the SPS control where all four switch capacitances are involved, here only two capacitances in one leg participate in the transient. The relationship between the inductor current and the voltage across P_1 is

$$i_L(v) = \sqrt{i_L^2(0) + \frac{2}{L}(E_{oss.bri}(0) - E_{oss.bri}(v) - Q_{i_L}(v)V_s + Q_{i_{in}}(v)V_{in})}\,. \quad (4\text{-}13)$$

(4-9) can still be used to estimate the time interval to realize ZVS. But from the energy point of view, the input voltage source supplies the energy, and the output voltage source consumes the energy. In this case, the minimal energy stored in the inductor to complete the ZVS transient process is

$$\frac{1}{2}Li_L^2(0) \geq 2Q_{oss}(V_{in})V_s - Q_{oss}(V_{in})V_{in}\,. \quad (4\text{-}14)$$

For the transient process shown in Figure 4.4 (c), the charge flowing through the input voltage source is

$$Q_{in}(v) = -\int_0^v C_2(V_{in} - v)dv\,. \quad (4\text{-}15)$$

In this circumstance, the input and output voltage sources both consume the energy from the inductor. So the minimal inductor energy to ensure ZVS is

$$\frac{1}{2}Li_L^2(0) \geq 2Q_{oss}(V_{in})V_s + Q_{oss}(V_{in})V_{in}\,. \quad (4\text{-}16)$$

where V_s can be positive, zero, or negative, depending on modulation strategies at the transformer secondary side.

In a summary, compared to the situation without inner phase shift, the input voltage source affects not only the ZVS transition time but also the minimum required initial

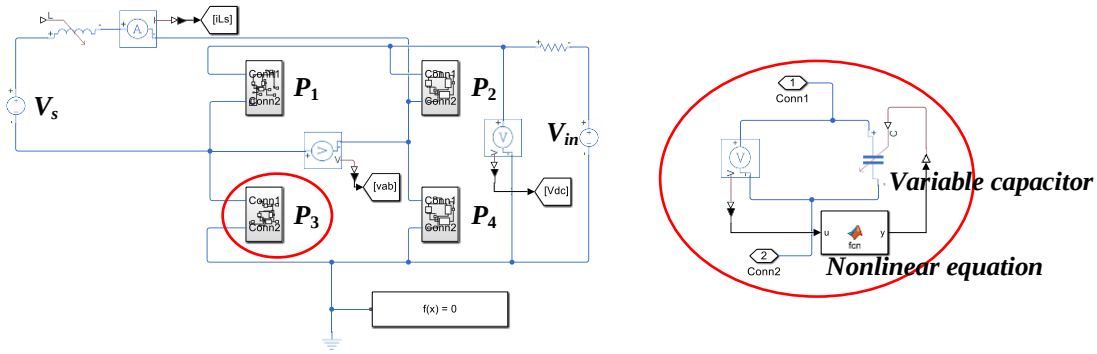
energy stored in the inductor. For different combinations of switching actions, V_{in} can dissipate or supply energy, which should be given full consideration in different modulation strategies. V_s still influences the ZVS process as discussed in Chapter III.

4.3 Simulation in MATLAB

To verify the resonance process described in the last section, the simulation model in MATLAB is built up, which is shown in Figure 4.5. The unit to analyze ZVS realization for primary-side switches contains H-bridge, reflected output voltage, and input voltage in Figure 4.5 (a). The switch model is replaced with the voltage-dependent capacitance which is used to represent the switch C_{oss} in Figure 4.5 (b). By adjusting the initial state of different capacitors, the resonance process during ZVS transient can be emulated.

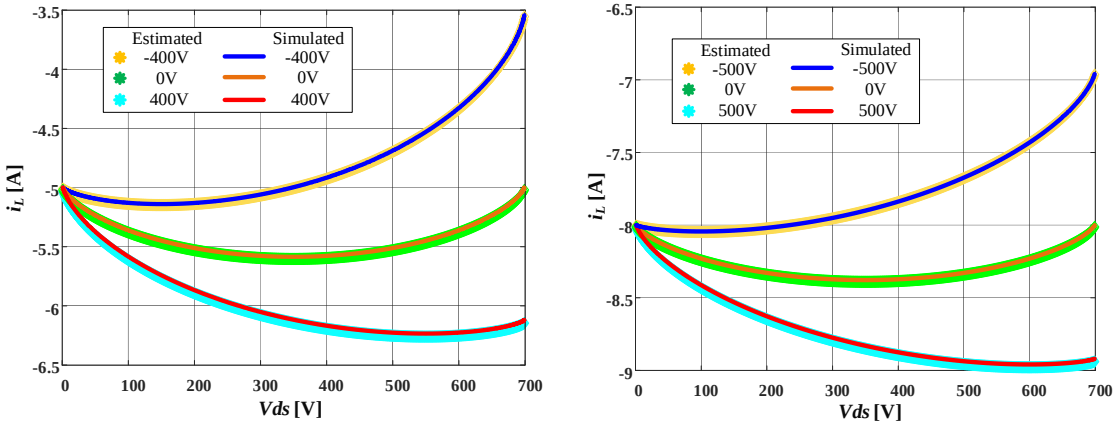
The simulation result is carried out to verify the ZVS transition when there is no inner phase shift in Figure 4.6. The input voltage is set at 700V, and the reflected output voltage is set at 400V and 500V, respectively in Figure 4.6 (a) and (b). To realize ZVS for P_2 and P_3, the initial inductor current is -5A and -8A.

Based on the simulation result, if the reflected output voltage is 0, the ZVS transition does not deplete any energy in the inductor. If the reflected output voltage is positive, it even provides the energy to the inductor to accelerate the resonance process. However, if the reflected output voltage is negative, it consumes the energy of the inductor. To complete the resonance process, there are requirements for the minimum initial inductor current. The result of estimation is matched with the simulation result, which verifies the accuracy of the derivation in the last section.



(a) (b)

Figure 4.5. Simulink model of primary-side H-bridge in DAB.



(a) (b)

Figure 4.6. Simulation and estimation result of ZVS transition without inner phase shift: (a) ±400V reflected output voltage; (b) ±500V reflected output voltage.

The transition time in the simulation and the result from equation derivation are shown in Table 4.1 and Table 4.2. The result from the ideal simulation is nearly the same as the calculation result.

4.4 Experiment Verification

To verify the ZVS transient process formulated above, an H-bridge prototype shown in Figure 4.7 has been built. The parameters are shown in Table 4.3 . The reflected secondary side voltage is replaced with a DC power supply. V_{ds} of the bottom switch P_2 and the inductor current is measured, which can indicate the energy exchange during the switching transient. Figure 4.8 shows an exemplary experimental waveform. Based on the measurement data, an I-V curve is plotted with ZVS transition time calculated. Such an experimental I-V curve is then compared with the estimated curve to verify the energy exchange in the proposed analysis. The estimated and experimental ZVS transition times are listed in Table 4.4, which shows a good match.

Figure 4.9 shows the experimental results of the ZVS transient process based on the modulation without inner phase shift at the primary side. The input voltage, output voltage, and the initial inductor current are provided in the corresponding figures. All the calculated I-V curves are overlapped with experimental results. When output voltage V_s=0, there is no energy dissipated in the transient process, i.e., initial and final inductor current values remain nearly the same. For the modulation with inner phase shift, Figure 4.10 shows the test results related to Figure 4.4 (a). Here V_{in} supplies the energy to help complete the ZVS process, resulting in the increment of i_L. Test results are consistent with the estimation.

Table 4.1. ZVS Transition time in Figure 4.6 (a).

V_s	Simulation time	Estimation time
-400V	59.5ns	59.4ns
0	51.9ns	52ns
400V	47.4ns	47.2ns

Table 4.2. ZVS Transition time in Figure 4.6 (b).

V_s	Simulation time	Estimation time
-400V	59.5ns	59.4ns
0	51.9ns	52ns
400V	47.4ns	47.2ns

Table 4.3. Prototype Setup

Name	Value	Name	Value
Switch	SCT3030KL	Inductor	20μH
Scope	MDO4104C	Voltage probe	TPP0805
Current probe	TCP0030		

Table 4.4. Transition time comparison

(ns)\#	1	2	3	4	5	6
Estimation	70.5	121.3	65.2	76.1	67.23	66.62
Experiment	71.4	118.3	65.8	77.8	69.6	71

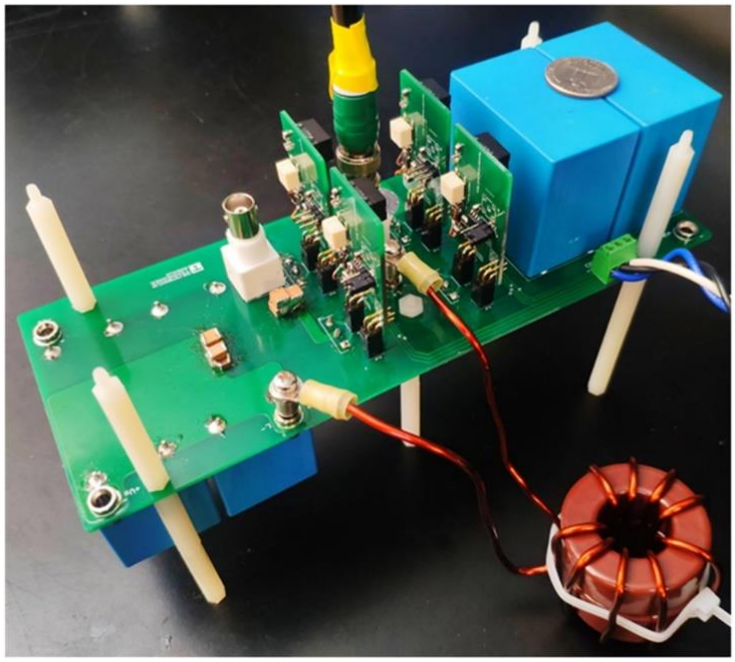


Figure 4.7. H-bridge prototype.

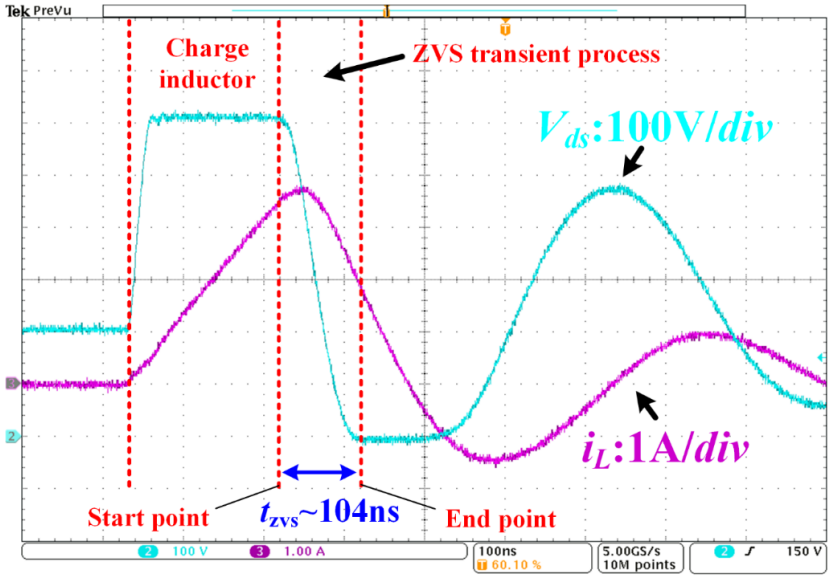


Figure 4.8. Example of the switching waveform.

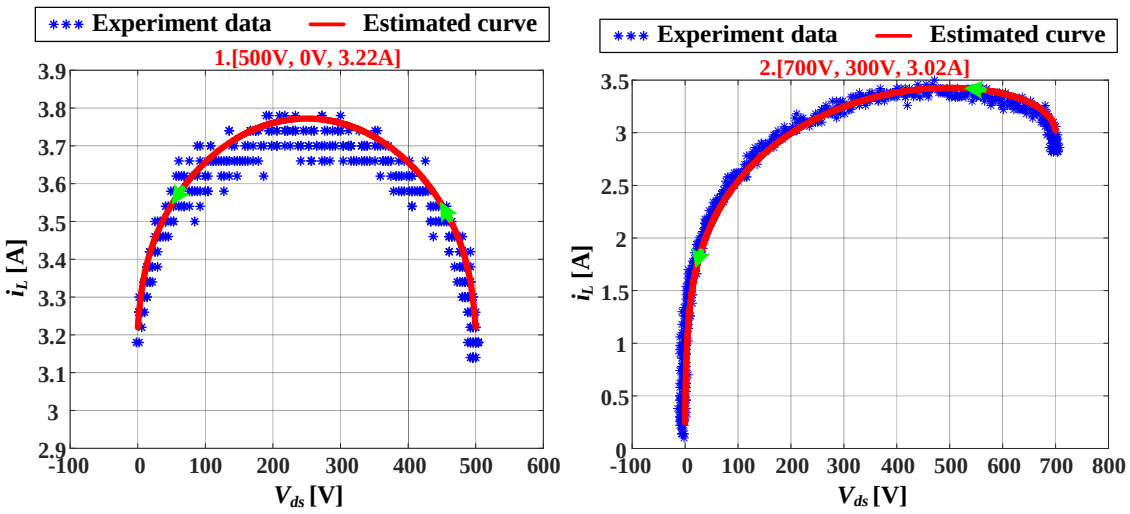


Figure 4.9. I-V curve comparison based on the modulation without inner phase shift @ [V_{in}, V_s, $i_L(0)$].

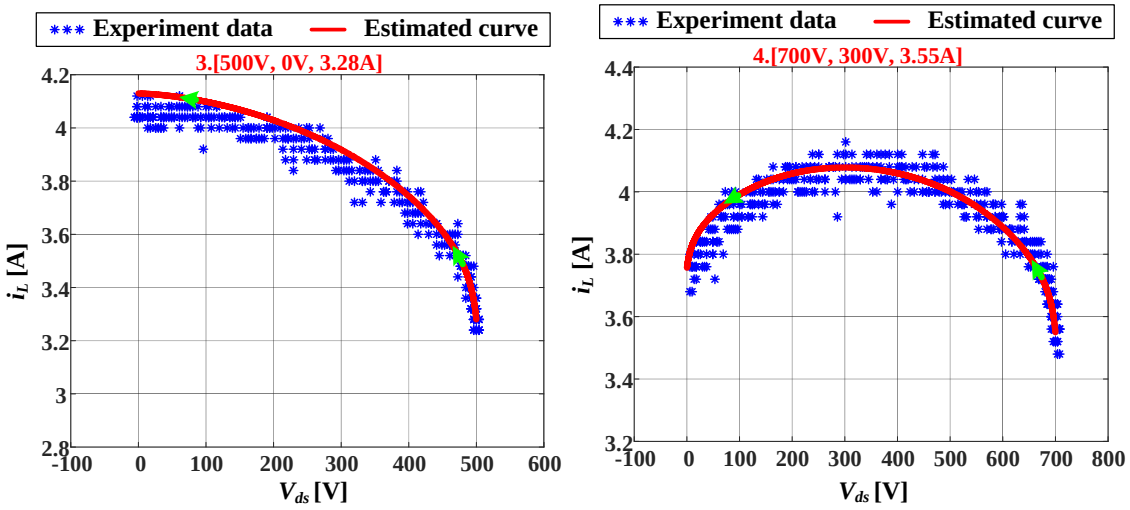


Figure 4.10. I-V curve comparison based on the modulation with inner phase shift-lower switch ZVS @ [V_{in}, V_s, $i_L(0)$].

The test results shown in Figure 4.11 correspond to Figure 4.4 (c). In this case, C_{oss} of P_2 is also discharged in the transient process, and V_{in} consumes energy. According to the figure below, the estimated and experimental I-V curves are still well aligned.

4.5 Comparison between Existing ZVS Current Requirement

Based on the analysis in the previous section, the minimum initial inductor current depends on the different modulation strategies, which are categorized in Table 4.5. An example of detailed values based on V_{in}=600V and V_s=400V in different circumstances is also shown in the table. It is observed that the calculations in references based on a single half-bridge are not accurate. The comparisons of minimum initial current to fully realize ZVS within a certain input and output voltage range are shown in Figure 4.12. The previous ZVS analysis cannot fulfill all circumstances, which can cause either underestimation or overestimation of ZVS current settings and dead time.

4.6 Conclusion

For DAB converters, previous literature does not consider the influence of modulation strategies, which can alter the resonant loop in ZVS transitions. The simple half-bridge model used in existing literature cannot cover all cases. In this chapter, three basic ZVS resonant loops based on the H-bridge model with different minimal initial inductor energy to fully realize ZVS are proposed, as the main contribution. The accuracy of the proposed analysis is verified experimentally. The comparison of I-V curves can be used to comprehend the energy exchange in the transient process, which helps to further verify the

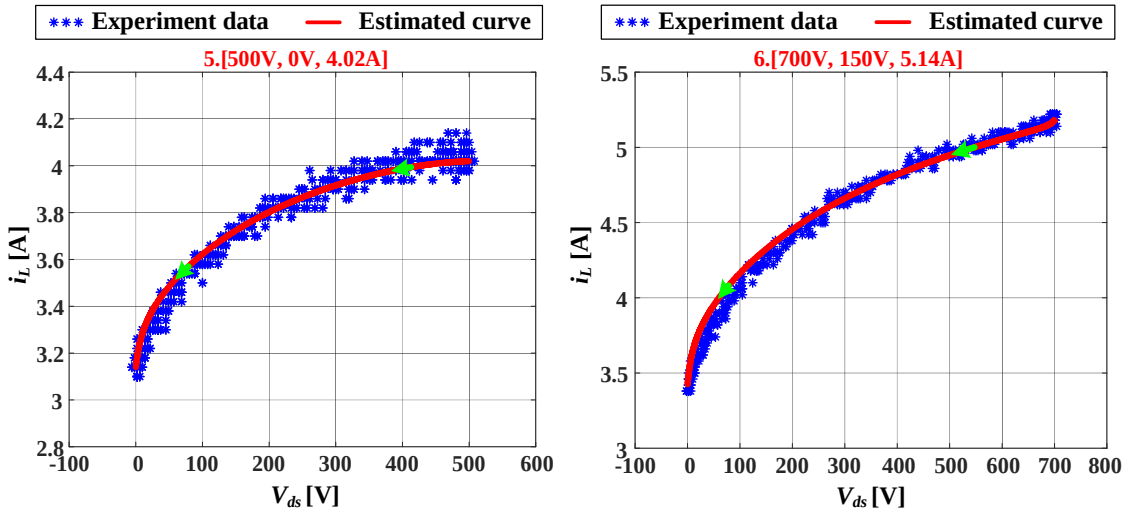


Figure 4.11. I-V curve comparison based on the modulation without inner phase shift-upper switch ZVS @ [V_{in}, V_s, $i_L(0)$].

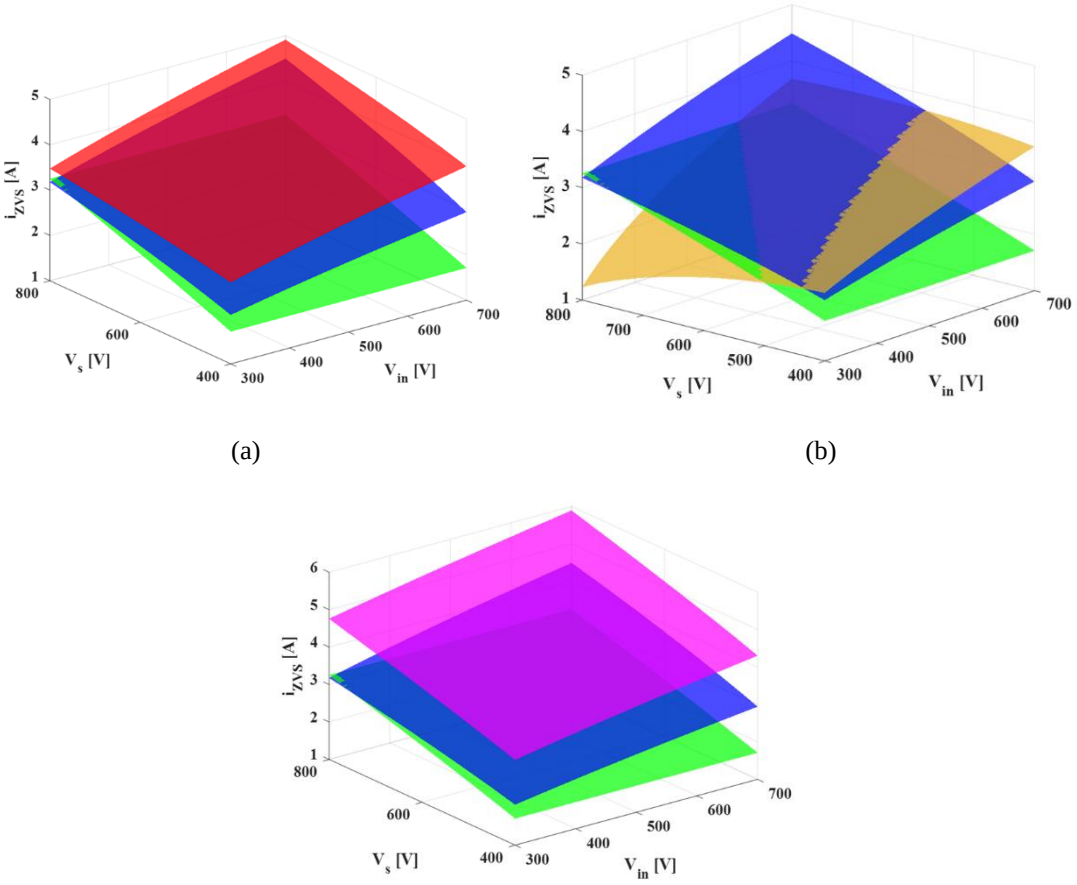


Figure 4.12. Comparison of minimal initial inductor current: (a) Without inner phase shift; (b) With inner phase shift 1; (c) With inner phase shift 2.

Table 4.5. Comparison of minimum initial inductor energy

Modulation	Minimum initial inductor current Equation	Value
Without inner phase shift	$\frac{1}{2}Li_L^2(0) \geq 2Q_{oss}(V_{in})V_s$	110.86μJ
With inner phase shift 1	$\frac{1}{2}Li_L^2(0) \geq 2Q_{oss}(V_{in})V_s - Q_{oss}(V_{in})V_{in}$	29.52μJ
With inner phase shift 2	$\frac{1}{2}Li_L^2(0) \geq 2Q_{oss}(V_{in})V_s + Q_{oss}(V_{in})V_{in}$	192.21μJ
Reference [1]	$\frac{1}{2}Li_L^2(0) \geq 2CV_{in}nV_o$	59.66μJ
Reference [8]	$\frac{1}{2}Li_L^2(0) \geq Q_{oss}(V_{in})V_{in}$	83.15μJ

proposed minimal initial inductor energy. Based on this, considering the non-linearity of switch output capacitance, this paper accurately derives the ZVS transition time by utilizing the C_{oss} curve from the datasheet. The proposed calculation of minimal initial inductor energy and the transition time can be accurate references to set ZVS current and dead time in real converter applications.

Chapter 5 ANALYTICAL COMMON-MODE VOLTAGE MODEL IN DUAL ACTIVE BRIDGE

The MPS modulation strategies of DAB have been proposed to optimize the efficiency, eliminate the reactive power, and release the current stress. While the previous literature focuses on the accurate loss model in steady states or small-signal analysis for the dynamic response, the CM model has been largely ignored. So, in this chapter, the analytical model of CMV is proposed for DAB, which considers the CM parasitic capacitances including those of grounded heatsink and transformer windings. Based on such a model, the CM performance is compared among different modulation strategies [145]. The impact of two H-bridge on the input and output CMV has been addressed.

5.1 Consideration of Parasitic Capacitance in DAB Common-mode Analysis

5.1.1 Parasitic Capacitor in Grounded Heatsink

In the DAB converter, switching actions at H-bridge generate high-frequency voltage pulses, which act as CMV sources. The parasitic capacitance then provides the common-mode path. In this section, the parasitic capacitance at different positions will be discussed.

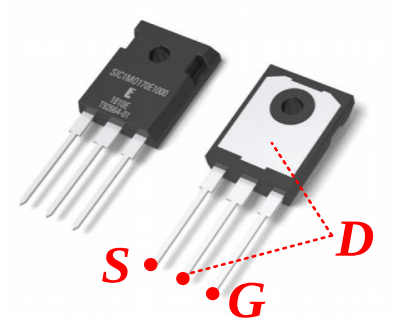
For the majority of discrete devices, thermal pads are not only for heat dissipation but also connected to drain or source of switches. In a cooling system, thermal interface materials (TIMs) are inserted between the thermal pad and heatsink, which has a high dielectric constant. The TIM should also be as thin as possible aiming at low thermal resistance, which then introduces the capacitance between D/S and the heatsink. The heatsink can be connected to the converter case, which is usually for safety concerns. In

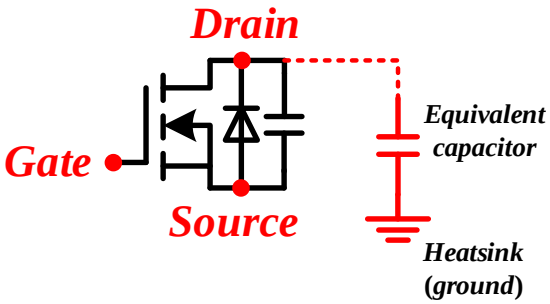
some designs, the enclosure can be directly used as the heatsink, which makes the overall parasitic capacitance between the switch thermal pad and ground considerable. Two WBG devices are shown in Figure 5.1. TO-247 is a commonly used package for SiC power MOSFETs, as shown in Figure 5.1 (a). The thermal pads are connected to the drain of the device, yielding an equivalent parasitic capacitance between drain and ground, as shown in Figure 5.1 (b). In Figure 5.1 (c), a top-cooled GaN device has the thermal pad connected to the source of the device, yielding the equivalent capacitance between the source and ground.

5.1.2 Common-mode Capacitance in Transformer

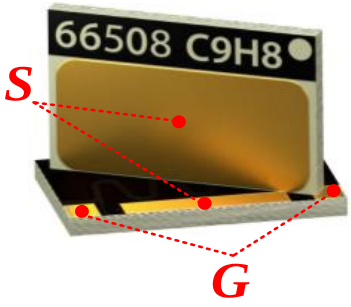
In the DAB converter, between two H-bridges is a high-frequency transformer for the galvanic isolation, power transfer, and voltage gain, which, however, also provides the path for the CMC between the primary and secondary sides. Assuming the parasitic capacitance is distributed evenly between the primary and secondary windings, as shown in Figure 5.2 (a) [146], we then can simplify the transformer model like Figure 5.2 (b) [147, 148].

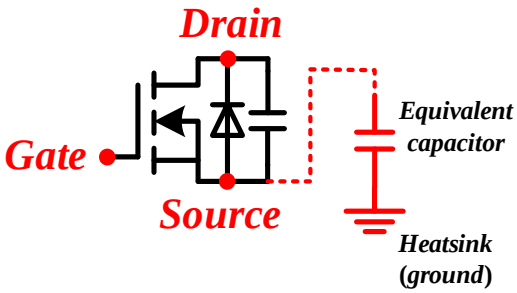
Here four equivalent capacitances are employed. The capacitance of primary-side winding or secondary-side winding is for the DM only. The capacitance between the primary side and secondary side is CM capacitance. It acts as a “bridge” to couple the CM loops on both sides. In addition, if the parasitic capacitance between PCB polygon and ground is large enough, it can also provide the CMC path.





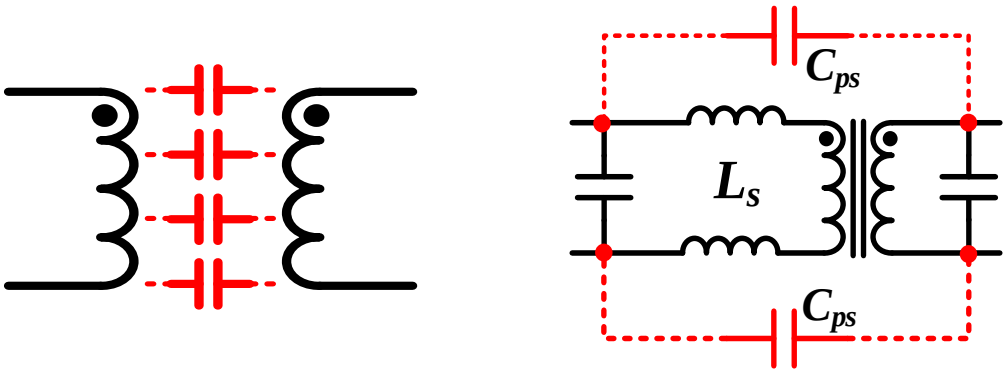
(a) (b)





(c) (d)

Figure 5.1. Equivalent parasitic capacitance of different switches to heatsink: (a) TO-247 package switch; (b) the equivalent capacitor to ground in TO-247 package [149]; (c) GS66508T [150]; (d) the equivalent capacitor to ground of GS66508T.



(a) (b)

Figure 5.2. Transformer considering parasites in the CM analysis: (a) the distribution of the parasitic capacitance between the primary side and secondary side of the transformer: (b) the transformer model with parasitic capacitances.

5.2 General Common-mode Parasitic Capacitance in DAB

In CM discussion, the frequency domain analysis is mainly based on the spectrum from kilo-Hz to mega-Hz. In this frequency domain, the impedance of the DC-link capacitor is quite small, which can be regarded as short-circuit in CM loops. Hence in the DAB converter, there are six networks formed by active switches and transformers, which include primary-side DC-link, secondary-side DC-link, and four mid-points of phase legs, as shown in Figure 5.3. Also, the equivalent parasitic capacitance, $C_{i\#,}$ and $C_{o\#}$, in the input source and load are considered to form CM loops in DAB. The CMV across $C_{i\#}$ and $C_{o\#}$ can represent the influence of the DAB converter on input source and load. When testing the prototype under certain EMI standards, the equivalent parasitic capacitance can be replaced by those inside LISNs, e.g., 50Ω and series capacitance. In this paper, only equivalent parasitic capacitance is used to build the analytical CM model without considering the impact of LISNs.To analyze the CM performance of the DAB converter, the topology shown in Figure 5.3 can be further simplified in Figure 5.4. The DM components are removed. The DC-link capacitors, transformer windings, and DC sources are removed from the CM topology. Phase legs are replaced with high-frequency voltage sources caused by switching actions.Because $C_{pg'}$, C_{i1} and C_{i2} are all connected to the primary-side DC-link, in CM topology they are paralleled. Such a scenario applies to the secondary-side DC-link. C_{pg} and C_{sg} in Figure 5.4 are

$$\begin{cases} C_{pg} = C_{pg'} + C_{i1} + C_{i2} \\ C_{sg} = C_{sg'} + C_{o1} + C_{o2} \end{cases}. \tag{5-1}$$

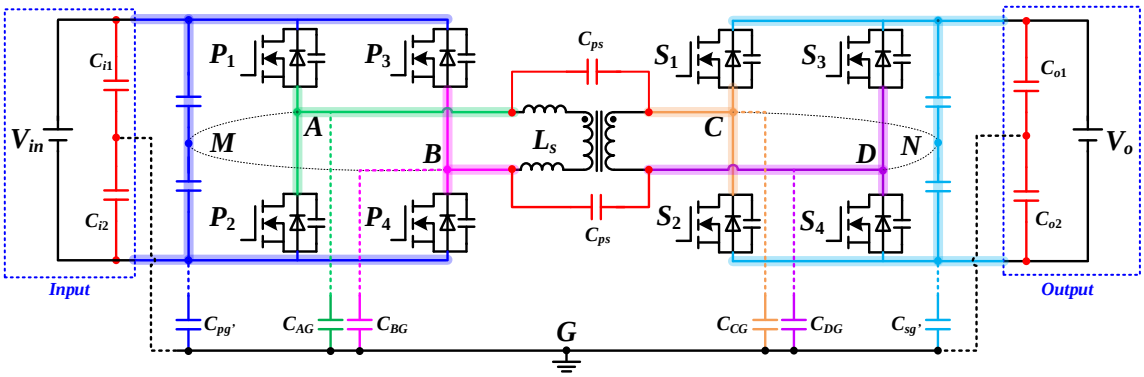


Figure 5.3. General parasitic capacitance from topology to ground in DAB converter.

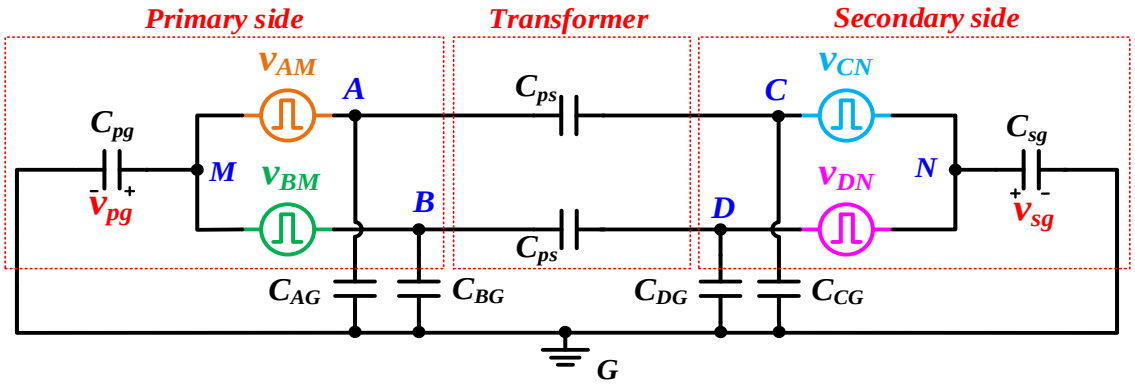


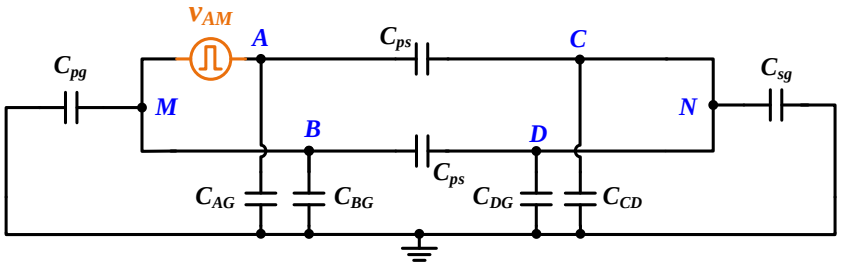
Figure 5.4. General common-mode topology of the DAB converter.

v_{pg} across the primary-side DC-link and ground is CMV applied to the input source of the DAB converter, which determines the CM performance. v_{sg} across the secondary-side DC-link and ground is CMV applied to the load. M and N points in Figure 5.3 and Figure 5.4 are the virtual middle points of DC-link and output capacitors, respectively. The CM topology shown in Figure 5.4 can be used for general DAB CM analysis, which includes all potential parasitic capacitance from the prototype to the ground in different networks. For the primary side, the parasitic capacitance from DC-link to ground is C_{pg}, and the parasitic capacitance from phase-leg mid-point to the ground is C_{AG} and C_{BG}. For the secondary side, the parasitic capacitance from the output to the ground is C_{sg}, and the parasitic capacitance from the phase-leg mid-point to the ground is C_{CG} and C_{DG}. The winding capacitance between the primary side and secondary side is C_{ps}. The definitions of different symbols in Figure 5.4 are presented in Table 5.1.

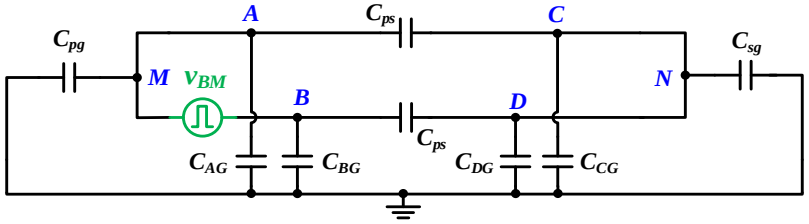
In this section, general CM capacitances in the DAB converter are introduced. The simplified CM topology will be proposed to derive the analytical model of the DAB converter in the next section.

5.3 Generalized Common-mode Voltage Model

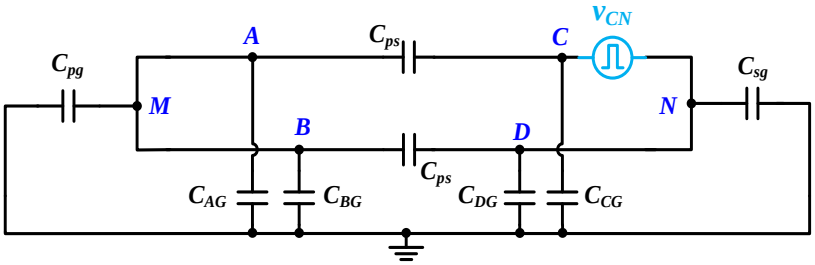
According to the general CM topology in Figure 5.4, the CM analytical model for the DAB converter is derived in the following content. To quantify the voltage distributed across both input and output capacitors, the Superposition Theorem is employed in Figure 5.5. Four CMV sources act in the circuit separately, as shown in Figure 5.5. The final voltage distributed across each capacitor is then the sum of the four individual circuits.



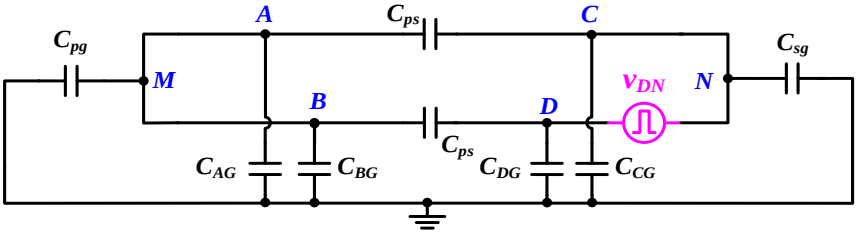
(a)



(b)



(c)



(d)

Figure 5.5. Decomposed circuit with Superposition theorem: (a) CM loop with first phase leg at the primary side; (b) CM loop with second phase leg at the primary side; (c) CM loop with first phase leg at the secondary side; (d) CM loop with second phase leg at the secondary side.

Table 5.1. General CM Parasitic Capacitance in DAB

Names of Capacitance	Symbol
Phase-leg Mid-point to Ground (Primary)	C_{AG}, C_{BG}
Phase-leg Mid-point to Ground (Secondary)	C_{CG}, C_{DG}
DC-link to Ground (Primary)	C_{pg}
DC-link to Ground (Secondary)	C_{sg}
Primary side to secondary side (Transformer)	C_{ps}

For each circuit in Figure 5.5, Thevenin's Theorem is used to abstract the equivalent voltage source and series impedance. For example, in Figure 5.6 (a) to quantify the CMV across the input parasitic capacitors, the circuit is summarized as a two-port network between M and G. Then according to Thevenin's theorem, the equivalent voltage source and series impedance are abstracted as Figure 5.6 (b) and (c). Here C_1 in the figure is

$$C_1 = C_{sg} + C_{CG} + C_{DG}. \tag{5-2}$$

The open-loop output voltage U of the two-port network in Figure 5.6 (b) is

$$U = v_{AM} \frac{2C_{AG}C_{ps} + C_{AG}C_{CG} + C_{AG}C_{DG} + C_{AG}C_{sg} + C_{ps}C_{CG} + C_{ps}C_{DG} + C_{ps}C_{sg}}{2C_{AG}C_{ps} + C_{AG}C_{CG} + C_{AG}C_{DG} + C_{AG}C_{sg} + 2C_{ps}C_{CG} + 2C_{ps}C_{DG} + 2C_{ps}C_{sg}} \tag{5-3}$$

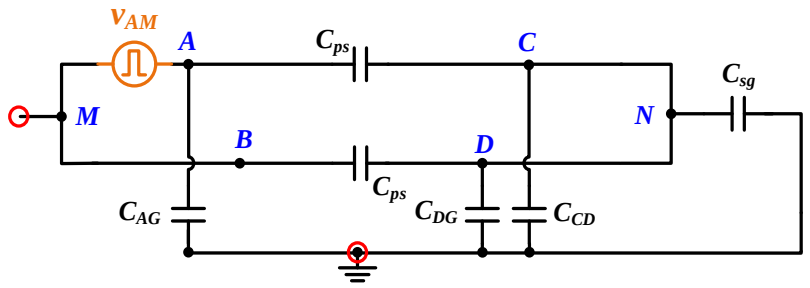
The internal impedance Z of the two-port network in Figure 5.6 (c) is

$$Z = \frac{2C_{ps} + C_{CG} + C_{DG} + C_{sg}}{\omega(2C_{AG}C_{ps} + C_{AG}C_{CG} + C_{AG}C_{DG} + C_{AG}C_{sg} + 2C_{ps}C_{CG} + 2C_{ps}C_{DG} + 2C_{ps}C_{sg})} \tag{5-4}$$

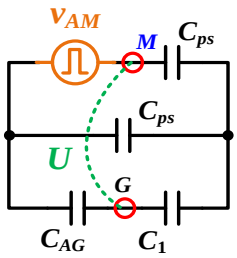
The CMV across the input capacitors can then be formulated as (5-5), with all variables provided in (5-6).

$$v_{pg} = P_1 v_{AM} + P_2 v_{BM} + S_1 v_{CN} + S_2 v_{DN}. \tag{5-5}$$

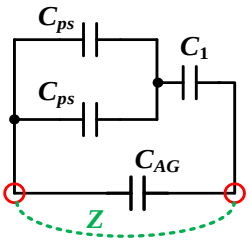
$$\begin{cases} P_1 = \dfrac{2C_{AG}C_{ps} + \left(C_{AG} + C_{ps}\right)\left(C_{CG} + C_{DG} + C_{sg}\right)}{\left(C_{AG} + C_{BG} + C_{pg} + 2C_{ps}\right)\left(C_{CG} + C_{DG} + C_{sg}\right) + 2C_{ps}\left(C_{AG} + C_{BG} + C_{pg}\right)} \\ P_2 = \dfrac{2C_{BG}C_{ps} + \left(C_{BG} + C_{ps}\right)\left(C_{CG} + C_{DG} + C_{sg}\right)}{\left(C_{AG} + C_{BG} + C_{pg} + 2C_{ps}\right)\left(C_{sCG} + C_{DG} + C_{sg}\right) + 2C_{ps}\left(C_{AG} + C_{BG} + C_{pg}\right)} \\ S_1 = \dfrac{C_{ps}\left(C_{CG} - C_{DG} - C_{sg}\right)}{\left(C_{AG} + C_{BG} + C_{pg} + 2C_{ps}\right)\left(C_{CG} + C_{DG} + C_{sg}\right) + 2C_{ps}\left(C_{AG} + C_{BG} + C_{pg}\right)} \\ S_2 = \dfrac{C_{ps}\left(C_{DG} - C_{CG} - C_{sg}\right)}{\left(C_{AG} + C_{BG} + C_{pg} + 2C_{ps}\right)\left(C_{CG} + C_{DG} + C_{sg}\right) + 2C_{ps}\left(C_{AG} + C_{BG} + C_{pg}\right)} \end{cases}. \tag{5-6}$$



(a)



(c)



(d)

Figure 5.6. Thevenin's theorem application: (a) Two-port network; (b) equivalent voltage source; (c) equivalent impedance.

With the same calculation procedure, the voltage across the output capacitors is then shown in (5-7), and the variables are provided in (5-8).

$$v_{sg} = P_3 v_{AM} + P_4 v_{BM} + S_3 v_{CN} + S_4 v_{DN} . \tag{5-7}$$

$$\begin{cases} P_3 = \dfrac{C_{ps}\left(C_{AG} - C_{BG} - C_{pg}\right)}{\left(C_{CG} + C_{DG} + C_{sg} + 2C_{ps}\right)\left(C_{AG} + C_{BG} + C_{pg}\right) + 2C_{ps}\left(C_{CG} + C_{DG} + C_{sg}\right)} \\ P_4 = \dfrac{C_{ps}\left(C_{BG} - C_{AG} - C_{pg}\right)}{\left(C_{CG} + C_{DG} + C_{sg} + 2C_{ps}\right)\left(C_{AG} + C_{BG} + C_{pg}\right) + 2C_{ps}\left(C_{CG} + C_{DG} + C_{sg}\right)} \\ S_3 = \dfrac{2C_{CG}C_{ps} + \left(C_{CG} + C_{ps}\right)\left(C_{AG} + C_{BG} + C_{pg}\right)}{\left(C_{CG} + C_{DG} + C_{sg} + 2C_{ps}\right)\left(C_{AG} + C_{BG} + C_{pg}\right) + 2C_{ps}\left(C_{CG} + C_{DG} + C_{sg}\right)} \\ S_4 = \dfrac{2C_{DG}C_{ps} + \left(C_{DG} + C_{ps}\right)\left(C_{AG} + C_{BG} + C_{pg}\right)}{\left(C_{CG} + C_{DG} + C_{sg} + 2C_{ps}\right)\left(C_{AG} + C_{BG} + C_{pg}\right) + 2C_{ps}\left(C_{CG} + C_{DG} + C_{sg}\right)} \end{cases} . \tag{5-8}$$

(5-5) and (5-7) are the analytical CMV model for the DAB converter, which is derived from the general CM topology shown in Figure 5.4. In equations, the CMVs at input and output are both decided by all four CMV sources.

Based on (5-6) and (5-8), the variables on both sides have similar expressions. When the primary-side full-bridge has the symmetric layout for two legs, which means C_{AG}=C_{BG}, P_1 is equal to P_2 and P_3 is equal to P_4. The same conclusion applies to the secondary side. Hence the input and output CMV are

$$\begin{cases} v_{pg} = P_1(v_{AM} + v_{BM}) + S_1(v_{CN} + v_{DN}) \\ v_{sg} = P_3(v_{AM} + v_{BM}) + S_3(v_{CN} + v_{DN}) \end{cases} . \tag{5-9}$$

Variables in the simplified equations are then

$$\begin{cases} P_1 = P_2 = \dfrac{2C_{AG}C_{ps} + \left(C_{AG} + C_{ps}\right)\left(2C_{CG} + C_{sg}\right)}{\left(2C_{AG} + C_{pg} + 2C_{ps}\right)\left(2C_{CG} + C_{sg}\right) + 2C_{ps}\left(2C_{AG} + C_{pg}\right)} \\ S_1 = S_2 = \dfrac{-C_{sg}C_{ps}}{\left(2C_{AG} + C_{pg} + 2C_{ps}\right)\left(2C_{CG} + C_{sg}\right) + 2C_{ps}\left(2C_{AG} + C_{pg}\right)} \end{cases}. \quad (5\text{-}10)$$

To verify the proposed general CM topology for the DAB converter with the analytical model in (5) and (7), a DAB prototype discussed in Chapter 3 is used to verify the proposed CMV model.

After including parasitic capacitances in the DAB converter, the topology with different CM capacitances is shown in Figure 5.7. C_{p1} is the parasitic capacitance between the polygon of primary side DC+ and ground, and C_{p4} is the parasitic capacitance between primary side DC- and ground. C_{p2}, C_{p3}, $C_{p5,}$ and C_{p6} are the parasitic capacitance from switches to the ground via the heatsink. C_{s1} is the parasitic capacitance between secondary side DC+ polygon and ground, and C_{s4} is the parasitic capacitance between secondary side DC- and ground. C_{s2}, C_{s3}, $C_{s5,}$ and C_{s6} are the parasitic capacitance from switches to the ground via the heatsink. C_{ps} is the equivalent winding capacitance between the primary and secondary sides of the transformer. Other parasites such as inductance (nH) and resistance (mΩ) caused by PCB traces have little influence on the CM performance in the high-frequency domain compared with capacitance above (pF), which are ignored in this chapter.

With TO-247 SiC MOSFETs, the CM capacitance of the switches is between the drain and the ground. All parasitic capacitance providing paths for CMI in the prototype is summarized in Table 5.2.

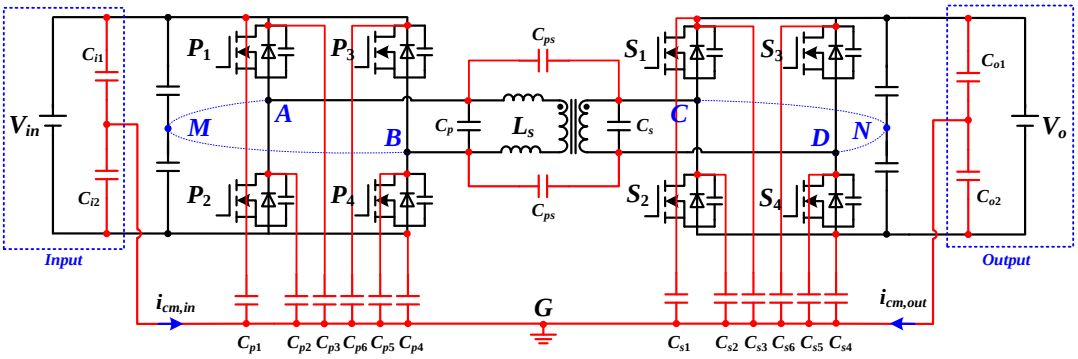


Figure 5.7. Common-mode loops in the DAB converter.

Table 5.2. Summary of Parasitic Capacitance

Names of Capacitance	Symbol	Values
Drain to Ground (Primary)	$C_{p2,\ 3,\ 5,\ 6}$	200pF
Drain to Ground (Secondary)	$C_{s2,\ 3,\ 5,\ 6}$	160pF
DC+ or DC- to Ground (Primary)	$C_{p1,\ 4}$	300pF
DC+ or DC- to Ground (Secondary)	$C_{s1,\ 4}$	220pF
Primary side to secondary side (Transformer)	C_{ps}	37.5pF
Equivalent capacitance (Input)	$C_{i\#}$	100pF
Equivalent capacitance (Output)	$C_{o\#}$	100pF

Furthermore, all the capacitances in the generalized model are

$$\begin{cases} C_{pg} = C_{i1} + C_{i2} + C_{p1} + C_{p3} + C_{p4} + C_{p6} = 1200\,pF \\ C_{AG} = C_{p2} = 200\,pF \\ C_{BG} = C_{p5} = 200\,pF \\ C_{sg} = C_{o1} + C_{o2} + C_{s1} + C_{s3} + C_{s4} + C_{s6} = 960\,pF \\ C_{CG} = C_{s2} = 160\,pF \\ C_{DG} = C_{s5} = 160\,pF \end{cases}. \tag{5-11}$$

Considering the parameters mentioned in Table 5.2, the analytical CMV model particularly for our built prototype at the input and output sides is formulated as

$$\begin{cases} v_{pg} = 0.1409(v_{AM} + v_{BM}) - 0.0159(v_{CN} + v_{DN}) \\ v_{sg} = -0.0199(v_{AM} + v_{BM}) + 0.1449(v_{CN} + v_{DN}) \end{cases}. \tag{5-12}$$

Although in the past, some qualitative analysis indicates the high frequency switching actions of four-phase legs are the excitations of the DAB CMV, (5-5) and (5-7) quantify the input and output CMVs and indicates CMVs are determined by the primary and secondary H-bridges together. The high-frequency voltage generated by each bridge leg is a two-level waveform. By summing all of them together, the input and output CMV can be a multi-level waveform. According to P_1, P_2, S_3, and S_4 in (5-6) and (5-8), the parasitic capacitance from the middle point of the bridge leg to the ground is caused by the heatsink provides the path for CMI at the primary side or secondary side. The winding capacitance of the transformer makes the CM loops at both sides coupled together. Last but not the least, from the equation (5-13), the input CMV is dominated by the primary side H-bridge and the output CMV is dominated by the secondary side H-bridge, respectively.

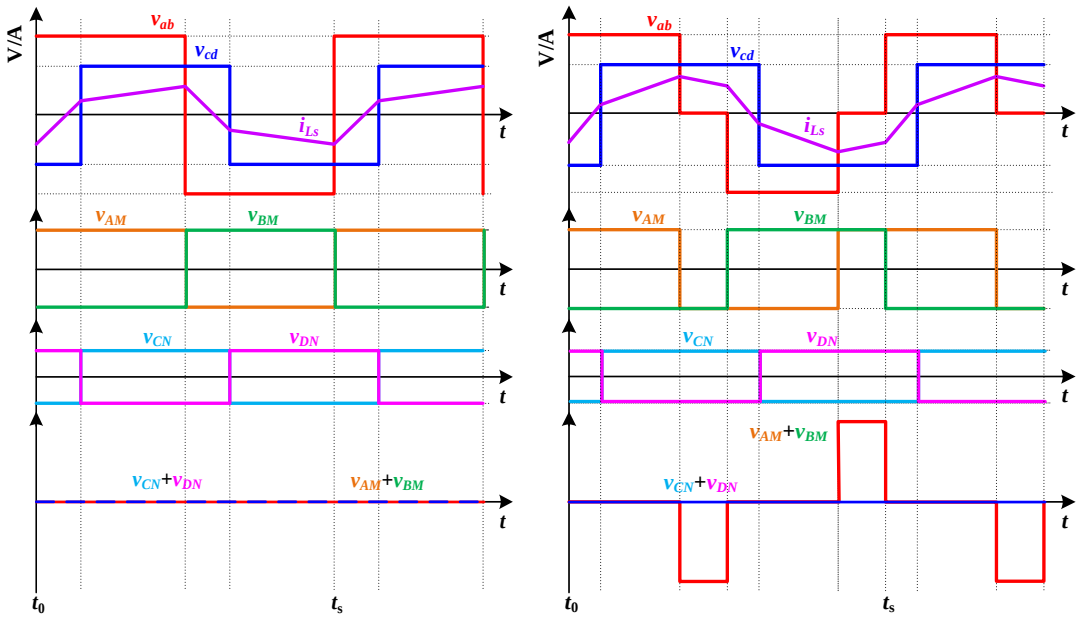
In phase-shift control algorithms of the DAB, the phase angles between different phase legs are implemented, which can shape the waveform in (5-12) drastically. Based on the analytical model developed in this section, the input and output CM behaviors of the DAB can be quantified when imposing various phase angles in SPS, DPS, and TPS modulation strategies, which is the main content of the next section.

5.4 Consideration of Common-mode Voltage Based on Multiple Phase Shift Modulation

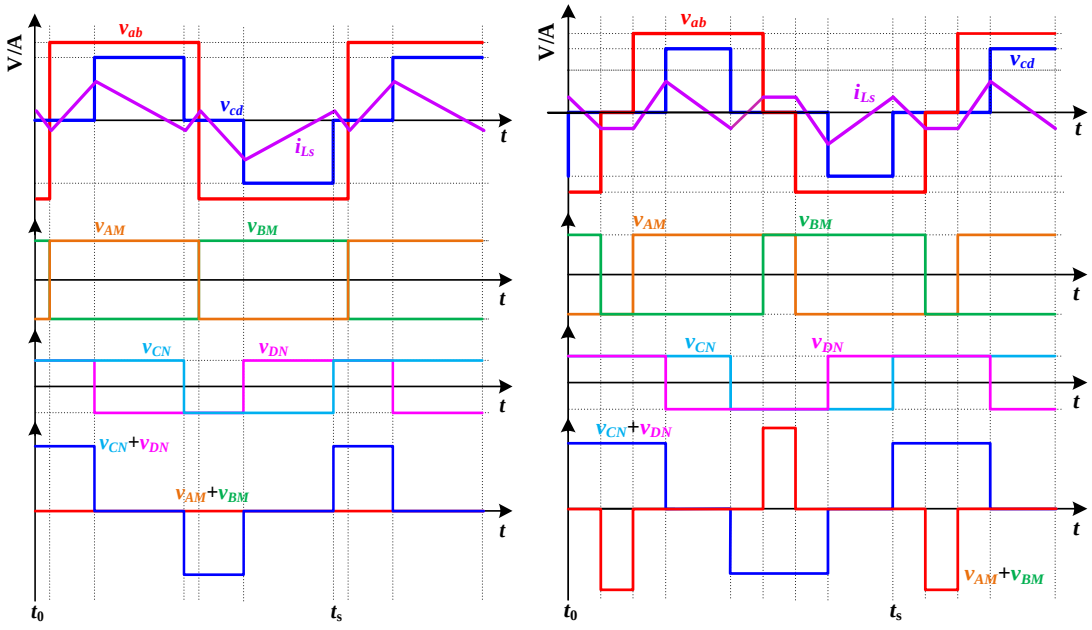
With the quantified CMV at input and output presented in the last section, this section will investigate various impact factors of CM performance of the DAB converter, mainly the phase shift and ZVS current.

For phase shift controls, when the inner phase shift is applied to H-bridge, its output voltage becomes a symmetric three-level waveform. For other hybrid modulation strategies, the output voltage of the H-bridge is an asymmetric three-level waveform. While different modulation strategies change the outlook of the CMV, this paper particularly focuses on SPS, DPS, and TPS, as shown in Figure 5.8.

For the SPS control, there is no inner phase shift at either the primary side or secondary side in Figure 5.8 (a), which means theoretically there is no CMV source existing. In Figure 5.8 (b), when the input voltage is higher than the reflected output voltage, the inner phase shift is implemented at the primary side H-bridge (PDPS).



(c) (d)



(c) (d)

Figure 5.8. Switching waveforms of different modulations: (a) SPS; (b) PDPS; (c) SDPS; (d) TPS.

Hence the CMV source is generated by the primary-side H-bridge. If the inner phase shift is only implemented at the secondary side (SDPS), the CMV source only appears at the secondary side, as shown in Figure 5.8 (c). In TPS control, both sides have inner phase shifts contributing to the CMV and CMI, as shown in Figure 5.8 (d). All CMV is shown as the last plot of each figure. It remains the same for hybrid modulation strategies.

Based on the analytical model in the last section, for DPS control, the input and output CMV should be three-level waveforms, which is the proportion of the output voltage of the H-bridge at the primary side or secondary side. When using TPS control, the input and output CMV should be five-level waveforms, which are combinations of the output voltage of the primary side and secondary side H-bridges.

A Ltspice simulation model is built to verify the analysis above, with the simulation result shown in Figure 5.9. Hence TPS modulation strategy is carried out in the simulation model. Both primary-side and secondary-side H-bridges act as CMV sources. The pulses only appear when there are zero platforms at the output voltage of either H-bridge. The voltages across the equivalent CM capacitances at the input voltage source and load end are five-level, which is decided by the primary side and secondary side H-bridges together. The CM loops of both sides are coupled through the equivalent CM capacitance of the transformer. The voltage values of such five-level waveforms are also marked in Figure 5.9. Based on the (5-12) in Section III, with 400V input voltage and 150V output voltage, the CMV at the input and output caused by the primary side H-bridge is calculated as 56.36V and 7.95V, respectively. The CMV at output caused by the secondary side H-bridge

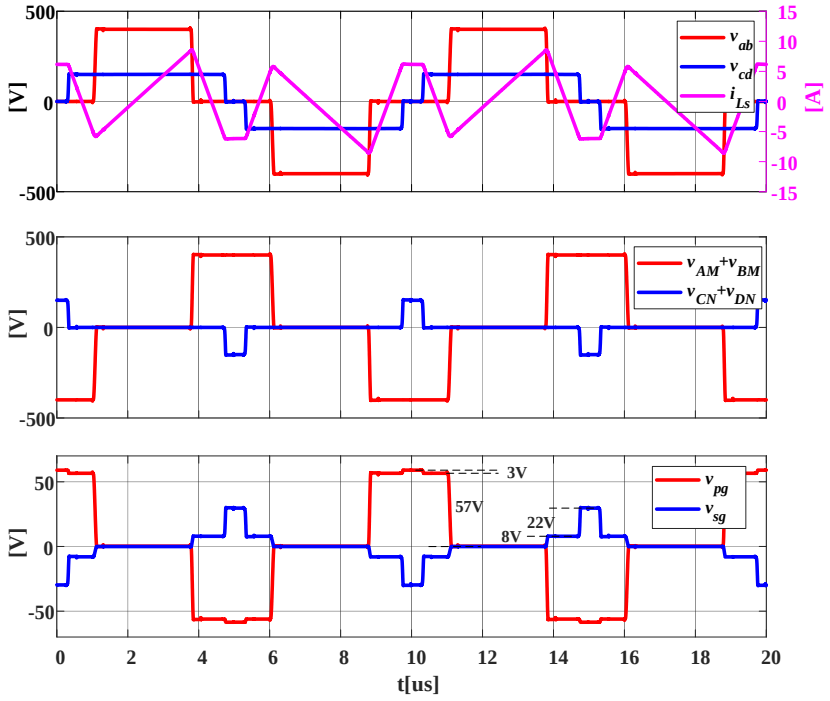


Figure 5.9. Ltspice simulation result of input and output CMV in TPS modulation @ input voltage 400V, output 150V, and 500W.

should be 2.38V and 21.73V. All numbers are aligned with the simulation result shown in Figure 5.9.

5.5 Experimental Verification

To verify the proposed DAB CM model and the influences of different modulation strategies on CM performance, an experimental setup is built, as shown in Figure 5.10. All the parasitic capacitances are measured with the impedance analyzer KEYSIGHT-E4990A at the switching frequency. The switch parasitic capacitance is measured from drain to heatsink before attaching the prototype to the copper plate, which are $C_{p2,\,3,\,5,\,6,}$ and $C_{p2,\,3,\,5,\,6}$. The transformer parasitic capacitance C_{ps} are measured between the dotted terminals, which is independent of the prototype. Once the PCB board is attached to the copper plate with the stainless-steel standoff, the DC-link capacitances are measured without transformer connections. Then the transformer should be installed, and the heatsink should be connected to the copper plate.

All experiments can be divided into two main parts. First, to verify the proposed CM model, the input and output CMV are measured. 100pF capacitors are added between the positive line and ground, and between the negative line and ground, at both input and output to serve as the parasitic capacitors in source and load. Then the CM performance under different modulation strategies is measured with LISNs. The experiments with different ZVS currents are implemented to compare the CM performances. Because of the symmetric structure of the DAB converter, to simplify the test procedure, only the output CM performance is measured.

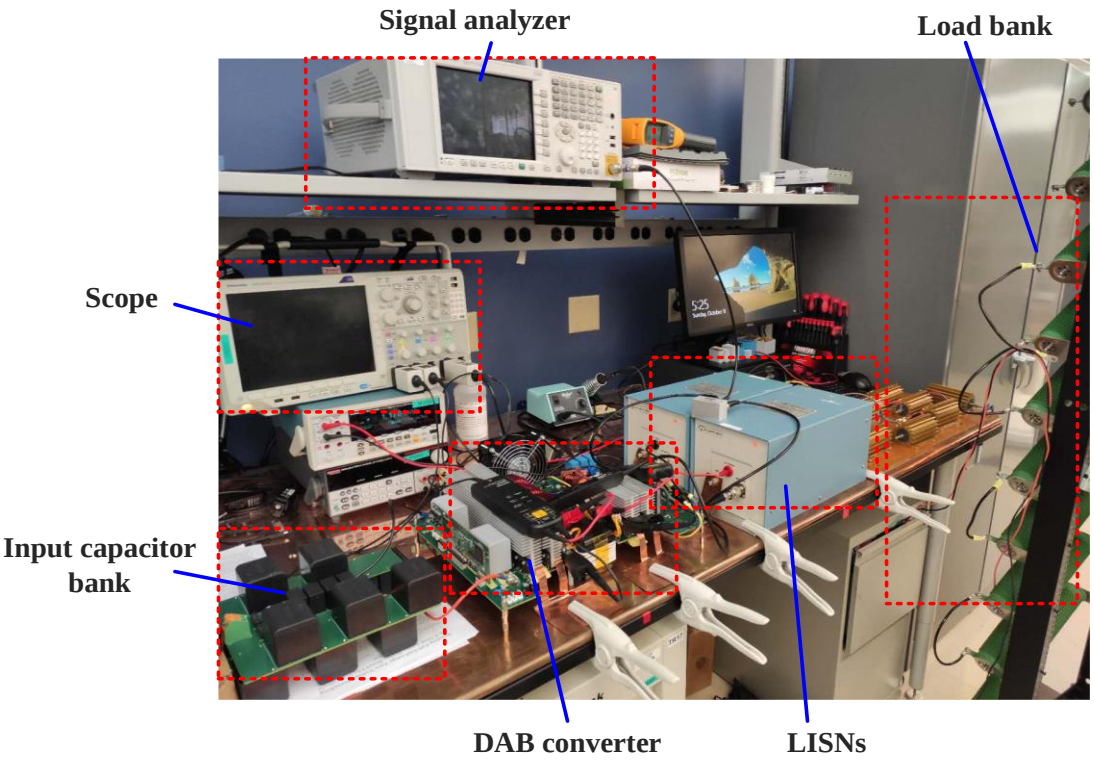


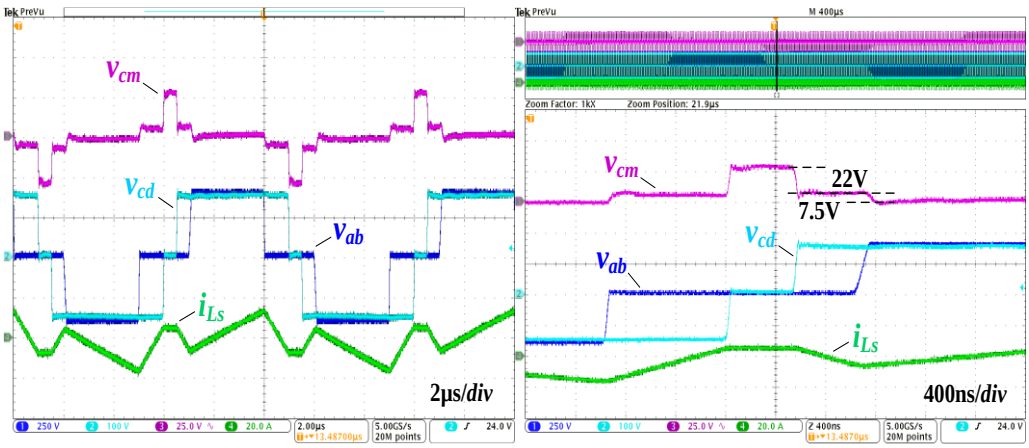
Figure 5.10. Experimental set-up.

5.5.1 Testing the CMV

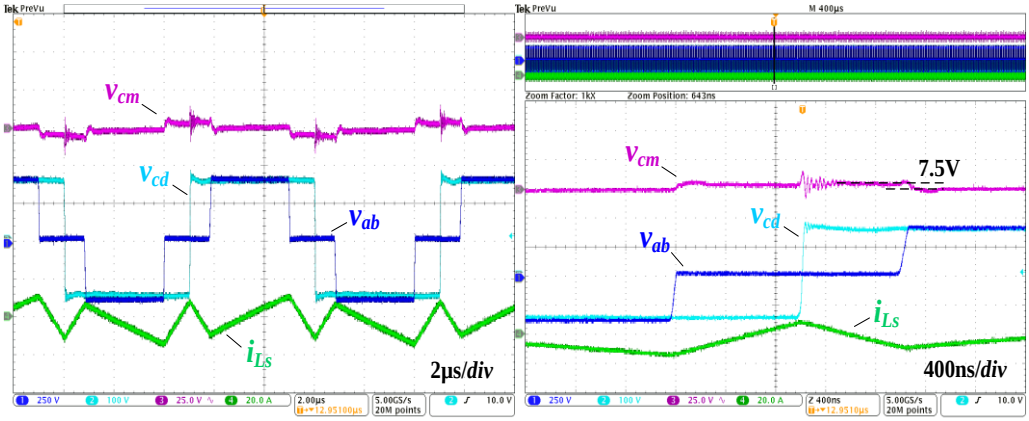
In Figure 5.11 (a) and (b), the output CMV is measured under TPS and DPS modulation, respectively, when the input voltage is 400V and the output voltage is 150V. In TPS modulation, the output voltage of the primary side and secondary side H-bridge are both three-level waveforms. According to the analysis in this chapter, the output CMV should be a five-level waveform. Based on equation (5-7), the voltage rating should be 7.95V and 21.73V. The pulse width should be corresponding to zero plateaus of the output voltage of H-bridges. The voltage waveform in Figure 5.11 (a) is consistent with the proposed analysis. For DPS modulation in Figure 5.11 (b), only the output voltage of the H-bridge at the primary side is a three-level waveform. The output CMV should be a three-level waveform with a 7.95V platform. All voltage values are shown in Figure 5.11 (a) and (b) are consistent with the calculation result of the analytical model.

When the output voltage is 250V, the experimental result is shown in Figure 5.11 (c) and (d). In TPS modulation, the output CMV is also five-level, where the platform caused by the H-bridge at the secondary side should be 36.22V based on the analytical model, which does not have a significant difference from the tested waveform. In DPS modulation, only the H-bridge at the secondary side has the inner phase shift, which can generate three-level CMV at the output. In Figure 5.11 (e), SPS modulation is implemented under 200V output voltage. There is nearly no CMV on the output side.

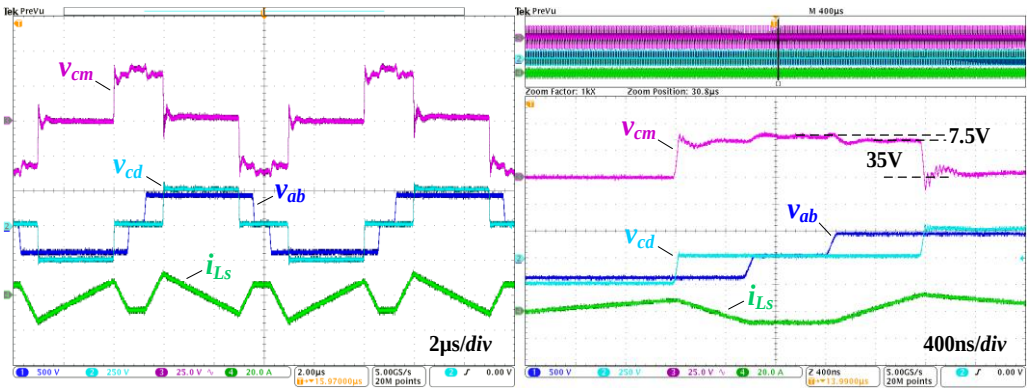
The values of the CMV sources depend on the input and output voltage. The comparisons of CMV between the calculation based on the analytical model proposed and the



(a)

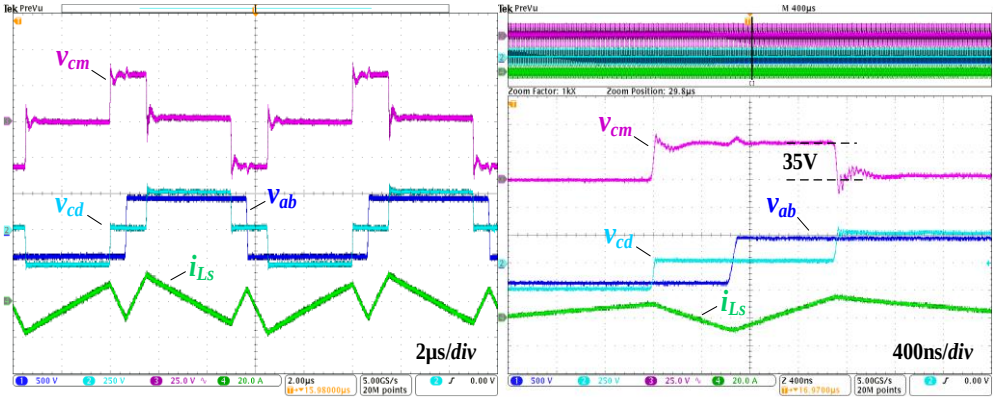


(b)

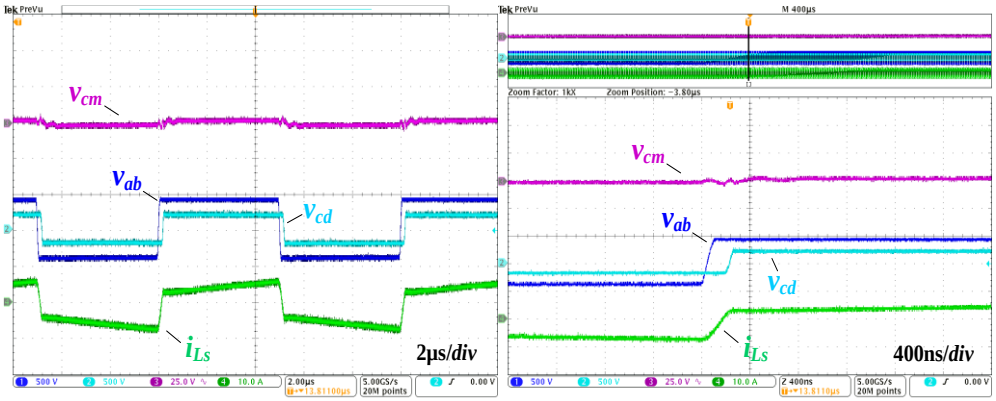


(c)

Figure 5.11. CMV in different modulation strategies: (a) TPS @ 150V output voltage: (b) PDPS @ 150V output voltage; (c) TPS @ 250V output voltage; (d) SDPS @ 250V output voltage; (e) SPS.



(d)



(e)

Figure 5.11 Continued. CMV in different modulation strategies: (a) TPS @ 150V output voltage: (b) PDPS @ 150V output voltage; (c) TPS @ 250V output voltage; (d) SDPS @ 250V output voltage; (e) SPS.

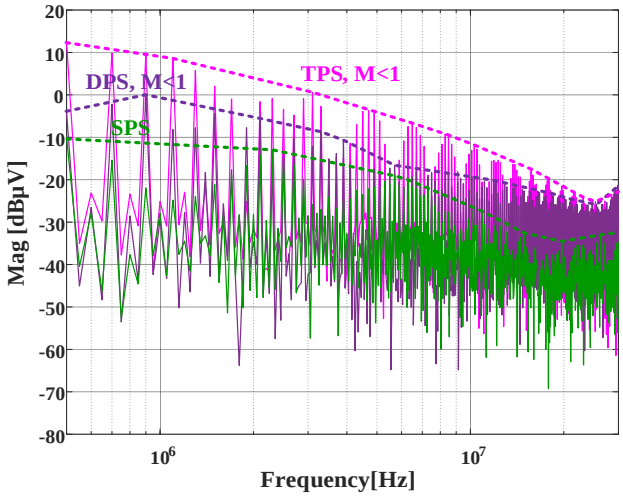
experiment under different voltage ratings are shown in Table 5.3.

Furthermore, the spectrums of the output CMV in Figure 5.11 are plotted in Figure 5.12. M here is the voltage gain, which is the reflected output voltage by input voltage divided. When M>1, the spectrums of TPS and DPS modulation are similar since the inner phase shift is added to the secondary H-bridge which dominates the output CMV. When M<1, e.g., the output voltage of 150V, the spectrum of TPS modulation has a much higher amplitude than that of DPS, given that the secondary-side H-bridge does not contribute to the CMV at DPS control while both side H-bridge contribute to CMV at TPS control. Regardless, SPS always has the lowest amplitude. Here dashed lines represent the amplitude envelope of the CMV components.

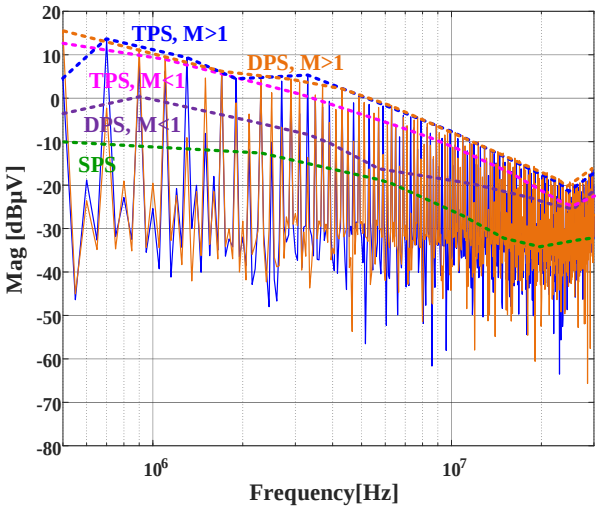
To verify the accuracy of measured parasitic capacitances and the proposed general CM topology, the comparisons of the CMV between the simulation model, as shown in Figure 5.9 using the parameters of the prototype, and the experiments are shown in Figure 5.13. The input voltage is 200V, and the output voltage is 75V, where TPS modulation is applied. The static steady DM switching waveforms are shown in the first two sub-figures. All the CM voltages across the parasitic capacitors in the proposed general topology are measured and provided in red. The corresponding simulation results in Ltspice are shown in blue. The simulation model is also used to verify the derivation of the generalized CMV model proposed in this chapter. The experimental results in Figure 5.13 are consistent with the simulation results, indicating the accuracy of the measured parasitic capacitances and the proposed CM topology.

Table 5.3. Secondary-side CMV Comparison between Analytical Model and Experiment

Modulation Strategy	Voltage Rating (V)	Platforms of output CMV	
		Calculation (V)	Experiment (V)
TPS	V_{in} 400/ V_o 150	7.95 / 21.73	≈ 7.5 / 22
	V_{in} 400/ V_o 250	7.95 / 36.22	≈ 7.5 / 35
PDPS	V_{in} 400/ V_o 150	7.95 / --	≈ 7.5 / --
SDPS	V_{in} 400/ V_o 250	-- / 36.22	≈ -- / 35
(SPS)	V_{in} 400/ V_o 190	0	≈ 0



(a)



(b)

Figure 5.12. CMV spectrums of different modulation strategies: (a) TPS, PDPS, and SPS when M<1; (b) all discussed modulation strategies.

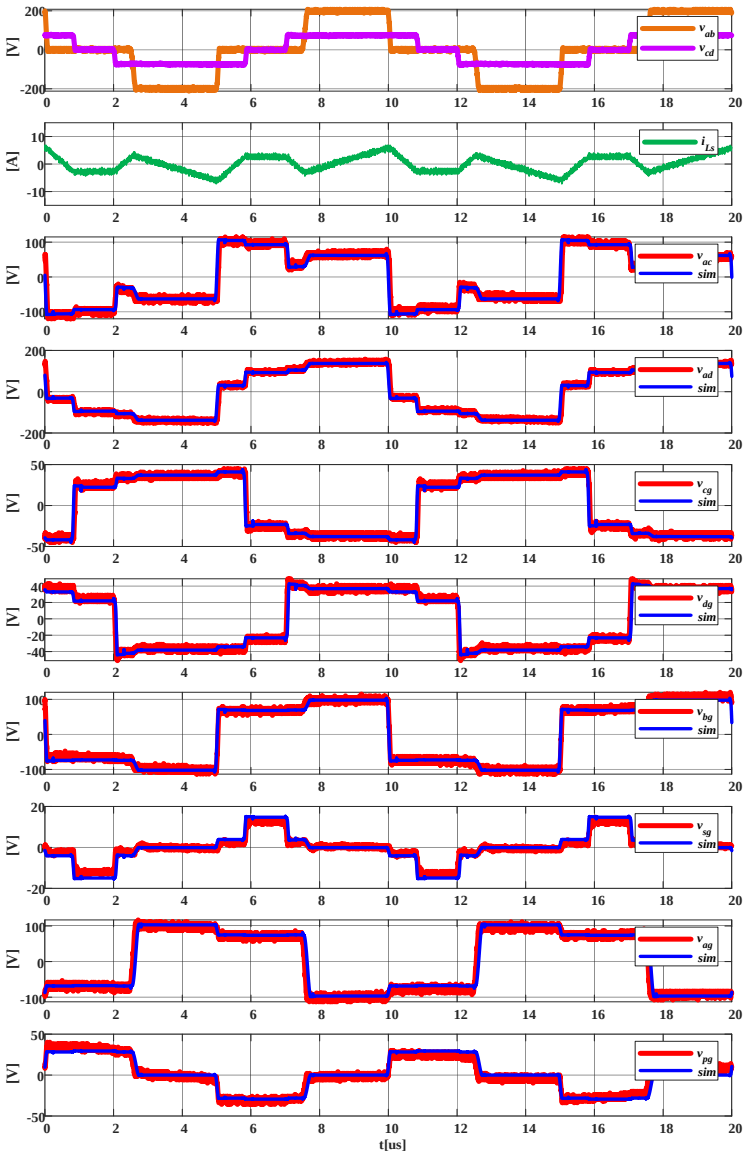


Figure 5.13. The comparison of the CMV distribution between experiments and simulation model.

5.5.2 Testing the CM Current

To further verify the analysis of the different EMI performances based on multiple phase shift modulation, Line Impedance Stabilization Networks (LISNs) are used in experiments to measure the CMI under different modulation strategies. The overall layout of the experimental setup with LISNs is shown in Figure 5.14.

With the connection of LSINs, the analytical model for the DAB converter should be further modified. The equivalent capacitance in the input source or load should be replaced with the impedance of LISNs which is composed of the impedance of C_{LISN} and 50Ω resistance in (5-13).

$$\omega C_{o\#} = \omega C_{LISN} + 50\Omega. \tag{5-13}$$

The spectrums of CMI under the different modulation strategies tested with LISNs have a similar trend as the spectrums of the CMV discussed above, as shown in Figure 5.15 (a) and (b).

5.6 The Influence of Modulation on the Common-mode Chock Design

The CM analytical model derived above is based on the equivalent capacitances at the load and the source. The CMV distribution across the different parasitic capacitors of the DAB converter in the EV chargers is then calculated. The influence of the modulation strategies on the CM performance is also proposed. For the real power electronics equipment, also needs to meet the requirements for the specific application. The proposed DAB converter research mainly focuses on the EV application, where the second stage of the output of DAB converter is directly connected with the high-voltage battery in EV,

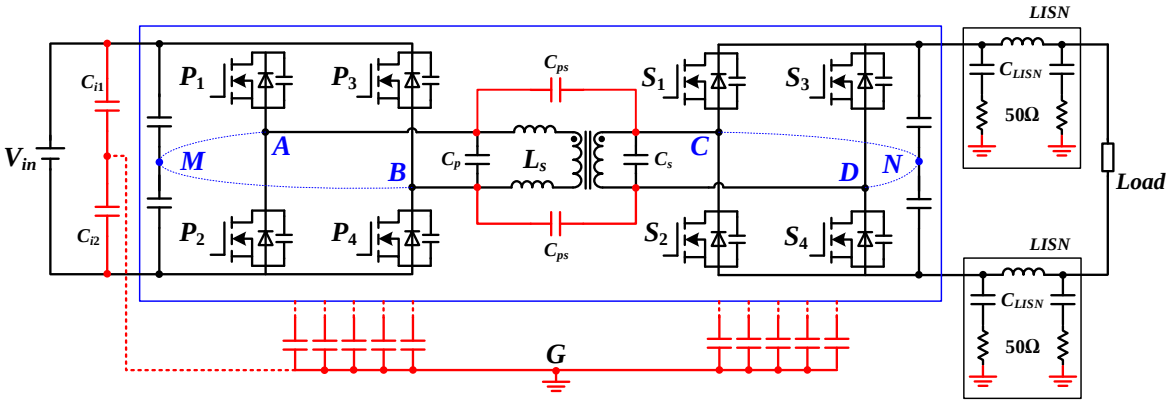
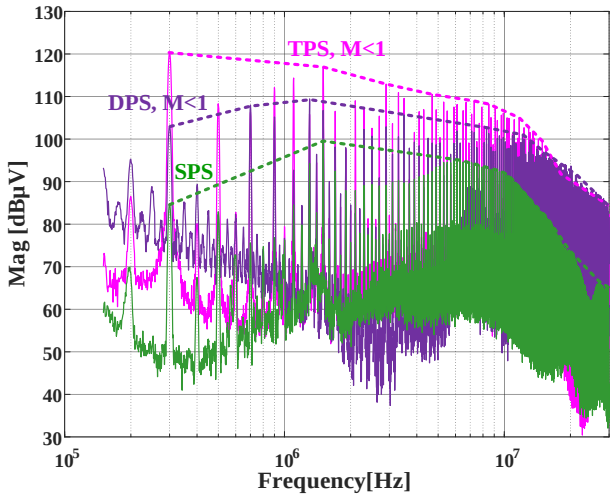
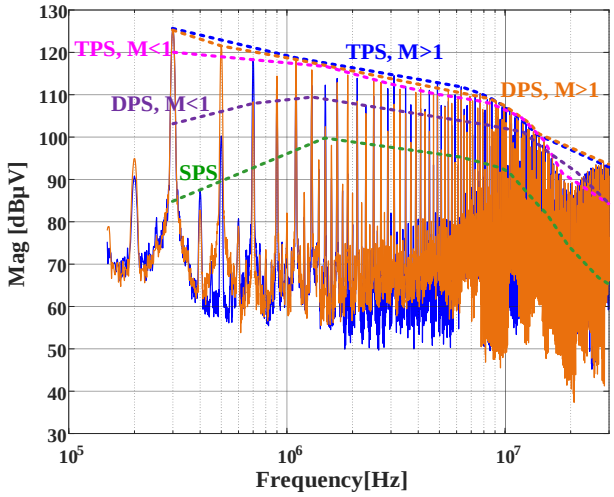


Figure 5.14. Prototype structure with LISNs.



(a)



(b)

Figure 5.15. CMI spectrums of different modulation strategies tested with LISNs: (a) TPS, PDPS, and SPS when M<1; (b) all modulation strategies.

ranging from 200V to 800V. For the safety concern in EVs, the chassis of the vehicle is grounded. The high-voltage battery is insulated with the vehicle chassis. An example of the EV high-voltage battery pack is shown in Figure 5.16.

The CM current then can flow through the parasitic capacitance between the battery and the chassis in Figure 5.17, which can cause the additional aging issue for the battery insulation. The existing standards for EV charger applications are CISPR 25 or CISPR 22. To meet the standard, the CM chock is necessary between the DAB converter and the high-voltage battery.

The designed CM chock should make sure the CM current flowing to the battery meets the standard under all the working conditions. The proposed analytical CM model can be utilized to figure out the worst case of the DAB CM performance with MPS modulation. By insetting the high-frequency voltage sources controlled by modulations into the CM model, the CM spectrum can then be predicted. Figure 5.18 is an example of the measured CM spectrum in Figure 5.15 and the corresponding model-based predicted CM spectrum envelop.

The main component in the spectrum starts from 300kHz under 100kHz switching frequency. When designing the CM chock, the component at 300kHz should be paid more attention to. With the model-based method, the 300kHz component with the different modulations can be derived. Figure 5.19 shows the 300kHz component with SDPS modulation. When the battery voltage changes with the different secondary-side inner phase shifts, the maximum magnitude of the 300 kHz component in the spectrum is 124.4

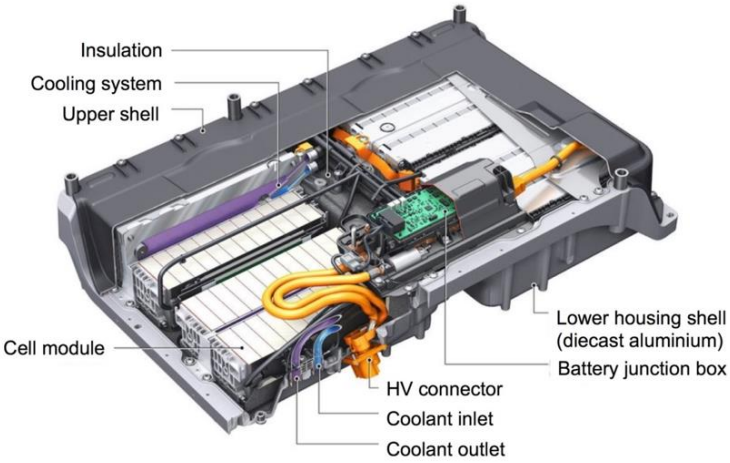


Figure 5.16. EV high-voltage pack [151].

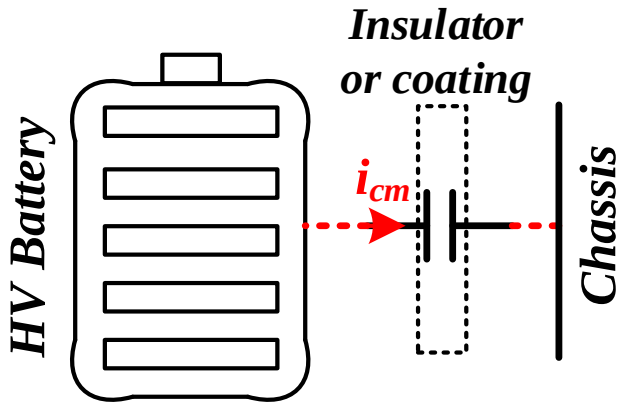


Figure 5.17. CM current flows between the high-voltage battery and vehicle chassis.

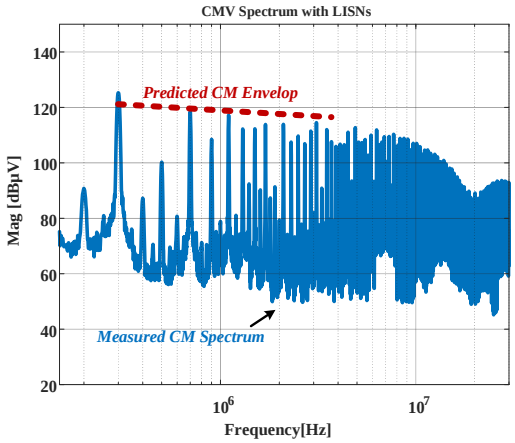


Figure 5.18. Model-based predicted CM envelop and the measured CM spectrum.

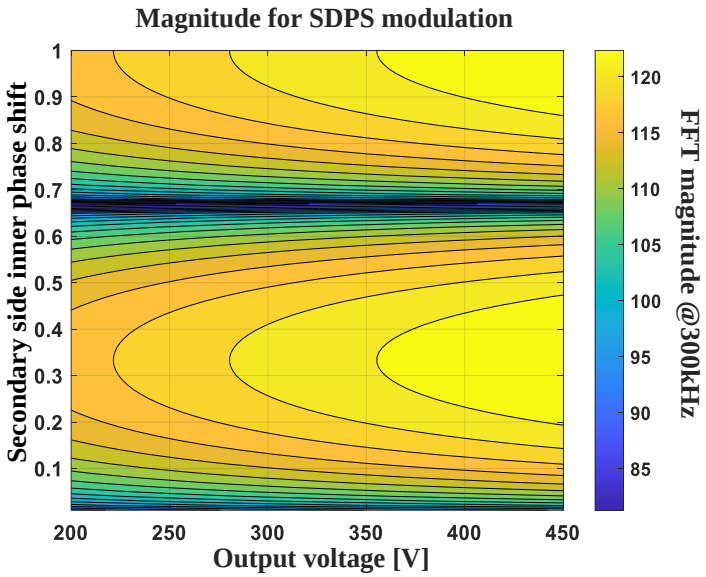


Figure 5.19. Component at 300kHz in CM spectrum with SDPS modulation.

dB. Figure 5.20 shows the 300kHz component at 450V output voltage when using MPS modulation within the whole operation range. The maximum magnitude is 124.8 dB in TPS modulation, which is the red dotted point in the figure.

Based on the CM spectrum with the maximum component at 300kHz, the CM mode chock is designed as the flow chart shown in Figure 5.21. The parameters of the different converters can be substituted for the analytical model, and the modulation method determines the CMV sources of the analytical model. In this way, the CM chock can be designed to meet the standard under the different operation conditions. A two-stage CM filter shown in Figure 5.22 is designed as an example to estimate the influence of the utilization of MPS modulation on the charger system design according to CISPR 22. The CM chock for the only SPS modulation is estimated based on the existing test result. With the consideration of the X capacitor, Y capacitor, and the CM chock, the dimension of the CM filters on board are estimated in Table 5.4. The dimension of the CM filter for MPS modulation is larger than the dimension of the CM filter with only SPS modulation. Therefore, MPS does increase the size of the CM filter, even though compared with the whole charger prototype it is still quite small.

For the designed CM filter discussed above, it needs to be applied between the output of the DC-DC converter and the vehicle interface to limit the CM noise generated by the off-board charger as shown in Figure 5.23 in case of any influence on the degradation of the battery pack insulation and the other electronic equipment in the vehicle. To prevent the potential problems, the standards need to be followed.

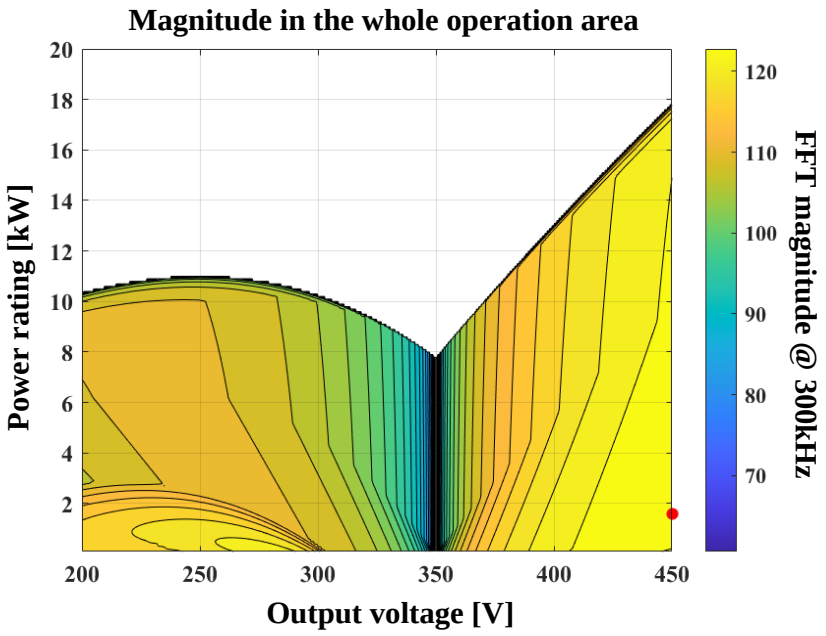


Figure 5.20. Component at 300kHz in CM spectrum with MPS modulation.

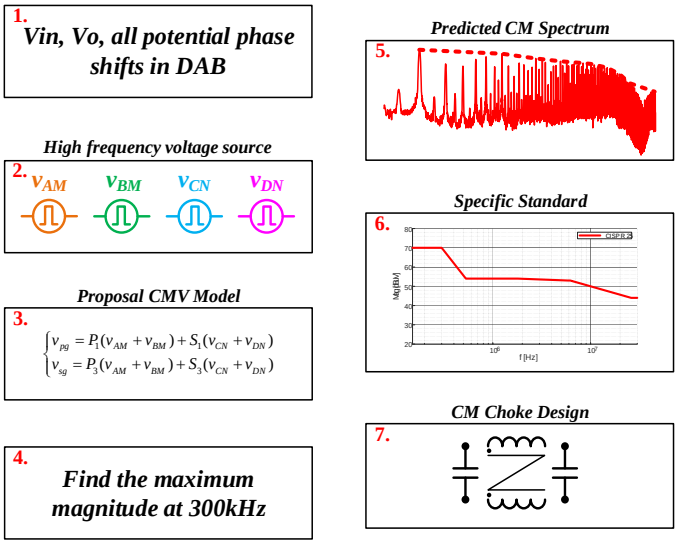


Figure 5.21. CM chock design with the analytical CM model.

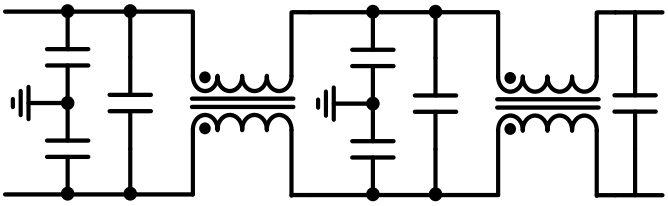


Figure 5.22. Two-stage CM filter.

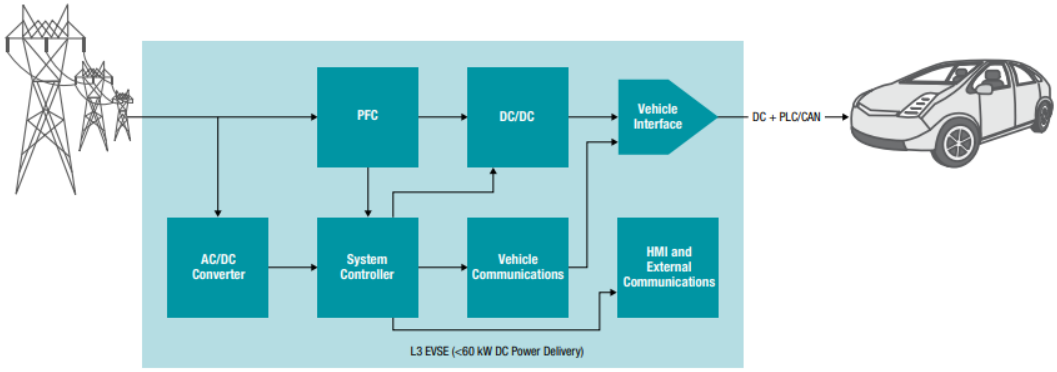


Figure 5.23. A typical block diagram of a DC charging station [14].

Table 5.4. Dimension of the CM Filter and Charger Prototype

	Filter type	Capacitance (nF)	Inductance (µH)	Dimension on Board (cm^2)	Existing prototype size (cm^2)
SPS	Two-stage	20	23	6.2 (3*2.1)	1085
MPS	Two-stage	20	175	17.2 (4.2*4.1)	

The proposed work (CM choke design guideline) is to try to meet the standards for EV applications. To provide protection for receivers installed in a vehicle from disturbances produced by the power electronics equipment, the standard should be developed and applied to any electronic component intended for use in vehicles [45]. For example, the radio spectrum is in the frequency range 9 kHz to 400 GHz [46], which covers the conducted EMI and radiated EMI. The CM current can also flow through the stray capacitance inside the vehicle to the metal chassis [152]. The leakage current may lead to the degradation or loss of the insulation material. Any single point for the failure of isolation loss does not have much impact on the operation of the system, but it does become a potential life risk when operators contact the high-voltage potentials inside the vehicle, which is a critical safety concern for EVs [153].

5.7 Conclusion

In this chapter, the analytical CMV model of the DAB converter considering different parasitic capacitance is built. The input and output CMV are derived. With the proposed calculation, its CM performances under different modulation strategies are also quantified and compared. As long as the output voltage of the H-bridge in DAB is a three-level waveform, CMV will appear. The primary side H-bridge dominates the input CMV, and the secondary side H-bridge dominates the output CMV. The parasitic capacitance between the primary and the secondary sides of the transformer couples the common-mode loops of both sides.

For phase shift controls, TPS control with inner phase shift at both primary and secondary sides has the worst common-mode performance. DPS control with inner phase shift at either the primary or the secondary side also has the considerable CMI flowing through the input or the output. SPS theoretically does not have CMV. The proposed analytical model is validated by the experiment with the CMV and CMI measured at the output under different modulation strategies. The proposed analytical model and the comparison of CM behaviors between different modulation strategies can provide a guideline when designing a CM chock for a DAB converter. For the present EV charger prototype, the dimension of the CM filter when using MPS modulation is higher than that only using SPS, though compared to the overall prototype it is still quite small.

Chapter 6 TRANSFORMER CURRENT SPIKE ELIMINATION DURING THE LOAD TRANSIENT

To accelerate the dynamic response speed in the DAB converter, feed-forward control can be applied, which is paralleled with the PI controller used for the closed-loop control. The transformer current will change significantly in the next switching cycle after the load change happens. So, the current spike and the DC offset appear during this load transient, especially, when using MPS modulation. The previous methods mainly focus on implementing the active compensation between two different steady-state operations to eliminate the transformer current spike, which however results in a complicated control structure. This chapter proposes a modulation design method unifying the transformer current for DPS and TPS modulation to mitigate the transformer current spike when switching between DPS and TPS during load transient. By applying the proposed PWM strategy, the transformer current is the same at the beginning of the switching period in different steady-state modulations, resolving the transformer current spike and DC offset fundamentally. The full-operational-range zero-voltage switching (ZVS) is also realized for the primary or secondary side by combining with the proposed modulation strategy. The experiments are also carried out for further validation.

6.1 Root Cause of the Current Spike in Transformer

The output current of the DAB converter is regulated by the phase shift between the primary-side and secondary-side H-bridges. When the load current transient happens, to track the reference current the phase shift needs to change fast enough. To accelerate the

dynamic response speed, feed-forward control is commonly applied paralleled with the PI controller. Figure 6.1 shows the structure of the closed-loop control for a DAB converter. Also, based on the implementation of MPS modulation the phase shift between the primary side and the secondary side determines the inner phase shifts associated with the input voltage and the output voltage.

A simulation example of the load current transient is provided in Figure 6.2. The simulation parameters are shown in Table 6.1, which is also the test condition for the control algorithm in the lab. To verify the proposed modulation strategy, the experiments are adopted at low voltage conditions. During the transient the reference current increases. A new phase shift will be uploaded to the DAB converter in the next switching cycle. Under light load, TPS modulation is applied to secure ZVS and reduce the reactive power. At medium load, DPS modulation is adopted. During the transition between TPS and DPS when the load current increases, the current spike appears in the transformer.

The root for the transformer current spike lies in the continuity of the transformer current and the discontinuous phase shift. Typically, the new phase shift is imposed on the switches at a certain point of the switching cycle, which is set by the micro-control unit (MCU). If setting the uploading point when the primary-side switching action happens as shown in Figure 6.3 (a), the transformer current at the switching point is provided in (6-2), and the current difference is also listed in (6-3). The switching current in SPS modulation is only related to the phase shift between the primary side and the secondary side, which means the switching current is determined by the load under certain voltage conditions. But under

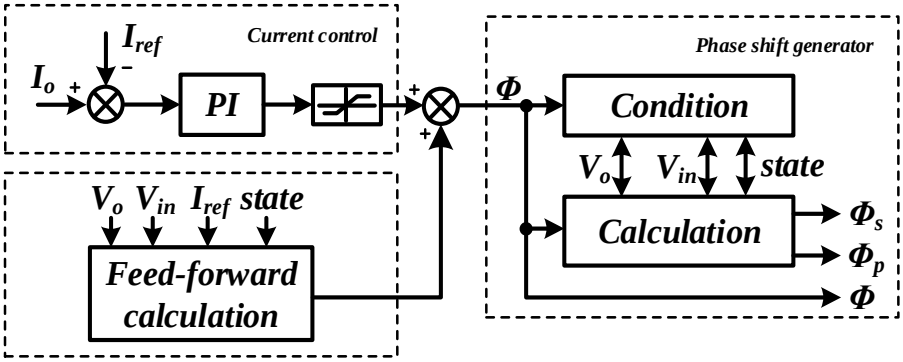
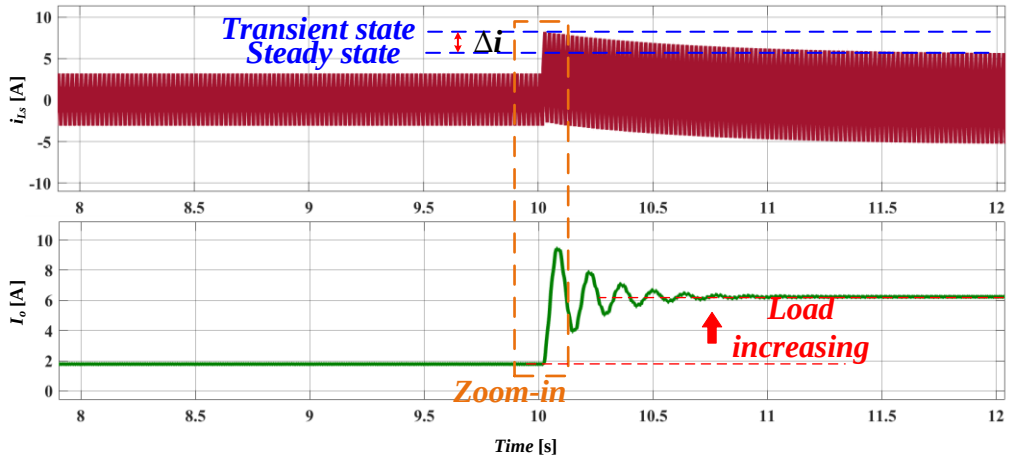


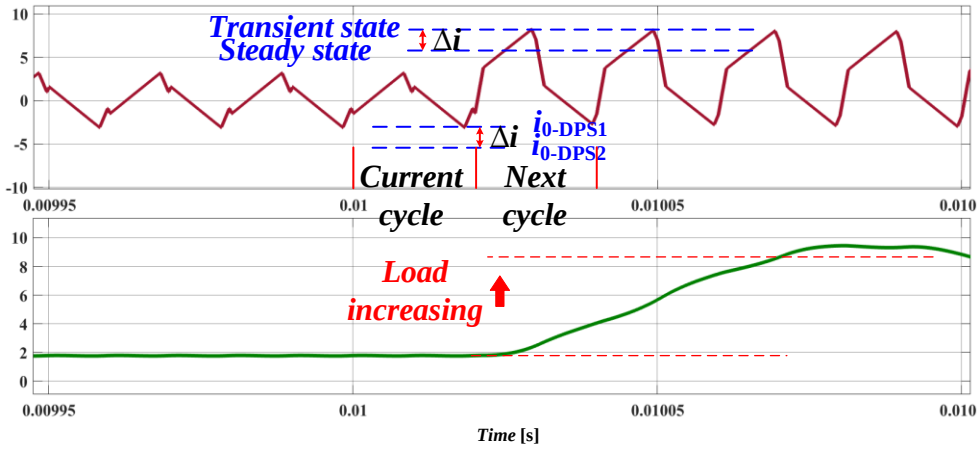
Figure 6.1. The structure of the closed-loop control in the DAB converter.

Table 6.1. Prototype Setup.

Symbol	Value	Name	Value
Input voltage	80V	Turn ratio	2
Output Voltage	30~50V	Inductance	36μH
Switching frequency	50kHz	--	--

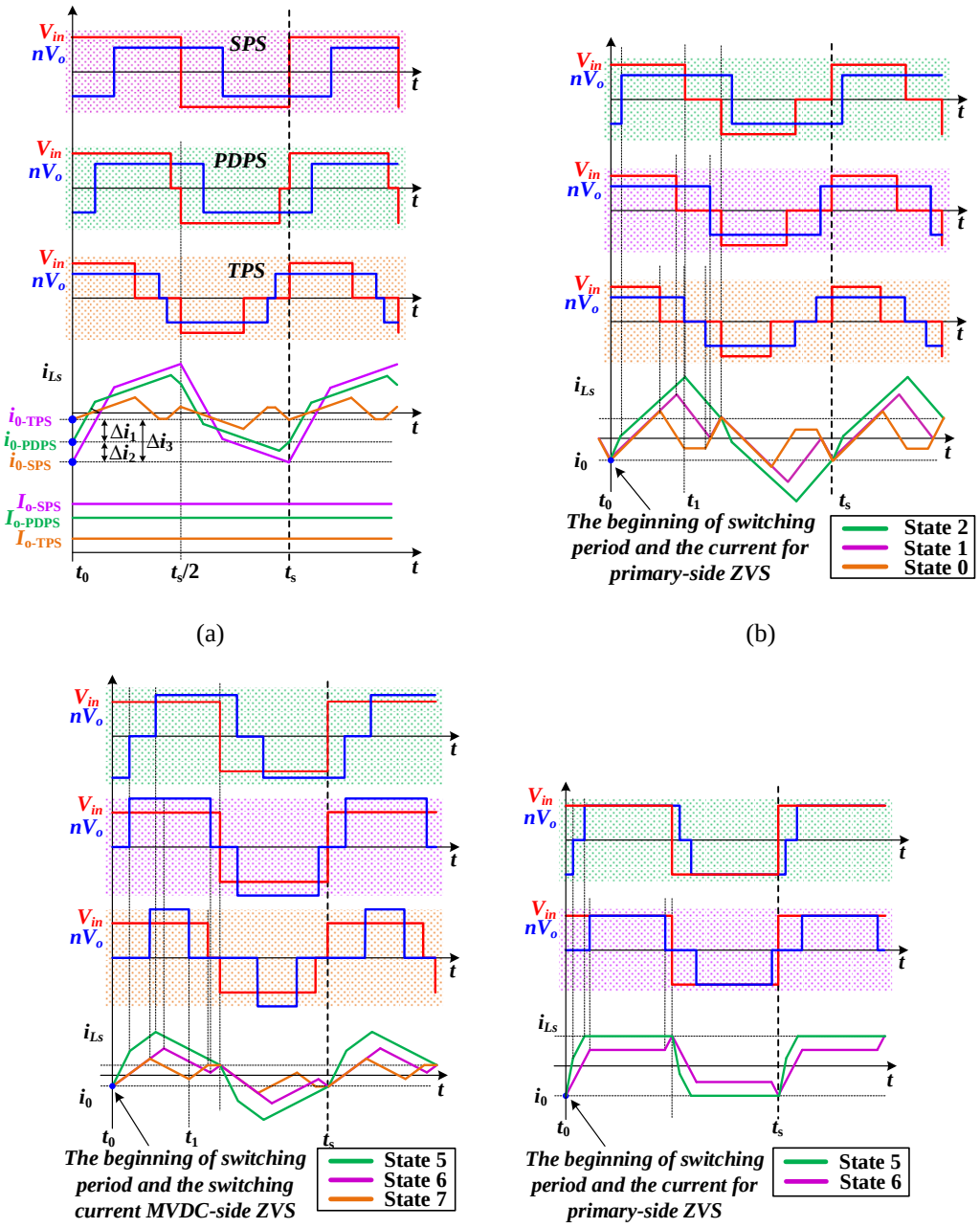


(a)



(b)

Figure 6.2. Simulation waveform during load transient with the transformer current spike: (a) load current increasing with the current spike in the transformer; (b) zoomed-in waveforms.



(a) (b)

(c) (d)

Figure 6.3. The switching waveform of the proposed modulation strategies: (a) the modulations without the unified switching current; (b) PDPS and TPS when $V_{in}>nV_o$; (c) SDPS and TPS when $V_{in}<nV_o$; (d) SDPS when $V_{in}=nV_o$.

DPS and TPS modulation, because of the additional inner phase shifts, the switching current is more flexible. It is adjustable by limiting the relationship between different phase shifts.

Therefore, if the switching currents at the beginning of the switching period under different conditions are the same, there will be no transformer current spike even if the phase shifts change fast. When the load transient happens between TPS and DPS modulation, there is no need for the additional active compensation as shown in the previous literature. Considering the load transient between SPS and other modulations, because of the unified switching current of DPS and TPS, other modulations can be regarded as a single pattern to be compensated, which simplifies the current spike control.

6.2 Unified Transformer Current in Multiple Phase Modulation

As mentioned above, the transformer current at a certain switching point of DPS and TPS modulations can be unified by adjusting the inner phase shifts. This switching current can keep the same under different load conditions and modulations. Meanwhile, if the selected switching action is corresponding to the primary-side switches, and if the value of the current setting is large enough, it can also realize ZVS for the primary side in the full-load range. Following this theory, the designed modulation strategies are shown in Fig. 6.

To fulfill the minimum initial current requirement to realize ZVS for the primary-side switches under different modulations, the transformer current at t_0 should be

$$I_{ZVS0}(V_o) \geq \sqrt{\frac{4Q_{oss}(V_{in})nV_o}{L_s}} \tag{6-1}$$

$$\begin{cases} i_{0_SPS} = -\dfrac{V_{in} + nV_o(2\phi - 1)}{4L_s f_s} \\ i_{0_PDPS} = -\dfrac{V_{in}\phi_p + nV_o(2\phi - 1)}{4L_s f_s} \\ i_{0_TPS} = -\dfrac{V_{in}\phi_p - nV_o(\phi + \phi_s)}{4L_s f_s} \end{cases} \tag{6-2}$$

$$\begin{cases} \Delta i_1 = \dfrac{nV_o(3\phi + \phi_s - 1)}{4L_s f_s} \\ \Delta i_2 = \dfrac{V_{in}(1 - \phi_p)}{4L_s f_s} \\ \Delta i_3 = \dfrac{V_{in}(1 - \phi_p) + nV_o(3\phi + \phi_s - 1)}{4L_s f_s} \end{cases} \tag{6-3}$$

When the input voltage is higher than the reflected output voltage, to unify the switching current in different modulations, the transformer current at the beginning of the switching period should be the same as (6-1).

$$i_{0_PDPS} = i_{0_TPS0} = I_{ZVS0}(V_o) \tag{6-4}$$

$$\begin{cases} PDPS1(\phi < 0) : \phi_p = \dfrac{4L_s f_s I_{ZVS0} + nV_o(1 + 2\phi)}{V_{in}} \\ PDPS2(\phi \geq 0) : \phi_p = \dfrac{4L_s f_s I_{ZVS0} + nV_o(1 - 2\phi)}{V_{in}} \end{cases} \tag{6-5}$$

The primary side inner phase shift in DPS modulation is derived in (6-5), according to (6-2) and (6-4).

At light load, to realize ZVS for the secondary-side switches the transformer current at t_1 should be large enough by varying the inner phase shifts. The switching waveform of the designed modulations is shown in Figure 6.3 (b).

$$TPS0:\begin{cases}\phi_p=\dfrac{nV_o(1+D)+2L_sf_s(I_{ZVS0}-I_{ZVS_t1})}{V_{in}}\\ \phi_s=\dfrac{nV_o-2L_sf_s(I_{ZVS0}+I_{ZVS_t1})}{nV_o}\end{cases} \tag{6-6}$$

The relationship between the phase shift and the output current in different modulations is shown in Figure 6.3 (a). However, with the phase shift increasing, the output current is not monotonically increasing in PDPS2 before switching to SPS. An additional DPS modulation is then designed to realize a seamless transition between PDPS and SPS modulation, as formulated in (6-7) and plotted as the dashed line in Figure 6.4 (a).

$$PDPS3:\phi_p=\frac{2V_{in}\phi+nV_o-4L_sf_sI_{ZVS}}{V_{in}} \tag{6-7}$$

When the input voltage is lower than the reflected output voltage, the inner phase is inserted among the secondary-side switches. The switching waveforms are shown in Figure 6.3 (c). To unify the transformer current at the beginning of the switching period, the inner phase shift at the secondary-side H-bridge in SDPS modulation is

$$\begin{cases}SDPS5(\phi\geq 0):\phi_s=\dfrac{4L_sf_sI_{ZVS0}+nV_o(2-\phi)-V_{in}}{nV_o}\\ SDPS6(\phi<0):\phi_s=\dfrac{4L_sf_sI_{ZVS0}+nV_o(2+\phi)-V_{in}}{nV_o}\end{cases} \tag{6-8}$$

In TPS modulation, to realize ZVS for the secondary-side switches, the switching current at t_1 should also be large enough to finish the ZVS transition. To meet the requirements of the unified transformer current and the ZVS current, the inner phase shifts are

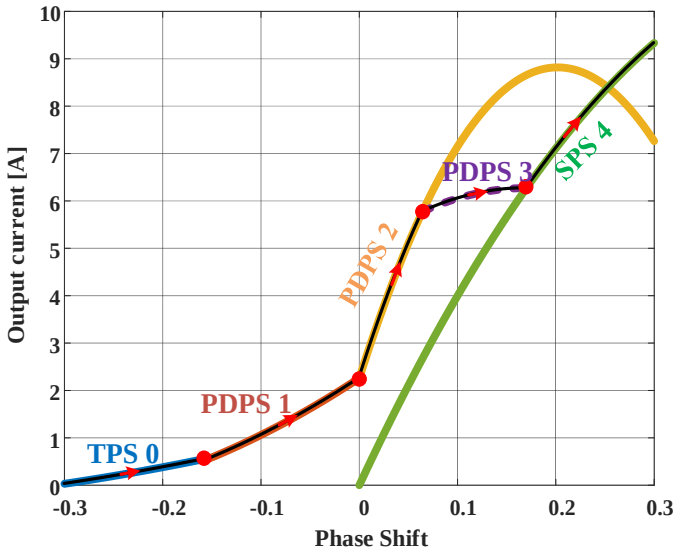
$$TPS7:\begin{cases} \phi_p = \dfrac{V_{iu}(1+\phi)+2L_s f_s(I_{ZVS0}+I_{ZVS_t1})}{V_{in}} \\ \phi_s = 2+\phi+\dfrac{2L_s f_s(I_{ZVS0}-I_{ZVS_t1})-V_{in}(1+\phi)}{nV_o} \end{cases} \tag{6-9}$$

The relationship between the phase shift and output current is shown in Figure 6.4 (b) among TPS, SDPS, and SPS modulations. The proposed modulations with the unified transformer current can operate under the different voltage gains and load conditions.

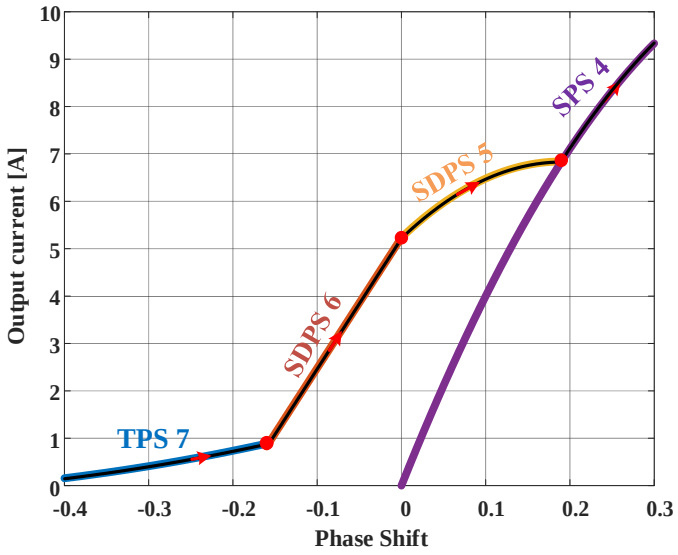
6.3 Active Compensation Between Different Patterns

By implementing the proposed modulation strategy, there is no current spike during the load current transient when using DPS and TPS modulation. However, the switching current of SPS modulation is decided by the load because there are no flexible inner phases. Hence the current spike elimination for SPS also needs to be considered. Owing to the unified switching current by the proposed modulation, the transformer current is the same under different DPS and TPS, which can be integrated as a single pattern when designing active compensation. Figure 6.5 (a) shows the distribution of the different modulation strategies. Case 1 is the operational area with SPS. Case 2 is the operational area with PDPS3 used for a seamless transition in a steady state. Case 3 is the DPS and TPS modulations with the unified transformer current.

To simplify the current-spike elimination method, the compensation process focuses on the first half switching cycle in the next switching period as shown in Figure 6.5 (b) when the load current increases. By limiting the time interval of the rising transformer current,

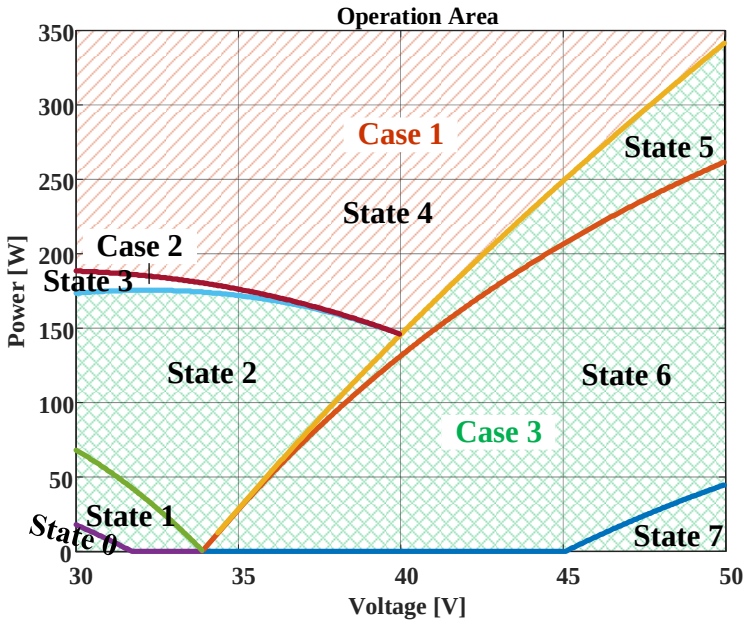


(a)

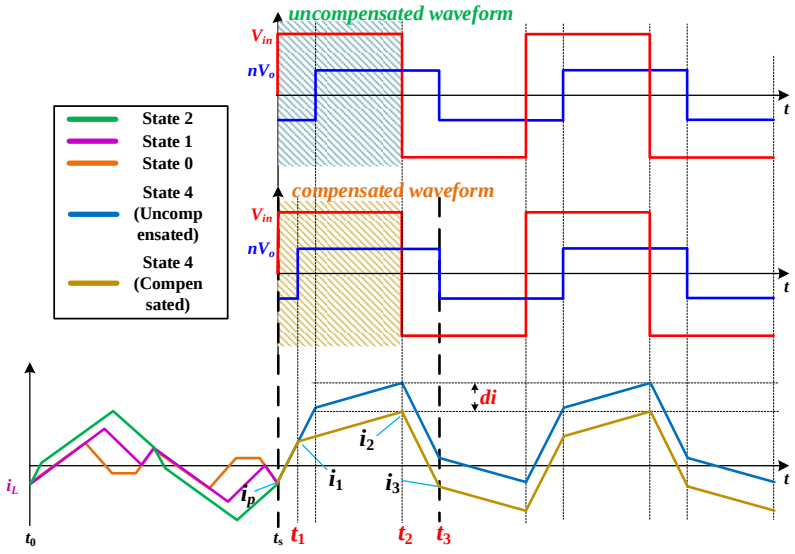


(b)

Figure 6.4. Example of phase shift vs output.



(a)



(b)

Figure 6.5. Transformer current spike elimination strategy: (a) Operational area for different modulations; (b) example of the active compensation between SPS and other modulations.

the transformer current spike can be mitigated. The same method can also be applied when the load current decreases.

6.4 Duty Cycle Compensation to Eliminate Current Spike

When the load transient happens between different cases shown in Figure 6.5 (a), the active compensation method is still needed to prevent any transformer current spike, particularly for SPS modulation where the phase shift is only related to the power and the voltage. An intermediate state is necessary between the different cases as shown in Figure 6.6. In this section, the example of how to design the active compensation method is discussed when the input voltage is higher than the reflected output voltage.

6.4.1 Load Current Increasing

As discussed in the last section, there are four modulation strategies to cover the full-load-range operation when $V_{in} > nV_o$. Typically, P_1 is set as the time reference for all phase shifts. TPS control and PDPS2 control have the same switching current at t_0. Therefore, they can be categorized as the same group in terms of the current spike elimination.

When the modulation strategy switches from TPS to SPS, to eliminate the positive current spike, the first interval needs to be limited, as shown in Figure 6.6 (a). The current at the endpoint of TPS is I_r, which is the ZVS current for primary-side switches. In the first half switching period, switching actions at t_1 can be adjusted to limit the spike current. Meanwhile, the current at t_2 should reach the steady-state value to make sure a smooth

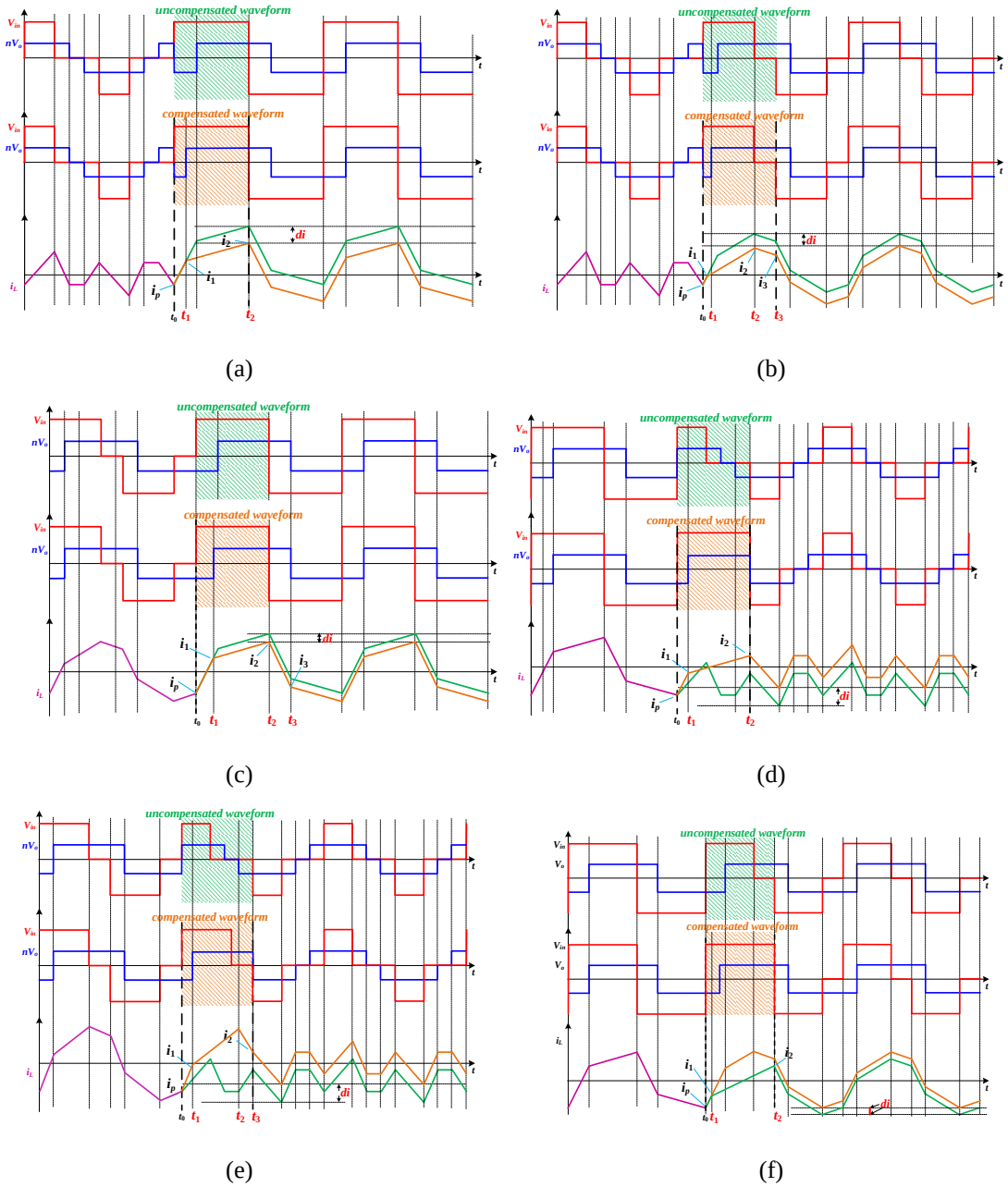


Figure 6.6. Current Spike elimination: (a) modulation switching from TPS to SPS (light load to heavy load); (b) modulation switching from TPS to PDPS (light load to medium load); (c) modulation switching from PDPS to SPS (medium load to heavy load); (d) modulation switching from SPS to TPS (heavy load to light load)); (e) modulation switching from PDPS to TPS (medium load to light load)); (f) modulation switching from SPS to PDPS (heavy load to medium load).

transition between the TPS and SPS control. To adjust the time interval from t_0 to t_1, duty cycles of S_1 ~S_4 need to be calculated based on the equation below.

$$\begin{cases} t_1 = t_0 + \dfrac{com}{2 f_s} \\ com = \dfrac{nV_o + V_{in}(\phi - \phi_p) + 2L_s f_s (I_r - I_{r1}) + nV_o\phi}{2nV_o} \end{cases} \tag{6-10}$$

By using a similar method, the current spike can also be eliminated when switching between other modulations. Figure 6.6 (b) shows the current spike elimination from TPS to DPS1. In the next switching period, the inner phase shift of the primary-side H-bridge is kept the same. The duty cycles of secondary-side switches, however, need to be modified. The time interval from t_0 to t_1 which needs to be compensated is

$$com = \frac{nV_o - V_{in} + 4L_s f_s I_r + 2nV_o\phi}{4nV_o} \tag{6-11}$$

Furthermore, when the modulation strategy switches from DPS to SPS, the designed compensation waveform is shown in Figure 6.6 (c). There is no inner phase shift at the primary-side H-bridge in the next half switching cycle. The compensation time interval from t_0 to t_1 is

$$com = \frac{nV_o + V_{in}(\phi_1 - 1) + 2L_s f_s (I_r - I_{r1}) + nV_o\phi_1}{2nV_o} \tag{6-12}$$

6.4.2 Load Current Decreasing

In the transient process, there could be a negative DC offset in the transformer current. For example, the current at the endpoint of SPS modulation is smaller than the current at

the starting point of TPS modulation in the steady state. To make sure the switching current at the end of the half switching cycle is the same as the current in the next period, the transformer current needs to increase to the desired value by adjusting the relationship between t_1~t_0 and t_2~t_1, as shown in Figure 6.6 (d). The first interval from t_0 to t_1 is

$$com = \frac{nV_o - V_{in} + 2V_{in}\phi_1 - 4L_s f_s I_{r1} + 2nV_o(\phi + \phi_1)}{4nV_o} \tag{6-13}$$

When the modulation strategy switches from DPS to TPS control, there is also a negative DC offset current appearing in Figure 6.6 (f). To eliminate such negative current DC offset, the inner phase shift at the primary-side H-bridge keeps the same as the last switching cycle. By changing the duty cycle in the next half switching cycle, the transformer current can have enough time to rise to counterpart the negative DC offset. The calculated time interval from t_0 to t_1 is

$$com = \frac{nV_o - V_{in} + 4L_s f_s I_r + 2nV_o\phi_1}{4nV_o} \tag{6-14}$$

Finally, to mitigate the potential negative DC offset when switching from SPS to DPS, the compensation method can also be applied to secondary-side switches in Figure 6.6 (f). The necessary time interval from t_0 to t_1 is

$$com = \frac{nV_o + V_{in}(1 + 2\phi - 2\phi_p) - 4L_s f_s I_{r1} + 2nV_o(\phi_1 + \phi)}{4nV_o} \tag{6-15}$$

By applying modified duty-cycle control to different switches, the transformer current spike, as well as the DC offset during the load change, is eliminated.

6.5 Control Algorithm Implementation

The structure of the control loop in a DAB converter is shown in Figure 6.7. The operation mode can decide if the regulated objective is the output voltage, output current, or output power. The state machine can decide which modulation strategy is going to be implemented in the next switching cycle based on the input voltage, output voltage, and the output of the PI controller, which is the phase shift between the primary side and the secondary side. The boundary conditions discussed above can specify when it is necessary to switch modulation strategies. Then, based on the modulation strategy and the phase shifts in the current and next switching periods, the compensated duty cycle is calculated. A PWM generator will provide square waveforms for all switches with a 50% duty cycle. Modified duty cycles will then be applied to certain switches. Finally, a microcontroller generates PWM signals to all switches.

The detailed duty-cycle calculation and compensation process are shown in Figure 6.8. In Figure 6.8 (a), as mentioned above, when the modulation strategy switches to another one, the duty-cycle compensation method is going to be triggered. An example of the modification for S_1 and S_2 is shown in Figure 6.8 (b). The duty cycle of S_1 is enlarged resulting in the time interval between t_0 and t_1 being reduced.

6.6 Experimental Verification

To validate the proposed modulation, the experiments are carried out based on the test conditions shown in Table 6.1. Without the duty-cycle compensation method, Figure 6.9 (a) shows that the current spike in the transformer appears when the load current suddenly

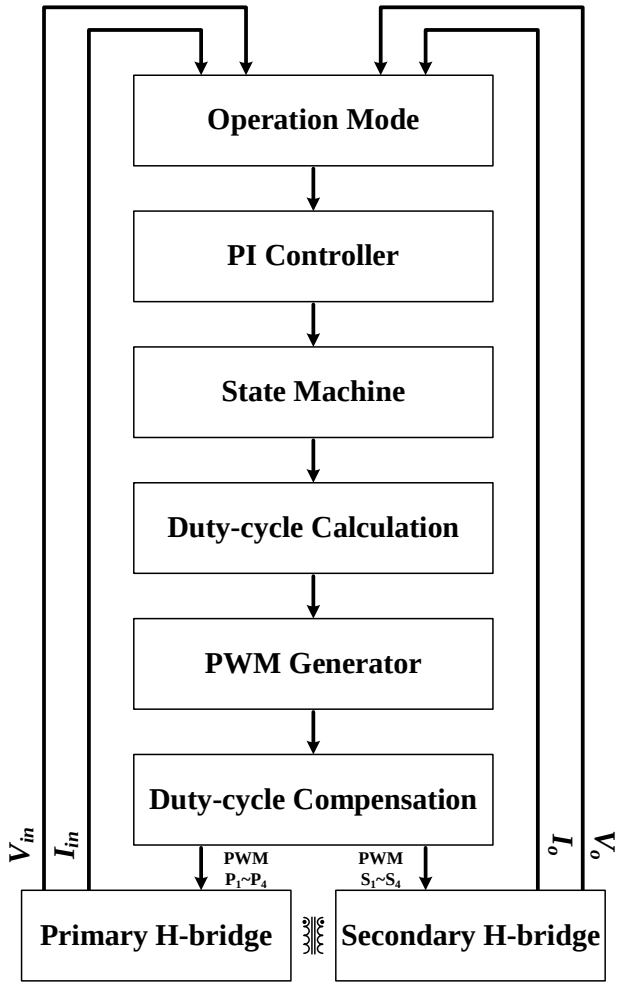
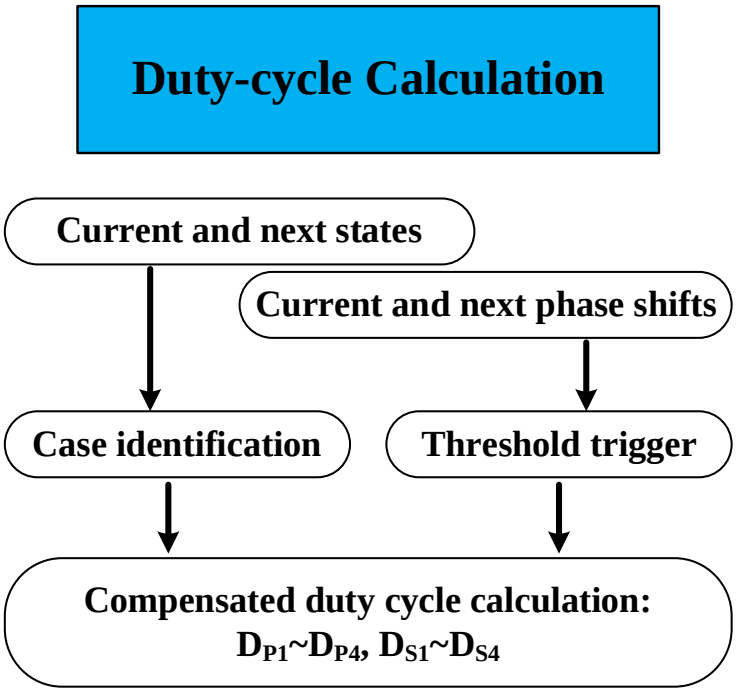
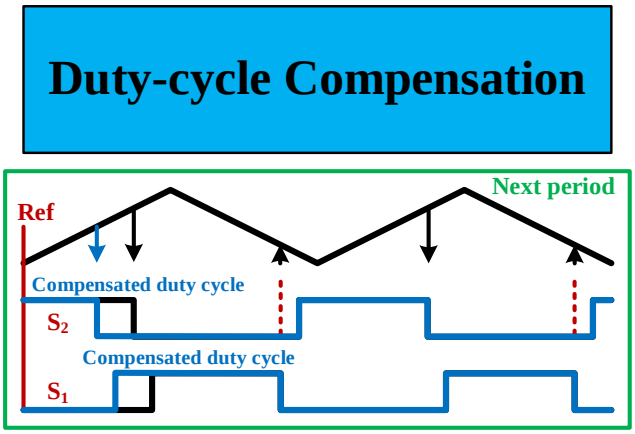


Figure 6.7. Structure of the control loop in DAB.

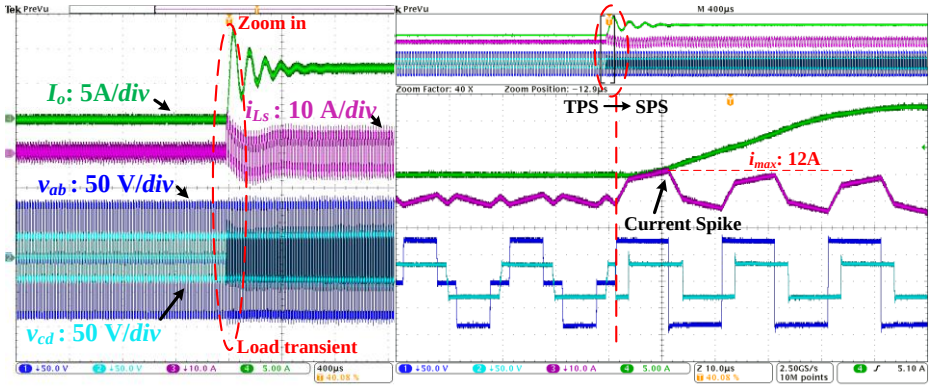


(a)

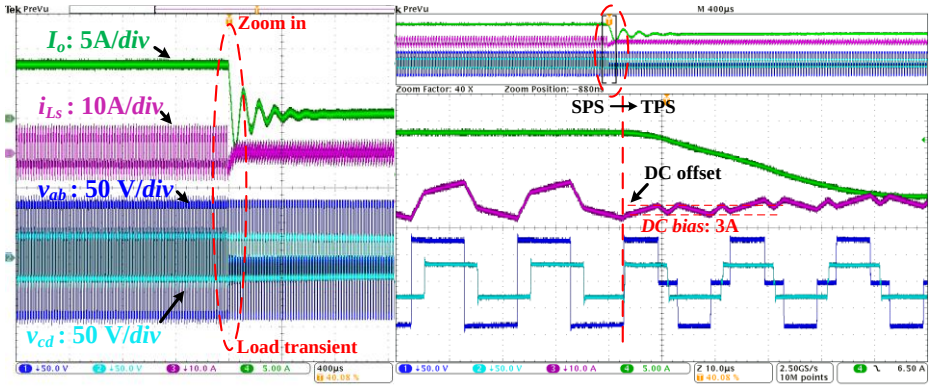


(b)

Figure 6.8. Duty-cycle compensation method: (a) calculation of duty cycle; (b) implementation of compensation duty cycle.



(a)



(b)

Figure 6.9. Transformer current spike when step change of phase shift happens, without the duty cycle compensation: (a) from TPS to SPS; (b) from SPS to TPS.

increases. The maximum current during the load transient is 12A, which is 5A higher than the current at the steady-state current. Figure 6.9 (b) shows the negative current DC offset in the transformer when the load current suddenly decreases. The transformer current DC offset in the next switching cycle after the load transient is around 3A.

For the load transient with the modulations switching between TPS and DPS, the proposed modulation strategy does not have the transformer current spike even without considering any active compensation. For the load transient between TPS/DPS and SPS, with the designed active compensation method the potential transformer current spike is also eliminated. The experiment results are shown in Figure 6.10 (a)~(f). The experimental results are shown in Figure 6.11 (a) and (b) are the experiments during the load transient when $V_{in} = nV_o$. In all the experiments, the primary-side switches can realize ZVS no matter the load condition within the wide secondary-side voltage range.

6.7 Conclusion

The transformer current spike is a common issue during the load transient in the DAB converter. The special compensation methods are developed in the previous research by adjusting the certain switches' duty cycle to mitigate the current spike. Especially, when using MPS modulation to improve the steady-state performance, the compensation method becomes much more complicated because of the different transformer current, which is independent of the steady-state operation. In this chapter, the elimination of the transformer current spike is considered when designing the steady-state modulation by unifying the transformer current in DPS and TPS modulation. In this case, there is no current spike

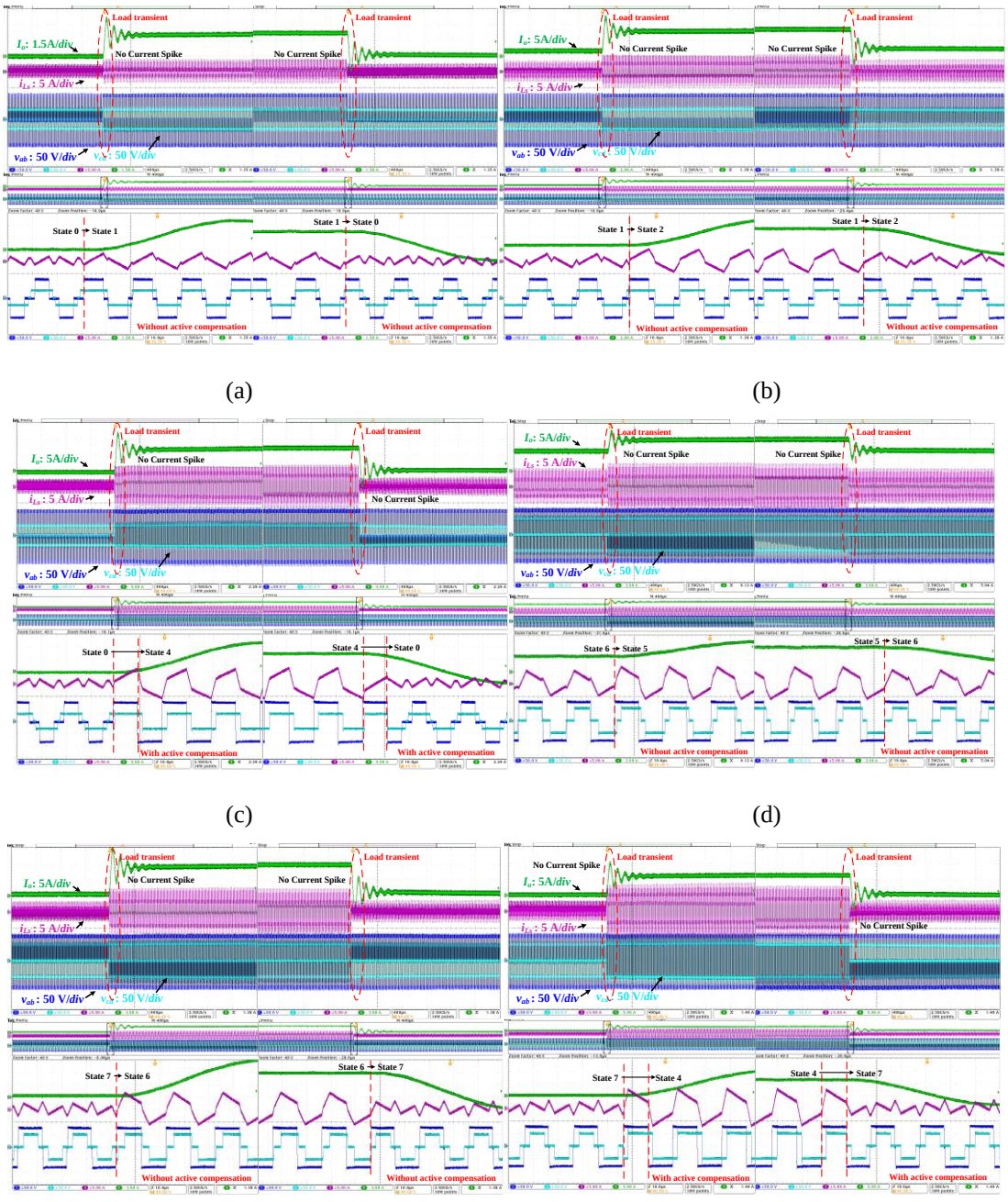
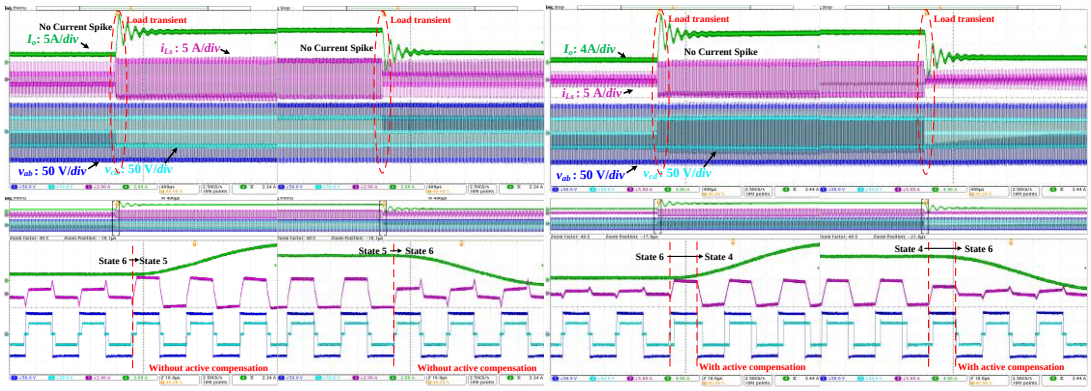


Figure 6.10. Experimental waveforms during load transient: (a) TPS0 to PDPS1 without active compensation; (b) PDPS1 to PDPS2 without active compensation; (c) TPS0 to SPS with active compensation; (d) TPS7 to SDPS5 without active compensation; (e) TPS7 to SDPS6 without active compensation; (f) TPS7 to SPS with active compensation.



(a) (b)

Figure 6.11. Experimental waveforms during load transient: (a) SDPS6 to SDPS5 without active compensation; (b) SDPS6 to SPS with active compensation.

fundamentally during the load transient between DPS and TPS modulations. Also, the compensation between SPS and other modulations is simplified because of the unified transformer current. Meanwhile, the proposed modulation strategy utilizes the unified current to realize ZVS for the primary-side switches throughout the whole operational range. Finally, the performance of the proposed modulation is validated by the experiments.

Chapter 7 CONCLUSION AND FUTURE WORK

Based on the work discussed in chapters 1~6, the conclusions of this thesis are summarized below. The potential work worth exploring in the future is also discussed in this chapter.

7.1 Conclusions

This thesis discussed the implementation of MPS control in the DAB converter.

(1) By applying MPS control, ZVS can be realized in the full operational range. When the boundary conditions between different modulation strategies are well defined, a smooth transition can be achieved, especially in EV battery charger application which requires the pre-charge mode and charging current ramping up.

(2) Accurate ZVS current and dead-time settings have been realized. When using MPS control, the inner phase shift can be applied to the primary-side H-bridge or the secondary-side H-bridge. For a single switch, the resonant loop is different when modulation strategies are different. To analyze the ZVS transition, H-bridge is used as the basic unit. Typically, there are three basic resonant loops with the different minimum required inductor energy to finish the ZVS transition. Therefore, the minimum required inductor energy and the ZVS transition time vary with switching patterns.

(3) An analytical model of the CMV of the DAB converter has been built. With the MPS control, DPS modulation can generate a three-level waveform at input and output, and TPS modulation can generate a five-level waveform, as the CMV. The transformer parasitic capacitance then acts as the bridge to couple the different common-mode loops. As a result,

the primary H-bridge dominates the input CMV, and the secondary H-bridge dominates the output CMV. Based on the parasitic capacitances of the DAB prototype, the analytical CM model is derived, which is used to analyze the CM performance of the different modulations and predict the CMI spectrum. To meet the standard for the EV battery charger, the CM choke is also designed for the MPS modulation.

(4) The elimination of the transformer current spike during the load transients is achieved by unifying the transformer current in all modulation modes. There is no current spike fundamentally during the load transient between DPS and TPS modulations. Also, the compensation between SPS and other modulations can be simplified because of the unified transformer current. Meanwhile, the proposed modulation strategy utilizes the unified current to realize ZVS for the primary-side switches through the whole operational range.

7.2 Future Work

The work discussed in this thesis is mainly focused on the MPS modulation in the DAB converter, including smooth transition, basic ZVS current setting, CM performance modeling, and the stability during the load transient. Still, there are more valuable topics worth being investigated. For instance, to improve the dynamic response and the control system stability, the small-signal model for DAB using MPS modulation is also important.

7.2.1 Small-signal Model for MPS Modulation

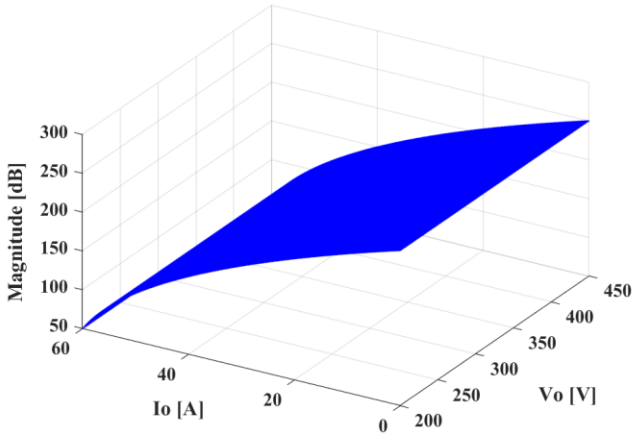
There are several modeling methods of SPS control already, including the averaged model [154], the fundamental frequency model [155], the generalized model [156, 157],

and so on. The small-signal models for DPS and TPS are also discussed [124, 158]. The averaged method is a simple way to build the system transfer function when the designed control bandwidth is lower than the sampling frequency or the switching frequency. The generalized method is a more accurate way to build the small-signal model even at high control bandwidth. At the same time, more detailed elements in the converter need to be considered, for example, the parasitic parameters in the loop and the delay caused by the digital controller.

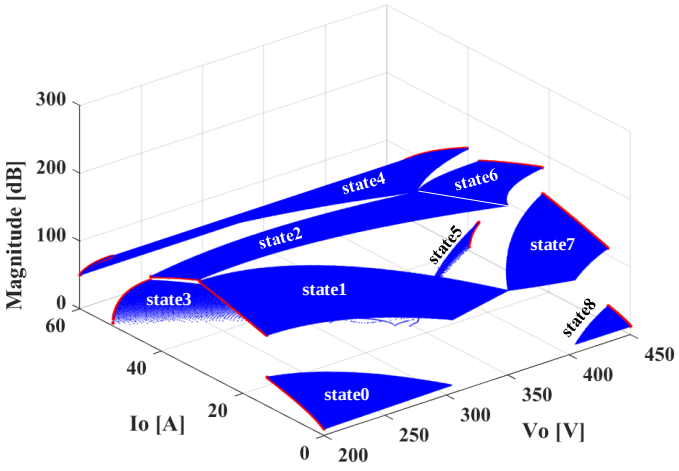
By using the averaged modeling method, the magnitude of the transfer function in the Bode plot at the low frequency is shown in Figure 7.1. If using SPS modulation for the whole operational area, the magnitude is shown in Figure 7.1 (a). If applying the MPS modulation proposed in Chapter 3, the magnitude throughout the whole operational range is shown in Figure 7.1 (b). The magnitude becomes discontinuous at the boundary between the different modulation strategies, which can bring a challenge when designing the compensator. With a more accurate generalized method and the utilization of different modulation strategies, to operate the DAB converter with higher control bandwidth the small-signal model throughout the whole operation range hasn't been addressed yet, and may bring more challenges to the control loop design.

7.2.2 Voltage Balancing Control for DAB Converter with Input-Series-Output-Parallel

For the applications with the high input voltage and the high output current, the input-series-Output-Parallel (ISOP) structure can help to release the higher voltage stress at the



(a)



(b)

Figure 7.1. Magnitude of the averaged small-signal model at 100Hz: (a) SPS; (b) MPS [124].

input and share the load current at the output. For a medium-voltage system shown in Figure 2.28, MV DC can be as high as 25 kV and the LV DC bus is around 1000 V. Even when using 10 kV SiC MOSFET, at least 4 H-bridges need to be series on the primary side. For a 200kW power rating, 4 H-bridges need to be paralleled to increase the current capability. Figure 7.2 shows the example of three DAB converters with an ISOP structure.

For ISOP structure, except for the control algorithm for a single DAB converter mentioned above, the voltage balancing control is necessary to make sure that each DAB converter can operate at the rated circumstance. For the safety concern, usually, the input voltage is selected as the feedback for the power balancing control, because the over voltage of the devices can damage the devices immediately. The previous literature has addressed different voltage balancing methods including the leader and follower method [159], central controller method [160-162], and self-balancing method [163, 164]. The central controller method is the most commonly used method, which is more flexible and reliable as shown in Figure 7.3. The detailed control-loop structure for the voltage balancing control is shown in Figure 7.4. The output current control is regulating the overall output power by sensing the total output current. Each input voltage is also sampled for the voltage balancing loop. The proposed control method can make sure that the power flowing through each DAB converter is the same. The influence of the relationship between the current loop bandwidth and the voltage loop bandwidth on the stability analysis and dynamic response has not been addressed yet, which is also an important topic. Because the load transient can introduce the extra voltage unbalance.

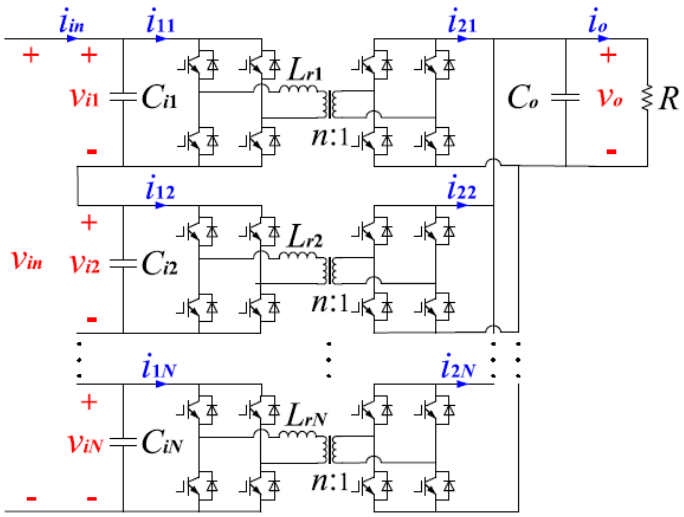


Figure 7.2. Topology of the DAB ISOP DC-DC converter [161].

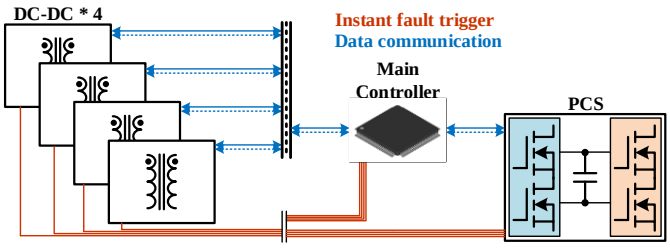


Figure 7.3. Example of the central controller method.

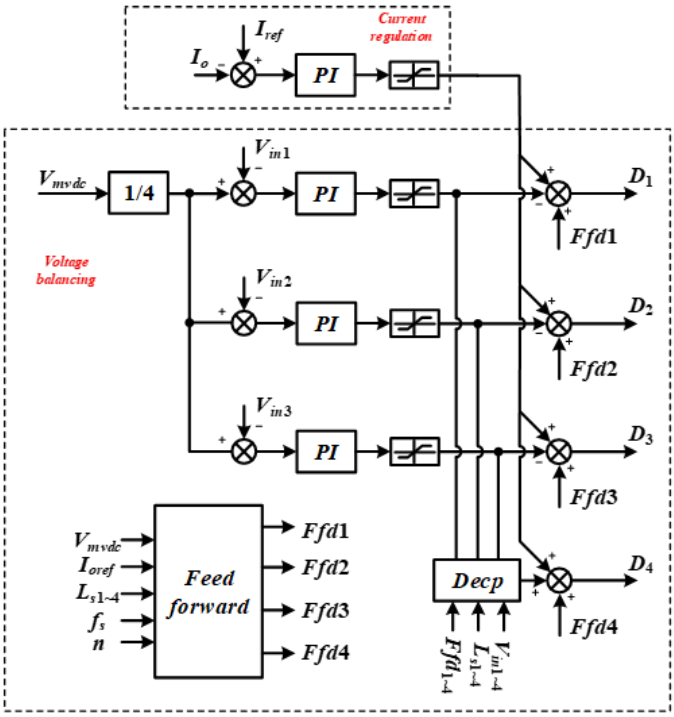


Figure 7.4. Control-loop for ISOP DAB converters.

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