To the Graduate Council:

I am submitting herewith a thesis written by Burak Ozpineci entitled "Studies on a Performance Enhanced DC-HFAC-AC Converter for AC Drive". I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

Bk. Bose

Bimal K. Bose, Major Professor

We have read this thesis and
recommend its acceptance:

Marshall Pace

Walter L. Green

Accepted for the Council:

Associate Vice Chancellor and
Dean of The Graduate School

STUDIES ON A PERFORMANCE ENHANCED DC-HFAC-AC CONVERTER SYSTEM FOR AC MOTOR DRIVE

A Thesis

Presented for the

Master of Science Degree

The University of Tennessee

Burak Ozpineci

May 1998

DEDICATION

I dedicate this thesis to my parents Gülderen and Oktay Özpineci. Without their great support, I wouldn't have been here.

Bu tezi annem Gülderen ve babam Oktay Özpineci'ye adıyorum. Onların vefakar desteği olmasaydı ben buralarda olamazdım.

ACKNOWLEDGEMENTS

I have to thank a lot of people with whose support I have finished this work. I am most thankful to my advisor, Dr. Bimal K. Bose for his trust on me for this work, for sharing his intellectual expertise, his wide guidance and teaching. Thanks are also extended to my committee members, Dr. Marshall O. Pace and Dr. Walter L. Green for their review and supervisory.

I recognize my colleagues from UT Power Electronics Laboratory for their thought provoking discussions : Joao O. P. Pinto, Li Hui, and Sewoong Kim..

I also want to thank the U.S. Office of Naval Research for their support in funding this project.

Many people helped me during this thesis but one of them especially needs recognition, Alev Narin Tajen who encouraged me the most to finish this work.

ABSTRACT

This work describes a high-frequency non-resonant link power conversion system where the input dc is converted to high frequency single-phase ac (20-50 kHz) through a high frequency inverter. Then, this is converted to variable frequency three-phase ac voltage by a hfac-ac matrix converter for driving an induction motor load. The scheme is particularly attractive for Electric Vehicle type applications.

A high-frequency low-weight coaxial transformer in the ac link provides isolation, voltage boost from the battery side and auxiliary power supplies. All the switches are soft-switched to eliminate switching loss, and there is no voltage or current penalty of the devices. Although the number of self controlled switches is somewhat larger, the projected efficiency, power density and reliability will be higher than the conventional soft-switched converters using the future MCT-PEBB (Mos Controlled Thyristor-Power Electronics Building Block) based modules. The system has been analyzed thoroughly, MATLAB®-SIMULINK® simulation model has been formulated, control strategy has been developed, and the system simulation study with a three-phase ac current source has been completed. The performance of the converter system appears to be excellent. An experimental drive system will be built and tested in the future.

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CHAPTER I

INTRODUCTION

The evolution of power electronics started in the 19th century, but the solid-state power electronics were first introduced in the second half of the 20th century. The first converters used hard switching. However, with the hard switching the switching losses constitute a great amount of the total losses, and as the frequency is increased these losses increase (Fig. 1.1). Therefore, the hard switching converter can not go to higher frequencies with high efficiency. With the great development of the power electronic switches, today switches can operate at higher frequencies. At higher frequencies, the waveform quality is better because the harmonics are of higher orders and the machine can filter them easily. In addition to this, the acoustic noise is taken care of because human ear cannot sense the sounds around 20kHz and above. Although high frequency operation has these benefits, hard switching limits the operation of the converters at these higher frequencies. If operation at higher frequencies is required, then the switches should be derated to have the switching trajectory in the safe operating area (SOA). Other disadvantages of the hard switching are the stress on the devices and electromagnetic interference (EMI). Prior to switching, the device sees the full dc voltage or carries the full load current. For switching in this condition, the SOA of the switch should be considered and possibly a snubber should be added (Fig. 1.2) for the safety of the

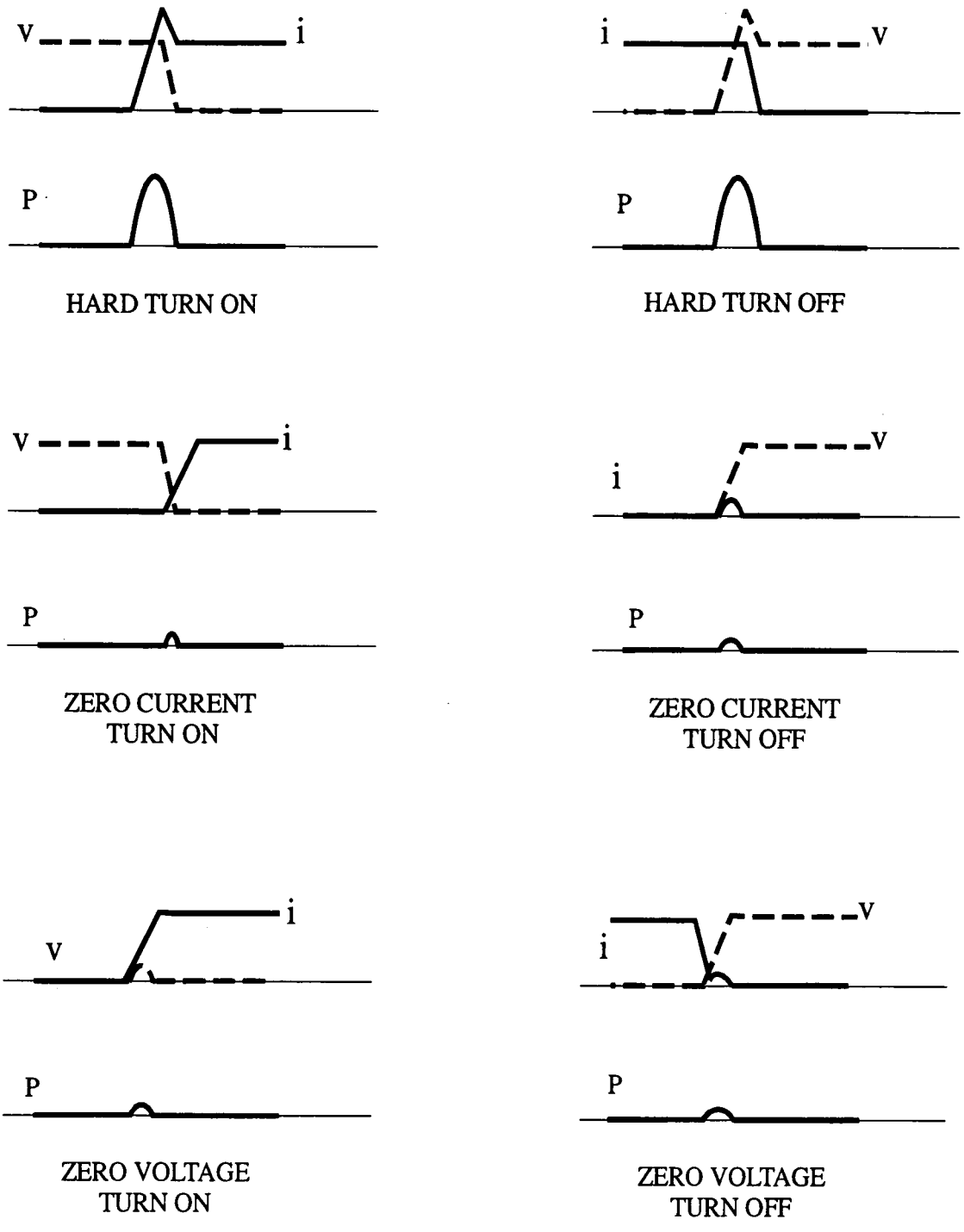


Fig. 1.1: Hard and Soft Switching of Devices

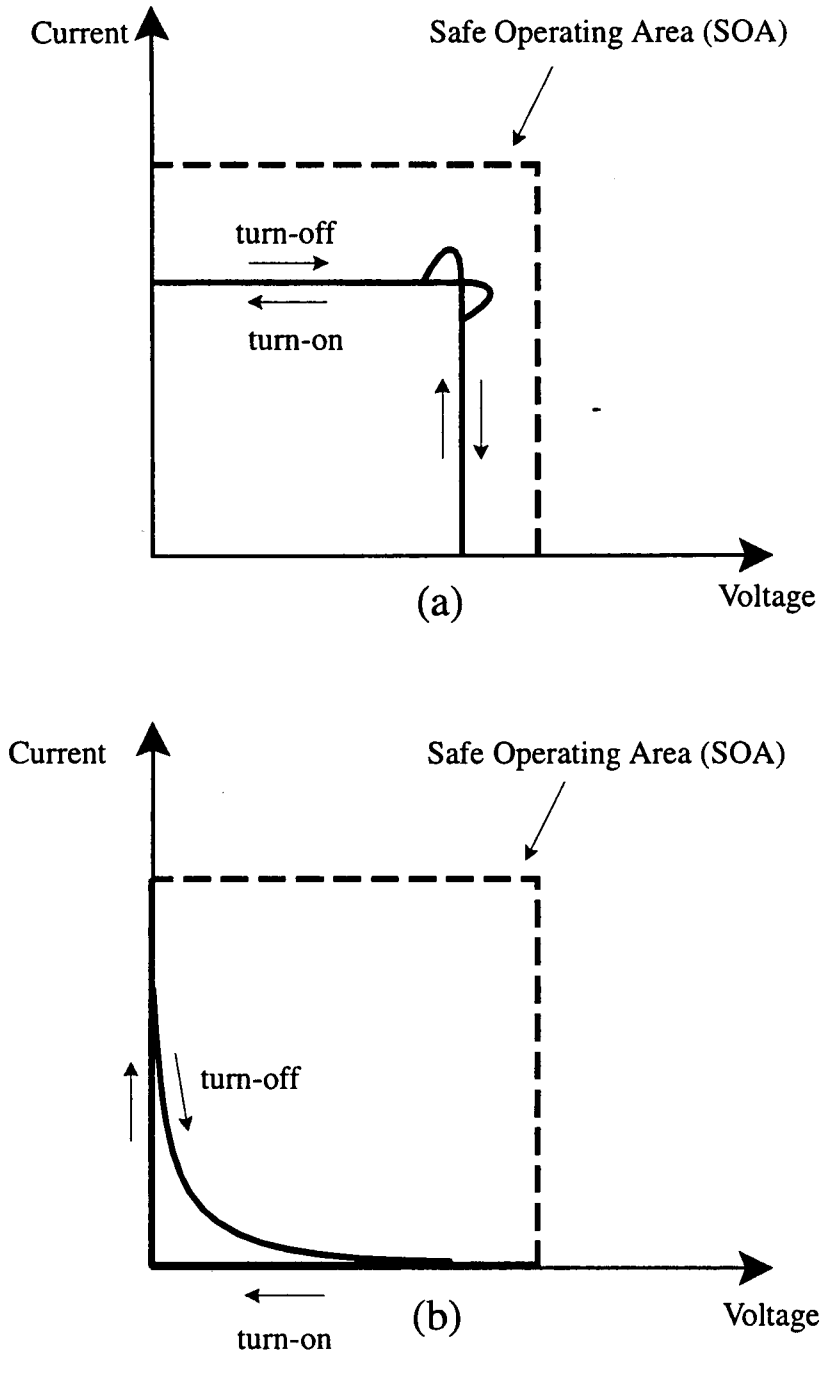


Fig. 1.2: Safe Operating Areas (SOA) and the Device Switching Trajectories for an IGBT Switch (snubberless) with
(a) Hard-Switching
(b) Soft-Switching

converter. The recovery effects and stray inductance put additional burden on the device stresses and losses during both turn on and off. On the other hand, switching with full voltage or full current results in the decreasing of these variables with a high slope as the switching speeds of the recent devices increase. This contributes to severe EMI problems, which if not avoided might cause problems of operation of the control electronics devices. In addition to it results in unwanted bearing currents, which decrease life of the bearings of the machine. To avoid these effects, EMI filters should be used, and this introduces a size penalty.

The problem addressed above is due to switching at full voltage or full current. Then the idea of switching when one of these variables is zero, i.e. zero current or zero voltage. This idea was later named as 'soft switching' of the devices. Therefore, to achieve soft switching, either the voltage across the switch should be zero, zero voltage switching (ZVS) or the current flowing through it should be zero, zero current switching (ZCS).

The answer to the question of 'why soft switching' should be clearly stated to show the superiority of soft switching compared to hard switching. The most important advantage of soft switching is that it brings solution to the problems of hard switching. At least one of the multipliers of power, i.e. voltage or current, is zero. Thus, theoretically the switching power loss is zero leaving just the conduction losses as the switch losses in the converter. In practice, there is a switching loss due to the device characteristics (Fig. 1.1.), but compared to the hard switching case this is almost negligible. This results in

more efficient converters. With decreased switching losses, higher switching frequencies can be achieved utilizing the high-speed switches. Apart from these, the switching operation is done with either zero voltage or zero current the operating region in SOA of the v-i plane corresponds to the trajectory along the axes (Fig. 1.2). Therefore, the switch can be turned on and off safely. There is no need for snubbers. In addition to these as side benefits for most of the cases, the diode recovery current and device capacitance do not cause problems during switching. Another by-product is that EMI effects are reduced with the slow rise of the voltage and current during commutation.

Soft switching discussions started during late 1980s with Divan's paper [1] proposing the resonant dc link inverter (Fig. 1.3). This inverter has an extra resonant inductor and a resonant capacitor on the dc link. Basically, with the resonant circuit in action the dc bus voltage swings between a negative peak to a positive peak, sinusoidally. At the zero crossing of the voltage the switches are turned on and off with zero voltage. The converter is controlled with integral cycle control, which basically selects a positive or negative pulse for the output. This scheme has the problems of voltage penalty on the switches because the resonant voltage increases to twice or higher the battery voltage. The resonant inductor carries the sum of the load current and the resonant current contributing to extra losses. The control, on the other hand, imposes sub-harmonic problem. Another difficult issue is to detect the zero crossing of the bus voltage so that the switches are turned at zero voltage. If the switching is not done exactly at the zero crossing, the switching can not be soft.

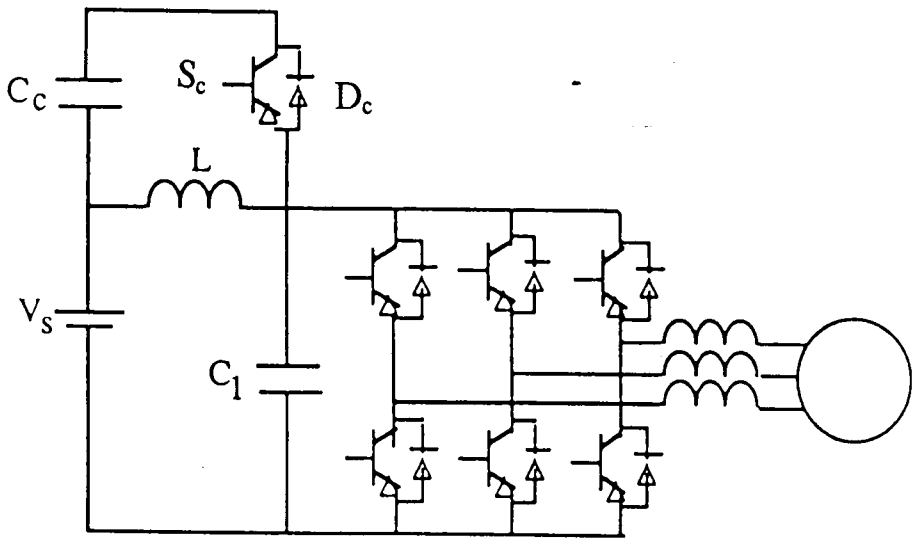


Fig. 1.3: Circuit Diagram of an Actively Clamped Resonant DC Link (ACRDCL) Inverter

After the first paper, many different converter topologies were proposed. They were all distinct from each other but their aim was to achieve zero voltage across the device or zero current through the device or both. To achieve this in inverters there are traditionally, two major techniques. The first one is to decrease the dc link voltage to zero and change the switch states simultaneously as in the previous example (Divan's converter). The inverters using this technique are called 'resonant dc link inverters (RDCL)'. The disadvantage associated with these inverters is that because all the switches turn on and off simultaneously, PWM (Pulse Width Modulation) flexibility does not exist. The other technique involves extra auxiliary resonant circuits for each phase leg, which with a special control turns on the diode anti-parallel to the switch to be turned on. When this diode is on, the switch can be turned on with zero voltage. The inverters utilizing this technique are called 'resonant pole inverters (RPI)'. These have more components and the cost is somewhat higher but switches on each phase leg can be turned on and off nearly independently resulting in a better PWM quality as compared to the previous technique.

Apart from these techniques, turning of a switch with a large lossless snubber capacitance across it at any time is considered to be soft switching. This is because with a large capacitor, the switch voltage builds up slowly. The current through the switch ceases before considerable voltage is built up. Therefore the switching loss is low. On the other hand, turning on a switch with a series inductance with zero initial current is also

considered to be soft switching with a similar reasoning. That is the voltage across the switch decreases to zero before the inductor lets the current through it to increase, therefore the current is around zero during switching.

To explain and comment on the entire family of soft-switching converters might take a lot of pages. Thinking that the principles of operation for all of them are similar, three or four types of these converters can help understanding the others and the work in this thesis. For this reason three types of converters are selected: Actively Clamped Resonant DC Link (ACRDCL) Inverter [2], Auxiliary Resonant Commutated Pole (ARCP) Inverter [3], and High Frequency AC Link (HFACL) Inverters [4]-[7].

The main problem with the RDCL is that there is a voltage penalty despite the advantages of soft switching. The same author [2], who proposed RDCL came with another solution, ACRDCL, which is simply an RDCL with a capacitor and a switch added to clamp the resonant voltage (Fig. 1.3). The converter works as a regular RDCL until the bus voltage tends to go above (1+K) Vs (where $0<K<1$) when D_c turns on conducting current and clamping the bus voltage at (1+K) Vs. As the diode is on S_c can be gated on at zero voltage and zero current, but it will not conduct before the current reverses direction. When the charge transferred to the capacitor C_c during the conduction of the diode is recovered during the conduction of S_c, this clamping switch can be turned off. Then the bus voltage resonates to zero and the converter switching can be done during this zero period. The bus voltage is clamped around 1.2-1.4 times V_s, which is quite less than the

$2V_s$ of the RDCL but still the voltage stress on the main devices is more than the battery voltage. Besides, the resonant inductor is carrying the load current resulting in a big inductance and extra losses. The clamping capacitor should be a big, therefore bulky capacitor and it has to be pre-charged to KV_s. Instead of a capacitor a battery can be chosen to solve the pre-charging problem but it will not bring any relief on the size problem. ACRDCL improves the voltage stress on the switching devices but other problems associated with RDCL remains the same.

The disadvantages of ACRDCL as the power circuit and control led to more research on controlling the phase legs independently with no voltage or current penalty. This resulted in resonant pole inverters and the final product of this research is the Auxiliary Resonant Commutated Pole (ARCP) inverter [3]. This inverter consists of three resonant pole phase legs (Fig. 1.4) operating independently as in a hard switching inverter. However, commutations are done in a soft switching manner with the help of the lossless snubbers and the auxiliary resonant circuit. The commutations in the converter do not always use the auxiliary circuit. For high current, the commutations from a switch can be easily done without the resonant circuit, but with the help of the lossless or energy recovery snubbers. For the same commutation at light load, the auxiliary resonant circuit must be used for rate of change of voltage (dv/dt) considerations. The resonant current is built up through the inductance and summed with the outgoing switch current to swing the phase voltage from positive rail to negative rail by charging and discharging the snubber capacitors. When the voltage across the capacitor parallel to the incoming switch tends to go

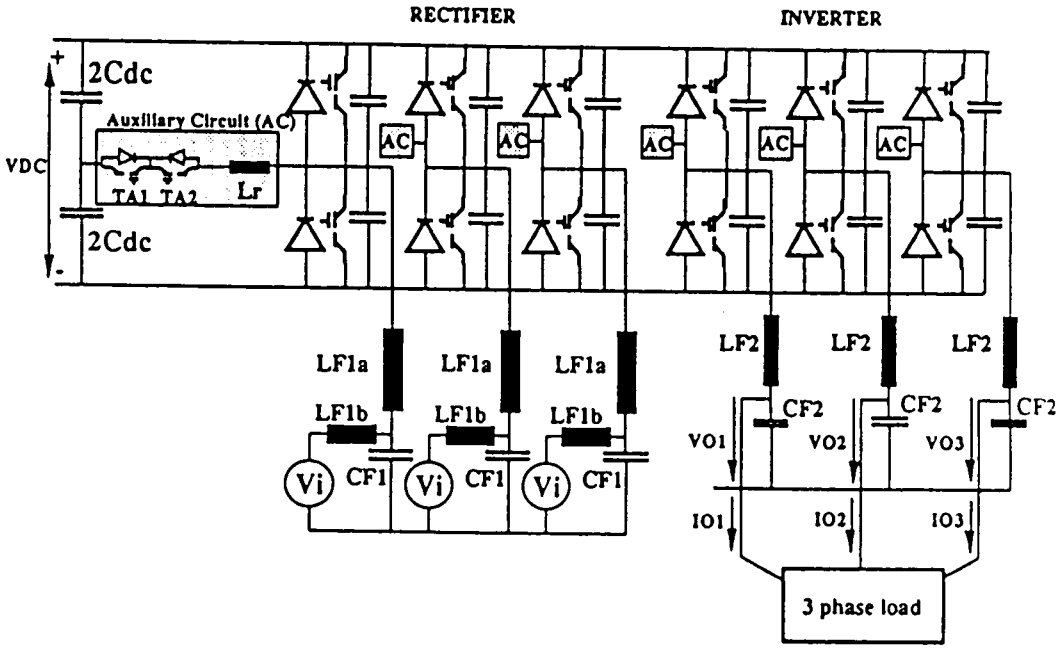


Fig. 1.4: Circuit Diagram of an Auxiliary Resonant commutated Pole (ARCP) Inverter

negative the anti-parallel diode turns on. This is the best time to turn the incoming switch on. The second type of commutations from a diode always uses the auxiliary circuit to divert the current to the diode anti-parallel to the incoming switch. Thus the switching of the main devices are done at zero voltage, unlike the auxiliary ac switches which are turned on and off at zero current with the help of the series inductance and the control. The ARCP inverter therefore decreases the voltage stress on the switches to $1.0V_s$ and increases the efficiency of the total inverter compared to RDCL type of inverters. Besides, the rates of change of current (di/dt) and voltage (dv/dt) can be controlled unlike the hard-switched converter. The individual control of the phase legs eases the operation of PWM, with the ability to go higher in switching frequencies the harmonic performance is improved. On the other hand, in addition to these advantages ARCP also has the disadvantages of high component count, dc link split capacitor charge balancing problem, and control complexity. The first one is because each phase leg in the ARCP inverter consists of two main inverter switches, and an auxiliary circuit with an ac switch and a resonant inductor, increasing the cost of the converter. For low-to-medium power applications, cost is more important than efficiency; therefore ARCP is not appropriate at this power range. On the other hand, the ARCP inverter is one of the best topologies at high power applications where efficiency is more important. The second disadvantage is due to building up the resonant current through the dc link capacitors. The charge balance of each dc link capacitor should be maintained at half the dc link voltage. Extra controls might be applied to recover the lost charge. The last of the major disadvantages is the control complexity, which is very obvious if all the PWM and commutation controls are

considered. However, nowadays, the control complexity is not a problem because there are very powerful and cheap controllers in the market.

Then comes the High Frequency AC Link (HFACL) Inverters [4]-[7]. This type of converters was first proposed by Bose et al. In 1977 [4], almost ten years before the soft-switched inverters were proposed. At that time device count was a big problem considering the size of the components. In the 90's, they are becoming the center of attention. This is mainly because of the shrinking device size and cost, and increasing device speed. The first proposed converter had a high frequency ac (hfac) link at 2-4kHz. Nowadays, the frequency is around 20kHz and it might go up to 50kHz. These converters basically convert the battery dc voltage to hfac voltage by a primary stage and then to a variable frequency variable voltage to feed an electrical machine. In the recent applications [5]-[7], the load was a brushless dc machine. The converter in reference [6] is shown in Fig. 1.5. In the primary stage there is an H-bridge inverter which converts the battery voltage to ac voltage at 16.7 kHz. In the secondary stage there is a naturally commutated cycloconverter, which is fed by the inverter through the high frequency (hf) transformer. The secondary stage has a lagging input current because it is phase controlled. This lagging current and the lossless capacitors help for the zero voltage switching of the inverter. The switches on the cycloconverter on the other hand are turned off at zero current with phase control as will be explained later. One major difference of this converter to the previous ones is that all of the commutations are non-resonant. Therefore, there is no storage between the input and the output and there are no resonant

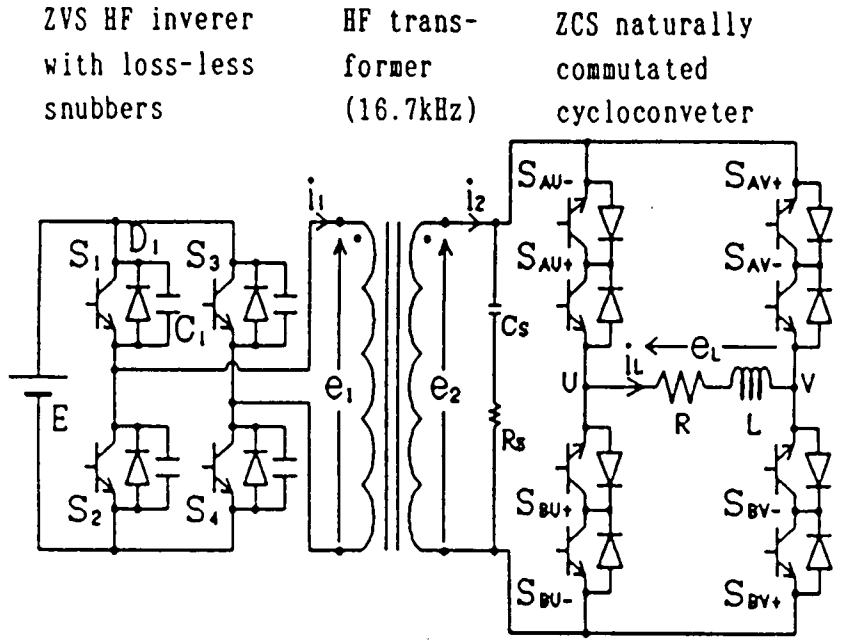


Fig. 1.5: Circuit Diagram of a High Frequency AC Link (HFACL) Inverter

losses. One major drawback is that at light load the rate of change of voltage in the ac link (dv/dt) is too small. This, results in loss of volt-sec area in the ac link voltage and therefore at the output voltage. Then it is hard to get the required output phase voltages. Extra means of controlling dv/dt is required and these extra controls are not described in the referred publications.

In this thesis, the advantages and disadvantages of the soft-switched converters are examined. The previous HFACL inverters were designed for single-phase outputs driving brushless dc motors. In addition to these, as mentioned earlier these inverters lose volt-sec areas at light load effecting the performance of the drive negatively. All the different topologies are considered (see the references) and a performance enhanced converter topology for driving a three-phase induction motor is designed (Fig. 2.1). This converter, in addition to being the first application of HFACL converters in three-phase converters, it also solves the associated volt-sec area loss by adding a simple resonant branch. The resonant branch is only used for light load conditions to improve the ac link voltage slope during commutation. As a result, programmable slope or dv/dt is obtained, which decreases the volt-sec loss of the output voltage, thus enhancing the performance of the drive.

Following the design, detailed mathematical analysis of the converter in this work is done. After the model of the converter is derived for all the operating modes, it is

extensively simulated using MATLAB®-SIMULINK® (a registered trademark of MathWorks Inc.).

CHAPTER II

SYSTEM OVERVIEW

The converter system in Fig. 2.1 consists of two power converters interconnected through a high frequency ac (HFAC) link. The first of the converters is a high frequency (HF) inverter, which inverts the supplied battery voltage to high frequency trapezoidal constant ac voltage at 20 kHz. This ac voltage is fed to the high frequency ac to ac (HFAC-AC) Matrix Converter through a high frequency transformer. The secondary converter converts the high frequency ac voltage to variable voltage variable frequency three-phase ac voltages at 0-300 Hz.

2.1 HF Inverter:

The HF inverter is a single-phase H-bridge inverter with a parallel resonant branch added to the load side to aid in commutation when required. This inverter works basically by turning on and off the pair of switches in diagonal together. Assume initially that one pair of switches are on, applying the battery voltage on the load. If these switches are turned off the load current charges and discharges the capacitors parallel to each switch. When the voltage across the other pair of switches swings down to zero and tends to go below zero, the diodes parallel to these switches conduct applying negative voltage to the load.

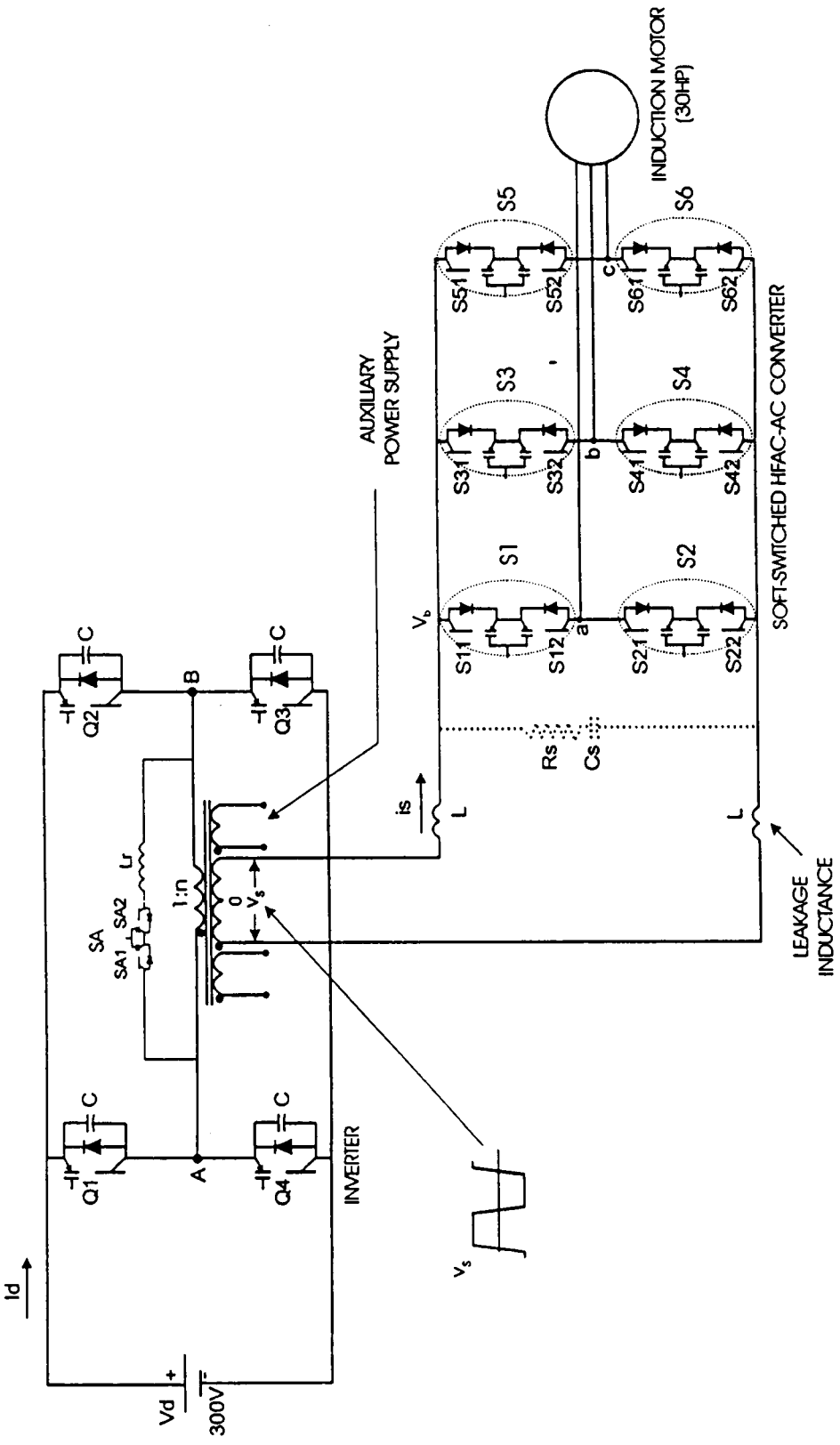


Fig. 2.1: Soft-Switched MCT-PEBB Based DC-HFAC-AC Phase Controlled Converter

It is then the time to turn on the switches at zero voltage condition. The load current, i.e. the input current of the phase controlled HFAC-AC Matrix converter is always lagging. Therefore the switches are gated on when the diodes conduct. They don't start conducting unless the lagging current reverses direction. The converter operates in this manner for the remaining cycles.

The charging and discharging time of the capacitors determine the dv/dt of the ac link voltage wave. This dv/dt, which is directly applied to the devices, should be low for the safety of the switches and for electromagnetic interference problems. However, because of volt-sec area problems in the secondary stage, which will be discussed later, the dv/dt cannot be lower than a minimum. Here comes the effect of the resonant branch. The maximum dv/dt can be set by choosing an appropriate value for the snubber capacitor, C. However, as the load current decreases, dv/dt decreases. At a certain value of the load current if an additional current in parallel to the load current can be obtained the dv/dt can be increased again. This is provided by the resonant circuit. For higher currents, there is no need to use the resonant branch but for lower currents resonant assisted commutation is a definite requirement. First, it must be decided if the load current is high enough for sufficient dv/dt or not. If it is low, before turning off the conducting switches, a boost current on the resonant inductor should be established. After the required amount of boost current is obtained, the on switches are turned off initiating resonance between the lossless snubbers and the resonant inductor. The boost current is required because without the boost current the resonance would fall short due to the resistances in the

circuit and conduction losses of the devices. At the end of the resonance, the resonant current swings back to the boost current value. This is the right time to turn on the incoming devices. After this point, the inductor current decreases linearly to zero and the auxiliary switch can be turned off with zero current.

As seen earlier switches are turned on when the diode parallel to them conducts. Therefore, they are turned on with zero voltage and zero current. The capacitors parallel to the switches, apart from effecting the dv/dt of the output voltage, also act as lossless snubbers. Therefore, a switch can be turned off at any time with zero voltage switching with the help of the large capacitors parallel to it. Zero voltage turn off is assured because the capacitor won't let the voltage across its terminals to increase abruptly. As the switch turns off, the current through it decreases fast but the voltage is around zero and doesn't change much. Therefore, the switching loss, which is the product of voltage and current, is very small.

2.1.1 Ordinary Turn Off (OTOF) Mode

When the load current is high enough the inverter operates in the OTOF (Ordinary Turn OFf) mode. The operation of the inverter in this mode is similar to the operation of the hard-switched H-bridge inverter. However, always lagging load current and the control assures soft-switched operation.

The operation of the HF inverter in OTOF mode is described below with the necessary local controls.

2.1.1.1 Mode-1:

At a time t_0 in Fig. 2.2 assume that Q_1 and Q_3 are on supplying positive battery voltage to the load and assume that the load current is in positive direction as shown in Fig. 2.3.a. The inverter is in the active mode supplying power to the load. The capacitors, C_2 and C_4 are charged to the full battery voltage and the others, C_1 and C_3 are at zero voltage. Full load current is passing through the on switches.

2.1.1.2 Mode-2:

To invert the sign of the output voltage Q_2 and Q_4 should be turned on while Q_1 and Q_3 are off. At a time t_1 turn off Q_1 and Q_3. From time t_1 to time t_2, the load current is shared equally between the snubber capacitors (Fig. 2.3.c). This current passing through the capacitors forces the capacitors to charge and discharge linearly. In this case, C_1 and C_3 are being charged to the full voltage while C_2 and C_4 are being discharged. The voltage across the latter pair capacitors swings from full battery voltage to zero voltage and tends to go negative. At this point, the diodes parallel to these capacitors are forward biased and they start conducting the current, applying negative battery voltage to the load. These

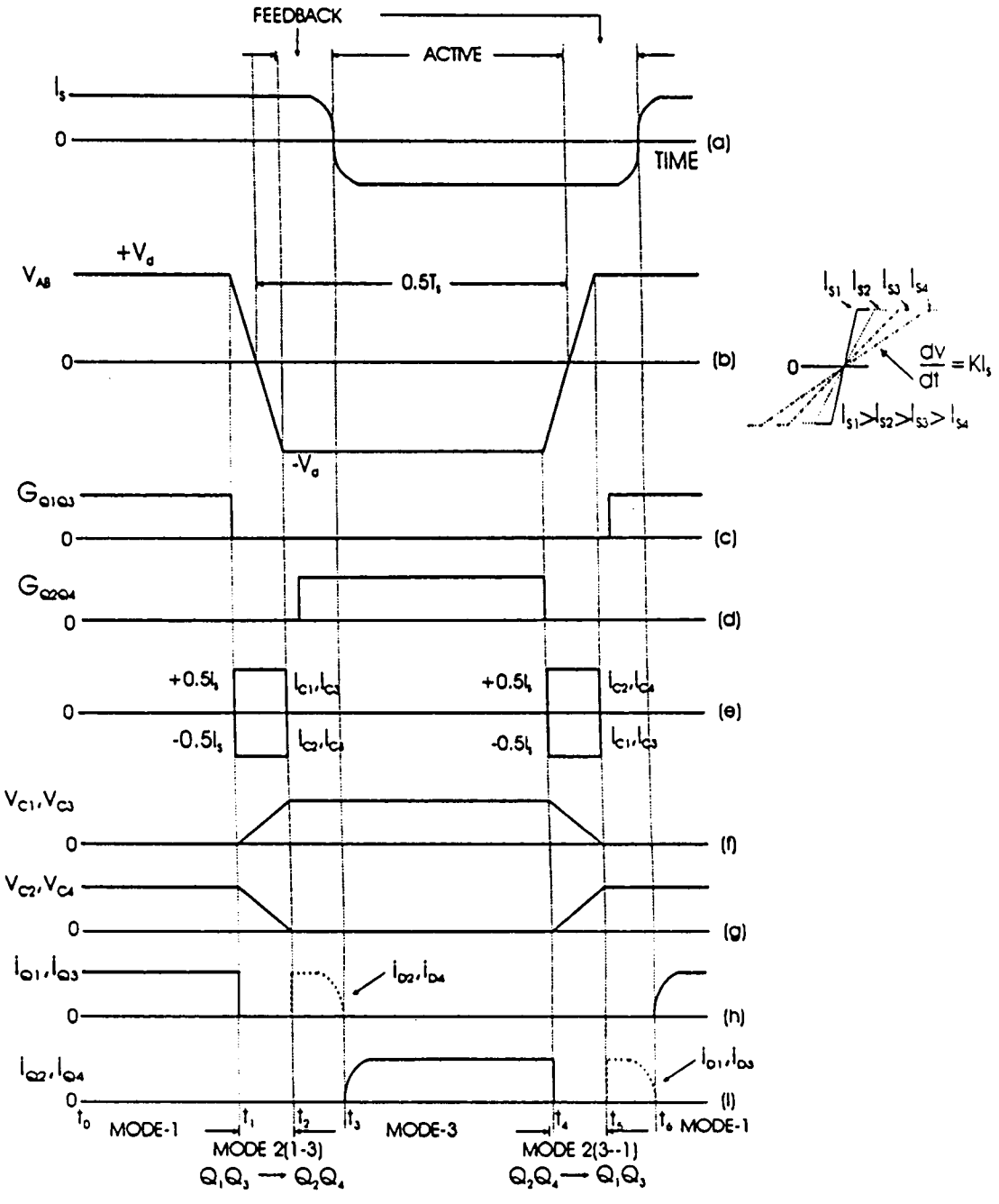


Fig. 2.2: HF Inverter Explanatory Waves-Non-Resonant Commutation (OTOF Mode)

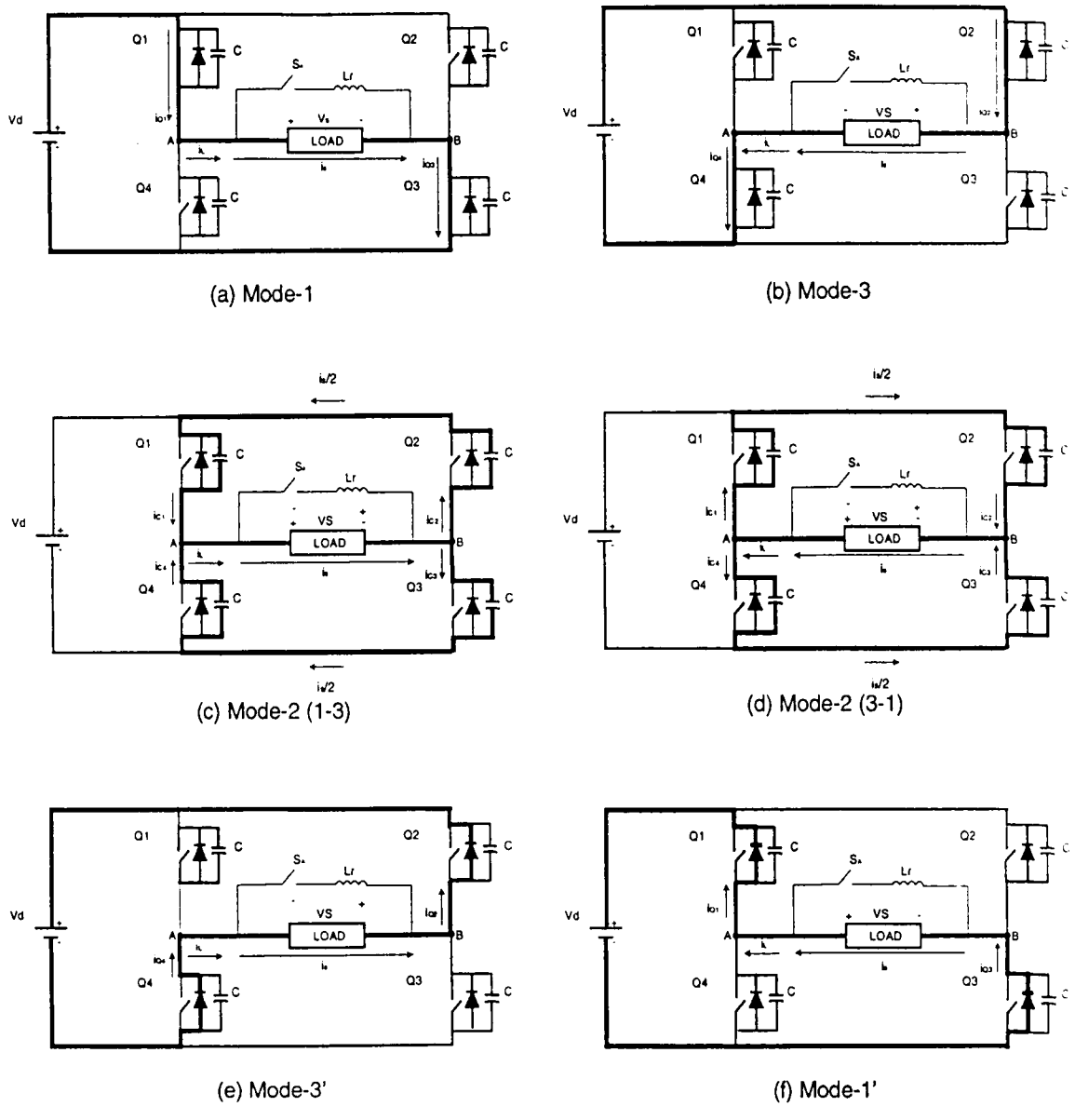


Fig. 2.3: Operation Modes of the HF Inverter (OTOF)

diodes turn on at zero voltage (assuming ideal diodes). Any time after the diodes turn on, the switches, Q_2 and Q_4 parallel to these diodes can be gated on at zero voltage and zero current. The current is still in the same direction as before, i.e. in the opposite direction of the switch current. Therefore, although the switches are turned on, they don't conduct current until the current changes direction at t_3.

In this mode, the voltage transition occurs but the current polarity does not change. There is no power flow from or to the battery. The current flows through the capacitors and the load as shown in Fig. 2.3.c.

2.1.1.3 Mode 3:

Before Mode3, there is a transition mode, Mode 3'. In this mode, the diodes are conducting the current as shown in Fig. 2.3.e returning power from the load to the supply. The load current is lagging and hence, following the voltage transition, the load current changes direction. As the load current reverses, Q_2 and Q_4 start conducting the load current at time t_3. After this point until time t_4, the battery power flows to the load while the inverter is in active mode. Mode 3 ends at t_4 when it is time to turn off Q_2 and Q_4 and turn on Q_1 and Q_3.

The commutation procedure of current from Q_2 and Q_4 back to Q_1 and Q_2 is similar to the above-described procedure except the subscripts and the mode numbers are interchanged

and polarities are reversed.

2.1.2 Resonant Assisted Turn Off (RTOF) Mode

When the load current is lower than a value such that the dv/dt of the load voltage is below the minimum, the inverter operates in the RTOF (Resonant assisted Turn OFf) mode. The operation of the inverter in this mode is different from the OTOF mode in the sense that a resonant branch is also included in the commutation. However, as before, the lagging load current and the control timing assures soft-switched operation.

2.1.2.1 Mode-1:

At a time t_0 in Fig. 2.4, the same conditions as OTOF operation mode 1 are seen. In addition to this, let's assume that resonant commutation is required to satisfy the requirements. The switch S_A is turned on at t_1 instant with an advance time t_a compared to t_2 where the commutation starts. With S_A on, the current of the resonant inductor starts increasing linearly with the constant battery voltage directly applied to its terminals. The current increases linearly until time t_2. The resonant current value at this time is the boost current, which is introduced to compensate for the losses during resonance so that the current resonates back. The inverter is still in the active mode supplying power to the

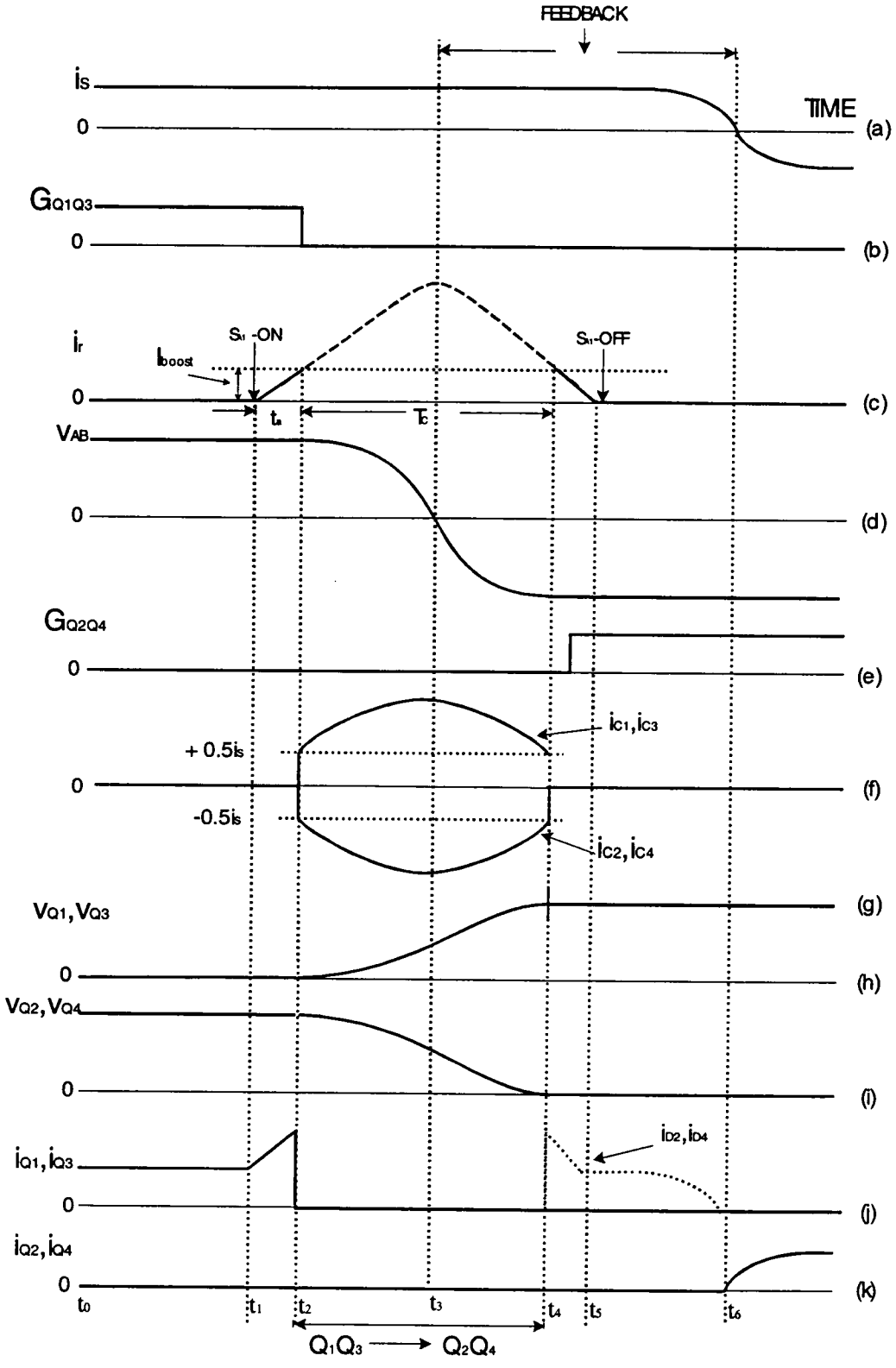
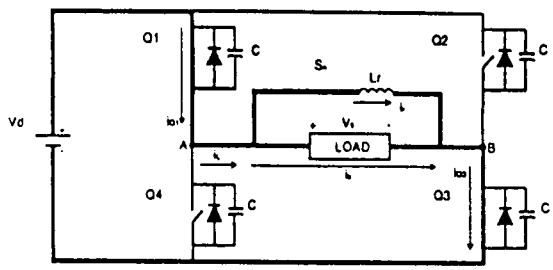


Fig. 2.4: Inverter Explanatory Waves-Resonant-Assisted Commutation (RTOF Mode)

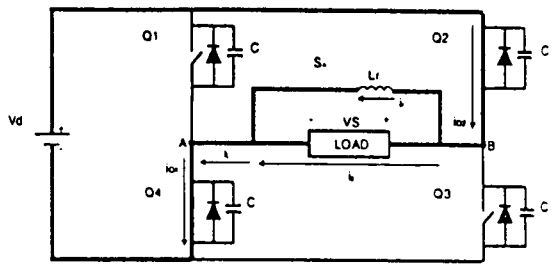
load. The capacitors, C_2 and C_4 are charged to the full battery voltage and the others, C_1 and C_3 are at zero voltage. The sum of the full load current and the resonant current is passing through the on switches.

2.1.2.2 Mode-2:

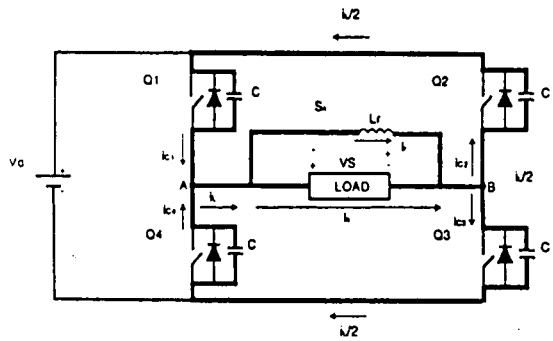
At a time t_2 turn off Q_1 and Q_3. The capacitances and the resonant inductance start resonating. From time t_2 to time t_4, the sum of the load current and the resonant current is shared equally between the snubber capacitors (Fig. 2.5.c). This current passing through the capacitors forces the capacitors to charge and discharge sinusoidally. In this case, C_1 and C_3 are being charged to the full voltage while C_2 and C_4 are being discharged. The voltage across the latter pair capacitors swings from full battery voltage to zero voltage and tends to go negative. At this point, the diodes parallel to these capacitors are forward biased and they start conducting the current, applying negative battery voltage to the load. These diodes turn on at zero voltage (assuming ideal diodes). Any time after the diodes turn on the switches, Q_2 and Q_4, parallel to these diodes can be gated on at zero voltage and zero current. The current continues to flow in the same direction as before. Therefore, although the switches are turned on, they don't conduct current until the current changes direction at t_6. At point t_4, with the conduction of the diodes the resonant commutation ends.



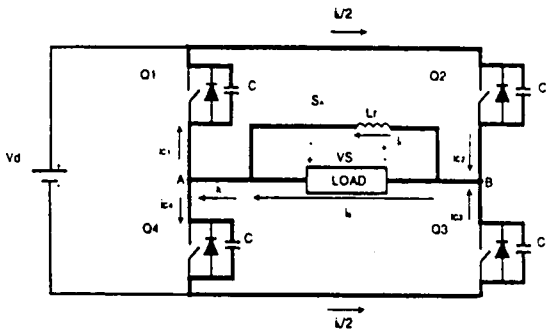
(a) Mode-1



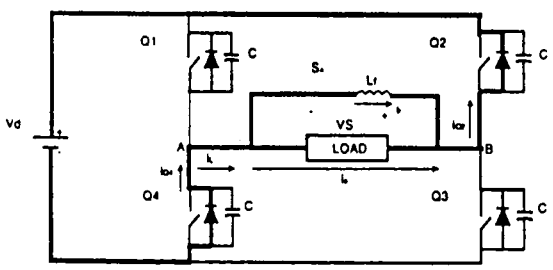
(b) Mode-3



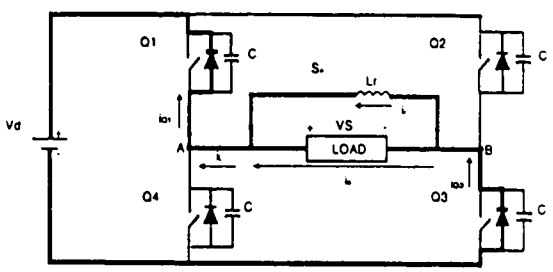
(c) Mode-2 (1-3)



(d) Mode-2 (3-1)



(e) Mode-3'



(f) Mode-1'

Fig. 2.5: Operation Modes of the HF Inverter (RTOF)

2.1.2.3 Mode 3:

Before Mode3, there is a transition mode, Mode 3'. In this mode, the diodes are conducting the current as shown in Fig. 2.5.e returning power from the load to the supply. With the diodes conducting a negative constant battery voltage is imposed on the resonant inductor which forces the resonant current to decrease linearly. As the resonant current ceases at t_4, the auxiliary switch S_A can be turned off at zero current. The rest is the same as in the OTOF mode 3.

The commutation procedure of current from Q_2 and Q_4 back to Q_1 and Q_2 is similar to the above-described procedure except the subscripts and the mode numbers are interchanged and polarities are reversed.

2.2 HFAC-AC Matrix Converter:

The secondary stage of the converter is the HFAC-AC Matrix Converter which converts high frequency single-phase ac voltage to three-phase lower frequency voltage waveforms to supply an induction motor. The input voltage for the current operation is at 20kHz and the output voltage frequency ranges from 0 to 300Hz. The converter consists of three phase legs with two ac switches on each totaling to six switches. Depending on

the reference voltage, input voltage and output current the switches are turned on using phase control. All the switching is done with zero current. To commutate current from one of the switches to the other one on the same leg, the second one is turned on which decreases the current through the first switch and increases the current through the second one. When the current through the outgoing switch is zero, this switch is turned off. A central snubber is placed across the ac link to damp the voltage spikes, which can occur if the outgoing switch turns off at a small finite current. Another use of the snubber is to suppress possible spike voltages caused by the reverse recovery properties of the diodes in the ac switches.

During the commutation of the current from one switch to the other, the ac bus is shorted giving zero voltage at the output of all three-phase voltages. After the commutation time is over the voltage rises back to its rated ac link value. The voltage gap introduced this way, which will often be referred to as the overlap period, if big, causes problems of obtaining the necessary output voltage peak. During overlap, the current is exchanged between two switches. The current in one switch decreases from full load current to zero and vice versa in the other switch. The rate of current decrease and increase in the switches is limited by the leakage inductance of the transformer. The overlap period therefore is effected by the magnitude of the phase load current and the hf transformer leakage inductance. Higher current and higher inductance causes a bigger zero voltage gap and that is not desirable to reach the output voltage goal. The load current depends on the load properties. Therefore, for a specific design the magnitude of the load current

cannot be changed. On the other hand, transformer leakage inductance is the property of the transformer, which depends on the design and the material used. Luckily, with the recent developments in the hf transformer technology the transformer leakage inductance is available at very low values (~0.15 μH), which is quite a reasonable value. With a leakage inductance value, this low, the overlap period will be negligible compared to the full period.

2.2.1 Operation:

The basic operation of the converter is explained below for a half-bridge converter. The half-bridge circuit configuration consists of one phase leg with two ac switches and a single-phase load as seen in Fig. 2.6. Two other phase legs can be added to this half-bridge to give the three-phase converter. The principle of operation and the control will be the same for all other phase legs. Therefore, the operation of the other phases will not be described separately.

2.2.1.1 Mode-1

First, assume that S_{21} is conducting the positive load current, i_a and ac switch S_1 is off (Fig. 2.6.b). The load directly sees the ac link voltage. Power flow is from supply to the load. The snubber capacitor is fully charged. This mode continues until the control

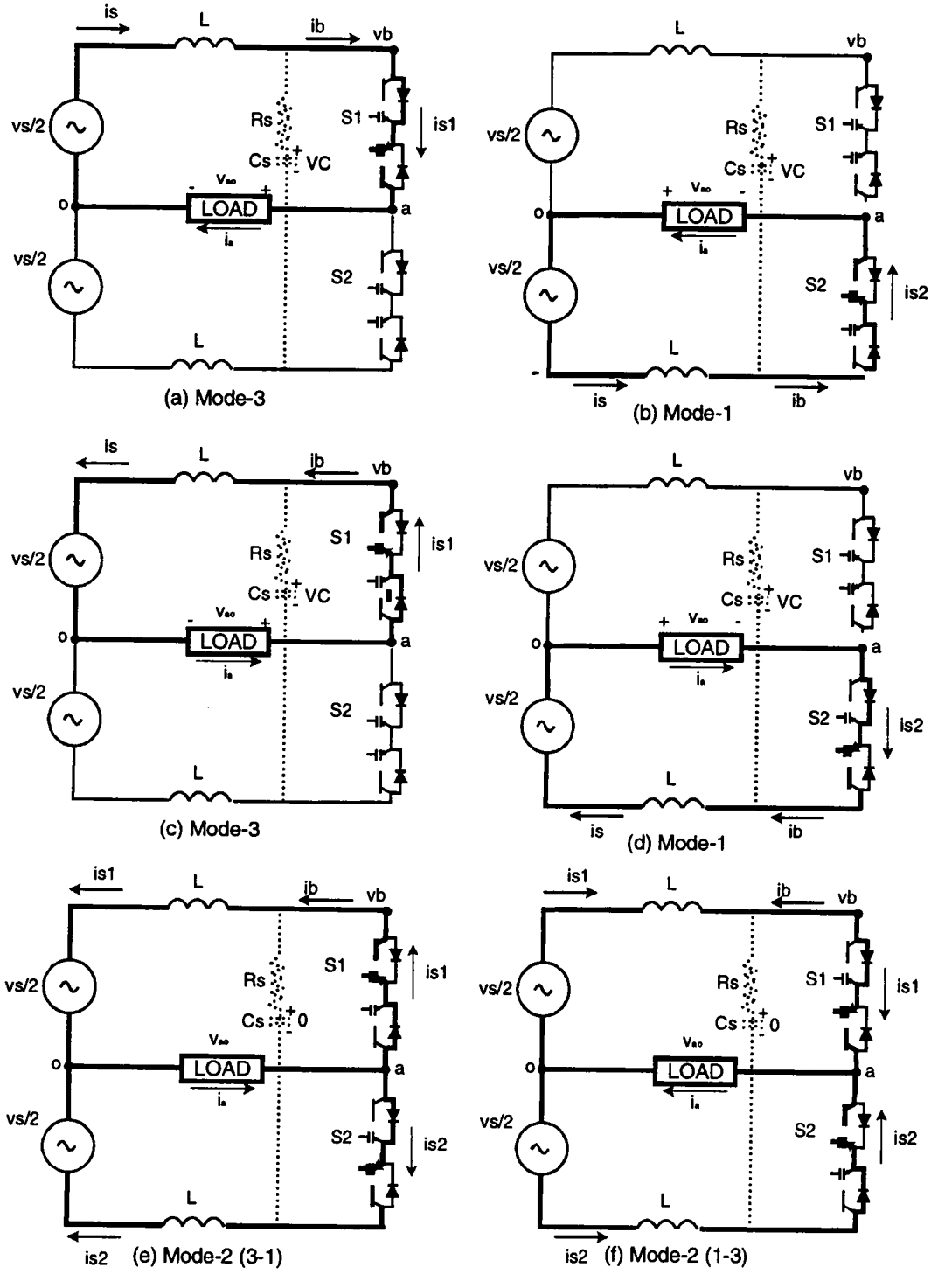


Fig. 2.6: Operation Modes of a One Phase Leg of the HFAC-AC Matrix Converter

requires the other ac switch to be turned on, i.e. until t_1 at a firing delay angle of α_a (Fig. 2.7). Then S_{12} can be turned on to start the current commutation.

2.2.1.2 Mode-2

S_{12} is turned on at zero current condition at a time t_1 to initiate Mode 2 (Fig. 2.6.f). In this mode which is also called the overlap mode, the ac bus is shorted (Fig. 2.7.a between t_1 and t_2 or t_2 and t_3 or t_4 and t_5). There are three zero voltage notches shown on the bus voltage in one half-period , one from each phase. The ac link voltage, v_s is in parallel to the transformer leakage inductance and a linear current builds up through this inductance. This increases the current through S_{12} and decreases the current through S_{21}. As the current in S_{21} goes to zero at a time t_4 (Fig. 2.7), it can be turned off with zero current. However, in practice after the commutation is completed, the reverse recovery current of the diode anti-parallel to S_{21} causes a parasitic oscillation with the parasitic capacitance of the diode and the transformer leakage inductance. S_{21} should be turned off after this oscillation is damped by the help of the snubber. If S_{21} turns off at a finite current, a voltage surge occurs, but the snubber can suppress this voltage surge. After the switch is turned off, the snubber capacitor again charges to full voltage.

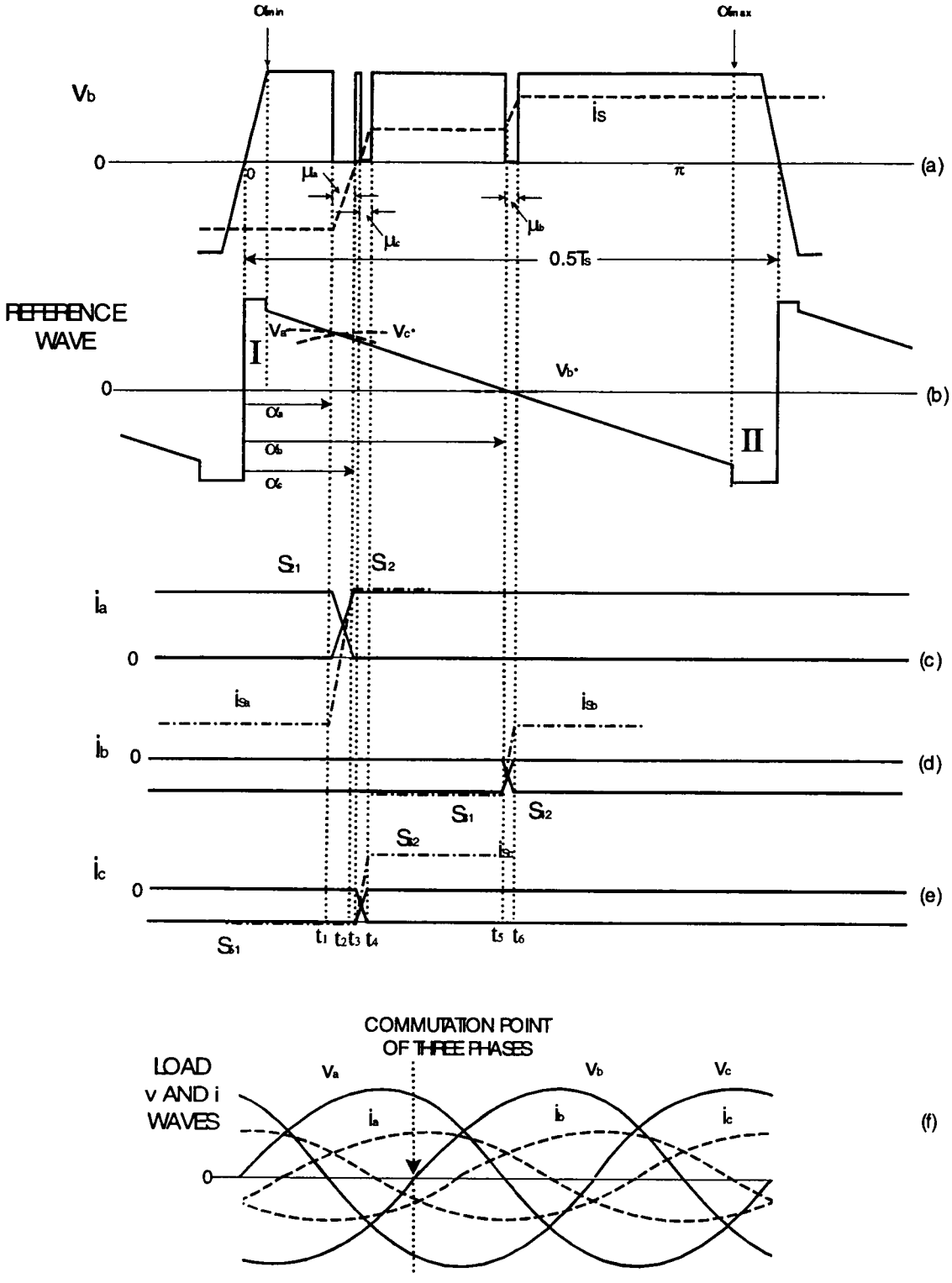


Fig. 2.7: Waveforms Explaining the Interaction of Three Phases of the HFAC-AC Matrix Converter

2.2.1.3 Mode-3

S_{12} is in conduction supplying power to the load. Switch S_2 is off (Fig. 2.6.a). The load voltage is reversed to negative battery voltage. The snubber capacitor is fully charged. This mode continues until the control requires the other ac switch to be turned on.

2.2.2 Control

Depending on the polarity of the voltages and currents of the converter, the necessary switch to be turned on is chosen. The instant or the delay angle, α to turn-on this switch is found by phase control using a form of cosine crossing technique. Two constraints can change the delay angle. The first one is that if α occurs while the HF inverter is in Mode 2, i.e. during the voltage reversal, it is postponed until the full positive or negative ac link voltage is reached. And the second one is that if α occurs during the overlap period of any other phase leg, it is postponed until it is over. The control faces another problem during the current reversal in one of the phases. These will be considered deeply in the following subsections.

2.2.2.1 Phase Control

All three phase legs are controlled using the same phase control algorithm. The switching instants in phase control are found by cosine crossing method where a sinusoidal modulating wave is compared with a reference wave. For the control of this converter the modulating wave is the voltage command and the reference wave is a quasi-triangular wave (Fig. 2.7.b). The reason for having a quasi-triangular waveform instead of a triangular waveform will be evident in the later sections. The sign of the modulating wave depends on the sign of the phase current. If the phase current is positive then there is no change in the modulating wave. However, if the phase current is negative, then the modulating curve is negated. This application will be obvious in the later figures, where with positive current, there is a positive v_{ao}^* and with a negative current the sign of v_{ao}^* is reversed. Notice that the delay angle α carries the polarity of the current as a subscript, i.e. $\alpha=\alpha_{N(P)}$ if i_a is negative (positive). Now consider Fig. 2.7.b, where a quasi-triangular reference waveform and the modulating waves for three phases (v_{ao}^*, v_{bo}^*, v_{co}^*) are given. The crossing point for phase a is at $t=t_1$, where S_{12} is turned on with a delay angle of α_a.

2.2.2.1.1 Switch Selection

The crossing point only implies that one of the switches in the specific phase leg should be turned on. Then, there's the need for deciding which switch should be turned on. It

might be thought that one of the switches is already on, therefore turn the other switch on. This works during the regular operation, but stalls, if prior to the switching instant all the switches are off. The correct answer to this question is given in Table 2.1, where the switch to be turned on is determined considering the ac link voltage and output current.

The half waves of the ac link voltage are taken and the effects of all different αs, for one phase, are shown in Fig. 2.8.

Table 2.1: The switch selection logic table. x=a,b,c

POLARITY OF i_x	POLARITY OF v_S	SWITCH TO BE TURNED ON	α- RANGE in degrees
+	+	S_1 (S_{12})	$0<\alpha_P<90$
+	-	S_2 (S_{21})	$90<\alpha_P<180$
-	+	S_2 (S_{22})	$90<\alpha_N<180$
-	-	S_1 (S_{11})	$0<\alpha_N<90$

2.2.2.1.2 Reference Wave Formation

Reference wave ideally is a triangular wave at the ac-link frequency, with a peak of '1', and a slope of '-1'. This wave is synchronized to the ac-link voltage wave, i.e. it changes polarity from '–1' to '1' at the same instant v_s changes polarity from (+) to (–) or vice versa. Because of the constraint that α's should be postponed if they occur during the

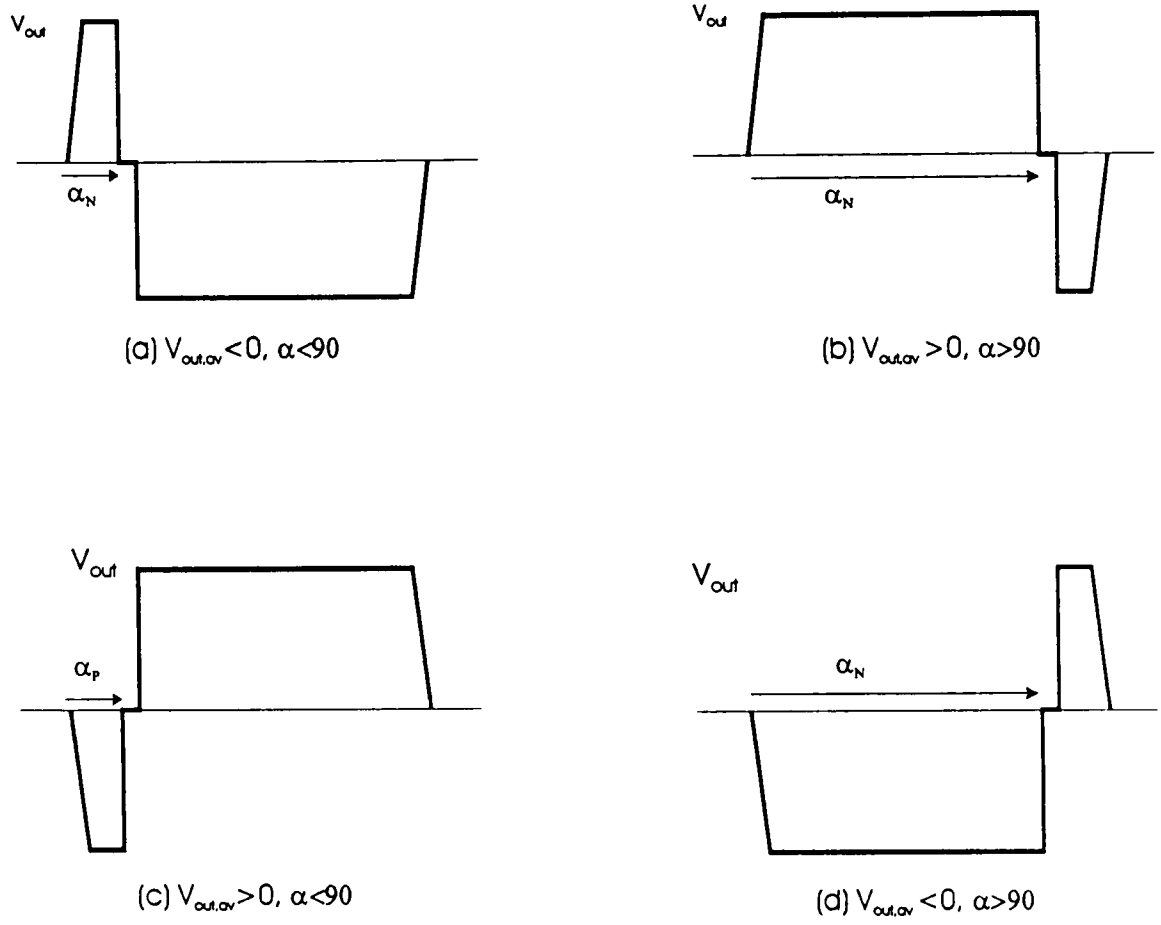


Fig. 2.8: The Waveforms of the output voltage wave for different αs

Mode 2 of the HF inverter, this triangular wave is modified to a quasi-triangular wave shown in Fig. 2.7.b. The modified wave is only different from the original triangular wave in regions I and II.

αs occur at the crossing points of the modulating wave and the reference wave. The maximum peak for the modulating wave is '1'. Therefore, if α is to be avoided in certain regions, the reference wave can be set to ±1 in those regions. As seen in Fig. 2.7.b region I the reference wave is set to +1 and in II to –1. Therefore the minimum and maximum α are set to α_{min} and α_{max} respectively. The reason, why II is wider than I is because of another constraint. That is, all the overlaps should be completed before HF inverter enters Mode 2. With a wider region II it is assured that the first constraint will be satisfied and the last overlap will have an α no bigger than α_{max}. The maximum overlap time is known by calculation, if α_{max} is chosen according to that there is no danger of overlap extending to the forbidden zones.

2.2.2.2 Clashing Overlaps

The αs of the three phases can be so that, if not avoided, two of the phases might have overlaps at the same time. This is an unwanted situation for the operation of the converter. The solution for this problem is to let the first overlap finish and postpone the overlap of the second one. In Fig2.7.c, it can be seen that the overlap of phase a starts at t_1 and ends at t_2. On the other hand, in Fig. 2.7.b it is observed that the overlap of phase c

should start after t_1 but before t_2, i.e. during the overlap of phase a. Without necessary controls this might have been the case. Instead, phase c waits for the overlap on phase a to end at t_2 and then it enters the overlap mode.

2.2.2.3 Current Reversal

The effect of the current polarity on the modulating wave was stated earlier. If the current polarity reverses the polarity of the modulating wave also reverses. This is shown in Fig. 2.9.c where the polarity of the modulating wave is negative at first and as the current polarity reverses the polarity of the modulating wave also reverses.
This is also evident from Fig. 2.10.c.

The current polarity also effects the α angles and the output voltage formation. In Fig. 2.9.d, it is seen that at first the output voltage is of the form in Fig. 2.8.d for positive current, with $\alpha=\alpha_P$. However, for negative current the form in Fig. 2.8.a, with $\alpha=\alpha_N$ is used. Notice that $\alpha_P+\alpha_N=180$ degrees, which is expected for a phase controlled converter. Now, considering Fig.2.10, the same reasoning as above can be done except that, instead of forms of Fig. 2.8a and d, the forms of Fig. 2.8b and c are used for the formation of the output voltage waveform.

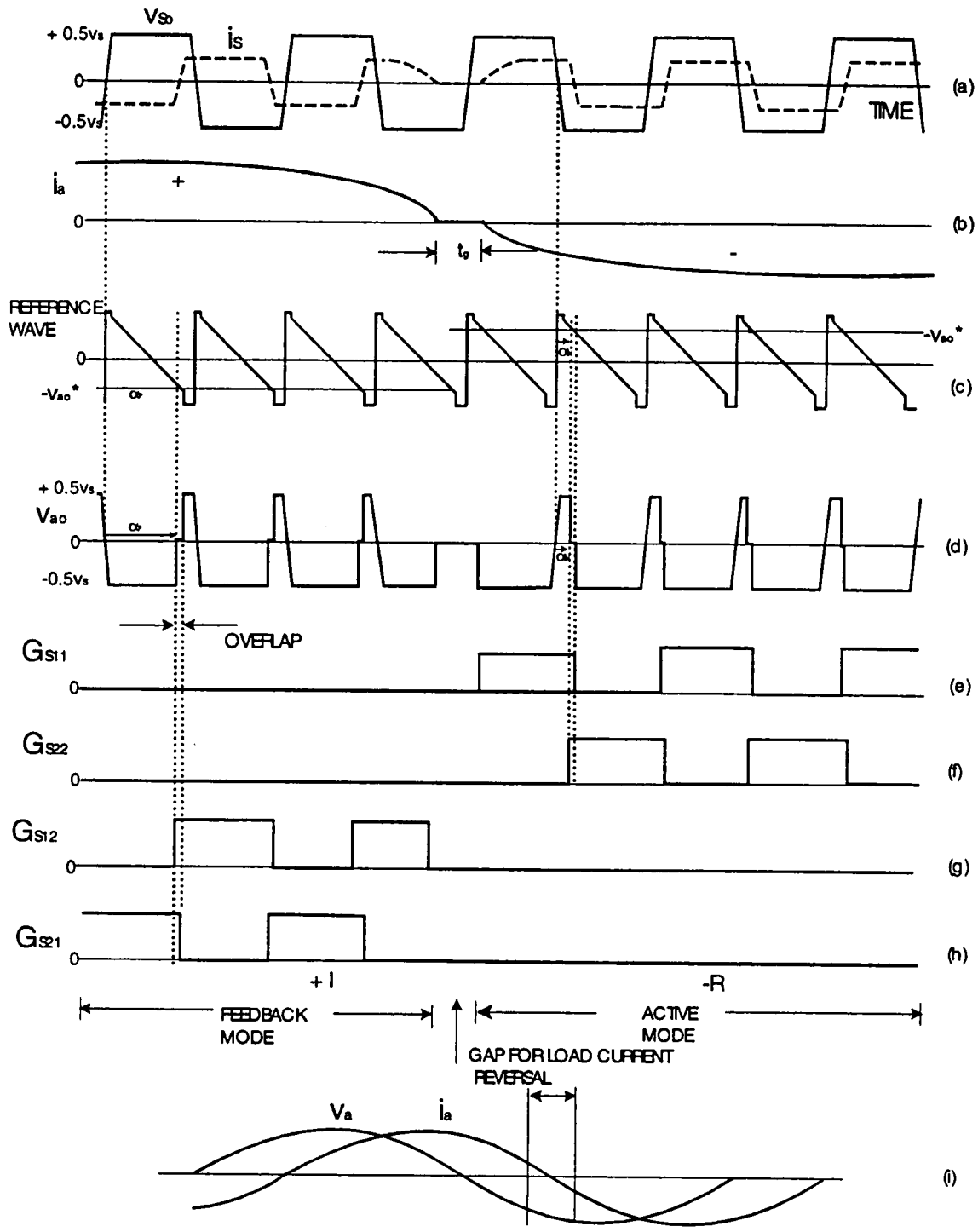


Fig. 2.9: Explanatory Waves of Half-Bridge HFAC-AC Matrix Converter

(transition from $-i_a$ to $+i_a$)

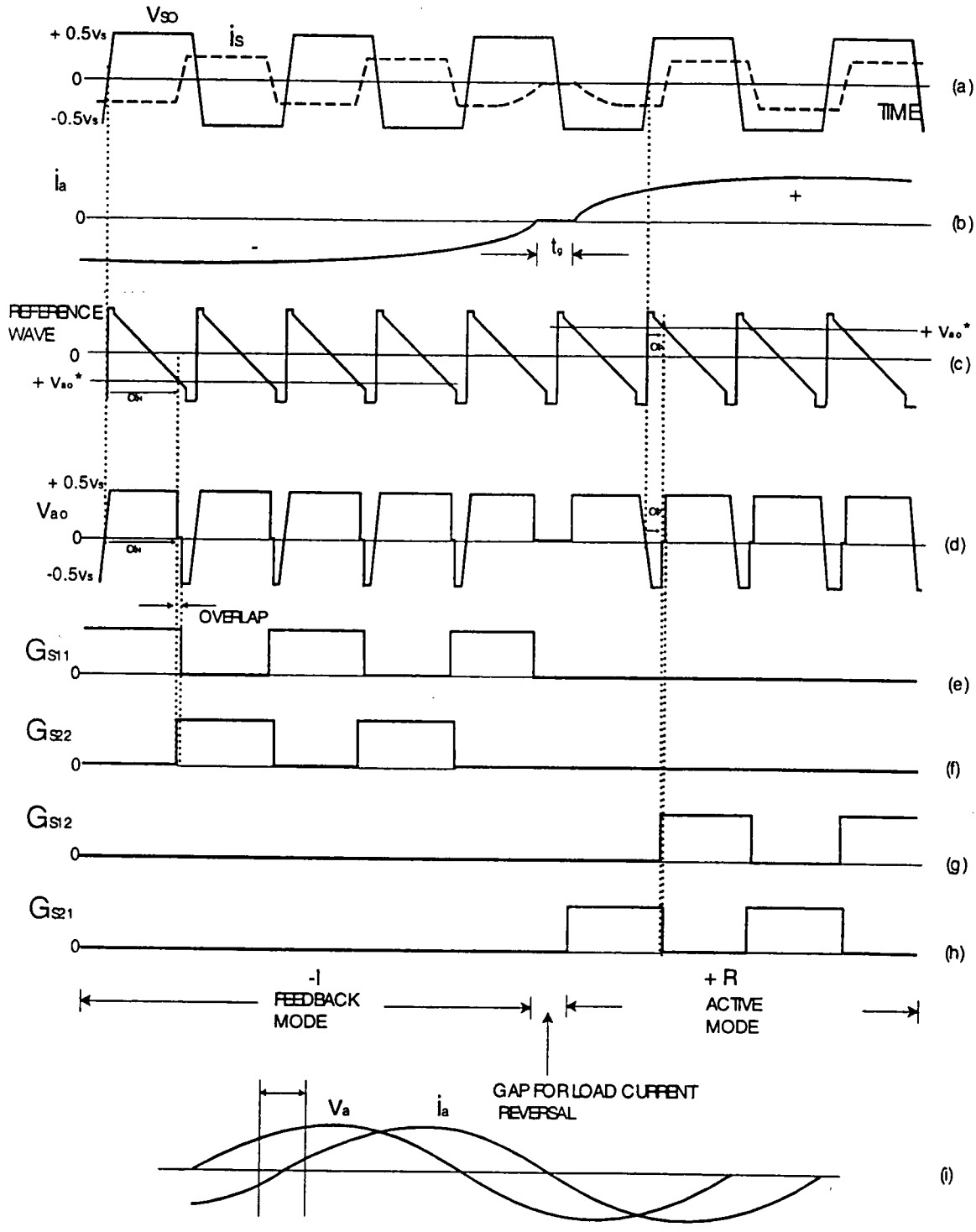


Fig. 2.10: Explanatory Waves of Half-Bridge HFAC-AC Matrix Converter

(transition from $+i_a$ to $-i_a$)

From the above consideration, it is obvious that as the current polarity reverses, the αs change and the output voltage changes form. The transition between waveforms is a problem and there are two solutions for this problem. The first one is to skip the first α after the current reversal. The second one is to turn-off all the switches immediately after the current passes through zero and turning on the selected one with the next α. In this work, the second method is preferred and the theoretical waveforms are given in Figs. 2.9 and 2.10 for current reversals in both directions. It is observed that the load current stays at zero for a small time period because all the switches are turned off at zero load current. During the same period the load voltage is also zero. Although the snubber capacitor is charged to full voltage, the first switching after current reversal is zero current switching. This is because the current starts to increase in one way, but it cannot increase much during the switching of the switch.

This is also evident from Fig. 2.10.c.

The current polarity also effects the α angles and the output voltage formation. In Fig. 2.9.d, it is seen that at first the output voltage is of the form in Fig. 2.8.d for positive current, with $\alpha=\alpha_P$. However, for negative current the form in Fig. 2.8.a, with $\alpha=\alpha_N$ is used. Notice that $\alpha_P+\alpha_N=180$ degrees, which is expected for a phase-controlled converter. Now, considering Fig.2.10, the same reasoning as above can be done except that, instead of forms of Fig. 2.8a and d, the forms of Fig. 2.8b and c are used for the

formation of the output voltage waveform.

2.3 The Overall System

Previous descriptions of the converters were on the basis that the two converters were working independently, but this is not the case for the total converter system in Fig. 2.1. The HF inverter and the HFAC-AC converter are coupled to each other through a high frequency link transformer.

The coupling of these two converters bring the problems of synchronization of control to meet the requirements and the start-up of the whole system.

The synchronization can be done by generating the reference waveform for cosine wave crossing from the output voltage of the HF inverter through waveform processing methods.

The start-up on the other hand is done by starting the HF Inverter first, establishing the ac link voltage. Before starting the inverter control, turn-on Q_1 and Q_3 and charge the capacitors C_2 and C_4 by the battery through a charging resistor. As the capacitors are fully charged, by-pass the charging resistor by turning on the by-pass switch parallel to the charging resistor at zero voltage. (Note that, neither the charging resistor nor the by-pass switch are shown in the figures.). Now, the inverter control can be enabled. It will start in

the RTOF mode, because the load current is zero. The ac link voltage can be established in this manner. It is then the time to start the matrix converter. Wait for the first α and turn on the selected switches from all three phases at zero current. With the starting of the matrix converter, three-phase voltages are applied to the machine and the drive operates in this manner.

In the case of a fault, the three ac switches in the upper half of the secondary converter can be turned off, while the lower ones are turned on. This way the machine current can freewheel easily. In addition to this, with machine current freewheeling the primary converter is isolated from the load. On the other hand, the ac link current can find a path through the snubber circuit. The switches in the primary circuit are also turned off. Then the converter can be started all again, using the startup procedure described earlier.

As a summary, the salient features of the proposed system are as follows:

The system consists of a primary high frequency (HF) inverter and a secondary high frequency ac to ac (HFAC-AC) matrix converter. All of the switches are soft switched: the primary stage switches use both ZVS and ZCS and secondary state switches use only ZCS. The high frequency ac link frequency can be increased up to 50kHz. There is neither voltage nor current penalty. Simple resonance assisted commutation is used at light load which results in controllable rate of change of voltage (dv/dt). Moreover, a lightweight high frequency transformer, which brings the advantages of isolation of the

two stages, voltage boost, and auxiliary power supplies, is inserted. The isolation is mainly required to prevent EMI and associated bearing current problems. With the voltage boost, on the other hand, the current rating of the secondary converter is decreased. The auxiliary supplies are especially important for electrical vehicle type of drives. There is no resonance in the hfac link. Four-quadrant operation is possible.

CHAPTER III

ANALYSIS

The operation of the converter system studied in this work is given in the previous chapter with details. Theoretical waveforms are also included. To have a healthy simulation some waveform analysis is required.

3.1 HF Inverter Waveform Analysis

The output of the hf inverter is basically a trapezoidal voltage waveform. When two of the switches are conducting the output voltage is equal to either positive battery voltage or negative battery voltage depending on which pair of switches is on. As explained in the previous chapter, this voltage changes direction at every 25μsec. This change can be either linear as in OTOF mode or sinusoidal as in RTOF mode. Note that, the three-phase load currents which constitute the ac link current, i_s are considered to be constant because the interval of voltage transition is negligible compared to the full period of the waveform. Typical linear and resonant voltage transition waveforms are shown in Fig. 3.1.

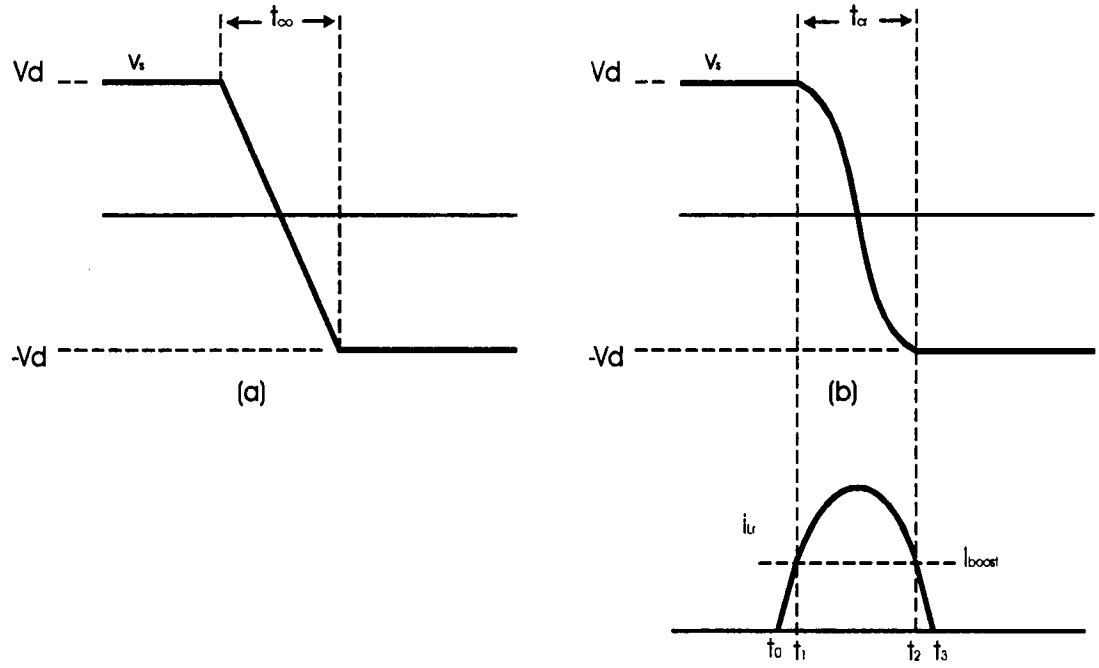


Fig 3.1: The transition of the output voltage
(a) in OTOF mode
(b) in RTOF mode

For OTOF operation, all the switches are turned off at a time t_1. Then there is only one way left for the ac link current to flow, and that is through the capacitors. This current is shared equally by the upper and lower capacitors. The capacitors are either charged or discharged with a constant current. Therefore the output voltage changes linearly. The equivalent capacitance during this interval C_{eq} is C (assume that individual capacitors have a value of C). Thus, the equivalent circuit is a constant current source parallel to a capacitor. The capacitor voltage current relation is

$$i_{Ceq} = C_{eq} \frac{dv_{Ceq}}{dt} \qquad (3.1)$$

The voltage across the equivalent capacitor is the ac link voltage. Therefore

$$i_{Ceq} = i_s = C \frac{dv_s}{dt} \qquad (3.2)$$

Multiplying each side by dt and taking the integral gives v_s as a linear function of time (See Appendix A.2).

Using the incremental values instead of the differential values in eqn (3.2) yields

$$\frac{dv_s}{dt} = \frac{\Delta v_s}{\Delta t} = \frac{I_{so}}{C} \qquad (3.3)$$

It is required to limit the dv_s/dt to 300V/μsec, which gives $\Delta t = t_{co} = 2\mu$sec for the voltage transition from +Vd to –Vd or vice versa. A higher value can lead to electromagnetic interference problems and a lower value decreases the voltage time area of the load voltage. The full load i_s during transition is calculated to be 120A (Appendix A.4). therefore C is found to be $(120/300)\mu = 0.4\mu$F.

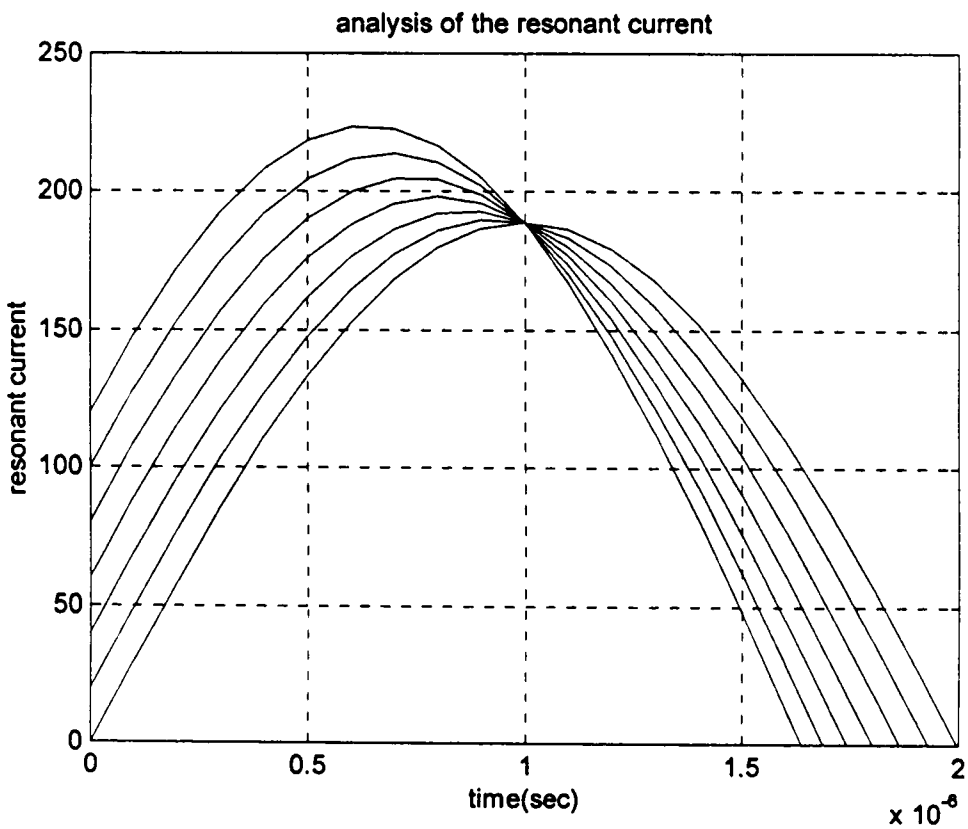
The value for dv_s/dt for a fixed capacitance value depends solely on i_s. As i_s decreases the rate of change in voltage decreases and so increases t_c. For light load at 20A of i_s, dv_s/dt is 50V/μsec and t_c is 12μsec. For 20kHz operation half-period is 25μsec, where t_c is comparable to half-period. To avoid this, a limit is set to dv_s/dt, which is 150V/μsec, half

the maximum value. This is reached with an i_s=60A and t_c=4μsec. This is reasonable thinking that the converter will be working at full load most of the time. Below this limit, the solution is the RTOF mode of commutation, which gets help from the resonant branch during commutation.

In RTOF mode, the auxiliary switch is turned at t=t_0 and current starts building up through the inductor. The inductor current rises linearly because the inductor sees the constant battery voltage across it. The voltage current relation for the inductor L_r is

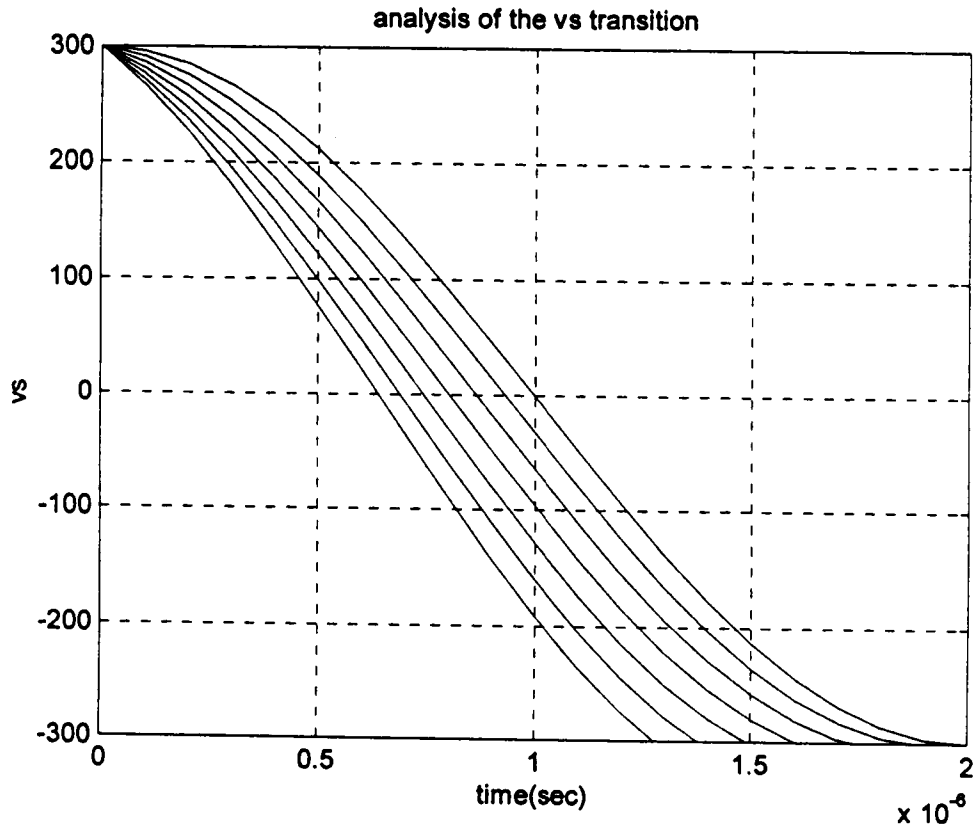
$$v_s = L_r \frac{di_{Lr}}{dt} \qquad (3.4)$$

Integrating both sides proves that the inductor current rises linearly with a constant voltage applied to it (Appendix A.2). This linear increase continues until a boost current, I_{boost} level is reached at t_1. Then, all the switches are turned off initiating the resonance. For a regular LC resonance operation half-period is given by $\pi\sqrt{LC}$ (Appendix A.5). For the resonance commutation of the inverter if i_s and I_{boost} are considered as zero, then the half period of oscillation, $t_{cr}=\pi\sqrt{L_r C}$. If t_{cr} is chosen to be 2μsec, then L_r=1.01μH. this gives a dv_s/dt of 300V/μsec. The resonance operation is analyzed in Appendix A.5. The results are given in Figs. 3.2 and 3.3. At first, i_s is kept constant at zero and v_s transition is observed for different values of I_{boost} starting from 0 to 120A at 20A steps (Fig. 3.2.a). When I_{boost} is zero the slope or dv_s/dt is 300V/μsec. As I_{boost} is increases, the slope



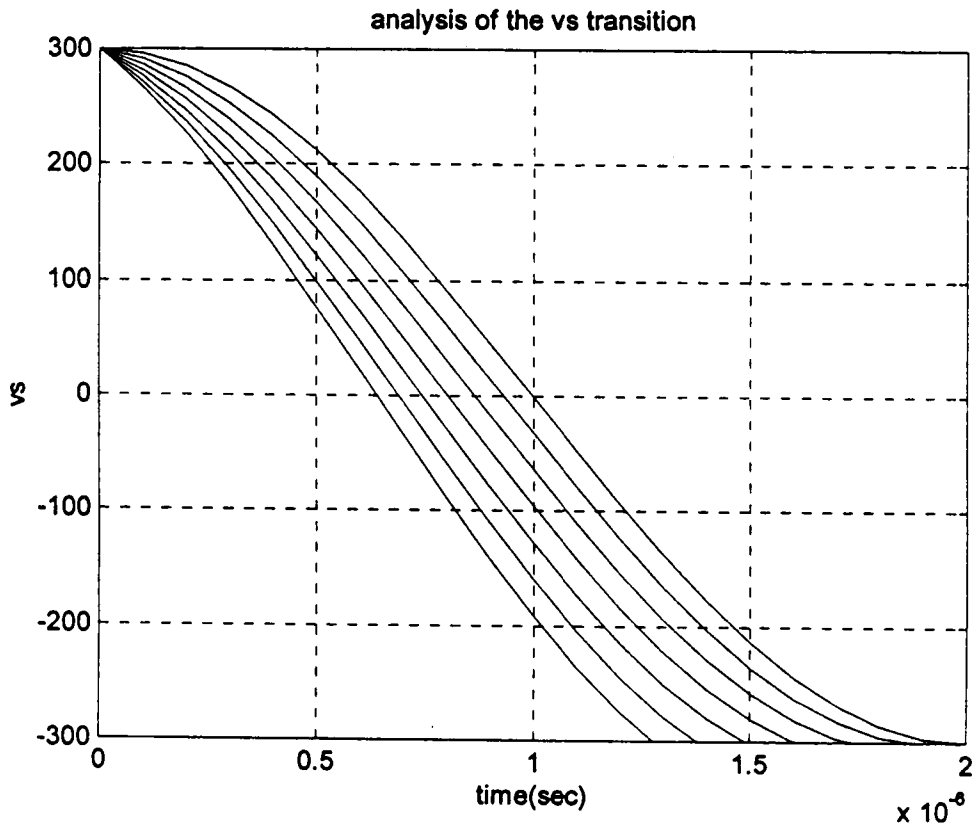
(a)

Fig. 3.2: Analysis of v_s Transition with i_s=0 and I_{boost} varying



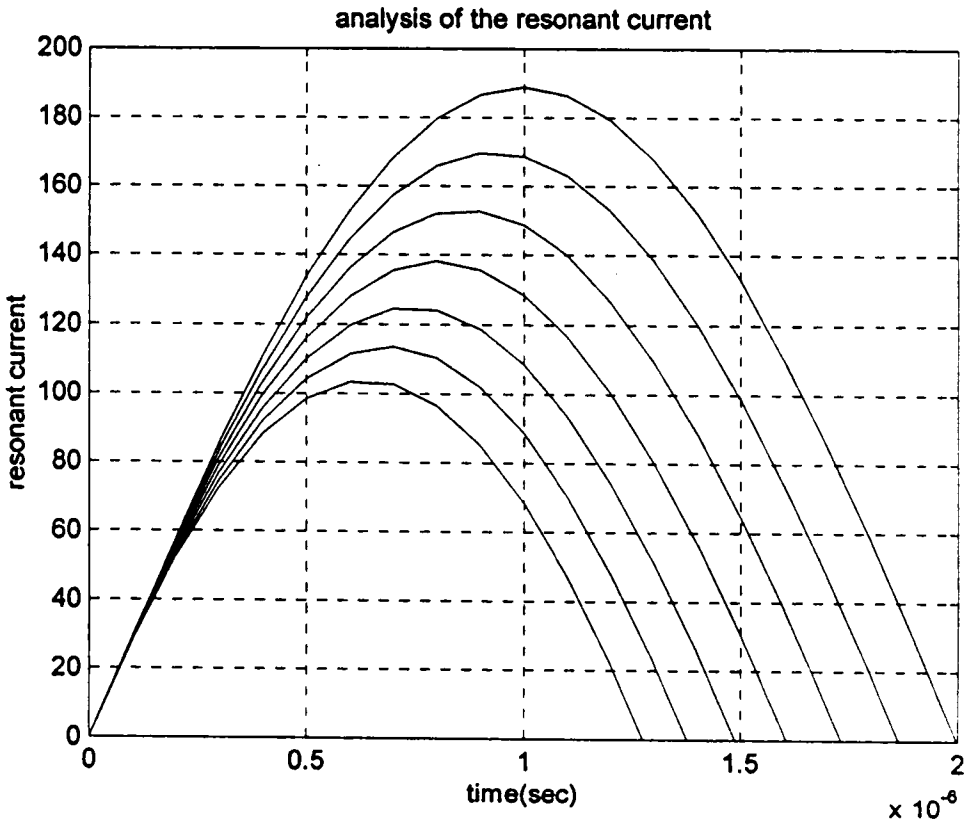
(b)

Fig. 3.2: (continued)



(a)

Fig. 3.3: Analysis of v_s Transition with I_{boost}=0 and i_s varying



(b)

Fig. 3.3: (continued)

increases. The resonant current for each operation is given in Fig. 3.2.b. The peak resonant current increases with the boost current. It is observed from these two graphs that with a constant i_s the slope of v_s can be increased by increasing the boost current and vice versa. On the other hand, increasing the boost current also increases the peak resonant current, which brings a current penalty on the auxiliary switch and the resonant inductor. In the next step, the boost current is kept constant at zero and i_s is varied from no-load to full-load (Note that RTOF mode is only used for i_s less than half of the full load). As seen in Fig. 3.3.a, for zero i_s, the slope is 300V/μsec, and it increase as i_s increases similar to the OTOF mode case. The resonant current for the same conditions is given in Fig. 3.3.b. Here, it is seen that as i_s increases the peak resonant current decreases.

3.2 HFAC-AC Matrix Converter

The important analysis issues for the HFAC-AC Matrix Converter are the waveform analysis, the snubber calculation and the output voltage calculation.

3.2.1 Waveform Analysis

The waveform analysis will explain the effects of the transformer leakage inductance, the corresponding volt-sec loss and the range of α for phase control.

3.2.1.1 Transformer leakage inductance effect

The hf inverter supplies HFAC-AC Matrix Converter through the high frequency transformer. The secondary voltage of the transformer is different from the primary voltage due to the switching of the devices in the hfac-ac converter and the transformer leakage inductance (Fig. 3.4).

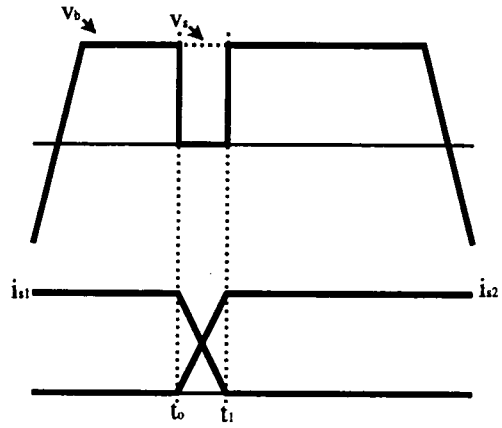


Fig. 3.4: The bus voltage and the effect of overlap of one phase

To commutate current from one switch to the other on the same leg the oncoming switch is turned on at t_0. Then the ac bus is short-circuited because both of the switches are on. This produces a notch in the ac bus voltage (Fig. 3.4) (The effects of only one phase overlap are considered in this figure for the sake of simplicity.) The equivalent circuit during overlap is the secondary of the transformer short-circuited. The secondary of the transformer can be represented as just the leakage inductance and the ac link voltage. Therefore there is an inductance (2L) parallel to the ac link voltage. This forces a linear

current in the reverse direction of the initial ac link current. Thus, the current decreases in the previous direction and increases in the other direction (see the previous chapter). The current voltage relation is

$$v_s = 2L\frac{di_s}{dt} \qquad (3.5)$$

From here the rate of change of current (di_s/dt) can be found to be $\frac{v_s}{2L}$. This rate is also the same for the switch currents. For a leakage inductance, 2L value of 2μH, this rate is equal to 150A/μsec. The peak phase current is 110Amps and the time for this current to cease with an 2L=2μH is 0.733μsec(=110A/150A/μsec). Therefore, the overlap time is also 0.733μsec. The leakage inductance value of 2μH is used in the simulation but with recent developments high frequency transformers with ultra low leakage inductance can be found (Appendix C). For 2L=0.15μH, di_s/dt is 2000A/μsec and the overlap time for peak phase current is 0.055μsec. This concludes that if the leakage inductance of the transformer decreases di_s/dt increases and the overlap time decreases. When designing, a compromise between these two values should be considered. A high di/dt can destroy the switches and a long overlap time can deteriorate the performance of the converter.

In Fig.3.4, the effect of overlap on the bus voltage is seen for one phase leg. The effect of all three-phase legs can be seen in Fig. 2.7 with more details. The load voltage directly sees the bus voltage or the negative of it as stated in the previous discussions. With the

overlap notches the output voltage is losing some volt-second area. The worst case occurs at full load when the lost volt-sec area is largest. For the general case, the total overlap time is the sum of the individual overlap times.

$$t_{overlap} = \frac{|i_a|}{\left(\frac{di}{dt}\right)} + \frac{|i_b|}{\left(\frac{di}{dt}\right)} + \frac{|i_c|}{\left(\frac{di}{dt}\right)} \qquad (3.6)$$

which is

$$t_{overlap} = \frac{|i_a| + |i_b| + |i_c|}{\left(\frac{di}{dt}\right)} \qquad (3.6)'$$

The numerator in eqn. (3.6)' has an average value of 1.9 times the peak value of the phase current. However, the worst condition occurs when this sum is maximum, i.e. 220A, twice the peak current. The overlap time for 2L=2μH is 1.47μsec and for 2L=0.15μH, it is 0.11μsec. these values show that a high inductance results in more volt-sec losses in the voltage waveform. Therefore, a low leakage inductance is good because it decreases the lost volt-sec area but at the same time increases the di/dt rate. On the other hand, a high leakage inductance increases the volt-sec area but decreases the di/dt rate.

3.2.1.2 The range of α for phase control

The range of α depends on the formation of the reference voltage. The reference voltage is a quasi-triangular wave modified from a regular triangular wave because of a

constraint. This constraint states that no overlaps are allowed during the voltage transition. From this the regions I and II are formed. Now consider the worst condition, i.e. dv_s/dt=150V/μsec, the sum of the absolute values of the three phase currents is 220A. For the leakage inductance, 2L=2μsec, the overlap time is 1.47μsec as calculated before.

It is also required to calculate the span of regions I and II. α_{min} should be calculated from

$$\alpha_{\min} = \frac{\omega_s V_d}{2\left(\frac{dv}{dt}\right)} \qquad (3.7)$$

where $\omega_s = 2\pi f_s$, i.e. the hfac link frequency in (rad/sec)

The interval I covers 2μsec with the given dv_s/dt. The interval II covers 2μsec plus the maximum overlap time of one phase, 0.733μsec, which results in an interval of 2.733μsec. Another constraint to be considered is that no firing is allowed if there is an overlap in one of the other phase legs further limiting the α range. The total α range lost is then the sum of interval I, II and the total overlap time, totaling to (4.733+1.47=) 6.203μsec. This corresponds to 44.66 degrees. The range of α is between 14.4 degrees to 160.3 degrees. Including the overlap angles the lost α range is 44.66 degrees.

For a leakage inductance value of 0.15μH, on the other hand, the interval I stays the same. Interval II is now the sum of 2μsec and the maximum overlap time of one phase, 0.055μsec. Therefore α ranges from 14.4 degrees to 165.2 degrees. The α loss due to the

overlap time of 0.11μsec corresponds to 0.792 degrees. Thus, the total α range loss is 29.998 degrees, which is way less than the case with the higher leakage inductance.

3.2.2 Analytical calculations

The information about the fundamental output voltage is important for the operation of the induction motor. If the rated voltage cannot be obtained at the output, the operation of the motor would not be satisfactory. For this reason, it is required to calculate the peak fundamental output voltage. Another important calculation is required to design the snubber. The response of the snubber circuit to the voltage changes across it is important. Depending on the kind of response required the snubber parameters can be calculated.

3.2.2.1 Output voltage calculation

Consider the bus voltage waveform in Fig. 3.5 where half-period of the ac link voltage with three notches are seen. The output voltage waveform consists of similar waveforms (Fig. 2.7.). As the firing angle for each phase changes the average value of this waveform changes. If the desired voltage waveform is at zero then α is at 90 degrees. The average output voltage waveform for the corresponding half-period is zero. Moreover, if the desired voltage waveform is at its peak then α is required to be zero. However with the constraints stated previously α is set to α_{min}, producing the maximum average output

voltage waveform. In Fig. 3.6.a the output voltage waveform for the first condition is shown giving an average of zero. On the other hand, Fig. 3.6.b shows what happens when the desired voltage is at its peak. For peak desired voltage at the output the maximum average voltage per half period is required and this occurs when α is minimum.

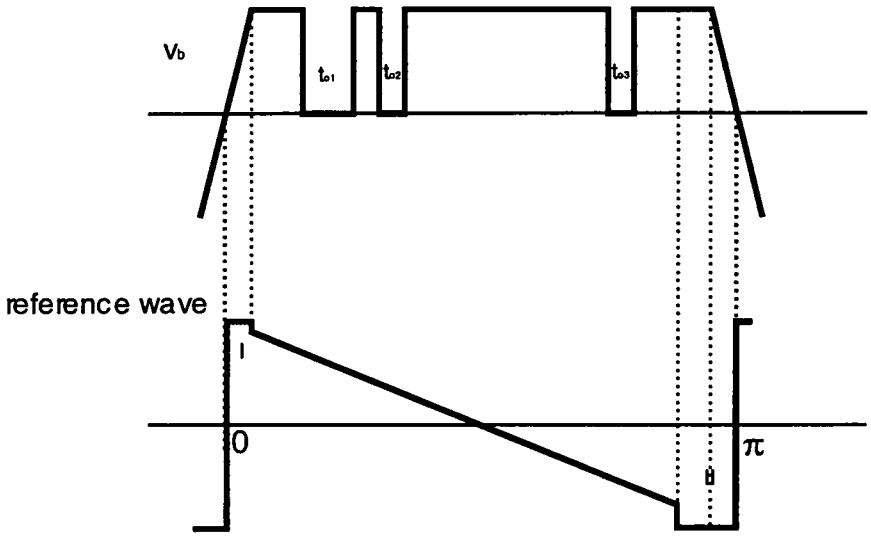


Fig. 3.5: The formation of the reference voltage

Therefore, the peak fundamental voltage can be estimated calculating the maximum average output voltage per half-period of the ac link voltage. To calculate the mean of the output voltage waveform for half a period consider a rectangular voltage angle area, A covering the v_b volt-angle area, the shaded areas and the overlap periods of each phase in Fig. 3.7.

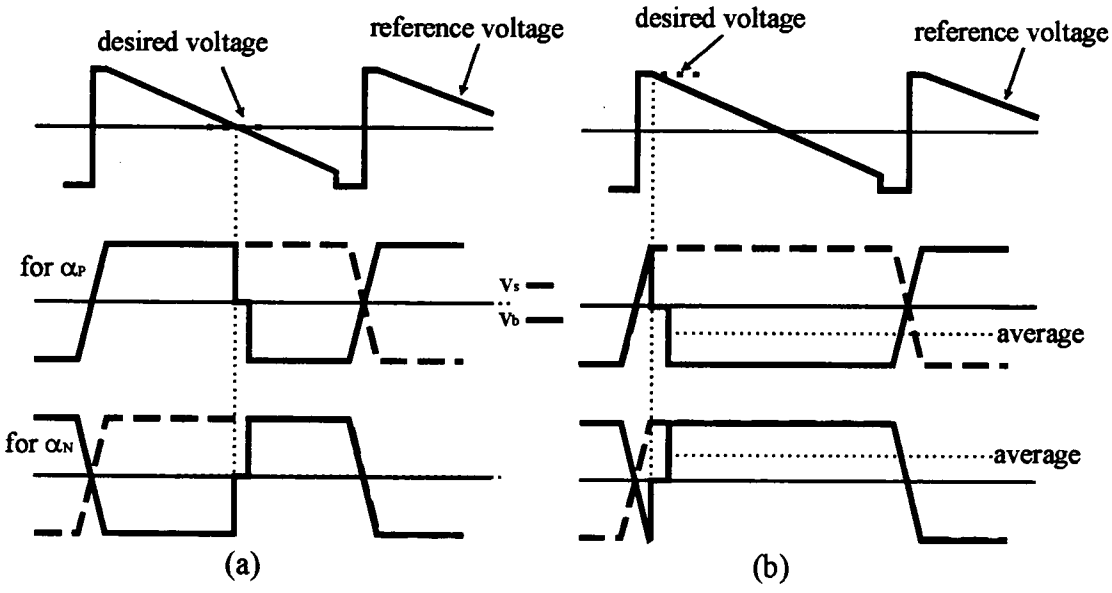


Fig. 3.6: The relation between the desired voltage output and the average of the voltage waveform (for a half-period) Note: For simplicity only one notch is shown instead of three

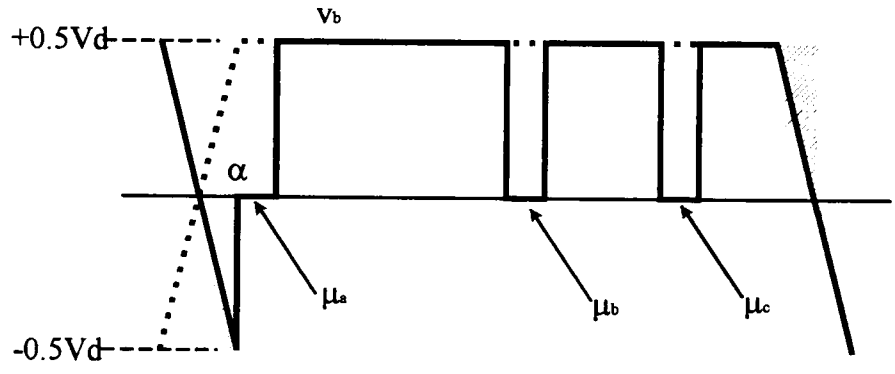


Fig. 3.7: Guiding waveform for output voltage calculations

Then,

$$A = -\alpha\frac{V_d}{2} + (\pi - \alpha)\frac{V_d}{2} \qquad (3.8)$$

To calculate the net area A_{net}, the shaded areas, Δs and the overlap volt-angles corresponding to angles $\mu 1$, $\mu 2$, and $\mu 3$ should be subtracted.

$$A_{net} = A - \Delta - (-\Delta) - \frac{V_d}{2}(\mu_a + \mu_b + \mu_c) \qquad (3.9)$$

resulting in

$$A = \frac{V_d}{2}(\pi - 2\alpha - \mu_a + \mu_b + \mu_c) \qquad (3.10)$$

The average value can be found by dividing this value for the angle corresponding to the half-period, i.e. π.

$$average = \frac{V_d}{2\pi}[\pi - (2\alpha + \mu_a + \mu_b + \mu_c)] \qquad (3.11)$$

In eqn. (3.11), $\alpha=\alpha_{min}$ as stated before for maximum average voltage, which is the fundamental peak voltage.

To be on the safe side, the numerical analysis should be done considering the worst conditions. The worst condition occurs when the average value is minimum, i.e. ($2\alpha+\mu a+\mu b+\mu c$) should be maximum. The $\alpha=\alpha_{min}$ value is inversely proportional to dv/dt value by eqn. (3.7).

Therefore, α_{min} is maximum when dv/dt is minimum. From the previous discussions minimum dv/dt was limited to 150V/μsec. From eqn (3.7), with fs=20kHz, Vd=300 and dv/dt=150V/μsec, α_{min} is calculated to be 0.25 rad or 14.4°.

The sum of the overlap angles is directly proportional to the sum of the absolute values of the line currents.

$$\mu_a + \mu_b + \mu_c = \frac{4Lw_s}{V_d}\left(|i_a| + |i_b| + |i_c|\right) \qquad (3.12)$$

To calculate the maximum overlap angles the maximum sum of absolute values of line current should be found. By analyzing this sum, it is found out that the maximum occurs at twice the peak line current. Then from eqn. (3.12), with fs=20kHz, Vd=300 and peak line current=108.67A, the sum of the overlap angles is found to be 0.36 rad or 20.8°.

Then the average voltage value, which is the same as the fundamental peak voltage for worst condition is

$$average = \frac{V_d}{2\pi}\left[\pi - (2 * 0.25rad + 0.36rad)\right] = 108.92V$$

The calculation of the peak load voltage required for a 30hp machine is found to be 187.8V (Appendix A.1). This value can be reached even with the worst condition if the transformer turns ration is increased to 1.72(=187.8/108.92).

Depending on the load voltage, varying the hfac transformer ratio, required voltage values can be obtained. Note that the values calculated above correspond to the minimum fundamental peak phase voltage. With the changing dv/dt and the phase currents this peak can increase.

Table 3.1: Comparison of Some Analytical Results for Different HFAC Link Frequencies

	f_s=20kHz, 2L=2μH	f_s=50kHz, 2L=2μH	f_s=50kHz, 2L=0.15μH
α_{min}	14.4°	36°	36°
α_{max}	180-19.68=160.32°	180-37=143°	180-37=143°
$\mu_a+\mu_b+\mu_c$	20.8°	52°	3.9°
output peak voltage	108.92V	66V	118.4V
turns ratio required	1:1.72	1:2.84	1:1.59

For large values of the transformer leakage inductance the operation at 20kHz the peak output voltage can be obtained with a transformer turns ratio of 1:1.72 (Table 3.1). To operate at 50kHz, on the other hand requires the turns ratio to be 1:2.84. If low leakage inductance transformer is used then the turns ratio can be kept at 1:1.59. Table 3.1. shows that the converter can possibly operate at 50kHz by increasing the transformer ratio to compensate for the volt-angle losses.

3.2.2.2 Snubber Calculation

A centralized snubber is inserted across the dc bus to avoid the voltage surges due to turning of switches at finite current and to damp the parasitic oscillations caused by the reverse recovery current of the diodes.

The switches are to be turned on at zero current but to detect the exact zero crossing might not be so easy. Therefore, turning off with a small finite current should also be considered during the design of the system. If there is a finite current during turn-off, there is stored energy in the leakage inductors and this should be dissipated. Without the snubber this energy would be dissipated on the off switch and this might damage the device. On the other hand with the snubber inserted, the inductor energy will be stored in the snubber capacitor and some of it will be dissipated on the snubber resistor. This resistive loss is not wanted because it decreases the efficiency of the system. However, considering that with enhanced zero current detection circuits the switches can be turned off at practically zero currents. Then no snubber losses due to finite current switching would occur.

The second use of the snubber, as stated before, is to damp the parasitic oscillations due to the diode reverse recovery current and the parasitic switch capacitance. When a switch is turned off, a reverse voltage is applied to it immediately after switching. This forces the reverse recovery current through the diode in the reverse direction, which goes to zero after a short period of reverse recovery time. During this period, the reverse recovery current finds a path through the parasitic capacitance of a switch and the transformer leakage inductors. This initiates an LC resonance, which can be damped by adding an RC snubber across.

Writing the loop equation for the resonant circuit

$$2L\frac{di}{dt}+Ri+v_c=V_d \qquad (3.13)$$

Adding the capacitor voltage current relationship and arranging, a second order differential equation for the capacitor voltage is obtained.

$$\frac{d^2v_c}{dt^2}+\frac{R_s}{2L}\frac{dv_c}{dt}+\frac{1}{LC_s}=\frac{V_d}{LC_s} \qquad (3.14)$$

To reduce the overshoot it is required that the solution to the capacitor voltage be critically damped which brings the constraint that ξ=1.

Then

$$\xi=\frac{R_s{}^2C_s}{4*2L}=1 \qquad (3.15)$$

For 2L=2μH, it is obtained that $R_s^2C_s=8x10^{-6}$. Now it is required to find another constraint to find the values for the snubber parameters. This can be obtained from the settling point considerations. The settling time can be considered as 4 times the time constant of the system. For the current case, the settling time, T_s is found as

$$T_s = 4\tau = 4\frac{2L}{R_s} \qquad (3.16)$$

The waveforms at 20kHz have a half-period of 25μsec. Therefore assuming that the bus voltage should be established in less than 1μsec at the end of each overlap. The settling time T_s can be chosen to be <<1μsec. Take T_s to be 0.1μsec, then R_s is calculated to be 640Ωs. Inserting this value in eqn. (3.15) C_s is found as 20pF.

With these parameters, the bus voltage overshoot percentage is limited to 10%.

CHAPTER IV

SIMULATION STUDY

The operation of the whole system was described earlier. Then the analysis was given. Before going for the experimental stage, simulation study should be performed to fine-tune the parameters and to evaluate the operation of the system once again. The main advantage of the simulation is that the real-time operation of the system can be modeled with computer time. The results of the simulation study can be compared to the theoretical waveforms to see if they match. If not, there is a problem with the theoretical analysis or the operation of the system. With simulation the converter system can be debugged, the design parameters can be tested, and the problems related to the system can be solved without risking human health and expensive equipment.

There are many tools for simulation purposes. Simulation can be done on computer either by writing a higher order language (PASCAL, C, Fortran, etc.) program or by using one of the Software Programs from the market. The former approach has the advantage of faster execution. On the other hand, these programs are usually written for a specific converter system. Therefore, they are not universal. This means that when simulation of a new converter is required all the programming should start from scratch. The latter approach involves the software programs in the market which are either equation solvers

(Matlab, SIMNON, ACSL, etc) or application specific software programs (Pspice, IsSpice, TINA, etc.). The second set of programs is designed just for circuit analysis. They have the problem of incorporating control blocks and circuit operations together. In addition to this, these programs do not have machine models, which are important for the simulation of electrical drive systems.

Any component can be modeled using differential equations. These equations can be easily solved on any one of the software programs in the first set. For the simulation in this thesis, MATLAB® is chosen because it is a control oriented program and it contains the SIMULINK® toolbox, which offers an easy to use graphical user interface.

4.1 MATLAB and SIMULINK

MATLAB is a technical computing environment used widely for solving problems in control, system analysis and signal processing. It considers the variables as either vectors or matrices and all of the operations are done using matrix algebra. SIMULINK is an extension toolbox to MATLAB with a user-friendly graphical user interface for easier modeling and simulation. Everything that can be done with MATLAB commands, can be done using the blocks in SIMULINK. Every block is designed for specific function with accessible parameters. To create a model, the required blocks from the SIMULINK libraries can be taken and they can be joined by dragging and connecting using a mouse device. The simulation parameters and algorithms can be changed from the menu. The

results of the simulation can be seen on screen through a scope block. Moreover, the C source code of the simulation model can be automatically generated from SIMULINK if required. This can be used in real-time control systems.

For switching circuit simulation, the switch blocks are provided in SIMULINK, which can be used as ideal power electronics switches. With extra blocks, the switches can also be modified to model the practical switches.

4.2 Modeling of HF Inverter

4.2.1 Power Circuit Model

The mathematical model below is derived assuming ideal switches (no switching loss, no conduction drop), i.e. when a switch is on, the voltage across it is zero and when it is off, the current through it is zero. Another assumption is that the transition from one state to the other is instantaneous, i.e., if an on switch is turned off its voltage immediately rises to the full voltage and the current through it instantly drops to zero. Although an ideal model is considered here, it can easily be extended to a model that is more practical.

The basic equations used for the modeling of the inverter are:

$$v_{Q1} = v_{Q3} \tag{4.1}$$

$$v_{Q2} = v_{Q4} \tag{4.2}$$

$$i_{Q1} = i_{Q3} \tag{4.3}$$

$$i_{Q2} = i_{Q4} \tag{4.4}$$

As the equations (4.1) to (4.4) suggest, there is no need to derive equations for all the devices. Instead the model for a half-bridge can be obtained to represent the whole H-bridge because voltages and currents of each pair of switches (Q_1, Q_3) and (Q_2, Q_4) are equal.

$$v_{Q1} + v_{Q4} = V_d \tag{4.5}$$

$$v_{Q2} + v_{Q3} = V_d \tag{4.6}$$

$$i_{Q1} - i_{Q4} = i_L \tag{4.7}$$

$$i_{Q2} - i_{Q3} = i_L \tag{4.8}$$

The operation of the HF inverter was described earlier with different modes in Chapter 2. It can be found out from the mode descriptions that at any instant either a pair of switches (Q_1, Q_3) or (Q_2, Q_4) are on or all the switches are off.

The derivations below consider the commutation of current from Q_1 and Q_3 to Q_2 and Q_4. The reverse commutation is similar with the exception of the subscripts. Therefore, no derivation will be done for the reverse.

4.2.1.1 Equations for Mode 1

Q_1 and Q_3 are ON and Q_2 and Q_4 are OFF

The Thevenin equivalent circuit looking from the load side is the battery with a voltage V_d. The equivalent circuit of the inverter is a current source parallel to a voltage source. The voltage source determines the load voltage and the current source determines the current of the load.

The capacitors C_2 and C_4 are fully charged while C_1 and C_3 are fully discharged

$$v_{Q1} = v_{Q3} = 0 \tag{4.9}$$

$$v_{Q2} = v_{Q4} = V_d \tag{4.10}$$

$$v_S = v_{AB} = v_{Q4} - v_{Q3} = V_d - 0 = V_d \tag{4.11}$$

$$i_{Q1} = i_{Q3} = i_L \tag{4.12}$$

$$i_{Q2} = i_{Q4} = 0 \tag{4.13}$$

4.2.1.2 Equations for Mode 2

All the switches are OFF

In this mode, the current, i_L passes only through the four capacitors, the load and the supply. The current i_L is divided into two at point B. In one direction, it passes through

Q_2 and Q_1 and in the other direction, it passes through Q_3 and Q_4. As seen from the current path, C_1 and C_2 are in series with each other and are parallel to C_3 and C_4, which are in series as the former pair. The Thevenin equivalent circuit from the load side, thus, is a capacitor C_{eq} where $Ceq=(C_1+C_2)//(C_3+C_4)$. With all the capacitance values equal to C, $C_{eq}=C/2+C/2=C$. The complete equivalent circuit is a current source in parallel with a capacitor either charging or discharging it.

If the actual circuit is considered, the current i_s, which equally shared by the capacitors, force C_2 and C_4 to discharge, C1, and C_3 to charge.

From eqn. (4.7)

$$i_L = i_{Q1} - i_{Q4} \tag{4.14}$$

Basic capacitor voltage and current relation

$$i_{Q1} = i_{C1} = C\frac{dv_{C1}}{dt} \tag{4.15}$$

$$i_{Q4} = i_{C4} = C\frac{dv_{C4}}{dt} \tag{4.16}$$

Then,

$$i_L = C\frac{dv_{C1}}{dt} - C\frac{dv_{C4}}{dt} \tag{4.17}$$

$$i_L = C\frac{d}{dt}(v_{C1} - v_{C4}) \tag{4.18}$$

Dividing both sides by C and then integrating gives

$$v_{C1} - v_{c4} = \left[v_{C1}(0^-) - v_{C4}(0^-) + \frac{1}{C}\int i_L dt \right] \tag{4.19}$$

Adding eqn. (4.19) and eqn (4.5) (Note that $v_{Ci} = v_{Qi}$, where i=1,2,3,4)

$$2v_{C1} = V_d + \left[v_{C1}(0^-) - v_{C4}(0^-) + \frac{1}{C}\int i_L dt \right] \tag{4.20}$$

Dividing both sides by 2 to obtain

$$v_{C1} = \frac{V_d}{2} + \frac{v_{C1}(0^-) - v_{C4}(0^-)}{2} + \frac{\int i_L dt}{2C} \tag{4.21}$$

$$v_{C4} = \frac{V_d}{2} - \frac{v_{C1}(0^-) - v_{C4}(0^-)}{2} - \frac{\int i_L dt}{2C} \tag{4.22}$$

$$v_S = v_{AB} = v_{Q4} - v_{Q3} = v_{C4} - v_{C3(or1)}$$

$$= -v_{C1}(0^-) + v_{C4}(0^-) - \frac{\int i_L dt}{C} \tag{4.23}$$

4.2.1.3 Equations for Mode 3

Q_2 and Q_4 are ON and Q_1 and Q_3 are OFF

The Thevenin equivalent circuit looking from the load side is the battery with a voltage $-V_d$. The equivalent circuit of the inverter is similar to the one in mode 1 with a sign change in the battery voltage.

The capacitors C_1 and C_3 are fully charged while C_2 and C_4 are fully discharged.

$$v_{Q1} = v_{Q3} = V_d \tag{4.24}$$

$$v_{Q2} = v_{Q4} = 0 \tag{4.25}$$

$$v_S = v_{AB} = v_{Q4} - v_{Q3} = 0 - V_d = -V_d \tag{4.26}$$

$$i_{Q1} = i_{Q3} = 0 \tag{4.27}$$

$$i_{Q2} = i_{Q4} = i_L \tag{4.28}$$

4.2.1.4 Equations for the Resonant Branch

Resonant branch is parallel to the load and it sees the load voltage, v_s if S_A is on and zero voltage when S_A is off. Therefore, this circuit, when S_A is on, can be considered to be an inductor supplied by v_s. The general voltage current relationship for an inductor supplied by a voltage, v_s, is given by

$$v_s = L_r \frac{di_r}{dt} \tag{4.29}$$

Dividing both sides by Lr and integrating the current through the inductor can be found as

$$i_r = i_r(0^-) + \frac{1}{L_r}\int v_s dt \tag{4.30}$$

The above equation simplifies even more considering that the initial current of the inductor is zero.

$$i_r = \frac{1}{L_r}\int v_s dt \qquad (4.30')$$

When the switch S_A is off, the current through the inductance is zero and i_L is equal to the load current. This is only true for ordinary turn-off conditions. When resonant assisted commutation is in charge, i_L is the sum of the load current and i_r.

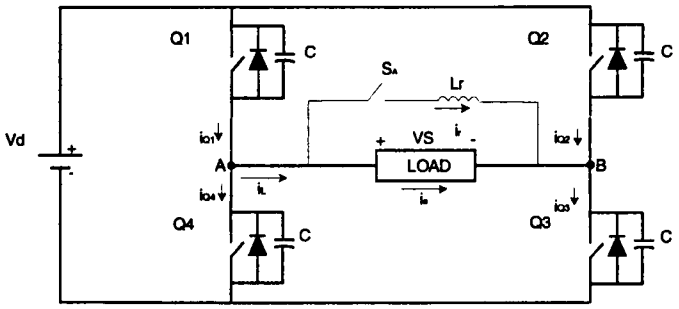
$$i_L = i_r + i_s \qquad (4.31)$$

Modeling equations of the HF Inverter are summarized in Fig. 4.1.

4.2.2 Control Modeling

The control was described earlier in Chapter 2. Here, the application of control for simulation purposes will be explained with the help of Fig. 4.2.

The output voltage waveform obtained is required to be at frequency, f_s. In addition to this, the waveform will have a trapezoidal shape. Therefore, a square wave reference (R) at a frequency, f_s, as shown in Fig. 4.2.a, is required. Notice that the negative portions of this wave are mapped to zero. This reference will force the output to have the same frequency.



General Equations:

$$i_L = i_r + i_s = i_{Q1} - i_{Q4} = i_{Q3} - i_{Q2}$$

$$= C\frac{d}{dt}(v_{Q1} - v_{Q4}) = C\frac{d}{dt}(v_{Q3} - v_{Q2})$$

$$v_{Q1} + v_{Q4} = v_{Q2} + v_{Q3} = V_d$$

$$i_r = \frac{1}{L_r}\int v_s dt \quad , \text{ } S_A \text{ on}$$

$$= 0 \quad , \text{ } S_A \text{ off}$$

MODE-1: (Q_1Q_3-on , Q_2Q_4-off)

$v_{Q1} = v_{Q3} = 0$, $v_{Q2} = v_{Q4} = V_d$

MODE-2: (Q_1Q_3-off , Q_2Q_4-on)

$v_{Q1} = v_{Q3} = V_d$, $v_{Q2} = v_{Q4} = 0$

MODE-3: (Q_1Q_3-off , Q_2Q_4-off)

$$v_{Q1} = v_{Q3} = \frac{V_d}{2} + \frac{v_{Q1}(0^-) - v_{Q4}(0^-)}{2} + \frac{1}{2C}\int i_L dt$$

$$v_{Q2} = v_{Q4} = \frac{V_d}{2} - \frac{v_{Q1}(0^-) - v_{Q4}(0^-)}{2} - \frac{1}{2C}\int i_L dt$$

Fig. 4.1: Modeling Equations of the HF Inverter

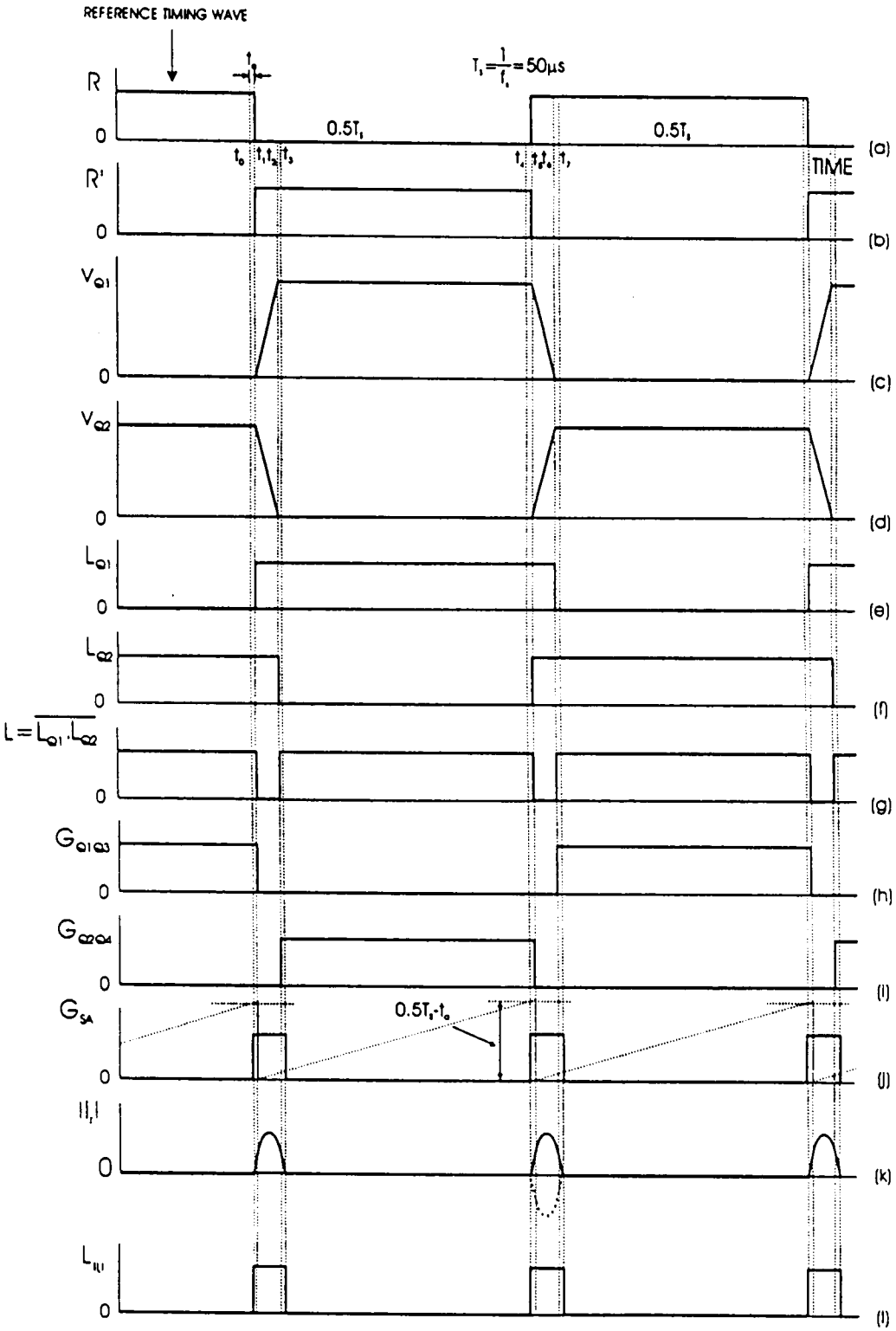


Fig. 4.2: Control Timing diagram of the HF Inverter in RTOF Mode

At the falling edges of this square wave, the switches Q_1 and Q_3 are turned off (Fig. 4.2.h). The inverse of the reference, R' (Fig. 4.2.b) is also used for control. At the falling edges of R, the other switches are turned off (Fig. 4.2.i).

Consider the time t_1, where the previously on switches, Q_1 and Q_3 are turned off, v_{Q1} and v_{Q3} increase while the others decrease (Fig. 4.2.c and d). When v_{Q2} (v_{Q4}) is equal to zero, it is time to turn on Q_2 and Q_4. Likewise, at point t_5 v_{Q1} (v_{Q3}) is equal to zero, so it is time to turn on Q_1 and Q_3. The controller then should check all the capacitor voltages and turn on the switches parallel to the capacitor, which is discharged.

The control of turning on and off the main switches is described above. These discussions are valid for OTOF operation. For RTOF operation the auxiliary switch should also be turned on and off by the controller. Before turning off all the switches, it should be decided if resonant operation is needed or not. If the load current is lower than a pre-specified value, RTOF mode commutation is required. Then the auxiliary switch should be turned on at an advance time, t_a. The advance time can be determined by comparing the $0.5T_s$-t_a value with a resettable counter (Fig. 4.2.j) and turning on S_A at the crossing point. The counter is reset at the edges of the reference wave. The current in the inductor builds up linearly until t_1 when the current level reaches the boost current level. Then all the switches are turned off initiating the resonance between the capacitors and the resonant inductor starts. The variation in the resonant current can be seen in Fig. 4.2.k. S_A is turned off when the current decreases back to zero

at a point t_7.

4.3 Modeling of HFAC-AC Converter

4.3.1 Power Circuit Model

The assumptions made for the modeling of the HF inverter are also valid for the HFAC-AC converter. In addition to these, there are other assumptions. The equivalent circuit used for HFAC transformer is series ideal split voltage sources and split leakage inductance. The resistances from the transformer equivalent circuit are neglected because at higher frequencies the inductance is more dominant and the effect of resistances is negligible. In addition, the impedance of the magnetizing inductance increases with frequency and at high frequencies it can be considered as an open circuit. The turns ratio of the transformer is chosen to be one for simulation purposes.

Note that for easier understanding all the voltages are referenced with respect to a virtual 'o' point which is in between the split voltage sources.

The converter is first divided into two parts: the ac link and the phase legs. The ac-link consists of the ac link supply, the leakage inductance of the high frequency transformer and the RC snubber. The ac link is common to all three phase legs. At first, the equations for the ac link will be derived. Then the model of one phase leg will be given. If phase

leg a is first considered, the operation can be summarized in three modes as explained in chapter 2: S_1 on, S_2 off; S_1 on, S_2 on; or S_1 off, S_2 on. For a more generalized simulation, a fourth mode where both of the switches are off is added. The same phase leg modeling equations can be extended to the other legs quite easily by only changing the subscripts from a to b or c.

The basic equations for the whole converter are:

$$i_{S1} + i_{S2} = i_a \tag{4.32}$$

$$i_{S3} + i_{S4} = i_b \tag{4.33}$$

$$i_{S5} + i_{S6} = i_c \tag{4.34}$$

$$v_{S1} + v_{S2} = v_{s3} + v_{S4} = v_{S5} + v_{S6} = v_b \tag{4.35}$$

$$i_{S1} + i_{S3} + i_{S5} = -(i_{S2} + i_{S4} + i_{S6}) = i_b \tag{4.36}$$

4.3.1.1 Modeling of the AC Link

There are two important variables in the ac link circuit: the leakage inductance current and the snubber capacitance voltage. All other variables can be found from these variables. These two variables can be found by solving a second order differential equation for one and find the other one from this solution. Using basic circuit analysis tools the equations for the bus voltage, v_b as a function of i_s and v_c can be obtained.

$$v_b = v_s - 2L_r \frac{di_s}{dt} \tag{4.37}$$

$$v_b = Ri_C + v_C \tag{4.38}$$

The current voltage relation for a capacitor:

$$i_C = C\frac{dv_C}{dt} \tag{4.39}$$

The relation between the branch currents in the ac link:

$$i_s = i_C + i_b \tag{4.40}$$

Plug eqn. (4.39) in eqn. (4.38) and in eqn (4.40)

$$v_b = RC\frac{dv_C}{dt} + v_C \tag{4.38'}$$

$$i_s = C\frac{dv_C}{dt} + i_b \tag{4.40'}$$

eqn. (4.40) in eqn. (4.37)

$$v_b = v_s - 2L_r\frac{d}{dt}\left(C\frac{dv_C}{dt} + i_b\right)$$

$$= v_s - 2L_rC\frac{d^2v_C}{dt^2} - 2L_r\frac{di_b}{dt} \tag{4.41}$$

Inserting eqn. (4.41) in eqn. (4.38') and arranging terms, give us a second order differential equation as a function of v_c.

$$2L_rC\frac{d^2v_C}{dt^2} + RC\frac{dv_C}{dt} + v_C = v_S - 2L_r\frac{di_b}{dt} \tag{4.42}$$

eqn. (4.42) together with eqn. (4.36) can be solved for v_c. Then, from eqn. (4.40') I_s can be found.

4.3.1.2 Modeling of the Phase Leg –Mode-1

S_1 is ON and S_2 is OFF

Then the switch voltage and currents are:

$$v_{S1} = 0 \text{ and from eqn. (4.32), } i_{S1} = i_a \qquad (4.43)$$

$$i_{S2} = 0 \text{ and from eqn. (4.35), } v_{S2} = v_b \qquad (4.44)$$

and the phase voltage with respect to 'o' point:

$$v_{ao} = \frac{v_s}{2} - L_r \frac{di_s}{dt} \qquad (4.45)$$

4.3.1.3 Modeling of the Phase Leg –Mode-2

S_1 is ON and S_2 is ON

Then the switch voltages and currents are:

$$v_{S1} = 0 \text{ and from eqn. (4.36), } i_{S1} = i_b - i_{S3} - i_{S5} \qquad (4.46)$$

$$v_{S2} = 0 \text{ and from eqn. (4.32), } i_{S2} = i_a - i_{S1} \qquad (4.47)$$

$$v_{ao} = 0 \qquad (4.48)$$

4.3.1.4 Modeling of the Phase Leg –Mode-3

S_1 is OFF and S_2 is ON

Then the switch voltage and currents are:

$$v_{s2} = 0 \text{ and from eqn. (4.32), } i_{s2} = i_a \tag{4.49}$$

$$i_{s1} = 0 \text{ and from eqn. (4.35), } v_{s1} = v_b \tag{4.50}$$

$$v_{ao} = \frac{v_s}{2} - L_r \frac{di_s}{dt} \tag{4.51}$$

4.3.1.5 Modeling of the Phase Leg –Mode-4

S_1 OFF S_2 OFF

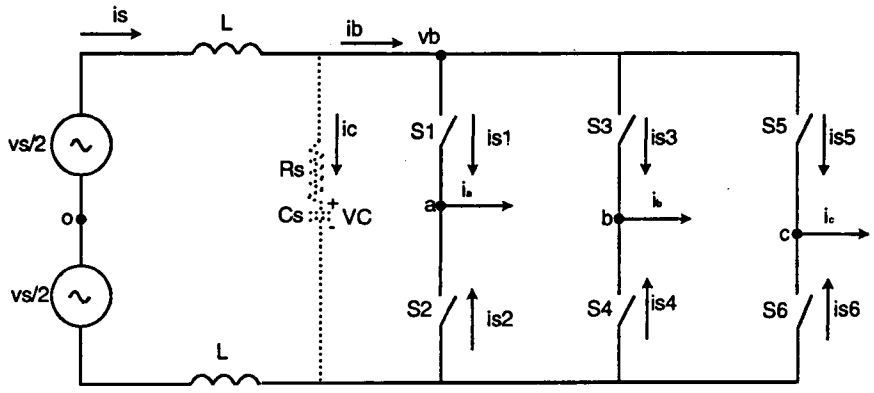
Then the switch voltage and currents are:

$$v_{s1} = \frac{v_b}{2} \text{ and } i_{s1} = 0 \tag{4.52}$$

$$v_{s2} = \frac{v_b}{2} \text{ and } i_{s2} = 0 \tag{4.53}$$

$$v_{ao} = 0 \tag{4.54}$$

The modeling equations of the HFAC-AC Matrix Converter are summarized in Fig. 4.3.



General Equations:

$$v_b = v_s - 2L\frac{di_s}{dt}$$
$$= Ri_c + v_c$$
$$i_c = C\frac{dv_c}{dt}$$
$$i_s = i_c + i_b$$
$$i_b = i_{s1} + i_{s3} + i_s$$

Phase-a:

MODE-1: (S_1-on , S_2-off)
$i_{s1} = i_a, v_{s1} = 0$, $i_{s2} = 0, v_{s2} = v_b$

MODE-2: (S_1-off , S_2-on)
$i_{s1} = 0, v_{s1} = v_b$, $i_{s2} = i_a, v_{s2} = 0$

MODE-3: (S_1-on , S_2-on)
$i_{s1} = i_b - i_{s3} - i_{s5}$, $v_{s1} = v_{s2} = v_b = 0$
$i_{s2} = i_a - i_{s1}$

Fig. 4.3: Modeling Equations of the HFAC-AC MatrixConverter

4.3.2 Control Modeling

As explained previously the HFAC-AC Converter is controlled by phase control. For this reason, a sinusoidal modulating wave and a quasi-triangular carrier wave are required. These waves when compared give the firing instant at the crossing points. At each firing instant, the switch to be turned on is determined by the criteria mentioned in Chapter 2. The turn on signal is ORed with the zero crossing signal, which ensures that the switch is turned off with zero current. The output of the OR is given to the switch gate. If there is an overlap at the same time, the ON signal is postponed until this overlap is done. The firing signal is also ANDed with a current reversal signal, which turns off all the switches if there is a zero crossing and turns the appropriate one with the next firing pulse. For more details please refer to Appendix B.

4.4 The Overall System

The overall system consists of the HF inverter and the HFAC-AC Matrix Converter. Therefore, these two converters should be connected together. During the interconnection of the two converters, there are two major problems: Synchronization and starting up. Synchronization is solved by obtaining the reference wave from the output of the inverter through waveform manipulations. For starting, the priorities are set as inverter first and then converter, i.e. the inverter starts working first, building the ac link voltage

waveform. In the mean time the firing signals are disabled by the 'Enable the hfac-ac converter switches' block. After the ac link voltage is established, the firing signal of the converter are enabled and the converter starts working.

4.5 Results

After the simulation model is obtained, necessary circuit parameters are selected according to the analysis results. The parameters used in the simulation are summarized in Table 4.1.

In Fig. 4.4, the operation of the hf inverter in OTOF mode for a small time segment corresponding to three cycles is seen. The top graph shows the ac link voltage and current plotted on top of each other. This operation corresponds to full load operation, i.e. when the peak currents are at 110A. Resulting from the OTOF mode the voltage transition is linear. In addition to these, it can also be observed how the ac link current is lagging the voltage waveform. The lag angle is less than 90 degrees corresponding to motoring operation. Another point to consider is that the three commutation steps can be observed on the ac link current. Note that no commutations occur during the transition of the ac link voltage. The second graph shows the capacitor voltage for a pair of switches. Remember that the voltages of the diagonal pair of switches are equal. The corresponding capacitor currents are given in the next graph. The capacitor current is the slope of the capacitor voltage. Therefore, for a linear capacitor voltage increase, the current is

Table 4.1: The values of the circuit components used in the simulation

Symbol	Definition	Value
HF Inverter:		
C	Lossless snubbers	0.4μF
Lr	Resonant inductor	1.01μH
HF Transformer		
L	Secondary leakage inductance	1μH
1:n	Turns ratio	1:1
HFAC-AC Matrix Converter		
Rs	Snubber resistance	640Ω
Cs	Snubber capacitance	20pF
3-phase current source load		
Vpeak	Peak value of the sine wave	110A
fo	Frequency	200Hz
ϕ	Phase shift	30°

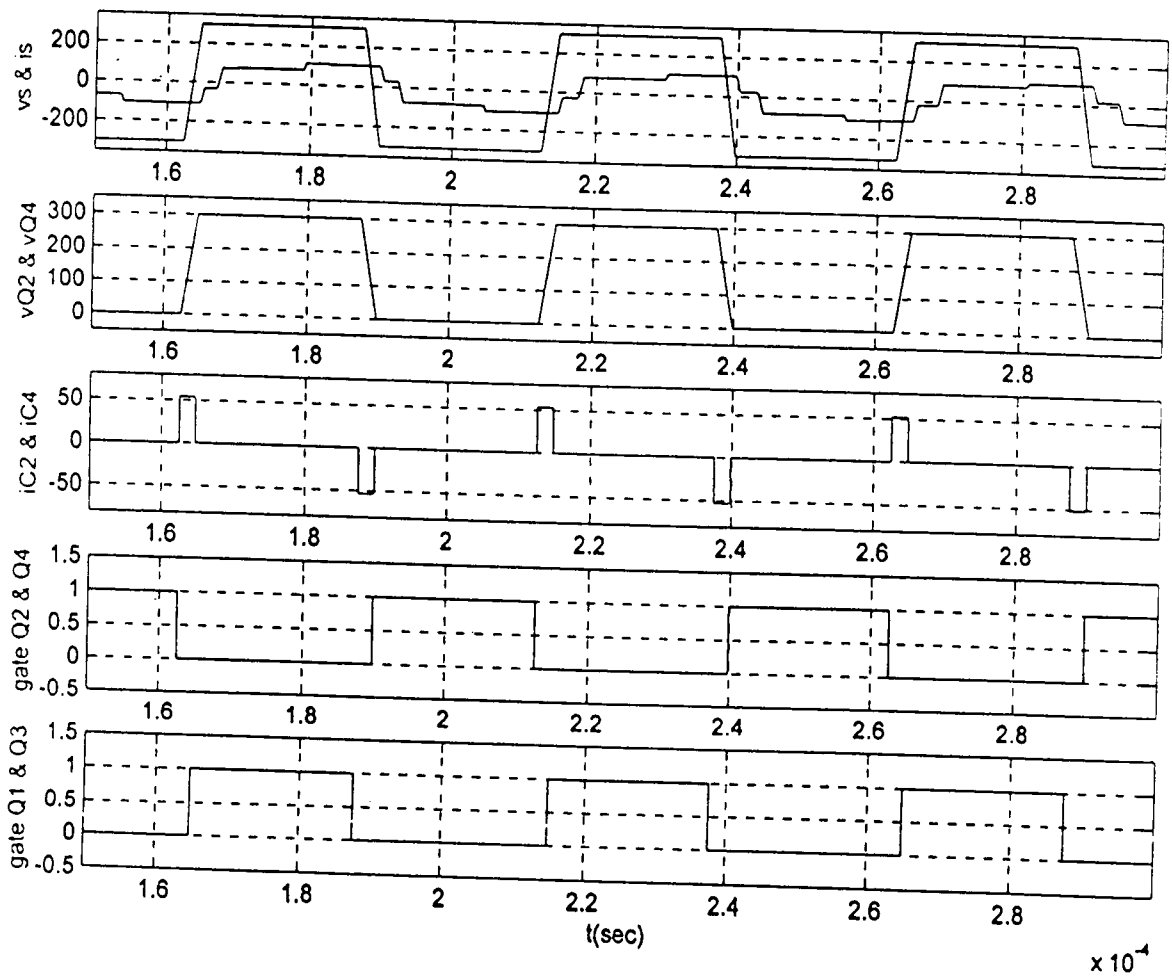


Fig. 4.4: HF Inverter Simulation Performance-OTOF Mode

constant and its sign is the same as the sign of the slope. For constant capacitor voltage the capacitor current is zero. The two bottom graphs show the gate signals. Notice that they are all zero during the voltage transition.

At light load the operation of the hf inverter is different due to the resonant assisted commutation. The waveforms corresponding to RTOF mode operation of the hf inverter are shown in Fig. 4.5. The difference from the previous figure is that the ac link current magnitude is decreased and the capacitor current waveform is modified due to resonance. The capacitor charging and discharging currents in the RTOF mode have an additional resonant current. This additional resonant current waveform is also shown below the capacitor current graph. The resonant current is zero accept during the voltage transition, therefore it is like a group current pulses with alternating polarity. The polarity is the same as the polarity of the ac link current during the transition. The next figures unlike the previous ones correspond to the operation of the hfac-ac matrix converter. The first one, Fig. 4.6 shows the interaction of the three phases. The top graph shows the bus voltage and the corresponding ac-link current for a full cycle of the ac-link. Here, the three notches corresponding to each phase can be seen. Under this graph, the reference voltage and the modulating voltage waveforms are given. It can be clearly observed that the crossing points of the reference voltage with the modulating waveforms give α for each phase. Starting with each crossing point, both of the switches are on, inserting a notch on the bus voltage. The corresponding switch currents are shown on the three bottom graphs where during the overlap period the current in one of the switches

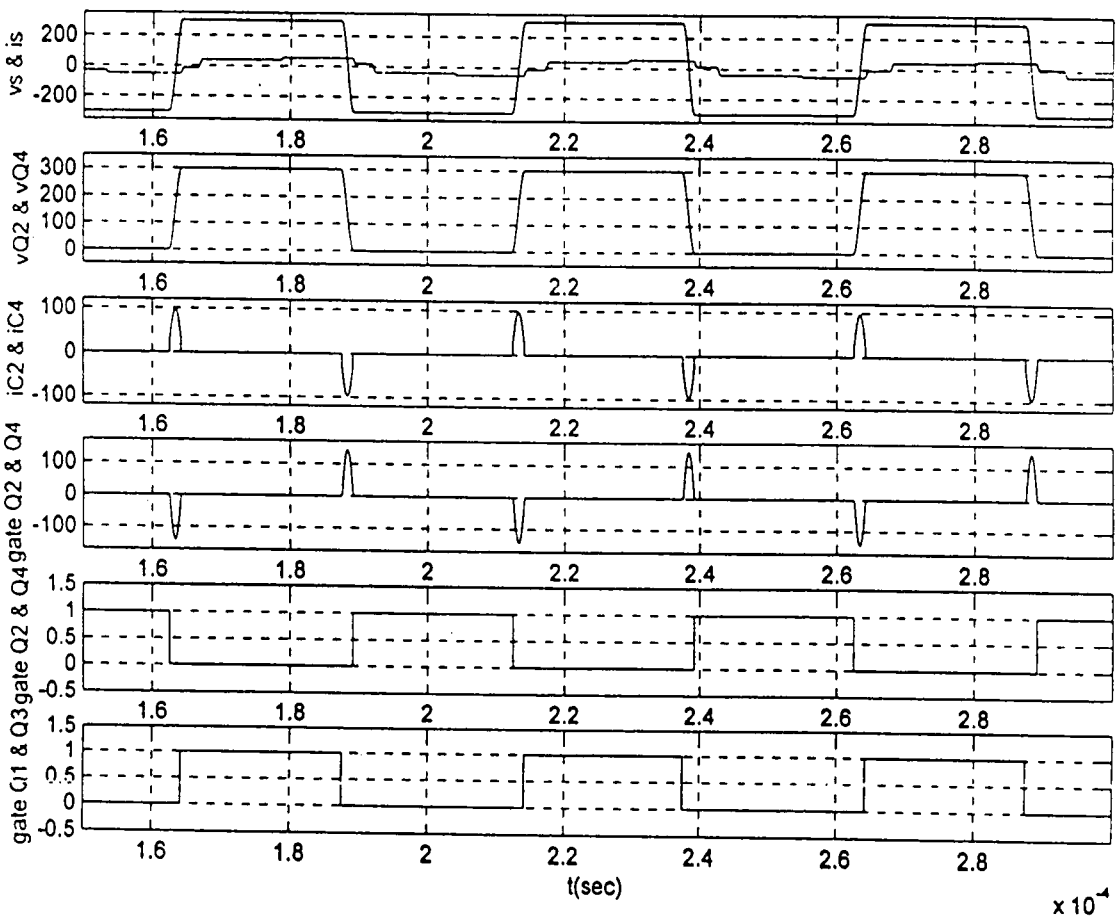


Fig. 4.5: HF Inverter Simulation Performance-RTOF Mode

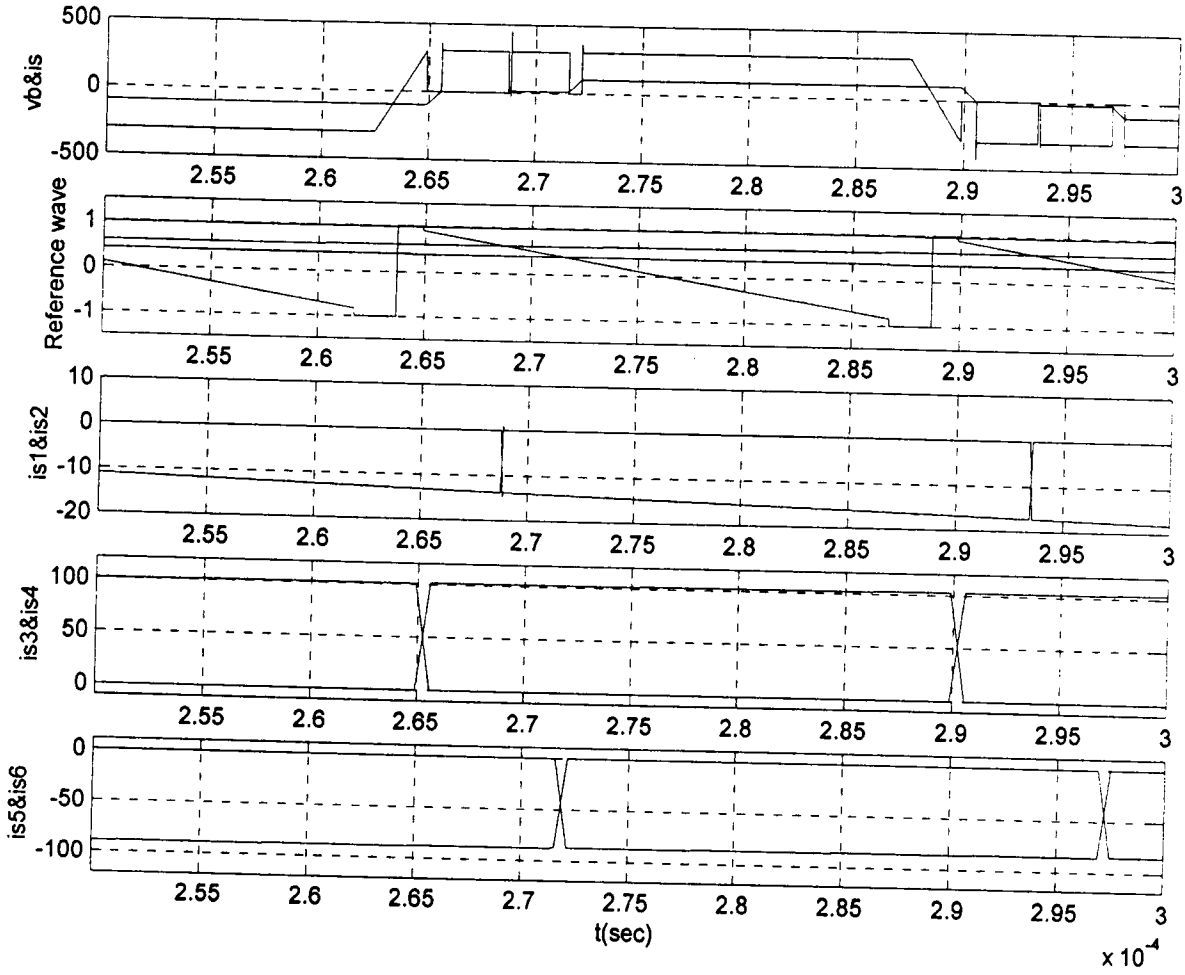


Fig. 4.6: Simulation Waveforms Explaining the Interaction of Three Phases of HFAC-AC Matrix Converter

decrease while the current in the other one increases. Notice also that the overlap period and therefore the notch on the voltage bus ends when one of the switch currents are zero. The top graph also shows that the ac link current is constant except for the overlap period where it increases or decreases corresponding to the phase leg currents. In the top graph, the bus voltage has an overshoot when a switch is turned off and the full bus voltage is established. This shows that the corresponding switch turns off with a finite current. For discrete time simulation, to obtain the exact zero, the sampling time should be decreased. Then simulation takes a lot of time. With the current sampling time, exact zero detection is a problem therefore the switches are not turned off at zero. In the practical system the problem of zero crossing detection can be solved and then no overshoot is expected.

The phase voltages are given in Fig 4.7. The top graph shows the corresponding ac link voltage and current. Then three phase voltages with neutral connection are given. If observed carefully even with a small segment of voltage waveform the phase control and the variation of the firing angle can be seen. The last graph in this figure shows the phase voltage with isolated neutral where one-third and two-thirds levels of the bus voltage are seen. Note that, this is typical for a phase voltage with isolated neutral. To solve the problem of current reversal a method was proposed earlier. The application of this method in simulation can be seen in Figs. 4.8 and 4.9 the reversal in both directions is simulated. The top graphs in both of the figures show the ac link voltage and current waveforms while the second graph shows the phase current. Note that when the current reverses, all the switches are turned off, i.e. all gate signals are zero. Then the phase

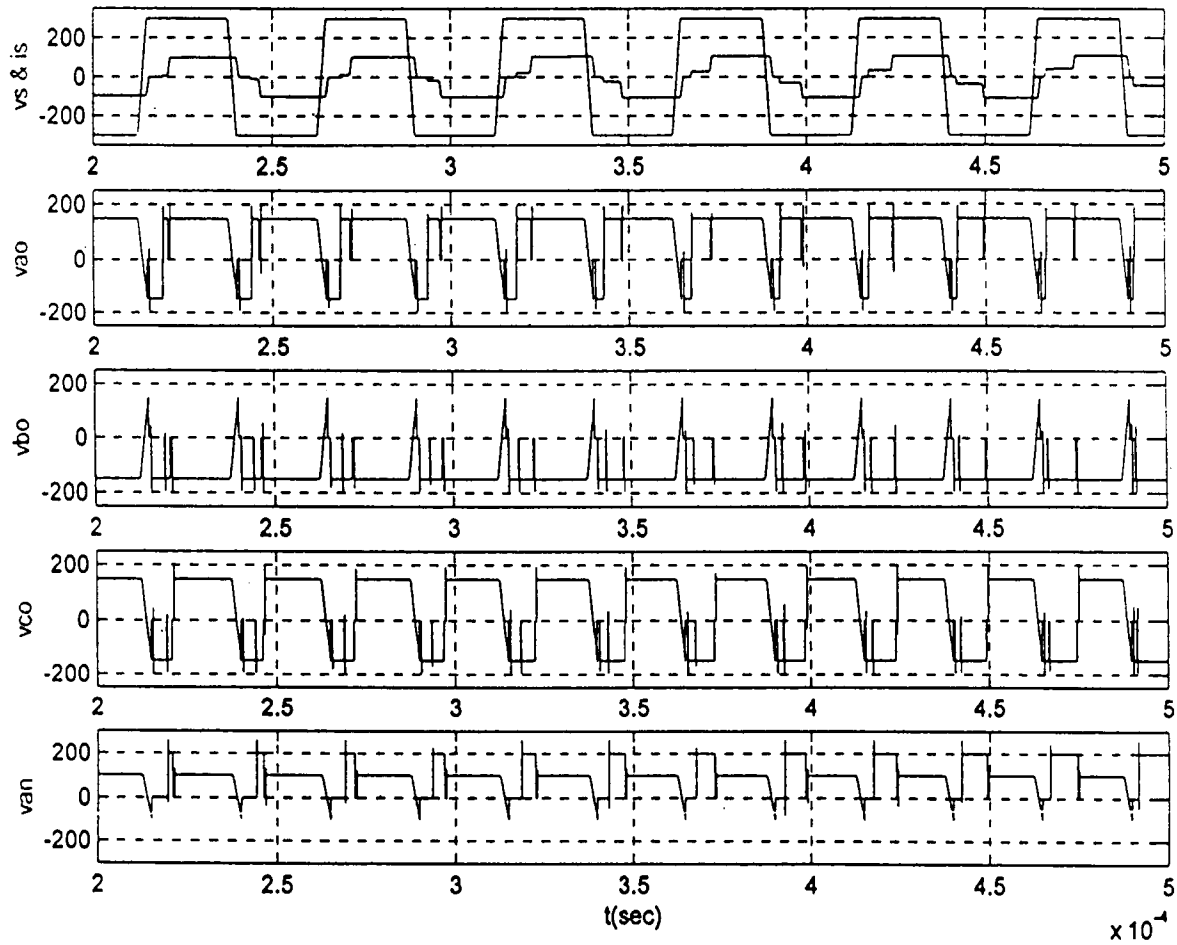


Fig. 4.7: Simulation Voltage and Current Waves of HFAC-AC Matrix Converter

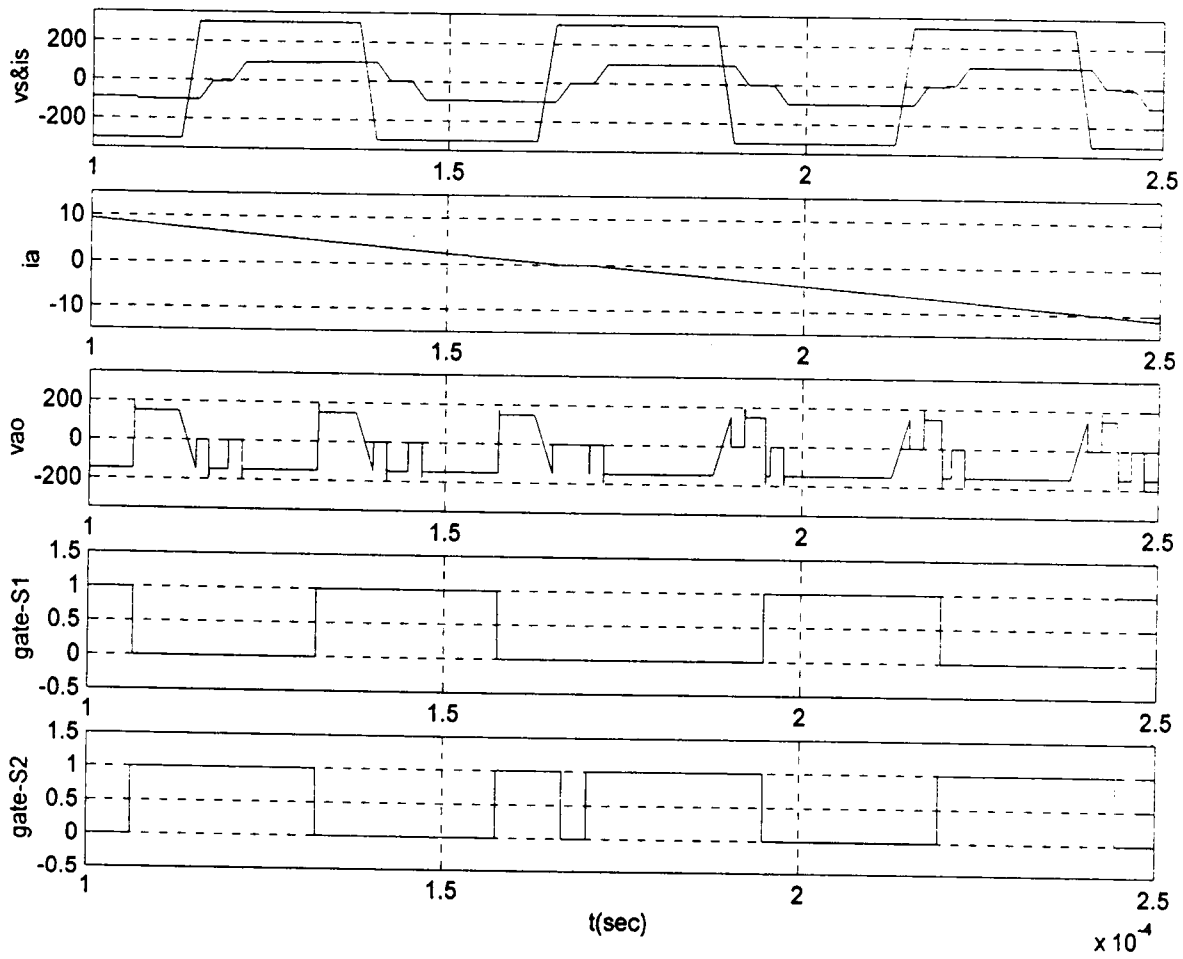


Fig. 4.8: Simulation Waveforms of HFAC-AC Matrix Converter
(Transition from $+i_a$ to $-i_a$)

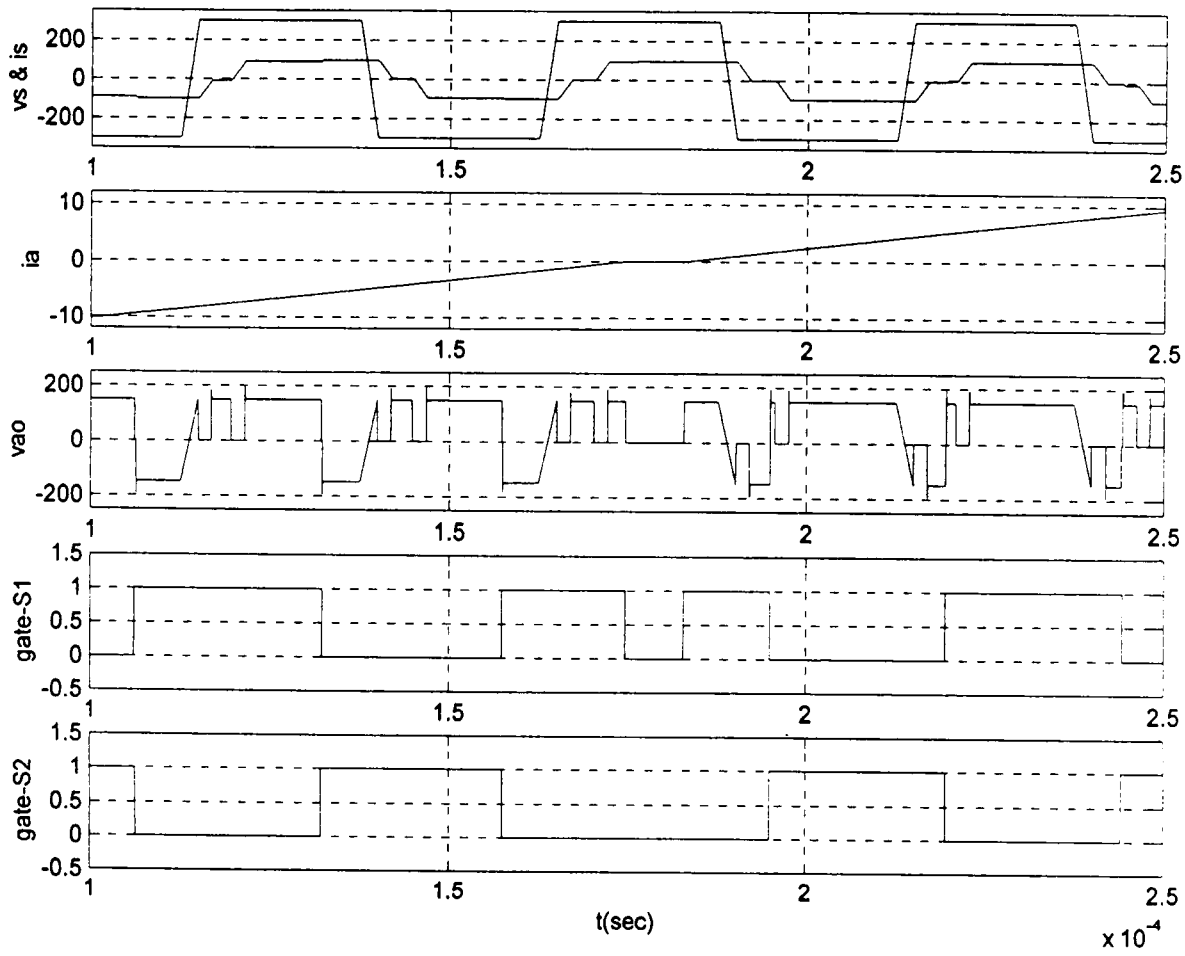


Fig. 4.9: Simulation Waveforms of HFAC-AC Matrix Converter
(Transition from $-i_a$ to $+i_a$)

current stays at zero. With the next firing pulse the gate signals are enabled again and the current starts to build up in the reverse direction. During the zero current period, the output voltage is also zero because the switches are off. Note that the current reversal only effects the operation of the corresponding phase. All other phases operate in normal condition.

This is a high frequency converter simulation. The ac link frequency is at 20kHz while the output frequency is at 200Hz. This means that there are 200 periods of ac link voltage in one full cycle of the output. To show the output voltage waveforms for a full cycle on a small graph would be meaningless considering all the notches and spikes. The aim is to show that the converter operates satisfactorily. The figures presented here show that everything works properly.

CHAPTER V

CONCLUSION

This work includes the studies on a performance enhanced DC-HFAC-AC converter system for AC drive. First the literature search is done to see the work in the field of soft-switching converters. Then the converter topology is developed. With the necessary waveform and mathematical analysis the feasibility of the system is proved and basic controls are formulated. The converter is simulated with the basic controls for a current source load using the simulation software MATLAB-SIMULINK. The simulation results are compared with the theoretical ones. The results show satisfactory performance of the converter. All the switches in the converter turn on and off with zero voltage or current switching, which greatly reduces the switching losses thus increasing the efficiency. Unlike most other soft-switched converters the commutations are mostly non-resonant, which decreases the resonant circuit losses. The lightweight high frequency transformer in the ac link, on the other hand brings the advantages of isolation and voltage boost. Moreover if required auxiliary supplies can be tapped from this transformer.

The drive system using this converter is intended for an electrical vehicle type of drive but it can also be extended to industrial type of drive. Following this work, for further study, the converter model will be coupled to a 30hp machine. The simulation will be

extended to include higher order controls like volts/hertz or rotor flux oriented vector control. Some intelligent control methods will also be added for estimation purposes and performance enhancement. All the computations will be done by a Texas Instruments TMS320C30 model DSP processor board. The ac link frequency will be at 20kHz initially. The aim is to increase this frequency to 50kHz.

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APPENDICES

APPENDIX A

CALCULATIONS AND DERIVATIONS

A.1 Load Considerations

The overall system is designed as a 30hp induction motor drive. However, in this work the load is considered to be a three phase current source. The peak current value, frequency,and phase shift values used are calculated for the induction machine with the ratings given in Table A.1.

Table A1: Induction machine ratings

Induction Motor 30hp, 230 V_L, 4pole 0-300Hz, f_b=200Hz cosϕ=0.85, η=0.86 at full load
R_s=0.025Ω R_r=0.025Ω L_s=255μH L_r=255μH L_m=2.61mH

The frequency and the phase shift are given in the table. The only rating to be calculated is the current rating, which is found using the three-phase power equation.

$$P_{in} = \sqrt{3} V_L I_L \cos\phi \qquad \text{(A-1)}$$

Leaving I_L alone on one side and inserting

$$P_{in} = \frac{P_{out}}{\eta} \qquad \text{(A-2)}$$

gives

$$I_L = \frac{P_{out}}{\eta\sqrt{3} V_L \cos\phi} = \frac{22.4 * 745.7}{0.86 * \sqrt{3} * 230 * 0.8} \qquad \text{(A-3)}$$

This calculation results in rms load current of 76.84A. The peak load current on the other hand can be obtained by multiplying this value by $\sqrt{2}$, which gives 108.67A.

A.2 dvs/dt and di/dt Expressions

The rate of change of v_s corresponds to the slope of v_s during commutation. The differential equation of the ac link current with respect to the ac link voltage is

$$i_s = C\frac{dv_s}{dt} \qquad \text{(A-4)}$$

Taking the integral of both sides

$$v_s = v_s(0^-) + \frac{1}{C}\int i_s dt$$

$$= v_s(0^-) + \frac{I_{so} t}{C} \qquad \text{(A-5)}$$

where I_{so} is the ac link current during transition. Although this current varies, it is considered constant for the short duration of the commutation in OTOF mode. In RTOF mode the integral in eqn. (A-14) cannot be integrated so easily because i_s is not constant and includes a resonant component.

Then the slope of voltage rise for the OTOF case

$$\frac{dv_s}{dt} = \frac{\Delta v_s}{\Delta t} = \frac{I_{so}}{C} \qquad \text{(A-6)}$$

The differential equation of the ac link voltage with respect to the ac link current is

$$v_s = 2L\frac{di_s}{dt} \qquad \text{(A-7)}$$

Noting that v_s is constant at $\pm 0.5V_d$ in the overlap period and taking the derivative of both sides

$$i_s = i_s(0^-) + \frac{1}{2L}\int v_s dt$$

$$= i_s(0^-) + \frac{\pm 0.5V_d t}{2L} \qquad \text{(A-8)}$$

Therefore,

$$\frac{di}{dt} = \frac{\Delta i}{\Delta t} = \frac{0.5V_d}{2L} \qquad \text{(A-9)}$$

A.3 α_{min} and μ Equation Derivation

Equations for α_{min} and μ are used in the previous chapters. Below, these equations will be derived. The angles are found by

$$angle = \omega_s t \qquad \text{(A-10)}$$

where t is basically the time corresponding to the angle.

Therefore,

$$\alpha_{min} = \omega_s t_{\alpha_{min}} \qquad \text{(A-11)}$$

α_{min} corresponds to the point where the ac link voltage reaches $\pm 0.5V_d$. As a result, the voltage rises from zero to full $\pm 0.5V_d$ in $t_{\alpha min}$.

$$\frac{dv}{dt} = \frac{\Delta v}{\Delta t} = \frac{0.5V_d}{t_{\alpha_{min}}} \qquad \text{(A-12)}$$

Taking $t_{\alpha min}$ from eqn. (A-6) and inserting it in (A-5), gives the expression for α_{min}.

$$\alpha_{min} = \frac{\omega_s * 0.5V_d}{\frac{dv}{dt}} \qquad \text{(A-13)}$$

The overlap angle μ can be found in a similar fashion. The only difference being in the calculation of the time.

$$\frac{di}{dt} = \frac{\Delta i}{\Delta t} = \frac{|i|}{t_\mu} = \frac{0.5V_d}{2L} \qquad \text{(A-14)}$$

where $|i|$ is the magnitude of the corresponding phase current

Taking t_μ from here and inserting it into the time angle equation gives the following:

$$\mu = \frac{\omega_s * 2L}{0.5V_d}|i| \qquad \text{(A-15)}$$

μs for individual phases can be calculated and added to find the sum of the of the overlap angles.

The sum of the absolute values of all the phase currents is required in the calculation of the overlap angles. Therefore this calculation is done for balanced three phases each with a magnitude of one. The values of the maximum, minimum and average are 1.9997, 1.7321, and 1.9079 respectively.

A.4 Load Considerations for the HF Inverter

As stated previously, the load for the hf inverter is the hfac-ac matrix converter. The inverter produces the load voltage, but the secondary converter determines the load current.

Assuming one hundred percent efficiency of the matrix converter, the full-load power rating of the ac link should be equal to the input power rating of the load. Therefore,

$P_{aclink} = P_{in} = \frac{P_{out}}{\eta} = 26.02kW$ and

$$P_{aclink} = V_s I_s \cos\phi_i \qquad \text{(A-16)}$$

where V_s = rms voltage of the fundamental ac link voltage

I_s = rms current of the fundamental ac link current

ϕ_i = phase angle between voltage and current in the ac link

If v_s is assumed to be a square waveform, then

$$V_s = \frac{4}{\pi} V_d \frac{1}{\sqrt{2}} = 270.09V \qquad \text{(A-17)}$$

ϕ_i can be found through a table from [8] (r=1) to have a cosine of 0.75.

Then I_s can be calculated

$$I_s = \frac{P_{aclink}}{V_s \cos\phi_i} = \frac{26.02KW}{270.09 * 0.75} = 128.45A \qquad \text{(A-18)}$$

This also corresponds to the primary current of the transformer.

The value of the current at the zero crossing of the fundamental ac link voltage can be determined as

$$I_{s0} = i_{s,peak} \sin(\cos^{-1}\phi_i) = \sqrt{2} * 128.45 * \sin(41.41°) = 120A$$

This is the maximum ac link current, $I_{so,max}$ during the commutation of the hf inverter.

A.5 Analysis of an LC Circuit

The resonance in the hf inverter during the RTOF mode is basically an LC resonance. To have a better understanding of the resonant behavior of the circuit, consider an ordinary source free LC circuit such as the one shown in Fig. A.1.

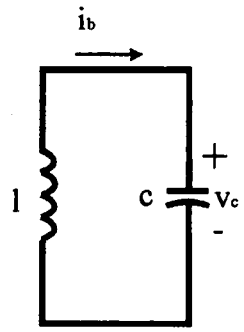


Fig. A.1: Circuit Diagram of a Source-free LC circuit

Writing the loop equation.

$$v_c = v_l = l\frac{di}{dt} \qquad \text{(A-19)}$$

This equation turns into a second order ordinary differential equation if the voltage current relation of the capacitor

$$i = -c\frac{dv_c}{dt} \qquad \text{(A-20)}$$

is inserted in eqn. (A-19).

$$-lc\frac{d^2v_c}{dt} = v_c \qquad \text{(A-21)}$$

or

$$\frac{d^2 v_c}{dt} + \frac{1}{lc} v_c = 0 \qquad \text{(A-22)}$$

The general solution to this differential equation is

$$v_c = A\cos(w_o t) \qquad \text{(A-23)}$$

where A is a constant

and $$w_o = \frac{1}{\sqrt{lc}} \qquad \text{(A-24)}$$

The initial condition for this case is $v_c(0^-)=V_d$. Therefore applying this initial condition to eqn. (A-24) gives the solution for the capacitor voltage is found to be

$$v_c = V_d \cos(w_o t) \qquad \text{(A-25)}$$

The resonant current on the other hand is the derivative of (A-25) multiplied by the capacitance value, giving

$$i = -V_d w_o \sin(w_0 t) \qquad \text{(A-26)}$$

Both the current and the voltage are sinusoidal with an expected frequency of w_o as expected. Thus, the period for the resonance waveform is $\frac{2\pi}{w_o}$, i.e. $2\pi\sqrt{lc}$.

For the full resonance analysis of the RTOF mode of operation, the effects of i_s and I_{boost} should also be considered. The boost current serves as an initial condition for the resonant current while i_s aids in charging and discharging of the capacitors.

APPENDIX B

SIMULATION BLOCKS

The MATLAB-SIMULINK simulation file is given in Plate 1 at the end of this thesis. The software versions are MATLAB 4.2 and SIMULINK 2.1. If the simulation program is run under MATLAB 5.1, then necessary conversion should be made. Note that during conversion problems might arise. It is recommended to use the original version.

The explanations for the simulation program are given below with associated block diagrams.

B.1 Simulink Implementation of HF Inverter Model

B.1.1 Power Circuit

Simulink implementation should start by implementing the switches first. As seen from the equations in Section 4.2.1, the important variables are capacitor and/or switch voltages. As stated earlier, ideal switches are used in the simulation. This means that when a switch is on, the voltage across it is equal to zero. Simulink has a built-in switch

block (Fig B.1 Q_1 and Q_2) , which has three inputs: if the second input is greater than a threshold voltage, then the output is the first input, otherwise it is the third input. In Fig B.1, it can be seen that the switches Q_1 and Q_2 are represented as Simulink switch blocks. The second input is the gate in this case. When the switch is on, the output, which is the capacitor voltage, is zero. What happens when the switch is off, depends on the capacitor charging or discharging. This happens in the second mode when all of the switches are off. Therefore, if the gate signals are ORed, a signal to control the charging circuit. This charging circuit model is simply but the implementation of eqn.s (4.21) and (4.22). The saturation blocks D1 and D2 serve as the diodes, which keep the switch voltage always positive. The load current i_L consists of two components (eqn. 4.21). These components are added by the block Sum2 and given as input to the charging circuit. The resonant current component of the load is taken from the resonant circuit. The resonant circuit is implemented using eqn. (4.30'). In this circuit, the model of the auxiliary switch is different compared to the other switch models; it works as an enable. If a positive gate signal is given to the gate (second input) of S_A, it enables the resonant circuit building up the resonant current by integrating v_s. When it is turned off, it disables the resonant circuit and resets the Reset Integrator in order to keep the resonant current at zero.

This power circuit model is converted into a block named 'hf inverter' (Fig. B.2) with control inputs: gate-1 (input1), gate-2 (input2) and gate-SA (input6). The other inputs are the battery voltage, V_d (input4), and the load current, i_s (input3). The outputs are the capacitor voltages v_{C1} (=v_{C3}) (output2), and v_{C2} (=v_{C4}) (output4), the capacitor currents

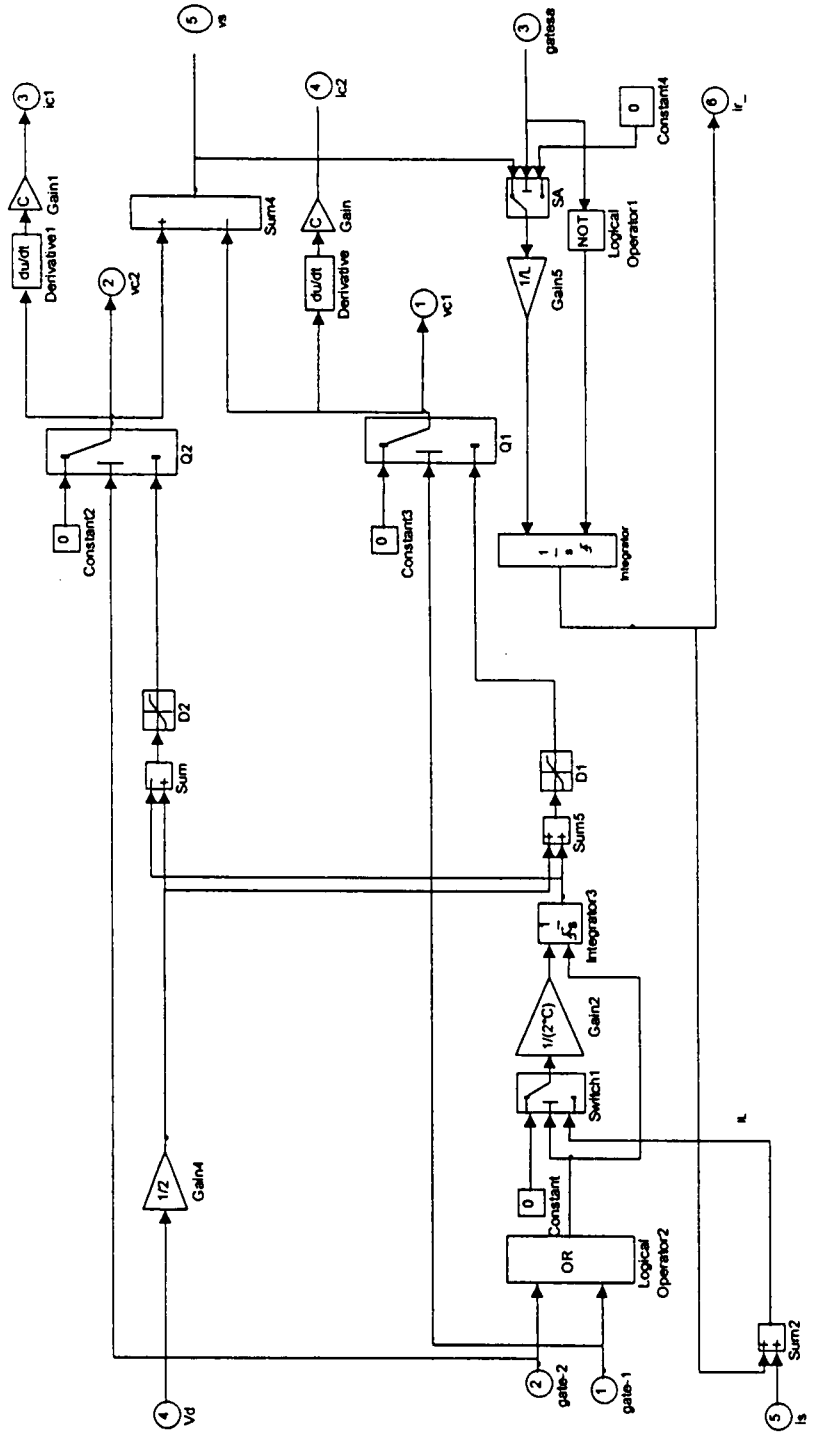


Fig B.1: SIMULINK Block Diagram of the HF Inverter Power Circuit

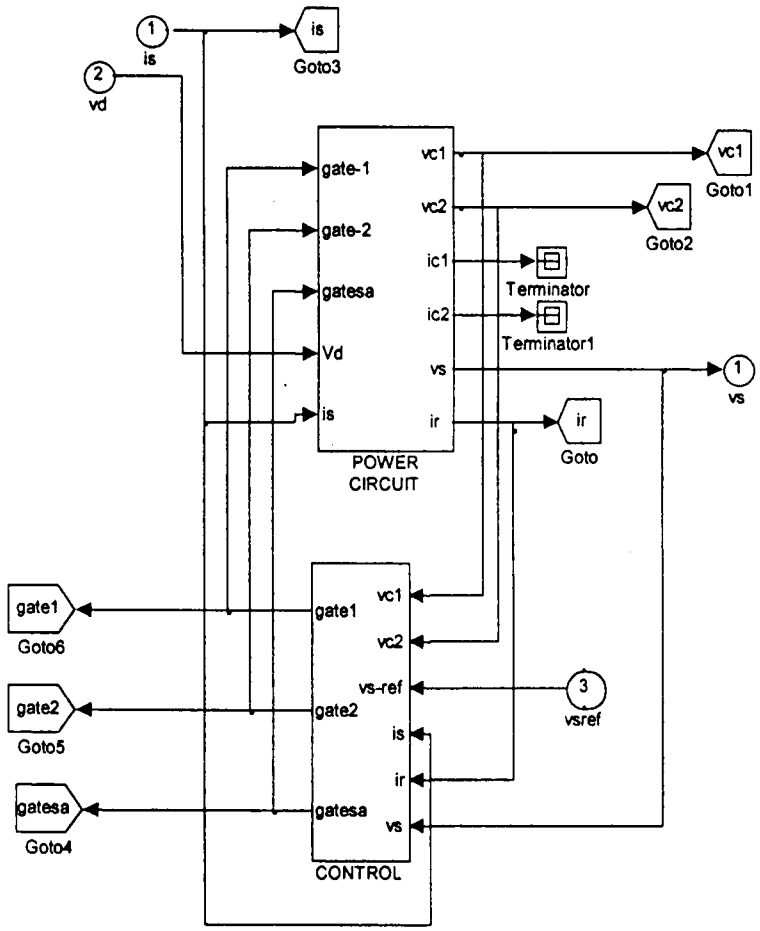


Fig. B.2 : Simulink Block Diagram of the HF Inverter Showing the Connection of Power Circuit Block and the Control Block

i_{C1} ($=i_{C3}$) (output5), and i_{C2} ($=i_{C4}$) (output1), the output voltage, v_s (output3), and the resonant current, i_r (output6).

B.1.2 Control Circuit

The algorithm for control of the hf inverter is implemented in Simulink (Fig. B.3) using the waveforms in Fig. 4.2 as a basis. First, signal R and R' are obtained by comparing the reference voltage with zero. The signals thus obtained are ANDed (Fig. B.3) with another signal L. This signal, L is obtained by NANDing two other signals, L_{Q1} and L_{Q2} (Figs. 4.2.e and f), which are zero, if the corresponding switch is on, and one vice versa. L_Q signals are obtained by finding the zero region of the capacitor voltages. The signal, L is used to keep all of the switches off during Mode-2. This concludes the implementation of control for the OTOF mode.

For the RTOF mode, the resonant circuit must be included, so the gating signal should be produced for the auxiliary switch. Before describing the RTOF control implementation, the decision between RTOF and OTOF operations should be clarified. For simulation purposes the boundary for i_s between low current and high current is chosen to be 50 percent of the load current, i.e. 60Amps. The absolute value of i_s is compared with 60. If i_s is larger than 60, then the output is a zero which disables the resonant operation, otherwise the resonant operation is initiated. The decision is given 1μsec before the advance time. Therefore, the correct instant is calculated from the 'ta-1us' block, which is

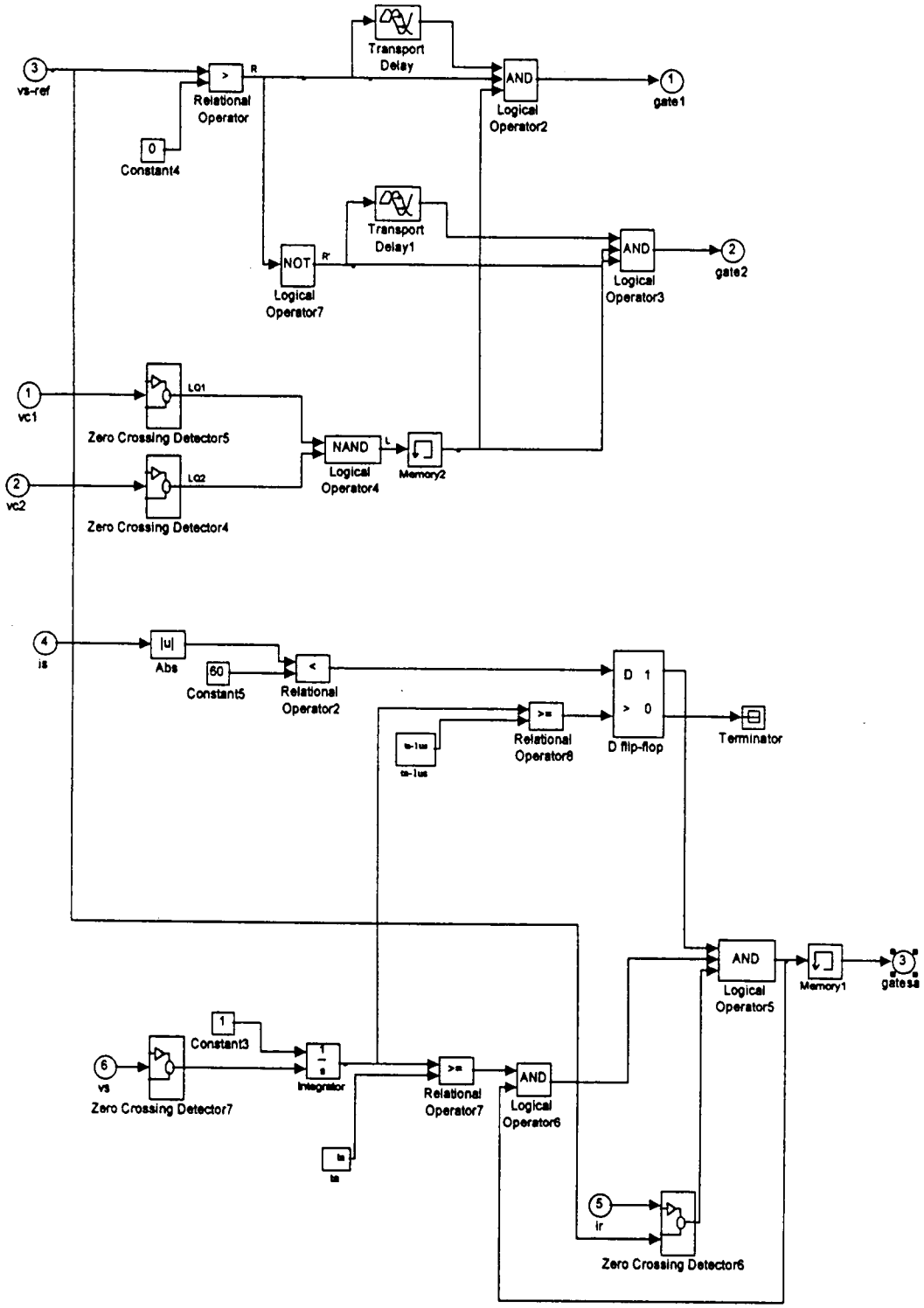


Fig. B.3: SIMULINK Block Diagram of the HF Inverter Control

compared to a counter to produce a clock to the D flip-flop. This way, the decision is done at discrete time instants just before all the switches are turned off. After deciding which control to use, assuming that RTOF was selected, the advance time should be found. This is calculated and then subtracted from $0.5T_s$ by the block called 'ta'. The calculated value is compared to the counter value (Fig. 4.2.j). The counter integrates the constant '1', giving a ramp as output. The counter is reset after each zero crossing of v_s. Therefore, the value of the counter at any time is the time passed after the last zero crossing of the ac link voltage. The crossing points of the counter and the time value, in Fig. 4.2.j, are the instants to turn on S_A. The turning off of S_A depends on the resonant current. The 'Zero Crossing Detector6' block gives a zero output if the resonant current reaches zero, which turns S_A off. Thus, the decision of turning S_A on and off is made by ANDing three control signals, which are : 1) RTOF-OTOF decision, 2) advance time, t_a before turn off is reached and 3) inductor current zero signals.

Note that there are extra two different kinds of Simulink blocks used in Fig. B.3. One of them is the 'delay' block, which breaks the algebraic loops in the model. The other block is the 'Transport Delay' block, which delay the input for the time specified in the parameters. This delay is used to prevent the problems of ANDing in Simulink if the existence of one of the signals to be ANDed depends on the other one. For more detail, please refer to the Matlab-Simulink Manual.

This model is converted to a subsystem named 'Control' (Fig. B.2). The inputs to this

subsystem are the reference voltage, vs-ref(input1), the capacitor voltages, v_{C1} ($=v_{C3}$) (input2) and v_{C2} ($=v_{C4}$) (input3), load current, i_s (input4), the output voltage, v_s (input6), and the resonant current, i_r (input5). The outputs, on the other hand, are the control signals gate-1 (output1), gate2 (output2), and gate-SA (output3).

B.2 Simulink Implementation of HFAC-AC Matrix Converter

B.2.1 Power Circuit

Implementation should start with the switch implementation as before. For this reason, switches S_1 and S_2 are modeled as ideal Simulink switches (Fig. B.4). The switch inputs 1 and 3 are implemented according to the equations in Chapter 4 for Modes 1, 3 and 4, i.e. when they are off, the current through them is zero and when they are on the current through them is zero. The 'Switch1' block on the other hand implements eqn. (4.46) of Mode2. 'Mux' blocks are multiplexer blocks and they make pairs from their inputs. The 'Demux' block does the reverse, separating the pairs into single variables. In this model, the voltage and current values of the switches are paired and are given as inputs to S_1 and S_2. These switches are controlled by the gate driving signals. On the other hand, output voltage is obtained by the switch 'vao', which gives a negative half bus voltage when S2 is on and a positive half bus voltage when it is off. S1 on and off effects are considered by this switch through the bus voltage value. Both off condition is implemented by

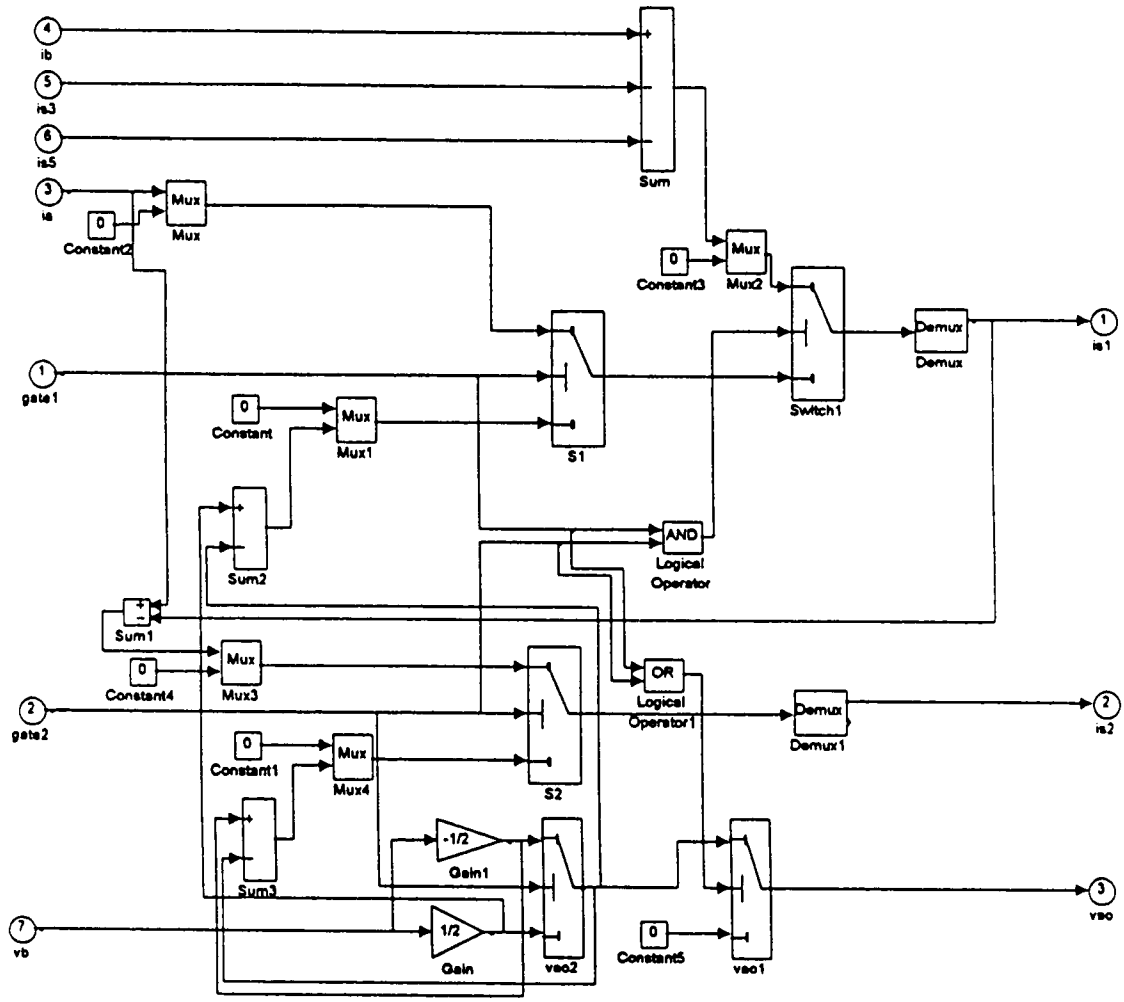


Fig. B.4: SIMULINK Block Diagram of the HFAC-AC Matrix Converter Phase Leg A

switch 'vao1' which gives an output of zero when S1 and S2 are off simultaneously. The control inputs are the firing signals gate1 (input1) and gate2 (input 2). The other inputs are the switch currents, is3 (input5), is5 (input6), the phase current, ia (input3), the bus current, ib (input4), and the bus voltage, vb (input7). The outputs, on the other hand, are the switch currents, is1 (output1), is2 (output2) and the phase voltage with respect to 'o' point, vao (output3).

Then comes the implementation of the ac link model, which is shown in Fig. B.5. The main equation to be solved for this implementation is eqn (4.42), which is a second degree, linear, ordinary differential equation. This is solved using the integrators of the Simulink. From this equation, the snubber capacitor voltage is obtained. Then using this and eqn. (4.38'), the bus voltage, v_b is calculated. 'Switch' block, which is controlled by the overlap signal controls the bus voltage. If there is an overlap, the resulting bus voltage is zero. For no overlap conditions the v_b is directly passed to the output. The bus current is calculated using the summer 'Sum 4' and it is also calculated using eqns. (4.37) and (4.40'). These two current values track each other but double calculation helps to see the interaction of the ac link with the phase leg blocks. The i_b, obtained by adding the switch currents, is used in the ac link modeling equations and then the value calculated using the other equations is fed to the phase legs. The control inputs to this block are the firing signals of all the switches, gate1 (input2), gate2 (input8), gate3 (input3), gate4 (input9), gate5 (input9), and gate6 (input10). Other then these, the additional inputs are the switch currents is1 (input5), is3 (input6), and is5 (input7), and the ac link voltage, vs (input1).

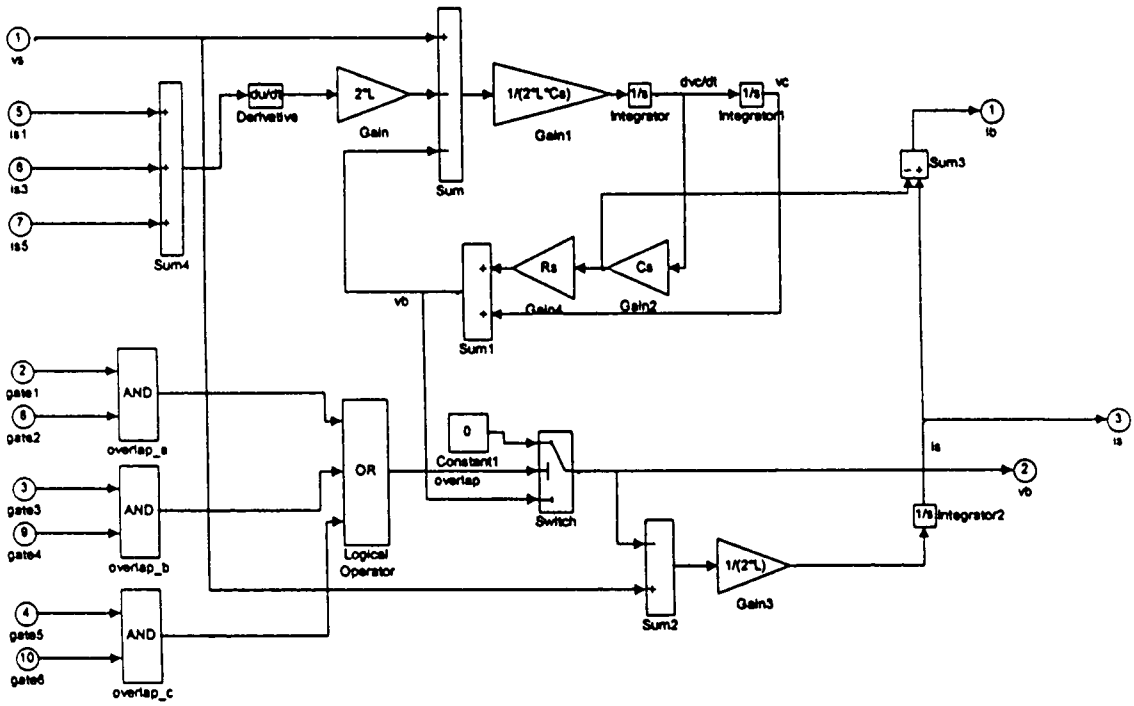


Fig. B.5: SIMULINK Block Diagram of the AC Link

The outputs are the bus current, ib (output1), the bus voltage (output2), and the ac link current, is (output3).

B.2.2 Control Circuit

The simulink implementation (Fig. B.6) starts with the phase control. For this reason the modulating wave should be compared to the carrier wave. First, the modulating wave and its inverse are given to the inputs of a switch. This switch is controlled by the current polarity signal. For negative currents, the polarity of the modulating wave is changed. The output of the switch is subtracted from the carrier wave and the result is passed through a zero crossing detector, which gives the crossing points of the two waveforms. The modulating wave crosses the reference wave at two points in one full period of the reference wave. The first one is unwanted, because it occurs during the ac link voltage transition. This is avoided by ORing the switch output with a signal, which deletes the crossing point during voltage transition. The resulting firing signal sequence is fed to the clock of a J-K flip flop. This flip flop toggles the output because both of its inputs are '1'. The output of this flip-flop is a waveform, which toggles between one and zero at each firing instant. This output can be used as the firing signal to the switches. On the other hand, the switch to be turned on or turned off, on the other hand is determined by the 'switch selector' using Table 2.1. The outputs of this block are the firing signals of the switches on phase a. The firing signal is ORed with the signals, which monitor the switch currents. With this ORing, the switches are turned off if the current through them is zero.

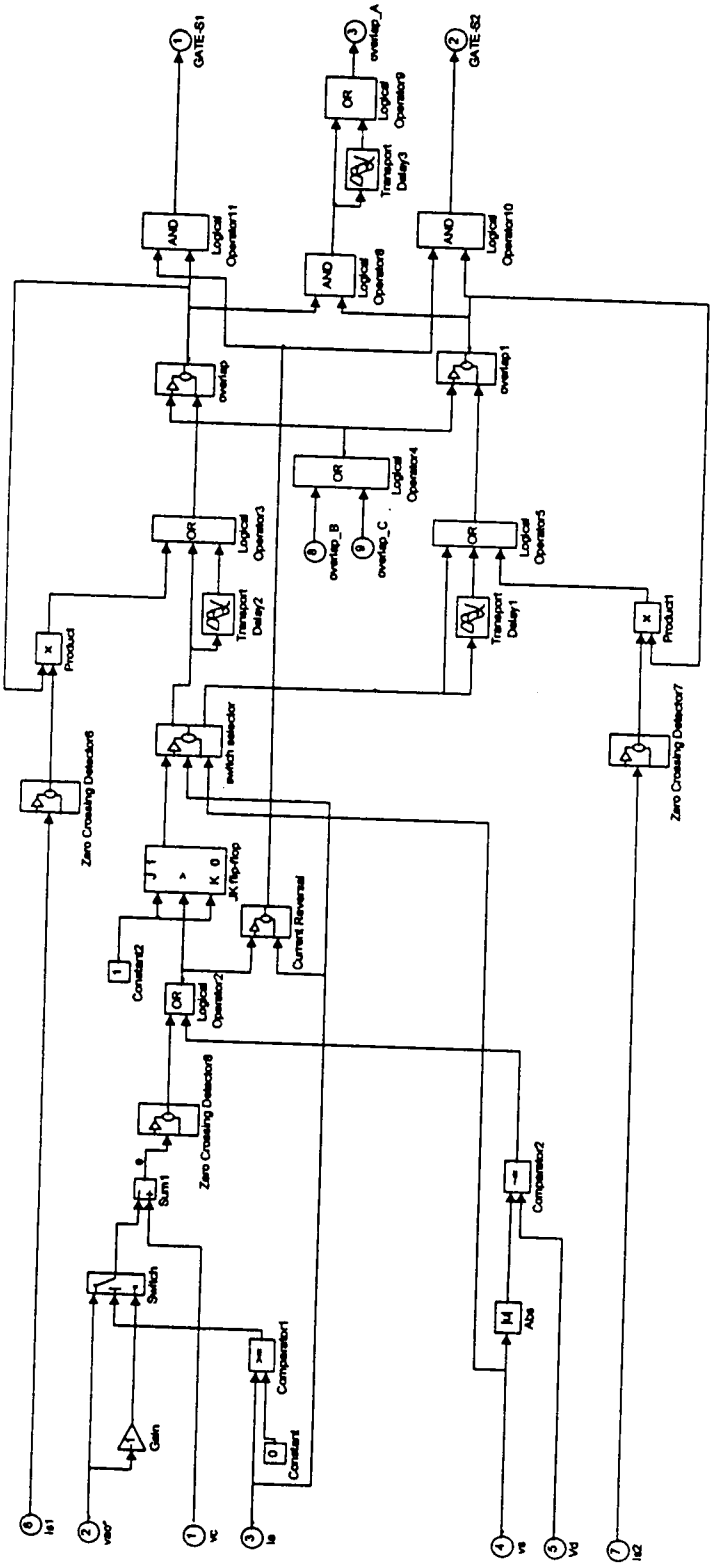


Fig. B.6: SIMULINK Block Diagram of the HFAC-AC Matrix Converter Control

The firing pulse formation continues with the overlap block, which checks if there is an overlap in one of the other phases. If there is, then the firing signals are postponed until the other overlap ends. The last stage before the firing signals are given to the switches is the effect of the current reversal. The 'current reversal control' block checks to determine if there is a current reversal. If so, it blocks the firing signals to the switches until the next firing pulse. Therefore this signal is ANDed with the output of the 'overlap' block. The output of the AND blocks is the final firing signal applied to the individual switches of a phase leg.

The inputs to this block are the carrier wave, vc (input1), the modulating wave, vao* (input2), the phase current ia (input3), the phase voltage vao (input4), the battery voltage Vd (input5), and the switch currents, is1 (input6) and is2 (input7). The outputs are the control signals GATE-S1 (output1), GATE-S2 (output2), and there is overlap in phase a signal, overlap_A (output3).

All of the blocks explained above are connected as shown in Fig. B.7.

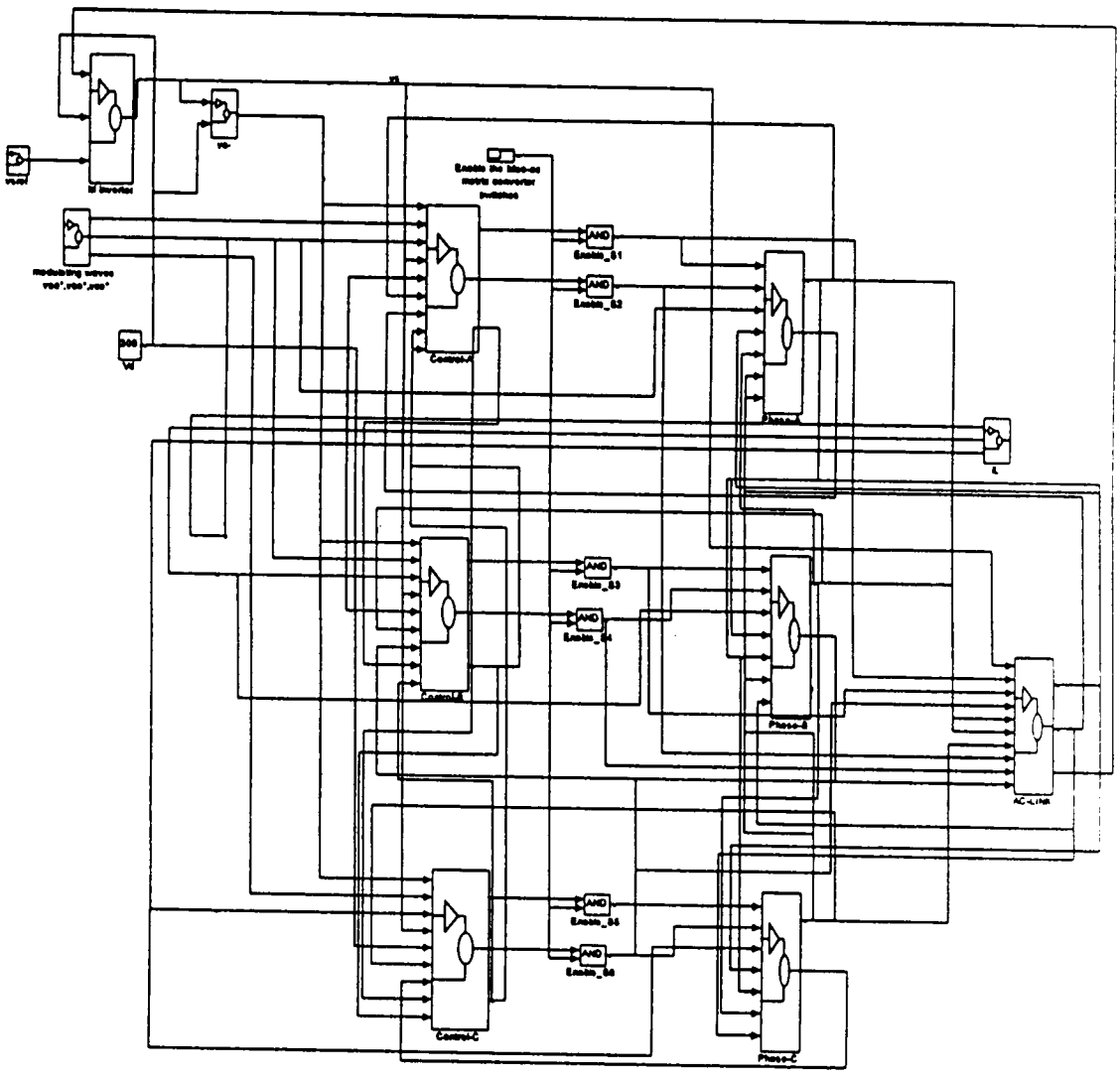
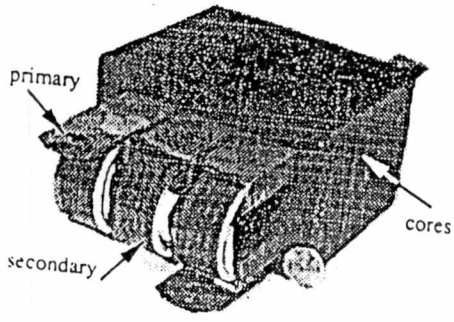


Fig. B.7: SIMULINK Block Diagram of the Overall DC-HFAC-AC Converter System

APPENDIX C

HIGH FREQUENCY TRANSFORMER

People who are used to 60Hz transformers, at first sight of this converter, might think that the ac link transformer would increase the size and weight of the system. However, this transformer is a high frequency transformer and high frequency transformers shrink in size and weight as the operating frequency increases until a certain frequency after which for thermal considerations their size and weight starts increasing again. Especially with the new transformer winding techniques high frequency transformer size is not a problem. Experimental values for a typical high frequency coaxial winding transformer is given in Fig. C.1. The transformer is tested [13] at a power rating of 40kVA and operating frequency is 50kHz, i.e. a typical transformer for this converter. Note that the leakage inductance is as small as 0.15μH, which means smaller notches in the output voltage wave. The weight of this transformer is just 3.83kg. The volume is not given as a figure but is stated as small which is expected. This implies that there is no weight or size problem. Note that if instead of Ferrite material, materials with higher flux density such as Amorphous metal or Permalloy cores are used the size and weight can be further decreased.



- 46 KVA, 50 kHz, Square Wave
- Core Material : Ferrite PC40
- Primary Voltage: 200 V
- Primary Turns: 3
- Secondary Turns: 7
- Magnetizing Inductance (Primary): 250 μH
- Leakage Inductance (Primary): 0.15 μH
- Open Circuit Core Loss: 70 W
- Short Circuit Copper Loss (230 A): 180 W
- Power Density: 0.083kg/kW
- Transformer Weight: 3.83 kg
- Efficiency: 99.4%

* "Design Considerations for High Power High Frequency Transformers", M.H.Kheraluwala et. al., IEEE IAS Meeting, pp. 734 -742, 1990.

Fig. C.1: High Frequency Coaxial Winding Transformer
(with ultra low leakage inductance)

VITA

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