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DESIGN AND ANALYSIS OF A WIDE LOOP-BANDWIDTH RF SYNTHESIZER USING RING OSCILLATOR FOR DECT RECEIVER

A Thesis Submitted
for
the Master of Science Degree.
The University of Tennessee, Knoxville.

Md. Hafijur Rahman
May 2003

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude and appreciation to my supervisor, Dr. Syed K Islam for his individual guidance throughout the course of this research work. His advice and assistance in the preparation of this thesis are thankfully acknowledged. Special thanks to Dr. Benjamin J. Blalock for allocating his time for me and without his kind help it might have been very difficult for me to finish my thesis. I would also like to thank Dr. Donald W. Bouldin for his valuable teaching on the essentials of IC design and I am really grateful to him for serving on my committee. I would like to thank all of my friends specially Md. Hasanuzzaman, Venkatesh Srinivasan, Lakshmipriya Seshan, Akila Gothandaramanand and Md. Nazmul Islam for helping me in every instant of my thesis work. I also wish to thank my fellow graduate students and all the faculty and staff in our department for making my graduate study such a rewarding experience.

I wish to thank my parents, brother and sisters for their support. My father deserves special thanks for his continuous support throughout my whole life. And finally, I want to thank my wife, Sumona, for her mental support to finish my thesis.

ABSTRACT

Wireless communication devices including cordless phones and modern digital cellular systems (DCSs) use portable transceiver systems. The frequency synthesis of this type of transceiver system is done using a phase-locked loop oscillator. Traditional on-chip implementation of a complete phase-locked loop using a ring type voltage controlled oscillator contributes higher noise at the output. An alternative architecture, phase-locked loop (PLL) with wide loop-bandwidth, is proposed in this research to suppress the noise from the traditional ring oscillator. The proposed PLL is amendable to on-chip integration as well as commercially suitable for a Digital Enhancement Cordless Telephone (DECT) system which needs flexible noise margin.

In this research, a 1.5552 GHz PLL-based frequency synthesizer is designed with a noisy ring oscillator. The wide loop-bandwidth approach is applied in designing the PLL to suppress the VCO noise. In this type of frequency synthesizer, the frequency divider is operated at higher frequencies with less noise and care is taken to design the delay flip-flops and logic gates that can be operated at higher frequencies. Current-mode control can be employed in designing the logic gates and the delay flip-flop to enhance the speed performance of the divider. An alternate approach in designing a high-speed divider using a current-mode control approach is also presented.

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Chapter 1

Introduction

1.1 Motivation

CMOS is the mainstream process for designing complex monolithic systems for low cost with dense logic, low power dissipation, low supply voltage, and highly automated synthesis. The rise of modern RF telecommunication systems has caused an increase in the demand for cheap monolithic ICs. An important component of a RF front-end is a high frequency phase-locked loop (PLL) used for frequency translation of the RF input signal. Wireless communication devices such as cordless phone, modern digital cellular system (DCS) and global positioning system (GPS) use a portable transceiver system. The frequency synthesis of this transceiver system is done using a phase-locked loop oscillator. The RF high frequency signal is translated down to the base band signal using a frequency synthesizer and the carriers for the different channels are tuned using a frequency synthesizer. A PLL-based frequency synthesizer is one of the major building blocks for an integrated transceiver. Most of the wireless base-band signal processing circuits use a CMOS process because of lower cost and higher integration capability. Research efforts are being made to integrate most RF functions in CMOS with the goal of realizing single-chip RF-to-base band systems [1].

Digital Enhancement Cordless Telephone (DECT) and Digital Cellular System such as DCS 1800 (3^{rd} Generation GSM system) use the RF carrier frequencies of *1.7 – 2.0* GHz band. Until recently, both DECT and DCS systems used conventional heterodyne structure in their transceivers. In heterodyne type receivers, the RF incoming signal is translated in two stages to get the base band signal. The RF signal is first tuned and shifted to an intermediate frequency (IF) signal using a programmable RF synthesizer and then the converted IF signal is translated to the base band signal using a fixed frequency IF synthesizer. The synthesizers use off-chip voltage controlled oscillator (VCO) components to minimize the VCO noise. The need for off-chip components is not amendable to integration of the synthesizers. An alternative architecture, a wideband IF double-conversion receiver architecture [4] has been proposed to facilitate the utilization of the wideband synthesizer. This approach is similar to a super heterodyne receiver architecture in which the frequency translation is accomplished in two steps. However, unlike a conventional super heterodyne receiver, all the RF channels are converted to IF using fixed RF synthesizer and then the IF signals are tuned and translated to the desired channels by programmable IF synthesizers. Both the synthesizers have been proposed for on-chip implementation, but on-chip VCOs are very noisy. It is essential that both synthesizers, especially RF synthesizers, offer less noise at their output. The RF synthesizer noise is transmitted through the IF stage towards the output of the receiver. The wide loop-bandwidth may be used for the synthesizers to suppress the VCO noise significantly. The wide loop-bandwidth approach for RF synthesizers is suitable for on-chip VCO implementation such as ring VCO and LC VCO with on-chip inductor.

In the case of a DECT receiver, the system should be realized for longer battery life and less noisy output. Considering these requirements, RF synthesizer must have the following two properties: i) low noise and ii) low power dissipation. In addition, the whole synthesizer must be realized for on-chip integration with less die area and lower cost. LC oscillators with on-chip inductors take enormous effort and die area to be implemented, which in turn may not be an economical solution to replace an off-chip inductor. LC oscillators also dissipate enormous power to attain desired output swing. On the other hand, ring oscillators overcome all these disadvantages. But ring oscillators are noisier than their on-chip LC counterparts. Using wide loop-bandwidth, this problem can be solved significantly. This method has some other adverse effects on the system. For this approach good knowledge about loop dynamic is essential to determine the optimum loop-bandwidth.

Until recently, limited research has been done to implement wide loop-bandwidth RF synthesizers using on-chip LC oscillators. In this thesis work, a RF synthesizer is designed using a ring oscillator for on-chip implementation of the complete frequency synthesizer. The phase noise from the ring oscillator is suppressed by the high-pass action using the wide loop-bandwidth. Analysis for the expected noise performance of the complete synthesize is done in two steps. In the first step, the phase noise of the ring oscillator is analyzed. The theoretical model of the phase noise is verified by the simulated noise performance. Two ring oscillator structures are analyzed to find the architecture for better noise performance. In the second step, the relation between the

loop-bandwidth and different circuit parameters is established. The effect of the length of the loop-bandwidth on VCO phase noise suppression at the output is analyzed.

In the frequency synthesizer, only two components i.e. VCO and frequency divider are operated at high frequencies. It is very difficult to operate the conventional digital frequency divider at higher frequencies *(>1 GHz*). Care must be taken to design delay flip-flops and logic gates that can be operated at those high frequencies. Current-mode control can be employed in designing the logic gates and the delay flip-flop to enhance the speed performance of the divider. Good knowledge of the factors and key issues are necessary to improve the speed performance. This type of analog divider definitely has good speed performance but it has greater power dissipation.

In summary, this thesis presents the design of a *1.5552 GHz* RF synthesizer for DECT receiver. The wide loop-bandwidth is employed to suppress the noise of an on-chip noisy ring VCO at low offset frequency. Analysis is done to show the effects due to the VCO noise on the output for the different bandwidths. This thesis also presents an approach to the design of a high-speed divider using a current-mode control approach. The key issues determining speed performance of the divider are also discussed.

1.1 Thesis Organization

In chapter two, the fundamentals of a frequency synthesizer are discussed. Frequency synthesizers are essential in DECT receivers. The roles of frequency synthesizers in a

super-heterodyne receiver architecture and a wideband IF double-conversion receiver architecture are explained in detail. The relationship between the various noise sources and the loop-bandwidth is established. The necessity of wide loop-bandwidth in a frequency synthesizer to suppress the noise from an on-chip noisy ring oscillator is discussed.

Chapter three presents the technique of current-mode control in designing differential dividers for high-speed operation. Two dividers with fixed dividing ratios and a programmable divider are analyzed to show the improvement over conventional digital dividers in speed and noise performance by using current-mode control and differential structure. The key features that influence the speed performance are explained. Best performances can be obtained by optimizing parasitics. Dividers and logic gates have been designed in a modular fashion so that any dividing ratio can be obtained.

Chapter four begins with a description of the ring type voltage controlled oscillators (VCOs) and its characteristics. A noise analysis of the delay cell is carried out based on the framework established by Weigandt [16]. The technique of improving noise performance in a ring VCO is presented and then three ring VCO structures are compared to get best noise performance. Comparison of simulated noise performance for these ring oscillators is also presented.

In chapter five, the operation of a phase frequency detector with a charge pump and a loop filter is discussed. The design technique of a simple current steering charge pump

and a loop filter is explained, and then loop dynamics of the phase-locked loop (PLL) are also discussed. The influence of loop-bandwidth on the overall noise performance of frequency synthesizers is explained and verified in this chapter.

Chapter six discusses key design issues and provides suggestions for future work.

Chapter 2

Fundamentals of Phase-Locked Loop Frequency Synthesizer

2.1 Introduction

Frequency synthesis is the generation of a frequency or frequencies, which are exact multiples of a reference frequency. Usually the reference frequency is very precise and the synthesized frequencies are selectable over some range of multiple of the reference frequency; that is, the output frequency is given by,

$$f_{out} = Nf_{ref} \qquad \text{....(Eq. 2.1)}$$

The role of a frequency synthesizer in DECT system is to provide reference frequency for the frequency translation.

2.2 DECT Receivers

DECT uses the frequency band between *1.88 GHz* and *1.90 GHz*, in which there are 10 frequency channels with a spacing of *1.728 MHz*. Most RF communication transceivers manufactured today utilize a conventional super-heterodyne approach. A typical RF receiver section of a DECT system is shown in Figure 2.1. The received RF signal spectrum is mixed down to the base-band in two steps. In the first step, a high frequency synthesizer signal is mixed with the incoming RF signal, shifting the information signal to a fixed IF frequency. To do this, a RF synthesizer (local oscillator, LO_1) needs to be tunable and the minimum frequency step must be smaller than or equal to the channel

spacing of the standard. Then a fixed frequency synthesizer at IF is mixed with the mixed-down version of the received signal and finally shifts it to the base-band. This type of receiver uses a narrow loop-bandwidth RF synthesizer (local oscillator, LO_1 in Figure 2.1) where the phase noise from the reference input of the crystal oscillator dominates over the VCO phase noise. This RF synthesizer uses off-chip VCO components with high Q that can offer low phase noise.

An alternate architecture with a wideband IF double-conversion receiver architecture [4] has been proposed to facilitate the utilization of wideband synthesizers. In this architecture, the entire signal band at RF is mixed down to the IF signal with a fixed RF frequency synthesizer. A variable frequency synthesizer at IF is used to tune the desired channel from IF to the base band. Because the RF LO is a fixed frequency, a high-frequency reference is allowed and hence a wide synthesizer control bandwidth is obtained. This approach is amenable to integration of a synthesizer because relatively poor VCO phase noise can be tolerated.

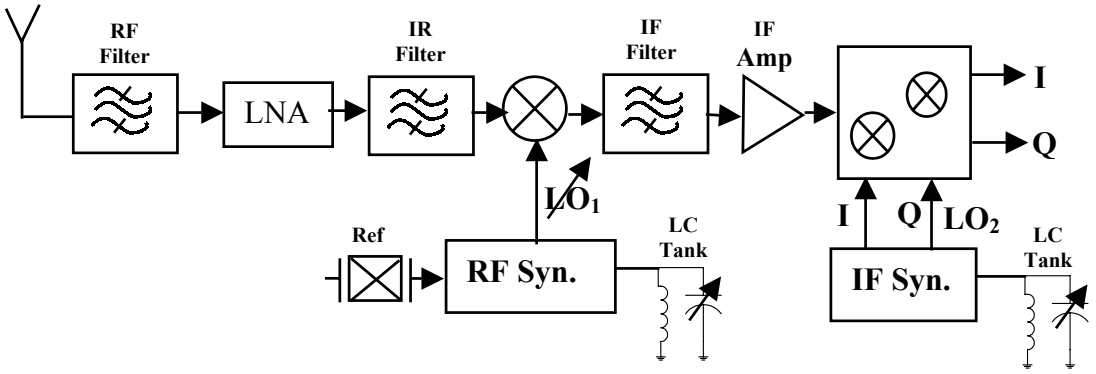


Figure 2.1 A conventional super-heterodyne receiver architecture [4]

2.3 Phase-Locked Loop

A phase-locked loop is a loop, which locks the output phase or frequency in accordance with an accurate reference frequency. The block diagram of a typical phase-locked loop (PLL) is shown Figure 2.2. In a PLL, a voltage-controlled oscillator (VCO) is used to generate an output at a frequency set by the control voltage, $V_{ctr.}$ The Phase/Frequency Detector (PFD) compares the phase/frequency of a reference frequency $f_{ref\text{-}clk}$ with the divided output phase/frequency $f_{clk\text{-}in}$ and generates the pulse with the width, which is proportional to the phase difference between these two signals. Charge pump converts the width of the pulses from the PFD to an equivalent voltage level. The loop filter rejects the high frequency from the output of the charge pump and generates control voltage (V_{ctr}) for the VCO. When the loop is locked, the PFD sees two identical waveforms at its inputs and f_{out} equals to $Nf_{ref\text{-}clk}$. As shown in the waveform, if for some reason $f_{ref\text{-}clk} > f_{clk\text{-}in}$, VCO control voltage V_{ctr} goes down and the VCO output frequency increases. Vice versa, if $f_{ref\text{-}clk} < f_{clk\text{-}in}$, V_{ctr} goes up and the VCO output frequency decreases. A loop filter (LPF) is also used to stabilize the loop by introducing zeros and poles into the loop.

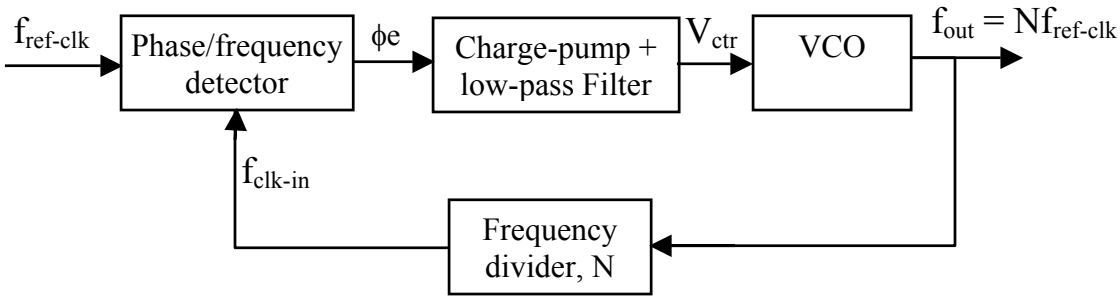


Figure 2.2 Phase-locked loop block diagram

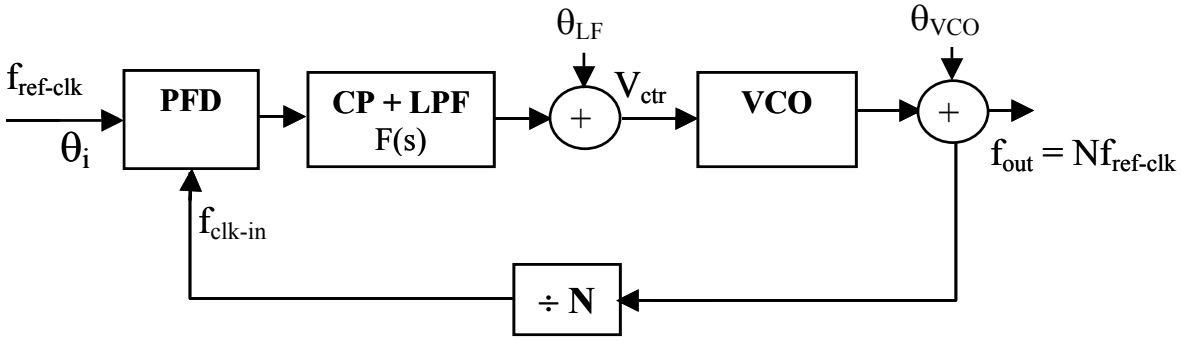


Figure 2.3 Phase-locked loop linear model

There are many different ways to analyze the behavior of a PLL. Generally, a linearized model can be used to get more insight into the PLL design. Figure 2.3 shows the linear model of a typical PLL [2, 3].

In the linear PLL model, the PFD has a gain of K_ϕ, the loop filter has a transfer function F(s), and the VCO has a gain of K_{vco} (Hz/V). Because phase is the integrated value of the frequency, an integrator 1/s is included into the VCO block so that the VCO block has a gain of K_{vco} /s. The open loop gain G(s) can be written as,

$$G(s) = \frac{K_\phi F(s) K_{VCO}}{Ns} \qquad \text{….(Eq. 2.2)}$$

If we consider a simple loop filter which has only one pole and one zero in the transfer function, then,

$$F(s) = \frac{1 + s/Z}{1 + s/P} \qquad \text{….(Eq. 2.3)}$$

The overall open-loop transfer function is,

$$G(s) = \frac{K_\phi K_{VCO}}{Ns} \frac{1 + s/Z}{1 + s/P} \quad \text{....(Eq. 2.4)}$$

This represents a second-order PLL. The PLL bandwidth f_{PLL} is defined as the frequency for which the open loop gain drops to unity i.e.,

$$\left| G\left(j2\pi f_{PLL} \right) \right| = 1 \quad \text{....(Eq 2.5)}$$

The sum of the phase noise from the reference, the phase detector and the frequency divider is represented by θ_i. The noise transfer function from θ_i to output θ_o is,

$$\frac{\theta_o}{\theta_i}(s) = N \frac{G(s)}{1 + G(s)} \quad \text{....(Eq. 2.6)}$$

Notice that the transfer function is a low-pass transfer function with a gain of N at frequencies below the loop-bandwidth. This means that the noise contributions from the reference, the phase detector, and the divider referred to the output are enhanced in effect by N at low offset frequencies from the carrier, and are suppressed at high offset frequencies from the carrier. Intuitively, for the low-frequency part of the noise, it can be seen that the loop is fast enough to modulate the VCO so that the output follows the input. The enhancement factor N comes from the fact that the PFD only compares one out of every N cycles of the VCO output. But for the high-frequency part of the noise, the loop is not fast enough to follow and suppress the noise from the input.

The noise from the charge pump and the loop filter is represented by θ_{LF}. The transfer function from loop filter output to the synthesizer output is,

$$\frac{\theta_o}{\theta_{LF}}(s) = \frac{K_{VCO}}{s} \frac{1}{1 + G(s)} \quad \text{....(Eq. 2.7)}$$

The response from the loop filter to the output depends on the VCO gain and the open loop gain. For example, the 2nd-order PLL has a loop filter with one zero and two poles, which gives the above transfer function a band-pass characteristics. Notice the noise is multiplied by the VCO gain at the output. Intuitively, for the low frequency part of the noise, it can be seen that the loop is fast enough to follow the reference rather than letting the output be affected by the loop filter noise. But for the high frequency part of the noise, the loop is not fast enough to correct the noise.

The noise from the VCO is represented by θ_{VCO}. The transfer function from the VCO output to the synthesizer output is,

$$\frac{\theta_o}{\theta_{VCO}}(s) = \frac{1}{1+G(s)} \qquad \text{....(Eq. 2.8)}$$

This has a high-pass characteristic. Intuitively, the lower-frequency part of the noise from the VCO can be corrected by the relatively fast PLL. But for the higher-frequency part of the noise from VCO, the loop is not fast enough and is essentially an open loop.

2.4 Narrow vs Wide Loop-Bandwidth in PLL

Two major noise sources in a phase-locked loop are the followings:

1) Phase noise from the input
2) Phase noise from the voltage controlled oscillator (VCO)

From the Eq 2.6 and Eq 2.8, it can be realized that for narrow loop-bandwidth the noise from the input can be suppressed significantly. In that case, the VCO noise dominates at the PLL output. On the other hand, for wide loop-bandwidth noise from the VCO is

suppressed and the noise from the input dominate at the output. Figure 2.4 shows the plot of the three transfer functions for three noise sources and the VCO noise with typical Gaussian Shape. It is clear from the plot that the noise from the input, the loop filter, and the VCO go through low-pass, band-pass, and high-pass filtering separately. It is evident from this figure that for wider loop-bandwidth the VCO noise goes to the PLL output with suppression from lower to much higher offset frequencies. This means that the VCO noise goes to the output with much suppression.

In most of the RF applications, low loop-bandwidth is desired in order to minimize the spectral components due to spurious tones in the output spectrum, which result from a noisy input reference. One consequence of the low synthesizer control bandwidth is that the phase noise of the overall synthesizer is dominated by the phase noise of the VCO. This makes the narrow loop-bandwidth approach suitable for the implementation with a discrete high Q component that is needed by the low-phase-noise LC VCO. The need for external components is not amenable to integration of the synthesizer.

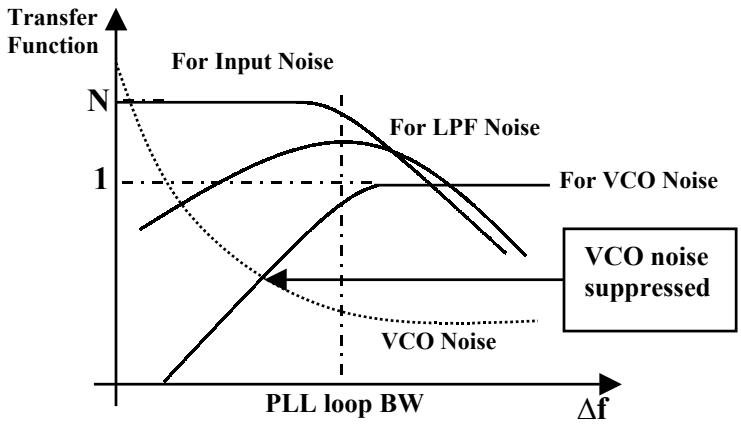


Figure 2.4 VCO phase-noise suppression in wide-loop-bandwidth PLL

A major challenge is to find ways to realize low-phase-noise synthesizers with a noisy ring Oscillator or an on-chip LC oscillator with a low Q component. The wide loop-bandwidth is necessary if fast frequency switching is needed in frequency synthesizers using programmable dividers or programmable fractional–N dividers. A PLL-based synthesizer has a frequency resolution of $f_{ref.}$ When very fine frequency resolution is needed, the loop-bandwidth is even lower in order to maintain the stability of the loop [5]. Usually loop-bandwidth f_{PLL} should be 10 times less than the reference frequency f_{ref}. This makes the PLL-based synthesizer not suitable in an agile system where fast switching is needed. However, a narrow band PLL-based frequency synthesizer is most commonly used in applications where extremely high performance (very low phase noise) is required.

In the fully integrated on-chip PLL, two types of VCO are used: a LC oscillator with an on-chip inductor or a ring VCO. In case of a LC oscillator with an on-chip inductor, it is difficult to set exact circuit model and it requires enormous die area. A LC oscillator dissipates significant amount of power to attain the desired output voltage swing at the output. Moreover, its contributed Q-factor is not so good enough with the added power and the die area. On the other hand, a ring VCO is easy to implement on-chip, dissipates less power and requires less die area. A Ring VCO has very poor noise performance. With a wideband PLL architecture, it is possible to obtain a good spectral purity with a noisy ring VCO. In this case, wide bandwidth is required to suppress the VCO noise. Using a wide loop-bandwidth has couple of adverse effects on the system:

1) It will significantly increase the effect of the input noise to the output
2) Phase margin of the system will be lower. This will cause the system ringing.

In a wide bandwidth PLL, a good crystal oscillator with excellent spectral purity is used as the reference. From the Eq 2.6, it is evident that the input noise is multiplied N times at the output. Another way to lower the effect of the input noise is to use a lower dividing ratio. This causes another problem. If integer division is assumed, the reference frequency must be larger than the loop-bandwidth. This means that the frequency step of a wideband PLL has to be large. In DECT application, the required frequency step is usually very small. For example, it has channel spacing of *1.728 MHz*. The wideband PLL-based frequency synthesizer cannot produce frequencies with a step of *1.728 MHz* because the loop-bandwidth may be in the MHz range and the reference frequency may be in tens of MHz range. To solve this problem, a Wideband IF Double-Conversion Receiver Architecture [4] has been proposed. In this architecture, the entire signal band at RF is mixed down to the IF with a fixed RF frequency synthesizer, and a variable frequency synthesizer at IF is used to tune the desired channel from IF to the base band. The IF synthesizer can tune the channels and still achieve low phase noise, because it is enervating outputs at lower frequencies.

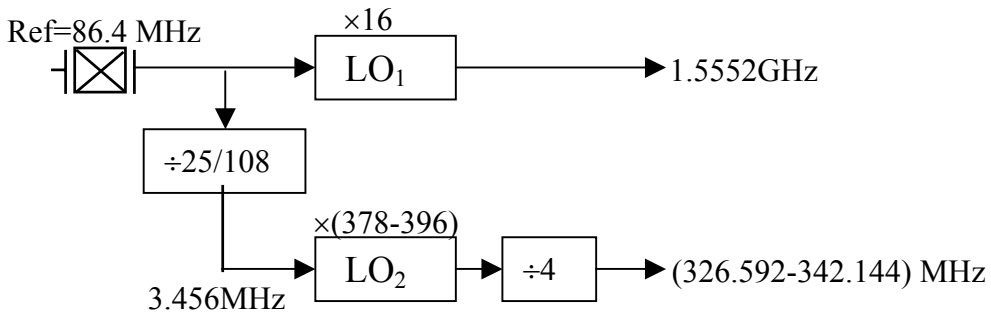


Figure 2.5 The proposed frequency plan [5] implemented by the PLL for DECT receiver

For DECT system, the proposed frequency plan [5] implemented by the PLL is shown in Figure 2.5. The RF synthesizer has been proposed with a fixed reference frequency of *1.5552 GHz* and the tunable IF synthesizer can tune the channel from the IF frequency band from *326.592MHz-342.144 MHz***.** Phase-noise requirement of a RF synthesizer for DECT receiver is ≤ - 90dBc/Hz.

Chapter 3

Fully Differential, High-Speed Current-Mode Controlled Dividers Designed Using Modular Approach

3.1 Introduction

Currently, most of the communication schemes employ giga Hz range frequencies. The VCO in the phase-locked loop for a frequency synthesis application generates high frequency signal. The higher frequencies should be stepped down to lower frequencies by a frequency divider to compare with the reference input frequency. This is a challenge in designing a frequency divider that can be operated at higher frequencies generated by the VCO. Until recently, a number of novel approaches have been introduced in designing latches and logic gates to speed up the frequency dividers for higher operating frequencies. One of these approaches utilizes design of the latches and the logic gates with current-mode control. The dividers with current-mode control and differential structure are preferred over their conventional counterparts for low noise and high-speed applications. In case of the digital dividers, internal propagation delay of the latch and logic gates limits their speed performance. The current-mode switching minimizes the propagation delays for latches and logic gates. It can operate with higher operating frequencies [9,10] and give better control over the circuit. This high-speed divider is best suited for PLLs in frequency synthesis applications. This type of analog divider uses current-mode switching to control current, parasitic, and other factors that minimizes

propagation delay. The input and the output of a divider are connected with voltage controlled oscillators (VCOs) and phase-frequency detectors (PFDs). A series of delay flip-flops (DFFs) are pipelined to form the divider architecture. The input/output voltage levels of the divider should be matched with the input/output voltage levels of the VCOs, the PFDs or the neighboring flip-flops. Current-mode control gives more flexibility to attain any desired output level to match the input or the output voltage of the next or the previous stage. Limiting the output voltage swing is another method to reduce propagation delay [11]. A current-mode switching circuitry offers better speed performance than its conventional digital counterpart.

Latches using MOS current-mode logic [9,11] generate less switching noise. Also, a current-mode logic combining with differential configuration has better electromagnetic compatibility (EMC) properties because of constant supply current and differential voltage switching operation [6]. Conventionally, differential structures are used for low noise circuitry because of their ability to reject the common mode noise. This structure is capable of producing inverting logic along with non-inverting logic. Their dependency on both inverting and non-inverting inputs and clock signals (as shown in Figure 3.3) provides more robust design without the need for an extra inverter stage. The main drawback of using a current-mode control and a differential configuration is greater power consumption due to the constant dc biasing current. Besides, this requires longer design time and larger cell area compared to an equivalent digital cell.

3.2 Frequency Divider

The building blocks of dividers are edge-triggered delay flip-flops (DFFs) and logic gates. If the outputs of an edge-triggered DFF are connected with the inputs in such a way that it provides a negative feedback loop, this circuit will provide a divider with fixed dividing ratio of 2 as shown in Figure 3.1(a). Figure 3.1(b) shows the divider with dividing ratio of 3 [2]. Similarly, divider with any dividing ratio can be designed using DFF and logic-gates.

Figure 3.2 shows the block diagram of a programmable frequency divider. The architecture for the logic gates, the delay flip-flops and the dividers are implemented in modular way, so that any dividing ratios can be derived. The output frequency equals the input clock frequency/ (2N+2+K) where N= number of DFF present in between dff1 and dff(N+2) and K=mode control {0,1,2,3}. From the block diagram we have found that if 'K'= '00', the outputs of dff(N+1) are connected with the inputs of dff1 through mux1 and mux2. These connections are made such a way that it provides a negative feedback path. So dff1, dff2, -------, dff(N+1) are connected in series in the negative feedback loop.

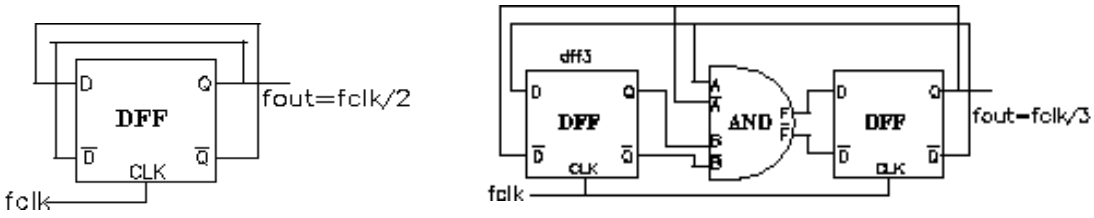


Figure 3.1 Dividers with fixed dividing ratio of (a) 2 (b) 3

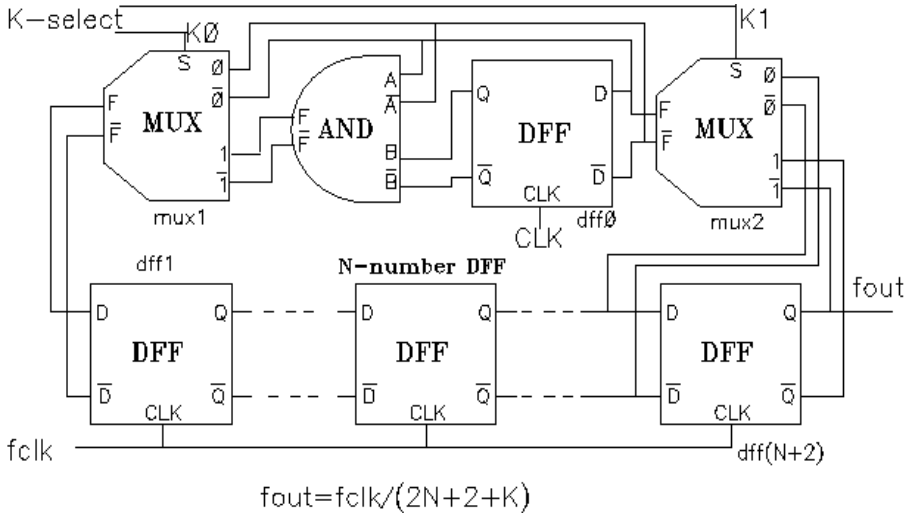


Figure 3.2 Programmable frequency divider

Each DFF in this loop contributes a dividing ratio of 2 and (N+1) numbers of DFF in the loop provide a dividing ratio of (2N+2). Again if 'K'= '10', dff(N+2) is included in the loop and the total dividing ratio is (2N+ 4). For 'K'= '01', dff0 and 'AND' gates are included in the feedback loop through mux1 and mux2. dff0 and dff1 with mux1 provide a dividing ratio of 3 and the total dividing ratio is (2N+ 3). For 'K'= '11', the total dividing ratio is (2N+ 5).

3.3 Delay Flip-Flop (DFF)

The edge-triggered delay flip-flop (DFF) is the fundamental module of a frequency divider. Delay in each stage of the DFF affects the speed performance of a frequency divider. Careful design of a DFF can effectively increase the speed of the frequency divider. A level sensitive (LS) differential DFF is shown in Figure 3.3. This circuit

provides a perfect example of current-mode control. In a current-mode switching circuit, the output is set between two levels by switching between two current levels. In case of MOS, if its drain current is forced to switch between these two currents, its gate-to-source voltage as well as its drain to source voltage can be controlled. The output of a MOS transistor circuit can be defined by controlling these two voltages.

In the LS-DFF structure, the NMOS transistors M3 and M4 are used to sense the input, and M5 and M6 provide the loop for positive feedback. These transistors with positive feedback action ensure the same logic level up to the next triggering edge. The diode connected PMOS transistors M1 and M2 are used as active loads of the differential circuit. M7 and M9 are switching NMOS transistors operated by the clock and the inverting clock as shown in Figure 3.3.

M11 and M12 transistors provide the tail current for the transistors M1 and M2 when the switching transistors turn one of the paths ‘OFF’. This makes the DFF switched from one considerable current level to a higher current level. It can be shown that switching between zero current and a higher current may cause additional delay in the circuit, which affects speed performance of the circuit. On the other hand, in order not to get he critical path by the gate-channel capacitances of these PMOS devices, these devices should be kept near the same point in saturation almost for the entire voltage swing at the output [8]. Unless otherwise, it will generate noise at the output.

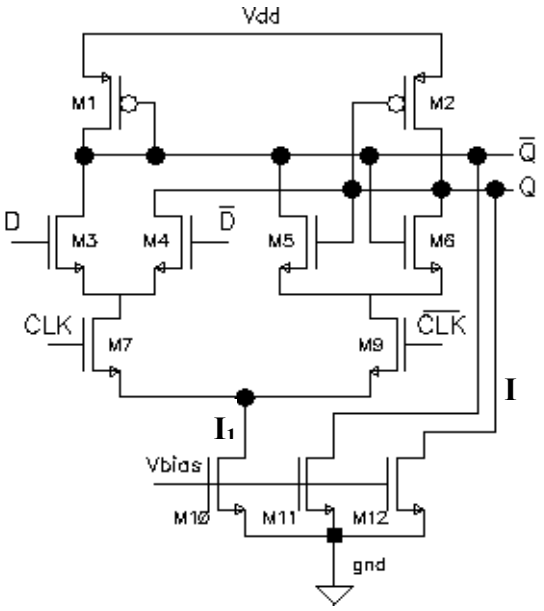


Figure 3.3 Level sensitive delay flip-flop

In order to improve the speed performance, the voltage swing at the output should be minimized as much as possible [11]. Let us that the tail current is I_1 in M10 and I_2 in M11/M12. If both the D and clock input are high, M1 will sustain a current that is the sum of the two tail currents (I_1+I_2). As M1 is in saturation, we get,

$$\left|V_{GS1}\right|^1 = \left|V_{TP}\right| + \sqrt{\frac{I_1 + I_2}{\mu_p C_{ox}\left(\frac{W}{2L}\right)}} \qquad \text{….(Eq. 3.1)}$$

So, $$\left[V_{\overline{Q}}\right]_{lower} = V_{dd} - \left|V_{GS1}\right|^1 = V_{dd} - \left|V_{TP}\right| - \sqrt{\frac{I_1 + I_2}{\mu_p C_{ox}\left(\frac{W}{2L}\right)}} \qquad \text{….(Eq. 3.2)}$$

If one of the D and clock input are low, M1 conducts only with a current, I_2. In this condition, we get,

$$\left|V_{GS1}\right|^2 = \left|V_{TP}\right| + \sqrt{\frac{I_2}{\mu_p C_{ox}\left(\frac{W}{2L}\right)}} \qquad \text{….(Eq. 3.3)}$$

So, $$\left[V_{\overline{Q}}\right]_{upper} = V_{dd} - \left|V_{GS1}\right|^2 = V_{dd} - \left|V_{TP}\right| - \sqrt{\frac{I_2}{\mu_p C_{ox}\left(\frac{W}{2L}\right)}} \quad \text{....(Eq. 3.4)}$$

So, the current in the PMOS loads swings between I_2 and (I_1+I_2) and as a consequence the output voltage of the oscillator swings from $\left[V_{\overline{Q}}\right]_{upper}$ to $\left[V_{\overline{Q}}\right]_{lower}$. From the Eq. 3.2 and Eq. 3.4, the output swing can be defined by the dimensions of the active PMOS loads (M1 and M2 PMOS transistors). Again, by altering the dimensions of M11 and M12 transistors, the upper limit of the output voltage can be controlled. The dimensions and the currents of the current mirror component M10 should be such that this transistor can be kept in saturation during entire swing. Otherwise, swing from the linear region to the saturation region during switching may cause the common mode voltage to vibrate, which in turn causes noise at the output.

In order to form a negative edge-triggered DFF, two level sensitive (LS) flip-flops are connected in series and the second LS flip-flop is triggered by the inverting clock to perform edge-triggering latch operation. Figure 3.4 shows the formation of a negative edge-triggered flip-flop.

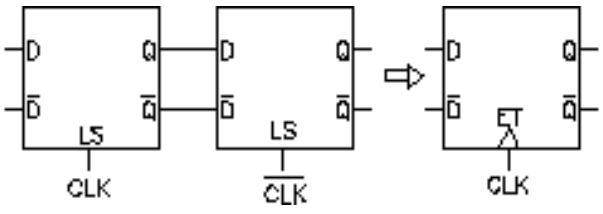


Figure 3.4 Formation of an edge triggering D flip-flop

3.3.1 Setup Time, Hold Time and Propagation Delay of DFF

Setup time and hold time are two important parameters of timing waveforms in logic circuits. Setup time and hold time describe the timing requirements on the data input of a flip-flop with respect to the clock input [33]. Setup time and hold time describe a window of time during which data must be stable in order to guarantee predictable performance over the full range of operating conditions and manufacturing tolerances. Specifically, the positive setup time is defined as the minimum time preceding the clocking event that the data input must remain stable to be validly recognized. A positive hold time, on the other hand, describes the length of time that the data to be clocked into the flip-flop must remain available and stable after the active clock edge. A positive setup time limits the maximum clock rate of a system, but a positive hold time can cause malfunction at any clock rate.

Basically, setup time and hold time can be looked at as the changes in the clock to the propagation delay as the sampling clock edge approaches the data edge [33]. The propagation delay is the amount of time it takes to charge the parasitics associated with the output node when the clock edge changes. There is also a propagation delay or parasitics associated with the internal node that the data edge charges when it changes. If the data edge and the clock edge become very close together, then the two delays become additive and the total propagation delay increases. The propagation delay will continue to increase as the edges become in phase then reduce as the edges cross and become skewed the other way. The setup and the hold windows are considered to be the area of non-constant propagation delays. The setup time, the hold time, and the propagation delay (when sampling a high data signal) are shown in Figure 3.5.

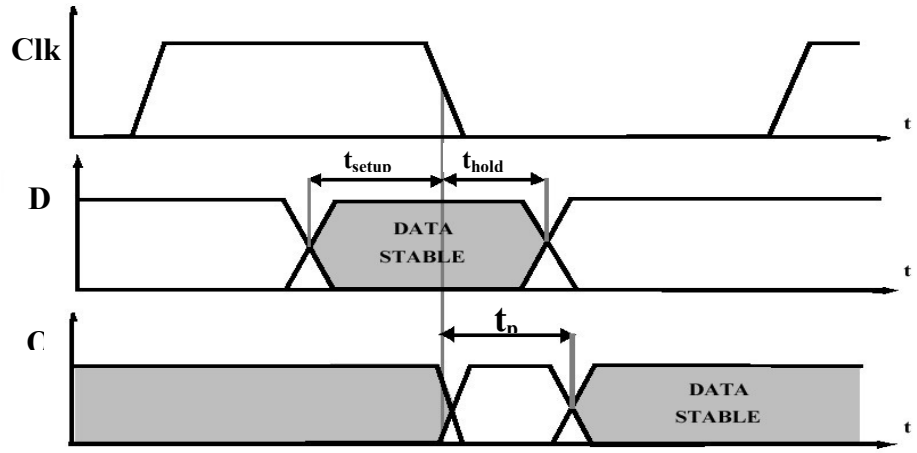


Figure 3.5 Setup time, hold time and propagation delay

Sum of the setup time and the propagation delay (clock to Q delay) is the only true measure of the speed performance. Maximum operating clock for a DFF is defined by minimum clock period which is-

$$T_{\min} = t_{setup} + t_{pd} + t_{skew} \quad \text{....(Eq. 3.5)}$$

Long propagation delay with longer setup time makes the latch permissible to operate at higher frequencies. The propagation delay depends on charging parasitics. The current trend in the high-speed logic circuitry is to reduce the output swing [11]. Charging or discharging in reduced swing minimizes the propagation delay. By using current-mode approach, switching between two currents can easily set the output voltage levels. The variation in propagation delay with respect to the clock-data edge time is shown in Figure 3.6. This figure compares this delay for the DFF under consideration with a typical digital DFF cell. For the designed DFF, the setup and the typical delay time are found to be *6.3 ps* and *380.1 ps*, respectively whereas for typical digital DFF, they are *152 ps* and *638.4 ps*, respectively.

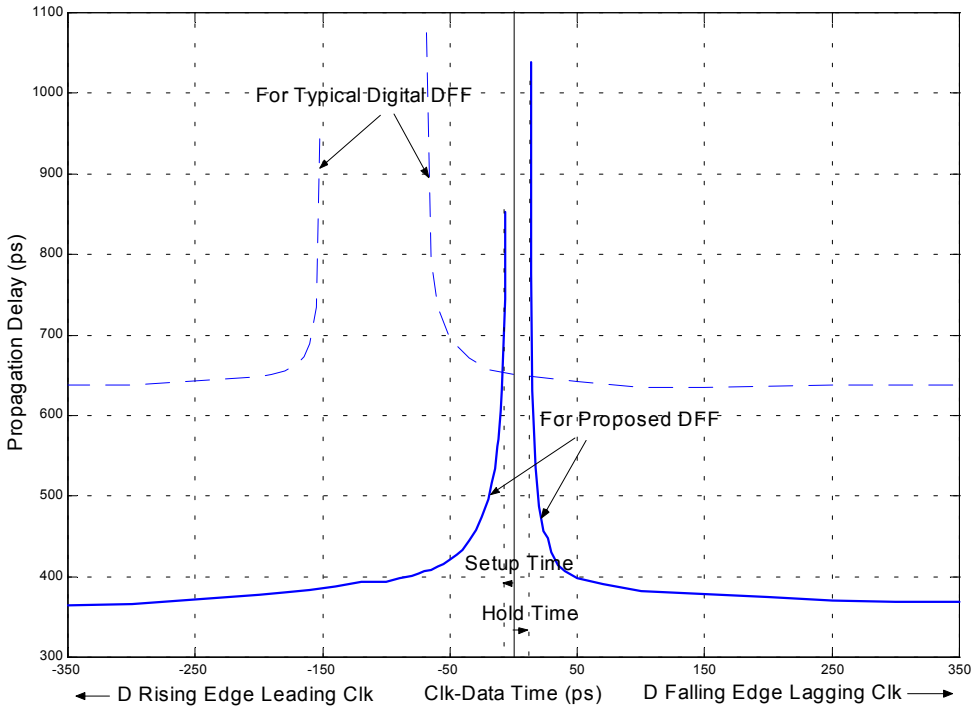


Figure 3.6 Delay vs setup/hold time curve

Now let us discuss the effect of the setup and the propagation delay time on the maximum operating clock frequency for the divider. Let us consider a divider with fixed diving ratio of 2. This divider is nothing but a DFF with negative feedback to the input. In this case, after one active clock edge the next clock should not be applied unless the data is stable to the input. It means that the clock period should be less than T_{min} as described in Eq. 3.5. Here T_{min} is the time required to make the data stable at the input. If the skew time is neglected, the T_{min} for the DFF under consideration is found to be *≈386.4 ps*. That means the maximum operating clock frequency for the divider with dividing ratio of 2 is *≈1/(386.4 ps) ≈ 2.58 GHz*. It is interesting to notice from the simulation that

the maximum operating clock frequency is *2.45 GHz* for this divider. For a typical digital divider with diving ratio of 2 it is found to be *1.25 GHz*.

3.4 Logic Gates

Figure 3.7 shows the differential circuit used for different logic operations. Depending on input logic level, this circuit can be used for 'AND', 'OR', 'MUX' or any logic operation.

The logic operations are found as follows:

'AND' operation: if B='LOW', F=A C

'OR' operation: if B='HIGH', F=A + $\overline{C}$

'MUX' operation: if C='HIGH', F=A

& if C='LOW', F=B

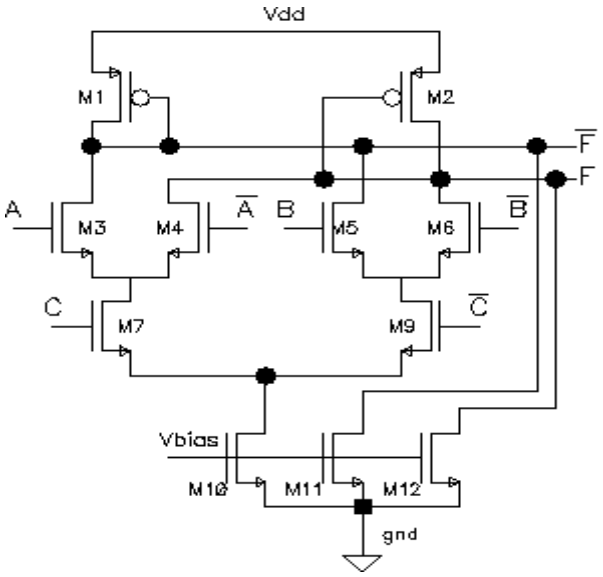


Figure 3.7 Logic gate

3.5 Results and Discussion

Dividers with fixed and programmable dividing ratios were designed and simulated in *CMOS 0.25* μm process using Cadence Design tools. Simulation has been performed by SPECTRE simulator for two dividers with fixed dividing ratios of 2 and 3 for a typical process corner. The results for the designed fixed dividers are compared with the results of the digital fixed dividers in Table 3.1. A programmable divider has been designed for N=2 and programmable dividing ratios of {6, 7, 8 and 9} have been obtained. This programmable divider has been simulated for all dividing ratios {6, 7, 8 and 9} for typical process as shown in Table 3.1. Circuits for dividing ratios 6, 7, 8 work well up to *1.37 GHz* for a typical process. Circuit for dividing ratio of 9 works up to *1.12 GHz* for typical condition as it uses all logic blocks and using all logic blocks introduce more delay. The summary of simulation results is shown in Table 3.1.

The simulated waveforms for "dividing ratio 9" for 1GHz input clock are shown in Figure 3.8. In real cases, the clock and inverting clock edges are not perfectly square wave. For simulation purpose, the clock and the inverting clock have been given to the input with larger rise and fall time. A reset control has been added with the dividers to reset the output at the start so that these can initiate the circuit from an initial condition.

The speed performance of the dividers depends on parasitic capacitances and resistances of the MOS transistors, the biasing currents, the input/output voltage swing, etc. The following factors limit the speed performance of the dividers:

Table 3.1 Simulation results for a typical process

Parameters	**From proposed DFF and logic gate**	**From typical digital DFF and logic gate**	**Unit**
Supply Voltage, Vdd	*3.3*	*3.3*	V
Operating Temperature	*27*	*27*	°C
Process	Typical	Typical	
Input Clock Voltage	*1.4-2.4*	*0-3.3*	V
Divider with fixed ratio 2			
Max Operating Input Clock	*2.58*	*1.25*	GHz
Output Volt at Max In-Clk	*1.48-2.15*	*0-3.3*	V
Output Voltage at 1.575 GHz	*1.35-2.35*	-	V
DC Power Dissipation	*2.59*	681.3×10^{-9}	Mw
Total 'ON' dc current	*≤ 783.8*	206×10^{-6}	μA
Divider with fixed ratio 3			
Max Operating Input Clock	*1.62*	*0.98*	GHz
Output Volt at Max In-Clk	*1.3-2.45*	*0-3.3*	V
DC Power Dissipation	*6.88*	1.25×10^{-6}	mW
Total 'ON' dc current	*≤ 2.08*	0.37×10^{-6}	mA
Programmable Divider with ratio {6, 7, 8 & 9}			
Max Operating Input Clock	*1.12*	*0.7*	GHz
Output Volt at Max In-Clk	*1.25-2.65*	*0-3.3*	V
DC Power Dissipation	*18.26*	*2.46*	mW
Total 'ON' dc current	*≤ 5.53*	741×10^{-3}	mA

1) The speed performance of the dividers is greatly affected by the gate-channel capacitances of the input transistors and the clock-switching transistors of the DFF. By detailed analysis, it can be shown that as the gate current is small, the gate capacitances play most important role for changing the input state from one to another. These gate capacitances are responsible for some delay to reach the required transition voltage, which introduces some delay from the inputs to the output. In fact, this delay affects the speed of the DFF.
2) For changing the voltage state from low level to high level, the PMOS active loads are charged by the changing current from a higher level to a lower level. The capacitance, resistance and the current of the PMOS transistors play most important role for speed performance. They cause coupling effect in the rising edge and the falling edge of the output. If the skews of the rising and the falling edge of the output are comparable with the period, it significantly affects the overall speed of the dividers.

To improve speed performance, the parasitic capacitance of the switching transistors should be lowered by reducing their dimensions. But reducing their dimensions does not leave enough headroom for M10 transistor (Figure 3.3). The dimensions (W/L ratios) of PMOS transistors, which are used as active load, are crucial for the design. They affect both the speed and the output level. The maximum attainable speed of the divider depends on the tradeoff between the parasitic capacitance and the current flow through these transistors. Increasing the dimensions of PMOS transistors increase their drain voltages, which in turn increase the current flowing through them. But it will increase their parasitic capacitance, as well.

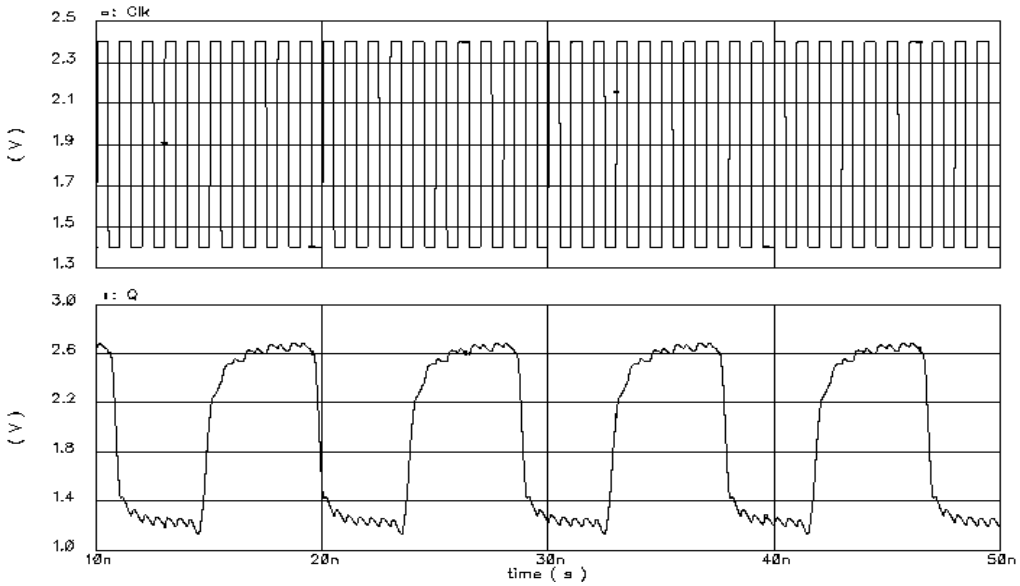


Figure 3.8 Simulation Waveforms for "dividing ratio 9" (for 1GHz input clock)

From simulation, it has been found that, for a certain range of W/L ratio, a *10%* increase of the dimensions (W/L ratio) of these transistors increase speed limit effectively by about *87 MHz*. Beyond this range, effect of the parasitics dominates and causes greater delay. Another drawback of increasing W/L ratio is that, it decreases the output swing. As the switching occurs from time to time, a constant noise level is introduced both in the upper limit and the lower limit of the output. This noise has constant level and it becomes comparable to reduced output swing.

Moreover, the output swing level can be increased by increasing the current in M10 (Figure 3.3) and the current can be increased by increasing the dimensions of M10. This may reduce enough headroom for this transistor and cause the device to operate in linear region rather than keeping in saturation region during switching. To ensure the perfect rejection to the common mode noise perfectly, we have to ensure that these transistors stay in saturation region in entire output swing during switching.

Chapter 4

Voltage Controlled Oscillator (VCO)

4.1 Introduction

The most sensitive and critical block that determines the noise performance of a frequency synthesizer is the oscillator, typically in the form of a voltage controlled oscillator (VCO). Low noise VCOs are integral part of high performance PLL systems such as frequency synthesizers used in wireless transceivers. It is therefore critically important to build a low power and low phase noise VCO to achieve low jitter in presence of large supply noise caused by digital circuitry. The output frequency of a VCO must typically cover a wide range of frequencies for a limited range of input control voltage, implying a high gain with a low control voltage. The oscillator pull-range has to be adequate to cover the frequency variation of the oscillator with temperature and power supply variations.

VCO can be implemented with several different ways. The resonant circuit VCOs with an LC tank as the resonant element has an excellent phase noise performance. However, these usually require off-chip components defeating the purpose of integration. Recently, on-chip implementations of inductors have been reported, but these generally have a low Q and are bulky. Bond-wire inductors have been proposed [17, 34] with a higher Q but require special processing. Modeling of the on-chip inductor is a cumbersome process. Generally LC oscillators take significant amount of power to achieve desired swing. Ring

oscillators however are attractive from integration and cost point of view and are being increasingly employed in noise sensitive applications. In this chapter, the design technique of ring oscillators using differential delay cells with different types of load elements is described. These ring oscillators are analyzed for their noise performance and frequency of oscillation.

4.2 Operating Principle of VCO

An oscillator generates a periodic output. As such, the circuit must entail a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal [12]. Most RF oscillators can be viewed as feedback circuits. Let us consider the simple linear feedback system as depicted in Figure 4.1, with the overall transfer function,

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)} \qquad \text{....(Eq. 4.1)}$$

A self-sustaining mechanism arises at the frequency s_0 if $H(s_0) = +1$, and the oscillation amplitude remains constant if s_0 is purely imaginary, i.e. $H(s_0=j\omega_0) = +1$. Thus, for steady oscillation, two conditions must be simultaneously met at ω_0:

1) The loop gain, $\left|H(j\omega_0)\right|$ must be equal to unity
2) The total phase shift around the loop, $\angle H(j\omega_0)$ must be equal to zero or 360° (or 180° if the dc feedback is negative)

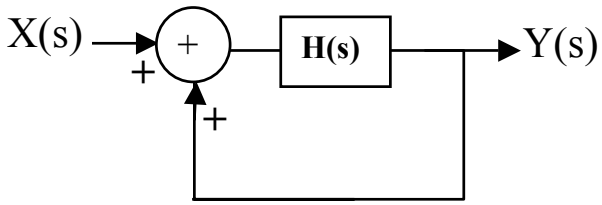


Figure 4.1 Feedback oscillatory system

These conditions are called "Barkhausen Criteria" for oscillation. The above conditions imply that any feedback system can oscillate if its loop gain and phase shift are chosen properly, as for example, ring oscillators and phase shift oscillators. These conditions are necessary but not sufficient. In order to ensure oscillation in the presence of temperature and process variations, the loop gain should be at least twice or three times the required value [25]. The frequency of most RF oscillators must be adjustable. In the VCO, the output frequency of an oscillator can be varied by a control voltage.

4.3 Ring Oscillators

A ring oscillator consists of a number of delay stages configured in a loop. Usually delay stages can be realized with normal single-ended or differential inverter delay cells. Because of common mode noise rejection, the differential delay cells are preferred over single-ended inverter stages for low noise applications [16]. If N numbers of delay stages are used in the ring oscillator, the frequency of oscillation can be shown as,

$$f_{osc} = \frac{1}{2NT_d} \qquad \text{....(Eq. 4.2)}$$

where T_d is the delay per stage.

In this work, ring oscillators are designed and analyzed with two different types of load elements for expected performance. The first oscillator consists of differential delay stages with PMOS active load operated in the triode region (often called triode load) and the second one is designed with symmetric load elements. Symmetric load elements are composed of a diode connected PMOS device in shunt with an equally sized biased PMOS device.

4.4 Ring VCO with Triode Load

In this work, a ring oscillator with three differential delay stages is designed. Figure 4.2 shows a ring oscillator which uses three differential delay stages and the wire inversion is made at the end. When the ring oscillator oscillates at f_{osc}, each stage contributes a frequency dependent phase shift of 60°, which makes total frequency dependent phase shift of 180°. The frequency of oscillation (f_{osc}) is found from Eq. 4.2 and that is,

$$f_{osc} = \frac{1}{6T_d} \qquad \text{....(Eq. 4.3)}$$

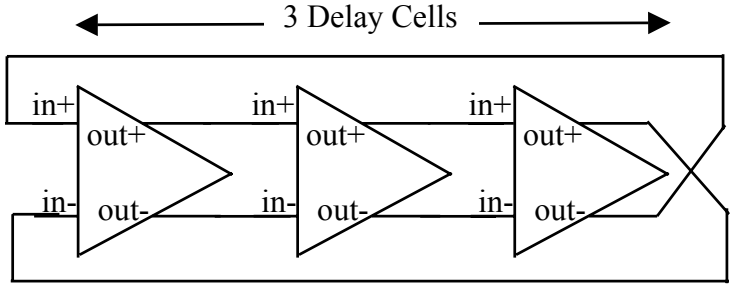


Figure 4.2 Ring oscillator with three differential delay stages

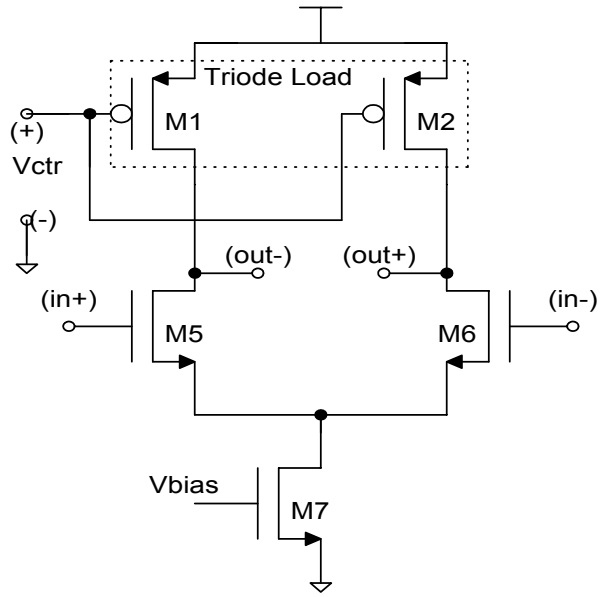


Figure 4.3 Differential delay cell with triode load

The differential delay cell with triode loads is shown in Figure 4.3. It features a source coupled NMOS differential pair M5/M6 with the active loads that are implemented by transistor pairs M1/M2. Transistors M1/M2 are biased such a way that they are operated in the triode or the linear region. In the triode region operation, the PMOS loads offer almost linear resistance with the variation of the drain-source voltage. The control voltage, V_{ctr} is used to vary the load resistance of the triode load, i.e. to vary the frequency of oscillation. The bias voltage, V_{bias} is obtained from a separate bias generation circuitry. For a fixed swing over the process, the temperature, and the power supply variation, a current source bias circuit is used. In this bias circuit, V_{ctr} is also used to generate the bias voltage, V_{bias} voltage for the NMOS current source. This bias circuit is discussed in Appendix A.1.

The typical DC transfer characteristic of a differential delay cell is shown in Figure 4.4. At equilibrium, the tail current is divided into two active loads, so half of the tail current ($I_{SS}/2$) flows through each of PMOS devices. During oscillation, the entire tail current (I_{SS}) is steered from one side to the other. Therefore, the voltage drop across the load swings from 0 to V_{sw} as shown in Figure 4.4 and the voltage swing at the output of the oscillator swings from V_{dd} to (V_{dd} - V_{sw}). The differential input voltage required to fully switch the differential pair is approximately $\sqrt{2}$ times the (V_{GS5} -V_{TN}) bias point of the differential pair in the balanced case with a differential input of zero [18]. The swing voltage, V_{sw} can be determined from the drain current equation for the triode region,

$$I_{SS} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_1 \left[2\left(V_{GS1} - V_{TP}\right)V_{DS1} - V_{DS1}^2\right]\Bigg|_{V_{DS1}=V_{sw}} \quad \text{....(Eq. 4.4)}$$

where, $V_{GS1} = V_{dd} - V_{ctr}$.

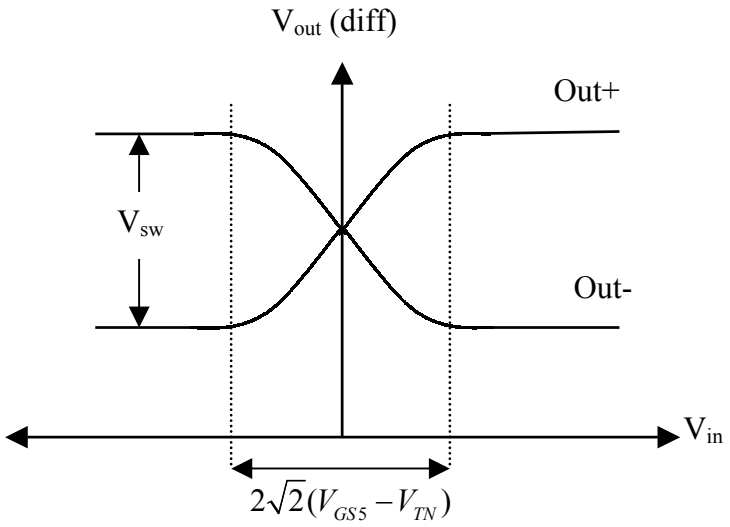


Figure 4.4 DC transfer characteristic for differential delay cell

It is desirable to keep the resistive PMOS load transistors in the triode region of operation. This requires a drain-source voltage that is kept below the (V_{GS1} -V_{TP}) bias point of the PMOS transistors,

$$V_{sw} \le V_{GS1} - V_{TP}$$

or, $$V_{sw} \le V_{dd} - V_{ctr} - V_{TP} \quad \text{....(Eq. 4.5)}$$

To calculate the frequency of oscillation, the delay in the each delay cell can be found to be,

$$T_d = R_L \cdot C_L \quad \text{....(Eq. 4.6)}$$

where, R_L, C_L are the effective output load resistance and the output capacitance of the delay stage.

The effective output resistance R_L is the parallel combination of the output resistance of the active load and the output resistance of the NMOS differential pair (M5 or M6 in Figure 4.3). Since the output resistance of the PMOS active load is typically much less than the output resistance of the differential pair, R_L is almost equals to the output resistance of the symmetric load.

The small signal resistance of the PMOS load is given by,

$$R_L = \left(\frac{dI_{D1}}{dV_{DS1}} \right)^{-1}$$

If the drain current for triode region is given by,

$$I_{D1} = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L} \right)_1 \left[2\left(V_{GS1} - V_{TP} \right) V_{DS1} - V_{DS1}^2 \right] \quad \text{....(Eq. 4.7)}$$

then, the effective resistance is,

$$R_L = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \left[V_{GS1} - V_{TP} - V_{DS1}\right]} \quad \text{....(Eq. 4.8)}$$

If the load is biased well into the triode region so that its output resistance is not too nonlinear, then the small signal resistance at the midpoint of the V_{DS} vs. I_D curve is a good representation of the average resistance. This is the point where $I_{D1}=I_{SS}/2$ and $V_{DS1}=V_{SW}/2$. In this case, the effective load resistance is,

$$R_L = \frac{V_{sw}}{I_{SS}} \quad \text{....(Eq. 4.9)}$$

The load capacitance, C_L seen at the output consists of the gate-to-source capacitance of the next stage, the drain-to-gate capacitance of the triode load, as well as the drain to bulk parasitic capacitances. The input capacitance of the next stage is either $(2/3)W_5L_5C_{ox}$ or $W_5L_5C_{ox}$ depending on whether the device is in the saturation or the cut-off regions. The triode load capacitance is approximately $(1/2)W_1L_1C_{ox}$. Likewise, the drain-to-bulk parasitics are approximately proportional to the product of the gate width and the gate length of the respective devices. Now, the total output capacitance can be reasonably modeled as a constant times $K_L(WLC_{ox})$, where the constant is made up of the contributions of each of the capacitances at the output.

$$C_L = K_L(WLC_{ox}) \quad \text{....(Eq. 4.10)}$$

If this is expressed in terms of the gate width and the gate length of the triode load device, then it can be substituted into Eq. 4.6.

$$T_D = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \left[V_{GS1} - V_{TP} - V_{DS1}\right]} \times K_L\left(W_1L_1C_{ox}\right)$$

or, $$T_D = \frac{K_L L_1^2}{\mu_p \left[V_{dd} - V_{ctr} - V_{TP} - V_{DS1} \right]} \quad \text{....(Eq. 4.11)}$$

So the frequency of oscillation is found from the Eq. 4.3,

$$f_{osc} = \frac{\mu_p}{6 K_L L_1^2} \left[V_{dd} - V_{ctr} - V_{TP} - V_{DS1} \right] \quad \text{....(Eq. 4.12)}$$

Hence, the relationship between the VCO operating frequency and the control voltage is linear to a first order. This is desirable especially in a PLL-based system because a highly non-linear voltage-frequency characteristic tends to degrade the performance of the PLL on account of a non-constant VCO gain.

4.4.1 Gain of Delay Cell and Swing Consideration

The small signal ac gain of the differential delay cell is,

$$a_V = g_{m5} R_L \quad \text{....(Eq. 4.13)}$$

For the delay cell with triode active loads, the gain is,

$$a_V = \mu_n C_{ox} \left(\frac{W}{L} \right)_5 \left[V_{GS5} - V_{TN} \right] \times \frac{V_{sw}}{I_{SS}}$$

If $$I_{SS} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right)_5 \left[V_{GS5} - V_{TN} \right]^2$$, then,

$$a_V = \frac{V_{sw}}{V_{GS5} - V_{TN}} \quad \text{....(Eq. 4.14)}$$

The choice of output swing, V_{SW}, is influenced by several competing factors. At the top level there is the trade-off between the noise margin and the speed where the speed favors low output swing and the noise margin favors high output swing. There are many other

factors as well. For example, the gain of each inverter stage must be greater than one (with a sufficient safety margin) for a ring to oscillate. From Eq. 4.14, the gain of a single stage is approximately equal to the ratio of the output swing to the (V_{GS5} -V_{TN}) bias point of the NMOS differential pair devices. That means a low swing will require a low (V_{GS5} - V_{TN}) bias point, which results in a higher thermal noise-induced jitter per stage.

There are also considerations which limit how large of an output swing is useful. First, it is desirable to keep the resistive PMOS load transistors in the triode region of operation. However, it is usually preferable to keep the load devices in the deep triode region over the entire range of the output voltage swing. This provides a more linear output resistance that helps with the shape of the output waveforms, including the matching between the rising and falling waveform shapes. It also guarantees good performance over process variation. For this reason an even smaller output swing is desired. Another limit on the output swing comes from considerations of the differential pair transistors. When one differential delay stage drives a similar, second stage, then the differential pair transistor with a high input voltage requires a large enough V_{DS} to remain in saturation.

4.4.2 VCO gain (K_{VCO})

The VCO gain is given by [15],

$$K_{VCO} = \left| \frac{df_{osc}}{dV_{ctr}} \right| \qquad \text{….(Eq. 4.15)}$$

Using Eq. 4.12, if we assume that the effective load capacitance remains unchanged with the change of the drain-source bias of the PMOS active loads, then the VCO gain is,

$$K_{VCO} = \frac{\mu_p}{6K_L L_1^2} \quad \text{....(Eq. 4.16)}$$

So, the VCO gain is approximately independent of the control voltage and a constant gain is achieved, which is desirable in most of the PLL system.

A ring VCO (Osc-1) is designed and simulated for *TSMC 0.25 μm* CMOS process. $(W/L)_1$ and $(W/L)_5$ are taken as *(1.2μ/0.3μ)* and *(6.3μ/0.3μ)*. Its tuning characteristic drawn from simulation results is shown in Figure 4.5. The sample simulation results for VCO output at *1.5552 GHz* oscillation frequency is shown in Figure 4.6. The required control voltage for *1.5552 GHz* frequency of oscillation is found to be *1.0146 volts*. The swing found from the Figure 4.6 is ≈ *0.80* volt. From Eq.4.5, the maximum control voltage that can operate the PMOS load in triode region is $V_{ctr} \le (3.3 - 0.80 - V_{TP}) \approx 1.7V$. The tuning characteristic curve reveals the same fact. The frequency of oscillation varies almost linearly with the control voltage up to *1.7 volts* and in this linear region, the VCO gain is found to be 1.08×10^9 *Hz/volts*.

4.5 Timing Jitter and Phase Noise in Ring VCO with Triode Load

Timing jitter and phase noise are the manifestation of random variation in phase. One is the time domain characterization of error and the other is the equivalent frequency domain characterization. Let us consider the output of an oscillator,

$$x(t) = A\cos\{2\pi f_{osc} t + \theta(t)\} \quad \text{....(Eq. 4.17)}$$

Here, $\theta(t)$ represents the phase fluctuations. Timing jitter arises from the uncertainty of the edge of the expected output. Figure 4.7 shows the individual delay stage timing jitter.

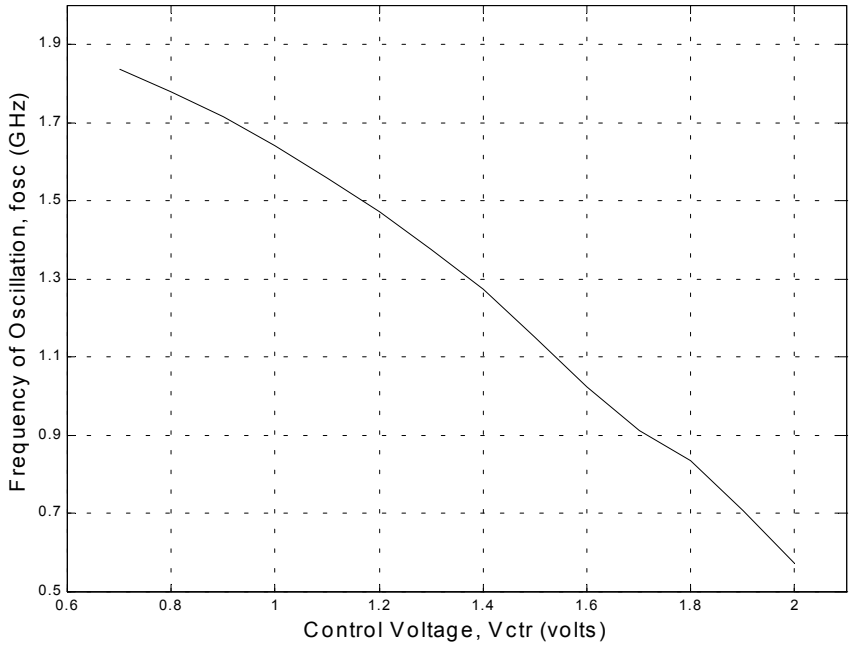


Figure 4.5 VCO tuning characteristics

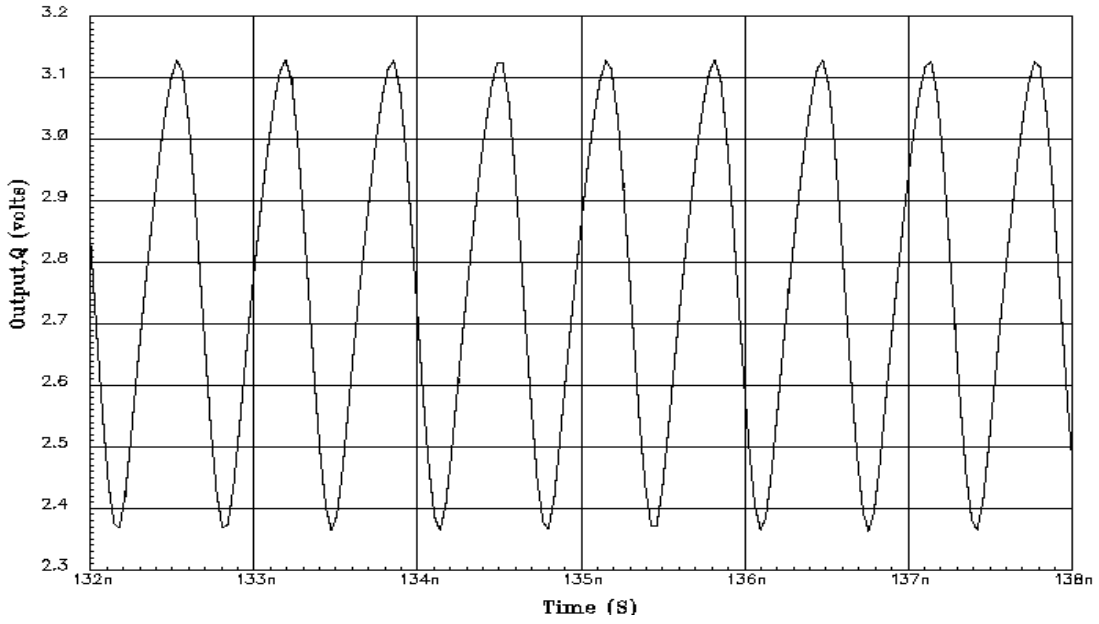


Figure 4.6 VCO output at 1.5552 GHz oscillation frequency

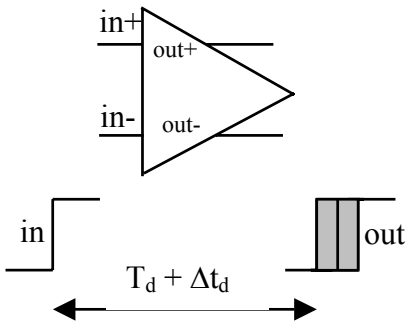


Figure 4.7 Intrinsic timing error per delay stage

4.5.1 Noise in MOSFET

Jitter can be caused by the internal or the external sources. Internal Jitter is contributed by the noise sources of the active devices. In the range of the offset frequency of 1kHz to 10MHz (approximately), the noise is dominated by the thermal noise. The aspect of the delay cell of primary concern in the latter section is device thermal noise and its impact on timing jitter. The schematic for this delay cell is repeated in Figure 4.9 with thermal noise sources added. These are the intrinsic output referred thermal noise current sources for each transistor, and should not be confused with the input referred noise sources used at other times when modeling the noise [18].

For the saturation region of the devices, the thermal noise current power spectral density is given by,

$$\frac{\overline{i_n}^2}{\Delta f} = 4kTg_m\gamma \qquad \text{....(Eq. 4.18)}$$

where, g_m is the transconductance for a given bias condition and γ is also function of bias.

In traditional noise analysis, for long channel, γ is usually 2/3. For short channel devices, however, experimental results [20, 21] suggest that value of γ is higher, and increases with increasing V_{ds}. For short channel devices in deep saturation, γ can be as high as 2 or 3.

For the triode region of operation, the thermal noise current power spectral density is modeled by:

$$\frac{\overline{i_n}^2}{\Delta f} = 4kTg_{dso}\gamma \qquad \text{....(Eq. 4.19)}$$

where, g_{dso} is the zero-bias drain to source conductance and γ varies from $1 < \gamma < 2/3$ as V_{DS} varies from zero to the onset of saturation. For the deep triode region, γ is close to 1. An expression for γ is derived in [22, 23] and is given as below,

$$\gamma = \frac{1-\upsilon+\left(\upsilon^2/3\right)}{1-\upsilon/2} \qquad V_{ds} < V_{dsat}$$

$$\gamma = 2/3 \qquad V_{ds} \geq V_{dsat} \qquad \text{....(Eq. 4.20)}$$

where, $\upsilon = V_{ds}/V_{dsat}$. As can be observed from the above equation, for V_{ds}=0, γ=1 and in saturation γ=2/3 and stays constant.

A more complicated model for triode region current noise in the short channel devices has been reported [21]. One major reason for the electrical characteristics of the short channel devices to deviate from those of long channel devices is the velocity saturation of the carrier caused by the high lateral electric field [24]. The thermal noise current density for a short channel device is given by [21],

$$\frac{\overline{i_n}^2}{\Delta f} = 4kTg_{meff}\gamma \qquad \text{....(Eq. 4.21)}$$

where,

$$\gamma = \left(\frac{g_{meff}}{I_d}\right)^3 \left[\left(V_{gs} - V_T\right)^2 V_{ds} - \alpha_x \left(V_{gs} - V_t\right) V_{ds}^2 + \frac{\alpha_x^2}{3} V_{ds}^3\right] - \frac{g_{meff}}{L I_d E_C}\left[\left(V_{gs} - V_T\right) V_{ds} - \frac{\alpha_x}{2} V_{ds}^2\right]$$

….(Eq. 4.22)

V_T is the threshold voltage and I_d is the drain current of the MOSFET.

The effective channel transconductance is given by,

$$g_{meff} = \sqrt{\mu_{eff} C_{ox} \left(\frac{W}{L}\right) I_d} \qquad \text{….(Eq. 4.23)}$$

In this expression, μ_{eff} is the effective surface mobility due to velocity saturation and it can be expressed as,

$$\mu_{eff} = \frac{\mu_0}{1 + \theta\left(V_{gs} - V_t\right)} \qquad \text{….(Eq. 4.24)}$$

Here, α_x represents the bulk effect on threshold voltage and θ is a fitting parameter roughly equal to $\left(10^{-7}/t_{ox}\right) V^{-1}$. These equations model both the triode region as well as the saturation region. For the saturation region, the value of γ is constant and it can be found from Eq. 4.22 for $V_{ds} = V_{dsat}$ (drain to source saturation voltage).

4.5.2 Jitter in Delay Stage and Zero-Crossing Approximation

The timing error per stage due to the noise can also be calculated with the assumption that the next stage will begin switching abruptly when the differential output voltage reaches zero. In exact terms, this amounts to a problem known as the “first crossing problem” [19], which is defined as the problem of predicting the time of the first

threshold crossing in the presence of noise. A useful approximation, frequently employed in this case is called the "first crossing approximation", and is illustrated at the bottom part of Figure 4.8. For a voltage error at the nominal time of crossing of magnitude ΔV_n, the actual time of crossing would be offset by an amount equal to ΔV_n divided by the slope the line through zero, or the slew rate. The first crossing approximation predicts that the variance of the timing jitter in this case is equal to the variance of the voltage noise divided by the slew rate squared, or

$$\overline{\Delta t_d^{\,2}} = \overline{\Delta V_n^{\,2}} \times \left(\frac{C_L}{I_{SS}} \right)^2 \qquad \text{….(Eq. 4.25)}$$

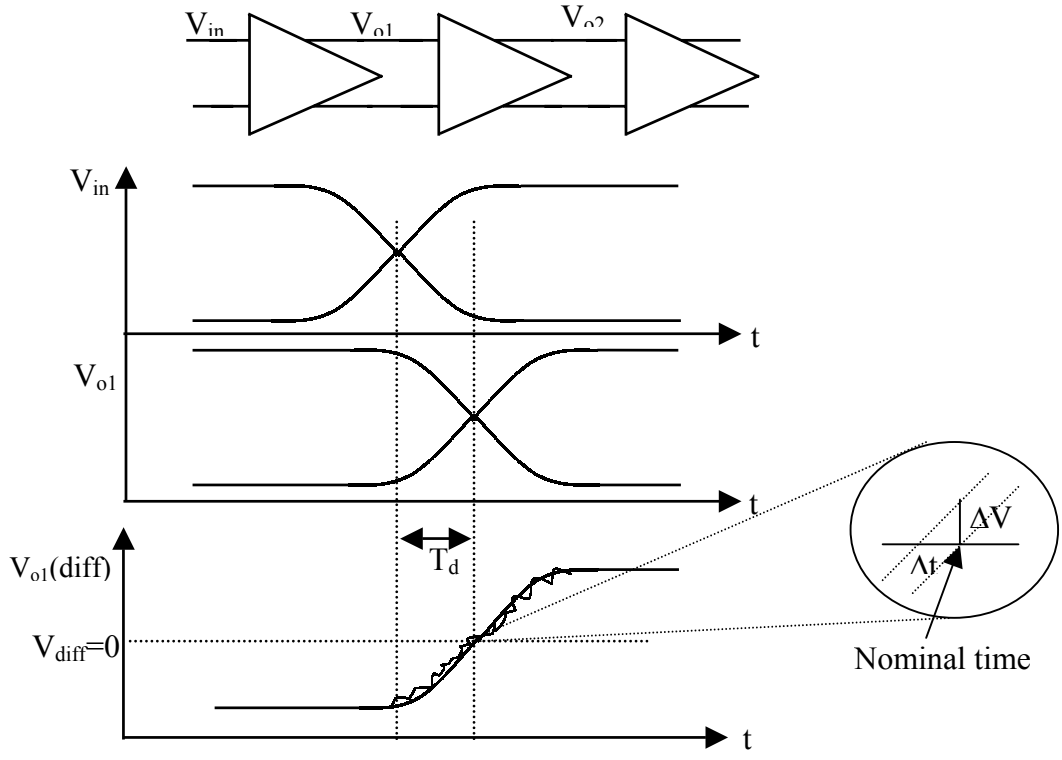


Figure 4.8 Output waveforms for differential delay stages

The delay cell with noise sources is shown in Figure 4.9. $\overline{i_{n1}^2}$, $\overline{i_{n2}^2}$, $\overline{i_{n5}^2}$, $\overline{i_{n6}^2}$, $\overline{i_{n7}^2}$ and $\overline{i_{n8}^2}$ represent the noise current densities for the transistors M1- M8. Now the total output noise voltage of the delay cell can be determined through the traditional noise analysis technique [18],

$$\overline{V_n^2} = \int_0^\infty \left(\overline{i_{n1}(f)^2} \left|H_1(f)\right|^2 + \overline{i_{n2}(f)^2} \left|H_2(f)\right|^2 + ... + \overline{i_{n8}(f)^2} \left|H_8(f)\right|^2 \right) df$$

…..(Eq. 4.26)

where, $H_1(f)$, $H_2(f)$, ……..,$H_6(f)$ are the transfer functions of the noise source referred to the output.

For the current source and biasing transistors (M7, M8), approximately half of the current noise shows up on each side of the differential output. Therefore a common mode noise signal results at the output, but not a differential one. The AC noise model is shown in Figure 4.10. R_L and C_L represent the effective load resistance and the capacitance at the output node.

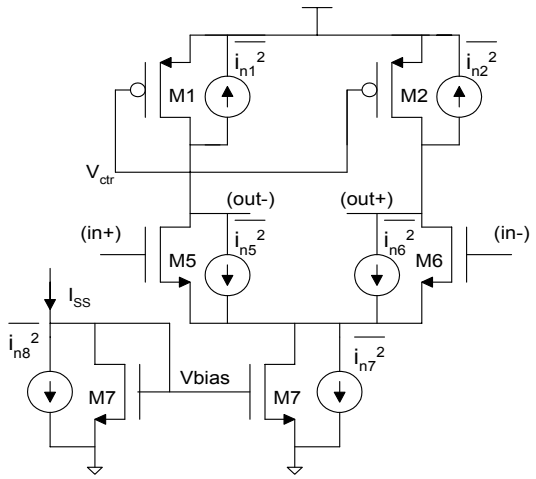


Figure 4.9 Noise current sources in the delay cell

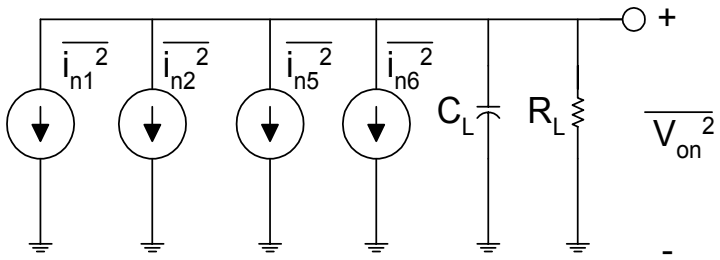


Figure 4.10 AC noise model for the delay cell

For the differential pair (M5/M6), both transistors are in saturation. So the noise current densities and the transfer functions are given by,

$$\overline{i_{n5,6}}^2 = 4kT\gamma_1 g_{m5}\Delta f \quad \text{....(Eq. 4.27)}$$

$$H_{5,6}(f) = \frac{R_L}{1 + j2\pi f R_L C_L} \quad \text{....(Eq. 4.28)}$$

where, γ_1 has the value of 2/3 for long channel device and for short channel it is as high as 2 or 3.

Output noise voltage for M5/M6,

$$\overline{V_{n5,6}}^2 = 4kT\gamma_1 g_{m5} R_L{}^2 \int_0^\infty \left| \frac{1}{1 + f/f_o} \right|^2 df \quad \text{....(Eq. 4.29)}$$

where, the 3-dB bandwidth of the RC system is,

$$f_o = \frac{1}{2\pi R_L C_L} \quad \text{....(Eq. 4.30)}$$

The integral in Eq. 4.29 reduces to $(\pi/2)f_o$ and so we get,

$$\overline{V_{n5,6}}^2 = \frac{kT}{C_L}\gamma_1 g_{m5} R_L = \frac{kT}{C_L}\gamma_1 a_v \quad \text{....(Eq. 4.30)}$$

where, a_v is the ac gain of each differential delay stage and $a_v = g_{m5}R_L = \frac{V_{sw}}{V_{GS5} - V_{TN}}$.

For PMOS loads M1/M2, calculating noise voltage is not straightforward. When $|V_{ds}| \to 0$, the transistors are in deep triode region and the noise current,

$$\overline{i_n}^2 = 4kT\gamma_2 g_{dso1}\Delta f$$

Here, γ_2 is very close to '1' as transistor M1/M2 are in deep triode region.

When $|V_{ds}| >> 0$, the transistor is in ohmic region depending on the value of drain to source bias. So, γ is determined by the drain to source bias. The noise current is given by,

$$\overline{i_n}^2 = 4kT\gamma_3 g_{dso1}\Delta f$$

where, g_{dso1} is the channel conductance with zero drain-to-source bias. If the load resistance with zero drain-to-source bias is R_{Lo}, then $R_{Lo} = \frac{1}{g_{dso1}}$.

The average noise current density is given by,

$$\overline{i_{n1,2}}^2 = 2kT(\gamma_2 + \gamma_3) g_{dso1}\Delta f \quad \text{....(Eq. 4.32)}$$

Finally, output noise voltage for M1/M2,

$$\overline{V_{n1,2}}^2 = \int_0^\infty 2kT(\gamma_2 + \gamma_3) g_{dso1} \left| \frac{R_{Lo}}{1 + j2\pi f R_{Lo} C_L} \right|^2 df$$

$$= 2kT(\gamma_2 + \gamma_3) g_{dso1} R_{Lo}$$

$$= \frac{kT}{C_L} \frac{\gamma_2 + \gamma_3}{2} \quad \text{....(Eq. 4.33)}$$

Combining all these results of (Eq. 4.31) and (Eq. 4.33), the total output voltage noise is given by,

$$\overline{V_n}^2 = \frac{kT}{C_L}\left[2A_v\gamma_1 + (\gamma_2 + \gamma_3)\right]$$

$$\overline{V_n}^2 = \frac{kT}{C_L}\xi^2 \quad \text{....(Eq. 4.34)}$$

where, $\xi^2 = 2A_v\gamma_1 + (\gamma_2 + \gamma_3)$ ....(Eq. 4.35)

and ξ^2 is called as the noise contribution factor [16].

The noise sources associated with the NMOS differential pairs and the tail currents are highly time varying in nature. Also, for a typical CMOS delay chain, the switching times of the adjacent stages overlap. This means that there are times when more than one stage is in the active region of amplification. This has been suitably accounted for in [16]. Analyzing these effects, the noise contribution factor changes and the output noise voltage gets multiplied by a factor of $a_v^2/2$. This is shown below,

$$\overline{V_n^2} = \frac{kT}{C_L}\cdot\xi^2\cdot\frac{a_v^2}{2} \quad \text{....(Eq. 4.36)}$$

Using First-Cross approximation, the output timing uncertainty at the output of noisy delay cell is found from the Eq. 4.25 as,

$$\overline{\Delta t_d}^2 = \frac{kT}{C_L}\xi^2\frac{a_v^2}{2}\left(\frac{C_L}{I_{SS}}\right)^2 \quad \text{....(Eq. 4.37)}$$

4.5.3 Jitter at VCO Output

For N-stage configuration, the period of oscillation is given by,

$$T_{osc} = 2NT_d \quad \text{....(Eq. 4.38)}$$

If the noise sources in the successive stages are independent, then the total jitter variance for one cycle of oscillation is given by,

$$\overline{\Delta t_{VCO}}^2 = 2N\overline{\Delta t_d}^2 \quad \text{....(Eq. 4.39)}$$

or, $$\overline{\Delta t_{VCO}}^2 = \frac{T_{osc}}{T_d}\frac{kT}{C_L}\xi^2\frac{a_v^2}{2}\left(\frac{C_L}{I_{SS}}\right)^2 \quad \text{....(Eq. 4.40)}$$

Substituting $a_V = \frac{V_{sw}}{V_{GS5} - V_{TN}}$, in the above equation, we get,

$$\overline{\Delta t_{VCO}}^2 = T_{osc}\frac{kT}{2I_{SS}}\xi^2\left(\frac{a_v}{V_{GS5} - V_{TN}}\right) \quad \text{....(Eq. 4.41)}$$

4.5.4 Phase Noise at VCO Output

If the VCO timing jitter is $\overline{\Delta t_{VCO}}$, the variance of phase error per cycle is given by [16],

$$\sigma_\phi^2 = (2\pi)^2\left[\frac{\overline{\Delta t_{VCO-rms}}}{T_{osc}}\right]^2 \quad \text{....(Eq. 4.42)}$$

If the phase noise of the oscillator has Gaussian Shape, it can be shown that the phase noise at the offset frequency of f_m is given by [16],

$$S_{VCO}(f_m) = \frac{1}{(2\pi f_m)^2}(2\pi.\Delta v) \quad \text{....(Eq. 4.43)}$$

and $$\sigma_\phi^2 = \frac{1}{(2\pi f_m)^2}(2\pi.\Delta v)T_{osc} \quad \text{....(Eq. 4.44)}$$

where, Δv is called the "line-width" of the spectrum.

Using these above three equations, power spectral density at the oscillator output can be derived as,

$$S_{VCO}(f_m) = \frac{1}{(2\pi f_m)^2} \frac{2\pi}{T_{osc}} \left[\frac{\overline{\Delta t_{VCO-rms}}}{T_{osc}} \right]^2$$

Substituting the value of $\left(\overline{\Delta t_{VCO-rms}}\right)^2$ in Eq. 4.44, we get,

$$S_{VCO}(f_m) = \left(\frac{f_{osc}}{f_m} \right)^2 \frac{kT}{2I_{SS}} \xi^2 \left(\frac{a_v}{V_{GS5} - V_{TN}} \right) \quad \text{....(Eq. 4.45a)}$$

or, $$S_{VCO}(f_m) = \left(\frac{f_{osc}}{f_m} \right)^2 \frac{kT}{2I_{SS}} \xi^2 \frac{V_{sw}}{(V_{GS5} - V_{TN})^2} \quad \text{....(Eq. 4.45b)}$$

From this noise analysis, an exclusive relationship between the phase noise and the power consumed by the ring VCO can be determined. I_{SS} can be scaled to reduce cycle-to-cycle jitter, or in this case, the phase noise. Once again, a scaling of I_{SS} implies a corresponding scaling of the gate width W of the load and the differential pair transistor, so that the output swing remains the same for the desired frequency of oscillation. From equation (Eq. 4.45), it is apparent that increasing the current consumed per delay stage will reduce the phase noise. For the current-mode-logic delay cells considered here, which consume static power, the power consumption is proportional to the tail current as well. That means, increasing tail current improves the noise performance, but it inherently increases power consumed by the oscillator. In addition, if the gate widths are scaled proportionally with the ratio of current to (V_{GS} -V_T), then total circuit area will increase as well.

4.6 Ring Oscillator with Symmetric Loads

The differential delay cell with the symmetric loads is shown in Figure 4.11. The reason for choosing these symmetric load elements is that they lead to good control over the

delay and the high dynamic supply noise rejection [13, 14, 15]. Transistors M2/M3 are in saturation and M1/M4 swing from the linear region to the saturation region.

The symmetric load is so called because its I-V characteristic is symmetric about the center of the voltage swing. Figure 4.12 shows the symmetric load and its I-V characteristics. The output impedance of this load is highly nonlinear. The dashed line in the Figure 4.12(b) shows the effective resistance of the load and illustrates the symmetry of its I-V characteristics. Let $V_{sw} = V_{dd} - V_{ctr}$. During oscillation, the entire tail current (I_{SS}) is steered from one side to the other. Therefore, the voltage drop across the load swings from 0 to V_{sw} as shown in Figure 4.12 and the voltage swing at the output of the oscillator swings from V_{dd} to V_{ctr}.

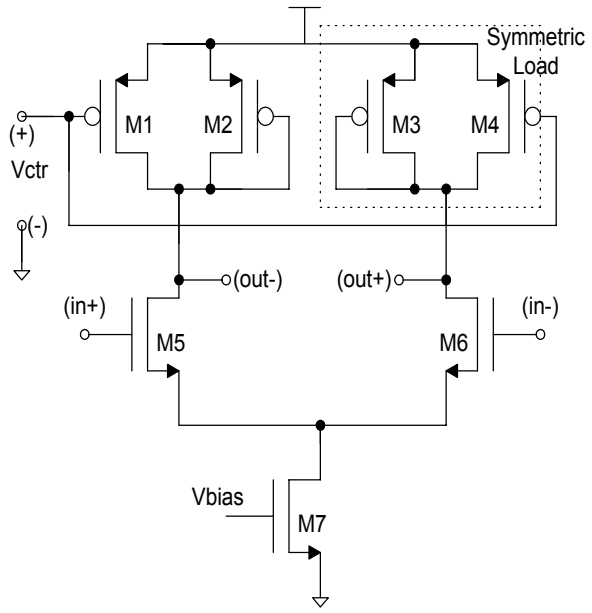


Figure 4.11 Symmetric load delay cell

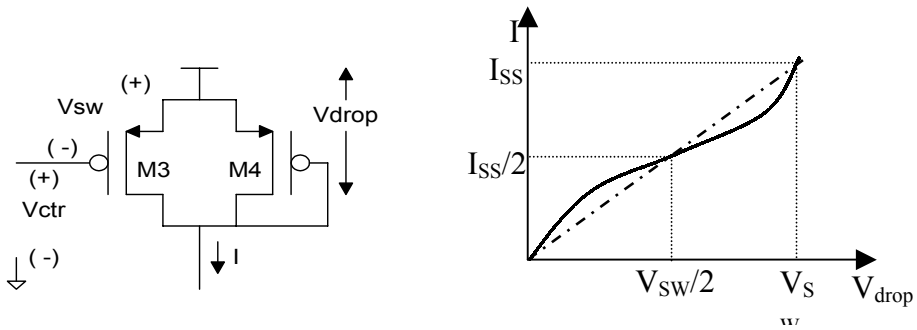


Figure 4.12 Symmetric load and its I-V characteristics

The effective load resistance and the frequency of oscillation are determined following the work of Maneatis [15]. It can be shown that the effective resistance of a symmetric load is directly proportional to the small signal resistance at the ends of the swing range which is reciprocal of the transconductance g_{m1} for one of the two equally sized PMOS devices when biased at V_{sw} [15]. In this case, the two equally sized PMOS devices are both biased at V_{sw} and each sources half of the tail current ($I_{SS}/2$). The drain current for one of the two equally sized devices biased at V_{drop} is given by,

$$\frac{I_{SS}}{2} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_1 \left[V_{drop} - V_{TP}\right]^2 \qquad \text{....(Eq. 4.46)}$$

The resistance of the symmetric load is found to be,

$$R_L = \frac{1}{g_{m1}} = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \left[V_{sw} - V_{TP}\right]} \qquad \text{....(Eq. 4.47)}$$

Therefore, the delay per stage is given by,

$$T_d = \frac{C_L}{\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \left[V_{dd} - V_{ctr} - V_{TP}\right]} \qquad \text{....(Eq.4.48)}$$

Now, substituting Eq. 4.48 into Eq. 4.3, we get the frequency of oscillation of symmetric load,

$$f_{osc} = \frac{\mu_p C_{ox}}{6C_L}\left(\frac{W}{L}\right)_1 \left[V_{dd} - V_{ctr} - V_{TP}\right] \quad \text{....(Eq. 4.49)}$$

4.6.1 Timing Jitter and Phase Noise in Symmetric Load

Noise analysis for the symmetric load ring VCO is very similar to that of ring VCO with triode load. The same expressions (Eq. 4.41 and Eq. 4.45) for timing jitter and phase noise are found, but the value of the noise contribution factor ξ^2 is changed.

At equilibrium, $\frac{I_{SS}}{2} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_5 \left(V_{GS5} - V_{TN}\right)^2$ and $g_{m5} = \mu_n C_{ox}\left(\frac{W}{L}\right)_5 \left(V_{GS5} - V_{TN}\right)$.

The expression for timing jitter (Eq. 4.41) can be rewritten as,

$$\overline{\Delta t_{VCO}}^2 = T_{osc}\frac{kT}{2I_{SS}}\xi^2\left(\frac{a_v}{V_{GS5} - V_{TN}}\right)$$

or,
$$\overline{\Delta t_{VCO}}^2 = T_{osc}\frac{kT}{2\left(I_{SS}\right)^{3/2}}\xi^2\left(\frac{\mu_n C_{ox}\left(\frac{W}{L}\right)_5}{\sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_1}}\right) \quad \text{....(Eq. 4.50)}$$

The expression for phase noise (Eq. 4.45) can be rewritten as,

$$S_{VCO}(f_m) = \left(\frac{f_{osc}}{f_m}\right)^2 \frac{kT}{2I_{SS}}\xi^2\left(\frac{a_v}{V_{GS5} - V_{TN}}\right)$$

or,
$$S_{VCO}(f_m) = \left(\frac{f_{osc}}{f_m}\right)^2 \frac{kT}{2(I_{SS})^{3/2}}\xi^2\left(\frac{\mu_n C_{ox}\left(\frac{W}{L}\right)_5}{\sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_1}}\right) \quad \text{....(Eq. 4.51)}$$

To evaluate the noise contribution factor ξ^2, let us consider the noise model for the symmetric load delay cell shown in Figure 4.13. M2, M3, M5 and M6 all are in saturation, the output noise voltages for these transistors,

$$\overline{V_{n2,3}}^2 = \frac{kT}{C_L}\gamma_1 \quad \text{....(Eq. 4.52)}$$

$$\overline{V_{n5,6}}^2 = \frac{kT}{C_L}\gamma_1 g_{m5} R_L = \frac{kT}{C_L}\gamma_1 a_v \quad \text{....(Eq. 4.53)}$$

For PMOS loads M1/M4, three conditions should be considered. In equilibrium, the transistor is in the ohmic region depending on the value of drain to source bias. So, γ is determined by the drain to source bias. So, the noise current is given by Eq. 4.18,

$$\overline{i_n}^2 = 4kT\gamma_2 g_{m1}\Delta f$$

When $|V_{DS}| \to V_{sw}$ and $V_{out} = V_{ctr}$, the transistors are in saturation.

$$\overline{i_n}^2 = 4kT\gamma_1 g_{dso1}\Delta f \quad \text{....(Eq. 4.54)}$$

where, g_{dso1} is the transconductance with zero drain-to-source bias. If the load resistance with zero drain-to-source bias is R_{Lo}, then $R_{Lo} = \frac{1}{g_{dso1}}$.

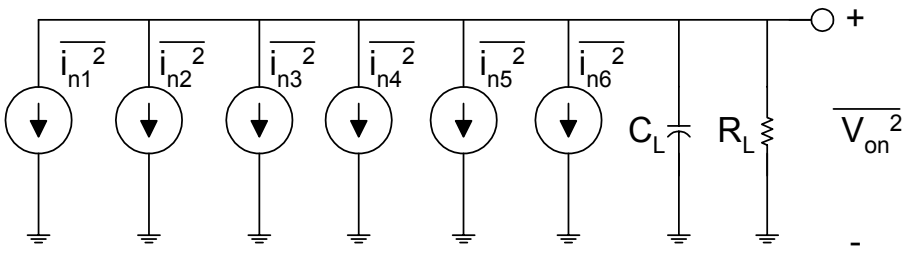


Figure 4.13 AC noise model for the delay cell with symmetric loads

When $|V_{DS}| \to 0$, the transistors are in deep triode region, and

$$\overline{i_n}^2 = 4kT\gamma_3 g_{dso1}\Delta f \quad \text{....(Eq. 4.55)}$$

Here, γ_3 will be very close to '1' as transistor M1/M4 will be in deep triode region.

The average noise current density is given by,

$$\overline{i_{n1,4}}^2 = \frac{4}{3}kT\left\{\gamma_1 g_{m1} + (\gamma_2 + \gamma_3) g_{dso1}\right\}\Delta f \quad \text{....(Eq. 4.56)}$$

Finally, output noise voltage for M1/M4,

$$\overline{V_{n1,4}}^2 = \int_0^\infty \frac{4}{3}kT\left[\gamma_1 g_{m1}\left|\frac{R_L}{1+j2\pi fR_LC_L}\right|^2 + (\gamma_2+\gamma_3) g_{dso1}\left|\frac{R_{Lo}}{1+j2\pi fR_{Lo}C_L}\right|^2\right]df$$

$$= \frac{4}{3}kT\left[\gamma_1 g_{m1}R_L + (\gamma_2+\gamma_3) g_{dso1}R_{Lo}\right]$$

$$= \frac{kT}{C_L}\frac{\gamma_1+\gamma_2+\gamma_3}{3} \quad \text{....(Eq. 4.57)}$$

Combining all these results of (Eq. 4.52), (Eq. 4.53) and (Eq. 4.57), the total output voltage noise is given by,

$$\overline{V_{on}}^2 = \frac{kT}{C_L}\left[2\left(\frac{4}{3}+A_v\right)\gamma_1 + \frac{2}{3}(\gamma_2+\gamma_3)\right] \quad \text{....(Eq. 4.58)}$$

So, the noise contribution factor for symmetric load delay cell is,

$$\xi^2 = 2\left(\frac{4}{3}+A_v\right)\gamma_1 + \frac{2}{3}(\gamma_2+\gamma_3) \quad \text{....(Eq. 4.59)}$$

4.7 Simulated Noise

Three ring-oscillators are designed and simulated in *TSMC 0.25μm* process for noise performance at desired frequency of oscillation (*1.5552 GHz*) and for same output swing. The first two oscillators (Osc-1 and Osc-2) are the oscillators with triode loads, but they have different tail currents and power consumptions to evaluate the noise performance improvement for increased power consumption. The last oscillator (Osc-3) is the VCO with symmetric load elements. Table 4.1 shows the design parameters used for these three oscillators. All of the oscillators approximately provide the same output swing of *0.8 volts* at the desired frequency of oscillation (*1.5552 GHz*). Figure 4.14 compares the phase noise plots for Osc-1, Osc-2 and Osc-3. The summery of phase noise result of these three oscillators is given in Table 4.2.

From the phase noise plots (in figure 4.14), it is evident that the Osc-2 has lower noise level than the Osc-1 since the tail current is increased in the delay stages. The rate of improvement in phase noise is found approximately to be *2.19dB* per *100μA* increase in the tail current. From Eq. 4.45 and Eq. 4.51, it can be shown that for a particular frequency of oscillation at a particular offset frequency, the phase noise in dBc/Hz,

$$S_{VCO}(f_m)\big|_{dB} \approx 20\log(const) - 15\log(I_{SS}) \qquad \text{.....(Eq. 4.60)}$$

Using this equation, the noise improvement is found to be *2.21 dB* per *100μA* increase in tail current.

Table 4.1 Oscillators' design parameters

Oscillator	Type of Load Elements (LE)	Aspect ratio of LE, $(W/L)_1$	Aspect ratio of diff pair, $(W/L)_5$	Gain a_v	Tail Current I_{SS}	Power Consumed by VCO	Frequency of Oscill., f_{osc}
Osc-1	Triode	$\frac{1.2\mu}{0.3\mu}$	$\frac{6.3\mu}{0.3\mu}$	*≈3.6*	*248 μA*	*3.67 mW*	*1.5552 GHz*
Osc-2	Triode	$\frac{1.65\mu}{0.3\mu}$	$\frac{9.6\mu}{0.3\mu}$	*≈3.6*	*372 μA*	*5.5 mW*	*1.5552 GHz*
Osc-3	Symmetric	$\frac{1.35\mu}{0.3\mu}$	$\frac{5.4\mu}{0.3\mu}$	*≈3.4*	*247 μA*	*3.65 mW*	*1.5552 GHz*

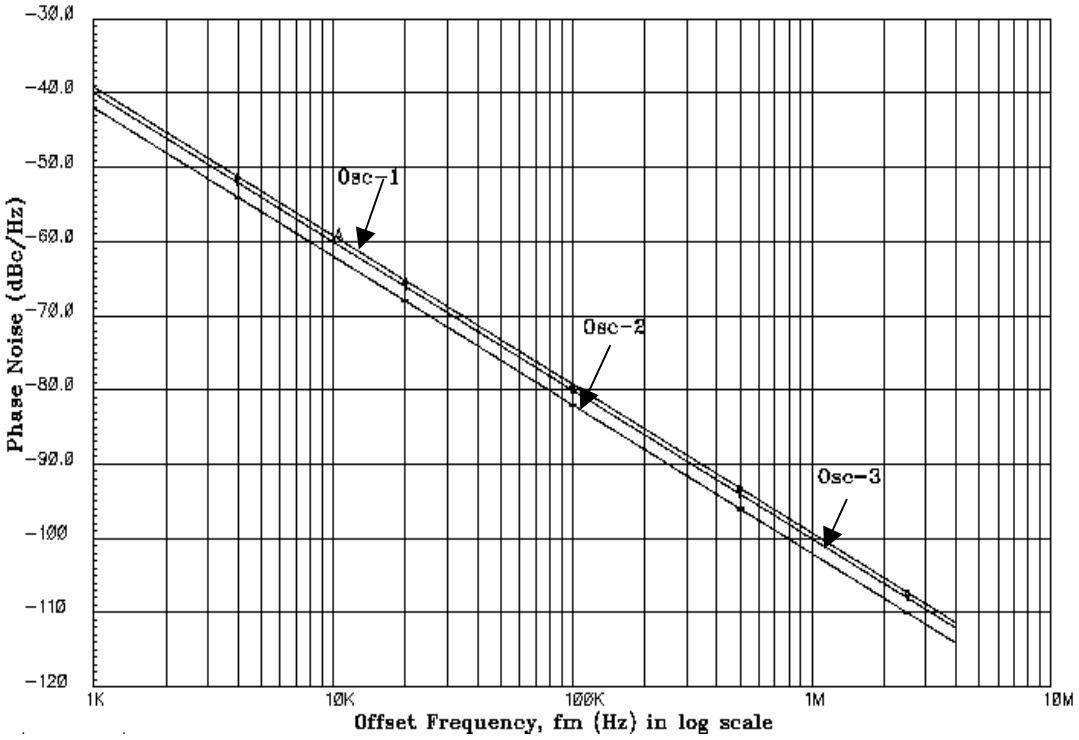


Figure 4.14 Phase noise plots for Osc-1, Osc-2 and Osc-3 at oscillation frequency of *1.5552 GHz*

Table 4.2 Phase noise vs. offset frequency for Osc-1, Osc-2 and Osc-3 at 1.5552 GHz oscillation frequency

Oscillator	@ 100 kHz offset (in dBc/Hz)	@ 1.728 MHz offset (in dBc/Hz)	@ 3.456 MHz offset (in dBc/Hz)
Osc-1	-79.2	-104.1	-110.3
Osc-2	-82.0	-106.8	-112.9
Osc-3	-80.1	-104.9	-110.9

Osc-3 needs almost the same tail current and consumes the same amount of power as Osc-1, but the same output swing is found with the lower gain (a_v). This leads the conclusion that the symmetric load ring VCO (Osc-3) is less noisy than the triode load ring oscillator (Osc-1).

Table 4.3 summarizes the phase noise calculated from empirical noise models (Eq. 4.45 and Eq. 4.51). Phase noise derived from the empirical models deviates from that of the simulation results and the lower phase noise is observed from the empirical model. These deviations are caused by the following reasons,

1) The analytical model is derived using simplified analysis neglecting the higher order non-linear effects of the delay stages. These higher orders non-linear affects influence the noise behavior of a ring VCO.
2) The value of noise contribution factor ξ^2 is not predicted correctly. Most of the cases, ξ^2 is determined from the experimental data of a fabricated ring VCO.

Table 4.3 Phase noise vs. offset frequency for Osc-1, Osc-2 and Osc-3 derived from the empirical noise model

Oscillator	@ 100 kHz offset (in dBc/Hz)	@ 1.728 MHz offset (in dBc/Hz)	@ 3.456 MHz offset (in dBc/Hz)
Osc-1	-83.5	-108.3	-114.3
Osc-2	-85.4	-110.2	-116.2
Osc-3	-84.0	-108.7	-114.8

The ring oscillator with triode load for 1.5552 GHz center frequency of oscillation is reported by Weigandt [16]. The measured phase noise for 1.0 volt output swing with the tail current of 400μA, the power supply of 3.3 volts and the power consumption of 5.3mW is shown in Table 4.4. The measured phase noise is also compared with simulated noise for proposed oscillator Osc-1 in Table 4.4.

Table 4.4 Measured phase noise by Weigandt [16] and simulated phase noise for Osc-1

	@ 1.728 MHz offset (in dBc/Hz)	@ 3.456 MHz offset (in dBc/Hz)
Measured noise for 1.0 volt output swing	-107.5	-113.3
Simulated noise for Osc-1 for 0.8 volt output swing	-104.1	-110.3
Calculated noise for Osc-1 for 0.8 volt output swing	-108.3	-114.3

Chapter 5

Charge Pump PLL, Loop-Bandwidth and Noise Performance

5.1 Introduction

The phase/frequency detector, the loop filter and the frequency divider are important in realizing a high performance frequency synthesizer. The noise from the PFD and frequency divider is multiplied by the divider ratio at the output of the PLL. When a wideband PLL is used, the divider ratio may be reduced. However, because the loop-bandwidth is very wide, noise is not suppressed until the frequency is above the loop-bandwidth, which is usually above the frequency of interest. Careful design of the loop filter is required to maintain good spectral purity at frequencies around the loop-bandwidth. In this chapter, the phase frequency detector with a charge pump and a loop filter will be discussed.

PLL loop dynamics are discussed and the relationship between the PLL loop-bandwidth and the different circuit parameters is established. The expressions for the open loop and the close loop transfer function, and the loop-bandwidth of the PLL are determined using the help of work in [15, 25, 26, 27]. The effect of loop-bandwidth on noise performance at the PLL output due to the input and the VCO phase noise are explained quantitatively.

Finally, the optimized loop-bandwidth is determined by iterative process in order to minimize the effects of the input and the VCO phase noise at the PLL output signal.

5.2 Phase/Frequency Detector

A phase/frequency detector (PFD) detects both the phase and the frequency differences between the reference clock and the input clock signals. Figure 5.1 shows schematic of a phase/frequency detector. In this PFD, conceptually two positive edge triggered delay flip-flops (DFF) with logic high in 'D' input are used to connect their outputs to the inputs of a 'AND' gate. The reference clock and the clock input (from the frequency divider) trigger the two flip-flops. If outputs of both DFFs become high, 'AND' gate resets both the outputs of DFFs to zero. So, if the frequency of the input clock (Clk-in) is greater than that of the reference clock (Ref-clk), then the PFD produces positive pulses at 'Up' while 'Down' remains zero. For $\omega_{clk\text{-}in}<\omega_{ref\text{-}clk}$, the positive pulses appear at 'Down' while 'Up'=0. For $\omega_{clk\text{-}in}=\omega_{ref\text{-}clk}$, the circuits generate pulses at either 'Up' or 'Down' with a width equal to the phase difference between the two inputs.

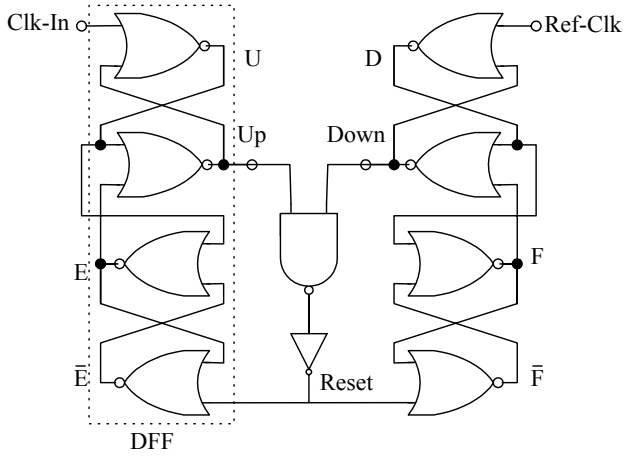


Figure 5.1 Phase frequency detector

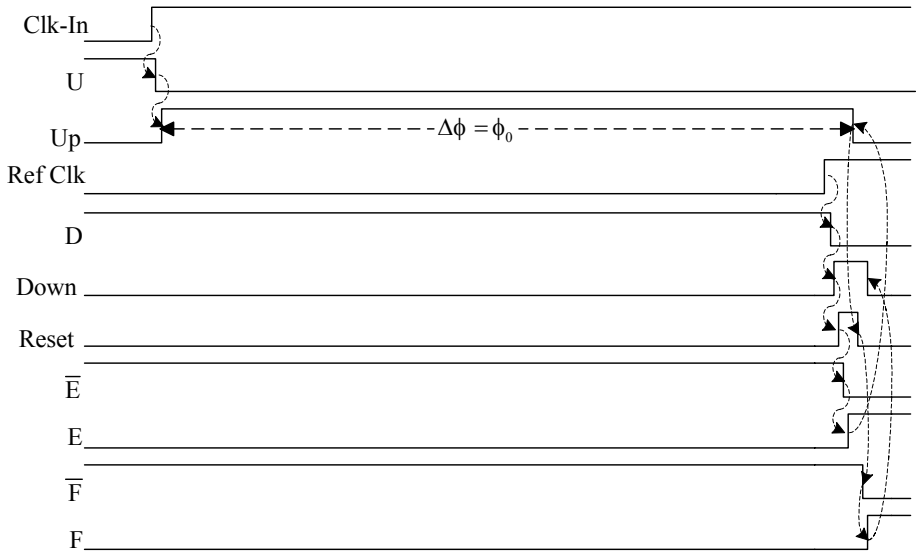


Figure 5.2 Timing diagram of the PFD

The timing diagram of the PFD is shown in Figure 5.2 where the input clock (Clk-in) leads the reference clock (Ref-Clk). So, the PFD produces positive pulses at 'Up' and the width of the pulses is proportional to the phase difference ($\Delta\phi = \phi_0$) between the two input clock signals.

5.3 Charge Pump and Loop Filter

A charge pump (CP) with a loop filter converts the pulse from the output of PFD into an equivalent average control voltage. A simple implementation of a charge pump based on the current steering concept is shown in Figure 5.3. The pass transistors M2 and M4 are used to steer the current one-way in the charge pump by the '$\overline{Up}$' and '*Down*' signals from the phase/frequency detector. These two-switched currents drive capacitors C_1 and C_2. If $\omega_{clk\text{-}in} > \omega_{ref\text{-}clk}$ or $\omega_{clk\text{-}in} = \omega_{ref\text{-}clk}$, and the input clock leads the reference clock, then positive charge accumulates on capacitors C_1 and C_2 steadily, yielding an infinite DC gain for the

PFD. Similarly, if pulses appear on 'Down', I_{ch} removes charges from capacitors C_1 and C_2 on every phase comparison, driving V_{ctr} towards -∝. Again, with 'Up'='Down'=0, V_{ctr} remains constant.

The transistor M1 and M3 minimizes leakage currents through the transistor M2 and M4 when either M2 or M4 is 'OFF'. The transistor pairs M5/M6 and M7/M8 are used as complementary pass gates that produce the same delay as the inverters. Without the complementary pass gates, due to delay mismatch between '$\overline{Up}$' and '*Down*' signals, there is a 'dead time zone' in which one of the pass transistors conducts even if the loop is locked i.e. the phase difference is zero. This disturbs the oscillator control voltage periodically even if the loop is locked. These complementary pass gates minimize the delay mismatches between '$\overline{Up}$' and '*Down*' signals, and between '*Up*' and '$\overline{Down}$' signals.

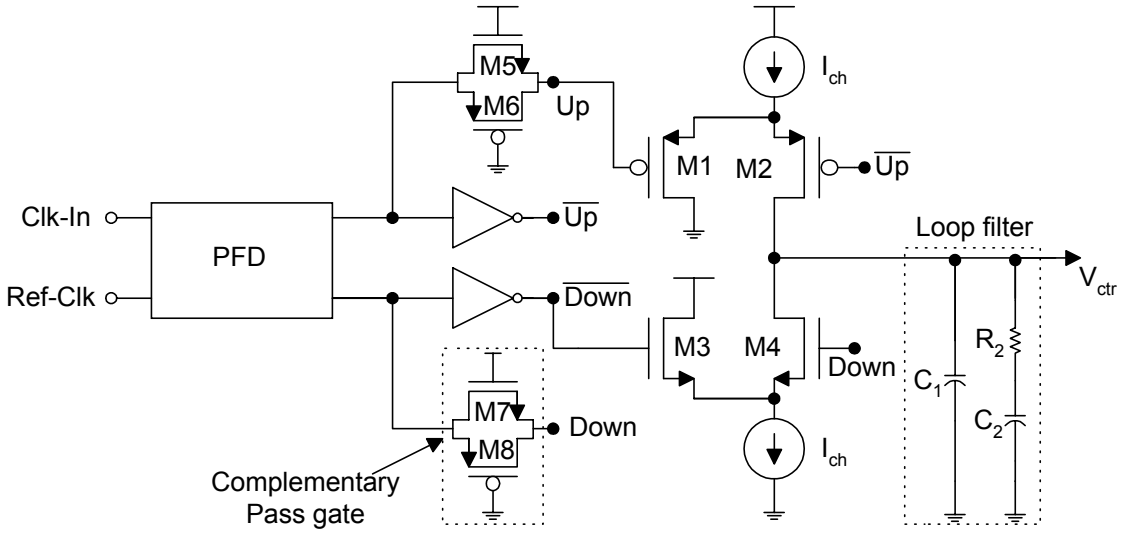


Figure 5.3 Current steering charge pump with the PFD and the loop filter

In this work, a simple RC low-pass filter is used. In Figure 5.3, R_2 and C_2 provide the filter action. R_2 provides a 'zero' in the loop transfer function; it usually helps to increase the stability of the whole system. Since the charge pump drives the series combination of R_2 and C_2, each time a current is injected into the loop filters (LF), the control voltage experiences a large jump. Even in the locked condition, the slight mismatches between the up and down current and the charge injection, the clock feed-through of the pass transistors M2 and M4 introduce voltage jumps in V_{ctr}. The resulting ripple severely disturbs the VCO, corrupting the output phase. To relax this issue, a second capacitor (C_1) is usually added to suppress the initial step.

5.3.1 Transfer Function of PFD/CP/LF Combination

Let us assume the PFD/CP/LF combination has linear relationship between its inputs and outputs. Figure 5.4 shows the step response of the PFD/CP/LF combination. If the input clock period is T_{in}, as shown in Figure 5.4, we begin with a zero phase difference and, at t=0, step the phase of Ref-clk by ϕ_0, i.e., $\Delta\phi = \phi_0 u(t)$. As a result, 'Up' or 'Down' continues to produce pulses that are $\frac{\phi_0 T_{in}}{(2\pi)}$ seconds wide, raising the output voltage by $\left(\frac{I_{ch}}{C_{eq}}\right)\frac{\phi_0 T_{in}}{2\pi}$ [2, 25] if we neglect the effect of the narrow reset pulses that appear in the other output. The effective equivalent capacitance can be calculated by,

$$sC_{eq} = \frac{1}{\frac{1}{sC_1}\left\|\left(R_2 + \frac{1}{sC_2}\right)\right.} \qquad \text{....(Eq. 5.1)}$$

Approximated as a ramp, V_{ctr} thus exhibits a slop of $\left(\frac{I_{ch}}{C_{eq}}\right)\frac{\phi_0}{2\pi}$ and can be expressed as,

$$V_{ctr}(t) = \frac{I_{ch}}{2\pi C_{eq}} t.\phi_0 u(t) \quad \text{....(Eq. 5.2)}$$

The impulse response is therefore given by,

$$h(t) = \frac{I_{ch}}{2\pi C_{eq}} u(t) \quad \text{....(Eq. 5.3)}$$

yielding the transfer function,

$$\frac{V_{ctr}}{\Delta\phi}(s) = \frac{I_{ch}}{2\pi C_{eq}} . \frac{1}{s}$$

so, $$\frac{V_{ctr}}{\Delta\phi}(s) = \frac{I_{ch}}{2\pi} \frac{1 + sR_2C_2}{s(C_1 + C_2 + sR_2C_1C_2)} \quad \text{....(Eq. 5.4a)}$$

or, $$\frac{V_{ctr}}{\Delta\phi}(s) = \frac{I_{ch}}{2\pi (C_1 + C_2)} \frac{1 + sR_2C_2}{s\left(1 + s\frac{R_2C_2}{C_1 + C_2}\right)} \quad \text{....(Eq. 5.4b)}$$

Thus, the PFD/CP/LF combination contains two poles and a zero.

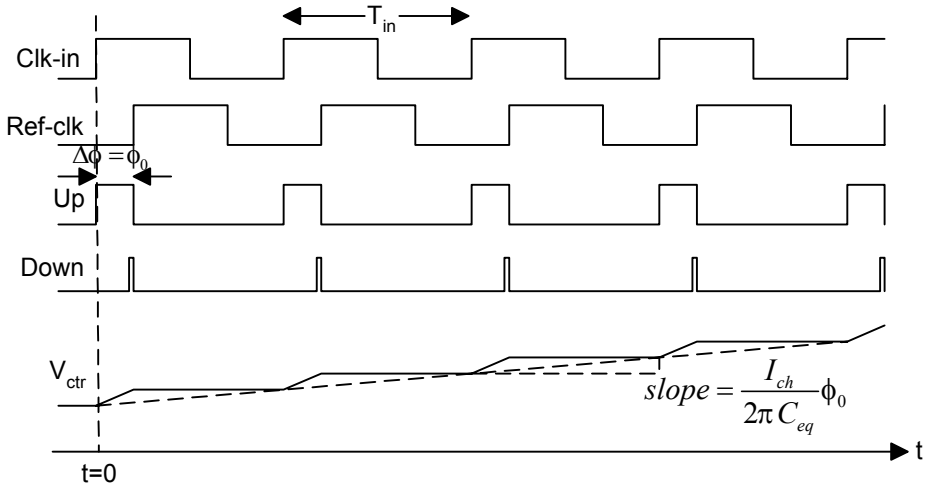


Figure 5.4 Step response of the PFD/CP/LF combinations

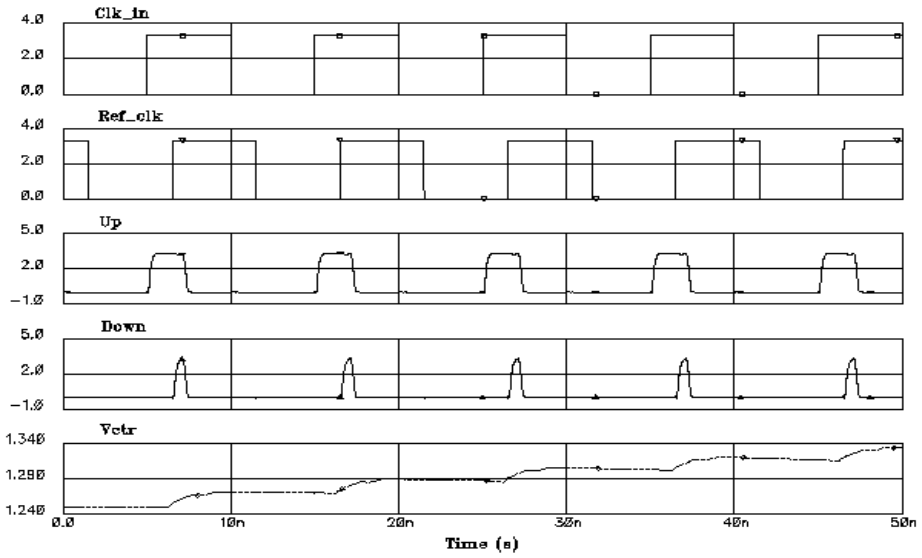


Figure 5.5 Simulation results of the designed the PFD/CP/LF combination

5.3.2 Simulation Results of PFD/CP/LF Combination

A combination of PFD/CP/LF is implemented and simulated in *TSMC 0.25μm* process. The simulation results of this combination are shown in Figure 5.5. For this case, the values of the charge pump current, the resistor, and the capacitors are chosen as I_{ch}*=45μA,* C_1*=5.5pF,* R_2*=20pF and* R_2*=18K*. The clock input leads the reference clock, so the positive pulses appears at 'Up'. The capacitors are charged and the control voltage starts increasing from its initial value. There are discontinuities when the control voltage rises. These discontinuities are caused by the narrow reset pulses that appears at 'Down'.

5.4 PLL Dynamics and Loop-Bandwidth

The linear model of a typical phase-locked loop is redrawn from Chapter 2 and shown in Figure 5.6. Using Eq. 2.2 and Eq. 5.4, we can derive the open loop gain of the PLL with simple R-C filter (shown in Figure 5.3). So, the open loop transfer function is,

$$G(s) = \frac{K_{VCO} I_{ch}}{2\pi N(C_1 + C_2)} \frac{1 + sR_2C_2}{s^2\left(1 + s\dfrac{R_2C_1C_2}{C_1 + C_2}\right)} \quad \text{....(Eq. 5.5)}$$

Close loop gain is found to be,

$$T(s) = \frac{G(s)}{1 + G(s)}$$

or, $$T(s) = \frac{1 + sR_2C_2}{1 + sR_2C_2 + s^2 \dfrac{2\pi N}{K_{VCO} I_{ch}}\left(C_1 + C_2 + sR_2C_1C_2\right)} \quad \text{....(Eq. 5.6)}$$

Here we have three poles and one zero. First two poles are at the origin and third pole is at,

$$p = -\frac{C_1 + C_2}{R_2C_1C_2}$$

The zero is at,

$$z = -\frac{1}{R_2C_2}$$

Let $$k = \frac{K_{VCO} I_{ch}}{2\pi N(C_1 + C_2)} \quad \text{....(Eq. 5.7)}$$

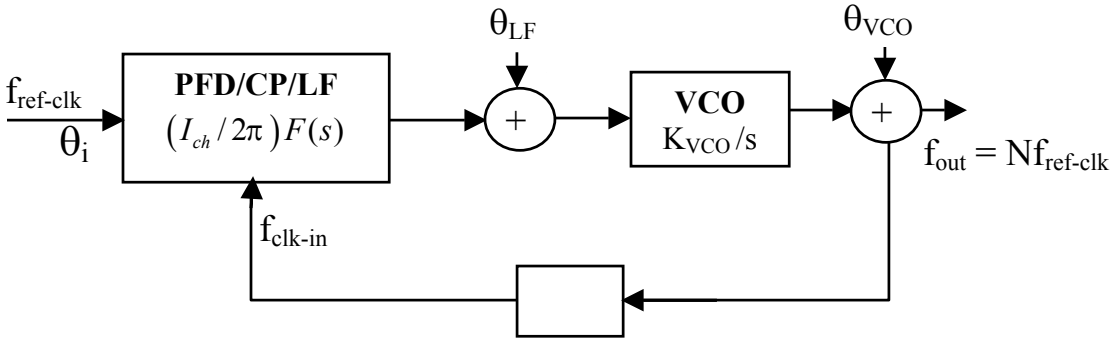


Figure 5.6 Phase-locked loop linear model

So, the Eq. 5.5 can be written as,

$$G(s) = k\frac{1+s/z}{s^2(1+s/p)} \quad \text{....(Eq. 5.8)}$$

Usually, $C_1 << C_2$, so the location of third pole is at, $p \approx {}^{1}\!/_{R_2C_1}$. The location of third pole is set far from zero location and the loop-bandwidth. So, for frequency response in the range of the loop-bandwidth, the effect of the third pole is negligible. Thus, the frequency response of this system can be considered as that of a second order linear system in the frequency range of the loop-bandwidth.

So, Eq. 5.5 and Eq. 5.6 can be written as,

$$G(s) = k\frac{1+sR_2C_2}{s^2} \quad \text{....(Eq. 5.8)}$$

and $$T(s) = \frac{1+sR_2C_2}{\frac{s^2}{k}+sR_2C_2+1} \quad \text{....(Eq. 5.9)}$$

Eq. 5.8 can be expressed as,

$$T(s) = \frac{1+2.\left(\frac{s}{\omega_n}\right).\zeta}{\left(\frac{s}{\omega_n}\right)^2+2.\left(\frac{s}{\omega_n}\right).\zeta+1} \quad \text{....(Eq. 5.10)}$$

where, ω_n is called 'angular natural frequency of oscillation' and ζ is the damping factor and we get,

$$\omega_n = \sqrt{k} = \sqrt{\frac{K_{VCO}I_{ch}}{2\pi N(C_1+C_2)}} \quad \text{....(Eq. 5.11)}$$

and $$\xi = \frac{R_2C_2}{2}\sqrt{\frac{K_{VCO}I_{ch}}{2\pi N(C_1+C_2)}} \quad \text{....(Eq. 5.12)}$$

5.4.1 Loop-Bandwidth

From Eq. 2.5 from Chapter 2, we get,

$$\left|G(j\omega_{PLL})\right| = 1$$

Inserting Eq. 5.8 in the above equation, we get,

$$\left| \omega_n \frac{1 + j2\left(\frac{\omega_{PLL}}{\omega_n}\right)\zeta}{\left(j\omega_{PLL}\right)^2} \right| = 1 \qquad \text{….(Eq. 5.13a)}$$

or, $\omega_{PLL}^4 = 4\omega_{PLL}^2(\omega_n\zeta)^2 + \omega_n^4$ ….(Eq. 5.13b)

Solving this forth order equation,

$$\omega_{PLL} = \omega_n\sqrt{2\zeta^2 + \sqrt{1+4\zeta^4}}, \quad \text{for } \zeta<1 \qquad \text{….(Eq. 5.14)}$$

From the analysis, it is found that, to increase the loop-bandwidth of the PLL we need to increase the natural frequency of oscillation or damping factor or both. Increase in damping factor decreases the ringing. In view of process and temperature variation of the loop parameters, ζ is usually chosen to be greater than $\sqrt{2}/2$ or even *1* to avoid excessive ringing [25]. Increasing both the frequency of oscillation and the damping factor makes the system settle down fast. In that case if the system has a programmable divider, the synthesizer will be able to switch the frequency fast and settle down in steady state very quickly. So for the systems that need fast frequency switching a wide loop-bandwidth is desired.

5.4.2 Loop-Bandwidth from Simulation

From the Eq. 5.11, Eq. 5.12 and Eq. 5.14, the loop-bandwidth can be increased by altering the following factors,

1) Increasing the value of $K_{VCO}.I_{ch}$. In Chapter 4, a ring VCO is designed with high VCO gain (K_{VCO}) and the VCO gain is found to be *1.08 GHz per volt*. There is a practical limit to increase both the VCO gain and the charge pump current.
2) Decreasing the diving ratio (N). Later it will be shown that smaller dividing ratio directly reduces the effect of the input noise. But the PLL for *1.5552 GHz* output frequency with too small diving ratio needs a crystal oscillator that is able to generate higher reference frequency with a low phase noise. Therefore, in this work the crystal reference frequency is chosen as *86.4MHz*. With an *86.4MHz* crystal reference frequency, the divider ratio *N* is significantly reduced to *18*.
3) The most practical way to increase the loop bandwidth is by altering the values of the R-C low-pass filter parameter. As $C_1 << C_2$, so $(C_1+C_2) \approx C_2$ and the loop BW is increased by decreasing the value of C_2, but decreasing the value of C_2 decreases the value of the damping factor that may in turn decrease the loop-bandwidth. From Eq. 2.12, we find that the damping factor can be increased by increasing the value of the resistor R_2.

In this work, two R-C low-pass filters are studied for two different loop-bandwidths. Figure 5.7 shows the open loop frequency response of the PLL system with the two LPFs. Table 5.1 shows the summary of the frequency response analysis.

Table 5.1 Summery of the frequency response.

Low-pass Filters	R-C values	Natural fre osci, ω_n (MHz)	Damping factor, ξ	Loop BW (MHz)	Phase Margin
1st LPF (LPF1)	*C_1=5pf, R_2=18 KΩ, C_2=20 pf*	*0.67*	*0.75*	*1.0*	*42.5°*
2nd LPF (LPF2)	*C_1=0.1pf, R_2=105 KΩ, C_2=0.6 pf*	*3.98*	*0.79*	*6.5*	*49.2°*

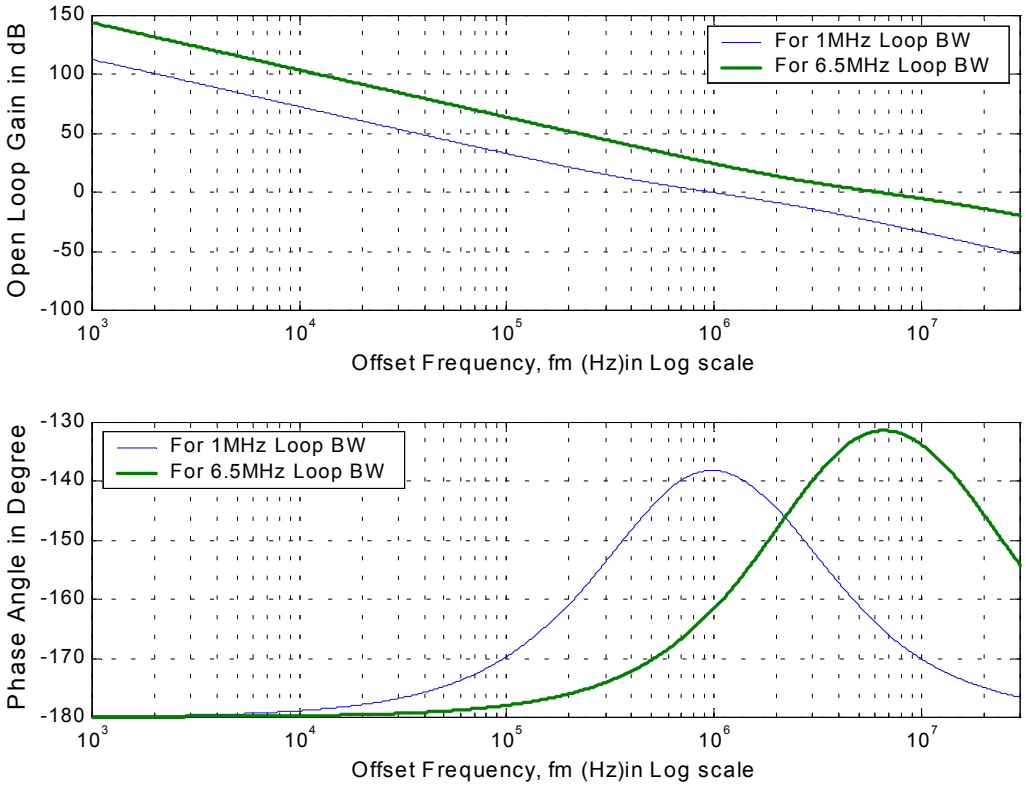


Figure 5.7 Open loop frequency response for the PLL with LPF1 and LPF2

The loop-bandwidth of PLL should be less than *1/10* of the reference frequency for the stability of the loop [5]. For this design, the loop-bandwidth of the PLL with LPF2 is chosen to be about 6.5*MHz* for maximum suppression of the VCO noise while maintaining a low noise at *1.728MHz* offset from the reference, the loop filter and the PFD.

5.5 Phase Noise Performance

The transfer function of the VCO output to the synthesizer output is given by Eq. 2.8 as,

$$\frac{\theta_o}{\theta_{VCO}}(s) = \frac{1}{1+G(s)} \qquad \text{....(Eq. 5.14)}$$

and the noise transfer function from θ_i to output,θ_o is,

$$\frac{\theta_o}{\theta_i}(s) = N\frac{G(s)}{1+G(s)} \qquad \text{....(Eq. 5.15)}$$

Substituting the value of G(s) in Eq. 5.14 we get

$$\frac{\theta_0}{Q_{VCO}}(s) = \frac{s^2}{s^2 + k(1+sR_2C_2)}$$

$$= \frac{1}{1+2\left(\frac{\omega_n}{s}\right)\zeta + \left(\frac{\omega_n}{s}\right)^2}$$

$$\left|\frac{\theta_0}{\theta_{VCO}}(\omega)\right|^2 = \left[1+2.\left(\frac{\omega_n}{\omega}\right)^2\left\{2\zeta^2-1\right\}+\left(\frac{\omega_n}{\omega}\right)^4\right]^{-1} \qquad \text{....(Eq. 5.16)}$$

The output noise due to VCO noise,

$$S_{out}(s) = \left|\frac{\theta_0}{\theta_{VCO}}(s)\right|^2 S_{VCO}(s)$$

So, output phase noise due to VCO noise at the offset frequency f_m is,

$$S_{out}(f_m) = \left| \frac{\theta_0}{\theta_{VCO}}(f_m) \right|^2 S_{VCO}(f_m) \quad \text{....(Eq. 5.17)}$$

If the natural frequency of oscillation is denoted by f_n, output phase noise due to VCO noise at f_m offset frequency in dBc/Hz

$$= \text{VCO phase noise in dBc/Hz} + 10.\log_{10} \left| \frac{\theta_0}{\theta_{VCO}}(f_m) \right|^2$$

$$= \text{VCO phase noise in dBc/Hz} - 10.\log_{10} \left[1 + 2.\left(\frac{f_n}{f_m} \right)^2 \left(2\zeta^2 - 1 \right) + \left(\frac{f_n}{f_m} \right)^4 \right]$$

....(Eq. 5.18)

So, the amount of VCO noise suppressed by the high-pass action

$$= 10.\log_{10} \left[1 + 2.\left(\frac{f_n}{f_m} \right)^2 \left(2\zeta^2 - 1 \right) + \left(\frac{f_n}{f_m} \right)^4 \right] \quad \text{....(Eq. 5.19)}$$

Figure 5.8 shows the phase noise of Osc-1 (Chapter 4) and the effect of loop-bandwidth on the PLL output phase noise due to the VCO phase noise. The phase noise of the Osc-1 and the output phase noise due to the VCO noise at different offset frequency is shown in Table 5.2. It is found that for *6.5 MHz* loop-bandwidth, the VCO phase noise is suppressed by the amount of *14.8 dBc/Hz*.

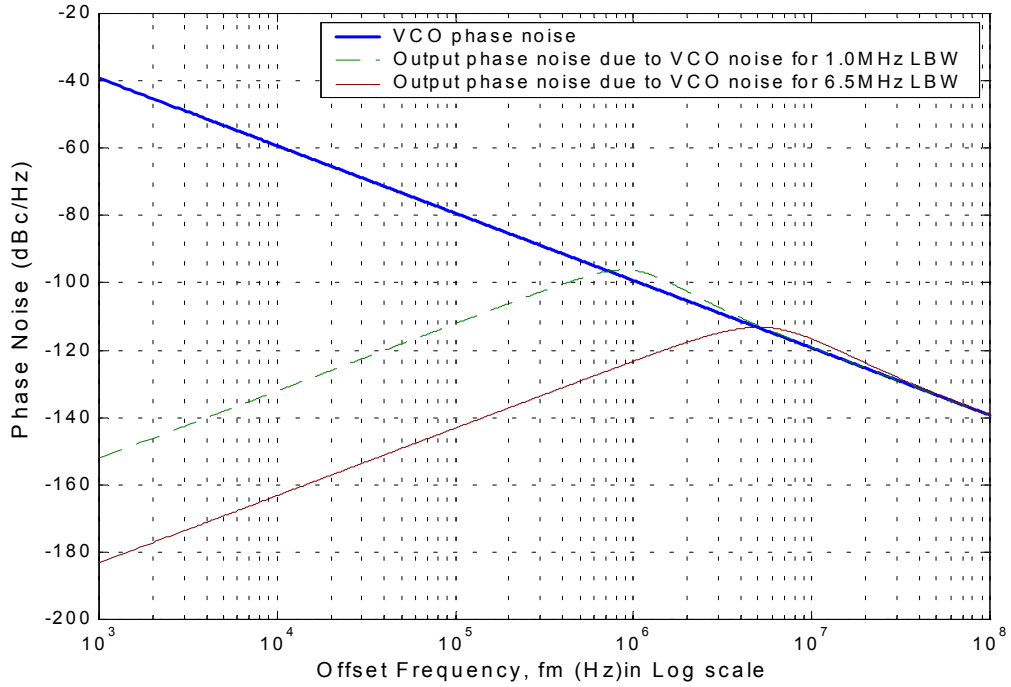


Figure 5.8 VCO phase noise and output phase noise due to VCO noise for different offset frequency

Table 5.2 VCO phase noise and phase noise at the output due to VCO noise vs. offset frequency at *1.5552 GHz* oscillation frequency

	@ 100 kHz offset	*@ 1.728 MHz* offset	*@ 3.456 MHz* offset
Phase noise of Osc-1	-79.2	-104.1	-110.3
Output phase noise due to VCO phase noise for *1.0 MHz* LBW	*-112*	*-100*	*-109.2*
Output phase noise due to VCO phase noise for *6.5 MHz* LBW	*-143*	*-118.8*	*-114.9*

The output noise due to the input noise (noise from the reference clock and the frequency divider) at f_m offset frequency in dBc/Hz (as derived from Eq 5.15),

$$= \text{Input phase noise in dBc/Hz} + 10.\log_{10}\left|\frac{N.G(f_m)}{1+G(f_m)}\right|^2$$

$$= \text{Input phase noise in dBc/Hz} + 20\log_{10} N + 20.\log_{10}\left(\frac{f_n}{f_m}\right) + 10.\log_{10}\left[4\zeta^2 + \left(\frac{f_n}{f_m}\right)^2\right]$$

$$-10.\log_{10}\left[1 + 2.\left(\frac{f_n}{f_m}\right)^2\left(2\zeta^2 - 1\right) + \left(\frac{f_n}{f_m}\right)^4\right] \quad \text{....(Eq. 5.20)}$$

So, the amount of the noise added at the output due to the input noise in dBc/Hz

$$= 20\log_{10} N + 20.\log_{10}\left(\frac{f_n}{f_m}\right) + 10.\log_{10}\left[4\zeta^2 + \left(\frac{f_n}{f_m}\right)^2\right]$$

$$-10.\log_{10}\left[1 + 2.\left(\frac{f_n}{f_m}\right)^2\left(2\zeta^2 - 1\right) + \left(\frac{f_n}{f_m}\right)^4\right] \quad \text{....(Eq. 5.21)}$$

Figure 5.9 shows the suppression or addition of the VCO phase noise (VPN) or the input phase noise (IPN) at the PLL output due to the increase in the PLL loop-bandwidth. In Figure 5.9 OPN stands for the output phase noise. For the VCO phase noise, the system acts as a high-pass filter and for the input noise the system acts as a low-pass filter. In order to implement a wide loop-bandwidth PLL, it should be ensured that the reference crystal oscillator has very good spectral purity and the dividing ratio should be as small as possible to reduce the effect of the input noise at the output.

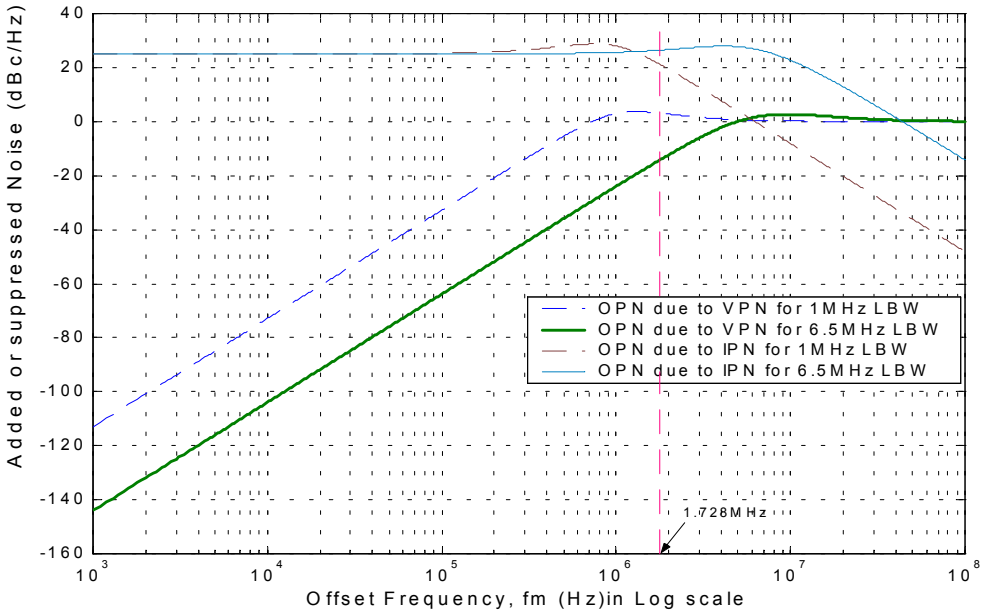


Figure 5.9 Added or suppressed noise due to input or VCO noise

Table 5.3 shows the added noise at the output due to the input phase noise and the suppressed noise at the output due to the VCO noise for the increased loop band from *1.0MHz* to *6.5MHz (@ 1.728 MHz* offset at *1.5552 GHz* frequency of oscillation).

From the previous analysis, the following advantages are found for wide loop-bandwidth-

1) Noisy oscillator can be used and the VCO phase noise can be suppressed.
2) Phase-locked loop frequency synthesizer with wide loop-bandwidth is suitable for the fast frequency scheme if a programmable divider is used.

But the main disadvantage of the PLL with wide loop-bandwidth is that it increases the effect of input noise at output. To reduce this effect, we have to use a reference crystal oscillator with extremely good spectral purity and smaller dividing ratio of the divider. But the PLL with small dividing ratio needs a higher reference frequency and it may be impractical to attain that frequency from commercially available crystal oscillator.

Table 5.3 Added or suppressed noise at the output due to VCO noise and input noise for the increased loop band from *1.0 MHz* to *6.5 MHz*

Suppressed phase noise at output due to VCO phase noise	Added phase noise at output due to input phase noise
18.3 dB	*4.3 dB*

The loop-bandwidth can be increased by increasing the VCO gain (K_{VCO}), the charge pump current or by decreasing the capacitor values (C_1 and C_2). There is practical limit to increase the VCO gain (K_{VCO}) and increasing the VCO gain decreases the frequency resolution of the VCO. Increasing the VCO gain (K_{VCO}) or decreasing the capacitor values or doing both increase the step jump of the control voltage and introduce ripple in the control voltage. This decreases the frequency resolution at the output of the PLL and even the PLL cannot be locked for bigger step in the control voltage.

5.5.1 Loop-Bandwidth Optimization

If VCO noise is the only noise source in a PLL, then a very large loop-bandwidth can potentially be used to obtain an output signal with very high spectral purity. However the reference source, usually a crystal oscillator, has some noise generated by its active circuits. The loop filter also generates noise. This noise goes through the low-pass and the band-pass filtering which is different from the VCO noise that goes through the high-pass filtering. This difference suggests that an optimal loop-bandwidth exists for a specific application. Depending on the level of the different noise sources and the location of the

frequency of interest, the optimal loop-bandwidth can be different. The goal is to find the optimal loop-bandwidth so that the total noise contributed by all noise sources is minimum at the output of the PLL at the frequency of interest.

To quantify the optimization process, the loop-bandwidth f_{PLL} can be written as a function of C_1, R_2, C_2, N, K_{VCO} and I_{ch} by using Eq. 5.14. We can choose an optimal loop-bandwidth by varying those parameters. Adequate phase margin should be designed so as to guarantee the stability of the loop. The actual optimization requires a knowledge of the noise spectrum from each individual noise source. This noise spectrum sometimes also depends on the choice of those parameters. Thus the optimization is an iterative process.

5.6 Simulation Results of the Complete System

The PLL with two different loop-bandwidths (using LPF1 and LPF2) is simulated in *TSMC 0.25μm* process by SPECTRE simulator of Cadence tools. The simulated transient response of the VCO control voltage, V_{ctr} for the PLL with loop-bandwidth of *6.5 MHz* is shown in Figure 5.10. The specifications found from the simulation result of this PLL are given below.

Reference frequency= *86.4MHz*

Dividing ratio = *18*

Loop-bandwidth= *6.5 MHz*

Phase margin = *49.2°*

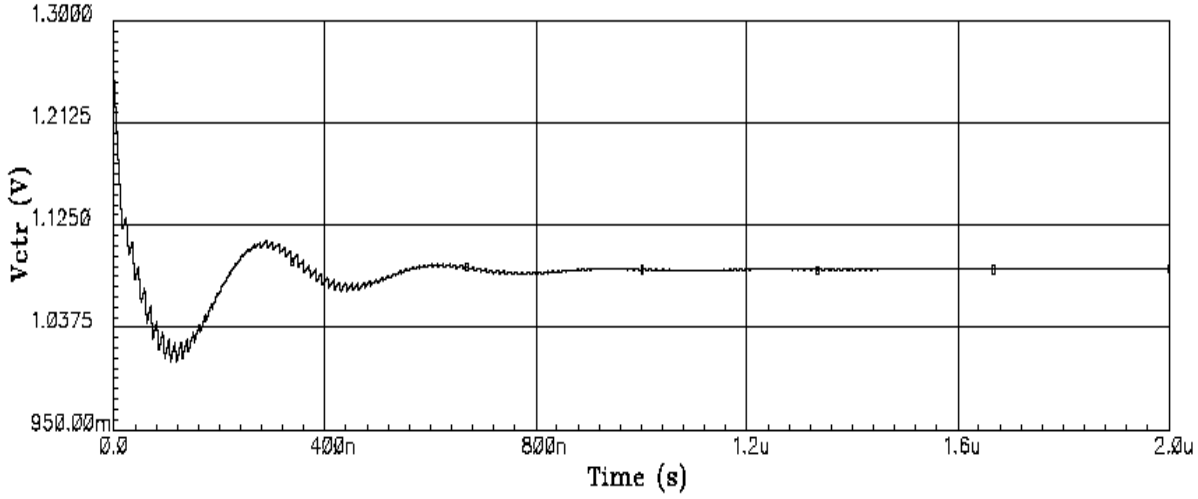


Figure 5.10 Transient simulation results for the control voltage

Damping factor = *0.79*

Natural frequency of oscillation = *3.98 MHz*

Total power consumption = *18.8 mW*

Lock time = *1.3*μ*S*

Phase noise of the VCO at *1.728 MHz = -104.1 dBc/Hz*

VCO noise suppression at *1.728 MHz= 14.7 dBc/Hz*

Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this thesis work, the architecture of a phase-locked loop (PLL) with wide loop-bandwidth for DECT application is proposed. Various design techniques to minimize the phase noise are explored. The relative advantages and the limitations of a wide loop-bandwidth PLL are discussed. The architectures of frequency dividers operating at higher frequencies are proposed.

The main points of this thesis work are:

1. Among several frequency synthesizer architectures, e.g., Direct Digital Frequency Synthesizer, narrow band PLL, fractional-N PLL, and wideband PLL, the wideband PLL is the most amenable to integration while still capable of high performance. In the proposed architecture, the noise contribution from the VCO is suppressed significantly within the loop-bandwidth. The amount of the VCO phase noise suppressed by the high-pass action of wide loop-bandwidth at the offset frequency of 1.728MHz (which equals to channel spacing) is 14.7 dB.
2. As significant amount of the phase noise can be suppressed by using wide control loop bandwidth, a noisy ring oscillator can be used for an on-chip implementation of the complete PLL.

3. The proposed phase-locked loop RF synthesizer is well suited for the application of DECT receiver because of two reasons. Firstly, this offers better economical solution for on-chip implementation of the complete PLL. Secondly, the phase noise requirements of a RF synthesizer for DECT receiver is ≤ -90 dBc/Hz. The contributed noise margin of the proposed RF synthesizer can meet this flexible phase noise performance requirement.
4. Because the noise from the VCO is suppressed in a wideband PLL architectures, other noise sources become more important in the overall synthesizer performance. Noise from the crystal oscillator reference, and phase/frequency detector become the most important contributors within the loop-bandwidth and are referred to the output enhanced in effect by the divider ratio N.
5. As the structure with current-mode logic control can be operated at higher frequencies, dividers with current-mode logic are designed to achieve high-speed performance and differential structure is chosen to reduce the common mode noise from the divider.

6.2 Future Work

1. In a PLL with wide loop-bandwidth, the phase noise from the input side cannot be suppressed significantly because of wide loop-bandwidth. The phase noise from the input side should be minimized as much as possible. The noise from the PFD and charge pump can be minimized by differential implementation. Fully differential implementation of the complete PLL path is important for better noise performance.

2. In order to remove noise from the frequency divider a low-noise buffer clocked by the VCO can be used after this frequency divider [5].
3. The VCO with body driven symmetric PMOS loads is used to optimize the output swing of the VCO for a particular desired frequency. The ring VCO with body driven symmetric loads can be realized to achieve low noise for a particular operating frequency.
4. The fabrication and analysis of the performance of this phase-locked loop (PLL) with wide loop-bandwidth would be another immediate step.

References

[1] C.H. Park and B. Kim, "A Low-Noise, 900 MHz VCO in 0.6-μm CMOS," *IEEE Journal of Solid State Circuit*, Vol. 34, No.5, pp. 586 –591, May 1999.

[2] B. Razavi, "RF Microelectronics," *Prentice Hall PTR*, Chapter 8, pp. 247 –295, 1998.

[3] T.H. Lee, "The Design of CMOS Radio Frequency Integrated Circuits," *Cambridge University Press*, Chapter 15, pp. 438 –478, 1998.

[4] J. C. Rudell, J. J. Ou, T. Cho, G. Chien, F. Brianti, J. A. Weldon and P. R. Gray, "A 1.9 GHz Wide-Band IF Double-conversion CMOS Receiver for Cordless Telephone applications," *IEEE J. of Solid-State Circuit*s, vol. 32, no. 12, pp. 2071-2088, December 1997.

[5] Li Lin, "Design Techniques for High Performance Integrated Frequency Synthesizers for Multi-standard Wireless Communication Applications," Ph.D. Dissertation, University of California, Berkeley, 2000.

[6] F. Piazza and Q. Huang, "A low power CMOS dual modulus prescaler for frequency synthesizers," *IEICE Trans. Electron.*, vol. E80-C, pp. 314-319, Feb 1997.

[7] N. Krishnapura and P.R. Kinget, "A 5.3-GHz Programmable Divider for HiPerLAN in 0.25-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1019 –1024, July 2000.

[8] B. Razavi, K.F. Lee and R.H. Yan, "Design of High Speed, Low-Power Frequency Dividers and Phase-Locked Loops in Deep Sub micron CMOS," *IEEE J. Solid-State Circuits*, vol. 30, pp. 101 –109, Feb 1995.

[9] J. Craninckx and M. S. J. Steyaert, "A 1.75-GHz/3-V dual-modulus divide-by-128/129 prescaler in 0.7μm CMOS, " *IEEE J. Solid-State Circuits,* vol. 31, pp. 890–897, July 1996.

[10] M. Mizuno, M. Yamashina, K. Furuta, H. Igura, H. Abiko, K. Okabe, A. Ono, and H. Yamada, "A GHz MOS adaptive pipeline technique using MOS current-mode logic, " *IEEE J. Solid-State Circuits,* vol. 31, pp. 784–791, June 1996.

[11] M. W. Allam, M. I. Elmasry, "Dynamic Current-mode Logic (DyCML): A New Low-Power High-Performance Logic Style, " *IEEE J. Solid-State Circuits,* vol. 36, pp. 550–558, March 2001.

[12] Ali Hajimiri, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-state Circuits*, Vol. 35, No.8, Feb. 1999.

[13] R. J. Betancourt-Zamora and T. H. Lee, "Low Phase Noise CMOS Ring Oscillator VCOs for Frequency Synthesis," *2nd International Workshop on Design of Mixed-Mode Integrated Circuits*, Guanajuato, Mexico, July 27-29, 1998, pp. 37-40.

[14] J. Maneatis and Horowitz, "Precise delay generation using coupled oscillators," *IEEE Journal of Solid-State Circuits*, Vol.28, pp.1273-1282, Dec.1993.

[15] J. Maneatis, "Low-jitter process-independent DLL and PLL-based on self-biased techniques," *IEEE Journal of Solid-State Circuits*, Vol.31, pp. 1723-1732, Nov.1996.

[16] Todd C. Weigandt, "Low-Phase-Noise, Low-Timing-Jitter Design Techniques for Delay cell based VCOs and Frequency Synthesizers," PhD Dissertation, University of California, Berkeley, 1998.

[17] Jan Craninckx, Michel S.J. Steyart, "A 1.8 GHz CMOS Low-Phase-Noise Voltage-Controlled Oscillator with Prescaler," *IEEE Journal of Solid-State Circuits*, vol. 30, No.12, pp. 1474-1482, Dec. 1995.

[18] P.R. Gray and R.G. Meyer, "Analysis and Design of Analog Integrated Circuits," Third Edition, *John Wiley & Sons*, NY, 1993.

[19] A. Abidi, R. G. Meyer, "Noise in Relaxation Oscillators", *IEEE Journal of Solid-State Circuits*, Vol. 18, No. 6, pp 794-802, Dec. 1983.

[20] D. Shaeffer, T.H. Lee, "A 1.5v, 1.5GHz CMOS Low Noise Amplifier", *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 32-33, June 1996.

[21] B. Wang, J.R. Hellums, and C.G. Sodini, "MOSFET thermal noise modeling for analog integrated circuits", *IEEE Journal of Solid State Circuits*, vol. 29, no. 7, pp. 833-835, July 1994.

[22] A. Van der Ziel, "Noise in Solid State Devices and Circuits," *John Wiley & Sons*, NY, 1986.

[23] A. Van der Ziel, "Thermal Noise in field-effect transistors," *Proc. IRE*, pp. 1808-1812, Aug. 1962.

[24] K. Y. Toh, P. K. Ko and R. G. Meyer, "An Engineering Model for Short-channel MOS devices," *IEEE Journal of Solid State Circuits*, vol. 23, no. 4, pp. 950-958, Aug. 1988.

[25] B.Razavi, "Design of Analog CMOS Integrated Circuits," *McGraw-Hall*, Chapter 14, pp. 481 – 530, 1998.

[26] "Design Technique for Charge Pump PLL's", Technical Paper, *National Semiconductor*, July 2001.

[27] Arun Mansukhani, "Phase-Locked Loop Stability Analysis", Technical Feature, *Motorola Inc*, 2000.

[28] Ken Kundert, "Modeling and Simulation of Jitter in PLL Frequency Synthesizers", Technical Paper, Cadence.

[29] David A. Johns, Ken Martin, "Analog Integrated Circuit Design," *John Wiley & Sons*, *Inc.*, 1997.

[30] Charles L. Philips, Royce D. Harbor, "Feedback Control System," *Prentice Hall*, 1996.

[31] R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout, and Simulation," *IEEE Press*, Eastern Economy Edition, December 2000.

[32] B. Razavi, "Analysis, Modeling and Simulation of Phase Noise in Monolithic Voltage-Controlled Oscillators," *IEEE Custom Integrated Circuits Conference*, 1995.

[33] "Setup and Hold Time Definition", Application Note, *Cypress Semiconductor*, 2002.

[34] Aleksander Dec, Ken Suyama, "A 1.9-GHz CMOS VCO with Micromachined Electromechanically Tunable Capacitors," *IEEE Journal of Solid State Circuits*, vol. 35, no. 8, pp. 1231-1237, Aug. 2000.

[35] Hafijur Rahman and Syed K. Islam, "Fully Differential, High-speed Current-mode Controlled Dividers Designed Using Modular Approach," 45th IEEE International Midwest Symposium on Circuits and Systems, Oklahoma, August 2002.

Appendix

Appendix A: Bias Generation Circuit and Differential-Single-Ended Converter

A.1 Current Source Bias Circuit with Half-Buffer Replica

To achieve a good static power supply noise rejection, a current source bias circuit is used. For a fixed swing over the process, temperature and power supply variation, a current source bias circuit is used. The current source bias circuit [14, 15] is shown in Figure A.1. Using half buffer replica, it achieves two functions. First, it sets the current through a NMOS current source in the delay stages in order to provide the correct load swing limits. Second, it dynamically adjusts the NMOS current source bias so that this current is held constant and highly independent of supply voltage.

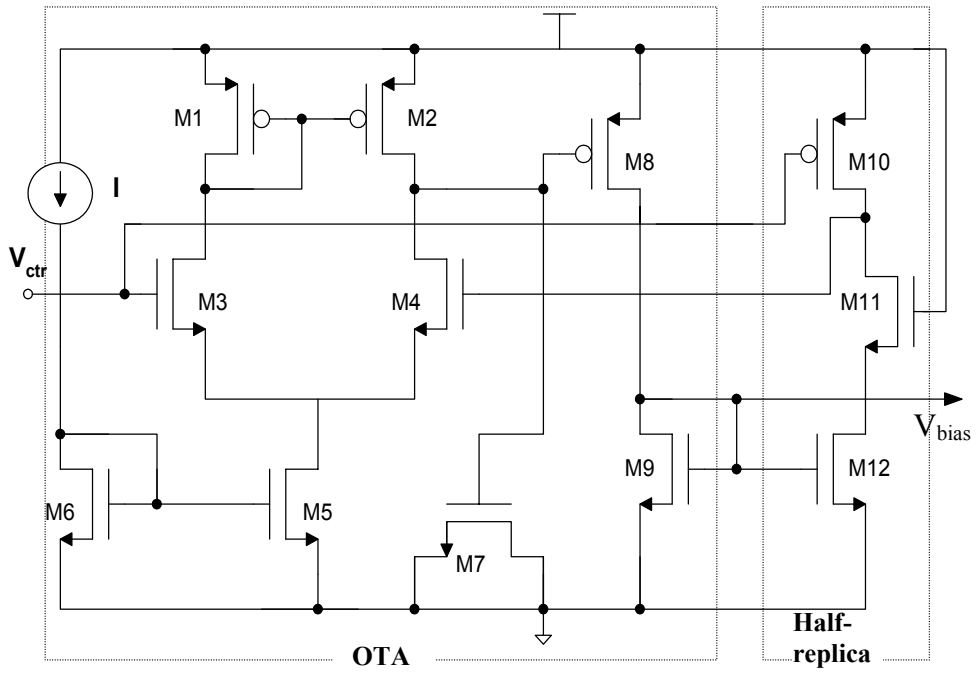


Figure A.1 Schematic of the replica-feedback current source bias circuit

This bias circuit consists a replica of half the delay stage (M10 – M12) and a simple OTA (M1 - M6 & current source 'I'), followed by a PMOS common source stage (M8 - M9). The transistor M7, configured as a MOS capacitor is connected to the highest impedance node of the circuit in order to provide adequate phase margin to the feedback network. The OTA and the half buffer replica are connected in a negative feedback fashion. The OTA adjusts the current output of the NMOS current source so that the voltage at the output of the replicated load element is equal to the control voltage, a condition required for the correct load swing limits. The net result is that the output current of the NMOS current source is established by the load element and is independent of the supply voltage. As the supply voltage changes, the drain voltage of the NMOS current source transistor (M12) changes. However, the gate bias is adjusted by the OTA to keep the output current constant, counteracting the effect of the finite output impedance. This current flowing thorough M12 is mirrored to the delay stages. This setup ensures that the tail current is set by an identical buffer of the delay stage and most importantly enables the symmetric load to constant swing from V_{dd} to ($V_{dd} - V_{sw}$). Table A.1 shows the aspect ratios for the transistors for current source bias with half buffer replica. Figure A.2 shows the magnitude and phase of the loop transmission of the feedback system. The gain bandwidth is found to be *5.65 MHz* and phase margin is *55.3*° at room temperature with *3.3* supply voltage.

Table A1 Aspect Ratios of the transistors for current source bias

M1/M2	M3/M4	M5/M6	M7	M8	M9
*4.5*μ/*1.8*μ	*3.3*μ/*1.5*μ	*9.0*μ/*1.8*μ	*21*μ/*24*μ	*7.5*μ/*1.5*μ	*9.0*μ/*1.8*μ

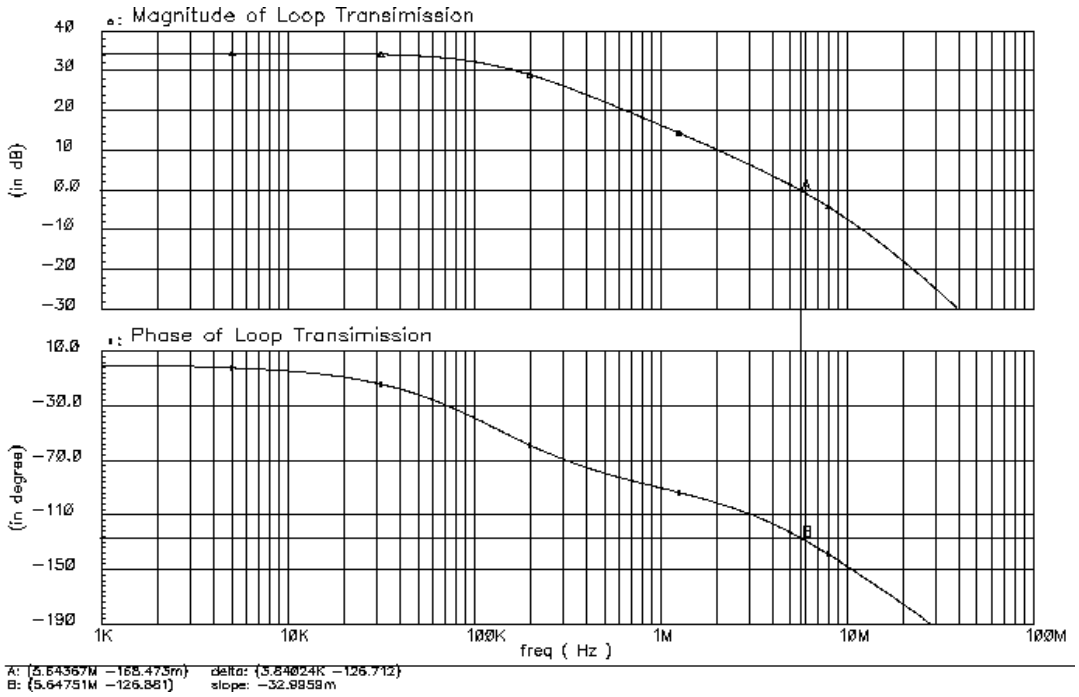


Figure A.2 The magnitude and phase of the loop transmission of the feedback system

A.2 Beta-Multiplier Referenced Self-Biasing

A β multiplier referenced biasing scheme [31] is shown in Figure A.3. The width of M5 is made K times larger than the width of M6, i.e.W_5=K.W_6 and L_5=L_6. So, β_5=K.β_6. And therefore,

$$V_{GS1} = V_{GS2} + IR \qquad \text{....(Eq. A.1)}$$

Considering the square-law relation of the drain current and gate voltage of M5 and M6, we get the current I_1 is,

$$I_1 = \frac{2}{R^2 \beta_1}\left(1 - \sqrt{\frac{1}{K}}\right)^2 \qquad \text{....(Eq. A.2)}$$

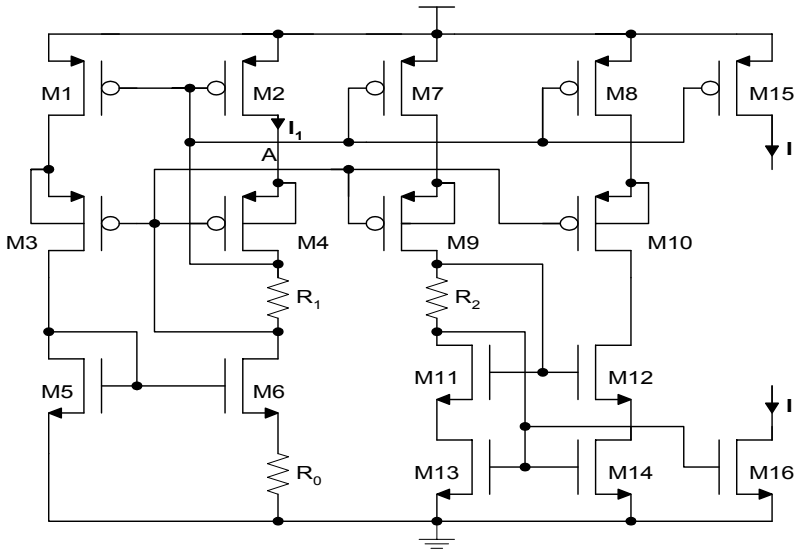


Figure A.3 Schematic of the β-multiplier referenced self-bias circuit

It can be found that the drain to source drive for the transistor M2 is,

$$V_{DS2} = I_1 R_1 + (V_{GS2} - V_{GS4}) \quad \text{....(Eq. A.3)}$$

If the same aspect ratio is used for M2 and M4, then,

$$V_{DS2} = I_1 R_1 \quad \text{....(Eq. A.4)}$$

From both Eq. A.3 and Eq. A.4, we get the V_{DS2} can be minimized by reducing R_1. So, from this circuit maximized swing is possible at node 'A' by altering the value of R_1. M7-M14 with resistance R_2 offers the option to achieve both current sourcing and sinking operation from the same circuit. This biasing circuit can directly be used in charge-pump. Table A.2 shows the aspect ratios of transistors used β-multiplier referenced self-biased circuit and the values of resistances R_1 and R_2.

Table A.2 The values of R_1, R_2 and aspect ratios of the transistors used in β-multiplier referenced self-biased circuit

Reference Current	Value of R_1, R_2	M5	M6	M1/M2	M3/M4
30μ	*R_1=34K, R_2=20.53K*	*W/L=7.8/0.9 m=8*	*W/L=7.8/0.9 m=1*	*W/L=3.0/1.2 m=4*	*W/L=1.5/0.9 m=2*
45μ	*R_1=24.85K, R_2=22.1K*	*W/L=7.8/0.9 m=8*	*W/L=7.8/0.9 m=1*	*W/L=3.0/1.2 m=4*	*W/L=1.5/0.9 m=2*

A.3 Differential-Single-Ended Converter

Figure A.4 shows a Differential-Single-ended Converter. A test input is given to illustrate test condition. When the 'test input' is high, the output becomes high. At the normal condition, the 'test input' is low. In that condition, M8 and M9 make the transistors M4 and M10 as diode connected. So the current through M10 is mirrored in the differential amplifier (M4-M5, M12-M14) by transistor M12.

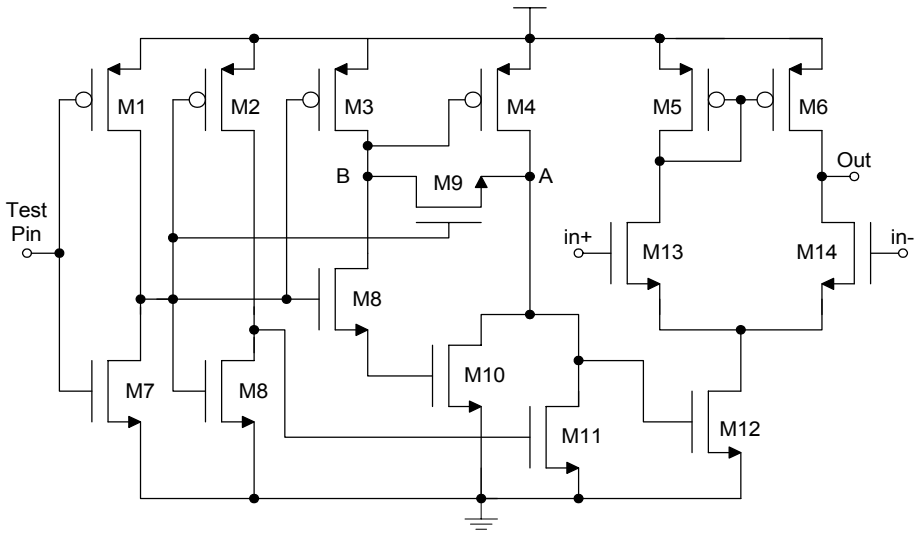


Figure A.4 Schematic of the differential-single-ended converter

Appendix B: Extracted Net list from SPECTRE Simulator

```
// Library name: Charge_pump
// Cell name: Charge_pump
// View name: schematic
subckt Charge_pump_schematic Out down downB up upB
    N22 (vdd! downB net050 0) tsmc25N w=2.1u l=300n as=1.575e-12 \
        ad=1.575e-12 ps=5.7u pd=5.7u m=1 region=sat
    N6 (net050 a4 0 0) tsmc25N w=1.8u l=1.2u as=1.35e-12 ad=1.35e-12 \
        ps=5.1u pd=5.1u m=1 region=sat
    N7 (Out down net050 0) tsmc25N w=2.1u l=300n as=1.575e-12 ad=1.575e-12 \
        ps=5.7u pd=5.7u m=1 region=sat
    N2 (a4 a3 net031 0) tsmc25N w=1.1u l=900n as=8.25e-13 ad=8.25e-13 \
        ps=3.7u pd=3.7u m=2 region=sat
    N4 (net031 a4 0 0) tsmc25N w=1.8u l=1.2u as=1.35e-12 ad=1.35e-12 \
        ps=5.1u pd=5.1u m=1 region=sat
    N3 (net027 a3 net023 0) tsmc25N w=1.1u l=900n as=8.25e-13 ad=8.25e-13 \
        ps=3.7u pd=3.7u m=2 region=sat
    N5 (net023 a4 0 0) tsmc25N w=1.8u l=1.2u as=1.35e-12 ad=1.35e-12 \
        ps=5.1u pd=5.1u m=1 region=sat
    N0 (net5 net5 0 0) tsmc25N w=900n l=7.8u as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N1 (a2 net5 net26 0) tsmc25N w=900n l=7.8u as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=8 region=sat
    P25 (0 up net081 vdd!) tsmc25P w=6u l=300n as=4.5e-12 ad=4.5e-12 \
        ps=13.5u pd=13.5u m=1 region=sat
    P10 (net081 a1 vdd! vdd!) tsmc25P w=3u l=1.2u as=2.25e-12 ad=2.25e-12 \
        ps=7.5u pd=7.5u m=4 region=sat
    P11 (Out upB net081 vdd!) tsmc25P w=6u l=300n as=4.5e-12 ad=4.5e-12 \
        ps=13.5u pd=13.5u m=1 region=sat
    P4 (net076 a1 vdd! vdd!) tsmc25P w=3u l=1.2u as=2.25e-12 ad=2.25e-12 \
        ps=7.5u pd=7.5u m=4 region=sat
    P5 (net072 a1 vdd! vdd!) tsmc25P w=3u l=1.2u as=2.25e-12 ad=2.25e-12 \
        ps=7.5u pd=7.5u m=4 region=sat
    P3 (a1 a2 net10 net10) tsmc25P w=1.5u l=900n as=1.125e-12 ad=1.125e-12 \
        ps=4.5u pd=4.5u m=2 region=sat
    P6 (a3 a2 net076 net076) tsmc25P w=1.5u l=900n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=2 region=sat
    P7 (net027 a2 net072 net072) tsmc25P w=1.5u l=900n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=4 region=sat
    P2 (net5 a2 net14 net14) tsmc25P w=1.5u l=900n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=2 region=sat
    P0 (net14 a1 vdd! vdd!) tsmc25P w=3u l=1.2u as=2.25e-12 ad=2.25e-12 \
        ps=7.5u pd=7.5u m=4 region=sat
    P1 (net10 a1 vdd! vdd!) tsmc25P w=3u l=1.2u as=2.25e-12 ad=2.25e-12 \
        ps=7.5u pd=7.5u m=4 region=sat
    R2 (a3 a4) resistor r=14.34K m=1
    R0 (net26 0) resistor r=33K m=1
    R1 (a1 a2) resistor r=22K m=1
ends Charge_pump_schematic
// End of subcircuit definition.

// Library name: PFD_digital
// Cell name: INV
// View name: schematic
subckt INV In Out
    N2 (Out In 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 ps=3.3u \
        pd=3.3u m=1 region=sat
```

```
    P2 (Out In vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 ad=1.125e-12 \
        ps=4.5u pd=4.5u m=1 region=sat
ends INV
// End of subcircuit definition.

// Library name: PFD_digital
// Cell name: AND2
// View name: schematic
subckt AND2 A B Out
    P2 (Out net028 vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P0 (net028 A vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P1 (net028 B vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    N2 (Out net028 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N1 (net028 A net16 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N0 (net16 B 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 ps=3.3u \
        pd=3.3u m=1 region=sat
ends AND2
// End of subcircuit definition.

// Library name: PFD_digital
// Cell name: NOR2
// View name: schematic
subckt NOR2 A B Out
    P1 (Out A net7 vdd!) tsmc25P w=1.35u l=300n as=1.0125e-12 \
        ad=1.0125e-12 ps=4.2u pd=4.2u m=1 region=sat
    P0 (net7 B vdd! vdd!) tsmc25P w=1.35u l=300n as=1.0125e-12 \
        ad=1.0125e-12 ps=4.2u pd=4.2u m=1 region=sat
    N0 (Out A 0 0) tsmc25N w=450.0n l=300n as=3.375e-13 ad=3.375e-13 \
        ps=2.4u pd=2.4u m=1 region=sat
    N1 (Out B 0 0) tsmc25N w=450.0n l=300n as=3.375e-13 ad=3.375e-13 \
        ps=2.4u pd=2.4u m=1 region=sat
ends NOR2
// End of subcircuit definition.

// Library name: PFD_digital
// Cell name: DFF
// View name: schematic
subckt DFF CLK F Reset
    I9 (net032 net11 F) NOR2
    I8 (CLK F net032) NOR2
    I10 (net032 net16 net11) NOR2
    I11 (net11 Reset net16) NOR2
ends DFF
// End of subcircuit definition.

// Library name: PFD_digital
// Cell name: PFD_dig
// View name: schematic
subckt PFD_dig Clk_in Ref_clk down up
    I34 (up down net019) AND2
    I31 (Clk_in up net019) DFF
    I32 (Ref_clk down net019) DFF
ends PFD_dig
// End of subcircuit definition.

// Library name: VCO
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```
// Cell name: delay_cell1
// View name: schematic
subckt delay_cell1 Bias Vctr inN inP outN outP
    M5 (outN inP net4 0) tsmc25N w=6.3u l=300n as=4.725e-12 ad=4.725e-12 \
        ps=14.1u pd=14.1u m=1 region=sat
    M6 (outP inN net4 0) tsmc25N w=6.3u l=300n as=4.725e-12 ad=4.725e-12 \
        ps=14.1u pd=14.1u m=1 region=sat
    M7 (net4 Bias 0 0) tsmc25N w=9u l=1.8u as=6.75e-12 ad=6.75e-12 \
        ps=19.5u pd=19.5u m=4 region=sat
    M2 (outN Vctr vdd! vdd!) tsmc25P w=1.2u l=300n as=9e-13 ad=9e-13 \
        ps=3.9u pd=3.9u m=1 region=sat
    M3 (outP Vctr vdd! vdd!) tsmc25P w=1.2u l=300n as=9e-13 ad=9e-13 \
        ps=3.9u pd=3.9u m=1 region=sat
ends delay_cell1
// End of subcircuit definition.

// Library name: VCO
// Cell name: VCO_beta
// View name: schematic
subckt VCO_replica2 Q QB Vctr divN divP
    I30 (net0143 Vctr QB Q divN divP) delay_cell1
    I23 (net0143 Vctr net39 net38 net29 net28) delay_cell1
    I25 (net0143 Vctr net29 net28 QB Q) delay_cell1
    I22 (net0143 Vctr Q QB net39 net38) delay_cell1
    R0 (net070 0) resistor r=34K m=1
    R3 (a1 a2) resistor r=20.53K m=1
    P28 (net0198 net0202 vdd! vdd!) tsmc25P w=4.5u l=1.8u as=3.375e-12 \
        ad=3.375e-12 ps=10.5u pd=10.5u m=1 region=sat
    P29 (net0202 net0202 vdd! vdd!) tsmc25P w=4.5u l=1.8u as=3.375e-12 \
        ad=3.375e-12 ps=10.5u pd=10.5u m=1 region=sat
    P30 (net0143 net0198 vdd! vdd!) tsmc25P w=7.5u l=1.5u as=5.625e-12 \
        ad=5.625e-12 ps=16.5u pd=16.5u m=1 region=sat
    P3 (a1 a2 net0102 net0102) tsmc25P w=1.5u l=900n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=2 region=sat
    P2 (net0117 a2 net090 net090) tsmc25P w=1.5u l=900n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=2 region=sat
    P0 (net090 a1 vdd! vdd!) tsmc25P w=3u l=1.2u as=2.25e-12 ad=2.25e-12 \
        ps=7.5u pd=7.5u m=4 region=sat
    P1 (net0102 a1 vdd! vdd!) tsmc25P w=3u l=1.2u as=2.25e-12 ad=2.25e-12 \
        ps=7.5u pd=7.5u m=4 region=sat
    P8 (net0190 a2 net078 net078) tsmc25P w=1.5u l=900n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=4 region=sat
    P26 (net0200 Vctr vdd! vdd!) tsmc25P w=1.2u l=300n as=9e-13 ad=9e-13 \
        ps=3.9u pd=3.9u m=1 region=sat
    P9 (net078 a1 vdd! vdd!) tsmc25P w=3u l=1.2u as=2.25e-12 ad=2.25e-12 \
        ps=7.5u pd=7.5u m=8 region=sat
    N19 (net0200 vdd! net0225 0) tsmc25N w=6.3u l=300n as=4.725e-12 \
        ad=4.725e-12 ps=14.1u pd=14.1u m=1 region=sat
    N21 (net0225 net0143 0 0) tsmc25N w=9u l=1.8u as=6.75e-12 ad=6.75e-12 \
        ps=19.5u pd=19.5u m=4 region=sat
    N22 (net0143 net0143 0 0) tsmc25N w=9u l=1.8u as=6.75e-12 ad=6.75e-12 \
        ps=19.5u pd=19.5u m=1 region=sat
    N23 (0 net0198 0 0) tsmc25N w=30u l=24.0u as=2.25e-11 ad=2.25e-11 \
        ps=61.5u pd=61.5u m=1 region=sat
    N24 (net0202 Vctr net0205 0) tsmc25N w=7.5u l=1.5u as=5.625e-12 \
        ad=5.625e-12 ps=16.5u pd=16.5u m=1 region=sat
    N25 (net0198 net0200 net0205 0) tsmc25N w=7.5u l=1.5u as=5.625e-12 \
        ad=5.625e-12 ps=16.5u pd=16.5u m=1 region=sat
    N26 (net0205 net0190 0 0) tsmc25N w=9u l=1.8u as=6.75e-12 ad=6.75e-12 \
        ps=19.5u pd=19.5u m=1 region=sat
    N0 (net0117 net0117 0 0) tsmc25N w=900n l=7.8u as=6.75e-13 ad=6.75e-13 \
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        ps=3.3u pd=3.3u m=1 region=sat
    N1 (a2 net0117 net070 0) tsmc25N w=900n l=7.8u as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=8 region=sat
    N6 (net0190 net0190 0 0) tsmc25N w=9u l=1.8u as=6.75e-12 ad=6.75e-12 \
        ps=19.5u pd=19.5u m=1 region=sat
ends VCO_beta
// End of subcircuit definition.


// Library name: Divider_digital
// Cell name: DFF1
// View name: schematic
subckt DFF1 CLB CLK DATA PrB Q QB
    N5 (net1 net4 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N6 (net_240 net25 net_241 0) tsmc25N w=900n l=300n as=6.75e-13 \
        ad=6.75e-13 ps=3.3u pd=3.3u m=1 region=sat
    N7 (net9 net1 net_240 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N8 (net_241 CLB 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N9 (net9 net4 net_87 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N10 (net_87 DATA 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N11 (net25 net9 net_135 0) tsmc25N w=900n l=300n as=6.75e-13 \
        ad=6.75e-13 ps=3.3u pd=3.3u m=1 region=sat
    N12 (net_135 PrB 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N13 (net18 CLB net_111 0) tsmc25N w=900n l=300n as=6.75e-13 \
        ad=6.75e-13 ps=3.3u pd=3.3u m=1 region=sat
    N14 (net_111 net1 net_115 0) tsmc25N w=900n l=300n as=6.75e-13 \
        ad=6.75e-13 ps=3.3u pd=3.3u m=1 region=sat
    N15 (net_115 net25 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N16 (net_99 net7 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N17 (net14 CLB net_99 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N18 (net18 net4 net14 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N4 (net4 CLK 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N3 (net_119 net18 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N2 (net7 PrB net_119 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N0 (QB net7 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 ps=3.3u \
        pd=3.3u m=1 region=sat
    N1 (Q net14 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 ps=3.3u \
        pd=3.3u m=1 region=sat
    P1 (net1 net4 vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P2 (net_18 DATA vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P3 (net9 net1 net_18 vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P4 (net_26 net25 vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P5 (net9 net4 net_26 vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
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    P6 (net_34 CLB vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P7 (net9 net4 net_34 vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P8 (net25 net9 vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P9 (net25 PrB vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P0 (net4 CLK vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P10 (net14 CLB vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P11 (net14 net7 vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P12 (net_82 net25 vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P13 (net18 net1 net14 vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P17 (net7 net18 vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P18 (QB net7 vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P19 (Q net14 vdd! vdd!) tsmc25P w=1.35u l=300n as=1.0125e-12 \
        ad=1.0125e-12 ps=4.2u pd=4.2u m=1 region=sat
    P15 (net7 PrB vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P14 (net18 net4 net_82 vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
ends DFF1
// End of subcircuit definition.

// Library name: Divider_digital
// Cell name: AND2
// View name: schematic
subckt AND2_schematic A B Out
    P2 (Out net028 vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P0 (net028 A vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    P1 (net028 B vdd! vdd!) tsmc25P w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    N2 (Out net028 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N1 (net028 A net16 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N0 (net16 B 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 ps=3.3u \
        pd=3.3u m=1 region=sat
ends AND2_schematic
// End of subcircuit definition.

// Library name: Divider_digital
// Cell name: Divider3
// View name: schematic
subckt Divider3 Clk Q
    V3 (net022 0) vsource type=pwl wave=[ 0 0 2n 0 2.1n 3.3 100n 3.3 ]
    I3 (net022 Clk net13 vdd! net17 net024) DFF1
    I4 (net022 Clk net20 vdd! Q net13) DFF1
    I2 (net13 net17 net20) AND2_schematic
ends Divider3
// End of subcircuit definition.
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```
// Library name: Divider
// Cell name: diff_sin
// View name: schematic
subckt diff_sin iddt inn inp out
    N4 (net063 iddt 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N5 (net046 net063 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N8 (net68 net046 0 0) tsmc25N w=900n l=300n as=6.75e-13 ad=6.75e-13 \
        ps=3.3u pd=3.3u m=1 region=sat
    N10 (net80 net063 net68 0) tsmc25N w=900n l=300n as=6.75e-13 \
        ad=6.75e-13 ps=3.3u pd=3.3u m=1 region=sat
    N7 (net68 net053 0 0) tsmc25N w=4.8u l=1.8u as=3.6e-12 ad=3.6e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    N6 (net80 net063 net053 0) tsmc25N w=900n l=300n as=6.75e-13 \
        ad=6.75e-13 ps=3.3u pd=3.3u m=1 region=sat
    N0 (net104 inp net107 0) tsmc25N w=4.8u l=300n as=3.6e-12 ad=3.6e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    N1 (out inn net107 0) tsmc25N w=4.8u l=300n as=3.6e-12 ad=3.6e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    N9 (net107 net68 0 0) tsmc25N w=4.8u l=1.8u as=3.6e-12 ad=3.6e-12 \
        ps=11.1u pd=11.1u m=4 region=sat
    P4 (net80 net063 vdd! vdd!) tsmc25P w=1.8u l=300n as=1.35e-12 \
        ad=1.35e-12 ps=5.1u pd=5.1u m=1 region=sat
    P2 (net063 iddt vdd! vdd!) tsmc25P w=1.8u l=300n as=1.35e-12 \
        ad=1.35e-12 ps=5.1u pd=5.1u m=1 region=sat
    P3 (net046 net063 vdd! vdd!) tsmc25P w=1.8u l=300n as=1.35e-12 \
        ad=1.35e-12 ps=5.1u pd=5.1u m=1 region=sat
    P5 (net68 net80 vdd! vdd!) tsmc25P w=3.9u l=3.6u as=2.925e-12 \
        ad=2.925e-12 ps=9.3u pd=9.3u m=1 region=sat
    P0 (net104 net104 vdd! vdd!) tsmc25P w=5.4u l=525.00n as=4.05e-12 \
        ad=4.05e-12 ps=12.3u pd=12.3u m=1 region=sat
    P1 (out net104 vdd! vdd!) tsmc25P w=5.4u l=525.00n as=4.05e-12 \
        ad=4.05e-12 ps=12.3u pd=12.3u m=1 region=sat
ends diff_sin
// End of subcircuit definition.

// Library name: Divider
// Cell name: DFF_LS
// View name: schematic
subckt DFF_LS Clk ClkB D DB Q QB iddt
    P3 (Q Q vdd! vdd!) tsmc25P w=1.8u l=300n as=1.35e-12 ad=1.35e-12 \
        ps=5.1u pd=5.1u m=1 region=sat
    P2 (QB QB vdd! vdd!) tsmc25P w=1.8u l=300n as=1.35e-12 ad=1.35e-12 \
        ps=5.1u pd=5.1u m=1 region=sat
    P1 (net79 net79 vdd! vdd!) tsmc25P w=1.8u l=300n as=1.35e-12 \
        ad=1.35e-12 ps=5.1u pd=5.1u m=1 region=sat
    P0 (net83 net83 vdd! vdd!) tsmc25P w=1.8u l=300n as=1.35e-12 \
        ad=1.35e-12 ps=5.1u pd=5.1u m=1 region=sat
    P5 (net25 net25 vdd! vdd!) tsmc25P w=3.9u l=3.6u as=2.925e-12 \
        ad=2.925e-12 ps=9.3u pd=9.3u m=1 region=sat
    P4 (net91 iddt vdd! vdd!) tsmc25P w=5.1u l=300n as=3.825e-12 \
        ad=3.825e-12 ps=11.7u pd=11.7u m=1 region=sat
    N26 (vdd! ClkB net0150 0) tsmc25N w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    N27 (net0150 net115 0 0) tsmc25N w=9u l=1.8u as=6.75e-12 ad=6.75e-12 \
        ps=19.5u pd=19.5u m=1 region=sat
    N25 (vdd! Clk net0128 0) tsmc25N w=1.5u l=300n as=1.125e-12 \
        ad=1.125e-12 ps=4.5u pd=4.5u m=1 region=sat
    N24 (net0128 net115 0 0) tsmc25N w=9u l=1.8u as=6.75e-12 ad=6.75e-12 \
        ps=19.5u pd=19.5u m=1 region=sat
```

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    N13 (net46 net115 0 0) tsmc25N w=9u l=1.8u as=6.75e-12 ad=6.75e-12 \
        ps=19.5u pd=19.5u m=4 region=sat
    N12 (net54 net115 0 0) tsmc25N w=9u l=1.8u as=6.75e-12 ad=6.75e-12 \
        ps=19.5u pd=19.5u m=4 region=sat
    N11 (net62 net0128 net46 0) tsmc25N w=5.1u l=300n as=3.825e-12 \
        ad=3.825e-12 ps=11.7u pd=11.7u m=1 region=sat
    N10 (net70 net0150 net46 0) tsmc25N w=5.1u l=300n as=3.825e-12 \
        ad=3.825e-12 ps=11.7u pd=11.7u m=1 region=sat
    N9 (net78 net0150 net54 0) tsmc25N w=5.1u l=300n as=3.825e-12 \
        ad=3.825e-12 ps=11.7u pd=11.7u m=1 region=sat
    N8 (net86 net0128 net54 0) tsmc25N w=5.1u l=300n as=3.825e-12 \
        ad=3.825e-12 ps=11.7u pd=11.7u m=1 region=sat
    N7 (Q QB net62 0) tsmc25N w=4.5u l=300n as=3.375e-12 ad=3.375e-12 \
        ps=10.5u pd=10.5u m=1 region=sat
    N6 (QB Q net62 0) tsmc25N w=4.5u l=300n as=3.375e-12 ad=3.375e-12 \
        ps=10.5u pd=10.5u m=1 region=sat
    N5 (Q net83 net70 0) tsmc25N w=4.5u l=300n as=3.375e-12 ad=3.375e-12 \
        ps=10.5u pd=10.5u m=1 region=sat
    N4 (QB net79 net70 0) tsmc25N w=4.5u l=300n as=3.375e-12 ad=3.375e-12 \
        ps=10.5u pd=10.5u m=1 region=sat
    N3 (net79 net83 net78 0) tsmc25N w=4.5u l=300n as=3.375e-12 \
        ad=3.375e-12 ps=10.5u pd=10.5u m=1 region=sat
    N2 (net83 net79 net78 0) tsmc25N w=4.5u l=300n as=3.375e-12 \
        ad=3.375e-12 ps=10.5u pd=10.5u m=1 region=sat
    N1 (net79 DB net86 0) tsmc25N w=4.5u l=300n as=3.375e-12 ad=3.375e-12 \
        ps=10.5u pd=10.5u m=1 region=sat
    N0 (net83 D net86 0) tsmc25N w=4.5u l=300n as=3.375e-12 ad=3.375e-12 \
        ps=10.5u pd=10.5u m=1 region=sat
    N18 (net83 net115 0 0) tsmc25N w=600n l=1.8u as=4.5e-13 ad=4.5e-13 \
        ps=2.7u pd=2.7u m=1 region=sat
    N14 (net91 iddt 0 0) tsmc25N w=12.6u l=300n as=9.45e-12 ad=9.45e-12 \
        ps=26.7u pd=26.7u m=1 region=sat
    N15 (net25 net91 net115 0) tsmc25N w=7.2u l=300n as=5.4e-12 ad=5.4e-12 \
        ps=15.9u pd=15.9u m=1 region=sat
    N17 (net115 net115 0 0) tsmc25N w=9u l=1.8u as=6.75e-12 ad=6.75e-12 \
        ps=19.5u pd=19.5u m=1 region=sat
    N21 (Q net115 0 0) tsmc25N w=600n l=1.8u as=4.5e-13 ad=4.5e-13 ps=2.7u \
        pd=2.7u m=1 region=sat
    N19 (net79 net115 0 0) tsmc25N w=600n l=1.8u as=4.5e-13 ad=4.5e-13 \
        ps=2.7u pd=2.7u m=1 region=sat
    N20 (QB net115 0 0) tsmc25N w=600n l=1.8u as=4.5e-13 ad=4.5e-13 \
        ps=2.7u pd=2.7u m=1 region=sat
    N16 (net115 iddt 0 0) tsmc25N w=12.6u l=300n as=9.45e-12 ad=9.45e-12 \
        ps=26.7u pd=26.7u m=1 region=sat
ends DFF_LS
// End of subcircuit definition.

// Library name: Divider
// Cell name: DIVIDEBY2
// View name: schematic
subckt DIVIDEBY2 Clk ClkB Q QB iddt
    I5 (Clk ClkB QB Q Q QB iddt) DFF_LS
ends DIVIDEBY2
// End of subcircuit definition.

// Library name: Divider
// Cell name: DIVIDEBY18_mixed
// View name: schematic
subckt DIVIDEBY18_mixed Clk Qout clkB iddt
    I5 (net017 net015) Divider3
    I6 (net015 Qout) Divider3
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```
    I4 (iddt net14 net15 net017) diff_sin
    I0 (Clk clkB net15 net14 iddt) DIVIDEBY2
ends DIVIDEBY18_mixed
// End of subcircuit definition.

// Library name: System
// Cell name: System4
// View name: schematic
I7 (Vctr net036 net031 net032 net020) Charge_pump_schematic
I16 (Down net031) INV
I1 (Up net020) INV
P1 (net036 0 Down vdd!) tsmc25P w=11.175u l=300n as=8.38125e-12 \
        ad=8.38125e-12 ps=23.85u pd=23.85u m=1 region=sat
P3 (net032 0 Up vdd!) tsmc25P w=11.175u l=300n as=8.38125e-12 \
        ad=8.38125e-12 ps=23.85u pd=23.85u m=1 region=sat
N3 (Up vdd! net032 0) tsmc25N w=10.95u l=300n as=8.2125e-12 ad=8.2125e-12 \
        ps=23.4u pd=23.4u m=1 region=sat
N1 (Down vdd! net036 0) tsmc25N w=11.25u l=300n as=8.4375e-12 \
        ad=8.4375e-12 ps=24.0u pd=24.0u m=1 region=sat
I0 (Clk_in Ref_clk Down Up) PFD_dig
R0 (Vctr net042) resistor r=100K m=1
C1 (net042 0) capacitor c=3p m=1
C0 (Vctr 0) capacitor c=500.0f m=1
I14 (Q QB Vctr divN divP) VCO_beta
I13 (divN Clk_in divP 0) DIVIDEBY18_mixed
V5 (Ref_clk 0) vsource type=pulse val0=0 val1=3.3 period=11.574n delay=0 \
        rise=10p fall=10p width=5.687n
// End of Netlist
```

Vita

Md. Hafijur Rahman was born on the December 31 ′1973 in Dinajpur, Bangladesh. During his initial schooling, he lived with his family in Birgonj, Dinajpur. He received his high school diploma from Rangpur Cadet College, Rangpur in 1991. Rahman began his academic career by enrolling at Bangladesh University of Engineering and Technology (BUET), Dhaka, majoring in Electrical Engineering in 1993. He graduated with Bachelor of Science in Electrical Engineering in December ′1998. After his graduation, he joined as a lecturer in the same university and successfully served as a lecturer until August ′2000. During this period, he also worked as a part-time lecturer in Islamic Institute of Technology (IIT), Dhaka and Ahasanullah Engineering University, Dhaka. He worked on research projects 'Microprocessor-based Power Factor Control' and 'Microprocessor-based Auto-meter for Power Supply Distribution'. In Fall ′2000, he enrolled as a graduate student at the University of Tennessee, Knoxville to earn a Master's in Electrical Engineering. During Summer ′2001, he worked as a summer intern at TranSwitch Corporation, Raleigh. He is currently working under the supervision of Dr. Syed K. Islam at the Analog-Mixed Signal VLSI and Devices Laboratory. He plans to complete his Master's with a specialization in Analog IC design in December ′2002 and work towards his Ph.D.