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I am submitting herewith a dissertation written by Peyman H. Dehkordi, entitled "Design For Packagability - The Impact of Bonding And Interconnect Technologies on The Performance of VLSI Dies." I have examined the final copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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DESIGN FOR PACKAGABILITY
THE IMPACT OF BONDING AND INTERCONNECT
TECHNOLOGIES ON THE PERFORMANCE
OF VLSI DIES

A Dissertation

Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Peyman H. Dehkordi

May 1992

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DEDICATION

This dissertation is dedicated to my family

Poori-jun, Baba, Golbarg, and Golshan

and

to the **best teacher** I have ever had

Mr. Ebraheim Khorami

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ABSTRACT

Silicon-on-silicon multichip module (MCM) packaging is maturing rapidly. It offers the integrated circuit (IC) designer a new approach over the conventional packaged IC on the printed circuit board. The bare ICs can now be mounted and interconnected on a silicon substrate for superior system performance. In general, the performance at the system level is a function of the package and the die and can be described as:

$$\text{Performance}_{\text{system}} = f(\text{Performance}_{\text{package}} + \text{Performance}_{\text{die}})$$

This work looks into the impact of the packaging technology from an IC designer's point of view. This dissertation is focused exclusively on investigating the "Performance_{die}" term due to a change in packaging technology.

As a proof of principle, two image processing chip-sets have been designed with the conventional wire-bond/PCB and flip-chip/MCM packaging in mind. This work demonstrates how the performance of the dies change as they are designed for wire-bond/PCB and flip-chip/MCM technologies. The impact of the bonding/substrate technologies (i.e. wire-bond/PCB and flip-chip/MCM) on the performance of dies are demonstrated quantitatively in the following areas:

- Power
- Size
- Testability
- Cost

TABLE OF CONTENTS

1. INTRODUCTION	1
1.1 Introduction to Multichip Module Packaging	1
1.2 Bonding and Interconnection Technologies	5
1.3 Work Motivation	10
1.4 The Image Processor Chip-Set	13
1.5 Organization of the Dissertation	14
2. RELATED WORK	15
2.1 SUSPENS	16
2.2 AUDiT	17
2.3 SDA	19
2.4 Nagesh Method	20
2.5 Comparison	21
3. SIZE ANALYSIS	23
3.1 Size Calculations of Flip-chip and Wire-bond ICs	23
3.2 Examples and Results	26
4. POWER CONSUMPTION ANALYSIS	43
4.1 CMOS Power Estimation	43
4.2 Power Calculation of Flip-chip and Wire-bond ICs	46
4.3 Examples and Results	50
5. TESTING ANALYSIS	55
5.1 Testability Measures	56
5.2 Importance of The Test Points	57
5.3 Scan-Path Technique	60
5.4 Examples and Results	62
6. COST ANALYSIS	65
6.1 A Simplified Cost Model	65
6.2 Examples and Results	67
7. SUMMARY	73
7.1 Conclusion	73
7.2 Future Work	75
LIST OF REFERENCES	77
VITA	82

LIST OF FIGURES

Figure 1. Packaging Hierarchy.	2
Figure 2. Multiple Levels of Interconnection.	2
Figure 3. Feature Size Comparison Between IC, PCB, and Package Pin Count ...	4
Figure 4. Comparison Between PCB and MCM's Levels of Connection.	4
Figure 5. Wire Bonding	6
Figure 6. TAB Assembly	7
Figure 7. Flip-Chip Technology	8
Figure 8. A Conceptual Diagram of The Work Motivation.	12
Figure 9. Image Processor Block Diagram.	13
Figure 10. A Typical Wire-bond Chip Layout.	24
Figure 11. A typical Flip-chip Chip Layout.	24
Figure 12. Logic Diagram of a 16-bit Adder.	27
Figure 13. Layout of a 16-bit full adder (wire-bond version)	28
Figure 14. Layout of a 16-bit full adder (flip-chip version)	29
Figure 15. Layout of the processing element (PE) chip (wire-bond version).	31
Figure 16. Layout of the processing element (PE) chip (flip-chip version).	32
Figure 17. Layout of the input/output (IO) chip (wire-bond version).	33
Figure 18. Layout of the input/output (IO) chip (flip-chip version).	34
Figure 19. Layout of the controller (CTL) chip (wire-bond version).	35
Figure 20. Layout of the controller (CTL) chip (flip-chip version).	36
Figure 21. Size Comparison of PE Chips for wire-bond and flip-chip.	39
Figure 22. Size Comparison of IO Chips for Wire-bond and Flip-chip.	39
Figure 23. Size Comparison of CTL Chips for Wire-bond and Flip-chip.	40
Figure 24. Size Comparison of All Chips for Wire-bond and Flip-chip.	40
Figure 25. I/O Pad Drivers for Wire-bond and Flip-chip Technologies.	47
Figure 26. I/O Pad Power Consumptions for Different Chip Sizes.	49
Figure 27. Power Consumption of PE chips for Wire-bond and Flip-chip.	53
Figure 28. Power Consumption of IO chips for Wire-bond and Flip-chip.	53
Figure 29. Power Consumption of CTL chips for Wire-bond and Flip-chip.	54
Figure 30. Power Consumption of ALL chips for Wire-bond and Flip-chip.	54
Figure 31. Impact of number of test points on observability, ...	59
Figure 32. Impact of number of test points on controllability.	59
Figure 33. Impact of number of test points in testability.	59
Figure 34. Maximum Number of I/O for Wire-Bond and Flip-Chip.	60
Figure 35. Scan-Path Testing Concept.	61
Figure 36. Comparison of Test Coverage Between Wire-bond and Flip-chip.	62
Figure 37. Cost Comparison of the PE Chip for Wire-bond and Flip-chip technologies.	70
Figure 38. Cost Comparison of the IO Chip for Wire-bond and Flip-chip technologies.	70
Figure 39. Cost Comparison of the CTL Chip for Wire-bond and Flip-chip technologies.	71

Figure 40. Cost Comparison of the All Chips for Wire-bond and Flip-chip technologies.	71
Figure 41. Over All Comparison of Flip-chip and Wire-bond Technology.	74

LIST OF TABLES

Table 1. Comparison of Different Die Attachment Techniques	9
Table 2. Dimensions and Area (in λ and λ^2) of the PE, IO, and CTL Chips.	37
Table 3. Size Reduction Estimations.	42
Table 4. The Power Consumption Measurements.	52
Table 5. Power Reduction Estimation	52
Table 6. Default Values for Cost Models.	68
Table 7. Cost Comparison of Wire-Bond and Flip-Chip Dies.	68
Table 8. Final Cost Break Down for Wire-Bond and Flip-chip.	69

CHAPTER I

INTRODUCTION

1.1 Introduction to Multichip Module Packaging

The cost and performance of VLSI systems have been improving for the last two decades. These improvements are mainly accounted for by higher levels of integration due to smaller device sizes with faster intrinsic speeds [1], [2]. It is desirable to implement a complete VLSI system as a single die. However, this is not possible in most cases due to the yield limitations of the technology. As an alternative, the entire system is partitioned into different subsystems. Each subsystem is then implemented in a single die and connected together by some kind of packaging and interconnection scheme.

The packaging hierarchy of a typical digital system is shown in Figure 1. A single die is packaged in a single-chip package that is mounted on a printed circuit board (PCB). The PCBs are then plugged into a backplane or communicate through cables. The path that a signal traverses from one chip to another is shown in Figure 2. The signal delay is the sum of the intrinsic device delay and the line delays (i.e. added delay due to the length and multiple levels of interconnections). Therefore, decreasing the chip delay by reducing the feature size below a typical line delay may have little impact on the speed of the overall system [3].

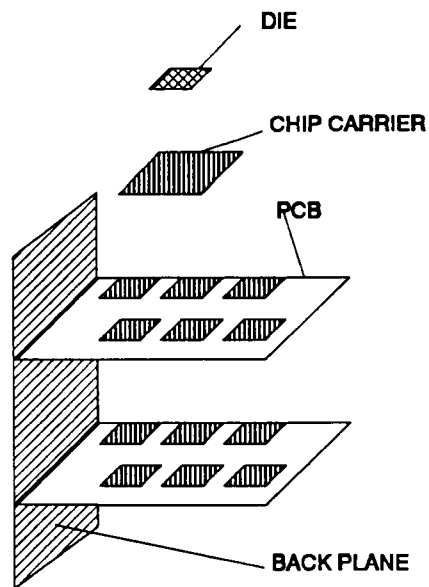


Figure 1. Packaging Hierarchy.

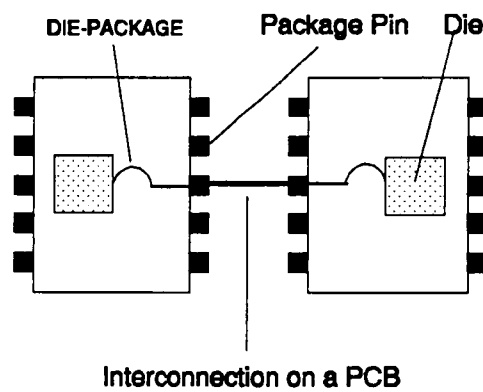


Figure 2. Multiple Levels of Interconnection.

Unfortunately, packaging technology has been delaying the advances in integrated circuits for quite some time. The IC feature size has been reduced by a factor of 6X over a ten year period as shown in Figure 3. PCB features have been reduced by 2.5X while pin count is estimated to have increased by 2.4X over the same period [4].

Larger chip area and smaller feature size have produced a one hundred-fold increase in device per chip every decade [5]. However, packaging efficiency (i.e. size, number of I/O pins, etc) has improved only by a factor of two [6]. Consequently, the industry is beginning to experience system limitations due to this mismatch. Fifty percent of the high-end system delays are accounted for by the packaging and this number is expected to grow to eighty percent by the year 2000 [7]. For example, 52% of the 17.2 ns cycle time of the IBM 3090 is due to its packaging [8].

Wafer scale integration (WSI) answers the intermediate packaging problems by integrating the entire system on a wafer. Ideally, it gives the best performance because it eliminates all intermediate levels of packaging. Although major technical problems have been overcome since WSI was first introduced in the 1960s, it is not commercially available yet because of its poor manufacturing yields [9].

Multichip module (MCM) packaging is a packaging technology which is emerging to combat this mismatch. The underlying idea behind this technology is to pack as many bare dies as possible on a single silicon or ceramic substrate. This not only provides shorter and faster signal paths but also reduces one level of packaging as shown in Figure 4.

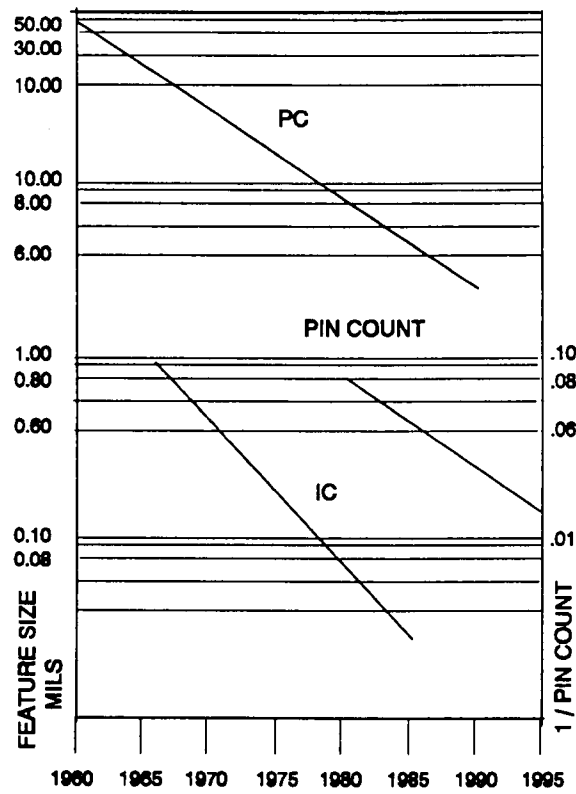


Figure 3. Feature Size Comparison Between IC, PCB, and Package Pin Count (reprinted from [4]).

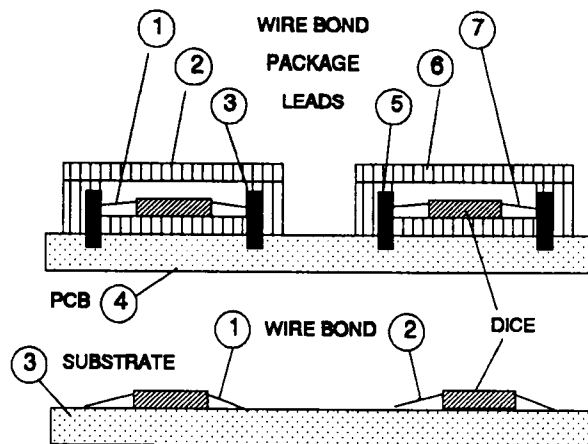


Figure 4. Comparison Between PCB and MCM's Levels of Connection.

There are arguments illustrating that an MCM can achieve performance and cost comparable to WSI [10]. This technology has shown promise to reduce the performance degradations induced by packaging.

1.2 Bonding and Interconnection Technologies

More recent types of MCMs use thin-film interconnects on a silicon substrate (si-on-si). This type of MCM borrows fine-line lithography from IC technology to fabricate fine interconnect lines with low parasitic parameters. Aluminum or copper is used as the interconnect material, and polyamide is often the choice for the insulating material. These silicon substrates usually have two to six layers of metal for interconnections. Dies are usually attached and electrically connected directly to the substrate by one of three ways: wire-bonding, tape-automated bonding (TAB), or flip-chip.

Wire-bonding is the most conventional die attachment method. In this technique, the back side of the die is glued down on the lead frame with diebond, which is a good thermal conductor. Then a wire-bonding machine connects the die I/O pads and the lead frame by aluminum or gold wires as shown in Figure 5. The wire-bonding method becomes inefficient as the number of I/O terminals increases. A high number of I/O terminals can cause shorts between the wires and a lengthy fabrication time because pads are bonded one at a time.

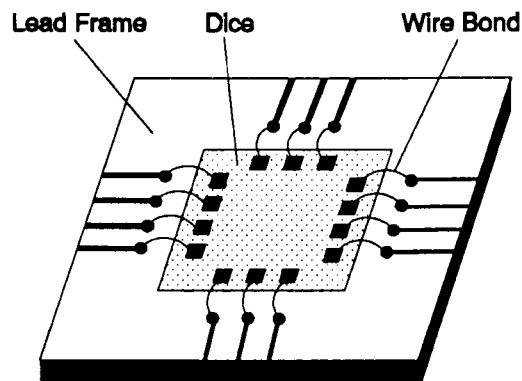


Figure 5. Wire Bonding

Another major problem is the large parasitic inductance of the bonding wires resulting in a noticeable delay at higher frequencies. Despite all these problems, wire-bonding continues to be a proven and cost-effective technology.

For a high I/O count, tape-automated-bonding (TAB) is a better choice of bonding than wire-bonding. In TAB technology, a rigid leadframe in the form of a polymer tape is positioned over the die with the inner leads aligned to the bond pads. Solder bumps are usually used between the tape and the bonding pads on the die as shown in Figure 6.

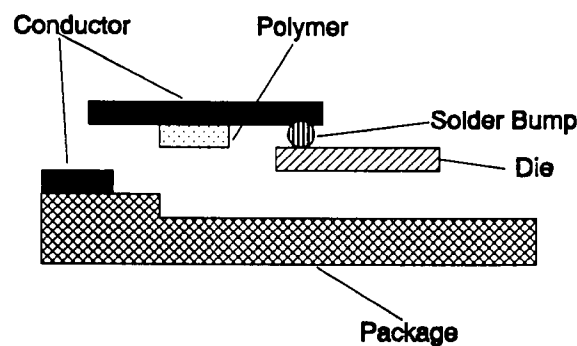


Figure 6. TAB Assembly

All the solder bumps form the connections simultaneously by a hot reflow process. This is an advantage over wire-bonding in which the connections are made one at a time. Another advantage of TAB is the short interconnection length between the die and the package, minimizing the lead inductance and capacitance. However, a major drawback in TAB technology is its cost. An individual TAB frame needs to be designed for each chip, requiring a large volume to justify the cost.

Another die attachment technique is the flip-chip method as shown in Figure 7. This method eliminates leads altogether by using solder bumps on the die that mate directly to the substrate. This method has many advantages including the minute parasitic

inductance and capacitance, small footprint and high I/O count. The I/O bonding pads can be placed all over the chip area as opposed to just the periphery in wire-bonding. This increases the number of I/O connections for a given die size and provides a more efficient routing scheme for interconnections within the chip.

The major problem with this technology is the shearing strain induced in the bumps due to the thermal expansion mismatch between the die and the substrate. This problem is even more severe for the bumps away from the center of the die. Investigations are underway promising solutions to this problem, specifically a stacked solder-bump method has been shown to increase the lifetime of the package by over 60x compared with the conventional methods [11]. Thermal resistance of the package may also increase because the chip is not attached to the package with a die bond. Therefore, the thermal path between the chip and the package is limited to the solder bumps unless a heat sink is placed on the back side of the chip.

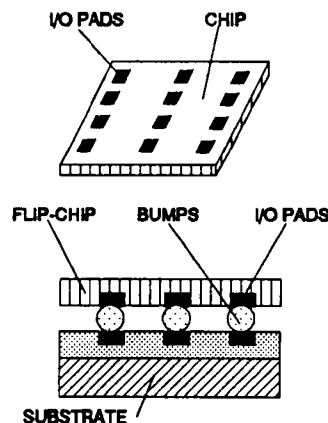


Figure 7. Flip-Chip Technology

A good comparison between the wire-bond, TAB, and flip-chip methods is given in [12] and summarized in Table 1. The flip-chip technology demonstrates superiority over other techniques in terms of parasitic inductance, the number of I/Os and the footprint size. In general, chips are not yet available to take advantage of the area array-bonding of the flip-chip technique. However, they are expected in the near future as VLSI designers start designing with flip-chip technology in mind.

Table 1. Comparison of Different Die Attachment Techniques (reprinted from [12]).

Technology Feature	Wire-Bond	TAB	Flip-Chip
Maturity	Very Good	Fair	Good
Chip Availability	Very Good	Fair	Poor
Cross Section (mil)	1 (dia)	1 x 3	2 x 2
Max I/O Count	300-500	500-700	> 700
Repairability	Poor	Fair	Good
Thermal Path	Substrate	Substrate	Substrate & Module
Chip Burn-in Test	Poor	Good	Fair
Parasitic Inductance	0.9 nH	0.7 nH	< 0.05 nH
Foot-print Size (mil)	20-100	80-600	Clearance
Area Array Bond Pitch	N/A	N/A	8-15 mil

1.3 Work Motivation

Most of VLSI systems are based on a single-chip package (i.e. one chip per package) as shown in Figure 2. In these systems, the chip is wire-bonded to the package and the package pins are connected together by a PCB trace. In multichip packaging (i.e. multiple chips per package), the bare version (i.e. unpackaged chip) of existing wire-bond dies is housed and interconnected on a substrate as shown in Figure 4. In general, the performance at the system level is a function of the package and the die and can be described as :

$$\text{Performance}_{\text{system}} = f(\text{Performance}_{\text{package}} + \text{Performance}_{\text{die}})$$

where $\text{Performance}_{\text{system}}$ is defined as the size, power consumption, cost, and speed of the system. Previous work have shown that the multichip approach has superior performance over the single-chip one. This gain in performance is achieved at the system level and is due to the " $\text{Performance}_{\text{package}}$ " term for the following reasons:

- 1) Elimination of the bulky conventional single-chip package.
- 2) Replacement of the PCB with an MCM substrate, which has better parasitic parameters.

The combination of the above results in a faster, smaller, and less power-consuming system. However, the performance of the die (i.e. the $\text{Performance}_{\text{die}}$ term) remains the same in either of the packaging environments. Therefore, the gain in the system performance is due completely to the packaging:

$$\Delta \text{Performance}_{\text{system}} = \Delta \text{Performance}_{\text{package}}$$

The motivation behind this work comes from the fact that all of the previous work have tried to identify the " $\Delta \text{Performance}_{\text{package}}$ " [13][14]. The work presented here shows that there could be an additional gain in performance due to " $\text{Performance}_{\text{die}}$ " because of a change in the packaging environment. Therefore, a more comprehensive model can be used to analyze the impact of packaging at the system level:

$$\Delta \text{Performance}_{\text{system}} = \Delta \text{Performance}_{\text{package}} + \Delta \text{Performance}_{\text{die}}$$

This work is exclusively focused on investigating the " $\Delta \text{Performance}_{\text{die}}$ " term due to the change in packaging and does not cover the " $\Delta \text{Performance}_{\text{package}}$ " and " $\Delta \text{Performance}_{\text{system}}$ ". As a proof-of-principle, an image processing chip-sets is designed for the conventional wire-bonding/PCB and then redesigned for the flip-chip/MCM as shown in Figure 8. This work shows how the performance of the die changes as the packaging changes from wire-bond/PCB to flip-chip/MCM. The impact of the packaging technology (i.e. wire-bond/PCB and flip-chip/MCM) on the performance of the dies is demonstrated quantitatively by evaluating a figure-of-merit for both approaches. This figure-of-merit is a measure of cost and performance and depends on the power, size, cost, and testability of the designed dies. It is computed as:

$$\text{Figure}_{\text{merit}} = \frac{W1}{\text{Size}} + \frac{W2}{\text{Power}} + W3 * \text{Testability} + \frac{W4}{\text{cost}}$$

where W's are the weight constants. It is important for the reader to note that all the comparisons are done at the chip level rather than the system level.

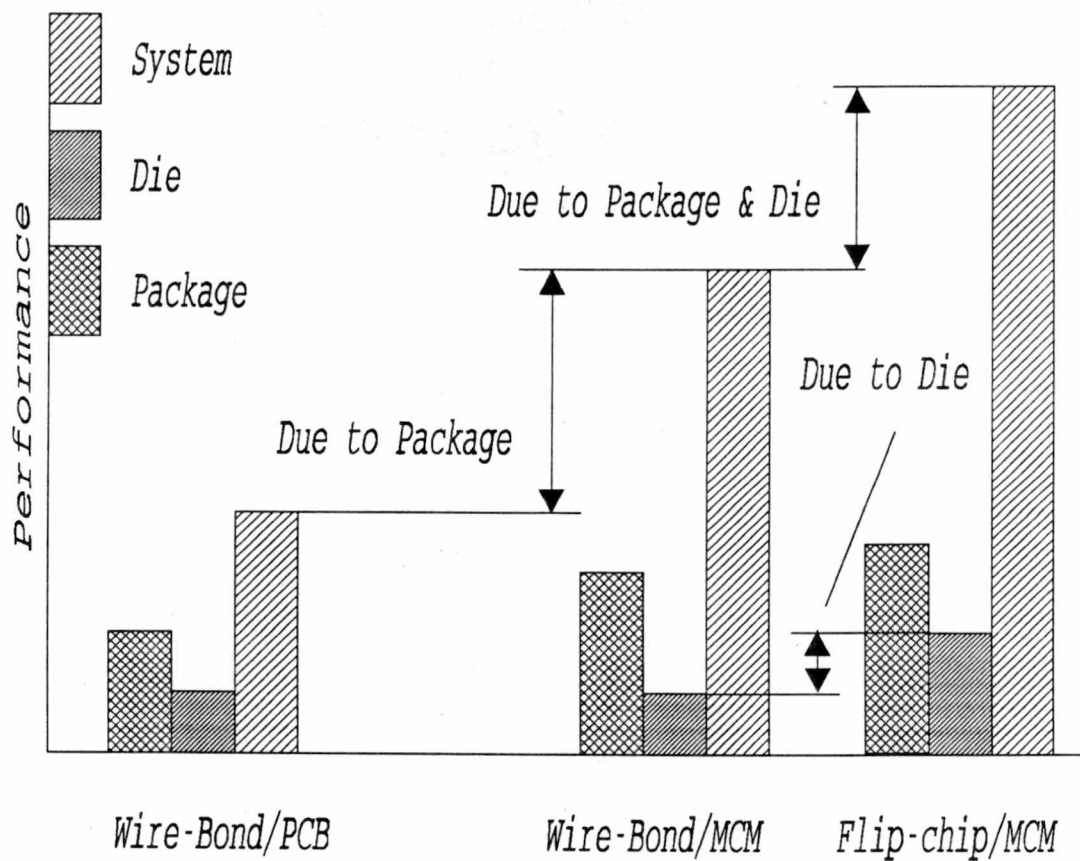
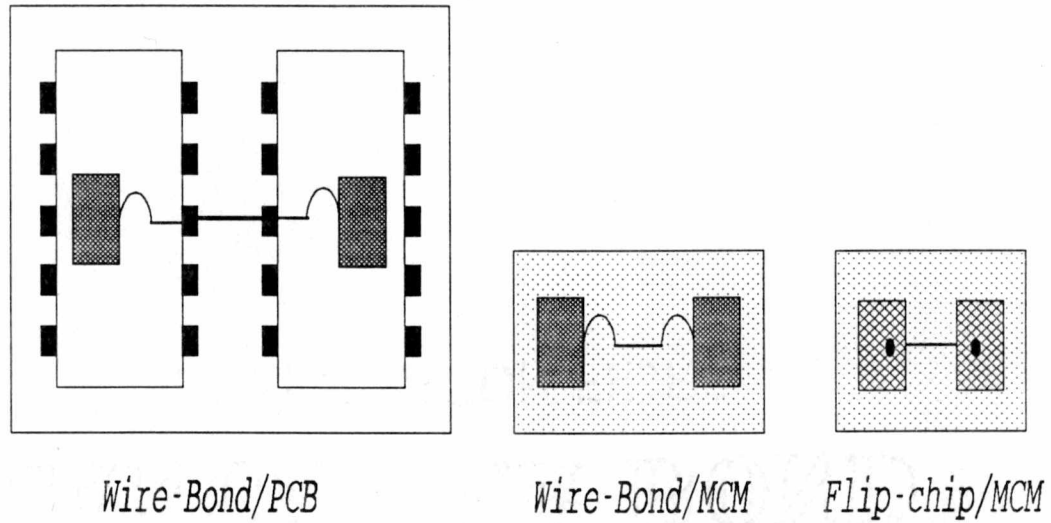


Figure 8. A Conceptual Diagram of The Work Motivation.

1.4 The Image Processor Chip-Set

An image-processor chip-set is used as a demonstrating vehicle. This chip-set was designed and synthesized for both wire-bond/PCB and flip-chip/MCM technologies. The building block diagram of the image processor is shown in Figure 9. It is partitioned into four types of chips: processing elements, inputs/outputs, global controller, and the memory chips. This partitioning is done strictly to create four chips with different characteristics for demonstration purposes.

The processing element (PE) is based on the massively parallel processing (MPP) architecture which was originally introduced by [15] and enhanced by [16][17]. An I/O section (IO) has been added to the original MPP for an easy serial interfacing to the digitized video signal. This is similar to the work proposed by [18]. The memory chips have not been designed due to their off-the-shelf availability. The controller (CTL) is responsible for decoding the user micro-instructions and provides all the control signals to the PE, IO, and memory sections.

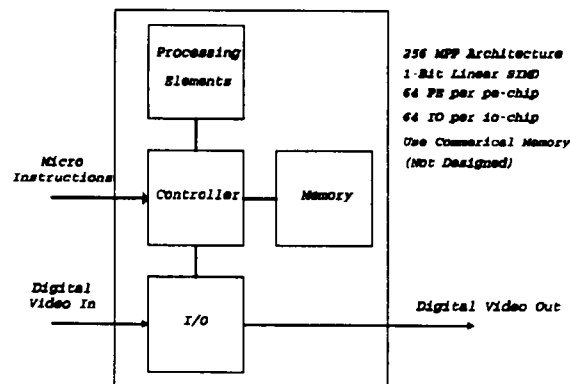


Figure 9. Image Processor Block Diagram.

1.5 Organization of the Dissertation

This report is organized into seven different chapters. Chapter two contains some of the previous work involved with the impact of packaging parameters on the performance of the VLSI systems. The next chapter explains the impact of packaging on the size of the die while chapter four discusses power consumption issues. Chapter five addresses some of the important issues in testing of the VLSI chips and then discusses how packaging may impact the testing. Cost-related parameters are presented next, where simplified cost models for flip-chip and wire-bond dies are presented. Chapters 3-7 explain the impact of the packaging technology in a general form, and specific examples (i.e. the image processor chip-set) are used to highlight the results. A summary of this work, as well as some suggestions for future work, are given in the last chapter.

CHAPTER 2

RELATED WORK

This chapter addresses some of the previous work involved with the impact of packaging-related issues. These may be divided into two areas: experimental, and global. The "experimental" work shows the impact of packaging by fabricating a system based on two or more packaging techniques. Works such as [14][13][19] compares conventional packaging with MCM packaging. The dies remain the same in either package and all comparisons are done at the system level. No formal discussions are given in this work and the change in the system performance is due completely to the change in the packaging environments.

The "global" work, in the other hand, uses formal discussions to describe the impact of packaging. They approach the issues by using a mathematical model to describe the system in terms of the package and the chips. This model is then used to describe the impact of the packaging in the overall system performance. The packages are described by their physical and electrical characteristics. The chips, however, are modeled globally by the physical size of the die and the number of I/Os. The rest of this chapter explains and compares some of this work together.

2.1 SUSPENS

SUSPENS (Stanford University System Performance Simulator) is a simulation model that emphasizes the interactions among devices, circuits, logic, packaging, and architecture [20]. It determines the impact of a proposed device or packaging technology on the overall system performance. The input to this model is a set of technology, design, and packaging parameters. The output is the overall system performance measured in terms of maximum clock frequency, total power dissipation, and chip and system size. The input parameters can be categorized in six sections as follows:

Chip Technology:	The choice of the different chip technologies (CMOS, nMOS, ECL, GaAs) is allowed to compare the electrical properties of these technologies.
Design Size:	This is the total number of gates in the design.
Packaging Technology:	The packaging related parameters are limited to the choice of the substrate. Four choices of packaging is supported: wafer-scale integration, si-on-si MCM, multilayer ceramic, and conventional single chip carriers on the PCBs.
Chip Integration Level:	This is the total number of gates allowed in a chip. This parameter, along with the total number of gates in the system determines the total number of chips.
Chip Architecture:	This set of parameters defines the performance of the chip in terms of logic depth, fan-out of the gates, and the Rent's constant, which is proportional to the number of I/Os.
System Architecture:	This has probably been the greatest challenge of the SUSPENS model to link the architectural and technological parameters together. This is achieved by

using Rent's rule to describe the architecture of the system. Rent's rule yields the number of connections and average interconnection length to and within a logic block.

SUSPENS is used to predict the performance of various size CMOS microprocessors for different packaging technologies [21].

2.2 AUDiT

AUDiT (AUtomed Design and Tradeoff) is another mathematical tool developed to investigate the trade-off issues in the partitioning of a multichip module design [22][23]. While SUSPENS approaches the packaging issues from a simulation point of view, AUDiT uses an optimization method to partition the design among different chips. In AUDiT, the full system is described by using a combination of physical and architectural models similar to SUSPENS. The packaging model consists of the chips, MCMs, and PCBs, which is more complete than SUSPENS's two levels (i.e the chip and MCM). Rent's rule is also used by AUDiT to account for the system architecture in terms of number of I/Os for a given circuit size.

There are a number of packaging parameters introduced in the model. Some of these parameters are fixed to a certain technology for simplicity purposes. For example, flip-chip bonding and pin-grid-array (PGA) packaging are assumed for die and MCM attachments. There are six packaging parameters selected for the optimization.

These parameters along with their ranges are:

- Chip Integration Density : This is the number of gates per chip, which in turns determines the chip size (1,000-100,000).
- Module Integration Density: This is the total number of MCMs on a PCB (1-100).
- Signal Layers: The number of multi-layer interconnects on the substrate of the MCMs (6-30).
- Grid Spacing: Interconnect is assumed to be organized in X and Y wire planes on a square via grid (10-100).
- Dielectric Constant: The dielectric value of the inter-layer on the substrate (2.2-9.4).
- MCM Line Resistivity: This is the MCM interconnect line resistivity, which in turns defines the type of metal interconnect to be used (0-20 Micro-Ohm / Cm).

These packaging variables are computed by solving a large set of model equations to optimize a cost function. The cycle time of the system under investigation is used as a cost function. The cycle time is defined as the total delay on the critical path through which a signal has to travel between any two nodes in the system. This cycle time is determined by the following equation:

$$\text{Cycle Time} = (\text{Chip.d} * \text{Chip.ld} + \text{MCM.d}) * \text{MCM.n} + \text{PCB.d}) * \text{PCB.n}$$

where:

- | | |
|---------|--|
| Chip.d | : Average delay on the chip. |
| Chip.ld | : Chip logic depth. |
| MCM.d | : Average delay involved with the MCM. |
| MCM.n | : Number of MCMs on the PCB. |
| PCB.d | : Average delay involved with the board. |
| PCB.n | : Number of the PCBs in the system. |

AUDit is used to predict the optimum solutions with a minimum cycle time for a logic sub-system and memory sub-system with 500,000 gates. The results show three partitions for the logic sub-system and two for the memory sub-system.

2.3 SDA

SDA (Substrate Die Attach) is a new packaging tradeoff analysis tool [24]. It is also a system-level tool for enhancing the manufacturability and decreasing the design risk associated with the selection of packaging technologies. It estimates geometric, electrical, thermal, and manufacturing metrics for the MCM design.

SDA is intended to be used before, during, and after prototype design and fabrication of the multichip packaging systems to provide design-specific performance estimations. It can be used in the early stage of the design before the use of detailed CAD tools. Rough performance estimates can be made at this stage requiring only a small amount of information from the designer. As the design and the fabrication progress, the SDA default values are refined using designed or measured values. This refinement allows a more accurate estimation which permits the designer to make in-line design or fabrication modifications.

SDA estimates the overall system size and power consumptions and time-of-flight in the substrate. The inputs to the SDA model are:

Die-Related Information: This is a set of information regarding the number of dies, die sizes, number of I/Os per die, and power dissipations per die.

Choice of Packaging:	The designer can select between a single-chip or a multichip packaging technology. Also, the designer has a choice of wire-bond, flip-chip, and tape automated bonding technologies.
Thermal Management:	Various choices of heat removal are also available to the designer at this level of design specification.
Substrate:	Various types of existing substrates are available to the designer. The designer can however, specify his own substrate specifications for analysis purposes.

SDA is similar to SUSPENS and AUDiT in concept but different in scope.

SDA and SUSPENS are mainly concerned with the partitioning of logic gates into chips and size estimation and package delays. SDA, on the other hand, assumes that the user already knows about the partitioning and the characteristics of the chips. It has a wider selection of packaging technologies and allows a mixture of them for evaluation.

The user has to input the design in terms of the number of chips and their electrical and geometrical characteristics and intended packaging technology. SDA then estimates the module area, power dissipation, package delay, and the module cost excluding the chip cost.

2.4 Nagesh Method

This work mainly attempts to compare the impact of various interconnect technologies on the system performance and interconnect density [25]. This work considers four types of bond/substrate technologies: wire-bond/pin-grid-array on PCB,

TAB/PCB, flip-chip/multilayer ceramic substrate, and flip-chip/si-on-si substrate. A new parameter is introduced by this work which is referred to as "number of electrically accessible circuits per nanosecond". This parameter is a measure of chip complexity in the form of number of circuit per chip, chip packing densities, and signal propagation time in the substrate.

The impact of the mentioned bond/substrate technologies are investigated for a hypothetical example. This example contains 200,000 logic gates and is assumed to be partitioned into nine VLSI chips. The electrically accessible gates per nanosecond" parameter is used to predict the number of signal layers for each case. The chip crossing delays (i.e. delay due to the chip interconnections) is also computed and compared.

2.5 Comparison

Although the above tools deal with packaging issues, their applications are quite different from each other. SUSPENS is a general-purpose simulation tool that does not solve any design parameters for the designer. It simply evaluates the interactions between a wide set of design parameters and their impact on the overall system performance. The SUSPENS model does not consider the choice of bonding technology and has a limited packaging model as compared to the others. It has been used successfully for the evaluation of some existing and futuristic microprocessors.

AUDiT, on the other hand, is an optimization tool. It is focused on the determination of the best design parameters based on a cost function. It is a useful tool when the best design parameters are needed for a given design. Unlike SUSPENS, the AUDiT model includes the bonding technology. However, the bonding parameter is not one of the parameters to be optimized and is assumed to be flip-chip.

SDA is probably the most versatile one as far as packaging-related parameters are concerned. It is also a simulation tool that is targeted exclusively at packaging evaluation. It covers a wide selection of packaging technologies, and "what if" packaging questions can be answered very easily. However, this tool requires that the system be already partitioned and the specifications of the dies be defined. SDA assumes that the designer is only interested in the impact of the different packages on the system performance.

All of the above tools only consider the " $\text{Performance}_{\text{package}}$ " when evaluating the impact of packaging parameters at the system performance. None of these methods takes into account the impact of " $\text{Performance}_{\text{die}}$ " term. They all assume that the performance of the die is independent from the choice of packaging.

CHAPTER 3

SIZE ANALYSIS

The size of a VLSI die continues to be an important issue to the VLSI designer because of the low manufacturing yield of large dies. The price of the silicon continues to grow exponentially with the die size with today's manufacturing techniques. Cost and ever increasing complexity of today's VLSI circuits require the VLSI designer to utilize properly and efficiently the available silicon on a die. This chapter explains how bonding technology may impact the size of VLSI dies.

3.1 Size Calculations of Flip-chip and Wire-bond ICs

The typical layout of a wire-bond IC is shown in Figure 10. In this type of layout, the circuit core is surrounded by the I/O pads on the perimeter of the chip. The size of the I/O pads for the wire-bond technology is bigger than those for flip-chip technology as shown in Figure 11. The size reduction that occurs when all of the wire-bond I/O pads are replaced with flip-chip I/O pads for a given die is:

$$\Delta Size_{due\ pads} = N_{w\ i/o} * (X_w Y_w - X_c Y_c)$$

where

$$N_{w\ i/o} = \text{Total number of the I/O pads}$$

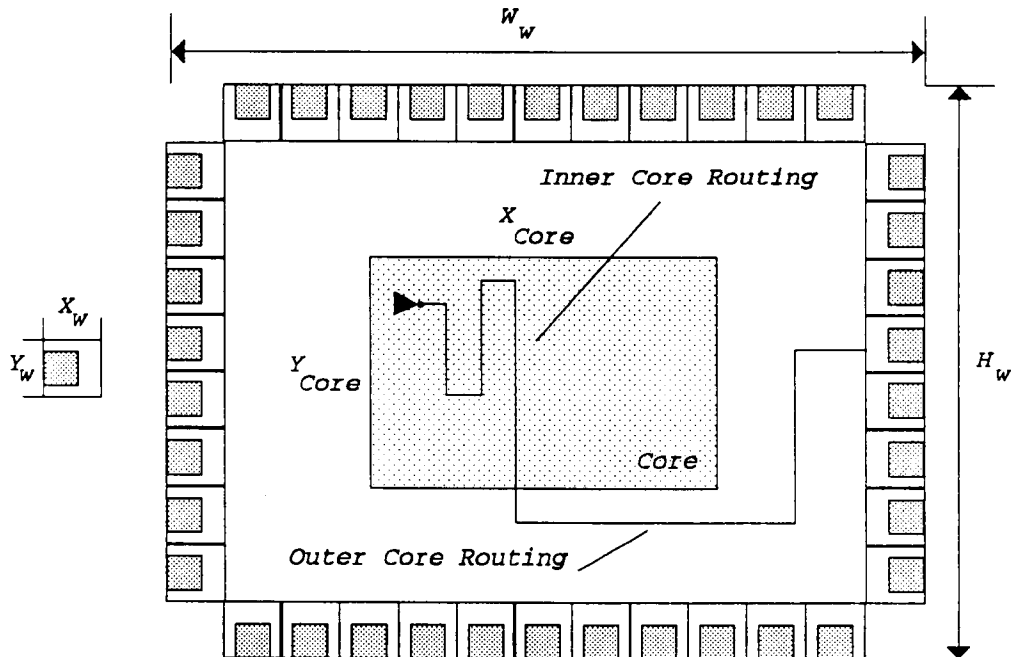


Figure 10. A Typical Wire-bond Chip Layout.

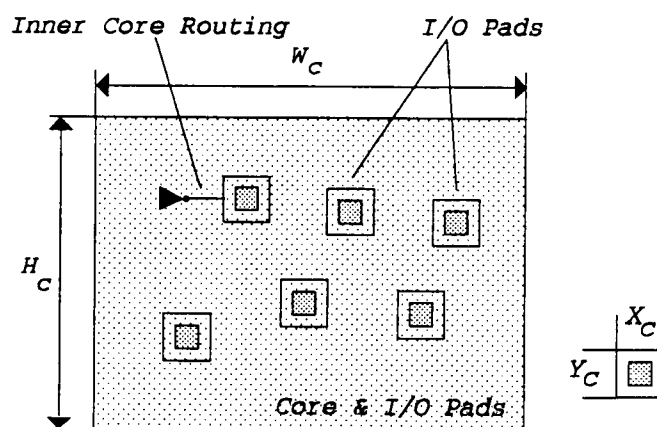


Figure 11. A typical Flip-chip Chip Layout.

X_w and Y_w = Size of the wire-bond I/O pads

X_c and Y_c = Size of the flip-chip I/O pads

It is also important to notice that, contrary to the wire-bond, the flip-chip I/O pads do not have to be placed on the perimeter of the chip. This allows the I/O pads to be placed within the chip core right next to the gate that needs to be connected to pad as shown in Figures 10 and 11. This simplifies the routing between the gates and the I/O pads, resulting in an additional reduction in size.

In general, the interconnection between a gate and an I/O pad consists of two segments: the inner-core and outer-core. The inner-core segment is the portion of the interconnection within the core while the outer-core is between the core and the pads. In a flip-chip layout, the inner-core routing can be minimized by placing the I/O pads right next to the gate as shown in Figure 11. The area between the core and the pads is due to the routing of the outer-core segment and the number of I/O pads. This area can be completely eliminated in a flip-chip IC by integrating the I/O pads within the core. This is a great saving in silicon area and generally occurs when there is a small core with a high number of I/O pins.]

Therefore, the size reduction that is observed when wire-bond technology is replaced by flip-chip technology is due to the following:

- 1) Smaller I/O pads
- 2) Elimination of the outer-core routing segment
- 3) Minimizing the inner-core routing segment

This reduction in size can be estimated as follows:

$$\begin{aligned} \Delta Size &= N_{w/o} [X_w Y_w - X_c Y_c] + [W_w H_w - X_{core} Y_{core} - N_{w/o} X_w Y_w] + KN_{w/o} X_{core} Y_{core} \\ \Delta Size &= N_{w/o} [-X_c Y_c] + [W_w H_w - X_{core} Y_{core}] + KN_{w/o} X_{core} Y_{core} \quad (1) \end{aligned}$$

where

X_{core} and Y_{core} = Size of the core

K = Proportionality factor

The $KN_{w/o}$ term shows the percentage of the core area that is used by the inner-core routing. The value of K has to be evaluated for various types of circuits and library cells experimentally.

3.2 Examples and Results

First, a simple example is introduced to illustrate clearly the impact of the bonding technology. A much more complex example is also given to show the impact for a large design. As an introductory example, a 16-bit full adder is designed and synthesized using the LAGER tool-set [26]. The design is based on a 2-micron standard-cell library [27]. The logic diagram for this adder is shown in Figure 12. The physical layouts for both wire-bond and flip-chip methods are shown in Figures 13 and 14. The wire-bond chip measures as:

$$W_w = 3252 \lambda$$

$$H_w = 3022 \lambda$$

$$X_{core} = 691 \lambda$$

$$Y_{\text{core}} = 851 \lambda$$

$$N_{w \text{ i/o}} = 51$$

where the flip-chip version measures:

$$W_c = 902 \lambda$$

$$H_c = 909 \lambda$$

The actual size reduction in this case is:

$$\Delta \text{Size} = (3252 * 3022) - (902 * 909) = 9,007,626 \lambda^2$$

The estimation from equation (1) yields:

$$\Delta \text{Size} = 8,913,919 + 588,041 * K * N_{w \text{ i/o}} \lambda^2$$

Equating the above two equations yields:

$$K * N_{w \text{ i/o}} = 0.1594 \lambda^2$$

$$K = 0.0031 \lambda^2$$

This shows that the inner-core routing takes 16% more of the core in the wire-bond layout than the flip-chip layout. Even if one ignores the contribution of the inner-core routing, the estimated size reduction will be $8,913,919 \lambda^2$ which is within 1% of the actual reduction.

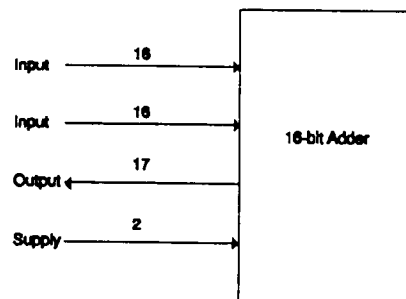


Figure 12. Logic Diagram of a 16-bit Adder.

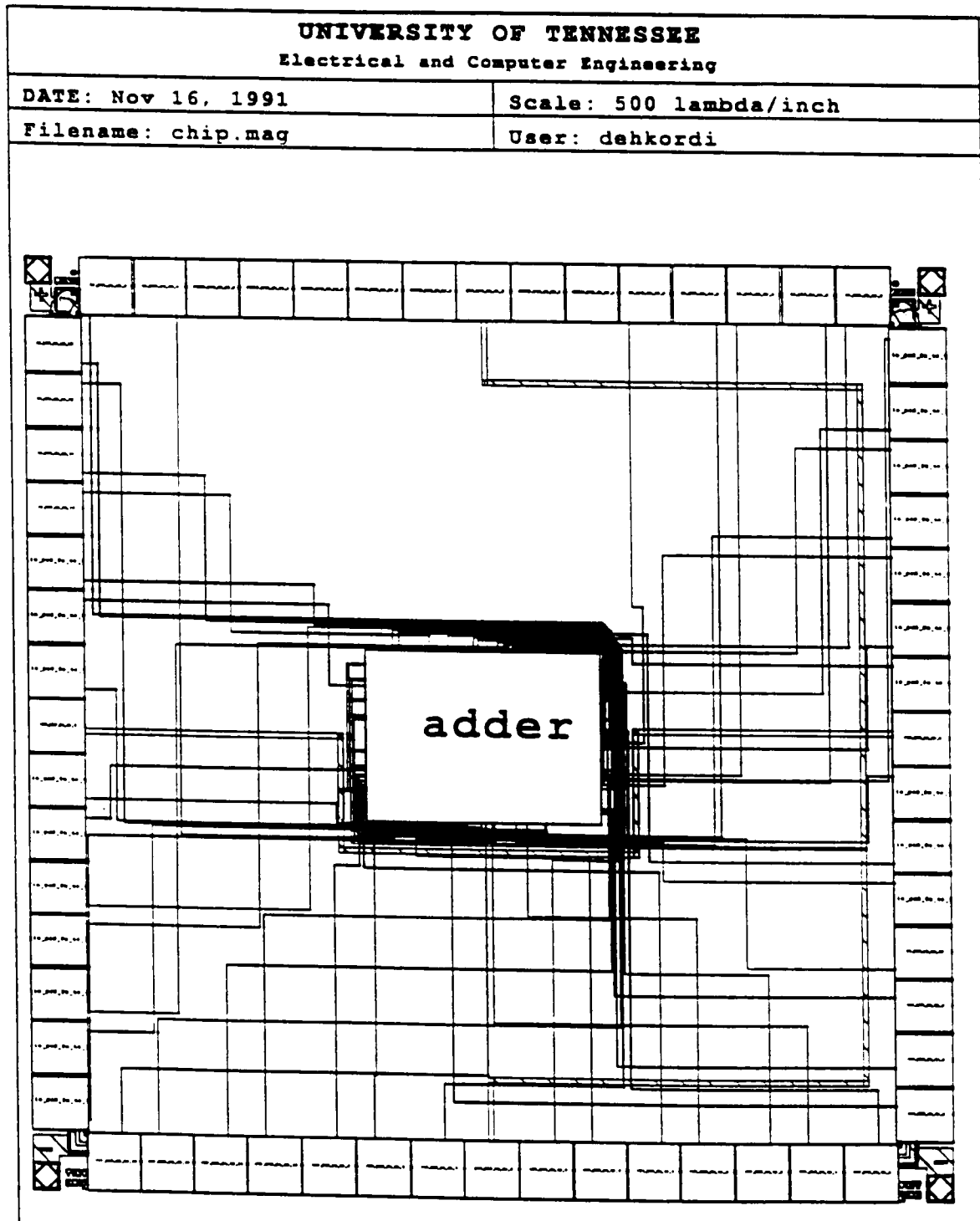


Figure 13. Layout of a 16-bit full adder
(wire-bond version)

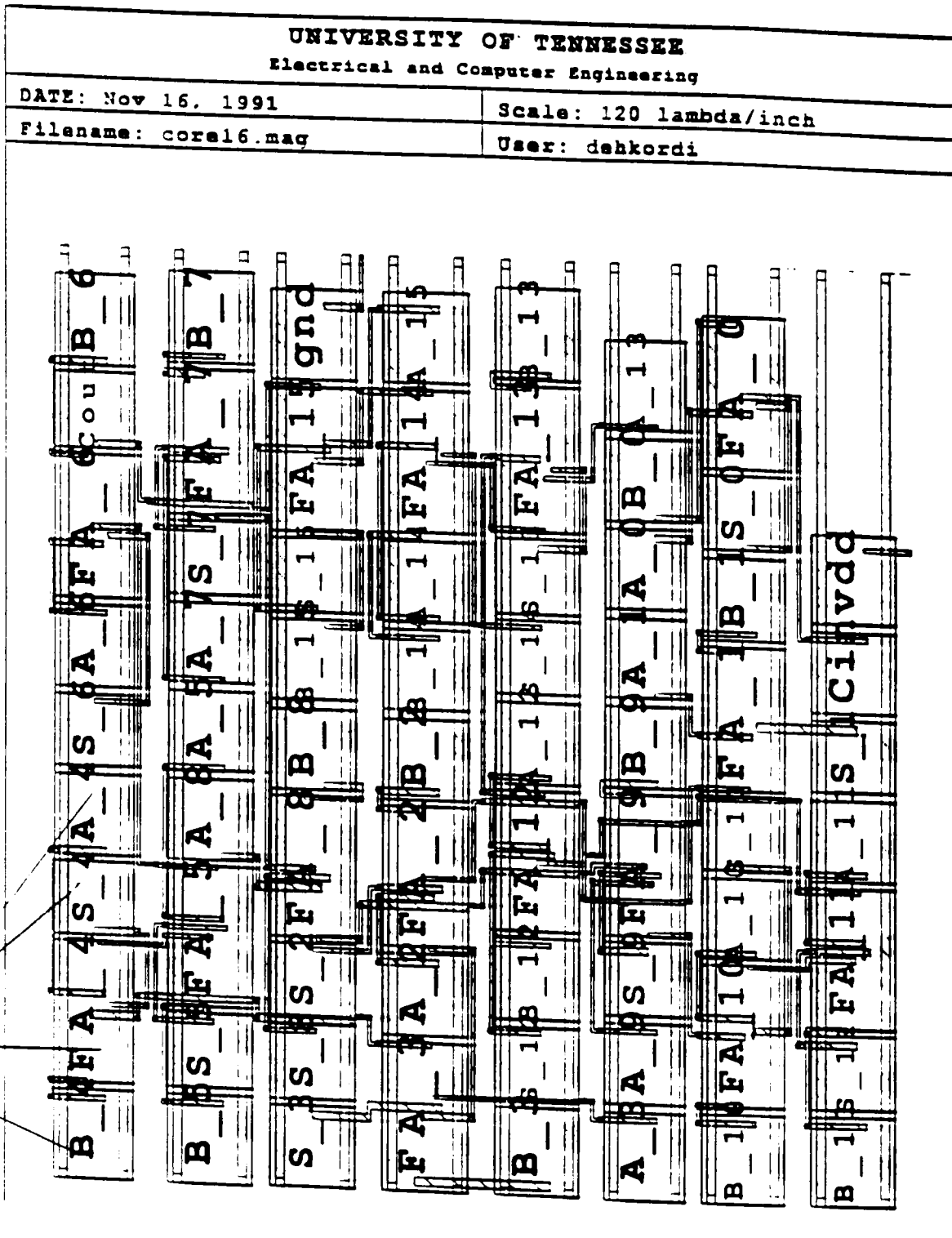


Figure 14. Layout of a 16-bit full adder (flip-chip version)

A three chip-set image-processor was also synthesized for both wire-bond and flip-chip technologies. These chips represent more realistic examples of typical VLSI IC complexity, size and I/O. The layouts for these chips (named: PE, IO, CTL) for wire-bond and flip-chip methods are shown in Figures 15 through 20. These chips were also synthesized using the Lager CAD tool-set based on the standard-cell library. All layouts are scaled for maximum visibility. The PE chip is designed for a 1.2-micron process due to its large size. The IO and CTL chips are, however, designed for 2-micron technology.

A visual comparison of the two different approaches (i.e. wire-bond vs. flip-chip) reveals several interesting features. The I/O pads are not quite as visible for the flip-chip as compared to the wire-bond. The reason for this is because the I/O pads are integrated within the core circuitry. The integration is accomplished by developing a new technique for placing the I/O pads as close as possible to the input/output driving gates. This involved redesigning the flip-chip I/O pads to conform to the standard-cell layout specification, and then adding them to the standard-cell library. Thus, these I/O pad cells were included along with the rest of the core circuitry at the lowest levels of the structural description language. Then, it was the responsibility of the standard-cell layout generator to place and route the I/O pads for optimum interconnection.

These measurements are shown in Table 2. The column labeled as "chip" contains the entire chip measurement in lambda (λ). The "core" column shows the size of the core, and the "I/O pad" is simply the difference between the chip and the core sizes.

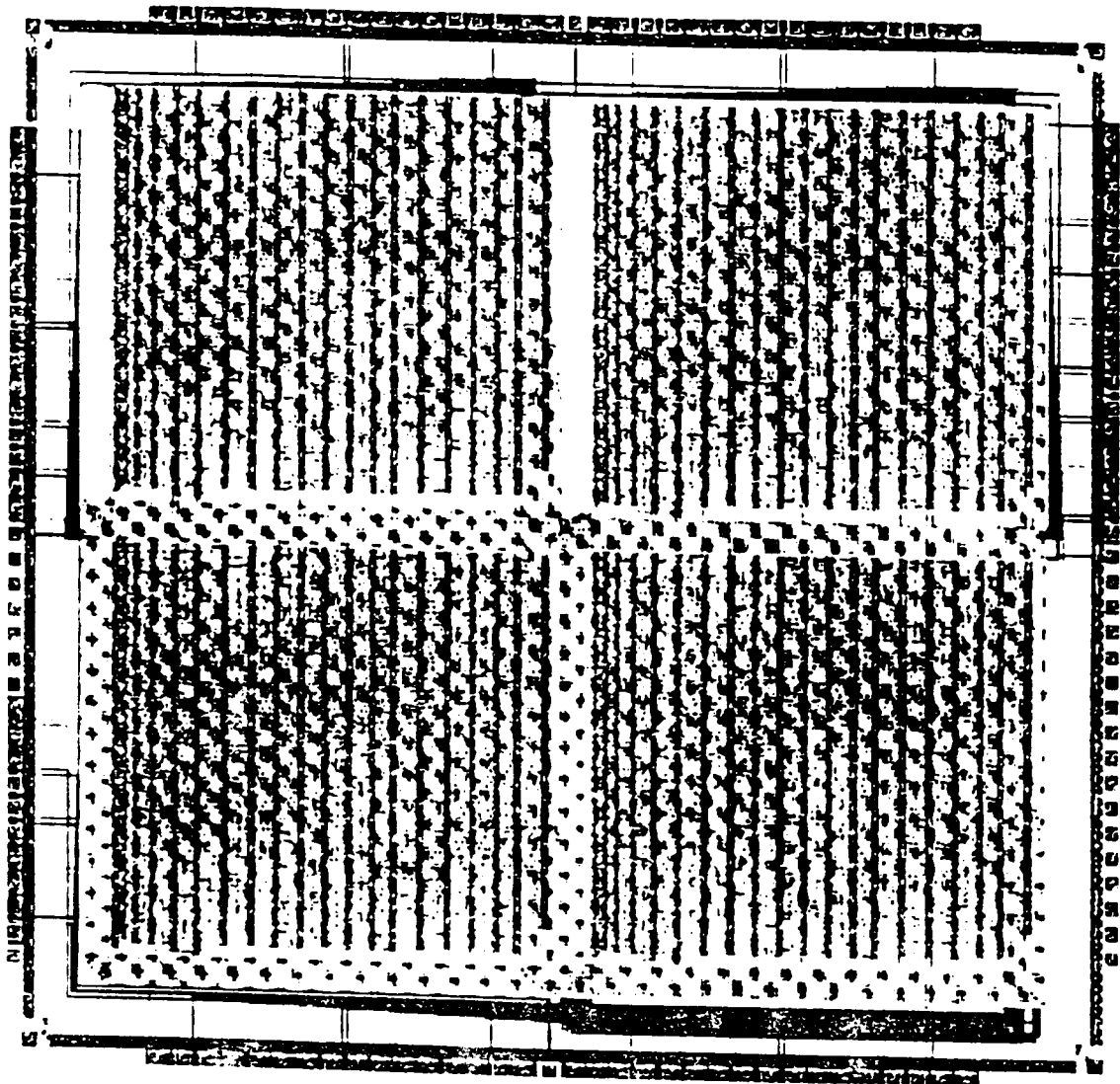


Figure 15. Layout of the processing element (PE) chip (wire-bond version).

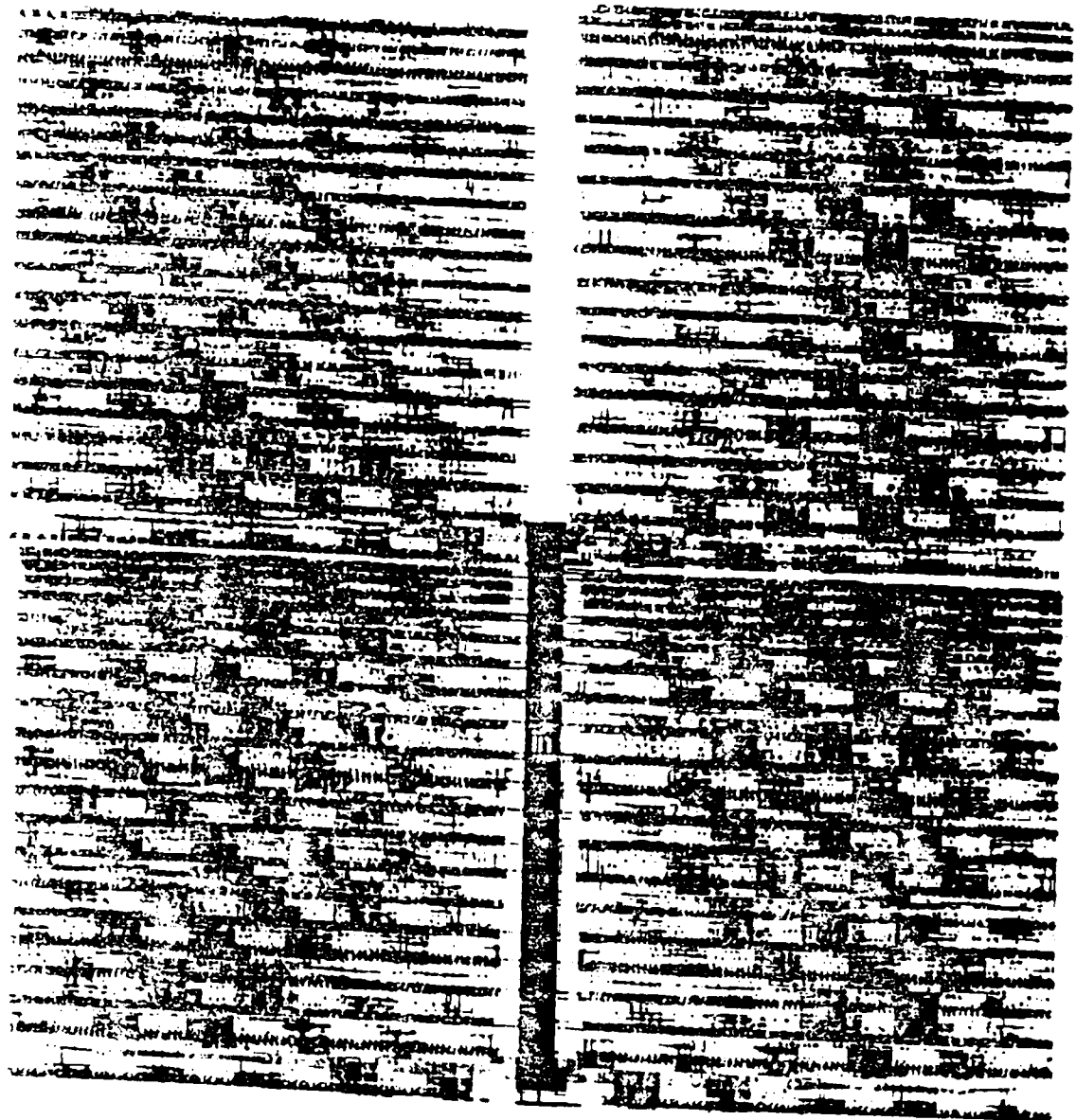


Figure 16. Layout of the processing element (PE) chip (flip-chip version).

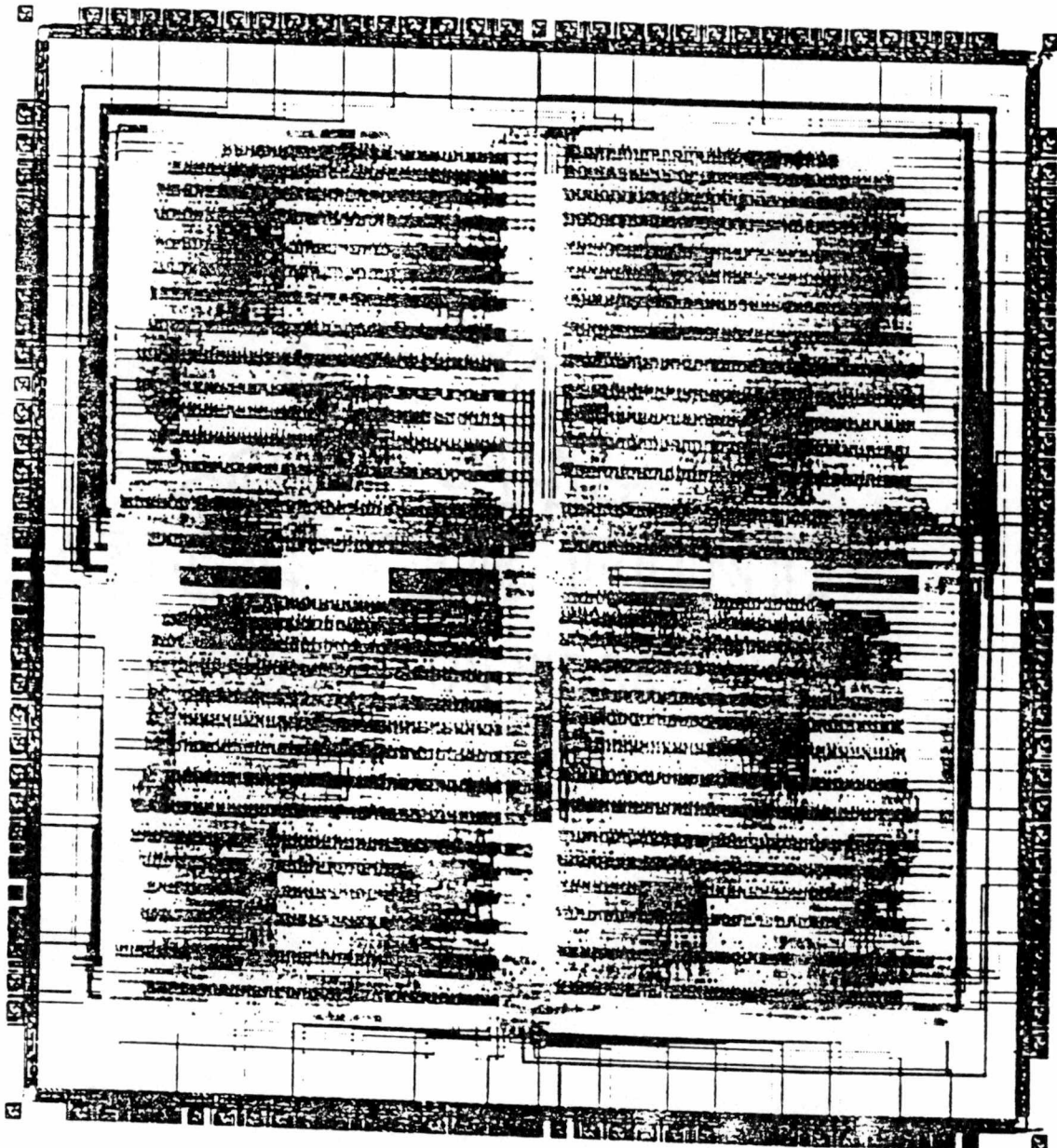


Figure 17. Layout of the input/output (IO) chip (wire-bond version).

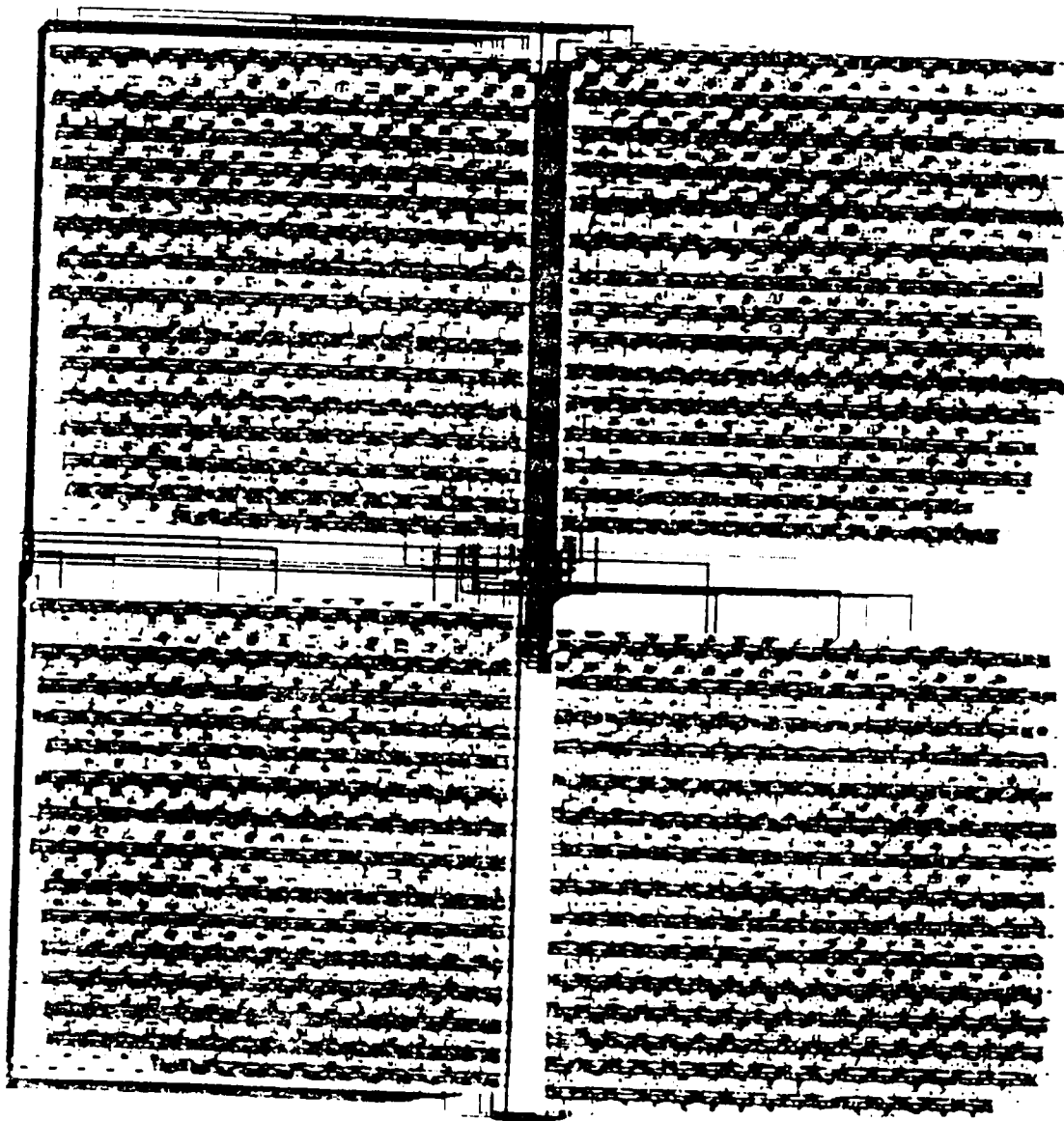


Figure 18. Layout of the input/output (IO) chip (flip-chip version).

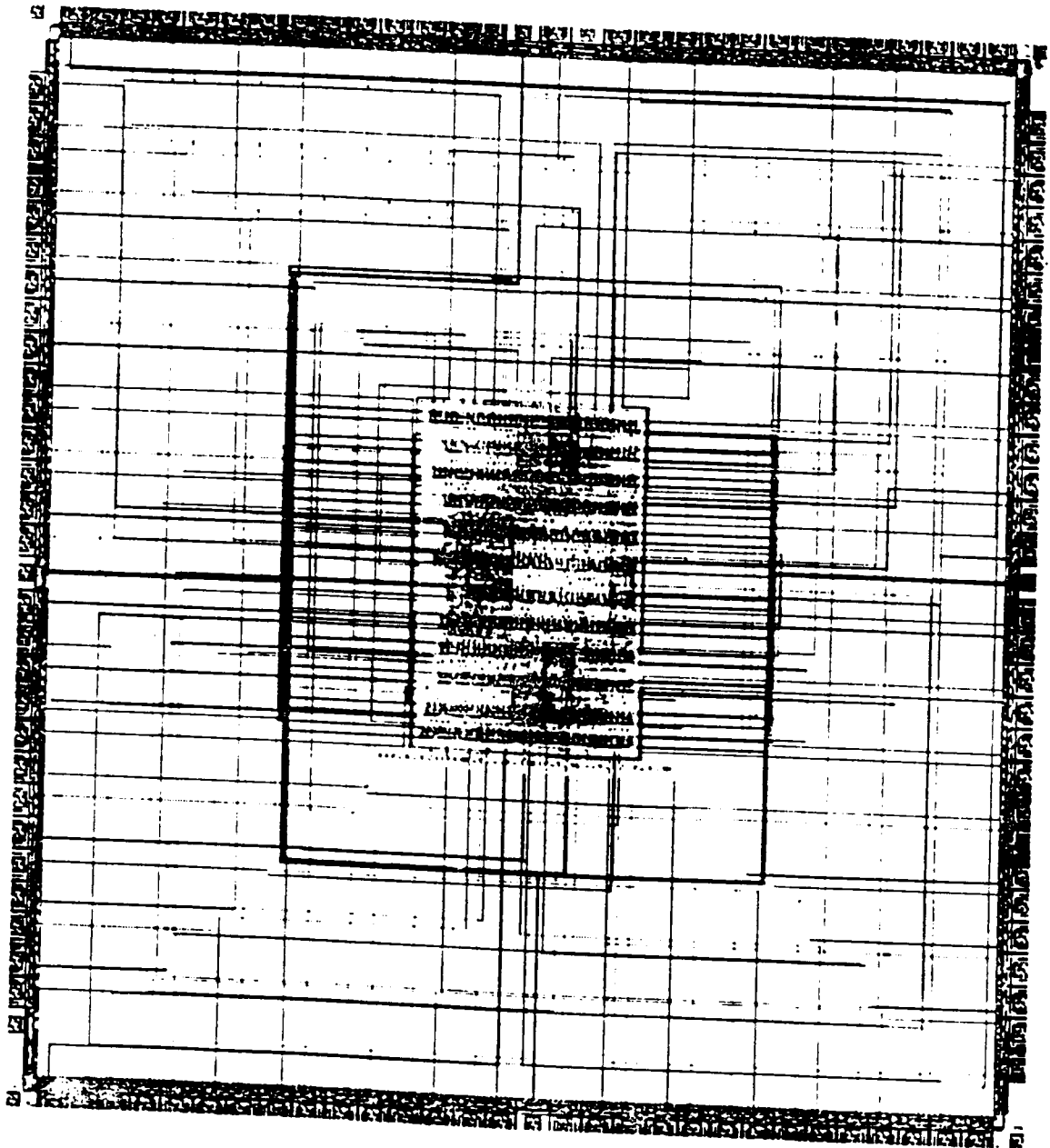


Figure 19. Layout of the controller (CTL) chip (wire-bond version).

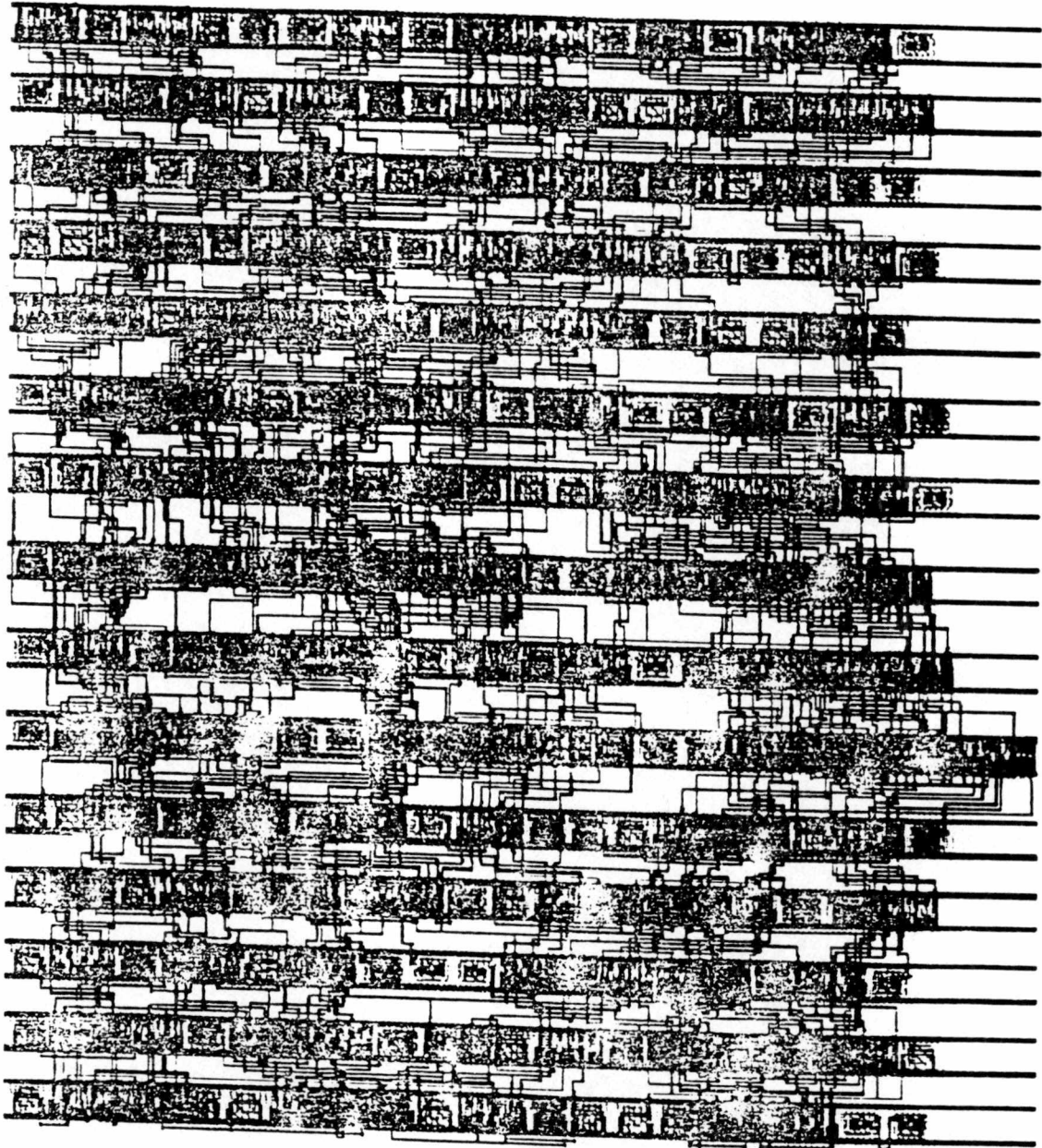


Figure 20. Layout of the controller (CTL) chip (flip-chip version).

Table 2. Dimensions and Area (in λ and λ^2) of the PE, IO, and CTL Chips.

	Chip	Core	I/O Pads
PE (wire-bond)	12275 x 13022 159,845,050	10432 x 11300 117,881,600	41,963,450
PE (flip-chip)	10570 x 10314 109,018,980	10662 x 9948 106,065,576	2,953,404
IO (wire-bond)	7458 x 7028 52,414,824	6022 x 5752 34,638,544	17,776,280
IO (flip-chip)	5578 x 5854 32,653,612	5274 x 6086 32,097,564	556,048
CTL (wire-bond)	6858 x 6428 44,083,224	2107 x 1392 2,932,944	41,150,280
CTL (flip-chip)	1914 x 1779 3,405,006	1510 x 1334 2,014,340	1,390,666
ALL (wire-bond)	256,343,098	155,453,088	100,890,010
ALL (flip-chip)	145,077,598	140,177,480	4,900,118

Charts comparing the size for each set of chips are shown in Figures 21 through 24. It is notable that these chips represent three distinct types of chips as far as core size and the number of I/Os are concerned. For example, the PE chip is a core-dominated chip in which the size of the chip is due to the size of the core. For this particular chip, the core and the I/O pads take 74% and 26% of the chip area respectively. As the PE wire-bond layout suggests, the number of I/Os does not dictate what the chip size should be. This is quite obvious by the number of extra I/O pads that are not used by the core. On the other hand, the CTL chip is an I/O-dominated chip. This is the type in which the size of the chip is mainly determined by the number of I/Os rather than the core size. For this chip, the core and I/O pads take up 7% and 93% of the chip area respectively. As can be seen in the CTL wire-bond layout, the size of the chip is mainly due to the outer-core routing rather than the core size. The IO chip is the most balanced chip as far as the core size and the number of I/Os are concerned. The area of the chip is distributed 66% and 34% between the core and the I/O pads respectively.

The core size in the flip-chip approach reveals some interesting features. The core sizes in all three chips are smaller than in the wire-bond counterparts. This is simply due to the minimization of the inner-core routing permitted by the flip-chip technology. It is also interesting to note that the PE and IO chip sizes of the flip-chip versions are even smaller than the core sizes of the wire-bond versions. Again, this shows how much the inner-core routing can take up for a fairly large chip with a high number of I/Os.

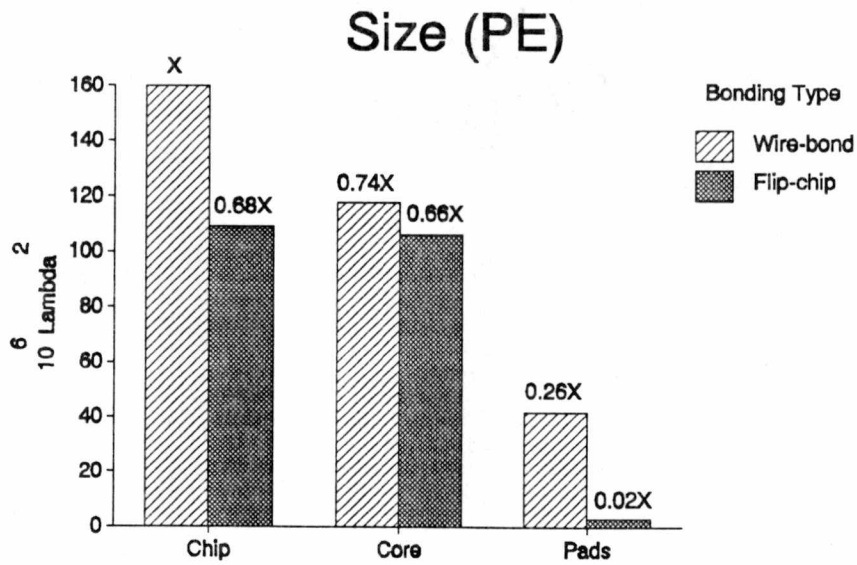


Figure 21. Size Comparison of PE Chips for wire-bond and flip-chip.

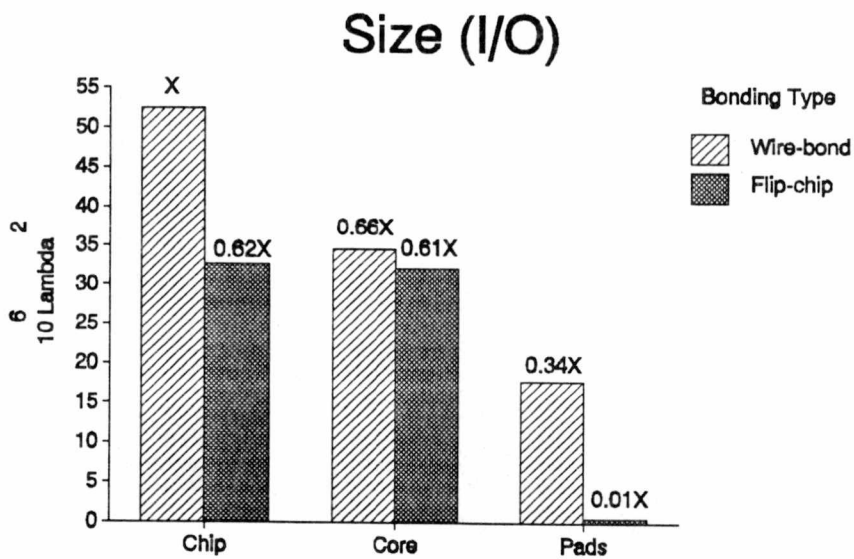


Figure 22. Size Comparison of IO Chips for Wire-bond and Flip-chip.

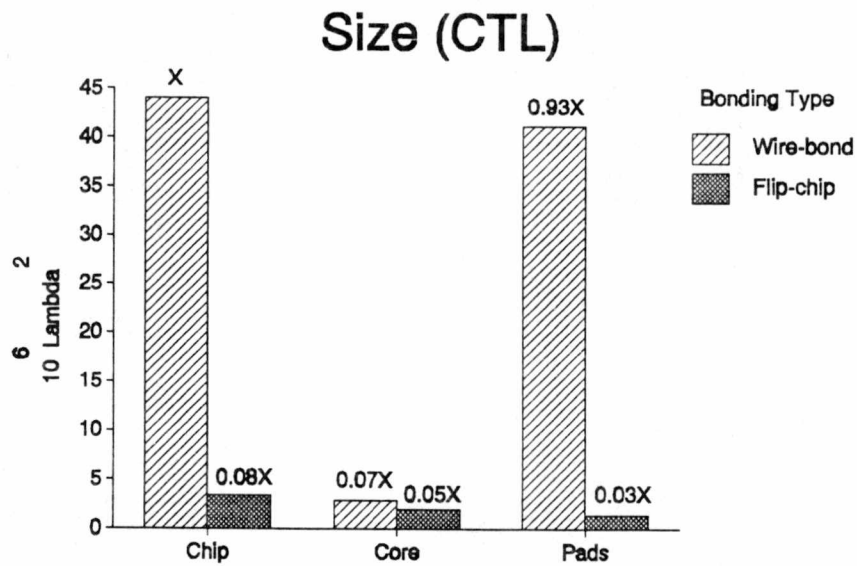


Figure 23. Size Comparison of CTL Chips for Wire-bond and Flip-chip.

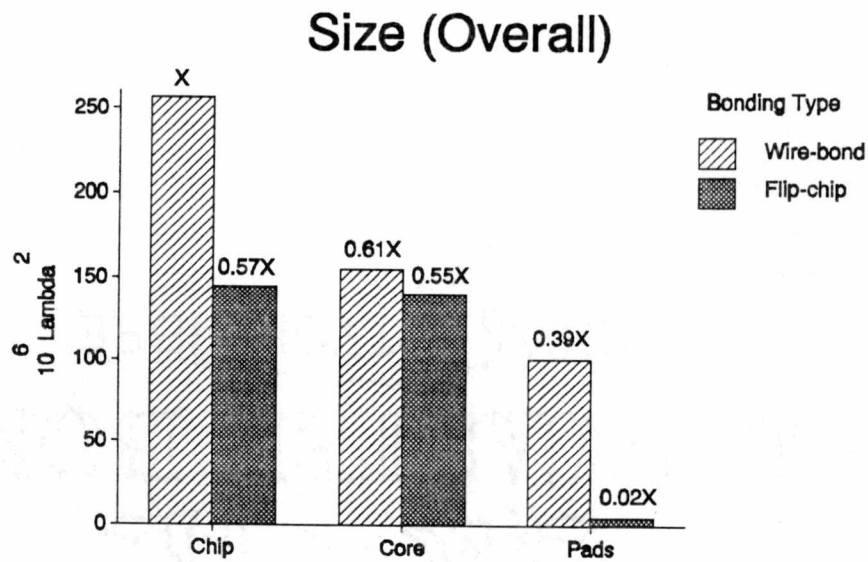


Figure 24. Size Comparison of All Chips for Wire-bond and Flip-chip.

By comparing the wire-bond and the flip-chip layouts and size measurements, the following conclusions can be drawn:

- 1) The outer-core routing is completely eliminated in the flip-chip method.
This could be very advantageous when the chip is I/O-dominated. This advantage decreases as the chip type changes from I/O-dominated to one that has balanced I/O and core to one that is core-dominated.
- 2) The inner-core routing is also minimized for the flip-chip method as compared with the wire-bond method. This minimization is obvious by comparing the number of high density interconnections present within the center of the chip. This minimization is measured to be as much as 8% of the total area for the PE chip and 6% for all three chips taken together.
- 3) The complete chip sizes for the flip-chip method are measured to be consistently smaller than the wire-bond in all three cases. These sizes are reduced by as much as 92% for the CTL chip and 43% for all three chips together.

Equation (1) has been used to estimate the size reduction (or could be thought of as the flip-chip size estimation) that the flip-chip method causes. These estimations are tabulated in Table 3. The first column represents the true reduction in size as measured. The second column estimates the relative size reduction. For this estimation, the impact of the inner-core routing is ignored ($K=0$), resulting in an error which is displayed in the third column. The reader should keep in mind that this error shows what percentage of the wire-bond core is actually used for the inner-routing of the I/O pads. The number of I/O signals is presented in the fourth column followed by the

proportionality constant "K". It should be noted that this value is fairly constant for these three chips, which is a measure of the performance of the standard-cell layout generator.

Table 3. Size Reduction Estimations.

	True Reduction	Estimated Reduction(K=0)	Error	N _{w i/o}	K
PE	50,826,070	41,261,210	18%	110	0.00074
IO	19,761,212	17,093,192	13%	107	0.00078
CTL	40,678,218	40,409,736	1%	116	0.00079

CHAPTER 4

POWER CONSUMPTION ANALYSIS

The sub-micron structures of today's technology have resulted in very dense and high speed integrated circuits. The high transistor-density has made power dissipation an important design consideration. Battery-backed and hand-held electronic instruments have also been gaining popularity in recent years. The demand for a low power-consuming design is more than ever. The purpose of this chapter is to investigate how the bonding technology may impact the power consumption of a VLSI die.

4.1 CMOS Power Estimation

In CMOS circuits, the power consumption of a circuit is due to three sources: static, dynamic, and short circuit dissipations. Therefore, power consumption is:

$$P = P_{dynamic} + P_{static} + P_{sc}$$

where P_{static} is due to the reverse bias leakage currents between diffusion regions and the substrate. The total static power dissipation for a circuit is:

$$P_{static} = \sum_{j=1}^{N_t} I_{leakage(j)} * V_{dd(j)}$$

where

N_t = total number of transistors in the circuit

$I_{leakage(j)}$ = leakage current in the j th transistor

$V_{dd(j)}$ = the supply voltage in the j th transistor

The short circuit dissipation (P_{sc}) occurs only during a transition in the circuit.

This is due to the complementary nature of CMOS circuits where both the pMOS and nMOS transistors conduct for a short period of time resulting in a low-resistance path between V_{dd} and ground during a transition. P_{sc} can be estimated as:

$$P_{sc} = \sum_{j=1}^{N_t} I_{avg\ short(j)} * V_{dd(j)}$$

where $I_{avg\ short}$ is the average short current during a transition given by [28].

The dynamic power dissipation ($P_{dynamic}$) also occurs only during a transition.

This power consumption is due to the charging and discharging of the output capacitive loads. For a CMOS circuit, this dissipation can be estimated as:

$$P_{dynamic} = \sum_{j=1}^{N_t} \frac{1}{2} * V_{dd(j)}^2 * F_{(j)} * C_{(j)}$$

where

$F_{(j)}$ = the operating frequency of the j th transistor

$C_{(j)}$ = the capacitive load of the j th transistor

Therefore, the total power consumption can be estimated as:

$$P = \sum_{j=1}^{N_t} I_{leakage(j)} * V_{dd(j)} + \sum_{j=1}^{N_t} I_{avg\ short} * V_{dd(j)} + \sum_{j=1}^{N_t} \frac{1}{2} * V_{dd(j)}^2 * F_{(j)} * C_{(j)}$$

In general, P_{static} is negligible compared with P_{dynamic} , and P_{sc} is only a fraction of P_{dynamic} [29][30]. Therefore, the power calculation can be simplified to estimating the P_{dynamic} . This estimation can be very complicated because it depends not only on the circuit but also on the characteristics of the input signals (i.e. in order to estimate $F_{(j)}$). Previous work such as [31] use probability functions to describe the transition of the input signals. These probability functions, along with the specific type of logic gates in the circuit, are used to determine $F_{(j)}$ more accurately. Other work such as [32], compute the input signal sequence that dissipates the maximum power for a given logic circuit. However, these solutions can become very computationally intensive and require consideration of the logic operations of the circuit in hand. For this work, the characteristics of the input signals and the logic operations of the circuit are not considered. This is for the sake of simplicity and the fact that only a relative measure of power consumption is needed for comparison purposes rather than the actual absolute measurements. Therefore, the power consumption that is used in this work is calculated as :

$$P = \sum_{j=1}^{N_t} \frac{1}{2} * V_{dd(j)}^2 * (F * A) * C_{(j)}$$

$$P = K * V_{dd}^2 * F * \sum_{j=1}^{N_t} C_{(j)}$$

$$P = K * N_t * V_{dd}^2 * F * C_{\text{avg}}$$

where

K = the percentage active time of a transistor on average

N_t = Total number of transistors

C_{avg} = average capacitive load

4.2 Power Calculation of Flip-chip and Wire-bond ICs

The total power consumption of a chip can be divided between its core and I/O pads:

$$P_{chip} = P_{core} + P_{pad\ total}$$

$$P_{chip} = P_{core} + N_{w\ i/o} * P_{pad}$$

where

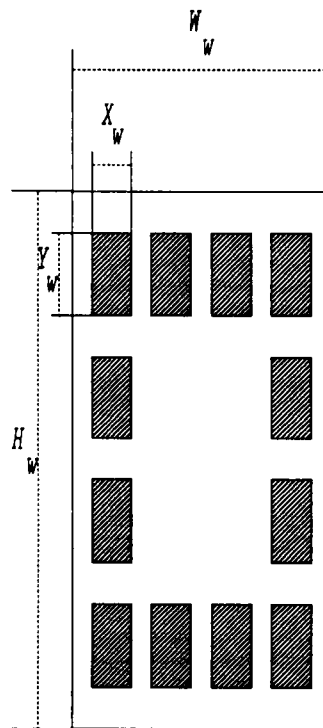
$N_{w\ i/o}$ = the total number of I/O pads

In a wire-bond packaging, the I/O pad drivers are placed on the periphery, as shown in Figure 25. These drivers are originally designed so that they can drive off-chip interconnections on a printed circuit board. For a given die size of W by H , the maximum number of the I/O pads can be calculated as follows:

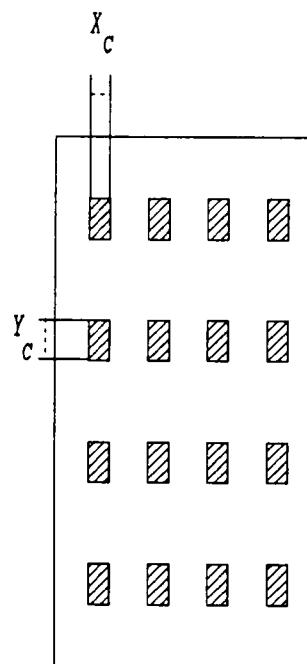
$$N_{w\ i/o} = \frac{2W}{X_w} + \frac{2H}{Y_w} - 8$$

Assuming that there are N_{tw} transistors per I/O pad with $C_{avg\ w}$ capacitive load, then the power consumption per I/O pad of a wire-bond chip can be estimated as :

$$P_{pad} = K * N_{tw} * C_{avg\ w} * V^2$$



Wire-Bonding I/O Pads Placement



Flip-Chip I/O Pads Placement

Figure 25. I/O Pad Drivers for Wire-bond and Flip-chip Technologies.

Therefore, the maximum power consumption of the wire-bonded I/O pads for a die size of W by H is as follows:

$$P_{pad\ total} = N_{w\ i/o} * P_{pad}$$

$$P_{pad\ total} = \left(\frac{2W}{X_w} + \frac{2H}{Y_w} - 8 \right) * (K * N_{tw} * C_{avg\ w} * V^2 * F)$$

In a flip-chip I/O pad driver, there are N_{tc} transistors driving $C_{avg\ c}$ capacitive loads. These I/O pad drivers are designed for lower capacitance interconnections on the MCM substrate. Consequently, the pads are smaller and less power-consuming compared with the wire-bond pads. Therefore, the total power consumption for the pads is reduced by:

$$\Delta P = (N_{tw} * C_{avg\ w} - N_{tc} * C_{avg\ c}) * (K * V^2 * F) * N_{w\ i/o} \quad (2)$$

$$\Delta P = (N_{tw} * C_{avg\ w} - N_{tc} * C_{avg\ c}) * (K * V^2 * F) * \left(\frac{2W}{X_w} + \frac{2H}{Y_w} - 8 \right)$$

The total I/O pad power consumptions for four different popular die sizes are shown in Figure 26. It is interesting to note that the power reduction is a linear function of the chip size. In all cases, the following values are used for the calculations:

$$F = 10 \text{ MHz}$$

$$C_{avg\ c} = 0.222 \text{ pf}$$

$$K = 0.00023$$

$$X_w = 210 \lambda$$

$$N_{tw} = 24$$

$$Y_w = 210 \lambda$$

$$N_{tc} = 2$$

$$C_{avg\ w} = 0.945 \text{ pf}$$

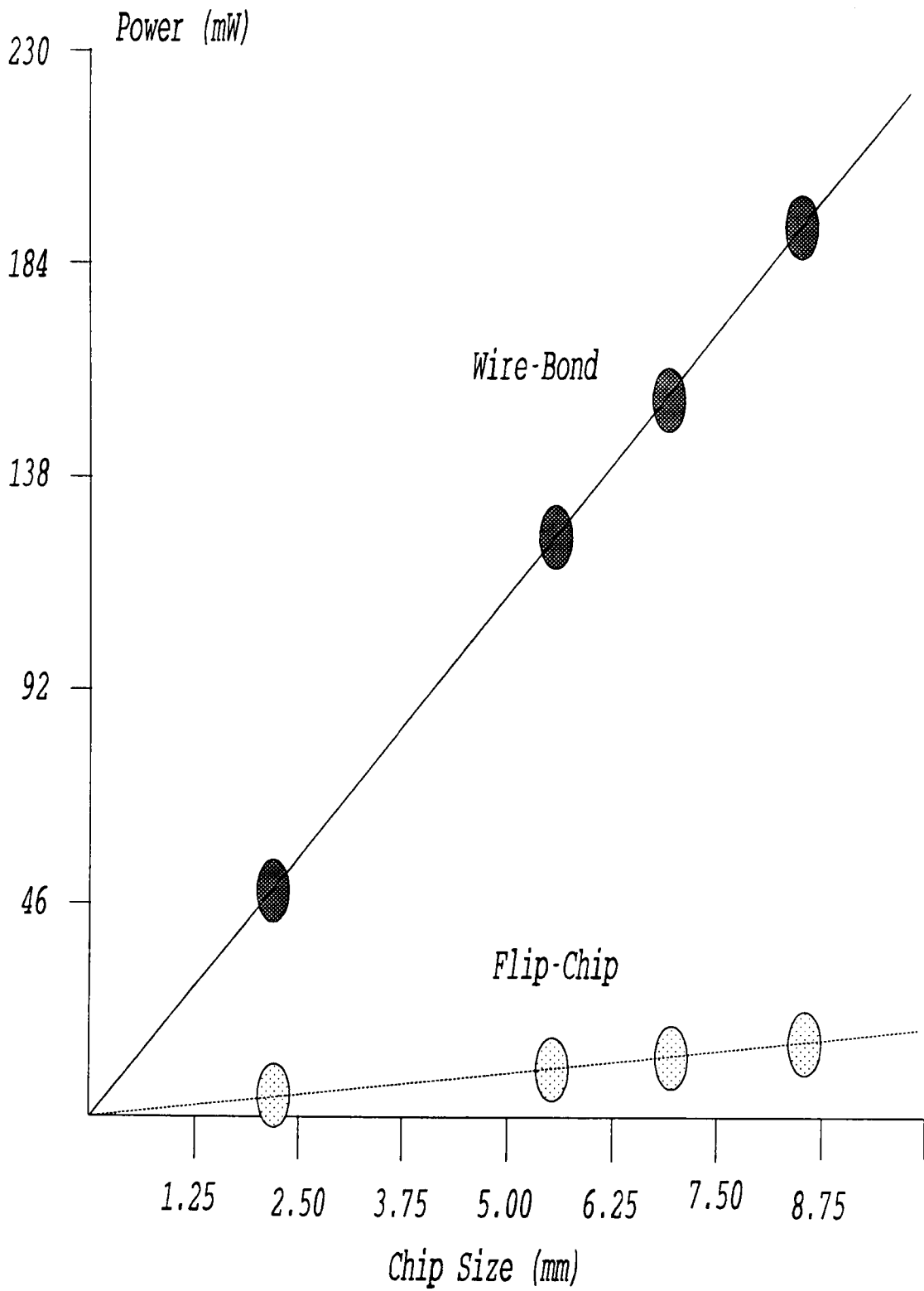


Figure 26. I/O Pad Power Consumptions for Different Chip Sizes.

4.3 Examples and Results

The 16-bit adder of the previous chapter is used as a simple example. The flip-chip approach simply replaces the wire-bond pad drivers with the less power-consuming flip-chip drivers and places the pads within the core. The wire-bond chip measures 3252λ by 3022λ , and the following power dissipations are observed:

$$P_{\text{core}} = 2.2 \text{ mW}$$

$$P_{\text{pads}} = 69.9 \text{ mW}$$

$$P_{\text{chip}} = 72.1 \text{ mW}$$

The flip-chip version yields the following measurements:

$$P_{\text{core}} = 2.1 \text{ mW}$$

$$P_{\text{pads}} = 1.6 \text{ mW}$$

$$P_{\text{chip}} = 3.7 \text{ mW}$$

Using the equation (2), the power reduction is estimated as:

$$\Delta P = 65.2 \text{ mW}$$

where as the measured value is:

$$\Delta P = 72.1 - 3.7 = 68.4 \text{ mW}$$

and the relative error is:

$$\xi = (68.4 - 65.2) / 68.4 = 5\%$$

It is interesting to note that the flip-chip version has resulted in a **19X** reduction in total power consumption compared with the wire-bond version. The equation (2) estimates this power reduction fairly well; however, it does not account for the different physical core layouts of the wire-bond and flip-chip.

This introduces an error into the estimation done by equation (2), which is highly dependent on the circuit and the layout generator used.

Table 4 shows the result of the power measurements on the three chip-set. All the measurements are in milliwatts and have been calculated at an operating frequency of 10 Mhz. The "chip" column represents the total power consumption of the chip, whereas the other two columns show how the consumption is divided between the core and I/O pads. Table 5 shows how close, the power reduction is estimated.

Charts comparing the power dissipation for each set of chips are shown in Figures 27 through 30. The following conclusions can be made by from these charts:

- 1) The CTL is an I/O-dominated chip where the power consumption due to the pads is considerably higher than of the core. In this type of chip, the power reduction is measured to be 90% as expected.
- 2) The PE and the IO chips also show a large power reduction of 61% and 59% respectively. Although the PE chip is designed for possible 1.2-micron fabrication, the power calculation is based on 2-micron parameters.
- 3) Considering all three chips at the same time, the power reduction is as much as 55%.

Table 4. The Power Consumption Measurements.

	Chip	Core	I/O Pads
PE (wire-bond)	671.9	419.2	252.7
PE (flip-chip)	412.9	407.5	5.4
IO (wire-bond)	370.5	225.8	145.7
IO (flip-chip)	220.3	216.9	3.4
CTL (wire-bond)	173.5	15.2	158.3
CTL (flip-chip)	17.9	14.2	3.7
ALL (wire-bond)	1215.9	660.2	556.7
ALL (flip-chip)	651.1	638.6	12.5

Table 5. Power Reduction Estimation

	Measured Reduction	Estimated Reduction	Relative Error (%)	Number of IO
PE	259.0	234.4	10%	110
IO	150.2	136.8	9%	107
CTL	155.6	148.3	5%	116

Power Consumption (PE)

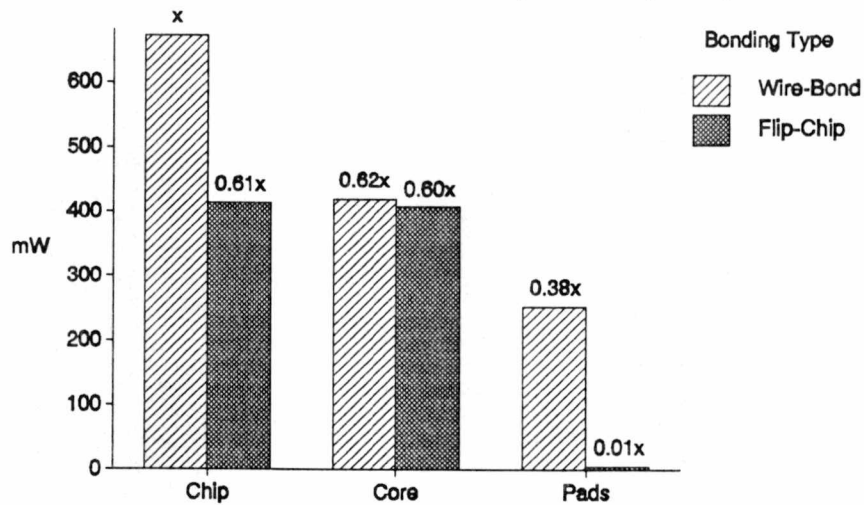


Figure 27. Power Consumption of PE chips for Wire-bond and Flip-chip.

Power Consumption (IO)

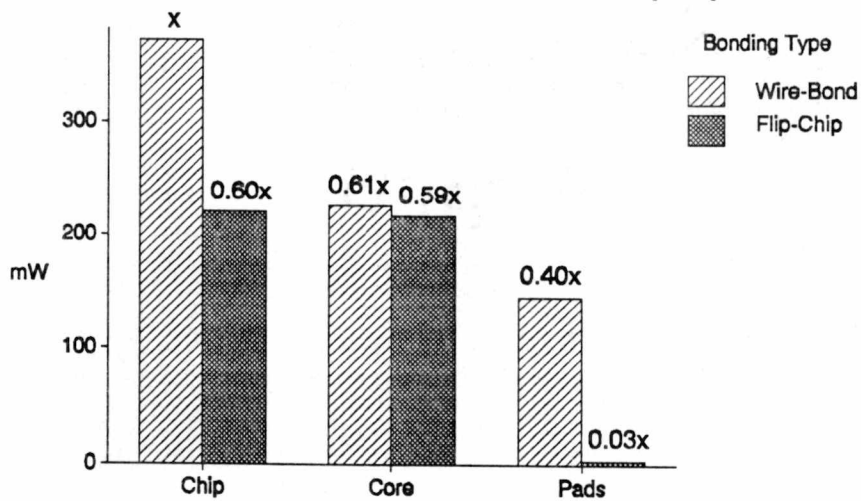


Figure 28. Power Consumption of IO chips for Wire-bond and Flip-chip.

Power Consumption (CTL)

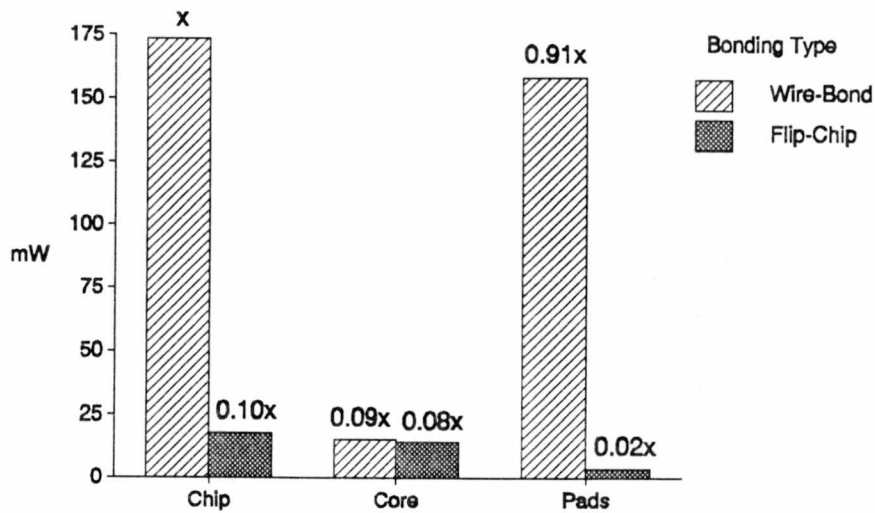


Figure 29. Power Consumption of CTL chips for Wire-bond and Flip-chip.

Power Consumption (Overall)

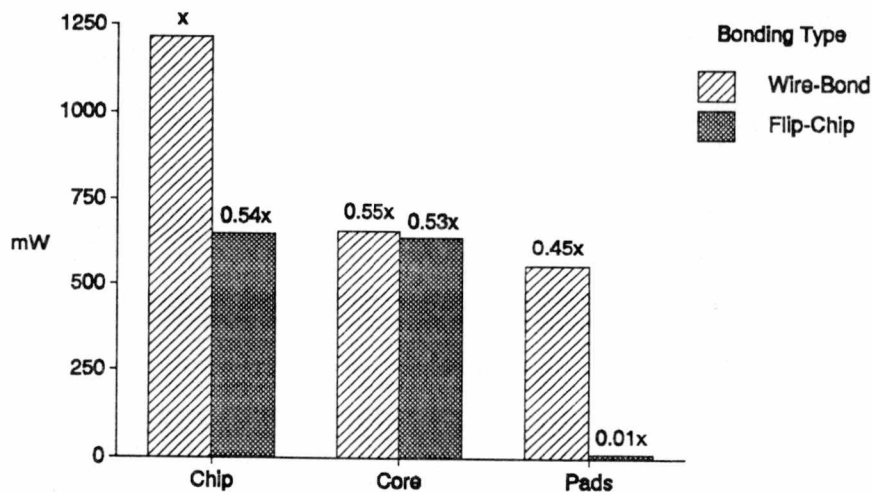


Figure 30. Power Consumption of ALL chips for Wire-bond and Flip-chip.

CHAPTER 5

TESTING ANALYSIS

Functional testing of digital systems continues to be a challenging job for designers. Design for testability (DFT) is a technique that has emerged to answer this challenge [33]. DFT encourages the designer to create testable designs by considering the testing issues at an early stage of a design.

The word "testability" tends to be used somewhat imprecisely. In general, it could be applied to any or all of the following areas:

- 1) Test generation
- 2) Test coverage
- 3) Test applications
- 4) Test cost

In this work, the word "testability" simply refers to the test coverage for detection of a set of stuck-at-zero or stuck-at-one models. In this model, the test coverage is calculated as the ratio of detected faults to all the potential faults within the circuit. The intention of this chapter is not to introduce any new DFT technique or to explore the world of testing; rather, it introduces the reader to some of the fundamentals of testing and shows how packaging may impact the testability of a VLSI chip.

5.1 Testability Measures

In order to investigate the impact of packaging on the testability of a VLSI chip, the testability measures should be understood. These measures quantify the testability of a circuit without actually completing the tasks of test generation and evaluation. These techniques generally rely on two concepts: controllability and observability.

Controllability refers to the ability to produce a desired logic level at a specific internal node through the primary input to the circuit. Observability refers to the ability to observe the logic level of an internal node through a primary output of the circuit. Therefore, the nodes driven by the primary inputs have the highest controllability, whereas the nodes driving the primary outputs have the highest observability.

There are various testability measure algorithms that use the concept of controllability and observability to estimate testability [34][35][36][37]. There have also been some statistical methods to shown a monotonic relationship between these measures and the actual test coverage of a circuit [38]. These algorithms, assign a controllability (CY) and observability (OY) value to each node in the circuit based on the logic components between the node and the primary inputs and outputs. Then, the testability of the circuit can be calculated as a function of the controllability and observability of all the nodes in the circuit.

For example, the CAMELOT algorithm [34] assigns a figure-of-merit between 0 and 1 for controllability and observability ($0 \leq CY \leq 1$, $0 \leq OY \leq 1$). The higher values of CY and OY are, The easier it is for a node to be controlled or observed. The testability (TY) at any node then may be computed as:

$$TY_i = CY_i * OY_i$$

and the overall testability can be computed as:

$$TY_{overall} = \frac{\sum_{i=1}^N TY_i}{N} = \frac{\sum_{i=1}^N CY_i * OY_i}{N}$$

where N is the total number of nodes in the circuit. The $TY_{overall}$ also has a value between 0 and 1 which reflects the least and most testability of the circuit.

5.2 Importance of The Test Points

As the previous section suggests, the testability of a circuit depends on the controllability and observability values of each node of the circuit. These CYs , OYs, and TYs are functions of the followings:

$$CY_i = f(\text{primary inputs, structure of the circuit})$$

$$OY_i = f(\text{primary outputs, structure of the circuit})$$

$$TY_i = f(\text{primary inputs, primary outputs, structure of the circuit})$$

Therefore, adding test points to most types of circuits (i.e. in the form of inputs

or outputs) should result in a better testability. Although this has not been shown quantitatively before, a monotonic relationship can be expected, as shown in Figures 31 through 33.

For example, the testability of a circuit with N nodes may be calculated as:

$$TY_1 = \frac{\sum_{i=1}^N CY_i * OY_i}{N}$$

Assuming that observable test points can be added to any node that has an OY value less than one, OY_i will become 1 and the testability measure can be rewritten as:

$$TY_2 = \frac{\sum_{i=1}^N CY_i * OY_i}{N} = \frac{\sum_{i=1}^N CY_i}{N}$$

Since $0 \leq OY, CY \leq 1$, then

$$0 \leq TY_1 \leq TY_2 \leq 1$$

which results in a more testable circuit.

Work such as [39] proposed a method for optimum placements of observable test points in combinational circuits. However, the main problem with this approach is the lack of available I/O test pins for a typical VLSI chip. This problem is somewhat eliminated by the high I/O capability of the flip-chip technology. The flip-chip technology can offer a higher number of I/Os than the wire-bond, as shown in Figure 34.

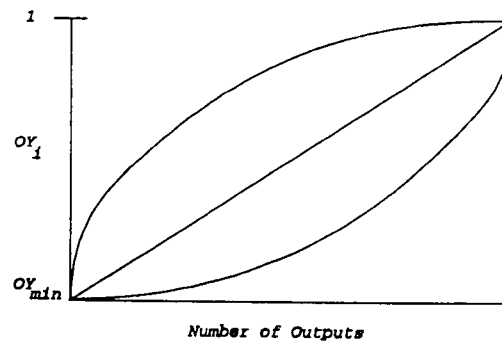


Figure 31. Impact of number of test points on observability,

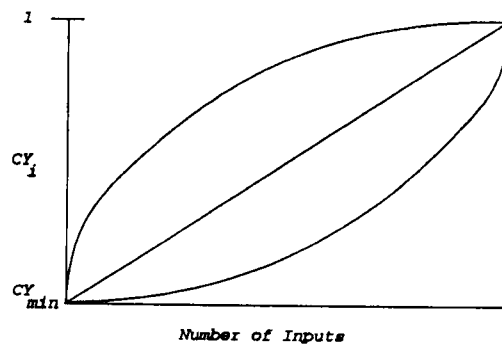


Figure 32. Impact of number of test points on controllability.

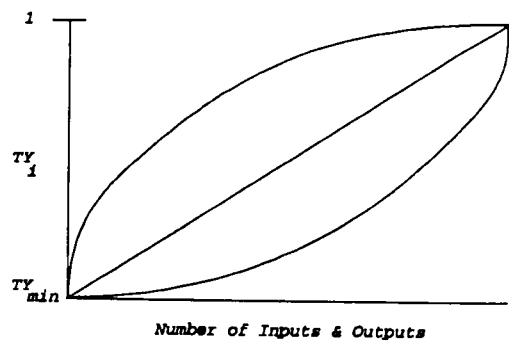


Figure 33. Impact of number of test points in testability.

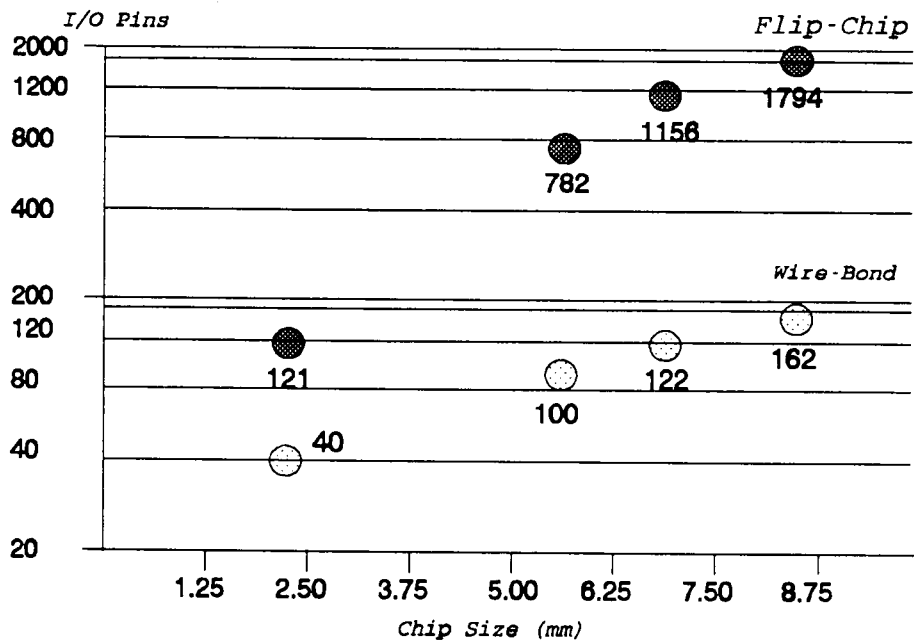


Figure 34. Maximum Number of I/O for Wire-Bond and Flip-Chip.

A higher number of I/Os can offer the designer with a higher number of test points and therefore, a more testable design. Of course, the designer has to consider the limitations of the testing equipment and test cost when he makes such a decision.

5.3 Scan-Path Technique

Many of the DFT techniques attempt to increase the testability by enhancing the controllability and observability of the circuit nodes. These techniques try to maximize the testability while keeping down the testing requirements such as the cost, the number of dedicated I/O pins, etc. Scan-path is one of these techniques which enhances the controllability and observability by using scannable latches [40].

The circuit employing the scan-path has two modes of operation: normal and testing. In the normal mode of operation, the scannable latches load the data in parallel

from the primary inputs, as shown in Figure 35. During testing, the latches load the test data serially from the test input. This allows the controllability and observability of the internal nodes without additional external test points. Another advantage of the scan-path is in test generation for sequential circuits. The test generation needs only be performed for the combinational circuits since the latches can be scanned and tested directly.

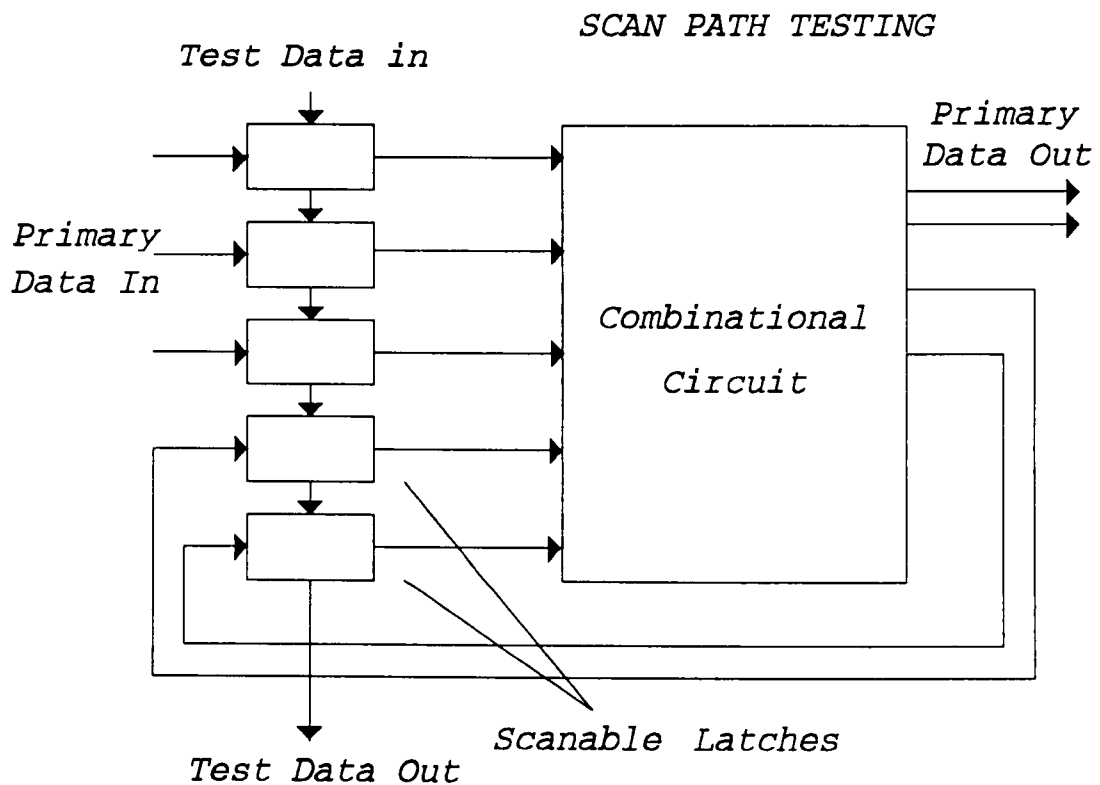


Figure 35. Scan-Path Testing Concept.

5.4 Examples and Results

The PE, IO, and CTL chips of the previous sections are used again as examples. All three chips are sequential circuits which can be modeled as shown in Figure 35. Scan-path testing is included in the design of the PE, IO, and CTL chips for both wire-bond and flip-chip approaches. This is done mainly due to the lack of available I/O pins, which is inherent to the wire-bond.

TGS [41] is an automatic test pattern generation tool which is included in the LAGER CAD tool-set. The TGS tool generates test vectors based on the PODEM algorithm. The PODEM algorithm guarantees to find a test vector if it exists for single stuck-at fault models. This tool is used to generate test patterns for the combinational circuits of the PE, IO, and CTL chips. The results of these test vectors are shown in Figure 36.

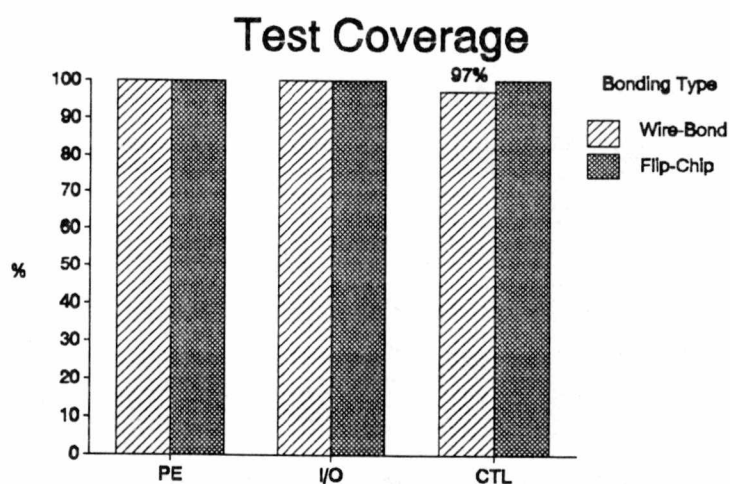


Figure 36. Comparison of Test Coverage Between Wire-bond and Flip-chip.

The IO chip is the easiest one to test because it consists purely of shift registers and some buffers. All the shift registers are implemented using the scannable latches which provide 100% testability. The combinational circuit consists of buffers which can also be tested to 100%.

The PE chip is composed of an easy circuit for testing because the MPP architecture is based on simple 1-bit processing elements. These processing elements contain a few scannable latches, a 1-bit adder, and a small local controller. The scan-path testing scheme creates proper controllability and observability for the combinational part of the PE chip. The TGS-generated test vectors provide 100% test coverage for the combinational part of the PE chip. This coverage, along with the easy testing of the scannable latches, results in a testability of 100%.

The CTL chip decodes all the micro-instructions and provides all the necessary signals for the other chips (i.e. PE, IO, and memory chips). The chip is designed using the BDS high level description language [42]. A high level synthesizer then implements the design using random logic. The CTL chip is slightly more difficult to test because of the random logic. The TGS-generated test vectors cover only 97%.

Another useful feature of the TGS is the generation of the fault table and fan-out and fan-in of the logic gates in the design. The fault table shows all possible faults and whether or not they have been detected by the generated test vectors. A more careful study of this table and fan-out and fan-in of the CTL circuit, reveals the undetected faulty nodes. By adding five test points to the selected undetected faulty nodes, the test coverage is raised to 100%. The selected nodes are chosen by trial and error due to the complexity of the circuit which prohibited the author from using techniques such as [39].

The flip-chip technology has an advantage over the wire-bond in the number of I/O pins. This could clearly be used to improve the testability of the chip in hand. However, the test coverage as demonstrated is not the only testing issue that has to be compared. Other aspects of the testing such as generation, application, and cost should also be evaluated for a fair comparison between the wire-bond and flip-chip technologies. These issues are not discussed here and are the subjects of future work in this area.

CHAPTER 6

COST ANALYSIS

A performance analysis between wire-bond and flip-chip technologies has been given in the last three chapters. In today's competitive electronics market, performance analysis by itself is not sufficient for comparison of two different technologies. The economy of the technologies are as important as the performance in a number of applications.

In this chapter, a simplified cost model is presented for the wire-bond and the flip-chip technologies. The intention of this chapter is not to introduce a new cost modeling technique. It simply provides the reader with a rough cost measure of the wire-bond and the flip-chip technologies. These measures are not complete by any means; however, it should be adequate for relative comparison.

6.1 A Simplified Cost Model

The cost model presented in this section is a simplified version of the technical cost model that is proposed by [43]. Technical cost modeling is essentially a quantitative cost breakdown of the manufacturing process flow.

The cost model is focused at the chip level and contains three elements as follows:

$$\text{Cost} = f(\text{cost of die, cost of bond, assembly cost, non-recurring engineering cost})$$

These cost elements depend on the specific manufacturer to a great extent. It is difficult to collect specific data from any manufacturer due to the proprietary nature of business. Therefore, the cost elements, and scenarios shown here are representative of the industry at large [44][45].

The cost of the die is a function of the size of the die and the number of defects in the die area. Using a Poisson distribution, probability of a die without defects is estimated by:

$$P = e^{-AD}$$

where A is the area of the die and D is the defect-density measured in number-of-defects in a unit area. The number of potential dies with area of "A" for a wafer with radius of "r" is given by:

$$N_{die} = \frac{\pi r^2}{A}$$

Therefore, the cost of a single die is given by:

$$\text{Cost}_{die} = \frac{\text{Cost}_{wafer}}{N_{die} P} = \frac{A \text{Cost}_{wafer}}{\pi r^2 e^{-AD}}$$

where $\text{Cost}_{\text{wafer}}$ is the cost associated with one wafer including the bond cost. This is because of the flip-chip process in which the wafers are bumped with solder balls as an integrated part of wafer fabrication.

The non-recurring engineering cost (NRE) is a one-time cost for setting up the proper manufacturing equipment. Due to the maturity and availability of the wire-bond technology, the NRE cost of the wire-bond is less than that of the flip-chip technology. Table 6 shows the assumptions used for the computation of the cost. A higher defect-density is chosen for the flip-chip because of its denser layout. Partial cost of bonding is included in the cost of the wafer for the flip-chip technology. This is due to the placing of solder bumps at the wafer level during the manufacturing process.

6.2 Examples and Results

The cost of dies are calculated for the flip-chip and wire-bond chip-sets and tabulated in Table 7. The N_{die} is the number of potential dies for a four-inch wafer. P is the probability of a defect-free die and $N_{\text{good die}}$ is the actual number of good dies per wafer. It is interesting to note that the cost of the flip-chip IO and CTL dies are less than the corresponding wire-bond dies, even though, the flip-chip has a higher wafer cost and defect-density. In the case of the PE chip, the cost is in favor of the wire-bond technology due to its large size. The complete cost of the die, along with the bonding and NRE cost for 1000 dies, is presented in Table 8.

Table 6. Default Values for Cost Models.

	Quantity	NRE cost Per Unique Wafer (\$)	Bond Cost Per Wafer (\$)	Cost of 4" Wafer (\$)	Defect Density "D" (/cm ²)
Wire-Bond	1000	1000	0.25	200	1
Flip-Chip	1000	4000	8	300 (bumped wafer)	2

Table 7. Cost Comparison of Wire-Bond and Flip-Chip Dies.

	N_{die}	P	$N_{\text{good die}}$	Cost _{die} (\$)
PE Wire-Bond	25.3	0.2	5	59
PE Flip-Chip	37.2	4.1	0.11	73.3
IO Wire-Bond	77.3	0.59	46	6.58
IO Flip-Chip	124.1	0.52	64.5	4.65
CTL Wire-Bond	91.9	0.64	59	5.1
CTL Flip-Chip	1188.2	0.93	1105	0.27

Table 8. Final Cost Break Down for Wire-Bond and Flip-chip.

	Wire-Bond				Flip-Chip			
	Die	Assem.	NRE	Total	Die	Assem.	NRE	Total
PE	59.00	0.05	1.00	60.05	73.30	2.00	4.00	79.30
IO	6.58	0.00	1.00	7.58	4.65	0.13	4.00	8.78
CTL	5.10	0.00	1.00	6.10	0.27	0.01	4.00	4.28

Relative comparison of these cost breakdowns for flip-chip and wire-bonding methods are shown in Figures 37 through 40. The cost of the flip-chip PE is 32% higher than that of the wire-bond version. This higher cost is largely contributed by the die cost (24%) and some by the NRE cost (5%). The IO chip reveals different characteristic. It is interesting to note that the cost of the flip-chip die is less than the wire-bond by 21%. However, the NRE cost of the flip-chip is higher than the that of the wire-bond by 40% resulting in a 16% cost advantage for the wire-bond. The CTL chip is the only one that shows a lower cost for the flip-chip by 30%. This cost advantage is contributed by the die cost, which in turn results from the enormously smaller size of the flip-chip die.

Cost Analysis (PE)

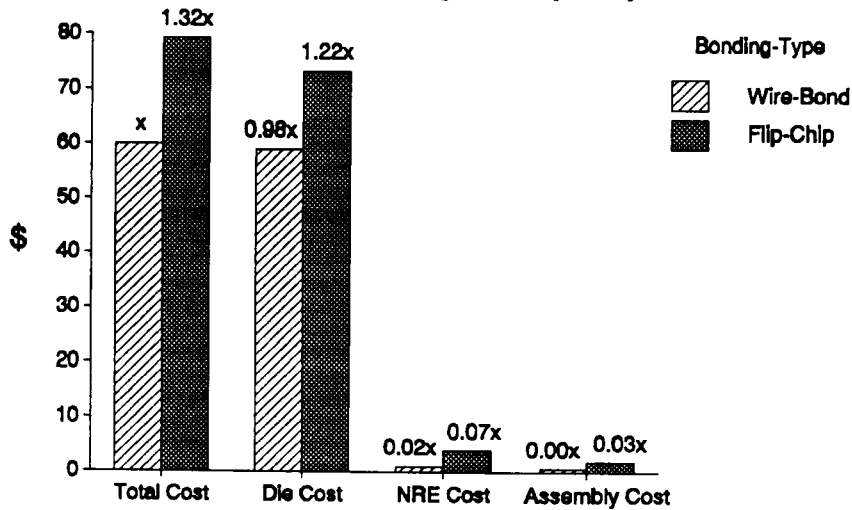


Figure 37. Cost Comparison of the PE Chip for Wire-bond and Flip-chip technologies.

Cost Analysis (IO)

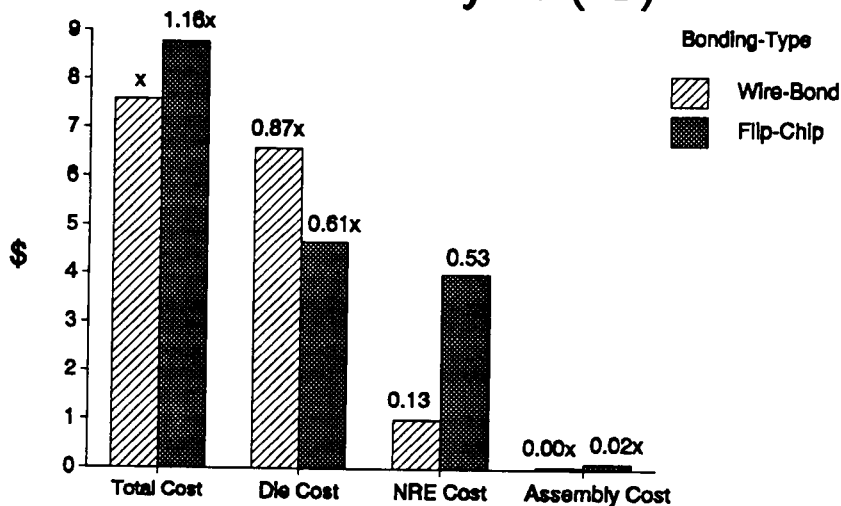


Figure 38. Cost Comparison of the IO Chip for Wire-bond and Flip-chip technologies.

Cost Analysis (CTL)

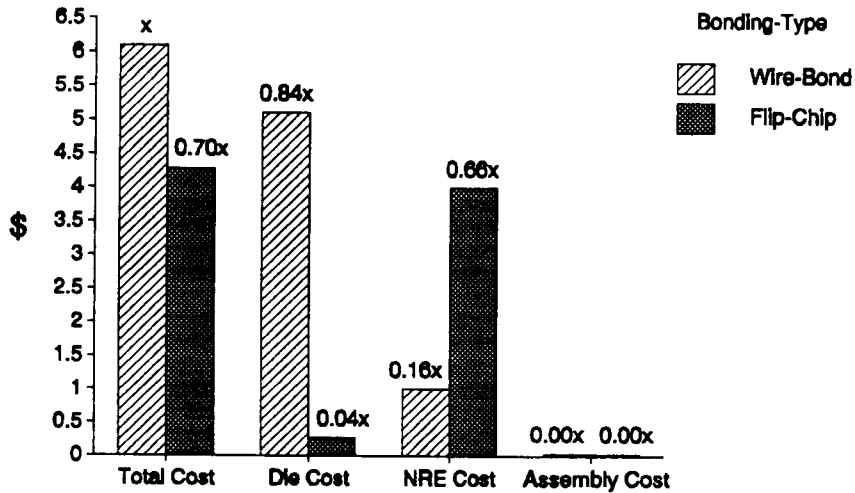


Figure 39. Cost Comparison of the CTL Chip for Wire-bond and Flip-chip technologies.

Cost Analysis (Overall)

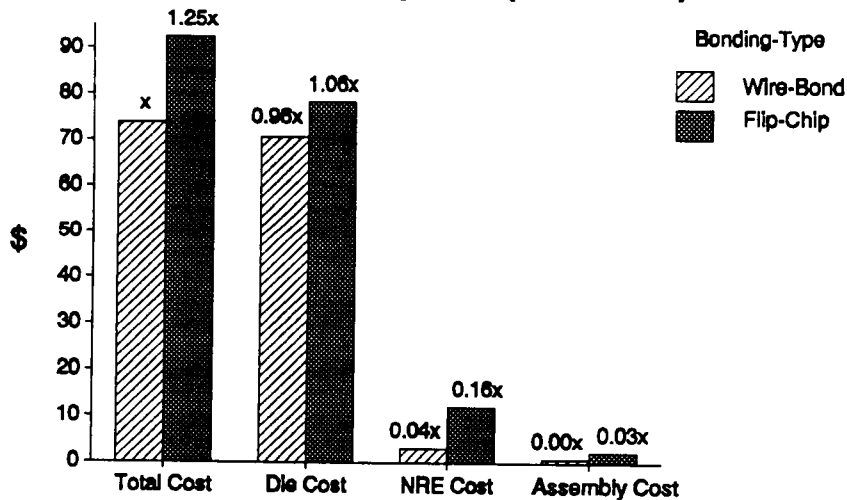


Figure 40. Cost Comparison of the All Chips for Wire-bond and Flip-chip technologies.

Considering all the three chips, the wire-bond technology is more cost effective by 25%. This cost advantage is due to die and NRE costs. The cost of the assembly does not seem to be a major contributing element as compared with the NRE and die costs. It should be taken into consideration that the cost model is intended at the chip level rather the system level. It should be noted, however, these cost estimations are only as good as the cost model and the default values. Therefore, a slight change in the model or the default values may change the results drastically.

CHAPTER 7

SUMMARY

7.1 Conclusion

A cost/performance comparison between wire-bond and flip-chip technologies has been presented. It has been shown that the bonding and Interconnect technologies may impact the performance of VLSI dies in the following areas:

- 1) Size
- 2) Power Consumption
- 3) Testability
- 4) Cost

The overall results of the previous chapters, along with a composite figure-of-merit, are shown in Figure 41. All the measurements are normalized to the wire-bond measurements for comparison purposes. The composite figure-of-merit is a weighted sum of size, power, testability, and cost and computed as:

$$Figure_{merit} = \frac{W1}{Size} + \frac{W2}{Power} + W3 * Testability + \frac{W4}{Cost}$$

where "Ws" are the weight associated with each of the above areas. The composite figure-of-merit shown in Figure 41 is calculated by setting all the "Ws" to 1. This work shows that the flip-chip technology has a higher figure-of-merit than the wire-bond by 135%. The following issues should be kept in mind when one considers the

results of this work:

- 1) The figure-of-merit presented in this work depends only on the few basic elements that have been discussed earlier. For a comprehensive figure-of-merit (if such a thing really exists), one has to consider additional areas such as thermal management, more complete test and cost models, etc.

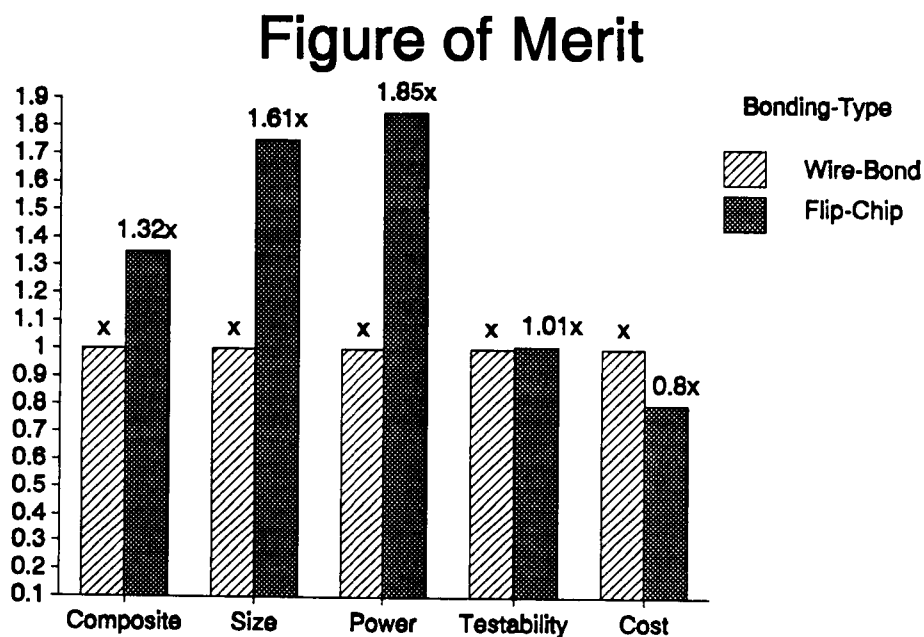


Figure 41. Over All Comparison of Flip-chip and Wire-bond Technology.

- 2) The scope of this work has been at the die level, not at the system level. This means that a superior figure-of-merit at the die level may not result in a superior figure-of-merit at the system level. This is due to the multi-dimensionality of the solution space where considering only one dimension of the solution space may not produce a globally optimum solution. For example, chapter three illustrated that the flip-chip approach results in a smaller die size which requires a smaller substrate for housing and interconnections. The number of the interconnection nets on the substrate is the same regardless of the choice of bonding technology. Therefore, the substrate in the flip-chip version is expected to have a higher interconnection density. This may require the substrate to have more layers resulting in a higher cost at the substrate and possibly at the system level. Therefore, the VLSI system designer should understand and consider the impact of packaging technology at the die level at an early stage of the design for an optimum system design.

7.2 Future Work

The two issues mentioned above set the direction for the future work. A more complete model of testing and cost should be developed at the die levels. The accuracy of the power consumption measurement should be evaluated and fine tuned

by possible fabrication and measurements. Other areas, such as thermal management, should also be included in a comparison of packaging technology for a given application.

Optimization of the design parameters at the system level is the most important. Impact of the packaging parameters at the die and system levels should be understood and considered. The performance/cost issues due to the die (this work) should be coupled with the ones due to packaging (previous work). A composite cost/performance model based on the die and the package can be developed for better comparison purposes. The same model can be used to optimize the packaging parameters for a given objective function.

LIST OF REFERENCES

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- [1] Fichtner, W., "0.15 Micron Channel Length MOSFETs Fabricated using E-beam Lithography", *International Electron Device Meeting*, pp. 722-724, 1982.
- [2] Boll, H., "Silicon MOSFETs Achieve High Speed Via Submicron Dimensions", *Microwave Systems News*, pp. 75-89, 1982.
- [3] Hatamian, M., "Fundamental Interconnection Issues", *AT&T Technical Journal*, Vol. 66, Issue 4, pp. 13-30, July 1987.
- [4] Richard, H., "Multichip Modules", *26th ACM/IEEE Design Automation Conference*, pp. 389-393, 1989.
- [5] Moore, G., "VLSI: Some Fundamental Challenges", *Spectrum*, Vol. 16, pp. 30, 1979.
- [6] Meindl, J., "Theoretical, Practical, and Analogical Limits in ULSI", *IEEE International Electron Devices Meeting (IDEM'83)*, pp. 8-13, Dec 1983.
- [7] EET Editor, "Bipolar Packaging Lags Technology", *Electronic Engineering Times*, pp. 75, Oct 3, 1988.
- [8] Balders, D., "Package Effects on CPU Performance of Large Commercial Processors", *Proceedings of 35th Electronic Components Conference*, pp. 351-355, 1985.
- [9] McDonald J., "The Trials of Wafer Scale Integration", *IEEE Spectrum*, pp. 32-39, Oct 1984.
- [10] Neugebauer C., "Comparison of VLSI Packaging Approaches", *Proc. Tech. Program, NEPCON*, pp. 227-234, Jun 1987.
- [11] Matsui, N., "VLSI Chip Interconnection Technology Using Stacked Solder Bumps", *IEEE Transaction on component, Hybrid, and Manufacturing Tech.* Vol. CHMT-12, pp. 566-570, Dec. 1987.

- [12] Blood Bill and Casey Allison, "Evaluating Multichip Module Packaging Technology", *ASIC Technology and News*, pp. 26-28, July 91.
- [13] Bartlett Charles, Segelken Jhon, and Teneketges Nicholas, "Multichip Packaging Design for VLSI-Based Systems", *IEEE Transactions on Componenets, Hybrid, and Manufacturing Technology*, Vol. CHMT-12, No. 4, pp. 647-653, Dec. 1987.
- [14] Shiao Jack and Nguyen Dong, "Performance Modeling of a Cache System with Three Interconnect Technologies: Cyanate Ester PCB, Chip-On-Board and CU/PI MCM", *Proceedings of 1992 IEEE Multi-chip Module Conference MCMC-92*, Santa Cruz, California, pp. 134-137, March 18-20, 1992.
- [15] Batcher K.E. and Potter J.L. Eds., "The Massively Parallel Processor", MIT Press, Cambridge, MA, 1985.
- [16] Heaton Robert, Blevins Don, and Davis Edward, " A Bit-Serial VLSI Array Processing Chip for Image Processing", *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 2, pp. 364-368, April 1990.
- [17] Blevins D., Davis E., and Reif J., "Processing Element and Custom Chip Architecture for The BLITZEN Massively Parallel Processor", Microelectronics Center of North Carolina, Research Triangle Park, Technical Report TR87-22, Revised June 10, 1988.
- [18] Scmitt L.A. and Wilson S.S., " The AIS-5000 Parallel Processor", *IEEE Transactions on Pattern Analysis and Machine Intelligence*, Vol. 10, No. 3, May pp. 320-330, 1988.
- [19] Kozak Al, "Applications of Multichip Modules for High Speed Communications Interface", *Proceedings of 1992 IEEE Multi-Chip Module Conference MCMC-92*, pp. 16-19, March 18-20, Santa Cruz, California, 1992.
- [20] Bakoglu H.B. and Meindl J.D., "A System Level Circuit Model For Multi- and Single-chip CPUs", *IEEE International Solid State Circuits Conference (ISSCC'87)*, New York, pp. 308-309, Feb 1987.
- [21] Bakoglu H.B., "Circuits, Interconnections, and Packaging for VLSI", Addison-Wesley, 1990.
- [22] Krusius, J, "System Interconnection of High Density Multi-Chip Modules", *SPIE International Conference on Advances in Interconnection and Packaging*, Vol. 1390, pp. 261-270, 1990.
- [23] Krusius J.P., "Packaging Architecture Considerations of High Density Multi-Chip Electronic Packages via System Optemization", *Transactions of the ASME*,

Journal of Electronic Packaging, 112, 267, 1990.

- [24] Sandborn, P., "A tool for Evaluating Performance and Technology Tradeoffs on Integrated Circuit Packaging", *MCC Technical report P/I-120-91*, 1991.
- [25] Nagesh V.K., Miller D., and Moresco L., "A Comparative Study of Interconnect Technologies", *Proceedings of The 9th International Electronics Packaging Conference*, San Diego, pp. 433-443, Sept 11-13, 1989.
- [26] Shung C.B., Jain R., Rimey K., Wang E., Sirvatava M.B., Richards B.C., Azim K., and Lettang E., "An Integrated CAD System for Algorithm-Specific IC Design", *IEEE Transactions on Computer-Aided Design*, Vol. 10, No. 4, pp. 447-463, April 1991.
- [27] The Institute for Technology Development, "Scalable CMOS (SCMOS) Standard-Cell Library d1mv2.2", Advanced Microelectronics Division, March 8, 1990.
- [28] Elmasry Mohamed, editor, "Digital Mos Integrated Circuits: A Tutorial", *IEEE Press*, pp. 4-27, 1981.
- [29] Veendrick Harry, "Short-Circuit Dissipation of Static CMOS Circuitry and Its Impact on The Design of Buffer Circuits", *IEEE Journal of Solid-State Circuits*, SC-19(4), August 1984.
- [30] Weste Neil and Eshraghian Kamran, "Principle of CMOS VLSI Design, A System Perspective", Addison-Wesley Publishing Company, Reading, Massachusetts, 1988.
- [31] Jeng Rong L., "A New Approach to Estimate Dynamic Power Dissipation of Synchronous Digital CMOS Combinational Circuits", Ph.D. Dissertation, University of Cincinnati, 1991.
- [32] Devadas Srinivas, Keutzer Kurt, and White Jacob, "Estimation of Power Dissipation in CMOS Combinational Circuits", *The Proceedings of Custom Integrated Circuits Conference*, Boston, MA, 1990.
- [33] Williams Thomas and Parker Kenneth, "Design for Testability - A Survey", *Proceedings of the IEEE*, Vol. 71, No. 1, pp. 98-112, January 1983.
- [34] Bennetts R.G., "Design of Testable Logic Circuits", Addison-Wesely Publishing, 1984.
- [35] Ratiu Ion and Sangiovanni-Vincentelli Alberto and Pederson Donald, "VICTOR: A Fast VLSI Testability Analysis Program", *1982 IEEE Test Conference*, pp. 397-401, 1982.

- [36] Goldstein L.H., "Controllability/Observability Analysis of Digital Circuits", SAND78-1895, Sandia Laboratories, Albuquerque, N. Mexico, Nov 1978.
- [37] Stephenson Jack and Grason John, "A Testability Measure For Register Transfer Level Digital Circuits", *Dig. 6th Int. Symp. Fault-tolerant Comput. (FTCS-6)*, Pittsburgh, pp. 101-107, Jun 21-23, 1976.
- [38] Agrawal V.D. and Mercer M.R., "Testability Measures - What Do They Tell Us?", *Dig. 1982 IEEE Test Conf.*, Philadelphia, pp. 391-396, Nov. 11-13, 1982.
- [39] Hayes J.P. and Friedman A.D., "Test Point Placement to Simplify Fault Detection", *Int. Symp. on Fault-Tolerant Computing FTC/3*, June 20-21, Palo Alto, 1973, PP:73-78.
- [40] McCluskey Edward J., "Logic Design Principles - With Emphasis on Testable Semicustom Circuits", Prentice-Hall, 1986.
- [41] Abramovici M., Breuer M.A., and Friedman A.D, "Digital Systems Testing and Testable Designs", ISBN 0-7167-8179-4, Computer Science Press, 1990.
- [42] Electronics Research Laboratory, "LAGER Tool Set", University of California, Berkeley, Dec 5, 1988.
- [43] Vardaman J., and Ng L.H., "A Cost/performance Analysis of Multichip Module Interconnects", *Proceedings of 91 ISHIM*, pp. 27-32, 1991.
- [44] Randall L.G. and Allen P.E. and Strader N.R., "VLSI Design Techniques For Analog And Digital Circuits", McGraw-Hill Inc, 1990.
- [45] Sandborn Peter and Ghosh R., "SDA/Technology Tradeoff Tool Installation and User's Guide - Version 1.1", Microelectronics and Computer Technology Corporation, Austin, Texas, 1992.

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