A Ringamp-Assisted, Output Capacitor-less, Analog CMOS Low-Dropout Voltage Regulator

A Dissertation Presented for the

Doctor of Philosophy

Degree

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I dedicate this entire work
to my wife, Jenny, and
our exceptional children,
Harper and Henry

Acknowledgments

My path to study electrical engineering began as an exercise of discipline and self-improvement, to cleanse my emotional state after the tragic loss of my little brother and best friend, Carson Ryan Sangid. The energy behind my daily thoughts wishing for one more minute with him has been my drive to reach the highest levels of education. I owe all my accomplishments from this journey to my brother, Carson.

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Abstract

Continued advancements in state-of-the-art integrated circuits have furthered trends toward higher computational performance and increased functionality within smaller circuit area footprints, all while improving power efficiencies to meet the demands of mobile and battery-powered applications. A significant portion of these advancements have been enabled by continued scaling of CMOS technology into smaller process node sizes, facilitating faster digital systems and power optimized computation. However, this scaling has degraded classic analog amplifying circuit structures with reduced voltage headroom and lower device output resistance; and thus, lower available intrinsic gain. This work investigates these trends and their impact for fine-grain Low-Dropout (LDO) Voltage Regulators, leading to a presented design methodology and implementation of a state-of-the-art Ringamp-Assisted, Output Capacitor-less Analog CMOS LDO Voltage Regulator capable of both power scaling and process node scaling for general SoC applications.

Table of Contents

1 Introduction **1**

1.1 Dissertation Overview . . . 1

1.2 Technology Trends . . . 2

1.2.1 On Integration and Scaling . . . 2

1.2.2 LDO Basics . . . 4

1.3 Motivation . . . 7

1.4 Problem Statement . . . 8

1.5 Original Contributions . . . 8

2 Literature Review **11**

2.1 Voltage Regulation in Literature . . . 11

2.1.1 Historical Contributions . . . 13

2.1.2 Granular Voltage Regulation . . . 24

2.1.3 Contemporary Fine-Grain LDOs . . . 27

2.2 Ring Amplifiers in Literature . . . 33

2.2.1 Ring Amplifier Behavior . . . 34

2.2.2 Ring Amplifiers for Data Conversion . . . 37

2.2.3 Ring Amplifiers for LDOs . . . 43

3 On-Demand Ring Amplifier Design **49**

3.1 A Ring Amplifier Design Guide . . . 49

3.1.1 Pre-Design Tasks . . . 52

3.1.2 Design Method . . . 53

3.1.3 Final Design Considerations . . . 55
3.2 Design Scripts Usage Guide . . . 56
3.2.1 Optimum Inverter Design Script . . . 56
3.2.2 Parameter Extractor Function . . . 63

4 A Multi-Loop Analog LDO 72
4.1 Design Objectives . . . 73
4.2 The Dual-Loop Analog LDO . . . 73
4.2.1 CMOTA-based LDO Loop . . . 74
4.2.2 Ringamp-based LDO Loop . . . 80
4.2.3 Power Supply Rejection . . . 97
4.3 Physical Implementation . . . 100

5 Evaluations & Results 106
5.1 Experimental Test Board . . . 106
5.2 Experimental Sample Verification . . . 108
5.3 LDO Evaluations . . . 109
5.3.1 Static Observations . . . 109
5.3.2 Line-to-Load Regulation . . . 113
5.3.3 Transient Current Load Step . . . 113
5.3.4 Power Supply Rejection . . . 118

6 Case Study: A 65-nm Scaled RLDO 122
6.1 Case Structure and Limitations . . . 122
6.2 Scaled Multi-Loop LDO Design & Results . . . 123
6.2.1 Scaled RLDOE . . . 123
6.2.2 Scaled CMOTA-based LDO . . . 124
6.3 Case Study Conclusion . . . 127

7 Conclusions 130
7.1 Comparison to Prior Art . . . 131
7.2 Proposed Future Work . . . 131

Bibliography **137**

Appendices **147**

A Nyquist-rate Analog-to-Digital Converters . . . 148

A.1 ADC Metrics and Figures of Merit . . . 148

A.2 The Pipelined ADC . . . 149

A.3 The SAR ADC . . . 149

B Source Code . . . 152

B.1 Optimum Inverter Design Script . . . 152

B.2 Parameter Extractor Function . . . 155

C Evaluation Printed Circuit Board . . . 157

C.1 Test Board Schematics . . . 157

C.2 Test Board Assembly Drawings & Layout . . . 157

C.3 Test Board Bill of Materials . . . 171

D Layout Figures . . . 187

D.1 180-nm Implementation . . . 187

D.2 65-nm Implementation . . . 187

E Additional Simulation Figures . . . 198

E.1 180-nm CMOTA Loop Simulations . . . 198

E.2 180-nm RLDOE Loop Evaluations . . . 202

E.3 65-nm Design Simulations . . . 205

E.4 65-nm RLDOE Loop Evaluations . . . 210

E.5 65-nm CMOTA Loop Simulations . . . 214

F Experimental Data . . . 219

F.1 Peripheral Circuit Evaluations . . . 219

F.2 RLDOE Loop Evaluations . . . 226

F.3 CMOTA Loop Evaluations . . . 237

Vita **257**

List of Tables

1.1 Comparison of Regulator Topologies for SoC Applications 10

2.1 Historically Significant Published LDO Performance Metrics 23
2.2 State-of-the-Art Fine-Grain LDO Performance Metrics 32
2.3 All Known Published Ringamp LDO Performance Metrics 48

3.1 Inverter Design Results 64
3.2 Parameter Extractor Results 71

5.1 RLDOE-Loop Current Load Step Results 116
5.2 CMOTA-Loop Current Load Step Results 117

6.1 Results of Scaled 65-nm LDO Compared to Original 129

7.1 Target Design Objectives Compared to Previous Ringamp-based LDOs . . . 133
7.2 Target Design Objectives Compared to Recent State-of-the-Art LDOs 135
E.1 Simulated RLDOE-Loop Current Load Step Results 211
E.2 Simulated CMOTA-Loop Current Load Step Results 215
F.1 Peripheral Circuit Test Results for Individual Chips 220
F.2 RLDOE Loop load step Evaluation Results for Individual Chips 228
F.3 CMOTA Loop Current Load Step Evaluation Results for Individual Chips . 241

List of Figures

1.1 TSMC technology node size over time 3
1.2 MOSFET intrinsic gain for multiple process technologies 6
1.3 Voltage regulator schematic and behavior 6

2.1 Summary of LDO performance metrics used within this dissertation 12
2.2 Original sub-micron voltage regulator topologies 15
2.3 Prior analog LDO examples 18
2.4 Original OCL LDO schematic 18
2.5 OCL LDO schematic with on-demand boost 20
2.6 Early non-analog voltage regulators 20
2.7 Ultra-fast load regulation LDO 22
2.8 Heterogeneous power delivery with multiple power domains 25
2.9 Multi-loop DLDO implementations 29
2.10 Multi-loop DLDO with NMOS pass device and NAPs 29
2.11 Time-to-Frequency domain LDO 31
2.12 Active capacitor ALDO 31
2.13 Basic five-inverter ring oscillator 35
2.14 Ringamp MDAC and output settling behavior 35
2.15 Switched-capacitor CLS circuit 38
2.16 The split-CLS MDAC structure 38
2.17 Ringamp with CSI embedded dead-zone 41
2.18 Four-stage fully differential ringamp 41
2.19 Ringamp enhancement techniques 44

2.20 Inverter-based LDO 44
2.21 Ringamp-based LDO schematic with replica biasing 46
2.22 AZ interleaving RLDO 46

3.1 On-demand ringamp with Class B output 50
3.2 On-demand ringamp with Class AB output 51
3.3 Design flowchart for proposed ringamp structure 57
3.4 IV curves for parameter extraction example 59
3.5 Required spreadsheet format for parameter extractor MATLAB® script . . . 60
3.6 Optimum inverter design script excerpt for user defined design parameters . 60
3.7 LTspice® testbench example for generating MOSFET IV curves 61
3.8 Optimum inverter design script excerpt for user defined device parameters . 64
3.9 Resulting transfer curve for optimized example inverter 65
3.10 LTspice® testbench example for evaluating optimum inverter design 66
3.11 IV plots of V_{GS} versus I_D for approximating threshold voltage 68
3.12 IV curves and approximated Early Voltage V_A 70

4.1 System-level schematic of the dual-loop analog LDO 75
4.2 Schematic of the CMOTA error amplifier 75
4.3 180-nm simulated loop gain analysis of CMOTA error amplifier 77
4.4 Equivalent schematic of the CMOTA-based LDO loop 79
4.5 180-nm simulated loop gain analysis of the CMOTA LDO loop 81
4.6 Equivalent schematic of the RLDOE loop 82
4.7 Schematic of RLDOE loop 84
4.8 Ringamp unit inverter schematic 87
4.9 180-nm simulated ringamp unit inverter transfer curve 87
4.10 Schematic of complementary transmission gate 88
4.11 180-nm simulated complementary transmission gate R_{DS} values 88
4.12 180-nm simulated pseudo-differential switch driver transition waveforms . . . 90
4.13 Schematic of the Pseudo-Differential Switch Driver 91
4.14 180-nm simulated open-loop frequency response of first stage inverter 93

4.15 Equivalent schematic of RLDOE with labeled pole locations 94
4.16 Split-Miller Compensation technique for designed multi-loop LDO 96
4.17 180-nm simulated loop gain analysis of RLDOE loop 98
4.18 Simplified schematic of dual-loop LDO output stage for PSR analysis 99
4.19 180-nm simulated PSR performance of the RLDOE loop 101
4.20 180-nm simulated PSR performance of the CMTOA loop 101
4.21 Teucer full chip photograph 103
4.22 Teucer full chip photograph with labelled sections 104
4.23 Photograph of the implemented multi-loop LDO's active area 105
4.24 Layout of the implemented multi-loop LDO's active area 105

5.1 Teucer test board for experimental evaluations 107
5.2 Experimental test configuration for unit inverter characterization 110
5.3 Experimental test configuration for PDSD characterization 110
5.4 Simulated inverter test cell incorporating experimental offsets 111
5.5 Simulated PDSD test cell incorporating experimental offsets 111
5.6 Experimental test configuration for current load step response evaluations . . 112
5.7 RLDOE loop experimental results of line-to-load regulation evaluation 114
5.8 CMOTA loop experimental results of line-to-load regulation evaluation . . . 114
5.9 RLDOE loop experimental PSR performance 120
5.10 Experimental test configuration for PSR evaluations 121

6.1 65-nm simulated ringamp unit inverter transfer curve 125
6.2 65-nm simulated open-loop frequency response of first stage inverter 125
6.3 65-nm simulated loop gain analysis of RLDOE loop 126
6.4 65-nm simulated loop gain analysis of CMOTA-based LDO loop 128

7.1 This work's results compared to those recently published 132
7.2 Multi-Loop LDO transient waveforms 134
A.1 Block diagrams of single stage pipelined and SAR ADCs 150
C.1 Teucer test board schematic page 1 158

C.2 Teucer test board schematic page 2 . . . 159
C.3 Teucer test board schematic page 3 . . . 160
C.4 Teucer test board schematic page 4 . . . 161
C.5 Teucer test board schematic page 5 . . . 162
C.6 Teucer test board schematic page 6 . . . 163
C.7 Teucer test board schematic page 7 . . . 164
C.8 Teucer test board schematic page 8 . . . 165
C.9 Teucer test board schematic page 9 . . . 166
C.10 Teucer test board schematic page 10 . . . 167
C.11 Teucer test board schematic page 11 . . . 168
C.12 Teucer test board schematic page 12 . . . 169
C.13 Teucer test board schematic page 13 . . . 170
C.14 Teucer test board layout and assembly drawings page 1 . . . 172
C.15 Teucer test board layout and assembly drawings page 2 . . . 173
C.16 Teucer test board layout and assembly drawings page 3 . . . 174
C.17 Teucer test board layout and assembly drawings page 4 . . . 175
C.18 Teucer test board layout and assembly drawings page 5 . . . 176
C.19 Teucer test board layout and assembly drawings page 6 . . . 177
C.20 Teucer test board layout and assembly drawings page 7 . . . 178
C.21 Teucer test board layout and assembly drawings page 8 . . . 179
C.22 Teucer test board layout and assembly drawings page 9 . . . 180
C.23 Teucer test board layout and assembly drawings page 10 . . . 181
C.24 Teucer test board layout and assembly drawings page 11 . . . 182
C.25 Teucer test board bill of materials (BOM) page 1 . . . 183
C.26 Teucer test board bill of materials (BOM) page 2 . . . 184
C.27 Teucer test board bill of materials (BOM) page 3 . . . 185
C.28 Teucer test board bill of materials (BOM) page 4 . . . 186
D.1 180-nm lowest impedance complementary transmission-gate layout . . . 188
D.2 180-nm highest impedance complementary transmission-gate layout . . . 188
D.3 180-nm pseudo-differential switch driver layout . . . 189

D.4 180-nm pass device array layout . . . 190
D.5 180-nm CMOTA layout . . . 191
D.6 180-nm RLDOE transistor-level layout . . . 192
D.7 65-nm lowest impedance complementary transmission-gate layout . . . 193
D.8 65-nm highest impedance complementary transmission-gate layout . . . 193
D.9 65-nm pseudo-differential switch driver layout . . . 194
D.10 65-nm pass device array layout . . . 195
D.11 65-nm CMOTA layout . . . 196
D.12 65-nm RLDOE layout . . . 197
E.1 Simulated CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8\,\text{V}$ . . . 199
E.2 Simulated CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8\,\text{V}$ . . . 199
E.3 Simulated CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8\,\text{V}$ . . . 200
E.4 Simulated CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9\,\text{V}$ . . . 200
E.5 Simulated CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9\,\text{V}$ . . . 201
E.6 Simulated CMOTA loop load step 1 mA to 50 mA with $V_{DD} = 1.8\,\text{V}$ . . . 203
E.7 Simulated RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8\,\text{V}$ . . . 203
E.8 Simulated CMOTA loop load step 500 µA to 50 mA with $V_{DD} = 0.9\,\text{V}$ . . . 204
E.9 Simulated CMOTA loop load step 5 mA to 50 mA with $V_{DD} = 0.9\,\text{V}$ . . . 204
E.10 65-nm simulated low resistance complementary transmission-gate R_{DS} values 206
E.11 65-nm simulated high resistance complementary transmission-gate R_{DS} values 206
E.12 65-nm simulated pseudo-differential switch driver transition waveforms . . . 207
E.13 65-nm simulated loop gain analysis of CMOTA error amplifier . . . 208
E.14 65-nm simulated PSR performance of the CMTOA loop . . . 209
E.15 65-nm simulated PSR performance of the RLDOE loop . . . 209
E.16 Simulated CMOTA loop load step 1 mA to 50 mA with $V_{DD} = 1.2\,\text{V}$ . . . 212
E.17 Simulated RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.2\,\text{V}$ . . . 212
E.18 Simulated CMOTA loop load step 500 µA to 50 mA with $V_{DD} = 0.6\,\text{V}$ . . . 213
E.19 Simulated CMOTA loop load step 5 mA to 50 mA with $V_{DD} = 0.6\,\text{V}$ . . . 213
E.20 Simulated CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.2\,\text{V}$ . . . 216
E.21 Simulated CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.2\,\text{V}$ . . . 216

E.22 Simulated CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.2$ V 217
E.23 Simulated CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.6$ V 217
E.24 Simulated CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.6$ V 218
F.1 Inverter test cell on Teucer Chip A 220
F.2 Inverter test cell on Teucer Chip B 221
F.3 Inverter test cell on Teucer Chip C 221
F.4 Inverter test cell on Teucer Chip D 222
F.5 Inverter test cell on Teucer Chip E 222
F.6 PDSD test cell on Teucer Chip A 223
F.7 PDSD test cell on Teucer Chip B 223
F.8 PDSD test cell on Teucer Chip C 224
F.9 PDSD test cell on Teucer Chip D 224
F.10 PDSD test cell on Teucer Chip E 225
F.11 RLDOE loop load step 1 mA to 50 mA with $V_{DD} = 1.8$ V on Teucer Chip A . 229
F.12 RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip A 229
F.13 RLDOE loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip A 230
F.14 RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip A . 230
F.15 RLDOE loop load step 1 mA to 50 mA with $V_{DD} = 1.8$ V on Teucer Chip B . 231
F.16 RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip B 231
F.17 RLDOE loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip B 232
F.18 RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip B . 232
F.19 RLDOE loop load step 1 mA to 50 mA with $V_{DD} = 1.8$ V on Teucer Chip C . 233
F.20 RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip C 233
F.21 RLDOE loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip C 234
F.22 RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip C . 234
F.23 RLDOE loop load step 1 mA to 50 mA with $V_{DD} = 1.8$ V on Teucer Chip D . 235
F.24 RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip D 235
F.25 RLDOE loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip D 236
F.26 RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip D . 236
F.27 RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 1.8$ V on Teucer Chip E . 238

F.28 RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip E 238
F.29 RLDOE loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip E 239
F.30 RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip E . 239
F.31 CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V on Teucer Chip A 242
F.32 CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V on Teucer Chip A 242
F.33 CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip A 243
F.34 CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V on Teucer Chip A . 243
F.35 CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ Von Teucer Chip A 244
F.36 CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V on Teucer Chip B 245
F.37 CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V on Teucer Chip B 245
F.38 CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip B 246
F.39 CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V on Teucer Chip B . 246
F.40 CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ V on Teucer Chip B 247
F.41 CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V on Teucer Chip C 248
F.42 CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V on Teucer Chip C 248
F.43 CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip C 249
F.44 CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V on Teucer Chip C . 249
F.45 CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ V on Teucer Chip C 250
F.46 CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V on Teucer Chip D 251
F.47 CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V on Teucer Chip D 251
F.48 CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip D 252
F.49 CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V on Teucer Chip D . 252
F.50 CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ V on Teucer Chip D 253
F.51 CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V on Teucer Chip E 254
F.52 CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V on Teucer Chip E 254
F.53 CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip E 255
F.54 CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V on Teucer Chip E . 255
F.55 CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ V on Teucer Chip E 256

List of Nomenclature

FOM	Figure of Merit
UGF	Unity Gain Frequency
C_G	Gate Capacitance
C_{EXT}	External Capacitor
f_T	Transition Frequency
GB	Gain Bandwidth
I_Q	Quiescent Current Draw
I_{LOAD}	Load Current
$P.M.$	Phase Margin
r_o	Small Signal Output Resistance
$R_{DS,PASS}$	Drain-to-Source Resistance of LDO Pass Device
V_{DO}	Dropout Voltage
V_{IN}	Input Voltage
V_{OUT}	Output Voltage
ACI	Air Core Inductor
ADC	Analog-to-Digital Converter

AZ	Auto-Zeroing
BGR	Bandgap Reference
BiCMOS	Bipolar CMOS
BJT	Bipolar Junction Transistor
CCO	Current Controlled Oscillator
CLS	Correlated Level Shifting
CMFB	Common-mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CMOTA	Current Mirror Operational Transconductance Amplifier
CRD	Current Regulator Diode
CSI	Current-Starved Inverters
DFC	Damping-Factor-Control
DLDO	Digital Low-Dropout Regulator
DUT	Device Under Test
DVFS	Dynamic Voltage and Frequency Scaling
DVS	Dynamic Voltage Scaling
DZD	Dead-Zone Degeneration
FG	Function Generator
FIVR	Fully Integrated Voltage Regulator
HEI	Hot-Electron Injection
HVT	High-Voltage-Threshold

IBA	Inverter-Based Amplifier
IO	Input or Output
IoT	Internet of Things
LCO	Limit-Cycle Oscillation
LDO	Low-Dropout Voltage Regulator
LHP	Left Half Plane
LSI	Large-Scale Integration
LVR	Linear Voltage Regulator
MIA	Magnetic Inductor Array
MIM	Metal-Insulator-Metal
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
OCL	Output Capacitor-less
OTA	Operational Transconductance Amplifier
PDK	Process Design Kit
PDN	Power Distribution Network
PoL	Point-of-Load
PSiP	Power Supply in Package
PSR	Power Supply Rejection
PSRR	Power Supply Rejection Ratio
PVT	Process Voltage Temperature
RAM	Random Access Memory

RHP	Right Half Plane
RLDO	Ringamp-based Low-Dropout Voltage Regulator
S/H	Sample and Hold
SC	Switched-Capacitor
SMPS	Switch-Mode Power Supply
SNR	Signal-to-Noise Ratio
SoC	System on Chip
THA	Track and Hold Amplifier
VLSI	Very Large-Scale Integration

Chapter 1

Introduction

1.1 Dissertation Overview

The intent of this paper is to present a novel Low-Dropout Voltage Regulator solution and summarize the corresponding body of work that would satisfactorily qualify the candidate for a Doctor of Philosophy within Electrical Engineering. The primary area of interest discussed within this dissertation is Power Management for System on Chips (SoCs). This area is not new but has maintained relevancy due to trends and resulting demands towards higher computationally dense and more power dense electronic systems that maximize power efficiency. These trends have also found a continuous push by market demands for battery operation in mobile applications and the Internet of Things (IoT). With respect to Power Management of these systems: the challenges presented by the current climate of trends and demands has not necessarily asked circuit designers to "reinvent the wheel (so to speak...)," but rather presented vast frontiers of opportunity for original innovations and novel solutions to keep the metaphorical "wheel" operating well into the future.

This introductory chapter establishes general trends of larger scale integration and process node scaling before narrowing the discussion to shifts in voltage regulator applications that have motivated this body of work. In Section 1.4, the ambition of this work is defined to enable a scalable design approach for Low-Dropout Voltage Regulators. Once the Motivation and Problem are both defined, Chapter 2 summarizes highlights of historical contributions to voltage regulation and recent state-of-the-art published works are used to elaborate upon

the Introduction's established trends and motivation. A scalable solution to the problem is introduced in Chapter 4 to adapt the Ring Amplifier structure with details of a design and physical implementation. The summary of experimental results are then outlined in Chapter 5. A supplemental design guide for the Ring Amplifier design approach and methodology is given in Chapter 3 along with an example case study in Chapter 6 supporting the arguments towards a scalable solution. This paper concludes with Chapter 7 with a summary of original contributions in addition to proposed future work to be considered by the next group of aspiring researchers.

1.2 Technology Trends

1.2.1 On Integration and Scaling

A classical definition of Moore's Law is with respect to transistor density or transistors-per-chip; but in modern times, some have re-interpreted this law to include number of computations-per-second, cost-per-transistor, or even power density. The System on Chip (SoC) is a one chip solution addressing a specific purpose or application; in which, a complete system is realized by the combination of heterogeneous elements with computational and/or functional necessity [1]. The continued large-scale, very-large-scale, and ultra-large-scale integration of SoCs has been completely enabled by the technology trends depicted in Figure 1.1 [2]. Steps into increasingly transistor-dense processes allow for a greater quantity of heterogeneous circuit elements to be combined upon the same chip, leading to expanded functionality of the SoC [3]. Therefore, we can also broaden the re-interpretations of Moore's Law to also include *functional-density*.

Noted by Hershberg [4], Moore's Law considers transistors to be simple switches with `on` and `off` states, neglecting the analog or continuous-time operation of the devices; and thus, the merits or benefits when discussing process node scaling have been largely isolated to digital applications. As the process node size decreases and voltage supplies are reduced, digital circuits have seen increased bandwidth due to higher MOSFET transition frequency (f_T) and reduced power consumption due to lower MOSFET gate capacitance (C_G) [5].

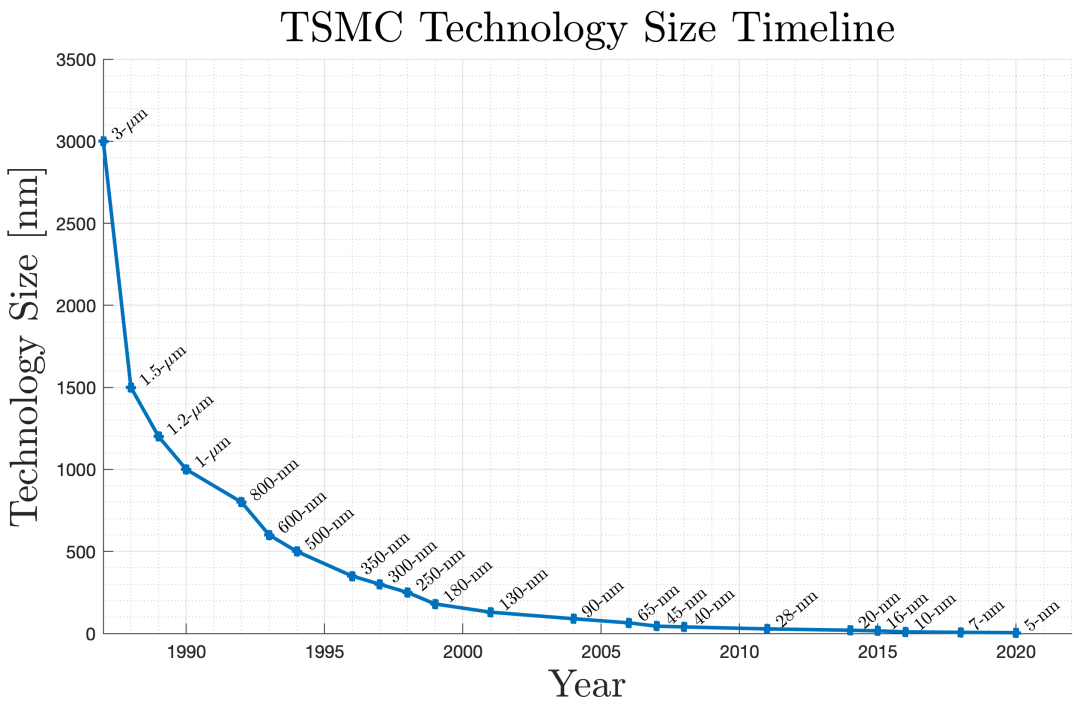


Figure 1.1: Taiwan Semiconductor Manufacturing Company technology node size over time from 3-µm in 1987 to 5-nm in 2020 [2]

The scaling prosperity of digital circuits is converse to the scaling misfortune seen by analog circuit structures. Analog amplifying circuits scaling to finer feature-size process nodes often suffer from less available signal swing as biasing overhead dominates the available voltage, a decrease in intrinsic gain as output resistance (r_o) decreases (demonstrated in Figure 1.2), as well as non-linear operation due to short channel and sub-threshold effects [5]. Thus, process node scaling and the continued validation of Moore's Law has forced designers to more and more frequently consider alternative digital solutions to classically analog problems.

The voltage regulator is one classically analog solution for power management that has undergone vast transformations coinciding with the trends of integration and scaling to meet several circuit requirements. As the performance of analog-based regulators has degraded in smaller process nodes, the precision at which they regulate a linear output voltage across dynamic current load ranges is often foregone in favor of both process node and supply voltage scalability (multi-scalability). This trend has forced the growth of multi-scalable digital-based low-dropout (LDO) regulators; currently widespread in use for fine-grain SoC voltage regulation. Also, due to the increased current demands of low-voltage SoCs, high power efficiency switching regulators have maintained an edge within the voltage regulation market, though they come with a significant trade-off for their area-inefficient but necessary capacitors and inductors. The digital-based LDOs (DLDOs) offer an initially lower circuit footprint are but have worse accuracy and noise performance than their analog counterparts [3]. Analog-based LDOs have continued relevancy with reduced area output capacitor-less (OCL) topologies and digital-assisted multi-loop configurations [7]; however, the main design goal for state-of-the-art voltage regulators is to minimize trade-offs and achieve the best of all worlds: high precision, low noise, high current efficiency, small circuit footprint, and ultimately a ***scalable solution***.

1.2.2 LDO Basics

The Low-Dropout Voltage Regulator is traditionally an analog-based Linear Voltage Regulator (LVR) operating within or near the threshold of the *Dropout Region* [7]. The schematic of a conventional analog voltage regulator with a PMOS pass device is shown in Figure 1.3a and the general behavior is described in Figure 1.3b. Operating within the

Linear Region, the LVR can maintain an output value nearly independent of disturbances and variations of the input voltage (V_{IN}) or load current (I_{LOAD}). This would be the ideal region of operation for the LVR if stability and line/load regulation were the sole design objectives. As the LVR approaches the *Dropout Region*, the output pass device moves out of saturation and into triode operation and the voltage dropout (V_{DO}) becomes entirely dependent on the I_{LOAD} and the drain-to-source resistance of the pass device ($R_{DS,PASS}$) as shown in Equation (1.1) [7].

$$V_{DO} = V_{IN} - I_{LOAD} \cdot R_{DS,PASS} \tag{1.1}$$

This allows for the maximum power efficiency of the LVR at a cost of reduced loop stability and greater dependence of output voltage (V_{OUT}) to dynamic behavior of V_{IN} and I_{OUT}. However, dominant pole compensation techniques can recover the loop stability and snappy transient response techniques can mitigate recovery overshoot and undershoot of V_{OUT}.

The maximized efficiency of the LDO regulator appeals directly to battery-powered applications; but the LDO also competes with the more efficient switching regulator approach within this market. The design edge of LDOs over switching regulators is based in speed and simplicity of the loop control; where switching regulators can share both digital and analog elements within the control path that can limit the response time to fast transient load demands [7]. Switching regulators demonstrate higher efficiency than LDOs, but also contribute more noise due to unfiltered switching artifacts on the output voltage; furthermore, switching regulators can require bulky passive components such as inductors and capacitors that can be placed off chip limiting the regulator's performance. In some practical applications the switching regulator is used in coordination with multiple distributed Point-of-Load (PoL) LDO regulators to reduce power supply noise locally for sensitive circuits or provide fine-grain voltage regulation [8]. A summary of the fundamental regulator topologies is given in Table 1.1.

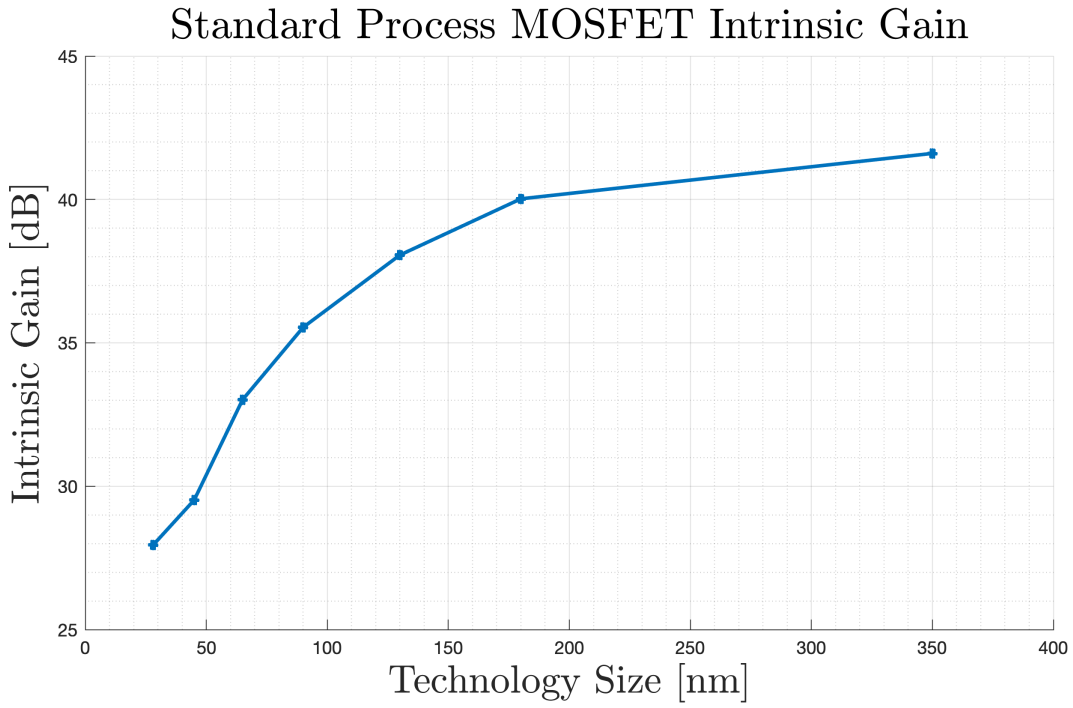


Figure 1.2: MOSFET intrinsic gain for multiple standard CMOS process technologies from 28-nm to 350-nm [6]

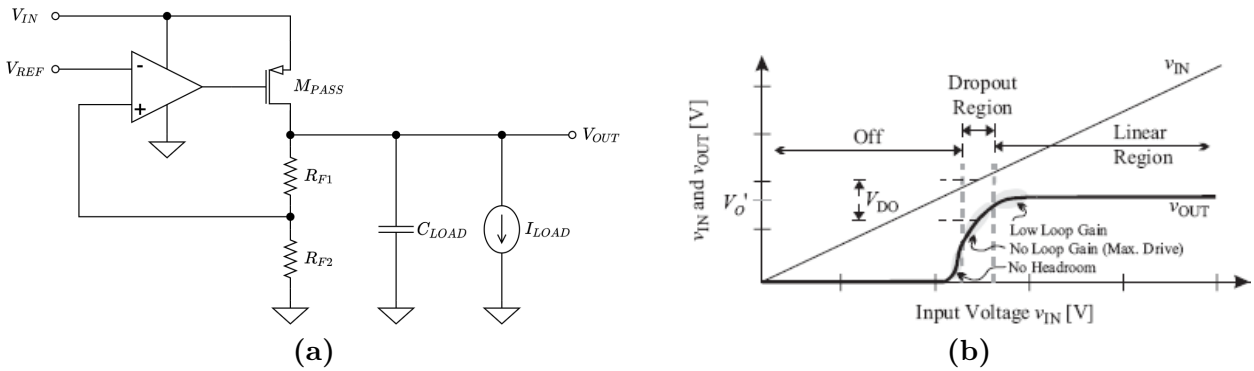


Figure 1.3: Conventional voltage regulator (a) schematic and (b) behavior [7]

1.3 Motivation

As fabrication technology for integrated circuits continues to advance into smaller and smaller node sizes, the demands and limitations stepping into each smaller process size have shifted to favor scalable digital-heavy structures and topologies. Recent published advancements in voltage regulation have been monopolized by these topologies that demonstrate suitability for low voltage applications, where precision and noise design targets have been relaxed, if not abandoned [3]. This progression has compounded the operational limitations on analog-heavy on-chip peripheral circuitry required for data converters and sensors providing the *in-real-life* (IRL) interfaces with the SoC's digital elements and the increasingly ubiquitous IoT.

In response to these trends, the Ring Amplifier originally proposed by Hershberg *et al.* [9] has grown into a popular choice where inherent scalability and analog behavior are concurrent design objectives. Previously published use of the Ring Amplifier has been almost entirely isolated to applications of data converters, a field that has been massively impacted by technology node scaling as it stands upon the precipice for advancing the balance of trade-offs for speed, accuracy, and efficiency. Continued pushes to expand the diversity of applications have contributed to the recent emergence of Ringamp-based LDOs (RLDOs) [10]. These examples demonstrate the potential benefit of Ring Amplifiers within Voltage Regulator applications, that can leverage the Ringamp's high slewing capabilities and high loop bandwidth for fast response to large transient loads [11, 12, 13]. The previous work has proven successful and generated competitive implementations, but the limited body of work does not establish ringamp-based LDOs (RLDOs) as current leaders within the published state-of-the-art topologies. Thus, an opportunity exists for a breakthrough execution of a RLDO that can advance the art by re-establishing the balance of LDO design trade-offs and pushing the metaphorical analog "wheel" far into the future for Power Management of System on Chips.

1.4 Problem Statement

Can there be a LDO Voltage Regulator capable of bridging the gap between Analog and Digital-based LDOs for fine-scale SoC regulation? An LDO that can simultaneously achieve *high precision*, *high power supply rejection (PSR)*, *high current efficiency*, *dynamic voltage scaling (DVS) capabilities*, and *process technology node scalability*?

The trade-off with selecting any voltage regulation scheme (*e.g.*, switching, LVR, LDO) is that no known examples can simultaneously achieve high precision, low noise, high current efficiency, small circuit footprint, or high scalability; but rather, can achieve a specific portion of these desired traits much better than adjacent voltage regulation schemes. For example: Low-power Analog-based LDOs have the least noise contributions and highest precision, Digital-based LDOs are highly scalable and can be implemented in very little chip area, switching regulators have the highest operating power efficiency. However, all these regulation schemes often fail to remain competitive with performance metrics at which they do not excel. This work will leverage the inherent scalability of the inverter-based ring amplifier and develop a general voltage regulator topology and design methodology to push these trade-off limitations and achieve multiple modes of success. The scope of this work will be limited to fine-grain point-of-load voltage regulation, which is an appropriate role for recent SoC applications. This limitation will focus the selection of comparable state-of-the-art LDOs to those that will reinforce the desired performance metrics and ultimately qualify a successful implementation of this body of work.

1.5 Original Contributions

This body of work will demonstrate successful completion of a Ringamp-Assisted Analog LDO that advances the state-of-the-art for Ringamp-based LDOs by establishing performance metrics leading all other known RLDO examples. Furthermore, this work is the first major body to reverse the role of the Ring Amplifier from central to support, opening the door for a wider use of ringamps across multiple potential applications that would benefit from the high-speed, analog behavior and inherent scalability of the ringamp for an improvement

to dynamic, on-demand, or need-based amplification. The original contributions of this work can be summarized as follows:

1. Advance the state-of-the-art for Ringamp-based LDOs with leading performance metrics
2. Bridge the gap between ALDO and DLDO performances for fine-grain SoC regulation
    a. High precision
    b. High PSR
    c. High current efficiency
    d. Dynamic voltage scaling (DVS) capable
    e. Process technology scaling capable
3. Develop a Ring Amplifier design methodology for a range of applications
    a. Reverse the role of the Ring Amplifier from central to support, opening the door for a greater diversity of application
        i. Scalable analog behavior
        ii. Dynamic, on-demand, or need-based amplification
    b. Create a supplemental ringamp design guide with intuitive explanations behind the large signal amplifier and its dynamic operating behavior
    c. Develop script-based tools to increase productivity and decrease design time

Table 1.1: Comparison of Regulator Topologies for SoC Applications [7]

Topology	Advantage	Disadvantage
Analog LDO	• High precision • Fast response • Low noise	• DVS-incapable • Low scalability • Moderate efficiency
Digital LDO	• High scalability • DVS-capable	• Quantization noise • Low precision • Slow response • Lower efficiency
Switching	• High efficiency	• Bulky passives • Switching noise • Slower response

Chapter 2

Literature Review

2.1 Voltage Regulation in Literature

The objective of this section is to trace the trends of miniaturization both in application and technology from the conception of circuit integration to the current state-of-the-art contributions for fine-grain voltage regulation. This will be accomplished beginning with general context into the period-relevant challenges being addressed by significant historical contributions and a fundamental discussion of circuit topologies in Section 2.1.1. Section 2.1.2 establishes context for the narrowed scope of this work to point-of-load (PoL) and fine-grain regulators by introducing fundamental power distribution schemes and introduces some relevant technical background. This culminates in Section 2.1.3 with an overview of current state-of-the-art voltage regulators for fine-grain general SoC applications and discusses the needs and demands addressed by the more notable contributions.

The discussions throughout this chapter will provide comments and comparisons of the performance metrics for any reviewed approach in the literature. It could become difficult to recall in-text definitions of these metrics if only provided casually and in-flow. To assist the reader with any quick references necessary while navigating through the Literature Review Chapter, a compilation of all mentioned performance metrics for low-dropout voltage regulators are summarized and defined Figure 2.1.

Summary of LDO Performance Metrics

1. Input/output voltage range
   a. V_{IN} – range of operational supply voltage
   b. V_{OUT} – range of regulated output voltage
   c. Mostly dependent on process technology
      i. Not always a fair comparison
      ii. Minimum operation bound to technology
2. I_{OUT} – Output current range
   a. Dictated by size of pass device M_{PASS}
   b. Larger area devices → larger I_{OUT}
   c. Can indicate drive strength of error amp
3. I_Q – Quiescent current draw
   a. Low I_Q better suited for mobile applications
   b. Shown with I_{OUT} to demonstrate LDO efficiency
4. PSR – Power supply rejection
   a. AC gain or attenuation from V_{IN} to V_{OUT}
   b. Measure of noise isolation to V_{OUT}
   c. Not typically reported for digital topologies
5. V_{DO} – Dropout voltage
   a. Minimum V_{DO} bound to process technology
   b. Dictated by size of M_{PASS} and $|I_{OUT}|$
   c. Can indicate drive strength of error amp
6. C_{TOTAL} – Total capacitance
   a. Total capacitance necessary for stable operation
   b. Sum of internal and external capacitance
   c. Statement to ease of integration
7. ΔV_{OUT} – Overshoot or undershoot voltage
   a. Output response to transient load-current step
   b. Demonstrates slew-rate and drive of error amp
   c. Measurement of accuracy and precision of LDO
8. T_{SETTLE} – Settling time
   a. Accuracy and speed of LDO
   b. Indicates loop stability in analog topologies
      i. Phase margin PM
      ii. Damping ratio ζ
   c. Indicates loop delay in digital topologies
      i. Binary output value search
      ii. Clock speed
      iii. Sample rate
9. *FOM_1 – Hazucha Figure of Merit [14]

$$FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right)$$

10. *FOM_2 – Guo Figure of Merit [15]

$$FOM_2 = \left(\frac{\Delta t_{edge}}{1\text{ ps}}\right)\left(\frac{\Delta V_{OUT} \cdot I_Q}{I_{O,MAX}}\right)$$

11. Active Area – Size of active circuit elements
    a. Minimum size is bounded by process technology
    b. Indicates complexity of circuit implementation
    c. Statement to ease of integration

* Lower FOM is better performance

Figure 2.1: Summary of LDO performance metrics used within this dissertation

2.1.1 Historical Contributions

Although the first working integrated circuits were developed by Jack Kilby shortly after joining Texas Instruments in 1958, full circuit integration failed to become mainstream until the late 1960s [16]. Prior solid-state voltage regulation was primarily for self-calibration of instrumentation and was provided by mercury cell batteries. These battery references transitioned into Zener diode-based references and expanded to Current Regulator Diodes as JFETs and semiconductor technology continued to develop [17]. The first monolithic voltage regulator was released in 1969 by National Semiconductor. The BJT-based LM109 was designed by Bob Widlar shortly after he produced the first commercial monolithic Operational Amplifier (LM702) and the fundamental Bandgap Reference (BGR) [17]. The work presented by Widlar [18] demonstrates design trade-offs weighted heavily in favor of greater ease of integration for circuit board level or "on-card" applications. The resulting design with integrated Darlington Pair pass devices reduced the required external terminals so that the LM109 regulator could be used in a standard three terminal transistor package that enabled more area efficient circuit board designs [18].

As digital complementary MOS (CMOS) technology and Large-Scale Integration (LSI) advanced through the 1970s to address a shift of technology towards specific applications (*e.g.*, electronic calculators and wristwatches), it became increasingly more "cumbersome" to maintain separate chips for solely analog or digital functions due to economic disadvantages and peripheral circuit requirements [19]. This pushed analog designers to explore purely CMOS variations of classic analog structures for more complex LSI applications [19]. The integration of both analog and digital CMOS circuits further enabled ASIC development and primitive SoCs with combinations of heterogeneous structures performing functions such as data conversion, analog arithmetic, memory, and digital computation [19]. However, as channel lengths approached and even descended below a single micron (1 µm), the hot-electron injection (HEI) phenomenon (characterized by Ning *et al.* [20]) emerged that resulted in unwanted voltage threshold shifts if supply voltages, or more specifically drain-to-source voltages were not reduced. This posed a design challenge in applications like integrated RAM in the 1980s and early 1990s that necessitated both 5 V supplies for

input/output (IO) peripherals and 3.3 V supplies for digital circuitry more vulnerable to HEI. The option of dedicating a greater number of package pins to off-chip voltage supplies resulted in undesirable limitations to the chip functionality. This put pressure on chip designers to develop integrated voltage-limiting circuits to use standard externally sourced 5 V supply and provide on-chip regulation for an internally-sourced 3.3 V supply; thus, successfully mitigating HEI and pioneering approaches to multiple monolithic voltage domains [21, 22, 23].

The voltage regulators originally proposed for sub-micron integration became the fundamental voltage regulator topologies that continue to be adapted for use in contemporary voltage regulators . These basic circuit structures were previously compiled by Den Besten and Nauta [24] and are redrawn in Figure 2.2. The first two topologies of Figures 2.2a and 2.2b are purely analog in nature, a CMOS-based OTA driving the gate of a pass device with negative feedback. With the PMOS pass device in Figure 2.2a, the peak output voltage is maximized since the PMOS can be driven deep into linear operation. Since the PMOS pass device's drain is seen at the output voltage V_{OUT}, the output impedance can be relatively high necessitating a large external (off-chip) output capacitor C_{EXT} to ensure wide range stability [7]. The NMOS pass device in Figure 2.2b has a relatively low output impedance since the source terminal is driving V_{OUT}; and is thus more stable than the regulator using a PMOS pass device without the need for a C_{EXT} [24]. The topology shown in Figure 2.2c uses a charge pump to drive the gate of the NMOS pass device. The benefit of this more digital approach is the high stability and low dropout voltage when the charge pump can exceed the value of the positive supply voltage V_{DD}; however, the lack of negative feedback leads to inaccurate regulation of V_{OUT} [24]. Later, some charge pump-based examples would adopt feedback sensing mechanisms, either analog, digital, or of some hybrid approach to improve accuracy limitations.

Through the 1990s, the demands of on-chip voltage regulators were increasing to support mobile and automotive applications that required larger load currents and higher current efficiency [24, 25]. These increasing demands pushed the limits of footprint area for finer scale integration; thus, limiting the ability for analog LDOs to reach loop stability with available architectures. A widely adopted approach was to use a matched output device

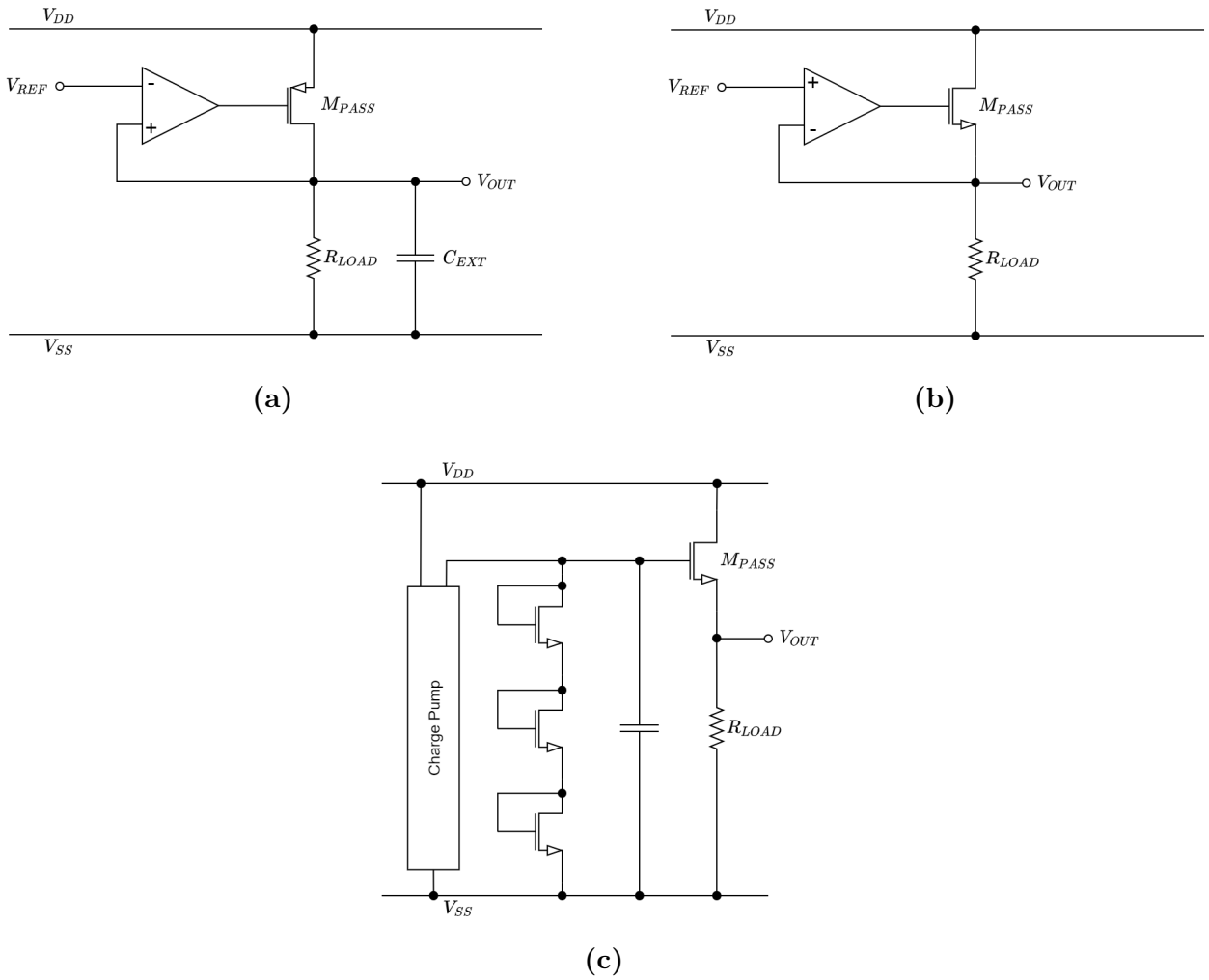


Figure 2.2: Original sub-micron voltage regulator topologies (a) OTA with PMOS pass device in feedback [22, 23], (b) OTA with NMOS pass device in feedback [23] (c) Charge pump with NMOS pass device without feedback [21]

replica or mirror load, as shown in Figure 2.3a [24]. This approach isolated the regulator circuit from the dynamic loading conditions of the output device by creating a smaller replica device to be used in the control loop that was physically located in the center of the output device transistor array to achieve optimum process and thermal matching. The main disadvantage to this approach is the inability to regulate responses to dynamic loads in favor of wide range stability without large-area compensation capacitors. Noted by Den Besten and Nauta [24], this inability to recover from transient loads was not necessarily an issue considering the circuitry necessary for feedback loops to achieve the same stability would have been so low bandwidth the results would have been similar. The circuit proposed by Rincón-Mora and Allen [25], shown in Figure 2.3b, responded to dynamic transient loads by body driving the pass device with a current mirror-based boost circuit. This example was fabricated in a low-cost 2-µm BiCMOS process with a goal of demonstrating techniques for low operating voltage capable LDO regulators. The experimental circuit could operate with $V_{IN} = 1\,\text{V}$ and driving $I_{LOAD} = 18\,\text{mA}$ while consuming 23 µA of quiescent current I_Q in the lowest voltage mode and with $V_{IN} = 1.2\,\text{V}$ the regulator was capable of driving $I_{LOAD} = 50\,\text{mA}$ and $I_Q = 230\,\mu\text{A}$. With the current boost engaged, the regulator had an 83 % droop improvement of 19 mV during a load pulse of 0 mA to 50 mA [25].

In attempts to further enable fully integrated voltage regulation for the growing SoC applications, much work was done in the 2000s to reduce the on-chip area of the LDOs. The much lower dropout voltages of the PMOS pass device compared to the NMOS variant was much preferred for LDO applications. The greatest disadvantage of the basic PMOS LDO topology (shown previously in Figure 2.2a) is the necessity for dominant pole compensation to prevent loop instability resulting from dynamic poles depending on the output current loading conditions. Stabilizing the poles at the output node required a discrete external compensation capacitor C_{EXT} that was often too large of a capacitance for consideration of on-chip integration. Thus, motivated by the drive for circuit volume compactness and still favoring the lower V_{DO} of the PMOS pass device, additional compensation techniques were explored by Leung and Mok [26] to improve the PMOS LDO's loop stability without reliance on C_{EXT}. Leung and Mok [26] adapted Damping-Factor-Control (DFC) and other pole-splitting techniques previously common to amplifiers with large capacitive loads. The

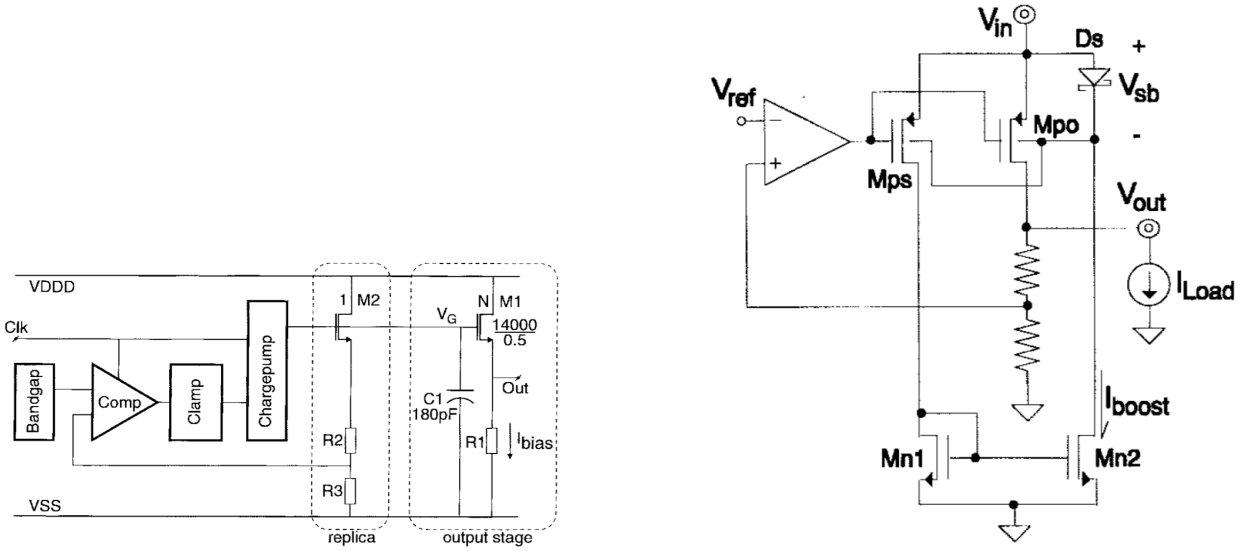
circuit in Figure 2.4 shows this DFC inverting gain stage with the Miller compensation by $Cm1$ and the pole-splitting achieved by $RF1$, $RF2$, and $CF2$. The work was fabricated within in a 0.6-µm CMOS process and was able to regulate $V_{OUT} = 1.3\,\text{V}$ with $V_{IN} = 1.5\,\text{V}$ at $I_{LOAD} = 100\,\text{mA}$ while $I_Q = 38\,\mu\text{A}$ [26].

The work by Leung and Mok [26] demonstrated a successful output capacitor-less analog LDO by moving the dominant pole of the system to an internal node. But this approach also weakened the LDO's ability to maintain constant output voltage during large transient loading conditions. In previous LDOs the large output capacitor would also serve as a charge reservoir to compensate for changes in the load. Without this compensation the overshoot and undershoot voltage at V_{OUT} was almost completely reliant on the slew rate of the error amplifier. The work by Milliken *et al.* [27] improves the transient response of the output capacitor-less LDO by inserting an auxiliary current amplifier between the LDO output node and the gate of the pass device shown in Figure 2.5. The differentiator amplifier senses the dynamic I_{LOAD} and provides a current boost to charge the gate of the pass device for faster transient response when the error amplifier is slew-limited, or the control loop was sluggish due to compensation schemes [27]. This work reduced the ΔV_{OUT} previously demonstrated by Leung and Mok [26] from 130 mV to 90 mV. This was done in a 0.35-µm process and regulated $V_{IN} = 3\,\text{V}$ to $V_{OUT} = 2.8\,\text{V}$ with $I_{LOAD} = 50\,\text{mA}$ and $I_Q = 65\,\mu\text{A}$ [27].

Removing the need of the off-chip capacitor was a critical inflection point in the development for contemporary LDOs. The achievement of this milestone further advanced progress towards more complex systems on chips. As technology process nodes pushed deeper into sub-micron gate lengths, so too did the transistor density and therefore power density of these SoCs. Smaller transistor geometries allowed for higher switching speeds for digital circuits that generated larger dynamic power losses described by Equation (2.1) [1, 28].

$$P_{dyn} = C_{eff} V_{DD}^2 f_{sw} \tag{2.1}$$

These losses were fundamental challenges to battery-powered applications, and necessary to address so to avoid bulky heat-sinks and thermal management techniques while market demands were shifting towards reduced circuit volume for mobile applications. Solutions such



(a) **(b)**

Figure 2.3: Prior analog LDO examples: (a) Charge pump-based LDO with pass device replica [24] (b) Analog LDO with current boost [25]

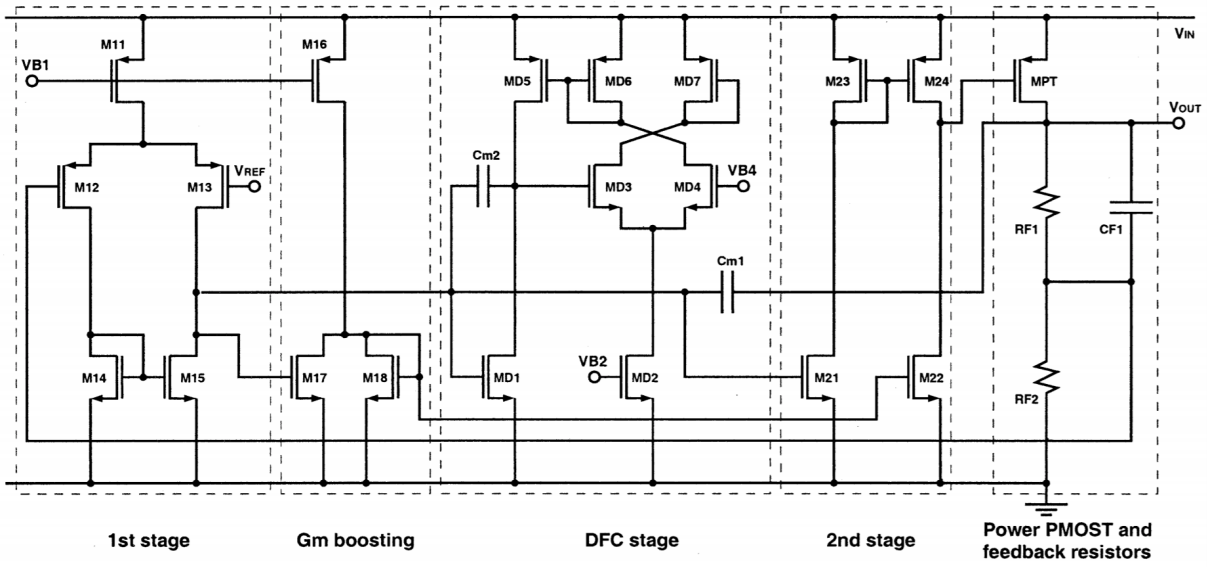


Figure 2.4: Original output capacitor-less LDO schematic [26]

as frequency scaling by reducing the switching frequency f_{sw} could be used to diminish P_{dyn}; however, voltage scaling had a more significant impact due to the quadratic proportionality of V_{DD} to P_{dyn}. The result of voltage scaling also reduces power losses due to static sub-threshold current leakage (also negatively impacted by higher transistor densities) as described by Equation (2.2) [1, 28].

$$P_{stat} = I_{stat} V_{DD} \tag{2.2}$$

Thus, voltage regulator designers would strive for low voltage headroom operation beyond the technology specific limitations to facilitate improved power efficiencies of downstream loads; a trend that continues to dominate current state-of-the-art LDO designs.

Targeting improved efficiencies, some voltage regulator solutions diverged from analog approaches into switching regulators or fully digital LDOs. Switching regulators offered the highest efficiencies of all the voltage regulation techniques; the earliest example of a partially integrated switching regulator by Kim and Horowitz [29] demonstrated a power efficiency near 95 %. The output voltage of switching buck converters (like that shown in Figure 2.6a) depended on duty cycled controlled pulses being integrated by a LC low-pass filter. For this reason, the regulator efficiency was uncorrelated to any pass device's continuous on-state dropout voltage, but rather the losses related to parasitics elements and switching behavior. In the most basic understanding, switching regulators perform as a DC-transformer where $P_{IN} \cdot \eta = P_{OUT}$ and η is the regulator's efficiency.[1] This improvement to efficiency came at a significant cost for scalability and full integration, requiring large off-chip inductors and capacitors [14]. A more scalable approach was the Digital LDO (DLDO). The original DLDO by Okuma *et al.* [30], shown in Figure 2.6b, was capable of operation with V_{IN} down to 500 mV. The output stage consisted of 256 parallel pass devices, for a 256 bit resolution current range. For maximum I_{LOAD}, all the 256 bits would be flipped to `1`, for $I_{LOAD} = 0$

[1] For those readers wishing for an extra step into switching buck regulator theory: $P_{IN} = P_{OUT}$ could also be equated to $V_{IN} \cdot I_{IN} = V_{OUT} \cdot I_{OUT}$ after applying Ohm's law. Continuing this transformer analogy, the duty cycle D of the control square wave would be the equivalent of a transformer's turns ratio where $D \cdot V_{IN} = V_{OUT}$ and $(1 - D) \cdot I_{IN} = I_{OUT}$. And for those readers seeking a significantly deeper dive (*á la* Mariana Trench) into the theoretical and physical analyses of switching Power Electronics should explore the text by Erickson and Maksimović [31]

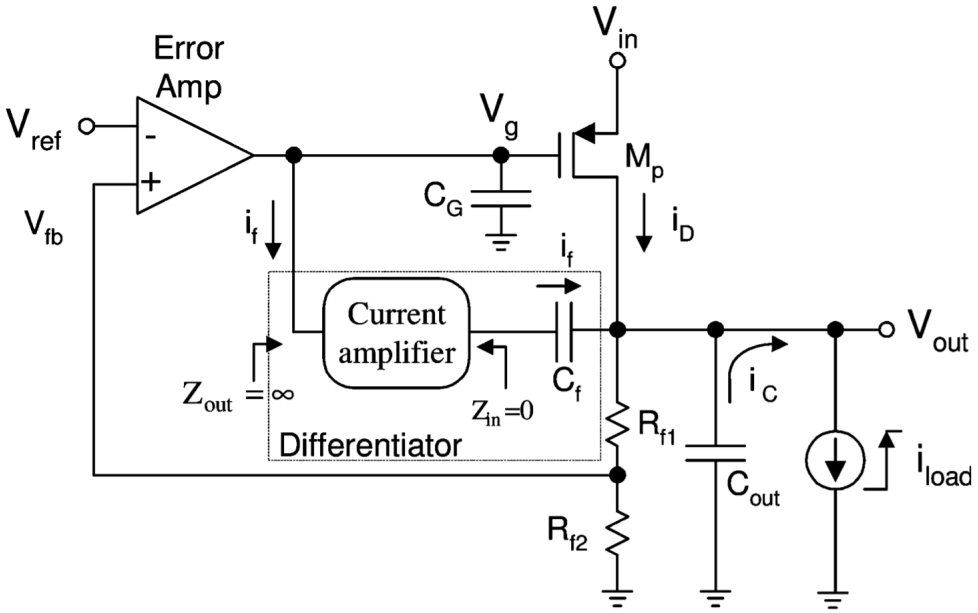
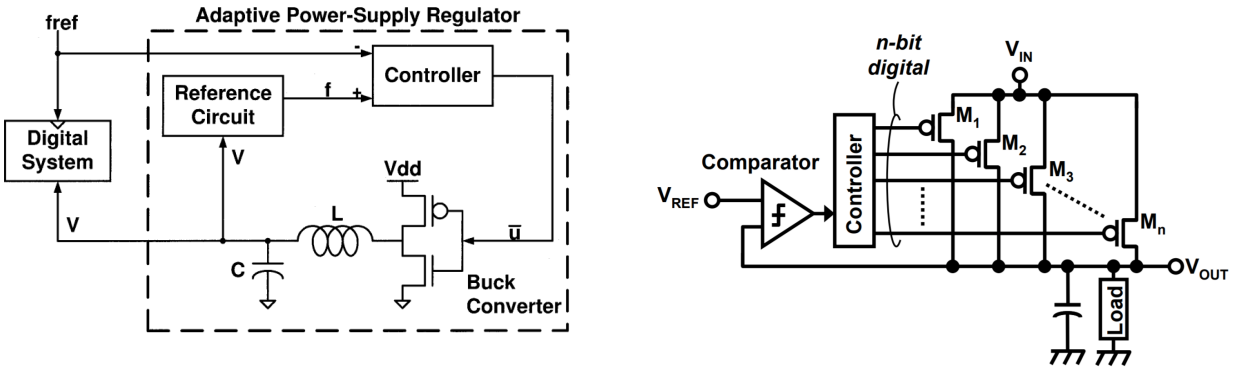


Figure 2.5: Output Capacitor-less LDO schematic with on-demand boost [27]



(a) **(b)**

Figure 2.6: Early non-analog voltage regulators (a) partially integrated switching regulator [29] (b) original fully-digital LDO [30]

allthe bits would be flipped to `0`, and then any number of the bits could be assigned a logic level of `1` or `0` for the LDO to deliver any of the 256 discrete output current levels [30]. The DLDO could be implemented with the very same digital elements that process node scaling and voltage scaling benefited; therefore, this type of LDO was very attractive for pure digital applications. The most apparent disadvantage of the DLDO is that the accuracy was limited to the resolution of discretized output current values; additionally, the response time of the system could be limited by the binary output value search and synchronous control [32].

The most historically relevant voltage regulators previously mentioned are summarized in Table 2.1. The ultra-fast load regulation LDO shown in Figure 2.7 demonstrated the greatest (lowest) Figure of Merit (FOM), originally introduced by the author of this work, and described by Equation (2.3) [14].

$$\mathrm{FOM}_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right) \tag{2.3}$$

Equation (2.3) from Hazucha *et al.* [14] has become the fundamental FOM for comparing LDOs due to the consideration of high impact LDO performance metrics that have maintained relevancy even through more contemporary works. Additionally, several general trends can be deducted from this summary in Table 2.1. Firstly, the reduction or scaling of process technology from 2.0-µm in 1998 to the 65-nm in 2010. The decline in circuit area footprint coincides with this scaling, but also the reduced output capacitor size. The exception to the lower capacitor value is the original DLDO presented by Okuma *et al.* [30]; however, poorer performance (especially with respect to the high FOM score of 270 ns) is indicative of the following trajectory for nanoscale LDOs that favored multi-scalable digital solutions over high performance or low current overhead analog topologies.

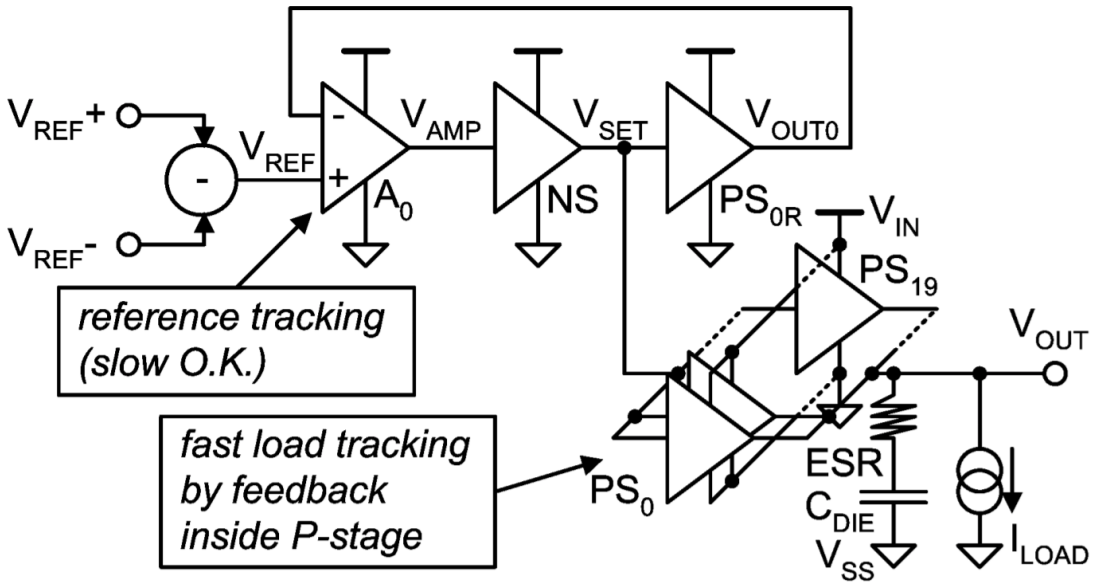


Figure 2.7: Ultra-fast load regulation LDO [14]

Table 2.1: Historically Significant Published LDO Performance Metrics

Parameters	**Unit**	**Rincón-Mora and Allen [25]**	**Kim and Horowitz [29]**	**Leung and Mok [26]**	**Hazucha *et al.* [14]**	**Milliken *et al.* [27]**	**Okuma *et al.* [30]**
Year		1998	2002	2003	2005	2007	2010
Technology	[nm]	2.0-µm (BiCMOS)	250	600	90	350	65
Control		Analog w/ Current Boost	Switching w/ Digital Sliding Control	Analog Output Capacitor-less	Analog Ultra-Fast Load Regulation	Analog Output Capacitor-less	Fully Digital
$\mathbf{V_{IN}}$	[V]	1-1.2	2.5	1.5-4.5	1.2	3	**0.5**
$\mathbf{V_{OUT}}$	[V]	0.9	1.1-2.3	1.3	0.9	2.8	**0.45**
$\mathbf{I_{OUT}}$	[mA]	50	2.5	**100**	**100**	50	0.2
$\mathbf{I_Q}$	[µA]	23-230	273	38	**6000**	65	**2.7**
$\mathbf{V_{DO}}$	[V]	0.232	n/a	200	300	200	**0.05**
$\mathbf{C_{OUT}}$		**47 µF**	**21.6 µF**	**0-10 nF**	**600 pF**	**0-100 pF**	100 nF
$\mathbf{\Delta V_{OUT}}$	[mV]	**19**	**15**	**150**	90	90	40
$\mathbf{T_{SETTLE}}$	[µs]	**1.8**	80	**1.6-2**	n/a	15	**590**
$\mathbf{FOM_1}$ *	[ns]	8.2	n/a	4.9	**0.032**	15	**270**
Active Area	[mm^2]	1.379	**1.43**	0.307	0.098	0.120	**0.042**

Leading performance **Lagging Performance**

$$* \; FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right) \; [14]$$

2.1.2 Granular Voltage Regulation

As process node scaling enables a higher quantity of transistors on chip, the Power Management and Power Distribution Network (PDN) have grown from elemental support roles into independent fields of study for SoC design and applications. The increasing number of on-chip heterogeneous elements has created a greater challenge for providing well-regulated power domains uniquely optimized for downstream circuitry. It has become unrealistic to address the specific needs for each unique element directly from off-chip power sources for reasons including the limited number of package pins and chip pads, parasitic losses associated with chip to pin to board connections, and on-chip metal routing densities. Ergo, the need for a granular approach to providing voltage regulation has grown along with the increasingly more functionally-dense SoCs enabled by process node scaling [8].

The more common PDN configurations are shown in Figure 2.8, featuring distributed LDOs for point-of-load (PoL) voltage regulation [8]. These configurations' hierarchy begins with a single or multiple highly efficient switch-mode power supplies (SMPS) providing initial regulation for downstream localized power conditioning. In more complex heterogeneous SoCs, the downstream regulation can support a larger area over multiple sub-domains but will ultimately accommodate the needs of fine-grain or PoL power regulation. As depicted in Figure 2.8, each voltage cluster is divided into smaller unique power domains or "Voltage Islands" where the voltage can be independently controlled, scaled, and optimized to address the fine-grain demands of each element inhabiting a given Voltage Island [28].

The initial power conditioning by the high efficiency SMPS had typically been implemented by fully-off-chip regulation due to their area inefficient passive components (*e.g.*, magnetic core inductors and large volume capacitors); however, as technology scaling enabled the increasing complexity and demands of contemporary SoCs, alternative configurations were explored and adopted. The work by Waldron *et al.* [33] provided an extensive evaluation of co-packaged power converters and partially integrated converters dubbed "Power Supply in Package" or PSiP approaches. The work concluded that finer feature sized technology and their higher associated switching frequencies *has* and *would continue to enable* more compact

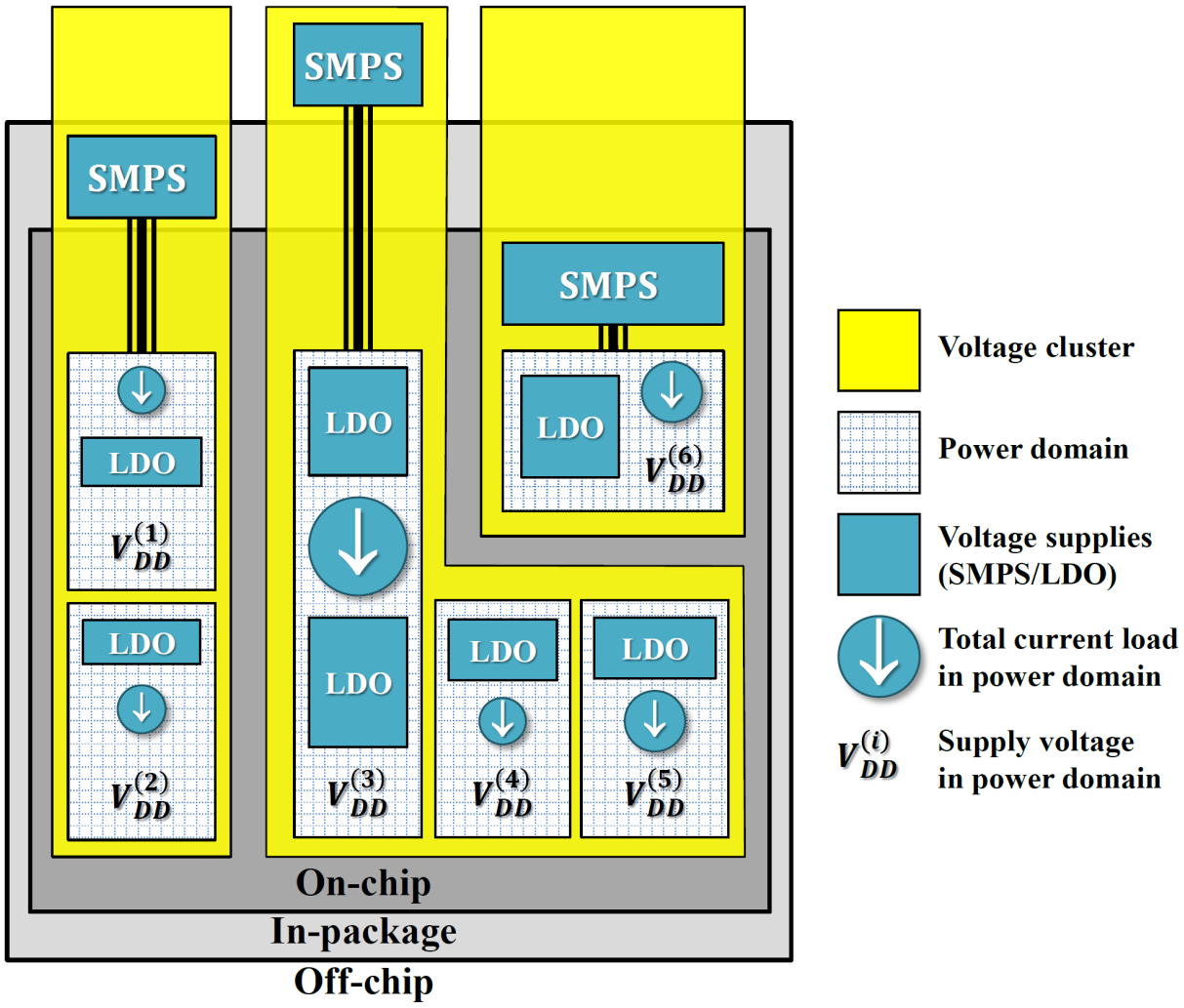


Figure 2.8: Heterogeneous power delivery with multiple power domains [8]

inductors and transformers, further propelling in-package integration and eventually fully on-chip integration. The work also demonstrated that by eliminating off-package connections between the power converters on the printed circuit board (PCB) and the packaged chip die, the parasitic power losses inherent to long interconnect paths would then be significantly reduced. Therefore, the PSiP approach would promote a more highly efficient PDN than previous fully-off-chip regulation schemes [33].

Coincidentally, while Waldron *et al.* [33] were speculating on the potential of widespread fully integrated power supplies, Intel had developed their 4th generation Core™ Haswell microprocessor chips, powered by their version the "Fully Integrated Voltage Regulator" or FIVR [34]. These distributed synchronous buck converters were switched at a frequency of 140 MHz that allowed air core inductors (ACI) to be integrated on the bottom metal layer of a flip chip package. The decoupling was provided by both integrated metal-insulator-metal (MIM) capacitors and on-package ceramic capacitors [34]. More recent FIVR advances noted by Sankarasubramanian *et al.* [35] in 2020 have enabled Magnetic Inductor Arrays (MIA) constructed from magnetic iron alloy micro-particles suspended within an epoxy matrix to be fully integrated on Intel's 10th generation Core™ Comet Lake microprocessor. The MIA demonstrated a four times higher inductance density than the previous Intel ACI technology, that translated to higher quality factor, lower output ripple and higher peak efficiencies. The cost associated with MIA is more significant than the ACI; therefore, only select voltage domains would see the MIA and the remaining would continue to use the ACIs. These inductors still consume volume within the package and add overall costs to the fabrication process [35]. It should also be noted that Intel's main competitor, AMD, continues to use dynamic voltage and frequency scaling (DVFS) with distributed LDOs in their Zen series ×86 microprocessors to achieve similar performance metrics to the Intel chipsets [36].

The innovations towards FIVRs have been tremendous towards support for SoCs; however, the role they play in the PDN is typically well beyond the capabilities of any general purpose LDO. Consider the previous Intel microprocessor examples, the 22-nm implementations of the 4th generation Core™ chips were capable managing up to 700 A per die with a current density of 40 A/mm^2 [34, 37]. Though there were many FIVR regulated domains within those values, their individual output currents approached 1 A; that is still

an order of magnitude greater than the highest output current presented from historically significant LDO publications summarized in Table 2.1. Hence, the most fundamental difference between the course regulation provided by the SMPS and the fine-grain LDO is the magnitude of current demands.

The high current demands can also be further expanded into the quality of regulation by what types of circuits are being supported. For less heterogeneous structures, like multi-core CPUs, the need for fine-scale regulation is weighted differently than if there were many heterogeneous small-scale elements with unique power demands; moreover, the accuracy demands of all-digital circuitry have become much less strict and lean more towards fast response and dynamic voltage scaling (DVS) [3]. This diversity in demands has also led towards the divergence of approaches to address voltage regulation, where there are roles to play for switching regulators as well as both digital and analog LDOs.

2.1.3 Contemporary Fine-Grain LDOs

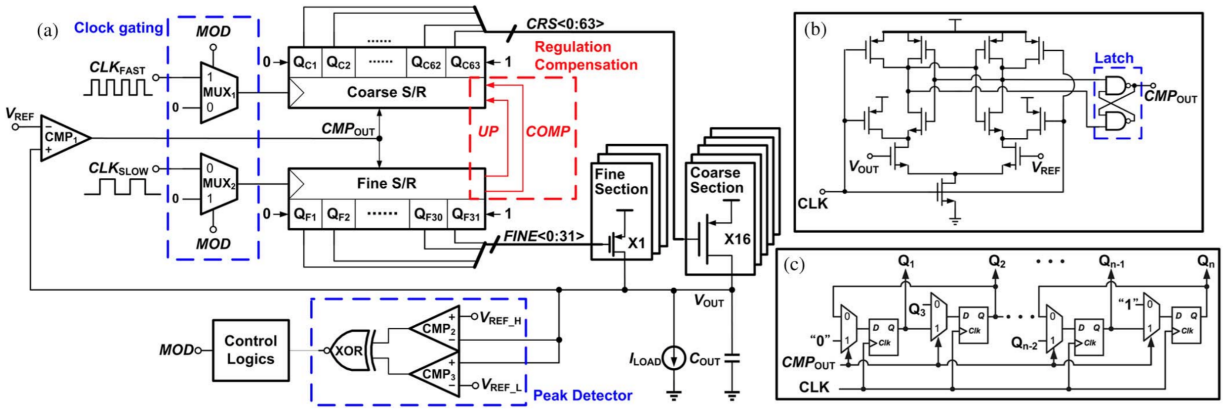
For SoC applications, Dynamic Voltage Scaling (DVS) has become a standard for improving power efficiency of digital circuits; thus, contemporary LDOs must be able to support voltage scaling by operating at a much lower voltage headroom (typically near threshold voltages for a given process). Analog circuits, already suffering from degradation due to process node scaling, are further impacted by the reduced voltage headroom of DVS when the process technology limitations require gain enhancement techniques such as cascoding to achieve the desired loop gains [32]. This has given considerable room for digital-based LDOs to demonstrate their value within the SoC application space. Though the current DLDO offerings provide solutions with DVS and process scalability, the performance of DLDOs still lags to their contemporary analog LDO (ALDO) counterparts with respect to speed, accuracy, and noise. Some recent advances in LDOs have attempted to bridge the gap between DLDO and ALDO regulators by offering Analog-Assistance to DLDOs or Digital-Assistance to ALDOs [32, 38]. But, even with the partially mitigated shortcoming of each approach, digital or analog, these underlying challenges remain.

One of the main issues separating the DLDO from the ALDO is noise management and intrinsic noise contributions. In typical applications, the fine-grain LDO is downstream from

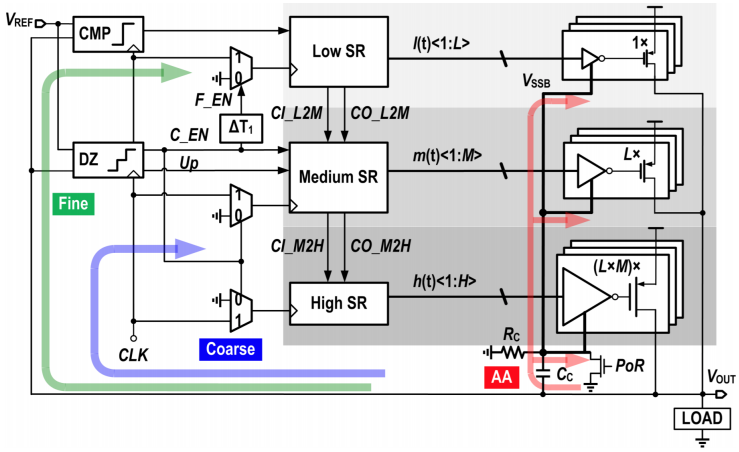
a DC-DC switching regulator that can generate considerable ripple on the supply lines. For ALDOs, if the noise exists within the gain bandwidth, it is continuously suppressed through negative feedback. The DLDO suffers worse power supply rejection (PSR), limited by a low sample rate to improve dynamic switching losses; and furthermore, by the finite set of output values available to adjust for power supply variations. The only mechanism for the DLDO to address power supply noise is the slight attenuation offered by the on-state resistance of the pass device array and any filtering by parasitic LC components, that are often reduced in size to enable fully integrated regulation. Another noise issue for the DLDO is its own intrinsic contributions. A common circumstance exists where quantization error couples to the output of the regulator, this is in the form of a static ripple known as limit-cycle oscillation (LCO) [32]. The multi-loop DLDOs published by Huang *et al.* [39, 40] in 2016 and 2018 (shown in Figures 2.9a and 2.9b) demonstrated the ability to mitigate the LCO noise by implementing a "freeze mode" on the fine-tuning loop when the settled output value was achieved. An added benefit of this freeze mode was that the power losses due to normally operating support circuitry were negligible when frozen further enhancing the regulator current efficiency [40].

The 2020 work by Ma *et al.* [41] presents improvements to the multi-loop DLDO by enhancing drive capabilities with an NMOS pass device array and an active NAND-gate-based analog path (NAP) assist loop, shown in Figure 2.10. The NMOS pass devices are inherently snappier to respond to dynamic loading conditions than PMOS pass devices since the carrier mobility $\mu_n > \mu_p$ in nearly all operating conditions for all CMOS process technologies. Additional benefits include wide-range stability due to dynamic poles less dependent on the output resistance of the pass device. The reduced output impedance of the NMOS pass devices and control schemes further reduce the effects of LCO. The NMOS pass devices along with the NAP assist loop also increase the PSR performance from negligible to 25 dB with a corner frequency ~ 1 kHz. However, to fully realize the benefits of the NMOS pass device, a $2 \times V_{DD}$ charge pump boosted voltage domain was required for the pass device gate driving stage [41].

With the growth in demand for IoT capable SoCs, event-driven sensing with on-demand voltage regulation has become more and more necessary for ultra-low power systems.



(a)



(b)

Figure 2.9: Multi-loop DLDO implementations (a) dual-loop with course-fine-tuning and burst-mode operation [39] (b) tri-loop with course-fine-tuning and analog-assist [40]

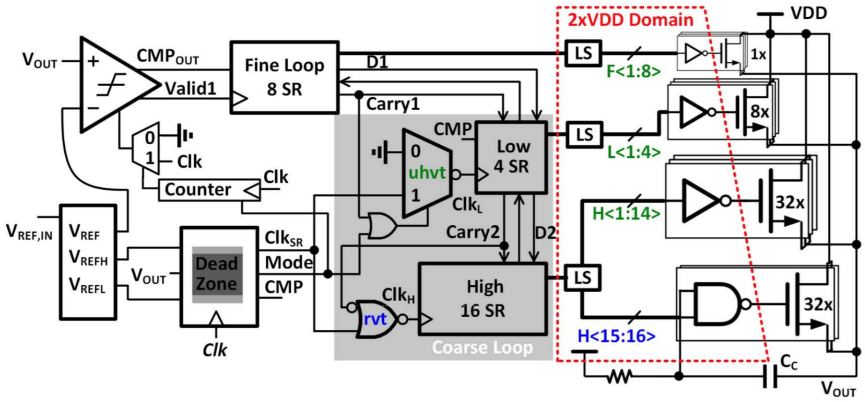


Figure 2.10: Multi-loop DLDO with NMOS pass device arrays and NAND-gate-based analog paths (NAPs) assist loop [41]

Targeting sub-1 µA quiescent current operation has brought LDO design back into the realm of low-power analog-centric or hybrid approaches. The oscillator-based LDOs, such as the 2021 current-controlled oscillator (CCO) by Zhao *et al.* [42] shown in Figure 2.11, have shown considerable advantages for high current efficiencies. The CCO-based LDO uses a fully-differential loop to control the oscillators, the oscillator outputs are subtracted from each other using a time-to-frequency domain comparator, then the difference is used to dictate a continuous charging or discharging the gate of the pass devices. The speed of this approach is much faster than DLDO alternatives with a much lower quiescent current, minimum $I_Q = 310\,\text{nA}$. The complexity of this regulator demonstrates the largest active area compared to all contemporary state-of-the-art LDOs evaluated despite being implemented in 65-nm technology.

Furthering the capabilities of sub-1 µA quiescent current LDOs is the more recent 2021 work presented by Han and Lee [43] in Figure 2.12. This ALDO achieved the greatest traditional FOM of all state-of-the-art LDOs evaluated (summarized in Table 2.2). This FOM success is mainly attributed to the absence of large capacitances within the circuit. The active capacitor methodology presented is a transient suppression technique that senses dynamic load transitions and pushes or pulls current to compensate for the load step. The behavior of the active capacitor support circuit is very similar to a Class B amplifier, that tends to settle in a dead-zone steady-state where the devices are in cutoff or near cutoff. The control loop during steady-state condition is extremely efficient, with an $I_Q = 340\,\text{nA}$ and implemented in a standard 180-nm CMOS process while occupying an active area of $0.04\,\text{mm}^2$ (half the area of the CCO-based 65-nm LDO presented by Zhao *et al.* [42]). The limitation of this LDO is the minimum load current necessary to maintain stability. With a load capacitance of 600 pF and driving 100 µA, a dynamic pole shifts to a frequency below the system's unity gain frequency and thus lowering the phase margin to 25° [43]. If this dynamic pole were to move much lower, the amplifier would likely become unstable and oscillate.

The summary of state-of-the-art fine-grain LDO performance metrics is given in Table 2.2. Initial observations of this data should conclude that the unavailable settling time and PSR metrics of the non-ALDO circuits were not notable enough to mention in the published

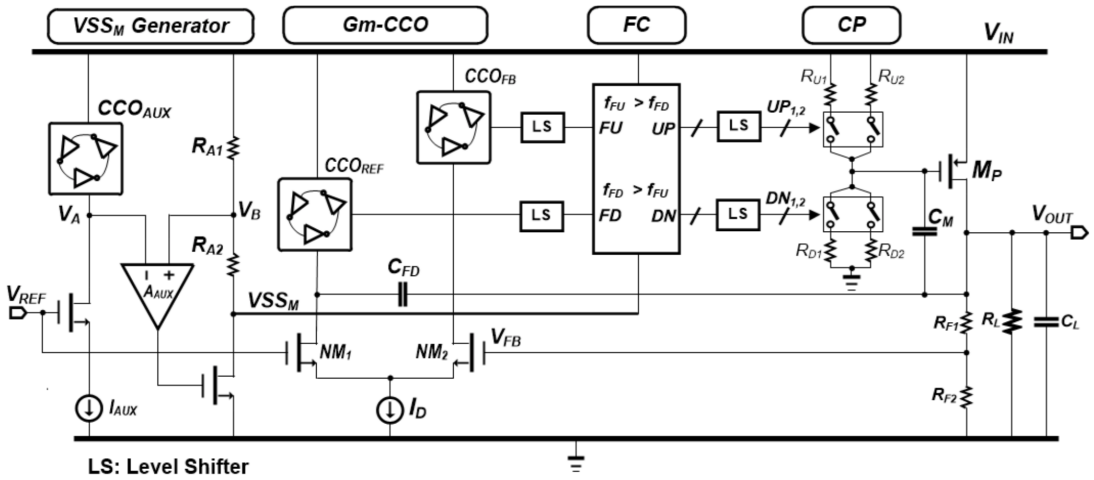


Figure 2.11: Time-to-Frequency domain CCO-based LDO [42]

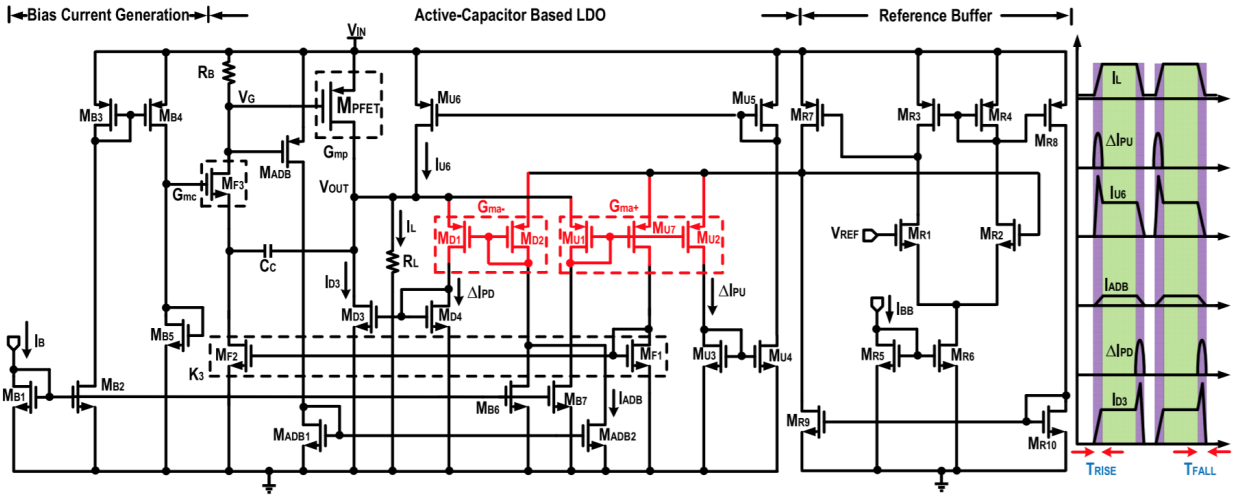


Figure 2.12: Active capacitor ALDO [43]

Table 2.2: State-of-the-Art Fine-Grain LDO Performance Metrics

Parameters	**Unit**	**Huang *et al.*** [39]	**Huang *et al.*** [40]	**Ma *et al.*** [41]	**Zhao *et al.*** [42]	**Han and Lee** [43]
Year		2016	2018	2020	2021	2021
Technology	[nm]	65	65	28	65	180
Control		DLDO w/ Coarse-Fine-Tuning and Burst-Mode	Tri-Loop DLDO w/ Analog Assist	DLDO w/ NAND-based Analog Assist	Current-Controlled Oscillator	Active Capacitor
$\mathbf{V_{IN}}$	[V]	0.6-1.1	0.5-1	0.4-0.55	0.5-1.2	1.2-1.4
$\mathbf{V_{OUT}}$	[V]	0.4-1	0.45-0.95	0.35-0.5	0.45-1.15	1.0-1.2
$\mathbf{I_{OUT}}$	[mA]	100	10	40	50	80
$\mathbf{I_Q}$	[µA]	82	3.2	0.85	0.31-0.5	0.34
$\mathbf{V_{DO}}$	[mV]	100	50	50	50	200
$\mathbf{C_{TOTAL}}$	[pF]	1000	100	59	15	3
$\mathbf{\Delta t_{edge}}$	[ns]	20	1	0.1	15	100
$\mathbf{\Delta V_{OUT}}$	[mV]	55	105	113	150	120
$\mathbf{T_{SETTLE}}$	[ns]	700			300	110
PSR at 100 kHz	[dB]			~ 2		34
$\mathbf{FOM_1}$ *	[fs]	430	230	26	3	0.02
$\mathbf{FOM_2}$ †	[V]	0.902	0.0336	0.00024	0.0225	0.051
Active Area	[mm^2]	0.01	0.034	0.0134	0.118	0.04

$$* \; FOM_1 = \left(\frac{C_{TOTAL}\cdot\Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right) \text{ [14]} \qquad \dagger \; FOM_2 = \left(\frac{\Delta t_{edge}}{1\text{ ps}}\right)\left(\frac{\Delta V_{OUT}\cdot I_Q}{I_{O,MAX}}\right) \text{ [15]}$$

works. This is a statement of how lagging these performances are to ALDOs and how this has become a generally accepted flaw of the topologies. It should also be noted that the voltage scaling capabilities of the DLDOs and CCO-based LDO far exceed the ability of the ALDO presented by [43] to operate at reduced voltages; however, some performance metrics are limited by the process technology used. Thus, it could be unfair to attempt an *apples-to-apples* comparison in a produce market filled with *oranges* and *bananas*. The larger trends can be deducted from this table showing a direction towards lower quiescent currents and generally larger output currents; but also, this demonstrates the inability for a single LDO to fully bridge the gap between ALDO and DLDO and span the desirable qualities that these separate approaches uniquely offer.

2.2 Ring Amplifiers in Literature

It has been demonstrated that leading analog design engineers have utilized techniques such as calibration, gain-enhancement, in addition to output-swing enhancement, to address some of the many design challenges associated with analog scaling [4, 5]. But the underlying issue continues to exist that *contemporary analog design engineers must repeatedly address, readdress, and further optimize any techniques for each step deeper into nanoscale processes.* Hershberg *et al.* [9] responded to this burdensome cycle by introducing **The Ring Amplifier**, an inherently scalable, rail-to-rail analog amplifier for use in mixed signal circuits. This topology has generated a devoted following of designers and academics, specifically in the application space of Nyquist-rate Analog to Digital Converters (ADCs); however, the ringamp has recently emerged in other applications benefiting from the built-in functionality of Sample and Hold (S/H) or Track and Hold Amplifier (THA) stemming from its switched-capacitor (SC) architecture [10].

The Ring Amplifier or ringamp is a general adaptation from the classic ring oscillator [9]. Shown in Figure 2.13, the basic ring oscillator is composed of an odd number of cascaded inverters with an applied feedback loop leading to an a-stable oscillation. The frequency of oscillation (f_{osc}) is dictated by the number of stages (n) and the propagation delay of each

stage (t_d) given in Equation (2.4) [44, 45].

$$f_{osc} = \frac{1}{n \cdot t_d} \tag{2.4}$$

Considering the linear relationship of f_{osc} to t_d for ring oscillators, foundries place ring oscillators on nearly every wafer of nearly every process technology to characterize gate delay within a given process; in addition to, simply verifying a successful wafer fabrication [9]. This application indicates the most appealing quality of the ring oscillator for modification and adaptation: ***complete and inherent scalablity.***

2.2.1 Ring Amplifier Behavior

The general structure of the Ring Amplifier is also that of the Multiplying Digital-to-Analog Converter (MDAC) structure, shown in shown in Figure 2.14a [9]. The ringamp MDAC builds upon a three-inverter ring oscillator but splits the signal into two independent paths to drive complementary output devices M_{CP} and M_{CN}. Within these independent paths, embedded offset voltages V_{OS} create a range of values at which neither output devices should conduct, a "dead-zone (V_{DZ})." The behavior of the ringamp within the dead-zone can be described as Class-B operation, without the dead-zone the ringamp performs as a Class-AB push-pull amplifier. This behavior is a significant oversimplification though, with the implementation of negative feedback, the ringamp is still qualitatively a ring oscillator. Dominant pole compensation in coordination with sizing the dead-zone are the main tools to maintaining stable or, at the least, quasi-stable operation. If stability is achieved, the ringamp's settling response to input can be separated into three distinct stages: **Initial Ramping**, **Stabilization**, and the final settled **Stead-State**. The waveforms in Figure 2.14c demonstrate the settling of a MDAC circuit like that shown in Figure 2.14a, with an embedded dead-zone biasing the amplifier at the edge of stable operation [4].

Initial Ramping: At the initiation of the ramping or slew-charging stage (0 ns to 2 ns in Figure 2.14c), the circuit behaves as the conceptual model shown in Figure 2.14b. Depending on the input value (V_{IN}), either the high-side device (M_{CP}) or low-side device (M_{CN}) will

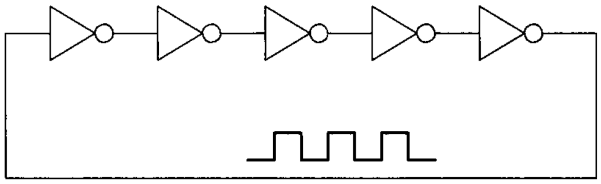


Figure 2.13: Basic five-inverter ring oscillator [44]

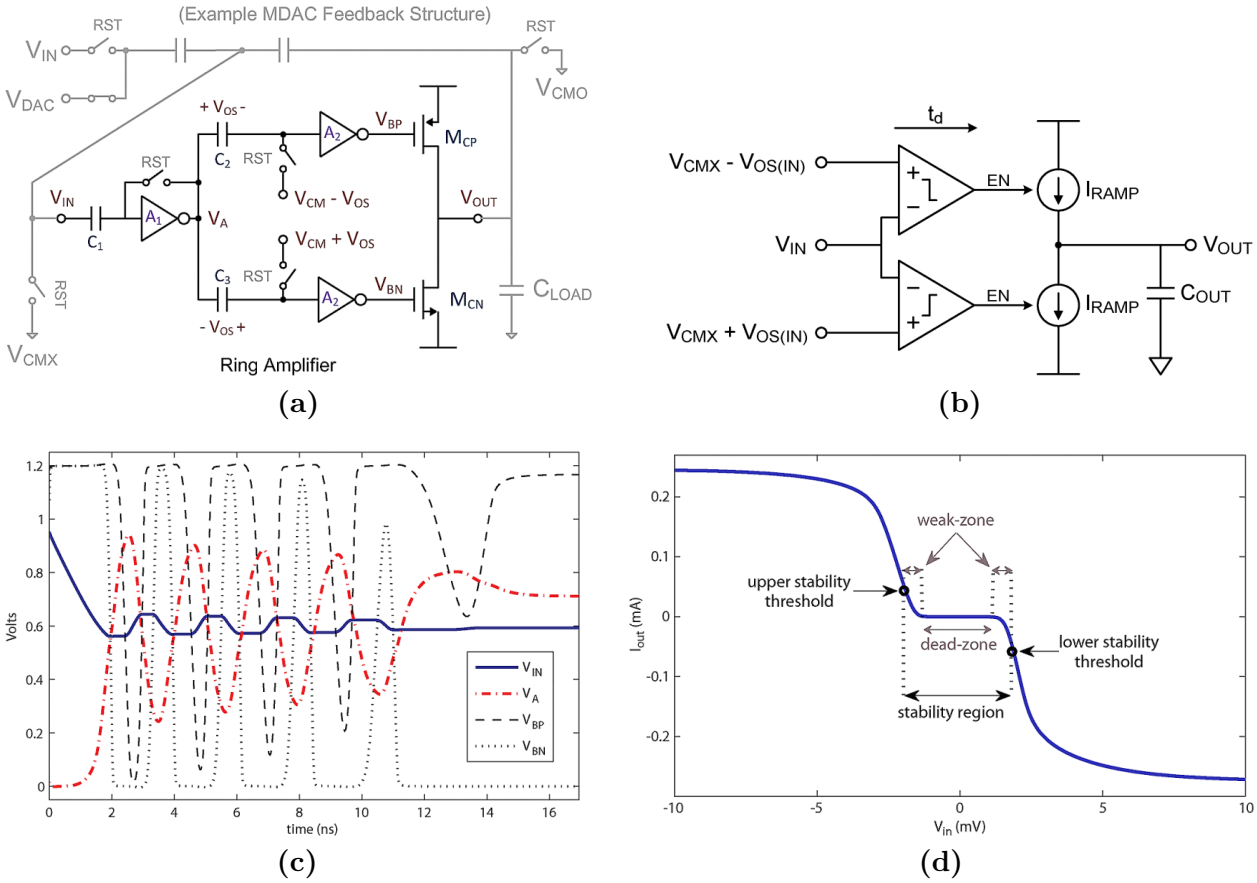


Figure 2.14: (a) Ringamp switched-capacitor MDAC structure and (b) conceptual model of slew-charging operation with (c) corresponding output settling waveforms [4] and (d) DC sweep of V_{IN} vs. I_{OUT} [9]

conduct. The conducting device will operate as a fully-biased current source (I_{RAMP}) to charge the output load capacitor (C_{OUT}). The end of this stage occurs when the threshold of the comparator is crossed; thus, turning off the current source. This transition is not instantaneous, though. Due to delay in the circuit (t_d), I_{RAMP} will continue to conduct and could lead to an overshoot or undershoot of the target voltage across C_{OUT}. The difference in overshoot or undershoot voltage across C_{OUT} to the final settled value can be defined as ΔV_{OUT} in Equation (2.5) [4].

$$\Delta V_{OUT} = \frac{t_d \cdot I_{RAMP}}{C_{OUT}} \tag{2.5}$$

Stabilization: Once the initial ramping stage concludes, the circuit begins to oscillate around the final settled value within the dead-zone region. This stage of operation occurs from 2 ns to 14 ns in Figure 2.14c. The settling time or number of oscillations of this stage is dependent on the size of V_{DZ}. For example, the MDAC retains a-stable qualities of the original ring oscillator if the dead-zone set to small $V_{DZ} = 0\,\text{V}$ and more quickly stabilizes as the size of V_{DZ} is increased [9]. The inverse proportionality of V_{DZ} to settling time suggests the crux of design trade-offs for the ringamp: ***accuracy vs. speed vs. power***. When designing a ring amplifier, one of these qualities cannot be optimized without sacrificing the performance within the other two areas. To decrease settling time by increasing speed: the designer may either increase V_{DZ}, resulting in lower amplifier accuracy; or increase the initial current ramp rate, that results in more significant power losses [4].

Steady-State: The steady-state condition of the ringamp is achieved when both output transistors M_{CP} and M_{CN} enter the cutoff region of MOSFET operation and the output signal V_{OUT} settles within the dead-zone. This occurs by 15 ns in Figure 2.14c. Shown in Figure 2.14d, a "weak-zone" may exist depending on quasi-stable states surrounding the dead-zone where one of the output devices stabilize outside the cutoff region of operation and continue to conduct current [9]. A weak-zone settling can be avoided by carefully designing the size of the dead-zone, adjusted the ratios of the inverter devices to achieve proper matching, and implementing AZ techniques to compensate for bias drift during operation.

2.2.2 Ring Amplifiers for Data Conversion

In a survey of currently published instances of the Ring Amplifier, the field is dominated by Analog-to-Digital Converter (ADC) applications, largely because the ADC is at the forefront of state-of-the-art analog design. Data converters are the primary bridge between the analog, continuous-time world in which we exist and the digital information on which we depend. As with voltage regulation, it is desirable to have these circuits fabricated on the same die as their digital counterparts for a fully realized SoC [5]. As has been discussed in previous sections, digital circuits have enjoyed the benefits of process node scaling such has higher f_T and lower C_G; therefore, analog sub-circuits of much larger systems are being forced to adapt for implementation within smaller process node sizes. Due to the excitement surrounding the ringamp promoted by Hershberg *et al.* [9], these amplifiers have found a niche within the application space of state-of-the-art ADCs, where scalability is almost necessary for the next generation of integration. Some level of knowledge for general ADC topologies, behavior, and terminology might be necessary for a more comprehensive understanding of this section; therefore, a short introduction to Analog-to-Digital Converters is provided in Appendix A.

The earliest two ring amplifier examples were presented by Hershberg *et al.* [9] in 2012 and consisted of a 10.5 b pipelined ADC and a 15 b split-CLS pipelined ADC. The example 15 b ADC incorporated the ringamp within a switched-capacitor MDAC feedback network previously shown in Figure 2.14a, also featuring the gain-enhancement technique split-CLS (split correlated level shifting). Correlated level shifting (CLS) was originally proposed by Gregoire and Moon [46] as a technique to address the reduced intrinsic gain ($g_m r_o$) inherent to the shorter channel lengths of smaller process node sizes. The split-CLS technique was then introduced by Hershberg *et al.* [47] to extend the benefits of CLS techniques to high-resolution Nyquist-rate data converters.

As demonstrated by the phase waveforms for the CLS circuit in Section 2.2.2, the input is sampled during the phase Φ_S before the amplifier switches to amplification mode during Φ_A. While Φ_A is active, the CLS begins two sub-phases: estimation (Φ_{EST}) and level shifting (Φ_{CLS}). For Φ_{EST}, the estimated output value is sampled by C_{CLS}, based on the amplifier's voltage reference or common-mode voltage. In the final sub-phase Φ_{CLS}, the capacitor C_{CLS}

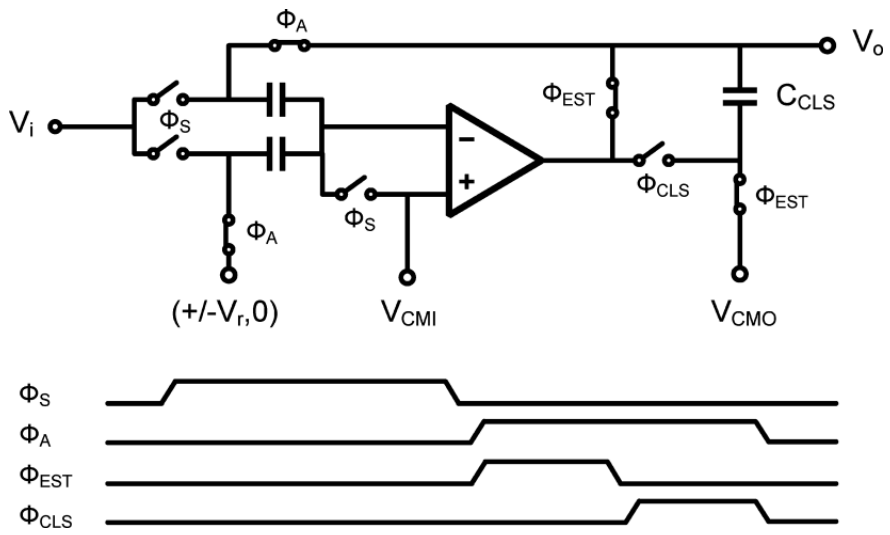


Figure 2.15: Switched-capacitor correlated level shifting (CLS) circuit [47]

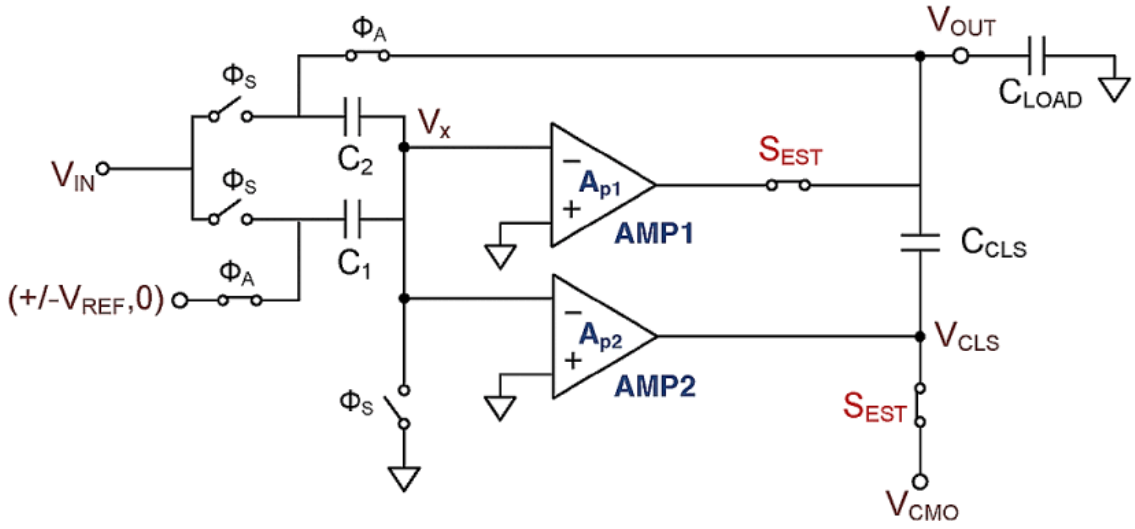


Figure 2.16: The split-CLS MDAC structure [9]

is placed between the MDAC's output and the amplifier's output, level shifting the amplifier output to the common-mode voltage (V_{CMO}). In this final configuration, the amplifier must only compensate for the error from the estimated output value; thus, limiting the amplifier finite gain error. The effective gain (A_{EFF}) of the CLS MDAC can be described by Equation (2.6) [47].

$$A_{EFF} \propto A_{EST} \cdot A_{CLS} \tag{2.6}$$

As noted by Hershberg *et al.* [47], the gains A_{EST} and A_{CLS} are not required to be the same, and the duration of the sub-phases Φ_{EST} and Φ_{CLS} may also be separately adjusted for amplifier performance. These qualities illustrate a distinct independence of operation during the amplifying phase Φ_A ; thus, the MDAC performance could be maximized by splitting the estimation and level shifting duties between two unique amplifiers. These unique amplifiers could then be further optimized for their own specific roles [47]. An example circuit of the split-CLS MDAC is shown in Section 2.2.2, where the effective gain can now be described by Equation (2.7) [9].

$$A_{EFF} = \psi \cdot A_{p1} \cdot A_{p2} \tag{2.7}$$

where ψ is given in equation (2.8) [9].

$$\psi = \frac{C_{CLS}}{C_{CLS} + C_{LOAD} + \frac{C_1 \cdot C_2}{C_1 + C_2}} \cdot \left(\frac{C_2}{C_1 + C_2}\right)^2 \tag{2.8}$$

In this configuration, AMP1 must be capable of delivering a large initial current ramp to C_{LOAD} during the Φ_{EST} sub-phase, an ideal application for the high-slewing ringamp. The role of AMP2 is simply to process the error from the initial estimate; therefore, a simple amplifier capable of only small output swings is necessary [47]. A single stage telescopic amplifier was selected for this role as it provided superior gain and bandwidth within the imposed design power budget [9].

The 2017 circuit in Figure 2.17 by Leuenberger *et al.* [48] builds upon that of Hershberg *et al.* [9] by replacing the capacitor embedded dead-zone with current-starved inverters (CSI) operating as CMOS triode resistors. The main benefits of this ringamp topology include the reduction of die area due to the removal of bulky capacitors and enabling a dynamically

controlled dead-zone for both coarse and fine amplification from a single error amplifier. Additionally, the sizing of the current-starving devices inherently controls a minimum dead-zone that can be optimized to maintain control for worst case supply voltages and ensure an immunity to instability across all operating conditions [48].

The first four-stage ringamp with a proposed improvement to an auto-zeroing technique was presented by Lim and Flynn [49] in 2017. By leveraging a degree positive feedback in the common-mode feedback (CMFB) loop, the addition of the 4th stage defeats some of the trade-off for gain and speed. A major design challenge is that if the positive feedback is not managed, the amplifier could become unstable and latch. The predisposition to instability is magnified by additional feedback loops generated from traditional auto-zeroing techniques.

In general, auto-zeroing (AZ) is a switched-capacitor technique to reduce both noise and DC offset contaminants from a process signal. In an AZ scheme, any undesirable noise or DC offset voltage is sampled, and the instantaneous value of this sample is subtracted from either the input or the output of the amplifier, resetting the applied node to some zero value, common-mode voltage, or reference value. The effects of AZ techniques are limited to narrow-band low-frequency random noise such as flicker noise ($1/f$) or DC offsets; thus, AZ essentially acts as continuous time high-pass filter. In classic examples of AZ, the main trade-off is an overall increased noise floor due to the aliasing of wide-band noise generated during switched-capacitor sampling [50].

The modified AZ technique presented by [49] is shown in Figure 2.18b along with the phase timing diagram. This AZ topology adds an auxiliary second stage that allows the AZ to be completed through negative feedback rather than CMFB; hence, preventing AZ contributions to common-mode positive feedback latching. Additionally, by avoiding AZ implementation at the first stage, the wide-band noise associated with AZ techniques would not be as significantly amplified resulting in a lower overall noise floor and higher signal-to-noise ratio (SNR).

Lagos *et al.* [51, 52] presented multiple ringamp enhancement techniques in 2019 that improved linear operation nearing the supply rails, improved stability over a larger bandwidth, and granted greater control of the embedded dead-zone for a fundamental 3-stage ring amplifier. The floating-battery bias structure embedded within the first stage

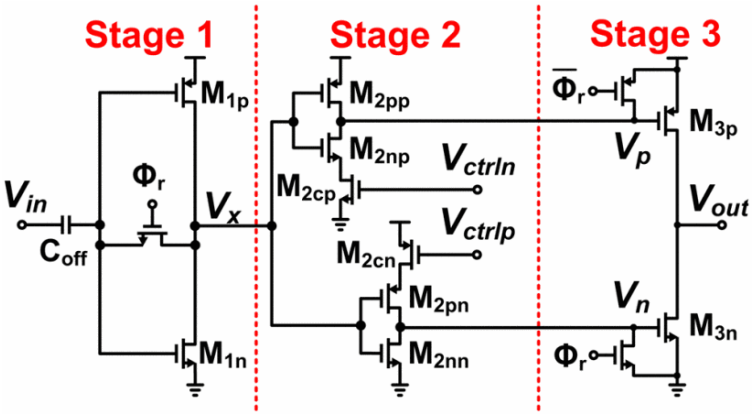
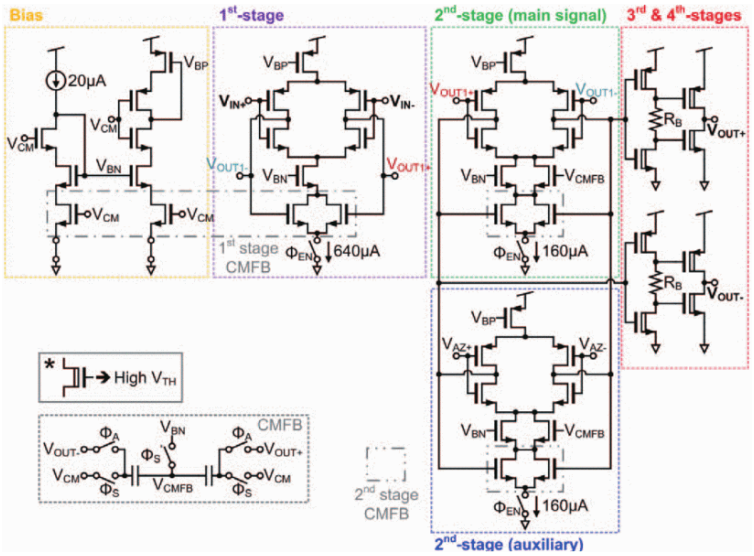
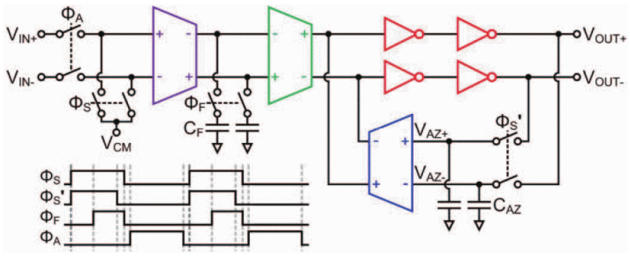


Figure 2.17: Ringamp with CSI embedded dead-zone [48]



(a)



(b)

Figure 2.18: Four-stage fully differential ringamp (a) transistor level and (b) corresponding block model with timing diagram [49]

of the circuit in Figure 2.19, is re-adapted from a Class AB output stage bias technique originally proposed by Monticelli [53]. This "2nd stage bias enhancement" generates an overdrive voltage V_{OD} across the anti-parallel CMOS (AP-CMOS) devices. The V_{OD} is then applied via cross-connection to the second stage inverter, decreasing the output resistance of the second stage devices. This results in two related benefits: (1) the second stage output pole is pushed further beyond the UGF and (2) the second stage gain is reduced, lowering the ringamp's open-loop gain A_{ol} and thus increasing the ringamp's phase margin. The relationship of the pole at the output of the second stage p_2 can be approximated by Equation (2.9), where $r_{o2}^{(P)\vee(N)}$ is the output resistance of the inverter devices and $C_{i3}^{(P)\vee(N)}$ is the input capacitance looking into the third stage devices.

$$p_2 \approx \frac{1}{2\pi \left(r_{o2}^{P} \parallel r_{o2}^{N}\right)\left(C_{i3}^{P} \parallel C_{i3}^{N}\right)} \tag{2.9}$$

A similar AP-CMOS floating battery structure is placed within the second stage, replacing the dead-zone embedding resistor shown previously in Figure 2.18a of the work presented by Lim and Flynn [49]. Under-driving the output stage by increasing the dead-zone, increases the output resistances of the ringamp $\left(r_{o3}^{P} \parallel r_{o3}^{N}\right)$; thus, pulling the output pole p_3 lower and assisting to establish a dominant pole with the load capacitance C_L, defined by Equation (2.10).

$$p_3 = \frac{1}{2\pi \left(r_{o3}^{P} \parallel r_{o3}^{N}\right) C_L} \tag{2.10}$$

Another demonstrated function of the AP-CMOS floating battery bias technique is that driving the gates so that the AP-CMOS structure is in cutoff mode of operation, the entire ringamp stage would be disabled with no current conducting [52]. Thus, in coordination with other control structures and complementary enable logic control signals EN and $\overline{EN}$, the ringamp can be forced into a shutdown or standby mode. This quality makes the ringamp capable of event-driven or on-demand applications requiring a high bandwidth amplifier for only short bursts of activity [54, 55, 56].

Also, within the circuit of Figure 2.19 is a dead-zone degeneration (DZD) linearity enhancement technique. The DZD is applied by placing the devices $M_{N,DZD}$ and $M_{P,DZD}$ in the local feedback paths of the output stage devices. These DZD devices exist normally in

cutoff mode or sub-threshold operation as the ringamp's output voltage V_{OUT} remains close to the steady-state dead-zone value. However, as the output voltage V_{OUT} deviates from the steady-state settled value and swings towards a power rail, the DZD devices begin to steal current from the second stage floating-battery bias structure. This current degeneration dynamically expands the dead-zone bias voltage, further under-driving the output devices and compensating for gain compression error during rail-to-rail operation [51].

2.2.3 Ring Amplifiers for LDOs

Though much work has been done to improve the performance of the Ring Amplifier, these advancements have been largely focused within the data conversion sub-disciplines of microelectronics, *e.g.*, SAR and Pipelined Nyquist-rate ADCs with much smaller representation in $\Delta\Sigma$ oversampling ADCs. The first published art for ringamps outside the confinements of ADC applications was the inverter-based LDO presented by Yang and Mok [11] in 2017. This was followed by the 2019 publication by Xiao *et al.* [12] and 2020 publication by Park *et al.* [13]. All of which have been limited to IEEE-affiliated conference proceedings (no journal or transaction papers) but represent the pool of all known published Ring Amplifiers for LDO applications.

The 65-nm implemented inverter-based amplifier (IBA) and LDO proposed by Yang and Mok [11], shown in Figure 2.20, was intended to offer a low-quiescent current alternative to the DLDOs capable of DVS operation with improved PSR performance. Operation was demonstrated with a supply voltage scaled from 0.2 V to 0.6 V and minimum quiescent current of 410 nA at the lowest supply voltage setting. The PSR was evaluated to be equal to or slightly better than 20 dB up to 20 MHz, that is assumed to be better than most DLDO prior-art since PSR is typically so low it is not reported in publications. However, the response time of this example is lagging and thus the FOMs are less competitive with other state-of-the-art LDOs.

A 180-nm Ringamp-based LDO was presented by Xiao *et al.* [12] from the Oregon State research group of Un-Ku Moon that proposed the original Ring Amplifier circuits with the work of Hershberg *et al.* [9]. This example borrowed dead-zone embedding techniques previously demonstrated by Leuenberger *et al.* [48] with current-starved inverters (CSI) in

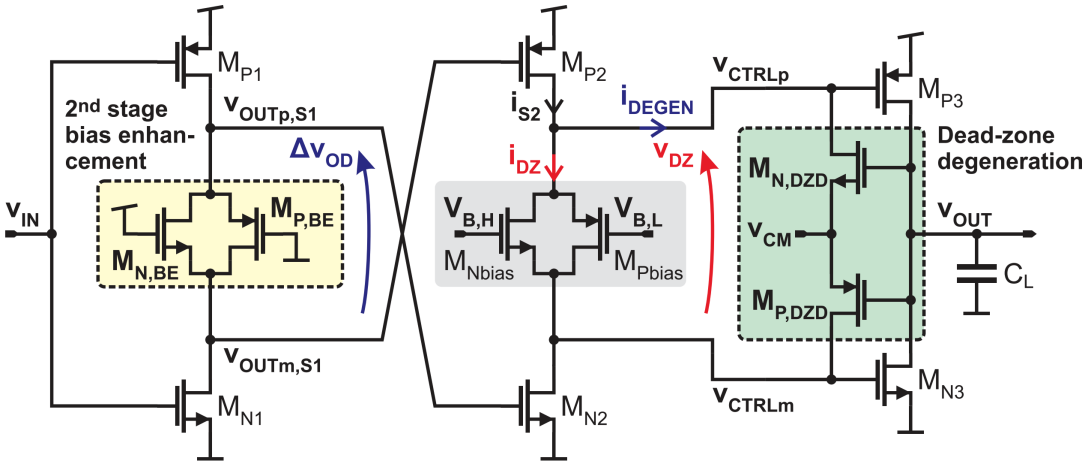


Figure 2.19: Enhanced linearity and bandwidth ringamp with increased dead-zone and bias control [51]

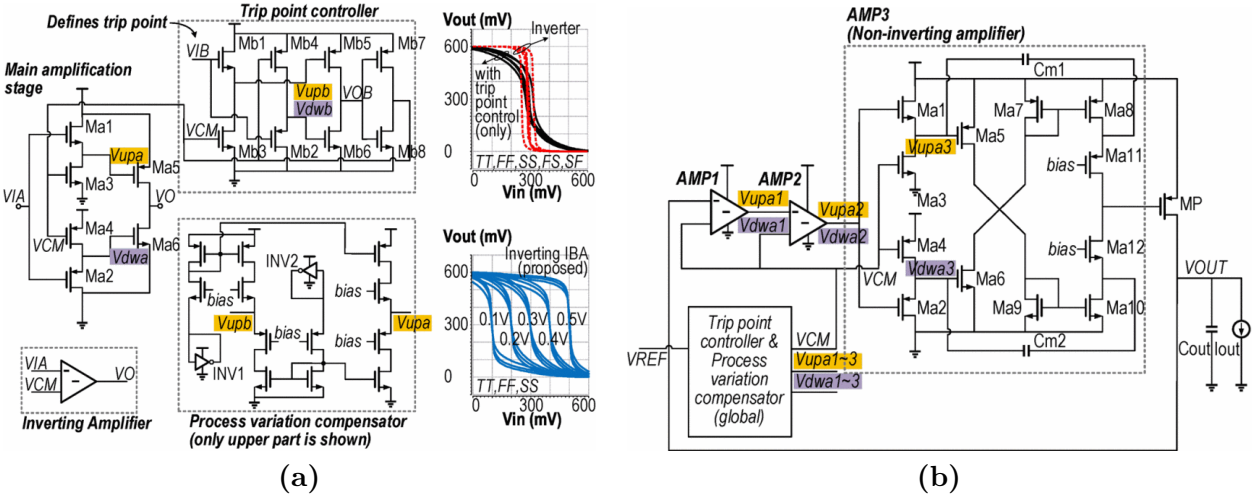


Figure 2.20: Inverter-based LDO: (a) inverter-based amplifier (IBA) and (b) LDO structure with IBAs inserted as ***AMP1*** and ***AMP2*** [11]

the second stage along with replica-based CSI dead-zone regulation techniques proposed by Venkatachala *et al.* [57]. The replica dead-zone biasing scheme shown in Figure 2.21b dynamically adjusts the control voltage of the CSI devices to maintain a constant dead-zone biasing condition in the third stage devices and mitigating any PVT errors [12, 57]. The third stage adaptive dead-zone biasing uses a mirror of the pass device to sense transient loading conditions and dynamically adjusts the dead-zone to a larger or smaller size to accommodating quick settling times and enabling wide-band stability without bulky compensation capacitors.

The most recent Ringamp-based LDO, presented by Park *et al.* [13], implemented in a 40-nm process is another attempt to compete directly with the DVS capable DLDOs. The circuit shown in Figure 2.22, offers two identical error amplifier paths to provide continuous regulation with time-interleaving the alternating AZ reset phases. This work contributes the dead-zone biasing technique by implementing high-voltage-threshold (HVT) and nominal threshold voltage devices to generate offset voltages within an inverter structure. The offset induced dead-zone is then dynamically controlled in response to transient loading allowing for extremely fast settling times in high loading conditions. An additional contribution is a PSR enhancement technique using a replica inverter that tracks the offset voltages, and then subtracts this error from the input of the main inverter with capacitive level shifting during the AZ phase. This LDO delivered the largest load of 400 mA compared to all other state-of-the-art LDOs examined. This work demonstrated an ability to scale with voltage supply from 0.4 V to 1.2 V, but enhanced performance came with a cost for the highest quiescent currents observed up to 1.28 mA.

The performance summary of all known published Ringamps in LDOs is shown in Table 2.3. While the ringamp is qualitatively described as inherently scalable, it is not necessarily apparent that the RLDOs presented follow the same suit. Two of the three demonstrated an ability to voltage scale, but the only metric that successfully separates them from DVS capable DLDOs is the PSR performance. An optimistic interpretation from the RLDO's performance is that there exist pathways to enhance the performance of these mostly-analog systems to compete directly with the DLDOs largely dominating SoC applications. Across these RLDOs and previous Ring Amplifier contributions the tools

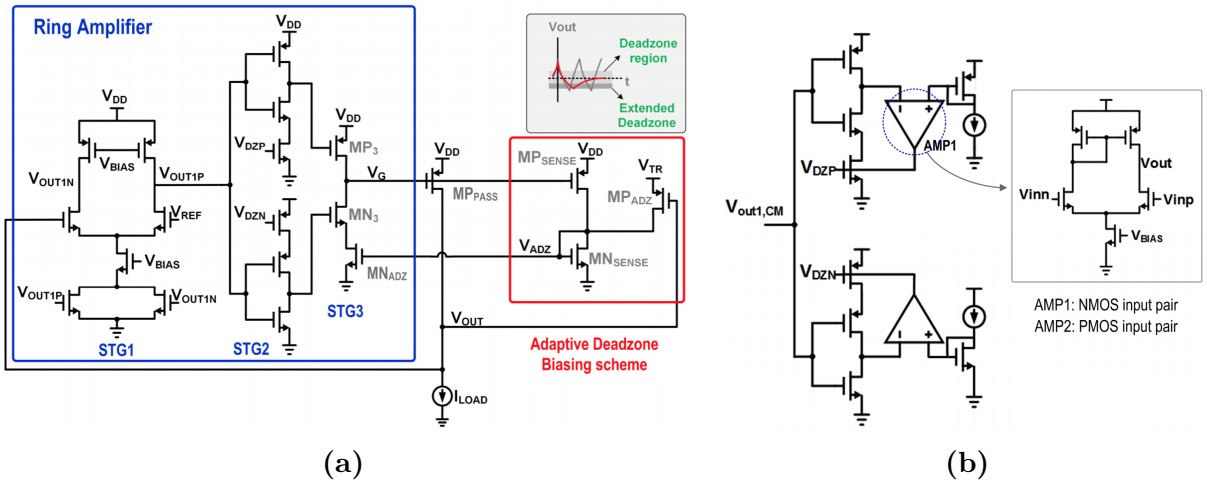


Figure 2.21: Ringamp-based LDO (a) schematic with (b) replica biasing circuit [12]

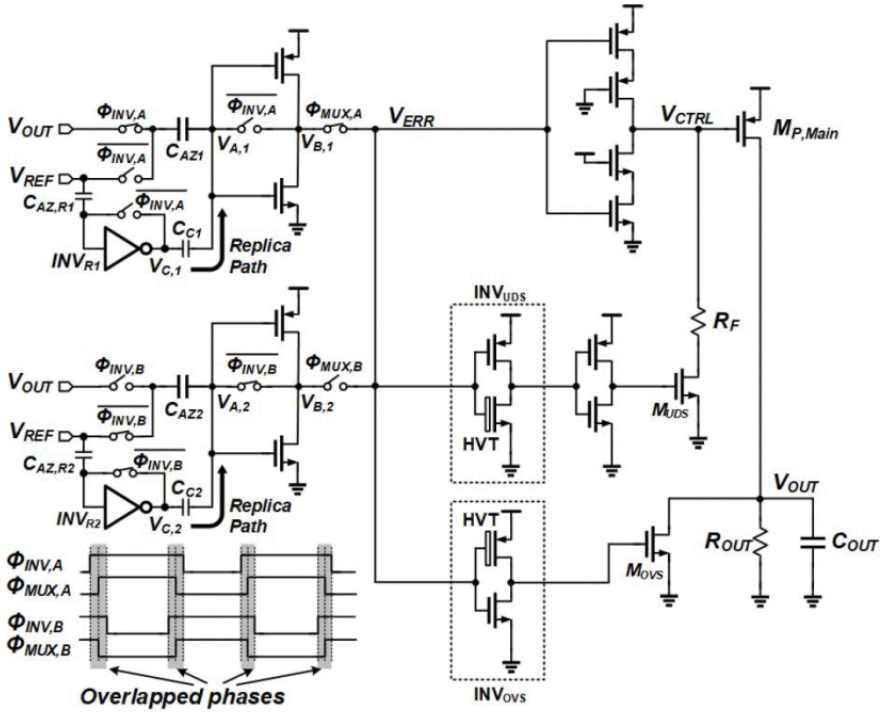


Figure 2.22: AZ interleaving RLDO [13]

and techniques are available that would allow for an improvement to state-of-the-art LDOs. Examples have been shown that demonstrate high slew rates and snappy transient responses, wide-band stability with dead-zone enhancement techniques, negligible quiescent draw with event-driven operation, small core circuit footprint area in its most elemental form, and complete and inherent scalability across nearly all process node technologies. The need for contributions exploiting the Ring Amp in LDO applications is immeasurable. The work thus far has been positive steps but has not yet galvanized the attention this approach deserves; leaving astronomical frontiers for further contributions.

Table 2.3: All Known Published Ringamp LDO Performance Metrics

Parameters	**Unit**	**Yang and Mok [11]**	**Xiao *et al.* [12]**	**Park *et al.* [13]**
Year		2017	2019	2020
Technology	[nm]	65	180	40
$\mathbf{V_{IN}}$	[V]	0.2-0.6	1.08-1.65	0.4-1.2
$\mathbf{V_{OUT}}$	[V]	0.05-0.55	1	0.2-1.18
$\mathbf{I_{OUT}}$	[mA]	0.1-50	40	400
$\mathbf{I_Q}$	[µA]	0.41-32	6.5	4.4-1280
$\mathbf{V_{DO}}$	[mV]	20	90	50
$\mathbf{C_{TOTAL}}$	[pF]	40	50	90
$\mathbf{\Delta t_{edge}}$	[ns]	10,000-150	100	10
$\mathbf{\Delta V_{OUT}}$	[mV]	133.9	46-163	78-45
$\mathbf{T_{SETTLE}}$	[ns]		234-700	500-25
PSR at 1 Hz	[dB]	20	~ 18	~ 30
$\mathbf{FOM_1}$ *	[fs]	228,300-1700	1505-8	28,600-55
$\mathbf{FOM_2}$ †	[V]	0.165	0.748	0.00858
Active Area	[mm^2]	1.379	0.1	0.12

$$* \; FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right) \text{ [14]}$$

$$\dagger \; FOM_2 = \left(\frac{\Delta t_{edge}}{1 \text{ ps}}\right)\left(\frac{\Delta V_{OUT} \cdot I_Q}{I_{O,MAX}}\right) \text{ [15]}$$

Chapter 3

On-Demand Ring Amplifier Design

3.1 A Ring Amplifier Design Guide

This Ring Amplifier Design Guide is intended to provide the future designer with a step-by-step and systematic path from design to implementation for the ringamp topologies shown in Figures 3.1 and 3.2. This is achieved by providing a greater level of design abstraction of the Ring Amplifier implemented in Chapters 4 and 5 so that it can assist in general on-demand amplifier applications where dynamic, high-gain, high-speed, and scalable analog behavior are desirable features.

As shown in previous published design examples by Megawer *et al.* [58], Conrad *et al.* [59], the large-signal dynamic behavior of the Ring Amplifier with limited amount of design control variables requires a more abstract and cyclical design procedure. The design approach of this work enhances the previous design examples by contributing a philosophical foundation that a more significant initial investment of time and effort into the organization and planning towards a ringamp design will lead to much more efficient and rapid design-to-implementation process. A large portion of this pre-design planning has already been completed with the development of the design assistance scripts found in Appendix B with a guide to their usage in Section 3.2. The Section 3.1.1 provides a pre-design procedure that will provide a robust starting point before leading into the systematic design method of Section 3.1.2.

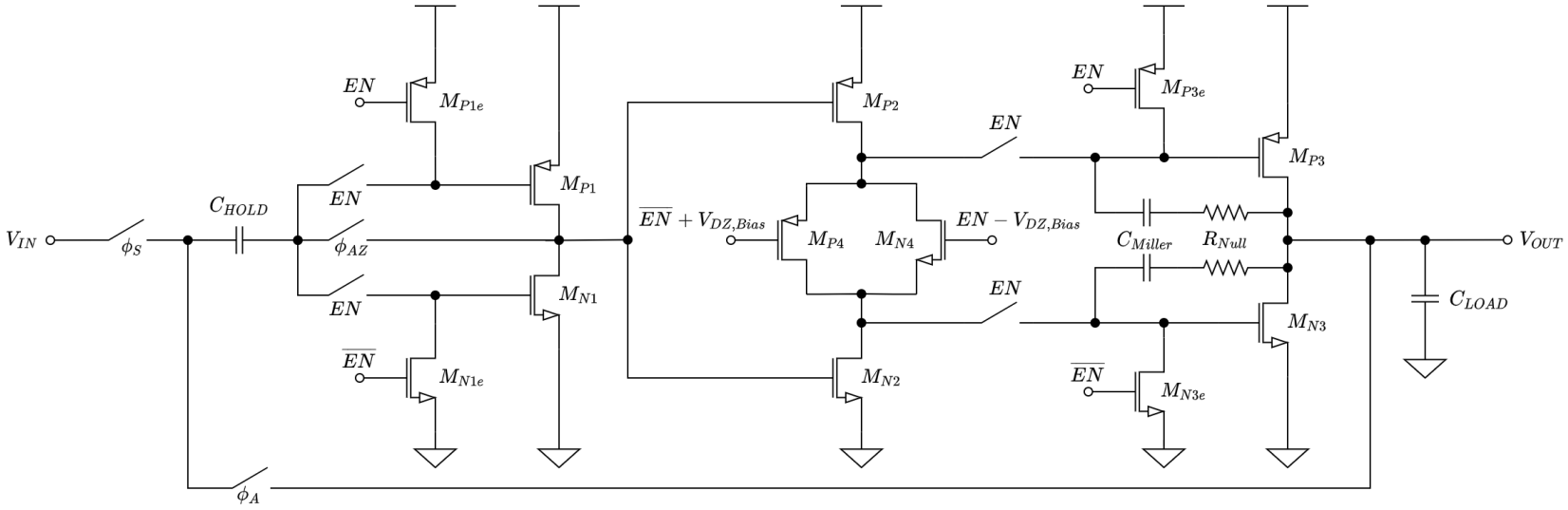


Figure 3.1: On-demand ringamp with under-driven Class B output stage

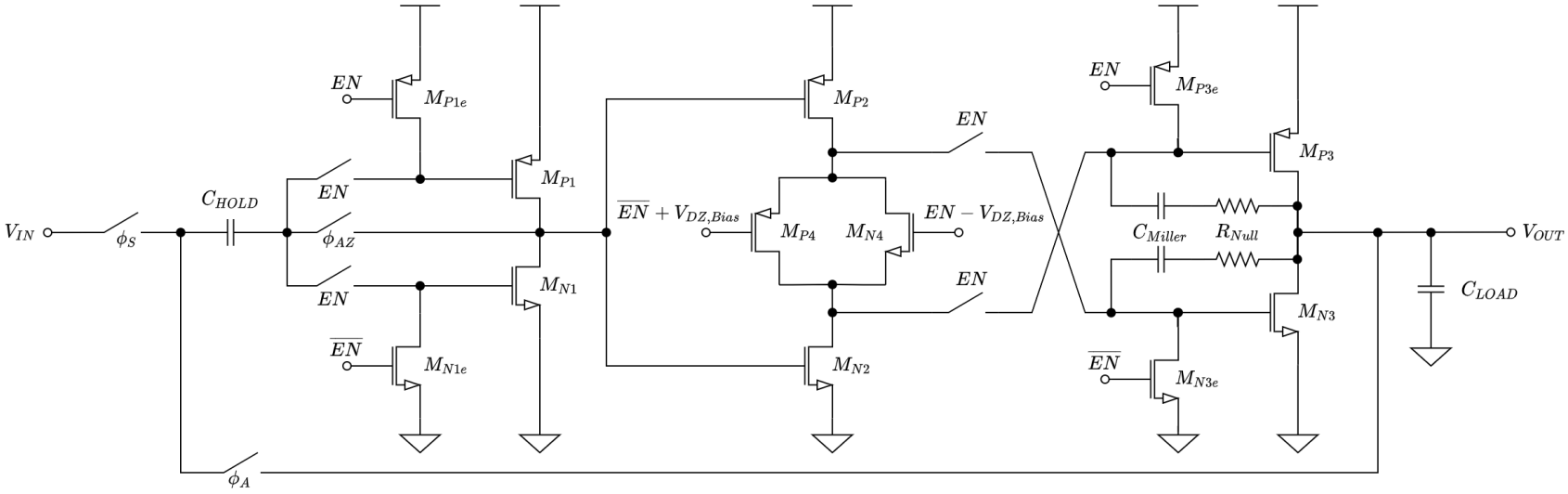


Figure 3.2: On-demand ringamp with over-driven Class AB output stage

3.1.1 Pre-Design Tasks

1. Organize design specifications and requirements
    a. Current budget?
    b. Target gain and bandwidth?
2. Generate IV curves for design assistance scripts
    a. Within the simulation environment, construct a device characterization testbench (like example shown in Figure 3.7)
        i. Use approximately unit size NMOS and PMOS devices
        ii. Verify selected unit sizes are reasonable for the intended PDK
    b. Using a constant V_{GS}, sweep V_{DS}
        i. Increment V_{GS} and reiterate V_{DS} sweeps
        ii. Save data V_{GS}, V_{DS}, and I_D data for each sweep
        iii. Note: higher data resolution will yield more accurate results
    c. Organize data into a `*.xlxs` Excel® spreadsheet
        i. Use Figure 3.5 as a template guide
        ii. Verify separate spreadsheet pages for NMOS and PMOS device data
        iii. Verify file is saved as `IMPORT_ME.xlxs` to use design assistance scripts
3. Implement MATLAB® design assistance scripts (source code in Appendix B)
    a. Input V_{DD}, desired V_M and I_Q to the source code (location shown in Figure 3.6).
    b. Input the values of W_n, W_p and L used for the IV curves to the source code (location shown in Figure 3.8)
    c. Review the results table after executing the design scripts
        i. Verify reasonableness of values
        ii. If necessary, implement any changes and run scripts again
4. Verify the optimum inverter sizing suggestions from the design scripts
    a. Within the simulation environment, construct an inverter characterization testbench (like the example shown in Figure 3.10)
        i. Scale the previously chosen unit sized transistors to conform to suggested results from the design assistance script

ii. Sweep the input voltage from 0 to V_{DD}

iii. Plot V_{OUT} versus V_{IN} (like Figure 3.9)

iv. Verify V_M is located at desired location (default $V_M = {}^{V_{DD}}/_{2}$)

b. If necessary, implement any changes and run scripts again

3.1.2 Design Method

This design guide presents two ringamp topologies for the designer's considerations. The most significant difference between the two options is the configuration of the floating battery offset in the second stage. The configuration shown in Figure 3.1 uses the offset to under-drive the output stage, forcing Class B behavior with a dead-zone like the original ringamp proposed by Hershberg [4]. The second configuration shown in Figure 3.2 alternates second stage output connections on either side of the floating battery to over-drive the output stage. This connection technique forces Class AB behavior, effectively eliminating any dead-zone in the output range. The designer's choice in between these configurations is only to enhance the balance of design trade-offs in a direction benefiting those metrics more desirable towards the final design.

1. Refer to target design specifications and requirements
2. Select an appropriate unit length to balance desired gain, quiescent current, and bandwidth requirements
   a. Maximizing gate length yields:
      i. Increased terminal voltage gain $A_{vt} = g_m r_o$ with higher r_o
      ii. Decreased power consumption with lower I_Q
   b. Minimizing gate length yields:
      i. Decreased $C_G \approx C_{ox} WL$
      ii. Increased bandwidth
      iii. Decreased loop delay
3. Use suggested ${}^{W_p}/_{W_n}$ ratio from design assistance scripts
   a. Verify transition voltage (a.k.a. trip point) V_M is desired auto-zeroing voltage
   b. Tune or micro-optimize width ratios to achieve more accurate V_{AZ}

4. Scale widths of the first stage to balance gain and noise requirements, where increased width yields:
    a. Decreased r_o
    b. Decreased kTR related noise
    c. Decreased terminal voltage gain $A_{vt} = g_m r_o$
5. Scale widths of the second stage to balance gain and speed requirements, where increased width yields:
    a. Decreased terminal voltage gain $A_{vt} = g_m r_o$ with lower r_o
    b. Decreased speed, increased loop delay with higher $C_G \approx C_{ox} WL$
6. Scale width of the third stage to achieve desired slew rate and accuracy
    a. Maximizing the scaled width yields:
        i. Increased initial current I_{RAMP}
        ii. Increased slew rate $SR = {}^{(I_{RAMP} t_{delay})}/_{C_{LOAD}}$
    b. Minimizing the scaled width yields:
        i. Decreased initial current I_{RAMP}
        ii. Decreased overshoot voltage $\Delta V_{OUT} = {}^{(I_{RAMP} \cdot t_{delay})}/_{C_{LOAD}}$
7. Prioritize design specifications, consider desirable offset voltage of floating battery structure
8. Select Class B (Figure 3.1) or Class AB (Figure 3.2) ringamp topology
    a. Class B selection
        i. Increased efficiency
        ii. Increased settling speeds
        iii. Increased stability
        iv. Decreased accuracy
        v. Decreased signal fidelity, linearity (*i.e* distortion)
    b. Class AB selection
        i. Increased accuracy
        ii. Increased sensitivity
        iii. Increased signal fidelity, linearity
        iv. Decreased stability

v. Decreased settling speed

vi. Decreased efficiency

9. Select (if needed) dominant pole compensation technique
   a. Dominant pole with large external output capacitor
      i. Decreased loop delay
      ii. Increased area constraints
   b. Dominant pole with Nested Miller Compensation (NMC)
      i. Increased loop delay
      ii. Decreased area constraints
10. Run transient simulations and observe and revisit previous steps as necessary to achieve the targeted performance

3.1.3 Final Design Considerations

- To increase design optimization speeds after the initial transient simulations have been observed, the decision tree dictating which steps should be readdressed is shown within the summary of this design method of Figure 3.3. This is a systematic design process; therefore, multiple iterations may be necessary to achieve the desired results.
- As with any ringamp design, there exists a limited amount of control variables; therefore, the range of optimization will be bound to the process technology and ringamp topology. For the designer's consideration, the list of major design handles within this guide can be summarized as:
  - Width scaling between stages
  - Length sizing for each stage
  - Offset voltage from second stage floating battery
  - Selection of Class B or AB configuration
  - Dominant pole compensation technique

- A design reference for major peripheral circuitry such as switches and digital buffers as well as suggestions for implementing the switched-capacitor timing controls can be found within the body of this dissertation in Section 4.2.2.[1]
- The designer could consider cascading additional ringamp stages, still maintaining an odd integer value of total stages. The disadvantage of this approach is an increase in loop delay; thus, consequentially a reduction in bandwidth and slew rate. The target advantage of this feature is an increase in available loop gain. There is potential for this approach in lower bandwidth analog applications (*e.g.*, active filters and sensor amplifiers), where the structures shown previously in figures 3.1 and 3.2 are unable to meet the desired gain specifications. Since most Ring Amplifier examples in literature are designed for higher speed applications, this approach is relatively uncommon; but, in the spirit of continued exploration of new applications for the Ring Amplifier, this could be a pivotal feature.

3.2 Design Scripts Usage Guide

3.2.1 Optimum Inverter Design Script

The most critical design step of the Ring Amplifier is also the most elemental. A poorly designed inverter can lead to an extremely unsuccessful ringamp implementation. Since the transition voltage or mid-point of the inverter (V_M) is used to establish an auto-zeroing voltage (V_{AZ}), if either high-side PMOS or low-side NMOS device is not fully in saturation at V_M, the gain and performance of the entire system will be asymmetrical. This asymmetry can lead to weighted DC offsets and ultimately a higher level of harmonic distortion. The designer must abandon the colloquial "rule-of-thumb" inverter design guidelines and refocus the PMOS-to-NMOS matching in the device level equations. For this reason, the *Optimum Inverter Design Script* in Appendix B.1 with the *Parameter Extractor Function* in Appendix B.2 should be used as design assistance for the inverters central to the suggested ringamp topologies shown in Figures 3.1 and 3.2.

[1] A standalone version of this design guide will include select portions of such information, but this is limited within the Appendix due to redundancy concerns.

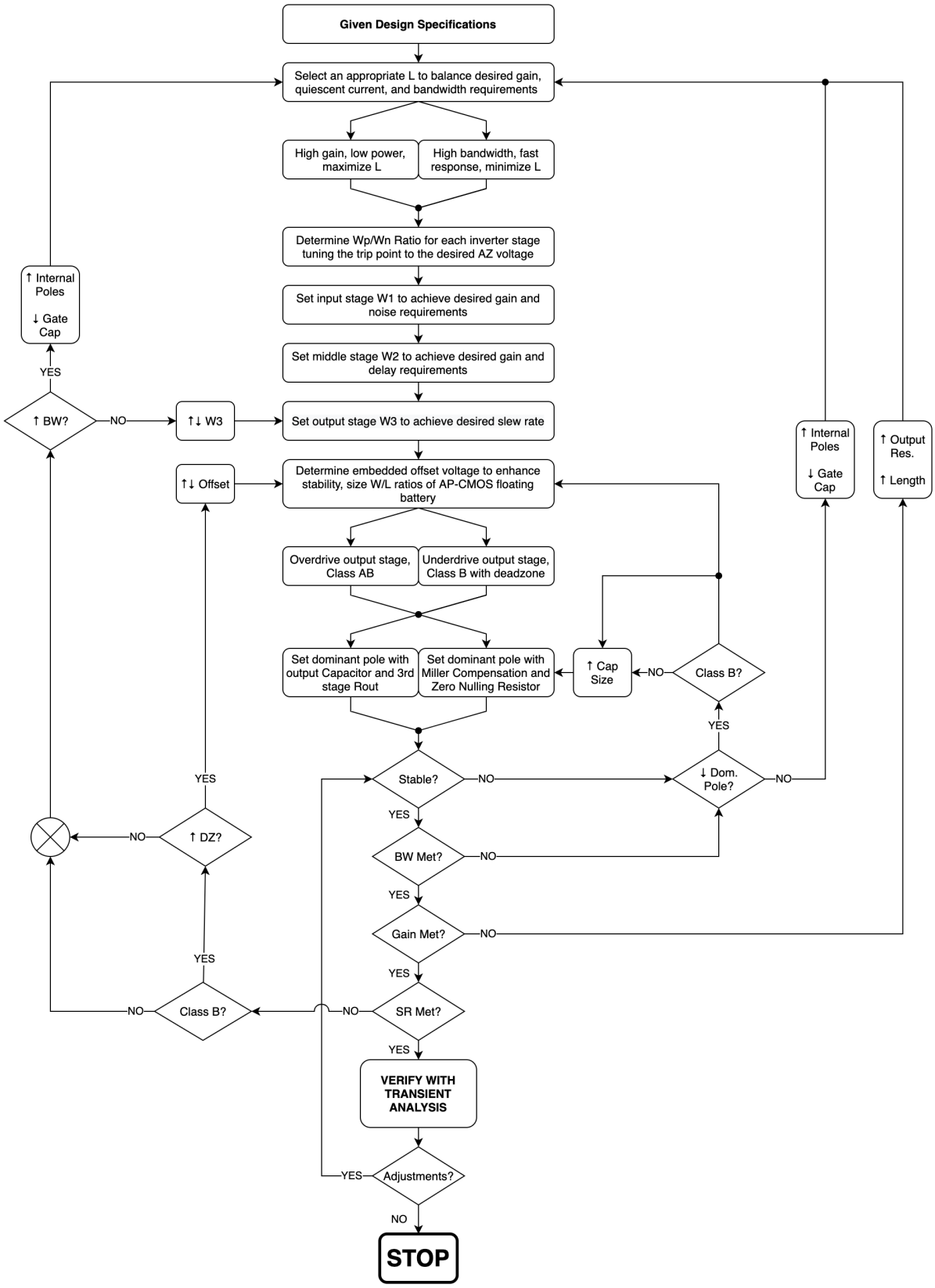


Figure 3.3: Design flowchart for proposed ringamp structure

IV Curves

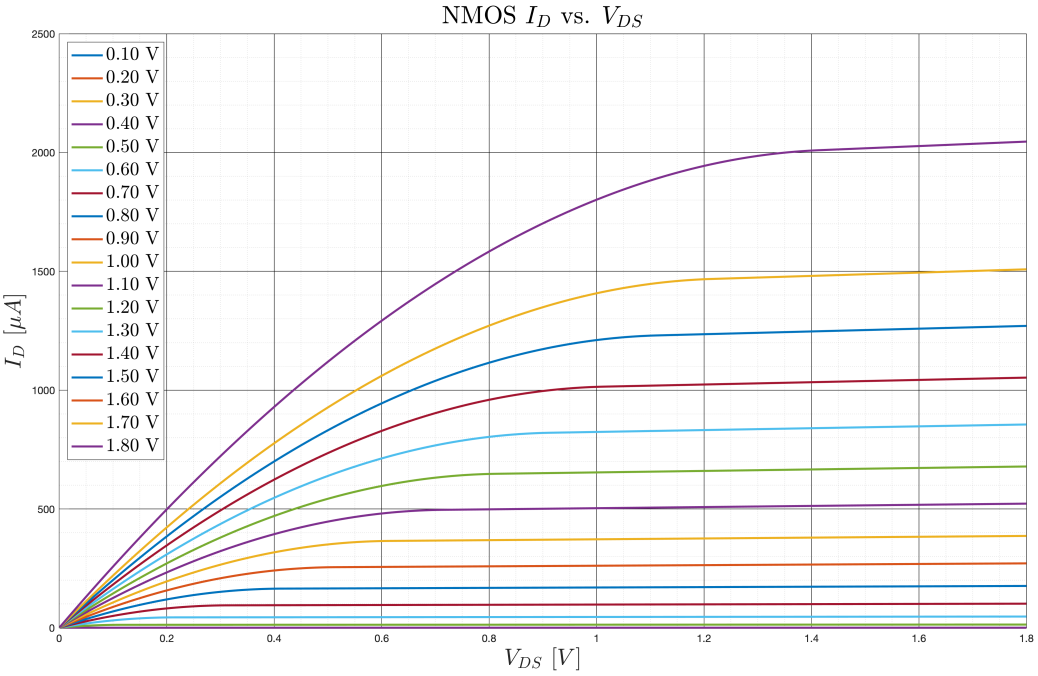
The IV curves are generated by simulating a DC sweep of the drain-to-source voltages V_{DS} for constant values of gate-to-source voltages V_{GS}. This can be achieved using nearly any simulation environment; originally intended for Cadence Spectre®, but an example case is shown for LTspice®.[2] With similar simulation configurations as in the example schematic of Figure 3.7, the IV curves in Figure 3.4 can be generated. It is important to note that more data points (or higher data granularity) should ultimately yield more accurate results with these design assist scripts.

Once the simulations have completed, the xy-data points of the IV curves must be migrated to an Excel® spreadsheet saved with a file name `IMPORT_ME.xlxs`. This spreadsheet must be in the format shown in Figure 3.5 to be read by the *Parameter Extractor Function* without any code modifications. This format consists of a first column of V_{DS} points that are to be consistent across all DC sweeps, a header row with all V_{GS} bias voltages, and columns under the V_{GS} values with their associated I_D points corresponding to the same row V_{DS} voltages within the first column. There will also be two pages in the spreadsheet: one for the NMOS device and second for the PMOS device titled `NMOS` and `PMOS`, respectively. These IV curves are necessary for extracting the best possible approximations for threshold voltage V_{Tn} or V_{Tp}, process transconductance parameter k', Early Voltage V_A, and channel length modulation factor λ. These parameter approximations are necessary for optimizing the inverter sizing to achieve desired design specifications. Further details of the *Parameter Extractor Function* are given in Appendix B.2.

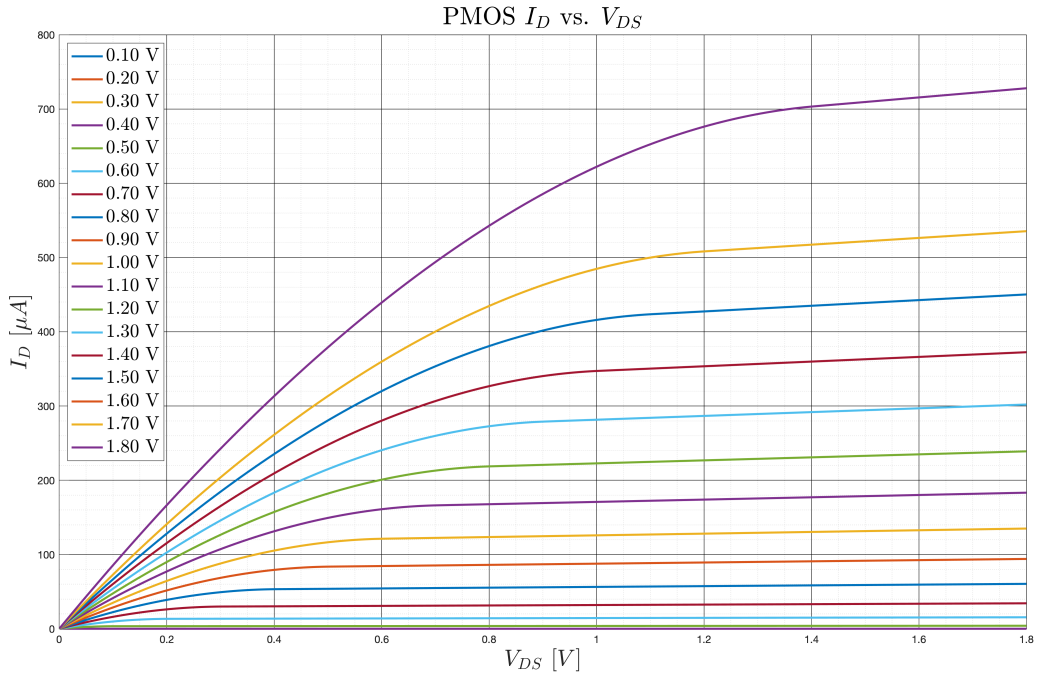
Inverter Script Configuration

The *Optimum Inverter Design Script* (shown fully in Appendix B.1) must be configured by the user for each series of usages. The starting design parameters of supply voltage V_{DD}, desired transition voltage V_M, and inverter quiescent current I_Q occurring when the input gates are DC biased at V_M must be correctly defined within the lines shown in Figure 3.6.

[2] Using LTspice® rather than Spectre® for this simple usage example avoids any possible sharing of intellectual property associated with the PDKs for which these tools were developed



(a)



(b)

Figure 3.4: *IV* curves generated in LTspice® for parameter extraction example, (a) curves for NMOS and (b) curves for PMOS

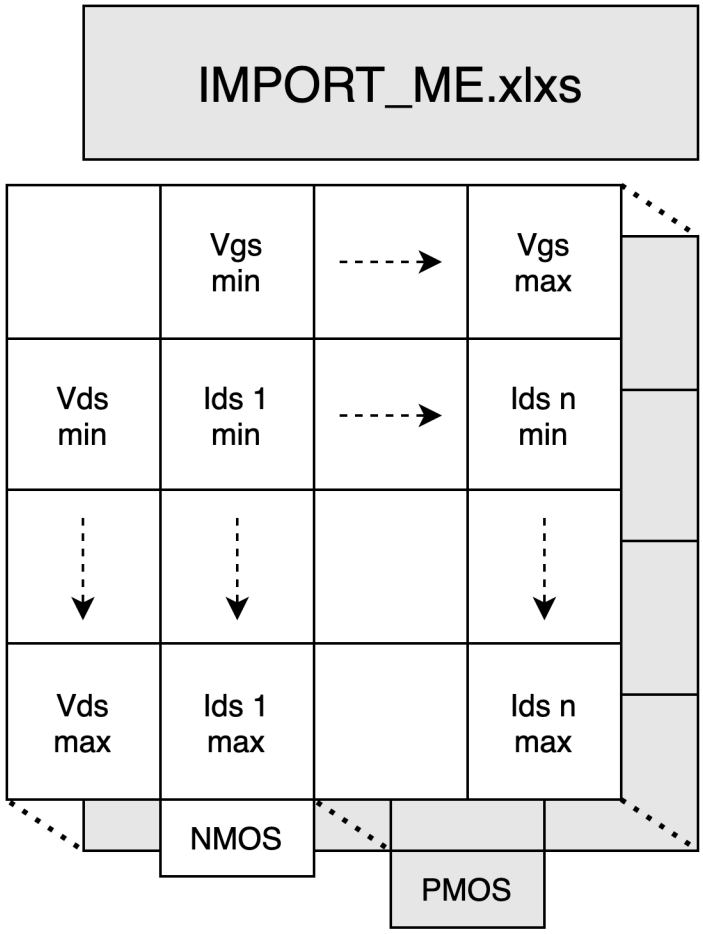
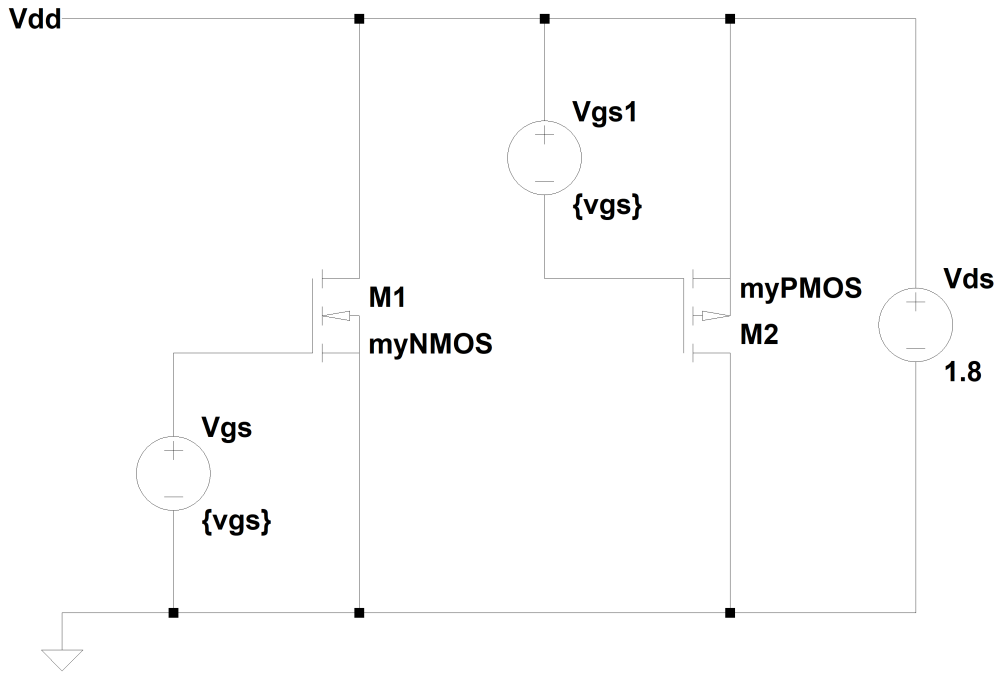


Figure 3.5: Required spreadsheet format for parameter extractor MATLAB® script

```
%%  USER INPUT  %%
%   Design Parameters
Vdd = 1.8;      % DC Supply Voltage
Vm = Vdd/2;     % Transition Voltage
IQ = 150e-6;    % Quiescent Current
```

Figure 3.6: Optimum inverter design script excerpt for user defined design parameters




```
.model myPMOS PMOS(L=1u W=5u VTO=-0.395 Kp=125u Lambda=0.1 TOX=1e-10)
.model myNMOS NMOS(L=1u W=5u VTO=0.385 Kp=375u Lambda=0.05 TOX=1e-10)

.step param vgs 0 1.8 0.1
.dc Vds 0.001 1.8 .001
```

Figure 3.7: LTspice® testbench example for generating MOSFET *IV* curves

Additional user input must be provided to interpret the processed IV curve spreadsheets. The widths of the NMOS (W_n) and PMOS (W_p), as well as the common gate length (L) for the devices used to generate the simulated IV curves must be correctly defined within the lines shown in Figure 3.8

Optimum Inverter Sizing

The optimum sizing of the inverter is the ratio of widths between the high-side PMOS and low-side NMOS devices. The desired behavior of the inverter is a behavioral line of symmetry at the transition voltage V_M for both input and output voltages [1]. The most accessible mechanism the designer must tune this behavior is the ratio W_P/W_n. This is achieved by balancing the set of I_D equations for both devices at the bias point where $V_{IN} = V_{OUT} = V_M$. The I_D equations for each device are defined by Equations (3.1) and (3.2) [60].

$$I_{Dn} = k'_n \frac{W_n}{L} \frac{(V_{GSn} - V_{Tn})^2}{2\alpha_n} \qquad (3.1) \qquad\qquad I_{Dp} = k'_p \frac{W_p}{L} \frac{(V_{GSp} - V_{Tp})^2}{2\alpha_p} \qquad (3.2)$$

The transition voltage V_M is designed to be $V_M = V_{DD}/2$. Then when the inverter's input is held at V_M, the V_{GS} for both NMOS and PMOS can be defined as V_M. To simplify this general case derivation, the surface potential linearization factor α is approximated to be 1. Equations (3.1) and (3.2) can then be rewritten as in Equations (3.3) and (3.4).

$$I_{Dn} = \frac{k'_n}{2} \frac{W_n}{L} (V_M - V_{Tn})^2 \qquad (3.3) \qquad\qquad I_{Dp} = \frac{k'_p}{2} \frac{W_p}{L} (V_M - V_{Tp})^2 \qquad (3.4)$$

The inverter devices share the same I_D, so the right halves of Equations (3.3) and (3.4) can be organized to follow $I_{Dn} = I_{Dp}$ as in Equation (3.5).

$$\frac{k'_n}{2} \frac{W_n}{L} (V_M - V_{Tn})^2 = \frac{k'_p}{2} \frac{W_p}{L} (V_M - V_{Tp})^2 \qquad (3.5)$$

The ratio of W_P/W_n can then be solved for by eliminating the constant 2 and length L if the NMOS and PMOS share a common gate length. This is shown by Equation (3.6)

$$\frac{W_p}{W_n} = \frac{k'_n}{k'_p} \cdot \left(\frac{V_M - V_{Tn}}{V_M - V_{Tp}} \right)^2 \qquad (3.6)$$

Evaluating the Results

If successfully implemented, the *Optimum Inverter Sizing Script* will print a table to the screen with the both the extracted and calculated values. The resulting values for the example devices of Figure 3.7 are summarized in Table 3.1. The example device characterization testbench is then reconfigured for Figure 3.10 to construct an inverter. Using the results of the design assistance script, the optimum sizing approximations are used to define the parameters within the `.param` spice statement and `.model` configurations to define the devices' geometries. The example inverter's simulated transfer curve is then shown in Figure 3.9 for $V_{DD} = 1.8\,\text{V}$. This simulated transfer curve shows a transition voltage $V_M = 905\,\text{mV}$; thus, demonstrating a very small error contribution from the script-based approximations.

Once arriving upon the results of this design assistance script, the designer could further enhance the inverter behavior with micro-optimizations to achieve any desired level of accuracy for a given application. The benefit of using the *Optimum Inverter Sizing Script* is the time saved to reach that point. This allows for a more effort-efficient and systematic design methodology that should decrease design time, facilitating a faster design-to-implementation workflow.

3.2.2 Parameter Extractor Function

The *Parameter Extractor Function* in Appendix B.2 addresses the need for starting-point parameters for classical MOSFET I_D equations. The typical Process Design Kit (PDK), does not generally provide values for the process transconductance parameter k', carrier mobility μ, or channel length modulation factor λ. These values are not absolutes and not behaviorally accurate for all cases of MOSFET operation; however, these parameters can be useful for ringamp design since the drift into corner cases can be dynamically readjusted for by the auto-zeroing function of the suggested ringamp topologies shown in Figures 3.1 and 3.2.

The parameter extraction uses IV curves generated from any simulation testbench (*e.g.*, either Spectre® or LTspice®). The only criteria is that the data be migrated to the spreadsheet

```
%   USER INPUT values from IV curves
WN = 5e-6;
WP = 5e-6;
L = 1e-6;
```

Figure 3.8: Optimum inverter design script excerpt for user defined device parameters

Table 3.1: Inverter Design Results

Parameter	**Symbol**	**Unit**	**Value**
Supply Voltage	V_{DD}	[V]	1.8
Peak Quiescent Current	I_D	[A]	1.50e−4
NMOS Threshold Voltage	V_{Tn}	[V]	0.3850
PMOS Threshold Voltage	V_{Tp}	[V]	0.3950
NMOS Inversion Slope Coefficient	n_n		2.0386
PMOS Inversion Slope Coefficient	n_p		1.9174
NMOS Process Transconductance	k'_n	[A/V^2]	3.7504e−4
PMOS Process Transconductance	k'_p	[A/V^2]	1.2503e−4
NMOS Channel Length Modulation	λ_n		0.0501
PMOS Channel Length Modulation	λ_p		0.1006
PMOS to NMOS Width Ratio	W_p/W_n		3.1197
NMOS Width to Length Ratio	W_n/L		1.4430
Terminal Voltage Gain	A_{vt}	[V/V]	33.8354
Terminal Voltage Gain (decibels)	A_{vt}	[dB]	30.5874

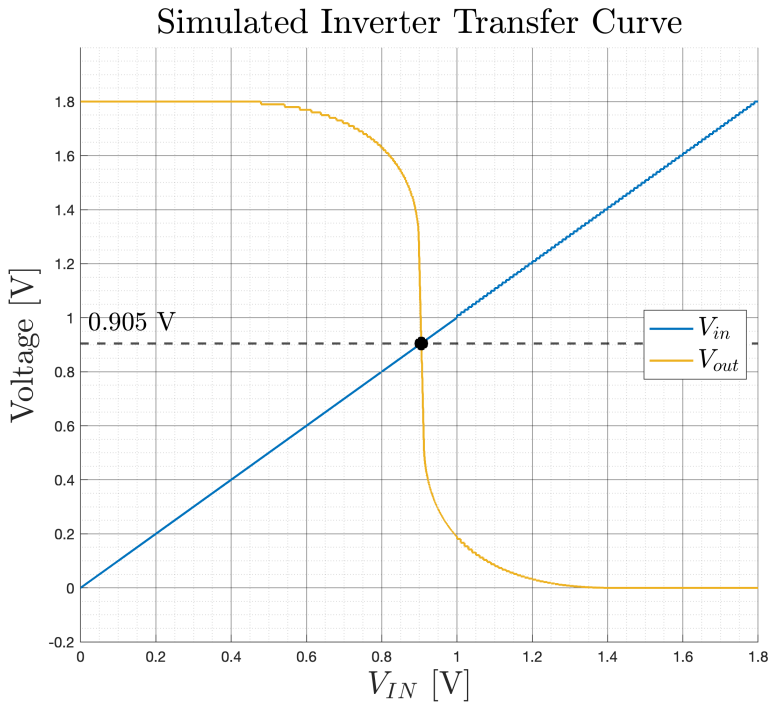


Figure 3.9: Resulting transfer curve for optimized example inverter

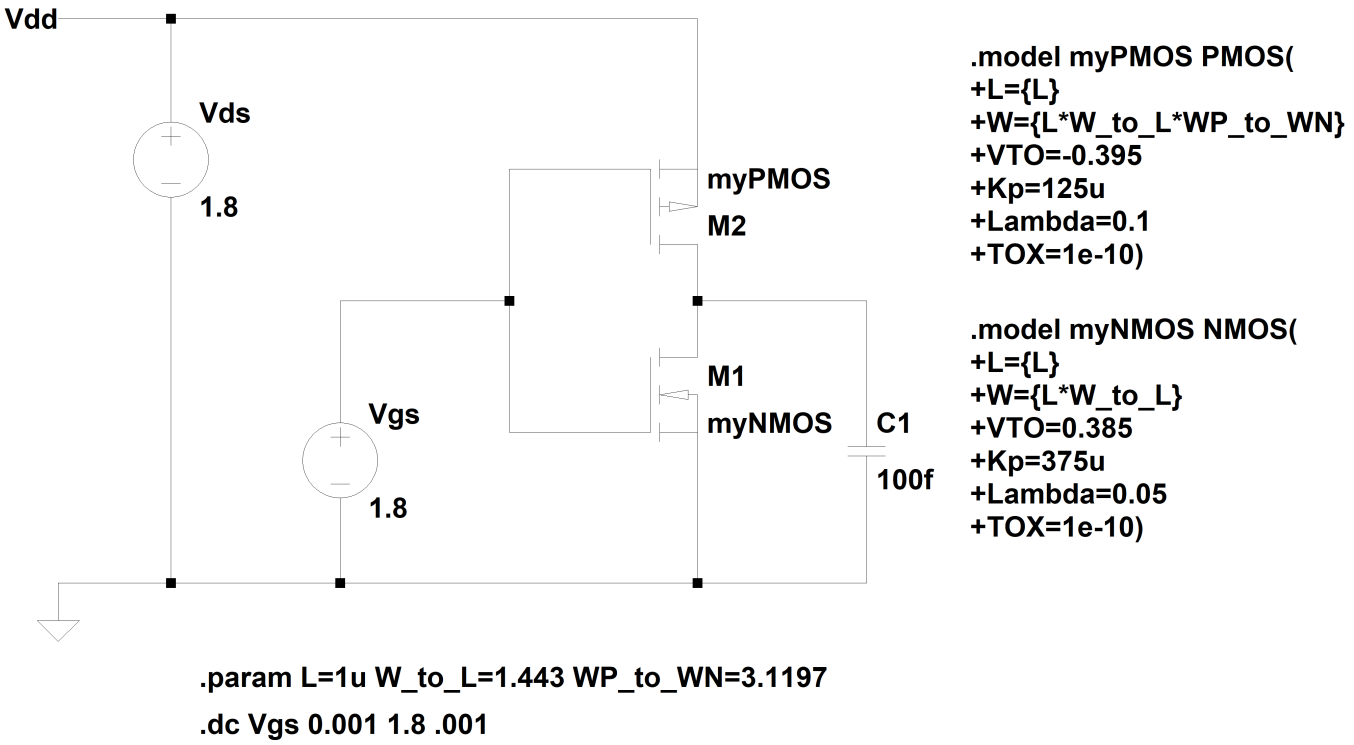


Figure 3.10: LTspice® testbench example for evaluating optimum inverter design

format detailed previously in Section 3.2.1. Through evaluation of both triode and saturation regions of operation within the curves, the necessary parameters can be extracted with the piece-wise MOSFET equations for I_D. The LTspice® testbench shown in Figure 3.7 is used as an example for this pre-inverter-design step. In this example the MOSFET parameters are defined by the `.model` statements. Using the generated IV curves in Figure 3.4, the accuracy of the parameter extraction can be demonstrated by returning similar values as those defined in the example testbench.

Threshold Voltage V_T

The threshold voltage can be approximated from the IV by plotting the V_{GS} versus I_D for a constant V_{DS} if the device is in triode operation. As demonstrated within Figure 3.11, a first-degree polynomial can be approximated from this curve. The x-intercept $V_{x\text{-}int}$ of this line is related to V_T as in Equation (3.7) where α is the surface potential linearization factor and can be approximated as 1 for general examples [60].

$$V_{x\text{-}int} = V_T + \frac{\alpha}{2} V_{DS} \tag{3.7}$$

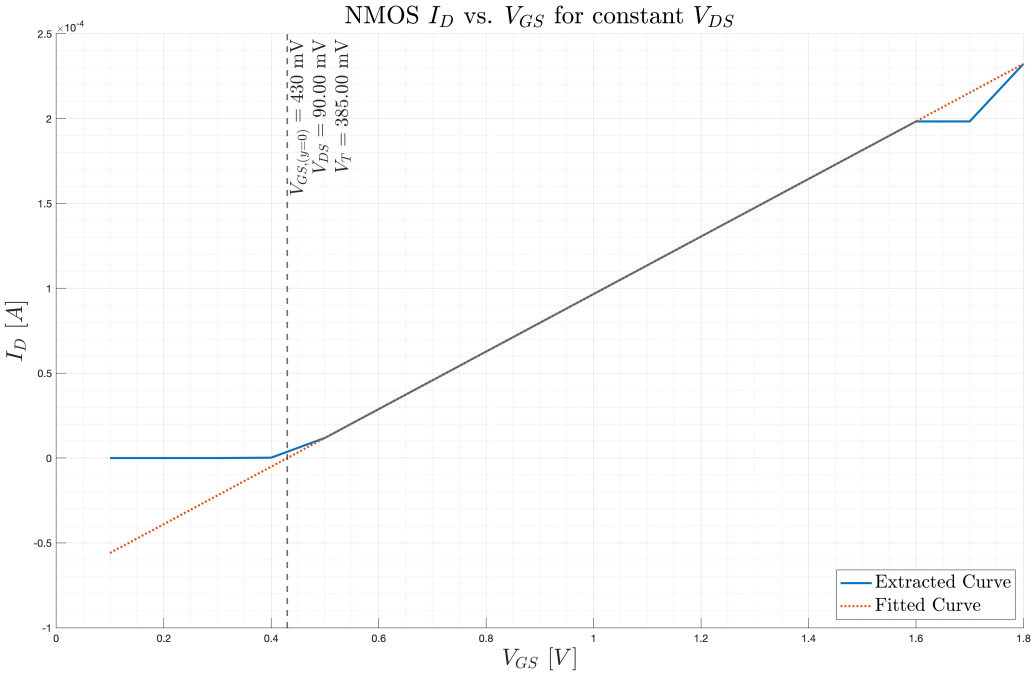
$$\implies V_T \approx V_{x\text{-}int} - \frac{V_{DS}}{2} \tag{3.8}$$

Process Transconductance Parameter k'

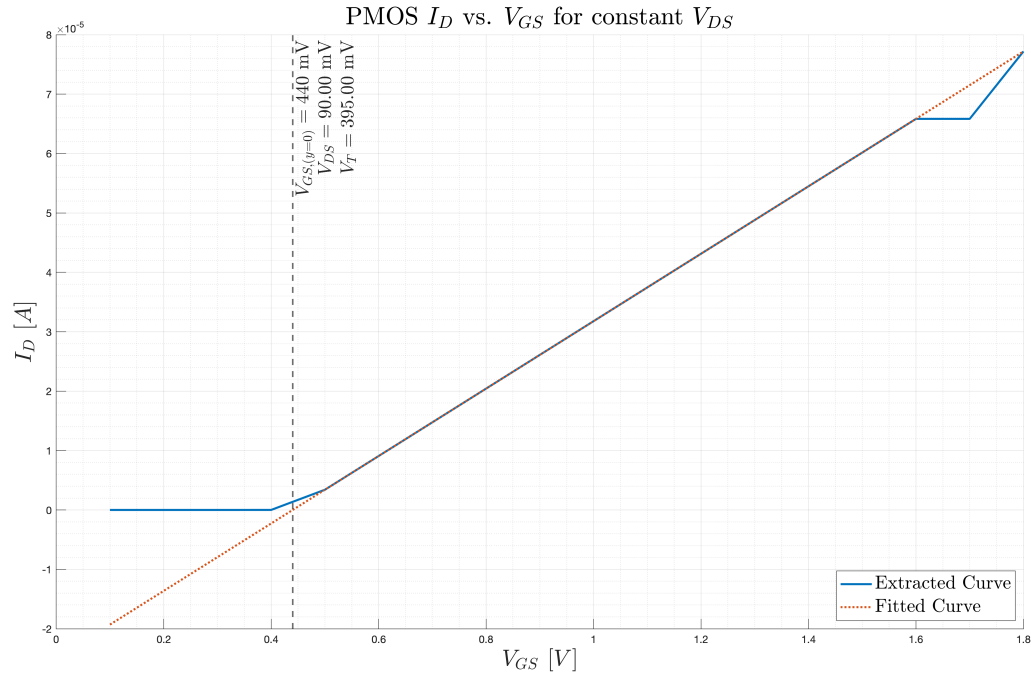
By examining the IV curves V_{DS} versus I_D for constant V_{GS} values an approximated process transconductance parameter k' can be extrapolated. Using the MOSFET I_D equation while in the triode mode of operation, Equation (3.9), removes the dependence of the unknown λ from the equation [60].

$$I_D = k' \frac{W}{L} V_{DS} \left(V_{GS} - V_T - \frac{\alpha}{2} V_{DS} \right) \tag{3.9}$$

Again, letting the surface potential linearization factor $\alpha = 1$ for a general case, and knowing the width W and length L from the simulation testbench configurations of Figure 3.7, the value for k' can be calculated for each point on the IV curves within the range of triode



(a)



(b)

Figure 3.11: *IV* plots of V_{GS} versus I_D for a constant V_{DS} for approximating the threshold voltage V_T of (a) the NMOS and (b) the PMOS devices

operation. The mean of this value is accepted as a satisfactory approximation for the needs of this design procedure.

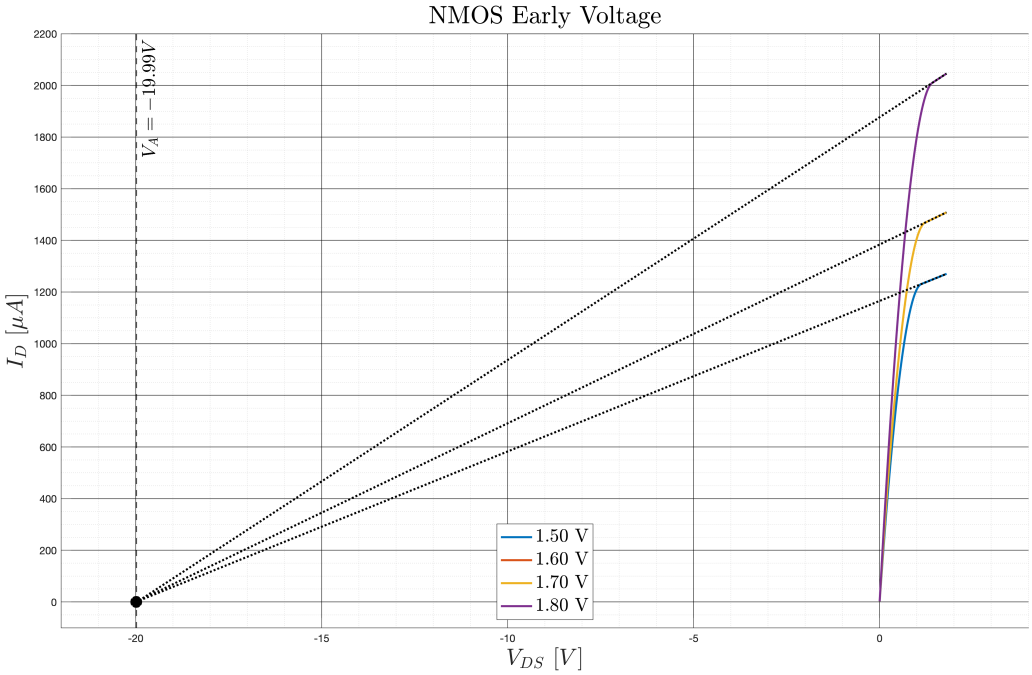
Channel Length Modulation Factor λ

The channel length modulation factor is extracted from the IV curve of V_{DS} versus I_D for constant V_{GS} when the MOSFET is within saturation mode of operation. The most linear portion with the lowest $^{dI}/_{dV}$ values between points can be used to fit a regression line. As in Figure 3.12, the line is extended to the x-intercept. This value of $V_{x\text{-}int}$ is approximately the Early voltage V_A, related to the effective width of the channel.[3] The V_A then has an inverse relationship to the channel length modulation factor λ given in Equation (3.10).

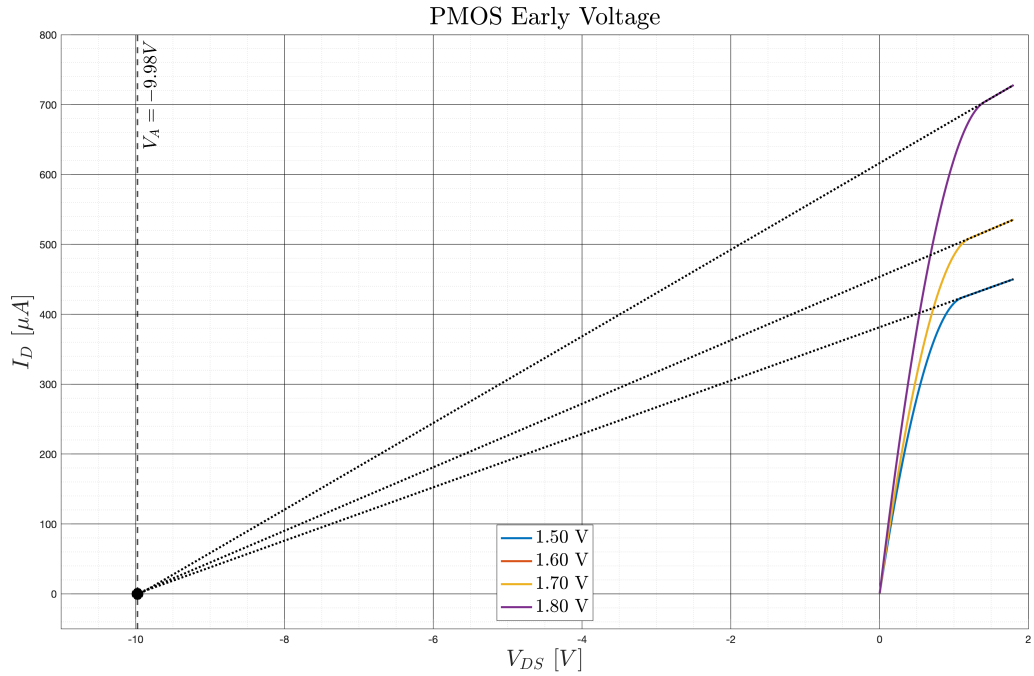
$$V_A = \frac{1}{\lambda} \tag{3.10}$$

The results of this example extraction are given in Table 3.2. The success rate for this example case is nearly perfect, but consideration should be given to the very simple LTspice® models used. For this example, the MOSFET models were unencumbered by the multi-layer behavioral effects built into the models used for most PDKs within Cadence Spectre®. In any case, the accuracy of results should be strong initial approximations to continue the design process.

[3] The phenomenon behind this effect was originally discovered for bipolar devices by Early [61]; thus, receiving the names "The Early Effect" and "The Early Voltage."



(a)



(b)

Figure 3.12: *IV* curves and approximated Early Voltage V_A for (a) the NMOS and (b) the PMOS devices

Table 3.2: Parameter Extractor Results

Parameter	**Unit**	**Input Value**	**Extracted Value**
V_{Tn}	[mV]	385	385
V_{Tp}	[mV]	395	395
k'_n	[µA/V^2]	375	375
k'_p	[µA/V^2]	125	125
λ_n		0.1000	0.1006
λ_p		0.0500	0.0501

Chapter 4

A Multi-Loop Analog LDO

The goal of this work is to design and implement highly efficient, output capacitor-less CMOS LDO voltage regulator for SoC applications. The implemented coordinated control-loop approach leverages the speed of the Ring Amplifier to provide high-speed on-demand assistance during dynamic load-current conditions while an ultra-low-power analog error amplifier maintains stability during quasi-static or steady-state conditions. To reduce the requirement for an area-hungry output capacitor and to maintain stability of a wide range of loading conditions, a Split-Miller internal compensation technique for multi-loop analog controllers is presented in Section 4.2.2, adapted from classic Nested Miller Compensation (NMC) methods.

This work also contributes an original Design Methodology for on-demand, scalable analog amplification using the Ring Amplifier. The design method (previously summarized in Section 3.1) provides a design plan evolved from the ideology that that need-based or performance mode assistance from the Ring Amplifier lessens the burden of LDO error amplifier selection; thus, giving greater freedom to future designers to choose topologies that might not have been solely capable of meeting design requirements. This expands the pool of error amplifier choices to include topologies granting a wider range of stability, increased overall efficiency, or even those whose performances have been degraded by process node scaling (discussed further in Chapter 6). It should then be considered that *any performance limitations inherent to process node scaling of the primary analog amplifier can be dynamically compensated for by the on-demand Ringamp Boost assistance*, enabling more

tilted design trade-offs for efficiency, speed, and accuracy. And furthermore, this realization would not simply be limited to LDO applications, but is portable to any applications space where dynamic, high-gain, high-speed, scalable analog behavior could prove to be technological advancement.

4.1 Design Objectives

The benchmarks for a successful state-of-the-art design should be derived from the performances reported in recent publications, such as those summarized in Chapter 2. These previously reviewed contributions represent the most significant and/or the highest performance LDOs regardless of class (*e.g.*, ALDO, DLDO, or Oscillator-based). Therefore, to achieve state-of-the-art performance the LDO must at minimum meet these target design objectives:

- Maximum output current $I_{OUT} \geq 100\,\text{mA}$
- Steady-state $I_Q \leq 1\,\mu\text{A}$
- Stability or quasi-stability for entire range of I_{OUT}
- Highly precise and rapid transient response
  - Overshoot and Undershoot $\Delta V_{OUT} < \max(V_{DD}) \times 10\,\%$
  - Average settling time $T_{SETTLE} < 500\,\text{ns}$
- Total compensation capacitance $C_{TOTAL} < 50\,\text{pF}$

4.2 The Dual-Loop Analog LDO

The designed output capacitor-less (OCL), dual-loop LDO shown in Figure 4.1 with individual design blocks highlighted. The LDO combines the current mirror operational transconductance amplifier (CMOTA) error amp and general OCL structure previously presented by Milliken *et al.* [27] but replaces the auxiliary transient response current amplifier with an on-demand ringamp. The selected Ring Amplifier topology is an adaptation of the works previously demonstrated for high-speed ADC applications by Lagos *et al.* [51, 52] and Venkatachala *et al.* [57]. The adopted dual-analog-loop control scheme builds upon concepts

presented within the multi-loop DLDOs explored by Huang *et al.* [39, 40], with separate, need-based loops for either ultra-high efficiency or high-performance operation modes.

4.2.1 CMOTA-based LDO Loop

The high efficiency loop is constructed around a current mirror operational transconductance amplifier (CMOTA) error amplifier like that in the previous work by Milliken *et al.* [27] and shown in Figure 4.2. The internal low impedance nodes of the CMOTA push the parasitic poles to very high frequencies, allowing greater space for trade-offs between gain bandwidth and other design objectives [27]. Since the high-performance loop will compensate for sluggish response times of the error amplifier in high demand applications, further room existed to enhance efficiency and stability of the CMOTA-based loop. Using this design leverage, the designed LDO also adapts the CMOTA for wider supply voltage range required in DVS control schemes by optimizing for sub-threshold operation. Maintaining sub-threshold or weak-inversion bias conditions also support ultra-low quiescent current draw (sub-1 µA), maximizing the overall effective LDO current efficiency [62].

CMOTA Error Amplifier

The basic CMOTA design allows for very simple customization for the given application. To reduce the current consumption and bandwidth, the CMOTA was biased to operate in the weak inversion region. Additionally, sub-threshold operation offers an improvement to peak intrinsic voltage gain in scaled process technologies [63, 64]. The small signal voltage gain A_{vo} of the CMOTA has been derived for Figure 4.2 in Equation (4.1) where S is the W/L sizing of the specific device, λ is the channel length modulation, n is the inversion slope factor, and V_t is the thermal voltage [62].

$$A_{vo} = \frac{S_{N4}/S_{N2}}{(\lambda_{N4} + \lambda_{P4})\, n_{P1} V_t} \tag{4.1}$$

The gain of the CMOTA is then almost entirely dependent on the sizing of the devices in the current mirror, the drain currents have very little influence if large signal bias conditions maintain weak inversion and moderate inversion operation. Then for a constant length L

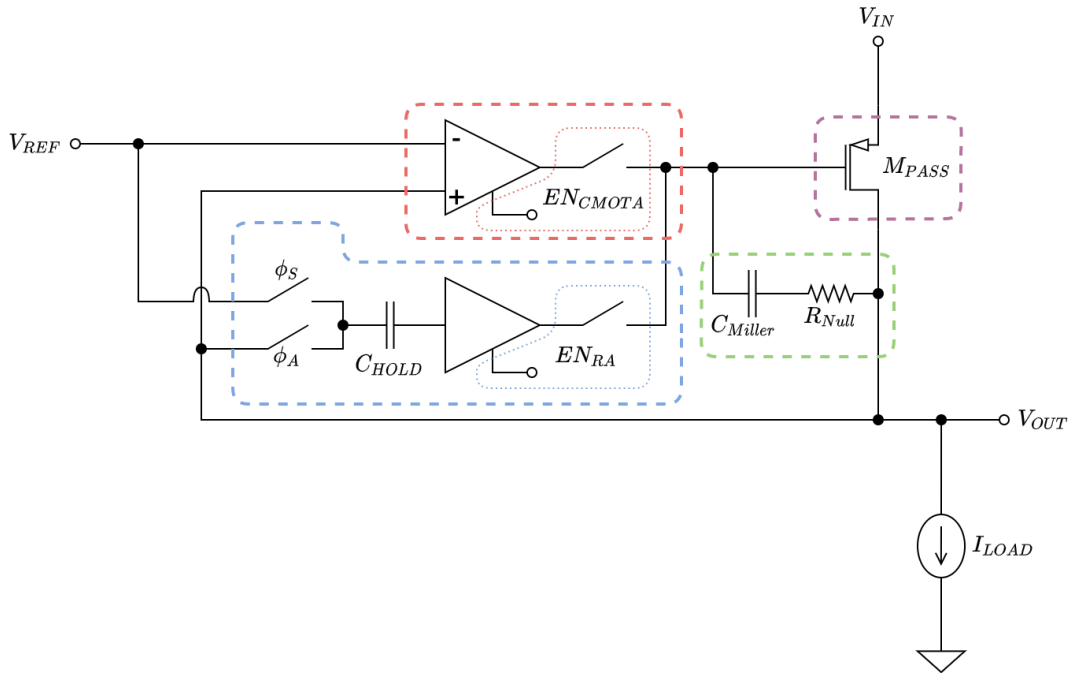


Figure 4.1: System-level schematic of the dual-loop analog LDO

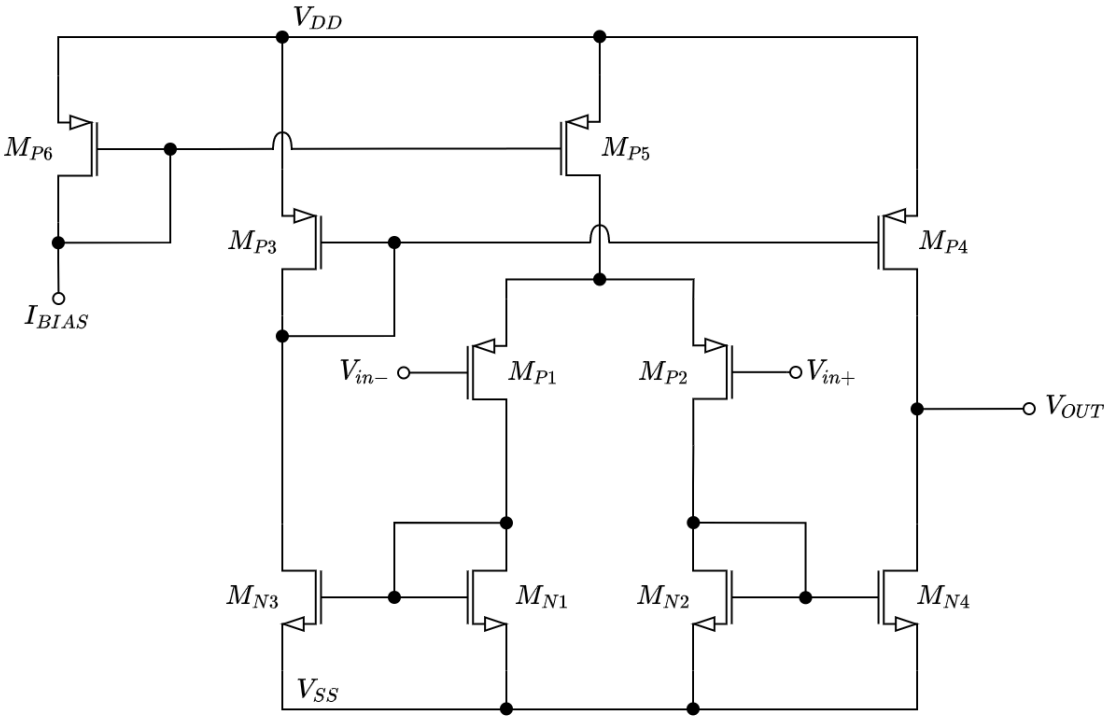


Figure 4.2: Schematic of the CMOTA error amplifier

shared between the devices, the gain can be controlled by the ratio of widths of M_{N4} and M_{N2}.

$$A_{vo} \propto \frac{W_{N4}}{W_{N2}} \tag{4.2}$$

The gain bandwidth GB at room temperature has been shown as Equation (4.3), where C_{out} is the output capacitance [62].

$$GB = \frac{{}^{S_{N4}}/_{S_{N2}}}{C_{out}} \tag{4.3}$$

Using device parameter approximations from the MATLAB® scripts in Appendix B, a CMOTA was designed to achieve $A_{vo} = 40\,\text{dB}$, a Unity Gain Frequency (UGF) of 250 kHz, phase margin $> 65°$ and $I_Q = 350\,\text{nA}$. The frequency response is of the CMOTA error amplifier is shown in Figure 4.3.

CMOTA-based LDO

The frequency response and stability changes dramatically when the weak inversion CMOTA is driving the PMOS pass device array. For a constant dropout voltage V_{DO}, where $V_{DO} = V_{DS}$ for the pass device array, as the LDO load current changes, the output resistance R_{out} due to the pass device's drain-to-source resistance R_{DS} linearly decreases. This relationship is shown in Equation (4.4).

$$R_{out} = \frac{V_{DS}}{I_{LOAD}} = \frac{1}{\mu_p C'_{ox} \frac{W}{L} (V_{GS} - V_T)} \tag{4.4}$$

As the LDO output current I_{LOAD} increases, the total output resistance decreases, pushing the output pole p_{out} into higher frequencies. As I_{LOAD} decreases, an uncompensated p_{out} is pulled much lower causing a dynamic drop in $P.M.$ that can potentially lead to system instability and oscillations. Therefore, any dominant pole compensation should be tuned to accommodate the lowest anticipated value of the uncompensated p_{out}.

Utilizing the Miller Effect to provide internal dominant pole compensation is a common technique for stabilizing output capacitor-less LDOs [7]. Applying Nested Miller Compensation (NMC) around the pass device uses the local negative feedback path to increase the effective capacitance seen looking into the gate of the pass device with respect to the terminal

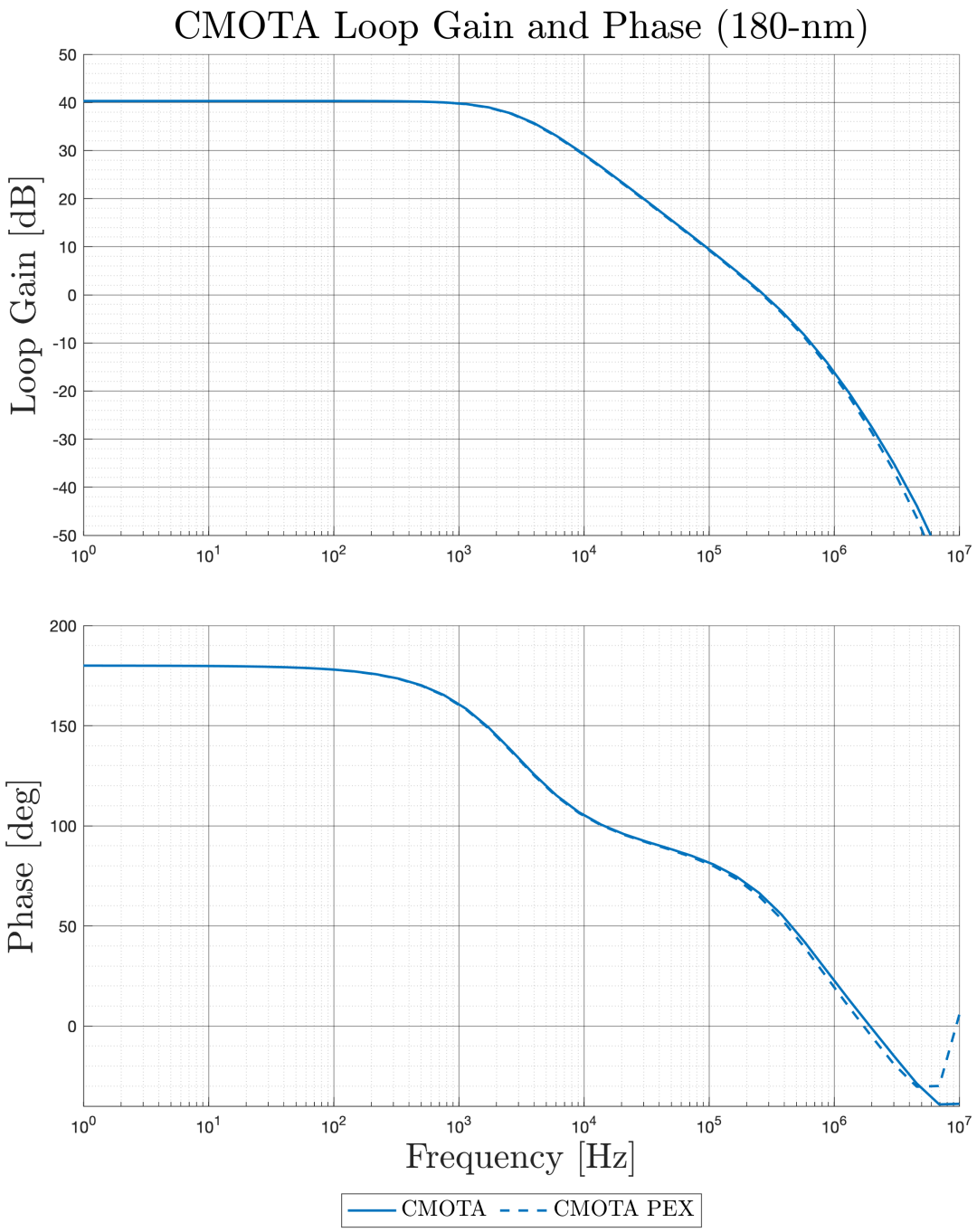


Figure 4.3: 180-nm simulated loop gain analysis of CMOTA error amplifier with post-layout parasitic extraction (PEX)

voltage gain (A_{vt}); but conversely, the Miller Effect reduces the effective capacitance seen looking into the drain towards the gate of the pass device as demonstrated by Equations (4.5) and (4.6) [65].

$$C_{in} = C_{gd}(1 - A_{vt}) \tag{4.5}$$

$$C_{out} = C_{gd}(1 - {}^{1}/_{A_{vt}}) \tag{4.6}$$

For the CMOTA-based LDO configuration shown in Figure 4.4, the dominant pole is established at the output of the error amplifier (p_{ea}). The frequency value of p_{ea} can be approximated as in Equation (4.8) for a given R_{out} [27, 66].

$$\text{Let,} \quad C_m = C_{gd} + C_{Miller} \tag{4.7}$$

$$p_{ea} \cong \frac{1}{R_{ea} C_m g_{mP} R_{out}} \tag{4.8}$$

The non-dominant output pole p_{out} can then be approximated by Equation (4.9) [27, 66].

$$p_{out} \cong \frac{g_{mP} C_m}{C_{ea} C_m + C_{out} C_m + C_{ea} C_{out}} \tag{4.9}$$

An undesirable byproduct of Miller compensation is pulling the Right Half Plane (RHP) Zero looking into the gate of pass device (z_{gd}) within the gain bandwidth of the LDO. The uncompensated RHP Zero can be described by Equation (4.10) [66].

$$z_{gd} = \frac{g_{mP}}{C_{gd}} \tag{4.10}$$

This can be countered by adding the Nulling Resistor R_{Null} to control the placement of this zero and push its location into the Left Half Plane (LHP). With the addition of R_{Null}, the value of z_{gd} can be approximated by the set of conditional definitions within Equation (4.11)

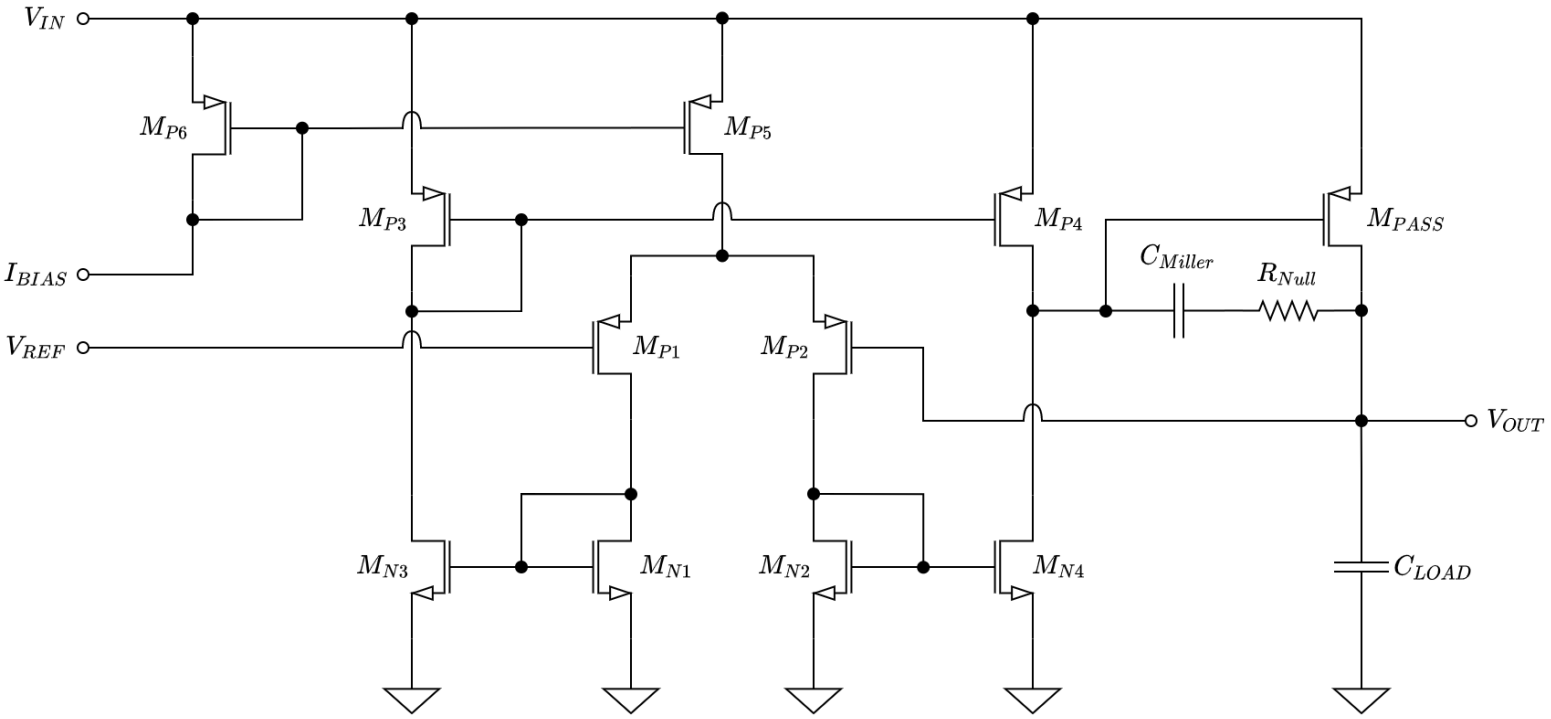


Figure 4.4: Equivalent schematic of the CMOTA-based LDO loop

[66].

$$z_{gd} \approx \begin{cases} +\frac{g_{mP}}{C_m} & \text{if } R_{Null} = 0; \\ -\frac{1}{C_m\left(\frac{1}{g_{mP}} - R_{Null}\right)} & \text{if } R_{Null} > 0; \\ -\frac{g_{mP}}{R_{Null} C_m} & \text{if } R_{Null} \gg {}^{1}/_{g_{mP}}. \end{cases} \tag{4.11}$$

For the designed CMOTA LDO-loop, z_{gd} was tuned to exist just beyond the UGF. This provides a conditional pole cancellation effect as p_{out} approaches and crosses the UGF. With device parameters extracted simulations, a CMOTA-based LDO was designed achieving $A_{vo} = 68\,\text{dB}$, UGF $= 165\,\text{kHz}$, $P.M. > 40°$ when $I_{LOAD} = 1\,\mu\text{A}$, and $I_Q = 350\,\text{nA}$. The frequency response is of the CMOTA-based LDO loop is shown in Figure 4.5.

4.2.2 Ringamp-based LDO Loop

The course burst-mode adjustment loop utilizes a Ring Amplifier adaptation from previous examples for state-of-the-art ADC applications [51, 52, 57]. The ringamp error amplifier within this loop is an abbreviated non-inverting core using only two inverter stages, previously adopted by the RLDO contribution by Park *et al.* [13]. In this configuration the PMOS pass device array functionally behaves as the third inverting stage to the ringamp. The equivalent unity-gain ringamp-based LDO loop is shown in Figure 4.6.

RLDOE Operational Overview

The dual-loop approach allows for both amplifiers share the NMC capacitor C_{Miller} and zero nulling resistor R_{Null}, reducing the need for additional compensation elements. However, the distributed control loops necessitate that each amplifier be asynchronously enabled or disabled from a standby or a similar shutdown state. Each amplifier must also be removed from the loop while inactive to avoid loading the adjacent amplifier's control loop. This was achieved by using transmission gates and expanding enable/disable features demonstrated previously for on-demand ring amplifiers [54, 55, 56]. The adapted RLDO with enable functionality (RLDOE) is shown in Figure 4.7. Additionally, when in standby mode, the

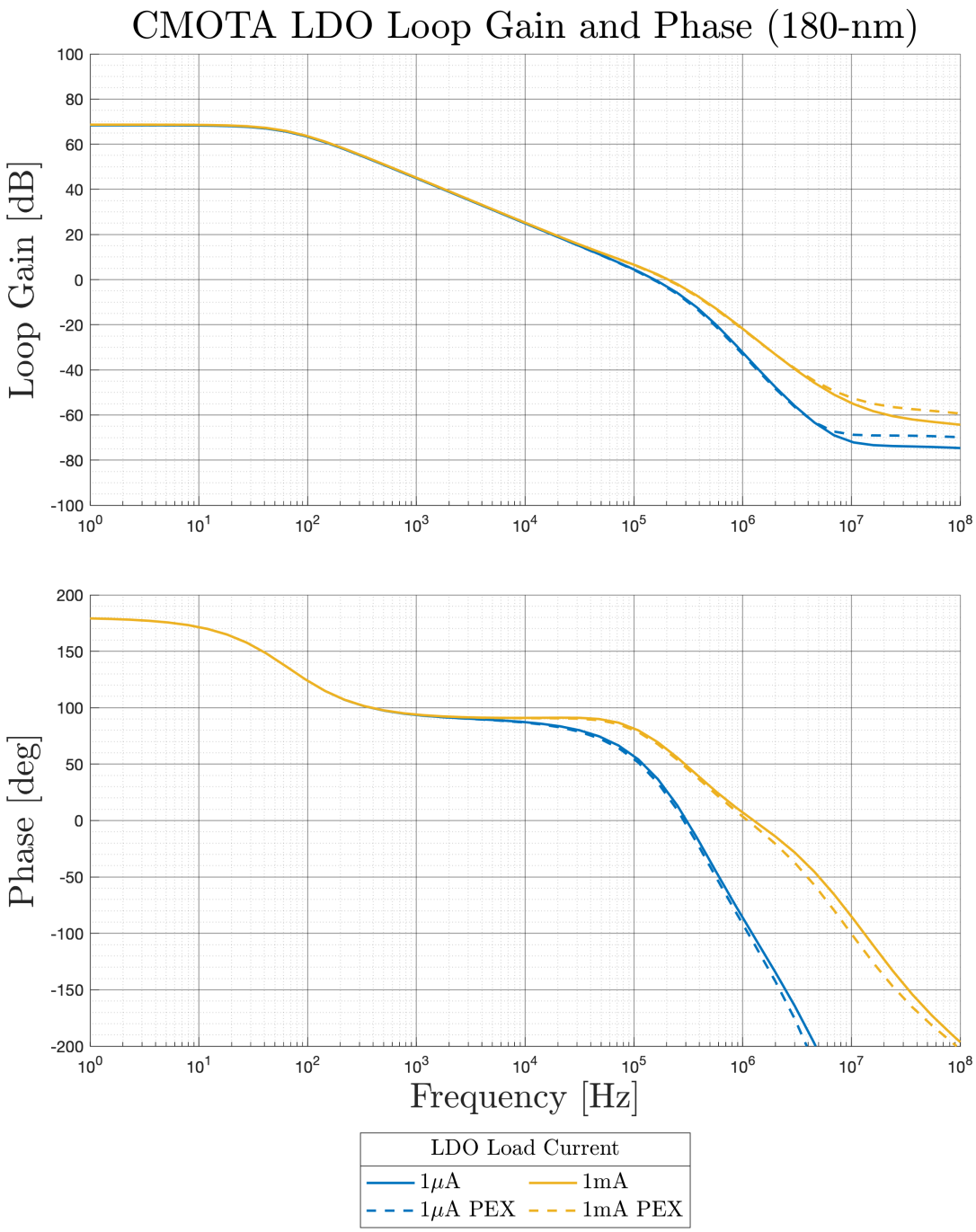


Figure 4.5: 180-nm simulated loop gain analysis of the CMOTA-based LDO loop with post-layout parasitic extraction (PEX)

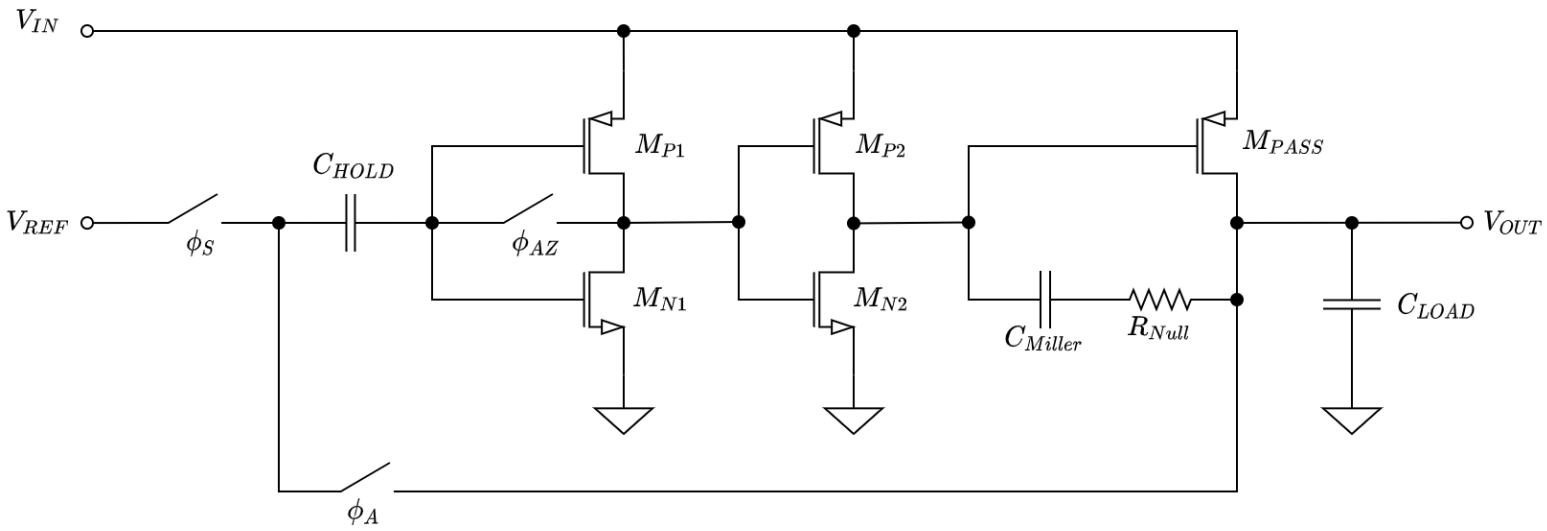


Figure 4.6: Equivalent schematic of the RLDOE loop

ringamp's quiescent current drops below 500 pA, having negligible impact on the overall current efficiency of the LDO.

When enabled, the ringamp samples the input reference voltage V_{REF} onto the bottom plate of the hold capacitor C_{HOLD}, while the top plate is pulled to the auto-zero voltage V_{AZ}. The value for V_{AZ} is designed to be mid-rail or $V_{DD}/2$ to prevent asymmetrical ringamp behavior. This operation is limited to the sampling phase ϕ_S, concluding with the voltage at the bottom plate of C_{HOLD} settles to V_{REF}. The final voltage across C_{HOLD} during ϕ_S is defined as V_{HOLD} in Equation (4.12).

$$V_{HOLD} = V_{REF} - V_{AZ} \tag{4.12}$$

It is advantageous to keep ϕ_S very short so that the LDO output does not slide while the control loop is intermittently broken for the sampling and auto-zeroing execution; hence, the work of Park *et al.* [13] using interleaved Ringamps during auto-zeroing. Since interleaving effectively increases the I_Q, this work's highly efficient design addresses this condition by tuning the time constant τ_{hold} formed by the sampling switch and C_{HOLD}. The duration of the sampling phase $\phi_S > 5\ \tau_{hold}$ to allow for C_{HOLD} to settle to an accurate value; however, a greater duration of ϕ_S leads to a greater magnitude of the LDO output value sliding $\Delta V_{OUT,\phi_S}$. To minimize the output sliding value, τ_{hold} must be much lower than the time constant at the gate of the pass device τ_{pass}. The proportionality of $\Delta V_{OUT,\phi_S}$ to the ratio of τ_{hold} to τ_{pass} can be written as Equation (4.13).

$$\Delta V_{OUT,\phi_S} \propto \frac{\tau_{hold}}{\tau_{pass}} \tag{4.13}$$

A second amplifying phase ϕ_A begins at the conclusion of ϕ_S, where the bottom plate of C_{HOLD} is flipped around the amplifier to the output node for negative feedback. The benefit of using a unity-gain switched-capacitor (SC) configuration is simplicity of the design. Without multiple capacitors matching is not a consideration. The feedback capacitor is perfectly matched to the input capacitor since they are the same physical capacitor. Typical capacitor mismatch mitigation techniques often involve common-centroid layout schemes

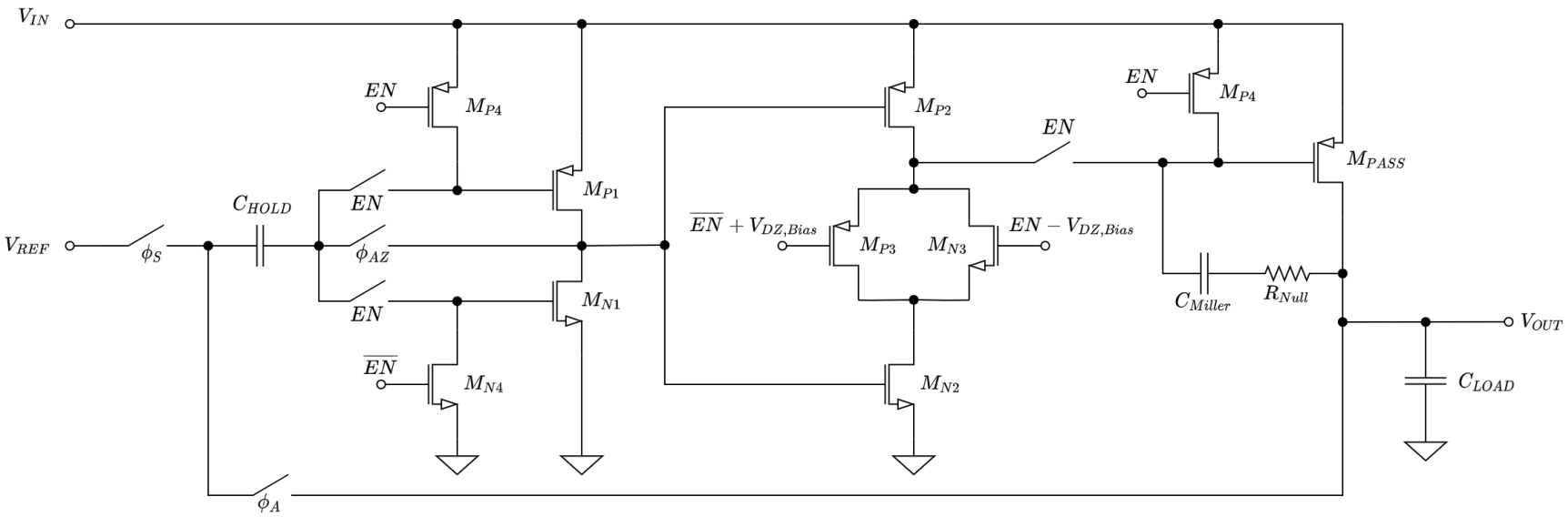


Figure 4.7: Schematic of RLDOE loop with internal dominant-pole compensation, Dead-Zone tuning, and shutdown/enable control

composed of an array of evenly distributed capacitors [67]. The unity-gain flipped-capacitor SC minimizes the required size of C_{HOLD} and maximizes the sampling speed of the amplifier. The negative impact of minimum sized C_{HOLD} is the increased error ratio from charge injection or clock feed-through of the switch and leakage currents from the physical layout of C_{HOLD}. The pedestal errors from the switch can be mitigated through dummy switches or complementary switches [68]; but since in this case the Ringamp loop is only providing an on-demand high-performance mode, any accuracy deficiencies unaccounted for can then be compensated for by the ultra-low power CMOTA loop when the Ringamp loop has been disengaged.

RLDOE Unit Inverter Sizing

The ringamp requires switched-capacitor (SC) feedback to operate, allowing for an auto-zeroing (AZ) interval where the initial DC bias values and operating points at each node can be quickly restored. In the selected ringamp topology, the AZ voltage V_{AZ} should be equal to the transition voltage of the first-stage inverter where $V_{IN} = V_{OUT}$; and furthermore, should be as close to $V_{DD}/2$ to maximize amplifier linearity and minimize offsets due to asymmetric operation. This could only be achieved if the width ratio of the PMOS and NMOS devices were scaled to compensate for the lower carrier mobility μ_p of the high-side PMOS device than higher carrier mobility μ_n of the low-side NMOS device. Using the "All-Region" MOSFET model by Tsividis and McAndrew [60], the drain-to-source large-signal current I_{DS} is defined by Equation (4.14).

$$I_{DS} = \frac{W}{L}\mu C'_{ox}\frac{(V_{GS} - V_T)^2}{2\alpha} \tag{4.14}$$

For Equation (4.14), W and L are the device's width and length, respectively, C'_{ox} is the oxide capacitance-per-unit-area, V_{GS} is the large-signal gate-to-source voltage, V_T is the device threshold voltage, and α is the surface potential linearization factor and will be approximated as $\alpha \approx 1$ for the purposes of initial design assumptions [60]. Using the *Optimum Inverter Design Script* with the *Parameter Extractor Function* in Section 3.2 for the inverter shown in Figure 4.8, values for carrier mobility μ and threshold voltage V_T were approximated for both the PMOS and NMOS devices. With these starting-point estimations, Equation (4.14)

could be solved for W/L as shown in Equation (4.15).

$$\frac{W}{L} = \frac{2 \cdot I_{DS}}{\mu C'_{ox} \left(V_{GS} - V_T\right)^2} \tag{4.15}$$

An inverter's width ratio W_p/W_n can be calculated by dividing the equation for W_p/L by that for W_n/L; letting I_{DS} and L be common between the devices yields Equation (4.16) [1, 60].

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \cdot \left(\frac{V_M - V_{Tn}}{V_M - V_{Tp}}\right)^2 \tag{4.16}$$

The design assistance scripts in Section 3.2 provided extremely accurate results, but transient-based micro-optimizations were iterated until an ideal transition voltage of 900 mV with a supply voltage of 1.8 V was reached. The final inverter transfer curve is shown in Section 4.2.2.

RLDOE T-Gate Design

To facilitate AZ transitions of the SC-architecture when anticipating rail-to-rail dynamic transients at any node, an exclusively NMOS or PMOS gate or switch topology would not be appropriate. Both NMOS and PMOS devices have a quadratic rise in on-state drain-to-source resistance R_{DS} when the input voltage approaches $V_{DD}/2$. This occurs when either V_{in} approaches $V_{DD}/2$ from a lower potential for an NMOS or from a higher potential for the PMOS device [68]. To reduce the effects of dynamic $R_{DS}(V_{in})$, complementary transmission gates (T-gates) were used like the structure shown in Figure 4.10. The equivalent drain-to-source resistance $R_{DS,eq}$ of the T-gate is described by Equation (4.17)

$$\begin{aligned} R_{DS,eq} &= R_{DSn} \parallel R_{DSp} \\ &= \left(\frac{1}{\mu_n C'_{ox} \left(W_n/L\right) \left(V_{DD} - V_{in} - V_{Tn}\right)}\right) \Bigg\| \left(\frac{1}{\mu_p C'_{ox} \left(W_p/L\right) \left(V_{DD} - V_{in} - |V_{Tp}|\right)}\right) \end{aligned} \tag{4.17}$$

Sizing the devices of the T-gate similarly to the process for the inverter results in nearly perfect symmetry of R_{DS} across all values of V_{in} demonstrated by the designed T-gate in Figure 4.11. This symmetrical behavior enables a wider input signal range and assists in

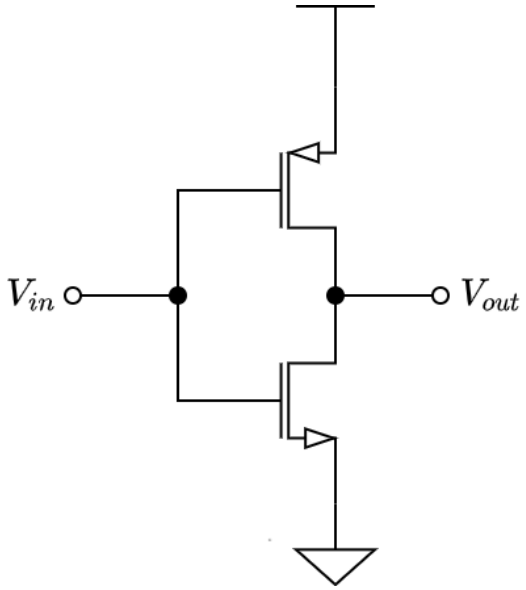


Figure 4.8: Ringamp unit inverter schematic

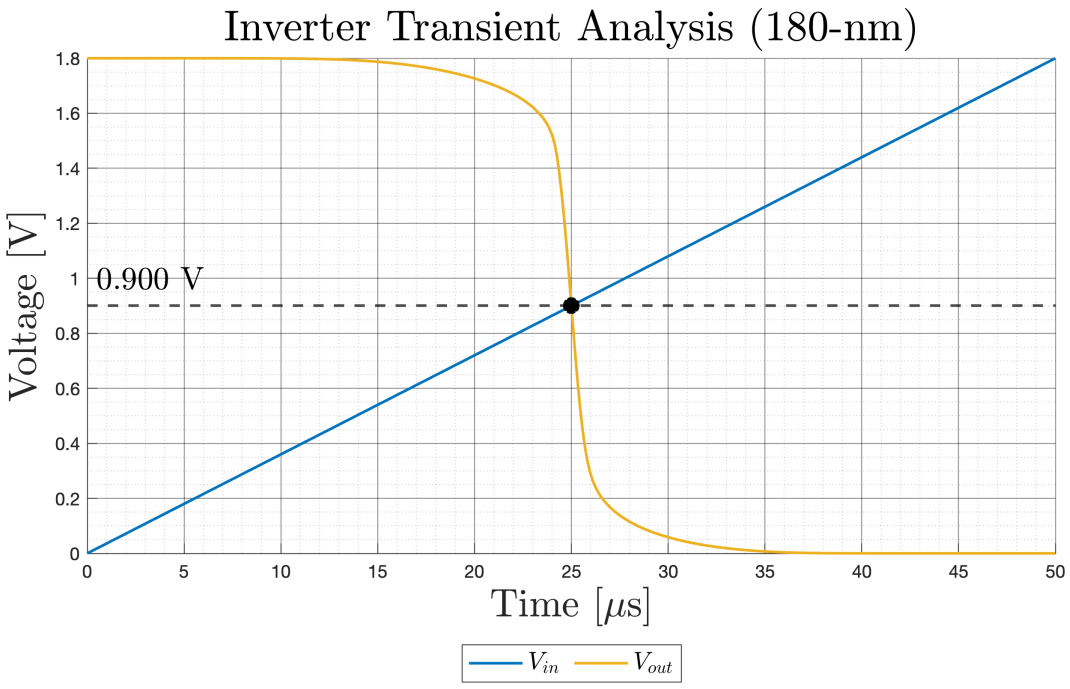


Figure 4.9: 180-nm simulated ringamp unit inverter transfer curve

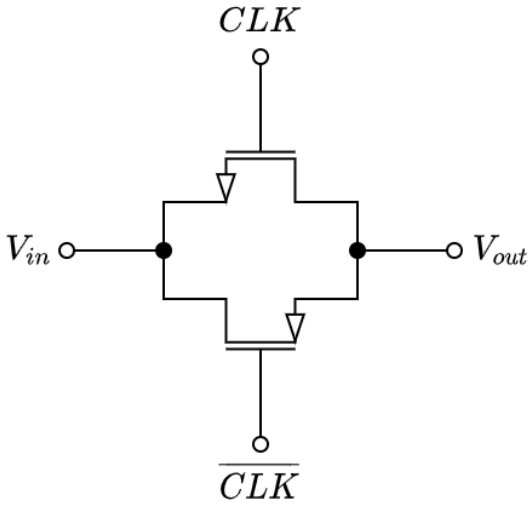


Figure 4.10: Schematic of complementary transmission gate

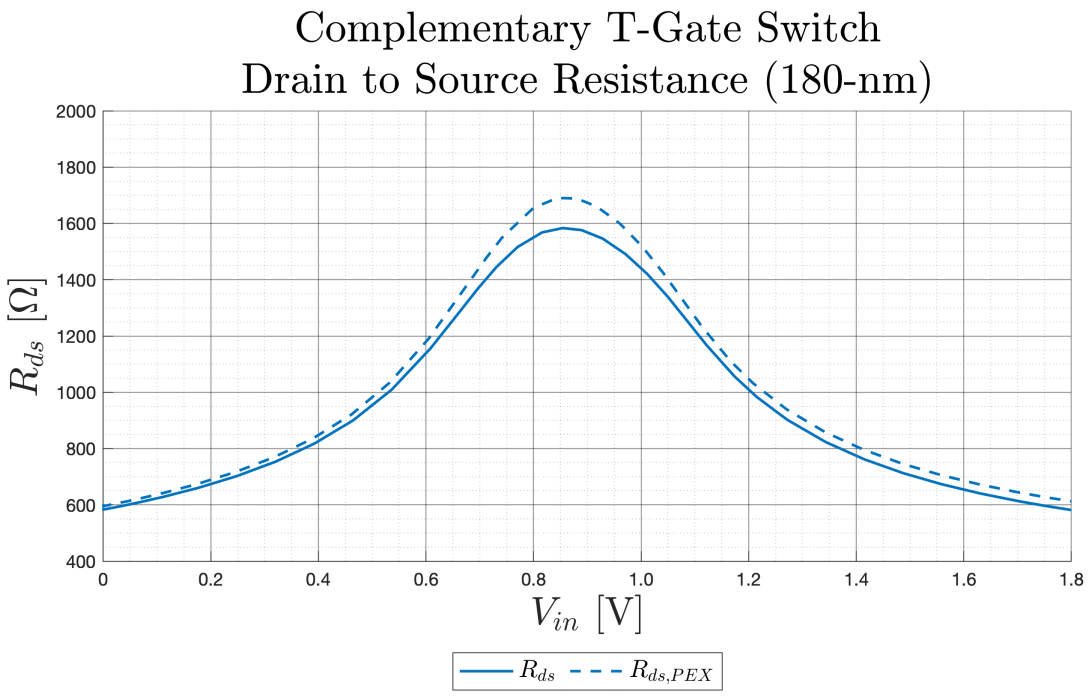


Figure 4.11: 180-nm simulated complementary transmission gate R_{DS} values for the range of input voltage with post-layout parasitic extraction (PEX)

DVS operation [68]. The RLDOE loop uses two sizes of T-gates for different ranges of R_{DS} values. A higher impedance was necessary for the sample and amplify switches to prevent leakage of the hold capacitor C_{HOLD}; however, this is a trade-off for increasing the time constant τ_{hold} and slowing the sample speed of the amplifier. A lower impedance AZ switch was used establish a stable V_{AZ} much more quickly at the top plate of the C_{HOLD} during the sample phase ϕ_S, minimizing the need for independent sub-phases for both sampling and AZ functions.

RLDOE Pseudo-Differential Switch Driver

With the multiple phases necessary for the SC operation of the designed LDO, multiple differential control signals were necessary to drive the complementary gates T-gate structures. To save package pins and chip pads for more validation critical elements, the differential control signals were generated on-chip using a Pseudo-Differential Switch Driver (PDSD) structure previously published by Opris and Kovacs [69]. The PDSD was optimized for the 180-nm process technology and tuned to consume negligible static quiescent current, achieving nearly 1 ns rise and fall times. The fast rise times enabled the PDSD to be used as a digital clock buffer as well to compensate for any control signal degradation from off-chip sources. The PDSD and associated transition waveforms are shown in Figures 4.12 and 4.13.

RLDOE Error Amplifier Design

The frequency response of the ringamp-based LDO loop is a more complicated triple-pole system compared to the dual-pole CMOTA LDO loop. Because of this, the Ring Amplifier topology selected for this work required dominant pole compensation techniques to maintain stability. Referring to Section 2.2.1, the ringamp structure is in essence a ring oscillator. The ringamp only ceases to be an oscillator when a dominant pole is formed at a point within the frequency domain that ensures high enough phase margin to maintain stable or quasi-stable operation.

According to the general ringamp design methodology presented by Hershberg and Moon [70], the individual inverter stages should be composed of as close to minimum sized devices as design specifications will allow. Minimum sized devices with lowest possible input and output

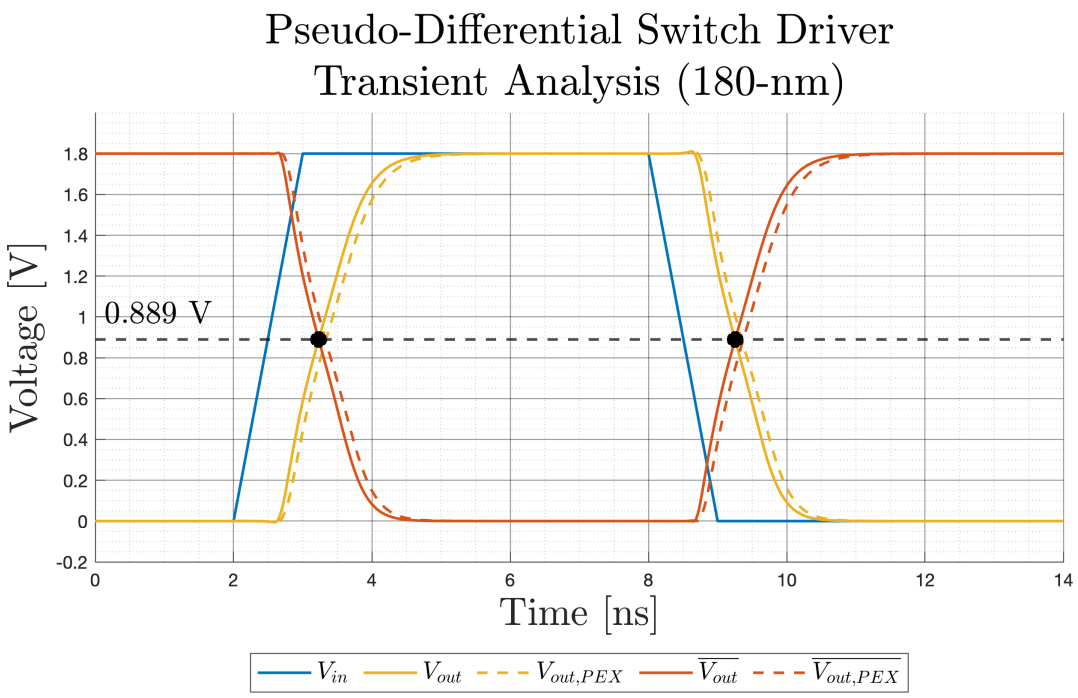


Figure 4.12: 180-nm simulated pseudo-differential switch driver transition waveforms with post-layout parasitic extraction (PEX)

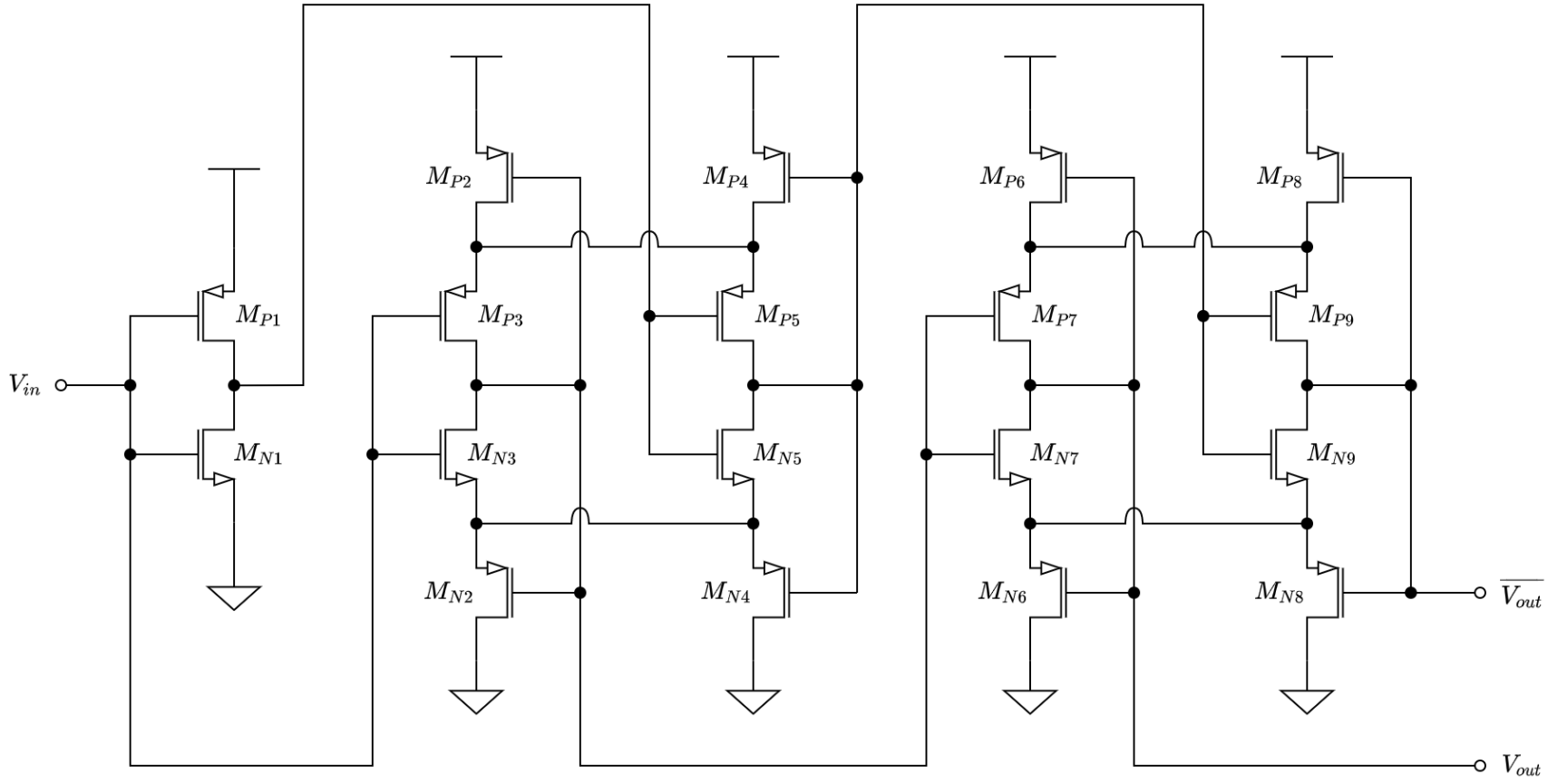


Figure 4.13: Schematic of the Pseudo Differential Switch Driver [69]

capacitances will maximize each stages output poles, allowing them to approach the process transition frequency f_T. With very high inter-stage poles, a much more acceptable value of capacitor can be attached to the output node to establish a dominant output pole and enable the ringamp to behave as a single-pole system with near 90° phase margin [10, 70]. This is a widely accepted compensation technique for ringamps designed for ADC applications where a large output compensation capacitor would consume minimal area compared to the massive arrays of capacitors used for multiple sample-and-hold or track-and-hold functions or even capacitor-based Flash sub-converters. Additionally, for some high-speed cases, internal pole compensation techniques such as NMC can lead to a significant trade-off for bandwidth and efficiency [70].

When designing a Ring Amplifier for LDO applications, the available techniques for stabilization shift considerably from those for data converter applications. In Figure 4.15, the size of the pass device M_{PASS} is dictated by the range of I_{LOAD} and the desired V_{DO}. For the designed multi-loop LDO, the desired peak $I_{LOAD} = 100\,\text{mA}$ a competitively designed $V_{DO} = 200\,\text{mV}$ for 180-nm process technology. This required the effective width of the pass device to be $4000\,\mu\text{m}$ yielding an approximate maximum gate-to-drain capacitance $C_{GD} = 6.2\,\text{pF}$. The pole p_{ra} associated with this node would be an intrinsic dominant pole of the system for a wide range of operating conditions. Compared to previous ADC ringamp examples, the RLDOE's inherently lower internal pole would require a significantly larger output capacitance to pull p_{out} to a position that limits effects of the phase shift from p_{ra} to the RLDOE loop's phase margin; furthermore, this compensation technique would also severely limit the bandwidth of the RLDOE loop. Since p_{ra} is an intrinsic dominant pole, a much smaller amount of compensation capacitance would be necessary lower the pole into a location that ensured stability across the anticipated range of I_{LOAD}. Using Nested Miller Compensation (NMC) would further reduce the required compensation capacitance since the Miller Effect would increase the effective capacitance that determines p_{ea}.

To establish a high bandwidth of stable operation, the first two stages of the ringamp in Figure 4.15 were sized near minimum dimensions so that p_1 would be much higher than the RLDOE's bandwidth, like the methodology proposed by Hershberg and Moon [70]. The first-stage inverter was sized to achieve the frequency response shown in Section 4.2.2 with

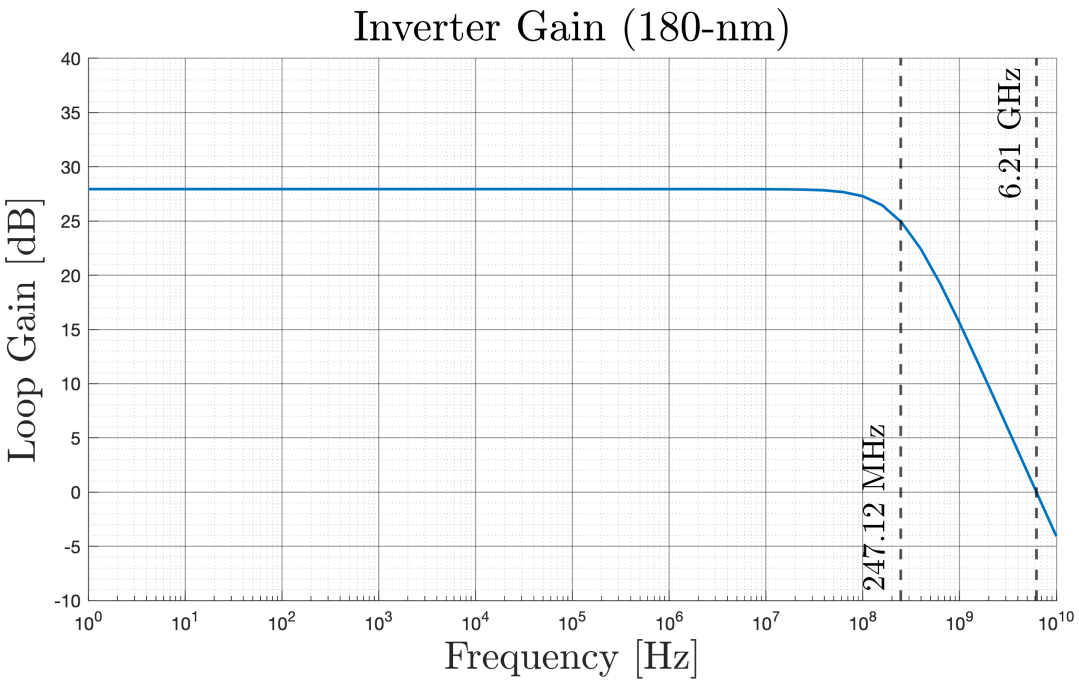


Figure 4.14: 180-nm simulated open-loop frequency response of the RLDOE loop's first stage inverter

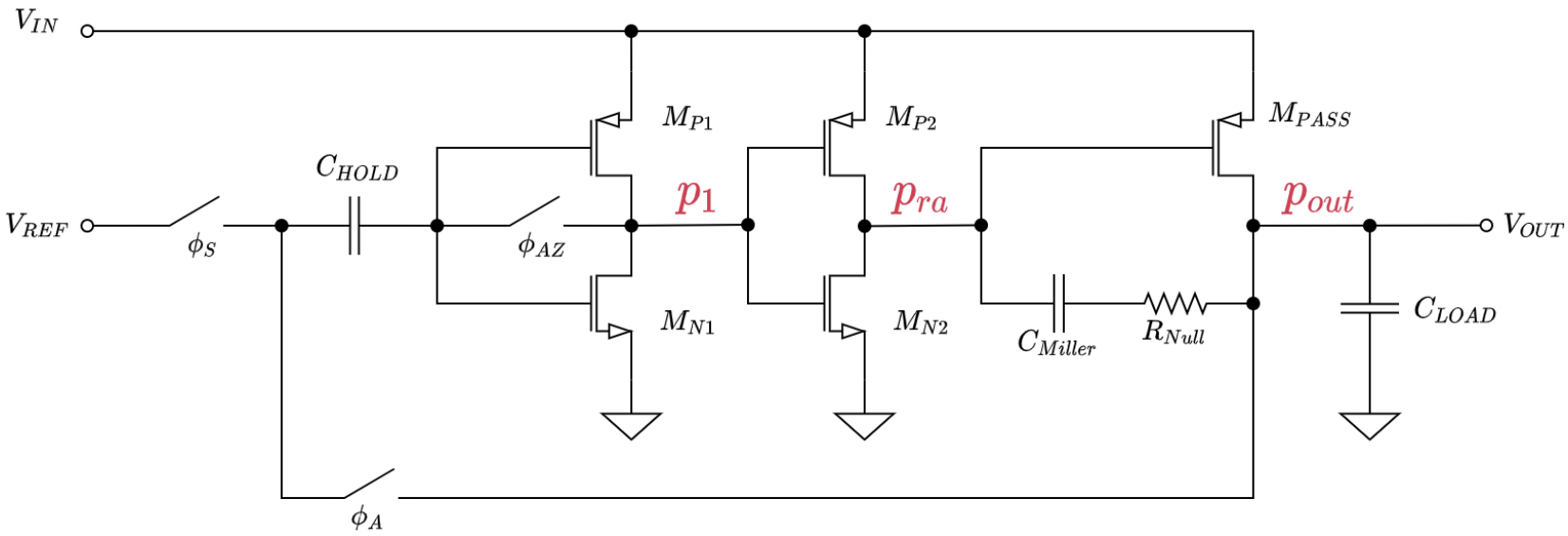


Figure 4.15: Equivalent schematic of RLDOE with labeled pole locations

$p_1 = 247\,\text{MHz}$ and open-loop gain of 28 dB. The dominant pole, p_{ra}, was then able to be optimized with NMC techniques using the local negative feedback around the drain-to-gate of the pass device. The dominant pole value necessary to stabilize the CMOTA loop was much lower than that needed by the RLDOE loop, reducing the bandwidth of the RLDOE loop, and defeating the speed benefit of the ringamp. To lessen this resulting over-damped RLDOE loop, the NMC was split between the loops as shown in Figure 4.16. This allowed the RLDOE loop's bandwidth to be maximized from $< 200\,\text{kHz}$ to 25 MHz.

Splitting the NMC network allows for two distinct sets of poles and zeros at the gate of the pass device for each control loop. The compensated dominant pole of the ringamp p_{ra} is approximated by Equation (4.18) where $R_{DS,eq}$ is the equivalent resistance looking into the T-gate switch and R_{ra} is the output resistance of the ringamp's second stage.

$$p_{ra} \cong \frac{1}{\left(R_{ra} + R_{DS,eq}\right)\left(C_{gd} + C_{Miller}\right) g_{mP} R_{out}} \tag{4.18}$$

Then the zero around the gate-to-drain of the pass device for the RLDOE loop z_{ra} can be defined as Equation (4.19).

$$z_{ra} = -\frac{1}{\left(C_{gd} + C_{Miller}\right)\left(\frac{1}{g_{mP}} - R_{Null}\right)} \tag{4.19}$$

When the Ringamp is disabled and the CMOTA is engaged, a new dominant pole is formed at the output of the CMOTA error amplifier. This pole, p_{cmota}, can be approximated by Equation (4.20) where R_{cmota} is the output resistance of the CMOTA and the same value $R_{DS,eq}$ is assumed for both loop's T-gate switches.

$$p_{cmota} \cong \frac{1}{\left(R_{cmota} + R_{DS,eq}\right)\left(C_{gd} + C_{Miller} + C'_{Miller}\right) g_{mP} R_{out}} \tag{4.20}$$

The zero around the gate-to-drain of the pass device for the CMOTA loop z_{cmota} can be defined as Equation (4.21).

$$z_{cmota} = -\frac{1}{\left(C_{gd} + C_{Miller} + C'_{Miller}\right)\left(\frac{1}{g_{mP}} - R_{Null} \| R'_{Null}\right)} \tag{4.21}$$

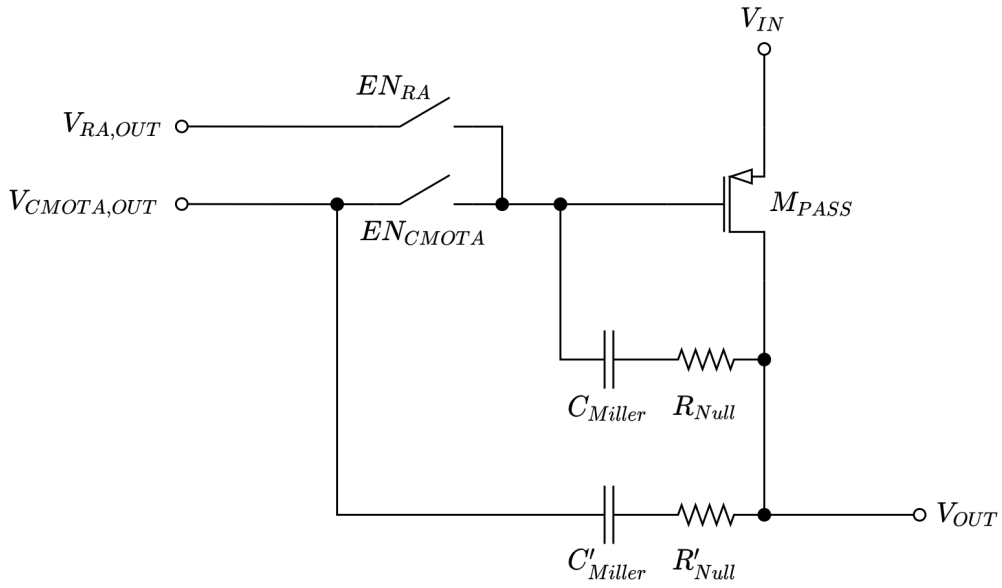


Figure 4.16: Split-Miller Compensation technique for designed multi-loop LDO

The primary disadvantage of this NMC splitting technique is that there always exists a current path from the CMOTA error amplifier's output to the output node of the LDO; this is regardless of the state of the CMOTA (engaged or disengaged). To mitigate the negative effects of this path, a large R'_{Null} was necessary. Since the relationship of z_{cmota} to R'_{Null} is limited by the parallel combination of $R_{Null} \| R'_{Null}$, the maximum size of R'_{Null} is only bound by parasitic effects and area constraints. The frequency response is of the ringamp-based LDO loop is shown in Figure 4.17.

4.2.3 Power Supply Rejection

A significant disadvantage of chosen NMC approach is its dominant effect on power supply rejection (PSR). Consider the simplified schematic of the designed dual-loop LDO's output stage shown in Figure 4.18 with limited small signal parameters. PSR is defined as the AC gain or attenuation from V_{in} to V_{out}. It can be seen from a simple nodal analysis how similar the PSR analysis of the dual-loop LDO is to the previous loop analysis. Since the designed LDO is an OCL topology we can assume that the output impedance Z_O is dominated by the split-Miller compensation loop impedance Z_{gs}. Then, let Z_{ds} be the lumped impedance of small signal parameters of M_{PASS} from the drain-to-source terminals. The PSR nodal system in Equations (4.22) and (4.23) can then be created.

$$0 = \frac{V_{out} - V_{in}}{Z_{ds}} + \frac{V_{out}}{Z_{gd}} \tag{4.22}$$

$$\frac{V_{out}}{V_{in}} = \frac{Z_{gd}}{Z_{gd} + Z_{ds}} \tag{4.23}$$

Since the values for C_{ds} of the pass device should be extremely small, this term can be neglected for simplified analysis and Z_{gd} can be defined as equal to R_{ds} or $1/g_{ds}$. We can simplify the terms contained within Z_{gd} by lumping the capacitances C_{Miller} and C_{gd} into the term C_M. Then the nodal system can be rewritten as Equation (4.24)

$$\frac{V_{out}}{V_{in}} = \frac{R_{Null} + 1/sC_M}{R_{Null} + 1/sC_M + R_{ds}} \Longrightarrow \frac{1 + sR_{Null}C_M}{1 + sC_M\left(R_{Null} + R_{ds}\right)} \tag{4.24}$$

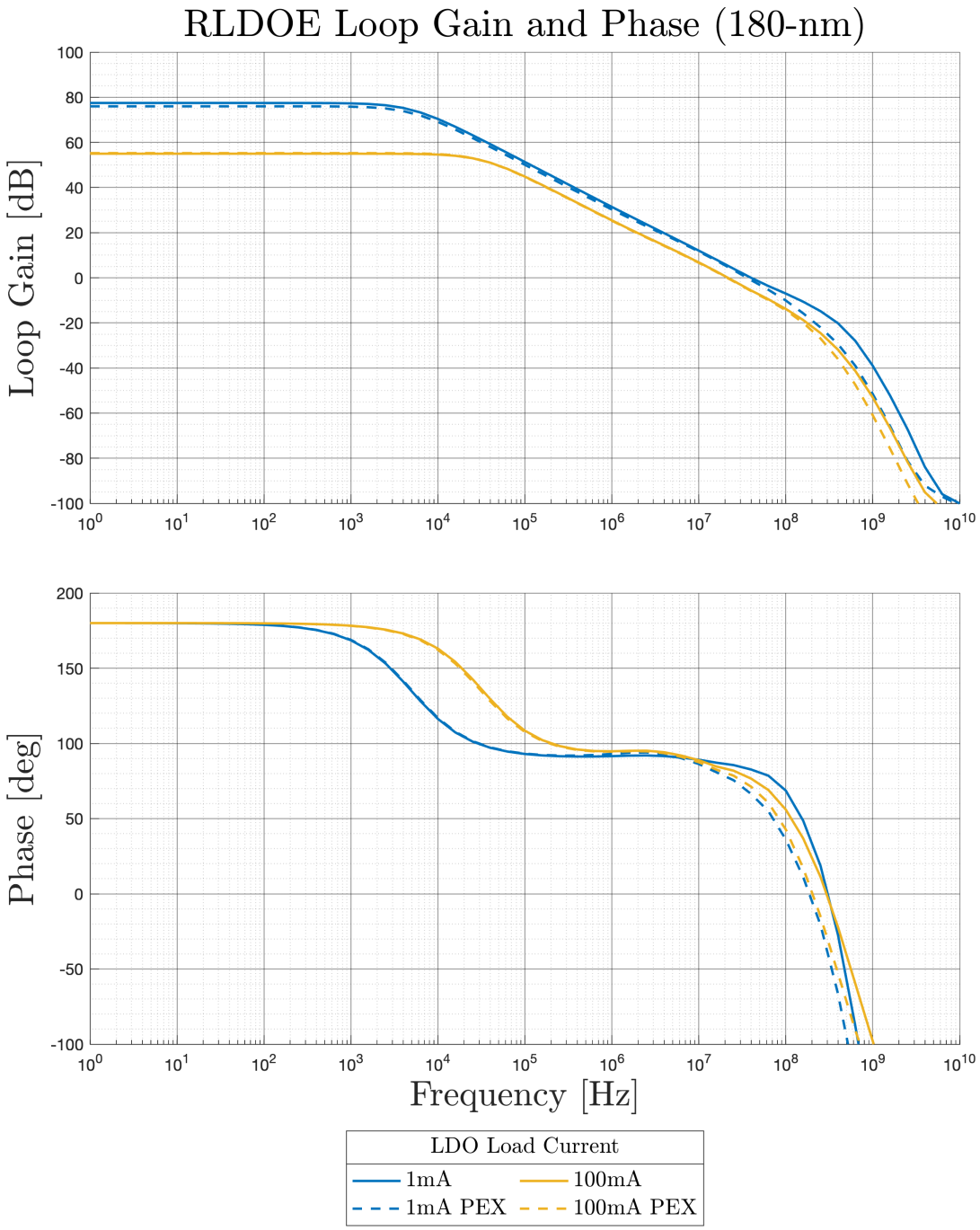


Figure 4.17: 180-nm simulated loop gain analysis of RLDOE loop with post-layout parasitic extraction (PEX)

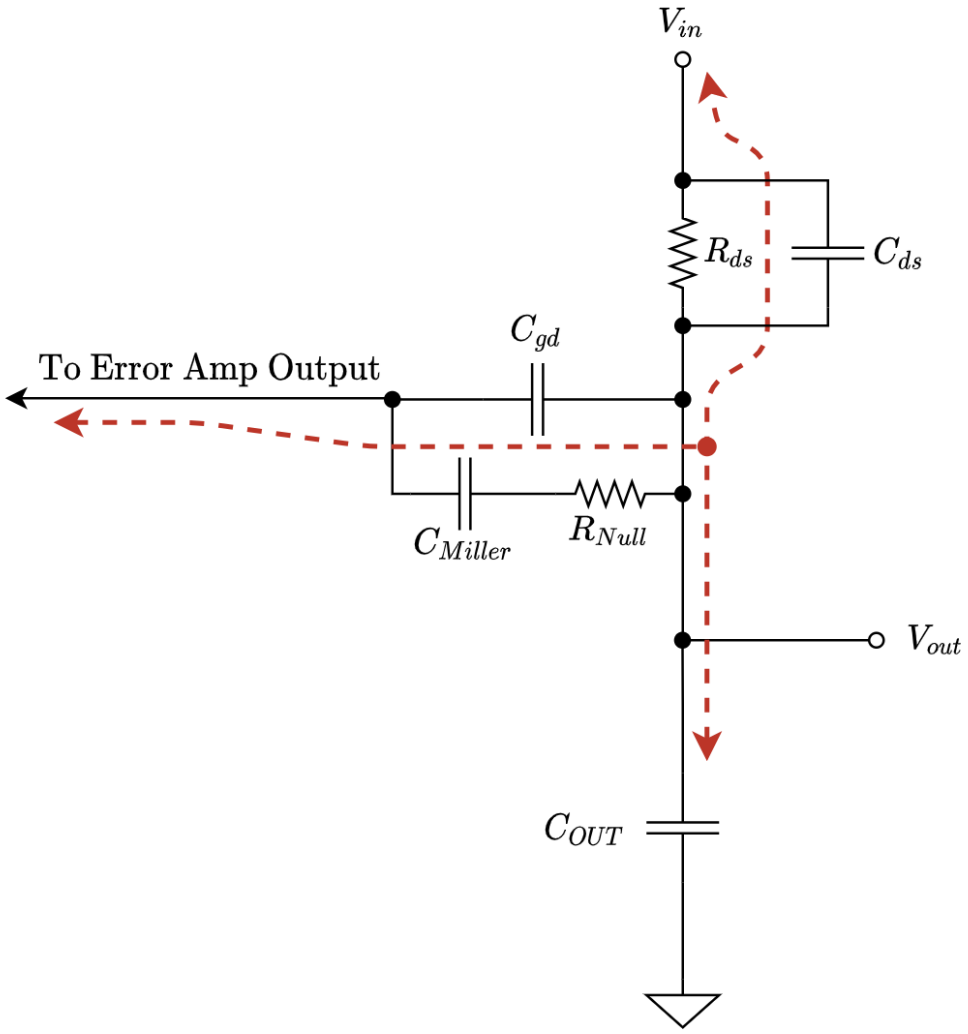


Figure 4.18: Simplified schematic of the designed dual-loop LDO's output stage with small signal parameters of the pass device M_{PASS}, for PSR analysis the AC current paths from V_{out} are shown by **red** arrows

Then separating the terms within C_M, the equation can be finally written as Equation (4.25)

$$\frac{V_{out}}{V_{in}} = \frac{1 + sR_{Null}\left(C_{gd} + C_{Miller}\right)}{1 + s\left(C_{gd} + C_{Miller}\right)\left(R_{Null} + R_{ds}\right)} \tag{4.25}$$

It should be apparent now that the pole and zero from the transfer function in Equation (4.25) are essentially the same as the poles and zeros defined previously in Equations (4.18) to (4.21) for the frequency tuning of the split-Miller compensation technique. Hence, the compensated dominant pole of NMC is the corner frequency of the PSR bandwidth as shown in the simulated PSR plots in Figures 4.19 and 4.20 [62]. It has also been shown that the magnitude of the PSR attenuation is directly proportional to the loop gain of the LDO [71].

4.3 Physical Implementation

The proposed multi-loop analog LDO was fabricated in a 180-nm standard silicon process. An optical microscope photograph of the full Teucer Chip is shown in Figure 4.21. The Teucer Chip's organization (shown in Figure 4.22) consists of two independent Multi-Loop LDO iterations and individual test cells for the CMOTA, M_{PASS} device, and peripheral circuitry for characterization or troubleshooting if it becomes necessary during the evaluations. The implemented LDO 1 includes multiple points of external connections to assist in behavioral evaluations, where LDO 2 is a direct implementation of the designed multi-loop LDO.

Each physical LDO is configured to have individual off-chip power supplies supporting the error amplifiers, V_{IN} for the pass device, in addition to $DVDD$ for the digital support circuitry. The power supplies for V_{IN} and $DVDD$ were shared between the two LDOs since the adjacent disengaged LDO's loading effect on those supplies was negligible during operation. Thus, there is a total of four isolated off-chip power supplies just between the two LDO circuits assisting in more accurate and distinguishable current consumption monitoring. The filter cap arrays in the northern corners provide power supply filtering for additional in-pad ESD protection and the test cells.

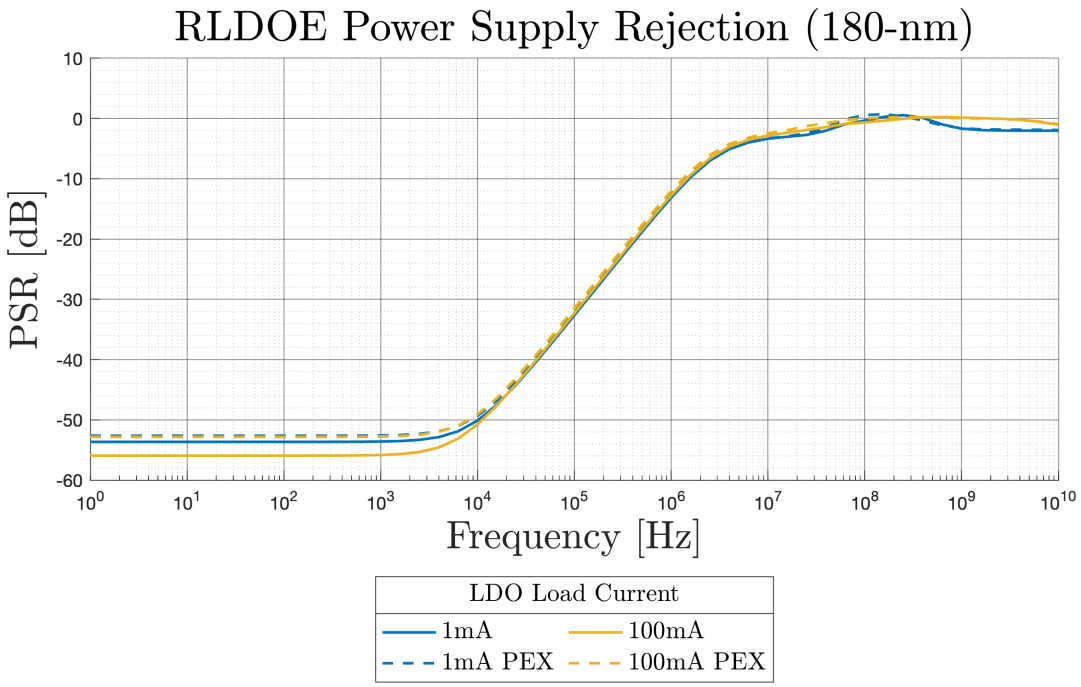


Figure 4.19: 180-nm simulated power supply rejection (PSR) performance of the RLDOE loop

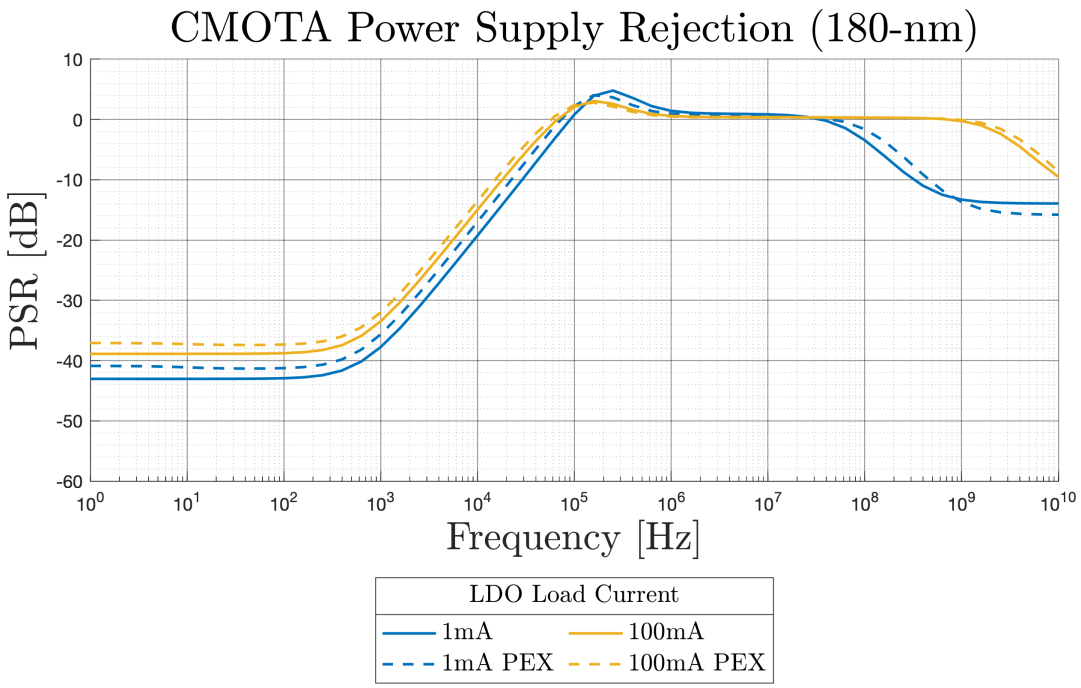


Figure 4.20: 180-nm simulated power supply rejection (PSR) performance of the CMOTA loop

The physical implementation of LDO 2, shown in Figures 4.23 and 4.24, has an active area of 0.018 mm^2. The pass device arrays consume 0.03 mm^2 each and the integrated compensation capacitance consumes 0.02 mm^2. The total area for the LDO is 0.068 mm^2. The determined Miller capacitance necessary for wide range stability is 23.3 pF. The RLDOE required 16.13 pF compensation capacitance and the CMOTA loop added the remaining 7.17 pF when engaged. The Cadence® layouts of individual cells are provided in Appendix D.1, including finer resolution figures and dimensions for the CMOTA, RLDOE, and all required support circuitry. The evaluation results of this physical implementation are described in Chapter 5.

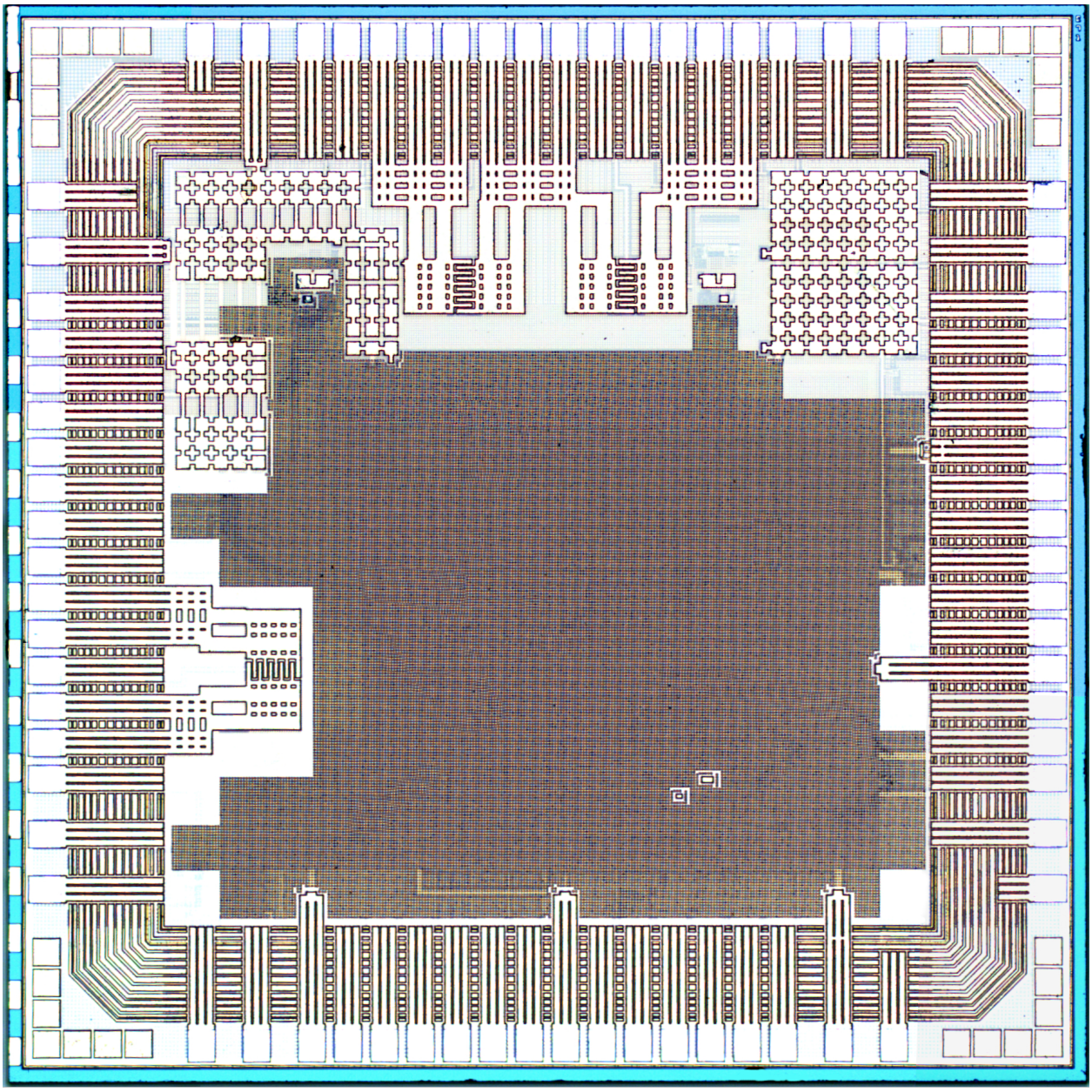


Figure 4.21: Microscope photograph of full 5 mm^2 Teucer chip; named for the Greek archer who suffered great personal loss during the Trojan War and then was forced into exile by his own father, King Telamon. Despite hardships, Teucer remained a positive and hopeful leader for his comrades and ultimately saw great fortunes by his own doing. "Do not despair... tomorrow we recross the wide, wide sea! (*Odes* 1.7.28-32 Conington 1882)"

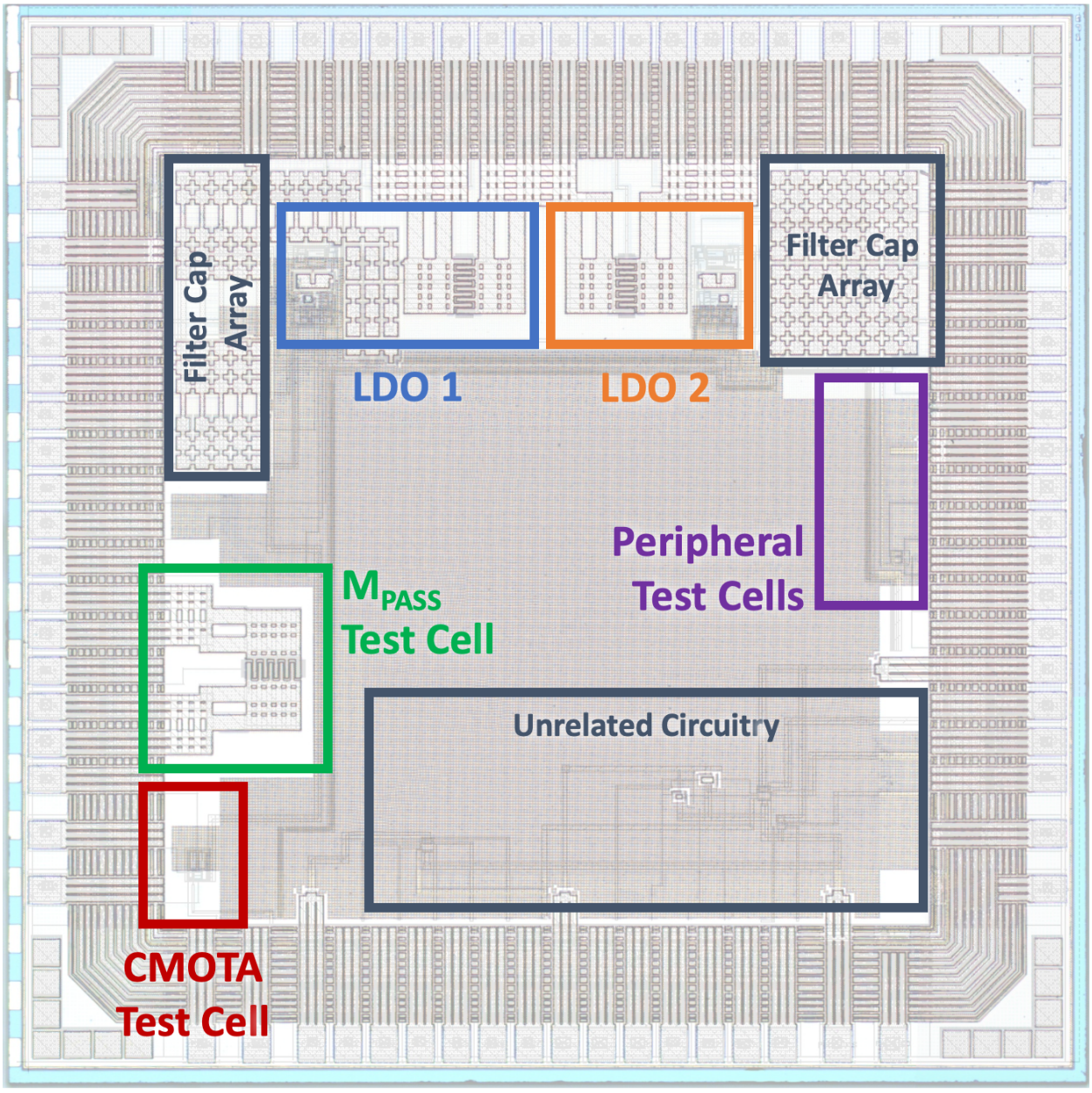


Figure 4.22: Teucer chip microscope photograph interlaced with a Cadence® full chip layout image with unique sections labelled

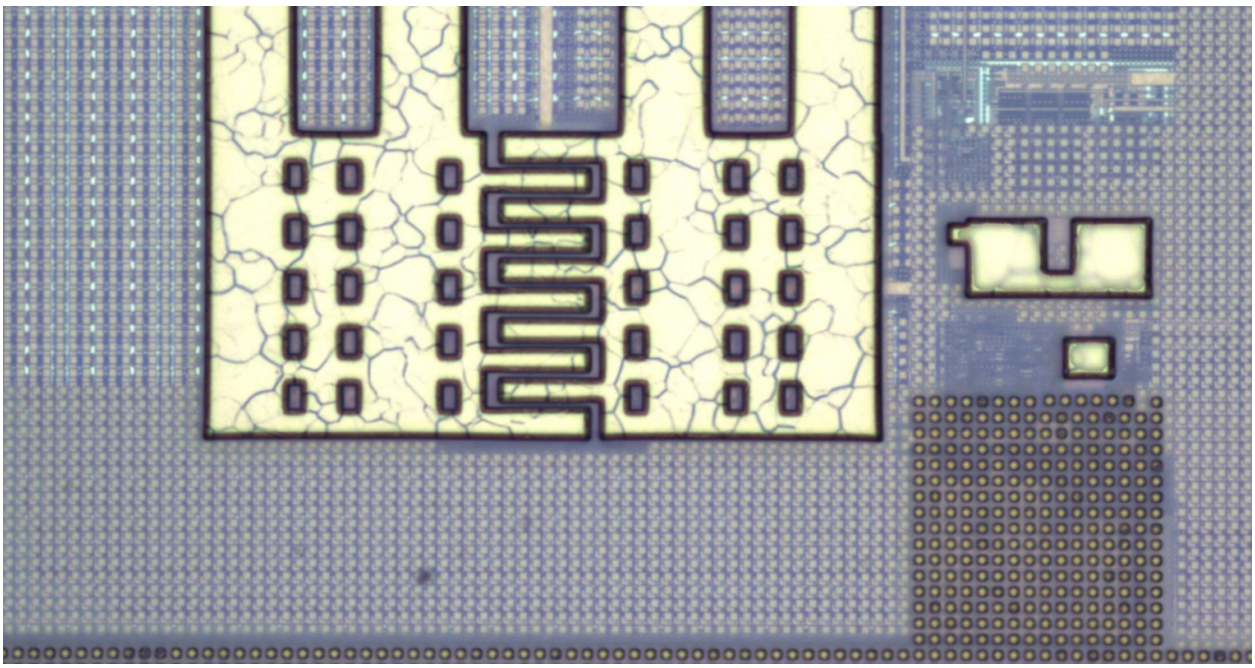


Figure 4.23: Microscope photograph of the implemented multi-loop LDO's active area)

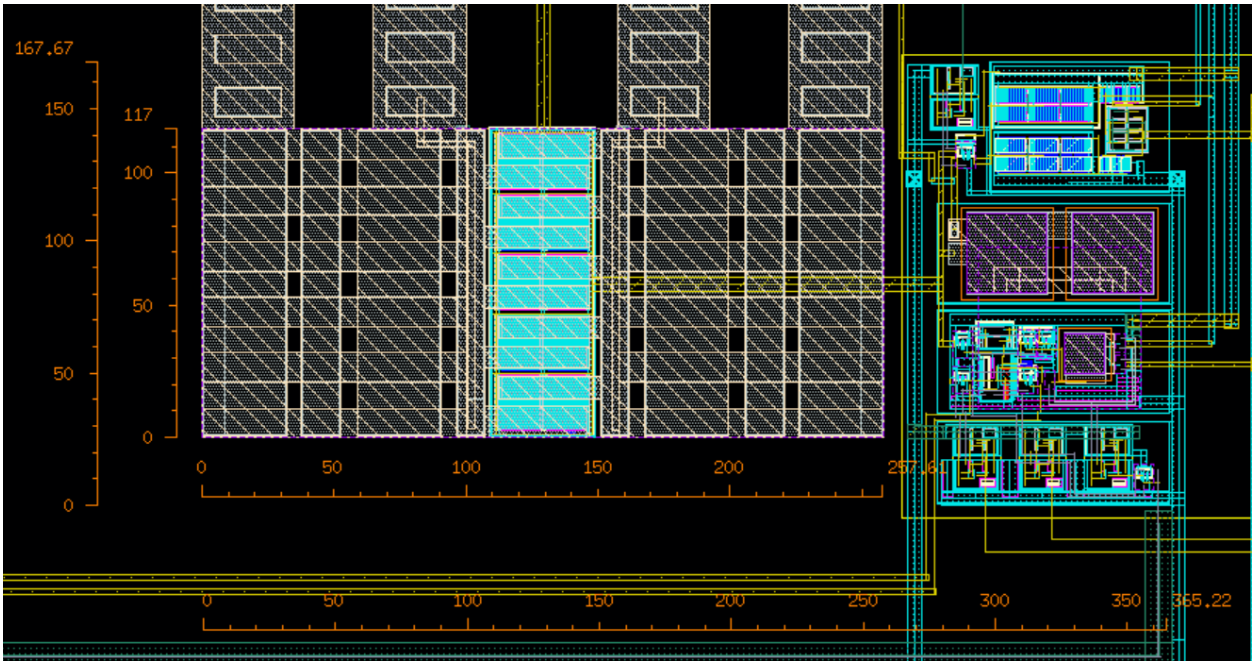


Figure 4.24: Cadence® layout of the implemented multi-loop LDO's 0.018 mm^2 with 0.03 mm^2 pass device array (0.048 mm^2 total active area)

Chapter 5

Evaluations & Results

As described in Section 4.3, the designed dual-loop LDO was physically implemented in a 180-nm standard silicon process. Essential simulation data verifying the design prior to fabrication is given in Section 4.2; however, a more robust catalog of figures and data is provided in Appendix E. The goals of the experimental evaluations are to obtain hardware validation of the LDO performance metrics previously defined in Figure 2.1 and compare these with those obtained in simulations. For each set of evaluations, the purpose of each evaluation is discussed, the experimental testing configurations are described, and the observations are summarized.

Five Teucer Chip samples were used for most of the experimental evaluations. For the evaluations of the Line-to-Load Regulation (Section 5.3.2) and Power Supply Rejection (Section 5.3.4), the experimental sample with the most consistently median performance across all other evaluations was the selected representative sample. This was Teucer Chip C.

5.1 Experimental Test Board

A printed circuit board (PCB) was designed to facilitate all the experimental evaluations. The Teucer Test Board is shown in Figure 5.1. Detailed design schematics, assembly drawings, and bill of materials for the test board are given in Appendix C. The test board allowed for thirteen independent power domains, and additional support for those

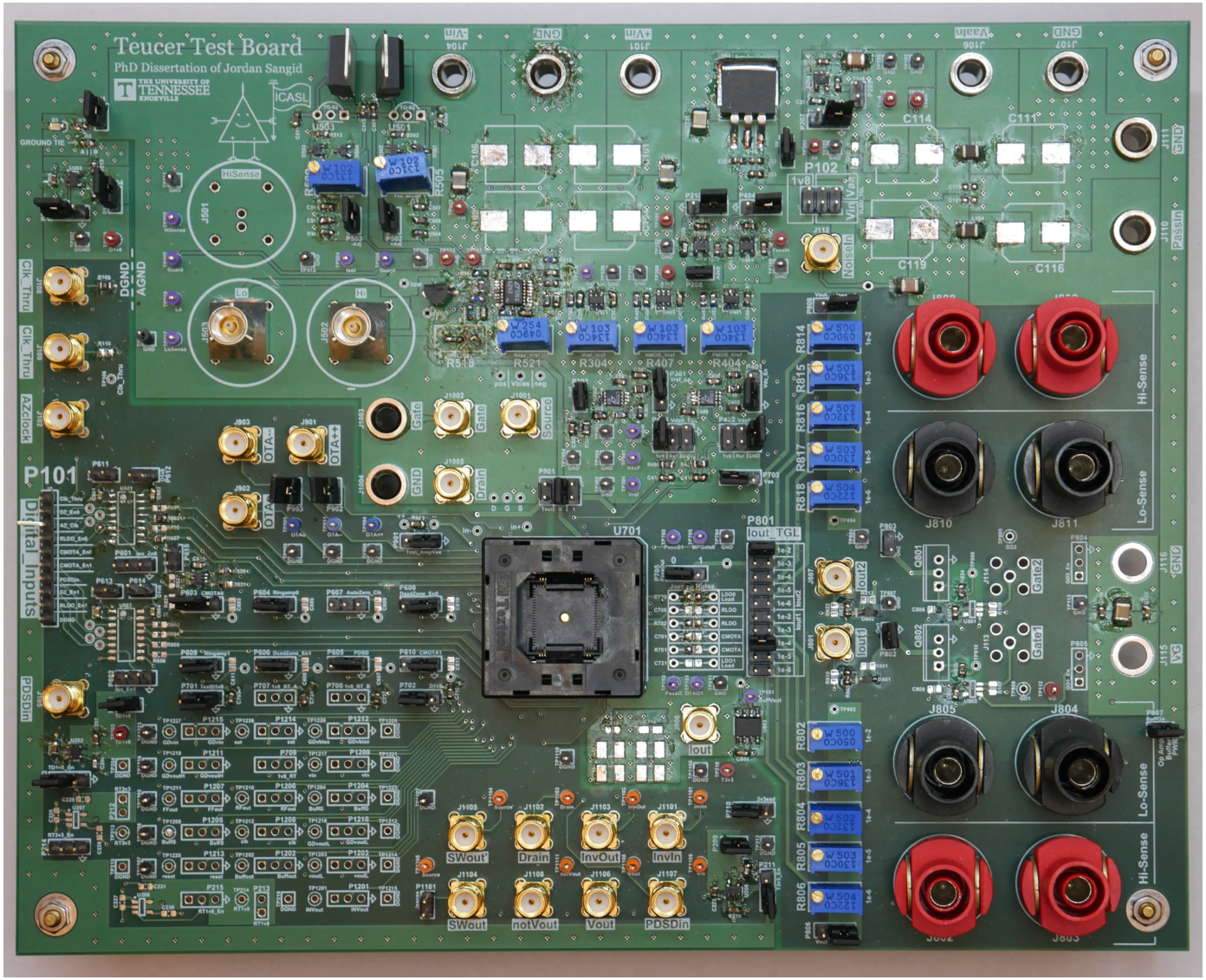


Figure 5.1: Teucer test board for experimental evaluations, 6-layer printed circuit board, and 80-pin quad-flat-pack chip socket for Teucer Chip

supplying evaluation critical on-chip circuitry so that continuous time monitoring of current consumption could be achieved. The test board input/outputs allowed for all control signals to be implemented with a lab bench computer and DAQ interface, with feed-through control paths for external triggering of testing equipment. This approach allowed for automated testing, ensuring consistent results, and limiting evaluation errors due to human error.

All digital control signals were buffered and level-shifted on-board, prior to interfacing with the Teucer Chip to restore fast signal edges and mitigate possible over-voltage exposure to the chip. Analog voltage references were provided by ultra-low noise precision regulators, further buffered, and filtered with low-noise precision amplifiers. All off-chip connections sensitive to loading conditions were buffered on-board before interfacing with the testing instrumentation, using precision operational amplifiers with ultra-low sub-10 pA input bias currents and a maximum of 1.5 pF of input capacitance. This minimized the capacitive loading of the OCL LDO to the on-chip routing/pad connections, in-package interface, and those of the PCB interface in combination with the 1.5 pF buffer amplifier input capacitance.

5.2 Experimental Sample Verification

Initial testing of the inverter and PDSD test cells were used to quickly verify the success of each fabricated sample. The digital test cells were not buffered on chip, but directly interfacing to the chip's padframe. This provided simulation design verification of transition points. The test setup for both the inverter and PDSD are shown in Figures 5.2 and 5.3, where a Function Generator (FG) was used to create a ramp or square wave with defined rise times and the resulting output waveforms were observed on the Oscilloscope (cataloged in Appendix F.1). An observed deviation from an ideal mid-rail switching point was due to parasitic elements within the padframe's ESD protection.

This preliminary evaluation demonstrated severe limitations of the supplied padframe's simulation models. Using the experimental test cell results and fine-tuning of the simulation models for the padframe and ESD protection, a best effort was made to account for all first order offsets including lumped parasitic elements during the evaluations. These updated models were then used for all the subsequent simulations necessary for post-fabrication

verification, with the most significant deviation from experimental results in experimental cases where high frequency content extends beyond the limited capabilities of the first order approximations. The experimental results often did not have a significant deviation across the five chips tested; thus, validating the results while highlighting the modelling inadequacies.

5.3 LDO Evaluations

The LDO systems were evaluated using the test configuration in Figure 5.6. Digital configuration states were determined by computer scripts and implemented by the DAQ unit interfacing directly with the test board. A feed through global clock on the test board provided external triggers to the testing instrumentation to begin and end the testing waveforms and capture specific timed events with the oscilloscope.

5.3.1 Static Observations

As shown in Figure 5.6, two synchronized Function Generators were used to supply digital control pulses. For the RLDOE evaluations, the Auto-Zero Clock was implemented with one Function Generator (FG) capable of producing a 5 ns pulse with 3 ns rise and fall times. As discussed previously in Section 2.2.3, a narrower sampling phase (ϕ_S) can lead to output level offset or droop while the output is not being driven within the Auto-Zero Phase (ϕ_{AZ}). Experimental results demonstrated negligible dynamic output offsets for the RLDOE loop over the range of $T_{S,\text{min}} = 200\,\text{ns}$ to $T_{S,\text{max}} = 10\,\mu\text{s}$. This observation also extended to all dynamic loading conditions and is indicative of a very small, but experimentally unobservable ${}^{dQ}/_{dt}$ on C_{HOLD} at the input of the RLDOE. Further evidence to support this can be interpreted from the absence of droop and instantaneous resumption of regulation from the RLDOE's standby mode when the CMOTA-based loop maintains continuous engagement.

The power consumption of the RLDOE loop was monitored with a precision source measurement unit (SMU). To enable direct monitoring of the error amplifier's current draw, isolated power planes on the test board supported unique error amplifier supply rails on the Teucer Chip. During operation, the average power consumption across the experimental

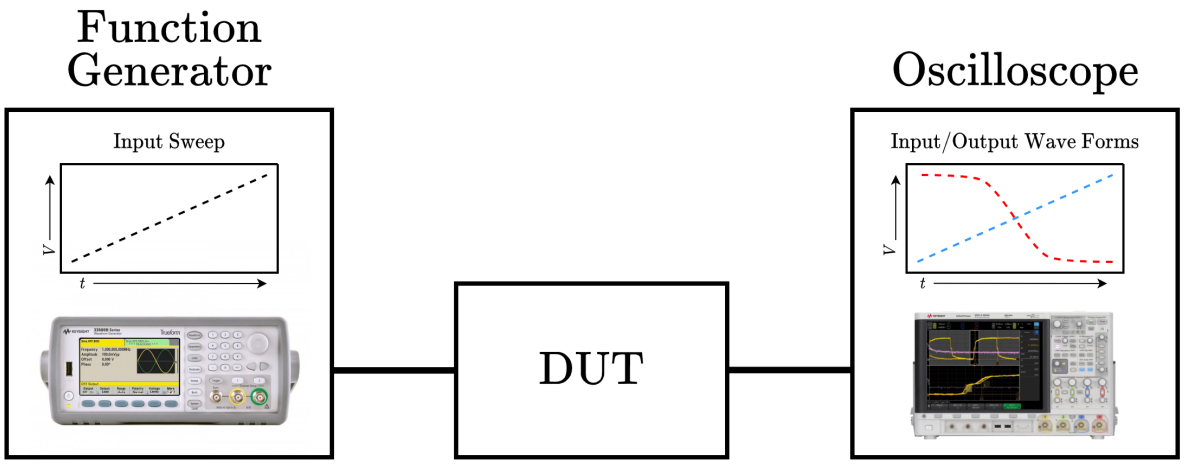


Figure 5.2: Experimental test configuration for unit inverter characterization

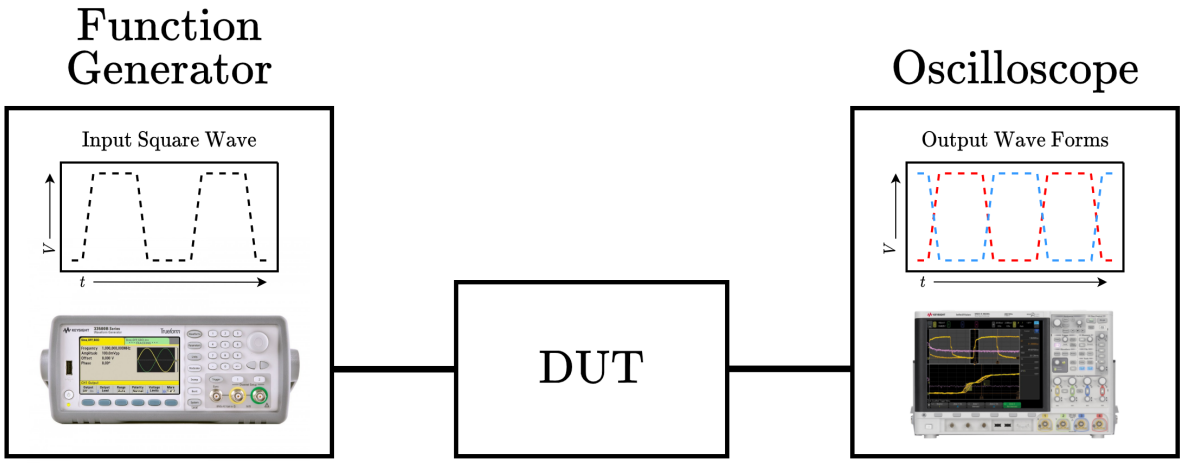


Figure 5.3: Experimental test configuration for Pseudo-Differential Switch Driver characterization

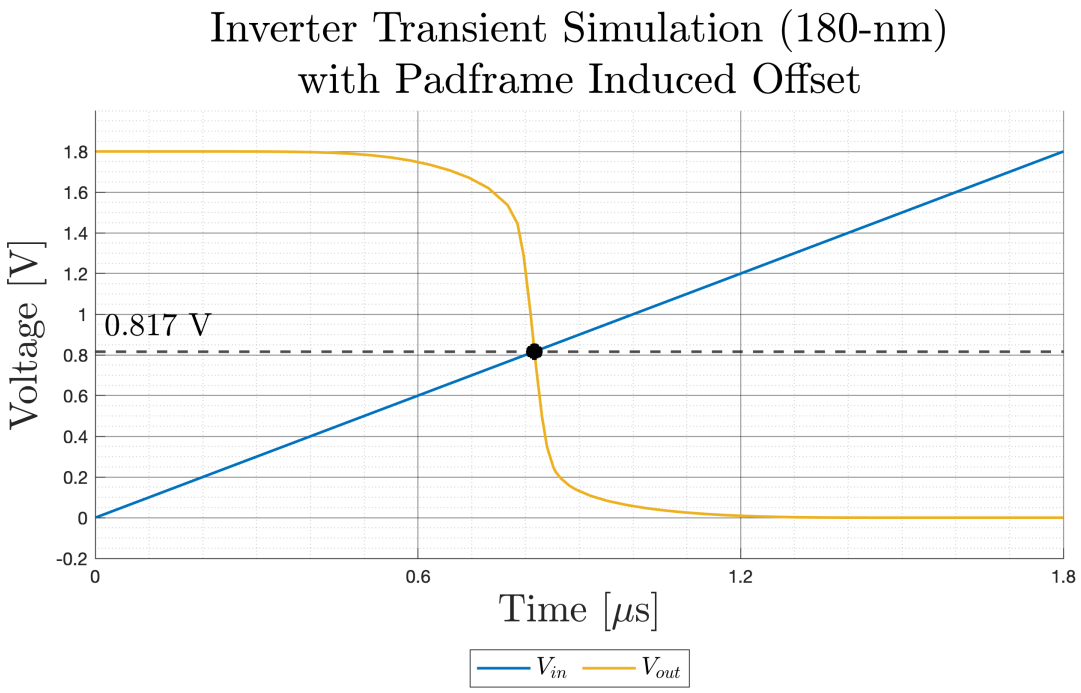


Figure 5.4: Simulated Teucer Chip inverter test cell transfer curves incorporating offsets due to the experimental testing configuration and interface parasitics

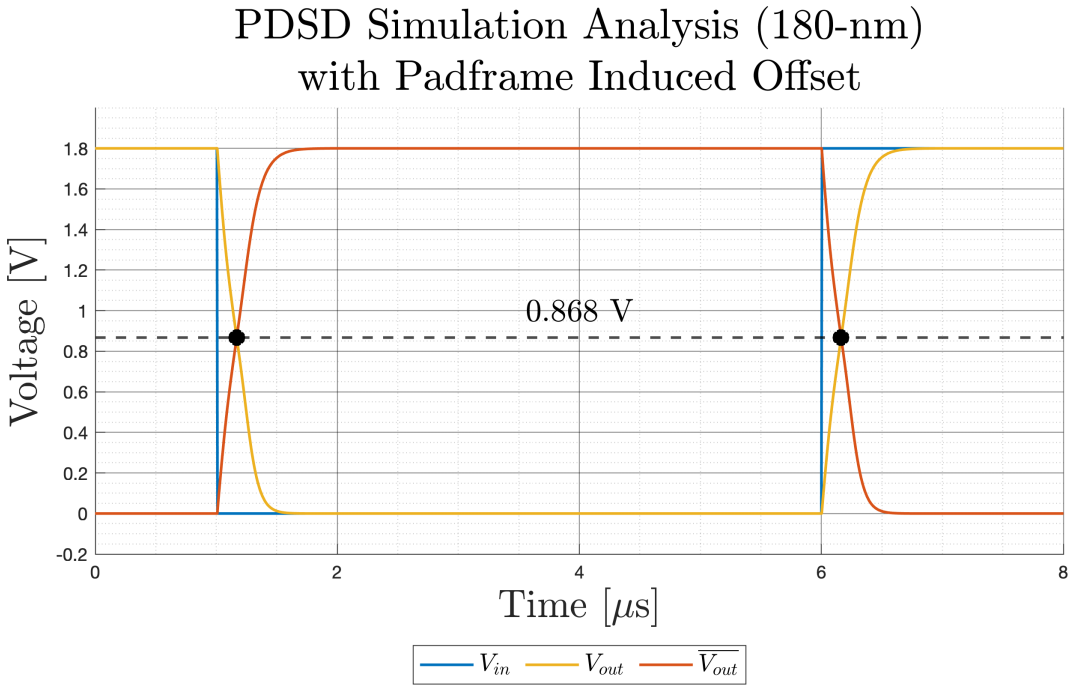


Figure 5.5: Simulated Teucer Chip Pseudo-Differential Switch Driver test cell transition waveforms incorporating offsets due to the experimental testing configuration and interface parasitics

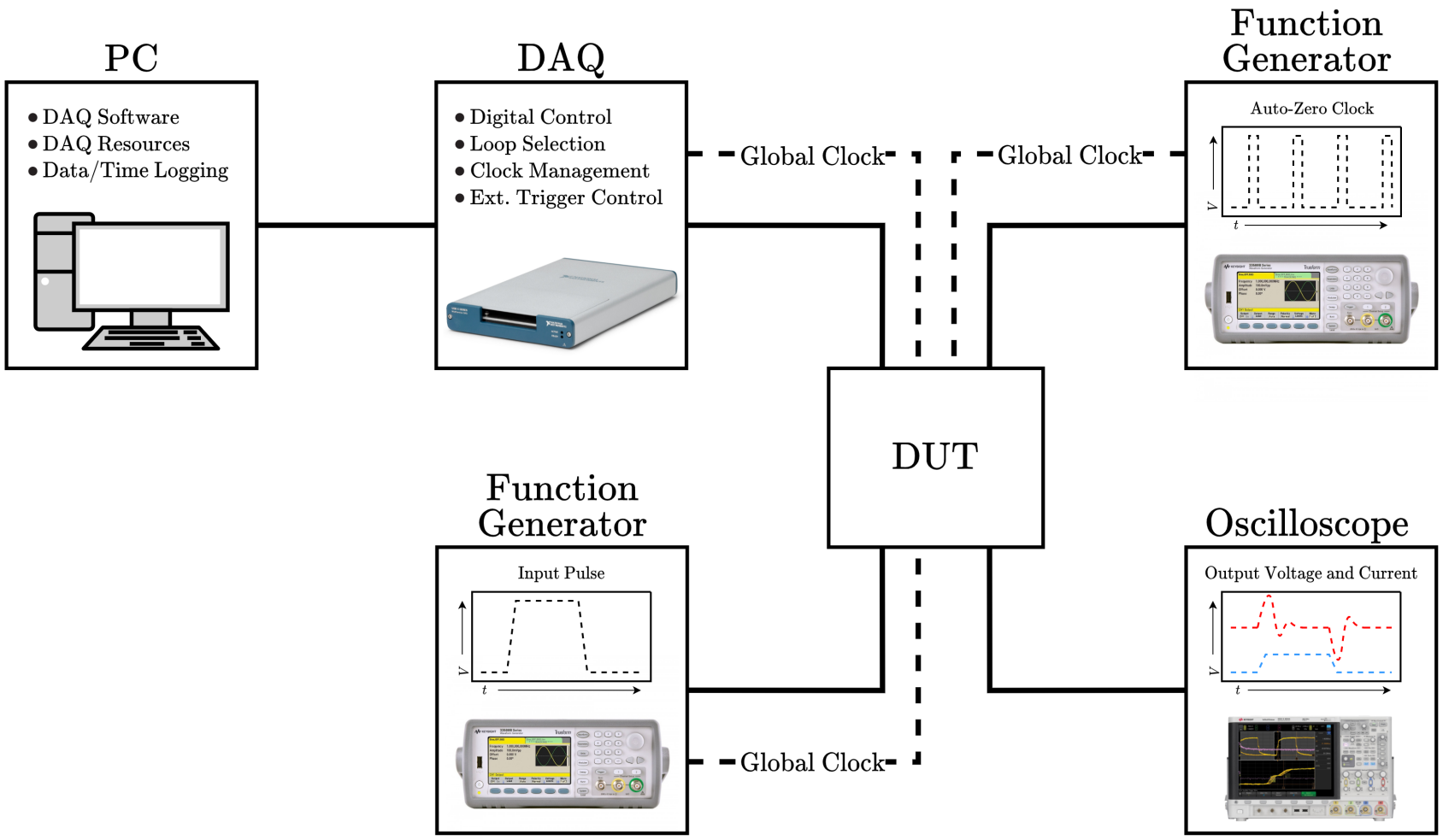


Figure 5.6: Experimental test configuration for transient current load step response evaluation

samples was 72.7 µA. While the RLDOE was in standby mode the static I_Q of the CMOTA loop became dominant masking any direct observations of the RLDOE's standby I_Q. In simulations, the RLDOE standby I_Q was shown to be 680 pA.

The CMOTA loop was biased off-chip by the test board's Nanoampere Current Source shown in Figure C.6, used previously in the work of Niemelä [72]. The current source was tuned to achieve a constant current sink of 25 nA. Using the same method described previously for monitoring the RLDOE loop's I_Q, the CMOTA error amplifier's observed I_Q was an average of 354 nA across all the experimental samples. This value also includes the 25 nA of current sinking off-chip.

5.3.2 Line-to-Load Regulation

The line-to-load evaluation determines the minimum achievable dropout voltage (V_{DO}) and characterizes the boundaries of large signal operation of the LDO. This is done by monitoring the LDO's load voltage (V_{OUT}) regulation with large signal changes in line voltage V_{IN}. Ideally when V_{IN} changes, V_{OUT} should continue to be constant. However, as the headroom of the error amp changes, so too does the loop gain. As V_{IN} approaches the value of V_{OUT}, or vice versa, the loop gain decreases by the effect of gain compression. The region of operation where gain compression begins, denotes the dropout region of the voltage regulator and non-linear regulation begins. A DC V_{IN} sweep was performed for a constant regulated voltage (V_{REG}) over the entire range of regulation with $I_{LOAD} = 100$ mA for both the RLDOE and CMOTA loops (shown in Figures 5.7 and 5.8). The minimum dropout voltage of the regulator at maximum output current was evaluated to be 100 mV. In these figures, the boundary of the dropout region exists, at the knee of the curve (positive of peak magnitude of $^{\Delta V_{OUT}}/_{\Delta V_{IN}}$ on each data series)

5.3.3 Transient Current Load Step

The current load step evaluations demonstrate the ability of the LDO to quickly adjust to dynamic loading conditions. The performance is dictated by the LDO's bandwidth, slew rate, error amplifier's dynamic range and drive strength, as well as the current capacity

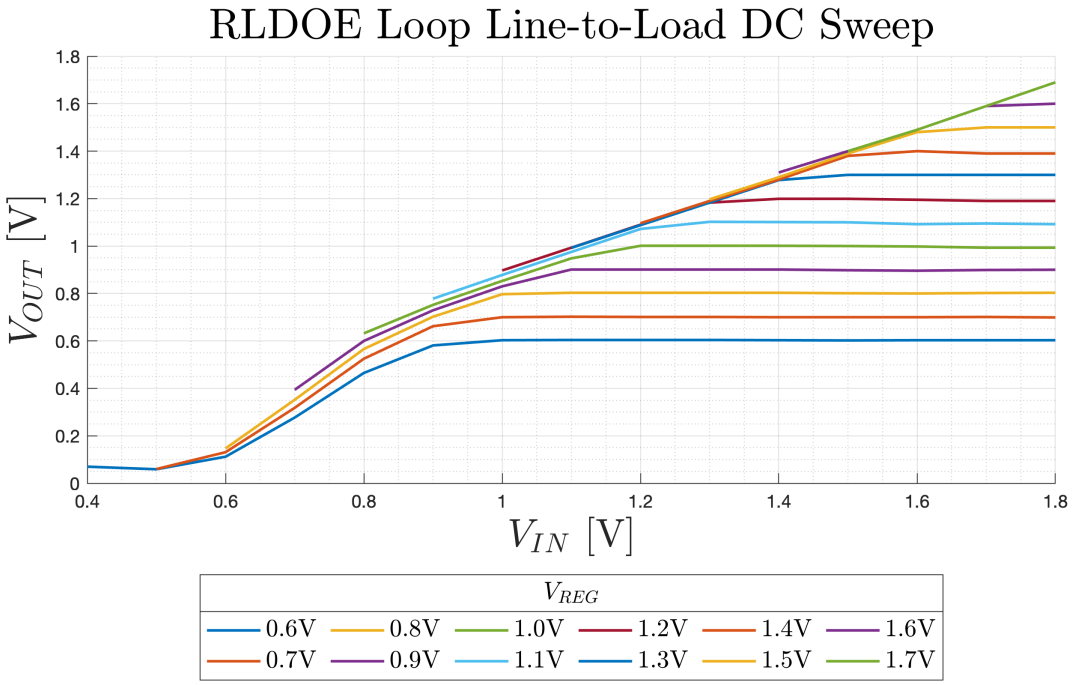


Figure 5.7: RLDOE loop experimental results of line-to-load regulation evaluation

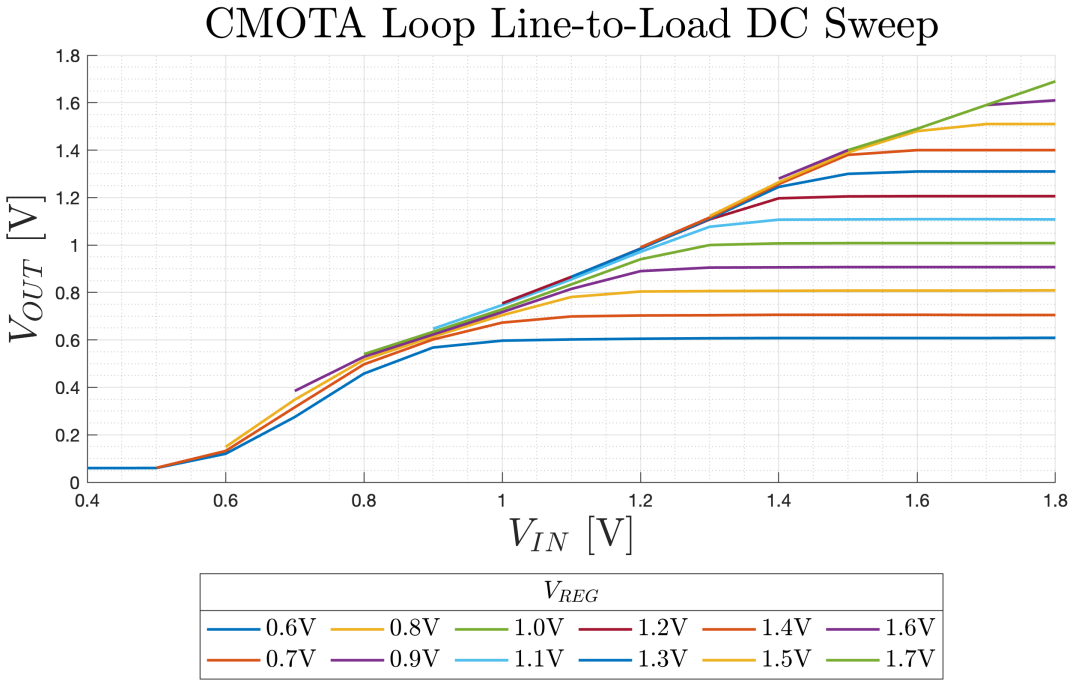


Figure 5.8: CMOTA loop experimental results of line-to-load regulation evaluation

of the pass device and the minimum dropout voltage (V_{DO}). The goal is to achieve a low overshoot or undershoot voltage (ΔV_{OUT}) and quickly settle to the regulated value. The rise and fall times of the current load pulse (t_{edge}) limit the minimum settling time of the response (T_{SETTLE}), but also can reduce the ΔV_{OUT} magnitude. A summary of the evaluations for this work are shown separately for the CMOTA loop in table 5.2 and the RLDOE loop in Table 5.1. Figures of the observed waveforms for each test case and their extracted data is given in Appendices F.2 and F.3

The test setup shown in Figure 5.6 provided the functionality of for the load step evaluations. The range and values of the load step was determined by the test board's current load step test circuit configuration, shown in Figure C.9. An array of 25-turn potentiometers allowed for fine tuning of the current values from 3.2 µA to 160 µA with an output voltage of $V_{OUT} = 1.6\,\text{V}$. Insulated banana jacks provided an interface for a precision SMU to fine tune the current levels prior to engagement of the on-chip LDO; but when not in tuning mode, the banana jacks could be configured to accept high input impedance testing probes and measure the voltage drop across a high precision 0.05 % 10 Ω resistor while the DUT was in operation to verify correct current load levels.

The test board allowed for two independent current values to be established. The baseline current was defined by connecting tuning resistor path to ground, the second level was controlled by a square wave from a Function Generator (FG), interfacing with SMA (SubMiniature version A) coaxial connector. A high speed Schottky diode would remain reversed biased and block any over-voltage from the FG but conduct current when the FG square wave bottomed at a common ground between the FG, the test circuit, and the LDO. The recovery and activation times of the Shottky diode as well as the capacitive loading and its potential to alter t_{edge} were considered; therefore, the diode was removed for the evaluations once proper test setup was achieved. Additional options for generating the current pulse were built into the test board with power MOSFETs and fast gate drivers, but the FG approach was preferable with the ability to quickly tune t_{edge} values across a wide range quickly and without adding passive components to create a time constant.

When conducting experimental verification of the dynamic voltage scaling (DVS) capabilities, the output current scaled with the output voltages. Only minor adjustments

Table 5.1: RLDOE-Loop Current Load Step Results

Evaluation	**Parameters**	**Unit**	**Simulated**		**Experimental**			
			Initial	PEX	Min.	Mean	Max.	$\sigma_{n=5}$
RLDOE Loop Set Up $V_{DD} = 1.8\,\mathrm{V}$	I_Q	[µA]	68.2		69.4	72.7	76	2.358
	I_{SYSTEM}	[µA]	-		1.501	1.512	1.524	0.009
RLDOE Loop Current Load Step 1 mA to 50 mA $V_{DD} = 1.8\,\mathrm{V}$ $V_{REF} = 1.6\,\mathrm{V}$ $t_{\Delta edge} = 15\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	201	203	190	194.0	200	5.477
	V_{OS}	[mV]	190	192	88	91.4	96	3.782
	$T_{OS,SETTLE}$	[ns]	10	10.3	183	236.6	268	32.090
	V_{US}	[mV]	231	241	108	113.0	117	3.937
	$T_{US,SETTLE}$	[ns]	10	11.6	54	55.4	58	1.673
RLDOE Loop Current Load Step 1 mA to 100 mA $V_{DD} = 1.8\,\mathrm{V}$ $V_{REF} = 1.6\,\mathrm{V}$ $t_{\Delta edge} = 15\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	202	203	190	196.0	200	5.477
	V_{OS}	[mV]	199	200	122	126.6	132	3.937
	$T_{OS,SETTLE}$	[ns]	13	14.3	145	277.4	426	113.582
	V_{US}	[mV]	350	362	139	146.6	152	4.827
	$T_{US,SETTLE}$	[ns]	13	16.1	51	71.8	132	34.091
RLDOE Loop Current Load Step 500 µA to 10 mA $V_{DD} = 0.9\,\mathrm{V}$ $V_{REF} = 0.7\,\mathrm{V}$ $t_{\Delta edge} = 15\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	110	114	98	103.8	107	3.834
	V_{OS}	[mV]	176	175	117	118.2	121	1.643
	$T_{OS,SETTLE}$	[ns]	21.7	38.1	656	806.0	970	119.908
	V_{US}	[mV]	208	205	174	181.0	187	5.477
	$T_{US,SETTLE}$	[ns]	40.4	51	260	336.6	452	75.132
RLDOE Loop Current Load Step 500 µA to 50 mA $V_{DD} = 0.9\,\mathrm{V}$ $V_{REF} = 0.7\,\mathrm{V}$ $t_{\Delta edge} = 15\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	110	119	100	104.8	108	3.633
	V_{OS}	[mV]	204	208	71	72.6	77	2.510
	$T_{OS,SETTLE}$	[ns]	42.8	59.2	209	285.0	374	65.977
	V_{US}	[mV]	322	318	75	77.4	81	2.510
	$T_{US,SETTLE}$	[ns]	57.2	81.2	164	250.6	330	67.726

Table 5.2: CMOTA-Loop Current Load Step Results

Evaluation	**Parameters**	**Unit**	**Simulated**		**Experimental**			
			Initial	PEX	Min.	Mean	Max.	$\sigma_{n=5}$
CMOTA Loop Set Up $V_{DD} = 1.8\,\text{V}$	I_Q	[µA]	0.380		0.352	0.354	0.355	0.001
	I_{SYSTEM}	[µA]	-		1.501	1.512	1.524	0.009
CMOTA Loop Current Load Step 100 µA to 1 mA $V_{DD} = 1.8\,\text{V}$ $V_{REF} = 1.6\,\text{V}$ $t_{\Delta edge} = 10\,\mu\text{s}$	$V_{DO(RMS)}$	[mV]	199	208	199	199.4	200	0.548
	V_{OS}	[mV]	94.8	97	85	98.2	108	8.438
	$T_{OS,SETTLE}$	[µs]	86	100	42.7	46.6	50.4	2.999
	V_{US}	[mV]	64.7	74.8	49	52.6	58	3.782
	$T_{US,SETTLE}$	[µs]	77	82	17.8	20.6	21.8	1.649
CMOTA Loop Current Load Step 1 mA to 10 mA $V_{DD} = 1.8\,\text{V}$ $V_{REF} = 1.6\,\text{V}$ $t_{\Delta edge} = 10\,\mu\text{s}$	$V_{DO(RMS)}$	[mV]	200	203	180	195.6	200	8.735
	V_{OS}	[mV]	126	128	84	105.6	115	12.896
	$T_{OS,SETTLE}$	[µs]	105	120	35.8	47.0	53.8	6.758
	V_{US}	[mV]	89.2	94	47	53.6	59	4.336
	$T_{US,SETTLE}$	[µs]	75	114	21.6	29.2	51	12.896
CMOTA Loop Current Load Step 1 mA to 100 mA $V_{DD} = 1.8\,\text{V}$ $V_{REF} = 1.6\,\text{V}$ $t_{\Delta edge} = 10\,\mu\text{s}$	$V_{DO(RMS)}$	[mV]	200	203	199	199.4	200	0.548
	V_{OS}	[mV]	183.7	185	149	157.6	167	6.986
	$T_{OS,SETTLE}$	[µs]	127	130	49	60.0	65.2	6.517
	V_{US}	[mV]	117	118	72	85.2	99	11.167
	$T_{US,SETTLE}$	[µs]	50	44.7	21	22.8	25.8	1.833
CMOTA Loop Current Load Step 40 µA to 4 mA $V_{DD} = 0.9\,\text{V}$ $V_{REF} = 0.6\,\text{V}$ $t_{\Delta edge} = 10\,\mu\text{s}$	$V_{DO(RMS)}$	[mV]	335	335	290	300.2	310	7.823
	V_{OS}	[mV]	160	164	37	40.8	45	3.768
	$T_{OS,SETTLE}$	[µs]	28.7	32.8	21.4	23.9	26	1.694
	V_{US}	[mV]	158	155	32	48.2	86	22.230
	$T_{US,SETTLE}$	[µs]	41.8	46.8	14.1	14.7	16.2	0.876
CMOTA Loop Current Load Step 400 µA to 40 mA $V_{DD} = 0.9\,\text{V}$ $V_{REF} = 0.6\,\text{V}$ $t_{\Delta edge} = 10\,\mu\text{s}$	$V_{DO(RMS)}$	[mV]	336	342	296	305.6	311	5.941
	V_{OS}	[mV]	216	223	23	27.8	34	4.087
	$T_{OS,SETTLE}$	[µs]	32.7	35.8	17.8	19.1	20	0.901
	V_{US}	[mV]	253	260	19	23.4	27	3.050
	$T_{US,SETTLE}$	[µs]	58.5	73.5	14	14.8	16	0.743

were needed when dropping V_{IN} from 1.8 V to 900 mV to scale to the current levels from 100 mA to 50 mA. This allowed for nearly direct scaling of LDO performance between the V_{IN} supply levels. Furthermore, for the evaluations other than those monitoring I_Q of the error amplifier, the pass device's V_{IN} and that of the error amplifier were tied together off-chip. So that, the DVS conditions were shared for all of the LDO circuits.

5.3.4 Power Supply Rejection

The power supply rejection (PSR) evaluations demonstrate the effectiveness of the LDO from preventing upstream V_{IN} noise or perturbations from passing through to the downstream load. There are multiple techniques to measuring PSR [73]; however, the selected approach is shown in Figure 5.10. This method injects a test tone into the V_{IN} power rail on the test board through a DC blocking capacitor (C_{ZDC}); but an AC blocking inductor (L_{ZAC}) must be used to prevent the test tone from being filtered by the source measurement unit or external power supply. The frequency of the test tone is incremented and the ripple on the output is observed. The evaluated PSR can then be determined by Equation (5.1).

$$PSR = 20 \log \left(\frac{v_{out-pp}}{v_{test-pp}} \right) \tag{5.1}$$

The primary limitation of this configuration is that the evaluation boundary is created by the critical resonant frequency (f_c) of the LC filter defined by Equation (5.2).

$$f_c = \frac{1}{2\pi\sqrt{L_{ZAC}C_{ZDC}}} \tag{5.2}$$

Any observable output ripple for test tone frequencies approaching f_c were too significantly attenuated to attain reliable measurement data; and for frequencies below f_c, measurements were not possible. For the experimental case during this evaluation, the data below 30 kHz was not usable. This limited any data for the PSR bandwidth of the weak-inversion CMOTA-based loop, considering a simulated PSR f_c below 1 kHz. Therefore, only the PSR for the RLDOE loop was attained and is shown in Figure 5.9. The maximum observed PSR

was $-43\,\mathrm{dB}$ and RLDOE loop's dominant pole was shown to be at approximately $300\,\mathrm{kHz}$; consistent with the simulated values in Section 4.2.3.

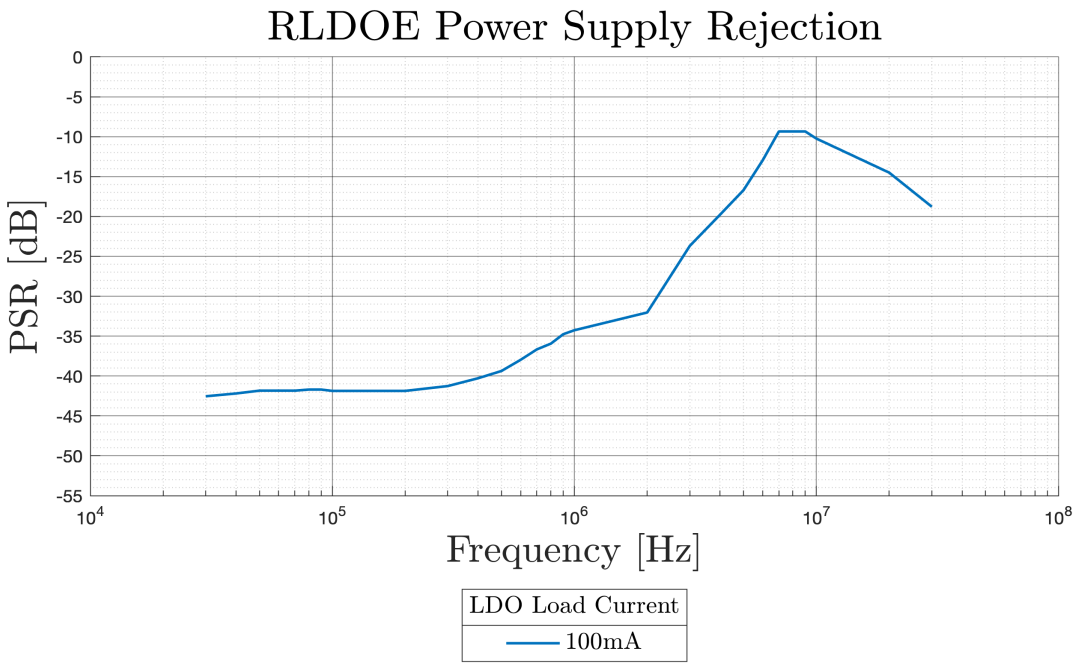


Figure 5.9: Experimental power supply rejection (PSR) performance of RLDOE Loop

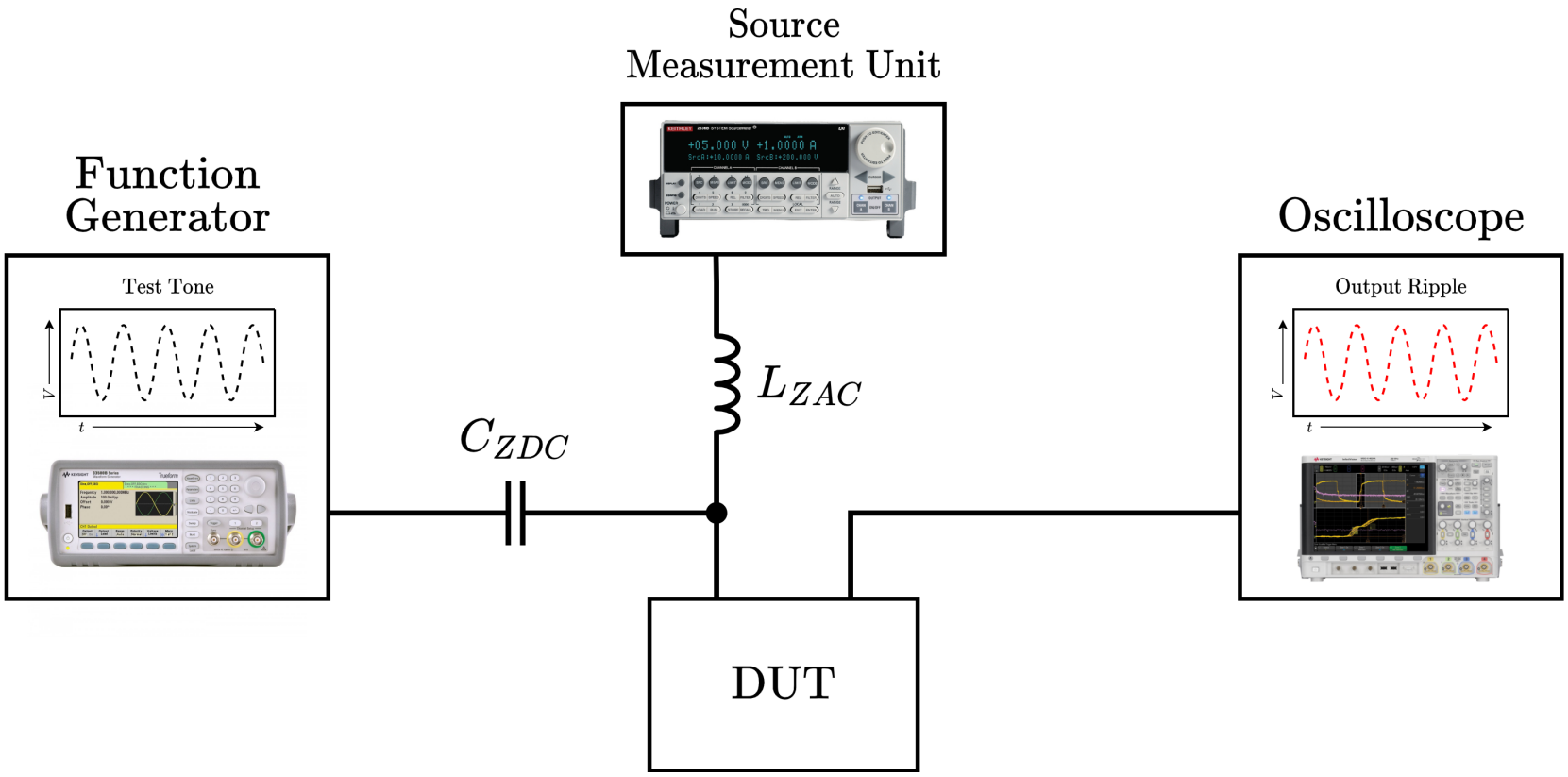


Figure 5.10: Experimental test configuration for power supply rejection (PSR) evaluations

Chapter 6

Case Study: A 65-nm Scaled RLDO

In addition to the fabricated implementation in the 180-nm process technology, a simulation-based version of the LDO was designed and implemented in a 65-nm process technology. The primary intent of this exercise was to validate the effectiveness of the contributed Ring Amplifier Design Guide and its supplemental materials within Chapter 3. A secondary intent of this technology node scaling case study was to provide simulation-based evidence to support the often-presumed inherent scalability of the Ring Amplifier. To achieve these targets, the RLDOE structure was scaled, leaping multiple generations of process technology, from a 180-nm to 65-nm standard silicon process.

6.1 Case Structure and Limitations

For the purposes of this case study, the action of direct scaling was limited to simply scaling the structures of an existing design from one process technology into another process technology. The Ring Amplifier has been presented as a scalable structure with analog behavior that could ease the burden of constantly addressing and readdressing scaling limitations of classic analog structures with each step into smaller process technology node sizes [4]. Therefore, the design handles of this case study were limited to only transistor sizing adjustments to showcase any qualitative scalability of the RLDOE. To directly illustrate any scaling disparity between the previously implemented error amplifiers, the CMOTA loop was also scaled in a similar method. Then to reduce masking of any potential shortcomings in

the frequency domain, the Split-Miller Compensation scheme was to be reduced to the bare minimum necessary to achieve quasi-stability across a similar output loading range of 100 µA to 100 mA to that of the physically implemented 180-nm Multi-Loop LDO.

6.2 Scaled Multi-Loop LDO Design & Results

The process of direct scaling of the RLDOE and CMOTA-based LDO loops is described in Sections 6.2.1 and 6.2.2. The RLDOE and CMOTA-based loops were both implemented with physical models within the 65-nm standard silicon process to include parasitic extraction data in all simulations for this case study. The layout cells are shown in Appendix D.2 and further simulation data and waveforms verifying the scaled design are given in Appendices E.3 to E.5.

6.2.1 Scaled RLDOE

Following the procedure of the Design Guide in Chapter 3, the minimum unit-sized PMOS and NMOS device models were characterized using IV sweeps for constant V_{GS} values. The data was exported and formatted into spreadsheets, then input into the *Optimum Inverter Design Script* given in Appendix B.1. A target I_Q of 12 µA was input into the script, resulting in calculated dimensions for the low-side NMOS and the scaling factor for the high-side PMOS. This 12 µA figure was determined by directly scaling the target I_Q of the original implementation by the ratio of minimum gate lengths between the two process technologies, determined in Equation (6.1).

$$I_Q = 35\,\mu\text{A}\left(\frac{60\,\text{nm}}{170\,\text{nm}}\right) \approx 12\,\mu\text{A} \tag{6.1}$$

To achieve direct scaling from the originally implemented 180-nm Multi-Loop LDO to the 65-nm variation, each cell and schematic was redrawn using the libraries and models provided by the 65-nm PDK. The calculated unit-sized inverters were adjusted for the new version, but the width scaling between RLDOE stages and the size of the width of the pass device were maintained between the variations. Demonstrating the success of the design assistance scripts

for this practical example, the suggested geometries of the RLDOE's first stage inverter's large-signal transfer curve is shown in Figure 6.1. The observable differences between this example and the previous version within the 180-nm process is the increase in inverter bandwidth and decrease in gain(shown in Figure 6.2 from a simulated $f_{-3\,\mathrm{dB}} \approx 250\,\mathrm{MHz}$ to $\approx 500\,\mathrm{MHz}$ and a decrease in A_{ol} from 28 dB to 24 dB.

The resulting simulated open loop transfer curve of the RLDOE loop is shown in Figure 6.3; similarly demonstrating an increase in loop bandwidth from the previous RLDOE's simulated $f_{-3\,\mathrm{dB}} \approx 20\,\mathrm{kHz}$ to $\approx 20\,\mathrm{MHz}$ and A_{ol} reduced from 55 dB to 40 dB while driving an output load current of 100 mA. These differences would translate to a decrease in necessary settling times to load current steps, but also decrease in accuracy due to an increase in finite amplifier gain error.

6.2.2 Scaled CMOTA-based LDO

The performance enhancements *versus* performance degradation of scaling analog structures into smaller process technologies were briefly hinted previously in Section 6.2.1. An increase in bandwidth mostly due to reduced gate area related capacitances and a decrease in gain due to reduced output resistances, are often the most attributed effects of process node scaling [5]. The simulated impact to the RLDOE structure can be qualitatively understood as a minor trade-off; however, this is not the case for the simulated scaled 65-nm CMOTA structure.

The CMOTA-based LDO loop was not able to directly scale between the process technologies to the same success as the RLDOE loop. The desired open loop gain required increasing the length of the output devices, increasing the effective output resistance (r_o); but, increasing the gate area introduced significant gate currents in the model simulations consistent with gate oxide tunneling current leakage in deep-submicron processes [74]. This gate current led to dynamic inter-stage voltage offsets dependent on the loading conditions of the amplifier, generating greater challenges to maintaining weak-inversion operation and an ultra-low current design.

The simulated 65-nm loop gain analysis of the CMOTA-based LDO loop is shown in Figure 6.4, showing a significant decrease in loop gain of 68 dB from the originally designed

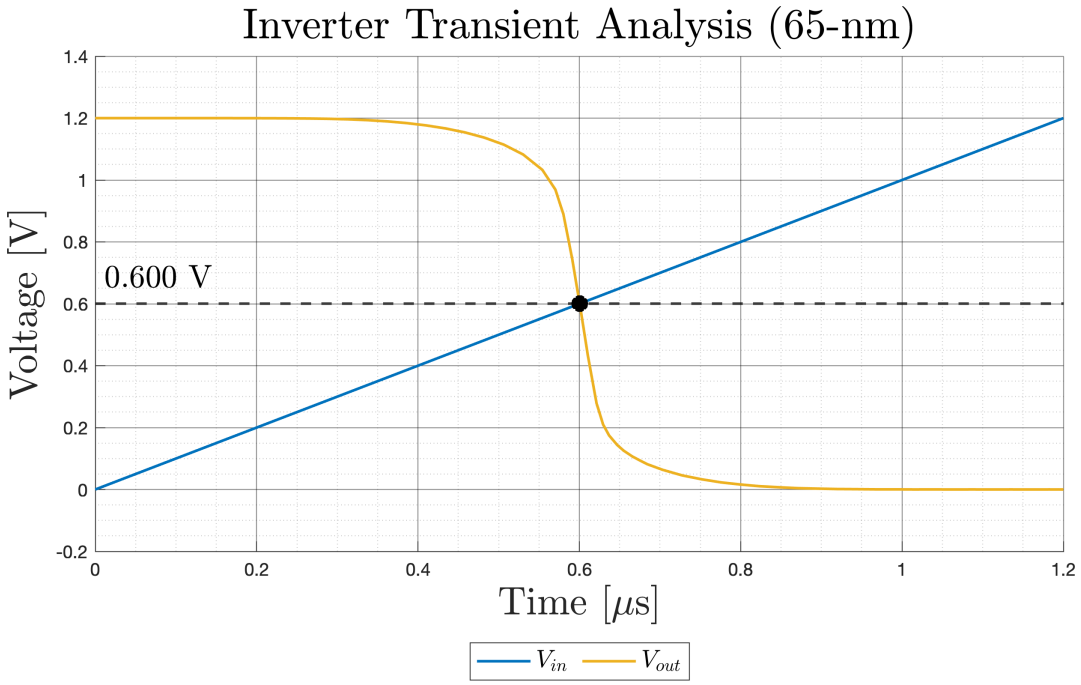


Figure 6.1: 65-nm simulated ringamp unit inverter transfer curve

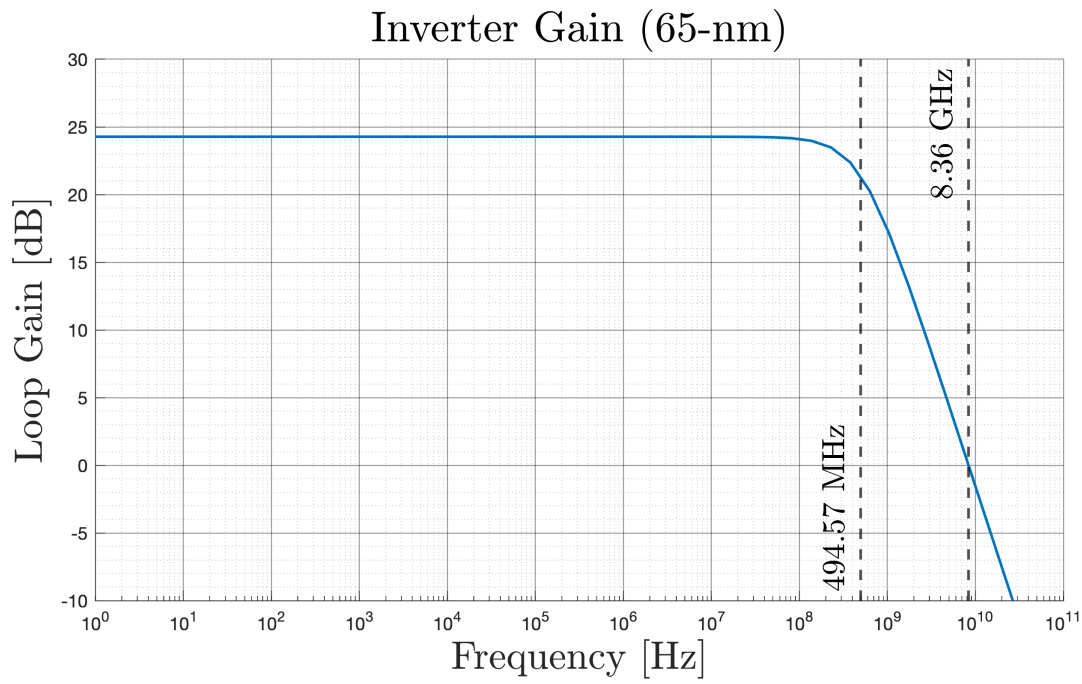


Figure 6.2: 65-nm simulated open-loop frequency response of the RLDOE loop's first stage inverter

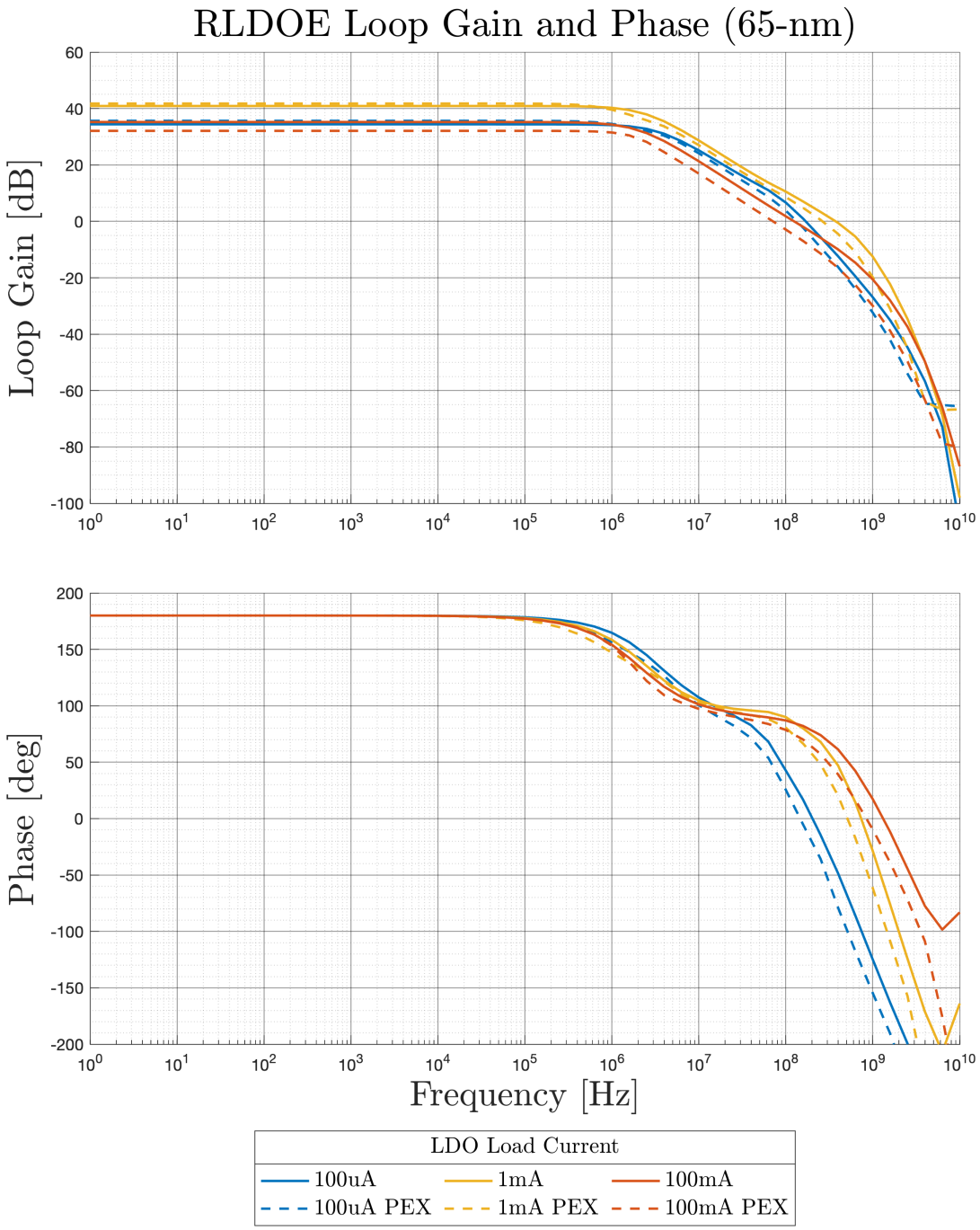


Figure 6.3: 65-nm simulated loop gain analysis of RLDOE loop with post-layout parasitic extraction (PEX)

180-nm simulations. These simulations also demonstrate a wide range in loop gain variation from LDO loading conditions from 25 dB when $I_{LOAD} = 1\,\text{mA}$ to $< 6\,\text{dB}$ when $I_{LOAD} = 100\,\text{A}$.

6.3 Case Study Conclusion

The results of the case study demonstrate a clear and direct scaling between the 180-nm process to the 65-nm for the RLDOE loop. This is not the case for the CMOTA-based LDO loop whose performance suffered considerable scaling related performance degradation. For this specific case study, the scalability of the Ring Amplifier can be clearly seen in contrast with the scaling inability of the CMOTA structure. But for the Multi-Loop LDO application, because the CMOTA-based loop is only responsible for maintaining steady-state conditions and subtle output loading variations, the evaluated performance of the Multi-loop LDO is not as significantly impacted by the CMOTA's inability to directly scale.

The performance summary of this simulated case study is compared to the summary of simulated results from the originally designed 180-nm Multi-Loop LDO in Table 6.1. There are some noticeable improvements possessed by the 65-nm simulated LDO, a lower ΔV_{OUT} even with a much lower compensation capacitance C_{TOTAL}. And the higher loop bandwidth directly translates to higher PSR. A consideration for the suggested Future Work in the following Section 7.2 will be to thoroughly design a 65-nm version of this RLDOE and Multi-Loop LDO to fully explore the surface-level observations and qualitative understanding presented in this Case Study.

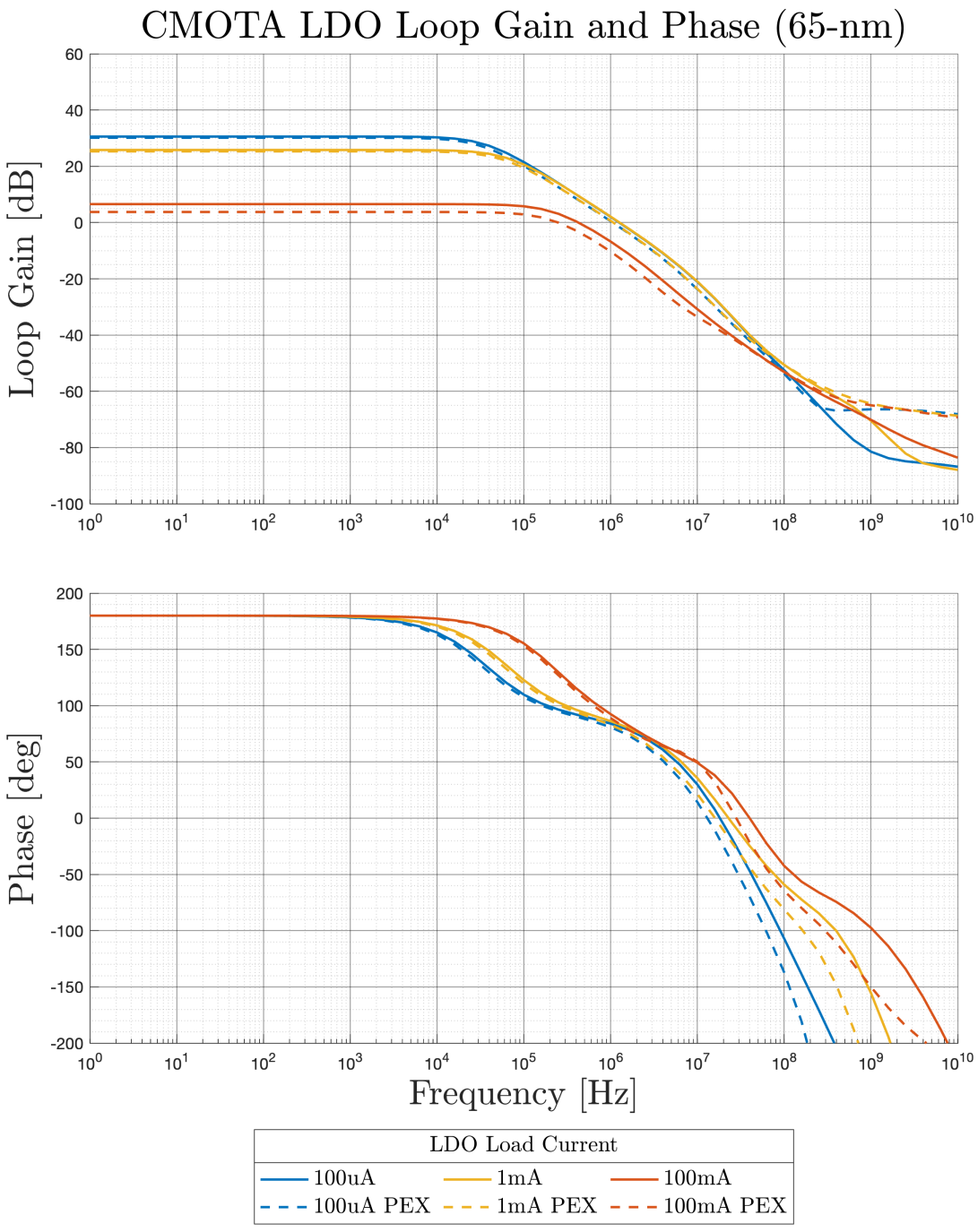


Figure 6.4: 65-nm simulated loop gain analysis of CMOTA-based LDO loop with post-layout parasitic extraction (PEX)

Table 6.1: Results of Scaled 65-nm LDO Compared to Original

Parameters	**Unit**	**Simulation**	
		180-nm	65-nm
$\mathbf{V_{IN}}$	[V]	0.9-1.8	0.6-1.2
$\mathbf{V_{OUT}}$	[V]	0.6-1.7	0.5-1.1
$\mathbf{I_{OUT}}$	[mA]	200	100
$\mathbf{I_Q}$	[µA]	0.380-68.2	0.894-36.4
$\mathbf{V_{DO}}$	[mV]	100	100
$\mathbf{C_{TOTAL}}$	[pF]	23.3	2
$\mathbf{\Delta t_{edge}}$	[ns]	15	15
$\mathbf{\Delta V_{OUT}}$	[mV]	240	110
$\mathbf{T_{SETTLE}}$	[ns]	16	35
PSR at 100 kHz	[dB]	30	42
$\mathbf{FOM_1}$ *	[fs]	0.0531	0.0197
$\mathbf{FOM_2}$ †	[V]	0.00684	0.0148

$$* \; FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right) \text{ [14]}$$

$$\dagger \; FOM_2 = \left(\frac{\Delta t_{edge}}{1\text{ ps}}\right)\left(\frac{\Delta V_{OUT} \cdot I_Q}{I_{O,MAX}}\right) \text{ [15]}$$

Chapter 7

Conclusions

This work has demonstrated a novel Low-Dropout Voltage Regulator approach to address a continued growth of demands for scalable fine-grain power management in System on Chip applications. The presented state-of-the-art Ringamp-Assisted Multi-Loop Analog LDO with Output Capacitor-less Split-Miller Compensation provides higher precision, higher power supply rejection, and higher current efficiency than contemporary digital-based LDO regulators; but also, provides greater dynamic voltage scaling and process node scaling capabilities than contemporary analog-based LDO regulators. To compound successfully bridging a gap between Analog and Digital LDO performance, the presented state-of-the-art work demonstrated a significant advancement to the prior art for Ringamp-based LDO regulators, elevating the RLDO topology to a much more competitive status among leading contemporary LDOs.

Further contributions include a Ring Amplifier design guide for general on-demand, scalable analog purposes that is coupled with script-based design tools to increase the effort efficiency of the design-to-implementation process. Then, by presenting the scaled Ring Amplifier case study to validate the effectiveness of the contributed design methodology, this becomes the first known work to demonstrate simulation-based evidence supporting the capability for a Ring Amplifier structure along with its behavior to directly scale between multiple generations of process technology. Thus, these efforts have widened the doors to a greater range of Ring Amplifier applications, creating countless avenues for future designers to contribute *their own* advancements within *their own* spheres of microelectronics.

7.1 Comparison to Prior Art

The presented state-of-the-art Multi-Loop Analog LDO, through experimental evaluations, met or vastly exceeded the target design specifications previously discussed in Section 4.1. These achievements have catapulted this work vastly beyond the performance of all previously published Ringamp-based LDOs (RLDOs), but also positioned this work in competition with other leading state-of-the-art examples along the performance edge for all evaluated LDOs as shown in Figure 7.1. The specific performance metrics extrapolated from the experimental evaluations are compared to the previous RLDO examples in Table 7.1 and all other reviewed leading state-of-the-art examples in Table 7.2.

7.2 Proposed Future Work

There exists several possibilities for continuation of the presented work. Perhaps, the most accessible would be to complete the 65-nm implementation simulated for the scaling case study in Chapter 6. For this task, if the steady-state control loop's error amplifier's I_Q could be reduced below 500 nA, there is potential for improved FOM performances and an additional leading state-of-the-art LDO implementation.

An alternate control approach briefly examined in simulations, but unable to be fully realized experimentally is a sample-and-hold LDO concept. The RLDOE in standby mode has negligible leakage through the anti-parallel floating battery structure within the second stage; thus, it could be designed to remove all other paths for the gate capacitance of M_{PASS} to be discharged if the RLDOE is disabled. This charge would stay on the gate and leave the pass device on and conducting. Then the RLDOE could be enabled in response to any changes required by the LDO and then resume standby operation, consider it as event-driven regulation. By leaving the LDO control loop unregulated except when necessary, the PSR would be negligible since the V_{GS} of M_{PASS} would behave as a floating battery. However, the effective quiescent current draw of this sample-and-hold LDO could be as low as the simulated standby I_Q of 680 pA of the RLDOE loop in standby mode. Potentially, a new

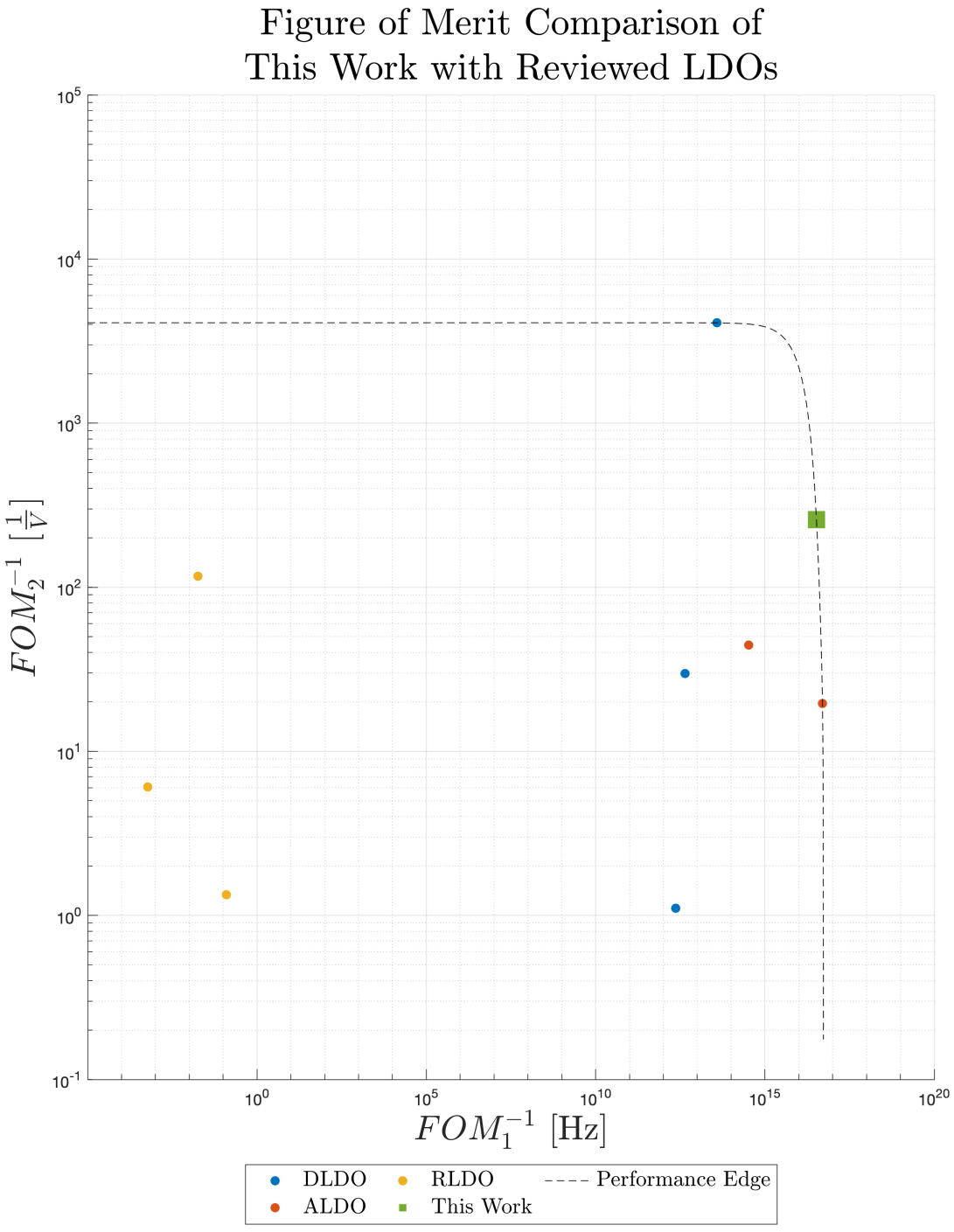


Figure 7.1: This work's results compared to those of recently published and reviewed in this dissertation

Table 7.1: Target Design Objectives Compared to Previous Ringamp-based LDOs

Parameters	**Unit**	**Yang and Mok [11]**	**Xiao *et al.* [12]**	**Park *et al.* [13]**	**This Work**
Year		2017	2019	2020	2022
Technology	[nm]	65	180	40	180
$\mathbf{V_{IN}}$	[V]	0.2-0.6	1.08-1.65	0.4-1.2	0.9-1.8
$\mathbf{V_{OUT}}$	[V]	0.05-0.55	1	0.2-1.18	0.6-1.7
$\mathbf{I_{OUT}}$	[mA]	0.1-50	40	400	200
$\mathbf{I_Q}$	[µA]	0.41-32	6.5	4.4-1280	0.354-72
$\mathbf{V_{DO}}$	[mV]	20	90	50	100
$\mathbf{C_{TOTAL}}$	[pF]	40	50	90	23.3
$\mathbf{\Delta t_{edge}}$	[ns]	10,000-150	100	10	15
$\mathbf{\Delta V_{OUT}}$	[mV]	133.9	46-163	78-45	146
$\mathbf{T_{SETTLE}}$	[ns]		234-700	500-25	125
PSR at 100 kHz	[dB]	20	~ 18	~ 30	42
$\mathbf{FOM_1}$ *	[fs]	228,300-1700	1505-8	28,600-55	0.0301
$\mathbf{FOM_2}$ †	[V]	0.165	0.748	0.00858	0.00388
Active Area	[mm^2]	1.379	0.1	0.12	0.068

* $FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right)$ [14] † $FOM_2 = \left(\frac{\Delta t_{edge}}{1\text{ ps}}\right)\left(\frac{\Delta V_{OUT} \cdot I_Q}{I_{O,MAX}}\right)$ [15]

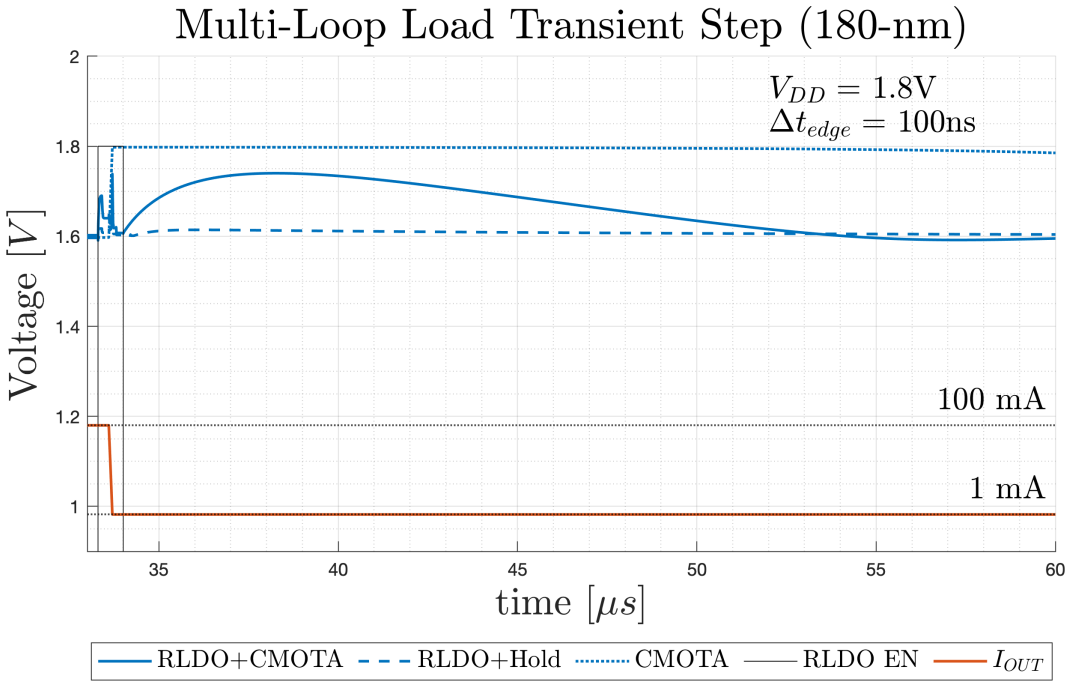


Figure 7.2: Multi-Loop LDO transient waveforms demonstrating multiple control approaches

Table 7.2: Target Design Objectives Compared to Recent State-of-the-Art LDOs

Parameters	**Unit**	**Huang *et al.*** [39]	**Huang *et al.*** [40]	**Ma *et al.*** [41]	**Zhao *et al.*** [42]	**Han and Lee** [43]	**This Work**
Year		2016	2018	2020	2021	2021	2022
Technology	[nm]	65	65	28	65	180	180
Control		DLDO w/ Coarse-Fine-Tuning and Burst-Mode	Tri-Loop DLDO w/ Analog Assist	DLDO w/ NAND-based Analog Assist	Current-Controlled Oscillator	Active Capacitor	Analog Multi-loop w/ RLDOE
$\mathbf{V_{IN}}$	[V]	0.6-1.1	0.5-1	0.4-0.55	0.5-1.2	1.2-1.4	0.9-1.8
$\mathbf{V_{OUT}}$	[V]	0.4-1	0.45-0.95	0.35-0.5	0.45-1.15	1.0-1.2	0.6-1.7
$\mathbf{I_{OUT}}$	[mA]	100	10	40	50	80	200
$\mathbf{I_Q}$	[µA]	82	3.2	0.85	0.31-0.5	0.34	0.354-72
$\mathbf{V_{DO}}$	[mV]	100	50	50	50	200	100
$\mathbf{C_{TOTAL}}$	[pF]	1000	100	59	15	3	23.3
$\mathbf{\Delta t_{edge}}$	[ns]	20	1	0.1	15	100	15
$\mathbf{\Delta V_{OUT}}$	[mV]	55	105	113	150	120	146
$\mathbf{T_{SETTLE}}$	[ns]	700			300	110	125
PSR at 100 kHz	[dB]			~ 2		34	42
$\mathbf{FOM_1}$ *	[fs]	430	230	26	3	0.02	0.0301
$\mathbf{FOM_2}$ †	[V]	0.902	0.0336	0.00024	0.0225	0.051	0.00388
Active Area	[mm^2]	0.01	0.034	0.0134	0.118	0.04	0.068

* $FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right)$ [14]

† $FOM_2 = \left(\frac{\Delta t_{edge}}{1\,\text{ps}}\right)\left(\frac{\Delta V_{OUT} \cdot I_Q}{I_{O,MAX}}\right)$ [15]

class of sub-nanoampere quiescent current LDOs. The waveforms for multiple simulated control schemes is shown in Figure 7.2 including the sample-hand-hold LDO approach.

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Appendices

A Nyquist-rate Analog-to-Digital Converters

The three most widely used Nyquist-rate ADC topologies consist of Flash, Pipelined, and Successive Approximation Register (SAR). The flash ADC or parallel ADC consists of a stack of comparators with resistive voltage dividers and is typically the most basic and easiest to understand. In most cases flash ADCs are limited to 8 b and not capable of high-resolution data conversion [75].

In principle, both pipelined and SAR ADCs operate the same way, with a binary search of values. These ADCs determine a binary guess of the analog input value and then converge to a solution through successive estimations, where the theoretical accuracy of the converged solution and resolution of approximation is determined by the number of iterations. During each successive estimation, the difference (known as "residue") between the n-th stage input and n-th stage guess is processed in a similar way as in the $(n-1)$-th stage. The processing iterations continue until the ADC converges upon a solution with a predetermined resolution [75].

A.1 ADC Metrics and Figures of Merit

There are two widely accepted figures of merit (FOMs) for ADCs: the Schreier FOM and the Walden FOM given in equation (A.1).

$$FOM_W = \frac{P}{2^{ENOB} + f_s} \tag{A.1}$$

where P is power dissipated, f_s is sampling frequency, and $ENOB$ is given in equation (A.2).

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{A.2}$$

$SNDR$ is signal to noise and distortion ratio and should not be confused with $SFDR$ which is the spurious free dynamic range.

A.2 The Pipelined ADC

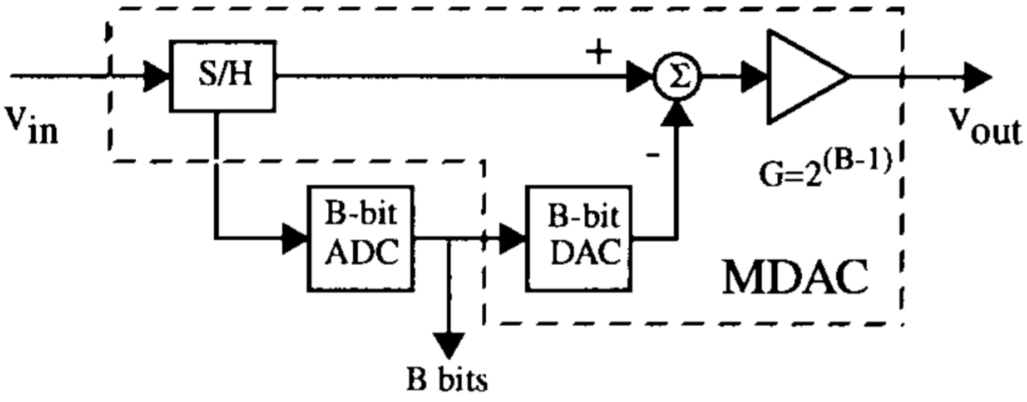
Pipelining incorporates multiple cascades of 1 b, 1.5 b, sometimes 3 b or higher processing stages [75]. Within each processing stage is at minimum one residue amplifier, and more stages are needed for higher resolutions. The amplifier is often used within a multiplying digital-to-analog converter (MDAC) switched-capacitor structure. The MDAC serves multiple functions based on the conduction phase of the switched-capacitors.

A block diagram of a basic single stage pipelined ADC is given for example in Figure A.1a [76]. In this basic pipeline stage, the MDAC functions as each element except for the sub-ADC. The MDAC initially behaves as a sample and hold (S/H), then subtracts the stored guess value from the S/H to generate sample residue, and finally amplifies the residue for processing in the subsequent cascaded pipeline stage [76]. Each of these functions is determined by the phase of the switched-capacitors. A full implementation of a pipelined ADC will cascade multiple stages, where the amplified residue from one stage is the input of the following stage.

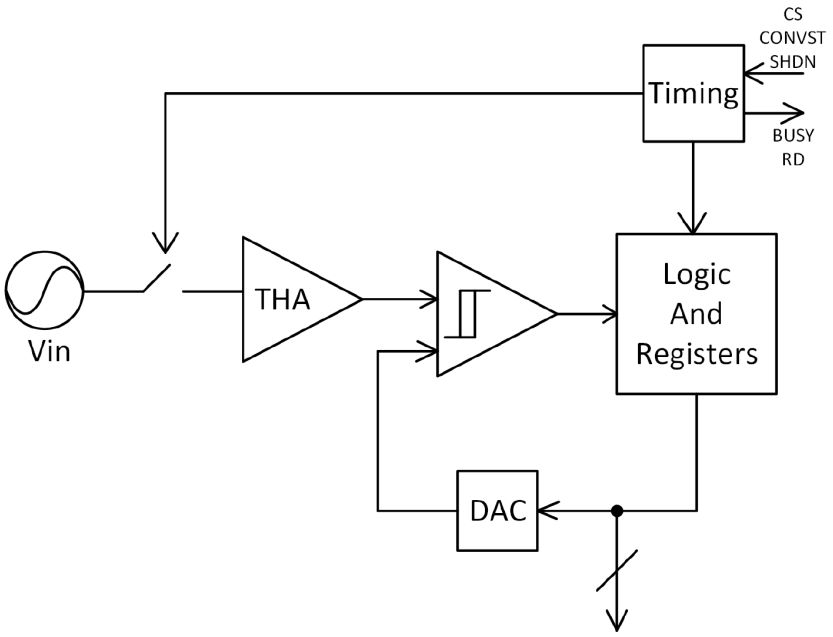
The overall performance of the pipelined ADC is inherently dependent on that of the internal amplifiers. The performance metrics or resulting FOMs of any given pipelined ADC are often simply the limitations of these internal amplifiers. The challenges with technology and voltage scaling of these analog amplifiers have then led to a rise in popularity of the amplifier-less SAR-based architectures [4, 75].

A.3 The SAR ADC

The initial concepts behind a SAR ADCs have been in circulation since the 1940s and 1950s; however, this topology was relatively uncommon until their potential for improved high-conversion efficiency was observed in the early 2000s [75]. The fundamental difference in processing operation between the pipelined and SAR architectures is that where a pipeline successively processes the residue of each iteration to a cascaded stage, the SAR loops the residue around a single stage, storing the estimated value of each iteration on to a register while the input to the system is frozen [75]. A typical block diagram of a SAR ADC stage is shown in Figure A.1b [77].



(a)



(b)

Figure A.1: Block diagrams of (a) single stage pipelined [76] and (b) SAR ADC [77]

Since the SAR relies on a single stage, processing must occur over multiple clock cycles demonstrating a major trade-off between speed and resolution. Another disadvantage of the SAR topology is that the sub-DAC requires high accuracy and thus many capacitors in a capacitor-based DAC or CDAC (2048 capacitors to be exact for a 10 b fully differential system [75]). The pipelined ADC, in contrast, requires a minimum of 2 capacitors per stage. Therefore, the SAR ADC has a fundamental need for large area; especially if capacitors are sized to reduce kT/C noise [75].

To compensate for these disadvantages, often multiple SAR stages are cascaded. This reduces the total die area, while improving the resolution. This approach includes N-step SAR (where N is the number of SAR stages cascaded) and SAR-assisted pipeline architectures. In these ADCs, an analog residue amplifier can be used between the stages to further enhance the overall resolution of the ADC; however, this addition inhibits the built-in scalability of the mostly digital SAR ADC. This trade-off between scalability and resolution has also become an opportunity for Ring Amplifiers.

B Source Code

These MATLAB® scripts and functions were used to assist in the design and implementation of the Ring Amplifier which was used as the core of the RLDO loop within this work.

B.1 Optimum Inverter Design Script

```
%%  Optimum Inverter Design Script
%   written by:  Jordan Sangid
%   Use NMOS and PMOS IV Curves to automate and
%       optimize inverter sizing

clear;
close all;

%   Create Directory for Generated Figures
Img_Directory = 'generated_figures_XLS';
Dir_Status = exist(Img_Directory,'dir');
if Dir_Status == 0
    mkdir(Img_Directory);
end

%   Delete previously saved results
%   This prevents appending to old results
if exist('optimum_inverter.csv', 'file')==2
  delete('optimum_inverter.csv');
end

%   Define size of figure to print
figSize=[600 500];

%%  USER INPUT  %%
%   Design Parameters
Vdd = 1.8;      % DC Supply Voltage
Vm = Vdd/2;     % Transition Voltage
IQ = 150e-6;    % Quiescent Current

%%  Extract Parameters
%   Import simulation results from XLS file
SpreadSheetN = xlsread('Example_Circuit.xlsx','NMOS');
SpreadSheetP = xlsread('Example_Circuit.xlsx','PMOS');
VdsN = SpreadSheetN(2:size(SpreadSheetN,1),1);
VdsP = SpreadSheetP(2:size(SpreadSheetP,1),1);
VgsN = SpreadSheetN(1,2:size(SpreadSheetN,2));
VgsP = SpreadSheetP(1,2:size(SpreadSheetP,2));
IdN = SpreadSheetN(2:size(SpreadSheetN,1),2:size(SpreadSheetN,2));
IdP = SpreadSheetP(2:size(SpreadSheetP,1),2:size(SpreadSheetP,2));

clear SpreadSheetN SpreadSheetP

%   USER INPUT values from IV curves
WN = 5e-6;
```

```
WP = 5e-6;
L = 1e-6;

%   Call the parameter extractor function
[KN_fit, lambdaN, VthN, nN] = ParamExtractorFunc(VgsN, VdsN, IdN);
[KP_fit, lambdaP, VthP, nP] = ParamExtractorFunc(VgsP, VdsP, IdP);

%  Calculate extracted transconductance coefficient for returned equations
KN = polyval(KN_fit,Vm);
kn = KN/(WN/L);
KP = polyval(KP_fit,Vm);
kp = KP/(WP/L);

%% Optimum Inverter Width Ratio
%   Cite: Digital Integrated Circuits. 2nd Ed. J. M. Rabaey
VdsatN = Vm-VthN;
VdsatP = Vdd - Vm - VthP;

%  Consider what is the optimum ratio of WP/WN for a range of Vgs values
WP_WN_Ratio = (kn*VdsatN*(Vm-VthN-VdsatN/2))/...
    (kp*VdsatP*(Vdd-Vm-VthP-VdsatP/2));

%% Inverter Gain Calculation
%   Assume DC voltage is the transition voltage Vm
%   Cite: Digital Integrated Circuits. 2nd Ed. J. M. Rabaey
syms WLN

%   Calculate Width to Length Ratio with respect to desired Quiescent
   Current
ID = IQ == WLN*kn*(Vm-VthN)^2*(1+lambdaN*Vm);
WLN = double(solve(ID,WLN));

%   Calculate gain of the inverter at Vin = Vm
Gain = abs(1/(IQ)*(kn*VdsatN + kp*VdsatP)/(lambdaN - lambdaP));
Gain_dB = 20*log10(Gain);

%% Organize results into a table and print to file
Values =     [  Vdd;
                IQ;
                VthN;
                VthP
                nN;
                nP;
                kn;
                kp;
                lambdaN;
                lambdaP;
                WP_WN_Ratio;
                WLN;
                Gain;
                Gain_dB ];

%   Write values to spreadsheet for other scritps to use
writematrix(Values,'optimum_inverter.csv');

T = array2table(Values,'RowName',{'Vdd','Id','VthN','VthP', ...
```

```
    'n_N','n_P','kn','kp', ...
    'lambdaN','lambdaP','WP_to_WN','W_to_L','Gain','Gain_dB'});

writematrix(Values,'optimum_inverter.xls');

%   Put Table into a Figure
figure()
hold on;
resultsTab = uitable('ColumnWidth',{100},...
        'Data',T{:,:},'ColumnName',T.Properties.VariableNames,...
        'RowName',T.Properties.RowNames,...
        'Units','Normalized','Position',[0 0 1 1]);
set(gcf,'Position',[100 100 figSize]);
print('generated_figures_XLS\InverterValues','-dpng','-r300');
hold off
```

B.2 Parameter Extractor Function

```
%%  Parameter Extractor Function
%   written by:  Jordan Sangid and Noah Archer
%   Extract Parameters from IV curve arrays

function [Kparam, lambda, Vthresh, n] = ParamExtractorFunc_XLS(Vgs, Vds, Id)
    %%  Threshold Voltage and Slope Factor Extraction
    %   This Extraction for Threshold Voltage must be done in Linear Region.
    %   Please see the Tsividis text book Indian 3rd Ed Figure 4.33 and
    %   surrounding text for explanation.  The extraction method for n, the
    %   weak inversion coefficient also comes from Tsividis around Figure
    %   4.31 in the Indian 3rd Ed
    Vth_Index = find(Vds <= max(Vds)*0.05,1,'last'); % ensure Vds<<(Vgs-Vt)
    Vth_Slope = diff(Id(Vth_Index,:)); % Find slope of Id vs. Vgs for line
       fit

    %   Find all index values for slopes within sensitivity threshold
    SensitivityThresh = 0.05;
    Vth_Slope_Underthreshold = find(abs(Vth_Slope-max(Vth_Slope))/...
        max(Vth_Slope) < SensitivityThresh);
    Vth_Line = polyfit(Vgs(Vth_Slope_Underthreshold),...
        Id(Vth_Index,Vth_Slope_Underthreshold),1);

    %   Tsividis says the x-intercept is equal to Vth + (alpha/2)*Vds
    %   let alpha = 1 for our purposes.
    Vth_Xint = -Vth_Line(2)/Vth_Line(1);
    Vthresh = Vth_Xint - Vds(Vth_Index)/2; % find x-intercept (0 = mx + b)

    %   log(Id) vs. Vgs for constant Vds
    SF_Index = find(Vds <= max(Vds)*0.5,1,'last');
    log_Id = log10(Id(SF_Index,:));
    SF_Slope = diff(log_Id); % Find slope of log(Id) vs. Vgs for line fit

    %   Find all index values for slopes within sensitivity threshold
    SensitivityThresh = 0.25;
    SF_Slope_Underthreshold = find(abs(SF_Slope-max(SF_Slope))/...
        max(SF_Slope) < SensitivityThresh);
    SF_Line = polyfit(Vgs(SF_Slope_Underthreshold),...
        log_Id(SF_Slope_Underthreshold),1);
    n = abs(1/(SF_Line(2)* log(10) * 0.0259));

    %%  Channel Length Modulation and Transconductance Parameter Extraction
    %   Assume that for all that strong inversion exists when Vgs>2*Vthresh
    %   Saturation should definitely exists when Vds>=Vthresh
    Vgs_On_Index = find(Vgs>Vthresh,1,'last');
    Vgs_Thresh_Index = find(Vgs>=Vthresh,1,'first');
    Vds_Sat_Index = find(Vds>=Vgs(Vgs_Thresh_Index));
    Vgs_On = Vgs(Vgs_On_Index);
    Vds_Sat = Vds(Vds_Sat_Index);
    Id_Sat = Id(Vds_Sat_Index,Vgs_On_Index);

    %   Slope of Id vs. Vds
    dId_dVds_Sat = diff(Id_Sat)./diff(Vds_Sat);

```

```
    %   This section uses a sensitivity threshold for percent difference
    %   between value(n) and value(final) and outputs the
    %   mean(values(UnderThreshold:final)) into a new array.
    SensitivityThresh = 0.5;
    finalValue = dId_dVds_Sat(length(dId_dVds_Sat),:);
    for i = 1:size(dId_dVds_Sat,2)
        UnderThreshold = find(abs(dId_dVds_Sat(:,i)-finalValue(i))/...
            finalValue(i) < SensitivityThresh);
        Vds_Points = Vds_Sat(UnderThreshold);
        Id_Points = Id_Sat((UnderThreshold),i);
        %   Determine the Early Voltage to find lambda
        %   lambda ~ 1/(EarlyVoltage)
        EarlyLine(:,i) = polyfit(Vds_Points,Id_Points,1);
    end
    Early_Xint = -EarlyLine(2,:)./EarlyLine(1,:);
    Early_Voltage = min(Early_Xint);
    lambda = abs(1./mean(Early_Xint));

    %   Triode mode should exist when Vds < Vgs - Vthresh
    Vds_Tri_Index = find(Vds<Vgs(Vgs_Thresh_Index));
    Vds_Tri = Vds(Vds_Tri_Index);
    Id_Tri = Id(Vds_Tri_Index,Vgs_On_Index);

    dId_dVds_Tri = diff(Id_Tri)./diff(Vds_Tri);
    finalValue = dId_dVds_Tri(length(dId_dVds_Tri),:);
    for i = 1:size(Id_Tri,2)
        UnderThreshold = find(abs(dId_dVds_Tri(:,i)-finalValue(i))/...
            finalValue(i) < SensitivityThresh,3,'first');
        %   Best way to solve for K-param is using the triode mode equation
        %   id = K*(Vgs-Vth-Vds/2)*Vds
        %   this approach allows K-param to be extracted independent
        %   from influence of lambda
        K(:,i) = Id_Tri(UnderThreshold,i)./((Vgs_On(i)-Vthresh ...
        -Vds_Tri(UnderThreshold)/2).*Vds_Tri(UnderThreshold));
    end
    Kparam = mean(K,'all');
end
```

C Evaluation Printed Circuit Board

C.1 Test Board Schematics

The Altium® schematics for the Teucer Test Board are shown in Figures C.1 to C.13.

- Figure C.1 – Top Level
- Figure C.2 – Off-board interface and connections
- Figure C.3 – Main power regulation and voltage domains
- Figure C.4 – Precision voltage reference for LDO V_{REF}
- Figure C.5 – Precision voltage references for deadzone tuning
- Figure C.6 – Regulated nanoamp current source for CMOTA
- Figure C.7 – Buffering and level-shifting for off-board digital control signals
- Figure C.8 – Teucer Chip socket and immediate on-board peripherals
- Figure C.9 – Connections and circuitry for LDO current load step evaluation
- Figure C.10 – CMOTA test cell
- Figure C.11 – Pass device array test cell
- Figure C.12 – Inverter, t-gate, and PDSD test cells
- Figure C.13 – Support interface for on-chip test cells for the MS Thesis of Roy Tan

C.2 Test Board Assembly Drawings & Layout

The Altium® assembly drawings and PCB layout for the Teucer Test Board are shown in Figures C.14 to C.24.

- Figure C.14 – Assembly drawing of top layer components
- Figure C.15 – Assembly drawing of bottom layer components
- Figure C.16 – Layout drawing of first (top) layer metal for components and routing
- Figure C.17 – Layout drawing of second layer metal for ground planes
- Figure C.18 – Layout drawing of third layer metal for power plane routing
- Figure C.19 – Layout drawing of fourth layer metal for power plane routing
- Figure C.20 – Layout drawing of fifth layer metal for ground planes
- Figure C.21 – Layout drawing of sixth (bottom) layer metal for components and routing

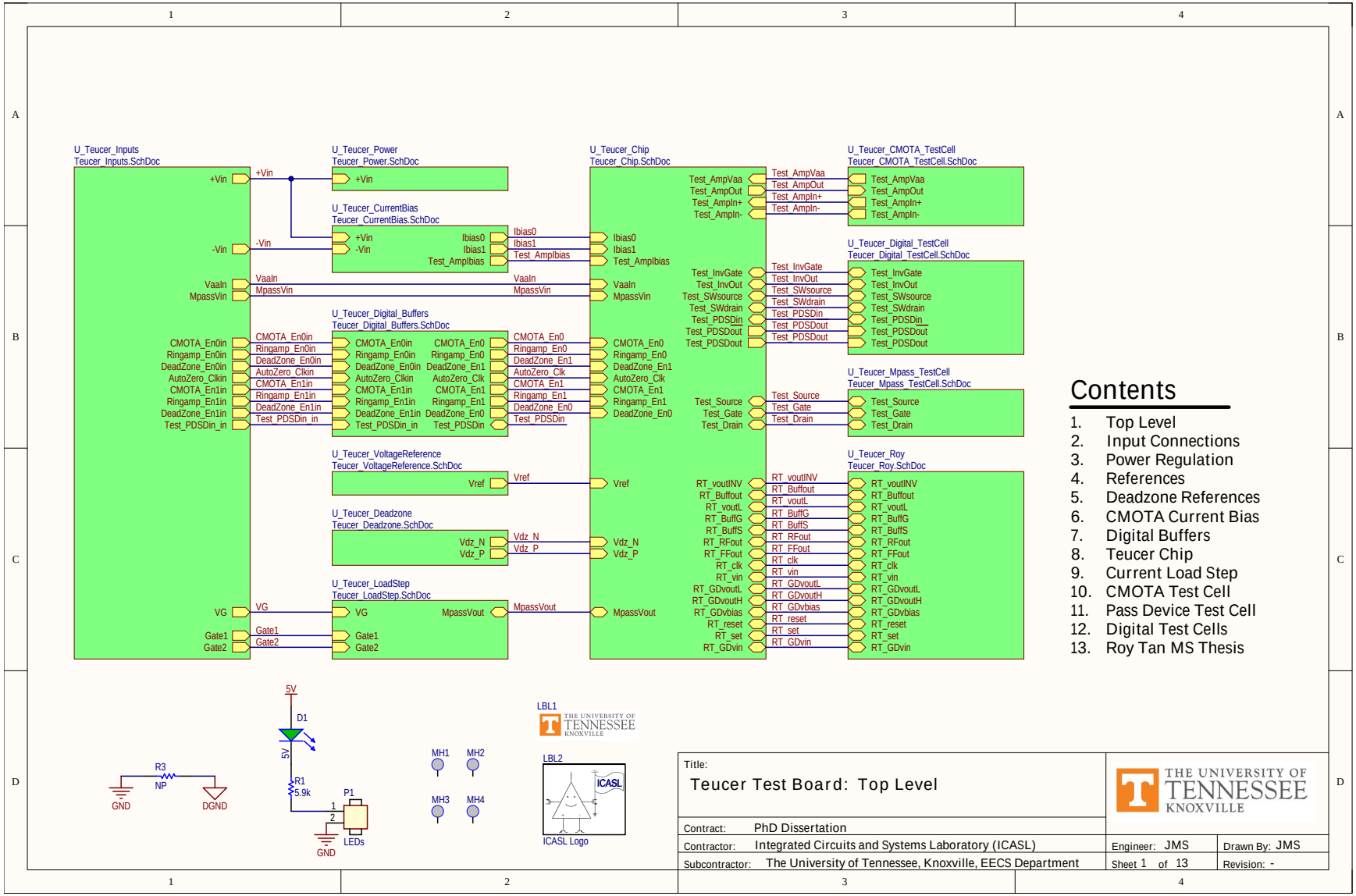


Figure C.1: Teucer test board schematic page 1

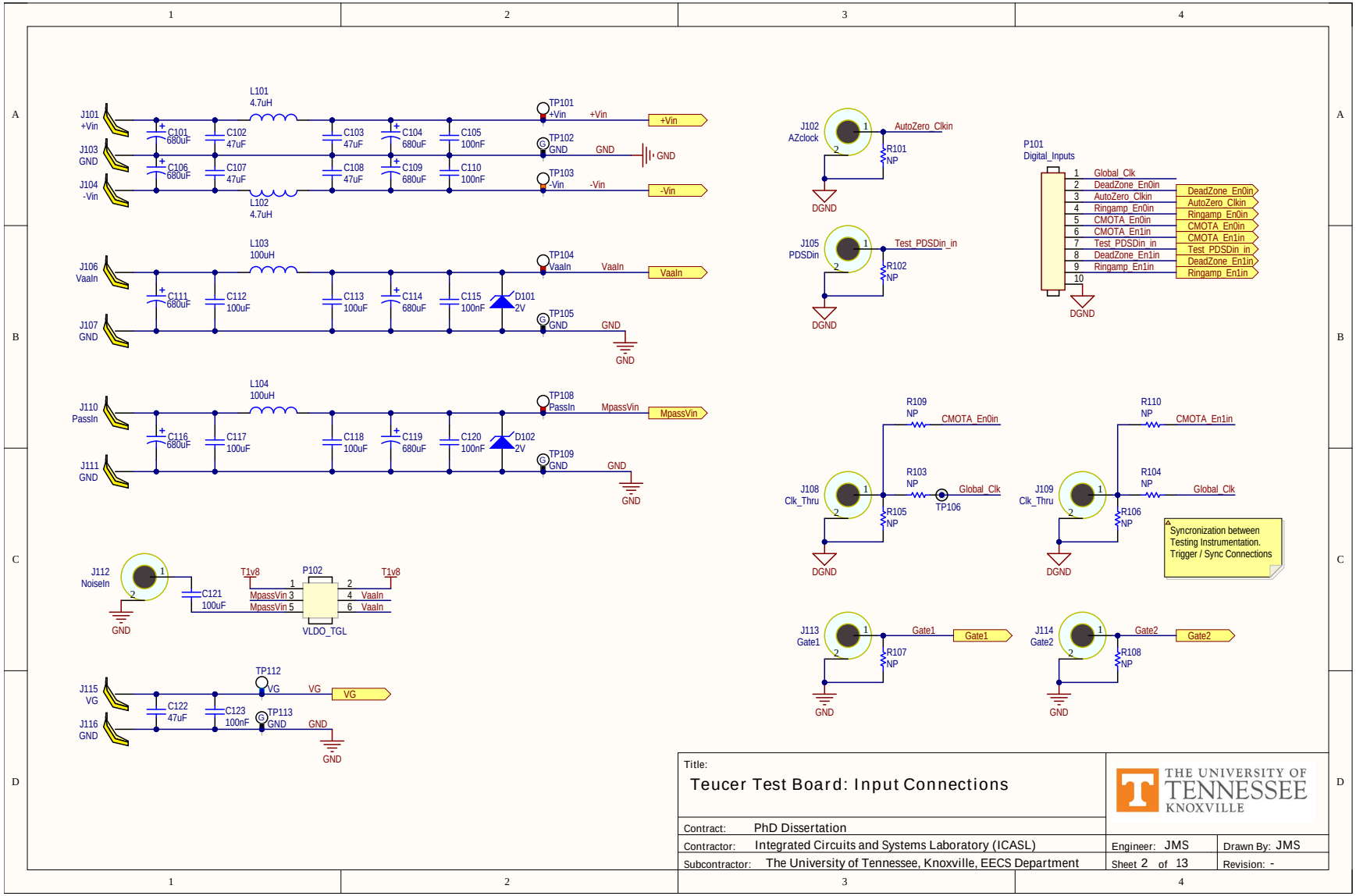


Figure C.2: Teucer test board schematic page 2

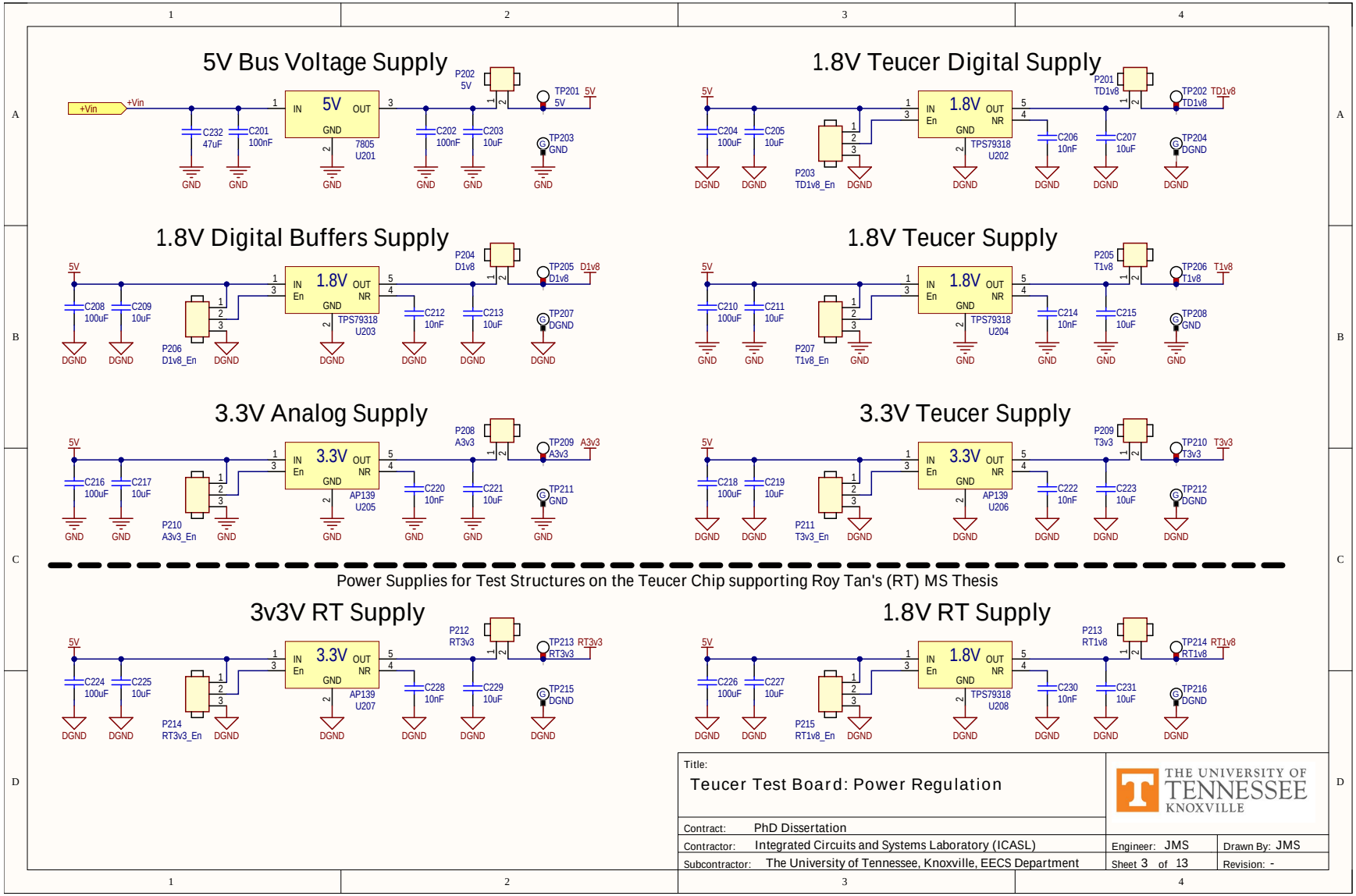


Figure C.3: Teucer test board schematic page 3

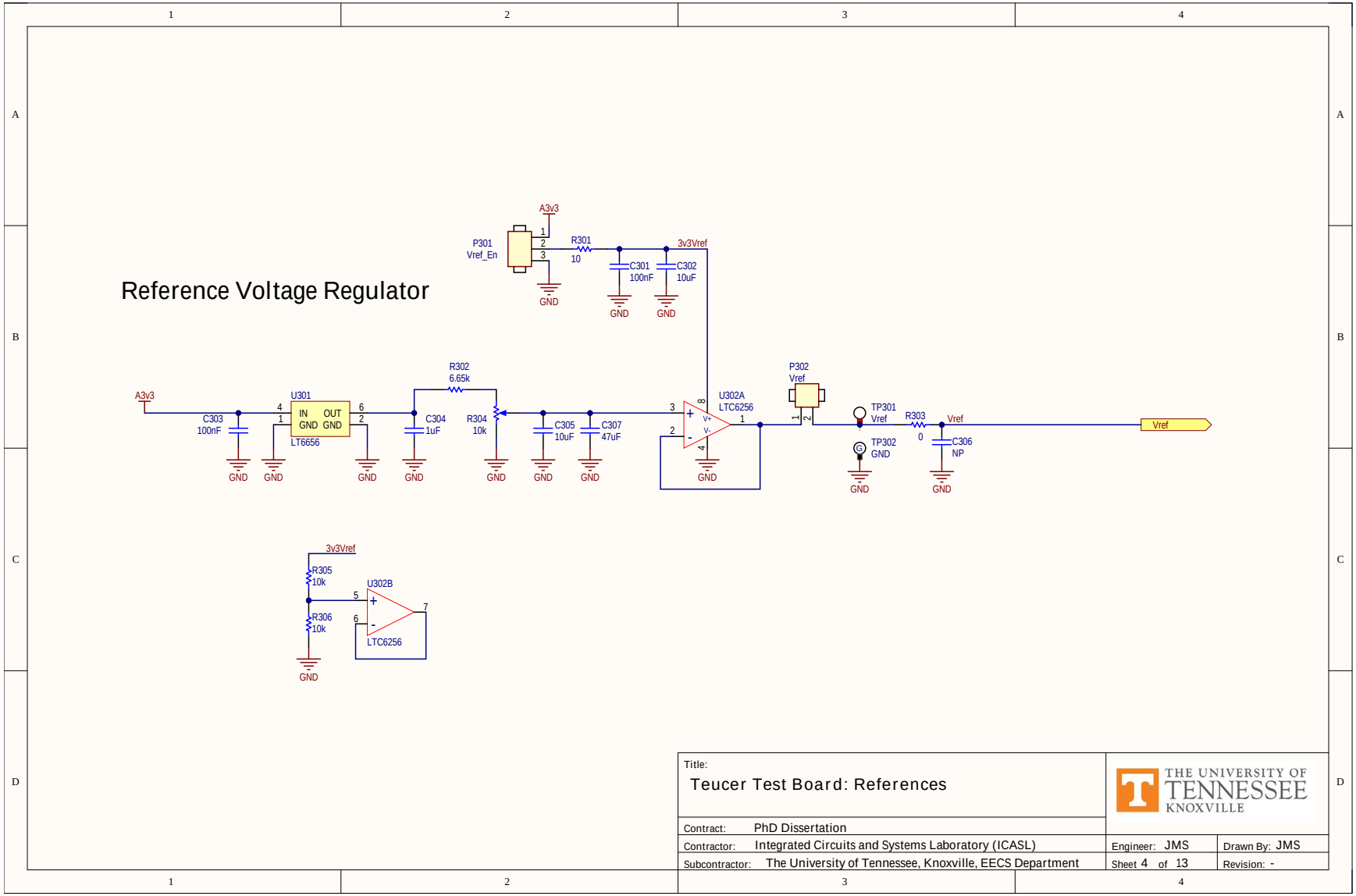


Figure C.4: Teucer test board schematic page 4

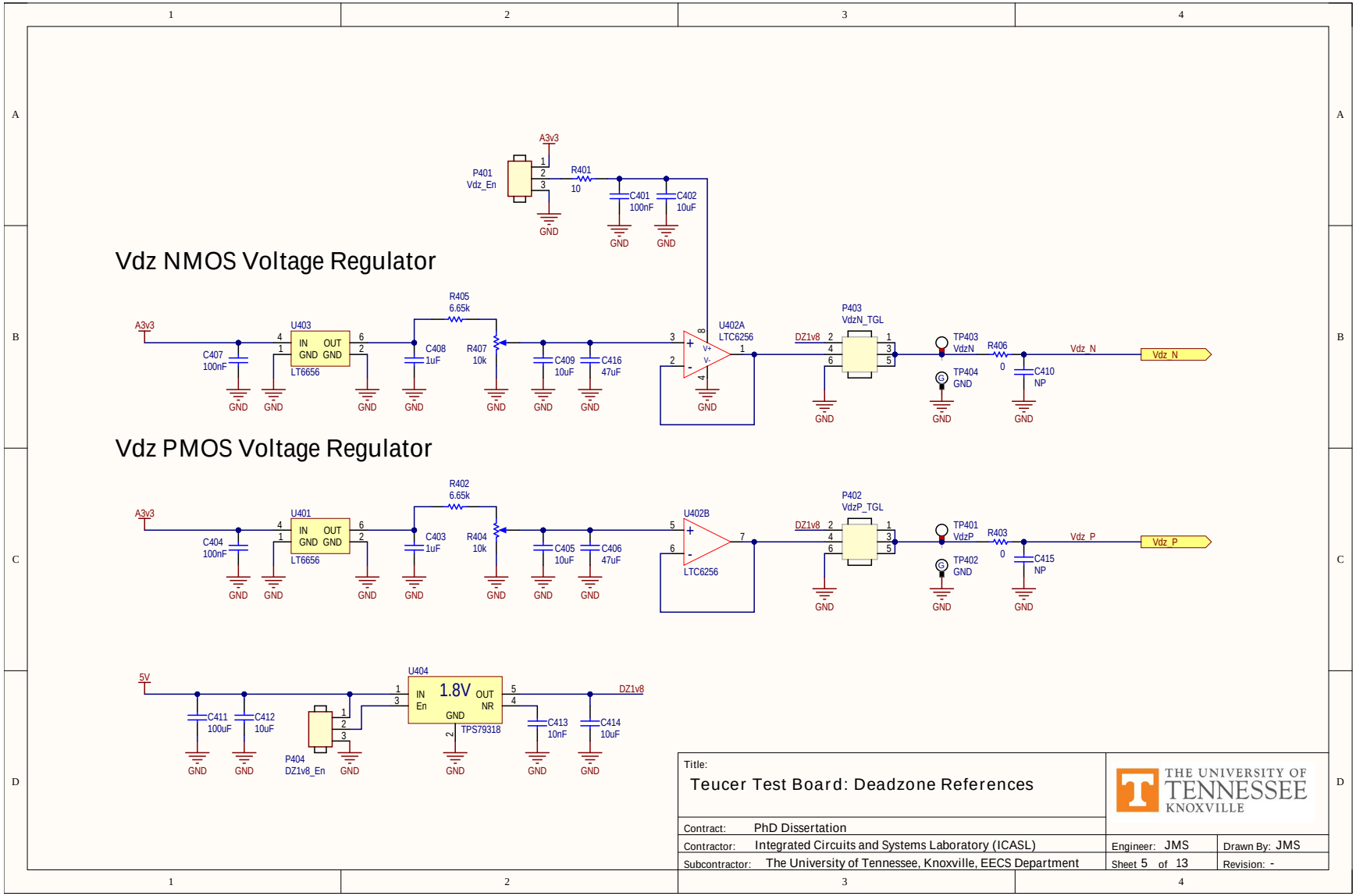


Figure C.5: Teucer test board schematic page 5

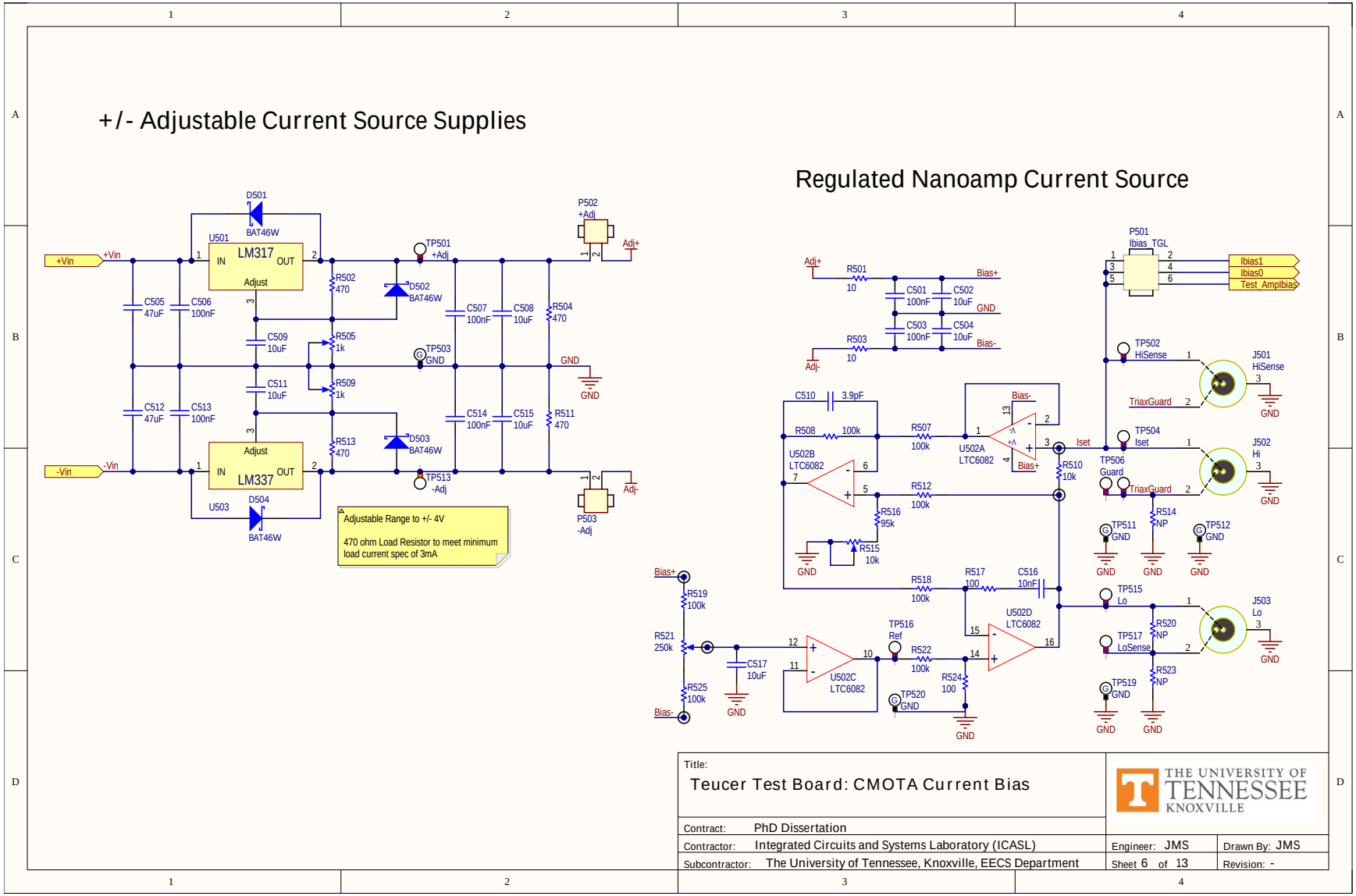


Figure C.6: Teucer test board schematic page 6

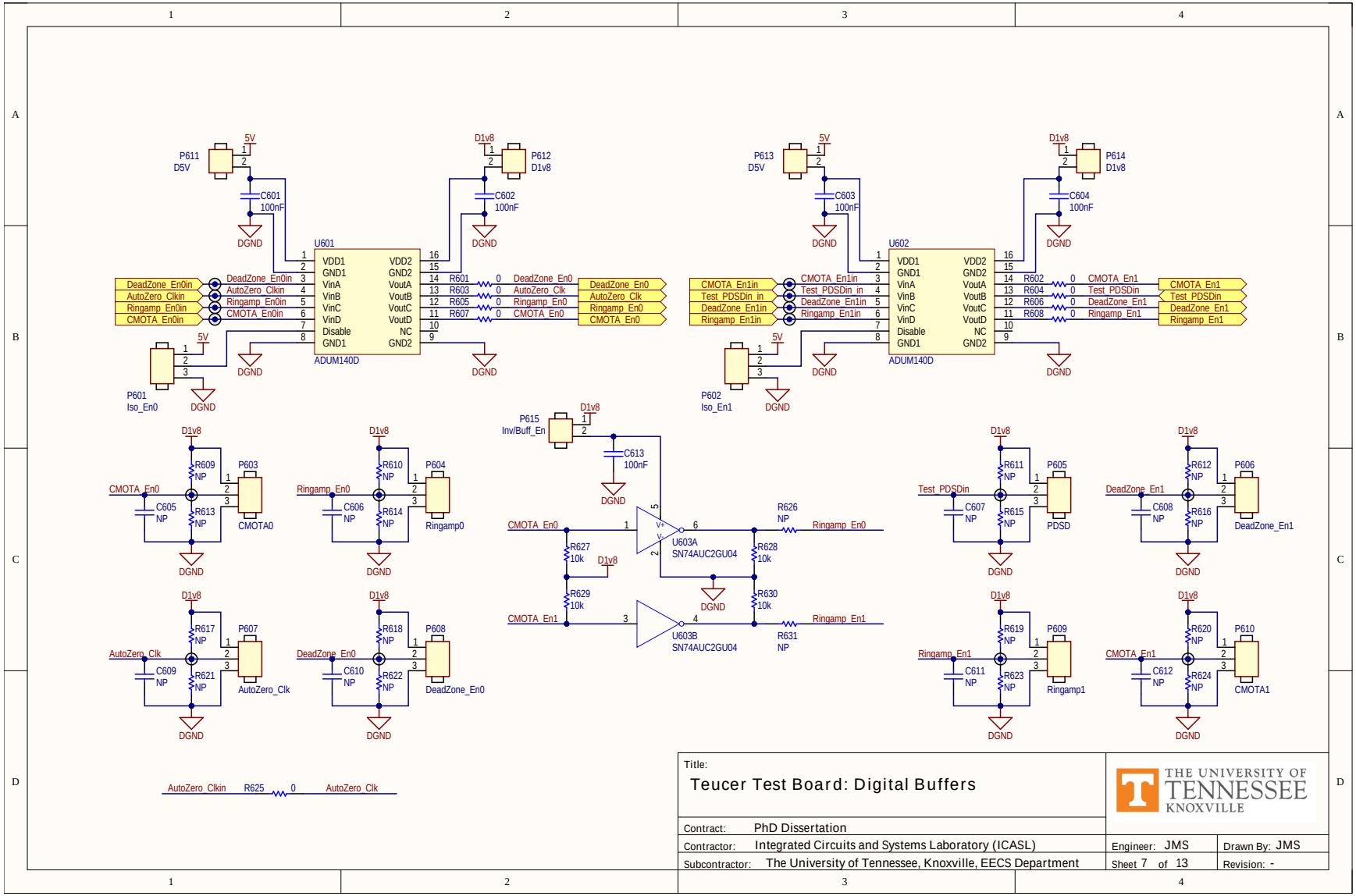


Figure C.7: Teucer test board schematic page 7

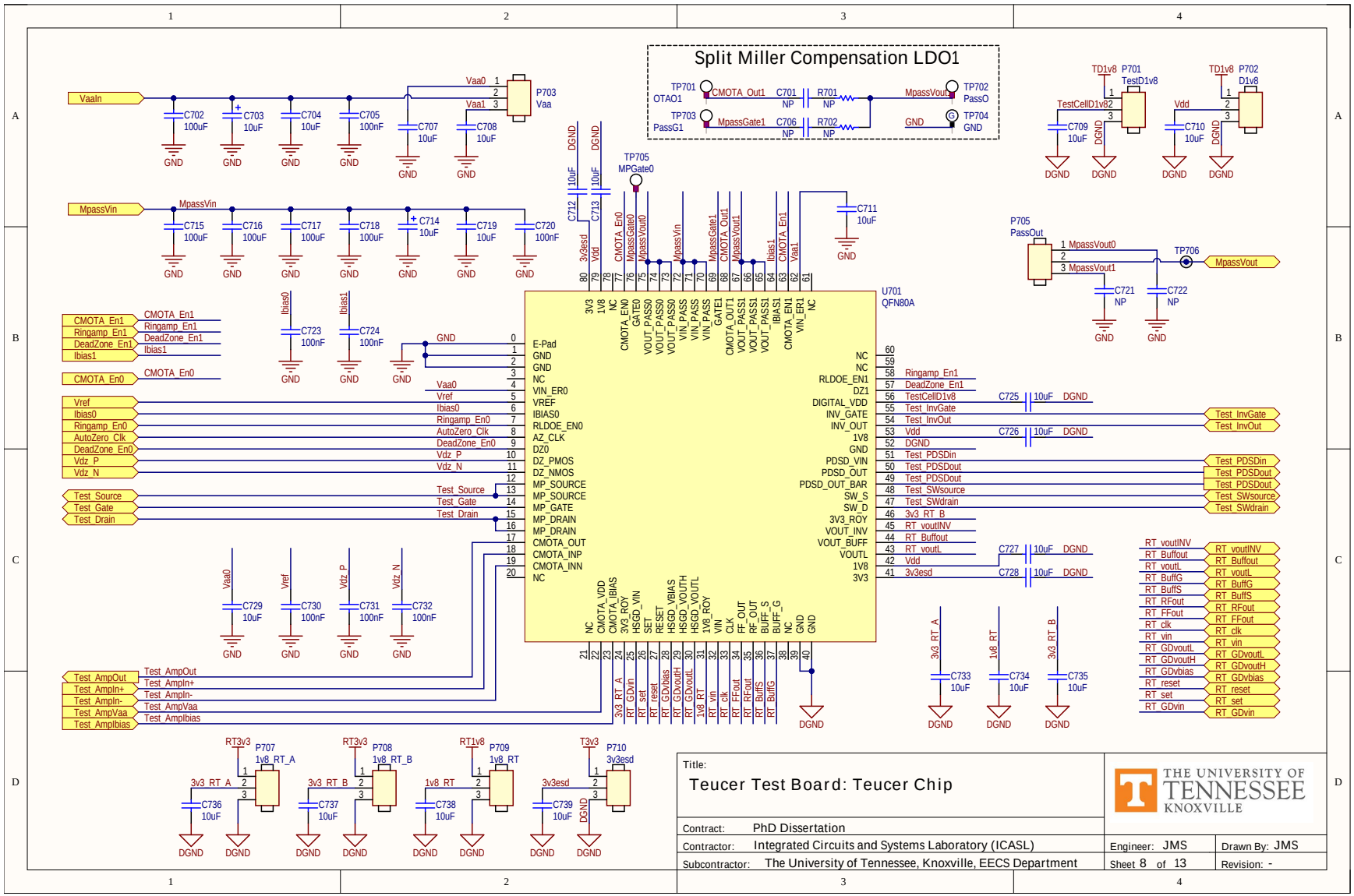


Figure C.8: Teucer test board schematic page 8

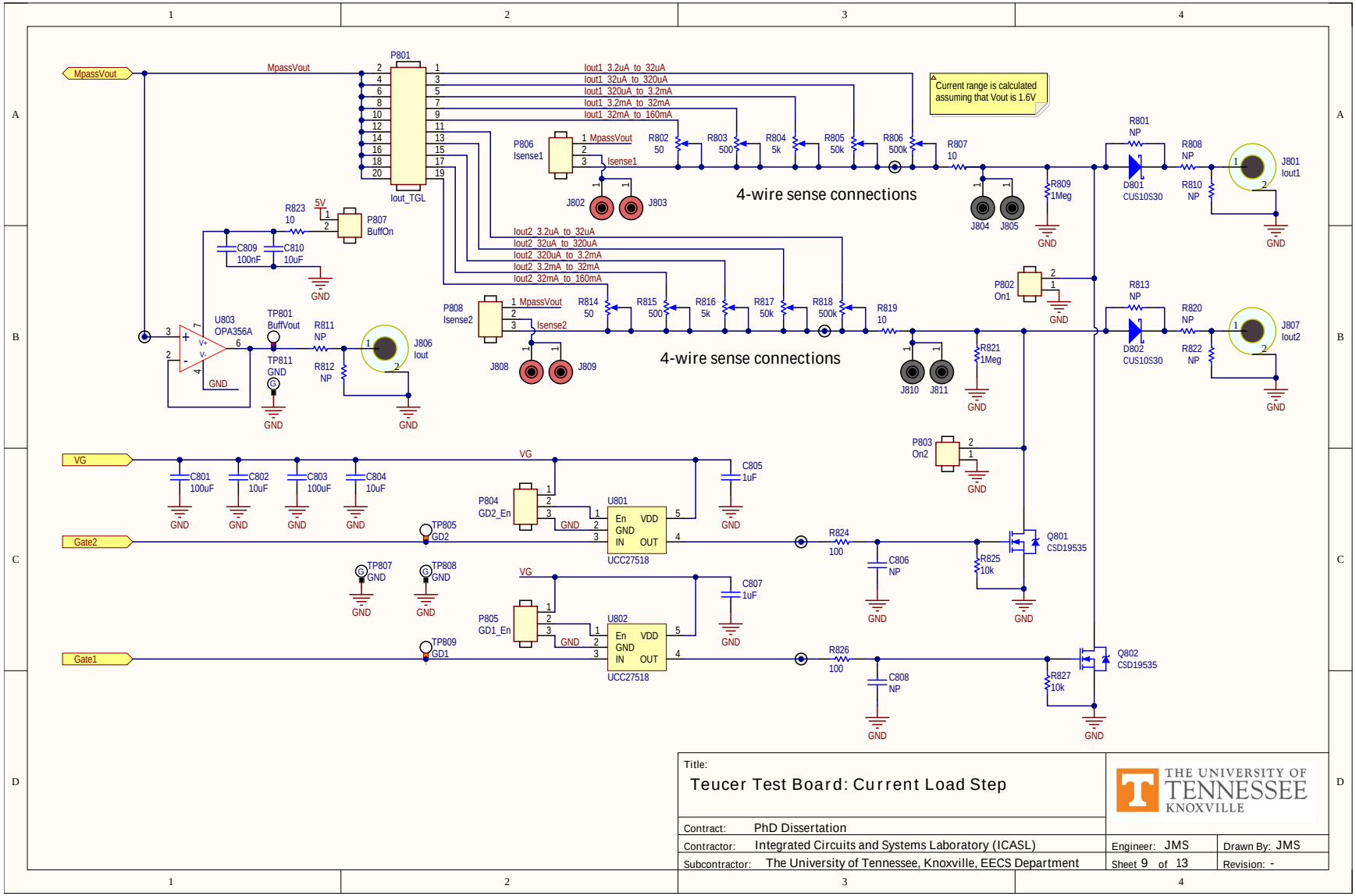


Figure C.9: Teucer test board schematic page 9

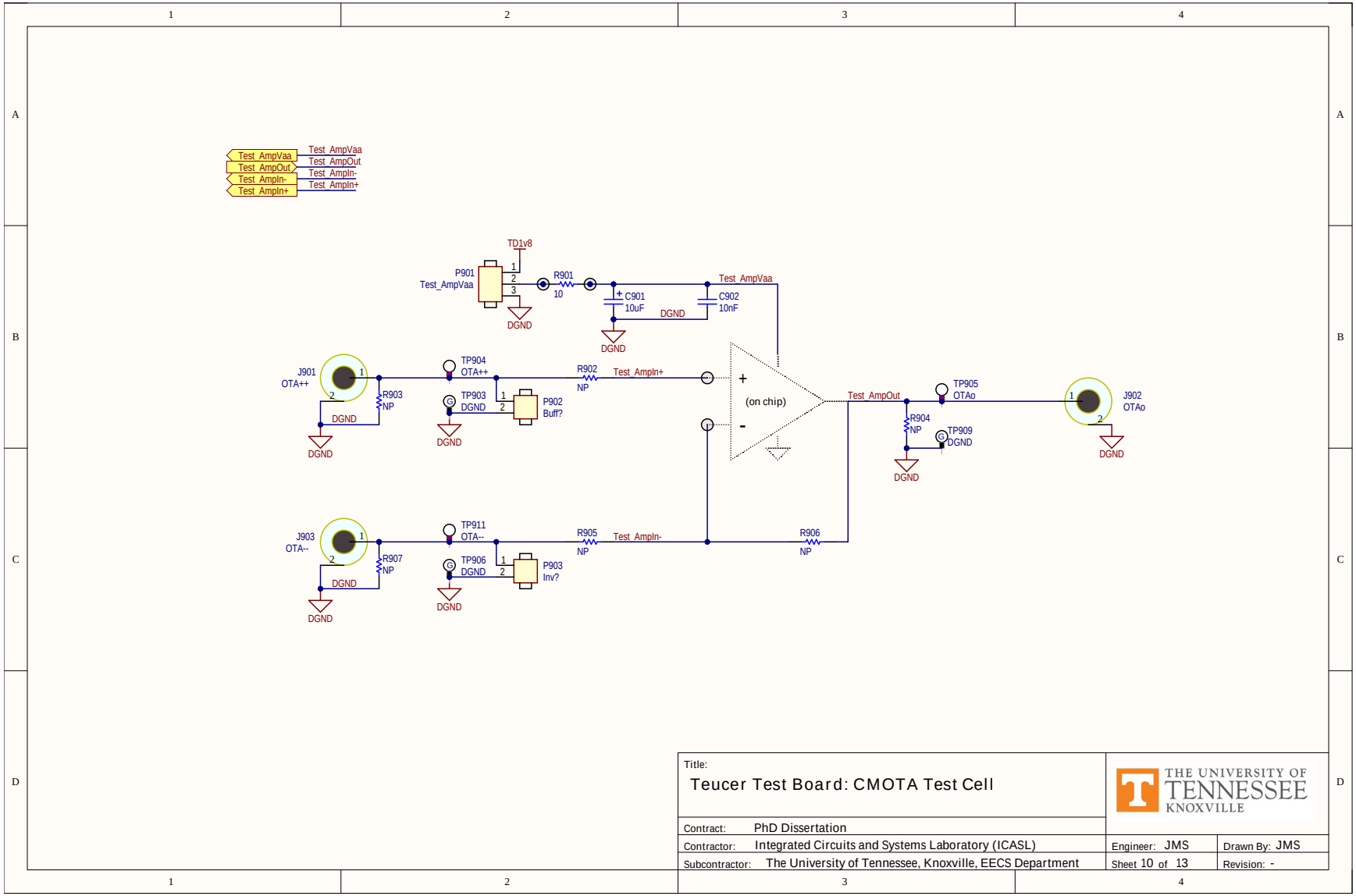


Figure C.10: Teucer test board schematic page 10

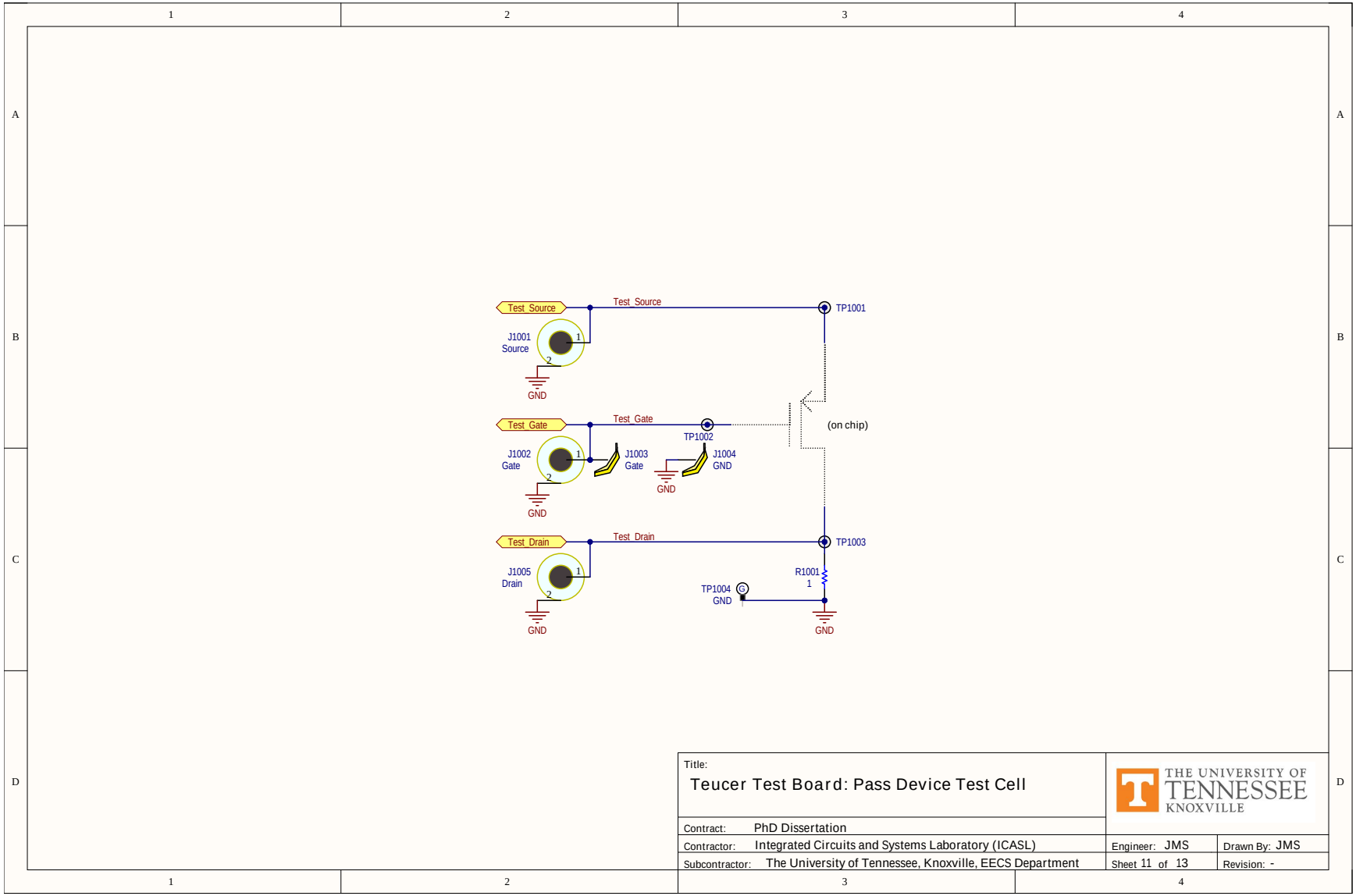


Figure C.11: Teucer test board schematic page 11

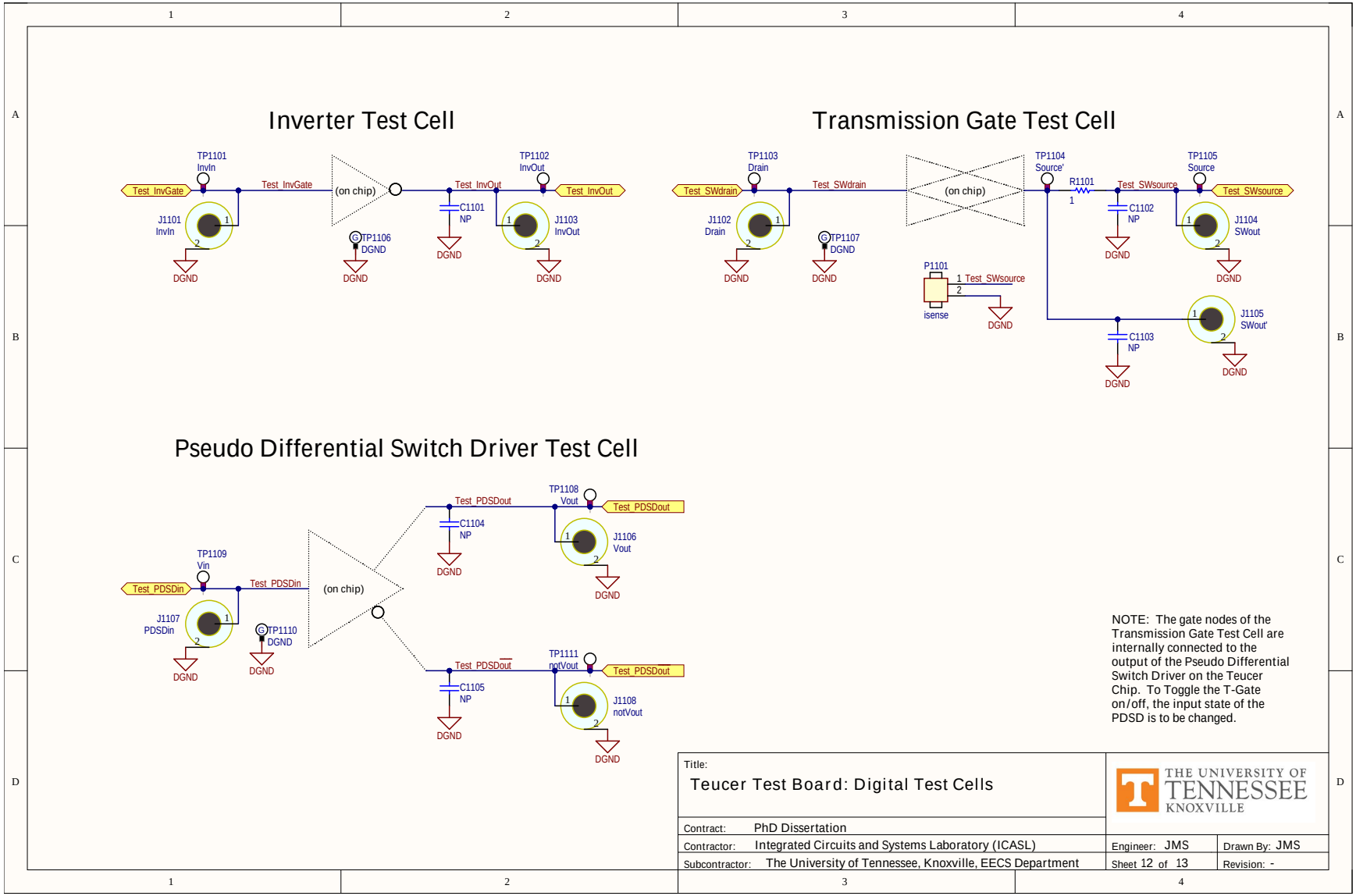


Figure C.12: Teucer test board schematic page 12

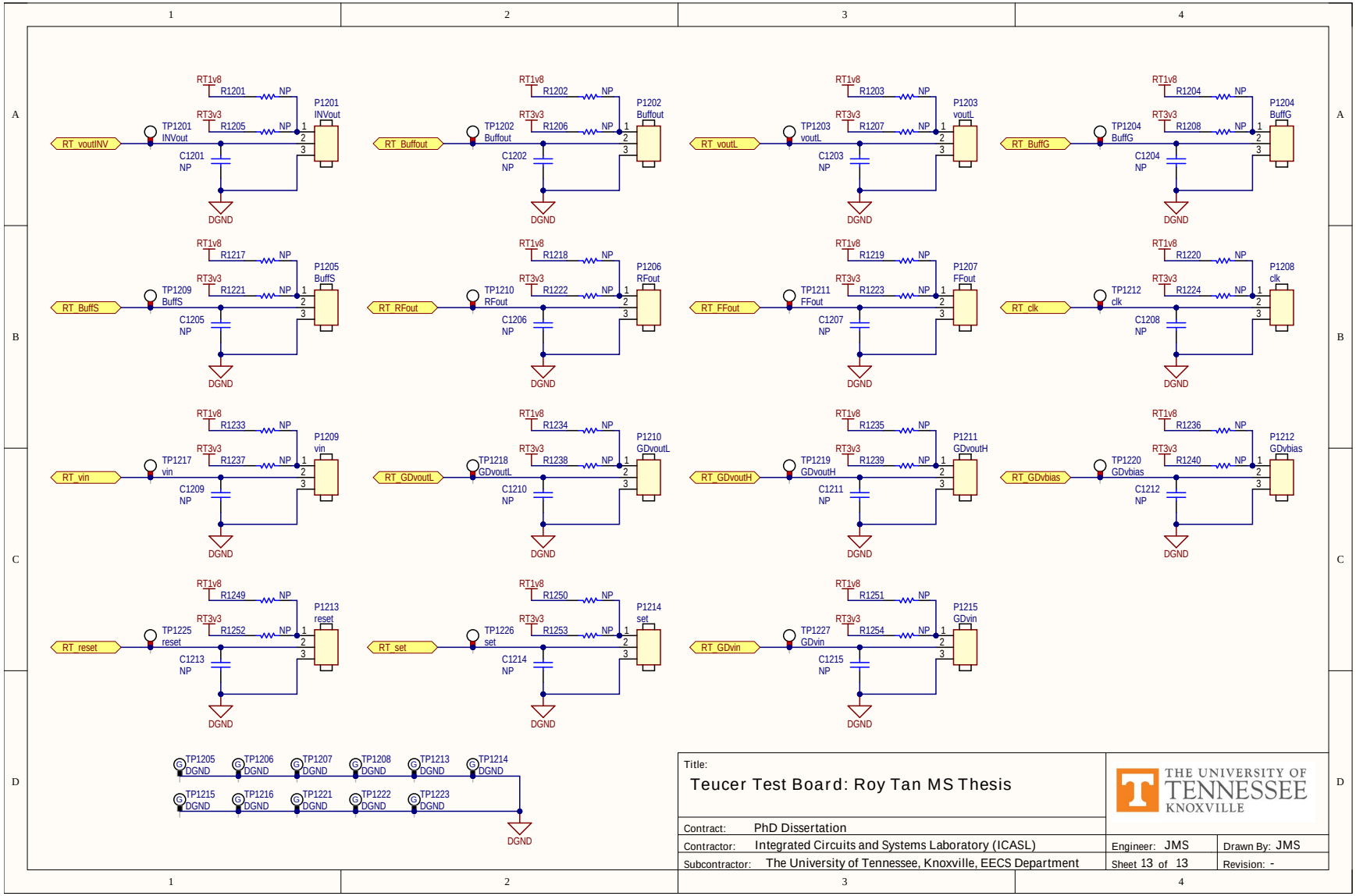


Figure C.13: Teucer test board schematic page 13

- Figure C.22 – 3D rendering of top side of PCB
- Figure C.23 – 3D rendering of bottom side of PCB
- Figure C.24 – 3D rendering of angled view of PCB

C.3 Test Board Bill of Materials

The bill of materials (BOM) for the Teucer Test Board is shown in Figures C.25 to C.28.

- Figure C.25 – Bill of Materials page 1
- Figure C.26 – Bill of Materials page 2
- Figure C.27 – Bill of Materials page 3
- Figure C.28 – Bill of Materials page 4

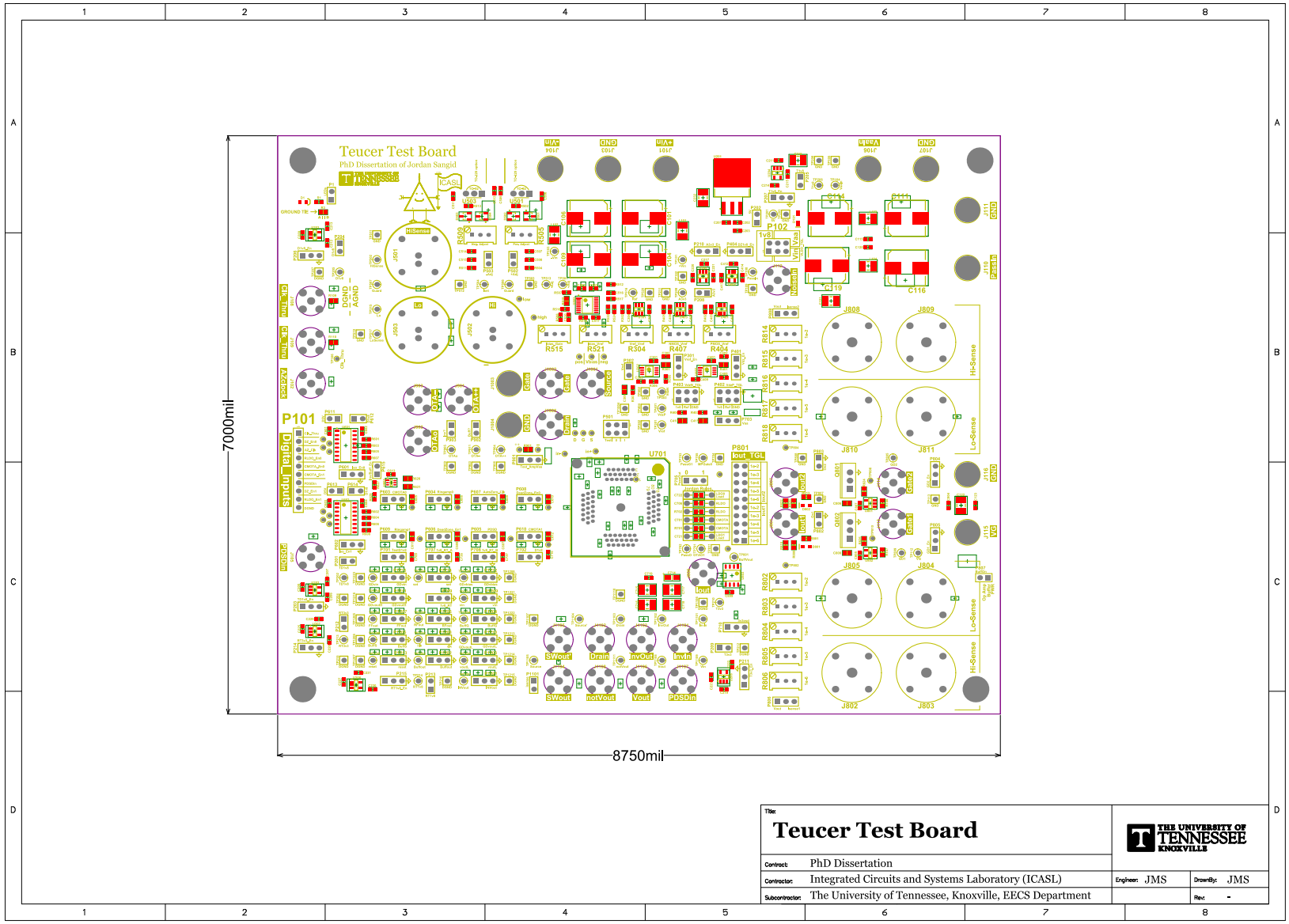


Figure C.14: Teucer test board layout and assembly drawings page 1, top layer components

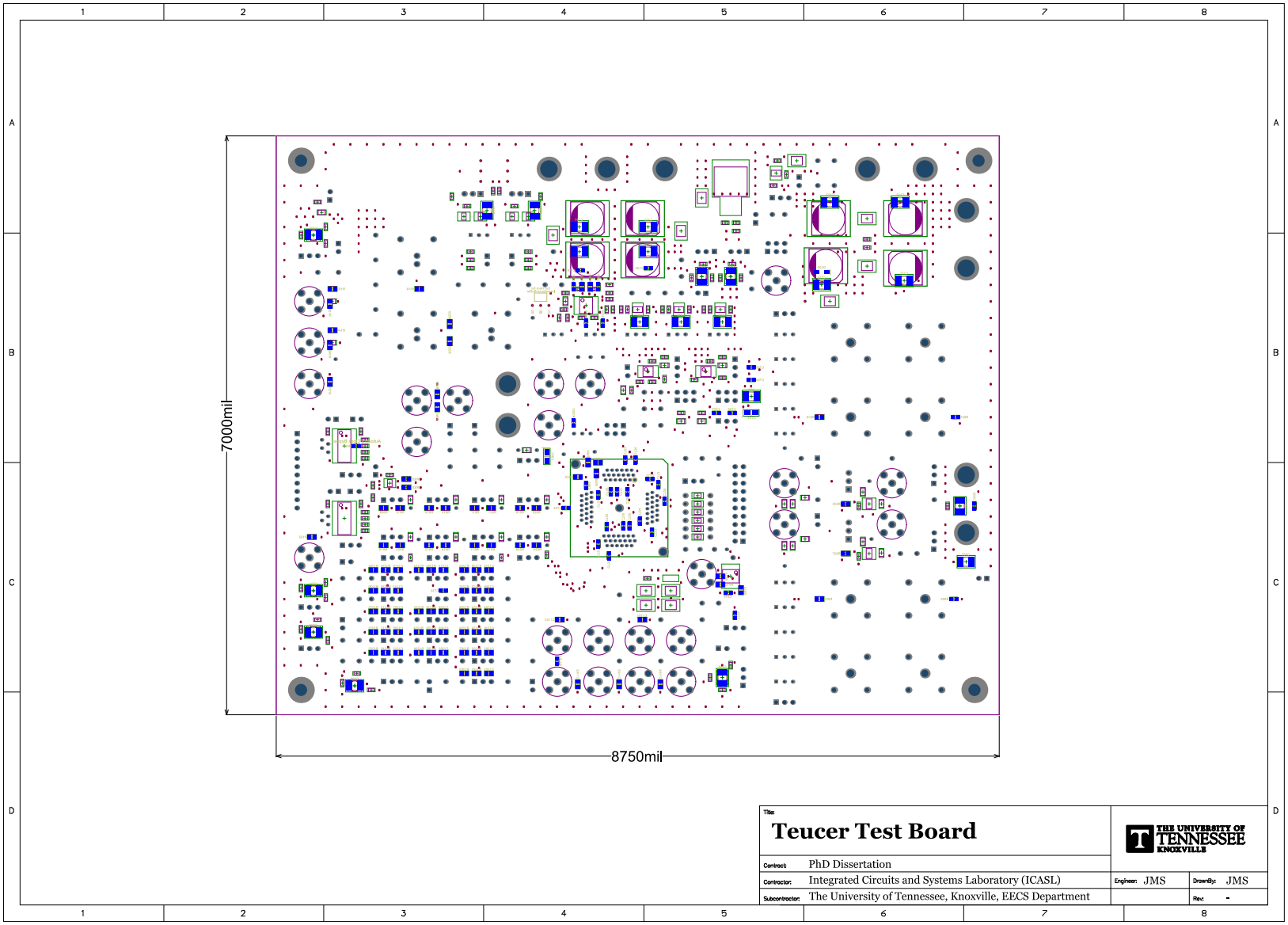


Figure C.15: Teucer test board layout and assembly drawings page 2, bottom layer components

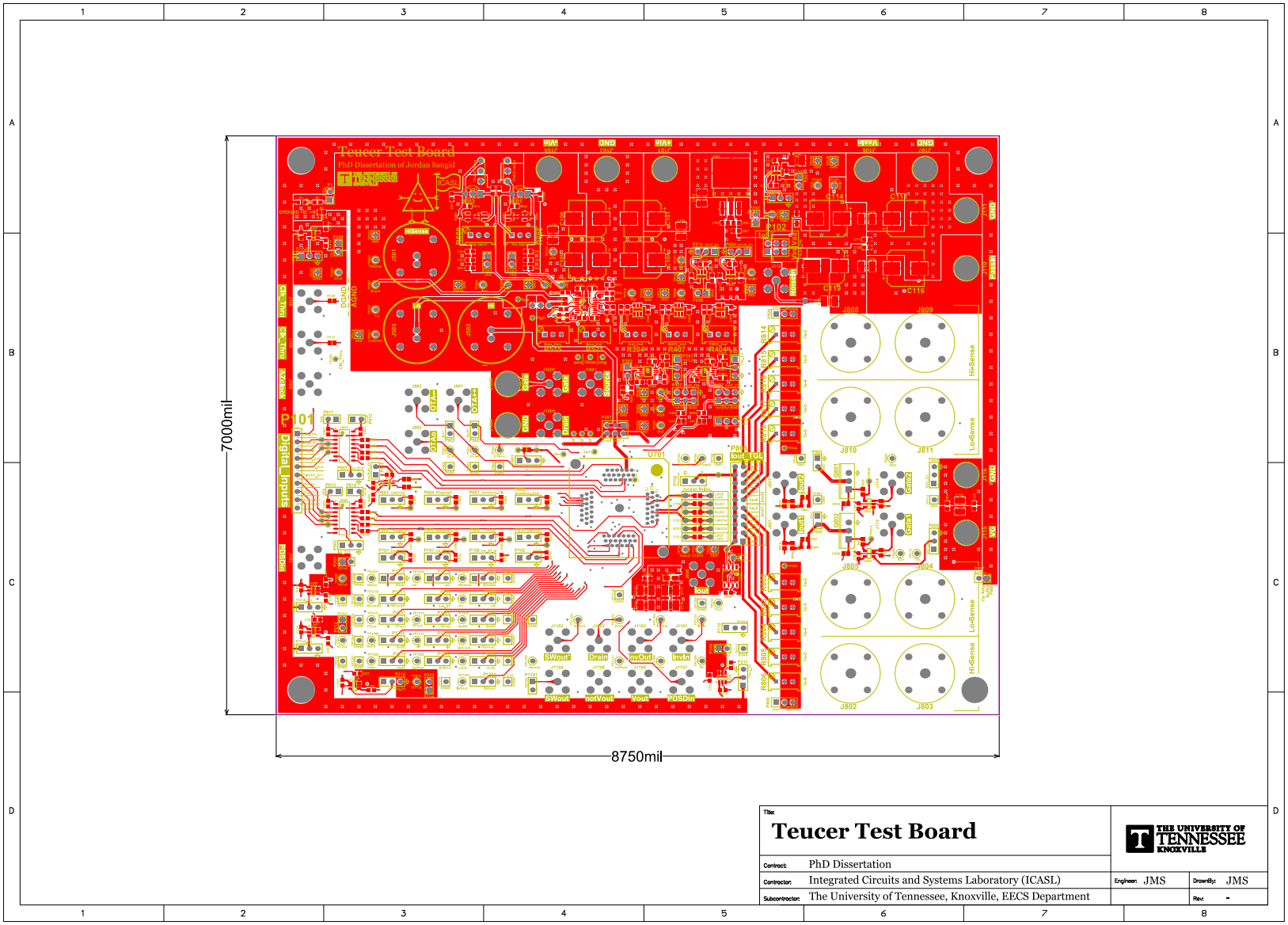


Figure C.16: Teucer test board layout and assembly drawings page 3, first (top) layer metal

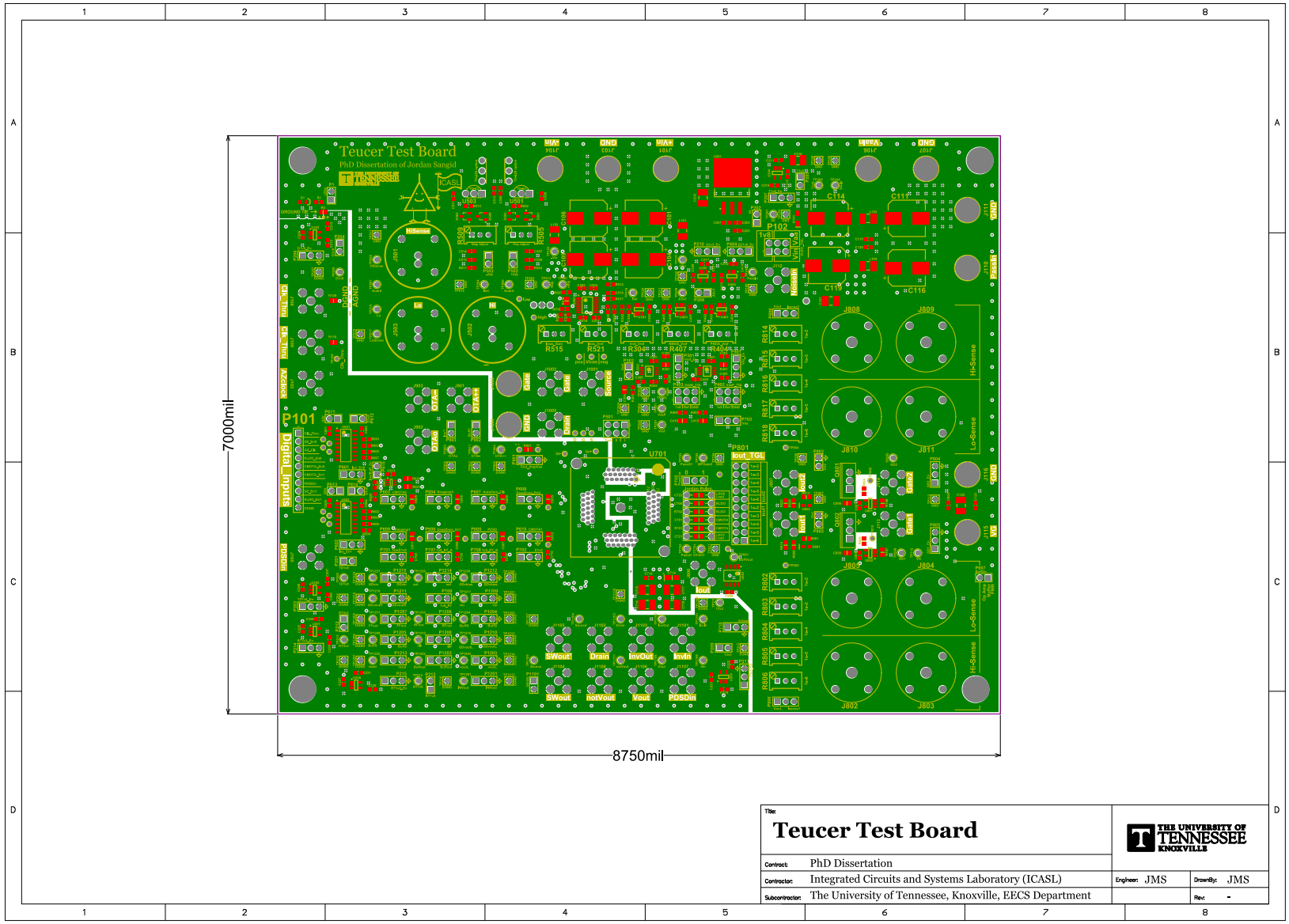


Figure C.17: Teucer test board layout and assembly drawings page 4, second layer ground metal

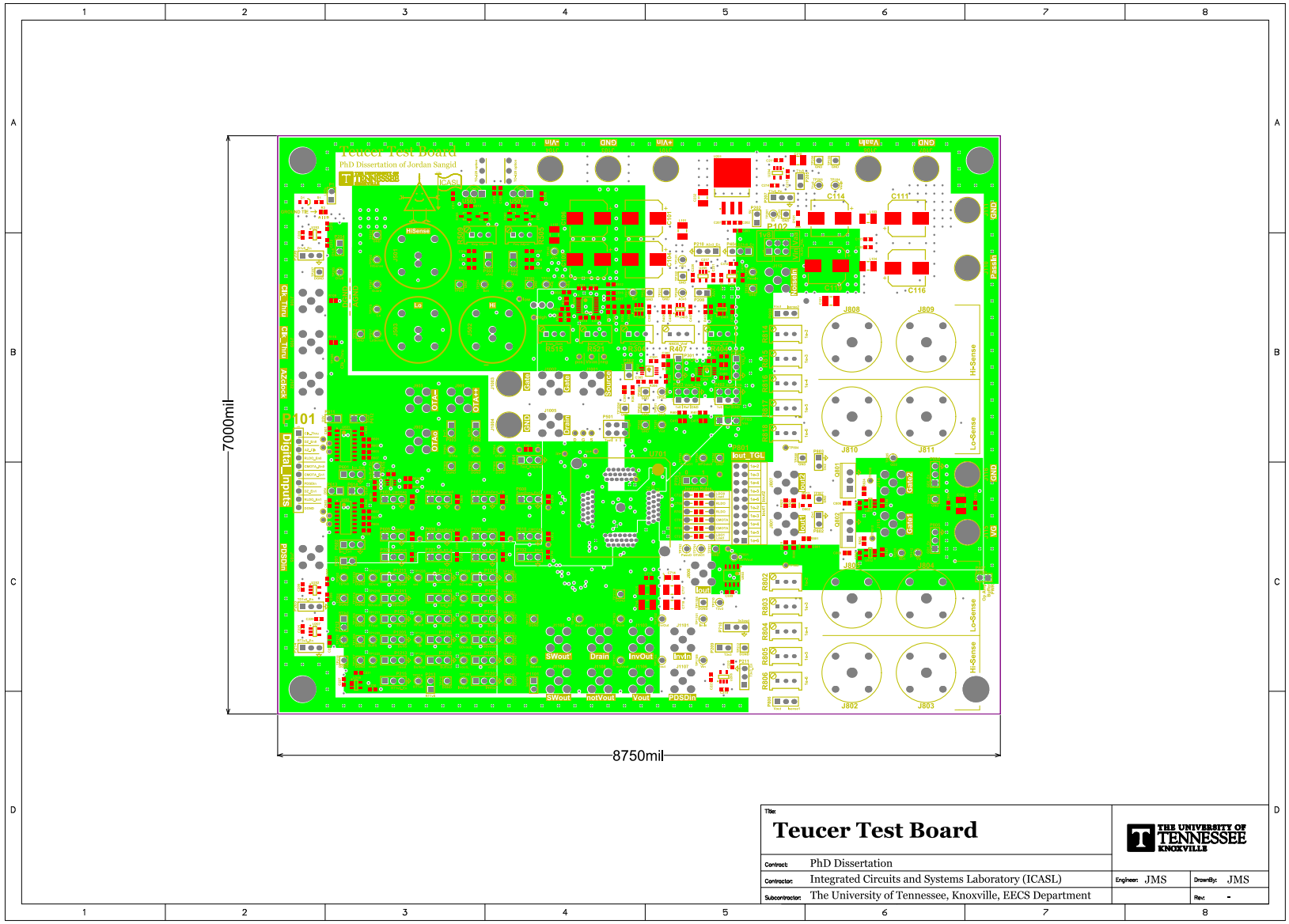


Figure C.18: Teucer test board layout and assembly drawings page 5, third layer power and routing metal

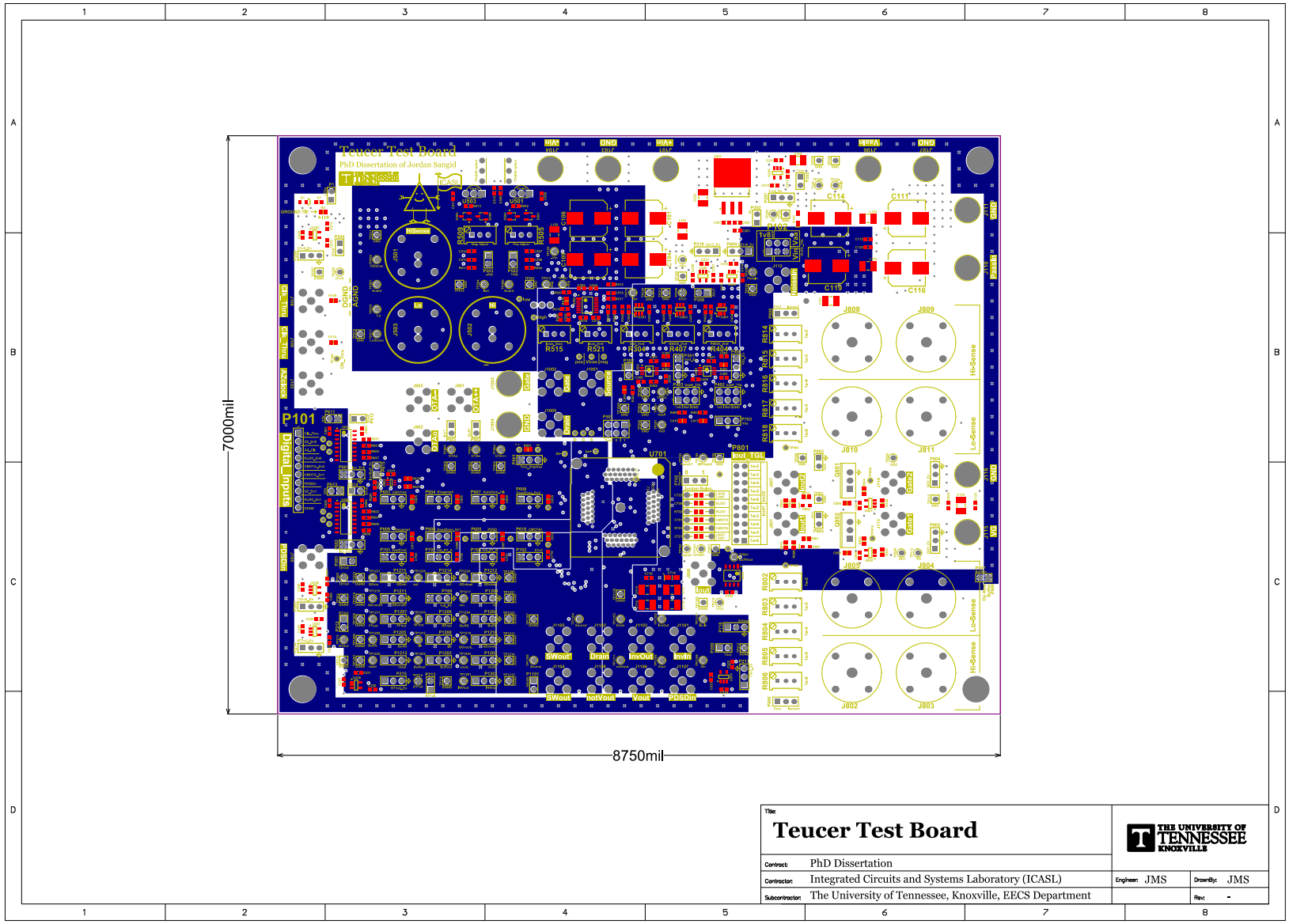


Figure C.19: Teucer test board layout and assembly drawings page 6, fourth layer power and routing metal

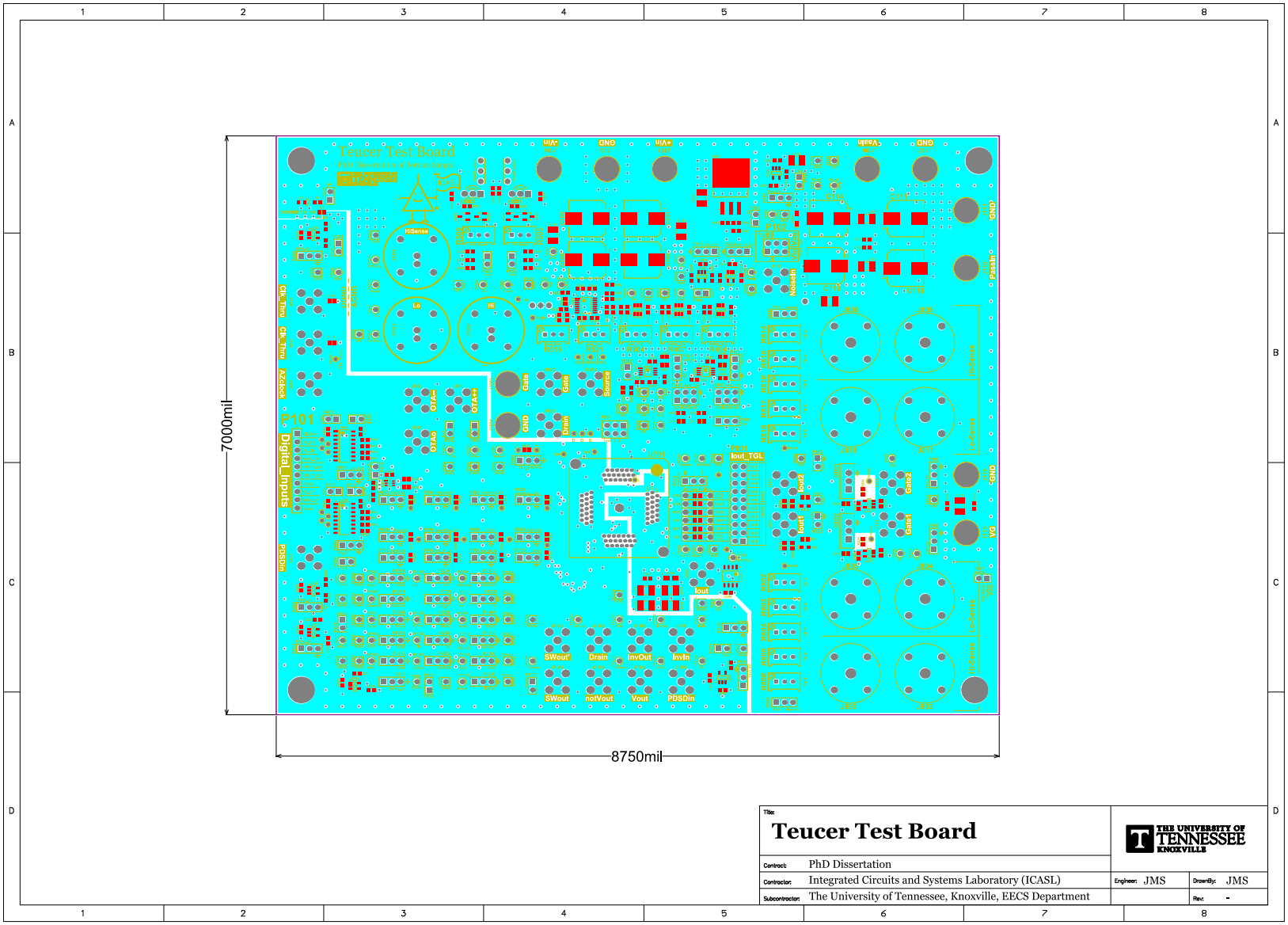


Figure C.20: Teucer test board layout and assembly drawings page 7, fifth layer ground metal

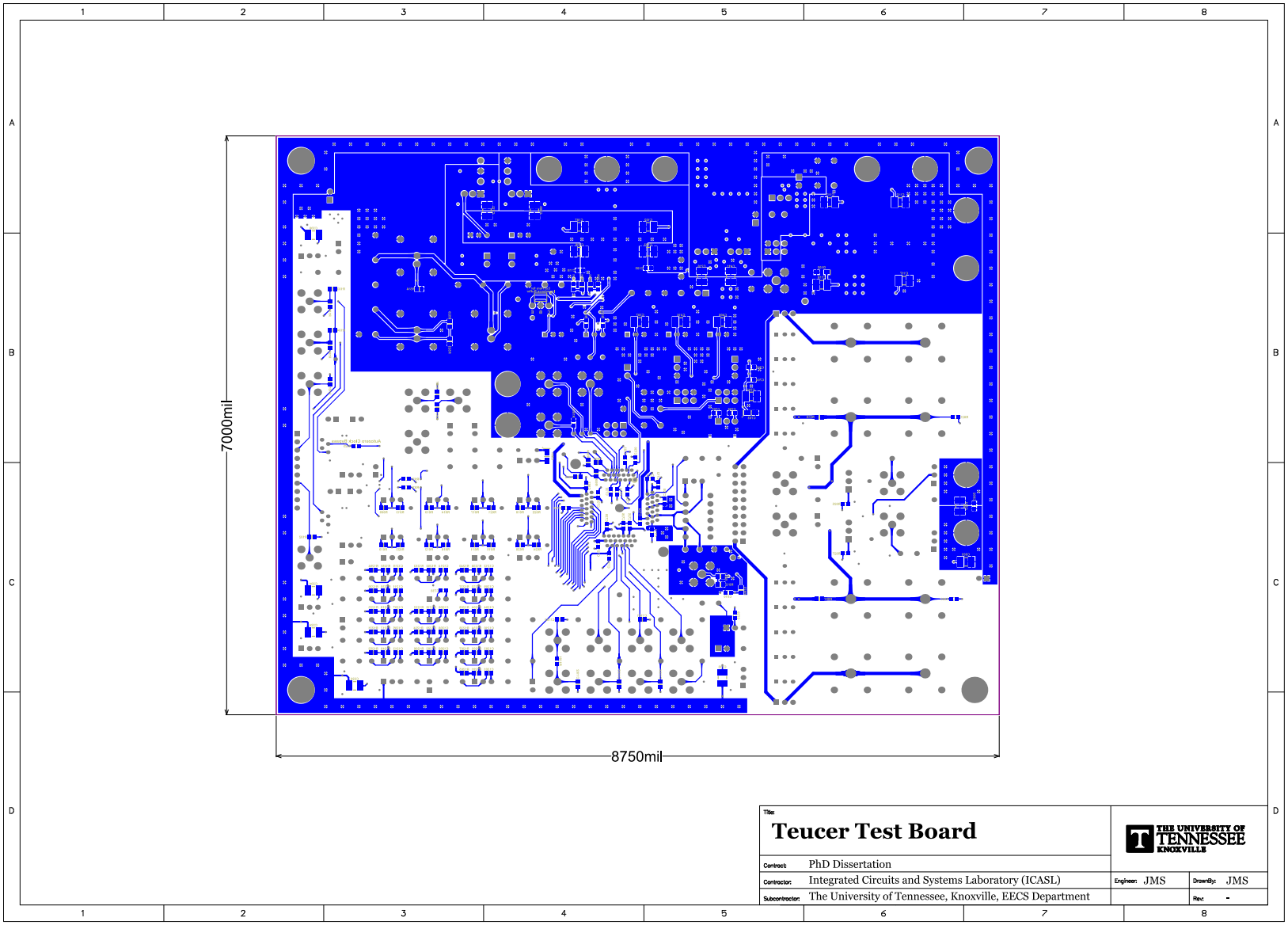


Figure C.21: Teucer test board layout and assembly drawings page 8, sixth (bottom) layer metal

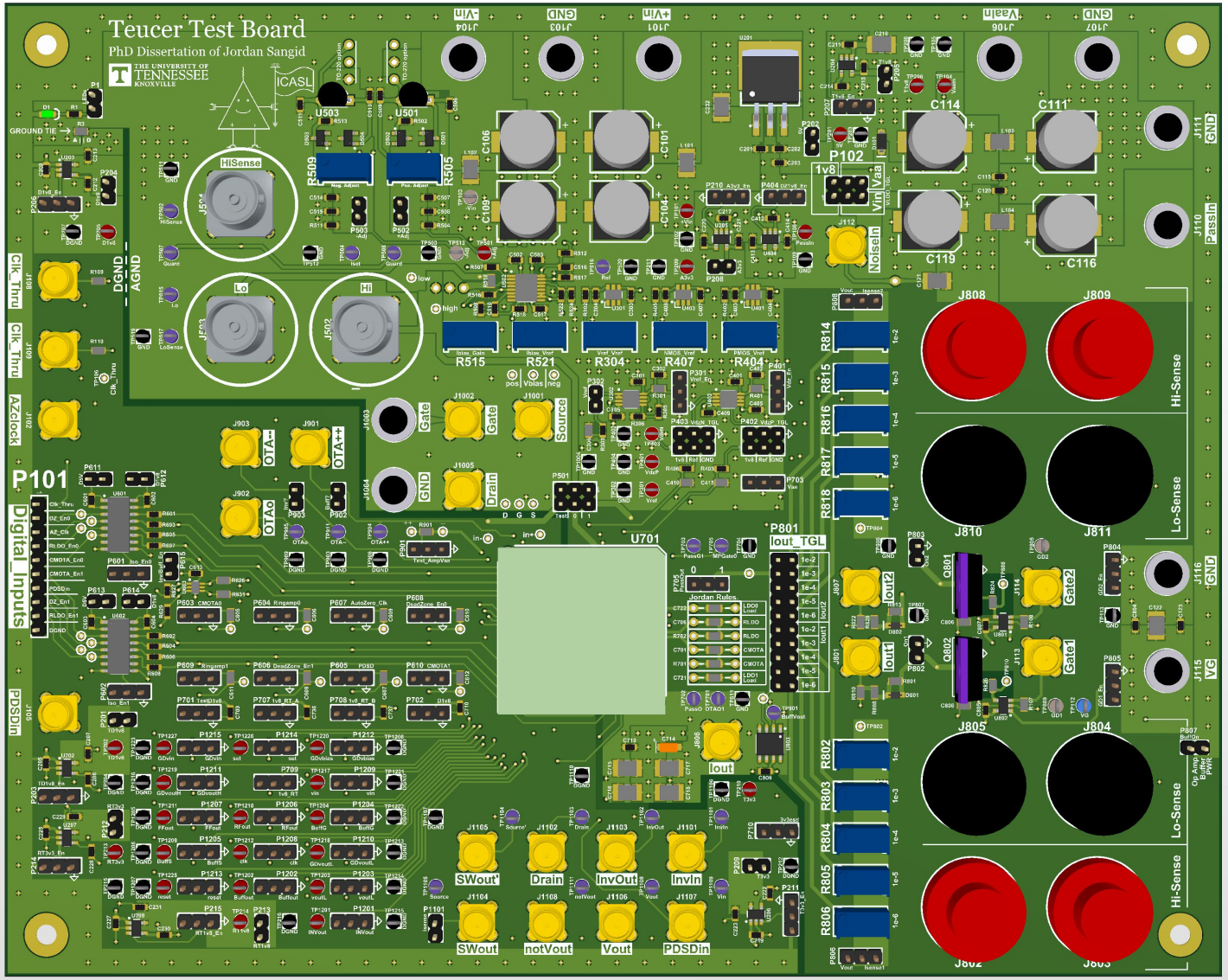


Figure C.22: Teucer test board layout and assembly drawings page 9, 3D render top-side direct

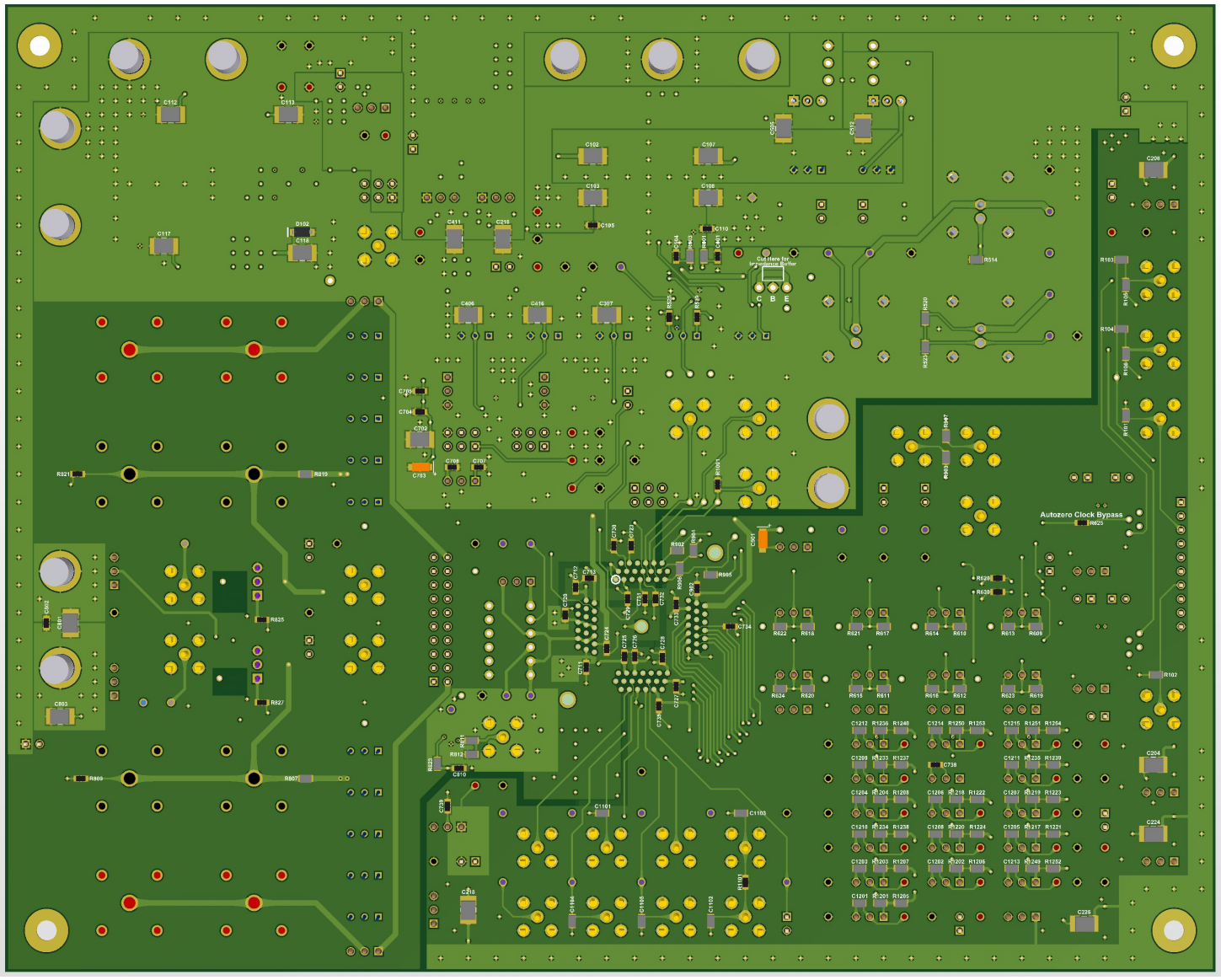


Figure C.23: Teucer test board layout and assembly drawings page 10, 3D render bottom-side direct

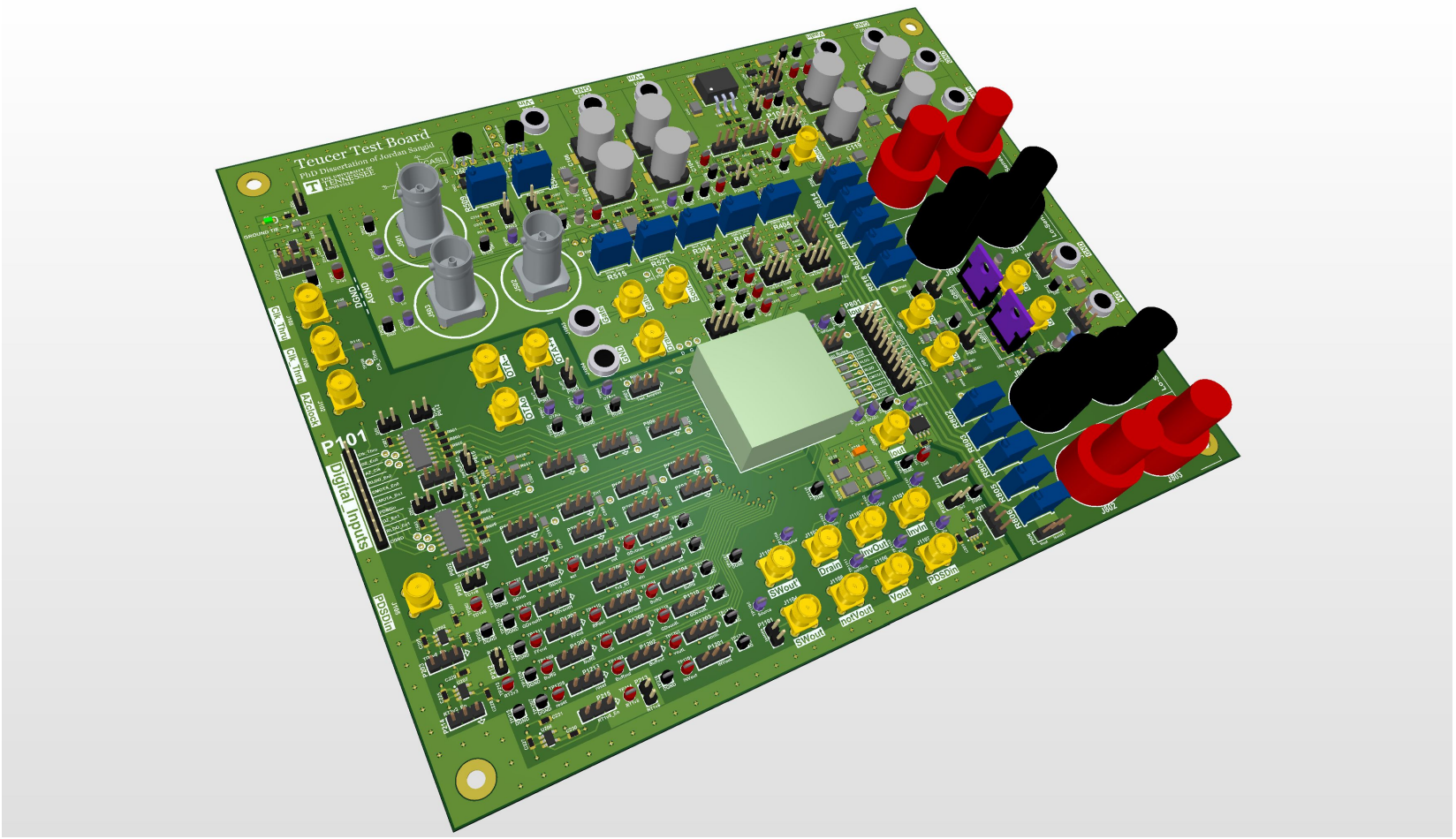


Figure C.24: Teucer test board layout and assembly drawings page 11, 3D render cinematic viewing

PhD Dissertation
Integrated Circuits and Systems Laboratory (ICASL)
The University of Tennessee, Knoxville, EECS Department

THE UNIVERSITY OF TENNESSEE KNOXVILLE

TeucerPCB.PrjPcb
10/26/2021

Quantity	Designator	Description	Value	Manufacturer 1	Manufacturer Part Number 1
8	C101, C104, C106, C109, C111, C114, C116, C119	Capacitor, Electrolytic	680uF	Nichicon	UCL1E681MNL1GS
11	C102, C103, C107, C108, C122, C232, C307, C406, C416, C505, C512	Capacitor, Ceramic	47uF	Taiyo Yuden	TMK325ABJ476MM-P
31	C105, C110, C115, C120, C123, C201, C202, C301, C303, C401, C404, C407, C501, C503, C506, C507, C513, C514, C601, C602, C603, C604, C613, C705, C720, C723, C724, C730, C731, C732, C809	Capacitor, Ceramic	100nF	Samsung	CL10B104KA8NNNC
20	C112, C113, C117, C118, C121, C204, C208, C210, C216, C218, C224, C226, C411, C702, C715, C716, C717, C718, C801, C803	Capacitor, Ceramic	100uF	Samsung	CL32A107MPVNNNE
53	C203, C205, C207, C209, C211, C213, C215, C217, C219, C221, C223, C225, C227, C229, C231, C302, C305, C402, C405, C409, C412, C414, C502, C504, C508, C509, C511, C515, C517, C704, C707, C708, C709, C710, C711, C712, C713, C719, C725, C726, C727, C728, C729, C733, C734, C735, C736, C737, C738, C739, C802, C804, C810	Capacitor, Ceramic	10uF	Murata	GRM188R61A106ME69D
10	C206, C212, C214, C220, C222, C228, C230, C413, C516, C902	Capacitor, Ceramic	10nF	Murata	GRT1885C1E103JA02J
5	C304, C403, C408, C805, C807	Capacitor, Ceramic	1uF	Samsung	CL10B105MO8NNWC

Figure C.25: Teucer test board bill of materials (BOM) page 1

1	C510	Capacitor, Ceramic	3.9pF	Yageo	CC0603BRNPO9BN3R9
3	C703, C714, C901	Capacitor, Tantalum	10uF	KEMET	T525A106M010ATE080
1	D1	Diode, LED, Green		Wurth Electronics	150080GS75000
2	D101, D102	Diode, Zener, 2V, 500mW		ON Semiconductor	MMSZ4679T1G
4	D501, D502, D503, D504	Diode, Schottky, 100V, 150mA		STMicroelectronics	BAT46WFILM
2	D801, D802	Diode, Schottky, 30V, 1A		Toshiba	CUS10S30,H3F
11	J101, J103, J104, J106, J107, J110, J111, J115, J116, J1003, J1004	Connector, Banana		Keystone Electronics	575-8
24	J102, J105, J108, J109, J112, J113, J114, J801, J806, J807, J901, J902, J903, J1001, J1002, J1005, J1101, J1102, J1103, J1104, J1105, J1106, J1107, J1108	Connector, SMA		TE Connectivity AMP	5-1814832-2
3	J501, J502, J503	Connector, Triax		Bel Trompeter	CBJ157
4	J802, J803, J808, J809	Connector, Safety Banana, Red		Pomona Electronics	5103858
4	J804, J805, J810, J811	Connector, Safety Banana, Black		Pomona Electronics	5103847
2	L101, L102	Inductor	4.7uH	Murata	DFE322520FD-4R7M=P2
2	L103, L104	Inductor	100uH	Taiyo Yuden	LBC3225T101KR
23	P1, P201, P202, P204, P205, P208, P209, P212, P213, P302, P502, P503, P611, P612, P613, P614, P615, P802, P803, P807, P902, P903, P1101	Header, 2 pos, 1 row, 100mil		Sullins	PRPC001DAAN-RC
1	P101	Header, 10 pos, 1 row, 100mil		Sullins	PRPC010SAAN-RC
4	P102, P402, P403, P501	Header, 6 pos, 2 row, 100mil		Sullins	PRPC003DAAN-RC
48	P203, P206, P207, P210, P211, P214, P215, P301, P401, P404, P601, P602, P603, P604, P605, P606, P607, P608, P609, P610, P701, P702, P703, P705, P707, P708, P709, P710, P804, P805, P806, P808, P901, P1201, P1202, P1203, P1204, P1205, P1206, P1207, P1208, P1209, P1210, P1211, P1212, P1213, P1214, P1215	Header, 3 pos, 1 row, 100mil		Sullins	PRPC003SAAN-RC
1	P801	Header, 20 pos, 2 row, 100mil		Sullins	PRPC010DAAN-RC
1	R1	Resistor	5.9k	Yageo	RC0603FR-075K9L
2	R1001, R1101	Resistor	1	TE Connectivity	CPF0603B1R0E1
8	R301, R401, R501, R503, R807, R819, R823, R901	Resistor	10	TE Connectivity	2-1625868-7

Figure C.26: Teucer test board bill of materials (BOM) page 2

3	R302, R402, R405	Resistor	6.65k	TE Connectivity	RQ73C1J6K65BTD
12	R303, R403, R406, R601, R602, R603, R604, R605, R606, R607, R608, R625	Resistor	0	Yageo	RC0603JR-070RL
4	R304, R404, R407, R515	Potentiometer	10k	Bourns	3296W-1-103LF
6	R305, R306, R627, R628, R629, R630	Resistor	10k	Yageo	RT0603DRD0710KL
4	R502, R504, R511, R513	Resistor	470	Panasonic	ERA-3AEB471V
2	R505, R509	Potentiometer	1k	Bourns	3296W-1-102LF
7	R507, R508, R512, R518, R519, R522, R525	Resistor	100k	Vishay Beyschlag	MCT0603MD1003DP500
1	R510	Resistor	10k	KOA Speer	RN73H2ATTD1002A05
1	R516	Resistor	95k	Yageo	RT0603DRD0795K3L
2	R517, R524	Potentiometer	100	Susumu	RG1608P-101-B-T5
1	R521	Potentiometer	250k	Bourns	3296W-1-254LF
2	R802, R814	Potentiometer	50	Bourns	3296W-1-500LF
2	R803, R815	Potentiometer	500	Bourns	3296W-1-501LF
2	R804, R816	Potentiometer	5k	Bourns	3296W-1-503RLF
2	R805, R817	Potentiometer	50k	Bourns	3296W-1-503LF
2	R806, R818	Potentiometer	500k	Bourns	3296W-1-504LF
2	R809, R821	Potentiometer	1Meg	TE Connectivity	CRGCQ0603F1M0
2	R824, R826	Resistor	100	Panasonic	ERJ-P06F1000V
2	R825, R827	Resistor	10k	Stackpole Electronics	RNCP0603FTD10K0
30	TP101, TP104, TP108, TP201, TP202, TP205, TP206, TP209, TP210, TP213, TP214, TP301, TP401, TP403, TP501, TP1201, TP1202, TP1203, TP1204, TP1209, TP1210, TP1211, TP1212, TP1217, TP1218, TP1219, TP1220, TP1225, TP1226, TP1227	Test Point, Red		Keystone Electronics	5000
42	TP102, TP105, TP109, TP113, TP203, TP204, TP207, TP208, TP211, TP212, TP215, TP216, TP302, TP402, TP404, TP503, TP511, TP512, TP519, TP520, TP704, TP807, TP808, TP811, TP903, TP906, TP909, TP1004, TP1106, TP1107, TP1110, TP1205, TP1206, TP1207, TP1208, TP1213, TP1214, TP1215, TP1216, TP1221, TP1222, TP1223	Test Point, Black		Keystone Electronics	5001

Figure C.27: Teucer test board bill of materials (BOM) page 3

4	TP103, TP513, TP805, TP809	Test Point, Orange		Keystone Electronics	5003
1	TP112	Test Point, Blue		Keystone Electronics	5117
23	TP502, TP504, TP506, TP507, TP515, TP516, TP517, TP701, TP702, TP703, TP705, TP801, TP904, TP905, TP911, TP1101, TP1102, TP1103, TP1104, TP1105, TP1108, TP1109, TP1111	Test Point, Violet		Keystone Electronics	5119
1	U201	IC, LVR 5V, 1.5A		Texas Instruments	LM7805SX/NOPB
5	U202, U203, U204, U208, U404	IC, LVR, 1.8V, 200mA		Texas Instruments	TPS79318DBVREP
3	U205, U206, U207	IC, LVR, 3.3V, 300mA		Diodes	AP139-33WG-7
3	U301, U401, U403	IC, LVR, Precision, 3V, 5mA		Analog Devices	LT6656AIS6-3#TRMPBF
2	U302, U402	IC, Op Amp, 6.5MHz, Rail-to-Rail		Analog Devices	LTC6256IMS8#PBF
1	U501	IC, LVR, Adjustable, 100mA		Texas Instruments	LM317LZ/LFT7
1	U502	IC, Op Amp, 6.5MHz, Rail-to-Rail		Analog Devices	LTC6082CGN#PBF
1	U503	IC, LVR, Neg. Adjustable, 100mA		Rochester Electronics	LM337LZ/NOPB
2	U601, U602	IC, Digital Isolator, 4 Channel		Analog Devices	ADUM140D0BRZ
1	U603	IC, Inverter, 2 Channel		Texas Instruments	SN74AUC2GU04DCKR
1	U701	Socket, QFN80		3M	280-5205-01
2	U801, U802	IC, Gate Driver, Low-Side, 4A		Texas Instruments	UCC27518DBVR
1	U803	IC, Op Amp, 450MHz, Rail-to-Rail		Texas Instruments	OPA356AID

Figure C.28: Teucer test board bill of materials (BOM) page 4

D Layout Figures

D.1 180-nm Implementation

The Cadence® layouts for individual cells implemented and fabricated in a 180-nm process are shown in Figures D.1 to D.6.

- Figure D.1 – Complementary T-gate with lowest impedance
- Figure D.2 – Complementary T-gate with highest impedance
- Figure D.3 – Pseudo-Differential Switch Driver
- Figure D.4 – Pass device array
- Figure D.5 – CMOTA
- Figure D.6 – RLDOE

D.2 65-nm Implementation

The Cadence® layouts for individual cells implemented in a 65-nm process are shown in Figures D.7 to D.12.

- Figure D.7 – Complementary T-gate with lowest impedance
- Figure D.8 – Complementary T-gate with highest impedance
- Figure D.9 – Pseudo-Differential Switch Driver
- Figure D.10 – Pass device array
- Figure D.11 – CMOTA
- Figure D.12 – RLDOE

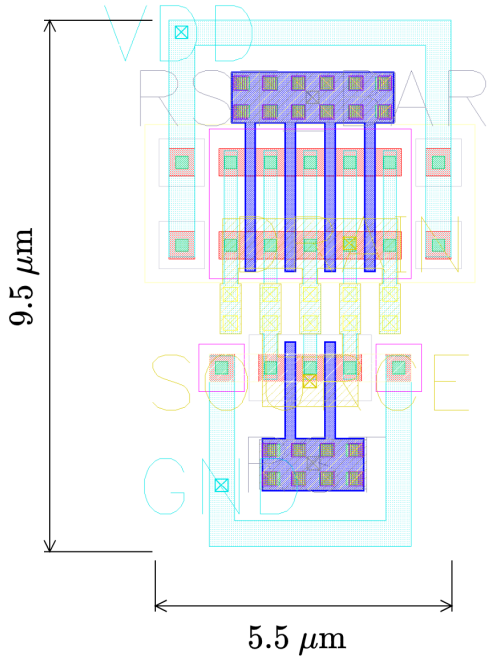


Figure D.1: 180-nm lowest impedance complementary transmission-gate layout

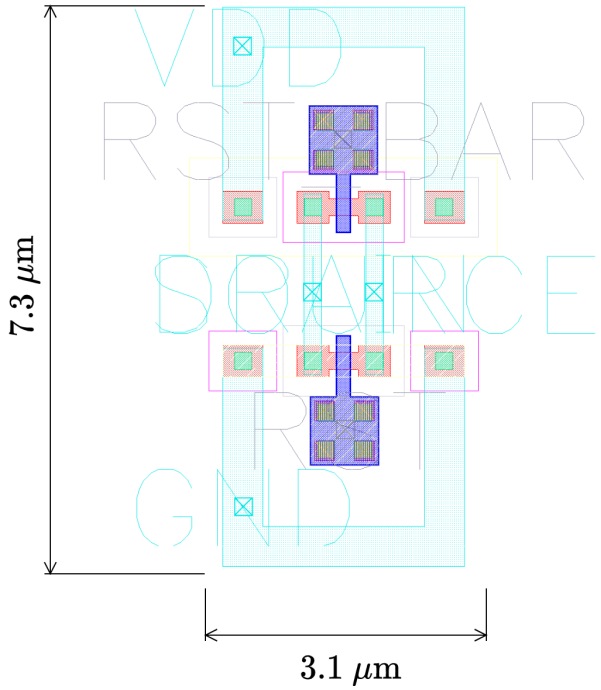


Figure D.2: 180-nm highest impedance complementary transmission-gate layout

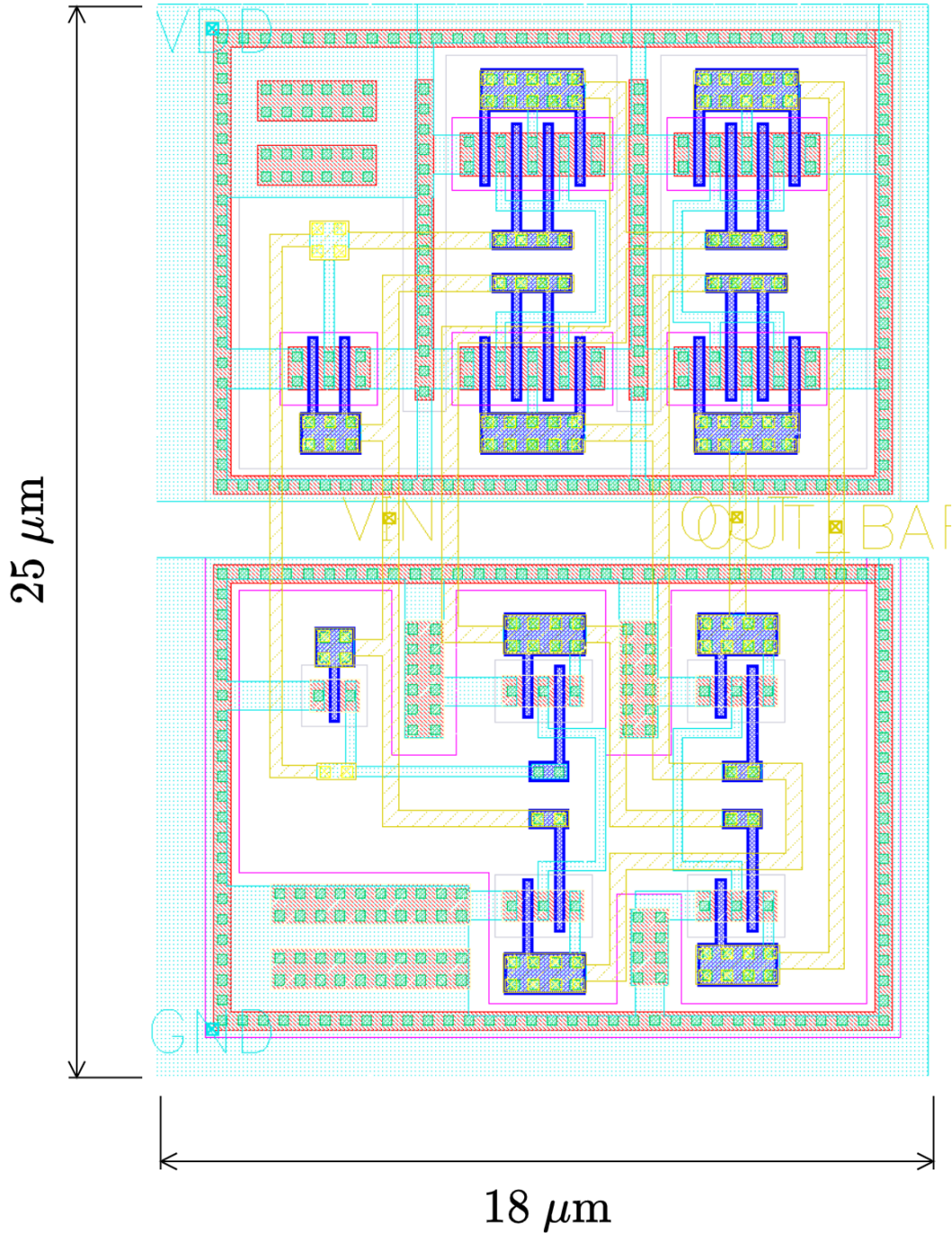


Figure D.3: 180-nm pseudo-differential switch driver layout

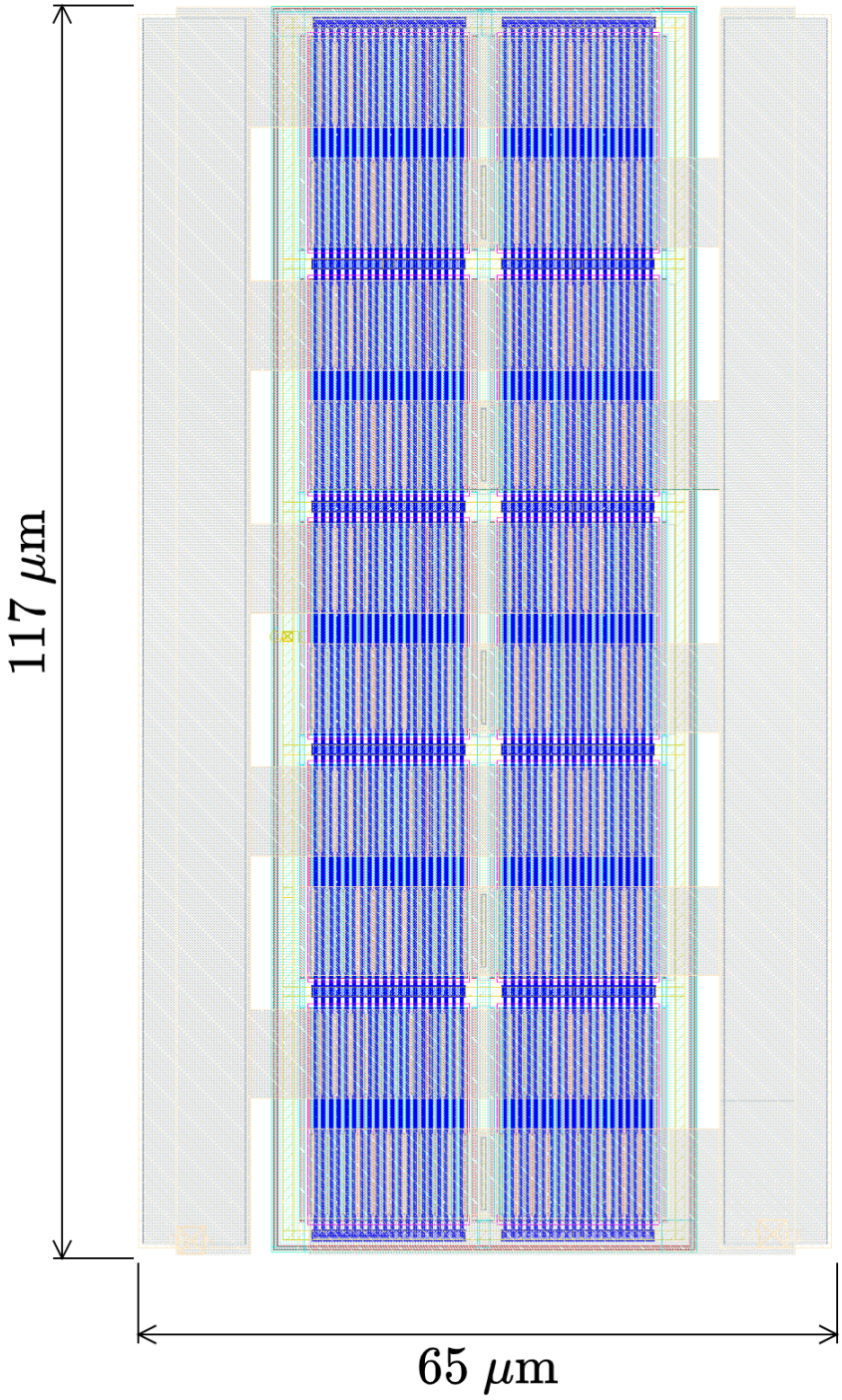


Figure D.4: 180-nm pass device array layout

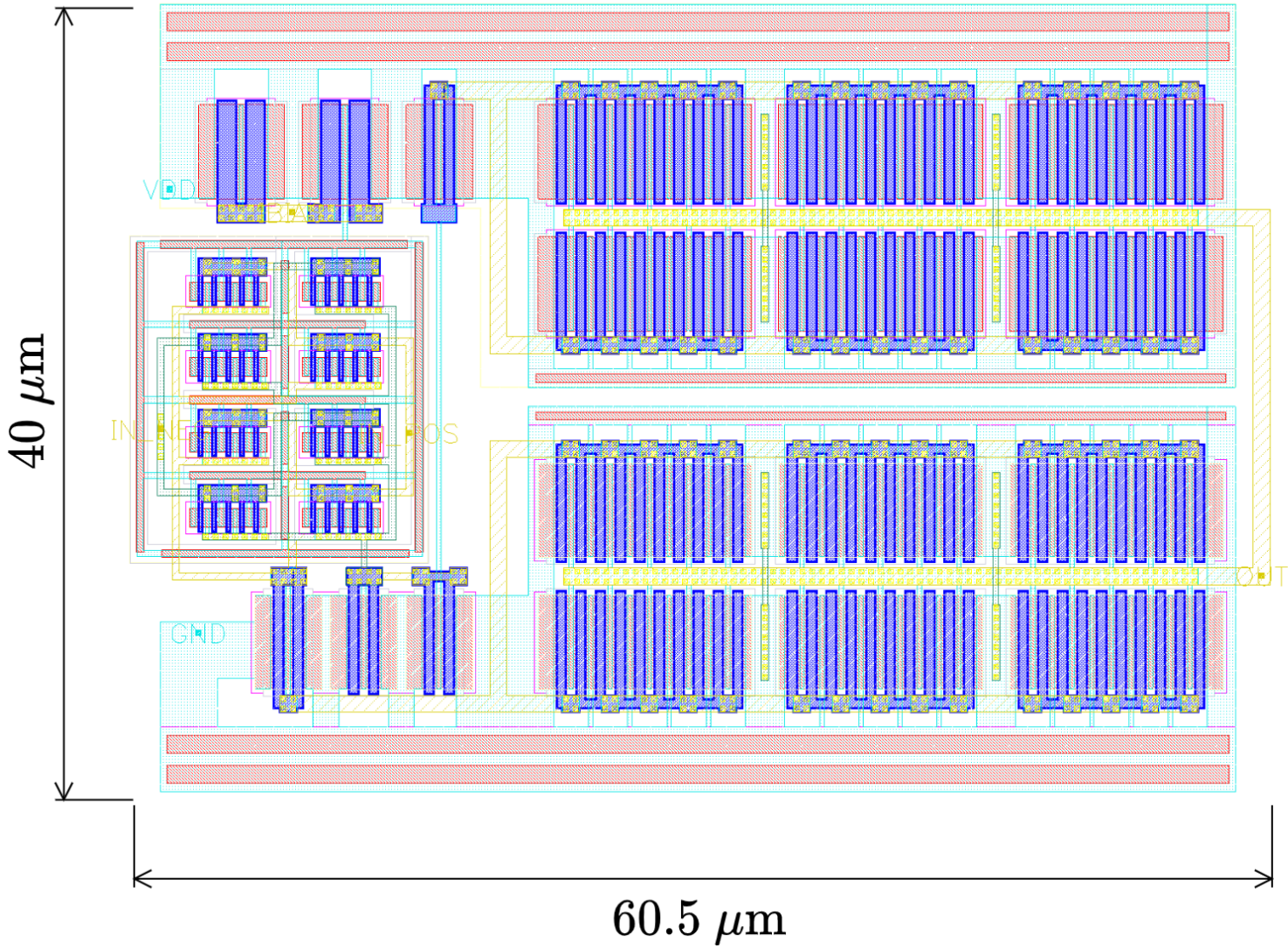


Figure D.5: 180-nm CMOTA layout

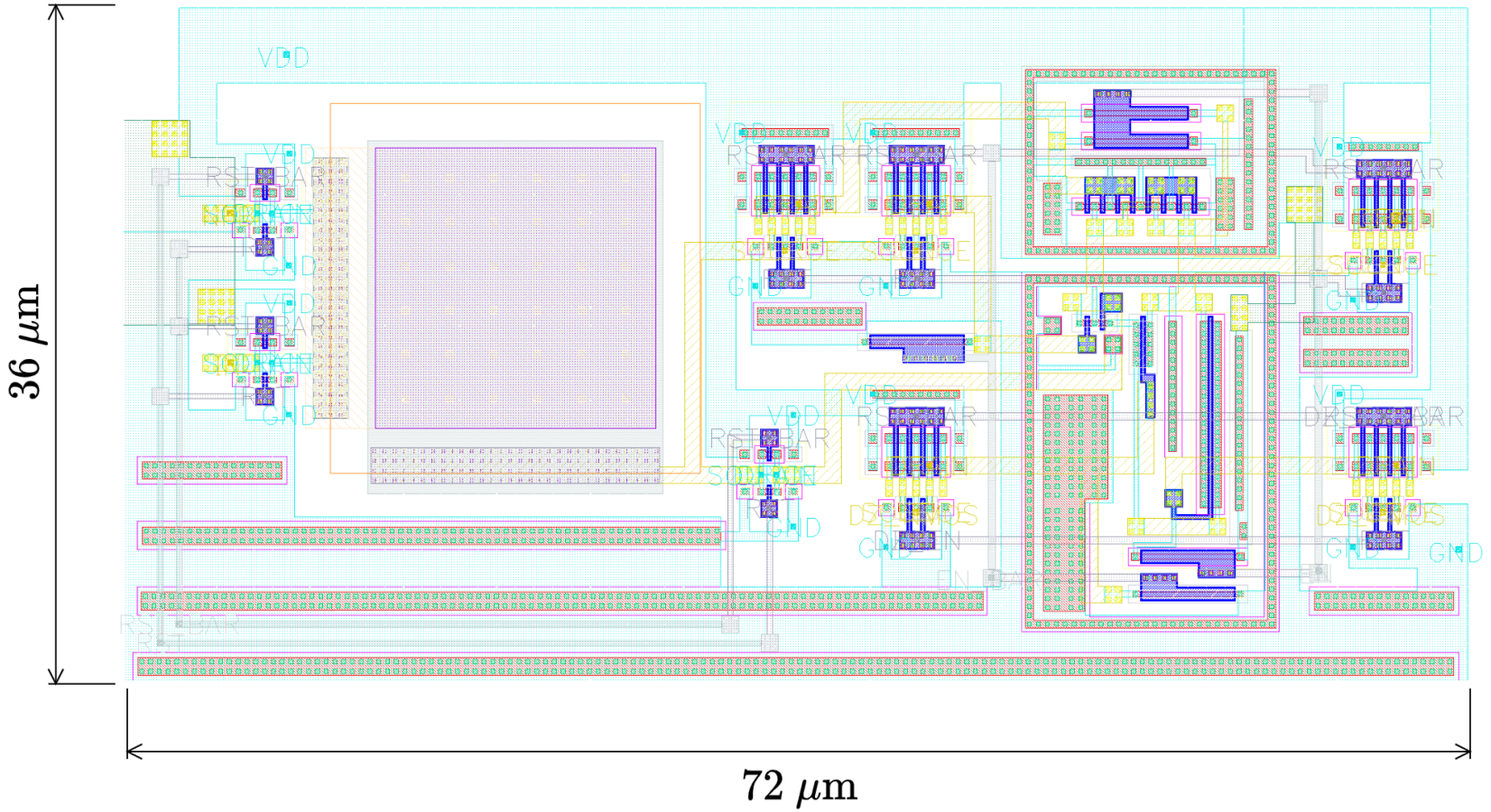


Figure D.6: 180-nm RLDOE transistor-level layout

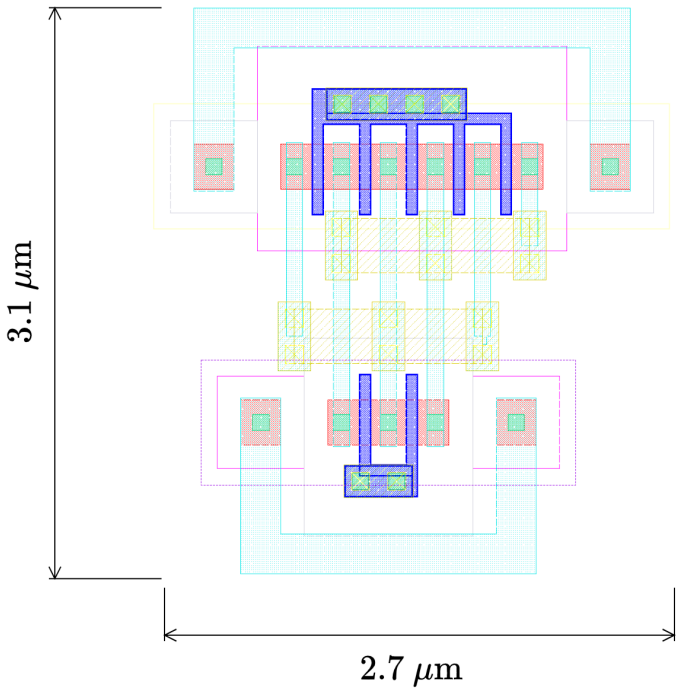


Figure D.7: 65-nm lowest impedance complementary transmission-gate layout

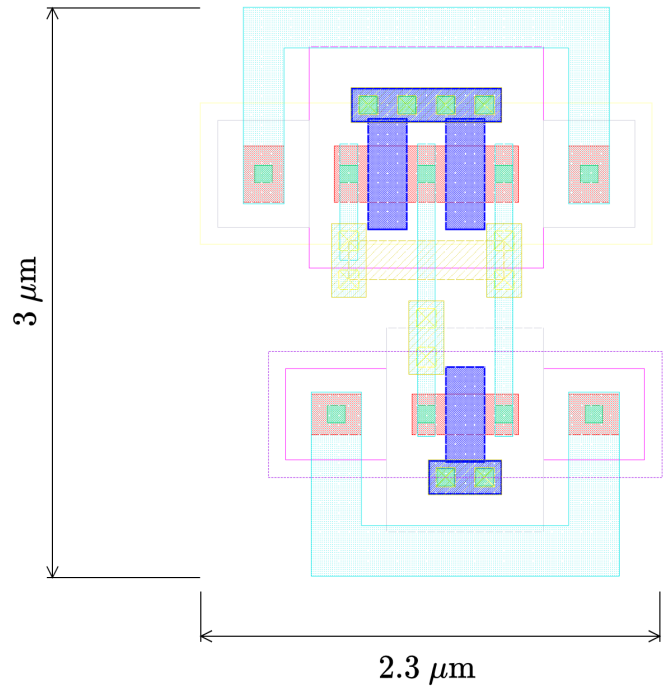


Figure D.8: 65-nm highest impedance complementary transmission-gate layout

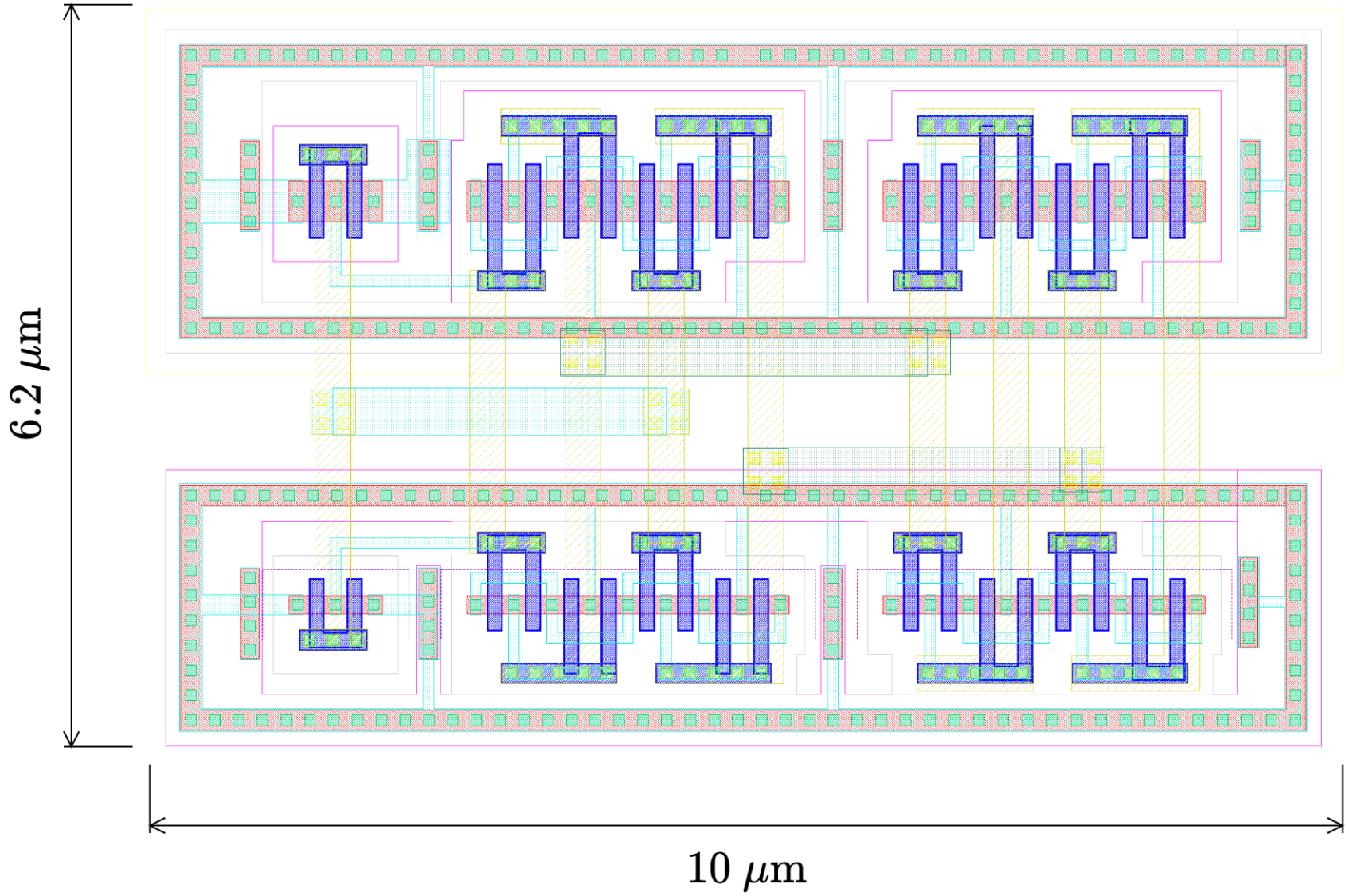


Figure D.9: 65-nm pseudo-differential switch driver layout

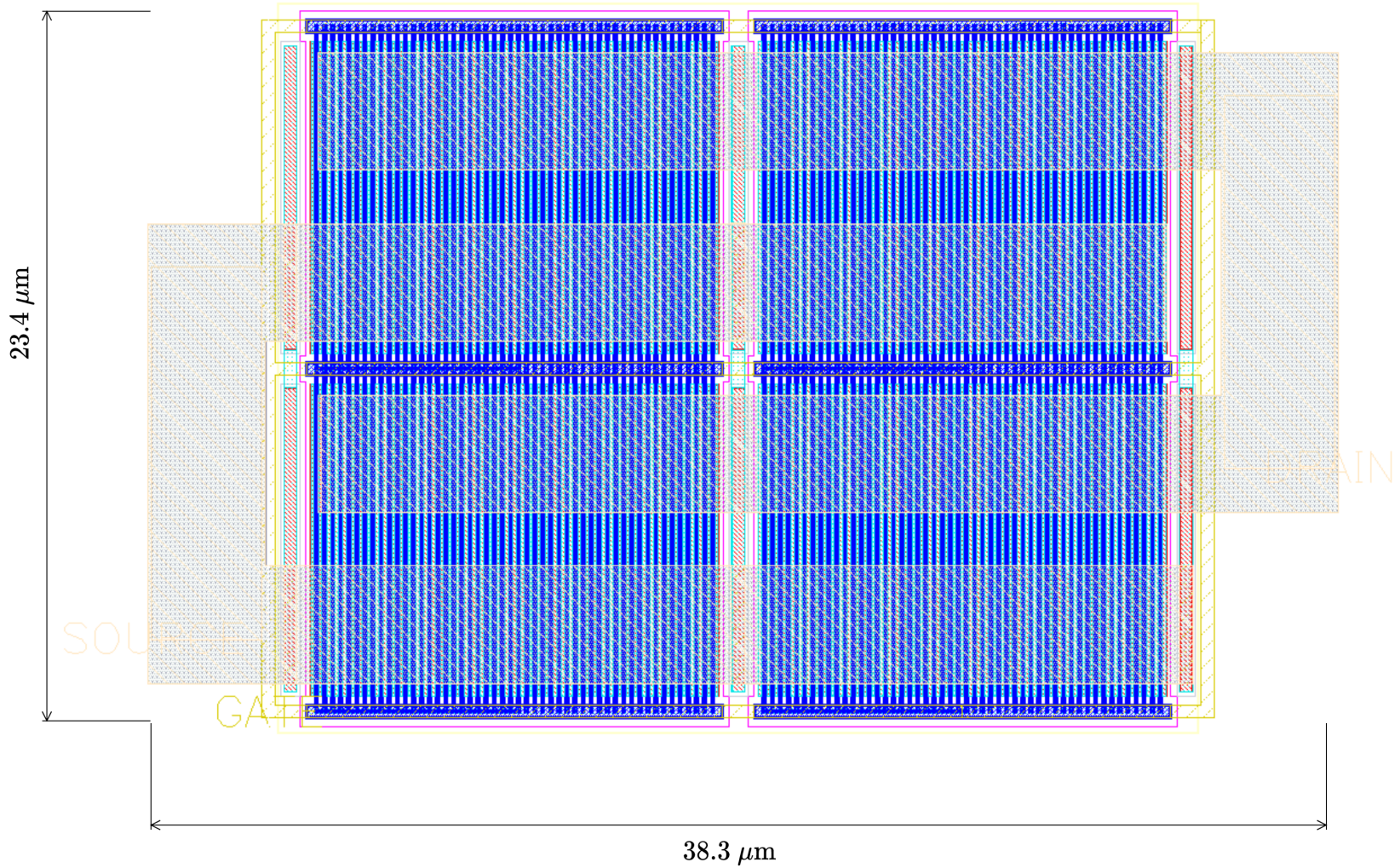


Figure D.10: 65-nm pass device array layout

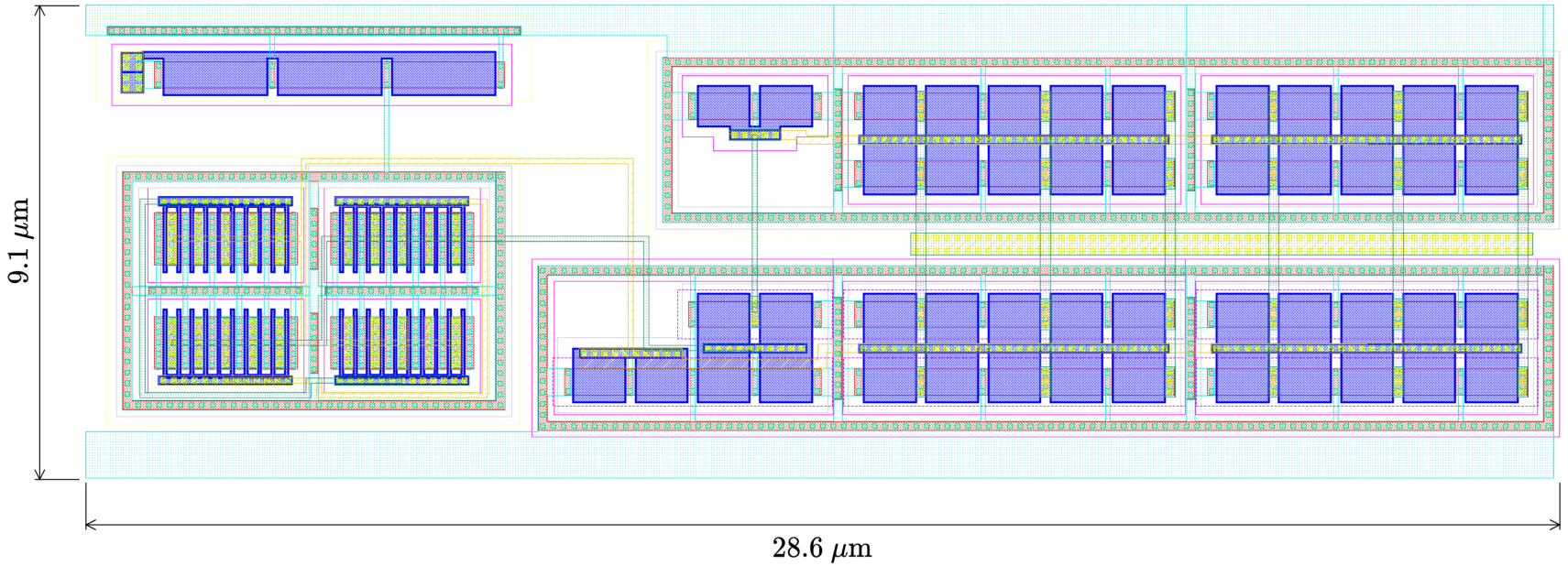


Figure D.11: 65-nm CMOTA layout

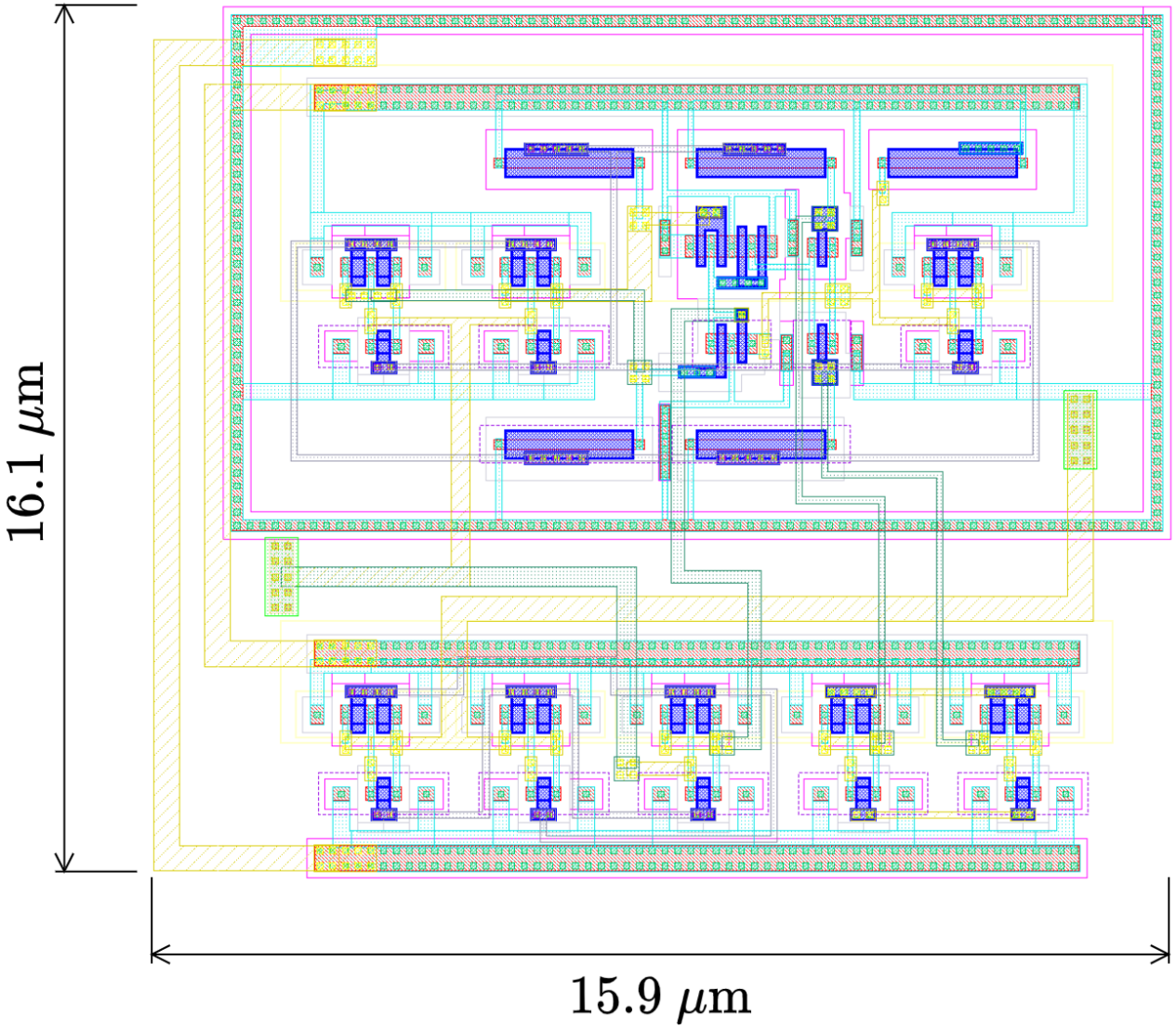


Figure D.12: 65-nm RLDOE layout

E Additional Simulation Figures

E.1 180-nm CMOTA Loop Simulations

The experimental evaluations for the CMOTA LDO loop are shown in Figures E.1 to E.5.

- For $V_{DD} = 1.8\,\mathrm{V}$
  - Figure E.1 Simulated CMOTA loop response between 100 µA to 1 mA load step
  - Figure E.2 Simulated CMOTA loop response between 1 mA to 10 mA load step
  - Figure E.3 Simulated CMOTA loop response between 1 mA to 100 mA load step
- For $V_{DD} = 0.9\,\mathrm{V}$
  - Figure E.4 Simulated CMOTA loop response between 40 µA to 4 mA load step
  - Figure E.5 Simulated CMOTA loop response between 400 µA to 40 mA load step

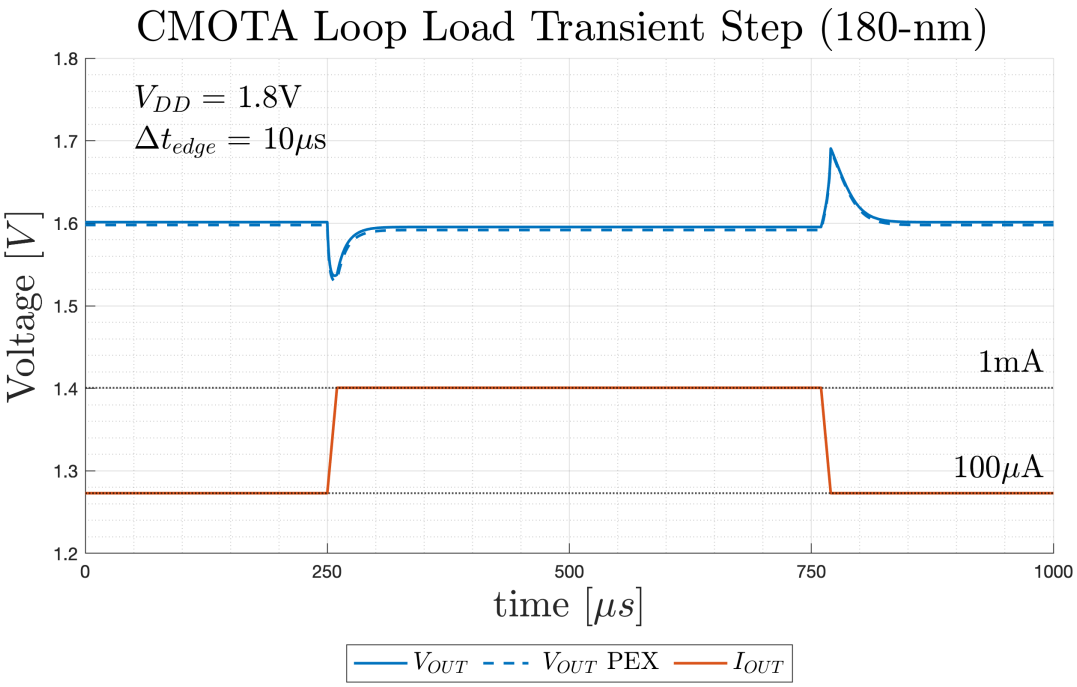


Figure E.1: Simulated CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V

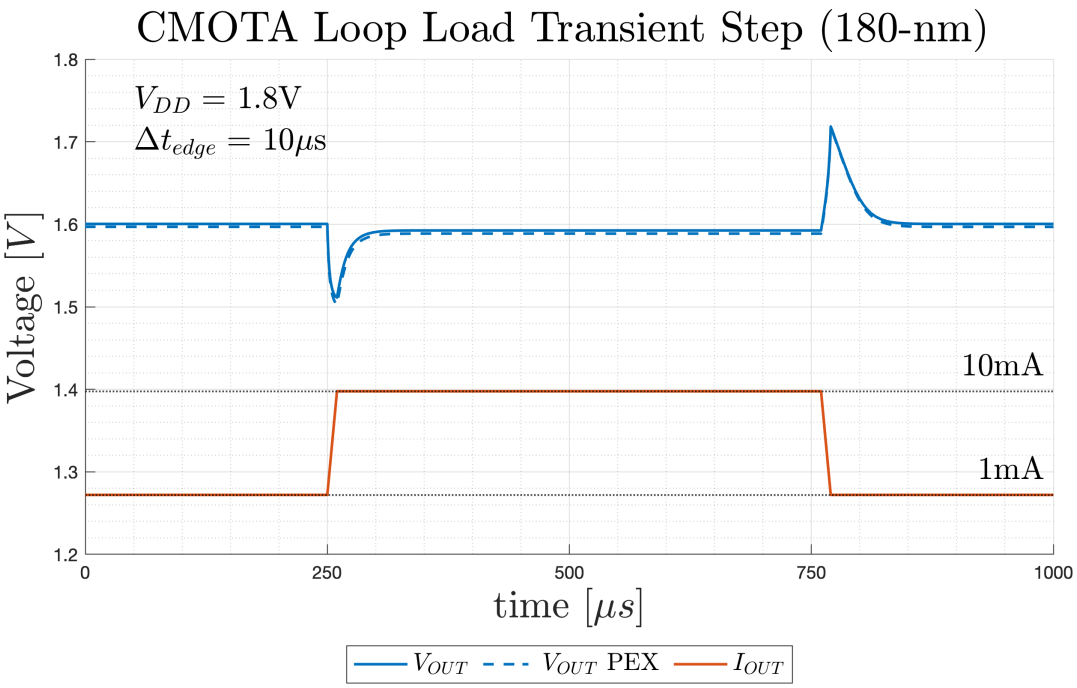


Figure E.2: Simulated CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V

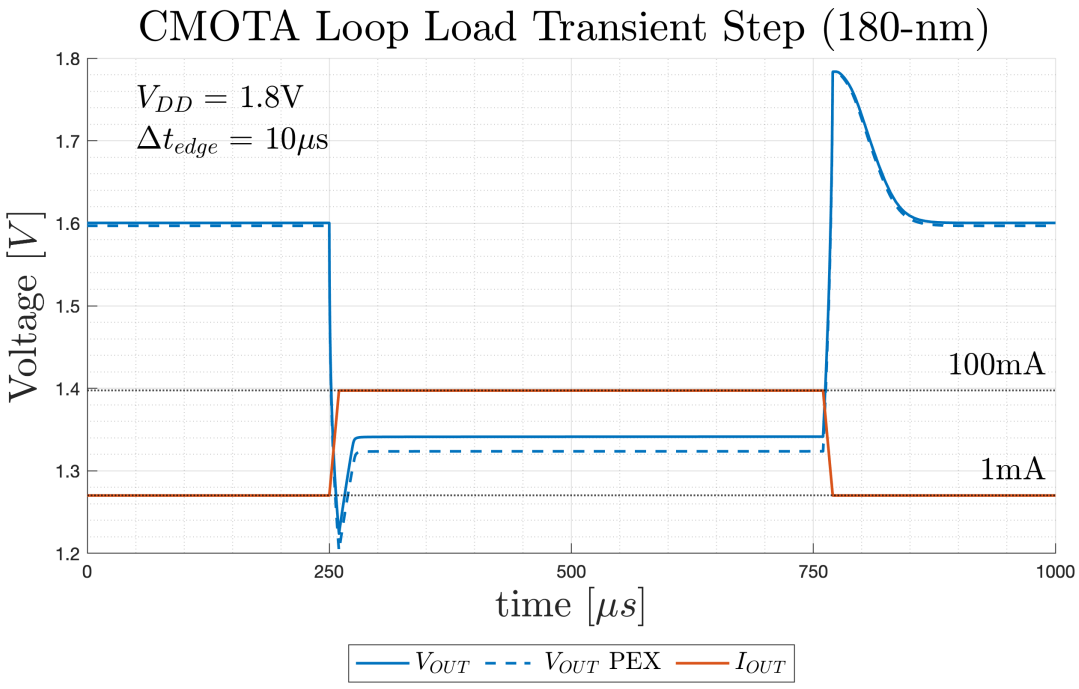


Figure E.3: Simulated CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V

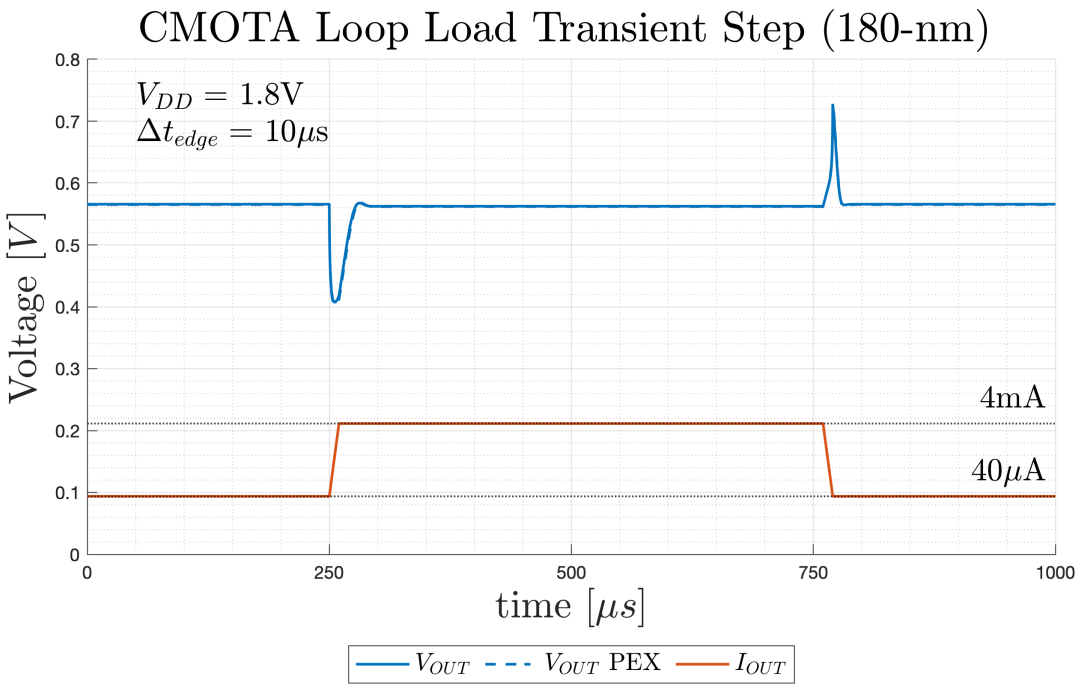


Figure E.4: Simulated CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V

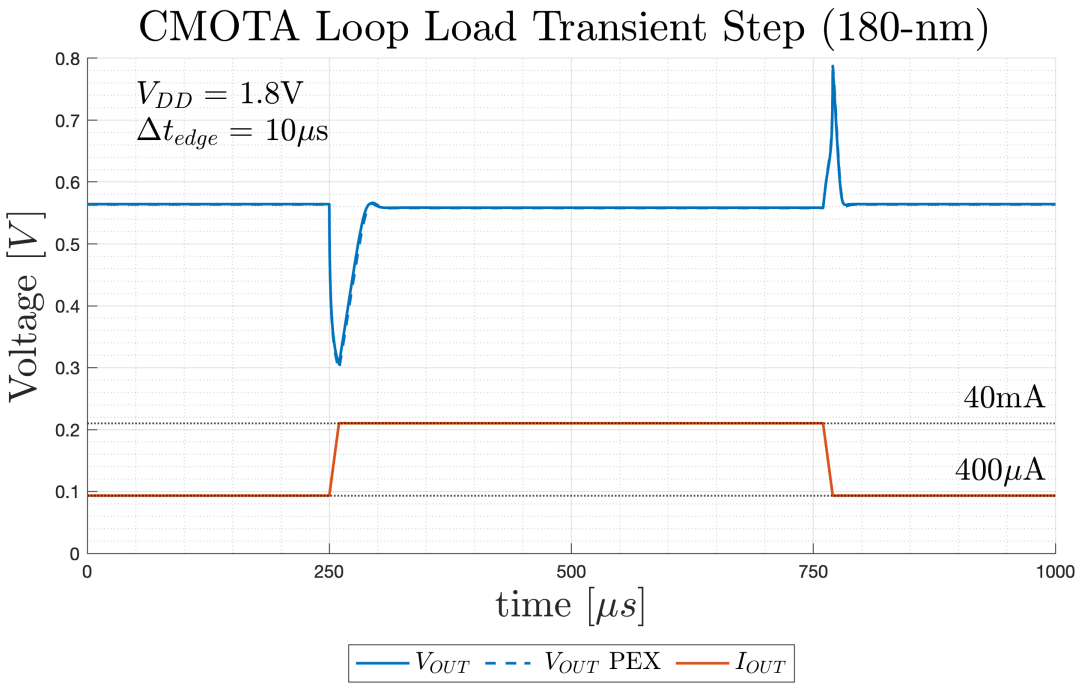


Figure E.5: Simulated CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ V

E.2 180-nm RLDOE Loop Evaluations

The experimental evaluations for the CMOTA LDO loop are shown in Figures E.6 to E.9

- For $V_{DD} = 1.8\,\text{V}$
  - Figure E.6 Simulated RLDOE loop response between 1 mA to 50 mA load step
  - Figure E.7 Simulated RLDOE loop response between 1 mA to 100 mA load step
- For $V_{DD} = 0.9\,\text{V}$
  - Figure E.8 Simulated RLDOE loop response between 500 µA to 50 mA load step
  - Figure E.9 Simulated RLDOE loop response between 5 mA to 50 mA load step

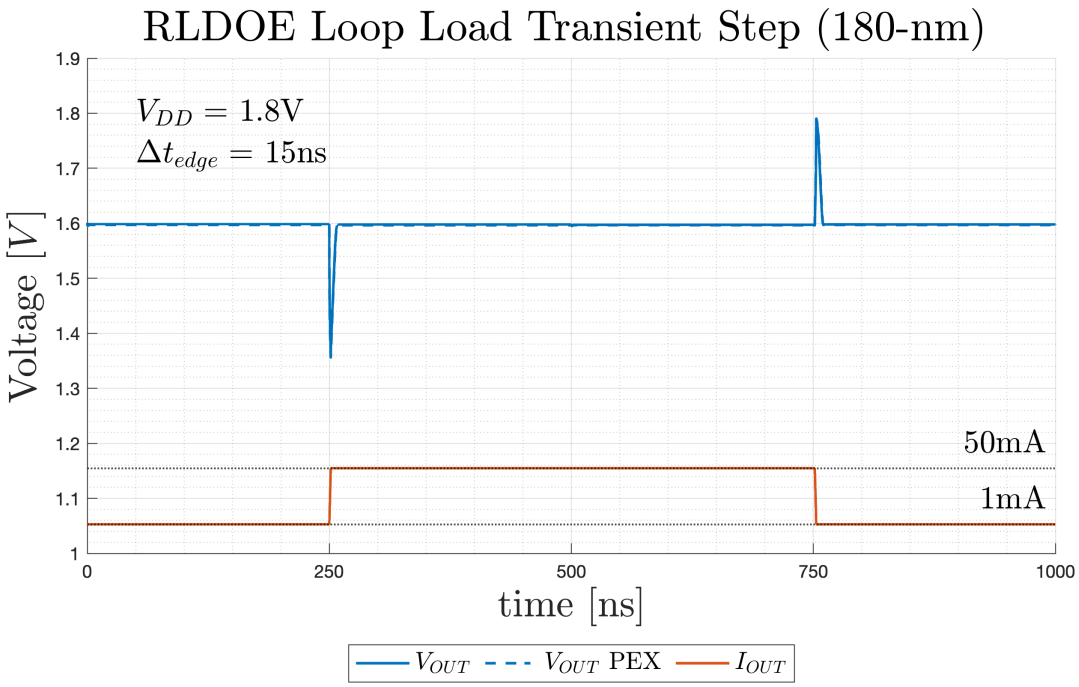


Figure E.6: Simulated CMOTA loop load step 1 mA to 50 mA with $V_{DD} = 1.8$ V

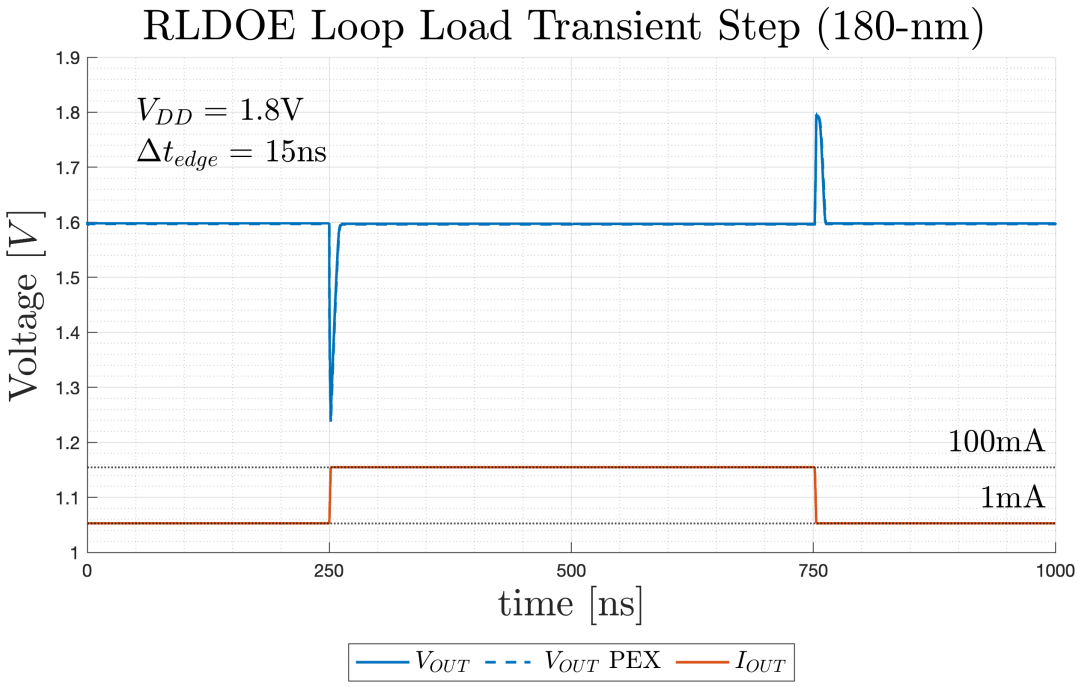


Figure E.7: Simulated RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V

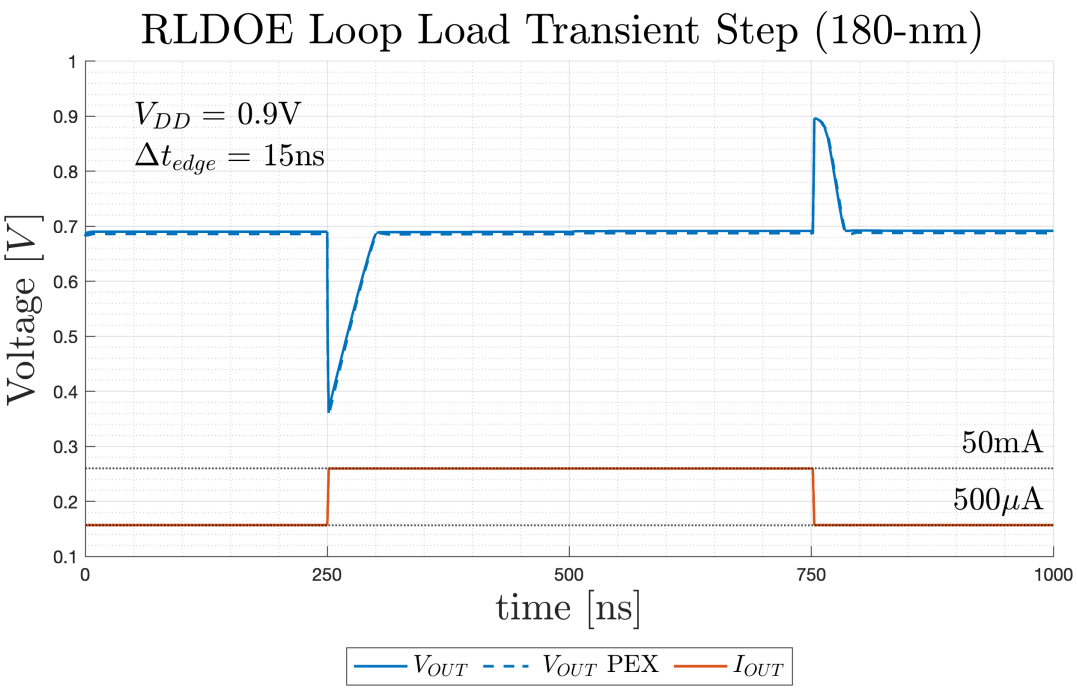


Figure E.8: Simulated CMOTA loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V

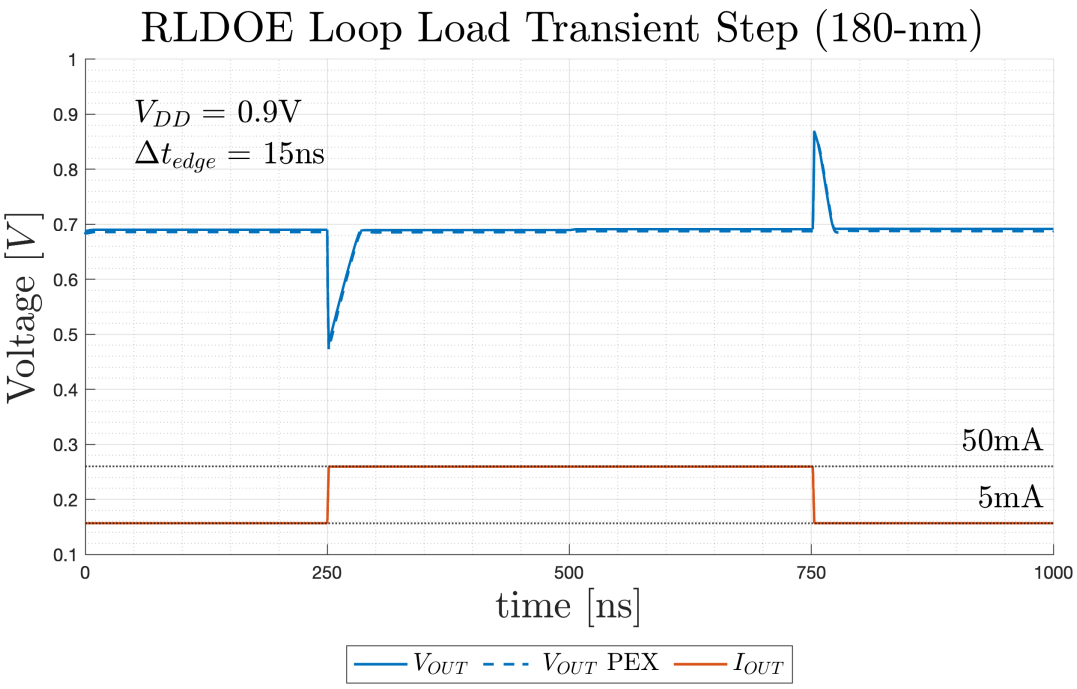


Figure E.9: Simulated CMOTA loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V

E.3 65-nm Design Simulations

The design simulations for individual test cells and small circuits implemented in a 65-nm process are shown in Figures E.10 to E.13.

- Figure E.10 – Complementary T-gate with lowest impedance R_{ds} evaluation
- Figure E.11 – Complementary T-gate with highest impedance R_{ds} evaluation
- Figure E.12 – Pseudo-Differential Switch Driver transition waveforms
- Figure E.13 – CMOTA loop transfer curves
- Figure E.14 – CMOTA-based LDO loop power supply rejection
- Figure E.15 – RLDOE loop power supply rejection

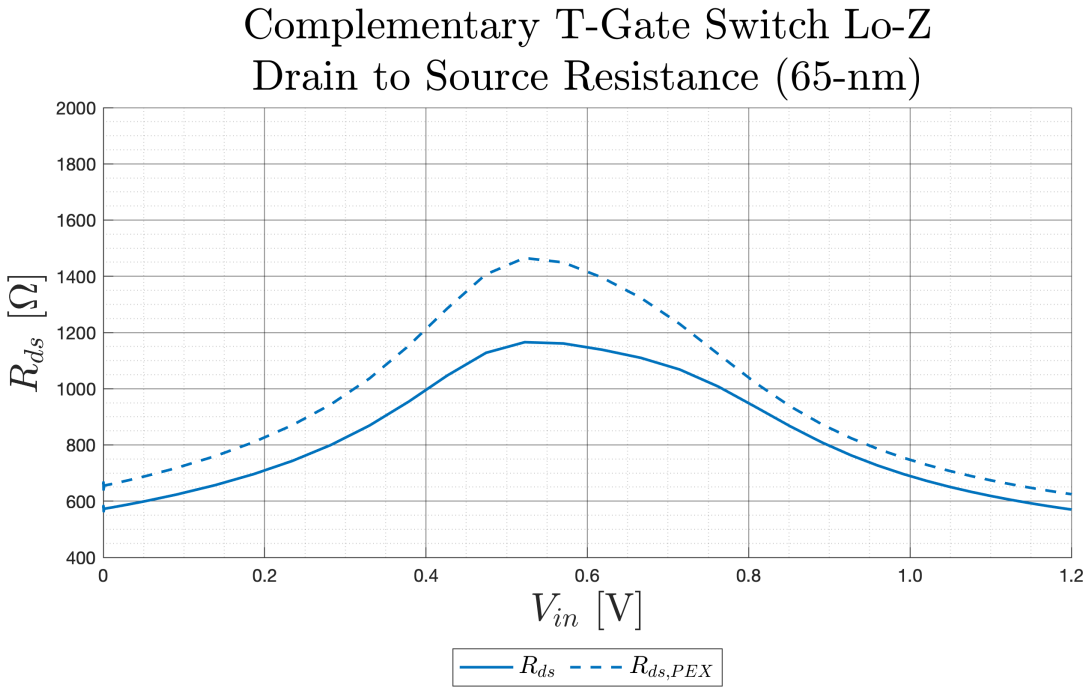


Figure E.10: 65-nm simulated low resistance complementary transmission-gate R_{DS} values for the range of input voltage with post-layout extraction (PEX)

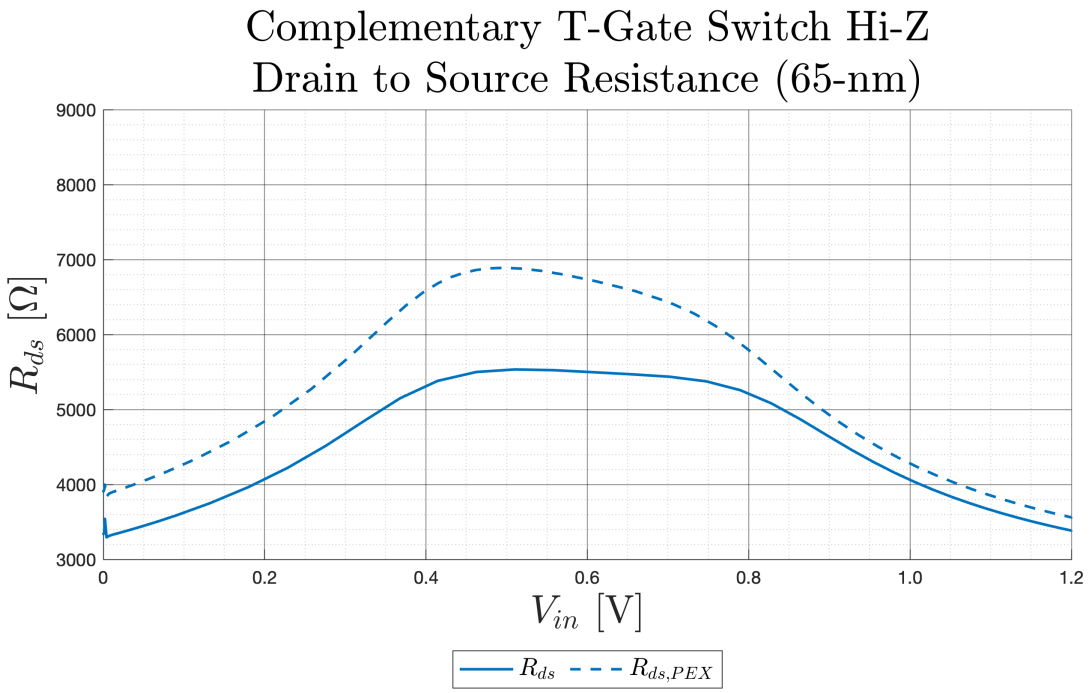


Figure E.11: caption[65-nm simulated high resistance complementary transmission-gate R_{DS} values for the range of input voltage with post-layout extraction (PEX)

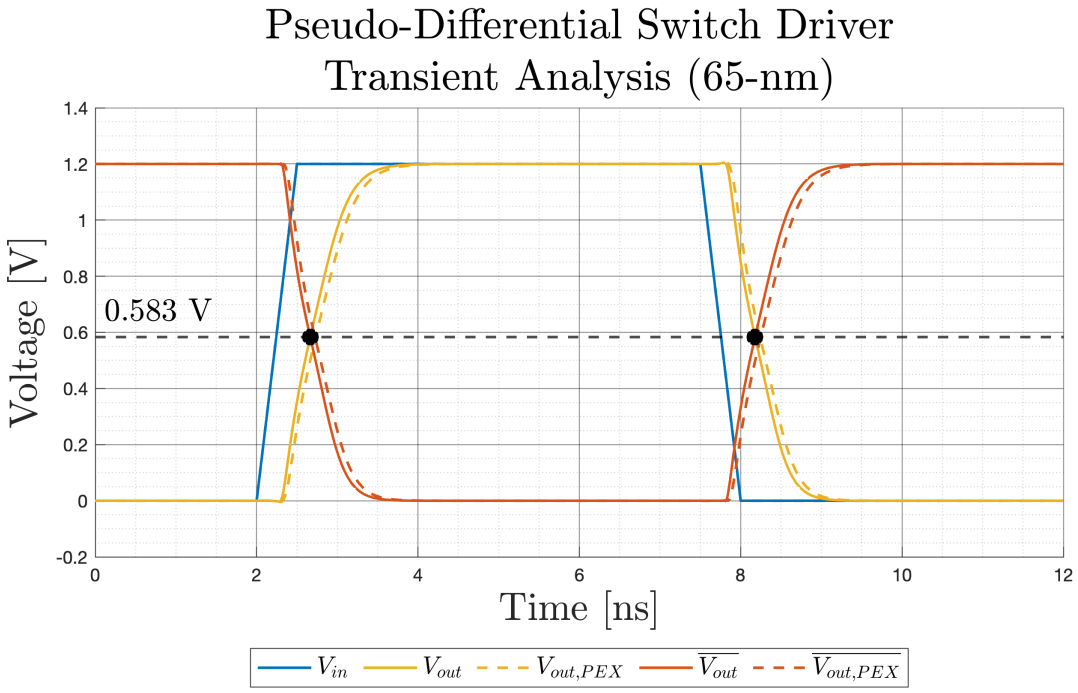


Figure E.12: 65-nm simulated pseudo-differential switch driver transition waveforms with post-layout extraction (PEX)

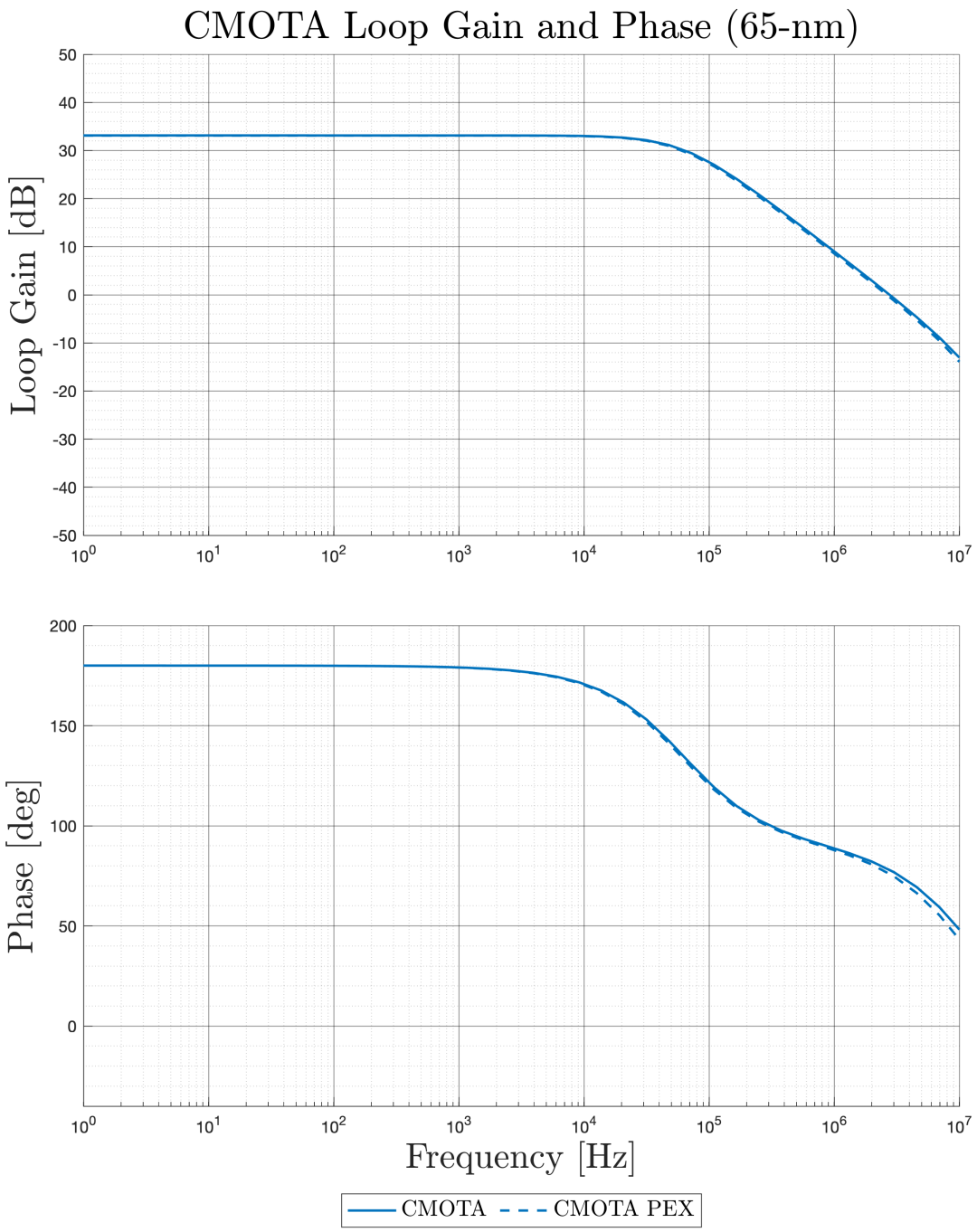


Figure E.13: 65-nm simulated loop gain analysis of CMOTA error amplifier with post-layout parasitic extraction (PEX)

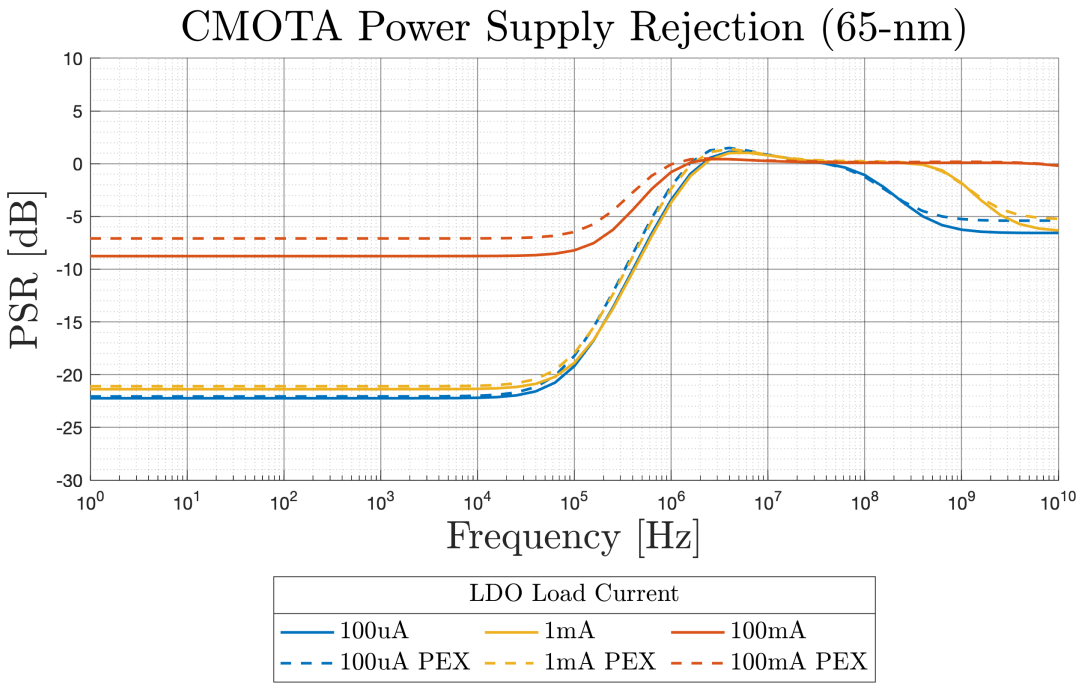


Figure E.14: 65-nm simulated power supply rejection (PSR) performance of the CMOTA loop

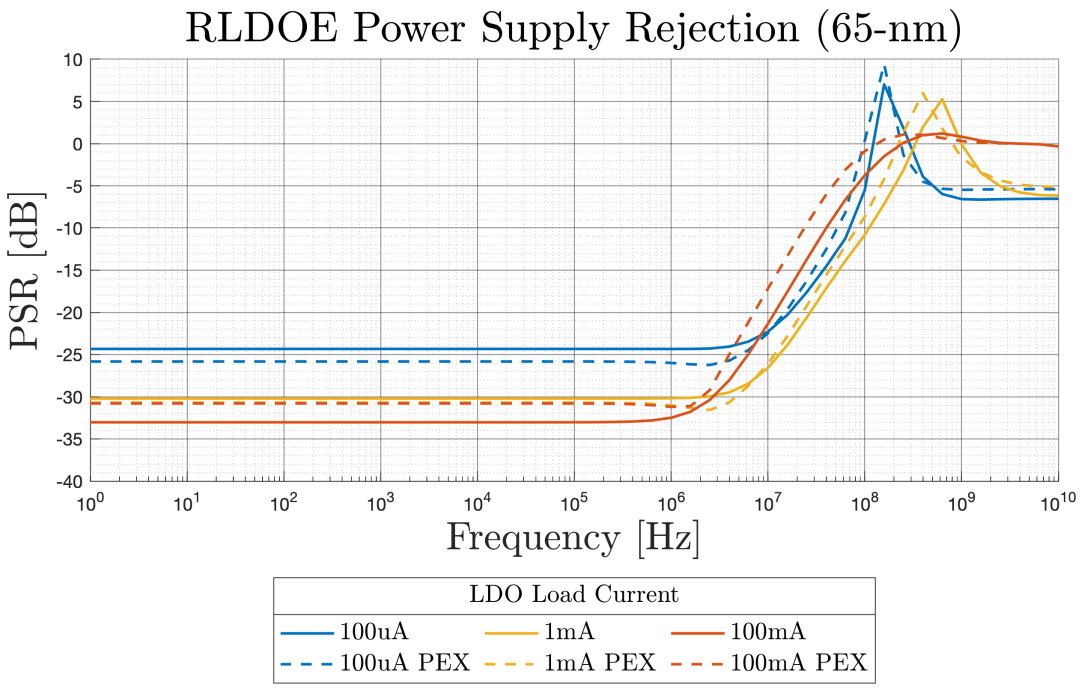


Figure E.15: 65-nm simulated power supply rejection (PSR) performance of the RLDOE loop

E.4 65-nm RLDOE Loop Evaluations

The experimental evaluations for the CMOTA LDO loop are summarized and compared to those from the 180-nm simulations in Table E.1. The current load step response waveforms are shown in Figures E.16 to E.19

- For $V_{DD} = 1.2\,\text{V}$
  - Figure E.16 Simulated RLDOE loop response between 1 mA to 50 mA load step
  - Figure E.17 Simulated RLDOE loop response between 1 mA to 100 mA load step
- For $V_{DD} = 0.6\,\text{V}$
  - Figure E.18 Simulated RLDOE loop response between 500 µA to 50 mA load step
  - Figure E.19 Simulated RLDOE loop response between 5 mA to 50 mA load step

Table E.1: Simulated RLDOE-Loop Current Load Step Results

Evaluation	**Parameters**	**Unit**	**180-nm**		**65-nm**	
			Initial	PEX	Initial	PEX
RLDOE Loop Test Configurations	I_Q	[µA]	68.2		36.4	
	$V_{\max}$	[V]	1.8		1.2	
	$t_{\Delta edge}$	[ns]	15		15	
RLDOE Loop Current Load Step 1 mA to 50 mA $V_{DD} = V_{\max}$ $V_{REF} = V_{DD} - 0.2\,\mathrm{V}$	$V_{DO(RMS)}$	[mV]	201	203	97.6	100
	V_{OS}	[mV]	190	192	81.2	87.3
	$T_{OS,SETTLE}$	[ns]	10	10.3	2.7	3.4
	V_{US}	[mV]	231	241	54.7	67.5
	$T_{US,SETTLE}$	[ns]	10	11.6	18	19
RLDOE Loop Current Load Step 1 mA to 100 mA $V_{DD} = V_{\max}$ $V_{REF} = V_{DD} - 0.2\,\mathrm{V}$	$V_{DO(RMS)}$	[mV]	202	203	97.6	99
	V_{OS}	[mV]	199	200	91.8	97
	$T_{OS,SETTLE}$	[ns]	13	14.3	33.5	34
	V_{US}	[mV]	350	362	90.3	109.4
	$T_{US,SETTLE}$	[ns]	13	16.1	21	25
RLDOE Loop Current Load Step 500 µA to 10 mA $V_{DD} = 0.5 \cdot V_{\max}$ $V_{REF} = V_{DD} - 0.2\,\mathrm{V}$	$V_{DO(RMS)}$	[mV]	110	114	107	108
	V_{OS}	[mV]	176	175	101	107
	$T_{OS,SETTLE}$	[ns]	21.7	38.1	76.2	87.5
	V_{US}	[mV]	208	205	223	269
	$T_{US,SETTLE}$	[ns]	40.4	51	81.7	95.3
RLDOE Loop Current Load Step 5 mA to 50 mA $V_{DD} = 0.5 \cdot V_{\max}$ $V_{REF} = V_{DD} - 0.2\,\mathrm{V}$	$V_{DO(RMS)}$	[mV]	110	119	108	109
	V_{OS}	[mV]	204	208	58.1	78.3
	$T_{OS,SETTLE}$	[ns]	42.8	59.2	83	86
	V_{US}	[mV]	322	318	104.4	140
	$T_{US,SETTLE}$	[ns]	57.2	81.2	82	89

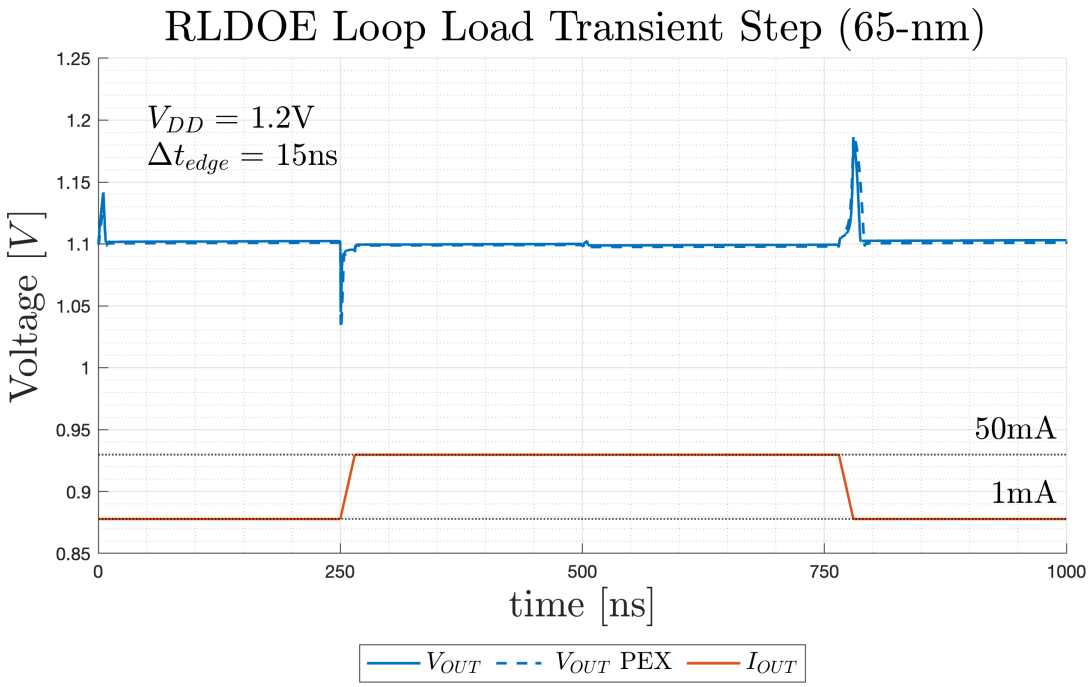


Figure E.16: Simulated CMOTA loop load step 1 mA to 50 mA with $V_{DD} = 1.2$ V

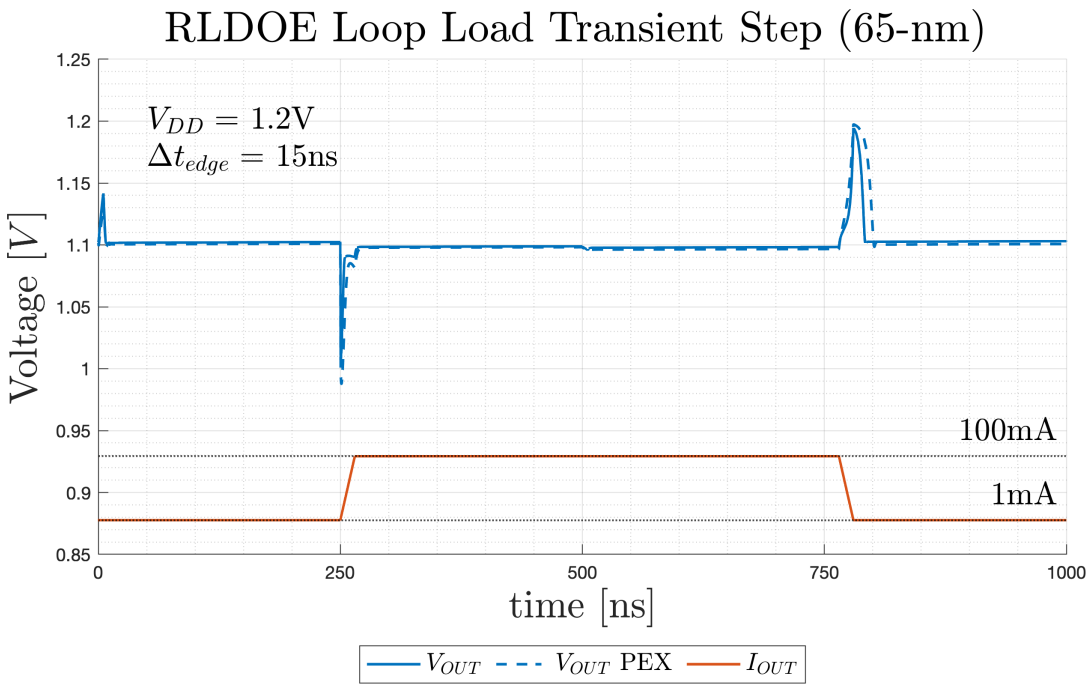


Figure E.17: Simulated RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.2$ V

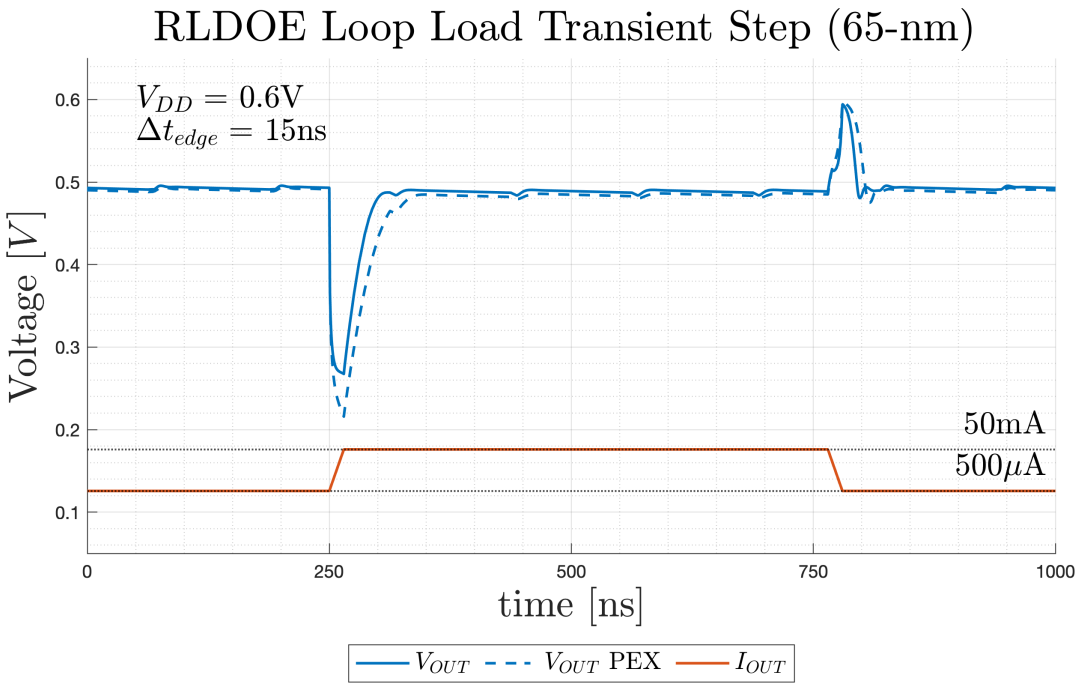


Figure E.18: Simulated CMOTA loop load step 500 µA to 50 mA with $V_{DD} = 0.6$ V

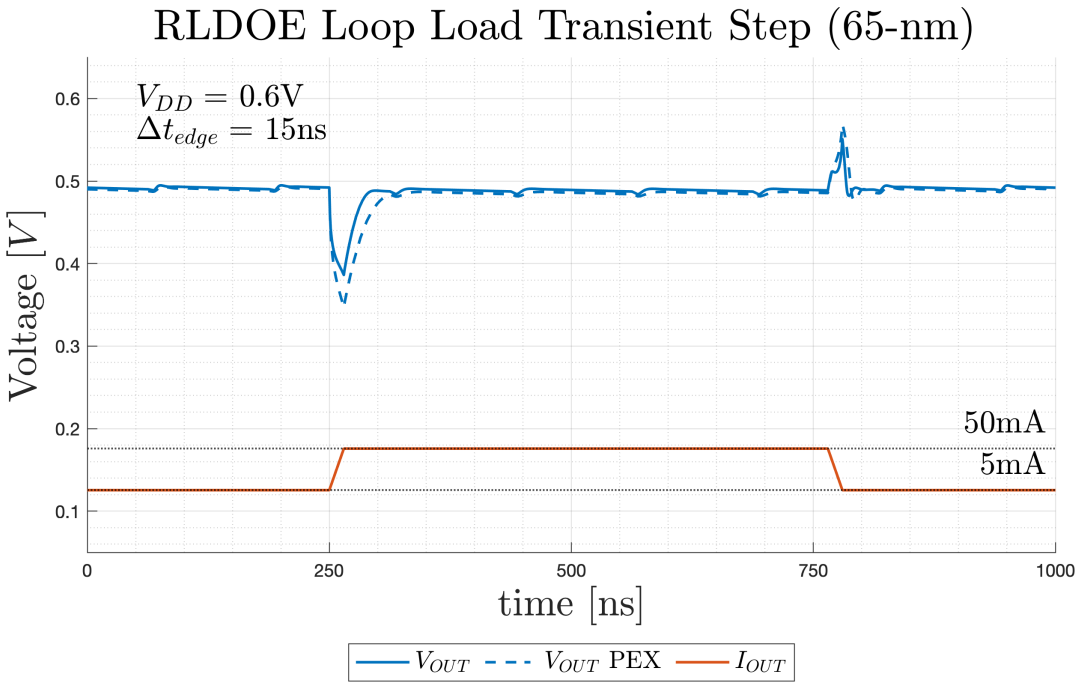


Figure E.19: Simulated CMOTA loop load step 5 mA to 50 mA with $V_{DD} = 0.6$ V

E.5 65-nm CMOTA Loop Simulations

The experimental evaluations for the CMOTA LDO loop are summarized and compared to those from the 180-nm simulations in Table E.2. The current load step response waveforms are shown in Figures E.1 to E.3, E.23 and E.24.

- For $V_{DD} = 1.8\,\text{V}$
  - Figure E.20 Simulated CMOTA loop response between 100 µA to 1 mA load step
  - Figure E.21 Simulated CMOTA loop response between 1 mA to 10 mA load step
  - Figure E.22 Simulated CMOTA loop response between 1 mA to 100 mA load step
- For $V_{DD} = 0.9\,\text{V}$
  - Figure E.23 Simulated CMOTA loop response between 40 µA to 4 mA load step
  - Figure E.24 Simulated CMOTA loop response between 400 µA to 40 mA load step

Table E.2: Simulated CMOTA-Loop Current Load Step Results

Evaluation	Parameters	Unit	180-nm		65-nm	
			Initial	PEX	Initial	PEX
CMOTA Loop Test Configurations	I_Q	[µA]	0.380		0.894	
	$V_{\max}$	[V]	1.8		1.2	
	$t_{\Delta edge}$	[µs]	10		1	
CMOTA Loop Current Load Step 100 µA to 1 mA $V_{DD} = V_{\max}$ $V_{REF} = V_{DD} - 0.2\,\mathrm{V}$	$V_{DO(RMS)}$	[mV]	199	208	92	92
	V_{OS}	[mV]	94.8	97	69.3	72.7
	$T_{OS,SETTLE}$	[µs]	86	100	0.767	0.896
	V_{US}	[mV]	64.7	74.8	74.5	85.8
	$T_{US,SETTLE}$	[µs]	77	82	1.1	1.1
CMOTA Loop Current Load Step 1 mA to 10 mA $V_{DD} = V_{\max}$ $V_{REF} = V_{DD} - 0.2\,\mathrm{V}$	$V_{DO(RMS)}$	[mV]	200	203	101.5	101.7
	V_{OS}	[mV]	126	128	80	82.2
	$T_{OS,SETTLE}$	[µs]	105	120	0.75	0.913
	V_{US}	[mV]	89.2	94	94.3	107.1
	$T_{US,SETTLE}$	[µs]	75	114	0.72	0.965
CMOTA Loop Current Load Step 1 mA to 100 mA $V_{DD} = V_{\max}$ $V_{REF} = V_{DD} - 0.2\,\mathrm{V}$	$V_{DO(RMS)}$	[mV]	200	203	102	102
	V_{OS}	[mV]	183.7	185	99.3	99.6
	$T_{OS,SETTLE}$	[µs]	127	130	1.076	1.227
	V_{US}	[mV]	117	118	282	309
	$T_{US,SETTLE}$	[µs]	50	44.7	1.85	2.67
CMOTA Loop Current Load Step 40 µA to 4 mA $V_{DD} = 0.5 \cdot V_{\max}$ $V_{REF} = V_{DD} - 0.2\,\mathrm{V}$	$V_{DO(RMS)}$	[mV]	335	335	190.2	189.6
	V_{OS}	[mV]	160	164	176.9	179.2
	$T_{OS,SETTLE}$	[µs]	28.7	32.8	0.954	1.067
	V_{US}	[mV]	158	155	189.9	205.1
	$T_{US,SETTLE}$	[µs]	41.8	46.8	0.928	1.294
CMOTA Loop Current Load Step 400 µA to 40 mA $V_{DD} = 0.5 \cdot V_{\max}$ $V_{REF} = V_{DD} - 0.2\,\mathrm{V}$	$V_{DO(RMS)}$	[mV]	336	342	198	198
	V_{OS}	[mV]	216	223	189.7	191.1
	$T_{OS,SETTLE}$	[µs]	32.7	35.8	1.088	1.282
	V_{US}	[mV]	253	260	243.2	274.5
	$T_{US,SETTLE}$	[µs]	58.5	73.5	1.14	1.358

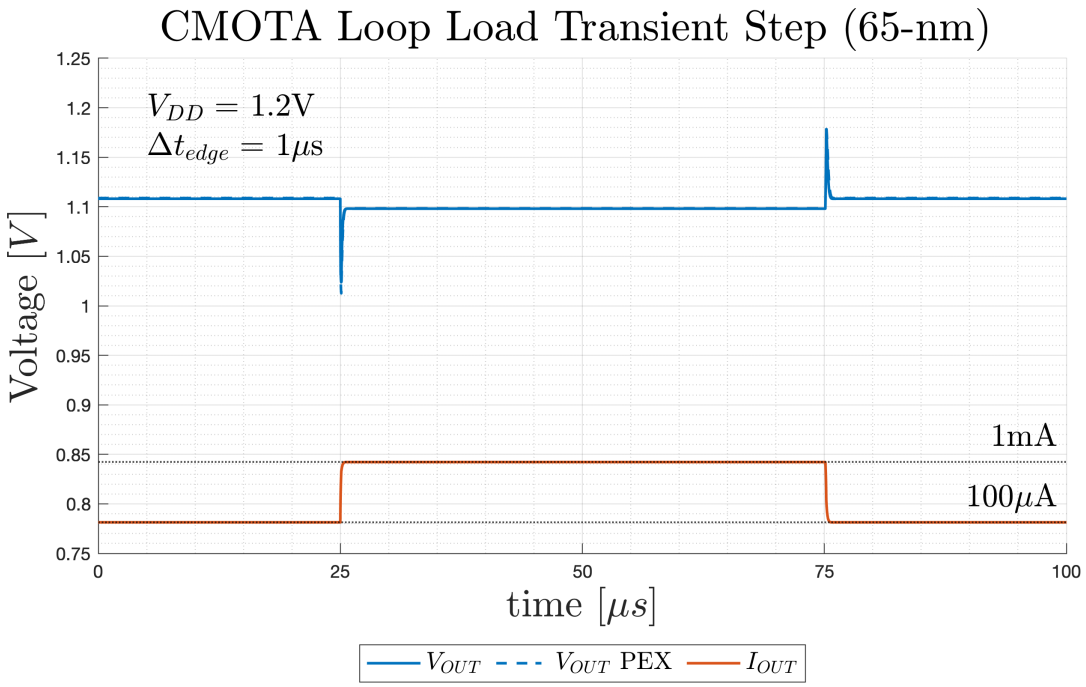


Figure E.20: Simulated CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.2$ V

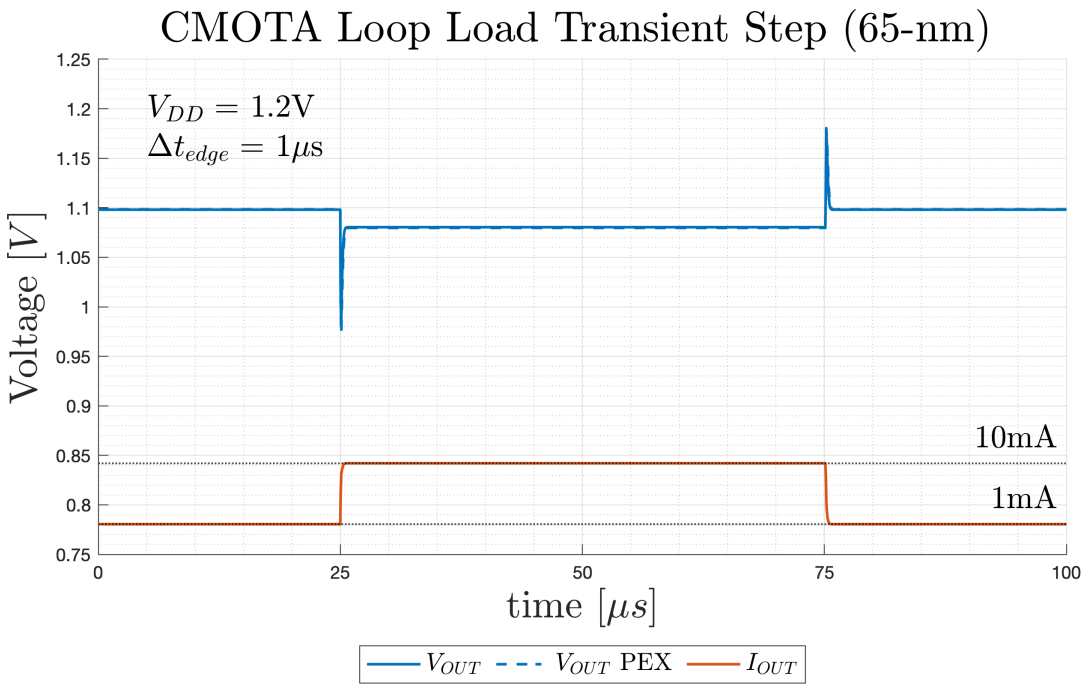


Figure E.21: Simulated CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.2$ V

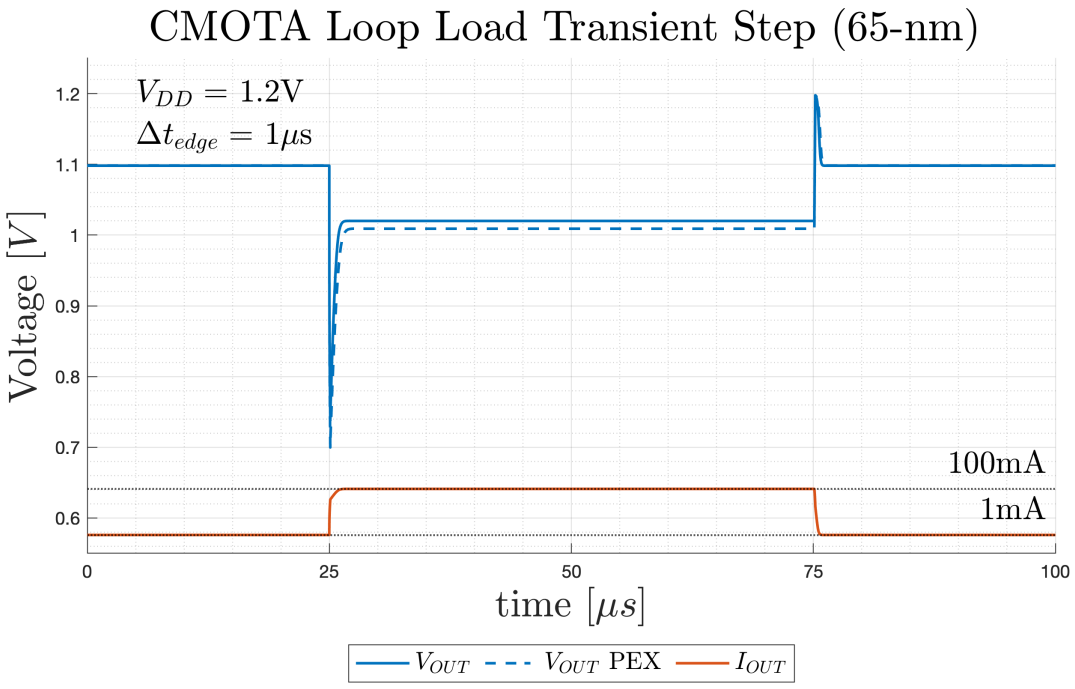


Figure E.22: Simulated CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.2$ V

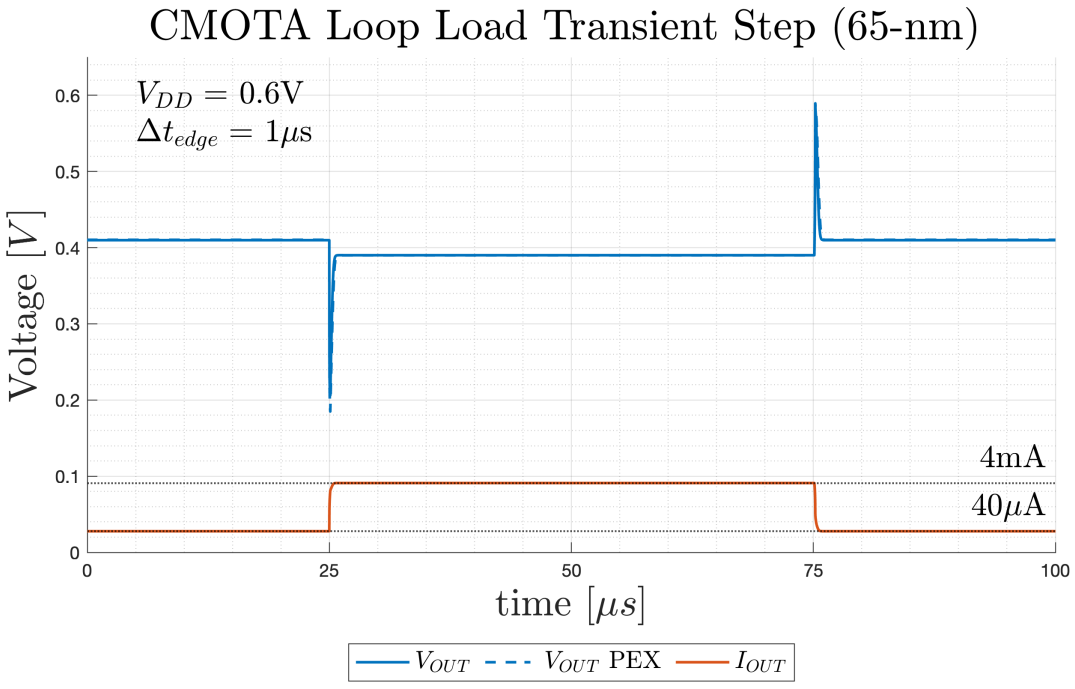


Figure E.23: Simulated CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.6$ V

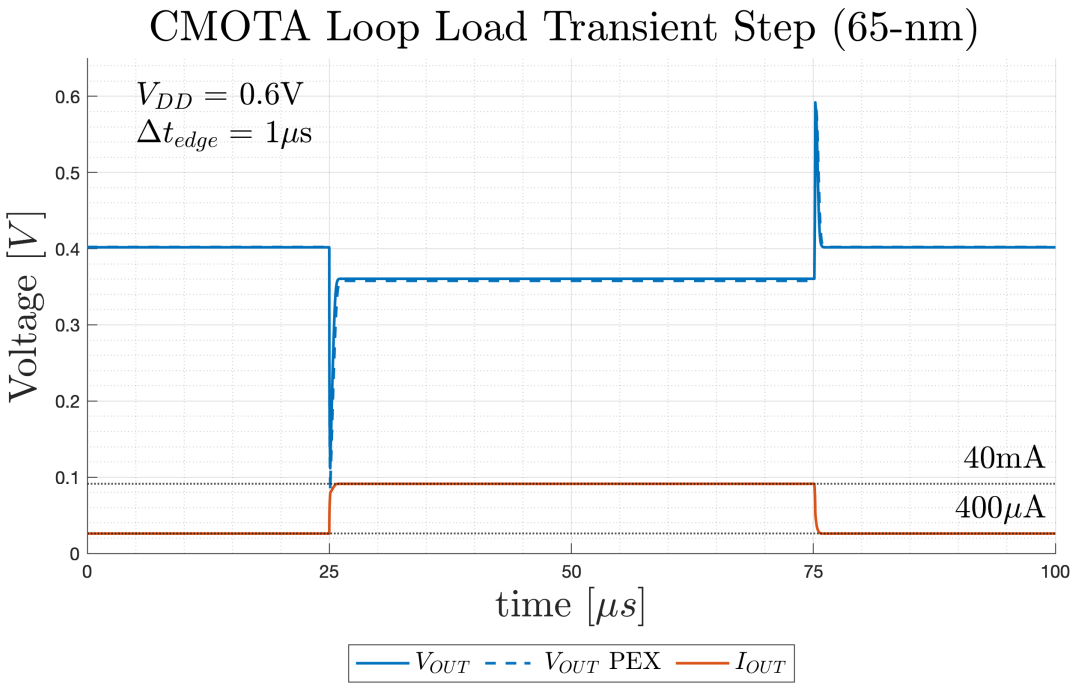


Figure E.24: Simulated CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.6$ V

F Experimental Data

F.1 Peripheral Circuit Evaluations

The experimental evaluations for the inverter and pseudo-differential switch driver (PDSD) on Teucer Chips A through E are shown in Figures F.1 to F.10 and the results are summarized within Table F.1.

- Figure F.1 Inverter transfer curve from Teucer Chip A
- Figure F.2 Inverter transfer curve from Teucer Chip B
- Figure F.3 Inverter transfer curve from Teucer Chip C
- Figure F.4 Inverter transfer curve from Teucer Chip D
- Figure F.5 Inverter transfer curve from Teucer Chip E
- Figure F.6 PDSD transition waveforms from Teucer Chip A
- Figure F.7 PDSD transition waveforms from Teucer Chip B
- Figure F.8 PDSD transition waveforms from Teucer Chip C
- Figure F.9 PDSD transition waveforms from Teucer Chip D
- Figure F.10 PDSD transition waveforms from Teucer Chip E

Table F.1: Peripheral Circuit Test Results for Individual Chips

Evaluation	**Parameters**	**Unit**	**Chip Sample**				
			A	B	C	D	E
Inverter Test Cell	V_M	mV	821	813	829	812	842
PDSD Test Cell	V_{TRANS}	mV	815	814	816	821	813

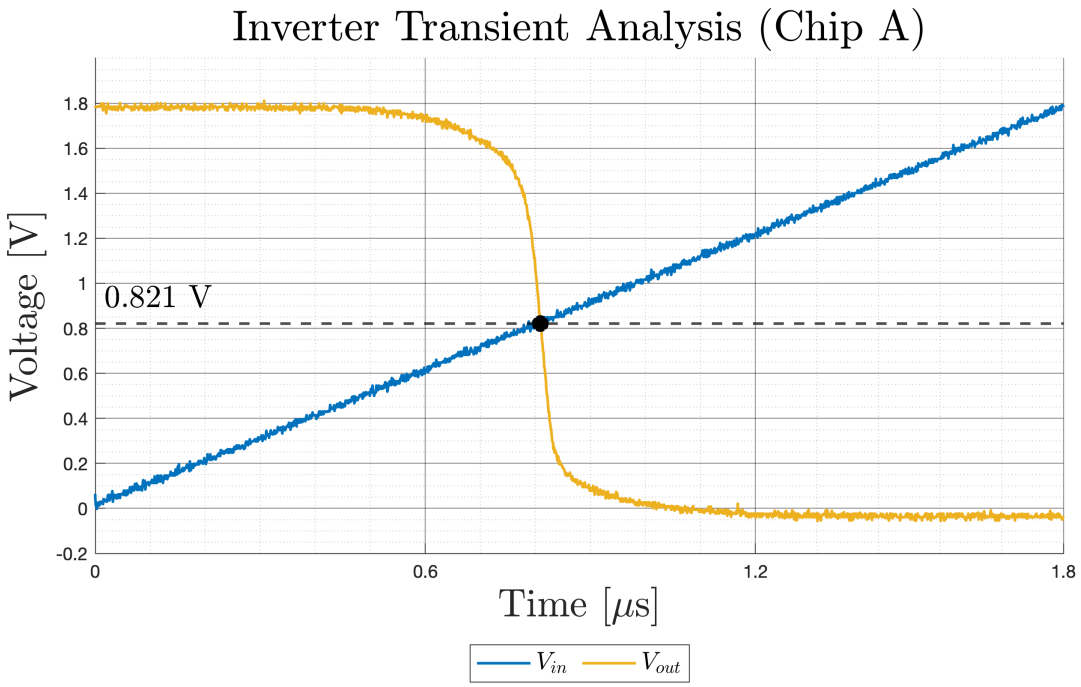


Figure F.1: Inverter test cell on Teucer Chip A

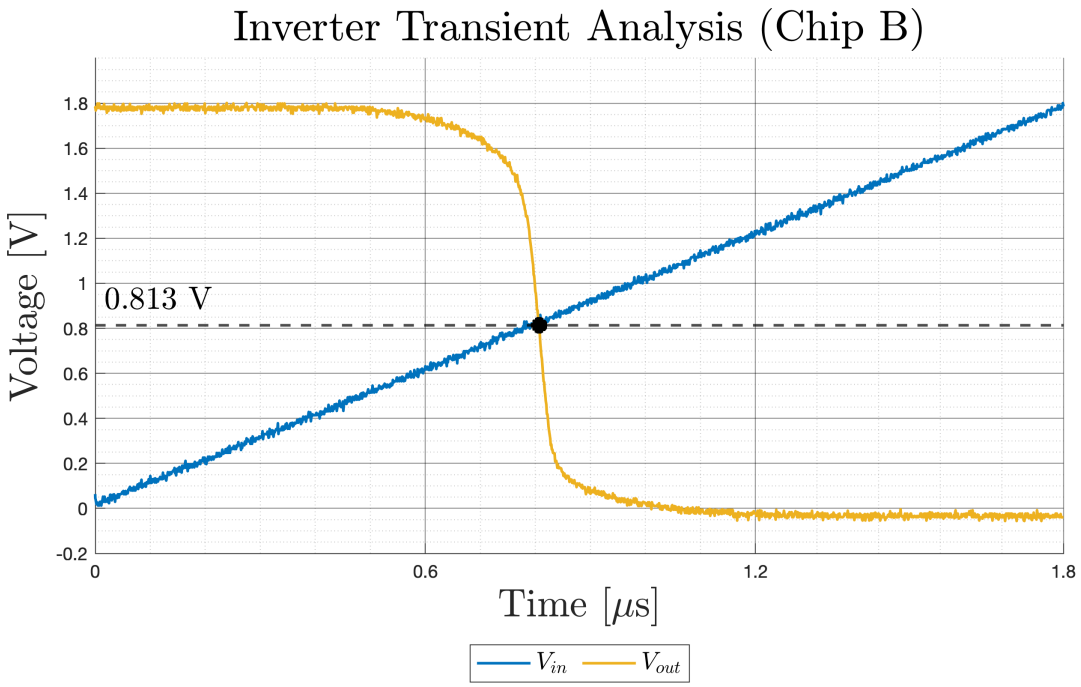


Figure F.2: Inverter test cell on Teucer Chip B

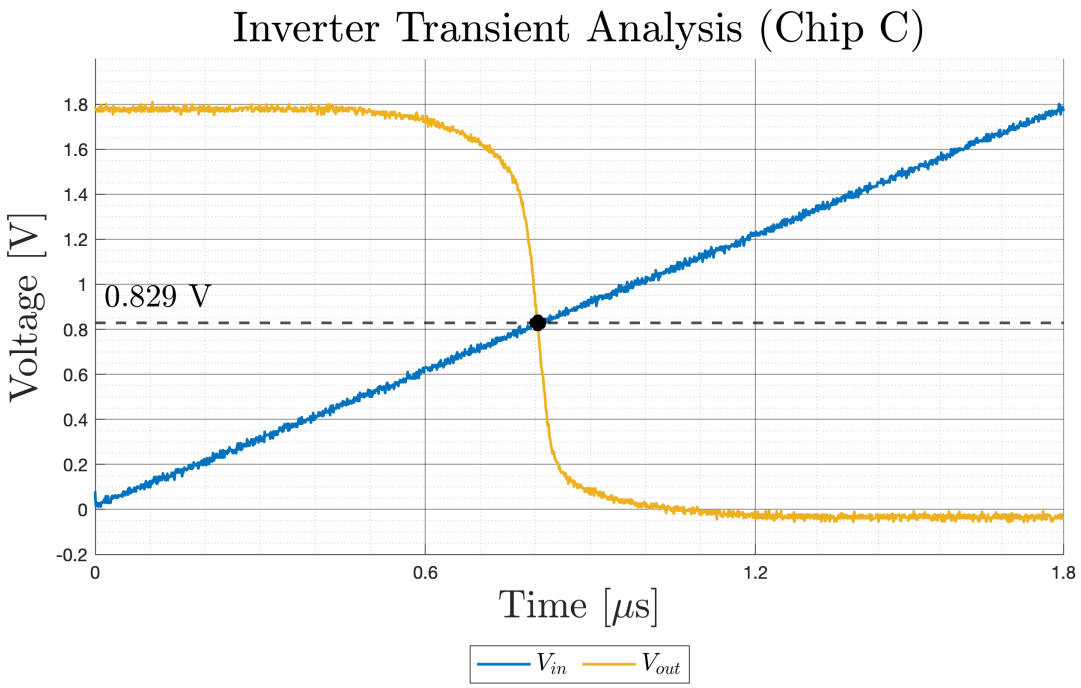


Figure F.3: Inverter test cell on Teucer Chip C

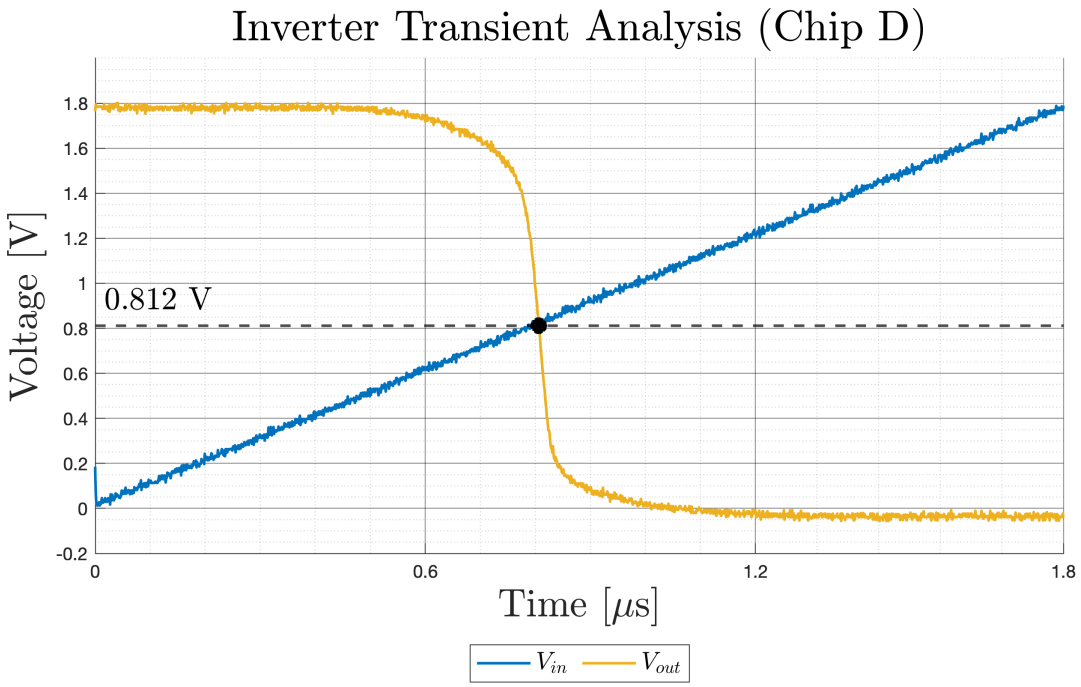


Figure F.4: Inverter test cell on Teucer Chip D

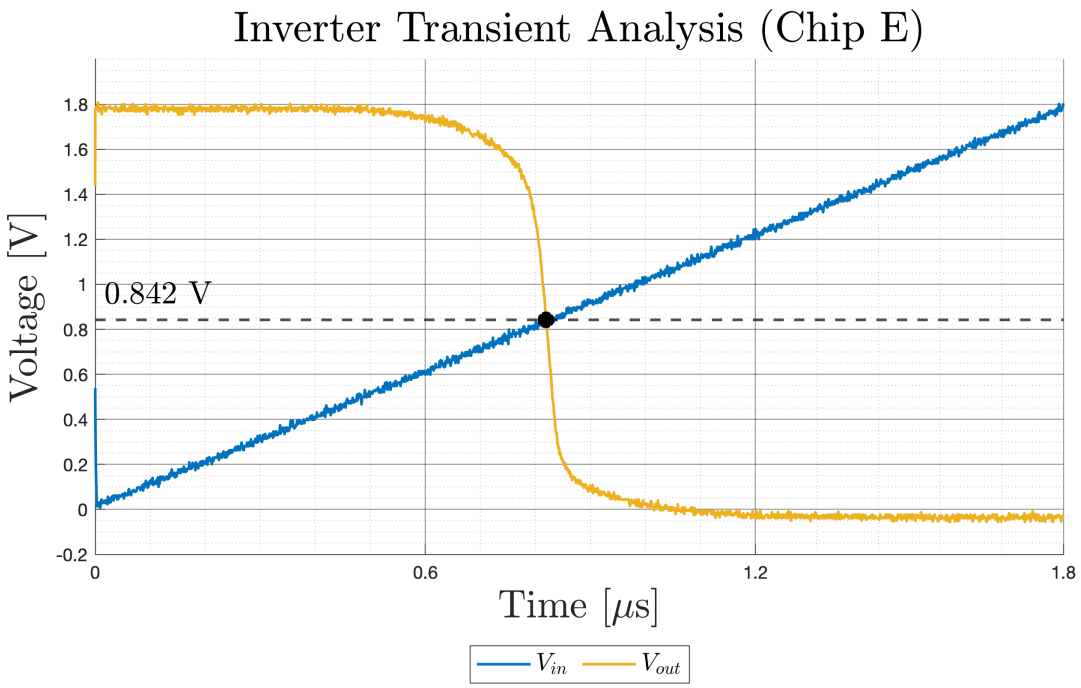


Figure F.5: Inverter test cell on Teucer Chip E

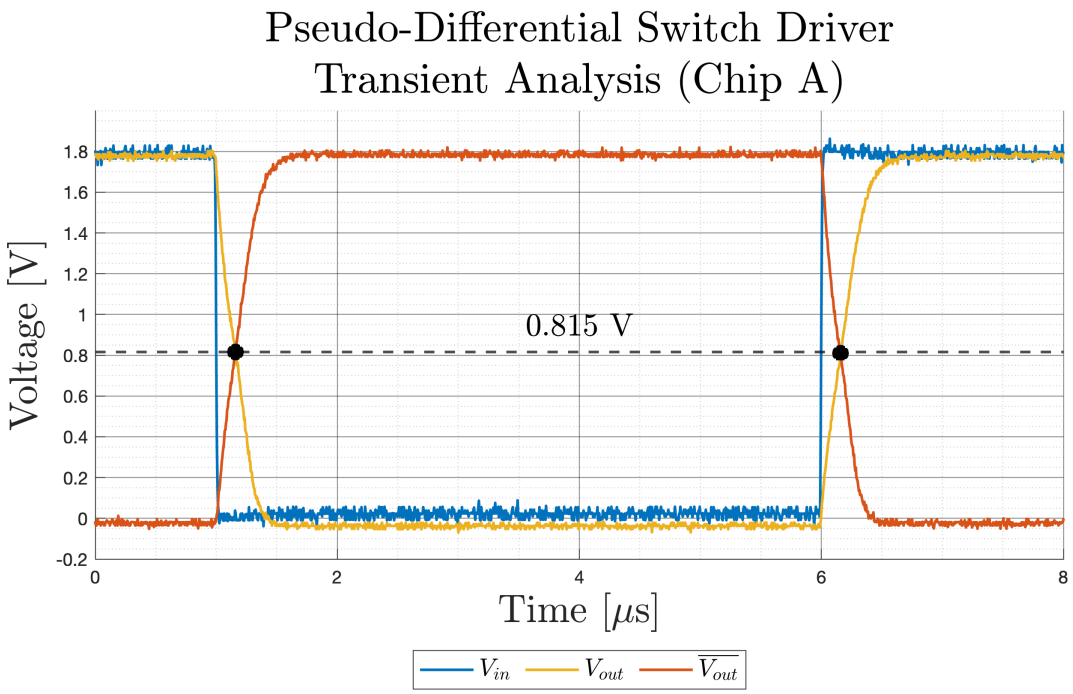


Figure F.6: PDSD test cell on Teucer Chip A

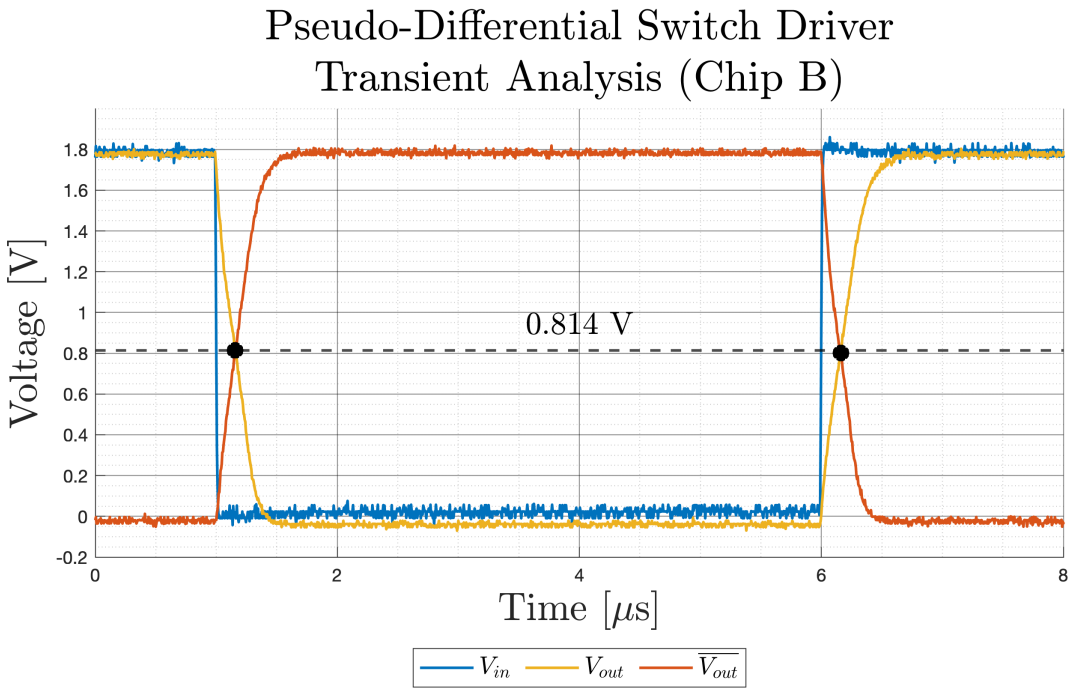


Figure F.7: PDSD test cell on Teucer Chip B

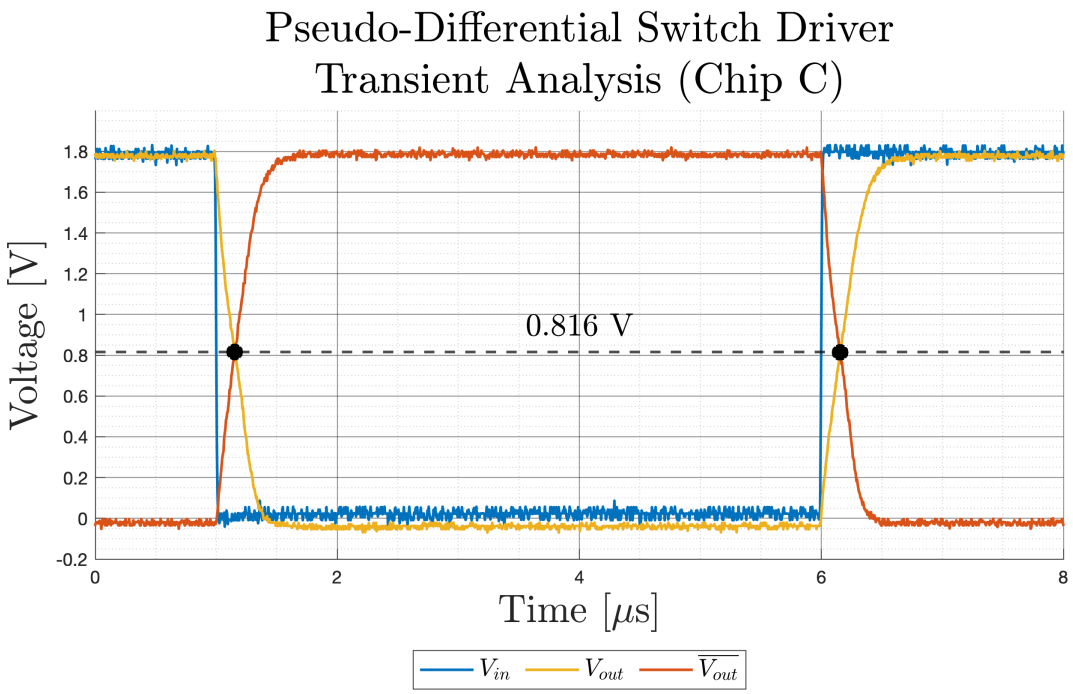


Figure F.8: PDSD test cell on Teucer Chip C

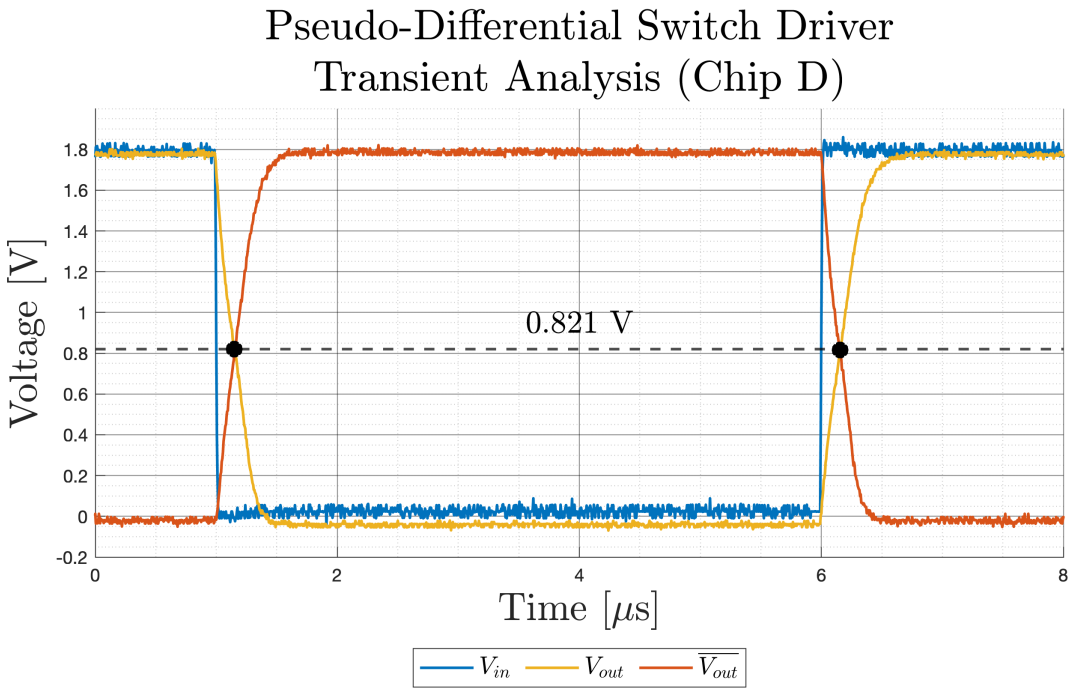


Figure F.9: PDSD test cell on Teucer Chip D

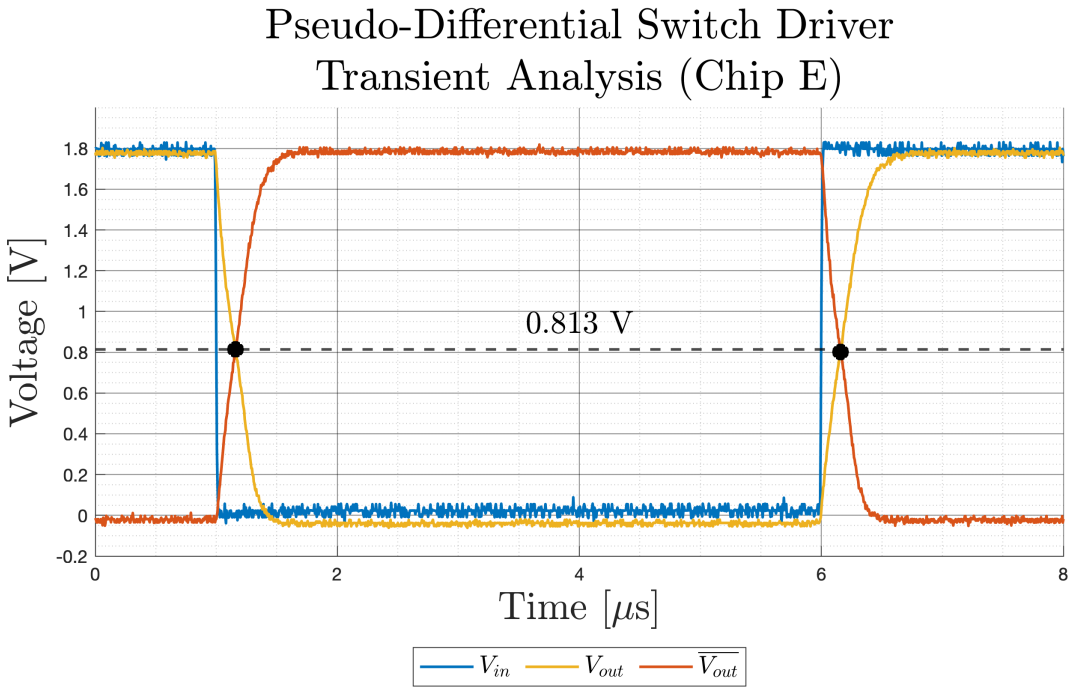


Figure F.10: PDSD test cell on Teucer Chip E

F.2 RLDOE Loop Evaluations

The experimental evaluations for the RLDOE loop on Teucer chip samples A through E are shown in Figures F.11 to F.30 and the results are summarized within Table F.2.

- Teucer Chip A
  - For $V_{DD} = 1.8\,\text{V}$
    - Figure F.11 RLDOE loop response between 1 mA to 50 mA load step
    - Figure F.12 RLDOE loop responses between 1 mA to 100 mA load step
  - For $V_{DD} = 0.9\,\text{V}$
    - Figure F.13 RLDOE loop response between 500 µA to 50 mA load step
    - Figure F.14 RLDOE loop response between 5 mA to 50 mA load step
- Teucer Chip B
  - For $V_{DD} = 1.8\,\text{V}$
    - Figure F.15 RLDOE loop response between 1 mA to 50 mA load step
    - Figure F.16 RLDOE loop responses between 1 mA to 100 mA load step
  - For $V_{DD} = 0.9\,\text{V}$
    - Figure F.17 RLDOE loop response between 500 µA to 50 mA load step
    - Figure F.18 RLDOE loop response between 5 mA to 50 mA load step
- Teucer Chip C
  - For $V_{DD} = 1.8\,\text{V}$
    - Figure F.19 RLDOE loop response between 1 mA to 50 mA load step
    - Figure F.20 RLDOE loop responses between 1 mA to 100 mA load step
  - For $V_{DD} = 0.9\,\text{V}$
    - Figure F.21 RLDOE loop response between 500 µA to 50 mA load step
    - Figure F.22 RLDOE loop response between 5 mA to 50 mA load step
- Teucer Chip D
  - For $V_{DD} = 1.8\,\text{V}$
    - Figure F.23 RLDOE loop response between 1 mA to 50 mA load step
    - Figure F.24 RLDOE loop responses between 1 mA to 100 mA load step
  - For $V_{DD} = 0.9\,\text{V}$

        * Figure F.25 RLDOE loop response between 500 µA to 50 mA load step
        * Figure F.26 RLDOE loop response between 5 mA to 50 mA load step
- Teucer Chip E
    - For $V_{DD} = 1.8\,\mathrm{V}$
        * Figure F.27 RLDOE loop response between 1 mA to 50 mA load step
        * Figure F.28 RLDOE loop responses between 1 mA to 100 mA load step
    - For $V_{DD} = 0.9\,\mathrm{V}$
        * Figure F.29 RLDOE loop response between 500 µA to 50 mA load step
        * Figure F.30 RLDOE loop response between 5 mA to 50 mA load step

Table F.2: RLDOE Loop load step Evaluation Results for Individual Chips

Evaluation	**Parameters**	**Unit**	**Chip Sample**				
			A	B	C	D	E
RLDOE Loop Set Up $V_{DD} = 1.8\,\mathrm{V}$	I_Q	[µA]	72.8	76.0	73.0	72.1	69.4
	I_{SYSTEM}	[µA]	1.5	1.5	1.5	1.5	1.5
RLDOE Loop Current Load Step 1 mA to 50 mA $V_{DD} = 1.8\,\mathrm{V}$ $V_{REF} = 1.6\,\mathrm{V}$ $t_{\Delta edge} = 15\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	200	190	200	190	190
	V_{OS}	[mV]	89	95	86	88	89
	$T_{OS,SETTLE}$	[ns]	268	252	240	183	240
	V_{US}	[mV]	117	117	108	111	112
	$T_{US,SETTLE}$	[ns]	56	54	54	58	55
RLDOE Loop Current Load Step 1 mA to 100 mA $V_{DD} = 1.8\,\mathrm{V}$ $V_{REF} = 1.6\,\mathrm{V}$ $t_{\Delta edge} = 15\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	200	200	200	190	190
	V_{OS}	[mV]	129	132	126	124	122
	$T_{OS,SETTLE}$	[ns]	328	184	145	304	426
	V_{US}	[mV]	152	139	149	147	146
	$T_{US,SETTLE}$	[ns]	60	132	52	64	51
RLDOE Loop Current Load Step 500 µA to 50 mA $V_{DD} = 0.9\,\mathrm{V}$ $V_{REF} = 0.8\,\mathrm{V}$ $t_{\Delta edge} = 15\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	102	107	98	105	107
	V_{OS}	[mV]	117	118	117	118	121
	$T_{OS,SETTLE}$	[ns]	734	810	970	656	860
	V_{US}	[mV]	178	186	174	180	187
	$T_{US,SETTLE}$	[ns]	336	260	354	281	452
RLDOE Loop Current Load Step 5 mA to 50 mA $V_{DD} = 0.9\,\mathrm{V}$ $V_{REF} = 0.8\,\mathrm{V}$ $t_{\Delta edge} = 15\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	102	108	100	106	108
	V_{OS}	[mV]	71	72	71	72	77
	$T_{OS,SETTLE}$	[ns]	254	258	374	209	330
	V_{US}	[mV]	75	76	76	79	81
	$T_{US,SETTLE}$	[ns]	164	267	292	200	330

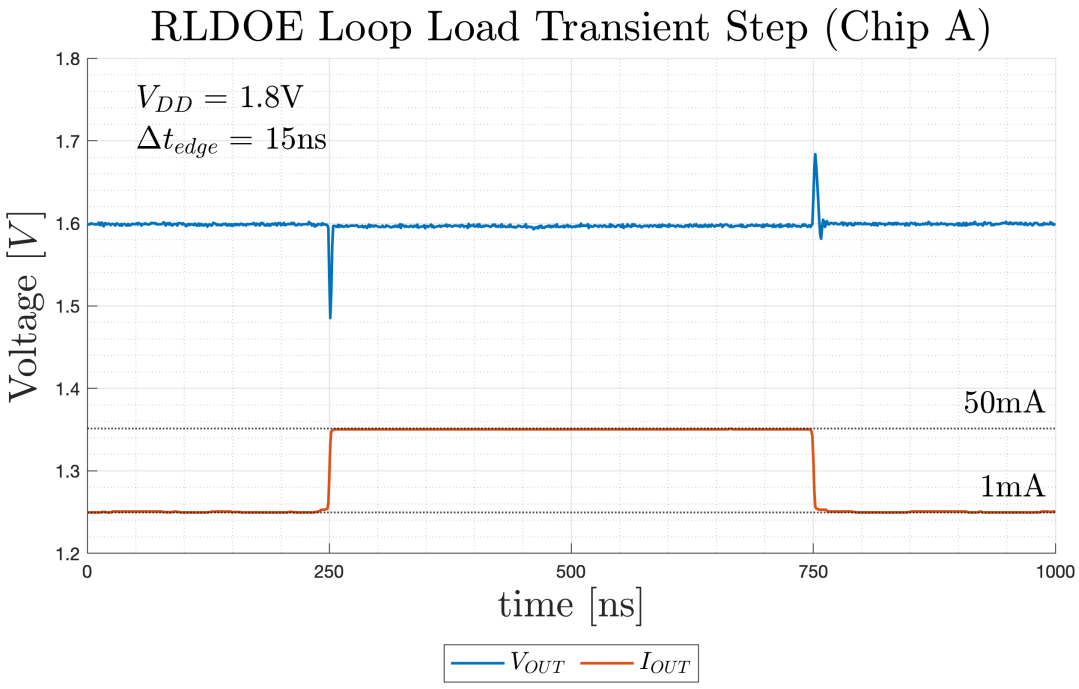


Figure F.11: RLDOE loop load step 1 mA to 50 mA with $V_{DD} = 1.8$ V on Teucer Chip A

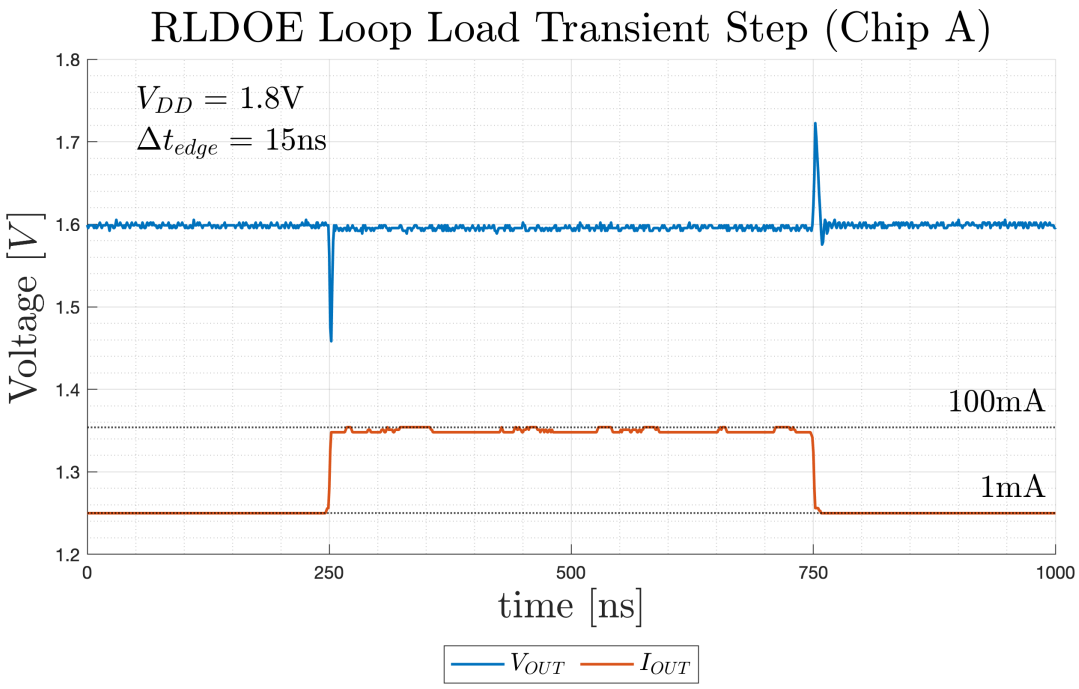


Figure F.12: RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip A

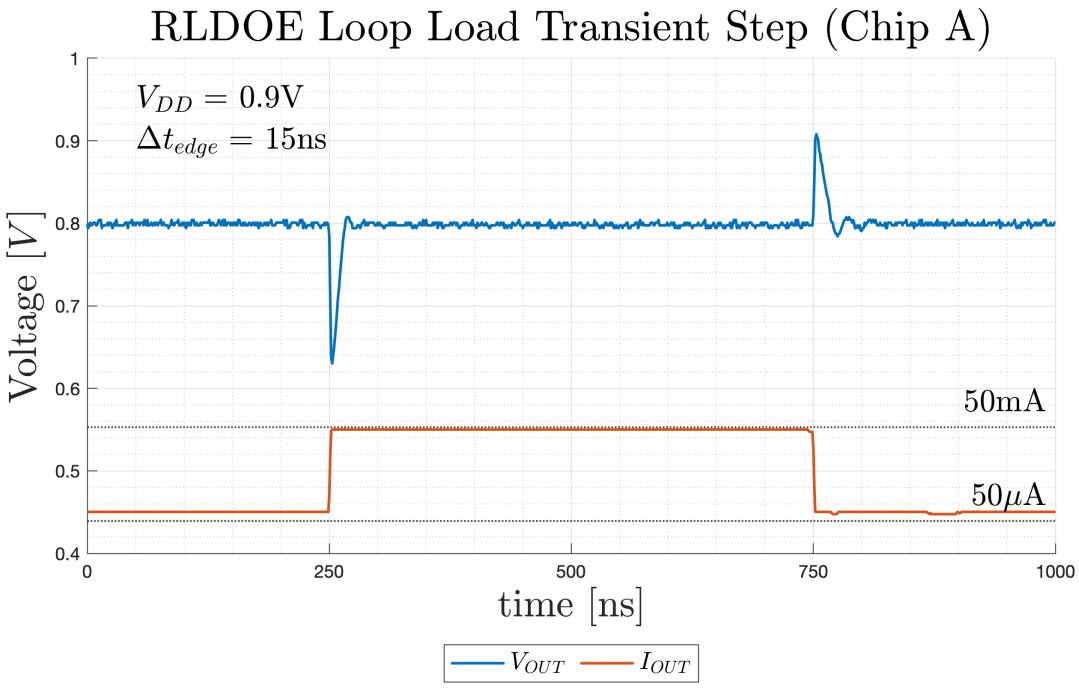


Figure F.13: RLDOE loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip A

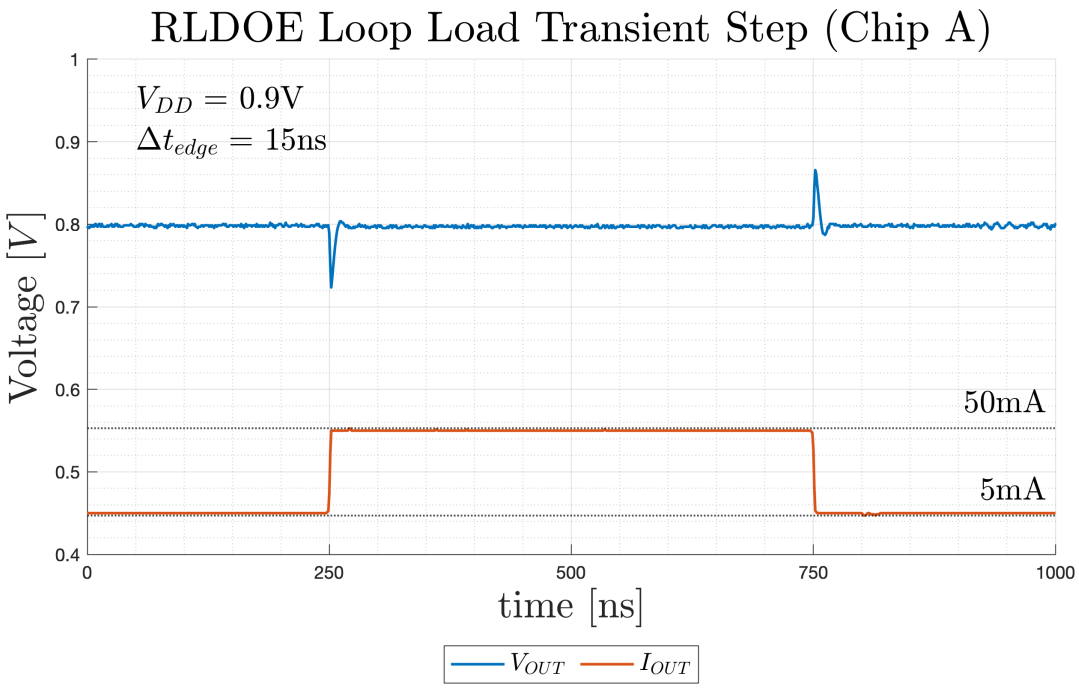


Figure F.14: RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip A

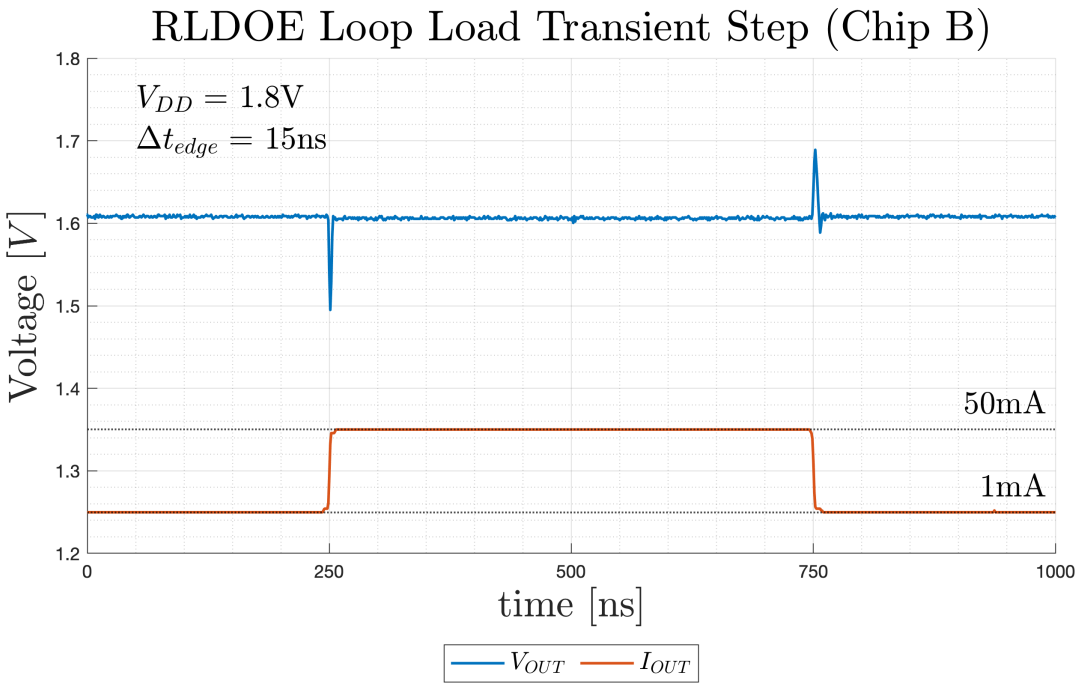


Figure F.15: RLDOE loop load step 1 mA to 50 mA with $V_{DD} = 1.8$ V on Teucer Chip B

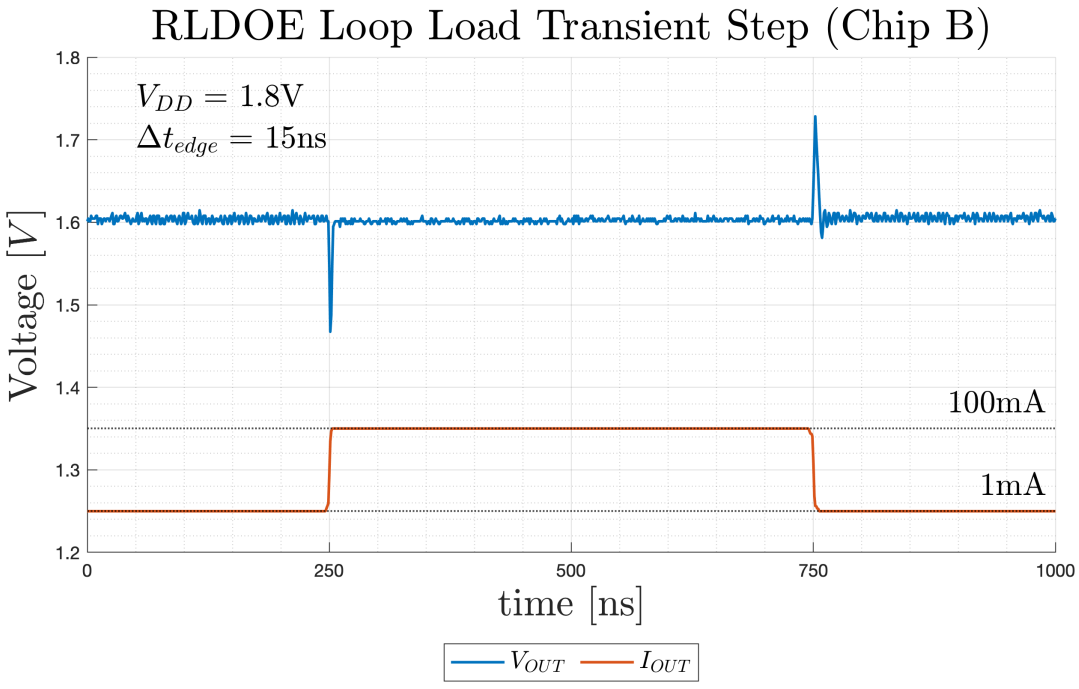


Figure F.16: RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip B

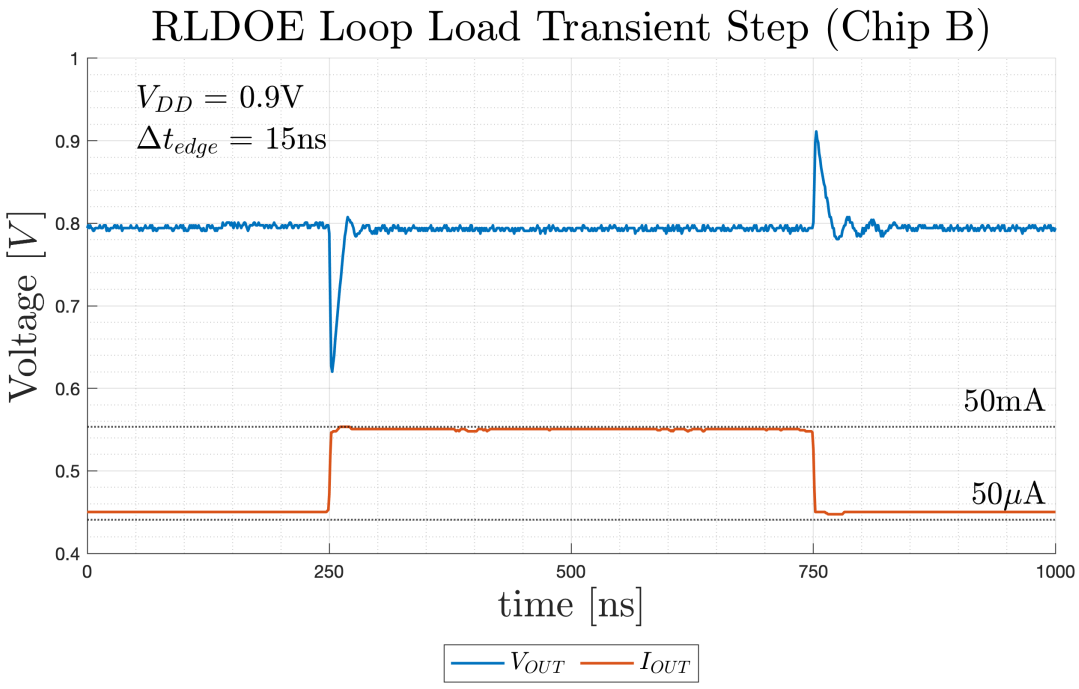


Figure F.17: RLDOE loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip B

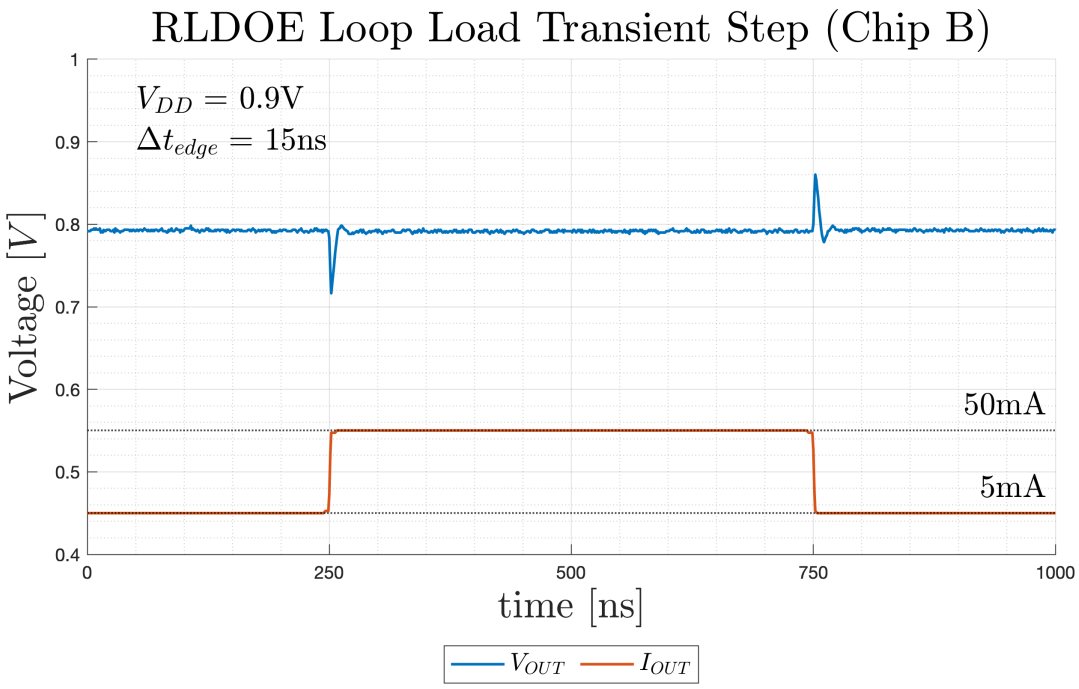


Figure F.18: RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip B

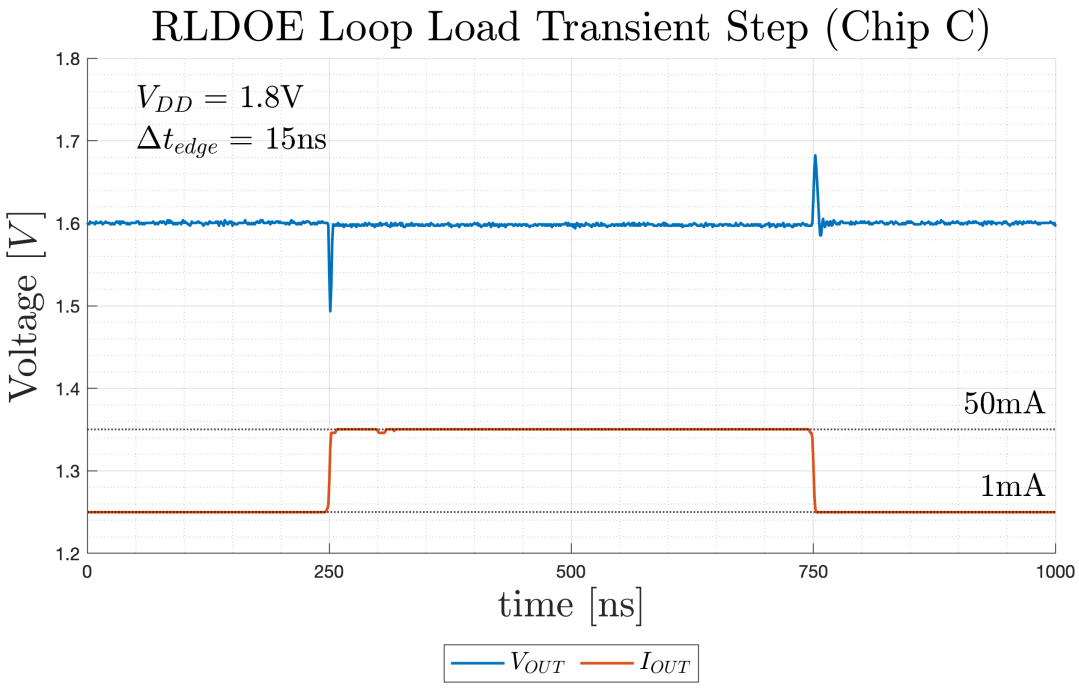


Figure F.19: RLDOE loop load step 1 mA to 50 mA with $V_{DD} = 1.8$ V on Teucer Chip C

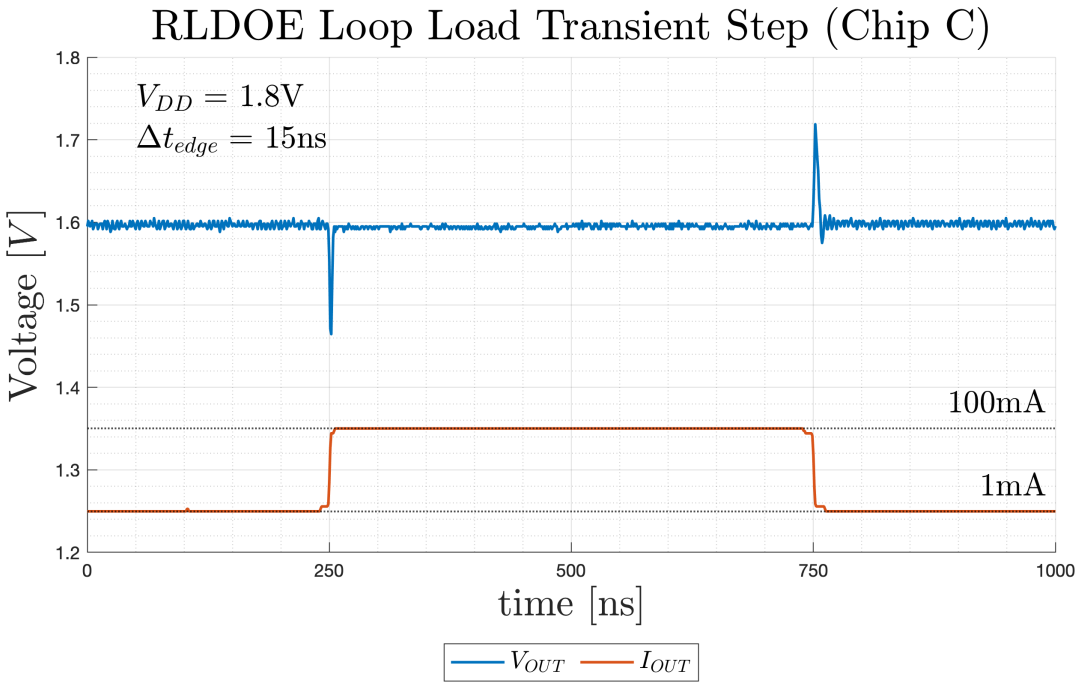


Figure F.20: RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip C

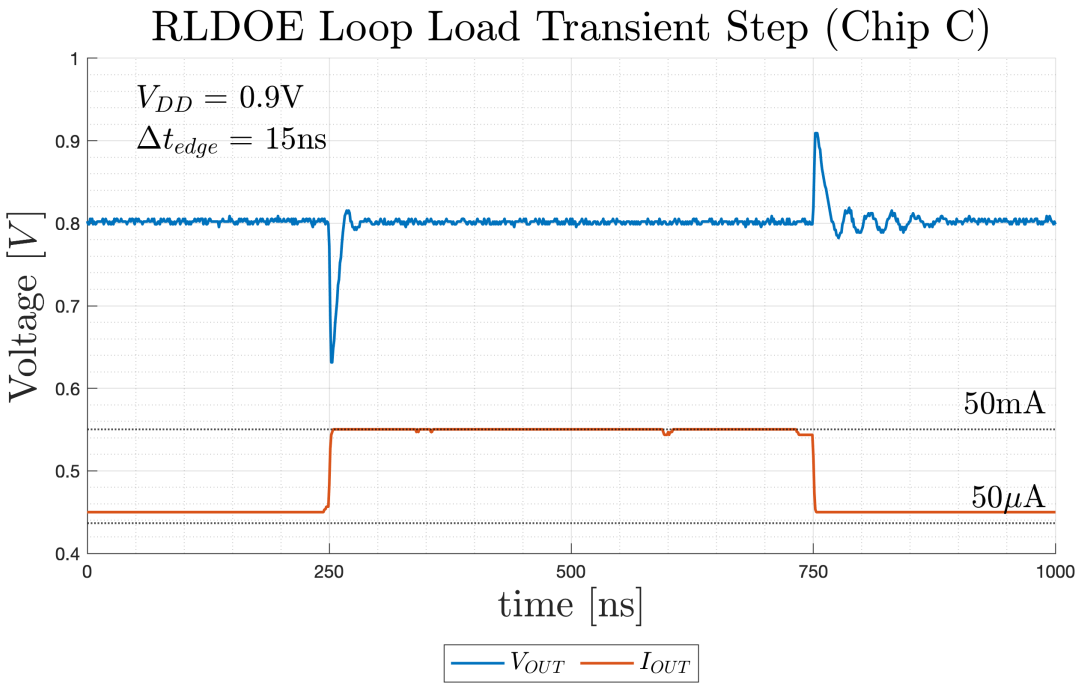


Figure F.21: RLDOE loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip C

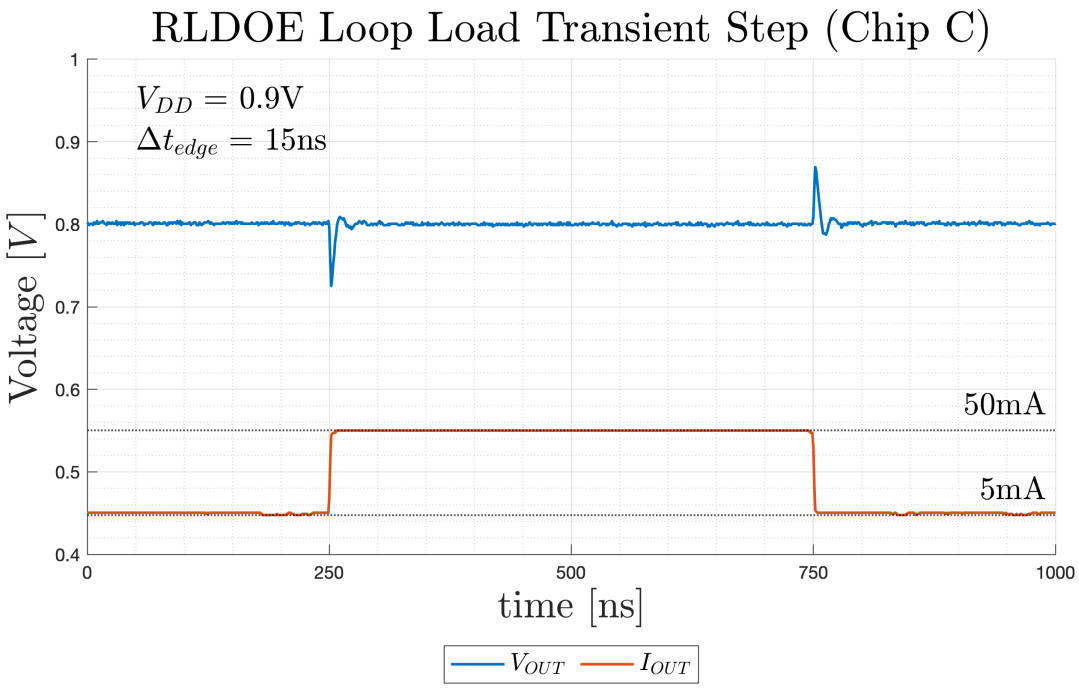


Figure F.22: RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip C

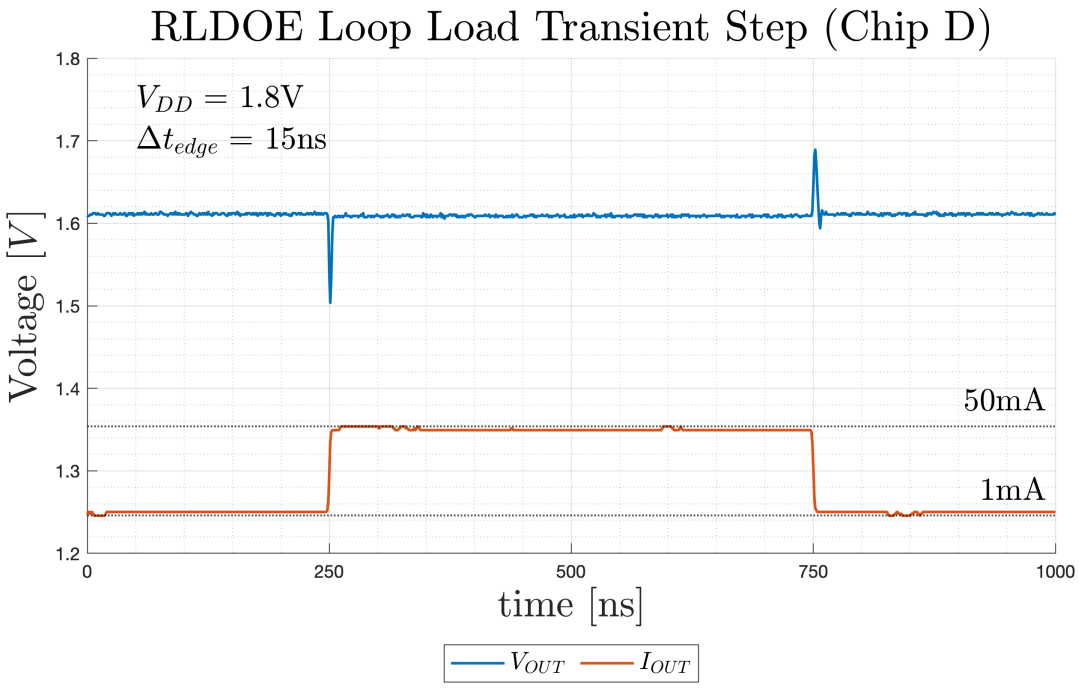


Figure F.23: RLDOE loop load step 1 mA to 50 mA with $V_{DD} = 1.8$ V on Teucer Chip D

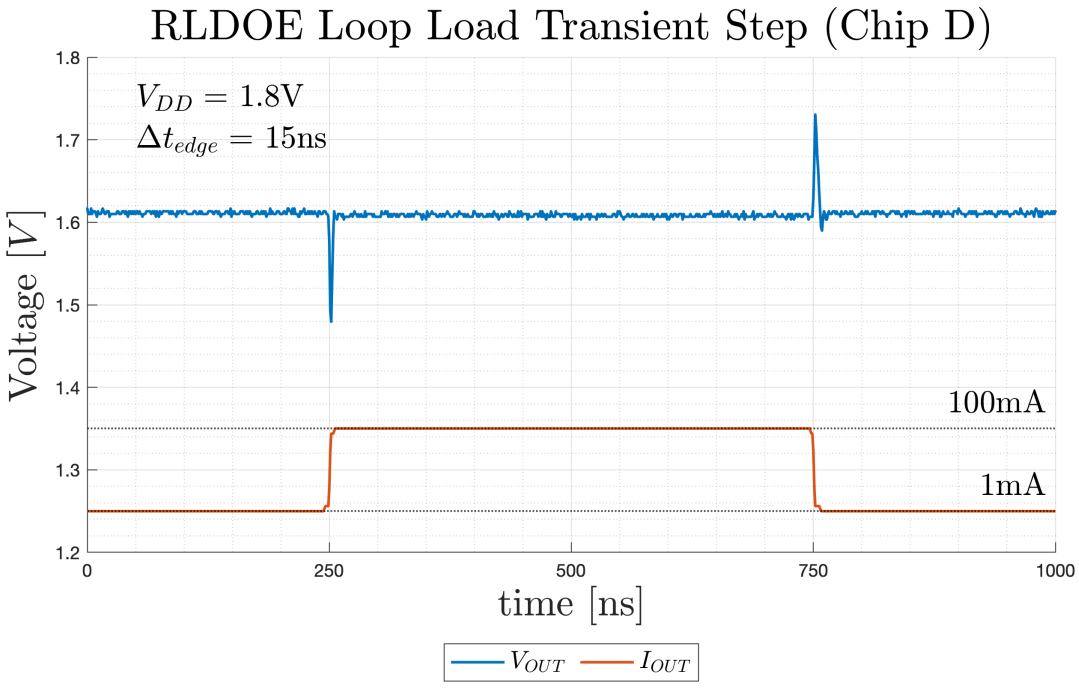


Figure F.24: RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip D

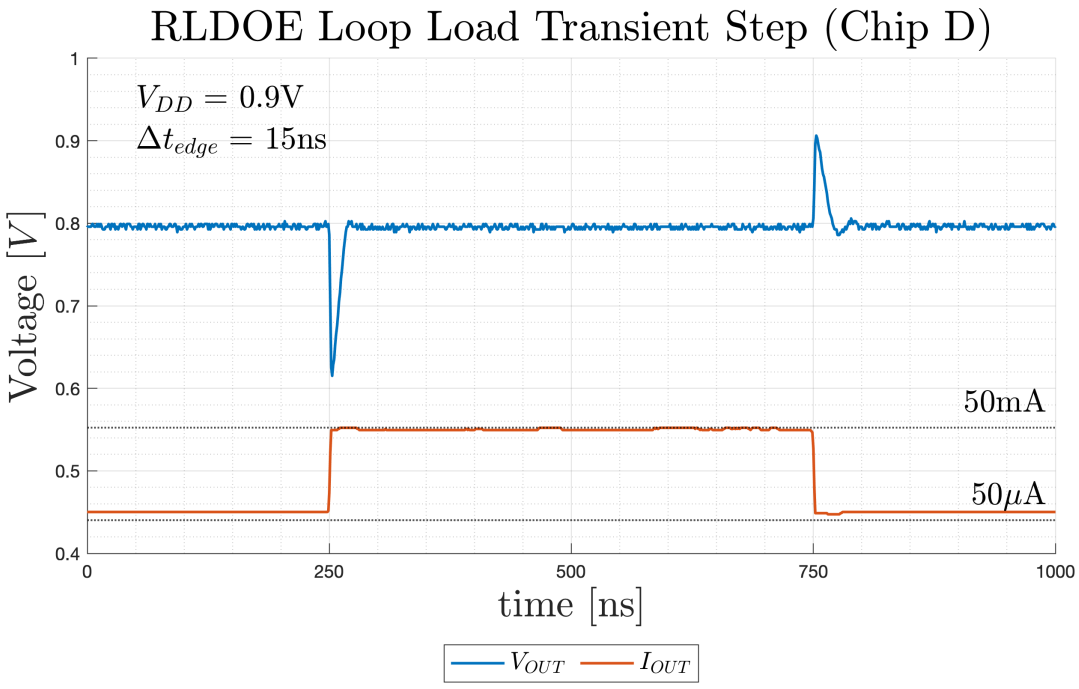


Figure F.25: RLDOE loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip D

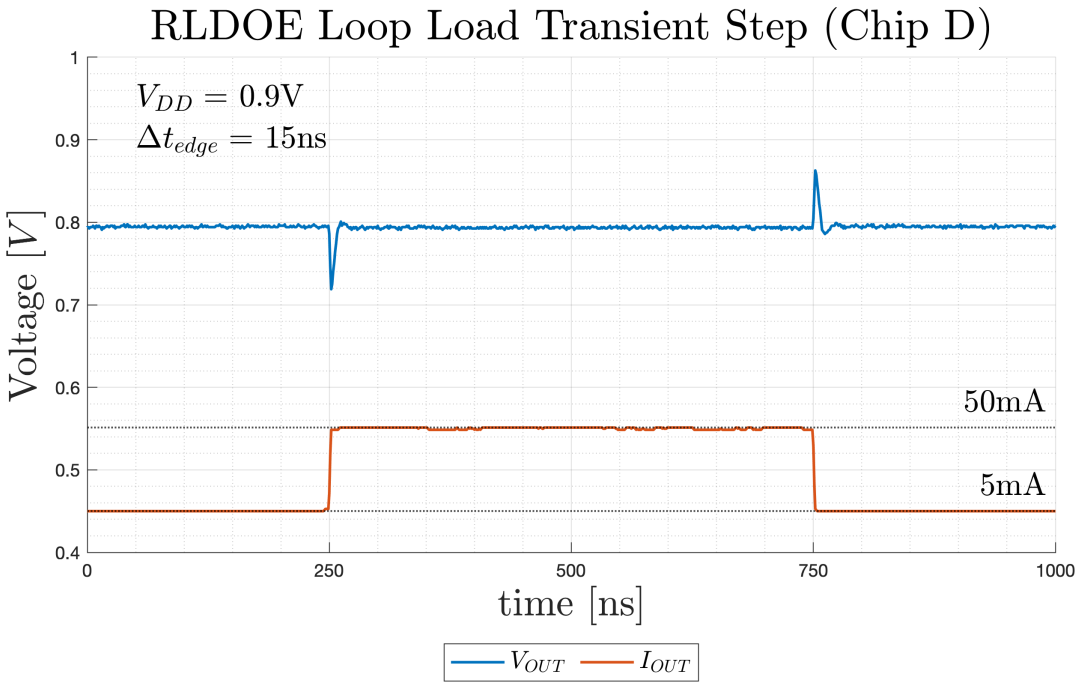


Figure F.26: RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip D

F.3 CMOTA Loop Evaluations

The experimental evaluations for the CMOTA LDO loop on Teucer Chips A through E are shown in Figures F.31 to F.55 and the results are summarized within Table F.3.

- Teucer Chip A
  - For $V_{DD} = 1.8\,\text{V}$
    - Figure F.31 CMOTA loop response between 100 µA to 1 mA load step
    - Figure F.32 CMOTA loop responses between 1 mA to 10 mA load step
    - Figure F.33 CMOTA loop responses between 1 mA to 100 mA load step
  - For $V_{DD} = 0.9\,\text{V}$
    - Figure F.34 CMOTA loop response between 40 µA to 4 mA load step
    - Figure F.35 CMOTA loop response between 400 µA to 40 mA load step
- Teucer Chip B
  - For $V_{DD} = 1.8\,\text{V}$
    - Figure F.36 CMOTA loop response between 100 µA to 1 mA load step
    - Figure F.37 CMOTA loop responses between 1 mA to 10 mA load step
    - Figure F.38 CMOTA loop responses between 1 mA to 100 mA load step
  - For $V_{DD} = 0.9\,\text{V}$
    - Figure F.39 CMOTA loop response between 40 µA to 4 mA load step
    - Figure F.40 CMOTA loop response between 400 µA to 40 mA load step
- Teucer Chip C
  - For $V_{DD} = 1.8\,\text{V}$
    - Figure F.41 CMOTA loop response between 100 µA to 1 mA load step
    - Figure F.42 CMOTA loop responses between 1 mA to 10 mA load step
    - Figure F.43 CMOTA loop responses between 1 mA to 100 mA load step
  - For $V_{DD} = 0.9\,\text{V}$
    - Figure F.44 CMOTA loop response between 40 µA to 4 mA load step
    - Figure F.45 CMOTA loop response between 400 µA to 40 mA load step
- Teucer Chip D
  - For $V_{DD} = 1.8\,\text{V}$

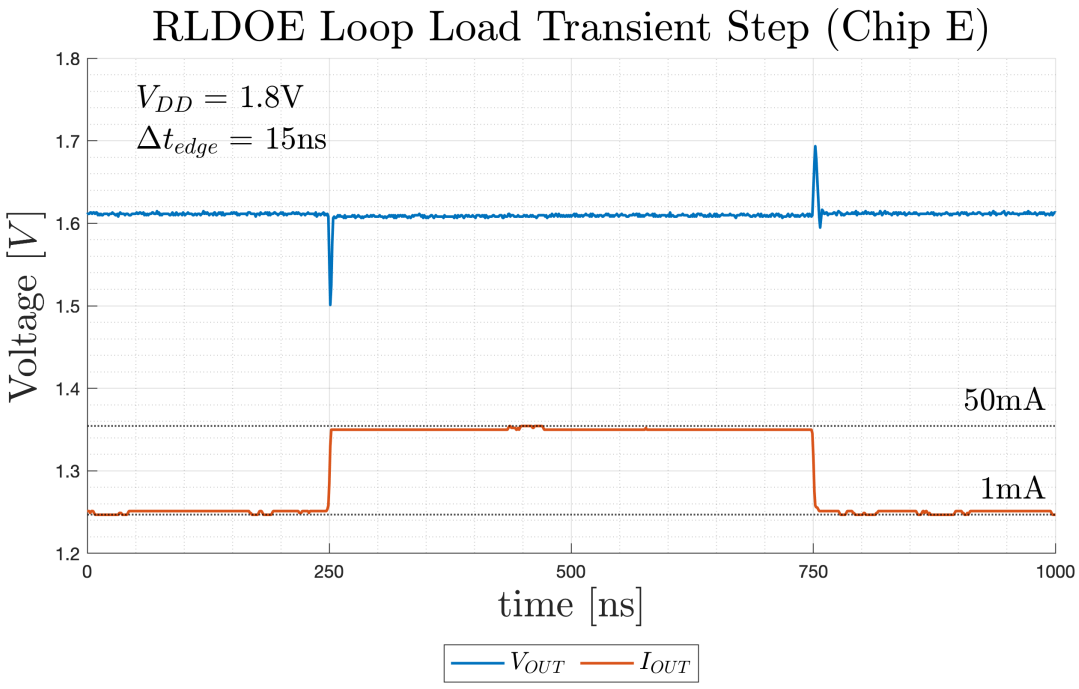


Figure F.27: RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 1.8$ V on Teucer Chip E

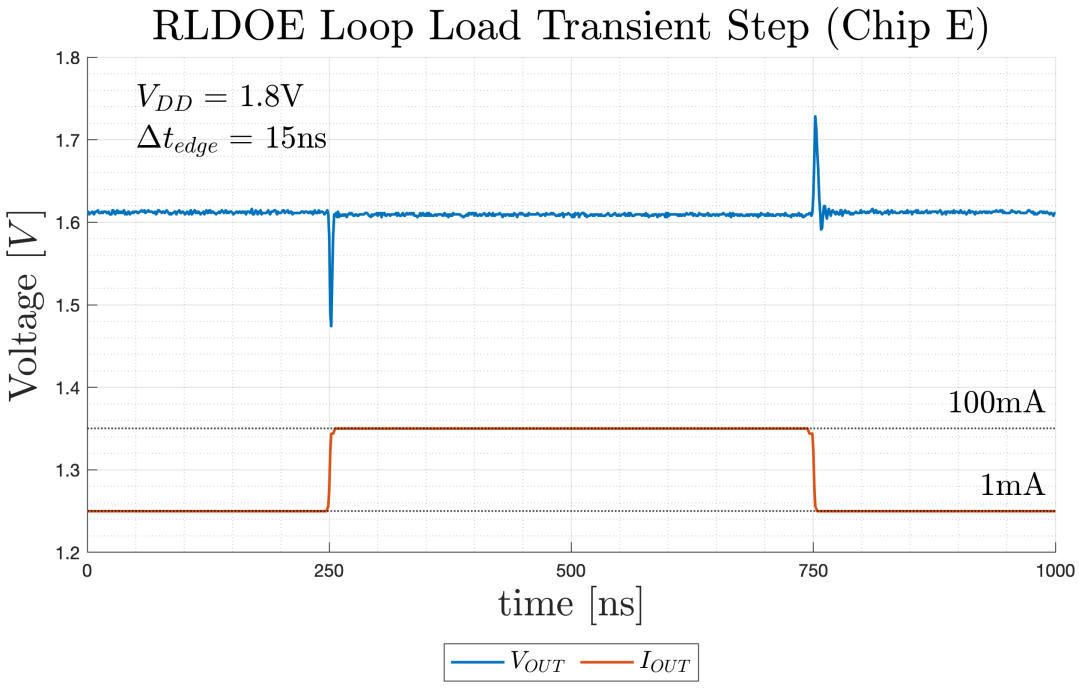


Figure F.28: RLDOE loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip E

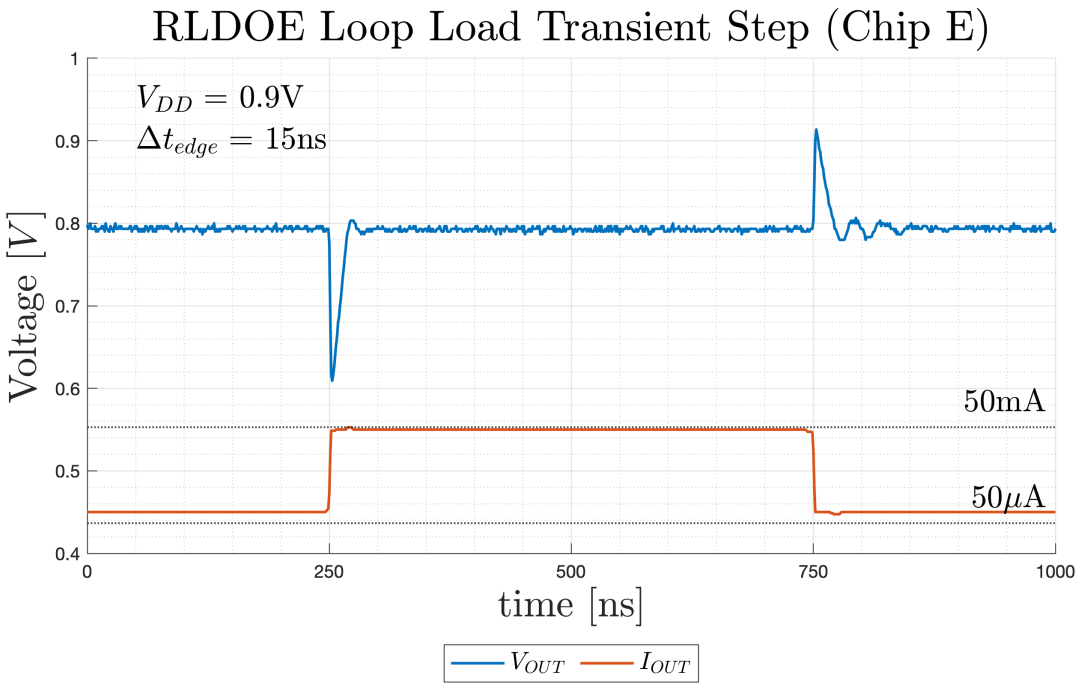


Figure F.29: RLDOE loop load step 500 µA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip E

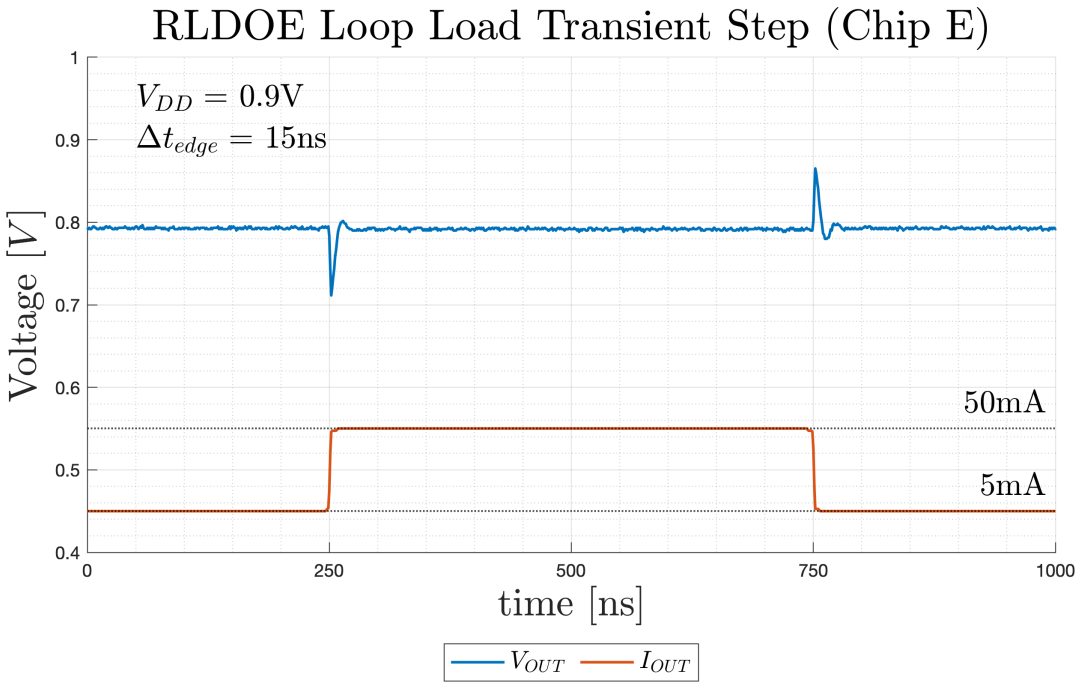


Figure F.30: RLDOE loop load step 5 mA to 50 mA with $V_{DD} = 0.9$ V on Teucer Chip E

        * Figure F.46 CMOTA loop response between 100 µA to 1 mA load step
        * Figure F.47 CMOTA loop responses between 1 mA to 10 mA load step
        * Figure F.48 CMOTA loop responses between 1 mA to 100 mA load step
    - For $V_{DD} = 0.9\,\mathrm{V}$
        * Figure F.49 CMOTA loop response between 40 µA to 4 mA load step
        * Figure F.50 CMOTA loop response between 400 µA to 40 mA load step
- Teucer Chip E
    - For $V_{DD} = 1.8\,\mathrm{V}$
        * Figure F.51 CMOTA loop response between 100 µA to 1 mA load step
        * Figure F.52 CMOTA loop responses between 1 mA to 10 mA load step
        * Figure F.53 CMOTA loop responses between 1 mA to 100 mA load step
    - For $V_{DD} = 0.9\,\mathrm{V}$
        * Figure F.54 CMOTA loop response between 40 µA to 4 mA load step
        * Figure F.55 CMOTA loop response between 400 µA to 40 mA load step

Table F.3: CMOTA Loop Current Load Step Evaluation Results for Individual Chips

Evaluation	Parameters	Unit	Chip Sample				
			A	B	C	D	E
CMOTA Loop Set Up $V_{DD} = 1.8\,\mathrm{V}$	I_Q	[µA]	0.353	0.355	0.355	0.352	0.353
	I_{SYSTEM}	[µA]	1.524	1.508	1.515	1.513	1.501
CMOTA Loop Current Load Step 100 µA to 1 mA $V_{DD} = 1.8\,\mathrm{V}$ $V_{REF} = 1.6\,\mathrm{V}$ $t_{\Delta edge} = 10\,\mu\mathrm{s}$	$V_{DO(RMS)}$	[mV]	200	200	199	199	199
	V_{OS}	[mV]	85	108	98	102	98
	$T_{OS,SETTLE}$	[µs]	42.7	48	44.6	47.2	50.4
	V_{US}	[mV]	49	58	51	55	50
	$T_{US,SETTLE}$	[µs]	21	21.8	20.6	17.8	21.8
CMOTA Loop Current Load Step 1 mA to 10 mA $V_{DD} = 1.8\,\mathrm{V}$ $V_{REF} = 1.6\,\mathrm{V}$ $t_{\Delta edge} = 10\,\mu\mathrm{s}$	$V_{DO(RMS)}$	[mV]	200	200	180	199	199
	V_{OS}	[mV]	84	115	104	115	110
	$T_{OS,SETTLE}$	[µs]	35.8	46.8	53.8	48.4	50
	V_{US}	[mV]	47	54	53	55	59
	$T_{US,SETTLE}$	[µs]	21.6	51	25.8	25.2	22.2
CMOTA Loop Current Load Step 1 mA to 100 mA $V_{DD} = 1.8\,\mathrm{V}$ $V_{REF} = 1.6\,\mathrm{V}$ $t_{\Delta edge} = 10\,\mu\mathrm{s}$	$V_{DO(RMS)}$	[mV]	200	200	199	199	199
	V_{OS}	[mV]	162	167	155	155	149
	$T_{OS,SETTLE}$	[µs]	49	60.8	60.2	64.6	65.2
	V_{US}	[mV]	99	87	72	76	92
	$T_{US,SETTLE}$	[µs]	21	22.4	21.8	25.8	23
CMOTA Loop Current Load Step 40 µA to 4 mA $V_{DD} = 0.9\,\mathrm{V}$ $V_{REF} = 0.6\,\mathrm{V}$ $t_{\Delta edge} = 10\,\mu\mathrm{s}$	$V_{DO(RMS)}$	[mV]	302	304	295	290	310
	V_{OS}	[mV]	45	44	37	37	41
	$T_{OS,SETTLE}$	[µs]	26	23.6	21.4	24.7	23.6
	V_{US}	[mV]	50	86	32	33	40
	$T_{US,SETTLE}$	[µs]	16.2	14.8	14.1	14.4	14.1
CMOTA Loop Current Load Step 400 µA to 40 mA $V_{DD} = 0.9\,\mathrm{V}$ $V_{REF} = 0.6\,\mathrm{V}$ $t_{\Delta edge} = 10\,\mu\mathrm{s}$	$V_{DO(RMS)}$	[mV]	305	306	296	310	311
	V_{OS}	[mV]	27	34	26	23	29
	$T_{OS,SETTLE}$	[µs]	19.6	18.6	17.8	19.6	20
	V_{US}	[mV]	24	27	22	19	25
	$T_{US,SETTLE}$	[µs]	14.6	14.8	14	16	14.5

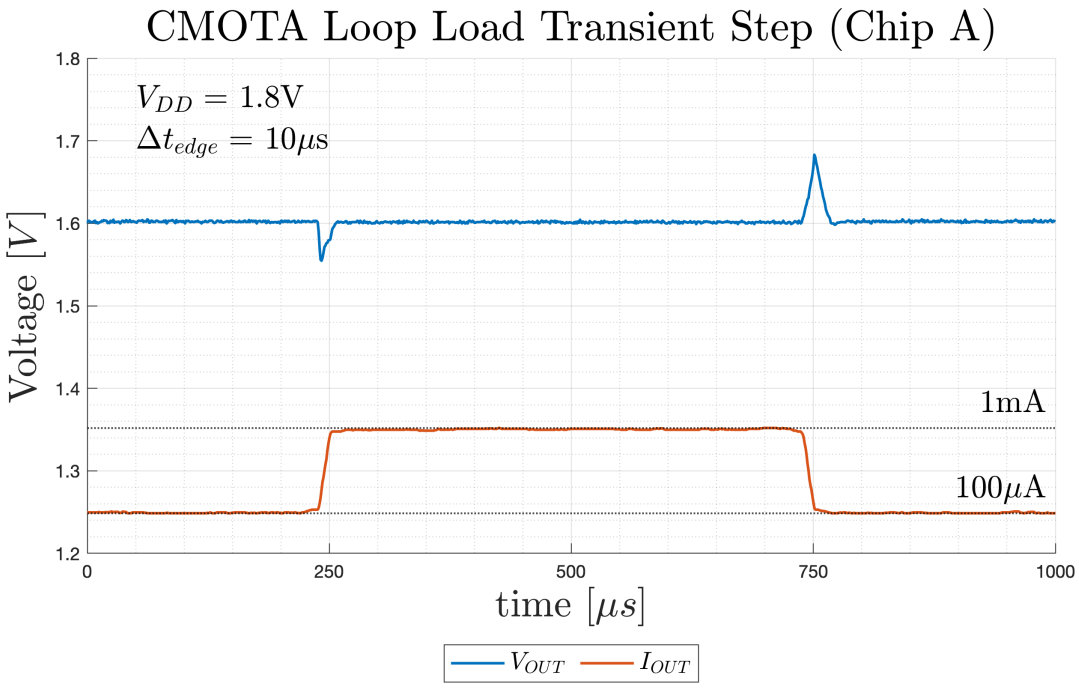


Figure F.31: CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V on Teucer Chip A

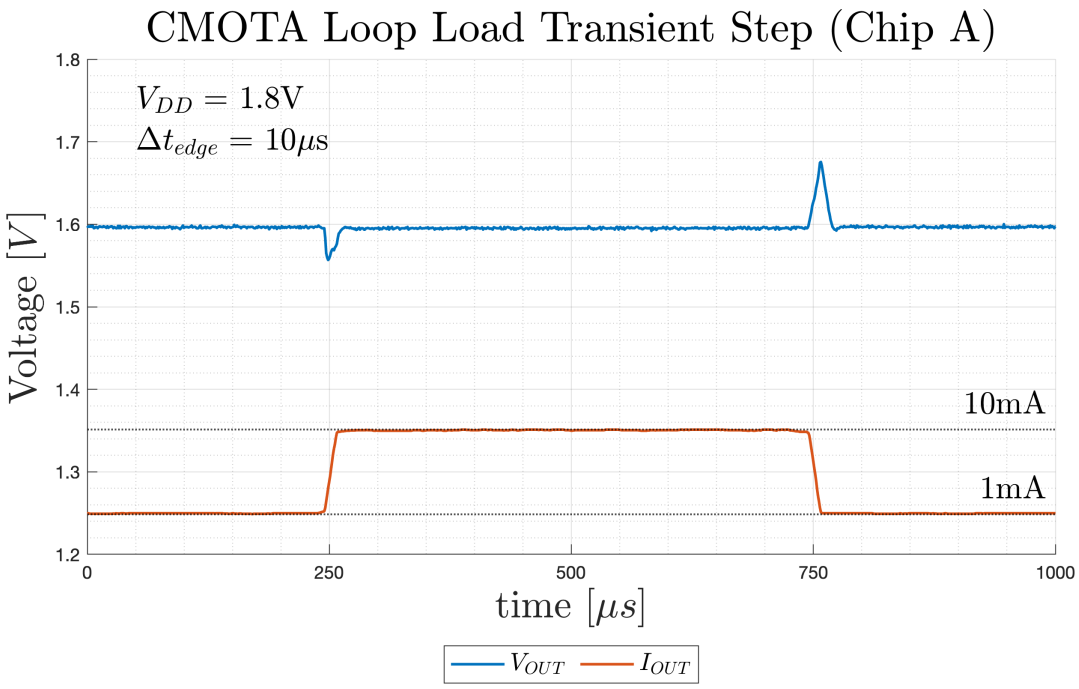


Figure F.32: CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V on Teucer Chip A

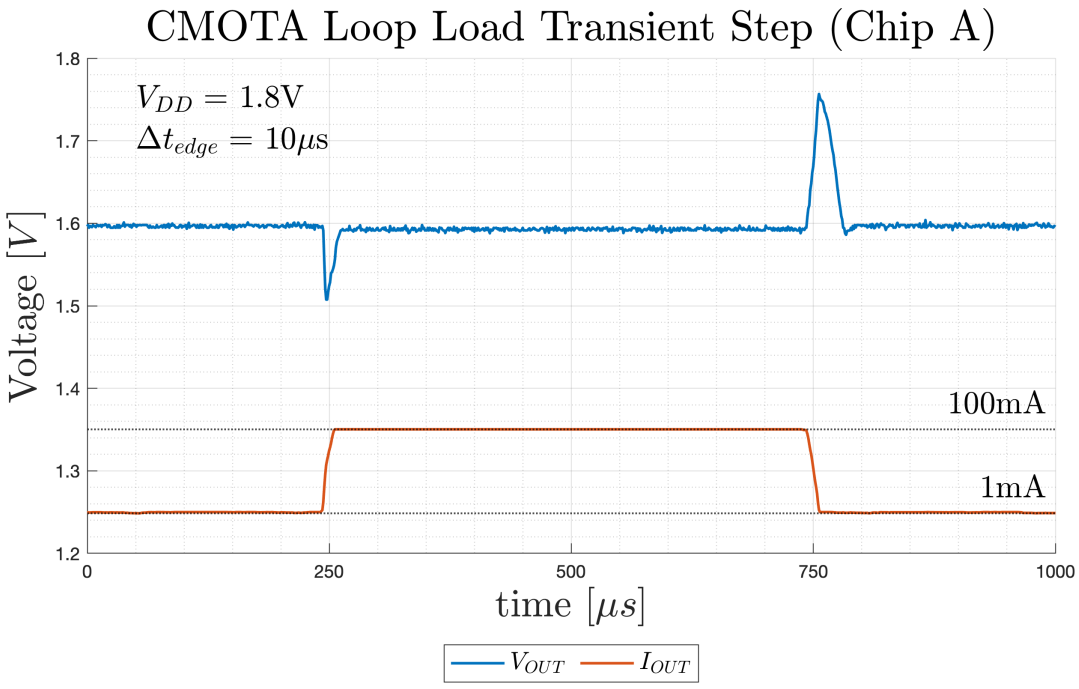


Figure F.33: CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip A

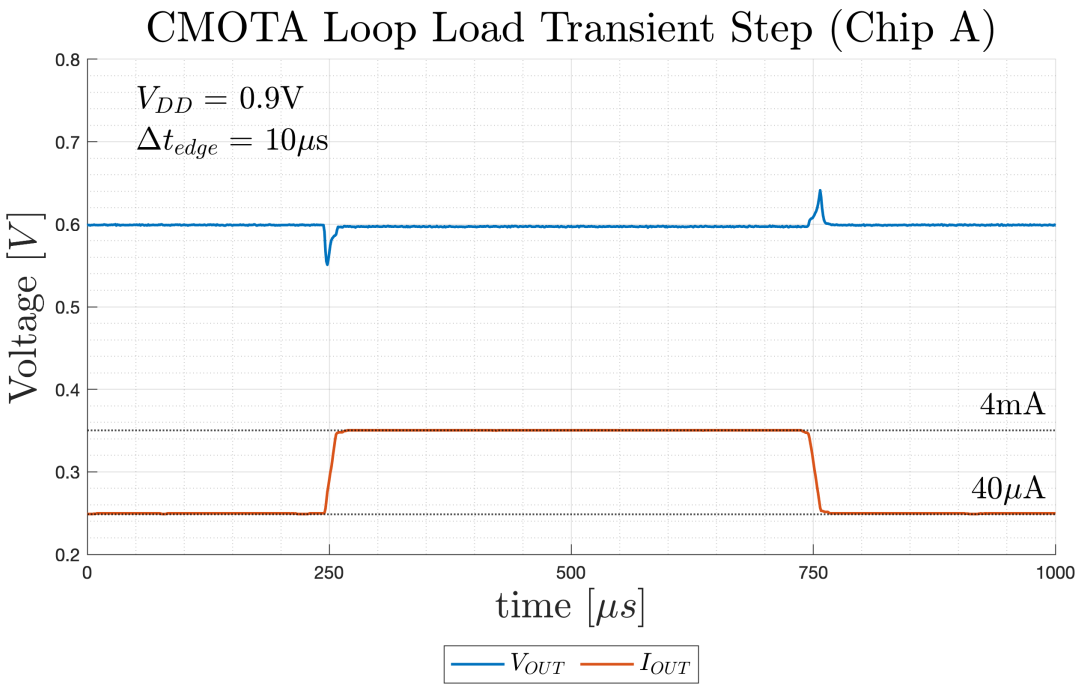


Figure F.34: CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V on Teucer Chip A

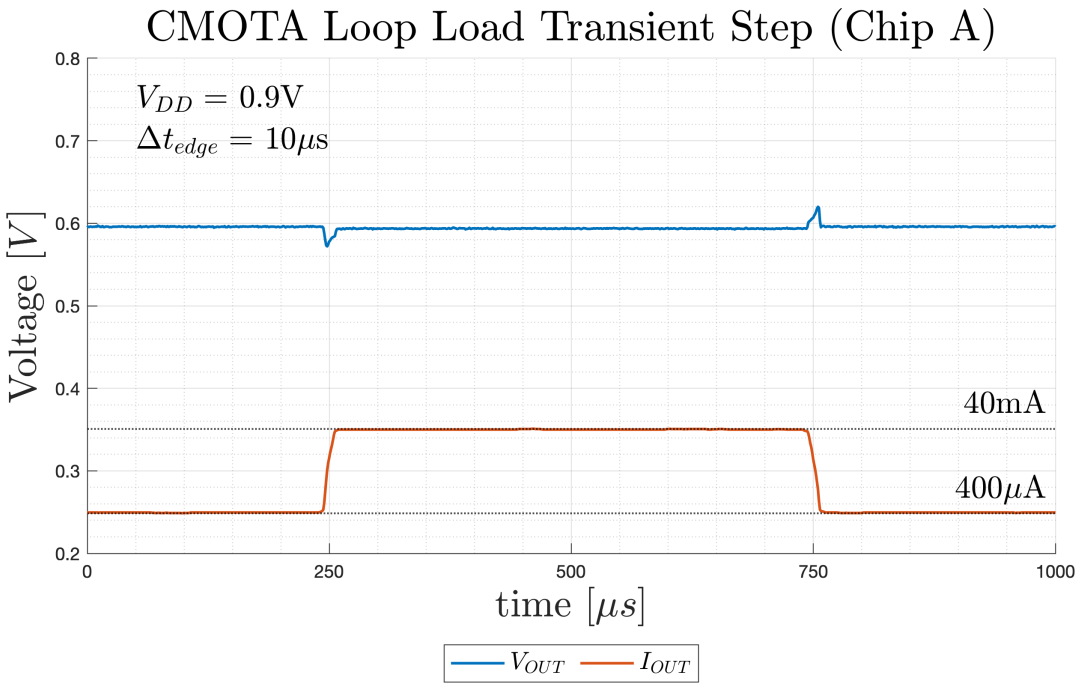


Figure F.35: CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ V on Teucer Chip A

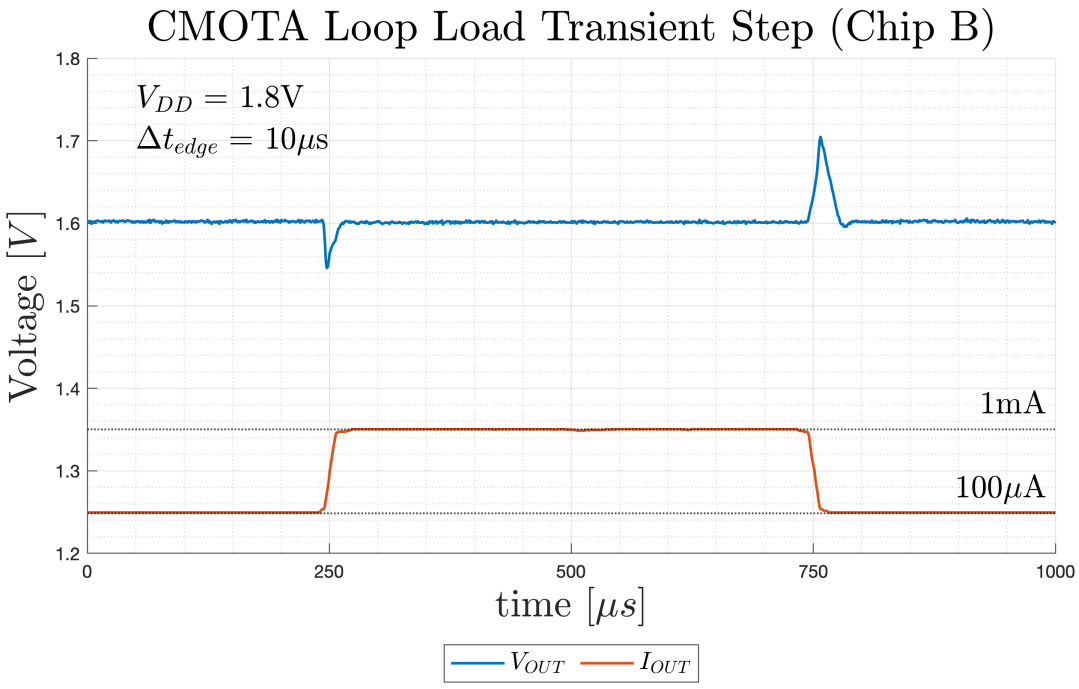


Figure F.36: CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V on Teucer Chip B

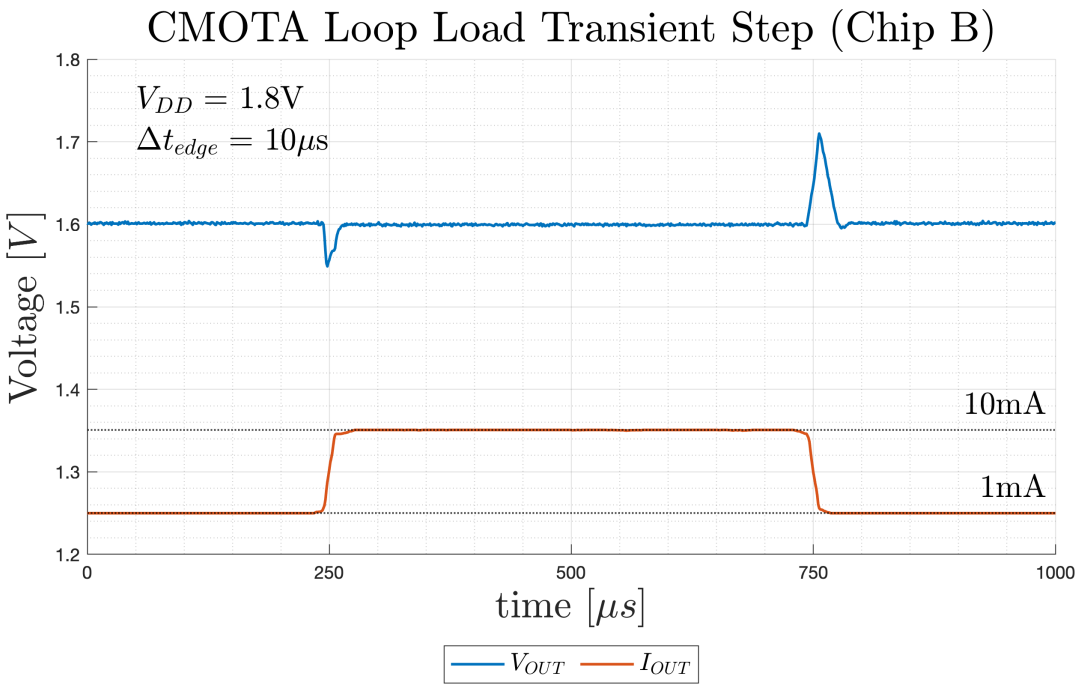


Figure F.37: CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V on Teucer Chip B

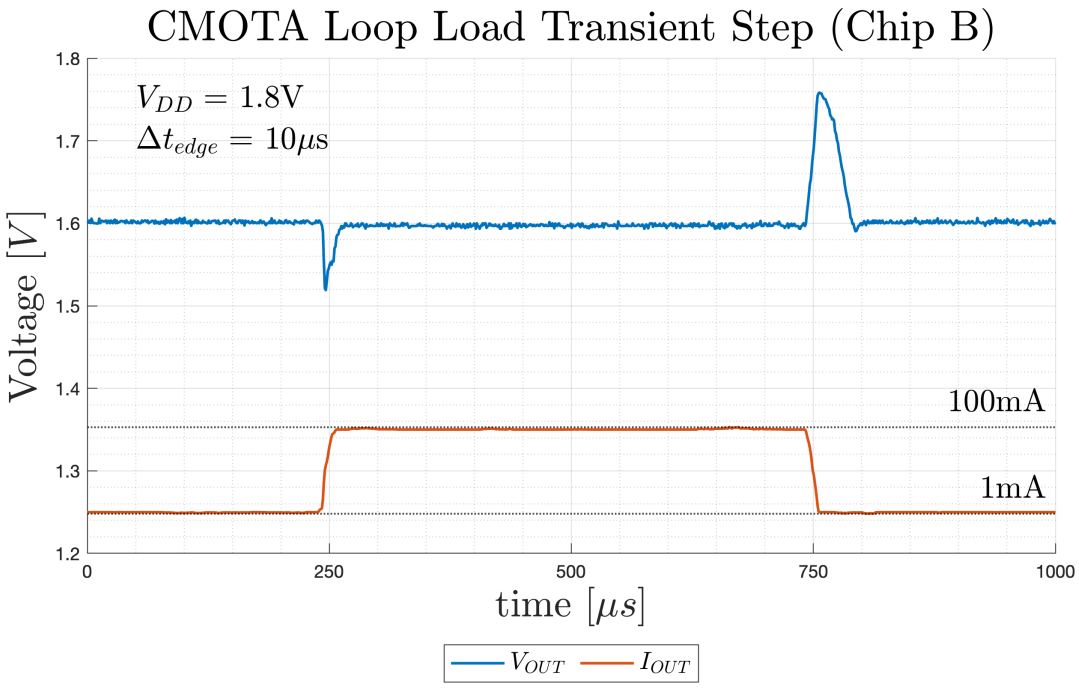


Figure F.38: CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip B

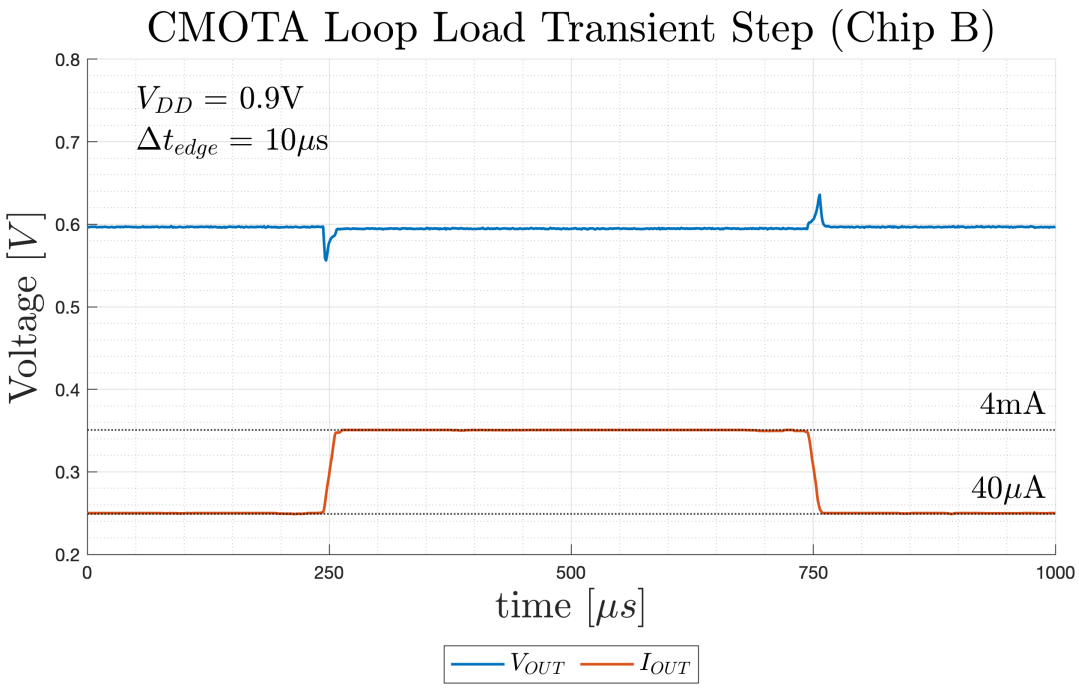


Figure F.39: CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V on Teucer Chip B

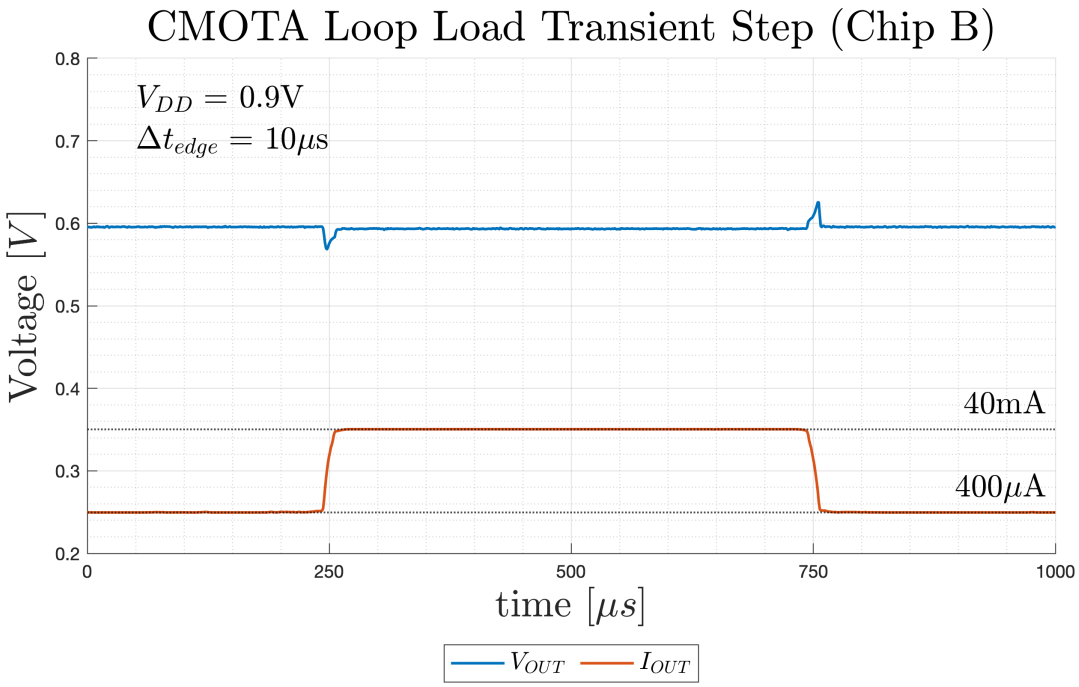


Figure F.40: CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ V on Teucer Chip B

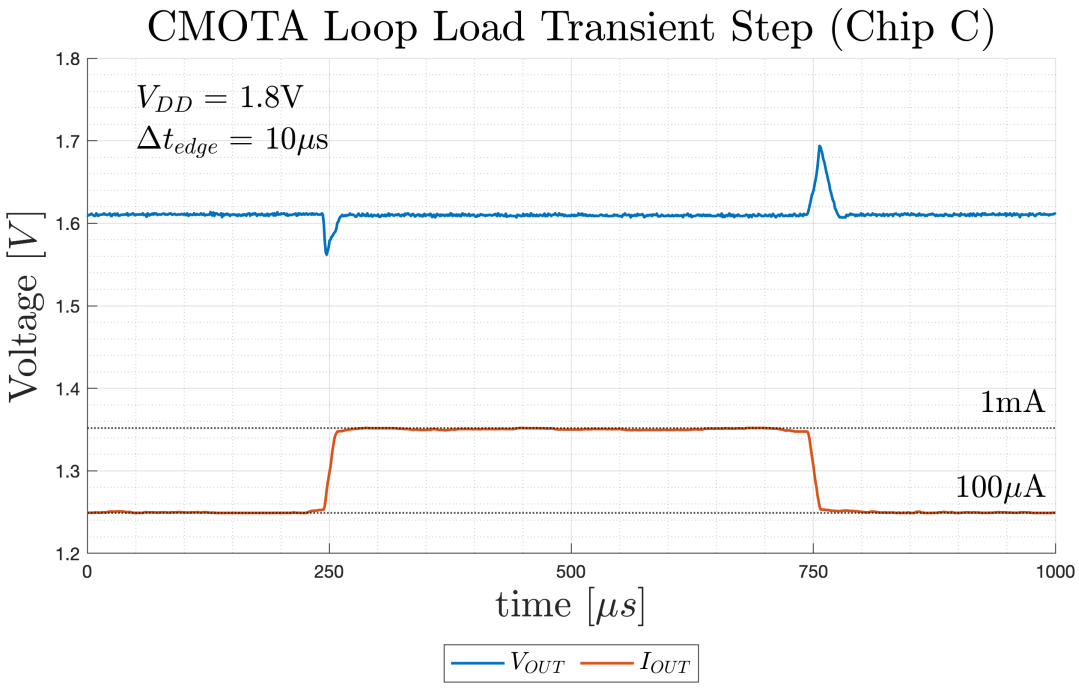


Figure F.41: CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V on Teucer Chip C

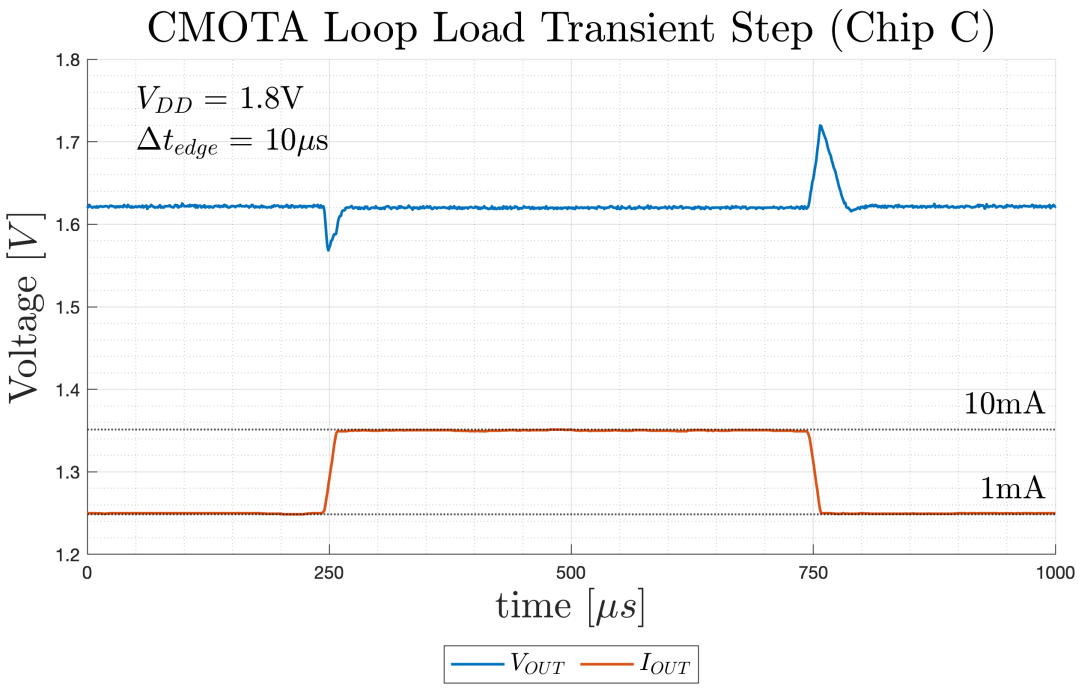


Figure F.42: CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V on Teucer Chip C

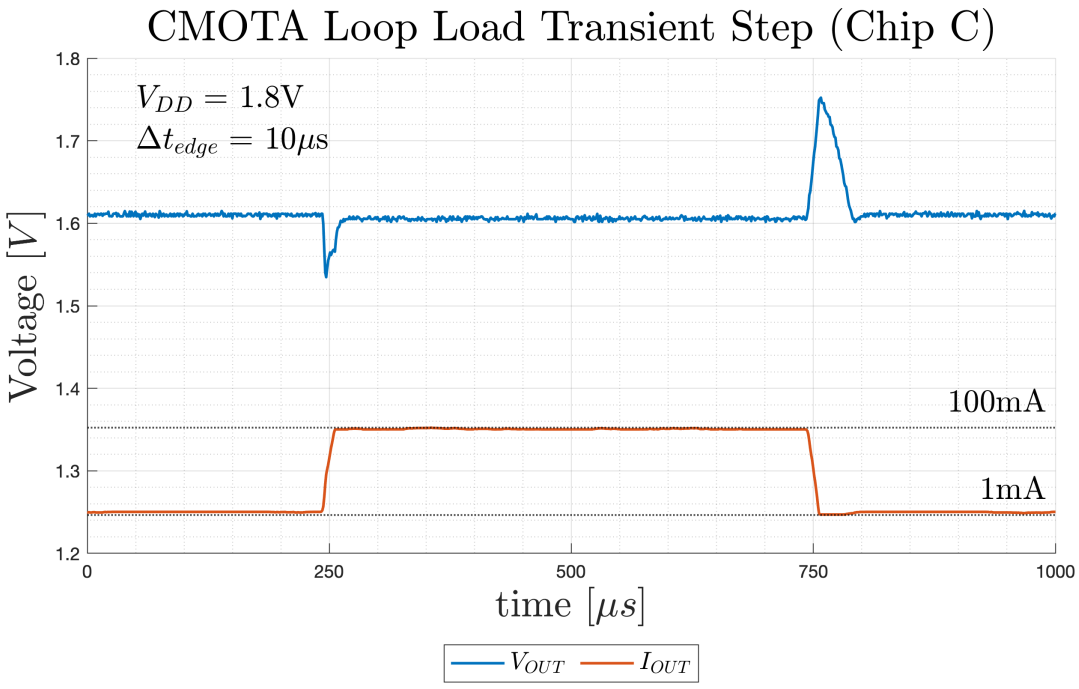


Figure F.43: CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip C

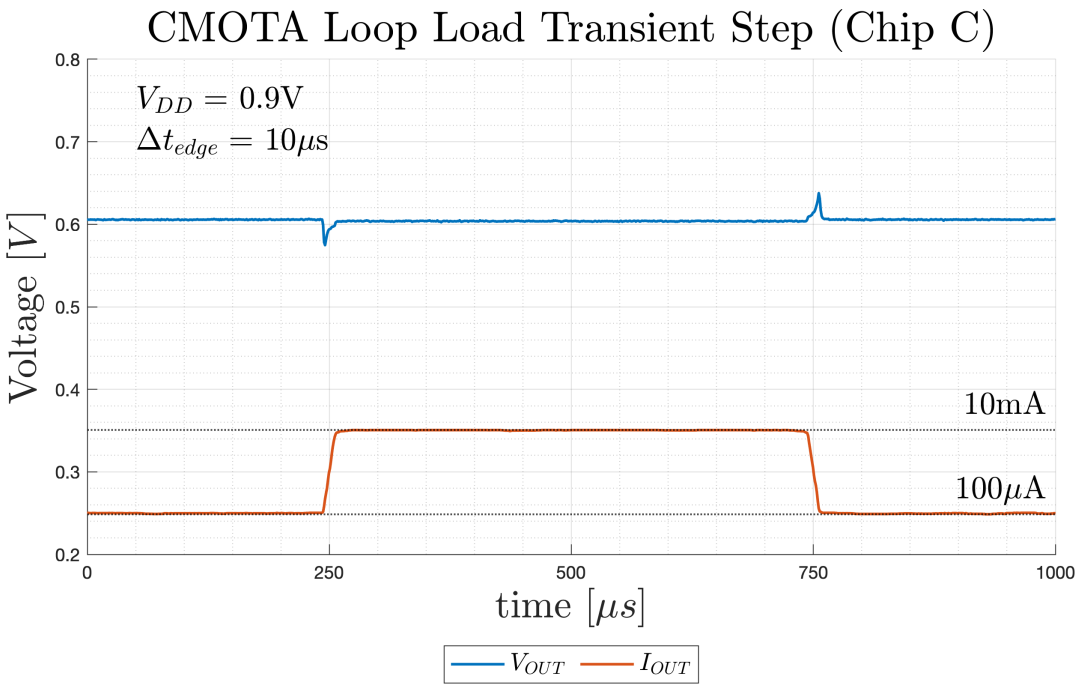


Figure F.44: CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V on Teucer Chip C

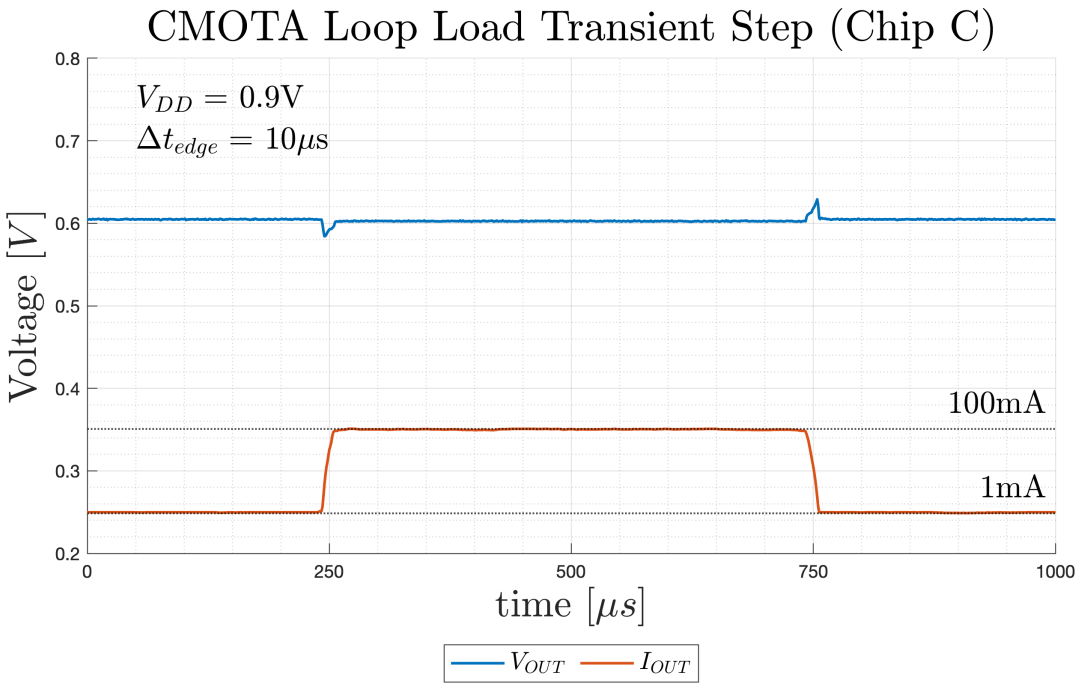


Figure F.45: CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ V on Teucer Chip C

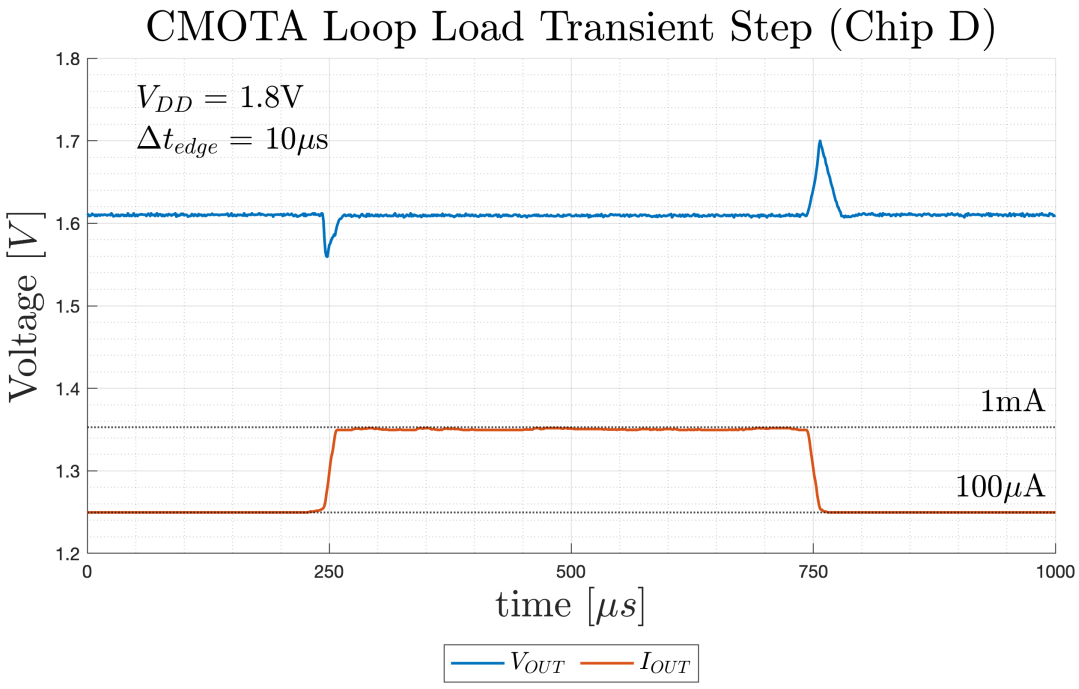


Figure F.46: CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V on Teucer Chip D

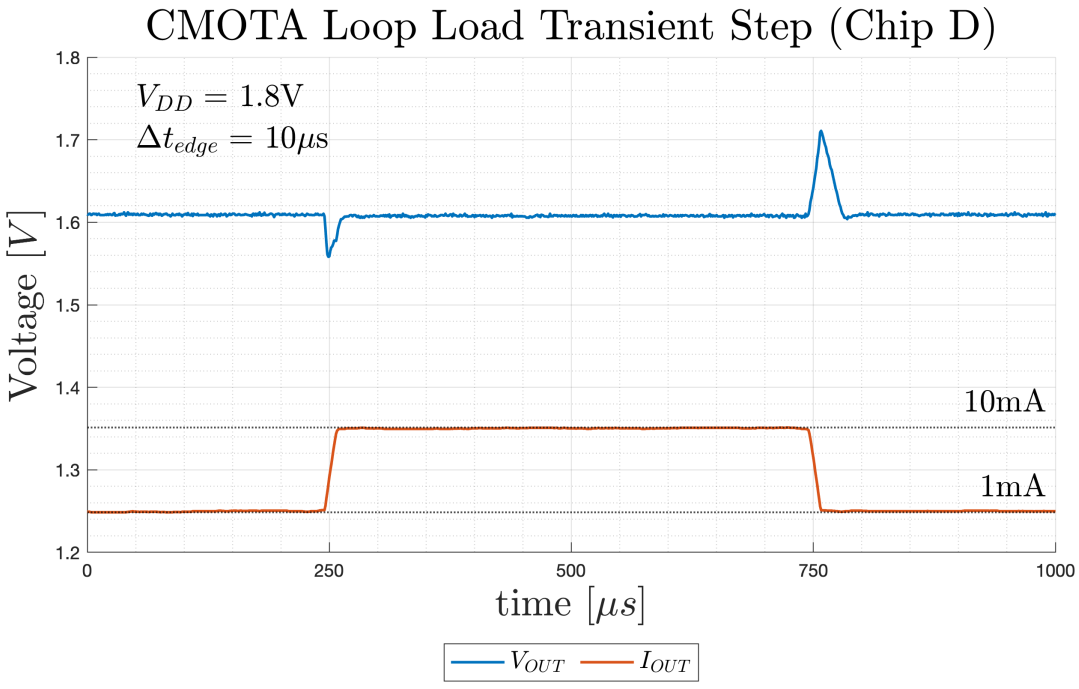


Figure F.47: CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V on Teucer Chip D

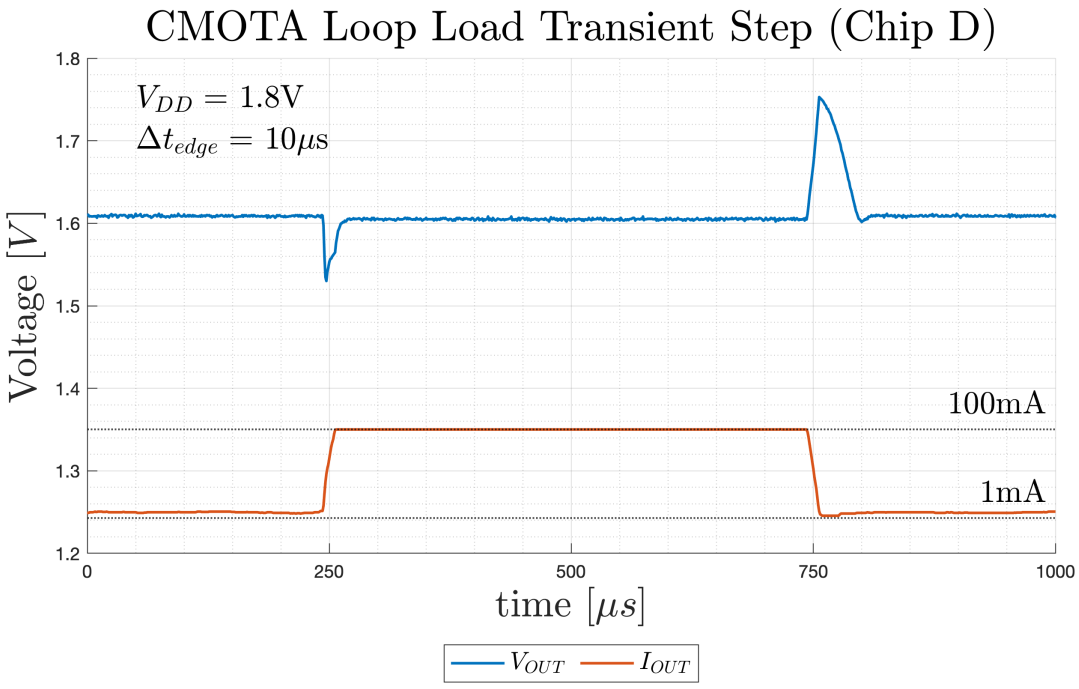


Figure F.48: CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip D

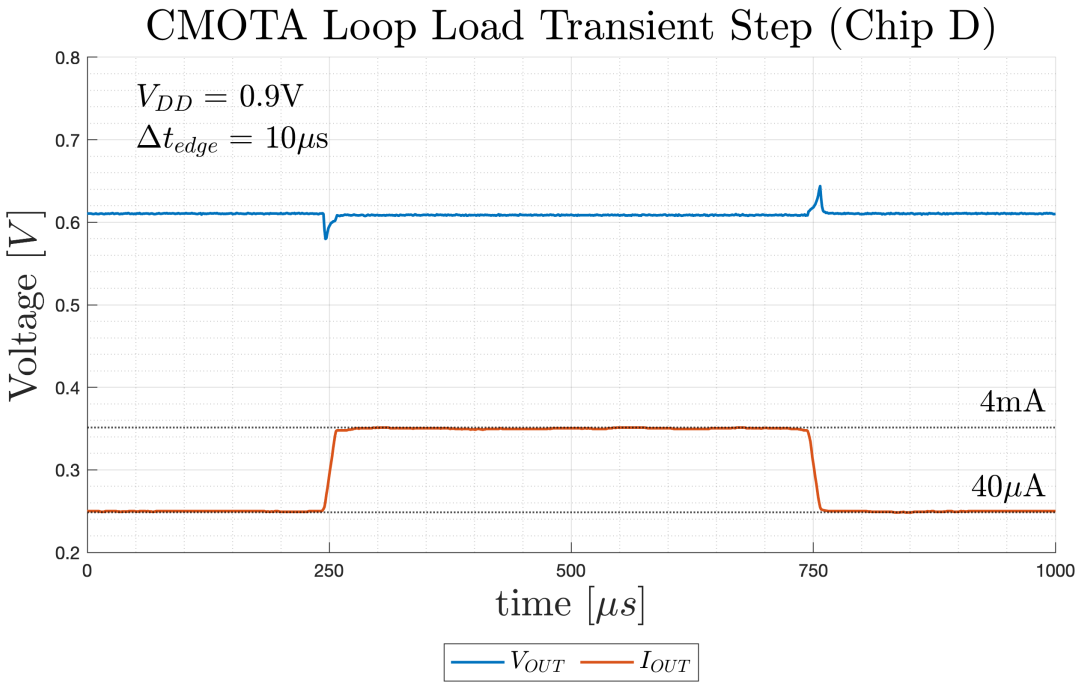


Figure F.49: CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V on Teucer Chip D

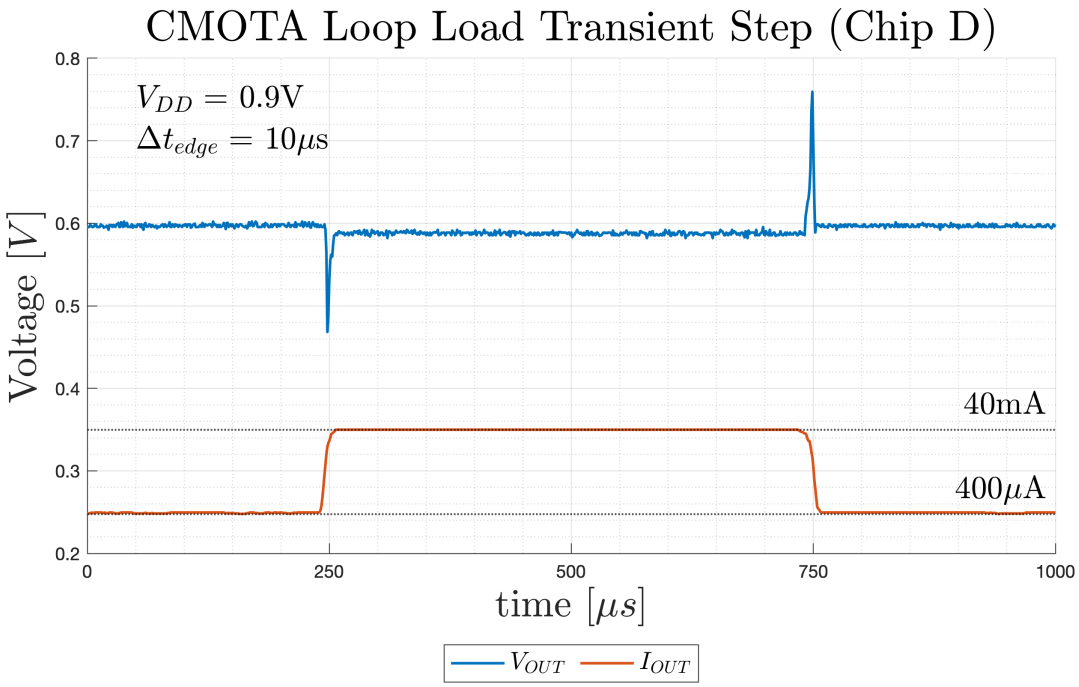


Figure F.50: CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ V on Teucer Chip D

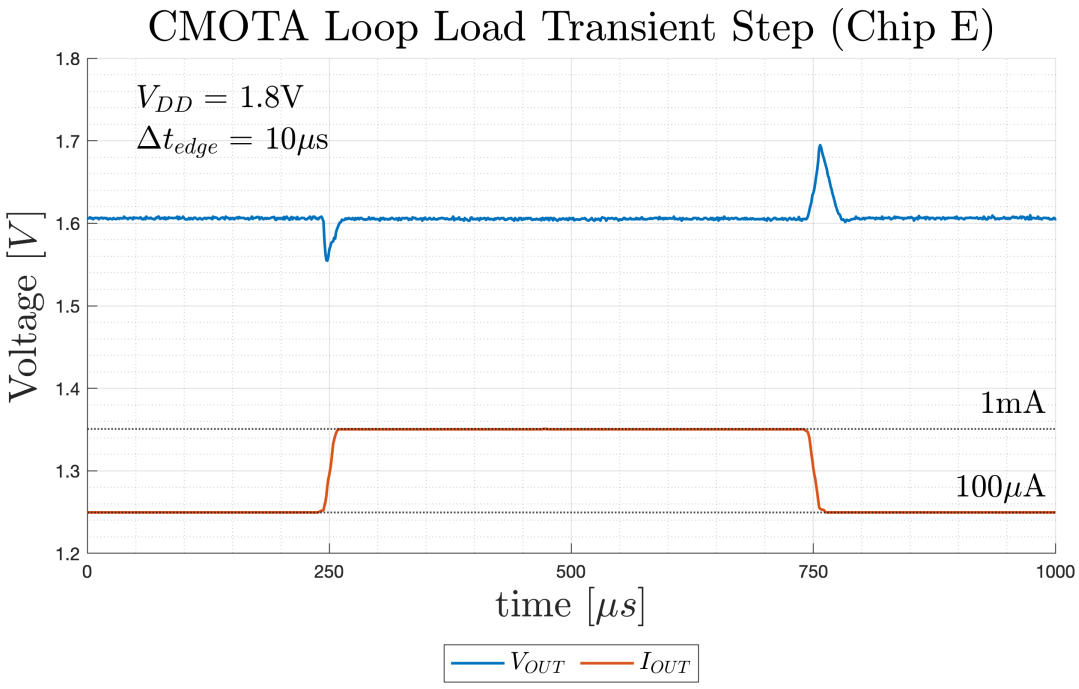


Figure F.51: CMOTA loop load step 100 µA to 1 mA with $V_{DD} = 1.8$ V on Teucer Chip E

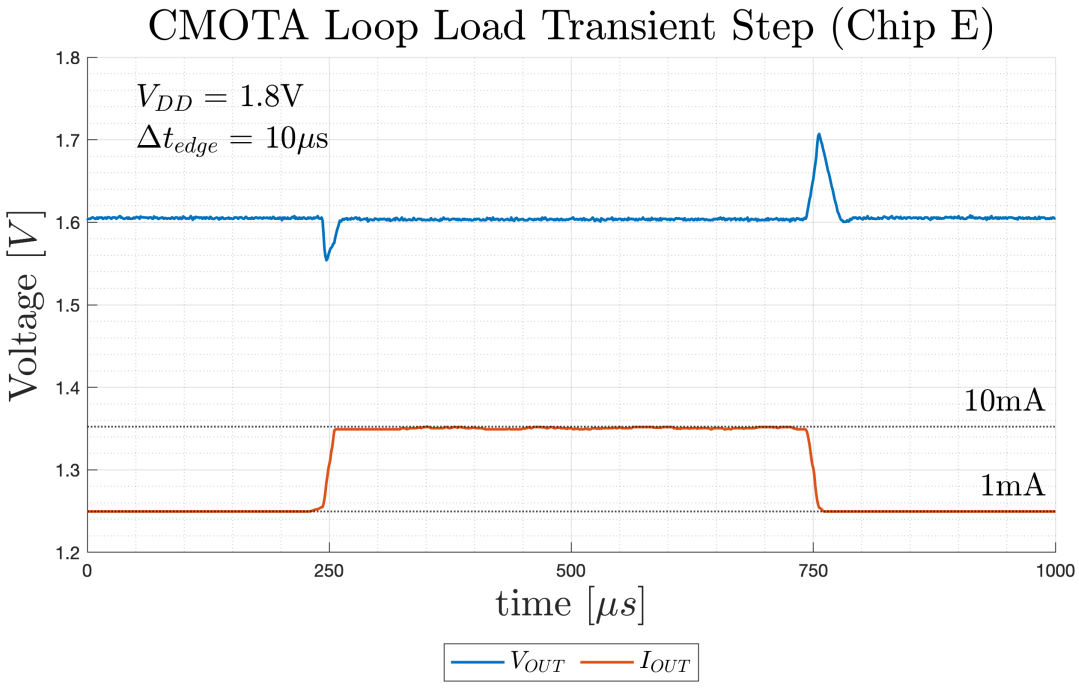


Figure F.52: CMOTA loop load step 1 mA to 10 mA with $V_{DD} = 1.8$ V on Teucer Chip E

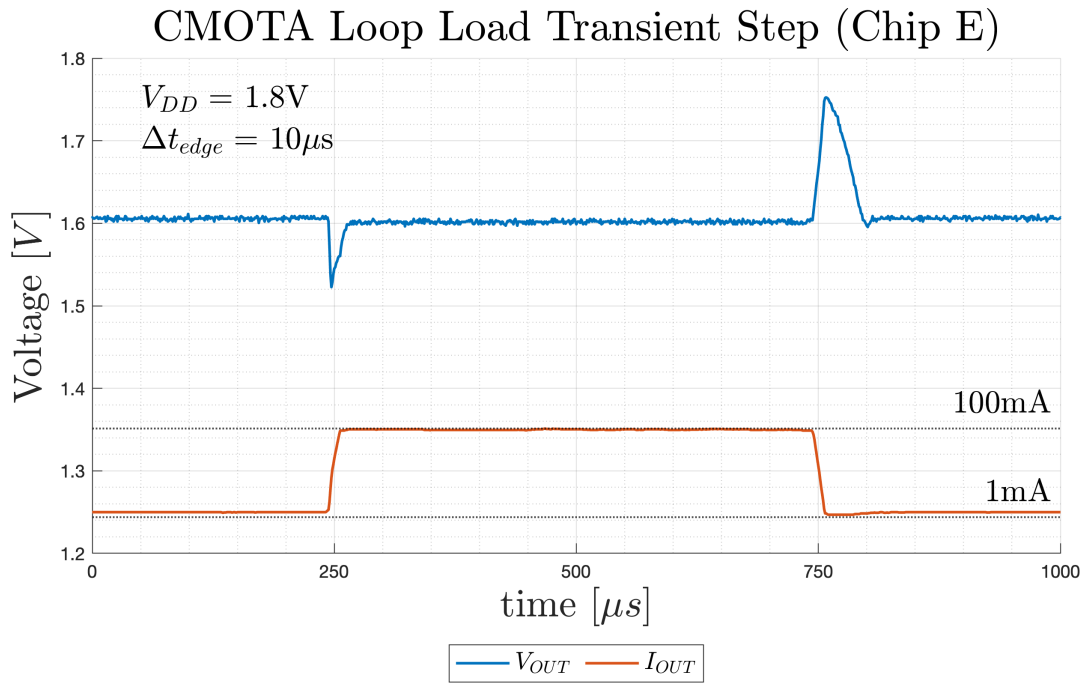


Figure F.53: CMOTA loop load step 1 mA to 100 mA with $V_{DD} = 1.8$ V on Teucer Chip E

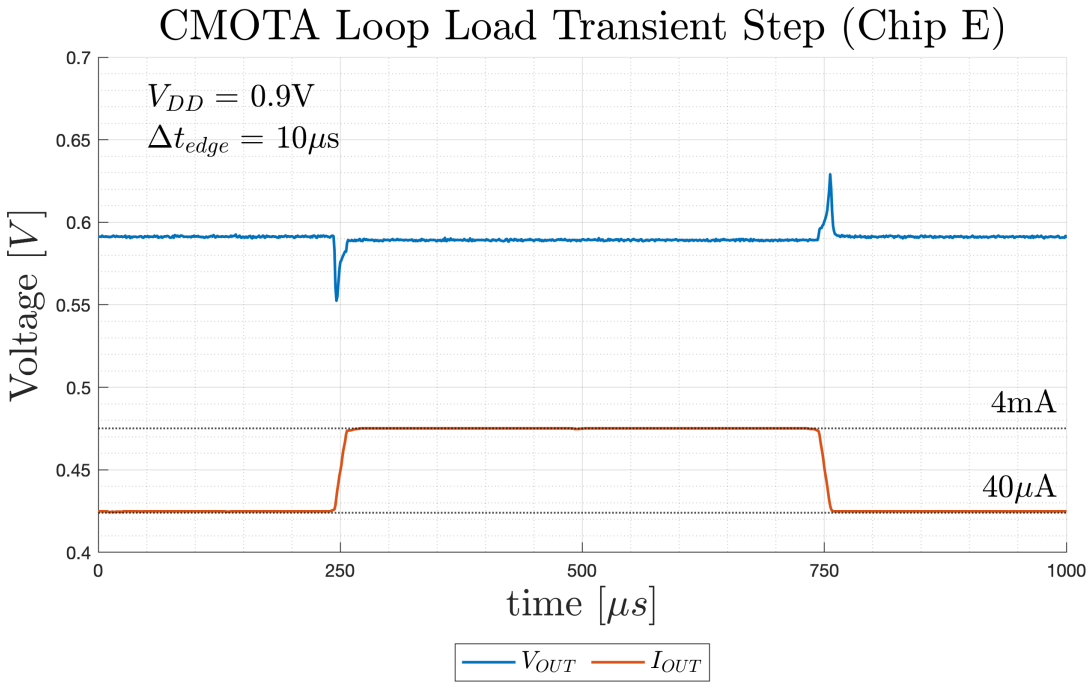


Figure F.54: CMOTA loop load step 40 µA to 4 mA with $V_{DD} = 0.9$ V on Teucer Chip E

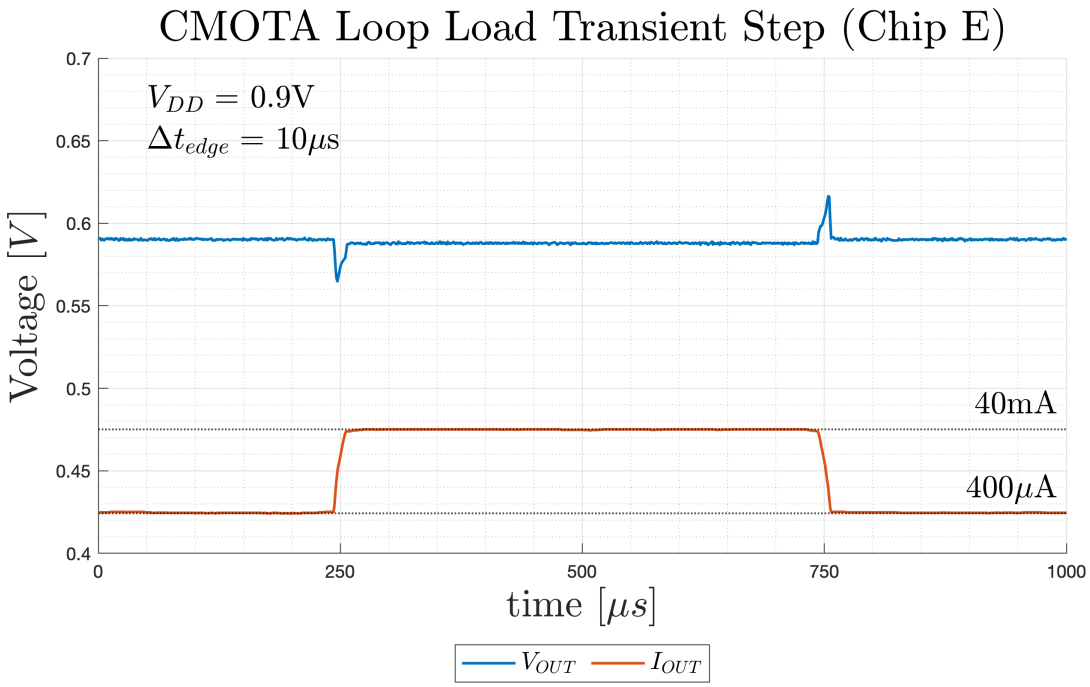


Figure F.55: CMOTA loop load step 400 µA to 40 mA with $V_{DD} = 0.9$ V on Teucer Chip E

Vita

After earning his Master of Science Degree from the University of Tennessee, Knoxville in December 2018, Jordan Michael Sangid continued to work towards a Doctor of Philosophy Degree under Professor Benjamin J. Blalock in the Integrated Circuits and Systems Laboratory (ICASL). Throughout his academic program, Sangid was selected for the 2019 Gonzalez Family Awards Outstanding Graduate Teaching Assistant, the prestigious Robert E. Bodenheimer Fellowship, Tennessee's Top 100 Fellowship, and extended opportunities from the Department of Energy's Wide Bandgap Traineeship. As a Graduate Teaching Assistant, Sangid led the effort towards a $60 000 purchase of new testing instrumentation with a corresponding donation of equipment from the Tektronix® Education Support Program valuing over $23 000. This endeavor was necessary to enhance the undergraduate electronics experience by updating the J. Frank Pierce Laboratory within the Min H. Kao Building, impacting nearly 120 students per semester. In response to all courses moving to virtual-only options amid the COVID-19 Pandemic, Sangid led an additional effort for the purchase of 100 portable electronics laboratory modules to be used by the undergraduate electronics students totaling over $50 000. As a Graduate Research Assistant, Sangid led or assisted on 3 integrated circuit fabrications and developed over 30 successful and unique printed circuit board designs all while being exposed to an enormous array research projects with Dr. Blalock and the ICASL group. After earning his PhD, Sangid continues to grow as an engineer beginning an industry career at Texas Instruments in Knoxville, Tennessee.