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DESIGN AND MEASUREMENT OF A SIX-BIT CMOS DIGITAL-TO-ANALOG CONVERTER

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Rita Najmi Horner

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DEDICATION

This thesis is dedicated to my wonderful husband Jim for his love, patience, and understanding, without which this would otherwise be impossible.

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ABSTRACT

A six-bit current steering digital-to-analog converter (DAC), integrated in a double-metal, single poly 2 μm standard n-well CMOS technology in the MOSIS process, is described. Current source matching and differential switch driving aspects are considered. Experimental results confirmed the theoretical predictions and show that the DAC is monotonic with DC differential and integral non-linearity of less than $\pm$1LSB over an input current range of 28 to 130 μA and output voltage range of 1 to 5 V; the non-linearity is greater than $\pm$1LSB for currents above 130 μA. The DAC is 298$\times$1079 μm^2 in area.

TABLE OF CONTENTS

CHAPTER PAGE

LIST OF FIGURES

FIGURE **PAGE**

FIGURE PAGE

CHAPTER 1

INTRODUCTION

Data conversion systems provide a means to interface between continuous-time signals representing measurements of physical parameters and their discrete-time digital equivalent. A digital-to-analog converter (DAC) is a device which receives digital information in the form of an N-bit word and transforms it into an analog signal. A digital-to-analog converter is an important part of many data acquisition and conversion systems, finding applications in telecommunications, digital audio tape recorders, speech recognition, digital TV, high definition TV, compact disc players, and instrumentation systems [1, 2, 3].

The rapidly developing technology of very large scale integrated (VLSI) circuits reflects the capabilities of the semiconductor industry to fabricate tens of millions of devices on a single silicon wafer. Integration of large systems on a chip requires that digital-to-analog converters be realized in CMOS technology [4]. A DAC that is part of a system on a chip is more convenient, cheaper, and potentially faster than the same DAC if external to the chip. A CMOS DAC is capable of being integrated along with memories, digital processing circuitry and other analog applications on the same chip. One of the advantages of using DACs in analog applications is the ability to keep the information in digital form, making it independent of drift with time and temperature and more immune to noise than analog information. A

CMOS DAC offers positive advantages of low-power, low-cost, and the ability to be produced in existing digital processes. The main advantages of CMOS devices are low-power consumption, high packing density, high noise immunity, ease of design, and relative ease of scaling [5]. For digital applications, CMOS devices require much less power than bipolar devices, and certain functions are available in CMOS that are not available in bipolar such as very high impedance circuits, charge scaling, and excellent analog switches.

There are many types of DACs; some produce a voltage output while others produce a current output. Some DACs have internal reference sources whereas for others it is necessary to provide external reference sources. DACs can be either unipolar or bipolar. The input signal may be either in serial digital words or in parallel digital words. Parallel digital-to-analog converters are usually very fast, but require many precision components.

In this thesis only parallel converters with external reference sources and external output stages are considered. The topologies that will be considered are:

- Capacitor Network
- Current Source Network
- Resistor Network

The purpose of this thesis is to design, test, and measure a six-bit binary-weighted current DAC in a 2 μm CMOS process after investigating the benefit of this network compared with the other DAC networks. This is not for the purpose of

inventing a new topology, but the objective is to design and characterize a reusable design that can be implemented as part of other future projects using standard 2 μm MOSIS's process. For the purpose of limiting the focus of this thesis and also due to the nonfeasibility of performing AC testing with the available test set up, only the DC performance of the DAC is considered here.

The body of this thesis is organized as follows:

Chapter 2 describes the basic principle of operation of a DAC, the basic topologies of different DAC networks. Also discussed is the feasibility of designing a Binary-Weighted Current Source DAC in a 2 μm CMOS process. Each considered topology will be described and compared with the others.

Chapter 3 describes the design details of the various elements of the current source DAC topology. Analytical results are presented and compared to simulation results when appropriate to validate the theoretical results. In this chapter the DAC layout is also described.

Chapter 4 presents and explains the measured performance results of the DAC. Comparison of experimental results with expected results is made.

Chapter 5 is a conclusion and discusses directions for future work.

CHAPTER 2

REVIEW OF DIFFERENT DAC TOPOLOGIES

Chapter 1 presented some of the advantages of a CMOS DAC as part of a system on a chip. In this chapter, the feasibility of implementing a current source DAC in the MOSIS process is discussed. Several different topologies of DACs are compared, and the relative advantages and disadvantages of each one are discussed.

The various blocks in a basic form of a DAC, as shown in Figure 2.1, are the binary switches, a scaling network, reference input(s), and output stage(s). Most commercially available DACs rely on precision analog elements such as capacitors, current sources, or resistors [6]. The inputs are digital words of N bits $(b_1, b_2, b_3, ..., b_N)$, and the scaling network and binary switches operate on the reference input(s) to convert the digital word to either a voltage, a current, or a charge signal. The output voltage V_{out} can be expressed as

$$V_{out} = HV_{ref}D \tag{2.1}$$

where H is a scaling factor, V_{ref} is the reference input voltage, and D is a fractional binary input given by

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + ... + \frac{b_N}{2^N} \tag{2.2}$$

b_i are the individual bits that are 1 or 0 as determined by the digital word; b_1 is the most significant bit (MSB), and b_N is the least significant bit (LSB). Similarly,

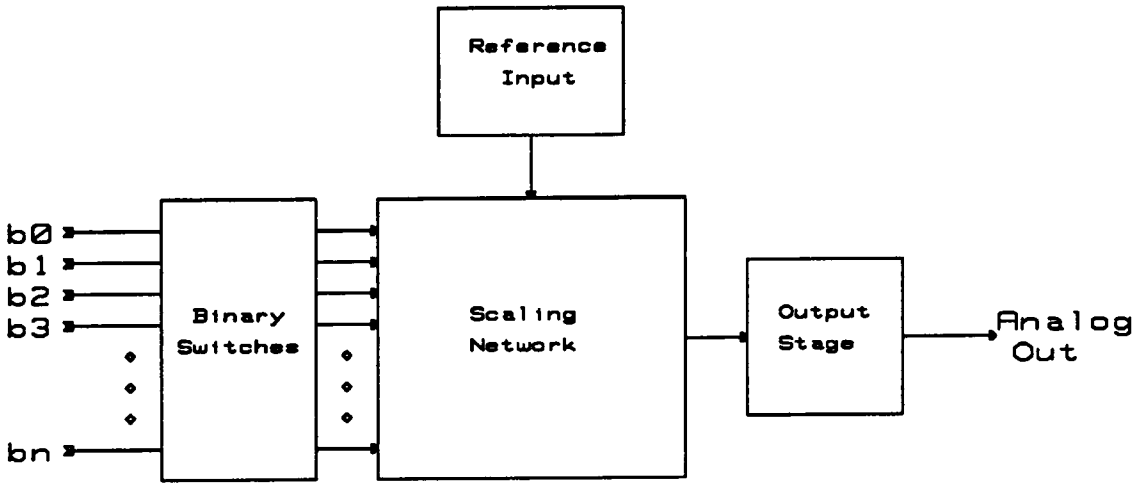

Figure 2.1: Block diagram of a DAC

the output current I_{out} can be expressed as

$$I_{out} = HI_{ref}D \tag{2.3}$$

where I_{ref} is the reference input current.

In order to restrict the scope of this thesis, only topologies for parallel converters with external reference sources and external output stages are considered. The main focus of comparison of each topology is the scaling network of each DAC. Since the references are external, the DAC is called a multiplying DAC (MDAC). The topologies considered are:

1. Charge-Scaling Binary-Weighted Capacitor
2. Charge-Scaling C-2C Ladder Network
3. Current-Scaling Binary-Weighted Resistor
4. Voltage-Scaling R-2R Ladder Network

5. Binary-Weighted Current Source

Some of the major parameters concerned in designing a DAC are full-scale absolute accuracy, relative accuracy, linearity, monotonicity, settling time, conversion time, size, power consumption, design cycle time, and cost.

Full-scale (FS) absolute accuracy is the difference between the measured full-scale output and the ideal full-scale output before any adjustments.

Relative accuracy is the worst-case input to output error of a data converter, expressed as a percent of the full-scale, referred to the converter reference. The error consists of offset, gain, and linearity components.

There are two types of linearity specifications that may be applied to a data acquisition system. The first, called integral linearity, is defined as the maximum deviation from a best straight line drawn through the transfer function curve. The second type of linearity is referred to as differential linearity, which is a measure of the maximum deviation of any given quantum interval in the system's transfer function from its theoretical value.

Monotonicity assures the user that the output will increase or decrease as the input is increased or decreased respectively.

Settling time is the time elapsed from the application of a full-scale step input to the time when the output has entered and remained within a specified error band around its final value.

Conversion time is the time required for a DAC to complete a single conversion to the specified resolution and linearity for a full-scale digital input change.

2.1 Charge-Scaling Binary Weighted-Capacitor Network

In MOS technology, capacitors are being widely used for designing precision analog circuits such as data converters because of their excellent matching characteristics [7]. Many MOS technologies have two layers of polysilicon. The additional layer provides an efficient capacitor structure referred to as a double-poly capacitor. But in processes with only one layer of polysilicon, alternative structures must be used to implement capacitive elements. The MOS transistor itself can be used as a capacitor when biased in the triode region, the gate forming one plate and the source, drain and channel forming another [8].

Binary-weighted DAC networks are the simplest of all DAC topologies [7]. As shown in Figure 2.2, a charge-scaling binary-weighted capacitor network for a DAC consists of a reference voltage source and a set of binary-weighted capacitors which have an associated switch. The bottom plates of all the capacitors are typically switched between V_{ref} and ground, and the top plates are all connected to one common point. This converter works on a charge redistribution principle in which the network binarily divides the total charge applied to the capacitor array. The resulting output voltage can be expressed as

$$V_{out} = V_{ref} \sum_{i=1}^{N} \frac{b_i}{2^i} \tag{2.4}$$

where b_i is either ONE or zero. This structure has the advantage that the conversion accuracy is dependent on the accuracy of the capacitor ratio rather than the absolute capacitor values, but the required total capacitance rises exponentially

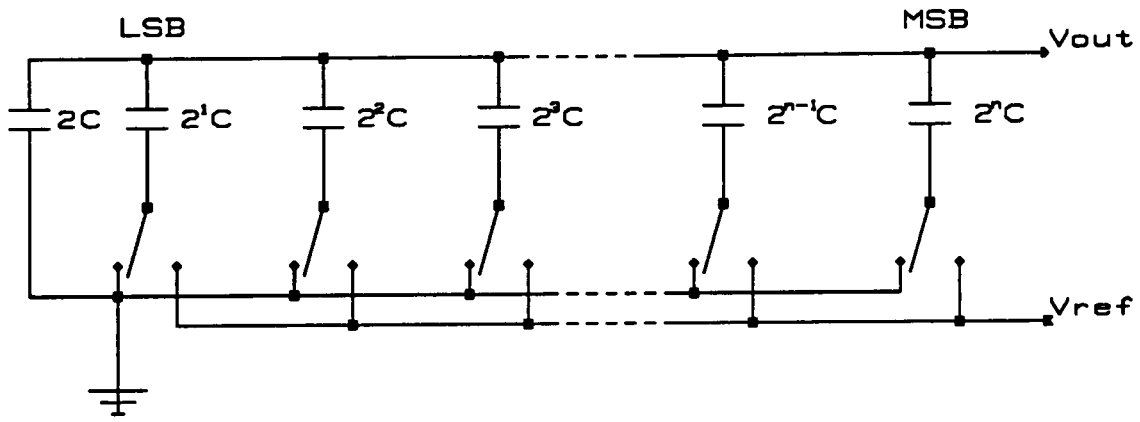

Figure 2.2: Charge-scaling binary-weighted capacitor network

with the number of bits. Some of the examples of this network can be found in [9] and [10].

A problem with the weighted capacitor network is that it requires a wide range of capacitor values for a large number of bits, and as the ratio of capacitors increases the accuracy of the capacitor ratio will decrease [11]. In this manner, the accuracy of the capacitors and the required area are the two factors that limit the number of bits used. A mismatch in the binary ratio of capacitors in the network causes non-linearity. Linearity is very sensitive to ratio change in the large capacitors and not very dependent on the smaller capacitors, which have greater allowable tolerance [7]. For an ideal case with matched capacitors, the output voltage is a regular staircase, when plotted with respect to the digital input values, as shown in Figure 2.3 for a three-bit DAC. But when there is a mismatch in the capacitor ratios the output voltage will differ from the ideal case and causes non-linearity.

Matching errors in capacitors can be caused by misalignment of the mask during the etching phase of the photomask process. This is a poorly controlled lateral

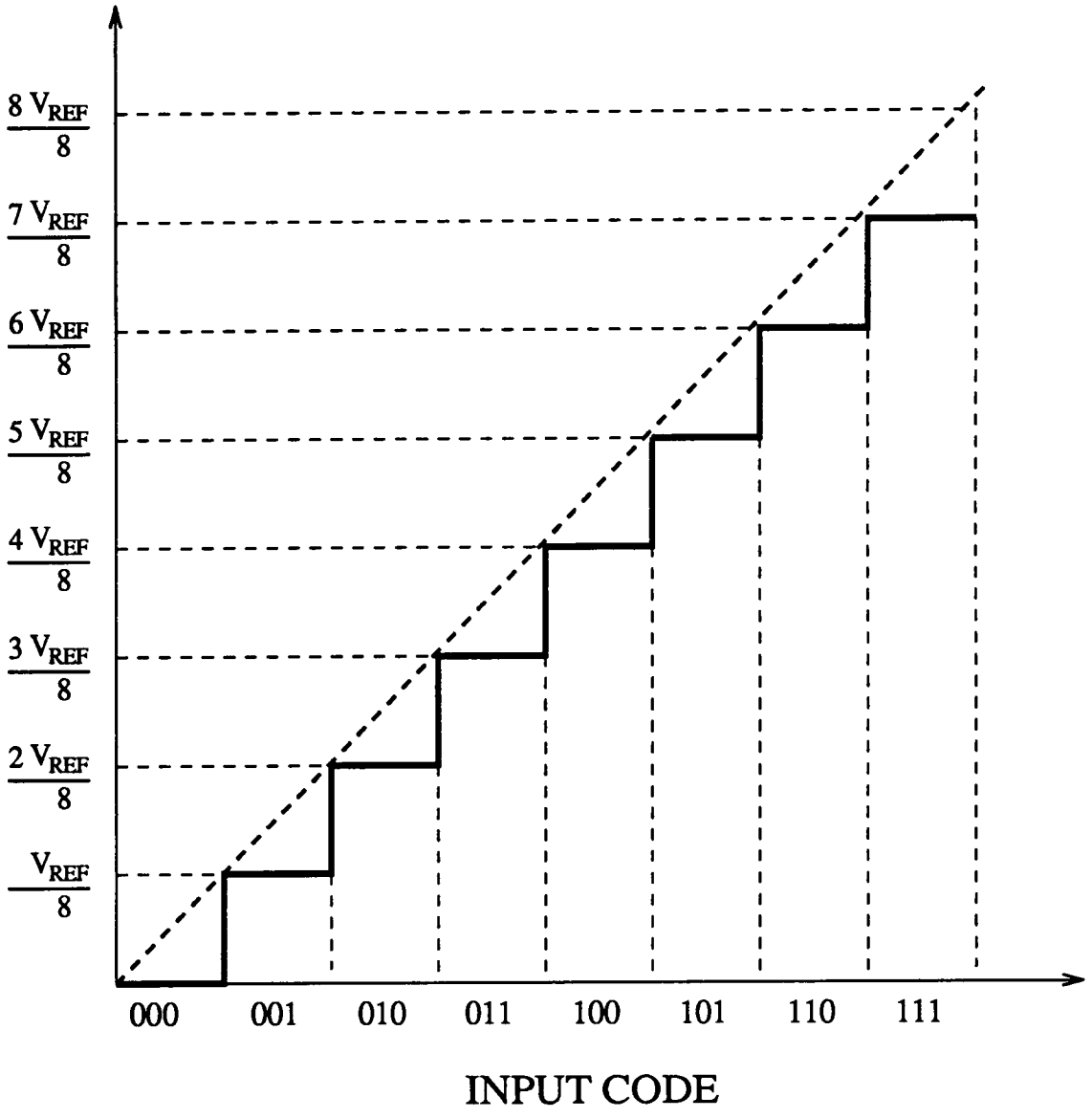

Figure 2.3: Input-output characteristics of a three-bit DAC

etch that is called undercut. Undercut error can be minimized by using parallel identical small size capacitors to form a larger capacitor. Capacitor ratio error can also be caused by nonuniform oxide growth conditions. Errors from this source can be minimized by utilizing a common centroid geometry and by improved oxide growth techniques [7].

2.2 Charge-Scaling C-2C Ladder Network

For an n-bit binary-weighted network DAC, the capacitor value spread is 2^n, making it very difficult to maintain the capacitor ratios in spite of their realization as multiples of smaller capacitors. In a charge-scaling C-2C ladder network as shown in Figure 2.4, the required total capacitance rises linearly, and the value spread is only two. The C-2C converter consists of a reference voltage source, switches, and a C-2C ladder network which consists of only two values of capacitors, one of which has twice the magnitude of the other. The bottom plates of the smaller capacitors are typically switched between V_{ref} and ground while the top plates of the respective capacitors are separated by the larger capacitors in π-type network. However, the conversion accuracy is now sensitive to the capacitor's top and bottom plate parasitics as well as to interconnect parasitics, since all of these appear at the intermediate nodes of the ladder [12]. The resulting output voltage can be expressed as

$$V_{out} = V_{ref} \sum_{i=1}^{N} \frac{b_i}{2^i} \tag{2.5}$$

In a C-2C ladder array, two is the largest ratio between capacitors; however,

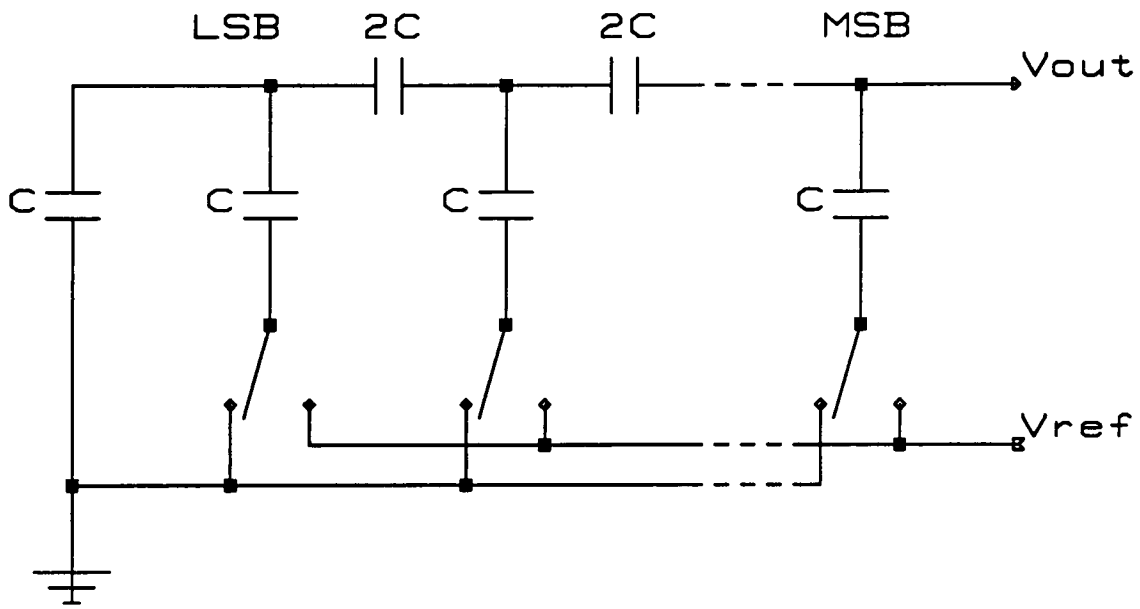

Figure 2.4: Charge-scaling C-2C ladder network

this introduces an additional matching constraint upon the large voltage dependent parasitic capacitors in the array in order to maintain the required voltage divider precision. While the effects of top plate and interconnect parasitics can be controlled by either choosing a large enough value of C or by mask trimming or both; those of the bottom plate parasitic are serious, since its value is quite large [13].

2.3 Current-Scaling Binary-Weighted Resistor Network

Another binary-weighted DAC network is the weighted resistor or current summing network of Figure 2.5. The network consists of a series of binary-weighted resistors, all tied to a common summing point. Each successive resistor doubles in value when moving from the most significant bit to the least significant bit.

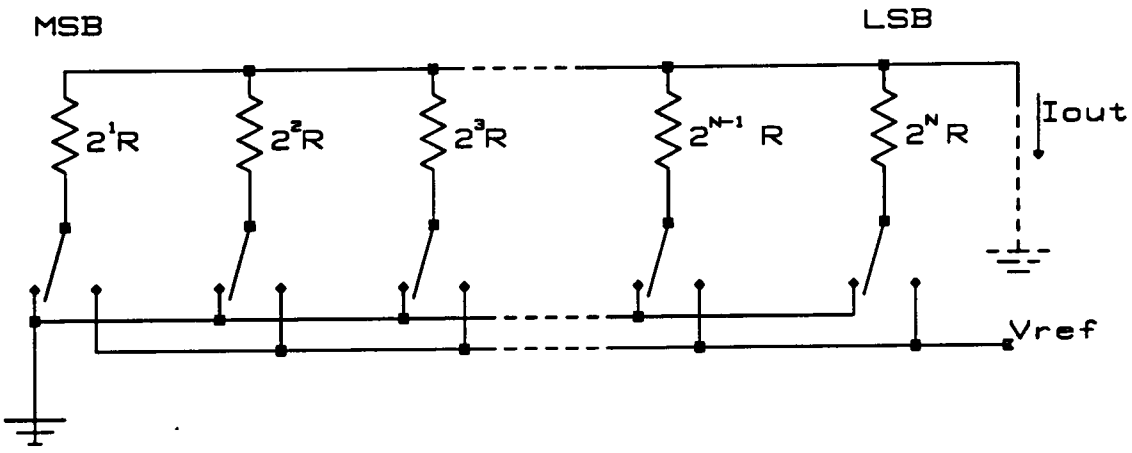

Figure 2.5: Current-scaling binary-weighted resistor network

When a given bit input is a logic ONE, the associated resistor is connected to the reference voltage, V_{ref} by a switch. When a resistor is not used, it is connected to ground. In the same way as most other binary-weighted networks, the required circuit device ratio rises exponentially with the number of bits. A wide range of resistor values is required for a large number of bits. This circuit faces similar accuracy and area problems as all the other weighted DAC networks. The resulting output current can be expressed as

$$I_{out} = V_{ref} \sum_{i=1}^{N} \frac{b_i}{2^i R} \tag{2.6}$$

where R is half of the value of the MSB resitor.

An important disadvantage of the resistor string is that the linearity of the transfer characteristic can be strongly affected by the differential temperature coefficient and the voltage coefficient of the resistors in the string. The area required for the DAC becomes large if the number of bits is increased. Also, the conversion speed of the converter will be sensitive to parasitic capacitances at each of its in-

ternal nodes. These resistors are typically either diffusion resistors or polysilicon resistors. The diffused layer used to form the source and drain of the n-channel and p-channel devices can be used to form a diffused resistor, or the one layer of polysilicon that is required in silicon-gate MOS technologies to form the gates of the transistors is often used to form polysilicon resistors. The typical resistance of diffused resistors is 10 to 100 $\Omega/\square$, and that of polysilicon resistors is 30 to 200 $\Omega/\square$ [14]. For diffused layers, the resistivity of material varies with the depth of the diffused layer and the surface impurity concentrations. Metal offers the least resistance and is therefore the most commonly used material to carry heavy currents, but the channels offer the most resistance. In CMOS technologies, the well region can also be used as the body of a resistor. It is a relatively lightly doped region and when used as a resistor provides a sheet resistance of much higher $\Omega/\square$. However, well-resistors are slightly voltage dependent and they always have large parasitic capacitances. A MOS transistor biased in the triode region can be used in many circuits to perform the function of a resistor, but there is a high degree of non-linearity in the resulting resistor element [8].

2.4 Voltage-Scaling R-2R Ladder Network

The other resistor network commonly used for DACs is the R-2R ladder circuit, as seen in Figure 2.6. The use of repeated resistance values in the R-2R network is efficient and the number of required resistor values are limited. But in CMOS technology, resistors have the least accurate absolute value; and analog circuits

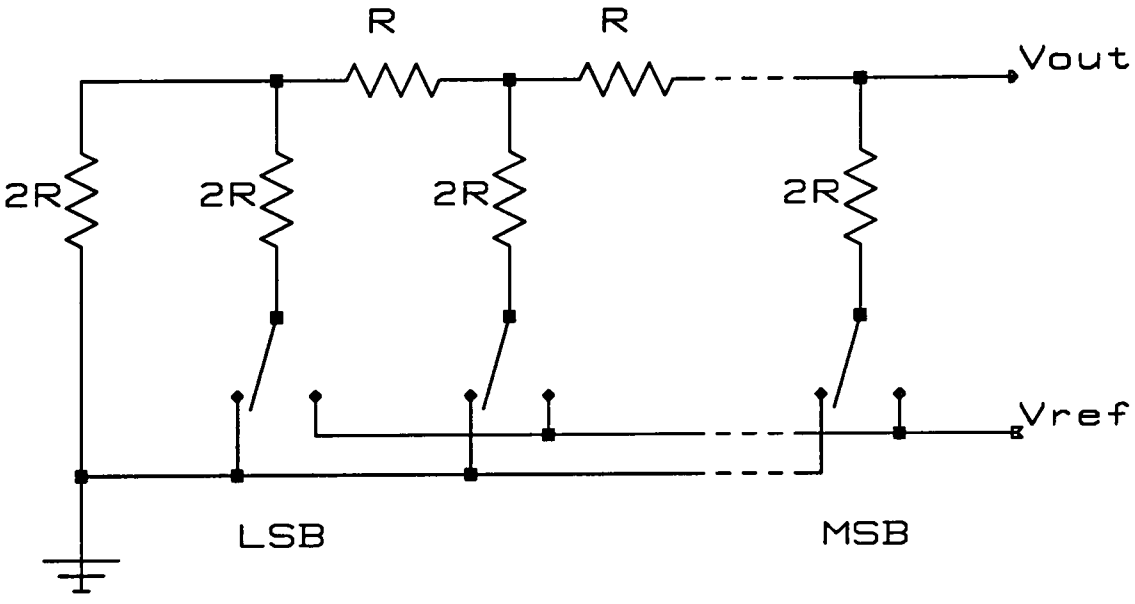

Figure 2.6: Voltage-scaling R-2R ladder network

should be based on ratios of resistors, where absolute accuracy is not too critical. The resulting output voltage of an R-2R network can be expressed as

$$V_{out} = V_{ref} \sum_{i=1}^{N} \frac{b_i}{2^i} \tag{2.7}$$

2.5 Binary-Weighted Current Source Network

The last type of topology considered is the binary-weighted current source network. As shown in Figure 2.7, the network consists of binary-weighted current sources, a reference current source, and a set of switches. Each successive current source doubles in value when moving from the LSB to the MSB. When a given bit input is a logic ONE, the associated current source is connected to the output, I_{out} by a precision switch. When a current source is not used, it is connected to

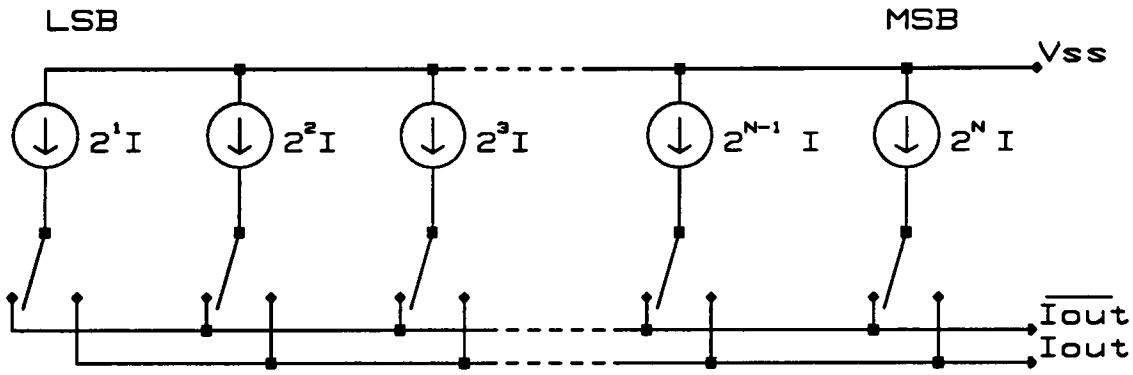

Figure 2.7: Binary-weighted current source network

$\overline{I_{out}}$. The problem with this circuit is that the size of the current sources increases exponentially with the number of input bits, and as the ratio of current sources increases, the accuracy of the current source ratio will decrease. Matching error in current sources can be caused by misalignment of the mask either because of mechanical error or error caused by temperature mismatch. A poorly controlled process could result due to surface-state-charge and ion-implanted-charge effects. Random matching errors in transistors can also be caused due to oxide effects. There are correction or prevention methods for each of the errors mentioned above. These methods are discussed in the following chapter. The resulting output current of the network can be expressed as

$$I_{out} = I_{ref} \sum_{i=1}^{N} 2^i b_i \tag{2.8}$$

where I_{ref} is the reference input current equal to half of least significant bit current.

Compared to current sources or resistor arrays, capacitors are easier to fabricate and more accurate in matching. But the limitations on using capacitor charge redistribution techniques are the large chip area required by the capacitors and

low speed. In technologies with one layer of polysilicon, an additional process step must usually be added to produce a capacitor of suitable quality. At the same time, a VLSI process may not even offer linear capacitors. Resistor networks are useful in technologies which contain no capacitors, but they are the least accurate passive components available in a MOS process. These factors are good motivations to study the matching behavior of a MOS transistor current source and the possibility of designing and fabricating a current source DAC network in a 2 μm CMOS process.

CHAPTER 3

DESIGN OF A BINARY-WEIGHTED CURRENT SOURCE NETWORK

In this chapter the design of a six-bit binary-weighted current source DAC will be described. After presenting the theoretical aspects of this type of DAC, the circuit for this research will be described. As shown in Figure 2.7, a binary-weighted current source network for a DAC consists of a set of binary-weighted current sources and a set of two-way current switches. For the purposes of this thesis, the combination of the current source and a pair of two-way current switches will be referred to as a unit cell. In this network, the size of the current sources increases exponentially with the number of input bits. A six-bit DAC requires six different size current sources, the values of which double when moving from the LSB to the MSB. A unit cell with a cascode current source will also be discussed.

PMOS transistors have a larger mismatch in conductance constants than do NMOS transistors. Poorer gate oxide capacitance matching and larger mobility variation are the two contributors of this mismatch in PMOS devices [15]. PMOS devices need to be about twice the size of NMOS devices for the same current, since the hole mobility is half of the electron mobility. Because of these facts it was decided to design the unit cell using NMOS transistors.

3.1 Unit Cell

A unit cell of the binary-weighted current source network consists of a current source and a switch to direct the current either to I_{out} or to $\overline{I_{out}}$ depending on the input settings. It has been demonstrated that for best matching of ratioed current sources it is better to form the larger current sources as a parallel collection of the smallest valued source [11]. This concept will be extended for this DAC by constructing the higher order bits from multiple copies of the unit cell. Figure 3.1 shows the implementation of a unit cell using NMOS devices. The operation of this circuit will now be described.

Transistor M_1 is connected in a current mirror configuration with diode connected transistor M_{ref}. The node V_{ref} is shared by all of the unit cells in the DAC. The reference current I_{ref} is injected into the drain of M_{ref} developing a voltage which is applied to the gate of transistor M_1, causing a current to flow in M_1. Transistor M_{ref} is operating in the saturation region because its drain-to-source voltage (V_{ds}) is equal to its gate-to-source potential (V_{gs}). For proper operation, transistor M_1 must also be operating in the saturation region.

The second part of the unit cell is the differential pair which steers the output current into I_{out} or $\overline{I_{out}}$ depending on the state of the differential select voltages V_{in} and $\overline{V_{in}}$. The differential pair consists of two matched NMOS transistors, M_{sw1} and M_{sw1b} which may be operating in either the linear or the saturation regions.

There are number of important characteristics of the unit cell that must be considered. They are:

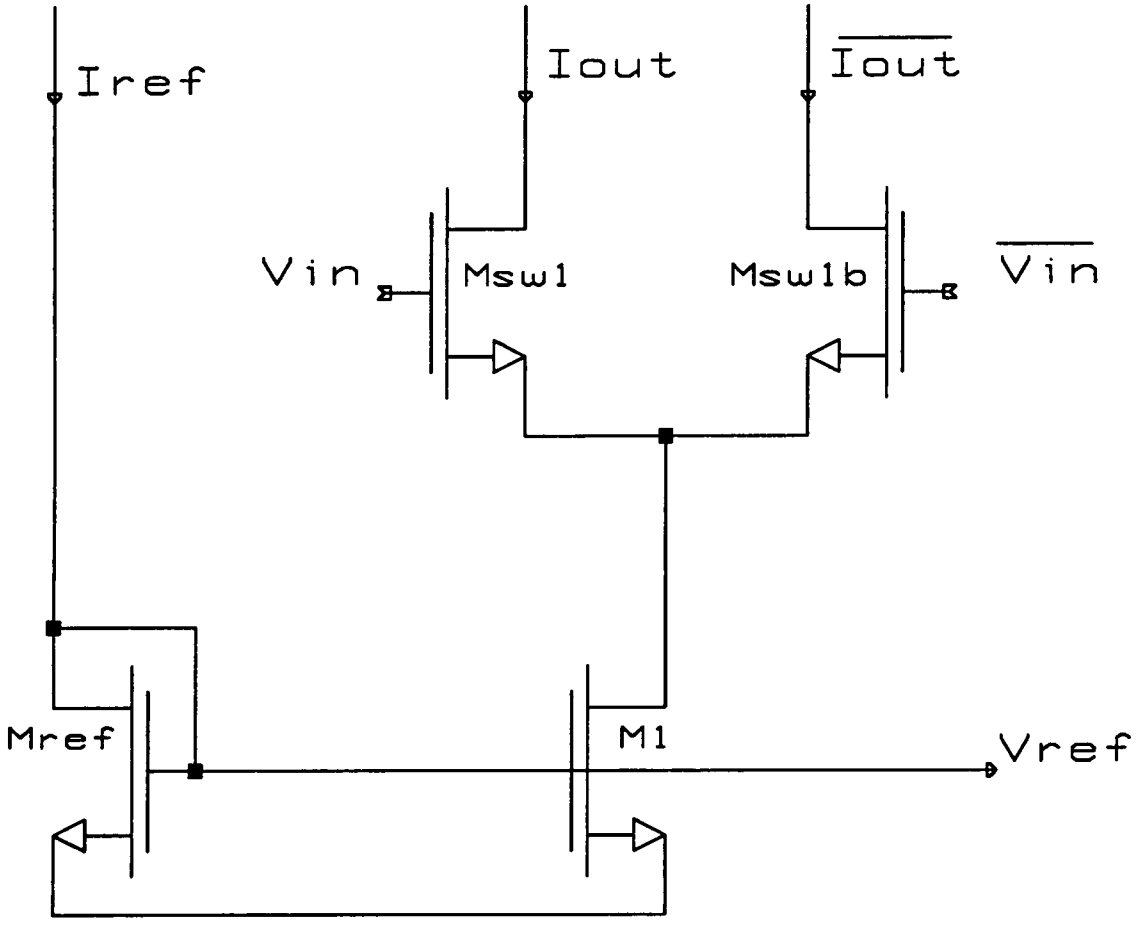

Figure 3.1: A unit cell of a simple current source network

- Output Current Characteristics
- DC Characteristics of the Switch
- Output Impedance
- Minimum Output Voltage and Maximum Output Current
- AC Switching Characteristics.

In the following sections, each of these characteristics will be examined in detail.

3.1.1 Output Current Characteristics

Using the level 1 large-signal model, the drain current of an n-channel MOS device with positive polarities of voltages and currents, operating in saturation and strong inversion can be expressed as

$$I_d = \frac{\mu_0 C_{ox} W}{2L}(V_{gs} - V_t)^2(1 + \lambda V_{ds}) \tag{3.1}$$

where $V_{ds} \geq (V_{gs} - V_t)$ and $V_{gs} \geq V_t$. The various parameters of Equation 3.1 are defined as

μ_0 = surface mobility of the channel for the NMOS device $(cm^2/volt-seconds)$

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ = capacitance per unit area of the gate oxide (F/cm^2)

ϵ_{ox} = dielectric constant of silicon dioxide = $3.9\epsilon_0$ (F/cm)

$\epsilon_0 = 8.85 \times 10^{-14}$ (F/cm)

t_{ox} = thickness of the gate dielectric (m)

W = effective channel width (μm)

L = effective channel length (μm)

The threshold voltage for an n-channel transistor is given by [11] as

$$V_t = V_{t0} + \gamma \left[\sqrt{2|\phi_f| + V_{sb}} - \sqrt{2|\phi_f|} \right] \tag{3.2}$$

V_{t0} = zero-bias threshold voltage ($volt$)

$\gamma = \frac{\sqrt{2q\epsilon_{si}N_{sub}}}{C_{ox}}$ = body-effect coefficient ($volt^{1/2}$)

$\phi_f = \frac{kT}{q} \ln\left(\frac{N_{sub}}{n_i}\right)$ = strong inversion surface potential ($volt$)

V_{sb} = voltage from the source-to-bulk ($volt$)

ϵ_{si} = dielectric constant of silicon = $11.7\epsilon_0$ (F/cm)

k = Boltzmann's constant = 1.381×10^{-23} ($J/°K$)

T = temperature ($°K$)

q = electron charge = 1.6×10^{-19} ($coulomb$)

N_{sub} = substrate concentration or doping (cm^{-3})

n_i = intrinsic carrier concentration (cm^{-3})

λ = channel length modulation parameter ($volt^{-1}$)

The channel length modulation parameter is defined in [11] as

$$\lambda = \frac{1}{L_{eff}V_{ds}} \left[\frac{2\epsilon_{si}}{qN_{sub}} \right]^{1/2} \left\{ \frac{V_{ds} - V_{ds}(sat.)}{4} + \left[1 + \left(\frac{V_{ds} - V_{ds}(sat.)}{4} \right)^2 \right]^{1/2} \right\} \tag{3.3}$$

$V_{ds}(sat.)$ = drain-to-source voltage in saturation region ($volt$)

$L_{eff} = L - 2(LD)$ = actual effective channel length (μm)

LD = lateral diffusion (μm)

Since M_1 is connected in parallel with M_{ref}, it will have the same V_{gs}. The currents

through M_{ref} and M_1 can be written as

$$I_{ref} = \frac{\beta_{ref}}{2}(V_{gs} - V_{t_{ref}})^2(1 + \lambda V_{ds_{ref}}) \tag{3.4}$$

$$I_1 = \frac{\beta_1}{2}(V_{gs} - V_{t_1})^2(1 + \lambda V_{ds_1}) \tag{3.5}$$

where $V_{ds_{ref}} \geq (V_{gs} - V_{t_{ref}})$, $V_{ds_1} \geq (V_{gs} - V_{t_1})$, $\beta_{ref} = \frac{\mu_0 C_{ox} W_{ref}}{L_{ref}}$, and $\beta_1 = \frac{\mu_0 C_{ox} W_1}{L_1}$. Equations 3.4 and 3.5 can be combined to obtain

$$I_1 = I_{ref}\left(\frac{L_{ref}W_1}{W_{ref}L_1}\right)\left(\frac{1 + \lambda V_{ds_1}}{1 + \lambda V_{ds_{ref}}}\right)\left(\frac{V_{gs} - V_{t_1}}{V_{gs} - V_{t_{ref}}}\right)^2 \tag{3.6}$$

Assuming the threshold voltages are the same, Equation 3.6 can be simplified to

$$I_1 = I_{ref}\left(\frac{L_{ref}W_1}{W_{ref}L_1}\right)\left(\frac{1 + \lambda V_{ds_1}}{1 + \lambda V_{ds_{ref}}}\right) \tag{3.7}$$

If $\lambda \simeq 0$ or if $V_{ds_{ref}} = V_{ds_1}$, Equation 3.7 can be further simplified to

$$I_1 = I_{ref}\left(\frac{L_{ref}W_1}{W_{ref}L_1}\right) \tag{3.8}$$

Thus, I_1 is a multiple of I_{ref} whose value is determined by device geometry. In practice this value of I_1 will be obtained only when the voltage at the drain of M_1 (V_{ds_1}) is equal to V_{gs}. Variation of the drain voltage will result in corresponding changes in I_1 due to the output resistance of M_1.

3.1.2 DC Characteristics of the Switch

An ideal switch has zero ON resistance (R_{ON}) and zero OFF leakage current (I_{OFF}) [11] when operating in the linear region.

M_{sw1} and M_{sw1b}, as shown in Figure 3.1, may be operating in either the linear or the saturation regions for correct unit cell operation. Assuming that the two

devices are identical and that M_{sw1} is the ON transistor in the linear region and M_{sw1b} is in the cutoff region, the drain currents of M_{sw1} and M_{sw1b} can be expressed as

$$I_{out} = \beta_{sw1}\left[(V_{gs_{sw1}} - V_{t_{sw1}})V_{ds_{sw1}} - \frac{{V_{ds_{sw1}}}^2}{2}\right](1 + \lambda_{sw1}V_{ds_{sw1}}) \tag{3.9}$$

$$\overline{I_{out}} = 0 \tag{3.10}$$

where $\beta_{sw1} = \frac{\mu_0 C_{ox} W_{sw1}}{L_{sw1}}$, $V_{ds_{sw1}} \leq (V_{gs_{sw1}} - V_{t_{sw1}})$, $V_{gs_{sw1b}} < 0$ since $\overline{V_{in}} = 0$, and $V_{ds_{sw1b}} \geq 0$. Assuming the drain-to-source voltage of M_{sw1} is small, and neglecting λ effect, Equation 3.9 can be simplified to

$$I_{out} \simeq \beta_{sw1}(V_{gs_{sw1}} - V_{t_{sw1}})V_{ds_{sw1}} \tag{3.11}$$

When M_{sw1} is in the saturation region, the drain current of M_{sw1} can be expressed as

$$I_{out} = \frac{\beta_{sw1}}{2}(V_{gs_{sw1}} - V_{t_{sw1}})^2(1 + \lambda_{sw1}V_{ds_{sw1}}) \tag{3.12}$$

where $V_{ds_{sw1}} \geq (V_{gs_{sw1}} - V_t)$. Neglecting λ effect, Equation 3.12 can be simplified to

$$I_{out} = \frac{\beta_{sw1}}{2}(V_{gs_{sw1}} - V_{t_{sw1}})^2 \tag{3.13}$$

From Equation 3.11, the large-signal ON channel resistance, R_{ON} of the transistor M_{sw1} for small values of $V_{ds_{sw1}}$, in the linear region can be described as

$$R_{ON} = \frac{\partial V_{ds_{sw1}}}{\partial I_{out}} = \frac{1}{\beta_{sw1}(V_{gs_{sw1}} - V_{t_{sw1}})} = \frac{L_{sw1}}{\mu_0 C_{ox} W_{sw1}(V_{gs_{sw1}} - V_{t_{sw1}})} \tag{3.14}$$

Therefore, R_{ON} of the switch is inversely proportional to W_{sw1}/L_{sw1} of M_{sw1} in the linear region. A similar result can be obtained for transistor M_{sw1b}, when M_{sw1b} is the ON transistor in the linear region and M_{sw1} is in the cutoff region.

The switch leakage current can be due to subthreshold current and to surface-leakage currents, which are in the 10 pA range at room temperature [11]. For this circuit $V_{gs} < 0$ when the switch is OFF. Therefore, there will be no subthreshold currents. Surface-leakage currents can be ignored for this design, since the least significant bit of the DAC will have at least 1 μA of current and the effect of picoAmps of leakage current can be neglected.

3.1.3 Output Impedance

An ideal current source is nonexistent in the real world; there is no physical device which will deliver a constant current regardless of the load resistance to which it is connected or of the voltage across its terminals. A practical current source can be modeled as shown in Figure 3.2 as an ideal current source (I_i) in parallel with an internal resistance (R_i). In this case R_i is the output impedance of M_1. The total output current of the current source is the sum of the current through the ideal current source and the current through R_i. Since the output impedance of simple current mirror is not infinite, variation of voltage at the drain of M_1 will change I_1.

Figure 3.3 shows the simplified small-signal model of the unit cell of Figure 3.1. This model is used for calculating the output impedance. Summing the current at the output node gives

$$I_{out} = g_{m_{sw1}} V_{gs_{sw1}} + g_{mbs_{sw1}} V_{bs_{sw1}} + (V_{out} - V_{ds_1}) g_{ds_{sw1}} \tag{3.15}$$

where $g_{m_{sw1}}$ is the transconductance of M_{sw1}, $g_{mbs_{sw1}}$ is the transconductance

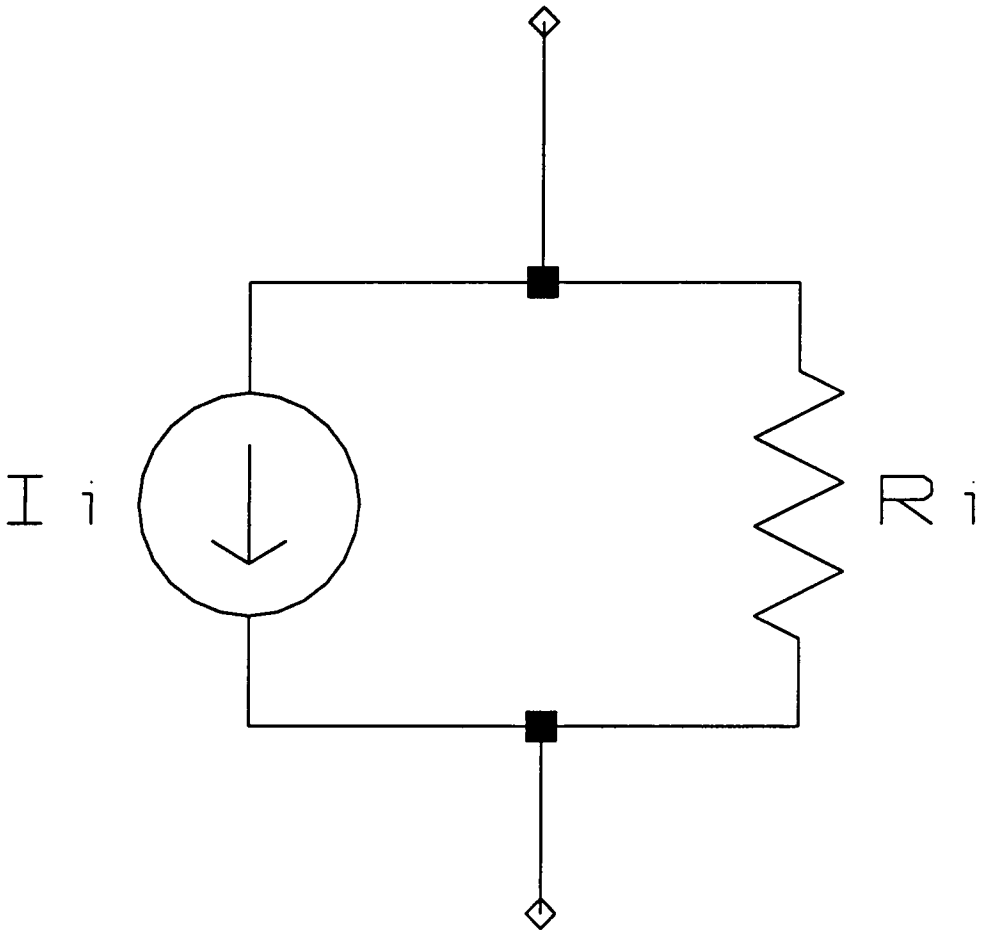

Figure 3.2: Practical current source model

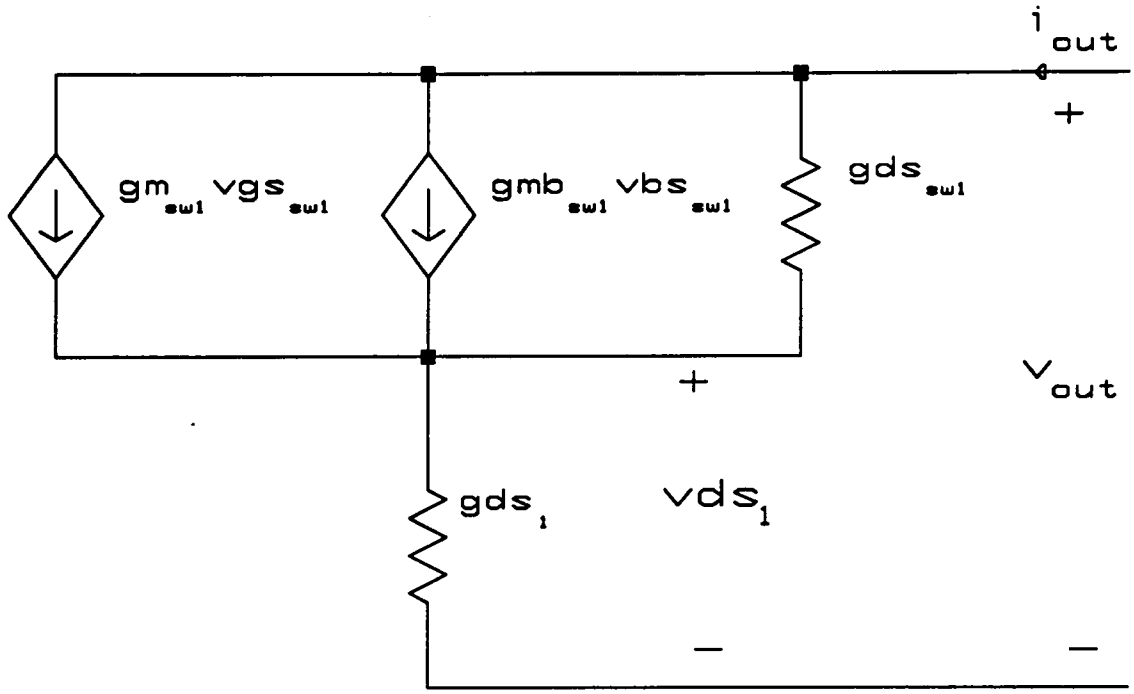

Figure 3.3: Output impedance model of a simple unit cell

due to body effect, and $g_{ds_{sw1}}$ is the drain-to-source conductance of M_{sw1}. Since $V_{ds_1} = I_{out} r_{ds_1}$, $g_{mbs_{sw1}} = \eta_{sw1} g_{m_{sw1}}$ [11], M_1 is in the saturation region, and M_{sw1} is in either the linear or the saturation region, the output impedance r_{out} can be calculated as

$$r_{out} = \frac{V_{out}}{I_{out}} = r_{ds_1} + r_{ds_{sw1}} + g_{m_{sw1}} r_{ds_1} r_{ds_{sw1}} (1 + \eta_{sw1}) \tag{3.16}$$

The various parameters of Equation 3.16 when M_{sw1} is in the linear region are defined as

$$\eta_{sw1} = \frac{\gamma}{2\sqrt{2|\phi_f| + V_{bs_{sw1}}}} \tag{3.17}$$

$$r_{ds_1} = \frac{\partial V_{ds_1}}{\partial I_1} = \frac{(1 + \lambda_1 V_{ds_1})}{I_1 \lambda_1} \tag{3.18}$$

$$r_{ds_{sw1}} = \frac{\partial V_{ds_{sw1}}}{\partial I_{out}} = \frac{(1 + \lambda_{sw1} V_{ds_{sw1}})}{[\beta_{sw1}(V_{gs_{sw1}} - V_{t_{sw1}} - V_{ds_{sw1}})(1 + \lambda_{sw1} V_{ds_{sw1}})^2] + I_{out}\lambda_{sw1}} \tag{3.19}$$

$$g_{m_{sw1}} = \frac{\partial I_{out}}{\partial V_{gs_{sw1}}} = \beta_{sw1} V_{ds_{sw1}}(1 + \lambda_{sw1} V_{ds_{sw1}}) \tag{3.20}$$

r_{out} terms can be further simplified to

$$r_{ds_1} \simeq \frac{1}{I_1 \lambda_1} \tag{3.21}$$

$$r_{ds_{sw1}} \simeq \frac{1}{\beta_{sw1}(V_{gs_{sw1}} - V_{t_{sw1}} - V_{ds_{sw1}})} \tag{3.22}$$

$$g_{m_{sw1}} \simeq \beta_{sw1} V_{ds_{sw1}} \tag{3.23}$$

And when M_{sw1} is in the saturation region

$$r_{ds_{sw1}} \simeq \frac{1}{I_{out}\lambda_{sw1}} \tag{3.24}$$

$$g_{m_{sw1}} \simeq \sqrt{2\beta_{sw1} I_{out}} \tag{3.25}$$

Larger output resistance results in a more constant current over the range of V_{out} values.

3.1.4 Minimum Output Voltage and Maximum Output Current

In order for the unit cell to perform properly, M_1 should be in the saturation region, and M_{sw1} or M_{sw1b} can be either in the linear region or the saturation region of operation. In the linear region a MOS device does not make a good current source, because of the low output impedance. But in the saturation region MOS devices make good current sources. Therefore, in order for M_1 to perform properly, V_{ds_1} should be greater than or equal to $(V_{gs_1} - V_{t_1})$.

By reducing the value of the minimum output voltage $V_{out(min.)}$, there will be a larger range of V_{out} values over which the current source will work properly. For the minimum output voltage calculation, the switches are assumed to operate in the linear region. Using Equation 3.9 and neglecting the λ effect, $V_{out(min.)}$ of a simplified unit cell in Figure 3.4, for M_{sw1} to stay in saturation can be given by

$$V_{out(min.)} = (V_{in} - V_{t_{sw1}}) - \sqrt{(V_{in} - V_{t_{sw1}})^2 + V_{ds_1(sat.)}\left[V_{ds_1(sat.)} - 2(V_{in} - V_{t_{sw1}})\right] - \frac{2L_{sw1}I_{out}}{\mu_0 C_{ox} W_{sw1}}} \quad (3.26)$$

where V_{in} is the input of the switch M_{sw1}. Since $I_{out} = I_1$, $V_{ds_1(sat.)} = (V_{gs_1} - V_{t_1})$, $(V_{gs_1} - V_{t_1}) = \sqrt{\frac{2I_1}{\beta_1}}$, and neglecting the λ effect, $I_{ref} = I_{out}$, the new value of $V_{out(min.)}$ can be expressed as

$$V_{out(min.)} = (V_{in} - V_{t_{sw1}}) - \sqrt{(V_{in} - V_{t_{sw1}})\left[(V_{in} - V_{t_{sw1}}) - 2\sqrt{\frac{2I_{out}L_1}{\mu_0 C_{ox} W_1}}\right] + \frac{2I_{out}}{\mu_0 C_{ox}}\left(\frac{L_1}{W_1} - \frac{L_{sw1}}{W_{sw1}}\right)} \quad (3.27)$$

For a given I_{out}, $V_{out(min.)}$ can be reduced by increasing the W/L values. Similar results can be calculated for switch M_{sw1b}.

To calculate the maximum output current $I_{out(max.)}$, $(V_{gs1} - V_{t_1})$ of the current source transistor increases as I_{out} increases. From Equation 3.5, this is given by

$$V_{gs1} - V_{t_1} = \sqrt{\frac{2I_{out}}{\beta_1}} \quad (3.28)$$

As I_{out} increases, V_{ds1} decreases. For the correct operation of the current source, M_1 should be in the saturation region and its drain-to-source voltage is given by

$$V_{ds_1} = V_{in} - V_{t_1} - V_{t_{sw1}} - \sqrt{\frac{2I_{out}L_{sw1}}{3\mu_0 C_{ox} W_{sw1}}} \quad (3.29)$$

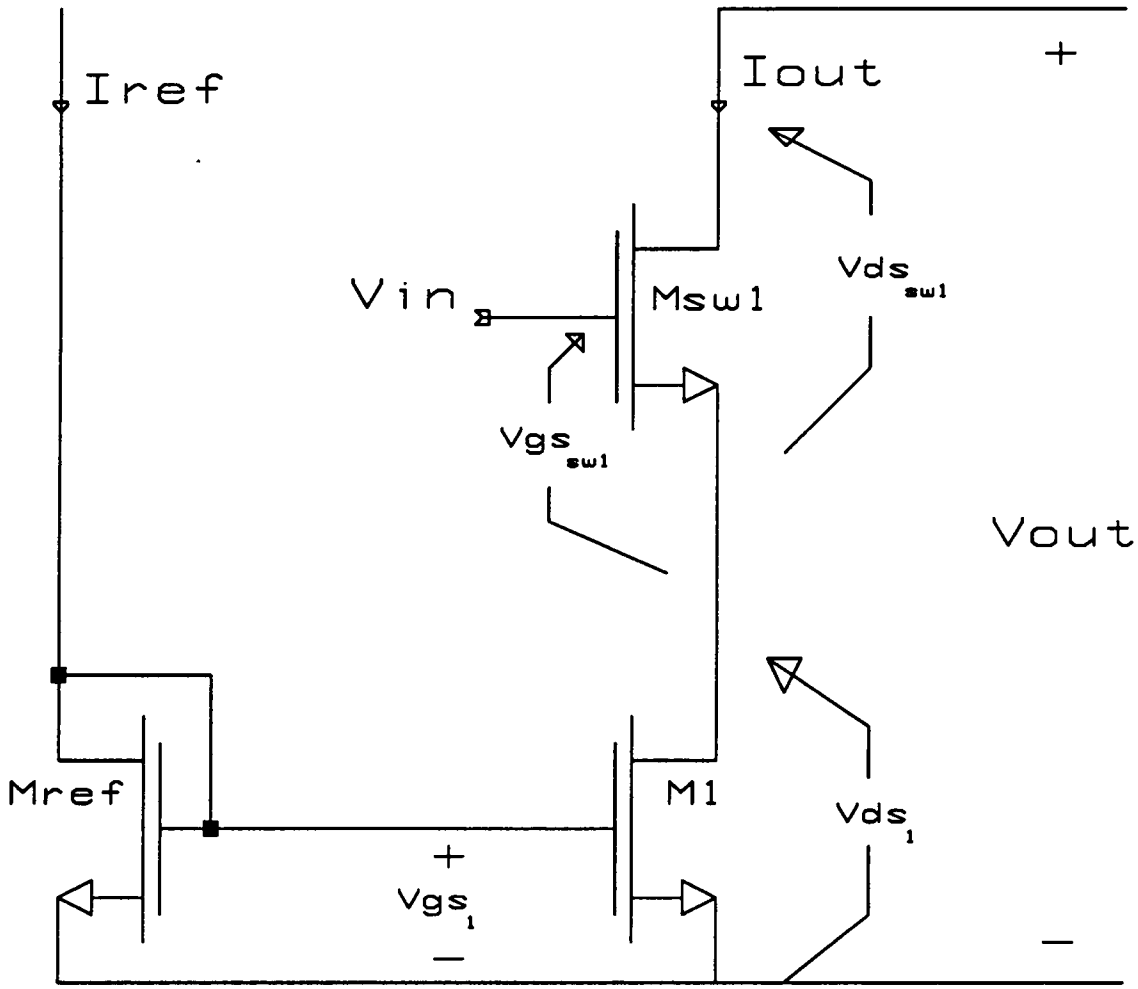

Figure 3.4: Simplified unit cell for minimum $V_{out(min.)}$ calculation

Setting Equation 3.28 equal to Equation 3.29, and solving for $I_{out(max.)}$ gives

$$I_{out(max.)} = \mu_0 C_{ox} (V_{in} - V_{t_{sw1}} - V_{t_1})^2 \left[\frac{3W_1 W_{sw1}}{2\left(\sqrt{2W_1 L_{sw1}} + \sqrt{6L_1 W_{sw1}}\right)^2} \right] \quad (3.30)$$

Due to body effect, $V_{bs_{sw1}}$ is not equal to zero, therefore $V_{t_{sw1}}$ must be calculated from Equation 3.2. $I_{out(max.)}$ can be increased by increasing the widths of the transistors.

3.1.5 AC Switching Characteristics

Due to the gate-to-channel parasitic capacitances, gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) as shown in Figure 3.5, transitions on the input of the switches will generate some feedthrough currents. These capacitances are functions of the transistor sizes of the switches and change value according to the region of the operation that the transistor is in. The differential pair switches will be either in the cutoff region or linear/saturation region of operation. The gate-to-substrate capacitance is assumed to be negligible.

In the cutoff region, there is no channel, and hence the total gate capacitance, C_g is the sum of the gate-to-source and gate-to-drain overlap capacitances. The total gate capacitance of a switch in the cutoff region can be approximated as

$$C_g \simeq 2C_{ox} LDW_{eff} \quad (3.31)$$

where W_{eff} is the actual effective channel width.

In the linear region of the switch $V_{gs} > V_{ds} + V_t$, the channel exists and extends from the drain to the source. Therefore, C_g is the sum of the overlap capacitance

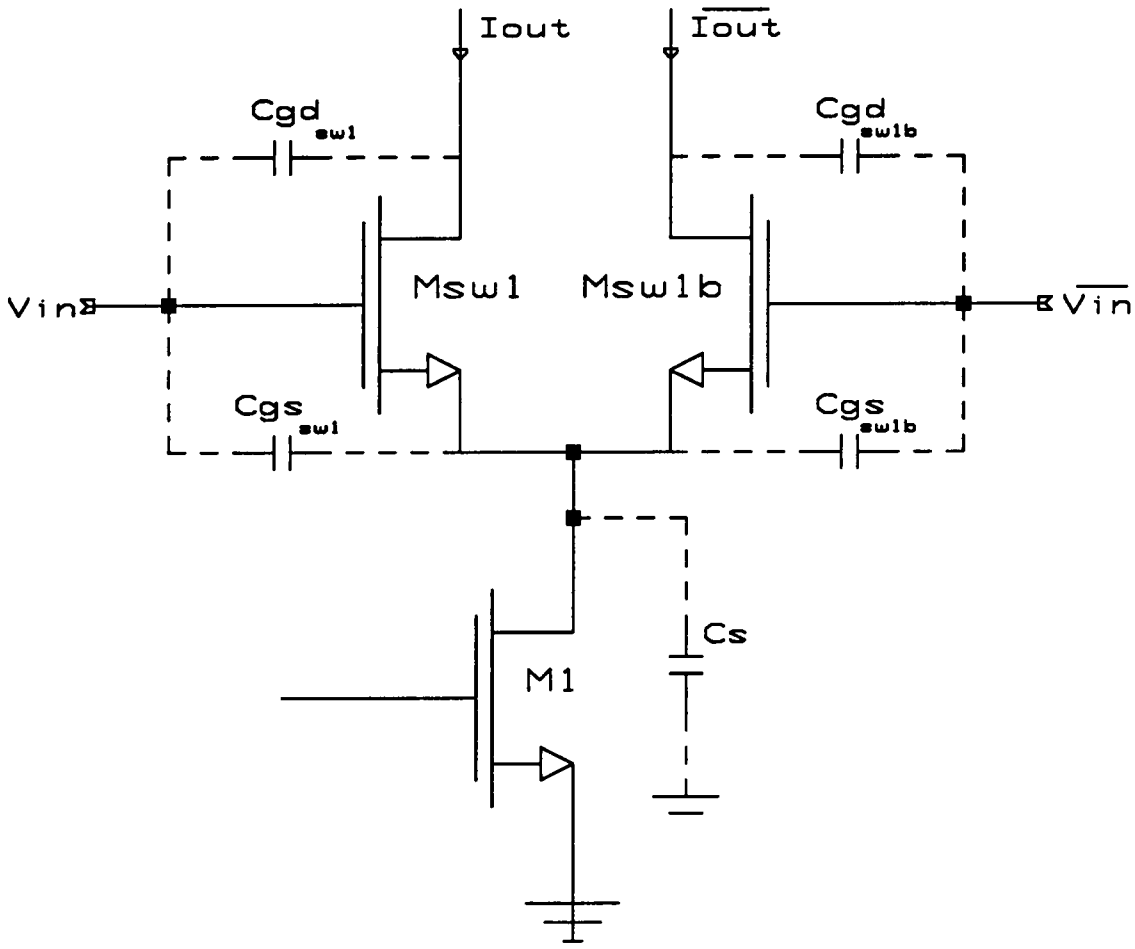

Figure 3.5: Critical parasitic capacitances of a unit cell

and the gate-to-channel capacitance. The total gate capacitance in the linear region can be expressed as

$$C_g \simeq C_{ox} W_{eff} (2LD + L_{eff}) \tag{3.32}$$

where the channel area $A_{ch} = W_{eff} L_{eff}$.

In the saturation region where $V_{ds} \geq (V_{gs} - V_t)$, the channel is heavily inverted and the drain region is pinched off. This caused C_{gd} due to gate-to-channel capacitance to be zero, and C_{gs} increases to approximately 2/3 of its channel capacitance in the case of the linear region [11]. Therefore the total gate capacitance can be approximated as

$$C_g \simeq 2C_{ox} W_{eff} (LD + 1/3 L_{eff}) \tag{3.33}$$

When the input of M_{sw1} rises and the input of M_{sw1b} falls, feedthrough current will be injected through the gate capacitance of M_{sw1} and is pulled out through the gate capacitance of M_{sw1b}. Since M_{sw1} is operating in either the linear or the saturation region at this point, its gate capacitance is not the same as the C_g of M_{sw1b}, which is in the cutoff region. As the result of this, the injected and the pulled currents are not equal. Due to the inequality of the capacitances, the voltage at drain of the current source M_1 moves up and down. At the same time M_1 is generating a constant current that should be equal to the output current, I_{out}. But due to feedthrough current through the gate capacitances of M_{sw1} and M_{sw1b}, there will be under shoots and over shoots in the currents of I_{out} and $\overline{I_{out}}$ by the total amount of the feedthrough currents.

Since C_g is not constant over different voltage ranges and is a function of the

transistor sizes of the switch, the larger the W of the switch is, the larger the C_g will be. Larger capacitances generate larger feedthrough currents that degrade the transient accuracy of the DAC.

3.1.6 Unit Cell with a Cascode Current Source

Another possible topology for the unit cell design is given in Figure 3.6. In this unit cell, the simple current mirror is replaced by the cascode current mirror. The transistors in the cascode current mirror operate in a similar fashion to those in the simple current mirror. The diode connected transistors M_{ref_1} and M_{ref_2} operate in the saturation region since their gates are connected to their respective drains. Transistors M_1 and M_2 are connected in a current mirror configuration with the diode connected transistors. The node V_{ref_1} is shared by all the bottom row transistors in each of the cascode unit cells, and the node V_{ref_2} is shared by all the second row transistors in each of the cascode unit cells in the DAC. For proper operation, transistors M_1 and M_2 must be operating in the saturation region. For M_1 to be in the saturation region, V_{ds_1} should be greater than or equal to $(V_{ref_1} - V_{t_1})$. V_{ref_1} should be at least equal to $V_{t_{ref_1}}$, for M_{ref_1} to be ON. Similarly, for M_2 to be in saturation, V_{ds_2} should be greater than or equal to $(V_{ref_2} - V_{ds_1} - V_{t_2})$. Therefore, V_{ref_2} should be at least equal to $(V_{t_1} + V_{t_2})$, for M_{ref_1} to be ON. Assuming all threshold voltages are the same and ignoring body effect, V_{ref_2} must be at least $2V_t$ for M_2 to be in the saturation region. Hence, this unit cell requires a higher minimum voltage compared to the simple unit cell.

The advantage of using cascode current mirror is its higher output impedance.

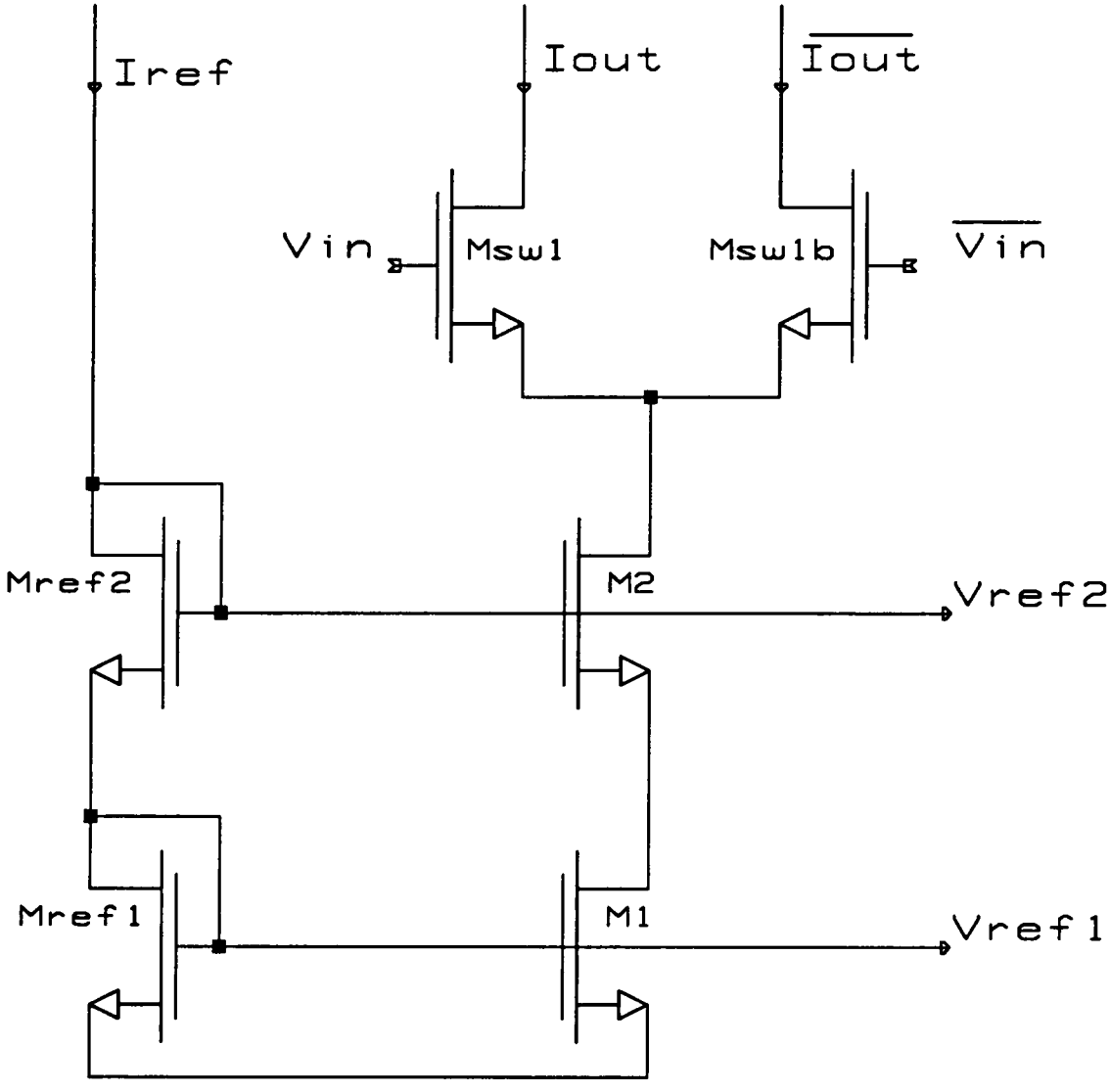

Figure 3.6: A unit cell of a cascode current source network

Figure 3.7 shows the simplified small-signal model of the cascode unit cell. Using this model, the output impedance of the cascode unit cell can be calculated as

$$\begin{aligned} r_{out} &= r_{ds_1} + r_{ds_2} + r_{ds_{sw1}} + g_{m_{sw1}}(1+\eta_{sw1})(r_{ds_1} + r_{ds_2}) \\ &\quad + g_{m_2} r_{ds_1} r_{ds_2}(1+\eta_{m2})[1 + g_{m_2} r_{ds_{sw1}}(1+\eta_{sw1})] \end{aligned} \tag{3.34}$$

where M_1 and M_2 are both pinched off. For M_{sw1} in the linear region, the r_{out} terms can be further simplified to

$$r_{ds_1} \simeq \frac{1}{I_{out}\lambda_1} \tag{3.35}$$

$$r_{ds_2} \simeq \frac{1}{I_{out}\lambda_2} \tag{3.36}$$

$$g_{m_2} \simeq \sqrt{2\beta_2 I_{out}} \tag{3.37}$$

$$r_{ds_{sw1}} \simeq \frac{1}{\beta_{sw1}(V_{gs_{sw1}} - V_{t_{sw1}} - V_{ds_{sw1}})} \tag{3.38}$$

$$g_{m_{sw1}} \simeq \beta_{sw1} V_{ds_{sw1}} \tag{3.39}$$

The values of $r_{ds_{sw1}}$ and $g_{m_{sw1}}$, for M_{sw1} in the saturation region are

$$r_{ds_{sw1}} \simeq \frac{1}{I_{out}\lambda_{sw1}} \tag{3.40}$$

$$g_{m_2} \simeq \sqrt{2\beta_{sw1} I_{out}} \tag{3.41}$$

Comparing the r_{out} of the simple unit cell in Equation 3.16 with the r_{out} of the cascode unit cell in Equation 3.34 clearly shows that the cascode current mirror offers higher output impedance than the simple current mirror. Therefore, the current of the cascode unit cell will be less sensitive to changes in the output voltage.

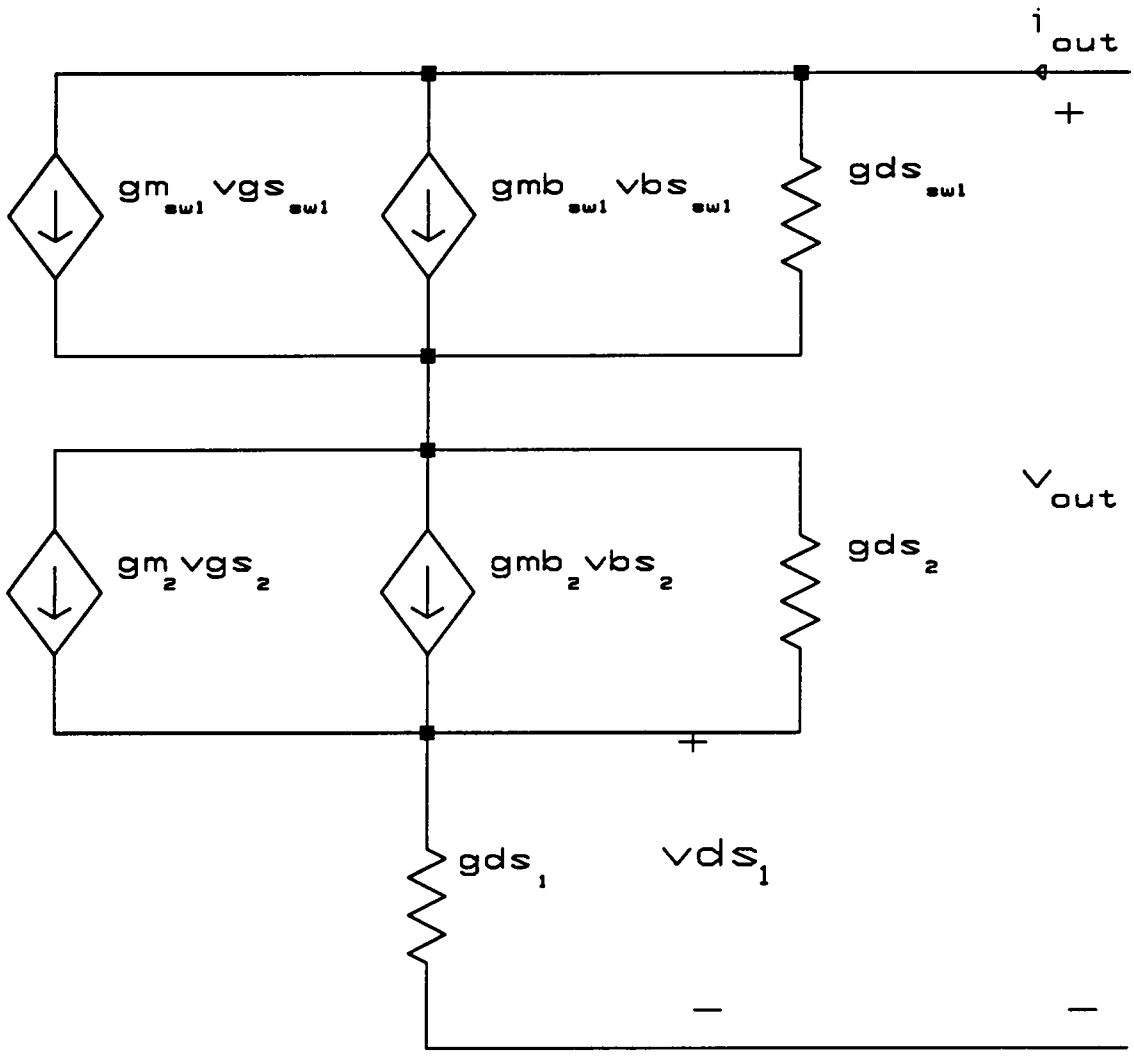

Figure 3.7: Output impedance model of a cascode unit cell

The price of the higher output impedance of the cascode cell is its higher minimum output voltage. Neglecting λ effect, $V_{out(min.)}$ for a simplified cascode unit cell in Figure 3.8 can be obtained as

$$V_{out(min.)} = (V_{in} - V_{t_{sw1}}) - \sqrt{(V_{in} - V_{t_{sw1}})^2 + 2(V_{t_{sw1}} - V_{in})(V_{ds_1} + V_{ds_2}) + (V_{ds_1} + V_{ds_2})^2 - \frac{2L_{sw1} I_{out}}{\mu_0 C_{ox} W_{sw1}}} \tag{3.42}$$

Since $I_{out} = I_1 = I_2$, $V_{ds_1} = V_{ds_1(sat.)} = (V_{gs_1} - V_{t_1})$, $V_{ds_2(sat.)} = (V_{gs_2} - V_{t_2})$, $(V_{gs_1} - V_{t_1}) = \sqrt{\frac{2I_1}{\beta_1}}$, $(V_{gs_2} - V_{t_2}) = \sqrt{\frac{2I_2}{\beta_2}}$, and neglecting the λ effect, $I_{ref} = I_{out}$. The new value of $V_{out(min.)}$ can be expressed as

$$V_{out(min.)} = (V_{in} - V_{t_{sw1}}) - \sqrt{(V_{in} - V_{t_{sw1}}) \left[(V_{in} - V_{t_{sw1}}) - 2\sqrt{\frac{2I_{ref}}{\mu_0 C_{ox}} \left(\frac{L_1}{W_1} + \frac{L_2}{W_2}\right)}\right] + \frac{2I_{ref}}{\mu_0 C_{ox}} \left[\left(\sqrt{\frac{L_1}{W_1}} + \sqrt{\frac{L_2}{W_2}}\right)^2 - \frac{L_{sw1}}{W_{sw1}}\right]} \tag{3.43}$$

$V_{out(min.)}$ can be reduced by increasing the W/L values and adjusting the gate-to-source voltage to get the same output current. Similar results can be calculated for switch M_{sw1b}, when it is ON.

Due to body effect, $V_{t_{sw1}}$ of the switch in the cascode cell will be larger than the threshold voltage of the switch in the simple cell, since the source voltage would be at a higher potential in the cascode mirror versus the simple mirror. The threshold voltages of M_{ref_2} and M_2 are also higher than the threshold voltages of M_{ref_1} and M_1, due to the body effect. Therefore, the transistors in the cascode unit cell require higher minimum operating voltage.

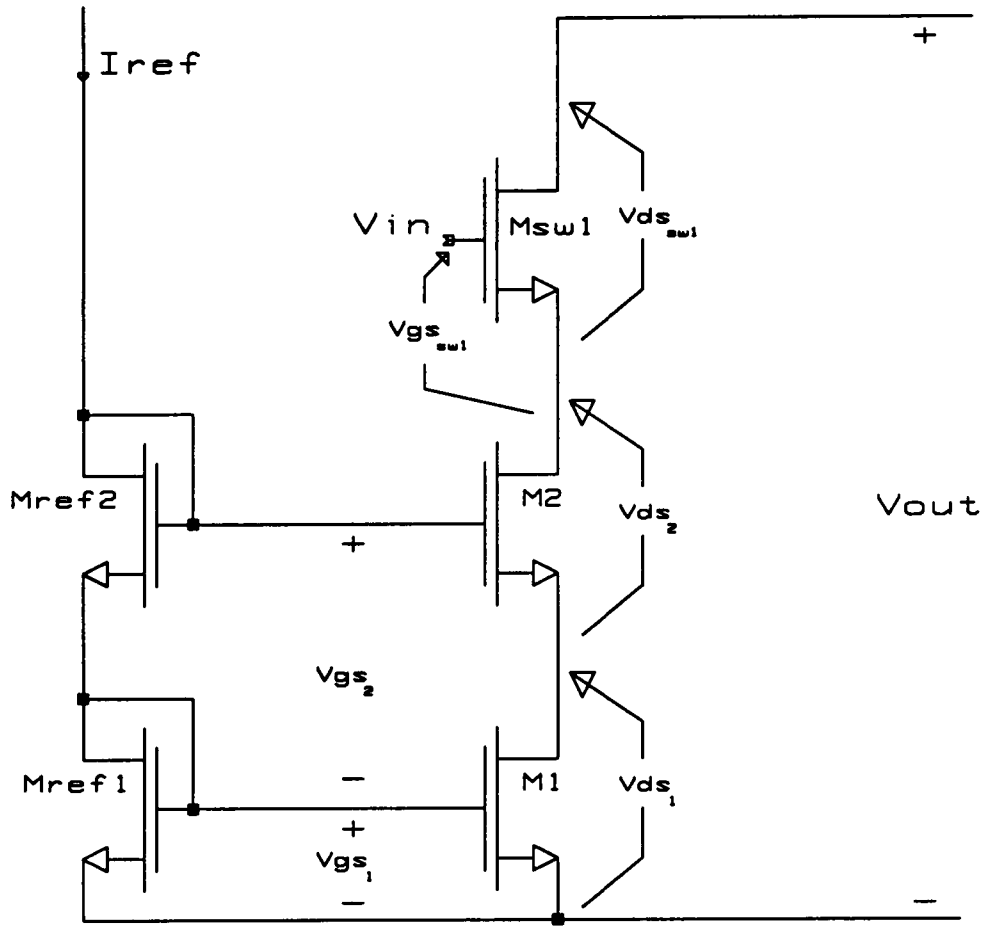

Figure 3.8: Simplified cascode unit cell for minimum $V_{out(min.)}$ calculation

Comparing Equations 3.27 and 3.43, for equal $V_{out(min.)}$, the W/L of the transistors in the cascode unit cell must be larger than in the simple unit cell. Increases in W/L translates to a larger area and a larger current. Maintaining the same area in the two unit cells requires the transistor sizes in the cascode mirror to decrease. Reducing the transistor sizes in the cascode unit cell increases $V_{out(min.)}$ and reduces the current capability of the cell. Reducing the transistor sizes also has an adverse effect on matching. Thus, in order to design a cascode unit cell with the same output current and minimum output voltage as an equivalent simple unit cell requires that the cascode version occupy a larger area.

With a smaller area, an adequate output impedance, and lower minimum output voltage, a DAC based on a simple unit cell can be designed. Therefore a simple current source topology was used for the design of the DAC.

3.2 Nonideal Effects in Current Mirrors

Mismatches represent major limitations to the accuracy of analog circuits. Current mismatch can degrade linearity and monotonicity which are important characteristics of a DAC. Mismatch that can be observed between the parameters of a group of equally designed MOS transistors is the result of several random variations in the process steps which occur during every fabrication phase of the devices. The absolute value of parameters can also be different from process to process, from wafer to wafer, or as the result of unwanted offsets caused by electrical or lithographic differences [16]. The majority of these errors are process dependent,

and there is not much that a designer can do in order to reduce or avoid the resulting problems without having access to the process. Transistor width and length are typically the only parameters available to be specified by the circuit designer. Another source of error is systematic error which affects adjacent elements with identical geometries [17]. These mismatches can be minimized by following a set of basic rules and by making maximum advantage of all the available components in a process. Process errors are random and cannot be corrected by improved matching techniques. They are the limitations of the achievable accuracy.

An examination of Equation 3.6 shows that there are three effects that can cause current mismatch in current source transistors. These are: (1) channel-length modulation mismatch, (2) threshold offset between transistors, and (3) imperfect geometrical matching. Each of these effects will now be described in detail.

The channel-length modulation parameter, λ, varies inversely with the length of the device, the drain-to-source voltage, and $\sqrt{N_{sub}}$, when ϵ_{si}, q, and $V_{ds}(sat.)$ are considered constants. Equation 3.3 shows that with increase in V_{ds}, substrate doping, and L_{eff}, λ decreases. As the result the two adjacent current source transistors can have different values of λ.

The assumption that the substrate is uniformly doped does not necessarily hold for small-geometry devices [15]. The nonuniformity of the substrate dopant is a process issue, but by using larger transistor sizes the effect can be minimized.

Threshold voltage, V_t as described in Equation 3.2 is equal to V_{t_0} when $V_{sb} = 0$. Since V_{bs} of all the transistors of the current sources are equal to zero, they will not have threshold mismatches due to body effect, and the threshold voltage will

be equal to the zero-bias threshold voltage. V_{t_0} can be expressed as [11]

$$V_{t_0} = V_{fb} + 2|\phi_f| + \frac{\sqrt{4q\epsilon_{si}N_{sub}|\phi_f|}}{C_{ox}} \tag{3.44}$$

Parameters of V_{t_0} are defined as

$V_{fb} = \phi_{gb} - \frac{Q_{ss}}{C_{ox}}$ = flatband voltage $(volt)$

$\phi_{gb} = \phi_{f(gate)} - \phi_{f(body)}$

$Q_{ss} = N_{ss}q$=oxide charge $(coulomb - cm^{-2})$

N_{ss} = surface state density (cm^{-2})

The mismatch in zero-bias threshold voltage is accounted for by variations in temperature, different charge quantities, and in the gate oxide. The gate oxide capacitance is quite uniform and has little influence on the threshold voltage mismatch. However, the non-uniform distribution of the dopant atoms in the bulk is a major contributor to this mismatch [15]. Since the nonuniformity of N_{sub} is an issue with small-geometry transistor sizes, the effect can be minimized by using non-minimum transistor sizes. As long as the power dissipated on the chip is very low, temperature will not have a major effect in mismatches of threshold voltage [15].

There are differences in the drawn W and L, due to mask, photolithographic, etch, and out-diffusion variations, even for two similar adjacent transistors [11]. The gate area of a MOS transistor is determined by several different masks. The poly mask determines the channel length, and the diffusion mask determines the channel width. Hence, length and width can be treated as independent random variables. Current matching can be improved by increasing the device size, and for transistors of identical size with W and L greater than $10\mu m$, the errors due

to geometrical mismatch will generally be insignificant compared to other sources of mismatch [11].

It is also possible that the mobility μ_0 of the current mirror is mismatched due to random impurities. The mobility of holes is different from the mobility of electrons and is also a function of impurity concentration. Mobility discussed here is the surface mobility, or the mobility of a carrier constrained to travel along a semiconductor surface. Electron mobility is approximately two times the hole mobility and decreases with increasing doping concentration because of increased collision with charge impurities. For n-channel devices, the variation in mobility has less effect on the mismatch of current mirrors; the corresponding quantity for p-channel transistors could be larger.

The drain current matching not only depends on the device dimensions but also on the operating points. Significant ratio error can exist when the current source transistors do not have the same drain-to-source voltages due to the mismatch in the ON resistance of the switch in the linear mode. Assuming that the V_{ds} voltages are not equal, but all other aspects of the transistors of a simple current mirror have the same values including λ, the ratio of the currents of two current sources can be simplified to

$$\frac{I_1}{I_2} = \frac{1 + \lambda V_{ds_1}}{1 + \lambda V_{ds_2}} \tag{3.45}$$

In this case, the differences in the V_{ds} values of the two transistors can cause differences in the ideal current mirroring. But for a given difference in V_{ds}, the current mirror matching can be improved as λ becomes smaller. This can be accomplished

by using larger L_{eff} values. The other benefit of larger L values is larger output impedance, since short-channel devices decrease the output impedance, and consequently, the linearity is degraded.

Equation 3.1 shows that better performance of the current mirrors can be achieved by using larger V_{gs} voltages because there will be less effect due to threshold offset. In order to achieve a higher V_{gs}, higher currents or larger W/L are required. The larger the V_{gs}, the less effect the $\Delta V_t = V_{t_2} - V_{t_1}$ will have on the output current. The differences in V_{gs} of the current sources would also can cause mismatches in the currents. In a current mirror, when the V_t and all other aspects of the transistors are identical except V_{gs}, the current ratio of two current sources can be simplified to

$$\frac{I_1}{I_2} = \frac{\left(V_{gs_1} - V_t\right)^2}{\left(V_{gs_2} - V_t\right)^2} \tag{3.46}$$

But since the gate of each of the current sources will be connected to the same common node, the V_{gs} differences would only be due to poor layout and high resistance in the connecting metals which would cause voltage drops across the metals.

3.2.1 Mismatch Calculation

A quantitative analysis of variations in λ, V_t, and transconductance parameter (β) will now be given. Assume that the current through the first unit cell is I_1, and the current through an adjacent unit cell is I_2. From Equation 3.1 the current

through each of the unit cells can be expressed as

$$I_1 = \frac{\mu_{0_1} C_{ox_1} W_1}{2L_1}(V_{gs_1} - V_{t_1})^2(1 + \lambda_1 V_{ds_1}) \tag{3.47}$$

$$I_2 = \frac{\mu_{0_2} C_{ox_2} W_2}{2L_2}(V_{gs_2} - V_{t_2})^2(1 + \lambda_2 V_{ds_2}) \tag{3.48}$$

For the purposes of limiting the scope of this mismatch analysis, V_{ds} and V_{gs} voltages are assumed to be constant. The differences in each of the parameters can be defined as

$\Delta\beta = (\beta_2 - \beta_1)$, and $\beta = 0.5(\beta_2 + \beta_1)$

$\Delta V_t = (V_{t_2} - V_{t_1})$, and $V_t = 0.5(V_{t_2} + V_{t_1})$

$\Delta\lambda = (\lambda_2 - \lambda_1)$, and $\lambda = 0.5(\lambda_2 + \lambda_1)$

Therefore, $\beta_1 = (\beta + 0.5\Delta\beta)$, and $\beta_2 = (\beta - 0.5\Delta\beta)$. $V_{t_1} = (V_t - 0.5\Delta V_t)$, and $V_{t_2} = (V_t + 0.5\Delta V_t)$. $\lambda_1 = (\lambda + 0.5\Delta\lambda)$, and $\lambda_2 = (\lambda - 0.5\Delta\lambda)$. The ratio of I_1 to I_2 from Equations 3.47 and 3.48 can be expressed as

$$\frac{I_1}{I_2} = \frac{(\beta + 0.5\Delta\beta)(V_{gs} - V_t + 0.5\Delta V_t)^2[1 + V_{ds}(\lambda + 0.5\Delta\lambda)]}{(\beta - 0.5\Delta\beta)(V_{gs} - V_t - 0.5\Delta V_t)^2[1 + V_{ds}(\lambda - 0.5\Delta\lambda)]} \tag{3.49}$$

Equation 3.49 can be further approximated to

$$\frac{I_1}{I_2} \simeq 1 + \frac{\Delta\beta}{\beta} + \frac{2\Delta V_t}{(V_{gs} - V_t)} + \frac{\Delta\lambda V_{ds}}{(1 + \lambda V_{ds})} \tag{3.50}$$

The approximation in Equation 3.50 is valid only when $\frac{0.5\Delta V_t}{(V_{gs} - V_t)} \ll 1$, $\frac{0.5\Delta\beta}{\beta} \ll 1$, and $\frac{(0.5V_{ds}\Delta\lambda - 1)}{V_{ds}\lambda} \ll 1$. When $(V_{gs} - V_t) \simeq 0.5\Delta V_t$, the Equation 3.49 can be approximated by

$$\frac{I_1}{I_2} \simeq 1 + \frac{\Delta\beta}{\beta} + \frac{\Delta\lambda V_{ds}}{(1 + \lambda V_{ds})} \tag{3.51}$$

In order to define $\Delta\lambda$ in terms of ΔL, from Equation 3.3 the different parameters are defined as $\Delta L = (L_1 - L_2)$, $L = 0.5(L_1 + L_2)$, and $\lambda = \frac{D}{L}$ where

$$D = \frac{1}{V_{ds}}\left[\frac{2\epsilon_{si}}{qN_{sub}}\right]^{1/2}\left\{\frac{V_{ds} - V_{ds}(sat.)}{4} + \left[1 + \left(\frac{V_{ds} - V_{ds}(sat.)}{4}\right)^2\right]^{1/2}\right\} \tag{3.52}$$

Thus, $L_1 = (L + 0.5\Delta L)$, and $L_2 = (L - 0.5\Delta L)$. Therefore, the ratio of $\Delta\lambda$ in terms of ΔL can be expressed as

$$\frac{\Delta\lambda}{\Delta L} = \frac{\partial\lambda}{\partial L} = \frac{D}{L^2} \tag{3.53}$$

Therefore, $\Delta\lambda$ from Equation 3.53 is given by

$$\Delta\lambda = \frac{D\Delta L}{L^2} \tag{3.54}$$

And since $\lambda = \frac{D}{L}$, $\Delta\lambda$ can be defined in terms of ΔL from Equation 3.54 as

$$\Delta\lambda = \frac{\lambda\Delta L}{L} \tag{3.55}$$

For calculating $\Delta I/I$, each of the parameters are defined as $\Delta I = I_2 - I_1$, $I = 0.5(I_2 + I_1)$, $I_1 = (I + 0.5\Delta I)$, $I_2 = (I - 0.5\Delta I)$, and

$$A = \frac{\Delta\beta}{\beta} + \frac{2\Delta V_t}{(V_{gs} - V_t)} + \frac{\Delta\lambda V_{ds}}{(1 + \lambda V_{ds})} \tag{3.56}$$

Therefore, the ratio of $\Delta I/I$ by substituting A in Equation 3.50 can be expressed as

$$\frac{\Delta I}{I} = \frac{2A}{(2 + A)} \tag{3.57}$$

According to [18], the threshold mismatch ΔV_t may have a mean standard deviation ranging from 1 - 20 mV, and $\Delta\beta/\beta$ mismatch ranging from 0.5 - 5 percent.

The mismatch in length and width is in the range of 0.01 - 0.03 μm [15]. For the purposes of worst case calculations here, ΔV_t is assumed to be $3\sigma = \pm 0.06\ V$, $\Delta\beta/\beta = \pm 0.05$, and $\Delta L = \pm 0.03\ \mu m$.

3.2.2 Non-Linearity Predication Due to Mismatch

Differential non-linearity and integral non-linearity are two of the general errors generated by a DAC. Linearity error occurs due to random mismatch in the conversion elements. Hence, the circuit yield is a function of the matching accuracy of the unit cell current sources. This enables the non-linearity to be expressed in terms of fractions of LSB or as a percentage of the unit cell current. A DAC with a differential non-linearity of greater than $\pm$1LSB, will not be monotonic.

The worst case differential non-linearity for a six-bit DAC usually occurs when the output changes from halfway through the full scale, binary code 011111 to the next input word 100000. For this code transition, every unit cell in the DAC changes state.

Assuming that the full scale output current of a six-bit current network DAC can be defined as

$$I_{fs} = I_{LSB}\,(32D_6 + 16D_6D_4 + 4D_3 + 2D_2 + D_1) \tag{3.58}$$

where I_{fs} is the full scale current of the the binary code 111111, D_i =0 or 1, $i = (1, 2, ..., 6)$, D_1 is the LSB, D_6 is the MSB, and I_{LSB} is the LSB current, which is the current of a unit cell. Ideally, $(I_{100000} - I_{011111})$ is equal to I_{LSB}. However, due to current mismatches the current differences of the two consecutive inputs

will not be equal to I_{LSB}. To calculate the worst case differential non-linearity, the output currents of I_{011111} and I_{100000} will be defined as

$$I_{011111} = 32I_{LSB} - \frac{32\Delta I}{2} \tag{3.59}$$

$$I_{100000} = 31I_{LSB} + \frac{31\Delta I}{2} \tag{3.60}$$

Therefore, the difference of the two output currents, I_{diff} will be

$$I_{diff} = I_{LSB} + \frac{63\Delta I}{2} \tag{3.61}$$

where $I_{diff} = (I_{100000} - I_{011111})$. Assuming worst case, the current error, I_{err} expressed in terms of LSB current can be obtained from Equations 3.57 and 3.61 as

$$I_{err} = I_{LSB}\left(\frac{63A}{2+A}\right) \tag{3.62}$$

where $I_{err} = (I_{diff} - I_{LSB})$. However, since the mismatch in the unit cells is an uncorrelated random process, a better estimate for the worst case differential non-linearity can be improved by a factor of $\sqrt{63}$. Thus,

$$\frac{I_{err(max.)}}{I_{LSB}} = \frac{\sqrt{63}A}{2+A} \tag{3.63}$$

Maximum error occurs halfway through the full scale, and the error contributions of the individual bits tapers off towards the LSB. Therefore, the MSB current could be the most critical bit in the performance of a DAC, and it should have the highest accuracy.

Integral non-linearity of a DAC is generally defined as the difference between the actual output to the desired output normalized to the full-scale output of the

DAC. In this case the maximum error due to mismatch would be in the case of the end-point linearity and it would be the same as the maximum differential non-linearity. In the case of best-straight-line linearity, the error will be less. In a current output DAC the output impedance does not have an affect on the integral linearity performance. But if the output current is converted to voltage output with a use of a resistor, the output impedance would effect the integral linearity performance of the DAC. In this design it has been assumed that either the DAC is used as a current output DAC or it can be converted to a voltage output DAC by using a high gain opamp, in which case the integral non-linearity of the DAC would still be independent of the output impedance.

3.2.3 Techniques for Reducing Mismatch

According to [13, 17, 18], for a given process, matching of critical devices may be improved by enforcing the following set of rules that are not specific to CMOS but are applicable to all kinds of IC technologies.

1. Devices to be matched should have the same structure.

2. They should have the same temperature. Device parameters such as mobility and threshold voltage are temperature dependent.

3. They should have the same shape and same size. For example, matched transistors should have same width and same length, and not simply the same aspect ratios.

4. Common-centroid geometries should be used to cancel constant gradients of parameters [17]. This also avoids troubling voltage drops on busses. Linearity error caused by a voltage drop along the analog ground bus can also be reduced by symmetrical layout and by ground tabs. This may not be feasible in some designs, since it generates additional complexity to the layout and also may not be practical in certain processes due to limited numbers of metal layers available.

5. The same orientation on chip is necessary to eliminate asymmetries due to unisotropic steps in the process, or to the unisotropy of the silicon substrate itself. In particular, the source-to-drain flows of current in matched transistors should be strictly parallel. Also, the drains of the transistors should lay on the same side of each transistor with respect to the chip.

6. Devices to be matched should have the same surroundings in the layout.

7. Minimum transistor sizes should not be used. Using nonminimum size transistors is an obvious way of reducing the effect of edge fluctuations and to improve spatial averaging of fluctuating parameters.

There are concerns with large separation between matched devices that cause mismatches, and, as a result, use of minimum distance between matched devices is recommended to take advantage of the spatial correlation of fluctuating physical parameters. But according to [13], the spacing between transistors can be ignored for transistor areas less than 100 μm^2.

Matching of currents in current mirrors can also be improved by careful layout techniques such as the use of guard rings.

3.3 Design Detail of a Six-Bit Current Steering DAC

Based on the understanding of the matching behavior of MOS devices and systematic design methodology, a six-bit DAC has been designed. Figure 3.9 shows a detailed circuit diagram of the six-bit non-weighted n-channel current steering DAC.

For this topology, the concept of unit cell was used in designing the DAC. The least significant bit (LSB) has one unit current source, the next significant bit has two unit current sources connected in parallel, and so on. The reference current I_{ref} is applied externally through a diode-connected transistor M_{ref}. The voltage developed across it is applied to the gate and source of the current source transistors which provide the currents. In each successive current source idealy, the size and current doubles when moving from LSB to MSB. For better matching and ease of layout and optimal density, 63 identical unit cells with non-minimum, non-weighted transistors were used.

3.3.1 Effects on Sizing

Current Sources

When designing the transistor sizes of the current source part of the unit cell, λ effect, transistor mismatches, and optimal minimum area were considered.

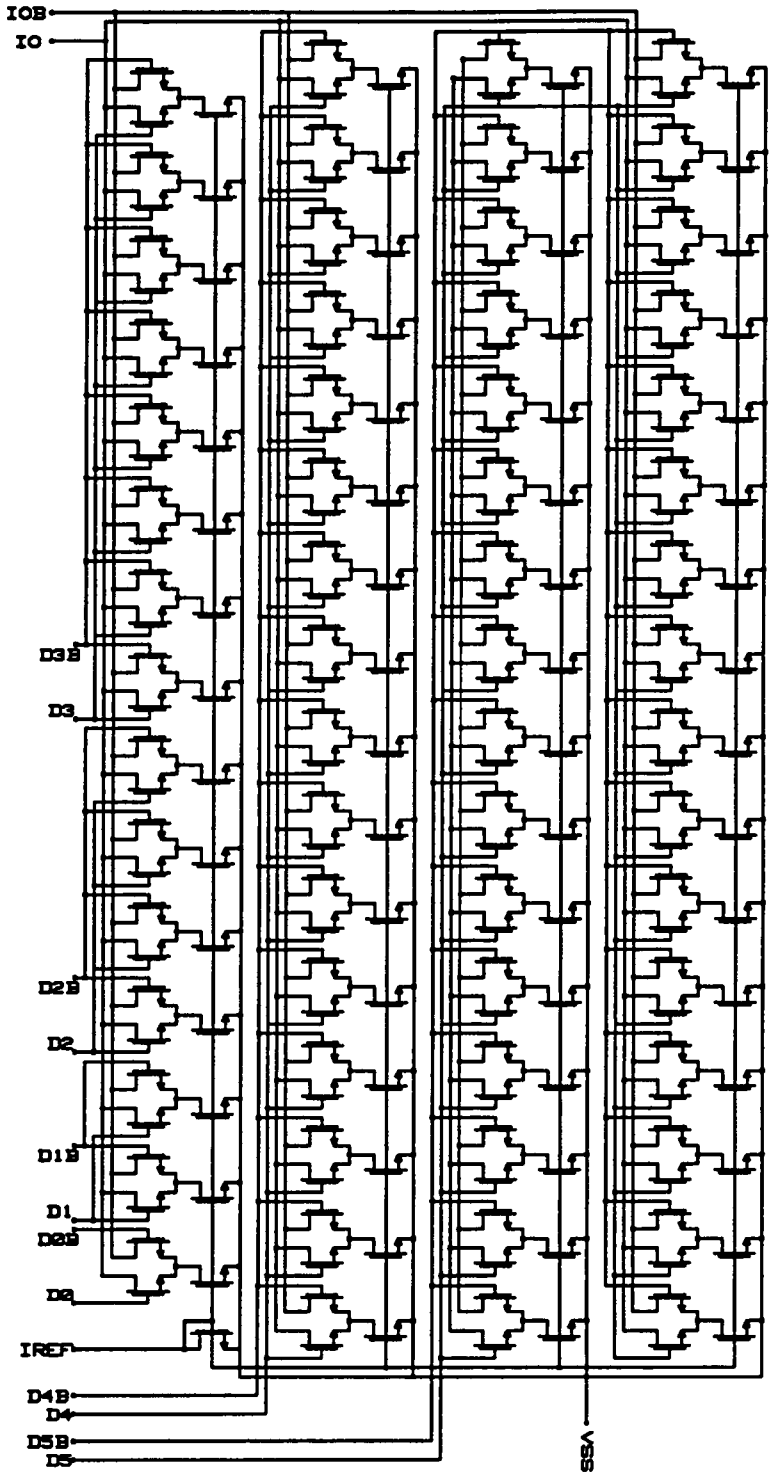

Figure 3.9: Six-bit binary-weighted current mirror

By using different SPICE models available from 2 μm MOSIS's process, λ effect versus the transistor length was simulated. The range of the values of λ for these models are from 0.022 - 0.063 $volt^{-1}$. It is quite obvious, both from theoretical calculations and from simulated results, that the transistors with smaller L values are more sensitive to λ effect. The curves of simulated λ versus transistor lengths for various models are given in Figure 3.10. Figure 3.11 shows the λ variation versus different values of L using the extracted DAC's SPICE model N02T. An examination of Figures 3.10 and 3.11 show that the knee of the curve occurs around an L of 10 μm. For L values less than 10 μm, λ increases exponentially. Therefore, the smallest reasonable L value for best channel modulation effect was chosen to be 10 μm.

According to [11], transistors with W and L values of 10 μm and larger will have the least amount of mismatch due to lithographic differences. From the previous mismatch discussions the worst case ΔW and ΔL were estimated to be 0.03 μm. Hence, the worst case W/L mismatch will be $(W+\Delta W)/(L-\Delta L)$. In this case by using transistors of $W = 10\mu m$ and $L = 10\mu m$, the transistor W/L ratio difference due to mismatch will only be 0.602%. Therefore, for least λ effect, better mismatch, and minimum area the unit current source, and the reference diode of the DAC are made up of a 10 μm wide and 10 μm long n-channel transistors.

Switches

The design considerations used in sizing the differential pair switches of the unit cell were 1) minimum ON resistance while operating in the linear region, 2)

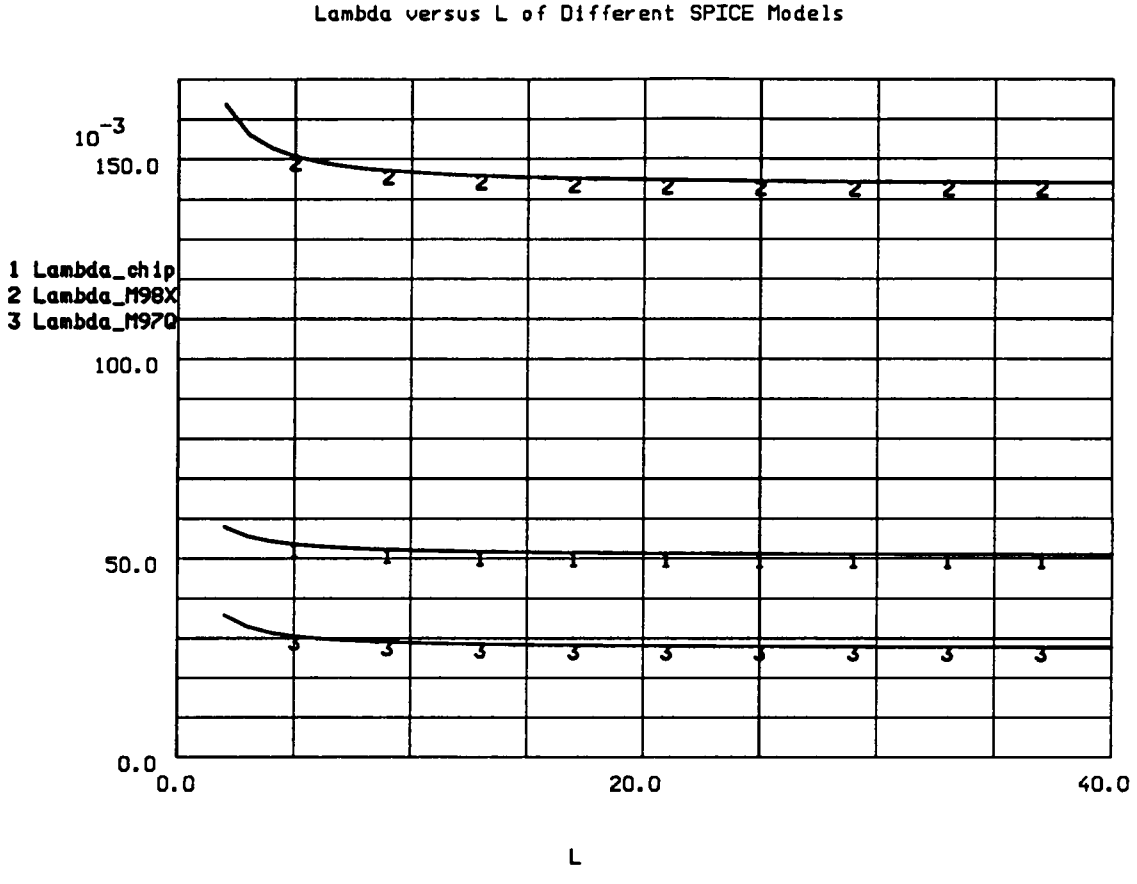

Figure 3.10: $\lambda(volt^{-1})$ variation versus transistor lengths (μm) for three different SPICE models

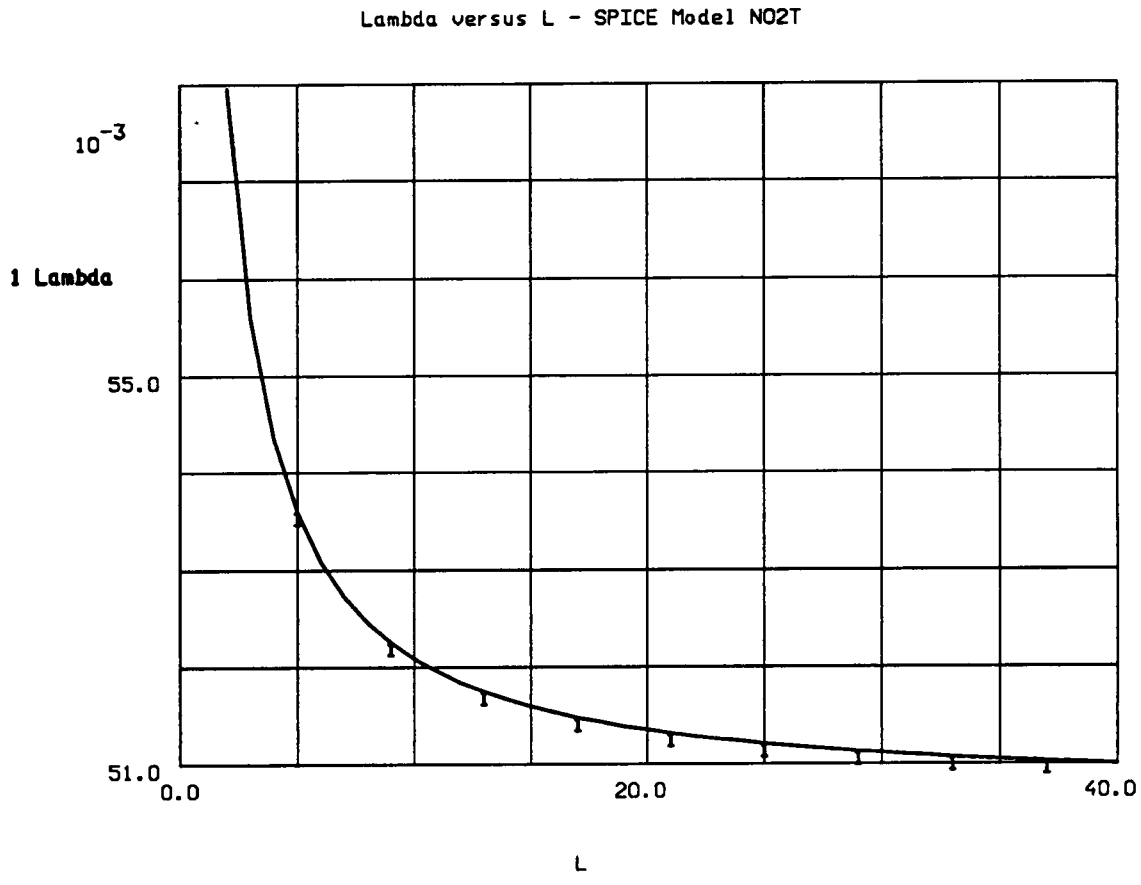

Figure 3.11: λ $(volt^{-1})$ variation versus transistor lengths $(\mu m)$of the chip - SPICE model N02T

optimal layout subject to constraints of area, and 3) minimum feedthrough current.

As shown in Equation 3.14, R_{ON} is inversely proportional to W/L of the switches. Therefore, for lowest output impedance, minimum L value and large W value should be used. But by using very large W, the gate capacitance increases which results in a larger feedthrough current. In order to realize a fast settling time, the stray capacitance at the output node should be small. The stray capacitance at the common source node should also be small to minimize the recovery time of the voltage at this node during the switching transition. This can be achieved by using small-sized transistors for the current source and the current switch. However, short-channel devices decrease the output impedance, and consequently, the linearity is degraded. For this reason the L value of the current source transistor was chosen as 10 μm instead of 2 μm. The switch part of the unit cell is made up of a 10 μm wide and 2 μm long n-channel differential pair transistors. This size transistors have better aspect ratio and minimum area, which is more optimal. Thus, by using this transistor size, there is a reasonable compromise between lower R_{ON}, better optimized layout, and small feedthrough current.

Substituting $\mu_0 = 608.8\ cm^2/V.s$, $C_{ox} = 8.48 \times 10^{-8}\ F/cm^2$, $W_{sw1} = 10\ \mu m$, $L_{sw1} = 2\ \mu m$, and $V_t = 0.779\ V$ in Equation 3.14 for output current of 1 μA and $V_{gs_{sw1}} = 1.526\ V$, the R_{ON} of the switch is equal to 5.18 $K\Omega$. The ON resistance of the switches at the maximum output current of 209.6 μA and $V_{gs_{sw1}} = 2.376\ V$, is equal to 2.42 $K\Omega$. Therefore, R_{ON} of the switches operating in the linear region is between 2.42 - 5.18 $K\Omega$.

3.3.2 Layout Detail of Six-Bit D/A Converter

Chip layout is critical to the performance of a high precision analog circuit. the considerations for planning the DAC network layout were aimed at minimizing 1) area, 2) mismatches, 3) voltage drop on the Vss ground bus, and 4) latchup possibilities. These considerations have been applied in the DAC network layout as shown in Figure 3.12.

The six-bit current DAC has been integrated in a 2 μm double-metal, single-poly CMOS technology. The DAC is made up of 63 unit cells and a reference diode. The repetitive nature of the circuitry has simplified the layout. The compactness of the layout of a unit cell is very important in minimizing the area of the network, since the same cell is replicated 63 times for the full network. For better density of the DAC, minimum spacing according to the layout rules was used in laying out the unit cell and similarly the network. By using 63 unit cells instead of weighted current sources, the current mismatch is minimized.

For better latchup performance the differential pair switch part of the DAC network is surrounded by n-well guard rings. The current sources are surrounded by another n-well ring, which is separated from the guard ring of the switches by a n+ diffusion guard ring. The n-well guard rings are connected to Vss supply and the n+ diffusion ring is connected to Vdd supply. To minimize voltage drop on the ground bus, a 20 μm wide metal1 bus was chosen, and also the bus was connected from both ends to Vss pads on the chip. A unit cell layout is shown in Figure 3.13.

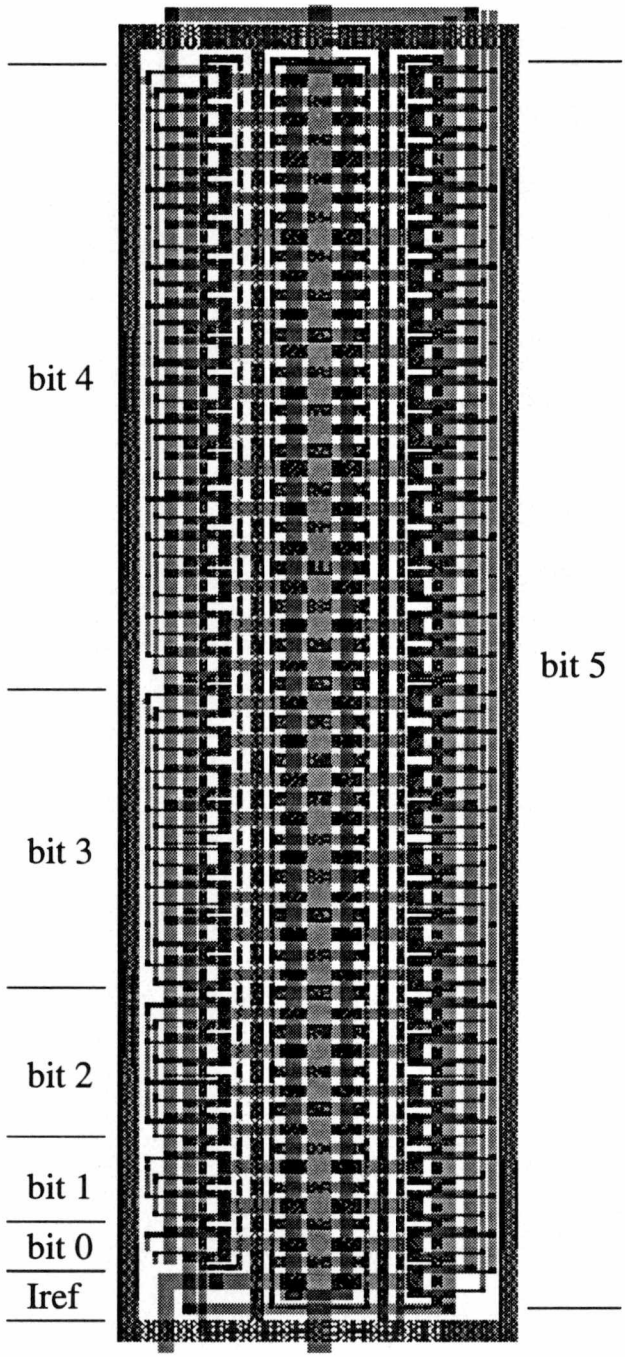

Figure 3.12: Layout of a six-bit current source DAC

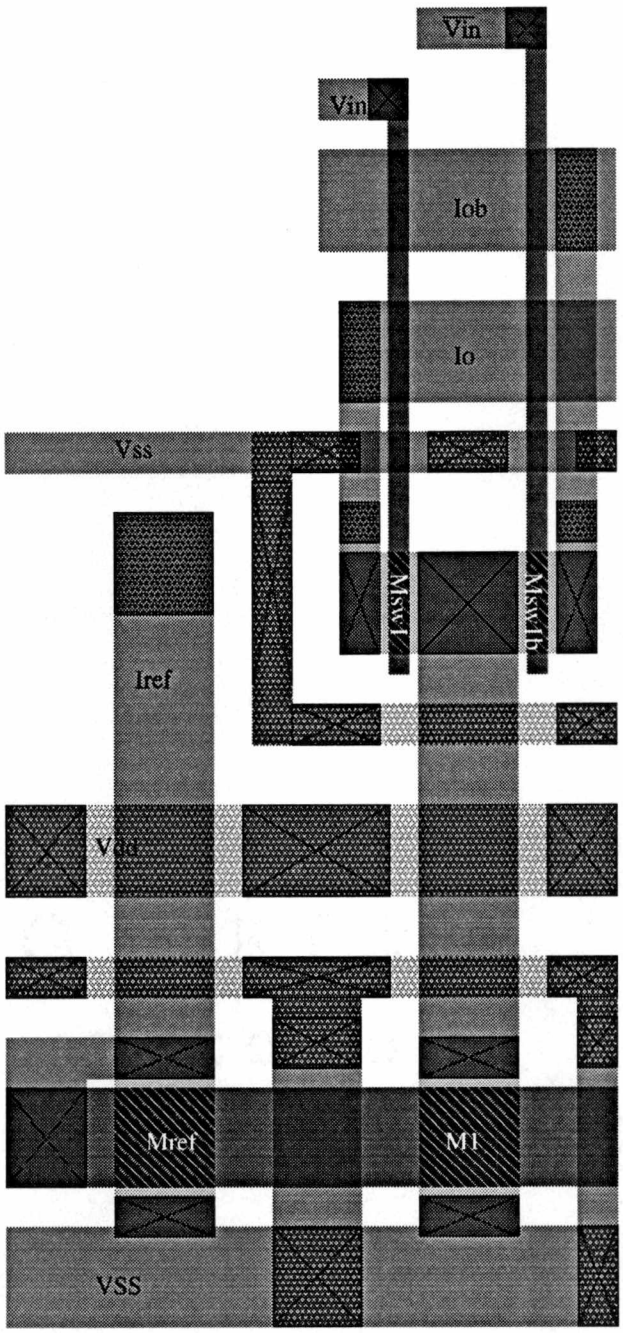

Figure 3.13: Layout of a unit cell current source

The size of the DAC is 298 $\mu m \times$ 1079 μm. In Figure 3.12, the left half of the DAC has the first five input bits of the network and the right half has the 32 unit cells for the MSB input. The LSB of the DAC consists of a single unit cell. The second, third, fourth, and fifth input bits have two, four, eight, and sixteen unit cells respectively.

In the layout of the switches, extra area was allowed for the connection to the input signals and connection to the other switches in the case of the higher input bits.

3.4 SPICE Simulations and Calculations of Expected Performance

3.4.1 Minimum Output Voltage ($V_{out(min.)}$)

The simulated $V_{out(min.)}$ curves using three different extracted SPICE models of 2 μm MOSIS process, for a unit cell are given in Figure 3.14. At the lower output currents, the $V_{out(min.)}$ of a unit cell using different models has similar performance, but at higher I_{out} values the different models behave differently. Curve number 1 is the simulation result using the extracted model of the DAC chip. These curves were generated by sweeping the reference current source I_{ref}, and the drain voltage of the switches, when one switch is ON and the other OFF. These curves represent the minimum output voltage required for the current source transistor to be in saturation. At voltages below $V_{out(min.)}$ for a given output current, the current source will be operating in the linear region and therefore would not be a good current source.

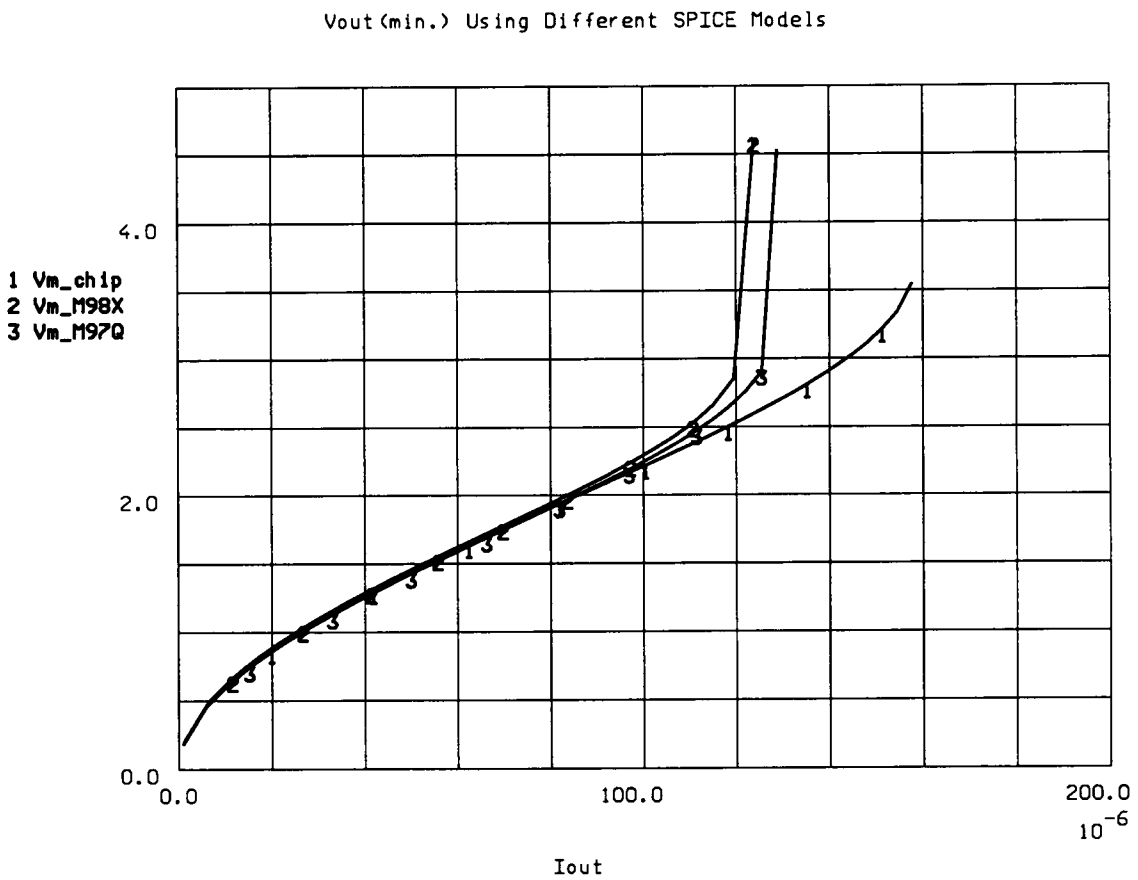

Figure 3.14: Simulated $V_{out(min.)}(volt)$ versus $I_{out}(\mu A)$ using three different extracted SPICE models of different chips in 2 μm MOSIS process.

The simulated and calculated $V_{out(min.)}$ of a unit cell using three different SPICE models are given in Figures 3.15, 3.16, and 3.17. The calculated curves represents Equation 3.27. The calculated curve in Figure 3.15 represents the $V_{out(min.)}$ when $V_{in} = 5\ V$, $V_{t_{sw1}} = 0.779\ V$, $(\mu_0 C_{ox}) = K_p = 5.167 \times 10^{-5}\ A/volt^2$, $W_1 = L_1 = W_{sw1} = 10\ \mu m$, and $L_{sw1} = 2\ \mu m$. The calculated data are equal to the simulated ones as long as the switch is operating in the linear region with low V_{ds_1}. The simulated data represent the switch operation both in the linear and the saturation regions, but in the calculated equation it was assumed that the switch will be operating in the linear region for the calculation of $V_{out(min.)}$. Because of this different representation of the switch operating point and also since λ effect was ignored in the calculated equation, the calculated curve deviates from the simulated one at higher output currents and V_{ds_1} voltages.

A sample SPICE netlist, along with the different SPICE models used for this simulation can be found in the Appendix A.

3.4.2 Maximum Output Current ($I_{out(max.)}$)

The simulated and calculated $I_{out(max.)}$ curves for the three different SPICE models are shown in Figures 3.18, 3.19, and 3.20. The simulated $I_{out(max.)}$ range is 131.7 - 209.6 μA. $I_{out(max.)}$ is defined as the maximum output current of a unit cell before the current source transistor M_1 goes out of the saturation region of operation. This is the current when $V_{ds_1} = V_{gs_1} - V_{t_1}$. $I_{out(max.)}$ was found by sweeping the input reference current source for different values of I_{ref}. From Equation 3.30, the calculated values of $I_{out(max.)}$ were found. Since $\mu_0 C_{ox} = K_p$,

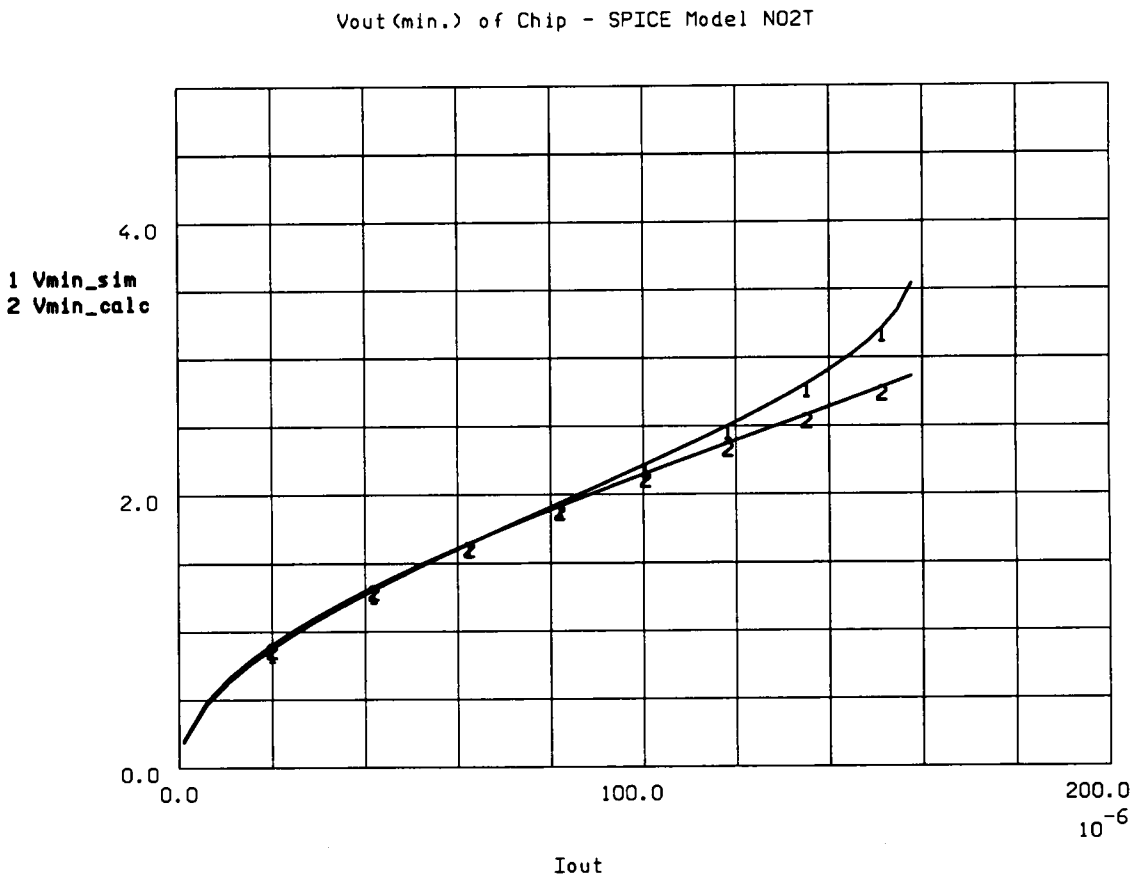

Figure 3.15: Simulated and calculated $V_{out(min.)}$ $(volt)$ of a unit cell versus I_{out} (μA) (SPICE model N02T).

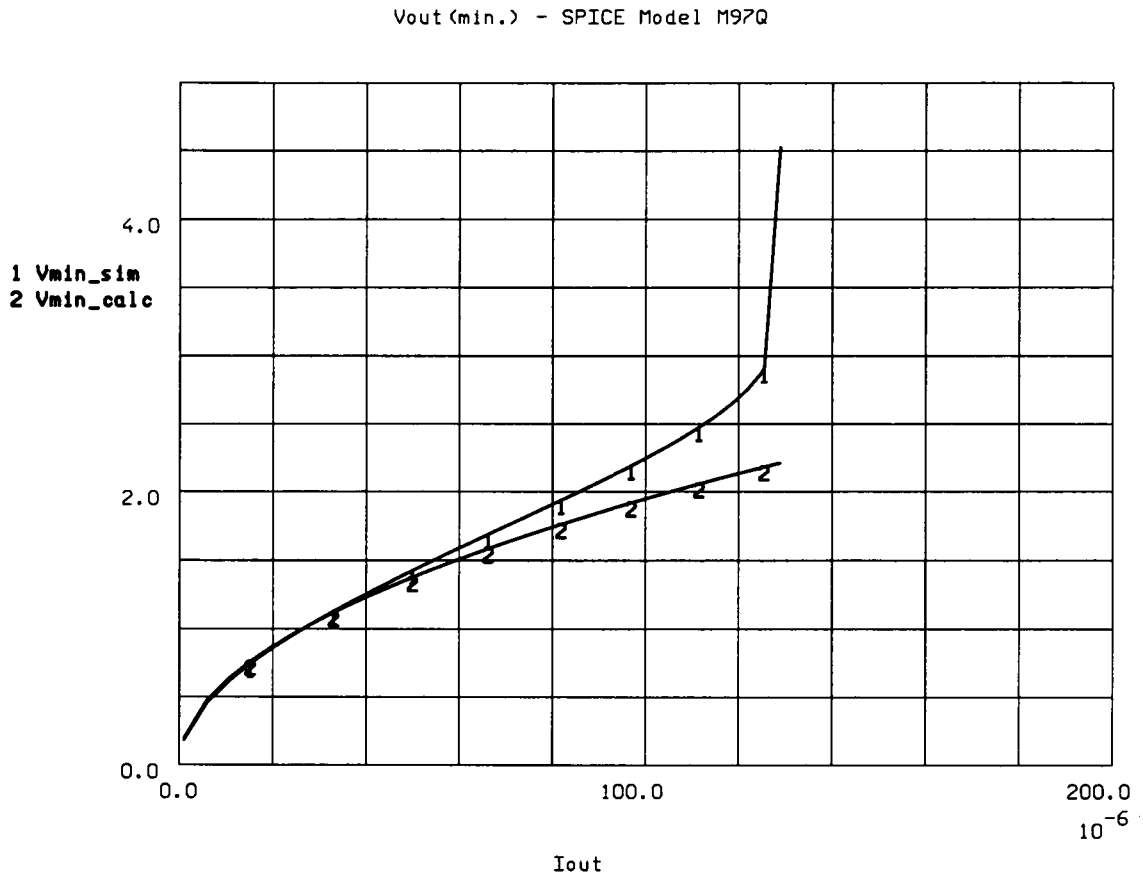

Figure 3.16: Simulated and calculated $V_{out(min.)}$ $(volt)$ of a unit cell versus I_{out} (μA) (SPICE model M97Q).

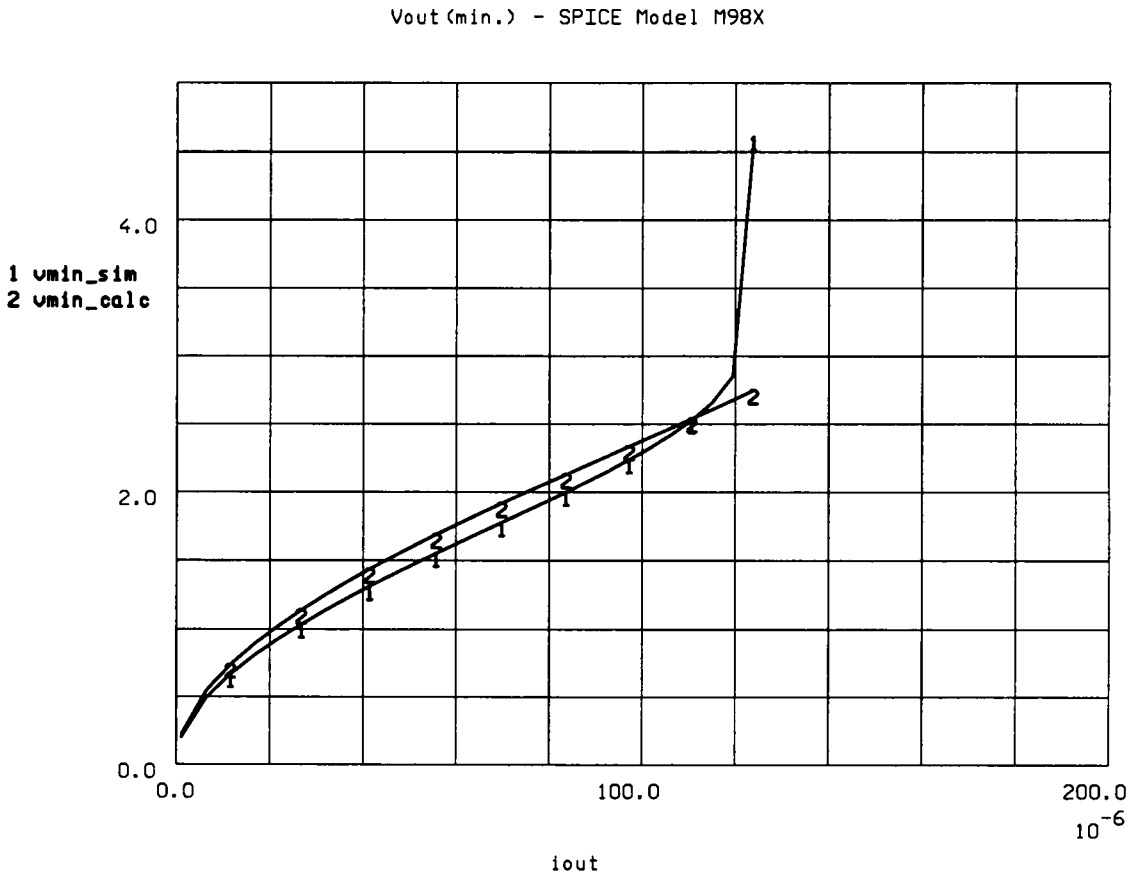

Figure 3.17: Simulated and calculated $V_{out(min.)}$ $(volt)$ of a unit cell versus I_{out} (μA) (SPICE model M98X).

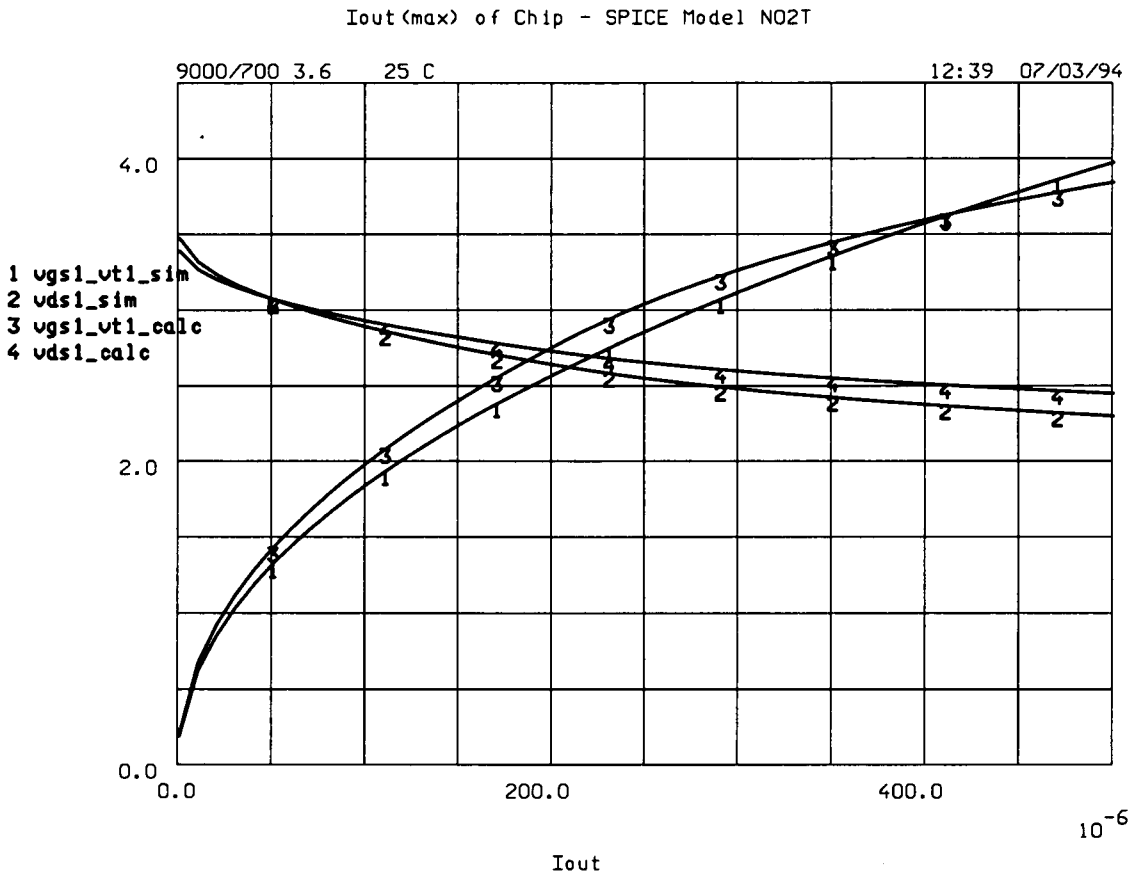

Figure 3.18: Simulated and calculated $I_{out(max.)}$ (μA) of a unit cell (SPICE model N02T).

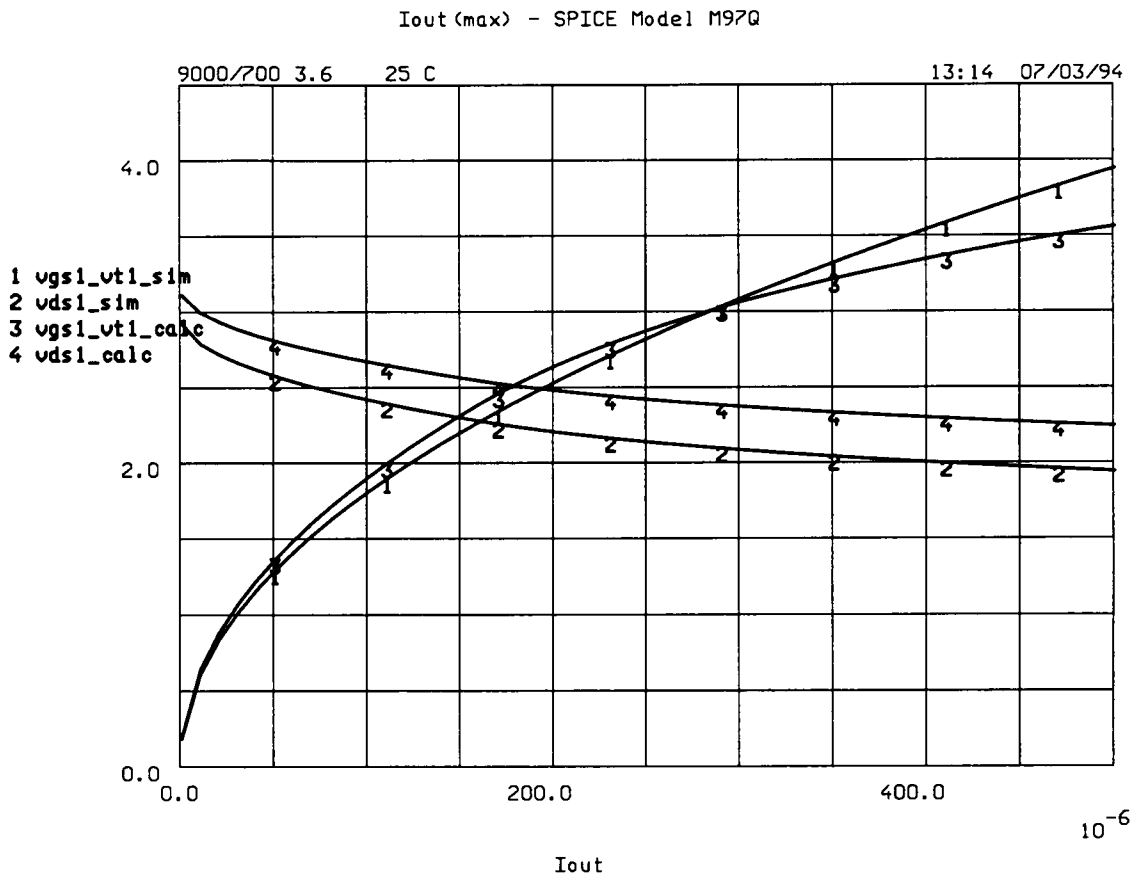

Figure 3.19: Simulated and calculated $I_{out(max.)}$ (μA) of a unit cell (SPICE model M97Q).

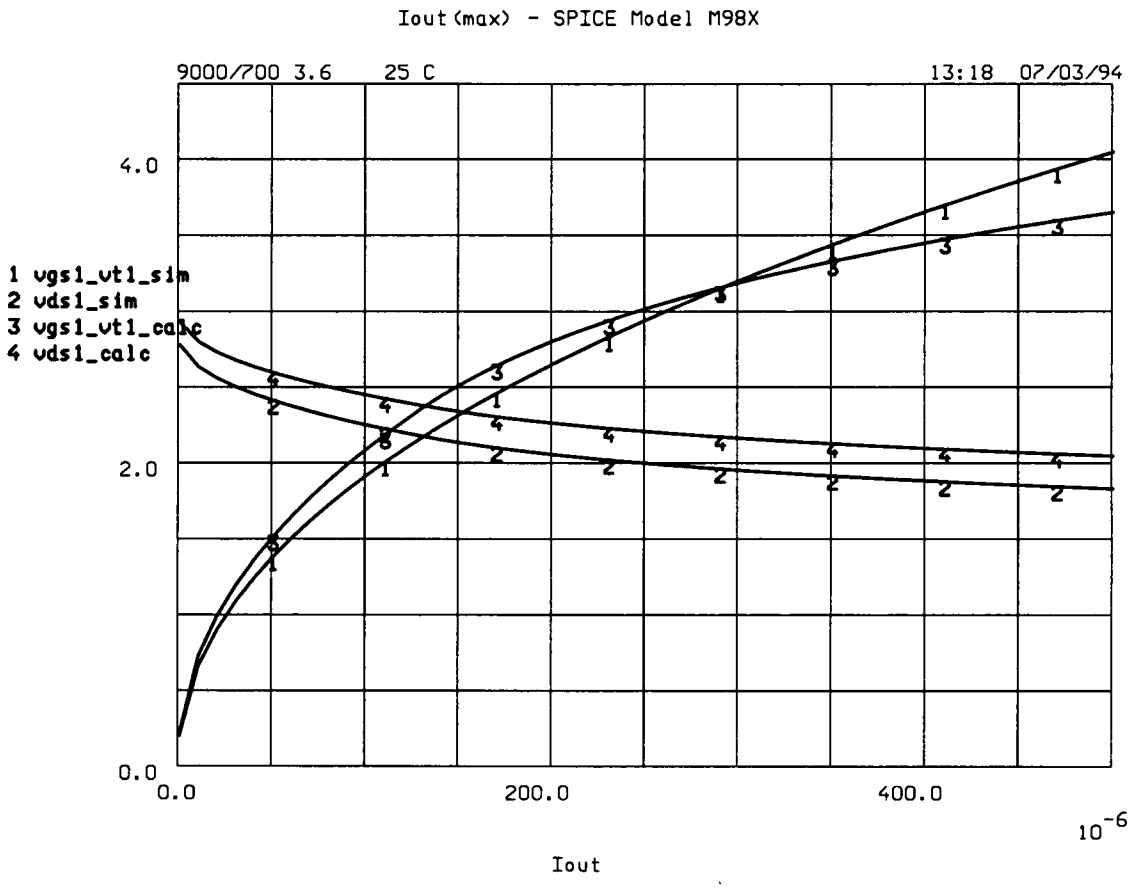

Figure 3.20: Simulated and calculated $I_{out(max.)}$ (μA) of a unit cell (SPICE model M98X).

V_t, and other process parameter of the three SPICE models are not the same, the simulated and the calculated $I_{out(max.)}$ values are not the same. By plotting the $(V_{gs} - V_t)$ with respect to I_{out} and V_{ds} with respect to I_{out} on the same plot, the cross point of the two curves is the $I_{out(max)}$ point of the respective input current. The simulated and calculated $I_{out(max.)}$ values of the different models are within $\pm 12\ \mu A$ of each other. This shows a good correspondence between the simulated and the calculated values.

A sample SPICE netlist used for this simulation can be found in the Appendix B.

3.4.3 Calculated Non-Linearity of the DAC

For calculating $\Delta\lambda$, $\lambda = 3.504 \times 10^{-2}(volt^{-1})$, $\Delta L = 0.03\ \mu m$, and $L = 10\ \mu m$ have been substituted in Equation 3.55. The calculated $\Delta\lambda$ is equal to 1.051×10^{-4} $volt^{-1}$. From Equation 3.56 for values of $\frac{0.5\Delta V_t}{(V_{gs}-V_t)} \ll 1$, $V_t = 0.779\ V$, $\Delta\beta/\beta = 0.05$, $\Delta V_t = 0.06\ V$, $V_{gs} = 3.403\ V$, and $V_{ds} = 2.624\ V$ at $I_{out(max.)}$, A is calculated to be 0.096. From Equation 3.63 worst case non-linearity is calculated to be $\pm 0.363 LSB$. For values of $(V_{gs} - V_t) \simeq 0.5\Delta V_t$ and $V_{ds} = 5\ V$, the differential non-linearity is equal to $\pm 0.05 LSB$.

In the case of this design, the worst case differential non-linearity of the six-bit DAC is calculated to be $\pm$0.363LSB, which is less than $\pm$1LSB. This will allow the DAC to be monotonic. This calculation was done for minimum V_{gs} and minimum V_{ds} which would contribute the maximum error due to mismatch. By operating the DAC at maximum V_{gs} and V_{ds}, the effect of mismatch on linearity can be

minimized. In this way, by using the mismatch data, the performance of a DAC is predicted.

3.4.4 Simulated AC Characteristics of the Switches

The simulated AC characteristics of the switches of a unit cell, at different input reference currents are shown in Figures 3.21, 3.22, 3.23, 3.24, 3.25, 3.26, 3.27, and 3.28. These curves were generated by switching the input voltages of the differential pair transistors, with a rise/fall of 2 ns and a pulse width of 20 ns, for different input reference currents.

Due to the inequality of the gate capacitance of the switches in different regions of operation, during input transition of the switches, V_{ds} of the current source will have a voltage spike due to feedthrough current. Figures 3.21, 3.23, 3.25, and 3.27 show the V_{ds} voltage change at different input reference currents. The maximum voltage change of 1.128 V and the minimum voltage change of 0.4 V occur at input currents of 209.6 μA and 1 μA respectively.

As the V_{ds} of the current source changes, there is also a change in the I_{out} and $\overline{I_{out}}$ currents. Figures 3.22, 3.24, 3.26, and 3.28 show the over-shoots and the under-shoots of the output currents as the result of feedthrough currents, for different values of I_{ref}. The maximum over-shoot of 75.3 μA and under-shoot of 7.964 μA were seen at I_{ref} = 209.6 μm, but these current spikes are less than 1LSB. In the case of I_{ref} = 1 and 28 μm the voltage spikes smaller but greater than 1LSB current.

A sample SPICE netlist used for this simulation can be found in the

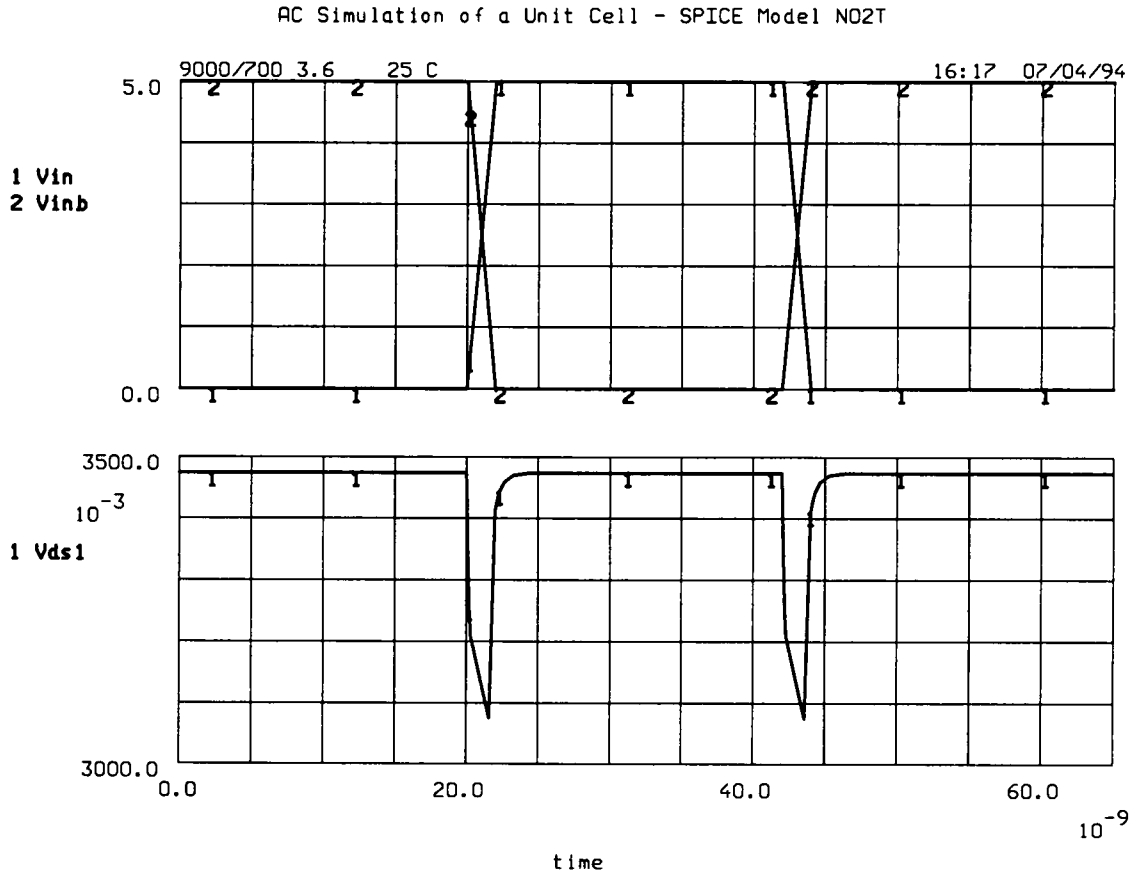

Figure 3.21: Effect of feedthrough current on the drain voltage of the current source transistor M_1 of a unit cell at $I_{ref} = 1\ \mu A$ (SPICE model N02T).

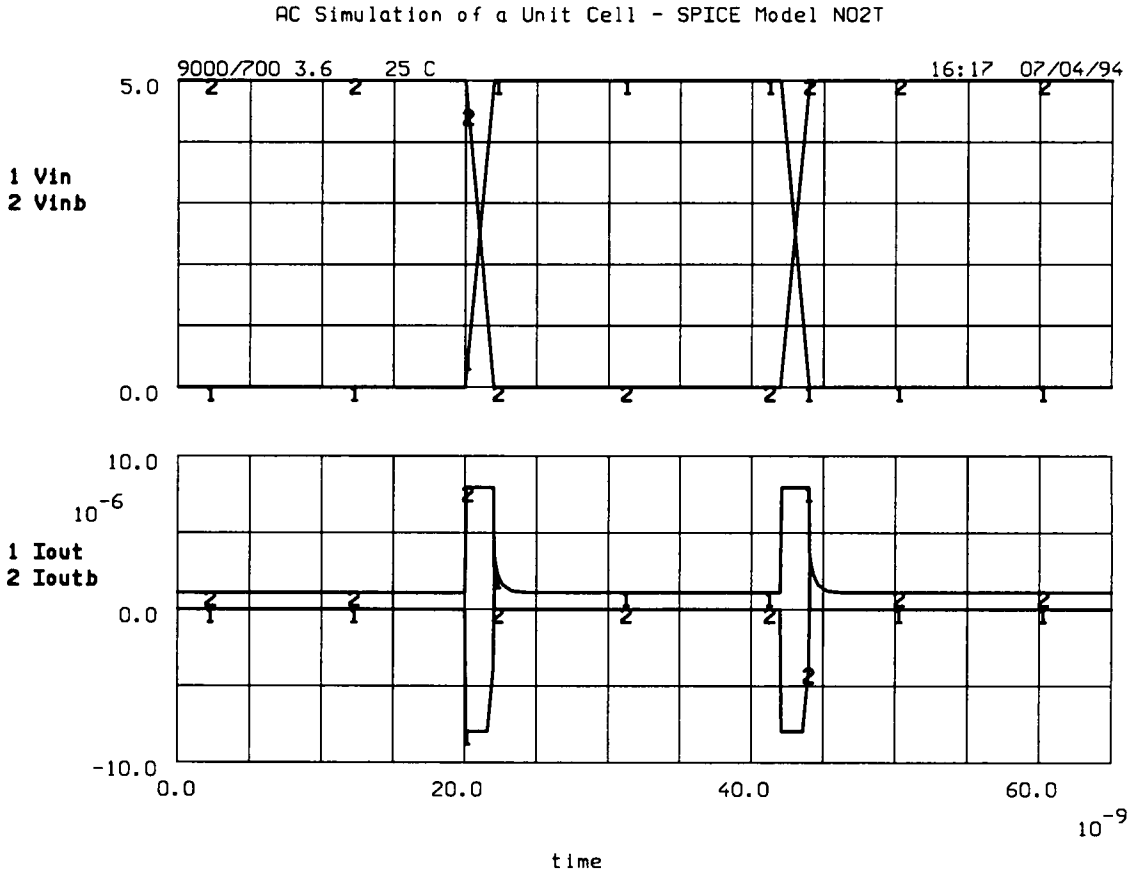

Figure 3.22: Effect of feedthrough current on the output currents I_{out} and $\overline{I_{out}}$ of a unit cell at $I_{ref} = 1\ \mu A$ (SPICE model N02T).

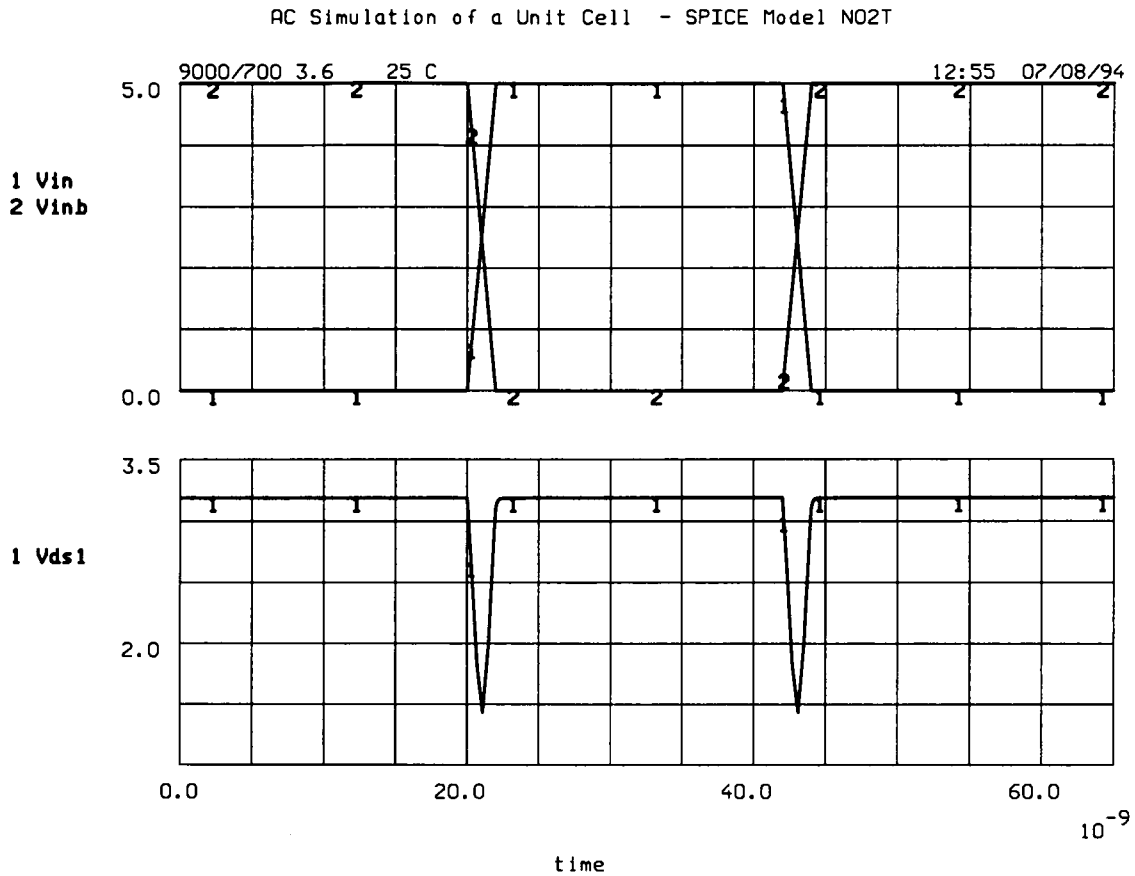

Figure 3.23: Effect of feedthrough current on the drain voltage of the current source transistor M_1 of a unit cell at $I_{ref} = 28\ \mu A$ (SPICE model N02T).

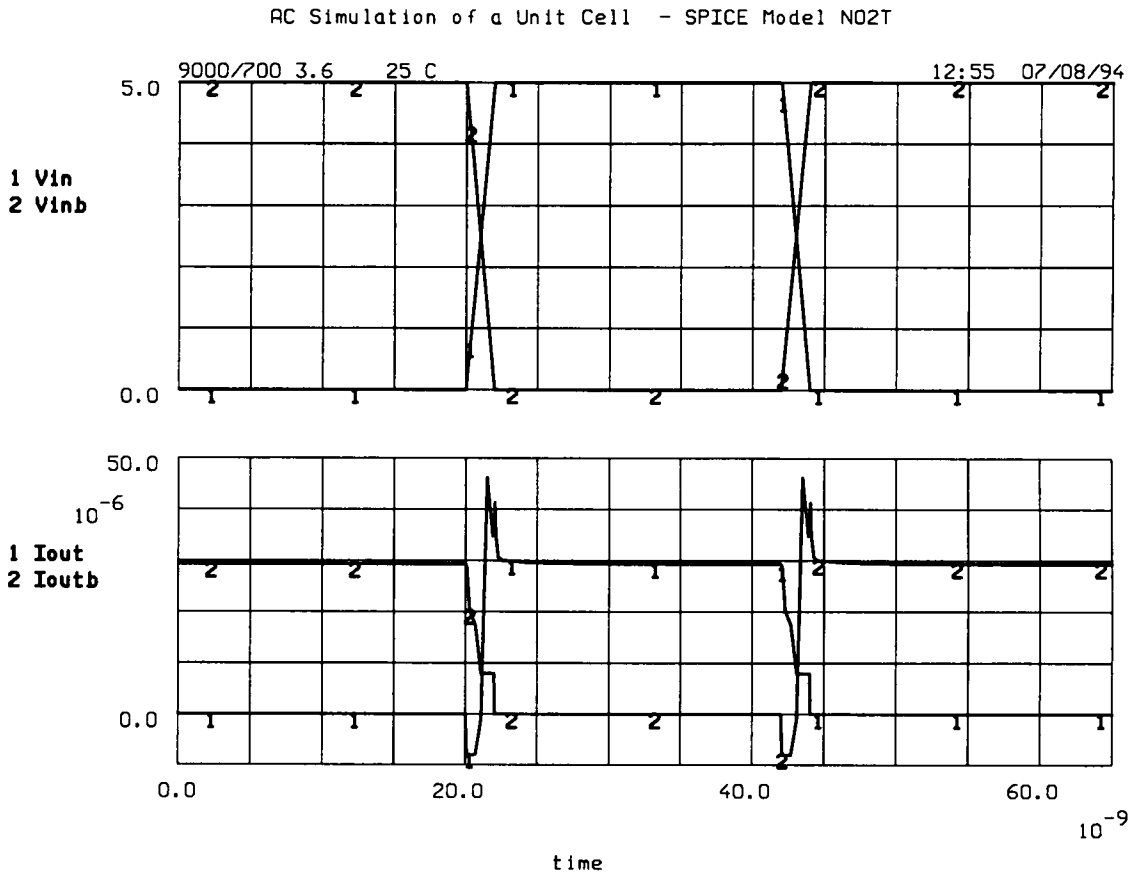

Figure 3.24: Effect of feedthrough current on the output currents I_{out} and $\overline{I_{out}}$ of a unit cell at $I_{ref} = 28\ \mu A$ (SPICE model N02T).

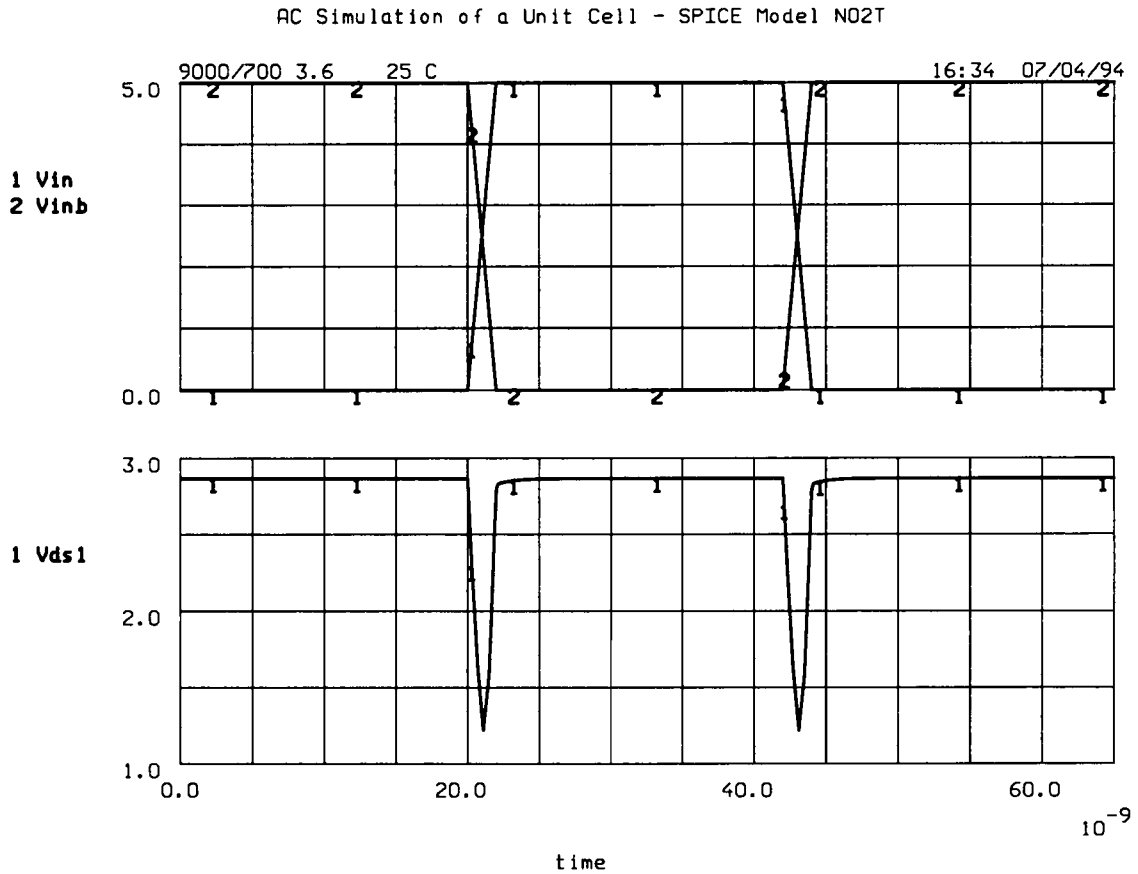

Figure 3.25: Effect of feedthrough current on the drain voltage of the current source transistor M_1 of a unit cell at $I_{ref} = 109\ \mu A$ (SPICE model N02T).

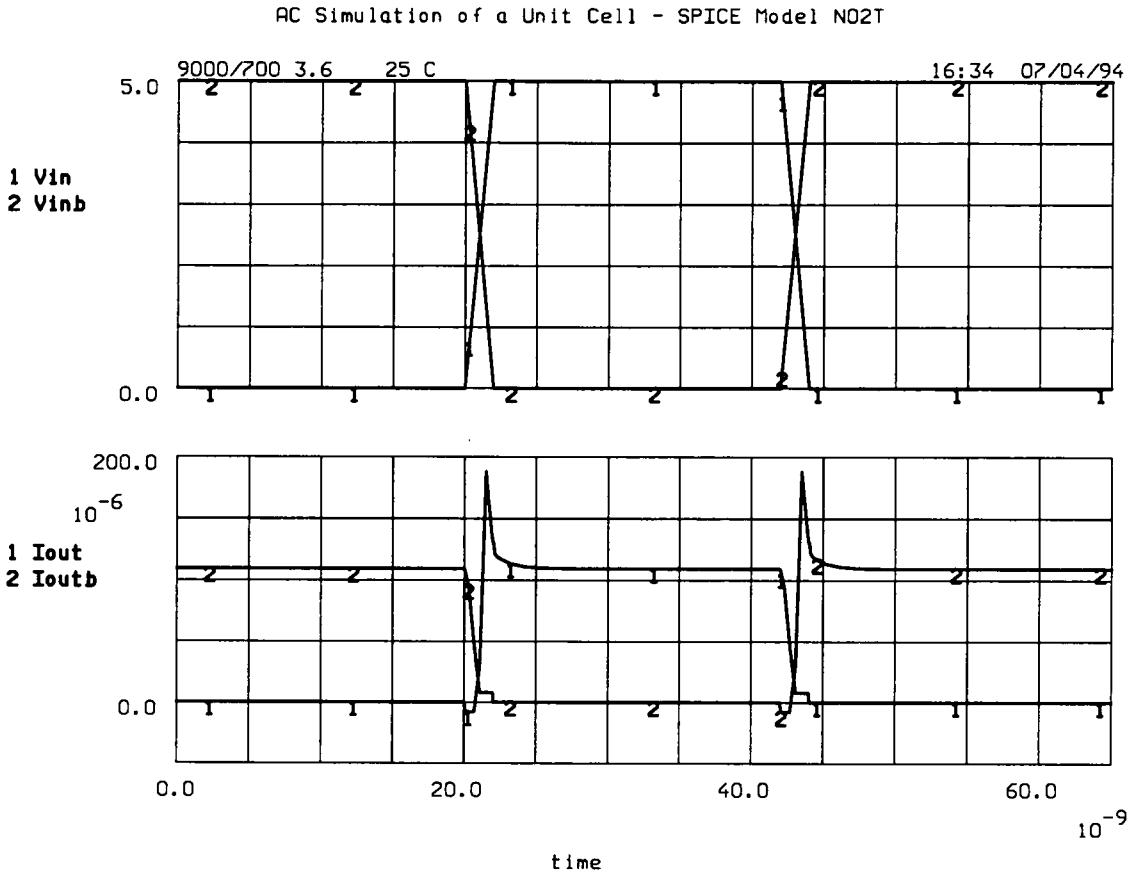

Figure 3.26: Effect of feedthrough current on the output currents I_{out} and $\overline{I_{out}}$ of a unit cell at $I_{ref} = 109\ \mu A$ (SPICE model N02T).

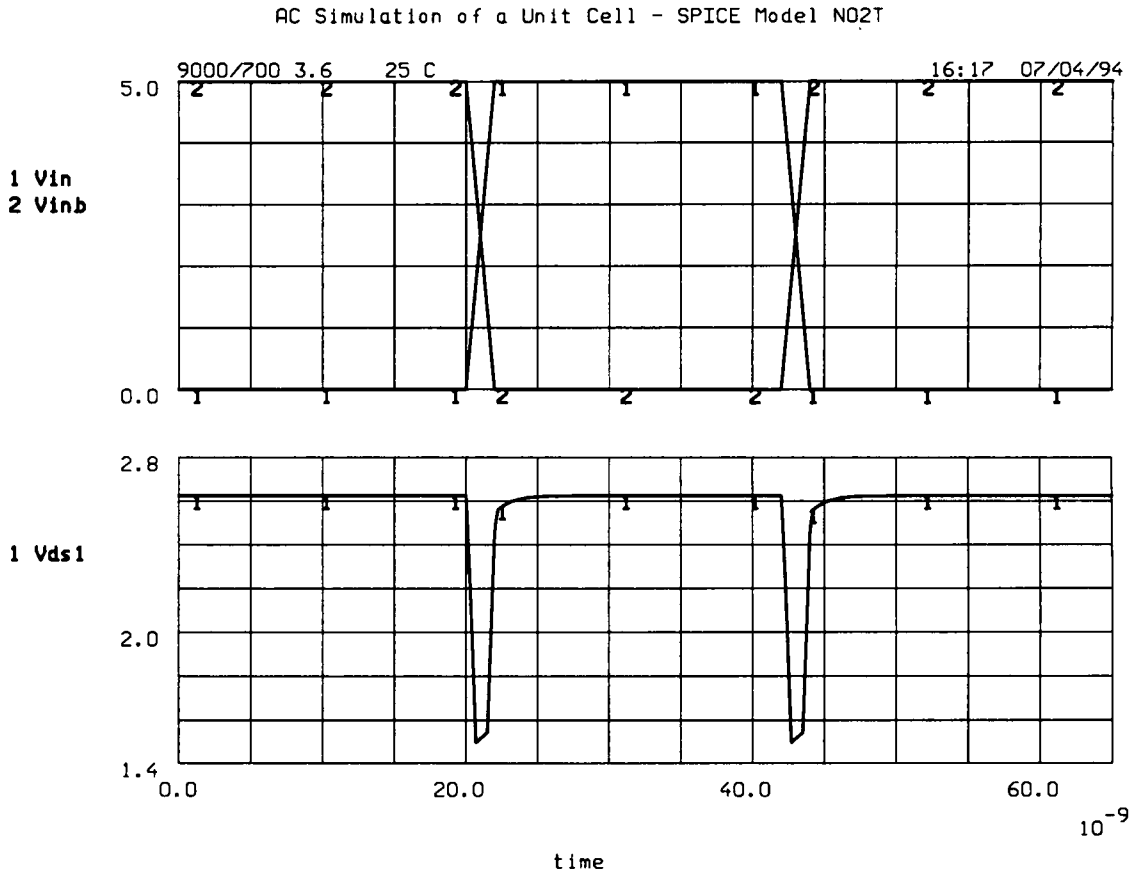

Figure 3.27: Effect of feedthrough current on the drain voltage of the current source transistor M_1 of a unit cell at $I_{ref} = 209.6\ \mu A$ (SPICE model N02T).

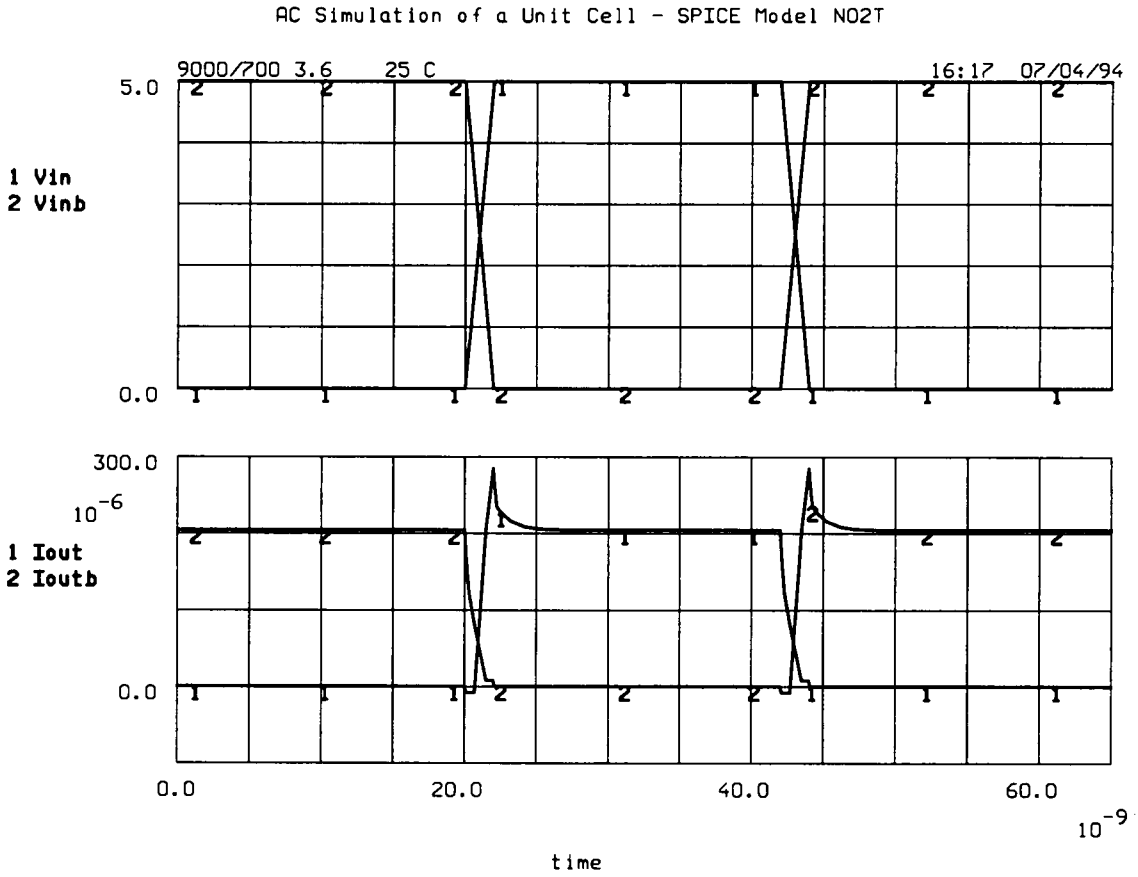

Figure 3.28: Effect of feedthrough current on the output currents I_{out} and $\overline{I_{out}}$ of a unit cell at $I_{ref} = 209.6\ \mu A$ (SPICE model N02T).

Appendix C.

3.4.5 Simulated Output Impedance of a Unit Cell

The simulated r_{out} of a unit cell using different SPICE models are given in Figures 3.29, 3.30, and 3.31. Figure 3.32 gives the r_{out} of the unit cell for different SPICE models plotted on the same graph. These simulations are as the result of AC analysis of the output voltage, while sweeping the gate voltage of the current source. As shown in the Figures 3.29, 3.30, and 3.31, the output impedance of the unit cell is quite large at low output currents, when V_{gs} of the current source is small and becomes smaller at higher output currents. This is due to the fact that r_{out} is inversely proportional to I_{out}. The slope of the curve is quite constant till the current source transistor switches from operating in the saturation region to the linear region. At this point there is a larger change in the output resistance of the unit cell as the output current increases. At higher output currents, when the current source is operating in the linear region, the current source is not a very good current source.

As shown in Figure 3.32, due to variation in the SPICE models the current source transistor mode of operation switching varies from model to model; and the variation in the output impedance of the different models is not too large.

A sample SPICE netlist used for this simulation can be found in the Appendix D.

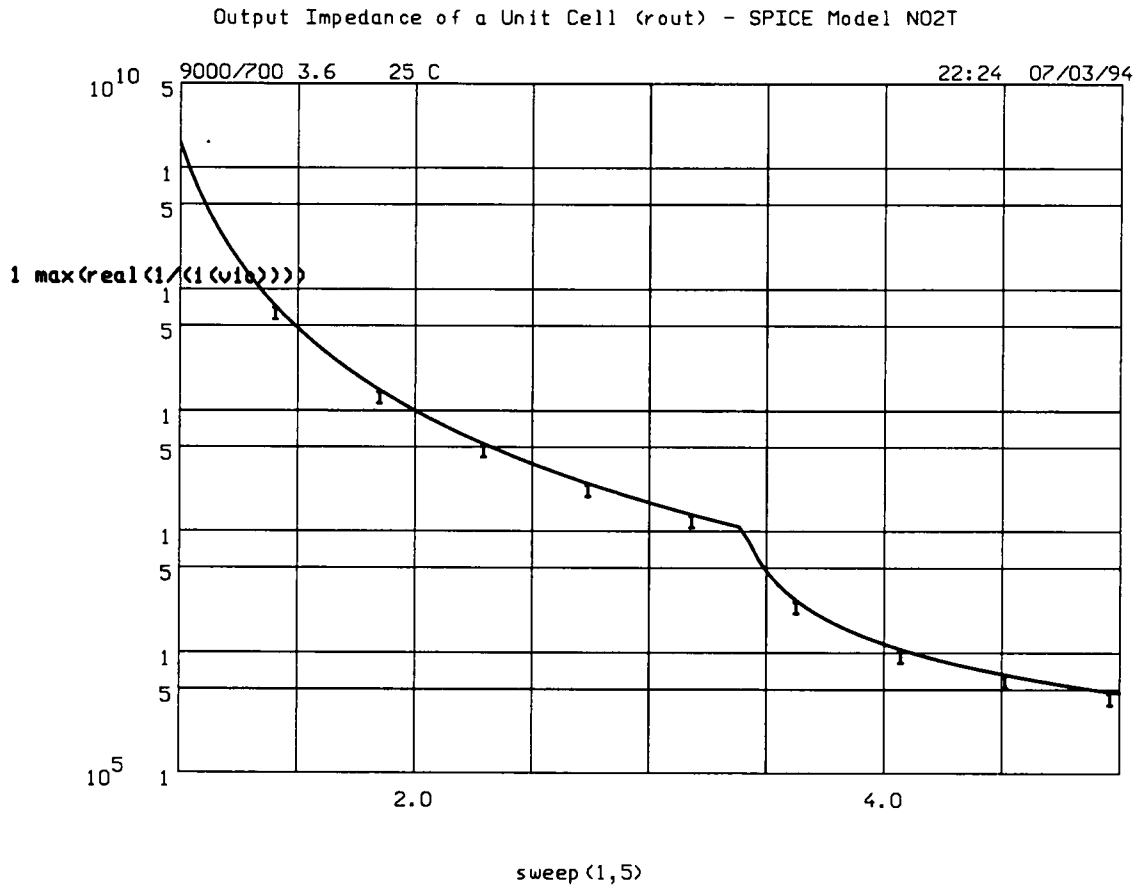

Figure 3.29: Simulated output impedance, $r_{out}(\Omega)$ versus the $V_{gs}(V)$ of the current source of a unit cell (chip SPICE model N02T).

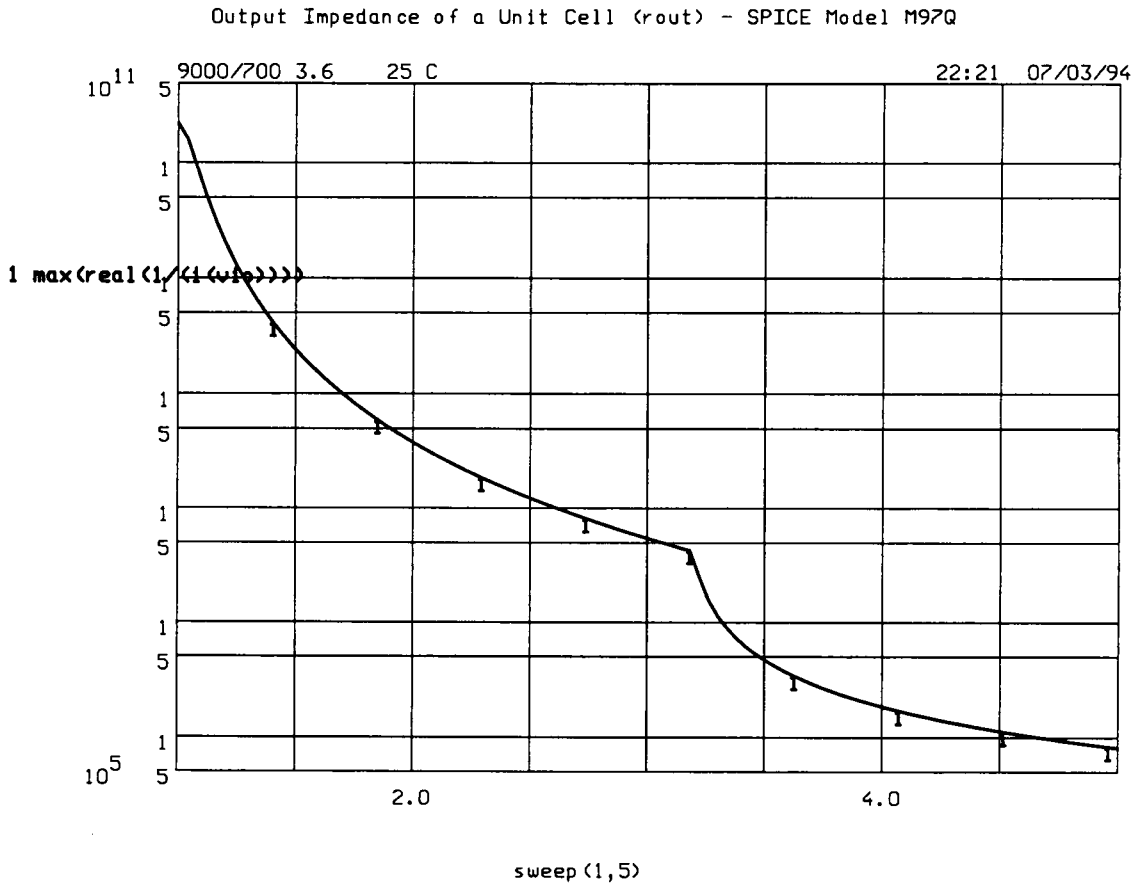

Figure 3.30: Simulated output impedance, $r_{out}(\Omega)$ versus the $V_{gs}(V)$ of the current source of a unit cell (SPICE model M97Q).

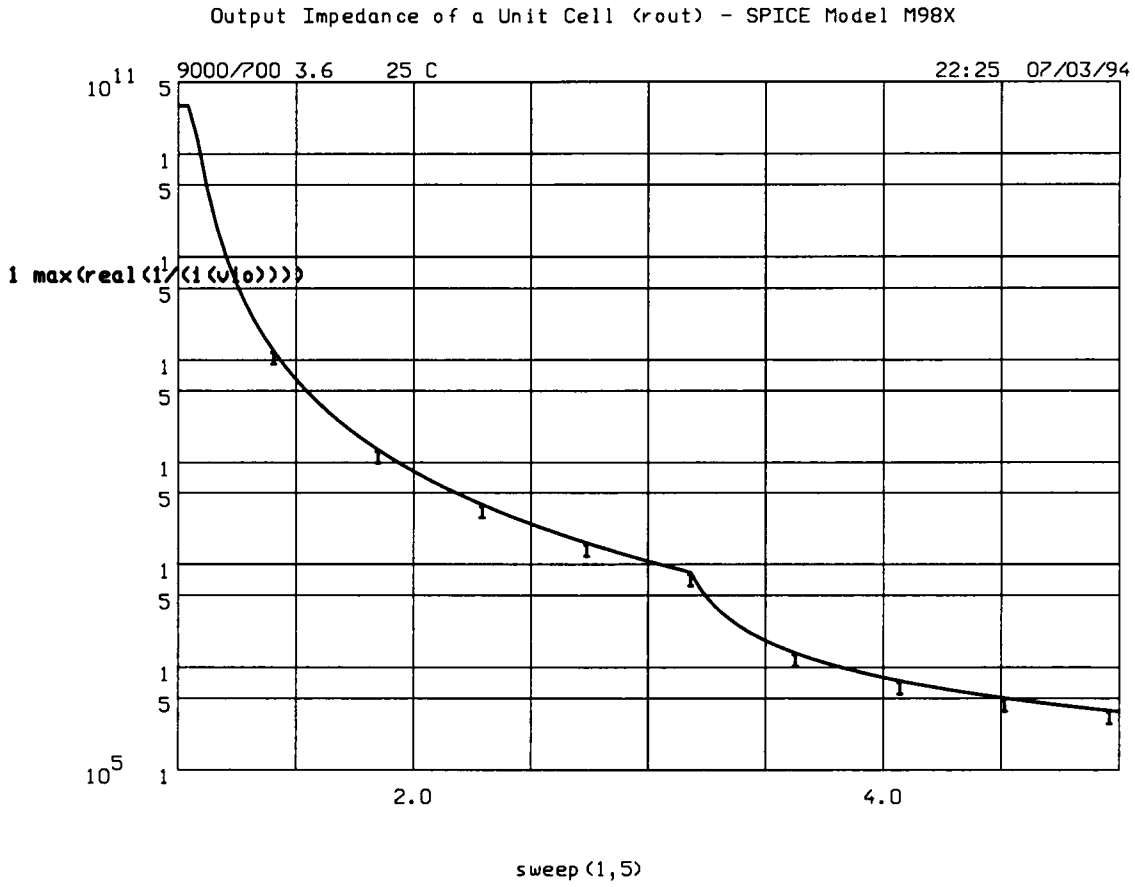

Figure 3.31: Simulated output impedance, $r_{out}(\Omega)$ versus the $V_{gs}(V)$ of the current source of a unit cell (SPICE model M98X).

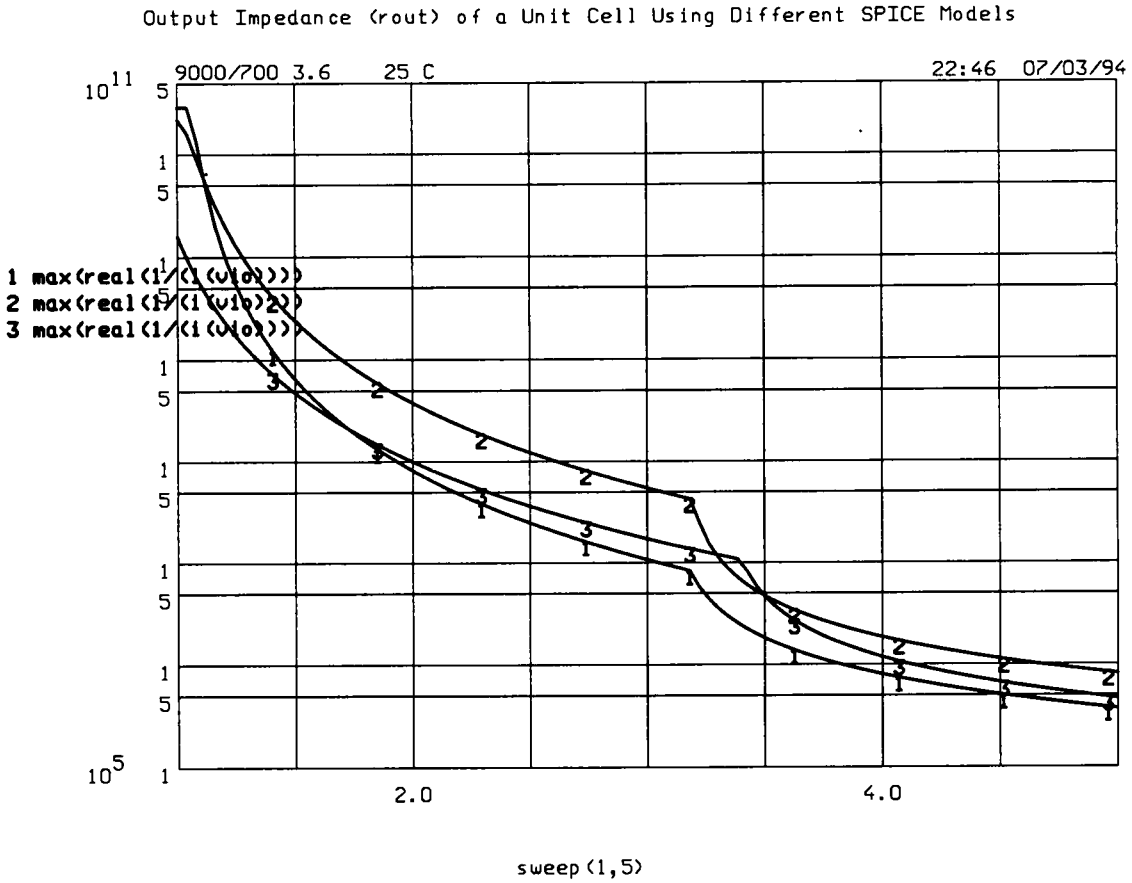

Figure 3.32: Simulated output impedance, $r_{out}(\Omega)$ versus the $V_{gs}(V)$. Curve 1 uses M98X model, curve 2 uses M97Q model, and curve 3 uses N02T (extracted chip) model

CHAPTER 4

EXPERIMENTAL RESULTS

The previous chapter presented the design detail and theory of operation of the six-bit current source DAC. In this chapter, experimental results showing the performance of the DAC are given. The DAC was fabricated in 2 μm MOSIS process. Four chips were received and three were fully functional.

4.1 Test Setup of the DAC

Figure 4.1 shows the block diagram of the test setup of the six-bit current DAC. As shown in Figure 4.1, the test setup consists of a six-bit dip switch, an HP4145B Semiconductor Parameter Analyzer, an external power supply to power the digital circuits of the chip, and the device under test (DUT). This setup allowed the forcing of current into the DAC at I_{ref} and measuring the voltage at that node. Voltages were forced at I_{out} and $\overline{I_{out}}$ and the currents were measured. Through source monitor units SMU2 and SMU3 voltages between 0 and 5 V were forced into the DAC at nodes I_{out} and $\overline{I_{out}}$ in 0.5 V increments. The input reference current I_{ref} of SMU1 was swept from 1 to 217 μA in steps of 27 μA. The input codes were set using the dip switches, and the currents I_{out} and $\overline{I_{out}}$ were measured. For each input combination, a total of 121 data points were taken per DAC.

The testings were semi-automated through the use of HP4145B for sweeping

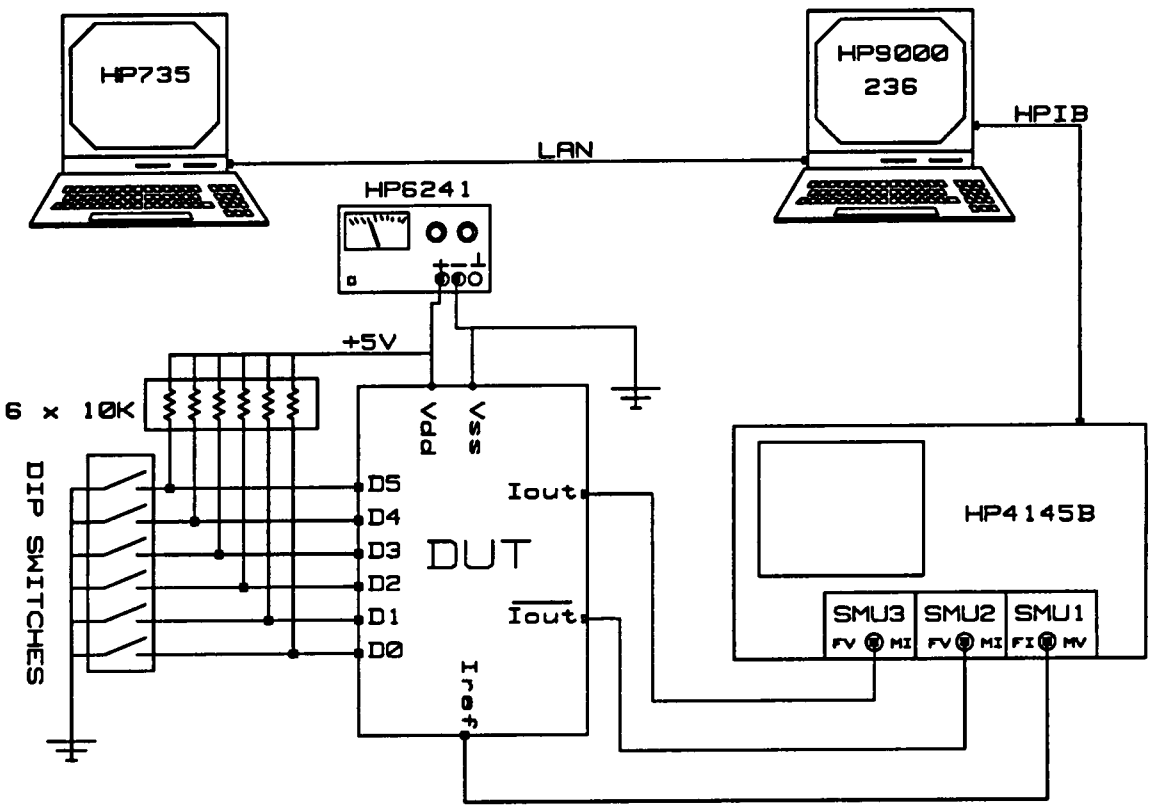

Figure 4.1: Block diagram of the test setup using HP4145B

voltages and current, but the switching of the input bits was done manually. The measured data was then transferred over the network to a computer where it was processed.

4.2 Input Reference Current (I_{ref}) Versus Reference Voltage (V_{ref})

Figure 4.2 shows the reference voltage V_{ref} versus the input current I_{ref} of the diode connected transistors of each of the DACs on Chip1, Chip2, and Chip3. The reference voltage is the V_{gs} and V_{ds} of the reference transistor M_{ref} as shown in Figure 3.1. This measurement was done by injecting a sweep of current from 1 to 271 μA into I_{ref} and measuring the voltage at that node.

4.3 Voltage-Current Characteristics and Output Impedance of a Unit Cell

The voltage-current characteristics of the LSB unit cell in each DAC are given in Figures 4.3, 4.4, and 4.5. These plots were generated by sweeping the reference current supply from 1 to 271 μA in 27 μA increments, while the output voltage supplies were swept from 0 to 5 V in steps of 0.25 V. These measurements were done using the LSB input code of 000001.

Figures 4.3, 4.4, and 4.5 show that the current source transistor, on each chip moves from the linear region of operation to the saturation region at $V_{out(min.)}$. This is when the vertical part of the curve changes to the horizontal. The measured

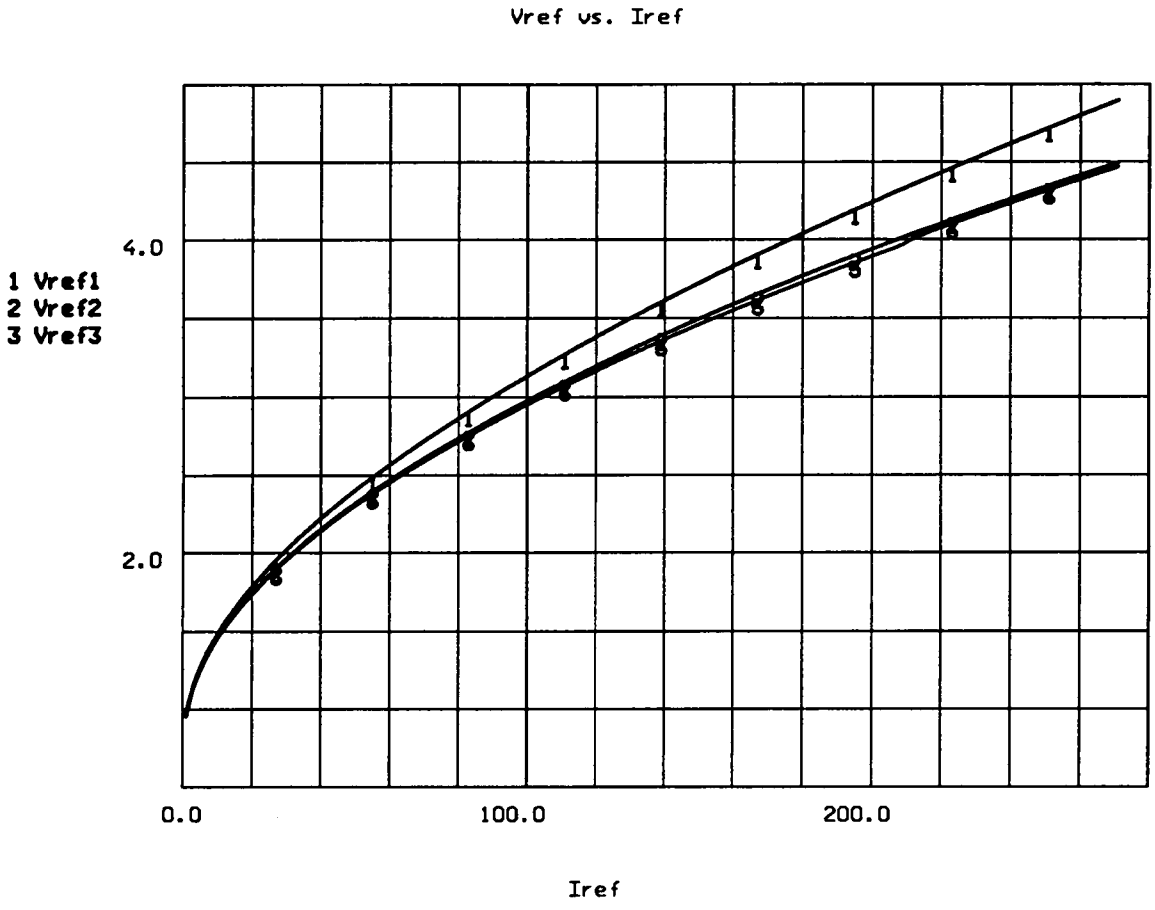

Figure 4.2: V_{ref} (V) versus I_{ref} (μA) of Chip1, Chip2, and Chip3

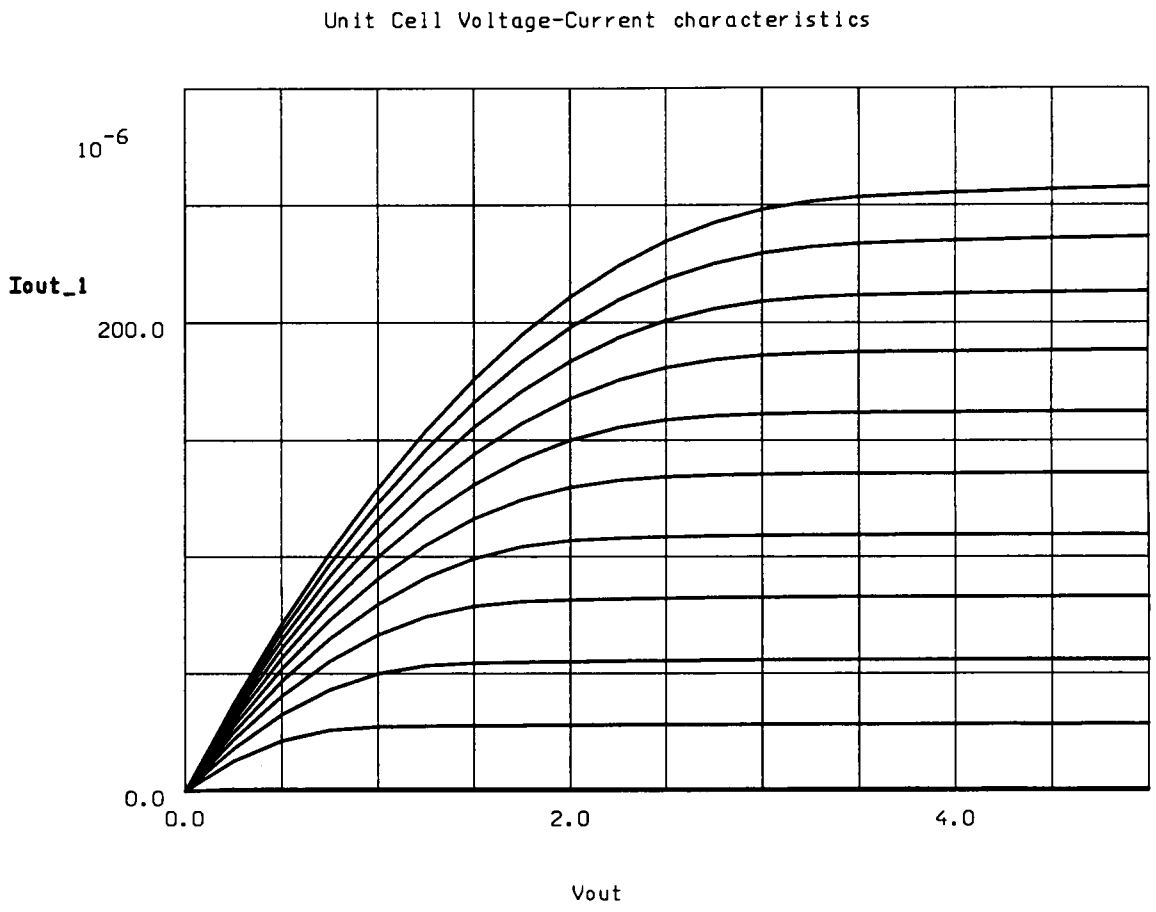

Figure 4.3: Unit cell output characteristics of Chip1

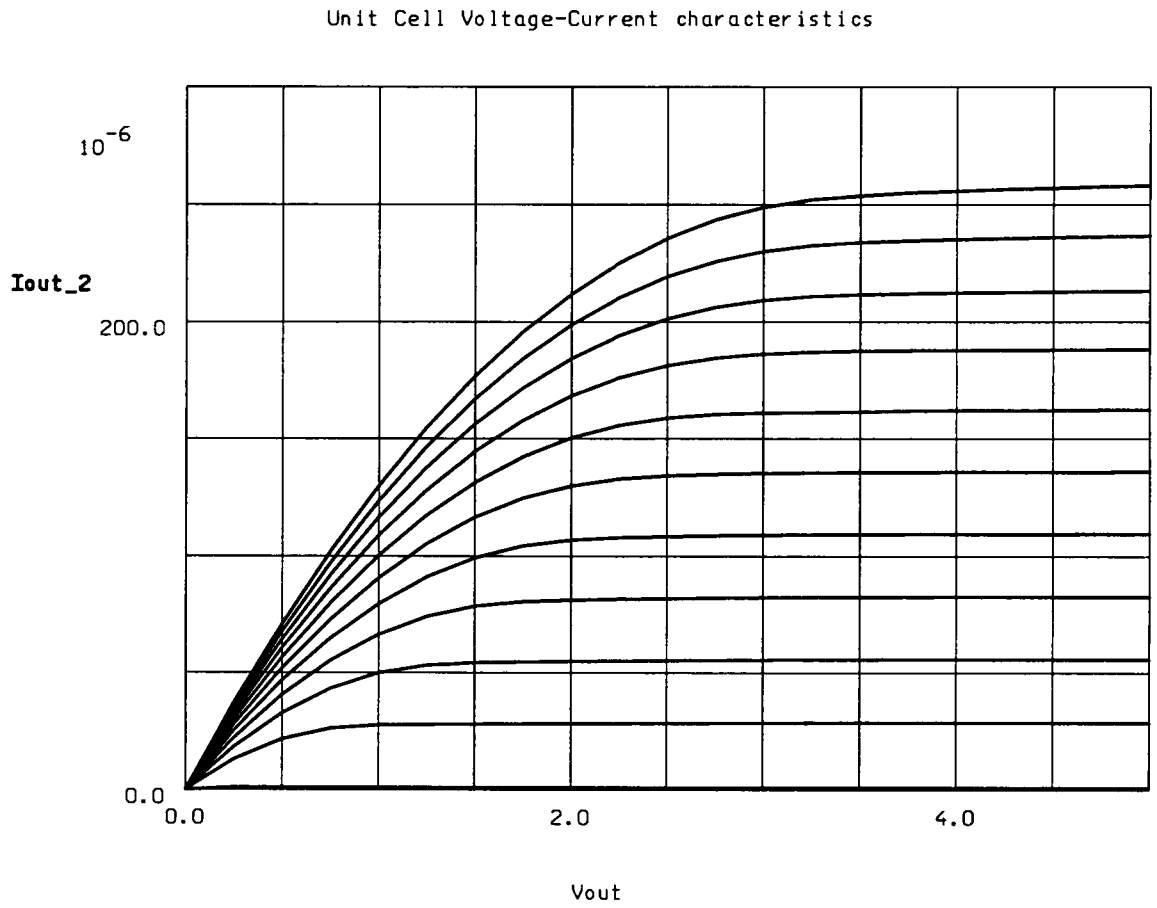

Figure 4.4: Unit cell output characteristics of Chip2

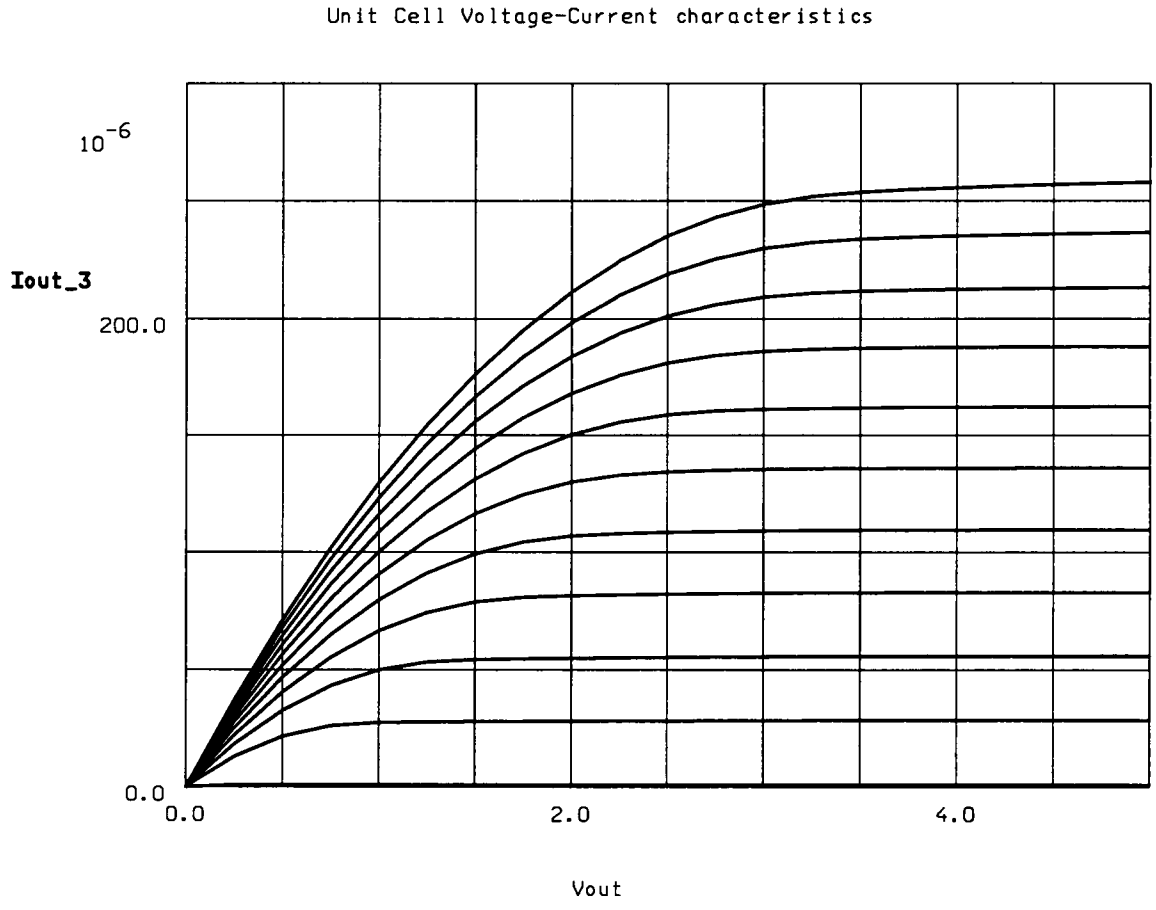

Figure 4.5: Unit cell output characteristics of Chip3

saturation points at $V_{out(min.)}$ on each chip matches the theoretical and simulated results, as were discussed in the previous chapter.

Although it appears that the unit cell is operating properly at higher I_{ref} currents after the output current passes $I_{out(max.)}$, the switch transistors will be operating in the saturation region and the current source transistor will no longer be operating in the saturation region. The current will therefore depend on the value of the switch gate voltage.

The output impedance of the unit cell was determined by calculating the slope of the family of the current curves at a V_{out} voltage of 4.5 V. Figures 4.6, 4.7, and 4.8 give the output impedance, r_{out} versus the reference current of each DAC's unit cell. The output impedance plots of each DAC match very closely with the simulated results presented in the previous chapter.

4.4 Transfer Characteristics of the DAC

For the representation of the transfer characteristics of each DAC, only four current levels per DAC are reported here. The input reference currents were swept from 1 to 271 μA in steps of 27 μA, while the output voltage at I_{out} and $\overline{I_{out}}$ were swept from 0 to 5 V in increments of 0.5 V. The transfer characteristics are reported here for input reference currents of 1, 28, 109, and 217 μA.

Figures 4.9, 4.10, and 4.11 give the transfer characteristics of I_{out}, $\overline{I_{out}}$, and $(I_{out} - \overline{I_{out}})$ for I_{LSB} =1 μA, for all three DACs at V_{out} voltages of 1 and 5 V. From these transfer characteristics plots, it is clear that the analog output of the

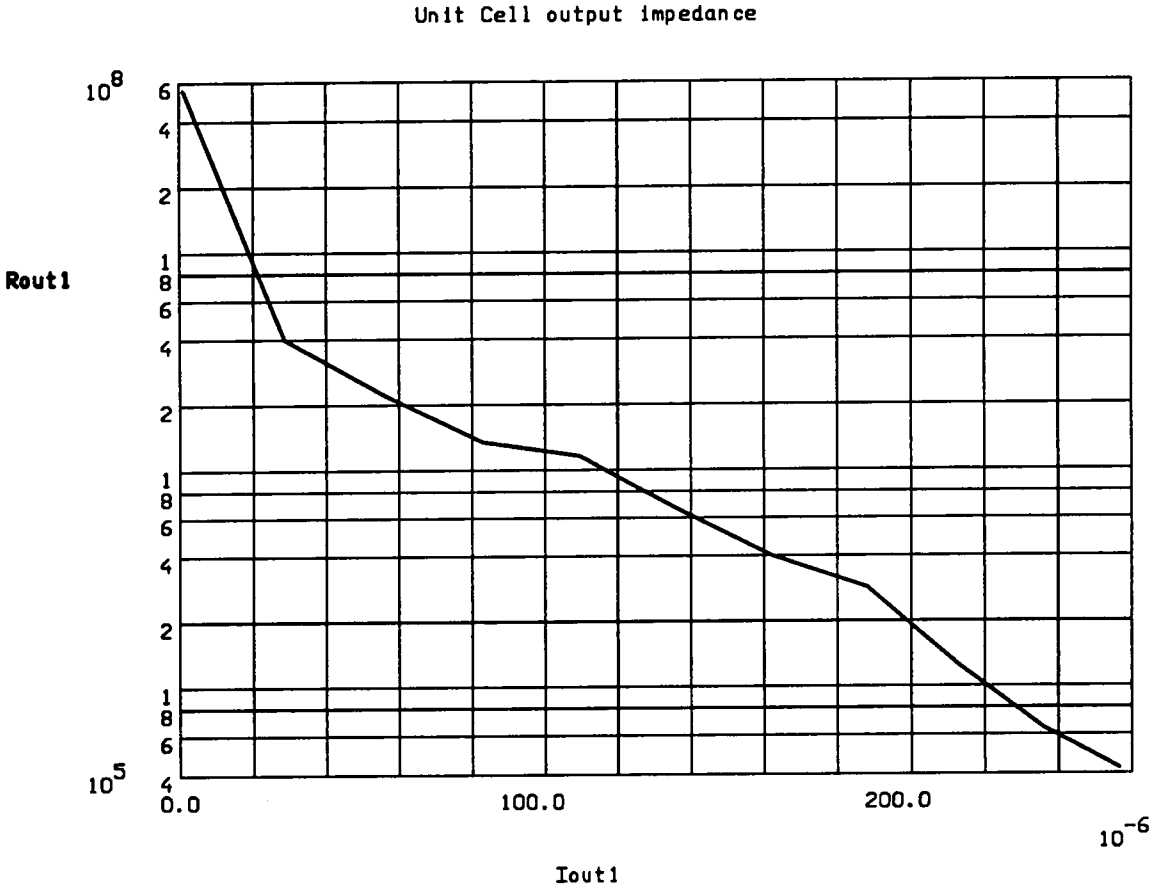

Figure 4.6: r_{out} (Ω) versus I_{out} (μA) - Chip1

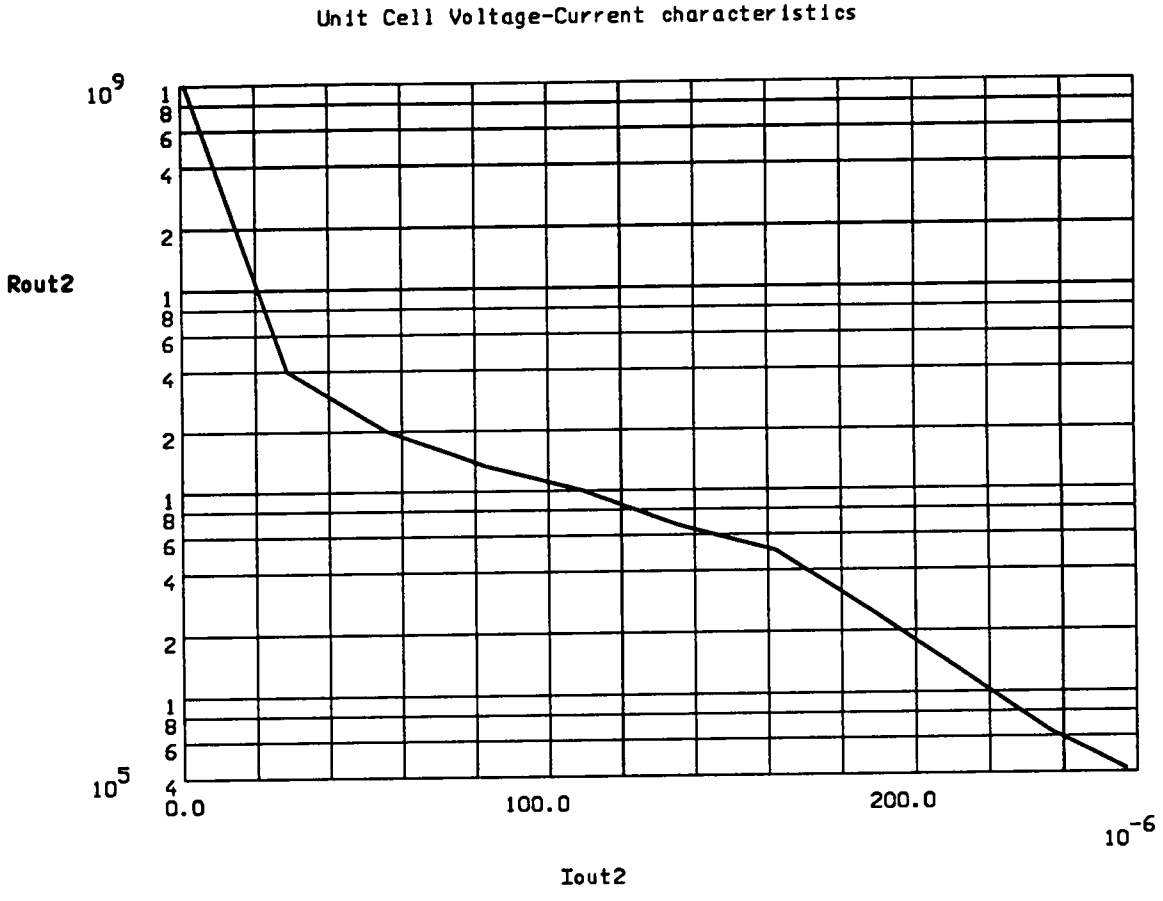

Figure 4.7: r_{out} (Ω) versus I_{out} (μA) - Chip2

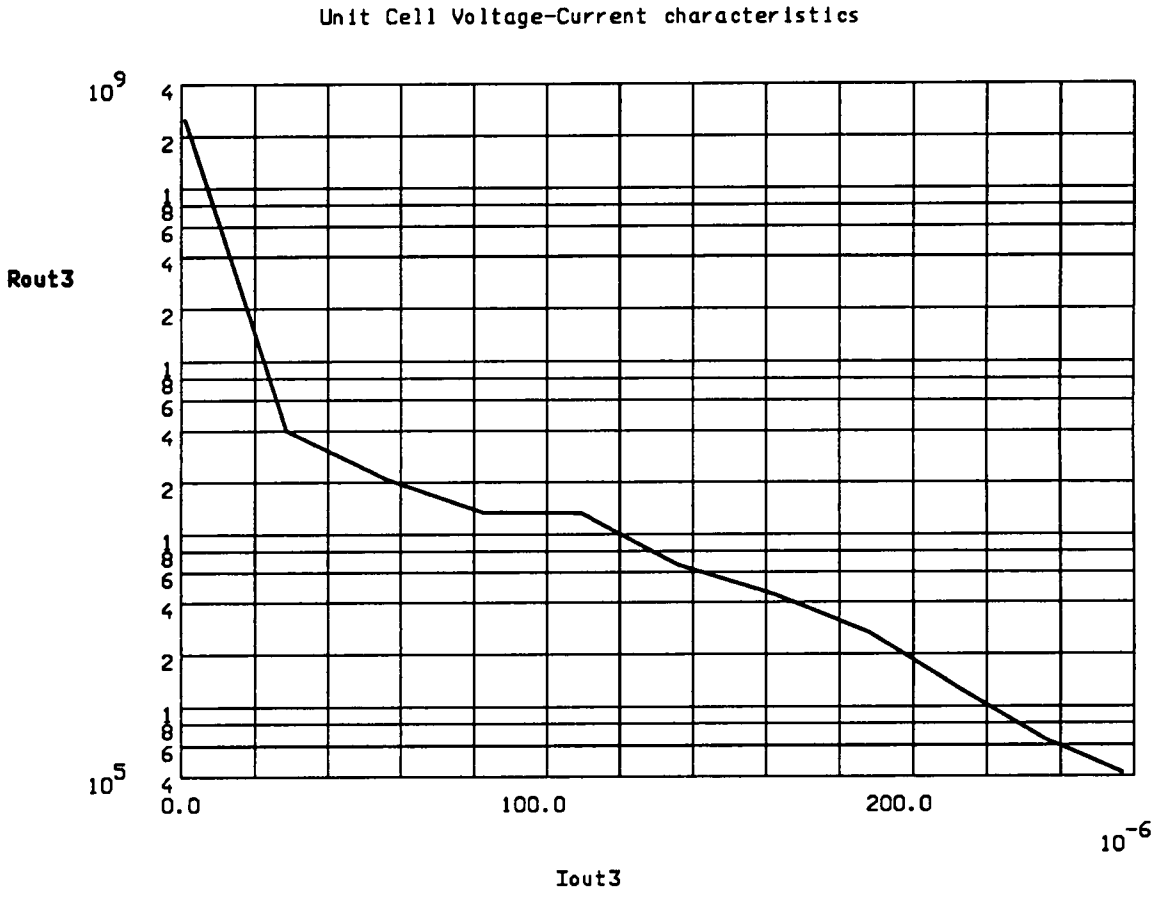

Figure 4.8: r_{out} (Ω) versus I_{out} (μA) - Chip3

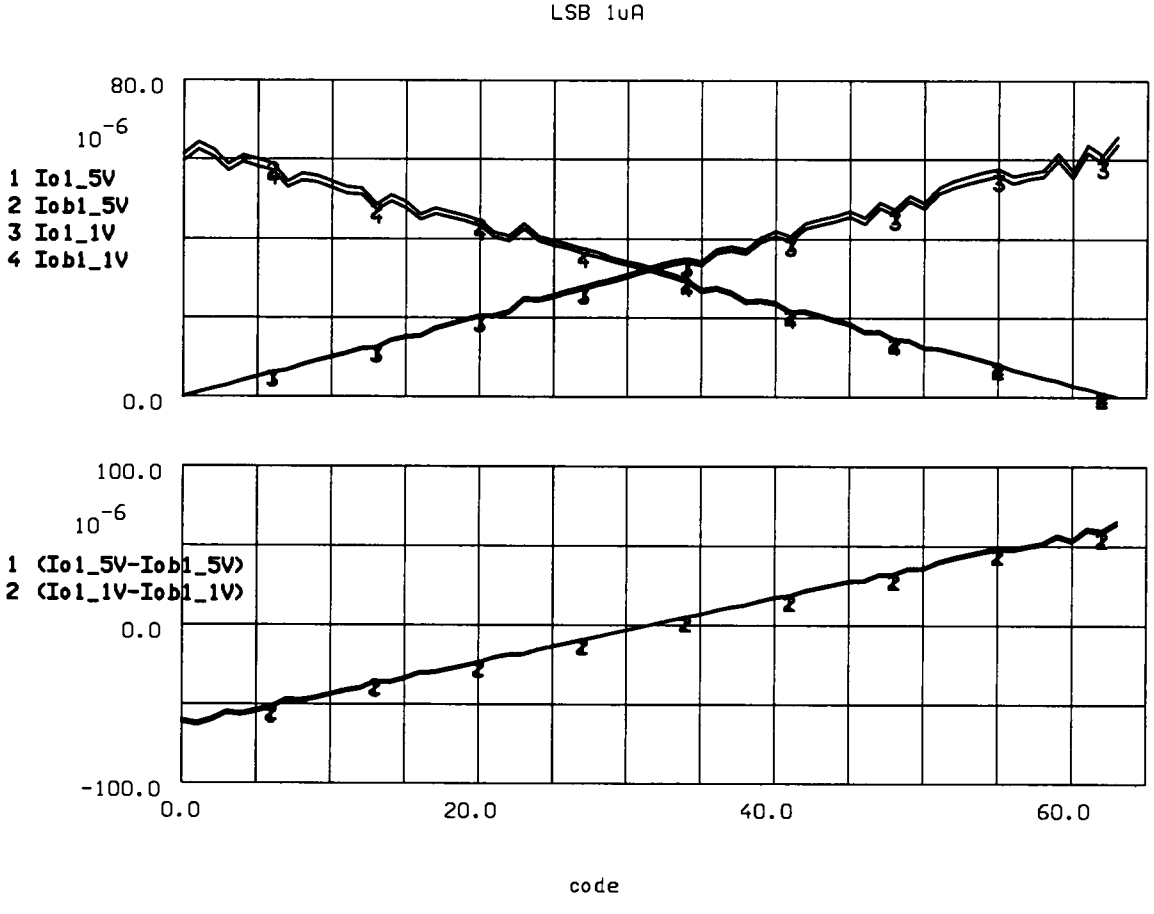

Figure 4.9: Transfer characteristics of DAC on Chip1 at $I_{LSB} = 1\ \mu A$, $V_{out} = 1,5V$

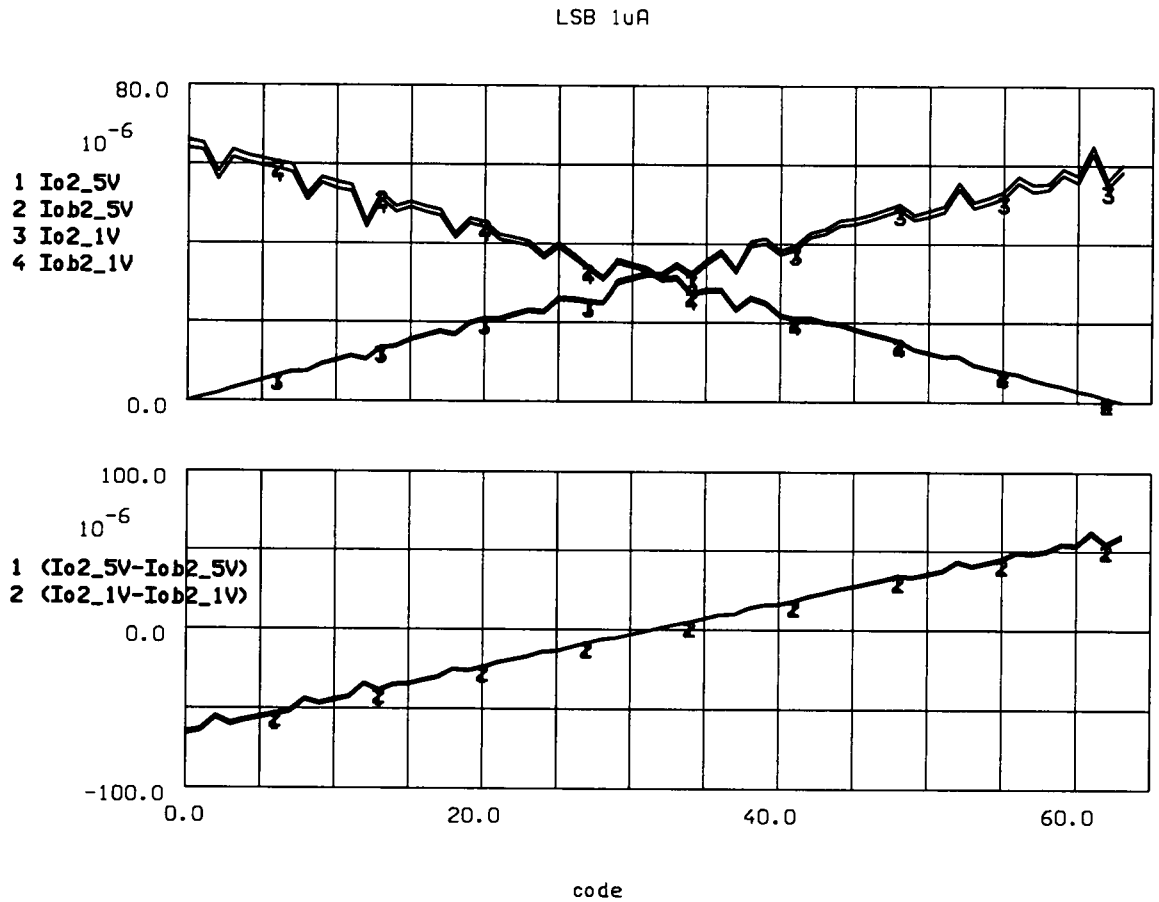

Figure 4.10: Transfer characteristics of DAC on Chip2 at $I_{LSB} = 1\ \mu A$, $V_{out} = 1,5V$

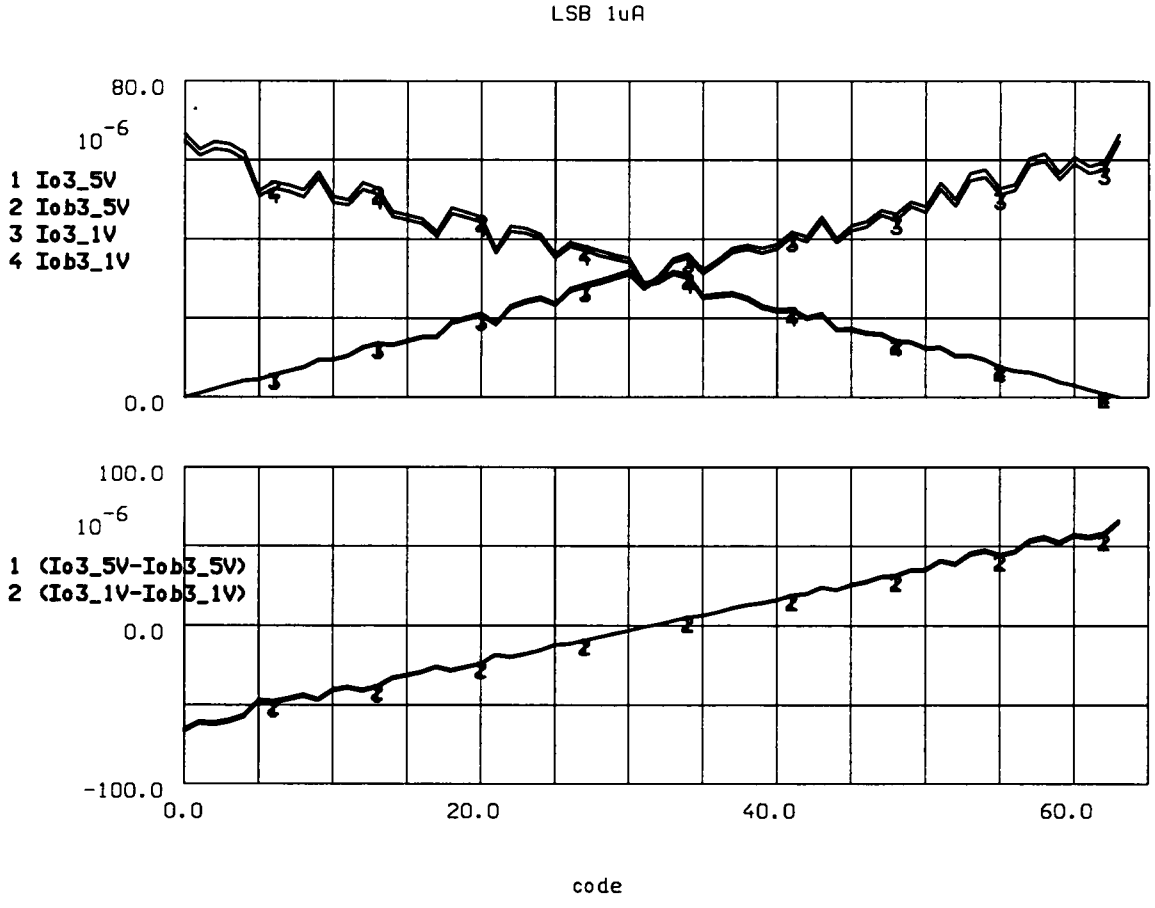

Figure 4.11: Transfer characteristics of DAC on Chip3 at $I_{LSB} = 1\ \mu A$, $V_{out} = 1,5V$

DAC is not monotonic at 1 μA. This type of behavior is independent of the output voltage.

Figures 4.12, 4.13, and 4.14 give the transfer characteristics for I_{LSB} =28 μA. Unlike the results for I_{ref} = 1 μA, at 28 μA the DAC is monotonic. As shown in these plots, the transfer characteristic curves are quite smooth, and the output current increases as the input code increases. The output current at output voltage of 1.5 V is not completely the same as the 5 V results, mainly due to λ effect, and the fact that the differential pair switches will no longer be operating in the linear region at the output voltage of 5 V.

Similarly, Figures 4.15, 4.16, and 4.17 show the transfer curves for I_{LSB} =109 μA and V_{out} voltages of 2.5 and 5 V, and Figures 4.18, 4.19, and 4.20 represent I_{LSB} =217 μA and V_{out} voltages of 3 and 5 V. The DAC is monotonic at 109 μA, and nonmonotonic at 217 μA, as shown in the plots. Since the higher input current measurements required higher $V_{out(min.)}$ values, the λ effect is minimized due to the fact that the V_{ds} of the current sources are higher. Therefore, the transfer curves at 109 μA currents for different voltages are almost equal. I_{LSB} = 109 μA is just below the simulated and calculated $I_{out(max.)}$, where the current source transistors are still in the saturation region. At I_{LSB} = 217 μA, the current source transistors are no longer in the saturation region and will be operating in the linear region. And at higher output voltages the switch transistors are no longer in the linear region and will be operating in the saturation region.

In summary, the DAC does not have a good transfer characteristics at low input currents of 1 μA, or above $I_{out(max)}$.

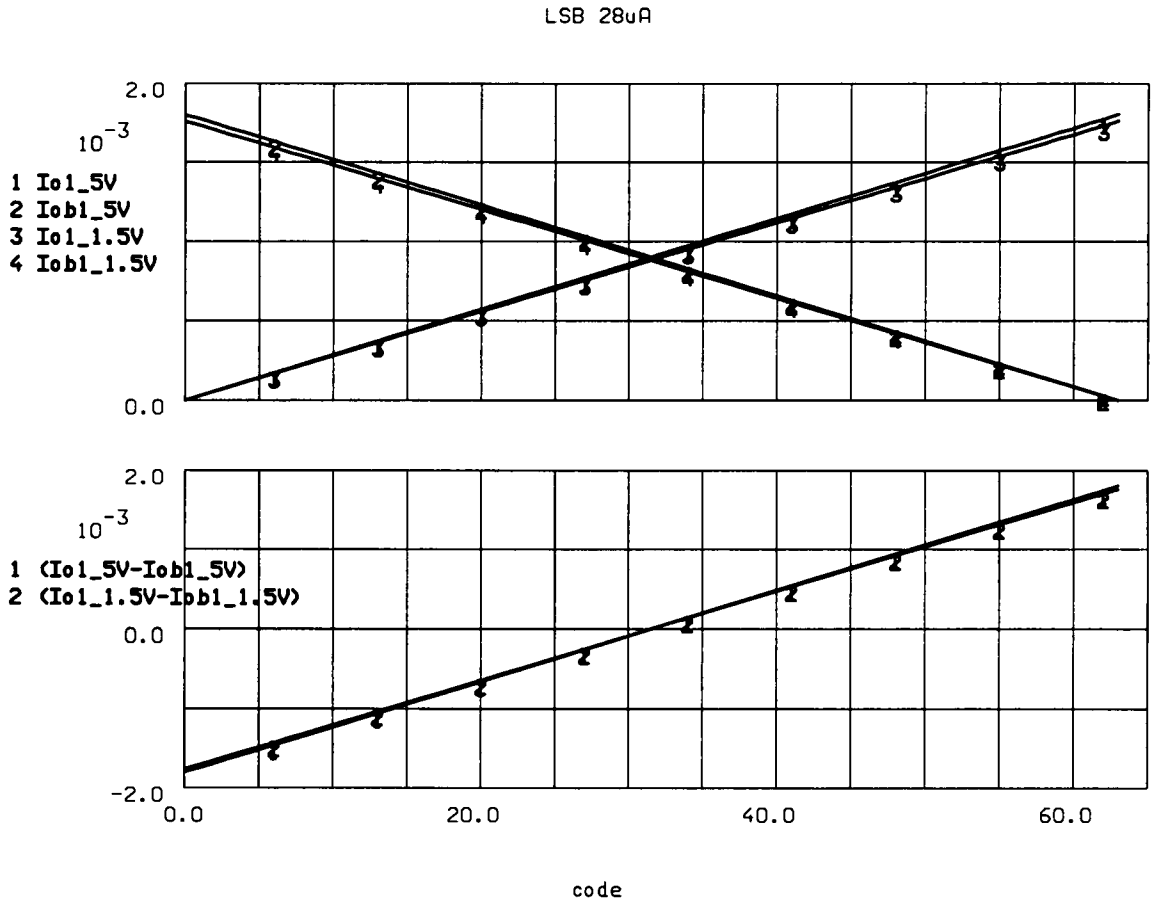

Figure 4.12: Transfer characteristics of DAC on Chip1 at $I_{LSB} = 28\ \mu A$, $V_{out} = 1.5, 5V$

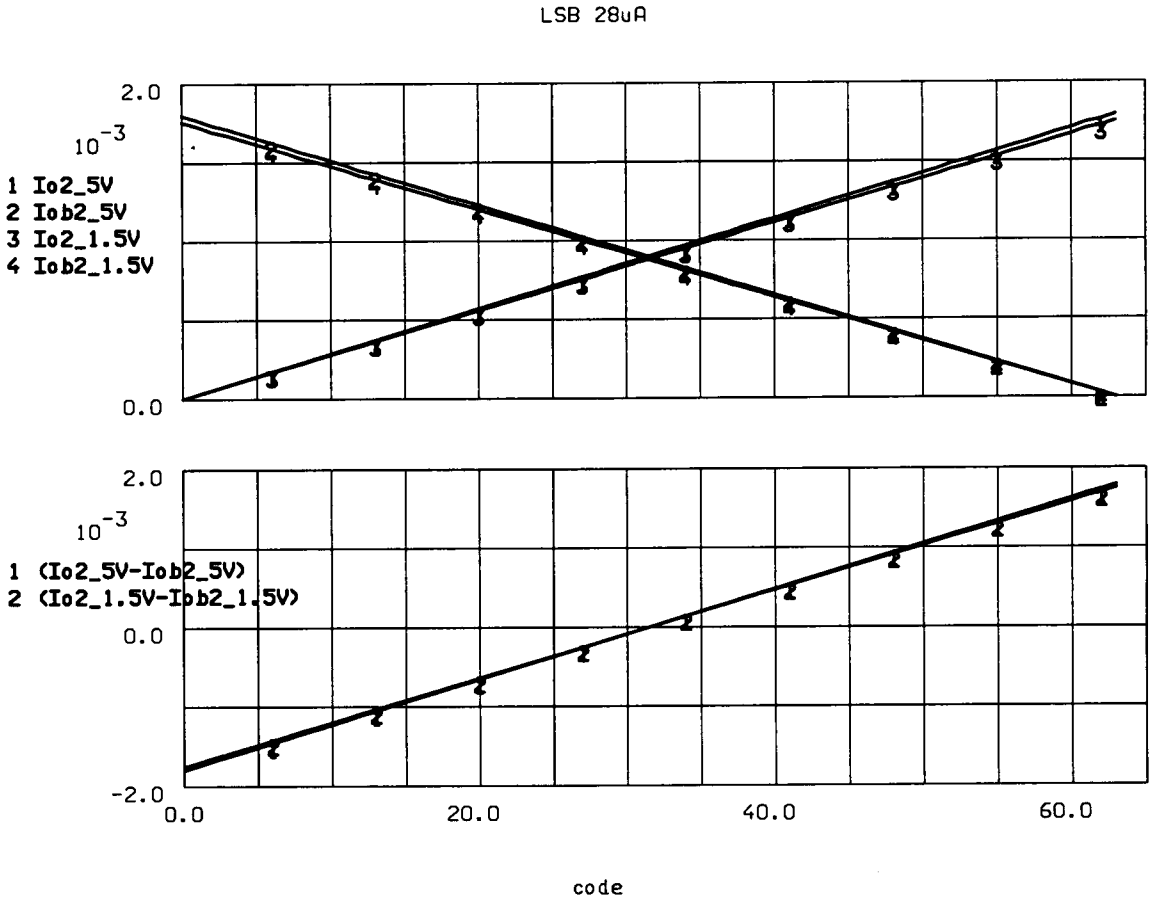

Figure 4.13: Transfer characteristics of DAC on Chip2 at $I_{LSB} = 28\ \mu A$, $V_{out} = 1.5, 5V$

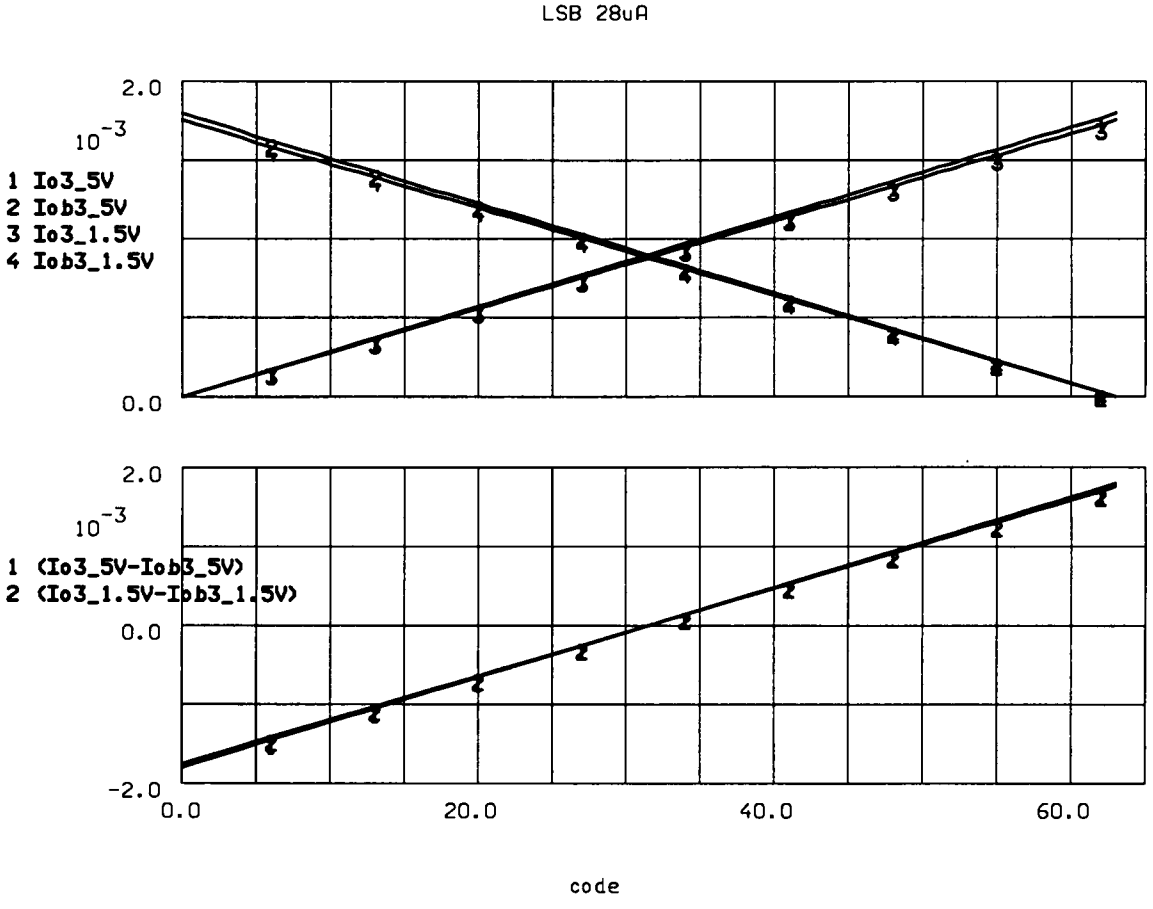

Figure 4.14: Transfer characteristics of DAC on Chip3 at $I_{LSB} = 28\ \mu A$, $V_{out} = 1.5, 5V$

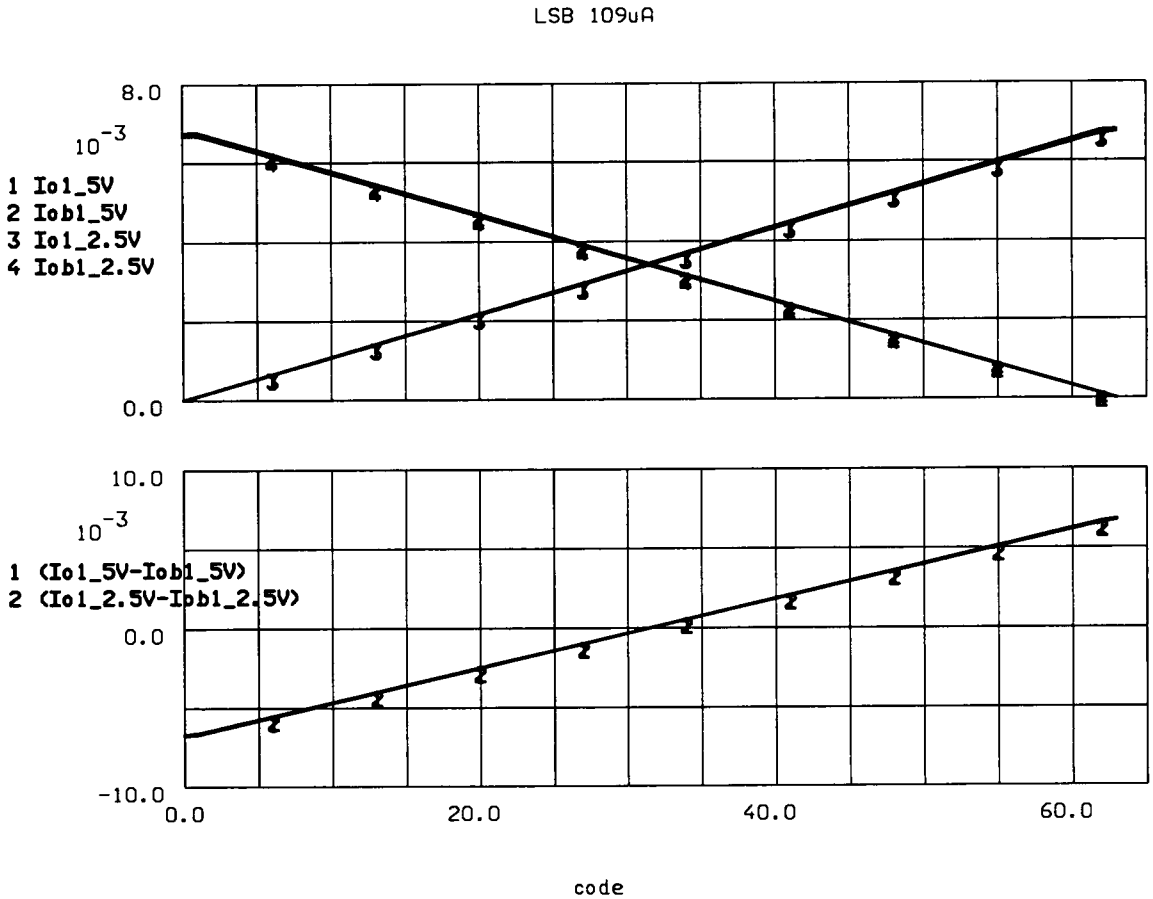

Figure 4.15: Transfer characteristics of DAC on Chip1 at $I_{LSB} = 109\ \mu A$, $V_{out} = 2.5, 5V$

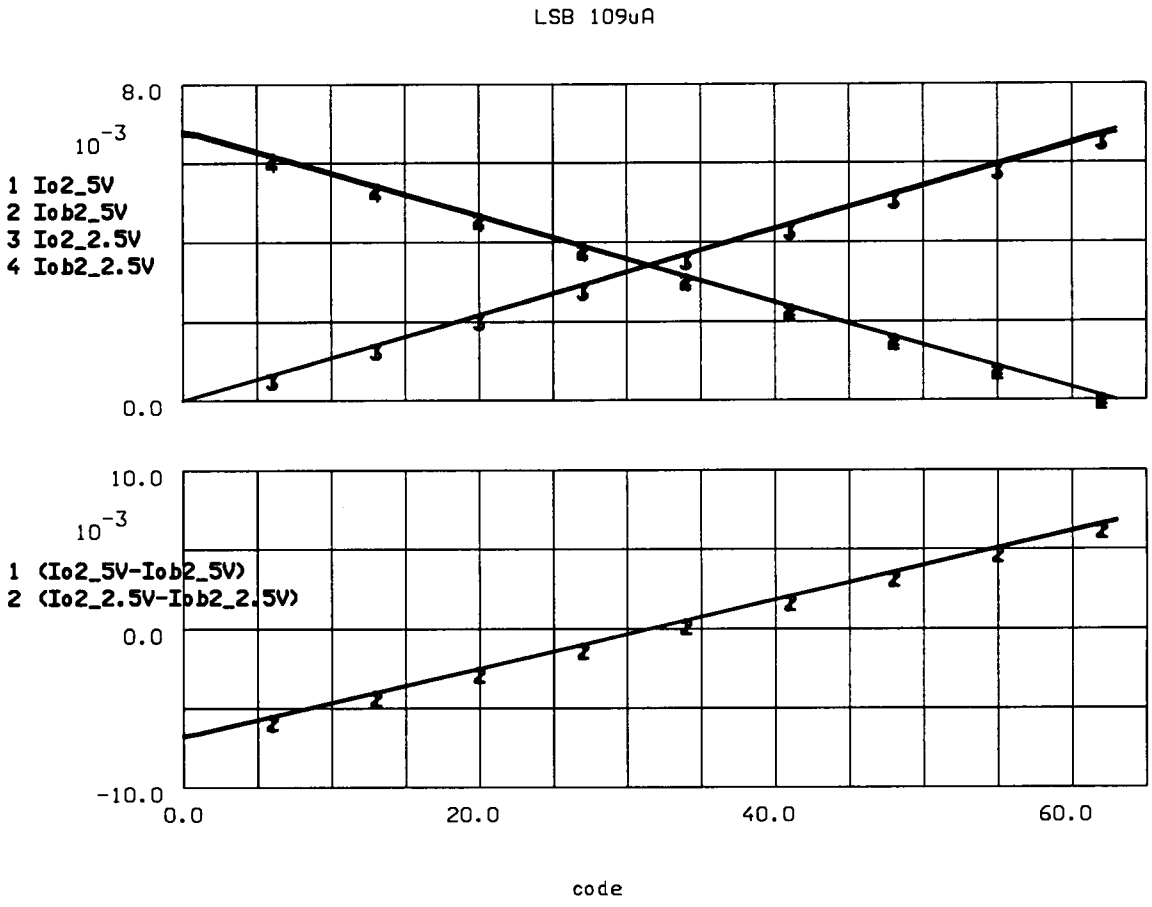

Figure 4.16: Transfer characteristics of DAC on Chip2 at $I_{LSB} = 109\ \mu A$, $V_{out} = 2.5, 5V$

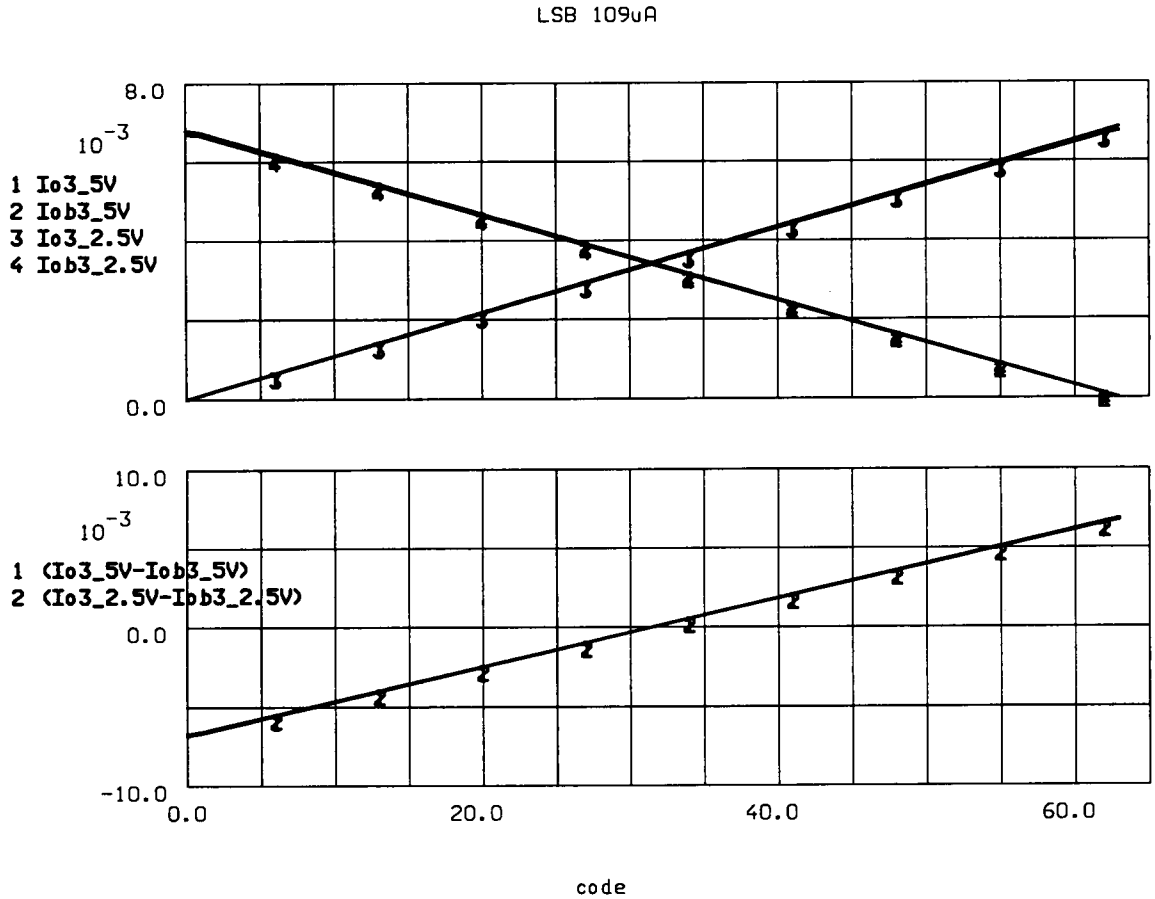

Figure 4.17: Transfer characteristics of DAC on Chip3 at $I_{LSB} = 109\ \mu A$, $V_{out} = 2.5, 5V$

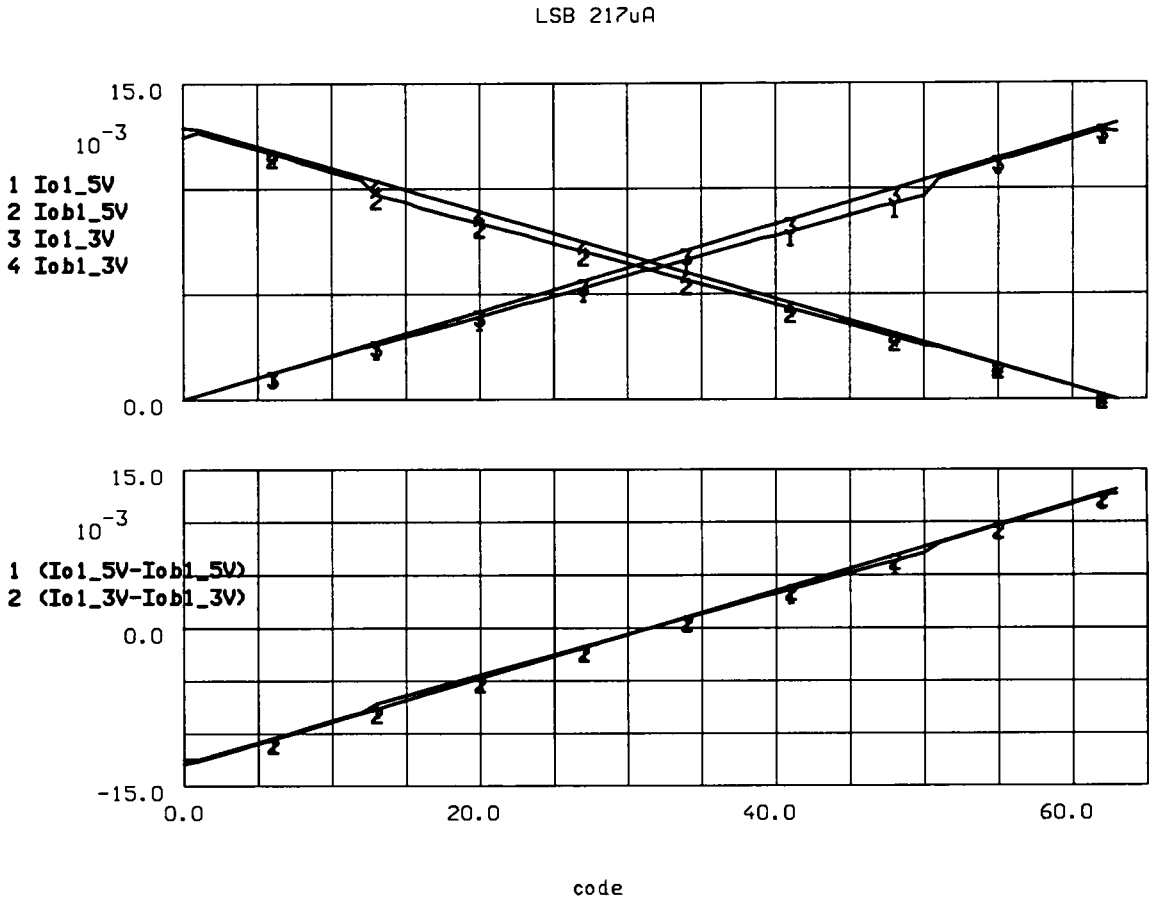

Figure 4.18: Transfer characteristics of DAC on Chip1 at $I_{LSB} = 217\ \mu A$, $V_{out} = 3,5V$

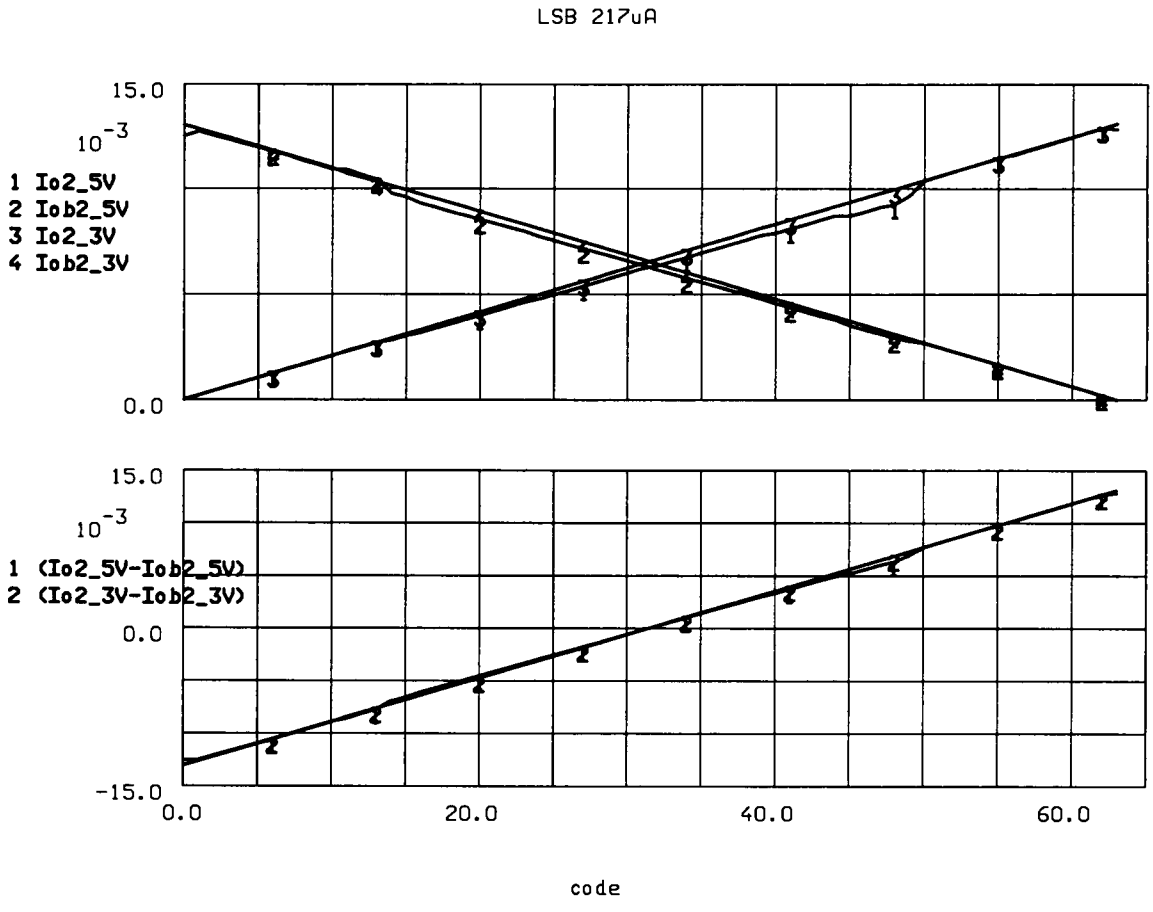

Figure 4.19: Transfer characteristics of DAC on Chip2 at $I_{LSB} = 217\ \mu A$, $V_{out} = 3,5V$

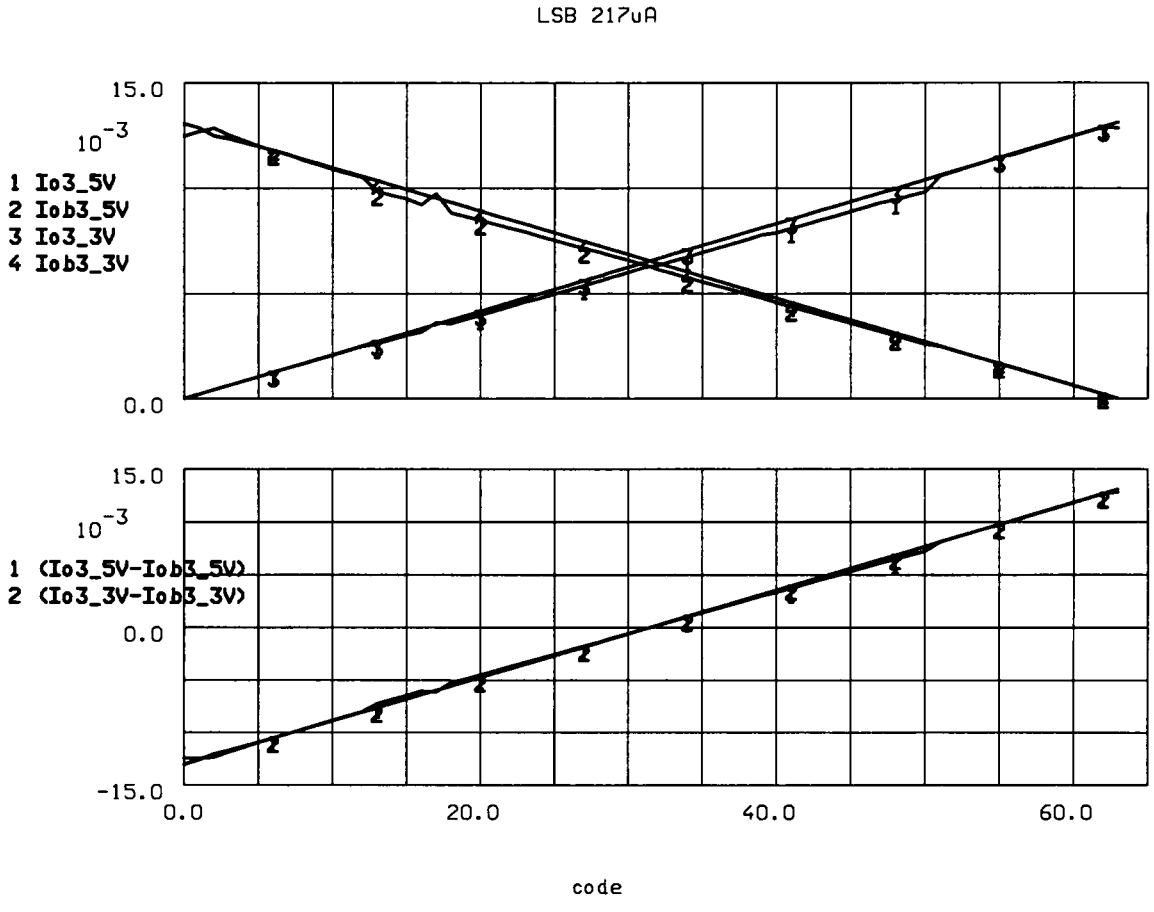

Figure 4.20: Transfer characteristics of DAC on Chip3 at $I_{LSB} = 217\ \mu A$, $V_{out} = 3,5V$

4.5 Differential Non-Linearity

Differential Non-Linearity (DNL) is a measure of the maximum deviation of actual step size from the ideal 1LSB. The measured DNL of each DAC for four different combinations of reference currents and output voltages are described here. A DNL better than ±1LSB will guarantee monotonicity.

Figures 4.21, 4.22, and 4.23 give the DNL of I_{out}, $\overline{I_{out}}$, and $(I_{out} - \overline{I_{out}})$ for Chip1, Chip2, and Chip3 respectively, when the input current is 1 μA and the output voltage is 1 V. As shown in these plots, the DNL of the DACs at this measured point is much larger than ±1LSB. This means that the DACs are not monotonic at this measured point. The best curves among these measurements are the DNL of $(I_{out} - \overline{I_{out}})$, which is about ±4.5LSB. As shown in Figures 4.24, 4.25, and 4.26, the DNL measurements of the DACs are not any better for $V_{out} = 5$ V.

The DNL of the DACs for $I_{ref} = 28$ μA at both output voltages of 1.5 and 5 V, are a lot better than the results for the 1 μA input current. Figures 4.27, 4.28, and 4.29 give the DNL of the DACs at $I_{ref} = 28$ μA and $V_{out} = 1.5$ V. Figures 4.30, 4.31, and 4.32 give the DNL results at I_{ref}=28 μA and $V_{out} = 5$ V. The worst case DNL at both output voltages of the I_{out} among all three chips is +0.247LSB and −0.335LSB. The DNL of $\overline{I_{out}}$ is +0.279LSB and −0.282LSB. DNL for $(I_{out} - \overline{I_{out}})$ is between +0.134LSB and −0.162LSB. The over all worst case DNL at 28 μA is ±0.335LSB, which confirms the theoretical prediction of ±0.363LSB.

The DNL of the DACs for 109 μA current was much better than the results of 28 μA input current with the exception of the spikes that were seen at the full

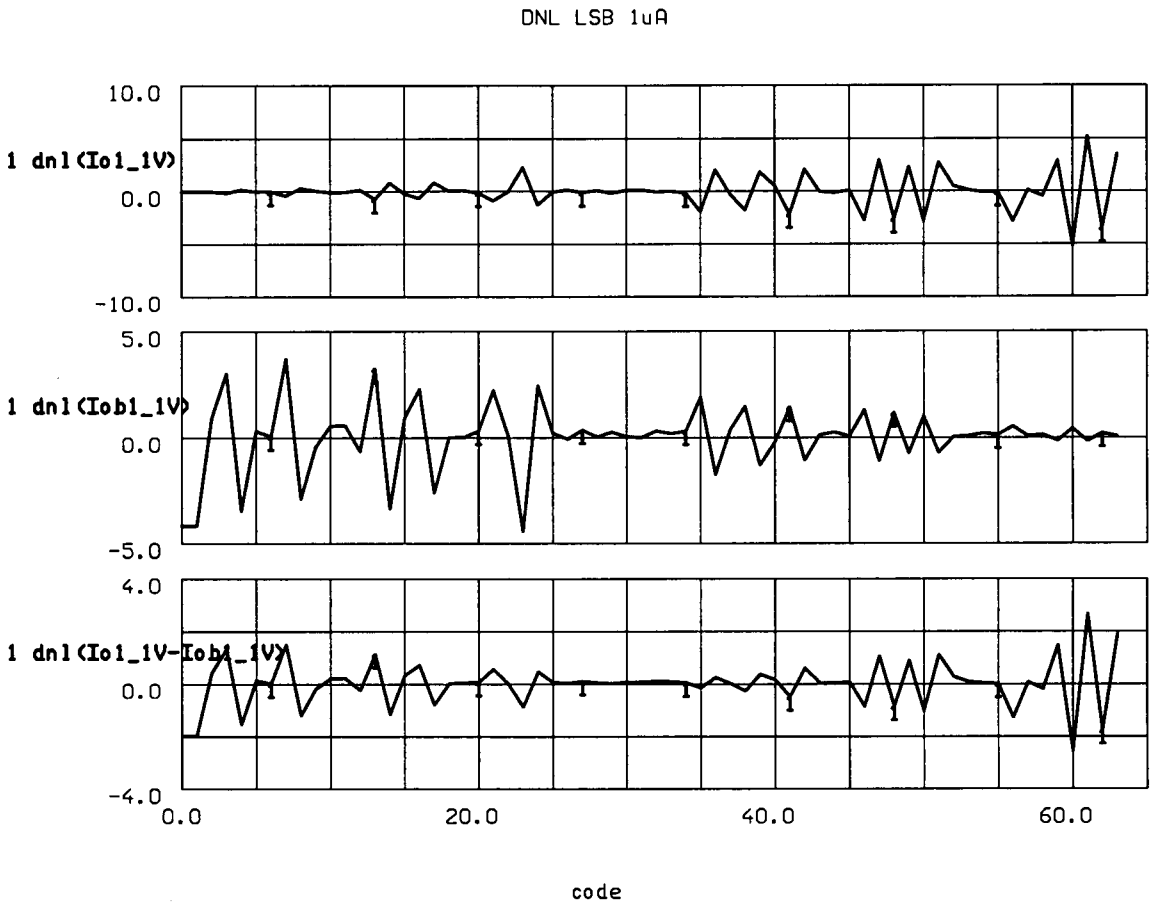

Figure 4.21: Differential non-linearity of DAC on Chip1 at $I_{LSB} = 1\ \mu A$, $V_{out} = 1V$

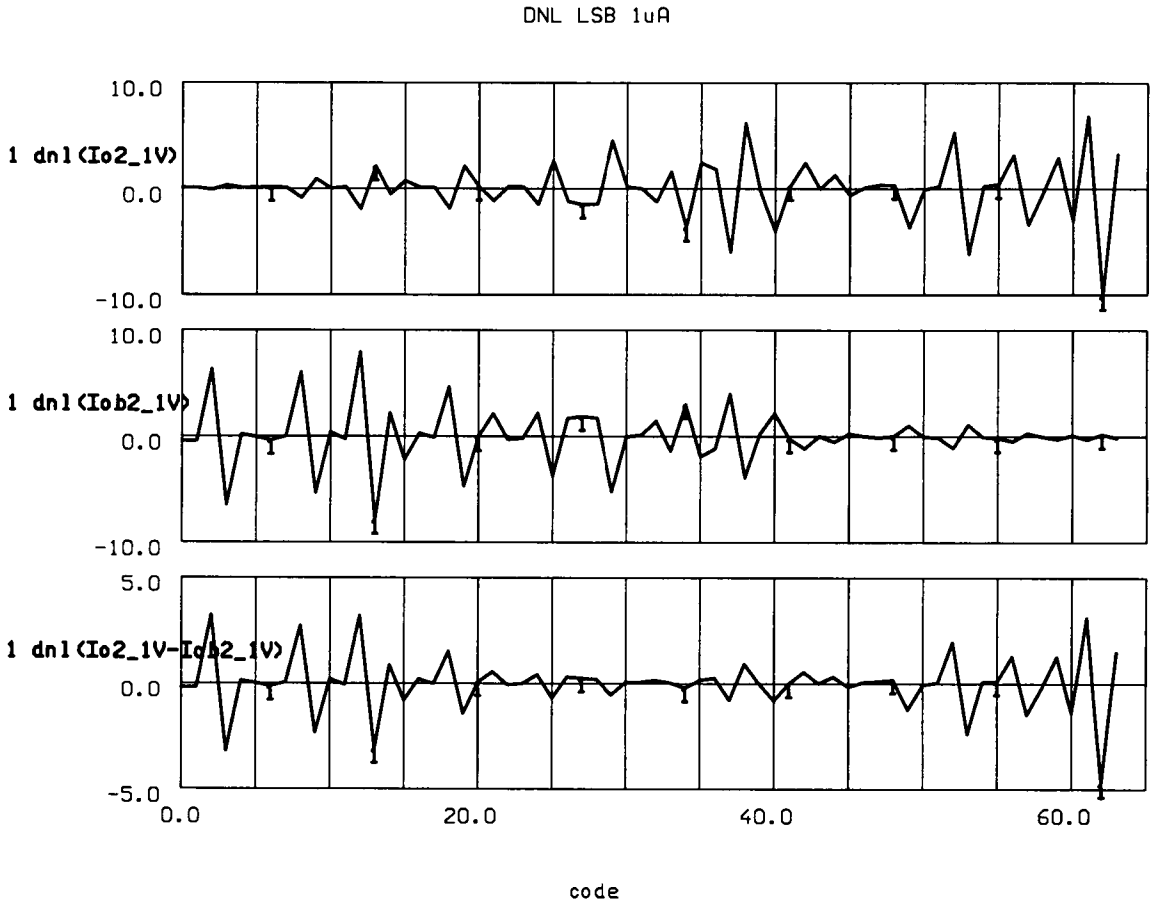

Figure 4.22: Differential non-linearity of DAC on Chip2 at $I_{LSB} = 1\ \mu A$, $V_{out} = 1V$

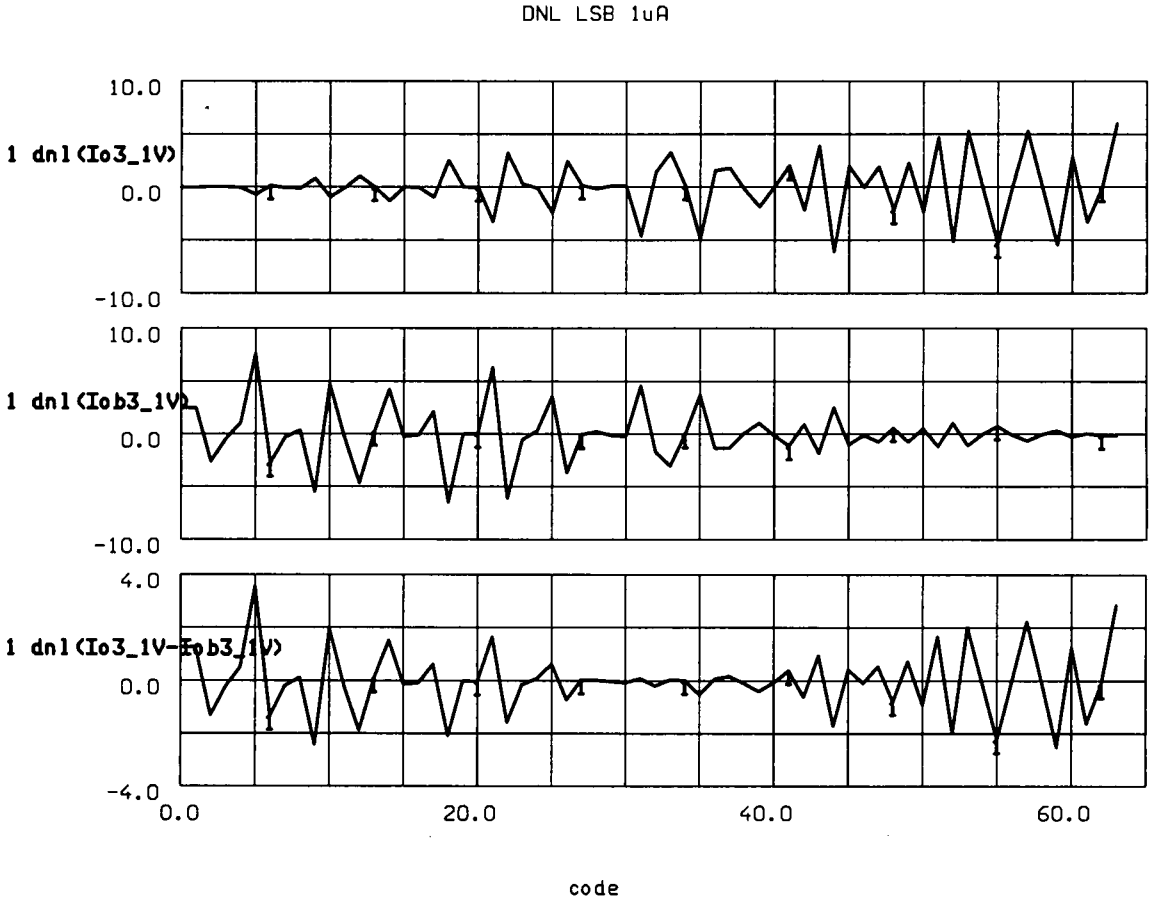

Figure 4.23: Differential non-linearity of DAC on Chip3 at $I_{LSB} = 1\ \mu A$, $V_{out} = 1V$

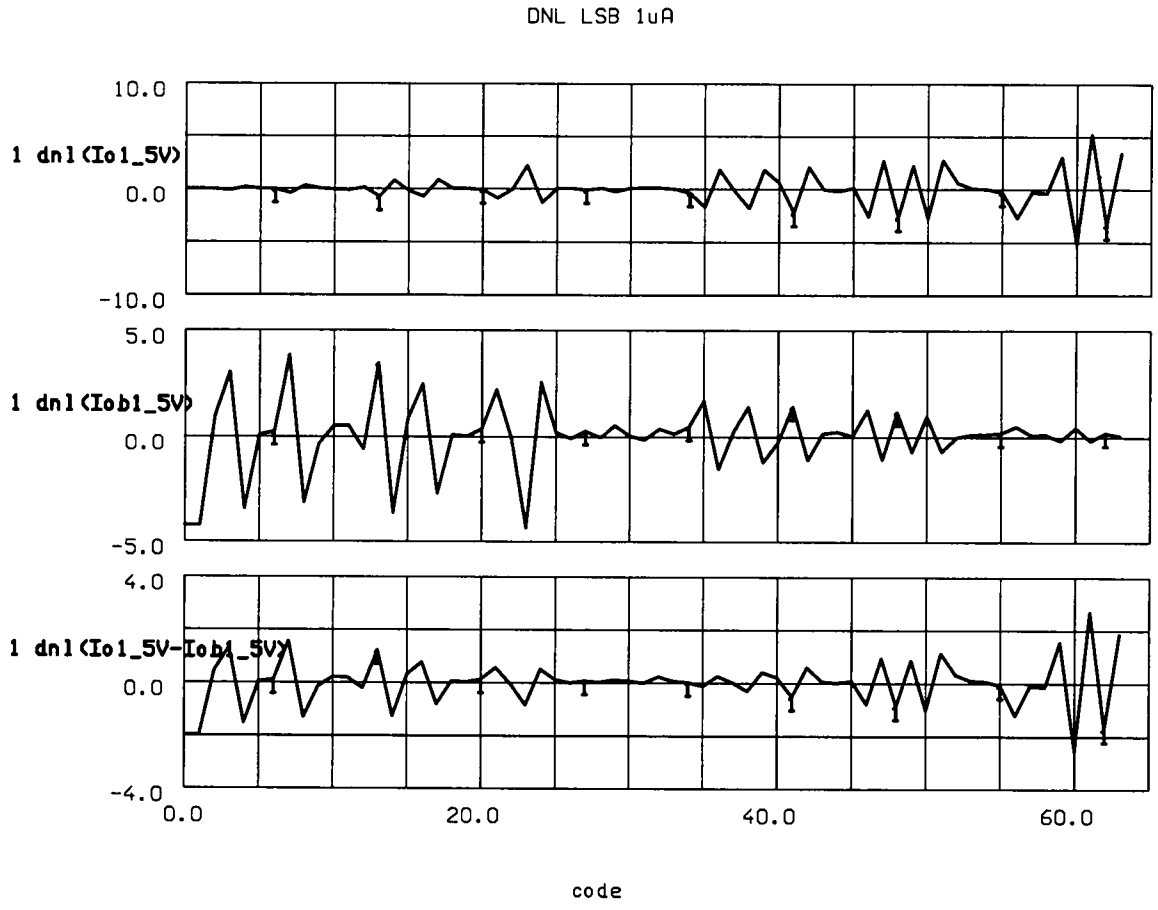

Figure 4.24: Differential non-linearity of DAC on Chip1 at $I_{LSB} = 1\ \mu A$, $V_{out} = 5V$

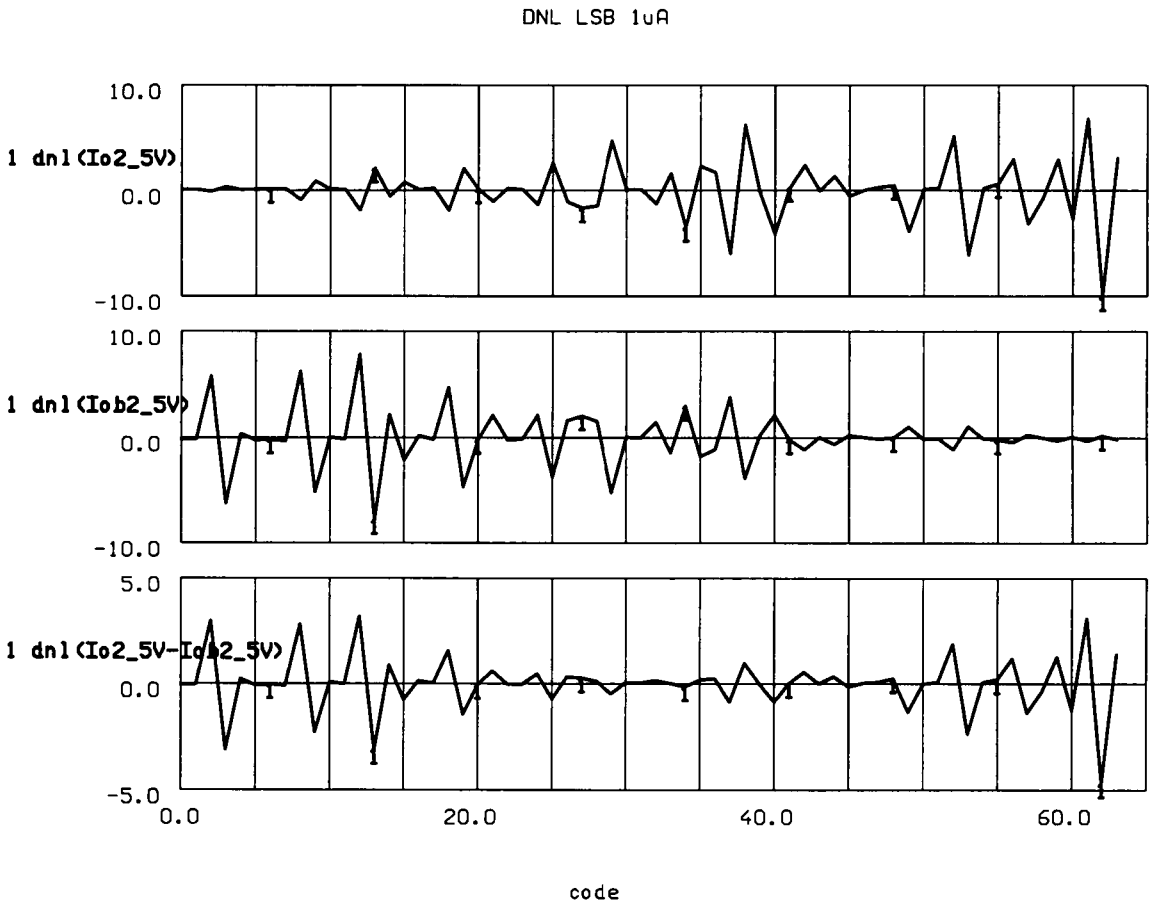

Figure 4.25: Differential non-linearity of DAC on Chip2 at $I_{LSB} = 1\ \mu A$, $V_{out} = 5V$

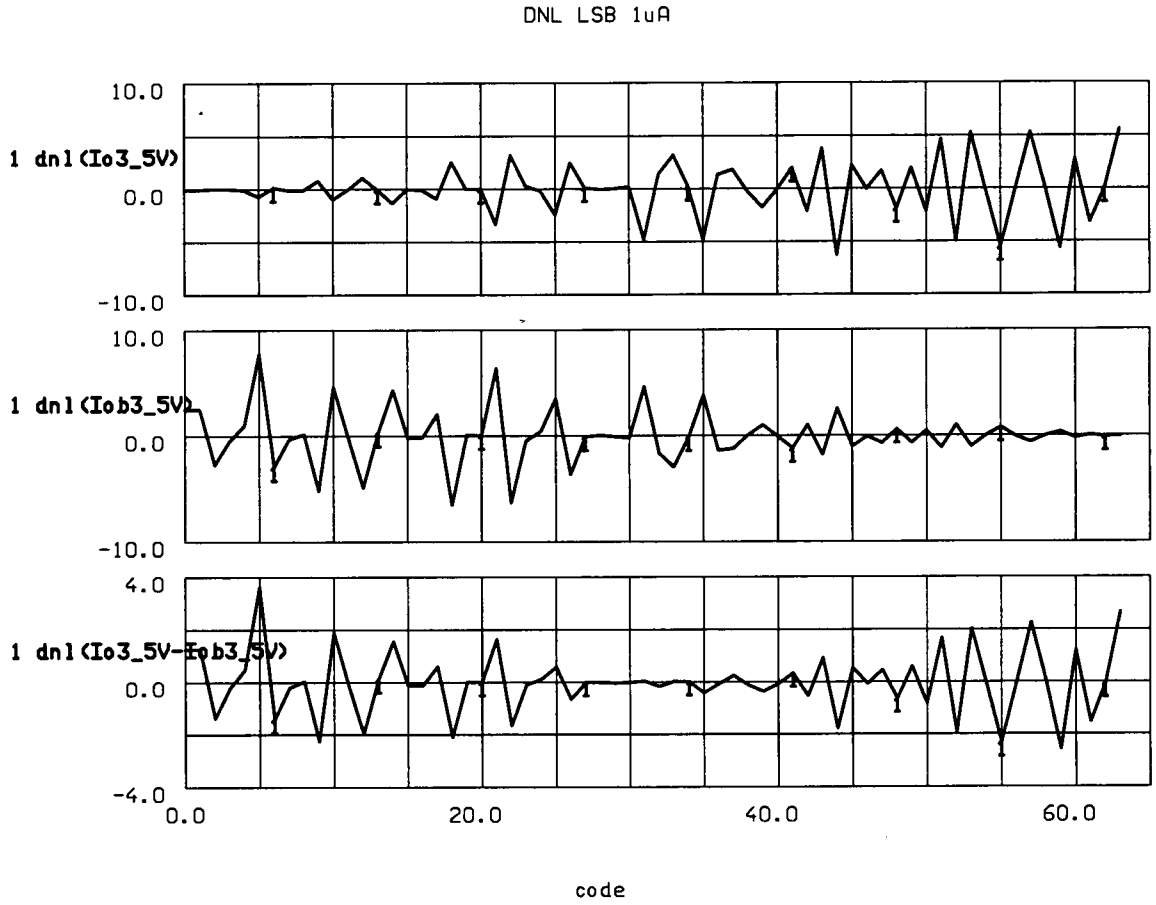

Figure 4.26: Differential non-linearity of DAC on Chip3 at $I_{LSB} = 1\ \mu A$, $V_{out} = 5V$

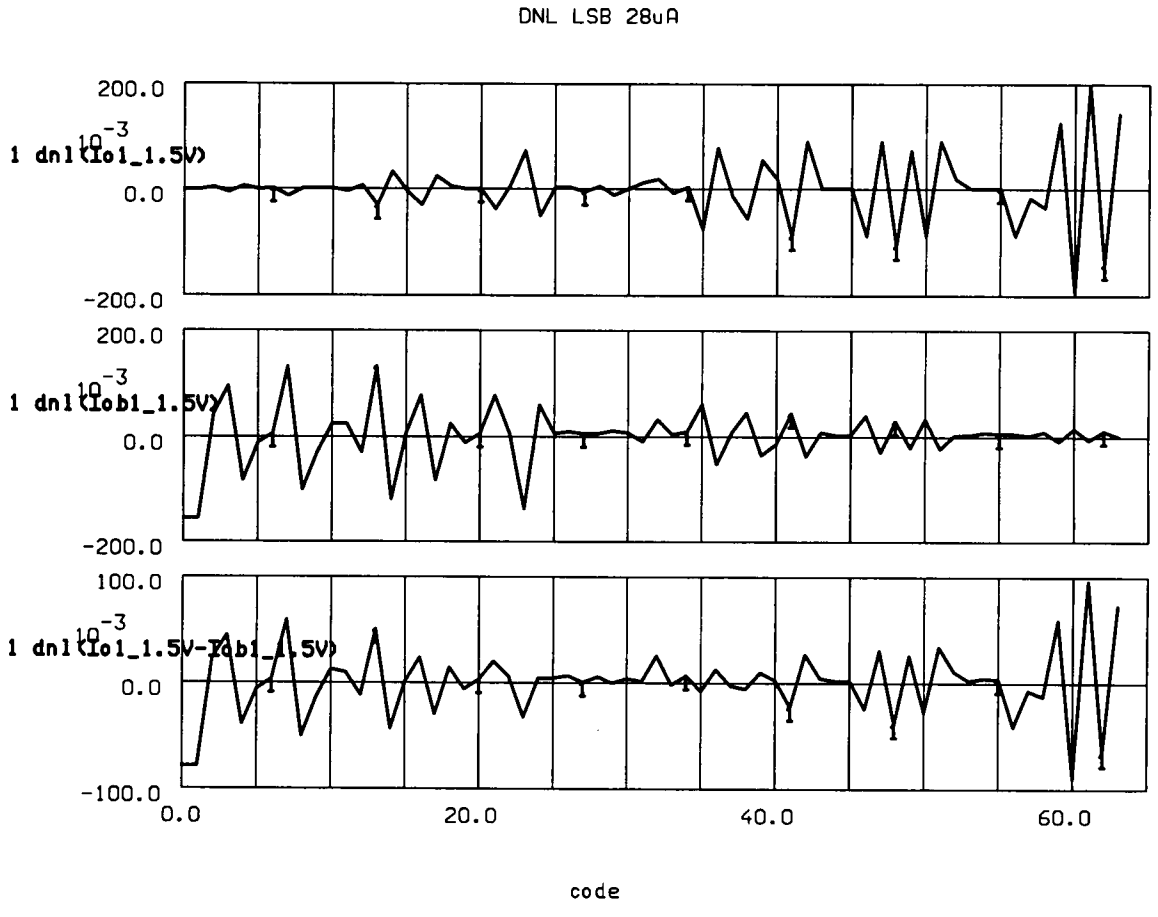

Figure 4.27: Differential non-linearity of DAC on Chip1 at $I_{LSB} = 28\ \mu A$, $V_{out} = 1.5V$

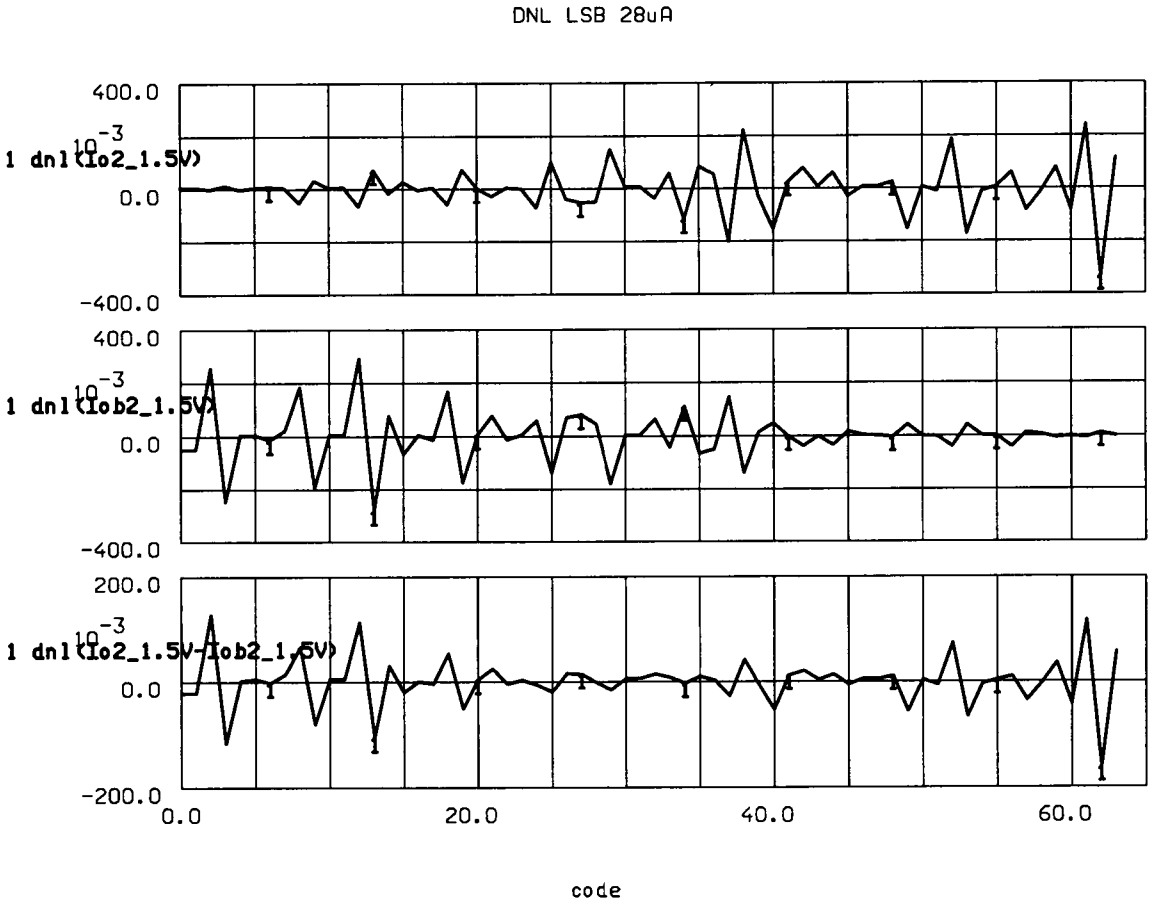

Figure 4.28: Differential non-linearity of DAC on Chip2 at $I_{LSB} = 28\ \mu A$, $V_{out} = 1.5V$

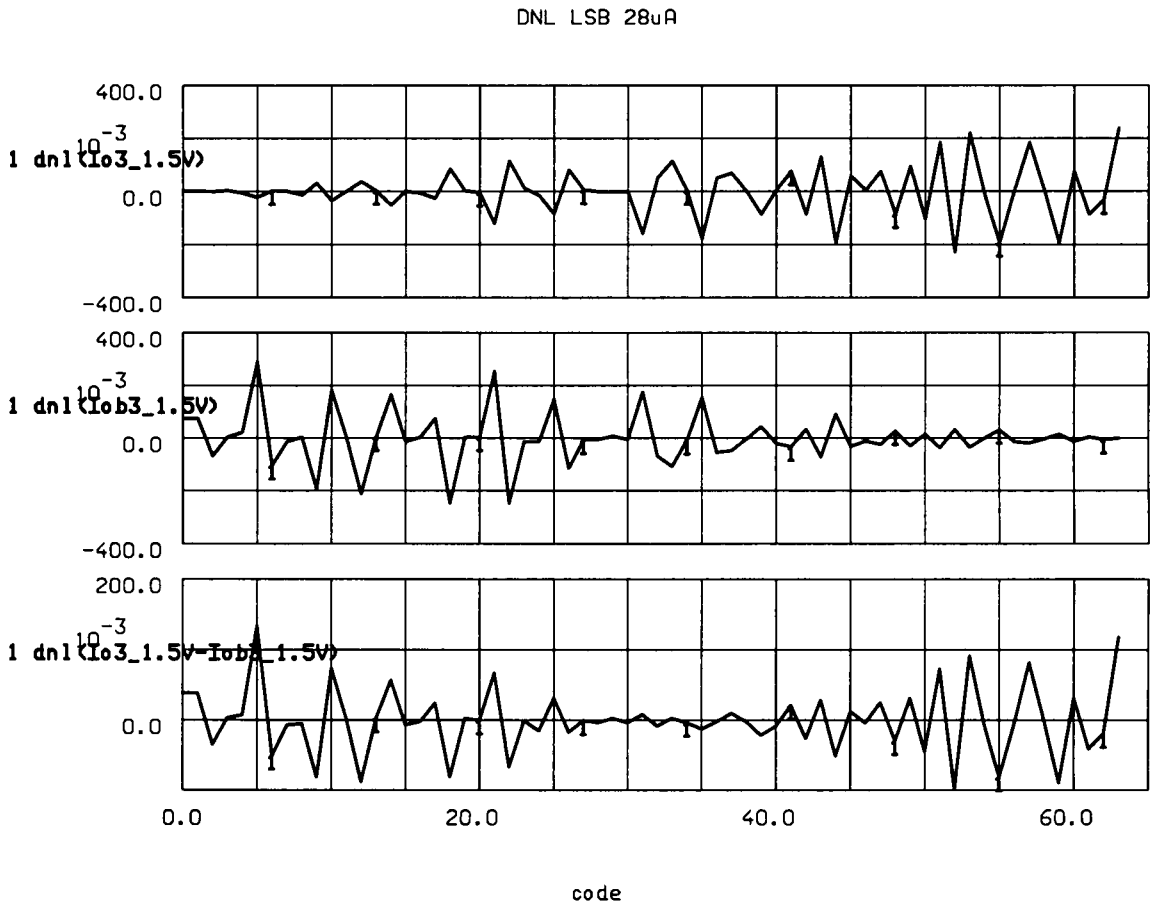

Figure 4.29: Differential non-linearity of DAC on Chip3 at $I_{LSB} = 28\ \mu A$, $V_{out} = 1.5V$

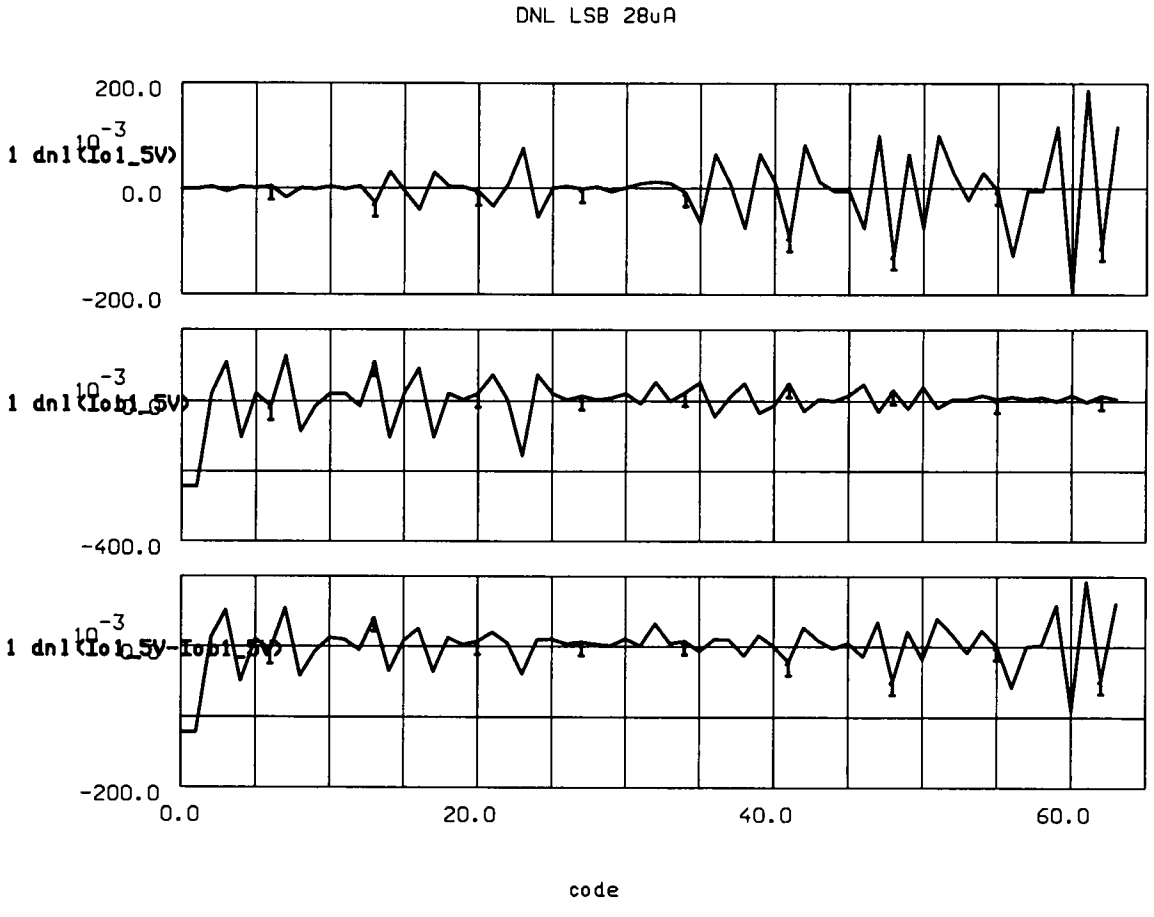

Figure 4.30: Differential non-linearity of DAC on Chip1 at $I_{LSB} = 28\ \mu A$, $V_{out} = 5V$

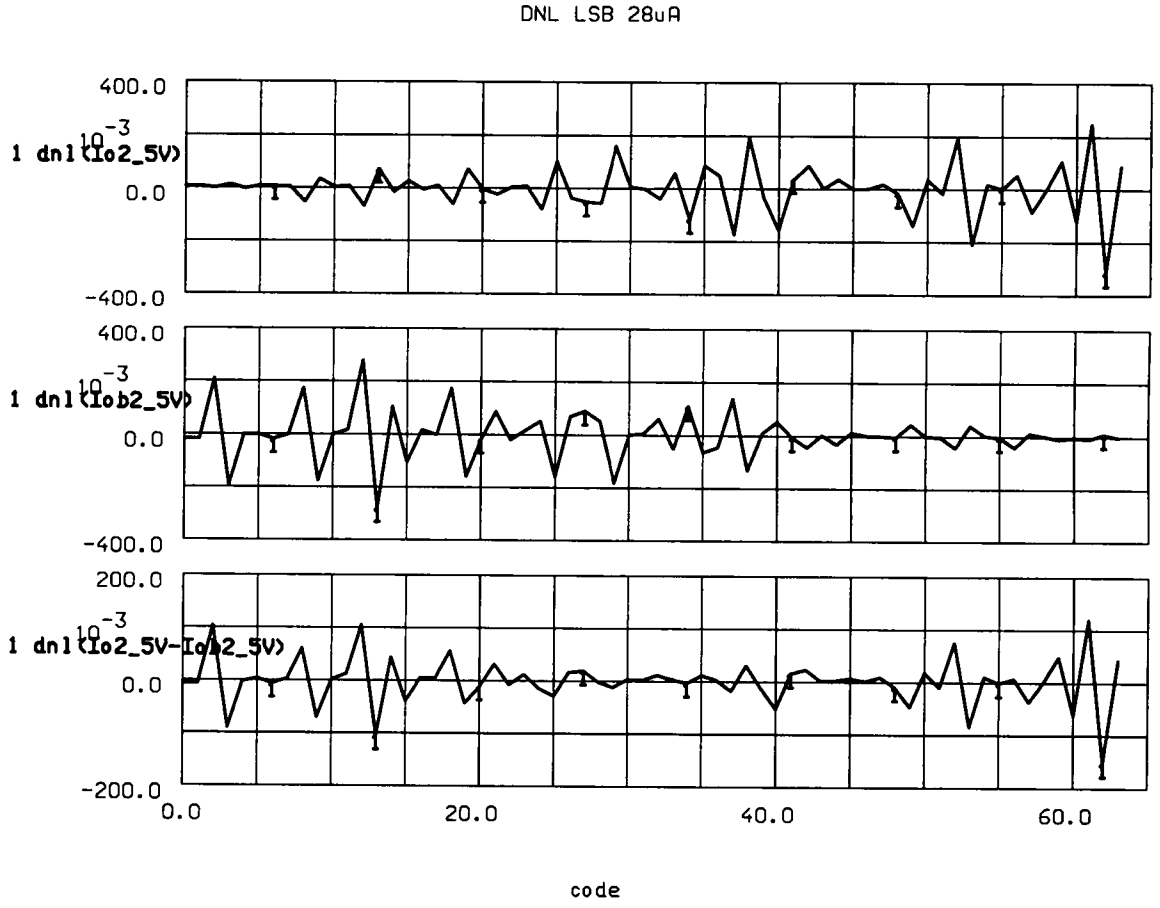

Figure 4.31: Differential non-linearity of DAC on Chip2 at $I_{LSB} = 28\ \mu A$, $V_{out} = 5V$

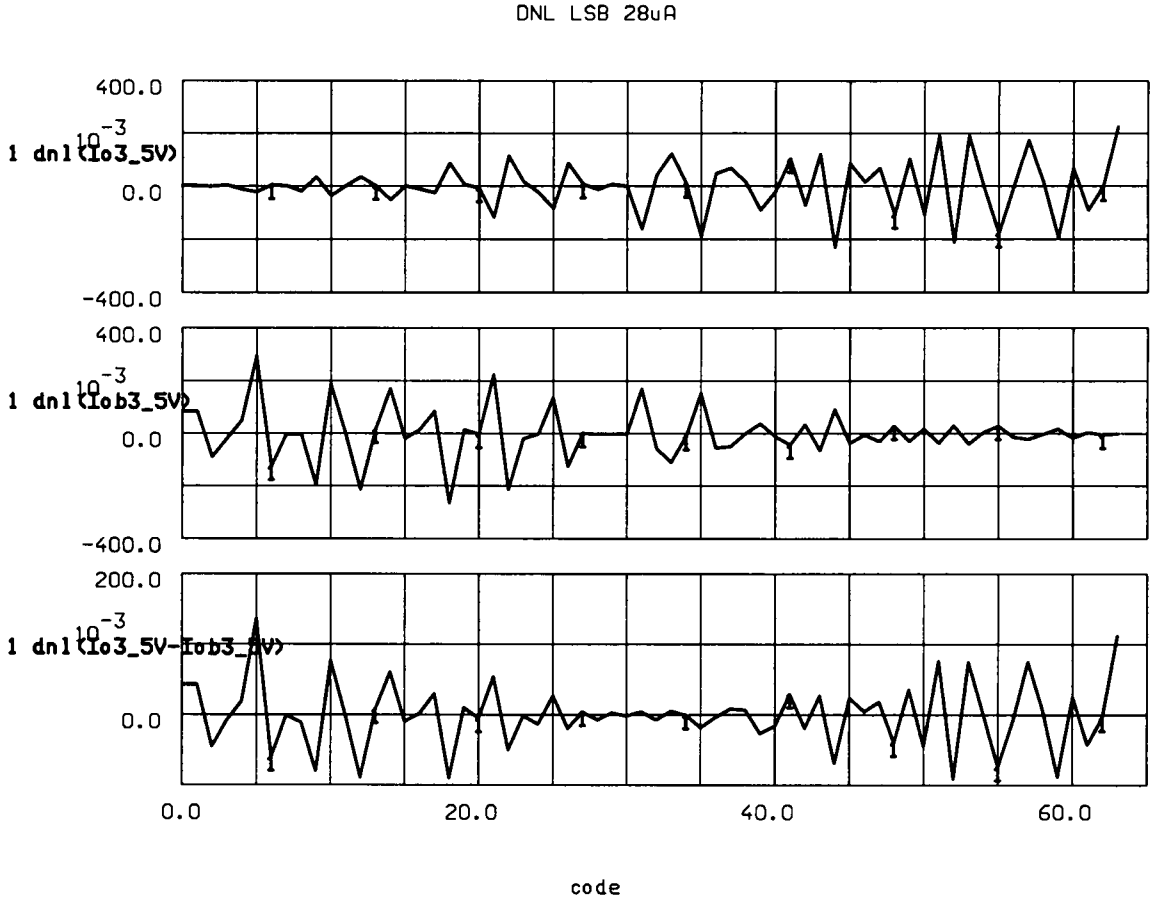

Figure 4.32: Differential non-linearity of DAC on Chip3 at $I_{LSB} = 28\ \mu A$, $V_{out} = 5V$

scale outputs. Figures 4.33 through 4.38, give the DNL of the DACs at $I_{ref} = 109$ μA for both output voltages of 2.5 and 5 V. The maximum DNL of the I_{out} is +0.067LSB and −0.561LSB. The DNL of $\overline{I_{out}}$ is +0.107LSB and −1.123LSB. DNL for $(I_{out} - \overline{I_{out}})$ is between +0.055LSB and −0.551LSB.

The DNL of the DACs at 217 μA input current was more than ±1LSB at high output voltage of 5 V, as shown in Figures 4.39, 4.40, and 4.41. But the DNL was less than ±1LSB for the lower V_{out} value of 3 V, as shown in Figures 4.42, 4.43, and 4.44. range of 1 to 271 μA at output voltages of 1.5, 3, and 5 V, I_{out} versus I_{ref} for Chip1, Chip2, and Chip3. The second set I_{ref}. And the bottom set of curves show the maximum DNL of To summarize, it is evident that the current DAC has DNL of ±1LSB at currents ranged between 28 and 109 μA. Even at higher currents than the $I_{out(max.)}$ range; as long as the output voltages are lower the DAC will have less than ±1LSB DNL.

4.6 Integral Non-Linearity

Integral Non-Linearity (INL) is a measure of the straightness of a DAC's transfer function. This is the measure of how far the points deviate from a reference straight line drawn through them as a group. For measuring the INL of the DAC, the best-fit straight line technique was chosen. The measured INL of each DAC for four different reference currents are reported. The INL values were obtained by determining the output current for each sequential input.

Figures 4.45, 4.46, and 4.47 give the INL of I_{out}, $\overline{I_{out}}$, and $(I_{out} - \overline{I_{out}})$ for

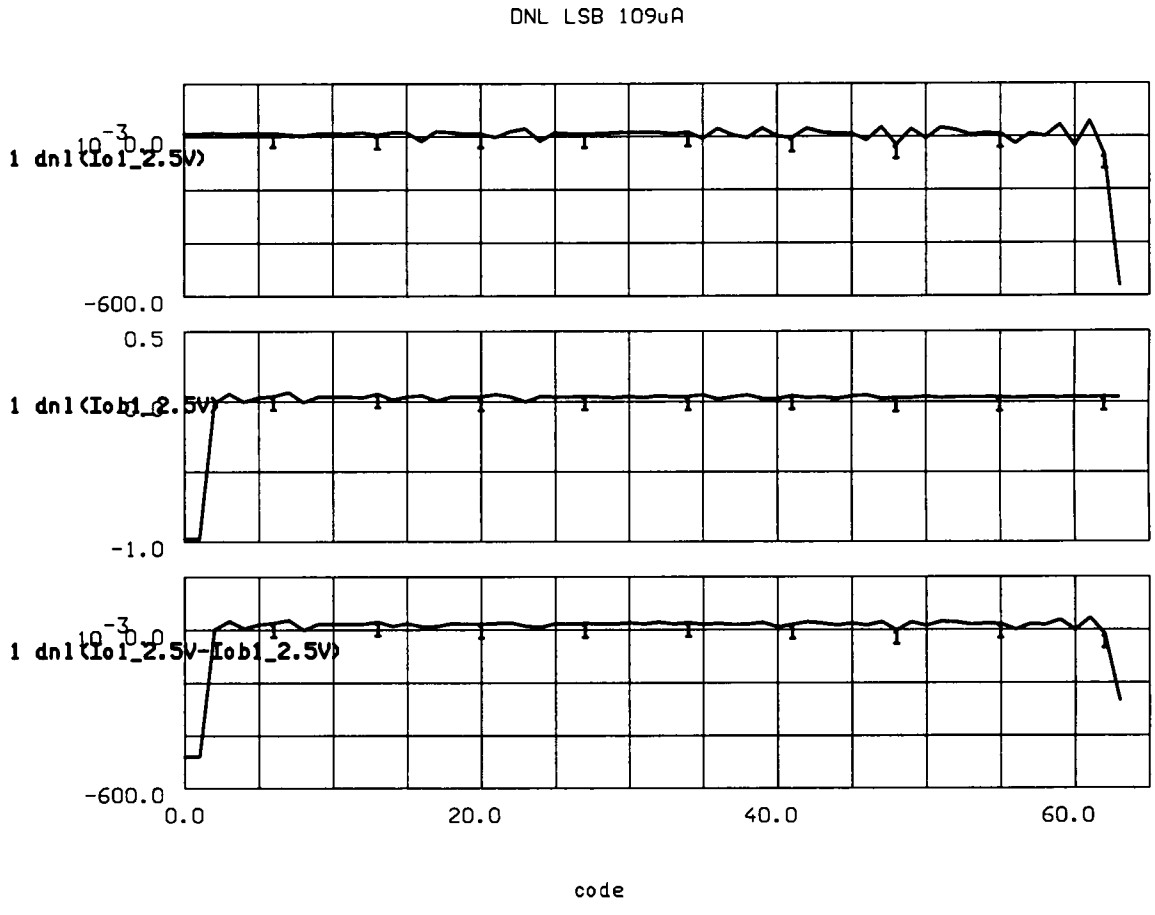

Figure 4.33: Differential non-linearity of DAC on Chip1 at $I_{LSB} = 109\ \mu A$, $V_{out} = 2.5V$

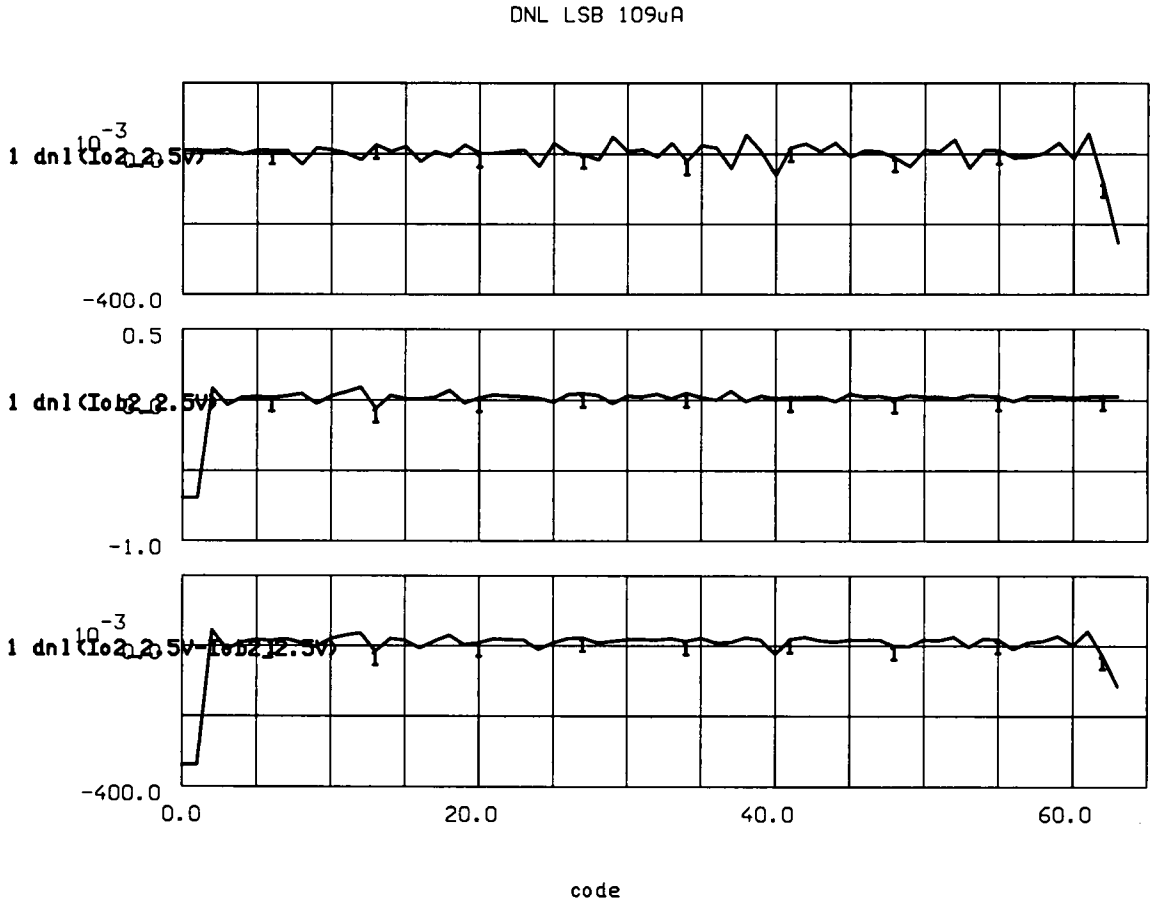

Figure 4.34: Differential non-linearity of DAC on Chip2 at $I_{LSB} = 109\ \mu A$, $V_{out} = 2.5V$

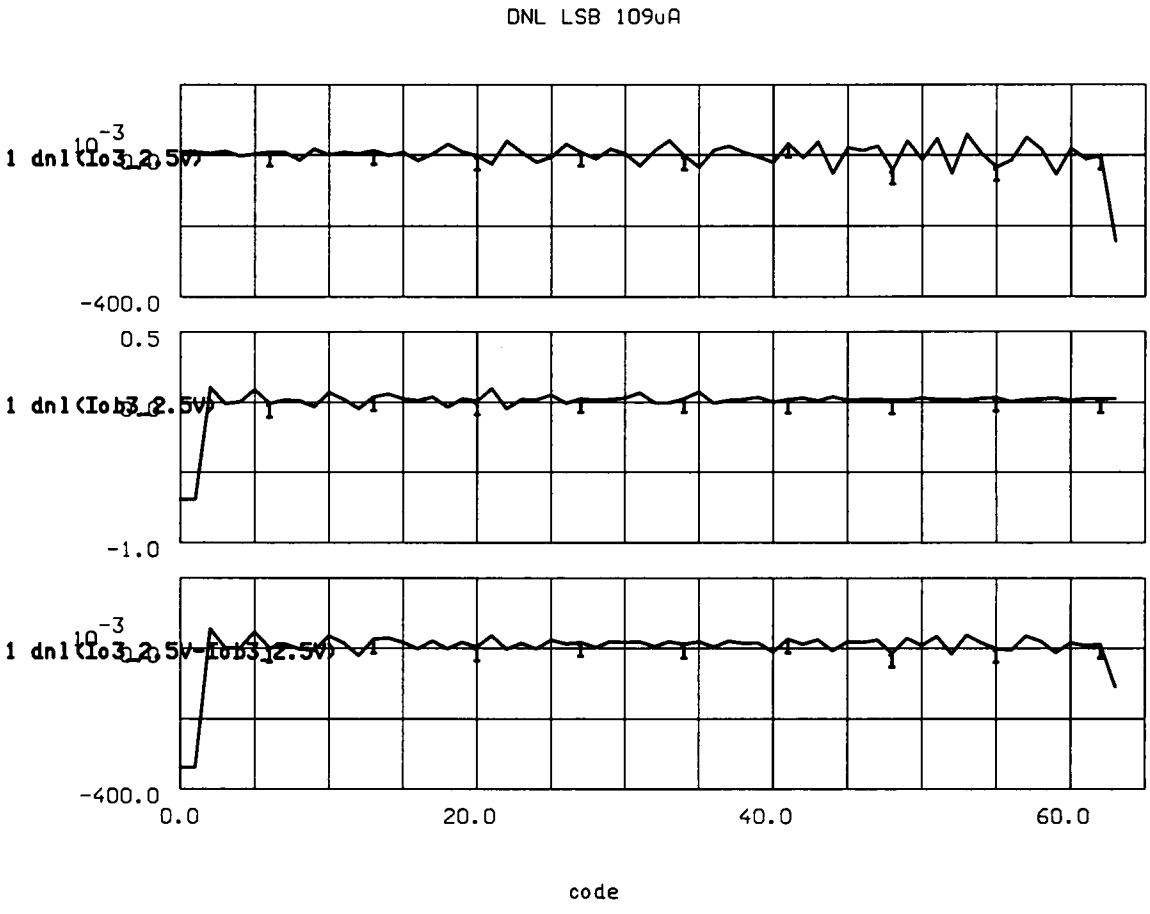

Figure 4.35: Differential non-linearity of DAC on Chip3 at $I_{LSB} = 109\ \mu A$, $V_{out} = 2.5V$

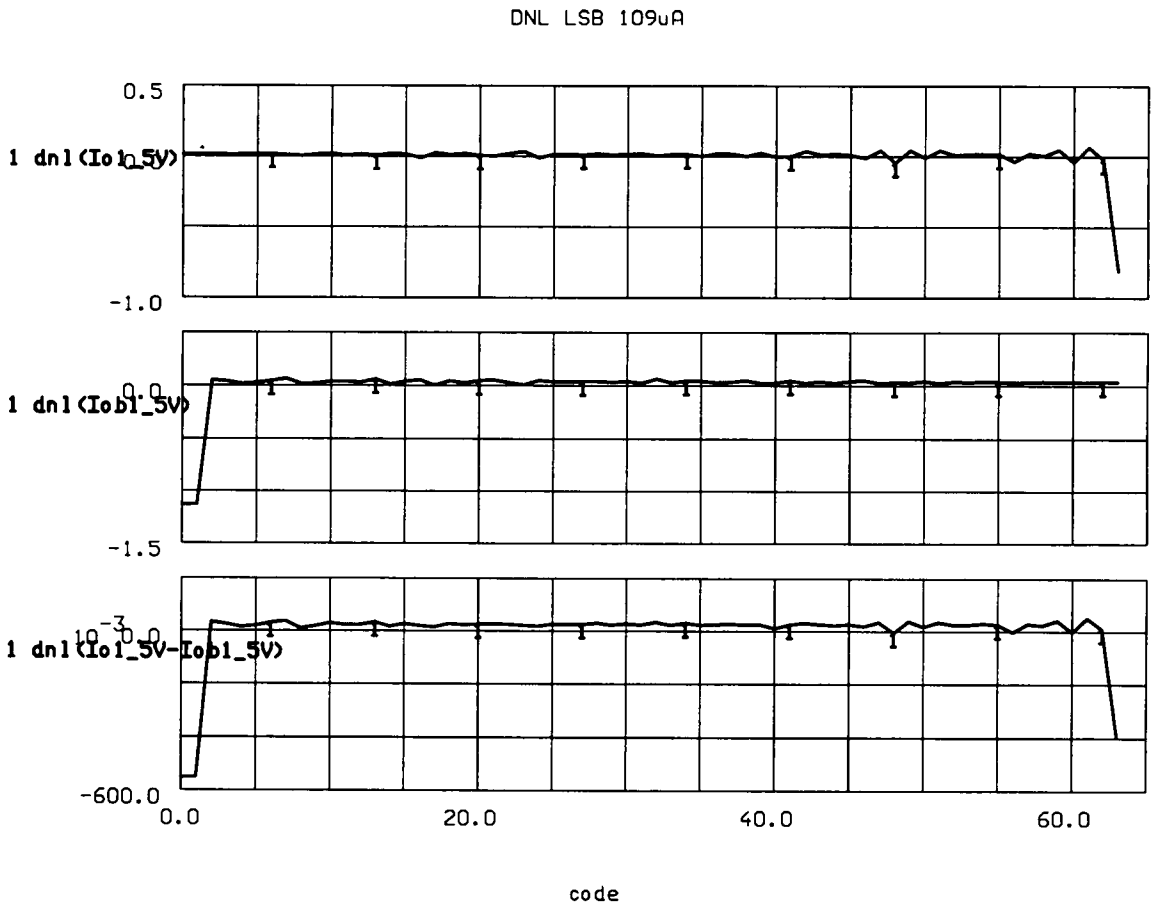

Figure 4.36: Differential non-linearity of DAC on Chip1 at $I_{LSB} = 109\ \mu A$, $V_{out} = 5V$

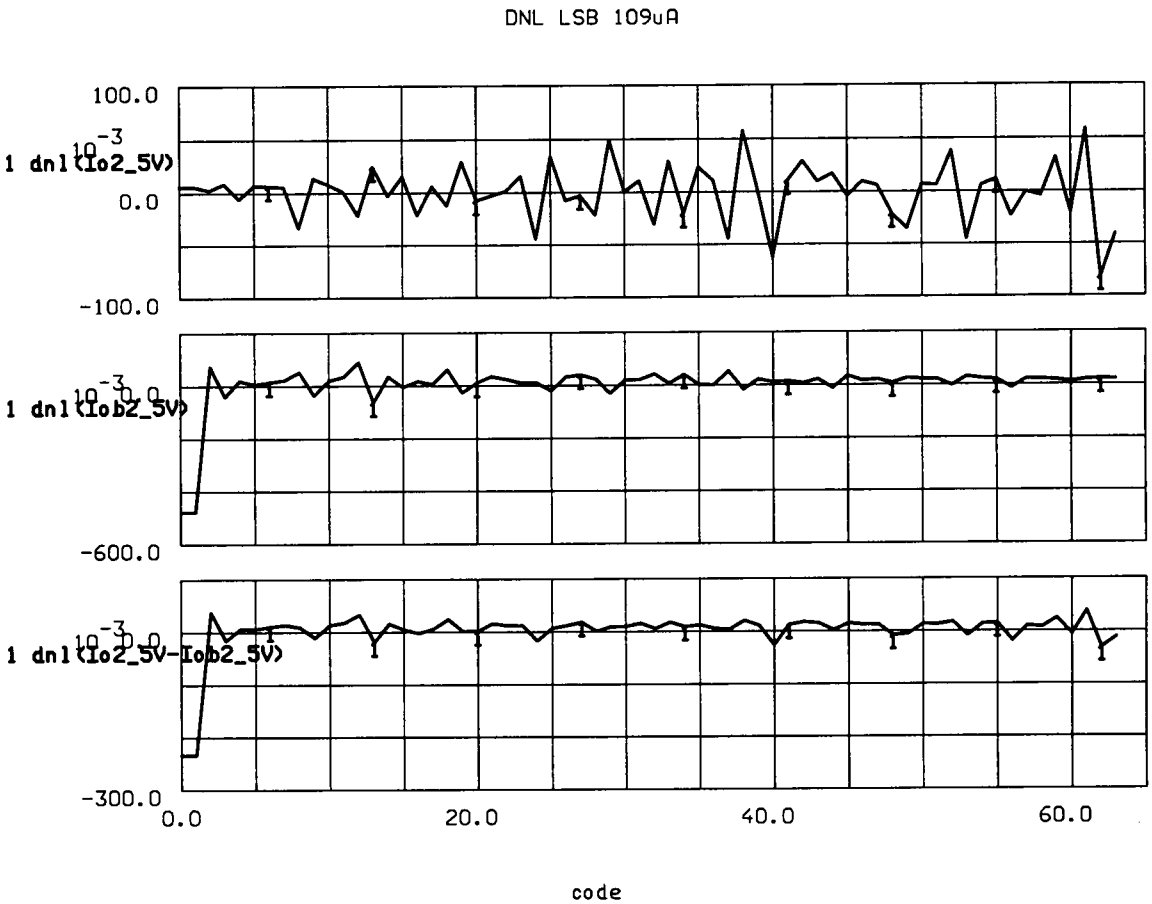

Figure 4.37: Differential non-linearity of DAC on Chip2 at $I_{LSB} = 109\ \mu A$, $V_{out} = 5V$

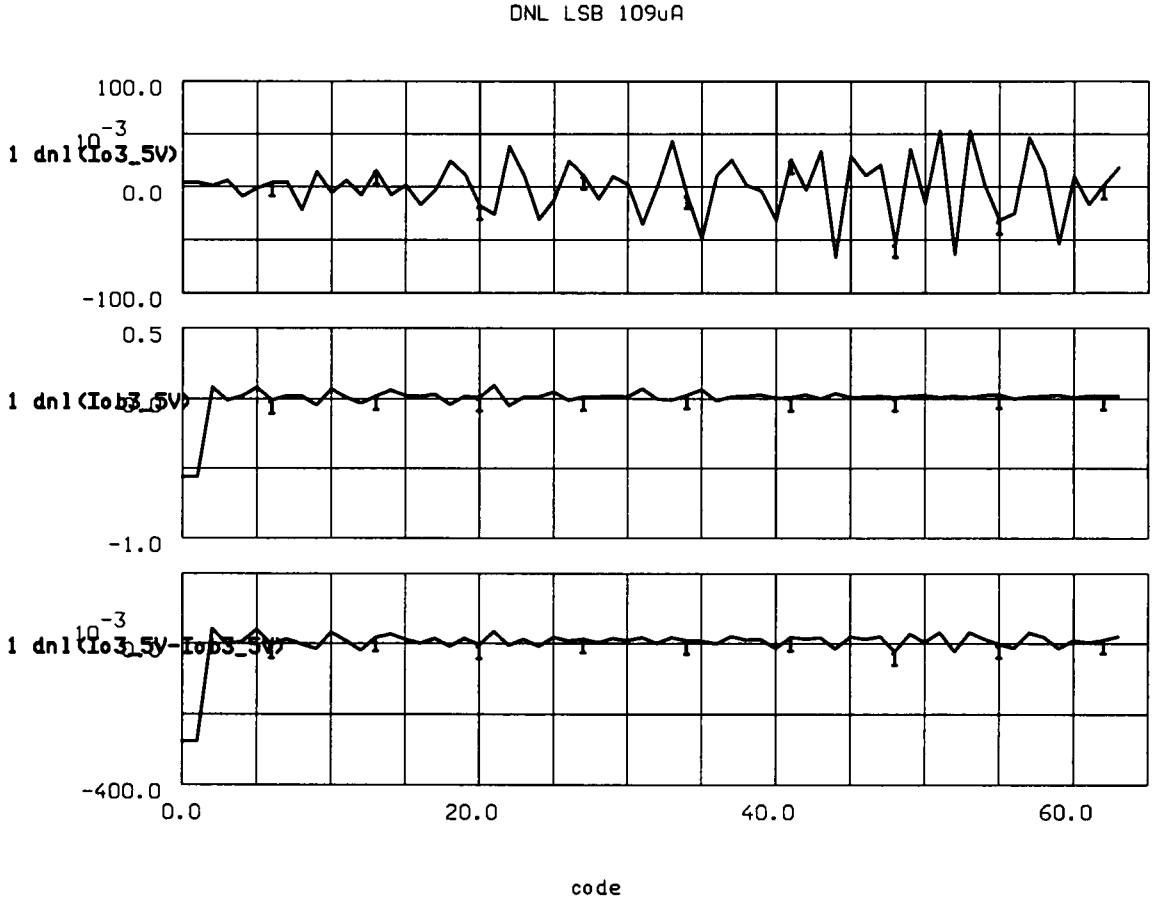

Figure 4.38: Differential non-linearity of DAC on Chip3 at $I_{LSB} = 109\ \mu A$, $V_{out} = 5V$

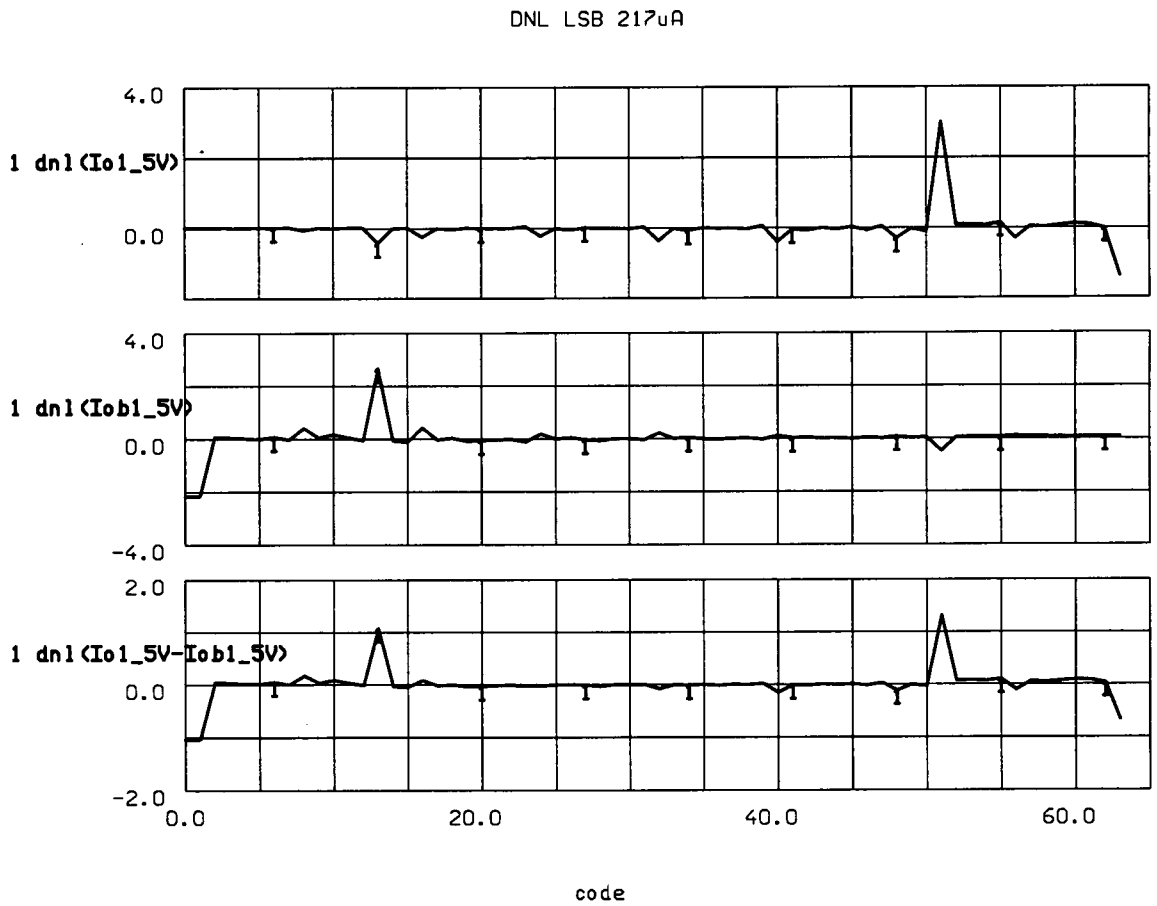

Figure 4.39: Differential non-linearity of DAC on Chip1 at $I_{LSB} = 217\ \mu A$, $V_{out} = 5V$

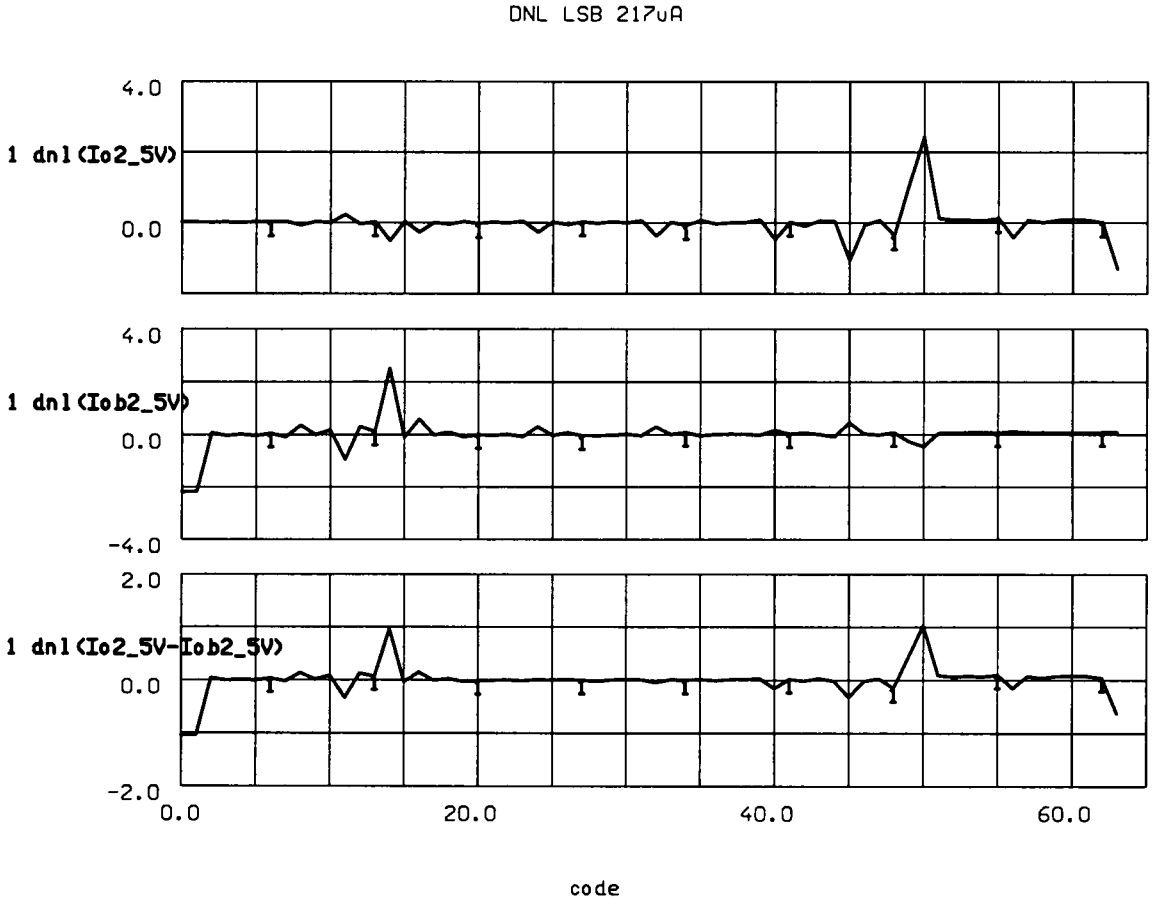

Figure 4.40: Differential non-linearity of DAC on Chip2 at $I_{LSB} = 217\ \mu A$, $V_{out} = 5V$

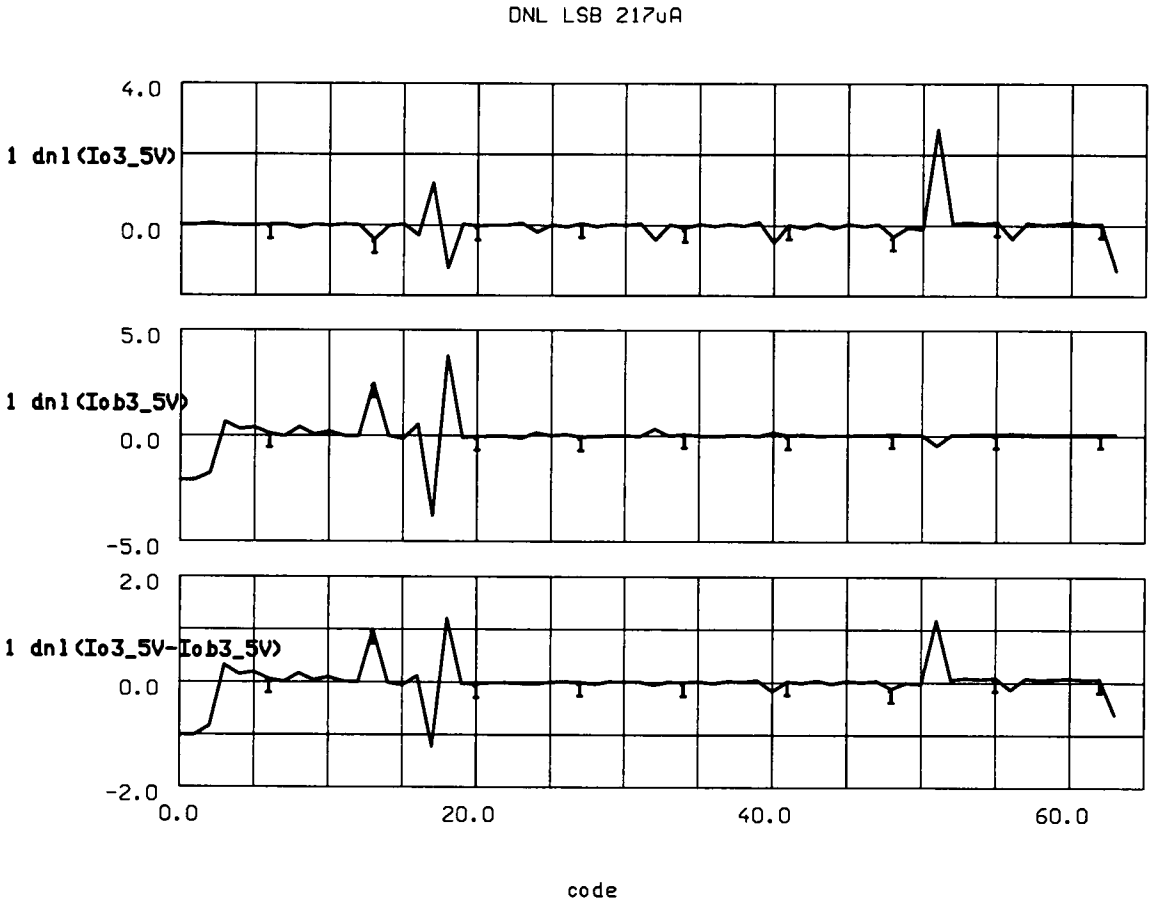

Figure 4.41: Differential non-linearity of DAC on Chip3 at $I_{LSB} = 217\ \mu A$, $V_{out} = 5V$

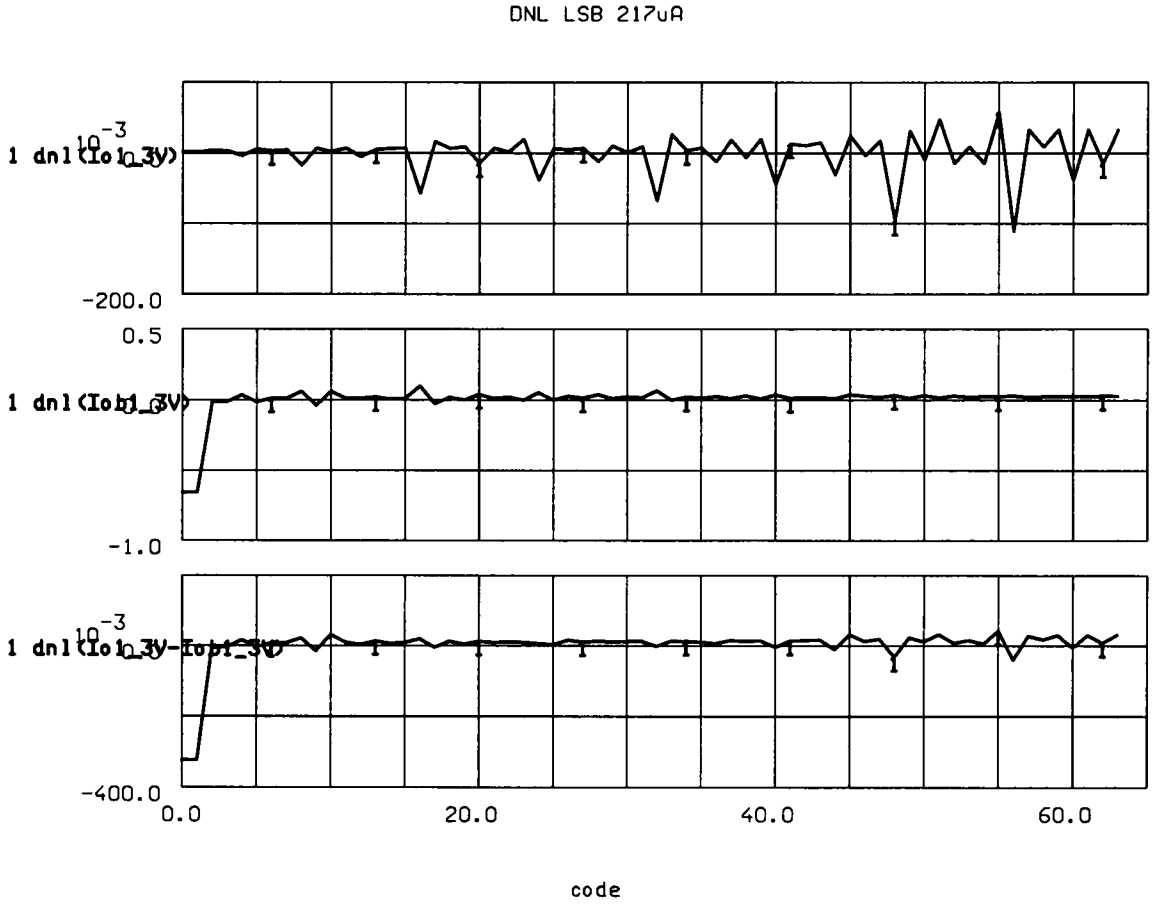

Figure 4.42: Differential non-linearity of DAC on Chip1 at $I_{LSB} = 217\ \mu A$, $V_{out} = 3V$

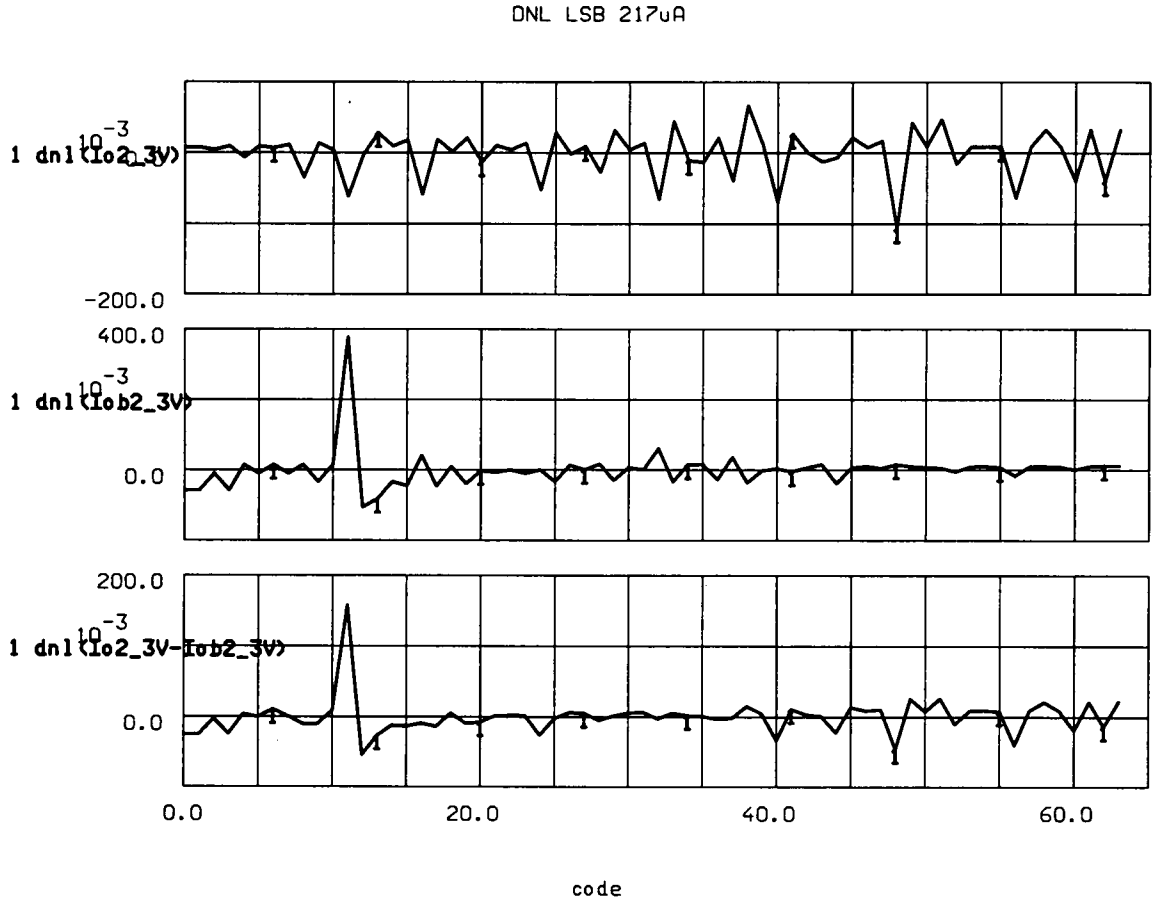

Figure 4.43: Differential non-linearity of DAC on Chip2 at $I_{LSB} = 217\ \mu A$, $V_{out} = 3V$

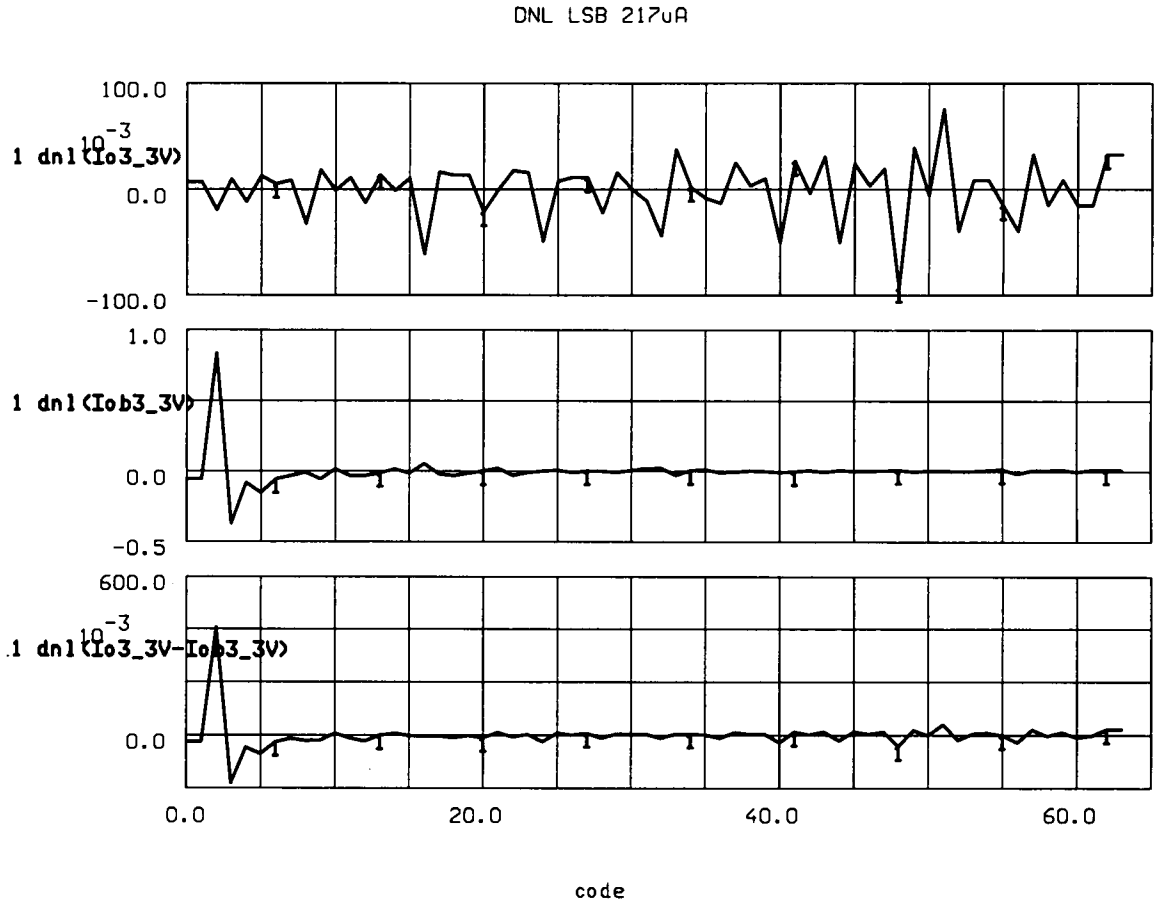

Figure 4.44: Differential non-linearity of DAC on Chip3 at $I_{LSB} = 217\ \mu A$, $V_{out} = 3V$

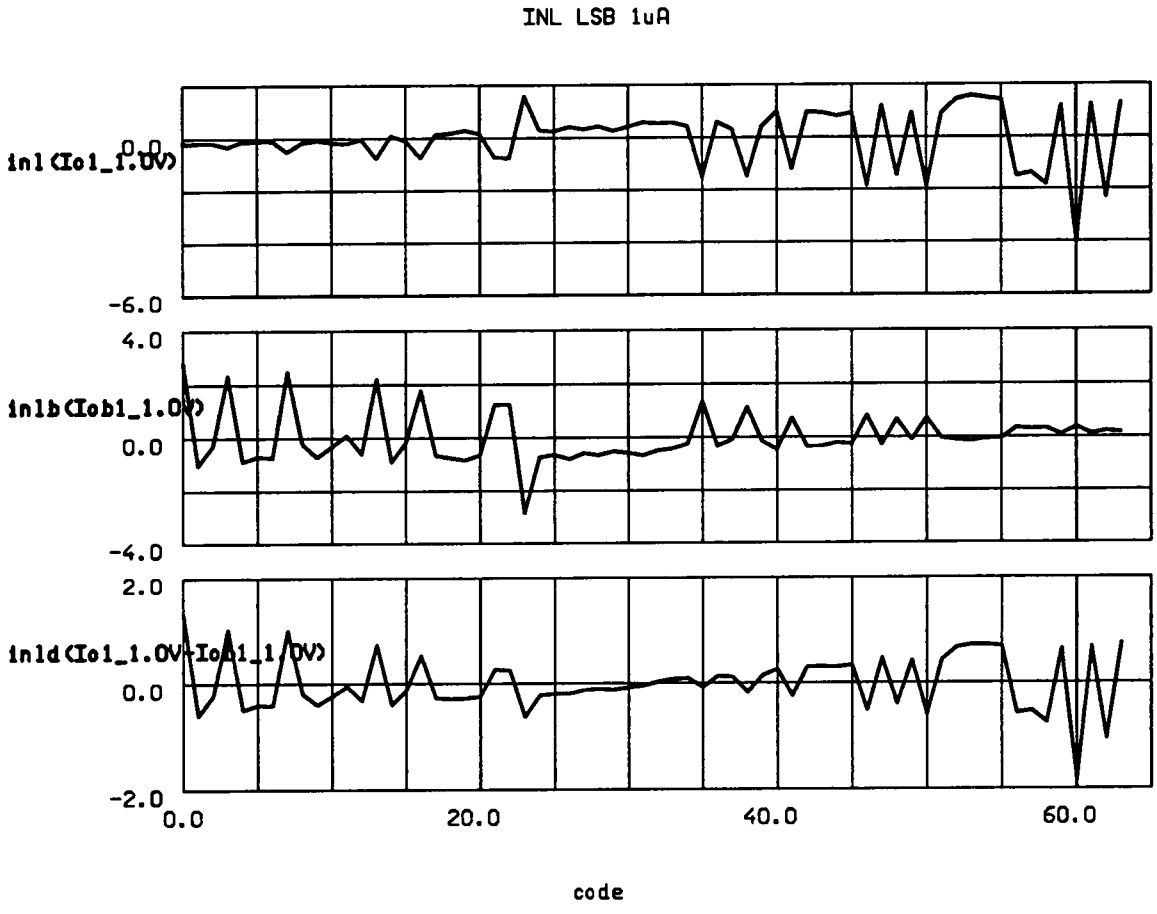

Figure 4.45: Integral non-linearity of DAC on Chip1 at $I_{LSB} = 1\ \mu A$, $V_{out} = 1V$

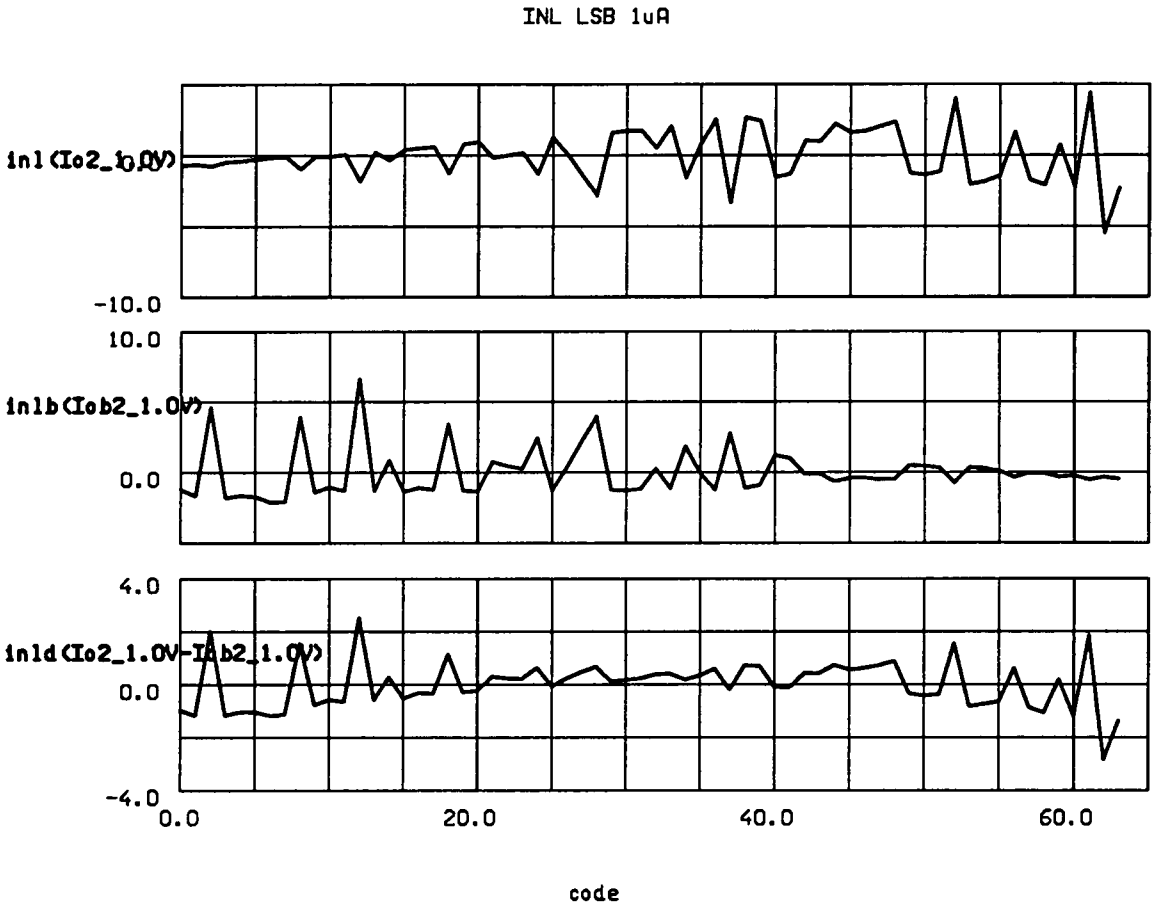

Figure 4.46: Integral non-linearity of DAC on Chip2 at $I_{LSB} = 1\ \mu A$, $V_{out} = 1V$

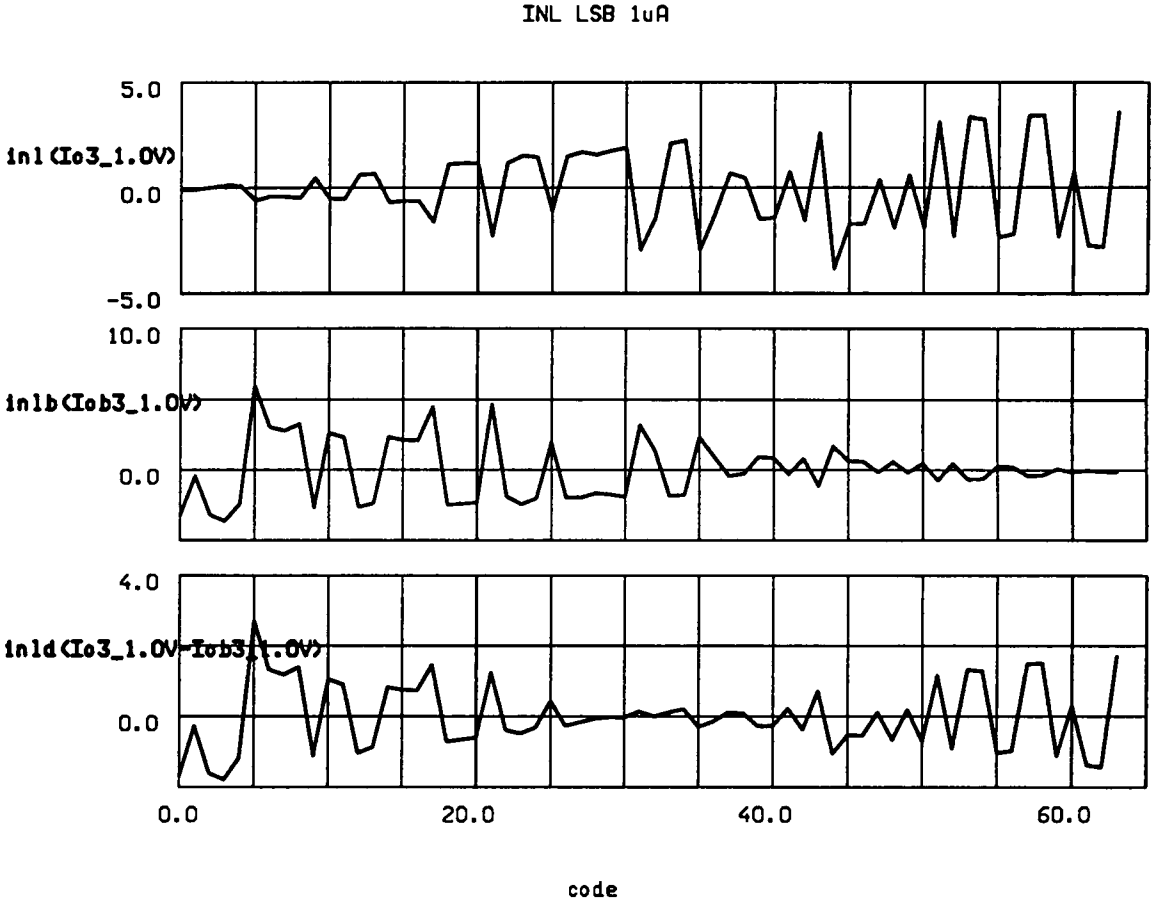

Figure 4.47: Integral non-linearity of DAC on Chip3 at $I_{LSB} = 1\ \mu A$, $V_{out} = 1V$

Chip1, Chip2, and Chip3 respectively, when the input current is 1 μA and the output voltage is 1 V. As shown in these plots, the INL of the DACs at this measured point is much larger than 1LSB. This means that the DACs are not monotonic at this measured point. The best curves among these measurements are the INL of $(I_{out} - \overline{I_{out}})$, which has the worst case INL of about $\pm$2.8LSB. As shown in Figures 4.48, 4.49, and 4.50, the INL of the DACs are not any better for $V_{out} = 5\ V$.

The INL of the DACs for $I_{ref} = 28\ \mu A$ at both output voltages of 1.5 and 5 V, are a lot better than the results for the 1 μA input current. Figures 4.51, 4.52, and 4.53 give the INL of the DACs at $I_{ref} = 28\ \mu A$ and $V_{out} = 1.5\ V$, and Figures 4.54, 4.55, and 4.56 give the INL results at I_{ref}=28 μA and $V_{out} = 5\ V$. The worst case INL at both output voltages of the I_{out} among all three chips is +0.175LSB and $-$0.175LSB. The INL of $\overline{I_{out}}$ is +0.220LSB and $-$0.180LSB. INL for $(I_{out} - \overline{I_{out}})$ is between +0.104LSB and $-$0.093LSB. Therefore, INL of the DAC at 28 μA is less than $\pm$0.5LSB.

The INL of the DACs at $I_{ref} = 109\ \mu A$ for both output voltages of 2.5 and 5 V are shown in Figures 4.57, 4.58, 4.59, 4.60, 4.61, and 4.62. The maximum INL of the I_{out} is +0.073LSB and $-$0.649LSB. The INL of $\overline{I_{out}}$ is +0.897LSB and $-$0.058LSB. INL for $(I_{out} - \overline{I_{out}})$ is between +0.483LSB and $-$0.305LSB.

The INL of the DACs at 217 μA input current was more than $\pm$1LSB at high output voltage of 5 V, as shown in Figures 4.63, 4.64, and 4.65. But the INL was less than $\pm$0.5LSB for the lower output voltage of 3 V, as shown in Figures 4.66, 4.67, and 4.68.

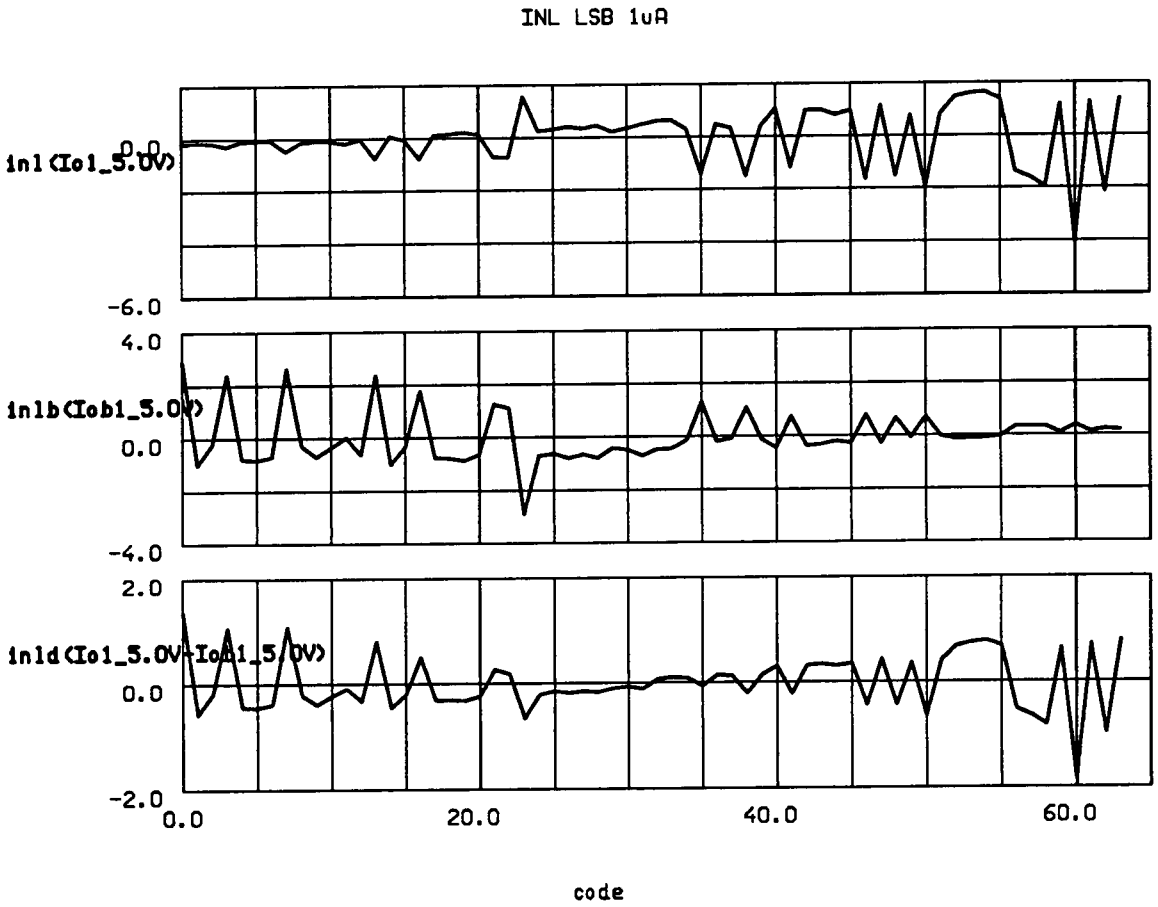

Figure 4.48: Integral non-linearity of DAC on Chip1 at $I_{LSB} = 1\ \mu A$, $V_{out} = 5V$

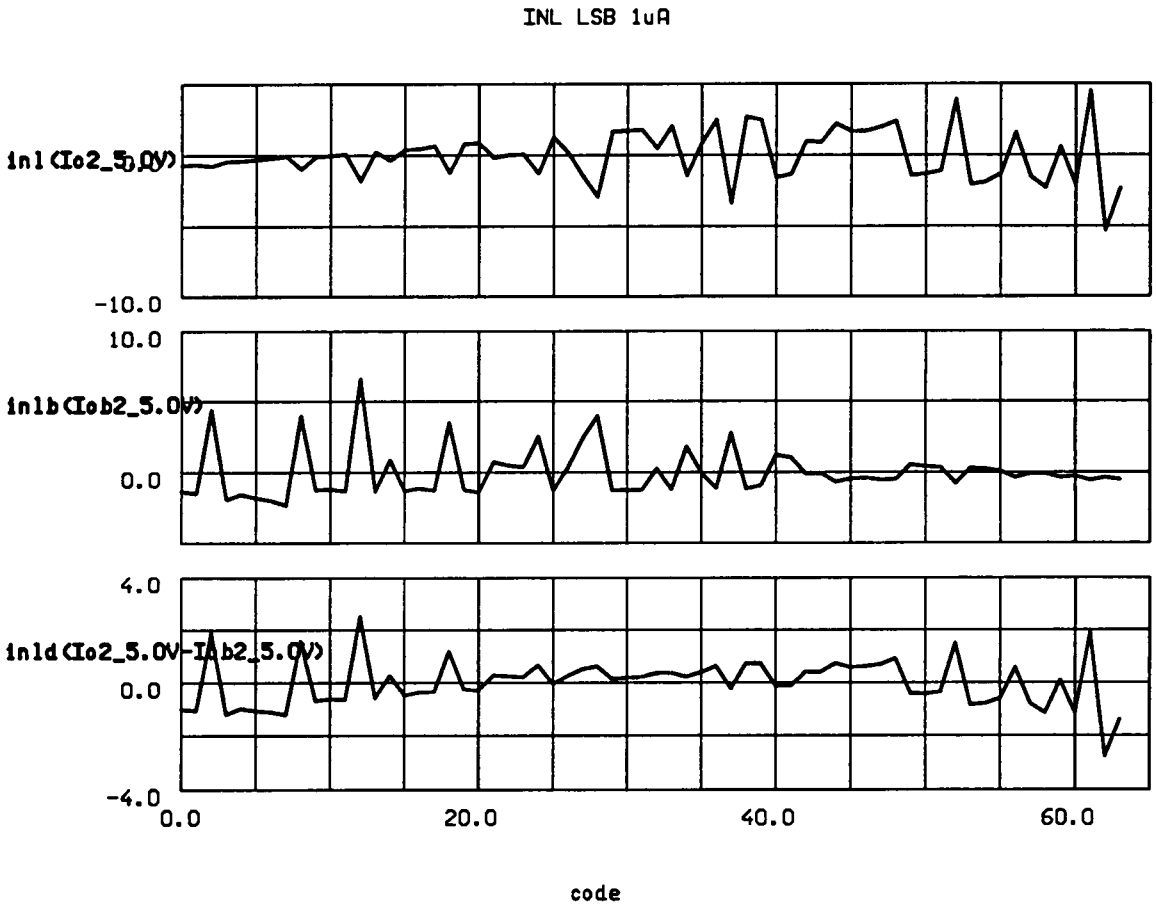

Figure 4.49: Integral non-linearity of DAC on Chip2 at $I_{LSB} = 1\ \mu A$, $V_{out} = 5V$

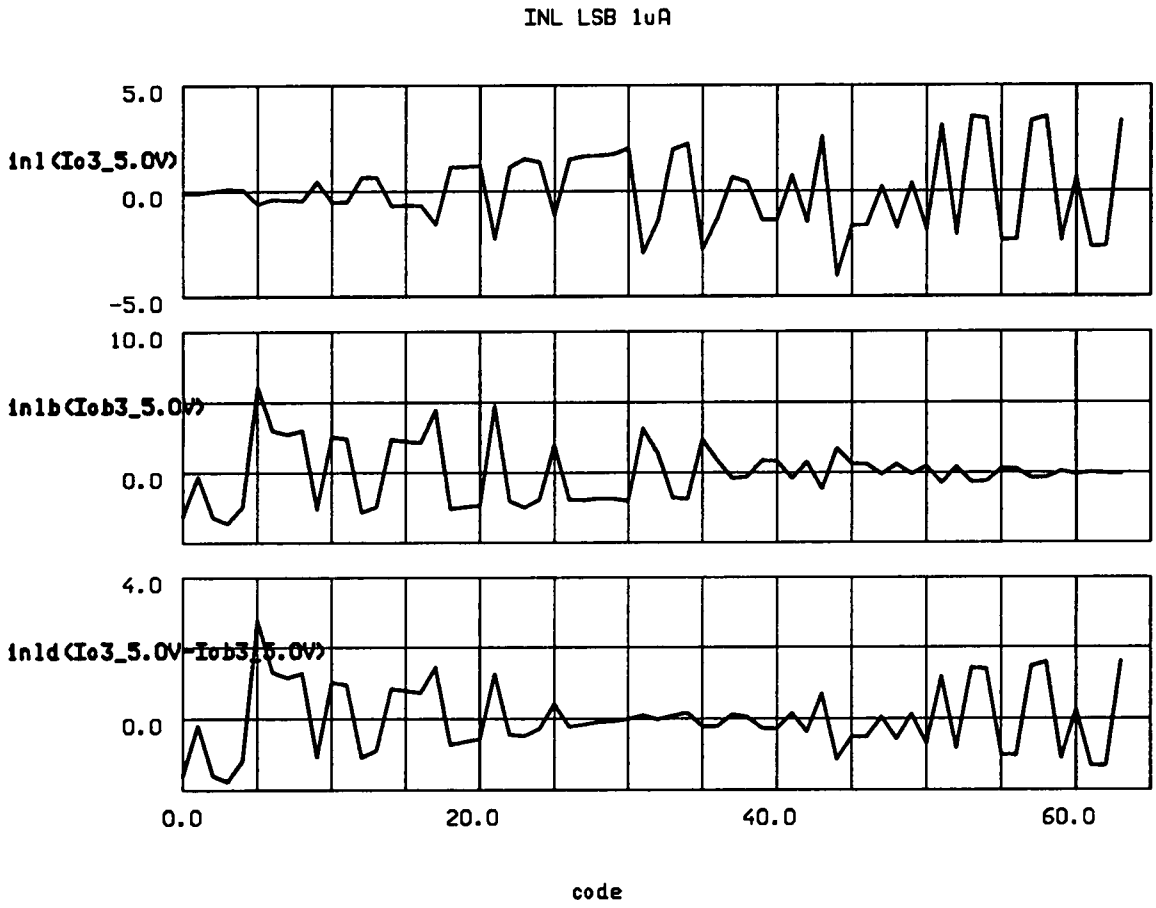

Figure 4.50: Integral non-linearity of DAC on Chip3 at $I_{LSB} = 1\ \mu A$, $V_{out} = 5V$

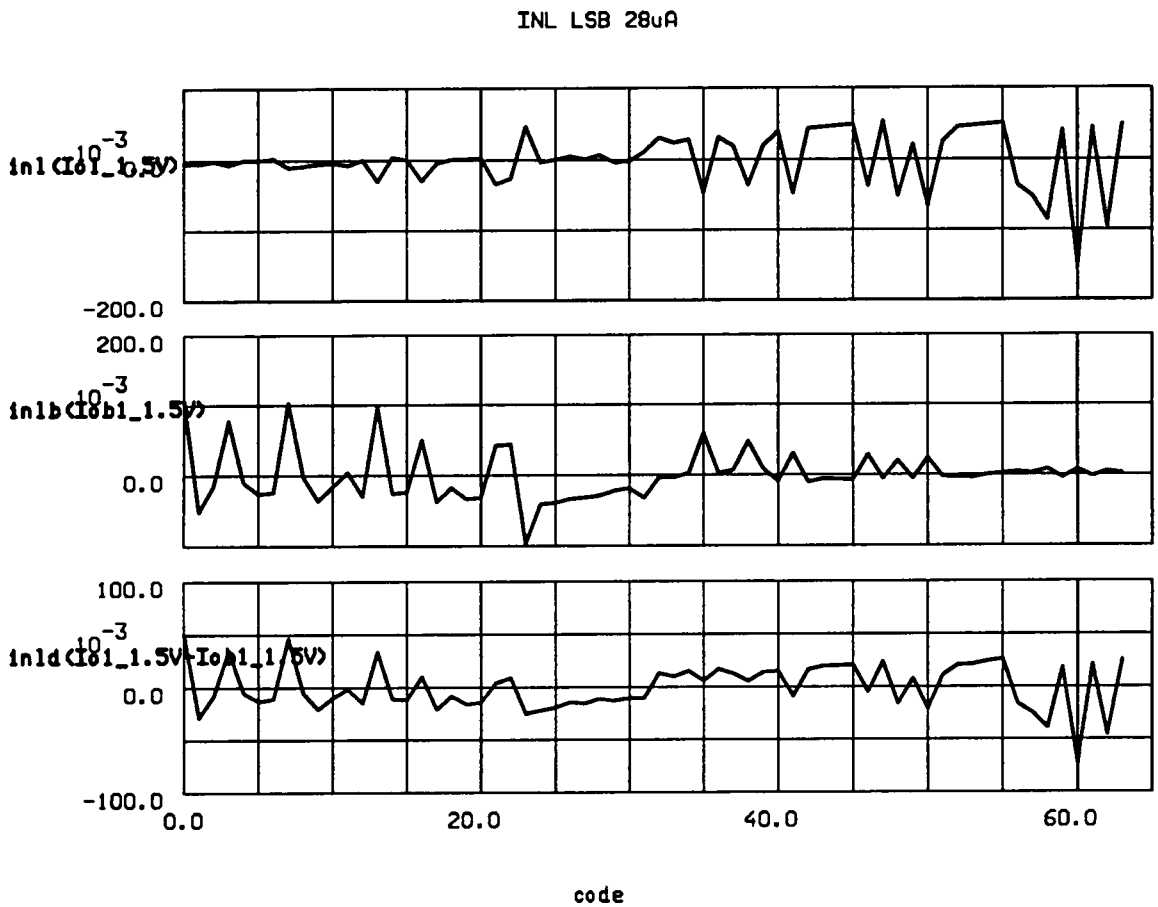

Figure 4.51: Integral non-linearity of DAC on Chip1 at $I_{LSB} = 28\ \mu A$, $V_{out} = 1.5V$

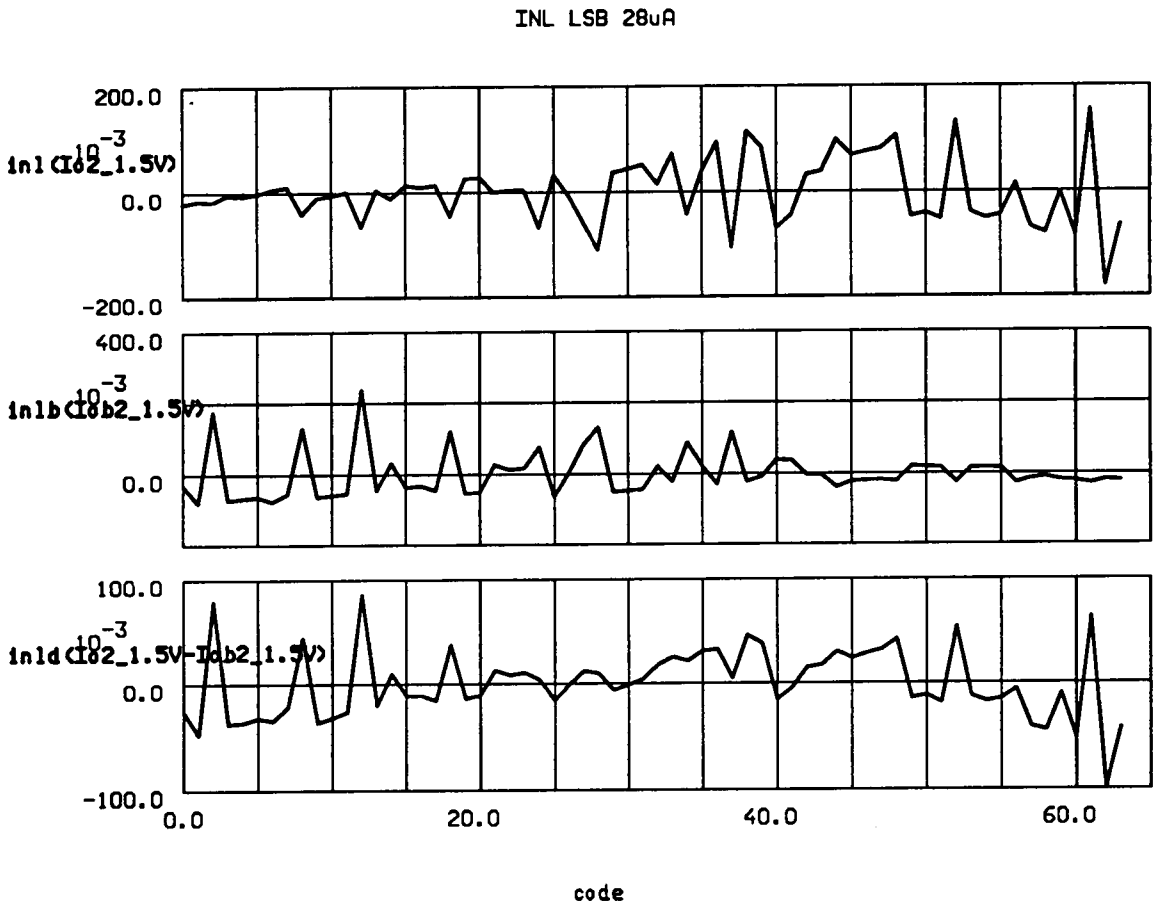

Figure 4.52: Integral non-linearity of DAC on Chip2 at $I_{LSB} = 28\ \mu A$, $V_{out} = 1.5V$

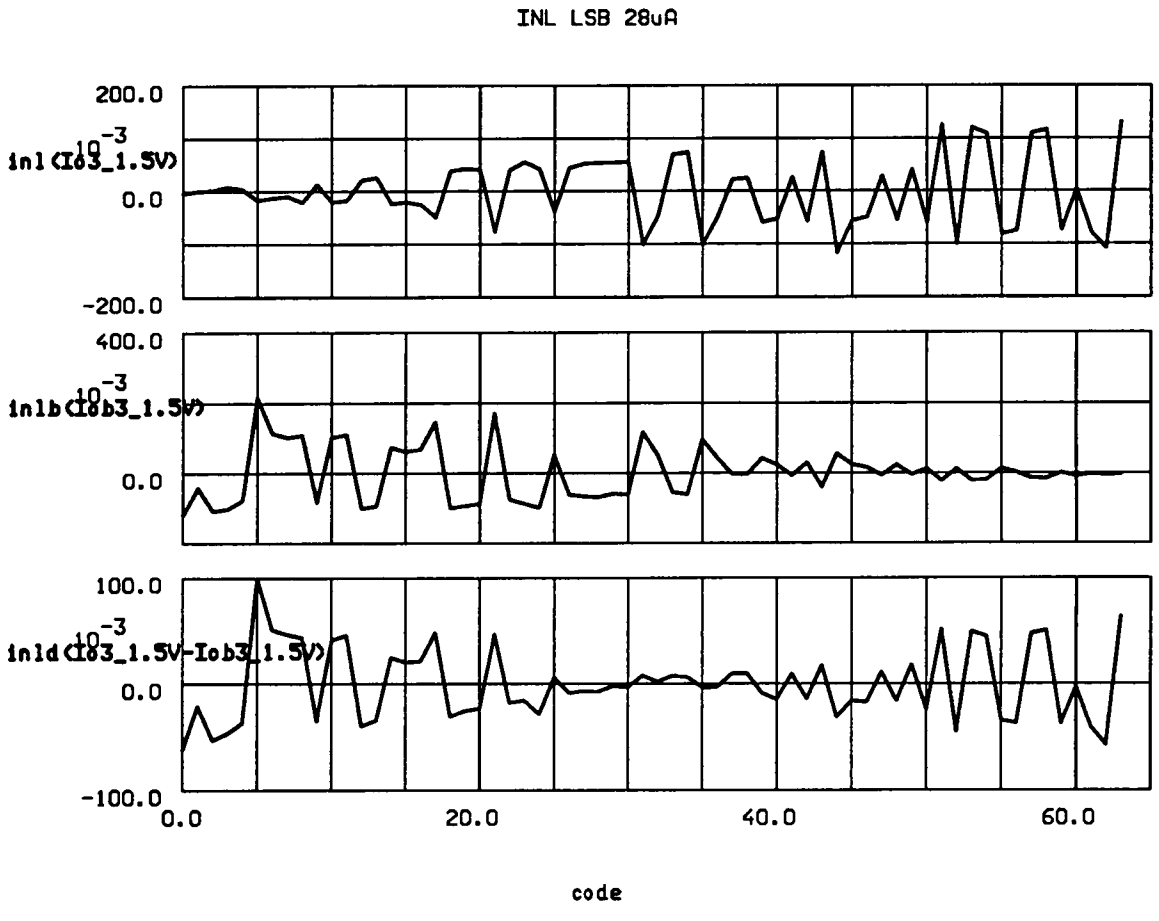

Figure 4.53: Integral non-linearity of DAC on Chip3 at $I_{LSB} = 28\ \mu A$, $V_{out} = 1.5V$

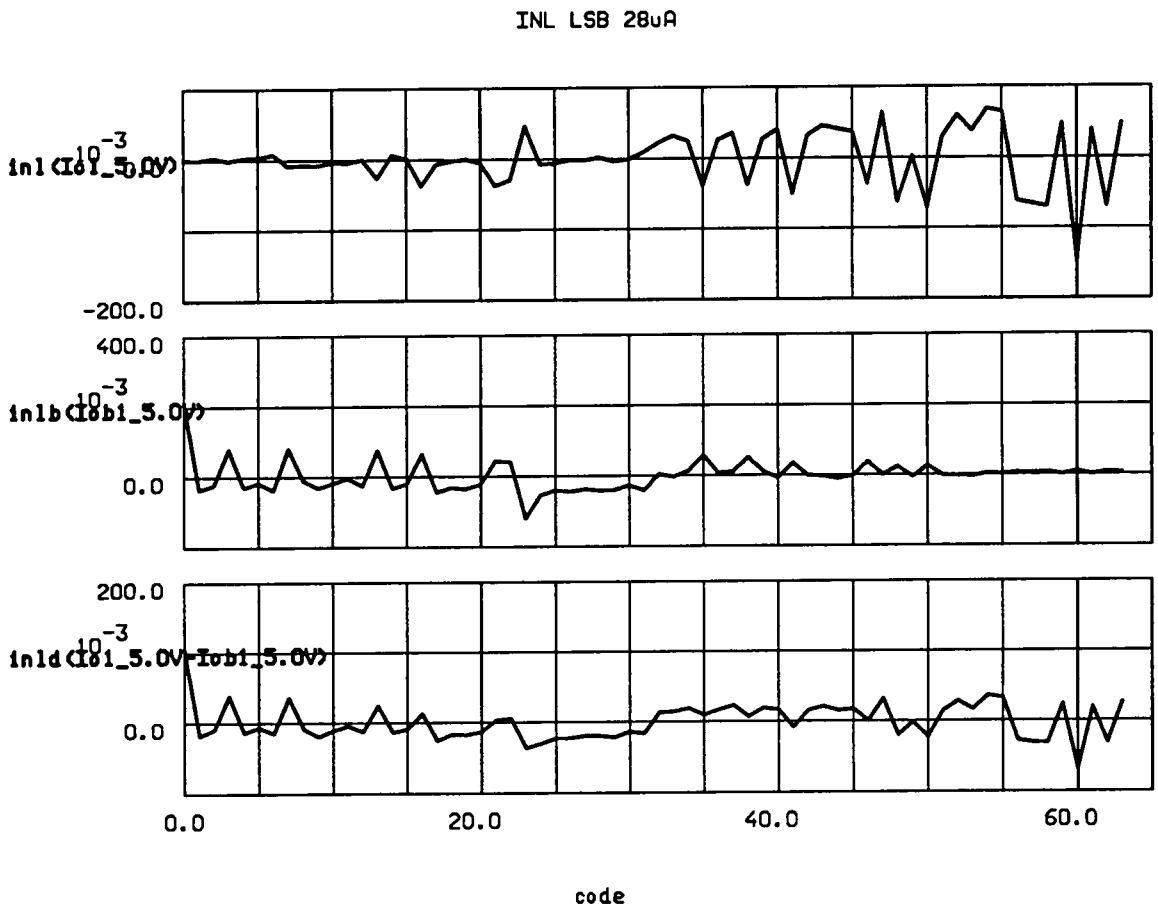

Figure 4.54: Integral non-linearity of DAC on Chip1 at $I_{LSB} = 28\ \mu A$, $V_{out} = 5V$

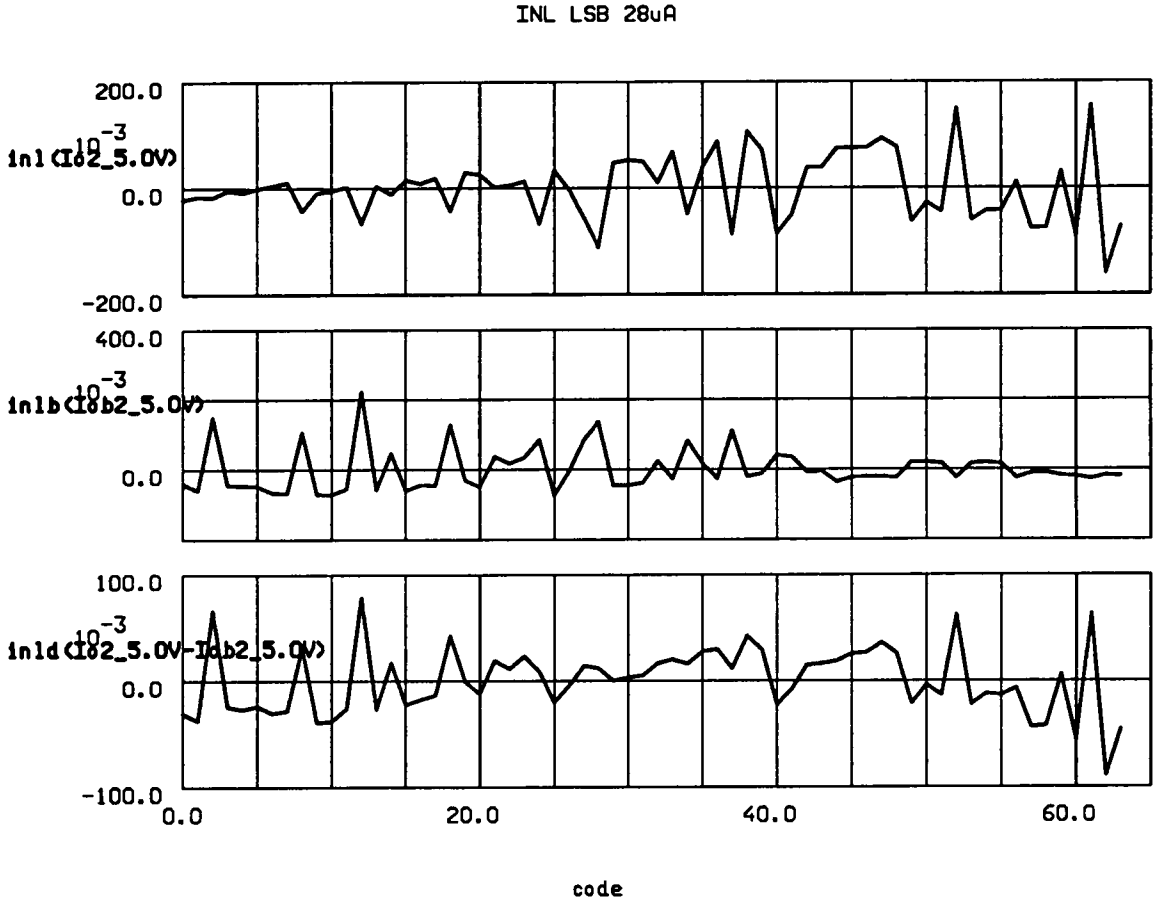

Figure 4.55: Integral non-linearity of DAC on Chip2 at $I_{LSB} = 28\ \mu A$, $V_{out} = 5V$

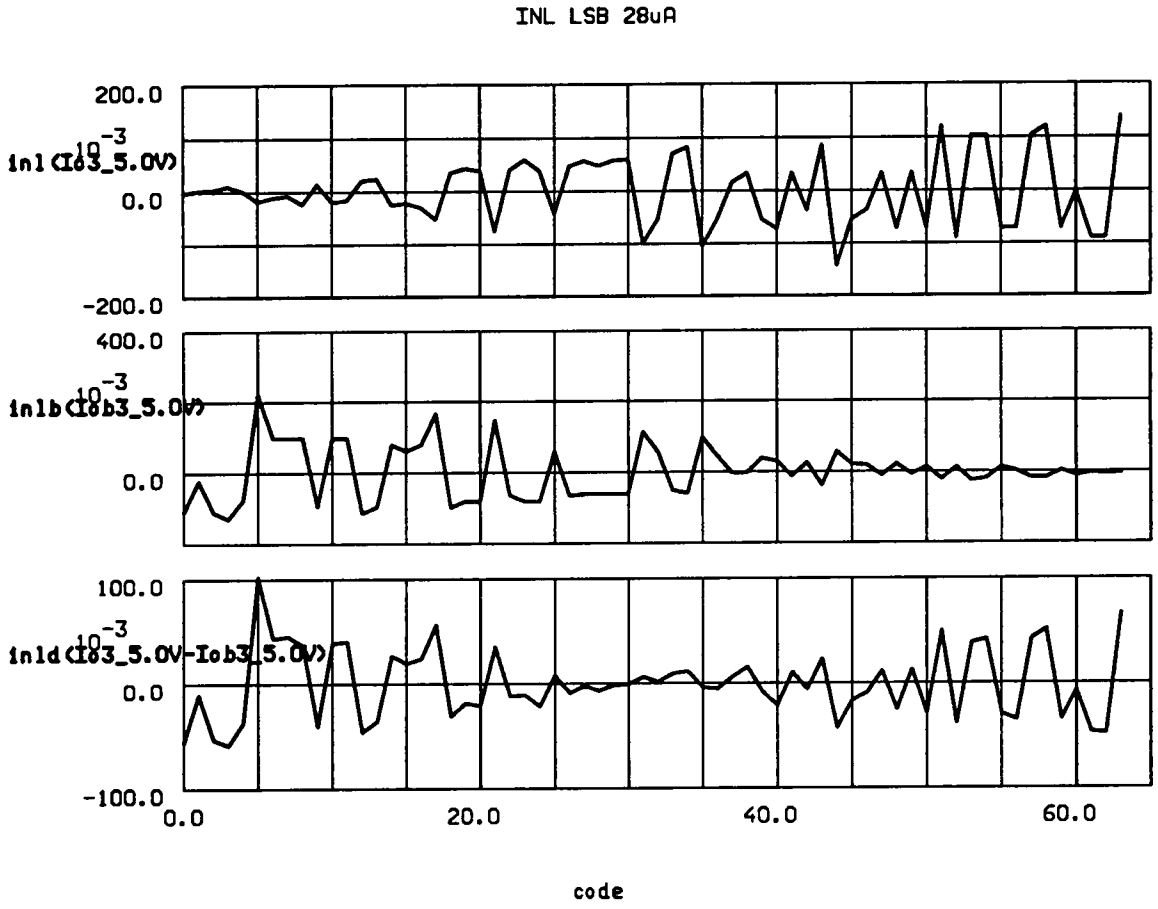

Figure 4.56: Integral non-linearity of DAC on Chip3 at $I_{LSB} = 28\ \mu A$, $V_{out} = 5V$

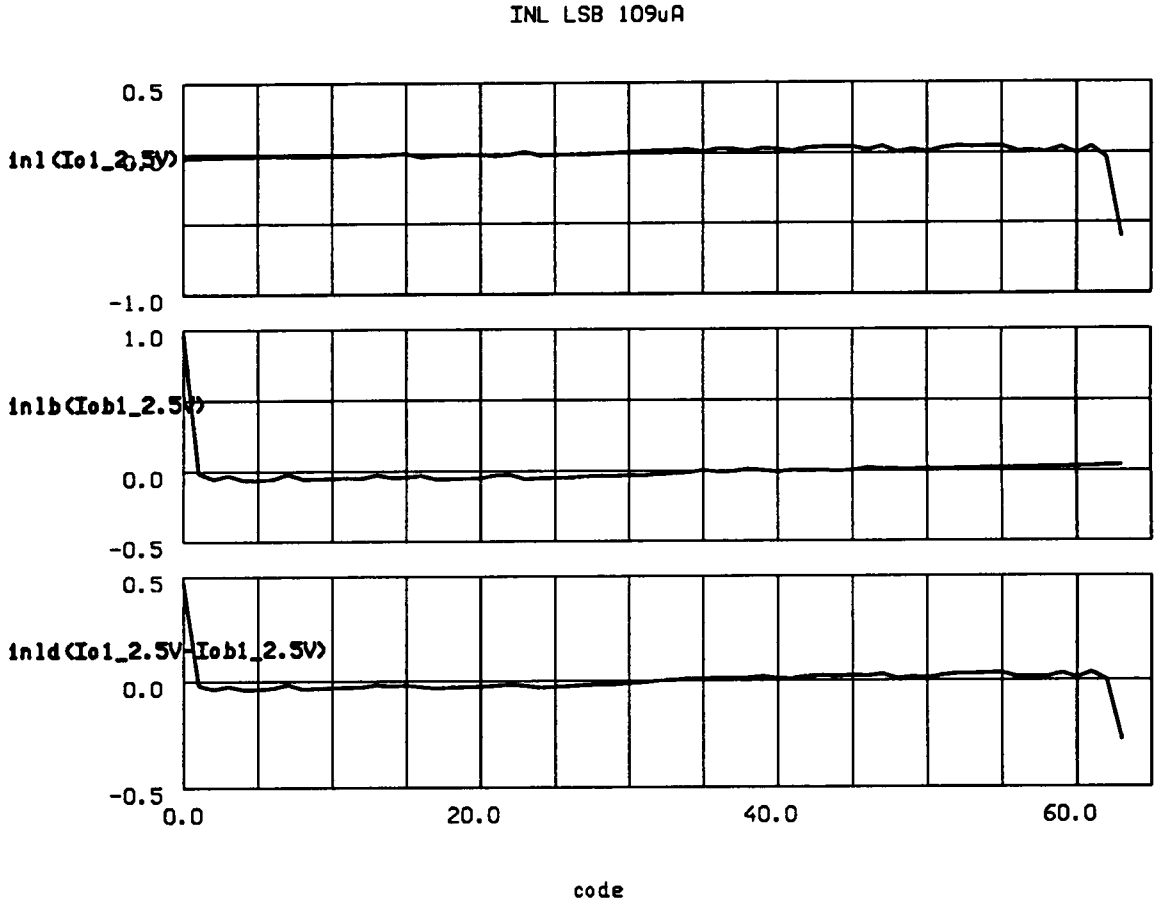

Figure 4.57: Integral non-linearity of DAC on Chip1 at $I_{LSB} = 109\ \mu A$, $V_{out} = 2.5V$

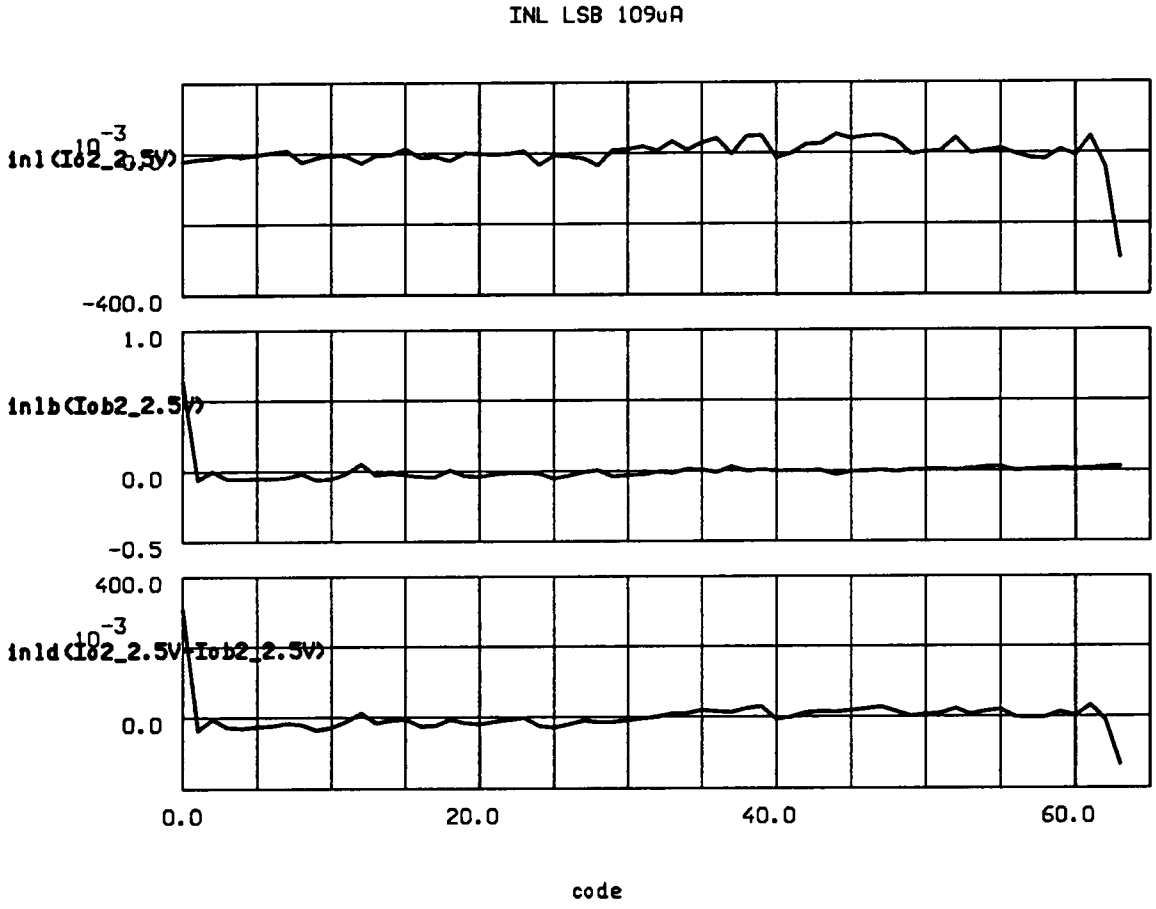

Figure 4.58: Integral non-linearity of DAC on Chip2 at $I_{LSB} = 109\ \mu A$, $V_{out} = 2.5V$

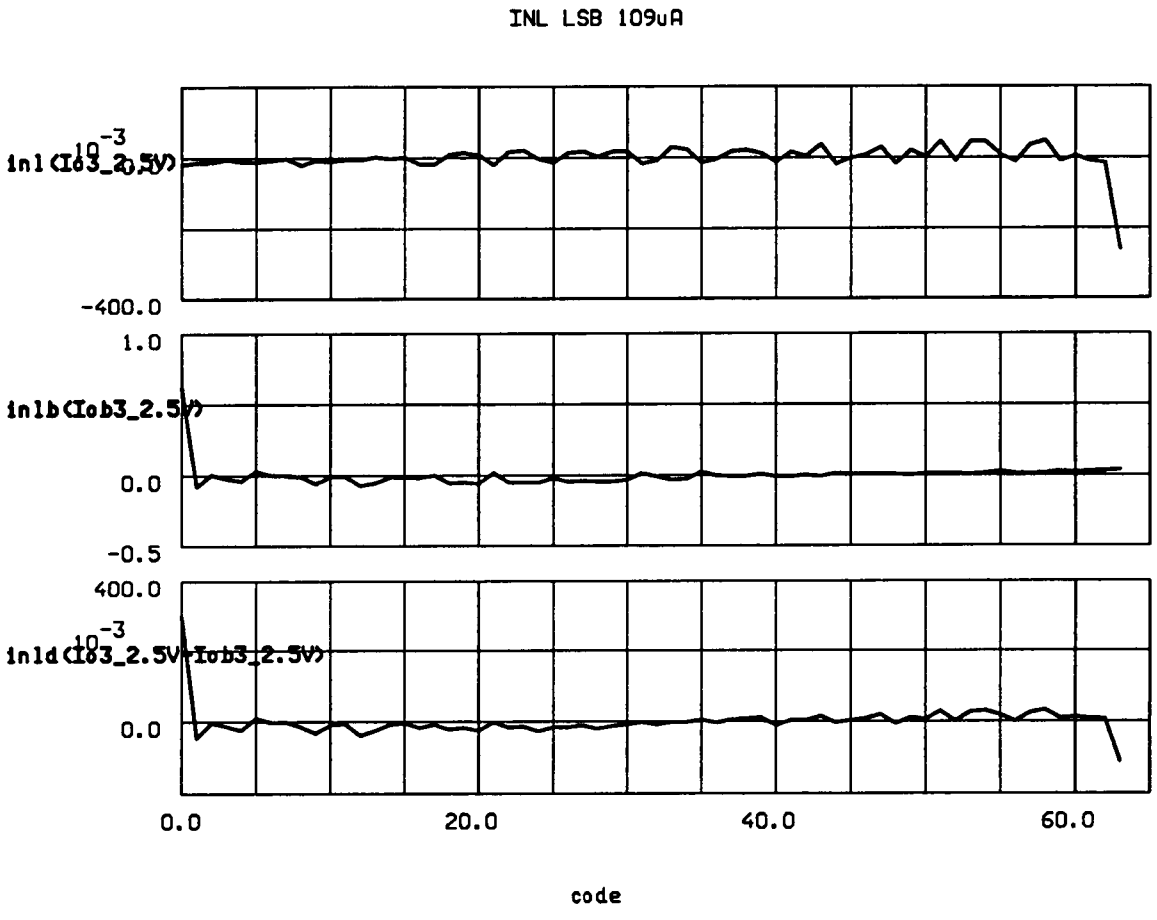

Figure 4.59: Integral non-linearity of DAC on Chip3 at $I_{LSB} = 109\ \mu A$, $V_{out} = 2.5V$

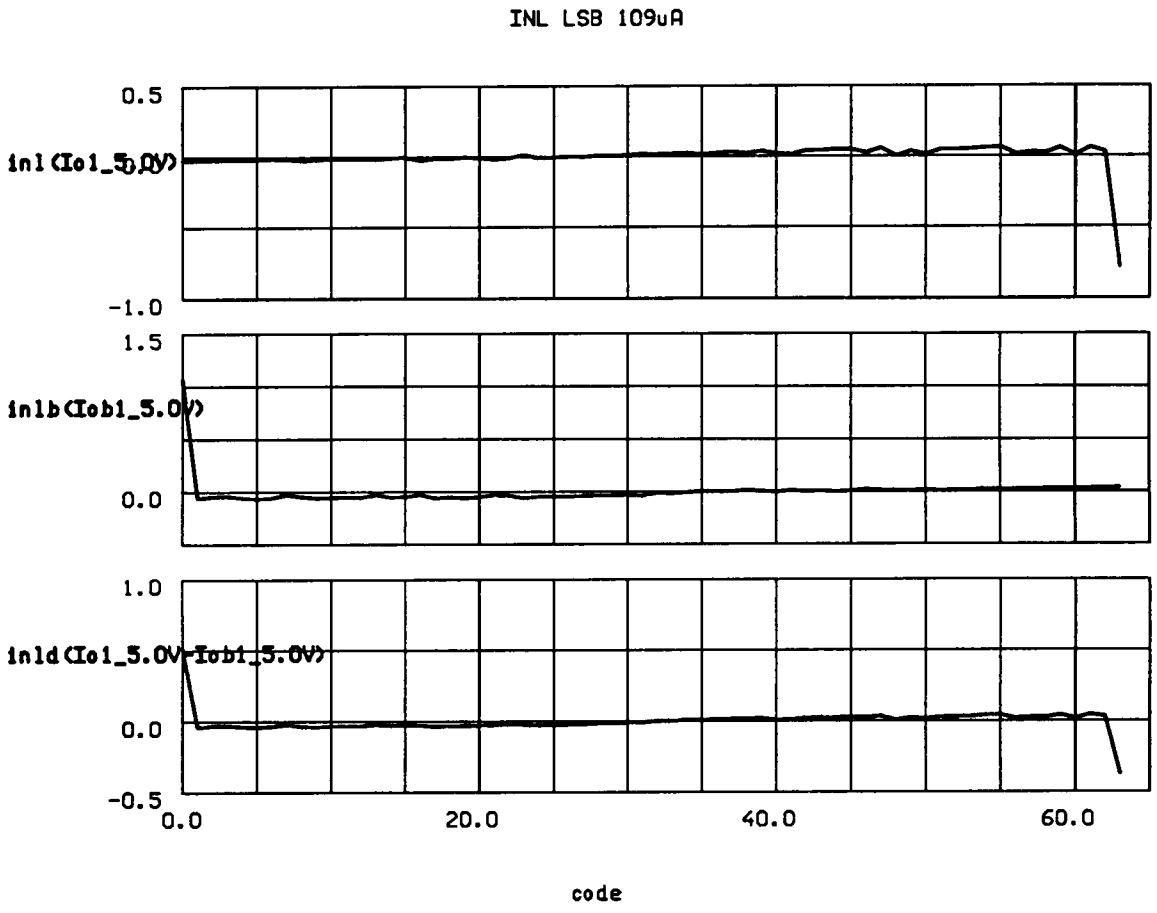

Figure 4.60: Integral non-linearity of DAC on Chip1 at $I_{LSB} = 109\ \mu A$, $V_{out} = 5V$

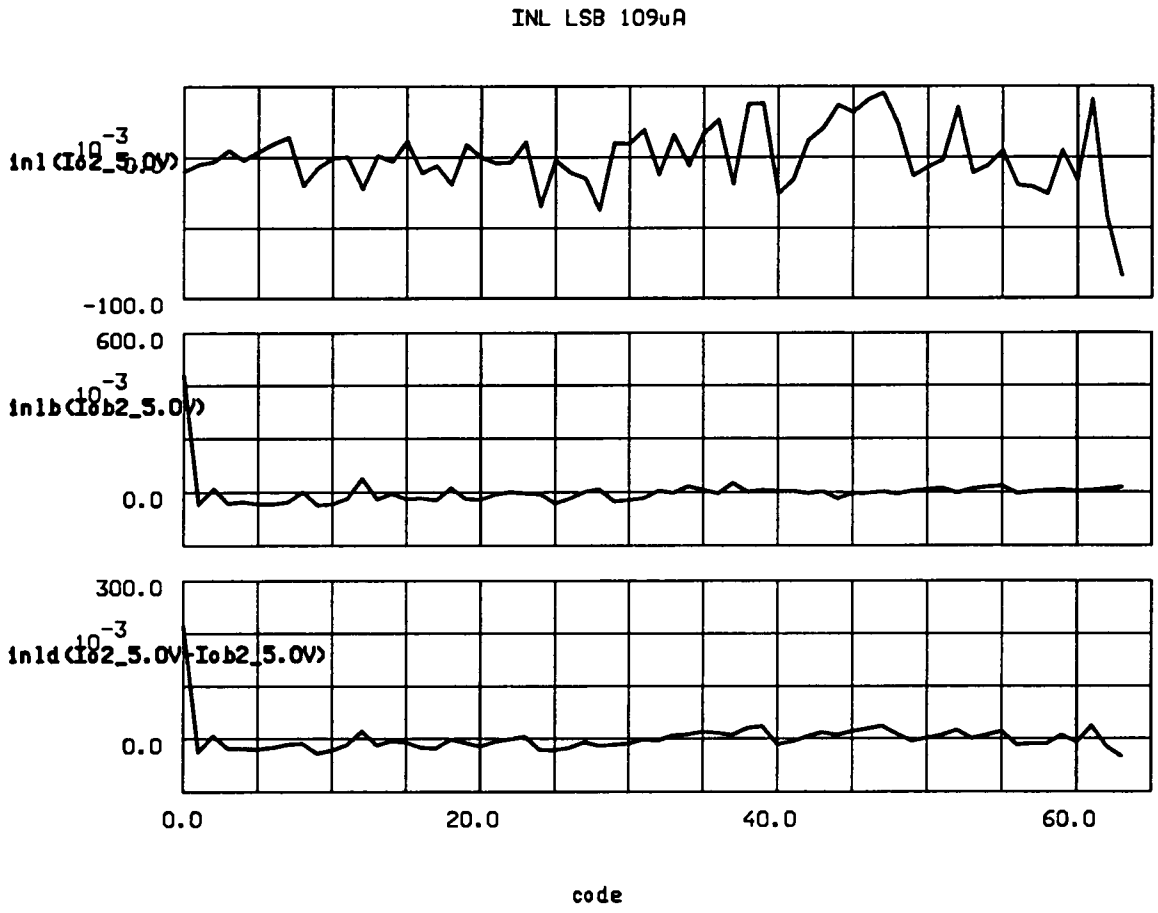

Figure 4.61: Integral non-linearity of DAC on Chip2 at $I_{LSB} = 109\ \mu A$, $V_{out} = 5V$

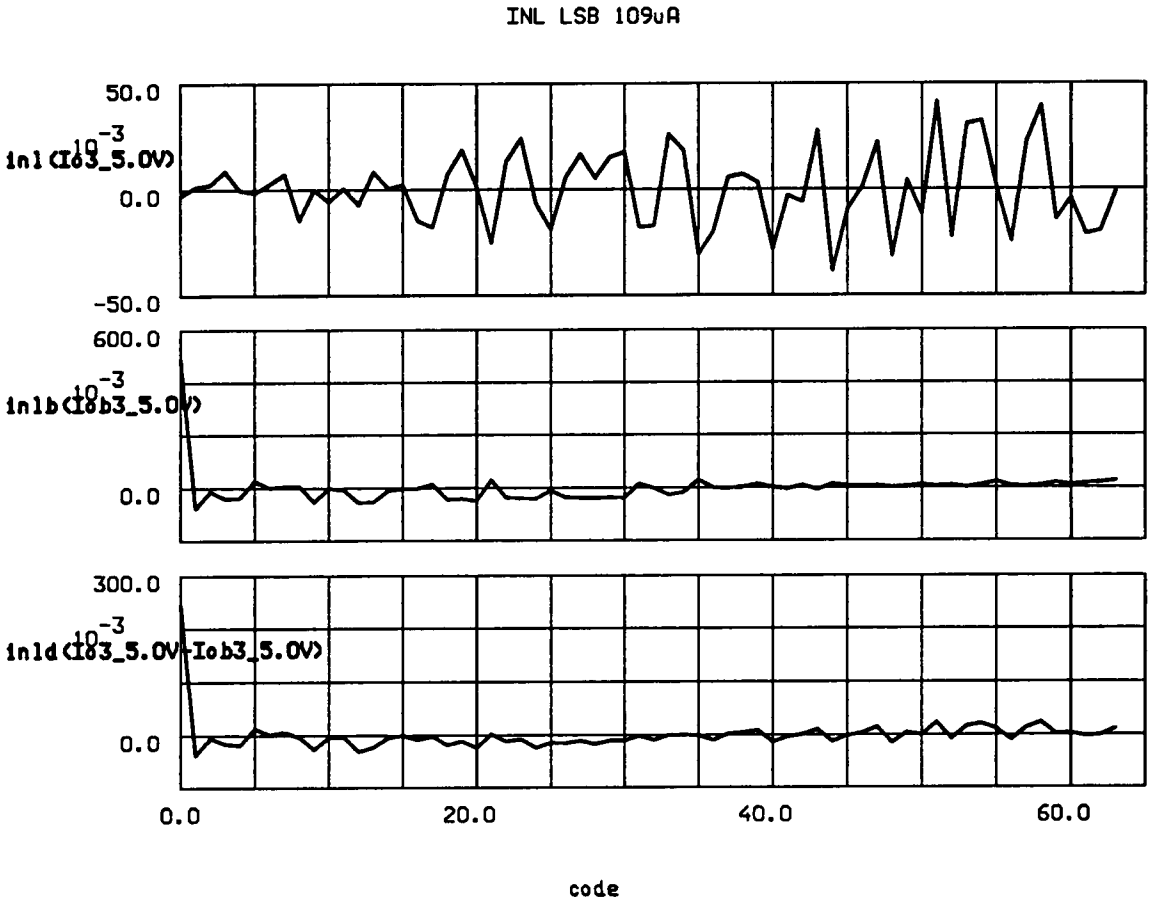

Figure 4.62: Integral non-linearity of DAC on Chip3 at $I_{LSB} = 109\ \mu A$, $V_{out} = 5V$

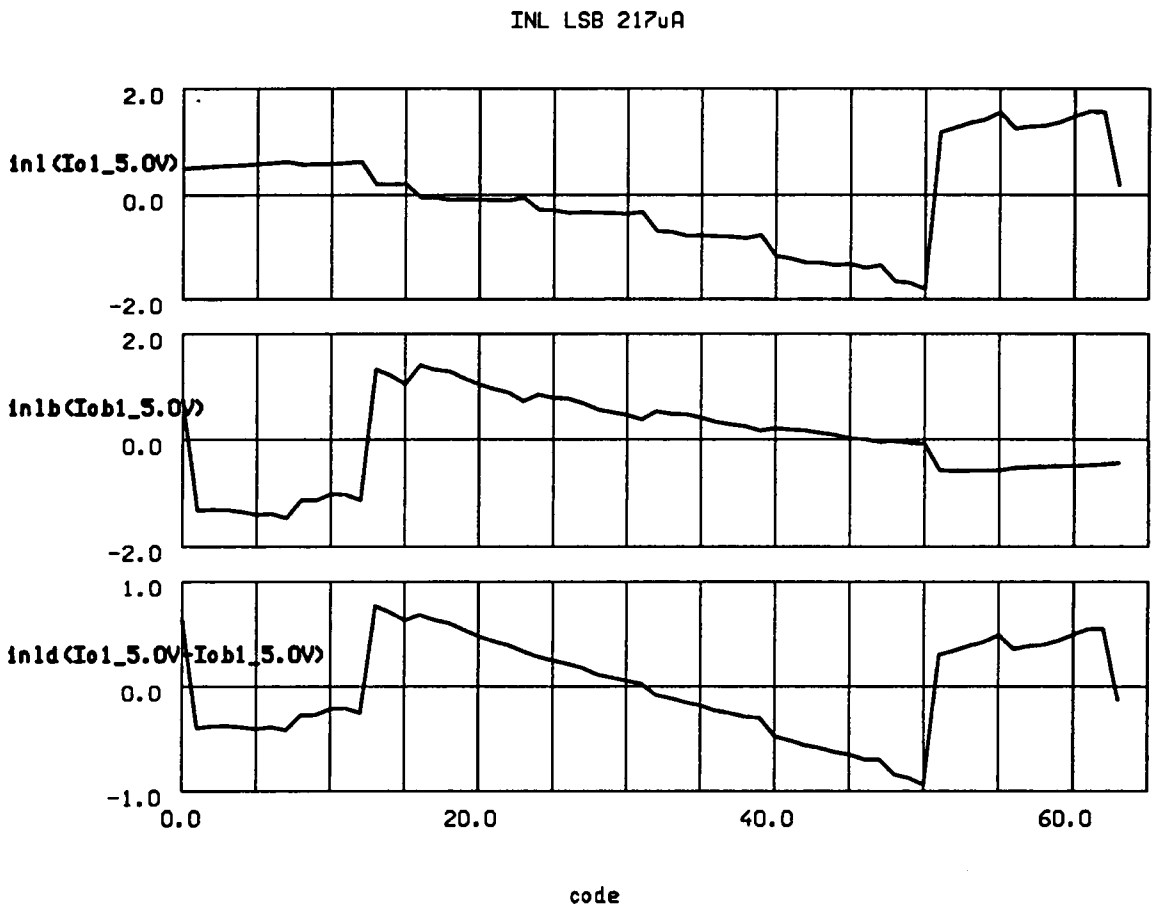

Figure 4.63: Integral non-linearity of DAC on Chip1 at $I_{LSB} = 217\ \mu A$, $V_{out} = 5V$

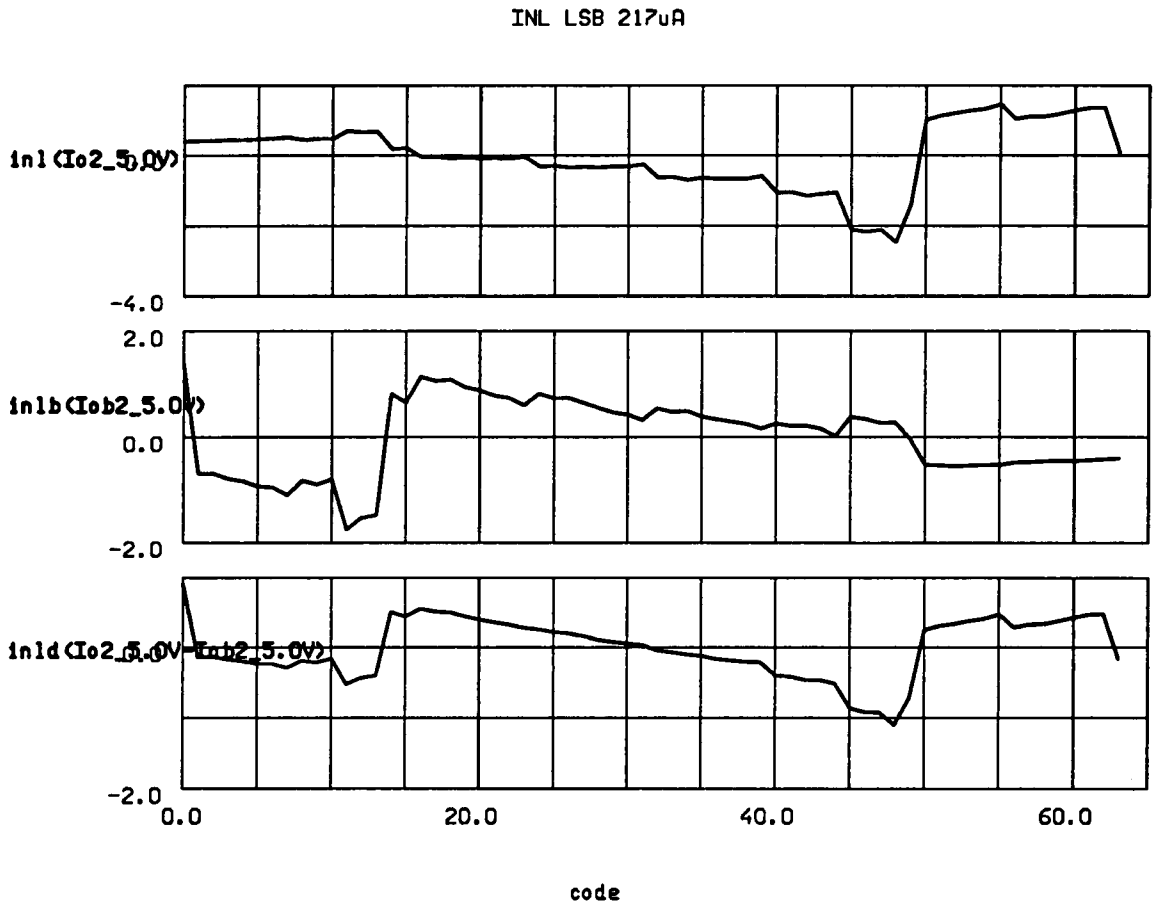

Figure 4.64: Integral non-linearity of DAC on Chip2 at $I_{LSB} = 217\ \mu A$, $V_{out} = 5V$

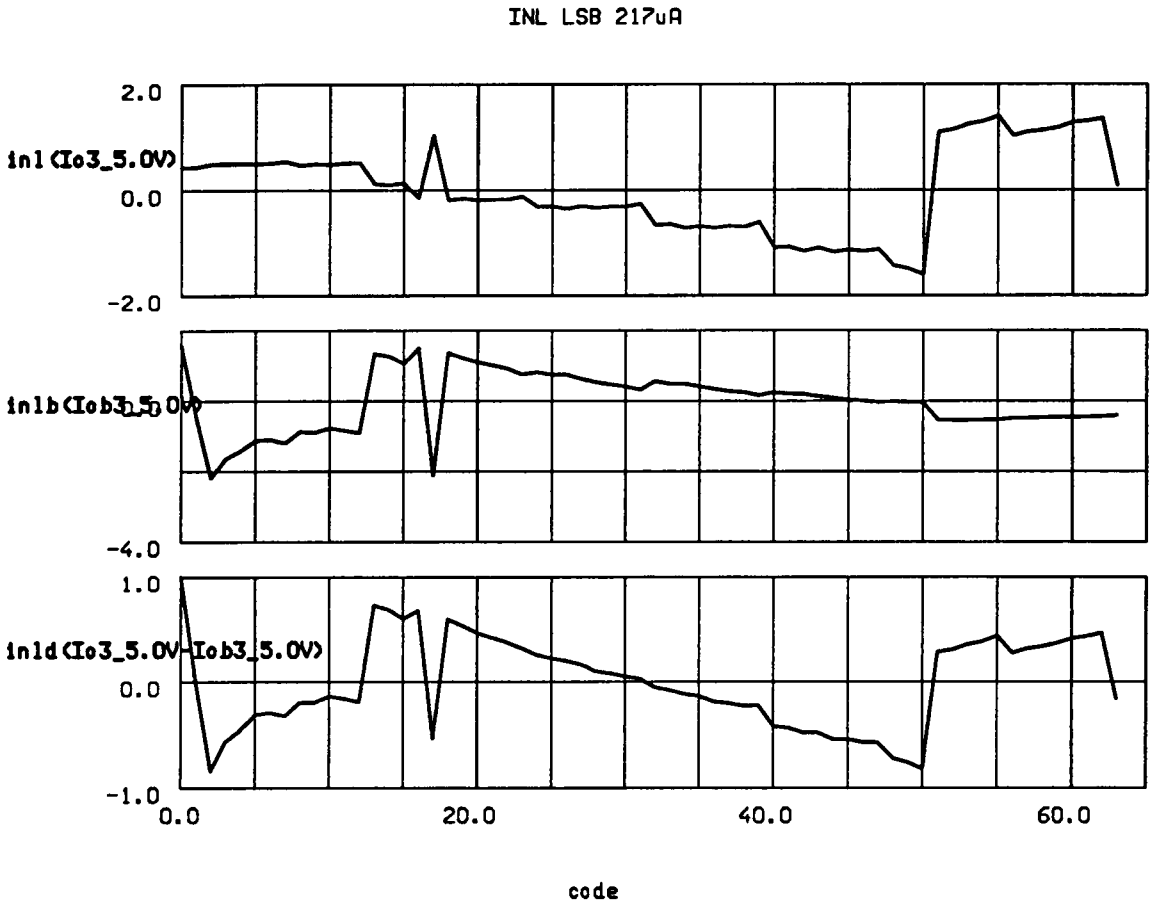

Figure 4.65: Integral non-linearity of DAC on Chip3 at $I_{LSB} = 217\ \mu A$, $V_{out} = 5V$

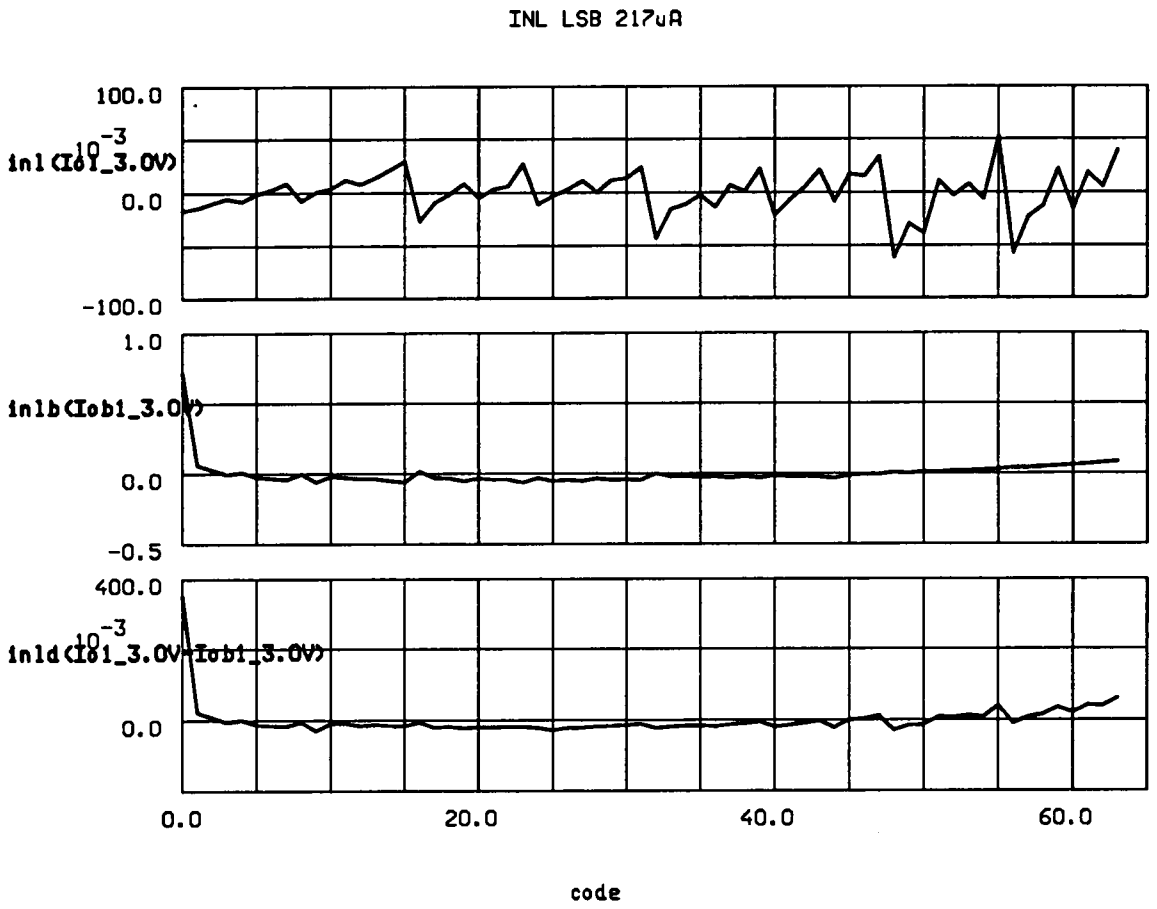

Figure 4.66: Integral non-linearity of DAC on Chip1 at $I_{LSB} = 217\ \mu A$, $V_{out} = 3V$

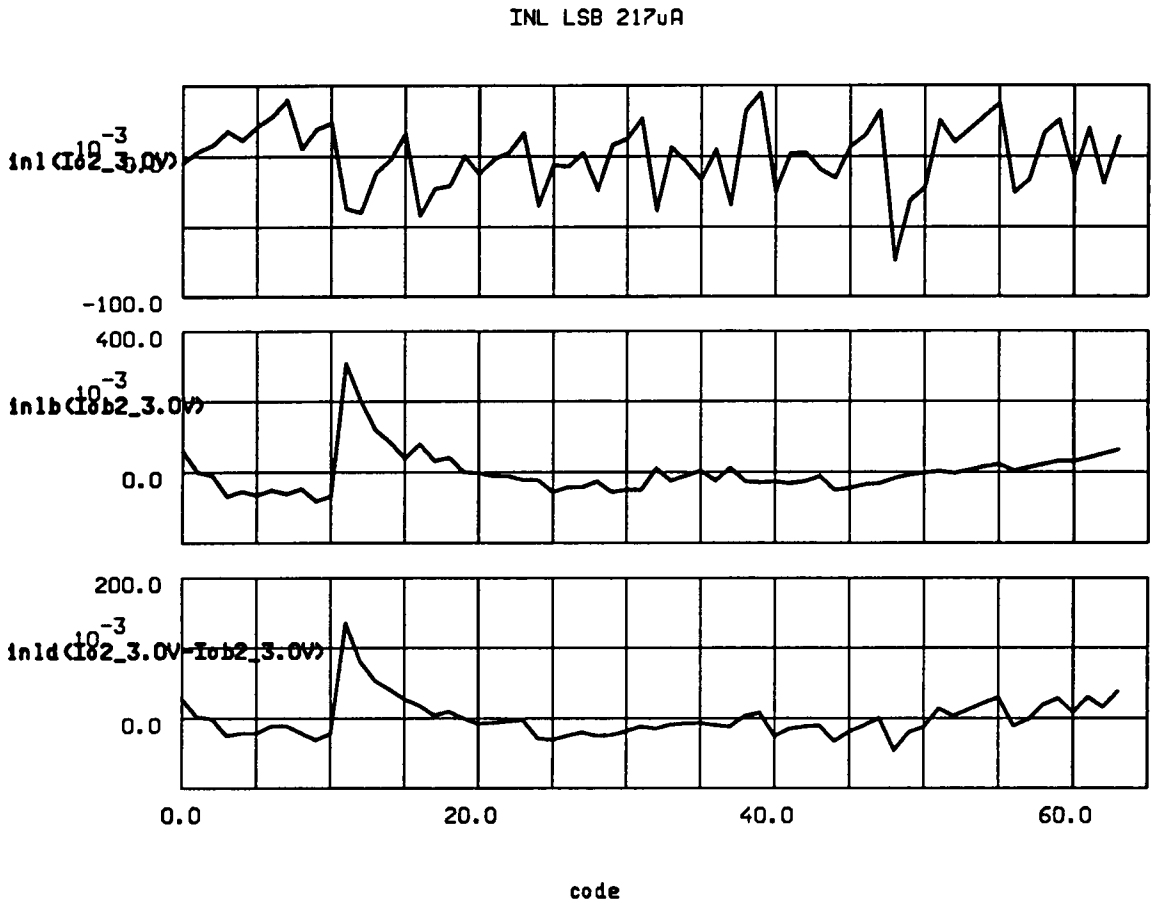

Figure 4.67: Integral non-linearity of DAC on Chip2 at $I_{LSB} = 217\ \mu A$, $V_{out} = 3V$

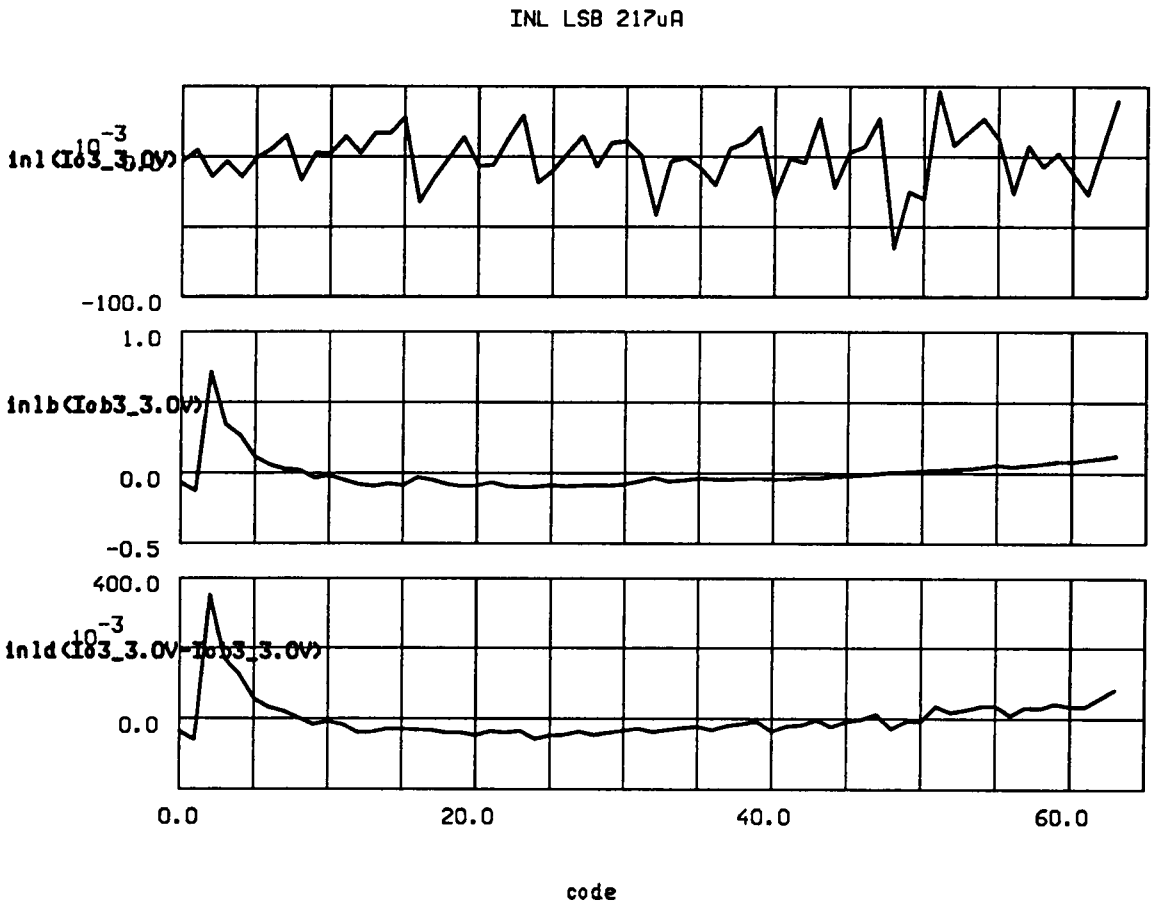

Figure 4.68: Integral non-linearity of DAC on Chip3 at $I_{LSB} = 217\ \mu A$, $V_{out} = 3V$

To summarize the INL results, it is evident that the current DAC has integral linearity of better than ±1LSB at currents ranges between 28 and 109 μA. Even at higher currents than the $I_{out(max.)}$ range, as long as the output voltages are lower, the DAC will have less than ±1LSB INL.

CHAPTER 5

SUMMARY AND CONCLUSIONS

This thesis has described the design and measurement of a six-bit current steering digital-to-analog converter. The converter was implemented in a 2 μm CMOS process, and fabricated by the MOSIS service. Three of the four DACs were found to be fully functional and were characterized over a range of reference currents and output voltages. The DAC was monotonic above 1 μA input current.

Figures 5.1, 5.2, and 5.3 summarize the maximum DNL versus I_{ref} of each chip's DAC, over the input current range of 1 to 271 μA at output voltages of 1.5, 3, and 5 V, respectively. The top set of the curves represent the maximum DNL of I_{out} versus I_{ref} for Chip1, Chip2, and Chip3. The second set of curves represent the maximum DNL of $\overline{I_{out}}$ versus I_{ref}. The bottom set of curves show the maximum DNL of $(I_{out} - \overline{I_{out}})$ versus I_{ref}. The differential non-linearity was found to be less than $\pm$ 0.5LSB at input current of 28 μA at all output voltages of 1 to 5 V. To summarize, it is evident that the current DAC has DNL of $\pm$1LSB at currents ranged between 28 and 130 μA. Even currents above 130 μA, (as long as the output voltages are lower than 5V), the DAC will have less than $\pm$1LSB DNL.

Figures 5.4, 5.5, and 5.6 summarize the maximum INL versus I_{ref} of each chip's DAC, over the input current range of 1 to 271 μA at output voltages of 1.5, 3, and 5 V, respectively. The top set of the curves represents the maximum INL of I_{out}

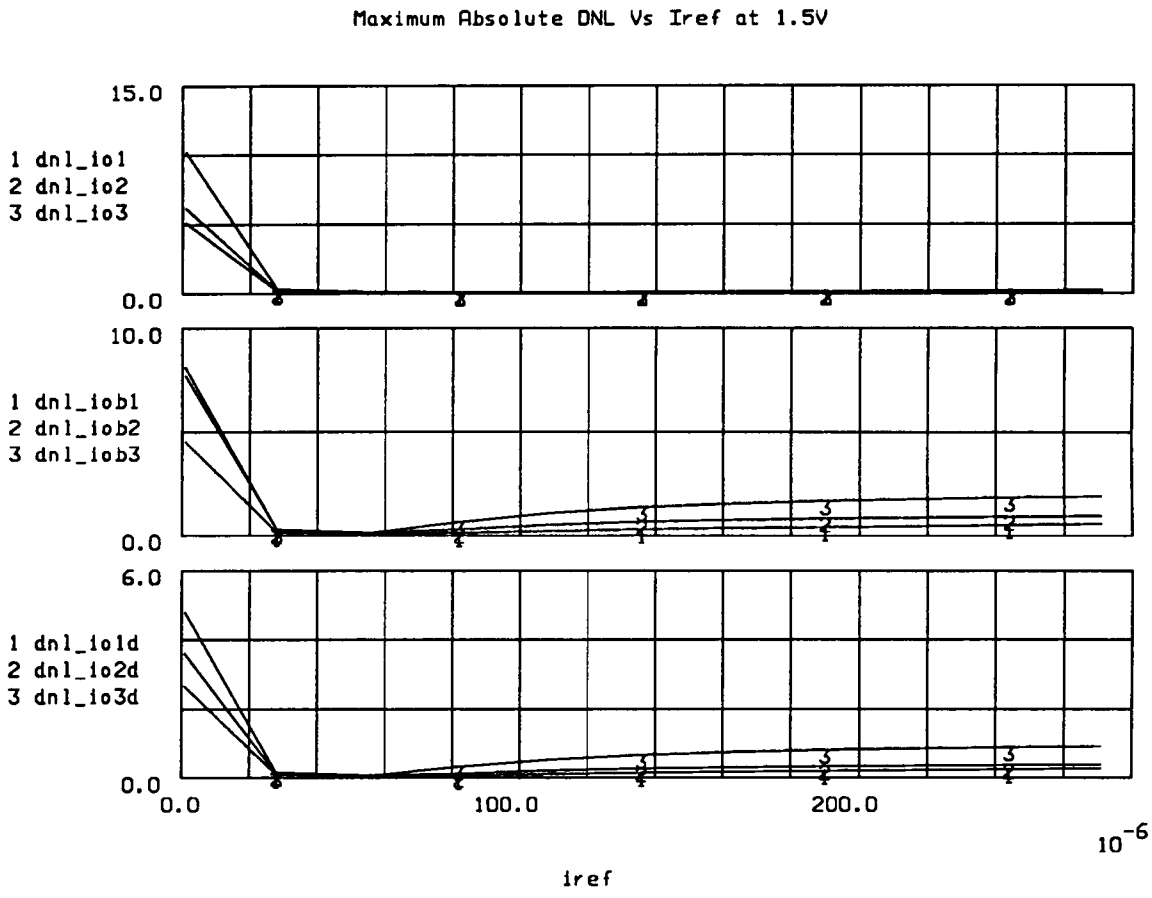

Figure 5.1: Maximum differential non-linearity plotted versus reference current of each chip at $V_{out} = 1.5V$

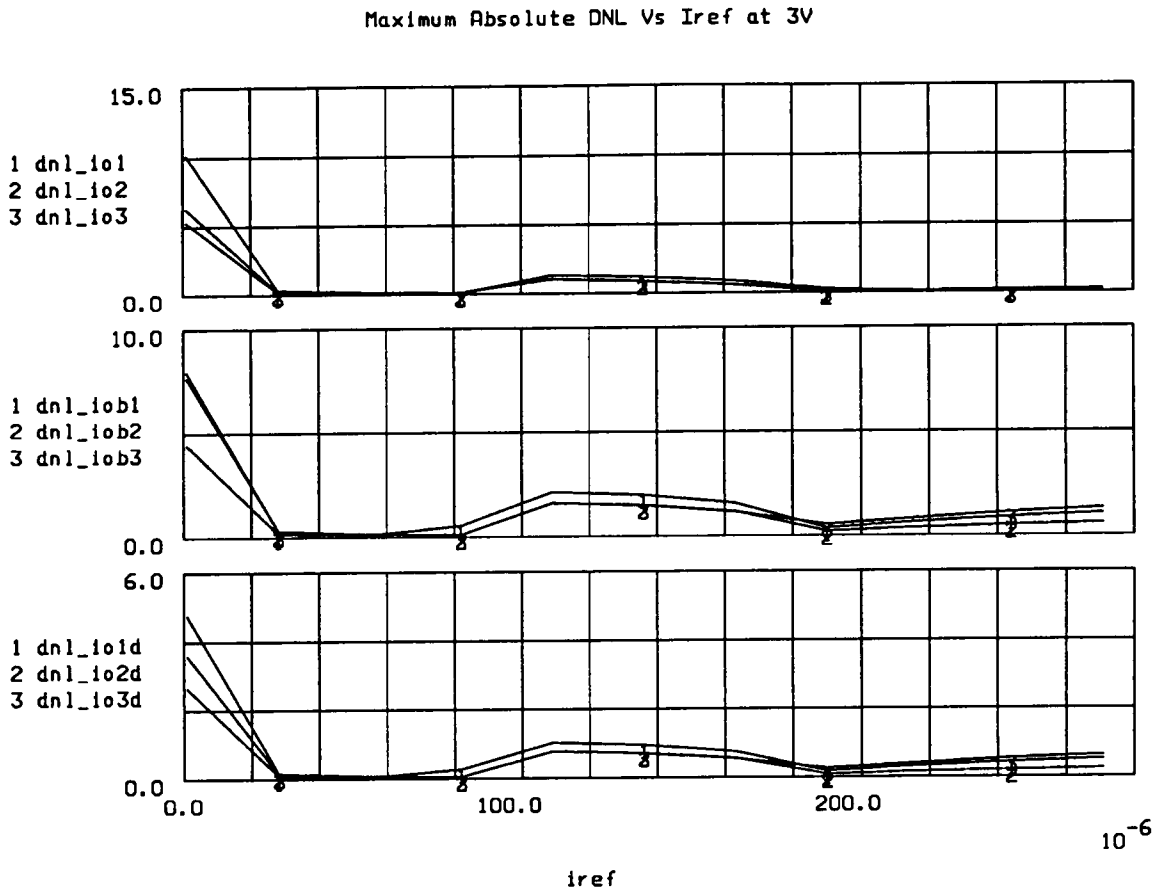

Figure 5.2: Maximum differential non-linearity plotted versus reference current of each chip at $V_{out} = 3V$

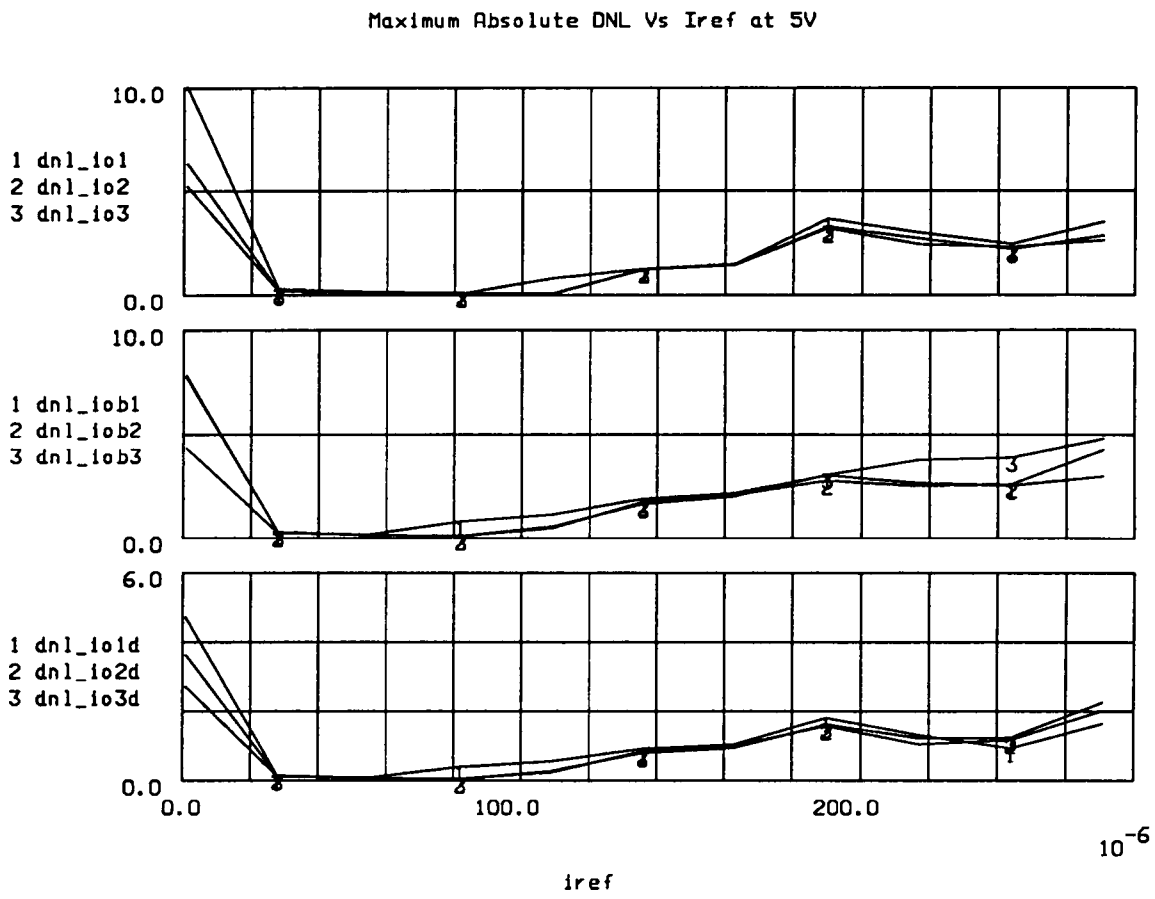

Figure 5.3: Maximum differential non-linearity plotted versus reference current of each chip at $V_{out} = 5V$

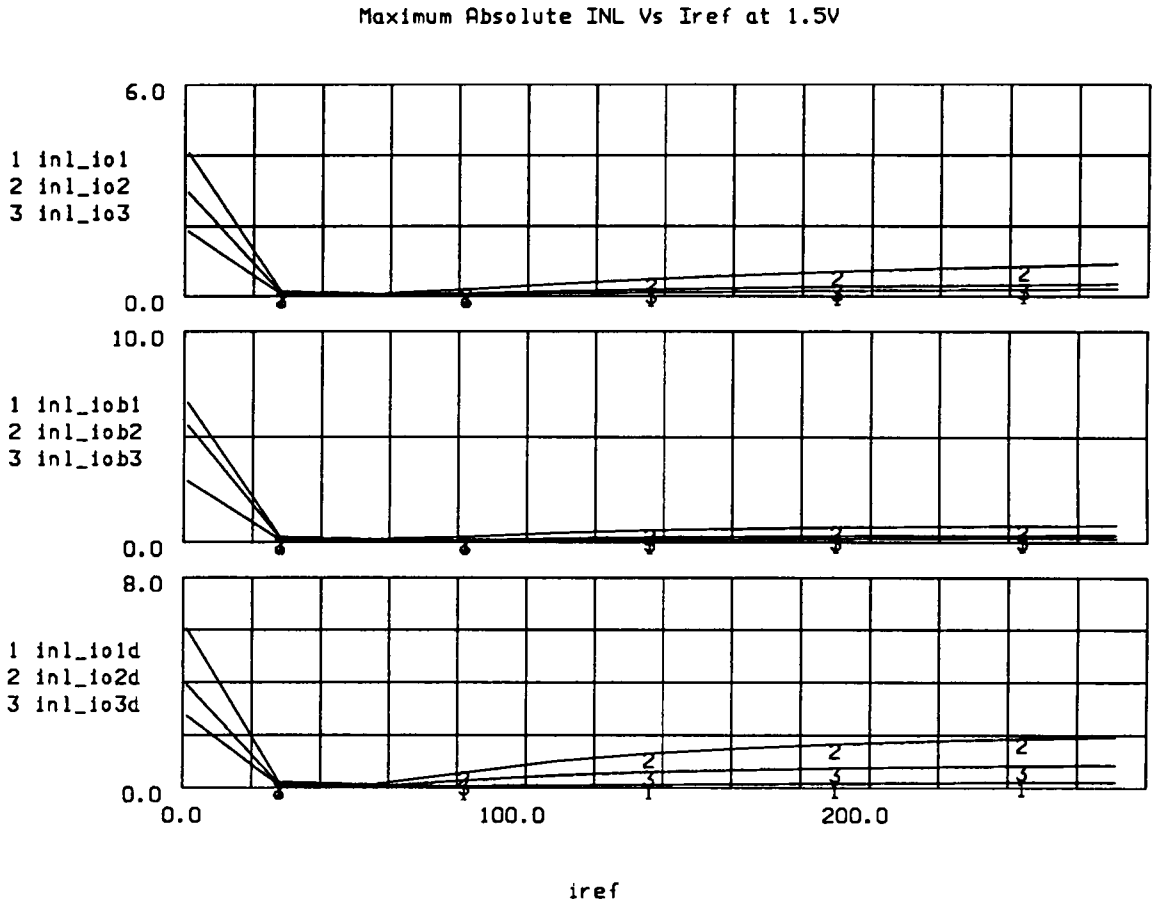

Figure 5.4: Maximum integral non-linearity plotted versus reference current of each chip at $V_{out} = 1.5V$

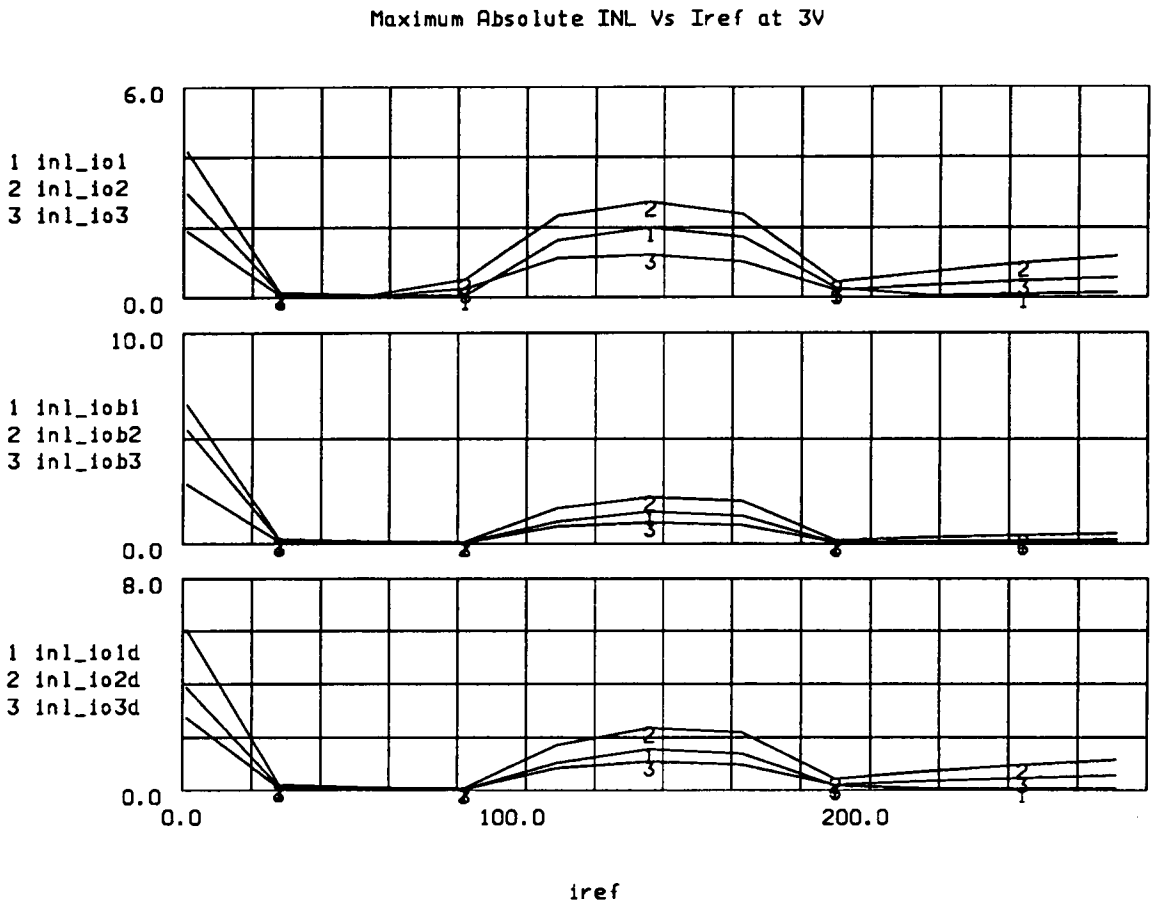

Figure 5.5: Maximum integral non-linearity plotted versus reference current of each chip at $V_{out} = 3V$

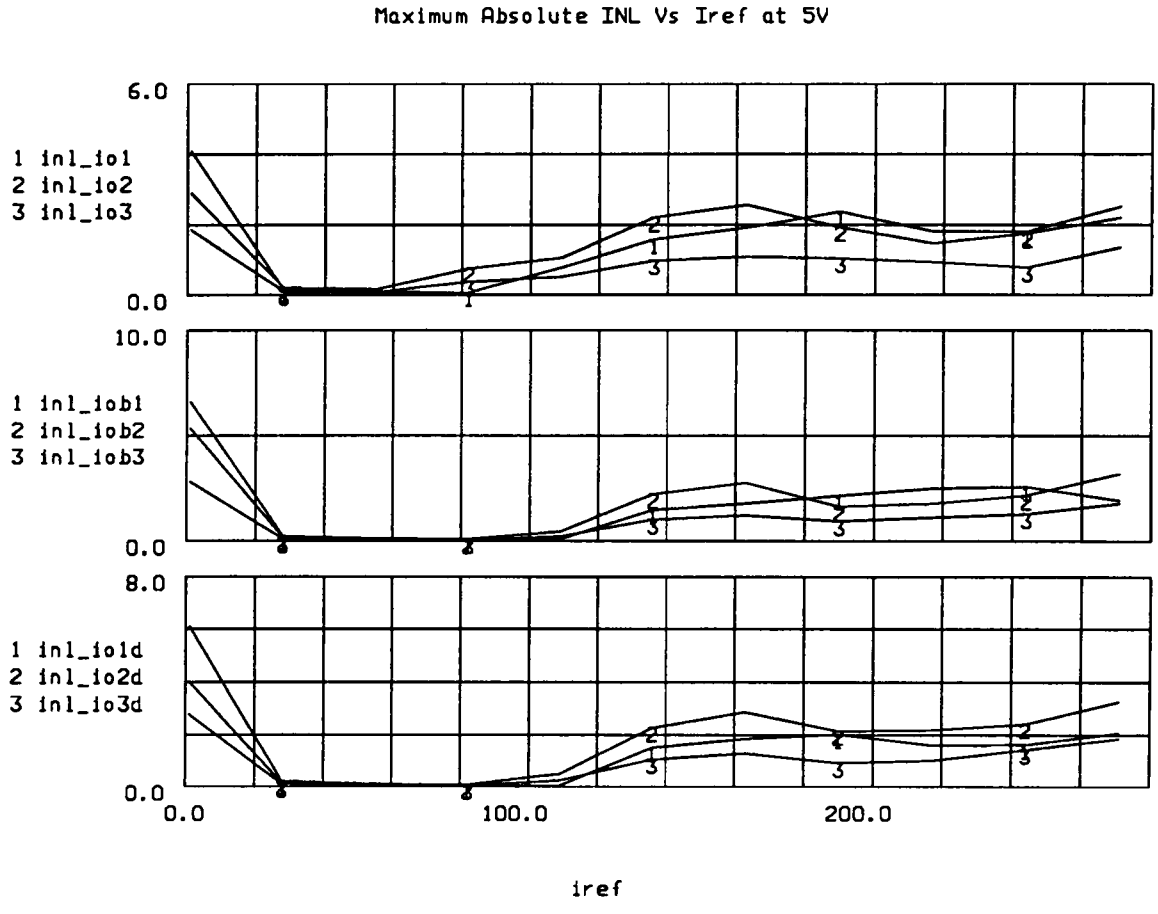

Figure 5.6: Maximum integral non-linearity plotted versus reference current of each chip at $V_{out} = 5V$

versus I_{ref} for Chip1, Chip2, and Chip3. The second set of curves represents the maximum INL of $\overline{I_{out}}$ versus I_{ref}. The bottom set of curves shows the maximum INL of $(I_{out} - \overline{I_{out}})$ versus I_{ref}. To summarize the INL results, it is evident that the current DAC has Integral Linearity of better than $\pm$1LSB at currents ranges between 28 and 109 μA. Even at higher currents than the $I_{out(max.)}$ range, as long as the output voltages are lower, the DAC will have less than $\pm$1LSB INL.

Therefore, integral and differential nonlinearity were found to be $\pm$1LSB over the current range of 28 to 130 μA, and output voltage of 1 to 5 V. Based on this, the implemented DAC will have good performance over these voltage and current ranges.

The DACs AC performance was not measured due to nonfeasibility for measuring output current pulses directly without converting the DAC's output to voltage by either resistor(s) or opamp(s).

Further work needs to be done in investigating the AC performance and to design input buffers to switch the DAC at high speed with minimum glitch energy.

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BIBLIOGRAPHY

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APPENDICES

APPENDIX A

SPICE Deck Used for the Simulation of Minimum Output Voltage

```
vout_min.cki

.options ucb

.options map oneconn reltol=1p

M1    %iref %iref  0   0 nfet  L=10U W=10U

M2    %d2   %iref  0   0 nfet  L=10U W=10U

M3    %io   %a0    %d2 0 nfet  L=2U  W=10U

M4    %iob  %a0b   %d2 0 nfet  L=2U  W=10U

vbias %bias 0 dc=0

vio    %bias   %io  dc=0

viob   %bias   %iob dc=0

iref 0 %iref dc=sweep(1u,301u)

.dc vbias 0 5 0.1

.sample 61

va0 %a0   0 dc=5

va0b %a0b 0 dc=0

.post dc i(all)

.include model.N02T

.end
```

```
*N02T SPICE LEVEL 2 PARAMETERS


.model nfet nmos
+ level=2 ld=0.250000u tox=407e-10 nsub=6.289058e+15
+ vto=0.779117 kp=5.167e-5 gamma=0.5385  phi=0.6
+ uo=608.8  uexp=0.132101 ucrit=32110.5 delta=2.78717
+ vmax=60367.3 xj=0.25u lambda=3.503483e-2 nfs=4.387229e+12
+ neff=1 nss=1e+12 tpg=1 #rsh=27.400000
+ cgdo=3.181644e-10 cgso=3.181644e-10  cgbo=5.524552e-10  cj=1.008e-4
+ mj=0.6448 cjsw=6.369e-10 mjsw=0.3454 pb=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.43um
.model pfet pmos
+ level=2 ld=0.216440u tox=407e-10 nsub=7.113789e+15
+ vto=-0.77632  kp=2.210e-5 gamma=0.5728  phi=0.6
+ uo=260.5   uexp=0.296141 ucrit=33335.2 delta=4.383185e-5
+ vmax=34955.1 xj=0.05u lambda=5.714336e-2 nfs=1.000000e+11
+ neff=1.001 nss=1e+12 tpg=-1 #rsh=88.400000
+ cgdo=2.754540e-10 cgso=2.754540e-10
cgbo=6.116211e-10   cj=2.451e-4
+ mj=0.5473 cjsw=2.971e-10 mjsw=0.3131 pb=0.800000
```

```
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.19um


*M97Q  SPICE LEVEL 2 PARAMETERS

.MODEL nfet NMOS LEVEL=2 LD=0.250000U TOX=381.000000E-10
+ NSUB=2.433000E+16 VTO=0.918934 KP=5.528000E-05 GAMMA=0.9816
+ PHI=0.6 UO=609.9 UEXP=0.235428 UCRIT=129971
+ DELTA=2.36199 VMAX=88054.1 XJ=0.250000U LAMBDA=2.204500E-02
+ NFS=2.575788E+12 NEFF=1 NSS=1.000000E+12 TPG=1.000000
* RSH=21.170000
+ CGDO=3.398764E-10 CGSO=3.398764E-10 CGBO=6.737632E-10
+ CJ=3.967000E-04 MJ=0.467900 CJSW=5.189000E-10 MJSW=0.404600 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 0.02 um
.MODEL pfet PMOS LEVEL=2 LD=0.225770U TOX=381.000000E-10
+ NSUB=4.807000E+15 VTO=-0.774249 KP=1.957000E-05 GAMMA=0.4407
+ PHI=0.6 UO=215.887 UEXP=0.113346 UCRIT=5004.07
+ DELTA=2.542239E-04 VMAX=44039.1 XJ=0.250000U LAMBDA=4.975166E-02
+ NFS=1.000000E+11 NEFF=1.001 NSS=1.000000E+12 TPG=-1.000000
* RSH=70.480000
+ CGDO=3.069355E-10 CGSO=3.069355E-10 CGBO=6.946509E-10
```

```
+ CJ=1.983000E-04 MJ=0.402400 CJSW=2.985000E-10 MJSW=0.342600 PB=0.700000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 0.10 um


*M98X  SPICE LEVEL 2 PARAMETERS


.MODEL nfet NMOS LEVEL=2 LD=0.198730U TOX=410.000000E-10
+ NSUB=2.409000E+16 VTO=1.00626 KP=4.451000E-05 GAMMA=1.0618
+ PHI=0.6 UO=557.94 UEXP=0.302096 UCRIT=167069
+ DELTA=1.76363 VMAX=100000 XJ=0.250000U LAMBDA=6.333964E-02
+ NFS=6.793426E+11 NEFF=1 NSS=1.000000E+12 TPG=1.000000
* RSH=21.730000
+ CGDO=2.510646E-10 CGSO=2.510646E-10 CGBO=6.628741E-10
+ CJ=4.010000E-04 MJ=0.450500 CJSW=5.460000E-10 MJSW=0.378500 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 0.03 um
.MODEL pfet PMOS LEVEL=2 LD=0.250000U TOX=410.000000E-10
+ NSUB=4.988037E+15 VTO=-0.7303 KP=2.343000E-05 GAMMA=0.4831
+ PHI=0.6 UO=278.2 UEXP=0.14205 UCRIT=5200.88
+ DELTA=4.773721E-03 VMAX=42517.9 XJ=0.250000U LAMBDA=5.593900E-02
+ NFS=1.887233E+12 NEFF=1.001 NSS=1.000000E+12 TPG=-1.000000
* RSH=68.810000
```

```
+ CGDO=3.158363E-10 CGSO=3.158363E-10 CGBO=6.228821E-10
+ CJ=1.865000E-04 MJ=0.403300 CJSW=2.872000E-10 MJSW=0.349500 PB=0.700000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.14 um
```

APPENDIX B

SPICE Deck Used for the Simulation of Maximum Output Current

```
Iout(max) of Chip - SPICE Model N02T

.options ucb

.options map oneconn reltol=1p

M1    %ref %ref  0    0 nfet  L=10U W=10U

M2    %d2   %ref  0    0 nfet  L=10U W=10U

M3    %io   %a0    %d2 0 nfet  L=2U  W=10U

M4    %iob  %a0b   %d2 0 nfet  L=2U  W=10U

vbias %bias 0 dc=5

vio    %bias   %io  dc=0

viob   %bias   %iob dc=0

iref 0 %ref dc=250u

.dc iref 1u 501u 10u

va0 %a0   0 dc=5

va0b %a0b 0 dc=0

.post dc i(all)

.include model.N02T

.end
```

APPENDIX C

SPICE Deck Used for AC Simulation of the Unit Cell

```
AC Simulation of a Unit Cell  - SPICE Model N02T
.options ucb
.options map oneconn reltol=1p
M1    %iref %iref  0   0 nfet  L=10U W=10U
M2    %d2   %iref 0   0 nfet  L=10U W=10U
M3    %io   %a0    %d2 0 nfet  L=2U  W=10U
M4    %iob  %a0b   %d2 0 nfet  L=2U  W=10U
vbias %bias 0 dc=5
vio    %bias   %io  dc=0
viob   %bias   %iob dc=0
iref 0 %iref dc=sweep(1u,271u)
.sample 11
va0 %a0   0 dc=5 pulse(0 5 20n 2n 2n 20n 65n)
va0b %a0b 0 dc=0 pulse(5 0 20n 2n 2n 20n 65n)
.tran 1n 65n
.post tran i(all)
.include model.N02T
.end
```

APPENDIX D

SPICE Deck Used for the Simulation of Output Impedance

```
Output Impedance of a Unit Cell (rout) - SPICE model N02T

.options ucb

.options map oneconn reltol=1p

M1    %iref %iref  0    0 nfet  L=10U W=10U

M2    %d2   %iref  0    0 nfet  L=10U W=10U

M3    %io   %a0    %d2  0 nfet  L=2U  W=10U

M4    %iob  %a0b   %d2  0 nfet  L=2U  W=10U

vbias %bias 0 dc=5 AC=1

vio    %bias   %io  dc=0

viob   %bias   %iob dc=0

vg %iref 0 DC=sweep(1,5)

.sample 100

.ac DEC 10 100 100K

va0 %a0   0 dc=5

va0b %a0b 0 dc=0

.post ac i(all)

.include model.N02T

.end
```

VITA

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Mrs. Horner was treasurer of the University of Tennessee student branch of the IEEE from 1987 to 1988, and the chairman of the Baha'i Club of the University of Tennessee, Knoxville from 1987 to 1989. She was married to Jim G. Horner on June 30, 1990.

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