

**Genetic Algorithm Based Design and Optimization
Methodology of a 3D Printed Power Module Packaging**

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Dedication

This dissertation is dedicated to the most precious people in my life:

To my wife, Qiuyi Li and my princess, Nuoyi Wu,
for the best gifts, I have ever gotten.

And to my parents,
Zhijia Wu and Huizhu Liu
for the warmest and strongest support all the time.

Acknowledgment

I would like to take this opportunity to thank many people who have been supporting me for the last five years throughout my Ph.D.

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Abstract

Power electronics design is an interdisciplinary research. Enhancing power density became more and more critical to the converter system-level design. Within a power electronics converter, two major components, i.e. cooling system and passive components, dominate overall power density. As stated in Liebig's barrel theory, the overall performance of a power converter is limited by the “shortest board”. For a high-power density converter design, considerations should not only focus on the electrical domain but also on the packaging design, including thermal domain, parasitic domain, semiconductor property, reliability and other aspects.

Design of power module packaging is the key to achieve the high-power density goal since it covers most of the interdisciplinary design domains. As an integration solution, it provides the physical containment of multiple semiconductor devices, with pre-layout sintered on substrates, covered by electrical encapsulation and mounted on the cooling system. Impacts brought by the power semiconductor technology, especially with the use of wide band gap power devices have shown significant improvements in power density. Ideally, features such as higher switching frequency, the higher operating temperature could lead to a more volumetrically efficient module design. However, the conventional packaging design methods are not keeping the pace with the semiconductor development and posing challenges for new technology realization.

In this dissertation, the multi-objective optimization algorithm based on genetic algorithm (GA) is constructed. Finite element analysis (FEA) based evaluation is embedded in the algorithm through the co-simulation interface to ensure the accuracy.

Three major targets, i.e. thermal performance, parasitic inductance and operating points, are being optimized. While the GA generates a population of design candidates in each iteration, a sequence of evaluations is proceeded and assign the fitness value to each candidate. With an approach that follows the rule “survival of the fittest”, this optimization process evolves automatically based on the “learned” design strategies of the previous generations. This process can converge within a short time and leads to a superior performance compared to the conventional design power modules. Due to the potential complexity of the optimized result, 3D printing with complexity free property is used for constructing prototypes packaging.

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1. Introduction

1.1. POWER ELECTRONICS CONVERTER

Power electronics converter has become a basic need of modern industrial and residential applications. Nowadays, power electronics devices and systems are widely used in various fields including, industrial, residential, transportation, utility, and aerospace. It acts as an interface by controlling and converting the flow of electrical energy from one type of source to another type. [1, 2] The power levels of converters range from Milli-Watts of implantable biomedical devices to several Mega-Watts of power system transmission applications. Besides both extreme cases, most power levels of power electronics applications are ranging from few Watts to few Kilo-Watts, as can be seen in daily life.

Began with the appearance of power semiconductor devices, first modern power electronics converter was built back to the 1950's. Since then, rapid developments in devices, circuit topologies, controls, and packaging technology significantly improved the power converter performance and pushed the application limitation further and further. As the close relationship to the industrial, power electronics is an application-driven research. Meantime, the semiconductor devices development is an “enable” technology to meet such application-based motivation. As most of the basic needs have been achieved by nowadays power electronics converters, research focus is now driven by the need for higher efficiency, lowering cost and enhanced reliability [3].

As the “enable” technology, development in wide band gap (WBG) devices has offered new opportunities for innovative designs. WBG devices, such as SiC MOSFETs, SiC Schottky diodes, and GaN FETs have shown overwhelming advantages compared to the Silicon-based devices. Beneficial properties by replacing Silicon-based devices to WBG device include:

- The higher critical electrical field is obtained compared to that of Si. Higher breakdown voltage can be achieved with an even thinner device structure. Advantages are found in both low $R_{ds(on)}$ value and high voltage rating.
- Higher thermal conductivity reduces the thermal resistance of the device (junction to case), leading to a lower junction temperature.
- More than twice higher current density can be achieved.
- The WBG material can hold the hot spot’s temperature over 300°C, which potentially allows a higher operating junction temperature.

The combination of such beneficial properties can result in a significant potential performance improvement and realize new power converter design that is not even possible to achieve as of the state of art. However, to fully utilize the desired features of WBG devices, an advanced power module packaging design is equally important to the device development. As an interdisciplinary research, design of power electronics system should involve, but not limited to topics:

- Power Semiconductor Devices
- Electromagnetic
- Electrical Circuit

- Heat Transfer
- Mechanical Design

To target aspects mentioned above, the conventional power electronics design procedure, as summarized in Fig. 1-1, this overall structure includes multiple discrete design steps. Generally speaking, the design is initiated by picking up the suitable circuit topology based on the application, e.g., traction drive, solar inverter, DC charger. Each switch position of the topology is then replaced by available devices/module with desired ratings. Type and modeling of the switch device are then implemented in the circuit simulation software. With operating spec parameters input, the circuit simulation is performed and switching behaviors including the losses information are generated. The cooling system is then designed by either thermal equivalent circuit (TEC) or finite element analysis (FEA) method to limit the junction temperature. At the same time, parasitic elements are extracted in another step to make sure safety operating conditions. If both thermal and electrical performance meets the desired targets, hardware implementation including PCB layout and assembly is performed for experimentally test of prototyping design.

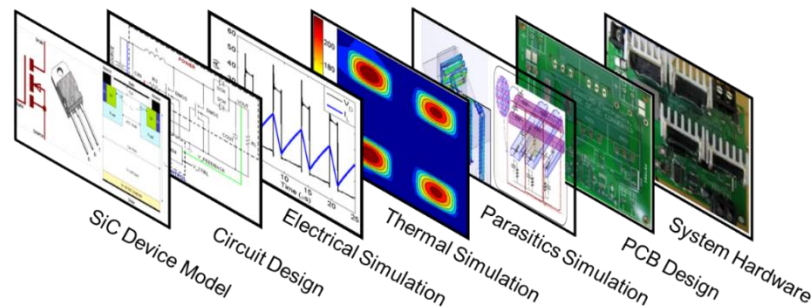


Fig. 1-1. Conventional power electronics design procedure [5]

Though varied by the designs, the order of steps may change, a complete research project should always include engineers with such multiple disciplines research background. As one of the design steps, the power packaging design approach, as illustrated in Fig. 1-2, is straightforward in this step-by-step structure.

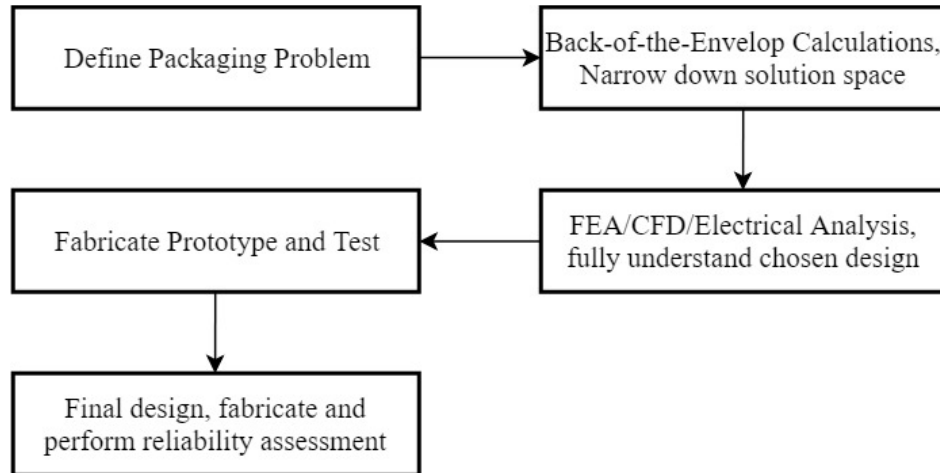


Fig. 1-2. Power electronics packaging design approach [6]

As a linear process, it delivers the designed parameters to the forward step met the design spec. Otherwise, an iterative loop shows up and take the backward step(s) to modify the previous designs. Following this design procedure, innumerable power electronics converters have been designed during the past decades with significant enhancement in performance revealed. However, the recent development of the power electronics industry seems to hit the limit while less and less improvement can be acquired. Among all desired improvements, power density, as one of the key contributors to either overall efficiency or marketing/ product requirement, has drawn significant research effort recently.

1.2. SIZE, WEIGHT, and POWER (SWaP) OPTIMIZATION

In recent years, the trend of power electronics research target shifts towards compact products design for a small, lightweight electronic systems that will consume less power, especially in applications with limited volume/weight, such as the applications of aerospace, airplane, defense electronics, and hybrid electric vehicles. In those cases, overall efficiency is highly dependent on the power density due to the limited space and allowed weight. Three objects, Size, Weight, and Power are qualified as SWaP parameters, to determine the quality of such compact design [7]. SWaP in power electronics design is usually interpreted as power density, defined as the amount of power per unit volume/ per unit weight. The increase in power density is desired by industrial. For example, in the traction drive system of an electrical vehicle, a power density increases of 843% is required by DOE as the R&D target of the year 2025 [8].

According to the analysis report of Nissan LEAF, the breaking down the percentage of the components' power density contributions in a powertrain is listed in Table 1-1.

Table 1-1. Power density contributions of major components [9]

Components	Percentage
Cooling System	37%
Power Modules	23%
Housing	15%
Capacitors	12%
Bus Bars	7%
Current Sensor	6%

As it can be noted, the major three electrical related components, cooling, power module and capacitors have taken most of the contributions. It is also true for most of the general power converters, as the power stage shown in Fig. 1-2. To further optimize power density, optimization effort on those three components of power converter should be addressed on. Individual effort of each target has been made to push the power density limit:

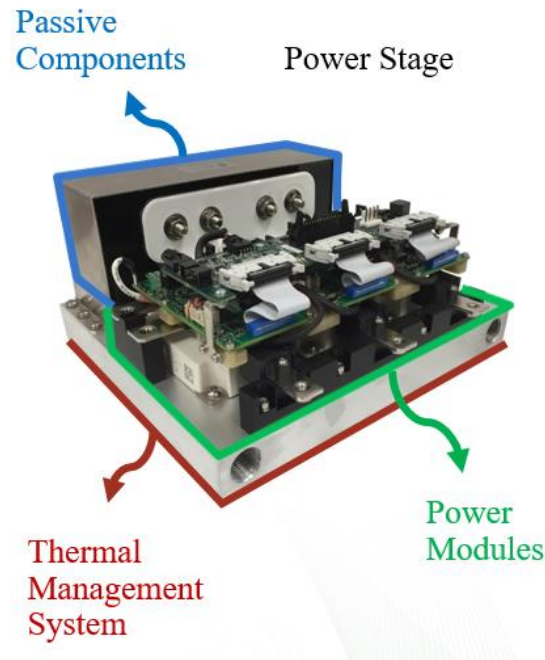


Fig. 1-3. Major components of a power stage

Optimizations on the thermal management system have been mostly done by mechanical engineers. Approaches based on either fundamental heat transfer equations or finite element analysis (FEA) method have been made for the optimal cooling system structure, i.e. heat sink design. The ability to dissipate heat losses, usually referred as the thermal resistance, is the main target to be optimized. By enabling a better thermal

performance, either the size of the cooling system can be reduced, or the junction temperature of devices will be lower.

Optimization of power modules most of the time is the duty of the device manufactures. The design of power module is based on the circuit schematic, e.g. half-bridge module, three-phase module and their rated parameters. Devices are placed on the substrate in parallel with electrical interconnections. The layout of devices and the substrate routing could make a huge difference on the module performance, i.e. the parasitic inductance. An optimized devices layout strategy will result in a lower parasitic inductance value, or a smaller package footprint.

Optimization of passive components is relatively complex. To get a good passive design, fundamental rules and formulas of electromagnetic, thermal and electrical should be all considered. The value/ size of the passive filter components, e.g., inductor and capacitor, are determined by what bandwidth they are designed to filter out. Generally speaking, the higher frequency noise, the smaller inductance or capacitance value are needed. As the filter inside a power converter, increase in switching frequency can reduce the its size.

As state of art, innumerable approaches have been proposed for the last decades targeting on either aspect individually. However, single-objective optimization as of most of case, didn't consider the negative impacts on the other objectives. As higher power density design target, balancing of multiple tradeoffs existing in objectives is more critical than the single-objective optimization. Co-design/ Co-engineering design considering the electrical, thermal and mechanical domains all together should be taken into consideration for further SWaP optimization.

1.3. TRADEOFFS IN SWaP OPTIMIZATION

Nowadays, the optimization of power converter systems more and more becomes a “multi-domain” task. Benefits brought by single-objective optimization might be overwhelmed by the drawbacks of other components. For example, a power module designed to put devices side-by-side for a small power loop, which is beneficial to the parasitic inductance reduction. However, the significant thermal coupling effect could result in a terrible a thermal performance. Major power density contributors of a power electronics system have been categorized into three domains:

- “Thermal” domain, mainly determined by the cooling method and the heat sink structure design.
- “Parasitic” domain, mainly determined by the device layout locations and the substrate routing.
- “Operation” domain, in this dissertation, refers to the optimal switching frequency that can minimize the passive components size.

Interactions and tradeoffs among three domains are illustrated as Fig. 1-4.

The first tradeoff locates between the “Thermal” domain and the “Parasitic” domain. The balance factor of this tradeoff is the separating distance of devices. On one hand, if devices are placed close to each other, severe thermal coupling issue could elevate the junction temperature, increase the need of a larger cooling system. On the other hand, a far separation could eliminate this thermal coupling issue. However, large commutation loop is formed by upper and lower devices under the transient period, leading to a huge parasitic inductance that will introduce high overshoot voltage spike during device turn-off transient.

To compensate this issue, a reduced switching speed is required that will increase the switching loss and potentially limit the switching frequency.

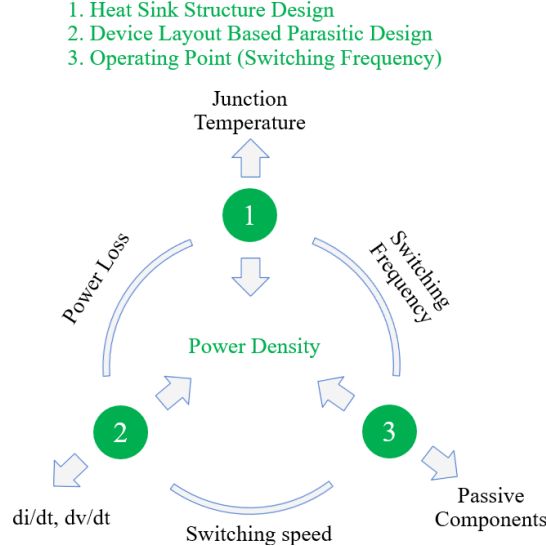


Fig. 1-4. Tradeoffs among three major domains

The second tradeoff locates between the “Thermal” domain and the “Operation” domain. Passive components, as one key contributor to the SWaP optimization, can be reduced by applying higher switching frequency. To efficiently filter out the undesired switching noise, the cutoff bandwidth of the passive filter, determined as Eq. 1-1 and Eq. 1-2 is usually selected as 1/10 of the switching frequency.

$$f_{cutoff} = \frac{1}{2\pi\sqrt{LC}} \approx f_{sw}/10 \quad \text{Eq. 1-1}$$

$$LC = \left(\frac{5}{\pi \cdot f_{sw}}\right)^2 = \frac{C}{f_{sw}^2} \quad \text{Eq. 1-2}$$

Approximately, the value of either L and C is can be modeled as inverse proportional to the switching frequency. This relation indicates one of the approaches to reduce the passive

components, that is to switch at a higher frequency. However, the switching loss, as a linear function of switching frequency, increases with the reduction of passive components. Extra loss aggravates the thermal stress of the power device, and lead to a larger cooling system.

The third tradeoff locates between the “Parasitic” domain and “Operation” domain. As an approximated relation, the need for higher switching frequency will potentially require a faster switching speed, di/dt . Overshoot voltage, on the other hand, is impacted by the switching speed as shown in Eq. 1-3.

$$V_{overshoot} = L \frac{di}{dt} \quad \text{Eq. 1-3}$$

If a higher switching speed is employed, the higher overshoot voltage caused by it could damage the device. This scenario is common to see in the applications such as an electric airplane, where an extremely high switching speed is needed for a lighter EMI filter.

Fig. 1-5 has illustrated the tradeoffs impacts on the power module volume optimization. Near both sides, though one individual target is doing well, the overall performance is bad. The optimal point, which is the valley of the green line, locates at a balanced region where tradeoffs are compromised. The method of approaching this valley point, is the main focus of this dissertation.

Other parameters, such as the DC link voltage, switching speed di/dt could also introduce other tradeoffs during the SWaP optimization. However, due to the page limit of this dissertation, these parameters are out of scope. Instead, they are treated as pre-designed constant parameters and will be involved in the future works as addition to the present structure.

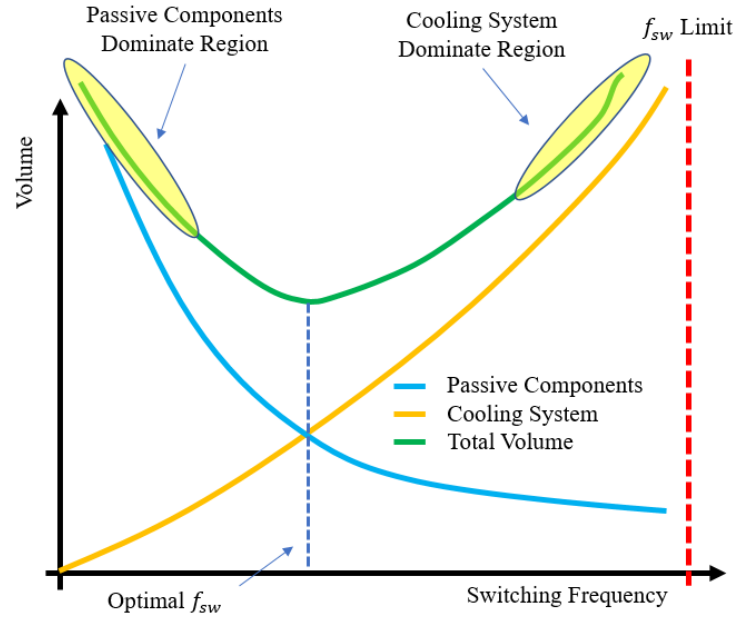


Fig. 1-5. Multiple tradeoffs impact on the overall volume minimization

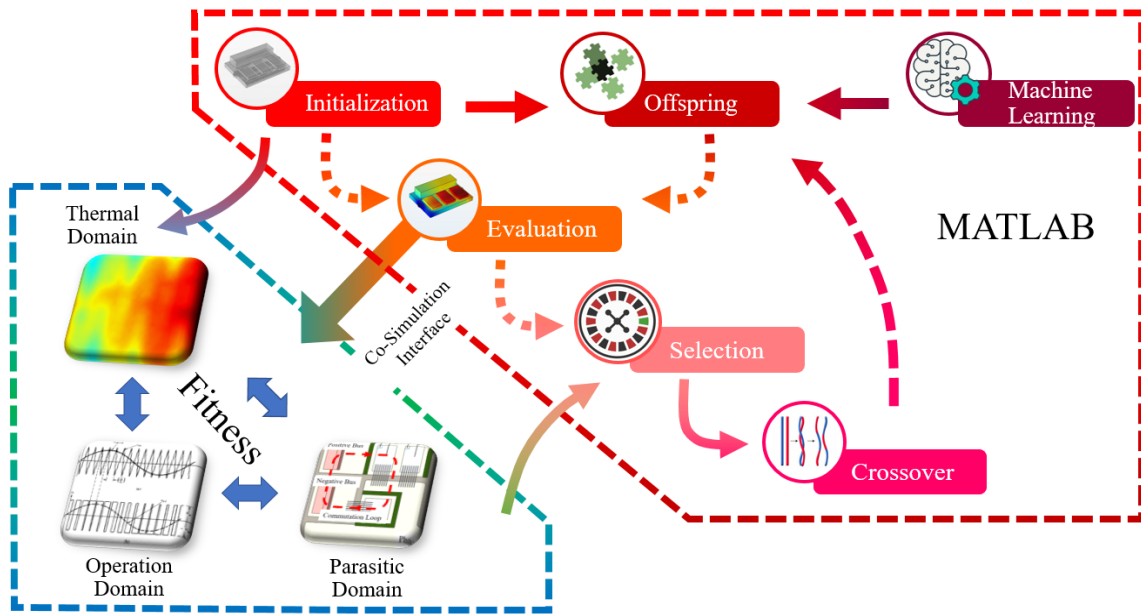


Fig. 1-6. Multi-objective optimization configuration

1.4. MULTI-DOMAIN EVALUATION STRUCTURE

A multi-objective optimization method, taking device layout, heat sink structure and the operating point into consideration is proposed in this dissertation.

The main algorithm is coded in MATLAB based on Genetic Algorithm (GA). It is an optimization engine that imitates the natural evolution process proposed in the Darwinian evolutionary theory. Each design is presented as a set of design parameters, named “chromosomes”. By evaluating chromosomes of each individual, the fitness score is assigned and used as a reference to qualify the performance. Designs with better performance have a higher chance to “heritage” parts of its design features to the next generation. By this way, algorithm itself can learn the beneficial design traits automatically.

As of each individual, how to evaluate its design quality will highly impact the optimization accuracy. Since more than one domain are involved in the evaluation, the linear structure as constructed by discrete steps is no longer efficient. To consider all interactions between domains, a multi-domain evaluation method is proposed as Fig. 1-7.

This structure includes three domains as one entirety.

The first domain, thermal domain, located on the left-hand side of the flowchart. For any qualified heat sink design and the device layout design input to the top of the, FEA simulation is studied based on pre-set boundaries conditions, including power loss of each device, fan/ pump parameter, material properties, flow physics type and mesh algorithm. Useful information, such as junction temperature profile is extracted from the simulation results. Those profiles are then linked to the other domains as input parameters.

loop is to determine the optimal switching frequency of this given design. For each operation point updated in the loop, the switching loss is updated in the parasitic domain and the junction temperature is updated in the thermal domain. The iterative loop continues until the max allowed junction temperature is reached. The optimal switching frequency then contributes to the fitness score.

All mentioned processes above have to be totally automatic, due to the complexity of this iterative flowchart and the large solution space. To enable continuous operation, save computation time and apply the machine learning features, co-simulation interfaces link all domains for interact processes is developed.

1.5. AUTOMATIC CO-SIMULATION INTERFACE

Iterative method[10], as defined in Wikipedia, is a “mathematical procedure that uses an initial guess to generate a sequence of improving approximate solutions for a class of problems”. Computation effort of iterative problem is extremely heavy since thousands of sequences need to be evaluated. This situation becomes even worse with the involvement of FEA simulations. As a well-known phrase raised by Benjamin Franklin, “Time is Money!”. The time usage of researchers and engineers in a research facility is one major cost during the research and development process. As a conventional design, either the quality of the design is reduced by limiting the total number of iterations, or the R&D cost will increase by taking additional revisions. To ease this quality-cost tradeoff, the unsupervised iterative process without the need of human labor involved is an ideal approach.

Inspired by the self-evolve capability of the machine learning based algorithms, such as Alpha-Go algorithm, similar approach is proposed for power module design based on GA. In the evaluation step of GA, one of the biggest challenges in the using of FEA simulations. Normally, most of the geometry construction and boundary condition settings are performed through the graphic user interface (GUI) manually. Interface constructed in this dissertation is to take over all manually processes and let the code “communicate”, and automatically extract and deliver information through all domains.

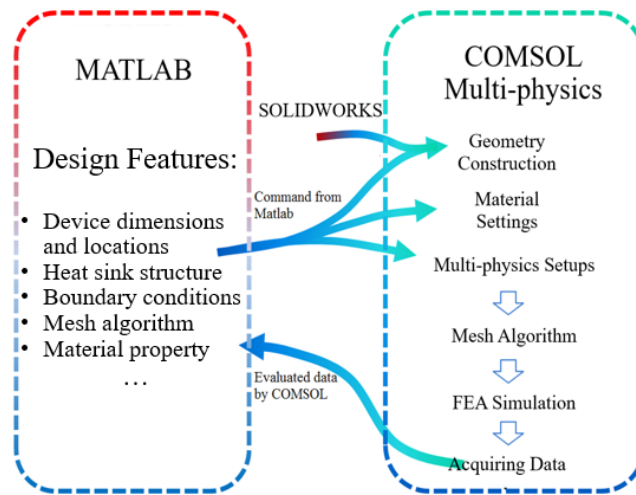


Fig. 1-8. Developed co-simulation interface

As shown in Fig. 1-8, the major function of FEA co-simulation interface is built in between MATLAB and COMSOL, where the design parameters are constructed based in MATLAB while most of the evaluations are performed in COMSOL.

This interface is the key to achieve benefits and computation power brought by Genetic Algorithm. Detailed information will be illustrated in the later chapters.

1.6. CONTAINS OF DISSERTATION

The objective of this dissertation is to develop a multi-objective optimization method for a high-power density power electronics module and packaging. As of this method, design tradeoffs are firstly pointed out which haven't been perfect solved as the art of state. An overall optimization and evaluation structure on these tradeoffs is then proposed as a solution. For each domain of the structure, individual optimization method is developed as a gear to the overall chain. With all components of the optimization structure, a multi-objective optimization case is studied using the proposed method.

Chapter 1 gives a whole scope of what will be proposed in this dissertation and the motivation to do so.

Chapter 2 firstly explains the detailed reason why the problem raised in this dissertation are important and have to be solved. Then, literature reviews about what researches have done as the art of state is listed with references. Drawbacks of some referred work are also analysis.

Chapter 3 provides the fundamental supports of the proposed works in this dissertation, including the basis of FEA simulation, Genetic Algorithm and the automatic co-simulation interface construction.

Chapter 4 discusses the whole picture of the optimization method and the brief introduction of each block function shown in the flowchart.

Chapter 5 focuses on the thermal design approaches, as named "Thermal Domain". Varied approaches in terms of heat sink types and initialization methods are proposed and

design cases of each method is studied and analyzed. Comparisons to the commercially available heat sink are also included in this chapter.

Chapter 6 explains the method for optimizing parasitic parameters, named as “Parasitic Domain”. As a “GA-enable” domain, detailed instructions about GA based layout design revision and study process are listed as step-by-step.

Chapter 7 covers the method of approaching the optimal operating switching frequency of the power module, named as “Operation Domain”. This sub-iterative process takes the advantage of the proposed MTEC network and coded in MATLAB as the last gear of whole optimization chain.

Chapter 8 performs a multiple-objective optimization design case by putting all domains together as one entirety and taking power density as the design goal. An overall summary of this work is also presented with future works that could additional function to this present work.

2. Research Background and Literature Review

2.1. THERMAL DOMAIN

2.1.1. Losses of power module

Power loss is inevitable during power electronics converter operation, according to the first law of thermodynamics. Normally, losses in the devices can be categorized into two major parts, switching losses and conduction losses, as shown in the waveform of Fig. 2-1. Switching losses are generated during state transient period, which device is switching during the conducting state to the blocking state or vice versa. Due to the limited switching speed of the device, the current through the device and voltage across the device, have an overlapped period during turn-on and turn-off transients. For each switching behavior, energy loss, proportional to the product of the peak current, voltage and the switching time will be dissipated once.

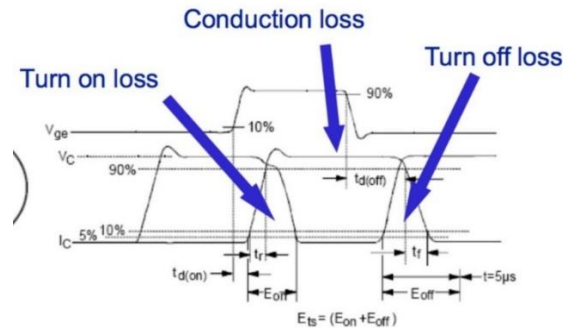


Fig. 2-1. Losses in power electronics module

Additional losses, such as hard switching loss due to the stored energy in the device body capacitances and reverse recover loss due to the property of the diode can also be counted as the switching losses. The total switching loss of one switch period is the sum of the turn-on and turn-off energy losses. The switching loss of the device is the product of the switching frequency and the total energy dissipation per switching period. That is to say, the switching loss is proportional to the switching frequency of the device.

Conduction losses, on the other hand, occur when the device is conducting current. According to the Ohm's law, Joule heating will dissipate energy with the electric current passing through the conductor. Stated by the Joule's first law that, the power dissipation generated by the conduction equals the product of the conductor resistance and the square of the current magnitude, as shown in the Eq. 2-1.

$$P = I_{\text{RMS}}^2 \cdot R_{\text{ds(on)}} \quad \text{Eq. 2-1}$$

The actual calculation of the conduction loss is based on its duty cycle of the topology and control strategy of the power electronics module, which equals to the product of the square of the RMS current flowing through the device and the on-state resistance of the device. For applications, especially with high rated currents, the square of the current contributes to a significant amount of the product value even with the low on-state resistances brought by advanced semiconductor devices.

2.1.2. Importance of junction temperature

Power losses of the device will eventually result in the temperature increase. Junction temperature is used in the power converter to represent the internal energy of the semiconductor devices. Temperature, in terms of thermodynamics, is defined based on the

magnitude of the molecules' movement. Energy dissipated by the devices transfers to the material molecules and increases the average velocity of the carriers. If keeping accumulating the internal energy, the active thermal motion of the carriers eventually reaches the same level of the electronic conduction and break down the semiconductor voltage blocking capability. High leakage current due to the high carrier motion will eventually damage the device and leads to the system failure. Thermal runaway, as one of the most common causes of the temperature-related failure often happens during the operation due to the increase in temperature higher than the thermal management capability of the system. This mismatch results in a vicious spiral to the destructive result. Eventually, the semiconductor device will be damaged.

Compared to the silicon-based devices, higher temperatures can be achieved by implementing WBG devices with the advanced material property. For example, SiC bare dies can withstand at least 300°C. However, the junction temperature of the module is still limited below 175°C, due to the thermal concerns about other components, such as solder, inductor, capacitor and module packaging.

Besides the thermal runaway issue, the long-term failure rate of the power module also relates to the operating junction temperature. As shown in Fig. 2-2, the device failure rate increases exponentially with rising of junction temperature[11]. Temperature-related failure modes include thermal expansion mismatch, thermal stresses caused by thermal cycling and the rating degradation of the devices.

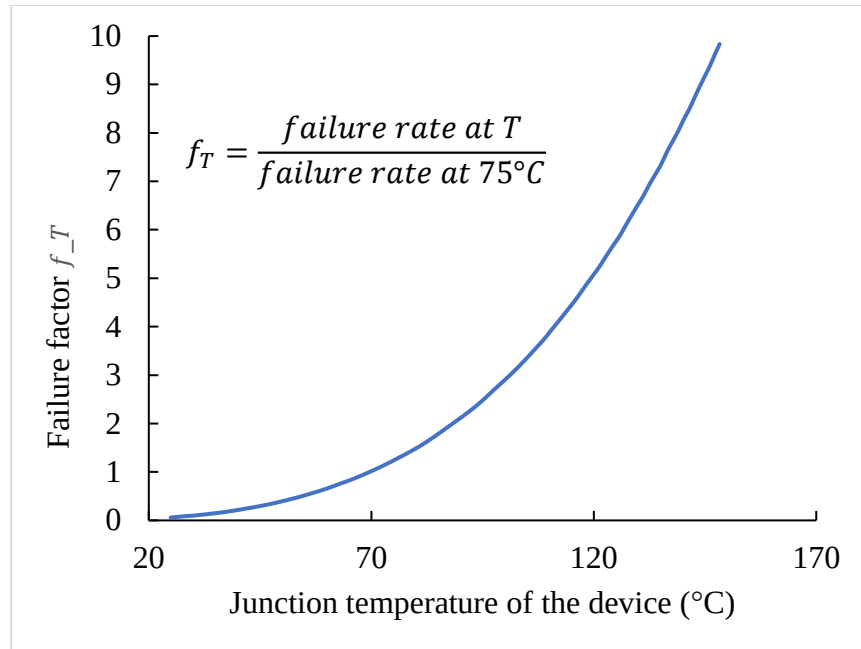


Fig. 2-2. Failure rate vs. junction temperature[11]

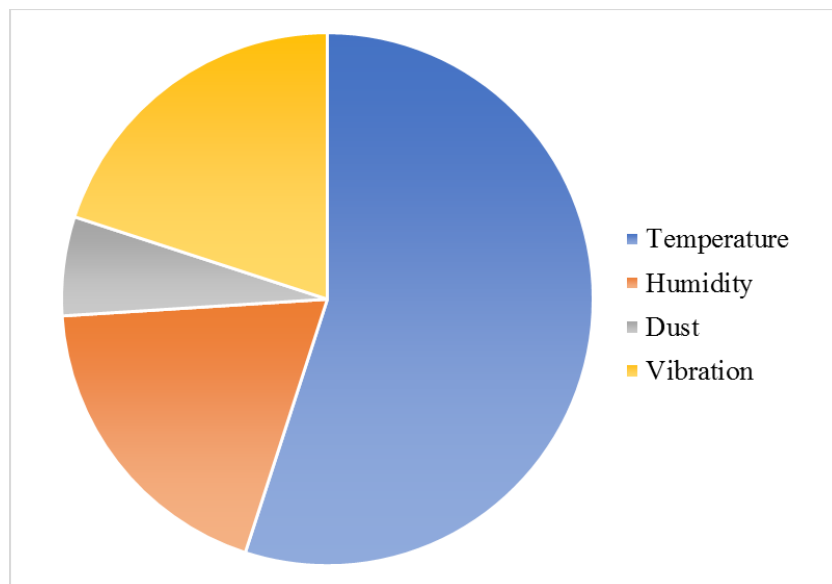


Fig. 2-3. Major causes of the power electronics module failure[12]

As shown in the Fig. 2-3, more than half of the electronics failure due to the temperature issues. To maintain a low-level temperature profile, a thermal management system is necessary for the power electronics application to dissipate adequate power loss from the devices.

2.1.3. Thermal management solutions

Solutions of thermal management are commonly implemented by using heat sinks. With a large contact surface and high thermal conductivity material, the power dissipated by the semiconductor can be transferred to the cooling media and the junction temperature gets reduced. Different approaches to design heat sinks have been proposed, including:

- Natural and forced convection air-cooled heat sinks
- Single and double-sided cooling with liquid-cooled heat sinks.
- Jet impingement and direct contact liquid cooling of DBC substrates.
- Liquid-cooled heat sinks with phase-change capability.
- Heat pipes.
- Combination of the above methods.

Different solutions are evaluated based on the heat transfer coefficient, h with the unit (W/(m²K)). This coefficient is defined as the proportionality constant between the heat flux and the temperature difference, as stated in Eq. 2-2

$$h = \frac{q}{\Delta T} \rightarrow \Delta T = \frac{q}{h} \quad \text{Eq. 2-2}$$

Generally speaking, the larger h , the smaller temperature increases with the same power input, and better thermal performance can be achieved. Among all the solutions, three kinds

of heat sinks are most commonly used: natural convection heat sinks, forced air-cooled heat sinks, and liquid-cooled heat sinks[11-15].

The natural convection heat sinks, with high reliability and simple systems, are named passive air-cooled heat sinks. This approach relies on the natural circulation of the buoyancy-driven flow. Based on the ideal gas law shown in Eq. 2-3, the volume of the air expands when heated up through thermal convection by the hotter surfaces of fins[12].

$$PV = nRT \quad \text{Eq. 2-3}$$

The density differences of the hot air near the heat sink and the cold air of the ambient lead to the buoyancy flow that moves the hot air away from the devices and cools the system. However, this passive cooling method is limited by the low flow velocity and the low thermal conductivity of the air. The heat transfer coefficient h of convection is only about 2 – 25 W/(m²K)[15].

To further improve the heat dissipation capability, a higher flow rate is desired. Forced air flow, for example, the flow from the fan, can significantly increase the flow rate and enhance thermal performance by more than ten times compared to the passive method. However, the cooling method is limited by the thermal capacitance of the air. As a low-performance thermal transfer medium, the heat transfer coefficient h , of the forced air-cooled solution is about 25 - 250 W/(m²K).

Liquid-cooled heat sinks, on the other hand, provides a better thermal performance by using better heat transfer mediums, water or other similar liquid materials. The liquid in the system is circulated by the pump and draws dissipated heat from semiconductor devices via contact interfaces. The thermal energy transferred to the liquid flows is then carried out by condenser outside the module. This application can boost the heat coefficient up to

20000 W/(m² K) with a single-phase liquid cooling solution. Even better performance can be achieved with phase change capability of the flow. Drawbacks including complex system, with the pump, condenser and other auxiliary components and, high installation cost and lower reliability, make this solution less complete. Liquid-cooled solutions are normally applied to the high-power applications [16].

2.1.4. Design a heat sink

Picking a heat sink from a variety of the designs, it is hard for researchers to manually calculate and design the heat sink. Alternatively, the thermal equivalent circuit (TEC), as shown in Fig. 2-4, is proposed as a simplified method to fast estimate the thermal performance [17-19]. By approximating the heat transfer path and ignoring details of the model, the heat flow can be modeled as a current flow and the thermal management system can be presented as an electrical circuit and the temperatures of each component are noted as node voltages. The capability of conducting the heat flow and the absorbing the energy is correspondingly represented by resistance and capacitance in the circuit. After reaching the steady state, capacitors in the circuit are fully charged and the node voltage reaches a constant value. The capacitors can be then replaced by the open circuit. And the thermal resistance of the thermal equivalent circuit is calculated in Eq. Eq. 2-4. Similar to the Ohm's law, the thermal resistance is the proportionality constant between the temperature difference and the power flow magnitude.

$$R_{th_AB} = \frac{T_A - T_B}{P} \quad \text{Eq. 2-4}$$

As defined, R_{th_AB} is the thermal resistance from location A to location B along the heat transfer path. The conventional steady state thermal equivalent circuit is drawn in Fig. 2-4.

The heat transfer path is divided into four segments and presented by four elements with five nodes. Each node is represented by a letter, as: “j” for junction, “b” for baseplate, “h” for top surface of the heat sink, “t” for the tip, which is the far-end of the heat sink and “a” for the ambient.

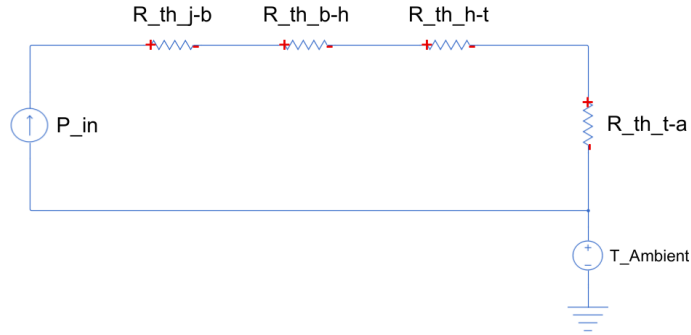


Fig. 2-4. Steady state thermal equivalent circuit

At the steady state, the junction temperature of the module can be evaluated simply based on the derivation of Ohm’s Law. The constraint of picking up the heat sink is shown as Eq. 2-5. During the design process, the maximum allowable thermal resistance of the heat sinks should not exceed:

$$R_{th_{HeatSink}} < \frac{T_{j_{max}} - T_A}{P} - R_{th_{jb}} - R_{th_{bh}} \quad \text{Eq. 2-5}$$

On the right-hand side of Eq. 2-5, both values of $T_{j_{max}}$ and $R_{th_{jb}}$ are available in the device manufacturer's datasheet. $R_{th_{bh}}$ is the thermal resistance brought by the thermal interface material (TIM) and can be determined using the thermal properties of the material and TIM’s thickness. T_A is the operating ambient temperature related to the environment and P as the total power loss, can be estimated by either mathematical model deduction or

the circuit simulation. With all the values assigned, an upper design limit of thermal resistance of a heat sink R_{th} is determined. With a suitable design margin, the design target for the heat sink is built up. Different approaches for designing heat sinks have been proposed for the last several decades.

For most of the power electronics applications, to simplify the design process, instead of designing the heat sinks from scratch, commercially available heat sinks are selected. Thousands of pre-designed heat sinks are manufactured by different vendors, with different materials, designs approaches and manufacture methods. For various applications with different dimensions, thermal resistances and prices, procedures of designing, the thermal management design procedure of a power converter are summarized in the Fig. 2-5[17].

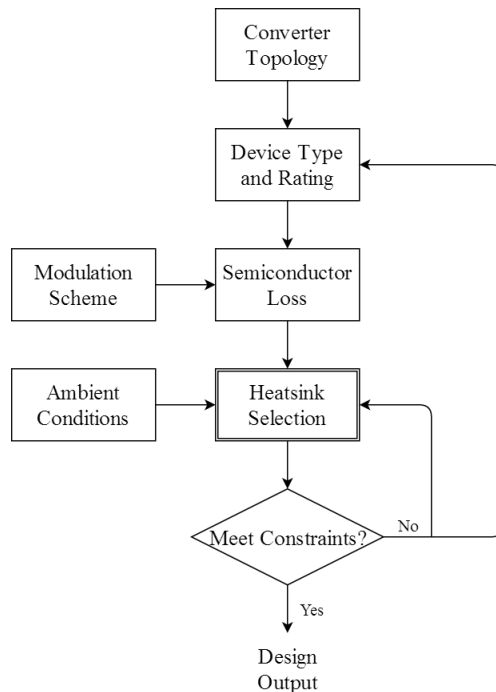


Fig. 2-5. The design procedure of the thermal management system[17]

This method provides a rough but quick design of the system. However, most of the design is only moderate in terms of the performance. This is mainly due to the following reasons:

First, the definitions of the thermal resistance vary by manufactures. The heat sink's thermal resistance is roughly estimated based on the temperature difference of different components. Junction temperatures have been measured as either the average temperature of the whole hot surface or the hot spot located at the center of the heat source. Ambient temperatures, on the other hand, are defined by either the tip temperature of the heat sink or the average temperature at the inlet location. Those mismatches lead to the uncertainties of the estimation and bring significant inaccuracy in the evaluation of the system.

Second, the thermal equivalent circuit is evaluated based on the one-dimensional approximation. This approximation is not suitable for the applications with discrete dies, for example, the applications with direct-bonded copper substrate (DBC). The uneven heat distribution compared to the uniform distribution may cause additional temperature increase locally. The thermal coupling between devices will moreover aggravate the error in the estimation. These underestimated factors will eventually lead to the system failure if without a sufficiently large margin left. Thus, an over-sized heat sink is usually picked to guarantee the design targets and the additional cost will be counted into the overall budget. Also, the oversized heat sink, as one of the largest components in the system, became the big challenge for the high-power density goal.

As introduced previously, by using advanced WBG devices in the power electronics module, both the number of the devices and the total loss can be reduced compared to the Silicon-based devices. Also, the advanced material properties of the WBG devices allow

higher switching frequencies. The size of the passive components, taking output filter as an example, highly depends on the switching frequency. The ripples caused by the switching behavior can be reduced with a higher switching frequency, so as the size of the filter. However, the increased switching frequency can lead to other problems. One of the issues is the high thermal stress. As stated previously, the switching loss of a semiconductor device is proportional to its switching frequency. To compensate for the higher loss brought by high switching frequency, a better thermal management system's design without simply over-sizing the heat sink is desired. Different works for pushing the limit boundary of the thermal performance further, by designing with more complex structure to increase the surface area are reviewed in the second part of 2.

2.1.5. 3D printing

On the other hand, even a superior design has been approached by the algorithm, the realization of the design still poses a challenge. As the conventional manufacturing process, the designed part is manufactured with the removal of material from a whole block (used in drilling and milling to manufacture heat sinks). However, for complex designs, especially the heat sinks with complex inner structures, the more complex designed geometry, the greater challenge will be posted. By using conventional methods, additional cost exponentially increases with the complexity added.

To avoid the overwhelming cost post by the manufacturing process of the complex parts, 3D printing technology have been considered as an alternative method of manufacturing heat sinks., 3D printing technology is employed to manufacture the power electronics module. On the contrary of the removal process, 3D printing additively constructs the part,

similar to the 2D ink-jet printing technology, where document is printed line by line based on the profile. As the 3D designed part with one dimension higher to the 2D document, lines of the documents convert to slices of the computer-aided drafting (CAD) design file and 3D printing process builds the part layer by layer. Take the metal printing as an example, starting from the bottom layer, Aluminum powders are melted with laser or fine e-beam following the pattern of the first slice layer. The second layer is then added to the first layer as another slice of the pattern. This process repeated until reaches the top slice layer. By this way, the manufacturing process is divided into multiple layers so that the cost of the 3D printing won't be affected by the complexity. This is the "Complexity free" property of the 3D printing[20, 21].

Available materials for 3D printing, including polymers and metals such as Titanium, Aluminum, Stainless Steel, Copper, and Brass can be used in the power module design. Aluminum printing, because of the relatively cheaper cost and acceptable property, is used as the major printed metal material. To fully utilize the technology, the thermal property material of additive manufactured Aluminum is compared to the conventional Al 6061. Due to different material composition and the impact of alloy, a degraded material property is founded. A post-process is proposed in this dissertation that can permanently eliminate this property mismatch issue.

2.1.6. Conventional heat sink design approaches

Conventionally designed heat sinks come with different structures, such as plate-fin, pin-fin, hexagon, etc. have been modeled and optimized for decades. Among them, heat sinks with plate-fin structure have dominated the application market due to their relatively

large contact surface and low-pressure drop. Parameters to be optimized of this kind of heat sink includes width W , depth L , thickness of the fin t , fin spacing s , and fin height H . Mathematic models of such design have been fully developed based on the simple and symmetrical geometry with reasonable approximations. Design and evaluations of the heat sinks can be easily converted to the optimization of the mathematics target function. Authors in [11] have illustrated the design procedure by mathematical derivation in details steps by steps.

As defined previously, the plate-fin heat sink is parameterized by (L, W, H, s, t) . The general configuration of the cross-section of the heat sink is shown in Fig. 2-6.

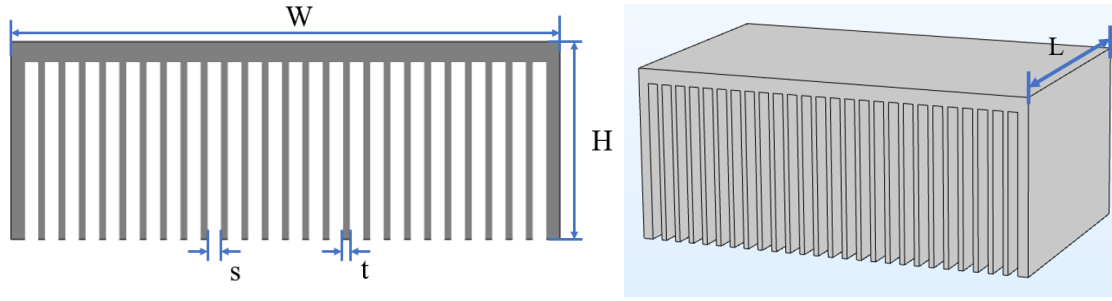


Fig. 2-6. Design parameters of conventional heat sinks with plate-fins

Thermal resistance of the heat sink, R_{th} is the optimization target of this problem. As shown in Eq. 2-6, thermal resistance is a function of heat convection coefficient h_c , the total surface area A and the surface efficiency η_t .

$$R_{th} = \frac{1}{h_c A \eta_t} \quad \text{Eq. 2-6}$$

η_t is the surface efficiency described in Eq. 2-7.

$$\eta_t = 1 - \frac{A_f}{A} (1 - \eta_f) \quad \text{Eq. 2-7}$$

Where A_f is the total area of fins, and A is the total surface for thermal convection. The fin efficient η_f is a function of fin parameter χ written as:

$$\eta_f = \frac{\tanh \chi}{\chi} \quad \text{Eq. 2-8}$$

Fin parameter χ is a parameter related to the fin height, and is expressed as:

$$\beta = H \cdot \sqrt{\frac{h_c \varrho}{\sum_{i=1}^N k A_{ci}}} \quad \text{Eq. 2-9}$$

The denominator inside the square root is the sum of product values of thermal conductivity of material and the heat conduction cross-sectional area. ϱ is the surface area per unit length of the fin and h_c is the value of the convective heat transfer coefficient expressed in Eq. 2-10.

$$h_c = \frac{N_{us} k_f}{s} \quad \text{Eq. 2-10}$$

Where k_f is the thermal conductivity of the fluid media, s is the fin spacing parameter and N_{us} is the Nusselt number written as:

$$N_{us} = \left[\left(\frac{R_{es}^* P_r}{2} \right)^{-3} + \left(0.664 \sqrt{R_{es}^*} P_r^{\frac{1}{3}} \sqrt{1 + \frac{3.65}{\sqrt{R_{es}^*}}} \right)^{-3} \right]^{-\frac{1}{3}} \quad \text{Eq. 2-11}$$

In this Eq. 2-12, P_r is the Prandtl number and R_{es}^* is the modified Reynolds number of the channel, written as:

$$R_{es}^* = R_{es} \cdot \frac{s}{L} \quad \text{Eq. 2-12}$$

R_{es} is the Reynolds number, as the weight factor of inertial forces over the viscous forces of the flow, is the key to determine type of the flow as either Laminar or Turbulent. The value of this number is calculated based on Eq. 2-13

$$R_{es} = \frac{\text{inertial forces}}{\text{viscous forces}} = \frac{(\text{mass})(\text{acceleration})}{(\text{dynamic viscosity})(\frac{\text{velocity}}{\text{distance}})(\text{area})} \quad \text{Eq. 2-13}$$

$$= \frac{\rho \cdot V_{ch} \cdot Dh}{\mu} = \frac{V_{ch} \cdot Dh}{\nu}$$

In this equation, ρ is the density of the fluid, μ is the dynamic viscosity ν is the kinematic viscosity which satisfy:

$$\nu = \frac{\mu}{\rho} \quad \text{Eq. 2-14}$$

Dh is the hydraulic diameter of the flow channel that related to the wetted parameter P, as shown in Eq. 2-15:

$$Dh = \frac{4A}{P} \quad \text{Eq. 2-15}$$

On the other hand, the channel velocity V_{ch} can be estimated based on the inlet flow velocity V_{in} :

$$V_{ch} = V_{in} \cdot (1 + \frac{t}{s}) \quad \text{Eq. 2-16}$$

Once the flow velocity inside the channel is obtained, the drag force of the heat sink can be calculated based on three parts, inlet pressure K_c due to the sudden contraction, outlet pressure K_e due to the sudden expansion and the viscosity force expressed as:

$$F = \frac{1}{2} \rho V_{ch}^2 f_{app} N (2HL + sL) \quad \text{Eq. 2-17}$$

Where f_{app} is the apparent friction factor that can be evaluated based on laminar flow formulation:

$$f_{app} = \frac{1}{Re_{Dh}} \left[\left(\frac{3.44}{\sqrt{L^*}} \right)^2 + (f \cdot Re_{Dh})^2 \right]^{1/2} \quad \text{Eq. 2-18}$$

Where

$$L^* = \frac{L}{D_h Re_{Dh}} \text{ and } Re_{Dh} = \frac{V_{ch} D_h}{\nu} \quad \text{Eq. 2-19}$$

The $f \cdot Re_{Dh}$ of Eq. 2-18 represents the friction factor of the fully developed flow interpreted by the Eq. 2-20:

$$f \cdot R_{edh} = 24 - 32.527 \left(\frac{S}{H}\right) + 46.721 \left(\frac{S}{H}\right)^2 - 40.829 \left(\frac{S}{H}\right)^3 + 22.954 \left(\frac{S}{H}\right)^4 - 6.089 \left(\frac{S}{H}\right)^5 \quad \text{Eq. 2-20}$$

Step by step backward, engineers can design heat sinks with the optimized set of the design parameters. Different approaches under various assumptions and objective functions are reviewed in this part.

Authors in [22, 23] present the fundamental models for evaluating heat sinks' performance by the fin layout efficiency and thermal convective correlations. Plots for evaluating the theoretical limit are generated based on the analytical model. A similar analysis is found in, by using Poiseuille's equation to the pressure drop based on the channel flow velocity. Fin thickness and channel spacing parameters have been optimized for a better heat sink. Other similar work can be found in [24-26]. Authors analytically optimized the heat sink performance by designing dimensions of fins and channels. The author in [27] evaluated the thermal performance of the heat sinks by a simplified equation of the design parameters. This equation directly calculates the cooling performance index CSPI by considering the thermal property of the material and P-Q curve of the fan. An entropy generation minimization (EGM) is proposed in [28] to optimize the performance of heat sinks with microchannels. The effect of fins' number and the bypass channels are studied in [29]. The phenomenon has been noticed that the heat sink's performance will decrease after passing the threshold of the fin number. The decrease is more obvious with the presence of the bypass channels.

In terms of the liquid-cooled heat sink design: The authors in [30] propose an optimization method of designing the liquid-cooled heat sinks with micro-channels at a given pressure, assuming fin height equals to channel thickness. However, for decades of

researches and revisions, the conventional heat sinks have reached the theoretical design limit. To improve the performance further, novel heat sinks with more complex designs are considered.

2.1.7. Novel heat sink design approaches

Instead of the canonical fin structure of the heat sink designs in part 1, the designs of heat sinks shown in this part jumped out of the design constraint of straight fin design and involved more flexible geometry majorly to increase the surface area, such as porous structures, laminates structure, metal foam, and other complex geometries.

Methods using advanced materials and porous structures to create larger contact surface have been found in many references. However, the larger surface area comes with two major drawbacks, high pressure-drop penalty, and unaffordable cost and limits the applications. Heat sinks with plain-weave screen laminates porous structure are proposed in [31, 32]. A superior performance can be achieved with a low flow rate. However, significant pressure drop due to the porous structure leads to a worse performance with the increase of the flow speed. Metal foam with lightweight and high porosity properties are used in [33] as the materials of the heat sink. Benefits such as a higher surface rate, good structural strength with lighter weight, and excellent flow mixing ability are brought in. Drawbacks, including the significant increase of pressure drop, lower fin efficiency, dust accumulation, and high cost make this approach less possibly used in air-cooled applications. Better performances with such porous materials can be found in liquid-cooled applications as illustrated in [34]. Other heat sinks with foam structure are designed in [35]. Four heat sink structures, named fin-foam, parallel plate, slotted hexagon, and Schwartz

structure are evaluated. However, due to the drawbacks of the pressure drop, none of the designs can show a complete improvement. Other applications by using the high-conductivity graphitic foam present a better performance. The difficulty in the manufacturing process and extremely high cost make this approach less realistic.

Researches based on the optimization of fin configurations provide another approach to the better performance. Authors in [36] proposed a highly-interrupted fin surface instead of the plain fin structure. By employing the forms of louver or slit fins, superior performances can be achieved with the fin spacing larger than 1.6 mm. surfaces. For a smaller fin spacing, the pressure drop penalty introduced by the interrupted rough surfaces reduces the performance. The same point of view can be also noticed in [37-39]. Another type of fin surface modification is proposed in [40], named as longitudinal vortex generator (LVG). Vortex patterns on the fin surface generate swirled flows as the secondary flow. This method has been proved in [41-43] provide that an improved heat transfer capability can be achieved without additional pressure drop. However, the solution is only effective in the region with high flow velocity and large fin spacing. The plain fin structure is still dominating for the dense fin applications.

In order to optimize the heat sink's performance under low-velocity operation, a novel cannellure fin structure is proposed in [44]. Instead of intruding surfaces as LVG methods, the author modifies the fin surface with the dimple/cavity structure. Low fin spacing is assumed in this method. Wall vortical motion and the local suction/blowing flow resulted by the cannellure fin enhances the performance of the heat sink in the fully developed flow region.

Another design of fin-structure heat sink is proposed by cross-cut design in [45]. Comparisons have been done based on the heat sinks with different fin structures: parallel plate fins, fins with single cut and fins with multiple cuts. Among them, heat sinks single cross-cut is proved to achieve the best performance due to the ability to mix airflow mechanism between adjacent channels, especially at a large flow rate.

The IPFM design, with an asymmetry design shown in [46], uses the combination of fin structures, where fins with rectangular shapes are assigned at odd numbers positions and parallelogram shapes at even numbers positions. Better performance is achieved with flow rate under 10 CFM.

2.1.8. 3D printed heat sinks

In addition to the novel design method, the manufacturing step poses another challenge when dealing with the complex structure of the heat sink. The more complex designed geometry, the greater challenge will be posted. Additional cost increases exponentially with the complexity added. Thus, to avoid the overwhelming cost post by the manufacturing process, 3D printing technology has been considered as an alternative method of manufacturing heat sinks. 3D printing, which is regarded as the “the third industrial revolution”, is increasingly being used in industrial and research applications by building parts by adding layers [20, 21, 47-49]. Based on the computer-aided design (CAD) of the part, an STL file is generated and sliced into 2D layers. Each 2D layer is built with a mechanism similar to the conventional 2D ink-jet printing. That is, after the completion of each layer, the next slice in the sequence is built on top of the previous layer. This process continues until the completion of the whole file. Commonly used 3D printing

processes include Stereolithography (SL), Selective laser sintering (SLS), Fused deposition modeling (FDM), Inkjet binder and Aerosol printer. Design of parts by conventional manufacturing is limited due to the constraint introduced by the manufacturing process. The 3D printing process allows for structures with multiple functionalities and reduces the part count as well as improves the fill factor. Some of the other benefits of 3D printing include quick prototyping less wasted material and easy assembly.

A 3D printed air-cooled heat sink design by Additive methods for is introduced in [50]. The process is based on topology optimization where a gradient-based optimizer coupled with FEA simulation is utilized. The predefined design domain meshes into small elements which are assigned either solid or fluid material, based on the density variable γ . The objective function is used to optimize γ to achieve the best performance. Similar methods are also found in [51]. Another additive method is proposed in [52] by imitating the growth of a tree, the 2D pattern of the heat sink cross-section is designed starting from the baseplate. The pattern grows by adding branches to the geometry from the previous iteration. There is a “Growth Tolerance Criteria” defined by the percentage of the thermal performance improvement. The optimization is terminated when either the designed “branch” reaches the boundary, or no additional improvement can be achieved by adding elements.

On the contract of additive methods, in [53], a Subtractive Design Methodology has been used for either “Unrestricted Removal” or “Top Surface Removal” to optimize a predesigned fin structure heat sink. The optimization target is to balance the thermal performance of the front end and the rear end. By introducing bypass airflow without close contact with the front part of the heat sink, cooler flow can reach the end part without being

heated up. Also, at the same time, the pressure drop reduction and as well as the material saving can be achieved.

2.1.9. 3D printing applications in power electronics

Not only the heat sink can be 3D printed, other components in power electronics such as bus bars, PCBs, packages, and inductor cores are also printable with benefits.

As one of the three major components contribute to the overall power density calculation, reduction of the passive components size can significantly increase the power density. Approaches have been employed either by optimizing the passive components' structure for compact design or by increasing the switching frequency using air-core inductors.

Ferromagnetic materials, due to the higher magnetic permeability are commonly used in power electronics applications. By integrating the 3D printing into the inductor design, advanced structures with integrated features can further increase the performance and shrink down the size. Applications in [54-56] are proposed using printable magnetic cores. Cores are constructed with the magnetic paste consisting of permalloy powder filled benzocyclobutene. The conductive windings are printed using nanosilver pastes to the cores. A planer inductor is printed in [54], with a plane magnetic core and the spiral silver paste on top as the windings. More complex toroid inductor as a 3D structure is built with eight turns of winding in [55, 56]. The round-shape magnetic core is printed and windings are embedded inside the core during printing. Advanced materials, the soft UV sensitive low-temperature sinterable ferrite paste is used in [57], resulting in more than 80% density improvement comparing to the conventional iron core inductor.

Air-core inductor, as an alternative approach due to the capability of high switch frequency, is designed for applications with switching frequency up to 1 GHz, beyond the operation range of inductor with the ferrite cores. An air-core inductor with 3D scaffold structure is developed in [58]. The inductor design is manufactured by casting based on the 3D printed mold. Tuning parameters are optimized based on both parasitic capacitances and inductances. High-frequency isolation is achieved by using selective electro-deposition and the integrated functions of the heat sink and EMI shield are also included in the design with added structural textures. A 70 W inverter with 27.12 MHz switching frequency is built based on five structural approaches of the air core inductor. In addition to this work, the author in [59] proposed a similar design approach with the toroidal inductors' cross-sections. Over 50% of the weight reduction and 90% efficiency can be achieved. An advanced material as the graphene-based filament is used for the coil construction in [60], with the same inductor structure and shows a further superior performance. However, the cost is a big issue. Other approaches such as the air-cored inductor with an adjustable shape are designed in [61, 62] by injecting the liquid-phase metal alloy into 3D printed micro-channels silicone elastomer. The printed flexible mold, as the container of the soft-matter electronics, can keep the performance under stretches, resulting in a higher fill factor of the package.

The flexibility of 3D printing can be also used in PCB with lead-based alloy as the RP printing material in [63]. Instead of using the screen printing method, the patterns of the circuit board are directly “written” with the small drop of liquid on the product case or another ink-jetable surface. However, the design of a complex circuit layout is still an issue, especially with isolation constraints included. The author in [64] used graphene

polymer nanocomposite as the printed material for the circuit board. Package with high fill factor enabled by the 3D printing can contribute to a significant improvement in power density. More integrated functions can also be designed into the package. The reduction in the component count and the elimination of interfaces lead to the compact design. Authors in [65] present approach to decouple the thermal expansion impact by eliminating solder, sinter layers, bond wires and structured geometry. Moreover, the integrated heat sinks in the packaging design ensure the cooling performance of the module. A 10-kW SiC inverter is built from the bare dies using 3D printing in [66]. A power density of 8.1 kW/L is achieved, which is 3.1 times higher than the commercial module-based design. Moreover, Rapid prototyping is achieved as the construction of the power module from prototype request to complete took less than one day.

Applications of 3D printing in different areas of power electronics research have been proven significant potential to improve the performance and power density of the power modules. To fully unitized the advantage of 3D printing, and achieve a 100% printed converter, challenges should be addressed [67-69]:

- Not all materials can be printed. As for now, limited materials can be employed, such as polymer, and few metals. But for an advanced design, for example, to manufacture printed capacitors and DBCs, the capability of printing dielectrics materials and ceramic are desired.
- Multi-material printing is difficult to achieve. Issues including the mix of the material with varied properties and the CTE difference must be considered. This feature has to be realized in order to further decrease the part count, reduce the assembly difficulty and increase the reliability of the module.

- High material and manufacture costs are another challenge, especially for a large-scale industrial production. Not only the metal powders, but also the protected inert gas (Argon) is expensive during the manufacture process. Also, the long manufacture time per part makes the printer less efficient.
- Removal of the powders as the one of the post-processes is necessary. However, the residual powders in a closed surface or a narrow channel is hard to get rid of. Moreover, potential dangers exist when recycling powders due to the flammable and combustible properties.
- Resolution of the printing is rough, especially for the small features and contact surfaces. Moreover, the impact of gravity lead to difficulties in printing fine threaded hole or the sharp corners. More advanced printer and post-processes including threads drilling, surface polishing is necessary.
- Design methods, especially conventional design approaches limit the performance due to the lack of design degree of freedom. To further enhance the printed parts' performance, more complex design method, such as the implementation of machine learning based optimization should be considered.

2.2. PARASITIC DOMAIN

2.2.1. Parasitic inductance

Inside power electronics converter, parasitic elements (resistances R , inductances L , and capacitances C) are unavoidable. Those elements are not desirable for designed performance. They usually come from the substrate configuration, the chip layout, arrangements and the electrical interconnections in module packaging. [70] For a converter

built with discrete devices in TO-247, due to the large physical separation of devices and the existing of multiple lead terminals, influences of parasitic elements are extremely large [71, 72]. Power modules, as an integrated solution of packaged devices, can shrink the physical dimensions of the devices and reduce the parasitic. However, no matter which approach is used to construct the converter, parasitic elements always exist. Parasitic inductance, as the most critical element, can significantly impact on switching performances of a power converter [73-76]. The inductance comes from the basic magnetic-physics laws.

Faraday's Law stated that "when a change in the magnetic flux inside a loop takes place, an electromotive force will be introduced to the loop, as the rate of change of the magnetic flux", as formulated

$$\varepsilon = -\frac{d\Psi}{dt} \quad \text{Eq. 2-21}$$

Where magnetic flux Ψ is defined as the contour integration of magnetic field and the area

$$\Psi = \oint_S \vec{B} \cdot d\vec{s} \quad \text{Eq. 2-22}$$

Where $\vec{B}$ is the magnetic field, and its value is related to the nearby current magnitude. Taking the neighborhood of an infinite long round wire as an example, the magnetic field can be modeled as

$$B = \frac{\mu_0 I}{2\pi r} \quad \text{Eq. 2-23}$$

Where μ_0 is the magnetic constant, I is the current through round wire and r is the distance from the test point to the wire. Taking the expression of Ψ and B into the Faraday's Law for a slightly opened loop, the voltage difference v can be expressed as

$$v = - \frac{d \oint_s \frac{\mu_0 i}{2\pi r} \cdot d\vec{s}}{dt} \quad \text{Eq. 2-24}$$

Taking all time independent parameters out, the equation can be rearranged as

$$v = - \left(\oint_s \frac{\mu_0}{2\pi r} \cdot d\vec{s} \right) \cdot \frac{di}{dt} = -L \frac{di}{dt} \quad \text{Eq. 2-25}$$

Where the di/dt is the current change rate and the coefficient before it is marked as L , called parasitic inductance. Due to exist of this element, extra voltage will be introduced to the loop when the current change. A voltage overshoot spike happens during turn-off transients of active switches with a negative current changing rate. This extra voltage spike will be added to the DC blocking voltage and put larger voltage stress[77]. In hardware implementation, to ensure the safety operation, three adjustment option, a slower switching speed di/dt , a smaller parasitic inductance L or a higher device rated voltage should be considered compared to ideal design case. However, the slower switching speed not only limit the switching frequency but also increase the switching loss per transient. The higher rated voltage required the advanced device that may add cost or add additional conduction loss.

This overshoot issue is aggregated with recent application of Wide Band Gap (WBG) semiconductor materials such as Gallium Nitride (GaN) and Silicon Carbide (SiC) [78, 79]. Taking SiC devices as example, because of the high rated voltage level enabled by the material property, SiC MOSFETs become an alternative choice for power electronics

engineers who are currently using IGBTs and they can allow a much higher switching frequency. However, the higher switching speed used in WBG devices lead to an even larger overshoot spike. Thus, more efforts should be targeted on the parasitic inductance and to ease the overshoot voltage stress.

2.2.2. Parasitic inductance extraction method

Parasitic inductance, as introduced previously, is not an “actual” circuit component. It parasites everywhere inside the module. As the state of art, most of the researchers are using the lumped inductance model as what used in [80] to present the influence of the parasitic element. Taking an equivalent MOSFET lumped inductance model as the example, three inductance components are added, named L_{d1} , L_{s1} and L_{s2} .

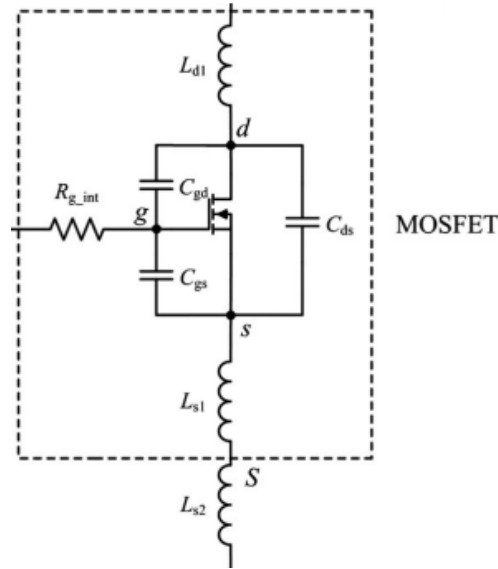


Fig. 2-7. Lumped inductance model of semiconductor devices

As the art of state, researchers have proposed several methods based on either numerical simulation, mathematical approximated model or the experimental test to extract the value of each lamped component.

Experimental based Extraction Method

As the most accepted circuitry for parasitic inductance, the two inductive-load double-pulse testers (DPT) have been built for device dynamic characterization evaluation [81, 82].

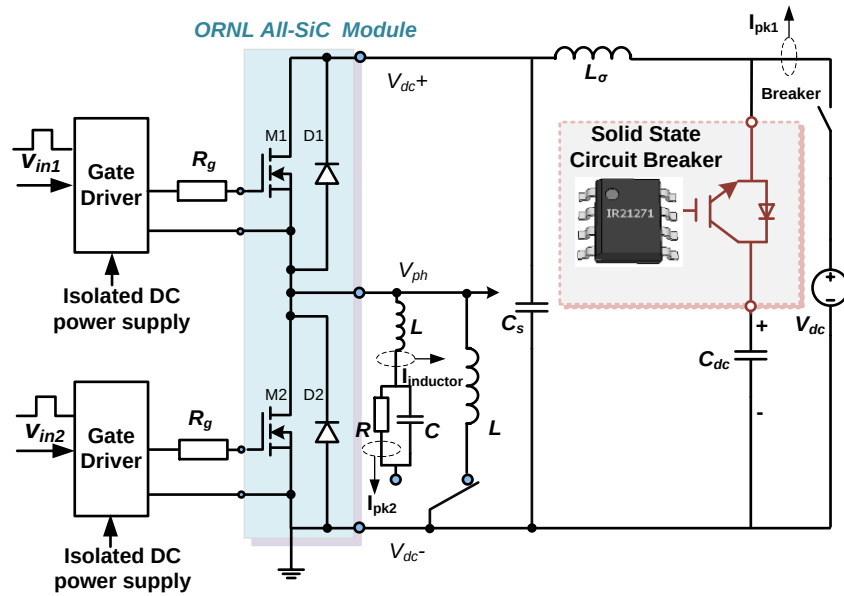


Fig. 2-8. DPT configuration of a phase-leg module

Similar to the DPT for device characterization, the parasitic inductance is also calculated based on the switching wave form of the device under test (DUT). By adjusting the V_{dc} to the rated operation voltage and turning on the DUT for a period until the inductor current reached the rated operation current, the DUT is then turned off and turned on again within a few microseconds. Because this switching transient is very short, the inductor can be

treated as a constant current source. The switching waveform of described test actions is shown as. Note that a coaxial shunt current sensor should be implemented instead of the Rogowski coil which is commonly used in the device characterization. Due to the extremely high ringing frequency, the limited bandwidth of Rogowski is not able to pick up the waveform ringing details. Coaxial Shunt, due to its “unlimited bandwidth”, should be replaced in the parasitic inductance extraction test.

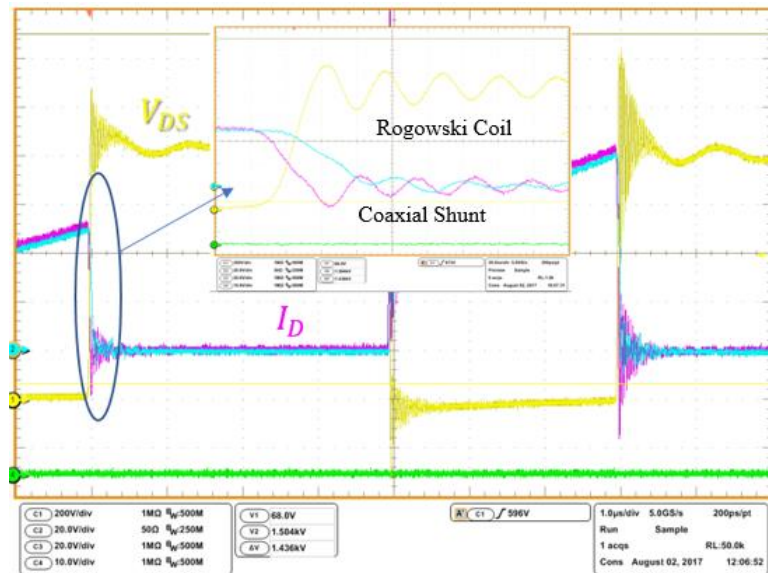


Fig. 2-9. DPT switching waveform

From the waveform, three approaches have been used to extract the desired parasitic inductance.

Overshoot voltage-based extraction

This method is straightforward using the inductance equation from Faraday’s Law. By measuring the overshoot voltage magnitude ΔV and the current change rate di/dt though

DPT, the parasitic inductance can be calculated. However, as the authors pointed out in [83, 84] that simply measuring the terminal voltage waveform V_{ds} could introduce errors due to the present of terminals and the due to measurement probe. Thus, a pair of Kelvin testers to sense the actual voltage waveform inside the module has to be fabricated and placed before testing. And the portion of the voltage overshoot spike caused by the power loop inductance is calculated using the difference of the V_{dc_Kelvin} and the $V_{dc_Terminal}$ over the switching speed di/dt .

Frequency domain analysis-based extraction

Authors in [74, 85-87] extracted the parasitic inductance parameter by measuring the ringing waveform of the kelvin connected drain to source voltage. Before testing, a set of ceramic decoupling capacitors are soldered near to the DC terminals for a constant voltage during the ringing period. After an overshoot spike introduced, the extra energy rings between the device's junction capacitor and the power loop inductance inside the module. With the known of junction capacitance C_{ds} and the measured ringing frequency f_0 , the parasitic inductance inside the module can be calculated as:

$$L_{loop} = \frac{1}{4 \cdot \pi^2 \cdot f_0^2 \cdot C_{ds}} \quad \text{Eq. 2-26}$$

This method has provided an accurate method of measuring the loop inductance inside the module without the impact of exterior inductances introduced by the bus bar and measurement probe. Similar method with a more complex reluctance model is used in [88]. However, the setup is relatively complex and requires a high accurate waveform measured by the shunt tester. This will add the hardware design difficulty as well.

Impedance Analyzer

Because of the semiconductor presented in the module, the defined power loop formed by DC bus, the freewheeling diode and the MOSFET device is not conductive at the normal stage. In order to use Impedance Analyzer to measure the loop inductance, the author in [89] fabricated an identical DBC substrate without semiconductor placed on and bonded the interconnection wires directly on the substrate. By this way, the inductance of conductive loop formed by wire bonds and copper trace can be measured using pin probe of Agilent precision impedance analyzer 4294A.

Analytical based Extraction Method

The experimental based extraction can provide accurate parasitic results by testing the module. However, in most of the cases, especially in the early design stage, it is not possible to extract parasitic inductance experimentally. Thus, lots of researchers have proposed mathematic model to analytically extract the desired parameters. The book [90] has deduced fundamental physics theory based equations for the parasitic inductance calculation. Authors in [91] used using Biot-Savart law to deduce a 2-D analysis of the magnetic field of the power loop at a high accuracy level. However, the computation time is one drawback. As of the wire bonds DBC structure, [92] proposed a practical method using parasitic inductance matrix to model both self and mutual inductance. Some other approaches, as in paper [93, 94] used approximated equations to model the loop inductance. Authors in [95] constructed an indicator λ as $C \cdot \ln(S) - l \cdot [\ln(2l) - 1]$ to estimate the relative commutation loop inductance. However, the model is not accurate enough to estimate all possible cases.

All mentioned model above can provide a general estimation of the parasitic magnitude as the optimization criterion. However, due to the large approximation involved, they are

less accurate to handle the parameter extraction case. Similar to the thermal case, FEA simulation can be also applied as the numerical extraction method for parasitic inductance.

Numerical FEA based Extraction Method

As of numerical extraction cases found in the literatures[96, 97], ANSYS Q3D Extractor is the most widely used tool. It uses finite element analysis to extract the electrical related parameters from the module structure. The benefit of this method is to provide a sufficient accuracy to the extraction, however, takes much longer time than the analytical model and need to involve external software. Parasitic inductance, as one major targets of the dissertation, is govern by Maxwell Equations, i.e. Ampere's Law, Faraday's Law and others. [98] Since all the govern equations are PDEs, similar to the thermal FEA simulation, the principle is to cut the target domain into small elements and using small approximation to convert PDE into ODE and solve the node values. Similar approached named Minimum-order boundary element method is found in [99] and Partial element equivalent circuits (PEEC) method in [100]. However, all mentioned methods above are time-consumable, the computation effort will be huge when used in an iterative optimization. In practical, numerical FEA based extraction methods are better to be implemented as an auxiliary function.

2.2.3. Review of parasitic inductance optimization method

As mentioned previously, the power loop parasitic inductance inside a module induced by the interconnections components can introduce large voltage spikes during turn-off transients of active switches. Design of a module packaging with reduced parasitic

inductance is critical to ensure the safety operation, especially for the WBG based applications[101].

2.2.4. Principle optimization approaches

According to the govern formula of the loop inductance calculation, a simple-minded equation can be expresses as:

$$L_{loop} = \frac{\mu_0 \cdot A_c}{l_m} \quad \text{Eq. 2-27}$$

Where A_c is the cross-section area of the loop, μ_0 is the vacuum permeability and the l_m is the effective magnetic path length. The reduction of inductance can be achieved by either reduce loop cross-sectional area with optimized routing layout or increase magnetic path length with larger wire gauge[102]. Practically inside the module, the current is conducted by the DBC and wire bonds and the magnetic path length of those components cannot be changed much. The most effective approach is to design the substrate layout design for a smaller power loop. As summarized in [95], two basic principles of low parasitic inductance substrate layout design are mostly considered:

- Layout of the device and terminals to minimize the commutation power loop area
- For the designs with similar area, design with shorter the commutation path length is preferred.

Most of the power loop design have been done manually by placing the devices on the substrate and using Q3D to extract and evaluate the performance [103][104]. Similar approach has been implemented in [105, 106]. By designing several GENs of substrate layout, the power loop is reduced lead to the improvement of loop parasitic inductance

from 11.3 nH to 3.4 nH. Authors in [107] split DC terminals and placed on both sides of the module to reduce effective parasitic loop. It is also a common design strategy noticed in commercially available power module. By placing decoupling caps on substrate, the power loop is shorted resulting a smaller inductance as implemented in [108]. However, this approach raises the concern of reliability related to the ceramic capacitor failure. All of the approaches mentioned above are focused on the optimal layout location of the units formed by active switch and anti-parallel diode of one same switch position. However, for an inductive load circuit, the power loop formed by the commutation current is between upper active switch and lower anti-parallel diode, or the other combination. The concept using switch position units will always pose a large physical separation between polarities. Based on this fact, a novel layout strategy can further reduce the loop inductance.

2.2.5. P-Cell and N-Cell concept

P-cell and N-cell layout concept was proposed in [89, 109-111] as a novel layout method to reduce the parasitic inductance. Instead of taking the active switches and their anti-parallel diode as a unit, the author split the devices into P-cell and N-cell in terms of the current commutation path. The cell names origin from the topologies of buck converters and used in the layout design to describe either unit of upper switch with lower diode or lower switch with upper diode. It can be noticed that the loop areas of the commutation current path are significantly reduced by using this layout method, so as the power loop inductance. Implementation of this method can be found in [112], where a SiC Trench module with low inductance is designed and tested. Similar concept is also used in [95] to

reduce power loop inductance. However, instead of using two set of bus bar, a pair of laminated bus bar is place in the center of the DBC.

2.2.6. Double-sided module structure

Besides the planar layout strategy, some researchers have also implemented 3D packaging design to optimize the module performance. As the basic principle illustrated in the loop inductance calculation, one of the effective approaches is to take the advantage of mutual inductance between current path of different polarity and compensate the self-inductance of each component. Reducing the loop area is one of the methods using this concept. However, due to the footprint and electrical isolation between polarities, power loop of a 2D planar layout always has an area larger than the total footprints of devices. Moreover, wire bonds of interconnection also contribute a big portion of the overall inductance. Thus, to eliminate such components and using a 3D packaging concept can be an alternative solution.

Double-sided planar power module, as the most practical approach, has been proposed in many literatures[84, 113, 114]. Inductance achieved by those structure can reach the level of several nH. In [115], authors used PCB as substrate and implement both switch cell and 3D packing concepts to design the module and achieve a high frequency operation GaN FET three phase inverter. Though, double sided power module can realize advanced thermal and parasitic performance, the high cost of module fabrication and the reliability concerns limit its application.

3. Fundamental Optimization Structure

3.1. CONVENTIONAL DESIGN APPROACH

As a conventional iterating design, most of heat sinks revision details are proposed based on the manual judgment of engineers. The flowchart of this iterating design is shown in Fig. 3-1.

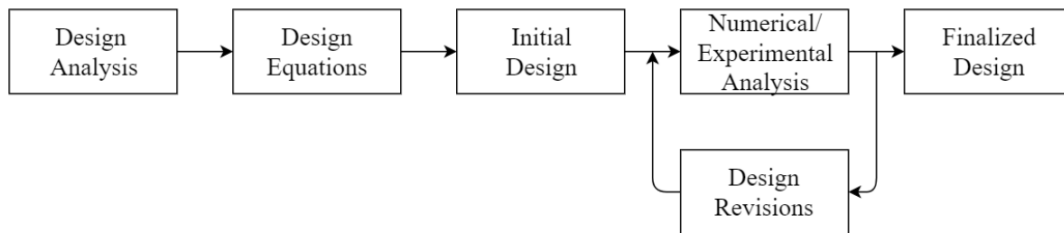


Fig. 3-1. Iterating design process

Performance of the optimization is highly dependent on the judgment of the engineers. Design details, such as the location of flow channels, are manually reviewed based on the experiences of the engineers, especially when no approximate math model can be applied. However, several limitations make this conventional engineering design less efficient:

First, the performance of the final optimized result is highly dependent on the initial guess. Starting with a bad design guess could eventually lead to the local optimum or even the divergence of the problem. This issue is critical, especially when using the optimization algorithm such as Newton's method since the converged solution is highly dependent on the initial guess. A reasonable initial design guess lots of times, indeed needs quite a high-level of design experience.

Second, most of the designs are carried out by the optimization on one single target. Taking the initial design as the baseline, the improvement is made based on the analysis of the previous iteration. Revisions are made to the previous weak points and try to resolve it in the next iteration. However, due to the design tradeoffs, there is a high chance that the modification on the previous version will create another design issue. Still, a high level of design experience is necessary, in order to precisely target the challenge and solve the problem.

Moreover, supervisions and involvement are required for the all-time during the evaluation process, since both evaluations and revisions have to be made manually. However, the limited working capability of engineers makes that only few iterations can be carried out before approaching the final the design. There is a high chance that it hasn't reached the global minimum and more iterations need to be done.

Finally, not only the time consumption but also the cost of labor will contribute a huge portion of the total cost of the project, especially involving the need for senior engineers.

Motivated by the high-performance computation capability of nowadays workstations and cluster super-computer, a fully automatic machine learning based optimization methodology with a higher capability of searching the global optimum point should be proposed to further enhance the optimization performance. As the first step of this methodology, instead of using the manual judgment or the mathematic derivation of the design model, the design process should rely on the computational simulation using finite element analysis (FEA).

3.2. FEA SIMULATION

As the first step of this proposed machine learning based optimization, FEA simulation should be used as the primary method of evaluation. Previously, the heat sinks are designed based on the mathematical deviation of the governing equations. However, one drawback of this method is the low accuracy, due to the approximations considered in the mathematics analytical model. And this drawback gets more significant with the increasing complexity of the design, especially including the plenty details of the model, such as the power module design with discrete devices.

Generally, the time- and space-dependent physics behaviors of the physics laws are described in the form of partial differential equation (PDE). However, except for limited cases, most of the PDEs have no analytical solutions. In order to approach the solution of those governing equations, discretization approximations have been made to simplify equations, making PDEs without analytical solutions solvable with the numerical approximated solutions. This discretization approximation method is called finite element analysis (FEA). The study domain are discretized with finite elements and the problem shrinks from the large scale into the single analysis only operated within the discretized element. In this way, each single analysis can avoid making the huge approximation on the whole study domain and will significantly increase the evaluation accuracy. This is the basic approach of individual evaluations used in this dissertation.

Take a governing equation u as an example. This u can be assigned to any dependent variable (i.e., temperature, pressure, etc.). By applying the finite elements, linear combinations of the basis u_i can be used to approximate the target function u :

$$u \approx \sum_i u_i \psi_i \quad \text{Eq. 3-1}$$

Where u_i is the approximated value of the function at the discretization node i and ψ_i is the basis function. Since for the most of cases in this dissertation, junction temperature is the target to be evaluated, the governing equations for this evaluation are called the conservation of internal energy:

$$\rho C_p \frac{dT}{dt} = g(T, t) \quad \text{Eq. 3-2}$$

Where ρ is the density and C_p is the heat capacity. Two variables are involved in, T and t . Where dependent variable, temperature $T(t)$ is a function of independent variable, time t . Also, g represents the heat source added to the system and it is a function of temperature and time. As the principle stated previously, instead of evaluating multiple variables at one time, only the independent variable (t) is evaluated. This, PDEs with only one variable are simplified to the solvable ordinary differential equation (ODE). Using the junction temperature T_0 as the initial condition of time t_0 , the boundary condition is expressed as,

$$T(t_0) = T_0 \quad \text{Eq. 3-3}$$

However, oftentimes, the dependent variable T is a function not only of time but also of space, generating the internal heat flux inside the solid body. In those cases, heat transfer equation gets another additional spatial dimension term. Such differential equation with one dependent variable $\mathbf{x}$ and two independent variables, T and t :

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot \mathbf{q} = g(T, t, \mathbf{x}) \quad \text{Eq. 3-4}$$

Where in addition to the previous designations, $\mathbf{x}$ ($\mathbf{x} = (x, y, z)$) is the newly introduced independent variable that represents the spatial coordinates. $\mathbf{q} = (q_x, q_y, q_z)$ is

defined as the heat flux vector within the solid domain. The divergence of $\mathbf{q}$ represents the heat flux magnitude changes in different directions as defined in the Cartesian coordinate system

$$\nabla \cdot \mathbf{q} = \frac{\partial q_x}{\partial x} + \frac{\partial q_y}{\partial y} + \frac{\partial q_z}{\partial z} \quad \text{Eq. 3-5}$$

As Fourier Law states, the heat flux is proportional to the gradient of temperature, and the negative of thermal conductivity is the proportionality constant:

$$\mathbf{q} = -k\nabla T \quad \text{Eq. 3-6}$$

k is thermal conductivity of the material and the equation states that the heat flux is proportional to the gradient in temperature. Taking equations above into the governing equation, the governing PDE equation to be solved is derived as:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k\nabla T) = g(T, t, \mathbf{x}) \quad \text{Eq. 3-7}$$

And the solution of this PDE will be approximated with numerical calculation using FEA. Expected result will present the temperature profile of the target module:

$$T_h(\mathbf{x}) \approx \sum_i T_i \psi_i(\mathbf{x}) \quad \text{Eq. 3-8}$$

This is a general introduction to the basic principles of the FEA simulation. Since it is still an approximating solving method, errors will always be compared to the actual solution. However, smaller elements size the evaluation has, the smaller error there will after approximation. However, tradeoff exists that the finer mesh has been built, the heavier computation effort should be paid, and that is the longer the computation time. A reasonable mesh suitable for the module is a key to achieve high optimization performance. Details of modified mesh algorithm will be introduced in the later chapters.

3.3. PROPOSED AUTOMATIC LOOP INTERFACE

To enable the machine learning function, one of the key functions is the automatic evolution capability. As defined in terms of machine learning, “computers the ability to learn without being explicitly programmed”, there should be no interference from outside during algorithm. On the other hand, thousands of individuals need to be evaluated through the optimization process. It is also impossible to manually run the simulation profile through the GUI window of the FEA simulation software. One of the requisitions of the algorithm in this dissertation is the construction of the fully automatic iteration loop. In this dissertation, COMSOL is picked as the software for evaluation, since each action in the GUI of COMSOL can be realized as a set of construction code.

For example, when drawing a square, no matter what the manual action is, COMSOL only records the coordinates of the four corners of the square. So, instead, the manual action can be achieved by inputting the construction parameter as a sequence of codes. Because of the convertible feature between .m file of the MATLAB and the code in COMSOL. This feature enables automation purposes. FEA simulation commands that should be executed in COMSOL can be now directly invoked from the algorithms implemented in MATLAB. The interface developed in this dissertation, enables the whole simulation process including geometry construction, material, and physics settings, mesh algorithm implementing, applying finite element solver and evaluation of the results can be “remotely” controlled by MATLAB.

The flow chart of the whole process is shown in Fig. 3-2. Individuals are generated by MATLAB in a mathematical expression named “DNA”. For each individual, the

evaluation is taken place in the COMSOL through the interface developed. Cooperating with the SOLIDWORKS for the construction of the auxiliary components, each individual expresses its “DNA” in the COMSOL by the coded instruction in MATLAB. Eventually, the evaluation results, such as the max junction temperature or the pressure drop of the module are acquired. Those results are reported back to MATLAB assigned as the performance of each individual. Development of this interface enables the automated evaluation which meets the basic requirement of the machine learning algorithm.

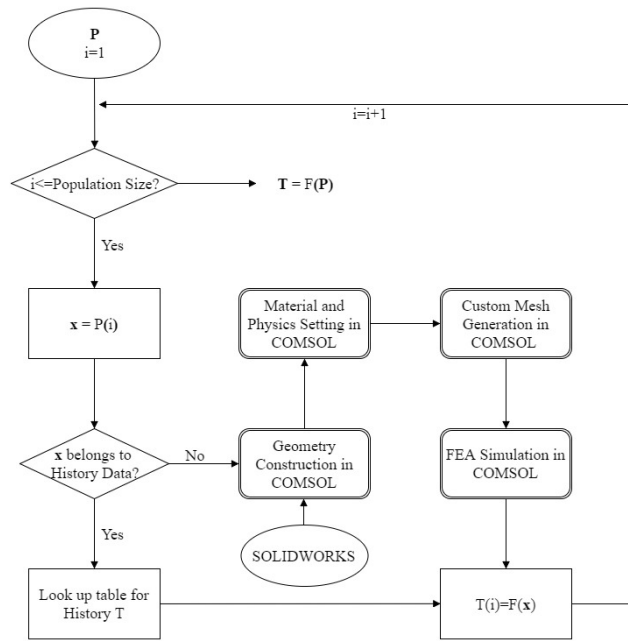


Fig. 3-2. Flowchart of evaluation interface

3.4. MACHINE LEARNING BASED ALGORITHM

Alternatively, instead of Newton's method of manually design process, algorithms based on the machine learning become one of the hottest topics in the research field. Machine learning can be found in a variety of applications, such as Alpha Go, auto self-driving system. The basic concept of the machine learning is described as: Evolving from the random initialization, the algorithms enable the machine itself to learn from the previous experiences of developed iterations and modified the individual with a trend of better performance until approaching to the optimal point automatically. The process is based on the evaluation of the fitness function of the problem. Fitness function of the problem is defined so that the individual with better performance can be assigned by a higher score and then build up an evolutionary trend towards the optimized result.

Before the beginning of the optimization process, a solution space has to be generated. The solution space is defined as the set of all possible solutions to the optimization problem that meet the problem's constraints, such as the manufacturing capability. And the optimization goal is to find out the individual with the best performance within the solution space.

For the particular optimization problems in this dissertation, due to the potentially huge solution space volume with countless possible designs exists, along with the high order of non-continues property of the solution space, conventionally used gradient-based optimizer such as Newton's method cannot be applied. Multiple local minimum points may potential trap such methods leading to a degraded performance. Instead, Genetic algorithms, as a population-based optimization algorithm has been proven very suitable for the multi-

objective optimization with a huge solution space. Also, the self-evolution property of the algorithm provides the machine learning capability without manual supervision.

3.5. OVERVIEW OF GENETIC ALGORITHM

Genetic algorithm (GA) is an optimization engine that imitates the natural evolution process proposed in the Darwinian evolutionary theory. This concept of the genetic algorithm is proposed by John Holland, a professor at the University of Michigan. In this algorithm, each individual, i.e. the heat sink geometry, layout of the devices or power module design, is coded in a mathematical. The mathematical expression of the individuals in the algorithm is called DNA, as the same concept in the biological individuals. DNAs carry the unique information of each individual and expressible as features of the individual. The set of all possible solutions (DNAs) of this optimization problem is called solution space. Each DNA may contain multiple chromosomes to present different features. In a canonical GA, chromosomes are conventionally coded as a string of binary. However, in some design case, for example, the heat sink optimization problem in this dissertation, the chromosomes are coded as matrix due to the high complexity of individuals. As a mathematical expression, each digit of the chromosome is regarded as one gene. The optimization goal is to approach the individual with the composition of genes that can maximize its performance. The expressions of the DNA in biological individuals create a variety of detailed features, such as the number of legs, the shape of legs and height of legs of an animal. Similarly, the expression process of the algorithm is achieved by decoding the chromosomes, and present as the design details of one individual. To ensure the

uniqueness quantification while expressing, a one-to-one mapping rule is constructed at the time of solution space generation.

As a canonical GA, five major steps are involved: Initialization, Evaluation, Selection, Crossover and mutation, and Recombination. Compared to the other optimization algorithm, such as the Newton's method and the Proof-number and Disproof-number Search(PDS) method, GA has a larger advantage when targeting on the optimization problems in this dissertation.

First of all, GA operation is only based on the evaluations of the fitness values. Gradients and Hessians of the candidates are not involved in the process. This property enables the algorithm to be efficient when dealing with the highly discontinuous solution space like problems in this dissertation. Because of the complexity of the solution space, which not all designs are feasible as a solution (due to Geometry constraint, Manufacture capability, etc.), the optimization problem is a nonconvex situation. The local minimum of such solution space may not always be the global minimum. Targeting on the multiple constraints and the complex solution space, Initialization and Recombination steps of GA allow a large enough and controllable searching step and keep the candidate under the design constraints.

Secondly, instead of optimizing a single candidate, GA operates on a group of individuals, which are referred as population. The impact of a worse individual can be weakened in a population-based evaluation. During the optimization process, not only the individual becomes better, but also the population evolved with iterations.

Thirdly, the performance of the optimization process is not highly dependent on the initial estimation. The initial guess in the optimization process is not as important as the manual design.

Finally, GA is fully based on probabilistic instead of the deterministic optimization process. In the case where the individual performs badly, but one of the chromosomes of its DNA is beneficial, there is still a chance for it to keep the good trait in the population. This feature leads to a higher searching capability within the whole solution space.

All those properties of GA enhance the chance of approaching the global optimized point. The overall flowchart of the process is shown in Fig. 3-3.

The first step of the process is the initialization. This step generates the initialized population $P[1]$ or uses recombined population $P[K+1]$ after the k th iteration. Each individual's performance, the junction temperature T , is evaluated. According to the performance, fitness score and the survival possibility of the individual is assigned. Selection is then performed based on the survival possibility of each individual. And a portion of the population can join the mating pool after the selection process. Then crossover happens by exchanging the features with each other the individuals in this mating pool and produces offspring P' with the mixed features in the mating pool. This group of children with other newly generated random individuals forms the next generation $P[k+1]$. A stopping criterion is then checked by either reaching the maximum number of iterations or the convergence of the results. Additional to the canonical GA, to enhance the performance of the optimization, a post-process by stochastically searching around the optimal point is engaged. Also, the parameters of GA are varying based on the optimization process, makes it adaptive to the convergence. In this dissertation, a customized Adaptive

Genetic Algorithm (AGA) is proposed with additional properties to the canonical Genetic Algorithm. These modifications can further improve the performance of the machine learning process. Detailed discussions are shown in the following sections.

3.5.1 Initialization

The optimization starts with an initialized population. Often, this population is generated randomly, for a larger explore area of the entire solution space. The solution space, as the set of all possible individuals of the algorithm, distinguish the initialization methods. As stated previously, individuals of this dissertation are mainly presented as a matrix. But the construction of the matrix is determined based on the solution space. Generally speaking, more complex initialization method can generate larger solution space, and a potentially better design can be found, however, the converging time to the optimized point can take longer as well. The initialized population is the set of random individuals of the solution space. The size of the population is determined based on the problem. The detailed construction of the solution space will be explained for each optimization method. Individuals of this population then went through the interface between MATLAB and COMSOL one by one for evaluation.

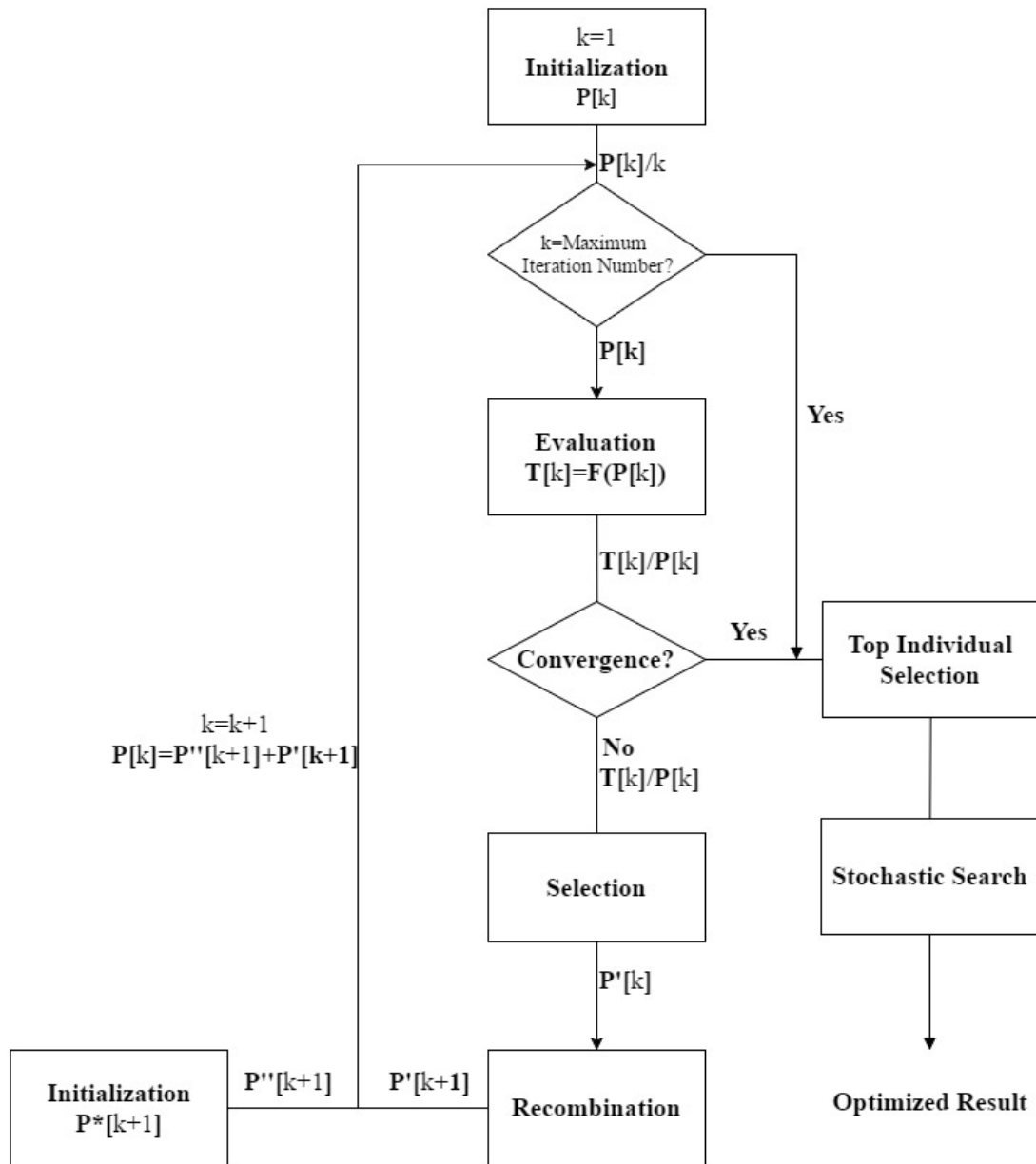


Fig. 3-3. Overall flowchart of the Genetic Algorithm

3.5.2 Evaluation

The fitness function is generated based on the optimization targets of the problem. Similar to the adaptation of each individual to the environment of the biological systems, this fitness function assigns the fitness score to each individual based on the evaluation performance. As designed evaluation process in this dissertation, DNA of one individual in MATLAB is transferred through the interface and express the features as the geometry structure in COMSOL, with other parameters assigned. FEA simulation is studied for this model and the target value is then reported back to the MATLAB as the performance. Fitness score is then calculated based on the performance. Those individuals with lower fitness scores are more likely to be eliminated and the rest survived individuals can enter the mating pool for crossover. Even though the computation time nowadays for FEA simulations are still in the order of minutes, the rapidly increasing computation capability can eventually result in a faster optimization process.

3.5.3 Selection

The key concept of the evolution of the biological systems is “Survival of the fittest”, as originating from Darwinian evolutionary theory. The definition of fit in biology is defined as reproductive capability. Darwin’s concept of the evolution can be best interpreted as: survival of the population will leave the most traits of itself to successive generations.

For each optimization iteration, only a portion of the population can enter the mating pool and possibly to breed offspring carrying its traits. The members of the mating pool

are selected through a fitness-based process, where the individuals with better performances are more likely to be selected. After the evaluation of the population, each individual has been assigned by a fitness score based on its performance. Survival possibility if the individual i , $s(i)$ is defined as the percentage of the individual i 's fitness score over the sum of scores of the population. Apparently, the sum of all survival possibilities of each iteration population is unity. Selection method varies based on the optimization goal and it is a stochastic process based on the survival possibilities. In this dissertation, roulette wheel selection is used based on the survival possibilities of the population, as shown in Fig. 3-4.

For the i th individual, the bet segment is located at the sharing interval $[\sum_{i-1} s(i), \sum_i s(i)]$. For each selecting action, a random number for 0 to 1 is generated indicating the rotation of the wheel. Whichever share of the wheel it lands, the representing individual of this interval will be picked up for the mating pool.

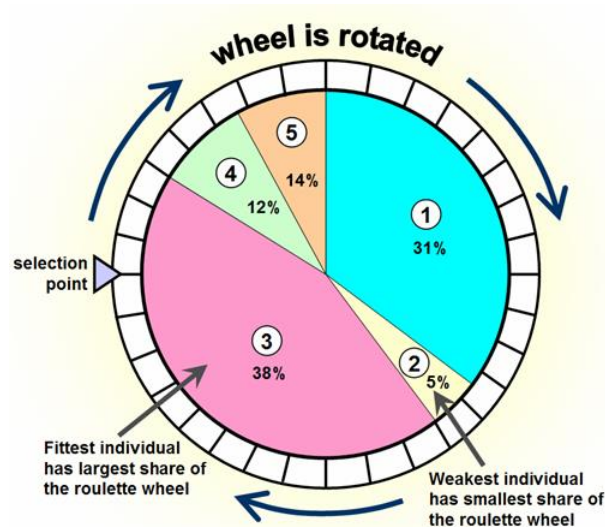


Fig. 3-4. Roulette wheel selection of GA

In this dissertation, as the concept of “adaptive algorithm”, a varying after-rotation-strategy takes effect based on the estimation of the population diversity and the level of convergence progress. For example, for the early period of the algorithm, the strategy is to explore the whole solution space for keeping a higher diversity of the population. Thus, no “put back” action is allowed. That means after each selection, the selected share interval will be removed from the selection candidates list and roulette wheel will be updated. In this way, the high diversity of individuals’ traits can be kept in the mating pool. Having a large group of too many identical or similar individuals can lead to the early-maturing solution which is stuck at the local optimization point. On the other hand, during the converging stage of the late period of the algorithm, higher “put back” possibility is defined. By putting back the selected individual, the individual with better performance will potentially have more offspring with its traits. The increasing elite individuals’ density of population is beneficial to the convergence. The variable strategies of “put back” balance the exploring and the converging trends during the process. A diversity control algorithm based on this concept is added to the main Genetic Algorithm. First of all, the kinship of individuals is defined as similarity in terms of the geometry structures. This definition of kinship varies from case to case. And the size of kin will determine whether to put back the selected individual to the roulette wheel. In a nutshell, the individual is more likely to be removed from the wheel if high kinship has been found in the mating pool. The maximum allowed size of each kin is a step function of the iteration number. Once the size of any one kin becomes larger than the half of the population size during one selection process, the individuals of kin have dominated the population. This can be regarded as one of the termination signs if the elite individual of each iteration is not changing for the next

10 iterations. And the optimization process will be claimed as converged. The overall flowchart of the selection process is illustrated in the Fig. 3-5.

After repeating the selection for the given number of times, which equals to the size of the mating pool, the selection process completes, and the rest of the individuals are eliminated. The selection builds up the trend that exactly matches the concept of the evolution theory, “survival of the fittest”.

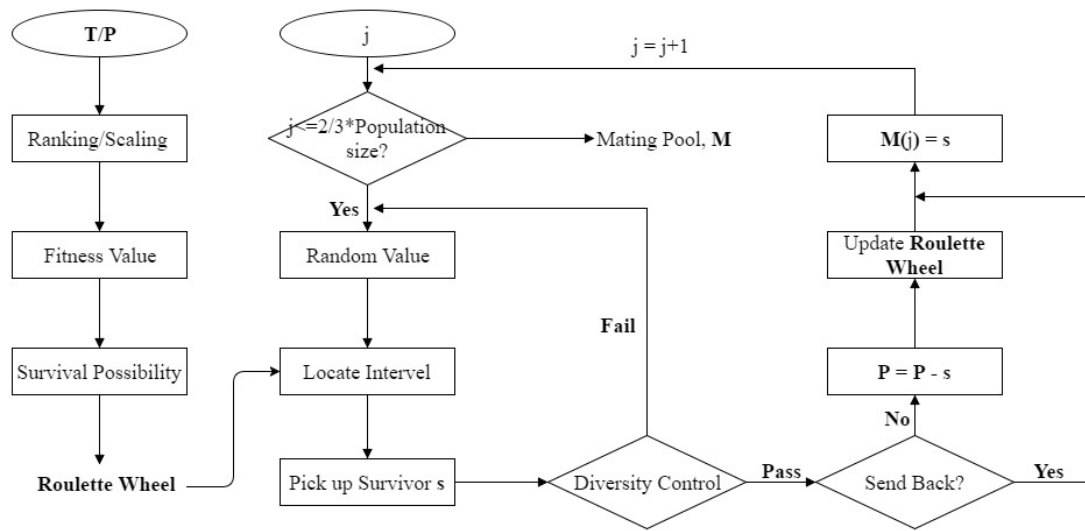


Fig. 3-5. Flowchart of the selection

3.5.4 Crossover

The action of exchanging of genetic material between homologous chromosomes is called as crossover. This action can be found in most of the living creatures. Crossovers in the evolution process produce many additional chromosomes besides the initialized population. Because of the crossover, the number of different chromosomes existing in the populations increases exponentially with iterations. Moreover, it can decouple some

beneficial traits of one chromosome from detrimental traits. This feature may result in a potentially better individual. Crossover is the key to achieve genetic diversity. Crossover is realized by breaking chromosomes of the parents into pieces and exchanging them to generate mixed chromosomes of the children. Crossover results in recombination of the chromosome information. By this way, the crossed children can bring the features of both parents. Possibly, the mixed features can lead to a superior performance than both of the parents. Crossover is the key to evolve the population.

For a mating pool with 16 survivors, it is divided into eight couples and each couple contains two individuals call as parents. For the individuals with multiple chromosomes, the crossover can only happen at the same position of the corresponding chromosome. Based on a given crossover possibility, only some of the parents can proceed to perform the crossover by exchanging segments of the parents' chromosomes, where the offspring inherit patterns of both parents. Other couples without crossover will exactly copy their DNA to the offspring. This randomness of the crossover is coded in the algorithm by comparing the random number of each couple to predefined crossover threshold to determine whether or not this couple will crossover. This randomness of crossover decides conservative and innovative trend of the optimization convergence. For the adaptive Genetic Algorithm, the crossover possibility is one of the adaptive parameters changing with the converging performance. This number is initially set as 0.8 and changed based on the convergence level and the degree of diversity inside the offspring.

3.5.5 Mutation

In addition to diversity increase due to crossover, mutation during the crossover plays another key role in evolution. In the process of duplication of the chromosomes, some of the gene locations in DNA may randomly convert to the other gene type with a small chance. For most of the time, either negligible effect or a fatal influence can be brought by this mutation. However, occasionally, the mutation may yield beneficial traits that improve the individual's performance, especially during the developing period of the population.

The mutation in the Genetic Algorithm leads an even higher diversity of the population after the crossover. For most of the cases, the chromosomes after mutation will be eliminated due to the worse performance. To maintain the stability of the population, a low mutation frequency is necessary. The decision of the mutation also depends on the mutation possibility of the algorithm. As the adaptive GA, the mutation possibility is also varying based on the maturity of the evolution.

In general, 5% mutation chance is allowed during each crossover at the beginning of the algorithm. After 50 iterations, this number goes down to 3%. After 100 iterations, the algorithm should be approaching the convergence point. Since most of the mutation at this period is harmful, for only 1% of chance, the mutation can happen. In most of the cases, the mutation is defined as replacing one of the gene's value with another random number. For different chromosome construction methods, mutation method is specifically designed.

3.5.6 Recombination

Except for the randomly created population of the first generation, the others contain the gene's information of previous generations. As a population in the biological systems, the majority of the individuals carrying traits from their parents locally. Species are sometimes isolated by strong barriers can be found, especially in a mature population. Sometimes, because of the movement of individuals, a few new individuals from outside of the population joined, named migration. The mating of the newcomers and the local population have a higher possibility of yielding individuals with the best performance. A similar idea is implemented in the Algorithm. For each iteration, a fixed number of individuals from the rest area of the solution space joined the population, called migration. Moreover, in order to keep the best individual of the iteration available, the elitism is guaranteed so that individual with the best performance will always be a member of the newly formed population. Even though this cannot be ensured in the biological systems, it has been shown to be powerful in terms of convergence acceleration of the algorithm. Take a population of 21 as an example, this population consists of 16 individuals carrying the “local” traits origin from the mating pool; 4 newly initialized individuals and the individual with the best performance of all time. This process is named recombination in the Genetic Algorithm. Each iteration ends with the recombination and the whole process repeated as evolution is happening.

3.5.7 Termination criterion

With the trend of approaching the convergence, the optimization progress is about to end. Whether or not the present solution can be regarded as the optimization result is determined by the termination criterion. For a general optimization problem where no minimum criteria present, three termination criteria are used to determine the convergence. Once two of three criteria are met, the optimization process will be terminated. Three termination criteria are stated as:

- **Budget cap termination:** The total iteration number reaches or has passed the maxima allowed iterations, or the total computation time has passed the allowed time budget.
- **Convergence termination:** The most optimized individual of each generation has reached a plateau and kept constant. It is defined as after successive iterations (usually tenth of the maxima iterations), no better results can be achieved.
- **Saturation termination:** The highest-ranking solution or its relatives has taken more than two third of the total population of any iteration. Relatives are defined as the similar design structure that less than 5% of the chromosomes are different.

For a specific design application, for example, to design a heat sink limiting the junction temperature below 120 °C, the desired function and time cost are the top two priorities. Design targets of such situation should convert from approaching the design to its ultimate performance to come up with a design that meet the design specs within the shortest time. Termination criteria become the following two statements:

- **Budget cap termination:** The total iteration number reaches or has passed the maxima allowed iterations, or the total computation time has passed the allowed time budget.
- **Performance termination:** The performance of any individual evaluated has met the design target.

Whichever criterion is met; the optimization process will be terminated. And the most optimized results will be recorded for further steps.

3.5.8 Post-process

Most of the time, genetic algorithms have a superior performance for approaching to a global optimal point. However, due to the termination criteria presented, the output solution may not always be the most optimized solution of the feasible region. The hybrid algorithm combining Genetic Algorithm and Nelder–Mead simplex method is proposed. After convergence of the genetic algorithm, individuals with high fitness scores are picked as a group for the post-process. A huge mutation possibility is added to this group for a deterministic search around the optimal point. Genes of the individuals are randomly adjusted to improve the fitness scores. After each iteration of the post-process, the heat sink individuals with the lowest fitness scores will be replaced with the one with higher fitness. This post-process repeats until the convergence of the group is approached.

3.5.9 Overall co-simulation process

Including all the steps of Modified Genetic Algorithm, the automatic iteration loop is built up as a co-simulation tool to support the proposed design methodologies. As shown

in Fig. 3-6, three major components are involved. Almost all essential steps of GA are coded in MATLAB, except the evaluation of each individual including geometry construction by both predesigned SOLIDWORKS part and expression of the chromosomes of individuals, simulation settings and results extraction proceed in the COMSOL FEA simulation software through this co-simulation process automatically. Using this proposed optimization structure, two major applications have been researched.

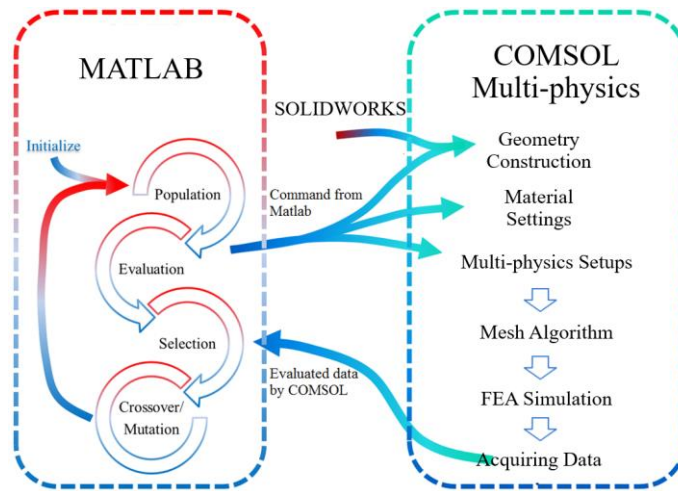


Fig. 3-6. Co-simulation interface

4. Multiple-Objective Optimization

4.1. OVERALL MULTI-OBJECTIVE OPTIMIZATION STRUCTURE

As stated in Liebig's barrel theory, also known as the Liebig's law of the minimum, “the capacity of a barrel with staves of unequal length is limited by the shortest stave”. When comes to the system level optimization, balancing of interact objects is more important than the optimizations on single targets. The same principle can be found during a power electronics converter design process. As shown in Fig. 4-1, a general structure of a power electronics converter/inverter includes multiple domains, i.e. the front and end filters, power stage, cooling system and others. Each of those domains can be individually treated as a “stave” of the “barrel” to be designed, where the amount of water this barrel can hold is regarded as performance of the overall system. That indicates, the overall performance of any converter is not determined by the most optimized component but limited by the weakest design point. Since power density optimization is the major focus of this dissertation, whatever combination of components that can contribute to the highest converter power density will be the optimized design. Because of the tradeoffs introduced in **Chapter 1**, one over-optimized component could lead to a destructive design of other components, e.g. the switching frequency vs. heat sink design. Multi-objective optimization should be used as a principle optimization structure to balance performance of all components together rather than the individual optimization of each component.

This overall algorithm of this multi-objective optimization is illustrated in Fig. 4-2.

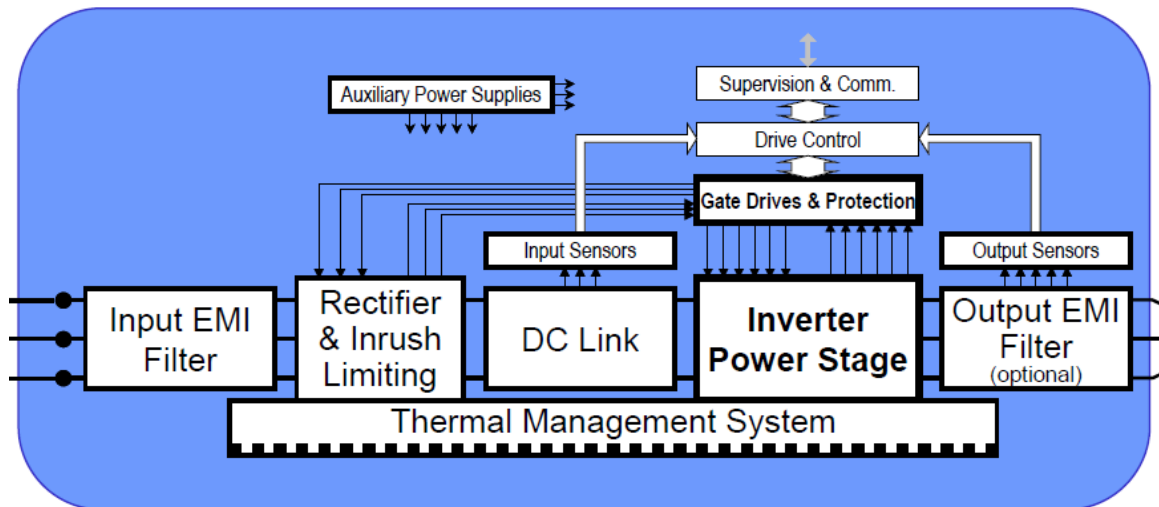


Fig. 4-1. The general structure of a power electronics converter

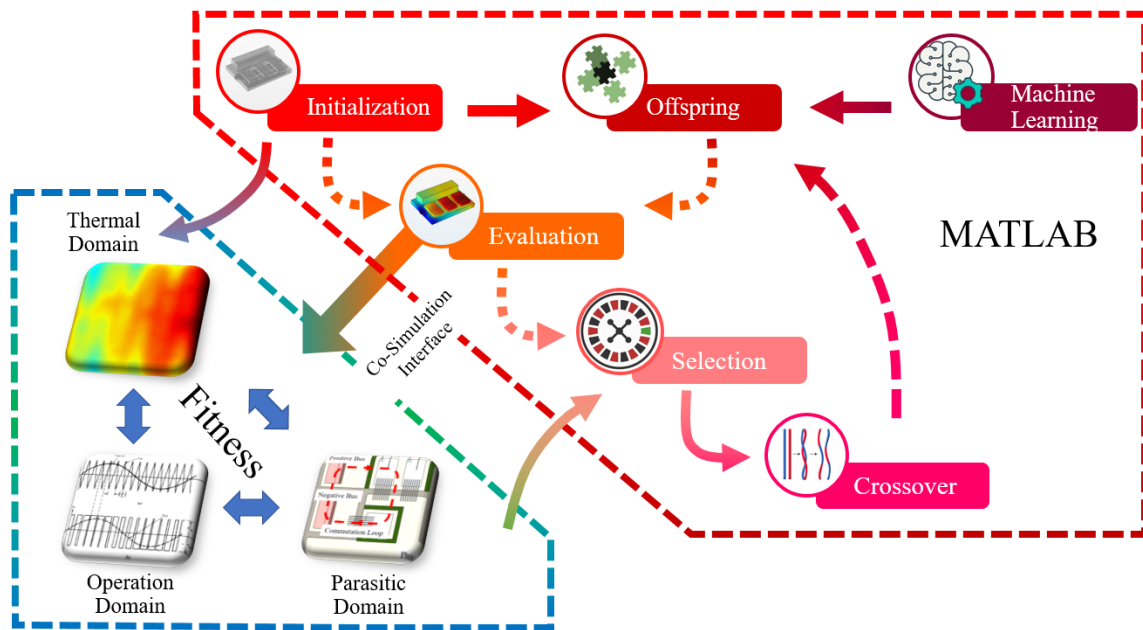


Fig. 4-2. Overall multi-objective optimization flowchart

The main optimization algorithm is constructed based on Genetic Algorithm. As described in **Chapter 3**, it is an automatic optimization process that evolves the target objects towards the fittest design based on the strategies learned from previous iterations.

On the right-hand side of the structure, main steps of GA including Initialization/Recombination, Evaluation, Selection and Crossover/Mutation are built in MATLAB as the detailed illustrated in **Chapter 3**. Besides the conventional GA steps, machine learning features are also introduced to the structure for a faster convergence. For the conventional initialization step of GA, all new individuals are initialed based on a random process constraint within the feasible region. However, the involvement of a high degree of randomness could hinder the smooth convergence trend and result in oscillations, especially during the ending period of GA. Instead of this total randomness, machine learning features that take the design trait strategies of previous elite individuals and initial new design with similar strategies can ensure the trend of convergence.

The left-hand side of the structure presents the evaluation step by a network of three individual domains, named “Heat Sink Structure” domain, “Device Layout” domain and “Operating Point” domain, for the fitness score calculation. For any power module design, evaluations of all domains are taken into calculation of the fitness score. Because of the interact relations between domains, the flowchart shown as Fig. 4-3 is proposed as the evaluation process. Each domain is evaluated individually and communicated through the co-simulation interface developed previously. The overall fitness score is then assigned to the input designed individual.

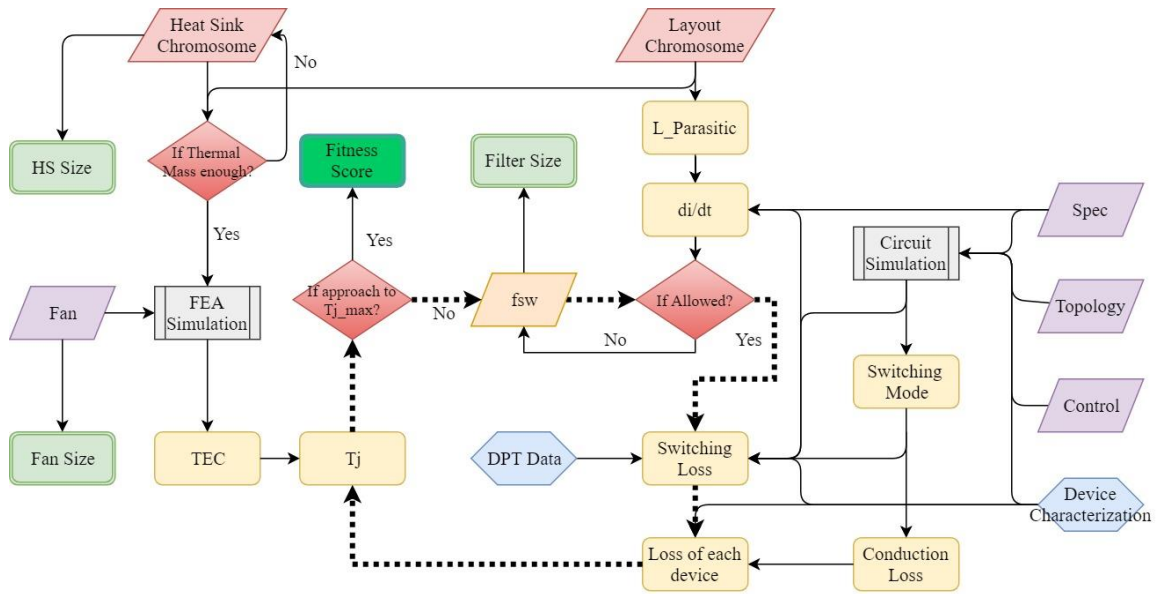


Fig. 4-3. Multi-Objective evaluation flowchart

The multi-objective evaluation is illustrated as this flowchart. Each block of this flowchart has different function and labeled in colors:

- Pink blocks are the design parameters of the power module input for evaluation;
- Orange block is the secondary optimization target for each sets of input parameters. This parameter is approached based on the given design and will also contribute to the overall fitness performance.
- Light green blocks are the fitness score/ evaluated results of each individual design domain and contribute to the overall fitness score;
- Dark green block is the overall fitness score that will be assigned to the designed power module.

- Gray blocks represent exterior operation other than the main algorithm. They are done by COMSOL and Simulink and connected to the main algorithm by the co-simulation interface. Those blocks take most of the evaluation time.
- Blue blocks are the experimental data extracted based on test results prior to the optimization. They are input to the flowchart as the device characterizations.
- Yellow blocks represent interior operation embedded in the main algorithm. They are constructed based on approximate mathematic models with data input from both gray or blue blocks;
- Purple blocks are pre-designed parameters, such as the circuit design, design spec, etc. Because of the limited scale of the optimization process, they are out of the scope and not to be optimized.
- Red blocks are the criterion of the iteration loop to decide if or not the design satisfy all the constraints.

4.2. FUNCTIONALITIES OF BLOCKS

4.2.1. Pink blocks

Pink blocks compose two main design parameters. Those parameters are the primary goals of multi-objective optimization, named as “chromosome” in terms of Genetic Algorithm. Each set of the two chromosomes determines one unique power module design. A power module design example is illustrated in Fig. 4-4 by a set of randomly generated chromosomes. This set of chromosomes include the design features of heat sink and the device layout.

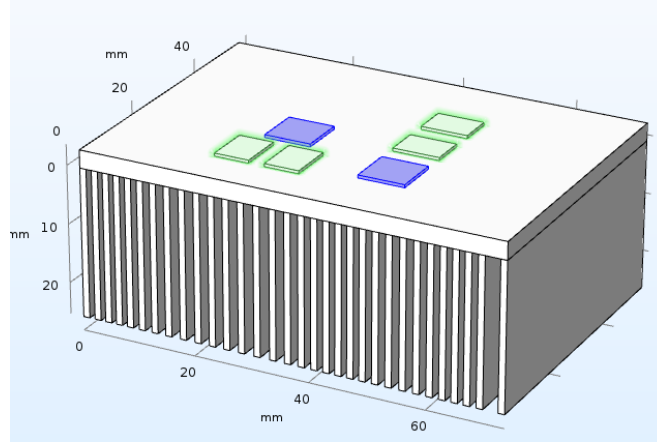
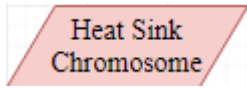


Fig. 4-4. Power module design example



Heat sink chromosome is the basic parameter of the Thermal Domain, located at the **Chapter V** of this dissertation. This chromosome determines the structure of the cooling system, such as the type of cooling system, detailed structure design of the heat sink and selection of fan/ pump. Design of the heat sink is based on the design of the cross-section, as shown in Fig. 4-6. It is constructed based on two pieces of chromosomes.

The first piece includes fundamental design parameters such as number of the fins, the thickness of fins, the height of fins, baseplate thickness and other overall substrate dimension, length and width.

The second piece of the chromosome, as shown in Table 4-2, determines the distribution of the fins.

This function is realized by fitting the discrete points to a density function of fin distribution as plotted in Fig. 4-6.

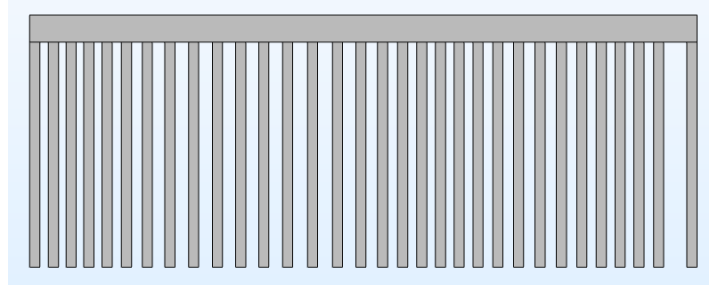


Fig. 4-5. Cross-section of the designed heat sink

Table 4-1. Fundamental design parameters

Fin Number	Fin Thickness	DBC Length	DBC Width	Fin Height	Baseplate
32	1.108	50.8	73.25	25.4	3.052

Table 4-2. Fin distribution

Fin Distribution									
1.136	1.193	0.937	0.968	0.886	1.116	1.780	1.031	1.185	0.825

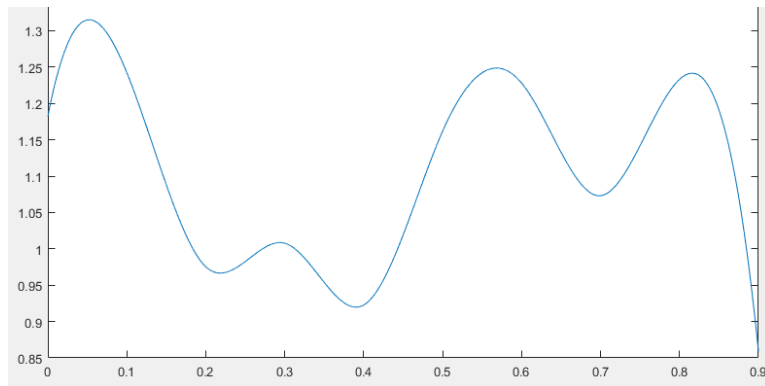
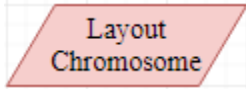


Fig. 4-6. Fin distribution density plot

At any horizontal location of the cross-section, the higher value found in the plot, of the higher fin density is can achieve locally. Combination of such two pieces of chromosomes result in the heat sink cross-section design shown in Fig. 4-5.



Layout chromosome is another important design feature that is proposed in the Parasitic Domain at **Chapter VI** of this dissertation.

This chromosome determines the layout locations, arrangement, and orientations of devices. For a design case of two MOSFETs and one Diode (2M1D) in one switch position, a random layout chromosome is generated and coded in Table 4-3.

Table 4-3. Layout chromosome

Upper Switch		
10.366	-1.209	112.877
Lower Switch		
-9.657	-8.774	313.36

Values of the first two chromosome columns represent the center location of the switches in a x-y coordinate. That means, the upper switches are centered at [10.36,-1.29] and the lower switches are centered at [-9.66,-8.77]. The last parameter of each row determines the arrangement and orientations of devices. Taking the last parameter of the upper switch, 112.877. as an example, this number can be decomposed into four sub-values: 1, 1, 2, and 0.877.

The first value indicates the arrangement of devices. As of this 2M1D case, three types of arrangements are available, as shown in Fig. 4-7.

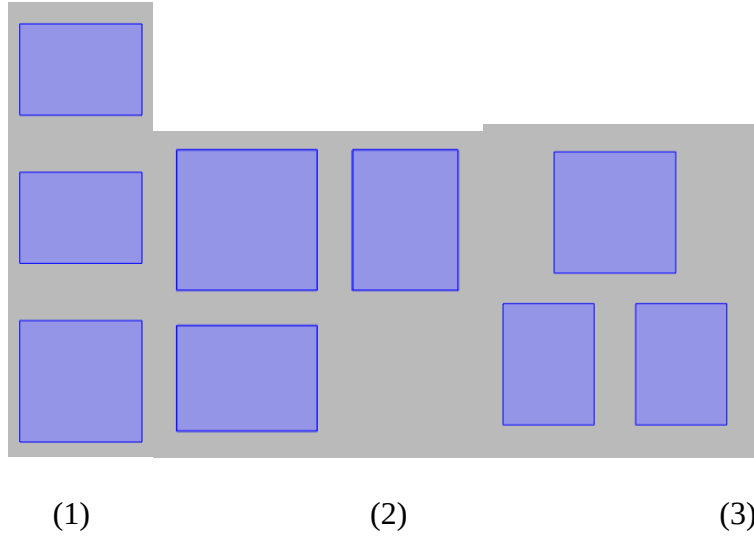


Fig. 4-7. Types of arrangement

In this application, MOSFETs are represented as an 8×6 mm rectangle and Diode takes a footprint 8×8 mm square. Those details are only needed in the thermal domain and regarded the heat source distribution profile. For the process in parasitic domain, power loop extraction will only use outer boundary of the devices as the reference to avoid overlap of devices and construct the current path. As what got from the chromosome, the arrangement type of the upper switch is one.

The second value determines the relative position of MOSFETs and Diodes inside the boundary. Taking the first arrangement type as example, there are two possible relative position: either the diode is located in between of the MOSFETs (M-D-M) or on the (M-M-D). With more devices involved, more possible relative position is available, so as the range of the second value.

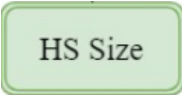
The third value is assigned as the orientation of the devices, ranging from 1 to 4. The orientation of devices is this value $\times 90^\circ$ from the default directions of Fig. 4-7. For these upper devices design, the rotation angle is $2 \times 90^\circ = 180^\circ$.

The last value comes from the decimal part of this parameter, e.g. 0.877. This value determines the separation distance between devices. As what has defined by the constraints, default separation between devices is 2mm. In addition to the original separation, an extra separation distance of $0.877 \times 2\text{mm}$ is included in this design which makes the total separation as $(1+0.877) \times 2\text{mm} = 3.75\text{ mm}$. This distance could impact the thermal coupling issue in the thermal domain.

4.2.2. Green blocks

Light green blocks

As illustrated in **Chapter I**, two components contribute highest portions to the power density, i.e. cooling system and the passive components. Design of either component can impact the overall system performance. The fitness score of each component locates at the green blocks as the individual contribution to overall fitness score.

 Heat sink power density contribution, ($Fitness_{HS}$) is calculated from heat sink design chromosome. If the volume matrix is used, the volume of outer box that covers the heat sink body is measured and calculated; If the weight matrix is the concern, the weight is calculated in COMSOL based on density properties of material and the volume of each material.

 Fan power density contribution origins solely from the datasheet of selected fan as of both volume and weight information. Since the fan design

in this dissertation is out of scope, the contribution of the fan (Fitness_{Fan}) becomes a constant value of C_2 .

Filter Size

Filter power density contributing portion is determined majorly based on the function of several operating parameters including switching frequency. Because of the complexity of this evaluation, only an approximate model will be considered. Take a boost converter filters design as example, the capacitance is calculated as

$$C_3 = \frac{I_{out} \cdot D}{2 \cdot V_{Ripple} \cdot V_{out} \cdot f_{sw}} \quad \text{Eq. 4-1}$$

And the inductance is calculated as

$$L = \frac{D \cdot V_g}{2 \cdot I_{Ripple} \cdot I_L \cdot f_{sw}} \quad \text{Eq. 4-2}$$

Since most of the parameters come from the circuit simulation which is regarded as constants, the only variable of the functions is the switching frequency located at denominators of both equations. It is reasonable to approximate that the volume, or the weight of the passive components is roughly inverse proportional to the switching frequency. Thus, the fitness score of the filter size (Fitness_{Passive}) can be modeled as:

$$\text{Fitness}_{Passive} = C_3 / f_{sw} \quad \text{Eq. 4-3}$$

Where C is a constant and the f_{sw} is the optimal switching frequency of the power module design.

L_{Parasitic}

Parasitic inductance also contributes to the overall fitness value. Though it may not directly impact the overall power density, this parameter is critical to other components of the power density calculation. As what has been inputted by the layout chromosome, a 2D model of the devices outer boundaries is plotted in Fig. 4-8.

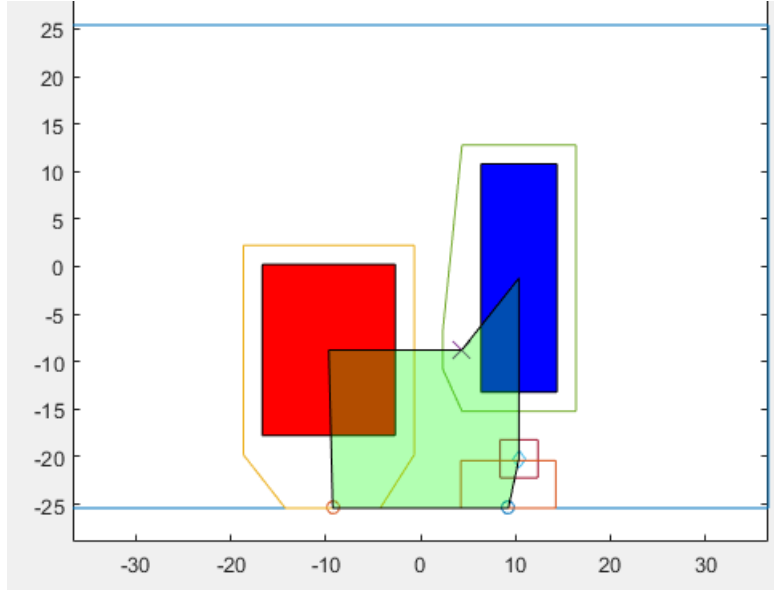


Fig. 4-8. Power loop extraction based on the given layout design

Parasitic inductance, as a function of the power loop profile, is extracted based on the method in **Chapter VI**. The optimized terminals, wire bonds locations and the minimum are found and current path from by those elements contribute to the fitness value of this block ($Fitness_{Parasitic}$). This value is mainly determined by the power loop information, both the loop area and the loop length and it is modeled as Eq. 4-4.

$$Fitness_{Parasitic} = C_4 \cdot function(A_{Loop}, L_{Loop}) \quad Eq. 4-4$$

Where C_4 is a constant, A_{Loop} is the power loop area and L_{Loop} is the power loop length.

Dark green block



Contributed by all values located in the light green blocks, the overall performance of the fitness as a combination of such. The default calculation of the fitness uses product of all inverse value of the weighted light green blocks, as calculated by. Obviously, the larger fitness score, the better design it has achieve.

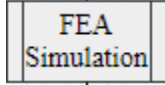
Fitness

$$= \frac{1}{Fitness_{HS}^{\alpha} \cdot Fitness_{Fan}^{\beta} \cdot Fitness_{Passive}^{\gamma} \cdot Fitness_{Parasitic}^{\delta}} \quad \text{Eq. 4-5}$$

$$= C \cdot f_{sw}^{\gamma} / V_{HS}^{\alpha} \cdot A_{Loop}^{\delta}$$

In this formula, C is a coefficient to scale the fitness value. Parameters such as $\alpha, \beta, \gamma, \delta$ are weight factor in terms of the importance of each component and are defaulted as unity. The Fitness value, as the key of to qualify the design, will be assigned to each sets of chromosomes for further learning process. The survival possibility in GA are also determined by this overall fitness score.

4.2.3. Gray blocks



With the set of design chromosomes inputted to the developed co-simulation interface, this block translates the chromosomes to the actual three-dimensional model in COMSOL. In this multi-objective flowchart, the desired results evalauted by the FEA simulation is not for the junction temperature profile but the MTEC model of the given module design. Thus, the power losses used in this block are not the actual losses but the sets of probe data that can construct an accurate MTEC model for the fast junction temperature estimation in the switching frequency iteration loop.

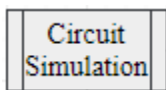
The mechanism of this interface is based on integrating MATLAB Code with COMSOL Multiphysics. Since all design features are expressed in a string of numbers in MATLAB, it has to be translated to a feasible language that COMSOL can recognize. As each operation done in the COMSOL, there is a corresponding Java command code generated. Java seems to be a perfect language for the communication between MATLAB and

COMSOL. Instead of directly controlling the COMSOL, using MATLAB to prompt Java command as lines of pre-coded instructions and imported into the COMSOL can eliminate the involvement of manual operation. This interface enables the automatic optimization procedure with two major functions:

The first function is to set up the model in COMSOL. As each input from the MATLAB to the block, it contains the general information including material properties, multi-physics settings, and mesh algorithms; the design details including the device layout locations, fin number, baseplate thickness, fin distribution, the fan curve; and the operation parameters including the power losses of each devices. All information need to be translated into the actual model and physics settings, through the positive path from MATLAB to COMSOL.

The second function is to analyze results and report them back to MATLAB. After the completion of FEA simulations, profiles such as the temperature distribution are generated. Though the negative path, from COMSOL to MATLAB, such results are transferred back to the main algorithm in MATLAB. Fitness score is then assigned based on the evaluation results.

Since block consumes the majority of the computation time. Thus, the optimization for speed on this block is critical which is mentioned in **Chapter V**. Additional approximations for repeatable FEA simulations to construct MTEC are introduced in **Chapter VII**. By decoupling the multi-physics simulation, instead of the process both flow and thermal simulation simultaneously, a two-step study essentially reduces the total computation time.

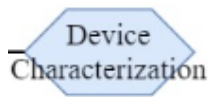


Circuit simulation provides necessary information to the overall optimization system. Based on the specs of design, control strategy, circuit

topology and device characterizations, the circuit simulation is implemented in Simulink prior to the beginning of the overall evaluation. Information such as both peak current and the RMS current value can be acquired based on the simulated results. Those simulated parameters along with the actual devices characterizations inputted from Blue blocks a detailed loss profile among devices. As one of the prerequisites of the process, an accurate loss profile is important to achieve the high optimization performance.

4.2.4. Blue blocks

Blue blocks are the experimental data obtained prior to the optimization. Data such as the on resistance and the switching loss per transient are input to evaluation flowchart.



Static Characterization is tested based on drain current vs. voltage drop output characteristics of the semiconductor device at the different gate to source voltage and varied temperature. A set of test data shown in Fig. 4-9 is plotted as an example. Based on the output characteristics, the on-state resistance is calculated and as fitted to a function of drain current level at the certain test temperature. This static characterization will be used to calculate the conduction loss by inputting to the corresponding block.



Dynamic Characterization is evaluated based on Double Pulse Test (DPT) as the schematic of the experimental setup shown in Fig. 4-10 and hardware setup in Fig. 4-11. The device under test (DUT) is placed at the lower side of the phase leg and is controlled by the double pulse pre-set program in DSP, and the upper side of the phase leg is equipped by the inductor as current source paralleled with a free-wheeling diode for the current conduction during the off period.

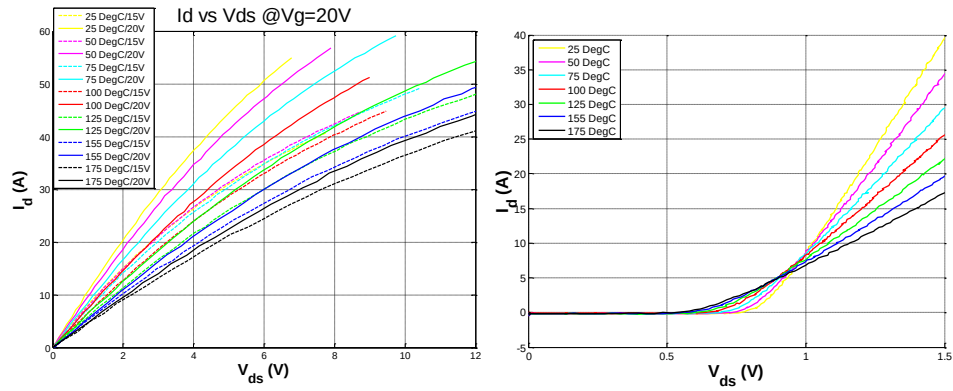


Fig. 4-9. Static output characteristics of active and passive power devices.

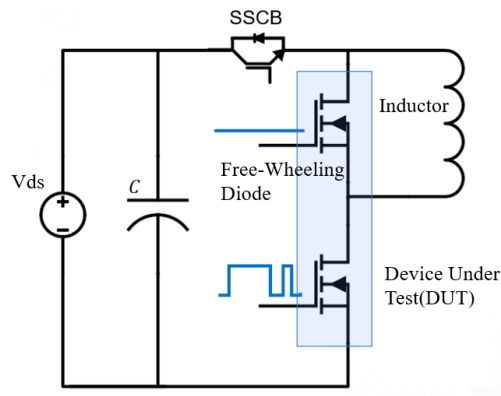


Fig. 4-10. Schematic of the double pulse test setup

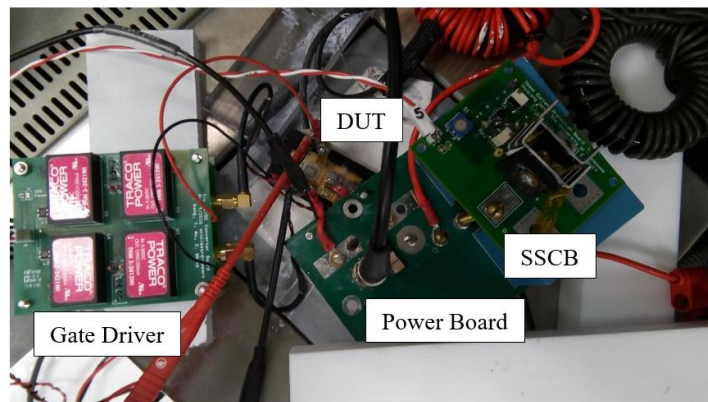


Fig. 4-11. Experimental setup for the double pulse test

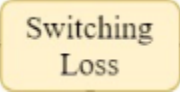
Double pulse tests are carried out at different current and voltage levels and the turn-on and turn-off energy losses at each test point are also calculated with varied temperatures. Additional information such as the current operation modes will also impact the loss of each device, which will be detailed explained in the following yellow blocks section. Data generated by this dynamic DPT characterization are then inputted to the switching loss block to calculate the actual switching loss of the module.

4.2.5. Yellow blocks

Yellow blocks appeared in this flowchart are assigned with the functions of interior operation that are embedded in the main algorithm. All calculations are approximated based on mathematic models with data input from either gray or blue blocks;

In total seven blocks are presented in this flowchart, named MTEC, T_j , di/dt , Switching Loss, Conduction Loss, Loss of each device. They can be categories into three functions: the power loss calculation, junction temperature estimation and determination of switching speed limit.

Group one: Loss calculation

 Switching loss occurs during every switching transient due to the overlap of raising current and dropping voltage of turn-on transient and dropping current and raising current of turn-off transient. Even though the switching speed is one of the impact factors of overlap time, which will further impact the switching loss calculation. This effect has been ignored to simplify the overall structure. In this flowchart, a constant energy loss per switch transient is assumed and calculated based on the double pulse test

data imported from previous blue block. Additional information provided by circuit simulation block determines the current waveform of each device. The profile of those waveforms further decides the operation mode of each device, i.e. continuous, discontinuous, ZVS, and other switching behaviors, which is important for the precise loss calculation.

Taking a buck converter as shown in Fig. 4-12 as an example, the actual switching loss of the circuit, especially the switching loss of the upper MOSFETs, could be significantly different from each other due to different operation modes. The best indicator to distinguish different operation modes is the inductor current, labeled as I_L . According to the inductor current profile, there are two major types of operation modes:

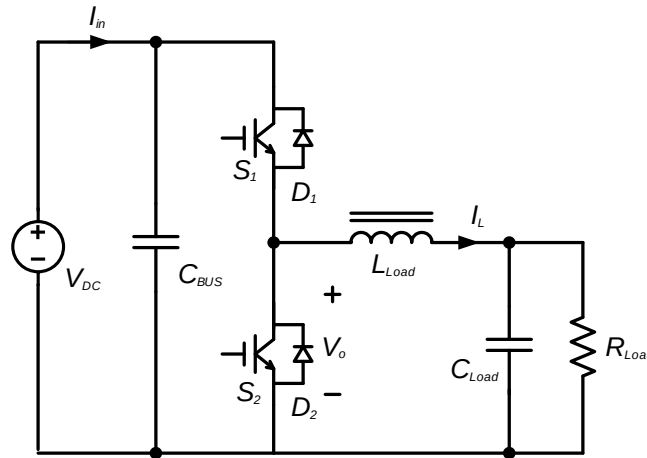


Fig. 4-12. The circuit diagram of phase-leg power test in Buck topology.

Mode 1: If the inductor current can go negative, a ZVS turn-on or partially ZVS turn-on of the upper switch can be guaranteed, which reduce the switching loss of the upper switch. Besides that, the turn-on transient of the lower MOSFET is always ZVS as the anti-

parallel diode D2 will always freewheel the load current and clamp the MOSFET voltage before turning on S2 once a proper dead-time is implemented. In such case, the switching losses of the phase-leg only include the turn-off losses of both MOSFETs. Based on the double pulse test data, the turn-on losses commonly dominate the switching losses. So, Mode 1 will lead to a much lower switching loss if the switching current is the same.

Mode 2: In other cases when the inductor current never goes negative, the inductor current is freewheeling through the anti-parallel diode D2 after the turn-off transient of lower MOSFET S2. Due to the voltage clamping, a ZVS turn-off of the lower device is achieved. Then, S1 turns on and all the inductor current will commute from D2 to S1, ending up with a hard turn-on switching event for the upper device. The switching losses of the phase-leg include the turn-off loss and turn-on loss of the upper device.

Moreover, the switching loss is not a constant value since the current and voltage magnitudes are not constant as well. The instantaneous value of current stress i_L and voltage stress v_0 during switching transients should be used, instead of average current through and average voltage across the switches S1 and S2. This phenomenon is illustrated in the waveform example as shown in Fig. 4-13. Basically, the turn-on transient of S1 and the turn-off transient of S2 occur during the inductor current reaches the valley, while the turn-on transient of S2 and the turn-off transient of S1 happens at the peak of the inductor current.

Moreover, for most of the operation points, i.e. drain current and blocking voltage of the switching time, no exact information can be looked up in the DPT data. Thus, the linear scale should be made to estimate the actual switching energy loss at a given point. Multiplying by the updated switching frequency from the loop which comes from the

orange block as the secondary optimization parameter, the switching is calculated based on Eq. 4-6.

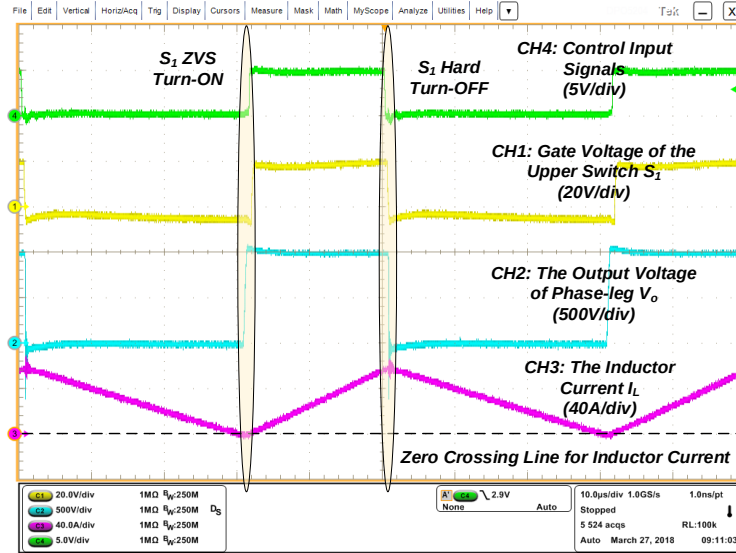


Fig. 4-13. The experimental waveforms example of a Buck converter

$$P_{sw} = (E_{on} \cdot \frac{V_{off}}{V_{offRated}} \cdot \frac{I_{on}}{I_{onRated}} + E_{off} \cdot \frac{V_{on}}{V_{onRated}} \cdot \frac{I_{off}}{I_{offRated}}) \cdot f_{sw} \quad \text{Eq. 4-6}$$

This modeling takes the advantages of the circuit simulation and used the dynamic operation parameter as the reference. Without this model, a significant error that can introduce more than 50% extra switching loss will be taken into the thermal design and result either an over-designed heat sink or an under-estimated switching frequency.

Conduction Loss

Besides the switching loss, conduction loss is another dominate parameter.

This block uses the temperature dependent static characterizations of the devices and the circuit profile origins from the circuit simulation. Conduction loss calculation of MOSFET has been well-modeled, based on the RMS value of the drain

current, the on-resistance and operating conditions, including the modulation index and power factor. Similar equations have also been well-developed for IGBTs and Diodes.

$$\begin{aligned}
 P_{M,cond} &= P_{M,forward_cond} + P_{M,reverse_cond} \\
 &= (I_{M,f,pk}^2 R_{on,M}) \left(\frac{1}{8} + \frac{1}{3\pi} M \cos \phi \right) \\
 &\quad + I_{M,r,pk}^2 R_{on,M} \left(\frac{1}{8} - \frac{1}{3\pi} M \cos \phi \right)
 \end{aligned}
 \tag{Eq. 4-7}$$

$$\begin{aligned}
 P_{D,cond} &= (I_{D,pk}^2 R_{on,D}) \left(\frac{1}{8} - \frac{1}{3\pi} M \cos \phi \right) + I_{D,ave} \\
 &\quad * V_f \left(\frac{1}{2\pi} - \frac{1}{8} M \cos \phi \right)
 \end{aligned}
 \tag{Eq. 4-8}$$

As the loss information generated from two above blocks, the specific loss distribution profile among devices is then determined in the following block.

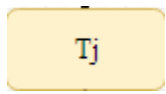
Loss of each device As one of the key information required by MTEC of **Chapter VII**, the detailed loss distribution across the DBC horizontally is necessary for accurate analysis of thermal coupling effect. Since the total loss of each type of devices. i.e., lower and lower MOSFETs and Diodes have been calculated, each device will be assigned based on its type and the number of paralleled devices. This profile will be then used in MTEC model for the junction temperature evaluation.

Group two: Junction temperature estimation

The second group of blocks is designed to estimate the junction temperature of the power module with the updated loss profile. Without relying on FEA simulations, the temperature profile inside the switching frequency iteration loop is calculated based on MTEC yellow block.

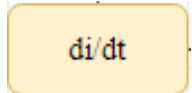
MTEC As proposed in **Chapter VII**, MTEC model is constructed based on sets of the FEA simulation profile. Each set of simulation profile has different artificial loss distribution among all devices. The number of the sets input is equal to the

number of devices for a unique and accurate MTEC. Based on profile sets, parameters of the MTEC is extracted using a sub-GA system. Optimization of GA is the set of resistance parameters of the MTEC network and the fitness function is the sum of estimation errors introduced by the MTEC compared to the actual thermal performance simulated by FEA. This MTEC model is then used for junction temperature estimation with a sequence of updated loss profiles.

 Junction temperature estimation block has two input terminals. While the input from MTEC block is constant, the other input from the loss group keeps changing with the iterative switching frequency updated. Since the overall fitness function focuses only on the maximum junction temperature, the output of this block is the maximum junction temperatures of each type of devices as well. Those updated temperatures will then be compared to the constraint limit in the following step.

Group three: Upper limit of switching speed

The third group of blocks contains only two functional blocks for the switching speed limit estimation. The first block is the parasitic calculation block. Though this block is painted in green categorized as the output fitness function, it also delivers the internal parameter, the parasitic inductance, to second switching speed block.

 As explained in the background section in **Chapter II**, the switching speed is limited due to the available voltage margin for the voltage spike introduced during the turn-off transient. As a given design, the rated voltage and the blocking voltage of semiconductor devices are fixed beforehand. Thus, the margin for the voltage overshoot spike is the difference of rated voltage and the blocking voltage, plus the

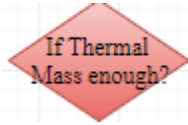
consideration of design margin, for example, 30%. To meet this constraint, the maximum switching speed is calculated by

$$(di/dt)_{max} < (V_{rated} - V_{block}) \times 70\% / L_{parasitic} \quad \text{Eq. 4-9}$$

Even though, for the real case, it is limited also by the switching capability of the gate driver and the gate loop parasitic elements. To simplify the multi-objective optimization in this dissertation, the gate drive related parameters are all assumed as ideal. And the only limiting factor is the voltage overshoot.

4.2.6. Red blocks

Red blocks are the criterion based on the constraints. They are involved in the iteration loop as a conditional operation that determines whether the updated design will fit the constraints and output yes/no statement. As introduced previous, two major factors limit the switching frequency, i.e. the switching speed di/dt limited by the parasitic inductance and the rated voltage for overshoot spike and the excessive losses additionally heat up the device limited by the maximum allowed junction temperature.



This criterion block “**If Thermal Mass enough?**” is particularly designed to justify the heat sink designs. As named Thermal Mass, it will exam the design impact on the dynamic performance of the heat sink while being heated up during the high-loss period. As generally speaking, the smaller thermal mass one system has, the quicker this system can be heated up. Even the losses calculated from yellow blocks are relatively low, this is the total energy loss on average of a switching period. During a fast switching transient, the energy loss over this short period could be extremely large and lead to a huge temperature spike if there is not enough thermal mass to slow this process down.

The thermal mass is modeled as the total weight multiplied by the thermal capacity correspondingly. Since most of the thermal mass is provided by the heat sink, the criterion block is to determine the lower limit of the heat sink mass. For most of the time, the design should pass the criterion. However, if the mass is too small, for example, a thin baseplate with low fin number, this design will be rejected as the fitness score will be assigned as zero.

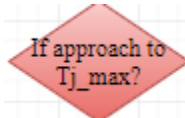


This criterion block “**If allowed?**” is after the switching frequency block.

By given the constraints, which is the switching speed, the minimum sub-interval length of any switching overlap period should be larger than the switching time plus the dead time. As a rough estimation, the switching overlap time is double of the current drop time and the minimum period length calculated as four times of the total turn on and turn off time, which is in total eight times of the current drop time. And the corresponding switching is then limited by

$$f_{sw_limit} < (di/dt)/(8 \cdot I_{peak}) \quad \text{Eq. 4-10}$$

Generally, 70 kHz as a fair assumption is taken in this application as a constant upper limit. By those constraints, this block can let the updated switching pass only if it is smaller than either f_{sw_limit} or 70 kHz.



This criterion block “**If approach to Tj_max?**” locates after the junction temperature calculation block. As the overall design target, to maximize

the power density of the design module, one of the approach rules is to fully “unitize” the “available” junction temperature to avoid the overdesigned system. The block is designed inside this loop to make sure this approach is guaranteed. If the junction temperature is below the limit, there should a room for a higher switching frequency that can further

reduce the filter size. The output of this criterion block becomes “No” with a positive feedback that will increase the switching frequency. On the other hand, if the junction temperature is over the upper limit, this design will damage the module. The output of this criterion block is still “No” but with a negative feedback that decreases the switching frequency. When approaching the optimized point, the junction temperature should be slightly below the temperature limit and criterion block should output “Yes” and proceed to the overall fitness calculation block.

5. Thermal Domain

This domain focus on the heat sink optimization. The target of this domain is to design the heat sink with the best thermal performance. Two approaches can be made based on the fitness function. If the junction temperature is the design target, the fitness function will be the maximum junction temperature of the module. This approach is straightforward that can be achieved by optimizing the design of heat sink individually. If the volume is the design target, the junction temperature will only contribute to the penalty value that if the design exceeds the maxima allowed junction temperature, a penalty will be added to the fitness value. The basic logic flow of this is illustrated as shown in Fig. 5-1

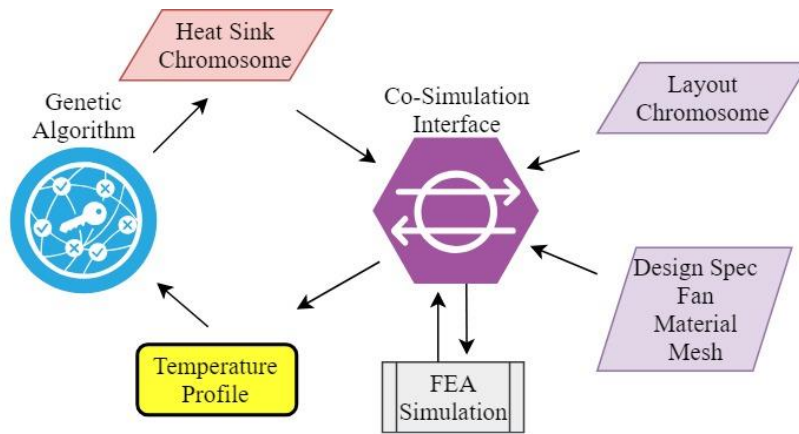


Fig. 5-1. Design flowchart of Thermal Domain

Since this chapter focuses only on the heat sink design, other parameters, such as the layout of devices, and all other circuit information are treated as given parameters. Genetic Algorithm interface, as constructed in the previous chapter, is used to generate heat sink

design and input to the co-simulation interface along with all pre-design parameters. Though the interface, FEA simulation is run in COMSOL and the simulation profile is reported backward to the GA for analysis. This is the overall structure of the optimization used in this chapter.

5.1. CONVENTIONAL OPTIMIZATION APPROACH

In most of the low power applications of power electronics module, the passive and active air-cooled solutions are commonly used due to the simple system. Of them, the passive air-cooled approaches, due to the low air flow rate, is not commonly seen except for in the applications low power losses, since the heat transfer coefficient h is only about $2 - 25 \text{ W/(m}^2\text{K)}$. More commonly, the implementation of the forced air-cooled solution with a fan can boost the heat transfer coefficient, h up to $25 - 250 \text{ W/(m}^2\text{K)}$. And this is the focus of the air-cooled solutions in this dissertation.

The air-cooled thermal management method dissipates heat from the contact surface of the heat sink to the surrounding air through thermal convection. The governing equation of convection is shown in Eq. 5-1

$$Q = h \cdot A \cdot (T - T_A) \quad \text{Eq. 5-1}$$

Where h is the thermal convection coefficient and it has a positive relation to the flow velocity. A is the surface area of the convection and $(T - T_A)$ is the temperature difference of the heat sink surface to the ambient air.

Empirically, air-cooled heat sink's design target can be simplified as to maximize the surface area of the heat sink, A . Heat sinks with fin-structures, due to the ease of manufacture and relatively large surface to volume ratio, have been selected as the primary

design outline. From decades of analysis and optimization, the performance of such the heat sink has reached the boundary. To further improve the performance, loose design constraints for a higher design freedom need to be considered. Thus, several designs approached have been proposed.

5.2. CASE STUDY

A design case, as 50 kW three-phase inverter with a 1000 V DC link is proposed as the optimization problem. Design spec is summarized in Table 5-1.

Table 5-1. Inverter design specs and operating points

Parameters	Value
Total Power Rating, P	50 kW
DC Bus Voltage, V_{DC}	1 kV
Power Factor(grid side), $\cos\theta$	1.0
Modulation Index, m_a	0.95
Line-to-line Voltage RMS, $V_{ll(RMS)}$	480 V
Switching Frequency, f_{sw}	20 kHz
Operating Temperature, T	150 °C
Gate Voltage, V_{gs}	20 V

The basic design idea of the phase-leg module is a face-to-face DBC layout that can put two heat sinks on the top and bottom of the DBA pair. The direct bonded copper (DBC) substrate is then designed in the topology of Fig. 5-2. Designed DBC for a switch in the phase-leg module.

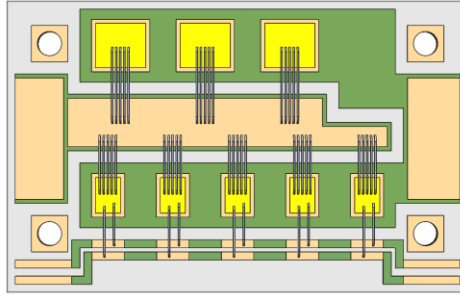


Fig. 5-2. Designed DBC for a switch in the phase-leg module

For one switch position, since the design spec of the module is 1000 V DC link voltage, SiC devices with high rated voltage need to be selected. In addition to carry the peak line current, five bare semiconductor die of 1700 V/34 A SiC MOSFETs and three of 1700 V/50 A SiC Schottky diodes are designed on the DBC. Characterizations of both SiC MOSFETs and SiC Schottky diodes are tested by static measurement and double pulse test (DPT). As shown in Fig. 5-3, losses can be calculated based on the characterization data.

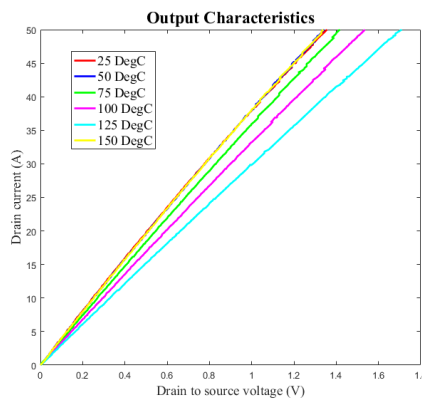


Fig. 5-3(a). SiC MOSFET static characteristics with 5 devices paralleled,

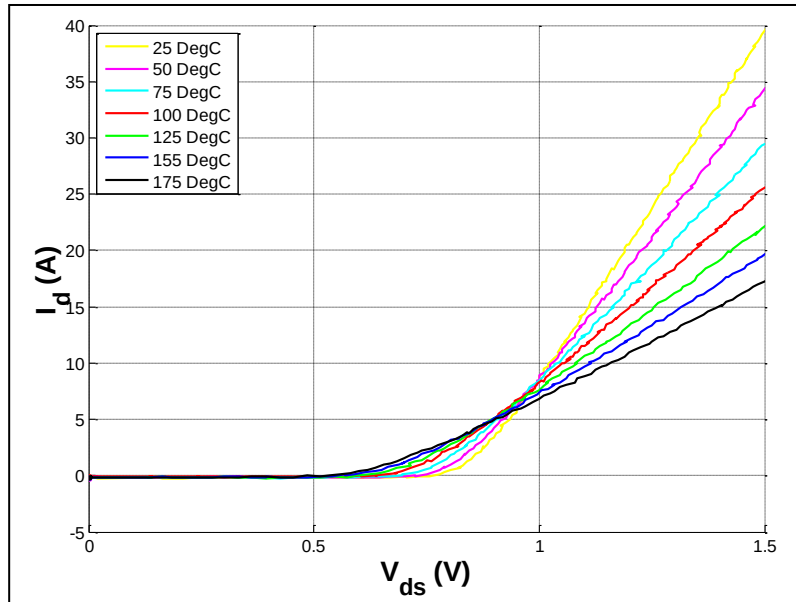


Fig. 5-3(b). SiC diode forward characteristics under different temperatures.

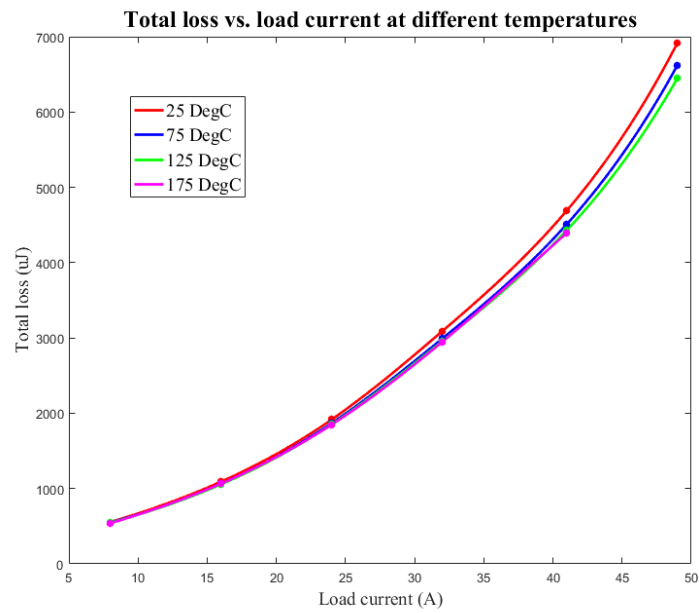


Fig. 5-3(c). Total loss per SiC MOSFET switch at different operating conditions.

Total losses of one phase-leg module are calculated as the sum of two terms: Conduction loss and Switching loss.

- Conduction Loss

Assuming all the current go through the MOSFETs' channels, the positive current I_{rms_P} and negative current I_{rms_N} can be derived as by Eq. 5-2 and Eq. 5-3..

$$I_{rms_P} = \sqrt{2} \cdot I_{ll(rms)} \cdot \sqrt{\frac{1}{8} + \frac{m_a \cdot \cos\theta}{3\pi}} = 40.42A \quad \text{Eq. 5-2}$$

$$I_{rms_N} = \sqrt{2} \cdot I_{ll(rms)} \cdot \sqrt{\frac{1}{8} - \frac{m_a \cdot \cos\theta}{3\pi}} = 13.23A \quad \text{Eq. 5-3}$$

Since the on-state resistance of five parallel devices at 125 °C is measured as 35 mΩ, the switching loss of the switch position is,

$$P_{cond} = I_{rms_P}^2 \cdot R_{ds(on)} + I_{rms_N}^2 \cdot R_{ds(on)} = 62.8W \quad \text{Eq. 5-4}$$

- Switching Loss

The switching loss, on the other hand, is calculated based on the dynamic double pulse test data shown in Fig. 5-3. Since each switch only presents switching behaviors during half fundamental cycle, the current used for loss calculation is counted as only half of average drain current of the module, that is around $(85/5)/\pi=5.3A$. However, this DPT test data is only valid for the single device at 600V. A linear scale using 1000V instead of 600V DC voltage should be considered. The energy loss of each device switching period is calculated based on the test data of 8A, 600V

$$\frac{5.3A \cdot 1000V}{8A \cdot 600V} \cdot 600\mu J = 662\mu J \quad \text{Eq. 5-5}$$

The switching loss of the switch position with 5 MOSFETs at the switching frequency of 20kHz is:

$$662\mu J \cdot 5 \cdot 20kHz = 66.2W \quad \text{Eq. 5-6}$$

The total loss dissipated by one switch position, by summing up conduction and switching losses, is 129W. This loss is used as the heat source of one heat sink.

The maximum junction temperature of the devices during the design process is set to be 125 °C at the room temperature with a 20 °C design margin and a 40 °C environment margin when operating in a high ambient temperature surrounding.

As a co-simulation, DBC and other components except heat sinks are built in SOLIDWORKS and imported to COMSOL through the interface for the evaluation of each individual heat sink. As a design target, the power density for this solar inverter is constrained under 100W/in³ and the design goal is to minimize the maximum junction temperature of the semiconductor devices.

The heat sinks are designed for each switch (MOSFET and diode) and are packaged in a phase leg as shown in Fig. 5-4 in COMSOL. Based on the space constraint, the available volume of the heat sink is 36mm×57mm×27mm, so that the power density of the inverter will not exceed the design constraint.

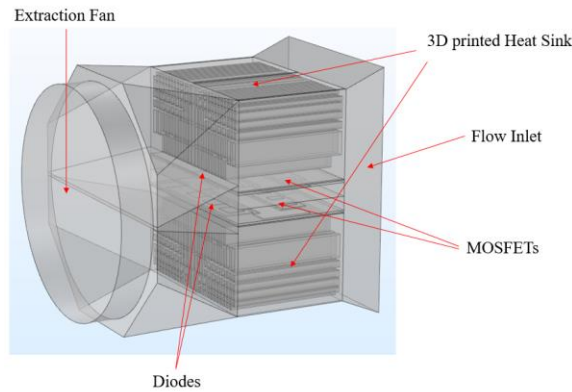


Fig. 5-4. Phase leg module geometry in COMSOL

Instead of using the fixed flow rate, flow input to this module is calculated based on the selected fan curve and the pressure drop of the module, as is shown in Fig. 5-5. The gray curve is obtained from the datasheet of the fan and the blue curve is the pressure drop curve of the designed heat sink. In this way, the pressure drop penalty has already been considered as a design fact.

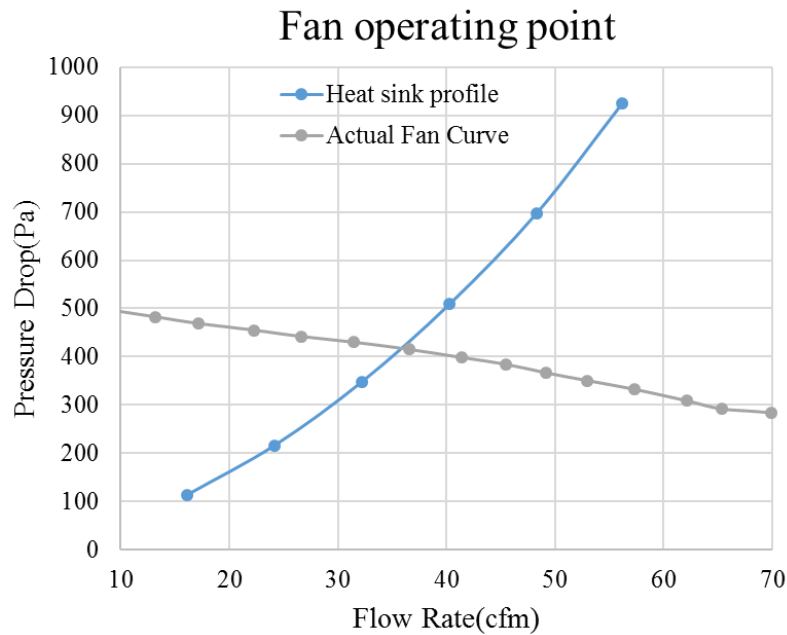


Fig. 5-5. The flow rate of the power module

The flow rate of the operating point is determined based on the crossing point of curves. Since the flow rate and junction temperature are directly related, the pressure drop of the designed heat sink is not separately optimized. Instead, only the maximum junction temperature is considered.

5.3. CELL MODEL

In this section, the optimization focus switches to the 2D optimization of the cross-section pattern. In order to provide enough design freedom, a method named as “meshed cell distribution” is proposed. The heat sink is divided into cell meshes and design the pattern of each cell individually. A heat sink with the same volume as previous cases is studied. For the design case-study, the available design area in the is $57\text{mm} \times 27\text{mm}$. The design area is divided into a 4×9 array of cells as shown in Fig. 5-6 where the size of each cell is $7\text{mm} \times 7\text{mm}$.

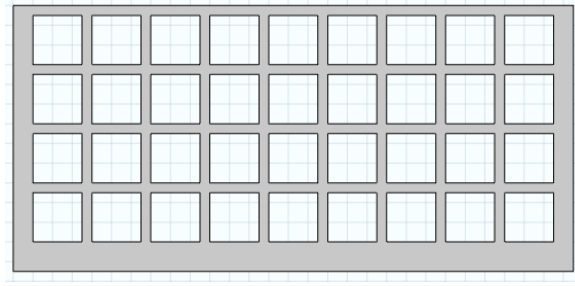


Fig. 5-6. The empty meshed template of the heat sink cross-section

As shown in Fig. 5-7, nine possible types of cell patterns are considered in this version, numbered as 1-9. One of these patterns will fill each of the empty cells in Fig. 5-6.

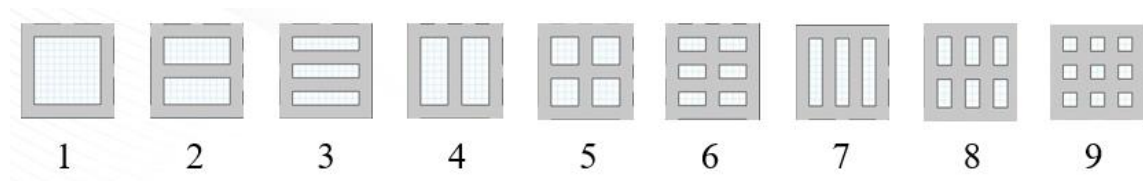


Fig. 5-7. Types of cell patterns

5.3.1. Initialization of cells

The individual cells of the heat sink in Fig 4-11 are initialized with a number indicating the cell pattern chosen. The 4×9 matrix of numbers is treated as a “cell distribution chromosome” in the GA. A solution space size around 10^{33} is created with this chromosome. A secondary smaller 3×9 matrix, named “wall-layout chromosome”, is created to determine the existence of the connected walls between any two vertically adjacent cells. Each entry in the matrix is 0 or 1, with 0 representing the absence of wall and 1 representing the converse case. The presence of a wall indicates the separation of 2 adjacent cells, as shown in Fig. 5-8.

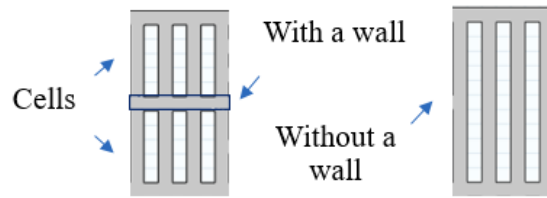


Fig. 5-8. Illustration of the wall-layout definition

The inclusion of the additional chromosome can generate greater variety with a larger solution space size around 10^{42} . The combination of two chromosomes forms the DNA of one individual. Each DNA in the population represents one heat sink cross-section geometry. A one-to-one mapping from DNAs to heat sink patterns is constructed based on this proposed method.

One design example of the heat sink patterns is presented in Fig. 5-9 for illustration. Based on a symmetrical design assumption, a cell distribution chromosome shown in Table 5-2 is generated. Two highlighted cells numbered 9 and 5 are in the blue box.

After applying the first chromosome to the empty meshed template of Fig. 5-6. The empty meshed template of the heat sink cross-section, the pattern of the heat sink with the highlighted cells is shown in Fig. 5-9(a).

Another wall-layout chromosome is applied to the pattern as shown in Table 5-3. The wall between the highlighted cells is marked in the matrix.

The final design of the cross-section pattern is shown in Fig. 5-9 b). The wall is broken down into the highlighted cells.

Based on the designed cross-section pattern, the heat sink block is created by extending the pattern to the third dimension, as shown by the red arrow in Fig. 5-10.

By assembling the heat sinks with the imported parts from SOLIDWORKS, the phase leg geometry, as shown in Fig. 5-4, is constructed in COMSOL.

This approach creates the initial population for the GA.

Table 5-2. Cell distribution chromosome

8	6	9	9	4
9	1	9	5	9
2	3	2	8	8
9	5	9	2	9

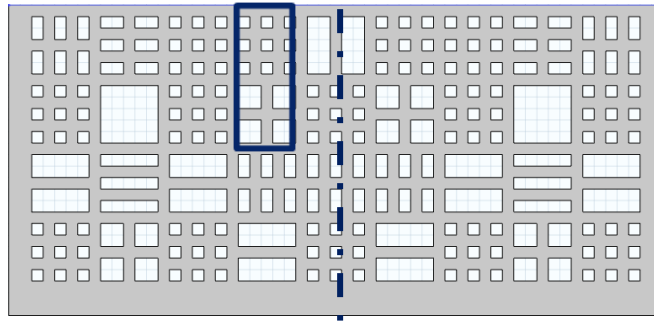


Fig. 5-9(a). The first step of the pattern design

Table 5-3. Wall-layout chromosome

0	1	0	0	0
0	1	1	1	0
0	0	1	1	0

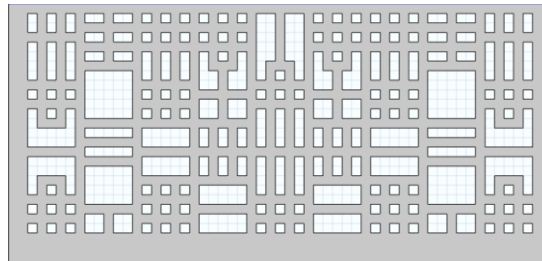


Fig. 5-9(b). The final design of the heat sink cross-section pattern

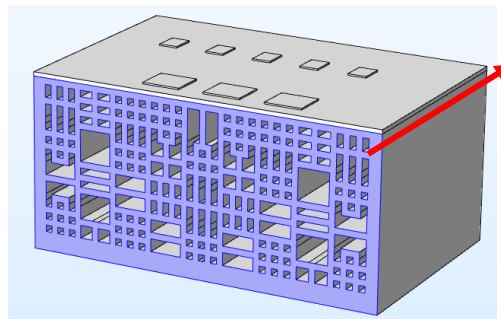


Fig. 5-10. The random created an air-cooled heat sink in COMSOL

5.3.2.Evaluation of cells

The temperature profile of each individual in the population is evaluated based on FEA simulation using COMSOL. A coupled FEA stationary solver including heat transfer and flow dynamic is used. Settings of the model are described as follows:

The material for each domain is set by the default properties built in COMSOL, except the thermal conductivity of the 3D printed Aluminum which is introduced in Chapter II.

The physics parameters then are set, according to the datasheet and the circuit simulation results of the converter. The initial temperature, ambient temperature, and the inlet air temperature are all set to be 28.2 °C. As estimated, the 290W loss is generated per phase leg. That is 27W loss for each MOSFET and 3.5W for each diode. Thermal interface material is applied between the DBC and the heat sink, with a thermal conductivity of 0.8 W/mK and a thickness of 100 µm. The outlet of the extraction fan is assigned based on the flow rate vs. pressure curve shown in Fig. 4-3 and the inlet are set to be free flow. The type of flow, either laminar or turbulence is determined based on the flow dynamic theory. Since the Reynolds number of the system is calculated to be larger than 2000, it is reasonable to use the weakly compressible turbulence flow physics module in COMSOL.

After the physics setting, finite element mesh grids are built. To save the computation time, custom meshes are generated to achieve a higher computation speed without sacrificing the simulation accuracy, as shown in Fig. 5-11. The number of custom mesh elements is around five to ten times smaller than the default.

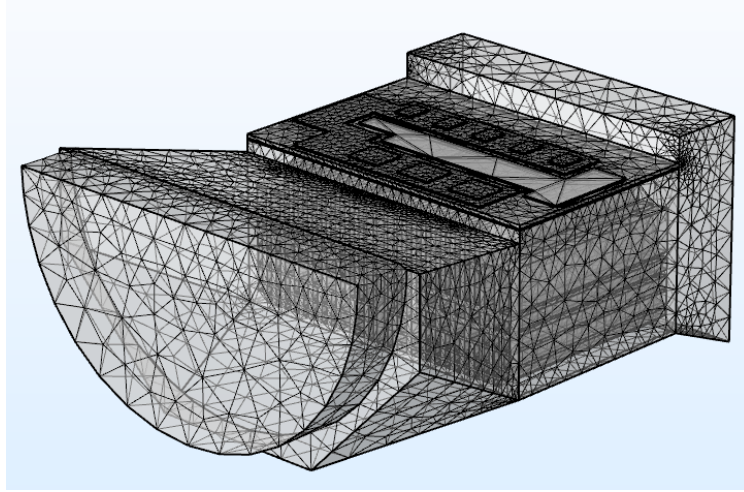


Fig. 5-11. Half of the geometry with an automatic custom mesh grid

The computation time for each individual varies from 2 to 10 minutes, simulated by the workstation with six-core, 3.5GHz Xeon processor and 40GB memory. Based on the temperature profile of the simulated result, the maximum junction temperature is reported back to the algorithm in MATLAB.

Evaluation in this section builds up an evaluation function $T=E(X)$ where X is the DNA (heat sink solution) of each individual and the output, T is the maximum junction temperature. For a population of 21 individuals, a list of 21 T s is Obtained. The fitness value is evaluated based on

$$f(i) = 1 / \left(\frac{\alpha T}{T_{limit}} + \frac{(1 - \alpha)R(i)}{21} \right) \quad \text{Eq. 5-7}$$

The fitness value is assigned to each individual correspondingly.

5.3.3. Selection of cells

Selection for this application uses a similar roulette wheel as previously introduced. Survival possibility of each individual is assigned as

$$s(i) = \frac{f(i)}{\sum_{j=1}^N f(j)} \quad \text{Eq. 5-8}$$

16 survivors of the population are picked to enter the mating pool based on their share of the roulette wheel and five lowest scorers are eliminated.

5.3.4. Crossover and mutation of cells

The 16 survivors in the mating pool are divided into eight couples. Each couple goes through crossover and produces two individuals to replace them in the next generation. Based on a pre-defined probability, the crossover can happen by randomly selecting and exchanging the values at each matrix position between the couples. If the crossover does not happen, the parents will remain and become the candidates in the next generation directly. Mutations may also occur during the crossover by changing an entry in the matrix representing the cell distribution DNA or the wall-layout DNA. As an adaptive algorithm, the probability of mutation is a function of the rate of convergence. A higher probability enables the algorithm to reach a global optimized point, while a lower probability can increase the rate of convergence.

5.3.5. Recombination of cells

Besides the 16 offspring from the previous generation, five more individuals are selected. Elitism operator is proposed here to make sure the best individual of the previous

generation will always survive and be identically copied into the next generation. Additional four newly generated individuals are introduced. This is a migration operator to prevent the premature convergence of the system. The new population to be used in the next iteration of the GA will consist of the 16 new-born heat sink candidates that inherit genetic information from the parents' generation, four newly generated heat sink candidates, and one of the best heat sink candidates of the previous generation.

5.3.6. Second-stage perturbation of cells

After convergence of the genetic algorithm, heat sink candidates with the high fitness scores are picked as the optimization objects for the second stage. Cells in each heat sink are randomly selected and changed. The thickness of the wall and the position are modified as well to improve the fitness scores. After each iteration of the second-stage optimization, the heat sink candidates with the lowest fitness scores are replaced with the better ones and the process is repeated until the best result is obtained.

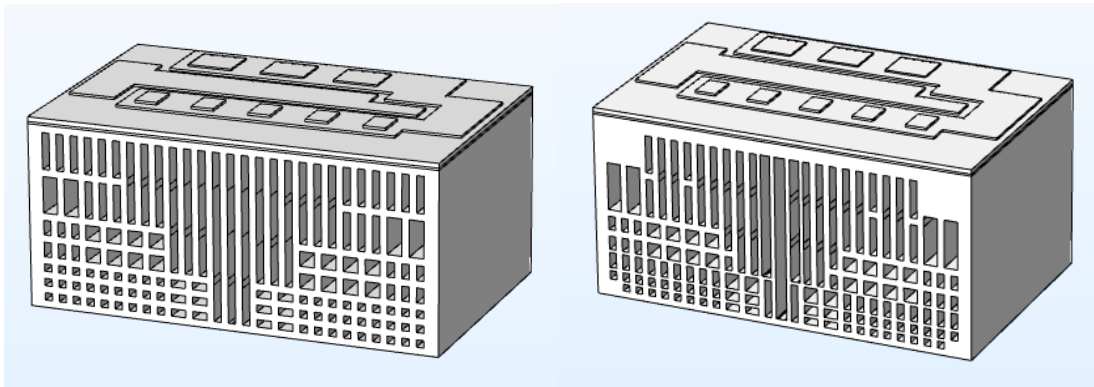


Fig. 5-12. Stages optimization

5.3.7.Optimization results of cells

After a computation time of in total 135 hours, the simulation results converge to the heat sink shown in Fig. 5-12(a), with a maximum junction temperature of 106.29 °C. Based on the results of the first stage, the second-stage optimized heat sink is developed. As shown in Fig. 5-12(b), the thickness of walls in the center decreases and other small modifications have implemented. As a result, a lower maximum junction temperature of 104.02 °C is achieved.

Referring to the method described in Fig. 5-1, the flow rate of the fan is estimated at 42 cfm at the cross point. The temperature profile of each device is tested according to the horizontal cut plane in Fig. 5-13. The maximum junction temperature of the bare semiconductor die is 104.2 °C, and the temperature variation among the MOSFETs is about 10%.

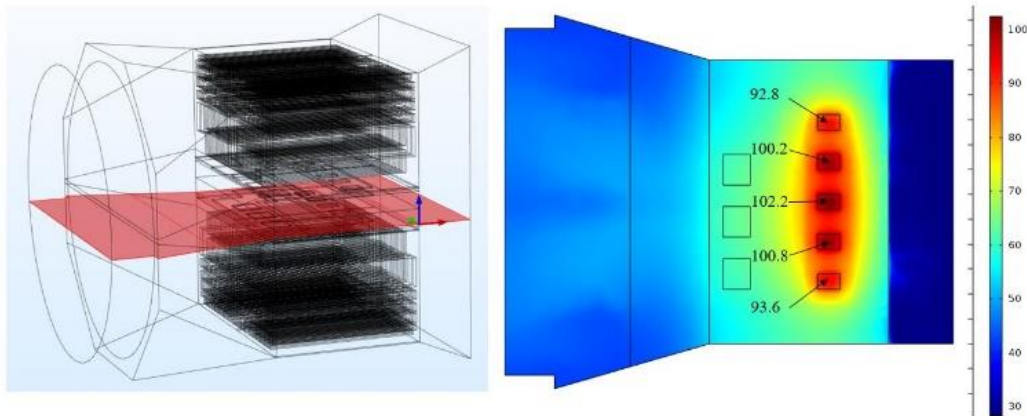


Fig. 5-13. Thermal profile plots of horizontal cut plane

5.4. COMPARISON OF CELLS

Benefits brought by the machine learning based algorithm optimization can be illustrated by comparisons to the commercially designed heat sink. A customized plain-fin heat sink based on conventional manufacture technique has been manually designed by heat sink supplier, as shown in Fig. 5-14. Dimensions of the fin-structure heat sink are: 60.5mm×36mm×32mm.

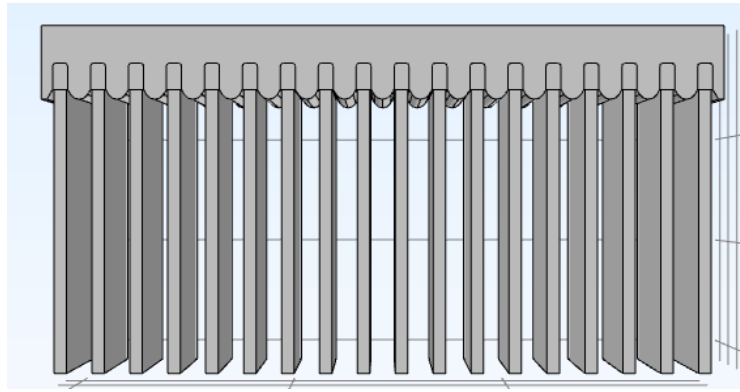


Fig. 5-14. Customized fin structure heat sink with conventional manufacture technique

The design is based on the same optimization parameters and demands as this design case study. A slight larger heat sink is designed by the supplier as the total volume of the conventionally designed heat sink is 60.5mm×36mm×32mm, which equals to 69696 mm³. For comparison, the 3D printed heat sink with the dimensions, 57mm×36mm×27mm, has a volume of 55404 mm³. In terms of power density, more than 15% improvement has been achieved by the machine learning based algorithm for the optimization of 3D printed heat sinks.

Rest of model is built in the COMSOL identically, except the different approaches of heat sinks of two modules. Flow profiles are obtained based on the simulation results. Due to the loose fin spacing and a lower pressure drop of 346 Pa, the conventionally designed heat sink has a higher flow rate of 64 cfm than the 38 cfm flow rate of 3D printed heat sink with a higher pressure drop of 437 Pa. The operating points of two heat sink models are shown in Fig. 5-15.

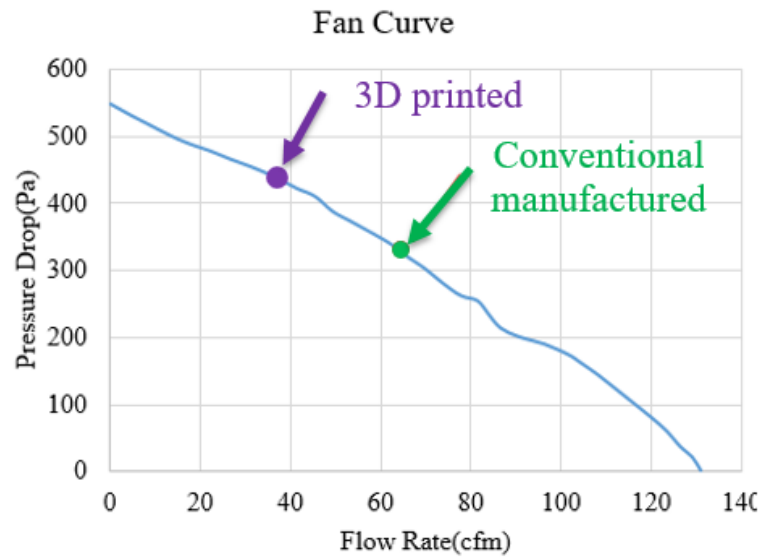
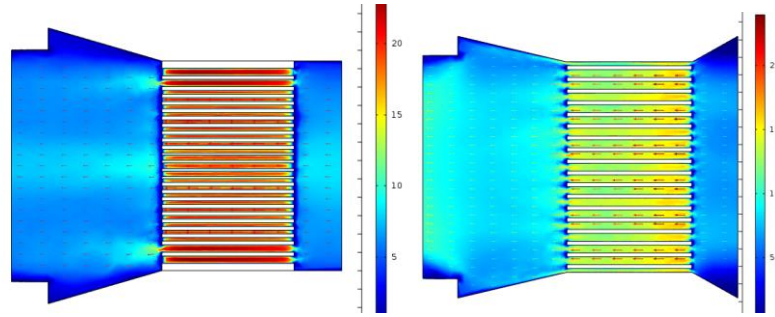


Fig. 5-15. Operating points on the fan curve

Even though the overall flow rate is lower as the machine learning based optimized heat sink, the flow velocity in the nearby region of the heat sources is higher compared to the manually designed heat sink, as shown in Fig. 5-16. The optimized flow distribution with the large contact surface near the heat source region leads to a huge heat transfer rate while the further part of the heat sink is designed with lower heat transfer capability.



3D printed heat sink

Conventionally manufactured heat sink

Fig. 5-16. Flow distribution right below the devices (m/s)

As a result, the 3D printed heat sink achieved a better performance by focusing the flow near to heat sources to maximize the ability of heat convection of the system. About 10% of the thermal resistance reduction can be achieved. As shown in Fig. 5-17, compared to the conventionally designed heat sink with the maximum devices' junction temperature of 108.3 °C, the performance of the 3D printed heat sink is 102 °C.

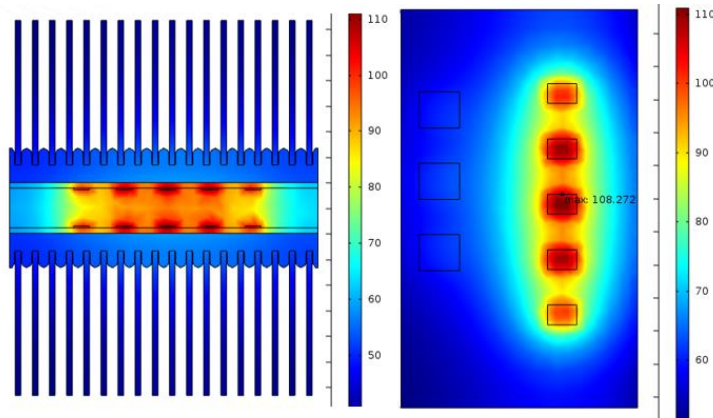


Fig. 5-17(a). Temperature profiles of the conventional heat sink model

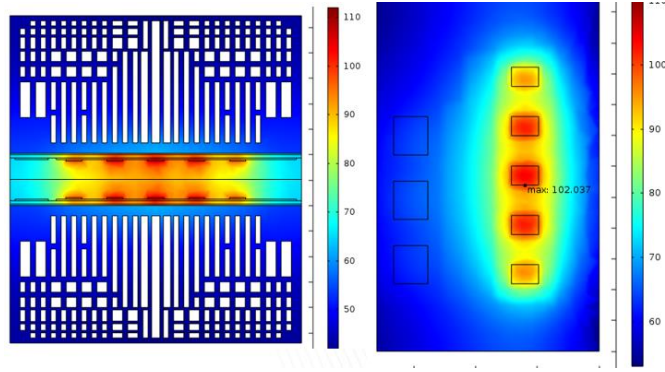


Fig. 5-17(b). Temperature profiles of the 3D printed heat sink model

Table 5-4. Parameters of thermal equivalent circuit comparison

Label	Description	Value of Printed HS	Value of Conventional HS
P_in	Total input power of power devices	290W	290W
R_th_j-b	Junction to DBC surface	0.0226 °C/W	0.0215 °C/W
R_th_b-h	DBC surface to HS surface	0.125 °C/W	0.134 °C/W
R_th_h-t	HS surface to Tip	0.0637 °C/W	0.0703 °C/W
R_th_t-a	Tip to Ambient	0.0386 °C/W	0.0403 °C/W
T_Ambient	Ambient temperature	28.2 °C	28.2 °C

As the TEC structure of Fig. 2-4, the parameters of each component are listed in Table 5-4.

The thermal resistance in the blue dashed box represents the performance of the heat sinks. About 10% of the improvement can be found based on the comparison.

5.5. EXPERIMENTAL VALIDATION

To validate the accuracy of the simulation model, a phase-leg module consisting of two switch packages, outside package for stress relief, mechanical support and air duct is designed and 3D printed correspondingly, as shown in Fig. 5-18.

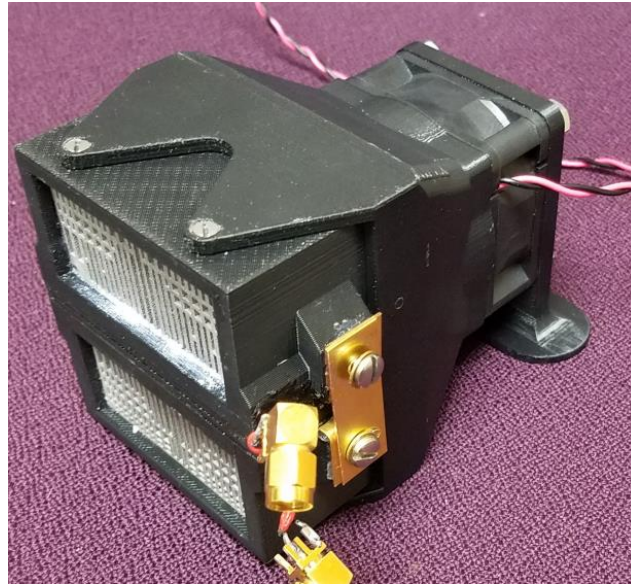


Fig. 5-18. Phase leg module of air-cooled phase leg

The 3D printed heat sink inside the phase leg module is compared to a penny, as shown in Fig. 5-19. The overall volume of this 3D printed part is 36mm × 57mm × 27mm.

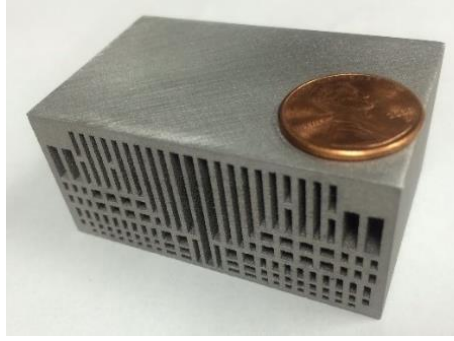


Fig. 5-19. 3D printed Aluminum air-cooled heat sink

Half of the phase-leg module, the package of one switch position is shown in Fig. 5-20. DBC is mounted on the ground surface of the heat sink with a thermal grease layer placed in between. DC buses, wire-bonds, gate signal and other connections are assembled.

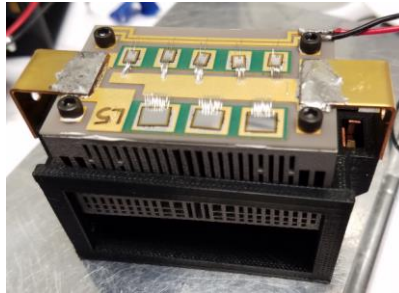


Fig. 5-20. 3D printed package of one switch position

Flow profile comparison is the first step of the validation. The flow profile is measured at different locations in the outlet channel of the module, marked as Top 1-5 and Bottom 1-5, for both simulation results and the experimental results. As shown in Fig. 5-21, the average output flow velocity for each location is obtained in COMSOL and compared with test data, as shown in Fig. 5-22.

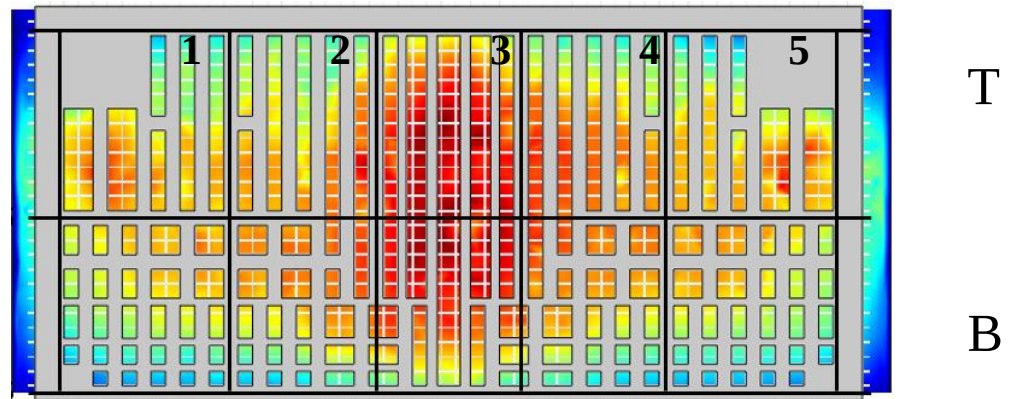


Fig. 5-21. Simulated air flow profile

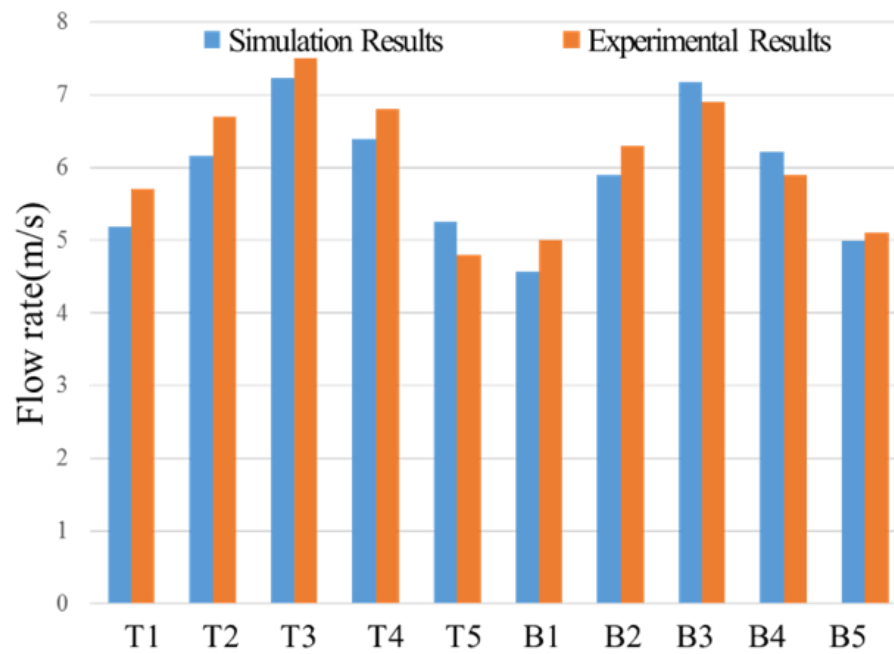


Fig. 5-22. Flow profile comparison

Negligible differences are observed between to group of data. It is reasonable to claim that the FEA simulation of the flow dynamic property matches well to the experimental test data. And the accuracy in terms of the flow distribution is valid. The average outlet flow velocity is 5.2 m/s.

Due to the lack of approach to measure the accurate junction temperature of the devices, the heat transfer simulation is valid based on the energy balance equation, as shown in the

$$\int \rho \cdot A \cdot v \cdot Cp \cdot \Delta T \cdot dt = \int P \cdot dt \quad \text{Eq. 5-9}$$

Where ρ is the density of the flow; A is the cross-section area of the flow channel; v is the average velocity of the flow; Cp is the heat capacity of the flow; ΔT is the average temperature rise between the inlet and outlet and P is the total power dissipation from devices. This equation indicates the second law of thermodynamics. All parameters in this equation are related to the air flow profile except for the temperature rise ΔT . The calculated average temperature rise of the outlet flow is 12.5 °C. The experimental measurement shows an inlet temperature of 27.5 °C, and an outlet temperature of 39.4 °C on average. The temperature rise measured in the experiment is 11.9 °C. Even with small difference in the results caused by the low quality of the mesh elements, this comparison validates the accuracy of using simulation result to estimate the real junction temperature of the devices. Based on the results, the actual junction temperature of the module then can be estimated based on the simulation results to be around 100 °C. That is far below the maximum allowed operation temperature.

In summary, comparisons between the conventionally manufactured heat sink designed with the fin-structure and the 3D printed heat sink optimized by Genetic Algorithm are presented in this section. The validation of the accuracy of the simulation model has been

studied as well. An overall 15% in terms of power density and 10% in terms of thermal resistance improvements can be achieved.

However, not a significant improvement can be achieved due to the poor material property of the heat transfer media, air and the high sensitivity to pressure drop. And those facts limit both performance and the design freedom the air-cooled heat sinks. In order to further improve performance, liquid-cooled solutions are considered.

5.6. SWITCH TO LIQUID-COOLED SOLUTIONS

To further improve the cooling system performance, liquid-cooled becomes a more reliable solution. Due to its better heat transfer media, taking water as an example, the thermal conductivity, 0.65 W/(m K) is 23 times larger than that of air, 0.0285 W/(m K) . Like the forced-air cooled case, pump needs to be involved in the cooling system for moving the heat transfer media and dissipating heat from devices to the heat exchanger. The more powerful pump used in the system enables a much higher pressure drop capability compared to air-cooled fan application. This tolerance of high-pressure drop allows the design of a more complex structure that can more efficiently deliver the coolant media to the target locations and get better performance. Generally, the performances (heat transfer coefficient, h) of liquid-cooled strategies range from 100 to $2 \times 10^4 \text{ W/(m}^2 \text{ K)}$. Liquid-cooled applications are commonly used in high power applications, such as the power-train of electrical vehicles and motor drive system.

In this chapter, several genetic algorithms-based design methodologies of the liquid-cooled heat sink are introduced. A design case using the most advanced method is evaluated and compared to the commercially available product.

5.7. TOPOLOGY OPTIMIZATION, BINARY MODEL

The initial design approach of the liquid-cooled heat sink is proposed with the similar concept of the cell model heat sink. By dividing the design space into mesh, the design chromosomes assign the meshed elements to either metal or liquid domain, where zero represents liquid and one is the metal domain. This method got the idea from a general mathematical optimization method, called “Topology optimization”. Since the composition of the chromosomes is only zeroes and ones, it is also named as “Binary Model”.

5.7.1.Initialization of binary model

Binary model is subject to fundamental constraints:

- The heat sink is designed two-dimensionally symmetric to save computation time.
- The heat sink is a block with a given volume. The liquid is restricted inside the body.
- A clear liquid path connecting inlet and outlet is guaranteed, otherwise, the design is void.
- Locations of Inlet and outlet are predefined at two opposite ends of the heat sink.
- Mechanical constraints, that the thickness of the boundary is defined.
- The power module is attached to the top surface of the heat sink.
- The module used in optimization is simplified as a uniform plate heat source.

Additionally, the design parameters and constraints are given:

- The material of the printed heat sink is Additive Manufactured Aluminum.

- Total Aluminum block volume of the heat sink is 42mm×28mm×10mm.
- The thickness of the side walls is 2mm.
- The design area of the liquid channels is 38mm×24mm in a 2D coordinate.
- Minimum element size is 2mm×2mm square pixel. And the design area is reduced to 19×6 pixels, which in total, a matrix of 114 elements.

A randomly initialized individual satisfied constraints above is shown in Fig. 5-23. A zero-one matrix represents the design chromosome and the red and gray colored cross-section is the actual liquid channel.

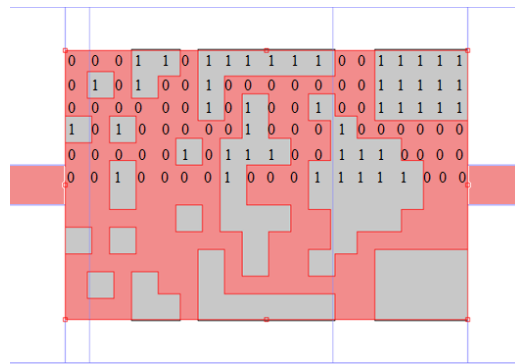


Fig. 5-23. Matrix present of the 2D channel pattern

3D heat sink model used in FEA simulation is extruded in the perpendicular direction from the 2D channel pattern, plus the upper and lower covers of the channels and a heat source as shown in orange color. For each individual initialized, it is evaluated in COMSOL through the developed interface under a sequence of the instructions. The maximum temperature of the heat source is recorded as the fitness score. The optimization target is to find the best chromosome matrix that has the lowest junction temperature.

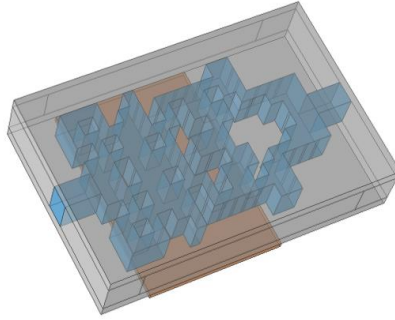


Fig. 5-24. 3D extruded FEA simulation model in COMSOL

5.7.2. Crossover and mutation of binary model

After initialization and evaluation steps, a group of individuals is selected into the mating pool. Crossover takes over in this step. The detailed method is illustrated based on a pair of individuals in the mating pool:

Step 1: A random location, named waist is picked in both of the individuals, for example, the 10th row inside the black boxes. Each individual, as well as its matrix, is divided into three domains, namely, head, waist, and tail.

Step 2: Exchange domain component, the tails with each other, keep the heads the same and leave the waist blank.

Step 3: New waist connecting head and tail is created based on the given head and tail of the new individual, as shown in Fig. 5-27. New waists are created to meet all constraints:

- The waist has to ensure that the connection constraint is always satisfied.
- Not be too many zeroes (liquid pixels) exist in the waist.
- Avoid the useless liquid pixel that connects to nowhere.
- Mutation by converting one to zero is expected for a small possibility.

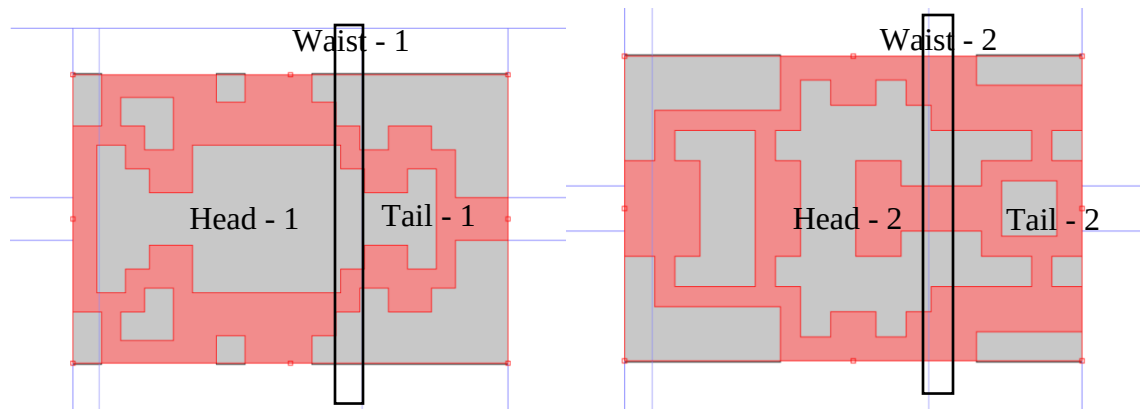


Fig. 5-25. Step 1 - A couple of parents in the mating pool

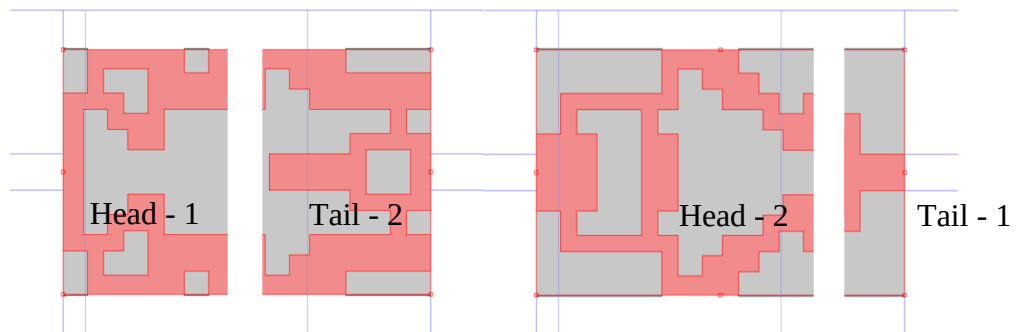


Fig. 5-26. Step 2 - Pattern split

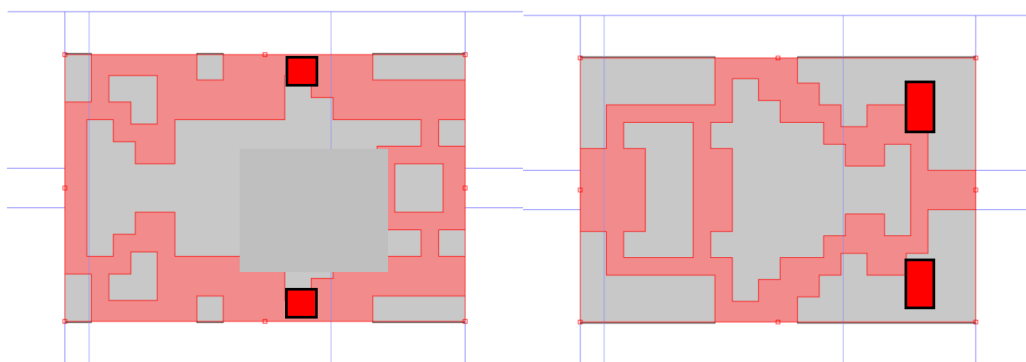


Fig. 5-27. Step 3 - Waist creation

Following the steps, the expected offspring are expected to be the new geometries with Individual 1's head + suitable waist + Individual 2' tail and Individual 2's head + suitable waist + Individual 1' tail. Those sequence instructions are the crossover and mutation method used in this Binary Model.

5.7.3.Results of binary model

A quick design case has been tested with a convergence after 40 iterations. The convergence so fast that the designed performance is not as excellent as expected. It is also limited by the small solution space and few possible solutions exist. To further improve the design, higher pixel numbers for a larger solution space is needed. However, one of the biggest challenges for applying Binary Method during enlarging the pixels' scale is to ensure the continuous feature of the individual. This challenge increases exponentially with the matrix dimension increase. A more powerful initialization method, first of all, ensuring the continuous channels is proposed in the next section, named random walking process.

5.8. RANDOM WALKING PROCESS

5.8.1.Design concept - Initial a river

Inspired by the natural growth process of a river, the Markov process of probability theory is introduced to initialize the liquid channels. Compared to the Binary Model, this process ensures the connection in the first place. Similar to a river, inlet/upstream is always connected to the outlet/downstream, no matter how wavy it may look like. As a mathematical model approximation, the wavy river is simplified into connected line segments. The initialization process of a river can be then treated as a Markov process.

That is, from given inlet, the first segment of the river flows towards a random direction with a random distance. A second segment starts from the end of the first segment and repeats the same process. Under an overall bias to downstream, the river from upstream will eventually approach to the outlet. Meanwhile, not only one path but several bypass channels can exist in parallel, forming a river with multiple branches.

To imitate the initialization of a river in the heat sink design, a sequence of steps is introduced. Each step is a line segment with directions and length and added to the previous pattern. A bias from upstream to downstream is also included as a function of the initialization stage. At the early stage of initialization, the direction and distance of the steps are absolute random under the boundary constraint. While the bias becoming stronger, the trend towards outlet built up. Eventually, the channel approaches to its outlet and a continuous channel are formed. The set of the line segments contributing to the channel is stored as a matrix, called chromosome in GA. Boundary constraints of the process are listed:

- The last line segment must end at the outlet location.
- Only four perpendicular directions are allowed during the walking process.
- Only integer distance of the walk distance is allowed.
- The channels have to stay within the design area.

For a channel branch with n segments, the corresponding chromosome matrix has a dimension of $(n+1) \times 2$. As a constraint, the chromosome should have such features:

- The first row of the matrix is the inlet coordinate and the last row is the outlet coordinate.
- Two continued rows have and only have one identical number.

- The matrix contains only integer numbers.

For a better design, additional rules are considered:

- The bias direction varies with steps:

This bias avoids either too simple or too complex individual design. Briefly speaking, the channel is more willing to explore the whole area rather than reaching the end point at the beginning period. However, the trend of approaching the exit area builds up after enough steps to end the walking process. This strategy is implemented by changing the possibility of the directions, which is called bias.

- Avoid dead ends while walking.

Dead end refers to the channel without other outlets except for its own reverse channel. It is useless and could even cause a fluid trap. To avoid this feature, the possibility of going reverse direction is zero for any channel.

- Converge channels are constructed near the outlet area

When approaching the outlet, there are preset instructions steps that converge the channels to the given outlet location. The definition of approach is a possibility-based function of the distance to the outlet. The closer one end stopped to the outlet, the larger chance the system can regard it as an approach.

- Channels can cross with each other

If two channels are crossed, the cross point is regarded as connected. With this definition, multi-branches channels can be created as what should be seen as a river.

- Overlapped channels double the shared channel width

If part of any two different channels overlaps, the overlapped channel doubles its width.

Above are general rules of the chromosome. Repeat this walking process for m times, where m is the number of channels, a heat sink with m channel branches is initialed and recorded as matrix chromosome.

A study case is illustrated in the following sections as an example.

5.8.2.Case illustration

A study case is created based on a three-phase inverter with the liquid-cooled system. A 100kW three phase Silicon IGBT based inverter is built in this case as the heat source of heat sinks. The efficient is inverter is estimated at 97%, where the 1kW loss is assigned to each phase-leg phase power module. Three commercially available phase-leg IGBT power modules PRX CM200DY-12NF are placed in the layout orientation as Fig. 5-28. With the identical heat source profiles, comparisons are made based on both numerical FEA simulations and experimental tests.

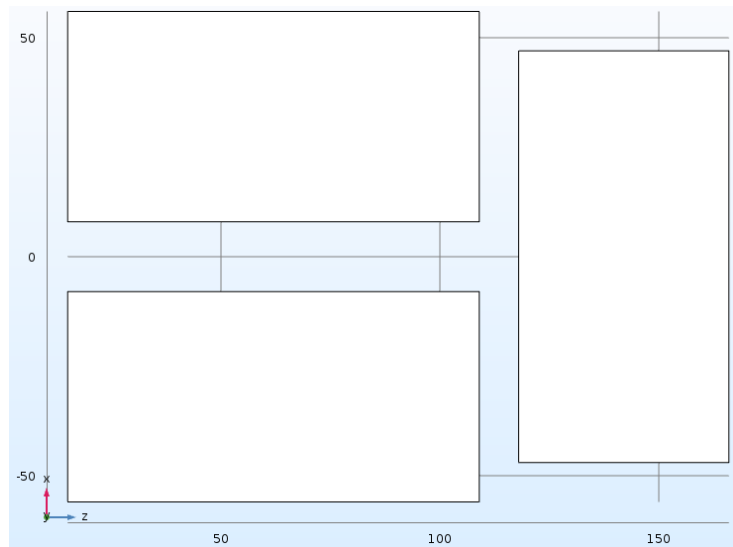


Fig. 5-28. Three-phase inverter power module layout

Comparisons include three candidates, 3D printed heat sinks of conventional designed Formed Tube Cold Plate (FTCP), GA based design heat sink without and with annealing post-process are evaluated in terms of the base temperatures. Thermal interface material (TIM) is placed between the power module and the heat sink in COMSOL to imitate the real experimental case. TIM uses a soft graphene material Tgon with a thermal conductivity of 5 W/mK. This material can limit the impact of the contact thermal resistance and focus more on the heat sink performance. The thickness of the TIM is modeled as 300 μm . Liquid inlet boundary conditional is modeled using a pump with the flow-pressure property shown in Fig. 5-29.

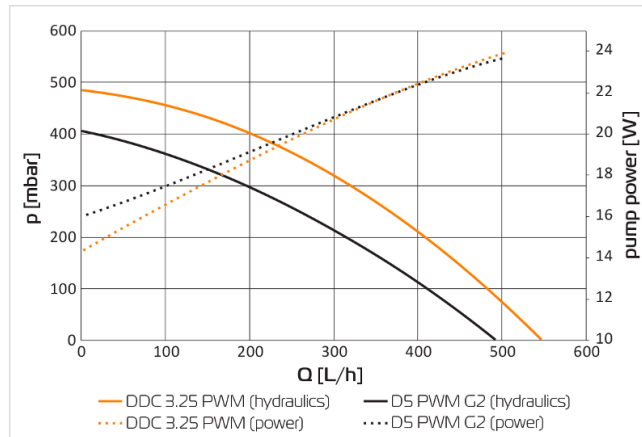


Fig. 5-29. Profile of the liquid pump

This boundary condition enables the flow rate adjusted based on the pressure drop of the designed heat sink. The flow rate of the operating point is then determined at the crossing point of the pump profile curve and the pressure drop curve of the heat sink. Dealing with a multiple-objective optimization problem will take a longer optimizing time. To

reduce the number of optimization objective, the impact of pressure drop is eliminated by this pump boundary condition. The flow rate and junction temperature are directly related, so the pressure drop of the designed heat sink will not be optimized separately. Instead, only the maximum junction temperature is considered, and this multiple-objective challenge is converted to be single-objective optimization problem. The temperature of the inlet fluid is the room temperature at 20 °C. The Reynolds number of the system is evaluated by

$$Re = V \cdot D / \nu \quad \text{Eq. 5-10}$$

Where V is the inlet velocity, D is the characteristic length and ν is the kinematic viscosity of the fluid material. As estimate and test run, the Re is much smaller than 1000, and the type of fluid can be set as Laminar flow. Since this problem focuses only on the junction temperature, the fitness score is determined solely by the maxima junction temperature of the power modules.

5.8.3. Conventionally designed heat sink

The conventionally designed heat sink is modeled based on the commercially available heat sink CP15G05 TUBED COLD PLATE. A liquid channel embedded Aluminum block with dimensions (Length×Width×Height), 164mm×134mm×16mm is constructed as the comparison baseline, as shown in Fig. 5-30, three predesigned layout modules are placed on top of the heat sink.

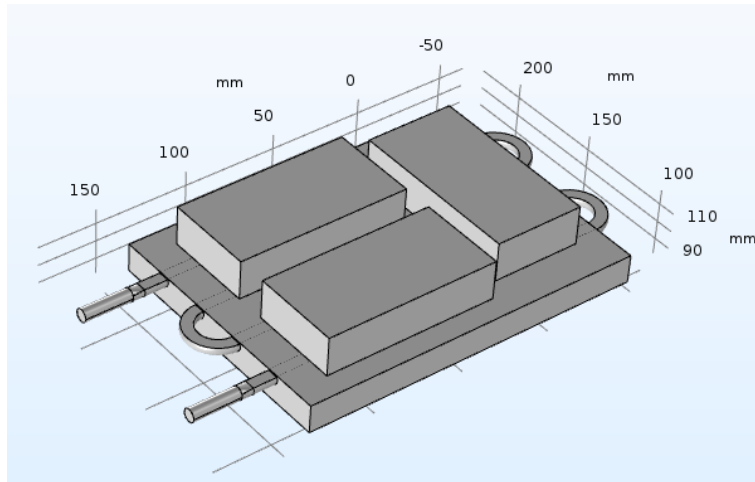


Fig. 5-30. Model of the three-phase inverter with conventionally designed heat sink

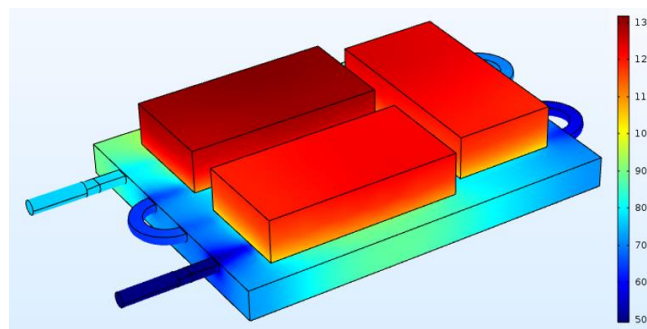


Fig. 5-31. (b) The temperature profile of the conventionally designed heat sink

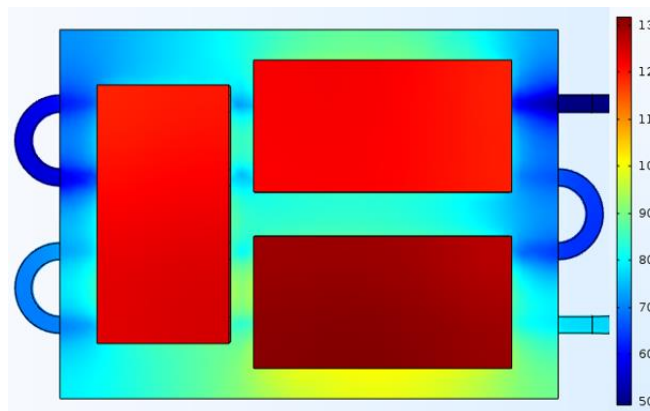


Fig. 5-31. (b) The temperature profile of the conventionally designed heat sink

FEA simulation of the conventionally designed heat sink is straightforward with the boundary conditions introduced previously. A normal size mesh is mapped to the model with additional boundary layer mesh along the convective surface. The temperature profile of the evaluated heat sink is shown in Fig. 5-31.

This FEA result is recorded as the baseline and Genetic Algorithm based geometry optimization result will compare to this baseline.

5.8.4. Genetic Algorithm based optimization initialization

In this section, the detailed procedures of initializing random individual are explained. The heat sink body block has the same overall dimensions as shown in Fig. 5-32. Inlet and outlet locations, in this case, are located at the opposite sides. Identical three phase-leg modules and TIM are included in the model. The optimization target is to find out the best liquid channels distribution to achieve the highest fitness score.

Resolution of this design is limited by 3D printed state of art precision. The minimum channel width and the minimum thickness of the wall are set to 2 mm. The design is similar to the previous method which 2D cross-section pattern is designed and extruded in the third direction used as the heat sink in COMSOL.

The available fluid area is 160mm×120mm. If to consider the potential locations of any connection points of segments, that equivalent to a pin net with 80×60 pixels. Because of the symmetrical power modules layout, symmetrical design assumption can further reduce the net size to 80×30 pixels, as shown in Fig. 5-33. Additional modifications to reduce the computation time, such as connect channels and power modules are also included that present the design, as shown in Fig. 5-34.

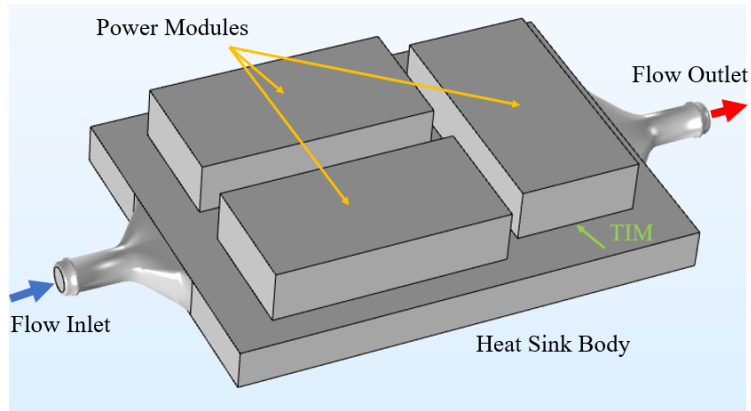


Fig. 5-32. Heat sink body block to be optimized.

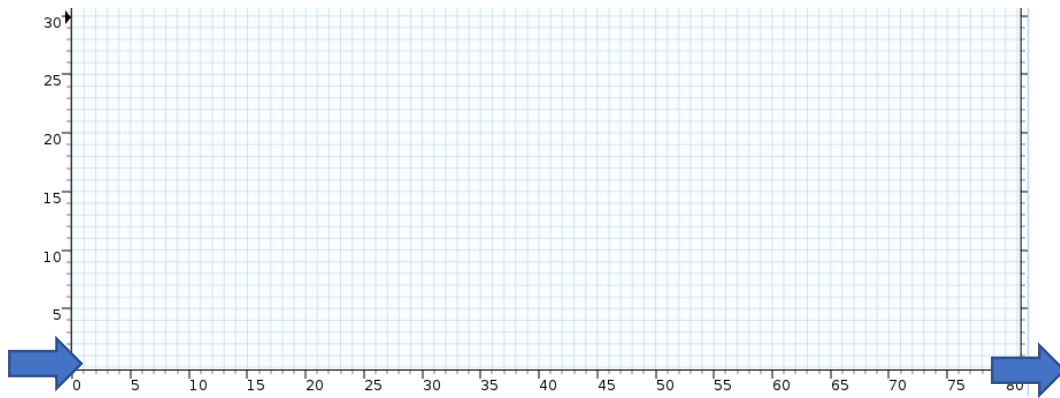


Fig. 5-33. Design space of liquid channels

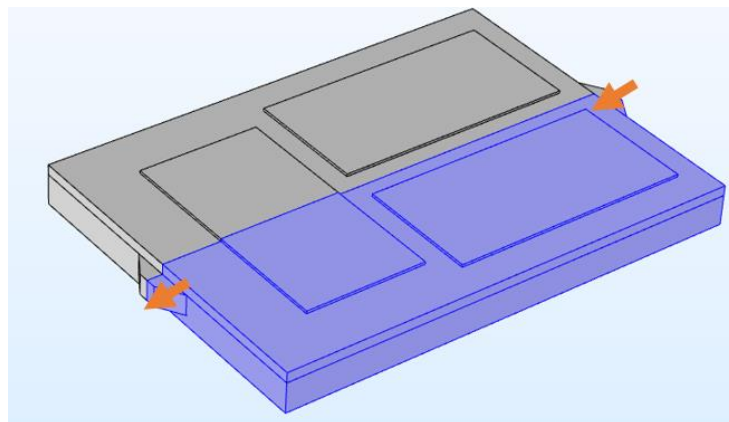


Fig. 5-34. The symmetrical layout of the power modules

5.8.5.Design procedures - Initialization

Within the design area shown in Fig. 5-36, the chromosome first channel branch starts from inlet coordinate, red dot at (1,1), following the instruction of the first line segment of the chromosome shown in Fig. 5-35, and ends at the blue dot at (22,1).

Then the blue endpoint (22,1) becomes red start point, the second segment is built upwards with a step length of 19, and ends at (22,20) as shown in Fig. 5-37.

Repeating the segment construction following the matrix instruction, the channel continues to explore until reaching the end 13th segment, (75,23) where landed inside the exit area in yellow and triggered the exit procedure, as shown in Fig. 5-38. Additional exit channel brings the liquid to the given outlet location, (89,1).

	1	2
1	1	1
2	22	1
3	22	20
4	3	20
5	3	7
6	1	7
7	1	17
8	26	17
9	26	13
10	9	13
11	9	20
12	72	20
13	72	23
14	75	23
15	75	6
16	76	6
17	76	1
18	89	1

Fig. 5-35. The chromosome of a channel branch

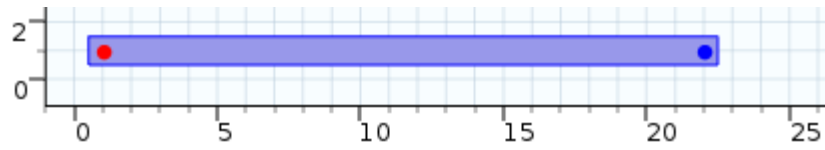


Fig. 5-36. The first segment of the channel

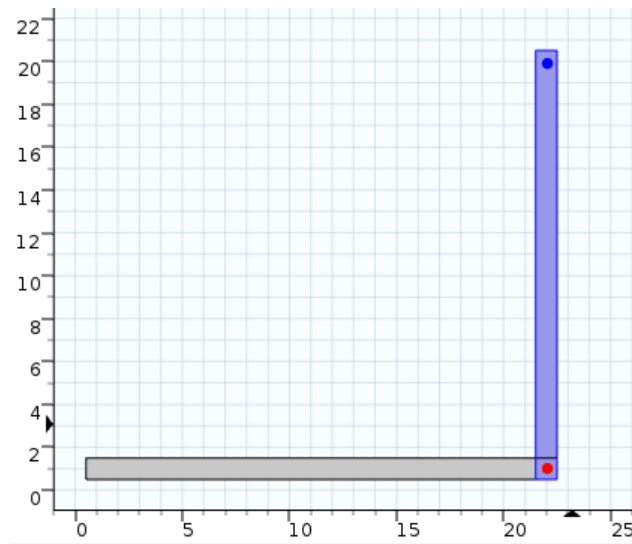


Fig. 5-37. Connecting channel segment

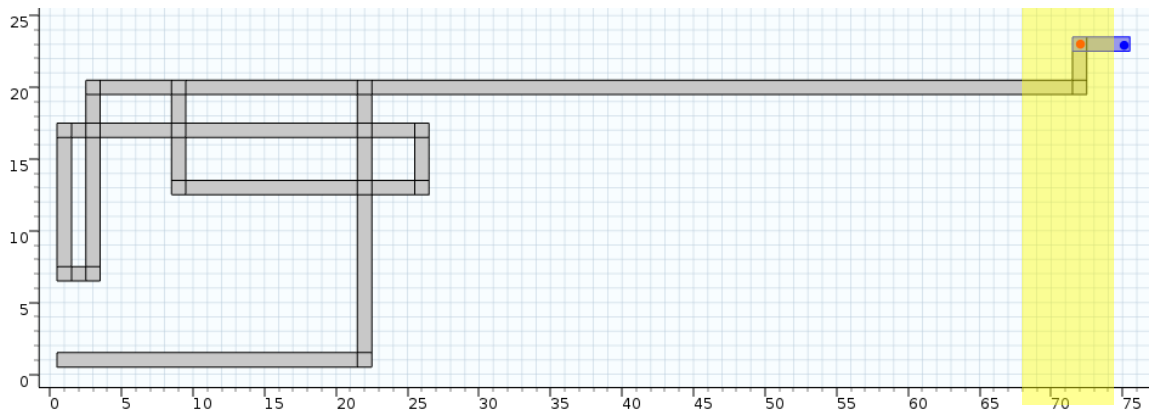


Fig. 5-38. Approaching the outlet

After finishing the first channel branch, a second branch repeats the same process. Starting from (1,2), the channel keeps walking until reaching the outlet location, (89,2). As shown in blue in the Fig. 5-39, there are some interactions with the first channel branch.

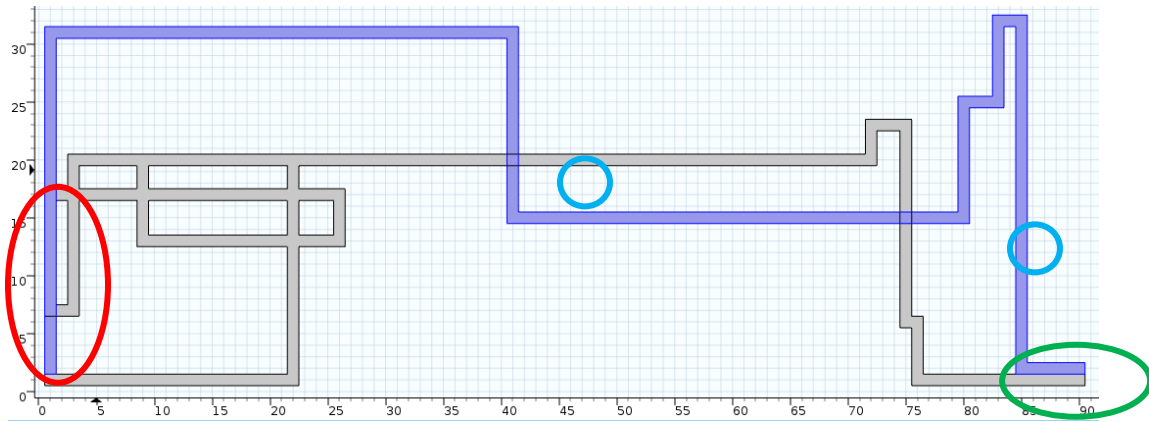


Fig. 5-39. Interaction between channels

- For the overlapped segment shown in the red circle, two channels share this same segment.
- Cross points are formed in the blue circles. Once crossed, the two independent channel branches are connected. Liquid comes to this point will be redistributed to all directions, based on the pressure drop of each branch.
- The parallel channels in the green circle merge to one channel with double width.

The number of channels inside the heat sink is randomly ranging from 2-10. In this example, six-channel branches, initialing from (1,1), (1,2), (1,5), (1,6), (1,9), (1,10) are initialized. After all channels are constructed, a merged channel is connected to the inlet and outlet of the pump, as shown in the blue block in Fig. 5-40.

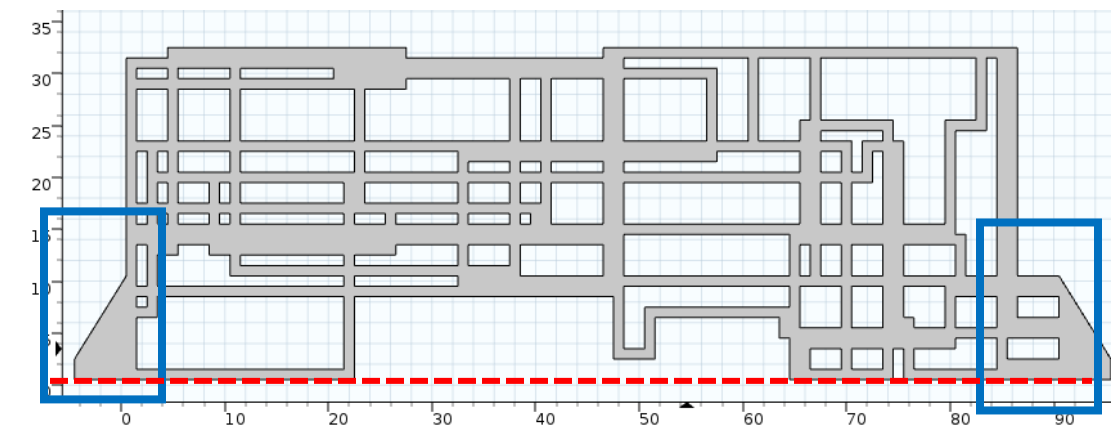


Fig. 5-40. Construction of channels

As shown inside the blue rectangle, the inlet and outlet are constructed correspondingly to match the width of the connected channels. Because of the symmetric, only half of the channel pattern is shown in Fig. 5-41.

Additional modifications are implemented named as “corner refinement”. Instead of using a sharp right angle of the elbow, the corner is replaced by a 45-degree turn with a smoother shape, as shown in Fig. 5-41. Instead of using a sharp right angle of the elbow, the corner is replaced by a 45-degree turn with a smoother shape.

This corner refinement contains two actions: The first action is named chamfer. It cut the previous sharp corner of the elbow turn, as shown in the red dashed line. The second action is named compensation. To maintain the pressure drop balance of the narrowed corner, this action adds an extra square at the turning point to keep the same channel width. The modified channel branches are shown in Fig. 5-42.

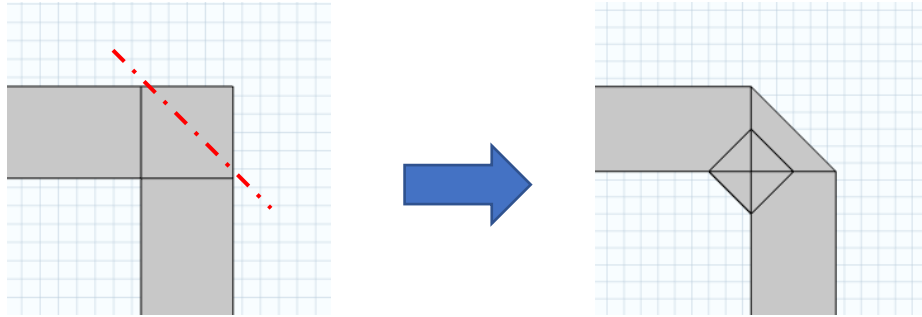


Fig. 5-41. Corner refinement

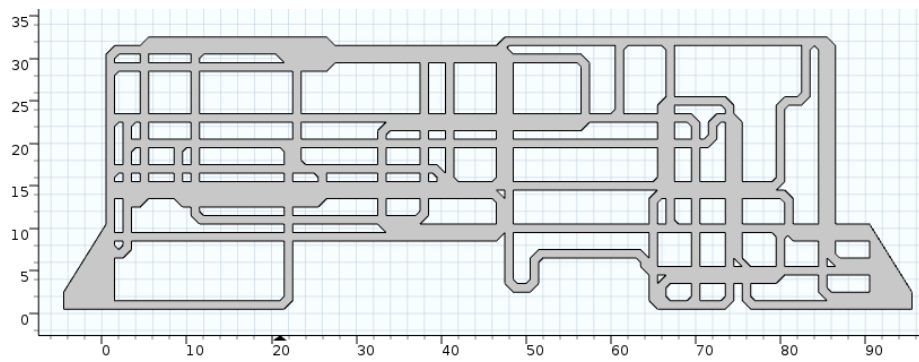


Fig. 5-42. Complete construction of a half symmetrical channel design

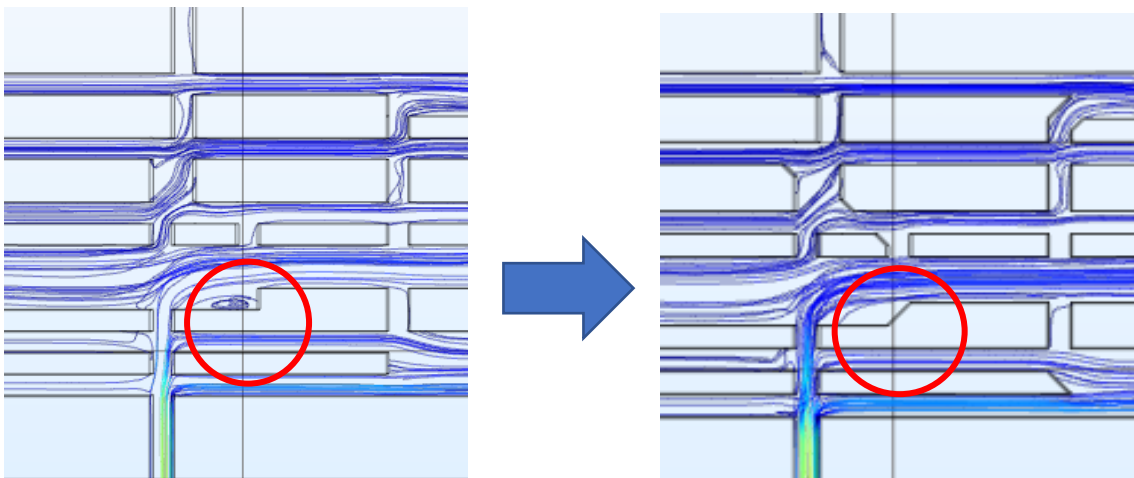


Fig. 5-43. The superior performance brought by the corner refinement

Due to the smoother elbows, benefits have been found based on the comparison results. Simulations have been studied with the same operating conditions. Less undesired turbulence presents as shown in Fig. 5-43 and 2% lower temperature profile plus 5% lower pressure drop have been achieved by this corner refinement

After initializing the channel pattern in the 2D cross-section workplace, this channel pattern is then extruded in the third direction and extracted from the Aluminum block of the heat sink block. Half of the symmetric heat model is built in the COMSOL as shown in Fig. 5-44. For a complete model, predefined heat sources are also constructed on the surface of the heat sink.

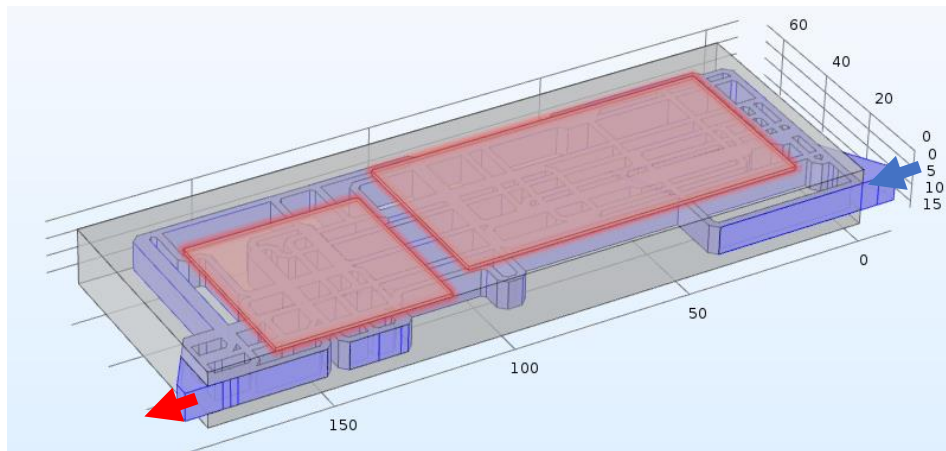


Fig. 5-44. Half of the symmetrical heat sink in COMSOL

For other cases with other auxiliary components, such as DBC, discrete dies, and screw thread holes, those parts can be imported into the model through the interface link between COMSOL and SOLIDWORKS. To simplify the design process, auxiliary components are not included in this design case.

The aforementioned construction process converts the heat sink DNA into a 3D structure model in COMSOL. FEA evaluation based on this model will be described in the following chapter.

5.8.6.Evaluation

Settings and evaluation of the 3D model are automatically accomplished. The overall contribution in this section is to define the evaluation function $T=F(\mathbf{X})$, where T is the fitness value of the individual, $\mathbf{X}$ is the DNA of the individual under evaluation and F is the evaluation function constructed in this section. Several steps are included in the evaluation process.

- Materials setting

For a more realistic performance evaluation, different materials are set to domains. Most of the materials property can be set by default material library built in COMSOL, only except the thermal property of additive manufactured Aluminum. The gray part of the figure is the Aluminum heat sink body. Based on the thermal property introduced in Chapter 2, the thermal conductivity is set to be a custom function of the local temperature of the material. The Heat sources of the red domains are as steel to present base plate material of the module, and the rest parts of the module are ignored as a simplification. The domain in blue is set to be water. A layer in between the heat source and the heat sink is constructed as TIM with an average thermal conductivity of 8.9 W/mK, as Arctic Silver® 5 thermal paste, with a thickness of 100 μm .

- Physics of heat transfer

All domains in this model contribute to the heat transfer evaluation. Heat conduction is set in both solid and fluid domain and heat convection is set on the contact surface of two media. The initial temperature of the model and the ambient temperature are set to be 20°C. The power loss of the converter is assumed to be uniformly distributed at 900W. As simplified, the symmetry boundary condition is set on the corresponding surface. The outlet is the only surface dissipating heat out of the system. All other boundaries are assumed to be thermal insulation without heat transfer to the ambient. A thin layer is created as the thermal interface material as stated in the material section.

- Physics of heat transfer in Fluid

This boundary condition enables the flow rate adjusted based on the pressure drop of the designed heat sink. The flow rate of the operating point is then determined at the crossing point of the pump profile curve and the pressure drop curve of the heat sink. As a multiple-objective optimization problem, which will take a longer optimizing time, the flow rate and junction temperature are directly related, and the pressure drop of the designed heat sink is not separately optimized. Instead, only the maximum junction temperature is considered as the optimization targets are converted to be single. The temperature of the inlet fluid is the room temperature assuming a radiator with enough capability. As the Reynolds number has been defined previously in Eq. 5-10. Re of this case is much smaller than 1000, and the type of fluid set as Laminar flow.

- Multi-physics interaction

Based on governing equations of different physics setting, two independent profiles: temperature distribution and flow field can be acquired after FEA solver. Multi-physics then interact the two profiles by regarding the fluid as a non-isothermal flow. By this mean,

the temperature profile will impact on the flow field distribution and verse visa. To ensure the convergence of the system, the fluid is set to be weakly compressible flow so that the density of the fluid is changeable as well.

- Finite element mesh

Genetic Algorithm, as introduced previously, is a population-based optimization tool. The optimal result will be reached by evaluating a huge amount of the individuals before convergence. Due to the high volume of computing requirement, it is necessary to evaluate one single individual as fast as possible. In the first section of this chapter, the introduction of the FEA simulation states the tradeoff between the computation time and the accuracy of the result. For a reliable solution, a property mesh is a key. By default, COMSOL has an automatic mesh algorithm to control the size of mesh elements. It is acceptable as a one-time simulation, even for hours or days. But to achieve a higher computation speed in this case, a custom mesh algorithm without sacrificing the accuracy is proposed. Variety size of mesh elements are constructed in different domains based on the significance of the final result profile:

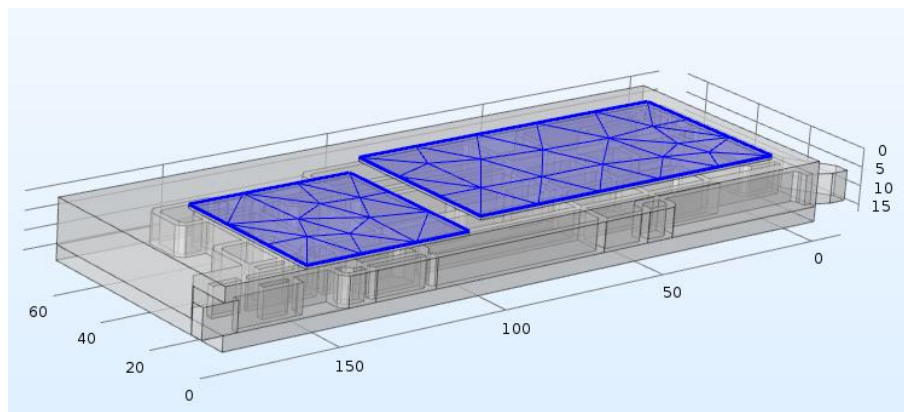


Fig. 5-45. The first step of the customized mesh algorithm

- Heat source domain: Due to the less significant of those domains as shown in blue in Fig. 5-45. The heat sources are considered as uniformly distributed and the coarsest mesh using triangular prism is implemented in this domain. Tens of finite mesh elements are constructed in this domain.
- Upper heat sink domain: including base plates and the top surface of the heat sink, the heat flux density is high and has a significant influence on the overall temperature profile. Either vertical or horizontal heat flux should be taken into consideration. Thus, a more flexible type of mesh – the free tetrahedral meshes are applied in this domain. The quality of the meshes is relatively high. More than five thousand of the mesh elements has been constructed in Fig. 5-46.

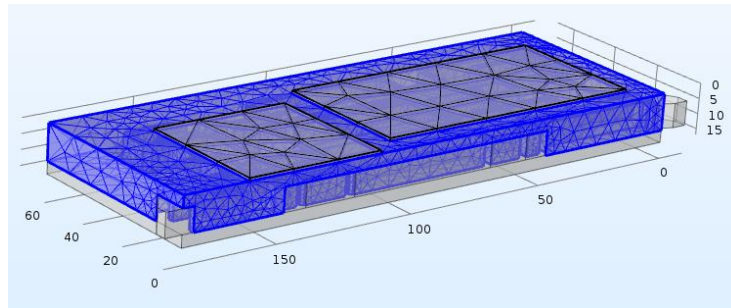


Fig. 5-46. The second step of the customized mesh algorithm

- Fluid domain: This domain has multiple physics governing equations, including heat conduction, heat convection, and fluid dynamic equations. Due to a high order of non-linear property and complex flow structure, this domain the highest mesh quality. Tetrahedral meshes with the limited maximum element size are built the region,

especially near the corners. As shown in Fig. 5-47, the majority of the mesh elements, around twelve thousand, are found in this fluid domain.

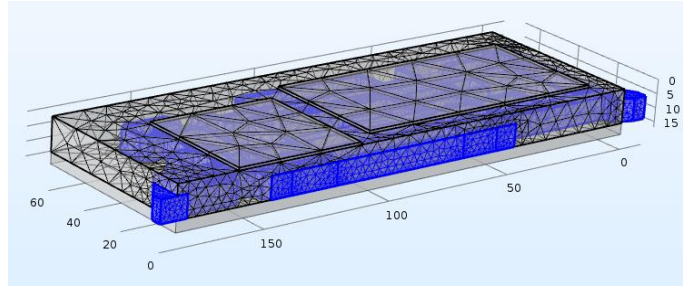


Fig. 5-47. The third step of the customized mesh algorithm

Contact surface domain: In addition to the mesh of fluid domain, the boundaries in between fluid and solid domains are taken care of with another type of meshes. During the simulation, the velocity of the flow changes relatively slowly in the direction of the fluid channels. However, rapid changes in the normal direction, especially when nearby the contact boundaries. On the other hand, addition thermal convection physics happens only on those domains. The contact boundaries are important to dissipating heat flux. Instead of tetrahedral meshes, prism meshes generated based on thin triangles or rectangles in 2D are applied, as shown in Fig. 5-48. With only an additional three thousand mesh elements built, the accuracy of the results is guaranteed.

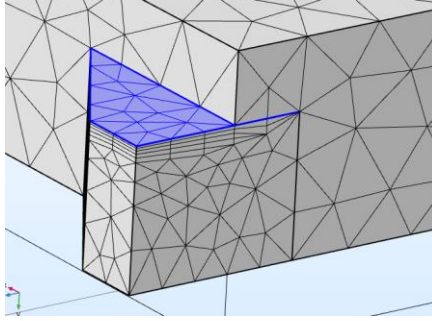


Fig. 5-48. The fourth step of the customized mesh algorithm

- Rest of domains: As shown in Fig. 5-49, the blue domain, especially near the lower side of the heat sink, the accuracy of the FEA simulation has a negligible impact on the performance evaluation. Only low-quality mesh elements are necessary. Few mesh elements are used in those domains.

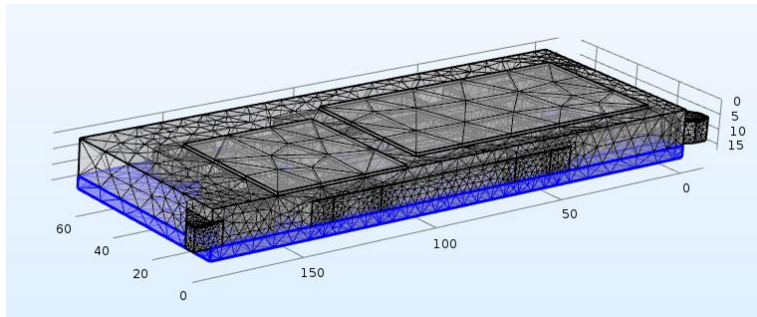


Fig. 5-49. The final step of the customized mesh algorithm

The custom mesh algorithm has been approved by comparing to the accurate performance evaluation results of a fine mesh. Based on the computation time-tested by a workstation with six-core 3.5 GHz processors and 40GB of RAM, 5 to 10 times computation time reduction can be expected without scarifying the accuracy.

- Evaluation

After the complete list of setting instruction invoked from the algorithms in MATLAB, a stationary solver is applied using the default fully coupled set. The target performance value is the maximum junction temperature of the whole module. With the maximum temperature probe, the target value is automatically reported back to the main algorithm through the interface. And the fitness value of each individual is assigned.

5.8.7. Optimization performance

The converge plot and the result comparison will be illustrated at the end. For a better comparison, variables except the liquid channel design are controlled identically to the conventionally designed heat sink. As the evaluation function $T=F(\mathbf{X})$, described in the previous sections, the Genetic Algorithm based optimization is applied in this case. For a population of 31 individuals, a list of fitness scores is created in GA. Survival possibility of each individual is proportional to the fitness. Selection is then applied to pick up 24 survived individuals into the mating pool and the crossover and mutation take place and generate a group of 24 offspring. With another six new individuals and one elite design, a total of 31 individuals becomes the next generation. This process repeats until the convergence reaches.

Convergence plot of this design case in Fig. 5-50 shows the optimization process. Red dash line in the plot is the baseline performance of commercial heat sink and the green lines divide the plot into three major periods.

Optimization of this design case took about 70 iterations, which is about 5 days to reach the convergence state. The temperature profile of this optimized design is shown in Fig.

5-51

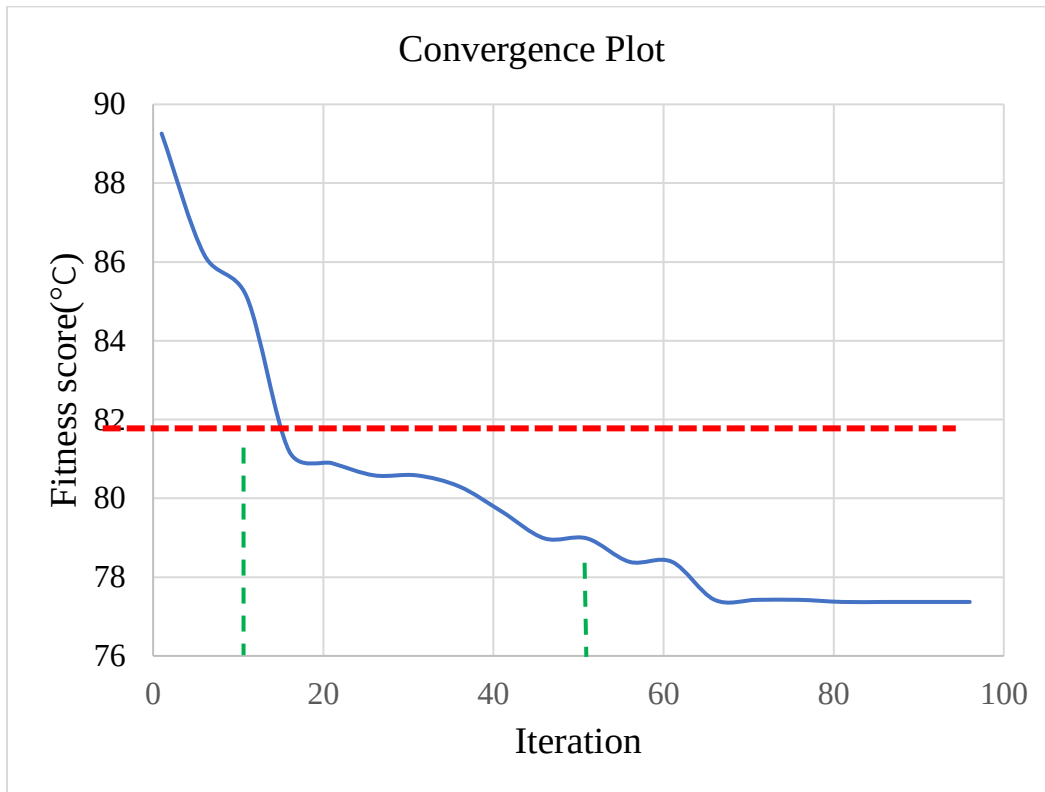


Fig. 5-50. Convergence plot of the optimization process

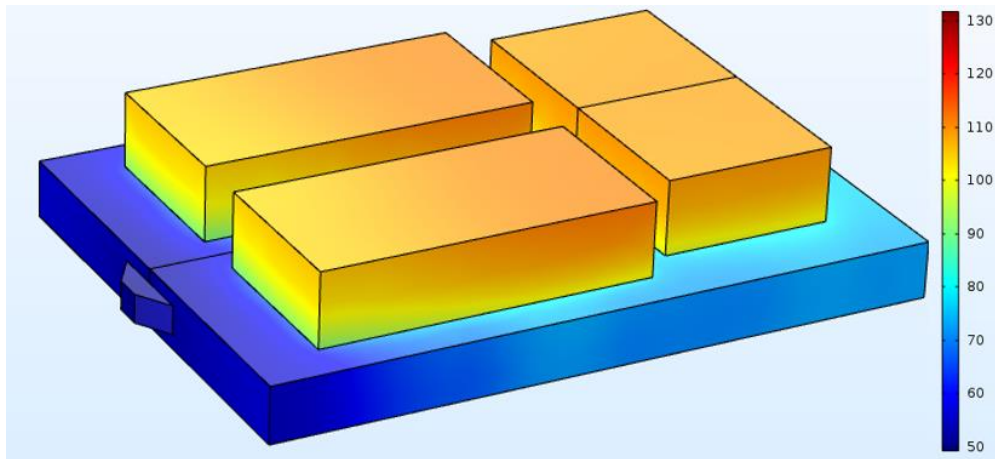


Fig. 5-51. (b)The temperature profile of optimized design

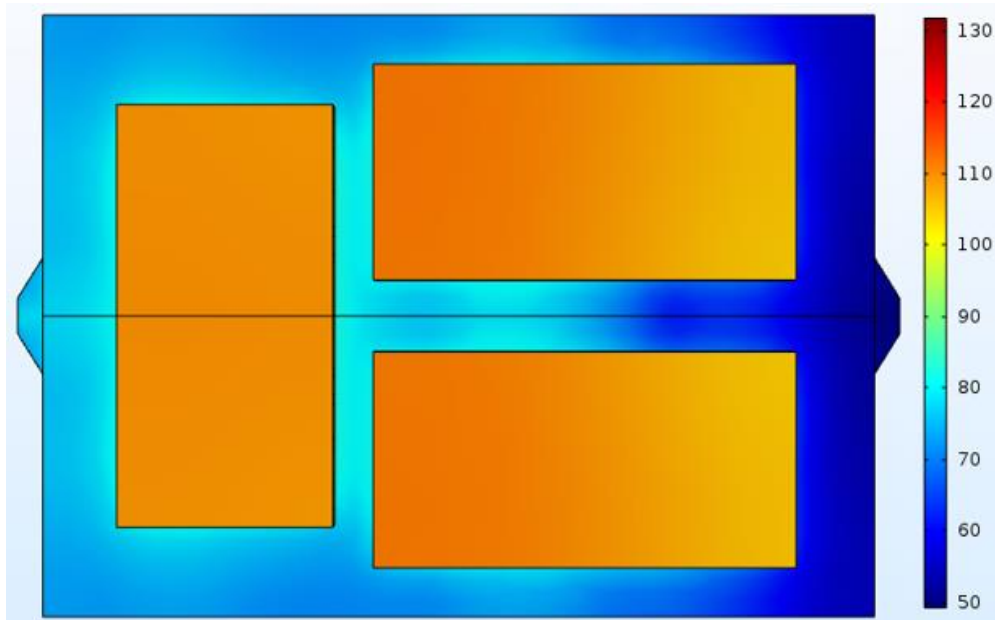


Fig. 5-51. (b)The temperature profile of optimized design

Compared to the temperature profile of the conventionally designed heat sink, a more evenly distribution of the junction temperature is achieved. This further leads to a reduced junction temperature. Under the identical simulation boundary conditions, the max junction temperature reduced from 103 °C of the conventionally designed heat sink to 88 °C of the optimized heat sink, that is about 30% improvement in terms of junction temperature.

5.8.8.Experimental test setup

As noticed from the simulation comparison, great performance improvement has been achieved by the proposed optimization method. Based on this optimization result, both conventionally designed heat sink and the optimized heat sink are 3D printed in Aluminum keeping size and design features identical, the printed part, as well as the x-ray scan of GA optimized heat sink, are shown in Fig. 5-52.

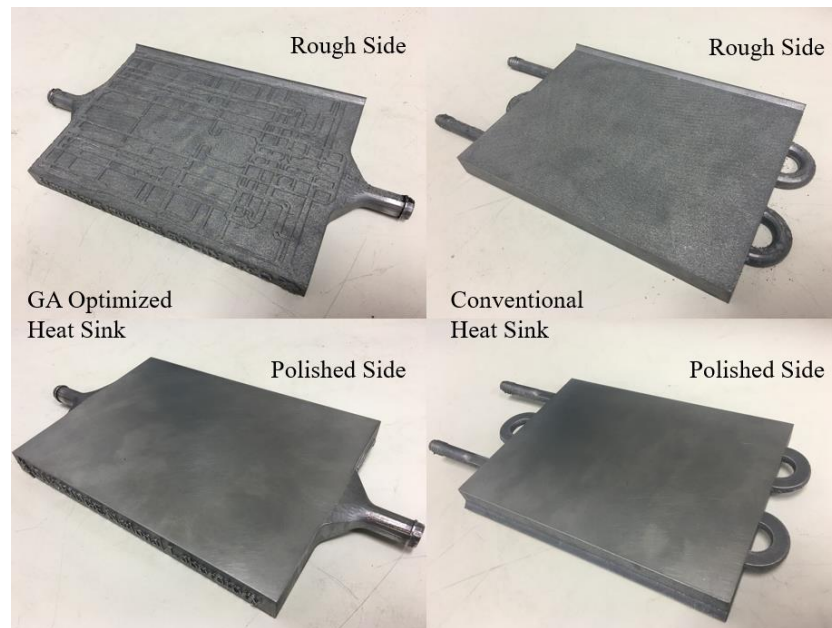


Fig. 5-52. 3D printed heat sinks

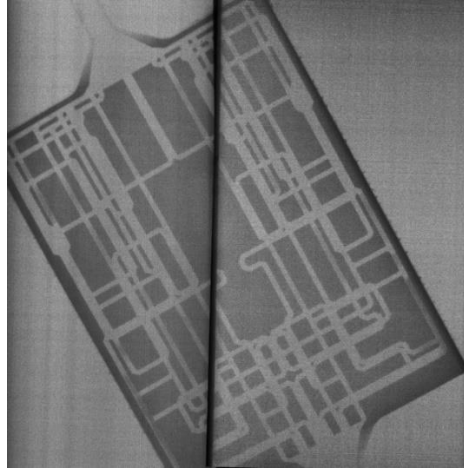


Fig. 5-53. X-ray scan of 3D printed optimized heat sink

The surface finish of 3D printed part is quite rough. Surface polishing as a post-process on the heat side contact surface is necessary to avoid additional thermal impedance introduced in TIM.

Two slots on the baseplate of the power module, which can test the temperature directly under the device and the center temperature are cutter as shown in Fig. 5-54. Two Omega K12 thermocouples are inserted into the slots and the baseplate temperature is determined by the average value of two measured temperatures. T_{gon} , as both TIM and agglutinant is attached to the baseplate of the power module.



Fig. 5-54. Phase-leg module and the thermocouple locations

Normal pressure over 100 psi is recommended in the Tgon datasheet to provide expected performance. Two pieces of cover printed by ABS plastics are designed in SOLIDWORKS, verified in COMSOL and printed out to provide the machinal support and enough normal pressure, as shown in Fig. 5-55. In total 10 screws connecting two covers provide large enough, evenly distributed normal pressure to suppress TIM thickness and fill the air gaps of all three modules.

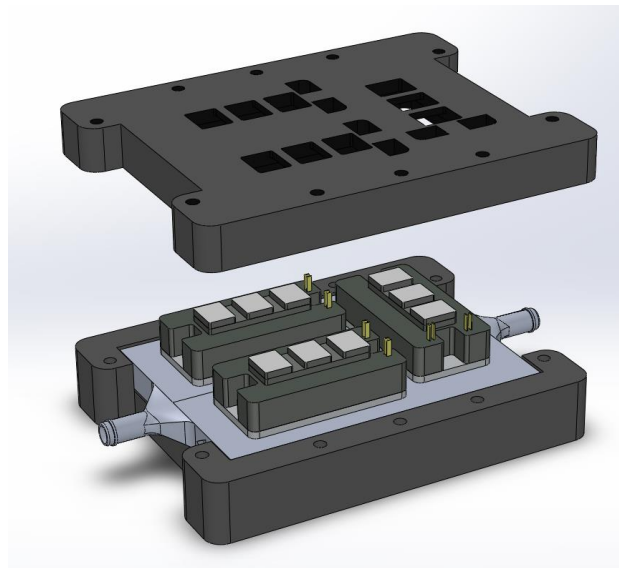


Fig. 5-55. Two-piece printed lead frame covers

In order to test the thermal performance of the module, power losses need to be generated. Because the test focuses on temperature performance of the heat sink, to simplify the experimental test, only conduction losses, $P = I_{CE} \times V_{CE}$ of IGBTs in the module are generated. To balance the heat loss distribution, both upper switch and lower switch are turned on at the same time. Because of the limited current rating of the power supply, a high on resistance is necessary to generate enough losses with the limited

current. Based on the output characteristics of power module in Fig. 5-56, the gate voltage V_{GE} is limited to 10V to keep the on-resistance larger than 20 m Ω .

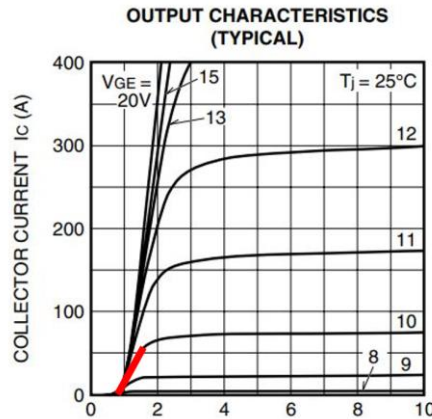


Fig. 5-56. Output characterization and the utilization region of the power module

In the designed experimental test, six gates will be turned on simultaneously. Because of the different emitter voltage level on different devices, six isolated V_{GE} should be applied. In order to provide a voltage penitential between gate and emitter terminals, a 24V input, $\pm 5V$ output DC/DC power supply, part number NMA2405SC, is picked. As shown in Fig. 5-57, a customized gate drive board with six picked power supplies are manufactured with auxiliary RC circuit to stable the output voltage.

Using this gate drive system, six isolated 10V voltage DC power can be applied separately to six gate and emitter terminals. Two topologies of connecting six switches, namely, parallel and series connection are available. Due to the limit of the main current rating of power supply, parallel connection can limit the total power losses available. Moreover, based on the temperature dependent characterization of the device, a negative

temperature coefficient can be noticed. Because of the uneven temperature distribution of three modules noticed from simulation, the negative coefficient can further enlarge the uneven temperature profile. Instead, series topology by connecting the lower E terminal of one module to upper C terminal of the second module can avoid such issues, as shown in Fig. 5-58.

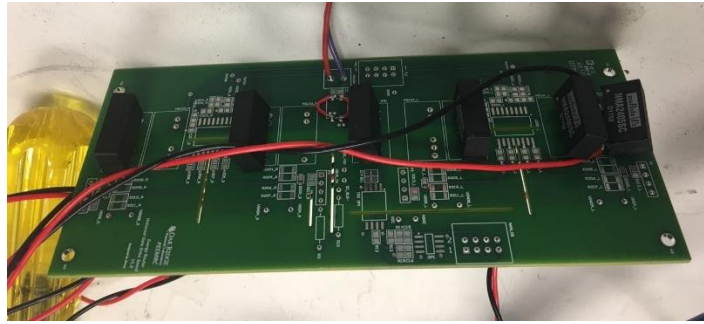


Fig. 5-57. Six-channel outputs gate voltage power supply board

Hardware is implemented in such topology and connected to the current source as shown in Fig. 5-59. Underneath the modules, six thermocouples are embedded and labeled from T1 to T6 as shown in Fig. 5-60.

The test bench is set up as shown in Fig. 5-61.

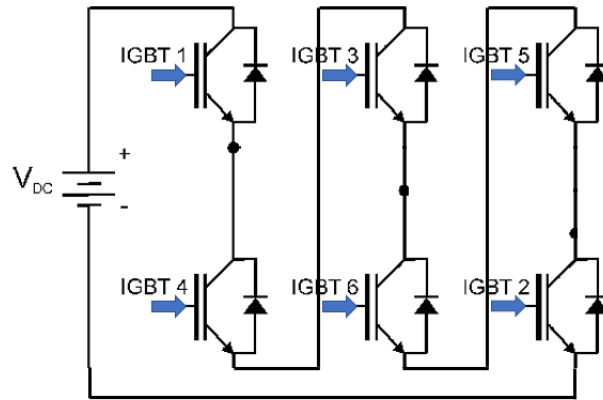


Fig. 5-58. Circuit schematic and interconnection of three power modules

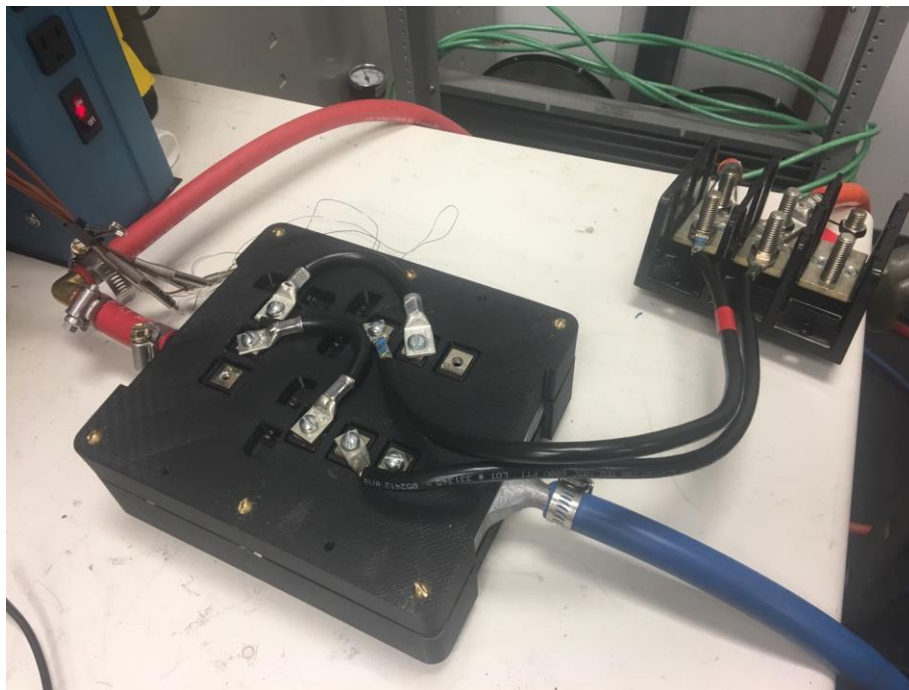


Fig. 5-59. Test hardware implementation

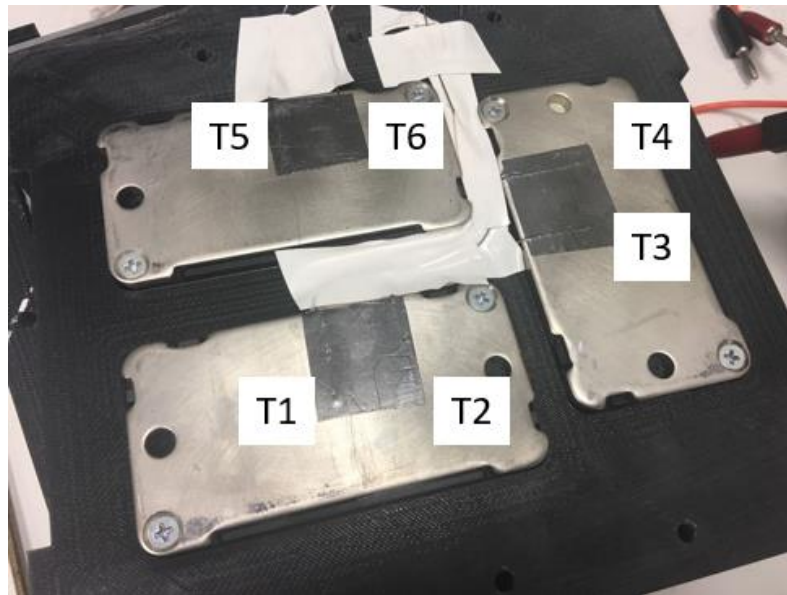


Fig. 5-60. Locations and labels of thermocouples

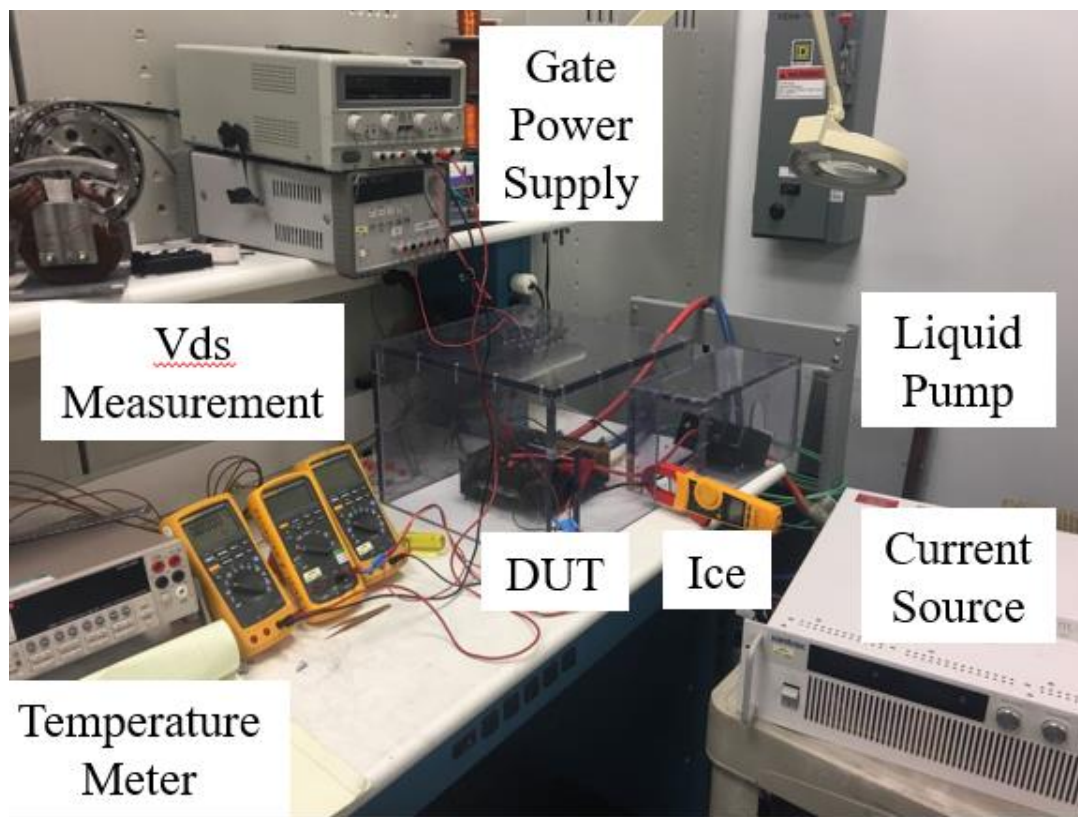


Fig. 5-61. Heat sink performance evaluation test bench

With the step increased current input, all temperature data from T1 to T6, the voltage drop across all three modules and the current source output are recorded for both conventional designed case and the GA optimized case.

5.8.9. Test results

The tests are implemented by varying the current level output from the current source, measuring the voltage drop across each module and collecting the temperature profile at each thermocouple location. Using the gate drive board shown previously, the input voltage from the gate power supply is 24 V and the output voltages are 5V and -5V. By connecting to all pairs of G and E pins of the module, a gate voltage around 10V is applied to each IGBT. At each test point, three data are recorded:

- The current from the current source through all six series switches: I (A)
- The voltage drops across both IGBTs of the module (V_C1-E2): V1 V2 V3 (V)
- Measured temperature from thermocouples of all six locations: T1~T6 (°C)

However, due to the high thermal resistance from junction to case, which is about 0.2 °C/W and not modeled in the simulation case, a reduced power loss is applied in the experimental case. Since the thermocouples used in this experimental test can only get the temperature of the case, which is located at the bottom of the baseplate. In order to limit the junction temperature within a safety region below 125 °C, the temperature at the case is limited based by:

$$T_c < 125 - T_A - P_{in} \times R_{th_{case}} \quad \text{Eq. 5-11}$$

Thus, the actual loss used in the experimental test is smaller than the simulation case when it was designed. However, the comparison, which can be interpreted as the case to ambient thermal resistance, is still valid to see the relative relations.

The test data of both conventional designed case and the Genetic Algorithm optimized case are shown in Table 5-5:

Calculated based on test data listed above, the loss of each module is calculated by the product of channel current I and its corresponding voltage drop $V_1 \sim V_3$. Temperature profiles (T_{Bottom} , T_{Left} and T_{Right}) use the average value of both test locations in one module, i.e. $T_B = (T_1 + T_2)/2$ as the reference temperature. The updated performances are summarized in Table 5-6.

Table 5-5.(a) Test data of Genetic Algorithm optimized heat sink

I	V1	V2	V3	T1	T2	T3	T4	T5	T6
6	1.64	1.64	1.64	24.6	24.5	22	22	25	24.5
10	1.8	1.8	1.79	28.4	27.4	23.4	23.2	29	28.2
15	1.95	1.93	1.93	33.5	32	25.3	25	34.5	33
20	2.05	2.06	2.04	38.8	36.7	27.6	27.8	40.5	38.5
25	2.15	2.13	2.12	44.2	41.3	29.5	30	46.5	43.9
30	2.23	2.2	2.2	50.1	46.6	32	33	52.7	49.6
35	2.3	2.26	2.25	56	52	34.6	36.7	59.3	55.6
40	2.36	2.32	2.3	62	57	37.5	40	65.9	61.6
45	2.42	2.37	2.35	68.4	62.8	40	43	72.9	68.1
50	2.48	2.42	2.39	74.9	68.7	42.7	46.4	80	74.6
55	2.52	2.46	2.43	81.6	74.8	45.6	50	87.4	81.6
60	2.57	2.5	2.46	87.9	80.5	48.1	53.4	94.4	88
65	2.61	2.53	2.5	94.8	86.8	51.1	57	101.6	94.8

Table 5-5.(b) Test data of conventionally designed heat sink

I	V1	V2	V3	T1	T2	T3	T4	T5	T6
5	1.59	1.59	1.59	23.9	23.4	22.2	22	24.9	24.6
10	1.8	1.8	1.78	28.3	27.1	24.3	23.9	30.5	30
15	1.94	1.93	1.92	32.9	31.1	26.6	26	36.3	35.2
20	2.05	2.04	2.02	37.9	35.4	29	28.3	42.6	41.1
25	2.14	2.13	2.1	43.4	40.2	31.9	31.1	49.6	47.5
30	2.22	2.2	2.17	49	45.1	34.7	34.2	56.6	54.2
35	2.3	2.27	2.23	54.9	50.3	37.7	37.5	63.7	60.8
40	2.36	2.33	2.28	60.43	55.2	40.4	40.3	70.8	67.4
45	2.42	2.38	2.33	66.6	60.6	43.6	44.1	78.2	74.3
50	2.47	2.43	2.37	72.4	65.7	46.3	47.2	85.5	81.2
55	2.52	2.47	2.4	78.5	71.2	50	51	92.9	88
60	2.56	2.51	2.43	84.6	76.6	52.7	55.2	100.3	95

Table 5-6.(a) Temperature responses of varied power losses, Genetic Algorithm HS

P_L (W)	T_L (°C)	P_B (W)	T_B (°C)	P_R (W)	T_R(°C)
9.84	24.095	9.84	23.2	9.84	24.275
18	27.11	18	25.28	17.9	27.74
28.95	31.475	29.25	28.24	28.95	32.375
41.2	35.975	41	32.32	40.8	37.55
53.25	40.475	53.75	35.6	53	42.68
66	45.515	66.9	40	66	48.035
79.1	50.6	80.5	45.04	78.75	53.705
92.8	55.55	94.4	50	92	59.375
106.65	61.04	108.9	54.4	105.75	65.45
121	66.62	124	59.28	119.5	71.57
135.3	72.38	138.6	64.48	133.65	78.05
150	77.78	154.2	69.2	147.6	84.08
164.45	83.72	169.65	74.48	162.5	90.38

Table 5-6.(b) Temperature responses of varied power losses, Conventional HS

P_L (W)	T_L (°C)	P_B (W)	T_B (°C)	P_R (W)	T_R(°C)
7.95	23.65	7.95	22.1	7.95	24.75
18	27.7	18	24.1	17.8	30.25
28.95	32	29.1	26.3	28.8	35.75
40.8	36.65	41	28.65	40.4	41.85
53.25	41.8	53.5	31.5	52.5	48.55
66	47.05	66.6	34.45	65.1	55.4
79.45	52.6	80.5	37.6	78.05	62.25
93.2	57.815	94.4	40.35	91.2	69.1
107.1	63.6	108.9	43.85	104.85	76.25
121.5	69.05	123.5	46.75	118.5	83.35
135.85	74.85	138.6	50.5	132	90.45
150.6	80.6	153.6	53.95	145.8	97.65

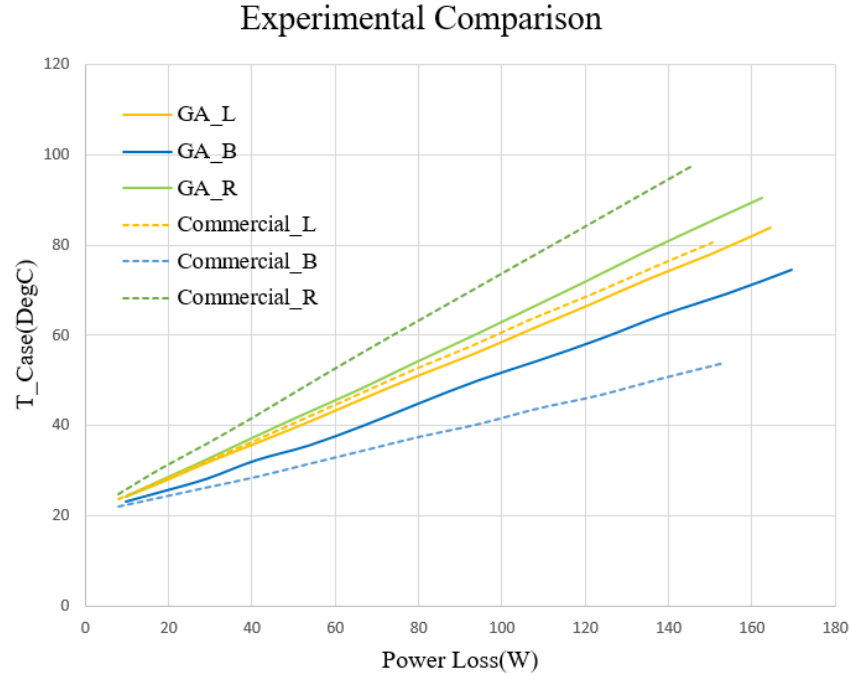


Fig. 5-62. Experimental comparison

For better comparison, the performances of both heat sinks are plotted in Fig. 5-62.

Several conclusion can be noticed from the plot:

- The max junction temperature of the GA optimized heat sink has been reduced compared to the commercial heat sink. Though the lowest module temperature of the commercial design is lower than all three modules of the GA based design.
- Huge temperature variations among all three modules of conventional design lead to the higher maxima temperature. On contract, the distribution strategy brought by the algorithm balances temperature profile. The best module performance may seem worse than the conventional group. But the overall performance of all three phases is enhanced with a lower maximum junction temperature. That consist of the fitness function set in the algorithm.

- Because of the different power levels in simulations and experiments, comparing junction temperature alone is not sufficient. Thermal resistance is used for the comparison of two groups since it has decoupled with the total power loss. Based on the calculation of GA designed case, the average case to the ambient thermal resistance of the experimental set is $0.37\text{ }^{\circ}\text{C/W}$. While this value of the simulation group is $0.33\text{ }^{\circ}\text{C/W}$. A small difference within two groups can be attributed to the contact resistance of the thermocouples that put an additional thermal resistance to the system.
- Ideally, the temperature profile of GA_L and GA_R should be identical because of the symmetrical heat sink design. However, due to the uncertainty inside the module, for example, the thickness of TIM, the contact resistance of the thermocouple, there are some mismatches.

Overall, according to the data analysis and comparison between conventional designed and GA optimized cases, a big improvement larger than 25% can be claimed by using such an optimization method. Though the junction temperature is used in this chapter as the variable of the fitness function, a similar method can be also applied to the volume based optimization in other applications. The methodology introduced in this chapter contributes to the left part, which is the thermal domain of the multi-objective optimization plot. The rest components of this flowchart will be introduced in the later chapters.

6. Parasitic Domain

6.1. PARASITIC INDUCTANCE

Whenever current flowing through a piece of metal, there will always be inductance, as interrupted by Lenz Law. The parasitic inductance, as it named, parasites inside the power module from chips to their terminals, regardless of what kind of packaging design is used. A large parasitic inductance existing in the packaging could cause serious overshoot issue and damage the device during the switching transients. During the on period, parasitic inductance stores electric energy when the current flows through the packaged module. Stored energy is then released during the turn-off transient when the current is decreasing. The extra energy forms a voltage spike in addition to the blocking voltage. The magnitude of overshoot spike is proportional to the product of parasitic inductance and turn off speed di/dt .

The purchasing higher switching speed not only enables an ultra-fast switching frequency for reduction of passive components but also decreases the switching loss per transient due to the shorter IV overlapped time. Developments in the power semiconductor devices and the advanced gate driver controller enable the fast switching potential. However, the high switching speed noted as di/dt further adds the voltage stress due to the voltage overshoot issue. Modifications such as reducing the nominal voltage or picking a higher rated voltage device could temperately apply for higher switching speed. However, side effects including higher conduction losses, higher device cost, and lower reliability still pose challenges. Alternatively, focus on the parasitic inductance

optimization could fundamentally solve this overshoot issue with elevated switching speed.

Three major contributions to the overall parasitic inductance calculation has been stated:

1. Inductance introduced by output terminals;
2. Inductance introduced by DBC substrate copper trace;
3. Inductance introduced by wire bonds;

As what can be found in a 300 A 1200 V commercial power module, parasitic inductance distribution of such components are shown in Table 6-1.

Table 6-1. Parasitic inductance distribution in a module

	Wire Bonds	DBC Substrate	Terminals
Parasitic Inductance	10-15 nH	4-7 nH	30-40 nH

Targeting on such elements, optimizations on packaging design have been made to reduce the parasitic values.

As the largest portion contributed to the overall parasitic calculation, Terminals of a power module are commonly made of bulk metal for the stable mechanical structure and a high current capacity. The huge self-inductance significant contributes to the overall module parasitic inductance. Generally, two basic approaches have shown enough performance that can offsite this big inductance.

The first approach is to “short” the terminals using decoupling caps. Parasitic inductance is critical to the overall performance only during the switch transient period, where a high di/dt occurs. By place, several decoupling caps near the terminals, the high-frequency

portion of the current will bypass the terminals with large parasitic inductance and be shorted by the caps. By this method, most of the inductance introduced by the terminals won't be counted as the power loop stray inductance and a significant reduction could be achieved. However, placing decoupling caps, most of time ceramic capacitors will bring in additional reliability issues.

Alternatively, another approach, laminated bus bar structure is also available for the module designs. The laminated structure is constructed by paralleling the positive and negative terminals. Because of the opposite current directions flowing through both terminals, a significantly large coupling mutual inductance is formed between two laminated bus bars. As an offsite, mutual inductance will reduce the overall terminal inductance introduced since the equivalent inductance equals to the self-inductances minus the mutual inductance.

With either of the approaches, the negligible contribution will be posted by terminals during the power loop parasitic inductance calculation. Without considering the impact of the terminals, optimization targets are reduced to only components on the substrate, i.e., wire bonds and DBC current routing. As for wire bonds, it can be optimized by shortening the wire length to reduce the self-inductance magnitude. The self-inductance of the straight round conductor, which can be modeled can be modeled as

$$L = \frac{\mu_0 l}{2\pi} \left(\ln \frac{2l}{d} - 1 \right) \times 10^{-3} \quad \text{Eq. 6-1}$$

Where l is the length of the conductor, d is the diameter of the cross-section, μ_0 is the

The rest of self-inductance coming from bond wire, the copper trace is negligible compared to the loop inductance. Thus, the main optimization target in this dissertation is the loop inductance optimization.

In this chapter, the optimization of parasitic inductance inside a phase-leg module is simplified to the optimization of power loop area formed by positive bus – upper switch – phase output trace – lower switch – negative bus.

6.2. SEMICONDUCTOR DEVICE LAYOUT ON SUBSTRATE

In nowadays power electronics applications, power module has gradually replaced the paralleled discrete devices due to its better-paralleled devices performance and lower parasitic inductance. The normal structure inside a power module contains single or paralleled bare devices with interconnected wire bonds soldered or sintered directly on the substrate. Among all available substrate materials, direct bonded copper (DBC) is the most commonly used material. They are manufactured as a sandwich structure where a ceramic tile in the mid-layer for electrical isolation with top and bottom boned by copper trace. The top copper layer is etched to the design pattern to provide the electrical interconnections while the bottom layer is usually attached directly to the baseplate or a heat sink for better thermal performance.

A typical example of DBC substrate with devices is shown in Fig. 6-2, where a phase-leg schematic with both upper and lower switches, as shown in Fig. 6-1, is placed on a DBC. Each switch position is composed by one MOSFET and one free-wheeling diode. Power loop in this design is marked in red with decoupling caps connecting dc bus terminals.

The power loop area inside the red loop is highly determined by the layout of devices. As mentioned previously, a smaller power loop is the key to achieve a lower parasitic inductance. Thus, the layout of devices is critical to the power module.

Similar to the manual heat sink design procedure, as a conventional layout design procedure, the design starts with an initial layout guess. Based on the parasitic inductance extraction result of the current design, revisions are made for further refinement. Repeating this process as iteration, each revision update generates a newer layout design. This design compares to previous cases designs and keeps up the better one. As reviewed for state of art, almost all power modules are designed in this method. However, the limited iteration capability of engineer makes this process not only time-consumable but also hard to reach the most optimized point. Genetic Algorithm optimization method, on the other hand, has shown great potential in the previous automatic optimization cased for heat sink design. The similar concept should be expected in the layout design as well for a superior performance.

6.3. LAYOUT OPTIMIZATION PROCEDURE

For any potential layout design candidate of this section, basic constraints of the layout are defined:

- No overlap is allowed as of any two components.
- Available DBC dimension is 60mm×40mm. All components must be inside the DBC boundaries.
- Geometry clearance between different components and distance to the boundaries (B_Clearance) should be larger than 2mm.

- Electrical clearance (E_Clearance) between polarities (Positive, Negative and Phase) is at least 5mm.
- Length of wire bond should be shorter than 12mm and the minimum landing area of the wire bond is 2mm×2mm.
- Each MOSFET is models as a rectangle of 6mm×8mm. Each diode is a square of 8mm×8mm.

Though certain values are given in the examples, those are adjustable for any particular design case. Starting from the simplest case, layout design procedure of a single MOSFET phase-leg module studied.

6.3.1. Layout design of a single MOSFET only module

In the first case, a power module constructed by single MOSFET without the anti-parallel diode is illustrated. As the phase-leg circuit assumed, only two MOSFETs are placed on the substrate. The design should follow the basic constraints.

Layout of either device is parameterized by center coordinate (x,y) and device orientation Ot. For each module layout design, a chromosome should include two pieces of information, (x1, y1, Ot1) and (x2, y2, Ot2). Ot can be either 1 or 2 where 1 means horizontally placed and 2 means vertically placed. The x is a random value ranging in $[-30+B_Clearance+3*\text{abs}(Ot-1)+4*\text{abs}(Ot-2), 30-B_Clearance-3*\text{abs}(Ot-1)-4*\text{abs}(Ot-2)]$ y is ranging in

$[-20+B_Clearance+4*\text{abs}(Ot-2)+3*\text{abs}(Ot-1), 20-B_Clearance-4*\text{abs}(Ot-2)-3*\text{abs}(Ot-1)]$

After initialization, the verification process is required to check if the given layout design has met all constraints. If not, the design is invalid and at either of the chromosome

will be modified until are constraints are met. A layout example, with chromosome of [6.12, 12.09, 1; 0.87, -9.76, 2] is shown in Fig. 6-3.

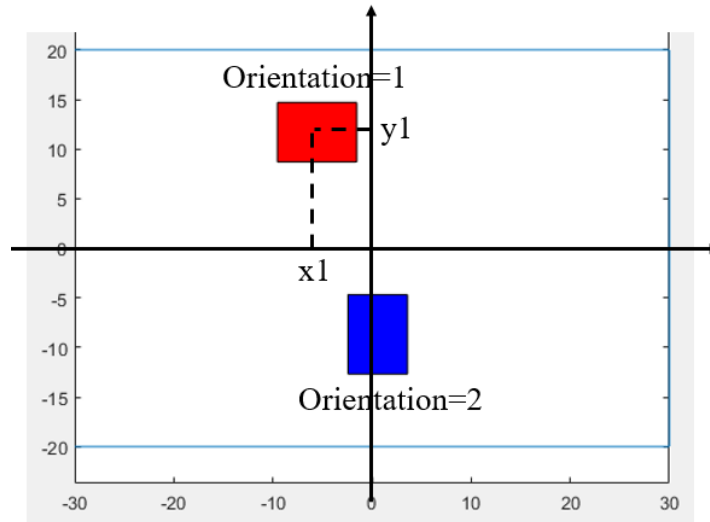


Fig. 6-3. Example of device layout on the substrate

Once the layout locations of the devices are confirmed, a routing process that determines the minimum power loop area is applied by several steps.

6.3.2.Branch and bound algorithm-based power loop extraction

Branch and bound algorithm (BB) is a strong algorithm to deal with discrete and combinatorial optimization problems. This algorithm performs the state space search by forming a rooted tree where all possible solutions are the branches of this tree. This method is similar to the method of exhaustion but with better-regulated searching principles. In order to reduce the number of calculations, the target tree is “pruned” to ignore completely sections of it which can't have better results than the best one already found in the searching history, without needing to fully calculate what results they may achieve. The target of this

algorithm is to find the best combinations of the devices, wire bonds and DC terminals locations that can form the minimum power loop. Steps of growing this tree are listed from the “root” to the “top of the tree”.

Step 1: Positive Terminal

The locations of the positive terminal are the first node of all branches. All possible terminals are located at the cross points by the line through the DBC center and the edges with a swept-step of 10° . But only terminals meet all following constraints can be selected as the first level nodes:

- As a planer DBC structure, terminals land on the boundaries only
- Terminals are modeled as a rectangle of $10\text{mm} \times 5\text{mm}$
- For any positive terminal location, the closer device is treated as upper switch and the other is the lower switch
- Positive terminal to the upper switch can separation of $B_Clearance$ while the other distance has to be $B_Clearance + E_Clearance$.

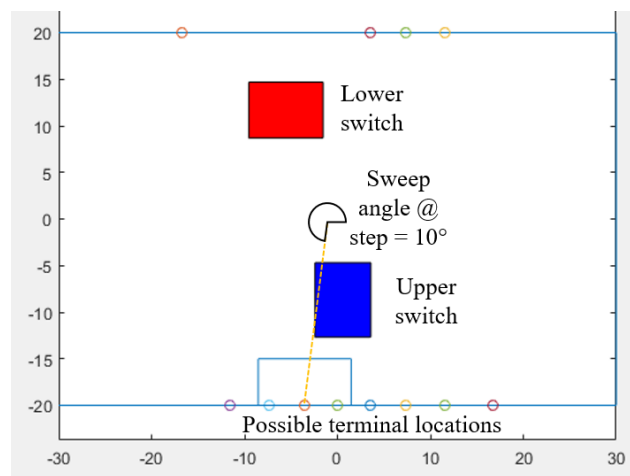


Fig. 6-4. Step 1: Positive Terminal

- The positive terminal cannot be more than half of the boundary length away from all devices.

With this given layout chromosome, all qualified terminal locations are plotted as round dot in Fig. 6-4. From each possible location, second level branches are initiated in Step 2.

Step 2: Positive Copper Trace and Upper Wire bond Location

For any of possible terminal location, the positive copper trace polygon is constructed by the clearance boundaries of the upper switch and positive trace. Except for the two “inner” corners, this polygon is formed by the other six corners. This trace is the drain of the upper switch and wire bonds reach out from the drain of the upper device. Only four perpendicular directions to the edges are assumed, with following additional constraints:

- Wire bond landing area is modeled as a square with edges of 2 mm. This landing spot should be inside the DBC boundaries.
- Wire bond originates from the device center and the maximum length is 12 mm. This limit may vary with different bonding machines.
- Electrical clearance needs to be kept between the bond spot and the positive trace polygon.
- Geometry clearance needs to be kept between the bond spot and the lower device.

As the second node of this tree model, as shown in this example, two branches originate from one of the first possible terminal location nodes. A positive trace is constructed with green edges and the potential left and down direction bond spots are invalid because of the distance to this trace. Initialed from any of those second nodes, the third brunch reaches out in Step 3.

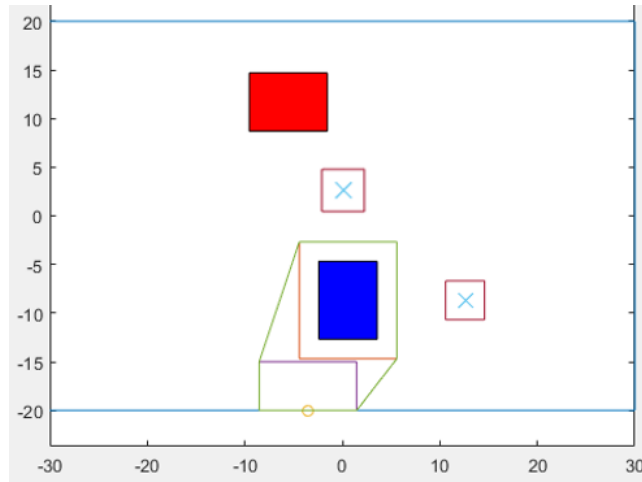


Fig. 6-5. Step 2: Positive Copper Trace and Upper Wire bond Location

Step 3: Phase Copper Trace

The phase copper is the largest copper trace of the DBC design. Functionally, it provides the electrical connection of drain (downside) of the lower switch, phase wire bond spot and the phase output terminal located on any edge of the DBC. Since the phase output has a negligible impact of the power loop extraction, and there should be always a race out to the edge, only the connection of phase wire bond and the lower device is considered here. For each possible bond spot, there should be always a shortest current path connecting to the lower switch, with the constraint:

- The path of current should keep the distance to the upper switch and the positive terminal edges larger than the electrical clearance.
- Direct connection is defined as the connection line segments are not cross with any clearance boundaries of other polarity domains.

If the wire bond location enables a direct connection, as shown in Fig. , the current path is straightforward.

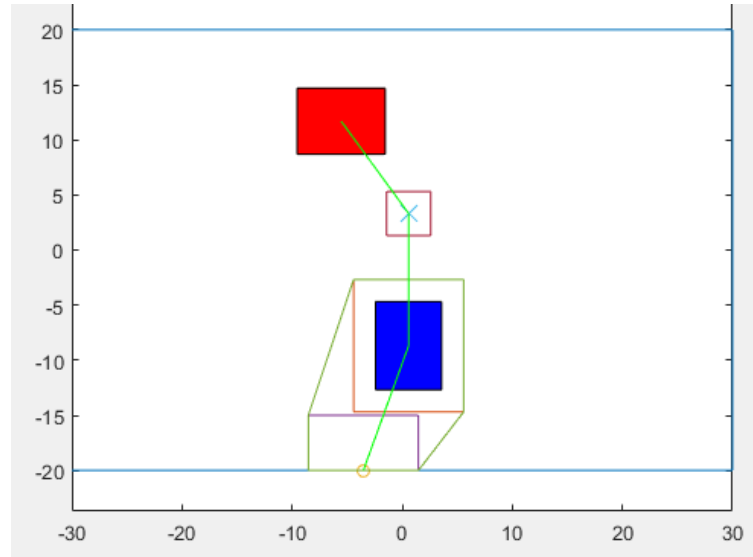


Fig. 6-6. The situation of the direct path

On the other hand, if the connection is not direct, a detour path is necessary for the current path. As illustrated in Fig. 6-7 if directly using line segment to connect the wire bond landing spot and the lower device, this line segment will cross with the clearance domain of the upper switch, as marked at the red cross. To keep enough clearance from upper devices, a detour path turning at the spot, marked as a star, is formed. The location of this spot is determined by the direction of the red cross point and clearance distance to the center of the device.

The set of green line segments presents partial of the current path origin from positive terminal and stop at the lower devices. Next step of this operation is the construction of phase copper trace. This copper trace is a polygon domain consisting phase wire bond landing spot, the lower device and the turning point if a detour path exists.

Both of the phase copper domains of two wire bond landing spots are illustrated in Fig. 6-8.

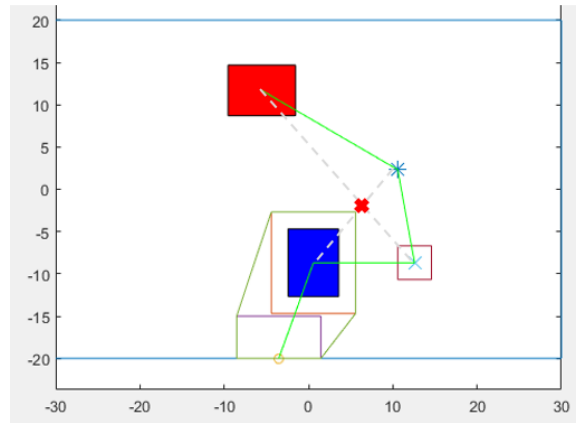


Fig. 6-7. The situation of the detour path

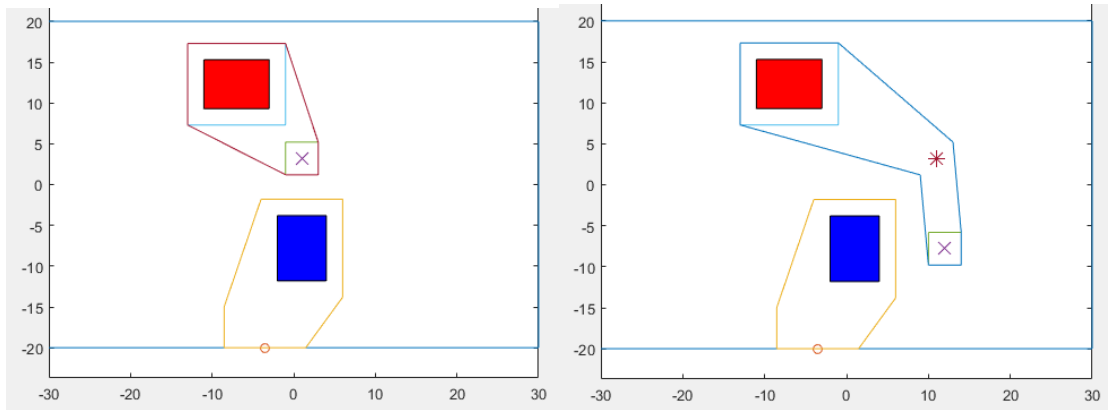


Fig. 6-8. Step 3: Phase Copper Trace

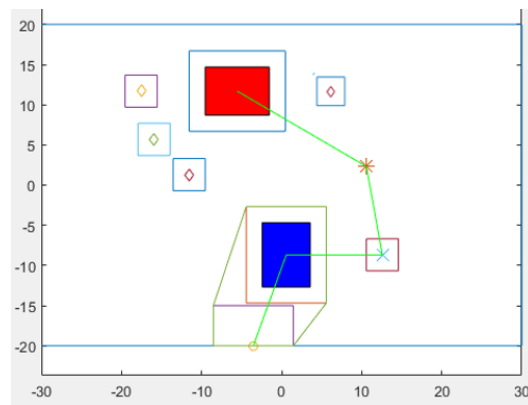


Fig. 6-9. Step 4: Lower Wire Bond Location

Step 4: Lower Wire Bond Location

As built so far, the phase copper trace has connected the drain of the upper device to the source of the lower device. The power loop then should continue to flow from through the lower device and connect to the negative bus terminal by wire bonds. Similar to the requirements of the upper wire bond, geometry constraints are listed as:

- Wire bond landing area is modeled as a square with edges of 2 mm. This landing spot should be inside the DBC boundaries.
- Wire bond originates from the device center and the maximum length is 12 mm. This limit may vary with different bonding machines.
- Electrical clearance needs to be kept between the bond spot and all other polarity domains.
- The angle between the last current path line segment and the new wire bond direction should be larger than 45 °to avoid sharp turning.

Since heavier constraints compared to the upper wire bond have been added, more possible wire bond directions are allowed at a step of 30 °.

Origin from one of the previous bifurcated node, three branches representing possible wire bond locations is plotted in Fig. 6-9.

Each of them can transfer to a new bifurcated node and reach out to the next brunch, which is the negative terminal location.

Step 5: Negative Terminal and Closed Power Loop

As the last components of the power loop, the negative terminal location will eventually determine the parasitic values. As the state of art, two major types of technologies are used for bus bars design, as called laminated bus bar solution and decoupling caps. As the basic

approach of layout design, the decoupling caps solution is assumed as its ease of assembly. Future work could include the availability of using laminated bus bar. Similar to the positive terminals, all locations of the negative terminal are located at the cross points by the line through the lower device center and the DBC edges with a swept-step of 10°. Only locations meet all following constraints can be selected as the potential negative terminals:

- As a planer DBC structure, terminals land on the boundaries only.
- Terminals are modeled as a rectangle of 10mm×5mm
- The separation distance between two terminals is shorter than half of the DBC diagonal distance. This constraint ensures the shortcut path of the decoupling cap.
- Boundaries of terminal need to be kept away from all other components except the lower wire bond landing spot larger than B_Clearance+E_Clearance.
- No crossed current path is allowed, and the negative copper trace is formed by a lower wire bond landing spot, a negative terminal, and a potential detour spot.
- Detour path is similarly defined as that of Step 3.
- Decoupling caps located at the edges of DBC. Thus, a closed power loop has to include some of the segments landing on the edges.

Following the instructions and constraints, all possible terminals constructing all power loops are shown in Fig. 6-10.

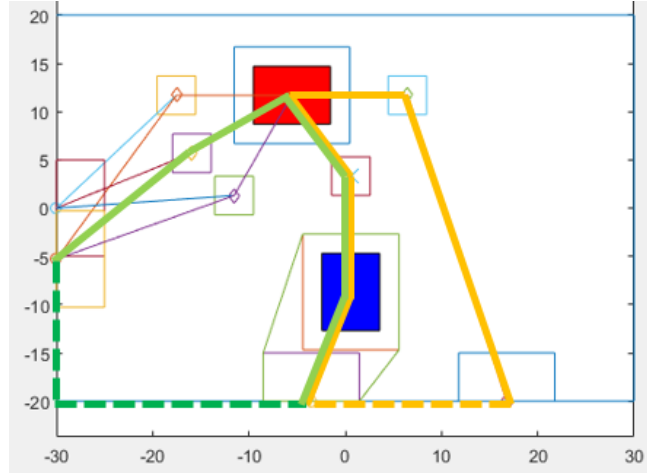


Fig. 6-10. Step 5: Negative terminal and closed power loop

As marked, two example loops are colored in green and orange. The solid line represents the current path on DBA and the dashed line represent the decoupling loop of the high frequency switching current. After this Branch and bound algorithm-based extraction, hundreds of power loop candidates are obtained based on this device layout design. Fitness will be assigned based on a parasitic parameter of each candidate.

6.3.3.Parasitic elements calculation

FEA simulations generally are both time-consuming and costly to extract the parasitic elements of the complex routing design of layouts. Considering the enumeration of candidate solutions of the BB algorithm, each layout design could take hours for parasitic extraction using FEA tools. Instead, a simplified and fast parasitic elements model should be constructed when the speed of evaluation is critical. Thus, as a simplification, no matter which media or what area of the cross-section conducting current, a uniform cross-section

area is assumed. The well-known formula of the single-turn rectangular loop inductance expressed as Eq. 6-2 is used to estimate the loop inductance value.

$$L = \frac{\mu_0}{\pi} [-2(w + l) + 2\sqrt{w^2 + l^2} + l \cdot \ln\left(\frac{w}{l + \sqrt{w^2 + l^2}}\right) + w \cdot \ln\left(\frac{l}{w + \sqrt{w^2 + l^2}}\right) + l \cdot \ln\left(\frac{w}{d}\right) + w \cdot \ln\left(\frac{l}{d}\right)] \times 10^{-3} \quad \text{Eq. 6-2}$$

Where w is the width(mm) and l is the length(mm) of the rectangular power loop, d is the cross-section diameter(mm) which is much smaller than w and l . μ_0 is the vacuum permeability. However, this model is approximated based on a well-defined rectangle current loop, which is normally hard to find in a power module. Since this optimization needs accrete parameters to ensure optimization quality, especially when approaching to convergence that improvements became slighter. Instead, an alternative method using fitted equation as the reference is proposed in this Chapter.

As what interpreted from analytical equations, the parasitic inductance of a loop major depends on two parameters, i.e. power loop area S and the power loop length L . Intuitively, the fitted equation should be a function of such two parameters, as initially guessed:

$$L_{Parasitic} = A_1 S + A_2 \cdot \ln(S) + A_3 \cdot S \cdot \ln(S) + A_4 \cdot L + A_5 \cdot \ln(L) + A_6 \cdot L \cdot \ln(L) + A_7 \quad \text{Eq. 6-3}$$

Where coefficients A_1 to A_7 are fitted parameters that can result the in minimum error for all possible cases. Values of A_1 to A_7 are calculated based on a set of Q3D FEA data. Randomly, 100 individuals are initialized following the construction steps and imported to the Q3D of Ansys to extract the AC parasitic inductance at a frequency of 5Mhz. Data of parasitic inductance along with the geometry prolife such as the loop area and the loop length are assigned to each design and input to the database.

With all data of database updated, parameters of Eq. 6-3 are fitted using Genetic Algorithm as the tool. The fitness function of the genetic algorithm is set to be the total error by summing up errors of all design cases. The smaller fitness one set of paraments can get, the more accurate it can model the parasitic inductance. As shown in Table 6-2, the fitted parameters converged after 1500 iteration. It is interesting to notice that the parasitic inductance of a power loop is highly dependent on the loop area which is A_1 and has negligible relation to the loop length.

Table 6-2. Fitted Parameters

A_1	A_2	A_3	A_4	A_5	A_6	A_7
2.518	9.23e-16	1.29e-15	0.0125	7.33e-16	9.04e-16	8.32e-16

Thus, the parasitic inductance of any design case can be modeled as with a high accuracy.

$$L_{Parasitic} = 2.52 \cdot S(cm^2) + 0.01 \cdot L(cm) \quad \text{Eq. 6-4}$$

7. Operation Domain

7.1. OPTIMIZATION TARGET

The third domain of this multi-objective optimization flowchart is the switching frequency iteration loop, as shown in Fig. 7-1. In this domain, the target is to locate the optimal switching frequency that scores highest while is kept under the constraints.

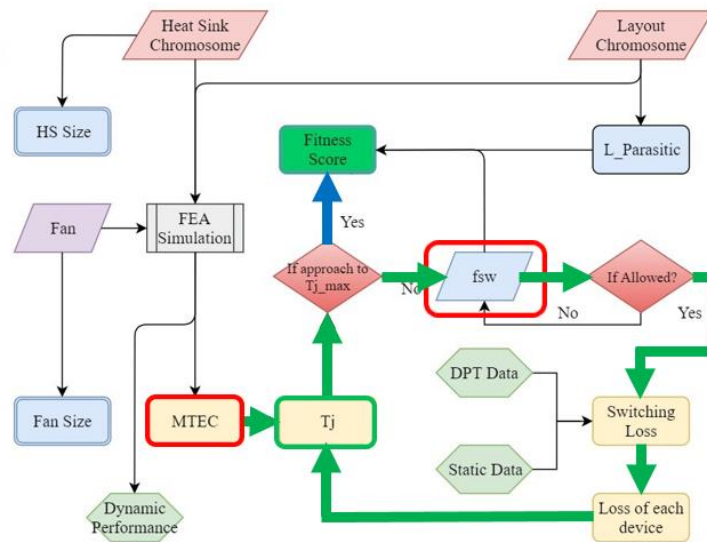


Fig. 7-1. Switching frequency iteration loop

As it was introduced in previous chapters, switching frequency will highly impact the overall passive components parameters, so as the volume and the weight of them. Generally speaking, the higher frequency one converter can switch, the lower requirements on the design of passive components, especially on the filters. However, because of the tradeoff existing between switching frequency and the switching loss, a too unduly high switching

frequency will pose a significant thermal stress on the power module. As the switching loss calculated in Eq. 7-1, a direct proportion relation exists between the switching loss per transient and the switching loss of each active device. And the coefficient is the switching frequency.

$$P_{sw} = (E_{on} + E_{off}) \times f_{sw} \quad \text{Eq. 7-1}$$

Moreover, the switching frequency is also limited by the switching speed, which furthermore, is limited by the power loop parasitic inductance. Thus, an iteration loop as marked in the green of Fig. 7-1 is proposed to approach the optimal operation point in terms of the switching frequency. For each switching frequency, the loop will update the junction temperature if this switching frequency is allowed by the switching speed limit. A criterion determining if the junction temperature reached the device temperature limit is then made and feedback to the switching frequency adjustment for either increase or decrease the switching frequency to meet the limit.

Since the huge time consumption of FEA simulation, it will take forever to iterate in this loop if the junction temperature is evaluated by FEA. Thus, the junction temperature should be estimated using an approximated mathematic-based thermal model for fast speed. This model has been widely used in conventional thermal design method, as named thermal equivalent circuit introduced in the background section. This method has been widely accepted for rough thermal design, as a parameter to present heat sink performance. However, as this application, the precise model is necessary for an accurate operation parameter selection. Several drawbacks of this TEC model impede the implementation in the iteration loop. Moreover, as a multi-chip module, loss of each component varies significant and different relationship to the switching frequency. Thus, a modified TEC

model is first introduced in this chapter. Then, a GA based construction method of the parameters of this TEC through the already built interface is developed. A design case is then illustrated to perform this loop iteration.

7.2. CONVENTIONAL DESIGN METHOD

Since the detailed introduction has been listed in the background section, a rough review of the conventional thermal design process will be performed. This method is majorly based on the steady state thermal equivalent circuit as

$$T_j = T_A + (R_{thj-b} + R_{thb-h} + R_{thHeat\ Sink}) \times P_t \quad \text{Eq. 7-2}$$

where T_j is the junction temperature, T_A is the ambient temperature, R_{thj-b} is the junction to baseplate thermal resistance, R_{thb-h} is the baseplate to heatsink thermal resistance, $R_{thHeat\ Sink}$ is the thermal resistance value of the heatsink and P_t is the power loss input to the cooling system.

Rearranging Eq. 7-2 into Eq. 7-3, the heatsink selection criterion is based on:

$$R_{thHeat\ Sink} < \frac{T_{j_max} - T_A}{P_t} - R_{thj-b} - R_{thb-h} \quad \text{Eq. 7-3}$$

The value of $R_{thHeat\ Sink}$, is obtained from the manufacturer datasheet as a function of the flow rate as shown in Fig. 7-2.

However, the definition of each component value is vague. Taking an FEA thermal analysis of a commercial SiC module as an example, the thermal related data sheet is shown in Table 7-1. The thermal profile of the SiC module is plotted in different views and layers.

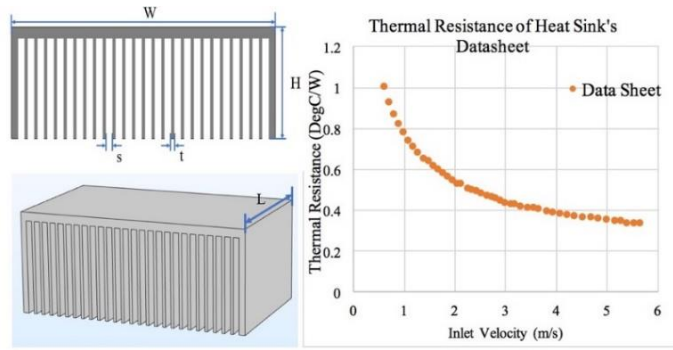


Fig. 7-2. Datasheet of the commercially available heat sink

Table 7-1. Datasheet of a commercial module

Symbol	Parameter	Typ.	Unit
R_{thj-cM}	Thermal Resistance Junction-to-Case for MOSFET	0.1	$^{\circ}\text{C}/\text{W}$
R_{thj-cD}	Thermal Resistance Junction-to-Case for Diode	0.11	$^{\circ}\text{C}/\text{W}$

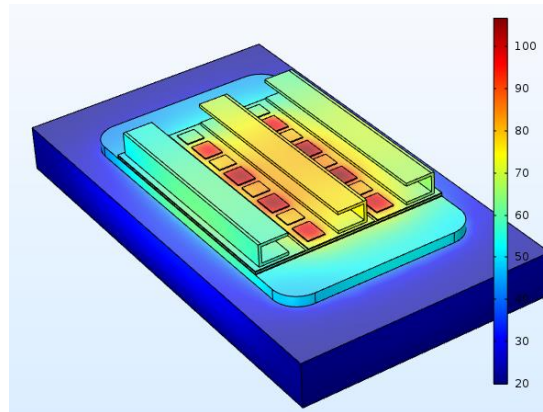


Fig. 7-3(a). FEA thermal simulation profile

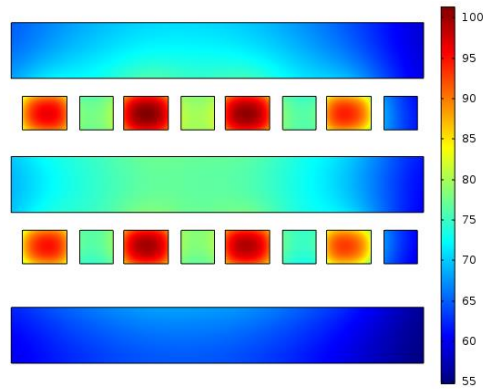


Fig. 7-3(b). Junction temperature profile

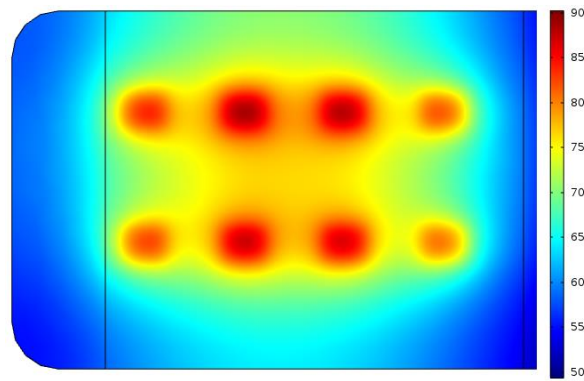


Fig. 7-3(c). Case temperature profile

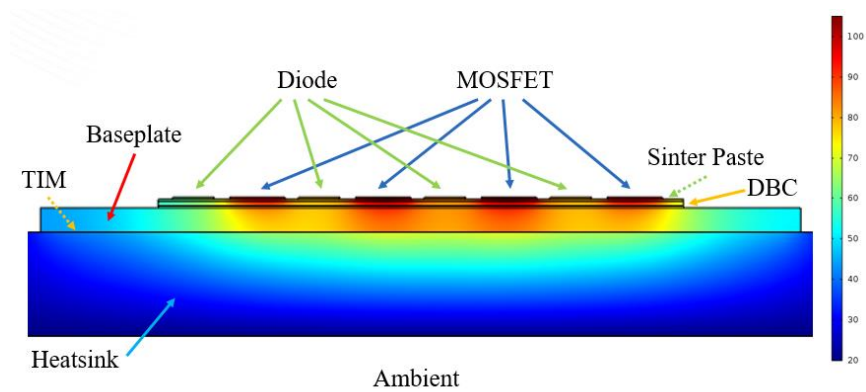


Fig. 7-3(d). Vertical cross-section view of the thermal profile

In this datasheet, a better thermal model by separating the thermal resistance of Diode and MOSFET is provided. Two parameters, namely, R_{thj-cM} and R_{thj-cD} represent the local thermal resistances. For example, the Thermal Resistance of Junction-to-Case for MOSFET is calculated using the equation:

$$R_{thj-c} = \frac{T_{j_MOSFET} - T_{c_MOSFET}}{P} \quad \text{Eq. 7-4}$$

Reading from both horizontal and vertical cross-section temperature profiles, there are eight sets of the temperature of T_{j_MOSFET} and T_{c_MOSFET} . Also, the power loss distribution of each device varies due to modulation schematics. Since all variables in the right-hand side of the equation are not unique, modeling the thermal performance using one set of parameters are not reliable. Multiple drawbacks are introduced as analyzed in following study cases.

7.3. DRAWBACKS ANALYSIS

7.3.1. Case 1: Impacts of footprint ratio

A group of identical power modules with different heat sources have been simulated. Assuming the heat sources are different size die, a footprint ratio is defined as:

$$\text{Footprint ratio} = \text{Die Area} / \text{Cross-section area of the heat sink} \quad \text{Eq. 7-5}$$

Thermal resistance profile comparisons among datasheet, the ratio of 0.9 and ratio of 0.2 are shown in Fig. 7-4, where reducing the heat source footprint ratio from 0.9 to 0.2, the thermal resistance of the junction to ambient is doubled with the same inlet flow of 6m/s. The thermal resistance profile for the ratio of 0.9 almost matches the profile from the

manufacturer's datasheet. It confirms the assumption that the datasheet of the heat sink is plotted based on the analysis of a large heat source.

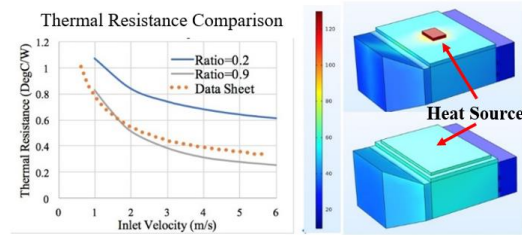


Fig. 7-4. Thermal resistance comparison of footprint ratio differences

7.3.2. Case 2: Impacts of thermal coupling

This case is studied to illustrate the impact of thermal coupling between the semiconductor die, which was briefly mentioned in [192, 193]. Impacts of the thermal coupling versus the separation distance have been tested in this paper for both perpendicular and parallel air flow directions. The perpendicular thermal coupling results are shown in Fig. 7-5, the maximum junction temperature reduced from 82 °C to 70 °C by separating the devices further. This example shows that the thermal coupling effect can introduce additional 12 °C, which is as large as 20% extra junction temperature.

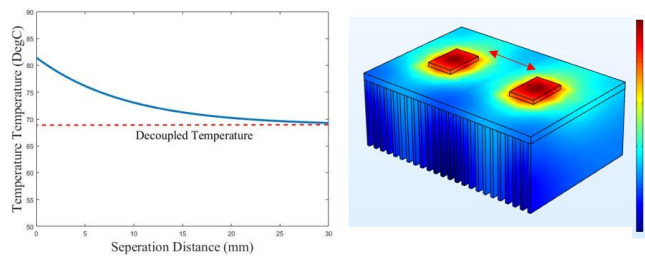


Fig. 7-5. Impact of perpendicular thermal coupling

7.3.3. Case 3: Impacts of the heat source location

Another impact related to the device layout is the location of devices. As shown in the junction temperature profiles of a single die placed in different locations are evaluated. This case is illustrated to prove that the vertical thermal resistance of a power module is not constant but a function of the location.

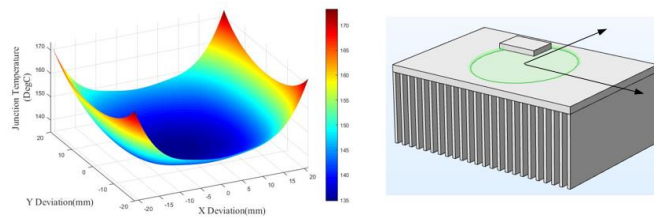


Fig. 7-6(a). The temperature profile of different locations (b) Allowed design area

By changing the device location of the module with a footprint ratio of 0.2 shown in the Case 1, the junction temperature of the device varies from 130 °C to 175 °C. As a design limit of 140 °C, the center of the device can be only placed inside the green domain.

7.3.4. Case 4: Overall impacts

Combining the impacts from the previous cases, both worst-case and best-case scenarios with the same power loss are constructed to illustrate the significant impacts of the heat dissipation profile. The best case is using two devices with large footprints with large enough separation and locating them at the center of the heat sink. The worst case is when devices with small footprints are put close to each other at the corner of the heat sink. For

all other possible layout designs, their junction temperatures should be in between these two extreme cases.

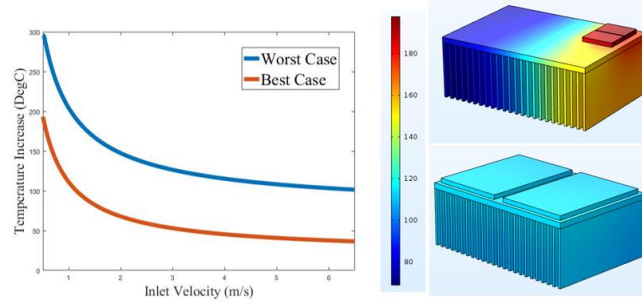


Fig. 7-7. Comparison of overall impacts

As the results shown in Fig. 7-7, take the same flow speed of 6 m/s, the junction temperature increases in the worst-case scenario, 100 °C is 200% higher than the best-case heat dissipation profile, 30 °C. However, without considering these scenarios, a “safe design” using the conventional method can lead to thermal failure. The impacts should be considered in the future power module design.

7.4. PROPOSED THERMAL MODEL

Previous comparisons indicate that the heat dissipation layout has to be considered in the design to avoid the thermal issues. But the layout impact has been overlooked in the one-dimensional TEC model. A modified thermal modeling is proposed in this paper based on the results of finite element analysis (FEA). For automation purposes, the thermal model construction with the same co-simulation loop interface used in **Chapter V**.

As a design example, a random heat sink with two devices on top is built in COMSOL, as shown in Fig. 7-8. This design has gone through the Thermal Domain and the Parasitic Domain and comes to the Operation Domain for the fittest switching frequency point.

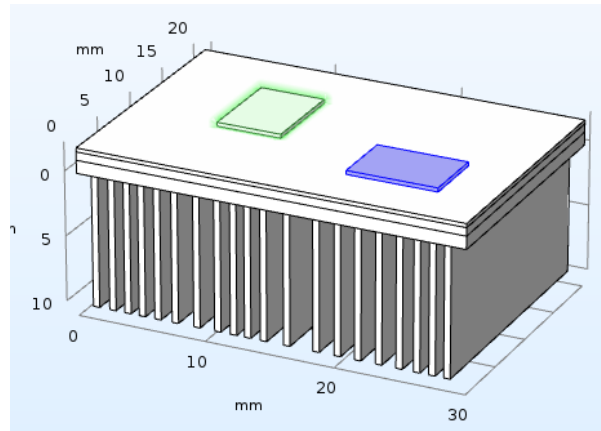


Fig. 7-8. The model of the heat sink with two heat sources

7.4.1. Modified Finite Element Analysis

Since advanced modeling details need to be extracted from the FEA simulation, at least two independent sets of test data should be extracted as input. To save on computation time, special setting adjustments have been done for the simulation with multiple data inputs. Assuming the temperature does not affect fluid material property significantly, a partial decoupling FEA method is reasonable to apply so that NITF (Non-Isothermal Flow) study can be used to solve for two physics interfaces (Laminar flow and heat transfer) sequentially.

The first step focuses on the flow profile only. The flow distribution is evaluated regardless of the thermal profile. That means, the temperature dependent parameters such

as density and dynamic viscosity are represented by $\rho(T_{\text{ref}})$ and $\mu(T_{\text{ref}})$ and are treated as constant values.

Next step is using the previous flow distribution as the initial solution to solve for temperature profile. Meanwhile, the temperature gradient change of the flow is updated through the Multiphysics NITF interface.

With this approach, it is much more efficient to evaluate case with varying heat source parameters. For two sets of data, a sequent auxiliary sweep is set. This decoupled with a two-step study essentially reduces the total computation time from 26min 18s of the fully coupled model to 4min 8s. At the same time, the additional error introduced by decoupling approach is no larger than 2 °C, which is about 3%.

Applying this method and by flipping the power loss profiles of two devices from [110W, 10W] to [10W, 110W], the junction temperature of two devices are evaluated in COMSOL as shown in Table 7-2, and the parameters are reported to MATLAB through the co-simulation loop for construction of the TEC model.

Table 7-2. Simulation results of two sets of data

Loss1(W)	Loss2(W)	T_J Device1(°C)	T_J Device2(°C)
10	110	72.658	172.02
110	10	157.91	73.704

7.4.2. Construction of Steady-State Thermal Equivalent Circuit

Thermal equivalent circuit, as a simplified electrical RC model, has been used for decades to estimate the steady-state thermal performance of a power circuit where heat flow is represented by the current, temperatures are represented by voltages. However, the accuracy of the estimation is highly dependent on the selected model. Several approaches TEC are compared in this section.

1. One-dimensional circuit modeling

1D-TEC is constructed based on the one-dimensional circuit, as shown in Fig. 7-9. This is the most common and simple model. A series of resistances represent the thermal impedances along the one-dimensional vertical direction.

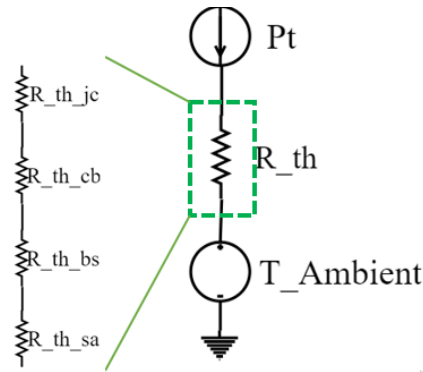


Fig. 7-9. 1D-TEC modeling

R_{th} is calculated as

$$R_{th} = (T_{jmax} - T_A)/P_t \quad \text{Eq. 7-6}$$

The thermal resistance value used in the following comparison is the average R_{th} values of two sets results. In this example, the R_{th} is calculated as 1.2 °C/W.

2. Two-dimensional decoupled circuit modeling

2D-TEC is constructed in a more realistic way, which is commonly seen in a power module datasheet. For example, datasheet of an IGBT power module contains two thermal resistance values, named as $R_{th(j-c)Q}$ referring to the freewheeling diode (FWD) part of the thermal resistance and $R_{th(j-c)R}$ referring to the IGBT part of the thermal resistance as shown in Fig. 7-10. In this model, the “location dependent discrete devices” concept has been considered. But the impacts between devices are not modelled.

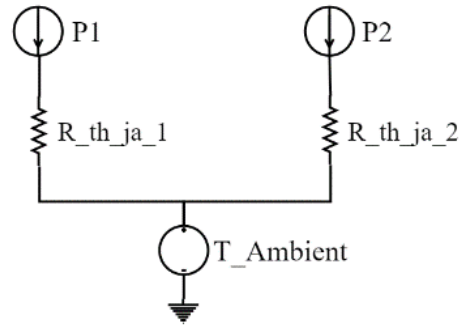


Fig. 7-10. 2D-TEC decoupled modeling

Parameters of the TEC are evaluated as:

$$R_{th1} = 1.38^{\circ}C/W \text{ and } R_{th2} = 1.25^{\circ}C/W \quad \text{Eq. 7-7}$$

3. Two-dimensional coupled circuit modeling

Different from the previous model, the proposed modified thermal equivalent circuit (MTEC) constructed in this paper considers the thermal coupling issues. As shown in Fig. 7-11, an additional resistance representing the horizontal heat transfer performance is included.

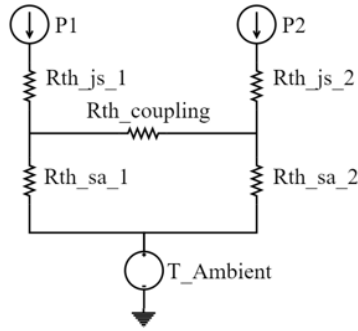


Fig. 7-11. 2D-TEC coupled modeling

There are five parameters to be evaluated though. To further simplify the circuit, a Delta – Y transformation leads to a simpler circuit as shown in Fig. 7-12.

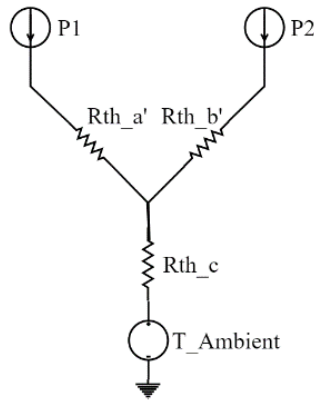


Fig. 7-12. Modified TEC (MTEC)

The junction temperatures of the model can be expressed as the net voltages at the current source input point. Though it is solvable with analytical approaches, to more efficiently acquire the parameters of the resistance network, a Genetic Algorithm is applied as the solution approach tool. For more detailed Genetic Algorithm information, please

refer to the previous paper published in 2016 [9]. Parameters of the three resistances initialized ranging between $0\text{ }^{\circ}\text{C}/\text{W}$ and $2\text{ }^{\circ}\text{C}/\text{W}$ and the fitness function is defined as the absolute error value of the estimated junction temperatures compared to the simulated results. Using the input parameter sets in the sequent of [P11, P21, T11, T21, P21, P22, T21, T22], as shown in Table 7-2. Simulation results of two sets of data, the output of the Genetic Algorithm converged after 210 iterations to [0.8538, 0.9817, 0.3595]. Those are the values of [R_{th_a} , R_{th_b} , R_{th_c}].

7.4.3. Comparison of Steady-State Thermal Equivalent Circuit

Three types of thermal circuit models have been built and compared to COMSOL based on varying losses from 10W to 110W for two devices. The junction temperatures for all operating points are recorded for comparison purposes. The estimated junction temperatures of the devices at these operating points are calculated based on the three modeling methods described earlier. The total deviation between estimation and the simulation results of two devices determines the performance, where higher deviation means worse performance for the model.

The performances of all three models are presented in Fig. 7-13-15, where P1 and P2 are the input power of devices and the vertical axis represents deviation which is the measure of performance.

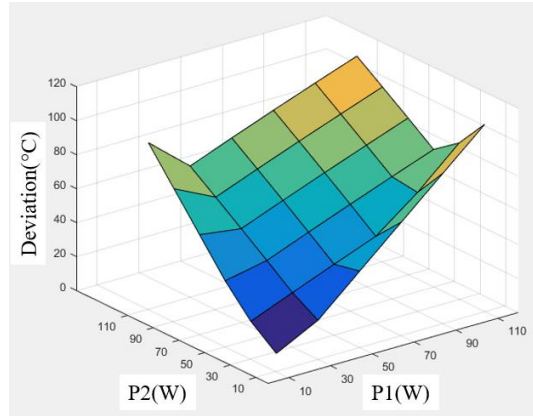


Fig. 7-13. Performance of the 1D-TEC modeling

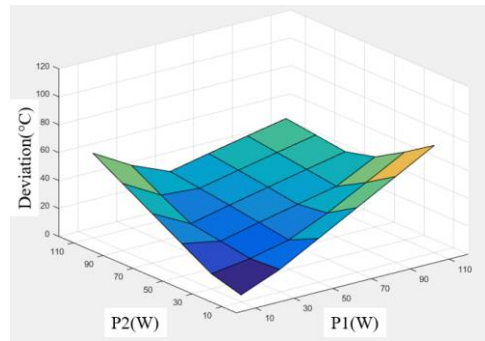


Fig. 7-14. Performance of the 2D-TEC modeling

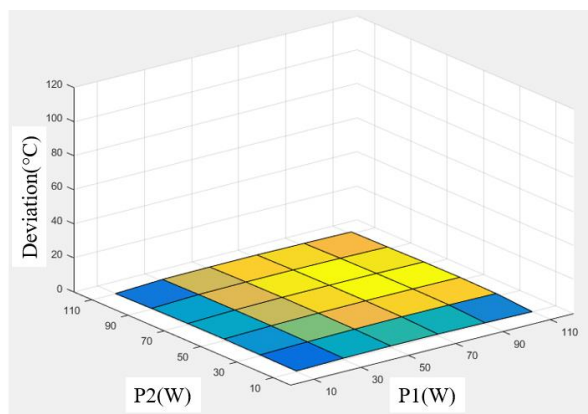


Fig. 7-15. Performance of MTEC

It can be observed that the one-dimensional approach (Fig. 7-13) has a significantly larger deviation for the application of multiple devices. The second model (Fig. 7-14) performed fairly well when the power input mismatch of two devices is small but performance got worse with the increased mismatch. MTEC model (Fig. 7-15) showed almost no error compared to the COMSOL simulation results. The MTEC modeling method perfectly represents the thermal features of two device modules.

8. Multi-Objective Optimization Case

With all domains developed in the previous chapters, the flowchart proposed in **Chapter 3** is completed as a closed-loop iterative optimization. An optimization case is illustrated in this chapter for the design of a phase-leg module used in the three-phase inverter. The optimized result is compared to the design case with similar specs using conventional design approaches proposed by CPES in [116].

8.1. DESIGN SPECS

The power module design specs in this chapter inherit the specs in used **Chapter 4**, where an “Alpha Version” SiC-based solar inverter was developed. Modules of “Alpha Version” inverter are designed as 1.7KV, 100A phase-leg modules with a face-to-face configuration. Since this design is focused on thermal performance only, the power loop inside the module was not regarded as an optimization parameter.

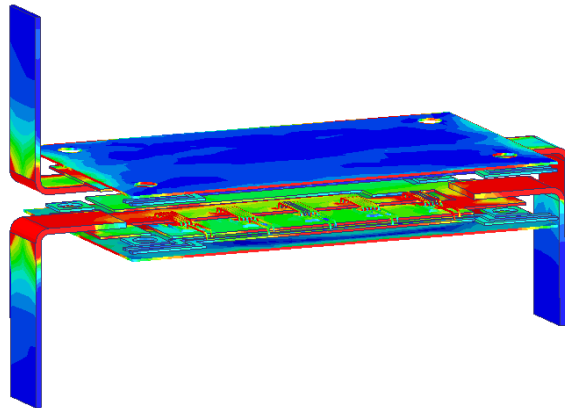


Fig. 8-1. Q3D simulation result of “Alpha version” designed power module

As simulated in Q3D, around 20 nH parasitic inductance was introduced by caused this large power loop formed by two pieces of DBC boards and the interconnection leads between them. This large parasitic inductance resulted in a huge voltage spike during the test and the switching speed, as well as the switching frequency, had to be limited to maintain a safe operation.

As a revision design case illustrated in this Chapter, “Gamma Version” module, is developed with the considerations of all major domains illustrated in previous chapters. Optimization method on individual domain keeps the same as what has been proposed, however, the evaluation as a multi-objective process is modified using the configuration as presented in Fig. 4-2. The spec of the module to be designed comes with a SiC-based phase-leg schematic. The rated DC voltage is 1KV and one-third of 50kW as the rated power level. As mentioned in Chapter V, Alpha version of the module was over-designed as a prototype illustration while the Gamma version will be designed with optimized parameters.

Moreover, after the two-year development of semiconductor, SiC MOSFETs, and Diodes used in this application get a higher current rating with the same voltage rating level maintained. Thus, instead of five MOSFETs and three Diodes, only two paralleled 1.7 kV SiC MOSFETs and one freewheeling 1.7 kV SiC Diode will be put as a switch position. Based on the similar calculation method, as described in Chapter IV, loss of each device is estimated based on the device characterizations, modulation and the other parameters are kept the same

On state resistance of a single MOSFET at 150°C is 36.53 mΩ and 18.26 mΩ of the when paralleling two switches. The conduction loss of the module is 66.1W as a constant

during the optimization. The switching loss, on the other hand, depends on the switching frequency and the energy loss per switch is calculated as 673.35uJ.

8.2. CONVENTIONAL DESIGN

One similar design case, as simulated in with the same number of devices is picked as a comparison. Details of such design have been illustrated in [116] by CPES, and it will be called as “referred design” in the later text. Similar layout approach can be also noticed in most of the commercially available power module, like the Rohm’s design analyzed in {Ren, 2017 #108}. The parasitic inductance of this comparison case is simulated as 16.9 nH based on the AC current of 50 MHz.

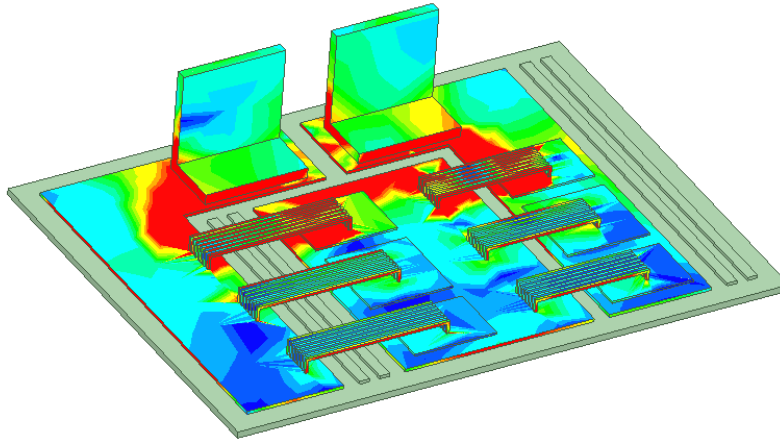


Fig. 8-2. Conventionally designed substrate for comparison

Since the rated parameters of the referred design are not identical to what used in this Chapter, devices are replaced with the same devices used in this Chapter to eliminate the

differences between two cases except the packaging designs Footprint dimension of DBC are 55mm×41mm as of both cases.

Because the heat sink is not involved in the reference, a commercially available heat sink manufactured by Aavid is picked for the referred design using the conventional thermal resistance-based method. The dimensions of the heat sinks are 73.25 mm×50.8mm×32mm, which is 117.6 cm³.

Though the number of devices is not identical for the “Alpha” and “Gamma” designs, the evaluation of “Alpha version” is still listed as a comparison reference.

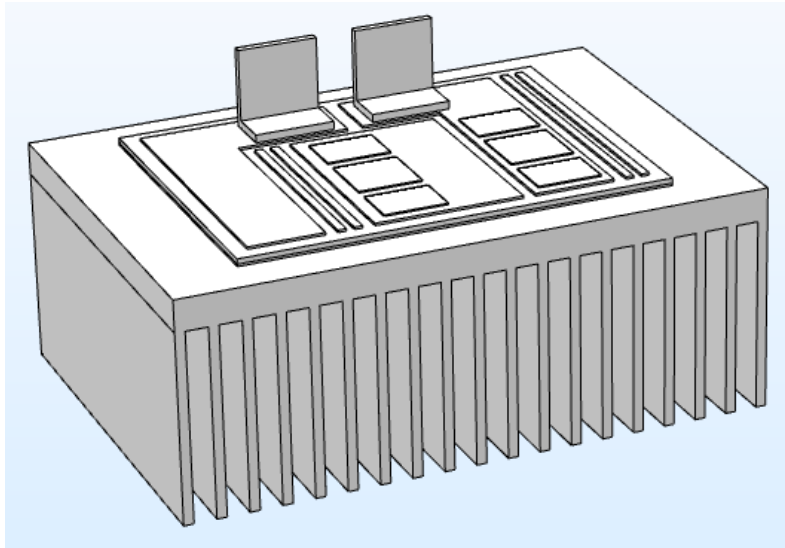


Fig. 8-3. Power module with heat sink designed for comparison

8.3. OPTIMIZATION AND RESULTS

Taking the design specs as the input, the phase-leg module is developed. As a multi-objective optimization problem, the overall fitness value includes the parameters origin

from all three domains, i.e., heat sink volume, parasitic inductance and the maximum switching frequency. As the general approach, the optimized result should get benefits from a small parasitic inductance, small heat sink volume and a high switching frequency. Straightforwardly, using these three performances to evaluate the fitness value, the fitness function is constructed as:

$$Fitness = \frac{f_{SW_Max}}{L_{Parasitic} \times V_{Heatsink}} \quad \text{Eq. 8-1}$$

Where the $L_{Parasitic}$ is parasitic inductance that calculated based on the power loop area S and the power loop length L as formulated in Eq. 5-4 of Chapter V.

$V_{Heatsink}$ is calculated by the minimum outer cuboid box that can fit the heat sink as

$$Volume = Length \times Width \times Height \quad \text{Eq. 8-2}$$

f_{SW_Max} is determined by the MTEC with the maximum junction temperature limited to 150 °C. The switching loss of each active device is updated with the change in switching frequency as Eq. 8-3 while the conduction loss of each device keeps constant.

$$P_{sw} = 673.35uJ \times f_{sw} \quad \text{Eq. 8-3}$$

The optimization target is to achieve the design with the highest fitness score. Noting that the fitness function used in this chapter is an approximated model by considering only the impact of each parameter. Even though the importance of each parameter is not identical, for example, the $V_{Heatsink}$ has directly impact on the total volume while $L_{Parasitic}$ is an intermediate parameter, the weight of all parameters are regarded equally as a simplification. In a specific application, weight factor can be adjusted by adding power function to each parameter. For a more precise model, the weighted factor of each parameter should be in a more logical way, with the construction of the larger optimization

scope, In that scope, all output should be volume/ weight-related parameters, and the fitness value is the sum of all volume contributors with the considerations of the filling factor. This fitness adjustment is a future work illustrated in the last chapter.

With the design approaches introduced in the previous chapters, the optimization started with a population of 51 individuals and stopped after 75 iterations where little improvement can be achieved within the continuous 20 iterations. The optimization is processed based on a workstation with a twelve-core 3.5 GHz processor and 40GB of RAM. Totally computation time before approaching convergence took about 7 days.

To present the convergence process, some intermediate data points that can present the change of all four performances are recorded during the optimization as listed in Fig. 8-4. Eight columns of data are presented. The first four columns of data (A-D) origin from the evaluated performance parameters and the next four columns of data (E-H) are calculated based on the first four columns of data. The last column I is the fitness value comes from Eq. 8-1. Column A is the number of individuals that the multi-domain evaluation flowchart has evaluated. Column E is based on A that roughly present the location of this individual in the convergence, as the iteration number. Column B, C, D individually represent the evaluated parameters, i.e. the power loop area, the junction temperature before adjusting the switching frequency and the heat sink outer box volume. Correspondingly, parameters in column F, G, and H represent the modified and normalized parameters contributing to the overall fitness value, which is the product of such three parameters.

Convergence plot as shown in Fig. 8-5 visually indicates the evolution of each domain and the overall fitness converging progress.

The optimized result after 75 iterations is plotted in Fig. 8-6.

	A	B	C	D	E	F	G	H	I
1	Evaluation	A_loop(mm)	Tj(degC)	V(cm3)	Iteration	Parasitic	Volume	Frequency	Fitness
2	2	823.2768	195.3265	178.3	0.1	1	1	1.000012	1.000012
3	3	593.9629	133.7974	179.2	0.15	1.386074	0.994978	1.894376	2.612558
4	5	451.6816	140.0637	166.2	0.25	1.822693	1.072804	1.736234	3.395017
5	62	451.6816	131.7018	169.3	3.1	1.822693	1.05316	1.953892	3.750666
6	190	384.8611	135.185	155.8	9.5	2.139153	1.144416	1.856923	4.545897
7	191	386.0243	134.2972	154.8	9.55	2.132707	1.151809	1.880713	4.619916
8	204	386.0243	132.2516	150.1	10.2	2.132707	1.187875	1.937919	4.909501
9	278	386.0243	130.6623	153.2	13.9	2.132707	1.163838	1.984824	4.926584
10	301	393.1498	128.8105	154.1	15.05	2.094054	1.157041	2.042424	4.948602
11	353	367.2326	130.7726	137.2	17.65	2.24184	1.299563	1.981496	5.772913
12	384	367.2326	128.1908	139.1	19.2	2.24184	1.281812	2.062454	5.926703
13	449	372.2326	127.4821	137.6	22.45	2.211727	1.295785	2.085847	5.977876
14	481	348.3592	133.4635	130.5	24.05	2.363299	1.366284	1.903615	6.14665
15	588	372.2326	124.65	136.5	29.4	2.211727	1.306227	2.18488	6.312158
16	593	348.3753	127.6699	127.7	29.65	2.363189	1.396241	2.079597	6.861801
17	772	348.3753	126.3562	127.2	38.6	2.363189	1.40173	2.124123	7.036269
18	829	348.3753	122.9502	130.3	41.45	2.363189	1.368381	2.248968	7.272582
19	837	343.3636	125.3615	124.4	41.85	2.397682	1.43328	2.159127	7.419945
20	846	343.3636	124.2355	124.4	42.3	2.397682	1.43328	2.252824	7.741941
21	1069	340.5731	122.851	125.4	53.45	2.417328	1.42185	2.252824	7.743131
22	1077	357.1	118.3	129.2	53.85	2.305452	1.380031	2.44518	7.779573
23	1327	344.4572	121.4945	126.3	66.35	2.39007	1.411718	2.306917	7.78378
24	1338	344.4572	121.4945	125.9	66.9	2.39007	1.416203	2.306917	7.80851
25	1370	340.5731	124.5632	120.7	68.5	2.417328	1.477216	2.188064	7.813394
26	1377	339.3416	124.5523	120.7	68.85	2.4261	1.477216	2.188465	7.843185
27	1441	339.2731	124.5512	120.7	72.05	2.42659	1.477216	2.188505	7.844913

Fig. 8-4. Intermediate data during convergence

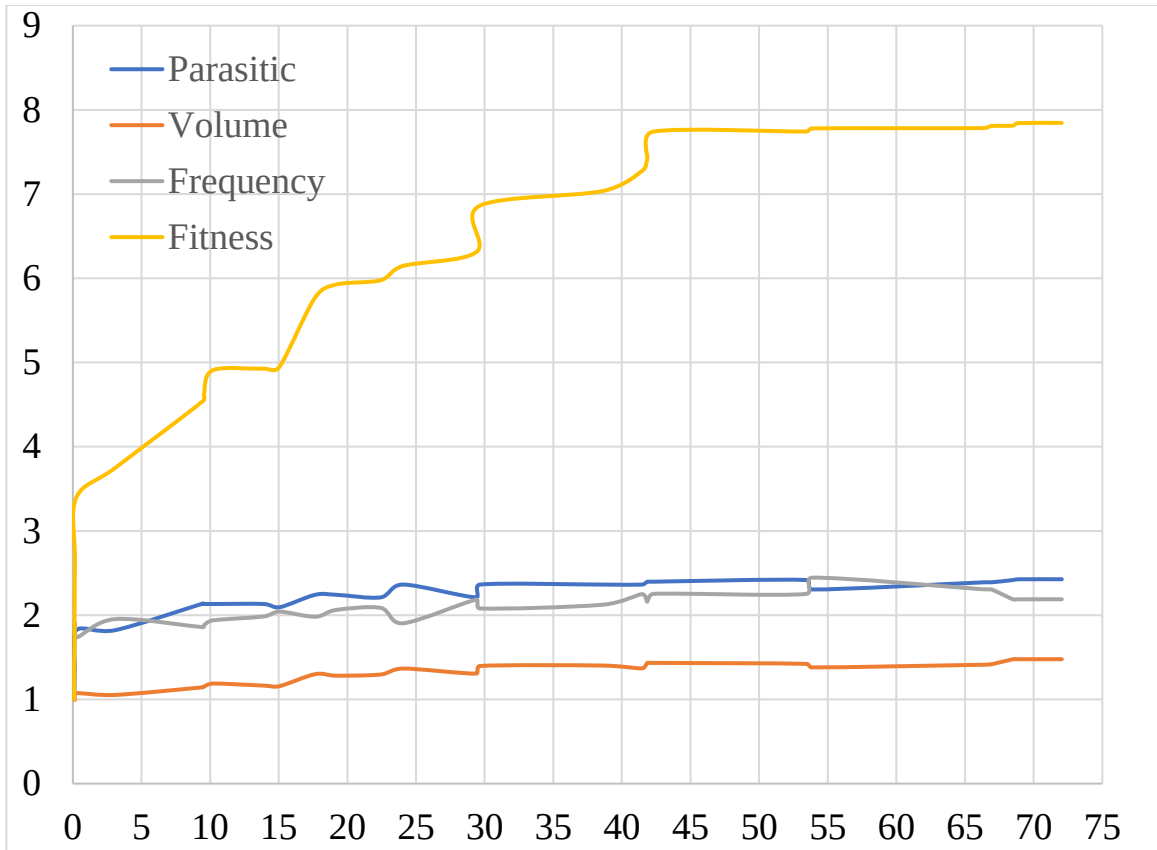


Fig. 8-5. Evolution progress of each sub-domain and the overall fitness value

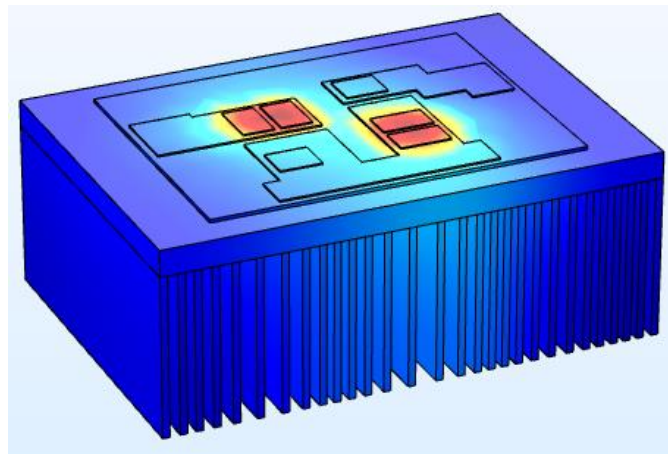


Fig. 8-6. Optimized heat sink design

Fitness value of this design is 7.845, where parasitic domain scores 2.42, as of the loop inductance of 8.54 nH; thermal domains scores 1.477, as of the volume of the module is 120.7 cm³; operation domains scores 2.188, as of the switching frequency of 77.3 kHz.

8.4. COMPARISONS AND CONCLUSION

As constructed, the comparison design is evaluated using the same method for optimization and assigned the fitness value as well. For the comparison case, the fitness value of this design is 3.27, where parasitic domain scores 1.22, as of the loop inductance of 16.9 nH; thermal domains scores 1.515, as of the volume of the module is 117.6 cm³; operation domains scores 1.77, as of the switching frequency of 62.7 kHz.

On the other hand, based on the evaluation of Alpha version, fitness value of this design is 3.27, where parasitic domain scores 0.84, as of the loop inductance of 20.7 nH; thermal domains scores 0.83, as of the volume of module is 215 cm³; operation domains scores 1.03, as of the switching frequency of 36.7 kHz. There is a huge difference between the newly optimized design and the previous over-designed Alpha version. It has to be admitted that the developments in SiC device have also contributed to this improvement, and it is not fair to directly compare the Gamma version and the Alpha version.

The comparisons between Gamma version power module and the conventionally designed power module are summarized as Fig. 8-7.

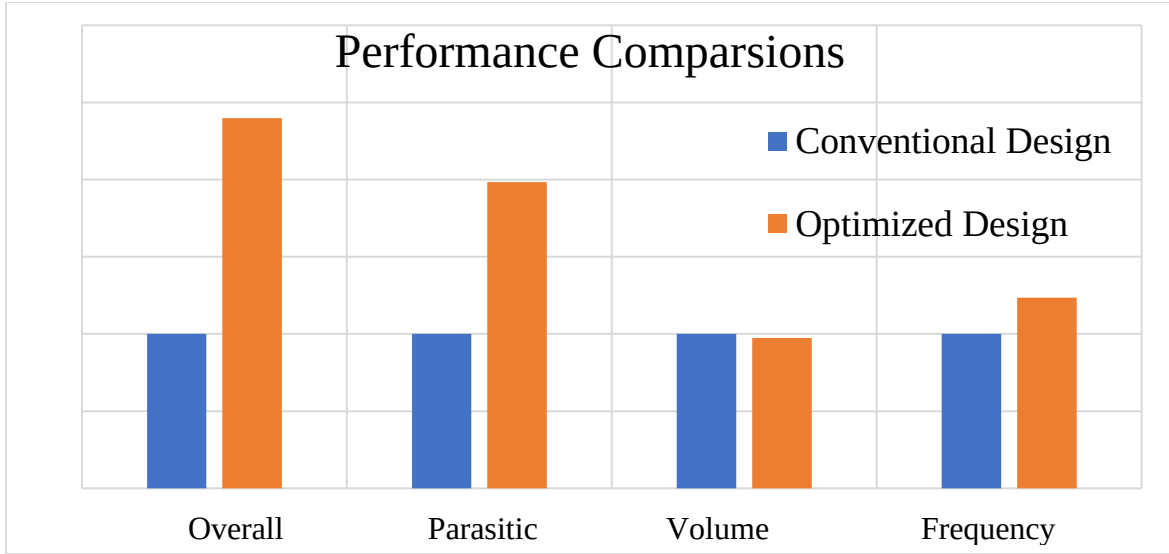


Fig. 8-7. Performance comparisons

It can be noticed that, for this particular case, the improvement is achieved by the layout optimization along with minor improvements in the other objects. As the overall performance, by applying the proposed optimization method, power density related performances almost doing twice as well as the conventionally designed case.

9. Conclusions and Future Work

Drawbacks due to the interaction tradeoffs between multiple optimization domains have overwhelmed the benefits brought by ultimate optimization on a single domain in the design of power modules. This dissertation targeted on this problem and developed a multi-objective optimization method for power electronics packaging. Multi-objective optimization methods have to be developed to further improve power electronics packaging performance.

9.1. CONCLUSIONS

As an interdisciplinary research, power electronics design includes considerations of different interacted domains. Optimization methods of the three major domains, i.e. the thermal, parasitic inductance and the operation domain are covered in this dissertation. Efforts on each domain have been made, as published in [117-122]. The key points of this dissertation are summarized as follows.

Tradeoffs among all interactive domains were analyzed based on literature review and state-of-art. Analyzed results indicated that balancing the tradeoffs is more important than a single-domain optimization. To further enhance the power electronics module performance, a multi-objective optimization is the key to achieve a higher power density design.

The Genetic Algorithm presented in this dissertation was modified specifically for power electronics packaging design purposes based on the conventional features. It provided an automatic method for customized high-power density packaging design.

Different from the conventional design methods, all tradeoffs are paralleled in one iteration loop and balanced automatically.

Co-simulation environment using FEA simulation inside the GA ensures the accuracy of the proposed method. Different from the analytical models used in many of the previous packaging researches, more complex structures can be involved without taking large approximations. To enable this feature in an automatic process, co-simulation interface connecting COMSOL and MATLAB was developed. This interface allowed direct controls from the script coded in the algorithm without manual supervisions.

3D printing was implemented in this dissertation as the primary manufacture method, due to its complexity free feature. A material property of 3D printed Aluminum (Al_AM) was compared to Aluminum alloy 6061 (Al_6061) by both simulation and experimental tests. 10% performance degradations due to the low thermal conductivity were noticed when using Al_AM. However, a thermal anneal process by heating the material up to 350 °C can bring the thermal performance equivalent to Al_6061. This finding supports the candidacy and consideration of 3D printed heatsink for advanced packaging design.

Thermal domain constructed in this dissertation provided a design approach for the customized and better heat sink design. Compared to the conventional thermal design approach, that is, using thermal resistance as a reference to select the commercially available heat sinks, the proposed work based on self-learning, enabled the algorithm to optimize the heatsink based on previously learned features. Compared to the conventional design cases, both enhanced thermal performance and reduced system volume have been achieved according to both simulation and experimental tests.

Substrate design of power modules was also enabled as an automated method in this dissertation. The function is realized by two loops, where the outer loop determines devices layout governed by GA and the inner loop is assigned to find the interconnection locations that can introduce minimum parasitic inductance. A hybrid parasitic inductance extraction method was also proposed in the inner loop, took the advantages of both FEA simulation and the analytical based extraction methods. Accurate results and fast evaluation could be achieved at the same time.

MTEC model in the operation domain is constructed as the secondary loop to find the optimal switching frequency of a given packaging design. Drawbacks of the conventional TEC were analyzed that can introduce large errors when estimating the thermal performance of multiple devices. MTEC targeting on this situation was constructed based on FEA test data and fitted by GA. This method can provide a more accurate junction temperature estimation when updating the switching frequency in the loop. This domain enables the iterative approach of optimal switching frequency with accuracy and speed.

With all three domains linked together, the overall multi-objective optimization case of an air-cooled power stage was studied and compared to the conventionally designed case. In terms of the fitness value which includes the consideration of thermal, parasitic inductance and the passive components size, the performance of optimized design was doubled. Results confirmed the expected performance of the proposed method of this dissertation. This multi-objective optimization method can be applied to more packaging design cases in the future.

9.2. RECOMMENDED FUTURE WORKS

There are some other functions which have not been developed in this dissertation.

These objectives targeting different tradeoff aspects and should be involved in the future works for a better and more powerful optimization method.

- Actual switching speed, di/dt , which has impacts on either the overshoot voltage issue or the overlapped switching loss magnitude. If considering this parameter, the switching speed will become an adjustable parameter and need to be optimized for balancing this tradeoff. By doing so, the gate loop property has to be included during the process.
- The gate loop information layout on the substrate has been ignored. Optimization on the gate configuration should be regarded as a separate domain, including the gate trace routing, the gate resistance selection and other properties.
- Operation domain needs to include more parameters other than the switching frequency. For example, if the DC link voltage can be adjusted, a tradeoff will be raised up between switching loss and the conduction loss. Also, this will also impact the voltage stress on the device, which regards the tradeoff between device rating and the overshoot voltage. Moreover, the dead time of each switch transient can be adjustable based on the switching speed and the switching frequency.
- The thermal domain can be modified with more complex design structures and the database of available fan or pump. Even though this domain is one of the most developed domains in this dissertation, the optimization of computation speed and the solution space could be beneficial for the better optimization performance.

- The passive components, which are represented in this dissertation by switching frequency, need to be covered by an individual domain. In this domain, accurate models of the passive components value, size to its operating conditions necessary to ensure the optimization performance. A database that includes all commercially available components needs to be built and the mathematics-based analytical model for inductance and capacitance of each type of the filter need to be implemented.
- Device and schematic selections freedom can be involved for a much larger solution space, potentially resulting in a better-optimized result.
- Cost, as one key factor of the SWaP-C optimization, has not been looked into in this dissertation. A compact database, including different components performances, such as the device characterizations, should be constructed. With this database, a device domain can be also added to the main structure enabling a more advanced solution.
- Temperature-dependent circuit simulation: The impacts of temperature on device behaviors have been studied during the device characterization. It will be beneficial if the temperature-dependent parameters are included in the structure as a good estimation of the real operation case. The SPICE model of such characterization can be built in SIMULINK and interacted with the MTEC model for the device behaviors update.
- Reliability related work has been slightly presented in this dissertation, a more detailed analysis needs to be done for a compact power module design package.
- Graphical User Interface (GUI), as the last modification, should be added to this package. For this version, the optimization is process based on the lines of codes in MATLAB. In the future, if trying to apply this method to a wider application, an easier operation and the clear display is necessary for it to be accepted by more researchers.

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References

- [1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd Ed. ed. Springer, 2001.
- [2] R. L. Steigerwald, "Power electronic converter technology," *Proceedings of the IEEE*, vol. 89, no. 6, pp. 890-897, 2001.
- [3] D. Costinett. (October 15, 2014). *Modeling Power in Electric Vehicles*.
- [4] B. Ozpineci, "System Impact of Silicon Carbide Power Electronics on Hybrid Electric Vehicle Applications," Ph.D., University of Tennessee, Knoxville, 2002.
- [5] R. Team. (2015). Available: <http://coolcadelectronics.com/proj1.html>
- [6] L. Boteler, "Thermal Design of Power Electronics," The Nation's Premier Laboratory for Land Forces, U.S. Amry2018.
- [7] J. Keller, "SWaP: how size, weight, and power are transforming the military electronics industry," 2013.
- [8] U. S. D. Partnership, "Electrical and Electronics Technical Team Roadmap," 2017.
- [9] John M. Miller, "Oak Ridge National Laboratory Annual Progress Report for the Power Electronics and Electric Motors Program," Electrical and Electronics Systems Research Division, ORNL2013.
- [10] Wikipedia. *Iterative method*. Available: https://en.wikipedia.org/wiki/Iterative_method
- [11] G. N. Ellison, *Thermal Computations for Electronic Equipment*, 2nd ed. New York, USA, 1989.
- [12] A. H. A. Kraus, *Thermal Analysis and Control of Electronic Equipment*. Washington, USA: Hemisphere Publishing Corporation, 1983.
- [13] S. J. E. Dede, and F. Zhou, "Topology Optimization, Additive Layer Manufacturing, and Experimental Testing of an Air-Cooled Heat Sink," *Journal of Mechanical Design*, vol. 137(11), p. 111403, October 12, 2015.
- [14] D. Christen, M. Stojadinovic, and J. Biela, "Energy efficient heat sink design: Natural vs. forced convection cooling," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2016, pp. 1-8.
- [15] S. S. Kang, "Advanced Cooling for Power Electronics," in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, 2012, pp. 1-8.
- [16] F. P. Incropera, *Liquid Cooling of Electronics Devices by Single-Phase Convection*. New York: Wiley, 1999.
- [17] L. Seri, "Optimum design and selection of heat sinks," in *Proceedings of 1995 IEEE/CPMT 11th Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM)*, 1995, pp. 48-54.
- [18] N. Seshasayee, "Understanding Thermal Dissipation and Design of a Heatsink," in "Application Report," Texas Instruments, 2011.
- [19] S. D. Sudhoff, *Power Magnetic Devices: A Multi-Objective Design Approach*. Wiley-IEEE Press 2014.
- [20] F. Calignano *et al.*, "Overview on Additive Manufacturing Technologies," *Proceedings of the IEEE*, vol. 105, no. 4, pp. 593-612, 2017.
- [21] A. Savini and G. G. Savini, "A short history of 3D printing, a technological revolution just started," in *2015 ICOHTEC/IEEE International History of High-Technologies and their Socio-Cultural Contexts Conference (HISTELCON)*, 2015, pp. 1-8.

- [22] R. W. Keyes, "Heat transfer in forced convection through fins," *IEEE Transactions on Electron Devices*, vol. 31, no. 9, pp. 1218-1221, 1984.
- [23] U. Drofenik, A. Stupar, and J. W. Kolar, "Analysis of Theoretical Limits of Forced-Air Cooling Using Advanced Composite Materials With High Thermal Conductivities," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 4, pp. 528-535, 2011.
- [24] R. W. Knight, J. S. Goodling, and D. J. Hall, "Optimal Thermal Design of Forced Convection Heat Sinks-Analytical," *Journal of Electronic Packaging*, vol. 113, no. 3, pp. 313-321, 1991.
- [25] R. W. Knight, D. J. Hall, J. S. Goodling, and R. C. Jaeger, "Heat sink optimization with application to microchannels," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 15, no. 5, pp. 832-842, 1992.
- [26] N. Puqi, L. Guangyin, F. Wang, and K. D. T. Ngo, "Selection of heatsink and fan for high-temperature power modules under weight constraint," in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, 2008, pp. 192-198.
- [27] S. Sasaki and T. Kishimoto, "Optimal structure for microgrooved cooling fin for high-power LSI devices," *Electronics Letters*, vol. 22, no. 25, pp. 1332-1334, 1986.
- [28] W. A. Khan, J. R. Culham, and M. M. Yovanovich, "Optimization of Microchannel Heat Sinks Using Entropy Generation Minimization Method," *IEEE Transactions on Components and Packaging Technologies*, vol. 32, no. 2, pp. 243-251, 2009.
- [29] R. E. Simons, "Estimating The Effect Of Flow Bypass On Parallel Plate-Fin Heat Sink Performance," in *Electronics Cooling*, ed. Calculation Corner, Design, Heat Sinks, Number 1, 2004.
- [30] K.-C. Chen and C.-C. Wang, "Performance improvement of high power liquid-cooled heat sink via non-uniform metal foam arrangement," *Applied Thermal Engineering*, vol. 87, pp. 41-46, 2015/08/05/ 2015.
- [31] X. Jun and R. A. Wirtz, "In-plane effective thermal conductivity of plain-weave screen laminates," *IEEE Transactions on Components and Packaging Technologies*, vol. 25, no. 4, pp. 615-620, 2002.
- [32] L. Chen and R. A. Wirtz, "Development of a high performance heat Sink Based on screen-fin technology," *IEEE Transactions on Components and Packaging Technologies*, vol. 28, no. 1, pp. 80-87, 2005.
- [33] Y. Zhu, H. T. Hu, S. Sun, and G. L. Ding, "Heat transfer measurements and correlation of refrigerant low boiling in tube parallel with copper foam," *Int. J. Refrig.*, vol. 38, no. 215, p. 226, 2014.
- [34] K. Boomsma, D. Poulikakos, and F. Zwick, "Metal foams as compact high performance heat exchangers," *Mechanics of Materials*, vol. 35, no. 12, pp. 1161-1176, 2003/12/01/ 2003.
- [35] S. Krishnan, D. Hernon, M. Hodes, J. Mullins, and A. M. Lyons, "Design of Complex Structured Monolithic Heat Sinks for Enhanced Air Cooling," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 2, no. 2, pp. 266-277, 2012.
- [36] K.-S. Yang, C.-M. Chiang, Y.-T. Lin, K.-H. Chien, and C.-C. Wang, "On the heat transfer characteristics of heat sinks: Influence of fin spacing at low Reynolds

- number region," *International Journal of Heat and Mass Transfer*, vol. 50, no. 13, pp. 2667-2674, 2007/07/01/ 2007.
- [37] R. L. Webb, "The Flow Structure in the Louvered Fin Heat Exchanger Geometry," *SAE Transactions*, vol. 99, pp. 1592-1603, 1990.
 - [38] A. Sadeghianjahromi, S. Kheradmand, and H. Nemati, "Developed correlations for heat transfer and flow friction characteristics of louvered finned tube heat exchangers," *International Journal of Thermal Sciences*, vol. 129, pp. 135-144, 2018/07/01/ 2018.
 - [39] A. Achaichia and T. A. Cowell, "Heat transfer and pressure drop characteristics of flat tube and louvered plate fin surfaces," *Experimental Thermal and Fluid Science*, vol. 1, no. 2, pp. 147-157, 1988/04/01/ 1988.
 - [40] A. M. Jacobi and R. K. Shah, "Heat transfer surface enhancement through the use of longitudinal vortices: A review of recent progress," *Experimental Thermal and Fluid Science*, vol. 11, no. 3, pp. 295-309, 1995/10/01/ 1995.
 - [41] C.-C. Wang, K.-Y. Chen, J.-S. Liaw, and C.-Y. Tseng, "An experimental study of the air-side performance of fin-and-tube heat exchangers having plain, louver, and semi-dimple vortex generator configuration," *International Journal of Heat and Mass Transfer*, vol. 80, pp. 281-287, 2015/01/01/ 2015.
 - [42] K. S. Yang, J. H. Jhong, Y. T. Lin, K. H. Chien, and C. C. Wang, "On the Heat Transfer Characteristics of Heat Sinks: With and Without Vortex Generators," *IEEE Transactions on Components and Packaging Technologies*, vol. 33, no. 2, pp. 391-397, 2010.
 - [43] K. S. Yang, S.-L. Li, I. Chen, and C.-C. Wang, *Analysis and Optimum for Air Cooling Thermal Module Using Dimple Vortex Generators*. 2010.
 - [44] C.-C. Wang, K.-S. Yang, Y.-P. Liu, and I. Y. Chen, "Effect of cannelure fin configuration on compact aircooling heat sink," *Applied Thermal Engineering*, vol. 31, no. 10, pp. 1640-1647, 2011/07/01/ 2011.
 - [45] T. Y. Kim and S. J. Kim, "Fluid flow and heat transfer characteristics of cross-cut heat sinks," *International Journal of Heat and Mass Transfer*, vol. 52, no. 23, pp. 5358-5370, 2009/11/01/ 2009.
 - [46] S. Chingulpitak, N. Chimres, K. Nilpueng, and S. Wongwises, "Experimental and numerical investigations of heat transfer and flow characteristics of cross-cut heat sinks," *International Journal of Heat and Mass Transfer*, vol. 102, pp. 142-153, 2016/11/01/ 2016.
 - [47] O. Vozisova, S. Eroshenko, E. Koksharova, A. Khalyasmaa, and S. Dmitriev, "Application of 3D scanning and printing technologies in Electric power industry," in *2016 IEEE International Conference on Industrial Technology (ICIT)*, 2016, pp. 892-897.
 - [48] M. Chinthavali, "3D printing technology for automotive applications," in *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, 2016, pp. 1-13.
 - [49] T. Keim, "Three-Dimensional Printing in Power Electronics Manufacturing [Happenings]," *IEEE Power Electronics Magazine*, vol. 4, no. 1, pp. 10-13, 2017.
 - [50] E. Dede, *Optimization and Design of a Multipass Branching Microchannel Heat Sink for Electronics Cooling*. 2012, p. 041001.

- [51] G. H. Yoon, "Topological design of heat dissipating structure with forced convective heat transfer," *Journal of Mechanical Science and Technology*, vol. 24, no. 6, pp. 1225-1233, 2010/06/01 2010.
- [52] R. Bornoff and J. Parry, "An additive design heatsink geometry topology identification and optimisation algorithm," in *2015 31st Thermal Measurement, Modeling & Management Symposium (SEMI-THERM)*, 2015, pp. 303-308.
- [53] R. Bornoff, J. Wilson, and J. Parry, "Subtractive design: A novel approach to heatsink improvement," in *2016 32nd Thermal Measurement, Modeling & Management Symposium (SEMI-THERM)*, 2016, pp. 198-205.
- [54] Y. Yan, D. Chao, K. D. T. Ngo, Y. Mei, and G. Q. Lu, "Additive manufacturing of planar inductor for Power Electronics applications," in *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, 2016, pp. 1-16.
- [55] Y. Yan, J. Moss, K. D. T. Ngo, Y. Mei, and G. Q. Lu, "Additive manufacturing of toroid inductor for power electronics applications," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-6.
- [56] Y. Yi, K. D. T. Ngo, M. Yuhui, and L. Guo-Quan, "Additive manufacturing of magnetic components for power electronics integration," in *2016 International Conference on Electronics Packaging (ICEP)*, 2016, pp. 368-371.
- [57] L. Liu, T. Ge, Y. Yan, K. D. T. Ngo, and G. Q. Lu, "UV-assisted 3D-printing of soft ferrite magnetic components for power electronics integration," in *2017 International Conference on Electronics Packaging (ICEP)*, 2017, pp. 447-450.
- [58] W. Liang, L. Raymond, and J. Rivas, "3-D-Printed Air-Core Inductors for High-Frequency Power Converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 52-64, 2016.
- [59] W. Liang *et al.*, "Low-Mass RF Power Inverter for CubeSat Applications Using 3-D Printed Inductors," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 880-890, 2017.
- [60] B. Chou, J. S. Park, and W. S. Kim, "3D printed inductor designs decorated with silver nano ink," in *2015 IEEE Nanotechnology Materials and Devices Conference (NMDC)*, 2015, pp. 1-2.
- [61] G. McKerricher, J. G. Perez, and A. Shamim, "Fully Inkjet Printed RF Inductors and Capacitors Using Polymer Dielectric and Silver Conductive Ink With Through Vias," *IEEE Transactions on Electron Devices*, vol. 62, no. 3, pp. 1002-1009, 2015.
- [62] N. Lazarus, C. D Meyer, S. S Bedair, H. Nochetto, and I. M Kierzewski, *Multilayer liquid metal stretchable inductors*. 2014, p. 085036.
- [63] S.-Y. Wu, C. Yang, W. Hsu, and L. Lin, "3D-printed microelectronics for integrated circuitry and passive wireless sensors," *Microsystems & Nanoengineering*, Article vol. 1, p. 15013, 07/20/online 2015.
- [64] M.-S. Kim, W.-S. Chu, Y.-M. Kim, A. P. G. Avila, and S.-H. Ahn, "Direct metal printing of 3D electrical circuit using rapid prototyping," *International Journal of Precision Engineering and Manufacturing*, vol. 10, no. 5, pp. 147-150, 2009/12/01 2009.
- [65] C. Staudigel, M. Hoffmann, G. Schwalme, U. Mohr-Matuschek, P. Heidemeyer, and M. Bastian, "Additive manufacturing of electric circuits based on graphene

- polymer nanocomposites," in *2016 12th International Congress Molded Interconnect Devices (MID)*, 2016, pp. 1-5.
- [66] M. Conrad, R. W. D. Doncker, M. Schniedenharn, and A. Diatlov, "Packaging for power semiconductors based on the 3D printing technology Selective Laser Melting," in *2014 16th European Conference on Power Electronics and Applications*, 2014, pp. 1-7.
 - [67] C. Bailey, S. Stoyanov, T. Tilford, and G. Tzouroulouk, "3D-printing and electronic packaging - current status and future challenges," in *2016 IEEE 18th Electronics Packaging Technology Conference (EPTC)*, 2016, pp. 1-4.
 - [68] J. Veres *et al.*, "Additive manufacturing for electronics “Beyond Moore”," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 25.6.1-25.6.3.
 - [69] W. Frank Fan and E. Parker, "3D printed micro-channel heat sink design considerations," in *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, 2016, pp. 1-13.
 - [70] *Parasitic element (electrical networks)*. Available: [https://en.wikipedia.org/wiki/Parasitic_element_\(electrical_networks\)](https://en.wikipedia.org/wiki/Parasitic_element_(electrical_networks))
 - [71] Y. Shen, J. Jiang, Y. Xiong, Y. Deng, X. He, and Z. Zeng, "Parasitic Inductance Effects on the Switching Loss Measurement of Power Semiconductor Devices," in *2006 IEEE International Symposium on Industrial Electronics*, 2006, vol. 2, pp. 847-852.
 - [72] J. B. Witcher, "Methodology for Switching Characterization of Power Devices and Modules," Master, Science In Electrical Engineering, Virginia Polytechnic Institute and State University, USA, January 2002.
 - [73] C. Martin, J. L. Schanen, and R. Pastarczyk, "Inside a power module," in *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, 2004, vol. 3, pp. 1519-1525 vol.3.
 - [74] M. Meisser, M. Schmenger, and T. Blank, "Parasitics in Power Electronic Modules: How parasitic inductance influences switching and how it can be minimized," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1-8.
 - [75] L. Schnur, G. Debled, S. Dewar, and J. Marous, "Low inductance, explosion robust IGBT modules in high power inverter applications," in *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting (Cat. No.98CH36242)*, 1998, vol. 2, pp. 1056-1060 vol.2.
 - [76] P. O. Jeannin, J. L. Schanen, and E. Clavel, "Original cabling conditions to insure balanced current during switching transitions between paralleled semiconductors," *IEEE Transactions on Industry Applications*, vol. 38, no. 1, pp. 181-188, 2002.
 - [77] W. Teulings, J. L. Schanen, and J. Roudet, "MOSFET switching behaviour under influence of PCB stray inductance," in *Industry Applications Conference, 1996. Thirty-First IAS Annual Meeting, IAS '96., Conference Record of the 1996 IEEE*, 1996, vol. 3, pp. 1449-1453 vol.3.

- [78] E. Shelton, X. Zhang, T. Zhang, N. Hari, and P. Palmer, "Low inductance switching for SiC MOSFET based power circuit," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 5093-5100.
- [79] J. Richmond *et al.*, "An overview of Cree silicon carbide power devices," in *Power Electronics in Transportation (IEEE Cat. No.04TH8756)*, 2004, pp. 37-42.
- [80] J. Wang, H. S. h. Chung, and R. T. h. Li, "Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 573-590, 2013.
- [81] Z. Chen, "Characterization and Modeling of High-Switching-Speed Behavior of SiC Active Devices," Master of Science, Electrical Engineering, Virginia Polytechnic Institute, 2009.
- [82] Z. Wang, J. Zhang, X. Wu, and K. Sheng, "Analysis of stray inductance's influence on SiC MOSFET switching performance," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 2838-2843.
- [83] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, 2010, pp. 164-169.
- [84] F. Yang, Z. Liang, W. Zhiqiang, and W. Fred, "Parasitic inductance extraction and verification for 3D planar bond all module," in *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, 2016, pp. 1-15.
- [85] Z. Chen, D. Boroyevich, P. Mattavelli, and K. Ngo, "A frequency-domain study on the effect of DC-link decoupling capacitors," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 1886-1893.
- [86] T. Ibuchi and T. Funaki, "A study on parasitic inductance reduction design in GaN-based power converter for high-frequency switching operation," in *2017 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2017, pp. 1-5.
- [87] F. Yang, Z. Liang, Z. J. Wang, and F. Wang, "Design of a low parasitic inductance SiC power module with double-sided cooling," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 3057-3062.
- [88] C. H. J. Poh, S. K. Bhattacharya, J. Ferguson, J. D. Cressler, and J. Papapolymerou, "Extraction of a lumped element, equivalent circuit model for via interconnections in 3-D packages using a single via structure with embedded capacitors," in *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*, 2010, pp. 1783-1788.
- [89] S. Li, L. M. Tolbert, F. Wang, and F. Z. Peng, "P-cell and N-cell based IGBT module: Layout design, parasitic extraction, and experimental verification," in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2011, pp. 372-378.
- [90] C. R. Paul, *Inductance Loop and Partial*. John Wiley & Sons, 2010.
- [91] A. Letellier, M. Dubois, J. P. F. Trovao, and H. Maher, "Calculation of PCB Power Loop Stray Inductance in GaN or High di/dt Applications," *IEEE Transactions on Power Electronics*, pp. 1-1, 2018.

- [92] K. Xing, F. C. Lee, and D. Boroyevich, "Extraction of parasitics within wire-bond IGBT modules," in *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual, 1998*, vol. 1, pp. 497-503 vol.1.
- [93] A. E. Ruehli, "Inductance Calculations in a Complex Integrated Circuit Environment," *IBM Journal of Research and Development*, vol. 16, no. 5, pp. 470-481, 1972.
- [94] M. K. Mills, "Self inductance formulas for quadrupole loops used with vehicle detectors," in *35th IEEE Vehicular Technology Conference*, 1985, vol. 35, pp. 81-87.
- [95] N. Zhu, M. Chen, and D. Xu, "A Simple Method to Evaluate Substrate Layout for Power Modules," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1-6.
- [96] Z. Chen, R. Burgos, D. Boroyevich, F. Wang, and S. Leslie, "Modeling and simulation of 2 kV 50 A SiC MOSFET/JBS power modules," in *2009 IEEE Electric Ship Technologies Symposium*, 2009, pp. 393-399.
- [97] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Simulation model development and verification for high voltage GaN HEMT in cascode structure," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 3579-3586.
- [98] M. W. Beattie and L. T. Pileggi, "Inductance 101: modeling and extraction," in *Proceedings of the 38th Design Automation Conference (IEEE Cat. No.01CH37232)*, 2001, pp. 323-328.
- [99] C. Yan, W. Yu, and Z. Wang, *A mixed boundary element method for extracting frequency-dependent inductances of 3D interconnects*. 2006, pp. 6 pp.-716.
- [100] P. A. Brennan, N. Raver, and A. Ruehli, *Three-Dimensional Inductance Computations with Partial Element Equivalent Circuits*. 1979, pp. 661-668.
- [101] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. Costinett, "Understanding the limitations and impact factors of wide bandgap devices' high switching-speed capability in a voltage source converter," in *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2014, pp. 7-12.
- [102] R. W. Erickson, "Supplementary notes on EMI and Layout Fundamentals for Switched-Mode Circuits," Department of Electrical and Computer Engineering: University of Colorado at Boulder
- [103] C. DiMarino, W. Zhang, R. Burgos, and D. Boroyevich, "Design of a high-density, diode-less 1.2 kV, 90 A SiC MOSFET half-bridge power module," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 210-214.
- [104] X. Zhang, Z. Shen, N. Haryani, D. Boroyevich, and R. Burgos, "Ultra-low inductance vertical phase leg design with EMI noise propagation control for enhancement mode GaN transistors," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1561-1568.
- [105] L. Zhang, S. Guo, X. Li, Y. Lei, W. Yu, and A. Q. Huang, "Integrated SiC MOSFET module with ultra low parasitic inductance for noise free ultra high speed switching," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 224-229.

- [106] L. Zhang, P. Liu, A. Q. Huang, S. Guo, and R. Yu, "An improved SiC MOSFET-gate driver integrated power module with ultra low stray inductances," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 342-345.
- [107] M. Wang, F. Luo, and L. Xu, "A double-end sourced multi-chip improved wire-bonded SiC MOSFET power module design," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 709-714.
- [108] Y. Ren *et al.*, "Voltage Suppression in Wire-Bond-Based Multichip Phase-Leg SiC MOSFET Module Using Adjacent Decoupling Concept," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8235-8246, 2017.
- [109] F. Z. Peng, L. M. Tolbert, and F. Khan, "Power electronics' circuit topology - the basic switching cells," in *IEEE Workshop Power Electronics Education*, 2005., 2005, pp. 52-57.
- [110] S. Li, L. M. Tolbert, F. Wang, and F. Z. Peng, "Reduction of stray inductance in power electronic modules using basic switching cells," in *2010 IEEE Energy Conversion Congress and Exposition*, 2010, pp. 2686-2691.
- [111] S. Li, L. M. Tolbert, F. Z. Peng, and F. Z. Peng, "Stray Inductance Reduction of Commutation Loop in the P-cell and N-cell-Based IGBT Phase Leg Module," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3616-3624, 2014.
- [112] Z. J. Wang, F. Yang, S. Campbell, and M. Chinthavali, "Development of a low-inductance SiC trench MOSFET power module for high-frequency application," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 2834-2841.
- [113] X. Zhao, B. Gao, L. Zhang, D. C. Hopkins, and A. Q. Huang, "Performance optimization of A 1.2kV SiC high density half bridge power module in 3D package," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 1266-1271.
- [114] X. Lin, J. Li, and C. M. Johnson, "Impedance analysis in a co-planar power bus interconnect prototype for low inductance switching," in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, 2018, pp. 1-6.
- [115] S. Savulak, B. Guo, and S. Krishnamurthy, "Three-phase inverter employing PCB embedded GaN FETs," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 1256-1260.
- [116] C. DiMarino, D. Boroyevich, R. Burgos, M. Johnson, and G. Q. Lu, "Design and development of a high-density, high-speed 10 kV SiC MOSFET module," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, pp. P.1-P.10.
- [117] T. Wu, B. Ozpineci, M. Chinthavali, Z. Wang, S. Debnath, and S. Campbell, "Design and optimization of 3D printed air-cooled heat sinks based on genetic algorithms," *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*, Chicago, IL, 2017, pp. 650-655.
- [118] A. A. Wereszczak, J. Cousineau, K. Bennion, H. Wang, R. H. Wiles, T. B. Burrell, and T. Wu "Anisotropic Thermal Response of Packed Copper Wire," *ASME. J. Thermal Sci. Eng. Appl.* 2017

- [119] T. Wu, A. A. Wereszczak, H. Wang, B. Ozpineci, "Thermal response of additive manufactured Aluminum," *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, Raleigh, NC, 2016, pp. 1-15.
- [120] T. Wu, B. Ozpineci, "Impact of Heat Dissipation Profiles on Power Electronics Packaging Design," *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, Long Beach, 2019.
- [121] M. Chinthavali, Z. J. Wang, S. Campbell, T. Wu and B. Ozpineci, "50-kW 1kV DC bus air-cooled inverter with 1.7 kV SiC MOSFETs and 3D-printed novel power module packaging structure for grid applications," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 133-140.
- [122] T. Wu, B. Ozpineci, and C. Ayers "Genetic algorithm design of a 3D printed heat sink," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 3529-3536.

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