# CMOS Silicon Photomultiplier using Perimeter Gated Single Photon Avalanche Diode

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Doctor of Philosophy

Degree

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# Dedicated to

*My husband & sons*

Mohammad Shah Alam

Ahnaf Alam and Ayaan Alam

*My parents*

Md. Shawkat Ali Sarkar

Khaleda Shawkat

*My teacher*

Dr. Mohammad Ali Choudhury

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# Abstract

Photomultiplier tubes (PMTs) are used as photo-sensors in many applications including the medical field, nuclear science, and astrophysics. Since silicon photmultipliers (SiPMs) are relatively insusceptible to magnetic fields, compact, and require relatively lower bias voltages, they have been aroused interests and showing a great potential as a substitute to photomultiplier tubes (PMTs). SiPM consists of a large array of parallel diodes biased above breakdown with a series resistor. These diodes are known as single photon avalanche diodes or SPADs. This dissertation designs and characterizes SiPMs based on a new device Perimeter Gated SPADs or PGSPAD, fabricated in standard CMOS process.

The novel contributions of this work are as follows.

1. The effectiveness of the additional gate terminal to modulate the breakdown voltage has been verified for the perimeter gated SPAD device fabricated in standard 0.5 $\mu$m HV and 0.35 $\mu$m CMOS processes.

2. PGSPAD noise has been experimentally characterized over a range of temperatures with the variation of gate voltage for the first time.

3. A full chip CMOS analog SiPM using PGSPAD has been reported for the first time and fully characterized for noise, sensitivity, signal to noise ratio throughout the visible spectral range, and thermal characterization for varying bias voltages.

4. A CMOS digital SiPM with fully digital asynchronous address event representation (AER) readout has been demonstrated for the first time to provide high bandwidth with tunable noise performance using PGSPAD based pixels.

5. Finally, a novel electrical model for the perimeter gated SPAD based silicon photomultiplier (SiPM) detector has been developed to accurately simulate the static, dynamic, and stochastic noise behavior of the SiPM detector with the effect of additional gate terminal.

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# Chapter 1
# Introduction and Motivation

## 1.1 Introduction

Silicon photomultipliers (SiPMs) have been widely used as photon-sensing devices in a wide range of nuclear imaging applications in medical, high energy physics, and other fields. SiPMs are preferred as an alternative to photomultiplier tubes (PMTs) due to their invulnerability to magnetic fields, compactness, low operating voltage, robustness, and lower cost [1–13]. They have been used to detect scintillation light in imaging applications such as position emission tomography (PET) [14–20], multimodality PET-magnetic resonance imaging (MRI) [15, 21], high-energy physics [22–24], and single photon emission computed tomography (SPECT) [25–29].

SiPMs may be classified as one of two types, either analog or digital. Analog SiPMs consist of a large array of parallel single avalanche photo diodes (SPADs) with a series resistor and biased beyond reverse breakdown [6, 30–34]. These avalanche photo diodes are known as single photon avalanche diodes or SPADs. The current of all the avalanched SPADs are summed to generate the total output current in an analog SiPM. The resulting current is proportional to the number of detected photons. Analog SiPMs have a broad range of uses. These include recording of single photon events and multi-photon events [30, 34].

Since a single photon jump starts the avalanche process, the amount of current generated by the avalanche is not important. Rather, the fact that an avalanche has occurred due to the presence of that single photon is the significant point. This means that only the recognition that an avalanche has occurred is required to register the presence or absence of a photon. Thus a SPAD's output can be considered to be an ON/OFF signal, i.e. almost wholly in the digital domain. In this domain, the noise performance is notably improved and has led to a number of digital SiPM architectures in literature [9–11, 13, 20, 35].

## 1.2 Motivation

The number of prospective applications taking advantages of solid-state sensors, along with the subsequent demand of integrated front-end electronics suitable for SiPM, is in great demand. Figure 1.1 demonstrates the variety of applications where SiPMs have shown a great potential to replace PMTs. These applications are PET, SPECT, PET-MRI systems, and high-energy physics systems. The main motivation underlying this dissertation is to conduct research on something that can create a potential impact on such a large and multifold field. The replacement of a photomultiplier tube (PMT) with SiPM to detect single photon makes device insensitive to magnetic fields, operating with low voltages, low cost, and compact.

In addition, another incentive for this research is the extent of the impact this work could make. These contributions impact the development of compact and less




**Figure 1.1:** Application areas where SiPMs have shown a great potential as a replacement of PMTs [36–39].

expensive silicon photomultiplier using perimeter gated SPAD for a broad range of applications including nuclear imaging and medical imaging such as PETs, SPECTs.

## 1.3 CMOS SiPM

SiPMs implemented in standard CMOS process, as opposed to a dedicated optical process, allows the optical sensor to be coupled on the same chip with the readout electronics [9,20,35,40]. This results in a compact, low cost, and low bias voltage SiPM detector. Figure 1.2 illustrates advantages of CMOS SiPMs compared with PMTs and Table 1.1 summarizes the comparison of CMOS SiPMs with commercial SiPMs

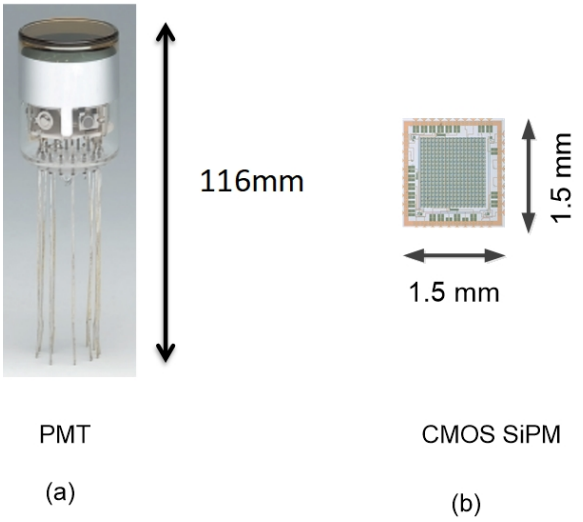



**Figure 1.2:** PMT vs. CMOS SiPM [43, 44].

**Table 1.1:** Benefits of CMOS SiPMs compared to PMTs and commercial SiPM

| PMT | Commercial SiPM | CMOS SiPM |
|---|---|---|
| Sensitive to magnetic field | Insensitive to magnetic field | Insensitive to magnetic field |
| High bias voltage ($\approx 1250V$) | Low bias voltage ($\approx 58V$) | Lower bias voltage ($\approx 10V - 30V$) |
| Expensive ($$$) | Cheap ($$) | Cheaper ($) |
| Bulky | Less bulky | Compact |

and PMTs. However, for SPADs implemented in standard CMOS electric field shows maxima at the edges due to the planar nature of CMOS technology. Therefore, the diode periphery undergoes breakdown earlier resulting in premature edge breakdown and reduction of the detector efficiency. [40–42]. Figure 1.3 shows the electric field distribution of a regular SPAD.

In order to prevent the premature breakdown a wide variety of guard ring structures for SPADs have been reported [40]. Placement of deep diffused p-well implants around the boundary of shallow p+ implantation in n-well has been reported in HV CMOS process to mitigate the PEB [35, 45, 46]. Nevertheless, the use of guard

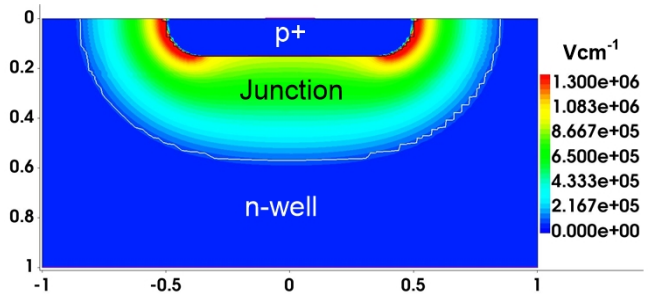



**Figure 1.3:** Electric field distribution for a regular SPAD (x-axis and y-axis are in $\mu$m).

ring adversely affects the fill factor, the ratio between the optically sensitive area to the total detective area [47,48]. Positioning n-wells closer together than allowed by the design rules allows for diffusion to occur, allowing the p-substrate to become a lightly doped n-type region. This along with a gate to control the depletion region mitigated PEB [47, 49]. These methods all rely on controlling the carrier concentration (both before and after fabrication) and the shape of the junction [49]. For SPADs fabricated in deep-submicron CMOS processes, the junction's geometry has been altered by taking advantage of the design rules for STI to prevent early breakdown [50].

Premature edge breakdown can be mitigated by placing a perimeter gate on top of the junction and regulate the electric field through the applied gate voltage without unduly enlarging the device area [41,42]. The addition of this perimeter gate creates a new device known as the perimeter gated single photon avalanche diode (PGSPAD). The applied voltage at the additional gate terminal of PGSPADs modulates electric field and makes it uniform throughout the junction. The electric field distribution of a perimeter gated SPAD is presented in Figure 1.4.

The effectiveness of applied gate voltage at the gate terminal of PGSPAD to make electric field uniform resulting in prevention of premature edge breakdown and

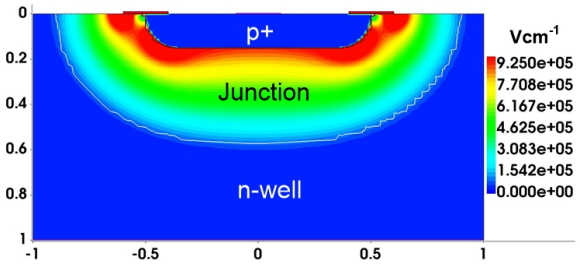



**Figure 1.4:** Electric field distribution for a perimeter gated SPAD (x-axis and y-axis are in $\mu$m).

achievement of full volumetric breakdown is demonstrated in Figure 1.5. In addition, PGSPADs can be used to adjust the device's noise floor, sensitivity, and detection range [41, 42].

SiPMs using PGSPADs fabricated in CMOS process exploits the benefits of standard CMOS process with added advantages of prevention of premature breakdown, tunabilty of noise and sensitivity. This dissertation presents and first fully characterizes a full chip analog CMOS SiPM using PGSPAD. The digital SiPM using PGSPAD with asynchronous address event representation (AER) readout to best serve the asynchronously arriving photon with high bandwidth has been demonstrated in this the dissertation for the first time. Finally, the dissertation models the perimeter gated SPAD based SiPM to evaluate and optimize the performance of SiPM detector with additional gate terminal.

## 1.4 Research Goals

The goal of this research is to improve performance of CMOS SiPM using perimeter gated single photon avalanche diode making it suitable for optical detection. In

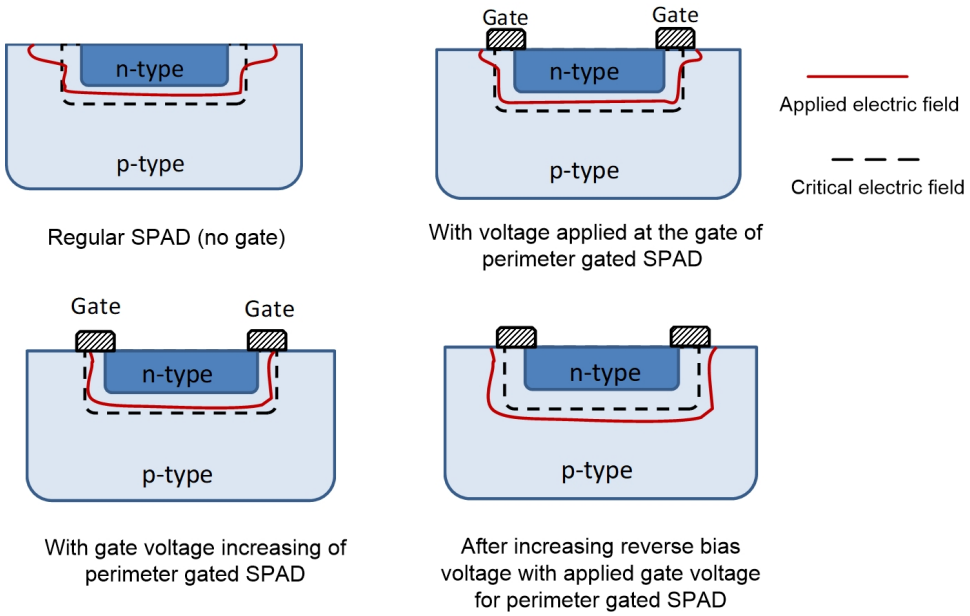



**Figure 1.5:** Effectiveness of the applied gate voltage to make electric field uniform resulting in prevention of premature edge breakdown and achievement of full volumetric breakdown.

addition, implementing in standard CMOS process helps in developing more compact and low cost SiPMs compared to those implemented in commercially available SiPMs for a broad range of applications including nuclear medical imaging and high energy physics. Perimeter gated SPAD based SiPMs are developed, modeled, and characterized. First, a full chip CMOS analog SiPM using perimeter gated SPAD is developed and fully characterized. The signal-to-noise ratio of the CMOS SiPM is enhanced through the applied gate voltage of perimeter gated SPAD device. The designed PGSPAD SiPM aims for applications such as neutron detection which requires high sensitivities and high signal to noise ratios. Since SPADs are event-based, triggered by an incident photon, they are therefore a natural partner of asynchronous address event representation (AER) multiplexing technique which provides high-bandwidth communication. A fully digital AER readout for a digital

SiPM based on PGSPAD is developed to best serve the asynchronously arriving photons with high bandwidth. Finally, a comprehensive model for SiPM based on perimeter gated SPAD is developed to evaluate the effect of parameters and to optimize the performance of SiPM with additional gate terminal. The research is subdivided into following major parts: (1) experimentally characterizing the PGSPAD noise over a range of temperature with variation of gate voltage, (2) developing and fully characterizing a full chip CMOS analog SiPM using PGSPAD for nuclear imaging applications including PETs, (3) designing a novel architecture for a CMOS PGSPAD based digital SiPM with fully digital asynchronous AER readout and evaluating the performance suitable for PET and SPECT applications including brain function analysis, clinical oncology, and clinical research, and (4) developing a new electrical model for PGSPAD based SiPM with the impact of extra gate terminal to shorten the design cycle.

## 1.5 Dissertation Overview

The dissertation is organized as follows. A comprehensive literature review of CMOS SiPMs along with the basic building block, SPAD, and its design metrics, readout electronics including SPAD front-end circuits and SiPM readout circuit is presented in Chapter 2. Chapter 3 reports the design and first complete characterization of a full chip analog SiPM using PGSPAD fabricated in standard 0.5 $\mu$m CMOS process. Characterization of SiPM implemented in 180 nm CMOS process is also

presented here. Chapter 4 demonstrates the new architecture of a digital SiPM based on PGSPAD with asynchronous fully digital address event representation (AER) readout. The characterization of the developed digital SiPM with AER readout fabricated in standard 0.5 $\mu$m is reported. The measured response of the parts of AER readout implemented in 350 nm CMOS process is reported here also. Chapter 5 describes the new electrical model for PGSPAD based SiPM to accurately simulate the static, dynamic, and stochastic noise behavior of the SiPM with the effect of additional gate terminal. Finally, the dissertation is concluded in Chapter 6.

# Chapter 2
# Literature Review

** **Portions of this chapter were published in:**

1. Mst Shamim Ara Shawkat, Mohammad Habib Ullah Habib, Md Sakib Hasan, Mohammad Aminul Haque, and Nicole McFarlane, *"Perimeter Gated Single Photon Avalanche Diodes in Sub-micron and Deep-submicron CMOS Processes,"* International Journal of High Speed Electronics and Systems, Vol. 27, no. 03n04, pp. 1840018-1-19, 2018.

2. Md Sakib Hasan, Mst Shamim Ara Shawkat, Sherif Amer, Syed Kamrul Islam, Nicole McFarlane, Garrett S Rose, *"Modeling Emerging Semiconductor Devices for Circuit Simulation,"* Modeling and Simulation in Engineering, IntechOpen, 2019.

## 2.1 Single Photon Avalanche Diode

A single photon avalanche diode (SPAD) is a p-n junction, which is biased, in the so-called Geiger mode region, above the breakdown voltage. In this region, the high electric field from the applied bias causes charge carriers to accelerate and they undergo impact ionization creating more free carriers. These are also undergo impact ionization and the number of carriers exponentially increases causing a sudden avalanche of current [41, 42, 51, 52].

Due to the impact ionization, a single photo-generated carrier in the space charge region can generate a divergent avalanche multiplication of carriers. In SPAD, the impact ionization includes both type of carriers, electrons and holes, with a built-in positive feedback effect. Therefore, the carrier multiplication becomes self-sustaining if the electric field is high. The multiplication factor indicates the number of charges accumulated for each generated charge. The relation between the multiplication factor, M, and the number of secondary carriers created by the primary moving carrier in presence of the electric field in the depletion region is given in [41, 52]

$$M = \{1 - \int_0^{W_D} \alpha_n e^{-\int_0^{W_D}(\alpha_n - \alpha_p)dx} dx\}^{-1} \tag{2.1}$$

where, $W_D$ is the depletion-layer width, and $\alpha_n$ and $\alpha_p$ are the electron and the hole ionization rates, respectively For $\alpha_n = \alpha_p = \alpha$ , the gain equation reduces to the simple form,

$$M = \frac{1}{1 - \alpha W_D}. \tag{2.2}$$

Breakdown corresponds to the situation when $\alpha W_D = 1$

Figure 2.1 illustrates the impact ionization creating a diverging avalanche multiplication process and resulting in a macroscopic avalanche current in the presence of a high electric field in the depletion region. The M tends to be infinity in eqn. 4.3 when the avalanche happens. However, there is a finite internal resistance of the device due to the space-charge effect, which reduces the voltage across the

junction. Therefore, the M is limited to some finite large value resulting in finite avalanche current.

The large avalanche current must be quenched to protect the long term use of the device. This is done by lowering the voltage across SPAD to below the breakdown voltage. Then the SPAD needs to be biased above the breakdown voltage to make it ready to detect the next photon event. Passive quenching uses a simple large resistor to reduce the voltage across the diode below the breakdown voltage [53]. This is due to the large voltage drop across the quenching resistor given by the avalanche current times the value of the resistor. In order to provide fast transition between

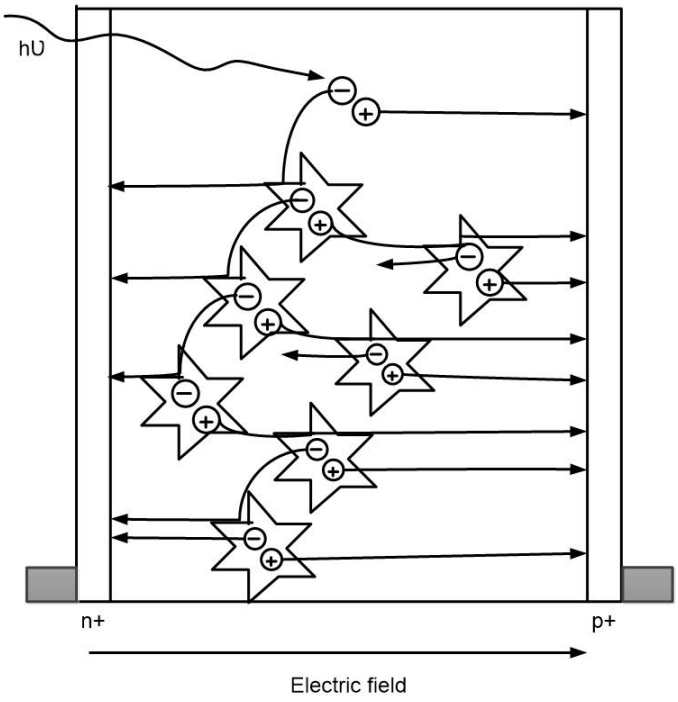



**Figure 2.1:** SPADs are biased above breakdown voltage and the diverging avalanche multiplication process is triggered by one photo generated carrier in the depletion region which leads to a macroscopic detectable output current [52].

avalanche and idle state, active quenching is also used that employs MOSFETs to bias the SPAD dynamically [40, 52].

Figure 2.2 (a) illustrates the basic SPAD operation through the avalanche upon photon arrival, quench, and reset using a quenching resistor. SPAD I-V characteristics and passive quenching load characteristics is presented in Figure 2.2 (b). In SPAD, when there is no current, the diode current, $I_D$ is zero and the voltage across the SPAD, $V_D$ is the applied reverse biased voltage, $V_A$. When the SPAD is biased above breakdown voltage with $V_A$ the avalanche is triggered due to the photon absorption or noise (thermally generated electron-hole pair, or a tunneling event). The avalanche current peaks and the bias point moves from "O" to "A" (avalanche). The avalanche current discharges the capacitor and the diode current and voltage reduces exponentially to the final value, $I_f$ and $V_f$ representing quenching. Finally, the device is reset back by increasing the bias above the breakdown voltage, moving back to "O" point.

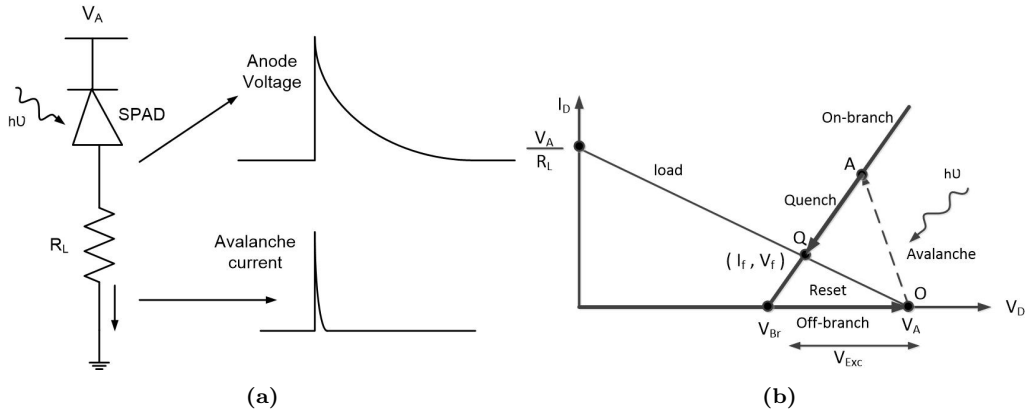



**Figure 2.2:** (a) SPAD operation goes through avalanche, quench, and reset using a quenching resistor (b) SPAD I-V characteristics and passive quenching load characteristics [54].

## 2.2 CMOS SPADs and Design Metrics

Specialized processes are typically used to fabricate SPADs due to the ability to control the noise and responsivity of the device through doping and other factors. However, the ability to make good optical devices typically means that the transistors fabricated in these processes are low quality transistors with inferior performance parameters. This means that it is difficult to integrate readout electronics onto the same chip with the SPAD [40, 41]. Thus, there is significant research into developing integrated SPADs and readout electronics in standard CMOS processes [1, 40, 41, 55–57]. There are significant benefits to the CMOS approach, this includes integrating the quenching, front end analog readout electronics, and digital processing blocks into a single chip along with the relatively low cost of fabrication and a compact design [1, 40, 41, 55–57]. Integration also reduces parasitics which improves the speed and noise of the system. In this section, the SPAD's design metrics such as dark count rate, guard ring structure, photon detection efficiency, and time resolution are briefly described.

### 2.2.1 Dark Count Rate

Ideally, only photons generate free carriers and in the absence of photons, there are no free carriers. However, there are a number of noise processes that generate these free carriers. These can be caused by thermal generation of carriers, minority carrier diffusion, and band-to-band tunneling. The dark count rate (DCR) is defined as the

effective noise for SPADs and is caused by these non-photon driven charged carrier generation processes. The technological SPAD design factors and CMOS fabrication process affects these noise generation mechanisms.

#### 2.2.1.1 Thermal Generation

Thermal generation of free-carriers is the main mechanism of dark counts for SPADs at room temperature. Local energy levels are inserted near the middle of the forbidden gap by impurities and/or crystal defects. These localized energy levels are the effective generation-recombination centers.According to the Shockley-Read-Hall statistics, the free carriers generated within a diffusion length of the SPAD space-charge region are trapped in these levels and released later. The carrier generation rate due to thermal generation, $CGR_{Th}$ is provided by the Shockley-Read-Hall theory [58] and given by

$$CGR_{Th} = \frac{n_i x_i A_D}{2\tau_0} \tag{2.3}$$

where $n_i$ is the silicon intrinsic concentration, $x_i$ is the effective thickness of the depletion region, $A_D$ represents the active area of SPAD and $\tau_0$ is the carrier life time.

Each generated carrier has a finite, non-zero probability of triggering an avalanche. $P_{tr}$ increases with the excess bias voltage ($V_{Exc}$), the difference between the applied

voltage and the breakdown. The relation between the $P_{tr}$ and $V_{Exc}$ is given in [59–61]

$$P_{tr} = \begin{cases} 0 & \text{for } V_{Exc} < 0 \\ 1 - e^{-\frac{V_{Exc}}{\eta_T V_{Br}}} & \text{for } V_{Exc} \geq 0 \end{cases} \tag{2.4}$$

where $\eta_T$ is an experimentally derived parameter.

If the avalanche is triggered by the thermally generated carrier and it causes the undesirable dark count. The dark count rate, the number of avalanche per unit time due to the thermally generated carrier is known as dark count rate, $DCR_{Th}$, is given by

$$DCR_{Th} = P_{tr} \times CGR_{Th} \tag{2.5}$$

where $P_{tr}$ is the avalanche triggering probability for a carrier.

#### 2.2.1.2 Band-to-Band Tunneling

The breakdown voltage of SPADs fabricated in deep sub-micron processes reduces due to higher doping concentrations. Furthermore, the junction dimensions become smaller causing higher electric field. Since the potential barrier between the valence band and conduction band reduces, higher electric field causes the electron to quantum mechanically tunnel into the conduction band. The carrier generation rate due to tunneling , $CGR_{Tunn}$, is given in [62]

$$CGR_{Tunn} = \frac{\sqrt{2m^*}q^2 F V_R}{h^2\sqrt{E_g}} \exp\left(-\frac{8\pi\sqrt{2m^*}E_g^{3/2}}{3qFh}\right) A_{Active} \tag{2.6}$$

where $m^*$ is the tunneling effective mass (reduced effective mass), q is the electron charge, $V_R$ is the reverse bias voltage, $h$ is Plank's constant, F is the mean depletion region electric field, and $E_g$ is the silicon bandgap energy.

The band-to-band tunneling causes avalanche resulting in $DCR_{Tunn}$ and given in [59]

$$DCR_{Tunn} = P_{tr} \times CGR_{Tunn} \tag{2.7}$$

where $P_{tr}$ is the avalanche triggering probability for a carrier.

#### 2.2.1.3 Minority Carrier Diffusion

The minority carrier generated outside the multiplication region i.e., at the neutral region, diffuses to the depletion region with a collection probability. The collection probability depends on the carrier mobility, diffusion constant, and recombination lifetime [63]. Therefore, free carriers are generated due to the minority carrier diffusion that can trigger avalanche. Prior study, presented in [63], shows the effect of this phenomena is negligible. The number of generated carrier in this process is 2-3 order of magnitude smaller than other carrier generation mechanisms.

### 2.2.2 After-pulsing

Due to the semiconductor impurities and defects, there exists deep energy levels in the depletion region intermediate between the mid-gap and the band-edge. Carriers

are captured in the deep energy level during the avalanche and release later with significant delay. During the time between the quenching the avalanche and resetting the SPAD biasing above the breakdown voltage (hold-off time), the SPAD is unresponsive to these carriers. However, if the carriers are released during resetting the SPAD biasing voltage above the breakdown voltage, they can re-trigger the avalanche process resulting in a comparable false pulse. This type of noise is known as after-pulsing (AP) dark noise and is unique to the SPADs. The avalanche current density and duration, and the hold-off time duration affect the AP performance. If the holding time is longer, more trapped carriers are released during the SPAD is biased below the breakdown voltage. Therefore, the effect of after-pulsing on the dark count rate is reduced [53]. However, the number of maximum counting rate is reduced with longer hold-off time. Therefore, there is a trade-off between the hold-off time and the maximum counting rate. The effect of after-pulsing, AP, on dark count rate, DCR, is given by [40]

$$DCR = \frac{DCR_0}{1 - P_{AP}} \tag{2.8}$$

where $DCR_0$ is the dark count rate without after-pulsing effect i.e., the DCR with a very long hold-off time [64, 65], and the probability of after-pulsing is represented by $P_{AP}$.

### 2.2.3 Mitigating Premature Edge Breakdown

In order to function accurately, the device structure must be designed delicately for SPADs. It is well known that the electric field is higher at sharp edges. Thus diodes exhibit higher field regions and lower field regions throughout the junction [41]. Therefore, only small portions of the diode will undergo breakdown leading to lowered efficiency. This premature edge breakdown, PEB, is one of the main issues facing CMOS SPADs [1, 40, 41, 55–57]. Therefore, the edge of the diode must be protected to prevent the PEB problem.

In order to prevent the premature breakdown and decrease the tunneling effect while complying with the design rule and technological rule restrictions in standard CMOS process, a wide variety of guard ring structures for SPAD have been reported [66]. Placement of deep diffused p-well implants around the boundary of shallow p+ implantation in n-well has been reported in HV CMOS process to mitigate the PEB (Figure 2.3) [45, 46, 67]. An isolated p-well region formed by exploiting the lateral diffusion of two closely placed n-well region works as a guard-ring reported in literature for the process in which p-well inside n-well is not permitted. Figure 2.3 shows the use of guard ring to mitigate PEB reported without any additional processing reported in [45]. In order to mitigate the PEB, a combination of gate to control the doping concentration and a filed bounded guard ring is employed in [68].

Nevertheless, the use of guard ring adversely affects the fill factor, the ratio between the optically sensitive area to the total detective area [47, 48]. Positioning

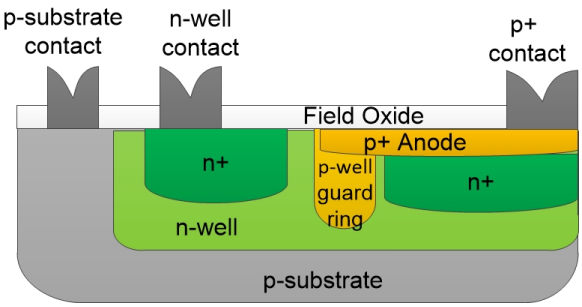



**Figure 2.3:** The anode is surrounded with a guard-ring to prevent premature breakdown [69].

n-wells closer together than allowed by the design rules allows for diffusion to occur, allowing the p-substrate to become a lightly doped n-type region. This along with a gate to control the depletion region mitigated PEB [47, 49] (Figure 2.4). These methods all rely on controlling the carrier concentration (both before and after fabrication) and the shape of the junction [49].

For SPADs fabricated in deep-submicron CMOS processes, the junction's geometry has been altered by taking advantage of the design rules for STI to prevent early breakdown [50]. Guard ring structures employing special p-well passivation implants around the STI peripheries have been used to avoid the adverse effect of STI in deep sub-micron process [70, 71]. Process stop-masks for STI such as polysilicon gate adjacent to the active region periphery have also been used to mitigate the adverse

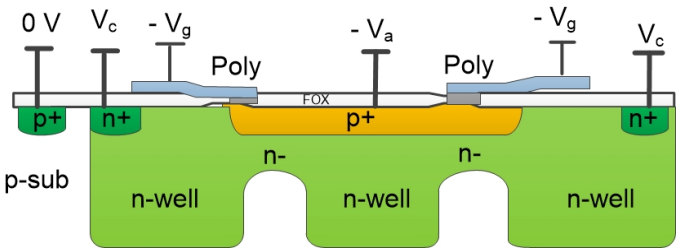



**Figure 2.4:** Lateral diffusion of two adjacent n-wells creates a lighter doped region at the edges of the junction and a poly control gate further depletes the surface to prevent premature breakdown [49].

effect of STI [41,72,73]. For example, the junction's geometry has been altered in [74] where STI has been used by taking advantage of the design rules to avoid the PEB (Figure 2.5).

Niclass *et al.* has used a guard ring of p-well around the p+ anode to prevent the premature breakdown (Figure 2.6) [50]. The fabricated SPAD was octagonal shape and used a p+/n-well junction with a guard ring around the anode.

In order to reduce the noise and have better yield, smaller active area for SPADs are encouraging. However, small SPADs results in lower pixel fill factor, particularly with in-pixel readout circuitry, reducing detection efficiency. Therefore, there is a trade off between the fill factor and noise performance. Most of the solutions for deep sub-micron processes tend to increase the size of the device. Premature edge breakdown can be mitigated by placing a perimeter gate on top of the junction and regulate the electric field through the applied gate voltage without unduly enlarging the device area [41, 42]. The addition of this perimeter gate creates a new device

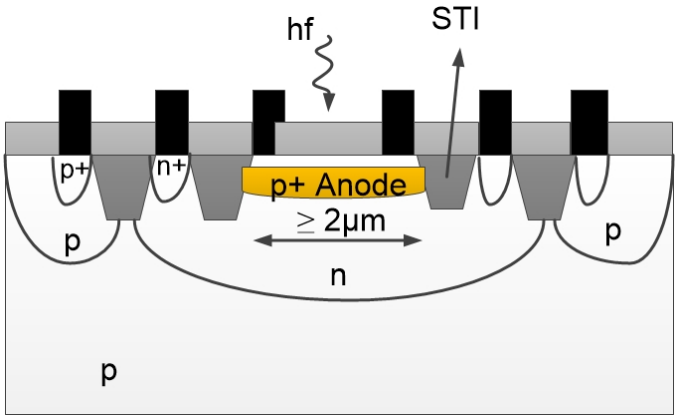



**Figure 2.5:** The silicon-dioxide trenches confines the p+ drain implant, thereby ensuring a planar junction and a uniform avalanche breakdown [74].

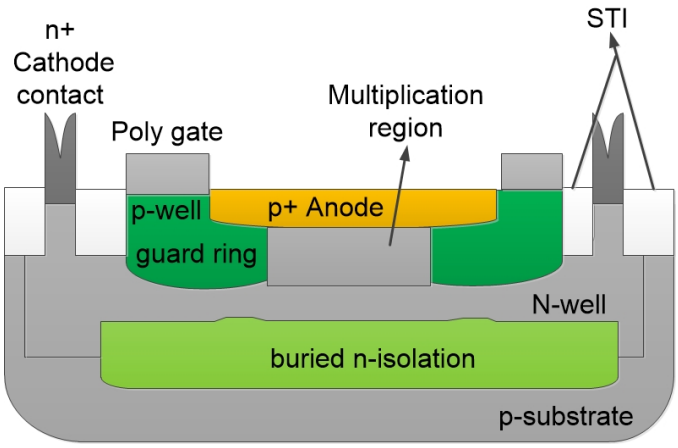



**Figure 2.6:** A guard ring of p-well around the p+ anode within n-well cathode is used to prevent premature breakdown [50].

known as the perimeter gated single photon avalanche diode (PGSPAD). SPAD with an additional perimeter gate is explained more in detail in the next chapter.

### 2.2.4 Photon Detection Efficiency

In order to detect a photon, it is required that the primary carrier generated by the absorbed photon triggers the avalanche. The photon detection efficiency is represented by the ratio of the number of detected photons to the number of incoming photons. The detection efficiency is determined by the product of absorption efficiency, the probability to trigger avalanche, and geometric fill factor (FF) [65, 75].

#### 2.2.4.1 Absorption Efficiency

In general, the incoming photon must be absorbed in space charge region to trigger avalanche. However, the photons are absorbed in the quasi-neutral region (within a few diffusion lengths of depletion region) and generates carriers. The photo generated

minority carriers in the neutral region potentially diffuses into the depletion region and trigger avalanche. Therefore, the absorption coefficient increases. The absorption efficiency is defined in [Zappa principle paper]

$$\eta = \Big(1 - P\Big) exp(-\alpha D) \Big(1 - exp(-\alpha W)\Big) \tag{2.9}$$

#### 2.2.4.2 Avalanche Triggering Probability

The probability that an electron-hole pair triggers a self-sustaining avalanche is measured by the avalanche triggering probability.The probability that a hole generates an infinite number of carriers, $P_p(x)$, and the probability that an electron generates an infinite number of carriers, $P_n(x)$, are defined in [76]

$$\begin{aligned} \frac{\partial P_p}{\partial x} &= -\Big(1 - P_p\Big)\alpha_p\Big(P_n + P_p - P_n P_p\Big) \\ \frac{\partial P_n}{\partial x} &= \Big(1 - P_n\Big)\alpha_n\Big(P_n + P_p - P_n P_p\Big) \end{aligned} \tag{2.10}$$

If the electric field profile is known, the triggering probability, $P_T$, can be determined by integrating eqn. with boundary condition that Pn(0)=0 and Pp(W) = 0 i.e., the avalanche triggering probability is zero outside the depletion region. Since the impurity doping profile shapes the electric field, the device structure affects the triggering probability. The triggering probability increases with the excess bias voltage, the difference between applied bias voltage and the breakdown voltage.

### 2.2.5 Time Resolution

The timing of the photon arrival with picosecond accuracy is desired for time resolution applications such as fluorescence lifetime imaging (FLIM), time-off-flight (ToF) positron emission tomography (PET), and Raman Spectroscopy (RS). However, there is a delays with statistical distribution between the true photon arrival time and the time when output pulse is detected. The delay causes the timing jitter known as time resolution for SPAD.

The TR can be estimated by using a laser pulse source directly coupled to the detector. The SPAD response curve, histogram of the statistical distribution of the delay between the laser pulse input signal and the SPAD output pulse measured through a multi-channel analyzer is collected with a timecorrelated single-photon counting (TCSPC) set-up [77]. The timing resolution is usually quoted by the full-width at half maximum (FWHM) of the curve. the curve has short peak followed by a slow tail. The peak is due to the photons absorbed in the space charge region and its width depends on the statistical variation of the avalanche build-up time [3, 77]. The minority carriers, photo-generated in the neutral region below the space charge region that reach the junction by diffusion causes the tail.

In order to trigger the avalanche, photo-generated carriers must drift (or diffuse) from the absorption point to the depletion region. The delay from the absorption time to the triggering time has statistical variations resulting in the SPAD timing jitter. When the electric field is higher at depletion region, carriers in the depletion region

drift faster and the triggering probability is higher. Since electric field is higher at higher excess bias voltage, the time resolution becomes better at higher excess bias.

## 2.3 SPAD Models for Circuit Simulation

This review of state of the art SPAD models for circuit simulation was reported earlier in [78]. In order to assure the proper static and dynamic behavior associated with the front-end circuit, comprehensive and accurate models are required for circuit simulation.

The SPAD models aim to represent the equivalent circuit representation of the SPAD for circuit level designs and simulation. Passive circuit components, and in some cases behavioral current sources and/or behavioral voltage sources are included in the model to reproduce static I-V characteristics and Geiger mode dynamic characteristics. These models provide a first order estimation of performance at the circuit level and allow simulation of readout circuits based on the electrical characteristics of SPAD [42, 59, 79–84]. The readout delays, time constant for both quenching and reset can be calculated using the models.

Traditional SPAD basic model reported in [80] includes voltage sources, resistors and capacitors to represent the diode characteristics (Figure 2.7). In the model, the diode resistance, $R_D$, includes both space charge resistance and resistance of neutral regions crossed by the avalanche current. $C_{AC}$ represents the junction capacitance and $C_{AS}$ and $C_{CS}$ represents the stray capacitance from anode and cathode respectively.

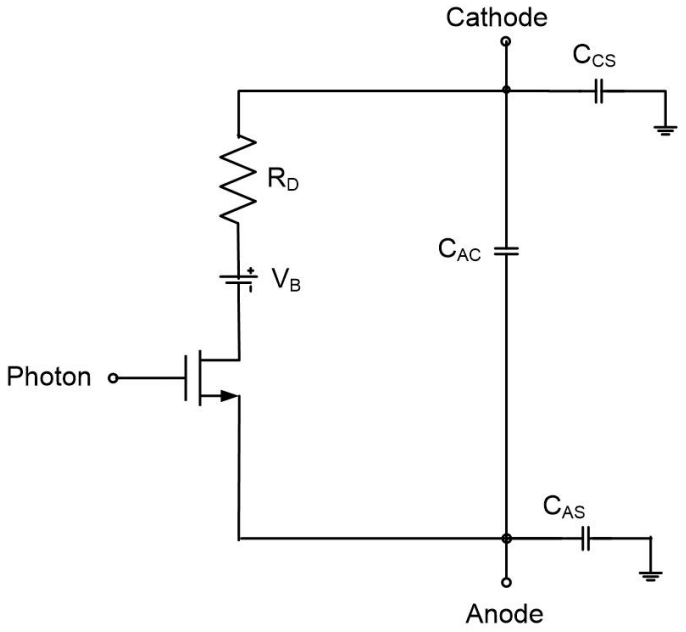



**Figure 2.7:** Traditional SPAD basic model where closing the transistor switch imitates the avalanche triggering [80]

The closure of n-MOS switch simulates the triggering of an avalanche due to photon absorption or other phenomenon including thermal generation or band-band-band tunneling.

Figure 2.8 shows the improved version, which includes the triggering, the self-sustaining process, and the self-quenching of the avalanche by incorporating of current-voltage controlled switches [85]. In order to represent the nonlinear I-V characteristics above breakdown, the model includes nonlinear voltage generator, $V_{SPAD}$, to generate piecewise linear curve with different slopes.

An accurate model for SPADs [86] exploits the behavioral description of the sensor with biasing circuits and is implemented by using Verilog-A description language. The model aims to provide optimal biasing circuit design through SPAD simulation.

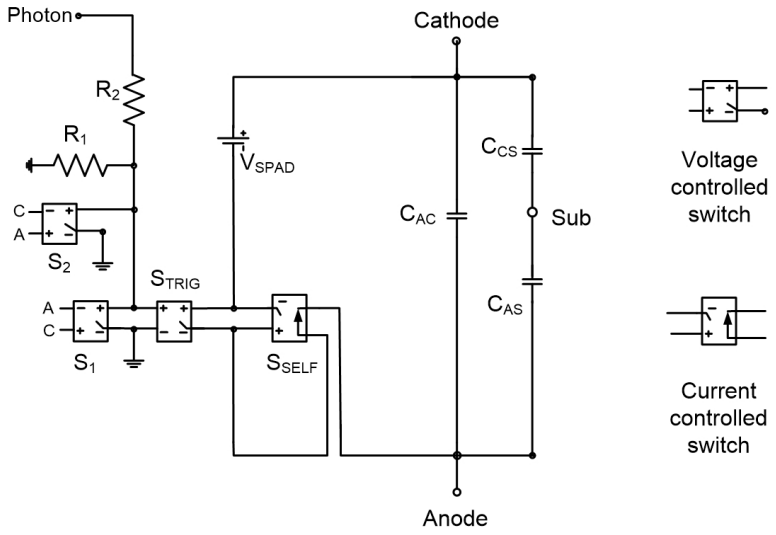



**Figure 2.8:** Improved SPAD Model [85]. Switch $S_{TRIG}$ is used to trigger the detector through "Photon" input, $S_{SELF}$ is used to include self-sustaining and self-quenching of the avalanche, and $V_{SPAD}$ represents the nonlinear I-V curve.

In order to represent the SPAD above breakdown and with the avalanche triggering and self-quenching mechanisms, a complete SPICE circuit model for SPAD has been presented in [54]. The SPAD is implemented using a piecewise non-linear approximation and modeled through a non-linear series resistance above breakdown. The model also includes the forward region and the secondary breakdown due to edge-junction or punch- through effects (Figure 2.9).

SPAD stochastic phenomena affects the switching behavior of the device and defines the transition of switch from no-avalanche to the avalanche (turn–on) and the opposite one (turn-off). In order to provide a more realistic simulation platform, models [85, 87, 88] include stochastic nature of Geiger mode operation which was not included in the earlier models [82–84]. The behavioral model (Figure 2.10) presented in [89] simulates the noise model due to dark count rate and after pulsing based on fabricated component for the first time.

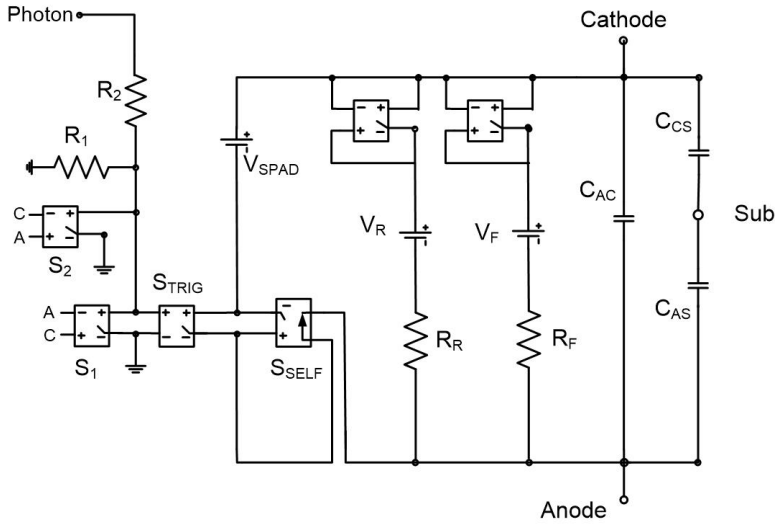



**Figure 2.9:** Complete SPAD Model [54] with switches $S_{TRIG}$ and $S_{SELF}$ representing avalanche triggering and self-sustaining. Two additional branches are included to represent forward and reverse biasing.

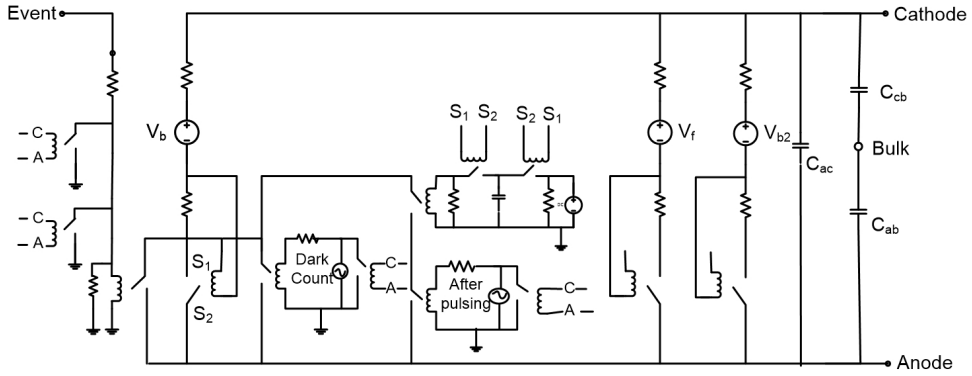



**Figure 2.10:** SPAD behavior model including I-V behavior and noise sources (dashed area)for dark counts and afterpulsing [89]

The model improves the previous circuit model [84] by adding the noise sources of avalanche photodiode . The model has been developed using Spectre active and passive components to represent the unwanted after-pulse and dark count events. At first, the parasitic capacitors of the sensors (anode-cathode capacitor, anode-bulk and the cathode-bulk capacitors) are included to represent the dynamic behavior. Three different branches representing forward, reverse and effects of noise behavior are incorporated to simulate the I-V behavior. Each branch is controlled by an ideal voltage controlled switch. Finally, the two noise sources, represented with the two corresponding branches are added to the design to simulate the noise effect.

An accurate behavioral model reported in [59] using Verilog-A hardware description language models the major statistical behaviors of SPADs including the turn-off probability, dark count rate and afterpulse phenomena. One the major focus of the model was to explore the dependence of the device capacitance on the reverse bias.

SPAD is unresponsive to any subsequent photons after detecting the first photon (during avalanche, quenching and resetting cycle) until it is reset back to undergo another avalanche. This time duration is known as dead time. In order to accurately interpret the SPAD measurements, dead time needs to be taken into account especially for large arrays of CMOS SPAD based detectors. In [82], a dead time model was reported for externally reset SPADs. The model is based on assumption that the time distribution of incidents counts in the device is Poissonian. Using the model, the photon detection efficiency can be measured accurately due to the dead time compensation included in the model.

Another probabilistic model [83] derive the signal-to-noise ratio based on photon detection efficiency, dark count rate, and after pulsing probability. Then Monte Carlo simulation has been performed to validate the derived model.

## 2.4 SPAD Front-End Readout Circuits

The basic function of the front-end circuit is to sense the leading edge of the avalanche current and produce a standard output pulse synchronized to the avalanche increase. In order to reduce charge trapping and power dissipation, avalanche current must be of very short duration. Therefore, quenching needs to be timely. Finally, the bias voltage of the SPAD must be reset back to above the breakdown voltage after a sufficient hold-off time. This reduces the triggering probability during the voltage reset phase [53]. The primary goals of the front-end circuit design are to promptly sense the avalanche and to reduce the avalanche charge.

### 2.4.1 Passive Quenching-Reset

Since SPAD operates in Geiger mode, once it is triggered the large avalanche current continues on flowing. Therefore, the device becomes useless for subsequent detection of photons.The purpose of the quenching circuit is to stop the avalanche process by reducing the voltage across the device below the breakdown voltage and bring back the SPAD device into its original quiescent state next.The time duration between the starting of the avalanche and ending the avalanche is known as quenching time. After

quenching the time required to bring back the SPAD to its initial ready state is called reset time.The aspects of the quenching circuit influences the operation of the device completely and the performance achievable from the device. Passive quenching-reset circuits are the most commonly used quenching circuit due to their compactness and resulting in improved fill factor, simple structure and reduced parasitic (Figure. 2.11) [40]. The passive quenching-reset circuit composes a series load resistor ($R_L$), a high-value ballast resistor, connected to the SPAD. At first, the SPAD is biased above the breakdown voltage, $V_{Br}$ through the $R_L$. When the photon arrives the avalanche is triggered due to the impact ionization. The current increases rapidly to its maximum value. As a result, the parasitic capacitance, $C_P$ connected at the cathode discharges. The bias voltage across the SPAD reduces exponentially towards zero. The quenching time constant, $\tau_q$ is given in [53]

$$\tau_q = C_P\Big(R_S||R_L\Big) \cong C_P R_S \tag{2.11}$$

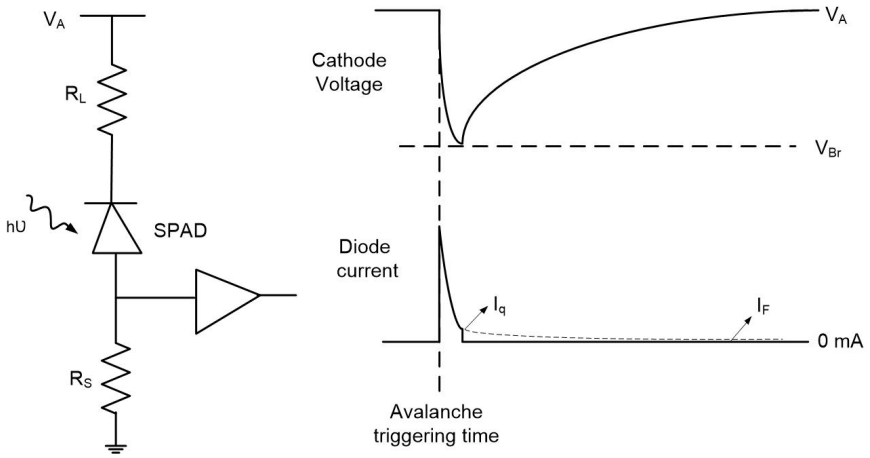



**Figure 2.11:** Schematic of a basic passive quenching-reset, PQR, circuit (left) and the cathode voltage and diode current for a SPAD connected to a PQR (right) [53].

where, $R_S$ is the SPAD's series resistance and $R_L \gg R_S$ .

However, the overall bias voltage across the SPAD never reduces below the breakdown voltage and the avalanche is not quenched completely. The current persists to flow through the device. The final value of the current. $I_F$ is

$$I_F \simeq \frac{V_{Exc}}{R_L} \tag{2.12}$$

If $I_F$ is greater than the quenching threshold current level, the latching current of 100 $\mu$A, the avalanche is self-sustaining. When the $I_F$ falls below the quenching threshold current level, the avalanche is self-quenching. Since the avalanche process is statistical, the quenching time is statistical also. The quenching threshold current sets a minimum value of ballast resistor. The quenching time is given in [53]

$$t_q = \tau_q \ln\left(\frac{I_0 - I_F}{I_q - I_F}\right) \tag{2.13}$$

where $I_0$ represents the peak initial avalanche current ($\frac{V_{Exc}}{R_S}$), $I_q$ is the quenching threshold current.

The total charge of the avalanche pulse, $Q_p$, is a critical parameter to estimate the trapping effect. The relation between $Q_p$ and time constant of voltage recovery, $\tau_r$, is defined in [53]

$$Q_p = V_{Exc} C_P = I_F.\tau_r \tag{2.14}$$

The time constant of voltage recovery, $\tau_r$, can be defined as

$$\tau_p = R_L C_P \tag{2.15}$$

One of the major problems with passive quenching-reset circuit is that the biasing reset time is very slow resulting in the possibility of avalanche triggering during the reset and a limited counting rate. Moreover, quenching time is not well defined in passive quenching-reset. Despite the disadvantages, the passive quenching-reset circuit is very useful for applications requiring small area and for large arrays with high fill factor.

MOS device (PMOS or NMOS) is used as quenching resistor to improve fill factor. Figure 2.12 shows the schematic of four different active device passive quenching options where PMOS is used as quenching resistor in Figure 2.12 (a), (c) and NMOS is used as quenching resistor in Figure 2.12 (b), (d).

### 2.4.2 Active Quenching-Reset

In order to avoid the disadvantages of the passive quenching-reset, active quenching-reset (AQR) has been reported in [53]. Active quenching-reset (Figure 2.13) provides superior performance in terms of count rate [90], after-pulsing [80, 91] while reducing fill factor. The fill factor can be improved by placing active quenching-reset circuit exterior the pixel's boundary and using a shared n-well for all the SPADs in the single pixel [20, 70].

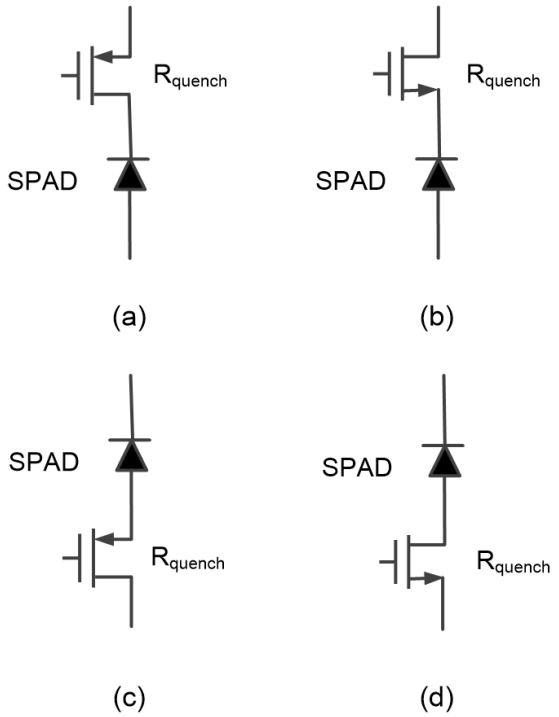



**Figure 2.12:** Schematic of different active device passive quenching.

In active quenching-reset, the biasing voltage is reduced below the breakdown voltage different from the passive quenching-reset. Therefore, the statistical variation of the avalanche multiplication does not influence the quenching time. The bias voltage is controlled to act on the device after detecting the avalanche. The bias voltage is retained below the breakdown voltage for the hold-off time and then reset back to the idle state. The quenching and reset are performed using active components and the avalanche is detected through the low impedance.

The basic schematic of the active quenching-reset is shown in Figure 2.13 with the pulse generator as the active circuitry and the cathode voltage and diode current for the SPAD with active quenching-reset circuit. The total charge of the avalanche pulse for the active quenching-reset, $Q_p$ is defined in [53]

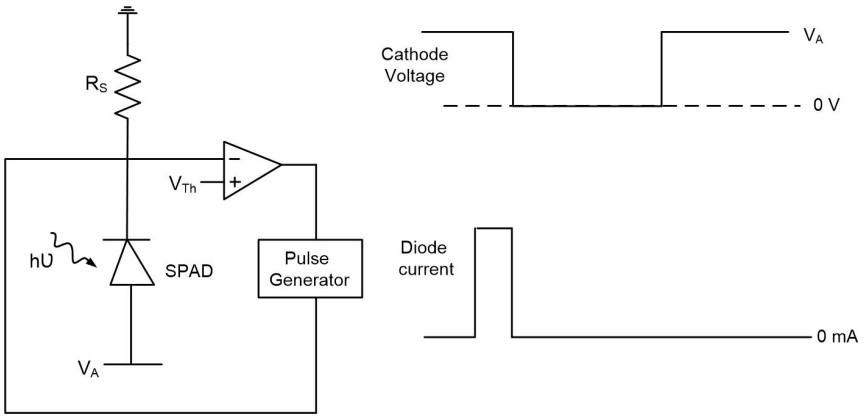



**Figure 2.13:** Schematic of the basic active quenching-reset circuit (left) and the cathode voltage and diode current for a SPAD connected to a AQR (right) [53].

$$Q_p = I_0 t_q = \frac{V_{Exc}}{R_S} t_q \tag{2.16}$$

where $I_0$ represents the peak initial avalanche current ($\frac{V_{Exc}}{R_S}$), $t_q$ is the quenching time, $V_{Exc}$ is the excess voltage, threshold current, and $R_S$ is the sensing resistor.

Although the quenching transition is faster, the overall quenching time is not so small. The AQR has to detect the avalanche and arbitrate literally before quenching the avalanche. During the wait time for active quenching, the avalanche current continues to flow leading to power dissipation and increasing the afterpulsing.

### 2.4.3 Mixed Active-Passive Quenching-Reset

In order to avoid the problems associated with passive quenching reset and active quenching reset, mixed active-passive quenching integrate the advantages of both quenching circuits. The SPAD is connected both to a large ballast resistor and active quenching and reset circuitry. Figure 2.14 shows the basic diagram of the mixed

active-passive quenching reset circuit. The switches are used as active circuitry. When the avalanche triggers, the current flows through the ballast resistor. Therefore, passive quenching takes place to quench the avalanche at first. The active quenching circuitry detects the avalanche shortly and begins the active quenching. The circuit acts like an AQC after that. Therefore, SPAD is quenched for hold-off time and reset to the operating bias voltage. The cathode voltage and diode current for a SPAD connected to a mixed active-passive quenching reset is shown in Figure 2.14.

This quenching circuit provides the benefits of a fast recharge and well-defined dead time similar to AQR circuit. Furthermore, the total avalanche charge is equal to that of PQR at most. If the active quenching arbitration delay is shorter, the avalanche charge is lower than that of PQR. The quenching time is the lowest between the active quenching arbitration delay and the passive quenching threshold crossing. The active quenching delay, $t_q$, for shorter delay is defined in [53],

$$t_q < \tau \ln\left(\frac{I_0 - I_F}{I_q - I_F}\right) \tag{2.17}$$

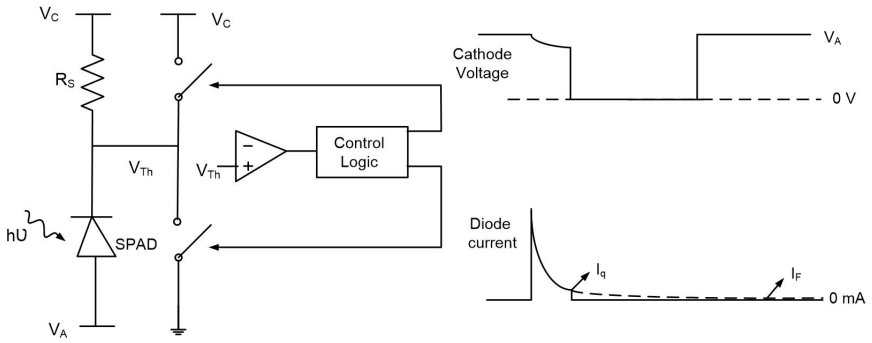



**Figure 2.14:** Schematic of the mixed active-passive quenching reset circuit (left) and the cathode voltage and diode current for a SPAD connected to a mixed active-passive quenching reset (right) [53].

where $I_0$ represents the peak initial avalanche current ($\frac{V_{Exc}}{R_S}$), $t_q$ is the quenching time, $I_q$ is the quenching threshold current, and $I_F$ is the final current similar to PQR.

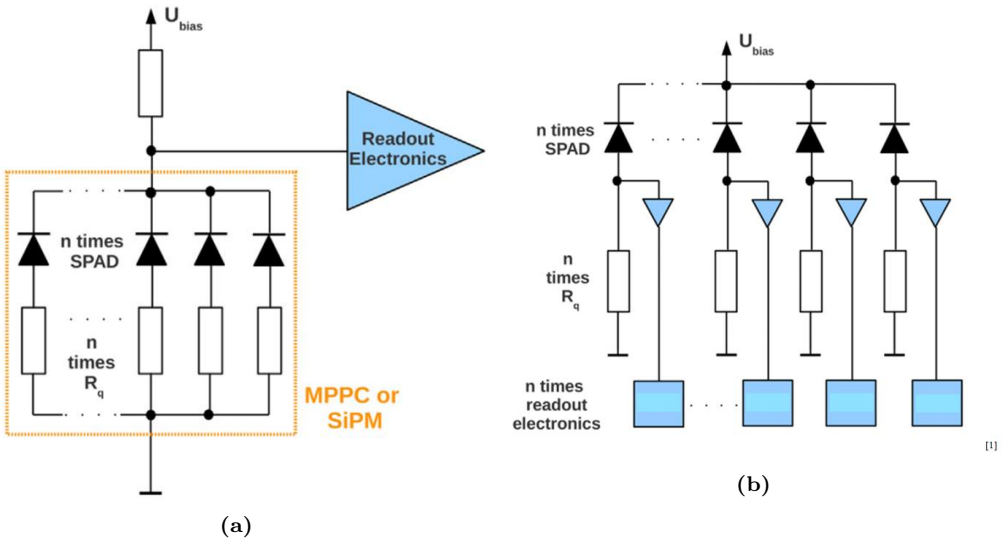
## 2.5 Silicon Photomultiplier

Silicon photomultipliers (SiPMs) are a particular type of solid-state detector that has been showing a great promise as an alternative to photomultiplier tubes (PMTs) in positron emission tomography (PETs) applications. In PETs, the scintillator is used to absorb the incoming gamma or neutron photons and then emits the light photon that are detected by photodetector. SiPMs are chosen due to their compactness, ruggedness, low operating voltage, and tolerance to magnetic fields. SiPMs consists of a large array of Geiger mode single photon avalanche diodes (SPADs). SiPMs may be classified as one of two types, either analog or digital. An analog SiPM composes a large array of parallel SPADs with a series resistor biased in reverse breakdown (Figure 2.15 (a)).

The current of all the avalanching SPADs are summed to generate the total output current in analog SiPM. Analog SiPMs are susceptible to noise variation and are highly sensitive to temperature variations due to signal degradation from the parasitics of interconnects, bonding wires, and external loads [9,11]. Furthermore, the analog-to-digital (A/D) conversion is only implemented at the final summed output current though readout electronics, the built-in photon counting capability of SPADs is not fully achieved in analog SiPMs.

A SPAD's output spike is an all or nothing signal due to a single photon initiating the avalanche process, and thus is intrinsically digital. If each individual SPAD has a digital output instead of an analog output, the noise performance can be enhanced significantly, giving rise to the recent advancements of digital SiPMs (Figure 2.15 (b)) [9,11,13,20], digital SiPM, and it is used in medical imaging, radiation detection, and high energy physics applications [14–19, 22–25]. Furthermore, digital SiPMs implemented in CMOS, as opposed to a dedicated optical process, allows the optical sensor to be coupled on the same chip with electronics to implement the digital functions such as pulse counting and time-stamping. Therefore, the cost for time-of-flight (TOF) PET systems is lowered remarkably with improved noise performance.

In [10], one of the first digital SiPM has been reported for PET applications which consists of an array of 2×2 pixels. Each pixel comprises 64×32 SPADs. The test has been carried out in a PET setup coupled to a $3\times\ 3\times\ mm^3$ scintillation crystal. Active




(a) (b)

**Figure 2.15:** SiPM (a) Analog SiPM where total current is measured as output (b) Digital SiPM where total count rate is measured as output.

quenching reset is used as front end SPAD readout circuit with fill factor of 50 %. A single TDC is integrated in the same chip that is shared by all pixels reducing I/O data rates. An acquisition controller is included to secure that only scintillation events are counted and time-stamped. In order to avoid false TDC triggering due to dark counts and reduce skew, a configurable-threshold trigger logic is implemented.

Another digital SiPM for PET applications has been reported in [35] that aims to improve fill factor. The digital SiPM includes in pixel data compression schemes, temporal and spatial compression. The array comprises 14×10 pixels implemented in a HV CMOS 0.35$\mu$m process. Each pixel includes 32 SPADs and a 4-bit digital counter. The achieved fill factor was 29 %. The fill factor is bounded by the size of the SPAD and the area takes up by the SRAMs of SPAD. In order to calculate the arrival time of the first photon in each column, one TDC per pixel column is incorporated.

When a single TDC is implemented in digital SiPM, only one timestamp per photon event is attainable. In order to achieve an improved evaluation of photon arrival time, multiple timestamps are necessary for each photon event [9, 20, 92, 93] . The digital silicon photomultiplier reported in [9] has been divided into columns. In order to enhance the timing resolution of single-photon detection, a column-parallel time-to-digital converter (TDC) was included in each column. The pixel-to-pixel skew is lessened by decreasing the number of pixels per TDC using a sharing scheme with three TDCs per column. The digital SiPM consists of an array of 16×26 pixels with

fully integrated 48-fold column-parallel TDC. The achieved temporal resolution is 51.8 ps and the fill factor is 21.2 %.

In [20], a new digital SiPM, an array of 8×16 pixels, using CMOS mini-SiPMs for PET applications is reported. Each pixel consists of 4 independent 180 SPAD mini-SiPMs with a full chip fill factor of 35.7 % and pixel fill factor 42.6%. In order to detect the temporal, spatial, and energy information of the scintillation event efficiently, a double threshold algorithm was employed. For each gamma detection, the pixel provides the total detected energy and a timestamp, achieved using two 7-b counters and two 12-b 64-ps TDCs. An adder tree overlaid on top of the pixel array adds the sensor total counts at up to 100 Msamples/s. The sums are then employed to detect the asynchronous gamma events on-chip. The output is also available in realtime. The detection performance was characterized with a $3 \times 3 \times 5\ mm^3$ LYSO scintillator. The achieved energy resolution of 10.9 % at 511-keV and a coincidence timing resolution of 399 ps.

## 2.6 Silicon Photomultiplier Readout Techniques

Readout electronics is an indispensable part of the detection system using SiPM. Integrating this essential part on the same chip is one of the main reasons why CMOS detectors are so popular. The integration of SiPMs and the required readout circuitry into CMOS technology has significantly improved the level of miniaturization of SiPMs and thus paved the way for large SiPMs arrays required for PET applications.

The readout circuitry varies with the type of SiPM and application. The state of the art SiPM readout circuits are presented in this section. In this section different readout techniques are briefly discussed.

### 2.6.1 Readout Techniques for Analog Silicon Photomultiplier

In analog SiPM, the SPAD cells each with the quenching element are connected in parallel and the output signal is the analog sum of the individual current of all the connected SPAD cells.

A transimpedance amplifier is used to convert the output current into corresponding voltage signal. In order to obtain the best possible timing performance with SiPMs, dedicated transimpedance amplifiers are required. One of the main requirements of the transimedance amplifier is that it does not degrade the rise time and signal-to-noise ratio of the SiPM signal. While designing the transimpedance amplifier, high capacitance of SiPMs (sum of all cell's capacitance and the internal interconnect capacitance) requires to be considered. Since the output impedance of the SiPMs depends on the number of triggered cells, the amount of incident light affects the output impedance. This characteristics of SiPMs needs to be considered in designing the transimpedance amplifier as well. The required transimpedance amplifier is integrated in the same chip or added as an external readout circuit [30,34]. In order to condition and digitize the output signal of SiPM, a dedicated multichannel mixed-signal ASIC is required. Figure 2.16 shows the typical single channel readout system for the analog SiPM [10].

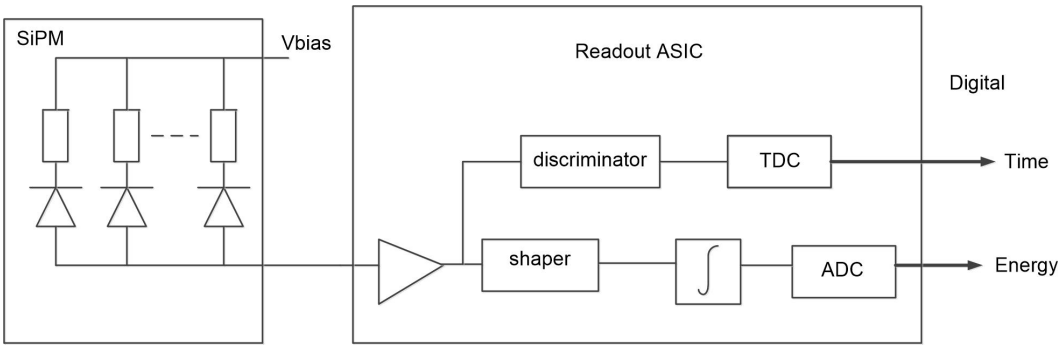



**Figure 2.16:** Schematic of analog SiPM for scintillation light detector system [10].

In [34], the designed analog SiPM consists of 16 × 16 SPAD cells organized in 4 macro-pixels each with 8 × 8 SPAD cells. All the cathodes of four pixels are combined together form the common cathode and all the anode after the quenching resistor connected together to form the common anode of an equivalent SiPM with 16 × 16 SPAD cells .

Figure 2.17 shows the SiPM form the common cathode readout circuit reported in [34] based on a transimpedance amplifier. The gain of the amplifier is determined by the feedback resistor and the stage is compensated by the feed back capacitor. The bandwidth is not limited by the readout circuits. The stray capacitances of the pn-junction defines the bandwidth of the detector.

### 2.6.2 Readout Techniques for Digital Silicon Photomultiplier

Digital SiPM takes the advantage of CMOS technology to achieve a 1-bit analog to digital conversion per SPAD using conventional CMOS circuits and to accommodate an on-chip digital accumulator to generate the sensors energy output. Furthermore, the time to digital converter(TDC) is included in the same chip to generate timing

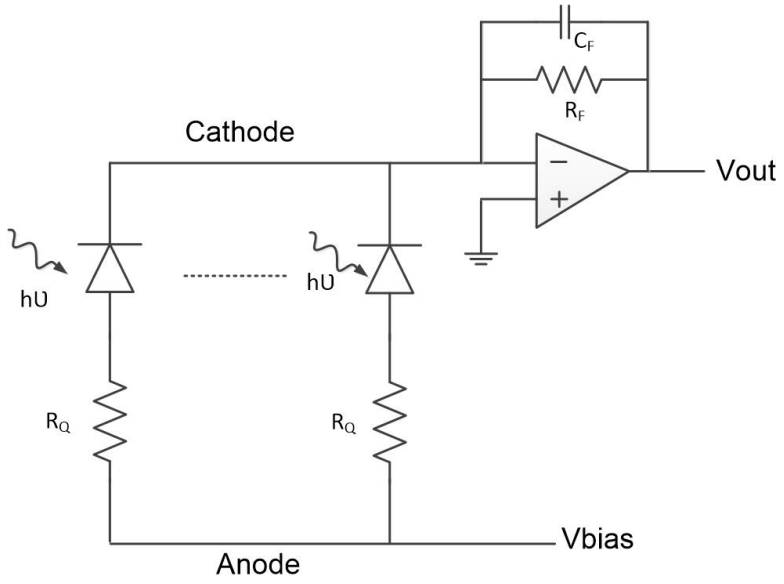



**Figure 2.17:** Schematic of CMOS Analog SiPM and readout circuitry for scintillation light detector system [34].

information. Therefore, digital SiPM implemented in CMOS technology enables on chip integration of the SiPM and processing readout circuits resulting in simplified PET systems from an electronic point of view.

One of the first fully digital implementation of SiPM based on SPAD has been reported in [10]. Figure 2.18 shows the digital SiPM with its integrated readout circuitry [10]. In order to detect the photon, a dedicated cell electronic block next to anode is used to sense the voltage at anode. The quenching and reset circuits and a one bit memory for carefully enabling or disabling the specific SPAD cell is included in the electronic block. Each cell consisting the SPAD itself and the respective electronic block is attached to the time to digital converter through a balanced and configurable network. In order to count the total number of detected photons, a photon counter is used that is connected to each SPAD cell through a different synchronous bus. A

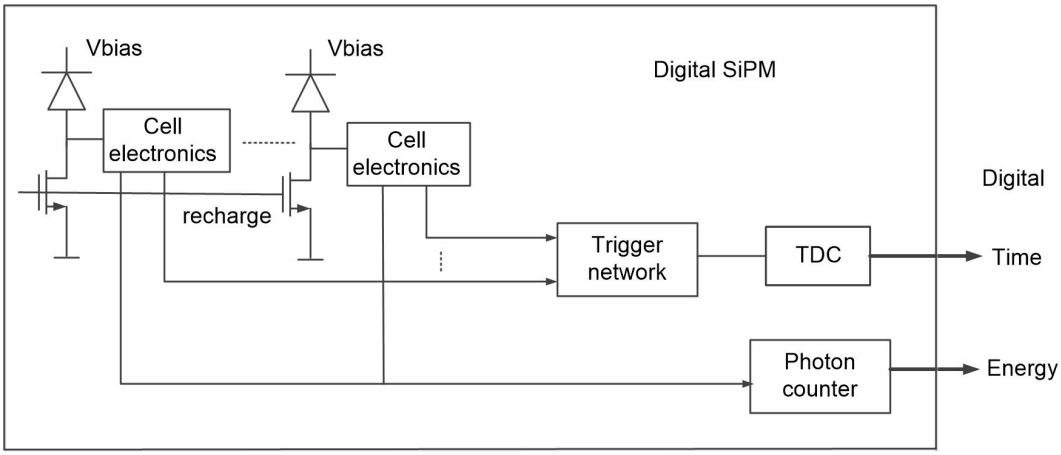



**Figure 2.18:** Schematic of digital SiPM for scintillation light detector system [10].

CMOS mini-SiPM with individual SPAD digitization and in-pixel data compression to improve fill factor has been reported in [35]. In order to improve the timestamp information per photon event, the readout circuitry includes column level TDC that obtains the time of arrival of the first photon in each column. The mini-SiPM consists a $14 \times 14$ pixel array where each pixel includes a mini-SiPM with 32 SPADs, a digital counter and SRAM for each SPAD to disable high DCR SPADs. Figure 2.19 shows the block diagram of the compression schemes used in [35] to reduce the electronic area occupation per SPAD whereas the block diagram of a TDC connected to a group of four mini-SiPM.

In typical digital SiPM , a single time-to-digital converter is included in the chip and shared by all the pixel to reduce external component and and temporal noise. In some other digital SiPMs, a group of pixel shared the same TDC . In order to improve the timing resolution of the single photon detection, some other digital SiPMs have been reported in [9, 20, 92, 93]. For example, a column-parallel TDC is included in each column of the digital SiPM to enhance the time resolution in [9]. Furthermore,

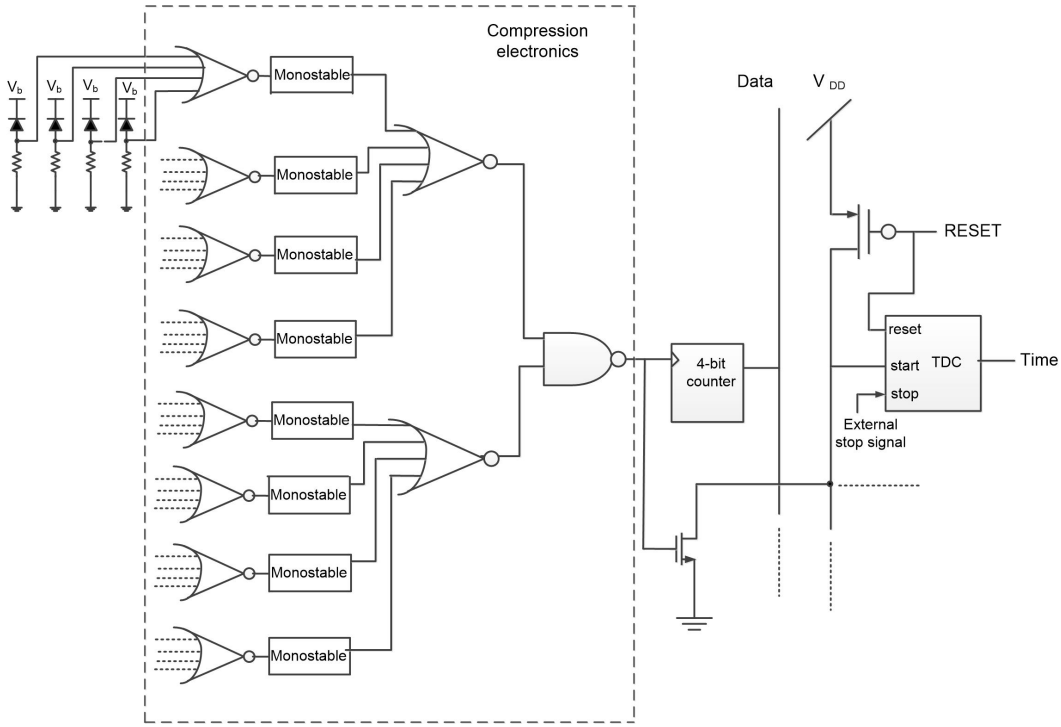



**Figure 2.19:** Schematic of mini-digital SiPM with in-pixel data compression [35].

the number of pixels sharing the same TDC was reduced further by using a sharing scheme with three TDCs per column. Figure 2.20 shows the schematic of typical digital SiPM. Figure 2.21 shows the block diagram of the multichannel digital SiPM consisting of an array of 16 × 26 pixels with the associated readout circuitry. In order to estimate the total number of detected photons, an energy register is included to readout the detected photon information. A mask register is incorporated to disable the pixels with DCR surpassing a threshold to reduce false TDC activation. A 48-fold column parallel TDC is implemented where three TDCs are used in each column to reduce number of pixel per TDC. In addition, a row decoder and precharge circuits are included in the readout circuit.

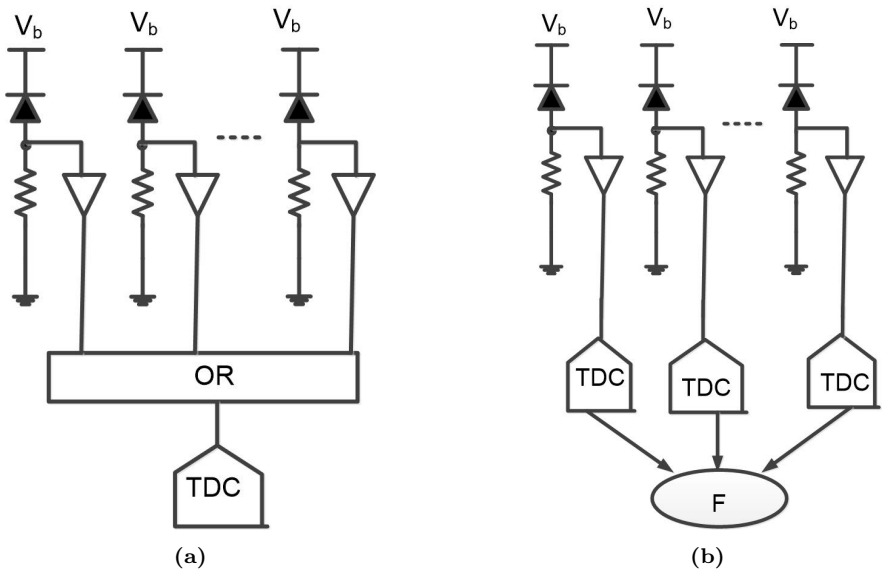



**Figure 2.20:** (a) Typical Digital SiPM where all pixels shared one TDC (b) Digital SiPM with on-pixel TDC [9].

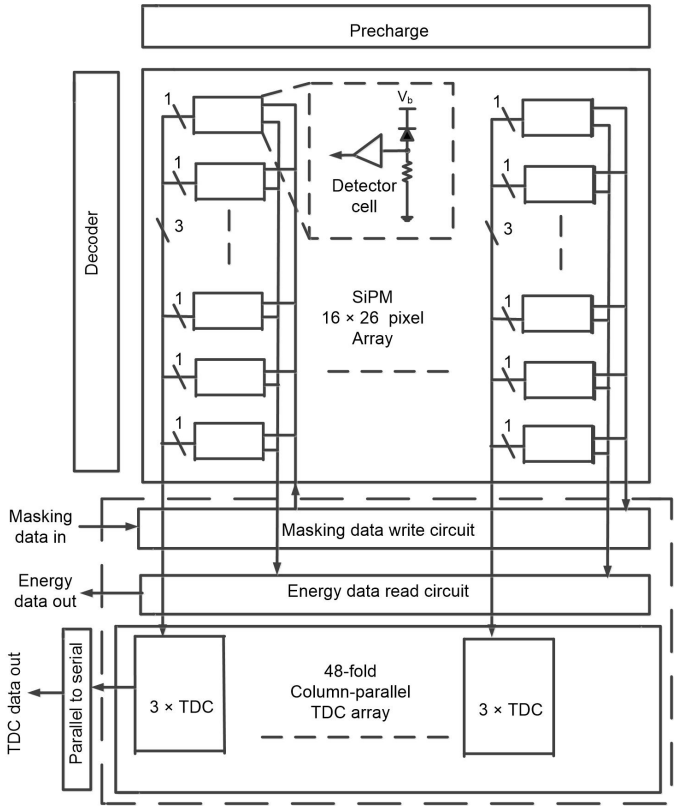



**Figure 2.21:** Schematic of digital SiPM with multichannel TDC [9].

The fully digital circuit reported in [20] is divided in three main hierarchy levels: the top-level, the pixel, and the mini-SiPM. The top level includes the control, I/O blocks and the gamma discriminator. Moving down, spatial information can be obtained from the pixel, the smallest unit. The pixel includes an array of $2 \times 2$ mini-SiPM, an energy collector and a TDC. The lowest level is the mini-SiPM consisting a $12 \times 15$ SPAD array connected to a counter. A clock is used to synchronize the works of all the levels. The counts move from the lowest level (mini-SiPMs) through the pixels and then through a distributed adder, finally arriving at the top level at each clock cycle. In order to identify a gamma event, the discriminator at the top level watches the total photon counts regularly and contrasts two successive time bins based on two thresholds. Once an event is detected, the discriminator sends back the *integrate* command to enable the pixel counting. The timestamps associated to the two discriminated time bins is stored for later use. At the end of the integration, the $freeze$ signal is sent to disable the pixel counting. Finally the full array is ready for readout.

# Chapter 3

# CMOS Analog Silicon Photomultiplier using Perimeter Gated SPAD

** **Portions of this chapter were published in:**

1. Mst Shamim Ara Shawkat, Mohammad Habib Ullah Habib, and Nicole McFarlane, *"An Analog CMOS Silicon Photomultiplier Using Perimeter Gated Single Photon Avalanche Diodes,"* IEEE Transactions on Circuits and Systems I (TCAS-I), Vol. 65, no. 11, pp. 3830 - 3841, Oct. 2018.

2. Mst Shamim Ara Shawkat, Mohammad Habib Ullah Habib, Md Sakib Hasan, Mohammad Aminul Haque,and Nicole McFarlane, *"Perimeter Gated Single Photon Avalanche Diodes in Sub-micron and Deep-submicron CMOS Processes,"* International Journal of High Speed Electronics and Systems, Vol. 27, no. 03n04, pp. 1840018-1-19, 2018.

## 3.1 Introduction

Perimeter gated single-photon avalanche diode (PGSPAD) is a p-n junction with an additional poly-silicon gate surrounding the junction [41, 42, 44, 49]. The perimeter gating technique has been proven to be an efficient method to prevent premature edge breakdown, one of the major problems in operating planar p-n junctions of avalanche

diodes implemented in standard CMOS process during avalanche breakdown [41, 42, 44, 49]. Therefore, CMOS PGSPADs adopt the benefits of commercial CMOS process such as low cost and integration capability while preventing premature edge breakdown. The effect of the applied voltage at the perimeter gate to develop a consistent electric field distribution at the junction through physical device simulation has been examined. The capability to tune the breakdown voltage for PGSPAD devices fabricated in 0.5 $\mu$m high voltage and 0.35 $\mu$m CMOS process has been verified in this work for the first time. Finally, the modulation of the breakdown voltage of fabricated PGSPAD devices in multiple CMOS processes with different vendors (0.5 $\mu$m, 0.5 $\mu$m high voltage, 0.35 $\mu$m, and 180 nm CMOS processes) has been compared. PGSPAD reduces noise in addition to preventing premature edge breakdown. PGSPAD noise has been characterized over a range of temperature with variation of the gate voltage through experiment for the first time.

A silicon photomultiplier (SiPM) consists of an array of parallel single photon avalanche diodes (SPADs) with a series quenching resistor, whose avalanche currents are added at the common node of all connected SPADs [6, 30–34]. In nuclear imaging applications, such as those using neutrons, the particle is detected indirectly through a scintillation material which emits photons. When a scintillation occurs, the total current at the output of SiPM is equivalent to the number of triggered SPADs. SiPMs are often a preferred substitute to photomultiplier tubes (PMTs) because of their immunity to magnetic field, compactness and low bias voltage. CMOS based SiPMs offer low cost, miniaturization, and improved performance by reducing parasitics

through integration of the detector and electronics in the same chip [9, 20, 40, 92]. In addition, CMOS PGSPAD SiPMs provide tunabilty of noise and sensitivity in addition of prevention of premature edge breakdown problem. A full chip analog CMOS SiPM using PGSPAD, 18 × 18 pixel array, was fabricated in standard 0.5 $\mu$m 2−poly, 3−metal CMOS process and fully characterized through experiments. The characterizations include electrical, optical, and temperature measurements. A performance comparison between the designed analog PGSPAD SiPM and state of the art SiPMs are presented. The designed SiPM was reported in [44] as first full chip analog SiPM using PGSPAD and first fully characterized.

## 3.2 CMOS PGSPAD and its Characterization

A perimeter gated SPAD (PGSPAD), a SPAD with an additional gate terminal, prevents premature edge breakdown in standard CMOS SPADs. The cross sectional view of PGSPAD device and its symbol are presented in Figure 3.1. The applied

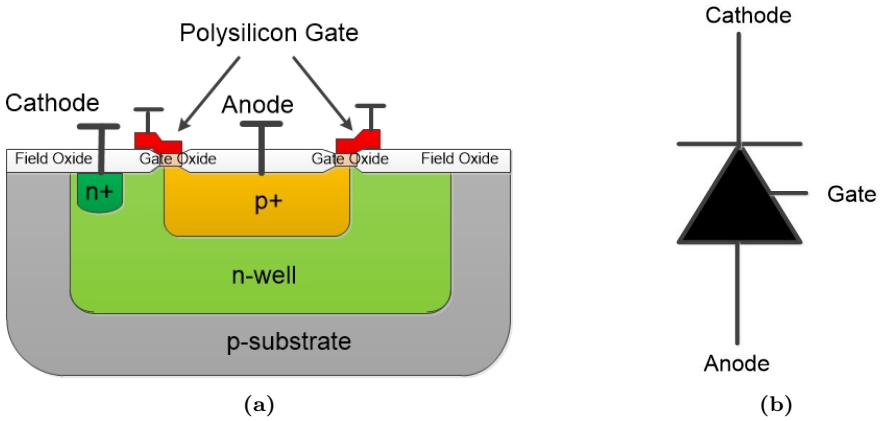



**Figure 3.1:** (a) Cross section of a PGSPAD, a SPAD with an additional polysilicon gate terminal. (b) PGSPAD symbol.

voltage at the additional gate terminal modulates the electric field making it uniform throughout the junction. PGSPAD device can be implemented with different junction type, for example psub-nwell and nwell-p+ junction type. In this work, PGSPAD device with nwell-p+ juntion type has been implemented.

### 3.2.1 Operating Principle of CMOS PGSPAD

The PGSPAD operates similarly to the SPAD with the added advantage of having a more uniform electric field around the junction due to the effect of the additional gate terminal.In order to operate in Geiger mode, the PGSPAD device is biased beyond the breakdown voltage similar to that of regular SPAD. The charge carriers are freed by the incoming photon. The free carriers are then accelerated by the high electric field generated by the high reverse bias voltage. These carriers go through the impact ionization in the depletion region producing a self-sustaining avalanche of carriers [58, 94]. The relationship between the avalanche gain, $M$, or multiplication factor and the breakdown voltage, $V_{br}$, is [95],

$$M = \left(1 - \left(\frac{V_A}{V_{br}}\right)^n\right)^{-1} \tag{3.1}$$

where $V_A$ is the applied voltage and $n$ is a process dependent constant. From equation (3.1), avalanche occurs (M $\rightarrow \infty$) when $V_A \rightarrow V_{br}$.

For a regular SPAD, when the electric field is applied across the device, the electric field is maximum at the sharp edges causing premature breakdown. In PGSPADs, the

premature breakdown can be suppressed through the applied voltage at the additional gate terminal through modulation of carrier concentration [41,44,49]. The breakdown voltage, $V_{br}$ , a parameter that is correlated with efficient SPAD operation, is defined in [96],

$$V_{br} = \frac{\epsilon_s E_{crit}^2}{2eN_B} \tag{3.2}$$

where $\epsilon_s$ is the permittivity, $E_{crit}$ is the critical electrical field at breakdown, $e$ is the charge of an electron, and $N_B$ is the doping concentration of the highly doped region.

It was experimentally verified that the breakdown voltage can be modulated using an external field at the surface. Either side of the junction can be depleted through the variation of the applied external field [97]. Therefore, the surface field tends to saturate at a maximum and at a minimum value with the variation of gate voltage. The induced field in the junction places an upper and lower limit of the breakdown voltage variation preventing further variation in shape of the depletion region. The breakdown voltage is defined between these two extremes in [49]

$$V_{br} = m|V_G| + \beta \tag{3.3}$$

where $V_G$ is the applied gate voltage, $\beta$ is a constant, and $m$ is the slope which approaches unity for small oxide thickness and low substrate impurity concentrations.

Therefore, the breakdown voltage can be changed in PGSPADs by applying the voltage at the gate based on the empirical expression. Since the performance of the

device depends on the breakdown voltage, the performance can be improved through applied gate voltage [41, 42].

### 3.2.2 Effect of Gate Voltage on Modulation of Electric Field Distribution

The effectiveness of modulation of electric field through the applied gate voltage has been verified using Sentaurus device simulation. The electric field distribution for a regular SPAD is also simulated for performance comparison. The implemented junction is a p+/n-well diode embedded in p-type bulk substrate. For the simulation, the doping profile of [41] was used and is repeated here for completeness. For the p+ region the peak concentration is $1 \times 10^{-20} cm^{-3}$ while the peak concentration for the n-well used is $1.22 \times 10^{17} cm^{-3}$ with Gaussian profile. The concentration reduces with $\sigma = 120nm$ in the lateral direction and with $\sigma = 50nm$ in the depth direction. A shifted Gaussian profile was used with a mean of 0.2 $\mu$m from the surface. For the p-substrate, the doping concentration of $1 \times 10^{15} cm^{-3}$ is used.

Simulation results presented in Figure 3.2 shows the electric field distribution for a regular SPAD without any gate terminal. Electric field shows maxima at the diode's edge. Therefore diode edge undergoes avalanche earlier compared to the other part of the junction resulting premature breakdown, one of the major problem of SPAD in CMOS process.

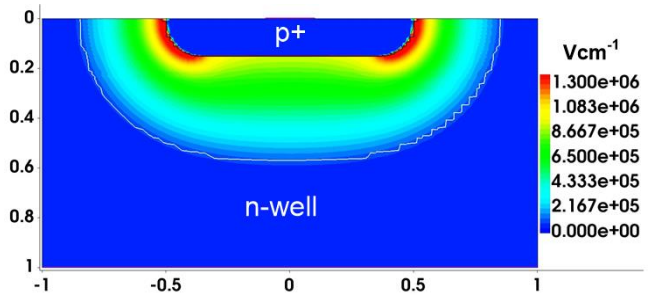



**Figure 3.2:** Simulation result of electrical field modulation of a regular SPAD (x-axis and y-axis are in $\mu$m) [98].

The electric field distribution for a PGSPAD with different applied gate voltages are presented in Figure 3.3. Figure 3.3 shows as the applied voltage magnitude at the additional gate terminal of PGSPAD increases from 0 V to 4 V, the electric field decreases at the edges and starts to become uniform throughout the junction compared to those at regular SPAD. If the applied gate voltage increases further to 8 V, the electric fields become more uniform and with 12 V the electric field distribution around the junction becomes almost fully uniform. This is due to the modulation of carrier concentration at the junction through the applied gate voltage. Therefore, the premature edge breakdown is prevented and full volumetric breakdown is achieved.

### 3.2.3 Effect of Applied Gate Voltage on Breakdown Voltage

In order to verify the effectiveness of the additional gate terminal of PGSPAD device, similar PGSPAD device have been fabricated in 0.5 $\mu$m, 0.5 $\mu$m high voltage, 0.35 $\mu$m, and 180 nm CMOS processes, with size of 22 $\mu$m $\times$ 22 $\mu$m. Particularly, the efficiency of the additional gate terminal to regulate the breakdown voltage for PGSPAD device fabricated in 0.5 $\mu$m high voltage and 0.35 $\mu$m CMOS process has been verified in

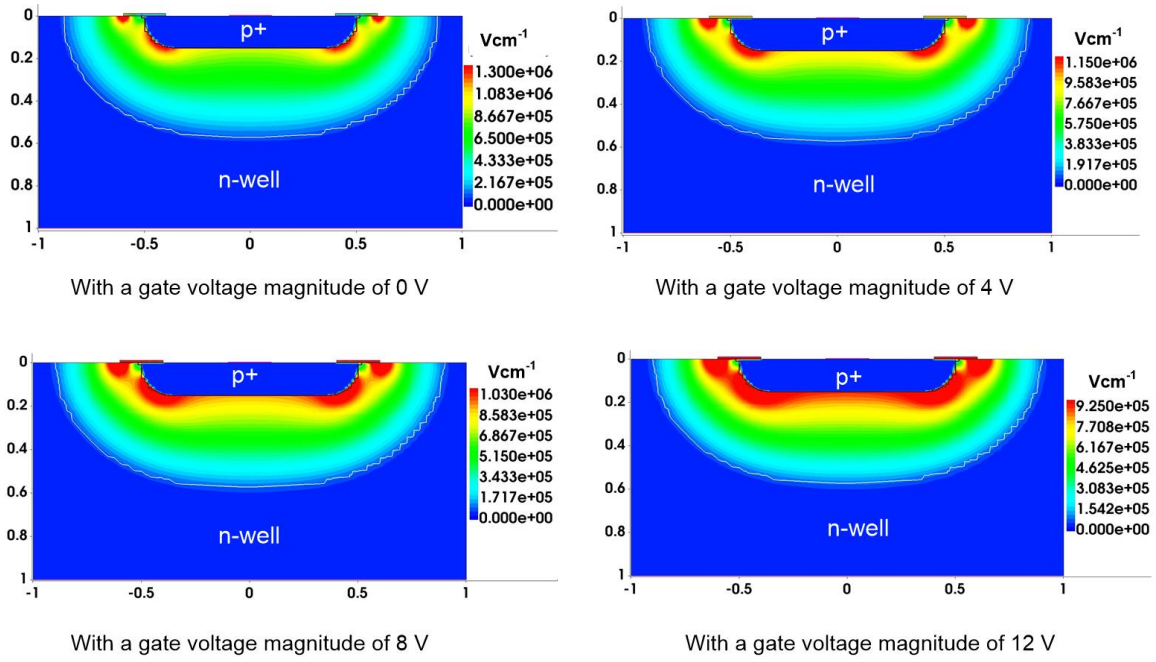



**Figure 3.3:** Simulation result of electrical field modulation using applied gate voltage magnitude of 0 V, 4 V, 8 V, and 12 V (x-axis and y-axis are in $\mu$m) [98].

this work for the first time. The experimental results reported here are the average values of three tested chips with a maximum deviation of approximately 2.81%. Photomicrographs of the fabricated PGSPAD device in sub-micron standard CMOS processes, 0.5 $\mu$m, 0.5 $\mu$m high voltage, 0.35 $\mu$m, and 180 nm CMOS processes, are shown in Figure 3.4.

Two source-measure-units, SMUs, (keithley 2400) were used to perform the I-V characterization of each fabricated PGSPAD sweeping the gate voltage. One SMU is used to sweep the forward and reverse voltage across the standard diode terminals while measuring its current, while the other SMU is used to sweep the gate voltage, $V_G$. Figure 3.5 presents the measured I-V characteristics for the PGSPAD device fabricated in a standard 0.5 $\mu$m HV CMOS process to show the modulation of the

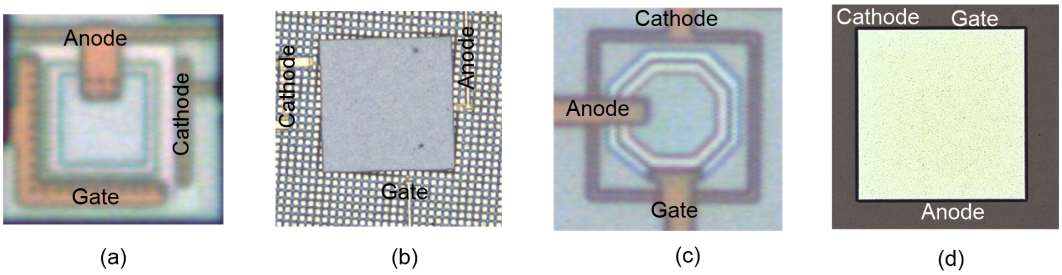



**Figure 3.4:** Photomicrographs of the fabricated PGSPAD device in standard CMOS process, (a) 0.5 $\mu$m CMOS process, (b) 0.5 $\mu$m high voltage CMOS process, (c) 0.35 $\mu$m CMOS process, and (d) 180 nm CMOS process no.1.

breakdown voltage with the applied gate voltage. The gate voltage magnitude is swept from 2 V to 14 V in 2 V step. The breakdown voltage increases with the increase of applied gate voltage.

The measured I-V characteristics for the PGSPAD device fabricated in a standard 0.35 $\mu$m CMOS process is presented in Figure 3.6. The results shows the tuning of the breakdown voltage with the applied gate voltage. The shifting of the breakdown voltage using the applied gate voltage shows a similar trend, the breakdown voltage

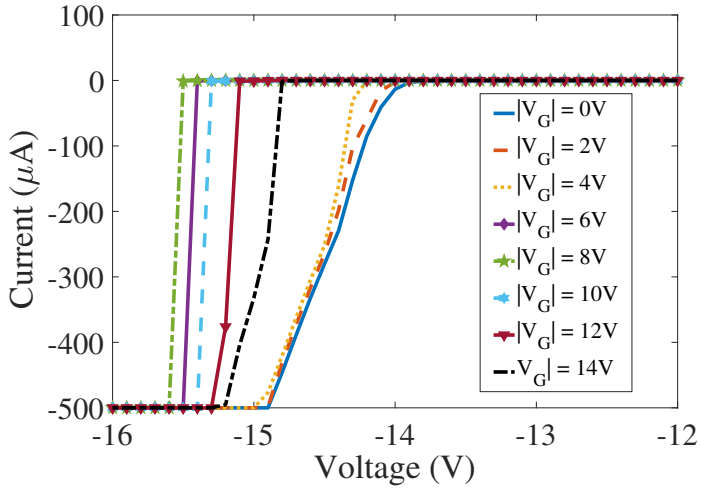



**Figure 3.5:** I-V characteristics showing the changes in the breakdown voltage, $V_{br}$, with the applied gate voltage magnitude, $|V_G|$, for PGSPAD device fabricated in a standard 0.5 $\mu$m HV CMOS process.

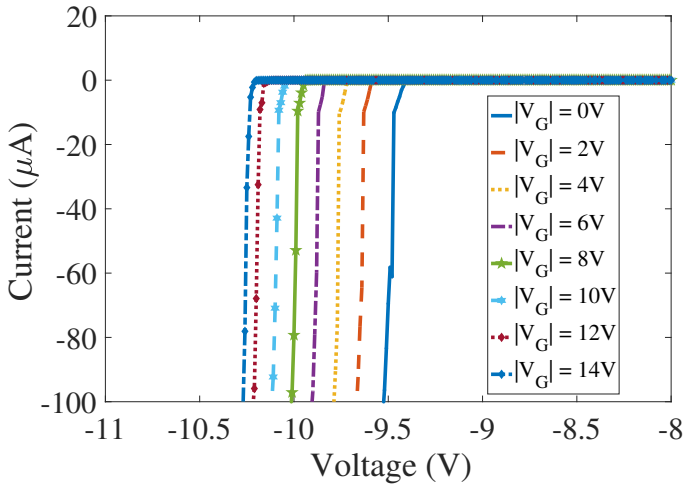



**Figure 3.6:** I-V characteristics showing the changes in the breakdown voltage, $V_{br}$, with the applied gate voltage magnitude, $|V_G|$, for PGSPAD device fabricated in a standard 0.35 $\mu$m CMOS process.

increases with the increase of the applied gate voltage. Since the device performance such as sensitivity, noise, and dynamic range depends on the breakdown voltage, the performance can be tuned using the applied gate voltage.

$V_{br}$ is calculated from the measured data by taking the maximum rate of change of the I-V characteristic. Figure 3.7 summarizes the effect of gate voltage on the breakdown for PGSPADs fabricated in multiple CMOS processes with different

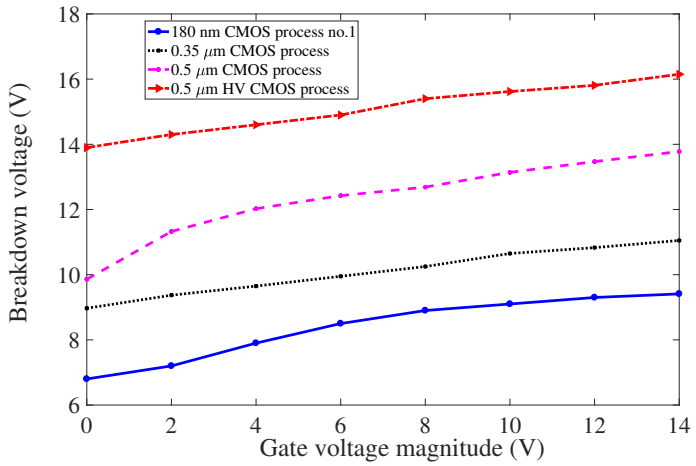



**Figure 3.7:** Variation of experimentally measured breakdown voltage, $V_{br}$ with applied gate voltage magnitude, $|V_G|$, from fabricated PGSPAD device in multiple CMOS processes ( [44] ©2018 IEEE).

vendors. The increase in applied $V_G$ results in increase of the $V_{br}$ for all the aforementioned processes. For a larger standard CMOS process of 0.5 $\mu$m, the experimental variation in the breakdown voltage shows a change of almost 3.9 V.

The perimeter gated technique has been verified in processes (180 nm standard CMOS process) which have shallow trench isolation (STI). Based on the typical submicron design rules, the placement of polysilicon causes the STI to be isolated from the anode. The $V_{br}$ increases with the increase of $V_G$ similar way to that of larger process. The $V_{br}$ varies from 6.8 V to 9.41 V for a $V_G$ of 0 V to 14 V. For a high voltage 0.5 $\mu$m CMOS process, the $V_{br}$ increases approximately 1.8 V due to the increase of the gate voltage. Since this process is a high voltage process, the measured breakdown voltage is higher compared to that of the other mentioned processes. For PGSPAD device fabricated in 0.35 $\mu$m CMOS process, the changes in $V_{br}$ (around 1 V) with the applied gate voltage confirms the tuning of breakdown voltage also.

PGSPAD device has been fabricated in 180 nm CMOS process with another different vendor and characterized also. Figure 3.8 shows the photomicrograph of the fabricated PGSPAD device while the measured I-V characteristics is shown in Figure 3.9 with variation of gate voltage, $|V_G|$. It is observed that the breakdown voltage, $V_{br}$, increases with the increase of $|V_G|$ showing the similar trend as observed in the I-V characteristics of PGSPAD devices implemented in other CMOS processes (Figure 3.7).

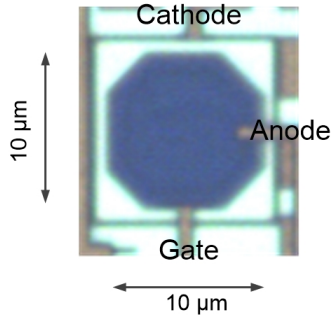



**Figure 3.8:** Photomicrograph of the PGSPAD device fabricated in a standard 180 nm CMOS process no.2.

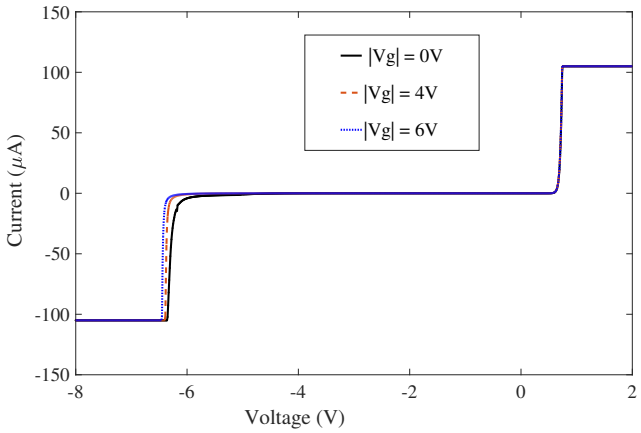



**Figure 3.9:** I-V characteristics for PGSPAD device fabricated in a standard 180 nm CMOS process no.2 for different gate voltages, $|V_G|$.

### 3.2.4 Effect of Gate Voltage on Dark Count Rate

In addition to preventing premature edge breakdown, PGSPAD reduces dark count noise. The reduction of dark count noise is primarily due to the reduction of band-to-band tunneling. The effectiveness of the gate voltage for reduction of dark count noise through the reduction of band-to-band tunneling by the applied gate voltage has been examined experimentally. Figure 3.10 shows the experimental measurements of the dark count rate for varying the $V_G$ of PGSPAD over a range of temperature, from -50°C to 30°C, with the excess bias voltage of 0.5 V. Figure 3.10 shows that the DCR

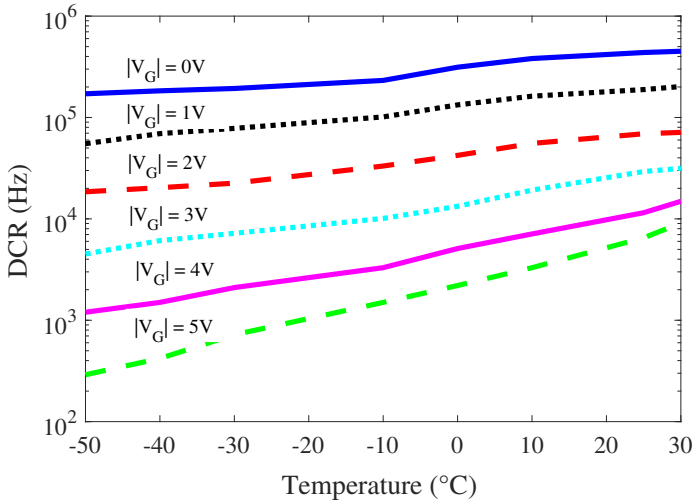



**Figure 3.10:** Effect of gate voltage, $|V_G|$, on dark count rate, DCR, over a range of temperatures for PGSPAD fabricated in 0.5 $\mu$m CMOS process with $V_{Exc} = 0.5V$ (experimental measurement) ( [44] ©2018 IEEE).

can be reduced to few Hz by increasing the gate voltage through the reduction of band to band tunneling at relatively low temperatures. However, when the temperature increases towards the room temperature, the effect of $V_G$ in reduction of noise is minimized due to the increase of noise caused by thermal generation.This is due to the fact that the gate bias of the PGSPAD device modulates the electric field through the modulation of the carrier concentration. With higher applied electric field and narrow depletion region, electrons can quantum mechanically tunnel between the conduction band and the valance band. Therefore, inter-band tunneling depends on the electric field verified through the empirical relation between the carrier generation rate due to $CGR_{Tunn}$, and the electric field, $F$ (equation 2.6). The gate voltage affects band to band tunneling through modulation of electric field. Therefore, the reduction of dark events in the PGSPAD is primarily caused by a reduction in band to band

tunneling. As a result, PGSPAD provides the tunability of noise through tuning the band to band tunneling noise using the applied gate voltage in PGSPAD based detectors.

## 3.3 Architecture of Designed SiPM using PGSPAD

Figure 3.11 shows the circuit diagram of the designed PGSPAD SiPM, an array of 18 × 18 pixel array incorporating a perimeter gated SPAD (PGSPAD) as the basic building block and a quenching resistor. A common anode bias is applied and all gates are connected together at a common gate for gate biasing. Each pixel has an individual quenching resistance and the cathode of the individual PGSPAD is connected to the

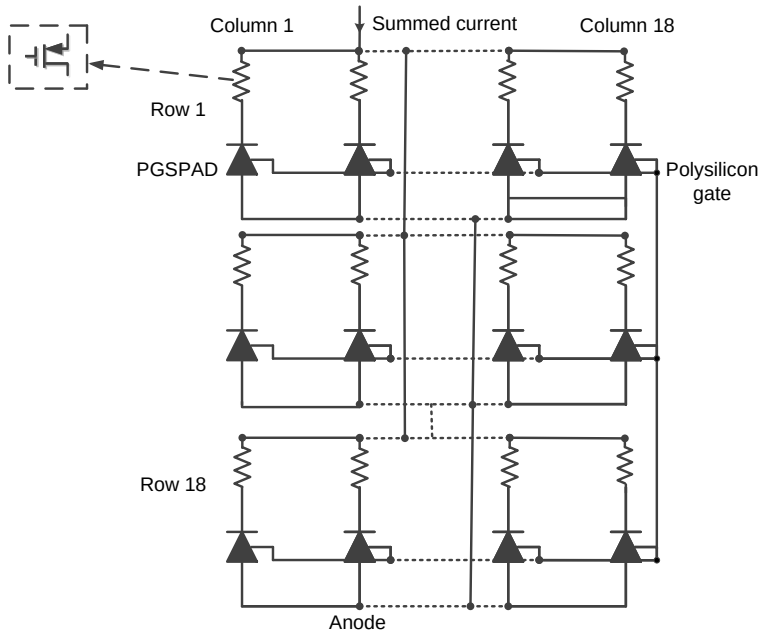



**Figure 3.11:** Schematic of designed SiPM using PGSPAD ( [44] ©2018 IEEE).

quenching resistance. Each PGSPAD can undergo avalanche independently under an incident photon flux.

In order to improve the fill factor and provide a variable quenching resistance, a MOS device is used to implement the quenching resistor in this design. The value of the resistance can be changed by varying the gate bias voltage of the MOS device. Figure 3.12 shows two different configurations, one with PMOS quenching resistor while the other one includes the NMOS as quenching resistor in the SiPM pixel. Since the source to gate voltage for the PMOS quenching resistor can be well controlled to operate in the triode region, the pixel architecture with PMOS based quenching resistor (Figure 3.12 (a)) is used in this work. The PMOS transistor was biased to make the value of the resistor about 100 kΩ. Since all the PGSPADs, including the quenching transistors, are in parallel, the individual avalanche currents are summed at the output (Figure 3.11). Increasing photon intensity increases the number of triggered PGSPADs, resulting in an increase in output current.

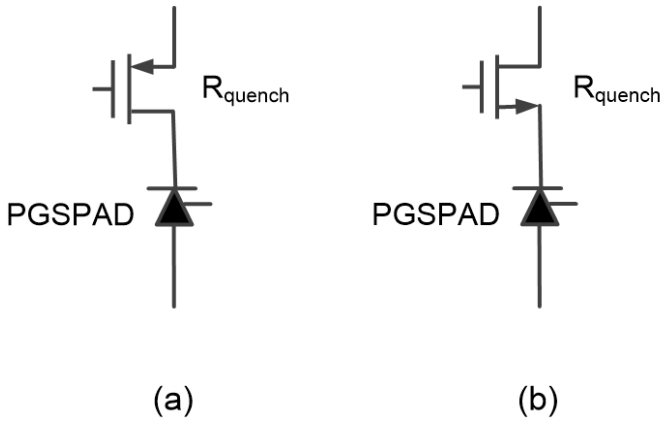



**Figure 3.12:** Pixel of SiPM using (a) PMOS based quenching resistor, (b) NMOS based quenching resistor.

The photomicrograph of the designed PGSPAD SiPM is shown in Figure 3.13. The implemented PGSPAD is an nwell-p+ junction type and is square shaped. A polysilicon layer of width 3.7 $\mu$m surrounds the junction. A PMOS is used to implement the quenching resistor. The additional advantage of implementing quenching resistor with PMOS provides the well controlled source to gate resistor in addition to the advantages of variable resistance and compact design. The designed SiPM was implemented in a standard 0.5 $\mu$m 2−poly, 3−metal CMOS process. The size of PGSPAD device is 20 $\mu$m $\times$ 20 $\mu$m. The pixel fill factor is 11.11%, with pixel dimension of 33 $\mu$m $\times$ 33 $\mu$m, including an active area of 11 $\mu$m $\times$ 11 $\mu$m.

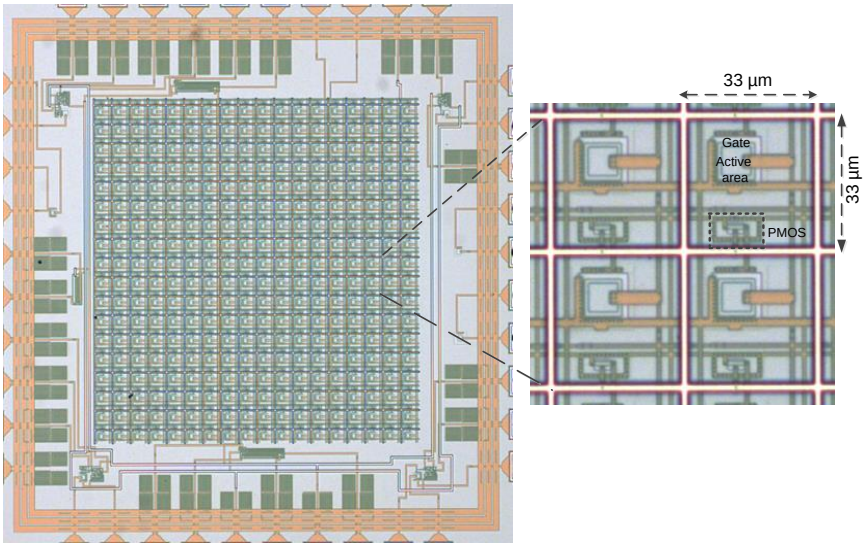



**Figure 3.13:** Photomicrograph of designed SiPM using PGSPAD SiPM fabricated in 0.5 $\mu$m CMOS process ( [44] ©2018 IEEE) .

## 3.4 Experimental Results of Designed SiPM using PGSPAD

This section presents a complete electrical, optical, and temperature characterization of the designed PGSPAD SiPM. The noise, signal to noise ratio (SNR), and sensitivity of the SiPM can be tuned using the additional gate terminal. Dark current, the output current of SiPM in absence of photon, is the effective noise of SiPM. The average values of three tested chips are reported here for each dataset, with a maximum deviation of $\sim 9\%$ for any measured data from the average value.

### 3.4.1 Electrical Characterization of PGSPAD SiPM

Figure 3.14 shows the change in dark current as a function of the gate voltage $V_G$. $V_G$ is varied from 2 V to 14 V and $V_{Exc}$ is varied from 0 V to 1.6 V using a source-measure-unit (SMU) for the anode-cathode and another for the gate. As with other standard SiPMs, the dark current increases with increasing $V_{Exc}$. This is due to an increased drift velocity of trapped and thermally generated carriers. The measured dark current reduces with increasing gate voltage. This is because increasing the gate voltage results in a more uniform electric field all over the junction, increasing the breakdown voltage. The avalanche probability due to thermally generated, band to band tunneling, or trapped carriers decreases with the breakdown voltage for a fixed excess bias voltage reducing the dark current. Figure 3.15 shows the variation of

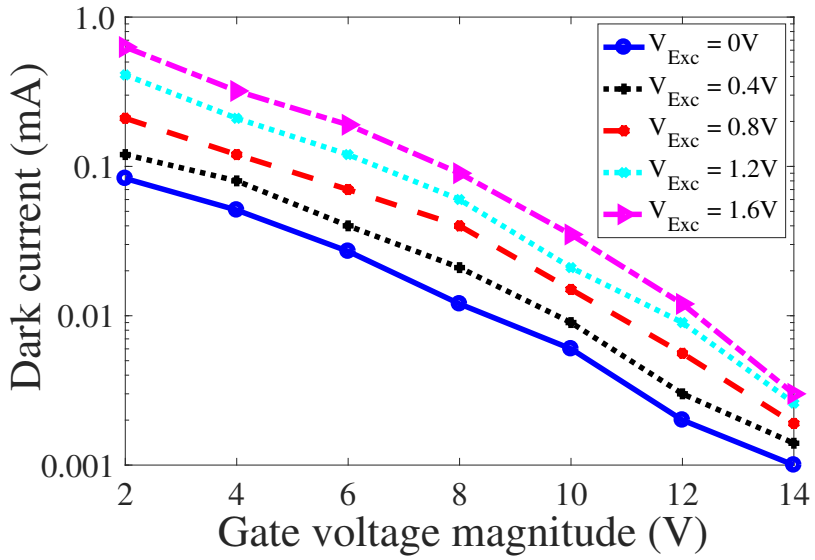



**Figure 3.14:** Variation of dark current with applied gate voltage ,$|V_G|$, for different excess bias voltage, $V_{Exc}$ for the designed SiPM fabricated in 0.5 $\mu$m CMOS process ( [44] ©2018 IEEE).

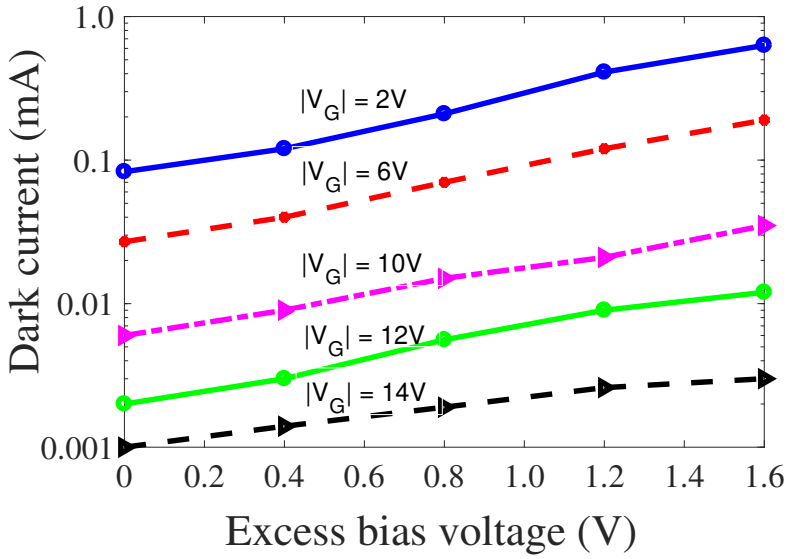



**Figure 3.15:** Variation of dark current with excess bias voltage, $V_{Exc}$, for different gate voltage, $|V_G|$ for the designed SiPM fabricated in 0.5 $\mu$m CMOS process ( [44] ©2018 IEEE).

dark current with excess bias voltage, $V_{Exc}$, for different applied gate voltages. The increase in excess bias voltage increases the probability of initiating an avalanche for a fixed gate voltage causing the dark current to rise.

### 3.4.2 Optical Characterization of PGSPAD SiPM

The optical set-up to measure the spectral response is schematically presented in Figure 3.16. For optical characterization, an optical power meter (1936-R), a monochromatic light source, (TLS-300X), along with an integrating sphere (819D-SL-3.3), and two keithley 2400 source-measure-units (SMUs) were used. The tunable monochromatic light source, TLS-300X, allows the variation of wavelength and optical power during the experiment. An optical coupler is used to connect the light source and the integrating sphere. The optical power meter was coupled to one port of integrating sphere to measure the incident power of the light source. Finally, the

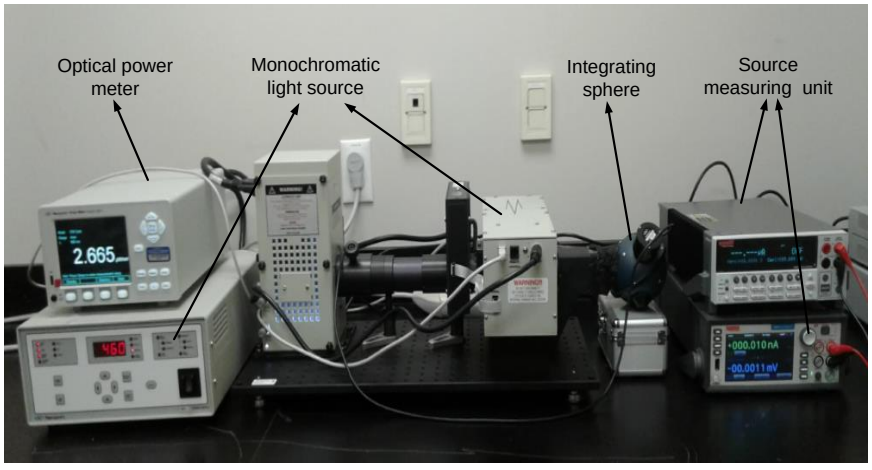



**Figure 3.16:** Optical testbench for experiment ( [44] ©2018 IEEE).

fabricated SiPM chip was coupled to the other port of the integrating sphere to measure the spectral response.

Signal to noise ratio, SNR, and photon detection efficiency, PDE, are functions of the measured photocurrent and their spectral responses are similar. PDE is the probability of producing an output by the SPAD due to the incident photon and is given by [99, 100]

$$PDE = \frac{I_m hc}{P_{op} G \lambda e} \tag{3.4}$$

where $I_m$ is the measured photocurrent, $h$ is Planck's constant, $c$ is the speed of light, $P_{op}$ is the incident optical power over the active area at a specific wavelength ($\lambda$), $G$ is the gain of the pixel of SiPM, and $e$ is the charge of an electron.

The gain of the pixel of SiPM is

$$G = \frac{CV_{Exc}}{e} \tag{3.5}$$

where $C$ is the total capacitance of the pixel and $V_{Exc}$ is the excess bias voltage.

The SNR of SiPM is [99, 100]

$$SNR = \frac{I_m - I_d}{I_d} \tag{3.6}$$

where $I_m$ is the measured photocurrent and $I_d$ is the dark current.

The spectral response of the PGSPAD SiPM as a function of gate and excess bias is shown in Figure 3.17 and 3.18. In order to measure the spectral response, the output photocurrent was measured for different wavelengths and different excess bias voltages while keeping the gate voltage fixed at 14 V (Figure 3.17). During these measurements, the optical power was kept fixed at 100 nW$cm^{-2}$ ($2.5 \times 10^{10}$ photons/s). We chose this number to make it comparable with the characterization measurements of commercially available SiPMs manufactured by Hamamatsu where the optical detectors are characterized within the range of $10^8$ - $10^{11}$ photons/s for a wavelength of 500 nm [99]. These Hamamatsu SiPMs have been extensively used for neutron detection [30, 101].

This suggests that our PGSPAD SiPM is suitable for neutron detection and offers a significant advantage over commercially available devices due to the possibility of incorporating the readout electronics. As $V_{Exc}$ increases, dark current and sensitivity increase, but at different rates. This is because with the increase in excess bias voltage the drift velocity of the noise generated carriers also increases. As the gate voltage the breakdown voltage also increases and the excess bias voltage (the difference between applied bias voltage and the breakdown voltage) decreases. On the other hand, with the increase of gate voltage the probability to imitate the avalanche of the noise generated carrier decreases. This results in an overall decrease in SNR. However, for a fixed $V_{Exc}$, the gate voltage has a significant effect on the SNR where the SNR increases by a factor of $10^3$ as a function of the gate voltage (Figure 3.18).

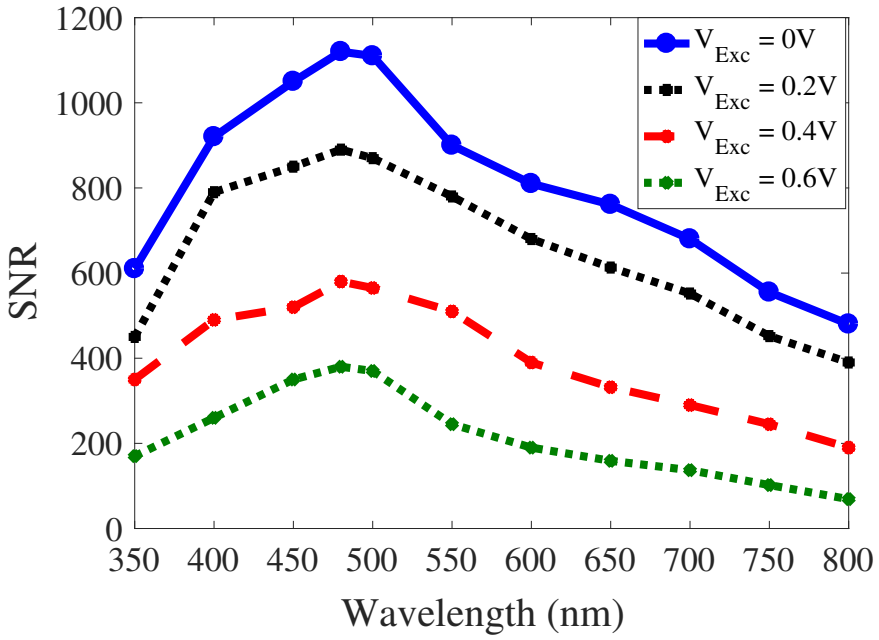



**Figure 3.17:** Variation of SNR with wavelength for different excess bias voltage for the designed SiPM fabricated in 0.5 $\mu$m CMOS process ($|V_G| = 14V$, optical power of 100 nW$cm^{-2}$) [44].

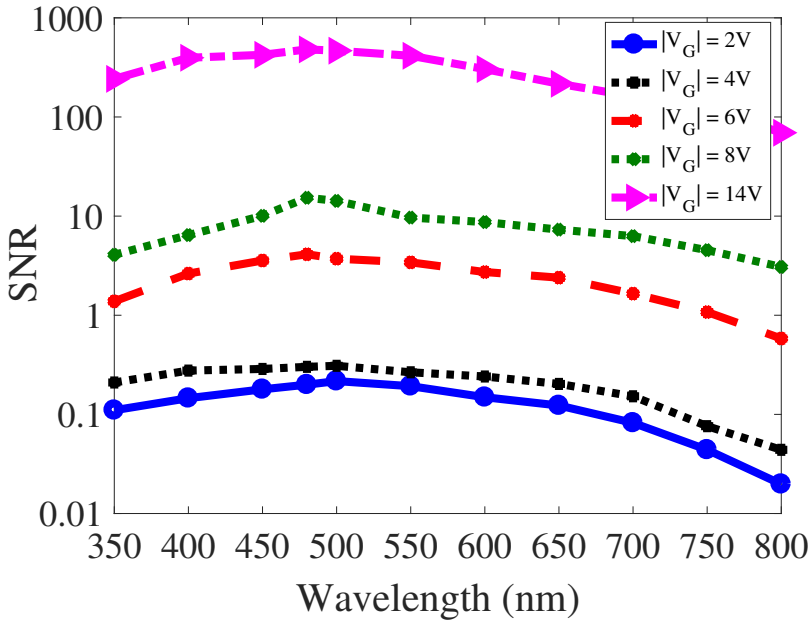



**Figure 3.18:** Variation of SNR with wavelength for different gate voltage, $|V_G|$ for the designed SiPM fabricated in 0.5 $\mu$m CMOS process ($V_{Exc} = 0.4V$, optical power of 100 nW$cm^{-2}$) ( [44] ©2018 IEEE).

Figure 3.19 shows the variation of the output measured current with optical power. For this measurement, the applied gate voltage magnitude was fixed at 14 V and a excess bias voltage of 0.4 V was used. In order to provide uniform incident light, a monochromatic light source and an integrating sphere were used. The optical power of the incident light was varied from 0.042 $\mu \mathrm{W} cm^{-2}$ to 2.486 $\mu \mathrm{W} cm^{-2}$ using an attenuator and optical filters. The wavelength was kept fixed at 500 nm during the measurements. Since the increase in optical power increases incident photon flux, more pixels are triggered resulting in increase of the total output current (Figure 3.19). The sensitivity of the designed SiPM is $1.06 \times 10^3$ A per $\mathrm{W}/cm^2$.

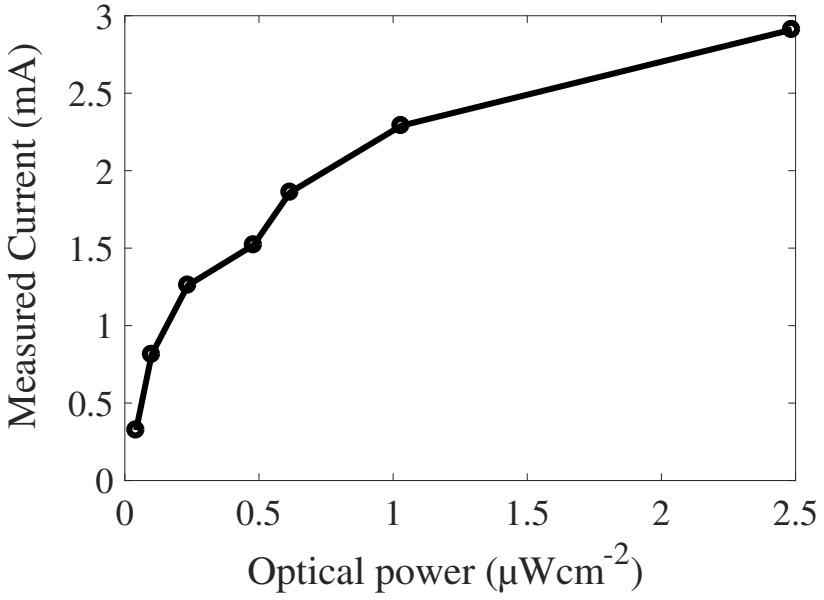



**Figure 3.19:** Variation of output current with incident optical power for the designed SiPM fabricated in 0.5 $\mu$m CMOS process ($\lambda = 500nm$, $|V_G| = 14V$, $V_{Exc} = 0.4V$) ( [44] ©2018 IEEE).

### 3.4.3 Temperature Characterization of PGSPAD SiPM

Temperature effects on the noise performance of the designed PGSPAD SiPM was characterized at three different temperatures, -60°C, 25°C, and 60°C. For the high temperature characterization, a temperature chamber (DELTA 9023) was used. For low temperature measurement, the chips were placed in a commercial precision low temperature freezer. For all the measurements, the gate voltage was kept at 5V. For each temperature, two sets of data were taken with two different excess bias voltage, $V_{Exc}$, of 0.8 V and 1.6 V. Figure 3.20 shows that the dark current increases with temperature. However, the change in dark current is more prominent at higher temperatures compared to lower temperatures. If $V_{Exc}$ increases, dark current increases. The temperature dependence of dark current can be explained by the temperature dependency of Shockley-Read-Hall generation (SRH), including trap assisted tunneling, and band-to-band tunneling.

The SRH generation dominates the band-to-band tunneling above room temperature and the dependency of dark count noise on temperature is exponential [102–104]. Therefore, the dark current increases exponentially in this temperature range. In contrast, at low temperature band-to-band tunneling is the dominating mechanism and since the dependency of band-to-band tunneling on temperature is very weak, the dark current increases slightly at low temperature [102–104]. Based on the effect of applied gate voltage on measured DCR (Figure 3.10), the PGSPAD SiPM is expected to have a more significant change in the dark current at lower temperatures.

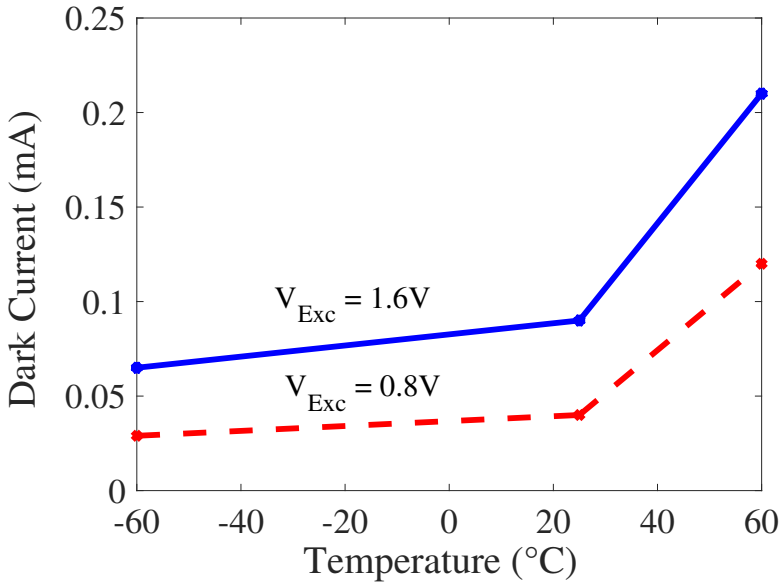



**Figure 3.20:** Variation of dark current with temperature for PGSPAD SiPM for fabricated in 0.5 $\mu$m CMOS process ($|V_G| = 5V$) [44].

## 3.5 Performance Comparison of Designed PGSPAD SiPM with Existing SiPMs

A performance comparison between the designed CMOS analog PGSPAD SiPM and other commercial SiPMs [29, 30, 105] found in the literature is summarized in Table 3.1 while comparison with standard CMOS analog SiPMs [106–108] reported in the literature are summarized in Table 3.2.

Although the developed analog PGSPAD SiPM provides a relatively lower fill factor than the other SiPMs, the designed detector is the only one which provides tunable SNR and sensitivity while maintaining the benefits of standard CMOS process. The relatively low fill factor is due to the chosen pixel size. Increase of

**Table 3.1:** Performance Summary and Comparison of designed CMOS analog SiPM with a selection of commercial analog SiPMs

| **Parameter** | **This Work** | **Sensl [105]** | **Hamamatsu [30]** | **Stolin [29]** |
|---|---|---|---|---|
| Process | 0.5 $\mu$m CMOS | Specialized | Specialized | Specialized |
| Tech. | Analog | Analog | Analog | Analog |
| Area ($mm^2$) | 0.86× 0.85 | 3×3 | 1×1 | 6×6 |
| Pixel Size ($\mu m^2$) | 33×33 | 35×35 | 25×25- 100×100 | 35×35 |
| Fill Factor (%) | 11.11 | 65-78 | 30-78 | 64 |
| Dark Current ($\mu$A) | 5.1 | 0.34 | Not Reported | 7.81 |
| $SNR_{peak}$ (%)@ wavelength | 1150 [500$nm$] | Not Reported | Not Reported | Not Reported |
| $PDE_{peak}$(%)@ wavelength | 29 [500$nm$] | 48.6 [420$nm$] | 56 [450$nm$] | 45 [410$nm$] |
| Turnable SNR | Yes | No | No | No |
| Turnable Sensitivity | Yes | No | No | No |

**Table 3.2:** Performance Comparison of designed CMOS analog SiPM with a selection of CMOS analog SiPMs

| **CMOS Node (nm)** | **Pixel Size ($\mu m^2$)** | **Typical Operation (V)** | **PDE (%)@ wavelength** | **Tunable SNR and Sensitivity** |
|---|---|---|---|---|
| 800 [106] | 2500 | BV + 1.5 | 15 @ 410 nm | No |
| 800 [107] | 913 | BV(26) + 3 | Not reported | No |
| 180 [108] | 2500 | BV(12) + 2 | 1.3 @ 410 nm | No |
| 500 (This work) | 1089 | BV(16.7) + 1.5 | 29 @ 500 nm | Yes |

the overall pixel size, results in an increase in active area and relatively smaller or no increase in the non-active area of the pixel. In addition, the PGSPAD SiPM provides a lower dark current noise and a comparable photon detection efficiency (PDE). The commercial SiPMs manufactured by the SensL, Hamamatsu [30, 105] and characterized in [29] offers the best PDE due to the use of specialized process to improve the performance while the designed SiPM implemented in standard CMOS process. The goal of this work was to achieve the best possible performance while implementing the SiPM in standard CMOS process.

## 3.6 PGSPAD SiPM fabricated in 180 nm CMOS process

An analog SiPM using PGSPAD, an array of 9×9 pixel array incorporating a perimeter gated SPAD (PGSPAD), has been designed and fabricated in 180 nm commercial CMOS process also. Figure 3.21 shows the photomicrograph of the PGSPAD SiPM chip fabricated in 180 nm standard CMOS process.

I-V characteristics of the developed PGSPAD SiPM has been measured. Two source measure units (SMUs) are used, one for common anode biasing and one for gate biasing. During the measurement, the gate voltage ($|V_G|$) was kept fixed at 0 V and the current compliance of anode biasing was 500 $\mu$A. Figure 3.22 shows the measured I-V characteristics for the pGSPAD SiPM fabricated in 180 nm CMOS process.

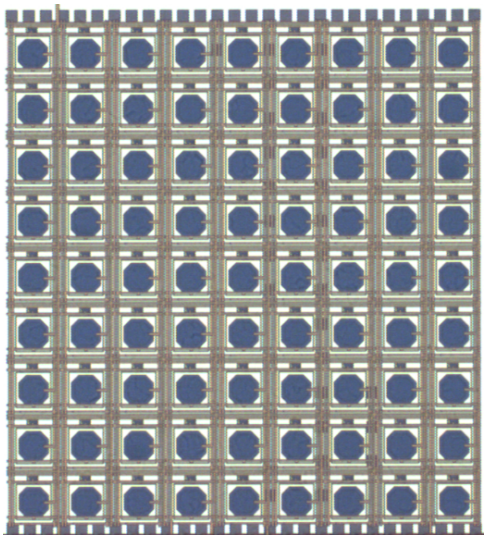


**Figure 3.21:** Photomicrograph of designed SiPM using PGSPAD SiPM fabricated in 180 nm CMOS process.

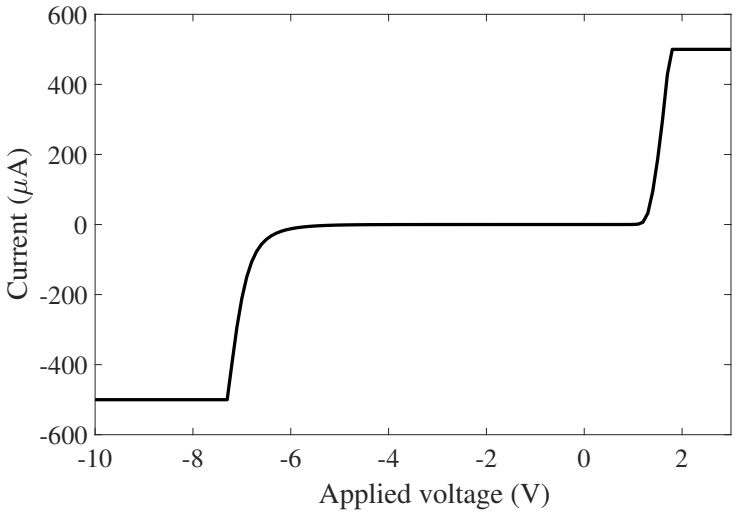



**Figure 3.22:** Measured I-V characteristics of the designed SiPM using PGSPAD, an 9×9 PGSPAD based pixel array, fabricated in 180 nm CMOS process ($|V_G| = 0V$).

Dark current for the designed SiPM has been measured for varying excess bias voltages with $|V_G|$ of 0 V. Figure 3.23 shows the variation of dark current with excess bias voltage, $V_{Exc}$, for the designed SiPM fabricated in 180 nm CMOS process for gate voltage, $|V_G|$, of 0V. It is observed that the dark current increases with the increase of $V_{Exc}$ as expected.

## 3.7 Conclusion

Over the years, SiPMs have shown a great promise as photosensors for a broad range of high resolution nuclear imaging applications in medical and other fields. In this chapter, a full chip analog PGSPAD based CMOS SiPM suitable for nuclear imaging applications has been presented and first fully characterized. The designed SiPM contains 324 PGSPADs, arranged in 18 $\times$ 18 pixels with pixel dimensions of 33 $\mu$m $\times$ 33 $\mu$m resulting in a 11.11% fill-factor. The PGSPAD based SiPM has been

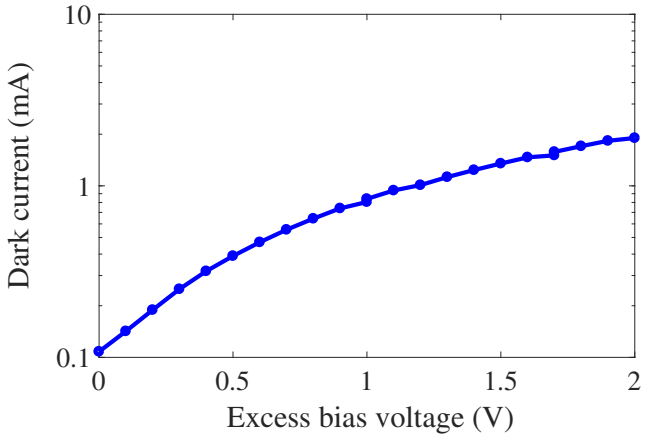



**Figure 3.23:** Variation of dark current with excess bias voltage, $V_{Exc}$, for the designed SiPM fabricated in 180 nm CMOS process for gate voltage, $|V_G|$, of 0V.

fully characterized for dark current, signal to noise ratio, sensitivity, and thermal characterization. The measured spectral response of the SiPM using PGSPAD showed that the signal to noise ratio can be tuned over a range of 1 to 1150 through the applied gate voltage reducing dark current. These characteristics makes the PGSPAD CMOS SiPM suitable for nuclear imaging applications. An analog PGSPAD SiPM, an array of 9×9 pixel array incorporating perimeter gated SPADs (PGSPADs), fabricated in 180 nm commercial CMOS process is presented and characterization results are reported also.

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# Chapter 4

# CMOS Digital Silicon Photomultiplier using PGSPAD with Asynchronous AER readout

** **Portions of this chapter were published in:**

1. Mst Shamim Ara Shawkat, and Nicole McFarlane, *"A CMOS Perimeter Gated SPAD Based Digital Silicon Photomultiplier with Asynchronous AER Readout for PET Applications,"* IEEE Biomedical Circuits and Systems Conference, Cleveland, Ohio, USA, Oct. 2018.

2. Mst Shamim Ara Shawkat, and Nicole McFarlane, *"A CMOS Perimeter Gated SPAD Based mini-Digital Silicon Photomultiplier,"* IEEE International Midwest Symposium on Circuits and Systems, Windsor, Canada, Aug. 2018.

## 4.1 Introduction

Positron emission tomography (PET) and single photon emission computed tomography (SPECT) are nuclear medical imaging techniques which find use in a broad range of applications including brain function analysis, clinical oncology, and clinical research [9–13, 20, 26–29, 33, 92, 109–111]. Silicon photomultipliers (SiPMs), a large array of Geiger mode single photon avalanche diodes (SPADs), are often preferred as a substitute to photomultiplier tubes (PMTs) which are magneto sensitive, expensive, bulky, and require

high voltages [9–13, 20, 92]. Since a SPAD's output is intrinsically digital due to the capability to differentiate between no photon and a photon, conversion to a digital output at each individual SPAD enhances the noise performance, making digital SiPMs a good option for PET and SPECT applications [9, 13, 20, 26, 27, 29].

CMOS based digital SiPMs take the benefits of commercial CMOS process to achieve analog to digital conversion for each SPAD and to combine the required electronics on the same chip [9, 20, 40, 92]. However, standard CMOS SPADs suffer from early breakdown resulting in a reduction of detection efficiency [40, 42, 44]. It has been previously shown that perimeter gated SPADs (PGSPADs) prevent premature edge breakdown, modulate breakdown voltage, and tune device's noise, sensitivity, and dynamic range [41, 42, 44].

In order to process the asynchronous scintillation events in PET and SPECT applications, photosensors require high bandwidth and high fill-factor (FF) [9, 10, 20, 26, 27, 29, 40, 92]. Existing digital SiPMs use synchronous readout schemes, sequential, in-column or fully parallel synchronous schemes, to process the detected photons [9, 10, 20, 112]. Although the sequential readout architecture in [10,11] provides the simple and excellent FF because of the sharing of all pixels with one single readout electronics block (time-to-digital converter or digital counter), it provides low bandwidth and poor photon detection efficiency. Alternatively, the in-column architecture reported in [9, 20] enhances the bandwidth and photon detection efficiency due to the partial parallelism at the cost of decreased FF. The fully parallel in pixel scheme presented in [112] provides the best detection bandwidth but worst FF as it requires substantial areas to implement per pixel functionalities.

Compared to the synchronous readout, asynchronous readout best serves the asynchronously arriving photons with high bandwidth and an improved signal to noise ratio.

Address event representation (AER) is an asynchronous digital multiplexing technique which allows high bandwidth communication. AER is data driven and removes the sampling of all the pixels regardless of their output which is inherent to the conventional sequential scanning, lessens temporal aliasing by sending the events as they happen. In an AER protocol, the output is an address which represents the address of the triggered pixel indicating that an event has occurred. Hence, this protocol is named as address event representation. Due to the inherent asynchronous and event-based nature of SPAD, they are therefore an innate partner of AER.

A new architecture for a CMOS PGSPAD digital SiPM with fully digital asynchronous AER readout for PET and SPECT applications is presented. To the best of my knowledge, this is the first AER based digital SiPM architecture for PET and SPECT applications. The PGSPAD pixel, PGSPAD mini digital SiPM, incorporates data compression schemes, and a compact analog counter to reduce the total electronics required for SPAD readout. An event generator is incorporated in the pixel to realize the fully digital asynchronous AER readout at the top level of the detector. The compact pixel is incorporated into a digital SiPM array with a fully digital AER readout to perform the asynchronous exposure more efficiently. The designed CMOS digital SiPM with AER readout circuit has been characterized. As pointed out in [113, 114], this is the first reported PGSPAD digital SiPM with asynchronous AER readout to provide high bandwidth.

## 4.2 Literature review on Asynchronous AER read-out

Address-event representation (AER) is an asynchronous digital multiplexing technique that was originally developed as an inter-chip communication protocol in VLSI analogs of neuronal visual processing [115]. AER has a lot of similarities with the action-potential representation used by real neurons. In this system, the interval between the events is analog whereas the amplitude of the event is standard digital amplitude. Therefore, the pattern of the events are similar to the action potential of neurons. The time interval between the events is used to encode the information.

The basic address-event representation is explained in Figure 4.1. In order to encode the output, a temporal sequence of digital amplitude events is produced by the neurons in the sender similar to a train of action potentials. Whenever a neuron notifies an event, the multiplexing circuitry announces that neuron's address on the inter-chip data bus. The announcement is based on the assumption that the interval between the events is much longer than the time needed to transmit the address. As a result, many addresses can be multiplexed on the same bus. The transmission of the address is annotated as an event by the receiver. Therefore, the communication code is named as an address-event representation, AER [115].

In order to provide high-bandwidth communication between large arrays of neuron elements, AER is implemented with the assumption that the data bus should be assigned to transmit the significant signal. Time-multiplexing is the only way to transfer data from

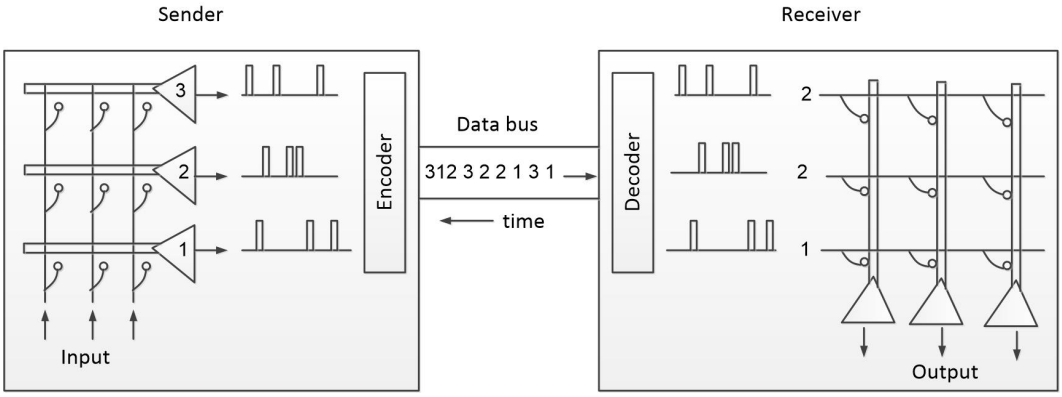



**Figure 4.1:** The basic address-event representation.Trains of action potentials are generated by self-timed neurons at the sender. Once neurons generate action potentials, they request control of the bus and are chosen to send their addresses by the multiplexing circuitry. A temporal stream of addresses transfers between the sender and the receiver.The receiver decodes the temporal stream into trains of action potentials that reach their proper postsynaptic targets. The detailed timing of the events is maintained [115].

several thousand output nodes within the pin limitations of existing packaging technology. Each node is sampled once every frame in conventional scanning. If there is any spatial or temporal change in the area of image, the retina produces output for only that particular area. Although most of the nodes will have almost no output, they are sampled anyway. On the contrary, the AER protocol is data driven. Only pixels that have something to inform are sending their output through the data bus. Therefore, areas of uniform illumination do not add to the communication load. Furthermore, AER reduces temporal aliasing by sending events as they occur.

Figure 4.2 represents the basic data transfer process of AER equivalent to the generation of the action-potential of a neuron. A three-inverter oscillator is used to represent the function. The oscillation is equivalent to the generation of an action potential. Therefore, the oscillation is similar to the data transfer process. The data event initiates the oscillation cycle i.e., the data transfer through the pull up transistor, $M_P$. Therefore the capacitor at the initiate node charges to $V_{DD}$ with the assumption that $M_P$ provides sufficient current to

pull the Initiate node well above the inverter threshold before the signal can pass through the oscillator. Once the Initiate node becomes high, the signal propagates through the oscillator causing the Req node to go low. As a result, the Ack node goes high and activates

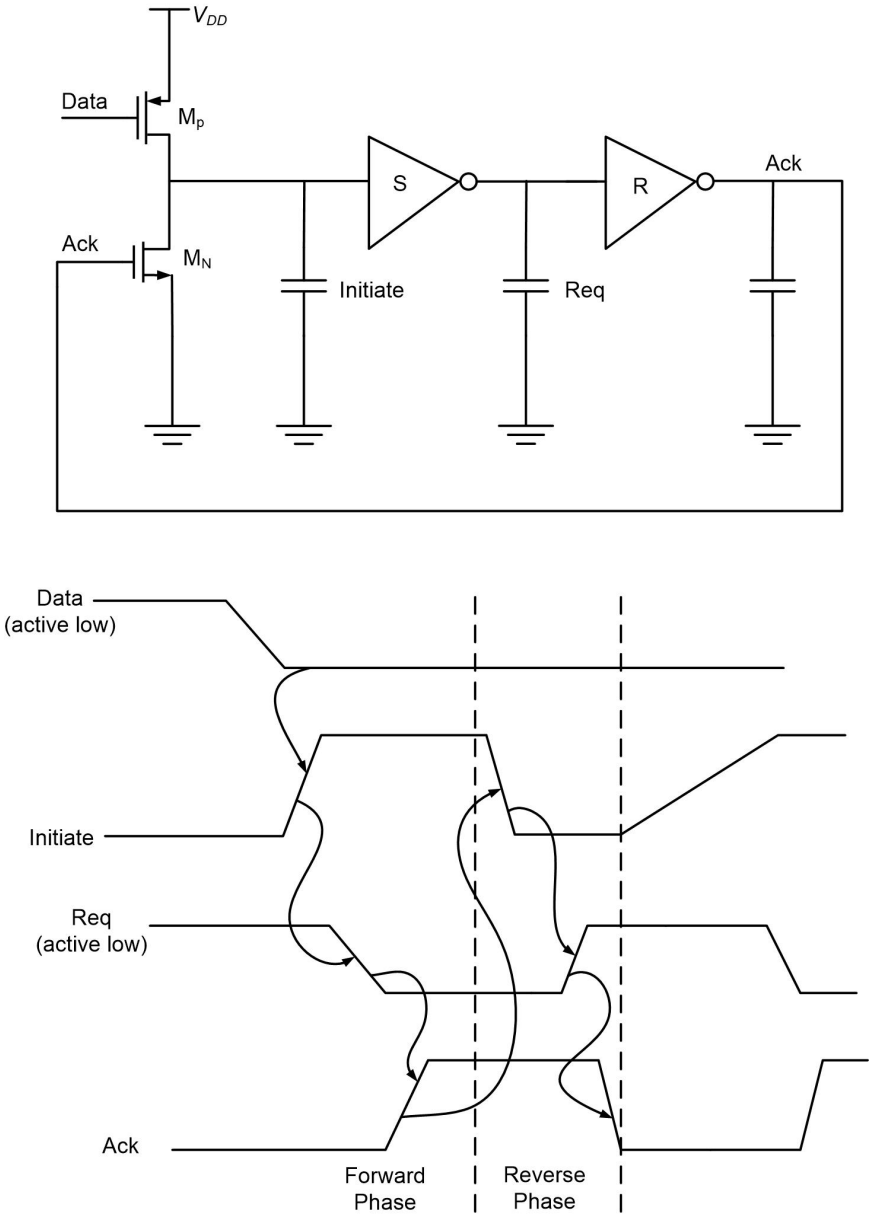



**Figure 4.2:** Three-inverter oscillator and timing diagram representing the sequence of events in a single cycle of the oscillator equivalent to the data transfer process of AER. Inverter S is part of the sender while the inverter R is part of the receiver [115]

the pull down transistor, $M_N$. $M_N$ is made stronger than $M_P$ to ensure that the Initiate node is pulled down, independent of the data event status [115].

Several imaging sensors using AER to communicate the pixel intensity, either by inter-event interval or mean frequency were later reported in the literature [116]. The pixel size is relatively small due to the absence of additional pixel storage circuit. The reset mechanism is not included. The intensity is encoded into the event interval. One of the big limitations is that the bus bandwidth is assigned according to the local scene brightness. Therefore, a dark pixel can take more time to emit an event and the bus can be saturated due to a single feature in the scene [116].

In order to improve the dynamic range, other vision sensors with AER readout where pixel reacts asynchronously to the corresponding change in intensity were reported in the literature [117–120]. The main aim of this work [119] was to implement a high-quality frame-free transient vision sensors with solution to the vision problem in the event-based, data-driven, redundancy-lessening style of computation. The brightness changes in the scene is encoded into the sensor output as an asynchronous stream of pixel address-events. Therefore, data redundancy is reduced while retaining the precise timing information regarding image and object motion that is helpful for dynamic vision problems. Figure 4.3 shows the block diagram of the pixel array inserted in the AER readout circuitry at the periphery. The 15-bit digital address of the pixel including 7-bit x and y addresses and an ON/OFF polarity bit is the final output of the chip. The addresses are transmitted in parallel. The function of the arbiter is to assign the common bus to the pixel events queuing and waiting. Moreover, the arbiter ensures that a row or column that is served by

the arbiter is maintained not to be served again before serving all other rows and columns that have registered requests [118, 119].

In conventional image/video sensors, although the information in some pixel has not changed since the last frame collected, each frame carries the information from all pixels. This causes a high degree of redundancy in the image data resulting in valuable resource utilization with complex and resource-greedy video compression techniques to handle these redundant data. Figure 4.4 illustrating the block diagram of the pixel array inserted in the AER readout circuitry at the periphery. Figure 4.4 shows the block diagram of the

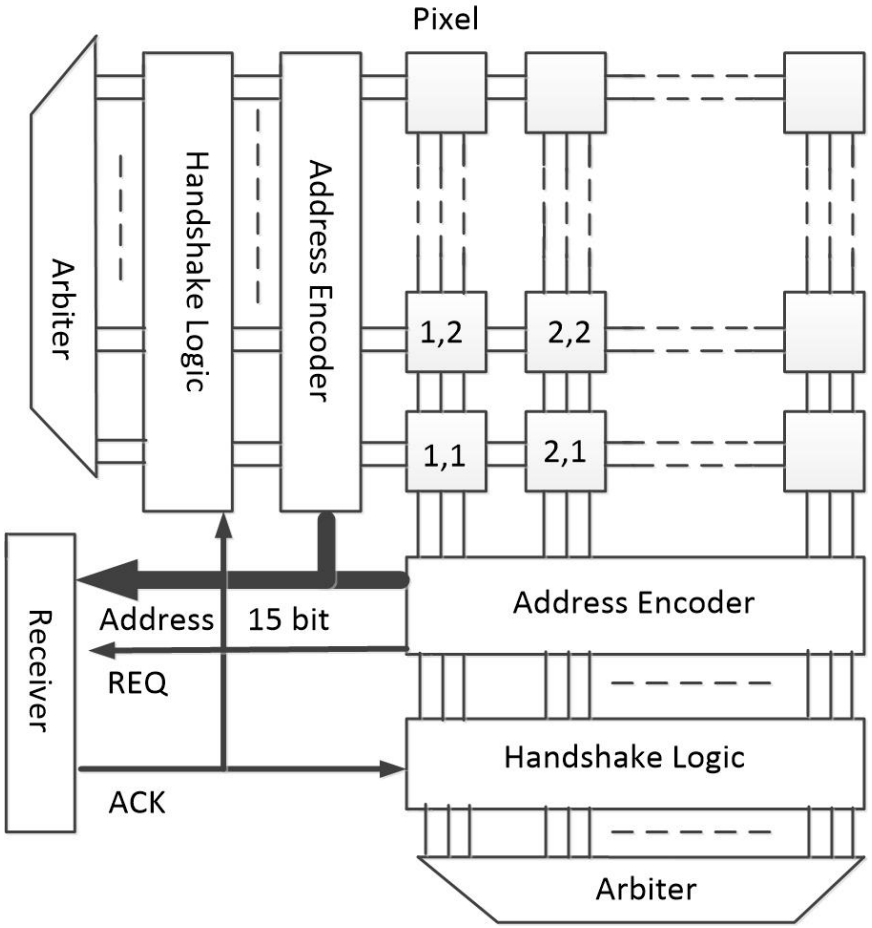



**Figure 4.3:** Block diagram of the pixel array inserted in the AER readout circuitry at the periphery [119].

pixel array inserted in the AER readout circuitry at the periphery. An array of fully autonomous pixels with AER readout that reduces the temporal redundancy is included in this work to reduce the acquisition and computing power, memory/bandwidth. The pixel does not depend on external timing signals and demands the access to an output channel independently and asynchronously only when it has a new illumination value to transmit. Furthermore, the Asynchronous Time-based Image Sensor reported in this work prevents the time quantization of frame based acquisition due to the asynchronous operation [118].

An asynchronous imaging sensor using SPAD with AER readout was reported in [121]. The image sensor consists of a 20 × 20 array of SPADs with fully asynchronous AER readout

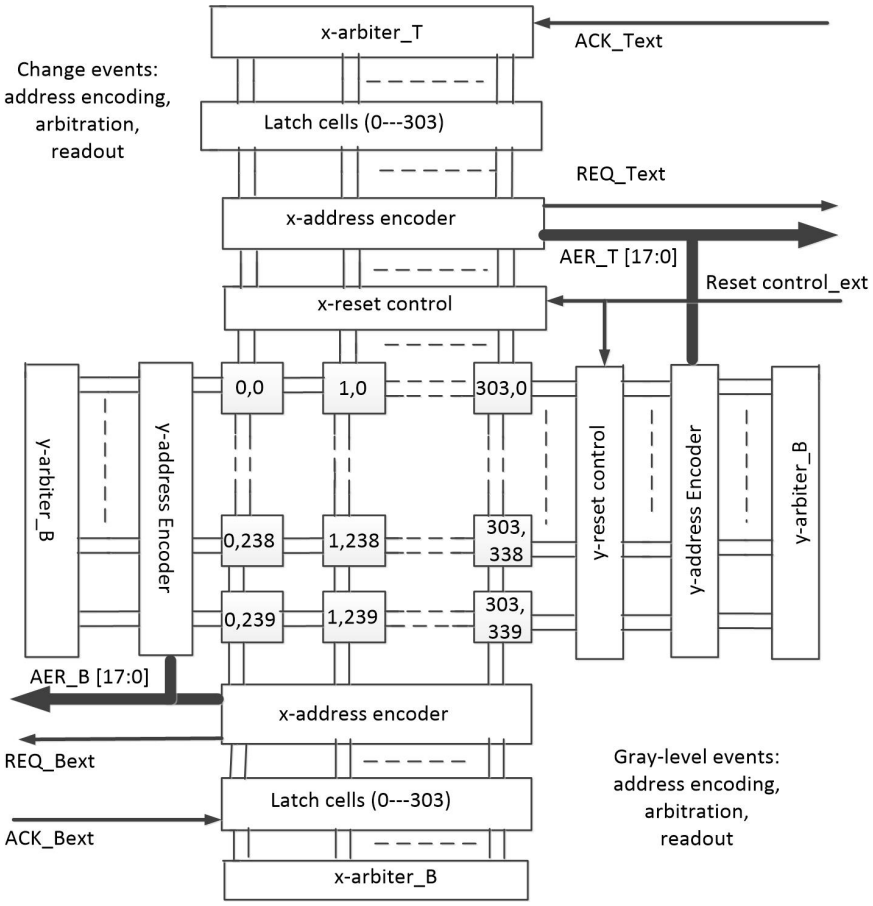



**Figure 4.4:** Block diagram of the pixel array inserted in the AER readout circuitry at the periphery [118].

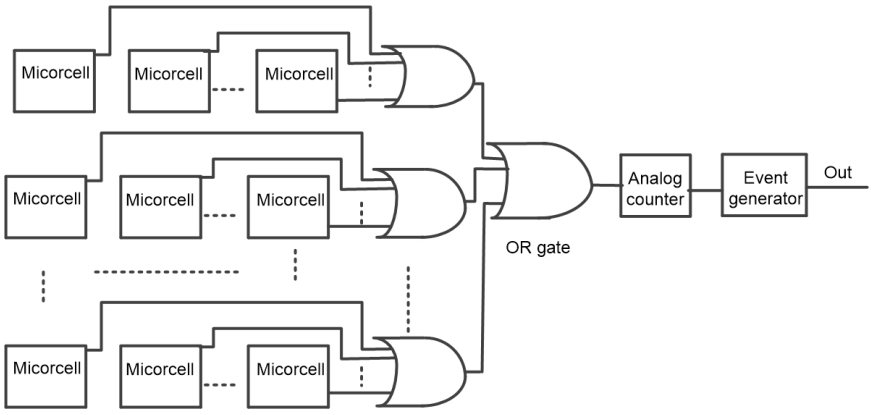



**Figure 4.5:** Pixel of digital SiPM which includes microcells based on the perimeter gated SPAD, analog counter, and event generator ( [114] ©2018 IEEE).

and is implemented for low light imaging applications. The designed AER readout is based on the original AER readout introduced in [115].

## 4.3 Architecture of the Designed PGSPAD based Pixel

The pixel of the digital SiPM, mini-digital SiPM, uses the PGSPADs which reduces the dark current/count and makes the device have a tunable dynamic range. The complete block diagram of the PGSPAD based pixel is shown in Figure 4.7. For this prototype design nine microcells, based on the PGSPAD, are used. The system consists of an analog counter for compact and low power implementation and an event generator for AER readout. For this prototype design, nine microcells are implemented. Figure 4.6 shows the photomicrograph of the pixel of a digital SiPM which includes nine microcells based on the perimeter gated SPAD, an analog counter, and an event generator. In the following subsections, each block of the pixel of the digital SiPM is described in detail.

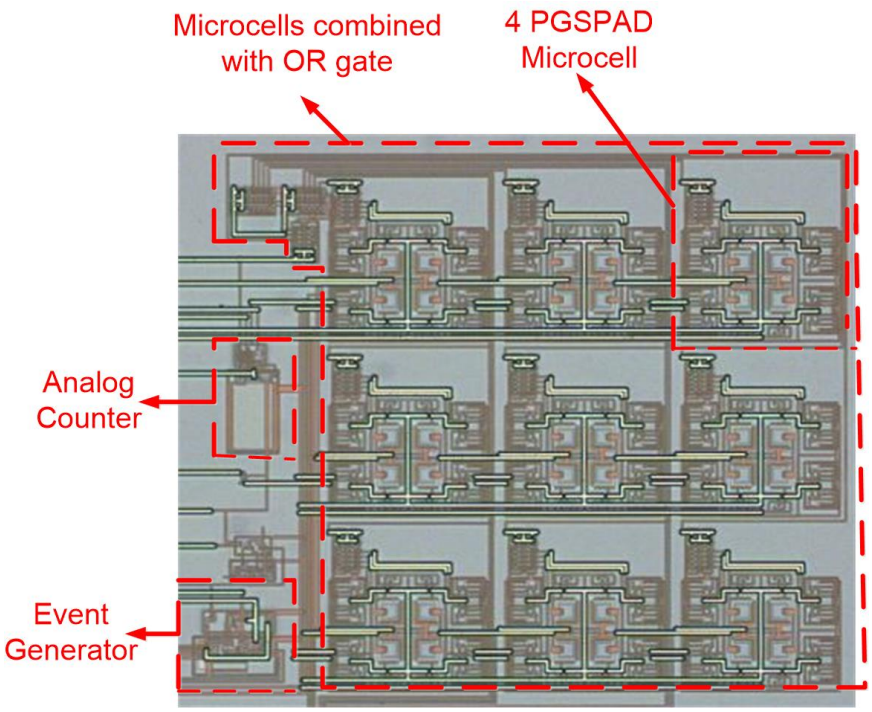



**Figure 4.6:** Photomicrograph of pixel of digital SiPM fabricated in 0.5 $\mu$m CMOS process which includes microcells based on the perimeter gated SPAD, analog counter, and event generator.

### 4.3.1 PGSPAD based Microcell

The designed PGSPAD microcell is shown in Figure 4.7. Each microcell uses 4 identical parallel PGSPADs instead of a single larger PGSPAD of same size as the sum of the four. This improves the temporal resolution of the device by reducing the dead time [122]. Here, dead time is defined as the period during which the PGSPAD is insensitive to any incident photons. This occurs when the PGSPAD is undergoing avalanche or quenching. Since the relation between the noise characteristics and the SPAD area is more-than-linear [123], use of a 4-PGSPAD pixel instead of a single larger PGSPAD also improves the noise performance. PGSPADs are able to modulate their breakdown voltage resulting in devices with the ability to tune the dark count, efficiency and measurement range of the device.

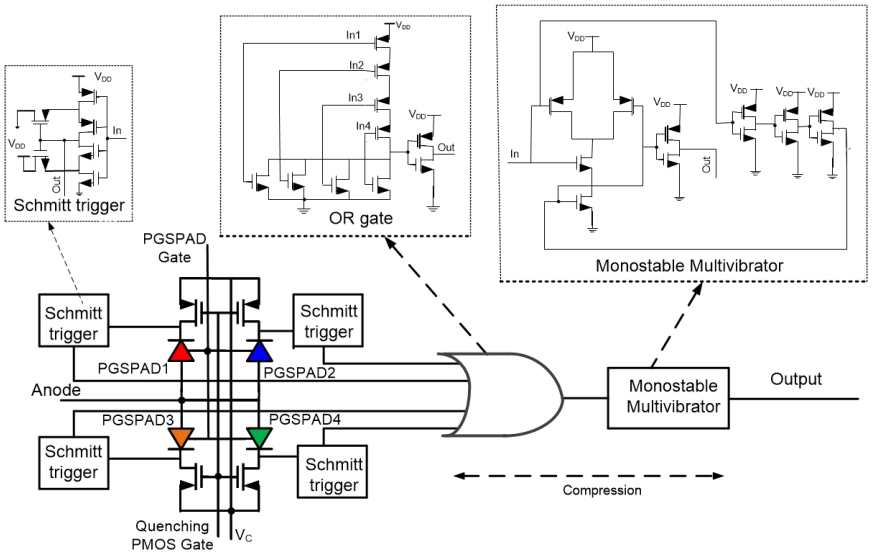



**Figure 4.7:** Schematic of the designed microcell based on PGSPAD ( [113] ©2018 IEEE).

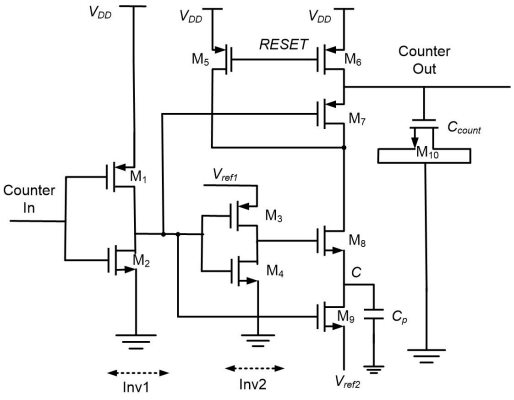
A common bias is applied to the anodes of all the devices. Similarly, a common bias is applied to all the perimeter gates. For quenching of the avalanche current, a linear region transistor is used instead of a resistor to improve the fill factor. Once a PGSPAD undergoes avalanche, the voltage across the device is reduced by the voltage developed across the quenching resistor due to the avalanche current. This results in the device leaving the breakdown region and being reset. During this cycle, the SPAD is in what is known as the dead time and is unable to respond to subsequent photons. Each PGSPAD of the four PGSPADs is able to respond to photons independently. That is, if any of the devices is avalanching or being quenched, one of the other three PGSPADs is able to respond to incoming photons. This therefore results in an overall reduction in the dead time of the combined 4-PGSPADs. Further reduction in the dead time can be accomplished by further subdividing the PGPSADs. A Schmitt trigger performs the required signal processing and a simple OR gate achieves signal digitization. This also has the effect of improving spatial compression. Finally, temporal compression is improved by using a monostable

multivibrator to reduce the pulse width after the digital logic. This has the effect of further improving the device dead time.

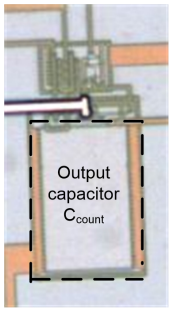
### 4.3.2 Analog Counter

The absolute value of the SPAD avalanche current is irrelevant making SPADs inherently digital devices, where an output is recorded only if there is a photon (or noise) triggered avalanche. Therefore, a pulse counter is used in order to provide temporal integration. Analog counters, an alternative to digital counters requiring large area and higher power, provide a more compact implementation, improving fill factor with lowered power consumption. The designed analog counter uses the concept of charge transfer [124]. The schematic of the designed analog counter and photomicrograph are shown in Figure 4.8.

When a SPAD triggers, due to an incident of a photon, a pulse with width of few nanoseconds is generated at the output of the microcell as described in previous subsection. This output pulse is the input of the analog counter. An inverter, $Inv1$, isolates the PGSPAD from the rest of the readout circuitry. $C_P$, the parasitic capacitance across the $M_9$




(a)




(b)

**Figure 4.8:** (a) Schematic of the designed analog counter ( [113] ©2018 IEEE). (b) Photomicrograph of the analog counter fabricated in 0.5 $\mu$m CMOS process.

transistor, depending on the existence of an incoming photon, is charged or discharged to a reference voltage. Finally, the collected charge is moved to the output capacitance, MOS capacitance $C_{count}$, where the charging and discharging of the capacitor in response to each photon results in discrete analog voltages. Initially, $C_{count}$ is precharged to $V_{DD}$ by applying the *Reset* signal. When the $CountIn$ is low, no photon is detected, and $C_P$, through the drain of $M_9$, is charged to ground potential. When a photon is detected, $CountIn$ is high, $M_7$ and $M_9$ are forced to switch on and off driven by inverter, $Inv2$. The change in the voltage at the gate of $M_8$, from ground to $V_{ref}$ supplied by $Inv2$, causes a voltage change at drain of $M_9$ resulting in a proportional charge transfer to this node through $M_8$. Finally, the charge is collected from $C_{count}$ for each avalanche event. The change in the output voltage, $V_{out}$ is,

$$\Delta V_{out} = (V_{ref} - V_{th8}) \frac{C_P}{C_{count}} \tag{4.1}$$

where $V_{th8}$ is the threshold voltage of the transistor $M_8$.

### 4.3.3 Event Generator

Since SPADs trigger on the incident of a photon, they are naturally event-based and therefore suitable for address-event representation, AER readout approaches. In order to realize the efficient fully digital AER readout at the detector for a large digital silicon photomultiplier, an event generator is designed at the pixel level, the mini digital silicon photomultiplier. Figure 4.9 shows the schematic and photomicrograph of the designed event generator and which is based on the original well known architecture [115].

The analog counter's output voltage, $V_{CountOut}$, is compared with a reference threshold voltage, $V_{thresh}$, using a comparator. When $V_{CountOut}$ crosses the specified $V_{thresh}$ in

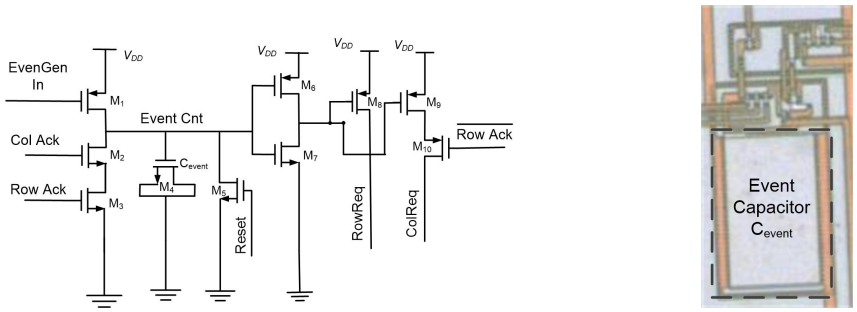



**Figure 4.9:** (a) Schematic of the designed event generator ( [113]©2018 IEEE). (b) Photomicrograph of the event generator fabricated in 0.5 $\mu$m CMOS process.

response to a pulse at the counter input detecting a photon, a logic 0 signal is produced at the output of the comparator. The output of the comparator is the input of the event generator $EvenGenIn$ (Figure 4.9). The input PMOS, $M_1$ is turned on upon receiving a logic 0 signal from the comparator. The storage capacitor, $C_{event}$, is charged indicating an event has occurred. In order to send the event occurrence to the top level, a row request, $Rowreq$, is sent by a pull-up switch, $M_8$, driven by the voltage across $C_{event}$ fed through an inverter. Then, the row request is acknowledged at the top level enabling the column request, $Colreq$, of that particular pixel through another pull-up switch, $M_9$, driven in a similar way to $Rowreq$. Once the event generator of a particular mini-digital SiPM receives the row acknowledgement, $RowAck$, and column acknowledgement, $ColAck$, the $C_{event}$ discharges to ground through turning on the series NMOS switches, $M_2$ and $M_3$, resetting the event generator. $M_2$ and $M_3$ transistors are made stronger than the pull up transistor $M_1$ to ensure that the $EventCnt$ node ($C_{event}$) is pulled down once $RowAck$ and $ColAck$ are received, independent of the $CompOut$ status.

## 4.4 System Architecture

Figure 4.10 shows the system architecture of the PGSPAD based digital SiPM with AER readout. For this prototype design, a 4 × 4 pixel array is implemented in standard 0.5 $\mu$m CMOS process. The photomicrograph of the PGSPAD digital SiPM with AER readout is presented in Figure 4.11. Each pixel consists of 36 PGSPADs, the analog counter, and the event generator. In order to resolve contentions causing data loss or errors, a fully arbitrated row-column architecture is employed in the system.

### 4.4.1 Arbiter

An arbiter is essential to the success of an AER protocol. By using a high gain positive feedback, the arbiter chooses one of the incoming requests for transmission avoiding the

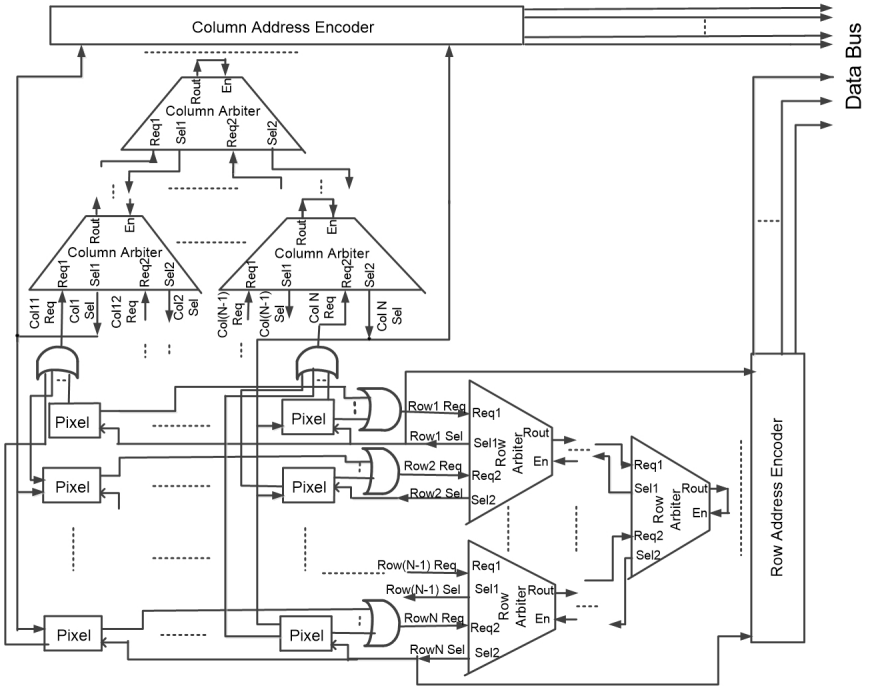



**Figure 4.10:** Block diagram of the system architecture ( [114] ©2018 IEEE).

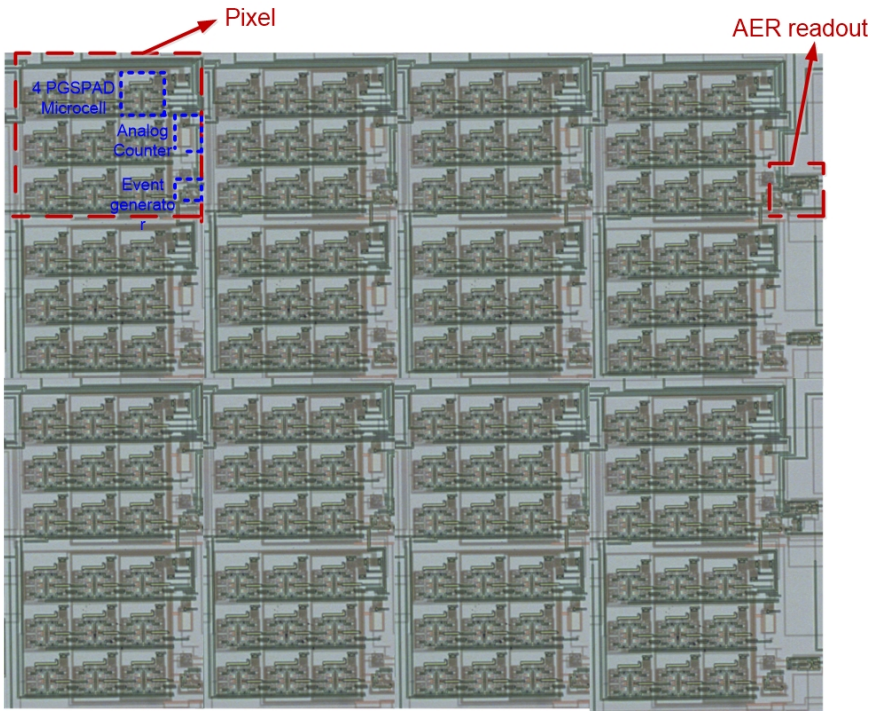



**Figure 4.11:** Photomicrograph of a 4×4 of digital SiPM using PGSPAD with AER readout fabricated in 0.5 $\mu$m CMOS process .

conflict. Figure 4.12 shows the basic one-dimensional arbiter as a binary tree of simple arbiter component. For every two rows or columns, one arbiter is required at the bottom level of binary tree. Therefore, if the total number of rows or columns is $N$, the number of arbiter is $N-1$. The function of each arbiter is to pick one of the request among the two arriving requests and to send back the select from the top level to the selected request. If it is selected by the top level arbiter, neither of the arriving requests is chosen. The amount of time needed for a request to pass to the top level of the tree and the select to pass back down defines the time needed to finish the arbitration. The total delay associated with the arbiter is equivalent to $log(N)$. Since the arbitration is happened in parallel at each level, the delay due to the arbitration increments only slightly with $N$ [115].

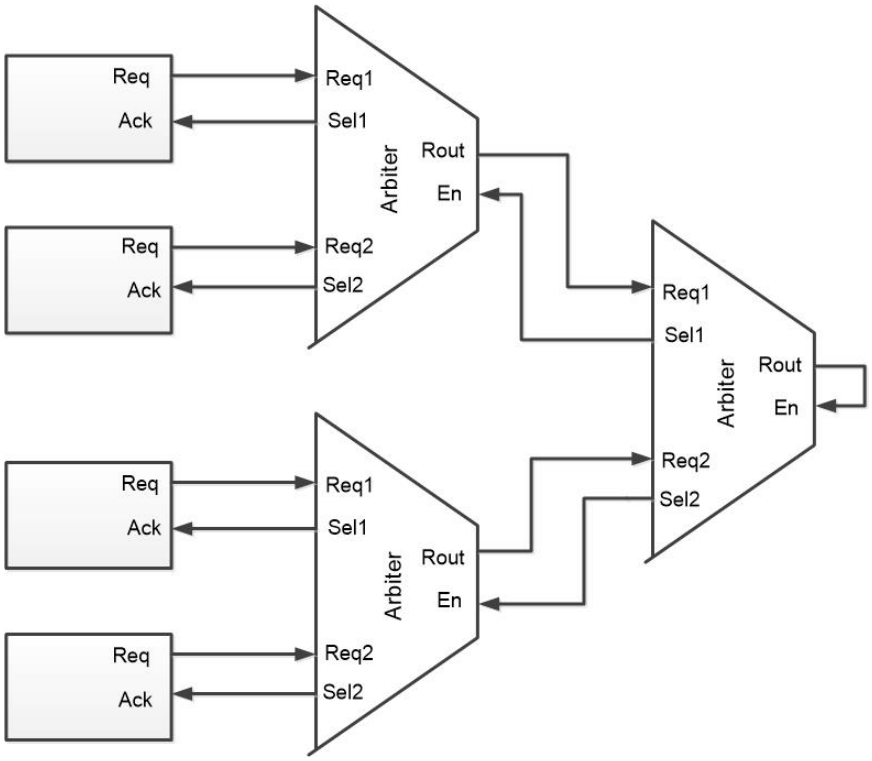



**Figure 4.12:** The arbiter is a a binary tree of two-input arbitration units. Each unit receives two requests from bottom and an acknowledgement from the top. It sends a request to the higher level of the tree and passes down two acknowledgements [115].

The schematic of the arbiter based on the first arbiter reported in [115] is shown in Figure 4.13 . Figure 4.14 shows the photomicrograph of the arbiter fabricated in 0.5 $\mu$m and 180 nm CMOS processes. If either incoming request, $Req1$ or $Req2$, is activated, the arbiter is first enabled through the OR gate. Two cross coupled NAND gates implement the decision circuit to ensure that only one request will be selected even if both requests are active. The signals $Req1'$ and $Req2'$ indicate which request has been chosen by the arbiter. Therefore, when the $Req1'$ is low, the $Req1$ has been picked up. The chosen request by the decision circuit will drive the corresponding select signal high through the driving circuit. The driving circuit performs as a differential amplifier which is enabled by the incoming

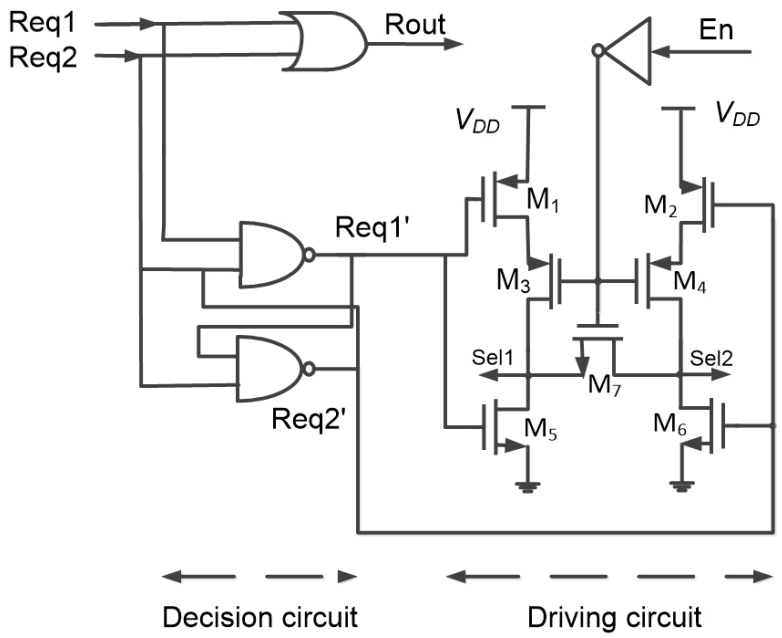



**Figure 4.13:** Schematic of the designed arbiter ( [113] ©2018 IEEE).




**Figure 4.14:** Photomicrograph of the arbiter (a) fabricated in 0.5 $\mu$m CMOS process, (b) fabricated in 0.35 $\mu$m CMOS process.

enable signal, $En$. The driving circuit passes the enable signal coming from the next level of the tree to the descending select output corresponding to the picked request.

The intercommunication between the decision circuit and the select driving circuit is the most important part for secure arbitration. There is a possibility that the select signal might be activated before a clear decision has been made. In order to avoid the select signal passing down to the tree before the decision and to avoid the undecided state of decision circuit, M5/M6 has been made strong relative to M1/M2.

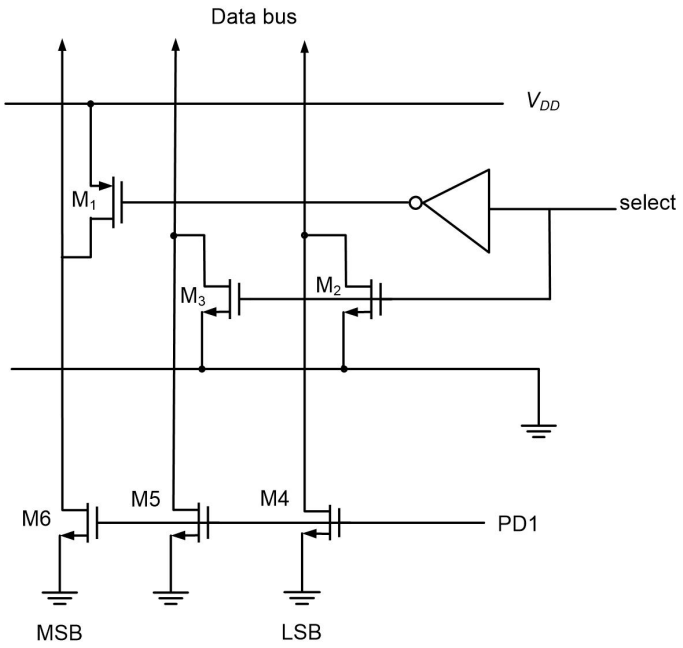



**Figure 4.15:** Schematic of the row address encoder for 3-bit row address of 100.

### 4.4.2 Address Encoder

Once the row of a triggered pixel has been selected by the corresponding row arbiter, the row address encoder encodes that particular row address and transmits into the data bus in parallel. When the row is selected by the row arbiter, the column request of that pixel is initiated. The column arbiter selects that particular column and the column address is transmitted after encoding by the column address encoder. A data valid bit has been included in the address encoder to allow time for the stabilization of the address lines and to indicate the valid time for address readout. For this design, we used 3-bits for row address and 3-bits for column address, with 1-bit for data valid. Figure 4.15 demonstrates the row address encoder for a simple 3-bit row address with the specific value 100. The encoder is designed based on [115]. Once the address encoder is stimulated by the select signal from the corresponding arbiter, the address bits are put onto the address lines. In order to ensure

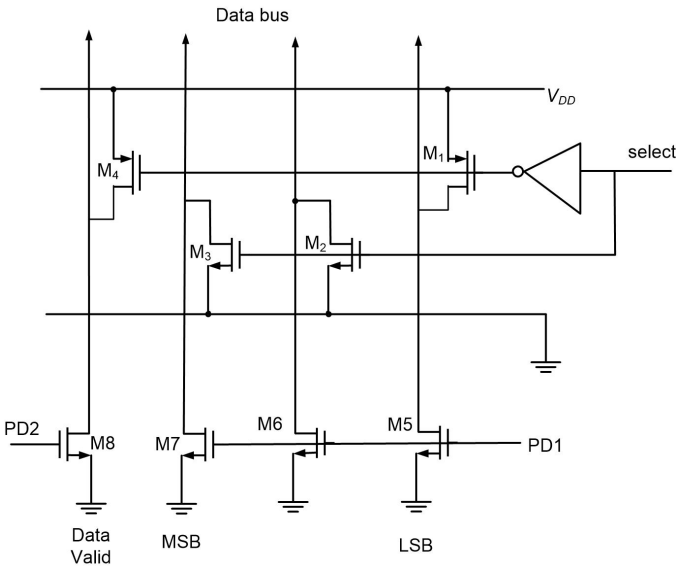



**Figure 4.16:** Schematic of the column address encoder for 3-bit column address of 001 with data valid bit.

that the address go to all zeros when none of the pixel is selected, pull-down transistors are included.

Figure 4.16 explains the column address encoder for a simple 3-bit column address with the specific value 001. The pull-down transistor of data valid bit, PD2, is made stronger than the pull-down transistor of the address bits, PD1. Therefore, the data valid bit approaches to high more gradually and goes to low more rapidly than the address bits.

## 4.5 Simulation and Experimental Results

### 4.5.1 Simulation Results

Cadence is used to simulate the PGSPAD microcell and the whole system of digital SiPM based on PGSPAD microcell with AER readout using a previously developed PGSPAD SPICE model [42]. The model is derived from previously fabricated devices, and is capable

of accurately emulating the IV curve and change in breakdown voltage as well as the development of the avalanche current due to an incoming photon. Additionally, noise or dark events have been added to this model. The additional gate terminal can be used to tune the mismatch of PGSPADs. Therefore, in this design, most of the errors due to mismatch related to the dependence on process variation is due to the analog counter.

#### 4.5.1.1 Results of PGSPAD based Microcell

The PGSPAD based microcell, mini-digital silicon photomultiplier, is implemented in a commercial 0.5 $\mu$m 2−poly, 3−metal CMOS process. The size of each PGSPAD in the microcell is 10 $\mu$m $\times$ 10 $\mu$m. From prior characterization experiments, a quenching resistor of 100 k$\Omega$ is a suitable value. Thus the triode region PMOS was biased accordingly. The timing diagram (Figure 4.17) shows the microcell's output. Upon an incident photon, PGSPAD1 generates an avalanche current giving rise to a digital output after the logic gate. While PGSPAD1 is unresponsive, i.e. there is still an appreciable avalanche current and the reverse bias voltage is still below the breakdown voltage, PGSPAD3 is able to respond to a second photon giving rise to a positive output at the logic gate. In this simulation, three photons are impinged on the 4-PGSPAD pixel within the non-responsive time of PGSPAD1 and all four including the first photon triggering the PGSPAD1 are detected after the logic gate. This validates the improvement in dead time of the designed microcell shown in Fig. 4.17. The improved dead time is less than 0.25 of the dead time of a single larger PGSPAD of same area. The monostable multi vibrator reduces the pulse width from 1 $\mu$s, is reduced to 100 ns (Figure 4.17).

#### 4.5.1.2 Results of 4× 4 PGSPAD Digital SiPM with AER

The whole system, PGSPAD digital SiPM (an array of 4 × 4 pixels) with designed AER readout was simulated. The response of the triggered pixels pixel1, P1, and pixel16, P16, (located at diagonally opposite sides of the array) are reported. Figure 4.18 shows the

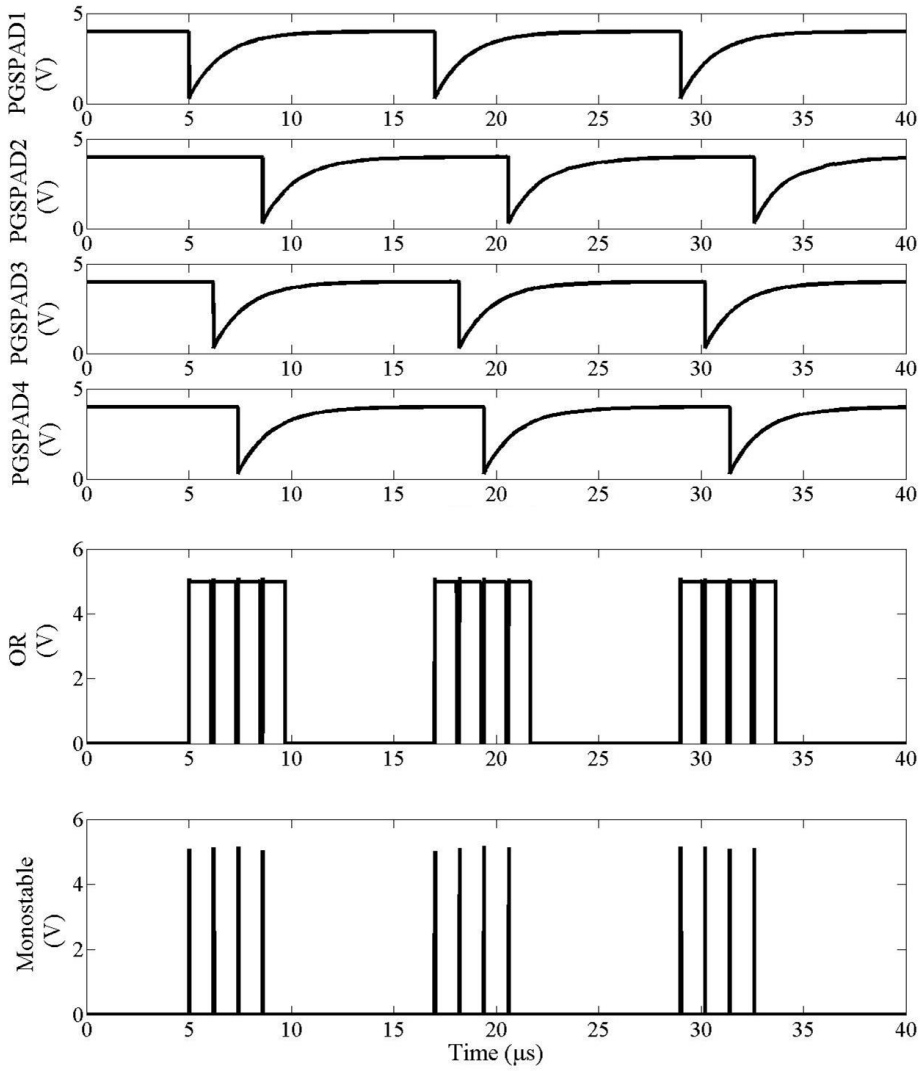



**Figure 4.17:** Simulated timing diagram of microcell. Each PGSPAD of the microcell can independently respond to incoming photons. Each output avalanche is digitized ( [113] ©2018 IEEE).

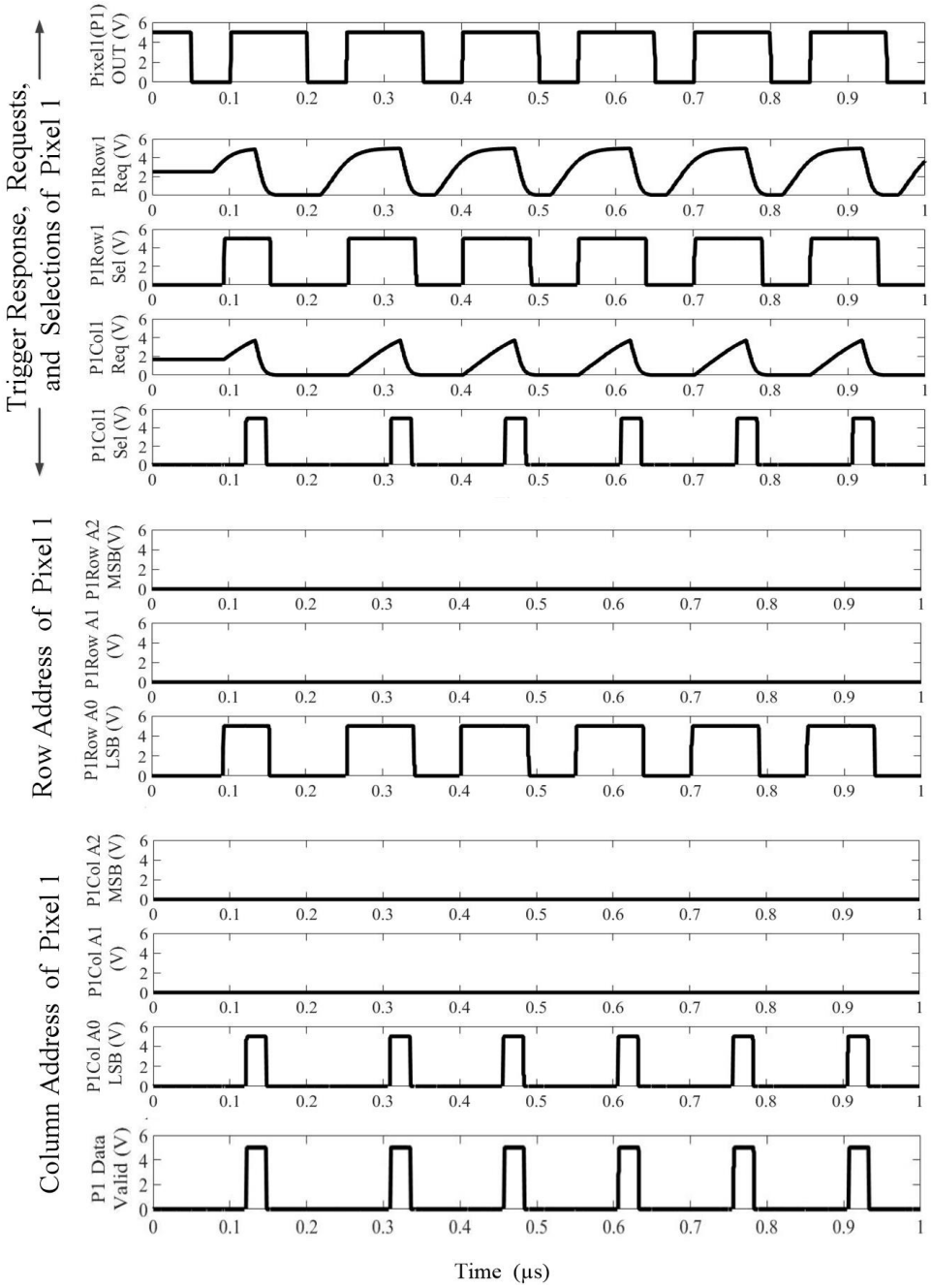



**Figure 4.18:** Simulated triggering response of pixel1 and resulting requests, selections. Once it is selected the address encoder puts its row address of pixel1 (001) and column address (1001) with data valid bit high indicating the valid address readout time ( [114] ©2018 IEEE).

simulated timing diagram of the triggering response of pixel1 and resulting requests and selections.

The pixel P1 output goes low once it is triggered upon the incidence of a photon. P1 sends the row request, $P1Row1\ Req$, to the row arbiter. Once the row arbiter selects the row request of P1 through $P1Row1\ Sel$, initiating the column request for P1 and enabling the row address encoder. The address encoder encodes the row address of P1 through $P1Row\ A2$ to $P1Row\ A0$ signals (001) and transmits it to the data bus (Figure 4.18). When the column of P1 is selected by the column arbiter through the $P1Col1\ Sel$, the column address encoder is enabled. The address encoder encodes the column address of P1 through $P1Col\ A2$ to $P1Col\ A0$ signals (001) and transmits it to the data bus with high data valid bit (Figure 4.18). The output addresses remains in the data bus until their acknowledgement.

Figure 4.19 shows the simulated timing diagram of the triggering response of pixel16 and resulting requests and selections. The pixel P16 output goes low once it is triggered upon the incidence of a photon. P16 sends the row request, $P16Row4\ Req$, to the row arbiter. Once the row arbiter selects the row request of P1 through $P16Row4\ Sel$, initiating the column request for P1 and enabling the row address encoder. The address encoder encodes the row address of P16 through $P16Row\ A2$ to $P1Row\ A0$ signals (100) and transmits it to the data bus (Figure 4.19). When the column of P16 is selected by the column arbiter through the $P16Col4\ Sel$, the column address encoder is enabled. The address encoder encodes the column address of P1 through $P16Col\ A2$ to $P1Col\ A0$ signals (100) and transmits it to the data bus with high data valid bit (Figure 4.19). The output addresses remains in the data bus until their acknowledgement.

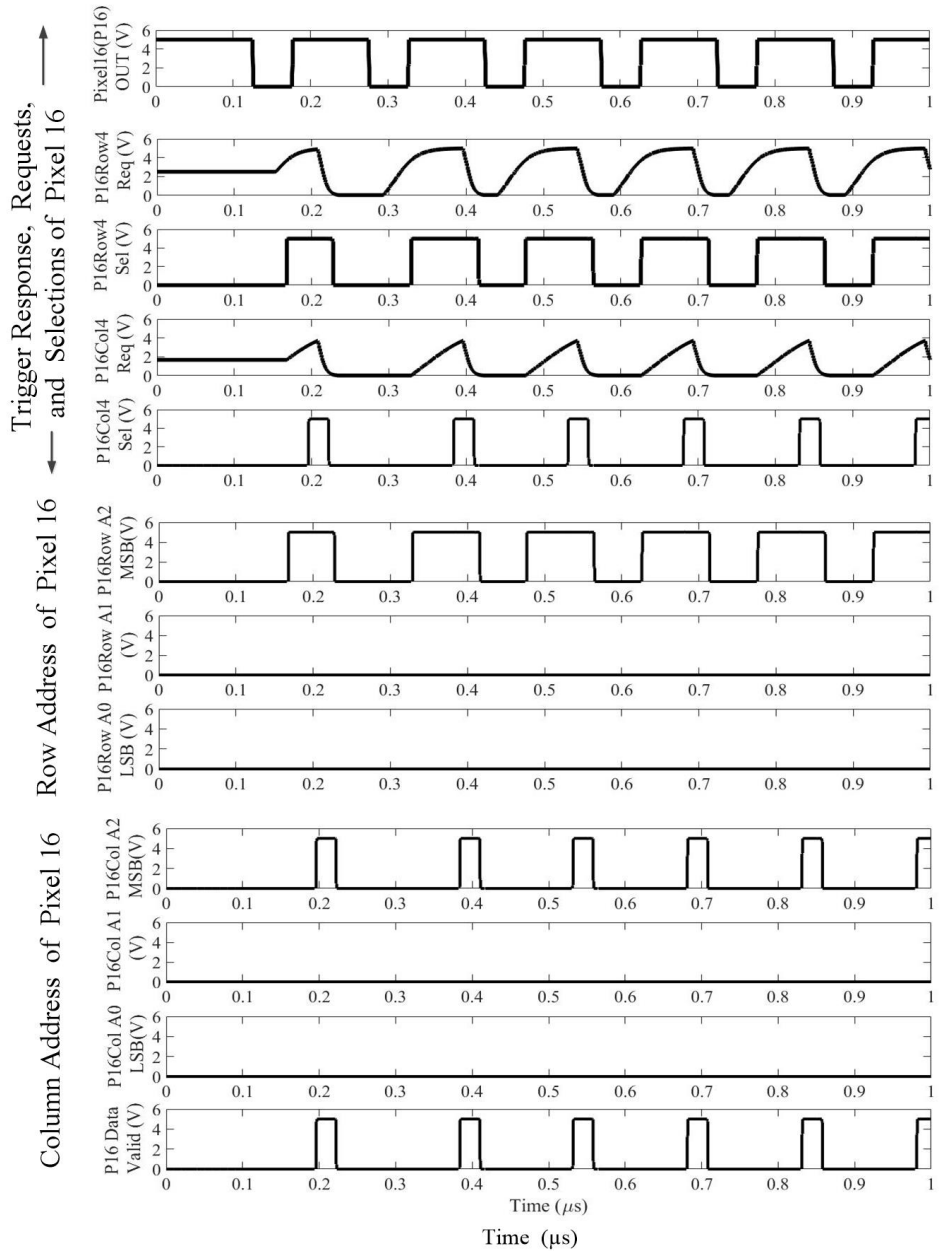



**Figure 4.19:** Simulated triggering response of pixel16 and resulting requests, selections. Once it is selected the address encoder puts its row address of pixel1 (100) and column address (1001) with data valid bit high indicating the valid address readout time ( [114] ©2018 IEEE).

## 4.5.2 Experimental Results of Parts of AER readout

### 4.5.2.1 Response of Analog Counter

The analog counter has been designed and fabricated in a 0.5 $\mu$m standard CMOS process. The counter takes up an area of 243.25 $\mu m^2$ and consumes power of 161 nW at $V_{DD}$ of 5 V

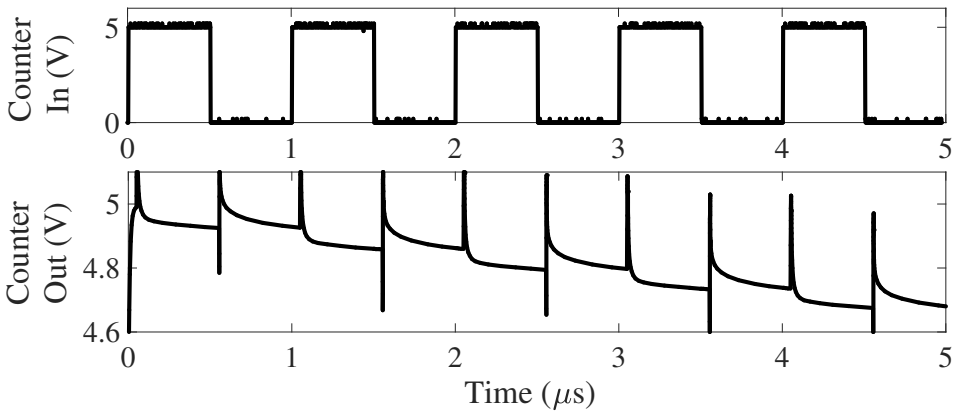



**Figure 4.20:** Measured output of the designed analog counter fabricated in 0.5 $\mu$m CMOS process.

with an external triggering pulse with period of 1 $\mu$s representing the SPAD ignition. Figure 4.20 shows the measured response of the analog counter. Each input pulse of analog counter, $CountIn$, produces a step decrease in voltage at the output of the counter, $CountOut$, shown in Figure 4.20. The subsequent pulse generates a new voltage decrements at $CountOut$ verifying the proper operation of the designed counter. Considering the thermal noise, single photon counting is guaranteed by a voltage increment of ≈3-5 mV [124]. The minimum voltage increment, at the incoming pulse, of around 78 mV is measured at the output of the designed counter. This is higher than the required voltage increment for photon counting with counting resolution of 8 bits. Adjusting the reference voltage affects the time resolution and voltage increment. For this PGSPAD based design, $V_{ref}$ of 3.5 V is used. A positive voltage step is occurred at the output during transition due to the clock feed through and charge injection from $M_7$ of the counter (Figure 4.8).

To minimize this effect, the output capacitance, $C_{count}$, should be designed as large as possible. In this design. $C_{count}$ is set to 350 fF and the size of $M_3$ was kept minimum.

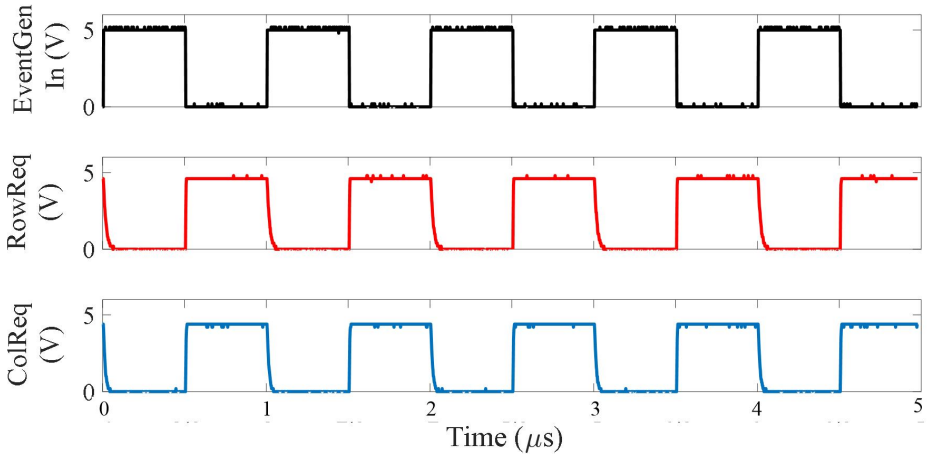



**Figure 4.21:** Measured response of event generator fabricated in 0.5 $\mu$m CMOS process which sends row request and column request of the pixel when it is triggered.

Due to charge injection and clock feedthrough of the *Reset* switch and inverter, spikes are observed at the counter output during transitions.

#### 4.5.2.2 Response of Event Generator

Figure 4.21 shows the measured output of the designed event generator fabricated in a 0.5 $\mu$m standard CMOS process. The voltage at the node $EventCnt$ goes high through charging of the $C_{event}$ capacitor when it receives response from analog counter due to the triggering of a pixel. Once the event generator received the date pulse due to avalanche, it sends RowReq and ColReq of that pixel to the top level. The voltage at the node $EventCnt$ goes low resetting the event generator through discharging of the $C_{event}$ capacitor after receiving the $RowAck$ and $ColAck$ from the top level of the detector.

#### 4.5.2.3 Characterization of Arbiter

The measured response of the individual arbiter fabricated in 0.5 $\mu$m CMOS process is shown in the Figure 4.22. The arbiter has been designed and fabricated in 0.5 $\mu$m standard

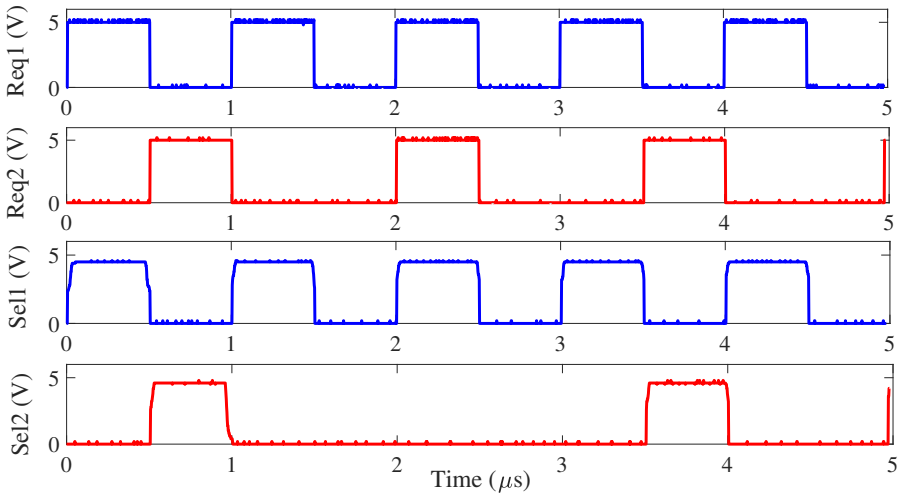



**Figure 4.22:** Measured response of arbiter fabricated in 0.5 $\mu$m CMOS process.

CMOS process. Two pulsed voltage sources are used to supply the inputs, $Req1$ and $Req2$. The measured output shows that when only $Req1$ input is high the arbiter selects the request by setting the $Sel1$ signal high. The similar response was observed for the high $Req2$ input only. However, when both $Req1$ and $Req2$ (both inputs) are high, only one request is chosen resolving the contention effectively. In this case, it is observed that only $Req1$ is selected through the high $Sel1$ signal even both $Req1$ and $Req2$ inputs are high (Figure 4.22). Figure 4.23 shows the measured response of the individual arbiter fabricated in 0.35 $\mu$m CMOS process. It is also observed that when $Req1$ input is high, that particular request is selected by the arbiter through high $Sel1$ signal. The similar response was observed for the high $Req2$ input results in selection of that request by the arbiter through $Sel2$ signal high.

#### 4.5.2.4 Characterization of Address Encoder

Figure 4.24 shows the measured response of column address encoder fabricated in 0.35 $\mu$m CMOS process for 3-bit column address of 100 with data valid bit high. It is observed that when the column address encoder receives high select signal, the address bit MSB (A2) goes

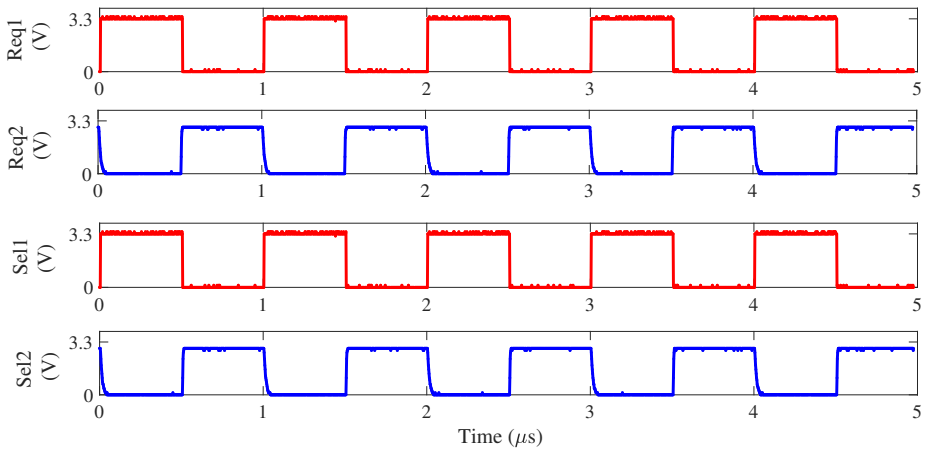



**Figure 4.23:** Measured response of arbiter fabricated in 0.35 $\mu$m CMOS process.

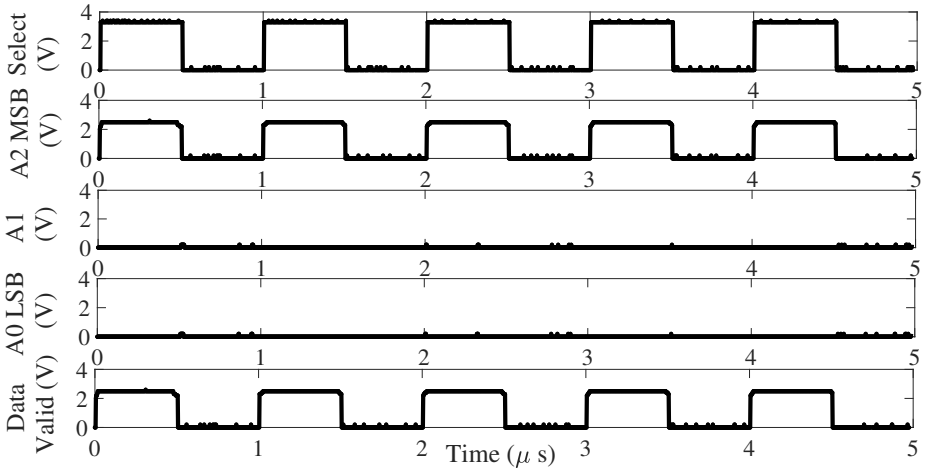



**Figure 4.24:** Measured response of column address encoder fabricated in 0.35 $\mu$m CMOS process for 3-bit column address of 100 with data valid bit high.

high and the other 2 bits of the address A1 and LSB (A0) goes low. The data valid bit also goes high once it receives the select signal indicating the availability of the corresponding address at the data bus.

### 4.5.3 Experimental Characterization of PGSAD Digital SiPM Pixel and SiPM with AER readout

#### 4.5.3.1 Dark Count Rate Characterization of PGSPAD Digital SiPM Pixel

The effect of gate voltage on the noise of the PGSPAD pixel of the SiPM fabricated in 0.5 $\mu$m CMOS process has been characterized. Figure 4.25 shows the variation of dark count rate (DCR) for the pixel, mini-SiPM based on PGSPAD, for variation of applied gate voltage with various excess bias voltages. In order to measure the DCR, the chip is placed inside a dark box to shield it entirely from the light. The reported results are the average result of

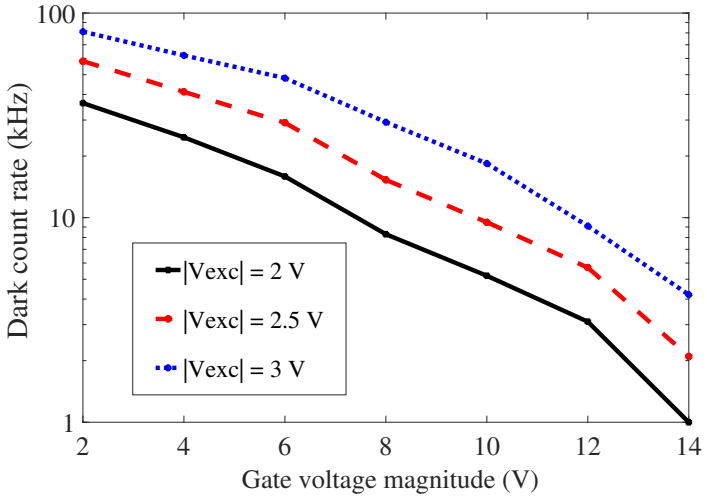



**Figure 4.25:** DCR characterization of PGSPAD based pixel, a mini-SiPM using PGSPAD, fabricated in 0.5 $\mu$m CMOS process for various applied gate voltages and excess bias voltages.

two tested chips where each data was 10s windows with each chip. DCR rises with the raise of excess bias voltage ($V_{exc}$), the excess applied bias voltage above the breakdown voltage, as expected with standard SiPM. However, for a fixed $V_{exc}$, DCR reduces significantly by raising the applied gate bias voltage. This is due to the fact that gate voltage reduces the avalanche probability of generated free carrier due to inter-band tunneling, thermal generation or trapping through modulation of breakdown voltage. Therefore, the noise performance of the digital SiPM can be tuned through the applied gate voltage.

#### 4.5.3.2 Characterization of 4×4 PGSPAD Digital SiPM with AER

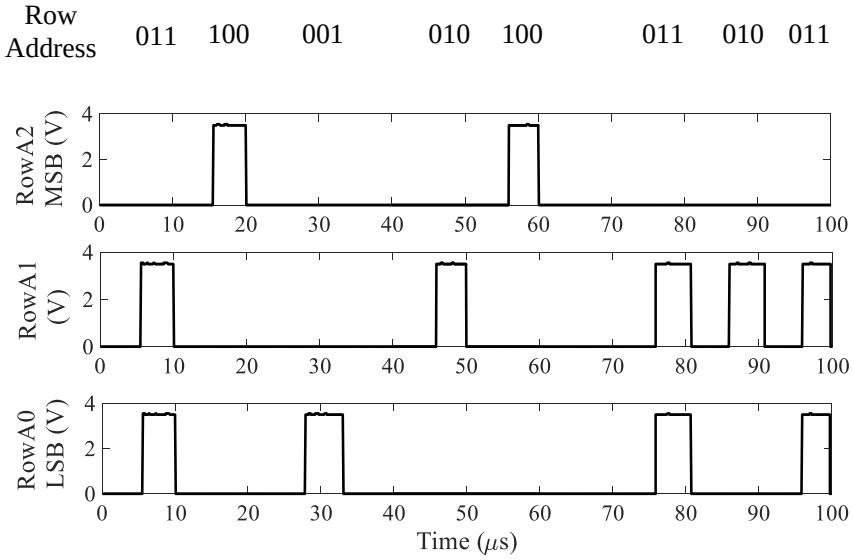
The PGSPAD digital SiPM with asynchronous AER readout has been fabricated in a standard 0.5 $\mu$m CMOS process. In order to characterize the designed PGSPAD SiPM, we used a monochromatic light source, (TLS-300X) which includes the feature to change the wavelength and power. An optical power meter (1936-R) was used to measure the power and an integrating sphere (819D-SL-3.3) was used to couple the light source and the SiPM detector. Two source measuring unit (SMU) were used to provide the anode and gate biasing.

Since the commercially available SiPMs manufactured by Hamamatsu used for the neutron detection including PETs were characterized within the range of $10^8$ - $10^{11}$ photons/s for a wavelength of 500 nm [30, 99, 101, 125, 126], the PGSPAD digital SiPM has been characterized with optical powers from 26 nW$cm^{-2}$ ($6.5 \times 10^{10}$ photons/s) to 130 nW$cm^{-2}$ ($3.2 \times 10^{11}$ photons/s) between those range and a wavelength of 500 nm to make it comparable. Moreover, the power range chosen here to characterize the PGSPAD Digital

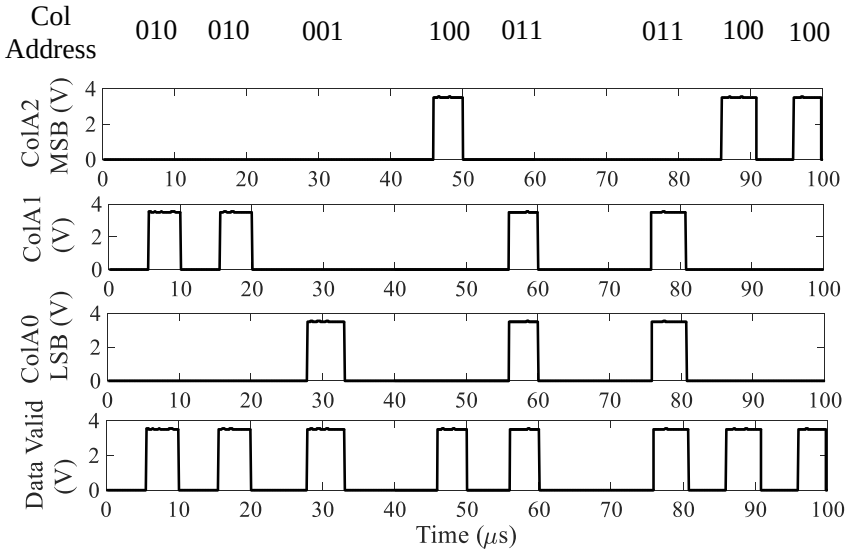
SiPM also used by SensL to characterize their SiPM detectors used for nuclear medical imaging including PET and SPECT [29, 127, 128].

Figure 4.26 shows the measured addresses of the triggered pixels using AER readout for the 4 × 4 pixels PGSPAD digital SiPM. During the measurements, the gate voltage magnitude was 14 V with the excess bias voltage of 0.4 V and the power was kept fixed at 100 nW$cm^{-2}$ ($2.5 \times 10^{11}$ photons/s) with the wavelength of 500 nm. The measured 7-bits address, 3-bits row address, 3-bits column address, and 1-bit data valid, represents the address of the triggered pixel. Since the data valid bit goes high, once a pixel is triggered, the number of triggered pixels is represented by the total number of data valid bit. In other words, the data valid bit represents the total number of detected photons.

When a photon incidents on a pixel, the pixel is triggered and undergoes into avalanche. The pixel sends the request to the corresponding arbiter and selected by the particular arbiter. At the same time the arbiter selects the particular encoder to enable its address sending. The address of that specific pixel is put on the data bus by the corresponding address encoder. From the address readout measurements, it is observed that the first triggered pixels is P10(011, 010). Here, first 3 bits represent the row address and last 3 bits represent the column address with data valid bit high. The next fallowing triggered pixels are P14(100, 010), P1(001, 001), P8(010, 100), P15(100, 011), P11(011, 011), P8(010, 100), and P12 (011, 100) respectively. It is observed that during this duration total 7 pixels are triggered which is equivalent to the 7 detected photons.




**(a)**



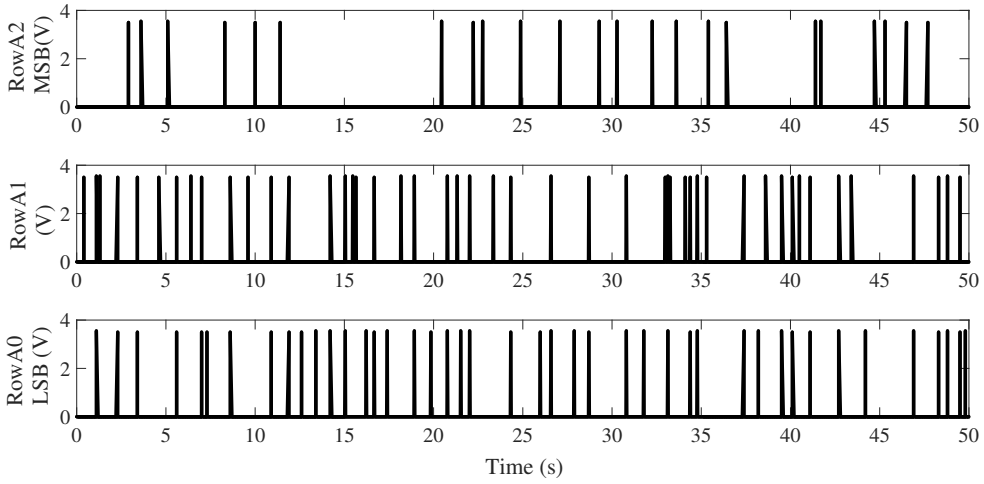

**(b)**

**Figure 4.26:** Measured address readout of the triggered pixels using AER readout for the $4 \times 4$ pixels digital PGSPAD SiPM fabricated in 0.5 $\mu$m CMOS process with optical power of 100 nW$cm^{-2}$ for a time period of 100 $\mu$s (a) Row address (b) Column address with data valid bit.

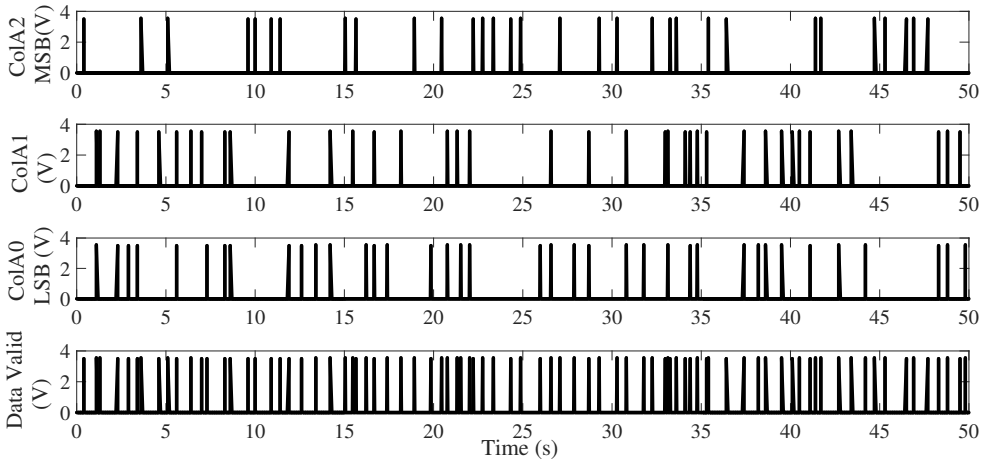
In order to investigate the response of the developed digital SiPM with AER readout with different optical intensity, optical power is varied over a wide range including low to high optical power. The optical power was varied from 26 nW$cm^{-2}$ to 130 nW$cm^{-2}$ and output address was measured for longer time duration of 50 s. When the photon incidents, the triggered pixel's address is put on the address line by the AER readout. The measured 7-bits address, 3-bits row address, 3-bits column address, and 1-bit data valid, represents the address of the triggered pixels which is equivalent to the number of detected photons. Figure 4.27 shows the measured address readout of the triggered pixels of the 4 $\times$ 4 pixels digital SiPM using AER readout with optical power of 26 nW$cm^{-2}$. During the measurements, the gate voltage magnitude was 14 V with the excess bias voltage of 0.4 V. The wavelength was kept fixed at 500 nm.

The measured 3-bits row address is shown in Figure 4.27 (a) while the measured 3-bits column address with 1-bit data valid is shown in Figure 4.27 (b). From the measurement it is observed that, the first triggered pixel is in second row with row address of 010 and in fourth column with column address of 100. At the same time the data valid bit is high to represent the valid time for address readout. The next triggered pixel is in the second row address of 010 and in third column with column address of 011. In a similar way, other following triggered pixels can found out from the measured 7-bit address output.

Input optical power is increased to 42 nW$cm^{-2}$. During the measurement the wavelength was kept fixed at 500 nm and the gate voltage magnitude was 14 V with excess bias voltage of 0.4 V. The measured output for the 4 $\times$ 4 digital SiPM array with AER readout for optical power of 42 nW$cm^{-2}$ is shown in Figure 4.28. The photon flux raises with rise of the optical power increasing the number of triggered pixels. The output address shows




**(a)**




**(b)**

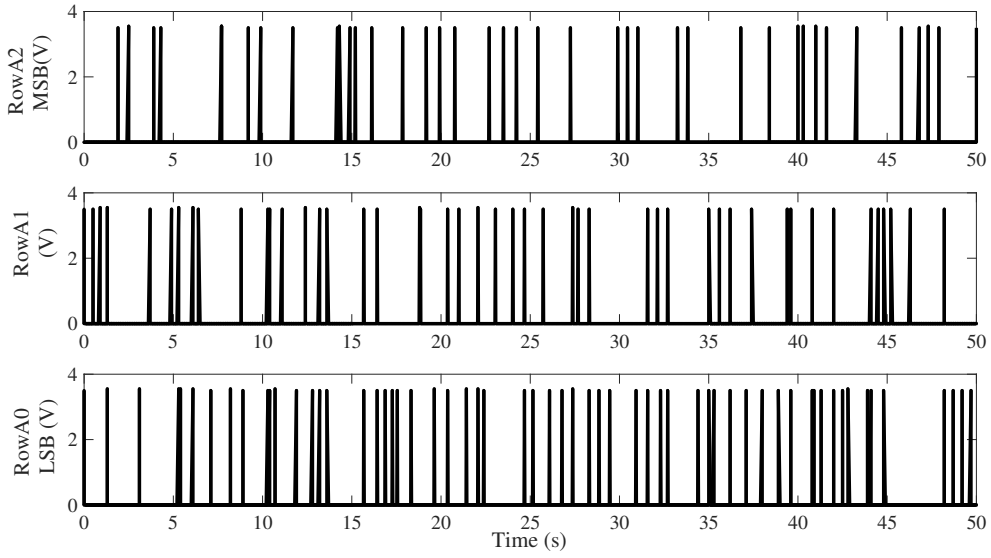
**Figure 4.27:** Measured address readout of the triggered pixels using AER readout for the 4×4 pixels digital PGSPAD SiPM fabricated in 0.5 $\mu$m CMOS process with optical power of 26 nW$cm^{-2}$, (a) Row address (b) Column address with data valid bit.

more addresses are readout with the 42 nW$cm^{-2}$ with compared to that of 26 nW$cm^{-2}$ (Figure 4.27) as expected.

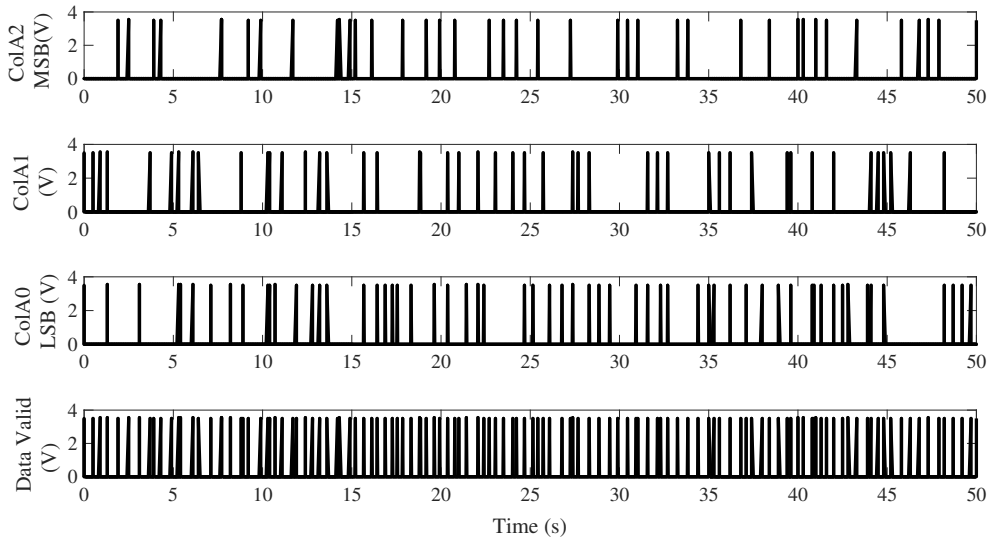
The measured 3-bits row address is shown in Figure 4.28 (a) while the measured 3-bits column address with 1-bit data valid is shown in Figure 4.28 (b). From the measurement it is observed that, the first triggered pixel is in third row with row address of 011 and in third column with column address of 011. At the same time the data valid bit is high to represent the valid time for address readout. The next triggered pixel is in the second row address of 010 and in second column with column address of 010. In a similar way, other following triggered pixels can found out from the measured 7-bit address output. It is also observed that more row addresses and column addresses are measured with input optical power of 42 nW$cm^{-2}$ compared to that with input optical power of 26 nW$cm^{-2}$. This is due to the fact that with the rise of optical power, the number of incident photon increases. As a result, more pixels are triggered and more addresses are available at output data bus.

In order to study the response of the developed digital SiPM with AER readout with higher optical intensity, optical power is increased to 100 nW$cm^{-2}$ and 130 nW$cm^{-2}$. At first, the power is increased to 100 nW$cm^{-2}$. During the measurement the wavelength was kept fixed at 500 nm and the gate voltage magnitude was 14 V with excess bias voltage of 0.4 V.

Figure 4.29 shows the measured address with input optical power of 100 nW$cm^{-2}$. It is observed that more pixel's addresses are available at the address bus compared to that with 26 nW$cm^{-2}$ and 42 nW$cm^{-2}$ shown earlier. This represents that more pixels are triggered indicating more photons are detected. The measured 3-bits row address is shown in Figure




**(a)**



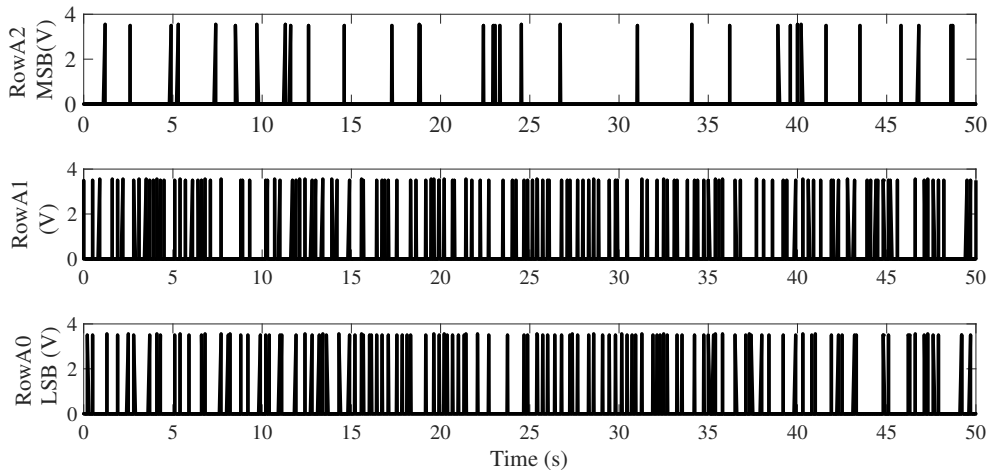

**(b)**

**Figure 4.28:** Measured address readout of the triggered pixels using AER readout for the 4×4 pixels digital PGSPAD SiPM fabricated in 0.5 $\mu$m CMOS process with optical power of 42 nW$cm^{-2}$, (a) Row address (b) Column address with data valid bit.

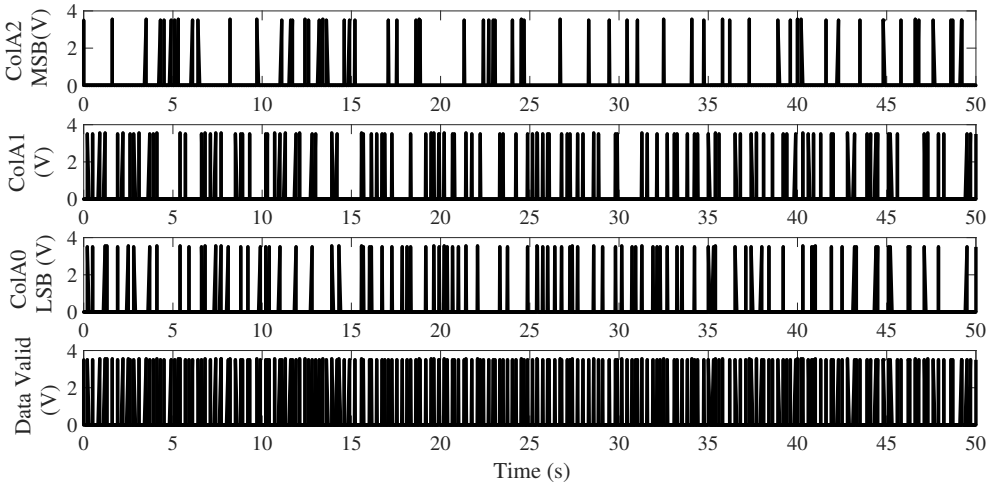
4.29 (a) while the measured 3-bits column address with 1-bit data valid is shown in Figure 4.29 (b).

From the measurement it is observed that, the first triggered pixel is in third row with row address of 011 and in fourth column with column address of 100. At the same time the data valid bit is high to represent the valid time for address readout. The next triggered pixel is in the 1st row address of 001 and in third column with column address of 011. In a similar way, other following triggered pixels can found out from the measured 7-bit address output. It is also observed that more row addresses and column addresses are measured with input optical power of 100 nW$cm^{-2}$ compared to that with input optical power of 42nW$cm^{-2}$ and 26 nW$cm^{-2}$. This is beacuse with the rise of optical power, the number of incident photon increases. As a result, more pixels are triggered and more addresses are available at output data bus as expected.

The input optical power is increased to 130 nW$cm^{-2}$. During the measurement the wavelength was kept fixed at 500 nm and the gate voltage magnitude was 14 V with excess bias voltage of 0.4 V.




**(a)**

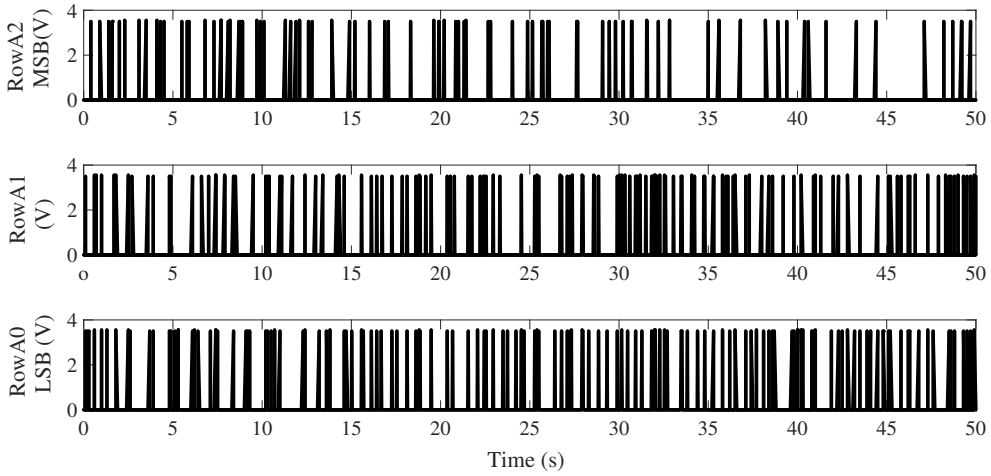



**(b)**

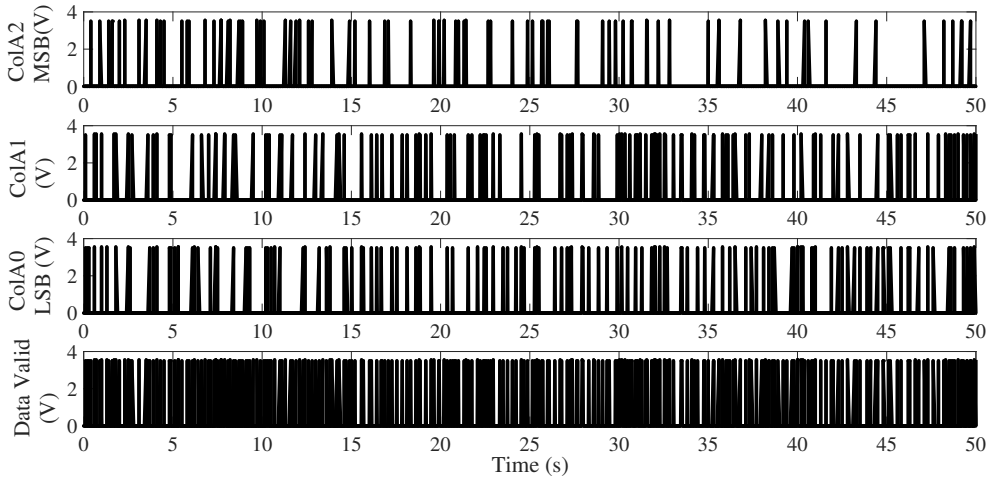
**Figure 4.29:** Measured address readout of the triggered pixels using AER readout for the 4×4 pixels digital PGSPAD SiPM fabricated in 0.5 $\mu$m CMOS process with optical power of 100 nW$cm^{-2}$, (a) Row address (b) Column address with data valid bit.

Figure 4.30 shows the measured address with input optical power of 130 nW$cm^{-2}$. It is observed that more pixel's addresses are available at the address bus compared to that with 26 nW$cm^{-2}$, 42 nW$cm^{-2}$ and 100 nW$cm^{-2}$ shown earlier. This represents that more pixels are triggered indicating more photons are detected. The measured 3-bits row address is shown in Figure 4.30 (a) while the measured 3-bits column address with 1-bit data valid is shown in Figure 4.30 (b).

From the measurement it is observed that, the first triggered pixel is in third row with row address of 011 and in third column with column address of 011. At the same time the data valid bit is high to represent the valid time for address readout. The next triggered pixel is in the fourth row with row address of 100 and in second column with column address of 010. In a similar way, other following triggered pixels can found out from the measured 7-bit address output. It is also observed that more row addresses and column addresses are measured with input optical power of 130 nW$cm^{-2}$ compared to that with input optical power of 100 nW$cm^{-2}$, 42 nW$cm^{-2}$ and 26 nW$cm^{-2}$. This is beacuse with the rise of optical power, the number of incident photon increases. As a result, more pixels are triggered and more addresses are available at output data bus as expected. The increase in triggered pixels are more noticeable with higher power of 130 nW$cm^{-2}$. As a summary, the designed digital SiPM with AER readout responses accurately with a range of input optical power including low and high optical power.




**(a)**



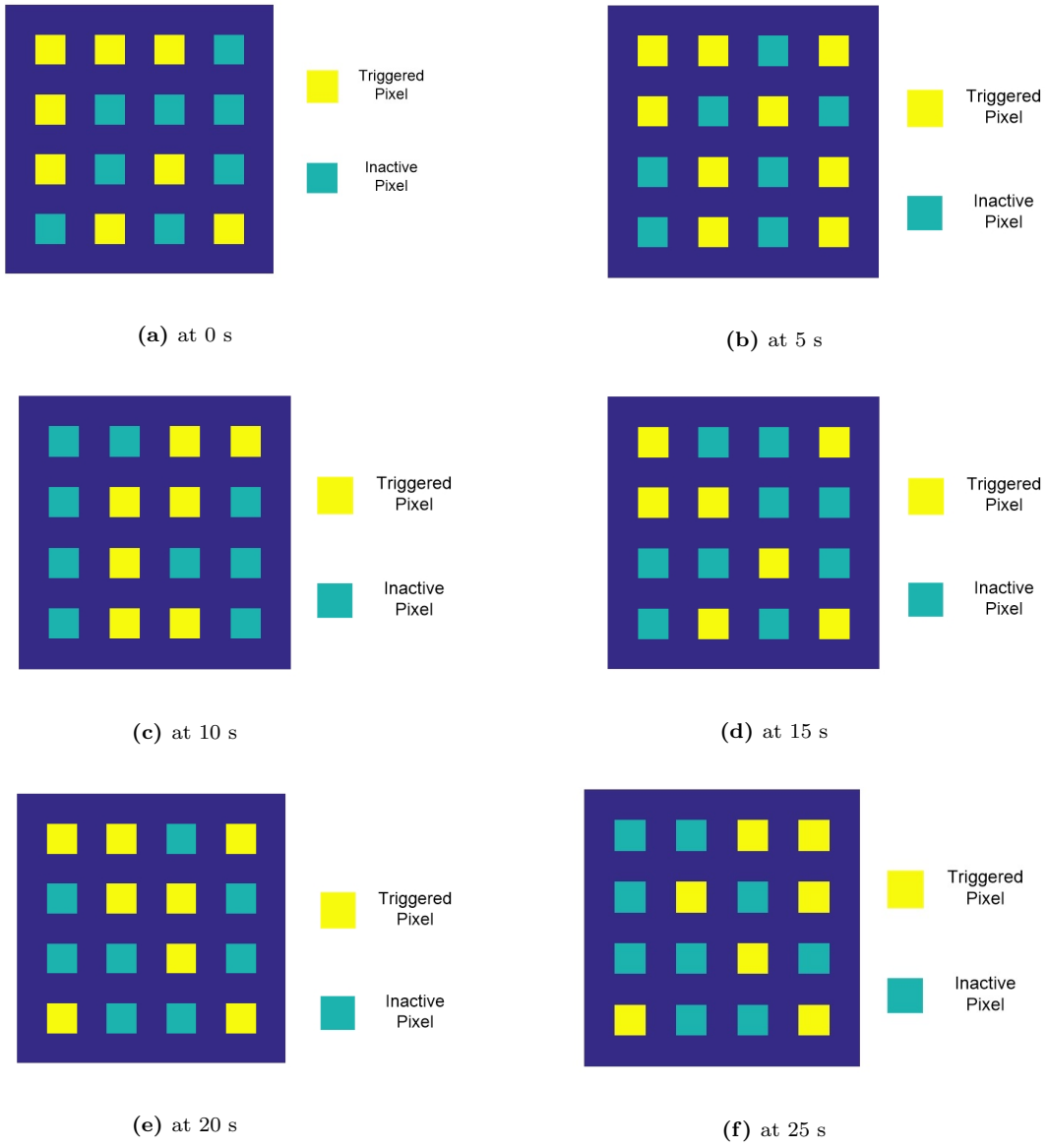

**(b)**

**Figure 4.30:** Measured address readout of the triggered pixels using AER readout for the 4×4 pixels digital PGSPAD SiPM fabricated in 0.5 $\mu$m CMOS process with optical power of 130 nW$cm^{-2}$, (a) Row address (b) Column address with data valid bit.

Photon incidents randomly over the entire array of a 4 × 4 pixels array digital SiPM, an array of PGSPAD based pixel. During the measurements, the gate voltage magnitude was 14 V with the excess bias voltage of 0.4 V. The wavelength was kept fixed at 500 nm. In order to investigate the spreading of the spreading of triggered pixels which is equivalent to the incident photons, triggered pixels are extracted from the measured address output at a particular time. The triggered pixels of the the developed PGSPAD digital SiPM with optical power of 100 nW$cm^{-2}$ was extracted at 5 s interval from the measurement data recorded during 50 s.

A color map of the output of the digital SiPM with AER readout at optical power of 100 nW$cm^{-2}$ is shown in Figure 4.31 from 0 s to 25 s. It is observed that the triggered pixels are pixel1, pixel2, pixel3, pixel5, pixel9, pixel11, pixel14, and pixel16 measured at 0 S. During the address readout at 5 s, the triggered pixels are pixel1, pixel2, pixel4, pixel5, pixel7, pixel10, pixel12, pixel14, and pixel16. It is found that the triggered pixels are pixel3, pixel4, pixel6, pixel7, pixel10, pixel14, and pixel15 at 10 s.

During the address readout at 15 s, the triggered pixels are pixel1, pixel4, pixel5, pixel6, pixel11, pixel13, and pixel6. It is observed that the triggered pixels are pixel1, pixel2, pixel3, pixel6, pixel11, pixel13, and pixel6 at 20 s. During the address readout at 25 s, it is found that the triggered pixels are pixel3, pixel4, pixel6, pixel8, pixel13, and pixel16. As a summary, the triggered pixels are spread at random in the entire array.




**(a)** at 0 s

**(b)** at 5 s

**(c)** at 10 s

**(d)** at 15 s

**(e)** at 20 s

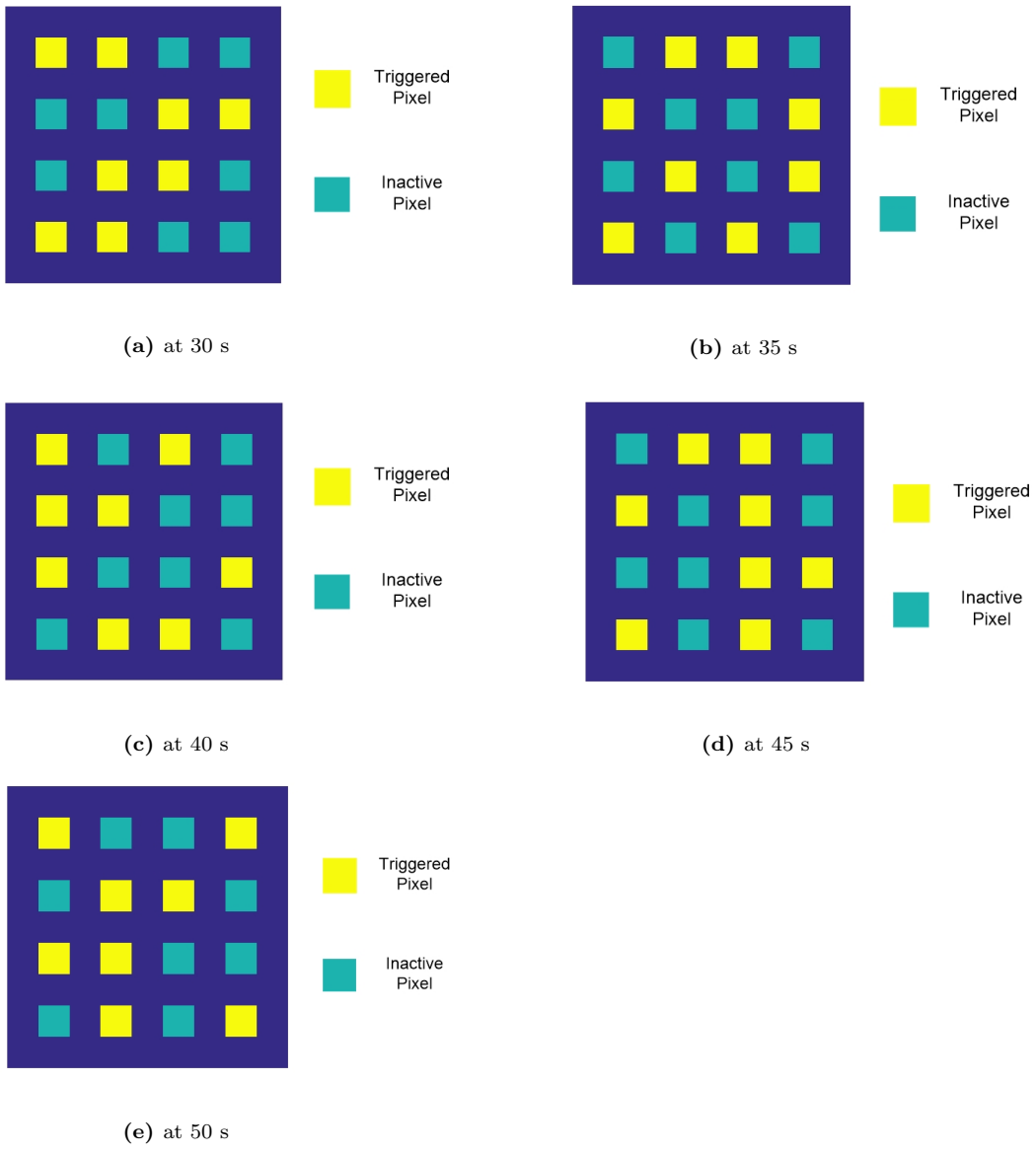
**(f)** at 25 s

**Figure 4.31:** Color map of the output of a $4 \times 4$ PGSPAD based digital SiPM using AER readout with optical power of 100 nW$cm^{-2}$.

A color map of the output of the digital SiPM with AER readout at optical power of 100 nW$cm^{-2}$ is shown in Figure 4.32 from 30 s to 50 s in 5 s step. During the measurements, the gate voltage magnitude was 14 V with the excess bias voltage of 0.4 V. The wavelength was kept fixed at 500 nm. It is observed that the triggered pixels are pixel1, pixel2, pixel7, pixel8, pixel10, pixel11, pixel13, and pixel14 measured at 30 S.

During the address readout at 35 s, the triggered pixels are pixel2, pixel3, pixel5, pixel8, pixel10, pixel12, pixel13, and pixel5. It is found that the triggered pixels are pixel1, pixel3, pixel5, pixel6, pixel9, pixel12, pixel14, and pixel15 at 40 s. During the address readout at 45 s, the triggered pixels are pixel2, pixel3, pixel5, pixel7, pixel11, pixel12, pixel13, and pixel15. It is observed that the triggered pixels are pixel1, pixel4, pixel6, pixel7, pixel9, pixel10, pixel14, and pixel16 at 50 s. During these measurements it is also observed that the triggered pixels are spread at random in the entire array in a similar way obsrved earlier.

Once the particular pixel is triggered due to the arrival of photon, the pixel's address is put on the address bus with data valid bit high. Therefore, the number of data valid bit in a specific time period represents the number of triggered pixels which is equivalent to the number of detected photons during that period. In PET nuclear imaging technique, the total number of detected photon is used to extract one of the important information, the radiation energy of the detected gamma rays. In order to have the information of the detected photons, the data valid bit is measured for a wide range of input optical power from 26 nW$cm^{-2}$ to 450 nW$cm^{-2}$. The total number of triggered pixels through the measured data valid bit for a range of power from 26 nW$cm^{-2}$ to 450 nW$cm^{-2}$ obtained from the testing of chip1 consisting the 4 $\times$ 4 digital SiPM array with AER readout are summarized and compared in Figure 4.33. As the power increases from 26 nW$cm^{-2}$ to 42 nW$cm^{-2}$,




**(a)** at 30 s

**(b)** at 35 s

**(c)** at 40 s

**(d)** at 45 s

**(e)** at 50 s

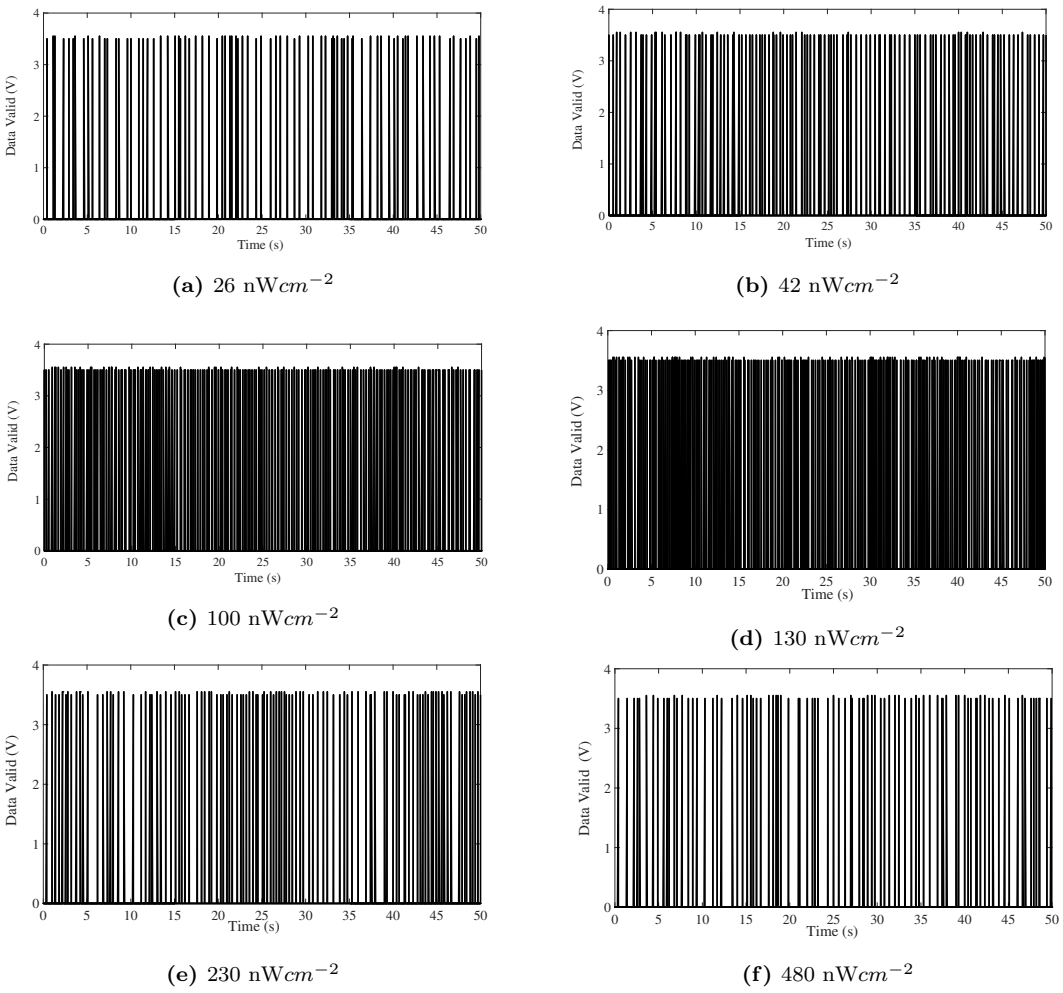
**Figure 4.32:** Color map of the output of a $4 \times 4$ PGSPAD based digital SiPM using AER readout with optical power of 100 nW$cm^{-2}$.

more pixels are triggered due to the increase of photon flux. Therefore, more addresses of the triggered pixels are available at the address bus.(Figure 4.33 (a) and Figure 4.33 (b)).

The input optical power is increased further to 100 nW$cm^{-2}$ and the measured data valid bit during 50 s duration is shown in Figure 4.33 (c). It is noticed that if the power increases further to 100 nW$cm^{-2}$, many more pixels are triggered due to the increase of photon flux as explained earlier. It is observed that the number of detected photon with optical power of 100 nW$cm^{-2}$ is higher compared to that with optical power of 26 nW$cm^{-2}$ and 42 nW$cm^{-2}$.

Figure 4.33 (d) shows the measured data valid bit during 50 s duration with input optical power of 130 nW$cm^{-2}$. It is noticed that if the power increases further to 130 nW$cm^{-2}$, many more pixels are triggered due to the increase of photon flux as explained earlier. It is observed that the number of detected photon with optical power of 130 nW$cm^{-2}$ is higher compared to that with optical power of 26 nW$cm^{-2}$, 42 nW$cm^{-2}$, and 100 nW$cm^{-2}$.

However, if the optical power is increased further beyond 130 nW$cm^{-2}$ to 230 nW$cm^{-2}$ and 480 nW$cm^{-2}$, the number of detected photon is decreased. It is observed that the number of measured output addresses is decreased (Figure 4.33 (c) and Figure 4.33 (d)). As a summary, the output addresses increases until input optical power of 130 nW$cm^{-2}$.




**(a)** 26 nW$cm^{-2}$ **(b)** 42 nW$cm^{-2}$

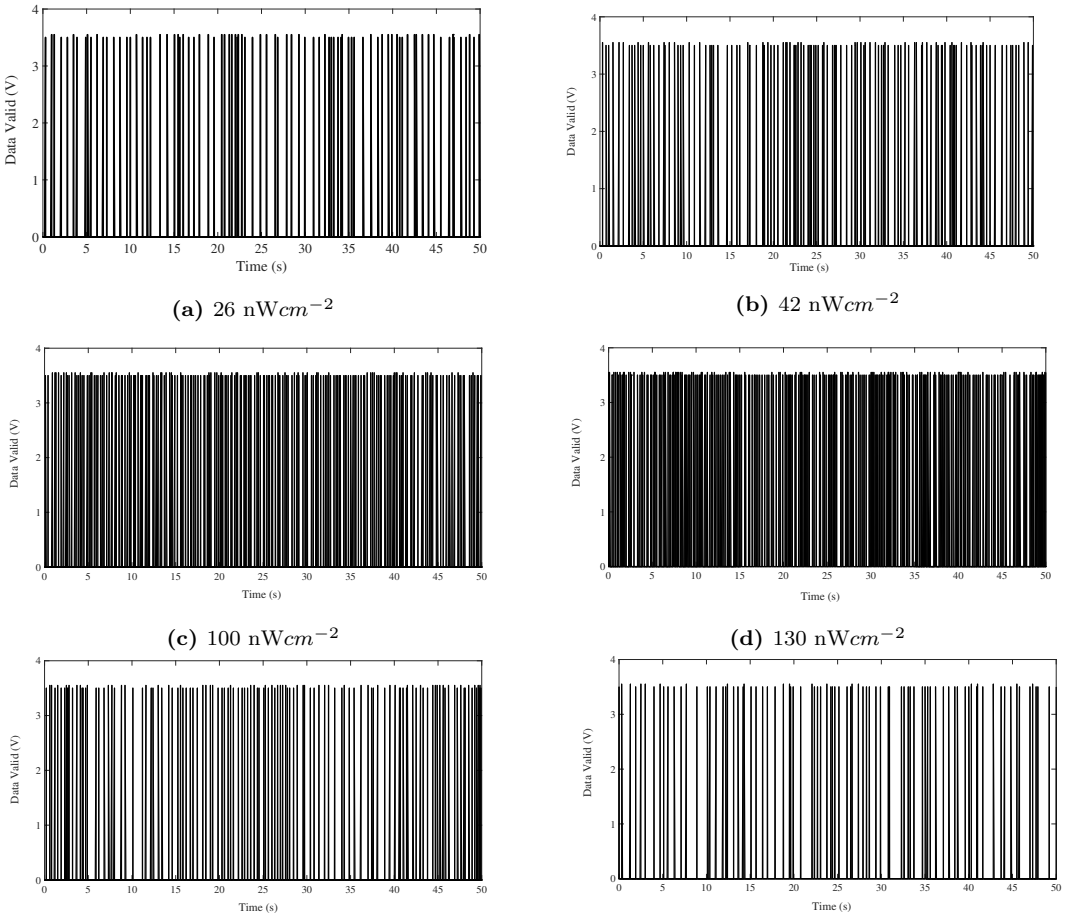
**(c)** 100 nW$cm^{-2}$ **(d)** 130 nW$cm^{-2}$

**(e)** 230 nW$cm^{-2}$ **(f)** 480 nW$cm^{-2}$

**Figure 4.33:** Chip1 measured data valid address readout representing total number of detected photon with different optical powers.

The measured data valid bit acquired from testing of chip2 consisting the 4 × 4 digital SiPM array with AER readout is shown in Figure 4.34. The data valid bit is measured for a wide range of input optical power from 26 nW$cm^{-2}$ to 450 nW$cm^{-2}$. The total number of triggered pixels through the measured data valid bit for a range of power from 26 nW$cm^{-2}$ to 450 nW$cm^{-2}$ obtained from the testing of chip2 consisting the 4 × 4 digital SiPM array with AER readout are summarized and compared in Figure 4.34. As the power increases from 26 nW$cm^{-2}$ to 42 nW$cm^{-2}$, more pixels are triggered due to the increase of photon flux. Therefore, more addresses of the triggered pixels are available at the address bus.(Figure 4.34 (a) and Figure 4.34 (b)).

The input optical power is increased further to 100 nW$cm^{-2}$ and the measured data valid bit during 50 s duration is shown in Figure 4.34 (c). It is noticed that if the power increases further to 100 nW$cm^{-2}$, many more pixels are triggered due to the increase of photon flux as explained earlier. It is observed that the number of detected photon with optical power of 100 nW$cm^{-2}$ is higher compared to that with optical power of 26 nW$cm^{-2}$ and 42 nW$cm^{-2}$. Figure 4.34 (d) shows the measured data valid bit during 50 s duration with input optical power of 130 nW$cm^{-2}$. It is noticed that if the power increases further to 130 nW$cm^{-2}$, many more pixels are triggered due to the increase of photon flux as explained earlier. It is observed that the number of detected photon with optical power of 130 nW$cm^{-2}$ is higher compared to that with optical power of 26 nW$cm^{-2}$, 42 nW$cm^{-2}$, and 100 nW$cm^{-2}$. However, if the power is increased further beyond 130 nW$cm^{-2}$ to 230 nW$cm^{-2}$ and 420 nW$cm^{-2}$, it is observed that the measured addresses decreases. It also confirms the same conclusion that the number of total count equivalent to the total output




**(a)** 26 nW$cm^{-2}$ **(b)** 42 nW$cm^{-2}$

**(c)** 100 nW$cm^{-2}$ **(d)** 130 nW$cm^{-2}$

**(e)** 230 nW$cm^{-2}$ **(f)** 480 nW$cm^{-2}$

**Figure 4.34:** Chip2 measured data valid address readout representing total number of detected photon with different optical powers.

data valid bits increases with the increase of input optical power and becomes saturated at around input optical power of 130 nW$cm^{-2}$.

Figure 4.35 summarizes the total count obtained from measured data valid output of two tested chips of the designed digital SiPM. It also confirms the same conclusion that the number of total count equivalent to the total output data valid bits increases with the increase of input optical power and becomes saturated at around input optical power of 130 nW$cm^{-2}$. Still with the upper input dynamic range limit of 130 nW$cm^{-2}$, the PGSPAD digital SiPM with AER protocol is suitable for a wide range of nuclear medical imaging applications including PET and SPECT applications with high bandwidth and added advantages of PGSPAD.

## 4.6 Performance Summary and Comparison

The developed SiPM is the first digital SiPM with asynchronous AER readout to provide high bandwidth and tunable noise performance using PGSPAD for a broad range of

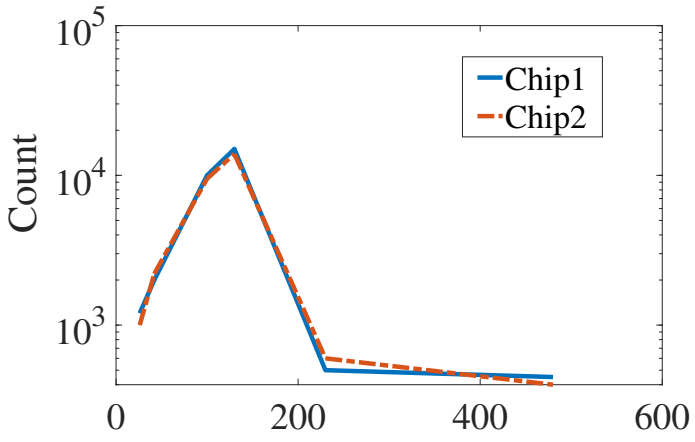



**Figure 4.35:** Count vs. Input optical power obtained from testing results of two chips .

applications including PET and SPECT. Moreover, the AER protocol is advantageous as it provides the spatial information through the address of the triggered pixel which is important to perform the position reconstruction required by the Anger camera in SPECT applications [26–29, 129]. The AER readout is also beneficial to pinpoint the scintillation point inside the crystal or crystal matrix in a large PET detectors [9, 20, 129] by locating the triggered pixels location through the output address.

However, there is a possibility to loss some temporal information due to the row and column sequential arbitration used in AER readout. For example, first pixel in the first row triggers and then another pixel in third row triggers and next last pixel in the first row triggers. Since at first, the first row will be selected due to the triggering of the first pixel in the first row, after transmitting the request of first pixel, the last pixel of the same row will be selected to send its address. As a result the photon triggered the pixel of the third row will be lost. The loss of photon degrades the performance specially at high input optical power with large number of simultaneously triggered pixels.

In order to prevent the loss of temporal information with this compact prototype design, the readout speed has been increased as much as possible without sacrificing power. The system was found to be able to read out addresses with a maximum speed of 80 MHz. The array level dynamic range is defined in [121].

$$DR = 20log_{10}\left(\frac{2^b.f_{max}}{DCR.N}\right) \tag{4.2}$$

where $b$ is the resolution of the pixel counter, $f_{max}$ is the maximum readout speed, DCR is the average dark count rate of the PGSPAD device, and N is the number of pixels in the array.

For the designed $4 \times 4$ pixel array with 8-bit in-pixel counter, an average DCR of 100Hz, and the maximum simulated readout speed of 80 MHz, the achieved array-level dynamic range is found to be 162 dB with AER readout area of 0.76% (dead area) of the total area. Minimization of the dead area at the chip level is an important requirement as an array of chips is used in a PET imaging array. The designed array provides a satisfactory dynamic range of around 102 dB even with a larger array size of $128 \times 128$ pixels with AER readout area of 0.03% (dead area) of the total area.

Table 4.1 summarizes the performance of the PGSPAD digital SiPM with fully digital asynchronous AER readout and compares with some other state of the art digital SiPMs [9, 10, 10, 20, 92, 130] reported in the literature. The proposed PGSPAD digital SiPM is the only CMOS digital SiPM which incorporates the asynchronous AER readout to provide high bandwidth with extra benefit of tunable noise performance due to the PGSPAD device. The PGSPAD SiPM provides lower noise compared to the reported SiPMs and a comparable photon detection efficiency (PDE). The pixel fill factor (FF) and PDE can be improved further by increasing the size of the optically sensitive area with increased overall area of the detector. However, the DCR noise also increases with the increase of the device size. Therefore, there is a tradeoff between the high FF and low DCR noise.

Finally, the figure of merit (FoM) based on [131] was computed for all the SiPMs using the following equation

$$FoM = PDE \times \frac{\sqrt{Area \times FF}}{\sqrt{DCR}} \tag{4.3}$$

where $PDE$ represents the photon detection efficiency, $FF$ is the fill factor, and $DCR$ is the dark count rate noise.

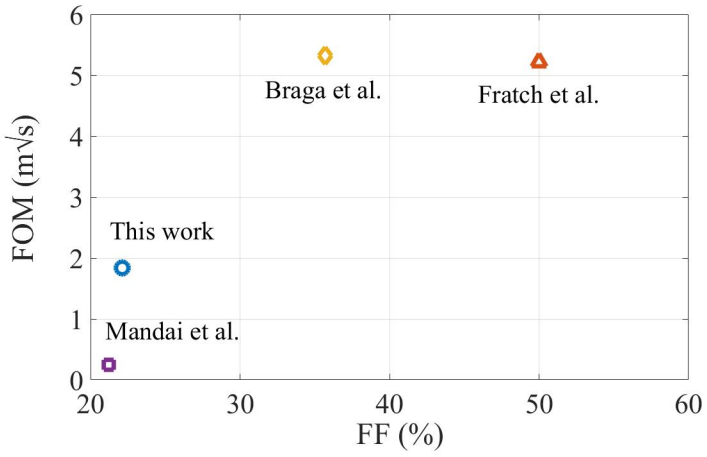
**Table 4.1:** Performance Summary and Comparison of designed digital SiPM with some other state of the art digital SiPMs

| Parameter | This work | [10, 11] | [20] | [9, 92] |
|---|---|---|---|---|
| Process | 0.5 $\mu m$ CMOS | High volume CMOS | 0.13 $\mu$m CMOS imaging | 0.35 $\mu$m HV CMOS |
| Tech. | Digital | Digital | Digital | Digital |
| Area ($mm^2$) | 1.2 ×1.15 | 3.9 ×3.2 | 9.85 ×5.45 | 1.8 ×0.78 |
| Fill Factor (%) | 22.1 | 50 | 35.7 | 21.2 |
| Readout | Asynchronous AER | Synchronous-sequential | Synchronous in-column | Synchronous in-column |
| Array-level dynamic range (dB) | 162 | Not Reported | Not Reported | Not Reported |
| DCR Noise (kHZ) | 1.1 | 2.2 | 13.7 | 30.7 |
| $PDE_{peak}$(%)@ wavelength | 35 [500 nm] | 31 [420 nm] | 45 [410 nm] | 24.8 [450 nm] |
| Tunable SNR | Yes | No | No | No |
| Maximum Speed (MHz) | 80 | Not Reported | 100 | 30.4 |
| FOM (m$\sqrt{}$s) | 1.84 | 5.22 | 5.32 | 0.244 |

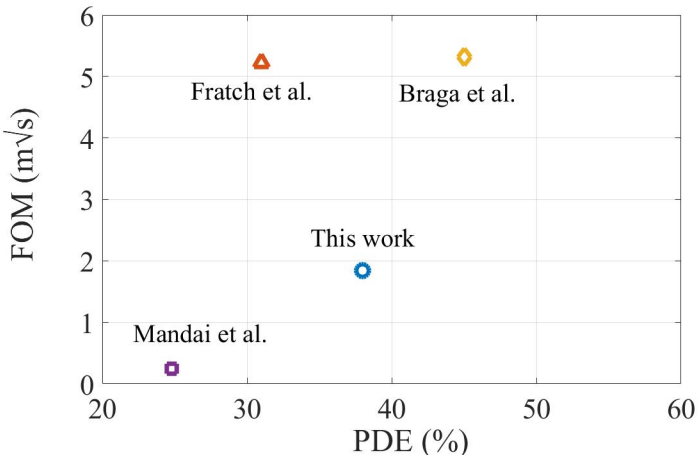
From the comparison, it is observed that the developed PGSPAD digital SiPM with AER provides a comparable FOM. Figure 4.36 shows the FOMs for all the SiPMs presented in Table 4.1. FOM of the designed SiPM can be improved further by increasing the FF as depicted in Figure 4.36 (a). The FF can be raised by increasing the optically sensitive area. Increasing the PDE also improves the FOM (Figure 4.36 (b)). In addition, low DCR benefits the FOM (Figure 4.36 (c)). As a summary, increasing the FF and PDE while decreasing the DCR improves the FOM.

## 4.7 Conclusion

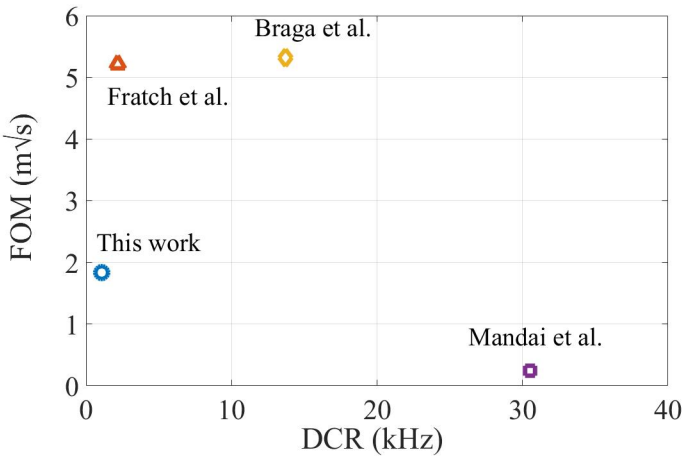
In this chapter, a PGSPAD based CMOS digital silicon photomultiplier has been presented suitable for a wide range of nuclear medical imaging applications including PET and SPECT. A fully digital asynchronous address event representation (AER) readout has been implemented for the designed digital SiPM to provide high bandwidth communication. This is the first ever CMOS digital SiPM with fully digital asynchronous AER readout. A factor of four improvement in the dead time by using 4 sub PGSPADs was achieved. A temporal compression factor of 10 has been achieved at the microcell level, and the designed analog counter provides a counting resolution of 8 bits with a programmable time resolution. The DCR characterization for the PGSPAD pixel of digital SiPM with variation of the applied gate voltage and excess bias voltage has been reported. The measured result showed that the noise performance of digital SiPM can be modulated using the applied gate voltage. An array-level dynamic range of 162 dB has been achieved. The PGSPAD digital SiPM has been characterized over a range of optical power from 26 nW$cm^{-2}$ to 450 nW$cm^{-2}$.




(a)




(b)




(c)

**Figure 4.36:** (a) FOM vs. FF, (b) FOM vs. PDE, (c) FOM vs. DCR.

The measured response showed the feasibility of the detector for a broad range of nuclear medical imaging applications including SPECT and PET applications. Since the AER protocol provides spatial information through the address of the triggered pixel, it would be helpful to perform the position reconstruction, the usual requirement of the Anger camera in SPECT applications, and pinpoint the scintillation point inside the crystal or crystal matrix in a large PET detectors. The proposed digital PGSPAD SiPM with AER readout can be expanded to a larger array with high bandwidth, high spatial resolution, improved fill factor, and an added advantage of tunable noise floor, sensitivity, and dynamic range due to PGSPAD.

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# Chapter 5

# Modeling of Silicon Photomultiplier based on Perimeter Gated SPAD

** **Portions of this chapter were published in:**

1. Mst Shamim Ara Shawkat, Md Sakib Hasan, and Nicole McFarlane, *"Modeling of Silicon Photomultiplier based on Perimeter Gated SPAD,"* IEEE International Midwest Symposium on Circuits and Systems, Dallas, pp. 1110–1113, Aug. 2019.

## 5.1 Introduction

Silicon photomultipliers (SiPMs) have been widely used as photo-sensing device to take over photomultiplier tubes (PMTs) in a broad range of uses. These includes nuclear medical imaging, cosmology, and high energy physics [9,20,32,44,109,111,113,114,132–138]. SiPMs consist of a large array of parallel single avalanche photo diodes (SPADs) with a series resistor and biased beyond reverse breakdown. The current of all the avalanched SPADs are summed to generate the total output current in an analog SiPM. The resulting current is proportional to the number of detected photons representing the number triggered microcells.

A complete comprehension of the working physics and the effect of front-side electronics is required to understand the SiPM signal completely. A comprehensive model to explain both the static and dynamic functioning is of vital importance. Simulation is useful to

study the static and dynamic behaviors of the design. In order to study those behaviors, models for single ordinary SPADs and SiPMs using ordinary SPADs have been presented in [54,139] and [134–138] respectively. An improved version SPAD with an extra polysilicon gate known as perimeter gated SPAD (PGSPAD) modulates electric field and prevents the perimeter edge breakdown [41, 44]. In order to study the impact of extra gate on the behavior of discrete PGSPAD device, models have been presented in [42,79]. Although the SiPM models using standard SPAD [134–138] accurately captures the behavior of SiPM, it is incapable to investigate the impact of the additional gate on those behavior of SiPM based on PGSPAD. Thus, a correct and comprehensive SiPM model using PGSPAD is necessary to study the device physics for the SiPM using PGSPAD including the impact of the additional gate terminal.

In this chapter, a comprehensive SiPM model based on perimeter gated SPADs (PGSPADs) has been presented to provide a useful simulation tool for SiPM detector with the impact of additional gate terminal of PGSPAD device for the first time. In addition, the model includes the underlying physical process to simulate the stochastic dark current noise behavior of SiPM behavior with the impact of gate terminal which has not yet been captured by prior reported SiPM models [134–138]. The proposed PGSPAD SiPM model emanates from the PGSPAD behavioral model reported earlier in [44]. Here, the PGSPAD model has been upgraded to be appropriate for the microcell of the SiPMs with many more parasitic elements and couplings. The model also includes the substrate effect to provide a more accurate simulation with additional parasitics. Furthermore, the model simulates the effect of different parameters of the PGSPAD based microcell, the statistical and deterministic mismatches among the PGSPAD microcells, the impact of the

number of triggered microcells out of the total number of microcells with the additional gate terminal. The model also verifies the tunability of dark current noise of PGSPAD SiPM with the applied gate voltage. Finally, the simulation results have been compared with the experimental measurements of PGSPAD SiPM fabricated in 0.5 $\mu$m CMOS process to validate the developed new PGSPAD SiPM model. The model was reported in [140] as first PGSPAD SiPM model considering the effect of additional gate terminal.

## 5.2 PGSPAD based Microcell Model

Figure 5.1 shows the schematic of a PGSPAD SiPM where each microcell incorporating the PGSPAD biased above breakdown voltage and a series quenching resistor are combined in parallel. Each microcell can go through avalanche independently. Since all microcells share the same anode and cathode, all single triggered PGSPAD's current are summed to generate an output current proportional to the total number of triggered microcells. In this section, we develop the equivalent circuit model of PGSPAD based microcell considering the impact of gate voltage which is based on the PGSPAD model reported in [44]. The model includes the parasitic components and coupling to make it suitable for SiPMs. Finally, in order to make a more complete PGSPAD SiPM model, the basic PGSPAD based microcell model has been extended and the noise behavior has been incorporated with the effect of gate voltage.

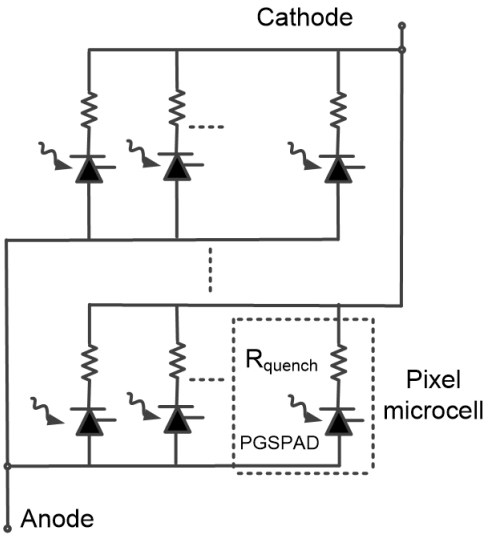



**Figure 5.1:** Schematic of the PGSPAD SiPM as a parallel connection of PGSPAD based microcell.

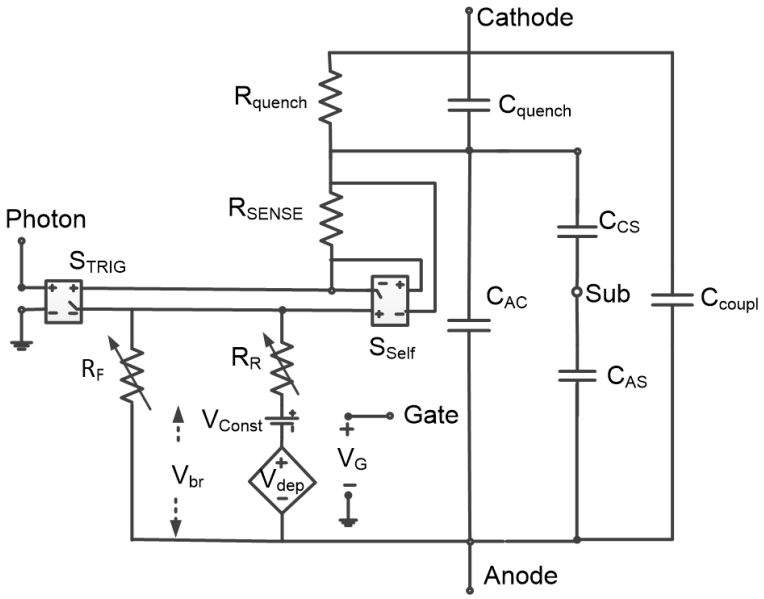



**Figure 5.2:** Schematic of the proposed PGSPAD SiPM microcell which includes the dependency of breakdown voltage on the gate voltage of PGSPAD, quenching resistance, parasitic and coupling capacitance ( [140] ©2019 IEEE).

### 5.2.1 Equivalent Circuit Model of PGSPAD based Microcell

The schematic of the proposed equivalent circuit model for PGSPAD microcell is shown in Figure 5.2 which is based on the comprehensive PGSPAD model [44]. The PGSPAD

model includes the dependence of the breakdown voltage on the gate voltage and the changeable reverse bias resistance with gate voltage which are specific to the PGSPAD device. The model incorporates two parallel branches to simulate both the forward-bias and reverse-bias operation. Model parameters are extracted from the measurement of fabricated PGSPAD device in 0.5 $\mu$m CMOS process. Since the reverse breakdown voltage is changed by the applied gate voltage, a dependent voltage source, $V_{dep}$, is included in the reverse-bias branch to represent the modulation of the breakdown voltage by the applied gate voltage. The PGSPAD is modeled as a parallel combination between the built-in resistance of the reverse biased junction, $R_R$, with the breakdown voltage consisting of a constant voltage source, $V_{Const}$, and a dependent voltage source, $V_{dep}$, representing the dependency of the breakdown voltage on the gate voltage, and the capacitance. The capacitance includes the junction capacitance, $C_{AC}$, and stray capacitance, $C_{AS}$ and $C_{CS}$. The microcell includes the quenching resistance, $R_{quench}$, and the parallel stray, $C_{quench}$. A coupling capacitance, $C_{coupl}$, is also incorporated to include the parasitic capacitance for the metal link of the parallel microcells.

In order to emulate the photon arrival, *Photon* pin is incorporated using a pulsed voltage source which triggers the avalanche through a voltage controlled switch, $S_{TRIG}$. Another voltage controlled switch, $S_{Self}$, with sensing resistor, $R_{SENSE}$, is used to emulate the current sustaining and self-quenching behavior of the avalanche process. The dependency of the breakdown voltage, $V_{br}$, on the applied gate voltage, $V_G$, based on the experimental measurement is defined as

$$V_{br} = \alpha V_G + V_{Const} \tag{5.1}$$

where $\alpha$ is a constant which is determined experimentally.

The value of the reverse branch resistance, $R_R$, varies exponentially with the applied bias voltage and the gate voltage, while the forward branch resistance, $R_F$, used in the PGSPAD model is a function of the applied bias voltage defined as, [42]

$$R_R = Xe^{Y(V_{CA}-V_{const}+\alpha V_G)} \tag{5.2}$$

and

$$R_F = Le^{-MV_{AC}} \tag{5.3}$$

where, X, Y, L, and M are constants estimated experimentally.

### 5.2.2 Noise Model of PGSPAD based Microcell

The comprehensive PGSPAD SiPM microcell model improves the equivalent microcell model of PGSPAD SiPM presented in the previous section and added the stochastic noise behavior to predict a more accurate behavior of SiPM signals with effect of gate voltage. Figure 5.3 presents the complete PGSPAD SiPM microcell model inclusive of the noise behavior as well as the static and Geiger mode response of SiPM detectors.

The noise model is developed on the basis of the basic theories of thermal generation, inter-band tunneling, and minority carrier diffusion. The current observed at the output of the SiPM due to these non-photon free carrier's generation phenomena is known as dark current noise. Since the diffusion current generated due to minority carrier diffusion is usually around 3 orders of magnitude lower than those by other processes, we ignored the minority carrier diffusion dark current in the SiPM noise model.

In order to include the sources of dark current noise, thermal generation, band-to-band tunneling, the noise model includes the behavioral resistances ($R_{thermal}$, $R_{btbt}$, and $R_{DCR}$) and current sources ($I_{thermal}$, $I_{btbt}$). Based on the Shockley-Read-Hall equation [58], the total generation rate due to the thermally generated carriers ($G$) is defined as

$$G \approx \frac{n_i v_t \sigma_i N_{gr}}{2} \tag{5.4}$$

where $n_i$ represents the intrinsic carrier concentration, the thermal velocity is represented by $v_t$, $\sigma_i$ is the cross section area, and $N_{gr}$ represents the density of generation-recombination centers. The lifetime for the holes and electrons are assumed to be same. The carrier generation rate due to thermal generation is defined using the total generation rate ($G$) and is given as

$$CGR_{th} = G \times A_{act} \times W_{dep} \tag{5.5}$$

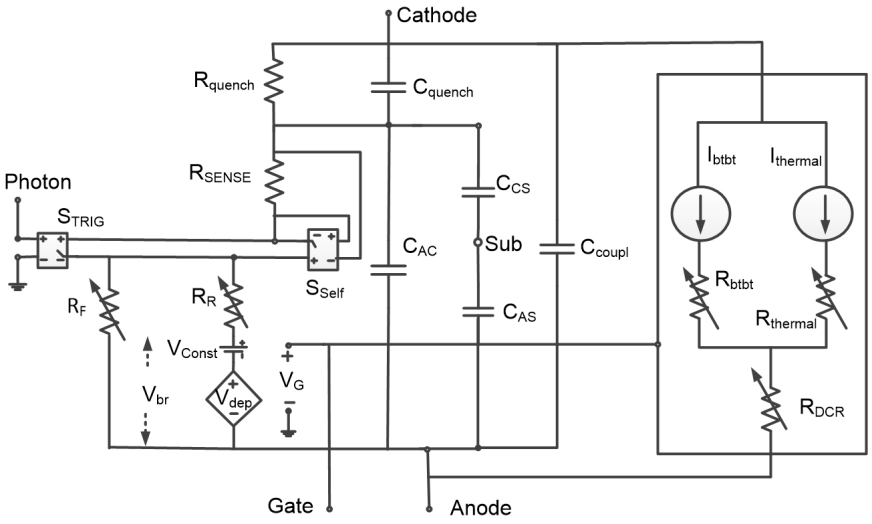



**Figure 5.3:** Schematic of the comprehensive PGSPAD SiPM microcell model to study the stochastic noise behavior along with the static and Geiger mode behavior of SiPM detectors with the effect of gate voltage.

where $A_{act}$ is the active area of the device and $W_{dep}$ represents the thickness of the depletion region. Each generated free carrier has a non-zero and finite probability of triggering an avalanche. The triggering probability, $P_{tr}$, increases with the excess bias voltage ($V_{Exc}$), the difference between the applied voltage and the breakdown voltage. The relation between the $P_{tr}$ and $V_{Exc}$ is given in [59–61]

$$P_{tr} = \begin{cases} 0 & \text{for } V_{Exc} < 0 \\ 1 - e^{-\frac{V_{Exc}}{\eta_T V_{Br}}} & \text{for } V_{Exc} \geq 0 \end{cases} \tag{5.6}$$

where $\eta_T$ is an experimentally derived parameter.

The dark count rate, the number of avalanche per unit time due to the thermally generated carrier is known as thermal dark count rate, $DCR_{th}$, (represented by $R_{thermal}$ in Figure 5.3) is given by

$$DCR_{th} = P_{tr} \times CGR_{th} \tag{5.7}$$

The carrier generation rate due to band-to-band tunneling is defined in [**?**] as

$$CGR_{tunn} = \frac{\sqrt{2m_t^*}e^2 F_{avg} V_{Rev}}{h^2\sqrt{E_{gap}}} \exp\left( - \frac{8\pi\sqrt{2m_t^*}E_{gap}^{3/2}}{3eF_{avg}h}\right) A_{act} \tag{5.8}$$

where $m_t^*$ represents the tunneling effective mass, e is the electron charge, $V_{Rev}$ is the reverse bias voltage, $h$ is Plank's constant, $F_{avg}$ is the average electric field in the depletion region, and $E_{gap}$ is the silicon bandgap energy.

It has been verified earlier that the gate voltage applied at the extra gate terminal helps to control the breakdown voltage and average electric field [44]. Detailed simulations have

also shown that the gate primarily affects the noise due to the band to band tunneling through the average electric field, $F_{avg}$.

The band-to-band tunneling generated carriers cause avalanche resulting in tunneling dark count rate $DCR_{tunn}$ (represented by $R_{btbt}$ in Figure 5.3) and is given in [59]

$$DCR_{tunn} = P_{tr} \times CGR_{tunn} \tag{5.9}$$

The total dark count rate, $DCR_{total}$, is the sum of dark count rate due to thermal generation and tunneling is defined as (represented by $R_{DCR}$ in Figure 5.3)

$$DCR_{total} = DCR_{th} + DCR_{tunn} \tag{5.10}$$

In PGSPAD device, the gate voltage affects the probability of triggering an avalanche by the free carrier generated due to these noise mechanisms (thermal generation and band-to-band tunneling) through the breakdown voltage. Furthermore, the $DCR_{tunn}$ is also influenced by the gate voltage through the average electric field, $F_{avg}$. Therefore, the applied gate voltage has an impact on the dark current of the SiPM through the dark count rate of the PGSPAD based microcell, $DCR_{total}$.

## 5.3 PGSPAD SiPM Electrical Model

In order to model the entire SiPM using the developed PGSPAD based microcell in previous section, the two macrocells approach has been adopted where one macrocell includes all the triggered microcells while the other macrocell incorporates all the non-triggered (passive)

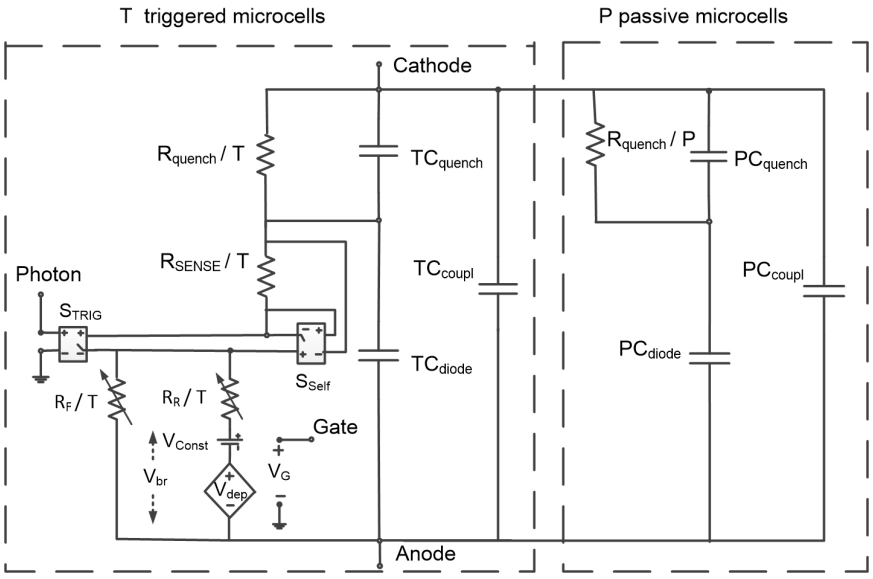



**Figure 5.4:** Schematic of the overall PGSPAD SiPM with $T$ triggered microcells and $P$ passive microcells out of total $N$ microcells ( [140] ©2019 IEEE).

microcells. Since the instantaneous electrical properties of the SiPM detectors are function of the number of triggered microcells, the designed PGSPAD SiPM model can adequately capture the behavior of SiPM detector with the impact of gate voltage. Figure 5.4 shows the schematic of the overall PGSPAD SiPM. Here, $N$ represents the total number of microcells, which includes the triggered microcells ($T$) and passive microcells ($(N - T)$). Since the microcells are connected in parallel, the j-th equivalent resistances and capacitances within the triggered macrocell are

$$R_{j,T} = R_j/T, C_{j,T} = C_j \times T \tag{5.11}$$

In a similar way, the k-th equivalent resistances and capacitances within the passive macrocell are

$$R_{k,T} = R_k/P, C_{k,T} = C_k \times P \tag{5.12}$$

In order to simulate the photon arrival, the *Photon* pin of the triggered macrocell is enabled by applying a pulsed voltage source whereas the photon pin of the passive macrocell is disabled. As a result, the $S_{TRIG}$ switch in triggered macrocell becomes closed providing a path for the avalanche current. With the increase of the avalanche current, the voltage across $R_{SENSE}$ increases and turns on the $S_{self}$ switch. This provides an alternative path for the avalanche current even though the *Photon* pin is disabled at this point capturing the current sustaining technique. Since, the voltage across the $R_{quench}$ is increased with the rise of the avalanche current, it reduces the voltage across the $R_{SENSE}$ turning off the $S_{self}$ and thus self-quenching the avalanche.

The equivalent capacitance, $C_{eqv}$, which includes the capacitance of all passive microcells $(N - T)$ and coupling capacitance, $C_{coupl}$, of all $N$ microcells is defined by

$$C_{eqv} = P \cdot \frac{C_{quench} \cdot C_{diode}}{C_{quench} + C_{diode}} + N \cdot C_{coupl} \tag{5.13}$$

where $C_{diode}$ represents the total capacitance of PGSPAD consisting of junction capacitance, $C_{AC}$, and stray capacitance, $C_{AS}$ and $C_{CS}$.

$C_{eqv}$ can be represented as a function of number triggered microcells $(T)$ and is given by

$$C_{eqv} = (N - T) \cdot \frac{C_{quench} \cdot C_{diode}}{C_{quench} + C_{diode}} + N \cdot C_{coupl} \tag{5.14}$$

## 5.4 Detailed Simulations

The model has been developed using Verilog-A. Simulations have been performed on the discrete microcell based on PGSPAD and the whole SiPM based on PGSPAD. Model

parameters are excerpted from the testing of PGSPADs in 0.5 $\mu$m CMOS process. A quenching resistor ($R_{quench}$) of 100 k$\Omega$, the capacitor associated with quenching resistor ($C_{quench}$) of 1 fF, and coupling capacitor ($C_{coupl}$) of 6 fF for each microcell are used.

### 5.4.1 SiPM Response with Varying $T$ and $V_G$

We have studied the effect of number of triggered microcells ($T$) on the transient behavior of the SiPM based on PGSPAD for two different gate voltages, $|V_G|$. $T$ is varied from 1 to 4 for $N$ of 324. Figure 5.5 shows the simulation result of the output current's transient behavior for the SiPM based on PGSPAD with four different values of $T$ values at $|V_G|$ of 2 V. The peak amplitude of output current raises linearly with the number of $T$ as expected with regular SiPM.

Figure 5.6 presents the simulation rasult of the transient behavior for the PGSPAD SiPM output current at $|V_G|$ of 4 V with four different values of $T$. it is also observed that

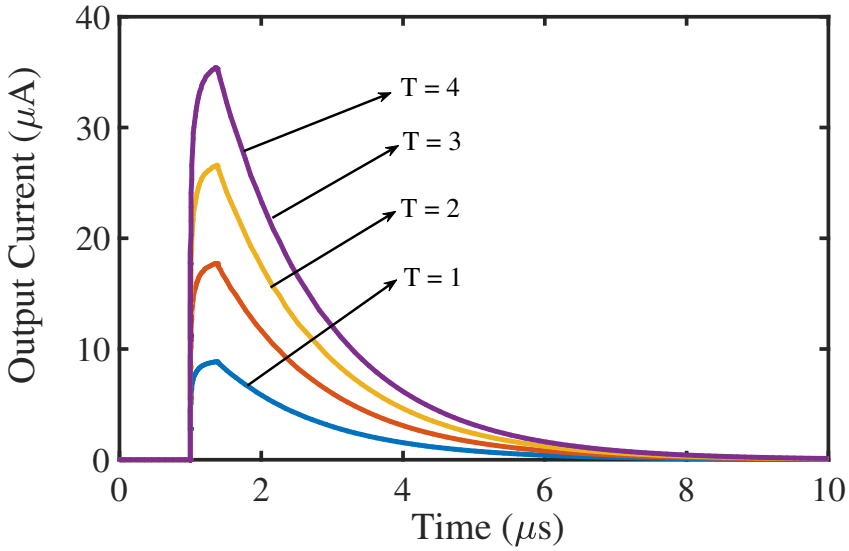



**Figure 5.5:** Simulated transient response of output current of PGSPAD SiPM with varying number of triggered microcell, $T$, from 1 to 4 for total number of microcells of 324 and applied gate voltage, $|V_G|$, of 2 V ( [140] ©2019 IEEE).

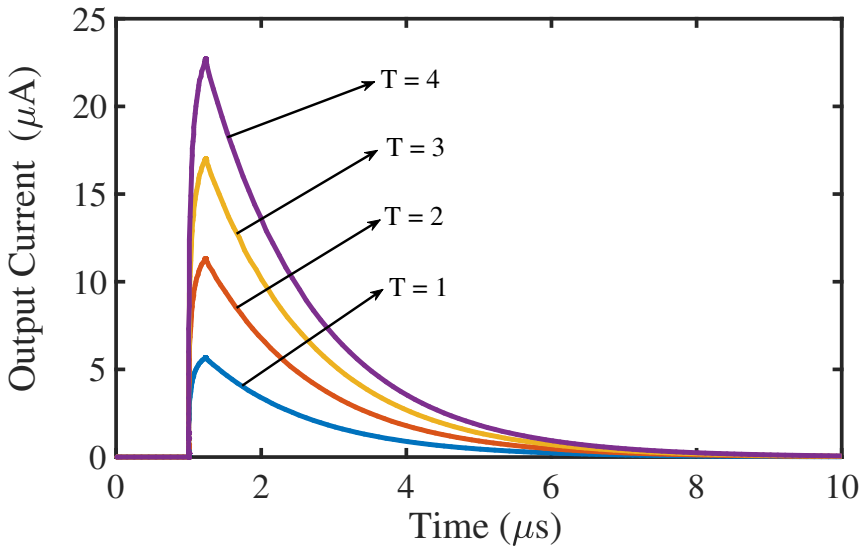



**Figure 5.6:** Simulated transient response of output current of PGSPAD SiPM with varying number of triggered microcell, $T$, from 1 to 4 for total number of microcells of 324 and applied gate voltage, $|V_G|$, of 4 V ( [140] ©2019 IEEE).

the maximum output current raises linearly with the rise of $T$. However, the value of the maximum output current with $|V_G|$ of 4 V is less compared to that with $|V_G|$ of 2 V (Figure 5.5). This is because with the increase of $|V_G|$ breakdown voltage increases and the excess bias voltage decreases. Therefore, the maximum value of the output current lowers as the excess bias voltage reduces. Thus, the model accurately predicts the SiPM behavior with the effect of gate terminal.

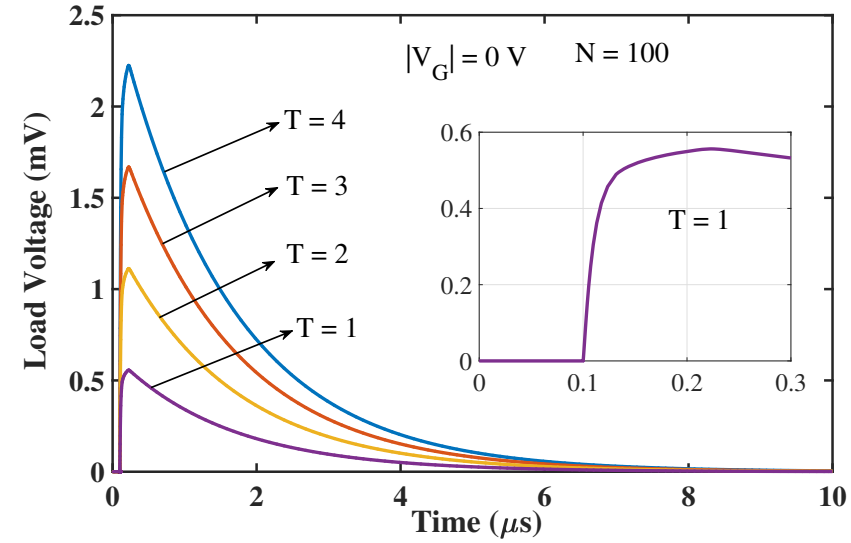
### 5.4.2 SiPM Response with Variation of $N$ and $T$

The transient response of PGSPAD based SiPM has been simulated with variation of number of total microcells, $N$, and number of simultaneous triggered microcells, $T$. The avalanche current of the PGSPAD SiPM has been readout through the voltage across the load resistor of 50 Ω connected in series with the SiPM. The transient response of the avalanche current of the PGSPAD SiPM is recorded through the voltage across the load

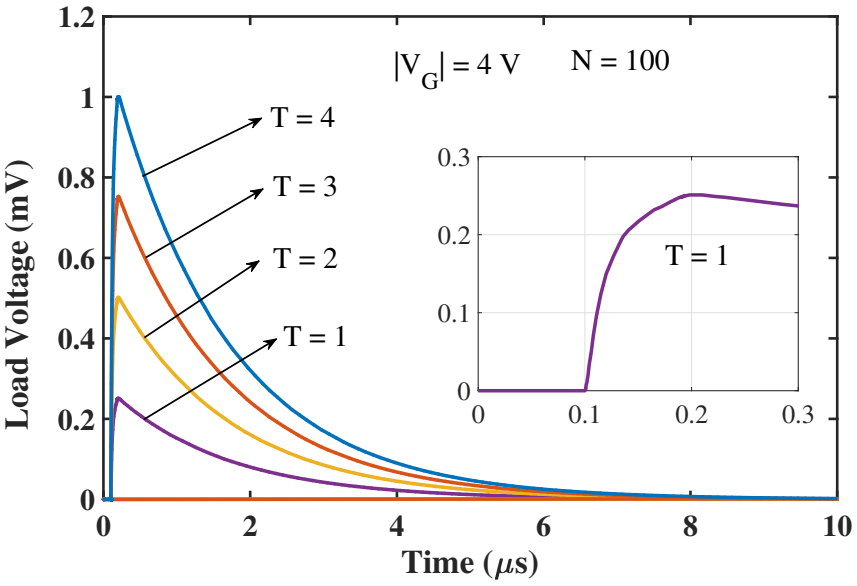
resistor of 50 Ω connected in series with the SiPM for two different SiPMs with $N$ of 100 and 1000 respectively.

The transient response of the SiPM with total microcells, $N$ of 100 has been simulated. For this simulation, $T$ is varied from 1 to 4 and two different applied gate voltages, $|V_G|$ of 0 V and 4 V is considered. Figure 5.7 shows the transient response of the SiPM with $N$ of 100, variation of $T$ from 1 to 4 and two different applied gate voltages. It is observed that the peak voltage amplitude increases linearly with the increase of T for both cases (Figure 5.7 (a) and (b)). However, if the gate voltage raises, the peak amplitude decreases. This is because with the increase of gate voltage, breakdown voltage increases. The excess bias voltage, the difference between the applied bias voltage and breakdown voltage, reduces with the increase of breakdown voltage. As a result, the peak amplitude of the output current reduces and the recorded output voltage across the load resistance decreases. Therefore, the peak voltage amplitude with $|V_G|$ of 4 V shown in Figure 5.7 (a) is lower than that with $|V_G|$ of 0 V presneted in Figure 5.7 (b). Since the number of total microcells is relatively small, the rise time is relatively faster. The inset in the Figure 5.7 shows the zoom-in version of the 1-photon displaying the fast rise time.

The effect of total number of microcells on the transient response of the PGSPAD SiPM has been studied. The number of total microcells, $N$, has been increased to 1000 and corresponding transient response has been simulated. For this simulation, $T$ is varied from 1 to 4 and two different applied gate voltage, $|V_G|$ of 0 V and 4 V is considered. The transient response of the SiPM with $N$ of 1000, variation of $T$ from 1 to 4 and two different applied gate voltages is presented in Figure 5.8. It is observed that the peak voltage amplitude increases linearly with the increase of T for both cases (Figure 5.8 (a) and (b)). However,




(a)



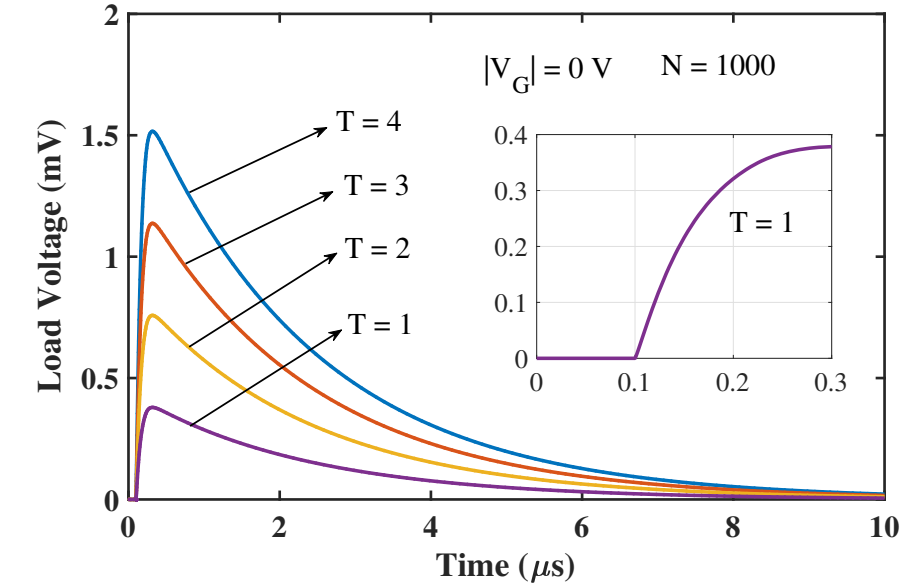

(b)

**Figure 5.7:** Simulated transient response for total microcells, $N$, of 100 with varying the simultaneously triggered microcells, $T$, from 1 to 4 when (a) applied gate voltage, $|V_G|$ is 0 V, (b) applied gate voltage, $|V_G|$ is 4 V. The zoom-in version of the 1-photon is shown in the insets.

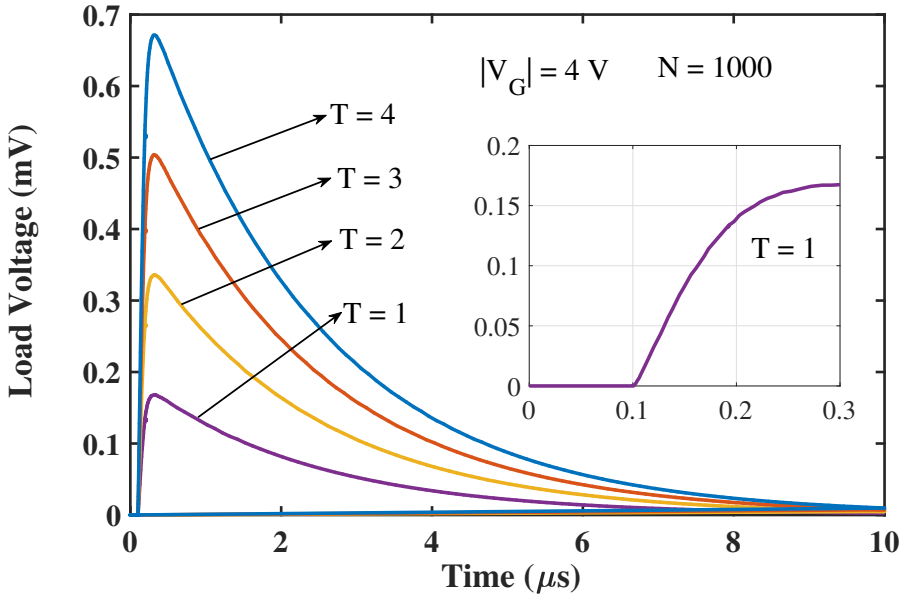
if the gate voltage increases, the peak amplitude reduces. This is due to the fact that with the increase of gate voltage, breakdown voltage increases. The excess bias voltage, the difference between the applied bias voltage and breakdown voltage, decreases with the increase of breakdown voltage. Therefore, the peak amplitude of the output current reduces and the recorded output voltage across the load resistance decreases. As a result, the peak voltage amplitude with $|V_G|$ of 4 V shown in Figure 5.8 (a) is lower than that with $|V_G|$ of 0 V reported in Figure 5.7 (b). Therefore, the increase in the peak voltage amplitude with the simultaneous triggered cells T (Figure 5.8) shows a similar trend for both applied voltages as those with 100 microcells (Figure 5.7).

However, overall the peak voltage amplitude with N of 1000 microcells presented in Figure 5.8 is lower than that with N of 100 microcells shown in Figure 5.7). This is because with the increase of microcells, the more parasitic effects including a large grid capacitance will be added resulting in the reduction of the peak amplitude. Since the number of total microcells is relatively high, the rise time is relatively slow. Therefore, it is noticed that the rising edge is more slower with large microcells of 1000 whereas the rising edge with small microcell of 100 is faster displaying in the inset of Figure 5.7 and Figure 5.8 respectively through the zoom-in version for $T$ of 1.

The effect of parasitic on the transient response of SiPM has been investigated also. In order to verify the parasitic effects on the SiPM performance, the transient response has been simulated for different SiPMs with different number of microcells from small to large with the effect of additional gate terminal. For this set of simulations, a constant number of simultaneous triggering microcells of 10 and 100 is studied. The transient response of the five different PGSPAD SiPMs each with different N of 100, 200, 400, 800, and 1600 for




(a)

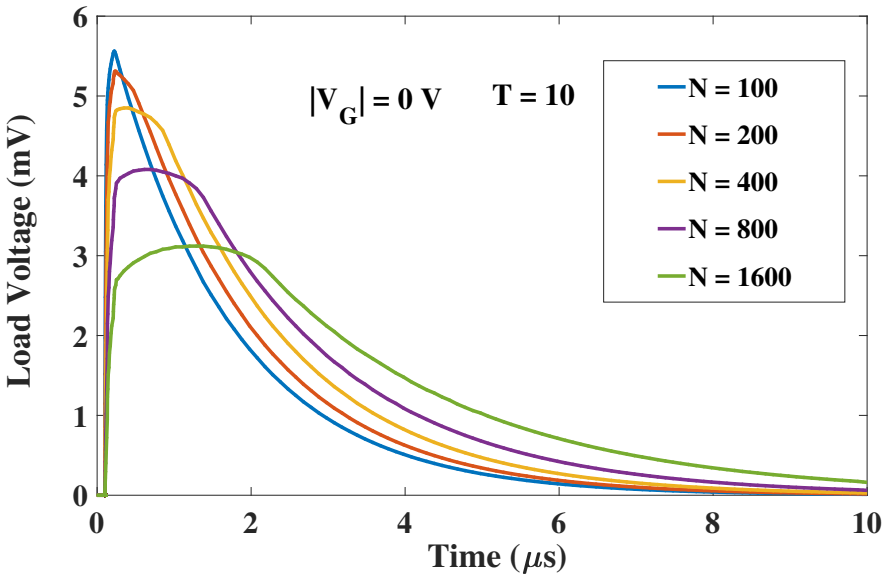



(b)

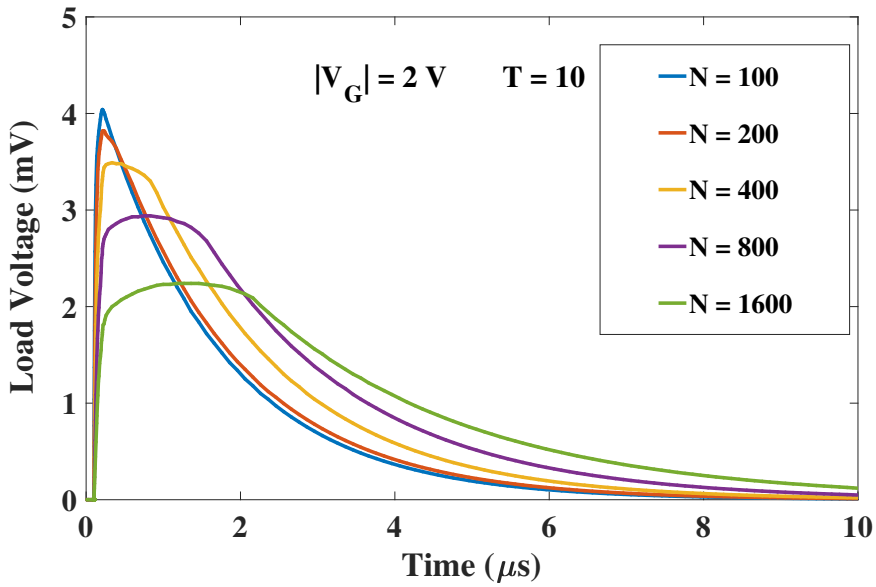
**Figure 5.8:** Simulated transient response for total microcells, $N$, of 1000 with varying the simultaneously triggered microcells, $T$, from 1 to 4 when (a) applied gate voltage, $|V_G|$ is 0 V, (b) applied gate voltage, $|V_G|$ is 4 V. The zoom-in version of the 1-photon is shown in the insets.

T of 10 and two different gate voltages, $V_G$, 0 V and 2 V is simulated at first. Figure 5.9 shows the transient response of SiPM for this simulation. The peak voltage amplitude of the larger SiPM ($N$ of 1600 ) is the lowest among all the SiPMs due to the large parasitic associated with the large number of microcells in large SiPM. Moreover, because of this effect, the rising and falling edge is becoming slower as the number of microcells increases. These results confirm the findings observed in Figure 5.8 that larger SiPMs need more time to reach the peak. Therefore, the rising edge is slower for larger SiPM compared with that of the other smaller SiPM shown in the figure. For all SiPMs, as the gate voltage increases the the excess bias voltage decreases due the increase of gate voltage. As a result, the peak output current reduces and peak voltage amplitude decreases.

The impact of large number of simultaneous microcells is studied. Here, number of simultaneous triggered microcells is increased to 100. For large simultaneous trigger microcells of 100, simulation has been preformed also for five different SiPMs including small and large SiPM with N of 100, 200, 400, 800, and 1600. Two different $V_G$, 0 V and 2 V have been considered for this simulation. The transient response of PGSPAD SiPM for large value of $T$ of 100 is shown in Figure 5.10. It is observed that the peak voltage amplitude of the larger SiPM ($N$ of 1600 ) is the lowest among all the SiPMs due to the large parasitic associated with the large number of microcells in large SiPM. Therefore, the results also confirms the same finding observed earlier that the larger SiPM with $N$ of 1600 microcells has the lowest peak due the increased parasitic effect associated with the larger SiPM. Moreover, for larger SiPM, the peak are delayed due to the same effect. However, the peak voltage amplitude is higher with large T of 100 for all the SiPMs (Figure 5.10) compared to what is found with T of 10 (Figure 5.9). The peak voltage also reduces with the




(a)




(b)

**Figure 5.9:** Simulated transient response for varying the total microcells, $N$, to 100, 200, 400, 800, and 1600 with simultaneously triggered microcells, $T$, of 10 when (a) applied gate voltage, $|V_G|$ is 0 V, (b) applied gate voltage, $|V_G|$ is 2 V.

raise of gate voltage as expected. This result also confirms the similar finding observed in previous transient responses (Figure 5.7 and 5.8). Therefore, the model accurately captures the transient behavior of the SiPM signal with the impact of extra gate terminal.

### 5.4.3 Photoelectron Spectrum

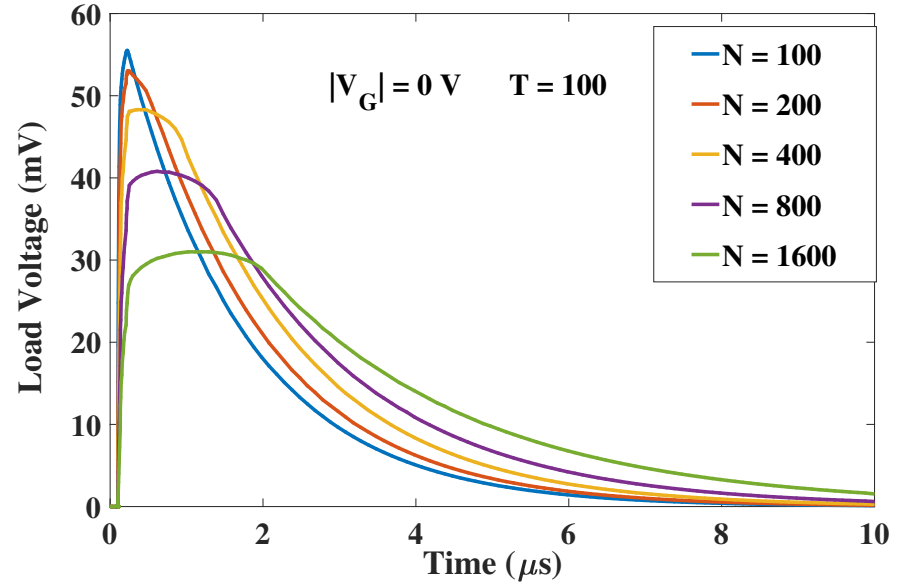
Since the photoelectron spectrum explains the ability to find the solution for a number of concurrent photons striking the detector, study of photelectron spectrum is necessary to characterize the SiPM performance. Poisson distribution can used to define the probability to detect T (triggering ) photons as

$$P_T = e^{-\bar{T}} \frac{\bar{T}^T}{T!} \tag{5.15}$$

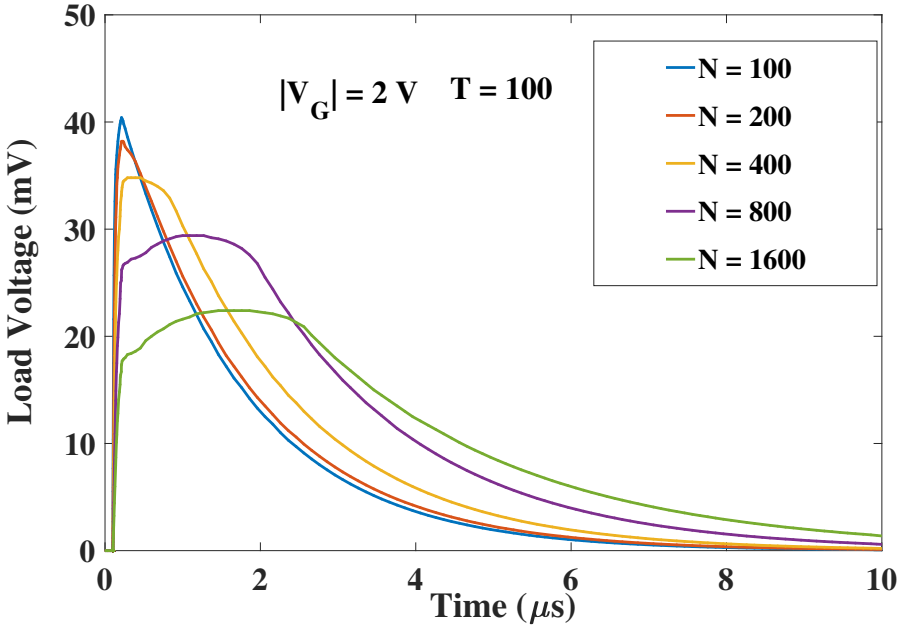
where $\bar{T}$ represents the mean value of the distribution.

At first, the expected number of count has been estimated through the probability distribution function using Matlab for $\bar{T} = 5$ varying $T$ from 1 to 15. Figure 5.11 (a) shows the expected count for $\bar{T} = 5$. The corresponding recorded load voltage for maen value of 5 is around 1 mV. It is observed that the number of count (number of occurrence) is same for the simultaneously triggered photon of 5 and 4 as expected from the eqn. 5.15. Since the expected count for $\bar{T} = 5$ for this simulation, the probability of triggering less and more than 5 simultaneously triggering microclells is low and therefore, the count is lower. Moreover, the load voltage increases with the number of triggered microcells.

The expected number of count has been estimated through the probability distribution function using Matlab for $\bar{T} = 15$ varying $T$ from 1 to 30. Figure 5.11 (b) shows the expected count for $\bar{T} = 15$. The corresponding recorded load voltage for maen value of 5 is




(a)




(b)

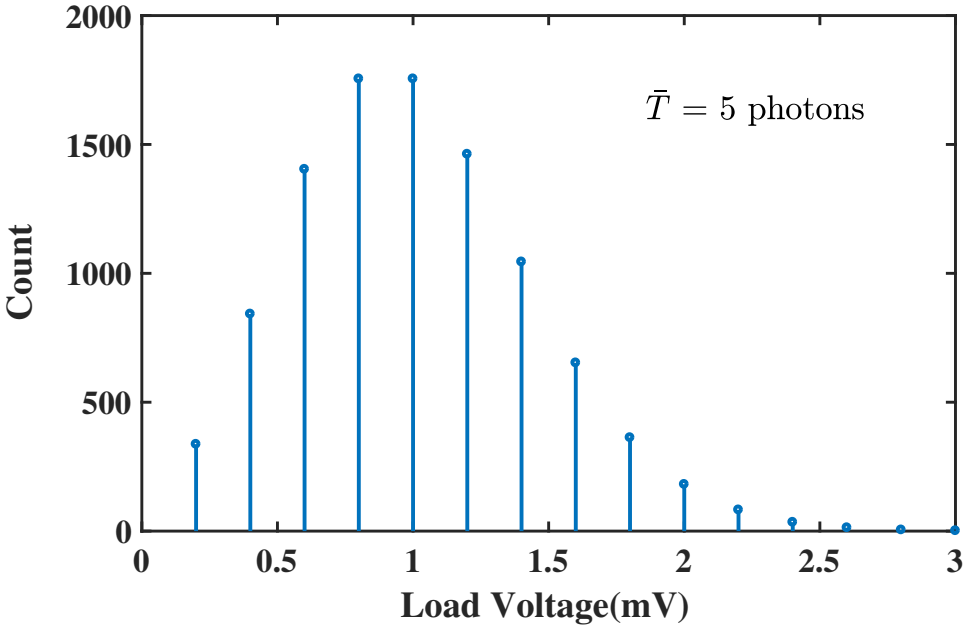
**Figure 5.10:** Simulated transient response for varying the total microcells, $N$, to 100, 200, 400, 800, and 1600 with simultaneously triggered microcells, $T$, of 100 when (a) applied gate voltage, $|V_G|$ is 0 V, (b) applied gate voltage, $|V_G|$ is 2 V.

around 1 mV. It is observed that the number of count (number of occurrence) is same for the simultaneously triggered photon of 15 and 14 as expected from the eqn. 5.15. Since the expected count for $\bar{T} = 15$ for this simulation, the probability of triggering less and more than 15 simultaneously triggering microclells is low and therefore, the count is lower. The load voltage also increases with the number of triggered microcells.

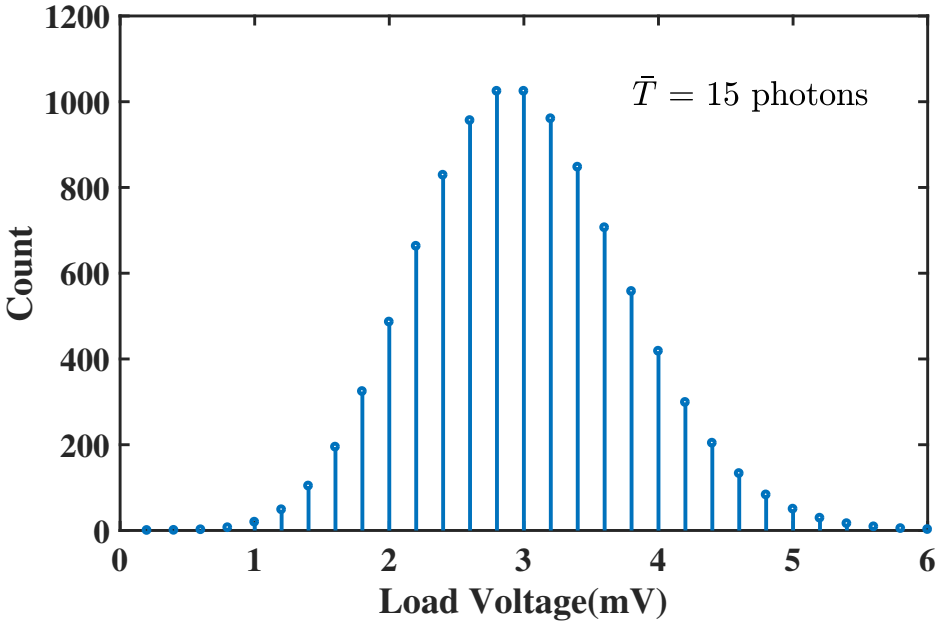
Two different distribution have been simulated with a total of number of event $10^4$, one for mean value ($\bar{T}$) of 5 while the other one with mean value of ($\bar{T}$) of 15. Monte Carlo simulations have been performed in cadence for an $8 \times 8$ array with 5% tolerance on the quenching resistor, $R_{quench}$, and 0.1 % tolerance on the breakdown voltage, $V_{br}$, including the impact of extra gate terminal.

Figure 5.12 (a) shows the avalanche amplitude distribution with $\bar{T} = 5$ for the applied gate voltage ( $|V_G|$) of 0 V. As the triggered microcells ($T$) increases, the mean value of the peak amplitude raises linearly with $T$. Standard deviation of the distribution also rises with the square root of T as predicted by the theory.

For the same applied gate voltage ( $|V_G|$) of 0 V, the avalanche amplitude distribution with $\bar{T} = 15$ is presented in Figure 5.12 (b). It is observed that when the triggered microcells ($T$) rises, the mean value of the peak amplitude raises linearly with $T$. It is also noticed that the peak voltage amplitude with $\bar{T}$ of 15 is higher compared to that of $\bar{T}$ of 5 (Figure 5.12 (b)). This is because for $\bar{T}$ of 15, more pixels are triggered and more current is measured at the output resulting in more measured voltage across the load resistor. Standard deviation of the distribution also rises with the square root of T as predicted by the theory. Therefore the amplitude distribution shown in Figure 5.12 (b) confirms the similar finding as observed in Figure 5.12 (a).



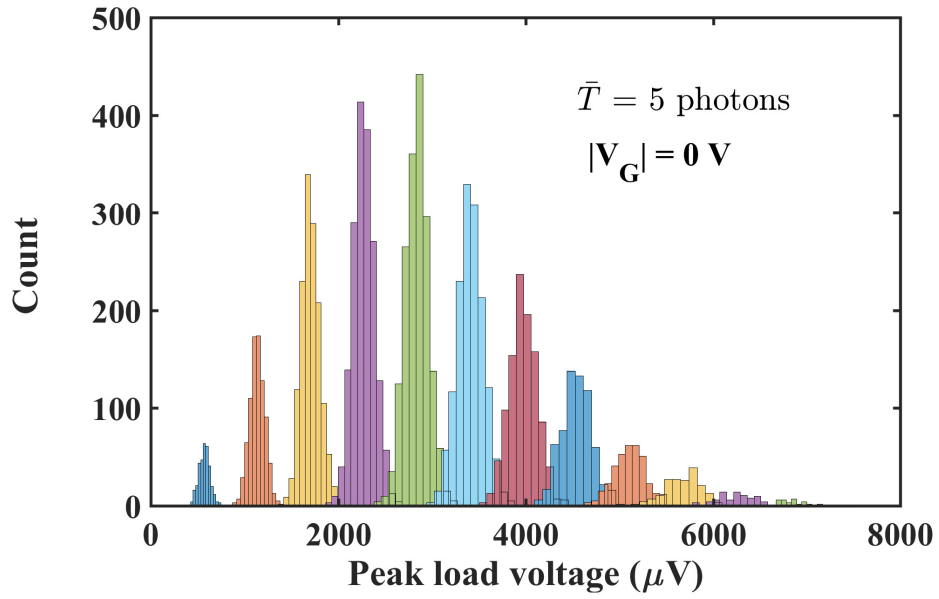

(a)



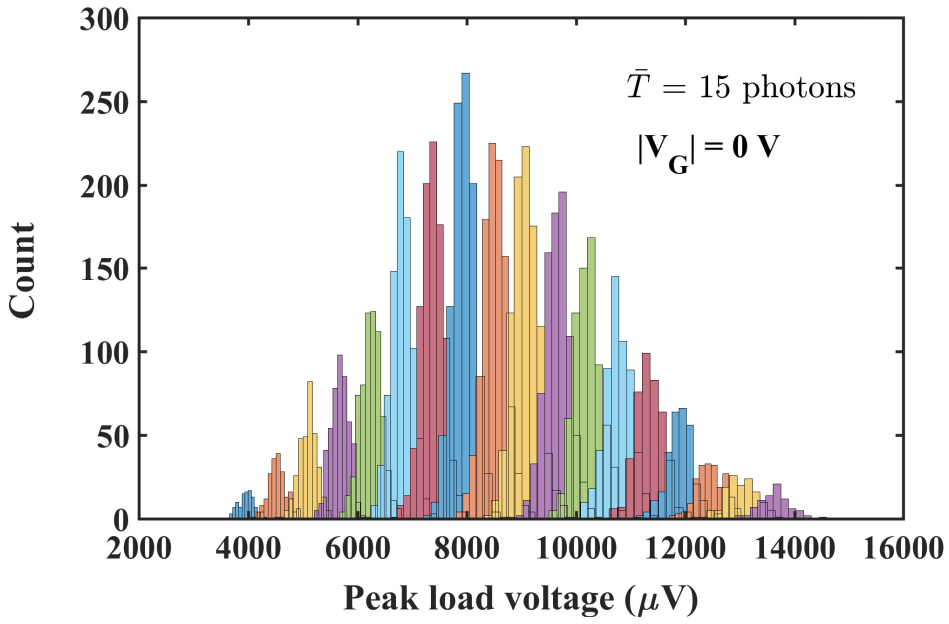

(b)

**Figure 5.11:** Expected count using probability distribution function varying the illumination condition such as (a) 5 photons on average, (b) 15 photons on average.

The impact of the applied gate voltage on the avalanche amplitude distribution has been investigated. In order to study the impact of the applied gate voltage on the avalanche




**(a)**




**(b)**

**Figure 5.12:** Simulated photoelectron spectrum for the applied gate voltage, $|V_G|$, of 0 V with variation of the illumination condition such as (a) 5 photons on average, (b) 15 photons on average.

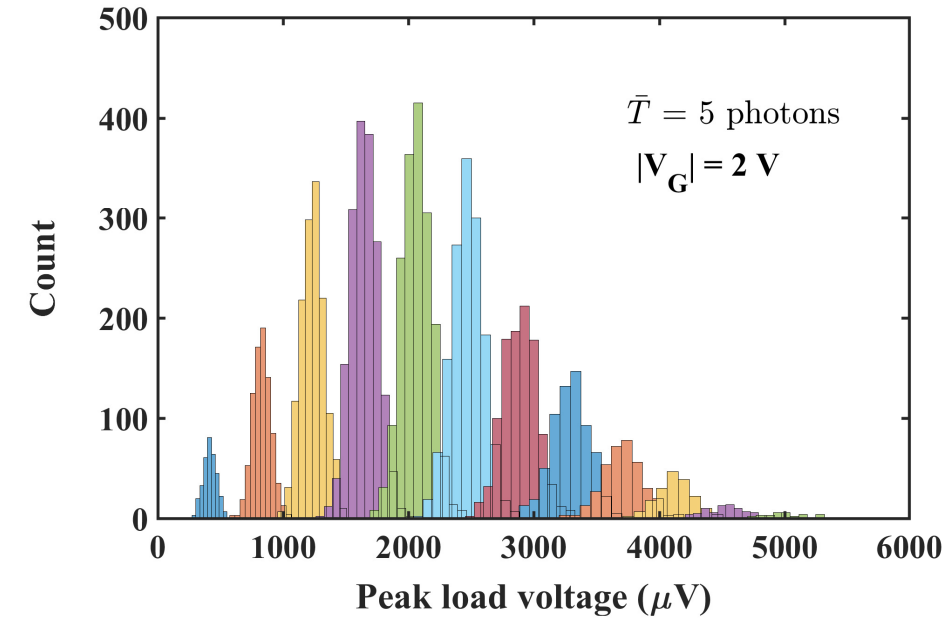
amplitude distribution, Monte Carlo simulation has also been performed for different gate voltages with $\bar{T}$ =5 and $\bar{T}$ =15. When the gate voltage magnitude increases to 2 V, the

mean value of the peak voltage amplitude reduces for both distribution due to the increase of breakdown voltage reducing the excess bias voltage.

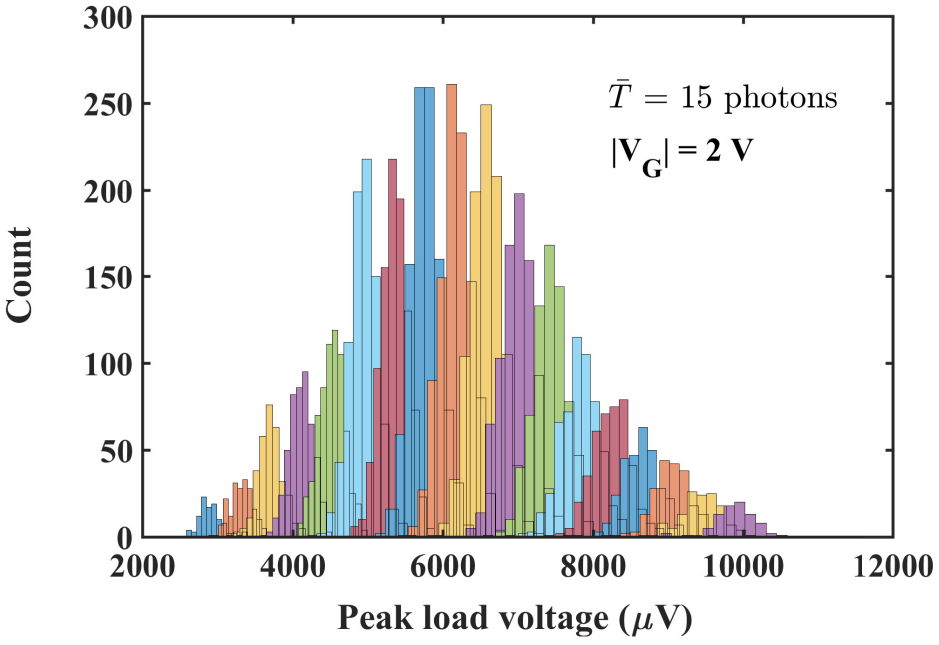
Figure 5.13 (a) shows the avalanche amplitude distribution with $\bar{T} = 5$ for applied gate voltage ($|V_G|$) of 2 V. Since the breakdown voltage ($V_{br}$) increases with the increase of gate voltage ($V_G$) which is particular to the PGSPAD device, the peak output current reduces due the decrease of excess bias voltage. Therefore, the peak load voltage with $|V_G|$ of 2 V is lower compared to that for $|V_G|$ of 0 V (Figure 5.12 (a)). Moreover, because of the dependency of breakdown voltage ($V_{br}$) on the gate voltage ($V_G$) specific to the PGSPAD device, the small changes in $V_G$ affects the standard deviation of the distribution also through the $V_{br}$ observed in the Figure 5.13(a).

The avalanche amplitude distribution with $\bar{T} = 15$ for $|V_G|$ of 2 V is presented in Figure 5.13 (b). It is observed that for $|V_G|$ of 2 V, the peak load voltage with $\bar{T} = 15$ is higher compared to that with $\bar{T} = 5$ (Figure 5.13 (a)). This is due to the fact that larger $\bar{T}$ of 15, more microcells are triggered providing more output current and large peak load voltage are recorded. In addition, for similar $\bar{T}$ of 15, the peak load voltage with $|V_G|$ of 2 V is lower compared to that for $|V_G|$ of 0 V (Figure 5.12 (b)). This is because the peak output current reduces with reduction of excess bias voltage due to the increase of breakdown voltage with the increase of gate voltage. Therefore the simulation results presented in Figure 5.13 (b) confirms the similar observation observed in Figure 5.13 (a).

The impact of more higher gate voltage on the avalanche amplitude distribution with $\bar{T}$ = 5 and $\bar{T} = 15$ for $|V_G|$ of 2 V is studied also. At first the Monte Carlo simulation has been performed for $\bar{T} = 5$ with gate voltages of 4 V and the avalanche amplitude distribution for the applied gate voltage magnitude, $V_G$, of 4 V is shown in Figure 5.14 (a). It is observed




(a)




(b)

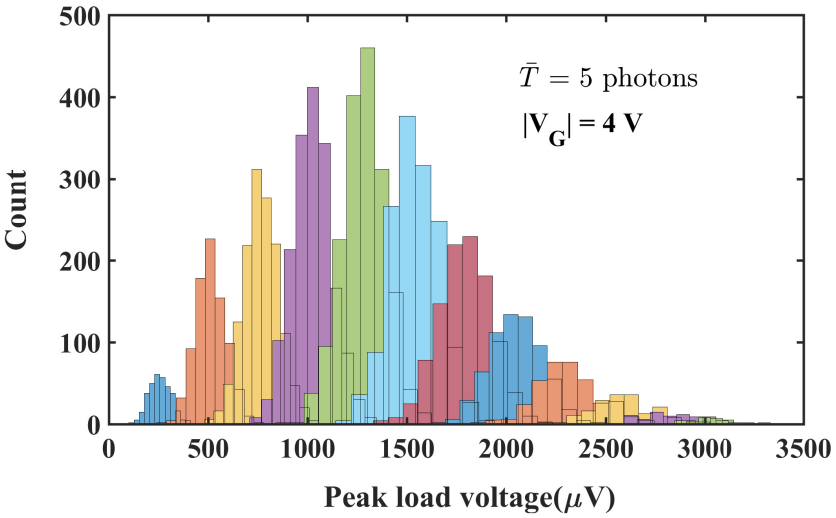
**Figure 5.13:** Simulated photoelectron spectrum for the applied gate voltage, $|V_G|$, of 2 V with variation of the illumination condition such as (a) 5 photons on average, (b) 15 photons on average.

that the peak voltage amplitude reduces further with the increase of $|V_G|$ to 4 V (Figure 5.14 (a)) compared to that with $|V_G|$ of 2 V and 0 V (Figure 5.13 (a) and Figure 5.12 (b)).

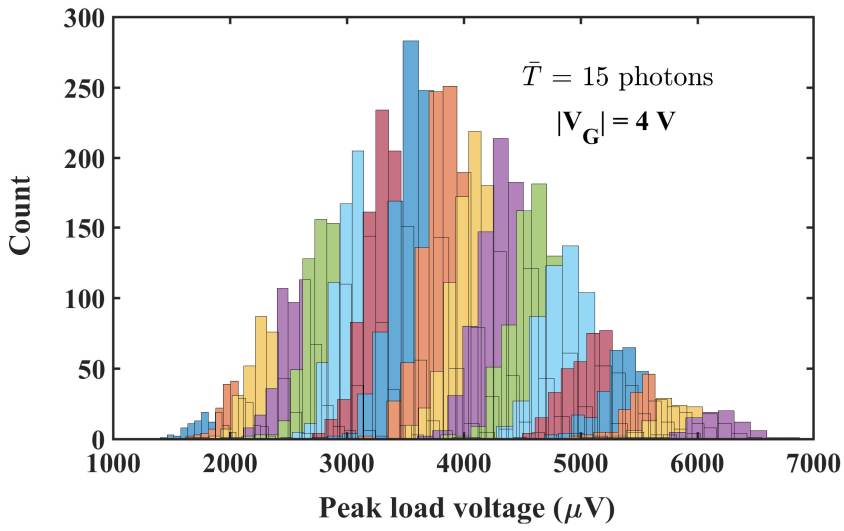
This is because the breakdown voltage ($V_{br}$) increases with the increase of gate voltage ($V_G$) and the peak output current reduces due the decrease of excess bias voltage. Therefore, the peak load voltage with $|V_G|$ of 2 V is lower compared to that for $|V_G|$ of 0 V and $|V_G|$ of 0 V (Figure 5.13 (a) and Figure 5.12 (a)). Moreover, because of the dependency of breakdown voltage ($V_{br}$) on the gate voltage ($V_G$) specific to the PGSPAD device, the increase of gate voltage also causes more spreading in both distribution through the breakdown voltage.

Figure 5.14 (b) shows the result of the Monte Carlo simulation performed for $\bar{T} = 15$ with gate voltages of 4 V. It is observed that for $|V_G|$ of 4 V, the peak load voltage with $\bar{T} = 15$ is higher compared to that with $\bar{T} = 5$ (Figure 5.14 (a)). This is due to the fact that larger $\bar{T}$ of 15, more microcells are triggered providing more output current and large peak load voltage are recorded. In addition, for similar $\bar{T}$ of 15, the peak load voltage with $|V_G|$ of 4 V is lower compared to that for $|V_G|$ of 2 V and $|V_G|$ of 0 V (Figure 5.13 (b) and Figure 5.12 (b)). This is because the peak output current reduces with reduction of excess bias voltage due to the increase of breakdown voltage with the increase of gate voltage. Therefore the simulation results presented in Figure 5.14 (b) confirms the similar observation observed in Figure 5.13 (b).

Finally, Monte Carlo simulations have been performed for another distribution with mean value of ($\bar{T}$) of 25 considering similar scenario (an 8 $\times$ 8 array with 5% tolerance on the quenching resistor, $R_{quench}$, and 0.1 % tolerance on the breakdown voltage, $V_{br}$) including the effect of extra gate terminal. The avalanche amplitude distribution with $\bar{T} =$ 25 is shown in Figure 5.15. For this simulation two different gate voltage of 0 V and 2 V is considered. Figure 5.15 (a) shows the avalanche amplitude distribution with $\bar{T} = 25$ for the applied gate voltage ( $|V_G|$) of 0 V. As the triggered microcells ($T$) increases, the mean




**(a)**




**(b)**

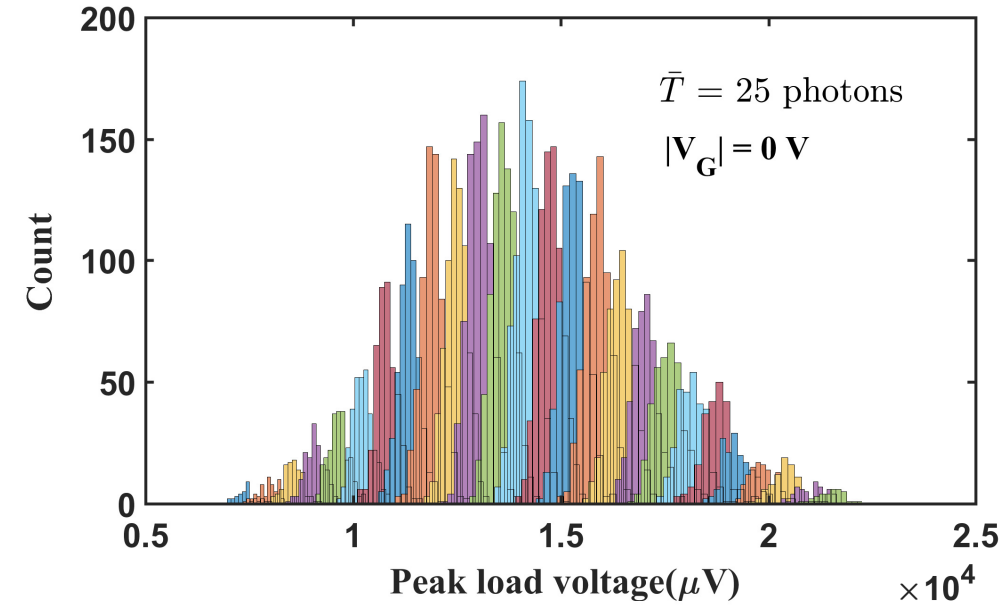
**Figure 5.14:** Simulated photoelectron spectrum for the applied gate voltage, $|V_G|$, of 4 V with variation of the illumination condition such as (a) 5 photons on average, (b) 15 photons on average.

value of the peak amplitude raises linearly with $T$. Standard deviation of the distribution also rises with the square root of T as predicted by the theory. It is observed that the peak voltage is highest compared to that with $\bar{T} = 15$ and $\bar{T} = 5$ presented earlier.

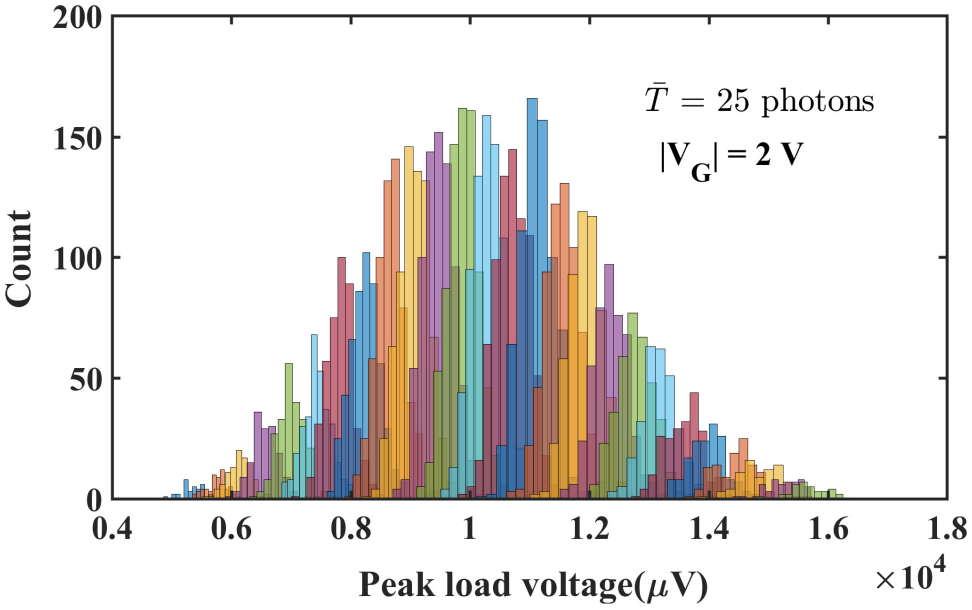
The similar avalanche amplitude distribution with $\bar{T} = 25$ for the $|V_G|$ of 2 V,is presented in Figure 5.15 (b). It is observed that when the triggered microcells ($T$) rises, the mean value of the peak amplitude raises linearly with $T$. It is also noticed that the peak voltage amplitude with $\bar{T}$ of 25 is higher compared to that of $\bar{T}$ of 15 and $\bar{T}$ of 5 shown earlier. Moreover, the peak value of the voltage amplitude is lower compared to that with $|V_G|$ of 0 V (Figure 5.15 (a)). Moreover, because of the dependency of breakdown voltage ($V_{br}$) on the gate voltage ($V_G$) specific to the PGSPAD device, the increase of gate voltage also causes changes in the spreading in standard deviation. Therefore, the mean value of the peak amplitude reduces with the increase of gate voltage as expected. The results also confirm the similar finding observed previously for other two distributions (Figure 5.12 and Figure 5.13). As a summary, the developed PGSPAD SiPM model correctly captures phtoelectron spectrum with different illumination conditions with the effect of extra gate terminal.

### 5.4.4 Noise Behavior of SiPM

The stochastic noise behavior of the SiPM has been incorporated with the impact of gate voltage to study a more real behavior of SiPM detectors which has not been captured by the reported SiPM models so far. The PGSPAD SiPM noise model simulates the dark current due to noise generated phenomena, at different excess bias voltages with the impact of gate voltage.




**(a)**




**(b)**

**Figure 5.15:** Simulated photoelectron spectrum for 25 photons on average with two different applied gate voltages, (a) $|V_G|$, of 0 V, (b) $|V_G|$, of 2 V.

Figure 5.16 shows the simulated dark current noise as a function of the applied gate voltage, $V_G$, with different excess bias voltages, $V_{Exc}$ of 0.4 V, 0.8 V, 1.2 V, and 1.6 V. The $|V_G|$ is changed from 2 V to 14 V. The dark current noise reduces with the increase of $V_G$ for a fixed $V_{Exc}$. This is due to the fact that as the $|V_G|$ rises the breakdown voltage raises and the probability of avalanche for the carrier generated due to band-to-band tunneling, thermally generated, and trapped carriers decreases. Therefore, the dark current noise decreases. However, the dark current raises with the rise of $V_{Exc}$ as expected with standard SiPM. It was found that the gate voltage primarily affects the dark current noise due to band-to-band tunneling through the average electric field (equation 5.8). In addition, the simulation results presented in Figure 5.16 verifies the tuning of dark current noise through the applied gate voltage.

The dark current noise has been simulated with the variation of $V_{Exc}$ with different $V_G$ of 2 V, 4 V, 6 V, 8 V, 10 V, and 12 V also. The $V_{Exc}$ is varied from 0.4 V to 1.6 V. The simulated response is shown in Figure 5.17. The dark current noise raises with the rise of $V_{Exc}$ for a fixed $|V_G|$. This is because the drift velocity of the thermally generated

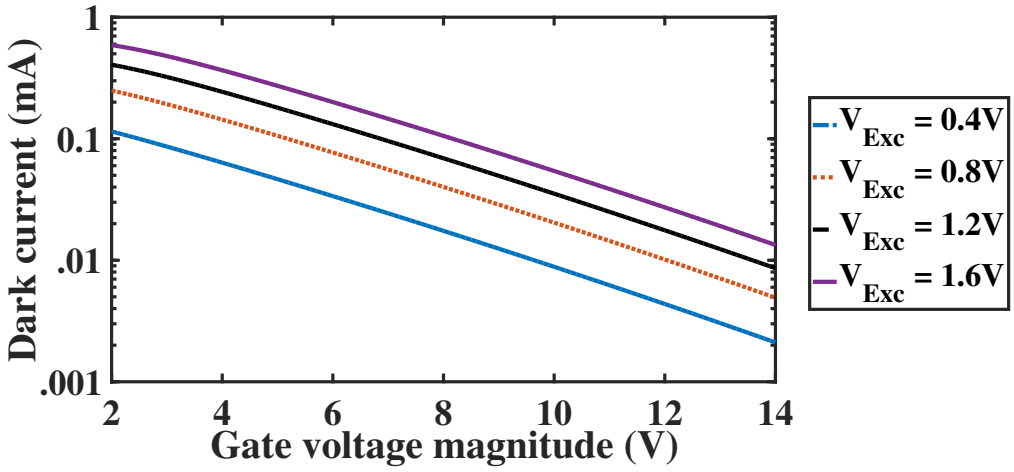



**Figure 5.16:** Simulated dark current noise as a function of the applied gate voltage with different excess bias voltages, $V_{Exc}$, of 0.4 V, 0.8 V, 1.2 V, and 1.6 V.

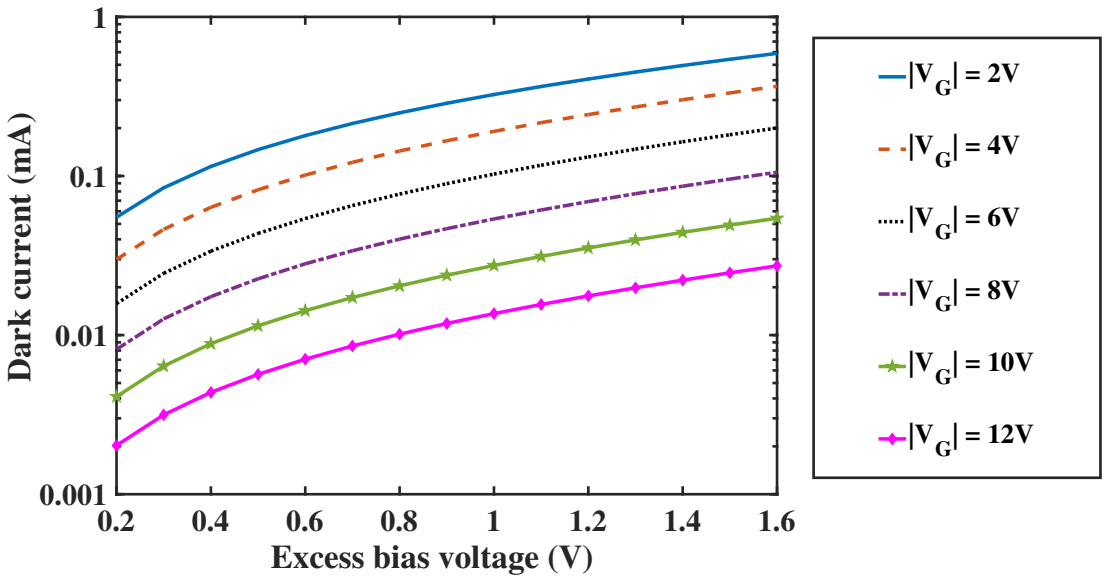



**Figure 5.17:** Simulated dark current noise as a function of excess bias voltages with two different applied gate voltages, $|V_G|$, of 2 V and 6 V.

and trapped carriers increases with the increase of $V_{Exc}$ increasing the dark current noise. However, the dark current noise reduces with the rise of $|V_G|$ confirming the observation found in Figure 5.16 earlier. Figure 5.17 confirms the tunability of dark current noise by the applied gate voltage also. As a summary, the noise model precisely predicts the noise behavior of SiPM detectors with the effect of the applied gate voltage.

## 5.5 Model Validation with Measurements

In order to validate and prove the accuracy of the developed PGSPAD SiPM model, simulation results have been compared with the measurement results. The measured results are obtained from the testing of a PGSPAD SiPM, a 18 $\times$ 18 array, fabricated in 0.5 $\mu$m CMOS process. Figure 5.18 compares the simulation results of the PGSPAD SiPM dark current noise for the variation of applied gate voltage with the experimental measurements.

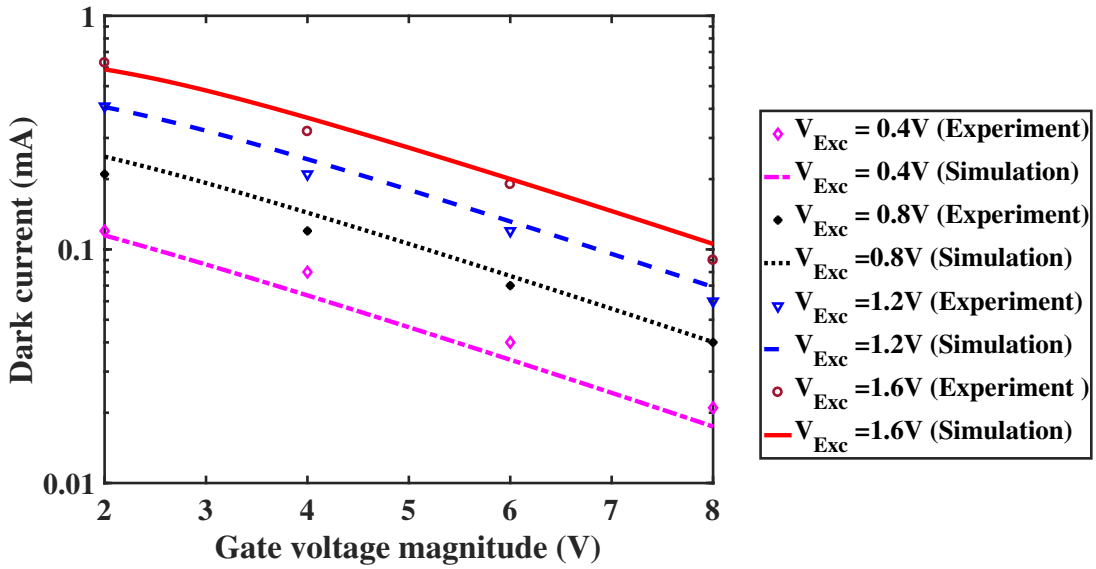



**Figure 5.18:** Dark current noise as a function of applied gate voltages, $|V_G|$, : simulation vs. experiments for different excess bias voltages, $|V_{Exc}|$, of 0.4 V, 0.8 V, and 1.2 V.

It is also observed that the simulation results of the dark current noise are in good match with the experimental results. Thus, the developed model can precisely predicts the noise behavior of PGSPAD SiPM with the impact of gate voltage.

The simulation results of SiPM dark current noise for the variation of excess bias voltage has been compared with the experimental measurements in Figure 5.19. The measured results have been collected from the testing of a PGSPAD SiPM, a 18 × 18 array, fabricated in 0.5 $\mu$m CMOS process. It is observed that the simulation results are in good agreement with the experimental results. Thus, the developed model can accurately capture the stochasticity of PGSPAD SiPM noise behavior with the effect of applied gate voltage.

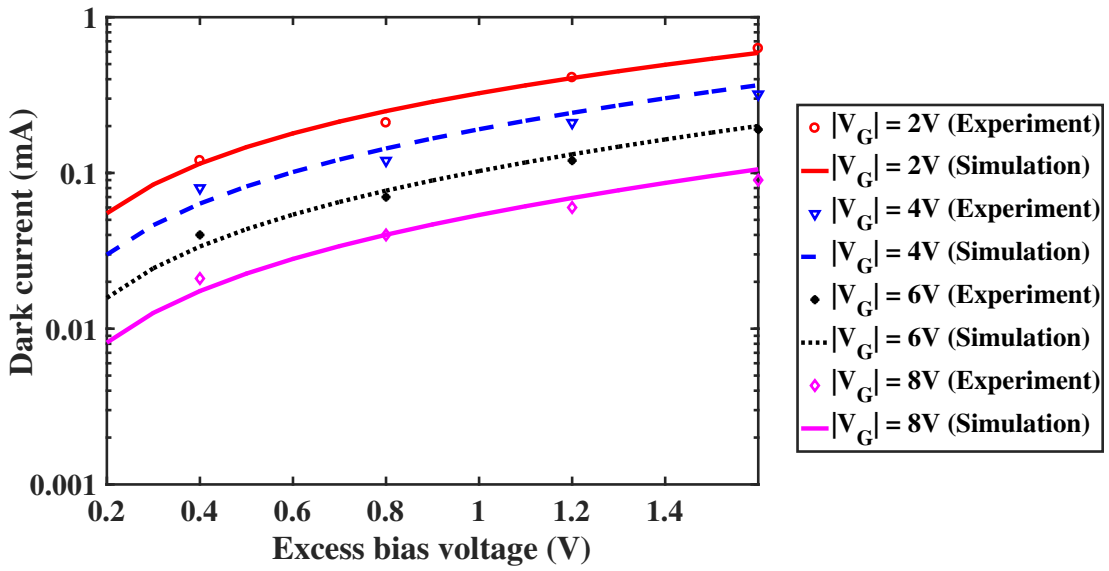



**Figure 5.19:** Dark current noise as a function of excess bias voltages, $|V_{Exc}|$, : simulation vs. experiments for different applied gate voltages, $|V_G|$, of 2 V, 4 V, 6 V, and 8 V.

## 5.6 Conclusion

This chapter presents a novel and comprehensive electrical model for silicon photomultiplier based on perimeter gated SPAD. In order to study the complete behavior of PGSPAD SiPM, the proposed model includes the impact of additional gate terminal and all parasitic components. The model also precisely captures the dark current noise behavior. The developed model investigates the SiPM behavior with the impact of gate terminal and predicts the randomness of SiPM dark current noise. The model has been verified with the experimental measurements of PGSPAD SiPM fabricated in 0.5 $\mu$m CMOS process. It was observed that the simulation results exhibit good matching with the experimental results confirming the precision and conformity of the developed model. The capability to modulate the dark current noise of SiPM using the gate voltage has been validated in the model also . The developed model can be used to study the comprehensive behavior of SiPMs based on

PGSPAD. It also helps the designer to design the optimal readout electronics considering the effect of gate terminal and reduces the design cycle.

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# Chapter 6
# Conclusion and Future Work

## 6.1 Original Contribution

CMOS silicon photomultipliers based on perimeter gated single photon avalanche diode are presented in this dissertation. This silicon photomultiplier adopts the benefits of standard CMOS process with added advantages of the perimeter gated single photon avalanche diode such as prevention of premature edge breakdown, tunabilty of noise and sensitivity.

The original contributions of this work are:

- The capability of the additional gate terminal to control the breakdown voltage has been verified for the perimeter gated SPAD device fabricated in standard 0.5 $\mu$m high voltage and 0.35 $\mu$m CMOS processes for the first time.

- Experimental characterization of the perimeter gated SPAD's noise over a range of temperature with varying applied gate voltage for the first time. Devices were fabricated and tested for varying the gate voltage of perimeter gated SPAD over a range of temperatures.

- Development of a full chip CMOS analog silicon photomultiplier (SiPM) using perimeter gated SPAD and first full characterization. The SiPM based on perimeter gated SPAD was characterized for dark current (noise) with the variation of the gate voltage and the temperature, sensitivity, signal to noise ratio throughout the visible

spectral range for varying the bias voltages. The signal to noise ratio of the developed silicon photo multiplier can be tuned over a range of 1 to 1150 though the applied gate voltage of perimeter gated SPAD reducing dark current.

- Demonstration of the first ever CMOS digital SiPM with fully digital asynchronous address event representation (AER) readout to provide high bandwidth. The digital SiPM provides tunability of noise performance using perimeter gated SPADs based pixel. Achieved array-level dynamic range was 162 dB with maximum readout speed of 80 MHz. The measured response of the PGSPAD digital SiPM with AER readout over a wide range of optical power showed the feasibility of the detector for a broad range of nuclear medical imaging applications including SPECT and PET applications. The AER protocol would be helpful to perform the position reconstruction, the usual requirement of the Anger camera in SPECT applications, and pinpoint the scintillation point inside the crystal or crystal matrix in a large PET detectors. The proposed architecture is scalable and can be extended to a larger array with added advantage of the perimeter gated SPAD's tunable noise floor, sensitivity.

- Development of a new electrical model for simulating the perimeter gated SPAD (PGSPAD) based silicon photomulitiplier (SiPM). This is the first reported model to predict the complete behavior of SiPM signal with the impact of the gate voltage. The comprehensive model accurately simulate the static, dynamic, and stochastic noise behavior of the SiPM with the effect of additional gate terminal. The model has been validated with the experimental measurements and showed very good matching.

## 6.2 Future Work

This research can be moved forward by studying the following issues as future works

- The success of the extra gate terminal to control the breakdown voltage can be verified for the perimeter gated SPAD device fabricated in lower processes.
- The readout circuit such as transimpedance amplifier or charge sensitive preamplifier and ADC can be integrated with the analog CMOS SiPM using PGSPAD on the same chip to make a complete system with improved performance, compact, and cheaper.
- For PET scanners, an array of chips is used. Minimization of the dead area at the chip level and design of the interface for digital SiPM with AER chips can be explored to make it applicable for PET scanners.
- The power consumption of the SiPM detector can be studied making it suitable for mobile biomedical applications, portable radiation detection, etc.

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# Appendix

# Noise Characterization of Analog SiPM

The dark current noise has been measured for the designed CMOS analog SiPM using PGSPAD based pixel. The SiPM was implemented in standard 0.5 $\mu$m CMOS process. The measurement results obtained from three tested chips with the variation of gate voltage, $|V_G|$, and excess bias voltage, $V_{Exc}$, are presented here.

## Noise Characterization with Variation of Gate Voltage

Figure A.1 shows the measured dark current noise for three different chips (chip1, chip2, and chip3) with variation of gate voltage, $|V_G|$, for excess bias voltage, $V_{Exc}$, of 0 V  For all three chips, the noise decreases with the increase of gate voltage.

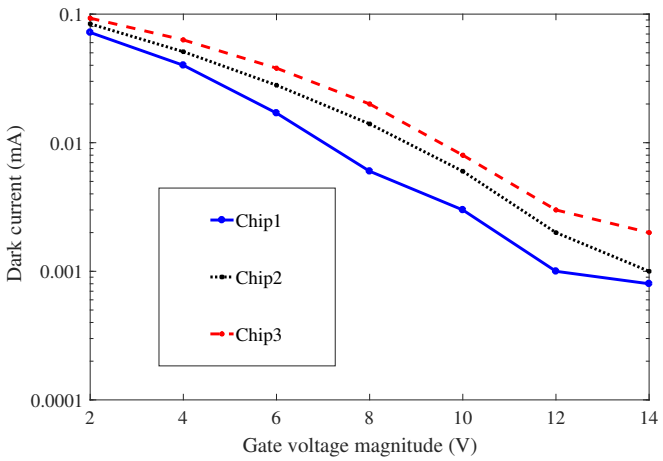



**Figure A.1:** Measured dark current noise with variation of gate voltage, $|V_G|$, for excess bias voltage, $V_{Exc}$, of 0 V.

The measured dark current noise for three different chips (chip1, chip2, and chip3) with variation of gate voltage, $|V_G|$, for excess bias voltage, $V_{Exc}$, of 0.4 V is shown in Figure A.2. It is observed that the dark current reduces with the raise of gate voltage in a similar way as observed in Figure A.1. This is due to the fact that with the increase of gate voltage breakdown voltage increases. The increase of gate voltage reduces the probability of avalanche for noise generated free carriers. However, for all the three chips, the dark current is higher compared to that of with $V_{Exc}$, of 0 V (Figure A.1) as expected.

Figure A.3 shows the measured dark current noise for $V_{Exc}$ of 0.8 V. The results also confirm the same conclusion that dark current decreases with the applied gate voltage. This is due to the fact that with the increase of gate voltage breakdown voltage increases. The increase of gate voltage reduces the probability of avalanche for noise generated free carriers. For all the three chips, the dark current is higher compared to those with $V_{Exc}$, of 0 V and 0.4 V (Figure A.1 and Figure A.2) as expected.

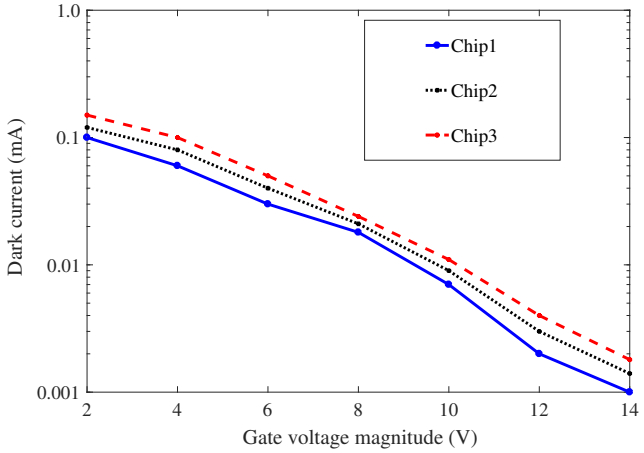



**Figure A.2:** Measured dark current noise with variation of gate voltage, $|V_G|$, for excess bias voltage, $V_{Exc}$, of 0.4 V.

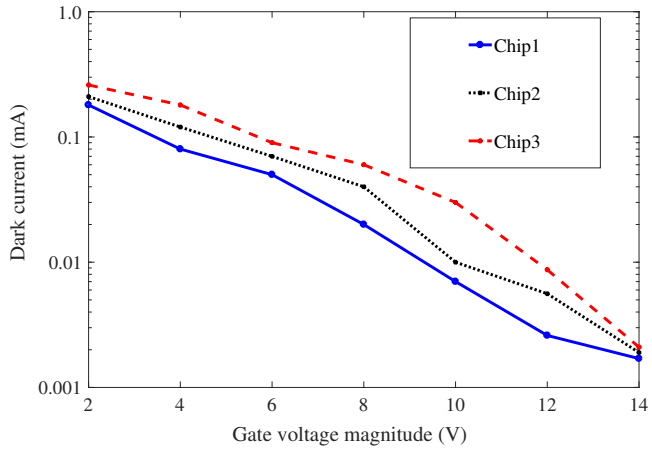



**Figure A.3:** Measured dark current noise with variation of gate voltage, $|V_G|$, for excess bias voltage, $V_{Exc}$, of 0.8 V.

Figure A.4 shows the measured dark current noise for $V_{Exc}$ of 1.2 V. It is observed that increasing the $V_{Exc}$ to 1.2 V, the dark current increases and is higher compared to those with $V_{Exc}$, of 0 V, 0.4 V and 0.8 V (Figure A.1, Figure A.2 and Figure A.3). This is because as the excess bias voltage increases, the drift velocity of noise generated carriers increases. Therefore, the dark current noise increases with increase of excess bias voltage. However, raising the applied gate reduces the dark current observed in the measurement from all three chips. This is due to the fact that with the increase of gate voltage breakdown voltage increases. The increase of gate voltage reduces the probability of avalanche for noise generated free carriers.

The measured dark current noise for $V_{Exc}$ of 1.6 V is reported in Figure A.5. The dark current increases as expected. The dark is higher compared to those with $V_{Exc}$, of 0 V, 0.4 V, 0.8 V, and 1.2 V (Figure A.1, Figure A.2, Figure A.3, and Figure A.4). This is because as the excess bias voltage increases, the drift velocity of noise generated carriers increases. Therefore, the dark current noise increases with increase of excess bias voltage. However, raising the applied gate reduces the dark current observed in the measurement from all three chips. This is due to the fact that with the increase of gate voltage breakdown voltage increases. The increase of gate voltage reduces the probability of avalanche for noise generated free carriers. It is also observed that the dark current decreases with increase of gate voltage applied at the additional gate terminal confirming the conclusions observed in the previous measured results (Figure A.1, Figure A.3, Figure A.2 and Figure A.4) .

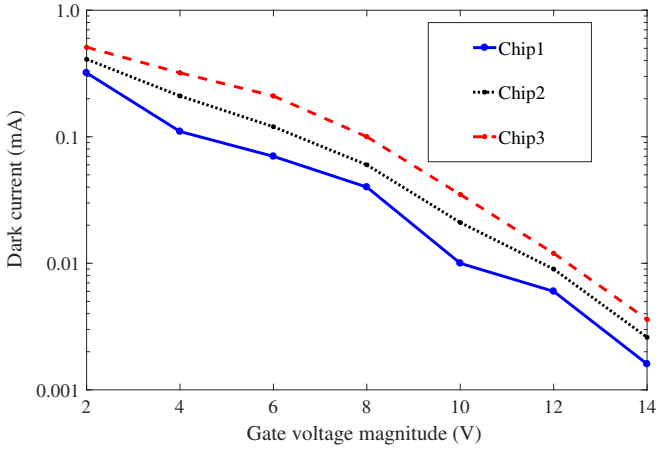



**Figure A.4:** Measured dark current noise with variation of gate voltage, $|V_G|$, for excess bias voltage, $V_{Exc}$, of 1.2 V.

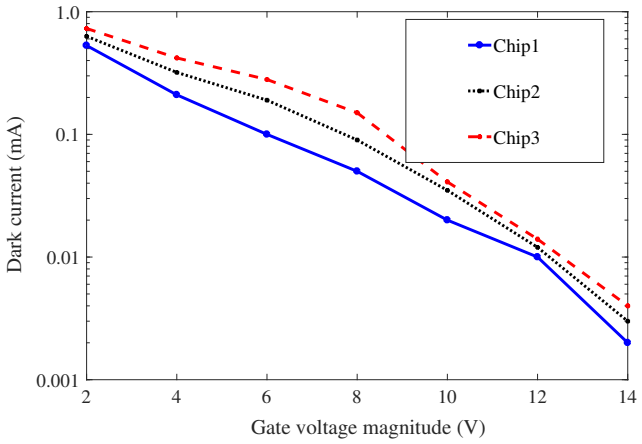



**Figure A.5:** Measured dark current noise with variation of gate voltage, $|V_G|$, for excess bias voltage, $V_{Exc}$, of 1.6 V.

## Noise Characterization with Variation of Excess Bias Voltage

Figure A.6 shows the measured dark current noise for three different chips (chip1, chip2, and chip3) with variation of excess bias voltage, $V_{Exc}$, for gate voltage, $|V_G|$, of 2 V. It is observed that the noise increases with the increase of excess bias voltage for all three chips. This is because as the excess bias voltage increases, the drift velocity of noise generated carriers increases. Therefore, the dark current noise increases with increase of excess bias voltage.

The measured dark current noise for three different chips (chip1, chip2, and chip3) with variation of excess bias voltage, $V_{Exc}$, for gate voltage, $|V_G|$, of 4 V is reported in Figure A.7. The result also confirms that the dark current noises with the increase of excess bias voltage. This is because as the excess bias voltage increases, the drift velocity of noise generated carriers increases. Therefore, the dark current noise increases with increase of excess bias voltage. However, the dark current noise with $|V_G|$, of 6 V is lower compared to that with $|V_G|$, of 2 V (Figure A.6). This is due to the fact that with the increase of gate voltage breakdown voltage increases. The increase of gate voltage reduces the probability of avalanche for noise generated free carriers.

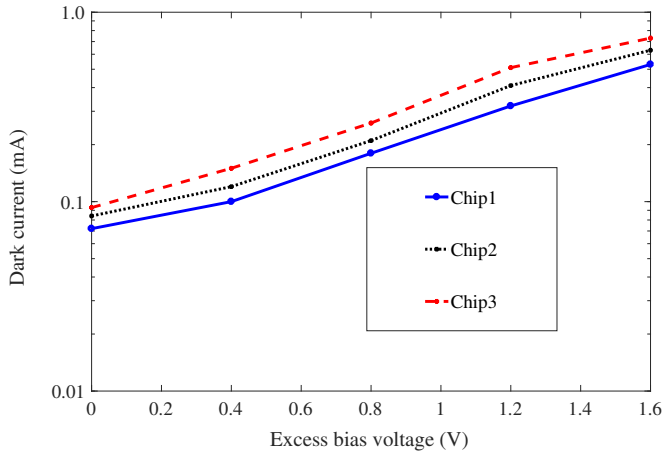



**Figure A.6:** Measured dark current noise with variation of excess bias voltage, $V_{Exc}$, for gate voltage, $|V_G|$, of 2 V.

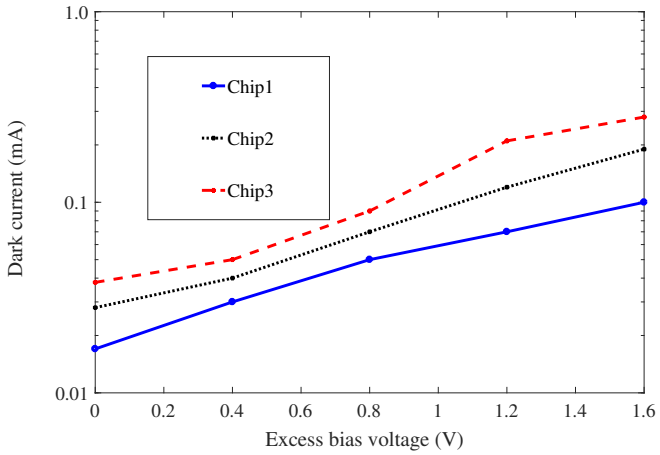



**Figure A.7:** Measured dark current noise with variation of excess bias voltage, $V_{Exc}$, for gate voltage, $|V_G|$, of 6 V.

Figure A.8 shows the measured dark current noise for three different chips (chip1, chip2, and chip3) with variation of excess bias voltage, $V_{Exc}$, for gate voltage, $|V_G|$, of 10 V. It is observed that the noise raises with the rise of excess bias voltage for all three chips. Figure A.8 also confirms that the dark current noise becomes lower by increasing the gate.

The measured dark current noise for three different chips (chip1, chip2, and chip3) with variation of excess bias voltage, $V_{Exc}$, for gate voltage, $|V_G|$, of 12 V is reported in Figure A.9. The result also confirms that the dark current noises with the increase of excess bias voltage. However, the dark current noise with $|V_G|$, of 12 V is lower compared to that with $|V_G|$, of 2 V, 6 V, and 10 V (Figure A.6, Figure A.7, and Figure A.8).

Figure A.10 shows the measured dark current noise for three different chips (chip1, chip2, and chip3) with variation of excess bias voltage, $V_{Exc}$, for gate voltage, $|V_G|$, of 16 V. It is observed that the noise increases with the rise of excess bias voltage for all three chips. However, the the dark current noise is lower compared to that with $|V_G|$, of 2 V, 6 V, 10 V, and 12 V (Figure A.6, Figure A.7, Figure A.8, and Figure A.9).

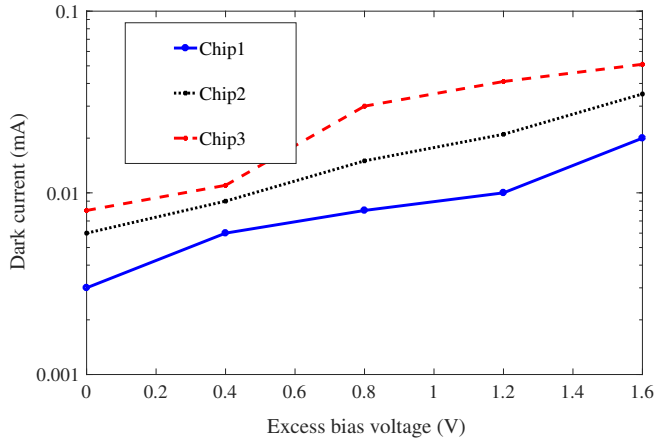



**Figure A.8:** Measured dark current noise with variation of excess bias voltage, $V_{Exc}$, for gate voltage, $|V_G|$, of 10 V.

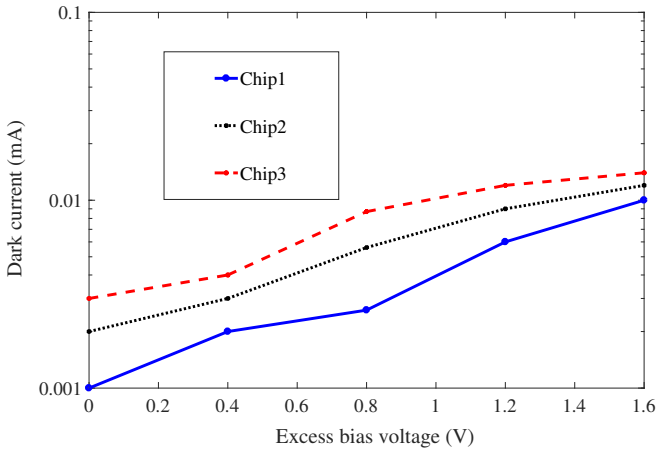



**Figure A.9:** Measured dark current noise with variation of excess bias voltage, $V_{Exc}$, for gate voltage, $|V_G|$, of 12 V.

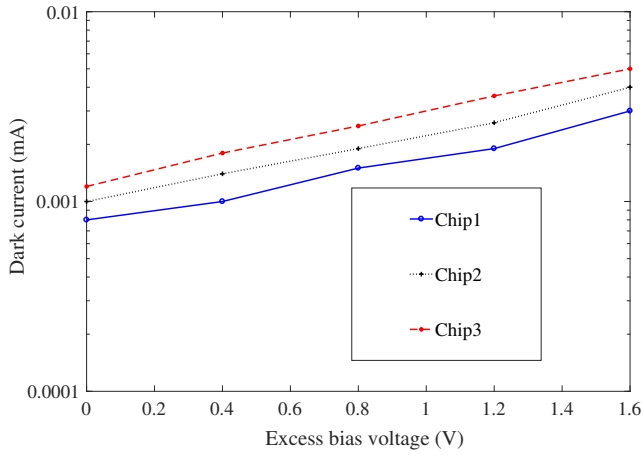



**Figure A.10:** Measured dark current noise with variation of excess bias voltage, $V_{Exc}$, for gate voltage, $|V_G|$, of 16 V.

As a summary, the results presented here confirms that the dark current noise increases with the increase of excess bias voltage as expected. However, the dark current noise can be reduced by increasing the applied gate voltage at the additional gate terminal.

# Noise Characterization of Pixel of Digital SiPM

The dark count rate noise has been measured for the pixel of designed CMOS digital SiPM using PGSPAD based pixel with AER readout. The SiPM was implemented in standard 0.5 $\mu$m CMOS process. The measurement results obtained from two tested chips with the variation of gate voltage, $|V_G|$, and excess bias voltage, $V_{Exc}$, are presented here.

The measured dark count rate noise for two different chips (chip1 and chip2) with variation of gate voltage, $|V_G|$, and for excess bias voltage, $V_{Exc}$, of 2.0 V is shown in Figure A.11. It is observed that the dark count rate noise reduces with the raise of gate voltage as expected and described earlier.

Figure A.12 shows the measured dark count rate noise for $V_{Exc}$ of 2.5 V with variation of gate voltage, $|V_G|$. The results also confirm the same conclusion that dark count rate noise decreases with the applied gate voltage. For all the two chips, the dark count rate noise is higher compared to those with $V_{Exc}$, of 2.0 V (Figure A.11) as expected.

The measured dark count rate noise for two different chips (chip1 and chip2) for excess bias voltage, $V_{Exc}$, of 3.0 V with variation of gate voltage, $|V_G|$, is shown in Figure A.13. The dark count rate noise reduces with the increase of applied gate voltage. It is observed that the dark count rate noise is higher compared to those with $V_{Exc}$, of 2.0 V and 2.5 V

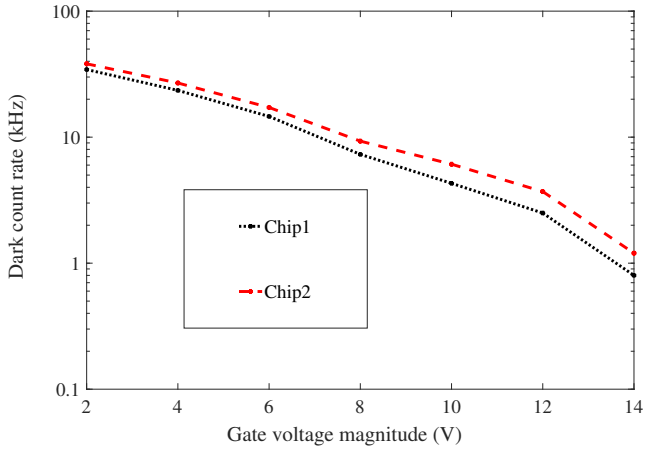



**Figure A.11:** Measured dark count rate noise of PGSPAD based pixel of digital SiPM with variation of gate voltage, $|V_G|$, and for excess bias voltage, $V_{Exc}$, of 2 V.

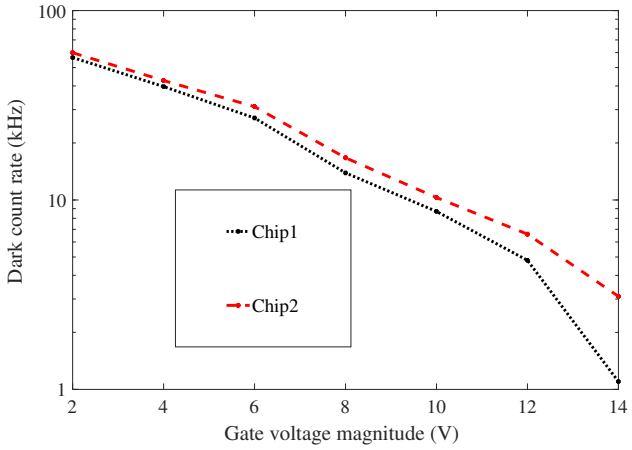



**Figure A.12:** Measured dark count rate noise of PGSPAD based pixel of digital SiPM with variation of gate voltage, $|V_G|$, and for excess bias voltage, $V_{Exc}$, of 2.5 V.

(Figure A.11 and Figure A.11) as expected. Therefore, the dark count rate noise of the digital SiPM can be reduced by increasing the applied gate voltage.

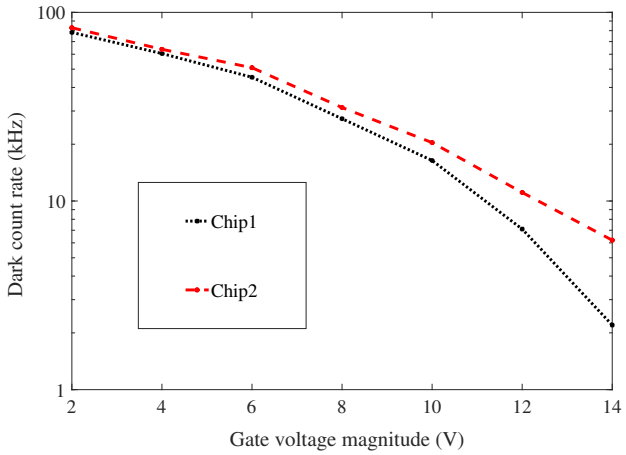



**Figure A.13:** Measured dark count rate noise of PGSPAD based pixel of digital SiPM with variation of gate voltage, $|V_G|$, and for excess bias voltage, $V_{Exc}$, of 3.0 V.

# Vita

Mst Shamim Ara Shawkat is currently pursuing the Ph.D. degree under the supervision of Dr. Nicole McFarlane in electrical and computer engineering with the University of Tennessee, Knoxville. Her research focuses on CMOS sensor design and characterization. She earned the B.Sc. degree in electrical and electronic Engineering from the Bangladesh University of Engineering and Technology (BUET) in 2002, and the M.Sc. degree in global information and telecommunications from Waseda University, Japan in 2006. Before joining University of Tennessee, she was employed as an Assistant Professor in BUET. Her research interests lie in mixed-signal circuit design, photodetector modeling, design, and testing, neuromorphic computing, biomedical sensors and wireless communications.