

Design and Testing of the Auxiliary Circuit and Cooling System in Medium Voltage Converter

A Dissertation Presented for the
Doctor of Philosophy
Degree
The University of Tennessee, Knoxville

Min Lin
August 2025

Abstract

The 10 kV silicon carbide (SiC) MOSFET is a promising power semiconductor device for high-performance medium-voltage (MV) converters, particularly in grid-connected applications. While offering exceptional device characteristics, its integration introduces significant challenges in the design of auxiliary circuits, thermal management systems, and converter-level testing.

This dissertation addresses these challenges by first focusing on the design of an auxiliary power supply (APS) capable of providing over 10 kV insulation and enhanced electromagnetic interference (EMI) immunity. A comprehensive protection scheme is proposed to isolate faults between multiple outputs, ensuring system reliability. Experimental validation powering a gate driver within an MV converter environment provides practical insights into achieving robust startup behavior and improved EMI resilience.

Temperature sensitive electrical parameters (TSEP) for 10 kV SiC MOSFETs have not been clearly identified in prior literature, yet they are essential for real-time thermal monitoring and health assessment of power modules. This work identifies and evaluates potential TSEPs through both static characterization and double-pulse testing. The influences of gate resistance and load current on TSEP measurements are analyzed to enable accurate calibration across various switching conditions.

At the converter level, the cooling system must not only be thermally effective and compact but also maintain high-voltage insulation between electrical and thermal components. Therefore, electric field simulations are performed to identify insulation stress points and optimize dielectric clearance. This dissertation details the liquid cooling system design, including coolant selection, temperature considerations, flow rate, and pump pressure. For air cooling, airflow distribution across different duct configurations is investigated.

Finally, the flying capacitor converter is fully tested at a DC voltage of 24 kV, successfully validating the aforementioned design methodologies and demonstrating the converter's overall performance and reliability under high-voltage and high EMI operation.

Table of Contents

Chapter 1 Introduction	1
1.1 Wide Bandgap Semiconductors	1
1.2 Medium Voltage Application of WBG Devices	1
1.3 Challenges of Medium Voltage Applications	2
1.3.1 Challenges in High Voltage Isolation	2
1.3.2 Challenges in EMI Tolerance	3
1.3.3 Challenges in Thermal Management	3
1.4 Dissertation Outline	4
Chapter 2 Literature Review	6
2.1 Design and Protection of APS	6
2.1.1 Local APS and Centralized APS	6
2.1.2 Insulation Design	11
2.1.3 EMI Tolerance	12
2.1.4 APS Protection	15
2.2 TSEP Selection for 10 kV SiC MOSFET	17
2.2.1 TSEP of Low Voltage Devices	17
2.2.2 TSEP of 10 kV SiC MOSFET	18
2.3 Cooling Design for MV Converter	18
2.3.1 Liquid Cooling	19
2.3.2 Two-phase Cooling	23
2.3.3 Air Cooling	26
2.4 Summary	30
Chapter 3 High Voltage Auxiliary Power Supply Design	31
3.1 Auxiliary Power Supply Design Requirements	31
3.1.1 Insulation Requirements	31
3.1.2 Interwinding Capacitance	32
3.2 Series LLC APS Protection Scheme Analysis	38
3.2.1 Operation Analysis Under Fault	38
3.2.2 Protection Scheme Analysis	42
3.3 Flybuck APS Testing in MV Converter	50

3.3.1	Interwinding Capacitance	51
3.3.2	APS Testing with Gate Driver	54
3.3.3	APS Mis-trigger Issue.....	57
3.4	Summary	61
Chapter 4 TSEP Selection for 10 kV SiC MOSFET Power Modules		63
4.1	Static TSEP	63
4.1.1	Forward Conduction Characteristics.....	63
4.1.2	Reverse Conduction Characteristics	67
4.1.3	Transfer Characteristics	67
4.2	Dynamic TSEP.....	67
4.2.1	Experimental Test Setup	67
4.2.2	Turn on Transient TSEP	71
4.2.3	Turn off transient TSEP	73
4.3	Impact Factors.....	77
4.3.1	Gate Resistance	77
4.3.2	Load Current	77
4.3.3	Parasitics	80
4.4	Comparison with Low Voltage SiC	84
4.5	Comparison with 10 kV Discrete Device	86
4.6	Temperature Sensor Based on TSEP	88
\		93
4.7	Summary	94
Chapter 5 Cooling System Design.....		95
5.1	Cooling Design Considering Insulation.....	95
5.2	Liquid Cooling Design.....	100
5.2.1	Coolant Selection.....	100
5.2.2	Cold plate Selection	102
	$R\theta = T_j - T_{case} / Q$	106
5.2.3	Chiller Selection.....	106
5.3	Air Cooling Design.....	107
5.3.1	Heatsink Selection	107

5.3.2	Power Module Model Building	108
5.3.3	Air duct Design	109
5.4	Experiment Verification.....	122
5.4.1	Straight Air duct Air Velocity Measurement.....	122
5.4.2	Phase Leg Testing	127
5.5	Summary	128
Chapter 6 8-level Flying Capacitor Converter Testing.....		131
6.1	Power Stage Parameters.....	131
6.1.1	Flying capacitor selection	132
6.1.2	Filter inductor.....	136
6.2	Power Module Test	137
6.3	Sensor Calibration.....	139
6.3.1	Current Sensor Calibration	139
6.3.2	Voltage Sensor Calibration	139
6.4	Mechanical Design of MV Phase leg.....	141
6.4.1	Busbar Design.....	141
6.5	MV phase leg testing	147
6.5.1	Static voltage test	147
6.5.2	Voltage balancing and protection	148
6.5.3	Multiple pulse test.....	150
6.6	Summary	150
Chapter 7 New Module Flying Capacitor Converter Testing.....		152
7.1	Power Module Comparison	152
7.1.1	Static Characterization Comparison	154
7.1.2	Junction Capacitance Comparison.....	154
7.1.3	Switching Loss Comparison	159
7.2	Decoupling Capacitor Comparison.....	159
7.3	Device overvoltage protection	164
7.3.1	Voltage sensor.....	164
7.3.2	Device drain source voltage.....	167
7.3.3	Flying capacitor voltage.....	167

7.3.4	Gate signal spikes	167
7.4	Summary	172
Chapter 8	Conclusions and Future Work.....	173
8.1	Summary	173
8.2	Contributions.....	174
8.3	Future Work.....	175
References		176
Vita		192

List of Tables

Table 2-1 Typical local APS operation voltage range, power rating and topology comparison. .	10
Table 2-2 Centralized APS ratings, insulation performance and topology comparison.	10
Table 2-3 Common coolant comparison.	22
Table 3-1 Specifications of LLC series connected converter	39
Table 3-2 Nomenclature of series resonance network	40
Table 3-3. Output voltage without coupling winding	43
Table 3-4. Output voltage with coupling winding.	43
Table 3-5 Interwinding capacitance comparison between different core shape.	53
Table 3-6. Flybuck APS specifications.	58
Table 4-1. Parameters of the XHV-9 10 kV SiC MOSFET Module.	64
Table 4-2. 10 kV SiC MOSFET Module turn on results at 2 Ω external gate resistance.	78
Table 4-3. 10 kV SiC MOSFET Module turn on results at 5 Ω external gate resistance.	78
Table 4-4. Temperature sensitivity of 10 kV SiC MOSFET power module TSEP	86
Table 4-5. Turn on parameters of discrete 10 kV 20 A SiC MOSFET.	87
Table 4-6. Turn off parameters of 10 kV 20 A SiC MOSFET.	87
Table 4-7 di/dt voltage undershoot sensing circuit parameters.	90
Table 5-1. Specification of 5-level MMC.	97
Table 5-2. Common Coolant Comparison.	103
Table 5-3. Nomenclature.	103
Table 5-4. Cooling performance between different cold plates configurations.	104
Table 5-5 Pump pressure at varying flow rate.	107
Table 5-6. Power module thermal characteristics.	109
Table 5-7. Air velocity of T-shape airduct.	113
Table 5-8. Calculation results of slanted airduct.	116
Table 5-9. Air velocity measured at different positions.	124
Table 6-1. 8-level FCC parameters.	131
Table 6-2 Flying capacitor values at seven stages.	133
Table 6-3. TRD at different filter inductance.	136
Table 6-4. Voltage sensor output frequency (MHz)	142
Table 7-1. Comparison of capacitance between different modules.	156

Table 7-2. Powerex module switching loss at 25°C.	160
Table 7-3. Wolfspeed module switching loss at 25°C	160
Table 7-4 Comparison of decoupling capacitors in 8-level and 5-level FCC systems.	162

List of Figures

Figure 2.1. Local APS extracts power from submodule capacitor.	6
Figure 2.2. Centralized APS is powered by an external power source.	9
Figure 2.3 APS grounding scheme.	12
Figure 2.4. Cylindrical capacitance between windings of a toroidal core [62].	14
Figure 2.5. PCB winding to core capacitance distribution [56].	14
Figure 2.6. Planar capacitance between two E cores [69].	16
Figure 2.7. (a) Formed tube cold plate (b) Deep drilled cold plate (c) Pocketed fold fin cold plate (d) Microchannel [97].	20
Figure 2.8. Chiller cooling capacity curve and pump pressure curve [102].	24
Figure 2.9. (a) heat pipe integrated with heatsink (b) heat spreader (c) Heat pipe heat exchanger [105].	25
Figure 2.10. Thermosiphon [109].	27
Figure 2.11. (a) Extruded aluminum heatsinks (b) bonded fin heat sink (c) Zipper fin heatsink [111].	28
Figure 3.1. First scenario electric field distribution with primary cable is centered in core.	33
Figure 3.2. Second scenario electric field distribution with conductor at edge of core opening..	34
Figure 3.3. Hipot test set-up.	35
Figure 3.4. Leakage current is within suitable range at 20 kV.	35
Figure 3.5 Toroidal transformer interwinding capacitance simulation model.	37
Figure 3.6. Four output series LLC topology.	39
Figure 3.7. Resonant voltage gains increase during short circuit.	40
Figure 3.8. Resonant frequency decreases during open circuit.	41

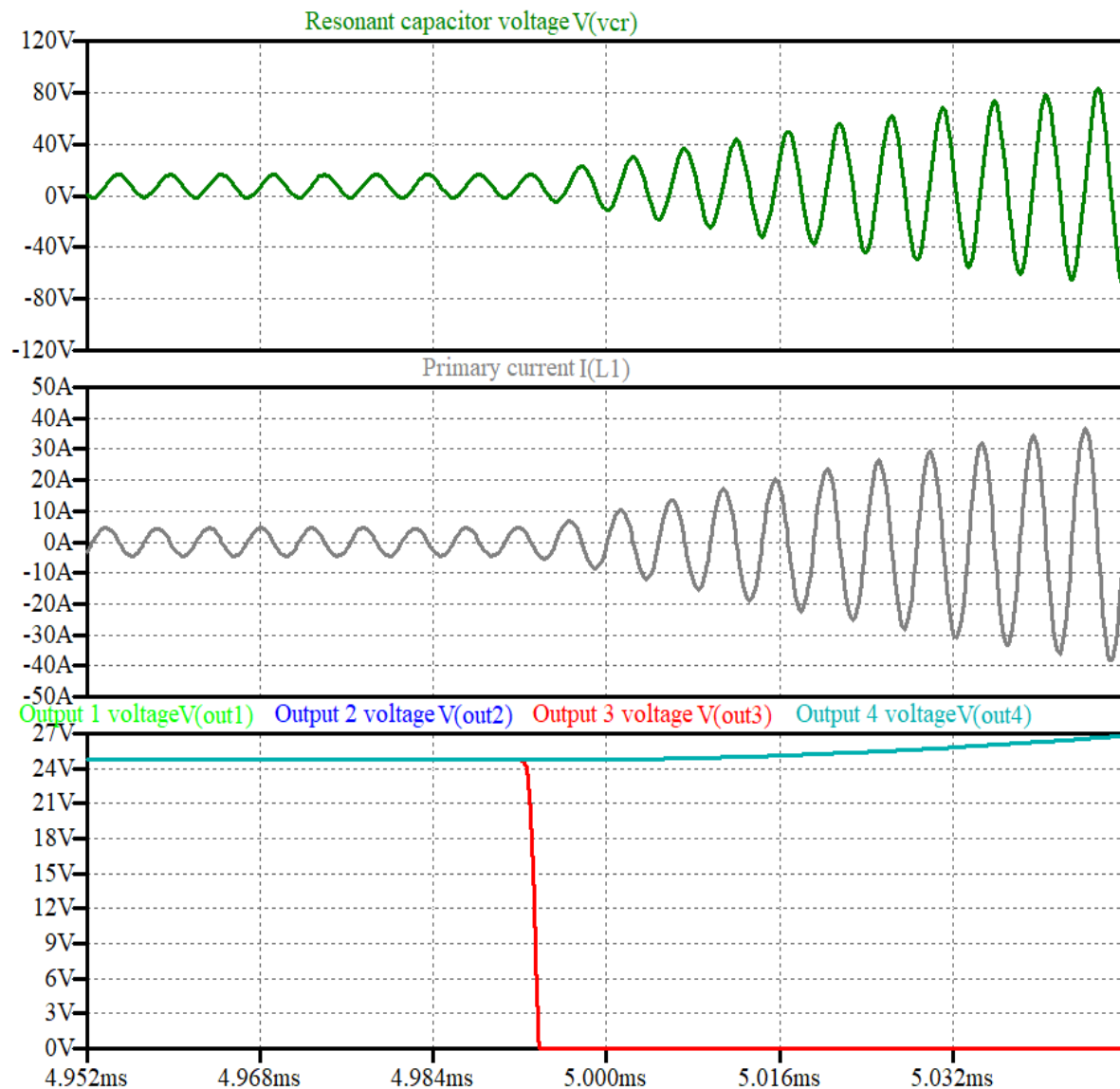


Figure 3.9. Short circuits happen at 4.99 ms when output power is 7.5W.	44
Figure 3.10. Short circuits happen at 4.99 ms when output power is 2.5 W.	46
Figure 3.11. Output 3 voltage ramps up to 40 V during open circuit fault at 4.99 ms.	47
Figure 3.12. Series LLC APS test setup.	48
Figure 3.13. Series LLC APS primary side waveforms are still stable during short circuit.....	49
Figure 3.14. Short circuit is cleared by secondary protection.....	49
Figure 3.15. Voltage is clamped during open circuit fault.	50
Figure 3.16. Toroidal core, U core and E core interwinding capacitance model in Ansys Maxwell.	52
Figure 3.17. APS unsuccessful startup due to overcurrent.	55

Figure 3.18. APS in hiccup mode before start up.	55
Figure 3.19. APS soft startup at low frequency, from top to bottom: primary side current (2A/div), switch node voltage (20V/div), primary output voltage (10V/div), secondary diode voltage (50V/div).	56
Figure 3.20. APS normal operation at designed frequency, from top to bottom: primary side current (2A/div), switch node voltage (20V/div), primary output voltage (10V/div), secondary diode voltage (50V/div).	56
Figure 3.21. Feedback resistance network of a flybuck converter.	58
Figure 3.22. Flybuck model with CM propagation.	59
Figure 3.23. Feedback voltage changes monotonically with primary current.	60
Figure 3.24. CM current causes feedback voltage spikes.	62
Figure 4.1. Wolfspeed XHV-9 10 kV 100A SiC MOSFET power module.	64
Figure 4.2. Forward conduction curves of the 10 kV SiC MOSFET module at 25°C.	65
Figure 4.3. Forward conduction curves of the 10 kV SiC MOSFET module at 125°C.	65
Figure 4.4. ON-resistance of the 10 kV SiC MOSFET module at different temperatures.	66
Figure 4.5. Threshold voltage decreases with increasing temperature in the 10 kV SiC MOSFET module.	68
Figure 4.6. Reverse conduction curves at 25°C of the 10 kV SiC MOSFET module.	68
Figure 4.7. Transfer characteristics of the 10 kV SiC MOSFET module at different temperatures.	69
Figure 4.8. Transconductance of the 10 kV SiC MOSFET module at different temperatures.	69
Figure 4.9. DPT circuit scheme for testing 10 kV SiC MOSFET module.	70
Figure 4.10. DPT experiment setup.	70
Figure 4.11. Turn on switching transient at 6.5 kV 57 A in 10 kV SiC MOSFET module.	72
Figure 4.12. t_{don} , t_{cr} , t_{vf} decreases with increasing temperature in 10 kV SiC MOSFET module.	74
Figure 4.13. Turn off delay time at $R_g = 5 \Omega$ is similar at different temperatures in 10 kV SiC MOSFET module.	74
Figure 4.14. Voltage rise time at $R_g = 5 \Omega$ is similar at different temperatures in 10 kV SiC MOSFET module.	75
Figure 4.15. Voltage overshoot at different temperatures in 10 kV SiC MOSFET module.	76

Figure 4.16. tdon turn on delay time is independent of current in 10 kV SiC MOSFET module.79

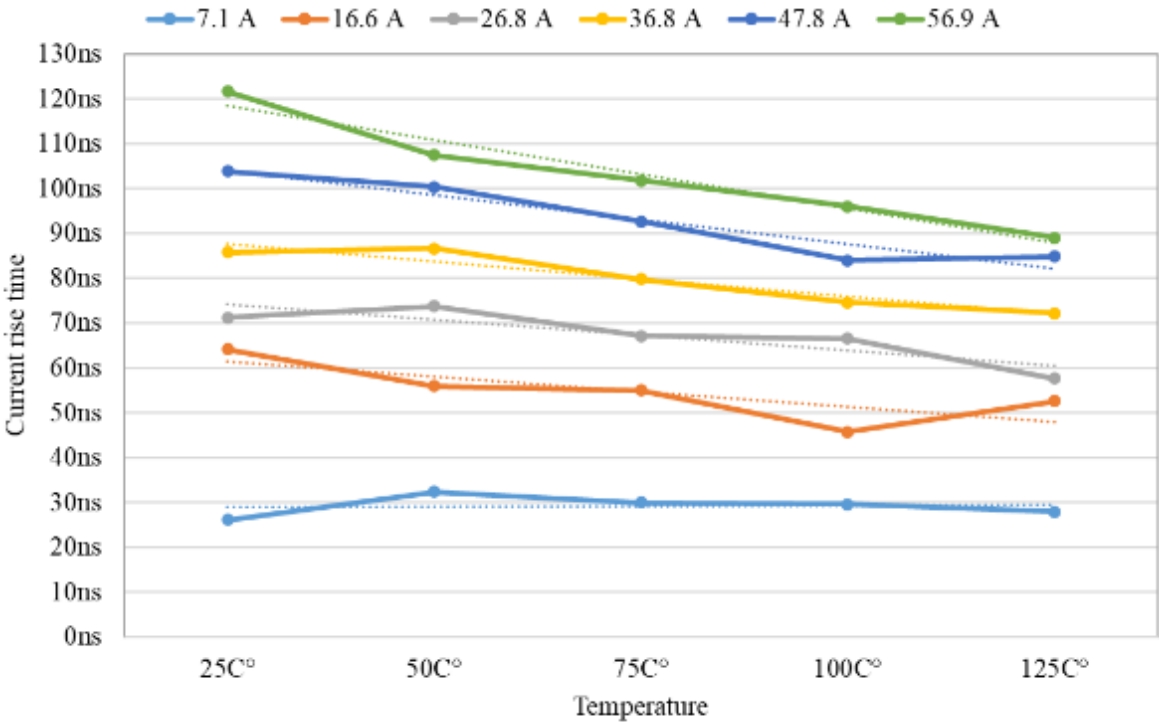


Figure 4.17. tcr current rise time increases with higher current in 10 kV SiC MOSFET module..... 79

Figure 4.18. tvf voltage fall time decreases with higher current in 10 kV SiC MOSFET module. 80

Figure 4.19. DPT circuit model with parasitics highlighted..... 81

Figure 4.20. Larger Lgs leads to higher current overshoot during turn on transient. 82

Figure 4.21. Lloop slows down voltage drop time during turn on transient. 83

Figure 4.22. Larger Cbp increases the voltage drop time during turn on transient. 85

Figure 4.23. di/dt increase with temperature measured at 6.5 kV 57 A. 89

Figure 4.24. Over-temperature protection circuit based on sensing turn on di/dt. 89

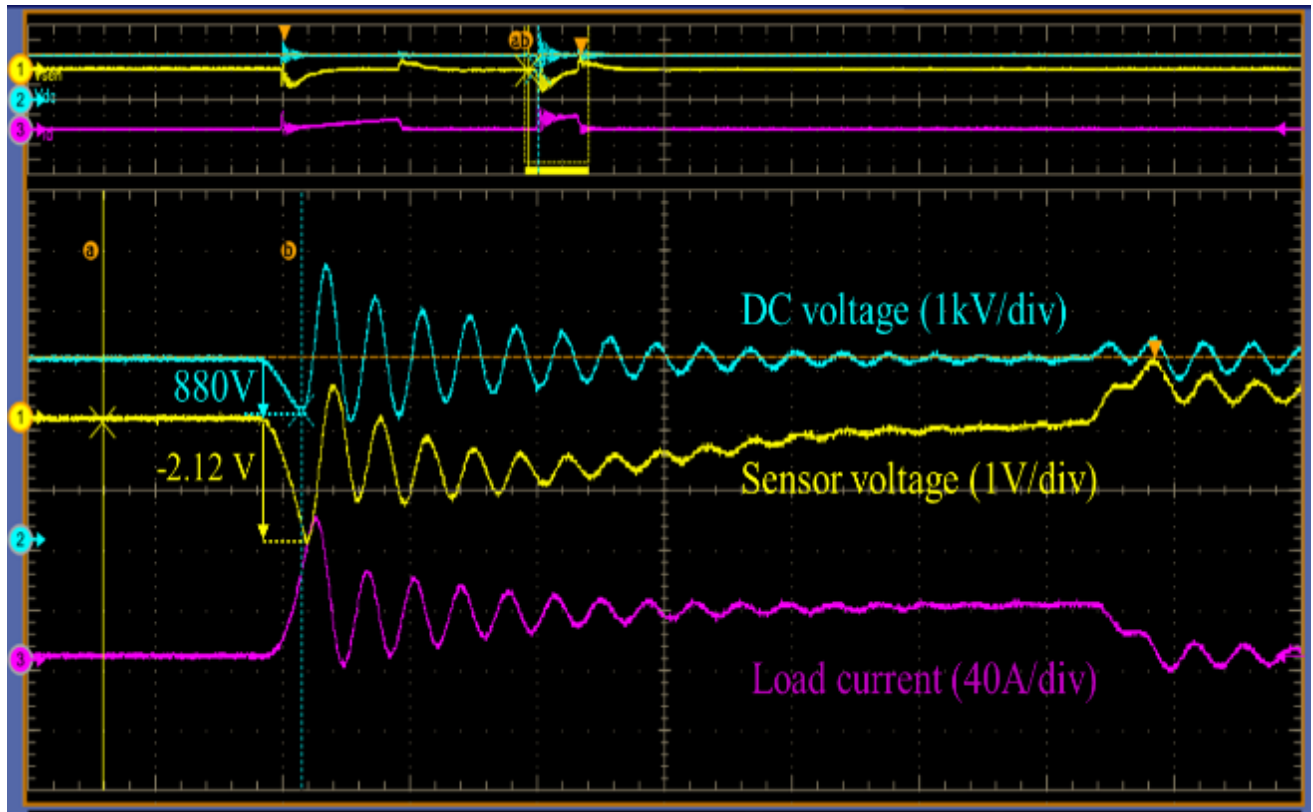


Figure 4.25. DC voltage undershoot and sensor voltage measurements during turn on at 25°C.	91
Figure 4.26. Experiment setup for TSEP calibration under different temperatures.	91
Figure 4.27. Voltage undershoot increases with higher temperature.....	92
Figure 4.28. Voltage undershoot increases linearly with higher temperature.	92
Figure 4.29. Sensor voltage increases with higher temperature.	93
Figure 4.30. Over-temperature protection triggered at 100 °C.....	93
Figure 5.1. 5-level MMC phase leg.	96

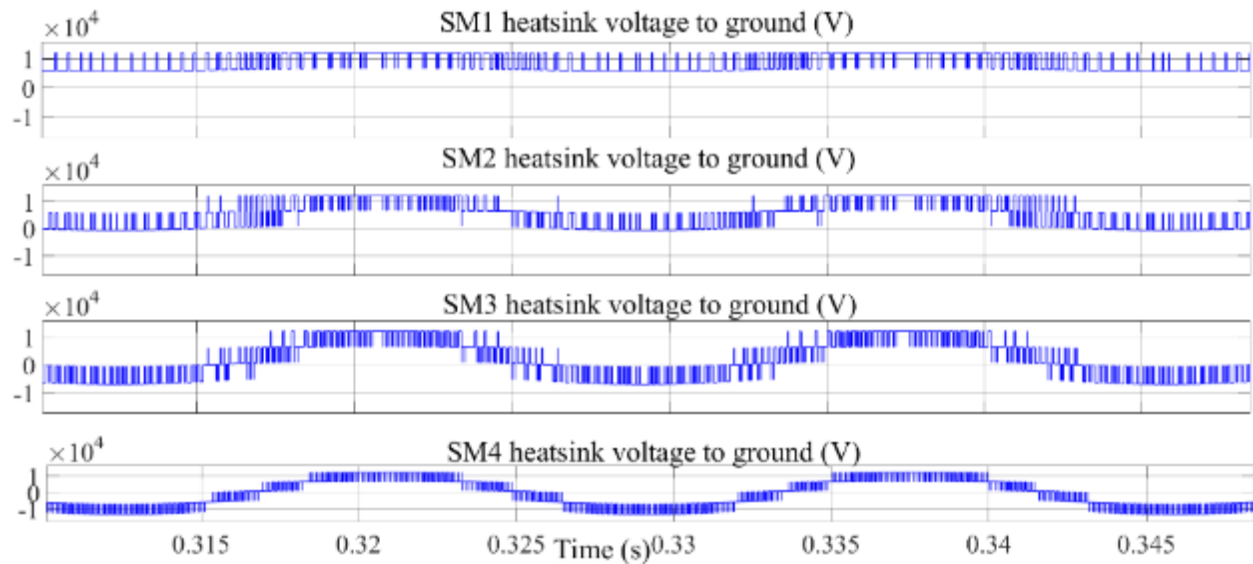


Figure 5.2. Heatsink voltage to ground of upper arm submodules.....	98
Figure 5.3. Voltage difference between adjacent heatsinks from SM1 to SM4 from top to bottom.	99
Figure 5.4. Electric field distribution at different voltages.....	99
Figure 5.5. Electric field simulation of air-cooling system.	101
Figure 5.6. Magnified view of the electric field of the heatsink.....	101
Figure 5.7. Design flowchart of liquid cooling.....	105
Figure 5.8. Power module model in Icepak.....	108
Figure 5.9. Thermal simulation of SiC power module mounted on air-cooled heatsink in Ansys Icepak.....	110
Figure 5.10. Airduct design procedure.	111
Figure 5.11. Multiple T-shape air duct top view.	112
Figure 5.12. Narrowing width slanted airduct top view and front view.....	113
Figure 5.13. Air flow distribution of slanted air duct.	118
Figure 5.14. Temperature distribution of the power module.....	119
Figure 5.15. Air velocity of straight air duct with heatsinks.	120
Figure 5.16. Heatsink temperature distribution.	121
Figure 5.17. Air temperature across the duct.....	121
Figure 5.18. Air flow velocity measurement locations.....	122
Figure 5.19. Flow rate measurement position at one cross-section.	123

Figure 5.20. Submodule testing with heatsink.....	125
Figure 5.21. Heatsink temperature measured	126
Figure 5.22. Single submodule testing with cold plate and chiller.....	127
Figure 5.23. MMC phase leg test setup.	129
Figure 5.24. MMC test waveforms from top to bottom: upper arm current (20A/div); lower arm current (20A/div); output current (40A/div); PWM voltage (4kV/div); output voltage (4kV/div).....	130
Figure 6.1. 8-level flying capacitor converter schematic.....	132
Figure 6.2. All seven upper devices drain source voltage is within 4 kV limit.	134
Figure 6.3. Voltage ripple values of flying capacitor voltage 7-1 are 427V, 499 V, 394V, 589V, 458V, 325V, 180V, respectively.....	135
Figure 6.4. Harmonic current percentage when filter inductance is 2.5 mH.	137
Figure 6.5. Forward conduction curves of ten 10 kV SiC MOSFET power modules when $V_{gs}=15$ V.....	138
Figure 6.6. Forward conduction curves of ten 10 kV SiC MOSFET power modules when $V_{gs}=10$ V.....	138
Figure 6.7. Transfer conduction curves of ten 10 kV SiC MOSFET power modules.....	138
Figure 6.8. Current sensor output frequency vs current.....	140
Figure 6.9. Voltage sensor diagram.	141
Figure 6.10. Voltage sensor output frequency vs input sampling voltage.....	142
Figure 6.11. Power module with gate driver and heatsink.	143
Figure 6.12. FCC phase leg layout first layer.	145
Figure 6.13. FCC phase leg layout second layer.	146
Figure 6.14. 8-level FCC dimensions.	147
Figure 6.15. FCC test setup.....	148
Figure 6.16. Voltage sensor signals 1-7 D0-D6 are interrupted.	149
Figure 6.17. The controller moved away from the converter cabinet.....	150
Figure 6.18. 8-level FCC test waveforms at 20 kV, from top to bottom: output current (5A/div), DC+ voltage (5kV/div), output PWM voltage (5kV/div), output voltage (5kV/div), DC- voltage (5kV/div), lowest stage flying capacitor voltage (5kV/div).....	151
Figure 7.1. Wolfspeed module vs Powerex module.	153

Figure 7.2. Powerex module Id-Vds curve at 25°C.....	155
Figure 7.3. Wolfspeed module Id-Vds curve at 25°C.	155
Figure 7.4. Output capacitance comparison between Powerex and Wolfspeed SiC modules....	156
Figure 7.5. Gate-drain capacitance comparison between Powerex and Wolfspeed SiC modules.	157
Figure 7.6. Gate-source capacitance comparison between Powerex and Wolfspeed SiC modules.	158
Figure 7.7. 5-level FCC decoupling capacitor before potting and after potting.	163
Figure 7.8. 5-level FCC phase leg for 1 MW converter (24 kV dc link, 13.8 kV line-line ac)..	163
Figure 7.9. 5-level FCC test setup.	165
Figure 7.10. Voltage sensor feedback signal D0-D3 all interrupted.....	166
Figure 7.11. Waveforms in a 5-level FCC at 12 kV dc link voltage illustrating the transition from voltage balancing stage to gate signal activation.	168
Figure 7.12. 3 rd stage flying capacitor voltage ripple at 10 kV dc link voltage.....	168
Figure 7.13. Gate PWM signal spikes at 20 kV dc voltage.	169
Figure 7.14. Gate PWM signals are clean at 22 kV after measures implemented.....	171
Figure 7.15. 2 nd stage voltage sensor is shielded.	171
Figure 7.16. Waveforms at 24 kV dc link voltage from top to bottom: output PWM voltage (5kV/div), DC+ voltage (5kV/div), DC- voltage (5kV/div), output current (50A/div).....	172

List of Abbreviations

APS	Auxiliary power supply
CFD	Computation fluid dynamics
CM	Common mode
DBC	Direct bonded copper
DPT	Double pulse test
EMI	Electromagnetic interference
FCC	Flying capacitor converter
GaN	Gallium nitride
Hipot	High potential
IC	Integrated circuit
MLC	Microchannel liquid cooling
MMC	Modular multilevel converter
MV	Medium voltage
PCB	Printed circuit board
PD	Partial discharge
SiC	Silicon carbide
SST	Solid state transformer
TSEP	Temperature sensitive electrical parameter

Chapter 1 Introduction

This chapter discusses the background of wide bandgap (WBG) devices, especially the challenges in the medium voltage application of 10 kV SiC devices.

1.1 Wide Bandgap Semiconductors

WBG semiconductors are materials such as SiC (Silicon Carbide) and GaN (Gallium Nitride) whose bandgap energy is significantly greater than that of silicon. SiC has been popular to replace Si in medium voltage applications because of the following three benefits: 1) SiC has a ten times higher critical electric field, which enables high voltage application; 2) The high electron saturation velocity in SiC leads to lower switching loss and faster switching speed; 3) The thermal conductivity of SiC is also superior to Si, which offers high temperature operation.

These capabilities reduce weight, volume, and life-cycle costs in a wide range of power applications. For example, 1) they can benefit electric vehicles by reducing electricity loss in driving and battery charging; 2) WBG devices enable higher efficiency and more compact drives in industrial motors; 3) WBG-based inverters that interface solar and wind energy with the grid can be more efficient due to less device loss [1].

Overall, in many ways, harnessing WBG devices contributes to dramatic energy savings in manufacturing electronics, accelerates the widespread use of electric vehicles, and promotes renewable energy integration into the grid [2].

1.2 Medium Voltage Application of WBG Devices

WBG devices have been extensively applied in medium voltage systems; the three most common grid applications of WBG devices are introduced as follows:

Solid-state transformer (SST): it is promising in replacing inverters and high-power line frequency step-up transformers in photovoltaic power generation plants with integrated battery energy storage [3], [4], [5], [6]. The SST involves cascading multiple low-voltage cells to achieve the targeted voltage [5], [7], [8], [9], offering advantages such as active and reactive power flow control and voltage balancing [10], [11], [12]. Implementing high voltage WBG devices can reduce the number of cells, making the SST more reliable and efficient.

Power conditioning system (PCS): for asynchronous microgrids, PCS can provide multiple benefits like under-voltage and under-frequency ride-through capability, smooth transition between grid-connected and islanded modes, unbalanced load support, and isolation of faults

[13], [14], [15], [16], [17], [18]. Implementing WBG devices can promote these features as they offer higher control bandwidth due to faster switching frequency.

Solid-state circuit breaker: it can protect electric equipment from overcurrent and short circuit events. Implementing WBG devices can boost response time, lower switching losses, and increase efficiency compared to conventional Si devices [19], [20], [21], [22].

1.3 Challenges of Medium Voltage Applications

While SiC devices exhibit superior breakdown voltage, faster switching speed, and higher operating temperature, the design of medium voltage hardware using these devices poses several challenges. These include the need for high voltage isolation, robust electromagnetic interference (EMI) resilience, and sufficient cooling [3], [6], [23], [24], [25]. These challenges are discussed in detail as follows [26], [27], [28].

1.3.1 Challenges in High Voltage Isolation

When a SiC device is utilized in higher voltage scenarios, the demand for higher voltage insulation extends to other crucial components within the system, including the auxiliary power supply (APS) and the cooling system [29], [30], [31], [32].

As the voltage excitation is often a high frequency pulse width modulation (PWM) waveform, the insulation material degrades faster under the high voltage change at a high frequency. Also, the faster switching transient causes a higher voltage slew rate, which wears down the insulation more rapidly than conventional applications with a mild voltage slew rate. This requires more reliable insulation on the APS and cooling system to withstand long-term high voltage stress.

APS is connected to the gate driver ground which is a high voltage floating reference. Many commercial APS solutions currently available in the market provide insulation levels that fall short of the demands posed by medium voltage (MV) applications, which frequently exceed 10 kV. Ensuring electrical isolation under such conditions requires substantial creepage and clearance distances. This presents a significant design challenge, as APS is typically intended to be compact in order to reduce the overall size of the converter. The trade-off between insulation performance and size becomes critical in multilevel architectures, where the number of APS units scales with the number of levels, further constraining insulation design.

With air cooling, the heatsink voltage affects the electric field distribution in the power module. To ensure the insulation integrity of the power module, the heatsink is recommended to be connected to the source of power module, which is a floating high voltage. Thus, the

insulation must be carefully designed between heatsink and adjacent electrical components, between heatsinks at different voltage levels, and between heatsink and low voltage fan [14] [15].

1.3.2 Challenges in EMI Tolerance

SiC devices present formidable EMI challenges, primarily stemming from their rapid rate of change of voltage (dv/dt), which can exceed 100 V/ns during switching transients. Managing conductive EMI emanating through the gate driver and APS poses a significant hurdle, as their propagation path is complicated due to multiple coupling paths within the system. It is challenging to accurately model or measure the total coupling capacitance, especially the interwinding capacitance between the primary side and the secondary side of APS.

To mitigate the common mode (CM) current flowing from the secondary to the primary side of APS, many efforts have been made to minimize interwinding capacitance. Researchers have streamlined transformer structures, simplifying them to a basic capacitance model to reduce the capacitance to less than 5 pF. However, the designs are dedicated to specific transformer configurations. There lacks a common method that compares the interwinding capacitance between different core shapes to guide the selection of the core in the initial stage. Thus, it is valuable to investigate how the core shape influences the capacitance given the same winding condition.

1.3.3 Challenges in Thermal Management

While SiC devices are known for their higher operational temperatures, their relatively small die size renders them more susceptible to thermal runaway issues. Unlike low voltage (LV) power modules, thermistors are generally not packaged near the die or on the substrate in 10 kV power modules for temperature monitoring, due to the risk of dielectric breakdown under strong electric fields. To overcome this challenge, numerous research has been dedicated to identifying temperature sensitive electrical parameters (TSEPs). These parameters serve as valuable indicators of temperature variations during either static or dynamic switching state. They can provide a fast response without disrupting the normal operation of the device.

While TSEPs for low voltage SiC MOSFETs (1.2 kV, 1.7 kV) have been extensively studied, TSEPs for high voltage SiC MOSFETs (10 kV) have not been fully investigated. The variation in TSEPs between 1.2 kV / 1.7 kV SiC and 10 kV devices is primarily driven by differences in device architecture and fabrication processes necessary to support higher breakdown voltages.

Higher voltage SiC devices require more robust structural features, such as thicker drift regions, advanced edge termination designs, and increased overall device thickness to maintain effective voltage blocking. These structural improvements alter the device's thermal characteristics, resulting in distinct TSEP profiles compared to lower voltage counterparts. Therefore, it is beneficial to find suitable TSEP for 10 kV SiC MOSFET to prevent thermal runaway issues.

Another aspect of the thermal management is the cooling system that dissipates the heat from device conduction loss and switching loss. It becomes challenging in MV applications as the sheer amount of heat requires bulky heatsinks and cold plates, making it difficult to meet the power density requirement simultaneously.

Numerous studies have concentrated on optimizing shapes and sizes of individual cold plate and heatsink to achieve optimal cooling performance. However, in multilevel converter, the flow rate of the coolant or the air passing through multiple cold plates and heatsinks varies and affects the actual cooling performance. It is necessary to investigate potential methods of providing uniform flow rate to reduce hot spots in the system.

1.4 Dissertation Outline

This chapter offers an overview of the current state-of-the-art in implementing SiC devices in MV converters. It highlights key challenges in three critical design areas: high insulation voltage, EMI tolerance, and thermal management. The chapter also details how these challenges manifest in the APS and the cooling system.

Chapter 2 presents a comprehensive survey of the design and protection of APS, TSEP selection for high voltage SiC devices, and cooling design for MV converters.

Chapter 3 focuses on APS design considering voltage insulation and capacitance minimization. Protection methods on both the primary and secondary sides are compared.

Chapter 4 discusses TSEP selection based on static and dynamic tests, providing numerical expressions for estimating temperature linearity and demonstrating the impact of gate resistance and load current on temperature sensitivity for each potential TSEP. An over-temperature protection method is also proposed for 10 kV SiC MOSFET based on sensing turn on di/dt .

Chapter 5 establishes a cooling system design with a focus on high-voltage insulation, presenting liquid cooling design procedures regarding flow rate and pressure drop, and comparing air cooling designs of different types of airducts.

Chapter 6 details the design and testing procedures for an 8-level flying capacitor converter. This chapter focuses on component selection to achieve high voltage operation and limiting overvoltage on the power modules. The testing procedures provide a systematic approach in testing high voltage and high power converters.

Chapter 7 introduces a 5-level flying capacitor converter featuring a differently packaged 10 kV SiC power module. The packaging impact on the power module insulation and switching loss is investigated. At the converter level, methods of preventing overvoltage protection false triggering are presented.

Chapter 2 Literature Review

Utilizing SiC MOSFET in MV grid connected converter brings benefits of reduced component count, higher control bandwidth and lower power loss. At the same time, it brings challenges in converter design due to elevated operation voltage, strong EMI noises and thermal management. To tackle the first two challenges in APS, this literature review mainly focuses on: 1) different categories of APS based on their insulation requirements and common insulation techniques, 2) interwinding capacitance model to reduce CM current interference, 3) APS protection to ensure reliable operation during fault.

To tackle the third challenge, it is crucial to monitor the temperature of high voltage SiC MOSFET and prevent thermal runaway. Thus, common TSEPs and evaluation of 10 kV SiC MOSFET are reviewed. On the other hand, to dissipate heat effectively, liquid cooling, two phase cooling and air cooling are reviewed. Details are presented as follows.

2.1 Design and Protection of APS

2.1.1 Local APS and Centralized APS

Generally, two categories of APS, local APS and centralized APS, are implemented in MV multilevel converters. Local APS extracts energy from its local submodule DC bus, shown in **Figure 2.1**.

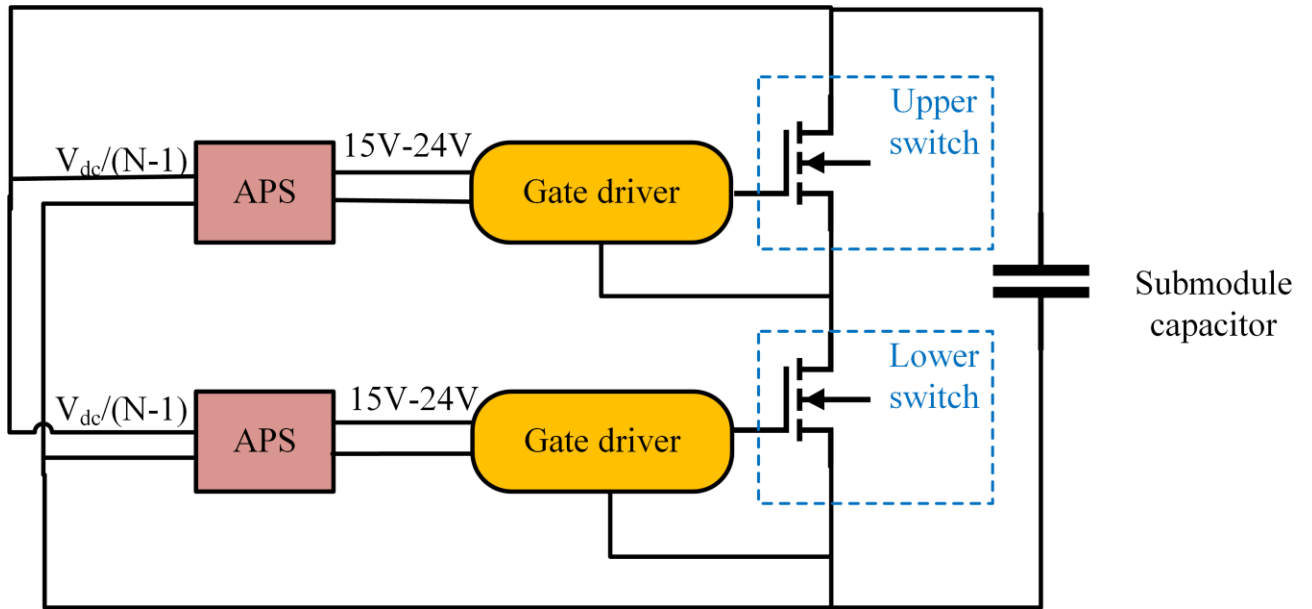


Figure 2.1. Local APS extracts power from submodule capacitor.

In this case, the input of APS is $\frac{V_{dc}}{N-1}$ considering an N level multilevel modular converter (MMC), where the DC link voltage is V_{dc} and the output is low voltage 15 V-24 V DC, which demands a high step-down voltage ratio and high voltage insulation between the primary side and the secondary side. In the centralized APS hierarchy, APS is powered from outside the converter at low voltage. The requirement on voltage ratio is relaxed, but compared to the local APS structure, the insulation requirement for the centralized structure is increased from the submodule DC voltage to the full converter DC voltage.

2.1.1.1 Local APS

When submodule dc link voltage is above 2 kV, to achieve a high step-down voltage ratio and tolerate high input voltage, three methods are often implemented in local APS: 1) input-series output-parallel (ISOP) dc-dc converters; 2) switched capacitor converters (SCC); 3) connecting low voltage devices in series.

The ISOP topology [33], [34], [35], [36], [37] reduces each converter module's input voltage rating within 1 kV, simplifying power device selection. However, challenges include the need for multiple transformers and numerous switching devices, resulting in a complex and bulky structure. Control issues like input capacitor voltage sharing and overvoltage protection pose additional challenges. Integrated transformers address these concerns but become more complicated with an increased number of series-connected modules [38], [39], [40].

SCC employs a capacitive voltage divider to handle high input voltages, allowing the output voltage to be drawn from a single capacitor [41], [42], [43], [44], [45], [46]. This eliminates the need for power devices with high voltage ratings. However, to ensure equal voltage sharing, auxiliary semiconductor devices and magnetic components must be connected between adjacent capacitors. Nevertheless, as the voltage level rises, the demand for power devices, clamping diodes, and flying capacitors increases significantly, resulting in control complexities. These drawbacks render multilevel converters less appealing in APS applications.

Connecting low voltage devices in series reduces the complexity of circuit structure and control. However, addressing dynamic voltage imbalance, resulting from unmatched gate driver and device parameters, becomes a new challenge [47], [48], [49], [50]. Faster turn-off or slower turn-on devices may experience higher transient voltage. Simple resistor-capacitor (RC) snubbers can achieve dynamic voltage balancing in APS but may lead to significant snubber

losses when optimal voltage sharing is required. Other methods like active delay time control, variable-speed gate drives [51], and closed-loop gate drives [52] are effective but involve costly and complex circuits, making them less appealing in APS applications [53].

Another challenge of local APS occurs during the initial power-up of the converter. This often includes sensing the input voltage and then starting to power up the APS primary side device gate driver with an additional DC/DC circuit once the input voltage reaches the threshold.

2.1.1.2 Centralized APS

In the centralized APS hierarchy, as shown in **Figure 2.2**, all APS inputs share a common energy source from the utility, which is often at low voltage. However, because the APS output is connected to the gate driver ground and the switching device floating source, the minimum insulation voltage for the centralized APS can be as high as the full DC voltage of the converter, which is significantly higher than local APS [54], [55], [56], [57].

2.1.1.3 Comparison Between Local APS and Centralized APS

A comprehensive comparison between local APS and centralized APS is conducted in this subsection.

Local APS is preferred in systems where the submodule DC-link voltage is below 3 kV, the number of submodules is high, and the total DC bus voltage is high. Within this range, insulation voltage requirements are moderate, making local APS cost-effective as listed in **Table 2-1**. However, for higher voltages, such as 6.5 kV submodule DC voltage for 10 kV SiC MOSFETs, local APS becomes less favorable. These include the need for a transformer with a much higher step-down ratio and insulation capability, which results in increased size and weight more than offset the benefit it brings.

To withstand 6.5 kV input voltage, series-stacking three 3.3 kV SiC or five 1.7 kV SiC becomes far more costly. Given the limitations of local APS, centralized APS, as illustrated in **Table 2-2**, is a more practical and reliable approach for 10 kV SiC MOSFET-based converters.

In summary, local APS is preferred in systems where the submodule DC-link voltage is below 3 kV, the number of submodules is high, and the total DC bus voltage is high, as typically seen in high-voltage direct current (HVDC) applications. Conversely, centralized APS is more suitable for medium-voltage applications with submodule DC-link voltages above 3 kV, fewer submodules, and a relatively low DC voltage.

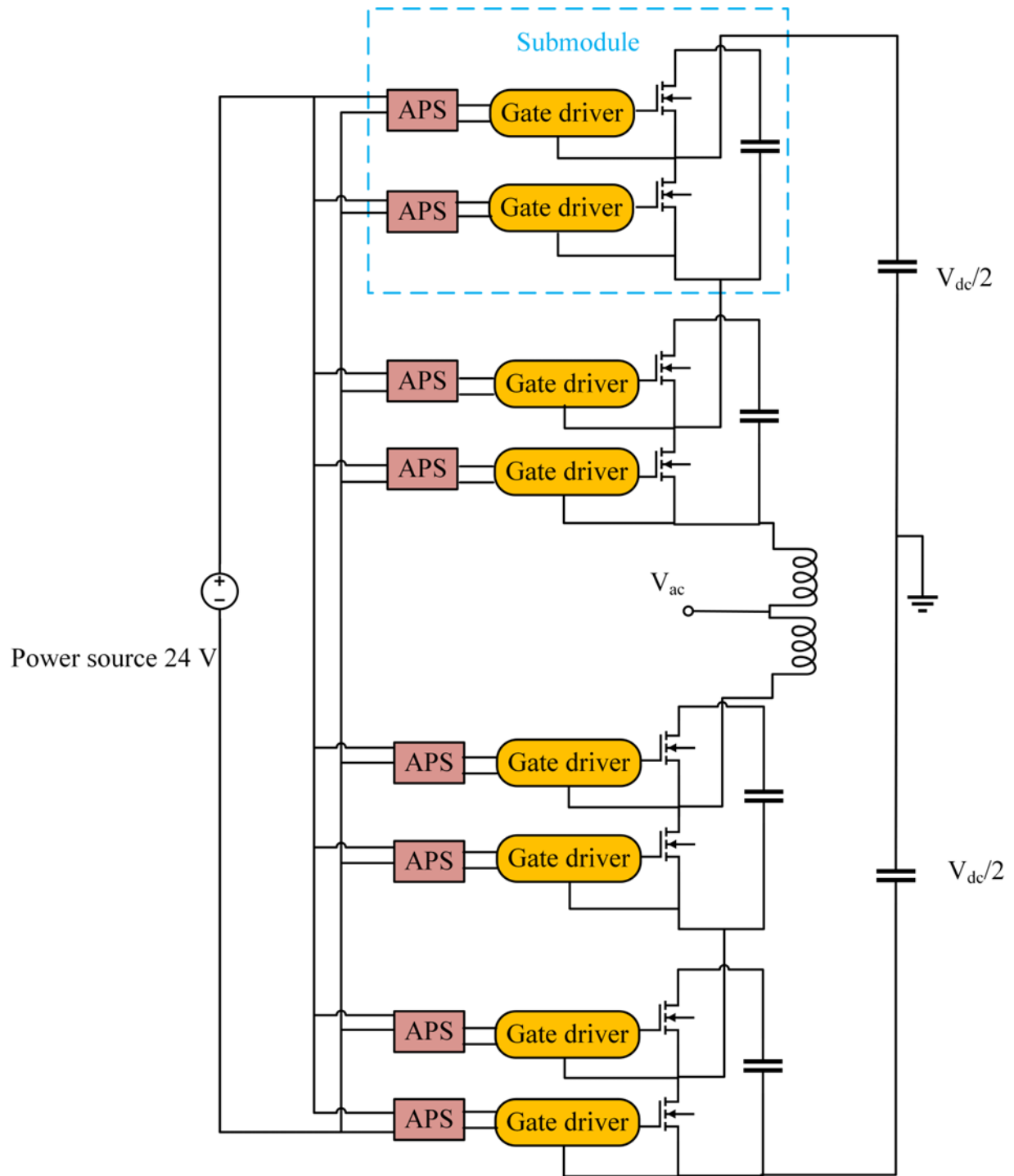


Figure 2.2. Centralized APS is powered by an external power source.

Table 2-1 Typical local APS operation voltage range, power rating and topology comparison.

Reference	Input voltage	Output voltage	Power rating	Topology	Device
[58]	200-900V	15 V	20 W	Flyback	1.5 kV/2 A 2SK4177 MOSFET
[59]	230-1300V	48 V	80 W	Two switch flyback	1.7 kV MOSFET
[60]	2800V	36 V	100 W	ISOP 3 stage flyback	NA

Table 2-2 Centralized APS ratings, insulation performance and topology comparison.

Reference	Output voltage	Power rating	Partial discharge inception voltage	Topology	Coupling capacitance
[61]	NA	1.67 W	16.4 kV	Resonant flyback	5.85 pF
[62]	24 V	20 W per output	15 kV	LCCL-LC	3.6 pF
[57]	24 V	2.5 W	15 kV	Flybuck	1.03 pF

2.1.2 Insulation Design

Insulation design is a major part in the APS design process for MV applications. Usually, higher than 10 kV insulation is required from the primary side to the secondary side. There are three common methods to meet this stringent standard: magnetic isolation [63], wireless power transfer [65], and optical fiber transfer [65].

The most common method of achieving insulation is using the isolation transformer. The insulation between the transformer primary and secondary windings is often improved by materials with high dielectric strength, such as air, Kapton tape, and silicone gel or epoxy [66]. When using air as the sole insulation, creepage and clearance distances are often designed according to the standard UL 60950 [67].

Kapton tape offers insulation up to 10 kV, but the air trapped between layers makes it difficult to achieve higher partial discharge (PD) free performance [68]. Silicone gel and epoxy are promising candidates that encapsulate the windings and the cores with a vacuum pressure potting (VPP) procedure to extract the air and impurities from the material. The PD test can measure up to 20 kV. The thermal properties of these materials should also be considered so that heat from the transformer can be dissipated effectively [69]. For a planar transformer with PCB windings, the insulation between copper layers is strengthened by high voltage FR4 materials [70].

The second method is wireless power transfer, which naturally provides high insulation voltage because the inductive coils are separated at a distance. The transmitter coils and receiver coils are placed face to face with an air gap in the middle. To reduce the air gap distance, high insulation voltage material Arlon 85N is used to replace air and fabricated together with the PCB coils [71], which is similar to a planar transformer.

The third method is using optical fiber transfer. The gate driver power is supplied by a laser light, which is transmitted through an optical fiber to the gate driver. It has negligible interwinding capacitance and provides a small weight and compact APS design. However, the power transmitted is limited to 0.5 W, and the laser emitter is relatively expensive compared with the other two methods [72]. It would not be cost-effective to use multiple laser emitters to power many submodules in an MV converter.

The insulation design involves electric field simulation in Ansys Maxwell to examine the weak point that experiences the highest electric field. The process starts by drawing real-size windings and cores in the model. Then the insulation material between them is assigned with

specific relative permittivity and dielectric strength. If the highest electric field strength in the model is within the dielectric strength of the material with some margins, the insulation is often considered adequate [73].

Still, the insulation can be further verified by hipot test to check if the leakage current becomes substantial under the rated voltage. In some literature, partial discharge (PD) test is also used to examine the insulation degradation and reliability [74].

2.1.3 EMI Tolerance

The voltage slew rate of the 3rd generation 10 kV SiC MOSFET can reach 100 V/ns, which acts as an CM voltage source, and generates a CM current i_{cm} through the APS interwinding capacitance between the primary side and the secondary side. The CM model of a half bridge is shown in **Figure 2.3**. The APS primary side ground is referenced to the ground. Z_1 represents APS primary impedance, Z_2 represents APS secondary impedance, and C_{ps} represents the interwinding capacitance between the two sides.

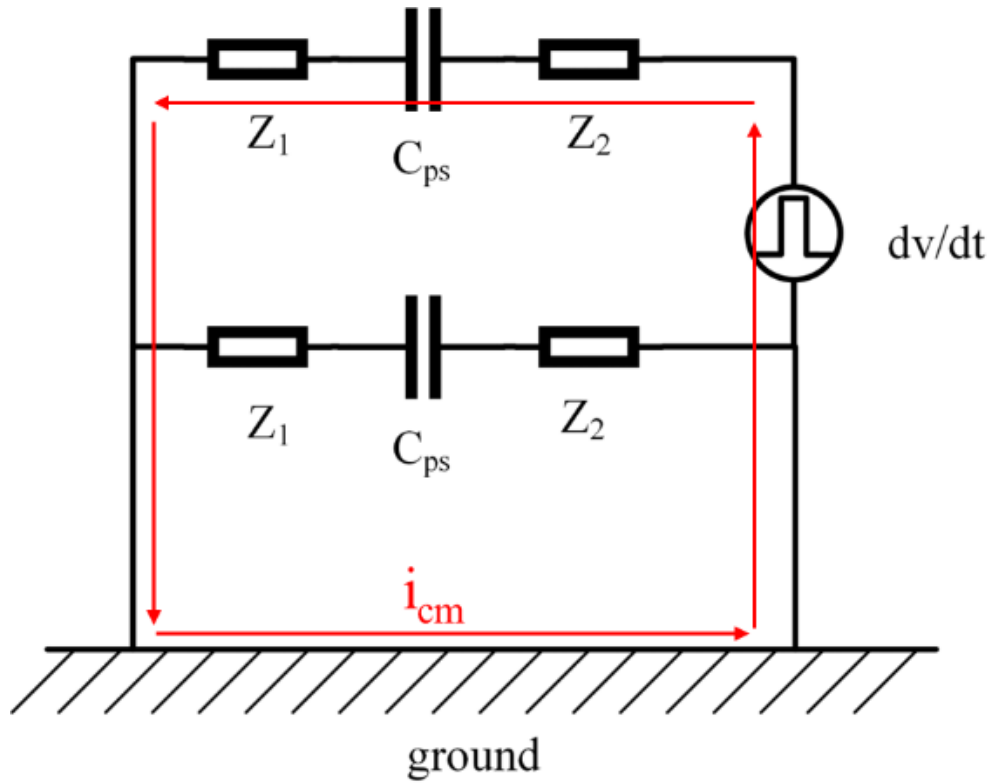


Figure 2.3 APS grounding scheme.

It can be explained under the assumption of 100 V/ns slew rate and 50 ns transient time; 500 mA common mode (CM) current is produced for a 5 pF interwinding capacitance due to Cdv/dt . At $0.35/(50 \text{ ns})=7 \text{ MHz}$, this current would cause 0.44 V voltage peak if 20 nH ground plane inductance is assumed [75]. This threatens the sensitive analog and digital signal processing circuit, which undermines the gate driver reliability [76]. Thus, most designs strive to achieve a less than 5 pF interwinding capacitance to reduce the high dv/dt impact.

The real CM conduction path can be more complicated as there are multiple sources of dv/dt [77]. To mitigate this issue, the switching speed of the device can be reduced, but this brings higher switching loss and lower efficiency. Another method is to increase the impedance in the CM loop by adding CM chokes. It may not be effective as the propagation path is unclear. Thus, the most common approach is to minimize the interwinding capacitance of the APS. Existing work has sought to simplify the interwinding capacitance to simple geometry for optimization.

The transformer-based APS, discussed in this paper, can at best reduce the interwinding capacitance to less than 2 pF [78]. Several structures are presented as state-of-the-art.

One is the toroidal core structure with a single primary turn situated in the middle [62], [79], [80], [81], where the interwinding capacitance can be simplified and modeled as a cylindrical capacitance between the primary copper cable and core shown **Figure 2.4**. The capacitance is given by (2.1).

$$C_{ps} = 2\pi\epsilon_0 h \left(\frac{\ln\left(\frac{r_{core}}{r_{iso}}\right)}{\epsilon_r} + \frac{\ln\left(\frac{r_{iso}}{r_{cond}}\right)}{\epsilon_{iso}} \right)^{-1} \quad (2.1)$$

where ϵ_r is the relative permittivity of material between the core and wire, and ϵ_{iso} is relative permittivity of the cable insulation. Another method of achieving a low interwinding capacitance with good standardization is using a PCB winding around a C core shown **Figure 2.5**.

The total interwinding capacitance is made of three parts, total capacitance from primary winding to core C_{pc} , total capacitance from secondary winding to core C_{sc} , and primary to secondary winding capacitance C_{ps} as presented in (2.2). The first two parts are in series and then in parallel with the third one. Each part of the capacitance can be adjusted by the PCB trace length, trace height and PCB trace to core distance [56].

$$C_{ps} = (C_{pc} \times C_{sc}) / (C_{pc} + C_{sc}) + C_{ps} \quad (2.2)$$

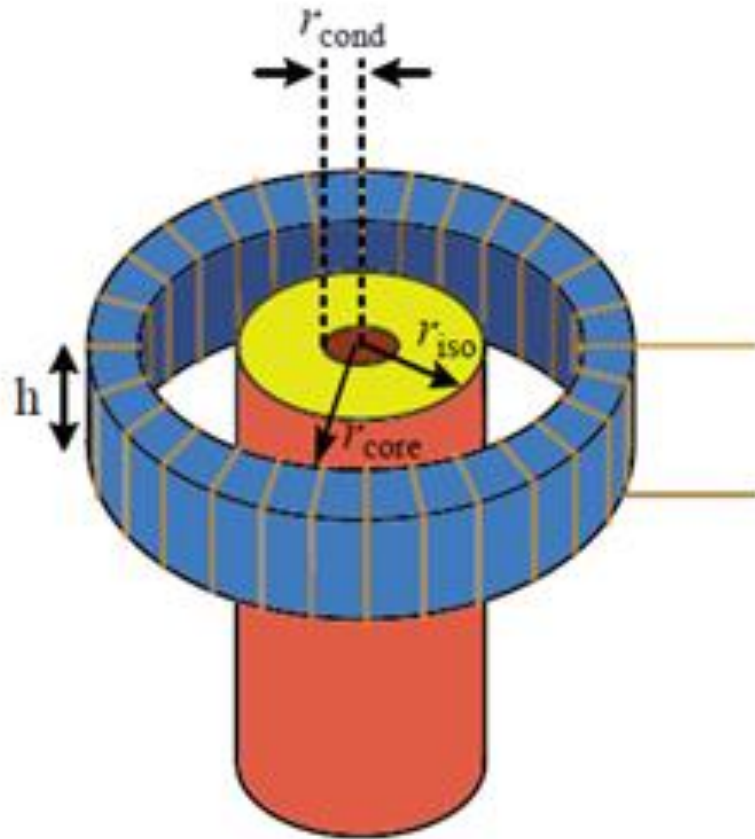


Figure 2.4. Cylindrical capacitance between windings of a toroidal core [62].

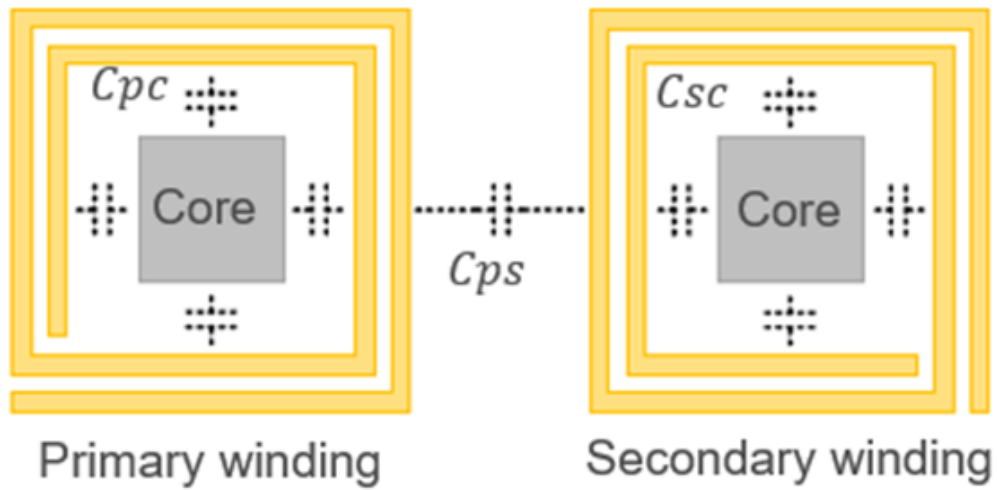


Figure 2.5. PCB winding to core capacitance distribution [56].

The third design of minimizing interwinding capacitance is using two E cores facing each other, separated at a distance as shown in **Figure 2.6**. This design models the two parallel plate capacitance which can be adjusted by the area of two cores facing each other, the distance between the two plates, and material relative permittivity [99].

In some cases, an impedance analyzer can measure the interwinding capacitance to verify the design. The APS can also be tested with the gate driver and power device. By measuring the CM current i_{cm} of the APS during device switching transients, the interwinding capacitance C_{ps} can be calculated by $C_{ps} = i_{cm} / \frac{dv}{dt}$, where dv/dt is the voltage slew rate.

2.1.4 APS Protection

Commercial isolated DC-DC APS, such as the PRC10W, incorporate basic protection mechanisms including Zener clamps for overvoltage protection, hiccup mode for overcurrent protection, and auto-recovery for short circuits. Similarly, single-input single-output APS employing primary-side regulated flyback or flybuck topologies feature integrated overcurrent and overvoltage protection. These topologies inherently contain faults within a single output, ensuring that failures do not affect other subsystems.

However, in single-input, multi-output APS, protection design is significantly more challenging. Since multiple outputs share a common power stage, a fault at one output can destabilize the voltages of all outputs simultaneously, making conventional protection schemes ineffective. This interdependence necessitates advanced fault isolation techniques to maintain stable operation across all outputs.

Some resonant topologies exhibit inherent fault tolerance. For instance, the LCCL-LC topology offers a degree of fault isolation because its current transformer-like behavior ensures that output voltage remains independent of load resistance, because of secondary resonant compensation [109]. However, its applicability in high-voltage auxiliary power supplies remains an area of further investigation.

Conversely, the widely adopted LLC series-connected converter presents a major challenge: it is highly susceptible to hazardous overvoltage at the output under open-circuit fault conditions [11]. One approach to mitigate this issue involves adding a bleeder resistor at the output [12], but this method reduces efficiency and fails to address output voltage dynamics under short-circuit conditions. Another study [111] proposes hysteresis-based protection, yet no experiment

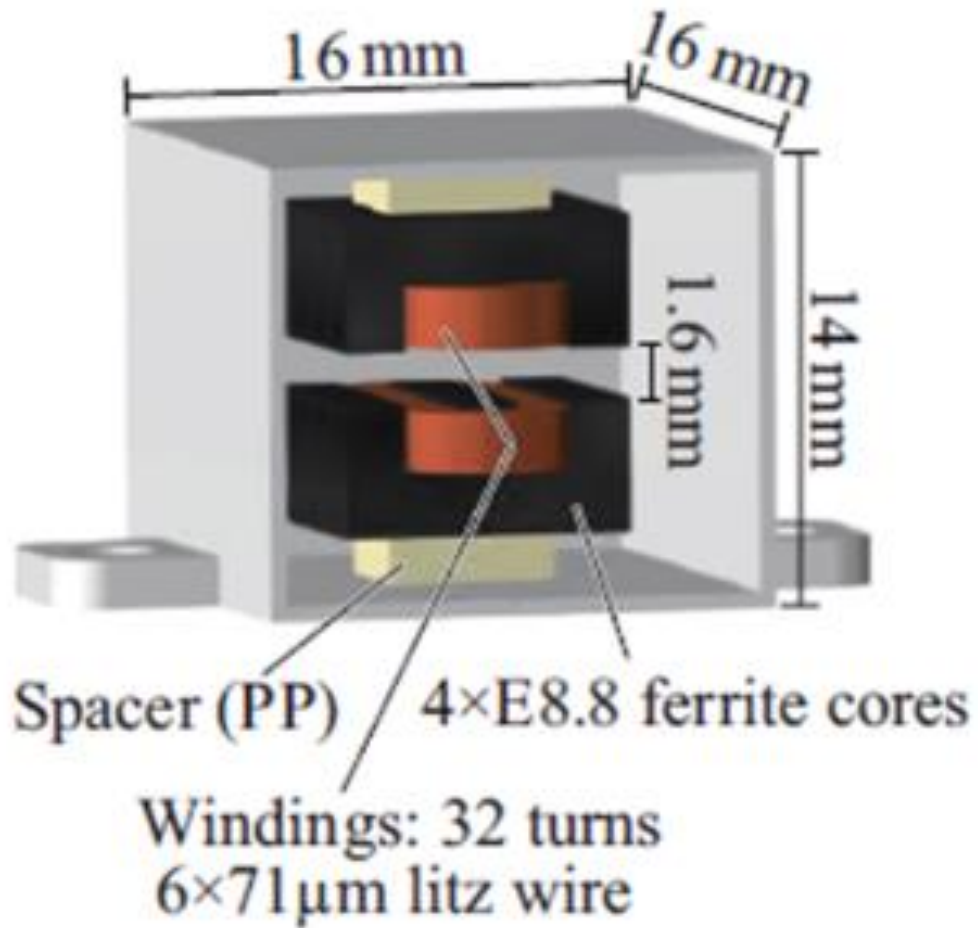


Figure 2.6. Planar capacitance between two E cores [69].

validation under fault conditions is provided, leaving a critical research gap in developing an effective fault protection scheme for series LLC converters.

Given these challenges, the design of fault-tolerant multi-output APS requires a novel protection approach that can effectively isolate faulty outputs while ensuring stable operation for the remaining outputs. Future research will focus on developing and testing robust protection mechanisms tailored to series LLC topologies, aiming to enhance fault isolation and system reliability.

2.2 TSEP Selection for 10 kV SiC MOSFET

Excessive heat is a major cause for device degradation and failure. Therefore, to protect switching devices from overheating, junction temperature monitoring is crucial in health management. TSEP is a popular method because it is easily measurable and offers a fast response. It can monitor the device online with a certain level of precision and not interfere with the normal operation of the device.

TSEPs are divided into two types: static TSEPs and dynamic TSEPs. Static TSEPs refer to the parameters that can be measured during conduction stage, such as ON-state resistance. Usually, device characterization under different temperatures can be done with a curve tracer, a hotplate and a temperature sensor. By doing the forward conduction characterization, the ON-state resistance can be calculated under a given gate voltage at different temperatures. Transfer characteristics investigate the relation between drain current and gate voltage, where transconductance can be extracted to determine its temperature dependency. This parameter also helps us to understand the impact of temperature on switching transients.

Dynamic TSEPs are parameters from switching transients, for example turn on delay time, current rise time and voltage fall time during turn on. At a given current, the current rise time is inversely proportional to the current slew rate. Thus, if one of these parameters is temperature sensitive, then the other one is also temperature sensitive. The same assumptions go with voltage fall time and voltage slew rate. In the same manner, during the turn off transient, turn off delay time, current fall time and voltage rise time are often examined for selection of TSEPs.

2.2.1 TSEP of Low Voltage Devices

TSEP is widely discussed in 1200 V IGBT power modules [82], [83]. On-state voltage of the IGBT is often utilized as TSEP, but it can be intrusive on the hardware to measure. Also, it shows a low resolution of a few millivolts per Celsius. In [84], turn off di/dt is used as a TSEP,

where voltage overshoot on leakage inductance of the Kelvin source is measured. In [85], voltage overshoot caused by turn off di/dt on bus parasitic inductance in the commutation loop is measured to monitor the temperature. This method reduces the number of overshoot voltage sensing circuits but has to be calibrated for the specific converter as the commutation loop changes. Unlike IGBTs, turn off di/dt is not temperature dependent for SiC MOSFET [86], thus other TSEPs are adopted instead.

On-state resistance is calculated in [47] for temperature estimation of a 1.2 kV SiC MOSFET, which requires both measurement circuits for drain-source current and voltage. Turn off delay time is measured in [87], it has the advantage of being independent of the current. A large gate resistance of $150\ \Omega$ is used to increase its sensitivity which significantly increases the switching loss. Reference [88] offers a comparison between threshold voltage, on state resistance, and switching transients of 1.2 kV SiC MOSFET from different manufacturers, which show similar trend with increasing temperature.

2.2.2 TSEP of 10 kV SiC MOSFET

Few studies have specifically addressed TSEP for 10 kV SiC devices, leaving a significant gap in overheating protection and device health monitoring. As power modules operate at higher voltages and temperatures, their electrical characteristics shift due to intrinsic material properties. Identifying a reliable TSEP is crucial for real-time thermal monitoring and early fault detection in high-voltage applications.

A model of 10 kV discrete device switching behavior under varying temperatures is presented in [114], offering insight into temperature-dependent variations in turn-on delay, turn-off delay, and switching losses. However, this study does not establish a quantifiable and specific TSEP that can serve as an indicator for overheating conditions. Most existing studies on 10 kV SiC MOSFETs focus on conventional electrical parameters, such as on-state resistance and threshold voltage, which, while temperature-dependent, may not be sufficiently sensitive [116]. A lack of comprehensive studies on temperature-sensitive behaviors in 10 kV SiC power modules hinder the development of effective thermal protection schemes, which are critical for ensuring long-term reliability in medium-voltage power converters.

2.3 Cooling Design for MV Converter

In power electronic converters, the cooling system effectively dissipates the heat to prevent device damage from excessive temperature [89]. Various technologies have explored removing

heat at the device level by packaging liquid microchannels or heat pipes into the power module itself [90], [91]. Still these endeavors are in the research stage when most commercially available power devices rely on external cooling. Cooling system generally targets major heat sources in the converter, such as power devices, busbar, inductor and transformer [92], [93], [94]. And different cooling methods are applied based on specific requirements of thermal efficiency, size, weight, and cost. Liquid cooling, air cooling and two phase cooling such as heat pipe and vapor chamber are widely used [95], [96].

2.3.1 Liquid Cooling

Liquid cooling has the highest heat conductivity and can transfer heat up to 4X higher than the capacity of air of the same mass. A liquid cooling system is a hydraulic circuit that consists of a cold plate that interfaces with the device (heat source), a pump that circulates the coolant through the system, and a chiller that dissipates the heat absorbed by the coolant from the device.

The most basic heat exchange element is the cold plate in which the coolant runs through and carries heat away. It has a lower profile than a heatsink with air cooling for the same application. Its thermal performance is determined by the cold plate structure, coolant, and air velocity.

The cold plate structures are classified into four major types. 1) Formed tube cold plate, which coolant tubes are soldered to the cold plate or with thermal epoxy. This is the least complex cold plate. With limited thermal performance, it is used in low power applications. 2) Deep drilled cold plate have deep holes drilled into the plate to reduce the thermal resistance between the tube and the plate. 3) Pocketed fold fin cold plate. To further improve the thermal performance, folded fins are inserted in the pockets of the cold plate. 4) Microchannel liquid cooling (MLC) [97]. These four types of cold plates are shown in **Figure 2.7**. In MLC, multiple micron (30-150) channels are machine cut into the plate. MLC is suitable for high heat flux applications, such as inverter in aircraft where the cooling capability requires higher than 100 W/cm^2 . [98]

A suitable coolant improves cooling performance, reduces maintenance effort, ensures safety, and meets environmental compliance. However, choosing the right coolant depends on the operation temperature, heat transfer capacity, material compatibility and safety concerns. Water is the most common coolant for its high thermal conductivity. It often requires purification process to remove chemicals and contaminants away.

Deionized (DI) water has the same thermal properties as water, and has its ions removed including sodium, calcium, iron, and copper. Thus, it is an excellent insulator, typically used in

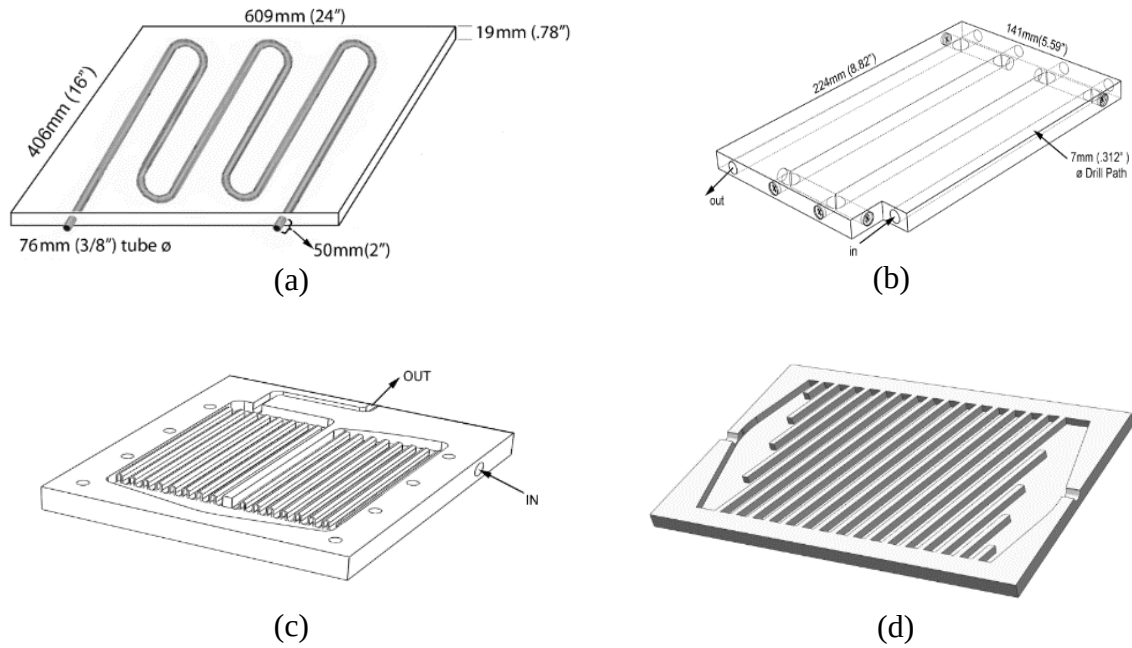


Figure 2.7. (a) Formed tube cold plate (b) Deep drilled cold plate (c) Pocketed fold fin cold plate (d) Microchannel [97].

medium and high voltage applications to prevent electric breakdown between high voltage components. Deionization uses a resin bed filter to remove these ions and impurities. To maintain the dielectric property of DI water, it must be filtered from time to time, which increases the operation cost. Also, with its nature of absorbing ions from contact surface, it is highly corrosive. Thus, only stainless-steel cold plate and chiller can be used with DI water.

Propylene glycol (PG) and Ethylene glycol (EG) are organic compounds that can lower the freezing point of water and increase its boiling point. Thus, glycol and water mixture can operate in both cold and hot environments as the operating temperature range is around (-45 to 106°C). EG is used in combustion engine cooling. PG has reduced heat transfer efficiency than water due to low thermal conductivity and specific heat. It is also more expensive than water. Proper disposal is necessary due to its toxicity. Synthetic mineral oils are nonconductive and non-corrosive. It is designed for submersion cooling that offers uniform cooling to the components immersed in the oil. It is thermally stable and evaporates over a lengthy period [99]. However, implementation brings safety concerns as oil is flammable. Oil has higher viscosity than other coolants, causing higher pressure drop.

Several properties of the coolant need to be considered when evaluating its thermal performance. Thermal conductivity measures how efficiently a fluid can transfer thermal energy through conduction. Specific heat is the amount of energy needed to heat up 1 gram of a substance 1 Celsius. Viscosity measures the fluid's internal resistance, which is often related to the thickness of the fluid and affects the pressure drop. The coolants discussed in the previous sections are listed below in **Table 2-3**.

The cold plate is connected to a chiller, which removes the heat from the coolant and circulates it back to the cold plate at a constant temperature and air velocity [100]. Chillers employ vapor compression refrigeration. It consists of a compressor, condenser, evaporator, and expansion valve, where the refrigerant undergoes phase transitions to cool the coolant. [101]. As there are many parts in liquid cooling, the installation, operation and maintenance take much more effort and cost than air cooling. Selecting a chiller depends on four factors: 1) heat load produced by the cooled device (Q), 2) the maximum allowable temperature for the fluid leaving the heat source (T_{out}), 3) the available fluid air velocity, and 4) the ambient operating conditions ($\dot{V}$). Frequently, equipment manufacturers provide specifications for the set point temperature

Table 2-3 Common coolant comparison.

Fluid	Thermal conductivity (W/mk)	Specific heat (J/kgK)	Viscosity (cP)	Boiling point (°C)	Freezing point (°C)
Water	0.580	4186	1.00	100	0
Deionized Water	0.606	4200	1.00	100	0
50-50 Water / Propylene Glycol	0.357	3559	5.20	106	-45
Mineral Oil	0.136	1700 to 2100	10 to 1000+	218-643	-40

and air velocity required for a chiller. In such instances, the process of choosing a recirculating chiller becomes straightforward. To determine the operational parameters of a chiller system, identify the intersection point between the specified cooling capacity and the setpoint temperature within the performance characteristic curves in **Figure 2.8**. Any chiller with a performance curve at or above these points ensures sufficient capacity. Subsequently, refer to the pump graph in **Figure 2.8** to choose a pump that aligns with the desired flow rate for the recirculating chiller [102].

2.3.2 Two-phase Cooling

The thermal performance of two-phase cooling is better than air cooling and lower than liquid cooling. Two-phase cooling is a passive system with no moving components like fans or pumps, thus it requires minimum maintenance and is highly dependable. The most common types of two-phase cooling are heat pipe, vapor chamber, and thermosiphon.

Heat pipes are metal pipes with working fluid (water) sealed inside. When one end of the heat pipe in contact with the heat source heats up, its working fluid evaporates and absorbs the heat.

Then the vapor moves to the lower temperature end of the heat pipe and condenses back to liquid form and returns to the heat source through capillary structure. This cycle of vaporization and condensation runs continuously and removes heat rapidly [103]. Thus, the maximum heat flux of heat pipes can reach above 300 W/cm^2 .

Heat pipes are very versatile as they can be bent, and their size and length can be adjusted. Three examples are shown here: 1) heat pipe integrated with heatsink; 2) heat spreader embedded with heat pipe for cooling and 3) heat pipe heat exchanger designed for electronic enclosure cooling, which carries heat away from the source and dissipates it at the surface of the enclosure [104] in **Figure 2.9**.

However, it can be daunting to select the right heat pipe, as its performance can be undermined. Some vendors provide online calculators to choose the specific length, diameter, coolant material, and wick structure based on heat load and ambient temperature. There are still limitations that undermine its thermal performance. Viscous forces prevent vapor flow inside the heat pipe due to low vapor pressure. Capillary refers to the capillary action in wick structure that cannot overcome gravitational and vapor flow pressure drop [106].

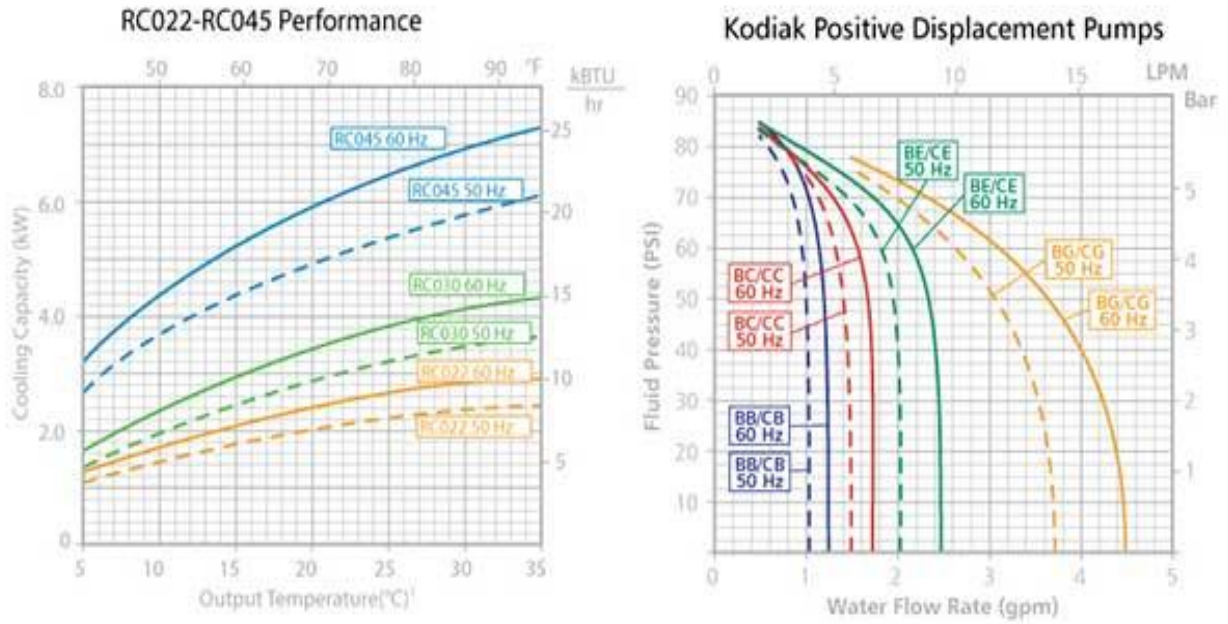


Figure 2.8. Chiller cooling capacity curve and pump pressure curve [102].



(a)



(b)



(c)

Figure 2.9. (a) heat pipe integrated with heatsink (b) heat spreader (c) Heat pipe heat exchanger [105].

Vapor chamber uses the same cooling theory of phase change process as heat pipes, but it houses vapor within a flat rectangular chamber rather than a pipe. Heat pipe has only one direction of heat spreading, which is along the axis. While vapor chamber can transfer heat in two dimensions, via a plane [107]. Vapor chamber is ideal in spreading heat more evenly through the surface, and is capable of transferring a large amount of heat [108]. It has a higher cost due to pressing two copper plates and sealing in the manufacturing process.

Like heat pipe, vapor chamber can be integrated into a heatsink base to transport heat quickly. In constrained spaces, they serve as highly efficient thermal spreaders, frequently employed in mobile phones and tablets. Alternatively, they may have attached fins for cooling purposes in servers, gaming consoles, routers, and larger industrial or aerospace applications [108].

Thermosiphon is also a passive and two-phase cooling system. It relies on gravity to circulate fluid instead of a capillary wick structure as introduced in heat pipes and vapor chamber [109]. A thermosiphon consists of an evaporator, a fluid loop, and a condenser as shown in **Figure 2.10**.

The evaporator is located below the condenser so the working fluid can return by gravity. Without the constraint of wick structure, it can carry a larger heat load over a longer distance than heat pipes [110]. Also, thermosiphon offers similar temperature across the whole assembly when there is multiple heat source. It is adopted in wind and solar IGBT inverter cooling. One disadvantage of thermosiphon is that it requires custom design, thus it can be more complex than off-the-shelf heat pipe constructions.

To summarize, heat pipe, vapor chamber and thermosiphon use two-phase cooling in which the cooling liquid absorbs heat and turns into vapor in the same enclosure, but they rely on different structures to circulate liquid back to the heat source area. They offer different level of heat capacity. They are implemented when forced convection cooling with heatsinks is not adequate for the heat load, or space limitation calls for lower profile. Manufacturers impose significantly higher charges for two-phase cooling due to its customized design and manufacture complexity. And the lead time is longer compared to other off the shelf products like heat sink and cold plate.

2.3.3 Air Cooling

Air cooling usually consists of a heat sink and a fan. It is very cost-effective and requires little maintenance. Heat sinks dissipate heat from the heat source to ambient air with a large surface area to maximize heat transfer. Their common function involves conducting the heat from the

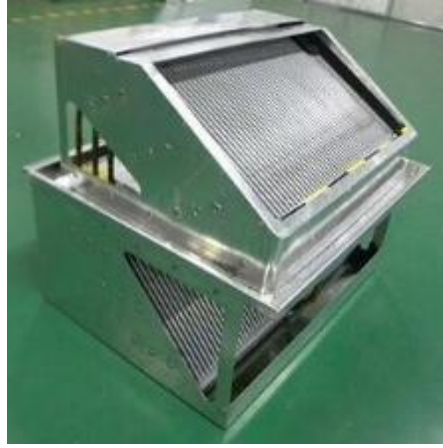


Figure 2.10. Thermosiphon [109].

base to fins with increased surface area and subsequently transferring heat to the surrounding air. There is a large variety of heat sinks that depend on application parameters such as volume, weight, air flow, flow type and environmental conditions as shown in **Figure 2.11**.

Extruded aluminum is one of the most cost-effective heat sink fabrications. It is usually employed in low to medium power applications. It can be scaled to high volume and offers simple customization. Because of its one-piece construction, it has limitations on maximum size.

A bonded fin heat sink is a dual-component assembly comprising an extruded or machined base featuring grooves or slots, and fins affixed using a thermally conductive bonding agent, commonly epoxy or soldering. With a higher number of longer fins, it offers better thermal performance.

Zipper fin stacks are constructed using a sequence of individual stamped metal fins, which are folded and interlocked through zipper-like features. Depending on the application requirements, the fins can be closed to form a finned duct or left open to allow multi-directional airflow.

Due to the high-power dissipation in MV converter, forced convection cooling is commonly applied. The fan provides a certain air velocity to direct cooler air into the heatsink or power device and forcing hot air out of the assembly. Fans are active components in which a motor rotates a bladed impeller around a central axis to induce air movement, resulting in a straight flow along the fan axis. Blowers, on the other hand, function by pulling intake air along the rotation axis and redirecting the airflow perpendicular to that axis through the blower housing. Blowers typically exhibit a higher pressure drop compared to fans, enabling them to exert greater force against flow resistances such as heat sinks or confined air ducts [112].



Figure 2.11. (a) Extruded aluminum heatsinks (b) bonded fin heat sink (c) Zipper fin heatsink [111]

When selecting a fan, PQ curves, commonly referred to as pressure-flow curves, are examined. The motor driving the fan has specific limitations in terms of speed and torque it can manage. The PQ curve illustrates the motor's capacity to push air through the impeller blades and the corresponding airflow at particular speeds for a fan or blower [113]. It is important not to operate above the curve.

Ideally, the fan size matches the component it intends to cool, such as a heatsink or air duct, so that the full air velocity is used. The fan volume should be small so that the power density of the converter is not compromised.

Fan and heatsink coordination can be tricky in a MV converter when the heatsink is connected to the source of power module at high voltage (kV) and the fan is powered by 24 V low voltage. Large clearance and creepage distance will undermine the thermal performance. In [114], a round guard ring with conductive painting surrounds the heatsink fin edges to limit the electric field strength to less than 2.4 kV/mm, which significantly reduces the chance of corona discharge. In [115], the heatsink is mounted with the drain terminal of 10 kV discrete device, an air duct directs air flow to the heatsink from a fan placed at a 60 mm clearance distance.

Air cooling has seen extensive research focusing on optimizing heatsink fin characteristics to reduce size and weight [116]. However, at the converter level, a comprehensive approach is needed to consider airflow direction and prevent hot exhaust air from affecting neighboring components [117] [118]. Studies in [119], incorporate impingement heatsinks with round pins, directing airflow from beneath the heatsink. To assess the thermal behavior comprehensively, a computational fluid dynamics (CFD) simulation for the entire converter is conducted for temperature evaluation. Another design approach in [120] encloses submodules in a box, directing airflow through the heatsink and then submodule capacitors. Similarly, [121] investigates optimal fan placement within the converter to ensure uniform airflow to prevent overheating in any one submodule.

Air-cooled systems offer a notable cost advantage compared to liquid systems. They do not necessitate regulated or specialized fluids and consist of fewer, more economical components when compared to their liquid counterparts. Due to the absence of liquids, there is a reduced risk of leaks, and with fewer components, the system has fewer potential points of failure. In addition to their higher reliability and lower overall cost, air-cooled systems are also simpler to modify or upgrade.

In typical applications, air cooling systems consist of an extruded or bonded fin heat sink, often accompanied by a fan. Forced convection solutions face limitations due to pressure drop. Heat sinks with extensive surface areas in practical volumes create significant air resistance, impeding the flow and, consequently, heat transfer achievable with a fan. Larger forced convection solutions may also require additional fans, contributing to increased noise levels. The primary constraint of air-cooled solutions, however, lies in thermal performance. Air lacks heat absorption and transfer capacity of liquid, reaching a threshold where air cooling becomes insufficient, necessitating a shift to liquid cooling solutions.

2.4 Summary

This chapter reviews key challenges associated with SiC MOSFET applications in MV power converters, focusing on APS insulation requirement, interwinding capacitance modeling, fault protection in series LLC APS, TSEPs, and thermal management strategies. The following aspects are investigated in the next chapters of this dissertation based on the research gaps discussed above:

- APS aspects: Insulation design and insulation material selection. Influence of core shape on reducing the interwinding capacitance of the APS transformer under the same winding configuration. Development of a protection method in a series LLC-based APS for isolation of faults, without interfering with other output voltages.
- TSEP: TSEP selections of 10 kV SiC MOSFET and evaluation of their temperature sensitivity. A sensor developed for 10 kV SiC MOSFET over temperature protection.
- Thermal management: Liquid cooling design procedure of multiple cold plates in MV converter regarding coolant selection, chiller pump sizing, and electrical insulation. Air cooling design in MV converter considering high voltage insulation. Design of uniform air flow air duct to provide uniform cooling performance.

Chapter 3 High Voltage Auxiliary Power Supply Design

This chapter focuses on high voltage auxiliary power supply (APS) design. Part of the content is from the paper published by the author in *IEEE 2023 ECCE* [122] and *IEEE 2024 ECCE* [123]. This chapter covers two different APS, sections 3.1 and 3.2 discuss the voltage balance methods and fault protection strategies of a series-connected LLC-based APS, which employs a single-input multiple-output configuration. Section 3.3 investigates the EMI immunity issue and startup issue of a flyback-based APS, which is a single-input single-output design.

3.1 Auxiliary Power Supply Design Requirements

The auxiliary power supply is used to power four gate drivers for a 10 kV H-bridge power module. Thus, it would be beneficial to employ a single input and four outputs topology so that the APS can be easily integrated with the gate driver. A series-connected LLC topology is selected for its simplicity.

The APS also needs to be small and compact, thus the centralized APS is adopted instead of a local APS. It will be much more challenging to reduce the size of the high voltage step-down transformer of the centralized APS to the required volume. Additionally, insulation requirement and interwinding requirements are crucial in APS; details are explained in the following sections.

3.1.1 Insulation Requirements

Under the worst-case operating condition of an APS in an MMC—when the highest-level submodule is inserted—the gate-driver reference (i.e., the device source) rises to the full DC-link potential. Because the APS output ground is tied to this high-voltage gate-driver ground while its primary side is driven by a low-voltage source, the secondary-to-primary isolation barrier must withstand the entire DC-link voltage, nominally 20 kV. To satisfy this requirement, the primary winding is realized with a 20 kV-rated high-voltage cable, and the transformer assembly is fully encapsulated in silicone gel exhibiting a dielectric strength of 20 kV/mm. This combination of high-voltage cable construction and gel encapsulation ensures reliable insulation of the core and windings without excessively enlarging the APS footprint.

To assess the insulation capabilities, a 2D electrostatic analysis is conducted in Maxwell software, focusing on the electric field exerted on a transformer operating at 20 kV. The model includes the core, windings, and cables, with accurate representations of the materials' electrical properties. The primary cable, encased in thick silicone rubber insulation, and secondary windings are specified with their relative permittivity and bulk conductivity. Excitation occurs at

the conductive part of the windings, with 20 kV applied to the secondary and 0 kV to the primary cable.

Two scenarios are simulated to test insulation strength: In the first scenario, the primary cable is centrally positioned within the core, with secondary windings evenly distributed. In the second scenario, the primary cable is located on one side, opposite the secondary windings. From **Figure 3.1** and **Figure 3.2**, the maximum electric field occurs near the conductor, gradually decreasing with distance. As the cable is rated 20 kV, the electric field within the primary insulation is assumed to be within acceptable limits and is therefore not evaluated here. In the first scenario, the potting material's required field withstand strength ranges from 0.99 kV/mm to 3.98 kV/mm, while in the second scenario, it varies from 0.47 kV/mm to 2.37 kV/mm. Considering a design margin, the second scenario is chosen due to its lower required field withstand strength in the silicone gel and the cable insulation jacket, ensuring a safer insulation level.

The transformer insulation is supported by encapsulation with silicone gel. Still, the exposed primary and secondary side PCBs are subject to high voltage. They need to meet clearance and creepage distance listed in IEC 60664 standards, which is 110 mm creepage distance for type II material at 20 kV voltage and 34 mm clearance distance in inhomogeneous field. The creepage distance is achieved by extending the primary cable to 60 mm, while the clearance distance is satisfied simultaneously.

The hipot test is conducted to verify the transformer insulation strength as shown in **Figure 3.3**. By applying a DC voltage of 20 kV DC across the primary and secondary winding for 10 minutes, the leakage current is 0.71 uA as shown in **Figure 3.4**.

3.1.2 Interwinding Capacitance

The interwinding capacitance between the primary and secondary windings in a toroidal transformer is largely determined by the size of the core. The capacitance is first estimated using energy conservative method, where each segment of the capacitance is calculated based on its geometry [79]. The first segment can be calculated in the following equation.

$$C_{11} = \frac{\varepsilon S_{p1} S_{s1}}{r_i (S_{p1} + S_{s1})} \quad (3.1)$$

where ε is the relative permittivity, S_{p1} and S_{s1} are the equivalent area of primary and secondary winding segments. Assuming the output voltage V_s is distributed linearly over the

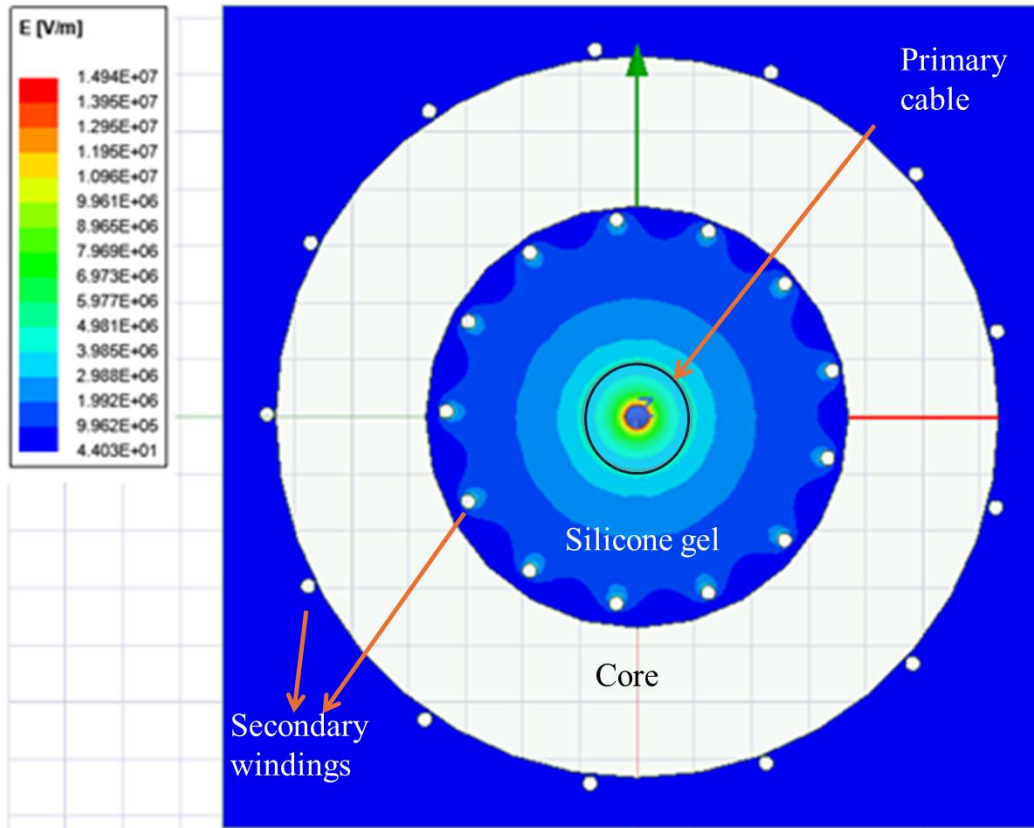


Figure 3.1. First scenario electric field distribution with primary cable is centered in core.

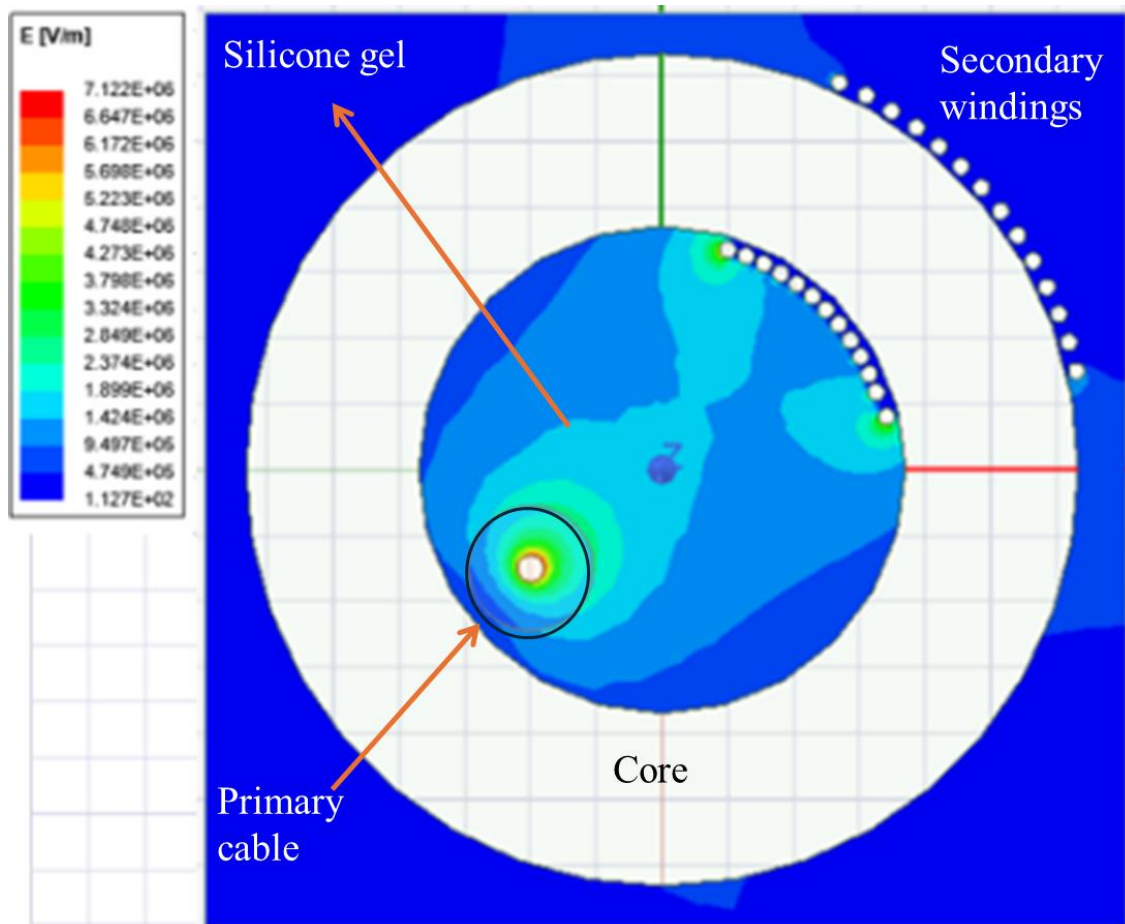


Figure 3.2. Second scenario electric field distribution with conductor at edge of core opening.

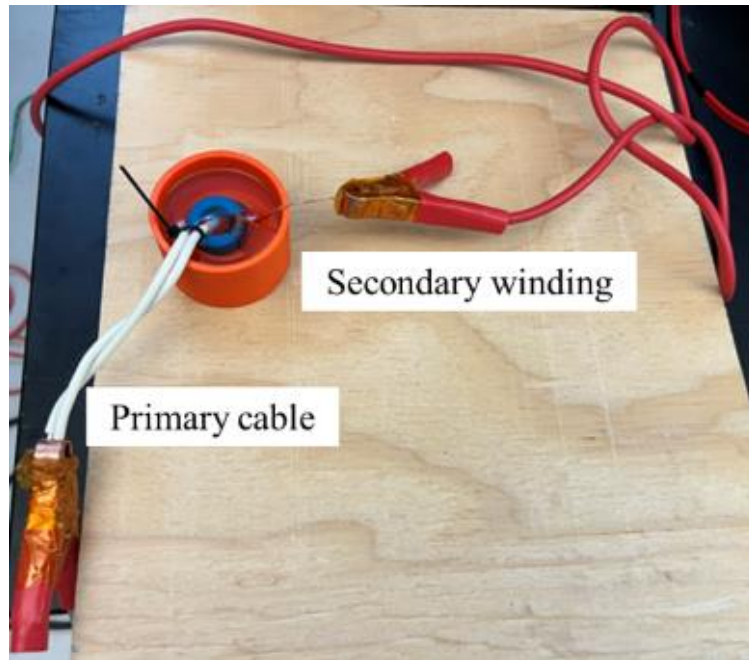


Figure 3.3. Hipot test set-up.

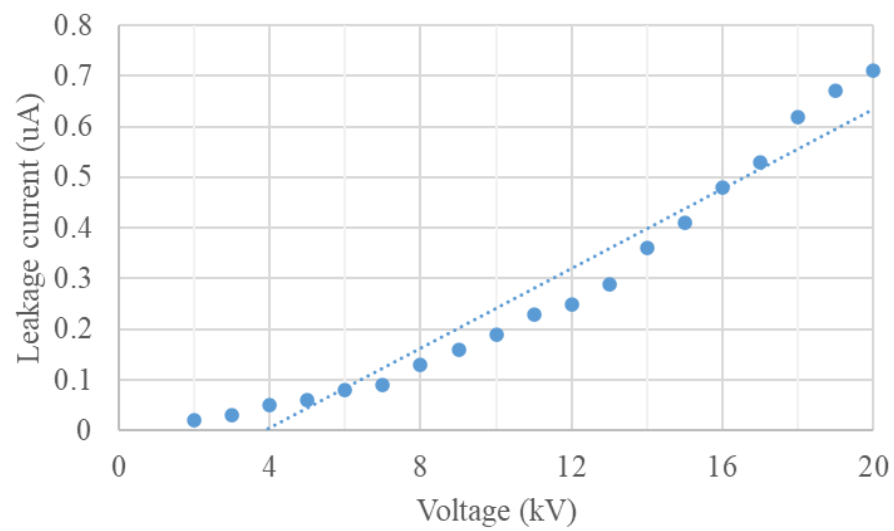


Figure 3.4. Leakage current is within suitable range at 20 kV.

secondary windings, the total energy stored in C_{11} is presented by:

$$E_{11} = \frac{1}{2} C_{11} \sum_{i=0}^{N_s-1} \left(V_p - \frac{V_s i}{N_i - 1} \right)^2 \quad (3.2)$$

where N_s is the secondary winding turns. Similarly, the capacitance and energy of the rest remaining windings can be calculated. Adding them together equals the total energy stored by the interwinding capacitance C_{io} .

$$E_{total} = \frac{1}{2} C_{io} (V_p - V_s)^2 \quad (3.3)$$

The core size selected is 25.3mm × 14.8mm × 15.0 mm with 14 turns of secondary windings, the value of interwinding capacitance estimated is 1.2 pF. Since the LLC resonant controller operating frequency is below 500 kHz, material N87 is selected.

The interwinding capacitance can be modeled as a cylindrical plate capacitance with two layers of insulation, the cable insulation, and potting materials as a rough estimate. Thus, the distance between the primary winding and secondary winding, the height of the toroidal core and insulation material dielectric constant determine the capacitance. The potting material is TSE3070 with dielectric constant of 2.7 and dielectric strength at 18 kV/mm. This material is chosen due to its relatively high dielectric strength to achieve the 20 kV insulation target and low dielectric constant to lower interwinding capacitance.

The primary cable is placed as far away as possible from the secondary windings to reduce the interwinding capacitance, and the secondary windings are congregated at the other end. The capacitance is simulated using 3D model in Ansys Maxwell under static electric field, where the 20 kV voltage is applied to the secondary side and 0 kV is applied to the primary cable.

The coupling matrix between these two objects is calculated using a finite element method. And the regional material covering the whole transformer is assigned with 2.7 dielectric constant to emulate potting material. The capacitance simulated is 0.63 pF as shown in **Figure 3.5**.

The actual value measured by the impedance analyzer Keysight E4990A in the air is 1.5 pF, which is close to the calculation from (3.3) at 1.2 pF. The connection to the impedance analyzer introduces some errors. The simulation depicts half of the interwinding capacitance; thus, it is around one-half of the actual value.

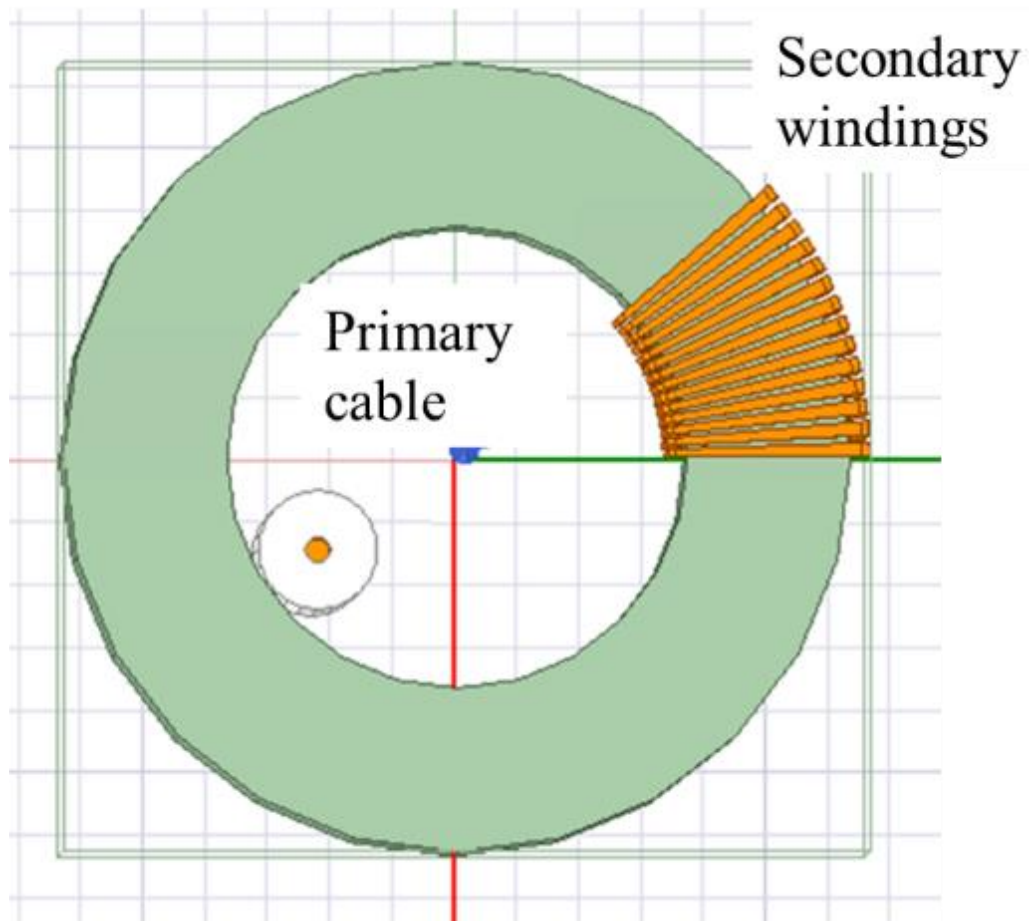


Figure 3.5 Toroidal transformer interwinding capacitance simulation model.

3.2 Series LLC APS Protection Scheme Analysis

3.2.1 Operation Analysis Under Fault

A series LLC converter with four outputs is implemented to provide power for four gate drivers of a H-bridge power module. The specifications are listed in **Table 3-1**. It is different from conventional LLC converter in that there are four magnetizing inductances in the resonant network as shown in **Figure 3.6**. This configuration distributes the magnetic coupling across all outputs, reducing the effective voltage gain of each individual port to one-quarter of the nominal value observed in single-output designs.

The voltage gain characteristics of the system were analytically derived using fundamental harmonic analysis (FHA), a widely adopted method for approximating resonant converter behavior. Equation (3.4) expresses the voltage gain M for each output port as a function of normalized frequency f_n and quality factor Q_e .

$$M = \left| \frac{L_n^2 f_n^2}{[(4L_n + 1)f_n^2 - 1] + j[(f_n^2 - 1)f_n Q_e L_n]} \right| \quad (3.4)$$

Where L_n denotes the normalized magnetizing inductance and all remaining terms are defined in **Table 3.2**. Parametric sweeps of this equation reveal the expected inverse relationship between load power and voltage gain: the lightest load condition (0.5 W) produces the highest gain curve, while the heaviest load (7.5 W) yields the lowest. This behavior aligns with classical LLC converter theory but exhibits compounded sensitivity due to the multi-output architecture.

The reflected secondary resistance to the primary side changes to zero under a short circuit fault or increases to infinity during an open circuit fault, thus changing the output voltage or the resonant frequency. Here, only one output fault is examined for protection.

In **Figure 3.7**, blue curves are under normal operation at different loads, and the red curves are under one output short circuit fault. Resonant frequency stays the same, but the voltage gains at the operating point shift upward. The output voltage increases significantly to over 40 V.

In **Figure 3.8**, the voltage gain of the open circuit fault is also plotted in red, this time the resonant frequency decreases. The controller's continued operation at the pre-fault frequency creates a critical mismatch: the three healthy outputs suffer insufficient gain (<5 V), jeopardizing gate driver functionality, while the open-circuited port experiences voltage runaway (>40 V) from un-dissipated resonant energy.

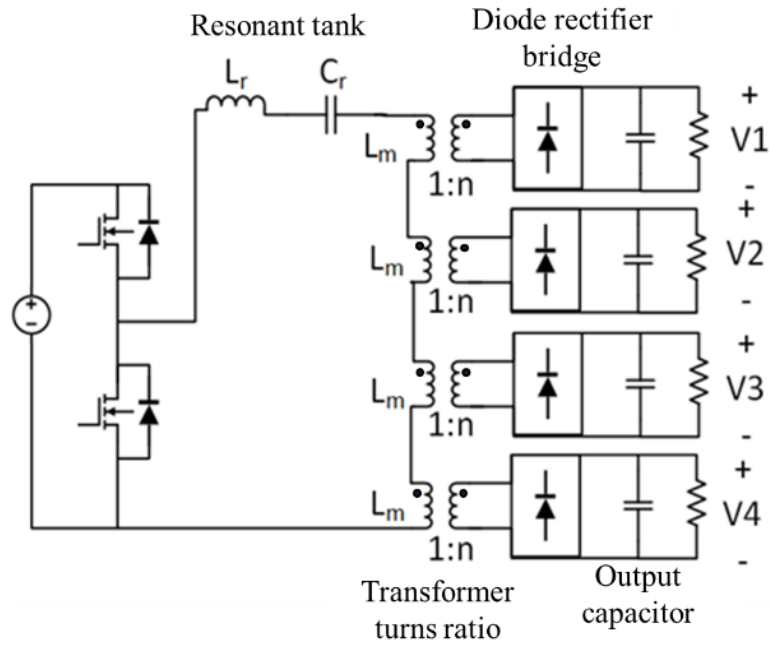


Figure 3.6. Four output series LLC topology.

Table 3-1 Specifications of LLC series connected converter

Specifications	Values
Input voltage	15 V
Output voltage	24 V
Output power for each output	7.5 W
Switching frequency	260 kHz
Resonant inductance	1.2 μH
Resonant capacitance	423 nF
Magnetizing inductance	3.12 μH
Turn ratios	1:14

Table 3-2 Nomenclature of series resonance network

Specifications	Symbol	Equation
Resonant frequency	f_r	$\frac{1}{2\pi\sqrt{L_r C_r}}$
Inductance ratio	L_n	$\frac{L_m}{L_r}$
Effective output resistance	R_e	$\frac{8N_p^2}{\pi^2 N_s^2} R_{load}$
Quality factor	Q_e	$\sqrt{\frac{L_r}{C_r}} / R_e$
Normalized switching frequency	f_n	$\frac{f_s}{f_r}$

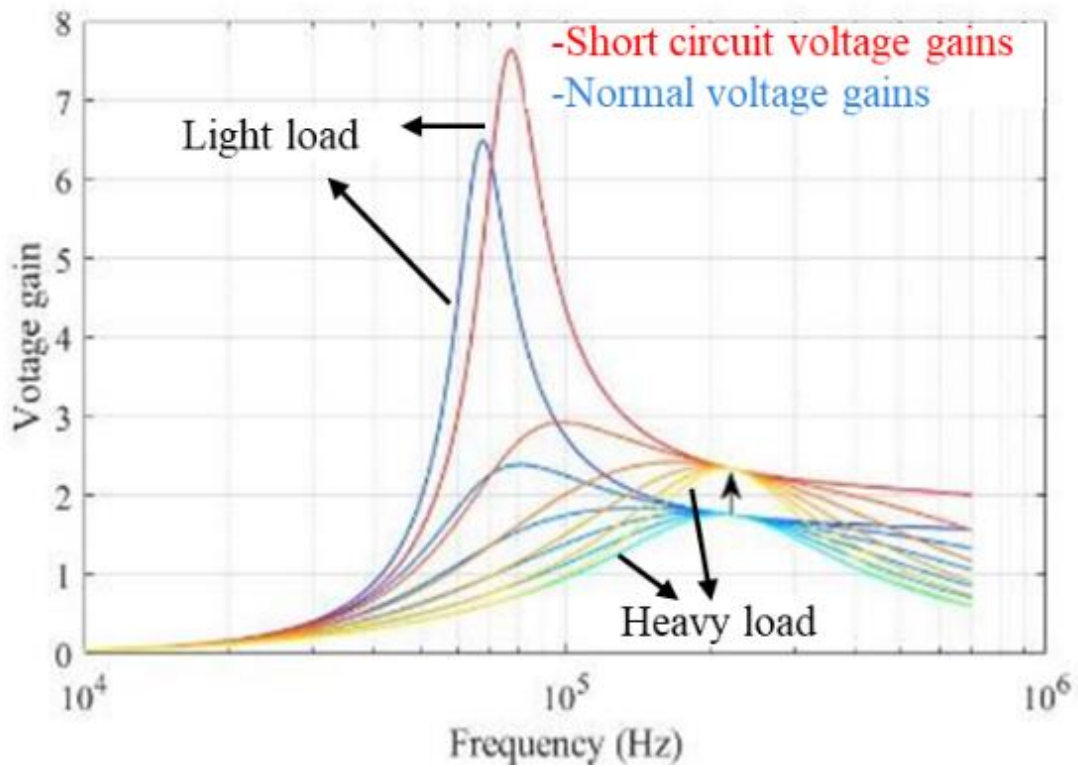


Figure 3.7. Resonant voltage gains increase during short circuit.

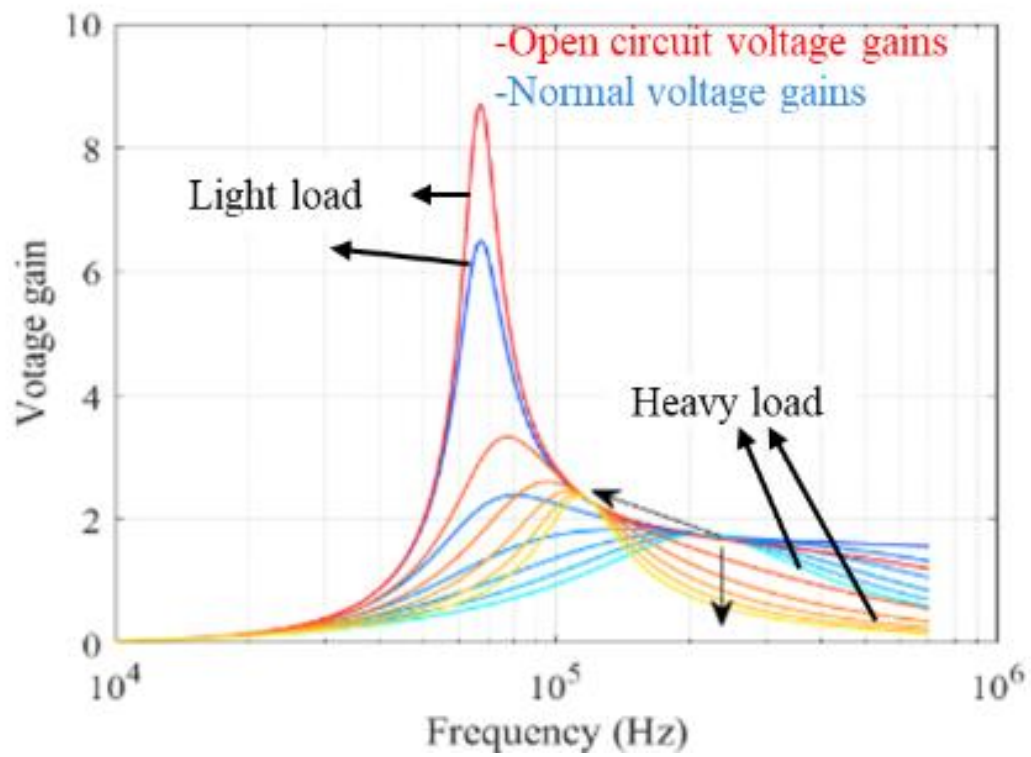


Figure 3.8. Resonant frequency decreases during open circuit.

3.2.2 Protection Scheme Analysis

3.2.2.1 Coupling Winding

A one-turn coupling winding is added between adjacent cores of the secondary winding to evaluate its effectiveness in mitigating voltage imbalance. Therefore, the fluxes between the cores are controlled to be equal, leading to uniform voltage output. The output voltages at 7.5 W are approximately half that at 3.8 W in **Table 3-3** where coupling winding is not implemented.

The voltage imbalance is significantly reduced when the coupling winding is implemented in **Table 3-4**. However, the voltage at the output adjacent to the output experiencing a short circuit fault is 10 V higher with coupling winding. During an open circuit fault, the voltage at the non-faulted outputs is maintained to the rated voltage without decreasing as shown in **Table 3-4**. However, this method is infeasible as the coupling winding reduces the insulation independence between the outputs, which compromises the operation of H-bridge gate driver connected to it.

3.2.2.2 Protection at Primary Side

The primary side of the LLC resonant converter can be effectively protected by monitoring the resonant capacitor voltage (V_{C_r}) as a key diagnostic parameter. This approach leverages the direct correlation between V_{C_r} and the primary-side resonant current, which exhibits measurable deviations during fault conditions. Under normal operation, the resonant capacitor voltage remains within a predictable range; however, a short-circuit fault in any of the four output channels causes a significant increase in primary current, reflected as a proportional rise in V_{C_r} .

For example, at the maximum rated output power of 7.5 W per channel, experimental measurements demonstrate that the peak resonant capacitor voltage escalates from approximately 19 V (nominal operation) to over 30 V during a short-circuit event (see **Figure 3.9**). This ~58% increase provides a reliable threshold for fault detection. The protection mechanism can be implemented by comparing V_{C_r} against a fixed voltage threshold (e.g., 25 V) using a high-speed comparator. Upon threshold violation, the controller is immediately disabled via a hardware interrupt, preventing further energy transfer and protecting both the converter and downstream components.

Table 3-3. Output voltage without coupling winding.

Operation condition	Output ratings	Output 1	Output 2	Output 3	Output 4
Unbalanced load	P_{load}	7.5 W	7.5 W	3.8 W	3.8 W
	V_{out}	17.7 V	17.7 V	33 V	32 V
Output short circuit fault	P_{load}	7.5 W	7.5 W	7.5 W	Short circuit
	V_{out}	35 V	35 V	35 V	0 V
Output open circuit fault	P_{load}	7.5 W	7.5 W	7.5 W	Open circuit
	V_{out}	8 V	8 V	8 V	80 V

Table 3-4. Output voltage with coupling winding.

Operation condition	Output ratings	Output 1	Output 2	Output 3	Output 4
Unbalanced load	P_{load}	7.5 W	7.5 W	3.8 W	3.8 W
	V_{out}	27.9 V	28.1V	22 V	23V
Output short circuit fault	P_{load}	7.5 W	7.5 W	7.5 W	Short circuit
	V_{out}	31 V	32 V	45 V	0 V
Output open circuit fault	P_{load}	7.5 W	7.5 W	7.5 W	Open circuit
	V_{out}	24.8V	23V	23 V	72 V

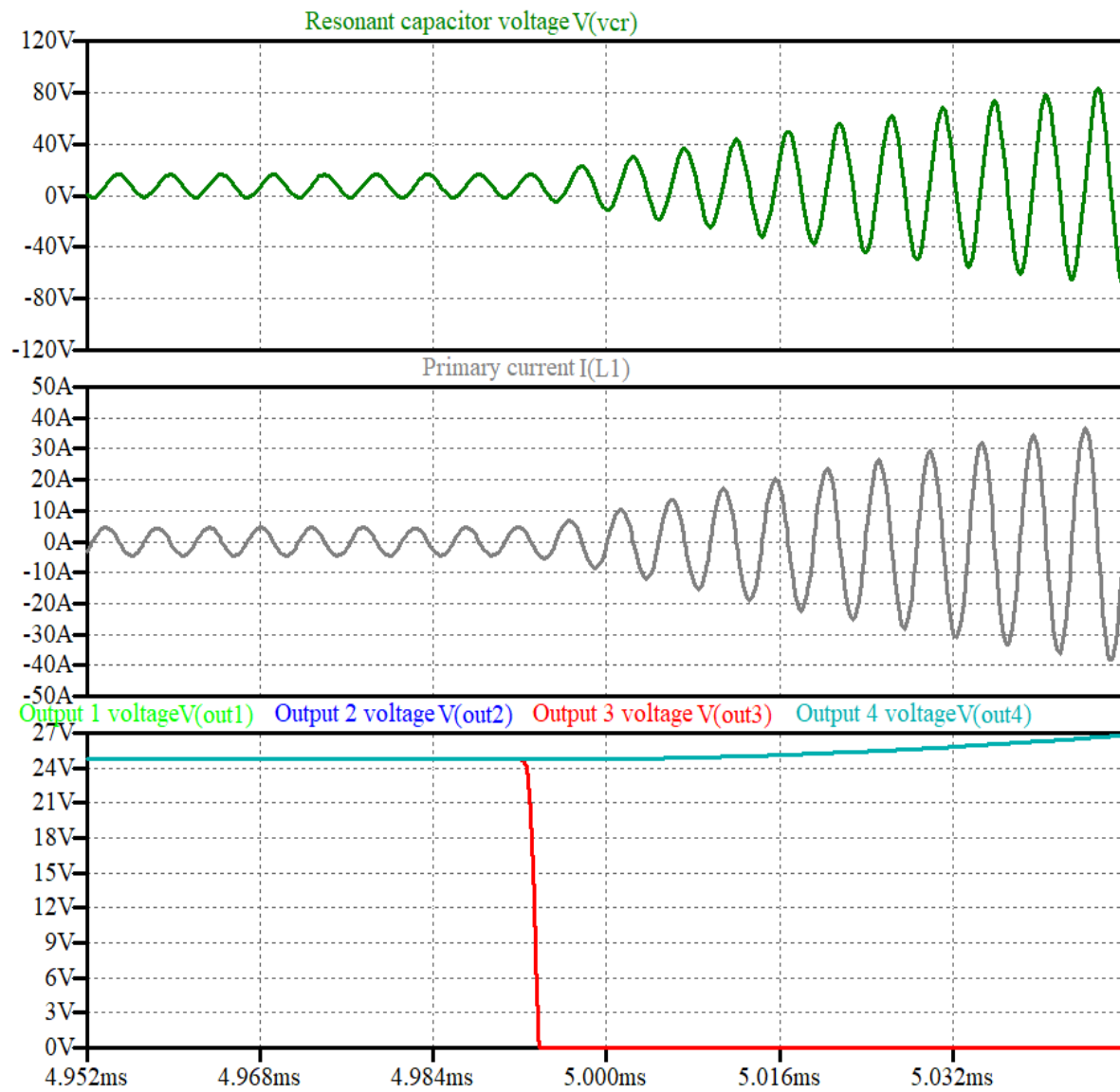


Figure 3.9. Short circuits happen at 4.99 ms when output power is 7.5W.

3.2.2.3 Protection at Secondary Side

Secondary-side protection is implemented because it enables isolation of individual faults without necessitating a complete shutdown of all output channels. When there is a short circuit at one output, that output voltage drops to zero as shown in **Figure 3.9** and **Figure 3.10**. While the other non-faulted output voltage increase.

In **Figure 3.11**, during open circuit fault, the output voltage at channel 3 ramps up to 40 V due to the increased voltage gain. In contrast, the output voltages of the remaining channels gradually decrease. Notably, both the resonant capacitor voltage and the primary current exhibit a reduction under this fault condition.

Protection at the secondary side is implemented by an e-fuse LTC4365 with a MOSFET behind the secondary rectifier bridge. The overvoltage threshold is set at 28 V, and the undervoltage threshold is set at 5 V. The output that experiences the short circuit would trigger the undervoltage protection, and e-fuse will switch off the MOSFET, separating the circuit from the gate driver. When an open circuit fault occurs, the output overvoltage will also trigger the overvoltage protection, and e-fuse will separate the faulted circuit.

The hardware test setup is presented in **Figure 3.12** to evaluate the APS. The primary board drain-source voltage, resonant capacitor voltage, and primary side current are measured with each output connected to a 75 Ω resistive load. As shown in **Figure 3.13**, the primary side current and resonant capacitor voltage remains stable even when the secondary output is experiencing a short circuit.

The controller is unaware of the short circuit fault due to the open loop operation. Convention output voltage feedback provided by optocoupler is infeasible in this application as it failed to meet 20 kV insulation requirement and less than 5 pF interwinding capacitance requirement. Thus, additional protection circuit has to be implemented to prevent overvoltage.

From **Figure 3.14**, the short circuit happens in the third output V_{o3} , the e-fuse isolates the fault immediately. The three not faulty output voltages ramp up to 28 V and are clamped for 200 μ s by the IC before returning to normal 24 V. The faulty output is cleared without interfering with the remaining not faulty outputs.

An open-circuit fault is intentionally introduced on the fourth output, V_{o4} , for a duration of 120 μ s by using a gate-controlled MOSFET placed in series with the load, as illustrated in **Figure 3.15**.

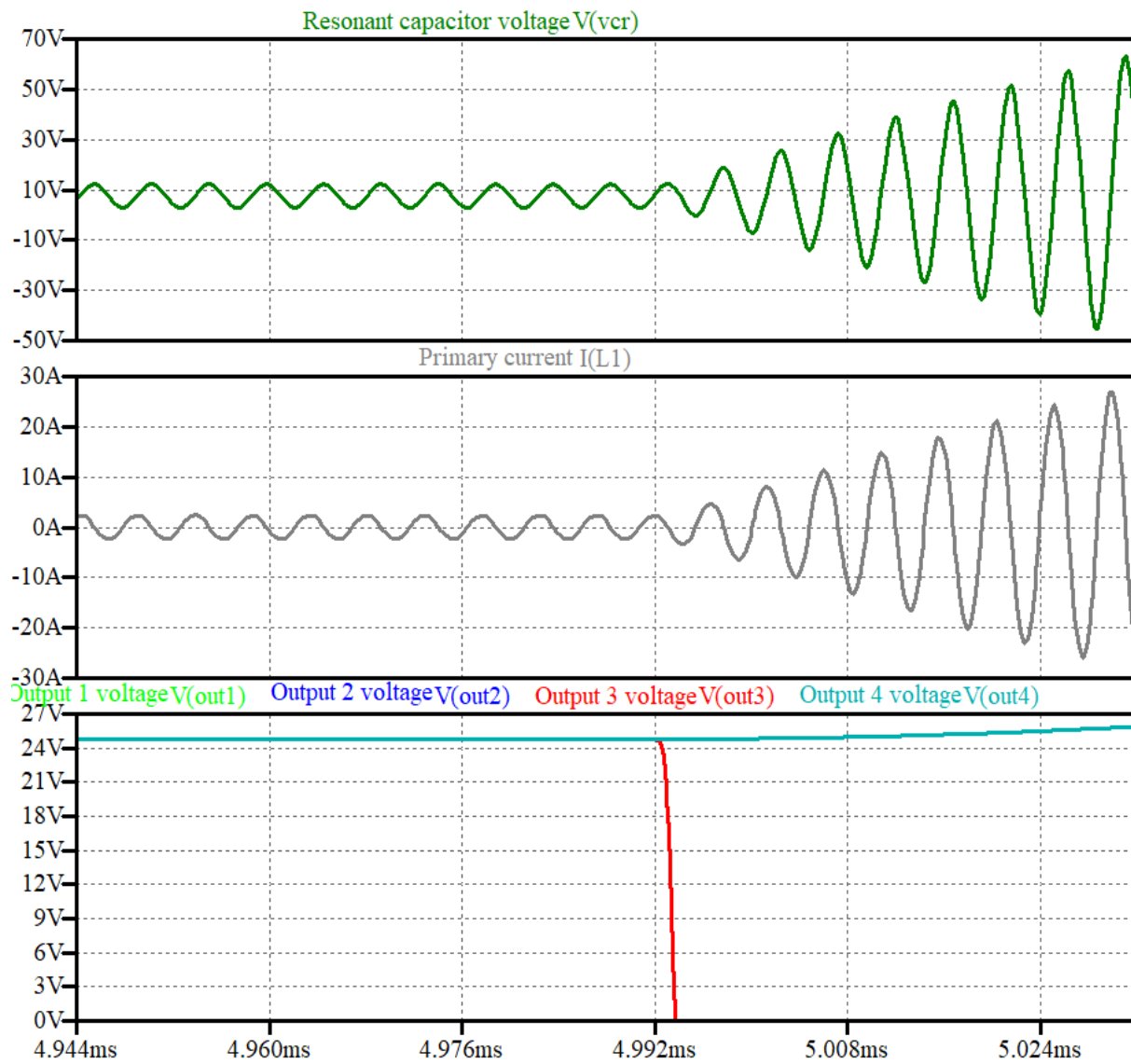


Figure 3.10. Short circuits happen at 4.99 ms when output power is 2.5 W.

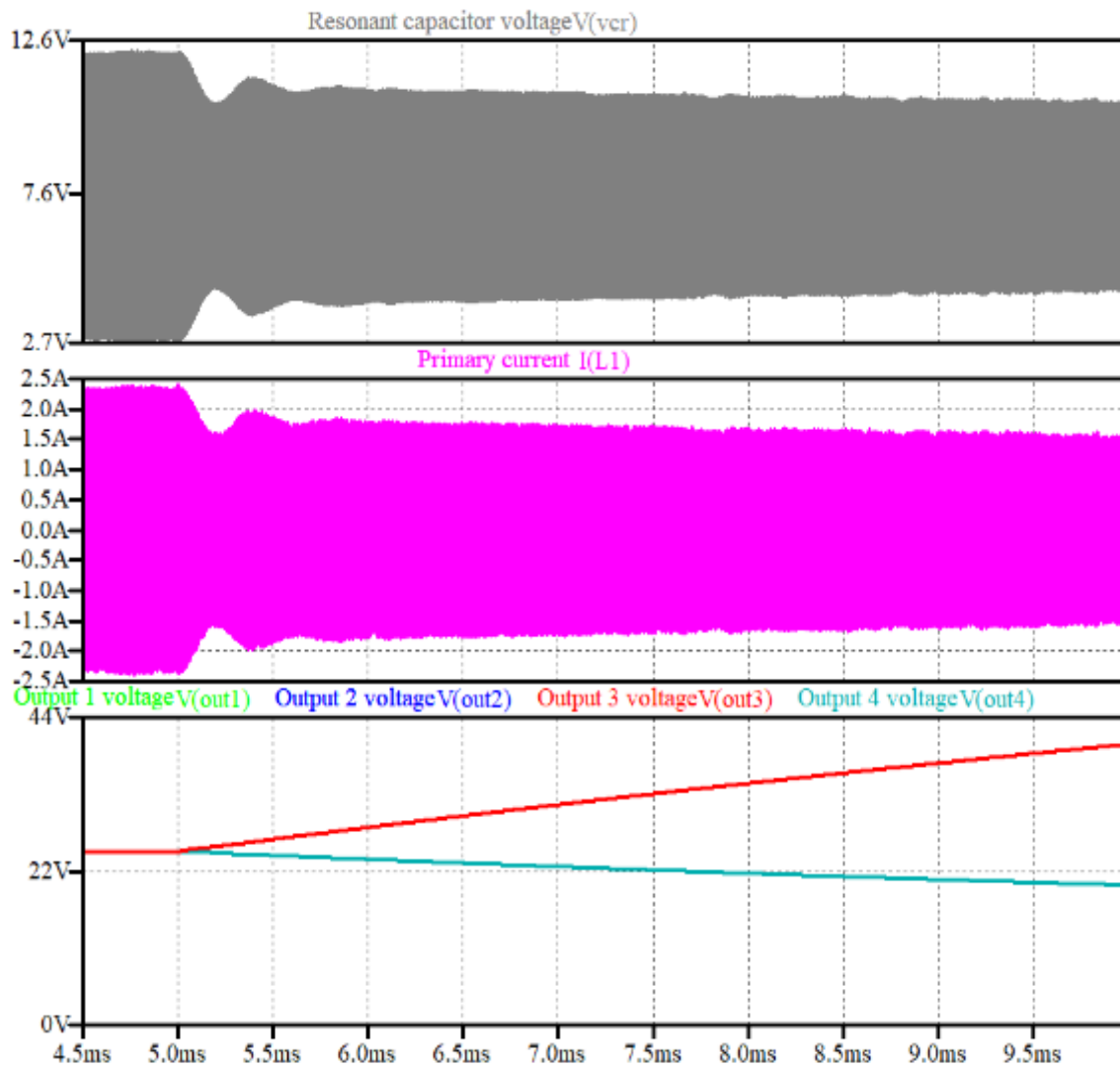


Figure 3.11. Output 3 voltage ramps up to 40 V during open circuit fault at 4.99 ms.

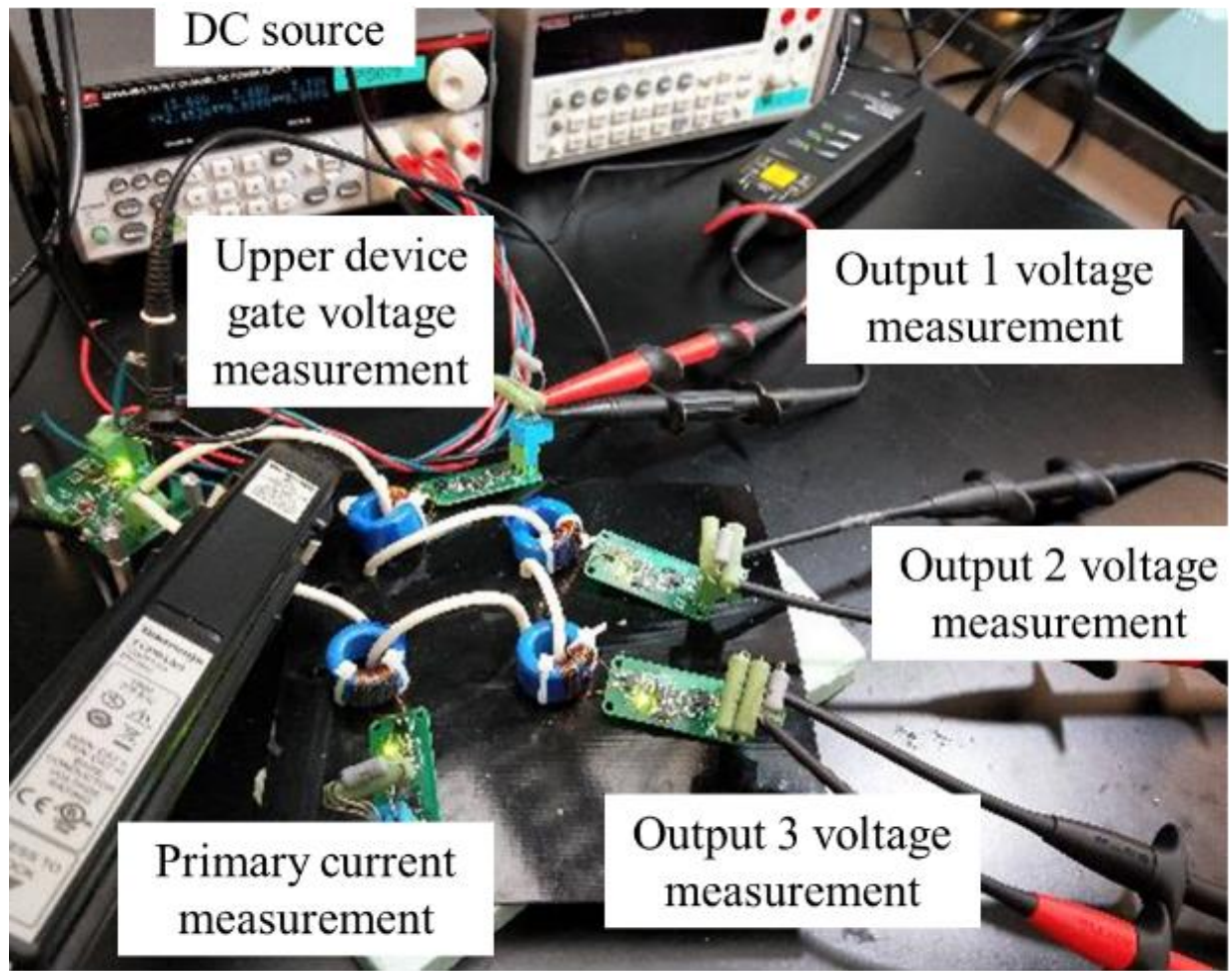


Figure 3.12. Series LLC APS test setup.

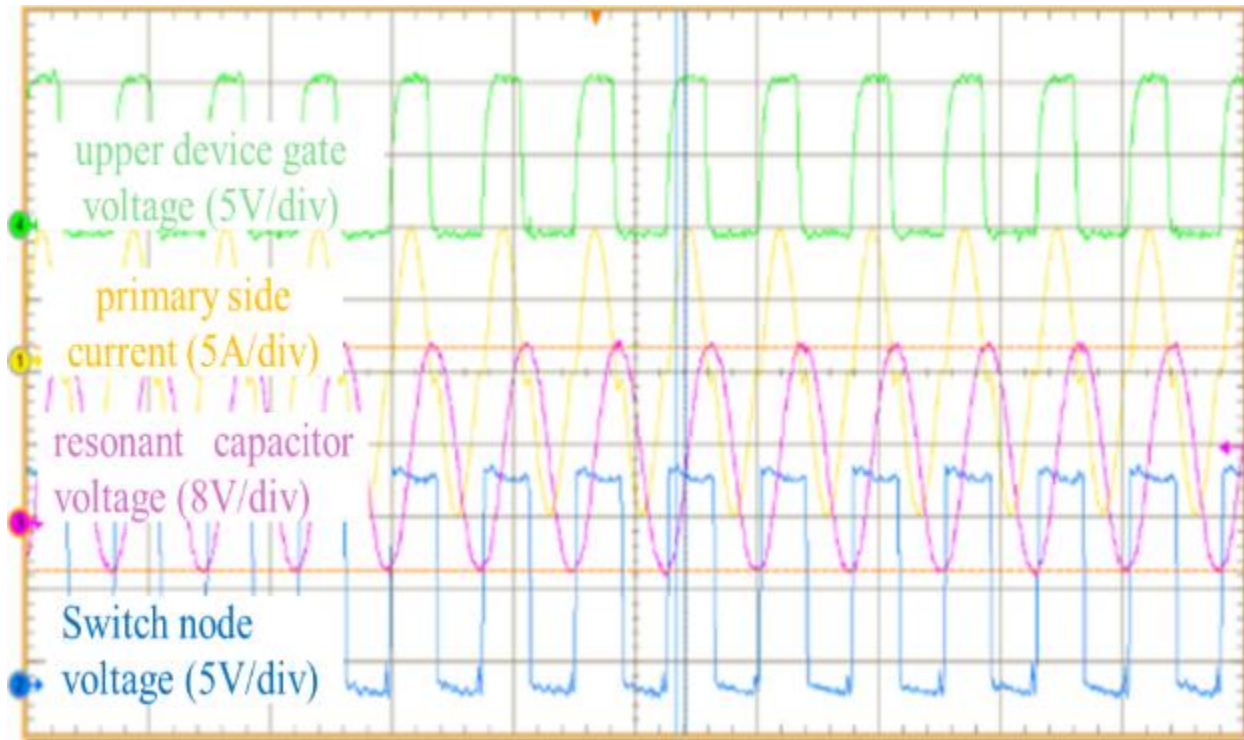


Figure 3.13. Series LLC APS primary side waveforms are still stable during short circuit.



Figure 3.14. Short circuit is cleared by secondary protection.

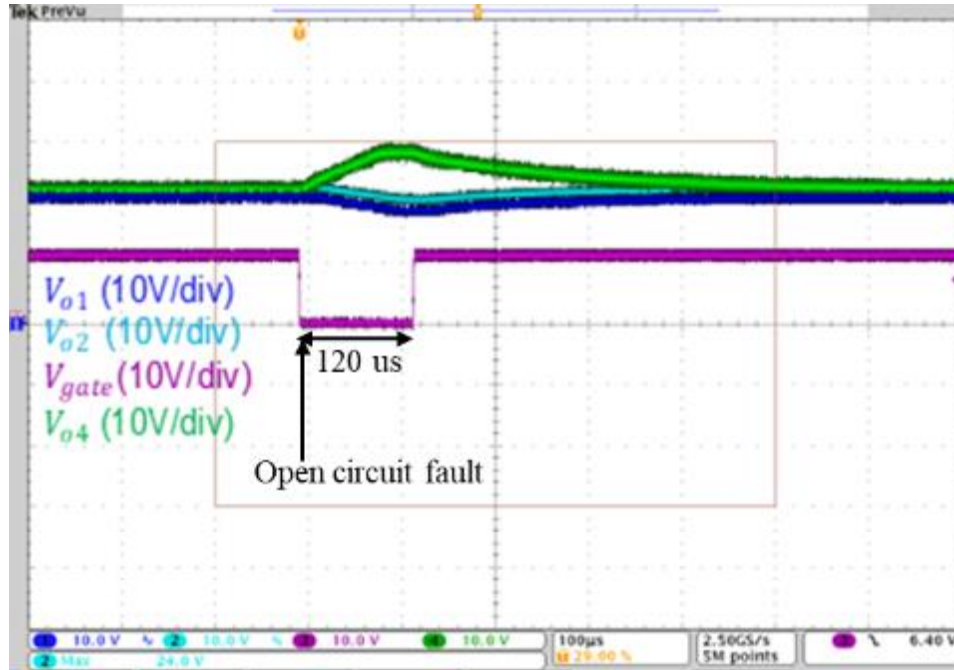


Figure 3.15. Voltage is clamped during open circuit fault.

As a result of the open-circuit condition, the voltages at output 1 V_{O1} and output 2 V_{O2} drops to 16.4 V and 15.8 V, respectively. Meanwhile, output 4 V_{O4} ramps up to 28 V in 86 us, at which point it is clamped by the IC. The clamping mechanism effectively limits the high voltage resulting from the open circuit to a safer range, thereby demonstrating the robustness and effectiveness of the implemented protection scheme.

3.3 Flybuck APS Testing in MV Converter

This section discusses another APS design that uses a different topology from the previous series LLC converter. The APS here is built in large quantities to supply power to multiple gate drivers in a multilevel MV converter. The APS adopts the same topology of a flybuck converter that support gate drivers of 10 kV 20A discrete device in a 100 kVA 13.8 kV AC cascaded H bridge converter [57].

This project is a 1 MVA 13.8 kV AC multilevel converter which uses a 10 kV 100 A power module. Thus, the gate driver requires more power to drive the module than the discrete device. The APS power is scaled up from 2 W to 3 W accordingly. The power module switches faster, the dv/dt is 100 V/ns compared with 10 kV discrete device at 60 V/ns [124], thus posing more challenges to the EMI tolerance of the APS. Much of the existing literature lacks coverage of the APS when in the demanding high-voltage and high-EMI environment typical of MV converters.

Consequently, the discussion on APS performance is expanded to address these specific operational challenges.

3.3.1 Interwinding Capacitance

To optimize the interwinding capacitance between the primary side and secondary side of the APS to less than 5 pF, the interwinding capacitance of different core shapes is analyzed.

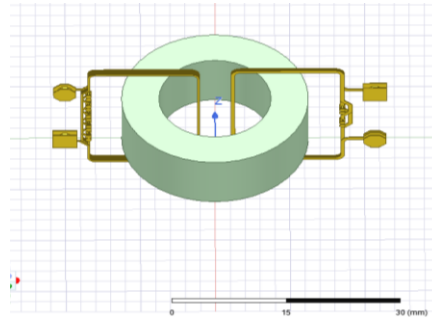
The capacitance $C_{coupling}$ can be represented in (3.5), where C_{pc} is the capacitance between primary winding and the core, C_{sc} is capacitance between secondary winding and the core, and C_{ps} represents capacitance between primary and secondary windings.

$$C_{coupling} = \frac{C_{pc}C_{sc}}{C_{pc} + C_{sc}} + C_{ps} \quad (3.5)$$

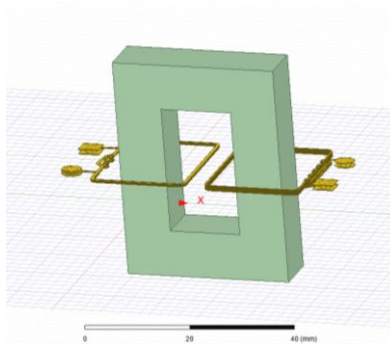
The basic physics of capacitance leads to placing the windings away from the core, separating the windings as far as possible and minimizing the facing area in between. The core shape effect on interwinding capacitance is investigated by comparing the toroidal core, U core, and E core. The core with relatively small size in each core shape category is selected. By controlling the winding parameters to be the same, such as trace width (0.5 mm and 0.25 mm), PCB winding turns (3:6), and winding distance (4 mm) from the core, the interwinding capacitance of different core shapes is simulated in Ansys Maxwell 3D electrostatic analysis in **Figure 3.16**. The voltage excitations are 20 kV on the secondary winding, 24 V on the primary winding and 0 V on the core respectively.

From **Table 3-5** interwinding capacitance is smaller in toroidal core than U core and E core. This can be explained by the fact that rectangular U core has a longer perimeter than toroidal core, thus larger capacitance. For E core, the distance between windings and core is constrained by the small winding area and its flat shape. Also, all four edges of winding are in parallel with the core, the overlapping area is larger than that of other core shapes, resulting in higher C_{pc} and C_{sc} .

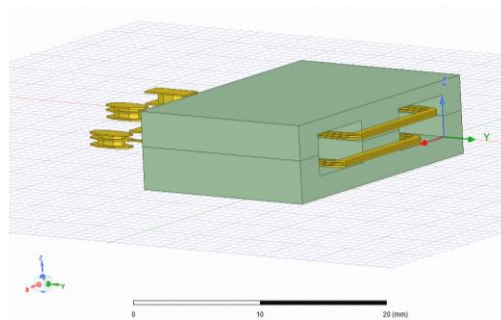
To optimize the interwinding capacitance, toroidal core and U core are promising candidates. Unlike conventional transformers, this arrangement of winding and core inevitably leads to a transformer with large leakage inductance. The coupling coefficient is around 0.96. The tradeoff between achieving low interwinding capacitance and sufficient magnetizing inductance is challenging as it depends on core size, material, core and winding distance, and geometry.



(a) TX25/15/10



(b) U33/22/9



(c) E22/6/16

Figure 3.16. Toroidal core, U core and E core interwinding capacitance model in Ansys Maxwell.

Table 3-5 Interwinding capacitance comparison between different core shape.

Core type	TX25/15/10	U33/22/9	E22/6/16
C_{pc} (pF)	0.93	1.18	1.48
C_{sc} (pF)	0.98	1.18	1.66
C_{ps} (pF)	0.17	0.17	0.56
$C_{coupling}$ (pF)	0.65	0.76	1.34

3.3.2 APS Testing with Gate Driver

APS may fail to start up when testing with the gate driver as there is much more capacitive load than a pure resistive load. The APS is a flyback topology which samples the feedback voltage and primary current for control regulation. As shown in **Figure 3.17**, the primary current reaches 3.88 A which exceeds the primary overcurrent protection threshold 3.2 A, then the IC will stop operating, failing to startup.

There is also case where the APS stops operating and restarts after some time, which is called hiccup mode in **Figure 3.18**. This behavior is often observed when the APS tries to adjust itself in response to overcurrent conditions. During this time, the APS operates at an initial low switching frequency of 186 kHz, which is about half of the normal operating frequency of 378 kHz. The lower switching frequency leads to higher primary current, as illustrated **Figure 3.19**, which further exacerbates the overcurrent shut-down.

To resolve the issue of high primary current during startup, one potential solution is to increase the switching frequency. By raising the switching frequency, the current ripple is reduced, allowing the APS to start more smoothly without triggering the overcurrent protection. This adjustment helps manage the capacitive load more effectively and prevents excessive current flow during the startup phase.

In addition to adjusting the switching frequency, another modification was made to the APS's output capacitance. Initially, the output capacitance was set to 22 μF , which was insufficient to match the input capacitance of the gate driver, which is 50 μF . Since the gate driver requires a higher capacitance for stable operation, the APS output capacitance was increased to 50 μF to better match the gate driver's needs. This adjustment allows for a more successful startup by reducing the impact of the gate driver's capacitive load and ensuring proper voltage regulation during the startup process as shown in **Figure 3.20**.

With these changes, the higher switching frequency and increased output capacitance—the APS becomes more capable of handling the higher capacitive load presented by the gate driver, resulting in a smoother startup process. These improvements allow the APS to start up more reliably without triggering overcurrent protection or entering hiccup mode, ensuring efficient operation of the multilevel converter.

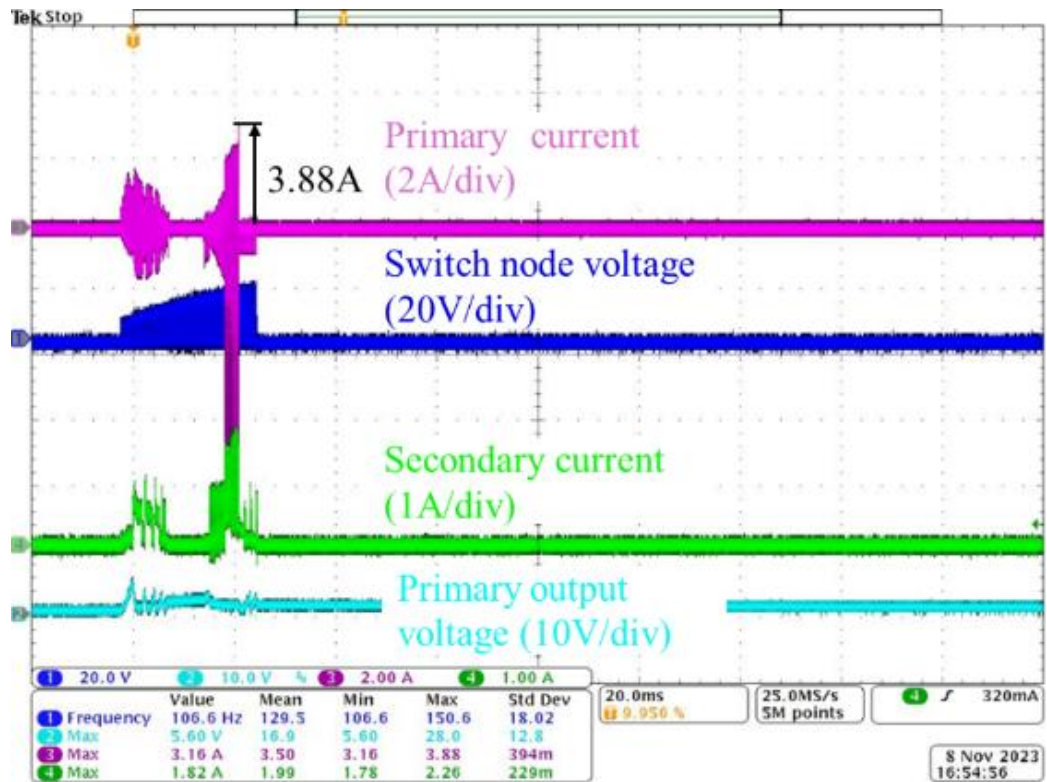


Figure 3.17. APS unsuccessful startup due to overcurrent.

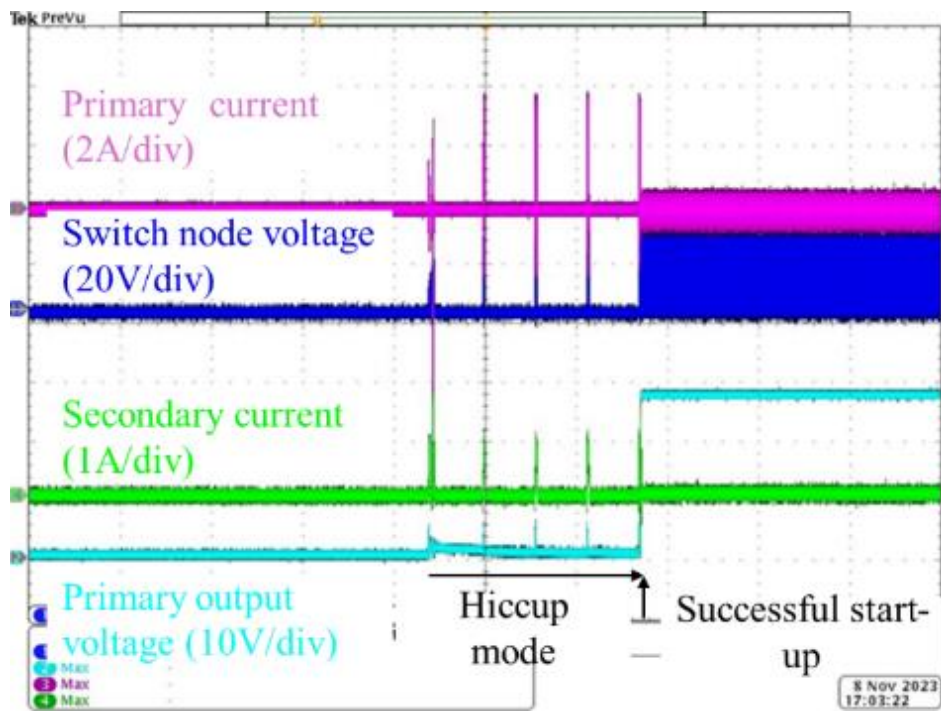


Figure 3.18. APS in hiccup mode before start up.

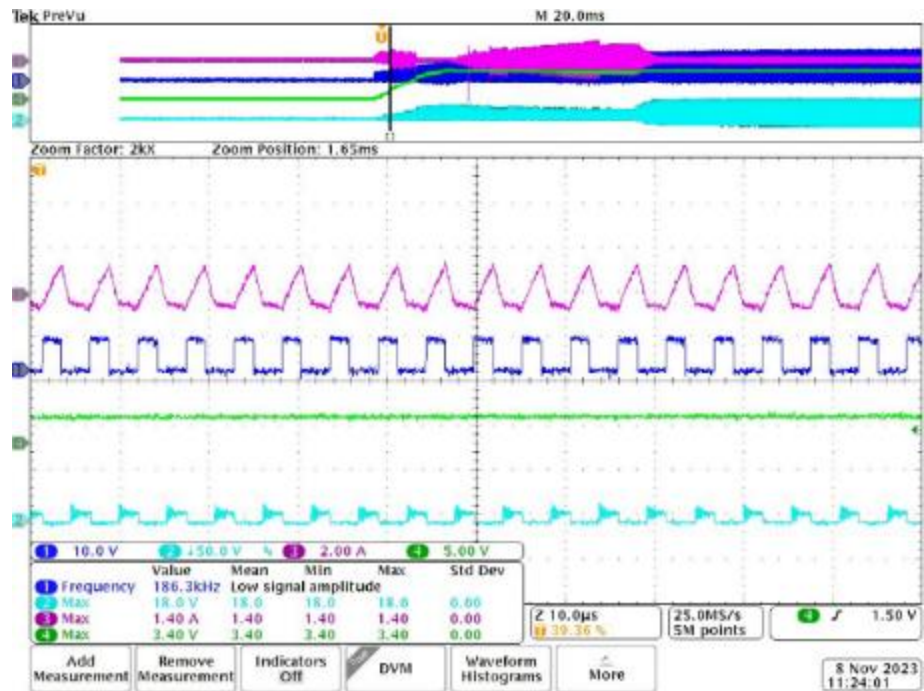


Figure 3.19. APS soft startup at low frequency, from top to bottom: primary side current (2A/div), switch node voltage (20V/div), primary output voltage (10V/div), secondary diode voltage (50V/div).

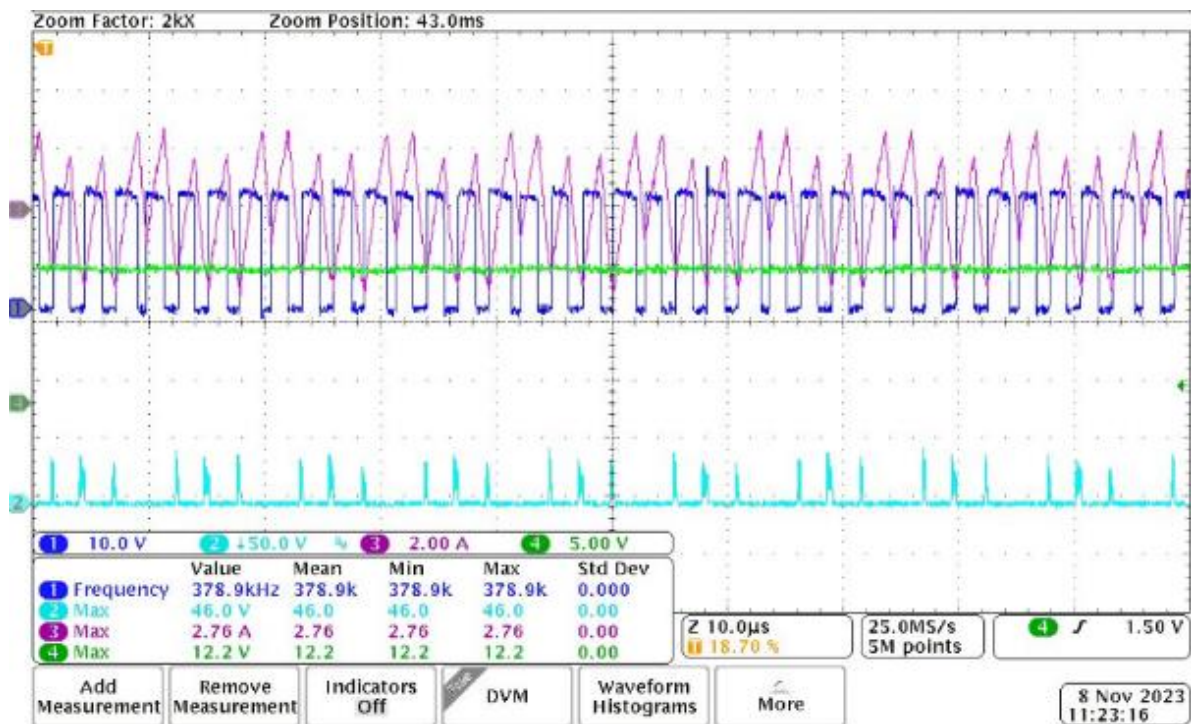


Figure 3.20. APS normal operation at designed frequency, from top to bottom: primary side current (2A/div), switch node voltage (20V/div), primary output voltage (10V/div), secondary diode voltage (50V/div).

3.3.3 APS Mis-trigger Issue

This APS has also been tested with a five-level half bridge MMC. There happens to be a desat protection triggered when the dc voltage reaches 4 kV. Recordings show the APS shuts off itself and then restarts immediately, causing the desat protection to be falsely triggered on the gate driver connected to it.

The basic flyback connection is shown in **Figure 3.21**, and the values are listed in **Table 3-6**. To enhance the system's immunity to EMI, a small capacitance of 80 pF was initially placed in parallel with the feedback resistance R_2 , to filter out noise that could couple into the primary side of the circuit. This noise reduction approach worked effectively until the DC voltage increased to 10 kV, at which point the system experienced instability. To address this, the original 80 pF capacitance was replaced with a larger 470 pF capacitance, which improved the system's performance. With this adjustment, the APS successfully operated under DC voltages up to 12 kV without any issues.

However, it was found that increasing the capacitance further to 1 nF caused the APS to fail to start up properly. This issue likely arises because the increased capacitance reduces the stability of the internal feedback loop, potentially leading to oscillations or delayed responses within the control system. Therefore, while increasing the capacitance beyond 470 pF initially improved the EMI immunity, further increases could compromise the APS's operation stability and startup reliability.

To examine the impact of CM current on the feedback voltage, a flyback model with CM (common mode) propagation path is built in LTspice as shown in **Figure 3.22**, where C3 (1 pF) represents the interwinding capacitance between the transformer primary side and the secondary side. V4 is a PWM voltage source that simulates the dv/dt of 25 V/ns, and the frequency is the power module switching frequency. The red arrow signals the CM propagation path. L1 (1 nH) represents the parasitic inductance in the path. Vfb is the feedback voltage.

When there is no CM source, Vfb reflects the change of the primary inductor current (I_{l2}) as shown in **Figure 3.23**. And the primary switch off time is terminated by the feedback voltage falling below the reference voltage.

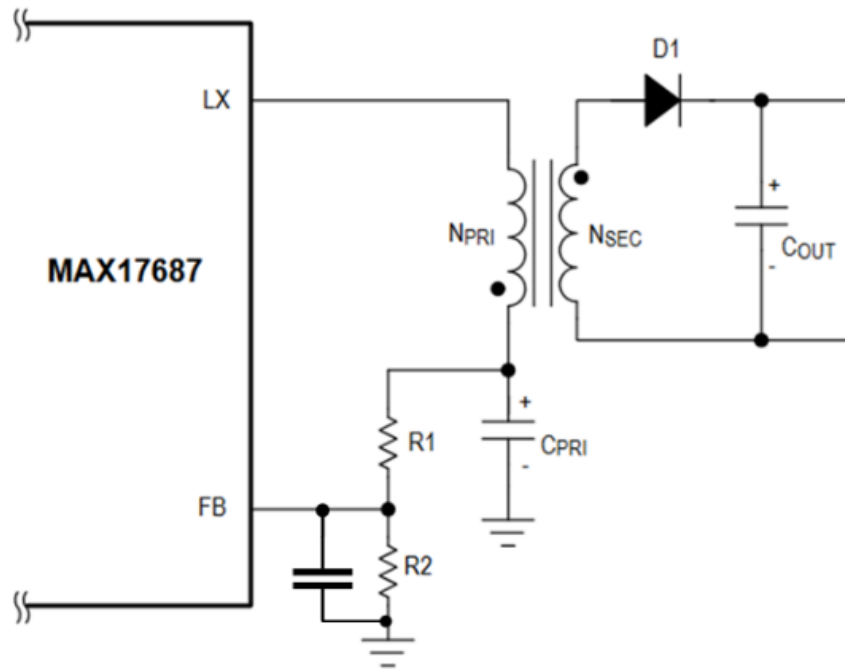


Figure 3.21. Feedback resistance network of a flyback converter.

Table 3-6. Flyback APS specifications.

Parameter	Values
N _{PRI}	5
N _{SEC}	12
R1	24.9 k Ω
R2	2 k Ω
C _{PRI}	22 μF
C _{OUT}	50 μF

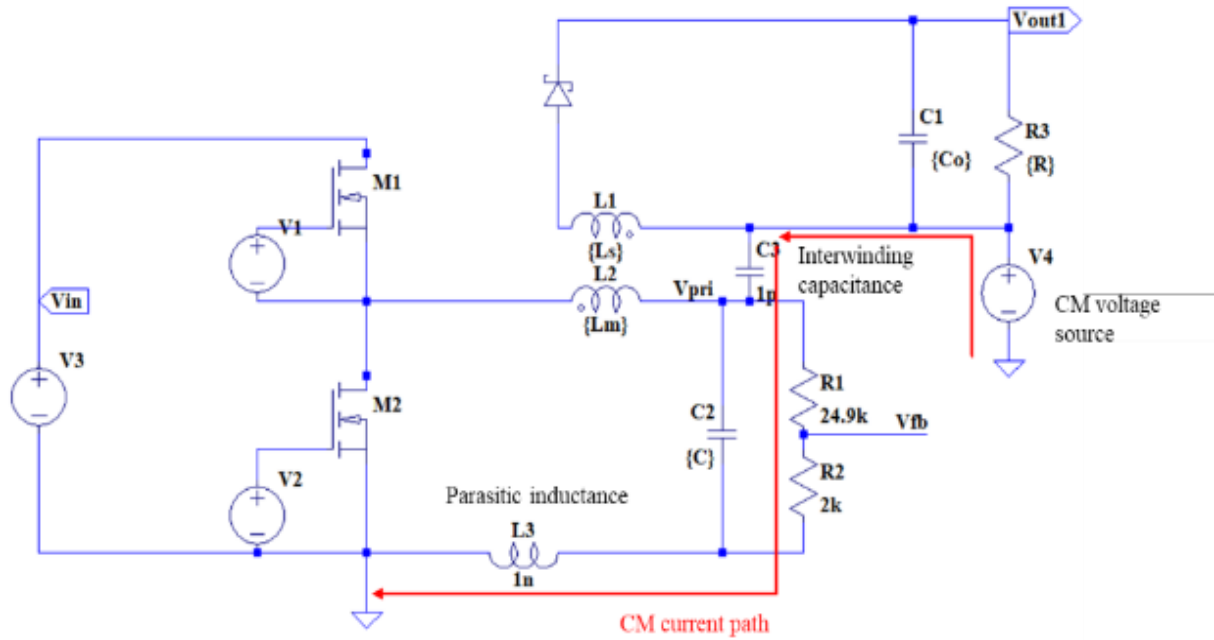


Figure 3.22. Flyback model with CM propagation

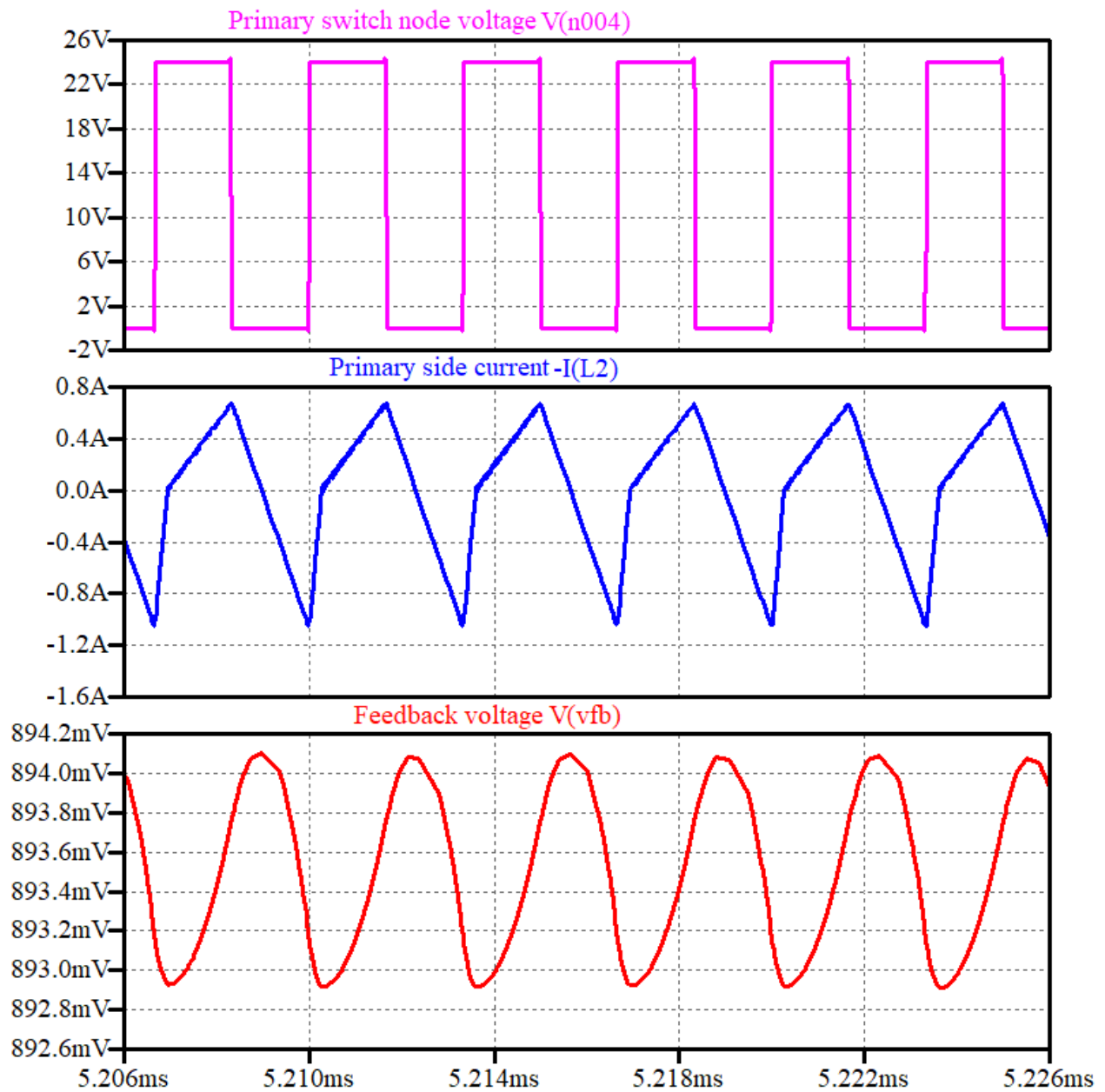


Figure 3.23. Feedback voltage changes monotonically with primary current.

When there is a common mode source, the CM current flows through C3 and R2, causing voltage spikes on the feedback voltage in **Figure 3.24**. If the voltage spike (1.6 V) overlaps with the feedback voltage valley point, it is likely to cause an interference with the control and eventually shut down the flybuck converter.

This simulation reveals the critical role of common-mode currents in flybuck converters. The coupling between the primary and secondary sides through parasitic capacitance can lead to voltage spikes on the feedback path. If not properly mitigated, these spikes can cause false triggering or unintended shutdown of the converter, highlighting the need for effective filtering and mitigation techniques to prevent CM interference and ensure stable operation of the flybuck converter.

3.4 Summary

This chapter addresses key design challenges of high-voltage APS for MV applications, with the following contributions:

- **Insulation Design:** The transformer's internal electric field distribution is analyzed to guide insulation layout, while clearance and creepage requirements between external PCBs are evaluated to ensure high-voltage safety compliance.
- **Interwinding Capacitance Optimization:** Comparative analysis of core geometries reveals that toroidal and U-cores yield lower interwinding capacitance than E-cores due to reduced winding-core overlap. Generalized design principles—minimizing winding turns, overlap, and inter-winding proximity—are established.
- **Fault Protection in Series LLC APS:** Fault analysis shows that short or open-circuit conditions affect voltage gain across outputs. Secondary-side protection is demonstrated to provide more effective isolation and voltage stability than primary-side protection across varying loads.
- **EMI Resilience in Multilevel Converters:** Flybuck APS behavior under strong EMI is examined in a multilevel MV converter environment. EMI-induced shutdown/restart issues are mitigated via feedback circuit filtering, enhancing system robustness without impairing control performance.

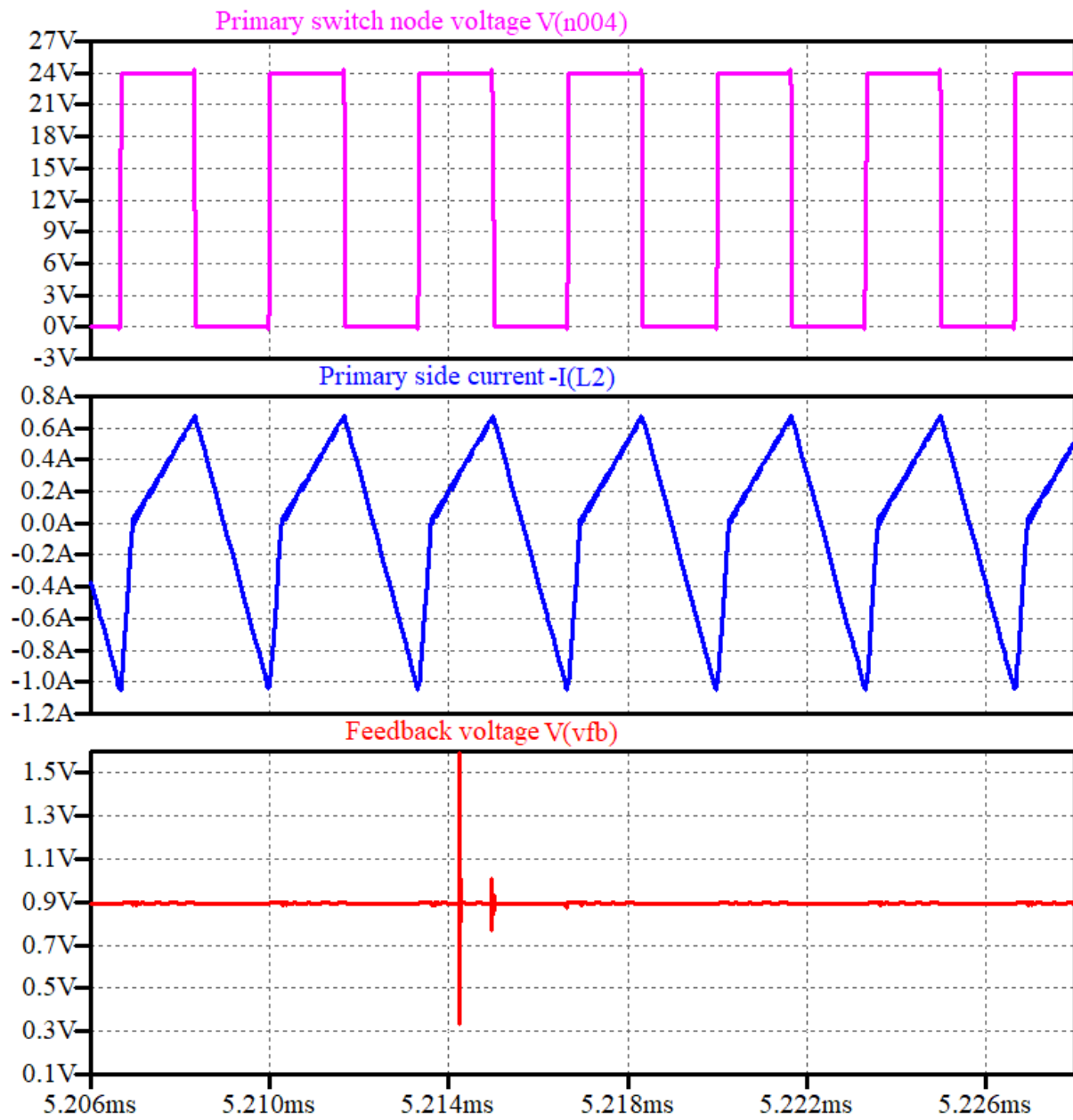


Figure 3.24. CM current causes feedback voltage spikes.

Chapter 4 TSEP Selection for 10 kV SiC MOSFET Power Modules

Temperature sensitive electric parameters (TSEPs) for 10 kV SiC MOSFET power modules are investigated in this chapter to examine potential candidates for online temperature monitoring. The ideal TSEP should change linearly with the temperature with sufficient sensitivity. Two categories of TSEPs are discussed to analyze the intrinsic temperature characteristics of 10 kV SiC MOSFET power modules: (1) during steady state and (2) during a switching transient state (ON to OFF or OFF to ON). Also, TSEP comparison with low voltage (1200 V) SiC MOSFETs is provided to identify the uniqueness of high voltage SiC MOSFET power modules. Part of the content in this chapter is from the author's conference paper published in *IEEE ECCE 2023* [125].

4.1 Static TSEP

The power module investigated is a Wolfspeed XHV-9 10 kV SiC MOSFET half-bridge module (shown in **Figure 4.1**). Each device has six dies in parallel; the detailed specifications are given in **Table 4.1**. Static tests are conducted using curve tracer Keysight B1505A to measure forward conduction, reverse conduction, and transfer characteristics. Junction capacitance, which includes gate source capacitance, gate drain capacitance, and drain source capacitance, remains stable across a wide temperature range, so they are not normally considered for TSEPs.

4.1.1 Forward Conduction Characteristics

The curve tracer is used to exert controlled duration and magnitude of gate source and drain source voltage pulses to the power module. The forward conduction test is conducted by limiting V_{ds} to less than 25 V and i_{ds} to less than 110 A; V_{gs} is swept from 1 V to 15 V in 1 V steps. In this way, the full operation range of normal working conditions is measured without exposing the power module to excessive power and current. The forward conduction curve at 25°C is presented in **Figure 4.2**. The same test is repeated under 25°C, 50°C, 75°C, 100°C (**Figure 4.3**) and 125°C by placing the power module on a hotplate with controlled temperature.

The ON-resistance at different temperatures when V_{gs} is 15 V are summarized in **Figure 4.4**. It is observed that the ON-resistance increases as the temperature rises; however, the rate of increase is not uniform across all temperature ranges. This behavior can be attributed to variations in carrier mobility and scattering mechanisms at different temperatures. The increase



Figure 4.1. Wolfspeed XHV-9 10 kV 100A SiC MOSFET power module.

Table 4-1. Parameters of the XHV-9 10 kV SiC MOSFET Module.

Static parameters	Wolfspeed XHV-9 SiC MOSFET Module
Minimum Breakdown voltage	10 kV @ $V_{gs} = 0$ V, $I_d = 6$ mA
ON state resistance	50 mΩ @ $V_{gs} = 15$ V, $I_d = 90$ A, $T_j = 25^\circ\text{C}$
Maximum junction temperature	175 °C

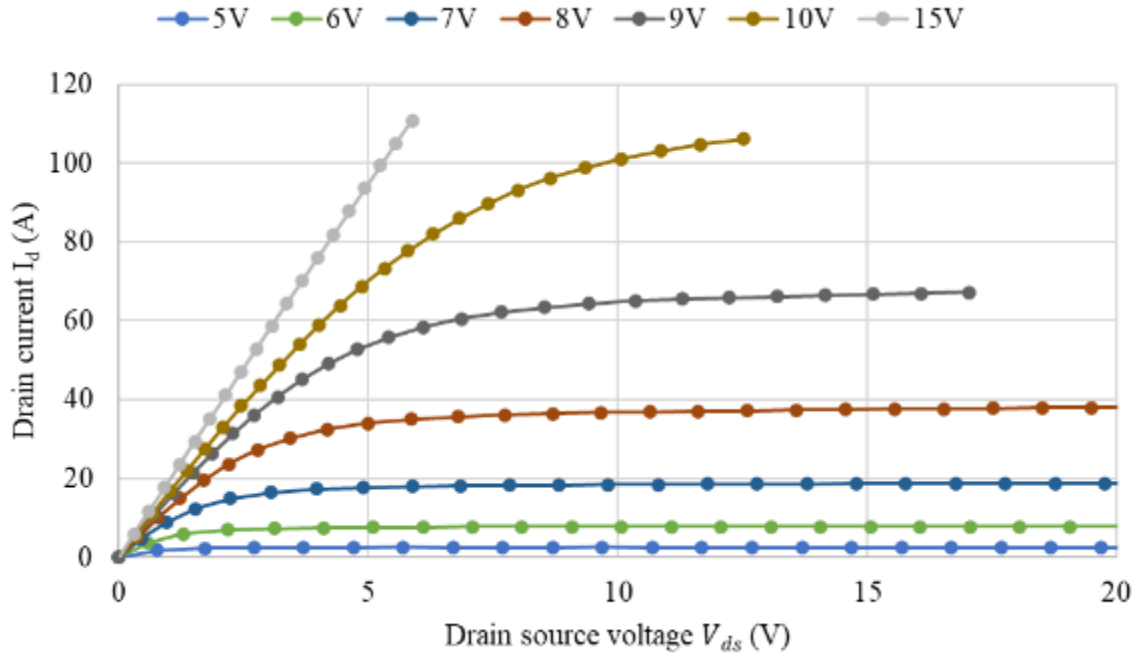


Figure 4.2. Forward conduction curves of the 10 kV SiC MOSFET module at 25°C.

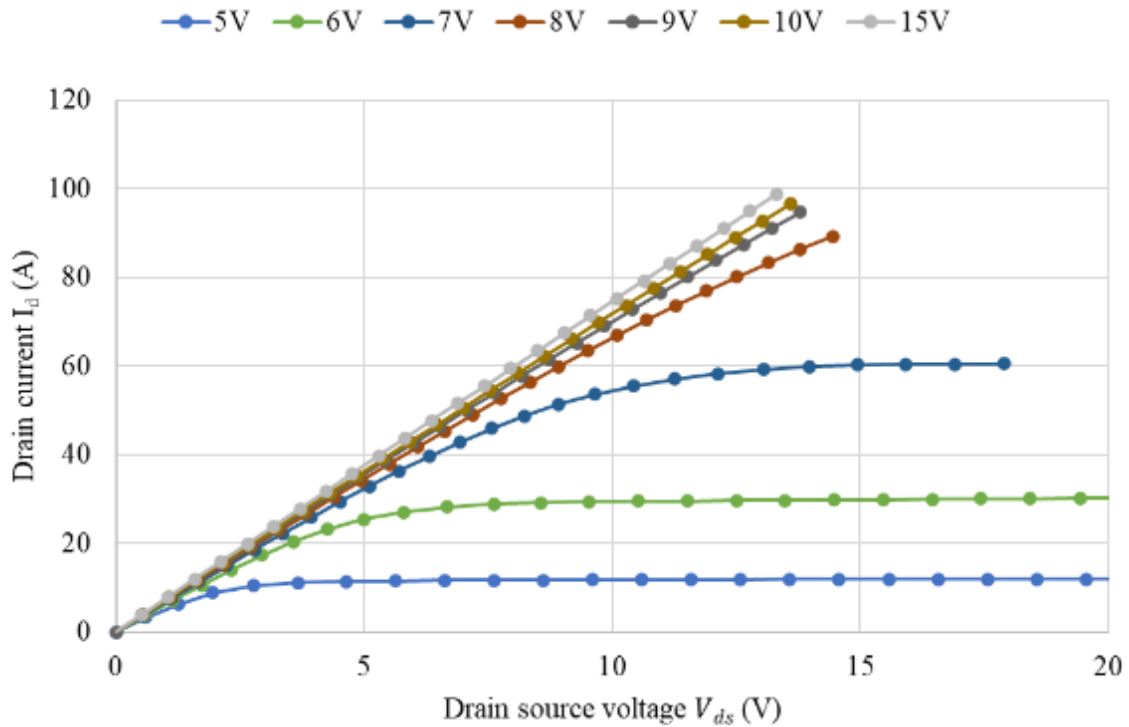


Figure 4.3. Forward conduction curves of the 10 kV SiC MOSFET module at 125°C

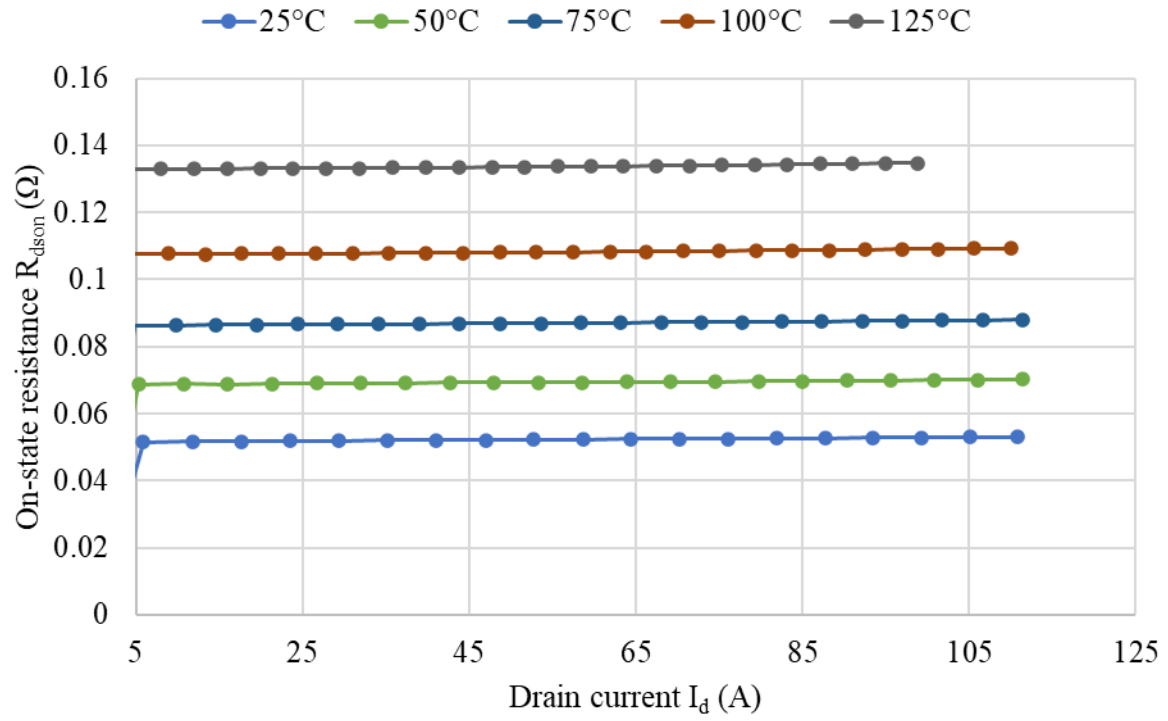


Figure 4.4. ON-resistance of the 10 kV SiC MOSFET module at different temperatures.

in resistance can lead to higher conduction losses in power devices, which is an important consideration in thermal management and efficiency optimization.

Additionally, the threshold voltage V_{th} decreases with increasing temperature as presented in **Figure 4.5**. This reduction is primarily due to the positive temperature dependence of the intrinsic carrier concentration, which leads to increased carrier generation and a subsequent shift in the threshold voltage.

4.1.2 Reverse Conduction Characteristics

The reverse conduction curve is measured in a similar process to the forward conduction curve. V_{gs} is stepped from 1 V to 15 V with 2 V steps. V_{ds} is limited to -15 V and i_{ds} is limited to -110 A.

In SiC MOSFET reverse conduction characterization, limiting V_{ds} to -15 V prevents device breakdown and ensures operation within the safe operating area (SOA). Although SiC MOSFETs feature a robust body diode to support reverse current, they are not designed to sustain high reverse bias voltage under gate control. The reverse conduction curve at 25°C is presented in **Figure 4.6**.

4.1.3 Transfer Characteristics

In **Figure 4.7**, i_d is measured when $V_{ds} = 10$ V and V_{gs} is stepped from 1 V to 15 V. A low drain-source voltage is used in transfer characteristic measurements to ensure that the drain current is predominantly controlled by the gate-source voltage, minimizing the influence of V_{ds} on the inversion layer electron mobility. Transconductance, shown in **Figure 4.8**, increases with temperature when the current is below 40 A, but deviates from linearity at higher current levels.

4.2 Dynamic TSEP

4.2.1 Experimental Test Setup

The DPT schematic is shown in **Figure 4.9**. The DPT platform shown in **Figure 4.10** was built to test 10 kV half bridge power module switching characteristics. The key components are described as follows. The DC link capacitor consists of four 2 kV 360 μ F capacitors in series. The DC link voltage can be adjusted from 0 to 7 kV. Due to the parasitic inductance in the commutation loop, a decoupling capacitor board is used to limit the device voltage overshoot. The load inductance is 5 mH.

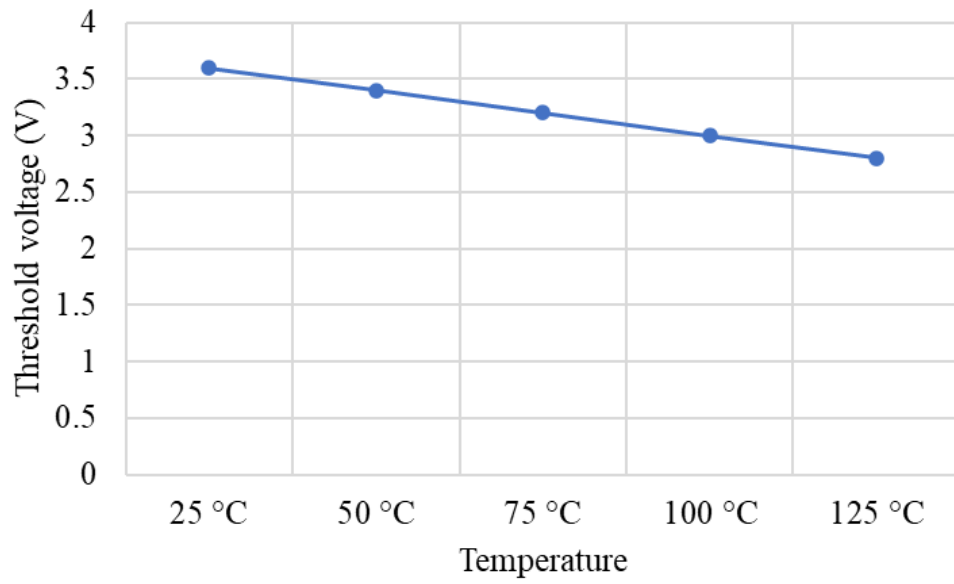


Figure 4.5. Threshold voltage decreases with increasing temperature in the 10 kV SiC MOSFET module.

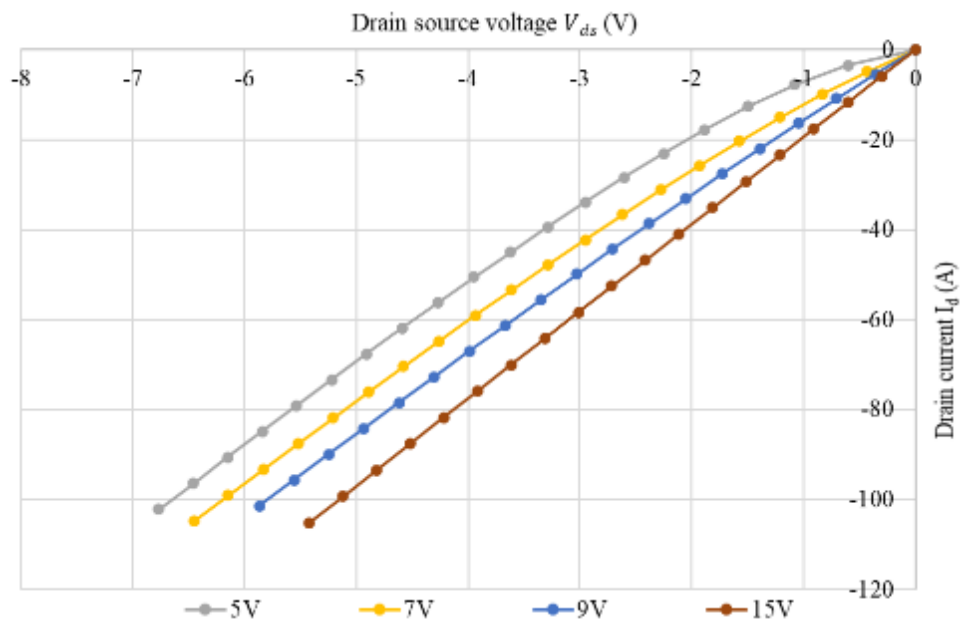


Figure 4.6. Reverse conduction curves at 25 °C of the 10 kV SiC MOSFET module.

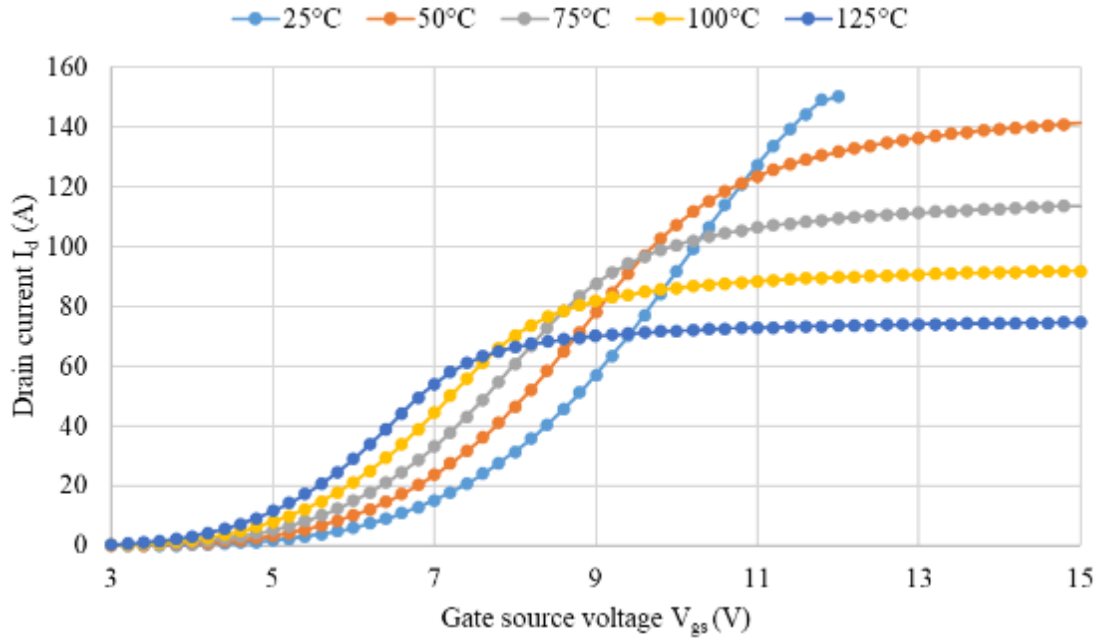


Figure 4.7. Transfer characteristics of the 10 kV SiC MOSFET module at different temperatures.

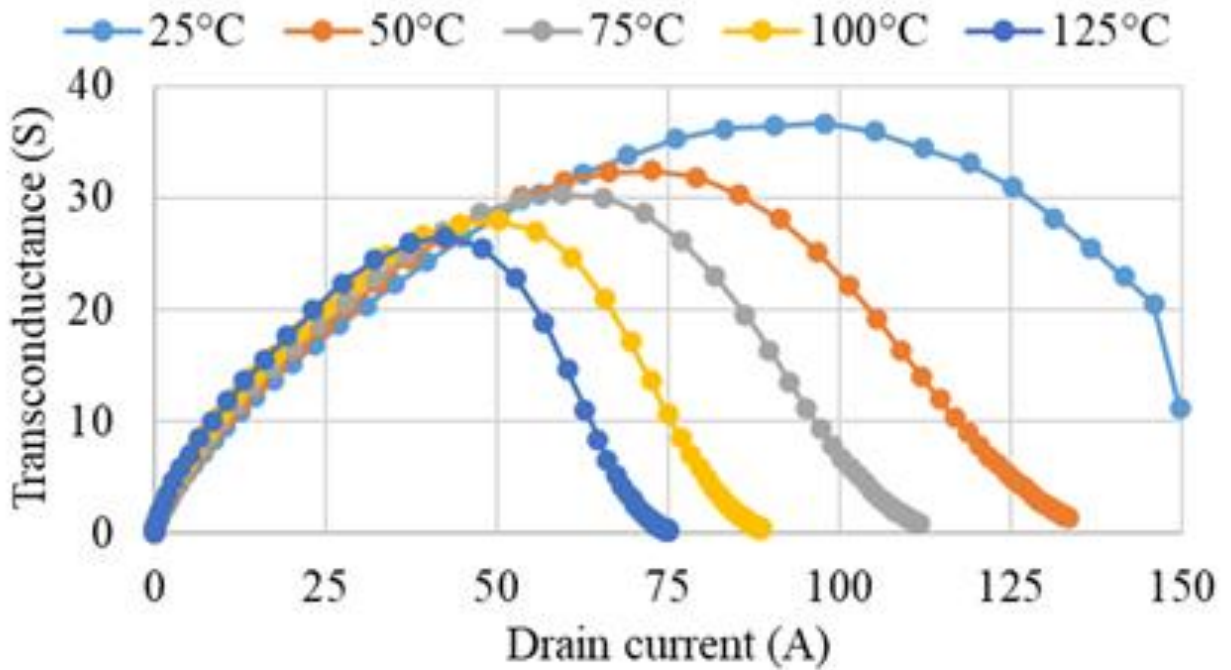


Figure 4.8. Transconductance of the 10 kV SiC MOSFET module at different temperatures.

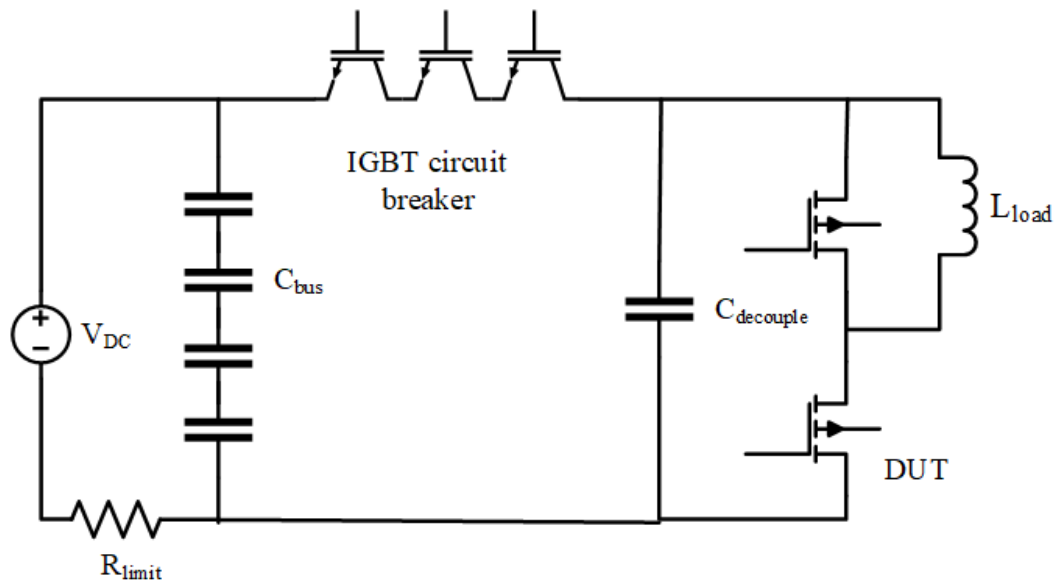


Figure 4.9. DPT circuit scheme for testing 10 kV SiC MOSFET module.

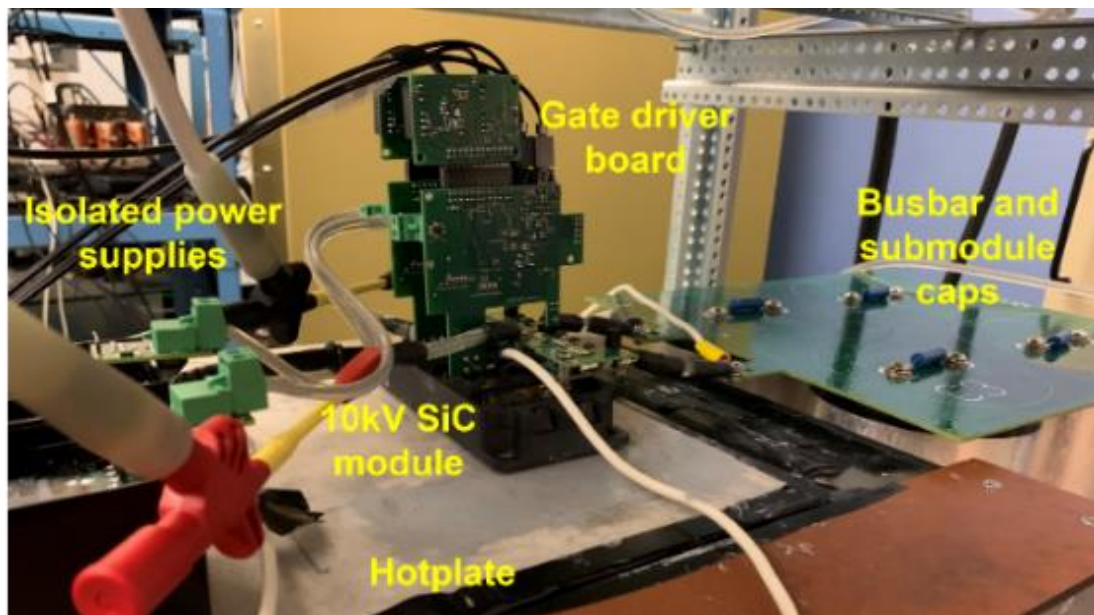


Figure 4.10. DPT experiment setup.

A circuit breaker with three Si IGBTs in series is connected in the main circuit to limit the maximum current in case a short circuit happens during testing. The dedicated gate driver receives control signals and transmits a feedback signal by optical fiber, connecting to the controller outside of the high voltage room. This provides high voltage isolation and ensures signal integrity and personnel safety. The gate driver has desat protection integrated, which protects the power module from short circuit faults. Gate turn-on voltage is 15 V and turn-off voltage is -5V. Gate resistance is 5 Ω for both turn-on and turn-off modes. The auxiliary power supply that provides power to the gate driver has a 10 kV isolation and 2 pF interwinding capacitance [126].

The measurement probes with sufficient bandwidth and isolation are used. Drain source voltage is measured by high voltage differential probe DP20-10k (17.5 kV, 120 MHz). Device current is measured by PEM CWTMini50HF Rogowski coil (50 MHz). Gate source voltage is measured by TPP1000 Tektronix passive voltage probe (1 GHz).

4.2.2 Turn on Transient TSEP

TSEP during the switching process is divided into two groups: (1) TSEP during the turn on transient, and (2) TSEP during the turn off transient. Normally, turn on delay time, current rise rate, and drain source voltage drop time are temperature dependent. These data can be extracted from DPT results. **Figure 4.11** shows the typical turn on waveform conducted at 6.5 kV, 57 A.

4.2.2.1 Turn-on Delay Time

During turn-on delay time, the device is in the cutoff region, C_{gs} charges from 0 V to V_{th} . Turn on delay time t_{don} in (4.1) measures the time when i_d starts to conduct after the gate source voltage is applied to the device. Here, V_{cc} is turn on gate voltage, and V_{ee} is turn off gate voltage. R_g is gate resistance and C_{iss} is the input capacitance of the power module. From the previous analysis, the threshold voltage drops with increasing temperature, t_{don} decreases as it takes a shorter time for C_{gs} to charge to V_{th} .

$$t_{don} = R_g C_{iss} \ln \left(\frac{V_{cc} - V_{ee}}{V_{cc} - V_{th}} \right) \quad (4.1)$$

4.2.2.2 Current Rise Time

As soon as the gate source voltage reaches V_{th} , the device starts conducting. The current rise time t_{ir} can be derived from (4.2), where I_L is load current and g_m is transconductance.

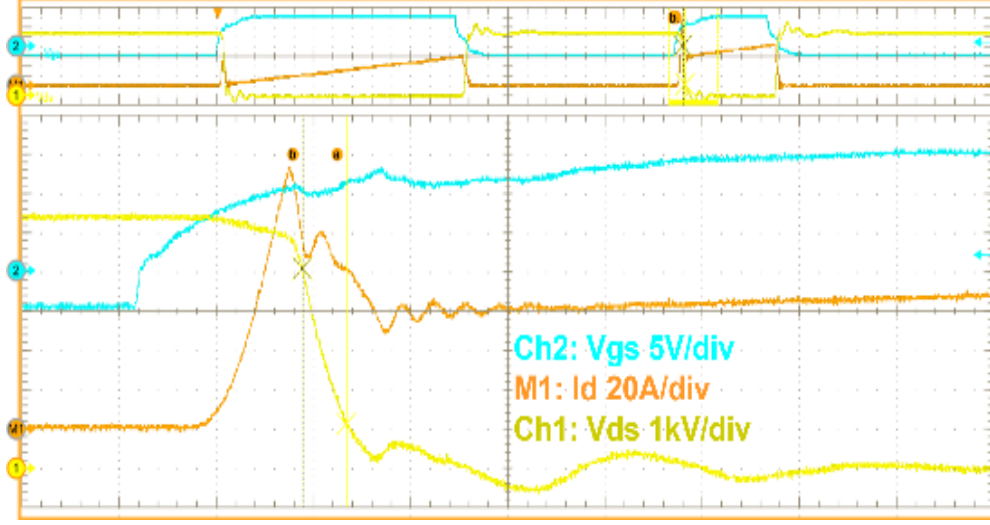


Figure 4.11. Turn on switching transient at 6.5 kV 57 A in 10 kV SiC MOSFET module.

$$t_{ir} = R_g C_{iss} \ln \left[\frac{V_{cc} - V_{th}}{V_{cc} - V_{th} - \frac{I_L}{g_m}} \right] \quad (4.2)$$

4.2.2.3 Voltage Fall Time

Drain source voltage starts to fall from the nonconducting high voltage the moment V_{gs} reaches the miller plateau and C_{gd} starts discharging. Thus, the drain source voltage fall time t_{vf} is given in (4.3), where Q_{gd} is gate charge.

$$t_{vf} = \frac{R_g Q_{gd}}{V_{cc} - V_{th} - \frac{I_L}{g_m}} \quad (4.3)$$

V_{th} has a negative temperature coefficient. g_m is also affected by temperature, but in this case and unlike the value measured by the curve tracer where the drain source voltage equals 10 V, the actual drain source voltage is several kilovolts during the switching transient of DPT.

According to [127], transconductance varies significantly with (V_{ds}), ranging from 20 V to 7 kV. However, its specific temperature dependency under these high-voltage conditions remains unclear. Due to this uncertainty, deriving a precise relationship between the observed parameters and temperature purely through theoretical equations is challenging. Instead, experimental validation is necessary to accurately determine the impact of temperature on these parameters in high-voltage switching conditions.

From test results in **Figure 4.12**, t_{don} , t_{cr} and t_{vf} decrease linearly with increasing temperature. The junction temperature (°C) in relation to TSEP (ns) is shown as follows; they all show pretty good linearity. Voltage fall time has the best temperature sensitivity because of the largest coefficient.

$$T = -0.268t_{vf} + 66.52 \quad (4.4)$$

$$T = -0.131t_{cr} + 16.47 \quad (4.5)$$

$$T = -0.262t_{don} + 27.19 \quad (4.6)$$

4.2.3 Turn off transient TSEP

4.2.3.1 Turn-off Delay Time

Turn-off delay time t_{doff} measures the time from the instant when gate-source voltage drops to the instant when drain-source voltage starts to increase from zero.

$$t_{doff} = R_g C_{iss} \ln \frac{V_{cc} - V_{ee}}{V_{th} + \frac{I_L}{g_m} - V_{ee}} \quad (4.7)$$

As threshold voltage is negatively correlated with temperature, and transconductance is nonlinearly dependent on temperature, it is difficult to derive from equation (4.7) alone the relation between turn-off delay time and temperature. From the experiment results in **Figure 4.13**, when $R_g = 5 \Omega$, turn-off delay time has a small variance of less than 5% across the entire temperature range for currents between 16.6 A and 47.8 A. This indicates that within this current range, temperature effects on turn-off behavior are relatively stable, likely due to compensating factors such as charge carrier dynamics and switching characteristics.

However, at lower (7.1 A) and higher (56.9 A) current levels, the turn-off delay exhibits a nonlinear dependence on temperature. This deviation suggests that additional temperature-dependent factors, such as carrier trapping, nonlinear changes in device capacitances, or variations in switching losses, become more prominent at the current extremes.

4.2.3.2 Voltage Rise Time

The turn-off transient of this 10 kV SiC power module is dominated by load current charging/discharging the device junction capacitances. As the device capacitance is temperature independent, most parameters are not affected by temperature. The voltage rise time has stable duration regardless of the temperature change. In **Figure 4.14**, voltage rise time difference across full temperature range from 25°C to 125°C is less than 4% when load current is less than 20 A.

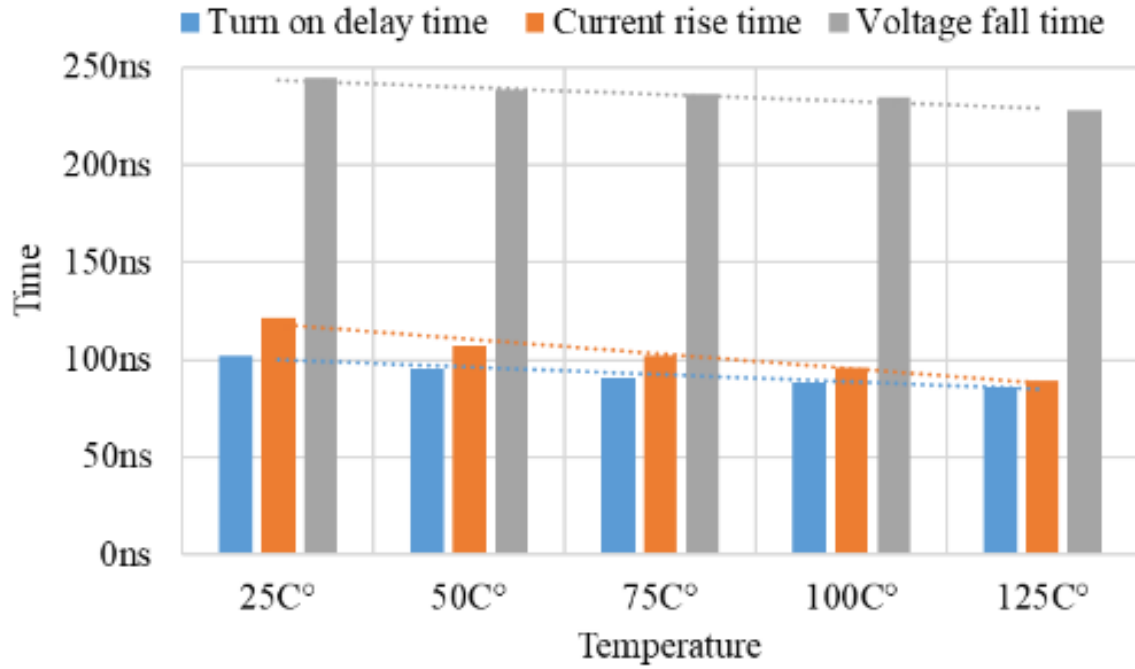


Figure 4.12. t_{don} , t_{cr} , t_{vf} decreases with increasing temperature in 10 kV SiC MOSFET module.

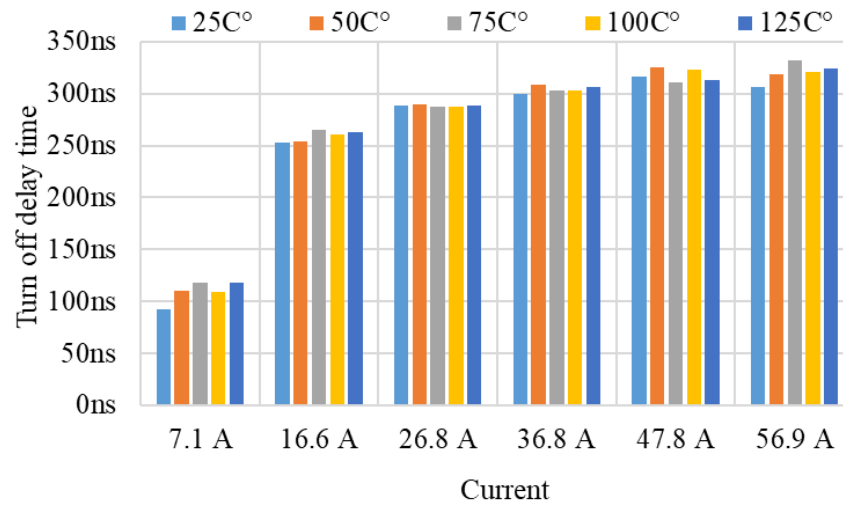


Figure 4.13. Turn off delay time at $R_g = 5 \Omega$ is similar at different temperatures in 10 kV SiC MOSFET module.

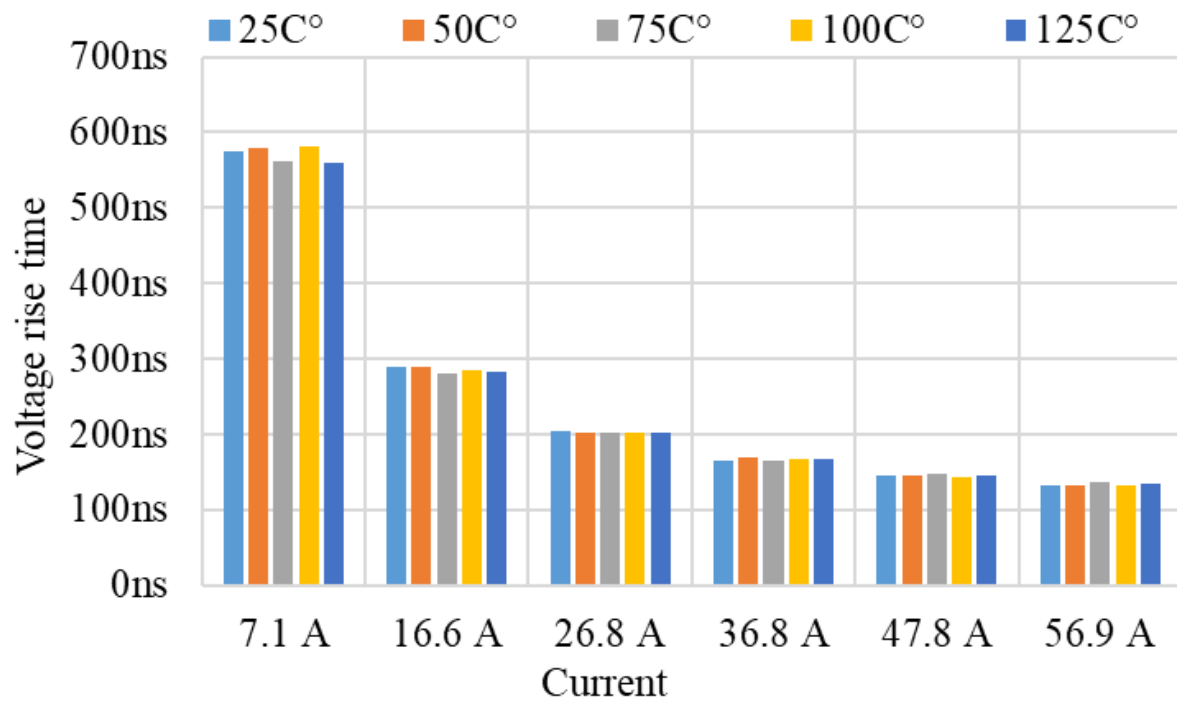


Figure 4.14. Voltage rise time at $R_g = 5 \Omega$ is similar at different temperatures in 10 kV SiC MOSFET module.

When load current is larger than 20 A, it is less than 5 ns. Voltage slew rate dv/dt corresponds with voltage rise time and is also temperature insensitive.

The same phenomenon is also observed in voltage overshoot V_{os} as shown in **Figure 4.15**. The experimental results indicate that the turn-off delay time does not exhibit a clear, consistent relationship with temperature across all operating conditions. This lack of a distinct correlation suggests that multiple factors influence the turn-off dynamics, including variations in threshold voltage, transconductance, and device capacitances, all of which respond nonlinearly to temperature changes.

For the 10 kV SiC MOSFET module under study, the turn-off delay time is found to be a reliable temperature-sensitive electrical parameter (TSEP) only under specific conditions. At a relatively fast switching speed—achieved with a small gate resistance ($\leq 2 \Omega$)—and a considerable load current (≥ 10 A), the turn-off delay time demonstrates a measurable and predictable temperature dependence. This makes it a suitable candidate for temperature estimation in practical applications.

However, under other operating conditions, such as higher gate resistance values or lower load currents, the turn-off delay time shows weak temperature sensitivity or follow nonlinear, inconsistent trends. This limits their usefulness as reliable indicators of device temperature,

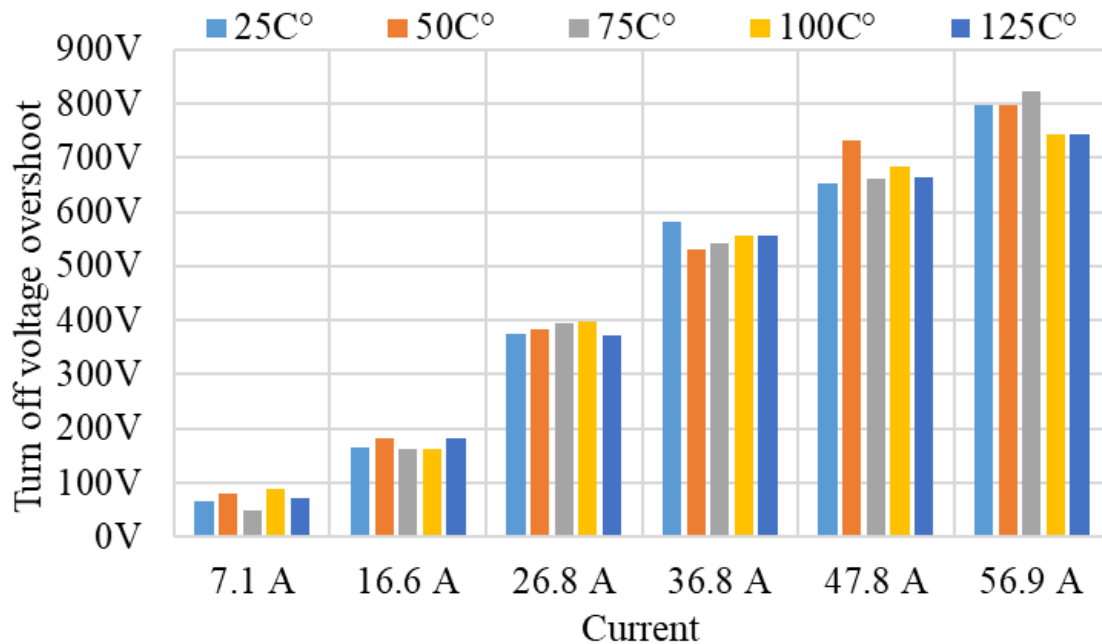


Figure 4.15. Voltage overshoot at different temperatures in 10 kV SiC MOSFET module.

reinforcing the need to carefully select operational parameters when using turn-off delay time for temperature estimation in SiC MOSFET modules.

4.3 Impact Factors

This section discusses other factors besides temperature that impact the electrical parameters measured, especially during switching transients. Gate turn on voltage and turn off voltage affect the switching speed and can be controlled in a versatile way with an intelligent gate driver. In this application, the power module is switched on and off by 15 V and -5 V respectively, so gate voltage impact is not investigated.

4.3.1 Gate Resistance

It is straightforward that gate resistance has a positive impact on t_{don} , t_{ir} , and t_{vf} as shown in (4.1)-(4.4). Thus, gate resistance can be used to increase temperature sensitivity of these TSEP, so it has a larger variance over the same temperature range. It is verified by the test results in **Table 4-2**, where $R_g = 5 \Omega$ and is higher than those measured in **Table 4-3**, where $R_g = 2 \Omega$. Due to 2Ω internal gate resistance, the values measured do not increase proportionally with the gate resistance.

4.3.2 Load Current

The following data are extracted from DPT waveforms at the same DC voltage 6.4 kV with varying current. During the turn-on process, load current does not affect turn-on delay time from theoretical analysis in (4.4). It is verified through test results in **Figure 4.16**, where current increases from 7.1 A to 56.9 A and at the same temperature, the turn-on delay time shows a small variance of less than 10 ns. By contrast, the current rise time increases significantly for this same testing as shown in **Figure 4.17**. In **Figure 4.18**, the voltage fall time gradually decreases with increasing load current, although some deviation is observed at high current levels (≥ 36.8 A).

Our testing of the 10 kV SiC MOSFET power module at 6.5 kV, 55 A aligns with the observations from [128], where a 10 kV power module was tested at 6 kV, 84 A. Specifically, the turn-on dv/dt was found to increase with rising temperature, indicating that the voltage fall time during turn-on decreases as temperature rises. This trend suggests that higher temperatures impact the turn on switching characteristics in a similar manner across different test conditions.

Table 4-2. 10 kV SiC MOSFET Module turn on results at 2 Ω external gate resistance.

Temperature	t_{don} (ns)	t_{cr} (ns)	t_{vf} (ns)
25 C°	67.6	58.0	200.8
50 C°	66.5	57.0	198.8
75 C°	63.0	54.4	199.6
100 C°	62.0	51.0	191.6

Table 4-3. 10 kV SiC MOSFET Module turn on results at 5 Ω external gate resistance.

Temperature	t_{don} (ns)	t_{cr} (ns)	t_{vf} (ns)
25 C°	101.6	121.6	244.4
50 C°	95.4	107.4	238.2
75 C°	90.6	101.8	236.6
100 C°	88.4	96.0	234.6

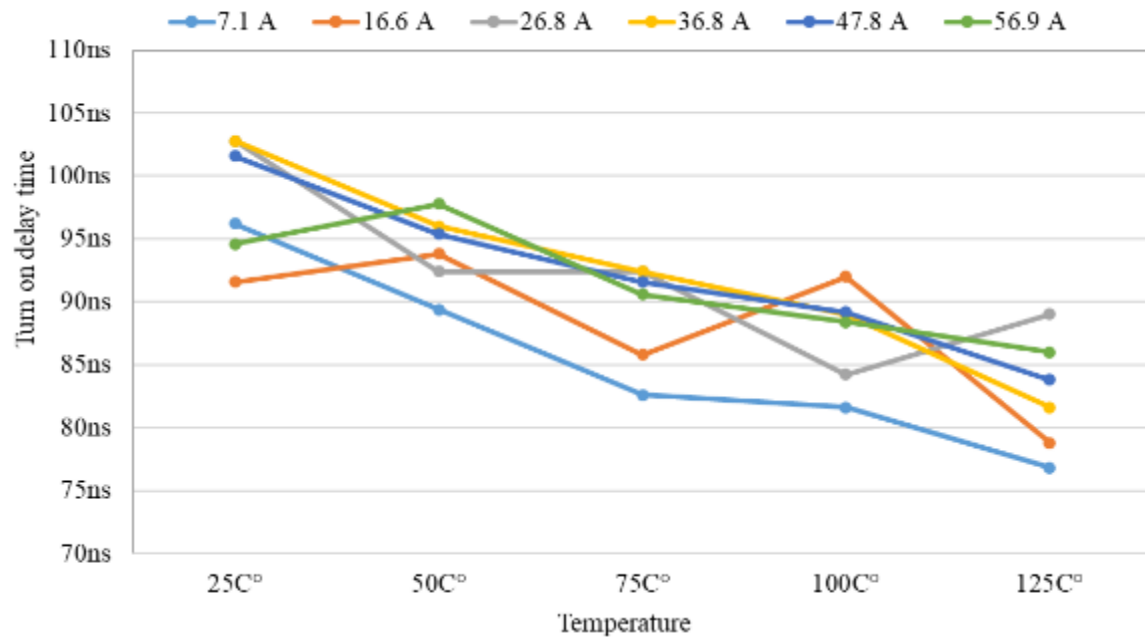


Figure 4.16. t_{don} turn on delay time is independent of current in 10 kV SiC MOSFET module.

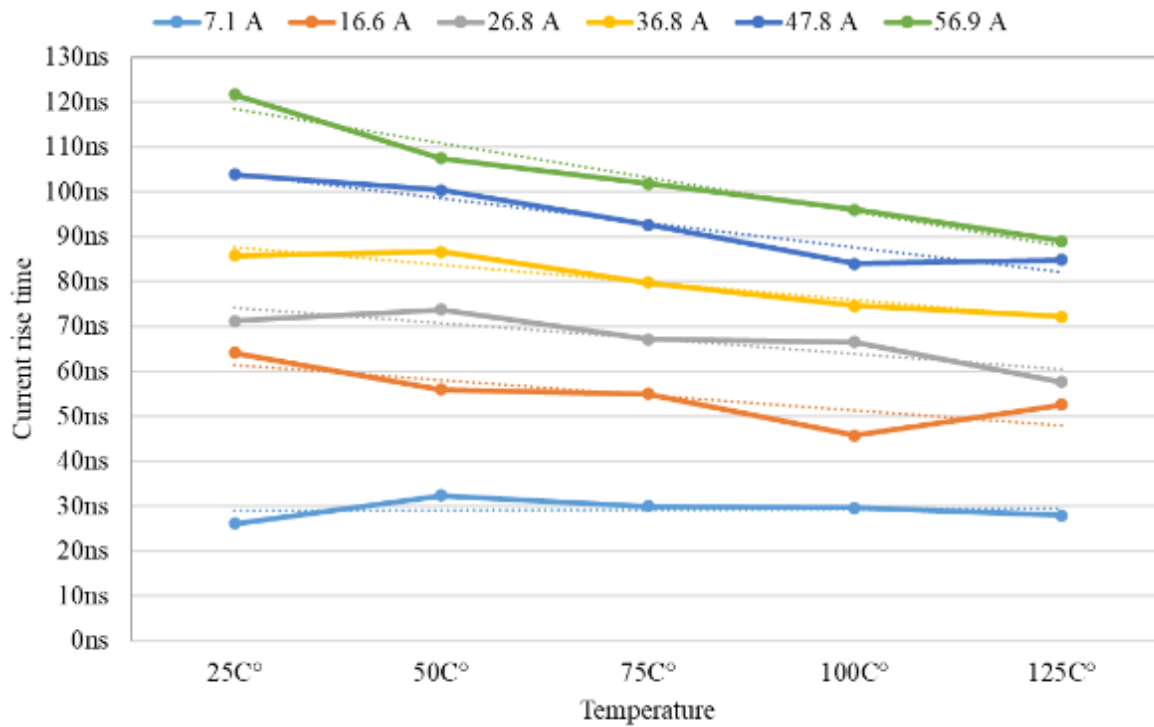


Figure 4.17. t_{cr} current rise time increases with higher current in 10 kV SiC MOSFET module.

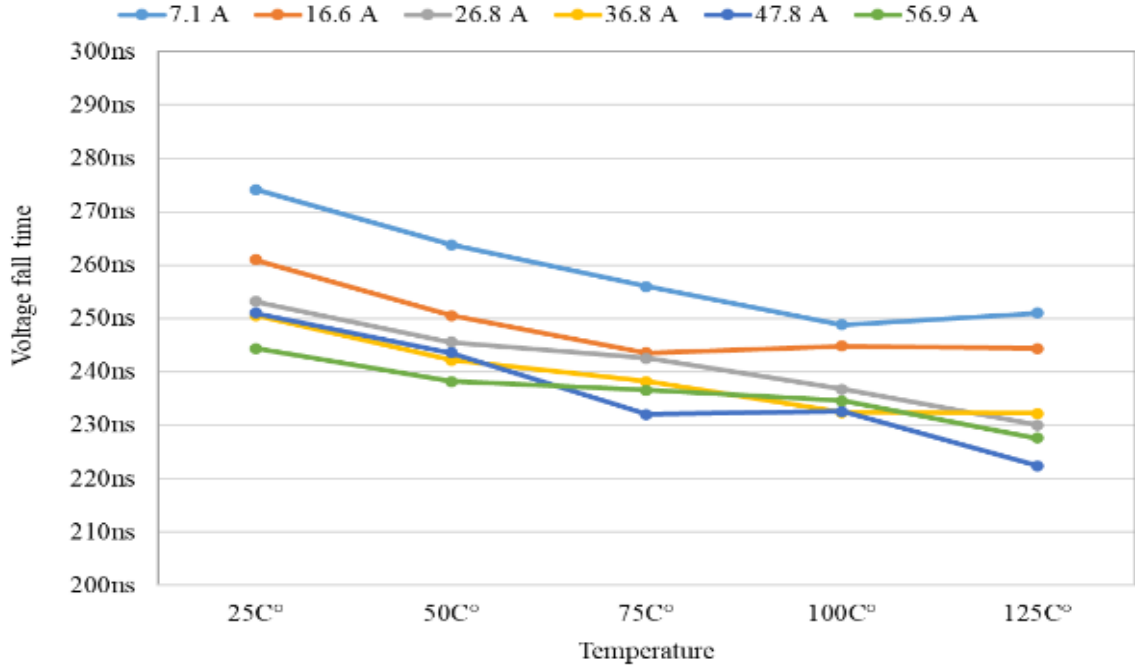


Figure 4.18. t_{vf} voltage fall time decreases with higher current in 10 kV SiC MOSFET module.

For turn off switching transient, [128] also reports that the turn-off dv/dt remains unchanged across the entire temperature range. This consistency indicates that turn-off behavior in 10 kV SiC MOSFET modules is less influenced by temperature variations compared to turn-on transitions. Similar results are also reported in [129], where a 10 kV module was tested at a lower voltage of 4.8 kV. Despite the lower operating voltage, the trends in dv/dt variation with temperature remain consistent, further validating that these switching characteristics are intrinsic to 10 kV SiC MOSFET modules.

4.3.3 Parasitics

Parasitic elements, such as gate loop inductance L_{gs} , power loop inductance L_{loop} , and baseplate capacitance C_{bp} , play a crucial role in influencing switching events. The presence of these parasitic elements can significantly impact the measurement of transient TSEPs, leading to deviations in protection thresholds and potential inaccuracies in temperature estimation.

To analyze these effects, a double-pulse test (DPT) simulation was conducted at 6 kV and 60 A using LTspice with a Wolfspeed SiC module model, systematically varying L_{gs} (10-70 nH), L_{loop} (420-800 nH), and C_{bp} (50-500 pF) to evaluate their impact on key switching characteristics. The simulation circuit is shown in **Figure 4.19**. This comprehensive parametric

study provides critical insights into how parasitic elements affect TSEP reliability in high-voltage applications while establishing design guidelines for parasitic minimization.

4.3.3.1 Gate loop inductance

Gate loop inductance is varied from 10 nH to 70 nH. **Figure 4.20** shows the zoomed in turn-on transient, where $I(Lcs)$ is device current and $V(sw)$ is drain-source voltage. Increasing the gate loop inductance modifies the impedance of the gate drive circuit, which can lead to increased current overshoot and faster switching transients due to reduced damping.

In the examined case, a gate loop inductance of 70 nH results in a shorter current rise time and voltage fall time compared to a 10 nH inductance.

4.3.3.2 Power loop inductance

The power loop inductance is varied from 420 nH to 800 nH, and the turn-on switching transient is illustrated in **Figure 4.21**. It appears that this change has a minimal impact on the turn-on delay time and current rise time. This can be attributed to the fact that the turn-on transient is primarily governed by the gate loop rather than the power loop. Since the gate drive circuit directly controls the gate voltage rise, its effect dominates the switching speed. The power loop inductance increases the voltage fall time, primarily due to the increased impedance in the current path, which slows the rate of voltage change during the turn on transient.

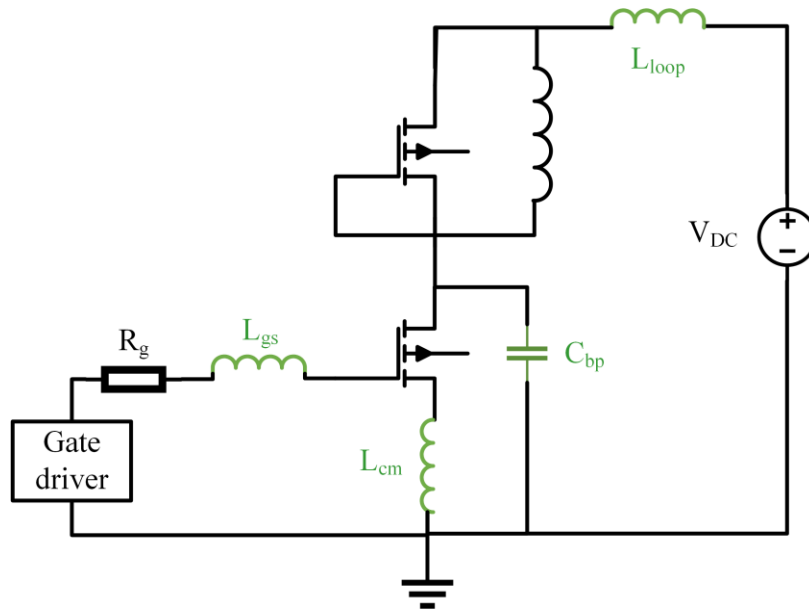


Figure 4.19. DPT circuit model with parasitics highlighted.

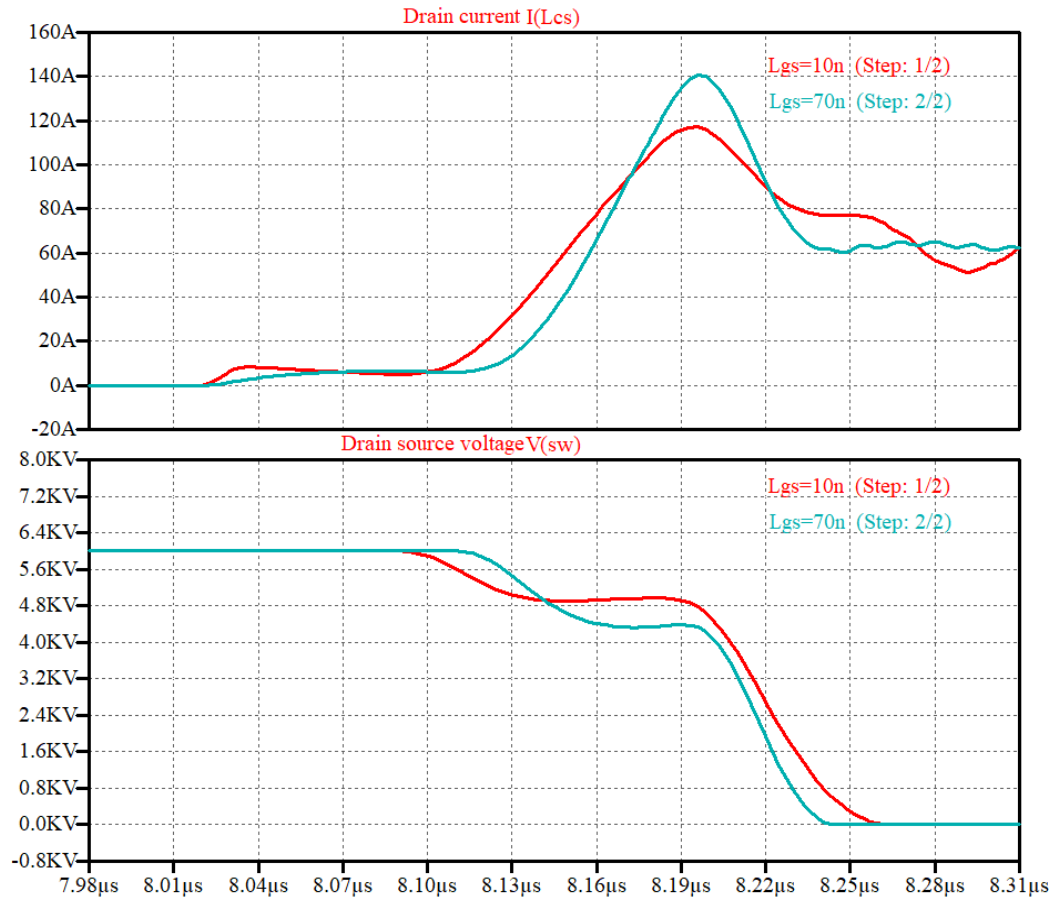


Figure 4.20. Larger L_{gs} leads to higher current overshoot during turn on transient.

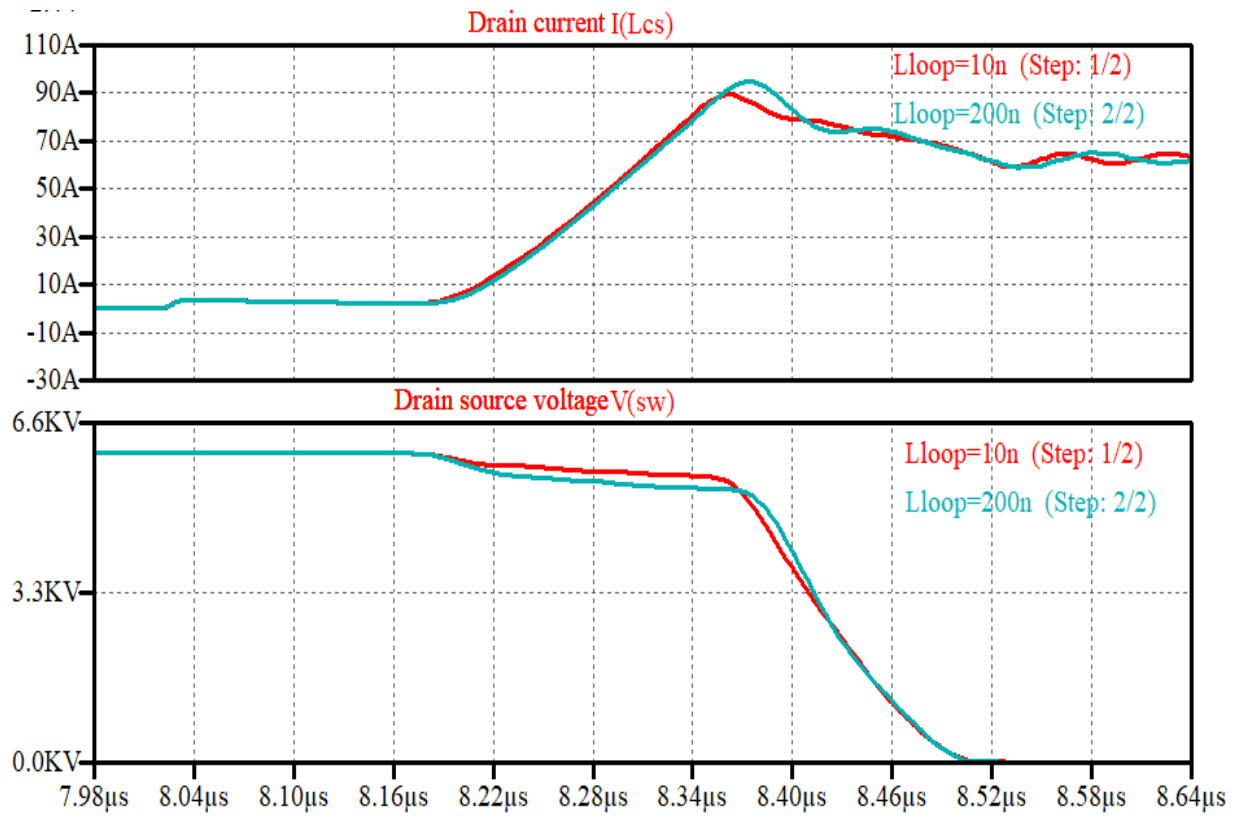


Figure 4.21. L_{loop} slows down voltage drop time during turn on transient.

4.3.3.3 Baseplate capacitance

Baseplate capacitance is changed from 50 pF to 500 pF. **Figure 4.22** shows that baseplate capacitance has a minimal impact on turn-on delay time and current rise time. This suggests that the capacitive coupling between the baseplate and the power circuit does not significantly interfere with the gate drive dynamics or the initial current transition during turn-on.

However, an increase in baseplate capacitance noticeably extends the voltage fall time. This occurs because higher capacitance introduces additional displacement current, which slows down the drain-to-source voltage transition during turn-on. The increased capacitance effectively increases the charge storage, leading to a more gradual voltage drop.

4.4 Comparison with Low Voltage SiC

TSEPs for the Wolfspeed XHV-9 10 kV SiC MOSFET power module are investigated. Among the static parameters, ON-state resistance and threshold voltage can be extracted as TSEPs. While both exhibit temperature dependence, the threshold voltage demonstrates better linearity with temperature, making it a more predictable parameter for temperature monitoring.

For turn-on characteristics, several TSEPs are identified, including turn-on delay time, current rise time, and voltage fall time. All these parameters exhibit negative temperature coefficients, meaning they decrease as temperature increases. Notably, turn-on delay time remains unaffected by load current, making it a more robust TSEP. In contrast, current rise time and voltage fall time are influenced by load current and require calibration to maintain accurate temperature tracking.

For turn-off characteristics, turn-off delay time is the only viable TSEP. Other parameters, such as voltage rise time and current fall time, do not exhibit significant temperature sensitivity, making them unsuitable for temperature estimation.

The temperature sensitivity is summarized in **Table 4-4**. when external gate resistance is 5 ohm. Compared with 3.3 kV, 5 A SiC MOSFET in [10], 10 kV SiC MOSFET power module has the same TSEPs of turn on delay time, current rise time, and turn off delay time.

Turn on current switching rate, which is calculated from current rise time, for a 10 kV, 100 A SiC MOSFET is 1600A/(ms·°C), compared with 328 A/(ms·°C) for a 3.3 kV SiC MOSFET. Turn on delay time is also significantly larger in 10 kV device at -106 ps/°C than -18.6 ps/°C of 3.3 kV device. Threshold voltage temperature sensitivity is also higher than 1.2 kV 30A devices at -

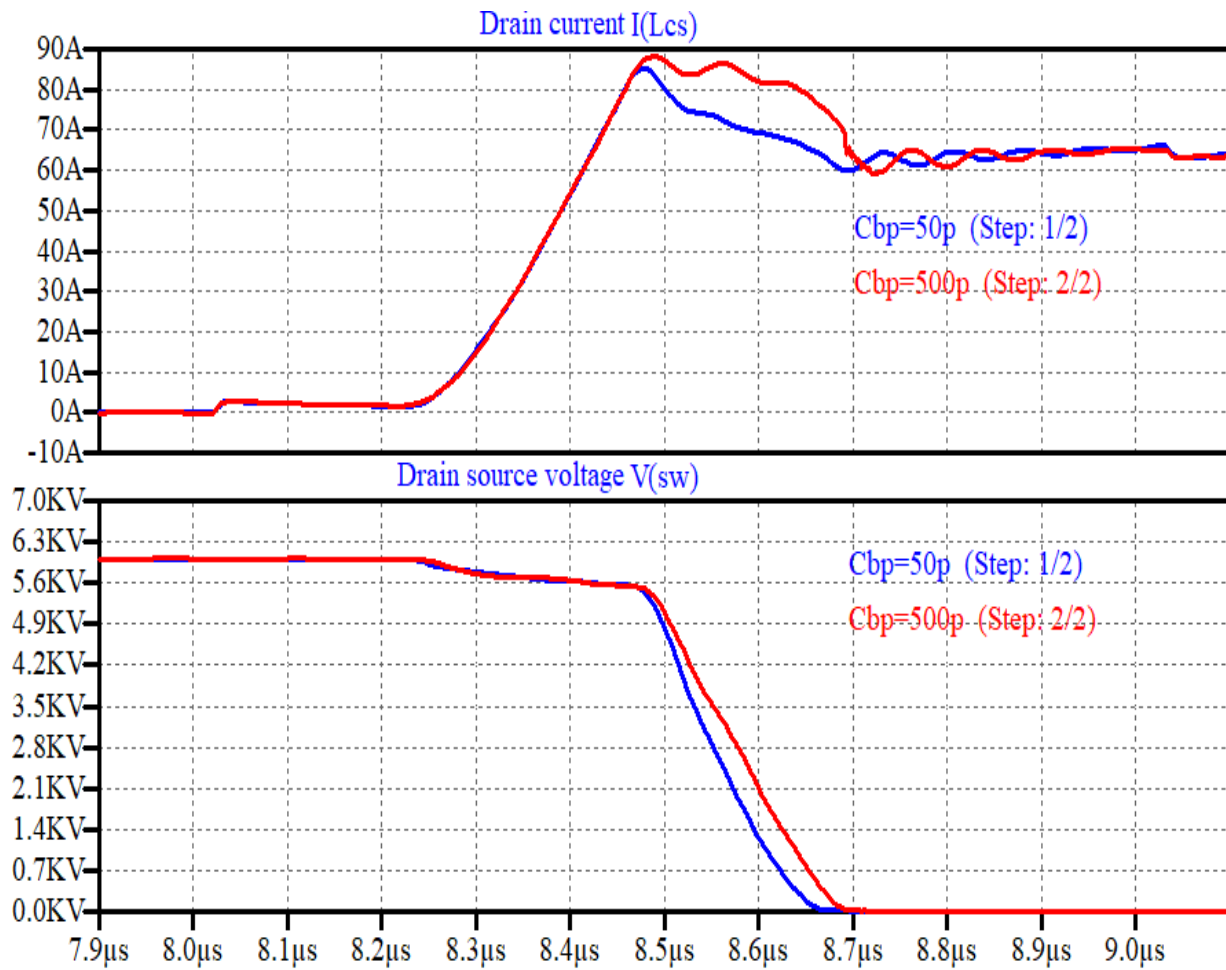


Figure 4.22. Larger C_{bp} increases the voltage drop time during turn on transient.

Table 4-4. Temperature sensitivity of 10 kV SiC MOSFET power module TSEP

TSEP	TSEP Symbols	Temperature Coefficient
Threshold voltage	V_{th}	$-0.08 \text{ V}/^{\circ}\text{C}$
Turn on delay time	t_{don}	$-106 \text{ ps}/^{\circ}\text{C}$
Current rise time	t_{cr}	$-306 \text{ ps}/^{\circ}\text{C}$
Voltage fall time	t_{vff}	$-149 \text{ ps}/^{\circ}\text{C}$

0.005 V/ $^{\circ}\text{C}$ in [9]. Due to the limited data available for SiC MOSFET, only a number of TSEPs can be compared. Unlike 3.3 kV and 1.2 kV devices, voltage slew rate dv/dt , voltage overshoot and switching loss during turn off cannot be selected as TSEPs.

4.5 Comparison with 10 kV Discrete Device

A discrete device rated at 10 kV and 20 A, featuring a single die, has also undergone testing at various temperatures. By doing DPT at 6.8 kV DC voltage and 8 A load current, turn-on parameters were extracted. These parameters, including turn-on delay time, current rise time, and voltage fall time, are presented in **Table 4-5**.

Similar to the 10 kV, 100 A power module, which consists of six dies in parallel, these turn-on parameters exhibit a linear decrease with increasing temperature. This consistent trend confirms their viability as TSEPs, making them useful for temperature monitoring and modeling in both discrete and module based SiC MOSFETs. Linear temperature dependence provides a reliable basis for predicting device performance under varying thermal conditions.

Conversely, turn-off parameters were also derived from the same DPT test. It is evident that the turn-off delay time increases with higher temperatures. However, similar to the power module, voltage rise time and dv/dt remain independent of temperature variations in **Table 4-6**.

This suggests that, similar to the power module, turn-off delay time is the only viable turn-off TSEP for the discrete device, while other turn-off characteristics are not temperature sensitive. These findings reinforce the importance of selecting the appropriate TSEPs for accurate

Table 4-5. Turn on parameters of discrete 10 kV 20 A SiC MOSFET.

Temperature (°C)	25	50	75	100	125
tdon (ns)	37.1	35.8	34.9	33.9	30.1
tcr (ns)	83.8	81.6	78.1	73.6	73
tvf(ns)	206.7	202.2	198.7	195.2	191
dv/dt (V/ns)	45.1	50.1	53.1	55.1	59.4

Table 4-6. Turn off parameters of 10 kV 20 A SiC MOSFET.

Temperature (°C)	25	50	75	100	125
tdoff (ns)	69.8	75.2	79.4	82.6	88
tvr (ns)	172.2	171.5	170.6	173.1	172.5
dv/dt (V/ns)	45.5	46	45.4	45.3	44.7

temperature monitoring and performance optimization in high voltage SiC MOSFET applications.

4.6 Temperature Sensor Based on TSEP

Dynamic TSEPs play a crucial role in assessing the performance of 10 kV SiC MOSFETs. Research has shown that these parameters can change by tens of nanoseconds across a 100°C temperature span, making real-time measurement challenging, especially given the fast-switching speeds inherent to WBG semiconductor applications.

Both voltage fall time and current rise time exhibit negative temperature coefficients. As temperature increases, the voltage fall time decreases, leading to a higher dv/dt , while the current rise time similarly shortens, resulting in an increased di/dt . This relationship is visually represented in **Figure 4.23**.

High-speed switching dynamics necessitate advanced sensing techniques capable of capturing nanosecond-scale variations, imposing significant demands on microcontroller resources. As an alternative, the voltage induced by TSEPs can be compared against a preset threshold calibrated at the maximum temperature, enabling effective over-temperature protection. This method aligns with the primary objective of most applications, which is to prevent over-temperature events rather than continuously monitoring the full temperature range.

Measuring the DC voltage of the half bridge power module as shown in **Figure 4.24**, turn on di/dt induces voltage drop on the power loop inductance L_{loop} , thus the dc voltage becomes $V_{DC} - L_{loop}di/dt$. This voltage drop is directly proportional to the rate of current change and the total loop inductance, which comprises the equivalent series inductance (ESL) of the DC-link capacitor, the busbar inductance, and any wire inductance in the power path.

The sensing circuit scales down this transient voltage using a resistive voltage divider, producing a signal denoted as V_{sense} . Since the turn-on di/dt typically increases with temperature due to faster switching transitions, the voltage drop observed at V_{sense} also becomes more pronounced at elevated temperatures. This temperature-sensitive behavior is exploited for over-temperature protection and is demonstrated experimentally.

V_{sense} signal is fed into a comparator with a predefined reference voltage. When the voltage drop exceeds a threshold—indicating an excessive di/dt and, a high device temperature—the comparator triggers a protection signal to the system controller.

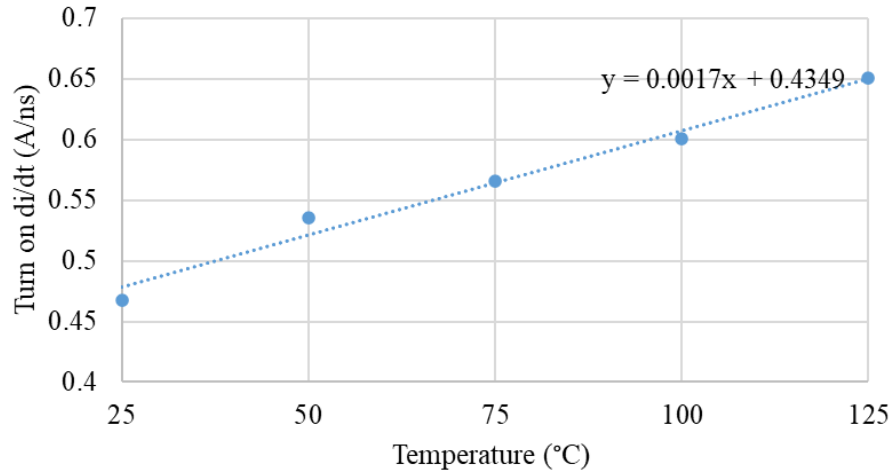


Figure 4.23. di/dt increase with temperature measured at 6.5 kV 57 A.

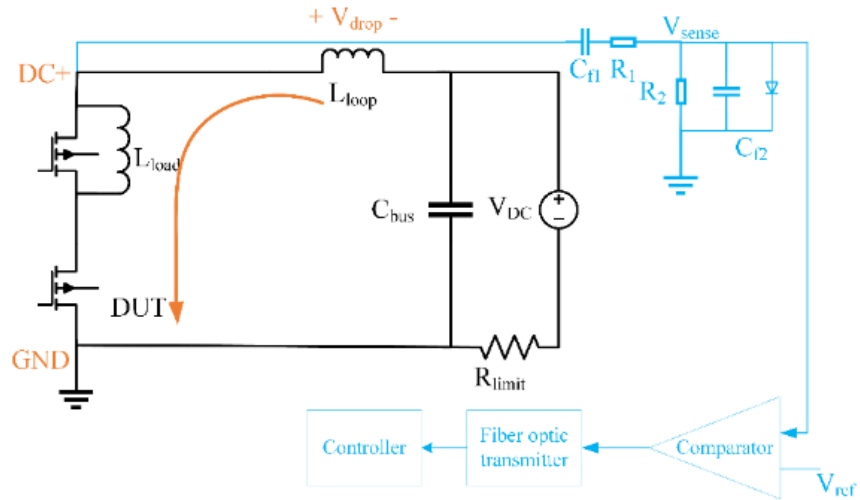


Figure 4.24. Over-temperature protection circuit based on sensing turn on di/dt.

The sensing circuit transfer function from $\frac{V_{sense}}{V_{DC}}$ can be written as (4.8) [1] :

$$H(s) = \frac{R_2 C_{f1} s}{R_1 R_2 C_{f1} C_{f2} s^2 + (R_1 C_{f1} + R_2 C_{f1} + R_2 C_{f2}) s + 1} \quad (4.8)$$

Due to operation at 3 kV, C_{f1} is a 10 kV capacitor capable of withstanding dc voltage. The parameters are listed in **Table 4-7**.

To establish a feasible threshold for accurate over-temperature protection, we calibrate the power module across different temperatures and measure voltage undershoot V_{drop} and sensor voltage V_{sense} at an operating condition of 3 kV and 30 A as shown in **Figure 4.25**. The test setup is shown in **Figure 4.26**, In this setup, a hotplate heats the power module to a specific temperature, while a fiber optic temperature sensor monitors the module to verify when the desired temperature is reached.

Figure 4.27 shows the DC voltage first undershoot increases with elevated temperatures. The detailed values of DC voltage undershoot and V_{sense} are presented in **Figure 4.28** and **Figure 4.29** respectively.

The protection threshold is set at -2.8 V for over-temperature protection at 100 °C. **Figure 4.30** shows the protection successfully triggered at 100 °C, as the DC voltage undershoot significantly increased at higher temperature and V_{sense} exceeded the threshold. The comparator output was pulled up and a signal was to the controller for over-temperature protection.

Table 4-7 di/dt voltage undershoot sensing circuit parameters.

Parameter	Value
R_1	24 kΩ
C_{f1}	10 pF
R_2	0.6 kΩ
C_{f2}	1 nF
L_{loop}	200 nH

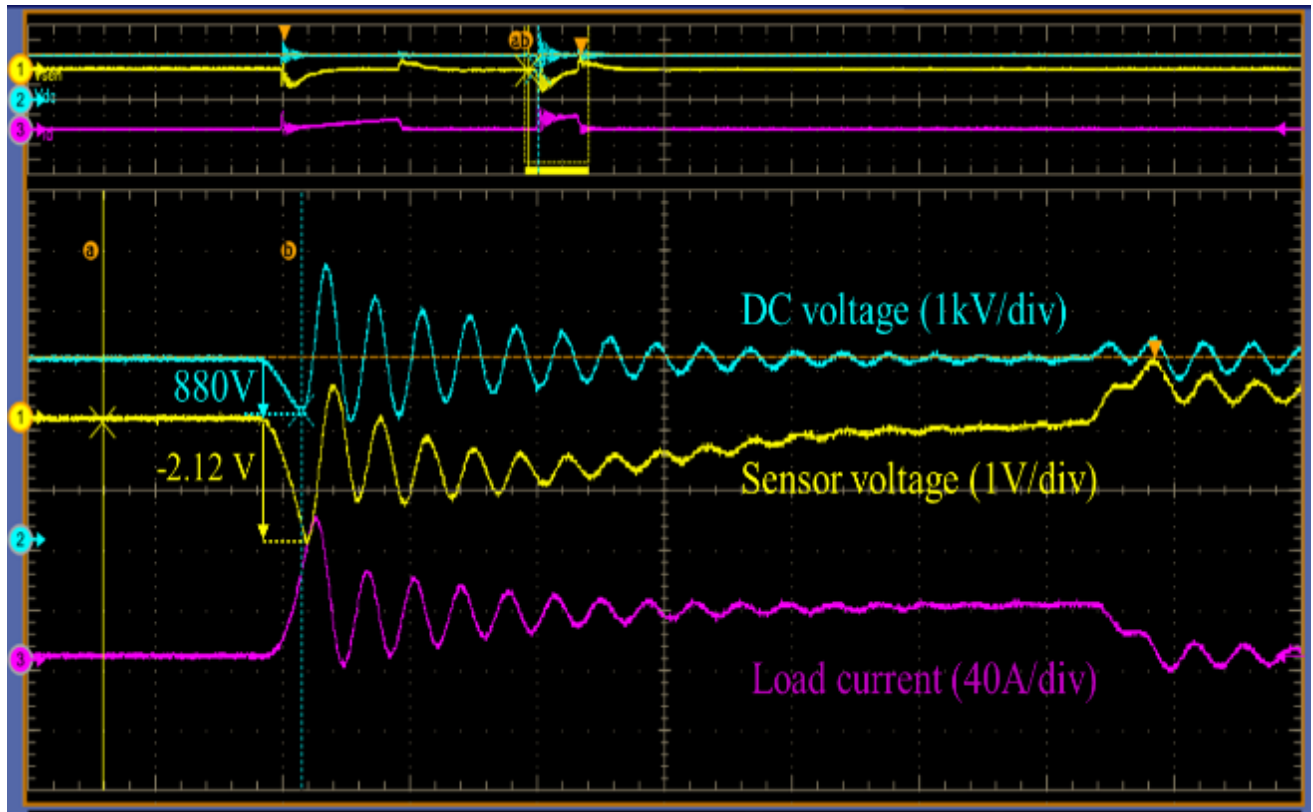


Figure 4.25. DC voltage undershoot and sensor voltage measurements during turn on at 25°C.

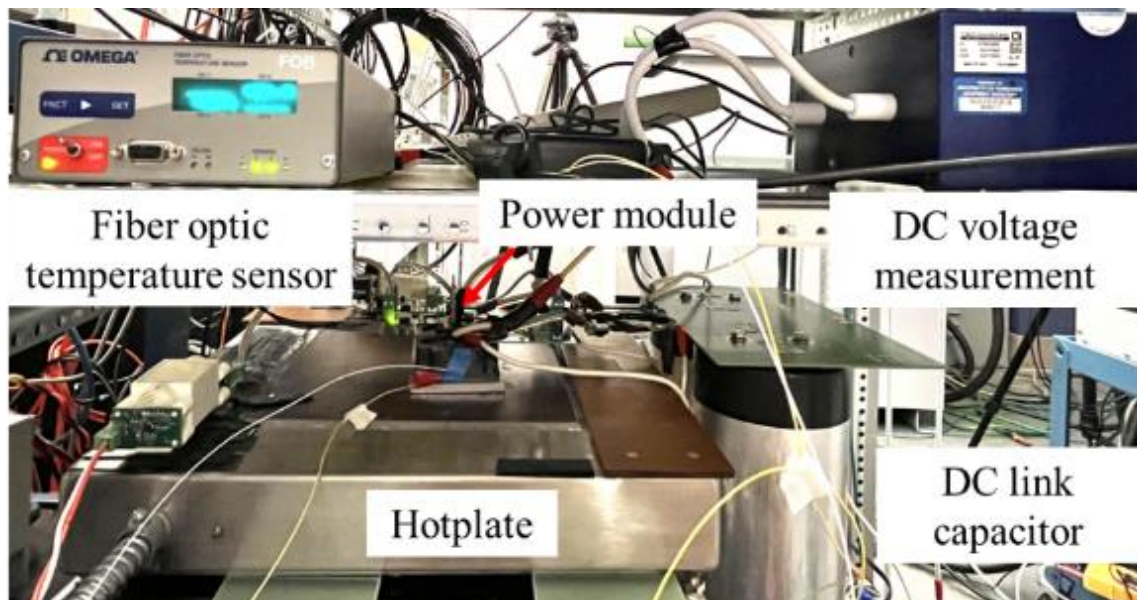


Figure 4.26. Experiment setup for TSEP calibration under different temperatures.

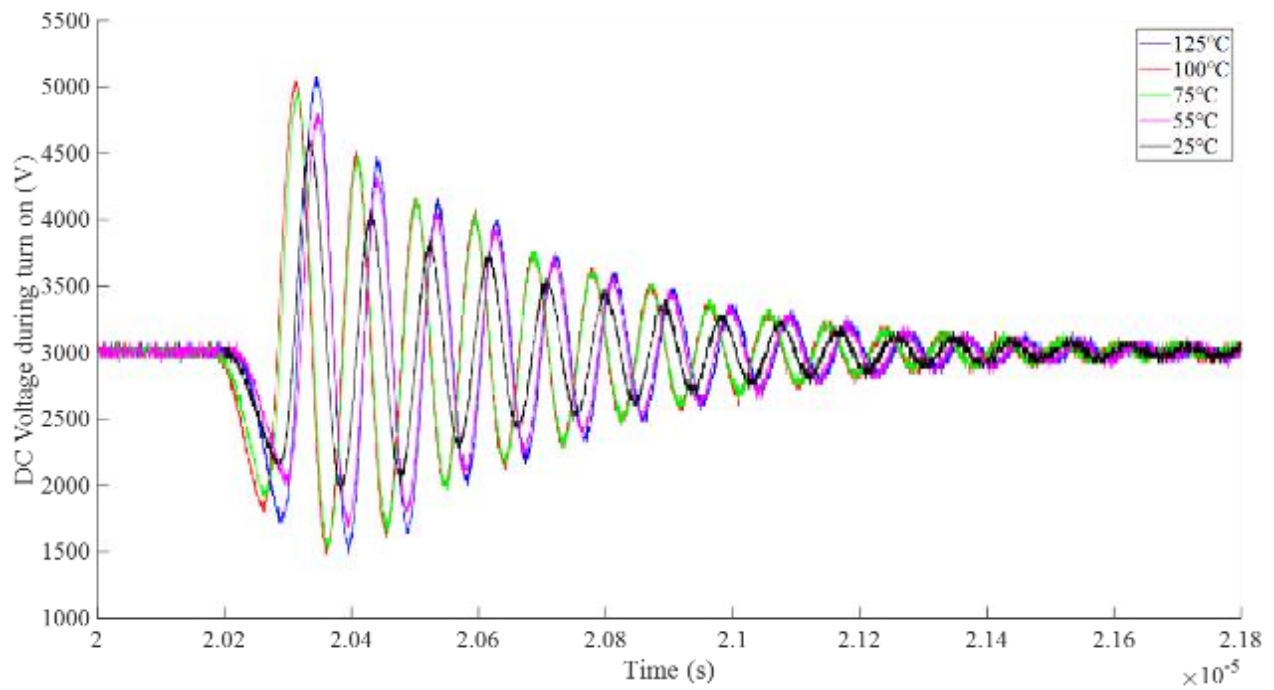


Figure 4.27. Voltage undershoot increases with higher temperature.

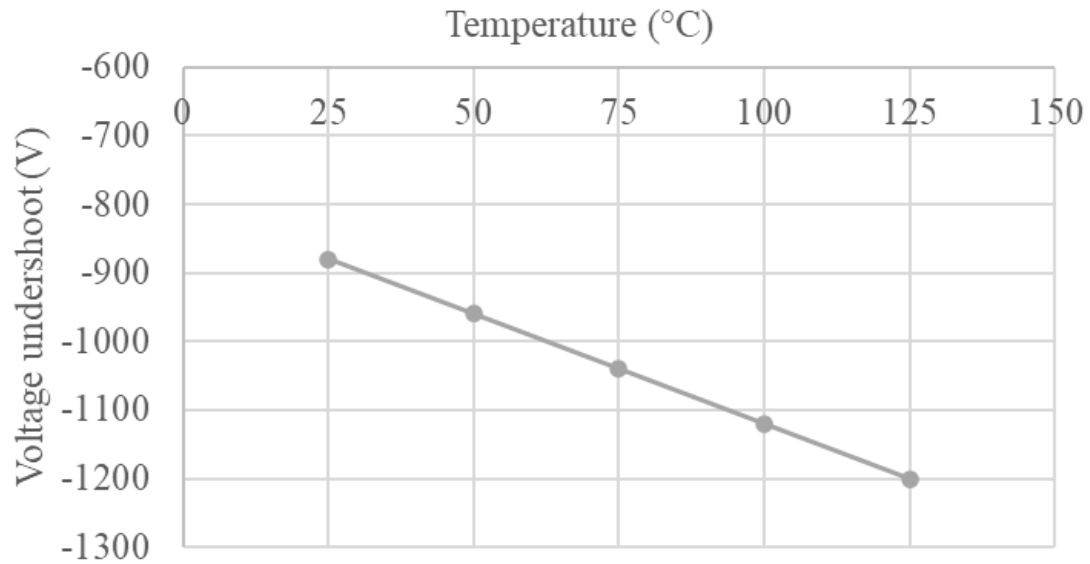


Figure 4.28. Voltage undershoot increases linearly with higher temperature.

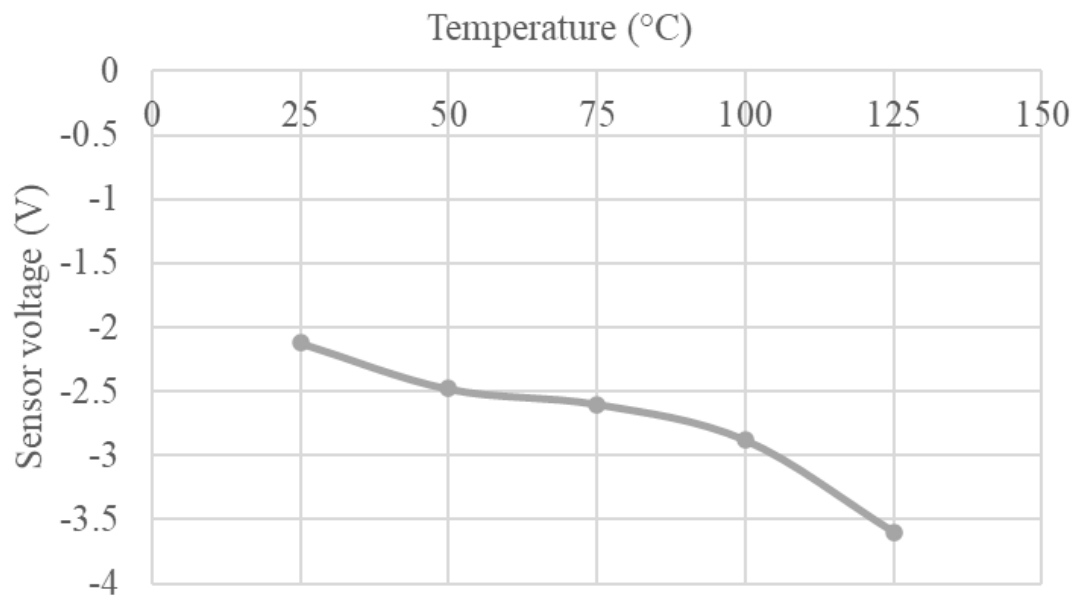


Figure 4.29. Sensor voltage increases with higher temperature.

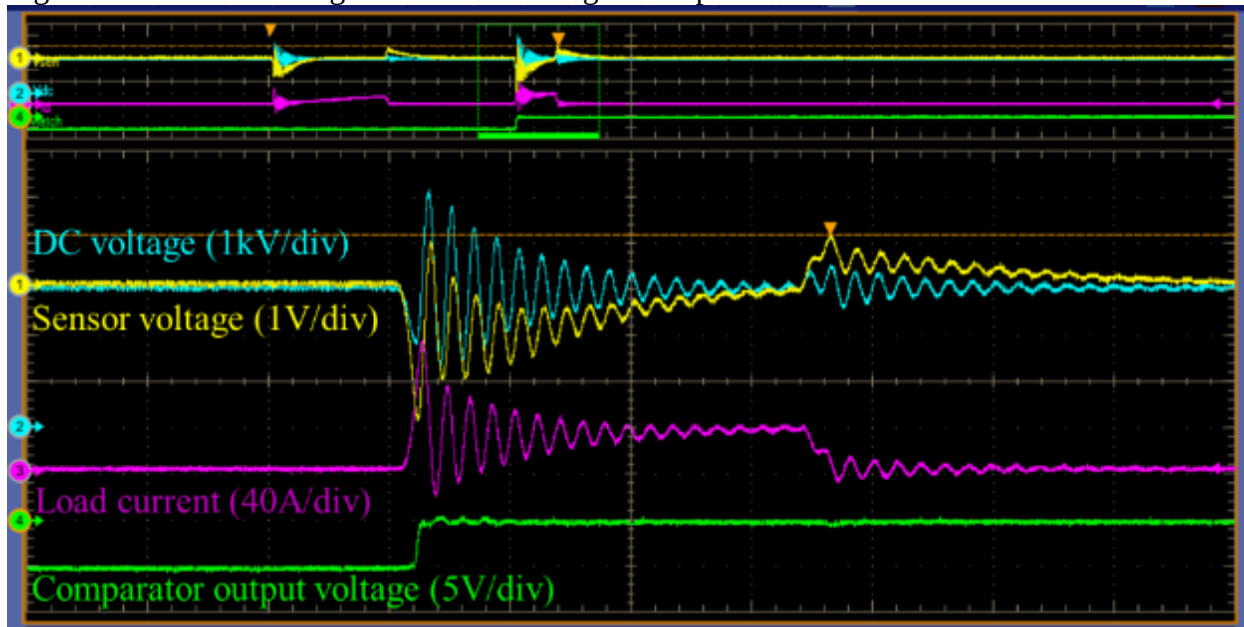


Figure 4.30. Over-temperature protection triggered at 100 °C. \

To establish a feasible threshold for accurate over-temperature protection, we calibrate the power module across different temperatures and measure voltage undershoot V_{drop} and sensor voltage V_{sense} at an operating condition of 3 kV and 30 A as shown in **Figure 4.25**. The test setup is shown in **Figure 4.26**. In this setup, a hotplate heats the power module to a specific temperature, while a fiber optic temperature sensor monitors the module to verify when the desired temperature is reached.

Figure 4.27 shows the DC voltage first undershoot increases with elevated temperatures. The detailed values of DC voltage undershoot and V_{sense} are presented in **Figure 4.28** and **Figure 4.29** respectively.

The protection threshold is set at -2.8 V for over-temperature protection at 100 °C. **Figure 4.30** shows the protection successfully triggered at 100 °C, as the DC voltage undershoot significantly increased at higher temperature and V_{sense} exceeded the threshold. The comparator output was pulled up and a signal was to the controller for over-temperature protection.

4.7 Summary

This chapter presents an in-depth analysis of TSEPs for Wolfspeed's XHV-9 10 kV SiC MOSFET power module. The key contributions are as follows:

- **TSEP Characterization:** Conducted a comprehensive extraction of critical TSEPs, on-state resistance and threshold voltage are temperature dependent. Also, turn-on delay time, current rise time, and voltage fall time during turn on transient are selected as TSEPs, all exhibiting negative temperature coefficients.
- **Cross Comparison of SiC Devices:** Demonstrated consistent temperature trends in turn-on TSEPs across both 10 kV and 3.3 kV SiC MOSFETs, with the 10 kV device showing more significant temperature induced variation. Turn-off parameters such as turn off delay time, voltage rise time and current fall time in 10 kV devices show negligible temperature sensitivity—contrary to the behavior observed in 3.3 kV and 1.2 kV counterparts.
- **Development of an over temperature protection sensor** which does not occupy resources from microcontroller.

Chapter 5 Cooling System Design

To dissipate heat effectively, a sufficient cooling system is required for a 1 MVA five-level MMC based on 10 kV, 100 A SiC power modules as shown in **Figure 5.1**. The MMC detailed parameters are listed in **Table 5-1**. However, achieving efficient heat dissipation necessitates a large cooling system, which in turn reduces the overall power density of the converter. Additionally, ensuring proper insulation between the high voltage switching devices and cooling components poses another challenge. This chapter addresses these issues by presenting a detailed design procedure for liquid cooling and selecting appropriate coolants with high dielectric strength. Air cooling with specific clearance and creepage distances is also presented. These two types of cooling methods are compared in terms of thermal performance, size, cost and installation effort. The effectiveness of the chosen design is validated through experimental measurements. Part of the content in this chapter is from the author's conference paper published in IEEE APEC 2024 [130].

5.1 Cooling Design Considering Insulation

In numerous low voltage applications, cooling designs often overlook insulation considerations. However, in MV systems, insulation is a crucial aspect of cooling design. In the case of this MMC converter, with a DC link voltage of 24 kV, the DC+ and DC- of the 24kV are +12kV and -12kV to the ground because the middle point is grounded. When the uppermost submodule is inserted, the drain of the lower device connects to the DC link at 12 kV to ground. Given that the device is rated at 10 kV, the DBC between the device and the cooling component may not offer adequate insulation.

In the scenario of liquid cooling, where cold plates are constructed from electrically conductive metal, the coolant circulating between these cold plates, the chiller, and the pump must be non-conductive. This measure eliminates the risk of electrical bridging between different components.

Regarding air cooling, the supplier recommends connecting the heatsink to the source of the device. This approach is intended to reduce the maximum electric field within the power module. However, because of this connection, the voltage of the heatsink relative to ground becomes a pulsating voltage, reaching a peak value of 12 kV, as illustrated in **Figure 5.2**.

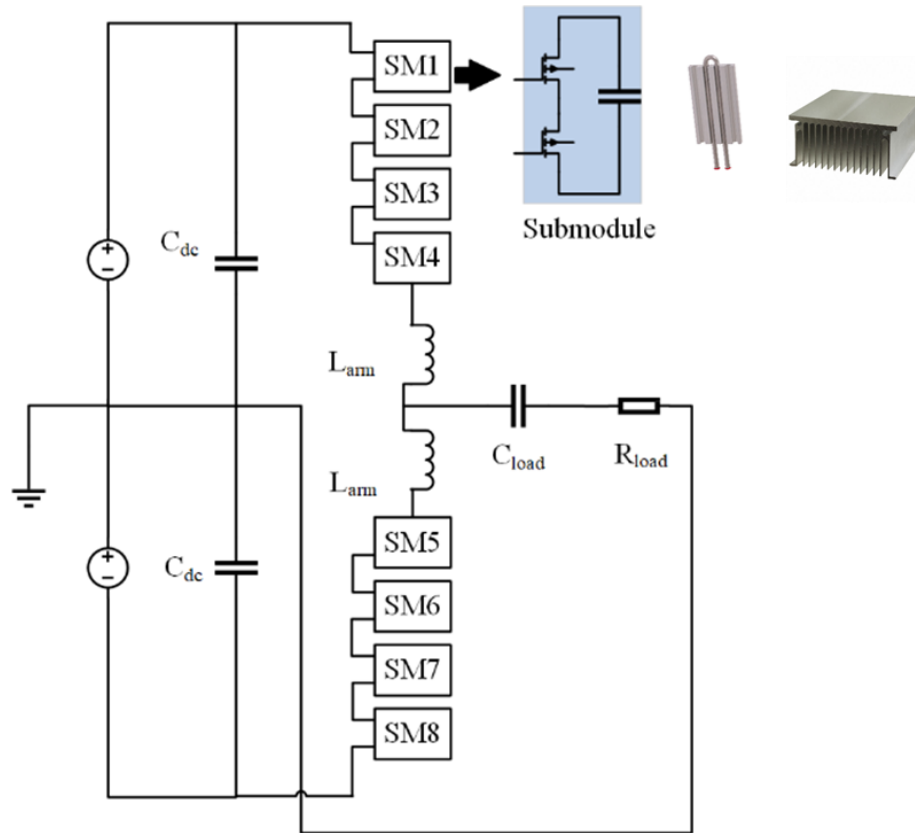


Figure 5.1. 5-level MMC phase leg.

Table 5-1. Specification of 5-level MMC.

Parameters	Values
DC link voltage	24 kV
AC output voltage	13.8 kV
Switching frequency	5 kHz
SM per arm	4
SM voltage	6 kV
SM capacitance	66 μ F
Arm inductance	5 mH

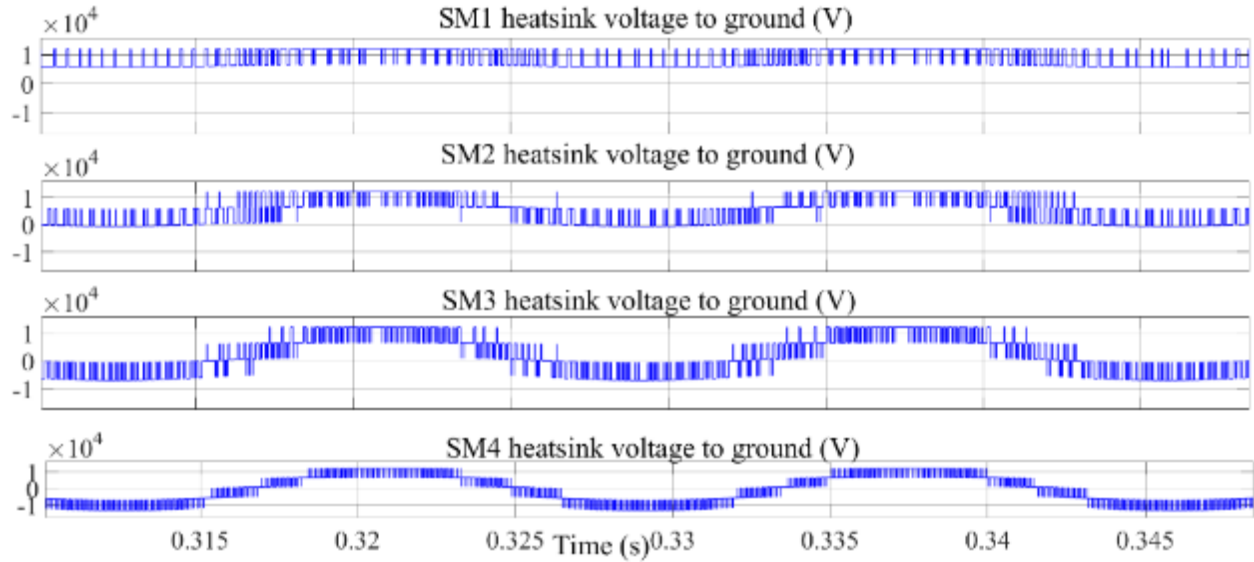


Figure 5.2. Heatsink voltage to ground of upper arm submodules.

This high pulsating voltage presents a significant hazard to nearby low-voltage components, such as the cooling fan, gate drivers, and APS. The risk arises from possible dielectric breakdown, unintended capacitive coupling, or EMI, which could lead to malfunction or voltage breakdown.

The voltage difference between adjacent heatsinks depicted in **Figure 5.3**, is a pulsating 6 kV. To prevent electrical breakdown and maintain insulation integrity, clearance and creepage distance requirements must be implemented between heatsinks. Clearance—the shortest air gap between conductive parts—must be sufficient to prevent arcing, while creepage distance—the surface path between conductors—must be designed to withstand prolonged high-voltage stress and potential surface contamination.

Within a single heatsink, where multiple fins are at the same voltage potential, the electric field between fins remains minimal. However, sharp edges of the heatsink act as points of high field concentration.

Figure 5.4. illustrates the simulated relationship between the maximum electric field ($E_{\max}$) and the excitation voltage for a single heatsink fin. The results indicate a linear increase in ($E_{\max}$) as the applied voltage rises, emphasizing that the maximum electric field occurs around the edges of the heatsink. This concentration presents a potential risk for air ionization, dielectric breakdown, and corona discharge.

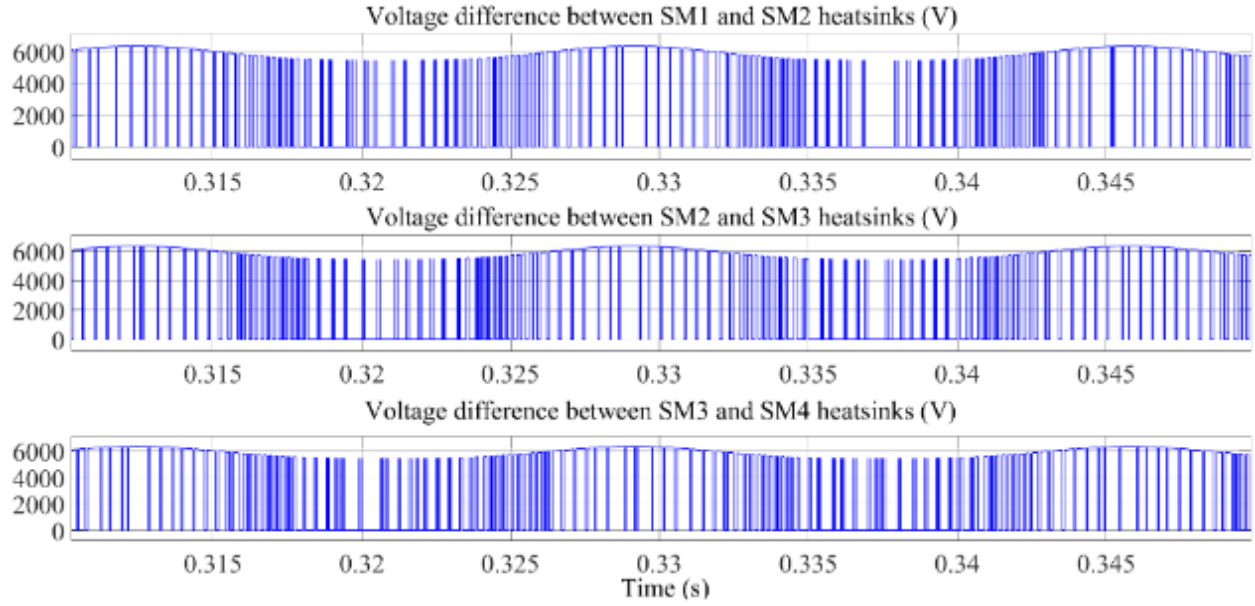
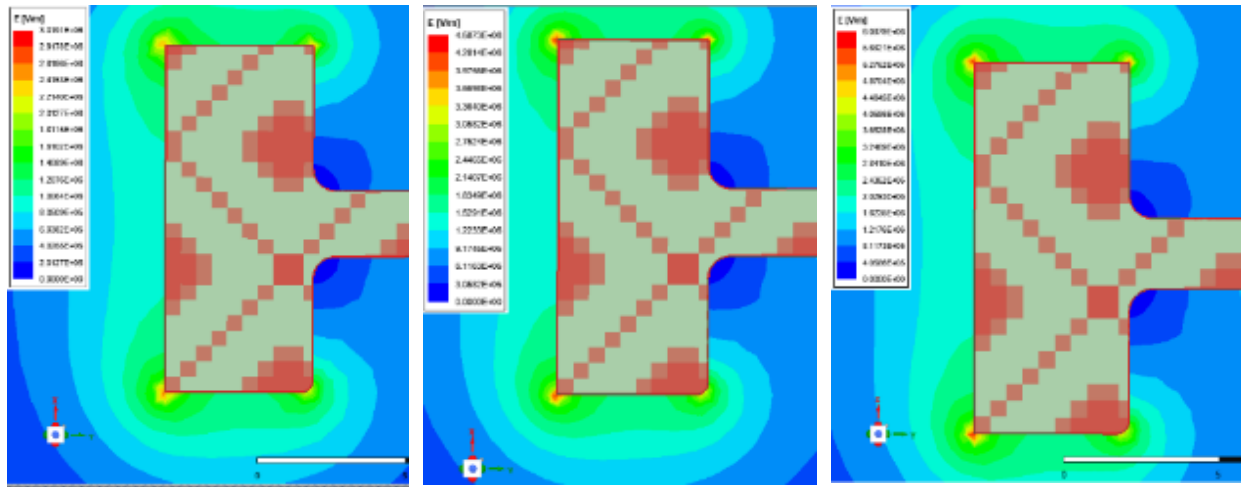


Figure 5.3. Voltage difference between adjacent heatsinks from SM1 to SM4 from top to bottom.



6 kV excitation:

$$E_{max} = 3kV/mm$$

9 kV excitation:

$$E_{max} = 4.5kV/mm$$

12 kV excitation:

$$E_{max} = 6kV/mm$$

Figure 5.4. Electric field distribution at different voltages.

To further validate the electric field distribution within the system, a 3D simulation was conducted using Ansys Electrostatic. The model, illustrated in **Figure 5.5**, includes key structural components such as heatsinks, air ducts, and fan adapters to closely replicate real-world conditions.

In the simulation setup, the top heatsink was applied a voltage of 12 kV, while the bottom heatsink was set to 6 kV, representing the maximum voltage on individual heatsink and the maximum voltage difference between adjacent heatsinks. To simulate the low-voltage fan, the top surface of the fan adapter was grounded at 0V.

From **Figure 5.6**, E_{max} is observed at the edges of the top heatsink, closer to the fan, with a value of $3 \times 10^5 \text{ V/m}$. This value is significantly lower than the air breakdown electric field threshold of $3 \times 10^6 \text{ V/m}$. Moreover, the maximum electric field between the top and bottom heatsink is approximately $8 \times 10^4 \text{ V/m}$, which also falls within the air breakdown limit. The clearance distance between the fan and the heatsink was established at 125 mm, in accordance with insulation coordination guidelines for systems operating at 12 kV. This design decision is based on standard atmospheric pressure, Pollution Degree 2 (typical for indoor environments), and material group III. The selected clearance aligns with recommendations from UL 840, ensuring adequate protection against electrical arcing under normal operating conditions. Overall, the simulation results indicate that the electric field distribution in the system remains below the air breakdown threshold.

5.2 Liquid Cooling Design

Liquid cooling systems for power electronics typically involve cold plates, a chiller, and connection tubes. The coolant determines the thermal performance and insulation strength of the whole system. The selection of a suitable coolant is first introduced.

5.2.1 Coolant Selection

Water is commonly chosen because of its high heat capacity and thermal conductivity. Facility water can be used directly in the chiller, but it may require filtration to remove minerals and chloride, which can negatively affect thermal performance and corrode metal tubing.

Deionized (DI) water is an alternative coolant option where ions are removed. It acts as an excellent insulator with high resistivity, preventing electrical arcing caused by static charge buildup. To safeguard the power module and gate driver from arcing damage, DI water is preferred over regular water. However, it is important to note that DI water is highly corrosive,

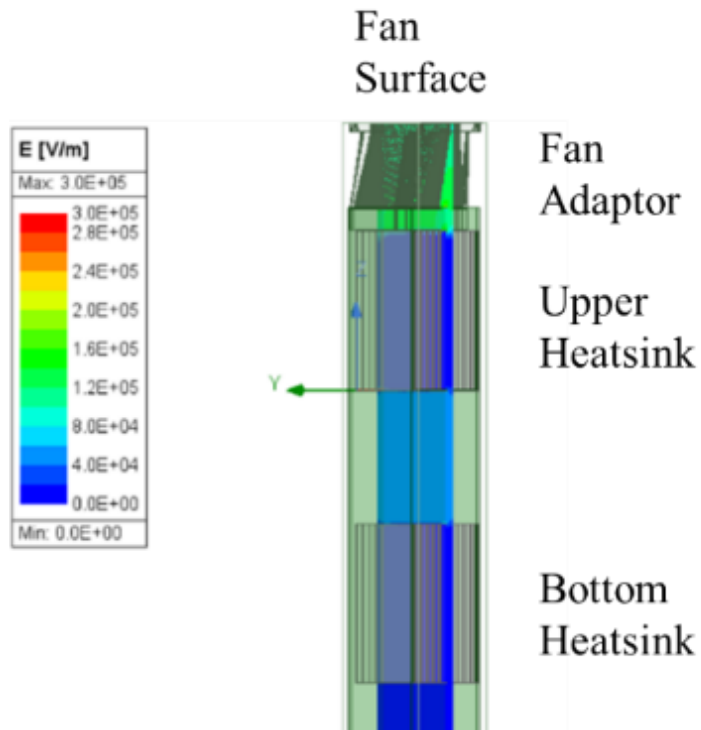


Figure 5.5. Electric field simulation of air-cooling system.

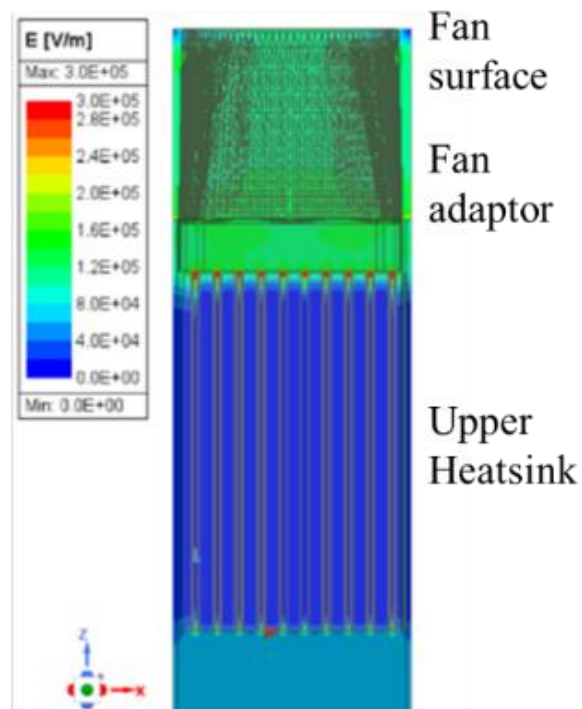


Figure 5.6. Magnified view of the electric field of the heatsink.

necessitating the use of corrosion-resistant materials such as stainless steel and plastics for the pump, cold plates, and plumbing. Also, DI water requires running a specialized deionization filter continuously to remove the ions from the water, which is expensive and time consuming.

Alternatively, dielectric fluids like 3M Fluorinert and 3M Novec 649 are non-conductive as shown in **Table 5-2**. However, they exhibit much lower thermal conductivity than DI water and are more expensive, making them less commonly used in liquid cooling systems. They are usually used to immerse electronic circuits for cooling.

5.2.2 Cold plate Selection

Each submodule, with a voltage difference of 6.5 kV, is mounted on an individual cold plate. The CP10 2-pass cold plate, similar in size to the XHV-9 power module, is selected. The nomenclature is given in **Table 5-3**. Calculating the outlet temperature (T_{out}) based on (5.1), with a flow rate of 0.5 GPM, an inlet temperature of 20°C, and a maximum heat dissipation of 300 W, the outlet temperature is 22.27 °C.

In the three-phase 5-level MMC, there are 24 power modules, each requiring a cold plate. To maintain a modular design, the cold plates are connected in series within a group, and these groups are then connected in parallel. As the coolant flows through the series-connected cold plates, the temperature of the coolant increases, causing the cold plate at the end of the series to reach the highest temperature. However, the cold plates in parallel will maintain similar temperatures due to the uniform flow rate across them. The coolant inlet temperature is 20°C. Given that the specific heat of water is very similar at 20°C, 25°C, and 30°C (4.1844 kJ/(kg·K), 4.1816 kJ/(kg·K), and 4.1801 kJ/(kg·K), respectively), 4.1816 kJ/(kg·K) is used for calculations.

In **Table 5-4**, junction temperature and main pipe flow rate of different arrangements of cold plates (different series and parallel combinations) are presented. The largest difference of maximum junction temperature between different configurations is around 8 °C, which is due to the fact that coolant temperature increases by 1.13°C after running through one cold plate at 1 gallon per minute (GPM). Due to the constraint of maximum flow rate provided by pump and flow rate loss caused by manifolds, we can only parallel a small number of cold plates.

Here lists an example of four cold plates in one arm connected in series. The general design steps follow the flow chart in **Figure 5.7**. As the coolant passes through each cold plate, the outlet coolant temperature increases. The fourth cold plate in the series has the highest coolant

Table 5-2. Common Coolant Comparison.

Coolant	Water	DI water	3M Fluorinert	3M Novec 649
Specific heat (J/kg· K)	4184	4184	1100	1103
Thermal conductivity (W/mK)	0.598	0.598	0.060	0.059
Dielectric strength (kV/mm)	NA	>20	>15.7	>15.7

Table 5-3. Nomenclature.

Temperature of fluid leaving cold plate	T_{out}
Inlet temperature of fluid	T_{in}
Heat load of device	Q
Density of the fluid	ρ
Cooling fluid air velocity	v
Specific heat of the fluid	C_p
Normalized thermal resistance	θ
Maximum cold plate surface temperature	T_{surf}

Table 5-4. Cooling performance between different cold plates configurations.

Number of cold plates in series (group)	Number of groups in parallel	Maximum Outlet temperature (°C)	Maximum SiC device junction temperature (°C)	Main pipe flow rate (GPM)	Total cold plates pressure drop (psi)
1	24	21.14	63.23	24	0.6
2	12	22.27	64.37	12	1.2
4	6	24.54	66.64	6	2.4
8	3	29.09	71.19	3	4.8

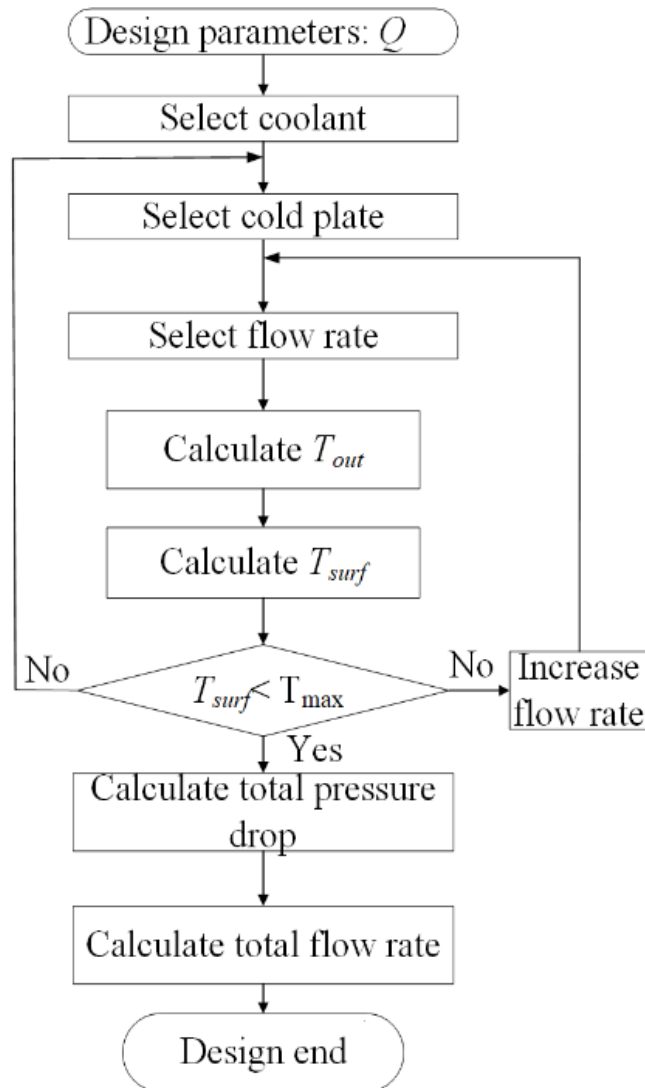


Figure 5.7. Design flowchart of liquid cooling.

temperature, then the surface temperature can be calculated using (5.2).

Silicone-based thermal interface material (TIM) with a thermal conductivity of 7 W/m·K was utilized to enhance heat transfer between the power module and the heatsink. The TIM layer was applied at a uniform thickness of 0.1 mm over a contact area of 150 mm × 75 mm. Under a steady-state power dissipation of 300 W, the resulting thermal resistance was calculated to be approximately 0.0013 K/W, yielding a temperature differential of only 0.39 °C across the interface.

Consequently, the temperature deviation across the interface remains negligible. Thus, assuming the cold plate surface temperature equals the power module case temperature, and the junction-to-case thermal resistance R_{θ} is 0.0689 °C/W, the maximum junction temperature calculated from (5.3) is 66.76 °C, less than the maximum allowable temperature limit (100 °C). The maximum allowable temperature is limited to 100 °C in order to mitigate thermally accelerated degradation mechanisms and ensure long-term device reliability.

If the junction temperature exceeds the maximum temperature limit, the flow rate can be increased, which will eventually require a larger pump. Another option is selecting a larger cold plate or a 4-pass cold plate to accommodate the heat load.

$$T_{out} = T_{in} + \frac{Q}{\rho v C_p} \quad (5.1)$$

$$\theta = \frac{(T_{surf} - T_{out})A}{Q} \quad (5.2)$$

$$R_{\theta} = \frac{T_j - T_{case}}{Q} \quad (5.3)$$

5.2.3 Chiller Selection

Next, we estimate the total pressure drop in the cooling system (P_{total}), which includes the pressure drop of the cold plates ($P_{coldplate}$), the pressure drop inside the chiller ($P_{chiller}$), and the pressure drop of the tubing (P_{tubing}).

$$P_{total} = P_{coldplate} + P_{chiller} + P_{tubing} \quad (5.4)$$

Pressure drop increases exponentially with flow rate. At a flow rate of 0.5 GPM, a single CP10G03 2-pass cold plate has a pressure drop of 0.3 psi. Therefore, 24 cold plates have a pressure drop of $P_{coldplate} = 24 \times 0.3 = 7.2$ psi. The pressure drop inside the chiller is approximately 10 psi.

Pipe friction losses depend on pipe diameter, flow rate, and length. Using the Hazen-Williams equation for water:

$$P_{tubing} = \frac{4.52V^{1.85}L}{(C^{1.85}D^{4.87})} \quad (5.5)$$

where V is flow rate (GPM), C is pipe roughness coefficient (~ 140 for PVC, ~ 100 for steel), D is pipe inner diameter and L is pipe length. Assuming $D = 0.5$ -inch, pipe length is 2 m per set, $Q = 0.5$ GPM per cold plate set, friction loss per PVC pipe is about 0.35 psi. Thus, the total pressure drop calculated from (5.4) is 18.7 psi.

A suitable pump can be selected to accommodate this flow rate and pressure. Referring to **Table 5-5**, it is evident that faster flow rate leads to improved thermal performance. However, this improvement necessitates a larger pump with higher head pressure to handle the increased pressure drop in the system. To cool 24 power modules, each dissipating 300 W of heat, the total heat load is 7.2 kW. Therefore, a 10 kW chiller is chosen for the cooling capacity.

5.3 Air Cooling Design

5.3.1 Heatsink Selection

The power module loss is determined by the switching speed, switching frequency, and modulation strategy in MMC. The loss is measured based on DPT of a single half bridge submodule at 6.5 kV and 55 A. The maximum loss is estimated to be 300 W. The junction to case thermal resistance of the 10 kV, 100 A power module from Wolfspeed is $0.0689^{\circ}\text{C}/\text{W}$. To maintain a junction temperature below 100°C , providing margin below the 125°C maximum operating limit, the case temperature is assumed to be approximately 80°C . The heatsink and baseplate surfaces are considered thermally equivalent to the case temperature.

Table 5-5 Pump pressure at varying flow rate.

Cold plate flow rate (GPM)	Pump flow rate (GPM)	Maximum junction temperature ($^{\circ}\text{C}$)	Single cold plate pressure drop (PSI)	Pump pressure drop (PSI)
0.5	3	76.7	0.3	17.55
1	6	65.9	0.55	24.05
1.5	9	61.7	0.8	30.05
2	12	59.4	1.4	44.45

Given a 55 °C ambient temperature stated in the project requirement, the maximum allowable thermal resistance of the heatsink is calculated to be 0.081 °C/W. A Wakefield 510-6M extruded aluminum heatsink (187 mm × 152 mm × 79.7 mm) is selected, which provides a thermal resistance of 0.07 °C/W at an airflow velocity of 4 m/s. Therefore, a minimum airflow of 4 m/s is required to ensure adequate thermal management under worst-case power dissipation conditions.

$$R_{th}(heatsink) = \frac{T_{surface} - T_{ambient}}{P_{loss}} \quad (5.5)$$

5.3.2 Power Module Model Building

To analyze thermal distribution within the power module, six dies operating in parallel for a single switch are modeled to account for variations in heat dissipation due to placement and electrical characteristics as shown in **Figure 5.8**. In the simulation, a constant power dissipation is applied to each die, and the thermal resistance of each layer is calculated based on the temperature difference at thermal equilibrium.

The thermal resistance of individual layers, including the silicon dies, solder layers, direct bonded copper (DBC), ceramic substrate, and baseplate, is systematically evaluated. The total simulated thermal resistance is then compared to the junction-to-case thermal resistance of 0.0689°C/W provided in the datasheet. The close agreement between these values confirms the validity of the steady-state thermal model.

The detailed material and its thermal characteristics are listed in **Table 5-6**. The primary heat dissipation path is directed downward, where heat generated by the dies is transferred through the DBC substrate and baseplate before reaching the heatsink.

In contrast, the upward heat flow through the silicone gel and outer case is minimal and, therefore, considered negligible in this analysis. Consequently, the silicone gel and outer case are excluded from the thermal model to focus on the dominant heat dissipation pathway.

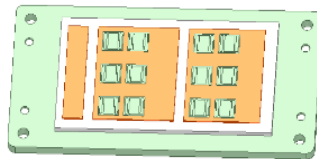


Figure 5.8. Power module model in Icepak.

Table 5-6. Power module thermal characteristics.

Component	Material	Specific heat	Thermal Expansion Coefficient
Die	SiC-kt grade	555 J/kg°C	4.0e ⁻⁶ /°C
DBC copper	Copper	385 J/kg°C	1.77e ⁻⁵ /°C
Substrate	Al ₂ O ₃	770 J/kg°C	5.2e ⁻⁶ /°C

In the simulation, a total power loss of 300 W, which comes from the loss calculation, is assigned for the power module, with each die dissipating 25 W of power. Under operating conditions with a 25°C ambient temperature and an air velocity of 10 m/s, the maximum junction temperature reaches 70°C, while the heatsink temperature is approximately 50°C, as shown in **Figure 5.9**. This temperature distribution indicates effective heat dissipation through the DBC substrate and baseplate to the heatsink, ensuring that the module operates within safe thermal limits.

5.3.3 Airduct Design

There are four submodules in one arm of the MMC, and eight submodules in one phase leg. It is preferred to have an air duct that provides airflow to four submodules simultaneously. Here, two types of air ducts are presented. Numerical estimation is done first to evaluate the viability of the design, which follows the steps shown in **Figure 5.10**. Then CFD simulation is carried out to verify the air velocity and power module temperature increase.

5.3.3.1 Multiple T-shape Airduct

A multiple T shape air duct, commonly used in ventilation systems is examined here as shown in **Figure 5.11**. The duct system begins with a fan located at Section 1, where air is drawn into the system. From there, the airflow proceeds through a T-shaped fitting, which distributes the flow into two branches. One of these branches incorporates a 90° bend that further directs the airflow toward four separate outlet sections. This configuration is analyzed to evaluate the airflow

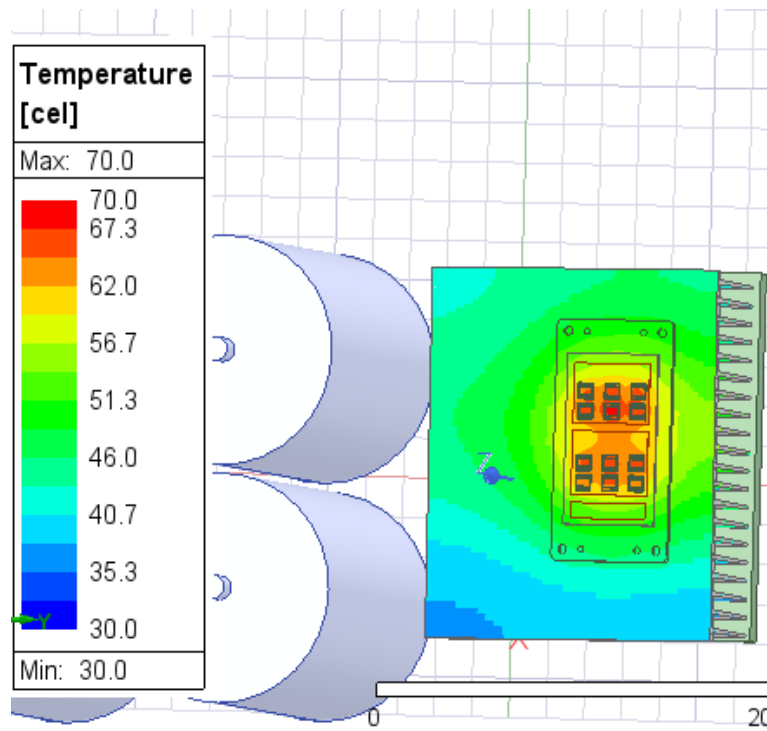


Figure 5.9. Thermal simulation of SiC power module mounted on air-cooled heatsink in Ansys Icepak.

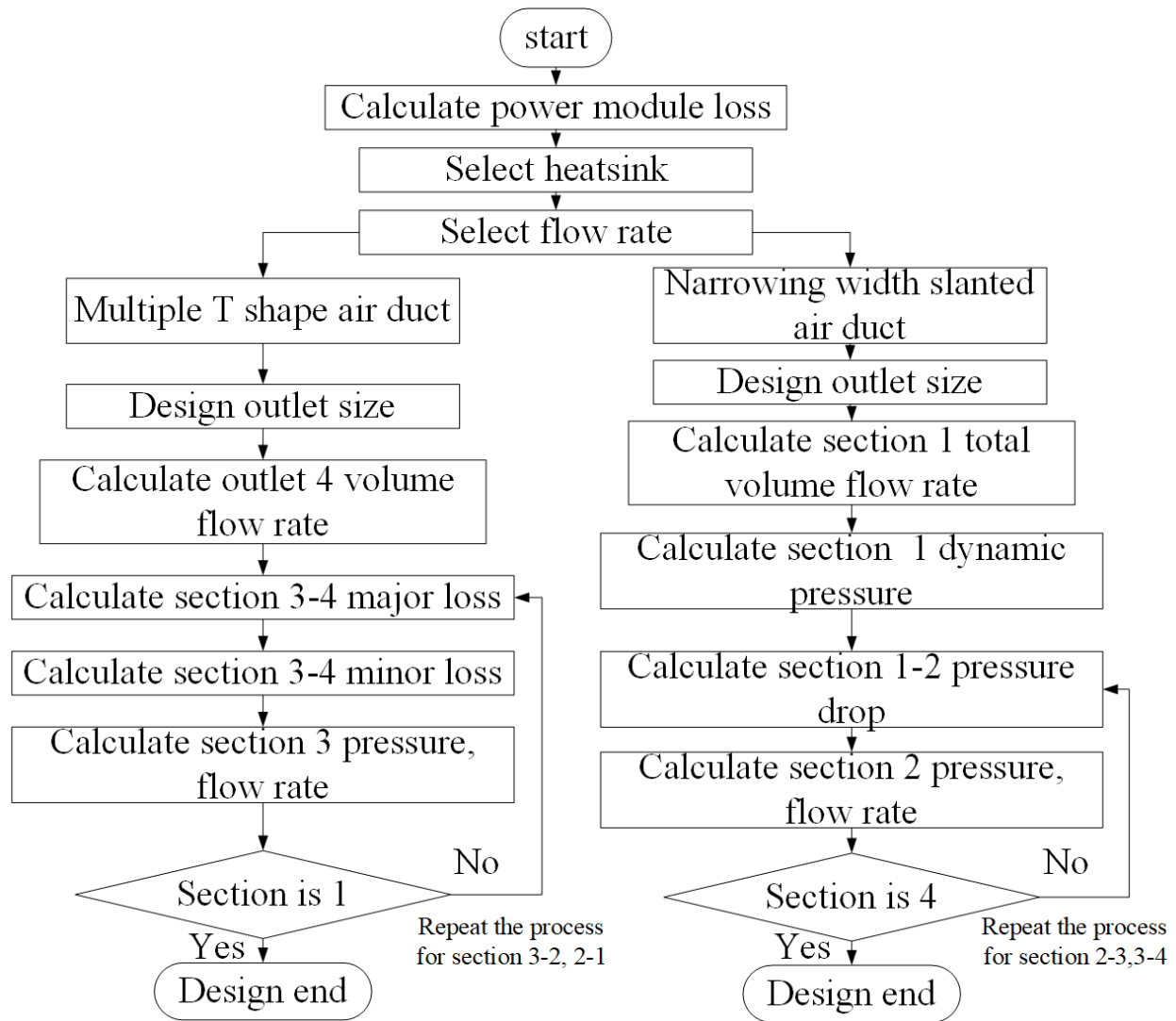


Figure 5.10. Airduct design procedure.

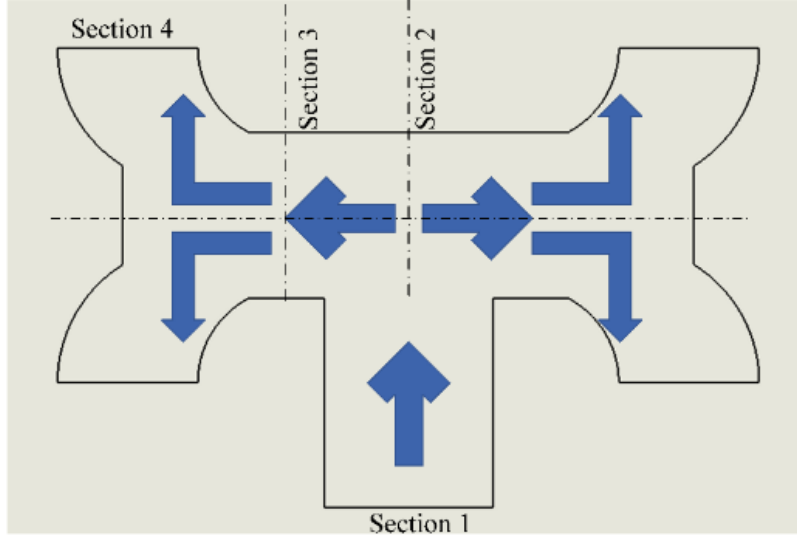


Figure 5.11. Multiple T-shape air duct top view.

distribution and pressure drop.

The energy required to push air through the pipe is dissipated in friction pressure loss, which can be further categorized into major loss and minor loss. Major loss is caused by friction within a pipe as shown in (5.6), where f is the friction factor, L and D are the pipe length and diameter, ρ represents the air density, and V is air velocity.

$$\Delta P_{major} = \sum f \times \frac{L}{D} \times \frac{1}{2} \rho V^2 \quad (5.6)$$

Minor loss occurs at the change of section, valve, bend or other interruption. In this case, the major loss is negligible as the air duct is short, while minor loss is dominant due to the T type fitting and 90° bends. Minor loss can be calculated in (5.7), where k is the minor loss coefficient. The detailed calculation is shown in **Table 5-7**.

$$\Delta P_{minor} = \sum k \times \frac{1}{2} \rho V^2 \quad (5.7)$$

5.3.3.2 Narrowing Width Slanted Airduct

Air velocity is significantly diminished as it passes through 90° bends; thus, a straight airduct with narrowing width is designed to have minimum air flow reduction. The airduct has four same size outlets facing the four heatsinks in a row as shown in **Figure 5.12**.

Each outlet has a size like a heatsink; with an air velocity V of 4 m/s, the volume air velocity can be calculated for each outlet. The total volume air velocity in the main airduct is the sum of

Table 5-7. Air velocity of T-shape airduct.

Section	Volume air velocity (m ³ /s)	Width×Height (m×m)	Actual air velocity (m/s)	Minor loss (Pa)	Minor loss coefficient
1-2	0.188	0.12×0.1	15.7	147.3	1
2-3	0.094	0.12×0.1	7.8	36.8	1
3-4	0.047	0.10×0.1	4.7	19.9	1.5

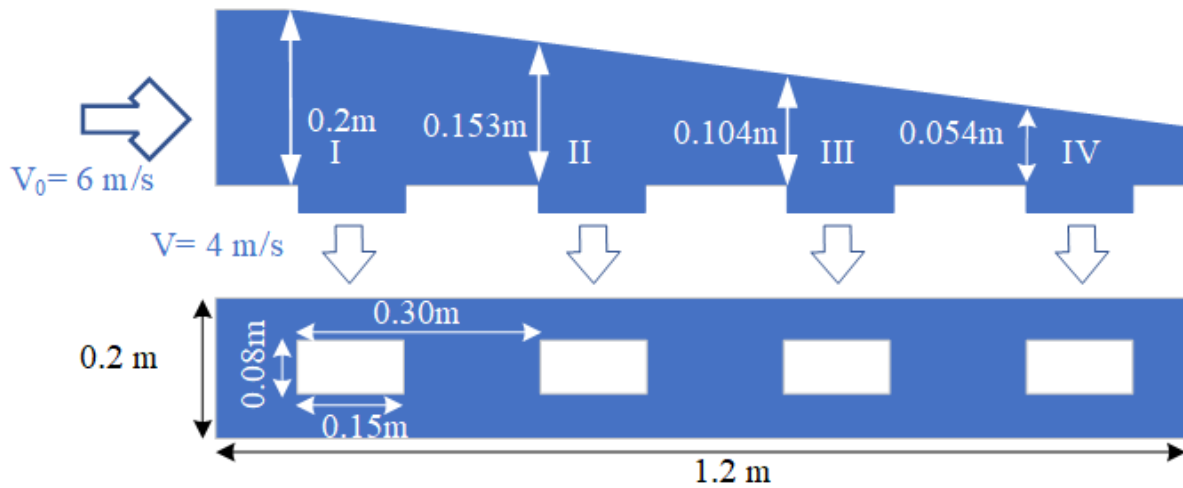


Figure 5.12. Narrowing width slanted airduct top view and front view.

four outlet volume air velocities in (5.8), where the 3600 factor converts m³/s to m³/hr.

$$L_1 = 4L = 4w \cdot h \cdot V \cdot 3600 \quad (5.8)$$

From the law of conservation of energy, for a steady, non-compressible flow for a fixed control volume, the change in total pressure between any two points in a system is equal to the sum of the change in static pressure between the points and the change in velocity pressure between the points. To maintain equal volume air velocity at all outlets, the pressure in the whole airduct should be the same, and the main duct air velocity V_0 is larger than outlet air velocity V .

Then the dynamic pressure loss from the beginning to the end of the duct is equal to the total pressure loss of the whole air duct as shown in (5.9), where Δp_m is average pressure loss per meter, l is the distance traveled by air and ΔP_i is the change of static pressure.

$$\frac{\rho}{2}(V_0^2 - V^2) = \sum (\Delta p_m l + \Delta P_i) \quad (5.9)$$

The aerodynamic design incorporates a gradually shrinking cross-sectional area along the main duct to compensate for the static pressure increase resulting from converted dynamic pressure as airflow progresses downstream. This area reduction follows conservation principles where decreasing velocity pressure is balanced by rising static pressure. The system assumes uniform flow factors (air resistance coefficients) across all outlets, accounting for consistent outlet geometry, discharge angles, and velocity ratios between outlets and the main duct.

Computational analysis initiates at the primary intake cross-section (L_1 representing total volumetric flow rate) and propagates sequentially through subsequent segments. This methodology ensures proper pressure balancing while maintaining design uniformity, with each outlet's flow characteristics being determined by its local static pressure and the predetermined resistance factor.

$$L_1 = A_1 \cdot V_1 \cdot 3600 \quad (5.10)$$

Dynamic pressure at cross section 1 is

$$P_{d1} = \frac{V_1^2 \rho}{2} \quad (5.11)$$

Then we calculate the pressure loss between section 1 and section 2. Hydraulic diameter of the duct is calculated in (5.12), which converts the rectangular duct dimension to a circular duct diameter, simplifying later stage friction loss calculations.

$$D_1 = \frac{2W_1H}{W_1 + H} \quad (5.12)$$

Unit average pressure loss caused by friction along the duct is

$$p_{m1} = 1.05 \times 10^{-2} D_1^{-1.21} V_1^{1.925} \quad (5.13)$$

Total pressure drops from section 1 to section 2 is

$$P_{m1} = p_{m1} l \quad (5.14)$$

Dynamic pressure at section 2 equals

$$P_{d2} = P_{d1} - P_{m1} \quad (5.15)$$

Air velocity at section 2 can be calculated from the dynamic pressure in (5.16)

$$V_2 = 1.29 \sqrt{P_{d2}} \quad (5.16)$$

L_2 is calculated by subtracting L_0 from L_1 . A_2 can be derived from the same equation as in (5.10). The same process repeats itself from section 2 to section 3 and from section 3 to section 4.

The calculation results are shown in **Table 5-8**.

To select a fan, the total pressure P for this duct is calculated in (5.17)

$$P = P_{d1} + P_j \quad (5.17)$$

The dynamic pressure is calculated in (5.18), and static pressure is explained as follows. As each outlet connection to the airduct is equivalent to a three-way bypass pipe, static pressure works to overcome its friction. The local drag coefficient is

$$\zeta_{tr} = 0.3 + \left(\frac{V}{V_0} \right)^2 \quad (5.18)$$

We can find the average local drag coefficient $\overline{\zeta_{tr}}$ between the first and the fourth outlet connection. The local drag coefficient ζ_k at the outlet is ~ 3.5 . Static pressure can be calculated in (5.19)

$$P_j = (\overline{\zeta_{tr}} + \zeta_k) \frac{V_0^2 \rho}{2} \quad (5.19)$$

The total pressure required is 67.7 Pa, which equals 0.28-inch water. At the same time, the volume air velocity is 864 m³/h or 509 CFM. From the fan curve, if the pressure at 509 CFM exceeds 0.28-inch water, then this fan would work. Also, it is better that the fan is the same size as the air duct, so no additional adaptor is needed. Due to the large pressure and flow velocity, a 205 × 205 × 72 mm 110 Vac fan OA205AN is selected.

Table 5-8. Calculation results of slanted airduct.

Cross section No	Volume air velocity $L(\text{m}^3/\text{h})$	Dynamic pressure $P_d(\text{Pa})$	Static pressure $P_i(\text{Pa})$	Air flow velocity $V(\text{m/s})$	Cross section area $A(\text{m}^2)$
1	866.3	21.6	46.1	6.0	0.040
2	649.7	20.9	46.1	5.9	0.031
3	433.2	20.0	46.1	5.8	0.021
4	216.6	19.0	46.1	5.6	0.011
Cross section No	Width Height (m×m)	Hydraulic diameter $D_m(\text{m})$	Air duct	Average pressure Loss p_m (Pa/m)	Pressure loss $P_m(\text{Pa})$
1	0.2×0.2	0.195	1-2	2.384	0.715
2	0.191×0.2	0.174	2-3	2.646	0.794
3	0.130×0.2	0.144	3-4	3.218	0.965
4	0.067×0.2	0.094	4-5	5.100	1.530

5.3.3.2.1 CFD Simulation in Icepak

The airduct is drawn in Solidworks and then imported into Icepak. An opening is assigned at the beginning of the airduct with a velocity of 6 m/s as shown in **Figure 5.13**. It is observed that the air velocity at all four outlets remains relatively uniform, averaging around 6 m/s. To further verify this, the velocity vector is decomposed to determine the velocity perpendicular to the outlet. The result shows an air velocity of approximately 4 m/s, which aligns closely with previous calculations. Additionally, the outflow direction at all four outlets is largely parallel, confirming the design's effectiveness.

The outflow angle is consistent across all outlets, indicating an equal flow rate. This consistency is supported by the fact that the outflow angle tangent value, determined by the ratio of velocity in the main duct to outlet velocity, remains stable. The main duct air velocity only slightly decreases from 6 m/s to 5.58 m/s. This observation confirms that the airflow is evenly distributed across all outlets, validating the accuracy and reliability of the air duct design.

Next, the power module, heatsinks and submodule capacitors are incorporated into the simulation with the air duct to model the real setup in **Figure 5.14**. Only one power module is simulated in this setup instead of four power modules to save computational resources and time. Still four heatsinks and their submodule capacitors are placed along the airduct outlets so the air flow across the heatsinks is the same as the actual setup. As the fourth outlet is most likely to exhibit the lowest air velocity due to the lowest dynamic pressure, the power module simulated is placed at the heatsink furthest away from the fan, presenting the worst case.

From the Simulink simulation using nearest level modulation, the lower switch in one submodule incurs a power loss of 225 W, while the upper switch incurs 75 W. Given that each switch consists of six parallel dies, the power loss is distributed evenly, assigning 37.5 W to each die in the lower switch and 12.5 W to each die in the upper switch.

As shown in **Figure 5.14**, upper switch dies' temperature is $\sim 73^\circ\text{C}$ and the lower switch die temperature is $\sim 50^\circ\text{C}$; these temperatures are all well within the safe operation range of 100°C . The maximum die temperature is larger than the calculated value based on thermal resistance due to the thermal cross coupling effects of multiple dies in the package.

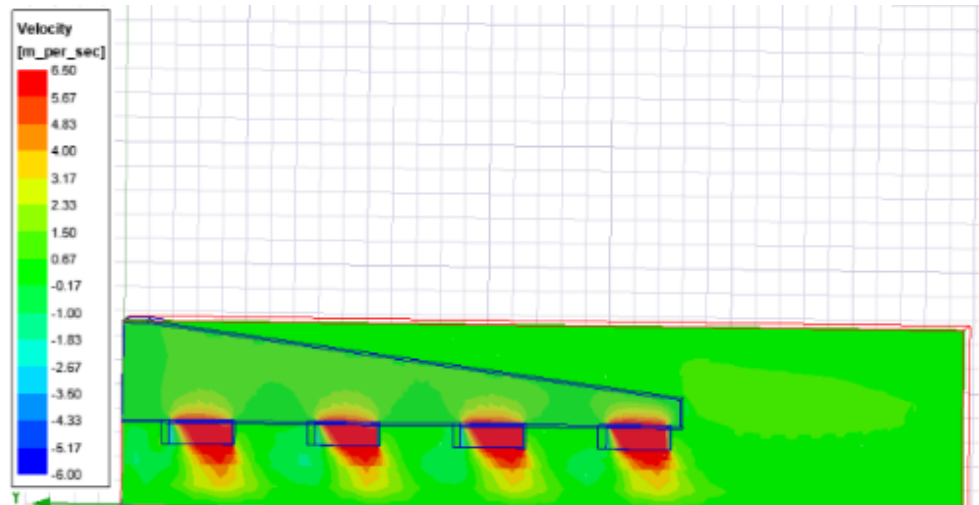


Figure 5.13. Air flow distribution of slanted air duct.

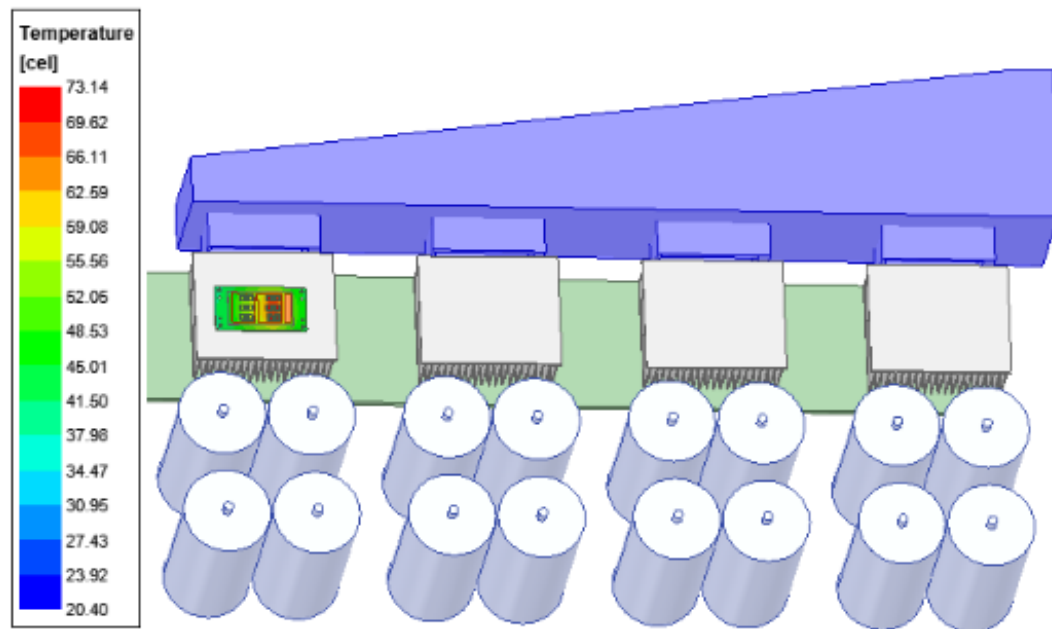


Figure 5.14. Temperature distribution of the power module.

5.3.3.3 Airduct Integrated with Heatsink

The last section 5.3.3.2 explores equal air velocity design based on ventilation theory; however, the air duct takes significant space which is nearly half of the power modules it aims to cool. To reduce the size of the cooling system, a more compact airduct is needed. This section investigates the air duct integrated with heatsinks, where heatsinks are placed inside a rectangular air duct. Calculating the airflow becomes more challenging due to the obstruction of the heatsinks.

However, assuming the air duct is ideally airtight, the principle of conservation of mass dictates that the volume of air flowing in must equal the volume flowing out, resulting in a uniform air velocity across the heatsinks. In the simulation, the power module model is simplified as a rectangular heat source to streamline meshing and computational efforts, given that the dies and DBC of the power module are significantly smaller than the heatsink and air duct. The CFD simulation imposes an inlet velocity constraint of 14 m/s based on measured values. The airflow direction is from left to right. Analysis of the cross-sectional view reveals a relatively uniform airflow across the four heatsinks, ranging from around 4 m/s at the bottom of the fin to 8 m/s at the base in **Figure 5.15**.

Notably, the maximum surface temperature of the heatsinks increases gradually from 25 °C at the first heatsink to 32 °C at the fourth heatsink in **Figure 5.16**. This temperature variation is attributed to the downstream air being hotter than the upstream air, contributing to the thermal behavior observed in **Figure 5.17**.

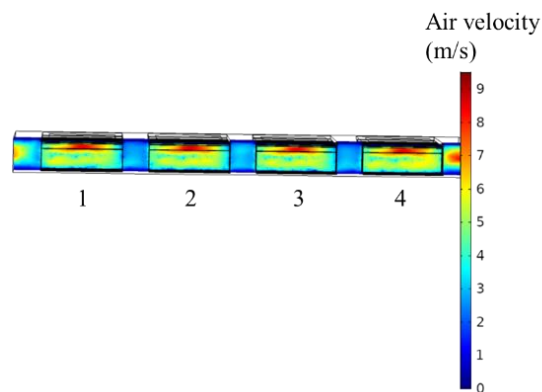


Figure 5.15. Air velocity of straight air duct with heatsinks.

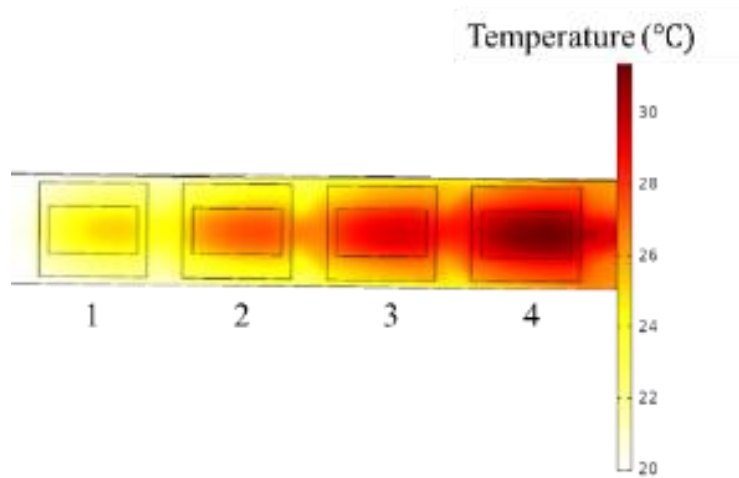


Figure 5.16. Heatsink temperature distribution.

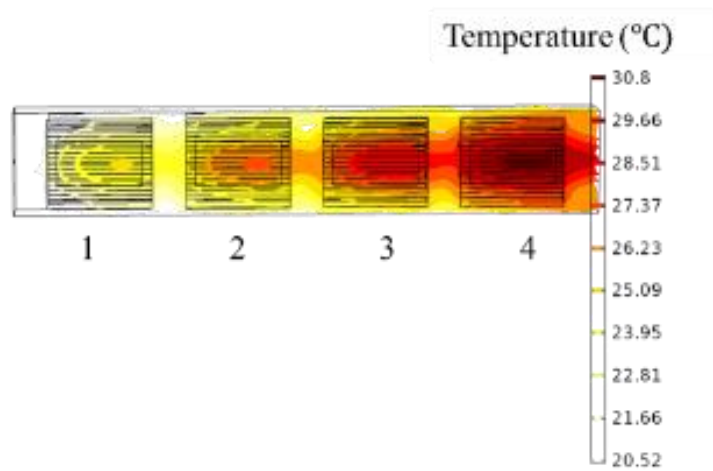


Figure 5.17. Air temperature across the duct.

5.4 Experiment Verification

5.4.1 Straight Airduct Air Velocity Measurement

The air velocity is measured at three cross sections marked I, II, and III between adjacent heatsinks as shown in **Figure 5.18**. At one cross section, ten measurements are made at horizontal positions 1, 2, 3, 4, and 5 from bottom to the top, as given in **Figure 5.19**. And $W = 15\text{ cm}$ and $H = 7\text{ cm}$.

The average flow rates were calculated from bottom to top at each position, and the overall average air velocity across all five positions offers a comprehensive view of the air duct's performance as listed in **Table 5-9**.

The flow rate experiences a slight decrease from 10.17 m/s to 9.42 m/s as the air passes through the first two heatsinks. However, after the third heatsink, the flow rate increases to 9.70 m/s . The flow rate drops due to the friction loss with the heatsink and the air duct. Also, the air duct is not entirely air proof. Despite these variations in the flow rate across different stages of the air duct, the overall average flow rate remains relatively stable.

This stability is consistent with the simulation results, confirming that the airflow distribution is well-maintained throughout the system. The minimal fluctuations indicate effective thermal management and airflow efficiency within the duct.

5.4.1.1 Air cooling verification

The test setup with a single heatsink is designed to closely resemble the conditions within an air duct, ensuring that the cooling performance in the test setup is representative of the final implementation. Identical Heatsink and Fan Usage: The test setup employs the same heatsink



Figure 5.18. Air flow velocity measurement locations.

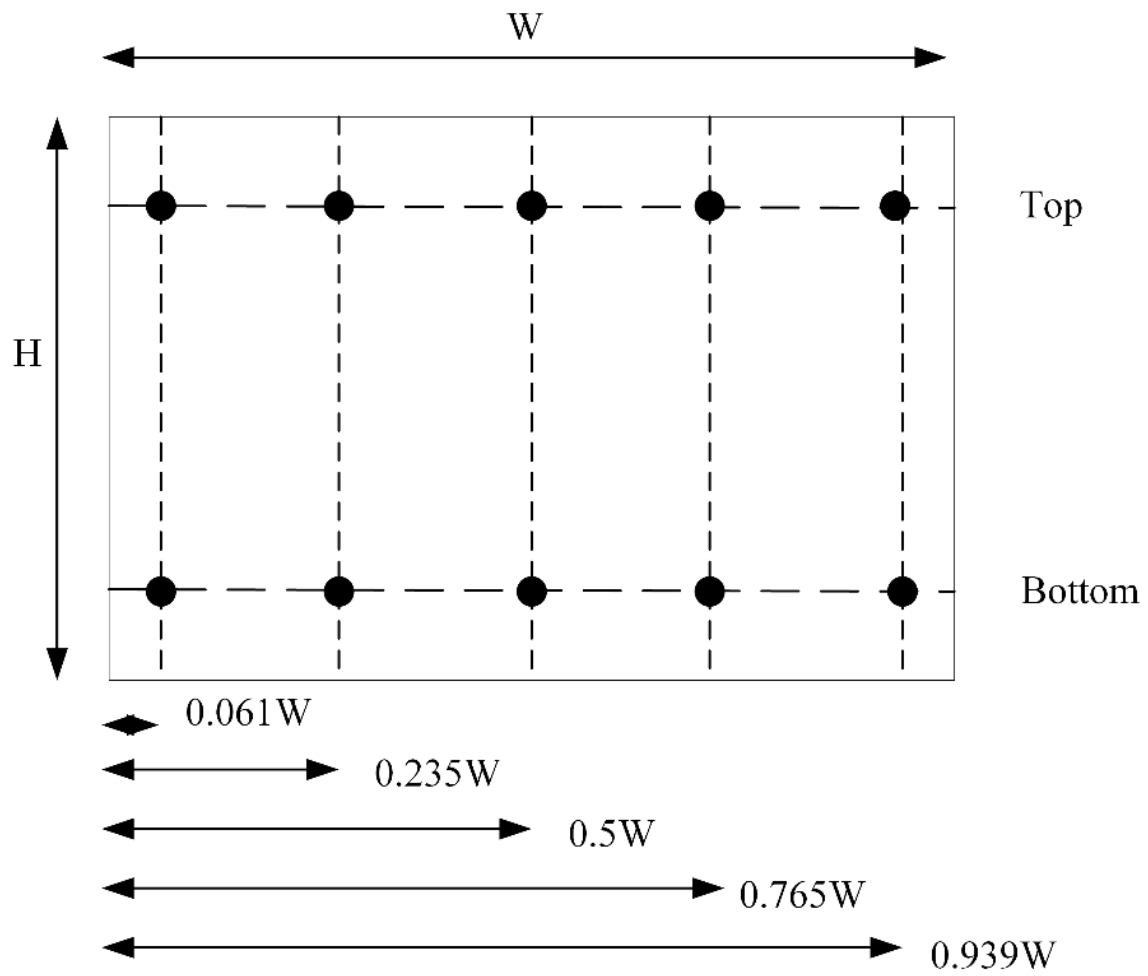


Figure 5.19. Flow rate measurement position at one cross-section.

Table 5-9. Air velocity measured at different positions.

Unit (m/s)	1			2			3		
Location	bottom	top	average	bottom	top	average	bottom	top	average
I	9.4	18.0	13.70	6.6	11.2	8.90	9.0	2.5	5.75
II	9.7	12.2	10.95	7.9	10.0	8.95	9.0	5.4	7.20
III	10.7	10.8	10.75	9.9	10.0	9.95	9.5	6.9	8.20
Unit (m/s)	4			5					
Location	bottom	top	average	bottom	top	average			
I	18.3	6.2	12.25	16.1	4.4	10.25			
II	14.8	7.4	11.10	10.6	7.2	8.90			
III	13.6	7.8	10.70	9.3	8.5	8.90			

and fan that will be used in the final air duct design. This ensures that the airflow characteristics, including velocity and distribution, remain consistent.

Airflow Validation Through Fan Adapter: In the air duct design, the fan is connected to the heatsink via a fan adapter. Measurements confirm that the air velocity remains nearly unchanged through the adapter, indicating that the adapter does not introduce significant losses or restrictions.

Matching Cross-Sectional Area: The cross-sectional area of the air duct is designed to match that of the heatsink. This prevents variations in airflow distribution that could arise from duct expansion or contraction, ensuring that the cooling conditions in the test setup accurately reflect those in the final implementation.

The test setup runs a half-bridge single submodule continuously at 5 kHz for five minutes at its full power rating of 6 kV and 50 A, resulting in a 300 W power loss. The hardware setup is shown in **Figure 5.20**. This mimics the operational conditions expected in the full MMC system, validating the heatsink's ability to manage thermal dissipation under real-world conditions. By replicating the airflow conditions and heat dissipation characteristics expected in the final system, the test setup effectively verifies that the heatsink will perform as intended when integrated into the air duct.

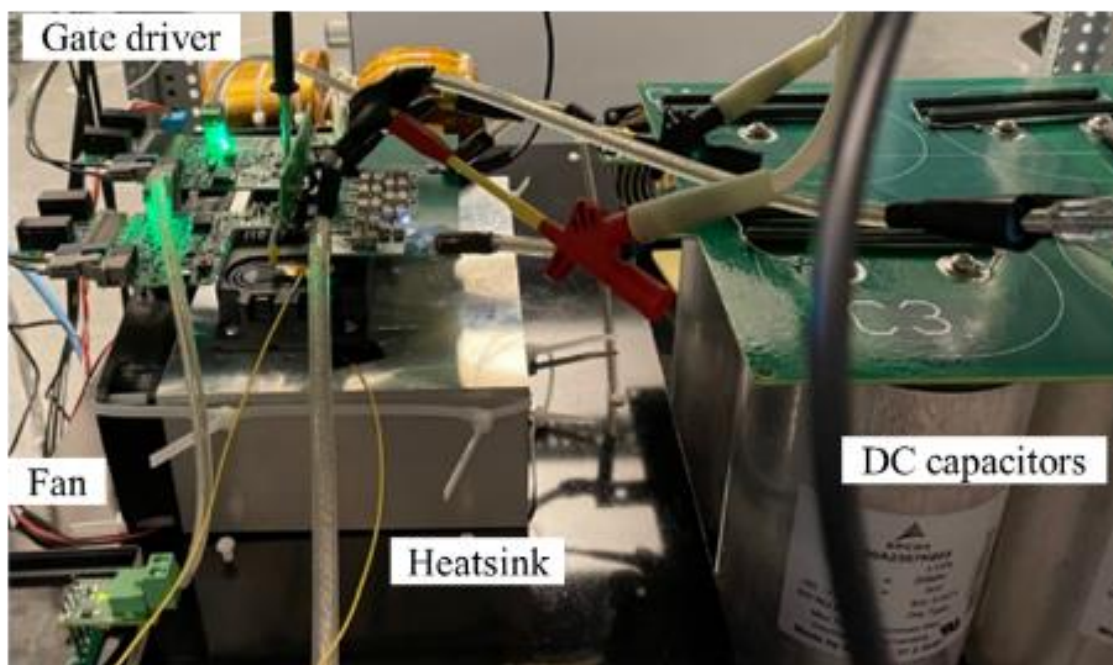


Figure 5.20. Submodule testing with heatsink

Using an Omega fiber optic temperature sensor, the blue curve in **Figure 5.21** illustrates the heatsink temperature's steady increase starting at 10.34 minutes, eventually reaching a thermal equilibrium state after approximately five minutes. During this period, the heatsink temperature stabilizes at 49.8°C, while the junction temperature of the power module is estimated to be around 65°C. These measured results align closely with both the simulation results presented in **Figure 5.9** and the theoretical calculations, effectively confirming the accuracy of the thermal design. This testing and comparison demonstrate that the heatsink and power module's thermal management system function as expected.

5.4.1.2 Liquid cooling verification

In addition to the heatsink testing, a performance evaluation was conducted using a two-pass cold plate (CP10G03) and a Poly Science chiller to assess the effectiveness of liquid cooling under similar operating conditions.

As shown in **Figure 5.22**, this setup was used to test the cold plate's performance under similar conditions. The cold plate's thermal resistance at a flow rate of 2 GPM and a coolant temperature of 25°C was determined to be 0.055 W/°C. This value corresponds to the last cold plate in the set, which experiences the highest coolant temperature, leading to a calculated cold

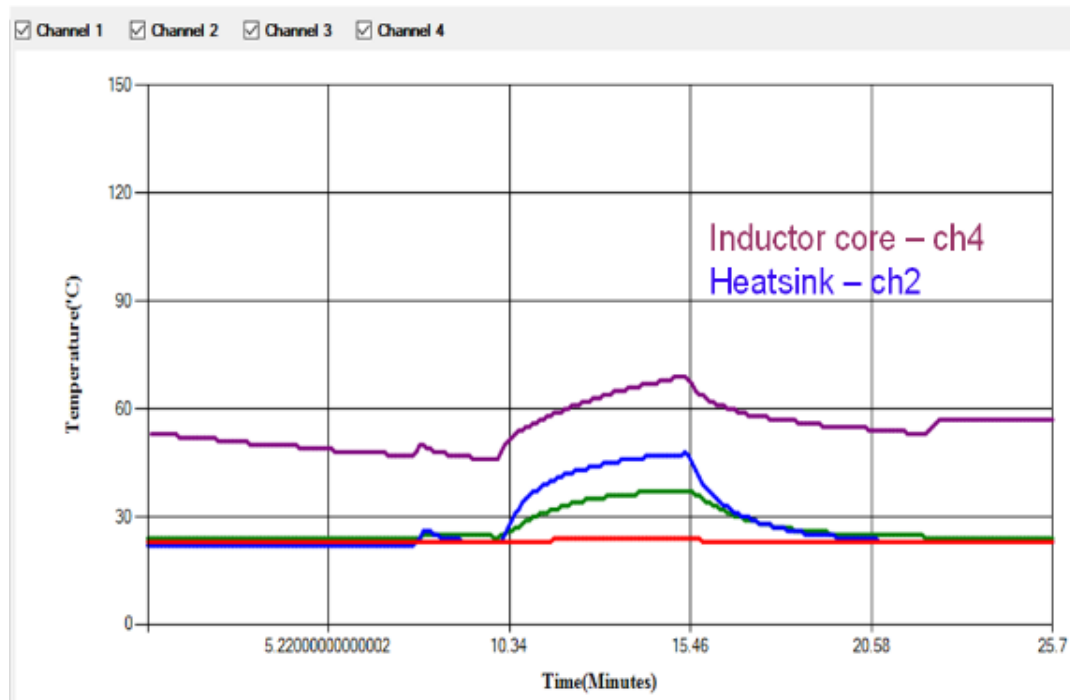


Figure 5.21. Heatsink temperature measured

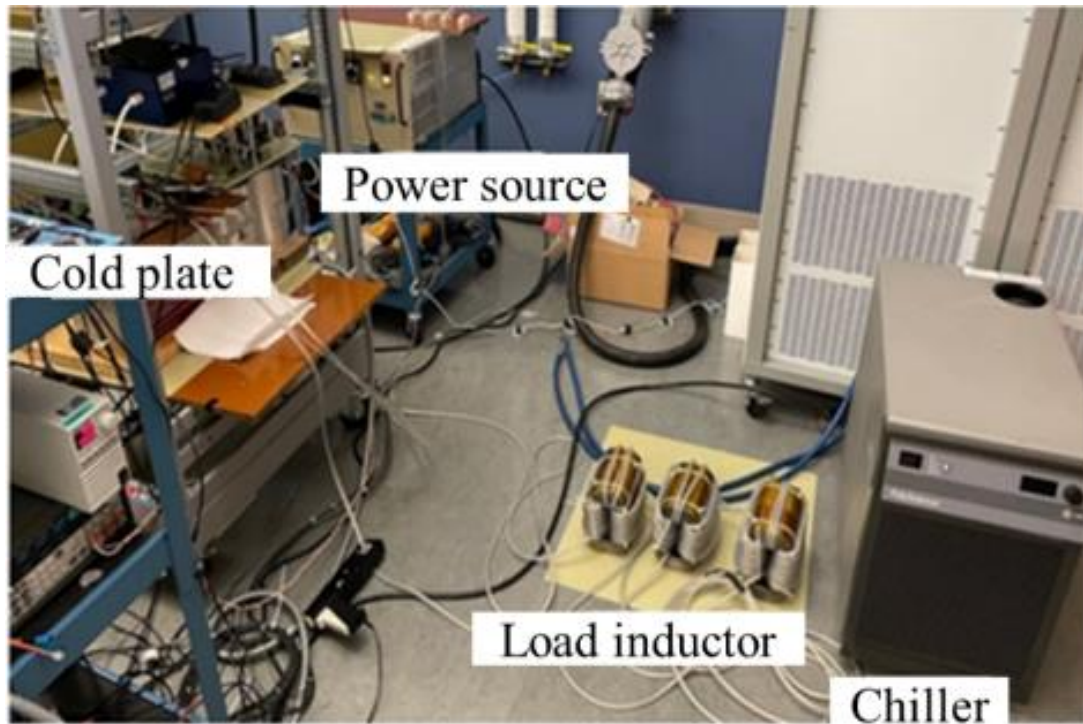


Figure 5.22. Single submodule testing with cold plate and chiller.

plate surface temperature of 41.5°C . The measured surface temperature was found to be 39°C , which falls within a reasonable range. These results validate the accuracy of the cold plate's thermal performance calculations at the specified flow rate and coolant temperature, confirming that the predicted cooling efficiency aligns closely with the actual test results.

5.4.2 Phase Leg Testing

In many cases, the heatsink is in direct contact with a dedicated fan to achieve optimum thermal performance. In this application, where the heatsink is connected to the source of the power module to preserve its insulation integrity, the heatsink has a minimum 6 kV voltage potential to ground reference. The clearance and creepage distance required between the heatsink and the fan makes placing the fan and heatsink in close range difficult. Especially, the high dv/dt of 10 kV power module which reaches more than 90 V/ns, seriously deteriorates air insulation capability.

Thus, in this design, the fan is situated 100 mm away from the high voltage potential heatsink, and air flow is distributed through an airduct, like the ventilation system in a building with a centralized air exchanger. This reduces the number of fans and avoids the insulation problem.

A straight air duct design is proposed, where the four heatsinks sit inside the rectangular air duct.. The heatsinks are separated from each other by 300 mm. Two identical fans rated at 24 V and 125 CFM, one is blowing in air from the right of the airduct, and another fan is extracting air from the left. The hot exhaust air is confined within an air duct, preventing heat from affecting adjacent electrical components. The MMC phase leg is illustrated in **Figure 5.23**. The MMC comprises of three distinct shelves. The top shelf accommodates dc link capacitors, the middle shelf houses MMC submodules and arm inductors, while the bottom shelf is dedicated to RC loads. Testing has been conducted with a 12 kV dc link voltage, lower than the proposed 24 kV target. This adjustment was made after multiple power modules failed during DPT at 6 kV. To preserve the remaining modules, the test voltage was reduced to 3 kV per submodule, resulting in a total of 12 kV DC link voltage in the 5-level MMC configuration. The load resistor is specified at $7.6\ \Omega$, and the load capacitor at $13.75\ \mu\text{F}$.

Figure 5.24 provides a visual representation of key performance metrics, including arm currents, output voltage, and load current. During testing, the measured heatsink temperature stabilizes at $28\ ^\circ\text{C}$, corresponding to a 50 W power module loss. The actual power loss is significantly lower than the maximum designed loss, which was established at a 24 kV dc link voltage, with additional safety margins considered.

The deviation from the original design specifications is the change in loading conditions. The initially intended resistive (unity power factor) loading cannot be tested in the lab due to the active power constraint of the Spellman high voltage power source. Instead, a mostly capacitive 0.039 power factor RC load is tested.

5.5 Summary

This chapter explored the cooling design challenges for a medium-voltage multilevel converter, addressing thermal management, power density constraints, and insulation requirements in both liquid cooling system and air cooling system. The detailed contributions are listed below:

- **System-Level Liquid Cooling:** Designed and analyzed multi-cold-plate configurations (series vs. parallel) for 24 power modules, addressing chiller integration, flow balancing, and system pressure drop—areas often overlooked in existing research.

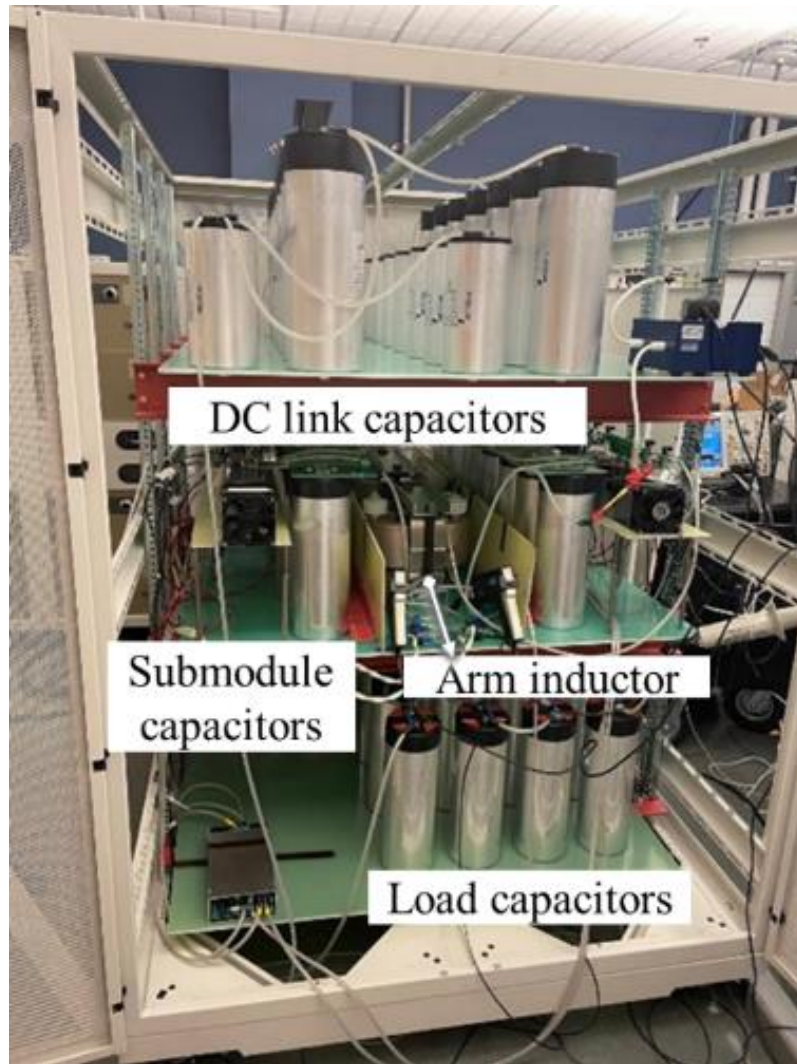


Figure 5.23. MMC phase leg test setup.

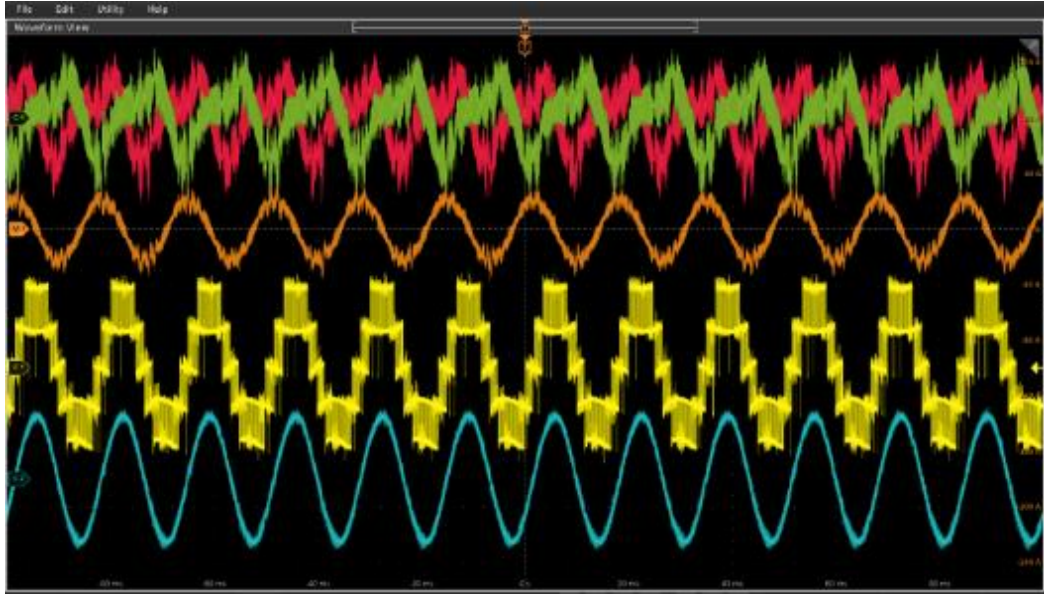


Figure 5.24. MMC test waveforms from top to bottom: upper arm current (20A/div); lower arm current (20A/div); output current (40A/div); PWM voltage (4kV/div); output voltage (4kV/div).

- Validated Air Cooling Strategies: Developed slanted ducts for uniform airflow. Tested another more compact integrated heatsinks airduct design with small flow rate drop. Experimental results aligned with CFD predictions, guiding practical air-cooled solutions for MV systems.
- Verified both liquid cooling and air cooling strategies under high voltage and high power conditions. Liquid cooling delivered superior thermal performance. Air cooling showed adequate thermal performance with advantages of cost-effectiveness and simple installation.

Chapter 6 8-level Flying Capacitor Converter Testing

The MMC presented in Chapter 5 cannot meet the 3.33 kW/L power density project target due to the large volume of submodule capacitors (66 μ F) and arm inductors (5 mH). To address this issue, a flying capacitor converter (FCC) topology is adopted, offering higher power density through the use of small flying capacitors and a more compact filter inductor.

The MV FCC is inherently complex, given the operation of multiple components within the system. Establishing a standardized test procedure is paramount to ensure each component's functionality and insulation strength. This involves conducting separate tests for each component before assembling them together for converter testing. This chapter delves into the individual components design of the power stage, sensors and mechanical layout. And finally, converter testing procedure regarding insulation, protection and operation at full power is presented.

6.1 Power Stage Parameters

The component parameters of the medium-voltage (MV) phase leg topology are listed in **Table 6.1**, and the corresponding 8-level flying capacitor converter circuit is illustrated in **Figure 6.1**. Two major components, the flying capacitor and output filter inductor are covered in this section.

Table 6-1. 8-level FCC parameters.

Component	Parameters
Device	Wolfspeed XHV-9 10 kV/100 A SiC MOSFET Switching frequency: 5 kHz/device, Loss: 150 W each device
DC link	Voltage: 24 kV Capacitance: 82.9 μ F
Limiting resistor	Two 2 k Ω resistors in parallel, and two of them in series
Filter inductor	Inductance: 2.5 mH Current: 60 A max / 22 A RMS

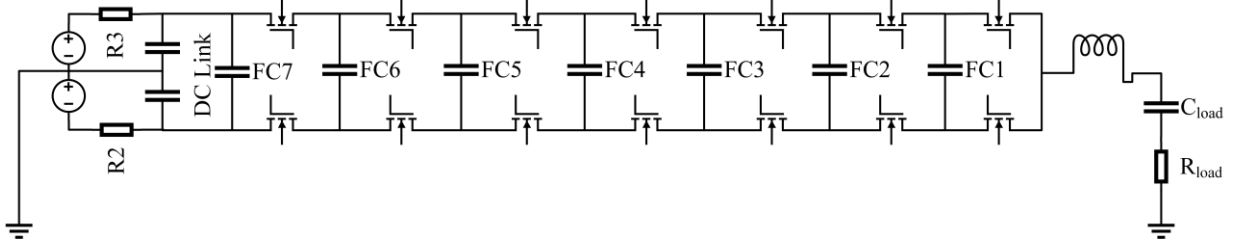


Figure 6.1. 8-level flying capacitor converter schematic.

6.1.1 Flying capacitor selection

In low-voltage applications, flying capacitors with the same voltage ratings and capacitance values are utilized across various stages in an FCC. The capacitance for these flying capacitors is defined by (6.1).

$$C = \frac{I_{out,max}}{\Delta V_{cf} f_{sw} (N - 1)} \quad (6.1)$$

where f_{sw} denotes the switching frequency, ΔV_{cf} is the required voltage ripple, and $I_{out,max}$ refers to peak output current. However, when this principle is applied in MV settings, it results in oversized flying capacitors for the FCC stages operating at higher voltage levels. For example, the initial stage operates at a rated voltage of 3.57 kV, whereas the seventh stage is rated at 24 kV in the examined 8-level FCC. To accommodate the voltage needs of the final stage, seven flying capacitor units from the first stage must be connected in series, which reduces the capacitance to one-seventh. This configuration requires seven such units to be paralleled to maintain the same total capacitance, leading to the flying capacitor in the last stage being 49 times larger than that in the first stage. To address the issue of size, this design keeps the voltage ripple percentages at 10% consistent across the different FCC stages, allowing for smaller capacitance requirements for flying capacitors in the higher stages. Overall, for the x^{th} stage, the size of the flying capacitor decreases from x^2 to x times that of the first stage.

The flying capacitors (FCs) follow a modular design. The first-stage FC1 consists of four 1.1 kV, 40 μF capacitors (TDK B32778G0406K00) connected in series on one daughter board. For subsequent stages, the x -stage FC will include x daughter boards, maintaining the same modular design approach. To manage the voltage stress on the power module effectively, the maximum drain-source voltage for the x -stage can be calculated by considering the voltage ripple induced by the charging and discharging of the adjacent flying capacitors in Equation (6.2) [131].

Because of the phase shift control, the maximum charging and discharging time for the FCs is determined as $\frac{1}{7f_{sw}}$. Note that for the 5th and 6th stages, the number of flying capacitors is doubled to ensure the device voltage remains below 4 kV. If not, the device voltages could reach 4.2 kV and 4.4 kV, which would compromise their reliability.

$$V_{x,max} = \frac{V_{dc}}{7} + 0.5\Delta V_{FCx} + 0.5\Delta V_{FCx-1} = \frac{V_{dc}}{7} + \frac{1}{14} \frac{I_{out,max}}{f_{sw}} \left(\frac{1}{C_{FCx}} + \frac{1}{C_{FCx-1}} \right) \quad (6.2)$$

The values of the flying capacitors are listed in **Table 6-2**. The device voltage is further validated through simulation as illustrated in **Figure 6.2**, confirming that it remains within the 4000 V limit. Due to the symmetrical configuration of the lower and upper devices, only the upper devices are presented. The flying capacitor voltage ripples of FC7 to FC1 are 427V, 499 V, 394V, 589V, 458V, 325V, 180V, respectively as shown in **Figure 6.3**, which are all maintained below 10% of the operating voltage, thereby meeting the design specifications.

Another important design consideration for flying capacitors is their current handling capability, particularly the RMS current rating. In this design, the flying capacitor is subjected to a pulsed current waveform with a switching frequency of 5 kHz and an effective RMS current of approximately 17 A. The capacitor selected for this application has a manufacturer-specified maximum RMS current rating of 21.5 A, measured at 10 kHz and an ambient temperature of 70 °C. Since the actual operating conditions involve a lower switching frequency (5 kHz) and an RMS current that is significantly below the rated limit, the thermal stress on the capacitor is substantially reduced. Lower frequency operation typically results in reduced dielectric losses and lower equivalent series resistance (ESR)-related heating. Therefore, under the given electrical and thermal conditions, the capacitor is expected to operate well within safe thermal limit.

Table 6-2 Flying capacitor values at seven stages.

Capacitor	FC1	FC2	FC3	FC4	FC5	FC6	FC7
Value (uF)	10	5	3.33	2.5	2*2	1.66*2	1.426

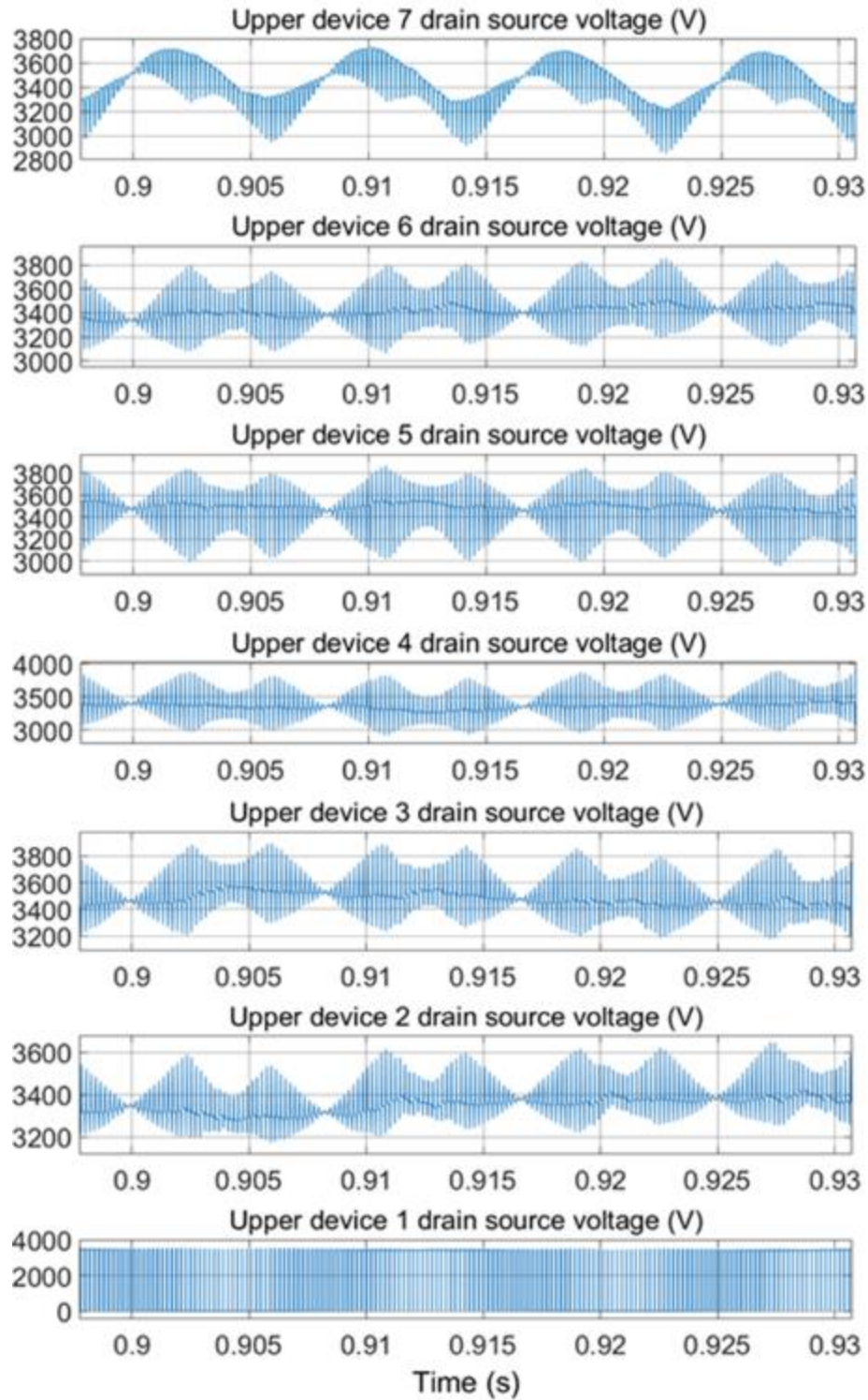


Figure 6.2. All seven upper devices drain source voltage is within 4 kV limit.

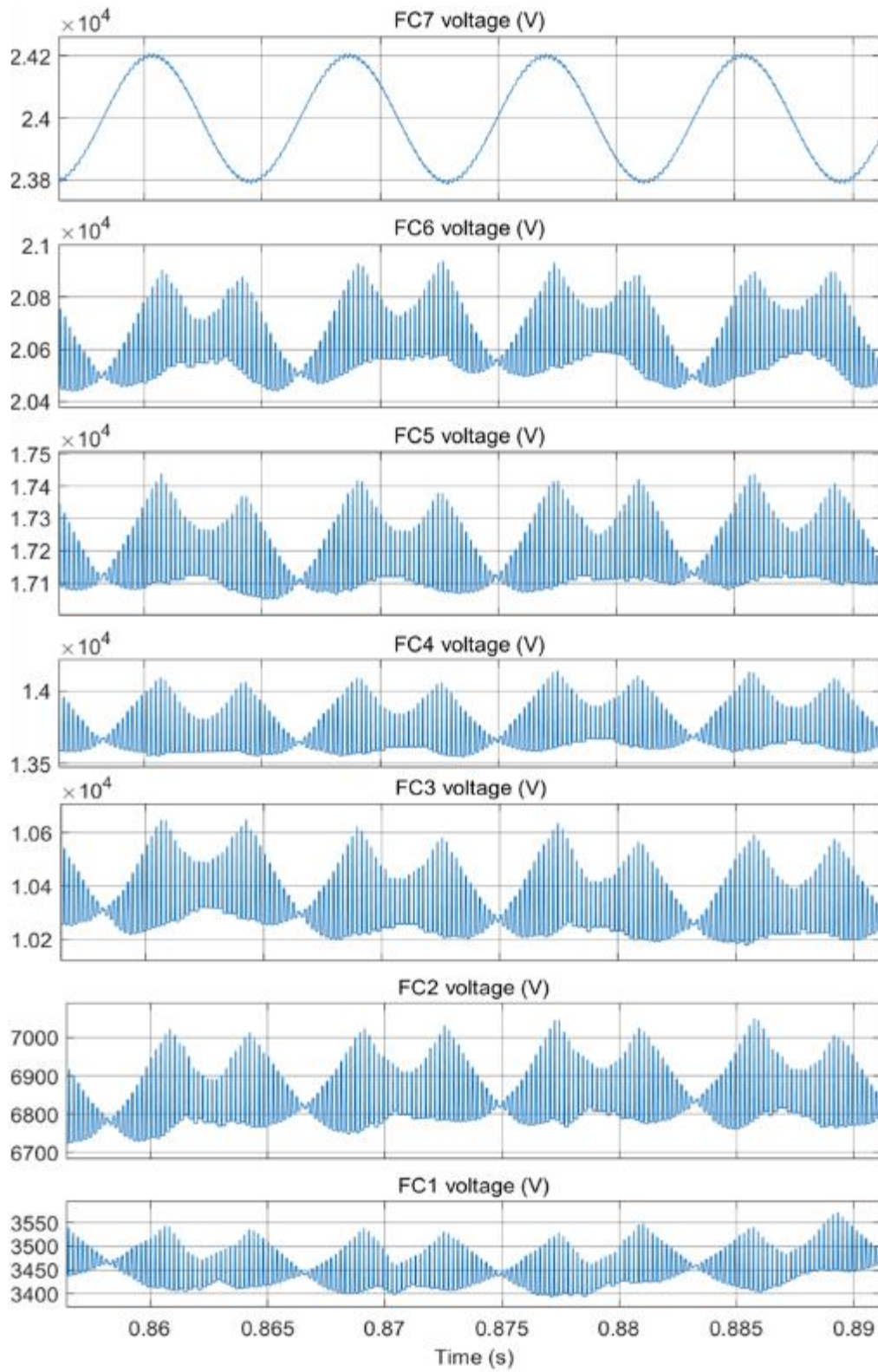


Figure 6.3. Voltage ripple values of flying capacitor voltage 7-1 are 427V, 499 V, 394V, 589V, 458V, 325V, 180V, respectively.

6.1.2 Filter inductor

For the source side inverter with L filter, the relationship between phase side voltage V_{ph} , the source side voltage V_s and source side phase current I_s and power factor angle φ is expressed in (6.3)

$$V_{ph} = \sqrt{V_s^2 + \omega_0^2 L^2 I_s^2 - 2\omega_0 L I_s V_s \sin\varphi} \quad (6.3)$$

where L is the filter inductance and ω_0 is fundamental angular frequency. With unity power factor, for a 0.01 p.u. inductance value, V_{ph} is approximately equal to V_s . For this 1 MVA, 13.8 kV system, the inductance of 0.01 p.u. is 5.05 mH.

We can verify the selected inductance value through simulation by ensuring that the distributed energy resource (DER) output current TRD (Total Rated Distortion) remains below 5%, in compliance with the IEEE 1547 standard. Initially, an inductance of 5.05 mH was used in simulation to evaluate TRD. The inductance can be reduced to 2.5 mH to improve converter power density without exceeding the TRD limit, achieving a TRD of 4.9% as shown in **Table 6-3**.

This reduction still meets the TRD requirement as illustrated in **Figure 6.4**. By reducing the size of the inductor, space is conserved in the overall design, allowing for a more compact and efficient layout. Minimizing losses in the inductor also contributes to better energy efficiency and reduces heat generation. Furthermore, the current ripple is restricted to less than 20% to achieve an optimal balance between performance and efficiency.

Table 6-3. TRD at different filter inductance.

Filter inductance (mH)	TRD
5.05	2.6%
2.5	4.9%
2.0	6.1%

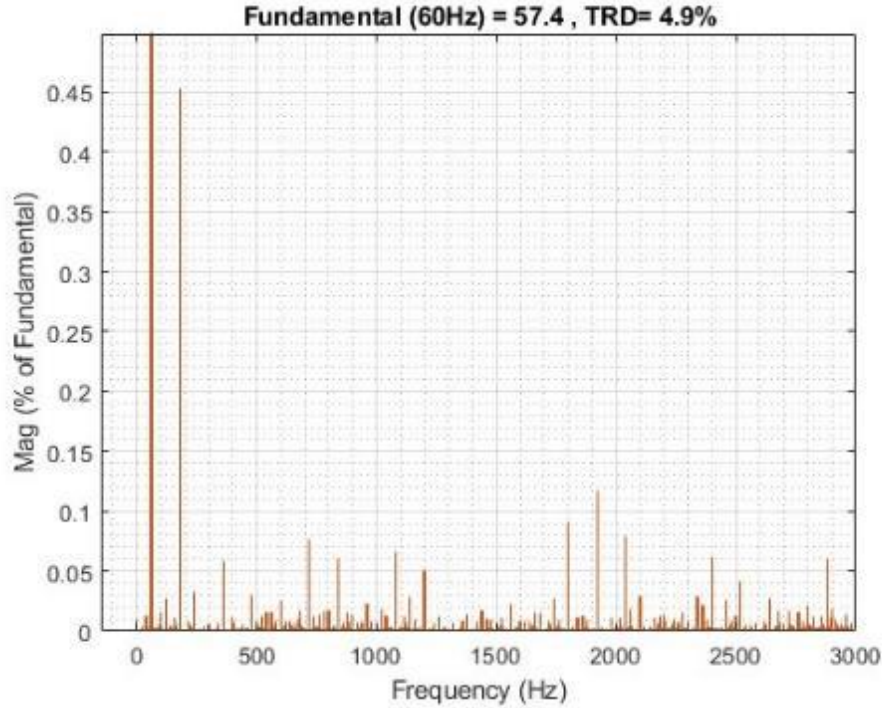


Figure 6.4. Harmonic current percentage when filter inductance is 2.5 mH.

6.2 Power Module Test

Originally, the MV converter comprised an 8-level FCC which is composed of 7 half-bridge power modules in one phase leg. Given that the power modules are still undergoing research and have been produced in two separate orders, static characterization tests are conducted on both the upper and lower devices of the same power module from each order. This is to evaluate whether the power modules have similar R_{dson} and transconductance.

The first batch of power modules, including modules 224, 225, 227, 291, 292, and 293, are represented by data points 1-12, while the second batch, consisting of modules 281, 314, 346, 241, and 280, are represented by data points 13-22. During forward conduction tests, it is observed from **Figure 6.5**, that the upper and lower devices within each module exhibit similarity, and most modules demonstrate uniform behavior, except for modules 241 and 280, when the gate voltage is set to 15 V. Consequently, most modules exhibit comparable on-state resistance and conduction loss.

However, it is noted that when the gate voltage is reduced to 10 V, the first batch of modules reaches saturation earlier than the second batch, as illustrated in **Figure 6.6**. At 60 A, voltage

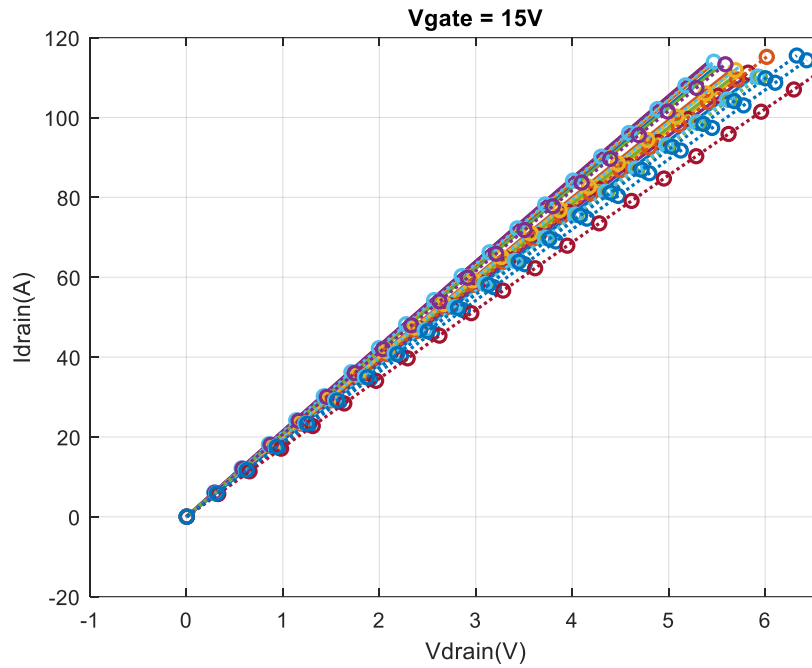


Figure 6.5. Forward conduction curves of ten 10 kV SiC MOSFET power modules when $V_{gs}=15$ V.

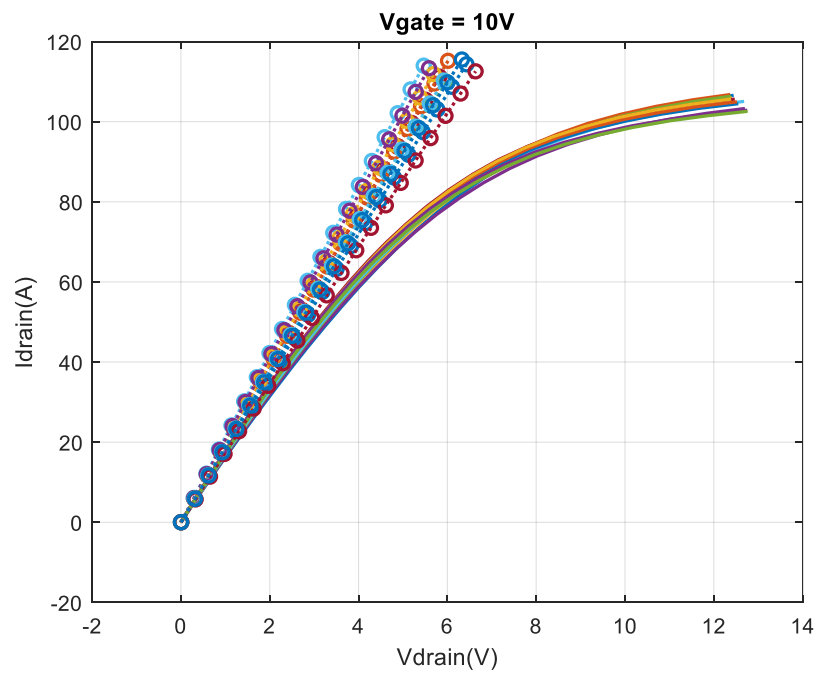


Figure 6.6. Forward conduction curves of ten 10 kV SiC MOSFET power modules when $V_{gs}=10$ V.

Figure 6.7. Transfer conduction curves of ten 10 kV SiC MOSFET power modules.

drop across modules is 2.8 V to 3.5 V when gate voltage is 15 V. Thus, it is best to switch on the power module with 15 V gate voltage for lower voltage drop and conduction loss. The transfer curves in **Figure 6.7.** show more uniformity, which indicates the power modules share similar switching speed thus similar switching loss.

Due to the failure of some modules above 4 kV, a hipot test was conducted on all 50 received modules. The power terminals were shorted together, and a high voltage of 7 kV was applied between the terminals and the baseplate to screen for modules exhibiting exceptionally high leakage current. Only those modules with low leakage current (less than 1 mA) were selected for further evaluation. It is important to note that the hipot test alone does not guarantee reliable insulation performance, as the actual application involves a 5 kHz PWM voltage applied between the drain and source terminals. Therefore, the selected modules subsequently underwent DPT at 3.3 kV to verify their switching performance under high-voltage conditions. Modules that passed both the hipot and DPT tests were assembled into the phase leg configuration.

6.3 Sensor Calibration

6.3.1 Current Sensor Calibration

Calibrating the current sensor is crucial because the closed-loop control of the converter relies on accurately sensing current direction to adjust the duty cycle effectively. The current sensor consists of a 100 A hall effect sensor, which converts current into a voltage signal. This voltage signal then undergoes amplification to enhance its sensitivity in proportion to the current. Subsequently, the voltage signal is converted into a frequency signal by a VFC and transmitted to the controller via optical fiber.

Since the current sensor measures AC output current, it is calibrated for both current directions. The test setup consists of a TDK GEN30-50 (0-50 A) power supply connected with several resistors. The main bus wire goes through the current sensor. The power supply controls the output current feeding into the sensor, and the frequency is read from the controller side. From **Figure 6.8.** frequency increases linearly with current. The lowest frequency is 1.34 MHz, meeting the requirement of 10x the current loop control bandwidth at 5 kHz.

6.3.2 Voltage Sensor Calibration

Each level of the flying capacitor converter is monitored by a dedicated voltage sensor to ensure stable operation and prevent overvoltage conditions. These sensors consist of a series of voltage dividers that scale down the voltage before feeding it into a VFC as shown in **Figure 6.9.**

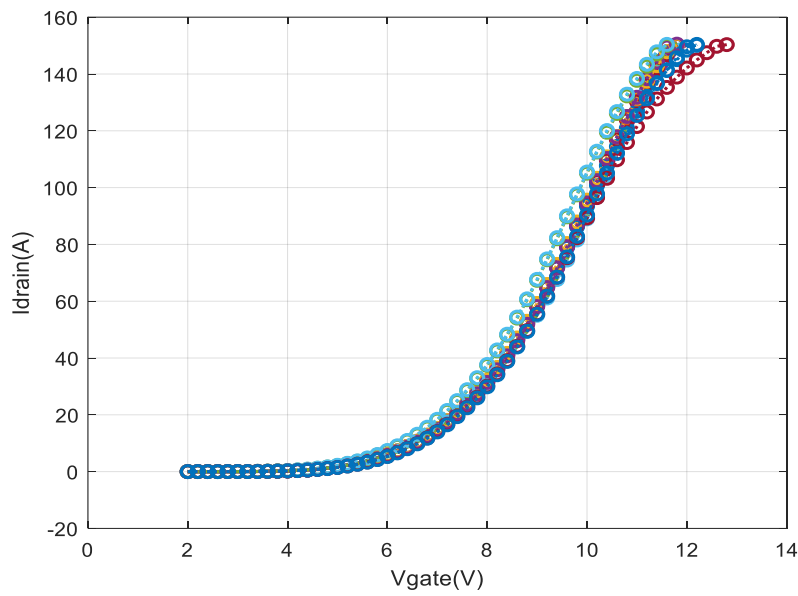


Figure 6.7. Transfer conduction curves of ten 10 kV SiC MOSFET power modules

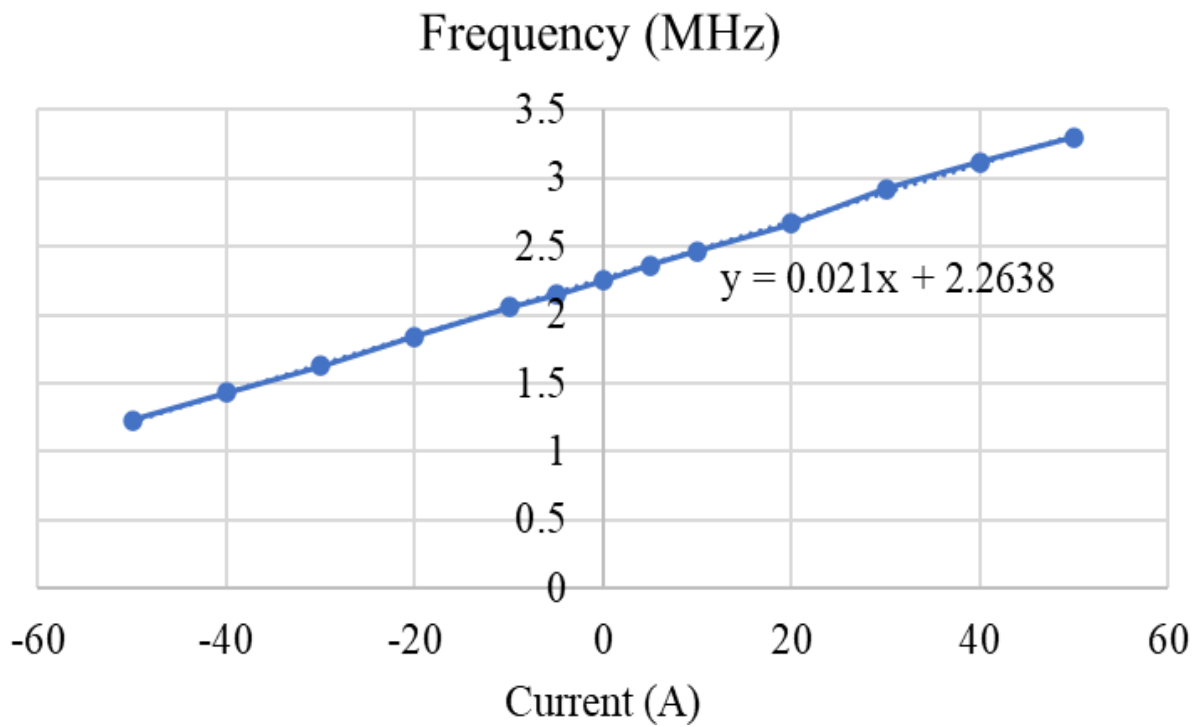


Figure 6.8. Current sensor output frequency vs current.

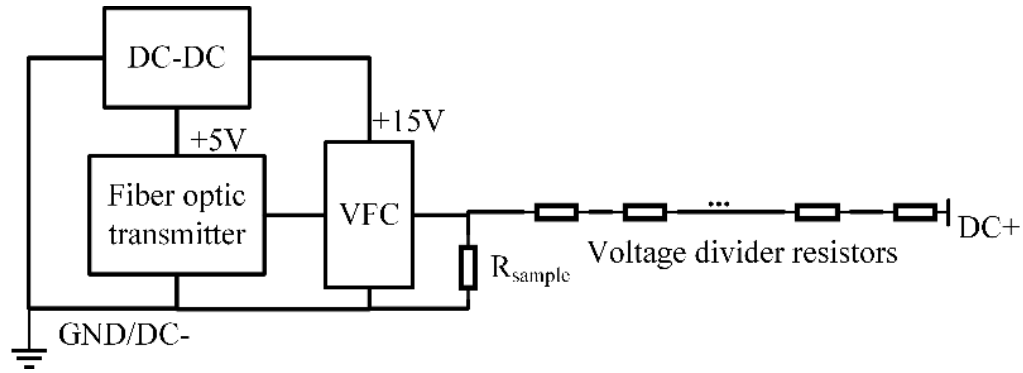


Figure 6.9. Voltage sensor diagram.

The VFC then converts the voltage into a high-frequency signal, which is transmitted via optical fiber to the controller.

This voltage information is crucial for two key protection mechanisms: Flying capacitor overvoltage protection (OVP) prevents excessive voltage in any capacitor level. Device OVP, by subtracting adjacent flying capacitor voltages, the drain-source voltage of each switching device can be determined, allowing for real-time monitoring and protection.

Since each phase leg contains seven voltage sensors, calibration is necessary to ensure uniform output across all sensors when subjected to the same input voltage. This enhances the accuracy of the OVP mechanisms. During calibration, a power supply applies a constant voltage to the R_{sample} , and the VFC output frequency is measured using an oscilloscope. The measured data for voltage sensors V1 to V7 is shown in **Figure 6.10** and presented in **Table 6-4**. Output frequency deviation stays within 2% across seven sensors at the same voltage.

6.4 Mechanical Design of MV Phase leg

As it is a modular design, each power module with its gate driver, desat diode, connection board with the flying capacitor (FC) and heatsink is depicted in **Figure 6.11**. The heatsink is installed with field shaping rings and a trapezoidal platform underneath to prevent potential corona discharge.

6.4.1 Busbar Design

The FCs are implemented using a modular design. The first-stage FC is built on a single daughter board that houses four 1.1 kV, 40 μ F capacitors connected in series. For higher stages, an x-stage FC is formed by integrating x daughter boards, following the same modular approach.

Table 6-4. Voltage sensor output frequency (MHz)

Vsample(V)	V1	V2	V3	V4	V5	V6	V7
0.5	0.2036	0.2023	0.2056	0.2031	0.2047	0.204	0.204
1	0.4074	0.4056	0.4096	0.4068	0.4087	0.407	0.4084
4	1.642	1.637	1.639	1.641	1.645	1.647	1.637

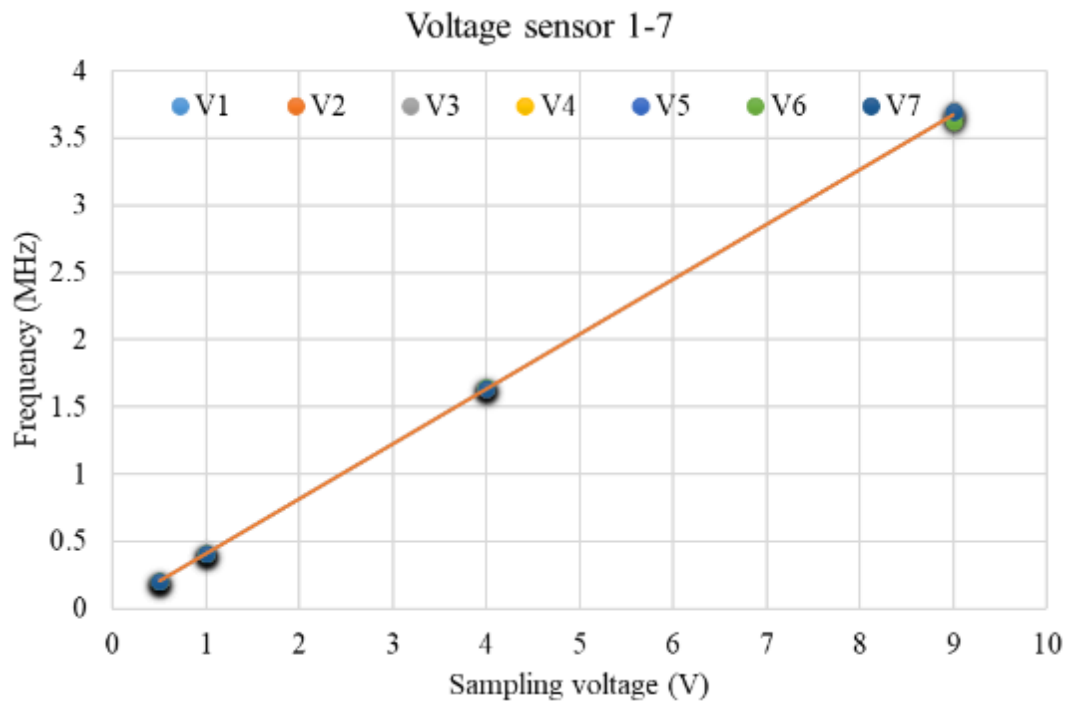


Figure 6.10. Voltage sensor output frequency vs input sampling voltage.

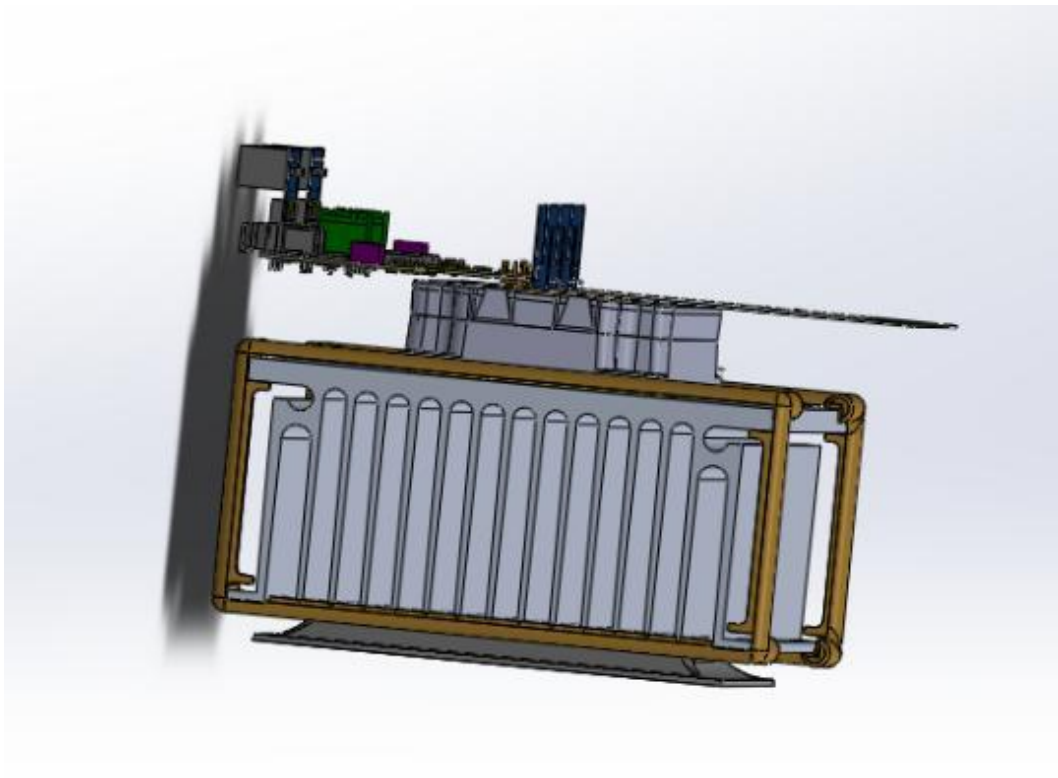
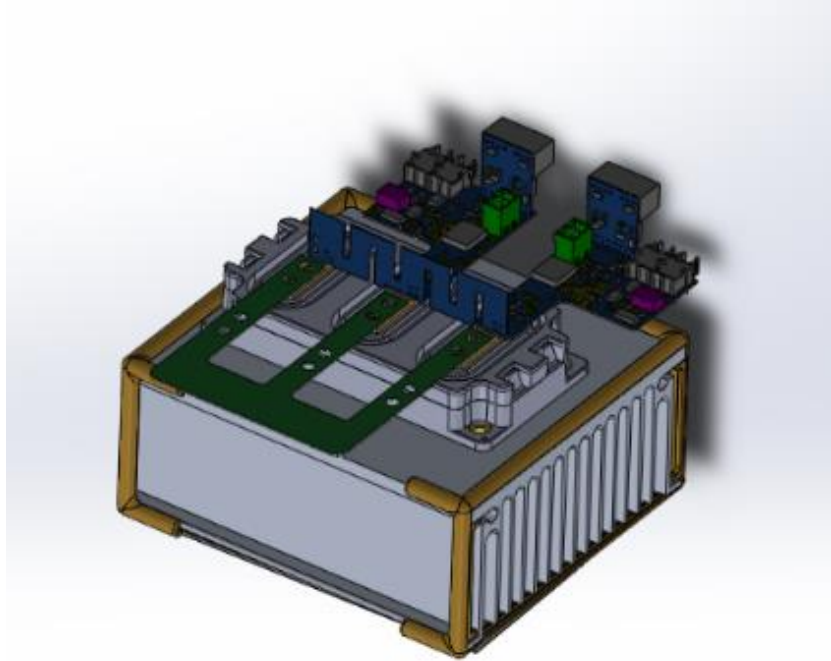


Figure 6.11. Power module with gate driver and heatsink.

This configuration directs the current along a zigzag path, which effectively reduces loop inductance through flux cancellation.

Due to the 8 kV voltage difference between adjacent capacitors at the edge, a slot measuring 15 mm in width and 52.5 mm in depth is introduced between their pads. This design achieves a creepage distance of 123.5 mm and a clearance distance of 52.5 mm, thereby providing a 30% safety margin above the 40 mm clearance distance required by IPC-2221B for surface tracks.

Furthermore, the PCB tracks connecting the capacitors are 20 mm wide and made with 2 oz copper on both the top and bottom layers. When conducting 60 A of current at an ambient temperature of 25 °C, these tracks experience a temperature rise of approximately 10 °C. The PCB itself is 120 mil thick, ensuring sufficient structural strength to support up to 28 capacitors.

Busbar design is essential for minimizing the commutation loop inductance in flying capacitor converters, ensuring fast switching and reducing voltage overshoot and oscillation. To achieve this, flying capacitors are placed between switching devices, while adjacent capacitor stages are stacked vertically to promote loop cancellation. This arrangement shortens the current paths and minimizes parasitic inductance, thereby improving overall switching performance.

As shown in **Figure 6.12** and **Figure 6.13**, the even-stage FCs are positioned at the bottom, while the odd-stage FCs are placed on top. A 1/4" G10 Garolite board is inserted between them, serving as an insulation barrier and structural support.

The layout of the high-voltage, high-current components is carefully designed, with these components positioned centrally between the power modules. Low-voltage components, such as the APS and the gate drivers are located at the edge of the power modules. This creates a clear separation between the primary and secondary side components, which maintains adequate insulation distances and minimizing the risk of electrical arcing. Additionally, the design reduces the signal distortion caused by radiated EMI, thereby protecting sensitive control circuits.

Another critical consideration is the output cable connected to the filter inductor. This cable is a high dv/dt and di/dt point, which can introduce transient disturbances. To mitigate these effects, it is vital that the APS and its connection wires be placed away from the filter inductor.

The power stage in **Figure 6.14**, occupies a volume of 0.096 m³, which meets the 3.33 kW/L power density requirement specified in the project's statement of work. However, when the decoupling capacitors is considered, the total volume increases to 0.122 m³, thereby failing to meet the specified power density target. To address this issue, an optimization strategy will be

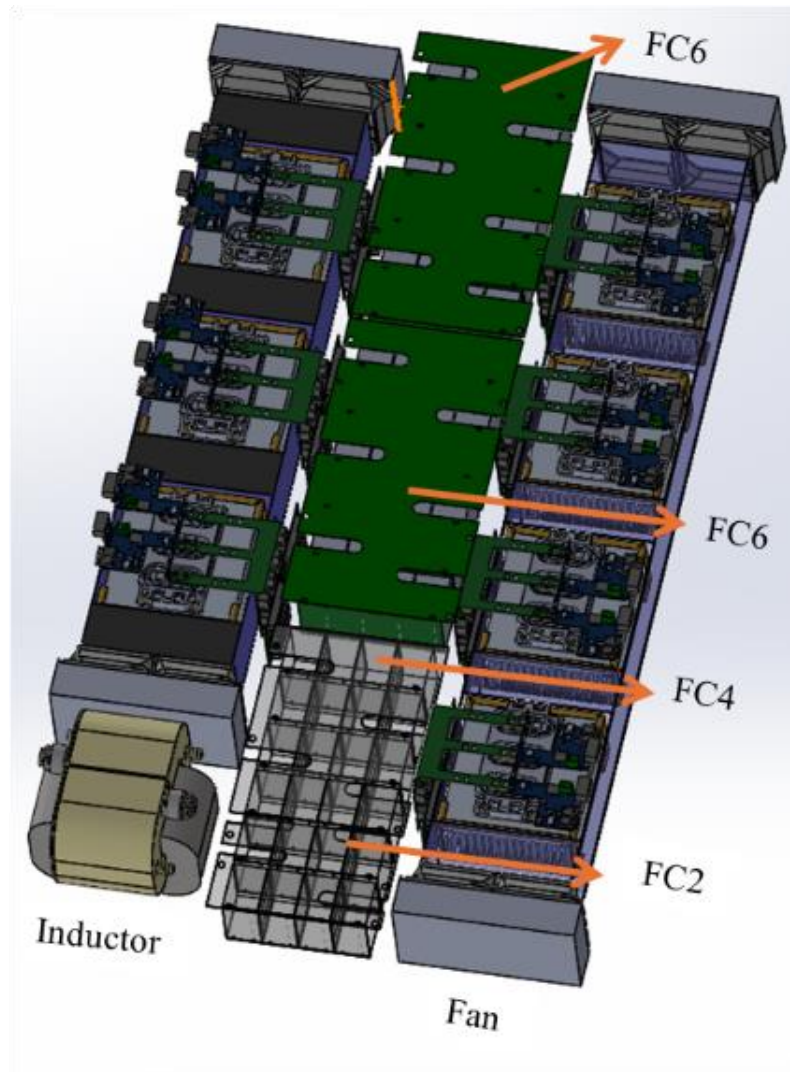


Figure 6.12. FCC phase leg layout first layer.

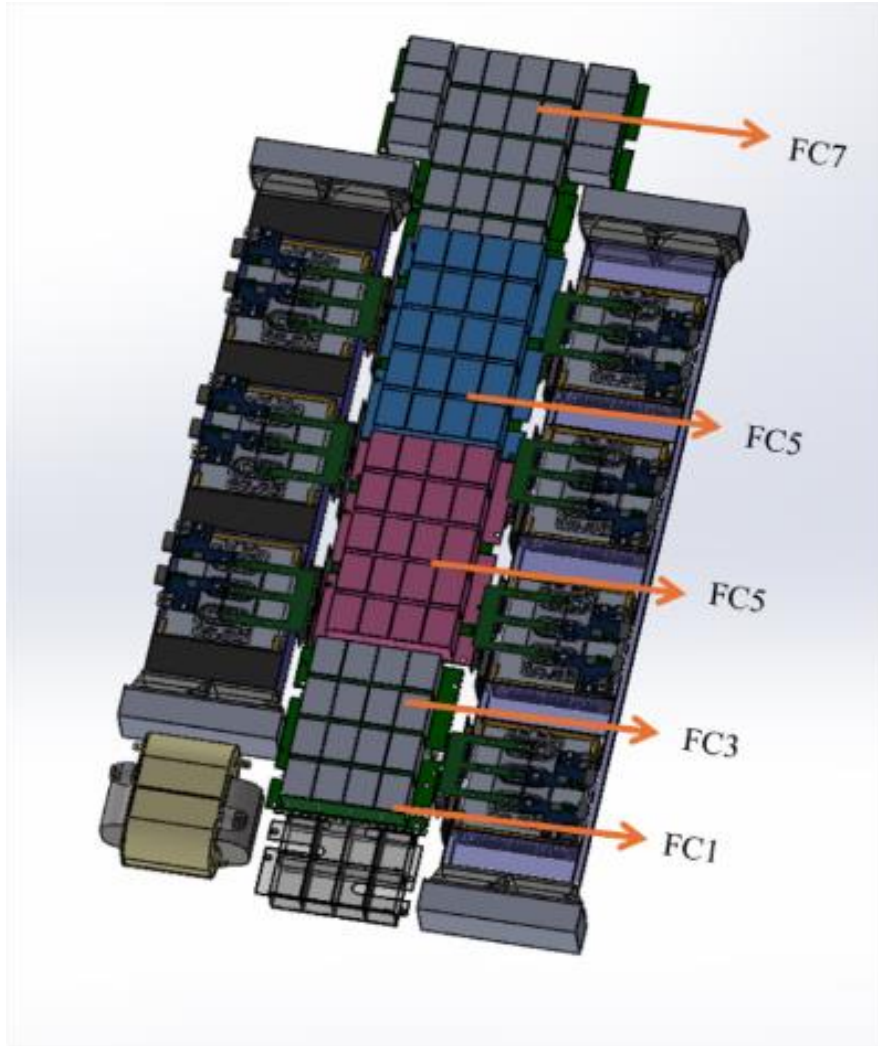


Figure 6.13. FCC phase leg layout second layer.

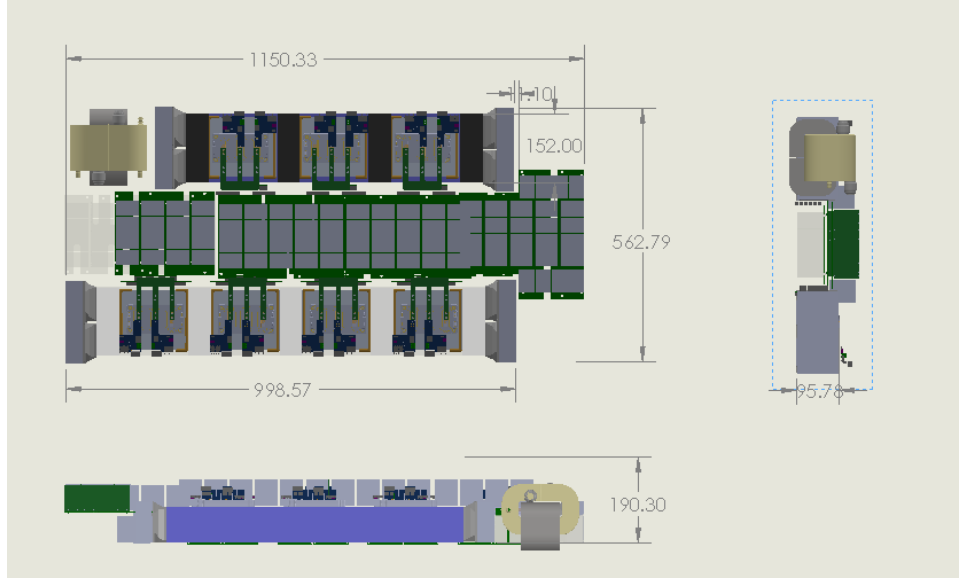


Figure 6.14. 8-level FCC dimensions.

presented in the next chapter, in which a smaller ceramic capacitor is selected to reduce the overall system volume. The final physical assembly is shown in **Figure 6.15**. the red decoupling capacitors are positioned above the FCs at the center of the structure, while the APSs are mounted adjacent to each gate driver.

6.5 MV phase leg testing

Before the assembly of the MV phase leg, each high-voltage component undergoes insulation testing to ensure its reliability and safety. Power modules are tested using a 3 kV DPT, while the APS is verified to be PD-free up to 15 kV. Partial discharge (PD) testing was conducted on adjacent heatsinks, with an inception voltage of 13.16 kV, to verify their insulation integrity. Additionally, the heatsink–fan assembly was tested up to 15.5 kV to ensure sufficient dielectric strength between components. Additionally, components like voltage sensors, flying capacitors, and decoupling capacitors are subjected to hipot tests to ensure their insulation quality.

6.5.1 Static voltage test

Once the components are assembled into the converter, a comprehensive system-level insulation test is performed. During this test, gate signals are intentionally disabled to keep the power modules in off state. The DC link voltage is gradually increased to 20 kV while closely monitoring for any signs of PD. This evaluates the insulation of the entire system under static high-voltage conditions.

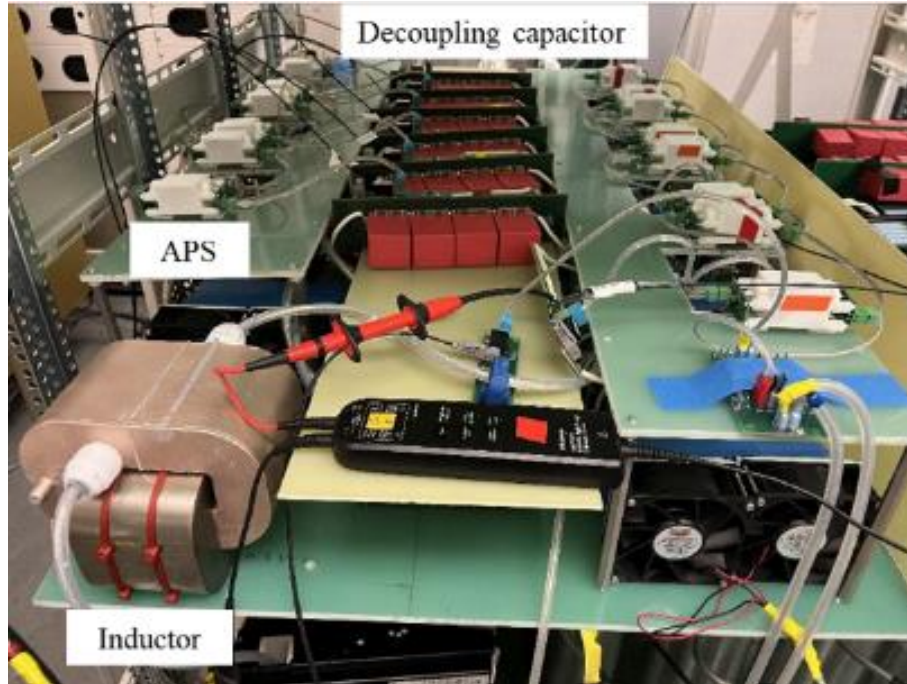


Figure 6.15. FCC test setup.

During testing, a snapping sound was heard when the DC voltage exceeded 20 kV, accompanied by voltage spikes observed on the oscilloscope. The test was immediately halted, and once the DC link voltage dropped to zero, all connections—including the DC link capacitors and balancing resistors—were thoroughly checked to ensure none were open-circuited.

Despite multiple test repetitions, the issue persisted. Further investigation revealed that the metal frame of the input resistors, which were used to limit input current and prevent overcurrent protection triggering in the Spellman power supply, was the root cause. The metal frame had sharp edges, leading to air discharge when subjected to high voltage. After removing the metal frames, subsequent tests showed no voltage spikes on the DC link voltage at 24 kV, confirming that the issue was resolved.

6.5.2 Voltage balancing and protection

The flying capacitor OVP and device OVP were tested separately. During initial testing, the DC link voltage gradually increased, allowing the flying capacitor voltages at each level to rise due to the balancing resistors. To prevent device degradation, no gate signals were applied to the power devices. The OVP threshold was set according to the DC link voltage. For example, if testing at 5 kV DC link voltage, the protection was expected to trigger at 130% of this value. The

voltage signals received by the controller were monitored on an oscilloscope, confirming that all seven voltage levels exhibited uniform frequency, indicating balanced capacitor voltages.

Subsequently, the converter was tested under full PWM operation and successfully reached 9 kV DC link voltage. However, at 10 kV, the OVP unexpectedly triggered. The flying capacitor voltages remained below the threshold, and neither the DC link voltage nor the AC output voltage displayed any abnormalities on the oscilloscope. Upon further analysis of voltage signals D0 to D6, we discovered a momentary disruption in all signals before the protection activated as shown in **Figure 6.16**.

The issue was likely caused by common-mode (CM) current from the power stage flowing through the controller ground, leading to interference. To mitigate this: 1) A large CM choke was added at the controller power input. 2) The controller was powered using a UPS to isolate it from supply fluctuations. 3) Shielding was added to the ribbon cable measuring voltage signals to reduce noise coupling.

Despite these efforts, the problem persisted. Eventually, we moved the controller 4 meters away from the converter and shielded the controller cabinet to prevent interference from radiated EMI as presented in **Figure 6.17**. This modification successfully eliminated the issue, allowing the converter to operate beyond 10 kV without premature protection triggering.

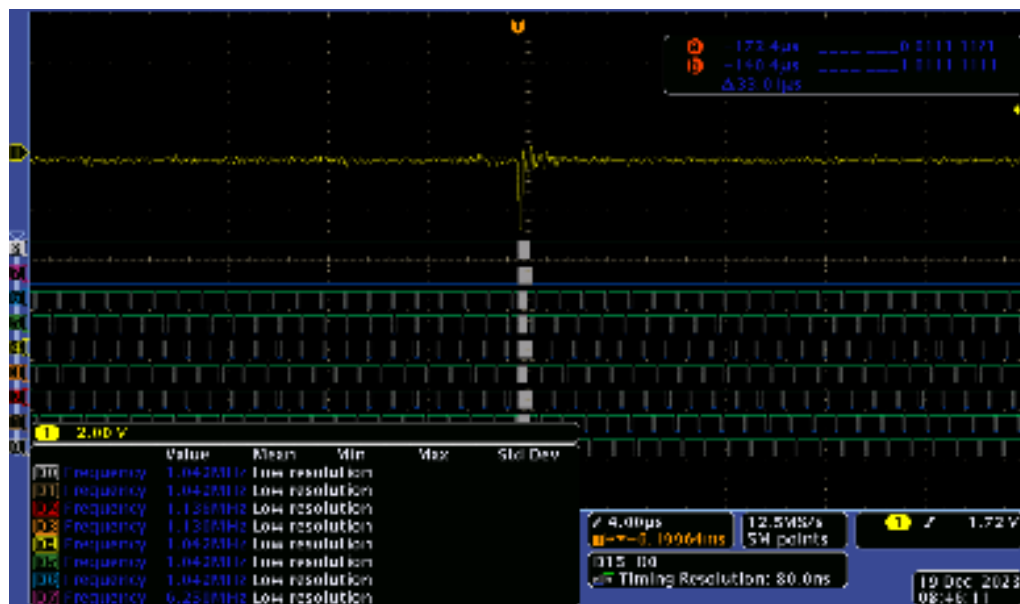


Figure 6.16. Voltage sensor signals 1-7 D0-D6 are interrupted.



Figure 6.17. The controller moved away from the converter cabinet.

6.5.3 Multiple pulse test

Following the insulation test and verification of the OVP, the gate signals and feedback signals of all gate drivers are monitored to verify correct dead time, phase shift, and to ensure there are no shoot-through or noise coupling issues. During continuous testing, it was observed that several power modules experienced failures at drain-source voltages below 3 kV. This suggests that these power modules degrade rapidly during continuous operation. To address this, a shorter multiple pulse test is adopted, where the converter first soft startup for 20 cycles and operates in full rating for 20 cycles, then dc power source turns off, ensuring the system's robustness and reliability. Successful operation demonstrated up to 20 kV in **Figure 6.18** validates the effectiveness of the testing procedures and the overall design of the converter.

6.6 Summary

In this chapter, we focus on the design and testing of an 8-level FCC, covering key aspects such as capacitor selection, busbar design, and output filter inductor to meet power density and

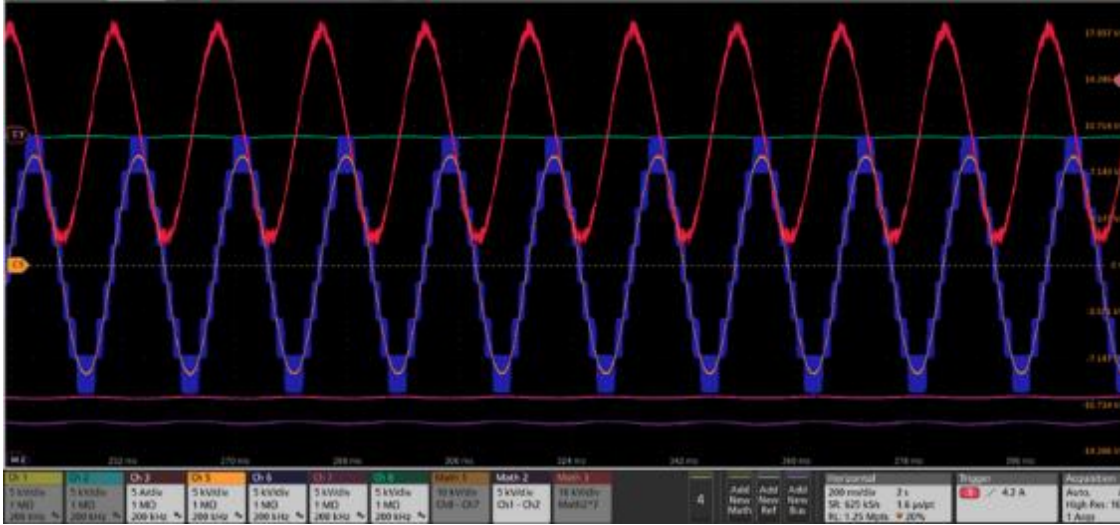


Figure 6.18. 8-level FCC test waveforms at 20 kV, from top to bottom: output current (5A/div), DC+ voltage (5kV/div), output PWM voltage (5kV/div), output voltage (5kV/div), DC- voltage (5kV/div), lowest stage flying capacitor voltage (5kV/div).

TRD requirements.

- **Capacitor Configuration Optimization:** Investigated series-connected capacitor arrangements, balancing reduced effective capacitance and increased voltage ripple through a trade-off between voltage stability and operating range.
- **High-Voltage Insulation and Layout Strategies:** Tackled insulation design challenges at high power density by optimizing spacing and minimizing parasitic coupling between primary and secondary components to suppress false triggering from dv/dt and di/dt transients.
- **Component-Level Testing:** Conducted screening of power modules (on-state resistance, transconductance), current sensors (zero-crossing calibration), and voltage sensors (linearity and accuracy) to ensure uniformity and reliability.
- **High-Voltage System Testing:** Validated converter performance through static insulation tests, PWM gate signal checks, voltage balancing across flying capacitors, and a multi-pulse testing at 20 kV to reduce power module stress and enhance reliability.

Chapter 7 New Module Flying Capacitor Converter Testing

During 8-level FCC testing described in chapter 6, approximately six Wolfspeed modules were damaged. Wolfspeed module insulation deteriorates rapidly and cannot withstand the voltage level at less than 4 kV (even though they used 10 kV SiC MOSFET dies). To achieve full voltage rating at 24 kV, a new FCC phase leg is built based on modules packaged by Powerex. All the modules successfully passed PD test at 10 kV and DPT test at 6 kV; thus, the FCC is reduced to 5 level. The DC link and load configuration are consistent with those of the 8-level FCC. The flying capacitor selection is based on the same criteria discussed in the last chapter. The voltage sensor adjustment involved modifying the voltage divider according to the operational voltage, while the current sensor remains unchanged. The primary differences involve the power module and the decoupling capacitor, which are discussed in detail in the following sections.

7.1 Power Module Comparison

The Powerex modules also used Wolfspeed's 3rd-generation 10 kV, 20 A dies, with six dies in parallel per switch. However, Powerex's design introduced several key improvements:

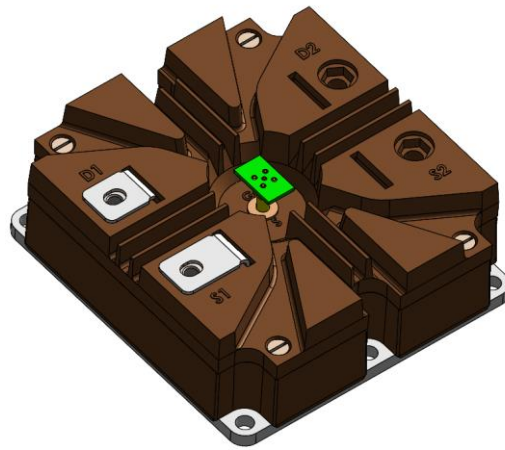
Each module contains only a single switch instead of a full bridge, effectively halving the voltage stress on the DBC substrate and potting materials. A double-layer DBC is implemented between the drain and baseplate, further reducing voltage stress compared to the single-layer DBC in the Wolfspeed module.

Dies with similar threshold voltage are grouped together in one power module. The Powerex module features a dedicated gate PCB, ensuring uniform gate-to-die inductance with only 3.7% variance. In contrast, Wolfspeed's module connects all dies to a single ring-shaped DBC, causing the dies farther from the gate to experience higher gate loop inductance. The internal gate resistance is higher in the Powerex module, with each die having a 5 Ω gate resistance, compared to 2 Ω in the Wolfspeed module. Due to a non-disclosure agreement, the internal structure of the power modules cannot be disclosed. However, the outer appearances of the modules are shown below in **Figure 7.1**.

Static characteristics are examined for the new module to investigate any differences in saturation current, on-state resistance, and junction capacitance that impact conduction and switching loss.



(a) Wolfspeed module: 2 switches in a half bridge, size (150x75x25) mm



(b) Powerex module: 1 switch, size (130x140x48) mm

Figure 7.1. Wolfspeed module vs Powerex module.

7.1.1 Static Characterization Comparison

Forward conduction test examined the Powerex module's drain-source voltage and current with gate voltage ranging from 5 V to 15 V. **Figure 7.2** shows the test waveforms. At $V_{gs}=15V$, the current reaches 100 A with a 5 V drop, slightly higher than Wolfspeed's 92 A in **Figure 7.3**. At $V_{gs}=8V$, Powerex's saturation current is 55 A versus Wolfspeed's 35 A. Although both modules are based on 3rd-generation dies, their saturation currents differ, and the underlying reason has not been specified by the manufacturer. Still, the on-state resistances are similar at 50 A, 15V gate resistance because of comparable voltage drop, which indicates similar conduction loss.

7.1.2 Junction Capacitance Comparison

Junction capacitance impact switching speed and loss. The drain-source capacitance C_{ds} is influenced by the permittivity of the semiconductor material, doping concentration, depletion width, and junction area. The gate-drain capacitance C_{gd} is determined by the overlap and fringing capacitances between the gate and drain terminals and is further amplified by the Miller effect during switching transitions. As a result, both C_{ds} and C_{gd} are highly nonlinear and strongly dependent on the drain-source voltage.

Meanwhile, the gate-source capacitance C_{gs} is primarily determined by the gate oxide capacitance and channel depletion capacitance. To accurately characterize C_{gs} , measurements are performed at a low drain-source voltage (300 V), as C_{gs} is governed by the gate-source voltage and remains largely unaffected by the drain-source voltage.

The gate-source capacitance is measured at lower drain source voltage at 300 V because it is not affected by drain source voltage but rather gate source voltage. Since both Powerex and Wolfspeed modules utilize the same dies, their capacitance values are mostly similar as shown in **Table 7-1**. These discrepancies can be attributed to variations in packaging layout, such as bond wire length and internal parasitics, rather than to differences in the semiconductor die itself.

Further comparisons of the capacitance characteristics across a broader voltage range are presented in **Figure 7.4**, **Figure 7.5**, and **Figure 7.6**. which consistently demonstrate that remains stable and closely matched between the two modules under various voltage range.

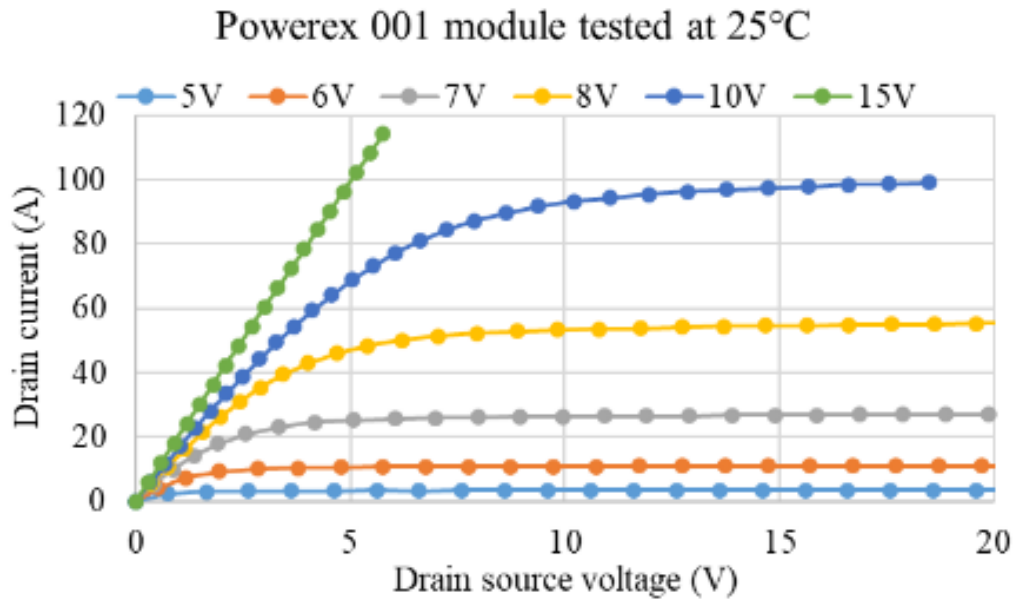


Figure 7.2. Powerex module $I_d - V_{ds}$ curve at 25°C.

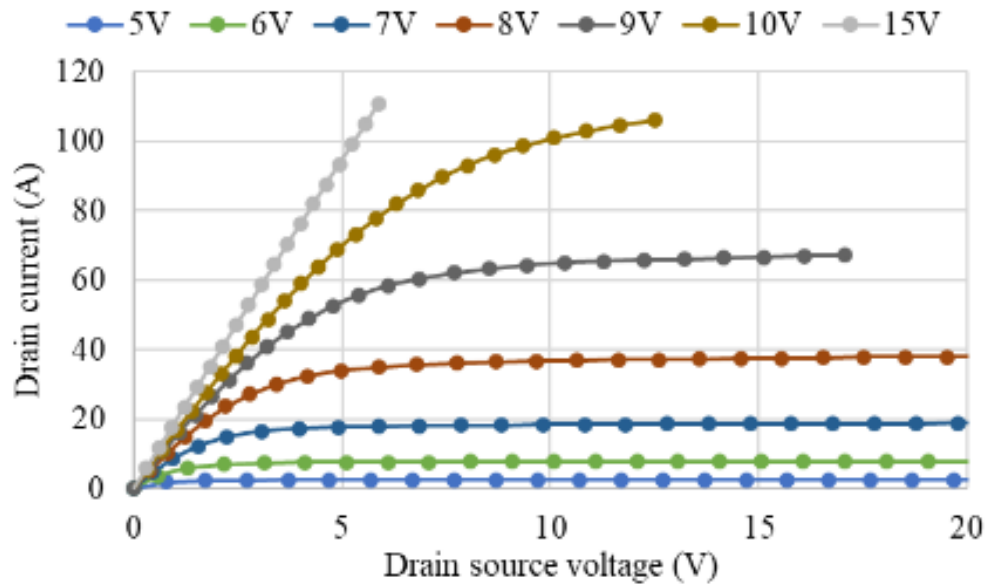


Figure 7.3. Wolfspeed module $I_d - V_{ds}$ curve at 25°C.

Table 7-1. Comparison of capacitance between different modules.

	C_{ds} at 3 kV V_{ds}	C_{gd} at 3 kV V_{ds}	C_{gs}
Powerex module	35.2 nF	97.8 nF	44 nF
Wolfspeed module	30.7 nF	105 nF	41 nF

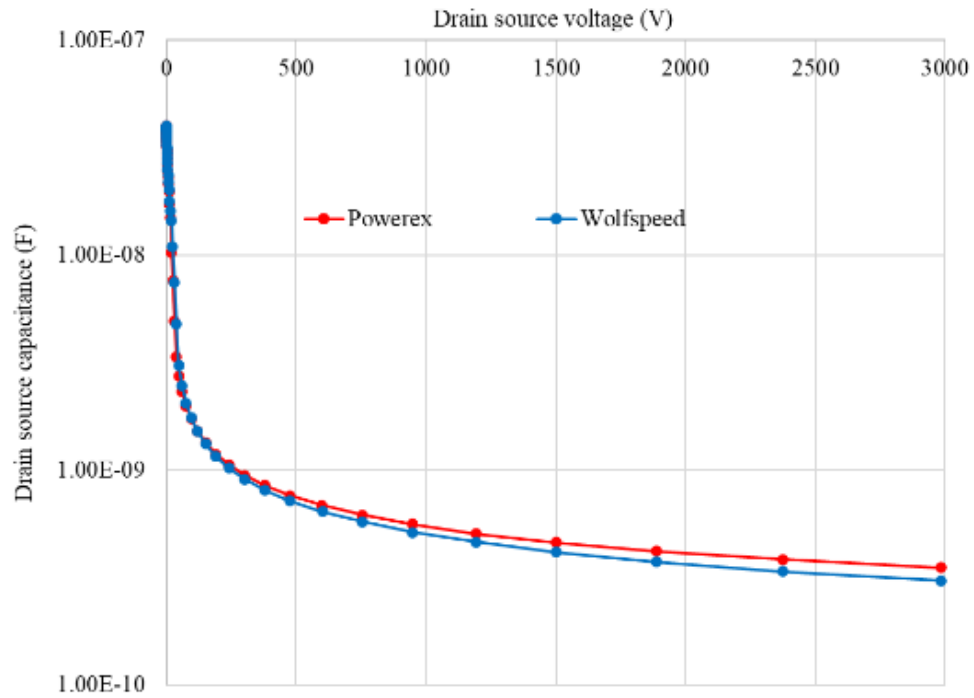


Figure 7.4. Output capacitance comparison between Powerex and Wolfspeed SiC modules.

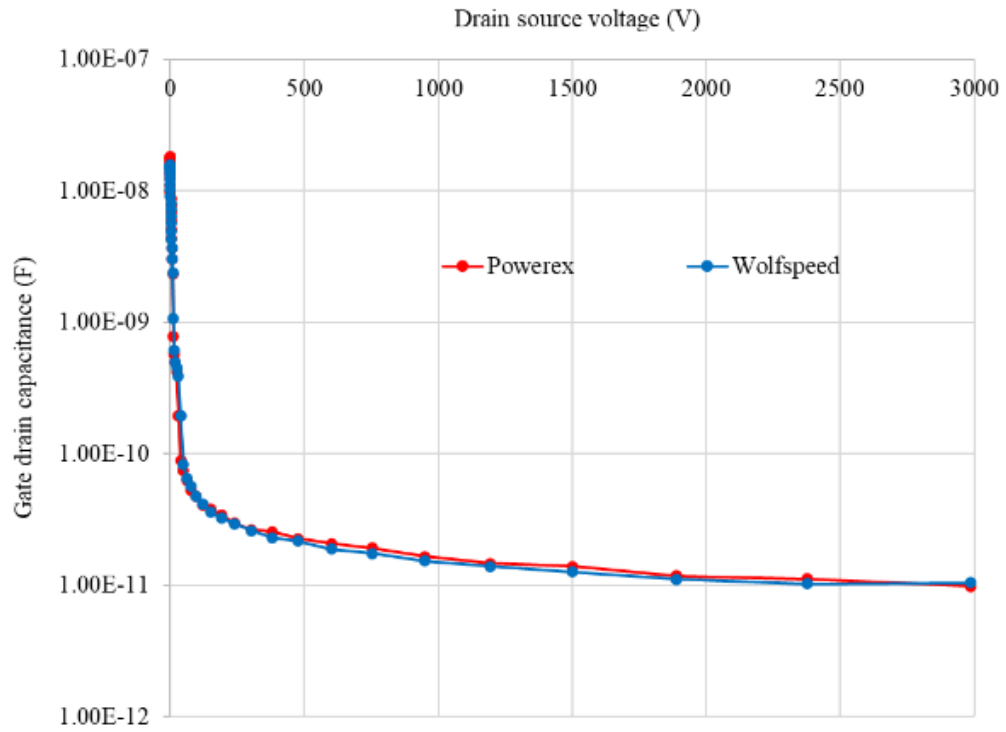


Figure 7.5. Gate-drain capacitance comparison between Powerex and Wolfspeed SiC modules.

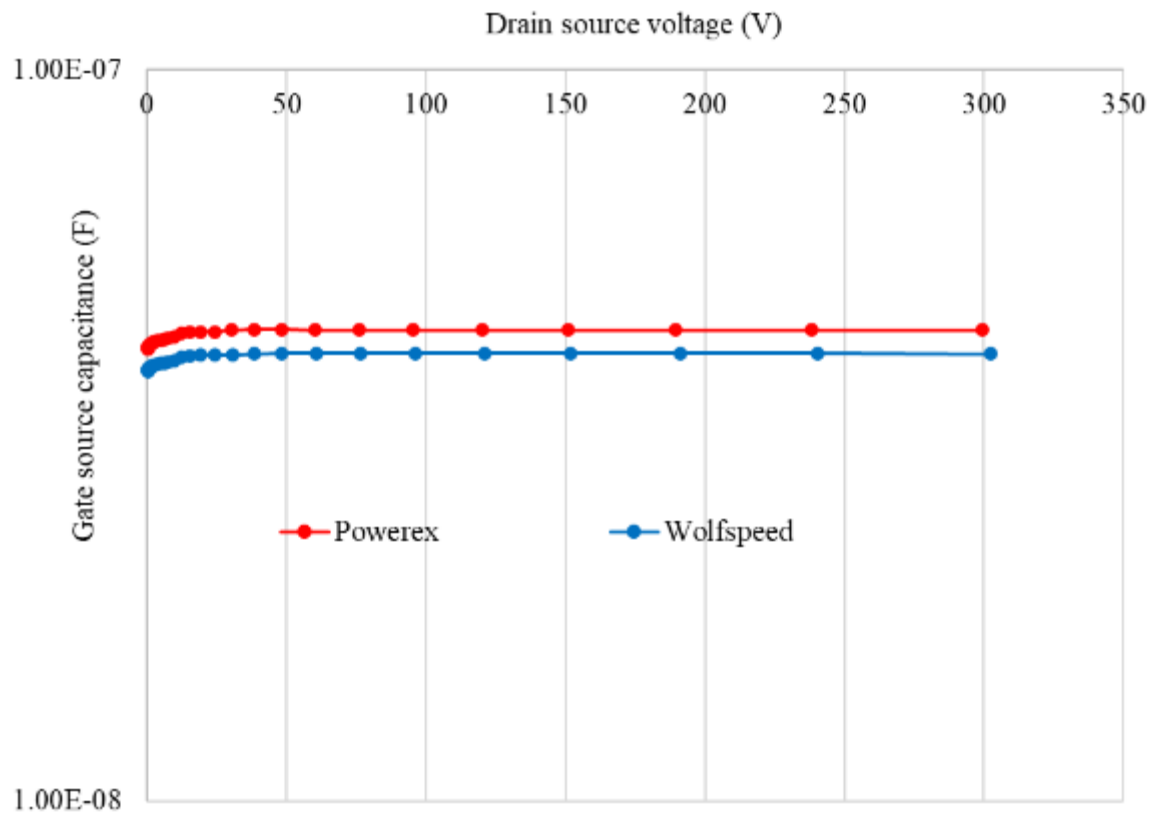


Figure 7.6. Gate-source capacitance comparison between Powerex and Wolfspeed SiC modules.

7.1.3 Switching Loss Comparison

The switching loss is separated into turn on loss E_{on} and turn off loss E_{off} . The turn on loss is calculated from the integral of V_{ds} and I_d over current rise time and voltage fall time. While the turn off loss is calculated from the integral of V_{ds} and I_d over voltage rise time and current fall time. The switching loss of Powerex module and Wolfspeed module tested at 2.5 Ω external gate resistance are presented in **Table 7-2.** and **Table 7-3.** respectively.

At comparable voltage and current conditions, such as 6.1 kV and 50 A, the switching loss of the Powerex module is 52.82 mJ, while that of the Wolfspeed module is 49.88 mJ. The slightly higher switching loss of 2.94 mJ in the Powerex module can be attributed to its larger internal gate resistance of 0.83 Ω per switch, compared to 0.33 Ω in the Wolfspeed module.

Additionally, the baseplate capacitance of the Powerex module is 118 pF, resulting in a capacitance-related loss of 2.20 mJ, whereas the Wolfspeed module, with a baseplate capacitance of 55 pF, exhibits a corresponding loss of 1.07 mJ. This difference further contributes to the observed variation in switching loss.

Furthermore, the larger power loop inductance in the Powerex module reduces the switching speed, thereby increasing the switching loss. Overall, the switching losses of the two modules are relatively similar.

7.2 Decoupling Capacitor Comparison

To manage high voltage, multiple flying capacitors are connected in series, which inevitably increases loop inductance and results in significant voltage overshoot during switching transients. To mitigate voltage stress on the device, a decoupling capacitor is incorporated to supply transient current.

In the 8-level FCC system, five 6 kV polypropylene (PP) film capacitors were utilized in series on one side of the PCB for 24 kV operation, and four capacitors on the opposite side for 21.2 kV operation. This configuration effectively reduced voltage overshoot, despite the large size of these decoupling capacitors. In the 5-level FCC system, each stage operates at 6 kV, compared to 3.4 kV in the 8-level FCC system at full 24 kV DC link voltage. This results in a higher di/dt, leading to greater voltage overshoot. To mitigate the resulting voltage stress on the power modules, a decoupling capacitor with lower equivalent series inductance (ESL) is selected to reduce the total inductance in the commutation loop. Accordingly, the high-voltage ceramic

Table 7-2. Powerex module switching loss at 25°C.

Vdc (kV)	IL (A)	Eon (mJ)	Eoff (mJ)	Ettotal (mJ)
6.1	13	21.74	10.85	32.59
6.1	31.7	30.56	11.85	42.41
6.1	50	39.62	13.2	52.82

Table 7-3. Wolfspeed module switching loss at 25°C

Vdc (kV)	IL (A)	Eon (mJ)	Eoff (mJ)	Ettotal (mJ)
6.04	17	24.66	7.11	31.77
6.04	40	35.77	7.48	43.25
6.06	50	41.85	8.03	49.88

capacitor TDK B58035U9754M062, which offers a more compact solution, is employed for the 5-level FCC.

A detailed comparison between decoupling capacitors is presented in **Table 7-4**, highlighting the advantages of using high-voltage ceramic capacitors. However, given its effective capacitance of only 0.39 μF at 900 V, two capacitors were paralleled and 30 of them were put in series to support 24 kV operation. This arrangement ensured stable performance and minimal voltage overshoot.

During a hipot test conducted at 20 kV, air discharge was observed from the metal frames of the ceramic capacitors—an issue that did not occur with the larger PP capacitors. This is threatening as it could potentially lead to component failure and corona discharge. To eliminate this problem, we designed an enclosure to house the capacitors on both sides of the PCB.

The complete assembly underwent encapsulation using Wacker 613 silicone gel, as illustrated in **Figure 7.7**. This specially formulated two-component gel was selected for its exceptional dielectric properties (20 kV/mm breakdown strength) and low viscosity (150 mPa·s before curing), which enabled complete penetration of allspaces. The encapsulation process involved:

- Pre-treatment with isopropyl alcohol to ensure surface cleanliness
- Vacuum degassing at 0.1 bar for 60 minutes to eliminate air pockets
- Controlled curing at 25°C for 24 hours to achieve optimal mechanical properties

After vacuum pressure potting, the flying capacitor assembly successfully passed the hipot test, demonstrating the effectiveness of our solution.

Current ratings were also evaluated. With a maximum pulse current of 0.73 A and an RMS current of 0.26 A at 5 kHz, both types of capacitors satisfy the application requirements.

The 5-level FCC phase leg, illustrated in **Figure 7.8**, is significantly more compact than the 8-level FCC depicted in Chapter 6. This design includes only eight power modules, thereby reducing the number of gate drivers and APS required. Four stages of flying capacitors, decoupling capacitors, and voltage sensors are centrally positioned, similar to the 8-level layout. The reduced component count leads to easier maintenance and higher reliability due to fewer points of failure.

Table 7-4 Comparison of decoupling capacitors in 8-level and 5-level FCC systems.

Converter	8-level FCC	5-level FCC
Part number	WIMA FKP1Y031007J00KSSD	TDK B58035U9754M062
Material	Polypropylene (PP)	Ceramic
Capacitance	0.1uF 10%	0.75uF 20%
Voltage	6 kV	900 V
Current	3 A at 5 kHz	4.5 A at 5 kHz
Capacitors in series for 24 kV	5	30
Overall size	25cmx4cmx10cm	25cmx4cmx5cm
Single capacitor ESL	30 nH	3 nH
Total ESL	150 nH	45 nH

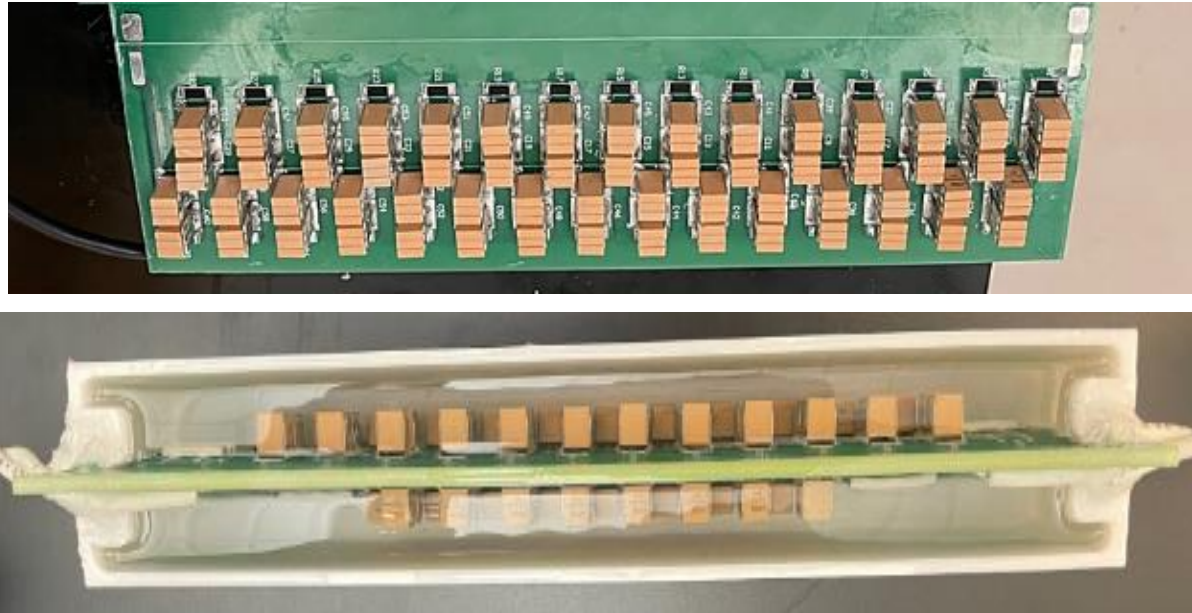


Figure 7.7. 5-level FCC decoupling capacitor before potting and after potting.

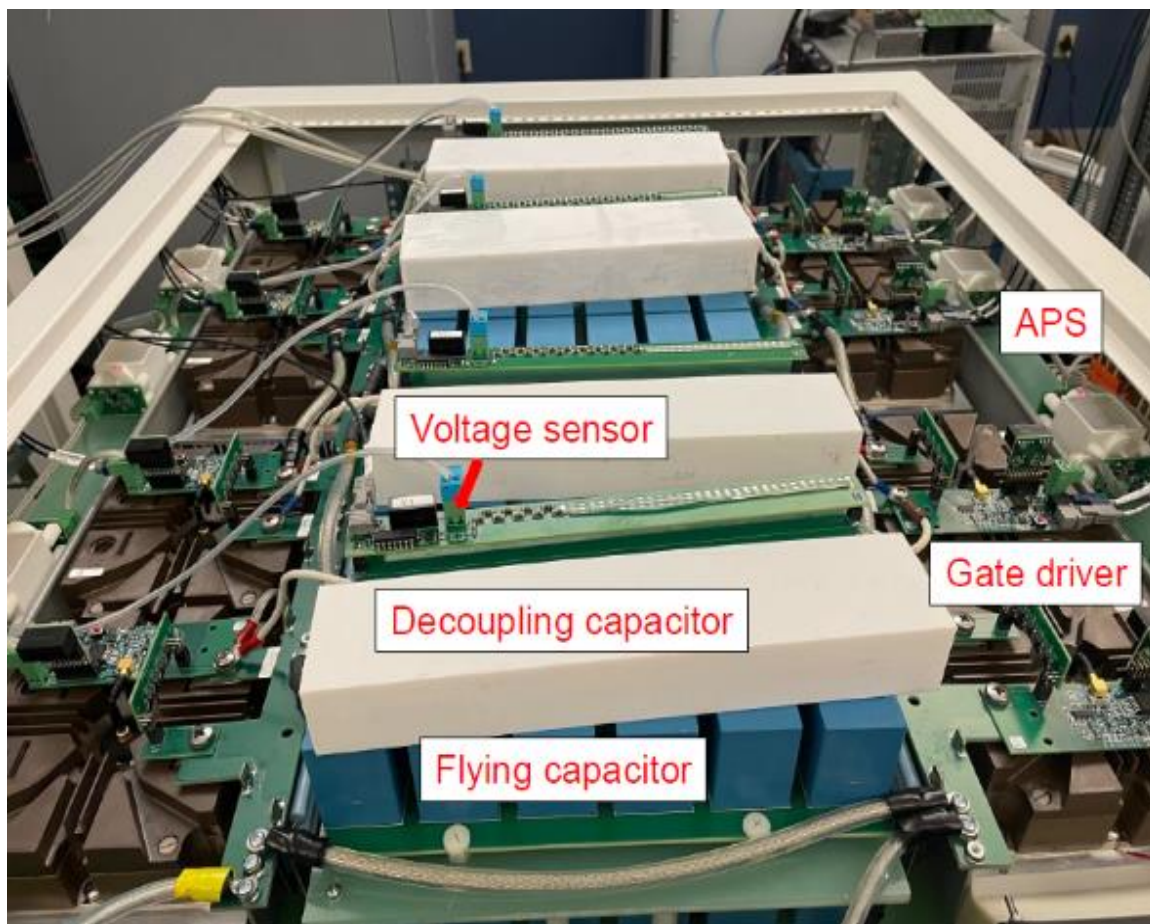


Figure 7.8. 5-level FCC phase leg for 1 MW converter (24 kV dc link, 13.8 kV line-line ac).

Figure 7.9 illustrates the complete experimental setup. On the left side, the phase leg input is connected to the DC link capacitor, while on the right side, the output is linked to the RC loads. Positioned centrally within the setup, the oscilloscope is placed at a distance of 0.5 m from the high-voltage power stage to minimize interference. The controller is located in the far back corner, isolated from the main power components to reduce noise interference.

7.3 Device overvoltage protection

The device overvoltage protection (OVP) calculates the voltage difference between adjacent stages from flying capacitor voltage sensor measurements. To evaluate the performance, feedback signals from four stages of flying capacitor voltage were continuously monitored by an oscilloscope.

However, during testing, an unexpected issue arose: the OVP was triggered prematurely at a DC voltage of 12 kV, despite the threshold set at 16 kV. As illustrated in **Figure 7.10**, all feedback signals experienced significant interference, which led to incorrect triggering of the OVP.

In addition to the compromised feedback signals, the gate signals for the first-stage power modules, D4 and D5, were also affected. This indicates a broader issue, possibly stemming from EMI, ground loops, or noise coupling between different system components. The disruption of gate signals can have severe consequences of improper switching behavior and even device failure. Given these observations, a thorough investigation is necessary to identify the root cause of the interference and premature OVP activation.

Despite the measures implemented in chapter 6 to enhance the shielding of the controller cabinet in 8-level flying capacitor converter (FCC), these issues persisted in the 5-level FCC. This is likely due to higher dv/dt values since each device operates at 3 kV when the DC link voltage is 12 kV in 5-level FCC, compared to 1.5 kV in 8-level FCC.

7.3.1 Voltage sensor

To improve the accuracy of the flying capacitor (FC) voltage sensors, several modifications were implemented in the sensor design.

One of the key adjustments is to increase the RC filter capacitor. Initially, the capacitance was increased from 47 pF to 680 pF, and later further increased to 2.2 nF to improve noise filtering. Additionally, the impedance of the voltage sensor divider for the first stage was reduced from 10M Ω /10k Ω to 5M Ω /5k Ω in an effort to mitigate voltage spikes induced by CM current.

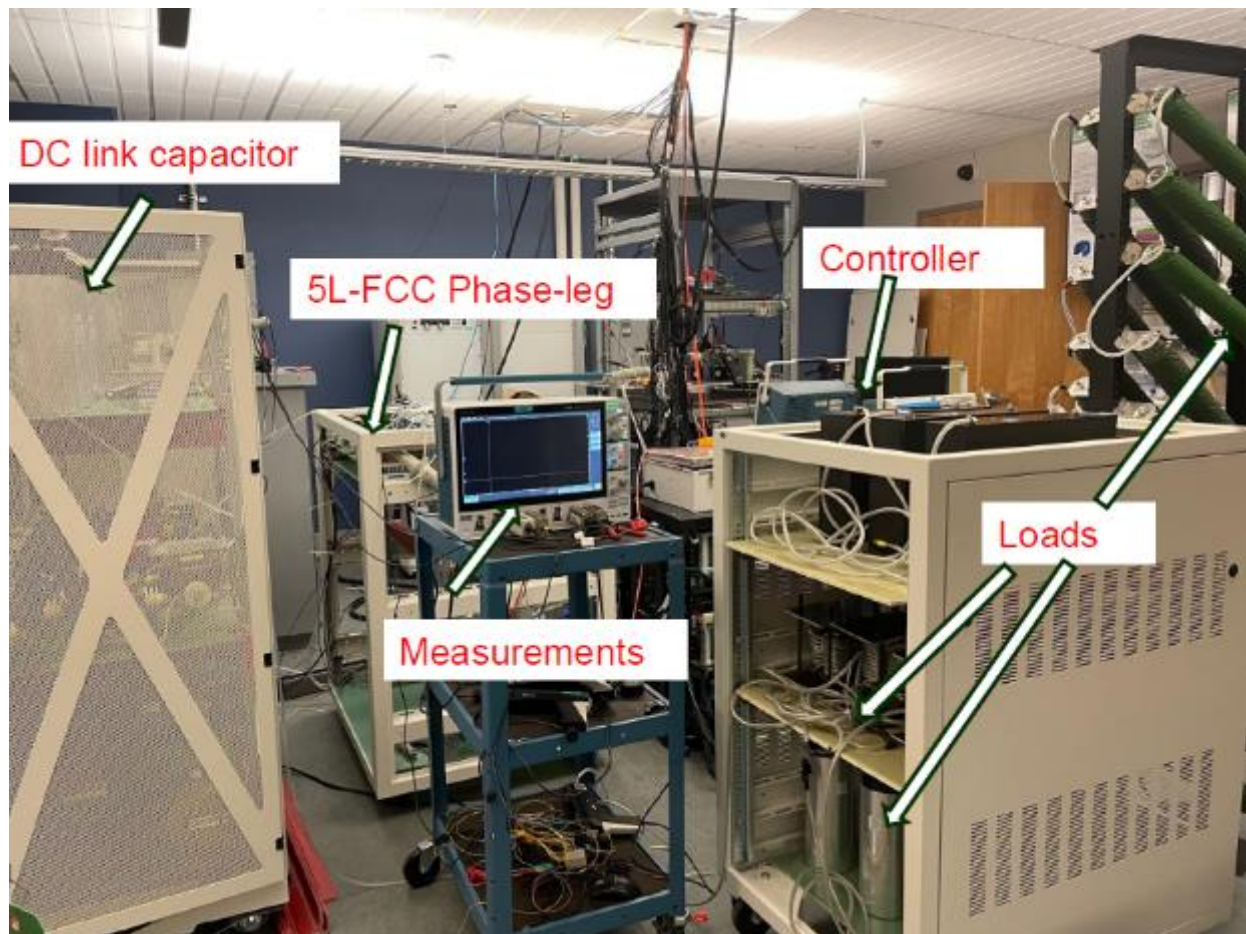


Figure 7.9. 5-level FCC test setup.



Figure 7.10. Voltage sensor feedback signal D0-D3 all interrupted.

However, it introduced an unintended consequence: the reduced impedance slowed down the voltage balancing process during start up. This occurred because the impedance of the voltage sensor divider became comparable to that of the precharge resistors, thereby interfering with the expected voltage distribution. To resolve this issue, the impedance values of the voltage sensor divider were ultimately reverted to their original configuration (10M Ω /10k Ω).

Beyond component-level modifications, multiple adjustments were made to the physical placement of the voltage sensor to minimize noise interference. Initially, the sensor was relocated from the decoupling capacitor board to the top of the FC capacitor to reduce the impact of a nearby dv/dt node, which was suspected of introducing unwanted interference. However, noise-related issues persisted. Further analysis indicated that the large pulse current flowing through the FC capacitor was likely contributing to the problem. Consequently, the sensor was repositioned once again—this time, back to the top of the decoupling capacitor board but placed to maintain a safe distance from both the dv/dt nodes and the di/dt effects of the FC capacitor. This final adjustment led to a significant reduction in noise, improving measurement accuracy.

To further enhance shielding and minimize EMI, additional precautions were taken. Specifically, the controller cabinet door was fully closed to ensure proper enclosure shielding, preventing external noise from affecting the sensitive control circuitry. With these combined improvements, the system demonstrated substantial stability, allowing the converter to be successfully tested up to a DC link voltage of 14 kV without inadvertently triggering OVP.

7.3.2 Device drain source voltage

The OVP of the 4th stage device was falsely triggered when the DC voltage ranged from 16 kV to 18 kV. To verify if this was a genuine overvoltage issue, we employed a differential probe to measure the drain-source voltage of the device at the 4th stage. Initially, the device's drain-source voltage is governed by the precharge resistors, with the upper and lower devices at the same stage each bearing half of the operating voltage at 1.5 kV. Upon activation of the gate signal, the drain-source voltage transitions to the full operating voltage as the load current circulates through the device, charging and discharging the flying capacitors. As indicated in the measurements, the maximum voltage is 3.28 kV, no overvoltage beyond the threshold 3.9 kV (130% of rated voltage) was detected at 12 kV dc link voltage as shown in **Figure 7.11**.

7.3.3 Flying capacitor voltage

To investigate whether the flying capacitor (FC) voltage ripple was responsible for triggering the OVP mechanism, measurements of the FC voltage at the third stage were obtained. The fourth stage was excluded from the measurements, as it remains stable in parallel with the DC link voltage and is therefore unlikely to contribute to the issue.

As illustrated in **Figure 7.12**, the measured FC voltage ripple at the third stage was 160 V. This ripple consists of both a low-frequency 60 Hz component and a high-frequency component from device switching events. Given that the operating voltage at this stage is 7.5 kV, the observed ripple accounts for 2% of the total voltage. Since the OVP threshold is set at 130% of the nominal voltage, it is unlikely that this level of ripple could have triggered a genuine overvoltage event. Suspecting that EMI may have disrupted the sensing or control signals, the gate signals of the power devices were analyzed.

7.3.4 Gate signal spikes

During the investigation, random voltage spikes were observed in the gate signals, as shown in **Figure 7.13**. Given that the controller already incorporates a minimum PWM signal bypass

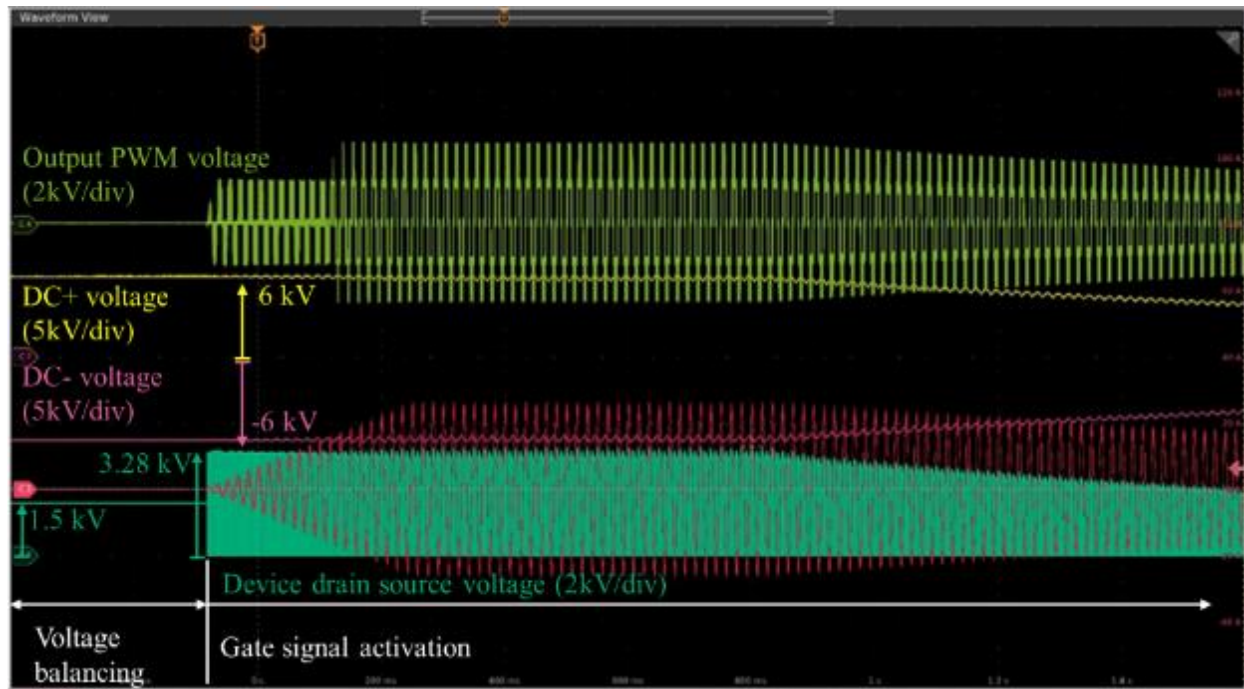


Figure 7.11. Waveforms in a 5-level FCC at 12 kV dc link voltage illustrating the transition from voltage balancing stage to gate signal activation.



Figure 7.12. 3rd stage flying capacitor voltage ripple at 10 kV dc link voltage.

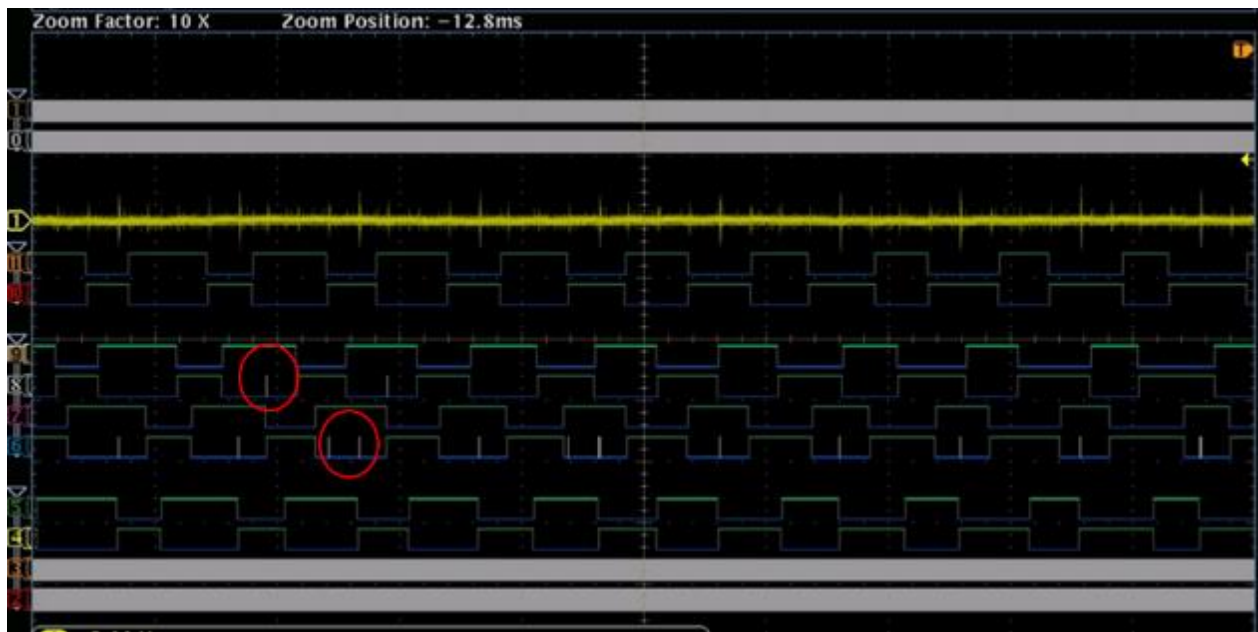


Figure 7.13. Gate PWM signal spikes at 20 kV dc voltage.

function to filter out unintended transients, these voltage spikes are likely attributable to noise rather than actual switching anomalies.

Considering the potential impact of EMI on signal integrity, multiple mitigation strategies were explored, and the corresponding observations were documented. As a first step, the converter's sidewalls were grounded. Subsequently, the APS input ground was connected to the cabinet ground to shorten the CM current path. By providing a more direct route for these currents, noise circulating within the system was minimized.

The same uninterruptible power supply (UPS) was then used for both the oscilloscope and the controller to ensure operation under identical electrical conditions, thereby reducing the likelihood of induced noise. Additionally, the controller was relocated farther from the converter to mitigate inductive and capacitive coupling effects between the converter and the controller.

Through the implementation of these methods, the noise issue was effectively mitigated. As shown in **Figure 7.14**, the gate signals became much cleaner, exhibiting no observable spikes, thus validating the effectiveness of the mitigation strategies. The DC-link voltage was subsequently increased to 22 kV without encountering premature OVP activation or gate signal anomalies

At DC voltages exceeding 22 kV, OVP for the third-stage device was unexpectedly triggered. Further investigation revealed that the second-stage voltage sensor output was severely disrupted, remaining constantly high. This indicated signal corruption caused by EMI. To address this problem, the sensor's RC filter capacitance was increased from 2.2 nF to 4.7 nF to improve noise filtering. However, this adjustment did not resolve the issue.

As shown in **Figure 7.15**, shielding is achieved by wrapping copper foil around the voltage sensor power supply and ICs, which is then grounded to the voltage sensor ground. This proved highly effective in mitigating interference, stabilizing the sensor's output, and preventing false OVP activation.

Following the resolution of the interference problem, the converter was operated at its full DC link voltage of 24 kV. Under these conditions, the system reached a maximum AC load current of 50 A, a peak AC voltage of 10.86 kV, and delivered a total apparent power of 271.5 kVA, as shown in **Figure 7.16**. Under these conditions, the output staircase voltage demonstrated voltage balancing across all four stages of flying capacitors. Furthermore, the output current displayed a sinusoidal waveform, with minimal distortion, which validates the



Figure 7.14. Gate PWM signals are clean at 22 kV after measures implemented.

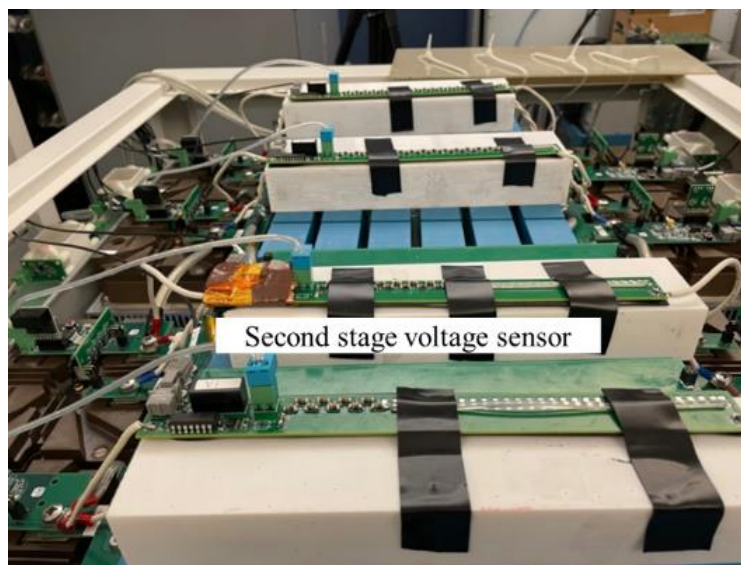


Figure 7.15. 2nd stage voltage sensor is shielded.

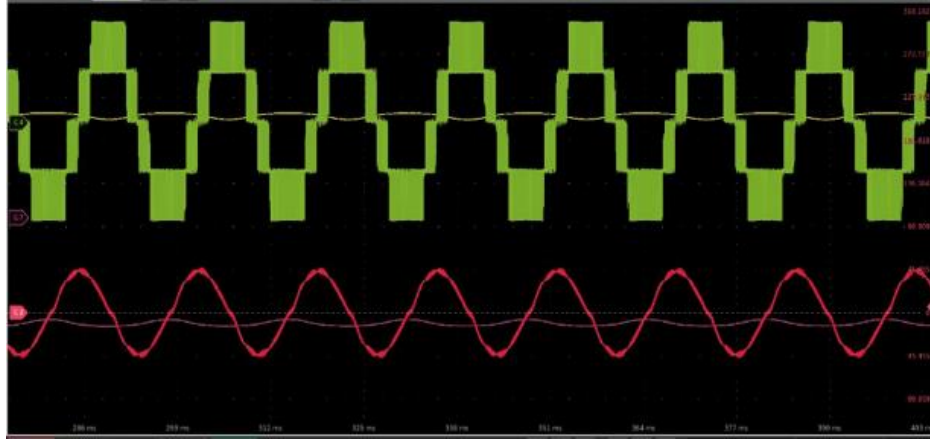


Figure 7.16. Waveforms at 24 kV dc link voltage from top to bottom: output PWM voltage (5kV/div), DC+ voltage (5kV/div), DC- voltage (5kV/div), output current (50A/div).

inductor design. These results demonstrate the effectiveness of the converter design in terms of component selection, switching loop optimization, insulation design and EMI resilience

7.4 Summary

This chapter discussed significant advances in the development of a new power module and its implementation in a 5-level 1 MW FCC converter.

- At the converter level, a new small-profile ceramic decoupling capacitor was introduced to reduce both the physical size and loop inductance.
- Investigated the cause of OVP mis-triggering by measuring the device drain source voltage and flying capacitor ripple voltage, which are within protection limit. Resolved OVP mis-triggering caused by EMI via sensor repositioning, shielding and increased input filter capacitance. Eliminated gate signal spikes caused by EMI via shielding and separating the power and control cabinets.
- Validated insulation and system operation through full converter testing at DC voltage 24 kV, AC maximum current 50 A.

Chapter 8 Conclusions and Future Work

8.1 Summary

In the preceding chapters, the application of 10 kV SiC MOSFETs in a 13.8 kV multilevel converter was investigated, with particular focus on insulation design, EMI resilience, thermal management, and comprehensive converter-level testing.

Chapter 3 explores the influence of magnetic core geometry on the reduction of interwinding capacitance, providing practical design guidelines aimed at mitigating interference induced by CM currents. A series LLC-based APS is designed with optimized insulation to enhance high-voltage isolation performance. The impact of output fault conditions is examined by analyzing voltage deviation when one of the four APS outputs fails, and corresponding protection strategies are evaluated for both the primary and secondary sides. For the flybuck APS topology, startup instability and erroneous shutdowns encountered during converter operation are also addressed.

Chapter 4 presents the thermal characterization of a 10 kV SiC power module across a range of operating temperatures. TSEPs are extracted from turn-on transients and conduction phases. It is observed that turn-off characteristics are largely temperature-independent and therefore unsuitable as TSEPs. The influence of gate resistance, load current, and parasitic elements on the accuracy of TSEP measurements is analyzed to enable reliable calibration under different test conditions. Based on the identified TSEPs, an over-temperature protection circuit is proposed, utilizing turn-on di/dt as the sensing parameter.

Chapter 5 addresses the thermal management strategies of the converter. For liquid cooling, factors such as coolant type, flow rate, thermal performance, and cold plate connection are considered. For air cooling, attention is given to maintaining adequate clearance and creepage distances to prevent electrical breakdown, and several air duct configurations are evaluated to ensure uniform airflow distribution. Both cooling approaches are validated through continuous power testing of an individual power module.

Chapter 6 details the design and integration of the power stage, including key passive components, sensors, and the mechanical layout of the FCC converter. In addition, the chapter outlines the converter testing procedures with respect to insulation integrity, protection mechanisms, and full-power operational validation.

Chapter 7 focuses on troubleshooting and resolving the OVP mis-triggering issue. Through a combination of sensor repositioning, improved shielding, and increased input filter capacitance,

the false triggering was effectively eliminated. Furthermore, gate signal disturbances were mitigated through enhanced shielding of both the power converter and the control cabinet. As a result, the converter achieved its full-rated performance of 24 kV and 50 A.

8.2 Contributions

This dissertation presents several original contributions to the field of MV power converter design, specifically in the areas of APS protection, TSEP selection, thermal management, testing procedure, and decoupling capacitor selection of MV systems. The key contributions are summarized as follows:

- Development of a series LLC-based APS with integrated secondary-side protection capable of isolating both output open-circuit and short-circuit faults. This design enhances the robustness and reliability of the power supply under fault conditions.
- Extraction and evaluation of TSEPs from a 10 kV SiC MOSFET power module, including a detailed analysis of temperature sensitivity, linearity, and the influence of gate resistance, load current, and parasitic parameters. This contributes to more accurate device monitoring and thermal diagnostics.
- Design and implementation of an over-temperature protection circuit that operates without the need for a microcontroller, relying instead on preset undervoltage threshold. This approach simplifies the hardware while maintaining effective thermal protection.
- Developed a comprehensive testing procedure encompassing component-level validation, static voltage testing of the converter, protection function verification, and full power testing
- Implemented high-voltage multilayer ceramic capacitors (MLCCs) in place of traditional film capacitors, effectively reducing the converter's size and loop inductance. The insulation performance was further enhanced by encapsulating the decoupling capacitors with silicone gel.
- Development of a fully functional FCC converter demonstrating high insulation performance and EMI resilience under challenging operation conditions of 24 kV dc voltage and 100 V/ns dv/dt. The converter design integrates optimized insulation structures, effective shielding, and robust testing to meet high-voltage operational requirements.

8.3 Future Work

Several potential directions for future research emerge from the findings of this dissertation:

- **Integration with Isolated Gate Driver ICs:** In the current design, a non-isolated gate driver IC is employed, requiring the APS to withstand the full insulation voltage. By integrating the APS with an isolated gate driver IC, the insulation requirement on the APS can be significantly reduced, enabling a more compact design. Additionally, this integration would increase the design margin for interwinding capacitance, because the total common-mode (CM) loop capacitance would be reduced due to the series connection with the gate driver's isolation capacitance.
- **Monolithic Integration of APS and Gate Driver:** With continued advancements in power electronics packaging technologies, future designs could integrate the APS and gate driver into a single package. This would not only reduce the overall component count but also improve system reliability and simplify mechanical integration.
- **CM Propagation in Multilevel Converters:** In multilevel converter architectures where multiple APS units share a common input power source, the CM current propagation paths become more complex. A detailed analysis of CM noise propagation under such conditions would help in understanding its impact on secondary-side circuits including gate drivers, APS units, and signal sensors.
- **TSEP Behavior in Multi-Die Power Modules:** In this work, TSEP extraction is performed on a power module with six SiC dies connected in parallel. However, it remains unclear how the number of parallel dies influences the linearity and sensitivity of TSEP behavior. Further investigation is needed to understand the role of thermal coupling between dies and its effect on the reliability and accuracy of TSEP-based temperature monitoring.

References

- [1] “Benefits,” Glenn Research Center | NASA. Accessed: Jul. 04, 2024. [Online]. Available: <https://www1.grc.nasa.gov/research-and-engineering/silicon-carbide-electronics-and-sensors/benefits/>
- [2] L. Zheng et al., “Modular Universal Converter for MVDC Applications,” in 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Sep. 2018, pp. 5544–5551. 0.1109/ECCE.2018.8558291.
- [3] W. Xu, Z. Guo, A. Vetrivelan, R. Yu, and A. Q. Huang, “Hardware Design of a 13.8-kV/3-MVA PV Plus Storage Solid-State Transformer (PVS-SST),” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 4, pp. 3571–3586, Aug. 2022, doi: 10.1109/JESTPE.2021.3082033.
- [4] Z. An, X. Han, V. R. Chowdhury, J. Benzaquen, R. P. Kandula, and D. Divan, “A Tri-Port Current-Source Soft-Switching Medium-Voltage String Inverter for Large-Scale Solar-Plus-Storage Farms,” *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13808–13823, Nov. 2022, doi: 10.1109/TPEL.2022.3185006.
- [5] A. Anurag, S. Acharya, S. Bhattacharya, T. R. Weatherford, and A. A. Parker, “A Gen-3 10-kV SiC MOSFET-Based Medium-Voltage Three-Phase Dual Active Bridge Converter Enabling a Mobile Utility Support Equipment Solid State Transformer,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 2, pp. 1519–1536, Apr. 2022, doi: 10.1109/JESTPE.2021.3069810.
- [6] Z. Chen, H. S. Rizi, W. Xu, R. Yu, and A. Q. Huang, “Hardware Design of a 150kW/1500V All-SiC Grid-forming Photovoltaic Synchronous Generator (PVSG),” in 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2022, pp. 1977–1984. doi: 10.1109/APEC43599.2022.9773550.
- [7] A. Agarwal, A. Anurag, N. Kolli, A. Kumar, and S. Bhattacharya, “Design considerations of 6.5kV enabled three-level and 10kV enabled two-level medium voltage SST,” in 2021 IEEE Energy Conversion Congress and Exposition (ECCE), Oct. 2021, pp. 282–289. doi: 10.1109/ECCE47101.2021.9595367.
- [8] A. Anurag, “HV SiC MOSFET Enabled Solid State Transformers for Mobile Utility Support Equipment based Applications,” p. 262.

- [9] A. Anurag, S. Acharya, N. Kolli, S. Bhattacharya, T. R. Weatherford, and A. A. Parker, "A Three-Phase Active-Front-End Converter System Enabled by 10-kV SiC MOSFETs Aimed at a Solid-State Transformer Application," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5606–5624, May 2022, doi: 10.1109/TPEL.2021.3131262.
- [10] S. Gulur, V. M. Iyer, and S. Bhattacharya, "Passive CM Filter Configuration for a Multi-Stage Grid-Tied Solid State Transformer," *IEEE J. Emerg. Sel. Top. Ind. Electron.*, pp. 1–8, 2023, doi: 10.1109/JESTIE.2023.3268623.
- [11] Y. He, Y. Li, B. Zhou and F. Z. Peng, "Switching-Cycle-Based Startup for Grid-Connected Inverters," in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 5, no. 3, pp. 950-961, July 2024, doi: 10.1109/JESTIE.2024.3365031.
- [12] Y. He, Y. Li, Q. Yang, R. B. Gonzatti, A. Taylor, and F. Peng, "Grid-connected converter without Interfacing Filters: Principle, Analysis and Implementation," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA: IEEE, Oct. 2020, pp. 4505–4511. doi: 10.1109/ECCE44975.2020.9235792.
- [13] L. Zheng et al., "SiC-Based 5-kV Universal Modular Soft-Switching Solid-State Transformer (M-S4T) for Medium-Voltage DC Microgrids and Distribution Grids," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11326–11343, Oct. 2021, doi: 10.1109/TPEL.2021.3066908.
- [14] R. Chen et al., "10 kV SiC MOSFET Based Medium Voltage Power Conditioning System for Asynchronous Microgrids," *IEEE Access*, vol. 10, pp. 73294–73308, 2022, doi: 10.1109/ACCESS.2022.3189003.
- [15] C. Nie et al., "A 13.8 kV, 100 kVA Multi-functional MMC-Based Asynchronous Microgrid Power Conditioning System with 10 kV SiC MOSFETs," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Jun. 2021, pp. 2229–2236. doi: 10.1109/APEC42165.2021.9487381.
- [16] D. Li et al., "Grid Stability Enhancement by a High Voltage SiC MOSFET-Based Asynchronous Microgrid Power Conditioning System," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Jun. 2021, pp. 111–118. doi: 10.1109/APEC42165.2021.9487223.
- [17] D. Li et al., "Paralleling Operation of 10 kV SiC MOSFET-Based Modular Multi-Level Converters (MMCs) for Scalable Asynchronous Microgrid Power Conditioning System,"

- in 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Jun. 2021, pp. 1444–1450. doi: 10.1109/APEC42165.2021.9487255.
- [18] D. Li, S. Ji, X. Huang, J. Palmer, F. Wang, and L. M. Tolbert, “Controller Development of an Asynchronous Microgrid Power Conditioning System (PCS) Converter Considering Grid Requirements,” in 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2020, pp. 616–621. doi: 10.1109/APEC39645.2020.9124437.
- [19] Z. Dong, R. Ren, and F. Wang, “Development of High-Power Bidirectional DC Solid-State Power Controller for Aircraft Applications,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 5, pp. 5498–5508, Oct. 2022, doi: 10.1109/JESTPE.2021.3139903.
- [20] Z. Dong, R. Ren, W. Zhang, F. F. Wang, and L. M. Tolbert, “Instability Issue of Paralleled Dies in an SiC Power Module in Solid-State Circuit Breaker Applications,” *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11763–11773, Oct. 2021, doi: 10.1109/TPEL.2021.3068608.
- [21] Z. Dong et al., “A Current Limiting Strategy for WBG-Based Solid-State Circuit Breakers With Series-Connected Switching Cells,” *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14062–14066, Dec. 2022, doi: 10.1109/TPEL.2022.3199162.
- [22] Y. He et al., “Control Development and Fault Current Commutation Test for the EDISON Hybrid Circuit Breaker,” *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8851–8865, Jul. 2023, doi: 10.1109/TPEL.2023.3262605.
- [23] X. Han, L. Zheng, R. P. Kandula, K. Kandasamy, D. Divan, and M. Saeedifard, “Characterization of 3.3-kV Reverse-Blocking SiC Modules for Use in Current-Source Zero-Voltage-Switching Converters,” *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 876–887, Jan. 2021, doi: 10.1109/TPEL.2020.2999878.
- [24] J. Wang, R. Burgos, D. Boroyevich, and Z. Liu, “Design and Testing of 1 kV H-bridge Power Electronics Building Block Based on 1.7 kV SiC MOSFET Module,” in 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia), May 2018, pp. 3749–3756. doi: 10.23919/IPEC.2018.8507368.
- [25] Z. Zhang, C. Liu, M. Wang, Y. Si, Y. Liu, and Q. Lei, “High-Efficiency High-Power-Density CLLC Resonant Converter With Low-Stray-Capacitance and Well-Heat-Dissipated Planar Transformer for EV On-Board Charger,” *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10831–10851, Oct. 2020, doi: 10.1109/TPEL.2020.2980313.

- [26] J. Hu et al., "Design and Qualification of a 100-kW Three-Phase SiC-Based Generator Rectifier Unit Rated for 50 000-Ft Altitude," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 2, pp. 1865-1878, April 2023, doi: 10.1109/JESTPE.2022.3223415.
- [27] S. Ji et al., "Medium Voltage (13.8 kV) Transformer-less Grid-Connected DC/AC Converter Design and Demonstration Using 10 kV SiC MOSFETs," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA: IEEE, Sep. 2019, pp. 1953–1959. doi: 10.1109/ECCE.2019.8912882.
- [28] N. Kolli et al., "Design Considerations of Three Phase Active Front End Converter for 13.8 kV Asynchronous Microgrid Power Conditioning System enabled by Series Connection of Gen-3 10 kV SiC MOSFETs," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2021, pp. 1211–1218. doi: 10.1109/ECCE47101.2021.9594975.
- [29] C.-C. Liu et al., "Microgrid Building Blocks: Concept and Feasibility," *IEEE Open Access J. Power Energy*, vol. 10, pp. 463–476, 2023, doi: 10.1109/OAJPE.2023.3282188.
- [30] S. Mocevic et al., "Design of a 10 kV SiC MOSFET-based high-density, high-efficiency, modular medium-voltage power converter," *iEnergy*, vol. 1, no. 1, pp. 100–113, Mar. 2022, doi: 10.23919/IEN.2022.0001.
- [31] S. Mocevic et al., "High Power Density 10 kV SiC MOSFET-Based Modular, Scalable Converter for Medium Voltage Applications," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2022, pp. 422–429. doi: 10.1109/APEC43599.2022.9773720.
- [32] S. Mocevic et al., "Power Cell Design and Assessment Methodology Based on a High-Current 10-kV SiC MOSFET Half-Bridge Module," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 3916–3935, Aug. 2021, doi: 10.1109/JESTPE.2020.2995386.
- [33] W. Chen, K. Zhuang, and X. Ruan, "A Input-Series- and Output-Parallel-Connected Inverter System for High-Input-Voltage Applications," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2127–2137, Sep. 2009, doi: 10.1109/TPEL.2009.2019578.
- [34] P. J. Grbovic, "Master/Slave Control of Input-Series- and Output-Parallel-Connected Converters: Concept for Low-Cost High-Voltage Auxiliary Power Supplies," *IEEE Trans.*

- Power Electron., vol. 24, no. 2, pp. 316–328, Feb. 2009, doi: 10.1109/TPEL.2008.2006975.
- [35] W. Chen, G. Wang, X. Ruan, W. Jiang, and W. Gu, “Wireless Input-Voltage-Sharing Control Strategy for Input-Series Output-Parallel (ISOP) System Based on Positive Output-Voltage Gradient Method,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 6022–6030, Nov. 2014, doi: 10.1109/TIE.2014.2308147.
- [36] T. Meng, Y. Song, Z. Wang, H. Ben, and C. Li, “Investigation and Implementation of an Input-Series Auxiliary Power Supply Scheme for High-Input-Voltage Low-Power Applications,” *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 437–447, Jan. 2018, doi: 10.1109/TPEL.2017.2669211.
- [37] T. Meng, H. Ben, Y. Song, and C. Li, “Analysis and Suppression of the Circulating Current Influence in the Input-Series Auxiliary Power Supply for High-Input-Voltage Applications,” *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6533–6543, Jul. 2019, doi: 10.1109/TPEL.2018.2876299.
- [38] R. Torrico-Bascop and N. Barbi, “A double ZVS-PWM active-clamping forward converter: analysis, design, and experimentation,” *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 745–751, Nov. 2001, doi: 10.1109/63.974372.
- [39] T. Meng, C. Li, H. Ben, and J. Zhao, “An Input-Series Flyback Auxiliary Power Supply Scheme Based on Transformer-Integration for High-Input Voltage Applications,” *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6383–6393, Sep. 2016, doi: 10.1109/TPEL.2015.2505322.
- [40] Qingcong Hu and R. Zane, “LED Driver Circuit with Series-Input-Connected Converter Cells Operating in Continuous Conduction Mode,” *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 574–582, Mar. 2010, doi: 10.1109/TPEL.2009.2029337.
- [41] S. Xiong, S.-C. Wong, S.-C. Tan, and C. K. Tse, “A Family of Exponential Step-Down Switched-Capacitor Converters and Their Applications in Two-Stage Converters,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1870–1880, Apr. 2014, doi: 10.1109/TPEL.2013.2270290.
- [42] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. A. Meynard, “Multicell converters: active control and observation of flying-capacitor voltages,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 998–1008, Oct. 2002, doi: 10.1109/TIE.2002.803200.

- [43] J. Won, G. Jalali, X. Liang, C. Zhang, S. Srdic, and S. M. Lukic, "Auxiliary Power Supply for Medium-Voltage Power Converters: Topology and Control," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 4145–4156, Jul. 2019, doi: 10.1109/TIA.2019.2915511.
- [44] M. Chen, K. K. Afridi, S. Chakraborty, and D. J. Perreault, "Multitrack Power Conversion Architecture," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 325–340, Jan. 2017, doi: 10.1109/TPEL.2016.2526973.
- [45] M. Kasper, D. Bortis, and J. W. Kolar, "Novel high voltage conversion ratio " Rainstick " DC/DC converters," in 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA: IEEE, Sep. 2013, pp. 789–796. doi: 10.1109/ECCE.2013.6646783.
- [46] M. Uno and A. Kukita, "PWM Switched Capacitor Converter With Switched-Capacitor-Inductor Cell for Adjustable High Step-Down Voltage Conversion," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 425–437, Jan. 2019, doi: 10.1109/TPEL.2018.2822344.
- [47] Z. Zhang et al., "High precision gate signal timing control based active voltage balancing scheme for series-connected fast switching field-effect transistors," in 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX: IEEE, Mar. 2018, pp. 925–930. doi: 10.1109/APEC.2018.8341125.
- [48] T. Wang, H. Lin, and S. Liu, "An Active Voltage Balancing Control Based on Adjusting Driving Signal Time Delay for Series-Connected SiC MOSFETs," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 1, pp. 454–464, Mar. 2020, doi: 10.1109/JESTPE.2019.2944164.
- [49] P. J. Grbovic, "High-Voltage Auxiliary Power Supply Using Series-Connected MOSFETs and Floating Self-Driving Technique," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1446–1455, May 2009, doi: 10.1109/TIE.2009.2012418.
- [50] F. Zhang, X. Yang, Y. Ren, L. Feng, W. Chen, and Y. Pei, "A Hybrid Active Gate Drive for Switching Loss Reduction and Voltage Balancing of Series-Connected IGBTs," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7469–7481, Oct. 2017, doi: 10.1109/TPEL.2016.2633658.
- [51] S. Ji, T. Lu, Z. Zhao, H. Yu, and L. Yuan, "Series-Connected HV-IGBTs Using Active Voltage Balancing Control With Status Feedback Circuit," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4165–4174, Aug. 2015, doi: 10.1109/TPEL.2014.2360189.

- [52] V. U. Pawaskar and G. Gohil, "Closed Loop dv/dt Control for Equal Voltage Sharing Between Series Connected SiC MOSFETs," in 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA: IEEE, Sep. 2019, pp. 3303–3310. doi: 10.1109/ECCE.2019.8913123.
- [53] F. Zhang, Y. Ren, X. Yang, W. Chen, and L. Wang, "A High Input Voltage Auxiliary Power Supply Utilizing Automatic Balanced MOSFET Stack," IEEE Trans. Ind. Electron., vol. 68, no. 11, pp. 10654–10665, Nov. 2021, doi: 10.1109/TIE.2020.3038097.
- [54] N. Yan, K. Sun, B. Fan, D. Dong, R. Burgos, and D. Boroyevich, "Scalable Auxiliary Power Supply System for SiC-based Modular Medium Voltage Converters," in 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2023, pp. 2333–2339. doi: 10.1109/APEC43580.2023.10131325.
- [55] K. Sun, N. Yan, X. Lin, R. Burgos, and D. Boroyevich, "A Scalable Self-Powered Balancing Circuit for High-Step-Down-Ratio Auxiliary Power Supply," IEEE Trans. Power Electron., vol. 39, no. 1, pp. 236–244, Jan. 2024, doi: 10.1109/TPEL.2023.3321583.
- [56] L. Zhang et al., "Design Considerations for High-Voltage Insulated Gate Drive Power Supply for 10-kV SiC MOSFET Applied in Medium-Voltage Converter," IEEE Trans. Ind. Electron., vol. 68, no. 7, pp. 5712–5724, Jul. 2021, doi: 10.1109/TIE.2020.3000131.
- [57] H. Li, Z. Gao and F. Wang, "Medium-Voltage Isolated Auxiliary Power Supply Design for High Insulation Capability, Ultra-Low Coupling Capacitance, and Small Size," in IEEE Transactions on Power Electronics, vol. 38, no. 6, pp. 7226–7240, June 2023, doi: 10.1109/TPEL.2023.3244855.
- [58] A. Christe, M. Petkovic, I. Polanco, M. Utvic, and D. Dujic, "Auxiliary submodule power supply for a medium voltage modular multilevel converter," CPSS Trans. Power Electron. Appl., vol. 4, no. 3, pp. 204–218, Sep. 2019, doi: 10.24295/CPSSTPEA.2019.00020.
- [59] G. Rizzoli, L. Zarri, J. Wang, Z. Shen, R. Burgos, and D. Boroyevich, "Design of a two-switch flyback power supply using 1.7 kV SiC devices for ultra-wide input-voltage range applications," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Sep. 2016, pp. 1–5. doi: 10.1109/ECCE.2016.7855028.

- [60] O. S. Senturk, T. Maerki, P. Steimer, and S. McLaughlin, “High voltage cell power supply for modular multilevel converters,” in 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Sep. 2014, pp. 4416–4420. doi: 10.1109/ECCE.2014.6953725.
- [61] Z. Guo and H. Li, “A MHz-Pulse-Transformer Isolated Gate Driver With Signal-Power Integrated Transmission for Medium-Voltage SiC MOSFETs,” *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9415–9427, Aug. 2022, doi: 10.1109/TPEL.2022.3158145.
- [62] N. Yan, D. Dong, and R. Burgos, “A Multichannel High-Frequency Current Link Based Isolated Auxiliary Power Supply for Medium-Voltage Applications,” *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 674–686, Jan. 2022, doi: 10.1109/TPEL.2021.3102055.
- [63] B. Zhou, Z. He, Z. Li, K. Chen, A. Luo, and L. Wang, “High frequency current-fed isolated auxiliary power supply for medium-voltage converter,” *CPSS Trans. Power Electron. Appl.*, vol. PP, no. 99, pp. 1–12, 2023, doi: 10.24295/CPSSSTPEA.2023.00031.
- [64] V.-T. Nguyen, V. U. Pawaskar, and G. Gohil, “Isolated Gate Driver for Medium-Voltage SiC Power Devices Using High-Frequency Wireless Power Transfer for a Small Coupling Capacitance,” *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10992–11001, Nov. 2021, doi: 10.1109/TIE.2020.3038095.
- [65] X. Zhang et al., “A Gate Drive With Power Over Fiber-Based Isolated Power Supply and Comprehensive Protection Functions for 15-kV SiC MOSFET,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 946–955, Sep. 2016, doi: 10.1109/JESTPE.2016.2586107.
- [66] S. Sen, L. Zhang, X. Feng, and A. Q. Huang, “High Isolation Auxiliary Power Supply for Medium-Voltage Power Electronics Building Block,” in 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA: IEEE, Mar. 2020, pp. 2249–2253. doi: 10.1109/APEC39645.2020.9124543.
- [67] N. Yan, Q. Chen, D. Dong, and R. Burgos, “Design of Insulation System in High-Frequency Auxiliary Power Supply for Medium Voltage Applications,” in 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA: IEEE, Oct. 2020, pp. 3492–3499. doi: 10.1109/ECCE44975.2020.9235743.
- [68] S. Srdic, F. Teng, and S. Lukic, “High-isolation Low-coupling-capacitance Standalone Gate Drive Power Supply for SiC-based Medium-Voltage Power Electronic Systems,” in

- 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA: IEEE, Sep. 2019, pp. 3287–3291. doi: 10.1109/ECCE.2019.8912766.
- [69] D. Rothmund, D. Bortis and J. W. Kolar, "Highly compact isolated gate driver with ultrafast overcurrent protection for 10 kV SiC MOSFETs," in CPSS Transactions on Power Electronics and Applications, vol. 3, no. 4, pp. 278-291, Dec. 2018, doi: 10.24295/CPSSTPEA.2018.00028.
- [70] J. Liu, L. Ravi, R. Burgos, S. C. Schmalz, A. Schroedermeier and D. Dong, "Compact MV-Insulated MHz Transformer-Coupled Gate Driver With Staged Turn-Off Scheme for Series-Connected Power Devices in DC Circuit Breaker Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 11, no. 2, pp. 1627-1638, April 2023, doi: 10.1109/JESTPE.2022.3227278.
- [71] K. Sun, Y. Xu, J. Wang, R. Burgos, and D. Boroyevich, "Insulation Design of Wireless Auxiliary Power Supply for Medium Voltage Converters," IEEE J. Emerg. Sel. Top. Power Electron., vol. 9, no. 4, pp. 4200–4211, Aug. 2021, doi: 10.1109/JESTPE.2020.3011075.
- [72] M. Ishigaki, S. Fafard, D. P. Masson, M. M. Wilkins, C. E. Valdivia, and K. Hinzer, "A new optically-isolated power converter for 12 V gate drive power supplies applied to high voltage and high speed switching devices," in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA: IEEE, Mar. 2017, pp. 2312–2316. doi: 10.1109/APEC.2017.7931022.
- [73] X. Liu et al., "A Compact Auxiliary Power Supply Design for a Medium Frequency Solid State Transformer," IEEE Trans. Transp. Electrification, vol. 9, no. 1, pp. 1443-1457, March 2023, doi: 10.1109/TTE.2022.3201574.
- [74] Z. Guo, A. Q. Huang, R. E. Hebner, G. C. Montanari, and X. Feng, "Characterization of Partial Discharges in High-Frequency Transformer Under PWM Pulses," IEEE Trans. Power Electron., vol. 37, no. 9, pp. 11199–11208, Sep. 2022, doi: 10.1109/TPEL.2022.3169747.
- [75] J. Wang, S. Mocevic, R. Burgos, and D. Boroyevich, "High-Scalability Enhanced Gate Drivers for SiC MOSFET Modules With Transient Immunity Beyond 100 V/ns," IEEE Trans. Power Electron., vol. 35, no. 10, pp. 10180–10199, Oct. 2020, doi: 10.1109/TPEL.2020.2980564.

- [76] H. Song, I. Cvetkovic, R. Zhang, C. DiMarino, and D. Boroyevich, "Gate Driver Switching Noise Propagation Study for Medium Voltage SiC-based Power Electronics Building Blocks," in 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Oct. 2022, pp. 1–8. doi: 10.1109/ECCE50734.2022.9948024.
- [77] T. Sun, X. Pei, Y. Shan, J. Pei, and D. Jiang, "Submodule Switching-State Based EMI Modeling and Mixed-mode EMI Phenomenon in MMC," IEEE Trans. Power Electron., vol. 38, no. 2, pp. 1831–1843, Feb. 2023, doi: 10.1109/TPEL.2022.3214990.
- [78] B. Sun, R. Burgos, and D. Boroyevich, "Ultralow Input–Output Capacitance PCB-Embedded Dual-Output Gate-Drive Power Supply for 650 V GaN-Based Half-Bridges," IEEE Trans. Power Electron., vol. 34, no. 2, pp. 1382–1393, Feb. 2019, doi: 10.1109/TPEL.2018.2828384.
- [79] J. Hu, J. Wang, R. Burgos, B. Wen, and D. Boroyevich, "High-Density Current-Transformer-Based Gate-Drive Power Supply With Reinforced Isolation for 10-kV SiC MOSFET Modules," IEEE J. Emerg. Sel. Top. Power Electron., vol. 8, no. 3, pp. 2217–2226, Sep. 2020, doi: 10.1109/JESTPE.2019.2943742.
- [80] D. Pefitsis, M. Antivachis, and J. Biela, "Auxiliary power supply for medium-voltage modular multilevel converters," in 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva: IEEE, Sep. 2015, pp. 1–11. doi: 10.1109/EPE.2015.7309388.
- [81] J. Gottschlich, M. Schafer, M. Neubert, and R. W. De Doncker, "A galvanically isolated gate driver with low coupling capacitance for medium voltage SiC MOSFETs," in 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), Karlsruhe: IEEE, Sep. 2016, pp. 1–8. doi: 10.1109/EPE.2016.7695608.
- [82] Y. Yang and P. Zhang, "In Situ Insulated Gate Bipolar Transistor Junction Temperature Estimation Method via a Bond Wire Degradation Independent Parameter Turn-OFF V_{ce} Overshoot," IEEE Trans. Ind. Electron., vol. 68, no. 10, pp. 10118–10129, Oct. 2021, doi: 10.1109/TIE.2020.3022526.
- [83] U.-M. Choi, F. Blaabjerg, S. Jørgensen, S. Munk-Nielsen, and B. Rannestad, "Reliability Improvement of Power Converters by Means of Condition Monitoring of IGBT Modules," IEEE Trans. Power Electron., vol. 32, no. 10, pp. 7990–7997, Oct. 2017, doi: 10.1109/TPEL.2016.2633578.

- [84] Y. Chen et al., “A thermo-sensitive electrical parameter with maximum dI_C/dt during turn-off for high power Trench/Field-Stop IGBT modules,” in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA: IEEE, Mar. 2016, pp. 499–504. doi: 10.1109/APEC.2016.7467918.
- [85] Y. Yang and P. Zhang, “A Novel Converter-Level IGBT Junction Temperature Estimation Method Based on the Bus Voltage Ringing,” *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4553–4563, Apr. 2022, doi: 10.1109/TPEL.2021.3119700.
- [86] A. Griffo, J. Wang, K. Colombage, and T. Kamel, “Real-Time Measurement of Temperature Sensitive Electrical Parameters in SiC Power MOSFETs,” *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2663–2671, Mar. 2018, doi: 10.1109/TIE.2017.2739687.
- [87] L. Qiao, F. Wang, J. Dyer, and Z. Zhang, “Online Junction Temperature Monitoring for SiC MOSFETs Using Turn-On Delay Time,” in 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA: IEEE, Mar. 2020, pp. 1526–1531. doi: 10.1109/APEC39645.2020.9124345.
- [88] C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, and P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” in 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA: IEEE, Sep. 2013, pp. 3235–3242. doi: 10.1109/ECCE.2013.6647125.
- [89] Y. Zhang, H. Wang, Z. Wang, Y. Yang, and F. Blaabjerg, “Simplified Thermal Modeling for IGBT Modules With Periodic Power Loss Profiles in Modular Multilevel Converters,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2323–2332, Mar. 2019, doi: 10.1109/TIE.2018.2823664.
- [90] B. Wang et al., “Air-Cooling System Optimization for IGBT Modules in MMC Using Embedded O-Shaped Heat Pipes,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 3992–4003, Aug. 2021, doi: 10.1109/JESTPE.2021.3054918.
- [91] B. Wang et al., “An Evaluation on Thermal Performance Improvements for SiC Power Module Integrated With Vapor Chamber in MMC,” in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 5, pp. 5214–5225, Oct. 2022, doi: 10.1109/JESTPE.2021.3138744.
- [92] M. Ngo, Y. Cao, K. Nguyen, D. Dong, and R. Burgos, “Computational Fluid Dynamic Analysis and Design of an Air Duct Cooling System for 18 kW, 500 kHz Planar

- Transformers,” in 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Jun. 2021, pp. 1496–1504. doi: 10.1109/APEC42165.2021.9487172.
- [93] Z. Guo, C. Chen, R. Yu, and A. Q. Huang, “A High Power 200kW Medium Frequency Transformer With Improved Thermal Management,” in 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA: IEEE, Oct. 2023, pp. 5587–5591. doi: 10.1109/ECCE53617.2023.10362391.
- [94] Y. Ruan, Y. Cao, D. Dong, and Q. Li, “A High-efficiency Modular Air-Cooling Method for PCB Winding with the Additive Manufacturing,” in 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA: IEEE, Mar. 2023, pp. 449–455. doi: 10.1109/APEC43580.2023.10131470.
- [95] S. Madhusoodhanan, K. Mainali, A. Tripathi, A. Kadavelugu, D. Patel, and S. Bhattacharya, “Thermal design considerations for medium voltage power converters with 15 kV SiC IGBTs,” in 2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Jun. 2015, pp. 1–8. doi: 10.1109/PEDG.2015.7223105.
- [96] A. Anurag, S. Acharya, S. Bhattacharya, and T. R. Weatherford, “Thermal Performance and Reliability Analysis of a Medium-Voltage Three-Phase Inverter Considering the Influence of High dv/dt on Parasitic Filter Elements,” IEEE J. Emerg. Sel. Top. Power Electron., vol. 8, no. 1, pp. 486–494, Mar. 2020, doi: 10.1109/JESTPE.2019.2952570.
- [97] S. G. Kandlikar and C. N. Hayner, “Liquid Cooled Cold Plates for Industrial High-Power Electronic Devices—Thermal Design and Manufacturing Considerations,” Heat Transf. Eng., vol. 30, no. 12, pp. 918–930, Oct. 2009, doi: 10.1080/01457630902837343.
- [98] C. -W. Chang et al., “Thermal Consideration and Design for a 200-kW SiC-Based High-Density Three-Phase Inverter in More Electric Aircraft,” in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 11, no. 6, pp. 5910–5929, Dec. 2023, doi: 10.1109/JESTPE.2023.3308854.
- [99] “Common Coolant Types and their Uses in Liquid Cooling Systems | The World Leader in Thermal Management Solutions.” Accessed: Jan. 06, 2024. [Online]. Available: <https://lairdthermal.com/thermal-technical-library/application-notes/common-coolant-types-and-their-uses-liquid-cooling-systems>

- [100] M. Marrone, “WHAT IS A CHILLER & HOW DOES IT WORK? | INDUSTRIAL CHILLER WORKING PRINCIPLE,” Cold Shot Chillers. Accessed: Jan. 07, 2024. [Online]. Available: <https://waterchillers.com/blog/how-does-a-chiller-work/>
- [101] “Chillers,” Boyd | Trusted Innovation. Accessed: Jan. 08, 2024. [Online]. Available: <https://www.boydcorp.com/thermal/liquid-cooling-systems/chillers.html>
- [102] B. Blog, “Selecting a Recirculating Chiller & Cooling Capacity Factors,” Boyd | Trusted Innovation. Accessed: Jan. 08, 2024. [Online]. Available: <https://www.boydcorp.com/blog/selecting-recirculating-chillers.html>
- [103] D. N. P. Group, “The Basics of Heat Pipes – Their History, Principle, and Varieties explained | Column | Solutions/Products/Services | DNP Dai Nippon Printing,” Dai Nippon Printing Co., Ltd. Accessed: Jan. 07, 2024. [Online]. Available: https://www.global.dnp/biz/column/detail/10162360_4117.html
- [104] “HiK Plates/ Heat Pipe Assemblies,” 1-ACT. Accessed: Jan. 07, 2024. [Online]. Available: <https://www.1-act.com/thermal-solutions/passive/heat-pipes/hik-plates/>
- [105] “Heat Pipes,” Boyd | Trusted Innovation. Accessed: Jul. 04, 2024. [Online]. Available: <https://www.boydcorp.com/thermal/two-phase-cooling/heat-pipe-assemblies.html>
- [106] “Heat Pipes 101,” 1-ACT. Accessed: Jan. 07, 2024. [Online]. Available: <https://www.1-act.com/thermal-solutions/passive/heat-pipes/heat-pipes-101/>
- [107] B. Blog, “Heat Pipes versus Vapor Chambers: What’s the Difference?,” Boyd | Trusted Innovation. Accessed: Jan. 07, 2024. [Online]. Available: <https://www.boydcorp.com/blog/heat-pipes-versus-vapor-chambers.html>
- [108] “Two Phase Thermal Solution Guide,” Boyd | Trusted Innovation. Accessed: Jan. 07, 2024. [Online]. Available: <https://www.boydcorp.com/about-boyd/resources/technical-papers-and-guides/two-phase-thermal-solution-guide.html>
- [109] B. Blog, “What Is a Thermosiphon?,” Boyd | Trusted Innovation. Accessed: Jan. 07, 2024. [Online]. Available: <https://www.boydcorp.com/blog/what-is-a-thermosiphon.html>
- [110] B. Blog, “Thermosiphons vs Heat Pipes,” Boyd | Trusted Innovation. Accessed: Jan. 07, 2024. [Online]. Available: <https://www.boydcorp.com/blog/thermosiphons-vs-heat-pipes.html>
- [111] “Heat Sinks,” Boyd | Trusted Innovation. Accessed: Jul. 04, 2024. [Online]. Available: <https://www.boydcorp.com/thermal/air-cooling/heat-sinks.html>

- [112] “Axial Fans,” Boyd | Trusted Innovation. Accessed: Jan. 08, 2024. [Online]. Available: <https://www.boydcorp.com/thermal/air-cooling/axial-fans.html>
- [113] B. Blog, “We’re a Big Fan of Forced Convection,” Boyd | Trusted Innovation. Accessed: Jan. 08, 2024. [Online]. Available: <https://www.boydcorp.com/blog/forced-convection.html>
- [114] Y. Xu et al., “High Power Density Medium-Voltage Converter Integration via Electric Field Management,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 1, pp. 895–905, Feb. 2022, doi: 10.1109/JESTPE.2021.3107343.
- [115] H. Li, Z. Gao and F. Wang, "Design and Demonstration of an 850 V dc to 13.8 kV ac 100 kW Three-phase Four-wire Power Conditioning System Converter Using 10 kV SiC MOSFETs," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 989-994, doi: 10.1109/APEC43580.2023.10131291.
- [116] C. Gammeter, F. Krismer, and J. W. Kolar, “Weight Optimization of a Cooling System Composed of Fan and Extruded-Fin Heat Sink,” *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 509–520, Jan. 2015, doi: 10.1109/TIA.2014.2336977.
- [117] S. A. Assadi et al., “Electro-Thermal Co-design of a High-Density Power-Stage for a Reconfigurable-Battery-Assisted Electric-Vehicle Fast-Charger using Multi-Physics Co-simulation and Topology Optimization,” in 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA: IEEE, Mar. 2023, pp. 1808–1815. doi: 10.1109/APEC43580.2023.10131627.
- [118] Y. Zhang, H. Wang, Z. Wang, and F. Blaabjerg, “System-Level Thermal Modeling of a Modular Multilevel Converter,” in 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2020, pp. 2766–2771. doi: 10.1109/APEC39645.2020.9124434.
- [119] H. Li et al., “Hardware design of a 1.7 kV SiC MOSFET based MMC for medium voltage motor drives,” in 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2018, pp. 1649–1655. doi: 10.1109/APEC.2018.8341238.
- [120] Y. P. Frei and D. Dujic, “Thermal Design of a Medium Voltage Modular Multilevel Converter Cell,” in 2023 25th European Conference on Power Electronics and Applications (EPE’23 ECCE Europe), Aalborg, Denmark: IEEE, Sep. 2023, p. P.1-P.8. doi: 10.23919/EPE23ECCEurope58414.2023.10264448.

- [121] X. Feng et al., “Multiscale electrothermal design of a modular multilevel converter for grid-tied applications,” in 2021 IEEE Energy Conversion Congress and Exposition (ECCE), Oct. 2021, pp. 5657–5664. doi: 10.1109/ECCE47101.2021.9595660.
- [122] M. Lin, R. Chen, D. Li, L. M. Tolbert, F. Wang, and H. Bai, “Design and Testing of a 6.5 kV Submodule Based on a 10 kV SiC Power Module,” in 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA: IEEE, Oct. 2023, pp. 5794–5800. doi: 10.1109/ECCE53617.2023.10362471.
- [123] M. Lin, L. M. Tolbert, and B. Rowden, “Protection Scheme Analysis of LLC Series Connected Auxiliary Power Supply for HV SiC Grid-Connected Inverters,” in 2024 IEEE Energy Conversion Congress and Exposition (ECCE), Oct. 2024, pp. 6822–6826. doi: 10.1109/ECCE55643.2024.10860777.
- [124] R. Chen et al., “Design of 10 kV SiC MOSFET Power Module Based MW-level Modular Multilevel Converter Phase-leg,” in 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA: IEEE, Feb. 2024, pp. 1087–1094. doi: 10.1109/APEC48139.2024.10509400.
- [125] M. Lin, R. Chen, D. Li, L. M. Tolbert, F. Wang, and H. Bai, “Temperature Sensitive Electrical Parameters Selection for 10 kV SiC Power Module,” in 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA: IEEE, Oct. 2023, pp. 5525–5530. doi: 10.1109/ECCE53617.2023.10362474.
- [126] L. Zhang et al., “Design Considerations for High-Voltage Insulated Gate Drive Power Supply for 10-kV SiC MOSFET Applied in Medium-Voltage Converter,” *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5712–5724, Jul. 2021, doi: 10.1109/TIE.2020.3000131.
- [127] R. Chen, M. Lin, X. Huang, F. Wang, and L. M. Tolbert, “An Improved Turn-on Switching Transient Model of 10 kV SiC MOSFET,” in 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2022, pp. 1–8. doi: 10.1109/APEC43599.2022.9773432.
- [128] D. Johannesson, M. Nawaz, and K. Ilves, “Assessment of 10 kV, 100 A Silicon Carbide mosfet Power Modules,” *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5215–5225, Jun. 2018, doi: 10.1109/TPEL.2017.2728723.
- [129] Z. Guo, H. Li, F. Z. Peng, M. Steurer, and K. J. Olejniczak, “Gate Driver Development and Stray Inductance Extraction of 10 kV SiC MOSFET Module for a Switched-Capacitor

- MMC Application,” in 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2022, pp. 1387–1393. doi: 10.1109/APEC43599.2022.9773466.
- [130] M. Lin, R. Chen, D. Li, L. M. Tolbert, F. Wang and H. Bai, "Design of a Cooling System in a Medium Voltage MMC," 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024, pp. 3041-3046, doi: 10.1109/APEC48139.2024.10509483.
- [131] X. Lin et al., “Design and Testing of a 13.8 kV/ 1.1MVA 3-Phase 5-Level Flying Capacitor Converter with 10 kV SiC MOSFETs”.

Vita

Min Lin is from Fuzhou, Fujian province in China. She received her B.S. in electrical engineering from the North China Electric Power University, China, in June 2019. She joined Professor Leon M. Tolbert's group at the University of Tennessee at Knoxville in August 2019 to pursue a Ph.D. degree in Electrical Engineering. Her research interests include application of 10 kV SiC MOSFET in medium voltage converter, auxiliary power supplies and cooling system design.