Design Considerations on Insulation and Magnetics for Medium Voltage DC/DC Converters

A Dissertation Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Zihan Gao

May 2025

© by Zihan Gao, 2025

All Rights Reserved.

To my grandparents and parents.

Acknowledgments

First, I would like to sincerely thank my advisor, Dr. Fred Wang, for his consistent support and guidance throughout my entire Ph.D. study. His deep knowledge and insightful vision in power electronics taught me how to approach real-world problems through research. Dr. Wang's open-mindedness in life, his rigorous attitude toward research and projects, and his experience in industry and academia have greatly shaped my thinking as a researcher and engineer. I also appreciate the opportunities he provided for me to challenge myself and to explore one of the cutting-edge topics of power electronics with greater depth and breadth.

I am also deeply grateful to Dr. Kevin Bai for his support throughout my Ph.D. study and for his valuable suggestions on research and writing. I am grateful to Dr. Daniel Costinett as well. His deep knowledge, shared through courses, publications, and insightful conversations, has greatly enriched my understanding and helped me address many challenges in my research. I also want to thank Dr. Hongbo Zhao for kindly accepting my invitation to serve on my Ph.D. committee. His thoughtful

feedback and advice on my research, presentations, and his friendship have been greatly appreciated.

I would like to extend my sincere appreciation and respect to the former and current staff members of CURENT and the Department of EECS for their professional and invaluable support throughout my study, research, and my role as chair of the 2023 CURENT Annual Industry Conference. These individuals include, but are not limited to, Mr. Robert Martin, Ms. Wendy Smith, Ms. Anne Skutnik, Mr. Ryan Smiley, Ms. Lisa Beard, Ms. Lori Houser, Ms. Dana Bryson, Ms. Michelle Champ, Ms. Reina Ortega, Mr. Michael Rogers, Mr. Dwayne Kelly, Ms. Samantha White, Mr. Hao Ye, and Mr. Alaa Alharzi. I am also grateful to our project consultant, Mr. William Giewont, for his helpful advice drawn from his extensive industry experience.

Many thanks also go to my colleagues, teammates, and alumni of UTK who generously supported me in both my research and daily life. I am especially grateful to Dr. Ruirui Chen, Dr. Shiqi Ji, Dr. Haiguo Li, Dr. Zhou Dong, Dr. Kong Le, Dr. Liang Qiao, Dr. Wen Zhang, Dr. Dingrui Li, Dr. Jingxin Wang, Mr. Jiahao Niu, Dr. Cheng Nie, Dr. Bo Liu, Dr. Ren Ren, Dr. Zhe Yang, Dr. Zheyu Zhang, Dr. Shuoting Zhang, Mr. James Palmer, Dr. Shimul Dam, Dr. Anubrata Das, Dr. Nurpur, Dr. Venkata Itte, Dr. Li Zhang, Mr. John Meadors, Dr. Pengfei Yao, Mr. Yanda Lyu, Mr. Xianchao Liu, Mr. Ching-Hsiang Yang, Dr. Yang Xu, Mr. Samuel Klein, Dr. Yiwei Ma, Dr. Yuru Wu, Dr. Xingxuan Huang, Dr. Handong Gui, Mr. Mohamed Al-Sager, Dr. Jingjing Sun, Dr. Shuyao Wang, Dr. Nattapatt Praisuwanna, Dr. Paychuda Kritprajun, Mr. Hoang Phuc Peter Pham, Mr. Min Lin, Mr. Xingyue

Tian, Dr. Shiyuan Fan, Dr. Niu Jia, Ms. Sadia Binte Sohid, Mr. Ziwei Liang, Mr. Shishir Lamichhane, Mr. Saurav Dulal, Dr. Yang Huang, Dr. Liyan Zhu, Dr. Yu Yan, Mr. Yicheng Zhang, Mr. Ximu Zhang, Mr. Yue Sun, Mr. Rajib Bijukchhe, Dr. Chengwen Zhang, Dr. Jie Li, Dr. Ling Jiang, Dr. Chongwen Zhao, Dr. Kamal Sabi, Dr. Andrew Foote, Dr. Jared Baxter, Mr. Jared Walden, Mr. Xin Xia, Dr. Ruiyang Qin, Mr. Denis Chertkovsky, Mr. Paxton Wills, Mr. William Norton, Ms. Xin Gao, Mr. Yiju Wang, Mr. Noah Wilding, Dr. Fei Yang, Mr. Jacob Dyer, Ms. Paige Williford, Mr. Ziming Wang, and Dr. Edward Jones. I would also like to thank my friends outside of Knoxville for their encouragement and support in recent years, including Dr. Zhehui Guo, Dr. Yunlei Jiang, Ms. Lin Zhang, Dr. Yuliang Cao, Dr. Zibo Chen, Dr. Rudy Wang, Dr. Zhicheng Guo, Dr. Yuchen He, Dr. Xiaofeng Dong, Dr. Min Gao, Dr. Lifang Yi, Dr. Bokang Zhou, Dr. Jinli Zhu, Dr. Qingyun Xie, Dr. Xingchen Zhao, Ms. Xueyue Liu, Dr. Bingrui Li, Dr. Yue Yuan, Dr. Jian Liu, Dr. Xiaoyan Liu, Dr. Zheqing Li, Dr. Maohang Qiu, Mr. Mian Liao, Mr. Ruomu Hao, and Mr. Yanwen Lai.

My heartfelt thanks go to my parents, Guangyong Gao and Suzhi Cao, and to my late grandparents, Xinghe Gao, Jinlan Zhao, Jimin Cao, and Guiying Zhi, for their unconditional love and support over the past 28 years.

This dissertation made use of Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and the Department Of Energy under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

Abstract

Medium voltage (MV) SiC devices have drawn considerable attention thanks to their high voltage blocking and fast switching capabilities, enabling new generations of high-power and high-density MV power conversion. However, many challenges can be found in implementing MV converters with MV SiC devices, such as insulation, efficiency, density, and parasitics. In this dissertation, several techniques have been proposed to address those issues.

First, a low-loss leakage integration technique using ferrite bridges and 2-D laminated magnetic cores is proposed for shell-type transformer structures. Then, a 2-D lamination configuration for ribbon- and sheet-based magnetic core is proposed, which further reduces the leakage-induced eddy current loss.

Second, a ferrite shielding strategy is introduced to reduce eddy current losses in laminated-core inductors and transformers by covering critical surfaces and bracketing the core sides. The mechanism of the proposed ferrite is analyzed and experimentally validated.

Third, a dry-type insulation scheme is proposed for the MV inductor and transformer windings. Insulation materials are characterized with simple test sample designs. The winding structure, shielding, and field grading methods have been introduced. A simplified vacuum encapsulation process is also proposed with fewer chambers and less tubing while the quality of the encapsulation is maintained.

A common-mode (CM) switching loss reduction method is proposed for DC/DC feeding cascaded H-bridge (CHB) converters by studying the mechanism and applying a diode-clamped grounding circuit. The operating principle of the diode-clamped circuit for the CHB is also discussed.

A compact MV power stage design strategy is also developed. The proposed heatsink field shaping is implemented to reduce the insulation clearance requirement. With the sloping air duct design, additional creepage distance can also be provided. Simplified gate drive design with commercial solution and compact power stage design are also demonstrated.

Finally, a flux balancing scheme for MV dual-active-bridge (DAB) converter transformers is proposed utilizing the magnetizing harmonic current. Ferrite gaps generate harmonics for flux unbalance detection, modeled and verified with dedicated sensing and control in DAB prototypes.

Table of Contents

1 Introduction 1

1.1 Background 1

1.2 Medium Voltage DC/DC Converters 4

1.2.1 MV Medium Frequency Transformers 10

1.3 Design Challenges of MV DC/DC Converters 15

1.3.1 Insulation 15

1.3.2 Leakage Integration 17

1.3.3 Parasitics Capacitance Induced Loss 20

1.3.4 Transformer Saturation 22

1.4 Dissertation Outline 25

2 Low-Loss MV Transformer Leakage Integration With 2D Lamination 27

2.1 Literature Review 27

2.2 Leakage Inductance and Eddy Current Loss 32

2.3 Ferrite Bridge-Based Leakage Integration 35

2.4 2-D Lamination 39
2.5 Test Verification 44
2.6 Potential Future 2-D Lamination Structure 51
2.7 Summary 53

3 Eddy Current Suppression for Ribbon-Based Magnetics Using Ferrite Shielding 56
3.1 Literature Review 56
3.2 Proposed Ferrite Shielding Structure: Case Studies 59
3.2.1 Eddy Current Reduction on Gapped Inductors 59
3.2.2 Eddy Current Reduction on Core-Type Transformer 67
3.2.3 Eddy Current Reduction on Shell-Type Transformer 72
3.3 Summary 77

4 Dry-Type Insulation Design for MV Transformers and Inductors . 79
4.1 Literature Review 79
4.2 Characterization of Insulation Materials 84
4.2.1 Mechanical Structural Material 84
4.2.2 Combination of Encapsulant and Structural Materials 88
4.3 Dry-Type Winding Insulation Structure 92
4.3.1 Structural Design of Dry-Type Winding 92
4.3.2 Partial Shielding and Field Grading 96
4.4 Dry-Type Encapsulation Procedure 102

4.5 Partial Discharge Test Validation 105
4.6 Validation in Converter Testing 109
4.6.1 MV Transformer Test in DAB Converter System 109
4.6.2 MV Inductor in Flying Capacitor Converters 109
4.7 Summary 113

5 Diode Clamped Grounding for Switching Loss Reduction due to Common-Mode Parasitic Capacitances 115

5.1 Literature Review 115
5.2 Mechanism on Capacitance Induced CM Switching Loss 116
5.3 Diode-Clamped Grounding Configuration 122
5.3.1 Topology with Diode Clamped Grounding Circuit 122
5.3.2 Operational Analysis of the Diode Grounding Circuit 124
5.4 Simulation and Test Validation 128
5.4.1 Simulation Verification 128
5.4.2 Experimental Verification 129
5.5 Impact Factors 133
5.5.1 Diode Parasitics 133
5.5.2 Grounding Loop Impedance 134
5.5.3 Gate Signal Delay 134
5.6 Summary 136

6 Compact MV Power Stage Design With Heatsink Electric Field Shaping 138

6.1 Literature Review 138

6.2 Electric Field Shaping and Air Duct 142

6.2.1 Field Shaping of Heat Sinks 142

6.2.2 Air Duct with Mechanical Support and Creepage 145

6.2.3 Simulation and Test Results 145

6.2.4 Field Shaping for MV Power Modules 152

6.3 Simplified Gate Drive Design 152

6.4 Power Stage Assembly and Test 157

6.4.1 Bus Bar Design 157

6.4.2 Power Stage Assembly 157

6.5 Summary 160

7 Harmonic-Based Transformer Flux Balancing Strategy for MV DAB Converters 167

7.1 Literature Review 167

7.1.1 Problem: Transformer Flux Unbalance 167

7.1.2 Flux Unbalance Estimation 170

7.1.3 Flux Unbalance Detection 171

7.1.4 Flux Balancing Methods 177

7.2 Flux Unbalance Analysis and Detection 181

7.2.1 Magnetic Gap and Non-Linear Magnetizing Current 181

7.2.2 Modeling of the Magnetic Gap in Dual-Active-Bridge Converters190

7.2.3 Harmonic Characteristics for Flux Unbalance 197

7.3 Flux Sensor Design and Validation 201

7.4 Flux Balancing Scheme and Test 209

7.4.1 Steady-state Flux balancing control 209

7.4.2 Test Verification 214

7.5 Summary 226

8 Conclusions and Future Work 228

8.1 Summary and Conclusion 228

8.2 Future Work 232

Bibliography 234

Vita 260

List of Tables

2.1 Leakage Integrated Transformer Parameters 45

4.1 Metrics of MV Flying Capacitor Converter and Its Inductor 112

7.1 Parameter Comparison for 850/850 V and 850/6700 V Transformers . 185

7.2 Sensor Gain Settings for Unity and Fractional Turns Ratios. 206

List of Figures

1.1 Global energy consumption trend by different sources [1]. 2

1.2 (a) The traditional and (b) future power grid [2]. 3

1.3 A configuration of flexible microgrid [3, 4]. 5

1.4 Topology of the MV (a) series resonant converter with series connected devices [5], (b) input-parallel-output-series (IPOS) modular converter [6], and (c) modular multilevel DC/DC converter [7]. 8

1.5 Photographs of 10 kV SiC (a) discrete MOSFET [8], and (b) power module XHV-6 [9]. 9

1.6 MV medium frequency transformers with the dielectric materials of (a) air [10], (b) epoxy without shielding [11], (c) epoxy and silicone with shielding [12], (d) coaxial cable [13]. 12

1.7 Planar MV medium frequency transformers: (a) leveraged concept from wire-less charging coils [14], (b) using PCB winding [15], (c) PCB Litz wire structure [16]. 14

1.8 Dry-type MV winding insulation failure. 16

1.9 MV heat sink insulation failure. 17
1.10 Ribbon core orthogonal flux can induce eddy current [17]. 19
1.11 Transformer test with leakage induced eddy current [18]. 19
1.12 MV converter with (a) switching loop including parasitics [3], (b) current spikes induced by common-mode current induced by parasitics [19, 20]. 21
1.13 Transformer unbalance with (a) switching loop including parasitics [21], (b) current spikes induced by common-mode current induced by parasitics [22]. 23
1.14 Noise waveform and FFT of the current sensor *HO-6P*. 24

2.1 (a) Magnetic energy concentrated on the core surface [23], (b) potential leakage integration methods [17]. 30
2.2 Thermal image of a leakage integrated core-type transformer with high eddy current loss [19]. 31
2.3 Model of the lamination layers: (a) three of lamination layers, and (b) homogenized lamination model [24]. 33
2.4 Simulation results for the core-type transformer under short-circuit test (a) magnetic field distribution, and (b) eddy current density distribution. 35
2.5 Proposed transformer structure for leakage integration, dashed lines: leakage field flowing directions [19]. 37

2.6 Test results of different type of leakage integration: (a) core-type, with total loss of 425 W and estimated eddy current loss 339 W; (b) vertical shell-type, with total loss of 280 W and estimated eddy current loss 113 W; (c) vertical shell-type with interleaved winding, with total loss of 120 W and estimated eddy current loss 31 W. 40
2.7 Transformer short-circuit simulation with proposed structure: (a) solid nanocrystalline core, (b) 2D Laminated core. 42
2.8 Transformer short-circuit simulation with 2D laminated cores (a) core-type, (b) vertical shell-type, (c) interleaved vertical shell-type. 43
2.9 Photograph of the DAB power stages [19] and (b) MV DAB transformer. 46
2.10 Pump back test setup for MV DAB converter. 47
2.11 Test results for MV DAB transformer/converter (a) no-load condition (b) full-load condition [19]. 48
2.12 Efficiency test results of the MV DAB (a) efficiency with bidirectional operation, (b) loss breakdown estimation at full load. 49
2.13 The old core-type MV DAB transformer (a) photo graph, (b) efficiency curve, and (c) loss breakdown estimation at full load. 50
2.14 2D lamination techniques for (a) ribbon-based cores, (b) block- or silicon steel-based cores, and (c) magnetic alloy wire-wound cores. . . 52

3.1 Conventional ferrite shielding structure, (a) bar shield [18], (b) hybrid core structure [25]. 58

3.2 Conceptual drawing of (a) bar shield [18], (b) hybrid core structure [25], and (c) proposed shielding [26]. 60
3.3 Proposed ferrite shielding (a) illustration for the gapped inductor case; (b) flux line simulation results at top view; (c) flux line at perspective view. 61
3.4 Photo of the amorphous inductor core with ferrite shielding. 62
3.5 Inductor simulation results (a) unshielded, current density; (b) shielded, current density; (c) shielded, flux density. 63
3.6 Inductor test results (a) unshielded, thermal image; (b) shielded, thermal image; (c) setup power loss. 65
3.7 Inductor DC bias test results (a) waveform; (b) power loss comparison. 66
3.8 Photo of the proposed (a) transformer with ferrite shielding, (b) nanocrystalline core with shielding. 67
3.9 Core-type transformer short-circuit test results (a) total loss comparison of the transformer short-circuit test setup; (b) unshielded, thermal image; (c) shielded, thermal image; (d) shielded, zoomed-in thermal image with tilted angle. 69
3.10 DAB test for core-type transformer (a) waveform, (b) loss comparison. 71
3.11 Photograph of (a) shell-type transformer with shielding, and (b) nanocrystalline core with shielding. 73
3.12 Test results shell-type transformer: (a) thermal image without shielding; (b) thermal image with shielding; (c) loss comparison. 75

3.13 DAB test for shell-type transformer (a) waveform, (b) loss comparison. 76

4.1 Designed insulation test sample for the 3D printing material, (a) perspective, (b) Cutaway view with features. 85

4.2 Electric field simulation of the 3D printing insulation sample. 86

4.3 Insulation test results of the 3D printed insulation sample, (a) photograph of the sample under test, (b) PD waveform, and (c) photograph of a sample after dielectric breakdown. 87

4.4 Designed insulation test sample for the material combination, (a) 3D drawing of the cutaway view, (b) Simulation results. 89

4.5 Insulation test results of test sample for the material combination, (a) photograph of the sample, (b) PD test waveform. 91

4.6 Mechanical Drawing of a MV DAB transformer, (a) structure of the MV transformer, (b) structure of the MV dry-type winding [27]. . . . 93

4.7 Mechanical Drawing of a MV inductor, (a) structure of the MV inductor, (b) structure of the MV dry-type winding. 95

4.8 Partial shielding of a MV winding, (a) structure of the partially shielded MV transformer with highlighted surfaces to be shielded, (b) simplified simulation of the MV transformer. 97

4.9 Electric field distribution of the partially shielded winding and a grounded PCB at a distance of 80 mm. 98

4.10 Simulation results of the partially shielded MV winding, (a) without high voltage putty, (b) with high voltage putty and zoomed-in zone of high voltage putty. 100
4.11 Simulation results of the high voltage putty covered area, (a) without voids, (b) with void. 101
4.12 The equipment for vacuum pressure encapsulation process, (a) the schematic diagram, (b) photograph of the vacuum chamber, and (c) photograph of the set-up. 103
4.13 The MV transformer winding, (a) PD test waveforms, (b) prototype cut-away photo. 107
4.14 The MV inductor winding, (a) photo, (b) PD test waveform. 108
4.15 Thermal simulation of the DAB transformer: (a) air flow, (b) temperature distribution. 110
4.16 Thermal images of the DAB transformer: (a) top view, (b) side view. 111
4.17 Photo of the 8-Level flying capacitor converter [28]. 112
4.18 Waveform of the 8-Level flying capacitor converter at full voltage rating [28]. 113

5.1 Topology of converter using cells consisting of DC/DC and DC/AC, showing conventional transformer solid grounding [20]. 117
5.2 Current spikes in transformers having high grounding capacitance [29]. 117
5.3 CM model and filter design for a solid-state transformer in [30]. . . . 118

5.4 Unbalanced modulation strategy to reduce CM noise and loss [31]. . . 119
5.5 Simplified 2-stage CHB converter scheme. 121
5.6 CM voltage and current waveforms in 2-stage CHB. 121
5.7 CHB commutation loop and model simplification considering CM capacitance. 123
5.8 Topology of converter using cells consisting of DC/DC and DC/AC, showing diode clamped transformer grounding [20]. 124
5.9 Topology under study: (a) lowest cell with DAB and CHB converters using diode clamped circuit, (b) simplified CM loop. 125
5.10 Grounding parasitic capacitance charging and discharging modes with: (a) positive CM voltage, (b) negative CM voltage. 127
5.11 Simulation results of diode clamped grounding, the transformer shielding potential swing for both upper and lower cell is reduced by half of LVDC link voltage (400 V) [20]. 129
5.12 Photography of (a) MV dc/dc transformer, (b) diode clamping circuit [20]. 130
5.13 Test waveforms for diode clamped grounding (with shielding voltage and grounding current for the upper cell) [20]. 131
5.14 Tested loss comparison between conventional and diode clamped grounding [20]. 132
5.15 Simulation sweep of grounding inductance and capacitance associated loss [20]. 135

5.16 Simulation sweep of gate driving delay and capacitance associated loss [20]. 135

6.1 Grounding connection of device base-plate and heatsink [32]. 140

6.2 Photograph of the 10 kV SiC discrete MOSFET. 141

6.3 Field shaping of heatsink proposed in [33]. 141

6.4 Device/heatsink arrangement of the H-bridge power stage [34]. 143

6.5 Device/heatsink arrangement of the H-bridge power stage [34]. 144

6.6 Proposed air duct (a) cross cut-away view, and (b) creepage distance. 146

6.7 Simulation comparison of (a) bare heatsinks, (b) field shaped heatsinks. 147

6.8 Photograph of heatsink insulation test: (a) at an air gap breakdown, (b) setup of heatsinks with field shaping [34]. 149

6.9 Test results of corona and breakdown onset voltage at different clearances and configurations [34]. 150

6.10 Thermal simulation with the proposed field shaped heatsinks: (a) temperature distribution, (b) air speed distribution. 151

6.11 A heatsink with field shaping for the XHV-9 module: (a) photograph, and (b) simulation result. 153

6.12 Gate drive schematic for discrete 10-kV devices [34]. 154

6.13 (a) Schematic and (b) test waveform for DESAT protection [34]. . . . 155

6.14 10-kV SiC power stage power loop and parasitic inductance [34]. . . . 158

6.15 Photograph of the assembled MV power stage with proposed heatsink structure [34]. 159
6.16 Volume comparison (a) old design and (b) proposed design of the MV power stage [34]. 161
6.17 Photograph of the assembled MV power stage with proposed heatsink structure [34]. 162
6.18 Thermal image of the proposed MV power stage [34]. 163
6.19 Heatsink temperature measurement of the proposed MV power stage. 164

7.1 Magnetizing current run-away during nanocrystalline-based transformer flux unbalance [22]. 168
7.2 Winding and magnetizing currents during load transient. 169
7.3 Magnetizing current sensors (a) for unity turns ratio [35], (b) based on flux gate [36]. 173
7.4 Magnetic branch-based flux sensors: (a) the "Magnetic Ear" [37], (b) internal flux sensor [38]. 174
7.5 The photograph of the magnetostriction based flux sensing [39]. . . . 175
7.6 Volt-second based measurement: (a) *RC* filter [39], (b) paralleled inductor [40]. 176
7.7 ZVS inherent balancing: (a) waveforms of inherent balancing, (b) effectiveness with modulation mismatch [41]. 178

7.8 Transformer flux density waveforms: (a) without transient balancing, (b) with transient balancing [6]. 180
7.9 Utility Transformer: (a) magnetizing current with 25% bias, (b) magnetizing current with 50% bias, (c) reluctance waveform of the core [42]. 182
7.10 $B-H$ loops of: (a) amorphous material from Metglas™[43], (b) ferrite material from Fair-Rite™[44]. 184
7.11 The current waveform with ferrite gap in open-circuit test. 185
7.12 The current waveform with ferrite gap in full load test with flux unbalance. 186
7.13 The current waveform for 850 V/6700 V MV transformer at no-load with (a) balanced flux, (b) unbalanced flux. 188
7.14 The current waveform for 850 V/6700 V MV transformer at full-load with (a) balanced flux, (b) unbalanced flux. 189
7.15 The model of DAB with ferrite gaped transformer. 190
7.16 Circuit diagram of different stages: (a) hysteresis current downward (non-saturated), (b) inductor switched-in (saturated), (c) hysteresis current upward (non-saturated). 192
7.17 Verification and curve fitting of the magnetic gap transformer. 193
7.18 Transformer magnetizing current with different DC bias at no-load. . 194
7.19 Transformer magnetizing current with different DC bias at full-load. . 195
7.20 Transformer magnetizing current with different DC bias at no-load. . 195

7.21 Transformer magnetizing current with different DC bias at full-load. . 196
7.22 FFT analysis of magnetizing current with DC bias. 199
7.23 Fundamental harmonic of magnetizing current with different DC bias and power. 200
7.24 The second-order harmonic component of the magnetizing current at different DC bias and power level [45]. 201
7.25 Schematic of the transformer current sensor. 202
7.26 Photographs of MFT magnetizing current sensors: (a) 850/850 V DAB transformers [45], (b) 850/6700 V DAB transformers [46]. 203
7.27 Test set-up for (a) 850/850 V and (b) 850/6700 V sensors. 205
7.28 Test results for (a) 850/850 V and (b) 850/6700 V sensors. 207
7.29 850 V/850 V sensor tested in DAB. 208
7.30 The control diagram of a DAB converter with flux balancing strategy [46]. 209
7.31 The diagram of the controller board used in test. 210
7.32 The sampling rate evaluation. 212
7.33 The diagram of the second order harmonic signal processing. 213
7.34 The diagram of duty-cycle compensation. 213
7.35 The diagram of the high resolution PWM modulator realized in FPGA. 214
7.36 Photographs of 850/850 V (a) PCS cabinet (b) PCS unit, and (c) test schematic for an 850/850 V DAB unit. 216

7.37 Test results for 850/850 V DAB (a) during transient, (b) after flux balanced [45]. 217
7.38 The test waveforms in an 850/850 V PCS [45]. 218
7.39 Photographs of 850/6700 V (a) PCS cabinet (b) PCS unit. 219
7.40 The test schematic for an 6700/850 V DAB unit. 220
7.41 Waveform for 850/6700 V DAB at no-load condition during disturbance injection. 220
7.42 Zoomed-in waveform for 850/6700 V DAB at no-load condition (a) zoomed-in when flux unbalanced (b) zoomed-in when balance resumed [46]. 222
7.43 Waveform for 850/6700 V DAB at full-load condition during disturbance injection. 223
7.44 Zoomed-in waveform for 850/6700 V DAB at full-load condition (a) zoomed-in when flux unbalanced (b) when balance resumed. 224
7.45 Test results for 850/6700 V DAB during load transition (a) waveforms during the whole transition, (b) zoomed-in waveforms. 225

Chapter 1

Introduction

1.1 Background

Electric power has been a type of energy medium widely utilized by the human's society. Thanks to the technologies developed in the past centuries, it can be easily transformed from and into different forms of energy so that people can harvest, convert, store, and utilize energy for different purpose. As the technologies keep advancing, the energy source has been changing in the past decades and will continue changing in the future, to form a cleaner and more sustainable society. As of the year of 2018, the major energy resources are fossil fuels (e.g., petroleum, coal, and natural gas), nuclear and renewable energies, and over 80% of all the energy utilized over the globe falls into the category of fossil fuels, causing environmental issues and global warming [1]. As estimated by US Energy Information Administration (EIA), which is shown in **Fig. 1.1**, the renewable energy as an energy source will increase

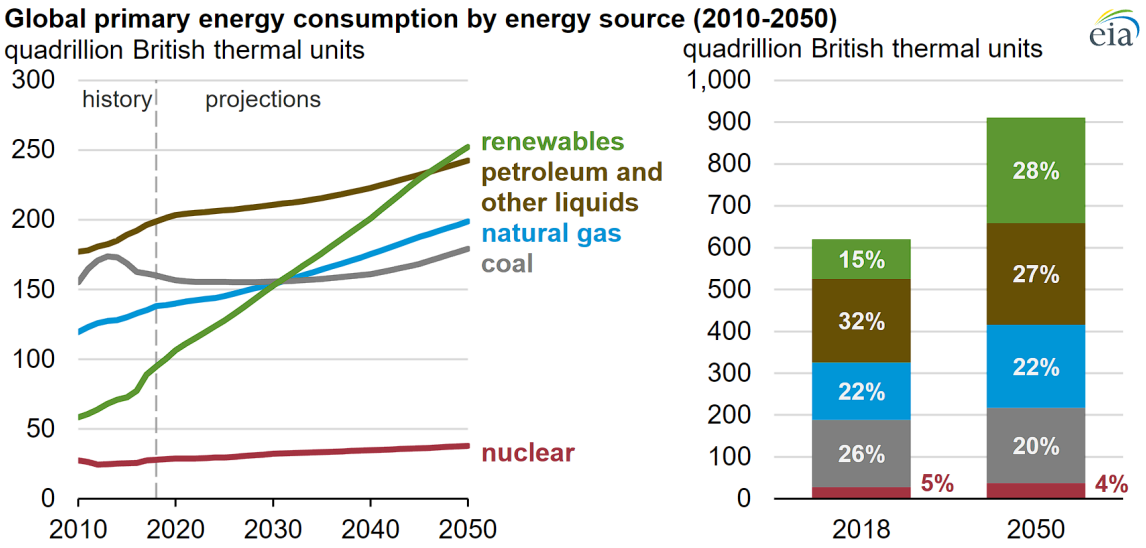
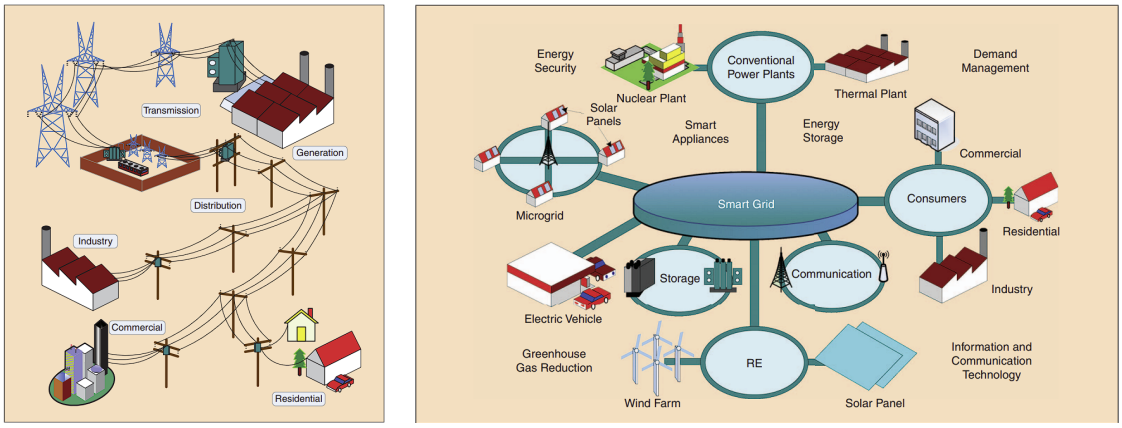


Fig. 1.1: Global energy consumption trend by different sources [1].

steadily, and until the year 2050, renewables will be the biggest source and account for 28% of the total amount of energy utilized throughout the world. With such an evolving trend, the technologies associated with renewable energy in generation, storage, transmission, and delivery, needs to be investigated to accommodate the change.

The network of electric power, i.e., the power grid, has been evolved in the past century with the maturing electrical engineering technologies. It has become a critical power supply for both industries and people's ordinary life, delivering electric power to every corner of the world through generation, transmission, distribution processes as shown in **Fig. 1.2** (a). With the increasing penetration of renewable energy into the power grid, adjustments are needed: as more and more renewable energy sources, especially distributed energy resources, are connected to the grid, energy storage is needed to balance the difference of instantaneous power generation and



(a) **(b)**

Fig. 1.2: (a) The traditional and (b) future power grid [2].

need; as different types and sizes of sources and load are connected into the grid, a more decentralized structure is needed. Finally, a new architecture of smart power grid will be formed as in **Fig. 1.2(b)** [2]. As suggested in the name of the new type of grid, smarter technology is needed to reform the grid, among which power electronics is needed to provide more flexible control and actuation of the new smart grid.

As aforementioned, the trend of high penetration of renewable energy, as well as smart grid, inherently needs new technologies to accommodate the change of electric energy utilization and delivery. The power electronics technology, converting electric power from and into different forms, are of greater and greater importance. The generation of renewable energies, such as wind turbine, photovoltaic, and fuel cell, need power electronic converters to convert the electric energy from different forms, i.e., direct current (DC), or variable frequency alternating current (AC), into constant voltage and frequency to connect to the power grid [47, 48]. The emerging energy

storage, as well as the implementation of emerging technologies on data center and electric vehicles, also requires high amount of energy transformed from the standard form in power grid to DC form to supply the battery or electronic loads [49–51].

Also, with the sources and loads possessing the nature of DC power, DC grid also becomes an emerging technology. With the DC grid, a simple power converter is needed to match only the DC voltage level of different sources and loads, without involving inverters and rectifiers and AC frequency monitoring and control. The DC grid can be more flexible with configuration and voltage variation, and if necessary, can also be connected to other DC and AC grids.

As the grid evolves with different forms of load and source, and also its own trend to form the smart grid, high demand of power electronics has also been implied. New generations of converters with higher voltage and power ratings, smarter functionalities such as grid support, are increasingly critical to the new generation of grid. **Fig. 1.3** shows a configuration with a converter-interfaced flexible combined heat and power (CHP) system, consisting of AC and DC microgrids [3, 4, 50].

1.2 Medium Voltage DC/DC Converters

Because of the trend of advancing grid and motor drives, the immediate need of medium voltage (MV) converter becomes more and more clear. Among the MV power converters, the MV DC/DC converters are of vital importance, as it was less investigated and implemented due to the conventional AC power grid structure, and

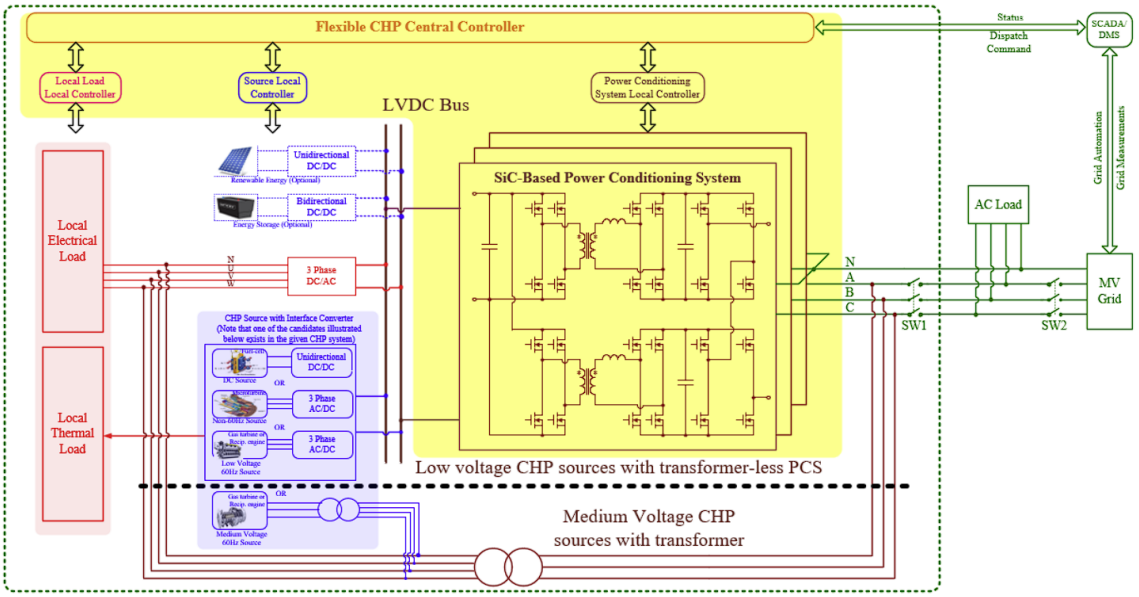


Fig. 1.3: A configuration of flexible microgrid [3, 4].

also the lack of MV passive components for DC/DC converters [52]. The MV DC/DC converters can be implemented into a wide range of applications, such as microgrids and distributive energy resources, electric vehicle charging stations, locomotives and electrified airplanes and ships.

In conventional MV DC/DC converters, With the conventional Si MOSFETs, IGBTs or IGCTs, complicated measures have to be taken in order to accommodate the high current and high voltage stresses which are imposed onto the semiconductor devices [53–58]. Due to the difficulties of high voltage rating requirements, the power density and efficiency of the traditional MV converters are far lower than the counterparts with low voltage but similar power ratings. Due to the high operating voltage and safety concerns, galvanic isolation is usually required. Therefore, the isolated DC/DC converters with medium frequency transformers are selected as the

topology, which mainly falls into two categories, i.e., dual-active-bridge (DAB) based, and resonant converters.

The DAB converter usually is composed of two bridges on both primary and secondary sides, with a transformer between both sides, and a series connected with a inductor. The primary and secondary bridges output two voltage waveforms having phase shift to each other, and the power flow is determined by the phase shift. The series resonant converter utilizes the LC resonant tank connected with the transformer. By resonating between the series inductor or the leakage inductance, and the capacitor, a sinusoidal current waveform can be formed, and thanks to the series resonance, the voltage gain between the input and output DC links can be determined by the switching frequency. In some cases, in order to have a wider operation range or bidirectional operation, different resonant tanks, such as LLC, $CLLC$, etc., can be used between the two bridges, to extend the operational range of the resonant converter.

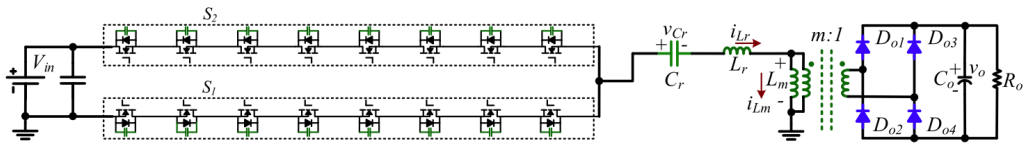
For the power devices, high voltage IGBTs or IGCTs, etc., have to be used in the MV converters so that the single or series connected devices can undertake the required high DC-link voltage in two-level topologies. Using single devices to undertake the whole MV is similar to the way in low voltage ordinary DC/DC converters, except that the voltage ratings and insulation become a more vital consideration.

However, if the voltage requirement is too high, which is unviable by using single device to undertake, another way has to be taken. By connecting devices in series in

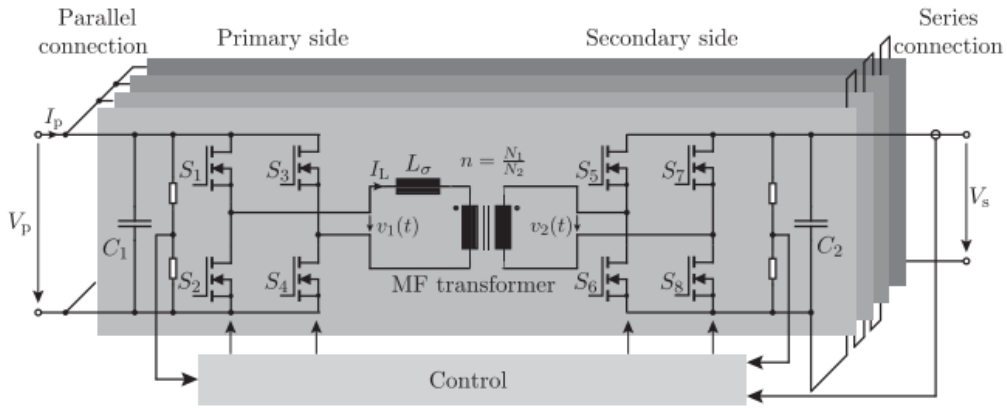
each switching position, a higher operating voltage can be achieved. In **Fig. 1.4(a)**, a MV series resonant converter with cascaded IGBTs in each switching position is shown [5]. With careful analysis, the series connected 8 MOSFETs can switch synchronously up to 15 kHz with the total DC-link voltage of 5 kV. With this method, the synchronization of devices becomes a big concern, in which both the deviation of devices themselves and gate drives require special care.

Another way to withstand high DC-link voltage is to adopt the method of modularity [59, 60], so that the voltage across on each stage is low. Therefore, several modular topologies can be derived from the conventional two-level DC/DC converters, e.g., multilevel converters, series/parallel modular converters, modular multilevel DC/DC converters. In **Fig. 1.4(b)**, an input-parallel-output-series (IPOS) converter is shown, with four secondary DC-links connected in series, the output voltage of 2.8 kV can be realized [6]. In **Fig. 1.4(c)**, a submodule-based multilevel converter topology has been implemented with a MV transformer, forming a modular multilevel DC/DC converter, so that the power transfer can be realized with the voltage ratings of 1 kV/5 kV, and power rating of 1 MW [7]. These modified topologies transferred the stress of high voltage of the power conversion system into the lower voltage ratings of the power modules, lessening the difficulties of high voltage power conversion.

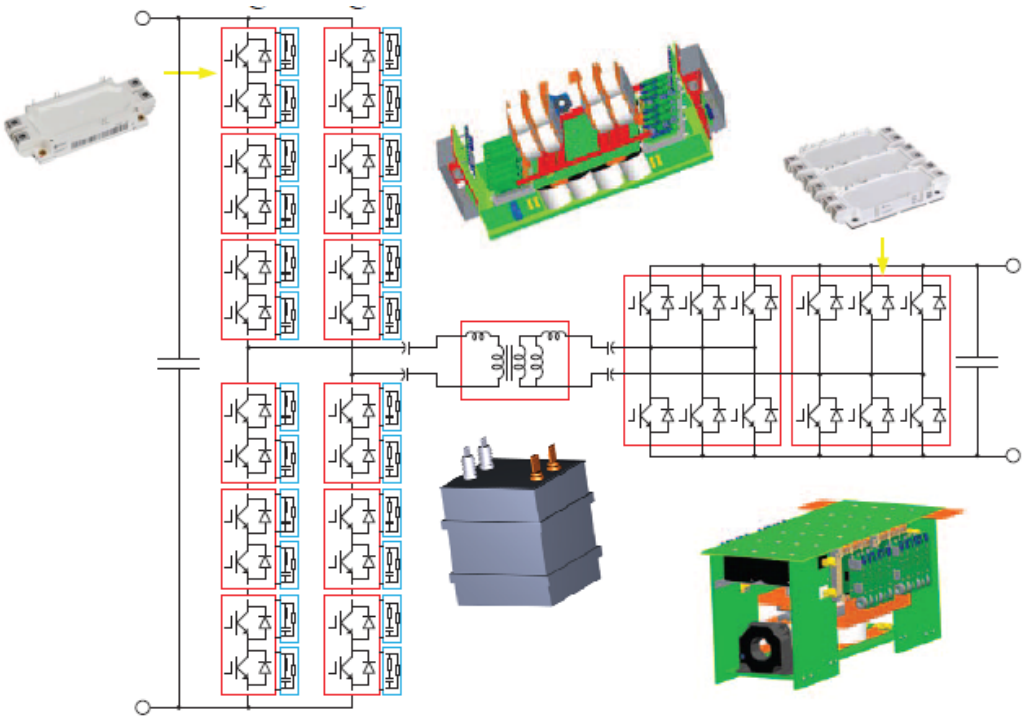
As progress has been made on the Wide-Bandgap devices, higher and higher MV devices, especially MV SiC MOSFETs, are available, enabling MV power electronic converters. Wolfspeed has developed single SiC MOSFET die with the ratings of 10 kV and 15 A , as well as power modules up to 10 kV, 240 A [8, 9], which are



(a)



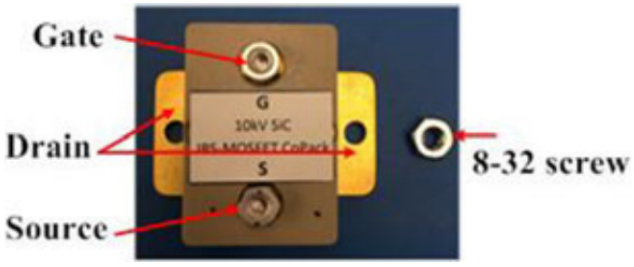
(b)



(c)

Fig. 1.4: Topology of the MV (a) series resonant converter with series connected devices [5], (b) input-parallel-output-series (IPOS) modular converter [6], and (c) modular multilevel DC/DC converter [7].

shown in **Fig. 1.5**. Thanks to the nature of higher critical electric field strength and lower specific on-state resistance, the emerging MV SiC devices possess a higher blocking voltage, lower parasitic capacitances and channel resistances, enabling the single stage converter to have a higher operating voltage, higher switching frequency and higher power efficiency. In [61], a 10-kV SiC-based 25-kW *LLC* converter has been built switching at 48 kHz. With the high switching frequency, the ferrite core transformer can be used to have a high efficiency, achieving 99% power efficiency and 3.8 kW/L power density. In [62], a two-level three-phase DAB converter with the voltage ratings of 7.2 kV/800 V has been realized with 10 kV SiC module.



(a)



(b)

Fig. 1.5: Photographs of 10 kV SiC (a) discrete MOSFET [8], and (b) power module XHV-6 [9].

In [63], a three-phase three-level DAB converter has been implemented between 22-kV DC bus and 800-V low voltage DC bus in a 15-kV SiC IGBT-based substation. With the emerging MV SiC devices, the less power stages are needed while the switching frequency can be further increased, improving both the power density and efficiency of the MV DC/DC converters. With the higher operating voltage and frequency, the challenges on the transformer inside the MV DC/DC converter is becoming more of a concern.

1.2.1 MV Medium Frequency Transformers

Along with the technical progress on MV SiC devices and its applications, the medium frequency MV transformers are also under development. Due to the high voltage requirement, the insulation performances of these transformers have to be carefully considered, which also affects the power density and efficiency of the transformers. To improve the performance of the transformer, efforts have been made on analyzing and designing insulation, thermal, magnetics.

In order to fulfill the insulation requirement, the dielectric materials and the electric field of the medium frequency transformers need to be considered and analyzed. In [64], the *LLC* transformers of a shunting locomotive is immersed in oil, which also serves as the coolant to cool the transformer. Insulating oil is usually used in low frequency utility transformers because of its low cost, but it may raise environmental concerns. In [61, 12, 11, 65], solid epoxy and silicone elastomer resins are utilized as the main insulation material. The epoxy has a higher thermal

conductivity, but a higher viscosity and higher dielectric loss, making it less reliable in high frequency and lab prototype applications, while silicone has less viscosity and dielectric loss tangent, which prevents potential thermal run-away or partial discharge [66]. When using dry type resin as the insulator, electric field in the air space may also be analyzed, as air has a lower dielectric constant comparing with silicone or epoxy, so the electric field may distribute into air and cause arc or corona discharge, enlarging the overall size of the transformer. To constrain the field within the insulating solid material, conductive shielding may be added on the surface of the solid MV winding [66, 12]. If the transformer turns ratio coincides with 1:1, coaxial cables can be used, so that the inner copper wire and outer shielding layer can be used as the primary and secondary windings, and the insulating material of the cable becomes the main dielectric material [13, 67–69]. However, by using the coaxial cable as the windings, the leakage inductance is impossible to be changed. Ref. [10] uses air as the dielectric material, in order to have a better thermal performance for a rated power flow of 200 kW. With air being the insulator, environmental parameters, such as elevation, humidity, and the placement of windings have to be considered, which constraints its application. Different insulation strategies have been shown in **Fig. 1.6**.

Since insulation material is used, a considerable space of the transformer has to be occupied by the insulation material, the size of the copper winding and core becomes more of a stringent concern than the those of the low voltage counterparts. Therefore, the core materials having high efficiency and high saturating flux density are preferable. In [12, 65], thanks to the high operational frequency (48∼300 kHz),

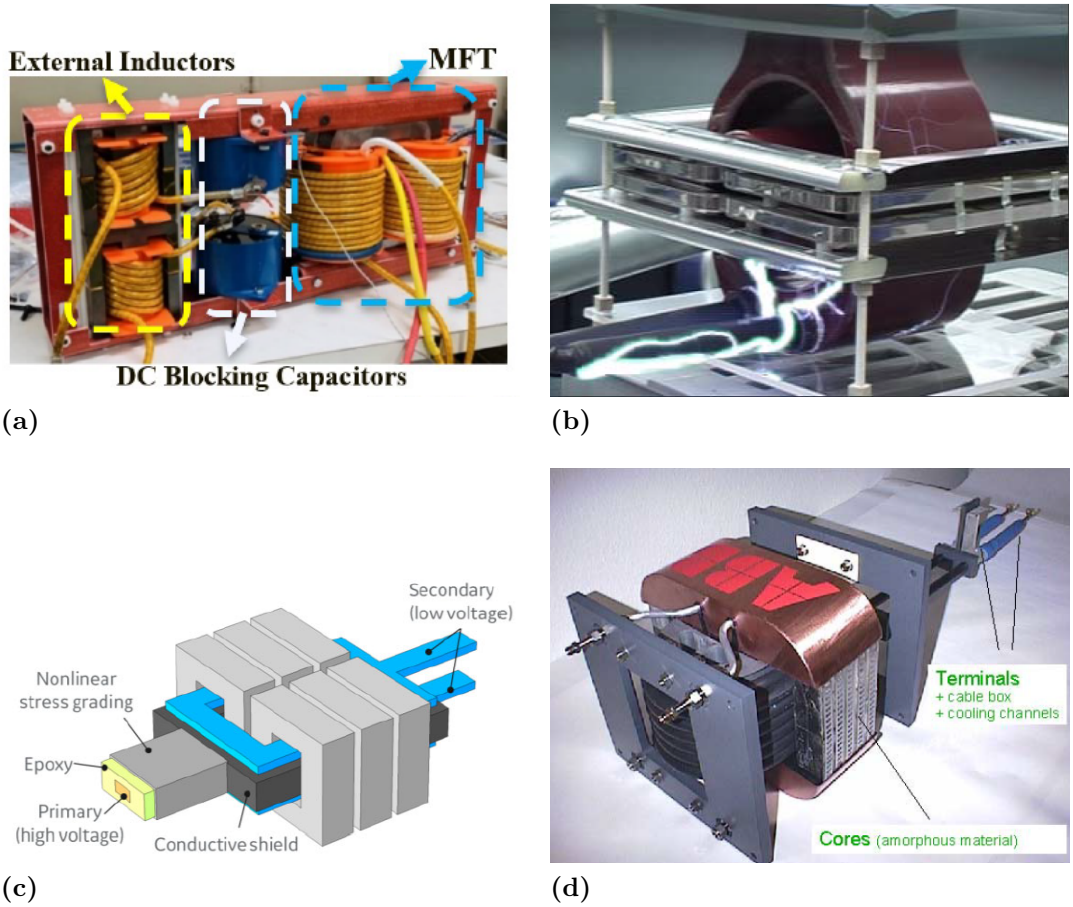
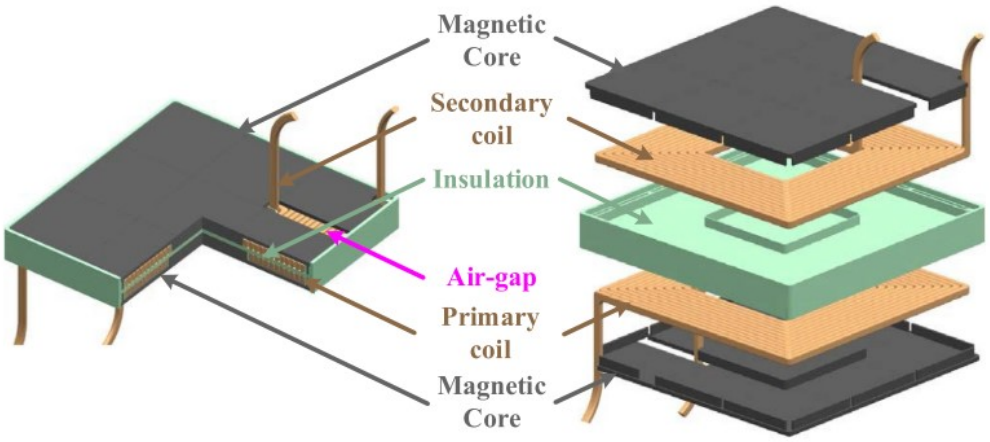


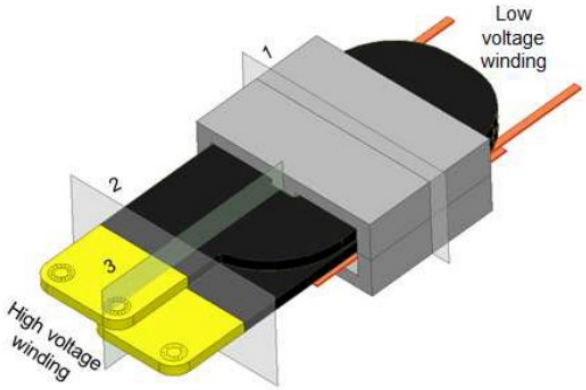
Fig. 1.6: MV medium frequency transformers with the dielectric materials of (a) air [10], (b) epoxy without shielding [11], (c) epoxy and silicone with shielding [12], (d) coaxial cable [13].

the ferrite can be used efficiently as the core material, which has the lowest loss in that frequency range among all other magnetic materials. In the larger power rating converters, because of the high switching current as well as lower switching speed of the devices with larger ratings, the switching frequency has to be reduced, in which range the nanocrystalline has the lowest loss and higher saturation flux density [70], so that a larger peak flux density can be used to save the space on windings and core [69, 10].

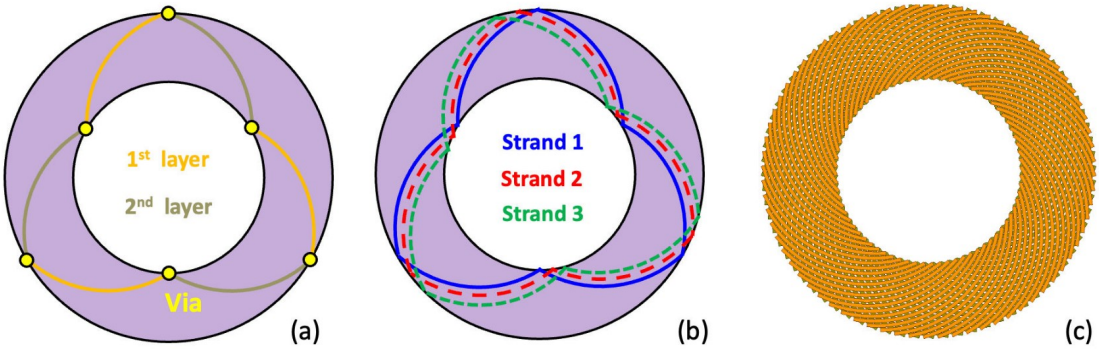
Recently, more thrust has been created to improve the power density and loss of the transformer. The concept of planar magnetics for low voltage power supplies has also been leveraged into the field. Ref. [14] proposed a planar transformer similar to wire-less charging coils, with ferrite core built by ferrite plates acting as the magnetic shielding. As illustrated in **Fig. 1.7(a)** only the epoxy dielectric barrier, instead of any magnetic pillars, is placed between the two coil windings. Therefore, an 'air' gap is created for both the insulation barrier and magnetic core, and the halves of the core can be placed as close as possible to the windings to save the insulation space, but the operating has to be high enough to cope with the limited magnetizing inductance. Thanks to the insulation material capability of print circuit board (PCB), PCB windings can also be used for MV transformers, [15, 71] used customized PCB windings as the MV winding, and the PCB substrate material and layer thickness and clearance can be customized (see **Fig. 1.7(b)**). Furthermore, to reduce the winding loss of the PCB winding, a Litz wire structure for PCB winding has also been proposed in [72, 16]. As can be seen in **Fig. 1.7(c)**, smaller PCB traces can



(a)



(b)



(c)

Fig. 1.7: Planar MV medium frequency transformers: (a) leveraged concept from wire-less charging coils [14], (b) using PCB winding [15], (c) PCB Litz wire structure [16].

serve as different strands, and then combined into different turns, forming the transformer windings. From the examples, the switching frequency is still required to be high enough to fit the planar transformer core and limited winding space. The limitation still occurs when implementing with MV SiC devices.

1.3 Design Challenges of MV DC/DC Converters

Although many MV DC/DC converters have been designed and implemented, there are still some challenges to be tackled to improve the performance and reliability of the MV DC/DC converters. There are mainly four challenges discussed here and will be further discussed in the Dissertation.

1.3.1 Insulation

First, as suggested in the name, MV DC/DC converters possess inherently high voltage rating and requirement on insulation. As shown in the past, several solutions of insulation for the MV DC/DC transformer have been discussed in the literature, such as air gap, oil immersion, and dry-type insulation. However, air- and oil-insulated transformers sometimes are undesirable, because the insulation capability of air is low and always determined by atmosphere pressure and humidity, and insulation oil could be environmental unfriendly and sometimes inflammable. However, the dry-type insulation design and implementation are also very critical for reliable operation. Several aspects of the design process and manufacturing quality affect the dry-type

insulation, including insulation clearance, winding structure, type of mechanical and insulating materials, vacuum potting setup, as well as shielding configuration. **Fig. 1.8** shows an insulation failed MV transformer winding, in which voids were formed in the epoxy encapsulation, and with high voltage stress partial discharge (PD) heated the surrounding epoxy and glass transited or cracked the solid material and finally caused insulation break down.

As the potential of power stage components are also elevated, the insulation consideration is also critical on power stages. Unlike the MV winding insulation, the MV power stage insulation design is more correlated to the thermal design. With



Fig. 1.8: Dry-type MV winding insulation failure.

air-cooled power stages, heat-sinks are involved with both air path for convection and high potential connected to the MV devices. **Fig. 1.9** shows electric discharge between two heat sinks with high voltage. Therefore, unlike in the MV winding design that encapsulation helps, insulation structure of MV power stages also needs careful discussion.

1.3.2 Leakage Integration

For DC/DC converters, the resonant tank is critical for power conversion and zero-voltage switching (ZVS) operation. The series inductance in the resonant tank is also needed as an unalienable component for resonant or DAB converters. Due to bulky insulation is demanded for the MV windings, it is desirable to reduce the size of the magnetics to achieve high power density. **Fig. 1.6(a)** shows a MV transformer with rated power at 100 kW and power density of 15 kW/L, yet it still

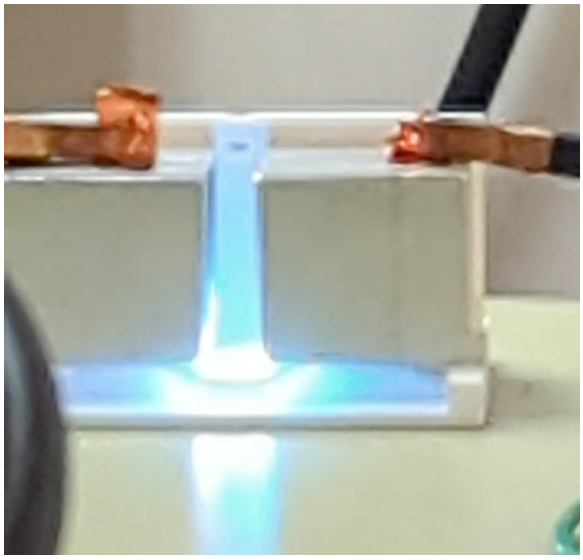


Fig. 1.9: MV heat sink insulation failure.

needs considerable space for series inductance and DC-blocking capacitors. If the inductance were integrated into the transformer, no more extra space is needed for external inductors. In that case, the leakage inductance can serve as part of the resonant tank, and hence the insulation for an extra MV inductor can be saved.

However, as aforementioned, it is beneficial for MV converters to use nanocrystalline cores thanks to its operating frequency and requirement on energy density. The leakage magnetic field induced by the leakage inductance can form eddy current on the outer surface of ribbon-based transformer cores, such as amorphous and nanocrystalline magnetic cores. As by definition the leakage field is the type of magnetic field that not always confined in the transformer core, and having orthogonal component to the lamination field somewhere in its flux line. Therefore, eddy current of the leakage inductance cannot be successfully suppressed by the thickness of lamination. Eventually a high eddy current can be formed on the outer surface of the laminated core (see **Fig. 1.10**) and cause considerable amount of conduction loss and heat. **Fig. 1.11** shows the temperature measurement of a core-type transformer with both magnetizing and leakage test. From the thermal images, it can be seen that the hot spot generated by the leakage is even higher than the magnetizing case, and loss could be doubled with unmanaged eddy current loss due to leakage [18].

This eddy current loss issue induced by leakage inductance has been less known as leakage integration for ribbon-based cores was uncommonly used for MV DC/DC converters. Several shielding methods have been proposed but the effectiveness is

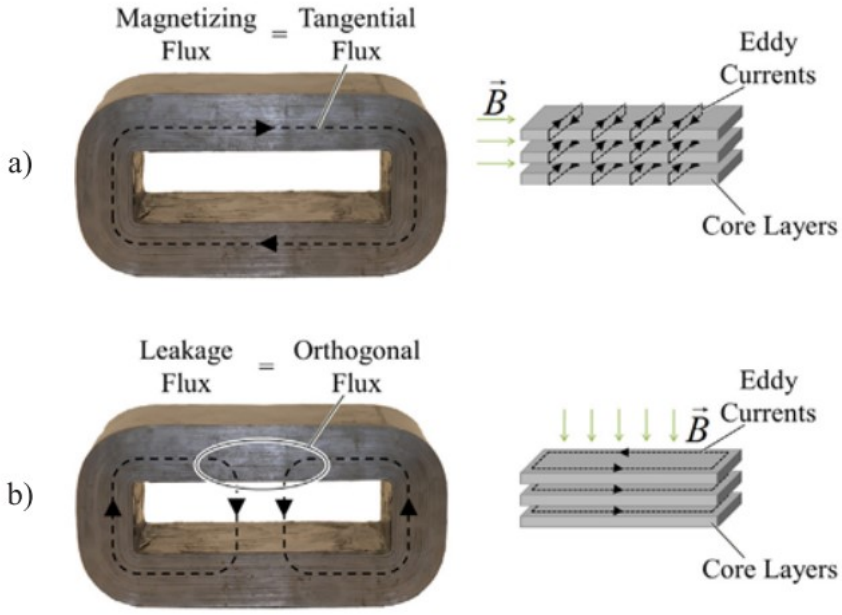
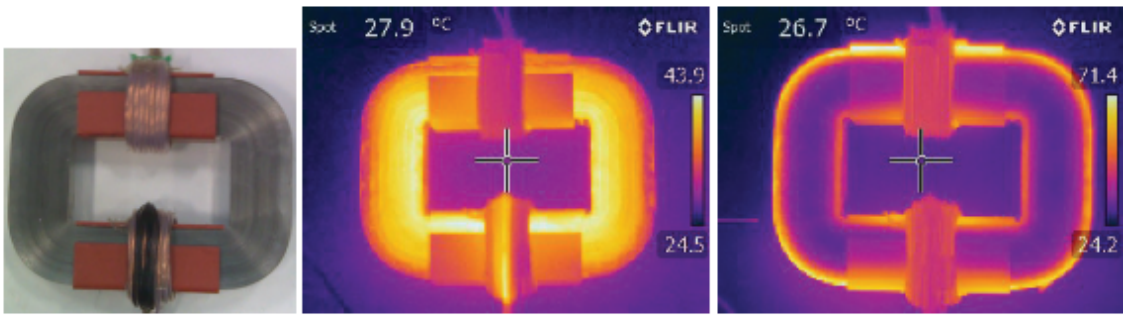


Fig. 1.10: Ribbon core orthogonal flux can induce eddy current [17].



(a) Transformer (b) Magnetizing Thermal (c) Leakage Thermal

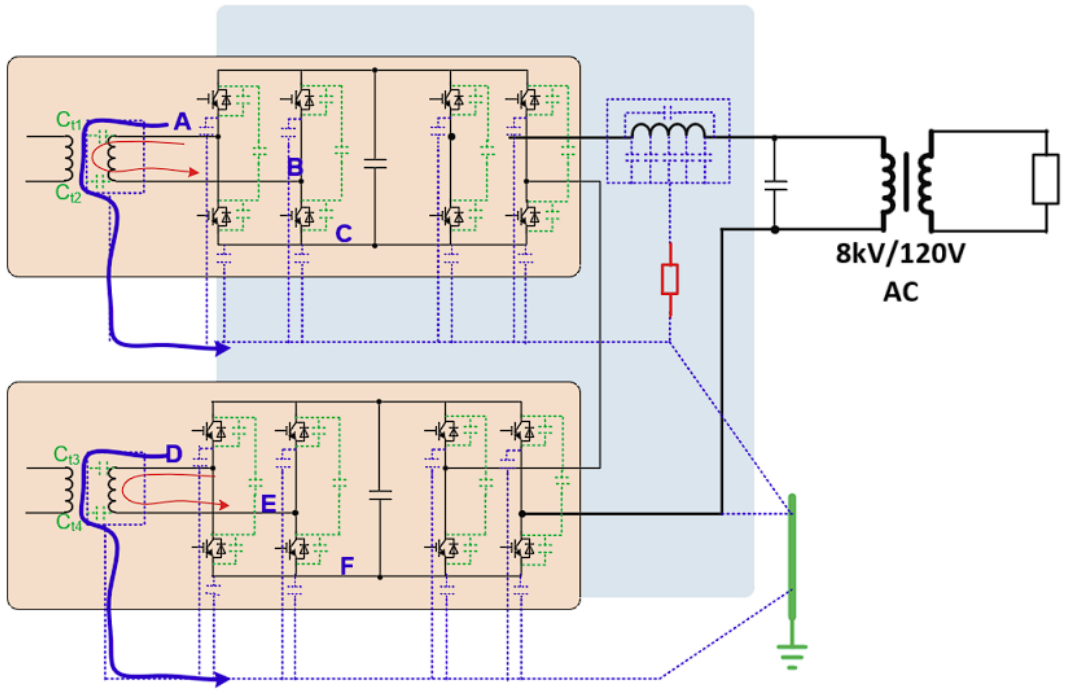
Fig. 1.11: Transformer test with leakage induced eddy current [18].

limited. And in power transformers, even with minimized leakage it may still be considerable with energy leak or EMI [73–75]. Hence, discussion on the strategy to have loss-less integration configuration is needed.

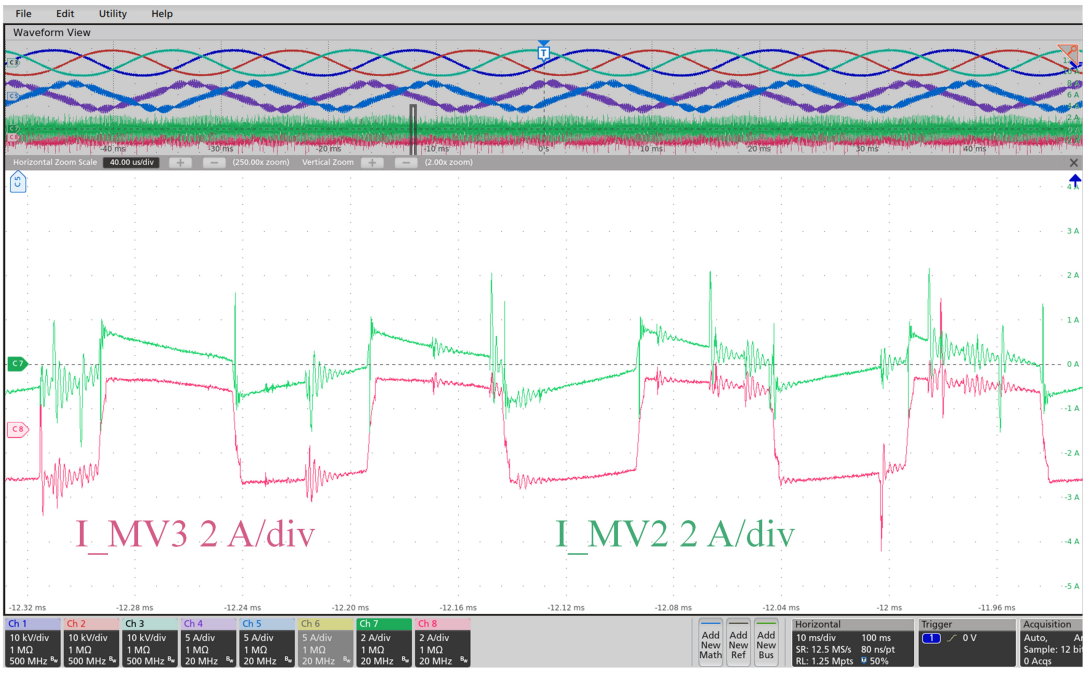
1.3.3 Parasitics Capacitance Induced Loss

Another less known issue for MV converters is that the parasitic capacitances can induce high switching loss for the converters [76]. Apart from the output capacitances of MV power devices, the parasitic capacitances of MV windings can also contribute to device switching losses during hard switching. **Fig. 1.12(a)** shows that the transformer parasitics can be in the loop when cascaded H-bridge (CHB) converter switching, causing extra switching loss for that DC/AC converters. In the meanwhile, it can also be seen from the transformer current waveform as in **Fig. 1.12(b)**. Even though the transformer is not switching, the parasitic capacitance charging and discharging current flows through the transformer winding from the devices and to the parasitics dielectric volume.

To tackle this problem, a PWM strategy was proposed for the CHB converter to reduce the equivalent switching frequency that can be seen from the parasitic capacitance [31]. However, this modified modulation also causes complicated modulation implementation and also switching unbalance of losses due to asymmetric switching events in the CHB switching devices. Therefore, more analysis and better technical methods are needed to solve this issue.



(a)



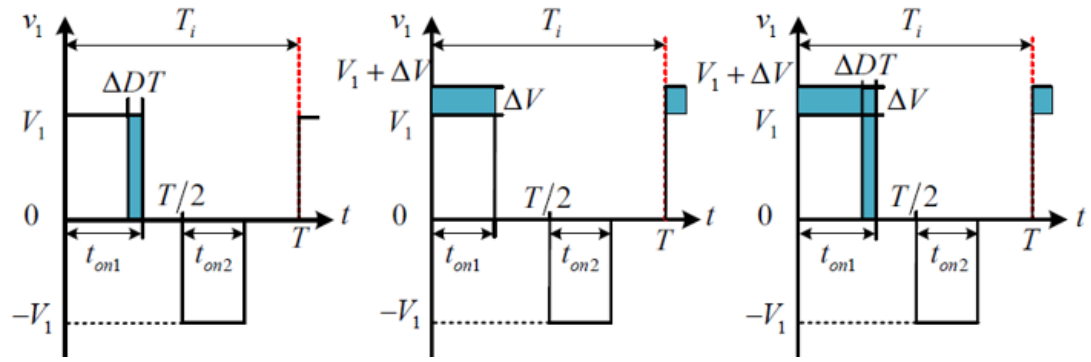
(b)

Fig. 1.12: MV converter with (a) switching loop including parasitics [3], (b) current spikes induced by common-mode current induced by parasitics [19, 20].

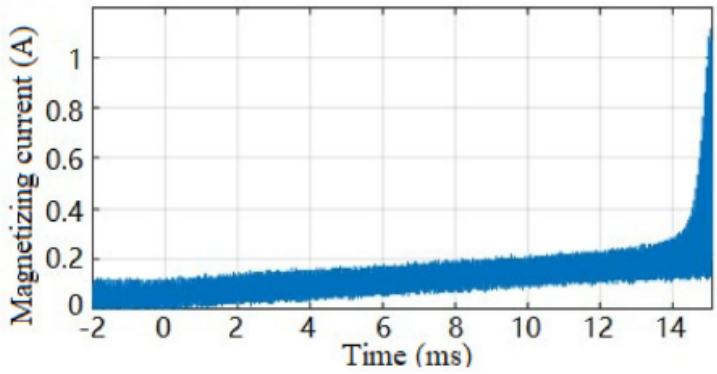
1.3.4 Transformer Saturation

As in MV DC/DC converters, the voltage rating is high while the switching frequency is moderately low, causing the energy requirement of the transformer core to be critical. Hence, a trade-off between the transformer size and the design margin has always occurred during the design process. Although the safe operation area must always be secured, a higher operating flux density is always desired to achieve a higher power density. As the flux density increases, the operating margin of the core shrinks, and the saturation of the transformer may become an issue. Due to voltage and device switching mismatch, the volt-second unbalance can be induced to the DC/DC transformer, which is shown in **Fig. 1.13(a)**, and as the low-frequency mismatch accumulates through time, DC bias can be formed in the transformer winding, causing the flux to be unbalanced and floated from the zero point. Shown in **Fig. 1.13(b)**, the unbalance of flux offsets the transformer core operating point and caused the transformer core to be unilaterally saturated. With a few milliseconds, the transformer current got higher as the saturation reduced the transformer's magnetizing current, and finally current runaway happens and the whole converter system runs into overcurrent fault.

In the literature, several solutions have been presented for the detection and control of low-voltage converters. However, these challenges become more pronounced in MV converters. On the one hand, the high voltage rating makes magnetizing current measurement difficult due to either high insulation requirements or a complex



(a)



(b)

Fig. 1.13: Transformer unbalance with (a) switching loop including parasitics [21], (b) current spikes induced by common-mode current induced by parasitics [22].

winding ratio; on the other hand, high switching noise and interference in the converter can further complicate the accurate measurement of flux unbalance [77, 78]. In particular, DC component detection in the magnetizing current relies on measuring the primary and secondary voltages of the transformer, but this method is highly dependent on the accuracy and noise level of the current sensor. Excessive offset or high noise levels may obscure the DC component, making detection and control

challenging. For a 6.7-kV, 16.7-kW DAB converter transformer, considering high-voltage insulation requirements, a through-hole current sensor combined with silicone-insulated conductors is used. Among commercially available sensors, the *LEM HO-6P* is the lowest rated and most suitable option. The output waveform of *HO-6P*, as shown in the **Fig. 1.14**, indicates a noise level of approximately 10 mV, while the FFT analysis reveals that the main noise components are concentrated in the low-frequency range, with noise levels increasing as frequency decreases. If this sensor is applied directly to DC detection, with its sensitivity of 100 mV/A, any DC components below 0.1 A (4% of the full-load current) cannot be accurately detected due to noise interference. These challenges highlight the need for further discussion on detection techniques and implementation strategies for transformer unbalance detection and control in MV converters.

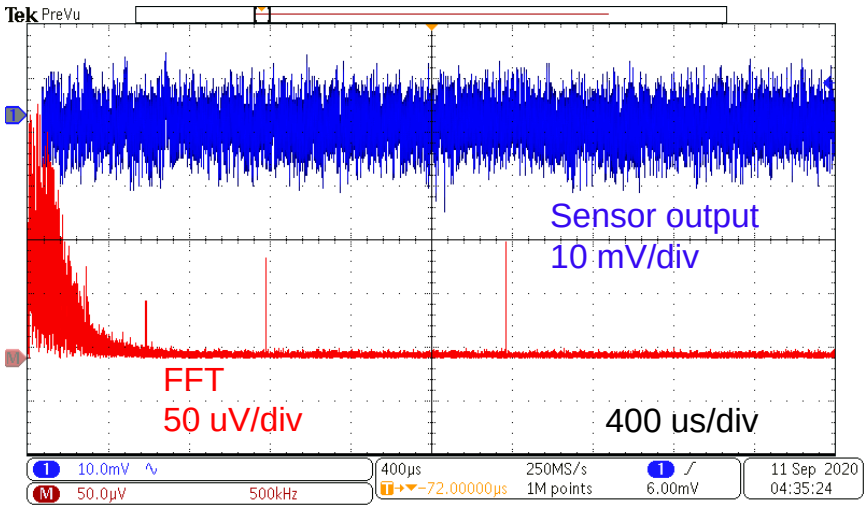


Fig. 1.14: Noise waveform and FFT of the current sensor *HO-6P*.

1.4 Dissertation Outline

In this Dissertation, the solutions to challenges of magnetics and insulation design for MV DC/DC converters are discussed. The content of the remainder of this dissertation is listed as follows.

Chapter 2 discusses the low-loss transformer leakage integration with 2-D lamination configuration. In this chapter, the mechanism leakage induced eddy current loss is discussed with modeling and simulation analysis. Then, a 2-dimensional lamination concept is introduced to suppress the eddy current loss. A low-loss leakage integration structure with ferrite bridge is also proposed. Test validation is also provided to verify the proposed method.

In **Chapter 3**, following Chapter 2, a new ferrite shielding method is proposed to further reduce the eddy current. The ferrite shielding structure is firstly proposed, and the principle of is demonstrated and explained. The effectiveness for implementation is also discussed, along with test results among different cases, namely gapped inductors, core-type transformers, and shell-type transformers. Performance comparison with existing method is also demonstrated.

Chapter 4 discusses dry-type winding insulation. The materials used in the dry-type insulation is characterized at first, followed by an introduction to the configuration of MV windings. The partial shielding with reduced parasitics, as well as electric field grading techniques will be proposed. A simplified vacuum encapsulation process is also provided.

Then, **Chapter 5** introduces a diode-clamped grounding configuration for MV DC/DC transformers to reduce common-mode parasitic capacitance induced switching losses. First, the mechanism of the generation of extra switching loss related to the parasitics is analyzed, after which the diode clamping circuit is proposed and analyzed for the proposed grounding circuit. Experimental test has also been performed to validate the proposed method, and the impact factors, including parasitic loop impedance and gate driving delays are provided.

Chapter 6 proposed a field shaping strategy for MV power stage designs to achieve high power density. In this chapter, the insulation structure of the MV power stage, including heat sink field shaping and air duct design are provided, with simulation and experimental test validation. A MV power stage design using commercial gate drive solution and minimized power loop are also discussed.

Chapter 7 is the chapter on MV DAB transformer flux balancing. A ferrite-gap-based transformer structure is introduced to create current harmonics for flux unbalance detection. Then, the modeling, implementation and validation of magnetizing current harmonic-based flux balancing will be elaborated. The detection and control techniques are also implemented in DAB converter systems for verification.

Finally, **Chapter 8** summarizes and concludes the technical contributions and listed potential future work to further improve the proposed and discussed techniques.

Chapter 2

Low-Loss MV Transformer Leakage Integration With 2D Lamination

2.1 Literature Review

For dual-active-bridge converters, the transmitting power is determined by the phase-shift and the series inductance between the two bridges.

$$P = \frac{nV_1V_2}{2f_sL}D(1-D) \tag{2.1}$$

Where D is the phase-shift, V_1, V_2 are the dc-link voltages on both sides, n the turns ration, f_s the switching frequency, L the series inductance. Unlike the resonant converters of which the resonant frequency and voltage gain can be also adjusted by the series resonant capacitances, the DAB series inductance and phase shift determine

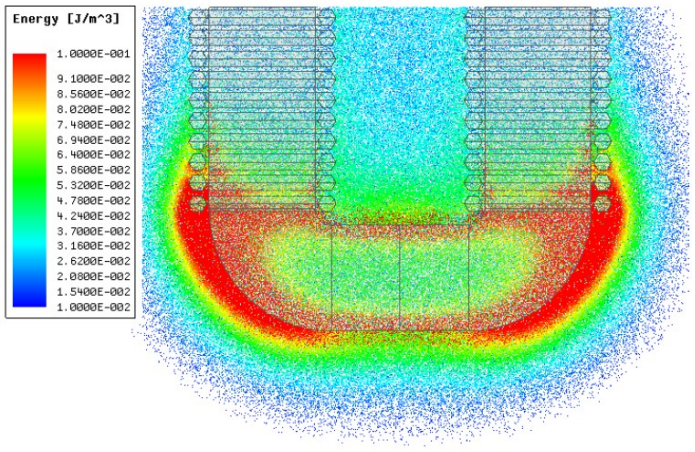
the power transferred through the converter, and the phase-shift should also have enough resolution for the control stability. In the meanwhile, the resonance process between the device output capacitances and sufficient series inductance can also achieve zero-voltage-switching (ZVS) for both sides. Hence, the series inductance for DAB converters should be sufficient for both stable power conversion and realizing ZVS to reduce switching losses. It should also be noted that the series inductance may also need MV insulation for MV DC/DC converters, which have an impact the volume and power density of the converter design, and hence may need to be integrated into the transformer.

Through the literature, many methods to estimate and integrate the series inductance into the transformer by utilizing the leakage inductance have been proposed. Many analytical models have been proposed by people to estimate the leakage inductance for different types of transformers [79]. However, most of them discussed based on the shell type transformers, which have low leakage inductance. Some methods of leakage integration for ferrite-based transformers have been introduced, such as different winding placement [80], and by adding shunt paths inside the core windows [81], whereas the winding placement may not have a significantly large enough change for MV DAB transformers, while adding shunt paths may introduce high eddy current loss due to the core lamination. Many of them focuses on ferrite-based transformer cores, whereas in nanocrystalline transformer different effect may be found.

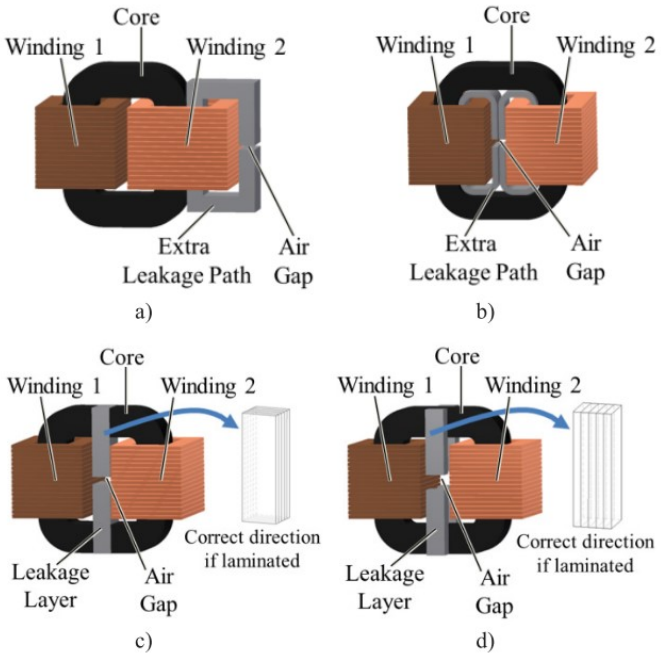
An important effect on nanocrystalline tape-wounded transformer is the eddy current on the lamination layers. As the lamination is mainly for eliminating eddy current component in the conventional magnetizing loop to reduce the core loss, it may not work on the leakage loop and may cause high eddy current loss [17], as the leakage flux always find a way different from the magnetizing loop, and hence may cross the lamination layer and cause high eddy current loss (see **Fig. 2.1(a)**).

Fig. 2.2 shows a thermal image during short circuit test of a core-type 850-V/6700-V 16.7-kW MV transformer, in which the low voltage (LV) and MV windings are placed on different core legs to have a leakage inductance of 250 µH on LV side, and the temperature distribution of the core is strongly uneven. Most of the heat has been concentrated on the outer surface of the core, where the eddy current is mainly concentrated. Similar phenomena have also been found in [18] and [17].

To tackle this issue, [18] introduced a ferrite shielding method to bypass the leakage flux so that the eddy current may not be generated in the lamination, but the effect is limited by test verification. For the transformer in **Fig. 2.2**, after the ferrite shielding shown in [18] added on the outer side of the transformer core, 105 W of eddy current loss was still estimated, accounting for 56% of the transformer loss. Core type transformers can have high leakage inductance, and some of the leakage can be made further by central legs [17] (see **Fig. 2.1(b)**), and the adapted leakage layers can reduce the eddy current loss to a significant low level. However, the structure of the dry-type MV winding has to be fit into the core window with limited space, and extra nanocrystalline bars have to be manufactured, making the manufacturing



(a)



(b)

Fig. 2.1: (a) Magnetic energy concentrated on the core surface [23], (b) potential leakage integration methods [17].

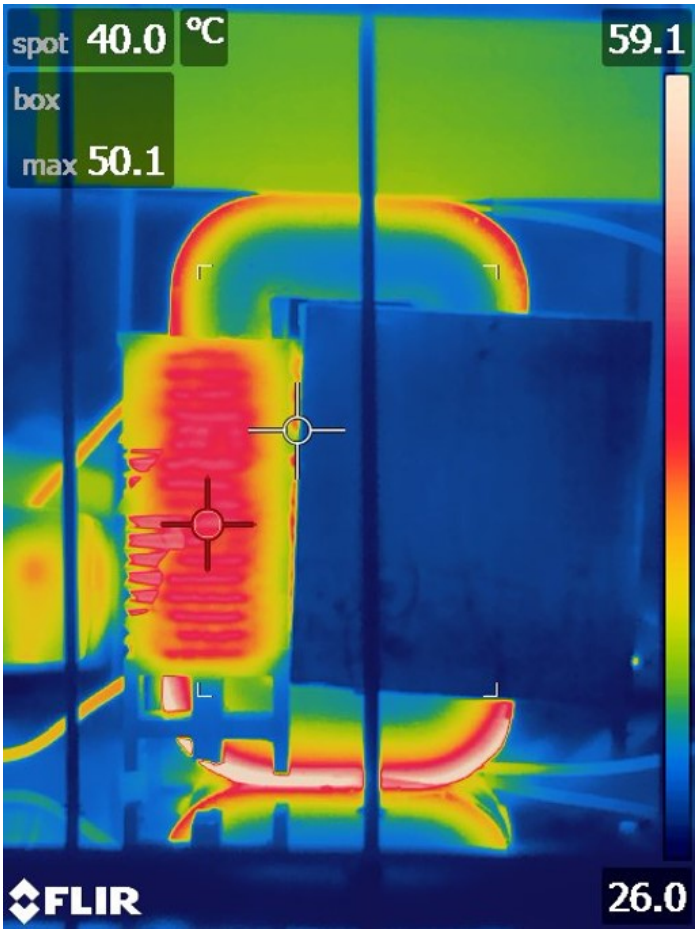


Fig. 2.2: Thermal image of a leakage integrated core-type transformer with high eddy current loss [19].

process complicated. Therefore, more careful design options may be necessary on leakage integration for nanocrystalline-based MV DC/DC transformers.

2.2 Leakage Inductance and Eddy Current Loss

To begin with, the leakage inductance of the MV transformer should be categorized as the combination of the intrinsic leakage inductance that the transformer structure itself possesses without any external structures, and the external inductance that produced by structures which are artificially added to the transformer, i.e.

$$L_l = L_i + L_e \tag{2.2}$$

Where L_l is the leakage inductance, L_i the intrinsic leakage inductance generated by the transformer structure of windings and core placement, L_e the external inductance with external magnetic structures. To find the transformer structure with low eddy current loss and high leakage integration capability, a quick simulation/test comparison can be made with different transformer structures.

To model the core lamination of the tape wounded cores, anisotropic material setting has to be used, as the lamination direction affects the permeability and resistivity [82, 24]. The model mainly uses the geometry and basic electromagnetic properties of the lamination layers and the size of the whole core, as illustrated in **Fig. 2.3**.

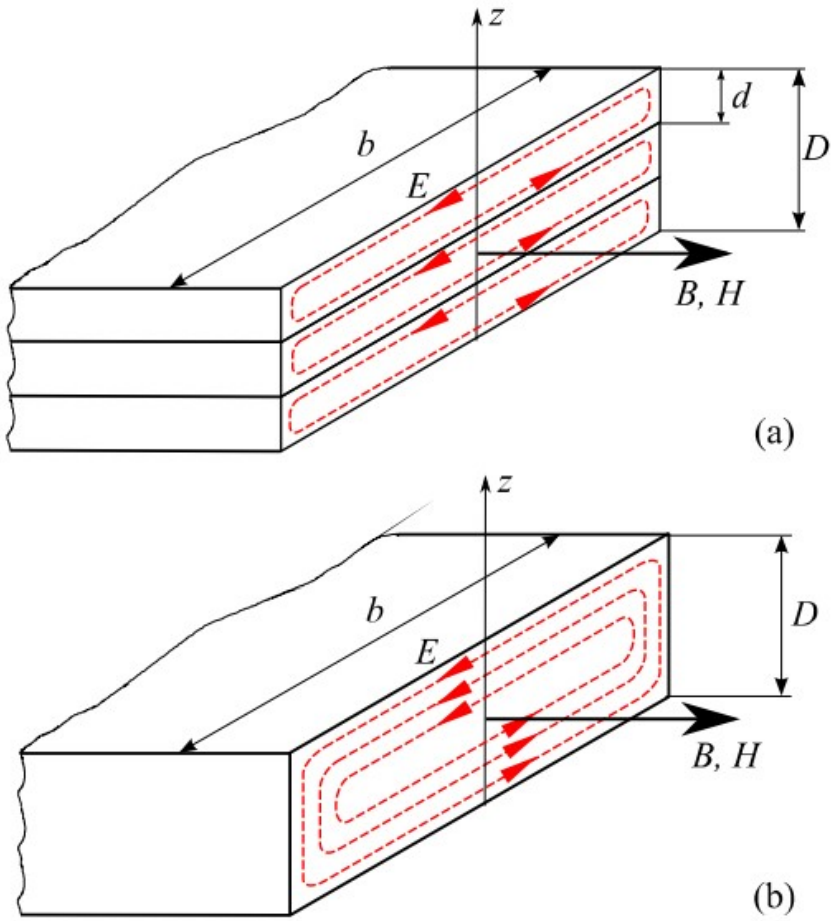


Fig. 2.3: Model of the lamination layers: (a) three of lamination layers, and (b) homogenized lamination model [24].

$$\begin{cases} \sigma_x = \sigma_y = \sigma_b \\ \\ \sigma_z = \left(\dfrac{d}{b}\right)^2 \sigma_b \end{cases} \tag{2.3}$$

$$\begin{cases} \mu_x = \mu_y = \mu_b \\ \\ \mu_z = \dfrac{1}{\dfrac{F}{\mu_b} + \dfrac{1-F}{\mu_0}} \end{cases} \tag{2.4}$$

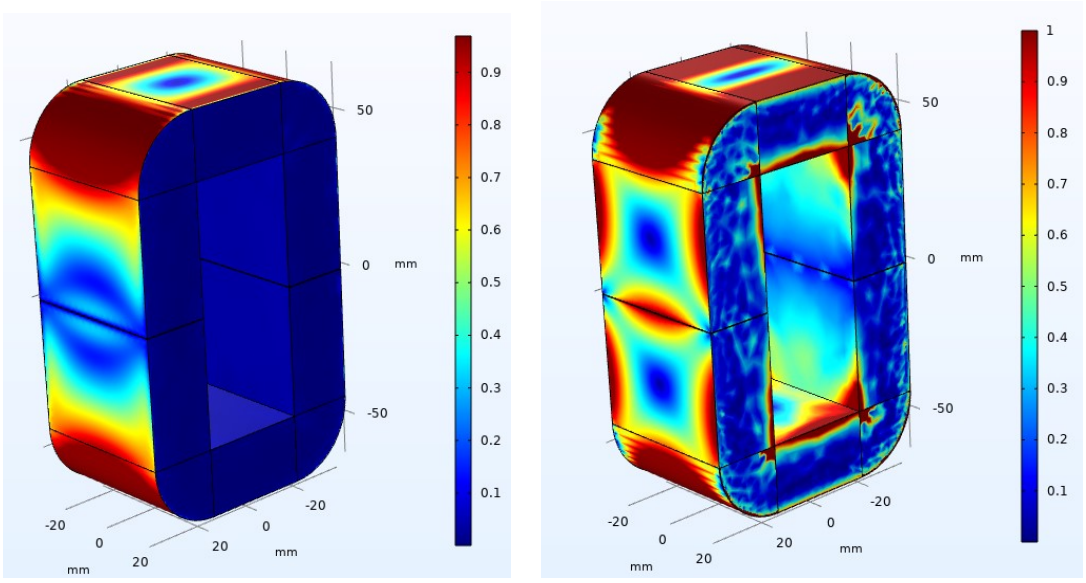
Where the x, y is the direction in parallel with the core lamination, while the z direction is the direction perpendicular to the core lamination, the conductivity, the permeability, subscript b is the isotropic solid material property.

Based on (2.3) and (2.4), the transformer core can be modeled in finite-element analysis (FEA) tools. Due to the orientation of the lamination in ribbon-based cores, the different segments, namely the legs, yokes, and rounded corners, have to be associated to different local coordinates. Then, the phenomenon shown in **Fig. 2.2** can be reproduced in the simulation. **Fig. 2.4** shows the simulation results of the core type transformer with separated MV and low voltage (LV) windings on both sides. Due to the non-linearity and core partitions for modeling different core segments, the true quantity of the loss may not be revealed, but it can qualitatively show the field and loss concentration on the tape-wounded cores, such as nanocrystalline cores. From the simulation, the significant magnetic and current field can be found on the outer surface of the transformer core. On the surface the xy plane properties in

(2.3) and (2.4) are exhibited, and hence the overall loss of the transformer leakage is significant.

2.3 Ferrite Bridge-Based Leakage Integration

From the discussion, it can be seen that the core-type transformer with two sets of windings on different legs separately has high intrinsic leakage inductance thanks to the core and winding structure itself. As the intrinsic leakage inductance is high, the leakage flux flowing along the transformer core is high, and at certain locations (top and bottom surfaces) the flux perpendicular to the core lamination is high. Hence, the leakage eddy current loss is significant. Therefore, the core-type transformer should not be desired on leakage integration.



(a) **(b)**

Fig. 2.4: Simulation results for the core-type transformer under short-circuit test (a) magnetic field distribution, and (b) eddy current density distribution.

Other possible leakage integration structures other than core-type transformers are shell-type transformers. However, the co-axial shell-type transformer is excluded, as the LV and MV winding placed together coaxial may compromise the transformer cooling and insulation and make the leakage integration complicated. As in shell type transformers, the windings can be split or interleaved to have low intrinsic leakage inductance, and hence low eddy current loss, and more leakage inductance can be integrated with ferrite structures. Therefore, a new structure can be found with low intrinsic leakage and can be externally integrated with ferrite structures. The proposed structure is shown in **Fig. 2.5**. As the LV winding is split into two set, and interleaved with the MV winding. Because the magneto motive force of interleaved windings is lower than the conventional core-type and shell type transformers, the intrinsic leakage flux should be lower compared to the core-type and conventional vertical stacked shell-type so that the eddy current should be low. However, thanks to the ferrite bridges, the high external leakage flux can be added and tuned by the air gaps. The leakage inductance can be estimated as the sum of leakage inductance for the LV windings and MV winding

$$L_l = L_{LV} + L_{MV} \tag{2.5}$$

Where, L_l is the total leakage winding, and L_{LV} is the LV side (top and bottom windings) leakage inductance, L_{MV} the MV side (center winding) leakage inductance. The two components are respectively

$$L_{LV} = N_{FB} \left(\frac{N_L V}{2} \right)^2 \mu_0 \frac{A_{FB}}{l_{gFB}} \tag{2.6}$$

Where N_{FB} is the numbers of ferrite bridges, which usually equals four as the ferrite bridges installed on each side of the core, N_{LV} is the LV winding total turns number, A_{FB} the equivalent cross-sectional area of air gaps of each ferrite bridge, l_{gFB} the air gap length for each ferrite bridge. And,

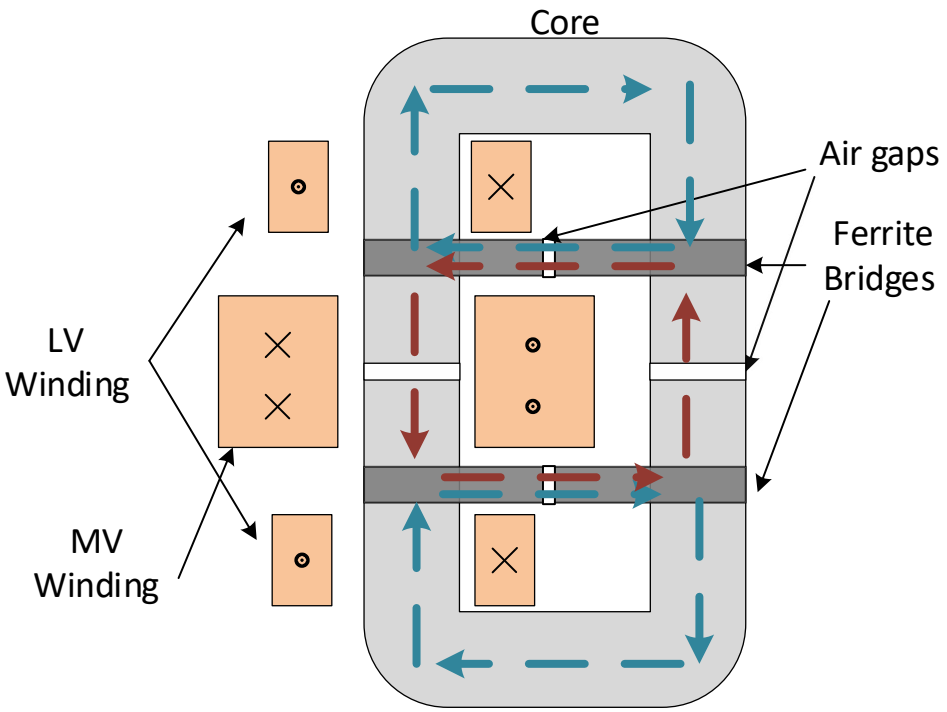


Fig. 2.5: Proposed transformer structure for leakage integration, dashed lines: leakage field flowing directions [19].

$$L_{MV} = \frac{N_{FB}}{2} \frac{N_{MV}^2 \mu_0}{\frac{2l_{gFB}}{A_{FB}} + \frac{2l_{gNC}}{A_{NC}}} \tag{2.7}$$

Where N_{MV} is the MV winding turns number, A_{NC} the cross-sectional area of the nanocrystalline transformer core and l_{gNC} the air gap length of each transformer core leg. As the leakage field flows through both nanocrystalline core and ferrite bridges twice, the total air gap length is doubled while the leakage branch number is halved compared to LV side.

With the formula (2.5) (2.6) (2.7), the leakage inductance can be estimated during the design process, and the flux density and loss in ferrite and nanocrystalline cores can be further calculated. As long as the flux density in the ferrite does not saturate, the overall loss when at short-circuit should be lower compared to the other methods.

To verify the effectiveness of different structures, quick tests have been performed to evaluate the losses and leakage inductance of different transformer types. In order to make fair comparison, the winding ratios are set to 31:31, and the leakage inductances are tuned close to 250 µH, and all tested up to 50 A peak-to-peak current. In this way, the current waveforms of different transformer types should be the same, and hence the switching and conduction losses except the eddy current losses.

In **Fig. 2.6**, the thermal images and measured total losses of the test setup are shown. The transformers are intended to transmit power up to 16.7 kW. For core type transformer, the high eddy current loss makes its performance least competitive,

while The vertical shell type transformer has less loss, and high intrinsic leakage inductance, as no external ferrite needed to achieve 250 µH. The leakage field is concentrated inside of the core window area, and the inner surface of the transformer core, also producing high eddy current losses and heat the lamination quickly. As for the interleaved winding shell type, less loss has been measured, and through the thermal image, less eddy current loss can be found on the inner side and outer side lamination surfaces. Therefore, the proposed leakage integration structure can significantly reduce the eddy current loss.

2.4 2-D Lamination

As can be seen in thermal image in **Fig. 2.6**, the shell type transformer with interleaved winding still has certain amount of eddy current loss on the inner surface of the transformer core, which may need to be further reduced. Note that the lamination reduces the eddy current loss by cutting the solid area perpendicular to the magnetic field smaller, similar strategy has also been adopted to reduce the gap losses for tape-wounded nanocrystalline cores [83, 84]. Same measure can also be taken to reduce the eddy current loss induced by the leakage inductance.

Therefore, simulation with split cut cores have been performed. Originally, the transformer core used is 50 mm in depth, and can be replaced with five thinner cores with 10 mm in depth with the state of current engineering capability, as it can be

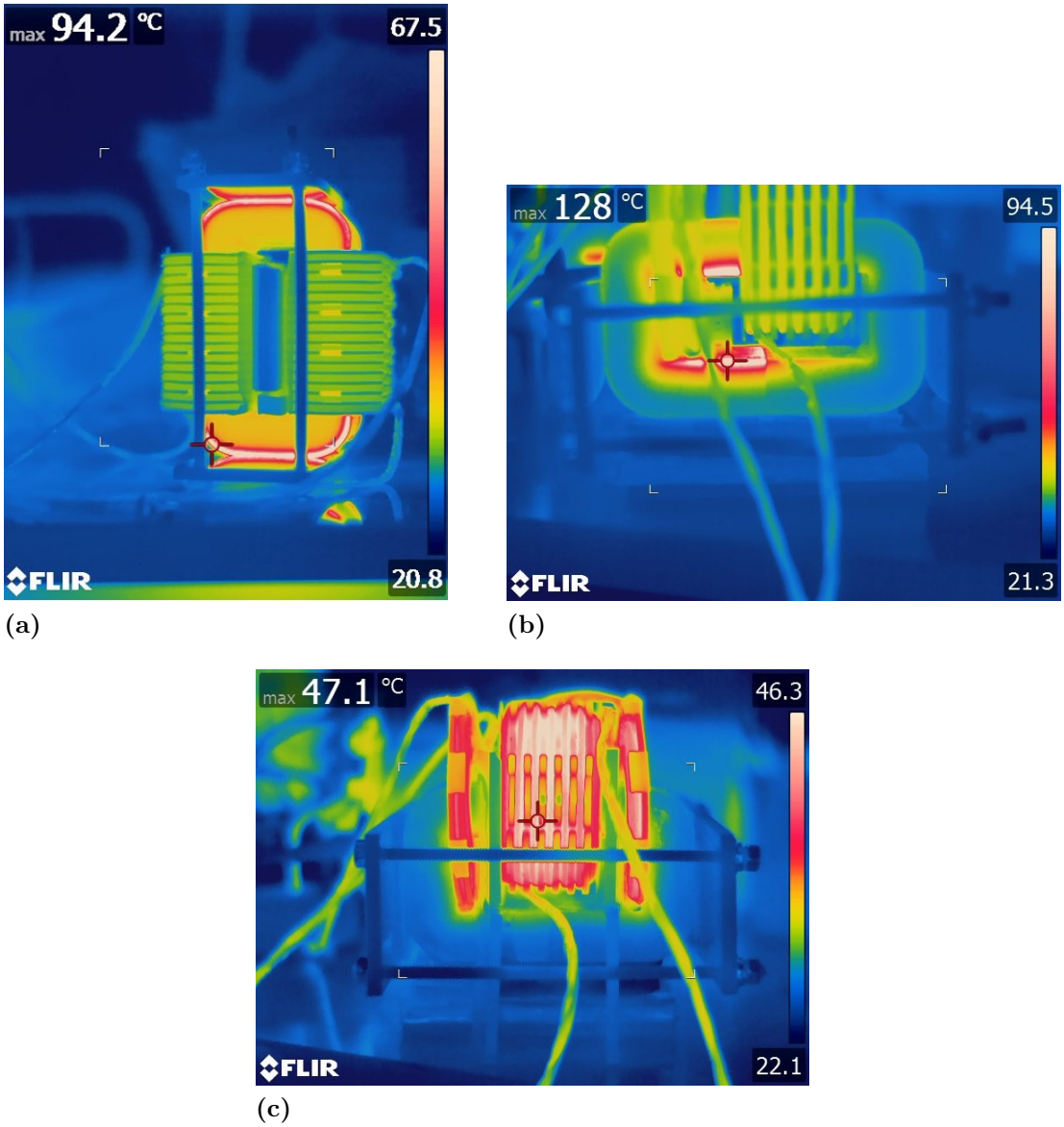
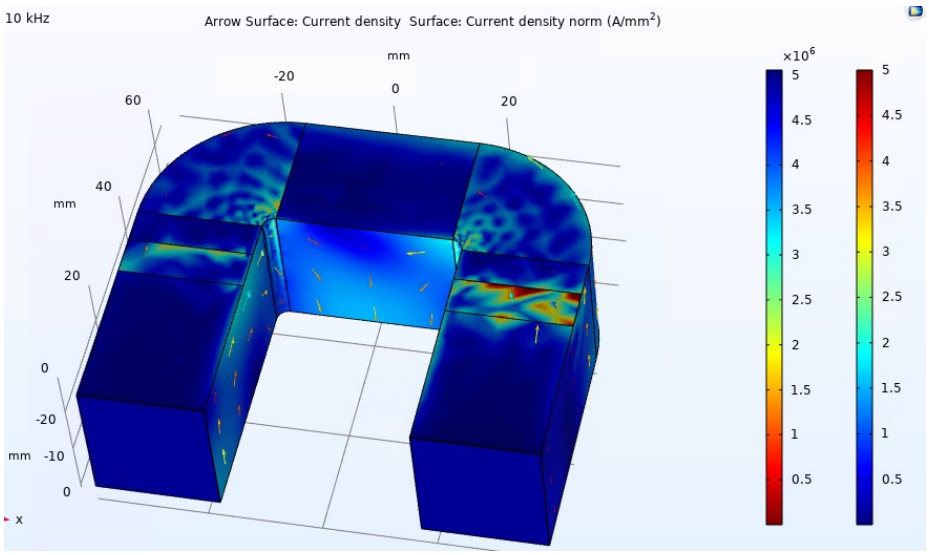


Fig. 2.6: Test results of different type of leakage integration: (a) core-type, with total loss of 425 W and estimated eddy current loss 339 W; (b) vertical shell-type, with total loss of 280 W and estimated eddy current loss 113 W; (c) vertical shell-type with interleaved winding, with total loss of 120 W and estimated eddy current loss 31 W.

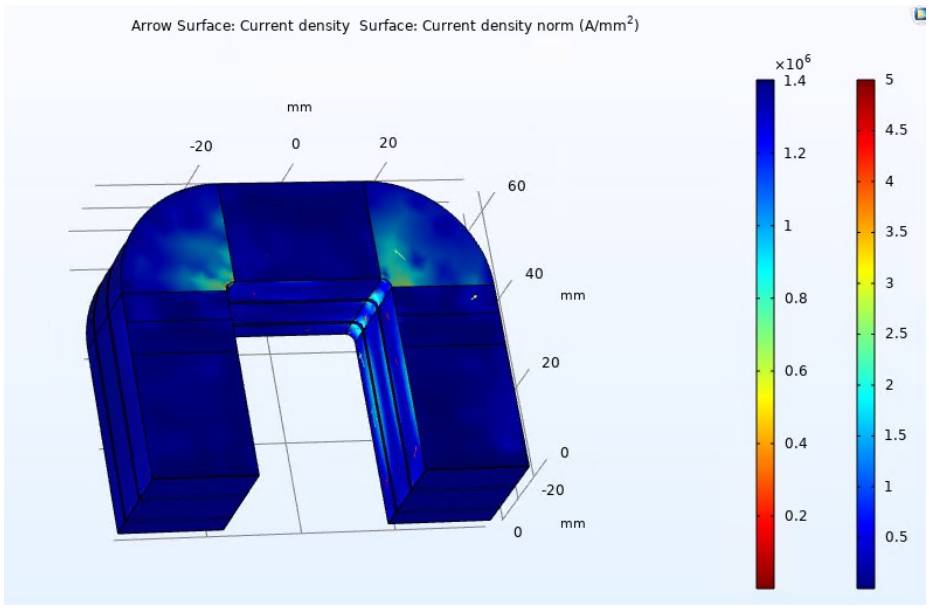
wounded easily with 10 mm wide nanocrystalline tape, which is the current available narrowest, without any cutting process.

Simulation have been performed to make the comparison and the results are shown in **Fig. 2.7**. In **Fig. 2.7(a)**, the original solid transformer core has been used with 50 mm in depth, and in the inner window surface the current density of 2 $A{\cdot}mm^{-2}$ can be found with a wide range, and the loss was measured as 28 W. For **Fig. 2.7(b)**, the cores are cut into five smaller cores (mirrored part not shown). The area having eddy current is significantly shrank, only the edge regions have some current density around 2 $A{\cdot}mm^{-2}$, and the eddy current loss is measured as 9.4 W, which is 60% further reduced.

To verify the results, tests have also been done with replaced customized cores. To show the significance, all the three mentioned structures were tested, and the higher the eddy current is, the significant reduction can be found among the structures. From **Fig. 2.8**, the temperature of the eddy current surfaces has all decreased, so did the total losses. For core type transformer, the total loss was reduced by 144.5 W, and vertical shell type 70.6 W, the proposed interleaved shell type 13.4 W, which account for 42.6%, 62.4% and 43% reduction on eddy current loss. As the proposed structure has already significantly reduced the eddy current loss, the reduction seems less significant in the absolute value, but from the thermal image it can be seen that the inner surface of the core now has no hot spot anymore. Therefore, the split core can further reduce the eddy current loss induced by the leakage flux.

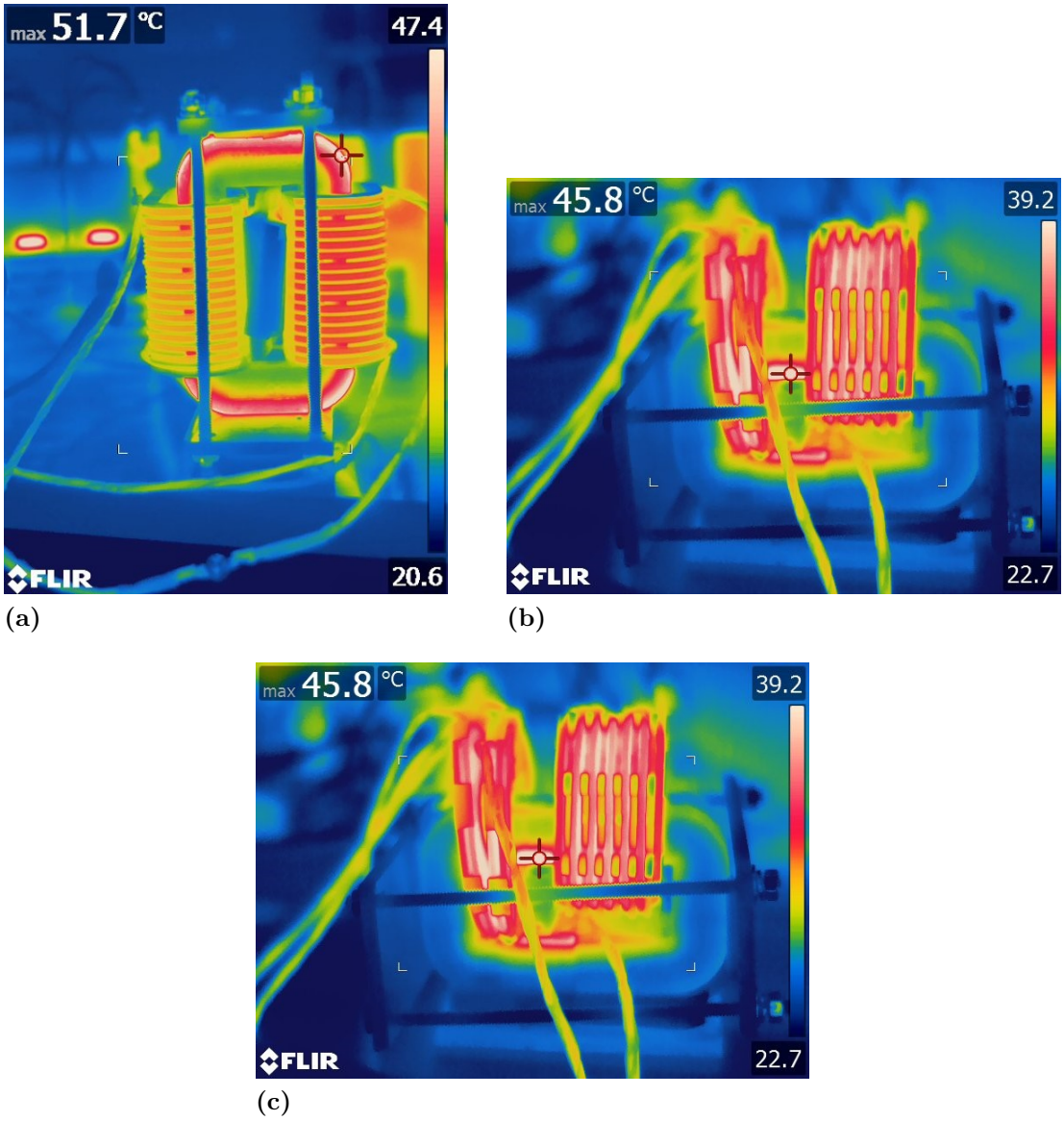


(a)



(b)

Fig. 2.7: Transformer short-circuit simulation with proposed structure: (a) solid nanocrystalline core, (b) 2D Laminated core.



(a) **(b)** **(c)**

Fig. 2.8: Transformer short-circuit simulation with 2D laminated cores (a) core-type, (b) vertical shell-type, (c) interleaved vertical shell-type.

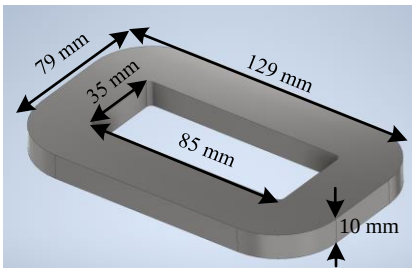
2.5 Test Verification

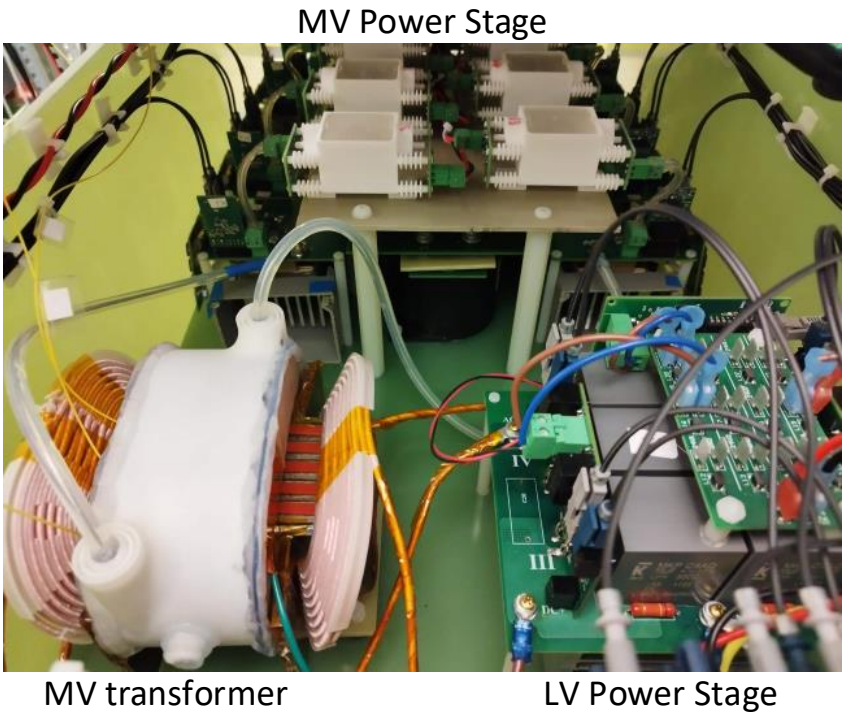
With the proposed leakage integration and insulation, the MV DAB transformer has been designed for a 10 kV SiC-based DAB converter, serving as a front end of a CHB inverter. The design parameters of the transformer are shown in **Table 2.1**. The photograph of the MV transformer with LV and MV power stages are shown in **Fig. 2.9**.

Two transformers have been installed in the DAB converter and paralleled on the MV side, so that power can be circulated between the DAB converters. The DAB has been tested from no-load to full load condition and bidirectionally. The test setup is shown in **Fig. 2.10**. The test waveforms are shown in **Fig. 2.11**. From the test waveforms, the transformer works as expected DAB transformers for both no-load and full-load conditions, and the waveforms of two transformers agree with each other.

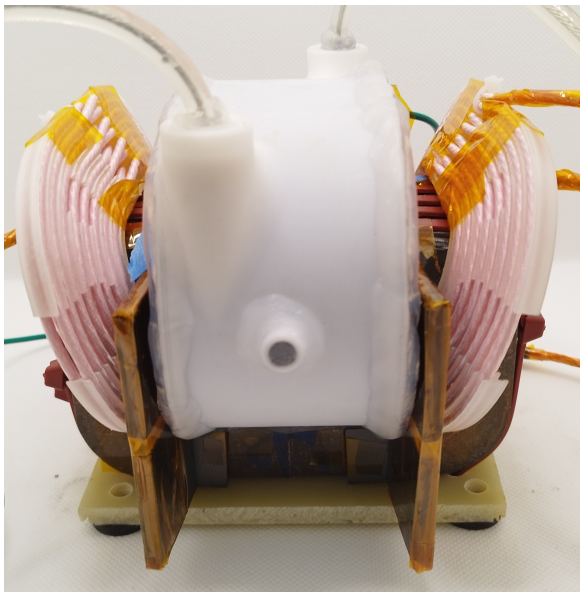
During the test, the efficiency of the setup has also been measured. It can be seen from **Fig. 2.12(a)** that the overall efficiency in heavy loads is greater than 98. 85%, with a peak efficiency of 99.02%. The estimated transformer loss should be around 131.6 W, making the transformer efficiency of 99.2% at full load. The transformer estimated loss breakdown is shown in **Fig. 2.12(b)**, showing that the calculated eddy current loss should be around 32.82 W. The details of the old core-type transformer in **Fig. 2.2** is shown in **Fig. 2.13**. The old transformer used bar ferrite shielding

Table 2.1: Leakage Integrated Transformer Parameters

Parameters	Values
Power Rating	16.7 kW
Voltage Ratings	850 V/6.7 kV
Switching Frequency	10 kHz
Core	
Air Gap	2× 0.2 mm
LV Winding	31 turn 259/AWG36 Litz Wire
MV Winding	244 turn 50/AWG36 Litz Wire
Ferrite Bridge	3C95 Plate, 4mm thick, 40 mm in depth
Ferrite Bridge Air Gap	5 mm
Insulation Rating (MV to ground)	13.4 kV Peak Partial Discharge Free Compliant to IEEE Std C57.12.91-2020
Power Density	8.5 kW/L



(a)



(b)

Fig. 2.9: Photograph of the DAB power stages [19] and (b) MV DAB transformer.

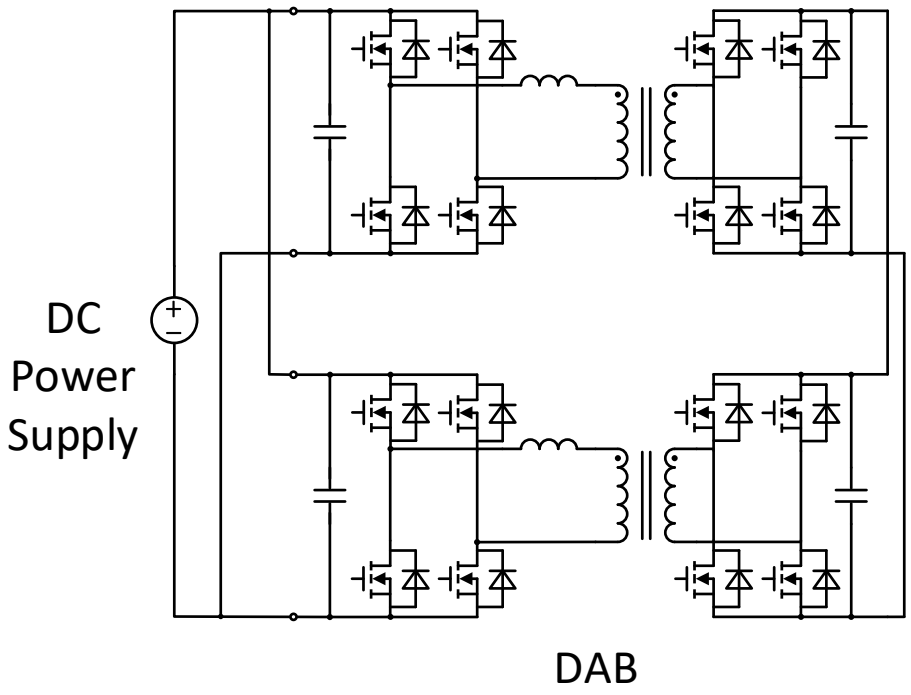
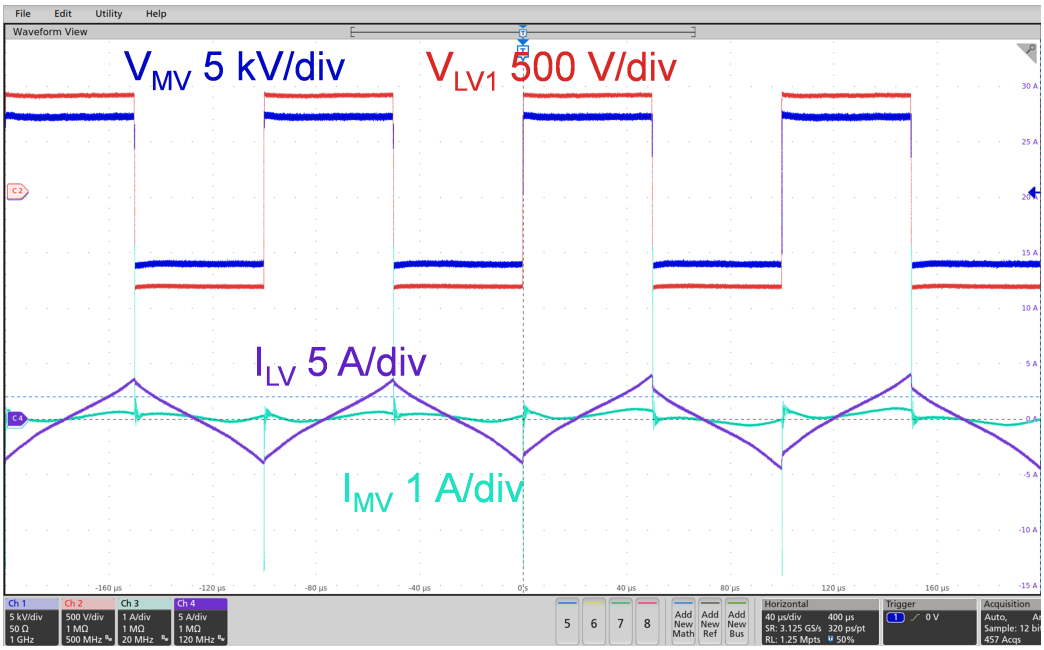
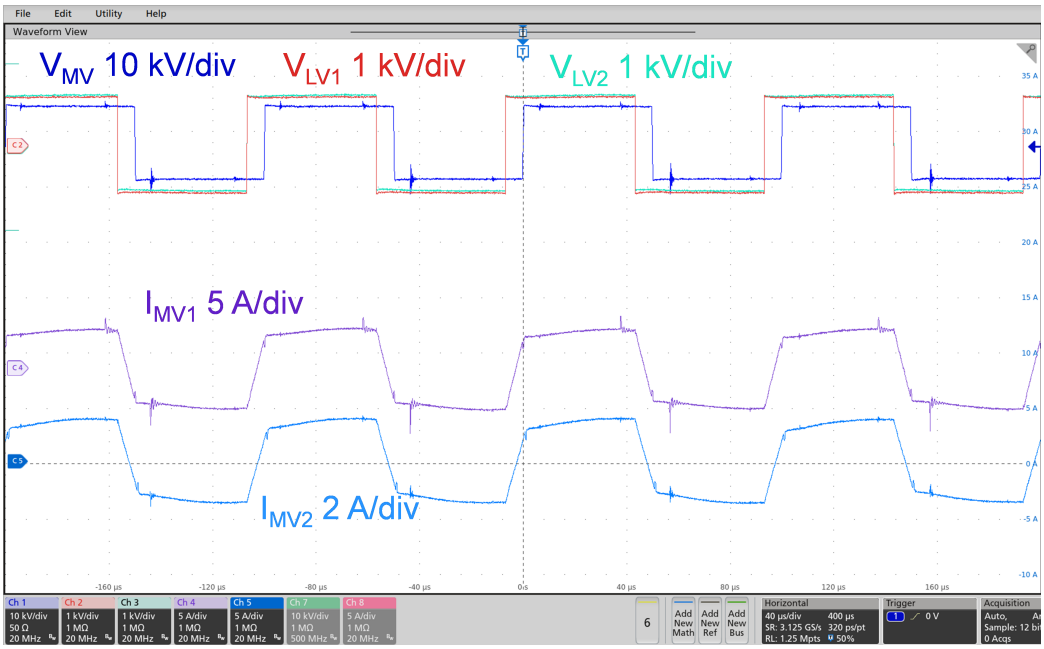


Fig. 2.10: Pump back test setup for MV DAB converter.

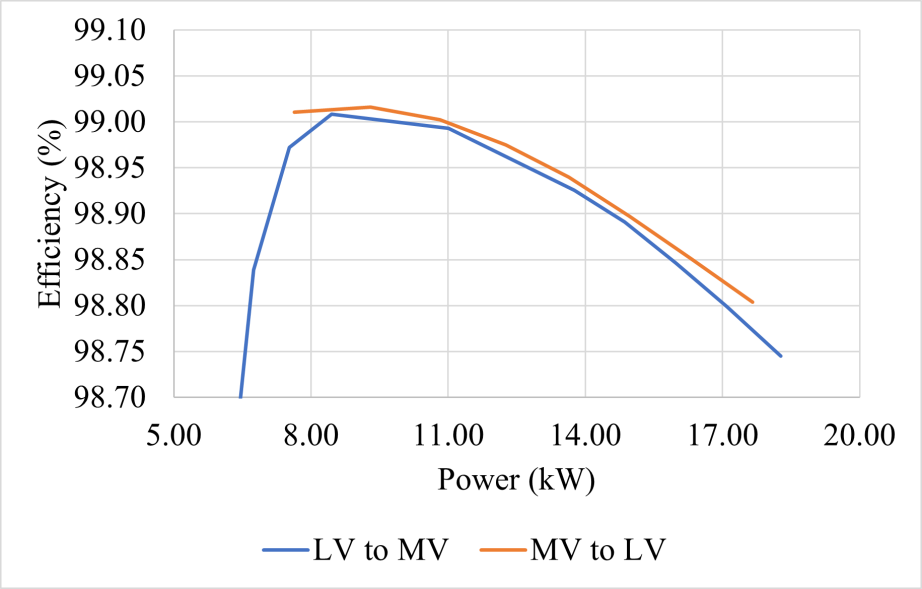


(a)

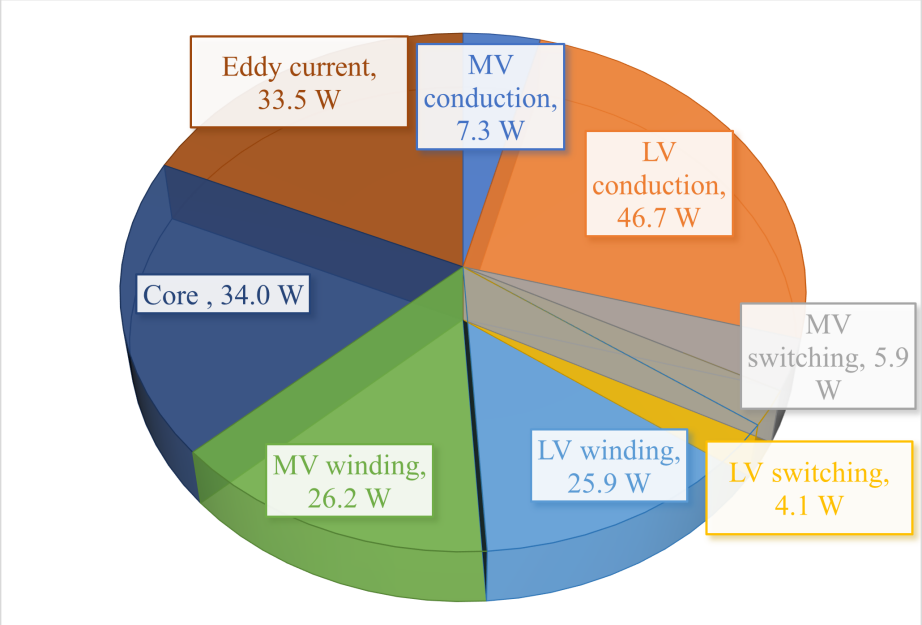


(b)

Fig. 2.11: Test results for MV DAB transformer/converter (a) no-load condition (b) full-load condition [19].

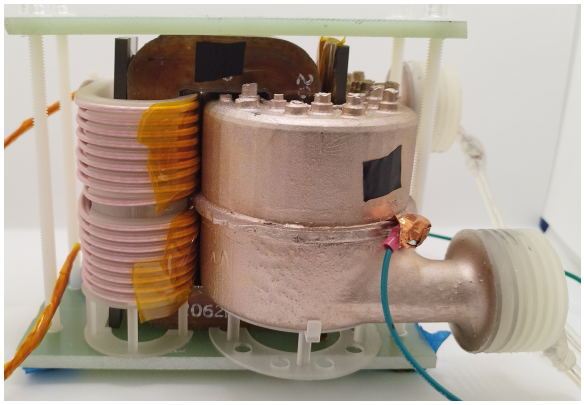


(a)

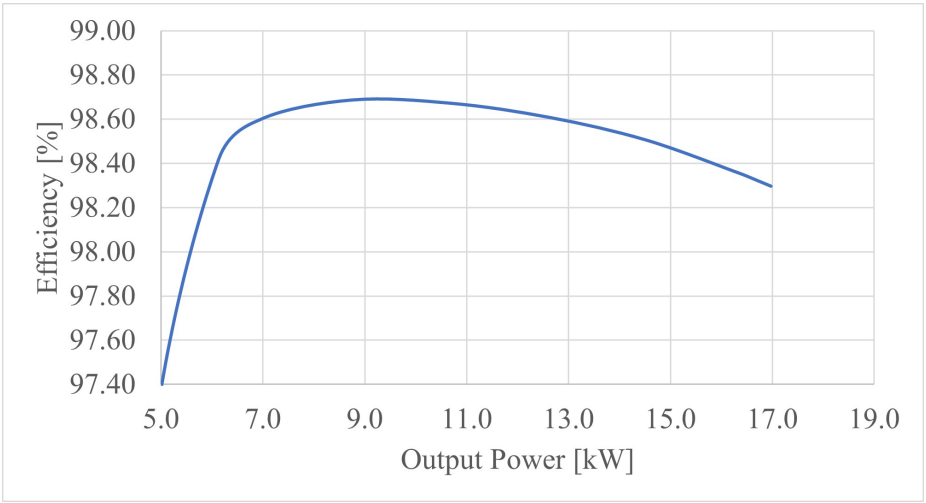


(b)

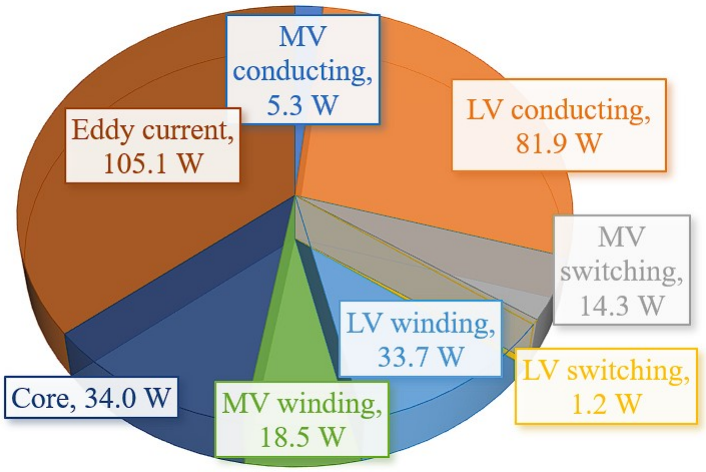
Fig. 2.12: Efficiency test results of the MV DAB (a) efficiency with bidirectional operation, (b) loss breakdown estimation at full load.



(a)



(b)



(c)

Fig. 2.13: The old core-type MV DAB transformer (a) photo graph, (b) efficiency curve, and (c) loss breakdown estimation at full load.

proposed in[18] and having full load efficiency of 98.3%, with a power density of 7.1 kW/L, a total loss of 294 W, and eddy current loss of 105.1 W. Compared to the old transformer, the new transformer using the low-loss leakage integration strategy can reduce total loss by 71.7 W, and the eddy current loss has been reduced by 72.28 W and 68.7%.

2.6 Potential Future 2-D Lamination Structure

As the 2D lamination structure has been introduced and verified in the previous sections, the limitation lies on the engineering capability and inherent shape of the ribbon-based cores: the depth of each core unit is limited to the width of alloy ribbons, with a minimum of 10 mm; the shape of the core has to be wound resembling to a race track, resulting in a circular, oval, or corner rounded rectangular shape. For different applications, the power rating may be higher, such as silicon steel-based line transformers, or continuous variable series reactors (CVSR) in power grid, with mild core saturation during normal operation [85]. Or, higher frequency and efficiency are required, so the eddy current has to be further mitigated. Regarding this, the proposed 2-D lamination can be further extended to new structures, and it can be potentially achieved in the future with improving manufacturing technology. **Fig. 2.14** illustrates the structures with 2D lamination concept, in which **Fig. 2.14(a)** is the aforementioned structure for ribbon-based cores, while **Fig. 2.14(b)** can be

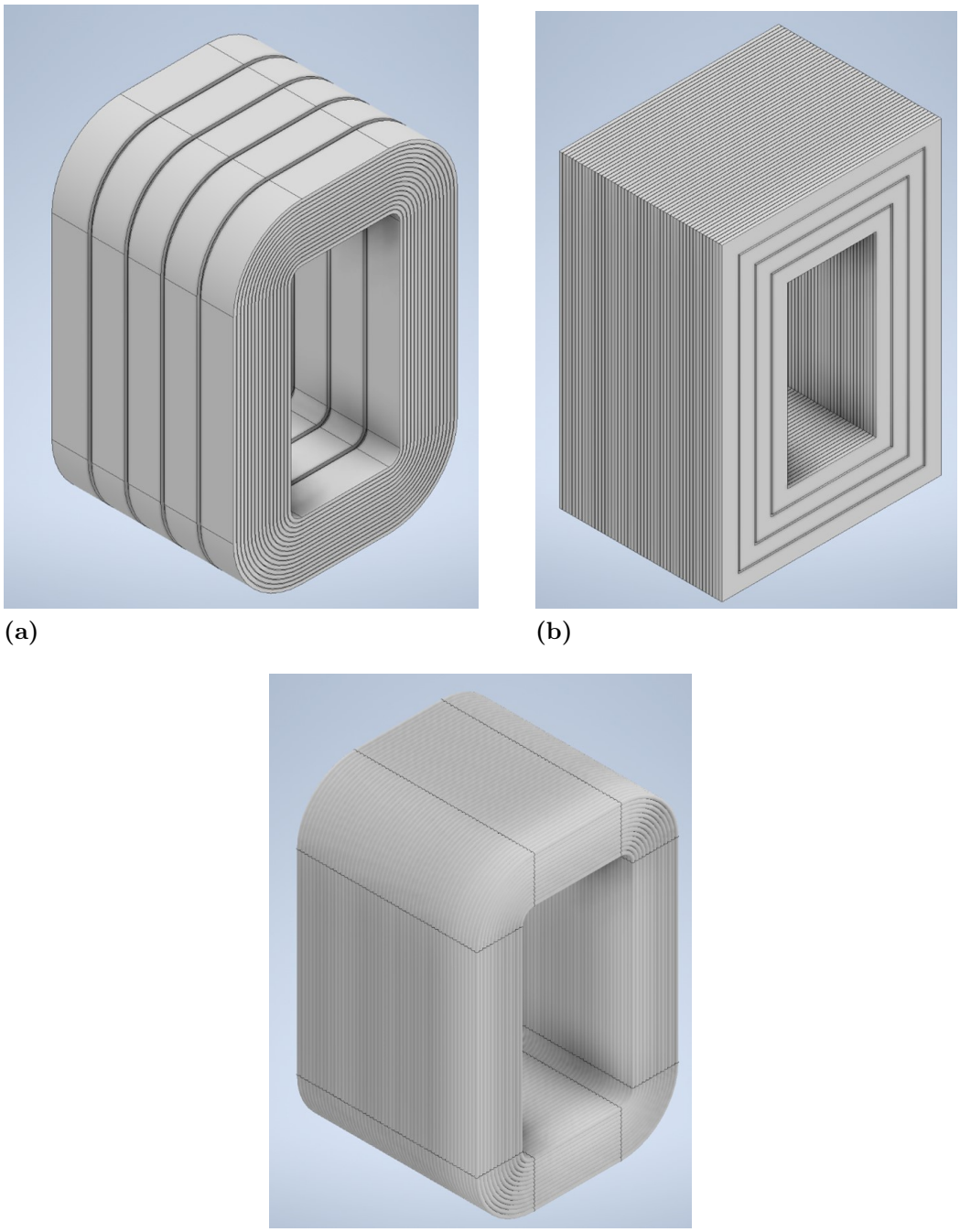


Fig. 2.14: 2D lamination techniques for (a) ribbon-based cores, (b) block- or silicon steel-based cores, and (c) magnetic alloy wire-wound cores.

implemented for block-core or silicon steel sheet-based cores, and **Fig. 2.14(c)** the magnetic wire-based core can be manufactured if magnetic alloy can be formed into insulated wires.

In **Fig. 2.14(b)**, this structure can be used when the silicon steel sheets or nanocrystalline bars/blocks are used to form the core. Either silicon steel sheets cut into narrower widths or block/bars manufactured into narrower geometry, the cores can be formed with stacking in two directions to form the two-dimensional lamination. In this way, the surface lamination area can be split into small blocks, and therefore the eddy current in the surface plane can be suppressed simply resembling the ribbon-based cores.

Furthermore, if current magnetic alloys, namely nanocrystalline, amorphous, or permalloy, can be extruded into thin and surface insulated wires, the core can be made by winding the wire radially and axially to form the core as shown in **Fig. 2.14(c)**. With this, the size of the core surface can be further divided even smaller than in ribbon or sheet-based cores, so that the eddy current can be suppressed.

2.7 Summary

In this chapter, a MV transformer design with low-loss leakage integration has been introduced.

- First, the leakage inductance is categorized into two terms: intrinsic and external inductances, and high level methodology of minimizing intrinsic leakage

and utilizing external leakage structure is introduced. Then, the leakage induced eddy current loss analyzed with homogeneous anisotropic core model.

- Low loss leakage integration with ferrite bridge proposed, analyzed and tested. Different transformer structures with similar leakage inductance is studied at short-circuit condition. Through the simulation and tests, the shell-type transformer with interleaved LV winding and ferrite bridges can have better leakage integration capability and loss performance.

- The leakage induced eddy current can be further reduced by implementing 2D laminated cores. Thanks to narrower ribbon-based cores, the surface area for eddy current conduction can be limited, forming a 2-D lamination structure. With the proposed 2-D lamination structure, the eddy current loss can be further mitigated.

- Based on the proposed techniques, a 850-V/6700-V 16.7-kW MV DAB transformer has been designed and tested. The whole DAB converter system achieved 98.85% power efficiency at full load condition, and the leakage inductance induced eddy current has been reduced by 68.7%, with the transformer having a power density of 8 kW/L.

- The concept of 2D lamination structure has been extended to different types of alloy wire, or sheet-based cores. Due to the current engineering capability, the depth of the core is limited to 10 mm, and also limited to the oval or C-core

structure. With the potential of technology development, the new structures can have better leakage mitigation capability, and hence lower loss and higher efficiency can be achieved.

Chapter 3

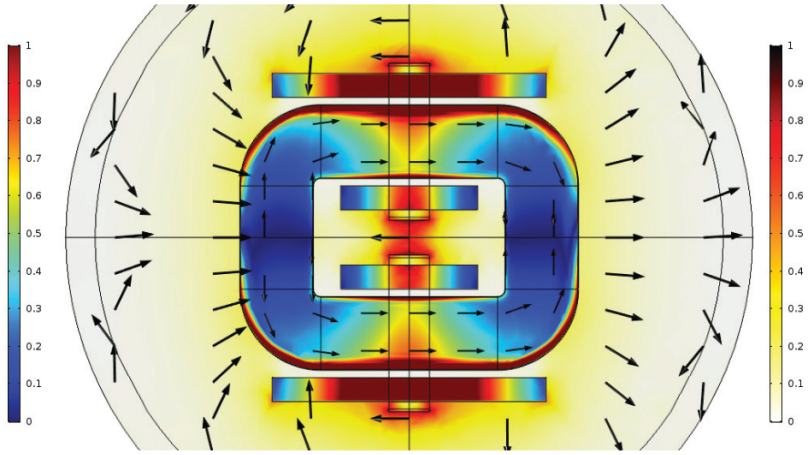
Eddy Current Suppression for Ribbon-Based Magnetics Using Ferrite Shielding

3.1 Literature Review

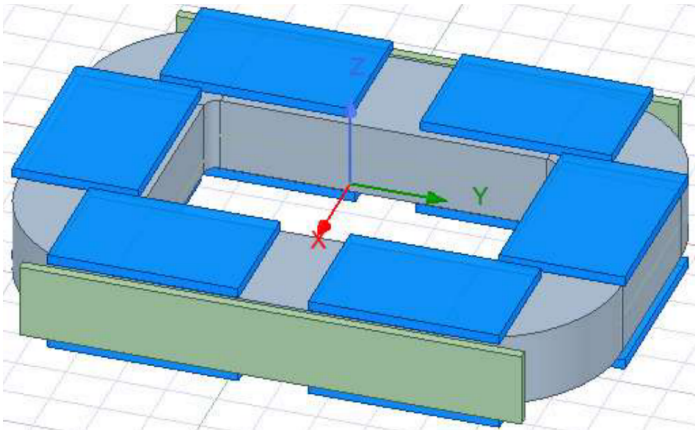
Ribbon-based magnetic cores, including nanocrystalline and amorphous cores, have been widely used for inductors and transformers in high power electronic converters. The ribbon-based cores are wound from thin (15˜25 μm) magnetic alloy ribbons into O-shaped loops, and then can be cut into different shapes. The ribbons have surface insulation to insulate between different layers to suppress the eddy current generated by the mainstream flux flowing along the core geometry. Thanks to the high saturation flux density, compact passive design can be achieved for medium voltage

high power converters. However, as the ribbon structure creates lamination layers, stray magnetic field going perpendicular to the lamination layer can cause high eddy current and extra loss [18, 23]. In the cases of fringing effect of air-gapped inductors, or leakage integration for transformers, considerable magnetic field can be generated in the direction orthogonal to the lamination plane, and hence extra eddy current is generated, causing unexpected high core loss and heat on the core surfaces.

In recent years, many solutions have been proposed to suppress the eddy current. Firstly, ferrite shielding has been proposed in [18] and [25], where the lamination surfaces are shielded by ferrite plates (see **Fig. 3.1(a)(b)**). With the stray magnetic flux redirected into the ferrite, which is far less conductive, the eddy current in the cores can be reduced. However, it requires careful strategy on the shielding geometry, as the permeability of ferrite is relatively low compared to ribbon-based materials, and the ferrite geometric coverage also plays an important role on eddy current reduction. One can easily see that the smaller shielding area may reduce the effectiveness, but covering too much area of core surfaces may link the ferrite shielding into the main magnetization loop and generate more ferrite core loss, and it can also block the core from convection cooling path. Another way is to split the cores into narrow units with smaller lamination surface, and by creating a 2-D lamination structure [27, 19], the eddy current can be naturally suppressed. The drawback is that it usually requires core customization with high cost, and due to the manufacturability, the cores cannot be narrower below 10 mm, and hence the reduction is incomplete.



(a)



(b)

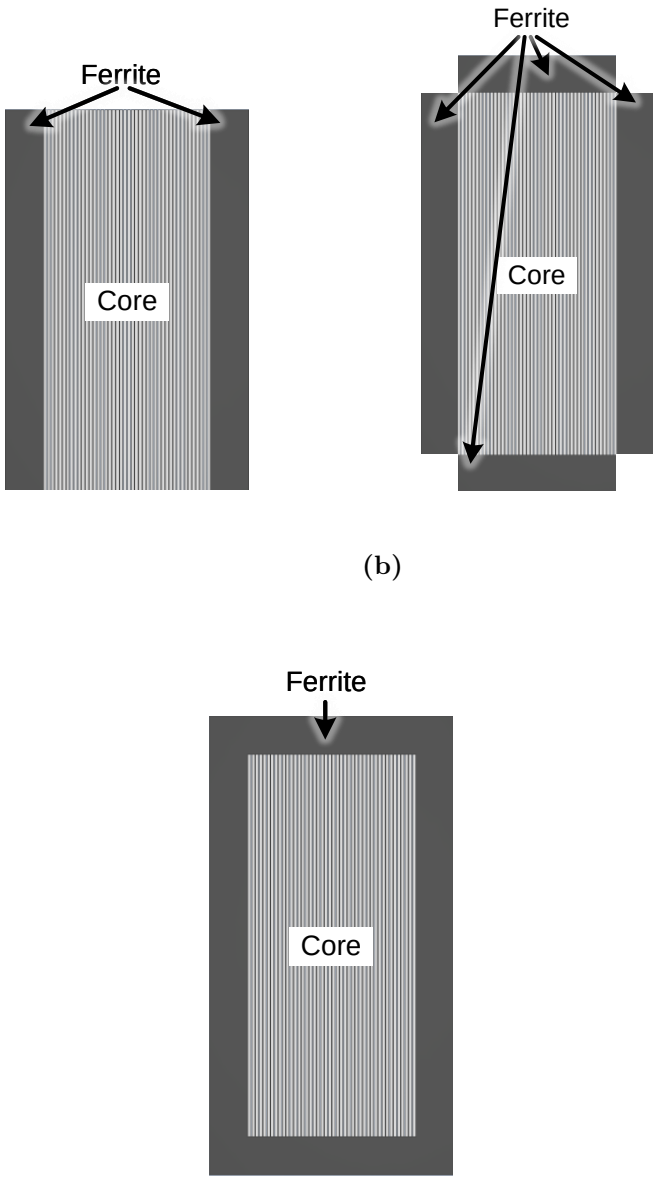
Fig. 3.1: Conventional ferrite shielding structure, (a) bar shield [18], (b) hybrid core structure [25].

3.2 Proposed Ferrite Shielding Structure: Case Studies

The conceptual drawing of the conventional shielding and the proposed structure is shown in **Fig. 3.2**. Unlike in [18] and [25], the proposed ferrite shielding extends to the two side surfaces of the cores, which expose the edges of each lamination layer, and the ferrite covering the adjacent faces are physically connected together. To better understand the proposed method, the proposed shielding for the gapped inductor case is shown in **Fig. 3.3(a)**. The proposed ferrite shielding is on the critical surfaces expected to see a high stray magnetic field, and the shielding is also further extended with a right angle to the two sides of the core. Therefore, a low-reluctance path can be formed for the stray flux passing the core lamination to the air, without directly crossing the lamination planes. **Fig. 3.3(b)(c)** show that with the proposed ferrite shielding, the flux can be shaped so that the flux line is parallel to the lamination plane, suppressing the eddy current to a minimum by the thickness of the ribbon, and the flux can be redirected by the lossless ferrite into the air gap.

3.2.1 Eddy Current Reduction on Gapped Inductors

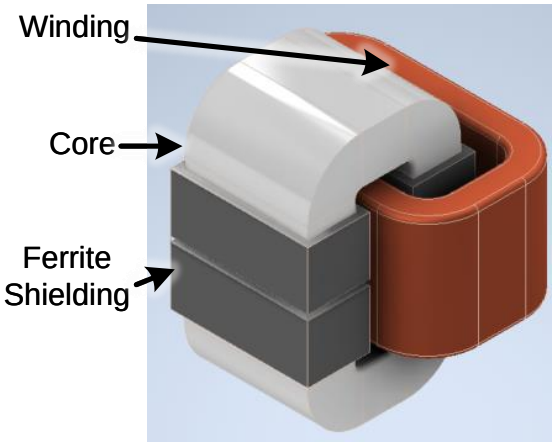
The proposed method is first implemented in amorphous-based inductors thanks to its simplicity. **Fig. 3.3(a)** already depicts the mechanical drawing of the proposed inductor. The inductor uses an *AMCC 1000* amorphous core and multiple ferrite plates (PLT38/25/3.8-3C95) in the vicinity of air gaps, surrounding both the



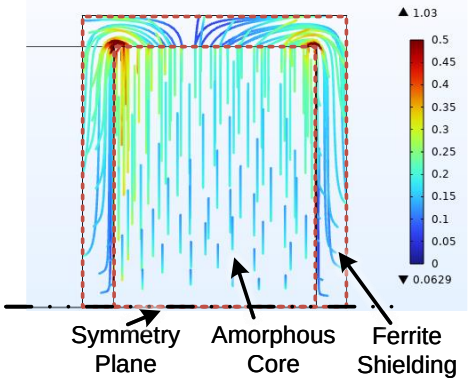
(a) **(b)**

(c)

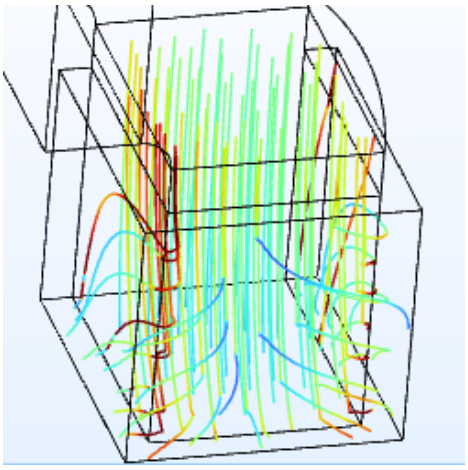
Fig. 3.2: Conceptual drawing of (a) bar shield [18], (b) hybrid core structure [25], and (c) proposed shielding [26].



(a)



(b)



(c)

Fig. 3.3: Proposed ferrite shielding (a) illustration for the gapped inductor case; (b) flux line simulation results at top view; (c) flux line at perspective view.

lamination planes and the core sides (see **Fig. 3.4**). In order to keep the inductance (1.4 mH) unchanged, the air gap without shielding was set to 5 mm for each leg, and 6.5 mm for the shielded inductor as the shielding inevitably added a portion of the cross-sectional area in the air gap.

A simulation has been performed to compare unshielded and shielded inductors, and selected results are shown in **Fig. 3.5**. The lamination has been homogenized as in [19]. From **Fig. 3.5**, it can be seen that without the shielding, the surface current density can be over 10 A/mm2 at the corners close to air gap, while when the ferrite added, the current can be significantly reduced, with most of the areas close to 0. From the simulation, the estimated eddy current loss can be reduced by 82%. The concern on the ferrite application with ribbon-based core is usually the mismatch of saturated flux level, and it can be found in **Fig. 3.5(c)** that, with a main flux

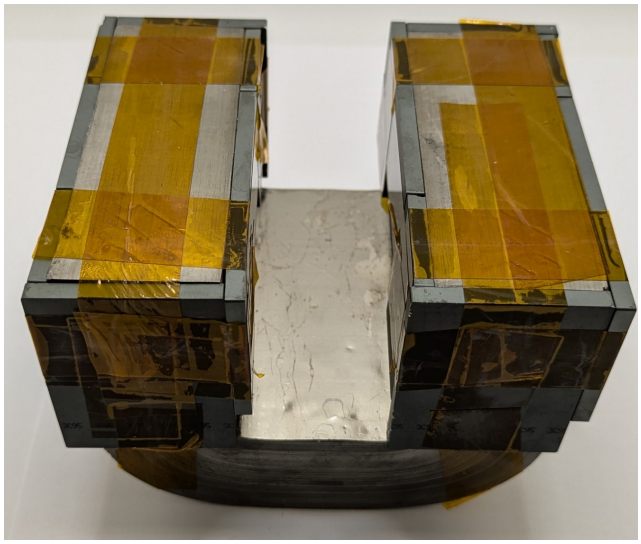
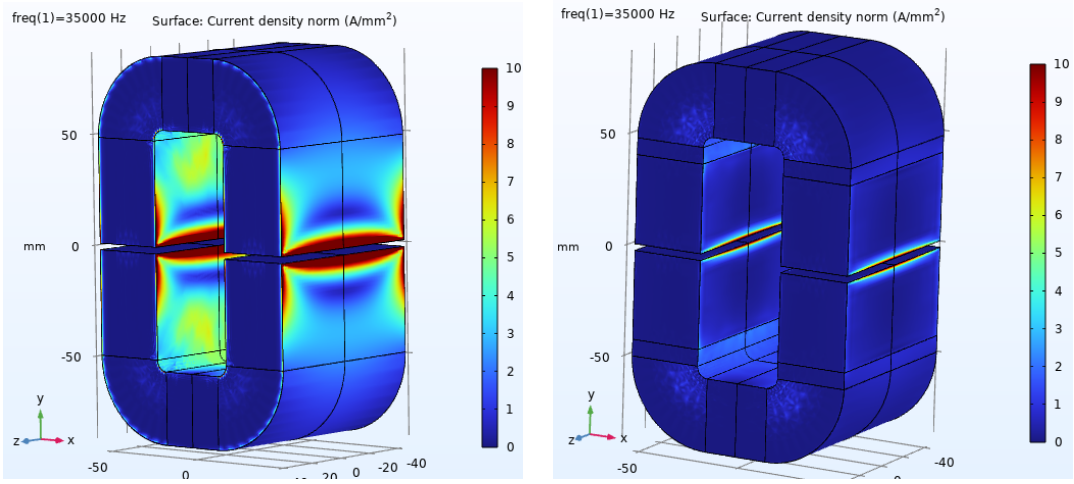
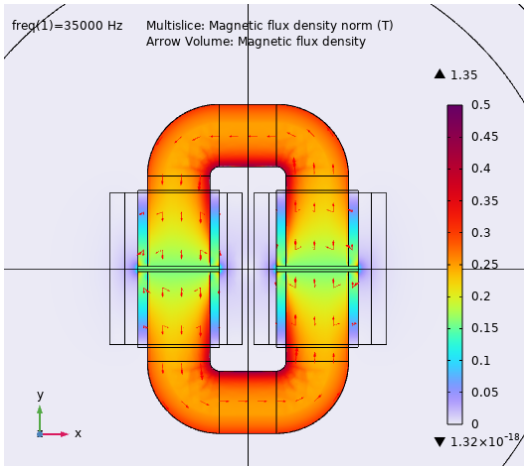


Fig. 3.4: Photo of the amorphous inductor core with ferrite shielding.



(a) **(b)**



(c)

Fig. 3.5: Inductor simulation results (a) unshielded, current density; (b) shielded, current density; (c) shielded, flux density.

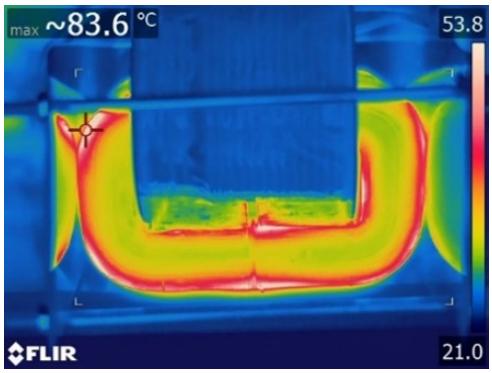
density of 0.4 T, the flux density within ferrite is lower than 0.15 T, which is below the saturation level of the ferrite.

Zero DC Current Test

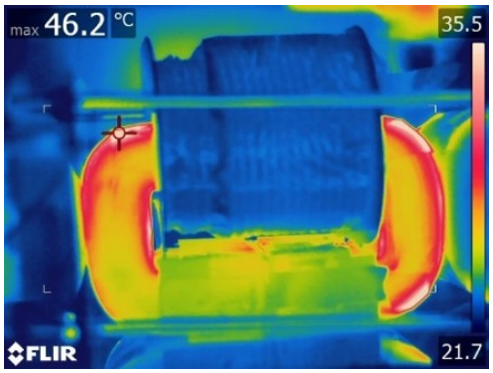
First, experimental tests with zero DC current have also been performed, an inductor with aforementioned core and gap size has been made, and the inductor is excited by H-bridge at 800 V dc-link and 20 kHz switching frequency and 50% constant duty cycle. The thermal images for both cases have been recorded as in **Fig. 3.6(a)(b)**, showing the hotspot has been reduced by 37℃. The loss of the setup is reduced from 105 W to 68 W with ferrite shielding.

DC Biased Test

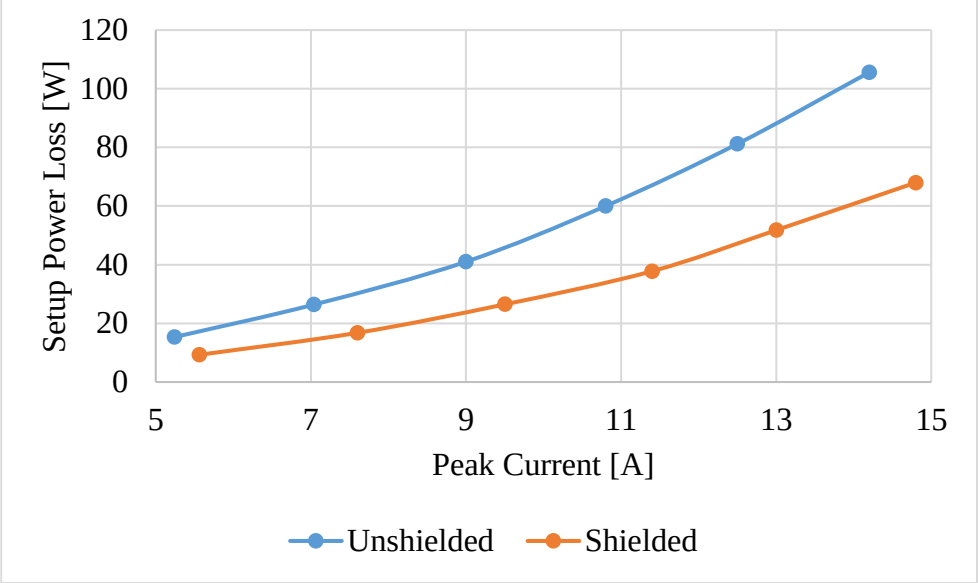
Then, to test with higher flux density, the inductor is excited with DC biased current. **Fig. 3.7(a)** shows the test waveform. The power losses are shown in **Fig. 3.7(b)**, and as the DC current increases, the power loss stays constant at first due to the devices transited from ZVS to hard switching state. At below 5 A, regardless of the current level, the reduction is constant which is around 69 W, because the current ripple in the inductor is constant at low DC biased voltage, and therefore the flux density ripple and eddy current remains constant. At around 57.3 A, the reduction decreases, which is due to partial saturation of ferrite shielding. At that level, the main amorphous core flux density is over 0.74 T, and some flux lines may crowd in the edges and corners of the ferrite, limiting the effectiveness of the ferrite shielding.



(a)

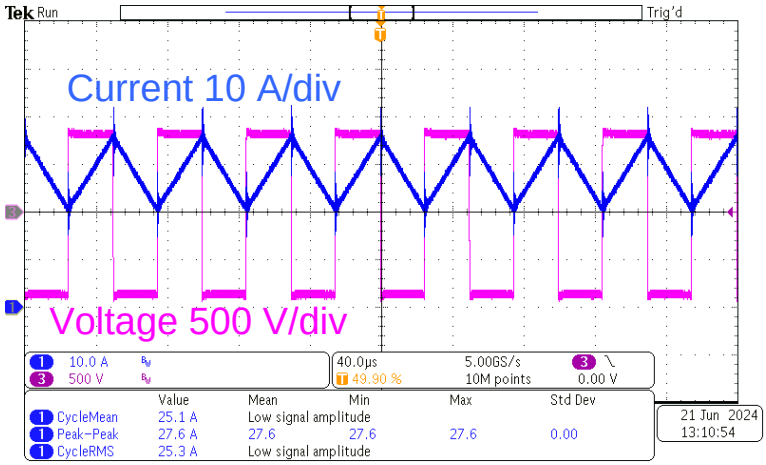


(b)

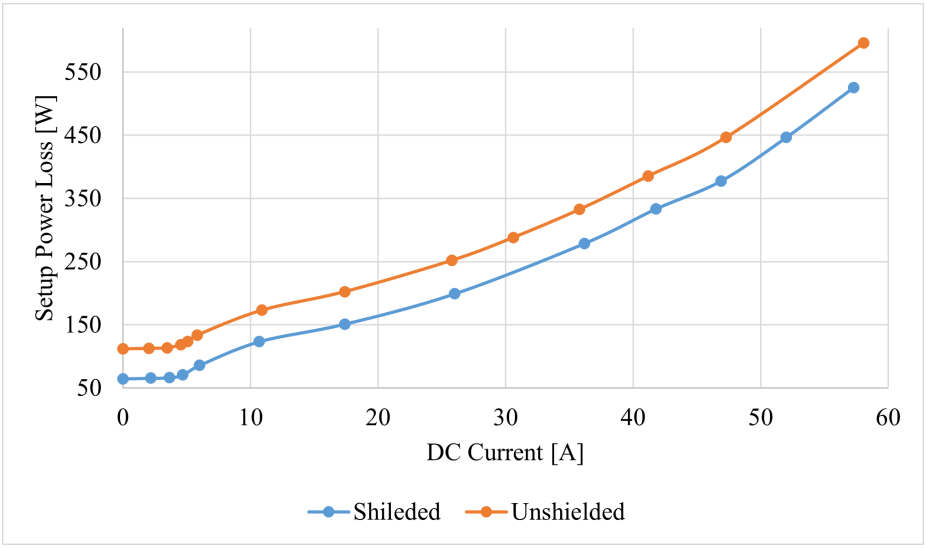


(c)

Fig. 3.6: Inductor test results (a) unshielded, thermal image; (b) shielded, thermal image; (c) setup power loss.



(a)

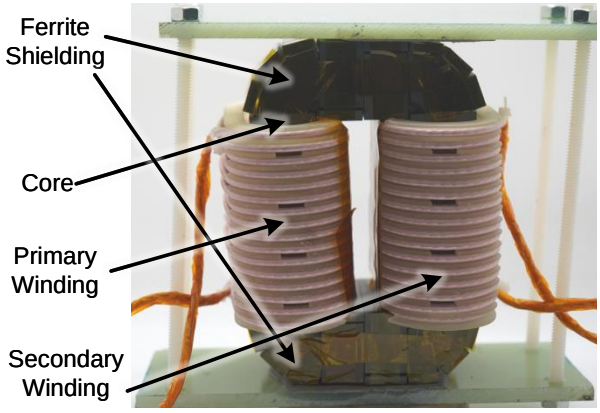


(b)

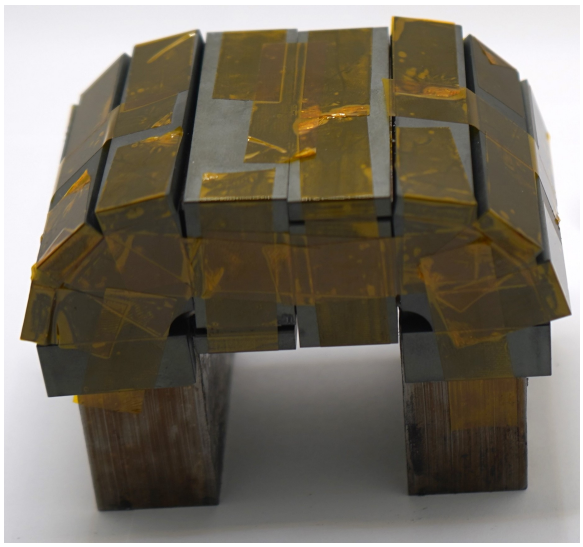
Fig. 3.7: Inductor DC bias test results (a) waveform; (b) power loss comparison.

3.2.2 Eddy Current Reduction on Core-Type Transformer

Similar analyses and tests have also been performed on a core-type transformer for a dual-active-bridge converter. The transformer uses nanocrystalline core SC2062M1 with 31-to-31 turns on both sides, and the main structure is shown in **Fig. 3.8**.



(a)



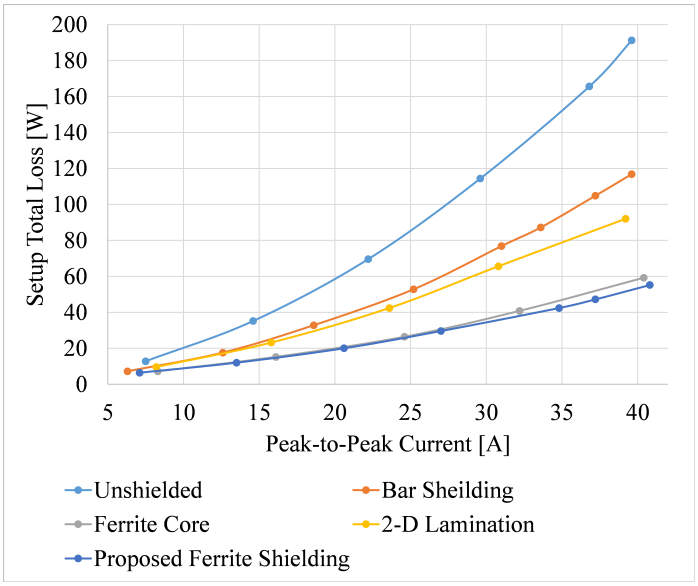
(b)

Fig. 3.8: Photo of the proposed (a) transformer with ferrite shielding, (b) nanocrystalline core with shielding.

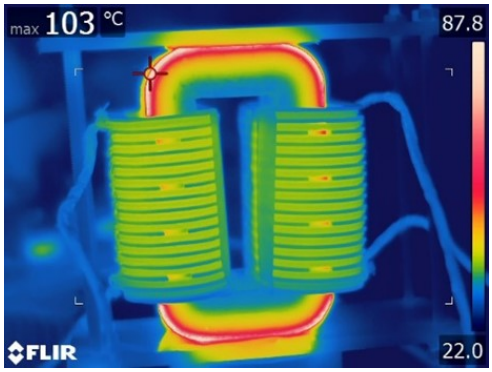
Short-Circuit Test

Different core configurations, i.e. original unshielded core, bar-shielded core as in [18], 2-D laminated core as in [19], a ferrite core with the same size and dimension, and the proposed ferrite shielded core, have been realized to compare the actual eddy current loss reduction. The leakage inductance of all core configurations is kept at 270 H thanks to the same outer geometry of all the core configurations, so that the differences of current waveform, H-bridge device losses are minimized. **Fig. 3.9(a)** presents the loss comparison among the five core configuration cases. The unshielded configuration exhibits the highest loss, exceeding 190 W. By using bar-shielded cores, the total loss is reduced by 75 W, with an additional reduction of 24 W achieved through 2-D lamination. The ferrite core and the proposed ferrite shielding configurations demonstrate the lowest losses, both approximately 60 W with minimal variation. The difference between the ferrite core case and the proposed case mainly comes from the copper and device losses due to the variation of leakage inductances, and possibly small amounts of core losses due to the leakage field in cores and measurement error.

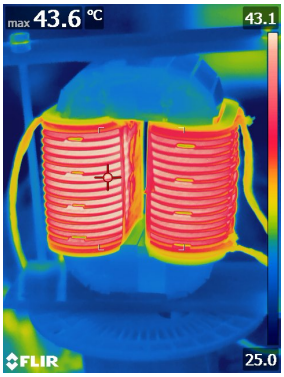
As the current waveform, winding losses, and device losses are consistent across all cases, and no core loss is expected during a short-circuit test, the observed reductions are attributed solely to eddy current losses. The minimized loss in the ferrite core configuration is due to its low electrical conductivity, effectively eliminating eddy current losses. Consequently, the proposed shielding case achieves a similar loss



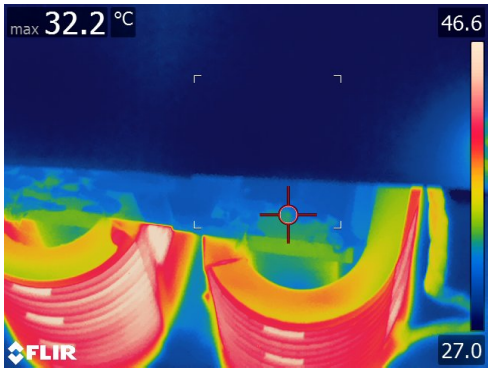
(a)



(b)



(c)



(d)

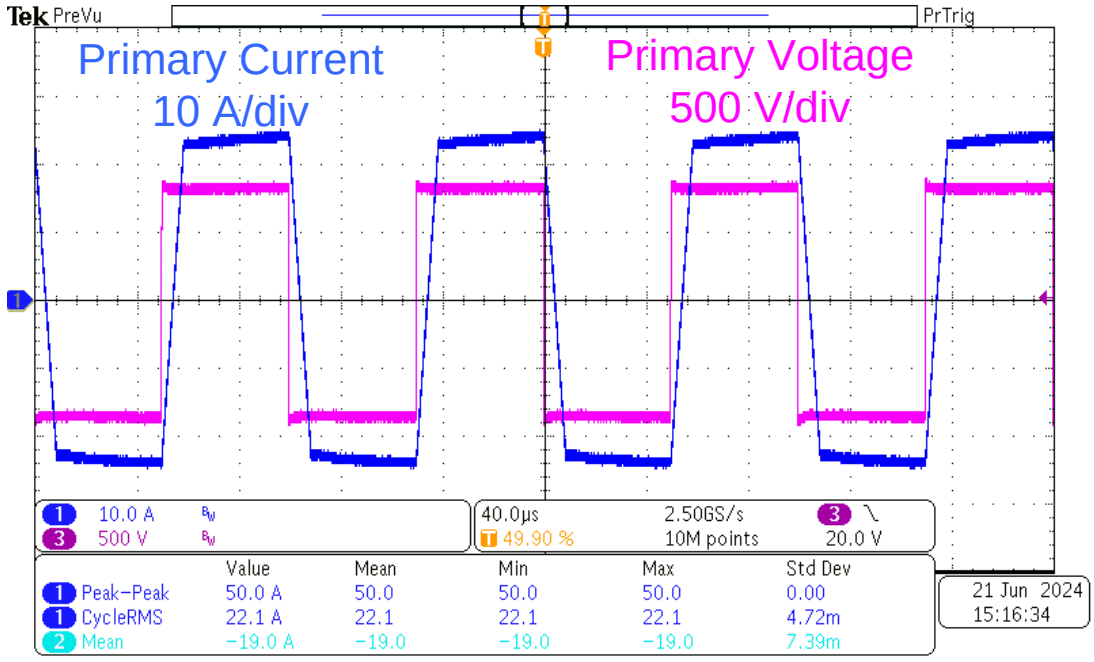
Fig. 3.9: Core-type transformer short-circuit test results (a) total loss comparison of the transformer short-circuit test setup; (b) unshielded, thermal image; (c) shielded, thermal image; (d) shielded, zoomed-in thermal image with tilted angle.

reduction compared to the ferrite core case. Given that core loss is negligible in all configurations, the eddy current reduction in the proposed shielding is deemed the most effective and comprehensive.

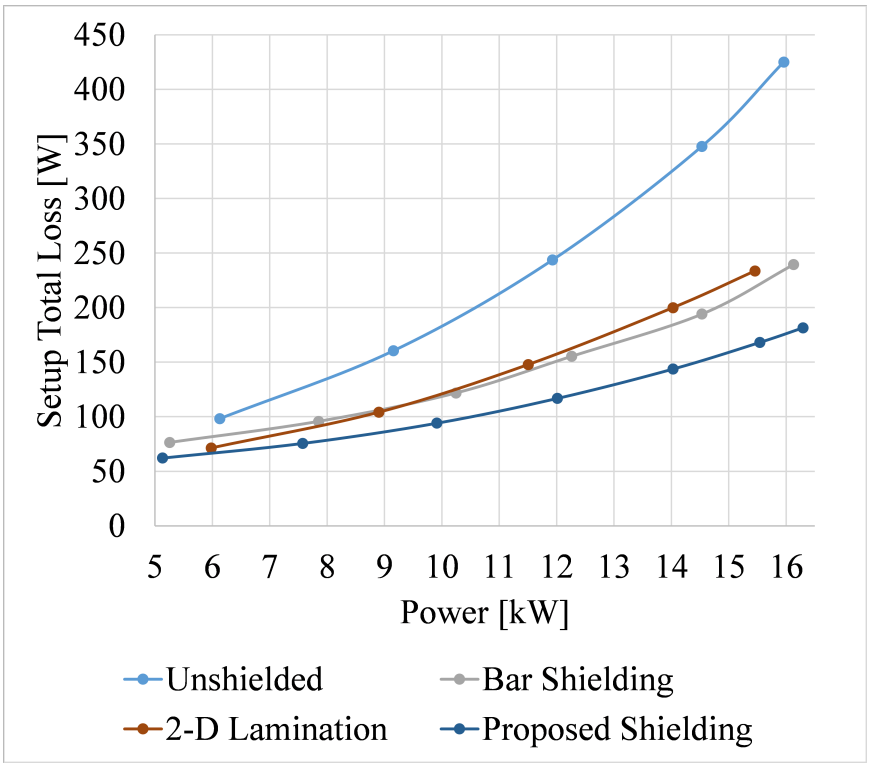
Thermal images have been recorded for the unshielded and proposed shielded case. **Fig. 3.9(b)** shows the thermal image taken after 5 minutes of operation of the test, and the outer surface of the nanocrystalline core has been heated up to 103℃due to the concentrated eddy current loss. As the thermal image of the proposed shielding at 10 minutes and around equilibrium shown in **Fig. 3.9(c)**, the nanocrystalline core and ferrite shielding are not significantly heated up. In case that the hotspot on the nanocrystalline core is covered by the ferrites, another thermal image is taken and demonstrated in **Fig. 3.9(d)**, from which the outer edges of the nanocrystalline are slightly warmer than the center layers of the core at around 35℃. Therefore, the proposed method is also verified through thermal measurement.

DAB Test

The core-type transformer has been put into a DAB converter to perform a pump-back test to rule out any possible discrepancy during the short-circuit test. As the ferrite core would saturate at the operational point of 0.8 T, the ferrite case is excluded from the DAB test. **Fig. 3.10(a)** shows the transformer waveform on the primary side. Again, as the leakage and magnetizing inductances do not vary significantly between the shielded and unshielded cases, the transformer current waveforms in the two cases should resemble each other, ruling out the change of device loss, copper



(a)



(b)

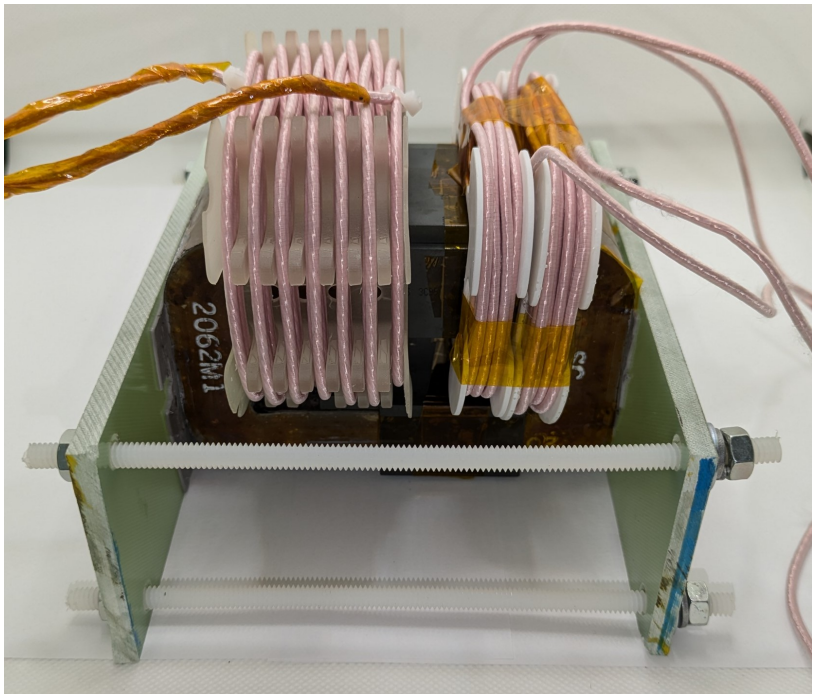
Fig. 3.10: DAB test for core-type transformer (a) waveform, (b) loss comparison.

loss and magnetizing core losses. **Fig. 3.10(b)** shows the test results. From the loss curves, it can be seen that the unshielded case has the highest loss around 425 W, and with bar shielding in [18], the total loss is reduced by approximately 185 W. Different from the results in **Fig. 3.9(d)**, the 2-D lamination seemingly has slightly higher loss, which is caused by the variation of the core from different batches during the manufacturing. The proposed shielding has the lowest loss, which reduces the eddy current loss by 245 W, which is 57% of the loss of DAB setup with unshielded core. From the loss comparison, it can be seen that the proposed ferrite shielding can effectively reduce the eddy current loss.

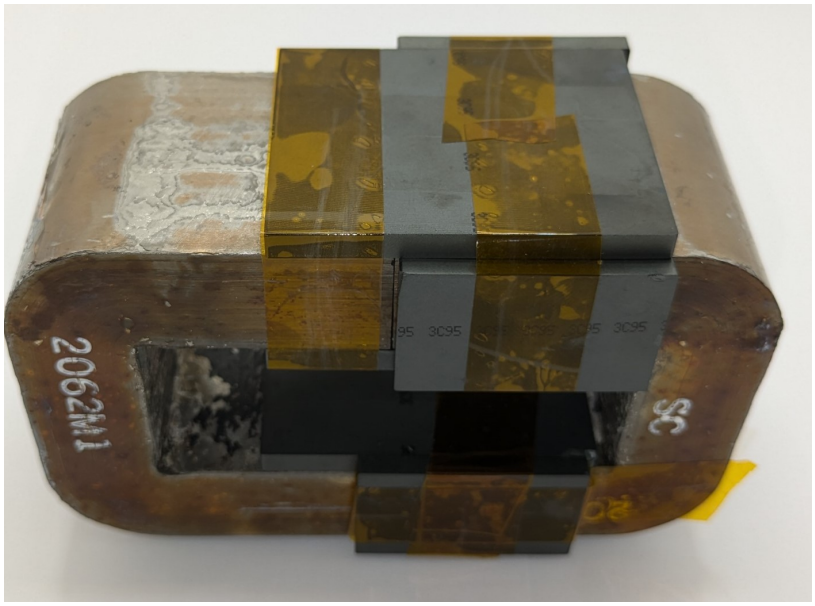
Compared to case studies for inductors, the shielding for transformers has more complete loss reduction. The reason is that the leakage flux and main magnetizing flux of transformers are decoupled, and only the leakage flux flows through the ferrite, while the fringing flux in the inductor serves as one part of the main flux in the inductor core, with which the ferrite may induce higher flux contributing to the main flux to induce eddy current. The leakage flux of transformers are also relatively small compared with the main flux, and hence it can be easier to be bypassed and shielded.

3.2.3 Eddy Current Reduction on Shell-Type Transformer

The proposed shielding has also been implemented into the vertical shell-type transformers. **Fig. 3.11(a)** shows the photograph of the transformer, and **Fig. 3.11(b)** shows the ferrite surrounded transformer core.



(a)



(b)

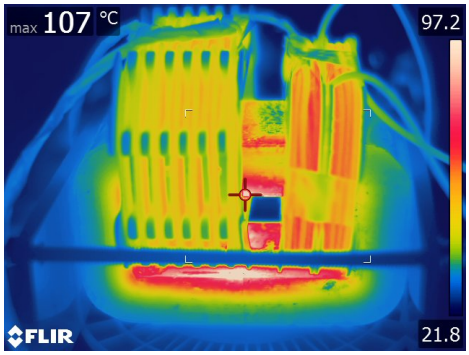
Fig. 3.11: Photograph of (a) shell-type transformer with shielding, and (b) nanocrystalline core with shielding.

Short-Circuit Test

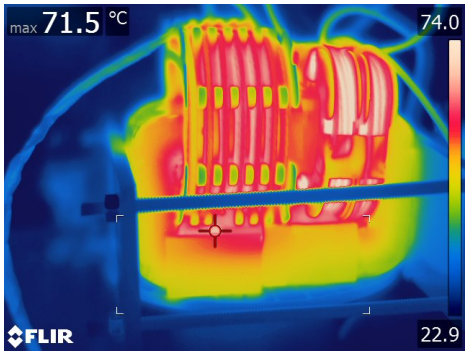
Similarly, short-circuit test is firstly performed to evaluate the performance. **Fig. 3.12(a)(b)** shows the thermal image when the transformer is excited with short-circuit current. In **Fig. 3.12(a)**, the hot spot temperature is over 100℃at the inner surface of the core, which is due to the leakage field inside of the transformer core window, while in **Fig. 3.12(b)**, although the hotspot may be buried in the ferrite shielding, the core surface outside of the shielding area has also lower temperature. Through **Fig. 3.12(c)**, loss reduction of as high as 35 W can be seen, verifying the shielding effectiveness.

DAB Test

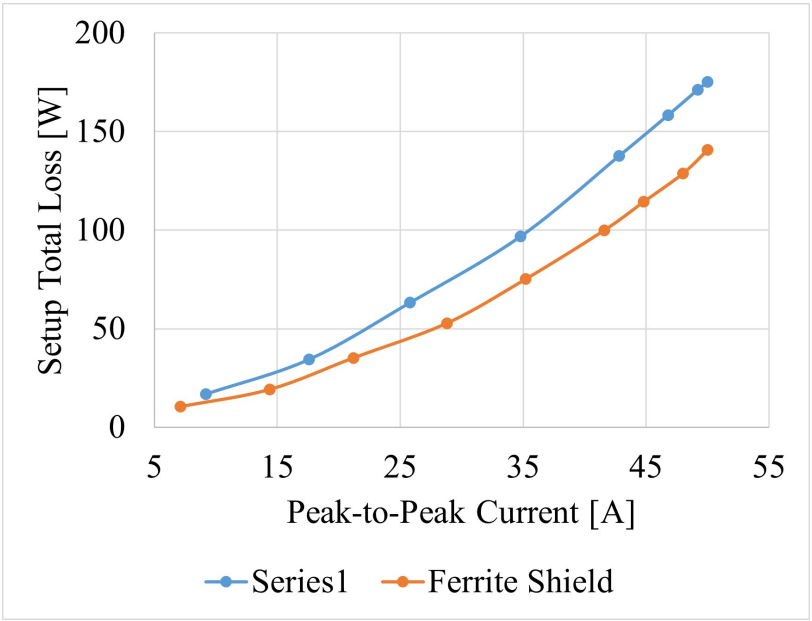
Finally, the DAB test is also performed for the shell-type transformer. **Fig. 3.13(a)** shows the test waveform of the transformer primary side. **Fig. 3.13(b)** shows the loss comparison between the transformer with and without ferrite shielding. As the DAB converting power from 7 kW to 15 kW, the loss reduction is getting higher, and reached around 20 W reduction at the full load, demonstrating the effectiveness of the shielding.



(a)

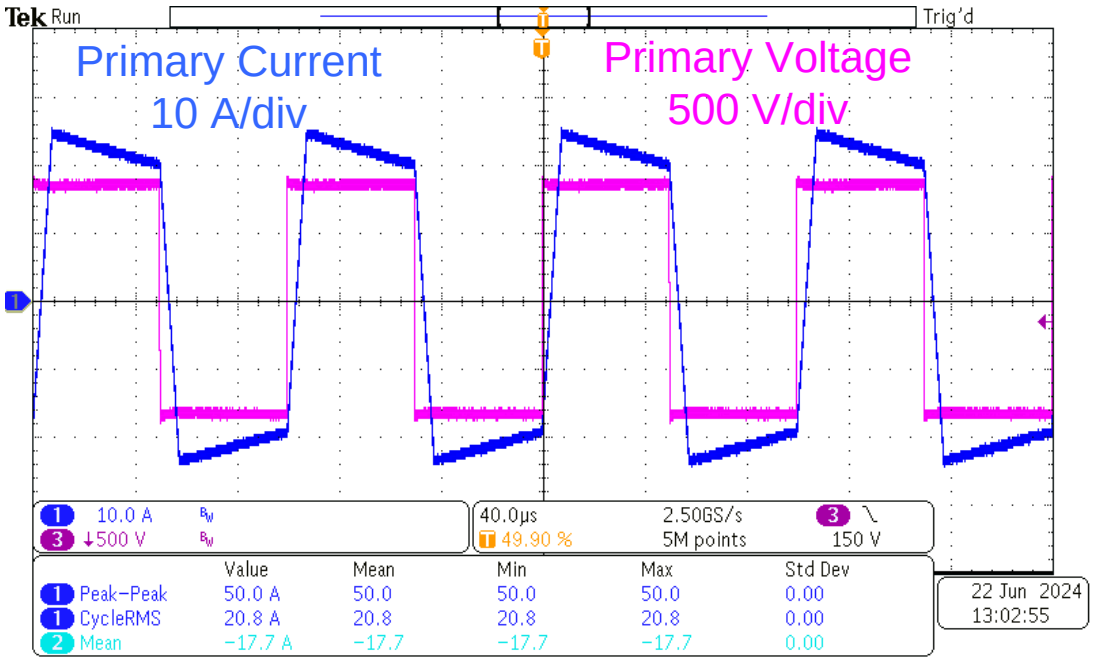


(b)

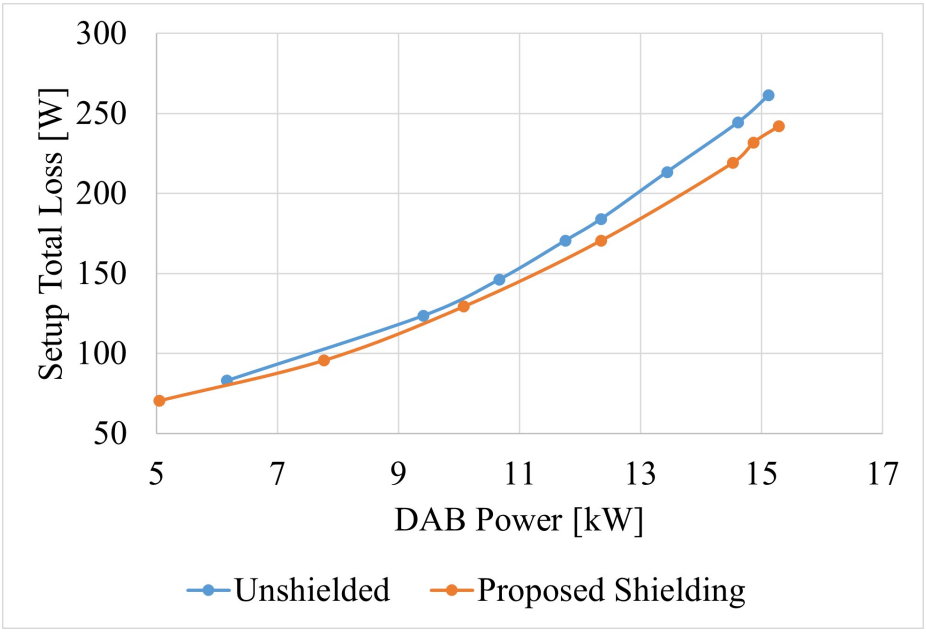


(c)

Fig. 3.12: Test results shell-type transformer: (a) thermal image without shielding; (b) thermal image with shielding; (c) loss comparison.



(a)



(b)

Fig. 3.13: DAB test for shell-type transformer (a) waveform, (b) loss comparison.

3.3 Summary

In this chapter, a novel ferrite shielding method to suppress eddy current loss on inductors and transformers using ribbon-based nanocrystalline/amorphous cores has been discussed.

- A new ferrite shielding scheme has been proposed for both gapped inductors and leakage integrated transformers using ribbon-based cores. The ferrite shielding is placed on the critical surface and extends with right angle to the sides of the cores to create stray magnetic path for each lamination layer. The mechanism of the proposed ferrite has been analyzed, showing that the stray flux can be redirected by the ferrite shielding structure from the ribbon-based cores into the air in a way with reduced eddy current loss.

- The proposed shielding ferrite technique has been implemented and validated in three cases: air gapped amorphous inductor, core-type nanocrystalline transformer, and shell-type nanocrystalline transformer. Through the simulation and test results, the proposed ferrite shielding can be verified to suppress the stray flux induced eddy current core loss, and the reduction can be more effective compared to the state-of-the-art techniques.

- It can be found through the test results that, in most cases the ferrite shielding is not saturated and can suppress the eddy current effectively. However, during the cases of high orthogonal flux density, the ferrite may be imposed to high

flux density and may cause partial saturation due to crowding in the corner or at the entire ferrite block. Therefore, the ferrite should be made thick enough to shield the flux and designed to work at below the saturation level. Further material optimization may be desired, so that a better material can be selected, such as magnetic paste [86].

Chapter 4

Dry-Type Insulation Design for MV Transformers and Inductors

4.1 Literature Review

The insulation becomes a key concern in MV transformers and inductors, as the high operating voltage is stressed on the converter hardware and the windings in the magnetic components. Over the years, many solutions have been proposed and implemented in the literature and industry products.

The first and most simple way of MV winding insulation is the air insulation. With sufficient turn-to-turn and inter-winding clearance in air, the insulation can be easily achieved. Ref. [10] designs a 200-kW medium frequency transformer, in which the two concentric windings are placed apart with an air gap of 18-19 mm, with poly-imide (PI) tapes and PEEK 3D printed bobbins placed onto the surfaces of

the two windings. The proposed transformer has been partial discharge tested up to 7.5 kV peak value at 60 Hz, verifying the proposed air insulation. One benefit of air insulation is that forced convection cooling can be applied directly on the surfaces of MV windings, and hence the cooling requirement can be lower than other methods. However, the air insulation faces a drawback since the insulation capability of air varies at different humidity, elevation, and atmosphere pressure. Enough margin and environmental control may be needed for air insulated magnetics.

Another type of insulation is oil or fluid emersed insulation. Oil-insulated magnetics are commonly used in the power system, thanks to the stable and high insulation capability of the transformer oil or similar dielectric liquid. The dielectric fluid, like air, while providing insulation for the transformer, can also serve as a heat transfer medium, enabling natural convection cooling within the oil tank. However, due to its relatively low heat capacity and high viscosity, the cooling performance is relatively inferior to that of air. Many medium voltage transformers are implemented with transformer oil. In [87], a group of traction DC/DC transformers are emersed in an oil tank and installed into a shunting locomotive by ABB. Ref. [88] built a DC/DC-based high voltage generator with oil-insulated transformers. In the transformer design, oil barriers and field shaping are also implemented to further improve insulation quality. A MW-level medium frequency transformer is built in [89], and only the copper pipe based windings are placed in an oil vessel for both insulation and cooling consideration. A multi-winding medium frequency transformer is designed in [90], in which the insulation performance of the bushing and oil gasket

structures are also considered, and fin structures are manufactured on the outer surface of the tank for forced air cooling from the outside of the transformer oil tank.

Due to the possible flammability of the transformer oil, the dry-type insulation is preferred thanks to its high insulation performance and better chemical stability. Ref. [12] introduces a transformer with casted silicone and epoxy to improve the insulation performance, and the MV winding was coated with a shielding layer to confine the electric field in the dielectric material inside the MV winding, so that the low voltage winding does not need to be encapsulated and has better cooling behavior. In [61], 10 kV SiC device-based resonant DC/DC converter is designed and implemented with silicone elastomer potted MV transformer, achieving single conversion from 7 kV to 400 V. In [91], a GaN/SiC-based converter for the data center was proposed, by increasing the switching frequency up to 500 kHz the transformer volume becomes small enough, and in [71], the dry-type insulation is further simplified as a thick customized PCB, eliminating the complicated process of encapsulating. As the switching frequency is high, the issues of skin and proximity effects have to be addressed to ensure the high conversion efficiency. In [72, 16] a Litz wire structure implemented in PCB copper layers has been introduced.

There also have been many insulation concepts other than the traditional solution. For example, a cable-based co-axial insulation structure can be realized by high voltage cables where the internal conductor serves as one continuous winding, while the shielding/grounding layer in the cable serves as the other set of winding. Hence,

the dielectric barrier of the cable becomes the insulation layer of two windings, while the turn ratio is limited as unity due to the structure of the cable [92]. In [93], apart from utilizing cable structure for the unity-ratio winding, the internal winding is also manufactured as hollow for liquid cooling channel, and therefore the cooper loss can be easily dissipated by the liquid cooling. Another typical solution is to leverage from the concept of wireless power transfer (WPT). By placing a long gap between the two windings and adjacent halves of cores, the insulation requirement between the winding and core halves can be reduced [14]. Therefore, a potential insulation volume reduction can be found when the switching frequency is high enough and suitable for the WPT-like magnetic structure.

There are also challenges on realizing or associated with the aforementioned insulation methods. As stated in [12], the high viscosity of the liquid encapsulant can be a hurdle to achieving high-quality dry-type insulation, as with a higher liquid viscosity of the liquid, the harder it is to fill in the small gaps inside or on the surface of the MV winding structures. Consequently, the voids inside of the imperfectly encapsulated winding may generate partial discharge and potentially damage the dry-type insulation in the long run. Therefore, Ref [12] used combined structure that the silicone gel is firstly potted with the Litz wire, while the epoxy is applied on the outside of the gel. Since silicone gel are soft and low viscous, the small gaps around Litz wire can be easily filled. Then, the high viscous epoxy can be potted in the outer layer for better thermal conduction. In [61], a vacuum pressure potting process is introduced, where the silicone elastomer liquid is de-gassed in vacuum chamber,

and then applied to the MV winding case through piping to provide better degassing process.

Parasitic capacitance can be a concern with high voltage insulation due to the high voltage energizing, high frequency excitation, and the high dielectric constant introduced by the dielectric material. Especially for the shielded MV windings, high grounding capacitance can be found due to the electric field confinement [94]. By implementing selective shielding, with which the winding surface with core window area can be shielded with semi-resistive coating, and the other surfaces can be coated with high resistive coating, so that the common-mode (CM) current can be limited by the resistivity of the shielding layer. The termination of the shielding layer is usually sharp, and hence in [15] and [91], the shielding layer edges are either potted with silicone gel or wrapped with high dielectric constant tapes to grade the high concentration of electric field.

Although the most of the key parts of insulation have been discussed in the existing literature, insulation design can still be challenging due to different requirements on high voltage rating, converter topologies, cooling, power density, etc. Hence, further study is continuously needed to further improve the existing methods and address the corresponding insulation-associated issues, such as potting process, parasitics control, and cooling.

4.2 Characterization of Insulation Materials

In Dry-type insulation, the material properties, especially the dielectric properties, play important roles. Since the potential drop and electric field distribution are mainly imposed on the solid body of the dry-type encapsulation structure, the dielectric constant will determine the field strength distribution along with the transformer winding geometry, while the dielectric strength will affect the actual thickness needed of each insulation layer and the margin of the whole insulation design. In this chapter, two dielectric material are considered in use for dry-type MV winding insulation, i.e., *Rigid 10K* from Formlabs as mechanical structural material and *TC-4605 HLV* from Dow Corning as silicone elastomer for encapsulation.

4.2.1 Mechanical Structural Material

The mechanical structural material mainly serves as the mechanical support and containing material in the dry-type insulated windings. The structural material of *Rigid 10K* is to be 3D printed into winding bobbins, spacers, and the winding cases, with 3D printer *Form 3L* from the same company. As shown in [95], it is a glass-filled photopolymer resin that can withstand 163°C, and have a dielectric constant of 3.4 at 1 GHz, while the dielectric strength is 458 V/mil (18.5 kV/mm).

To test and verify the insulation performance of the 3D printing material, insulation (PD and Hi-Pot) tests have been performed. First, a test sample is designed to provide an accurate insulation thickness 3D-printed using the 3D printing material,

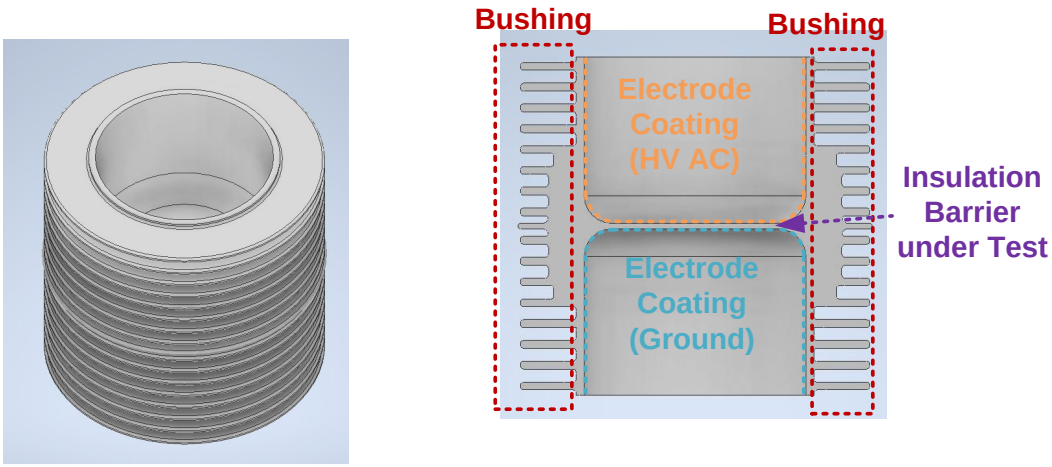


Fig. 4.1: Designed insulation test sample for the 3D printing material, (a) perspective, (b) Cutaway view with features.

and the dedicated surfaces are coated with conductive copper paint as the electrodes for high voltage terminal and ground. Finally, the fabricated insulation test sample is plugged into the high voltage test platform for insulation testing. **Fig. 4.1(a)** shows the mechanical design of the 3D-printing material test sample, with the cutaway in **Fig. 4.1(b)** showing the designed insulation barrier with 3D printing material under test, the electrodes by copper coating, and the bushing to avoid surface discharge. The corresponding simulation result is shown in **Fig. 4.2**, and with a terminal excitation of 30 kV, the insulation barrier of 3D printing material has an approximately evenly distributed electric field with maximum field strength of 33 kV/mm for a 1-mm barrier, and the corners have no field concentration thanks to the rounded edges.

After the design and simulation are validated, insulation samples are 3D printed and coated. A sample is shown in **Fig. 4.3(a)**, and the PD test waveform is shown

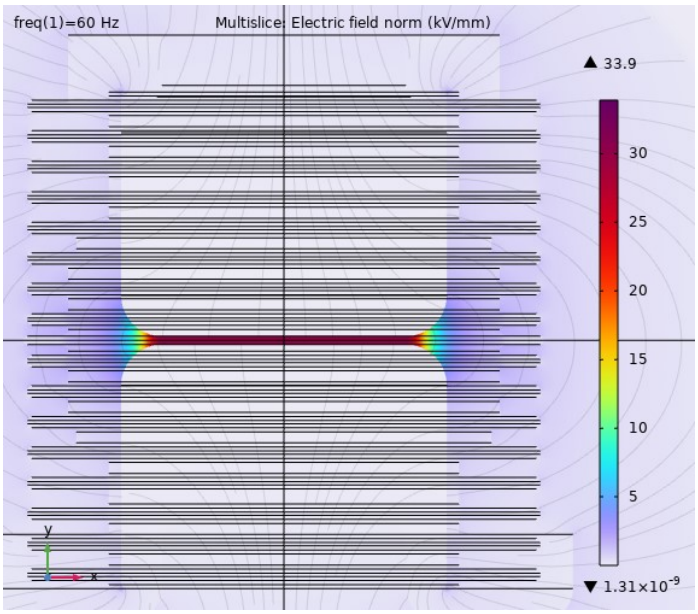
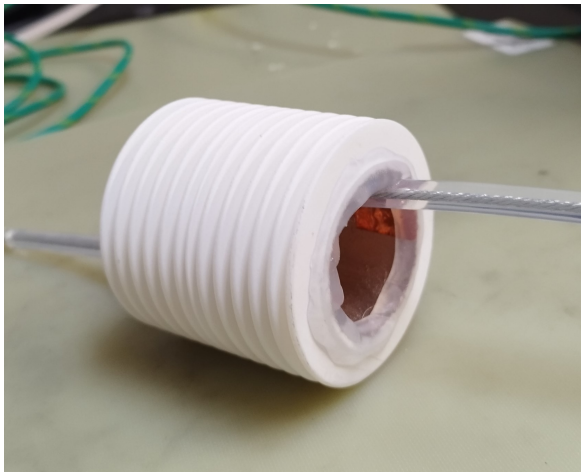


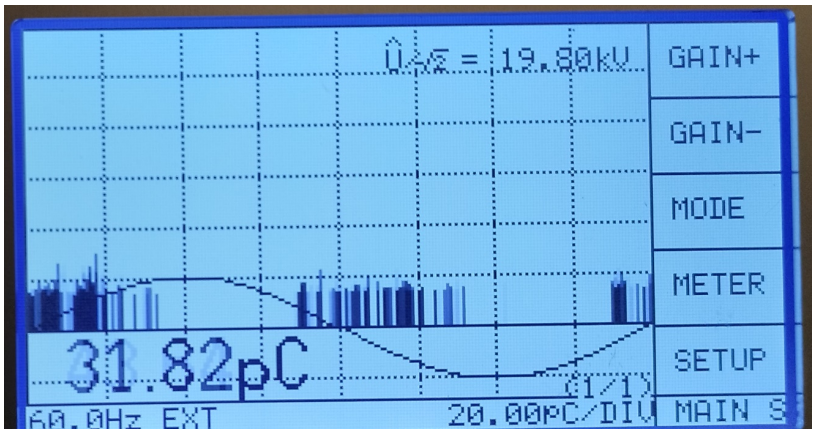
Fig. 4.2: Electric field simulation of the 3D printing insulation sample.

in **Fig. 4.3(b)**. The results of the PD test showed that no PD can be observed below 19 kV (RMS) for the test samples, and the PD incepted at around 19 kV. As the voltage increases above 19 kV, the PD charge value increases rapidly, from initially from tens of pico-coulomb (pC) to nano-coulomb (nC) level, and the barriers broke down at above 21 kV (RMS), and some samples could withstand up to 30 kV (RMS). The break down point can be clearly found in the testing samples (see **Fig. 4.3(c)**), and the burnt mark can verify that the dielectric break down happened in the tested insulation barrier. Therefore, the inception electric field strength of PD for this material is around 19 kV/mm (27 kV/mm in peak value), and the dielectric strength is above 21 kV/mm (30 kV/mm in peak value).

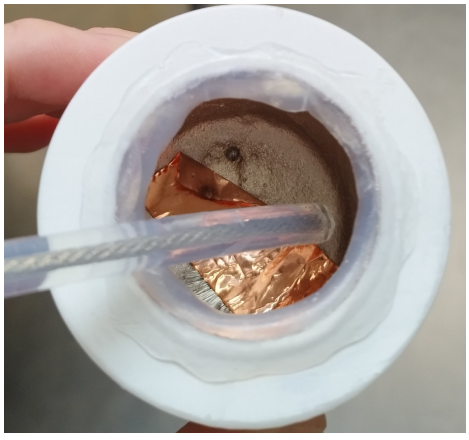
The thermal conductivity of this material has also been tested as 0.29 W/mK.



(a)



(b)



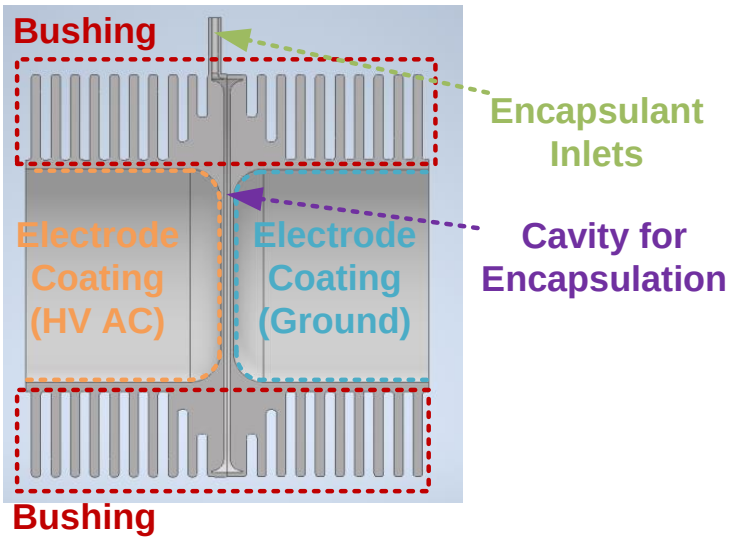
(c)

Fig. 4.3: Insulation test results of the 3D printed insulation sample, (a) photograph of the sample under test, (b) PD waveform, and (c) photograph of a sample after dielectric breakdown.

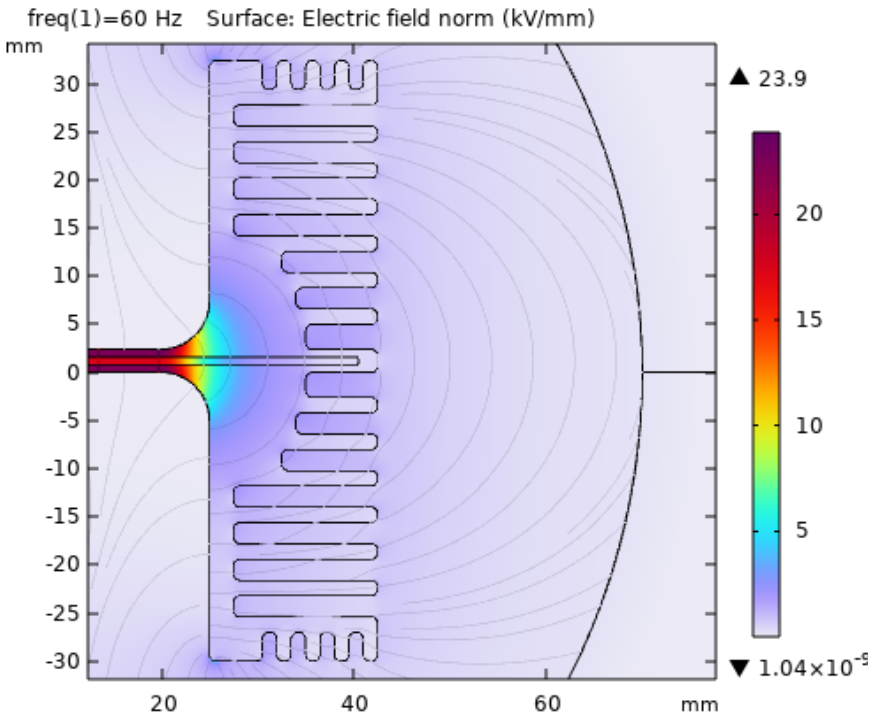
4.2.2 Combination of Encapsulant and Structural Materials

As the insulation performance of the mechanical structural 3D printing material has been verified, further tests can be performed to test the encapsulant and the combination of materials in the encapsulation. As stated in [96], the selected encapsulant *TC-4605 HLV* has a dielectric strength of 24 kV/mm, thermal conductivity of 1 W/mK, and Ref. [66] tested that the dielectric constant to be ¡4.1 at above 50 kHz. With this information, another test sample is also designed to test the performance of the material combination of the mechanical support and encapsulant materials.

The designed test sample for material combination is illustrated in **Fig. 4.4(a)**. resembling the mechanical support test sample, the new sample features bushings and conductively coated electrodes considering the high voltage test, whereas the insulation barrier under test is a combination of the two materials - inside is a 1-mm thick cavity for the encapsulation of silicone elastomer, with two sides of 0.5-mm each thin 3D printed walls to confine the encapsulant material. In addition, liquid inlets are added to the sample to allow the encapsulant liquid to flow in. A corresponding simulation result is shown in **Fig. 4.4(b)**, showing that due to the difference of the dielectric constant, the electric field is unevenly distributed between the 3D printing material and the encapsulant. As the 3D printing material has lower dielectric constant, the electric field strength becomes higher, while the silicone elastomer encapsulant shares less field strength. The designed structure can also render the electric field to be evenly distributed.



(a)



(b)

Fig. 4.4: Designed insulation test sample for the material combination, (a) 3D drawing of the cutaway view, (b) Simulation results.

The new test sample is then 3D printed and fabricated with vacuum potting process, and the fabricated sample is shown in **Fig. 4.5(a)**, and the PD waveform is shown in **Fig. 4.5(b)**, with the voltage is applied up to 14.7 kV, the PD starts to happen inside the sample. Therefore, the averaged PD inception field strength can be derived for the material combination as

$$E_{PDI,avg} = \frac{V_{AC}}{d_{barrier,tot}} = 7.4 \text{ kV/mm} \tag{4.1}$$

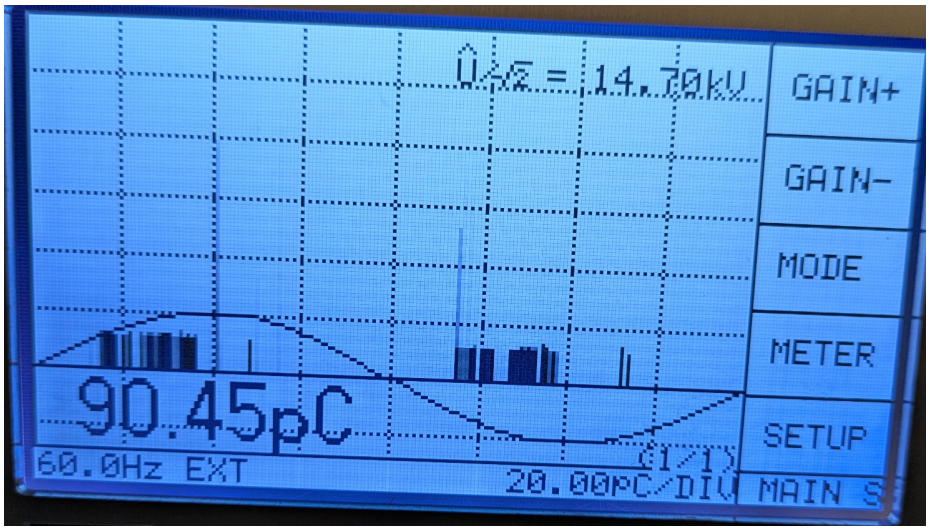
where, the V_{AC} is the applied voltage, and $d_{barrier,tot}$ the total insulation barrier thickness, which is 2 mm. Then the field strengths in the two materials are

$$\begin{cases} E_{PDI,3D} = E_{PDI,avg}\dfrac{\epsilon_{Silicone}}{\epsilon_{3D}} = 9.8 \text{ kV/mm} \\ E_{PDI,Silicone} = E_{PDI,avg}\dfrac{\epsilon_{3D}}{\epsilon_{Silicone}} = 5.6 \text{ kV/mm} \end{cases} \tag{4.2}$$

where, the ϵ_{3D} is the dielectric constant of the 3D printing material, and $\epsilon_{Silicone}$ the dielectric constant of the encapsulant. All the field strengths and voltage are RMS value, and hence the peak value for the partial discharge inception field strengths are 13.8 kV/mm for the 3D printing material, and 7.9 kV/mm for the encapsulant. The value is lower compared to the 3D printing material test result and the encapsulant datasheet, which is caused by the imperfect encapsulation process and potential material interface issue at the material contacting interface between the two materials.



(a)



(b)

Fig. 4.5: Insulation test results of test sample for the material combination, (a) photograph of the sample, (b) PD test waveform.

Additionally, the thickness of the cavity may also have loose tolerance due to 3D printer deviation and mechanical assembly.

The breakdown of the testing sample is also tested as above 35 kV RMS, and therefore the dielectric strength of the two materials, should be above

$$\begin{cases} E_{br,3D} > \dfrac{V_{br,AC}}{d_{barrier,tot}} \dfrac{\epsilon_{Silicone}}{\epsilon_{3D}} = 23 \text{ kV/mm} \\ E_{br,Silicone} > \dfrac{V_{br,AC}}{d_{barrier,tot}} \dfrac{\epsilon_{3D}}{\epsilon_{Silicone}} = 13.1 \text{ kV/mm} \end{cases} \tag{4.3}$$

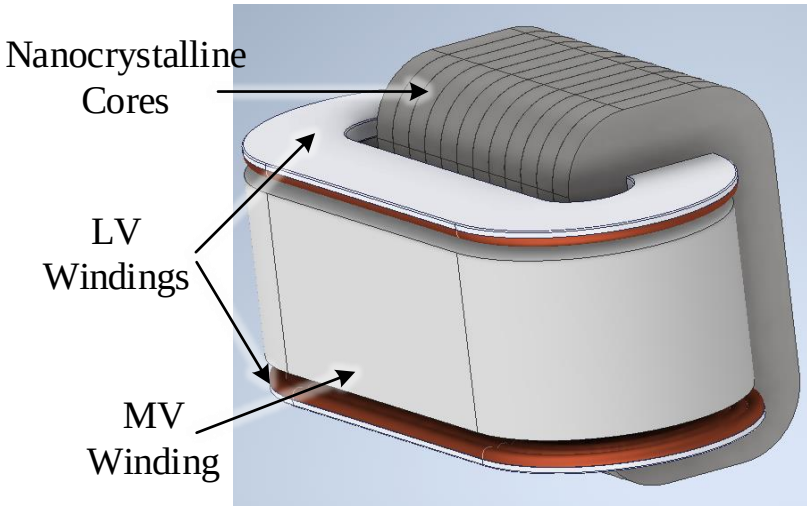
where, $V_{br,AC}$ is the voltage of the AC RMS at the breakdown. Similarly, the breakdown strengths for the combined insulation in peak values are 32.5 kV for the 3D printing material, and 18.5 kV/mm for the encapsulant.

4.3 Dry-Type Winding Insulation Structure

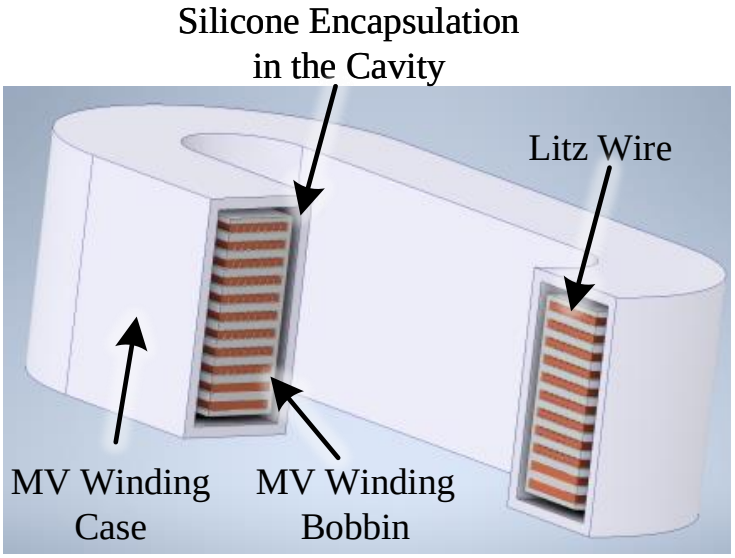
With the grasp of dielectric properties of the materials, the insulation structure for MV windings in MV magnetics can be designed. In this section, MV windings for DAB transformers and DC/AC inductors rated at 6-7 kV (peak) between MV winding terminals and 12-13.4 kV (peak) to ground are discussed.

4.3.1 Structural Design of Dry-Type Winding

Fig. 4.6(a) shows the structure of the MV transformer considered for the MV DAB converter. The magnetic structure has already been depicted in **Fig. 2.5** and



(a)



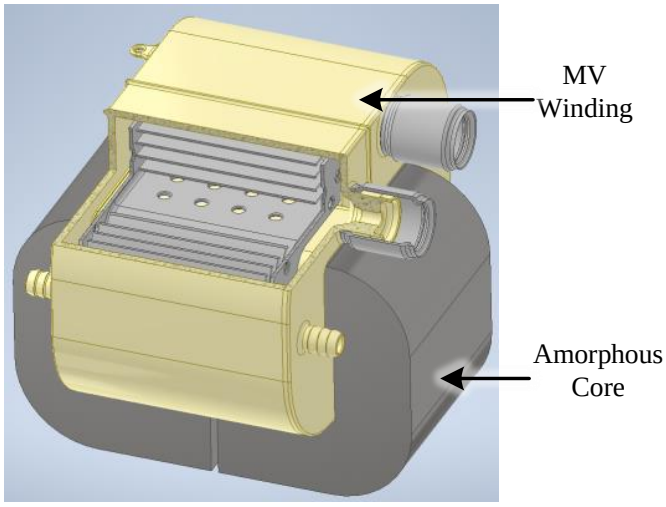
(b)

Fig. 4.6: Mechanical Drawing of a MV DAB transformer, (a) structure of the MV transformer, (b) structure of the MV dry-type winding [27].

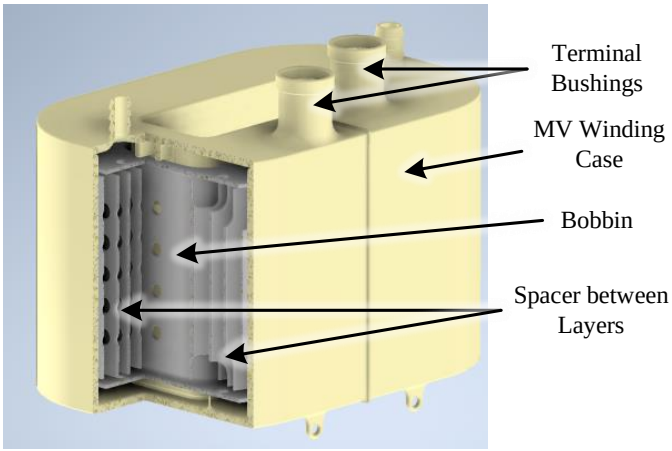
Fig. 2.9(b), while the MV winding is with dry-type insulation. To achieve a compact design and reduce thermal stress, only the MV winding is encapsulated with dry-type insulation, while the LV winding and transformer cores are exposed to the air with forced air convection cooling. Therefore, only the heat generated by the MV winding needs to be dissipated across the insulation material, which has only thermal conduction for dissipation and also relatively low thermal conductivity as discussed previously.

The MV winding is comprised of three parts, i.e., the Litz wire, the 3D printed winding case, the bobbin, and the silicone elastomer filled inside the winding cavity [97], which is illustrated in **Fig. 4.6(b)**. In order to confine the electric field inside of the MV winding and avoid discharge onto the other components, the MV winding is selectively shielded with conductive coating on the surfaces facing the transformer core and LV windings [19].

Similarly, a MV Inductor design is illustrated in **Fig. 4.7(a)**, using MV dry-type insulation in MV winding and the amorphous magnetic core of *AMCC 1000*. The inductance designed is 2.5 mH, and winding consists of 56 turns of 329/AWG33 Litz wire (equivalent to AWG8). **Fig. 4.7(b)** illustrates the detailed structure of the dry-type insulated winding, with the 3D printed MV winding case to hold the structure and silicone elastomer encapsulant, bobbins and spacers for different layers of winding, terminal bushings, and the cavity for silicone encapsulant to fill.



(a)



(b)

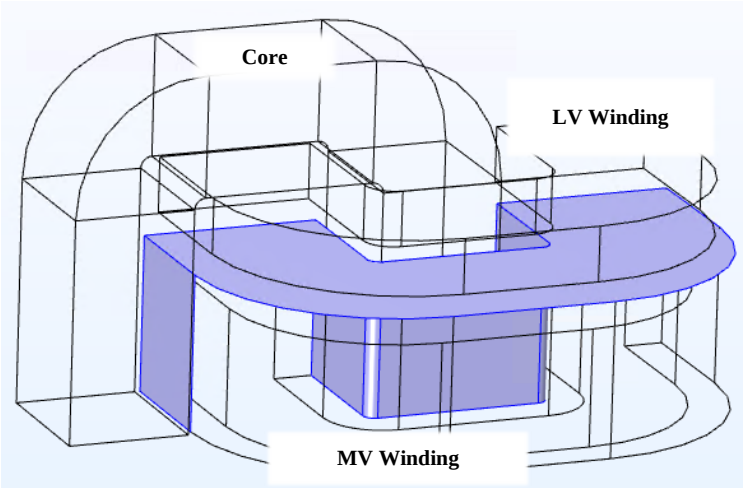
Fig. 4.7: Mechanical Drawing of a MV inductor, (a) structure of the MV inductor, (b) structure of the MV dry-type winding.

4.3.2 Partial Shielding and Field Grading

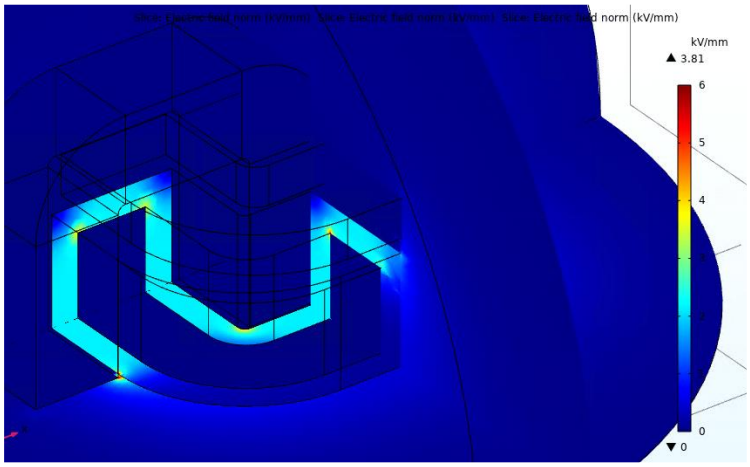
Winding Partial Shielding

CM capacitance can always be a concern for high voltage power converters, as the high voltage stress and high frequency switching can cause high CM current and more switching losses [20, 31]. A selective shielding method has been proposed in [94], only the critical surfaces are close to the ground potential should be shielded with higher conductivity, as the ground and high potential difference may impose a high electric field in the air, causing corona or flashover discharge during operation, while the other surfaces can be resistively shielded to reduce CM current. The selective shielding can reduce the CM current as the resistance of grounding loss is increased by the resistive shielding, while the parasitic capacitance is not reduced since the equivalent electrode surface area is not reduced. Hence, a partially shielded transformer has been considered in **Fig. 4.8(a)**. The field distribution is only partially evenly distributed due to that the shielding is only on selected surfaces, and the electric field extends to the air where the surface is not shielded. With partial shielding, the capacitance between the high potential winding and shielding ground is 102 pF, which is reduced by 50% compared to the fully shielded winding with 216 pF.

As the electric field partially leaks into the air via non-shielded surfaces,analyzing its distribution near adjacent objects is essential to prevent unintended discharges. **Fig. 4.9(a)** illustrates a simulated case involving a partially shielded MV winding and a PCB for the low-voltage power stage, which is positioned 80 mm away from the

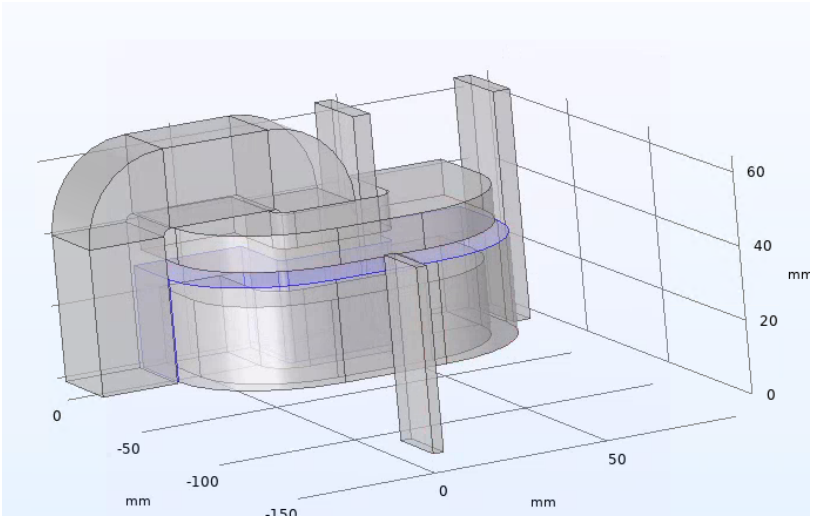


(a)

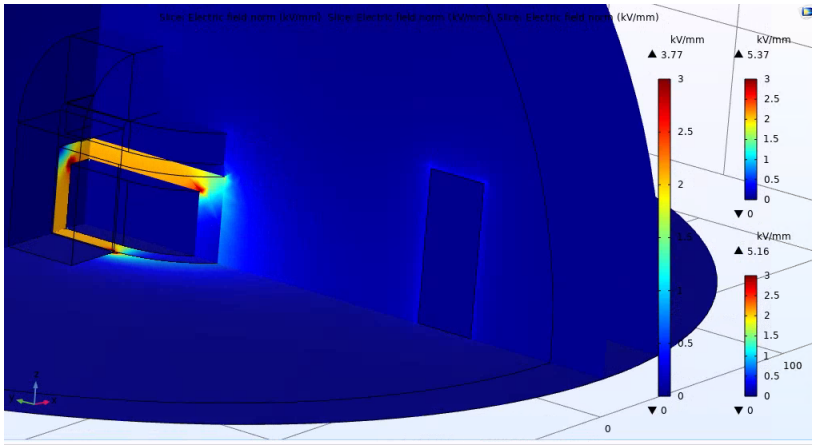


(b)

Fig. 4.8: Partial shielding of a MV winding, (a) structure of the partially shielded MV transformer with highlighted surfaces to be shielded, (b) simplified simulation of the MV transformer.



(a)



(b)

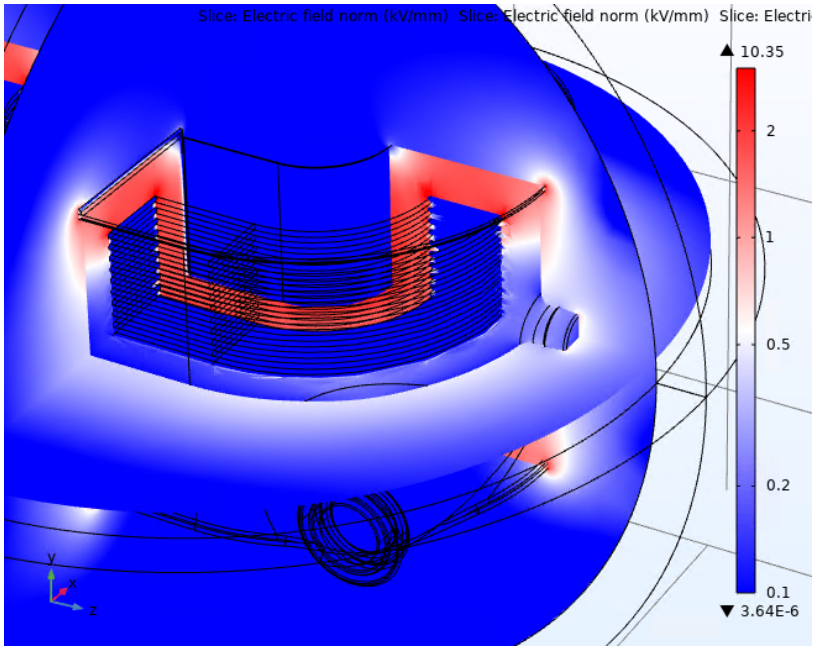
Fig. 4.9: Electric field distribution of the partially shielded winding and a grounded PCB at a distance of 80 mm.

MV winding. The MV winding is set to have a potential of 15 kV while the low-voltage power stage is set to ground potential for simplification. It can be found in **Fig. 4.9(b)** that beyond the dry-type insulation, the electric field mainly concentrates on the surface of the MV winding and PCB edges, and the electric field is approximately 1 kV/mm and below the dielectric strength of the air (3 kV/mm).

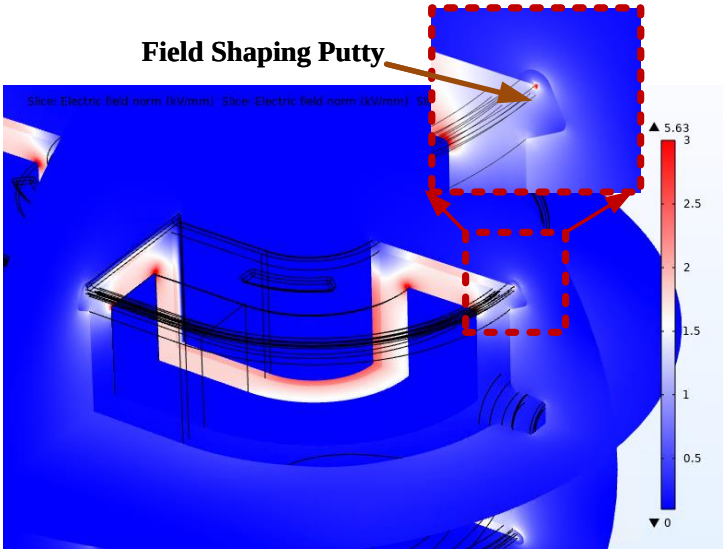
Field Grading at Shielding Termination

The electric hot spot now is at the edges or terminations of the shielding layer, which could be as high as 6 kV/mm and may cause a breakdown in the air. The hot spot on the shielding termination can be reduced by applying silicone putty. The silicone putty can withstand electric field of 550 V/mil (21.65 kV/mm), and dielectric constant of 3.03. The applied silicone putty forms a rounded corner with low curvature in the real prototype, and the dielectric constant also helps redistribute the electric field. The detailed simulation with the silicone putty is shown in **Fig. 4.10(a) and (b)**. Without high voltage silicone putty, the voltage stress at the shielding termination can easily exceed 3 kV/mm and approaching 10 kV/mm. By applying silicone putty, the field strength can be reduced to 1.5 kV/mm on the edges of the shielding surfaces. The hot spot of electric field at the shielding edge termination is confined as only one small spot and the field strength can be reduced to 5.63 kV/mm.

As the silicone putty is applied by hand, imperfection such as voids or contamination may occur within the putty structure. Simulations are also performed to investigate the impact with the undesired imperfectness. **Fig. 4.11** shows the

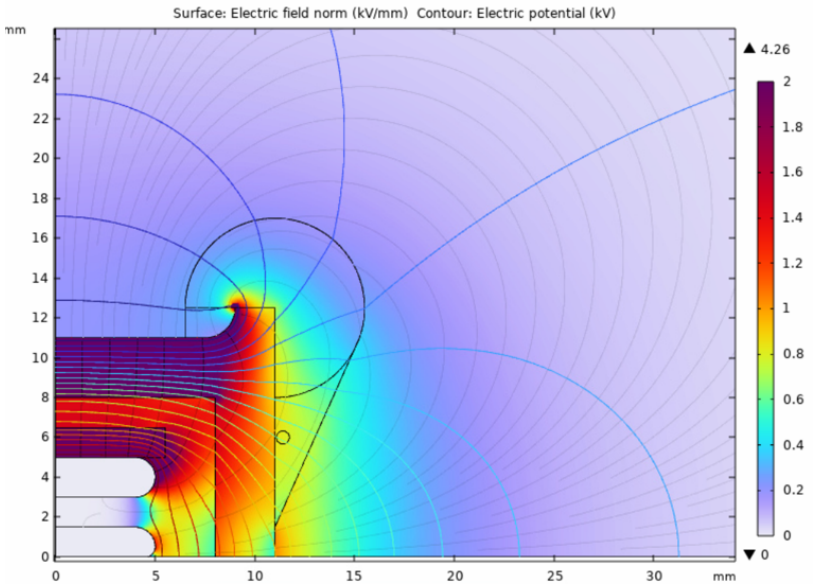


(a)

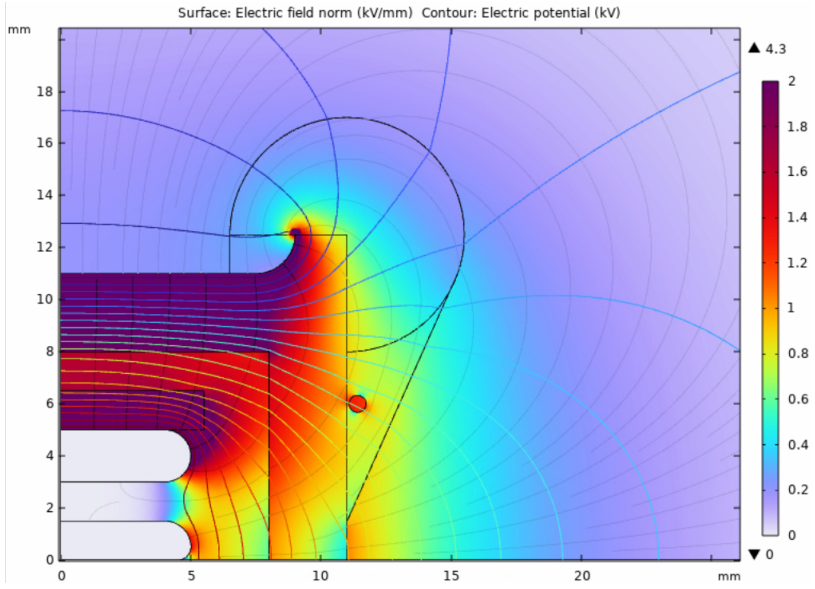


(b)

Fig. 4.10: Simulation results of the partially shielded MV winding, (a) without high voltage putty, (b) with high voltage putty and zoomed-in zone of high voltage putty.



(a)



(b)

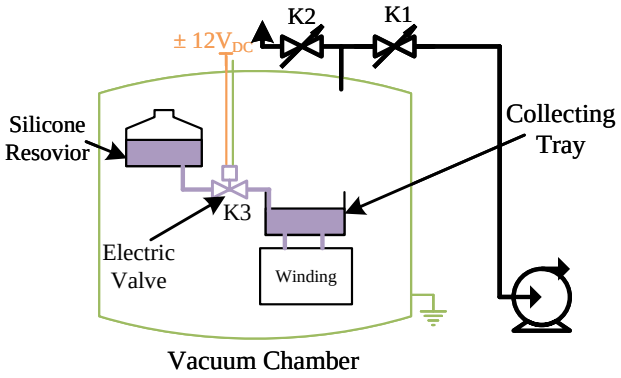
Fig. 4.11: Simulation results of the high voltage putty covered area, (a) without voids, (b) with void.

simulation results of the shielding termination and silicone putty. In **Fig. 4.11(a)**, the electric field is normally distributed as no voids are inside the silicone putty, while in **Fig. 4.11(b)**, a red dot can be found as a void occurs in the putty, and the putty void has a electric field strength below 2 kV/mm at rated voltage, which can be confined by the dielectric strength of the air and will not cause PD issue. Therefore, the voids inside silicone putty may cause high concentration of electric field at the spot of void, and if the putty is applied with care and the voids are small enough, no PD issue will be found at the void spot.

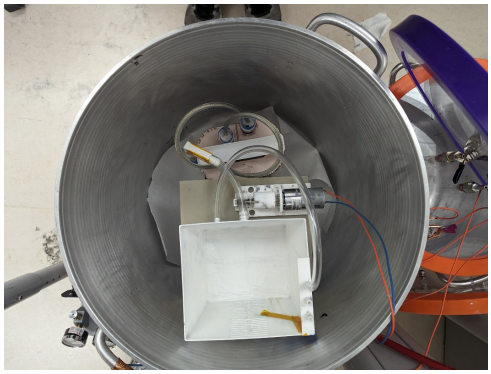
4.4 Dry-Type Encapsulation Procedure

For dry-type insulation, the encapsulation procedure is an important process, as the quality of the encapsulation process will immediately impact the quality of encapsulation and the insulation performance. If the encapsulation is performed with contamination and inadequate degassing, voids and contamination will be formed inside the insulation body, which may cause partial discharge in during the PD test and actual operation. In this section, an improved vacuum-pressure encapsulation process is introduced that is similar to the one proposed in [61], but with only one chamber and fewer tubing and feedthroughs to simplify the process while ensuring encapsulation quality.

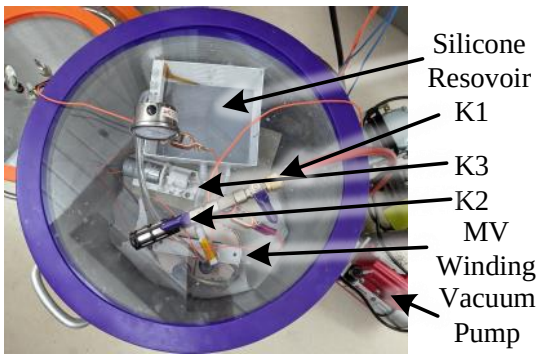
Fig. 4.12(a) illustrates the schematics of the encapsulation set-up: the vacuum pump retracts air from inside of the vacuum chamber to create a vacuum environment;



(a)



(b)



(c)

Fig. 4.12: The equipment for vacuum pressure encapsulation process, (a) the schematic diagram, (b) photograph of the vacuum chamber, and (c) photograph of the set-up.

the silicone reservoir stores liquid encapsulant during the early stage of de-gassing; the electric pinch valve K3 controls the liquid flow to the winding; the winding has a collecting tray to ensure that the encapsulant overfills the winding with the effect of gravity; the electric valve can be controlled electrically either directly by 12-V wire connections through metal feed-throughs installed on the lid for air tubing and gauge, or by 12-V wire connection and a Raspberry Pi controller through Wi-Fi connection. **Fig. 4.12(b) and (c)** show the tubing and wiring of the actual setup.

The procedures for the vacuum potting should be as follows:

1. Prepare all the parts: silicone reservoir, valves, tubing, and the vacuum pump, and then close the chamber lid.

2. Close K2 and K3, open K1, and turn on the vacuum pump to draw air from the chamber.

3. Monitor the pressure gauge on the chamber lid, and wait for the silicone to be de-gassed, and also estimate the time allowed for silicone to flow and fill the MV winding.

4. When the gas bubble subsidies or reduces to reasonably low, open the K3 valve by external power supply or attached Raspberry Pi, and let the liquid flow and fill the winding.

5. When the Winding is almost filled, close K3 and K1, and turn on K2 to re-pressurize the chamber to the room atmosphere. The re-pressurization can help

on encapsulant impregnation into the Litz wire structures through the yarn. The pump can be turned off as not needed in this step.

6. Close K2, open K1 and turn the pump back on to regain deep vacuum environment as the previous de-gassing stage.

7. When the desired deep vacuum is reached, re-open K3 to overfill the winding to one-third depth of the collecting tray.

8. When the target liquid depth is reached, close K1 and K3, turn off the pump, and open K2 to finally pressurize the chamber to the air atmosphere.

9. Open the chamber lid, remove the tubing from the winding and tray. Heat-cure the encapsulated MV winding with the collecting tray as needed.

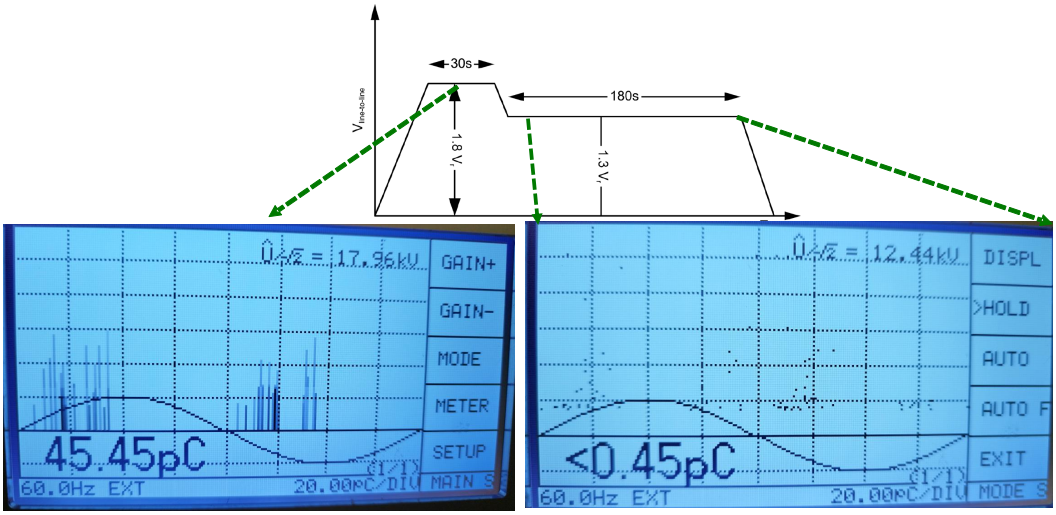
With the proposed vacuum process, the deepest vacuum achieved is approximately 7.5 mbar measured by the Raspberry Pi controller and pressure sensor embedded into the vacuum chamber. The proposed procedure has to be finished within the pot life of the encapsulant to avoid unwanted early curing during the vacuum process, and therefore a deep vacuum is needed to de-gas the liquid quickly.

4.5 Partial Discharge Test Validation

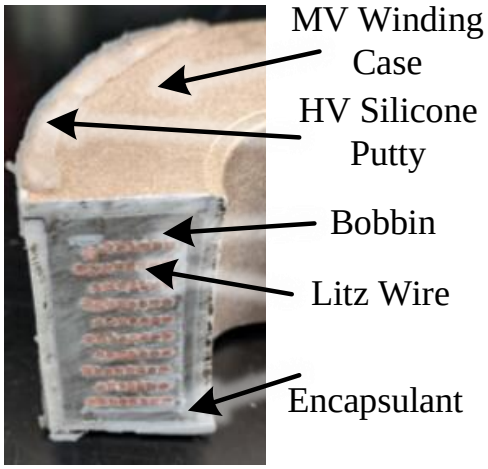
With the introduced dry-type insulation structure and proposed partial shielding and field grading techniques, a DAB transformer winding as shown in **Fig. 2.9(b)** has been fabricated for PD testing. The applied voltage follows the *IEEE Standard Test*

Code for Dry-Type Distribution and Power Transformers [98], which is depicted in **Fig. 4.13(a)**. The AC high voltage is applied between the MV terminals and the shielding layer (grounded), and the nominal insulation voltage is 9.5 kV RMS (13.4 kV peak of two cascaded 6.7-kV units). Firstly, the voltage is pre-stressed up to 1.8 times the nominal voltage for 30 seconds, and then the PD discharge is recorded at 1.3 times the nominal voltage for 3 minutes. As shown in the results, at the pre-stress stage, the PD level is around 45 pC, and after the 3 minutes of recording at 1.3 times nominal voltage, only small and rare PD has been spotted and most are below 60 pC, which means the proposed transformer has passed the PD test. A prototype has been cut to demonstrate the detailed insulation structure with the dry-type insulation structure and the proposed field grading. The bobbin holds the Litz wire in position, while the encapsulant successfully filled the all the gaps and corners inside the winding cavity, and the shielding coating covers the critical area.

Similarly, PD test has also been performed for the MV inductor (see **Fig. 4.14(a)**). The MV inductor will be used at a 1-MW AC/DC converter for 13.8 kV microgrid, and therefore the nominal voltage would be the DC-link to ground voltage, i.e., 12 kV peak, and 8.5 kV RMS for 60 Hz AC with equivalent peak value. The result of the PD test is shown in **Fig. 4.14(b)**. At stress of 1.35 times the nominal insulation voltage, the PD level is within 50 pC. Hence, the proposed MV inductor winding can also pass the PD test.

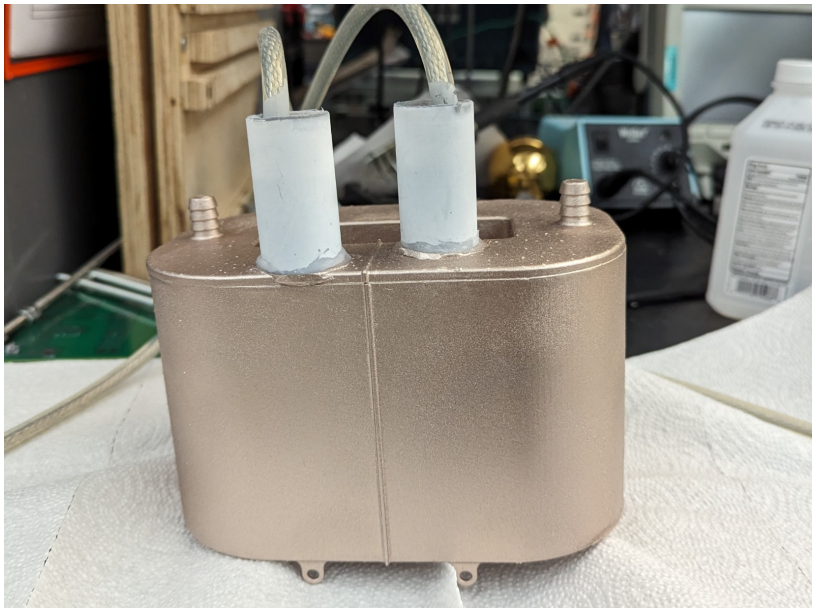


(a)

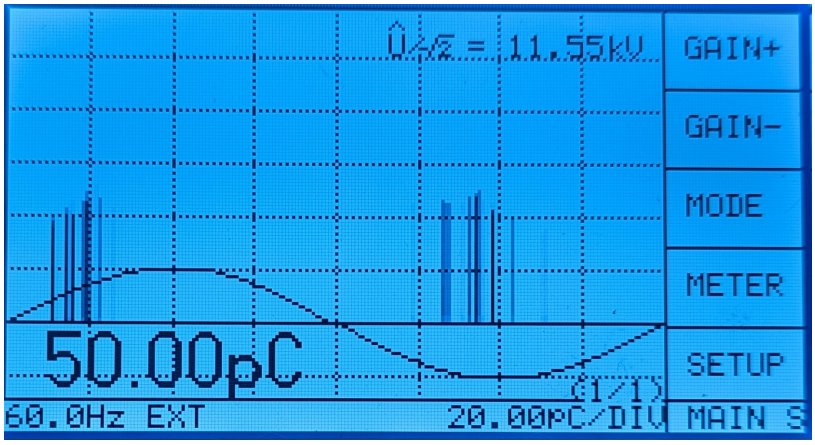


(b)

Fig. 4.13: The MV transformer winding, (a) PD test waveforms, (b) prototype cut-away photo.



(a)



(b)

Fig. 4.14: The MV inductor winding, (a) photo, (b) PD test waveform.

4.6 Validation in Converter Testing

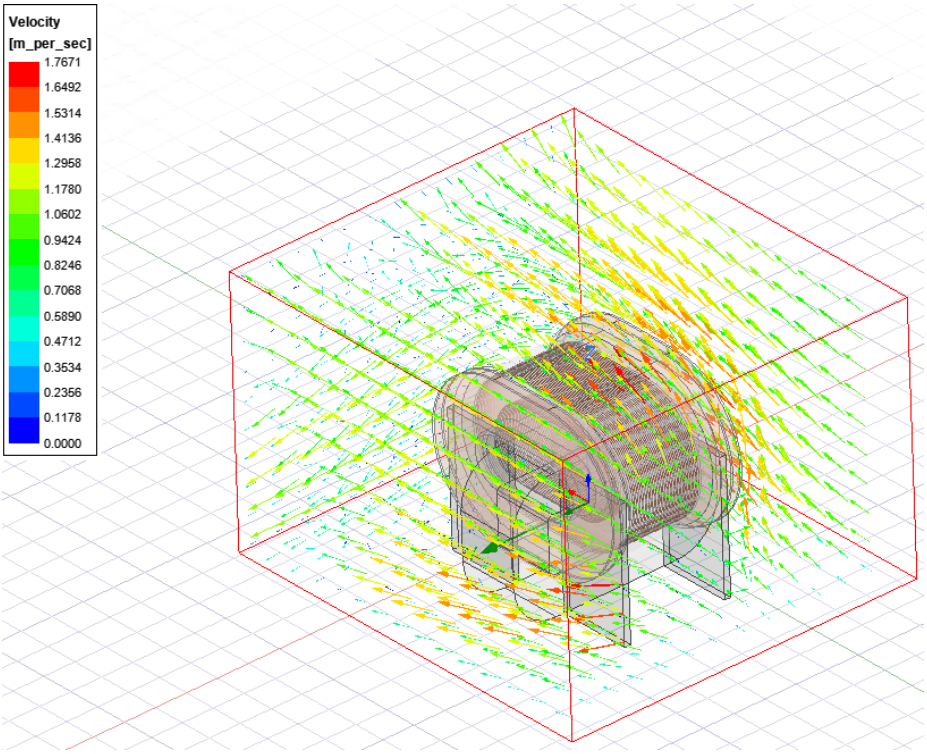
After the PD tests validated the MV winding design, the MV transformers and inductors have been installed into DAB and flying capacitor AC/DC converters for MV converter tests. The converter testing ultimately verifies the insulation design with actual converter operating voltage stress.

4.6.1 MV Transformer Test in DAB Converter System

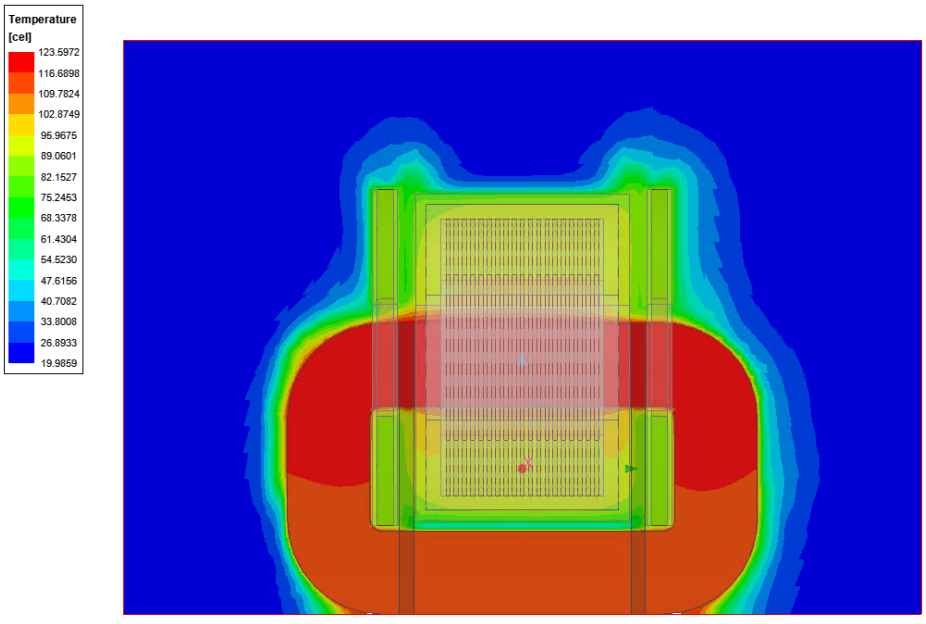
The MV transformers are installed in the DAB and CHB converter systems depicted in Fig. **2.9**, and the design metrics are listed in **Table 2.1**. The DAB has been tested up to full voltage and full load, and the waveforms are shown in **Fig. 2.11**. The DAB transformer is cooled with a slight airflow around 1 m/s from the air duct of the MV power stage. The corresponding results of thermal simulation are shown in **Fig. 4.15**. The thermal image is recorded during the test, and is depicted in **Fig. 4.16**. As is shown in **Fig. 4.16**, the hot spot is mainly on the transformer core due to high core loss, while the outer surface of the MV winding is around 50℃, which is similar as in **Fig. 4.15**.

4.6.2 MV Inductor in Flying Capacitor Converters

MV inductors are also built and installed into a 1-MW 8-level flying capacitor converter (FCC), and the photograph of the converter setup is shown in **Fig. 4.17**, the converter metrics is listed in **Table 4.1** [28]. The 8-L FCC has been tested up to

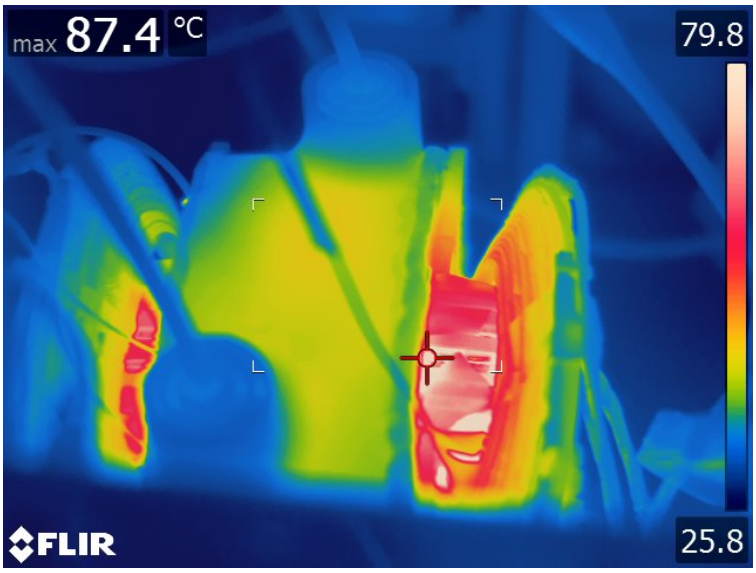


(a)

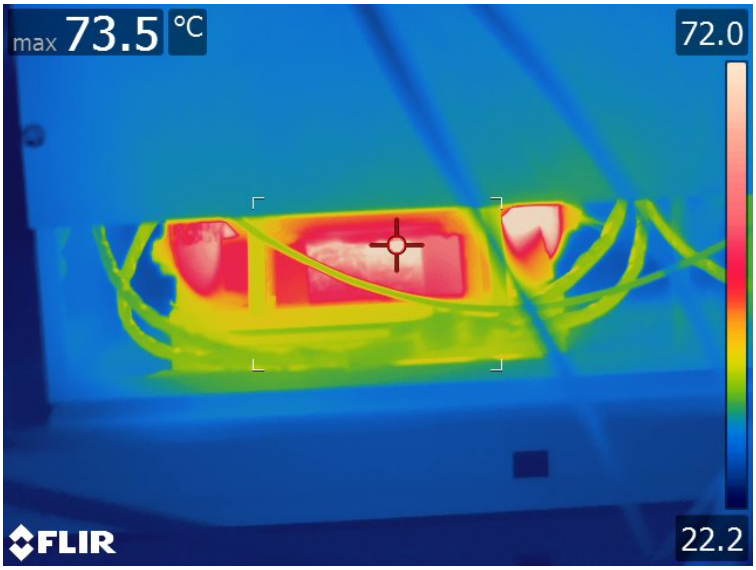


(b)

Fig. 4.15: Thermal simulation of the DAB transformer: (a) air flow, (b) temperature distribution.



(a)



(b)

Fig. 4.16: Thermal images of the DAB transformer: (a) top view, (b) side view.

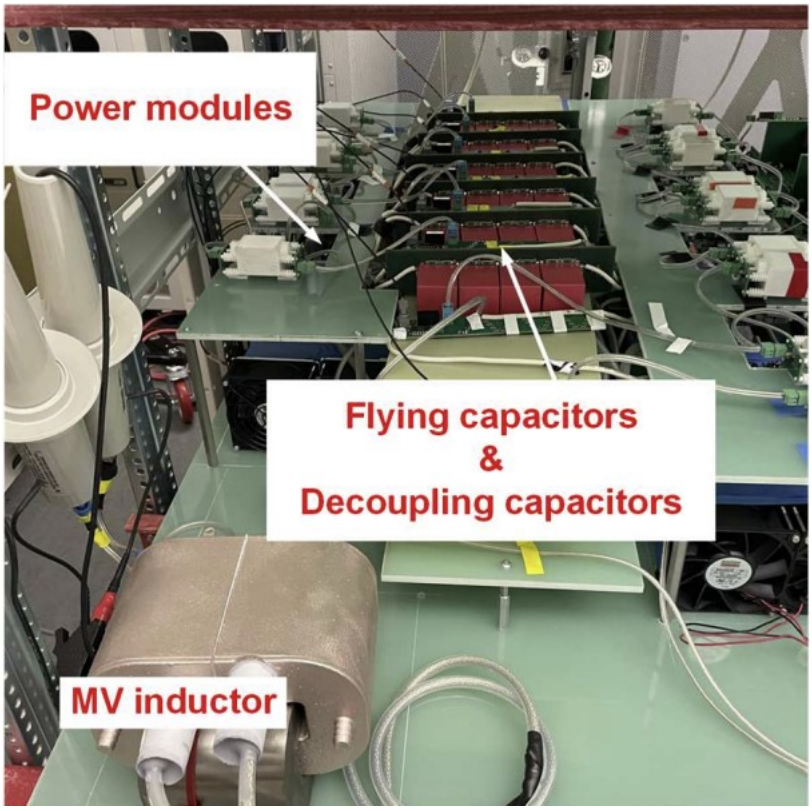


Fig. 4.17: Photo of the 8-Level flying capacitor converter [28].

Table 4.1: Metrics of MV Flying Capacitor Converter and Its Inductor

Parameters	Values
Power Rating (3-phase)	1 MVA
AC Output Voltage	13.8 kV (3-phase)
DC-link Voltage	22 kV
Switching Frequency	5 kHz
Filter Inductance Value	2 mH
Inductor Winding	64 turns of 329/AWG33
Inductor Core	AMCC1000
Inductor Air Gap	4.4 mm

the full voltage, and the inductor can withstand the voltage stress during the all the converter operation (see **Fig. 4.18**), validating the inductor insulation design.

4.7 Summary

In this chapter, the insulation design for the magnetic component windings in MV converters are introduced.

- First, the insulation properties of the mechanical structural material and the combination of encapsulant and structural materials have been characterized. The testing samples are proposed which can be easily implemented in laboratories to test and validate the properties of different materials used in the actual dry-type insulation.

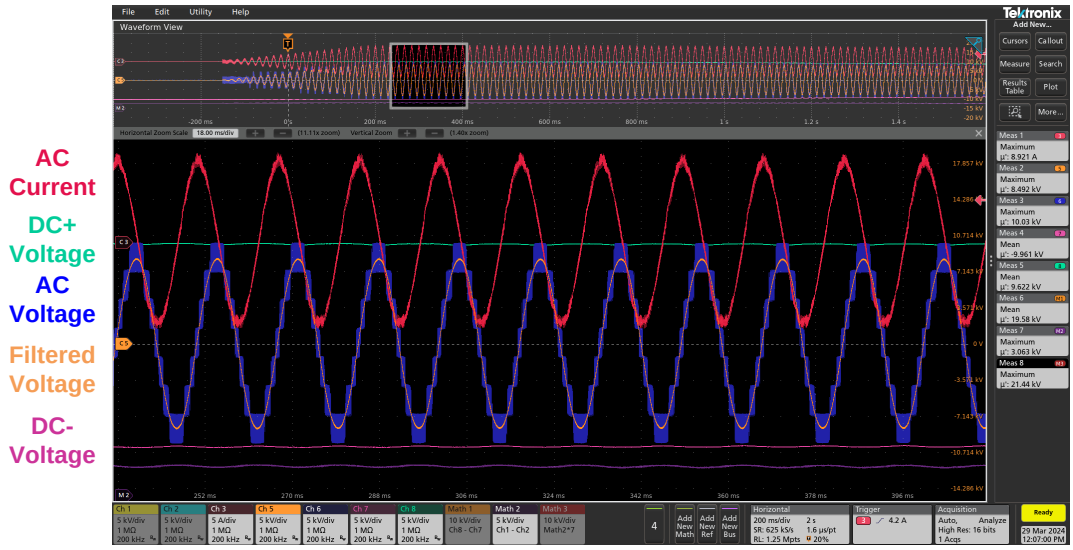


Fig. 4.18: Waveform of the 8-Level flying capacitor converter at full voltage rating [28].

- Then, with the introduced dry-type winding structure, the structures of MV transformer winding and inductor windings are illustrated. To reduce the parasitic CM winding capacitance, partial shielding is proposed to cover only the critical areas of the winding while still effectively confine the electric field to avoid any discharge to the low voltage windings and cores.

- In the meanwhile, the shielding termination can cause high concentration of electric field due to the sharp edges. Field grading is proposed to cover the shielding edge region with high voltage putty to refract the high electric field. Simulation has shown the effectiveness even when the putty is applied with small voids or contamination.

- The improved vacuum pressure encapsulation process for the laboratory environment has also been proposed. With reduced count of chambers and feed-throughs, the encapsulating process can be simplified while maintaining the encapsulating quality. A detailed steps of the procedure is also provided. With PD test results, the proposed potting process demonstrates the insulation quality satisfying the industrial standard.

Chapter 5

Diode Clamped Grounding for Switching Loss Reduction due to Common-Mode Parasitic Capacitances

5.1 Literature Review

For converter systems using isolated DC/DC converters, the parasitics may become a concern on interference and losses as the operating and insulation voltages increase [30, 99–101]. One of the critical parasitics is the common-mode (CM) parasitic capacitance of the MV DC/DC transformers and inductors [29, 97]. Due to safety and noise suppression concerns, the transformer electric shielding or metal case is

usually grounded to the earth (see **Fig. 5.1**), which connects the CM capacitance from the transformer MV winding to the ground [52]. In this case, the low voltage (LV) winding or the area near the MV winding may not see high electric field, yet the voltage of MV winding can charge and discharge the CM or grounding capacitance through the grounding loop with grounding current [102–104]. Current spikes can be induced by charging and discharging the DC/DC transformer parasitic capacitance, which can be seen in **Fig. 5.2**, causing insulation and EMI concerns, in [30] CM model and RL filter have been modeled and proposed to address the EMI issue as shown in **Fig. 5.3**. However, it also brings extra switching losses for CHB devices, which can account for over 15% of converter total loss [31]. Previous efforts have been made on CHB modulation to equivalent parasitics charging frequency which is shown in **Fig. 5.4**, but the complex modulation can cause unbalanced switching losses on different devices [31]. The CM capacitance induced loss can also be limited by reducing the parasitics with different shielding strategies [19], but difficulties will be added on insulation design for the transformers and converters.

5.2 Mechanism on Capacitance Induced CM Switching Loss

For CM loops of CHB converters, the LV side can be neglected due to the shielding effect of the shielded transformer, and the transformer itself as well as the DAB MV

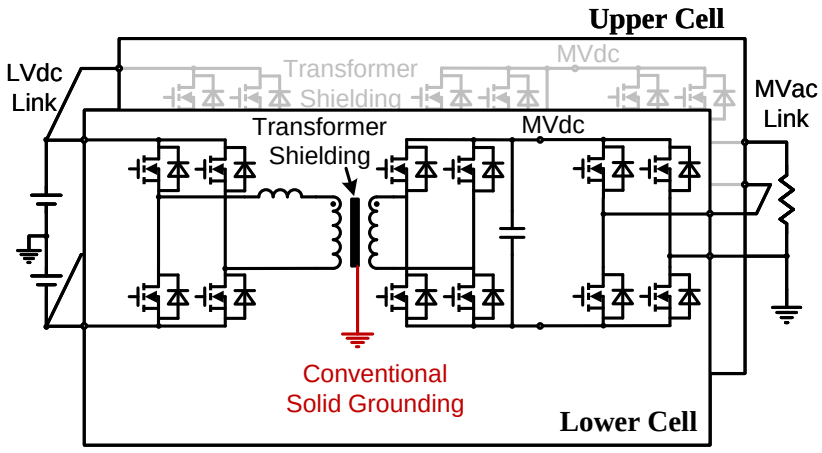


Fig. 5.1: Topology of converter using cells consisting of DC/DC and DC/AC, showing conventional transformer solid grounding [20].

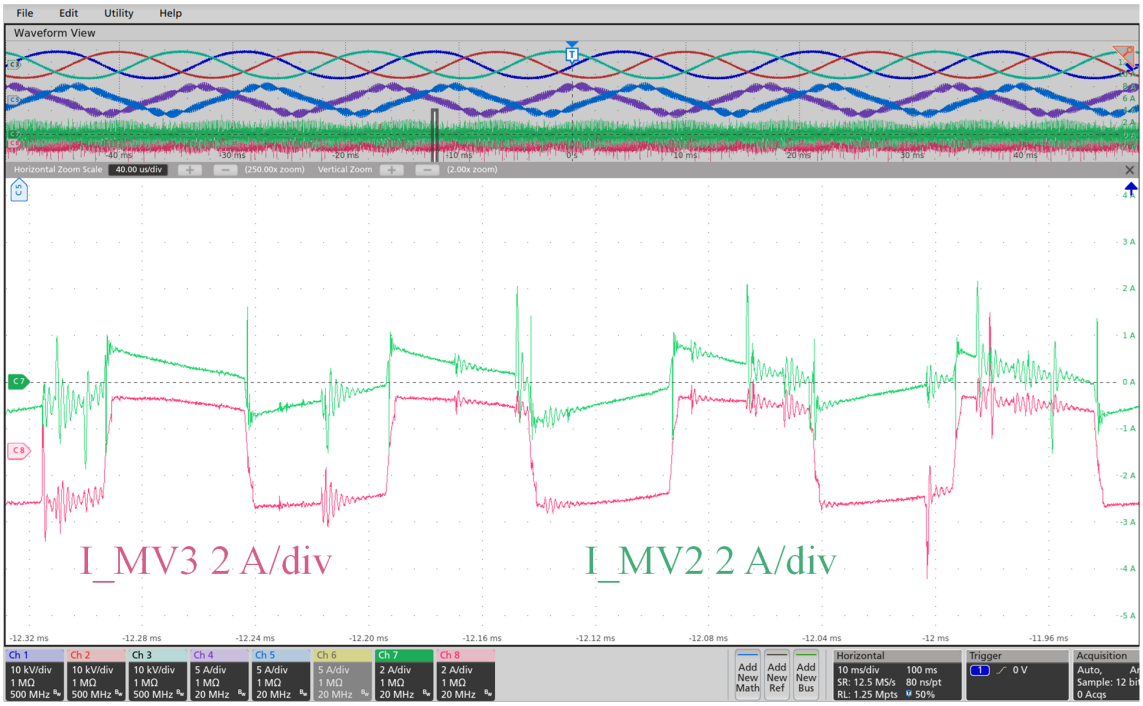
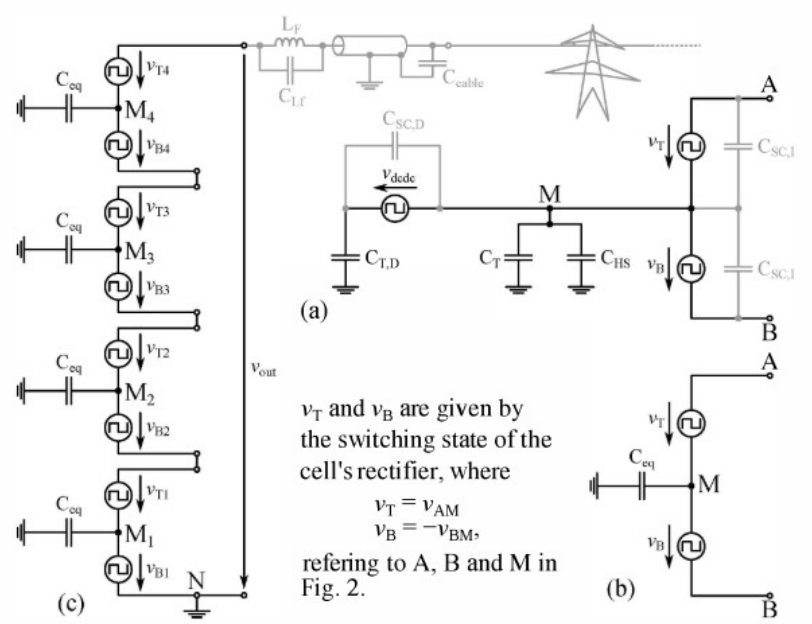
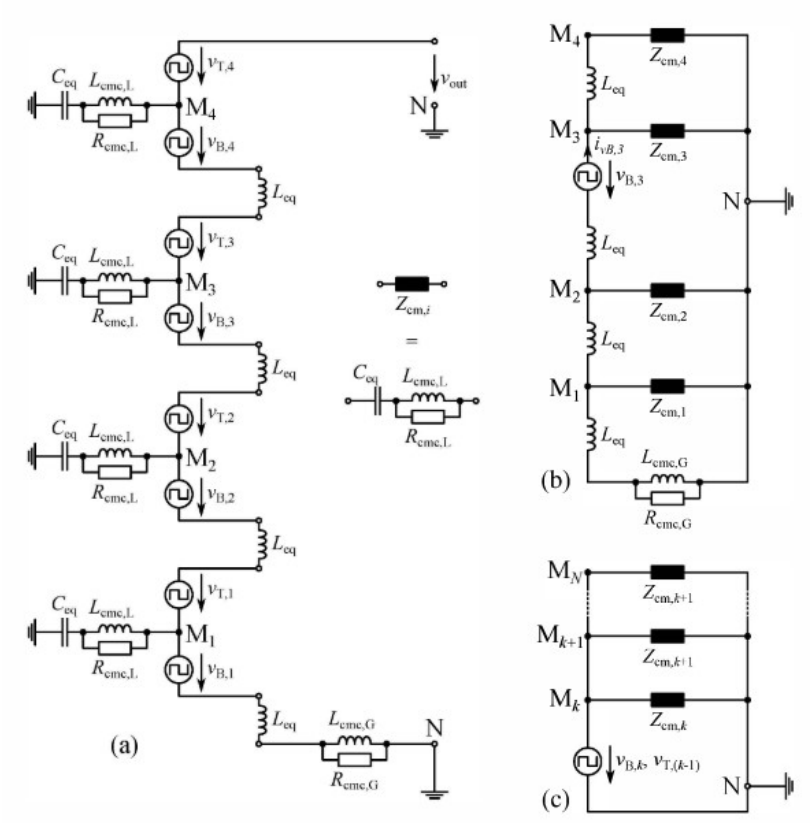


Fig. 5.2: Current spikes in transformers having high grounding capacitance [29].



(a)



(b)

Fig. 5.3: CM model and filter design for a solid-state transformer in [30].

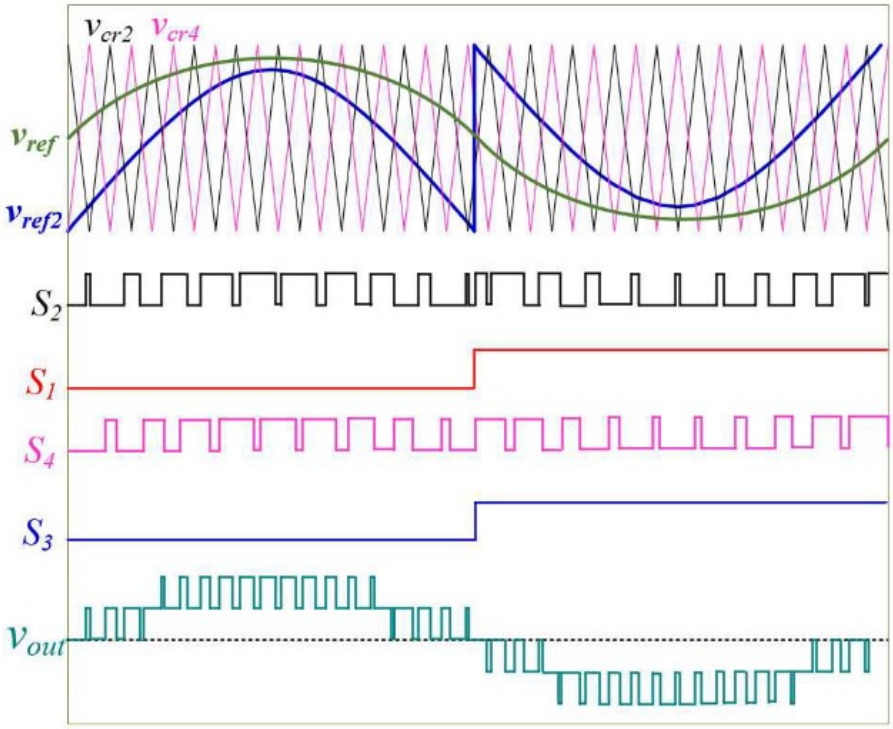


Fig. 5.4: Unbalanced modulation strategy to reduce CM noise and loss [31].

side can be simplified as the *RLC* circuits, when the DAB is operating in single phase-shift mode without generating evident CM noise. Hence, take 2-stage CHB (CHB2) as an example, the circuit can be simplified as in **Fig. 5.5**. Therefore, **Fig. 5.6** shows the CM voltage and current waveform in that CHB2 model in simulation. One can easily see the the upper stage in CHB2 has a tripled CM frequency compared to the lower stage. As one terminal of the lower stage is grounded, the CM noise of the lower stage is at its actual switching frequency, with a shape of rectangular waveform with a peak-to-peak value of the DC-link voltage. Similarly, for the upper stages, its CM noise is generated by both the CM voltage by itself, but also the elevated potential thanks all the output voltages below it. The higher level the stage is situated, the higher CM noise frequency is generated, yet the bouncing voltage level is always the same as the DC-link voltage. And, due to the rectangular shape of the CM noise, the parasitic capacitance to the ground is always being charged and discharged every time the CM voltage level changes, with current spikes.

Fig. 5.7 shows the model simplification as a single-stage CHB and its commutation loop. Before and after the commutation, it is clear that the devices conducting current with the load and source, and CM loop or ground are not involved. However, when the CHB is switching and generating CM noises, as the bridge arm connected to the ground switches, CM voltage changes its level or polarity, and the charging and discharging current can be generated from ground to the transformer CM capacitance, and then back to the ground through the devices and AC side loads.

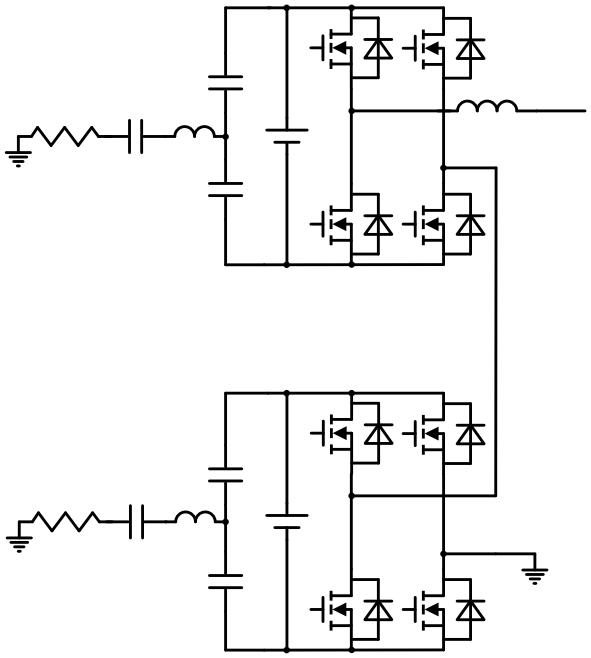


Fig. 5.5: Simplified 2-stage CHB converter scheme.

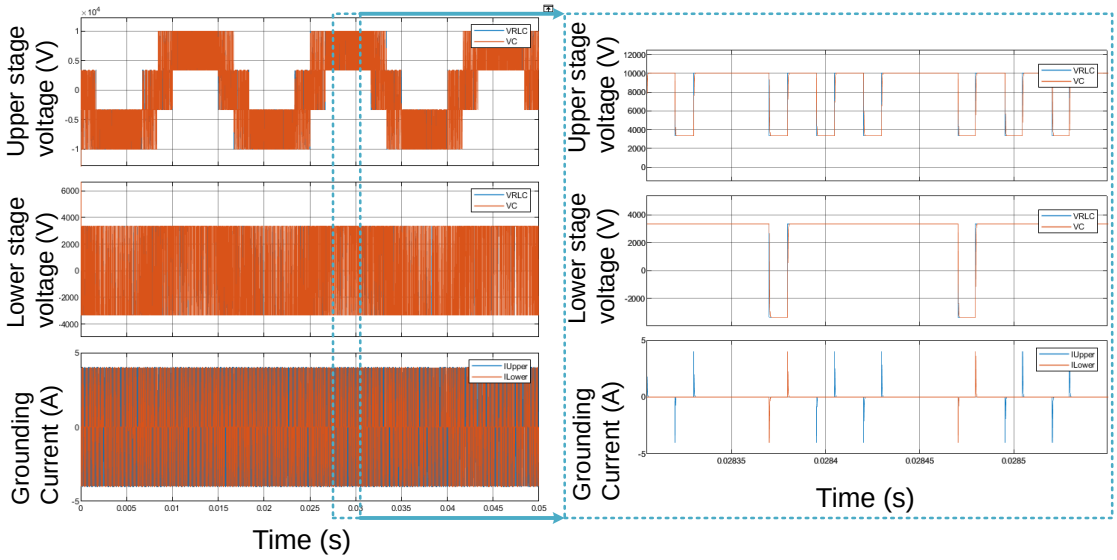


Fig. 5.6: CM voltage and current waveforms in 2-stage CHB.

That is, theoretically, the common-mode (CM) current flows only through the ground and the connected devices, and it does not pass through or appear on the AC live wires. As a result, it cannot be directly measured at the AC input lines. Furthermore, this type of current is not influenced by varying load conditions, meaning that changes in the load or in soft-switching operations do not have a significant impact on it. Consequently, the associated power loss due to CM current should remain relatively constant regardless of the load level or the switching scheme being used.

5.3 Diode-Clamped Grounding Configuration

5.3.1 Topology with Diode Clamped Grounding Circuit

First, the proposed topology with diode-clamped grounding is illustrated in **Fig. 5.8**. Unlike the conventional configuration shown in **Fig. 5.1**, where the transformer shielding is directly connected to the earth ground, the proposed design features a different approach. In this topology, the transformer shielding is instead connected to a diode half-bridge network, which is further linked to the LV DC link. As a result, the potential of the transformer shielding is no longer solidly grounded but becomes partially floating. This semi-floating potential enables dynamic adjustment, which helps in effectively canceling out the CM voltage that is induced on the MV winding by the modulation of the CHB converter. This mitigates CM current and associated EMI concerns.

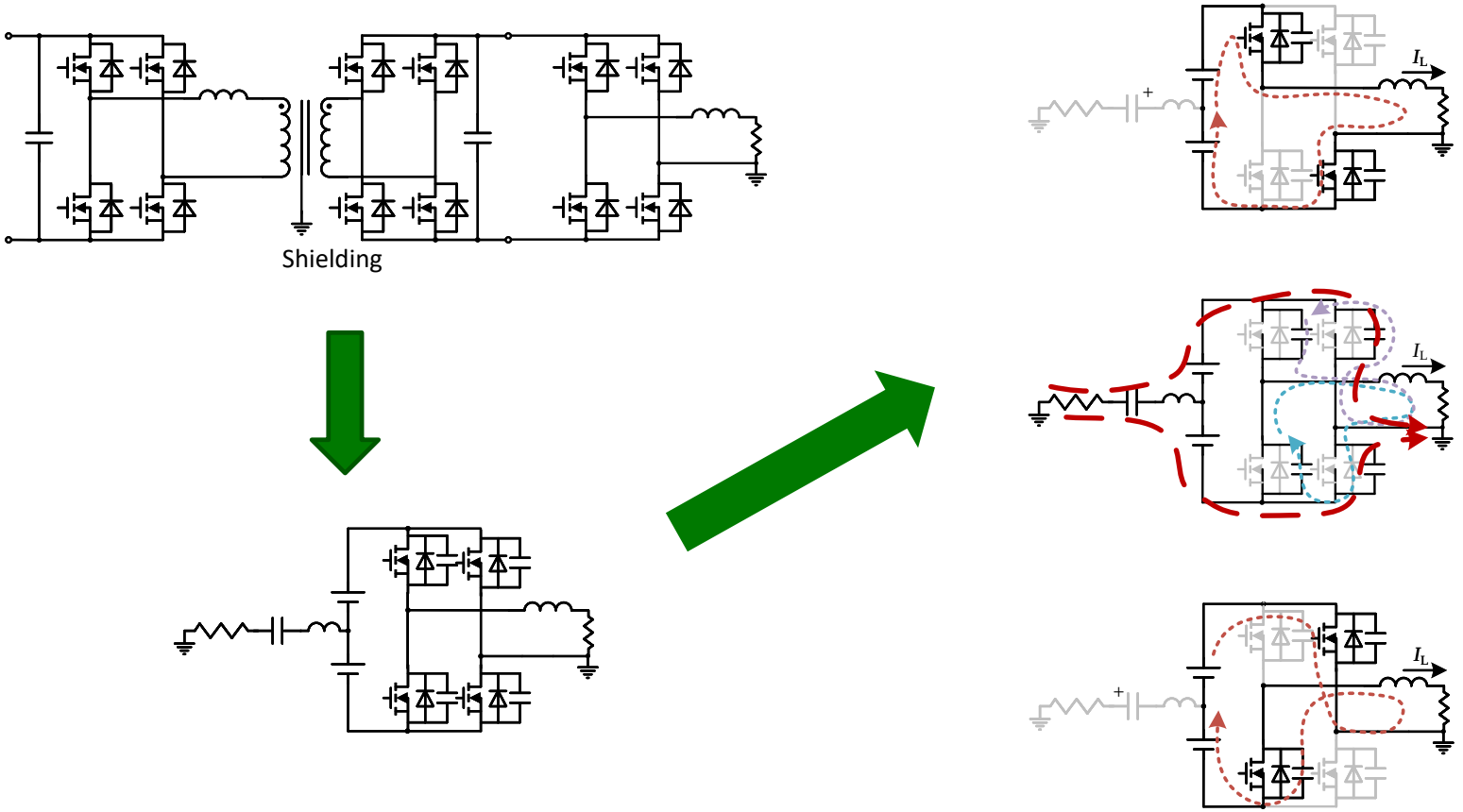


Fig. 5.7: CHB commutation loop and model simplification considering CM capacitance.

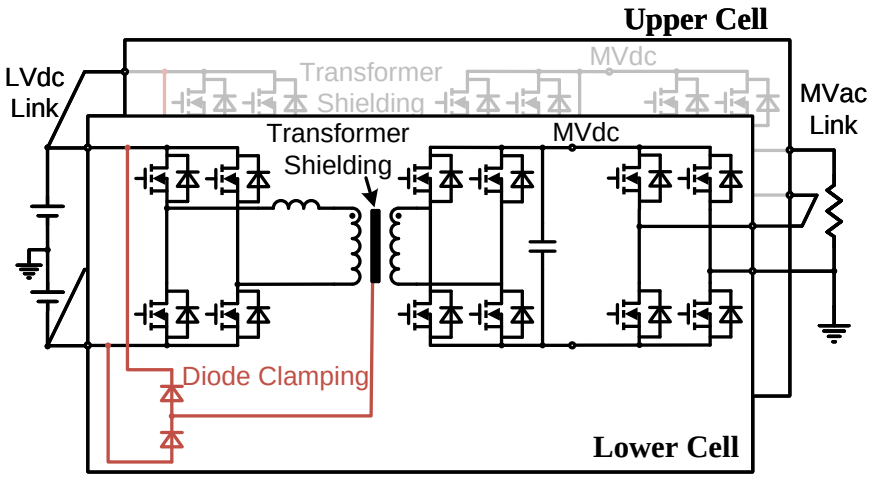


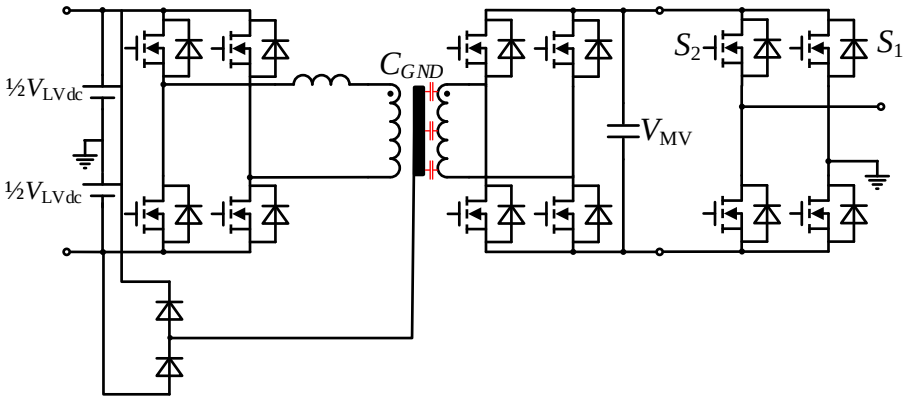
Fig. 5.8: Topology of converter using cells consisting of DC/DC and DC/AC, showing diode clamped transformer grounding [20].

5.3.2 Operational Analysis of the Diode Grounding Circuit

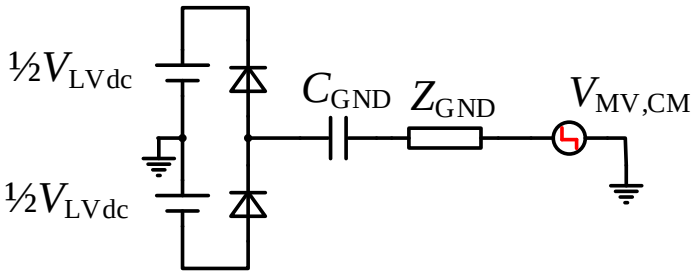
As the MV DC/DC transformer is usually shielded between the LV and MV windings, only the MV side switching is studied. Also, with DAB converter acting with single phase-shift modulation, the DAB itself does not generate CM mode voltage. Therefore, the circuit loop concerning CM capacitance induced loss can be further simplified as the grounding CM capacitance directly connected to the CHB converter and diode clamping circuit, which is also grounded on the AC side, which is illustrated in **Fig. 5.9**.

Hence, the CM loop of CHB can be analyzed. As the CHB is grounded, for the lowest stage, the CM voltage of the MV DC side is

$$v_{MV,CM} = \frac{(1-2S_1)V_M V}{2} \tag{5.1}$$



(a)



(b)

Fig. 5.9: Topology under study: (a) lowest cell with DAB and CHB converters using diode clamped circuit, (b) simplified CM loop.

where, S_1 is the switching function as in **Fig. 5.9(a)** [20]. From (5.1), the CM voltage of the MV DC side is flipping between half and negative half of the MV DC-link voltage. Therefore, as the CM voltage changes the polarity, the CM capacitance gets charged and discharged, through the diode clamping circuit. The two modes of the CM loop can be depicted as in **Fig. 5.10**.

From **Fig. 5.10**, as the CM voltage changes, the diode clamping circuit rectifies the charging/discharging current, causing voltage drop of half LV DC-link voltage on the circuit. Therefore, the voltage across the capacitance can be reduced by half of V_{LVDC}. Suppose the grounding impedance Z_{GND} is mainly resistive, the energy lost in the capacitance charging circuit is

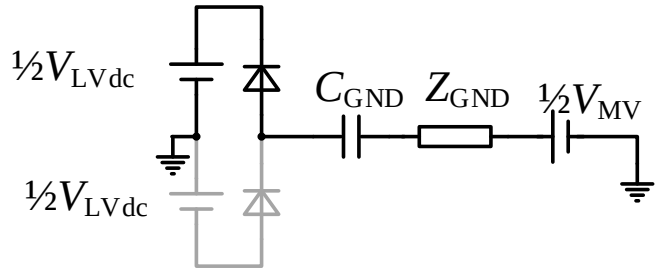
$$E_{loss} = \frac{1}{2} C \Delta V^2. \tag{5.2}$$

Where, C is the grounding CM capacitance, ΔV the voltage change on the CM capacitance. For conventional solid grounded transformer, the total CM grounding induced loss for the lowest stage is [31]

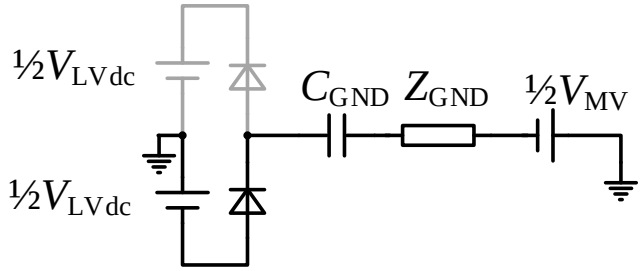
$$P_{loss,solid} = C V_{MV}^2 f \tag{5.3}$$

Where, f is the equivalent switching frequency of the CHB converter. For the proposed diode clamping circuit, the loss can be reduced to

$$P_{loss,proposed} = C \Delta V^2 f = C (V_{MV} - V_{LVDC})^2 f \tag{5.4}$$



(a)



(b)

Fig. 5.10: Grounding parasitic capacitance charging and discharging modes with: (a) positive CM voltage, (b) negative CM voltage.

By subtracting (5.4) with (5.3), the loss reduction for the lowest stage is

$$\Delta P_{loss} = C\left[V_{MV}^2 - (V_{MV} - V_{LVDC})^2\right] f \tag{5.5}$$

Note that, the closer values V_{MV} and V_{LVDC} yield more effective loss reduction, and the analysis can be easily scale up to multiple cells cascaded by changing the switching frequency f to the sum of equivalent CM frequencies [31], and the **Fig. 5.10** can also be valid with correct CM voltage levels.

5.4 Simulation and Test Validation

.

As the effectiveness of the diode clamping circuit has been analyzed, simulation and experimental tests have been performed to get the proposed grounding method validated.

5.4.1 Simulation Verification

First, the simulation of a two-stage CHB converter with DAB transformers, as shown in **Fig. 5.1** and **Fig. 5.8**, has been performed. The LV and MV DC-links are set to 800 V and 1600 V, and the waveforms of CM voltage, voltages across CM capacitances and charging currents are shown in **Fig. 5.11**. As the CHB device

switches, the transformer parasitics see the common mode (CM) voltage abstracted by $\frac{1}{2}$LVDC voltage (400 V) as in **Fig. 5.11**.

5.4.2 Experimental Verification

Then, tests have been performed with the same rating of the simulation. The photographs of the MV DC/DC transformer and the diode clamping circuits are shown in **Fig. 5.12**. The test waveforms are shown in **Fig. 5.13**. From the waveforms, the shielding layer potential is not constantly zero, floating between the positive and negative of half LVDC link. The power loss with constant resistive load up to 12 kW is shown in **Fig. 5.14**. Loss reduction can be achieved constantly under variable output voltage by approximately 18 W, 53% of parasitic loss reduced

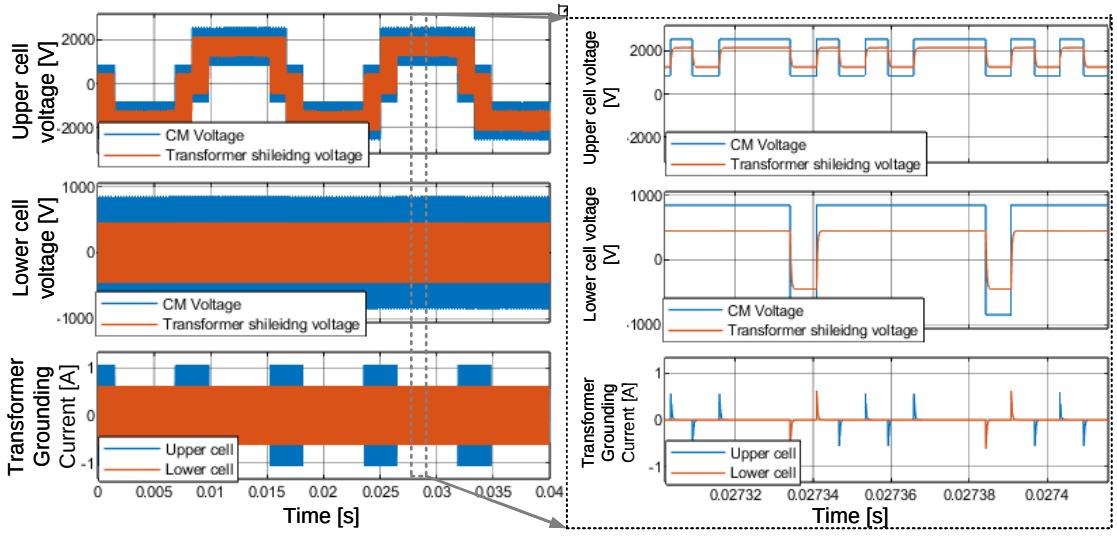
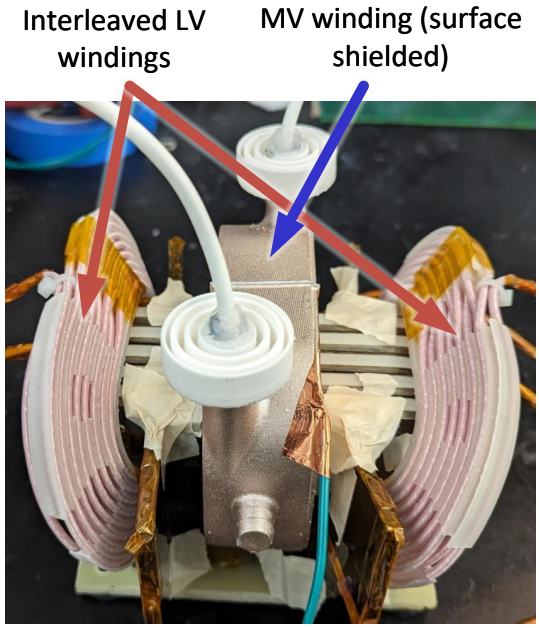
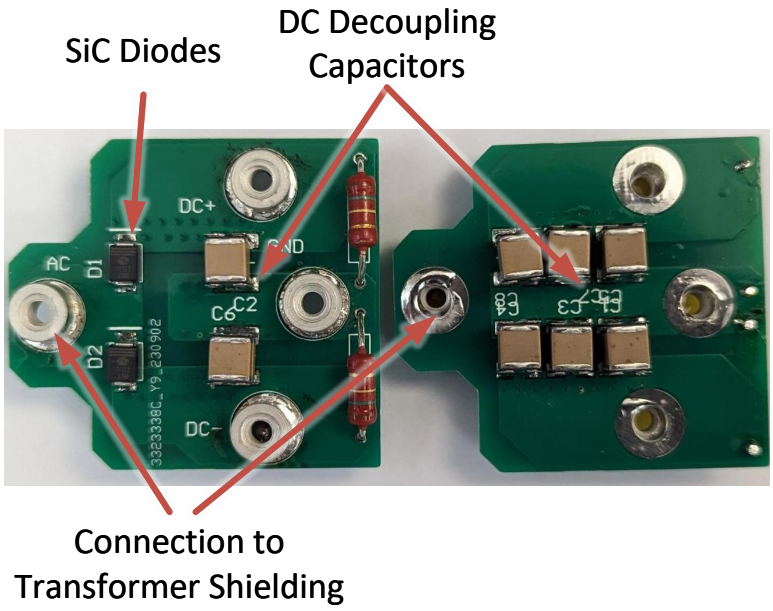


Fig. 5.11: Simulation results of diode clamped grounding, the transformer shielding potential swing for both upper and lower cell is reduced by half of LVDC link voltage (400 V) [20].



(a)



(b)

Fig. 5.12: Photography of (a) MV dc/dc transformer, (b) diode clamping circuit [20].

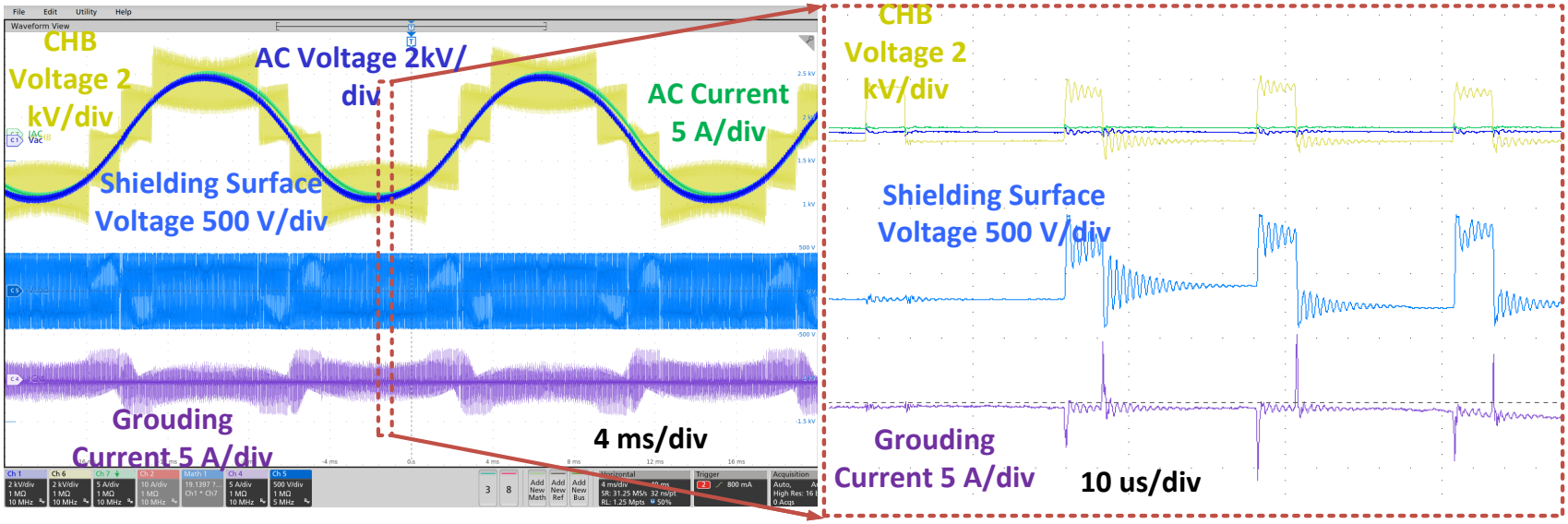


Fig. 5.13: Test waveforms for diode clamped grounding (with shielding voltage and grounding current for the upper cell) [20].

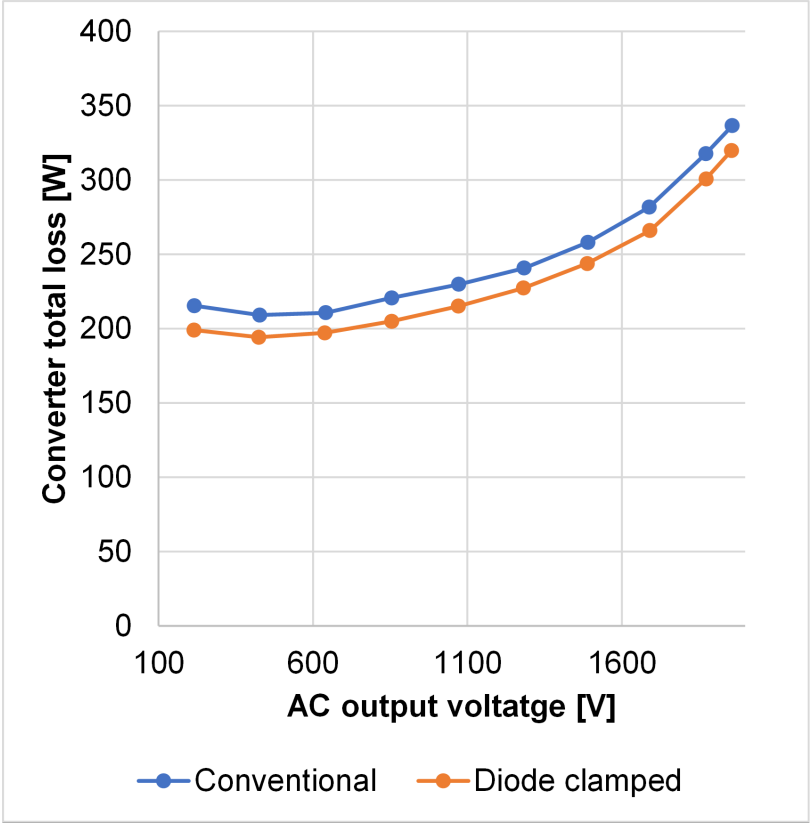


Fig. 5.14: Tested loss comparison between conventional and diode clamped grounding [20].

(theoretically 34 W), and 6% reduction on the total converter loss. Although the transformer potential swings ($\frac{1}{2}V_{LVDC}$), the LV DC-link is typically below 1 kV and the margin on low voltage side insulation is usually high enough, so no further requirement on LV winding and power stage insulation is required.

5.5 Impact Factors

Since several different components can be found in the grounding loop, e.g., clamping diodes, grounding impedance, CHB devices, the effectiveness of the loss reduction can be influenced by multiple factors, too. The impact factors mainly include diode parasitics, grounding impedance, and modulation non-ideality, such as gate signal delays.

5.5.1 Diode Parasitics

For the diodes, the non-idealities may cause extra conduction and switching losses. As the charging current is pulsating current with amplitude up to several amperes and short duration (¡400 ns), and the diode forward voltage drop is also low compared to the CM voltage change, the conduction loss can be negligible. For the switching loss, as SiC Schottky diodes are used, no reverse recovery loss is assumed, while the charges built-up in the junction capacitance should be considered. As the CHB MV devices hard switch, the diode junction capacitance discharges and causes CHB device switching loss. The switching energy loss for each diode is

$$E_{loss,SBD} = \int C(v_r) v_r dv_r \tag{5.6}$$

where, the v_r is the diode reverse bias voltage during CHB device switching. As estimated during the test, the diode switching loss should be around 0.96 W.

5.5.2 Grounding Loop Impedance

The grounding parasitics can be complicated, which may be comprised of impedances of grounding wires, transformer shielding layer, and commutating loop of diode clamping boards. As the grounding loop should be low impedance required by the safety guidelines, only inductances are considered. To study the impact of total grounding impedance, a simulation sweep has been done to find out the loss variation on the grounding loop. **Fig. 5.15** shows the loss results, from which the parasitic inductance increases from zero to 10 µH, while the loss is increased by 3 W. Hence, the inductance may impact the loss reduction, while as long as the grounding loop is controlled as short as possible, the loss impact is low.

5.5.3 Gate Signal Delay

Modulation mismatches may cause mismatched CM voltages waveform, which can cause unexpected charging and discharging events on the CM capacitances. **Fig. 5.16** shows the simulation sweep with gate driving delays. As shown in the figure, when gate driving delays up to 1% of the switching period, the loss can be increased by

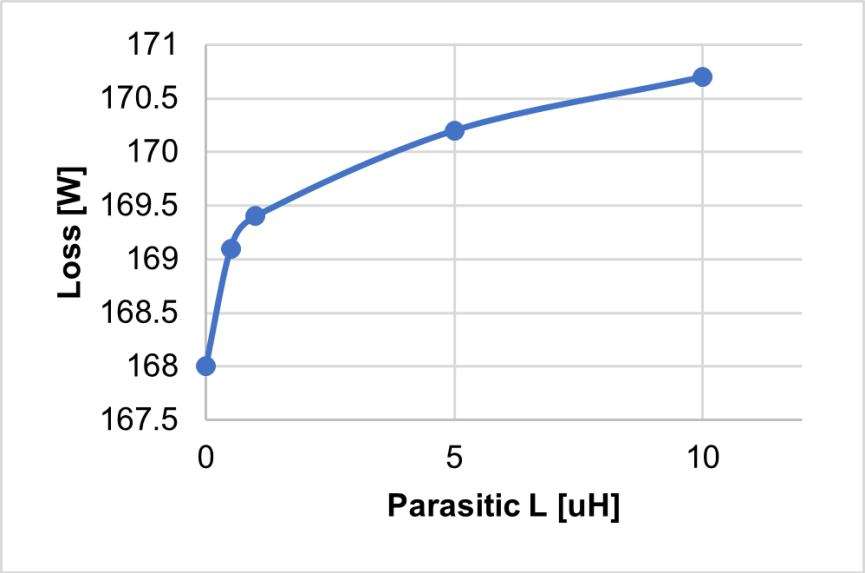


Fig. 5.15: Simulation sweep of grounding inductance and capacitance associated loss [20].

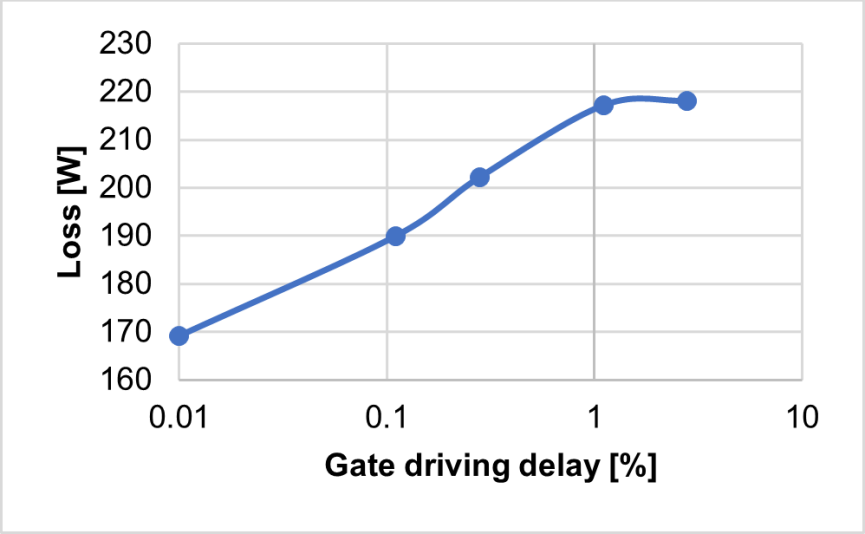


Fig. 5.16: Simulation sweep of gate driving delay and capacitance associated loss [20].

30%, which can counterpart the proposed loss reduction. Therefore, the modulation and gate signaling may increase the CM capacitance induced loss, and the modulation delay and dead-time should be well managed.

5.6 Summary

In this chapter, a diode clamping circuit is proposed to reduce the CM parasitics induced switching loss on the CHB converters.

- First, the mechanism of the common-mode capacitance induced switching loss has been analyzed. The CM loss is associated to the switching of CHB converters, if DAB is at single phase-shift mode without emitting CM noise to the transformer. The CM loss is only associated to the grounding loop, so its level is not affected by the AC side load or soft-switching condition.

- Then, the diode clamped grounding circuit has been proposed. The mechanism of the diode clamped circuit has also been analyzed. The relationship between DC/DC voltage ratio and reduction effectiveness is also derived.

- The proposed method has been experimentally validated in MV cascaded H-bridge converters with isolated DC/DC converters. For the tested cases, the proposed method has reduced the parasitics associated loss up to 53%, which aligns with the analysis. It can also be potentially higher when the ratio of MV

to LV DC voltages to be closer to unity, regardless of the transformer turns ratio.

- A theoretical analysis has been performed including different impact factors, namely diode parasitics, loop impedance, and gate driving delays, among which the diode junction energy and gate signal delays may have high impact and should be carefully considered.

Chapter 6

Compact MV Power Stage Design With Heatsink Electric Field Shaping

6.1 Literature Review

10-kV SiC MOSFETs have been implemented into medium voltage (MV) power converters due to their high blocking voltage, and the corresponding power stage, gate drive circuitry, and cooling system must be properly designed to withstand similar high voltage stress to that of MV SiC devices, so that the utilization of high voltage capability can be maximized [105]. As the voltage stress rises, the required clearance and creepage distance between components with different potential increases, taking more space, introducing parasitics, and causing inconvenience for cooling.

Designs have been introduced in the literature, to tackle the issues for 10-kV SiC power modules. Several gate drive designs have been proposed for short-circuit protection, consistency and reliability [106–109]. Gate driver power supply designs with high insulation and low common mode capacitance are also presented [110, 111]. Laminated bus-bars considering loop inductance and insulation stress are also discussed in [107]. Literature can also be found to discuss the insulation issues on cooling systems, which are also important for the implementation of 10-kV SiC devices.

To address the module base-plate associated partial discharge (PD) issue, the grounding configuration of heatsinks for XHV-9 modules (see **Fig. 6.1**) are discussed in [32]. Field shaping can also be used when the heatsink is floating with the potential of base-plate [33]. Nonetheless, less discussion can be found on design with discrete 10-kV SiC devices (see **Fig. 6.2**). In [33], a field shaping structure of the heatsink for XHV-6 power module has been proposed, which is depicted in **Fig. 6.3**, but the field shaping strategy has low space utilization due to its extra clearance between the heatsink and field shaping ring. For discrete devices, because an external connection for the switching node is needed, and the base-plate is attached to the drain, careful consideration should be made on insulation clearance of the power stage design. In [112], a laminated bus-bar with Mylar insulator was used for a 10-kV discrete device test setup. Stacked PCB bus-bar and gate drive power supply have been introduced in [113] for the discrete device. However, to further improve the power density of the

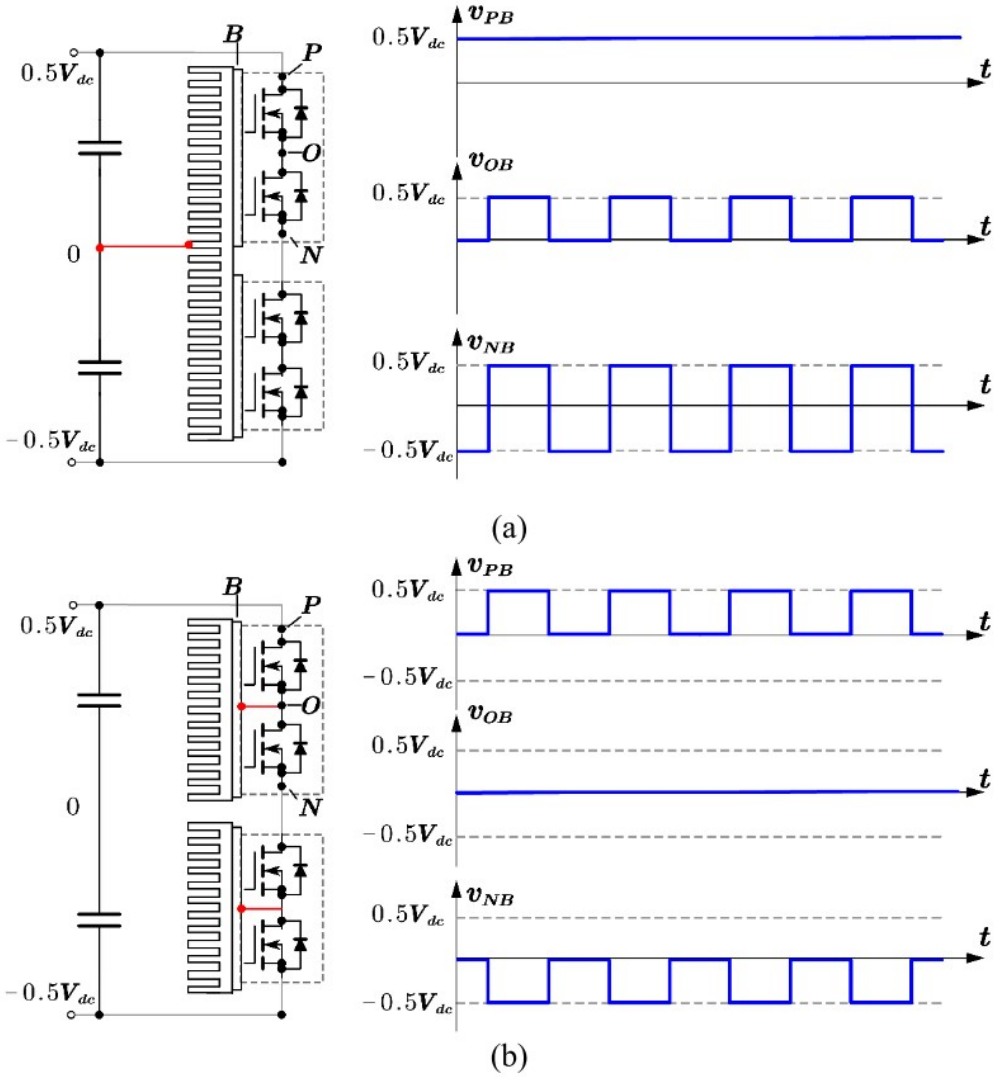


Fig. 6.1: Grounding connection of device base-plate and heatsink [32].

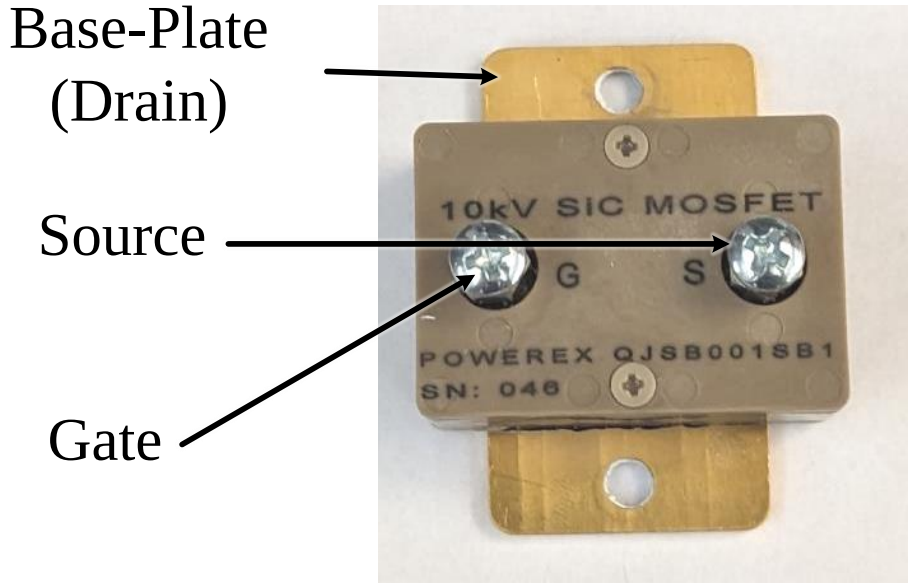


Fig. 6.2: Photograph of the 10 kV SiC discrete MOSFET.

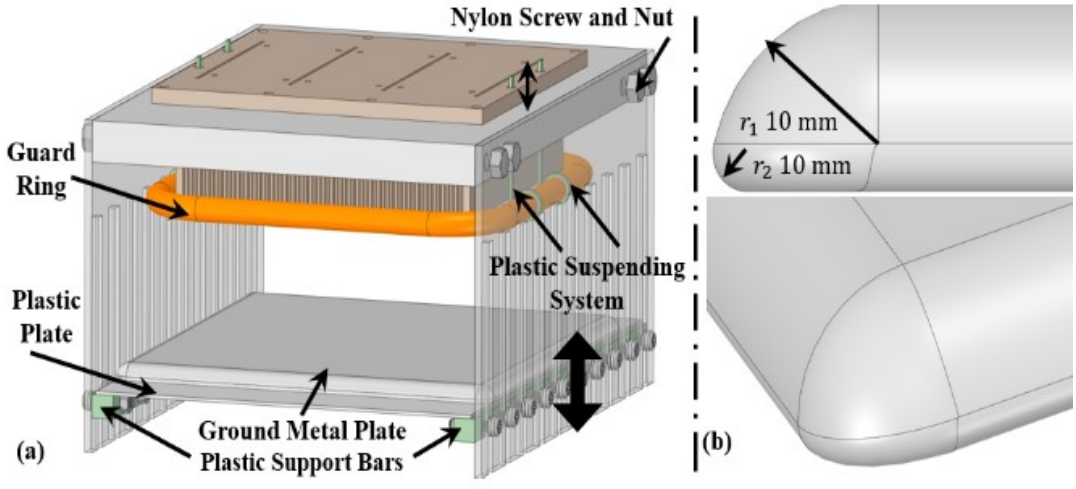


Fig. 6.3: Field shaping of heatsink proposed in [33].

10-kV SiC-based converters, more effort should be made on integration of the gate drive, bus-bar, and cooling system, considering the insulation requirement.

6.2 Electric Field Shaping and Air Duct

6.2.1 Field Shaping of Heat Sinks

As shown in **Fig. 6.2**, the base-plate is also the electrical drain terminal of the discrete MV SiC device. Insulation is needed between either the device or the heatsink, or between heatsinks for the devices nearby. For better cooling performance, placing insulator between the base-plate and heatsink is unfavorable, as the insulator needs to withstand the high voltage while providing heat conducting path, which introduces high thermal resistance. Instead, the discrete device is directly attached to the heatsink through thin thermal interface material (TIM), and the heatsink is electrically connected to the drain terminal. With this, an air gap is needed between heatsinks to withstand the voltage stress.

To achieve high compactness, the volume of the air gap needs to be minimized, because it can only help insulation but creates longer commutation loop and diverts the airflow for cooling. Therefore, the heatsinks for different devices with similar potentials should be placed as close as possible without complicating the commutating loop. Therefore, the arrangement of the four devices with heatsink is illustrated as **Fig. 6.4**, where the two heatsinks of the upper devices can be mounted together because of the same potential of their drain terminals.

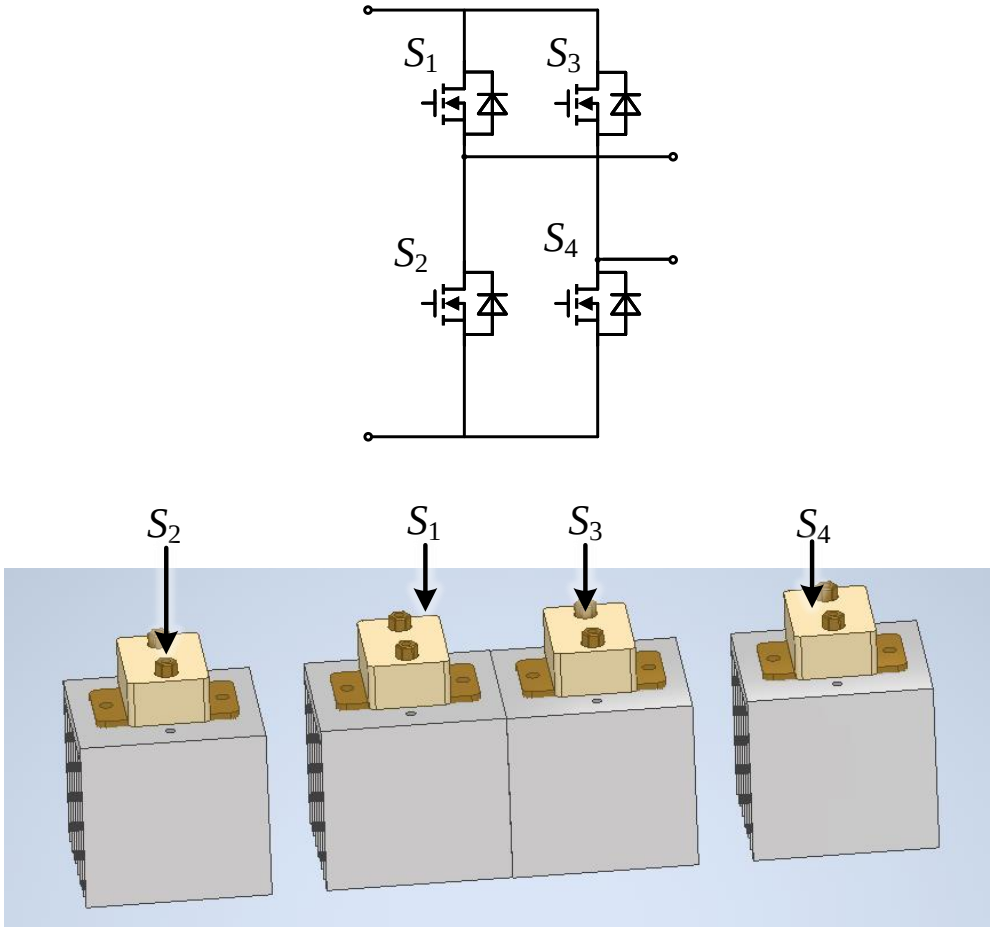


Fig. 6.4: Device/heatsink arrangement of the H-bridge power stage [34].

Clearance has to be added between the upper and lower devices, to withstand the large potential difference between the devices. Due to the 90 degree edges and thin fins of heatsinks, the electric field in the air is highly uneven, and long clearance is usually needed to suppress the electric field on sharp edges. To minimize the clearance, field shaping has been used in [33] for power modules, but it still occupies a wide space between the heatsink and field shaping ring. In this paper, a field shaping structure directly built on the edges of heatsinks is proposed. Its structure is depicted in **Fig. 6.5**. By using rounded edges covering the right angle edges, the curvature of the heatsink assembly can be suppressed, and hence the electric field can be more evenly distributed.

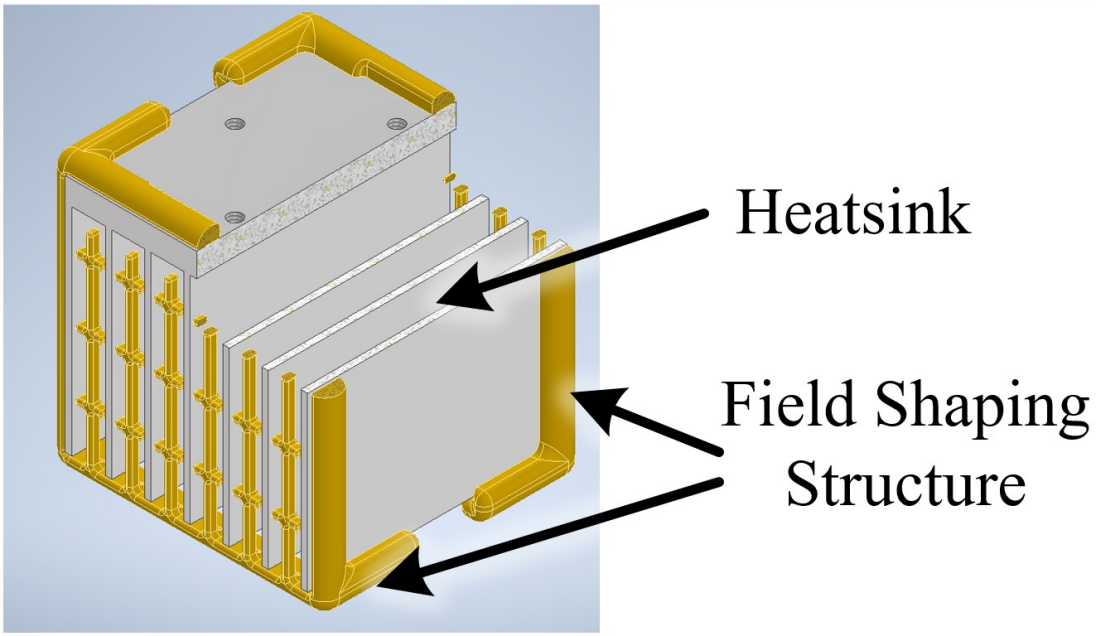


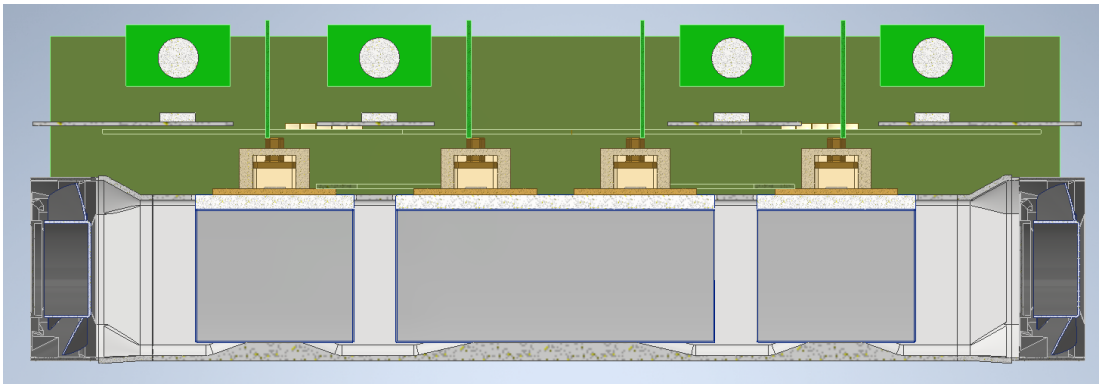
Fig. 6.5: Device/heatsink arrangement of the H-bridge power stage [34].

6.2.2 Air Duct with Mechanical Support and Creepage

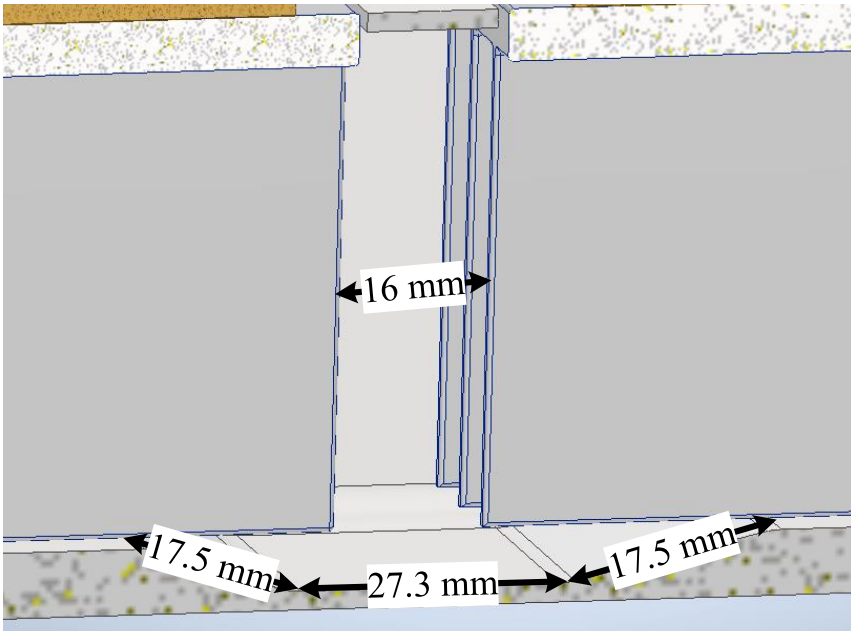
The air duct is also necessary for air-cooled converters mainly to direct air to flow through heat sinks, and it is especially important for MV converters considering insulation. **Fig. 6.6(a)** shows the overall structure of the air duct in the MV power stage in the cutaway drawing. The proposed air duct structure can provide both mechanical support and insulation creepage distance. The heat sink and circuitry above can be directly supported by the bottom of the air duct with a bumping structure, and, in the meantime, the ramp of the bumping structure can also provide extra creepage distance for the heat sinks. **Fig. 6.6(b)** shows that the two heat sinks are placed apart at 16 mm, while the creepage distance across the bottom of the air duct structure is 62.3 mm, which is greater than 40 mm at 10 kV per the UL840 standard.

6.2.3 Simulation and Test Results

The structure is first verified in simulation, and the results are shown in **Fig. 6.7**. From **Fig. 6.7(a)**, without field shaping, the electric field is mainly concentrated on the sharp edges of the heatsink, and the maximum value is 2 kV/mm, which may cause corona discharge even if the air gap does not break down. In **Fig. 6.7(b)**, with the field shaping radius of 3 mm, the electric field can be more evenly distributed, with peak field strength of 1.1 kV/mm, which is a reduction of 44%, and hence, the heatsinks can be placed closer to maintain the same dielectric stress.

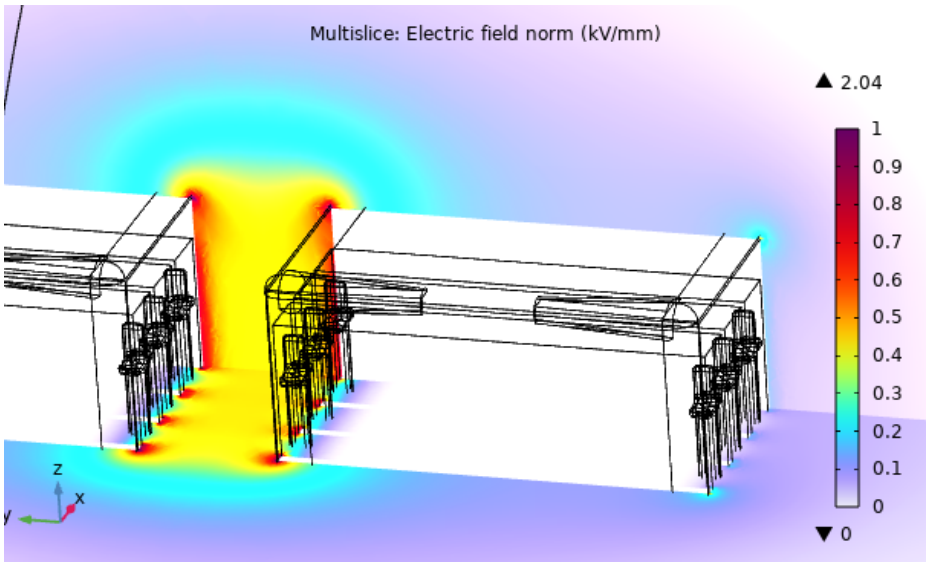


(a)

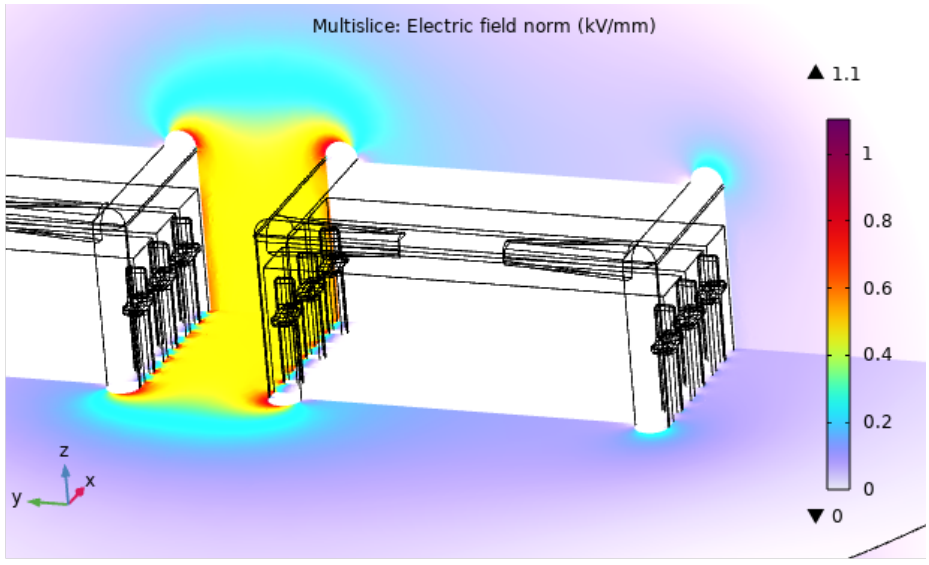


(b)

Fig. 6.6: Proposed air duct (a) cross cut-away view, and (b) creepage distance.



(a)

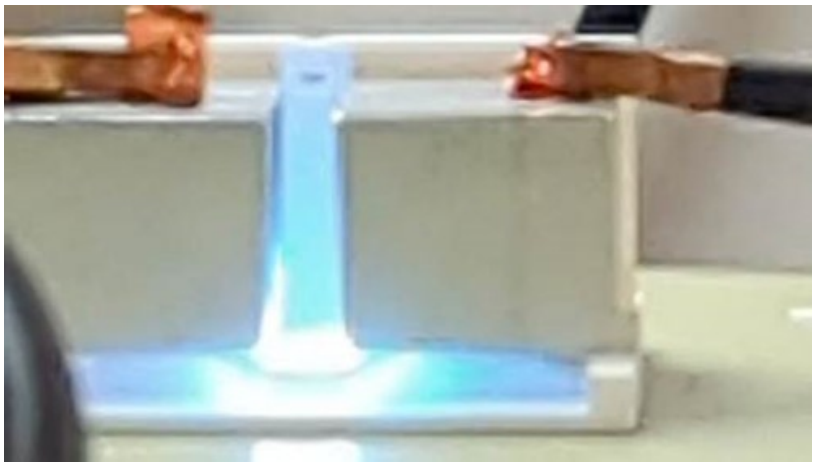


(b)

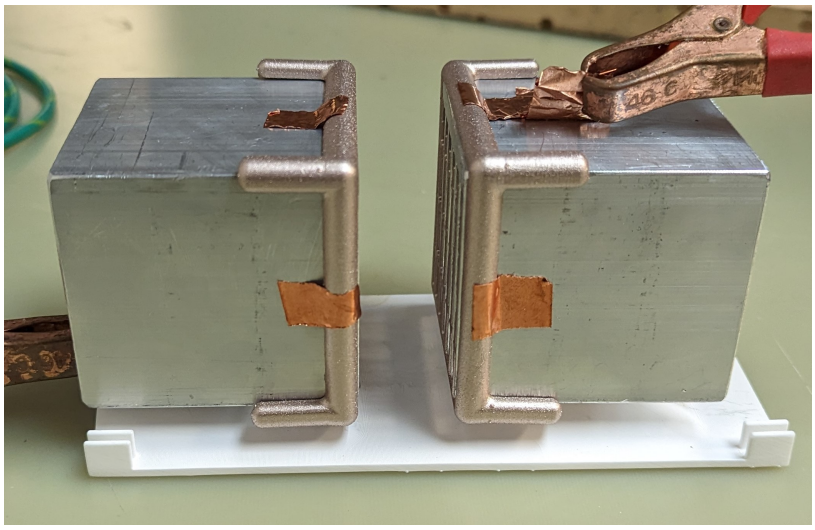
Fig. 6.7: Simulation comparison of (a) bare heatsinks, (b) field shaped heatsinks.

Experimental tests have been performed to verify the simulation results. **Fig. 6.8(b)** shows the insulation test setup of the heatsinks with field shaping structures. In **Fig. 6.8(a)**, an air gap insulation breakdown was observed with extreme high voltage excitation on purpose, showing that the weak point of insulation occurs at the sharp heatsink fins on the bottom. **Fig. 6.9** shows the insulation test results of the heatsinks with and without the field shaping, and by adding the field shaping structure, the corona discharge onset voltage can be increased by 2 kV, while the breakdown voltage can be increased by 30%. Because the electric field is still not perfectly evenly distributed, the corona onset voltage increase is not as high as the breakdown voltage, but the improvement is still evident. Without the field shaping, the clearance is selected as over 20 mm for corona-free operation, while the distance can be selected as 10 12 mm with field shaping.

The impact of the field shaping on thermal performance is also verified. To ensure that the proposed field shaping does not affect the cooling performance, a thermal simulation is then performed as in **Fig. 6.10**. As it shows, the four devices can be effectively cooled, and the hot spot is on the leftmost device, with the peak temperature of 60℃, which is within the safe operating range of SiC devices. As shown in **Fig. 6.10(b)**, the air flow is not blocked by the field shaping ring within the heatsinks.



(a)



(b)

Fig. 6.8: Photograph of heatsink insulation test: (a) at an air gap breakdown, (b) setup of heatsinks with field shaping [34].

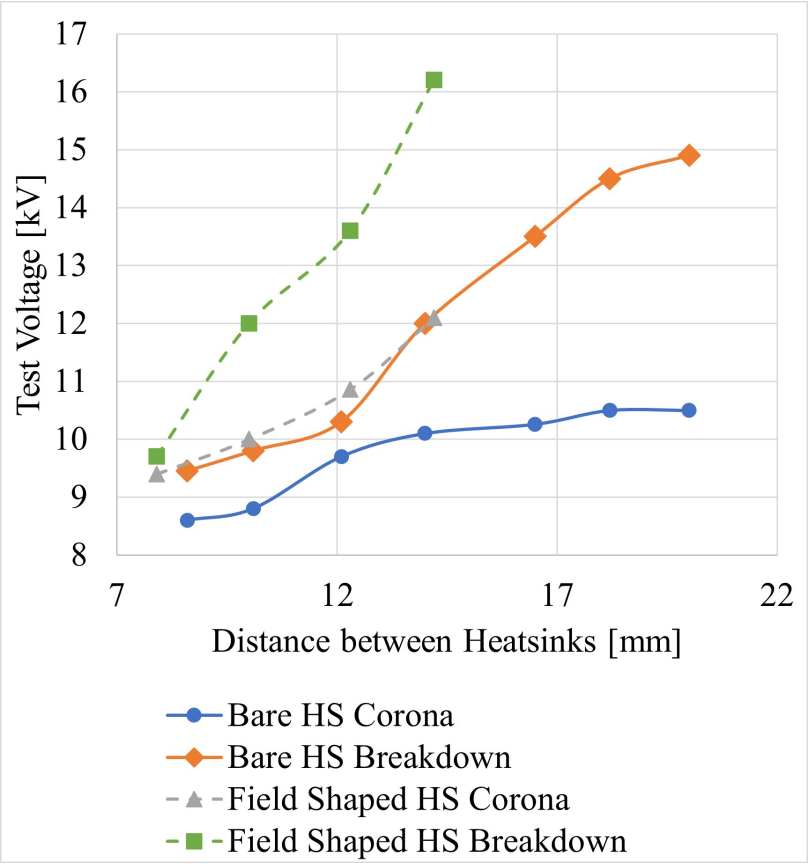
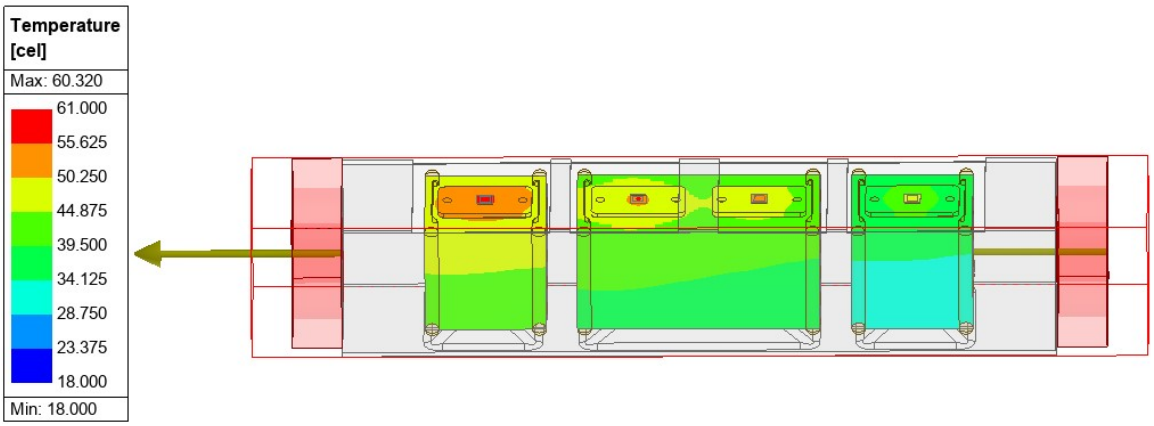
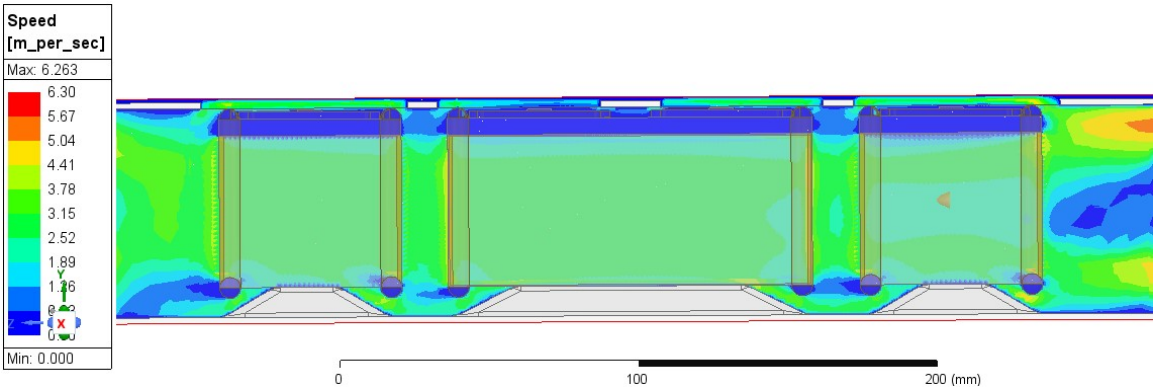


Fig. 6.9: Test results of corona and breakdown onset voltage at different clearances and configurations [34].



(a)



(b)

Fig. 6.10: Thermal simulation with the proposed field shaped heatsinks: (a) temperature distribution, (b) air speed distribution.

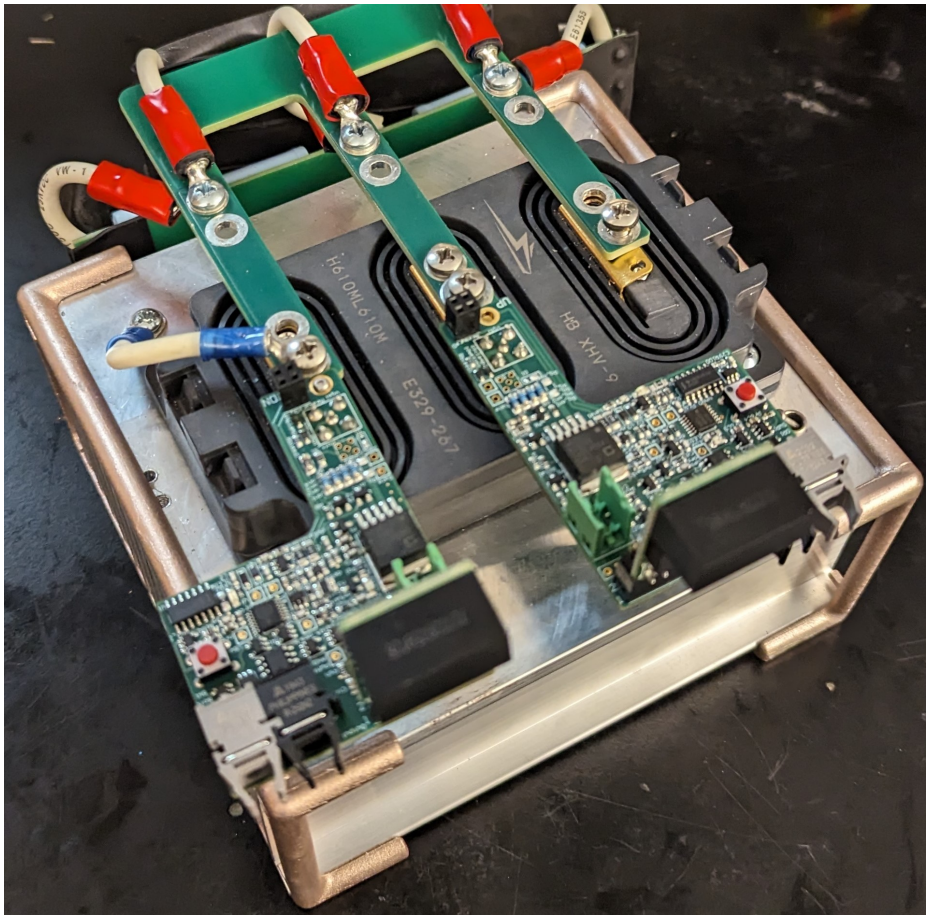
6.2.4 Field Shaping for MV Power Modules

The proposed field shaping is not only valid for the discrete 10-kV SiC devices, but also the heatsinks for MV power modules, such as XHV-9. **Fig. 6.11** shows a heatsink with field shaping for the XHV-9 power module. Tests have also been performed with a pair of heatsinks at 40 mm apart, and the results show that without the field shaping, the corona onset voltage is 9.3 kV, while the onset voltage increases to 13.3 kV with the proposed field shaping.

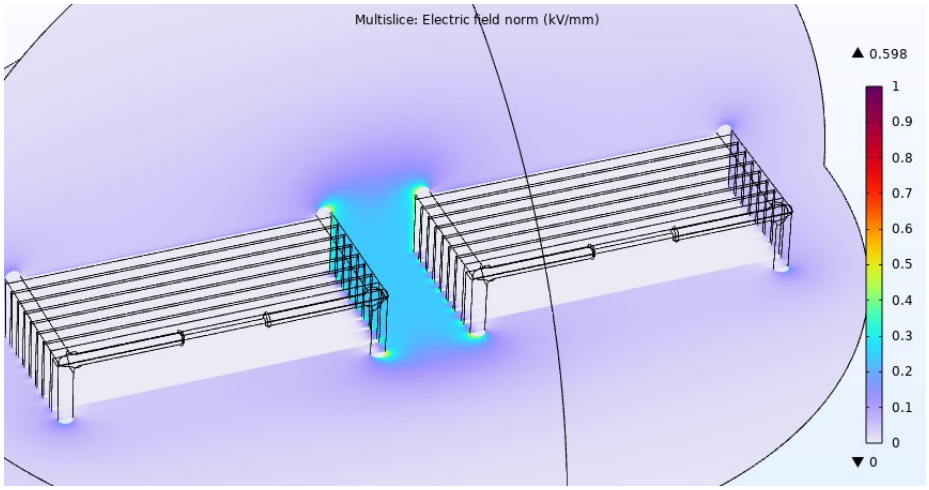
6.3 Simplified Gate Drive Design

To simplify the use of 10-kV SiC devices, commercial gate driving solution for SiC MOSFETs has been adopted, with minor circuit change. In this implementation, the gate drive integrated circuit *IX4351* is selected, and **Fig. 6.12** illustrates the overall design of the gate drive, similar to the ordinary low voltage MOSFET gate drive configurations.

On-chip desaturation protection (DESAT) is used to protect the device from overcurrent and short circuit faults, while the configuration has to be adapted for 10-kV SiC devices. As the voltage drop of the 10-kV SiC devices is higher compared to the 1.2- or 1.7-kV SiC MOSFETs, the desaturation voltage supply and threshold voltages have to be elevated. **Fig. 6.13(a)** shows the key schematic diagram for desaturation protection. First, the DESAT supply voltage is increased to 40 V by an isolated power supply *R24P22005D* from RECOM Power. Then, four 3.3-kV



(a)



(b)

Fig. 6.11: A heatsink with field shaping for the XHV-9 module: (a) photograph, and (b) simulation result.

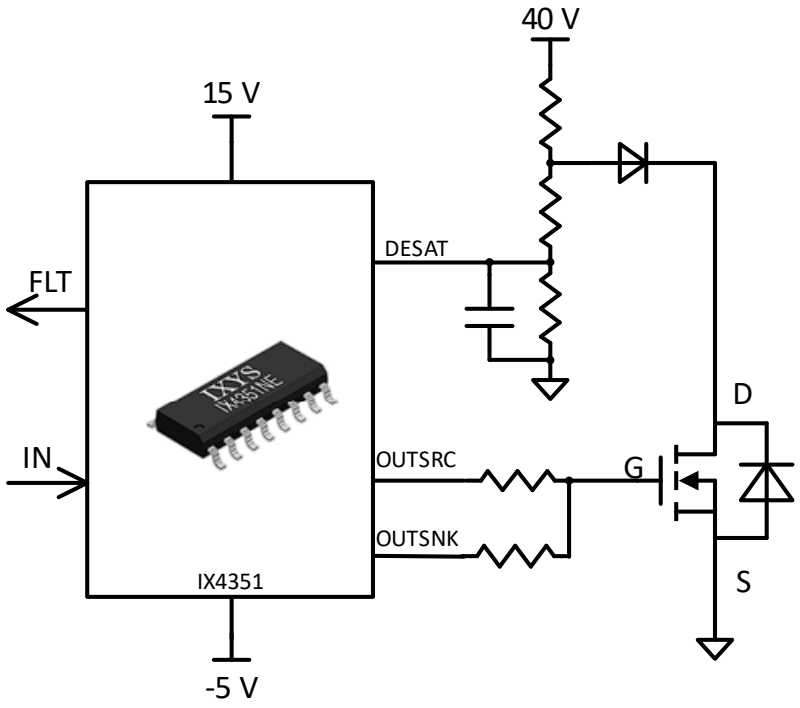
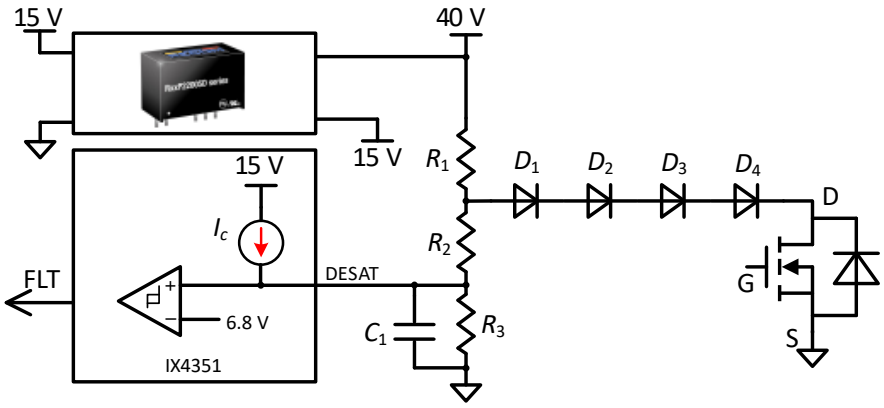
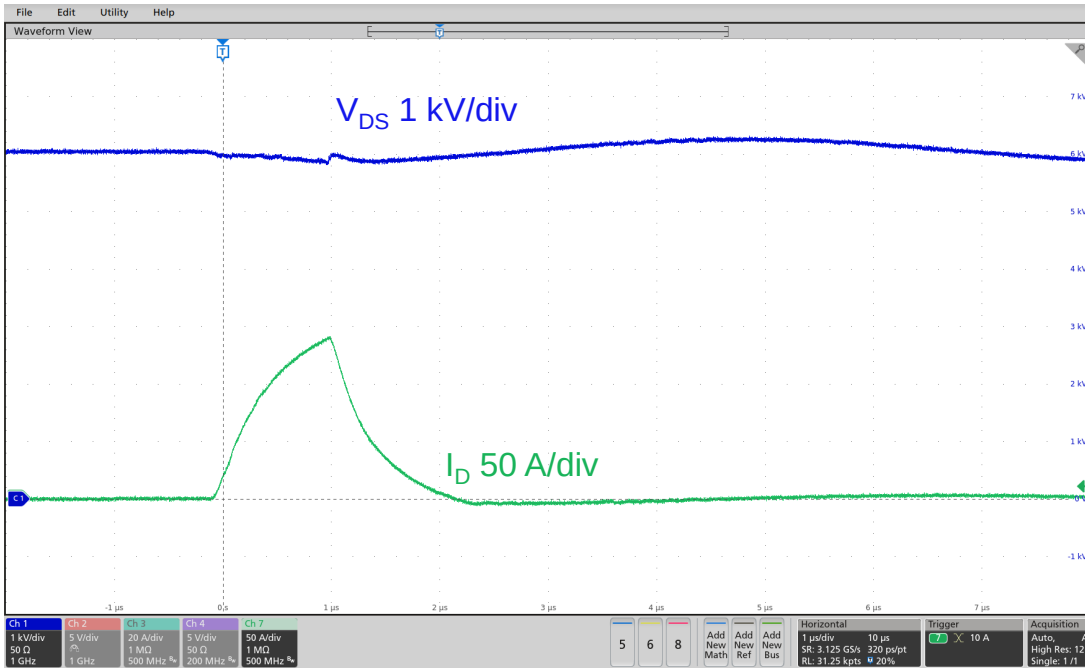


Fig. 6.12: Gate drive schematic for discrete 10-kV devices [34].



(a)



(b)

Fig. 6.13: (a) Schematic and (b) test waveform for DESAT protection [34].

SiC diodes are series connected as the DESAT diode, to undertake the high reverse blocking voltage (6.25 kV). As the current rating and packages of the SiC diodes are small, the reverse blocking voltage should be derated to avoid its thermal runaway due to leakage current at reverse bias. Unlike the DESAT protection for low voltage devices, the node voltage of the DESAT circuit is further scaled down by using a resistor divider R_2 and R_3 to match with the threshold voltage in the chip. As inside some of the gate drive IC the DESAT port is driven by a current source, the threshold voltages in this case are related as

$$V_{desat,th} = \frac{R_3}{R_2 + R_2}(V_{DS,th} + nV_D) + I_c(R_2 \parallel R_3) \tag{6.1}$$

Where, $V_{desat,th}$ is the threshold in the IC, and $V_{DS,th}$ is the threshold of MOSFET drain to source, and V_D is the forward voltage drop of each SiC DESAT diode. For the gate drives without current source driving the node, I_c can be set to 0.

The device short circuit test is shown in **Fig. 6.13(b)**, showing that the proposed DESAT protection successfully protected the MV SiC device at a device short-circuit fault. The threshold is set to at 50 A room temperature, and the blanking time is 700 ns, including 250 ns delay inside the . As the device current hit the threshold, the drain-to-source voltage rises to the threshold, and the voltage across C1 keeps increasing until the on-chip DESAT protection is triggered. The peak short-circuit current through the device is 140 A, which is acceptable for the devices.

6.4 Power Stage Assembly and Test

6.4.1 Bus Bar Design

The bus bar design for half of the MV power stage is depicted in **Fig. 6.14**, and the other half is fully mirrored. In **Fig. 6.14**, C represents the ceramic decoupling capacitors. The PCB is mainly used to connect the MOSFET sources, decoupling capacitors, and bulk capacitor bank, and the rigid PCB can provide rigid mechanical support to prevent wire deforming and short circuit faults. The high voltage insulated wire is only used to connect the bus bar PCB to the lower MOSFET drains. Conformal coating is applied to the bus bar and capacitor bank PCBs, along with the air clearance, and wire silicone insulation to provide insulation barriers. The commutation paths and corresponding parasitic inductances are shown in **Fig. 6.14** with different colors. Thanks to the decoupling capacitors, the loop can be minimized with PCB traces and wires. The total parasitic inductance outside of the 10-kV SiC devices is 60.8 nH, which is reduced by 78% compared to the power stage PCB with 288 nH in [113].

6.4.2 Power Stage Assembly

With the proposed heatsink configuration, the MV H-bridge power stage with 10-kV discrete devices has been assembled as shown in **Fig. 6.15**. The power stage is rated for 6.25 kV/10 A for a 10-kHz dual-active-bridge converter. Dc-link of 2.5 µF is included in the design, along with the PCB bus-bar to reduce commutation loop.

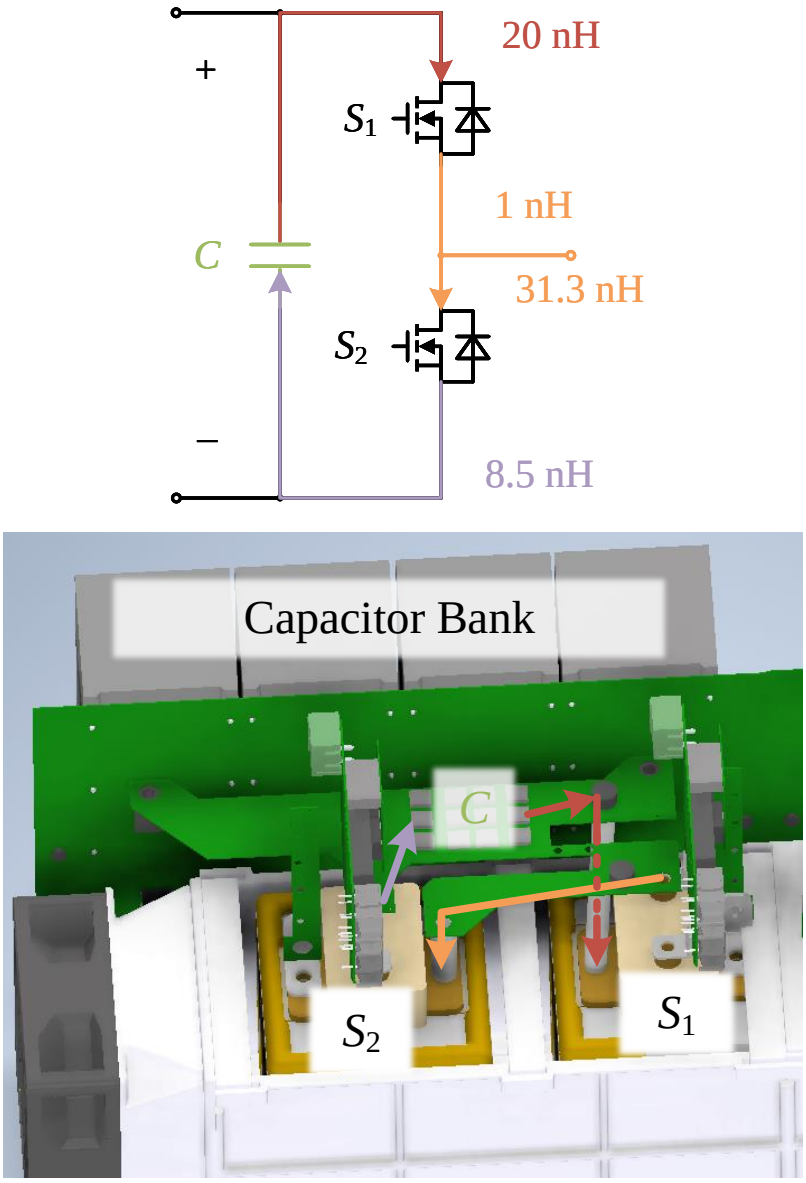


Fig. 6.14: 10-kV SiC power stage power loop and parasitic inductance [34].

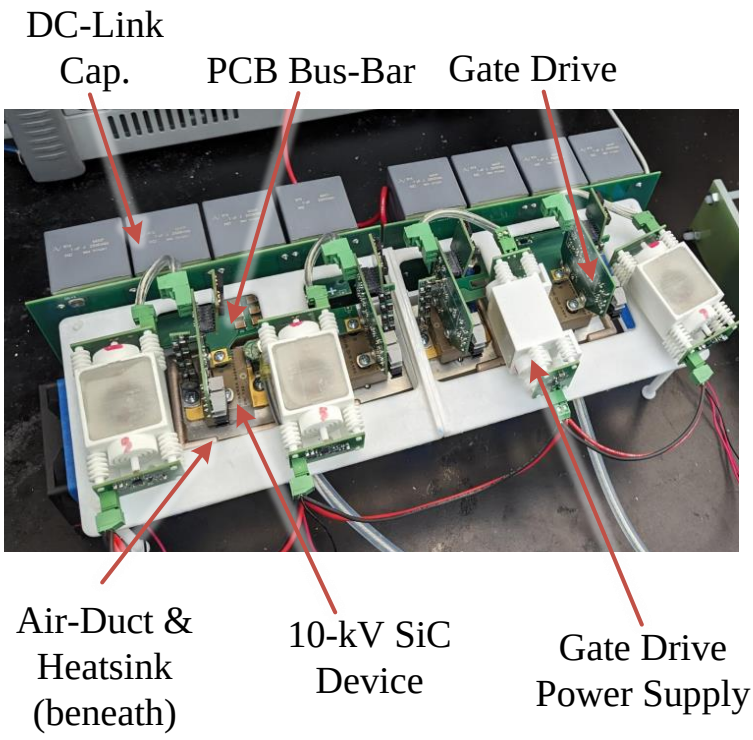


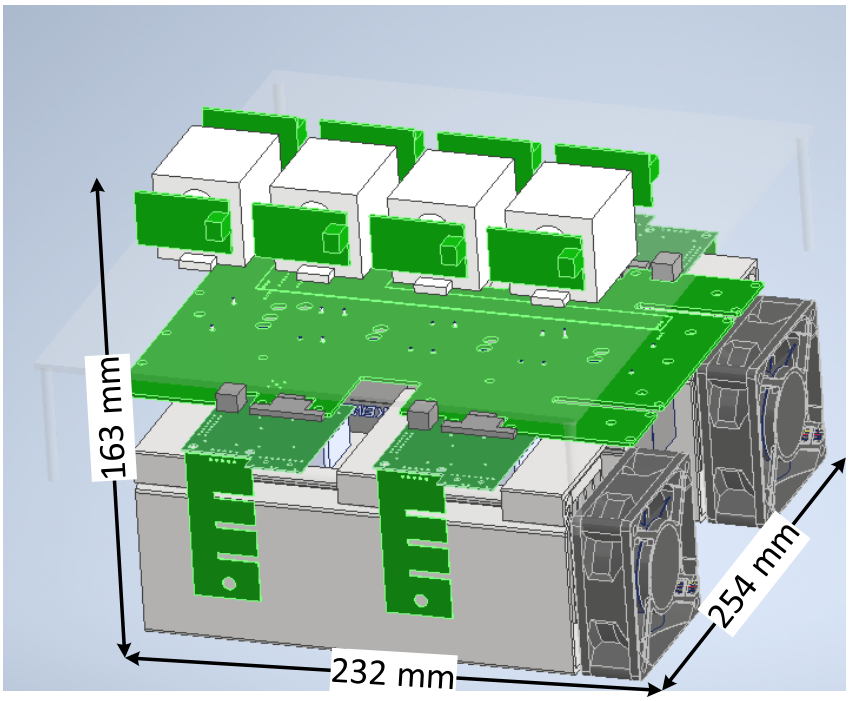
Fig. 6.15: Photograph of the assembled MV power stage with proposed heatsink structure [34].

With the proposed heatsink design, and the other components including gate drive power supplies [110], the power stage dimension including the dc-link is 408 mm W×138 mm D×146 mm H, which has been reduced by 30% compared to the original design, while the DC-link capacitance increased from 0.5 µF to 2.5 µF (see **Fig. 6.16**).

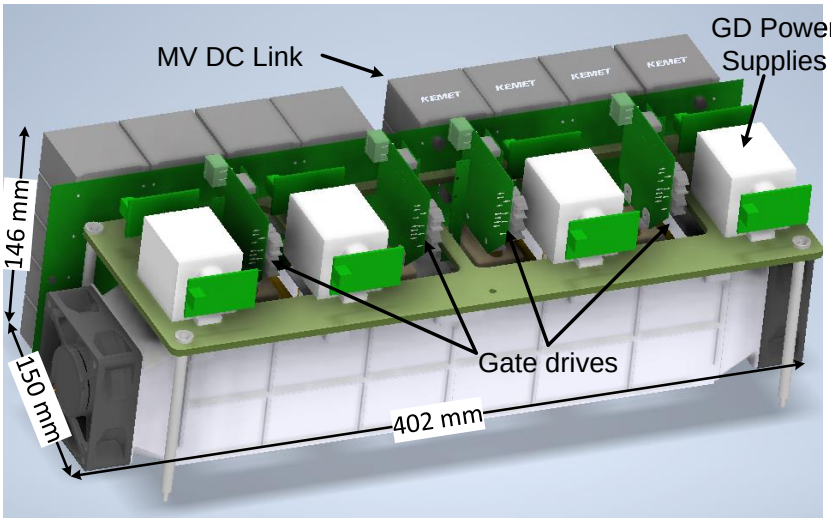
Fig. 6.17 shows the test waveform and that the power stage has been tested up to 6.25 kV/10 A with a LV side-shorted MV DAB transformer. The case temperature of the devices has been measured with an infrared thermal imager, as shown in **Fig. 6.18**, and the steady state hot spot is 32℃ on the device case. The surface temperatures of the device S_1 and S_2 are also recorded by the fiber optic temperature sensor in **Fig. 6.19**. Both **Fig. 6.18** and **Fig. 6.19** implies that the device case and the maximum temperature of the heat sink is close to 32℃ in steady state. Compared to the simulation results in **Fig. 6.10**, the heatsink temperature is approximately 10℃ lower, so the actual device junction temperatures should be below 70℃ due to the conservative estimation of device loss, validating the cooling design of the proposed power stage.

6.5 Summary

In this chapter, a compact heatsink structure has been proposed for 10-kV SiC-based power stages.



(a)



(b)

Fig. 6.16: Volume comparison (a) old design and (b) proposed design of the MV power stage [34].

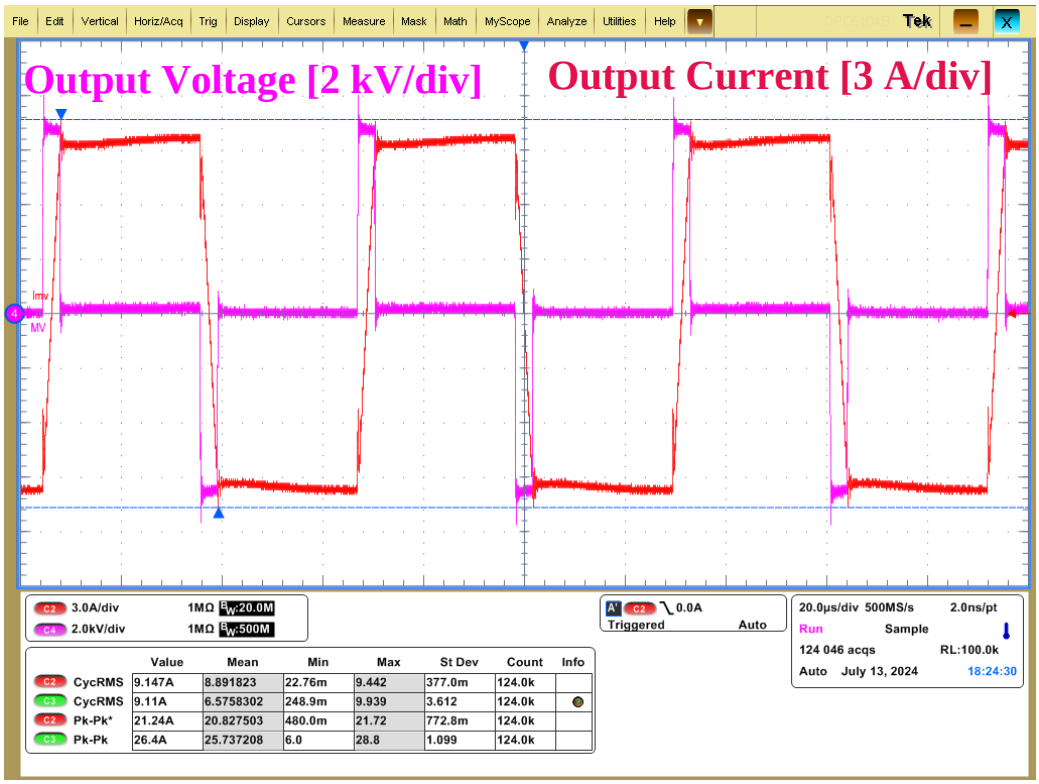


Fig. 6.17: Photograph of the assembled MV power stage with proposed heatsink structure [34].

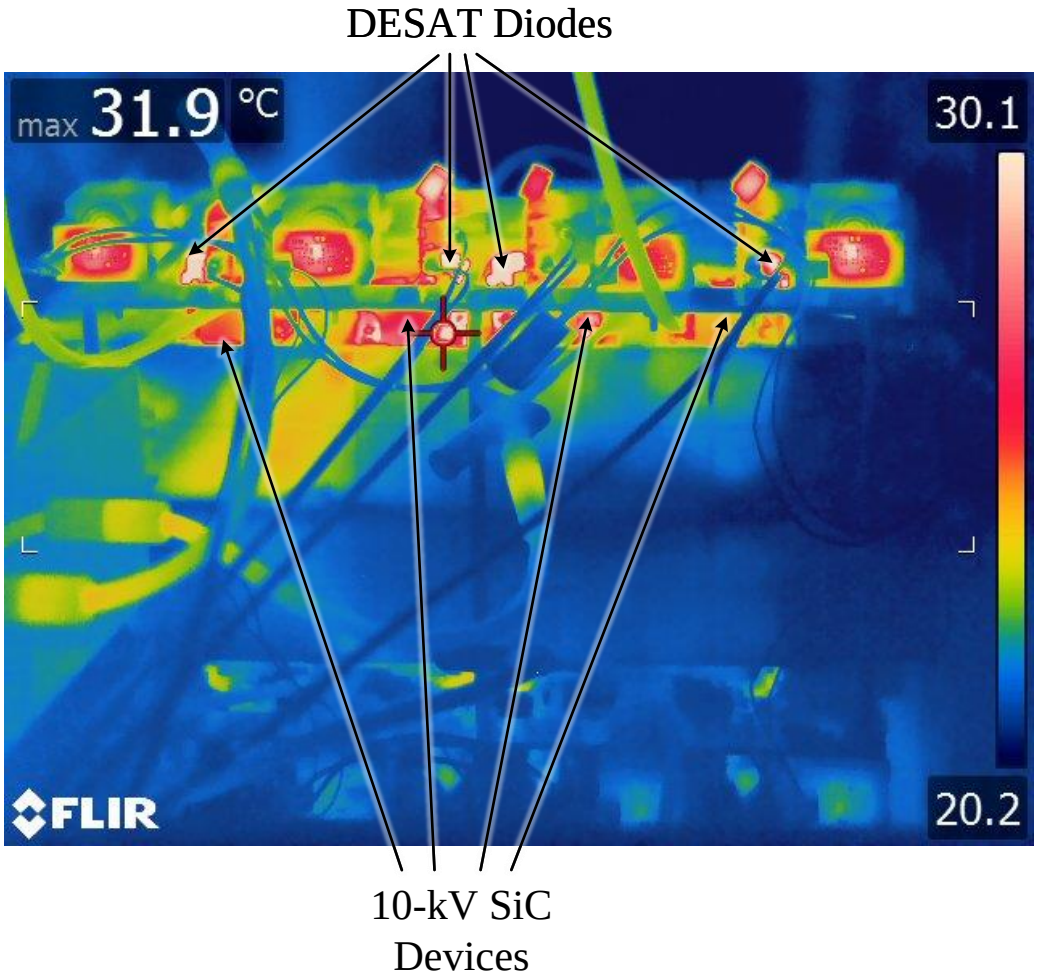


Fig. 6.18: Thermal image of the proposed MV power stage [34].

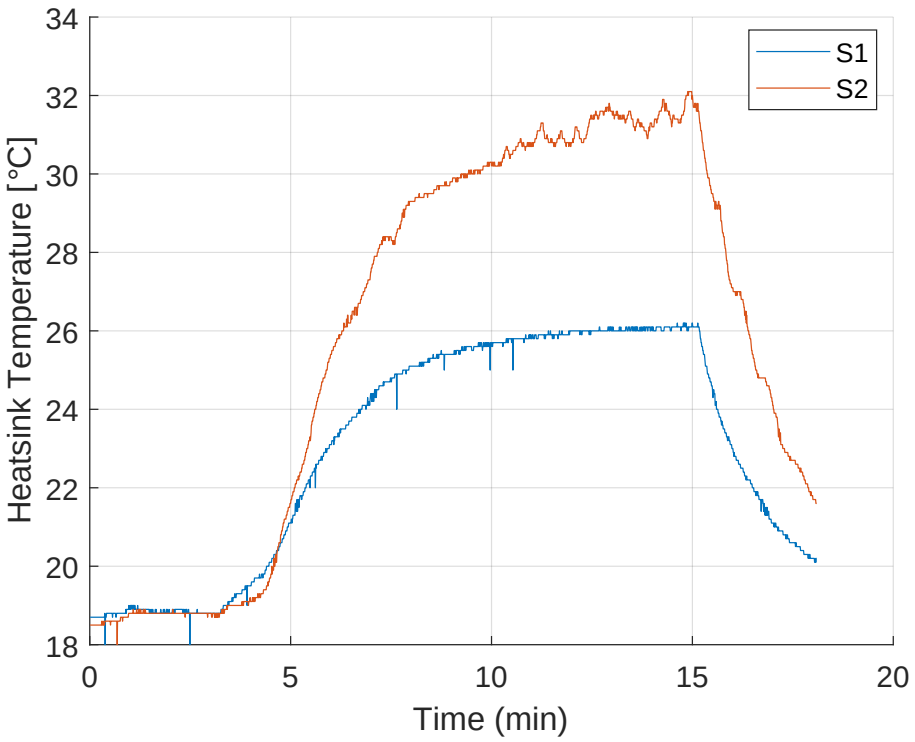


Fig. 6.19: Heatsink temperature measurement of the proposed MV power stage.

- First, the field shaping structure for MV power stage has been proposed and validated. The proposed field shaping structure is tangential to the heatsink surface at the right angle edges. The test results have shown that, with the proposed field shaping technique the breakdown voltage can be increased by 33%.

- The air duct considering mechanical support and creepage distance has also been proposed. With the bumped air duct structure, mechanical support can be provided to the heatsinks and devices and circuitry above them. The bumping and ramp structures also can provide extra creepage distance to prevent surface discharge.

- The proposed structure, with field shaping and air duct techniques, has also been applied and validated in XHV-9 10-kV SiC power modules for a flying capacitor converter.

- Simplified gate drive design using commercial IC solution has also been proposed. With the commercial gate driver IC *IXYS4351*, the gate driving functionality along with the DESAT protection can be fulfilled. With the architecture, the design procedure and implementation can be simplified.

- The PCB bus bar design can provide both insulation capability and minimized commutation loop for the power stage. The power stage has been verified

through experimental test up to 6.25 kV/10 A, and the total converter volume is reduced by 30% with higher DC-link capacitance installed.

Chapter 7

Harmonic-Based Transformer Flux Balancing Strategy for MV DAB Converters

7.1 Literature Review

7.1.1 Problem: Transformer Flux Unbalance

Since the medium voltage medium frequency transformers are having higher and higher power densities, the utilization of the core and all other materials have been pushed higher, and design margin to the physical limit has become less. As the high flux density, current density, and the smaller semiconductor devices being used in the transformer and DC/DC converters, the safe operation has to be secured in case of

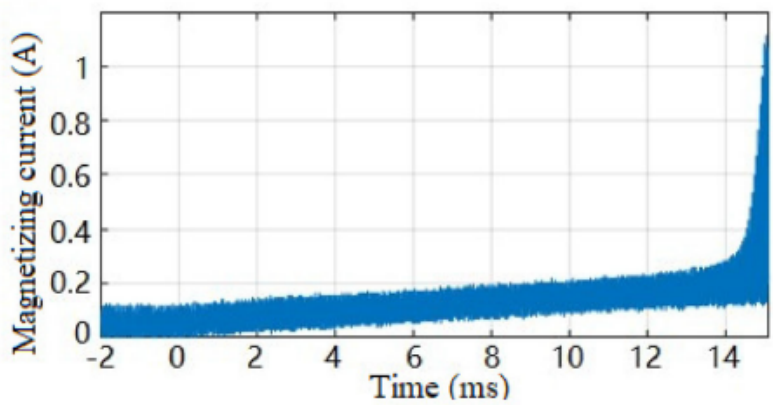


Fig. 7.1: Magnetizing current run-away during nanocrystalline-based transformer flux unbalance [22].

any possible fault or failure of the components. Hence, the reliable operating of the transformer is more and more important not only to the transformer itself but also to the stable operation of the whole converter system.

Because of the designed higher flux density, the transformer saturation may become a severe issue, because the voltage and switching timing mismatches could introduce volt-second unbalance into the medium frequency transformer (MFT), as has been discussed in [114–116]. In the low-frequency range, the MFT magnetizing impedance appears to be modest, allowing DC bias to accumulate slowly in the transformer magnetizing current. The DC component superimposed on the transformer current may induce higher loss on devices and transformer, or even saturate the transformer core and causing more severe issues, such as over-current failure of power devices [35, 22]. In **Fig. 7.1**, the average of magnetizing current increases rapidly when the core gets saturated due to the accumulation of unbalanced core flux [22].

There is a difference between the DC component in transformer winding current and magnetizing current, especially for transient bias in a multi-switching-cycle range. From **Fig. 7.2**, the phase-shift between two H-bridges changed suddenly, and without any compensation, the current spike is clearly shown in the primary side winding current, which lasts for several switching-cycles, while in the magnetizing current, no significant spike or balance can be found. The unbalance of the transformer magnetizing current during load or control transients should be based on the duty-cycle on primary and secondary voltages and the distribution of the leakage inductance. The phase-shift change can introduce large current spikes in winding. As the current spikes will be seen on both sides of windings and finally canceled by each other, much less spikes on the magnetizing current can be found. As for the steady DC component, the DC bias on two sides of the transformer is superimposed, and

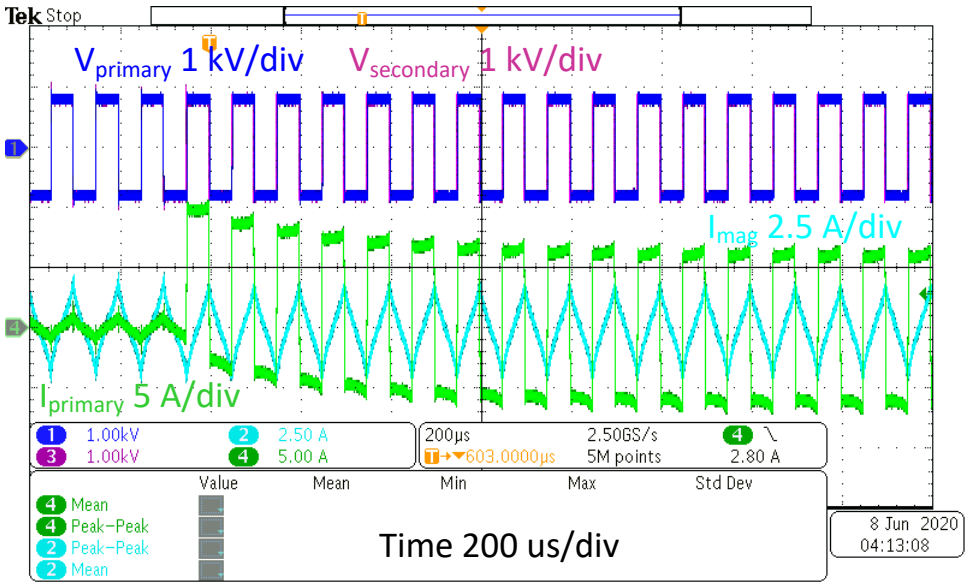


Fig. 7.2: Winding and magnetizing currents during load transient.

therefore, the total DC bias in magnetizing current is the weighted sum of DC bias in winding current based on the transformer ratio. The DC bias on two sides can add-up, or cancel the DC component in the magnetizing current, and therefore, the core flux unbalance.

7.1.2 Flux Unbalance Estimation

In steady-state, the majority cause of the flux unbalance, or the DC bias in the core flux, is the inconsistency of the devices and gate drive signals [115, 116]. As the core flux is determined by the magnetizing current, and the magnetizing current of the transformer is determined by the volt-second products of the waveforms of the primary and secondary voltages, the deviations of pulse width and amplitude of the transformer voltages may cause the steady-state DC bias of the voltage, and hence, the magnetizing current waveforms. Ref. [115] gives a detailed analysis on predicting the DC component of magnetizing current and the transformer flux, considering the mismatches of device turn-off time, and the voltage drops for both IGBT- and MOSFET-based converters. It is reported that the unmatched turn-on time has no impact on the flux unbalance, but the mismatched turn-off time does introduce significant DC bias. For MOSFET-based converters, during the process of Zero-voltage-switching (ZVS), the turn-off time can be strongly associated with the flux unbalance. And it is found that the DC bias on each side is caused by the mismatch on the respective side, which means the analysis based on DAB can be extended to multi-port active bridge converters [115].

However, the flux unbalance may also be caused by the other factors, such as the resolution of digital controller, gate signal delays, etc., which introduces further complexity on the model. It is also unclear for the level of deviations on each factor. Therefore, the analysis may exhibit a rough relationship between each factor and flux unbalance, but may not precisely reveal the amount of flux unbalance in real converters.

7.1.3 Flux Unbalance Detection

The unbalance detection, as the feedback, may be required for certain closed-loop control-based flux balancing methods. However, since the amplitude of the magnetizing current is designed significantly lower than the winding currents, and the turns ratio may be complex, it is not always easy to measure the magnetizing current out of transformer winding currents. Therefore, several ways of measuring or revealing the flux unbalance have been proposed in the literature. In most cases, detecting the flux unbalance can be realized by sensing the magnetizing current, and then, the amplitude and polarity of DC bias in the magnetizing can reveal the severeness and polarity of the flux unbalance.

Magnetizing Current Sensing

The straightforward of sensing the transformer flux is to measure the magnetizing current of the transformer. In [41, 117, 118], the steady-state DC component of the magnetizing current was extracted by measuring the winding currents, in which the

magnetizing current can be derived by adding the two winding currents together, with the corresponding turns ratio.

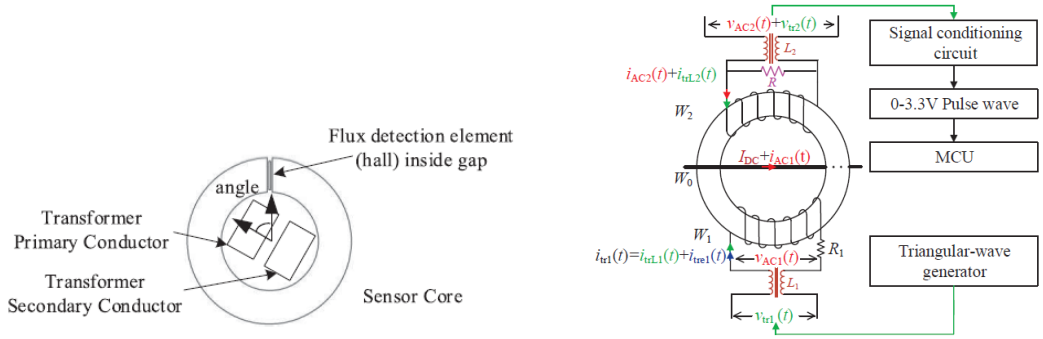
$$i_{mag} = i_p + \frac{N_s}{N_p} i_s \tag{7.1}$$

Where, the I_{mag} is the magnetizing current, $i_p,\ i_s$ the primary/secondary currents, $N_p,\ N_s$ the numbers of turns on both sides. However, as in medium voltage DC/DC converters, the magnetizing current is small compared to the winding current, which demands a high resolution on measuring the winding currents, and measuring a small DC bias, superimposed by a large AC signal, could be difficult due to the sensor circuitry offset.

It can be easier for the transformers with the unity turns ratio. Ref. [22] discussed a method to sense the magnetizing current by using only one single current sensor. Since the turns ratio is unit, the magnetizing current is

$$i_{mag} = i_p + i_s \tag{7.2}$$

Then, similar to measuring the common-mode current, the two windings can be clamped together with one single current sensor (see **Fig. 7.3(a)**) [22]. In this way, the measurement resolution and implementation can be easily improved. Nevertheless, this direct measurement method still remains challenging for transformers with high-voltage insulation and almost irreducible turns ratio.



(a) **(b)**

Fig. 7.3: Magnetizing current sensors (a) for unity turns ratio [35], (b) based on flux gate [36].

Another way to customize the current sensors to detect DC signal out of large DC+AC signal is to use the flux gate sensor. Instead of measuring DC+AC signals precisely, a flux gate sensor can measure only the DC with a high precision [36] (see **Fig. 7.3(b)**). So, it is suitable to use flux gate to measure the DC bias on each side of the transformer, and then the DC bias of the transformer magnetizing current can be then derived, though this method require complicated circuitry and extra magnetic cores has to be used for its fabrication.

Magnetic Flux Sensors

Apart from measuring the magnetizing current, the transformer flux can be measured, too. Magnetic structures can be made to create another branch along with the main magnetic branch of the transformer core, so that the flux of the core can partially flow into the added magnetic shunting branch. The extra magnetic branch can be wound with some picking up winding, and therefore, the flux flowing within the branch can

induce a voltage signal. By analyzing the voltage signal of the picking up winding, the information of the transformer flux balancing can be extracted. In [38], both external and internal flux sensors have been proposed. In the proposed basic external sensor, flux can be detected when the main transformer core is saturated. For the integrated internal sensor, it can be embedded in the core leg next to the air gap, and therefore, part of the main flux can be directed into the branch and picked up by the coil during both the normal and saturated operations [38].

In [37, 119], a method of "Magnetic Ear" has been introduced (see **Fig. 7.4(a)**), which is similar to the external magnetic branch. The placement of the "Magnetic Ear" has been studied, and extra circuitry has been added to extract the inductance of the "Magnetic Ear". The drawback of this method is also obvious, as it only works for the ferrite cores, because the complicated core structure may need further machining, and the circuitry can also be complicated compared to the other methods.

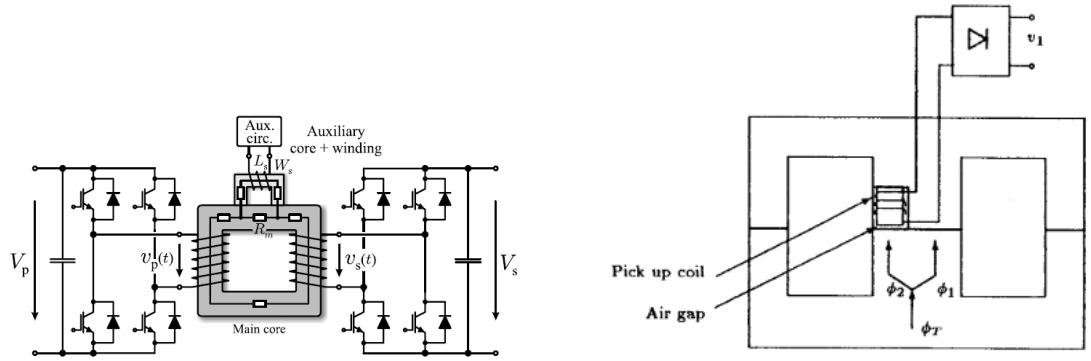


Fig. 7.4: Magnetic branch-based flux sensors: (a) the "Magnetic Ear" [37], (b) internal flux sensor [38].

The transformer flux can also be sensed by the Hall effect sensors that can be embedded in the transformer air gap (see **Fig. 7.4(b)**) [120]. However, this means that the transformer has to have air gap inserted, and the insertion of the Hall effect sensor may bring challenges on fabricating the sensor.

Magnetostriction Sensor

Since the cores may vibrate due to magnetostriction with AC magnetizing excitation, which might be undesirable if the acoustic noise is too strong. However, the flux unbalance may also possible be represented by the mechanical vibration, allowing piezoelectric transducers serving as the sensor to detect the flux unbalance. In [39] a DC+AC flux sensor utilizing the magnetostriction effect has been proposed (see **Fig. 7.5**). During the operation of the transformer or inductor, a high frequency small signal can be induced with an excitation winding, so the transformer flux can

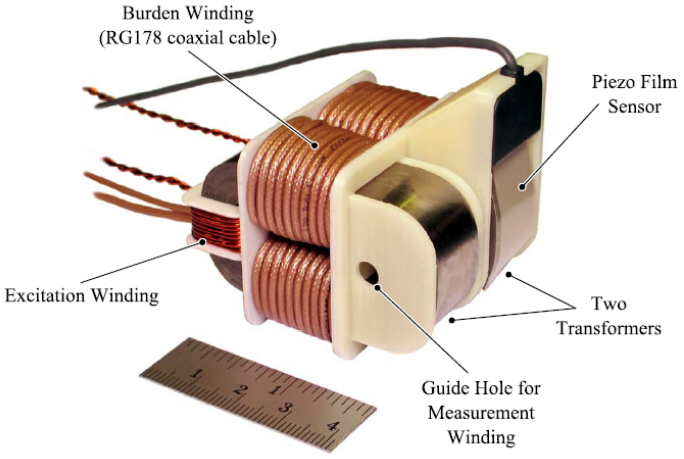
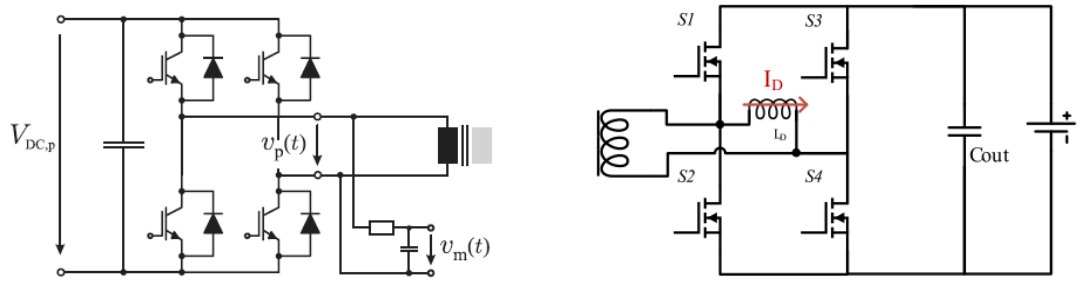


Fig. 7.5: The photograph of the magnetostriction based flux sensing [39].

be modulated with the exciting signal, and then a piezoelectric sensor can pick up the modulated vibration signal, and finally, the flux information can be extracted by signal processing. However, by using this method, the complicated exciting, sensing and signal processing procedures may bring considerable amount of challenge. And, it may not work for some materials having low magnetostriction, such as the nanocrystalline.

Volt-Second Product Measuring

Since the source of this flux unbalance issue is ultimately caused by the unbalanced volt-second product of the transformer terminal voltage, the DC bias of volt-second product can be measured and then controlled. To measure the DC bias of the transformer terminal voltage, **Fig. 7.6** shows that *RC* filtering circuit or paralleled inductor can be connected to each port of the transformer [121, 40]. With this method, extra *RC* or inductor circuit has to be made to withstand the high voltage, and the following current or voltage sensor with high insulation requirement has to be designed, which introduces extra challenges on implementation.



(a) **(b)**

Fig. 7.6: Volt-second based measurement: (a) *RC* filter [39], (b) paralleled inductor [40].

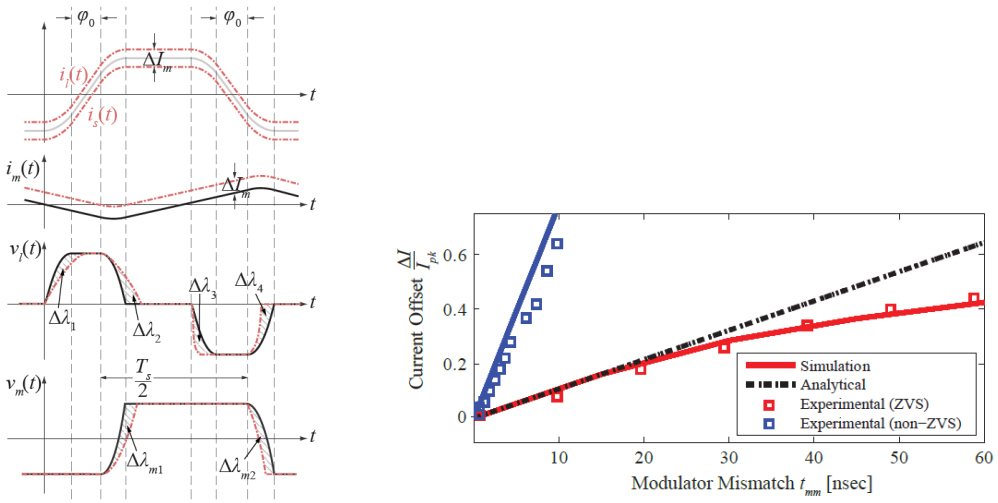
7.1.4 Flux Balancing Methods

With the introduced estimation and detection methods, the flux can be balanced passively and actively.

Passive Balancing

First, the intuitive way to suppress DC bias of the magnetizing current is to suppress the DC current in each winding, and a simple way is to insert series connected DC blocking capacitors on each side, as capacitors naturally reject the DC signal. However, the topology can be similar to the series resonant converters, which brings the resonant poles in the circuit, so the capacitance should be sufficiently large to avoid any potential resonance. Hence, the DC blocking capacitor may introduce more volume, cause extra loss, and also affect the converter transient response.

Ref. [122, 123] reported that in converters having ZVS features, the volt-second product can be limited by the features brought by the zero-voltage transition (ZVT). During the ZVT, the current of the transformer is charging the output capacitances of the semiconductor devices, providing an effective series capacitance to limit the DC bias on each side, which means that to some extent, the transformer flux can be adaptively compensated during the ZVS operation, due to the effect of resonance in dead-time, as is shown in **Fig. 7.7**. However, with a high switching current or at the hard switching region, either the duration of resonance is significantly shorter, or the resonance is not formed. As a result, the effectiveness at those conditions is less or none [122].



(a) **(b)**

Fig. 7.7: ZVS inherent balancing: (a) waveforms of inherent balancing, (b) effectiveness with modulation mismatch [41].

Steady-State Control

For the steady-state flux balancing, closed-loop control-based method is widely used. By using the feedback signal from all types of flux and current sensors, the magnitude and polarity of the flux unbalance can be found, and then be corrected by adjusting the pulse width of the converter bridges. PI controller-based methods are often used as the steady-state difference between the reference and feedback can be mitigated [41, 117]. Because the DC bias is of interest and the magnetizing current is with the switching frequency, multiple sampling within one switching cycle is usually needed [118, 124].

Transient Balancing

In [6, 22, 125, 126], the transient flux unbalance caused by the control or load transients has been addressed. Some of the method cope with the winding current spikes, which, however, may not necessarily be the DC bias in the magnetizing current, but instead simply the DC bias of the winding current. With an intermediate adjustment of phase shift or duty-cycle, the magnetizing current can be balanced for several modulation schemes, from the single phase-shift (SPS), to the more generalized triple phase-shift (TPS). The generalized modulation updating scheme is

$$D_x[k] = D_x[k-1] + \frac{\Delta D_x[k]}{2} \tag{7.3}$$

Where, $D_x[k]$ is the transformer voltage duty cycle of either side at the switching cycle k, and $\Delta D_x[k]$ is the backward difference of D_x at the cycle k. Some simulation waveform is shown in **Fig. 7.8**. Moreover, no matter how precise this method is used, it is not effective to the steady-state volt-second product, which exists if no action coping with steady-state mismatch is taken.

As has been mentioned above, multiple methods of estimating, sensing, and controlling the transformer flux unbalance have been introduced. From the literature, the estimation method can reveal the main part of the mismatch causing the transformer flux unbalance, and several flux measuring methods can be implemented by either sensing the magnetizing current, transformer flux, core vibration, as well

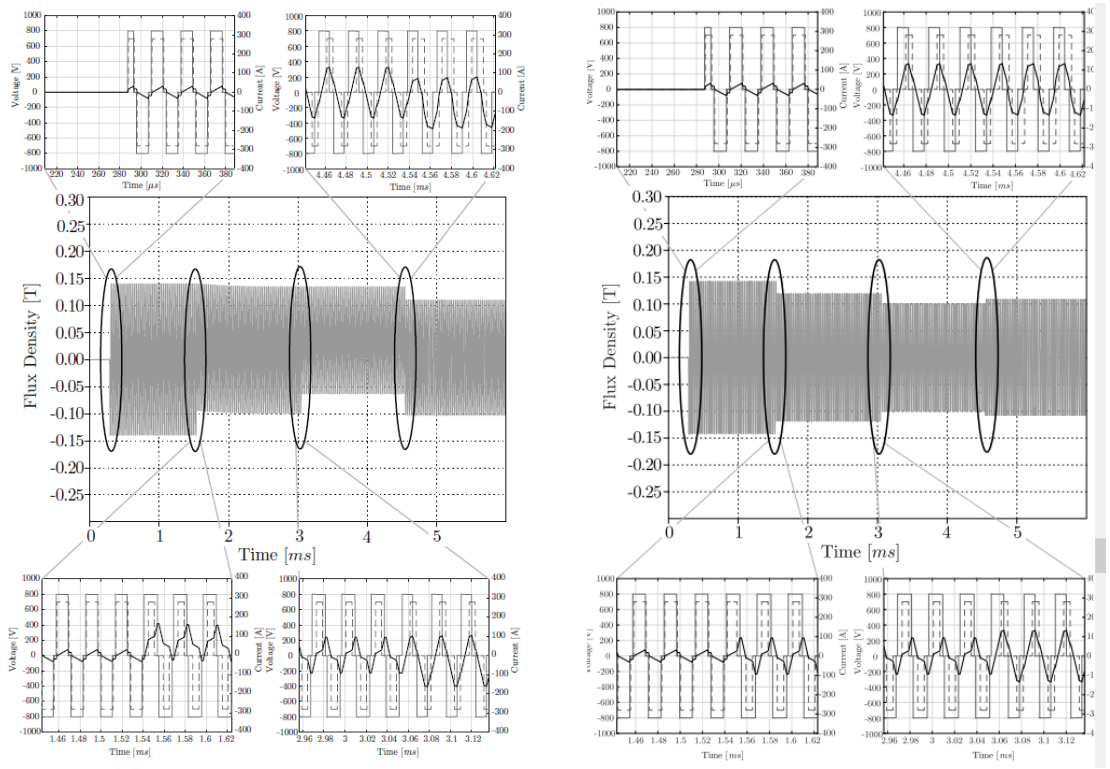


Fig. 7.8: Transformer flux density waveforms: (a) without transient balancing, (b) with transient balancing [6].

as converter volt-second unbalance. To control the flux unbalance, the passive ways using external or intrinsic capacitances in the converter topology mitigates part of the transformer flux unbalance, and the steady-state balancing mainly depends on the feedback-based active control schemes, while during the control and load transients, the volt-second product and the flux is balanced by the modulation methods. The methods can all work under certain circumstances.

However, for medium voltage DAB transformers, due to the specific requirement and application, not all methods are applicable. The volt-second product measuring method cannot be implemented because of the high operating voltage on both LV and

MV sides of the transformer, while the magnetostriction and flux measuring method can be over complicated for implementation, making them out of the scope for the real converter design. The current sensing method may be viable, but the insulation is a concern, for which the trade-off might be needed between the sensor ratings and precision, as the high voltage current sensors on the market tend to have a high current rating. Turns ratio can also be a concern, since the magnetizing current is to be measured, while for the implementation at least one side of the current has to be scaled by analog circuit or digital computing. In the next chapter, the aforementioned concerns will be considered to design a magnetizing current sensor applicable for unity and fractional turns ratio MFTs.

7.2 Flux Unbalance Analysis and Detection

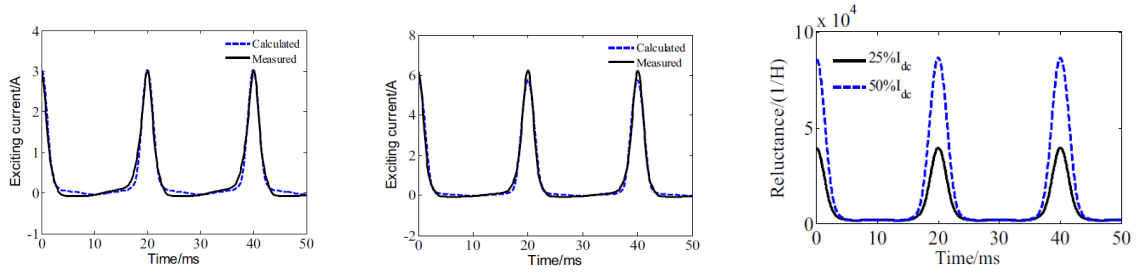
7.2.1 Magnetic Gap and Non-Linear Magnetizing Current

Introduce of the Magnetic Gap

As has been discussed in the literature review, several methods on flux unbalance detection have been proposed. A direct way is to measure the magnetizing current by sensing the winding currents [45]. Other ways are also available, such as flux Hall sensors, magnetic branches, magnetostriction sensors, and electrical filters. For medium voltage transformers, due to the implementation complexity, the current sensing method is still preferable. However, because of the large difference

between winding and magnetizing currents, strategies must be taken to improve the measurement accuracy. Otherwise, the flux unbalance, which is represented by the DC bias in the magnetizing current, will be submerged into the DC offset and sensing noises, bring a high challenge on stably balancing the transformer flux.

Thanks to the high permeability and saturation flux density of the advanced nanocrystalline and amorphous cores, higher operational flux density can be chosen for the medium voltage transformers to reduce their size. However, the higher flux density may lead to a smaller margin of the flux density, having the transformers expose to a higher possibility of saturation at flux unbalance [45]. In the meanwhile, due to the saturation of the transformer core, a higher magnetizing current will be observed as the magnetizing impedance will be reduced due to the core saturation. State-space based method has been used to estimate the magnetizing current waveform in the 50 Hz utility transformers, and from the test waveforms in **Fig. 7.9**, the DC bias of the transformer leads to variation of the core reluctance, and the magnetizing current spikes [42].



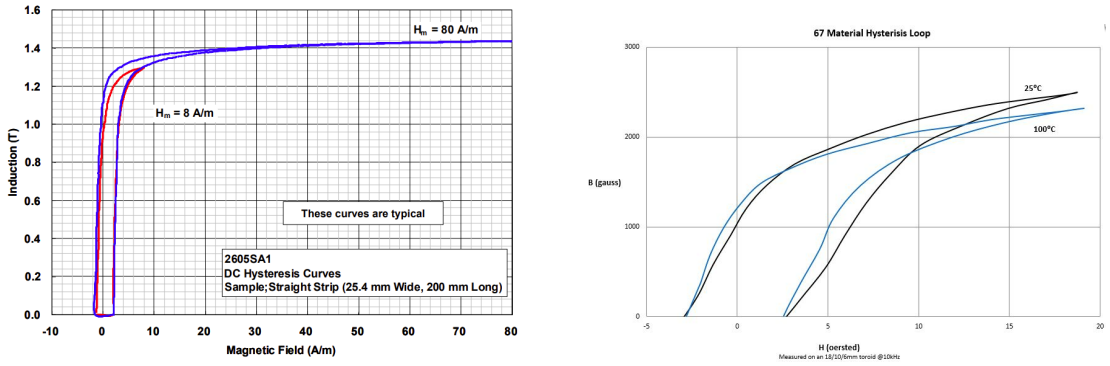
(a) **(b)** **(c)**

Fig. 7.9: Utility Transformer: (a) magnetizing current with 25% bias, (b) magnetizing current with 50% bias, (c) reluctance waveform of the core [42].

The results of saturation test of the 50 Hz utility transformer can also be extended into medium frequency medium voltage transformers. Due to the high operating point, partial saturation may be observed due to the non-linearity of the core, resulting in non-linear magnetizing current. If the flux DC bias is different, the saturation level within one switching cycle will be different, too. Then, the saturation may be used as the information to sense to extract the flux unbalance level, by which no DC bias measurement will be used for the flux balancing feedback.

However, because the high switching frequency makes the transformer power denser compared with the 50/60 Hz utility transformers, the evident flux unbalance may lead to a more severe situation quickly before the flux balancing control strategy functions. In other word, if the transformer saturates at an obvious level, the operational margin may be too small for the balancing control to work and lead to magnetic current run-away. That means, some non-linear factor may be needed in the magnetic loop so that the flux unbalance can be more evidently revealed before the core is saturated.

As some of the medium voltage transformers tend to have air gap to prevent saturation due to flux unbalance, one of the ways to introduce non-linearity in the transformer core is to replace the air gap with a magnetic gap. The magnetic gap can be a thin ferrite sheet with a lower saturation flux density, in contrast to the nanocrystalline and amorphous cores. **Fig. 7.10** shows the $B - H$ curves of the amorphous and ferrite materials [44, 43], from which it can be seen, the amorphous material have high permeability and saturating flux density, while the ferrite can have



(a) **(b)**

Fig. 7.10: $B-H$ loops of: (a) amorphous material from Metglas™[43], (b) ferrite material from Fair-Rite™[44].

relatively lower permeability and saturation level. If the saturation level of the two materials can be mismatched, a non-linear current curve with a partial saturation can be realized in the magnetizing current.

To verify the introduced non-linearity, two transformers with different ratings for the 850/850 V and 850/6700 V PCS have been made, and the parameters are shown in Table. 7.1. The 850/850 V transformer is made with two paralleled amorphous cores of **AMCC0125A**, and one ferrite sheet of **38M4010AA1212** on each side of the leg. The winding turn ratio is 34:34, rated voltage 850 V/850 V. The estimated saturation current of the transformer ferrite gap is 2.5 A (see **Fig. 7.11**). The peak-to-peak value of the magnetizing current is around 5 A.

In **Fig. 7.12**, the 850/850 V is working in full load mode, and the DC bias of 1.7 A in magnetizing current is inserted. Similar to the waveforms in **Fig. 7.9**, the transformer current is with large distortion, along with the significant DC bias. The peak-to-peak value is 6.8 A, much higher than that in **Fig. 7.11**, even though

Table 7.1: Parameter Comparison for 850/850 V and 850/6700 V Transformers

	850/850 V DAB Transformer	850/6700 V DAB Transformer
DC Voltage Rating (V)	850/850	850/6700
Turns Numbers	34/34	33/260
Switching Frequency (kHz)	10	10
Magnetic Gaps (mm)	2 × 0.13	2 × 0.23
Ferrite Saturation Level (A)	2.5	3
Current Rating (A)	19/19	19/2.43

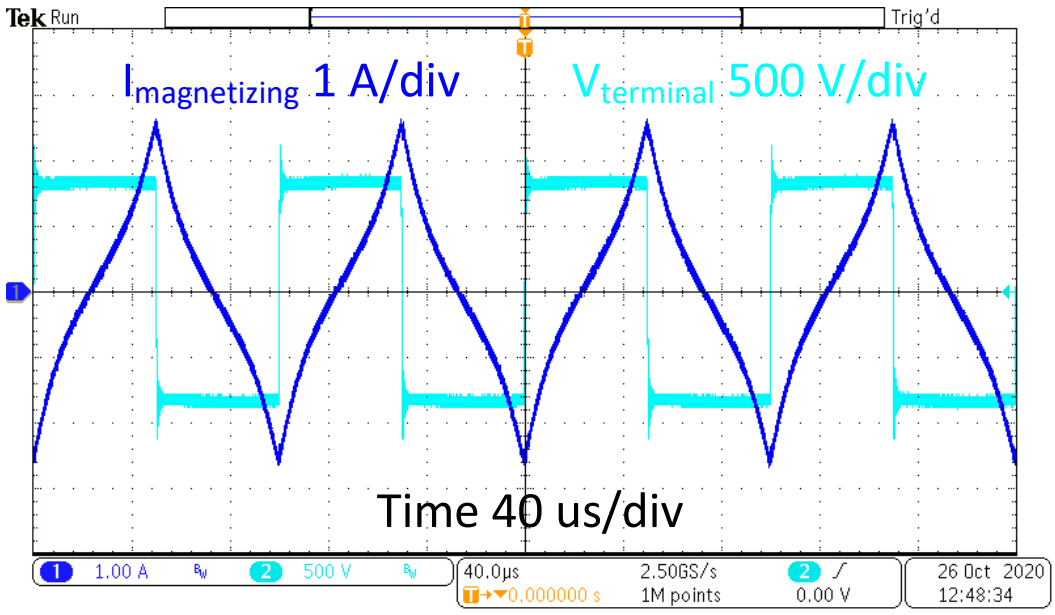


Fig. 7.11: The current waveform with ferrite gap in open-circuit test.

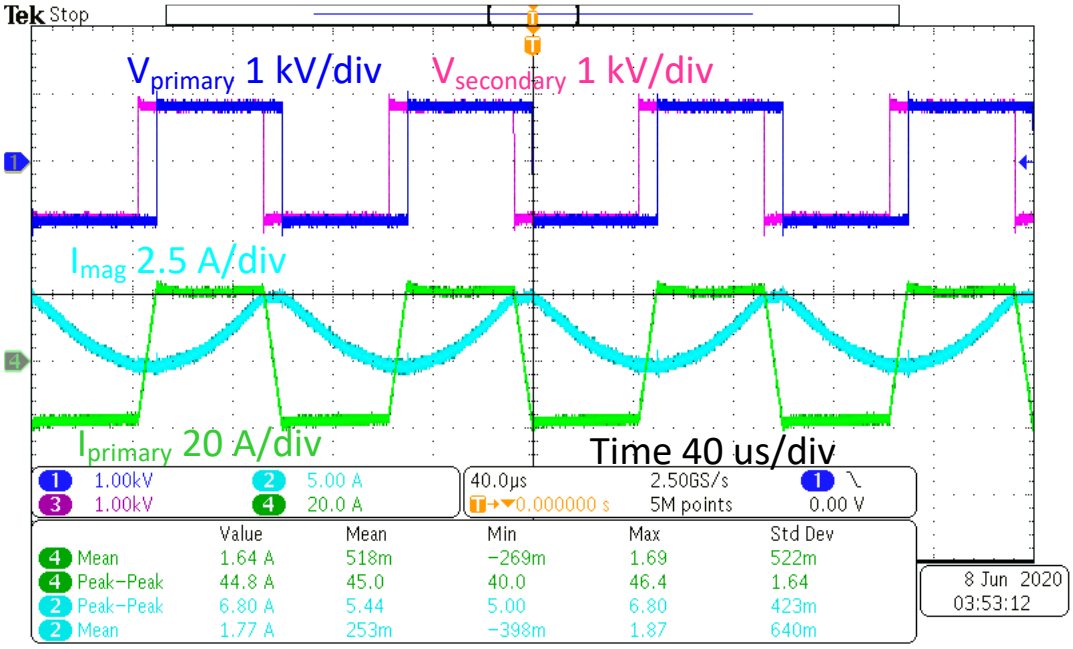
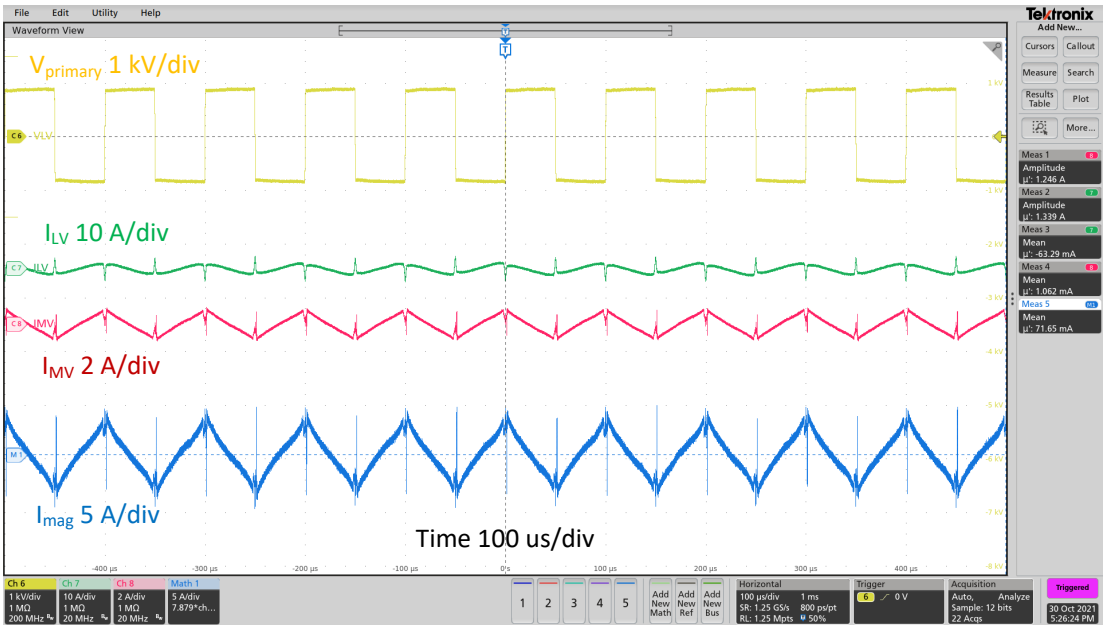


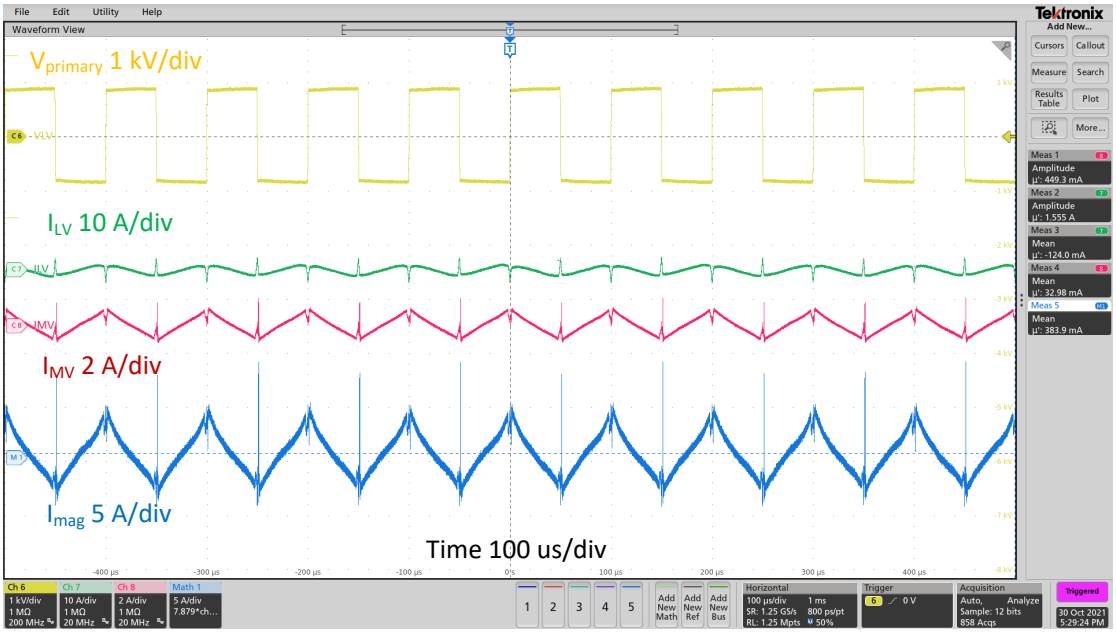
Fig. 7.12: The current waveform with ferrite gap in full load test with flux unbalance.

at the full-load condition the volt-second product in magnetizing current is lower. The positive and negative half-cycles are also asymmetric, which means different saturation level and the variation of the magnetizing current, the higher the current, the smaller the inductance, and hence the slower current slope.

Similar tests have also been done in the 850/6700 V DAB transformer. The MV transformer is made with nanocrystalline core of **SC2062M1** from MK Magnetics™, and ferrite gaps of **38M4010AA1212**, with which the estimated saturation level is 3 A. The turns ratio of the transformer is 33:260. The test results are depicted in **Fig. 7.13** at no-load and **Fig. 7.14** at full-load conditions. From the waveforms, due to the parasitic capacitance of the transformer windings, current spikes can be found on the current waveforms, while the shape of the partially saturated triangular shape can still be observed. In **Fig. 7.13(a)**, a minimal DC bias of 71 mA can be found, while in **Fig. 7.13(b)**, the DC bias of magnetizing current is 383 mA, and for **Fig. 7.13(b)**, the shapes of positive and negative are no longer symmetric, with the positive peak sharper than the negative valley. Similar in **Fig. 7.14**, the shape of transformer magnetizing current changes due to the phase-shift and higher eddy current loss in the laminated core, due to the high winding current. In **Fig. 7.14** (a), with the DC bias of 134 mA, the distortion of the current shape is small, while in **Fig. 7.14(b)**, the DC bias of the magnetizing current is 546 mA, with a sharper slope at the adjacent of the positive peak.

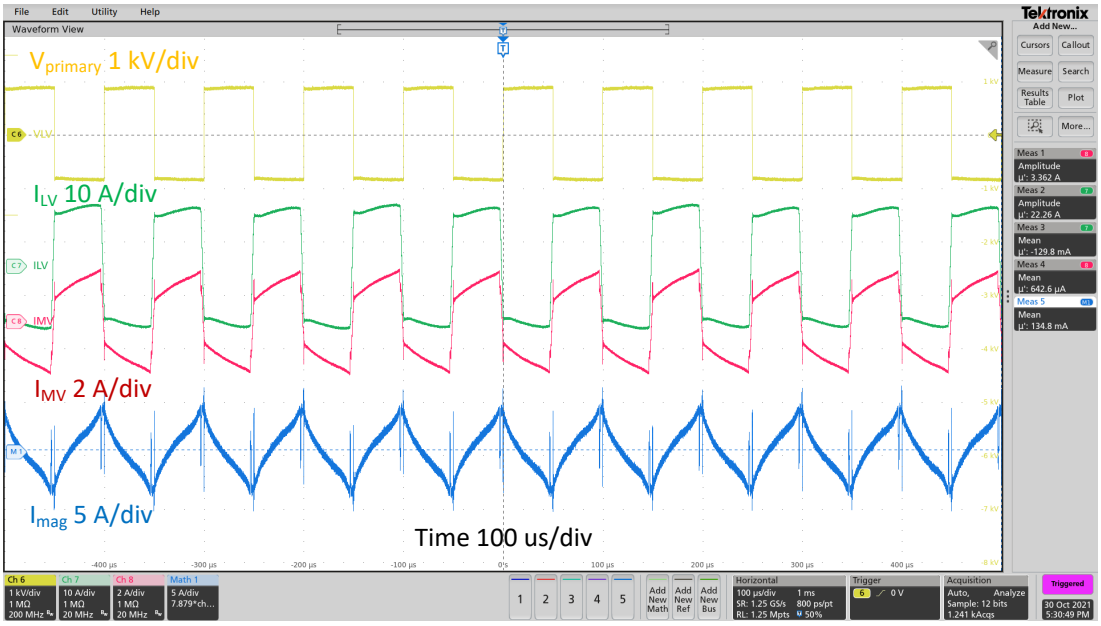


(a)

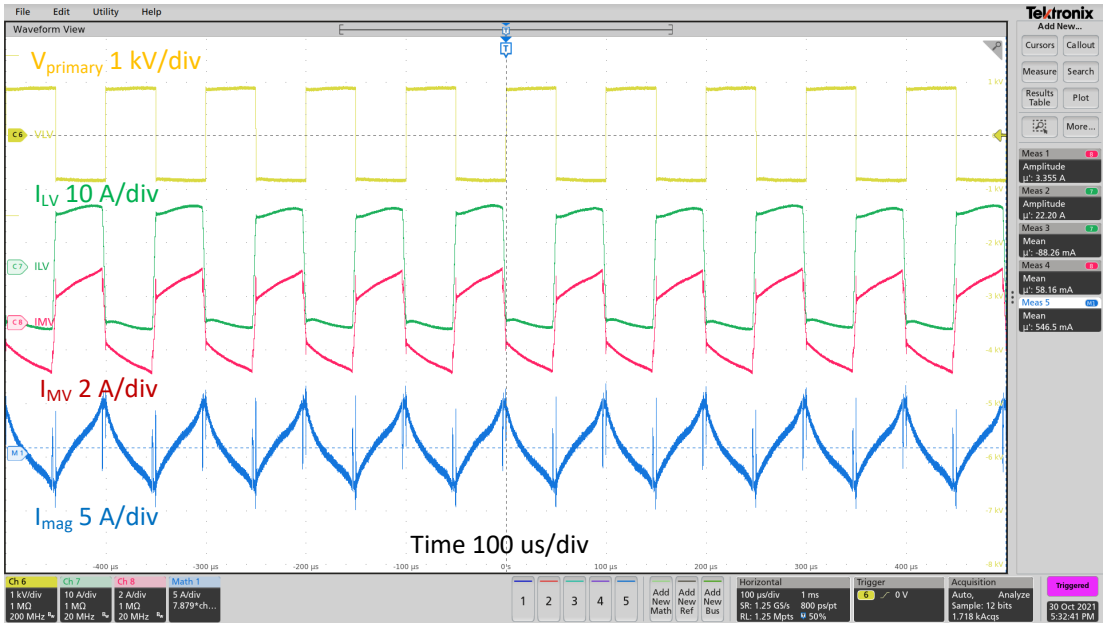


(b)

Fig. 7.13: The current waveform for 850 V/6700 V MV transformer at no-load with (a) balanced flux, (b) unbalanced flux.



(a)



(b)

Fig. 7.14: The current waveform for 850 V/6700 V MV transformer at full-load with (a) balanced flux, (b) unbalanced flux.

7.2.2 Modeling of the Magnetic Gap in Dual-Active-Bridge Converters

In order to avoid high complexities of analysis, a piecewise linear model can be used to model the proposed transformer with magnetic gap without considering the detailed permeability change of the combined transformer core. In order to model the partial transformer saturation, an inductive network has to be adopted to have a variant magnetic inductance. The topology of the model is shown in **Fig. 7.15**.

In the proposed DAB model, virtual DC blocking capacitors are inserted in series with the transformer windings, to avoid DC errors in calculation from the DAB, and paralleled DC source I_b is added to introduce the DC bias current of the magnetizing current. To simplify the analysis, only one side of the transformer has the DC bias. L_{m0} serves as the unsaturated magnetizing inductance, while L_{m1} and L_{m2} are the paralleled inductance to mimic the inductance reduction during saturation. Two stages are used in order to have a smoother transition from the unsaturated state to the saturated state, which will be verified with the curve fitting. Current sources I_{h11},

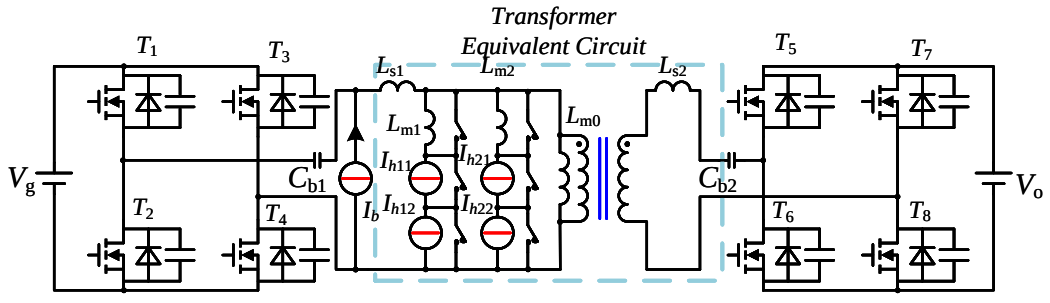
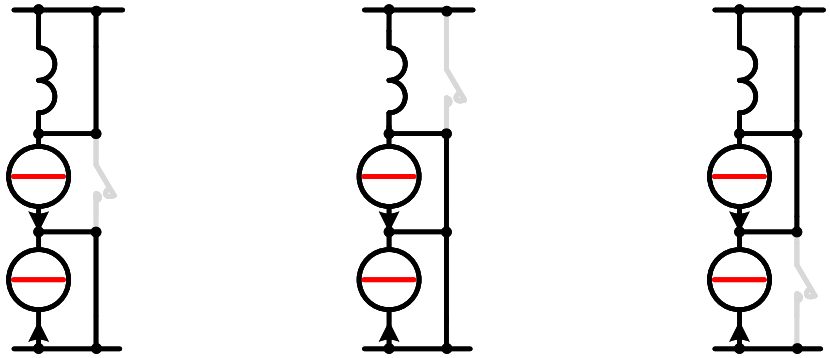


Fig. 7.15: The model of DAB with ferrite gaped transformer.

I_{h12} I_{h21} and I_{h22} with by passing virtual switches are inserted to model the behavior of $B-H$ hysteresis of the saturable ferrite sheets. If the magnetizing inductance of unsaturated core is L_{nonsat}, and ferrite partially saturated L_{pasat}, and ferrite gap fully saturated L_{sat}, the values of L_{m0}, L_{m01} and L_{m2} can be determined as

$$\begin{cases} L_{m0} = L_{unsat} \\ \dfrac{L_{m0}L_{m1}}{L_{m0}+L_{m1}} = L_{pasat} \\ \dfrac{L_{m0}L_{m1}}{L_{m0}L_{m1}+L_{m1}L_{m2}+L_{m0}L_{m2}} = L_{sat} \end{cases} \tag{7.4}$$

In each saturable inductive branches, two current sources are used to act as the hysteresis current of the transformer current on each stage. Whichever switch is open, the corresponding component in parallel with it is switched in the circuit and functions actively. In **Fig. 7.16(a)**, as the switch of the middle current source is open, the circuit is with a current flowing from top to the bottom, which means the saturation of that stage is inactivated, and the transformer went out from saturation with the current polarity from top to the bottom. While for **Fig. 7.16(b)**, the impedance of the branch is reduced to the inductance, which means the saturation of that stage is functioning. Similarly, in **Fig. 7.16(c)**, as the switch of the bottom current source is open, the circuit is with a current flowing from bottom to the top, which means the saturation of that stage is inactivated, and the transformer went out from saturation with the current polarity from bottom to the top.



(a) **(b)** **(c)**

Fig. 7.16: Circuit diagram of different stages: (a) hysteresis current downward (non-saturated), (b) inductor switched-in (saturated), (c) hysteresis current upward (non-saturated).

As only the stead-state flux unbalance is of interest here, state-space method has been used to analyze the non-linear behavior of the magnetic gap in the DAB converter. Due to the complexity of the adopted model, the computation of the state space has been performed in the combined platform of Simulink/MATLAB and PLECS, so that the topology can be easily implemented in Simulink and all the state matrices can be extracted automatically in PLECS. Then, the initial state can be found at the steady state by using the equation of

$$\mathbf{x_0} = \prod_{i=1}^{k} e^{\mathbf{\tilde{A}_i t_i}} \mathbf{x_0} \tag{7.5}$$

Where, $\mathbf{x_0}$ stands for the initial vector of state variables in one switching cycle, and $\tilde{A}_i$ is the state matrix at the subinterval i, as well as t_i the time duration of subinterval

i. The matrix exponential computes the state after one switching interval, in which several intervals modeling both the saturated and non-saturated transformer states, and finally in the end of the switching cycle the state variables should coincide with the initial condition. Then, with particle swarm algorithm, both t_i and $\mathbf{x_0}$ can be found with negligible computation error, with the controlled preset saturation level in each branch.

The method has been verified with open-circuit test of the transformer, and meanwhile the current waveform is also used to curve fit parameters of the model. In **Fig. 7.17**, both test waveform and curve fitted modeling result have been shown. In order to have a high precision, one core with 4 turns winding has been used to enlarge the current for more accurate measurement. With the test result, the non-saturated inductance is 22 mH, and partial transitional saturated 10.46 mH, and ferrite fully

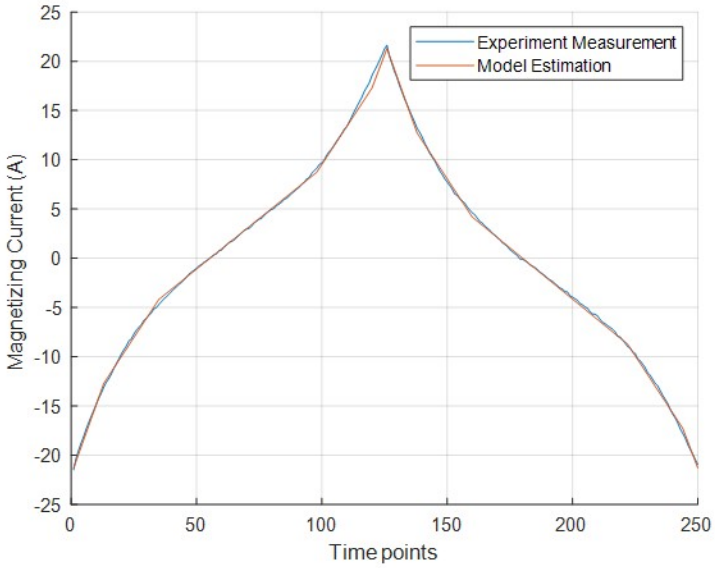


Fig. 7.17: Verification and curve fitting of the magnetic gap transformer.

saturated 5.85 mH. The threshold of saturation on each branch is 0.44 A and 0.98 A respectively, with a hysteresis of 0.12 A. The curve fitting is 2.4%.

With the curve fitted model, the DAB operating waveform can be derived. In **Fig. 7.18**, the DAB transformer winding current waveforms at different load levels have been shown. As the load increases, the phase shift and current level increases clearly. The corresponding magnetizing current waveforms are shown in **Fig. 7.19**, from which as the load level goes up, the waveform peak decreases and the plateau elongated, as during phase shift the magnetizing current is not increased. In **Fig. 7.20**, magnetizing current with different DC bias at no-load condition is depicted, from which the saturation threshold of the transformer core should be kept the same, regardless of the DC bias current. Similarly, in **Fig. 7.21**, the magnetizing current

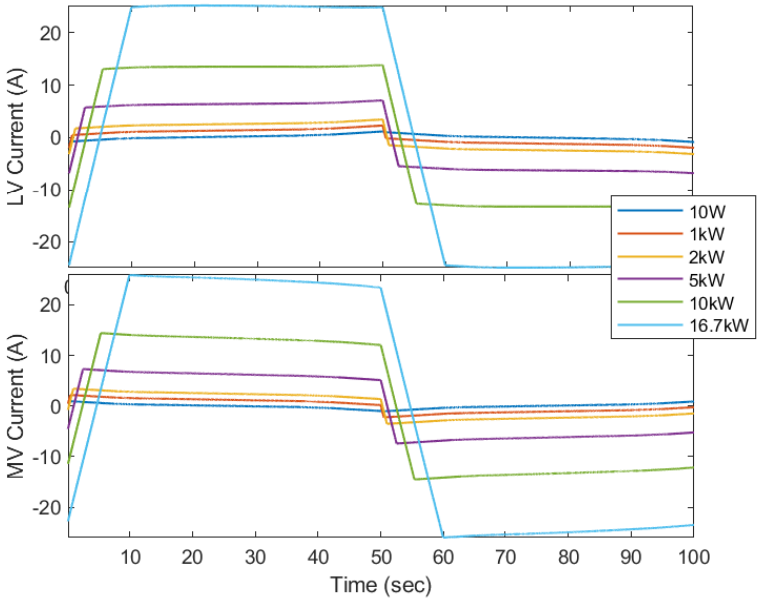


Fig. 7.18: Transformer magnetizing current with different DC bias at no-load.

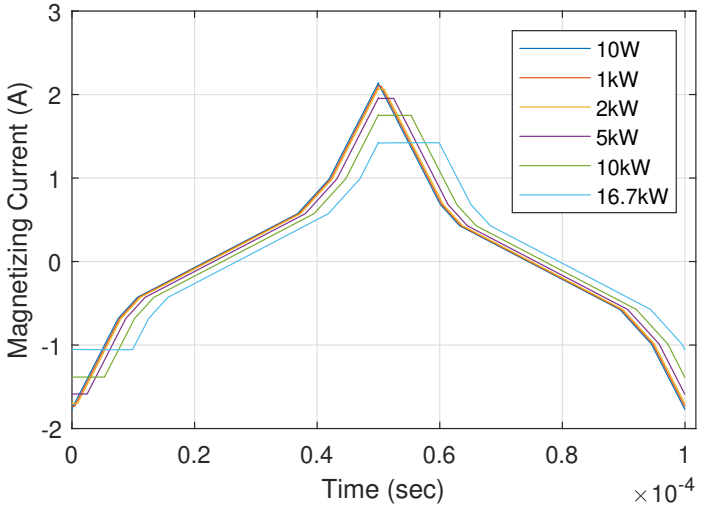


Fig. 7.19: Transformer magnetizing current with different DC bias at full-load.

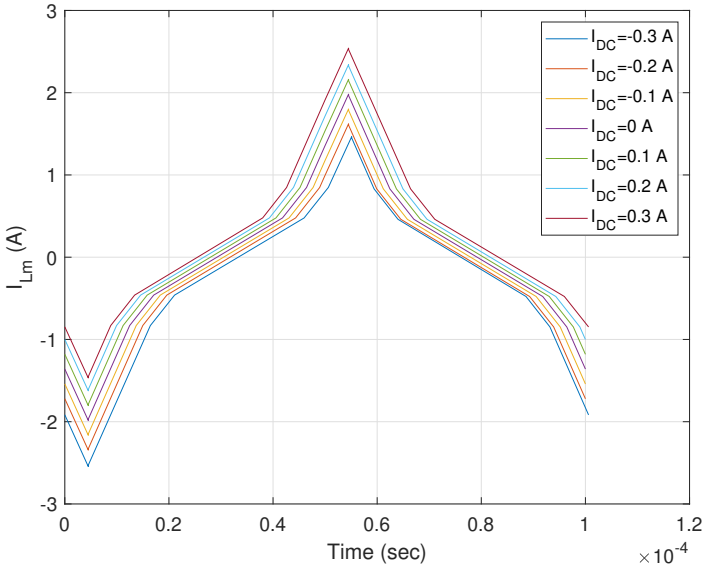


Fig. 7.20: Transformer magnetizing current with different DC bias at no-load.

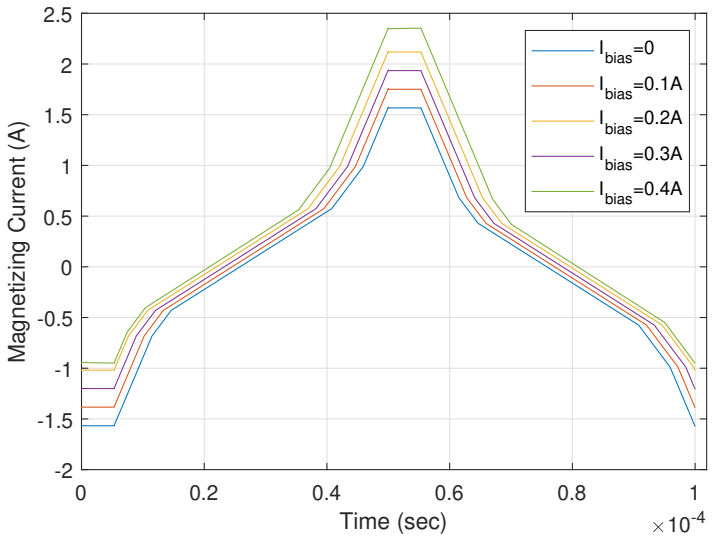


Fig. 7.21: Transformer magnetizing current with different DC bias at full-load.

at full load condition is also depicted. Because of the phase shift of the full load condition is large, the current waveform has a plateau, and the peak value is reduced. In this case, even though the peak value is reduced, partial saturation can still be achieved.

7.2.3 Harmonic Characteristics for Flux Unbalance

As the non-linearity of the transformer core can be added, and the corresponding current waveform can vary as the DC bias changes. The next step is to find the key indicator of the DC biased magnetizing current, and hence the transformer steady-state flux unbalance.

In the normal DAB transformers with no saturable magnetic gap, the magnetizing current should be linear with no significant distortion, assuming that the nonlinearity of the transformer cores are negligible. In this case, the magnetizing current waveform should be triangular or trapezoidal. In this case, the magnetizing current harmonics can be found in closed forms, for triangular waveform:

$$|I_k| = \frac{8I_{pk}}{\pi^2(2n-1)^2} \tag{7.6}$$

where I_{pk} is the peak value of the current, $|I_k|$ the magnitude of the k-th harmonic. And for trapezoidal waveform:

$$|I_k| = \frac{8I_{pk}}{\pi\omega d}\frac{\sin\left[(2n-1)\omega\frac{d}{2}\right]}{(2n-1)^2} \tag{7.7}$$

where I_{pk} is the amplitude of the current, $|I_k|$ the magnitude of the k-th harmonic, ω the fundamental angular frequency, and d the transition half duty cycle.

For the magnetizing current with magnetic gap, it is complex to calculate the closed-form harmonics, but it is possible to have a simple relationship between some specific component and the level of DC bias component. From **Figs. 7.20** and **7.21**, it can be seen that thanks to the ferrite gap distortion, the positive and negative half cycle wave no longer has symmetry along the zero axis, with different DC bias. As the ferrite saturation threshold remains unchanged, the harmonic contents at different DC bias may be different, especially for even-order harmonics. Since in a centrosymmetric waveform the even order harmonics should be zero, for noncentrosymmetric waveforms the even order harmonics are non-zero. Therefore, it is expected that with different DC biases, the even-order harmonics should be different.

Fourier analysis can be performed to derive the relationship between the DC biased magnetizing current and the harmonics. In **Fig. 7.22**, under full load conditions with different DC bias, the 2500-point fast Fourier transformation (FFT) has been

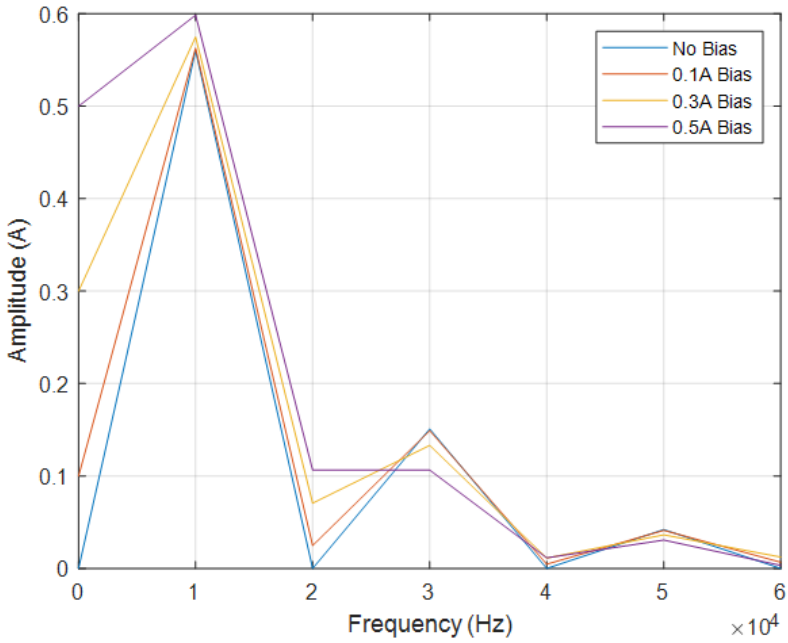


Fig. 7.22: FFT analysis of magnetizing current with DC bias.

calculated, and from the DC to sixth harmonics are depicted. As the DC bias level changes, the harmonic contents change, too. Moreover, From **Fig. 7.22** the components from DC to third order exhibit a relationship with DC bias. However, not all of them can be used as the feedback of the flux balancing. For DC component, it has been mentioned that due to the offset and noise of the sensors, it may be hard to accurately measure 0.5 A DC bias. For the fundamental harmonic, as the power level and phase-shift also change the peak value and plateau of the waveform, the fundamental component may also be affected by the load level. Moreover, the change of the fundamental along DC bias is also relatively small, which may degrade the measurement accuracy, and so is the third order harmonic. For second order harmonic, it can be seen that with no DC bias, the harmonic is zero, while as the DC bias increases, the second order harmonic also increases.

The fundamental and second order harmonics have been studied in more detail at different load conditions and DC bias levels. From **Fig. 7.23** and **Fig. 7.24**, the fundamental harmonic changes with both DC bias and output power, whereas the second-order harmonics only change with DC bias and apparently irrelevant to the power level. The phase angle of the second-order harmonic exhibits independence along the power and DC bias, which can be selected as the indication of the polarity of flux unbalance.

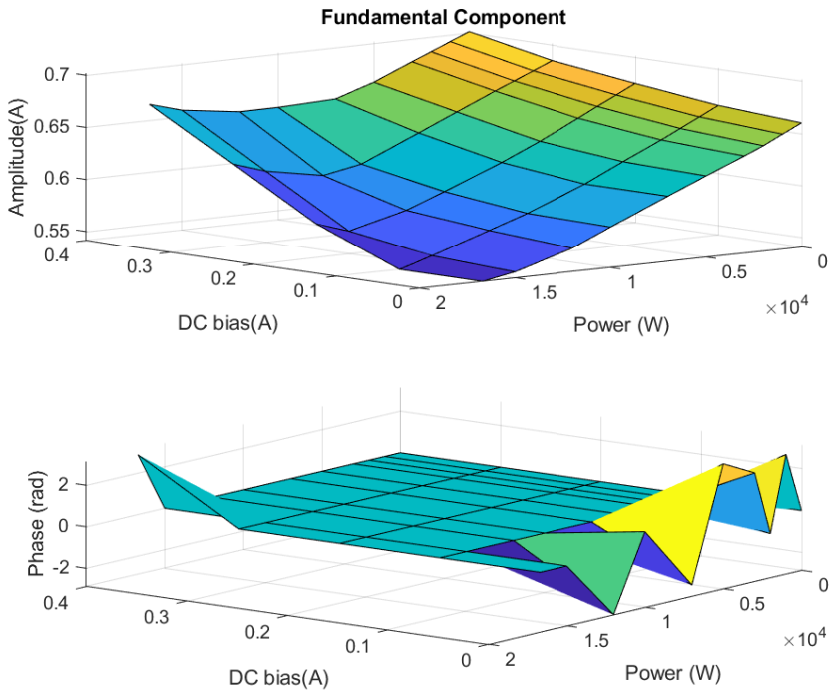


Fig. 7.23: Fundamental harmonic of magnetizing current with different DC bias and power.

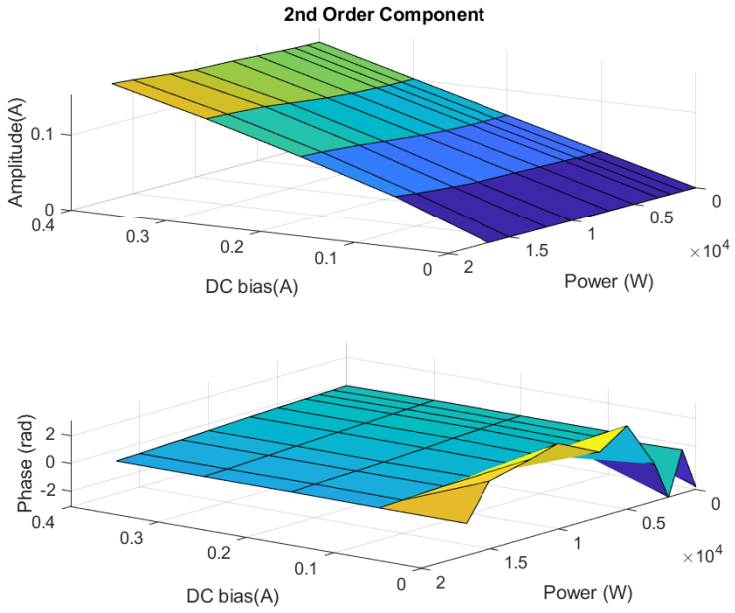


Fig. 7.24: The second-order harmonic component of the magnetizing current at different DC bias and power level [45].

7.3 Flux Sensor Design and Validation

The straightforward way to measure the magnetizing current by sensing the combined winding in [22] seems not feasible, as in different DAB and MFT designs, the turns ratios are not always unity or a simple fractional number. Therefore, the two winding currents have to be measured separately, and summed up through analog or digital circuitry [45].

The proposed scheme of magnetizing current sensor is shown in **Fig. 7.25**. To meet the insulation requirement, the two winding currents are sensed separately, with through hole Hall effect sensors. Then, the two analog signals representing two currents are summed together with same or different preset gain. The gain is tuned

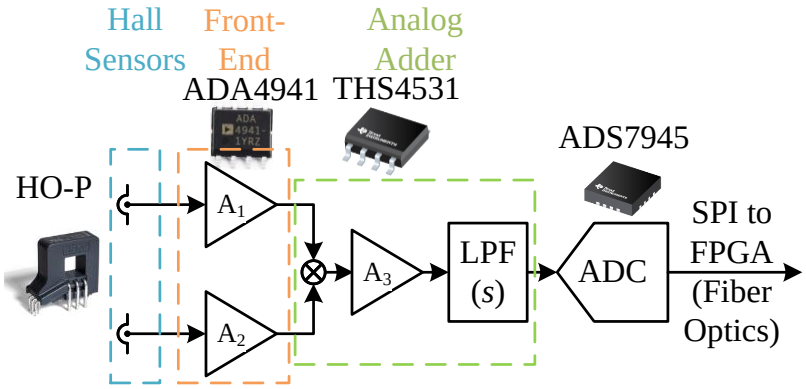


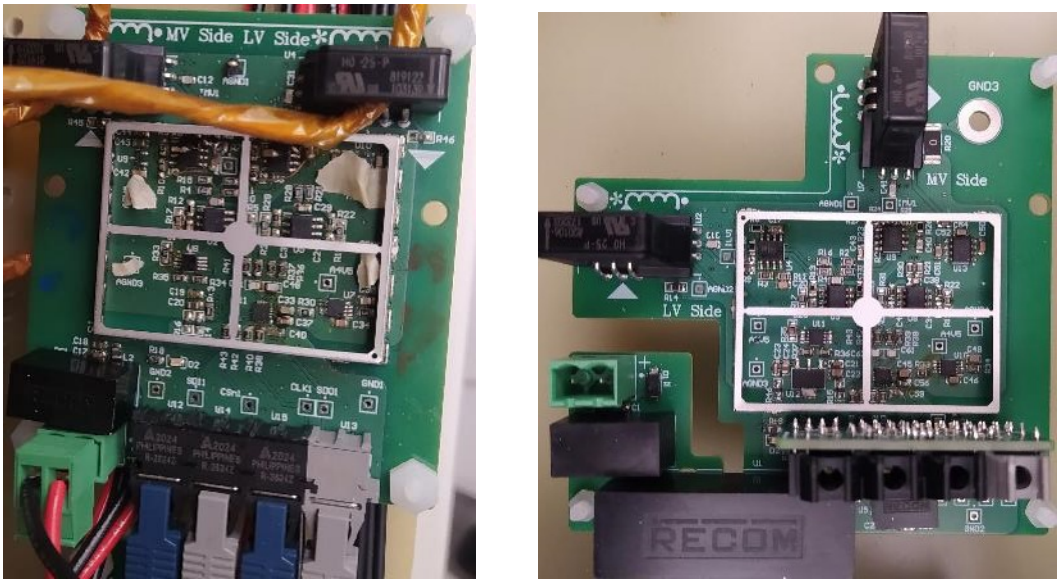
Fig. 7.25: Schematic of the transformer current sensor.

so that the output of the summation circuit should be the magnetizing current, which means the gains of the two scalers should be

$$\frac{A_1}{A_2} \cdot \frac{A_{Hall,1}}{A_{Hall,2}} = \frac{N_1}{N_2} \tag{7.8}$$

where A_1, A_2 are the gains of the scalers, and $A_{Hall,1}$, $A_{Hall,2}$ the Hall sensor gains, N_1, N_2 the winding turns for both sides. It is not necessary for both sides to use the same model sensors, as their ratings may be different. Low-pass filter (LPF) is added along with the analog adder circuit, after which the ADC samples the summed signal several time per switching cycle to extract the second order harmonics.

The designed sensor board for the 850/850 V and 850/6700 V transformers are shown in **Fig. 7.26**. In order to provide insulation for both sides, through hole sensors **HO-P** series are selected to transfer the winding current to the unipolar voltage signal. Fully differential amplifier **ADA4941-1** are used as the scaler and



(a) **(b)**

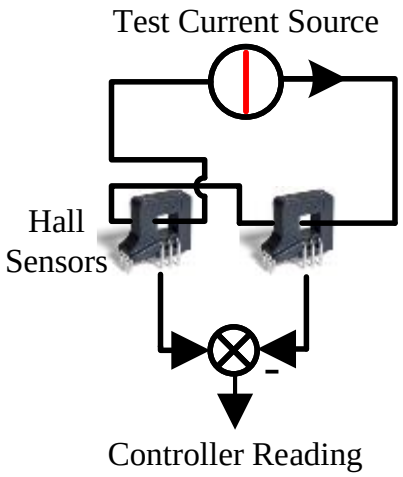
Fig. 7.26: Photographs of MFT magnetizing current sensors: (a) 850/850 V DAB transformers [45], (b) 850/6700 V DAB transformers [46].

front-end converting single-end signal to differential signal, and **THS4531** as the adder op amps, with E192 series chip resistors having a tolerance of 0.1%. The output of the amplifiers typically is designed to have full-scale range of 2.0 p.u. for both sides. The adder amplifier also serves as the ADC driver, as well as the anti-aliasing LPF, to filter the intrinsic white or pink noise of Hall sensor and amplifiers and avoid possible aliasing during FFT calculation.

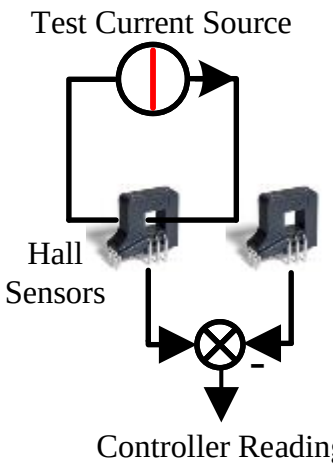
The harmonics exceeding the Nyquist frequency should be attenuated before going into the ADC, or the harmonic component of interest could be at the risk of interference of higher-order harmonics and noise, and then the detection results [45].

The fully differential ADC **ADS7945** is used as the ADC to convert analog signal to digital signal and send out the results to the DC/DC controller through fiber optics. Moreover, the fully differential circuitry can also help attenuate inherent even-order distortions from sensors and amplifiers. As the signal of interest is relatively weak and needs high amplifier gains, a shielding box is added on each board to shield the switching noises from the power stage. For the 850/6700 V sensor, an isolated power supply with insulation capability up to 20 kV DC is used to have a safer insulation.

Table 7.2 lists the sensor design parameters for both 850/850 V and 850/6700 V DAB transformers, demonstrating the configuration of sensor gains. To test the magnetizing current measurement, the schematic of the test setup is illustrated in **Fig. 7.27**. The steady-state test results for both 850/850 V and 850/6700 V sensors are depicted in **Fig. 7.28**, showing that six 850/850 V sensor boards exhibit obvious consistency and linearity, and they did not need any explicit effort for sensor calibration or adjustment, as the initial linearity is all acceptable, although the circuitry may have different DC offsets. For the 850/6700 V sensor, as the turns ratio cannot be simplified to a simple fraction, the LV and MV sides are tested separately, but through the test, the linearity is also high enough. Specifically, due to the lower insulation requirement, the 850/850 V sensor is also tested inside the DAB converter, and from the waveform in **Fig. 7.29**, the magnetizing current can be measured at the input of the ADC.



(a)

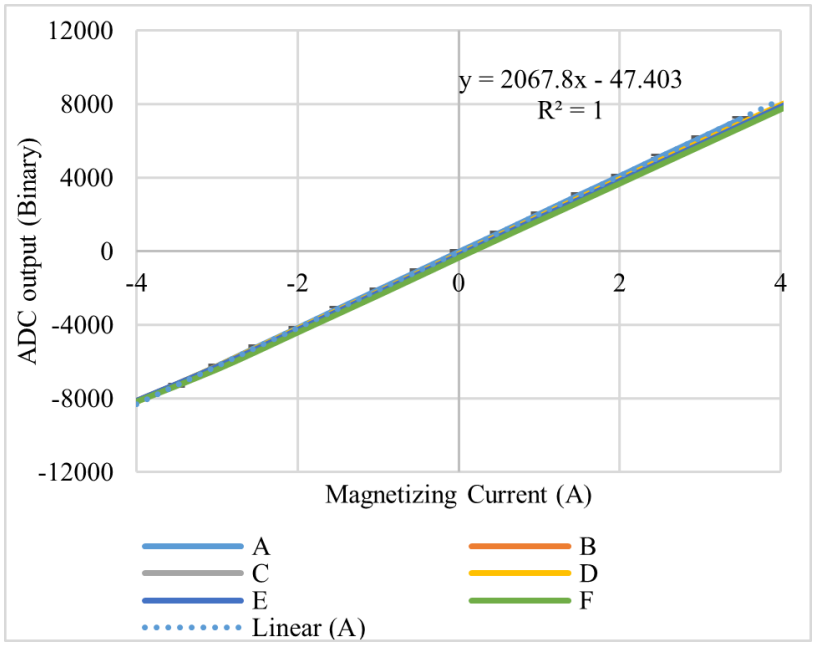


(b)

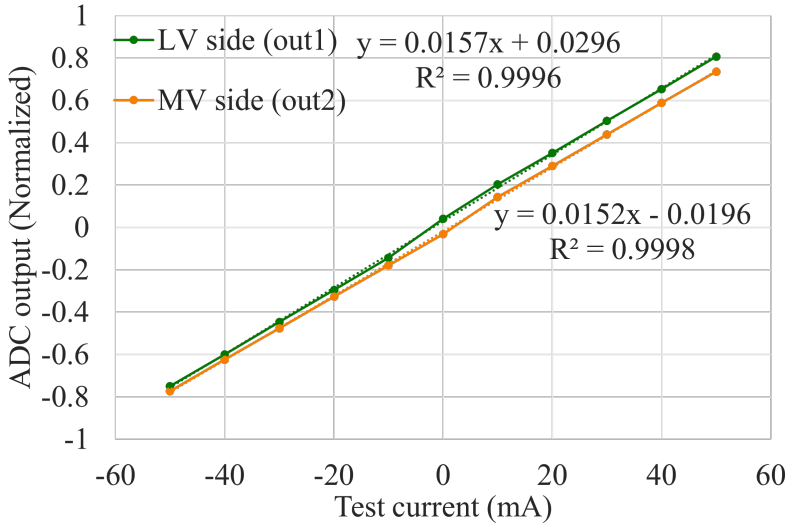
Fig. 7.27: Test set-up for (a) 850/850 V and (b) 850/6700 V sensors.

Table 7.2: Sensor Gain Settings for Unity and Fractional Turns Ratios.

	850/850 V DAB	850/6700 V DAB
Turns Ratio	34:34 (1:1)	33:266 (1:7.879)
Current Rating	19 A/19 A	19 A/2.41 A
Hall Sensors	HO 25-P/HO 25-P	HO 25-P/HO 6-P
Hall Sensors Sensitivities (mV/A)	32/32	32/100
A_1/A_2	3.5/3.5 (2×ADA4941)	3.5/8.765 (2×ADA4941)
A_2/A_1 Ratio with Hall sensitivities	1.0	7.825
A_3	4.975 (THS4531)	4.975 (THS4531)



(a)



(b)

Fig. 7.28: Test results for (a) 850/850 V and (b) 850/6700 V sensors.

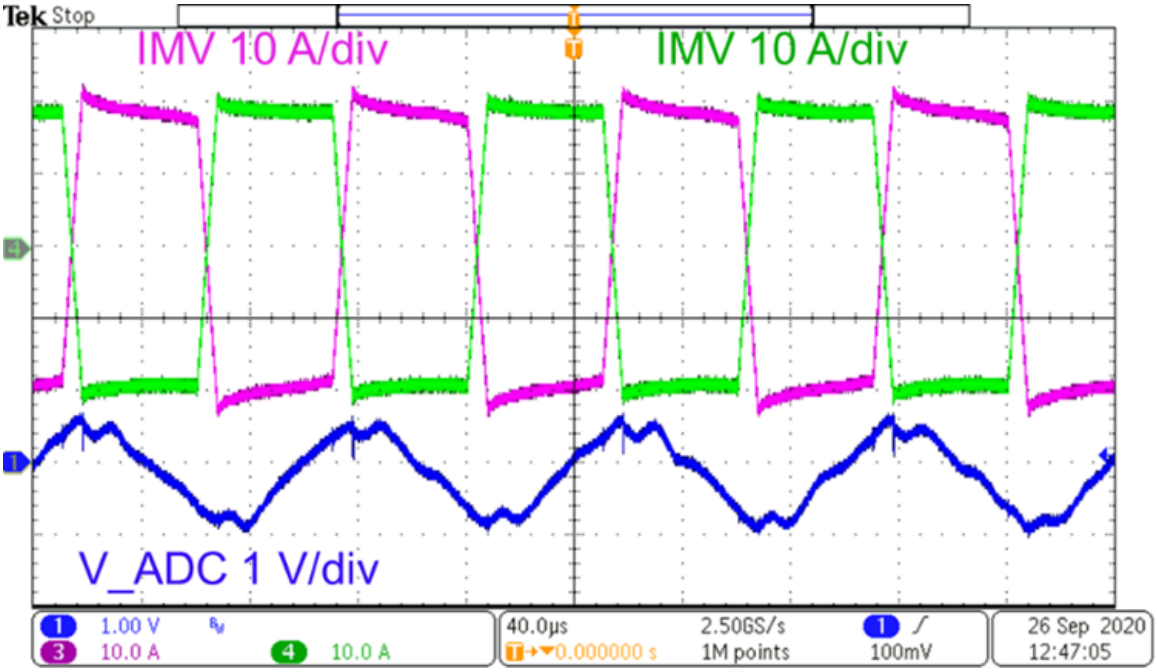


Fig. 7.29: 850 V/850 V sensor tested in DAB.

7.4 Flux Balancing Scheme and Test

7.4.1 Steady-state Flux balancing control

As the detection scheme being proposed, analyzed, and verified, the corresponding controller can be designed to control both the power conversion of the DAB and also the DC flux of the transformer. The diagram showing both DAB controller and flux balancing scheme is depicted in **Fig. 7.30**. From the control diagram, the DC-link voltage of the output side is sampled, and then a notch filter in the digital controller is used to filter out the second order power harmonic induced by the downstream

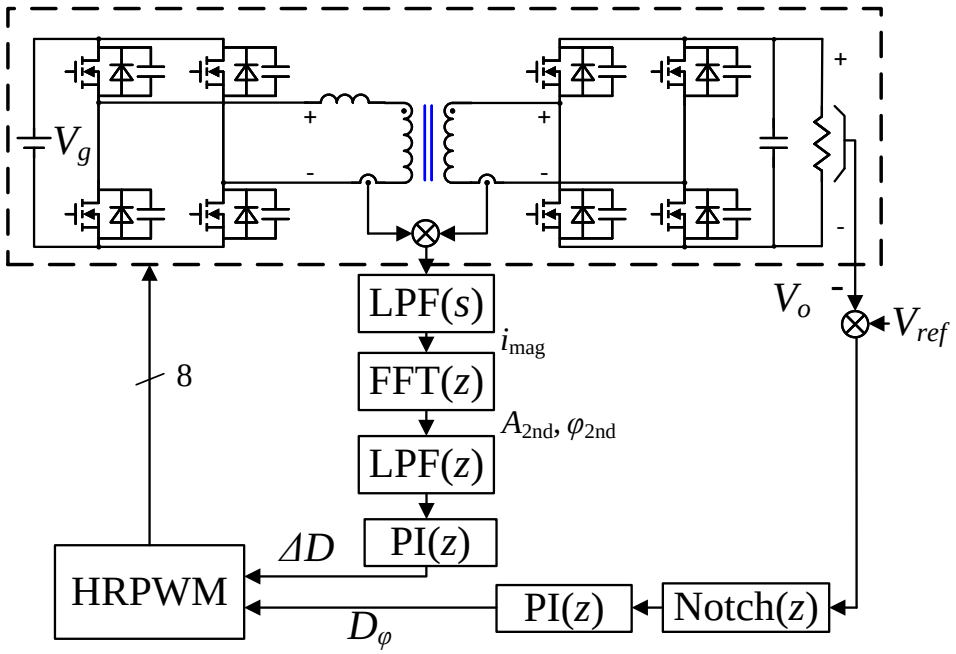


Fig. 7.30: The control diagram of a DAB converter with flux balancing strategy [46].

single-phase DC/AC converter. The output voltage is controlled by the PI controller, and then the phase shift reference D is transferred into the pulse-width modulation (PWM) generator.

Similar to the voltage loop, in the DAB converter, the transformer winding currents are measured by the transformer sensor designed in **Chapter 3**, and then the magnetizing current is derived on the sensor board, after which the magnetizing current is sampled and communicated to the controller board (**Fig. 7.31**) through

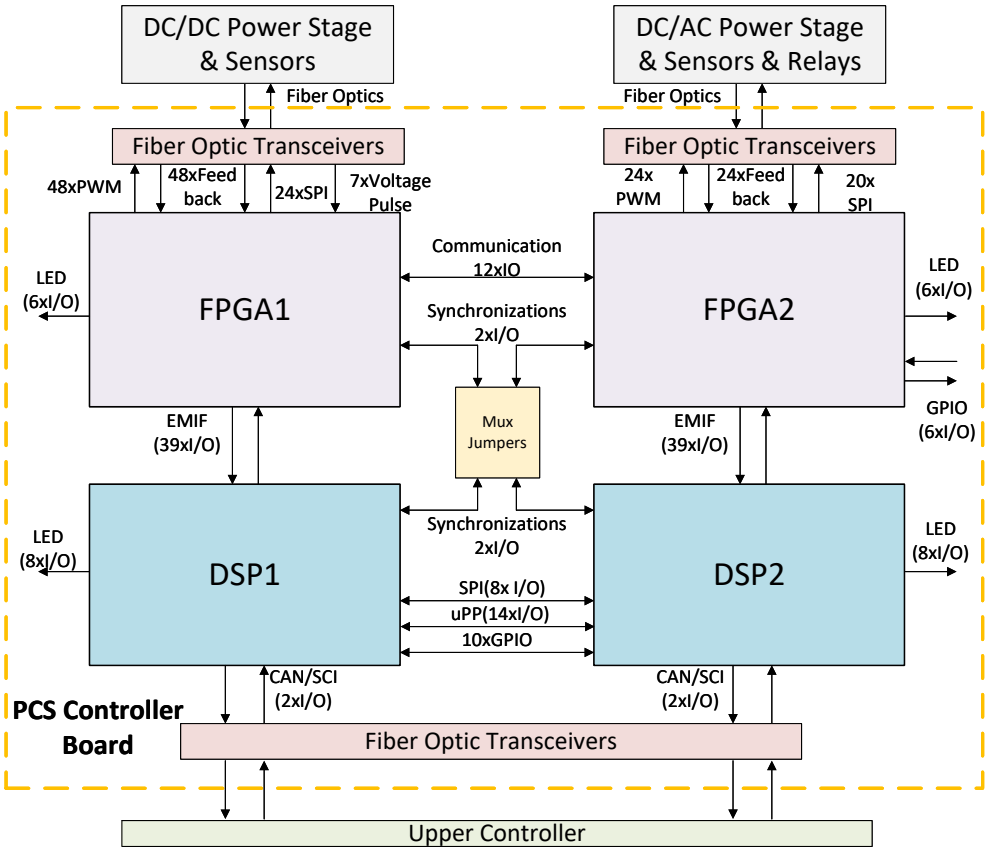


Fig. 7.31: The diagram of the controller board used in test.

the fiber optics and SPI protocol. The controller DC/DC side FPGA serves as the communication master, and actively controlling the sampling speed and start/stop of the data conversion. The DSP on the controller board gets the data from FPGA and finally the FFT algorithm and control loops are implemented in the DSP, while the resultant modulation parameters are sent out back to FPGA, a high-resolution modulator in FPGA generates the gate signals controlling the switches through fiber optics.

The sampling frequency of the transformer sensor is of importance, as using a high sampling rate leads to a high cost on board and communication design, while a too low rate may result in poor precision and unstable control response. Since the sampling rate of the flux balancing scheme has to be several times higher than switching frequency, a reasonable sampling rate is needed. To find the sampling rate for the flux balancing control, some calculation has been performed as shown in **Fig. 7.32**. From the result, the window size mainly limits the resolution of the frequency, while the sampling point in each switching cycle governs the accuracy on each harmonic component. Since the only the second order harmonic is needed, 8-point FFT with single cycle per sampling winding can be used. As the switching frequency is 10 kHz, the sampling rate is then 80 kHz, and Nyquist frequency 40 kHz. Although the steady-state flux density can be balanced with the feedback control loop, it is still necessary to implement the transient flux balancing, by implementing the intermediate duty cycle update scheme, which is mentioned in **Chapter 2**. As high noise from the Hall sensors has been found, digital filters have to be used in

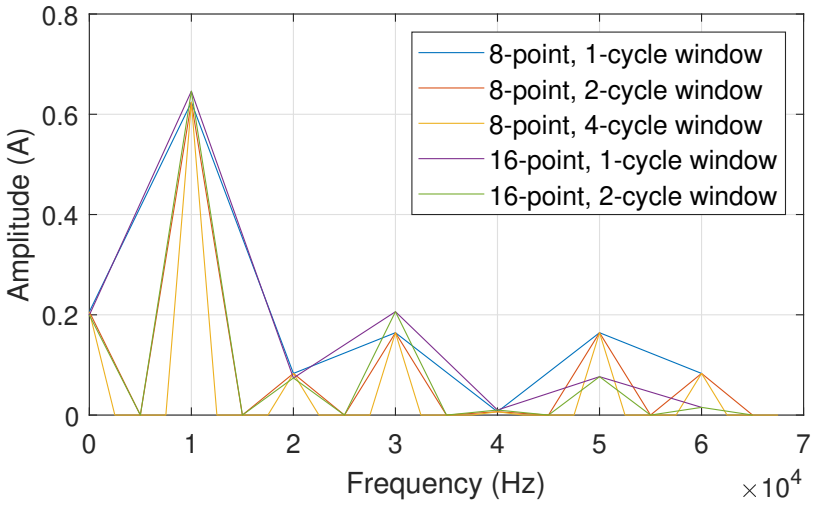


Fig. 7.32: The sampling rate evaluation.

the digital controller, after the FFT calculation has been conducted. The signal processing considering noise and polarity of flux unbalance is illustrated in **Fig. 7.33**.

Flux Balancing Modulation

Since the transformer voltage is as high as 850 V and 6700 V, and the DC impedance of the transformer can be as low as tens of milliOhms, the resolution of PWM is also important. As has been discussed in **Section 7.2**, the DC offset unbalance and compensation can be injected independently on one side. The duty-cycle compensation ΔD can be added on either low voltage side, or the high voltage side. In the converters discussed, the compensation is solely added on the duty-cycle of secondary side, or the medium voltage side, as has been found that the medium voltage SiC device has more deviation. The duty cycle compensation is shown in **Fig. 7.34**.

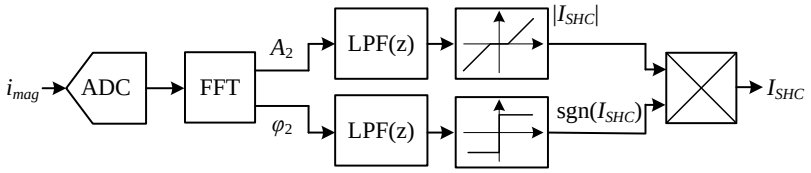


Fig. 7.33: The diagram of the second order harmonic signal processing.

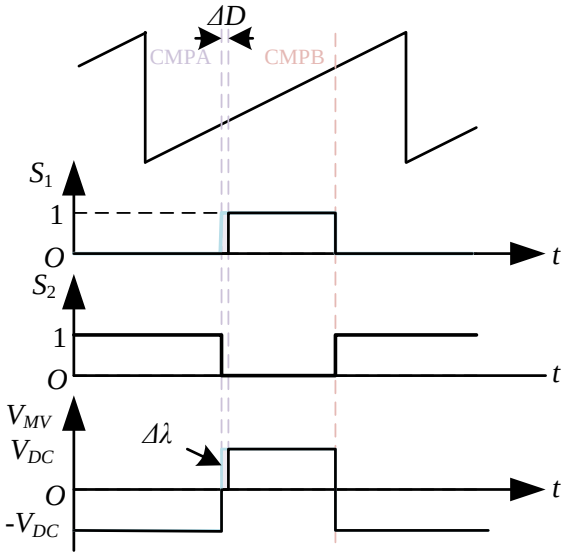


Fig. 7.34: The diagram of duty-cycle compensation.

For each step of the duty cycle change, the volt-second change can be

$$\Delta\lambda = V_{DC} \cdot \Delta t_{PWM} \tag{7.9}$$

where $\Delta\lambda$ is the change of volt-second product, V_{DC} the DC-link voltage on the compensated side, and Δt_{PWM} the step change of 1-bit in PWM modulator. In **Fig. 7.35**, a high resolution PWM modulator is implemented in the FPGA. By utilizing both the rising and falling edge of the system clock, and therefore, the resolution of the PWM output is half of the clock period. In the controller for the converters under test, the modulation carrier frequency is 10 kHz, with a step resolution of 2.5 ns, while the digital clock frequency is set to 200 MHz.

7.4.2 Test Verification

With the measurement, control, and modulation schemes aforementioned, the complete scheme has been verified in both 850/850 V and 850/6700 V DAB converters.

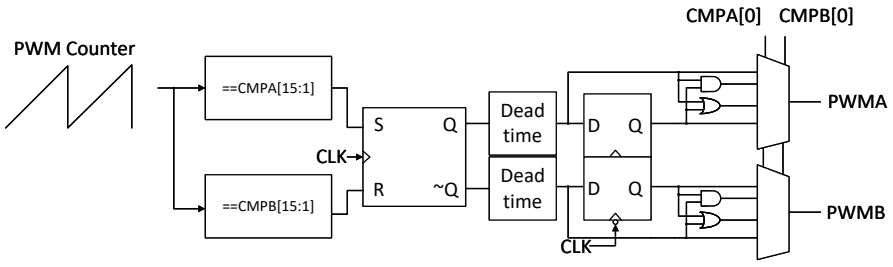
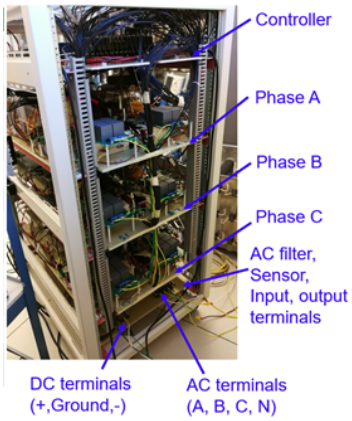


Fig. 7.35: The diagram of the high resolution PWM modulator realized in FPGA.

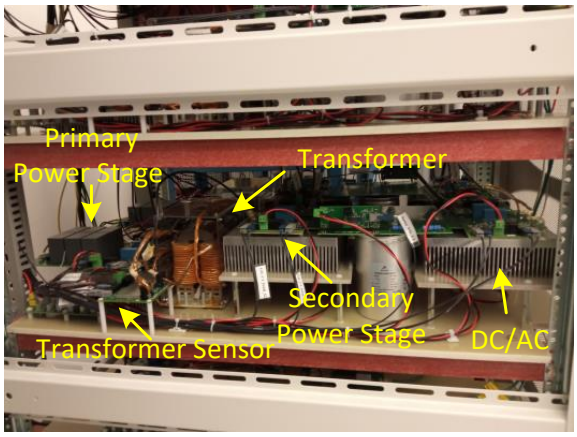
Test on 850/850 V DAB converters

Firstly, the flux balancing test is carried out in one 850/850 V DAB unit. The photographs of 850/850 V converter under test is shown in **Fig. 7.36**. In **Fig. 7.36(c)**, two secondary DC-link are connected together, so that power can be circulated between the two DAB converters, and the output power can be adjusted for the converter under test.

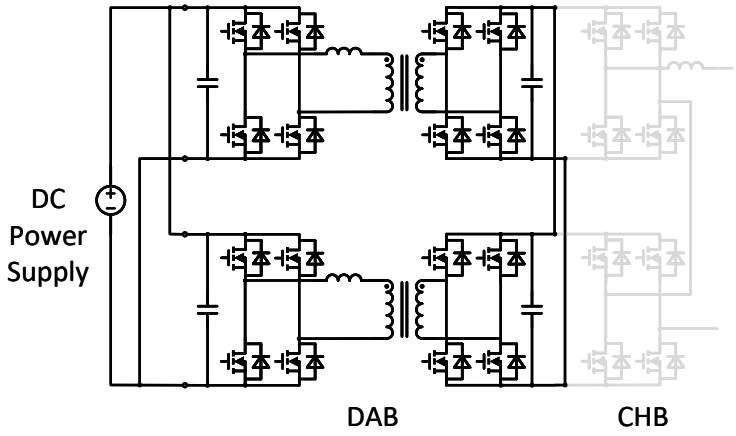
The magnetizing current of the 1:1 transformer can be easily extracted, with a through-hole current probe clamping both single-turn wires from the primary and secondary windings. The test waveforms are in **Fig. 7.37**. In **Fig. 7.37(a)**, the DC component of the magnetizing current drops from 0.35 A to -0.05 A after the transient, and in **Fig. 7.37(b)**, it can be seen that the magnetizing current after balanced is symmetric about the zero axis, with the proposed partial saturation. Having verified the flux balancing in one unit, a test has also been performed with six DAB units that forming a power conditioning system (PCS) with cascaded H-bridge converters. The results are shown in **Fig. 7.38** measuring two of them. At first, the flux in six DAB transformers were controlled with the proposed scheme, and then the flux balancing control were disabled. The magnetizing currents are shifted due to the converter mismatch when the flux control was bypassed, as can be observed from the overall current waveforms. The discrepancy of symmetry between magnetizing and winding currents can also be seen in the zoomed-in waveforms.



(a)

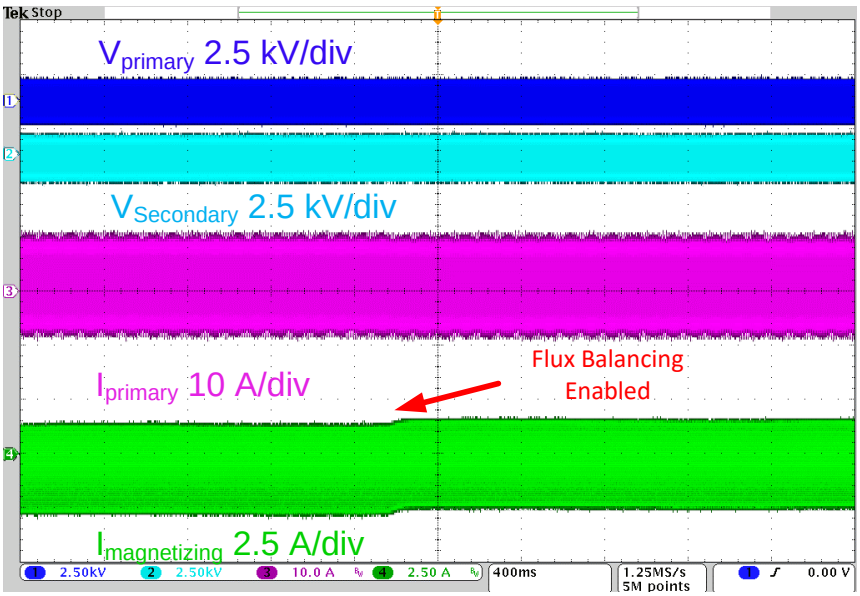


(b)

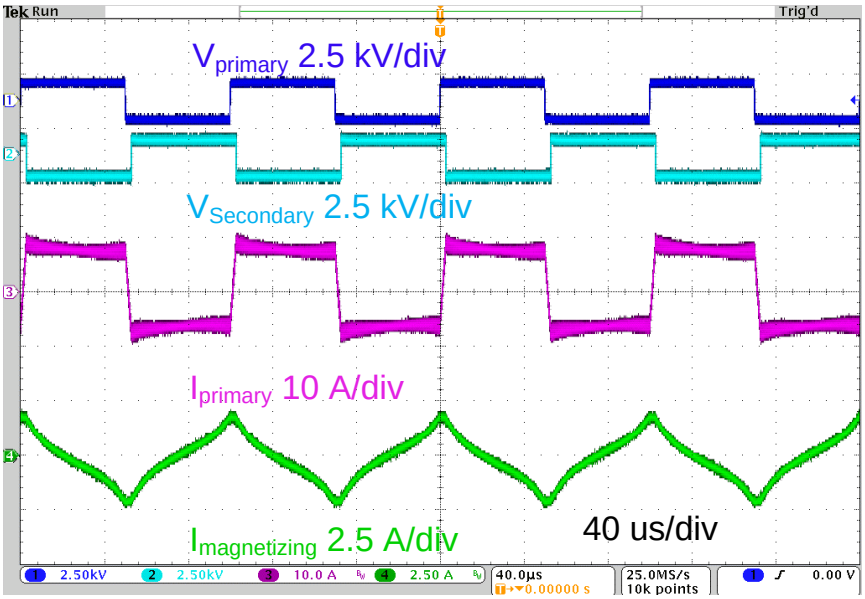


(c)

Fig. 7.36: Photographs of 850/850 V (a) PCS cabinet (b) PCS unit, and (c) test schematic for an 850/850 V DAB unit.



(a)



(b)

Fig. 7.37: Test results for 850/850 V DAB (a) during transient, (b) after flux balanced [45].

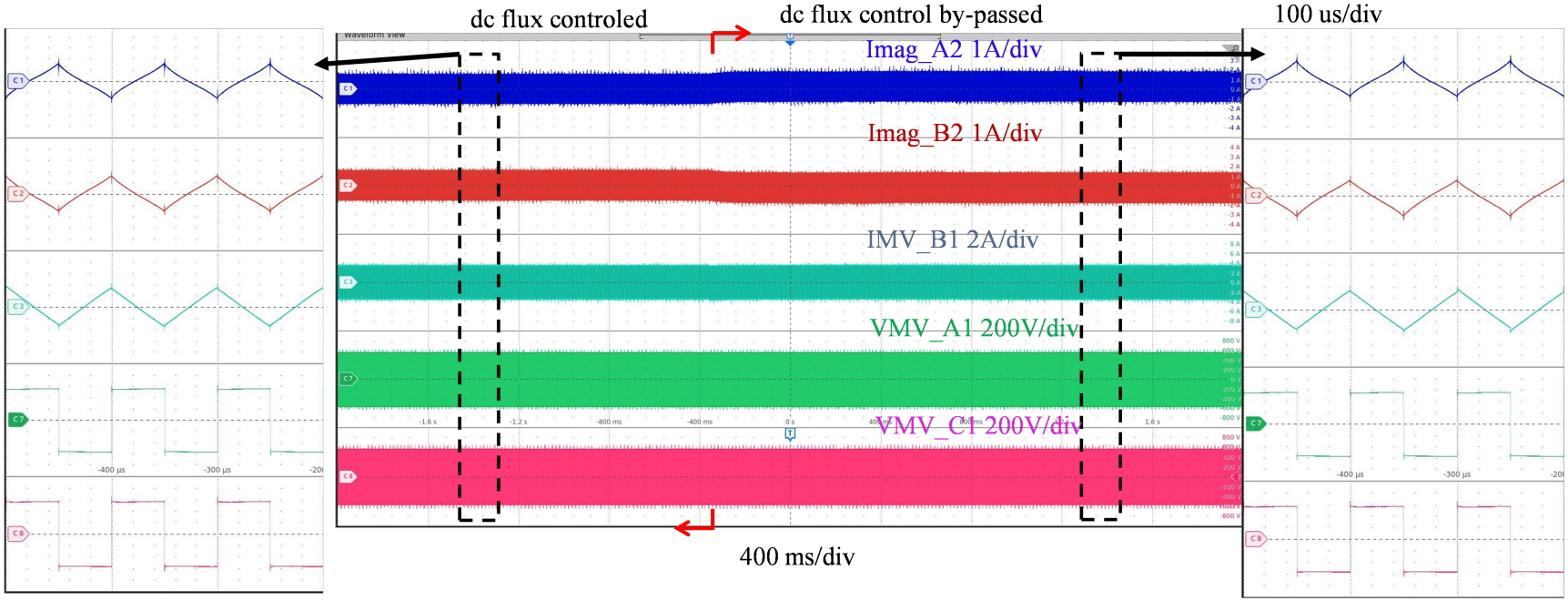


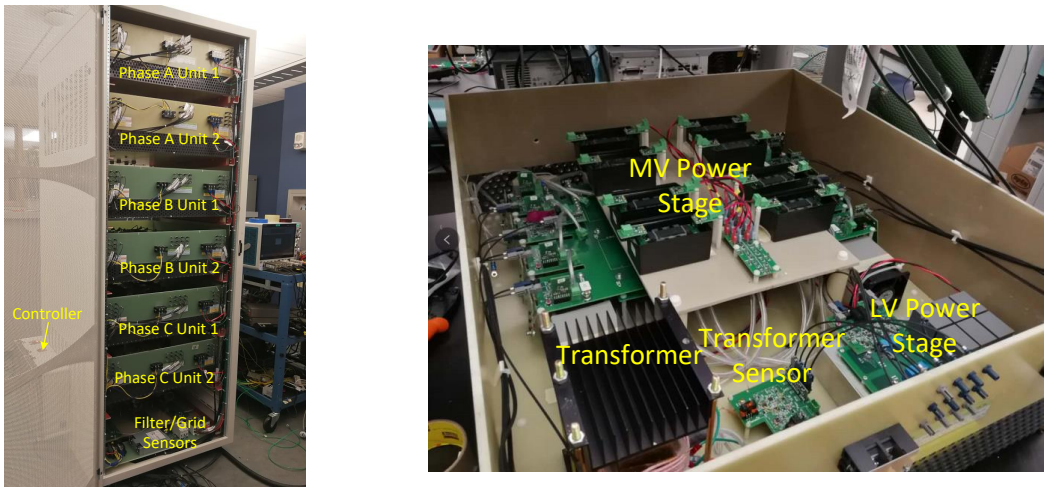
Fig. 7.38: The test waveforms in an 850/850 V PCS [45].

Test on 850/6700 V DAB converters

Test has also been performed in 850/6700 V DAB converter. The photographs of 850/6700 V converter under test is shown in **Fig. 7.39**. In **Fig. 7.40**, two secondary DC-link are connected together by turning the MV devices on CHB side on, so that power can be circulated between the two DAB converters, and the output power can be adjusted for the converter under test.

For MV DAB converter, the flux balancing detection and control are operating during the test. With some injected volt-second unbalance on MV side, a disturbance can be injected into the magnetizing current, so that the stability of the flux balancing method can be tested.

From **Fig. 7.41**, when the volt-second unbalance of 1.5% injected at the no-load condition, an evident current offset step-up can be found on the magnetizing



(a) **(b)**

Fig. 7.39: Photographs of 850/6700 V (a) PCS cabinet (b) PCS unit.

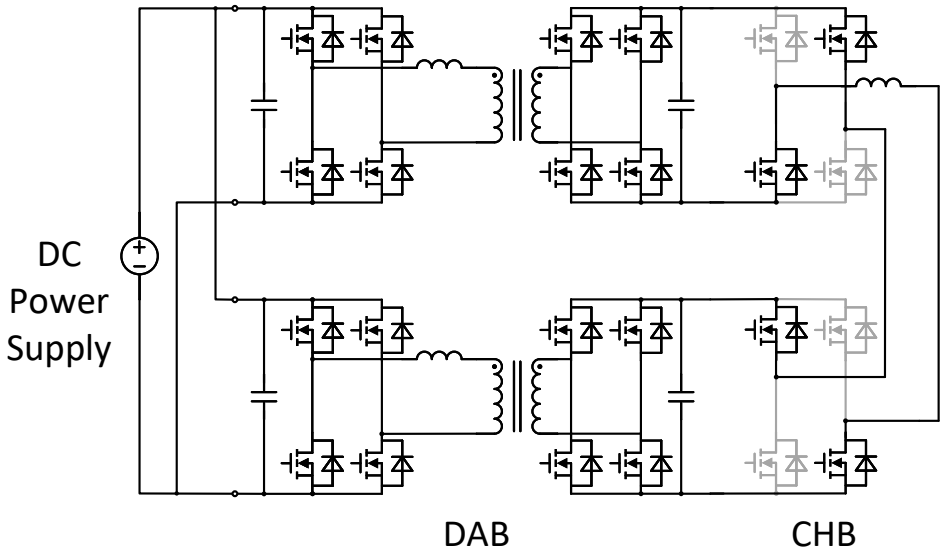


Fig. 7.40: The test schematic for an 6700/850 V DAB unit.



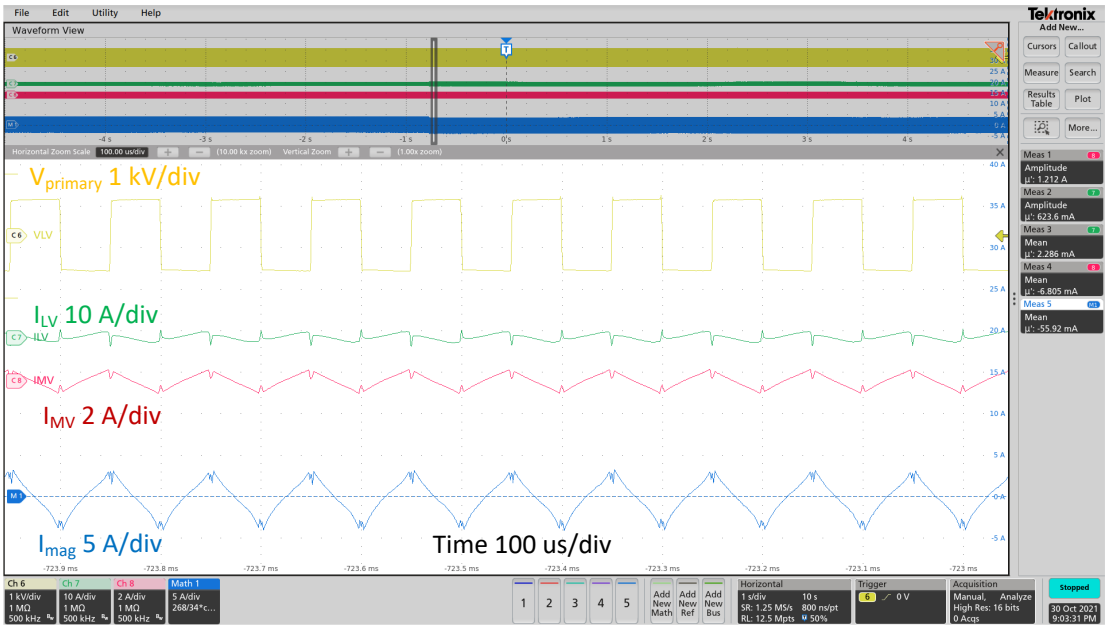
Fig. 7.41: Waveform for 850/6700 V DAB at no-load condition during disturbance injection.

current, and after around 1.02 s, the envelope of the magnetizing current resumed to the value before the disturbance is added. Unipolar distortion can be found in the magnetizing currents in **Fig. 7.42** (a), the DC bias in the magnetizing current is approximately -1.3 A (reflected on LV side). After the flux balanced again, in **Fig. 7.42(b)**, the magnetizing current is more symmetric with control compensation, and the DC component is negligible.

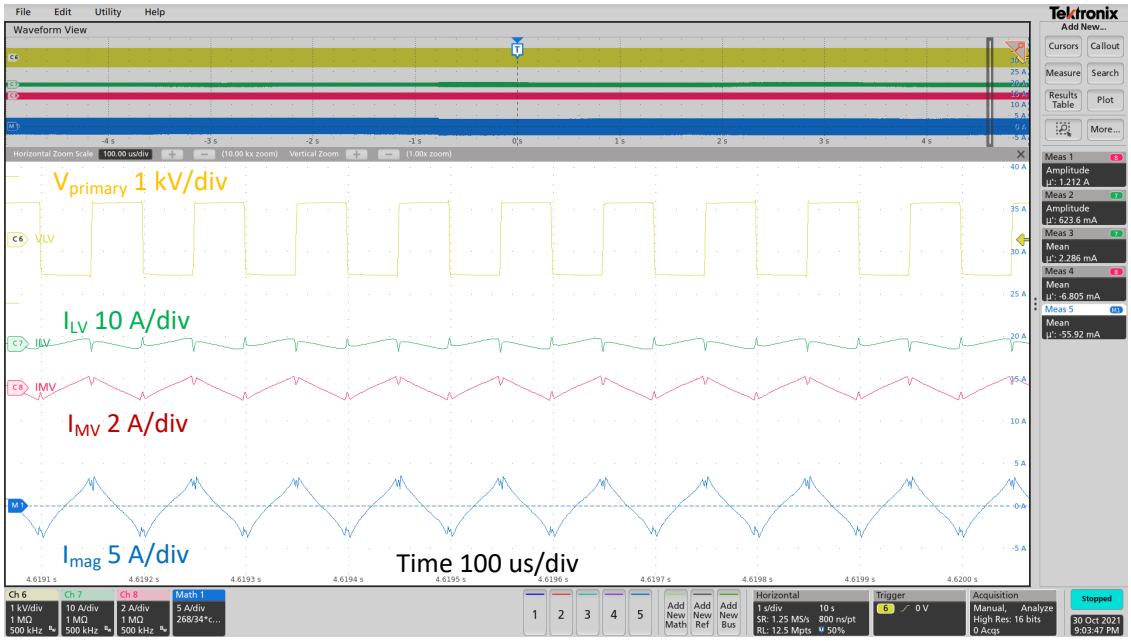
From **Fig. 7.43**, at full-load condition, when the volt-second unbalance of 1% injected, a current offset step-up can be found on the magnetizing current, too, and it took around 0.9 s for the envelope of the magnetizing current to resume the state before the disturbance was injected. The distortion can be found in the magnetizing currents in **Fig. 7.44(a)**, the DC bias in the magnetizing current is approximately 2 A. After the flux balanced by the control, in **Fig. 7.44(b)**, the magnetizing current can be balanced, and the DC component is also negligible.

To verify the stability during the load or control transient, a test has been conducted during the load transient from full-load to no-load, shown in **Fig. 7.45**. After the full-load from the DAB serving as the load, current transition can be found on transformer winding currents, as well as the magnetizing current. The load transition is set after 5 ms, and after 80 ms, the oscillation faded away, while the DC component of the magnetizing current remains unchanged, which can be more clearly seen in the zoomed-in waveforms in **Fig. 7.45(b)**.

From the tests on 850/850 V and 850/6700 V DAB converters, the proposed flux balancing control can be verified. For DAB converters with different voltage



(a)



(b)

Fig. 7.42: Zoomed-in waveform for 850/6700 V DAB at no-load condition (a) zoomed-in when flux unbalanced (b) zoomed-in when balance resumed [46].

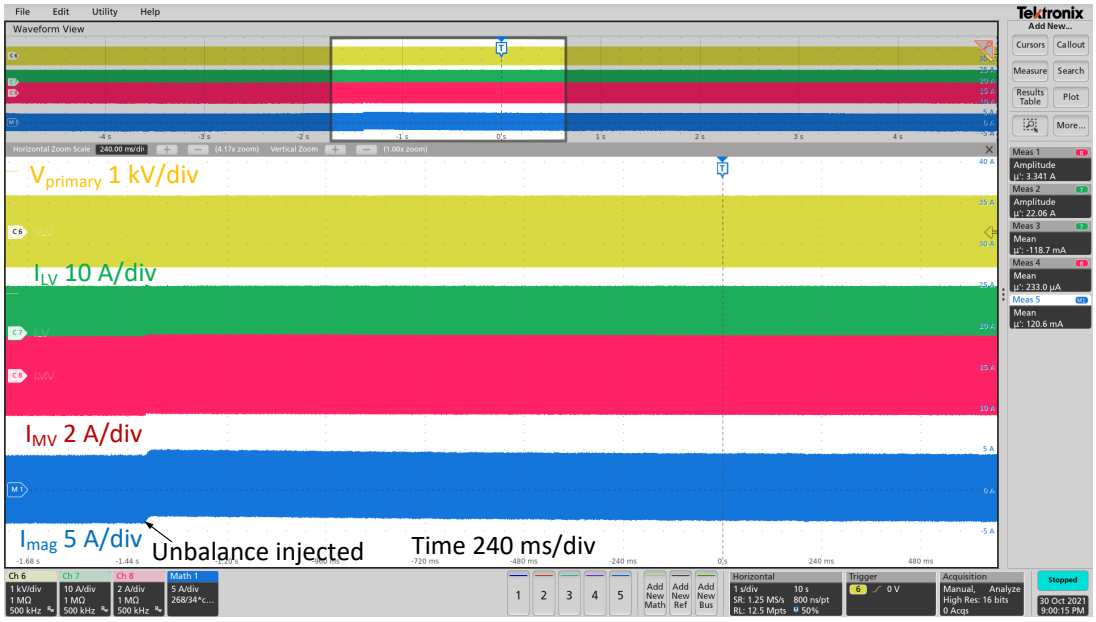
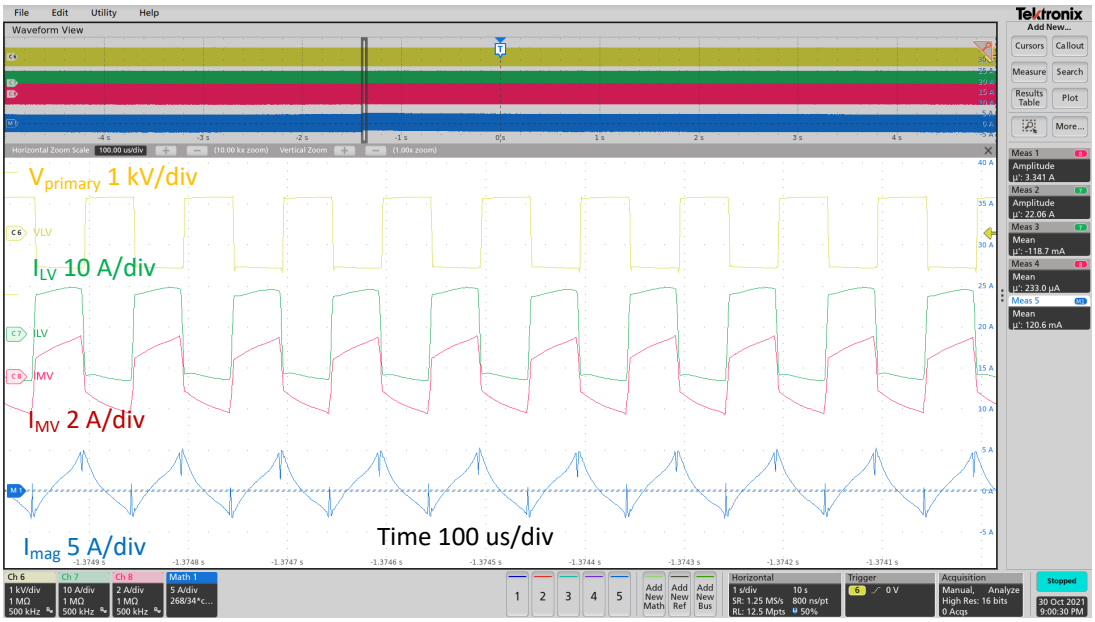
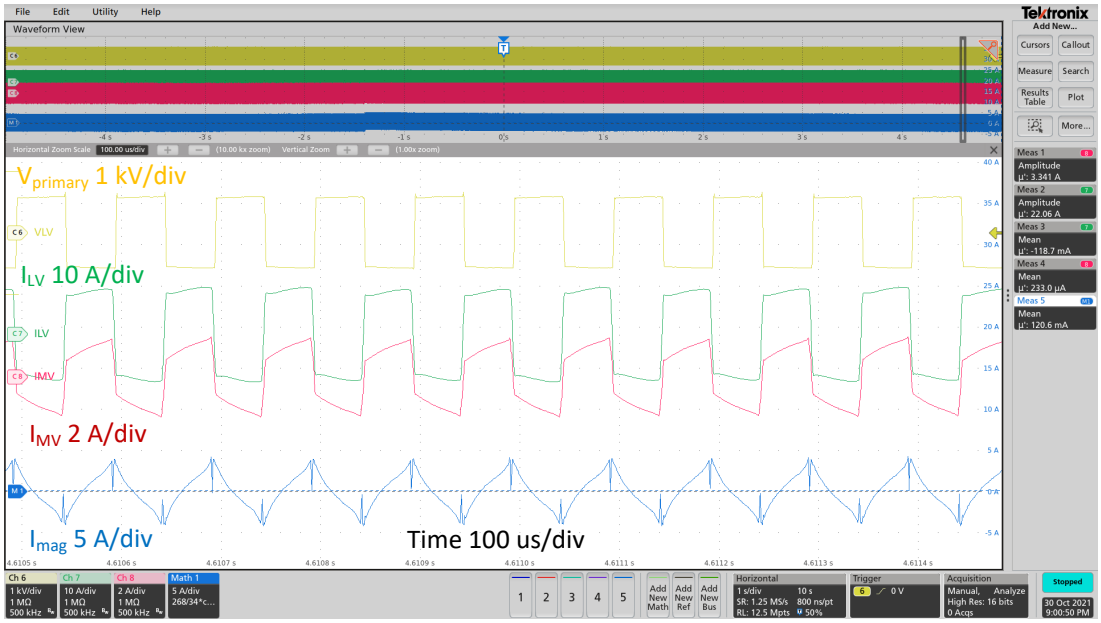


Fig. 7.43: Waveform for 850/6700 V DAB at full-load condition during disturbance injection.

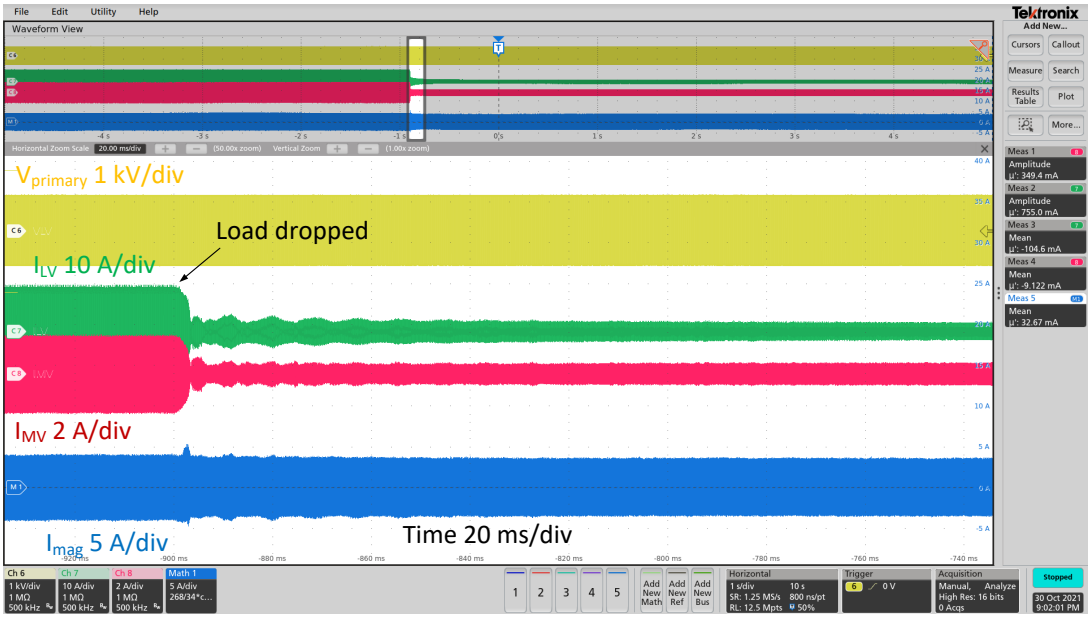


(a)

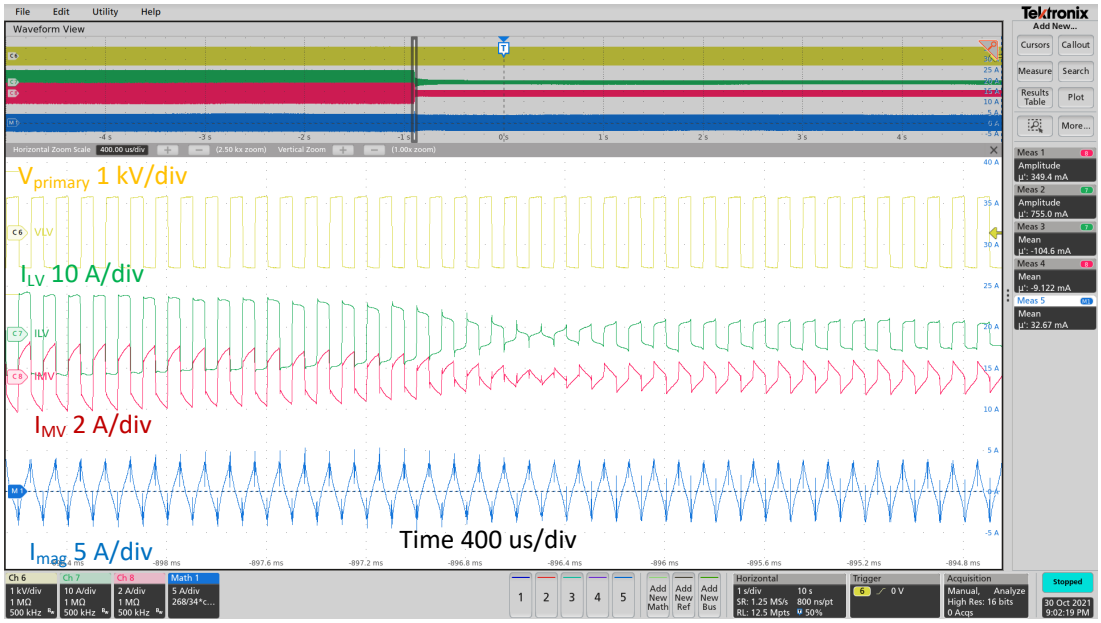


(b)

Fig. 7.44: Zoomed-in waveform for 850/6700 V DAB at full-load condition (a) zoomed-in when flux unbalanced (b) when balance resumed.



(a)



(b)

Fig. 7.45: Test results for 850/6700 V DAB during load transition (a) waveforms during the whole transition, (b) zoomed-in waveforms.

ratings and gains, the flux can be balanced with the proposed feedback control method. For both steady-state and transient disturbances, the proposed balancing scheme can maintain the balanced and symmetrical magnetizing current and core flux. The method can also be immune to fast load changes, which is verified in the load transition test. The control response seems to be in hundreds of milliseconds level, which is due to conservative parameter setting in flux balancing controller. The steady-state flux unbalance and deviation usually change slowly thanks to the high magnetizing impedance, so the steady-state flux balancing is acceptable to be slower compared to the other control loops.

7.5 Summary

In this chapter, a harmonic-based medium voltage transformer flux balancing scheme, considering both the sensing and control, has been introduced and validated through analyses and tests.

- First, the sensing and control methods available in literature have been reviewed. The flux unbalance in a DAB converter can be roughly estimated, based on the characteristic of the devices, and the signal transportation delay deviations. The flux unbalance can be measured by sensing the transformer currents, magnetic core flux, magnetostriction vibration, or the volt-second product of the H-bridges. The flux balancing control can be categorized into three ways, i.e., relying on passive components or ZVS transitions, feedback

control loops, and the modulation compensation on load/control transitions. However, due to high operation voltage and high density/efficiency requirement, the methods for medium voltage DAB have to be capable for high voltage insulation, noise immune, and simple implementation.

- Then, the non-linearity and magnetic gaps of the transformer core has been introduced. Thanks to the earlier saturation of the ferrite sheets than the amorphous/nanocrystalline, nonlinear magnetic inductance can be achieved with ferrite-gaped transformers. With inserted ferrite gaps, the mathematical link between second-order harmonic current and steady-state unbalance has been analyzed. The proposed sensing circuits are then introduced, with good linearity and no DC offset calibration needed.

- Moreover, the sampling consideration and balancing control strategies have been discussed in **Section 7.4**. DAB Converters rated at 850/850 V as well as 850/6700 V have been tested to validate the proposed measurement and control strategy. According to the discussion and experimental validation, the proposed flux detection and balancing strategy based on current harmonic are feasible with both unity and fractional transformer turns ratios, and for DAB converters rated up to medium voltage range.

Chapter 8

Conclusions and Future Work

8.1 Summary and Conclusion

In this dissertation, several technologies addressing issues on magnetic leakage losses, CM noise induced switching losses, and power stage insulation designs for MV DC/DC converters. The conclusion and contributions are as follows:

- A low-loss leakage integration technique has been proposed. The leakage inductance in transformers can be categorized into two terms, namely the intrinsic and external inductances. The high level methodology is to minimize the intrinsic leakage field and maximize the ratio of external leakage structure. Hence, the low-loss leakage integration with ferrite bridge is introduced for shell-type transformer structures. Furthermore, a 2-D lamination configuration for ribbon and sheet-based magnetic core is proposed, which can further reduce the leakage induced eddy current loss. Based on the proposed methods, a MV DAB

transformer has been implemented, and the leakage induced eddy current loss can be suppressed by 68.7%, validating the proposed methodology to integrate leakage with lower loss.

- Then, a new ferrite shielding strategy is also introduced to reduce eddy current loss for inductors and transformers using metal-based cores. The ferrite shielding plates are placed on the critical core surface, and extends with right angle to the sides of the cores to create stray magnetic path for each lamination layer. The mechanism of the proposed ferrite has been analyzed, showing that the stray flux can be redirected by the ferrite shielding structure from the ribbon-based cores into the air in a way with reduced eddy current loss. The tests with proposed shielding ferrite technique has validated the technique in three cases: air gapped amorphous inductor, core-type nanocrystalline transformer, and shell-type nanocrystalline transformer. Comparison with conventional method has also shown superiority on eddy current loss reduction of the proposed method. Due to the utilization on ferrite, saturation and flux crowding must be avoided to maintain the effectiveness. Further material study may be desired to enhance the effectiveness, so that a better material can be selected, such as magnetic paste.

- Dry-type insulation design for MV transformer and inductor is proposed. The insulating materials are characterized with proposed test samples to gain the dielectric performance which is important for insulation design. The

dry-type insulation structure for MV transformers and inductors are then introduced. The MV winding partial shielding method with reduced parasitic CM capacitance is discussed. The field grading and potting process for shielding edges are also proposed and validated. The simplified vacuum potting process, for MV transformer and inductor windings is also provided to facilitate implementation in laboratory environment. The PD test results of MV DAB transformer and MV inductor for flying capacitor inverter validates the overall structural design and proposed partial shielding, field grading, and the vacuum encapsulation process.

- A CM switching loss reduction method by diode-clamped grounding is proposed for conversion systems based on CHB converters. The mechanism of the CM loss has been studied at first, and the CM loss remains constant, and is not affected by the load or CHB soft-switching conditions. The operating principle of the diode-clamped circuitry for CHB is also discussed. With the proposed method, the CM switching loss of CHB can be effectively reduced, and the closer of the MV/LV ratio to unity, the better loss reduction can be achieved. Theoretical analysis has been performed including diode parasitics capacitance, loop impedance, and gate driving delays, among which the diode junction energy and gate signal delays may have high impact and should be carefully considered.

- A compact MV power stage design strategy with heatsink field shaping has been developed. To achieve high compactness, the proposed heatsink field shaping

has to be implemented. By adding rounded angles to the heatsinks, the electric field hotspot can be rendered, and breakdown voltage can be increased by 33%. With the bumping air duct design, both mechanical support and extra creepage distance can also be provided. Moreover, a simplified gate drive design for 10-kV discrete device using commercial gate driving solution has been proposed, along with adaption to the embedded DESAT protection. Finally, the compact MV power stage can be built with volume reduction by 30% with extra DC-link capacitance.

- A DC-blocking capacitor-less MV DAB transformer flux balancing strategy is finally proposed. A ferrite-gapped DAB transformer scheme is proposed to generate current harmonics for the flux unbalance detection. The magnetizing current harmonics of MV transformers with non-linear magnetic gaps has been modeled and the relation between flux unbalance and harmonics is derived. The flux unbalance detection based on magnetizing current harmonics as well as the flux balancing control strategy are also proposed and demonstrated in converter tests. The proposed flux detection method can be suitable for MV converters as the required sensor resolution and noise level are relatively low, which can be easier to achieve in MV DAB converters.

8.2 Future Work

- For the eddy current loss, further modeling may be needed to quantitatively estimate the loss that is induced by the core surface eddy current. The difficulties due to the core non-linear property, narrow skin depth, and time variant on have to be considered to model the phenomenon accurately in the time domain. The time consuming process of the current simulation methodology needs also to be improved, since the core property has to be anisotropic, and multi local coordinates are required to model the core corners, slowing down and overly complicating the simulation process. A lumped circuit model may be also desirable to investigate detailed waveform change in converter level simulations.

- For ferrite shielding and of laminated cores, advanced material and shielding technology are needed to improve the effectiveness of flux redirection and eddy current reduction. The current method relying on ferrite plates or customized ferrite parts have the limitation of unwanted air gaps and dimensional deviations, which creates high reluctance in the flux re-directional loop, causing the flux redirection and eddy current reduction to be incomplete. Possible ways include to use ferrite powder sintering on the surface of laminated cores, as well as specially machined and assembled metal laminated cores so that the surfaces are partitioned and further laminated in multi-directions to limit the eddy current.

- For transformer insulation development, better cooling design integrated with dry-type insulation is also required, since the thermal conductivity of both the 3D printing and potting polymer materials are relatively low. Moreover, a more complete way to reduce the parasitic loss is desirable. As it is always possible that the ratio of low voltage side and high voltage side DC-link voltages is high, the reduction by diode clamping can be relatively low compared to the extra switching loss induced.

- For harmonic-based DAB transformer flux balancing, a simplified way of detection is preferable since the proposed detection method involves two current sensors and analog signal processing, which is still resource consuming and noise susceptible. Furthermore, the potential method should also provide more information of the DAB converter, such as the winding/output current, ZVS realization, which can be used for DAB converter control beyond maintaining balanced transformer flux.

Bibliography

[1] "Eia projects nearly 50% increase in world energy usage by 2050, led by growth in asia," Sept 2019. [Online]. Available: https://www.eia.gov/todayinenergy/detail.php?id=41433

[2] X. Yu, C. Cecati, T. Dillon, and M. G. Simões, "The new frontier of smart grids," *IEEE Industrial Electronics Magazine*, vol. 5, no. 3, pp. 49–63, 2011.

[3] F. Wang, Z. Gao, H. Li, Y. Ma, S. Ji, Y. Su, and Z. Yang, "Sic based modular transformer-less mw-scale power conditioning system and control for flexible chp system," Report, 2023-03-30 2023. [Online]. Available: https://www.osti.gov/biblio/1963762https://www.osti.gov/servlets/purl/1963762

[4] H. Li, Z. Gao, F. Wang, Y. Ma, Y. Su, D. Li, P. Yao, S. Ji, Z. Yang, and R. Chen, "Design, development, and testing of a flexible combined heat and power (f-chp) system with 10-kv sic mosfet-based power conditioning system (pcs) converter," *IEEE Access*, vol. 11, pp. 134 769–134 793, 2023.

[5] Z. Lu, C. Li, A. Zhu, H. Luo, C. Li, W. Li, and X. He, "Medium voltage soft-switching dc/dc converter with series-connected sic mosfets," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1451–1462, 2021.

[6] M. Stojadinović, E. Kalkounis, F. Jauch, and J. Biela, "Generalized pwm generator with transformer flux balancing for dual active bridge converter," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, Conference Proceedings, pp. P.1–P.10.

[7] D. Dong, L. Garces, M. Agamy, Y. Pan, X. Wu, H. She, H. Xu, X. Li, and J. Dai, "Control and operation of medium-voltage high-power bi-directional resonant dc-dc converters in shipboard dc distribution systems," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, Conference Proceedings, pp. 1–9.

[8] S. Ji, S. Zheng, F. Wang, and L. M. Tolbert, "Temperature-dependent characterization, modeling, and switching speed-limitation analysis of third-generation 10-kv sic mosfet," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4317–4327, 2018.

[9] B. Passmore, Z. Cole, B. McGee, M. Wells, J. Stabach, J. Bradshaw, R. Shaw, D. Martin, T. McNutt, E. VanBrunt, B. Hull, and D. Grider, "The next generation of high voltage (10 kv) silicon carbide power modules," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, Conference Proceedings, pp. 1–4.

[10] Z. Guo, R. Yu, W. Xu, X. Feng, and A. Q. Huang, "Design and optimization of a 200-kw medium-frequency transformer for medium voltage sic pv inverters," *IEEE Transactions on Power Electronics*, pp. 1–1, 2021.

[11] T. B. Gradinger, U. Drofenik, and S. Alvarez, "Novel insulation concept for an mv dry-cast medium-frequency transformer," in *2017 19th European*

Conference on Power Electronics and Applications (EPE'17 ECCE Europe), 2017, Conference Proceedings, pp. P.1–P.10.

[12] Q. Chen, R. Raju, D. Dong, and M. Agamy, "High frequency transformer insulation in medium voltage sic enabled air-cooled solid-state transformers," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Conference Proceedings, pp. 2436–2443.

[13] L. Heinemann, "An actively cooled high power, high frequency transformer with high insulation capability," in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, vol. 1, 2002, Conference Proceedings, pp. 352–357 vol.1.

[14] S. Lu, D. Kong, S. Xu, L. Luo, and S. Li, "A high-efficiency 80-kw split planar transformer for medium-voltage modular power conversion," *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 8762–8766, 2022.

[15] R. Wang, Z. Shen, C. Zhang, B. Zhang, and P. Barbosa, "Planar structure high-frequency transformer design for medium voltage applications," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022, Conference Proceedings, pp. 1–6.

[16] Z. Li, F. Jin, X. Lou, Y. H. H. Q. Li, and F. C. Lee, "Design and optimization with litz wire version of pcb in solid-state transformer," in *2024*

IEEE Applied Power Electronics Conference and Exposition (APEC), 2024, Conference Proceedings, pp. 1453–1459.

[17] B. Cougo and J. W. Kolar, "Integration of leakage inductance in tape wound core transformers for dual active bridge converters," in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, 2012, Conference Proceedings, pp. 1–6.

[18] R. B. Beddingfield, S. Bhattacharya, and P. Ohodnicki, "Shielding of leakage flux induced losses in high power, medium frequency transformers," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, Conference Proceedings, pp. 4154–4161.

[19] Z. Gao, H. Li, and F. Wang, "A medium-voltage transformer with integrated leakage inductance for 10 kv sic-based dual-active-bridge converter," in *2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, 2022, Conference Proceedings, pp. 221–226.

[20] Z. Gao, R. Chen, D. Li, and F. Wang, "Switching loss reduction on cascaded h-bridge converter with diode clamped transformer grounding scheme," in *2023 IEEE 10th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, 2023, Conference Proceedings, pp. 1–5.

[21] Y. Zhou, B. Qi, M. Zheng, and B. Cong, "A novel dc bias suppression strategy for single-phase full-bridge dc-dc arc welding converter," 2021.

[22] P. Yao, X. Jiang, P. Xue, S. Ji, and F. Wang, "Flux balancing control of ungapped nanocrystalline core-based transformer in dual active bridge converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11 463–11 474, 2020.

[23] X. Li, W. Huang, B. Cui, and X. Jiang, "Inductance characteristics of the high-frequency transformer in dual active bridge converters," in *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, 2019, Conference Proceedings, pp. 1–5.

[24] H. Neubert, J. Ziske, T. Heimpold, and R. Disselnkötter, "Homogenization approaches for laminated magnetic cores using the example of transient 3d transformer modeling," 2013.

[25] C. Chen, Z. Guo, R. Yu, and A. Q. Huang, "A novel hybrid core structure for 100kw medium frequency transformers," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, Conference Proceedings, pp. 5651–5657.

[26] Z. Gao and F. Wang, "Ferrite shielding for eddy current suppression on inductors and transformers using ribbon-based magnetic cores," in *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2024, Conference Proceedings, pp. 7167–7174.

[27] Z. Gao, D. Li, R. Chen, H. Bai, L. Tolbert, and F. Wang, "Design of a 50-kw medium frequency medium voltage transformer for 10-kv sic-based dual active bridge converter," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, Conference Proceedings, pp. 5839–5845.

[28] R. Chen, M. Lin, Z. Gao, Y. Xu, M. A. Sager, F. Wang, H. Bai, and L. M. Tolbert, "A high power density mw-level medium voltage eight-level flying capacitor converter," in *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2024, Conference Proceedings, pp. 3457–3464.

[29] H. Li, P. Yao, Z. Gao, and F. Wang, "Medium voltage converter inductor insulation design considering grid requirements," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 2339–2350, 2022.

[30] J. E. Huber and J. W. Kolar, "Common-mode currents in multi-cell solid-state transformers," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, Conference Proceedings, pp. 766–773.

[31] H. Li, Z. Gao, and F. Wang, "A pwm strategy for cascaded h-bridges to reduce the loss caused by parasitic capacitances of medium voltage dual active bridge transformers," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022, Conference Proceedings, pp. 1–6.

[32] L. Ravi, X. Lin, Y. Xu, D. Dong, and R. Burgos, "Analysis of alternative baseplate-to-heatsink grounding schemes in 10 kv sic mosfet modules with

series-connected devices," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, Conference Proceedings, pp. 1456–1463.

[33] Y. Xu, J. Stewart, H. Song, L. Cheng, I. Cvetkovic, R. Burgos, and D. Boroyevich, "High power density medium-voltage converter integration via electric field management," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 1, pp. 895–905, Feb. 2022.

[34] Z. Gao, R. Chen, H. Bai, L. Tolbert, and F. Wang, "A compact power stage design for 10-kv sic device-based converters with heatsink electric field shaping," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, Conference Proceedings, pp. 2580–2585.

[35] P. Yao, X. Jiang, P. Xue, S. Li, S. Lu, and F. Wang, "Design optimization of medium frequency transformer for dab converters with dc bias capacity," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2020.

[36] G. Qiu, L. Ran, H. Jiang, T. Long, A. Forsyth, and W. Shao, "A method for detecting dc bias in transformer of dual active bridge dc-dc converter," in *2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia)*, 2021, Conference Proceedings, pp. 714–719.

[37] G. Ortiz, L. Fässler, J. W. Kolar, and O. Apeldoorn, "Application of the magnetic ear for flux balancing of a 160kw/20khz dc-dc converter transformer,"

in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, Conference Proceedings, pp. 2118–2124.

[38] S. Klopper and J. A. Ferreira, "A sensor for balancing flux in converters with a high-frequency transformer link," *IEEE Transactions on Industry Applications*, vol. 33, no. 3, pp. 774–779, 1997.

[39] L. Schrittwieser, M. Mauerer, D. Bortis, G. Ortiz, and J. W. Kolar, "Novel principle for flux sensing in the application of a dc + ac current sensor," *IEEE Transactions on Industry Applications*, vol. 51, no. 5, pp. 4100–4110, 2015.

[40] D. Wilson, "A new pulsewidth modulation method inherently maintains output transformer flux balance," in *8th Nat. Solid-State Power Convers. Conf.*, vol. D1, Conference Proceedings, pp. 1–14.

[41] Y. Panov, M. M. Jovanović, and B. T. Irving, "Novel transformer-flux-balancing control of dual-active-bridge bidirectional converters," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, Conference Proceedings, pp. 42–49.

[42] Z. Xiaoxin, L. Huiqi, L. Yang, Z. Xiaojun, and C. Zhiguang, "Analysis of the dc bias phenomenon by the harmonic balance method based on the electromagnetic coupling model," in *2013 IEEE INTERNATIONAL CONFERENCE ON MICROWAVE TECHNOLOGY & COMPUTATIONAL ELECTROMAGNETICS*, 2013, Conference Proceedings, pp. 387–390.

[43] 2011. [Online]. Available: https://metglas.com/wp-content/uploads/2021/06/2605SA1-Magnetic-Alloy-Updated.pdf

[44] 2021. [Online]. Available: https://www.fair-rite.com/67-material-data-sheet/

[45] Z. Gao, P. Yao, H. Li, S. Ji, Z. Yang, F. Wang, and Y. Ma, "A transformer flux balancing scheme based on magnetizing current harmonic in dual-active-bridge converters," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, Conference Proceedings, pp. 1894–1899.

[46] Z. Gao, P. Yao, H. Li, and F. Wang, "A flux balancing strategy for 10-kv sic-based dual-active-bridge converter," in *2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, 2022, Conference Proceedings, pp. 148–153.

[47] H. Li, Z. Gao, S. Ji, Y. Ma, and F. Wang, "An inrush current limiting method for grid-connected converters considering grid voltage disturbances," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 2608–2618, 2022.

[48] Q. Yang, M. Steurer, S. Song, M. Pickles, J. Hauer, M. Bosworth, N. Bonaventura, Y. He, M. Coleman, K. Schoder, Y. Shi, and L. Graber, "Modeling and experiments of a nonlinear inductor-based fault current commutation strategy for a hybrid dc circuit breaker," in *2024 IEEE Applied*

Power Electronics Conference and Exposition (APEC), 2024, Conference Proceedings, pp. 965–970.

[49] H. Li, Z. Gao, Z. Yang, C. Nie, and F. Wang, "A medium voltage testbed for the performance and function tests of a 13.8 kv power conditioning system converter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, Conference Proceedings, pp. 757–763.

[50] H. Li, D. Li, Z. Gao, Y. Ma, Z. Yang, J. Wang, and F. Wang, "Development of a power electronics-based testbed for a flexible combined heat and power system," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, Conference Proceedings, pp. 764–770.

[51] Y. He, Y. Li, Q. Yang, R. B. Gonzatti, A. Taylor, and F. Peng, "Grid-connected converter without interfacing filters: Principle, analysis and implementation," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, Conference Proceedings, pp. 4505–4511.

[52] Q. Huang, Y. Yang, Y. Lai, Z. Ma, and S. Wang, "A survey of cm emi modeling and reduction technique of transformer for isolated converters," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, Conference Proceedings, pp. 1484–1490.

[53] J. Niu, J. Wang, Z. Gao, R. B. Martin, W. B. Giewont, and F. Wang, "Modular multilevel converter based reconfigurable ac load emulator," in *2021 IEEE 12th*

Energy Conversion Congress Exposition - Asia (ECCE-Asia), 2021, Conference Proceedings, pp. 438–442.

[54] R. Chen, M. Lin, D. Li, Z. Gao, F. Wang, H. Bai, and L. M. Tolbert, "A si igbt circuit breaker for protection of 10 kv sic mosfet power module," in *2023 IEEE 10th Workshop on Wide Bandgap Power Devices Applications (WiPDA)*, 2023, Conference Proceedings, pp. 1–6.

[55] A. Li, D. Jiang, Z. Gao, W. Kong, S. Jia, and R. Qu, "Three-phase four-leg drive for dc-biased sinusoidal current vernier reluctance machine," *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2758–2769, 2019.

[56] A. Li, Z. Gao, D. Jiang, W. Kong, and R. Qu, "Drive system with asymmetrical power electronics devices for novel reluctance machines with dc-biased sinusoidal current," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 4, pp. 2303–2313, 2019.

[57] A. Li, Z. Gao, D. Jiang, W. Kong, S. Jia, and R. Qu, "Three-phase four-leg drive for dc-biased sinusoidal current vernier reluctance machine," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, Conference Proceedings, pp. 1236–1241.

[58] A. Li, Z. Gao, D. Jiang, S. Jia, R. Qu, and W. Kong, "Drive for dc-biased sinusoidal current vernier reluctance motors with asymmetrical power

electronics devices," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, Conference Proceedings, pp. 3725–3730.

[59] R. Chen, D. Li, M. Lin, M. A. Sager, Z. Gao, F. Wang, H. Bai, and L. M. Tolbert, "Design of 10 kv sic mosfet power module based mw-level modular multilevel converter phase-leg," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, Conference Proceedings, pp. 1087–1094.

[60] ——, "Switching cell design for medium voltage flying capacitor converter with 10 kv sic mosfet," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, Conference Proceedings, pp. 2468–2474.

[61] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kv sic-based 7 kv/400 v dc transformer for future data centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753–767, 2019.

[62] A. Anurag, S. Acharya, S. Bhattacharya, T. R. Weatherford, and A. Parker, "A gen-3 10 kv sic mosfets based medium voltage three-phase dual active bridge converter enabling a mobile utility support equipment solid state transformer (muse-sst)," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2021.

[63] K. Mainali, A. Tripathi, S. Madhusoodhanan, A. Kadavelugu, D. Patel, S. Hazra, K. Hatua, and S. Bhattacharya, "A transformerless intelligent power substation: A three-phase sst enabled by a 15-kv sic igbt," *IEEE Power Electronics Magazine*, vol. 2, no. 3, pp. 31–43, 2015.

[64] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer—medium voltage prototype," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3257–3268, 2014.

[65] Z. Li, Y. H. Hsieh, Q. Li, F. C. Lee, and M. H. Ahmed, "High-frequency transformer design with high-voltage insulation for modular power conversion from medium-voltage ac to 400-v dc," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Conference Proceedings, pp. 5053–5060.

[66] T. Guillod, R. Faerber, D. Rothmund, F. Krismer, C. M. Franck, and J. W. Kolar, "Dielectric losses in dry-type insulation of medium-voltage power electronic converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2019.

[67] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," in *2007 European Conference on Power Electronics and Applications*, 2007, Conference Proceedings, pp. 1–10.

[68] L. Zheng, X. Han, Z. An, R. P. Kandula, K. Kandasamy, M. Saeedifard, and D. Divan, "Sic-based 5-kv universal modular soft-switching solid-state transformer (m-s4t) for medium-voltage dc microgrids and distribution grids," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11 326–11 343, 2021.

[69] M. Kaymak, R. W. D. Doncker, and T. Jimichi, "Design and verification of a medium-frequency transformer in a three-phase dual-active bridge dc-dc converter for medium-voltage grid connection of offshore wind farms," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, Conference Proceedings, pp. 2694–2701.

[70] [Online]. Available: https://www.hitachi-metals.co.jp/products/elec/tel/pdf/hl-fm9-h.pdf

[71] Z. Li, F. Jin, Y. H. Hsieh, and Q. Li, "A high-frequency pcb-winding transformer design with medium voltage insulation for solid-state transformer," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, Conference Proceedings, pp. 1536–1542.

[72] Z. Li, F. Jin, X. Lou, Y. H. Hsieh, Q. Li, and F. C. Lee, "A transformer design with pcb litz wire concept for solid state transformer," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, Conference Proceedings, pp. 848–854.

[73] X. Liu, H. Peng, and L. M. Tolbert, "An ac-dc converter with maximum power tracking for multi-input electromagentic energy harvester," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, Conference Proceedings, pp. 3266–3272.

[74] ——, "An ac-dc converter with maximum power tracking for multi-input electromagentic energy harvester," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 3266–3272.

[75] Y. Lai, S. Wang, and B. Zhang, "Investigation of magnetic field immunity and near magnetic field reduction for the inductors in high power density design," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5340–5351, 2019.

[76] R. Chen, M. Lin, D. Li, Z. Gao, F. Wang, H. Bai, and L. M. Tolbert, "Analysis of 10 kv sic mosfet module baseplate parasitic capacitance impact on switching loss," in *2023 IEEE 10th Workshop on Wide Bandgap Power Devices Applications (WiPDA)*, 2023, Conference Proceedings, pp. 1–6.

[77] Y. Yang, Y. Lai, S. Wang, and Z. Luo, "Modeling and prediction of low-frequency near-field radiation for a power converter based on the operating principle of a monopole antenna," *IEEE Transactions on Power Electronics*, vol. 39, no. 11, pp. 14 387–14 397, 2024.

[78] B. Zhang, S. Wang, Y. Lai, and Y. Yang, "Modeling and prediction of low-frequency radiated emi for a sic motor drive system," *IEEE Transactions on*

Industrial Electronics, vol. 71, no. 9, pp. 10 210–10 220, 2024.

[79] R. Doebbelin, M. Benecke, and A. Lindemann, "Calculation of leakage inductance of core-type transformers for power electronic circuits," in *2008 13th International Power Electronics and Motion Control Conference*, 2008, Conference Proceedings, pp. 1280–1286.

[80] D. De, C. Klumpner, M. Rashed, C. Patel, P. Kulsangcharoen, and G. Asher, "Achieving the desired transformer leakage inductance necessary in dc-dc converters for energy storage applications," in *6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012)*, 2012, Conference Proceedings, pp. 1–6.

[81] S. A. Ansari, J. N. Davidson, and M. P. Foster, "Fully-integrated solid shunt planar transformer for llc resonant converters," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 26–35, 2022.

[82] D. E. Gaona, C. Jiang, and T. Long, "Highly efficient 11.1-kw wireless power transfer utilizing nanocrystalline ribbon cores," *IEEE Transactions on Power Electronics*, vol. 36, no. 9, pp. 9955–9969, 2021.

[83] G. Calderon-Lopez, Y. Wang, and A. J. Forsyth, "Mitigation of gap losses in nanocrystalline tape-wound cores," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4656–4664, 2019.

[84] Y. Wang, G. Calderon-Lopez, and A. J. Forsyth, "High-frequency gap losses in nanocrystalline cores," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4683–4690, 2017.

[85] S. Zheng, J. Wang, F. Wang, and L. M. Tolbert, "Dc-saturated continuously variable series reactors (cvsrs) for power flow control in power transmission systems," *IEEE Transactions on Power Delivery*, vol. 37, no. 1, pp. 268–278, 2022.

[86] L. Liu, T. Ge, K. D. T. Ngo, Y. Mei, and G. Q. Lu, "Ferrite paste cured with ultraviolet light for additive manufacturing of magnetic components for power electronics," *IEEE Magnetics Letters*, vol. 9, pp. 1–5, 2018.

[87] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer—medium voltage prototype," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3257–3268, 2014.

[88] M. Jaritz and J. Biela, "Isolation design of a 14.4kv, 100khz transformer with a high isolation voltage (115kv)," in *2016 IEEE International Power Modulator and High Voltage Conference (IPMHVC)*, 2016, Conference Proceedings, pp. 73–78.

[89] N. Djekanovic and D. Dujic, "Copper pipes as medium frequency transformer windings," *IEEE Access*, vol. 10, pp. 109 431–109 445, 2022.

[90] S. Isler, T. Chaudhuri, D. Aguglia, and X. A. Bonnin, "Development of a 100 kw, 12.5 kv, 22 khz and 30 kv insulated medium frequency transformer for compact and reliable medium voltage power conversion," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, Conference Proceedings, pp. P.1–P.10.

[91] Z. Li, E. Hsieh, Q. Li, and F. C. Lee, "High-frequency transformer design with medium-voltage insulation for resonant converter in solid-state transformer," *IEEE Transactions on Power Electronics*, vol. 38, no. 8, pp. 9917–9932, Aug. 2023.

[92] L. Zheng, X. Han, Z. An, R. P. Kandula, K. Kandasamy, M. Saeedifard, and D. Divan, "Sic-based 5-kv universal modular soft-switching solid-state transformer (m-s4t) for medium-voltage dc microgrids and distribution grids," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11 326–11 343, 2021.

[93] L. Heinemann, "An actively cooled high power, high frequency transformer with high insulation capability," in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, vol. 1, 2002, Conference Proceedings, pp. 352–357 vol.1.

[94] T. Guillod, F. Krismer, and J. W. Kolar, "Electrical shielding of mv/mf transformers subjected to high dv/dt pwm voltages," in *2017 IEEE Applied*

Power Electronics Conference and Exposition (APEC), 2017, Conference Proceedings, pp. 2502–2510.

[95] Formlabs, "Rigid 10k resin technical data sheet," Report, 2020/07/10 2020. [Online]. Available: https://media.formlabs.com/m/522eb50e6c8ac0e3/original/-ENUS-Rigid-10K-TDS.pdf

[96] Dow, "Dowsil™ tc-4605 hlv technical data sheet," Report, 2023/05/15 2023. [Online]. Available: https://ecommapi.krayden.com/Content/pdf/datasheet/dow_tc_4605_hlv_tds.pdf

[97] H. Li, P. Yao, Z. Gao, and F. Wang, "Medium voltage converter inductor insulation design considering grid insulation requirements," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, Conference Proceedings, pp. 2120–2126.

[98] "Ieee standard test code for dry-type distribution and power transformers," *IEEE Std C57.12.91-2020 (Revision of IEEE Std C57.12.91-2011)*, pp. 1–102, 2021.

[99] Y. Lai, S. Wang, Y. Yang, Q. Huang, and Z. Ma, "Review on modeling and emissions from emi filters in power electronics: Inductors," in *2023 IEEE Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMC+SIPI)*, 2023, Conference Proceedings, pp. 566–572.

[100] Z. Ma, Y. Lai, Y. Yang, Q. Huang, and S. Wang, "Review of radiated emi modeling and mitigation techniques in power electronics systems," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, Conference Proceedings, pp. 1776–1783.

[101] Y. Yang, Q. Huang, Y. Lai, Z. Ma, Y. Liu, and S. Wang, "Analysis and modeling of the near magnetic field distribution of toroidal inductors," in *2023 IEEE Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMC+SIPI)*, 2023, Conference Proceedings, pp. 573–578.

[102] Y. Lai, Y. Yang, S. Wang, and Z. Luo, "Modeling of low-frequency radiated emi from the inductors of power converters in electric vehicles," *IEEE Transactions on Transportation Electrification*, vol. 11, no. 2, pp. 6904–6915, 2025.

[103] Y. Lai, S. Wang, Y. Yang, Q. Huang, and Z. Luo, "Modeling, analysis and reduction of radiated emi due to the pulsating voltage on pcb ground plane in a non-isolated power converter," in *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2024, Conference Proceedings, pp. 4874–4881.

[104] J. Zhu, Y. He, B. Zhou, and Y. Li, "Modeling of rail transit earth current distribution at neutral point of ac grounding transformer," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, Conference Proceedings, pp. 3145–3150.

[105] H. Li, Z. Gao, R. Chen, and F. Wang, "Improved double pulse test for accurate dynamic characterization of medium voltage sic devices," *IEEE Transactions on Power Electronics*, vol. 38, no. 2, pp. 1779–1790, 2023.

[106] Z. Guo, H. Li, F. Z. Peng, M. Steurer, and K. J. Olejniczak, "Gate driver development and stray inductance extraction of 10 kv sic mosfet module for a switched-capacitor mmc application," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, Conference Proceedings, pp. 1387–1393.

[107] J. Wang, S. Mocevic, J. Hu, Y. Xu, C. DiMarino, I. Cvetkovic, R. Burgos, and D. Boroyevich, "Design and testing of 6 kv h-bridge power electronics building block based on 10 kv sic mosfet module," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, 2018, Conference Proceedings, pp. 3985–3992.

[108] X. Huang, S. Ji, D. Li, C. Nie, L. M. Tolbert, F. Wang, and W. Giewont, "Analysis and gate driver design considerations of 10 kv sic mosfets under flashover fault due to insulation failure," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, Conference Proceedings, pp. 2842–2849.

[109] Y. Yang, Y. Lai, Q. Huang, and S. Wang, "Modeling and reduction of radiated emission caused by isolated gate drivers in wide bandgap half-bridge-based

power modules," in *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2024, Conference Proceedings, pp. 7013–7020.

[110] H. Li, Z. Gao, and F. Wang, "Medium-voltage isolated auxiliary power supply design for high insulation capability, ultra-low coupling capacitance, and small size," *IEEE Transactions on Power Electronics*, vol. 38, no. 6, pp. 7226–7240, 2023.

[111] Z. Guo and H. Li, "A 20mhz-transformer-based isolated gate driver for 3.3kv sic mosfets," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, Conference Proceedings, pp. 2480–2484.

[112] E. P. Eni, T. Kerekes, C. Uhrenfeldt, R. Teodorescu, and S. Munk-Nielsen, "Design of low impedance busbar for 10 kv, 100a 4h-sic mosfet short-circuit tester using axial capacitors," in *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2015, Conference Proceedings, pp. 1–5.

[113] H. Li, Z. Gao, and F. Wang, "Design and demonstration of an 850 v dc to 13.8 kv ac 100 kw three-phase four-wire power conditioning system converter using 10 kv sic mosfets," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, Conference Proceedings, pp. 989–994.

[114] L. Shu, W. Chen, Z. Lin, D. Ma, X. He, and W. A. Syed, "Dc bias study for dc-dc dual-active-bridge converter," in *2018 IEEE 4th Southern Power Electronics*

Conference (SPEC), 2018, Conference Proceedings, pp. 1–5.

[115] L. Shu, W. Chen, and Z. Song, "Prediction method of dc bias in dc-dc dual-active-bridge converter," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 2, pp. 152–162, 2019.

[116] D. Yuan, J. Yang, Y. Liu, Y. Jia, R. Liu, and Z. Song, "A prediction method of dc bias for dc-dc dual-active-bridge converter with mosfets," in *2019 14th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 2019, Conference Proceedings, pp. 1228–1232.

[117] Y. Panov, M. M. Jovanović, L. Gang, and M. Yueyong, "Transformer-flux-balancing control in isolated bidirectional dc-dc converters," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, Conference Proceedings, pp. 49–56.

[118] Z. Wang, J. Chai, and X. Sun, "Method to control flux balancing of high-frequency transformers in dual active bridge dc–dc converters," *The Journal of Engineering*, vol. 2018, no. 17, pp. 1835–1843, 2018.

[119] G. Ortiz, L. Fässler, J. W. Kolar, and O. Apeldoorn, "Flux balancing of isolation transformers and application of "the magnetic ear" for closed-loop volt–second compensation," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4078–4090, 2014.

[120] F. P. Dawson, "Dc-dc converter interphase transformer design considerations: volt-seconds balancing," *IEEE Transactions on Magnetics*, vol. 26, no. 5, pp. 2250–2252, 1990.

[121] L. Zhu, H. Bai, A. Brown, and M. McAmmond, "Design a 400 v–12 v 6 kw bidirectional auxiliary power module for electric or autonomous vehicles with fast precharge dynamics and zero dc-bias current," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5323–5335, 2021.

[122] D. Costinett, D. Seltzer, D. Maksimovic, and R. Zane, "Inherent volt-second balancing of magnetic devices in zero-voltage switched power converters," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Conference Proceedings, pp. 9–15.

[123] C. Winter, J. Riedel, Z. Mohzani, R. Mencher, and S. Butzmann, "Enhancing inherent flux balancing in a dual-active bridge using adaptive modulation," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, Conference Proceedings, pp. 2202–2209.

[124] P. B. Steckler, J. Y. Gauthier, X. Lin-Shi, and F. Wallart, "Polynomial multi-variable control strategy for flux balancing in dual active bridge converter," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, Conference Proceedings, pp. 1–9.

[125] B. Zhao, Q. Song, W. Liu, and Y. Zhao, "Transient dc bias and current impact effects of high-frequency-isolated bidirectional dc–dc converter in practice," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3203–3216, 2016.

[126] J. A. Claassens and I. W. Hofsajer, "A flux balancer for phase shift zvs dc-dc converters under transient conditions," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, Conference Proceedings, p. 5 pp.

Vita

Zihan Gao was born in Anqiu, Shandong, China. He obtained M.S. in Electrical Engineering degree from University of Tennessee, Knoxville, in 2022, and B.S. in Electrical Engineering degree from Huazhong University of Science and Technology, Wuhan, China, in 2018. He is now a Ph.D. student in Electrical Engineering, in the University of Tennessee, Knoxville. His research interests include medium voltage DC/DC converters and medium voltage transformers.